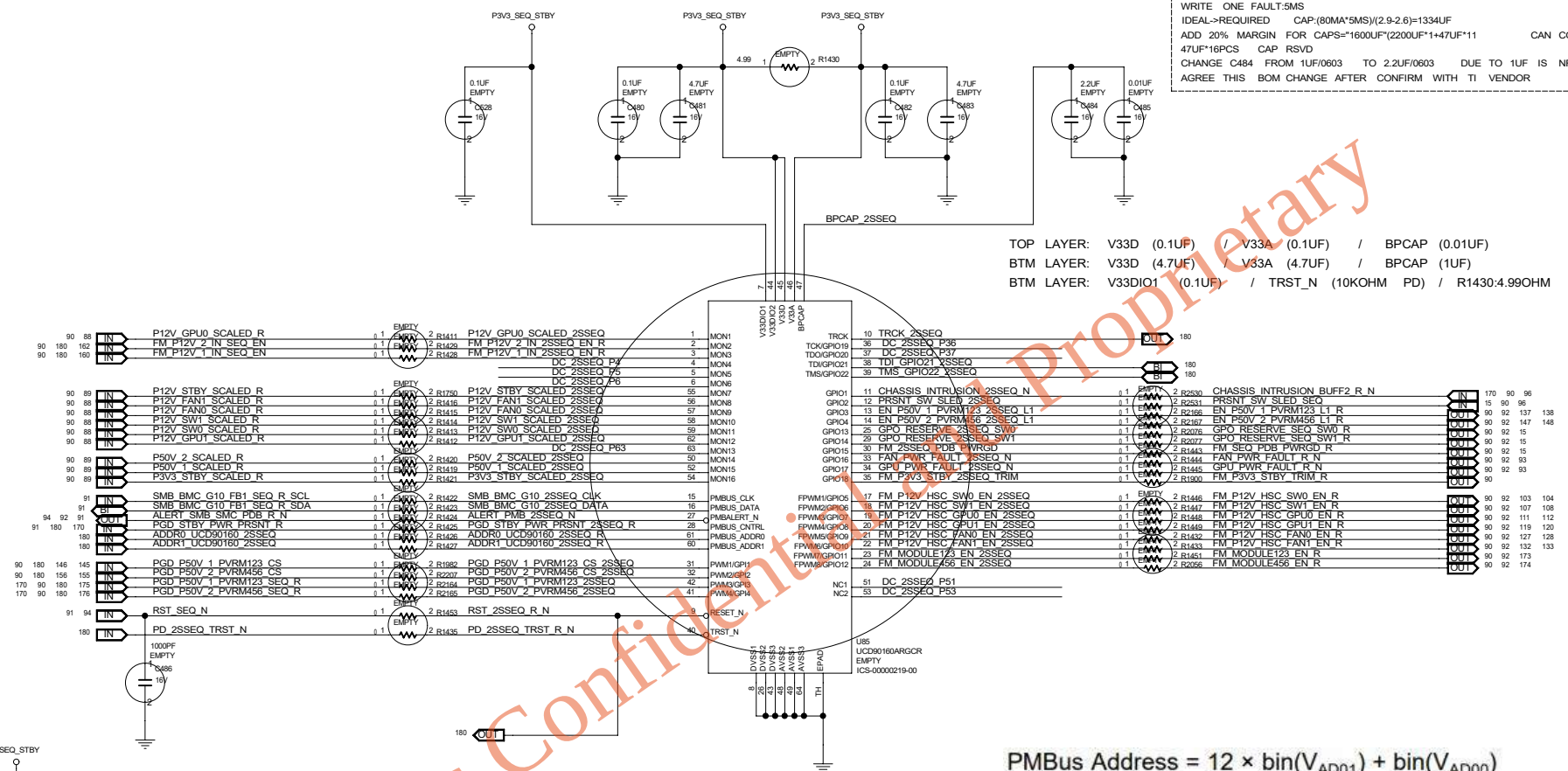
2S SEQUENCER

CO-LAYOUT 2ND SOURCE SEQUENCER WITH U79

DESIGN NOTE

VF:0.2V, P3V3_SEQ_STBY:3.3-0.2=3.1V
IPROG:80MA
VDD(AT LEAST):2.6V
VDD(TRIGGER BROWNOUT):2.9V
WRITE ONE FAULT:5MS
IDEAL->REQUIRED CAP:(80MA*5MS)/(2.9-2.6)=1334UF
ADD 20% MARGIN FOR CAPS="1600UF"(2200UF*1+47UF*11 CAN COVER)
47UF*16PCS CAP RSVD
CHANGE C484 FROM 1UF/0603 TO 2.2UF/0603 DUE TO 1UF IS NRND
AGREE THIS BOM CHANGE AFTER CONFIRM WITH TI VENDOR



TOP LAYER: V33D (0.1UF) / V33A (0.1UF) / BPCAP (0.01UF)
BTM LAYER: V33D (4.7UF) / V33A (4.7UF) / BPCAP (1UF)
BTM LAYER: V33DIO1 (0.1UF) / TRST_N (10KOHM PD) / R1430:4.99OHM

I2C ADDRESS: 0X68(8BITS)

$$\text{PMBus Address} = 12 \times \text{bin}(V_{AD01}) + \text{bin}(V_{AD00})$$

Table 8. PMBus Address Bins

ADDRESS BIN	R_{PMBus} PMBus RESISTANCE (kΩ)
open	—
11	200
10	154
9	118
8	90.9
7	69.8
6	53.6
5	41.2
4	31.6
short	—

zt Systems	DEPARTMENT	DESIGNER PAUL LEI	PROJCET RIGEL	DOCUMENT NUMBER <ZT_NUMBER>	REV 001
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