REV	ECO #	DESCRIPTION OF CHANGE	LIST PAGES MODIFIED	OWNER / DATE
REVISION	ECO NUMBER	DESCRIPTION OF CHANGE		Howard Ho
01.00	ECO-112	INITIAL ENGINEERING RELEASE		03.31.2017
01.01	ENG RELEASE	Rpelacing R166 due to long-lead time ERJ-PB3B6982V ==> 7-2176089-5	13	04.19.2017
02.00	ECO-228	Fix U50, U58 footprint; Add voltage test points; Add source terminations on clock lines; Corrected I2C nets; Updated reset lines; Added schmitt trigger to POR reset; Changed PHY addresses	9, 10, 13, 17, 18, 20, 27, 34, 35, 47-51, 53	07.28.2017
02.01	ENG RELEASE	Corrected J19 note on PG 55, Added note on 11.3G diff pairs to state that ordering is intentional on PG 35	35, 55	08.01.2017
02.02	ECO-241	Updated parts due to insufficient operating range and obsolescence (DDR3, DDR4, QSPI Flash, Kintex FPGA, Crystal)	24-49	08.10.2017
03.00	ENG RELEASE	o JTAG Daisy-chain o Replaced U64,U63 ==> U89, U90 (uni-directional) (TXB0108RGY ==> SN74AVC8T245RHLR) o Cleaned up LS1021A's POR circuit o Rearranged I2C Slave devices o Removed FPGA's controls to VTT regulator. o DNI all components that are not used. o U18 and U22: New Part IS43TR16256AL-125KBLI o U43: New Part S25FL256SAGNFI010 o Removed C1 o Changed all 11 chassis MTH to NPTH_1457H_3013P	55	10.08.2017 11.19.2017
04.00	ECO-000358	U43: Replaced S25FL256SAGNFI011 with MX66U51235FZ4I-10G	25	12.06.2017
04.01	ECO#: E00718	o DNI R787, R851 o Changed R872 from DNI to 51.1k	18, 20, 50	06.19.2018

	NAME	DATE
DRAWN		
CHECKED		
M. ENGR		
E. ENGR		
QA		
PROD		

Date Last Modified
Tuesday, June 19, 2018

SA Photonics
120 Knowles Dr
Los Gatos, CA 95032

MODEM BOARD

Size	Document Number	Rev
B	SCH-000012-00	04.01

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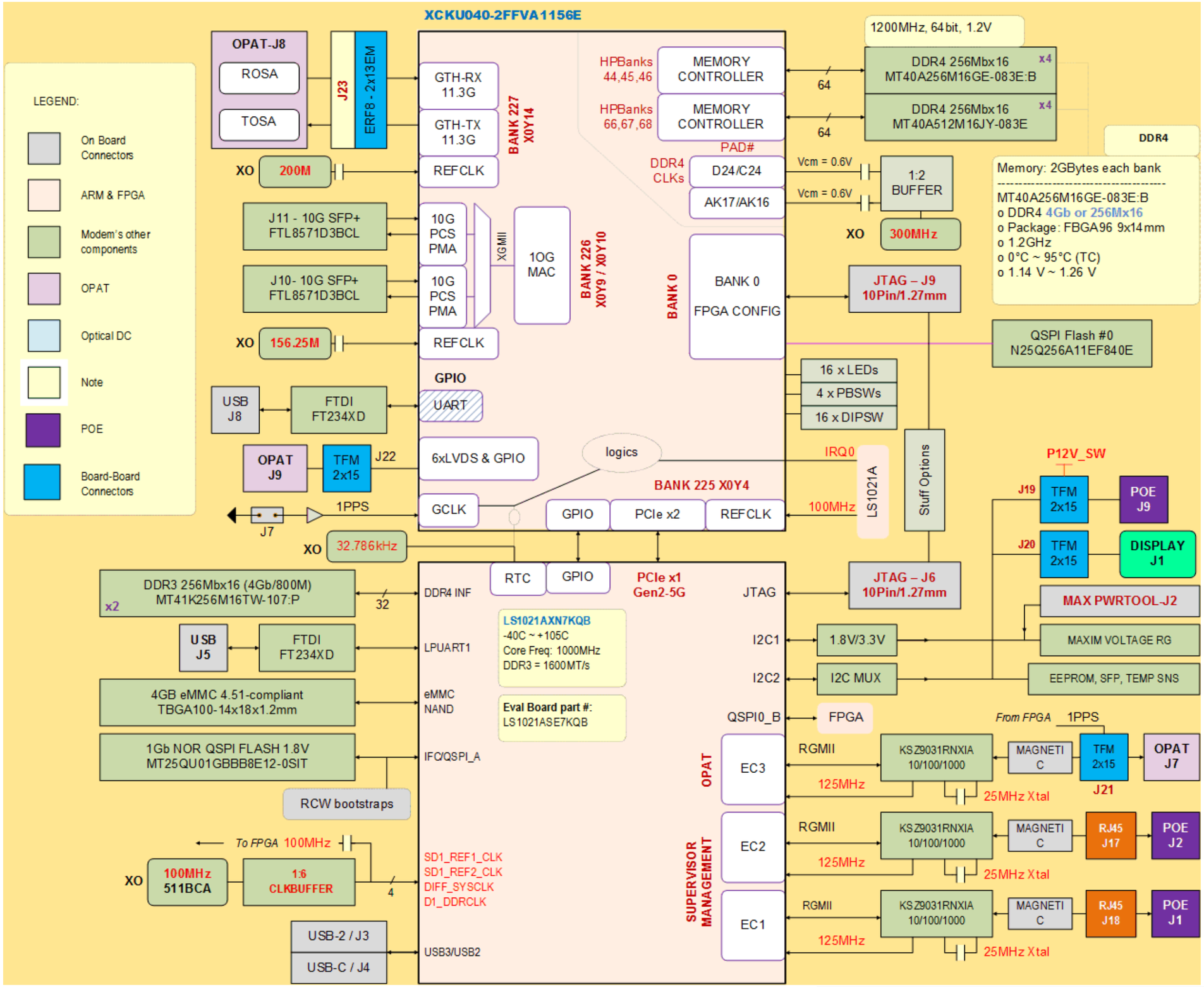
PAGE 2
MODEM BLOCK DIAGRAM



Title: PG02: MODEM BLKDGRM		
Size: Custom	Document Number: SCH-000012-00	Rev: 04.01
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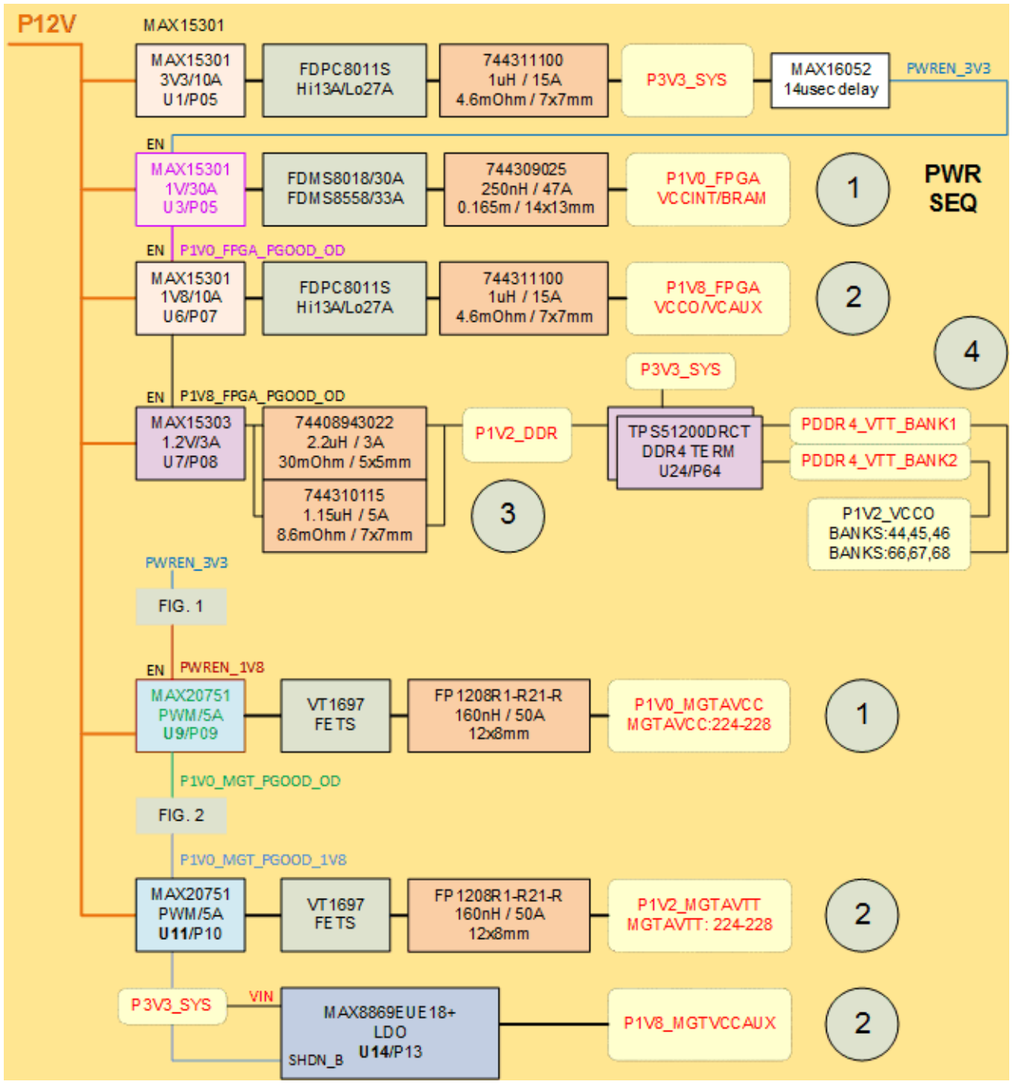
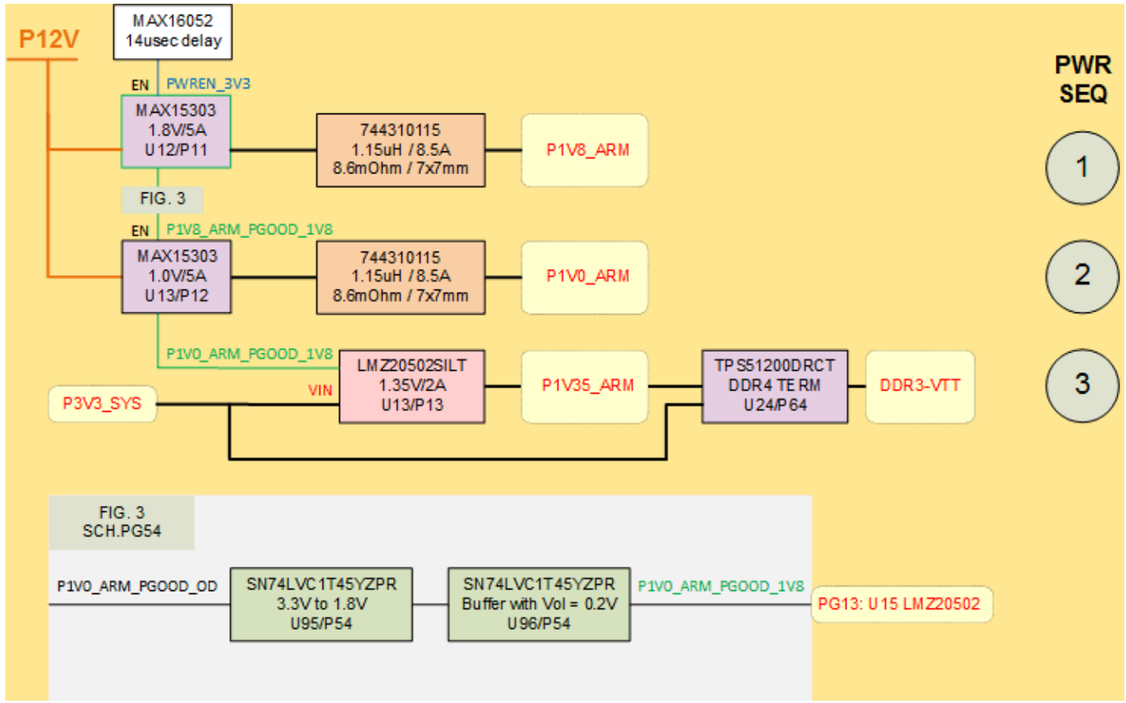
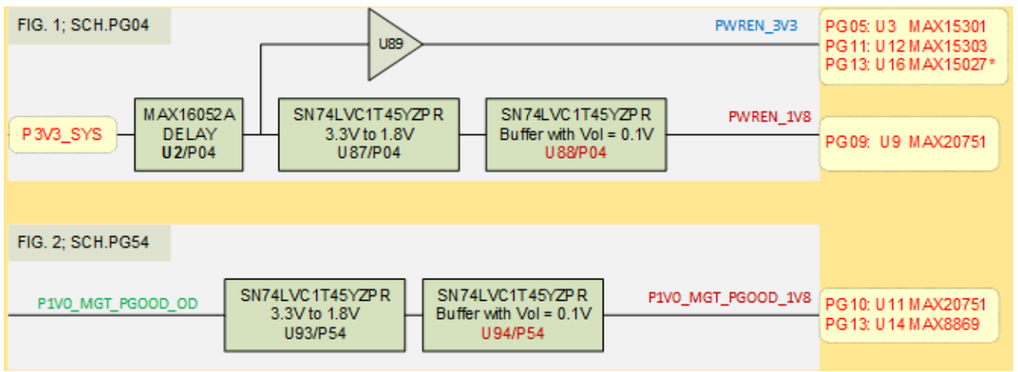
PAGE 3 POWER DESIGN

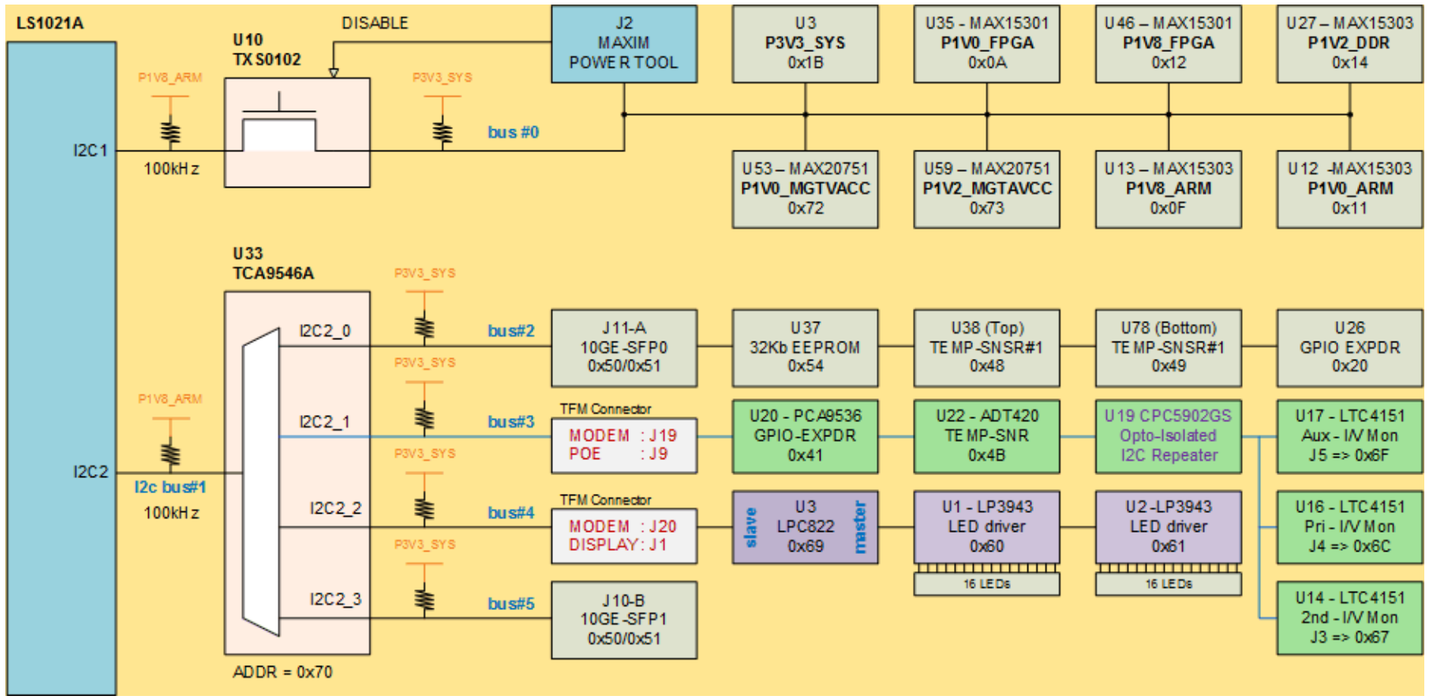






Title	PG03: POWER SEQUENCING	
Size Custom	Document Number SCH-000012-00	Rev 04.01
Date: Tuesday, June 19, 2018	Sheet 3 of 55	

I2C ADDRESS



Title: PG04: I2C ADDR		
Size: Custom	Document Number: SCH-000012-00	Rev: 04.01
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P3V3_SYS @10A

Power GND. Connect SGND and DGND using short wide PCB traces"

P3V3_SYS
P12V_SW
P3V3_SYS_FETPWRIN
FB1
48
28F0121-0SR-10
0.75mOhm
10A
C221 2.2uF 25V
C222 22uF 25V
C223 22uF 25V
GREEN TLMG1100-GS08
D38
R849 261

Must place on the bottom side **********

R11 2.0K P3V3_SYS_INSNS 13 INSNS
R348 10.0 P3V3_SYS_INPWR 22 PWR
C212 1uF 35V

P23 P3V3_SYS_ALRT_OD
P6,7,8,9,10,11,12,53 LS1021A_I2C1_SCL_3V3
P6,7,8,9,10,11,12,53 LS1021A_I2C1_SDA_3V3
R15 0 P3V3_SYS_SALRT 9 SALRT
R14 0 U3_SCL 10 SCL
R13 0 U3_SDA 11 SDA
P54 P3V3_SYS_PGOOD_OD 32 PG
P12V_SW R339 4.70K 3.29V P3V3_SYS_EN 12 EN
P3V3_SYS_SYNC 1 SYNC
R12 1.78K
R22 12.7K
AGND5

I2CADDR = 0x1B

P3V3_SYS_ADDR0 2 ADDR0
P3V3_SYS_ADDR1 4 ADDR1
P3V3_SYS_RSET 3 SET
Rset = 50.5k ~ 51.7k ==> 3.3V
P3V3_SYS_TEMPX 7 TEMPX
8 CIO
28 IC-28
29 IC-29
5 DGND
R21 68.1K
R19 140K
R20 51.1K
Q7 MMBT3904,215 SOT-23-3
C208 100pF 50V
AGND5
Collector
TOP VIEW
BASE Emitter

LAYOUT NOTES:
Place MMBT3904 on the backside of the board
directly under output inductor 744311100

U3
MAX15301AA02+CJK
TQFN32_5MMX5MM_0_75MM
2A/4A.
Vi:4.5V~14V,Vo:0.5V~5.25V.

3P3-24 24
3P3-25 25
1P8 6
C211 4.7uF 6.3V
C209 10uF 6.3V
AGND5

LBO 23 P3V3_SYS_LBO L2 10uH 74479887310A
LBI 21 P3V3_SYS_LBI

OUTP 27
OUTN 26
C4 1000PF 25V
C210 0.01uF 50V
AGND5

DCRN 31
DCRP 30
C5 0.15uF 16V
R18 8.87K
P3V3_SYS_DCR_N
P3V3_SYS_DCR_P

DH 15 R10 10.0 P3V3_SYS_DH
BST 17 C3 0.22uF 16V
LX 16
LXSNS 14 R9 2.0K
DL 19 P3V3_SYS_DL
GDRV 18 P3V3_SYS_GDRV
PGND 20
EP-SGND 33
C2 2.2uF 25V
AGND5

Q1
HSG VP8
GND5 VP9
GND6 SW2
GND10 SW3
LSG SW4
FDPC8011S
POWERCLIP33_3_3MMX3_3MM_0_65MM
P3V3_SYS_FETPWRIN
C10 22uF 25V
C9 22uF 25V
P3V3_SYS_FETSW
R349 2.0
C213 2.2nF 50V

R340 0
R341 0
R342 0
R352 0
2
1uH
744311100
L1
P3V3_SYS_OUTCAP
R8 0.005 1W
10A
P3V3_SYS
R351 1.0K
C214 100UF 6.3V
C215 100UF 6.3V
R350 0
AGND5

LAYOUT NOTES:
Min Load requirement: 1K Ohm.
Must place before Sense Resistor.

GND **GND_POWER**

LAYOUT NOTE:
Differential Pair

LAYOUT NOTE:
Differential Pair

LAYOUT NOTE:
Remote Sense Connections:
At DUT Pads.

P3V3_SYS_SNS_P R574 0
P3V3_SYS_SNS_N R573 0
P3V3_SYS

SYSMON_P3V3_SYS_SNS_P P15
SYSMON_P3V3_SYS_SNS_N P15

LAYOUT NOTES:
Connect AGND1 TO GND
at the output capacitors

Replace the 0 Ohm resistor.
Connect AGNDX TO GND
via a short wide pcb trace.

P3V3_SYS
U4
SN74LVC1T45YZPR
A1 VCCA 1 6 VCCB A2
C1 A 3 4 B C2
B2 DIR 5 2 GND B1
1:A->B
DSBGA6_1_39MMX0_9MM_0_5MM
P1V8_FPGA

P1V8_FPGA
NC7SZ125L6X
U5
OE VCC NC
A Y
GND
MPAK-6_1MMX1_45MM_0_5MM
PWREN_1V8 P9

DESIGN NOTES (NC7SZ125L6X)
Voh = 1.70V (min)
Vol = 0.10V (max)
for Vin = Vil, Iol = 100uA.

P12V_SW
P3V3_SYS
R356 3.32K
R26 10K
C220 0.01uF 50V
R357 1.5K
R358 10K

DESIGN NOTES (MAX16052)
Vol = 0.4V (max) Isink = 1mA
Voh = Open Drain

U6
MAX16052AUT+T
IN 0.5Vthreshold
EN Vil_max=0.5V Vih_min=1.4V
2.5V~28V VCC
Opendrain OUT
30us/14us CDLY
GND
SOT-23-6
23uA
2.25V ~ 28V
P12V_SW
P3V3_SYS
R27 40.2K
MAX16052_OUT
C219 DNI <VOLTAGE>

P3V3_SYS
U7
VCC GND
SN74LVC1G126DCKR
SC-70-5

DESIGN NOTES (SN74LVC1G126)
Vol: 3V
Iol = 16mA ==> 0.40V (max)
Iol = 24mA ==> 0.55V (max)

PWREN_3V3
PWREN_3V3 P6,11,13

Title	PG05: P3V3_SYS@10A	
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0.95V
P1V0_FPGA @40A

P12V_SW
FB12
48
28F0121-0SR-10
0.75mOhm
10A
P12V_P1V0_FETPWRIN
C538 2.2uF 25V
C531 22uF 25V
C539 22uF 25V

U35

R181 2.0K P1V0_FPGA_INSNS → INSNS
R560 10.0 P1V0_FPGA_INPWR → PWR
C521 1uF 35V

DESIGN NOTE (ALERT)
SALRT: Interrupt to the SMBus master. Active low, Open-drain

I2C: Vih(min) = 2.0V

P23 P1V0_FPGA_ALRT_OD — R185 0 P1V0_FPGA_SALRT → SALRT
P5,7,8,9,10,11,12,53 LS1021A_I2C1_SCL_3V3 — R184 0 U35_SCL → SCL
P5,7,8,9,10,11,12,53 LS1021A_I2C1_SDA_3V3 — R183 0 U35_SDA → SDA
P7,54 P1V0_FPGA_PGOOD_OD → PG
P5,11,13 PWREN_3V3 — R182 0 → EN
P1V0_FPGA_SYNC → SYNC
R214 2.21K
AGND1

I2CADDR = 0x0A
P1V0_FPGA_ADDR0 → ADDR0
P1V0_FPGA_ADDR1 → ADDR1
P1V0_FPGA_RSET → SET
Rset = 12.5k ~ 12.9k ==> 0.95V
R213 2.21K
R203 140K
R204 12.7K
P1V0_FPGA_TEMPX → TEMPX
CIO
IC-28
IC-29
DGND
Q11 MMBT3904,215 SOT-23-3
C519 100pF 50V
AGND1

Collector
TOP VIEW
BASE Emitter

LAYOUT NOTES:
Place MMBT3904 on the backside of the board directly under output inductor 744309025

DESIGN NOTES (External Temp Sensor)
Any PN junction can be used as a temperature sensor. The 2N3904, 2N2222 transistors and integrated thermal diodes found in microprocessors, FPGAs, and ASICs are commonly used temperature sensors. Connect a 100pF filter capacitor as shown in Figure 7 to ensure accurate temperature measurements.

3P3-24
3P3-25
1P8
C529 4.7uF 6.3V
C520 10uF 6.3V
AGND1

LBO — P1V0_FPGA_LBO — L11 10uH 74479887310A
LBI — P1V0_FPGA_LBI

OUTP — C123 1000PF 25V
OUTN
C528 0.01uF 50V
AGND1

DCRN — C124 0.15uF 16V — R212 8.87K — P1V0_FPGA_DCR_N
DCRP — P1V0_FPGA_DCR_P

DH — R180 0 — P1V0_FPGA_DH
BST — C97 0.22uF 16V
LX
LXSNS — R179 2.0K
DL — P1V0_FPGA_DL
GDRV — P1V0_FPGA_GDRV
PGND
EP-SGND
C108 2.2uF 25V
C522 2.2nF 50V
R561 2.0

P12V_P1V0_FETPWRIN
Q5 FDMS8018
Q4 FDMS8018
C530 22uF 25V
C532 22uF 25V
R228 0
R227 0
Q2 FDMS8558S
Q3 FDMS8558S
P1V0_FPGA_FETSW
L10 250nH 744309025
P1V0_FPGA_OUTCAP
R229 1.0K

MAX15301AA02+CJK
TQFN32_5MMX5MM_0_75MM
2A/4A.
Vi:4.5V~14V,Vo:0.5V~5.25V.

DESIGN NOTES (MAX15301):
Power Sequence:
TON_DELAY defaults to 1ms.
TON_RISE defaults to 5ms.

Start with PreBias
A prebias condition occurs when there is already a voltage at the output of the power supply before it has been enabled. This can be caused by precharged output capacitors, or a parasitic ESD diode in the load IC that pulls the output up to another system supply rail.

DESIGN NOTES (MAX15301):
Inductor Selection:
1. Value:
   - o Higher ==> better efficiency by reducing RMS current.
   - o Lower ==> lower size/cost, might also improve transient response.
2. Isat: Must exceed Ilim (current limit).
3. Rdcr: small ==> minimize losses in efficiency.
4. For the design of the power distribution system consult UG583.

DESIGN NOTES (FDMS8018):
Vdss (drain-source) = 30V
1.8 mOhm@30A,10V
Ciss (input capacitance) = 5235pF@15V
Power (max) = 2.5W

DESIGN NOTES (FDMS8558S):
Vdss (drain-source) = 25V
1.5 mOhm@33A,10V
Ciss (input capacitance) = 5118pF@13V
Power (max) = 2.5W

DESIGN NOTES (744309025):
L = 250nH (Shielded Wirewound)
Isat = 47.5A
DCR = 0.165mOhm
Freq(self resonant) = 300MHz
Material: Manganese Zinc Ferrite

LAYOUT NOTES:
Min Load requirement: 1K Ohm.
Must place before Sense Resistor.

DESIGN NOTE (PGOOD)
PG: Open-Drain Power-Good Indicator. During startup and during a fault condition, PG is held low. PG is asserted high after the output has ramped to a voltage above the POWER_GOOD_ON (5Eh) threshold and a successful InTune calibration has completed.

DESIGN NOTES:
BABY BUCK REGULATOR:
1. BUCK: Connector 10uH between LBO and LBI
2. LDO: 100k pull-up between LBI and VIN
3. If Gate Drive available: 2k pull-up between LBI and VIN and GDRV connect to external source.

LAYOUT NOTE:
Differential Pair

LAYOUT NOTE:
Remote Sense Connections:
At DUT Pads.

P1V0_FPGA_SNS_P — R709 0 — P1V0_FPGA
P1V0_FPGA_SNS_N — R710 0

LAYOUT NOTE:
Differential Pair

P1V0_FPGA_DCR_N
P1V0_FPGA_DCR_P

SYSMON_P1V0_FPGA_SNS_P P15
SYSMPN_P1V0_FPGA_SNS_N P15

R562 0
R563 0

P1V0_FPGA
S2 S1
R202 0.003 3W
D36 MMSZ4680T1G

P1V0_FPGA_OUTCAP
C533 100UF 4V
C524 100UF 4V
C523 100UF 4V
C535 100UF 4V
C525 100UF 4V
C534 100UF 4V
R559 0
AGND1

LAYOUT NOTES:
Connect AGNDx TO GND at the output capacitors

Title	PG06: P0V95_FPGA@40A	
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P1V8_FPGA @10A

BRING-UP NOTES:
The value of IOUT_CAL_GAIN is initially set by the ADDR1 resistance according to Table 4b and should be set as close as possible to the inductor DCR.

The C141 *R256 must equal L12/DCR for correct current sense which is:
0.15uF * R256 = 1uH / 4.6m Ohm (refer to page 25 of IC data sheet)
R256=1.45k 1%
V[DCRP] - V[DCRN] = DCR x Iout_max
R[L] * C[L] = L / DCR
C141 * R256 = L12/DCR
0.15uF * R256 = 1uH / 4.6m Ohm
==> R256=1.45k 1%

DESIGN NOTES:
IOUT_CAL_GAIN = DCR x Iout_max / 25A
Optionally, for best precision, set IOUT_CAL_GAIN to match the actual inductor DCR and adjust the overcurrent fault threshold IOUT_OC_FAULT_LIMIT directly using PMBus commands.

P12V_SW
FB14
48
28F0121-0SR-10
0.75mOhm
10A
P12V_P1V8_FETPWRIN
C148 2.2uF 25V
C569 22uF 25V
C570 22uF 25V

U46
MAX15301AA02+CJK
TQFN32_5MMX5MM_0_75MM
2A/4A.
Vi:4.5V~14V,Vo:0.5V~5.25V.

R248 2.0K P1V8_FPGA_INSNS → INSNS
R598 10.0 P1V8_FPGA_INPWR → PWR
C567 1uF 35V

P23 P1V8_FPGA_ALRT_OD → R252 0 P1V8_FPGA_SALRT → SALRT
P5,6,8,9,10,11,12,53 LS1021A_I2C1_SCL_3V3 → R251 0 U46_SCL → SCL
P5,6,8,9,10,11,12,53 LS1021A_I2C1_SDA_3V3 → R250 0 U46_SDA → SDA
P8,54 P1V8_FPGA_PGOOD_OD → PG
P6,54 P1V0_FPGA_PGOOD_OD → R249 0 → EN
P1V8_FPGA_SYNC → SYNC
R260 2.21K AGND2

I2CADDR = 0x12
P1V8_FPGA_ADDR0 → ADDR0
P1V8_FPGA_ADDR1 → ADDR1
P1V8_FPGA_RSET → SET
R259 14.7K
R257 140K
R258 38.3K
Rset = 37.9k ~ 38.7k ==> 1.8V
P1V8_FPGA_TEMPX → TEMPX
Q12 MMBT3904,215 SOT-23-3
C563 100pF 50V
CIO, IC-28, IC-29, DGND
AGND2

Collector / TOP VIEW (3, 1, 2) / BASE / Emitter

LAYOUT NOTES:
Place MMBT3904 on the backside of the board directly under output inductor 744311100

3P3-24, 3P3-25, 1P8
C566 4.7uF 6.3V
C564 10uF 6.3V
AGND2

LBO, LBI
P1V8_FPGA_LBO L13 10uH 74479887310A
P1V8_FPGA_LBI

OUTP, OUTN
C565 1000PF 25V
C140 0.01uF 50V AGND2

LAYOUT NOTE:
Differential Pair

DCRN, DCRP
C141 0.15uF 16V
R256 1.43K
P1V8_FPGA_DCR_N
P1V8_FPGA_DCR_P

LAYOUT NOTE:
Differential Pair

P1V8_FPGA_SNS_P R707 0 P1V8_FPGA
P1V8_FPGA_SNS_N R708 0

LAYOUT NOTE:
Remote Sense Connections:
At DUT Pads.

SYSMON_P1V8_FPGA_SNS_P P15
SYSMON_P1V8_FPGA_SNS_N P15

P12V_P1V8_FETPWRIN

FDPC8011S
Q6
DH, BST, LX, LXSNS, DL, GDRV, PGND, EP-SGND
R247 10.0 P1V8_FPGA_DH
HSG, GND5, GND6, GND10, LSG, VP8, VP9, SW2, SW3, SW4
FDPC8011S
POWERCLIP33_3_3MMX3_3MM_0_65MM
C139 22uF 25V
C138 22uF 25V
C137 0.22uF 16V
R246 2.0K
R599 2.0
C568 2.2nF 50V
C136 2.2uF 25V
P1V8_FPGA_FETSW
P1V8_FPGA_DL
P1V8_FPGA_GDRV

R581 0
R582 0
R243 0
R244 0
L12 2 1uH 744311100
P1V8_FPGA_OUTCAP
R245 0.005 1W
10A
P1V8_FPGA
D12 MMSZ4686T1G 3.9V/500mW
R593 1.0K
C547 100UF 6.3V
C548 100UF 6.3V
1210
R592 0 AGND2

DESIGN NOTES (FDPC8011S):
Vdss (drain-source) = 25V
Id = 13A,27A.
Rds On (max) = 6 mOhm@13A,10V
Ciss (input capacitance) = 1240pF@13V
Power: 800mW,900mW

DESIGN NOTES (744311100):
L = 1uH (Shielded Wirewound)
Isat = 15A
DCR = 4.6 mOhm
Freq(self resonant) = 85MHz
Wirewound

DESIGN NOTES (C3225X6S0J107M250AC):
C = 100uF
V = 6.3V

LAYOUT NOTES:
Min Load requirement: 1K Ohm.
Must place before Sense Resistor.

LAYOUT NOTES:
Connect AGNDx TO GND at the output capacitors

Title	PG07: P1V8_FPGA@10A	
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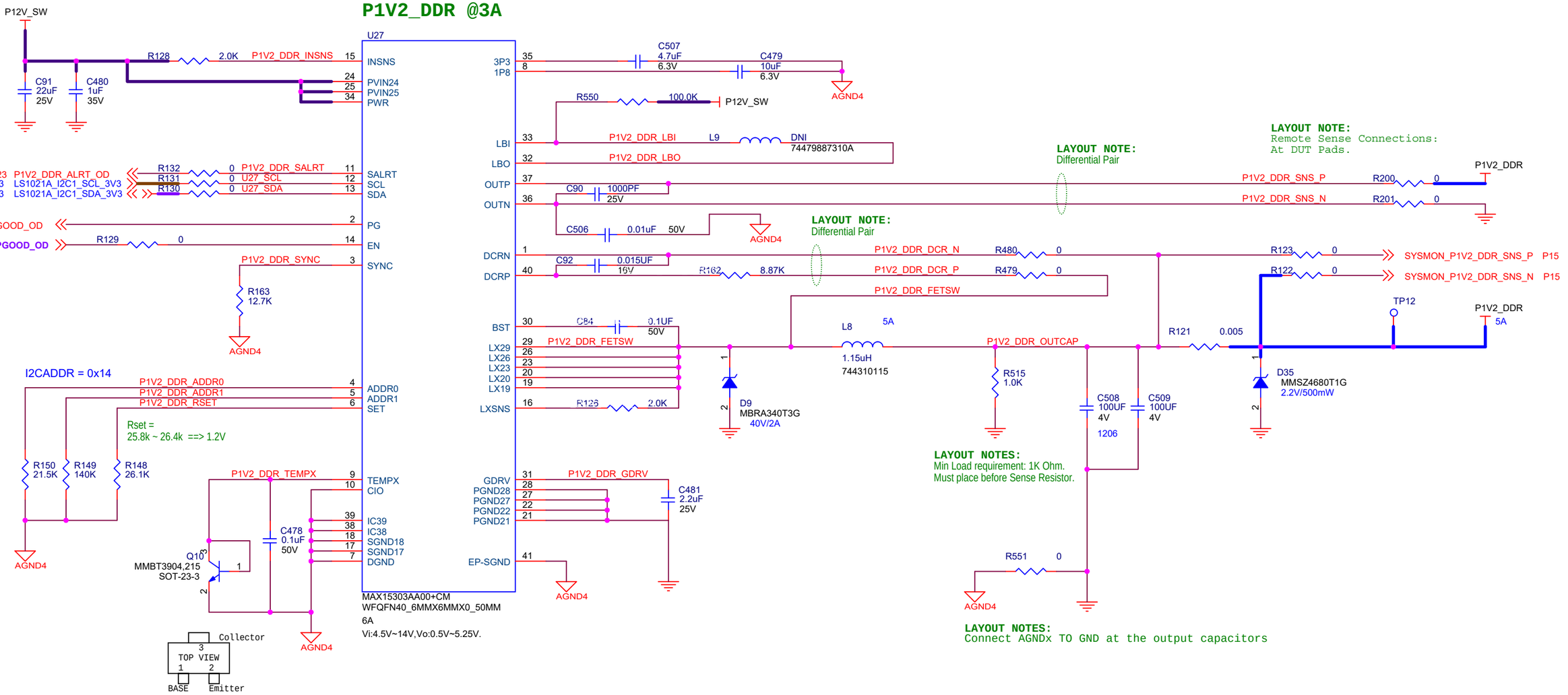
P1V2_DDR @3A



Title	PG08: M15303 P1V2_DDR@2A	
Size: Custom	Document Number: SCH-000012-00	Rev: 04.01
Date: Tuesday, June 19, 2018	Sheet 8 of 55	

P1V0_MGTAVCC @5A

P12V_SW
FB15
48
28F0121-0SR-10
0.75m0hm
10A
C593
2.2uF
25V

P12V_P1V0_MGT
measured 12.0V

U50
VDDH
VCC
VDD
AGND14
BST
PWM
ISENSE
TS_FAULT_B
VX6
VX7
VX8
VX9
VSS2
VSS3
VSS4
VSS5
Vin: 8.5V ~ 14V
55A
VT1697SBFQ
VFQFN16_6MM_3_75MM

R267
10.0
C623
1UF
25V
C661
0.1UF
16V
R268
DNI
C662
0.22uF
16V
P1V0_MGT_VX
L14
210nH
FP1208R1-R21-R
P1V0_MGT_VX_IND
C663
DNI
<VOLTAGE>
R280
0.001

R279
1.0K
R278
1.0K
C158
2.2uF
10V
C160
0.022uF
10V
C159
0.022uF
10V
SYSMON_P1V0_MGT_SNS_P P15
SYSMON_P1V0_MGT_SNS_N P15

P1V0_MGTAVCC
D13
MMSZ4680T1G

INPUT CAPS FOR P1V0_MGTAVCC
C624
47uF
25V
C147
47uF
25V
C594
22uF
25V
C152
22uF
25V
C627
0.1uF
50V
C626
0.1uF
50V
C625
1UF
25V
C666
22uF
10V
C665
22uF
10V
C664
22uF
10V
C151
100UF
4V
C149
100UF
4V
C667
100UF
4V

P1V0_MGT_PWM2
P1V0_MGT_ISENSE2
R281
4.7
C162
100pF
50V
C161
1000PF
25V

LAYOUT NOTE:
Provide AGND shielded to these noise sensative signals.

P1V0_MGT_TS_FAULT_B

P1V8_MGT_SLAVE
C154
1UF
25V
measured 1.8V
R270
4.99
C153
22uF
25V
C622
1UF
25V
R271
174
C156
1UF
25V
C155
0.1UF
16V

U53
VDD
PVX
P1V0_MGT_VIN_UV
VIN_UV
Scaled Version of Slave VDDH Voltage.
P3V3_SYS
VDD33_IN
C685
0.1uF
50V
C684
1UF
25V
C170
10uF
6.3V
Open-Drain,
Active-Low
PMBus Alert
Output
PMALERT_B
PMCLOCK
PMDATA
PWRGD
VR_ON
TS_FAULT_B
Vin:1.71V ~ 3.63V
55A (VT1697)
R_REF
MRAMP
R_SEL0
R_SEL1
R_SEL2
R_SEL3
N.C.
GND
SENSE+/-
A1_OUT
A2_IN
A2_OUT
A2B_OUT
A3_IN
A3_OUT_PS
A3_OUT_NORM
PWM1
PWM2
PWM3
PWM4
ISENSE1
ISENSE2
ISENSE3
ISENSE4
SENSE_P
SENSE_N
PGND
EPAD
MAX20751EKX+
VFQFN36-EP_6MM_6MM

waveform
L15
3.3uH
VLS252012ET-3R3M

P12V_SW
R285
29.4K
R687
2.15K
C660
100pF
50V
AGND6

P23 P1V0_MGT_ALRT_OD
P5,6,7,8,10,11,12,53 LS1021A_I2C1_SCL_3V3
P5,6,7,8,10,11,12,53 LS1021A_I2C1_SDA_3V3
R284 0 P1V0_MGT_PMALERT_B
R283 0 U53_SCL
R282 0 U53_SDA
P54 P1V0_MGT_PGOOD_OD
P5 PWREN_1V8
R269 0 measured 1.8V

VR_ON: Vih = 0.9V(min)
VR_ON: Vil = 0.2V(max)

I2CADDR = 0x72
P1V0_MGT_R_REF
P1V0_MGT_MRAMP
P1V0_MGT_R_SEL0
P1V0_MGT_R_SEL1
P1V0_MGT_R_SEL2
P1V0_MGT_R_SEL3
R277
20.0K
R276
22.1K
R275
0
R274
576
R273
402
R272
80.6
Vout = 1.0V
R_SEL2 = R273 = 402 ==> 0.970V
R_SEL1 = R274 = 576 ==> 0.030V

R288
220
C165
220pF
50V
R289
DNI
C163
DNI
R286
332
R290
680
C164
0.022uF
10V
R287
604
P1V0_MGT_A3_IN
R295
0
C166
DNI
C167
8200pF
50V
R291
499
R296
2.49k

This pin goes 400mV and stays at that level when power applied
P1V0_MGT_PWM2
P1V0_MGT_ISENSE2_PIN
R294
3.01K
P1V0_MGT_ISENSE2
C169
22PF
50V
P1V0_MGT_TS_FAULT_B
P1V0_MGTAVCC
P1V0_MGT_SENSE_P
R809
0
P1V0_MGTAVCC_SPLIT_RES
P1V0_MGT_SENSE_N
R808
0
R688
0

AGND6

Title: PG09: P1V0_MGTAVCC
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P12V_SW
FB16
48
28F0121-0SR-10
0.75mOhm
10A
C736
2.2uF
25V
P12V_P1V2_MGT
U58
VDDH
VCC
VDD
AGND14
PWM
ISENSE
TS_FAULT_B
BST
VX6
VX7
VX8
VX9
VSS2
VSS3
VSS4
VSS5
Vin: 8.5V ~ 14V
55A
VT1697SBFQ
VFQFN16_6MM_3_75MM
R730
10.0
C174
1UF
25V
C771
0.1UF
16V
R308
DNI
R309
4.7
C184
100pF
50V
C183
1000PF
25V
C775
0.22uF
16V
P1V2_MGT_VX
L16
210nH
FP1208R1-R21-R
P1V2_MGT_VX_IND
C776
DNI
<VOLTAGE>
R320
0.001
R319
1.0K
R307
1.0K
C188
2.2uF
10V
C189
0.022uF
10V
C179
0.022uF
10V
SYSMON_P1V2_MGT_SNS_P P15
SYSMON_P1V2_MGT_SNS_N P15
D37
MMSZ4680T1G
P1V2_MGTAVTT
C779
22uF
10V
C180
22uF
10V
C777
22uF
10V
C182
100UF
4V
C181
100UF
4V
C778
100UF
4V

INPUT CAPS FOR P1V2_MGTAVTT

C172
47uF
25V
C173
47uF
25V
C738
22uF
25V
C739
22uF
25V
C774
0.1uF
50V
C773
0.1uF
50V
C772
1UF
25V

P1V2_MGT_SLAVE

C176
1UF
25V
R299
4.99
C175
22uF
25V
C737
1UF
25V
R300
174
C177
1UF
25V
C178
0.1UF
16V

P1V2_MGTAVTT @5A

U59
VDD
PVX
VIN_UV
VDD33_IN
PMALERT_B
PMCLOCK
PMDATA
PWRGD
VR_ON
R_REF
MRAMP
R_SEL0
R_SEL1
R_SEL2
R_SEL3
N.C.
GND
SENSE+/-
A1_OUT
A2_IN
A2_OUT
A2B_OUT
A3_IN
A3_OUT_PS
A3_OUT_NORM
PWM1
PWM2
PWM3
PWM4
ISENSE1
ISENSE2
ISENSE3
ISENSE4
TS_FAULT_B
SENSE_P
SENSE_N
PGND
EPAD
Vin:1.71V ~ 3.63V
55A (VT1697)
MAX20751EKX+
VFQFN36-EP_6MM_6MM

L17
3.3uH
VLS252012ET-3R3M

P12V_SW
R314
29.4K
R729
2.15K
C770
100pF
50V
AGND7

P3V3_SYS
C839
0.1uF
50V
C838
1UF
25V
C191
10uF
6.3V

Open-Drain,
Active-Low
PMBus Alert
Output

P23 P1V2_MGT_ALRT_OD
P5,6,7,8,9,11,12,53 LS1021A_I2C1_SCL_3V3
P5,6,7,8,9,11,12,53 LS1021A_I2C1_SDA_3V3
R313 0 P1V2_MGT_PMALERT_B
R312 0 U59_SCL
R311 0 U59_SDA

P54 P1V2_MGT_PGOOD_OD
P13,54 P1V0_MGT_PGOOD_1V8
R310 0

VR_ON: Vih = 0.9V(min)
VR_ON: Vil = 0.2V(max)

I2CADDR = 0x73

R306
20.0K
R305
24.9K
R304
0
R303
1.02K
R302
576
R301
1.02K

R316
220
C187
220pF
50V
R318
DNI
C186
DNI
R315
332
R317
680
C185
0.022uF
10V
R323
604
P1V2_MGT_A3_IN
R322
0
C192
DNI
C193
8200pF
50V
R325
499
R324
2.49k

P1V2_MGT_PWM2
P1V2_MGT_ISENSE2
R321
3.01K
C190
22PF
50V
P1V2_MGT_TS_FAULT_B
P1V2_MGTAVTT
P1V2_MGT_SENSE_P
P1V2_MGT_SENSE_N
R749
0
R748
0
R747
0

Title: PG10: P1V2_MGTAVTT
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P1V8_ARM @5A

P12V_SW

C69 22uF 25V
C259 1uF 35V
R83 2.0K P1V8_ARM_INSNS

U13

INSNS 15
PVIN24 24
PVIN25 25
PWR 34

P23 P1V8_ARM_ALRT_OD
P5,6,7,8,9,10,12,53 LS1021A_I2C1_SCL_3V3
P5,6,7,8,9,10,12,53 LS1021A_I2C1_SDA_3V3

R87 0 U13_SALRT → SALRT 11
R86 0 U13_SCL → SCL 12
R85 0 U13_SDA → SDA 13

P12,54 P1V8_ARM_PGOOD_OD → PG 2

P5,6,13 PWREN_3V3
R84 0 U13_EN → EN 14

SYNC 3

R97 12.7K
AGND8

I2CADDR = 0x0F

P1V8_ARM_ADDR0 → ADDR0 4
P1V8_ARM_ADDR1 → ADDR1 5
P1V8_ARM_RSET → SET 6

Rset =
37.9k ~ 38.7k ==> 1.8V

R96 9.53K
R95 140K
R88 38.3K
AGND8

P1V8_ARM_TEMPX → TEMPX 9
CIO 10

C257 0.1uF 50V

IC39 39
IC38 38
SGND18 18
SGND17 17
DGND 7

Q9
MMBT3904,215
SOT-23-3

Collector
TOP VIEW
BASE Emitter

AGND8

P12V_SW

3P3 35
1P8 8

C266 4.7uF 6.3V
C258 10uF 6.3V
AGND8

R408 100.0K

LBI 33
P1V8_ARM_LBI L6 DNI 74479887310A

LBO 32
P1V8_ARM_LBO

OUTP 37
P1V8_ARM_SNS_P

C264 1000PF 25V

OUTN 36
P1V8_ARM_SNS_N

C265 0.01uF 50V
AGND8

LAYOUT NOTE:
Differential Pair

R423 0
R422 0
P1V8_ARM

DCRN 1
C68 0.015UF 16V
DCRP 40
R94 8.87K

P1V8_ARM_DCR_N R92 0
P1V8_ARM_DCR_P R93 0
P1V8_ARM_FETSW

R391 0 SYSMON_P1V8_ARM_SNS_P P15
R390 0 SYSMON_P1V8_ARM_SNS_N P15

BST 30
C67 0.1UF 50V

LX29 29
LX26 26
LX23 23
LX20 20
LX19 19

LXSNS 16
R82 2.0K

D8
MBRA340T3G
40V/2A

L5
1.15uH
744310115

R389 1.0K

P1V8_ARM_OUTCAP

C268 100UF 6.3V X6S
C269 100UF 6.3V

R81 0.005

TP6
5A
P1V8_ARM

D34
MMSZ4686T1G
3.9V/500mW

R409 0
AGND8

GDRV 31
P1V8_ARM_GDRV
PGND28 28
PGND27 27
PGND22 22
PGND21 21

C267 2.2uF 25V

EP-SGND 41
AGND8

MAX15303AA00+CM
WFQFN40_6MMX6MMX0_50MM
6A
Vi:4.5V~14V,Vo:0.5V~5.25V.

LAYOUT NOTES:
Connect AGNDx TO GND at the output capacitors

P1V8_FPGA @10A

P1V8_FPGA
FB8
DNI
28F0121-0SR-10
P1V8_ARM

C270 2.2uF 25V
C260 22uF 25V
C48 22uF 25V

Title: PG11: P1V8_ARM@5A
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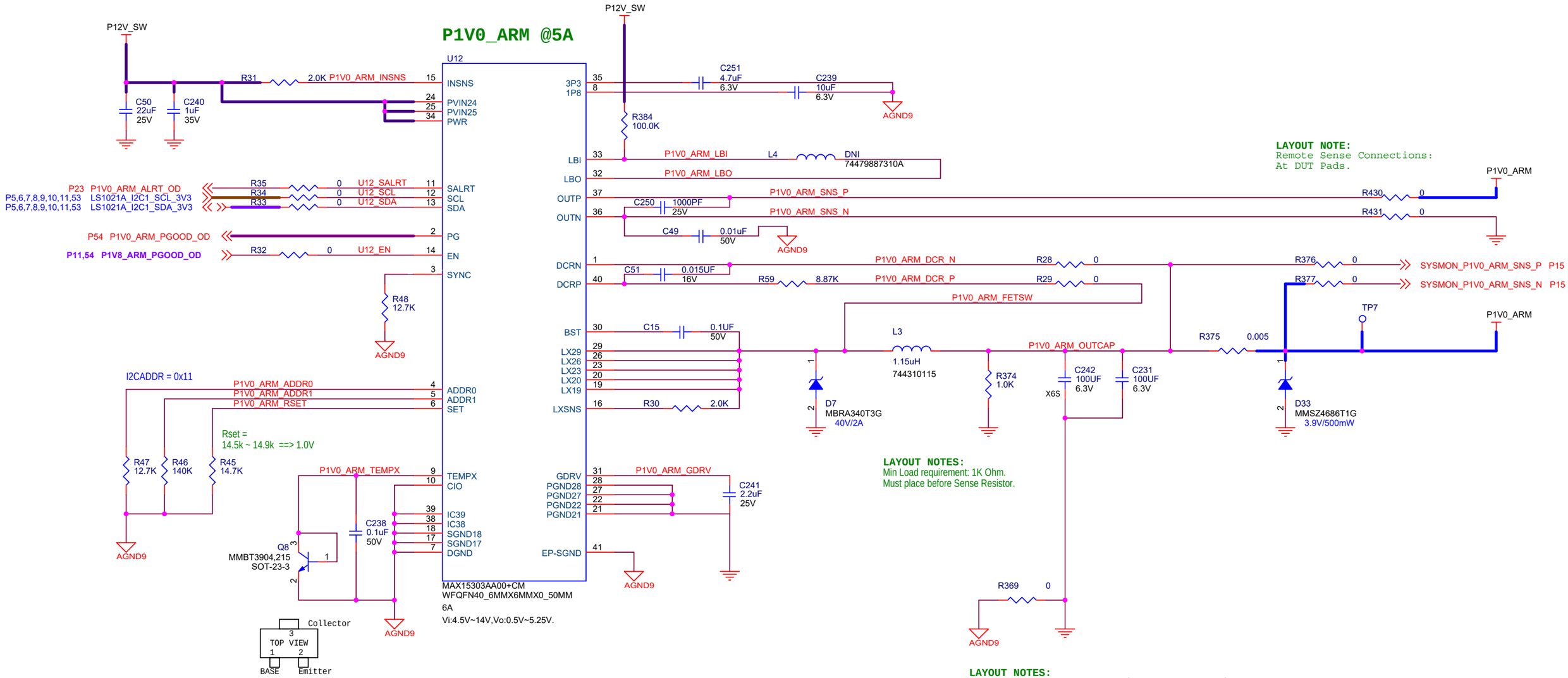
P1V0_ARM @5A



LAYOUT NOTE:
Remote Sense Connections:
At DUT Pads.

LAYOUT NOTES:
Min Load requirement: 1K Ohm.
Must place before Sense Resistor.

LAYOUT NOTES:
Connect AGNDx TO GND at the output capacitors

LAYOUT NOTES:
Place MMBT3904 on the backside of the board
directly under output inductor 744310115.

Title	PG12: P1V0_ARM@5A	
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DESIGN NOTES: (Reset Output)
Open-drain output is low when VOUT is 8% below its nominal value.
RST remains low while the output voltage (VOUT) is below the reset threshold and for at least 3ms after VOUT rises to within regulation.
Connect a 100k pull-up resistor to OUT to obtain an output voltage.

VOUT = VSET * (1 + R1/R2)

P3V3_SYS

C555
1UF
25V

U42
MAX8869EUE18+

IN02 IN03 IN04 IN05 (2 3 4 5)
OUT15 OUT14 OUT13 OUT12 (15 14 13 12)

P1V8_MGTVCCAUX

C556
10uF
6.3V

TP23 **PLACE TP CLOSE TO U42**

R236
10.2K

R216
8.06K

P54 P1V8_MGTVCCAUX_PGOOD_OD — 6 RST_B PGOOD

P10,54 P1V0_MGT_PGOOD_1V8 — R217 0 — U42_SHDN_B — 7 SHDN_B Vih=1.6V

11 U14_SET — SET 0.8V

8 SOFTSTART

C542
DNI

17 EP17
10 GND

NC01 (1) NC09 (9) NC16 (16)

TSSOP-16EP
1.0A
1.8V

LDO
200mV dropout
1A

DESIGN NOTES (SCALE DOWN)

Scale 3.3V to 3.3V / 4 = 0.825V
==> 3R2 = R1

R1 R620 3.0K
R622 100 — SYSMON_AD07_P P26
R2 R621 1.0K
C581 820pF 50V
P3V3_SYS / 4
R619 100 — SYSMON_AD07_N P26

LAYOUT NOTES:
1. Pin 1 of 10.2K resistor must be routed as a sense line directly to a MAX8869's power pin.
2. Place MAX8869 near FPGA.

DESIGN NOTES: (LMZ20502 VOUT)
VOUT = 0.6 * Rfbt/Rfbb + 0.6
VOUT = 1.3478V for Rfbt = 69.8K and Rfbb = 56K

DESIGN NOTES: (LMZ20502 PGOOD)
PGOOD
Open drain.
High = power good;
Low = power bad.
If not used, leave unconnected.

DESIGN NOTES: (LMZ20502 EN)
Vih(min) = 1.4V (max = Vin+0.2)
Vil(max) = 0.4V
Active High
A valid input voltage, on pin 8, must be present before EN is asserted. Do not float.

P3V3_SYS

C85
47uF
10V
3.03 mOhm

U28
LMZ20502SILT

8 VIN — VOUT 5

P1V35_ARM
2A

04.19.2017 - Part replacement
R166
ERJ-PB3B6982V ==> 7-2176089-5

TP24 **PLACE TP CLOSE TO U28**

R164
DNI

P54 P1V0_ARM_PGOOD_1V8 — R165 0 — U28_EN — 2 EN

P54 PG_P1V35_DDR_OD — 1 PG

3 MODE
11 EP3
12 EP4

NC 7

C94
56pF
50V

R166
69.8K
Rfbt
0.1%

C86
22uF
10V
3.57 mOhm
CMP-000940-00
C3216JB1A226M160AC

FB 4 — U15_FB

R151
56.0K
Rfbb
0.1%

GND 6
EP2 10
EP1 9

SMD8_3_5MMX3_5MMX1_8MM
Vi:2.7V~5.5V/Vo:0.8V~3.6V
2A

R1 R616 1.0K
R615 100 — SYSMON_AD09_P P26
R2 R617 1.0K
C580 820pF 50V
P1V35_ARM / 2
R618 100 — SYSMON_AD09_N P26

The maximum value of total output capacitance should be limited to between 100 µF and 200 µF. Large values of output capacitance can prevent the regulator from starting-up correctly and adversely affect the loop stability. If values in the range given above, or larger, are to be used, then a careful study of start-up at full load and loop stability must be performed.

DESIGN NOTES (MAX15027ATB+T)

Vout = Vfb * (1+R1/R2)

Iout = 1A
Cin = 1.0µF ceramic (lower the source impedance)
Cout = 4.7µF ceramic (low ESR)

Cin lowers the source impedance of the input supply.
If input supply source impedance is high, place a larger input capacitor close to IN to prevent VIN sagging due to load transients.
Smaller Cout can be used for output currents less than 1A.

Cout = Iout(max) * (1uF/0.25A)

P3V3_SYS

C559
X6S
1uF
10V

U41
MAX15027ATB+T

1 IN1
2 IN2
3 IN3

OUT09 9
OUT10 10

P2V5_SYS
1A

TP25 **PLACE TP CLOSE TO U41**

R233
DNI

R234
40.2K

P5,6,11 PWREN_3V3 — R232 0 — 5 EN

FB 7 — U16_FB

C133
4.7UF
16V
X5R

C558
X7R
0.1UF
16V

6 SS

GND 8
IC_GND 4
EP_GND 11

R235
10K

TDFN10-EP_3MMX3MM
1.0A
0.5V~3.3V

LDO
225mV dropout
1A

R1 R596 3.0K
R594 100 — SYSMON_AD10_P P26
R2 R597 1.0K
C557 820pF 50V
P2V5_SYS / 4
R595 100 — SYSMON_AD10_N P26

Title: **PG13: P1V8_MGT / P1V35_ARM / P2V5**

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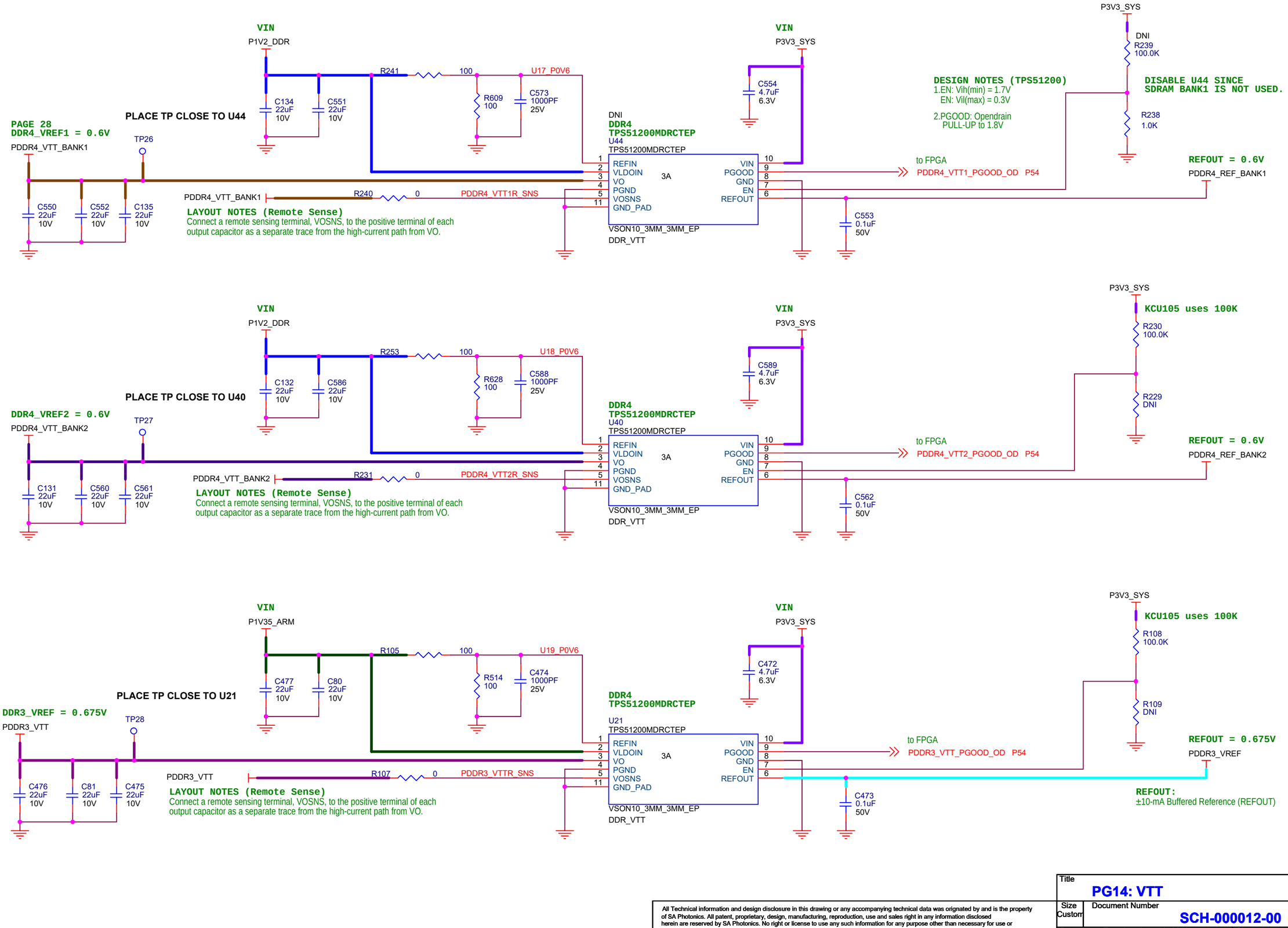

Title	PG14: VTT	
Size: Custom	Document Number: SCH-000012-00	Rev: 04.01
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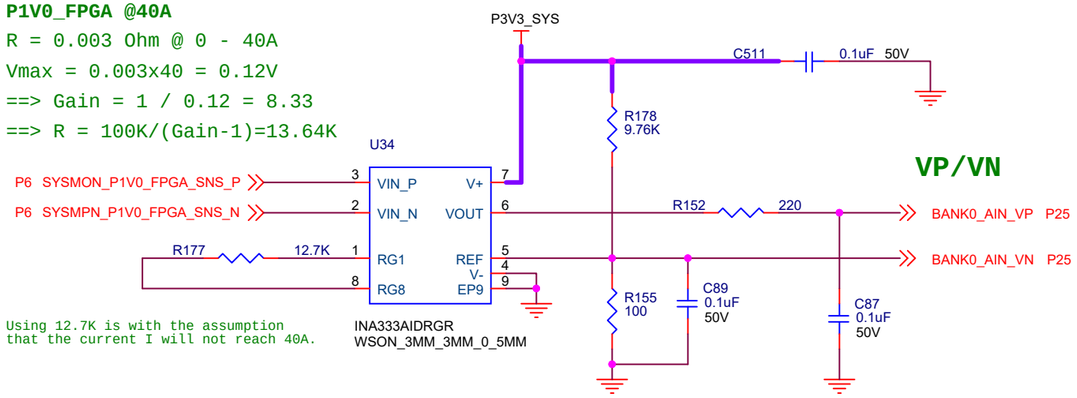
P1V0_FPGA @40A

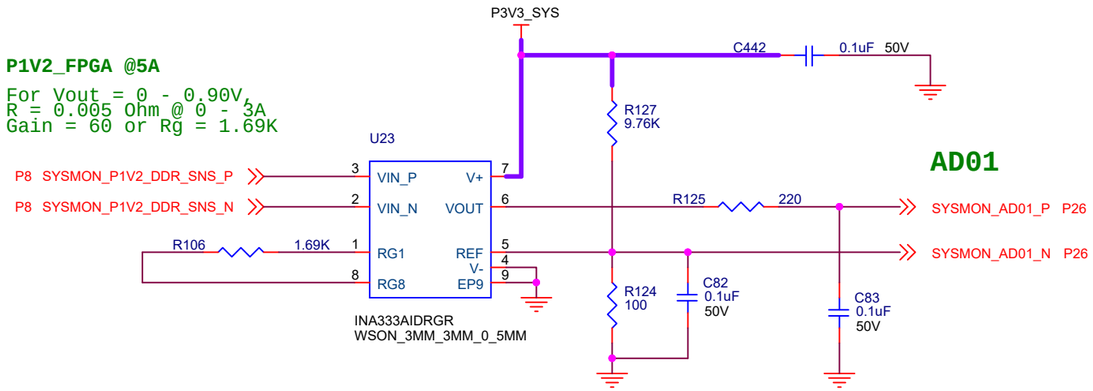
R = 0.003 Ohm @ 0 - 40A
Vmax = 0.003x40 = 0.12V
==> Gain = 1 / 0.12 = 8.33
==> R = 100K/(Gain-1)=13.64K



Using 12.7K is with the assumption that the current I will not reach 40A.

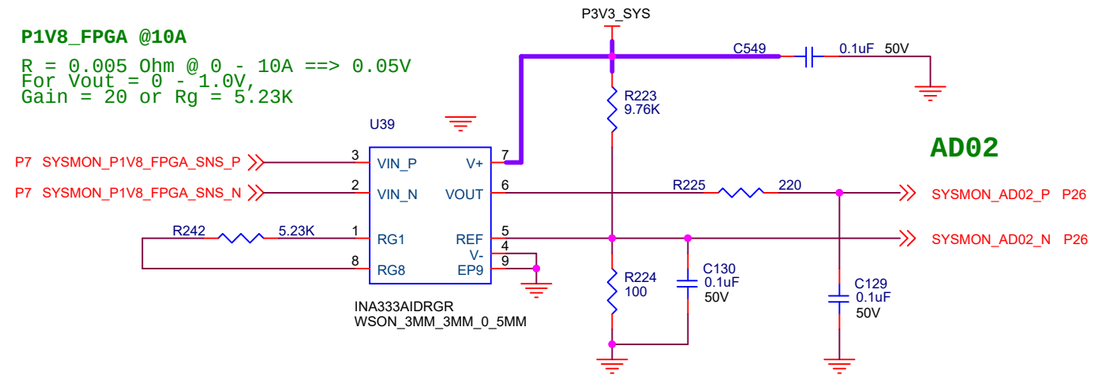
P1V2_FPGA @5A

For Vout = 0 - 0.90V,
R = 0.005 Ohm @ 0 - 3A
Gain = 60 or Rg = 1.69K



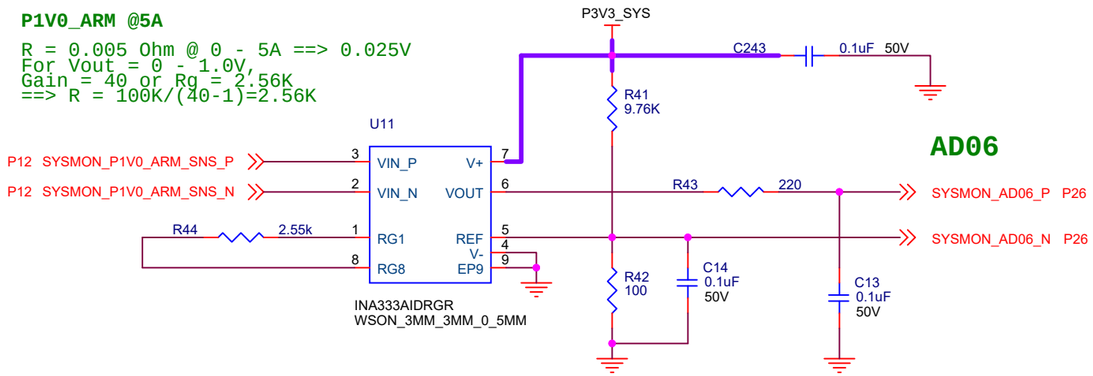
P1V8_FPGA @10A

R = 0.005 Ohm @ 0 - 10A ==> 0.05V
For Vout = 0 - 1.0V,
Gain = 20 or Rg = 5.23K



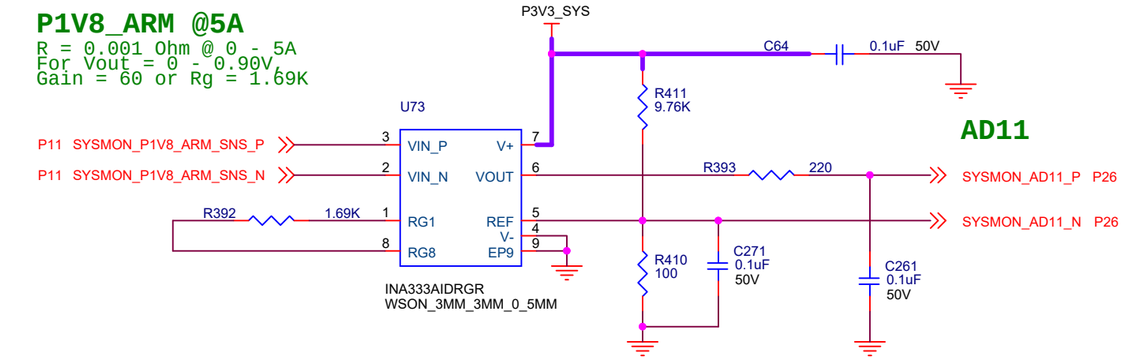
P1V0_ARM @5A

R = 0.005 Ohm @ 0 - 5A ==> 0.025V
For Vout = 0 - 1.0V,
Gain = 40 or Rg = 2.56K
==> R = 100K/(40-1)=2.56K



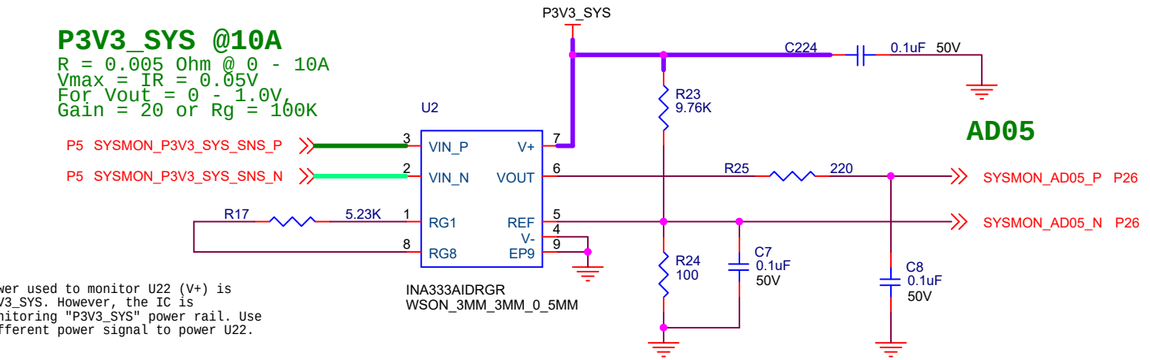
P1V8_ARM @5A

R = 0.001 Ohm @ 0 - 5A
For Vout = 0 - 0.90V,
Gain = 60 or Rg = 1.69K



P3V3_SYS @10A

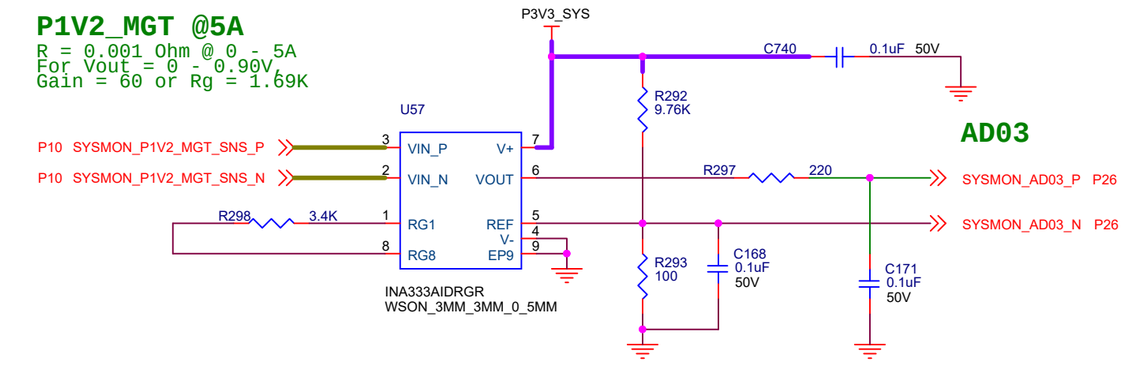
R = 0.005 Ohm @ 0 - 10A
Vmax = IR = 0.05V
For Vout = 0 - 1.0V,
Gain = 20 or Rg = 100K



Power used to monitor U22 (V+) is P3V3_SYS. However, the IC is monitoring "P3V3_SYS" power rail. Use different power signal to power U22.

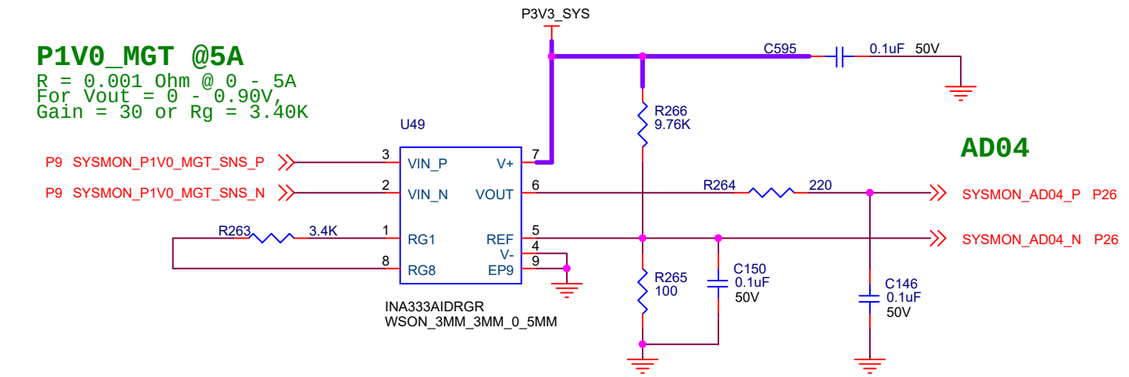
P1V2_MGT @5A

R = 0.001 Ohm @ 0 - 5A
For Vout = 0 - 0.90V,
Gain = 60 or Rg = 1.69K



P1V0_MGT @5A

R = 0.001 Ohm @ 0 - 5A
For Vout = 0 - 0.90V,
Gain = 30 or Rg = 3.40K



Title: PG15: SYSMON OPAMPS
Size: Custom
Document Number: SCH-000012-00
Rev: 04.01
Date: Tuesday, June 19, 2018
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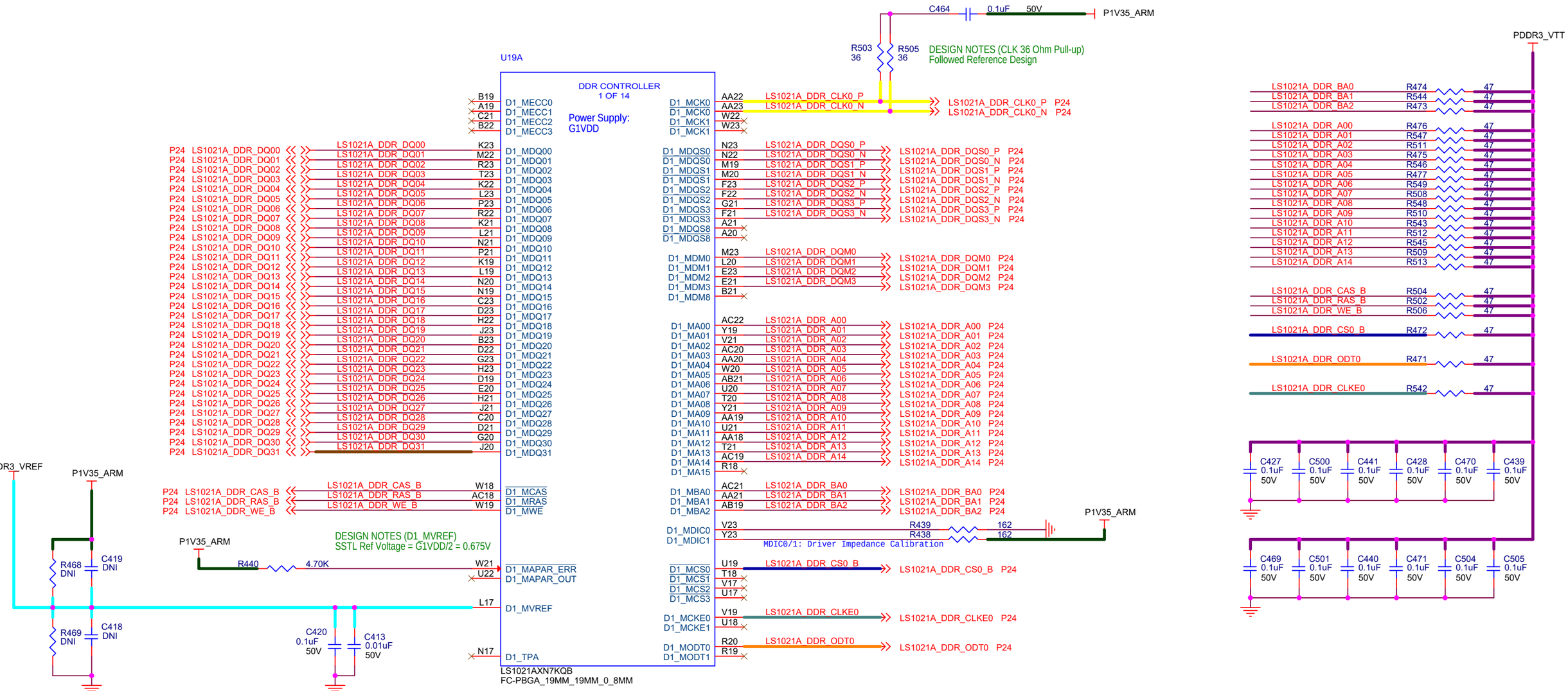
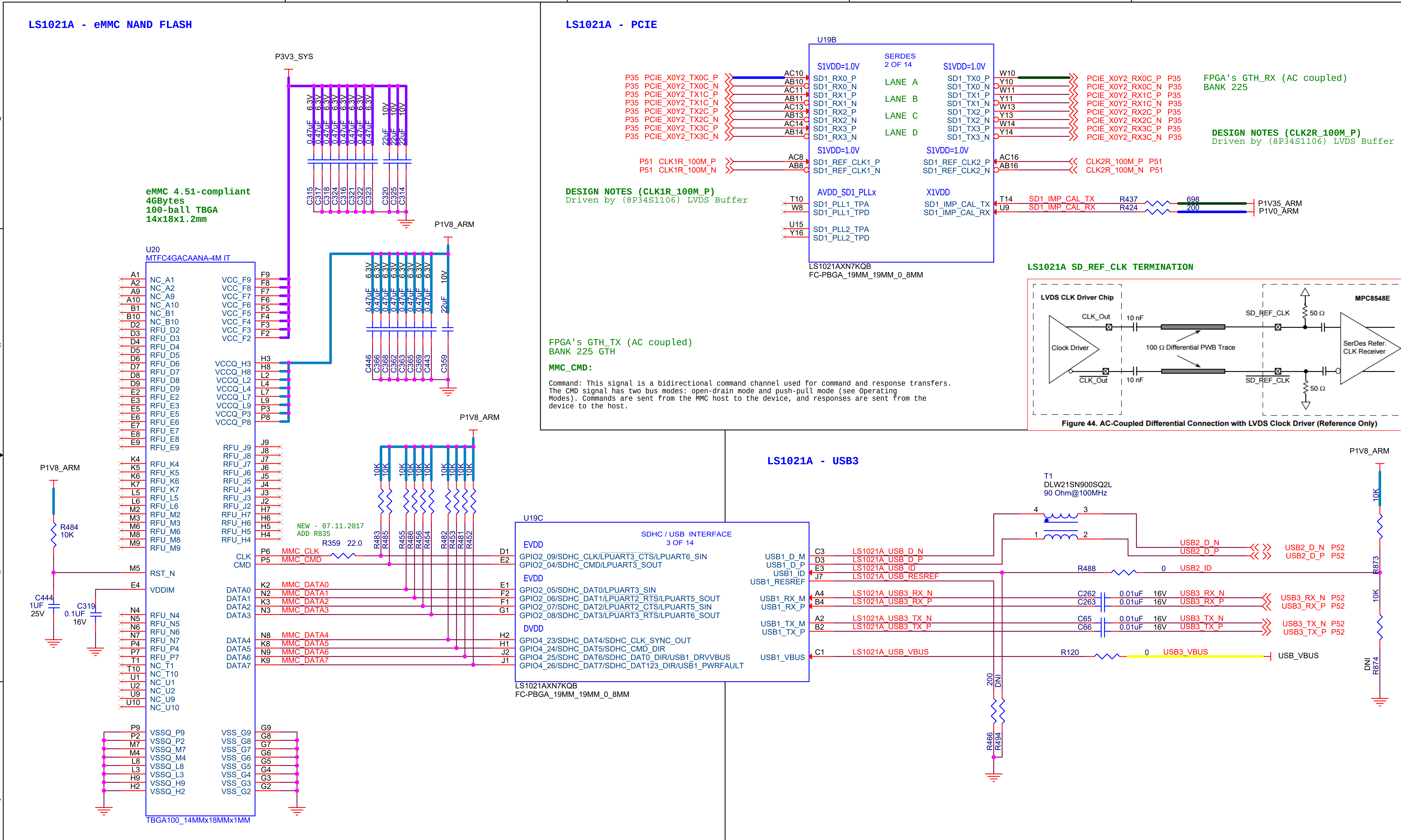
LS1021A - DDR3 INTERFACE



Title: **PG16: LS1021A DDR3 INTERFACE**

Size: Custom | Document Number: **SCH-000012-00** | Rev: 04.01

Date: Tuesday, June 19, 2018 | Sheet 16 of 55


LS1021A - eMMC NAND FLASH
P3V3_SYS
P1V8_ARM
eMMC 4.51-compliant
4GBytes
100-ball TBGA
14x18x1.2mm
U20
MTFC4GACAANA-4M IT
TBGA100_14MMx18MMx1MM
NEW - 07.11.2017
ADD R835
R359 22.0
MMC_CLK
MMC_CMD
MMC_DATA0
MMC_DATA1
MMC_DATA2
MMC_DATA3
MMC_DATA4
MMC_DATA5
MMC_DATA6
MMC_DATA7
R484
10K
C444
1UF
25V
C319
0.1UF
16V
LS1021A - PCIE
U19B
SERDES
2 OF 14
S1VDD=1.0V
LANE A
LANE B
LANE C
LANE D
P35 PCIE_X0Y2_TX0C_P
P35 PCIE_X0Y2_TX0C_N
P35 PCIE_X0Y2_TX1C_P
P35 PCIE_X0Y2_TX1C_N
P35 PCIE_X0Y2_TX2C_P
P35 PCIE_X0Y2_TX2C_N
P35 PCIE_X0Y2_TX3C_P
P35 PCIE_X0Y2_TX3C_N
PCIE_X0Y2_RX0C_P P35
PCIE_X0Y2_RX0C_N P35
PCIE_X0Y2_RX1C_P P35
PCIE_X0Y2_RX1C_N P35
PCIE_X0Y2_RX2C_P P35
PCIE_X0Y2_RX2C_N P35
PCIE_X0Y2_RX3C_P P35
PCIE_X0Y2_RX3C_N P35
FPGA's GTH_RX (AC coupled)
BANK 225
DESIGN NOTES (CLK2R_100M_P)
Driven by (8P34S1106) LVDS Buffer
P51 CLK1R_100M_P
P51 CLK1R_100M_N
CLK2R_100M_P P51
CLK2R_100M_N P51
DESIGN NOTES (CLK1R_100M_P)
Driven by (8P34S1106) LVDS Buffer
AVDD_SD1_PLLx
X1VDD
SD1_IMP_CAL_TX
SD1_IMP_CAL_RX
R437 698
R424 200
P1V35_ARM
P1V0_ARM
LS1021AXN7KQB
FC-PBGA_19MM_19MM_0_8MM
LS1021A SD_REF_CLK TERMINATION
LVDS CLK Driver Chip
Clock Driver
CLK_Out
10 nF
100 Ω Differential PWB Trace
SD_REF_CLK
50 Ω
MPC8548E
SerDes Refer. CLK Receiver
Figure 44. AC-Coupled Differential Connection with LVDS Clock Driver (Reference Only)
FPGA's GTH_TX (AC coupled)
BANK 225 GTH
MMC_CMD:
Command: This signal is a bidirectional command channel used for command and response transfers. The CMD signal has two bus modes: open-drain mode and push-pull mode (see Operating Modes). Commands are sent from the MMC host to the device, and responses are sent from the device to the host.
LS1021A - USB3
T1
DLW21SN900SQ2L
90 Ohm@100MHz
U19C
SDHC / USB INTERFACE
3 OF 14
EVDD
DVDD
GPIO2_09/SDHC_CLK/LPUART3_CTS/LPUART6_SIN
GPIO2_04/SDHC_CMD/LPUART3_SOUT
GPIO2_05/SDHC_DAT0/LPUART3_SIN
GPIO2_06/SDHC_DAT1/LPUART2_RTS/LPUART5_SOUT
GPIO2_07/SDHC_DAT2/LPUART2_CTS/LPUART5_SIN
GPIO2_08/SDHC_DAT3/LPUART3_RTS/LPUART6_SOUT
GPIO4_23/SDHC_DAT4/SDHC_CLK_SYNC_OUT
GPIO4_24/SDHC_DAT5/SDHC_CMD_DIR
GPIO4_25/SDHC_DAT6/SDHC_DAT0_DIR/USB1_DRVVBUS
GPIO4_26/SDHC_DAT7/SDHC_DAT123_DIR/USB1_PWRFAULT
LS1021A_USB_D_N
LS1021A_USB_D_P
LS1021A_USB_ID
LS1021A_USB_RESREF
LS1021A_USB3_RX_N
LS1021A_USB3_RX_P
LS1021A_USB3_TX_N
LS1021A_USB3_TX_P
LS1021A_USB_VBUS
USB2_D_N P52
USB2_D_P P52
R488 0 USB2_ID
USB3_RX_N P52
USB3_RX_P P52
USB3_TX_N P52
USB3_TX_P P52
R120 0 USB3_VBUS
USB_VBUS
R466 200
R494 DNI
R873 10K
R874 10K DNI

Title: PG17: USB3 AND eMMC NAND

Size	Document Number	Rev
Custom	SCH-000012-00	04.01

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LS1021A - NOR FLASH 1Gbits

LS1021A-QSPI to program the FPGA's configuration Flash.

U19D

BVDD = 1.8V
ALL = BVDD

IFC INTERFACE
4 OF 14

IFC_AD00/CFG_GPINPUT0		IFC_CS0	C17 LS1021A_IFC_CS0_B R540 10K → P1V8_ARM
IFC_AD01/CFG_GPINPUT1		GPIO2_10/IFC_CS1/SPI1_PCS0/FTM7_CH0	D17 LS1021A_GPIO2_10 R353 10K → P1V8_ARM
IFC_AD02/CFG_GPINPUT2		GPIO2_11/IFC_CS2/SPI1_SCK/FTM7_CH1/IIC3_SCL	C18 LS1021A_GPIO2_11 R354 10K → P1V8_ARM
IFC_AD03/CFG_GPINPUT3		GPIO2_12/IFC_CS3/QSPI_DIO_B3/IIC3_SDA/FTM7_EXTCLK	F18 LS1021A_QSPI_B_IO3 R558 10K → P1V8_ARM
IFC_AD04/CFG_GPINPUT4		QSPI_B_D3 (F18)	
IFC_AD05/CFG_GPINPUT5		IFC_WE0/CFG_ENG_USE0	F14 LS1021A_IFC_WE_B 20k internal PU R532 1.0K → GND
IFC_AD06/CFG_GPINPUT6		IFC_CLE/CFG_RCW_SRC8	E17 LS1021A_IFC_CLE cfg_rcw_src8
IFC_AD07/CFG_GPINPUT7		IFC_OE/CFG_ENG_USE1	E16 LS1021A_IFC_OE_B 20k internal PU DNI R534 1.0K
IFC_AD08/CFG_RCW_SRC0/SPI1_PCS1		IFC_AVD	C16 LS1021A_IFC_AVD
IFC_AD09/CFG_RCW_SRC1/SPI1_PCS2		IFC_BCTL	E14 IFC buffer control (N.C.)
IFC_AD10/CFG_RCW_SRC2/SPI1_PCS3		IFC_TE/CFG_IFC_TE	D14 cfg_ifc_te 20k internal PU 33k internal PU R535 4.70K → GND
IFC_AD11/CFG_RCW_SRC3/SPI1_PCS4		IFC_CLK0	A17 LS1021A_IFC_CLK0
IFC_AD12/CFG_RCW_SRC4/SPI1_PCS5		IFC_CLK1	B17 LS1021A_IFC_CLK1
IFC_AD13/CFG_RCW_SRC5/SPI1_SOUT		IFC_NDDDR_CLK	C14 LS1021A_IFC_NDDDR_CLK
IFC_AD14/CFG_RCW_SRC6		IFC_NDDQS	D16 LS1021A_IFC_NDDQS
IFC_AD15/CFG_RCW_SRC7		IFC_WP0	E18 LS1021A_IFC_WP0_B R541 4.70K → P1V8_ARM
IFC_A16/QSPI_CS_A0 pull-down		IFC_RB0	F16 LS1021A_IFC_RB0_B R539 10K
IFC_A17/QSPI_CS_A1 pull-up		IFC_RB1/SPI1_SIN	F15 LS1021A_IFC_RB1_B R538 10K
IFC_A18/QSPI_CK_A			
IFC_A19/QSPI_CS_B0			
IFC_A20/QSPI_CS_B1			
IFC_A21/QSPI_CK_B/CFG_DRAM_TYPE CFG_DRAM_TYPE = 1 ==> DDR3			
IFC_A22/QSPI_DIO_A0/IFC_WP1			
IFC_A23/QSPI_DIO_A1/IFC_WP2			
IFC_A24/QSPI_DIO_A2/IFC_WP3			
IFC_A25/GPIO2_25/QSPI_DIO_A3/FTM5_CH0/IFC_RB2/IFC_CS4			
IFC_A26/GPIO2_26/FTM5_CH1/IFC_RB3/IFC_CS5			
IFC_A27/GPIO2_27/QSPI_DQS/FTM5_EXTCLK/IFC_CS6			
QSPI_B_D2 (C15)		GPIO2_15/IFC_PERR/QSPI_DIO_B2/FTM6_EXTCLK	C15 LS1021A_QSPI_B_IO2 R557 10K
QSPI_B_D0 (D15)		GPIO2_13/IFC_PAR0/QSPI_DIO_B0/FTM6_CH0	D15 LS1021A_QSPI_B_IO0
QSPI_B_D1 (E13)		GPIO2_14/IFC_PAR1/QSPI_DIO_B1/FTM6_CH1	E13 LS1021A_QSPI_B_IO1

LS1021AXN7KQB
FC-PBGA_19MM_19MM_0_8MM

Single Oscillator Source: differential / sysclk

cfg_eng_use0
1: SYSCLK
0: DIFF_SYSCLK+/-
cfg_eng_use1

IFC_PERR: schematic open;
AN4878 recmd pull-up to BVdd

FPGA QSPI PINOUTS

QSPI_CLK	W23
QSPI_CS0	W25
QSPI_Q0	W24
QSPI_Q1	AA24
QSPI_Q2	AA25
QSPI_Q3	Y22

P1V8_ARM

For LS1021A:
IFC_A16 pulled donw
IFC_A17 pulled up @ power-on reset.

R517 4.70K / R526 10K	LS1021A_QSPI_A_CS0	QSPI_A_CS0	C8
	LS1021A_QSPI_A_CS1	QSPI_A_CS1	D8
	LS1021A_QSPI_A_CLK	QSPI_A_CLK	C9
	LS1021A_QSPI_B_CS0	QSPI_B_CS0	D9
	LS1021A_QSPI_B_CS1	QSPI_B_CS1	C10
R527 10K	LS1021A_QSPI_B_CLK	QSPI_B_CLK	D10
	LS1021A_QSPI_A_IO0	QSPI_A_D0	C11
	LS1021A_QSPI_A_IO1	QSPI_A_D1	D11
	LS1021A_QSPI_A_IO2	QSPI_A_D2	C12
R518 10K	LS1021A_QSPI_A_IO3	QSPI_A_D3	D12
R531 10K	LS1021A_IFC_ADDR26	GPIO2_26	C13
R533 10K	LS1021A_IFC_ADDR27	GPIO2_27	D13

LS1021A_IFC_AD00	cfg_gpinput0	A7	
LS1021A_IFC_AD01	cfg_gpinput1	B8	
LS1021A_IFC_AD02	cfg_gpinput2	A8	
LS1021A_IFC_AD03	cfg_gpinput3	B9	
LS1021A_IFC_AD04	cfg_gpinput4	A9	
LS1021A_IFC_AD05	cfg_gpinput5	A10	
LS1021A_IFC_AD06	cfg_gpinput6	B11	
LS1021A_IFC_AD07	cfg_gpinput7	A11	
LS1021A_IFC_AD08	cfg_rcw_src0	B12	
LS1021A_IFC_AD09	cfg_rcw_src1	A12	
LS1021A_IFC_AD10	cfg_rcw_src2	A13	
LS1021A_IFC_AD11	cfg_rcw_src3	B14	
LS1021A_IFC_AD12	cfg_rcw_src4	A14	
LS1021A_IFC_AD13	cfg_rcw_src5	B15	
LS1021A_IFC_AD14	cfg_rcw_src6	A15	
LS1021A_IFC_AD15	cfg_rcw_src7	A16	

LS1021A_QSPI_B_CS0	LS1021A_QSPI_B_CS0	P34
LS1021A_QSPI_B_CLK	LS1021A_QSPI_B_CLK	P34
LS1021A_QSPI_B_IO0	LS1021A_QSPI_B_IO0	P34
LS1021A_QSPI_B_IO1	LS1021A_QSPI_B_IO1	P34
LS1021A_QSPI_B_IO2	LS1021A_QSPI_B_IO2	P34
LS1021A_QSPI_B_IO3	LS1021A_QSPI_B_IO3	P34
LS1021A_IFC_ADDR26	LS1021A_IFC_ADDR26	P34
LS1021A_IFC_ADDR27	LS1021A_IFC_ADDR27	P34

FPGA QSPI

LS1021A to FPGA's QSPI Flash Upgrade USING QSPI-B PORT

NO LONGER NEED 2 SPI FLASH DEVICES
REF: XAPP1280 & XAPP1191

LS1021A - NOR QSPI FLASH 1Gbits USING QSPI-A PORT

DNI U25 128MB (1Gb)
MT25QU01GBBB8E12-0SIT

P1V8_ARM	VCC_B4	B4	
C485 0.10uF 10V			
	DNU_A2	A2	
	DNU_A3	A3	
	DNU_A5	A5	
LS1021A_QSPI_A_CS0	S#	C2	
LS1021A_QSPI_A_CLK	C	B2	
LS1021A_QSPI_A_IO0	DQ0	D3	
LS1021A_QSPI_A_IO1	DQ1	D2	
LS1021A_QSPI_A_IO2	DQ2/W#	C4	
LS1021A_QSPI_A_IO3	DQ3	D4	
	DNU_B1	B1	
	DNU_B5	B5	
	DNU_C1	C1	
	DNU_C3	C3	
	DNU_C5	C5	
DNI R516 4.70K → P1V8_ARM	RESET#	A4	
	DNU_D1	D1	
	DNU_D5	D5	
DNI C484 10uF 10V			
	DNU_E1	E1	
	DNU_E2	E2	
	DNU_E3	E3	
	DNU_E4	E4	
	DNU_E5	E5	
	VSS_B3	B3	

TPBGA25_6MM_8MM_1MM

LS1021A: DEBUG LEDs

P1V8_ARM
C205 0.10uF 10V
P3V3_SYS
C206 0.10uF 10V

U1 TXS0104EZXUR

	VCCA	B2	
	VCCB	B1	
LS1021A_GPIO2_10	A1	A1	
LS1021A_GPIO2_11	A2	A2	
LS1021A_GPIO1_20	A3	A3	
LS1021A_GPIO1_22	A4	A4	
P1V8_ARM R7 0 / R6 DNI	OE	B3	
	GND	B4	
	B1	C1	U1_C1 R4 240 D4_CA → D4
	B2	C2	U1_C2 R3 240 D3_CA → D3
	B3	C3	U1_C3 R2 240 D2_CA → D2
	B4	C4	U1_C4 R1 240 D1_CA → D1

BGA12_2_5MMX2MMX0_50MM

GREEN TLMG1100-GS08

P20 LS1021A_GPIO1_20
P20 LS1021A_GPIO1_22

LS1021A - EEPROM

P3V3_SYS
C537 0.1UF 16V
U37
LS1021A - EEPROM 32Kbits
24LC32AT-I/MNY

	A0	1	
	A1	2	
R851 DNI	A2	3	
	VCC	8	
	WP	7	R571 4.70K
P50,53,54 LS1021A_I2C2_SDA_3V3 R211 0	SDA	5	
P50,53,54 LS1021A_I2C2_SCL_3V3 R210 0	SCL	6	
	VSS	4	
	GND_PAD	9	

TDFN-8_2MMX3MM_0_5MM_PAD

06.19.2018
REWORK REV40.0x
I2C addr 0x50 to 0x54
1. Remove R851
2. Jumper wire from R851.2 to U37.8
3. R851 should be pullup.

DESIGN NOTE:
I2C ADDR: 0x50 ==> 0x54
I2CADDR = 1010_A2.A1.A0.R/W#

CFG_RCW_SRC[0:8]

P1V8_ARM

R119	DNI		
R116	DNI		
R136	10K		
R556	DNI		
R133	DNI		
R113	DNI		
R114	DNI		
R110	DNI		
R537	DNI		
R118	4.70K	LS1021A_IFC_AD08 cfg_rcw_src0	0
R117	4.70K	LS1021A_IFC_AD09 cfg_rcw_src1	0
R135	DNI	LS1021A_IFC_AD10 **cfg_rcw_src2**	1
R555	4.70K	LS1021A_IFC_AD11 cfg_rcw_src3	0
R134	4.70K	LS1021A_IFC_AD12 cfg_rcw_src4	0
R112	4.70K	LS1021A_IFC_AD13 cfg_rcw_src5	0
R115	4.70K	LS1021A_IFC_AD14 cfg_rcw_src6	0
R111	4.70K	LS1021A_IFC_AD15 cfg_rcw_src7	0
R536	4.70K	LS1021A_IFC_CLE cfg_rcw_src8	0

BOOT FROM:
cfg_rcw_src[0:8] = 0_0100_0000 ==> Table 4-9: SD/eSDHC

Title: **PG18: LS1021A QSPI and GPIOs**

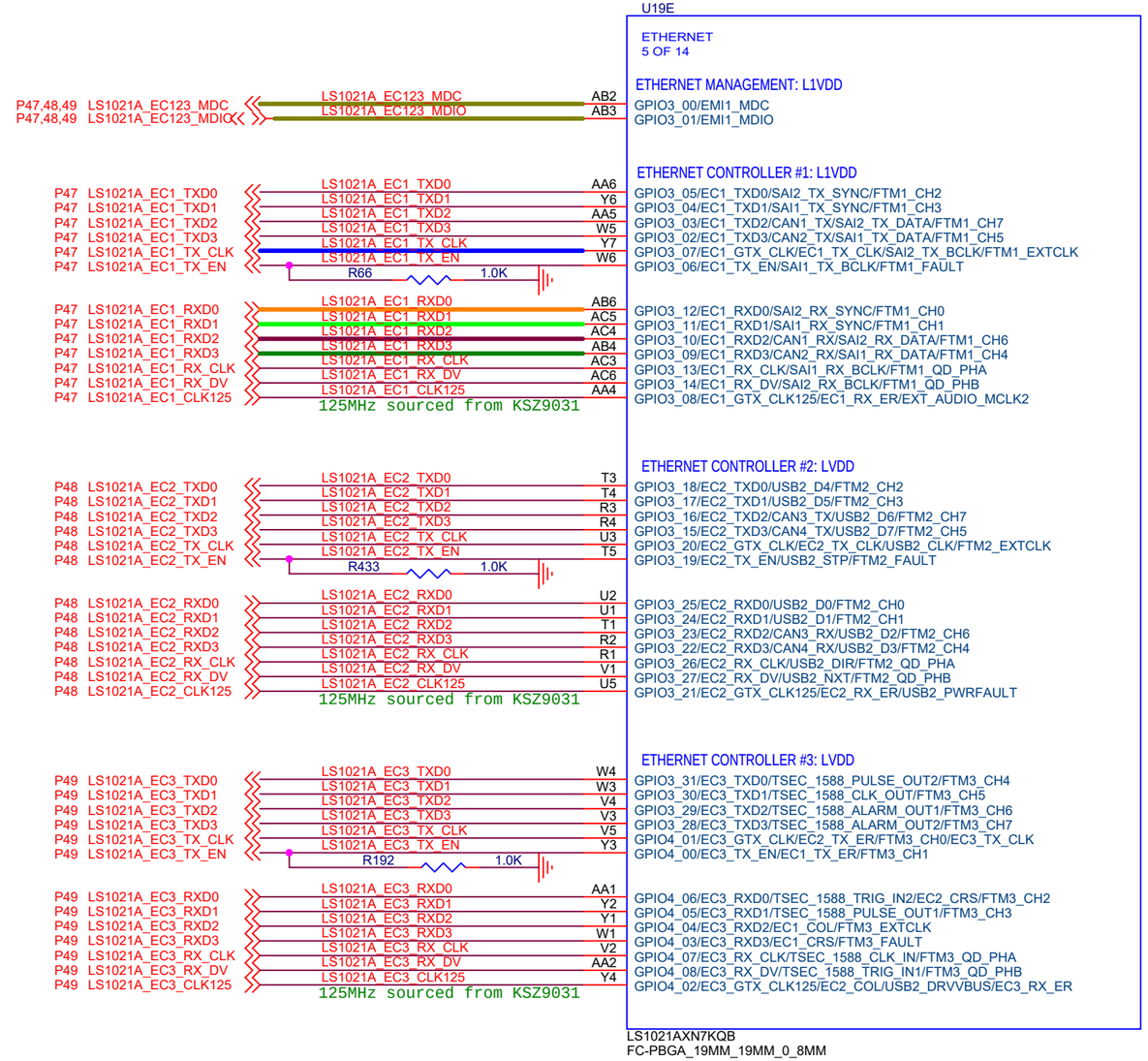
Size	Document Number	Rev
Custom	SCH-000012-00	04.01
Date: Tuesday, June 19, 2018	Sheet 18 of 55	

LS1021A - ETHERNET CONTROLLER

DESIGN NOTES:

1. Need to verify that signal LS1021A_EC1/2/3_CLK125 are configured correctly. These pins are outputs from the PHY chips ... a). measure the frequency, b). make sure EC1/2/3_GTX_CLK125 are the right input port for 125MHz clock for RGMII Ethernet controller.

POWER RAIL: L1VDD
POWER RAIL: LVDD



Title: PG19: LS1021A ENET CONTROLLERS		
Size: Custom	Document Number: SCH-000012-00	Rev: 04.01
Date: Tuesday, June 19, 2018	Sheet 19 of 55	

DURING BOUNDARY SCAN TEST:
TEST_SEL_B at U19.F3 must be tied low "0" during BST. *** Need to make change ***
SCAN_MODE_B at U19.G3 must be held high. *** Good ***
PORESET_B at U19.G9 must be low. *** Need to re-visit ***
EVT2_B at U19.A6 must be held high *** Good***

R552 4.70K
R553 4.70K
R554 4.70K
P1V8_ARM

U19F
P1V8_ARM
O1VDD
SCAN_MODE
TEST_SEL
P1V8_ARM
6 IRQ: O1VDD,O1VDD,L1VDD,LVDD,DVDD,DVDD
IRQ0
IRQ1
IRQ2
GPIO1_23/IRQ3
GPIO1_24/IRQ4/SDHC_VS
GPIO1_25/IRQ5/SDHC_CLK_SYNC_IN/SPI2_PCS5
P1V8_ARM
OVDD, TA_BB_VDD
TA_TMP_DETECT
TA_BB_TMP_DETECT
O1VDD P1V8_ARM
PORESET
HRESET
RESET_REQ
OVDD P1V8_ARM
TDI
TDO
TCK
TMS
TRST
P1V8_ARM
O1VDD,OVDD
SYSCLK
DDRCLK
O1VDD
DIFF_SYSCLK
DIFF_SYSCLK LVDS
O1VDD,TA_BB_VDD
GPIO1_14/RTC
TA_BB_RTC
LS1021AXN7KQB
FC-PBGA_19MM_19MM_0_8MM

SYSTEM LOGIC
6 OF 14
L1VDD=P1V8_ARM
LVDD=P1V8_ARM
O1VDD=P1V8_ARM
OVDD=P1V8_ARM
D1VDD=P1V8_ARM
DVDD1=P1V8_ARM
DVDD2=P1V8_ARM
RESERVED
EVENT:O1VDD
TD1_ANODE
TD1_CATHODE
EVT0
EVT1
EVT2
EVT3
EVT4
GPIO2_24/EVT9
I2C1:D1VDD
D1VDD=P1V8_ARM
IIC1_SCL
IIC1_SDA
I2C2:DVDD
DVDD1=P1V8_ARM
GPIO4_27/IIC2_SCL/SDHC_CD/SPI2_PCS3
GPIO4_28/IIC2_SDA/SDHC_WP/SPI2_PCS4
DUART1: DVDD DVDD=P1V8_ARM
M1:LPUART1_SIN
N1:DUART1_SOUT
N4:DUART1_CTS
N3:DUART1_RTS
GPIO1_17/UART1_SIN
GPIO1_15/UART1_SOUT
GPIO1_21/UART1_CTS/UART3_SIN/LPUART2_SIN/SPI2_SIN/2D-ACE_VSYNC
GPIO1_19/UART1_RTS/UART3_SOUT/LPUART2_SOUT/SPI2_SOUT/2D-ACE_HSYNC
LPUART1: D1VDD D1VDD=P1V8_ARM
P2:LPUART1_SIN
P1:LPUART1_SOUT
P5:LPUART1_CTS
P3:LPUART1_RTS
GPIO1_18/UART2_SIN/LPUART1_SIN/SPI2_PCS1
GPIO1_16/UART2_SOUT/SPI2_PCS0/LPUART1_SOUT
GPIO1_22/UART2_CTS/UART4_SIN/SPI2_SCK/LPUART1_CTS/LPUART4_SIN
GPIO1_20/UART2_RTS/UART4_SOUT/LPUART1_RTS/LPUART4_SOUT/SPI2_PCS2
GPIO1_13/ASLEEP
CKSTP_OUT
CLK_OUT
FA_ANALOG_PIN
FA_ANALOG_G_V

LS1021A contains:
4 - 16550 compliant UARTs.
6 - LPUARTs.

LS1021A_ANODE R386 0
LS1021A_CATHODE R385 0
R489 4.70K
R490 4.70K
R520 4.70K
R519 4.70K
R524 4.70K
P1V8_ARM
J6
K6
C5 EVT0_B
D5 EVT1_B
A6 EVT2_B
B6 EVT3_B
C7 EVT4_B
D7 LS1021A_GPIO2_24
N6 LS1021A_I2C1_SCL
P6 LS1021A_I2C1_SDA
LS1021A_I2C1_SCL P53
LS1021A_I2C1_SDA P53
I2C1
K1 LS1021A_I2C2_SCL
L1 LS1021A_I2C2_SDA
LS1021A_I2C2_SCL P53
LS1021A_I2C2_SDA P53
I2C2
=> UART/USB
M1 DUART1_SIN
N1 DUART1_SOUT
N4 LS1021A_GPIO1_21
N3 LS1021A_GPIO1_19
DUART1_SIN P52
DUART1_SOUT P52
LS1021A_GPIO1_21 P34
LS1021A_GPIO1_19 P34
=> FPGA
P2 LS1021A_GPIO1_18
P1 LS1021A_GPIO1_16
P5 LS1021A_GPIO1_22
P3 LS1021A_GPIO1_20
LS1021A_GPIO1_18 P34
LS1021A_GPIO1_16 P34
LS1021A_GPIO1_22 P18
LS1021A_GPIO1_20 P18
=> FPGA
LS1021A_SLEEP P34
E6
E11 RSRV_CKSTOP_OUT_B
R528 4.70K
P1V8_ARM
C6 LS1021A_CLK_OUT
F12
G13
TP11

P1V8_ARM
R491 1.0K U19_G3_SCAN_MODE_B
R493 1.0K U19_F3_TEST_SEL_B
G3
F3
P34 1PPS_OUT1
P34 FPGA1V8_B48_W31
P34 FPGA1V8_B48_V32
P25 LS1021A_IO1_23_DONE
P25 LS1021A_IO1_24_INITB
P25 LS1021A_IO1_25_PRGB
G6
G8
W7
R5
L2
M2
GPIO1_23
GPIO1_24
GPIO1_25
R496 0 F9
R432 0 U6
LS1021A_POR_B G9
LS1021A_HRS_B E5
LS1021A_RSTREQ_B G5
This is an output
JTAG_TDI E7
JTAG_TDO F7
JTAG_TCK E8
JTAG_TMS F8
U19_F6_TRST_B F6
P1V8_ARM
R868 10K
DNI
F5
H18
P51 CLK1_CMOS_100M
P51 CLK2_CMOS_100M
The RCW[DDR_REFCLK_SEL] ==>
(DIFF_SYSCLK or DDRCLK)
to the DDR PLL.
51.0
51.0
DNI R495
R467 DNI
SYSCLK
DIFF_SYSCLK LVDS Receiver
P51 CLK3R_100M_P
P51 CLK3R_100M_N
F4
G4
R857 22.0 RTC
R858 22.0
RTC_32_768M P34
RTC_E10 E10
TA_BB_RTC R6
R434 4.70K

P1V8_ARM
R446 10.0
10K
10K
10K
10K
R364
R427
R448
R428
JTAG_J6_1
J6
1
2 TMS
3
4 TCK
5
6 TDO
7
8 TDI
9
10
FTSH-105-01-L-D-K
HEADER_2X5_1_27MM_ST_TH
1.27/3.05mm(TH)
JTAG_TMS PIN2
JTAG_TCK PIN4
JTAG_TDO PIN6
JTAG_TDI PIN8
JTAG_TRST_B PIN10
nRESET_J6.10
BST_GND PIN7

P1V8_ARM
U24
ASAK2-32.768KHZ-LRS-T
VCC OUT
GND E/D
XO_2MMX1_6MM
32.768 kHz
C489
0.1UF
25V
XO32.768M
R859 1.0K
P1V8_ARM

BST_GND J6.7
U91
74LVC3G07GT
1A 1Y
2A 2Y
3A 3Y
GND VCC
SOT833-1_1MM_1_9MM_0_5MM
U91_Y1 R865 0 U19_F3_TEST_SEL_B
U91_Y2 R866 0 U68_6_RESET_N
U91_Y3 R867 0
P1V8_ARM

P1V8_ARM
C933 0.1UF
16V
U92
TPS3808G18DRVR
SENSE VCC
MR RST
X ms delay
GND Ct
PAD
PWSON-6_2MMX2MM_0_45MM_PAD
R870 4.70K
R875 0
R876 0
DNI
R869 0
U19_F6_TRST_B
U92_6_RESET_N
R871 4.70K
P1V8_ARM
U92_3_CT
R872 51.1K
C934 0.1UF DNI
16V
=> to DDR3 Reset
DDR3_RST_B_1V8 P24
=> to PHY Resets
LS1021A_EC_RESET_N P20,47,48,49

TRST_B NOTES:
o During BSDL - TRST_B = 0
o Normal Mode - TRST_B = Reset at Power On.
* The NXP Design Guide requires to have this pin be POReset.
It was checked that the POReset is done internally to the chip.
NXP did not acknowledge this finding, hence this circuit is added here, just in case.

Pull-up and no connection.
LS1021A_HRS_B R363 1.0K P1V8_ARM
Pin E5.HRESET from LS1021A to FPGA

This is the reset from CodeWarrior.
JTAG_TRST_B
nRESET_J6.10 from JTAG Conn
R364 0
U68_6_RESET_N
R846 0 U88_P3
U88
NC7WZ17P6X
A1 VCC
A2
Y1
GND Y2
SC-70-6
P1V8_ARM
C216 16V 0.1UF
U88_P6 R880 0
U88_P4 R887 0
LS1021A_POR_B
LS1021A_POR_B: rise/fall time requirement is 10ns max.

LS1021A's RESETS
P1V8_ARM
DNI
SW1
FSMSM
C218 0.1UF 16V
R365 0
U68_4_MR#
R362 4.70K
P1V8_ARM
U68
TPS3808G18DRVR
SENSE VCC
MR RST
X ms delay
GND Ct
PAD
PWSON-6_2MMX2MM_0_45MM_PAD
P1V8_ARM
C932 0.1UF
16V
U68_6_RESET_N
R366 4.70K
P1V8_ARM
U68_3_CT
R835 51.1K
C217 DNI
<VOLTAGE>
LS1021A_RSTREQ_B
Pin G5.RESET_REQ from LS1021A
R845 0
DNI
R360 0
LS1021A_RSTREQ_RB P34

TPS3808G18DRVR
50K ==> 300ms
Open ==> 20ms
Caps ==> CnF/175 +0.5*10^-3 [ns]

Title: PG20: LS1021A POR/JTAG/GPIOs
Size: Custom
Document Number: SCH-000012-00
Rev: 04.01
Date: Tuesday, June 19, 2018
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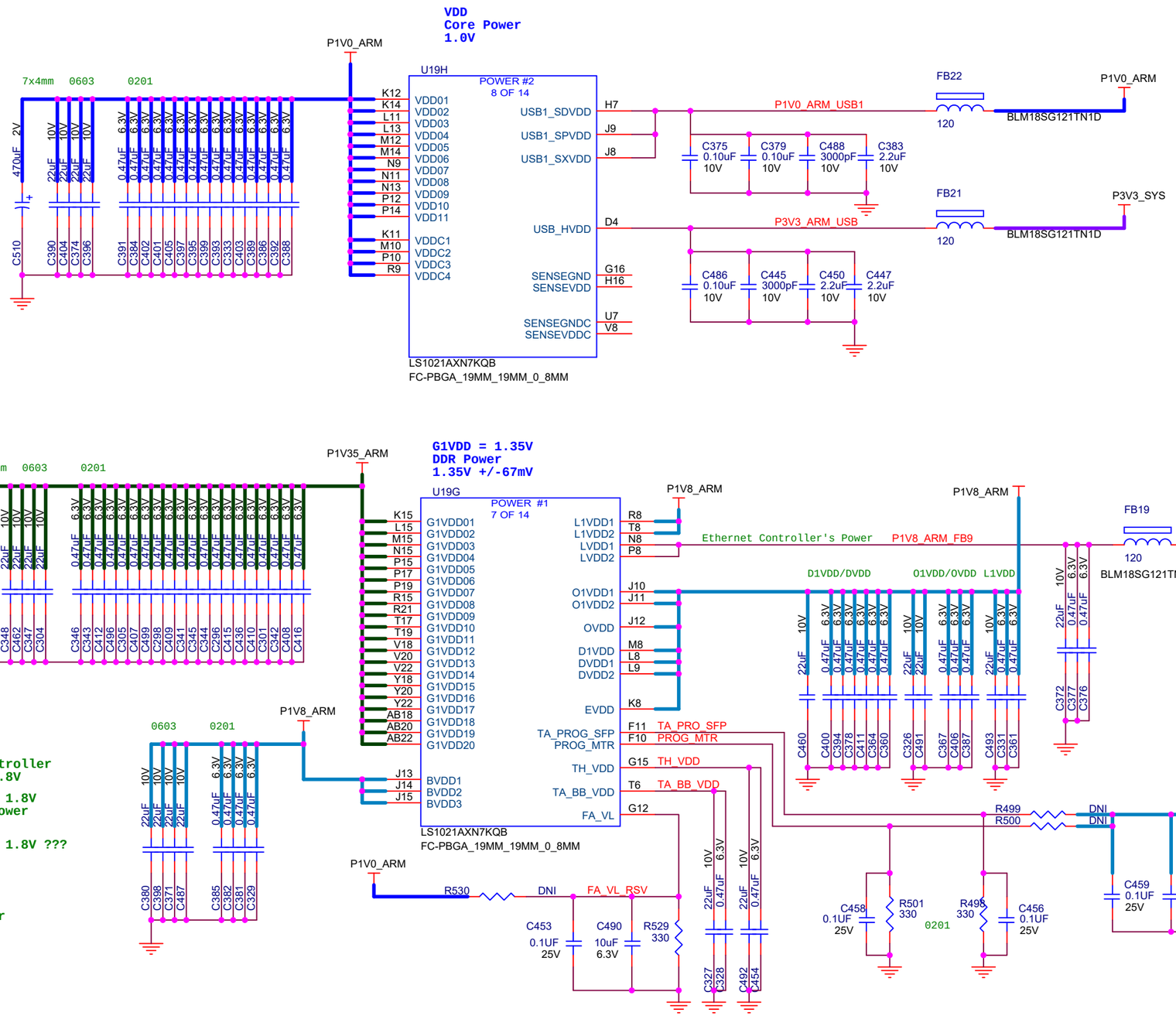
LS1021A - Powers: Core and IO



VDD
Core Power
1.0V

VDD
Core Power
1.0V
Always On

G1VDD = 1.35V
DDR Power
1.35V +/-67mV

BVDD = 1.8V
IFC/SPI Power
Switchable

L1VDD = 1.8V
Ethernet Controller
Switchable 1.8V

O1VDD/OVDD = 1.8V
General IO Power
Always On

D1VDD/DVDD = 1.8V
UART/I2C
Always On

EVDD = 3.3V
eSDHC Power
Always On

TA_PROG_SFP
SFP Fuse Programming

PRO_MTR
Reserved

TH_VDD
Thermal Monitor

TA_BB_VDD
Reserved

FA_VL
Batt Backed Security

Place at least one decoupling capacitor at each VDD, VDDC, TA_BB_VDD, O1VDD, OVDD, BVDD, D1VDD, DVDD, EVDD, L1VDD, LVDD, and G1VDD pin of the device.

These decoupling capacitors should receive their power from separate VDD, VDDC, TA_BB_VDD, O1VDD, OVDD, BVDD, D1VDD, DVDD, EVDD, L1VDD, LVDD, G1VDD, and GND power planes in the PCB, utilizing short traces to minimize inductance.

These capacitors should have a value of 0.1 µF. Only ceramic surface mount technology (SMT) capacitors should be used to minimize lead inductance, preferably 0402 or 0603 sizes.

As presented in Core and platform supply voltage filtering, it is recommended that there be several bulk storage capacitors distributed around the PCB, feeding the VDD, VDDC and other planes (for example, VDD, DVDD, EVDD, LVDD, and G1VDD), to enable quick recharging of the smaller chip capacitors.

NXP recommends that these bulk capacitors be chosen to maintain the positive transient power surges to less than +50 mV (negative transient undershoot should comply with specification of -30 mV) for current steps of up to 2A with a slew rate of 1.5A/µs.

Title: **PG14: LS1021A POWER 1/2**		
Size: Custom	Document Number: **SCH-000012-00**	Rev: 04.01
Date: Tuesday, June 19, 2018	Sheet 21 of 55	

LS1021A - Powers: PLL, SERDES, USB

U19J
POWER #4
10 OF 14

A3	GND001	GND056	K18
A5	GND002	GND057	K20
A18	GND003	GND058	L4
A22	GND004	GND059	L7
B1	GND005	GND060	L10
B3	GND006	GND061	L12
B5	GND007	GND062	L14
B7	GND008	GND063	L16
B10	GND009	GND064	L18
B13	GND010	GND065	L22
B16	GND011	GND066	M7
B18	GND012	GND067	M9
B20	GND013	GND068	M11
C2	GND014	GND069	M13
C4	GND015	GND070	M16
C19	GND016	GND071	M17
C22	GND017	GND072	M18
D2	GND018	GND073	M21
D6	GND019	GND074	N2
D18	GND020	GND075	N7
D20	GND021	GND076	N10
E4	GND022	GND077	N12
E9	GND023	GND078	N14
E12	GND024	GND079	N16
E15	GND025	GND080	N18
E19	GND026	GND081	P4
E22	GND027	GND082	P7
F17	GND028	GND083	P9
F20	GND029	GND084	P11
G2	GND030	GND085	P13
G7	GND031	GND086	P16
G19	GND032	GND087	P18
G22	GND033	GND088	P20
H4	GND034	GND089	P22
H6	GND035	GND090	R7
H8	GND036	GND091	R10
H9	GND037	GND092	R14
H10	GND038	GND093	R16
H11	GND039	GND094	R17
H12	GND040	GND095	T2
H13	GND041	GND096	T7
H14	GND042	GND097	T16
H15	GND043	GND098	T22
H17	GND044	GND099	U4
H20	GND045	GND100	U8
J16	GND046	GND101	U23
J18	GND047	GND102	V6
J19	GND048	GND103	W2
J22	GND049	GND104	Y5
K2	GND050	GND105	Y17
K7	GND051	GND106	AA3
K9	GND052	GND107	AB1
K10	GND053	GND108	AB5
K13	GND054	GND109	AC2
K16	GND055		

LS1021AXN7KQB
FC-PBGA_19MM_19MM_0_8MM

U19K
POWER #5
11 OF 14

T9	S1GND01	X1GND01	V10
T11	S1GND02	X1GND02	V11
T12	S1GND03	X1GND03	V13
T13	S1GND04	X1GND04	V14
T15	S1GND05	X1GND05	W9
U12	S1GND06	X1GND06	W12
AA7	S1GND07	X1GND07	W15
AA8	S1GND08	X1GND08	Y9
AA9	S1GND09	X1GND09	Y12
AA10	S1GND10	X1GND10	Y15
AA11	S1GND11		
AA12	S1GND12		
AA13	S1GND13		
AA14	S1GND14		
AA15	S1GND15		
AA16	S1GND16		
AA17	S1GND17		
AB7	S1GND18		
AB9	S1GND19		
AB12	S1GND20		
AB15	S1GND21		
AB17	S1GND22		
AC7	S1GND23		
AC9	S1GND24		
AC12	S1GND25		
AC15	S1GND26		
AC17	S1GND27		

LS1021AXN7KQB
FC-PBGA_19MM_19MM_0_8MM

This circuit is intended to filter noise in the PLL's resonant frequency range from a 500 kHz to 10 MHz range.

P1V8_ARM

R457 5.1 P1V0_AVDD_CGA1
C373 2.2uF 10V Low ESL
C370 10uF 6.3V
C452 0.47uF 6.3V

R487 5.1 P1V0_AVDD_PLAT
C449 2.2uF 10V Low ESL
C448 10uF 6.3V
C451 0.47uF 6.3V

R470 5.1 P1V0_AVDD_D1
C417 2.2uF 10V Low ESL
C457 10uF 6.3V
C414 0.47uF 6.3V

U19L
POWER #6
12 OF 14

G11	AVDD_CGA1	AVDD_SD1_PLL1	U11
		AGND_SD1_PLL1	U10
G10	AVDD_PLAT	AVDD_SD1_PLL2	U14
		AGND_SD1_PLL2	U13
K17	AVDD_D1		

LS1021AXN7KQB
FC-PBGA_19MM_19MM_0_8MM

P1V0_AVDD_SD1_PLL1
C277 3000pF 10V
C276 4.7uF 25V
C275 47uF 10V
R413 0.33
R412 0

P1V0_AVDD_SD1_PLL2
C278 3000pF 10V
C279 4.7uF 25V
C280 47uF 10V
R415 0.33
R414 0

P1V35_ARM

AVDD_SD1_PLLx	= 1.35V
AVDD_CG1	= 1.8V
AVDD_PLAT	= 1.8V
AVDD_D1	= 1.8V
S1VDD	= 1.0V
X1VDD	= 1.35V

P1V0_ARM
FB17 BLM18SG121TN1D 120
P1V0_S1VDDX
C339 2.2uF 10V
C274 2.2uF 10V
C272 3000pF 10V
C338 1500pF 10V
C273 0.47uF 6.3V
C336 0.47uF 6.3V
C334 0.47uF 6.3V

U19I
POWER #3
9 OF 14

R11	S1VDD1	
R12	S1VDD2	
R13	S1VDD3	
V9	X1VDD1	
V12	X1VDD2	
V15	X1VDD3	
Y8	X1VDD4	

LS1021AXN7KQB
FC-PBGA_19MM_19MM_0_8MM

P1V35_ARM
FB18 BLM18SG121TN1D 120
P1V35_X1VDD
C306 22uF 10V
C498 22uF 10V
C295 22uF 10V
C337 2.2uF 10V
C285 2.2uF 10V
C286 3000pF 10V
C340 1500pF 10V
C335 0.47uF 6.3V
C330 0.47uF 6.3V
C332 0.47uF 6.3V

Title: PG22: LS1021A POWER 2/2
Size: Custom
Document Number: SCH-000012-00
Rev: 04.01
Date: Tuesday, June 19, 2018
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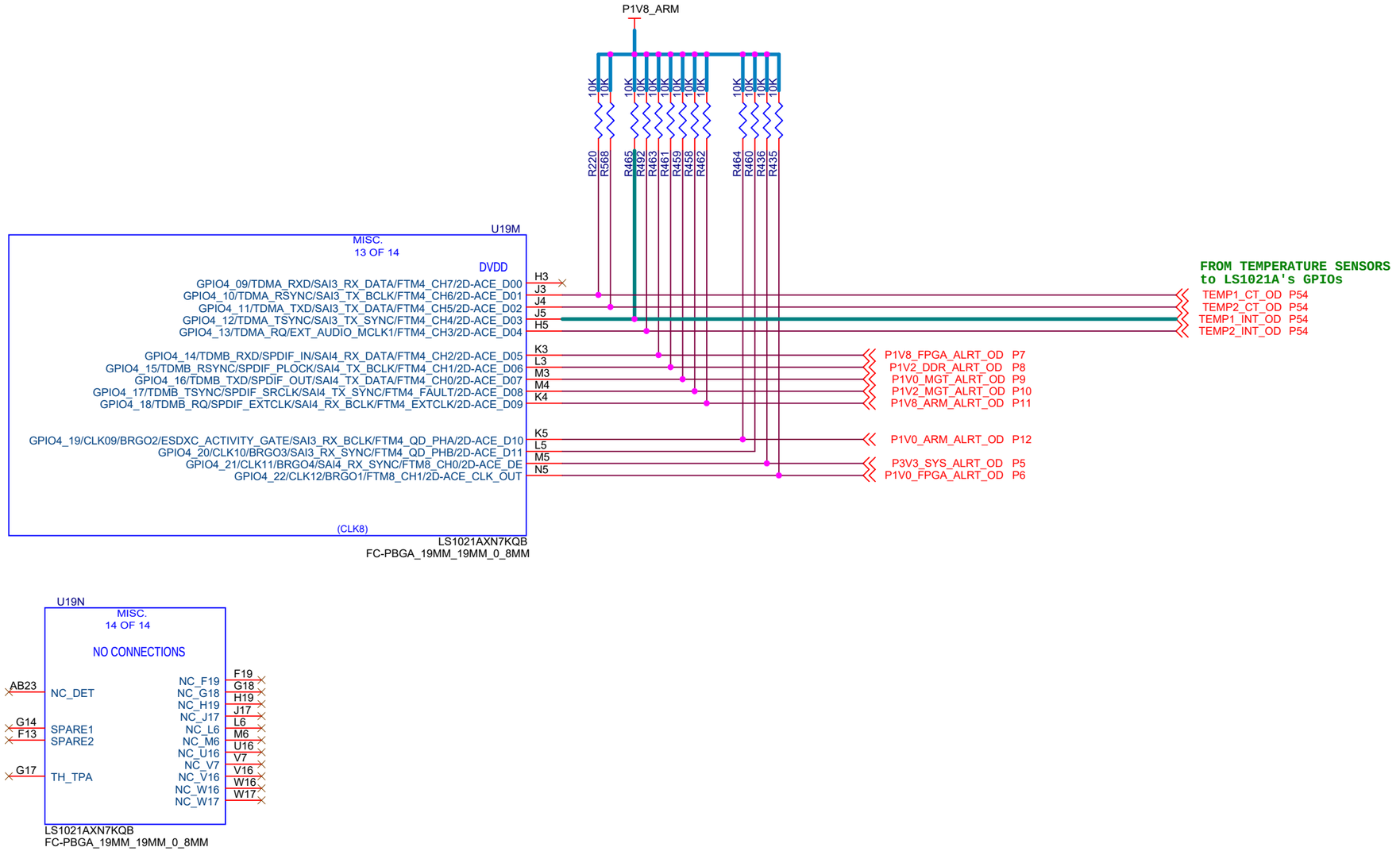


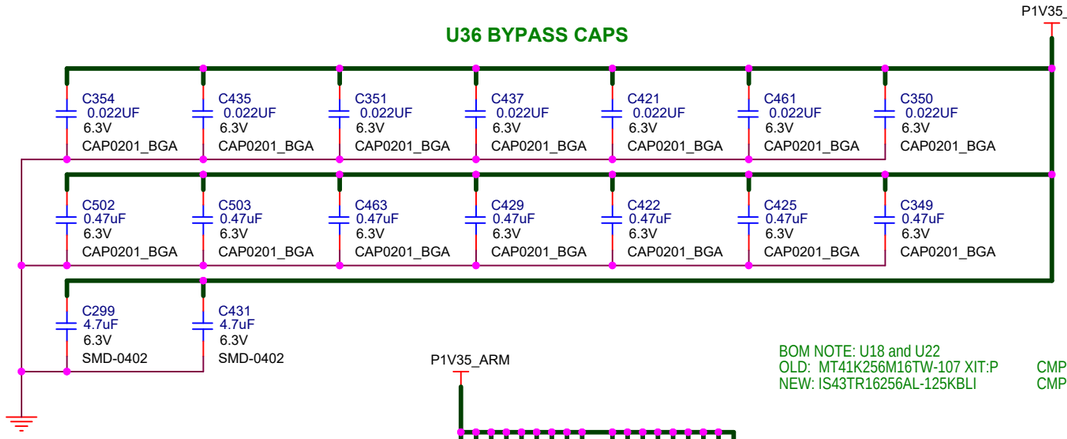
Title: **PG23: LS1021A DDR3 COMPONENTS**

Size	Document Number	Rev
Custom	SCH-000012-00	04.01

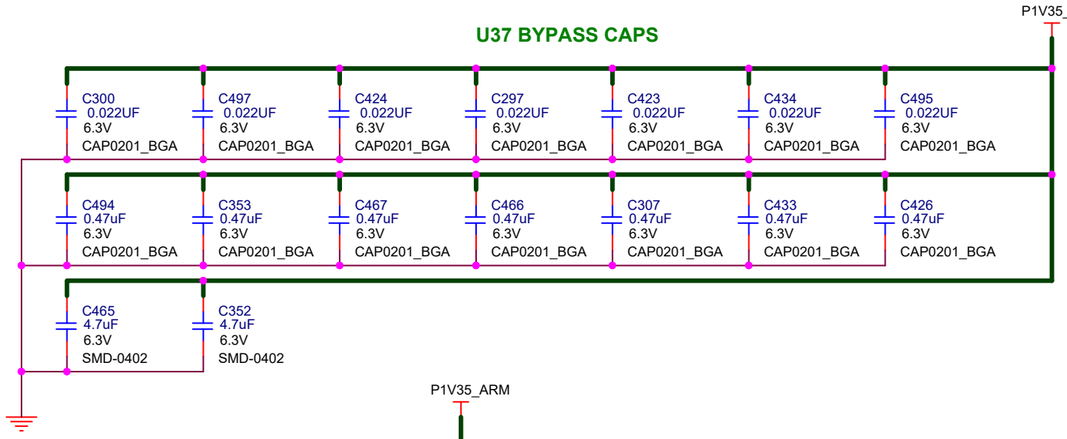
Date: Tuesday, June 19, 2018 Sheet 23 of 55

LS1021A - DDR3 INTERFACE

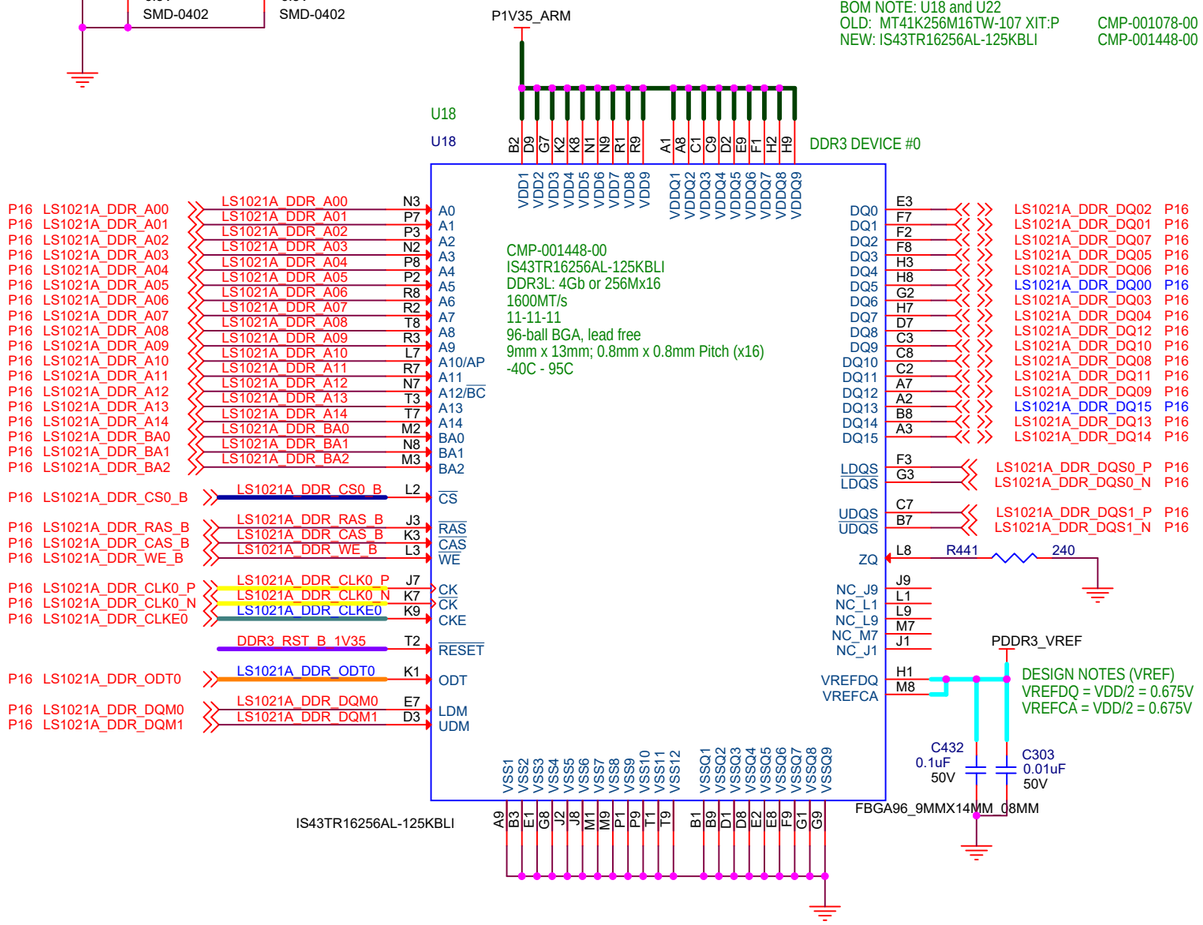
U36 BYPASS CAPS

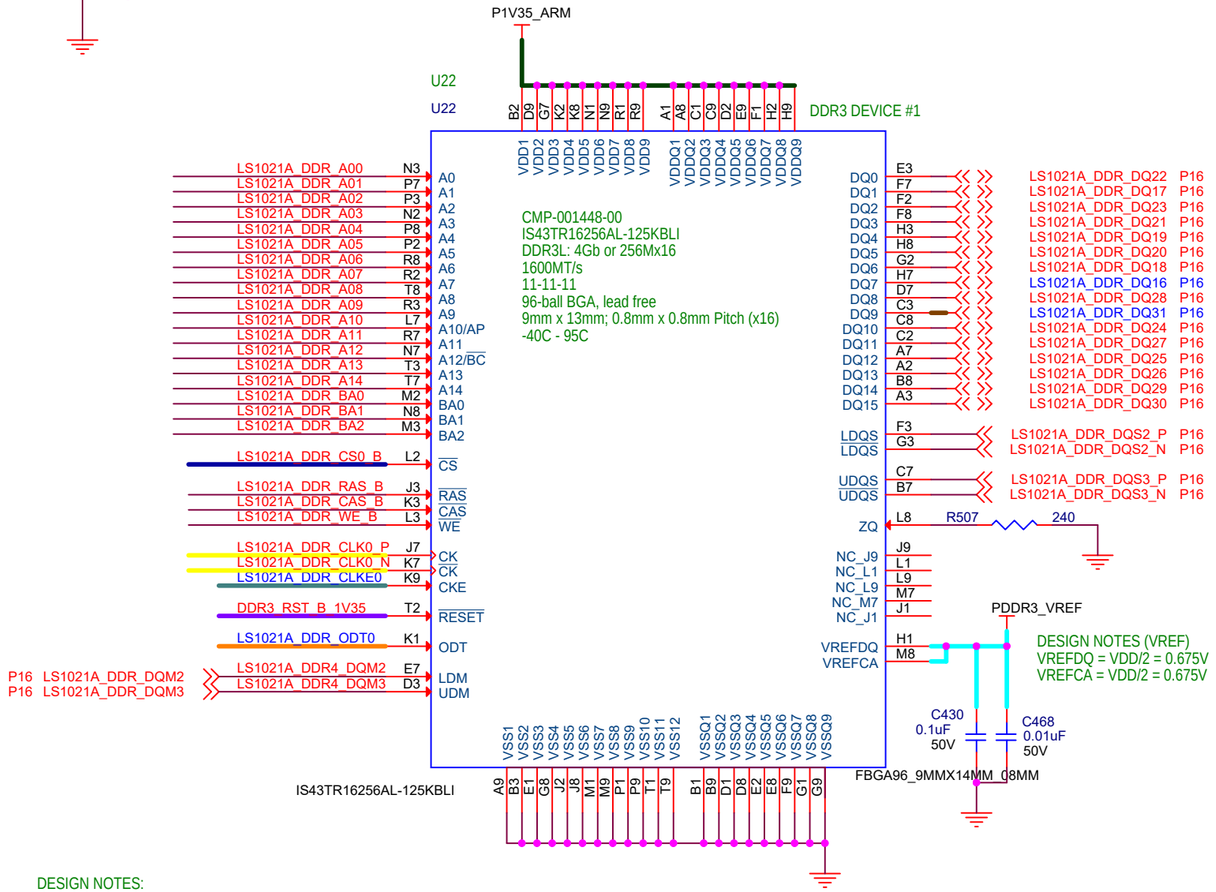


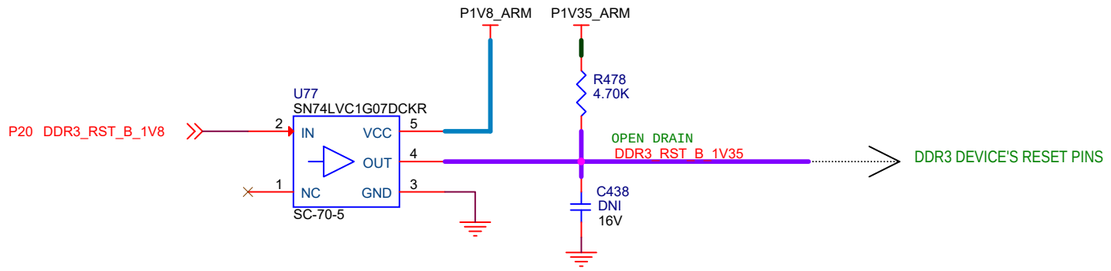
U37 BYPASS CAPS



BOM NOTE: U18 and U22
OLD: MT41K256M16TW-107 XIT:P CMP-001078-00
NEW: IS43TR16256AL-125KBLI CMP-001448-00







DESIGN NOTES:
Power Rails:
1. PDDR_VTT = 1.35V
2. PDDR_VREF = 1.35/2
2. P1V35

DESIGN NOTES:
In the LS1021A reference design, pins J1,J9,L1,L9,M7 of MT41K256M16HA-125:E
are connected to DDR_ODT1,DDR_CLKE1,DDR_CS1,DDR_ZQ1,DDR_A15, respectively.

Title: PG24: DDR3L DEVICES		
Size: Custom	Document Number: SCH-000012-00	Rev: 04.01
Date: Tuesday, June 19, 2018	Sheet 24 of 55	

FPGA - BANK 0 : CONFIGURATION

M[2:0]	MODE
101	JTAG (DON'T CARE)
001	MASTER SPI

U83
TPS3808G18DRVR
PWSON-6_2MMX2MM_0_45MM_PAD
C905 0.1UF 16V
R756 0
R755 10K
20ms delay

U54A
BANK 0 - CONFIGURATION
XCKU040FFVA1156 A
XCKU040-2FFVA1156I
FFVA1156_35MM_35MM_1MM

U84
REF3012AIDBZT
SOT-23-3
25mA
1.2V

FB23
120 OHM
BLM15EG121SN1D

U43 MX66U51235FZ4I-10G
256Mb
WPDFN8-8MMX6MM_1_27MM_pad

D30
RED
DONE: LED OFF
SML-P11VTT86

FPGA CONFIG
MASTER SPI X4

ADAPTER BOARD

Xilinx JTAG Conn (SMD)

Pitch	2.00 mm
Contact Length	3.60 mm

1.27MM Conn (TH)

Pitch	1.27 mm
Contact Length	3.05 mm

MODEM

1.27MM Conn (TH)

Pitch	1.27 mm
Contact Length	3.05 mm

J9
FTSH-105-01-L-D-K
HEADER_2X5_1.27MM_ST_TH
1.27/3.05mm(TH)

LAYOUT NOTES: QSPI U43
FPGA_QSPI_CCLK, FPGA_QSPI_CS_B, FPGA_QSPI_IO[3:0] – trace length match

Temperature-sensing diode pins
DXP: Anode
DXN: Cathode
When not used, tie to GND.
To use the thermal diode an appropriate external thermal monitoring IC must be added.
Consult the external DXP thermal monitoring IC data sheet for usage guidelines.

Title: PG25: FPGA CONFIGURATION
Size: Custom
Document Number: SCH-000012-00
Rev: 04.01
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U54H

BANK 65 HR H

XCKU040FFVA1156

AD00_P/N and AD08_P/N are not used, since the pins might be conflict with SPIx8 Master Mode Configuration.

(CONFIG CLK) IO_L24P_T3U_N10_EMCCLK_65_K20	K20			
IO_L24N_T3U_N11_DOUT_CSO_B_65_K21	K21			
IO_T3U_N12_PERSTN0_65_K22	K22			
IO_L23P_T3U_N8_I2C_SCLK_65_N21	N21			
IO_L23N_T3U_N9_I2C_SDA_65_M21	M21			
IO_L22P_T3U_N6_DBC_AD0P_D04_65_M20	M20			
IO_L22N_T3U_N7_DBC_AD0N_D05_65_L20	L20			
IO_L21P_T3L_N4_AD8P_D06_65_R21	R21			
IO_L21N_T3L_N5_AD8N_D07_65_R22	R22			
IO_L20P_T3L_N2_AD1P_D08_65_P20	P20	SYSMON_AD01_P	SYSMON_AD01_P	P15
IO_L20N_T3L_N3_AD1N_D09_65_P21	P21	SYSMON_AD01_N	SYSMON_AD01_N	P15
IO_L19P_T3L_N0_DBC_AD9P_D10_65_N22	N22	SYSMON_AD09_P	SYSMON_AD09_P	P13
IO_L19N_T3L_N1_DBC_AD9N_D11_65_M22	M22	SYSMON_AD09_N	SYSMON_AD09_N	P13
IO_L18P_T2U_N10_AD2P_D12_65_R23	R23	SYSMON_AD02_P	SYSMON_AD02_P	P15
IO_L18N_T2U_N11_AD2N_D13_65_P23	P23	SYSMON_AD02_N	SYSMON_AD02_N	P15
IO_L17P_T2U_N8_AD10P_D14_65_R25	R25	SYSMON_AD10_P	SYSMON_AD10_P	P13
IO_L17N_T2U_N9_AD10N_D15_65_R26	R26	SYSMON_AD10_N	SYSMON_AD10_N	P13
IO_L16P_T2U_N6_QBC_AD3P_A00_D16_65_T24	T24	SYSMON_AD03_P	SYSMON_AD03_P	P15
IO_L16N_T2U_N7_QBC_AD3N_A01_D17_65_T25	T25	SYSMON_AD03_N	SYSMON_AD03_N	P15
IO_L15P_T2L_N4_AD11P_A02_D18_65_T27	T27	SYSMON_AD11_P	SYSMON_AD11_P	P15
IO_L15N_T2L_N5_AD11N_A03_D19_65_R27	R27	SYSMON_AD11_N	SYSMON_AD11_N	P15
IO_L14P_T2L_N2_GC_A04_D20_65_P24	P24			
IO_L14N_T2L_N3_GC_A05_D21_65_P25	P25			
IO_T2U_N12_CSI_ADV_B_65_N27	N27			
IO_L13P_T2L_N0_GC_QBC_A06_D22_65_P26	P26			
IO_L13N_T2L_N1_GC_QBC_A07_D23_65_N26	N26			
VREF_65_J21	J21			
IO_L12P_T1U_N10_GC_A08_D24_65_N24	N24			
IO_L12N_T1U_N11_GC_A09_D25_65_M24	M24			
IO_T1U_N12_PERSTN1_65_N23	N23			
IO_L11P_T1U_N8_GC_A10_D26_65_M25	M25			
IO_L11N_T1U_N9_GC_A11_D27_65_M26	M26			
IO_L10P_T1U_N6_QBC_AD4P_A12_D28_65_L22	L22	SYSMON_AD04_P	SYSMON_AD04_P	P15
IO_L10N_T1U_N7_QBC_AD4N_A13_D29_65_K23	K23	SYSMON_AD04_N	SYSMON_AD04_N	P15
IO_L9P_T1L_N4_AD12P_A14_D30_65_L25	L25			
IO_L9N_T1L_N5_AD12N_A15_D31_65_K25	K25			
IO_L8P_T1L_N2_AD5P_A16_65_L23	L23	SYSMON_AD05_P	SYSMON_AD05_P	P15
IO_L8N_T1L_N3_AD5N_A17_65_L24	L24	SYSMON_AD05_N	SYSMON_AD05_N	P15
IO_L7P_T1L_N0_QBC_AD13P_A18_65_M27	M27			
IO_L7N_T1L_N1_QBC_AD13N_A19_65_L27	L27			
IO_L6P_T0U_N10_AD6P_A20_65_J23	J23	SYSMON_AD06_P	SYSMON_AD06_P	P15
IO_L6N_T0U_N11_AD6N_A21_65_H24	H24	SYSMON_AD06_N	SYSMON_AD06_N	P15
IO_L5P_T0U_N8_AD14P_A22_65_J26	J26			
IO_L5N_T0U_N9_AD14N_A23_65_H26	H26			
IO_L4P_T0U_N6_DBC_AD7P_A24_65_J24	J24	SYSMON_AD07_P	SYSMON_AD07_P	P13
IO_L4N_T0U_N7_DBC_AD7N_A25_65_J25	J25	SYSMON_AD07_N	SYSMON_AD07_N	P13
IO_L3P_T0L_N4_AD15P_A26_65_K26	K26			
IO_L3N_T0L_N5_AD15N_A27_65_K27	K27			
IO_L2P_T0L_N2_FOE_B_65_G25	G25			
IO_L2N_T0L_N3_FWE_FCS2_B_65_G26	G26			
IO_T0U_N12_A28_65_H23	H23			
IO_L1P_T0L_N0_DBC_RS0_65_H27	H27			
IO_L1N_T0L_N1_DBC_RS1_65_G27	G27			

10A

P1V8_FPGA

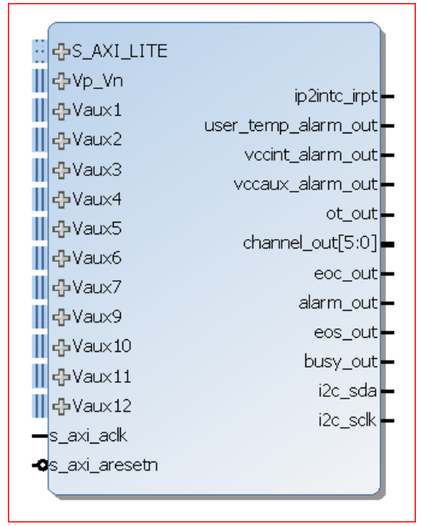
H25	VCCO_65_H25
J22	VCCO_65_J22
L26	VCCO_65_L26
M23	VCCO_65_M23
N20	VCCO_65_N20
P27	VCCO_65_P27
R24	VCCO_65_R24

XCKU040-2FFVA1156I

FFVA1156_35MM_35MM_1MM

SYSMON PORTS:

VP/VN	P1V0_FPGA
SYSMON_AD01	P1V2_DDR
SYSMON_AD02	P1V8_FPGA
SYSMON_AD03	P1V8_MGT
SYSMON_AD04	P1V0_MGT
SYSMON_AD05	P3V3_SYS
SYSMON_AD06	P1V0_ARM
SYSMON_AD07	P1V8_MGTVCCAUX
SYSMON_AD09	P1V35_ARM
SYSMON_AD10	P2V5_SYS
SYSMON_AD11	P1V8_ARM
SYSMON_AD12	P2V5_SYS



Title: **PG26: FPGA'S SYSMON INTF**

Size: Custom | Document Number: **SCH-000012-00** | Rev: 04.01

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U54G

BANK 64 HR G

XCKU040FFVA1156

DESIGN NOTES (INPUTS)
DS892 - Table-9
LVCMOS33
Vil(max) = 0.8V
Vih(min) = 2.0V

DESIGN NOTES (INPUTS)
DS892 - Table-9
LVCMOS18
Vil(max) = 0.63V
Vih(min) = 1.17V

DESIGN NOTES:
DIPSW2 was designed in as a bug tool during bring-up. In production, this switch will be DNI. FPGA needs to reflect this change.

4.70K R818 R819 R820 R821 R822 R823 R824 R826

DIPSW2
218-8LPSTR
SW_DIP16_8POS_SM

AK8	FPGA_DIPSW2_1	1	16	PU_FPGA_DIPSW2_1	R827	39.2
AL8	FPGA_DIPSW2_2	2	15	PU_FPGA_DIPSW2_2	R828	39.2
AM9	FPGA_DIPSW2_3	3	14	PU_FPGA_DIPSW2_3	R829	39.2
AJ9	FPGA_DIPSW2_4	4	13	PU_FPGA_DIPSW2_4	R830	39.2
AJ8	FPGA_DIPSW2_5	5	12	PU_FPGA_DIPSW2_5	R831	39.2
AN8	FPGA_DIPSW2_6	6	11	PU_FPGA_DIPSW2_6	R832	39.2
AP8	FPGA_DIPSW2_7	7	10	PU_FPGA_DIPSW2_7	R833	39.2
AK10	FPGA_DIPSW2_8	8	9	PU_FPGA_DIPSW2_8	R834	39.2

P1V8_FPGA

P3V3_SYS

GREEN D14 TLMG1100-GS08
GREEN D15 TLMG1100-GS08
GREEN D16 TLMG1100-GS08
GREEN D17 TLMG1100-GS08
GREEN D18 TLMG1100-GS08
GREEN D19 TLMG1100-GS08
GREEN D20 TLMG1100-GS08
GREEN D21 TLMG1100-GS08
GREEN D22 TLMG1100-GS08
GREEN D23 TLMG1100-GS08
GREEN D24 TLMG1100-GS08
GREEN D25 TLMG1100-GS08
GREEN D26 TLMG1100-GS08
GREEN D27 TLMG1100-GS08
GREEN D28 TLMG1100-GS08
GREEN D29 TLMG1100-GS08

change to smaller values

FPGA_LED14	R782	261
FPGA_LED15	R781	261
FPGA_LED16	R780	261
FPGA_LED17	R778	261
FPGA_LED18	R777	261
FPGA_LED19	R776	261
FPGA_LED20	R775	261
FPGA_LED21	R774	261
FPGA_LED22	R773	261
FPGA_LED23	R772	261
FPGA_LED24	R771	261
FPGA_LED25	R770	261
FPGA_LED26	R769	261
FPGA_LED27	R768	261
FPGA_LED28	R767	261
FPGA_LED29	R766	261

8 7 6 5 4 3 2 1
1
0

AP9	FPGA_LED27	FPGA_LED14	
AL10	FPGA_LED26	FPGA_LED15	
AM10	FPGA_LED29	FPGA_LED16	
AH9	FPGA_LED14	FPGA_LED17	
AH8	FPGA_LED22	FPGA_LED18	
AD9	FPGA_LED19	FPGA_LED19	
AD8	FPGA_LED20	FPGA_LED20	
AD10	FPGA_LED21	FPGA_LED21	
AE10	FPGA_LED16	FPGA_LED22	
AE8	FPGA_LED17	FPGA_LED23	
AF8	FPGA_LED18	FPGA_LED24	
AF9	FPGA_LED15	FPGA_LED25	
AG9	FPGA_LED23	FPGA_LED26	
AJ10	FPGA_LED28	FPGA_LED27	
AF10	FPGA_LED24	FPGA_LED28	
AG10	FPGA_LED25	FPGA_LED29	
AD13			
AG11	IOAG11_SFP0_RS0_1V8		
AH11	IOAH11_SFP0_RS1_1V8		
AJ11	IOAJ11_SFP0_TXDIS_1V8		
AG12	IOAG12_SFP1_RS0_1V8		
AH12	IOAH12_SFP1_RS1_1V8		
AD11	IOAD11_SFP1_TXDIS_1V8		
AE11	SFP0_FAULT_AE11_1V8		
AE12	SFP0_LOS_AE12_1V8		
AF12	SFP0_EMPTY_AF12		
AH13	SFP1_FAULT_AH13_1V8		
AJ13	SFP1_LOS_AJ13_1V8		
AE13	SFP1_EMPTY_AE13_1V8		
AF13			
AK13	PDDR3_VTT_EN1V8		
AL13	PDDR4_VTT1_EN1V8		
AK12	PDDR4_VTT2_EN1V8		
AL12			
AM12			
AN12			
AM11			
AN11			
AN13			
AP13			
AK11			
AP11			
AP10			

IO_L24P_T3U_N10_64_AK8	
IO_L24N_T3U_N11_64_AL8	
IO_T3U_N12_64_AM9	
IO_L23P_T3U_N8_64_AJ9	
IO_L23N_T3U_N9_64_AJ8	
IO_L22P_T3U_N6_DBC_AD0P_64_AN8	
IO_L22N_T3U_N7_DBC_AD0N_64_AP8	
IO_L21P_T3L_N4_AD8P_64_AK10	
IO_L21N_T3L_N5_AD8N_64_AL9	
IO_L20P_T3L_N2_AD1P_64_AN9	
IO_L20N_T3L_N3_AD1N_64_AP9	
IO_L19P_T3L_N0_DBC_AD9P_64_AL10	
IO_L19N_T3L_N1_DBC_AD9N_64_AM10	
IO_L18P_T2U_N10_AD2P_64_AH9	
IO_L18N_T2U_N11_AD2N_64_AH8	
IO_L17P_T2U_N8_AD10P_64_AD9	
IO_L17N_T2U_N9_AD10N_64_AD8	
IO_L16P_T2U_N6_QBC_AD3P_64_AD10	
IO_L16N_T2U_N7_QBC_AD3N_64_AE10	
IO_L15P_T2L_N4_AD11P_64_AE8	
IO_L15N_T2L_N5_AD11N_64_AF8	
IO_L14P_T2L_N2_GC_64_AF9	
IO_L14N_T2L_N3_GC_64_AG9	
IO_T2U_N12_64_AJ10	
IO_L13P_T2L_N0_GC_QBC_64_AF10	
IO_L13N_T2L_N1_GC_QBC_64_AG10	
VREF_64_AD13	
IO_L12P_T1U_N10_GC_64_AG11	
IO_L12N_T1U_N11_GC_64_AH11	
IO_T1U_N12_64_AJ11	
IO_L11P_T1U_N8_GC_64_AG12	
IO_L11N_T1U_N9_GC_64_AH12	
IO_L10P_T1U_N6_QBC_AD4P_64_AD11	
IO_L10N_T1U_N7_QBC_AD4N_64_AE11	
IO_L9P_T1L_N4_AD12P_64_AE12	
IO_L9N_T1L_N5_AD12N_64_AF12	
IO_L8P_T1L_N2_AD5P_64_AH13	
IO_L8N_T1L_N3_AD5N_64_AJ13	
IO_L7P_T1L_N0_QBC_AD13P_64_AE13	
IO_L7N_T1L_N1_QBC_AD13N_64_AF13	
IO_L6P_T0U_N10_AD6P_64_AK13	
IO_L6N_T0U_N11_AD6N_64_AL13	
IO_L5P_T0U_N8_AD14P_64_AK12	
IO_L5N_T0U_N9_AD14N_64_AL12	
IO_L4P_T0U_N6_DBC_AD7P_64_AM12	
IO_L4N_T0U_N7_DBC_AD7N_64_AN12	
IO_L3P_T0L_N4_AD15P_64_AM11	
IO_L3N_T0L_N5_AD15N_64_AN11	
IO_L2P_T0L_N2_64_AN13	
IO_L2N_T0L_N3_64_AP13	
IO_T0U_N12_64_AK11	
IO_L1P_T0L_N0_DBC_64_AP11	
IO_L1N_T0L_N1_DBC_64_AP10	

P1V8_FPGA

AF11	VCCO_64_AF11
AG8	VCCO_64_AG8
AJ12	VCCO_64_AJ12
AK9	VCCO_64_AK9
AM13	VCCO_64_AM13
AN10	VCCO_64_AN10

XCKU040-2FFVA1156I
FFVA1156_35MM_35MM_1MM

P1V8_FPGA

C910 0.1UF 16V

U89
SN74AVC8T245RHLR

R852 1.0K

	VCCA	VCCB_24	24		
1	DIR	VCCB_23	23		
IOAG11_SFP0_RS0_1V8	3	A1	B1	21	IOAG11_SFP0_RS0 P50
IOAH11_SFP0_RS1_1V8	4	A2	B2	20	IOAH11_SFP0_RS1 P50
IOAJ11_SFP0_TXDIS_1V8	5	A3	B3	19	IOAJ11_SFP0_TXDIS P50
IOAG12_SFP1_RS0_1V8	6	A4 DIR=1	B4	18	IOAG12_SFP1_RS0 P50
IOAH12_SFP1_RS1_1V8	7	A5 A=>B	B5	17	IOAH12_SFP1_RS1 P50
IOAD11_SFP1_TXDIS_1V8	8	A6	B6	16	IOAD11_SFP1_TXDIS P50
R804 10K	9	A7	B7	15	
R803 10K	10	A8	B8	14	
R805 10K	22	OE	GND	13	
	25	EP	GND	12	
			GND	11	

10GE CONTROLS

PVQFN-24_5_65MMx3_65MM_EP

P3V3_SYS

C911 0.1UF 16V

P1V8_FPGA

C912 0.1UF 16V

U90
SN74AVC8T245RHLR

R853 1.0K

	VCCA	VCCB_24	24		
1	DIR	VCCB_23	23		
SFP0_FAULT_AE11_1V8	3	A1	B1	21	SFP0_FAULT_AE11 P50
SFP0_LOS_AE12_1V8	4	A2	B2	20	SFP0_LOS_AE12 P50
SFP0_EMPTY_AF12	5	A3	B3	19	**SFP0_EMPTY_AF12** P50
SFP1_FAULT_AH13_1V8	6	A4 DIR=1	B4	18	SFP1_FAULT_AH13 P50
SFP1_LOS_AJ13_1V8	7	A5 A=>B	B5	17	SFP1_LOS_AJ13 P50
SFP1_EMPTY_AE13_1V8	8	A6	B6	16	SFP1_EMPTY_AE13 P50
	9	A7	B7	15	R854 10K
	10	A8	B8	14	R855 10K
R806 10K	22	OE	GND	13	
	25	EP	GND	12	
			GND	11	

SFP STATUS
10GE

PVQFN-24_5_65MMx3_65MM_EP

DNI
SW3
FSMSM
1 2 FPGA_PBSW3
R387 4.70K P1V8_FPGA
C252 1uF 35V

DNI
SW5
FSMSM
1 2 FPGA_PBSW5
R378 4.70K P1V8_FPGA
C244 1uF 35V

DNI
SW4
FSMSM
1 2 FPGA_PBSW4
R379 4.70K P1V8_FPGA
C245 1uF 35V

LAYOUT NOTES:
Place these Diodes in a sequential order according to their reference designators.

DESIGN NOTES (LEDS)
DS892 - DC Input and Output Levels - Table-9
Supported drive strengths of 4,8,12,16mA in HR banks.
20mA ==> 100% Relative Luminous Intensity

Title: **PG27: FPGA'S GPIO - LED/SW**

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U54C

BANK 45 HP **C**

XCKU040FFVA1156

P1V2_DDR

R720 DNI

IO_L24P_T3U_N10_45_AD16	AD16	BANK1_DDR4_WE_B		BANK1_DDR4_WE_B P39,40,41,42
IO_L24N_T3U_N11_45_AD15	AD15	BANK1_DDR4_CKE		BANK1_DDR4_CKE P39,40,41,42
IO_T3U_N12_45_AD14	AD14	IO_AD14		
IO_L23P_T3U_N8_45_AE17	AE17	BANK1_DDR4_A00		BANK1_DDR4_A00 P39,40,41,42
IO_L23N_T3U_N9_45_AF17	AF17	BANK1_DDR4_BA0		BANK1_DDR4_BA0 P39,40,41,42
IO_L22P_T3U_N6_DBC_AD0P_45_AE16	AE16	BANK1_DDR4_CK_T	AC_PU_36	BANK1_DDR4_CK_T P39,40,41,42
IO_L22N_T3U_N7_DBC_AD0N_45_AE15	AE15	BANK1_DDR4_CK_C	AC_PU_36	BANK1_DDR4_CK_C P39,40,41,42
IO_L21P_T3L_N4_AD8P_45_AE18	AE18	BANK1_DDR4_A02		BANK1_DDR4_A02 P39,40,41,42
IO_L21N_T3L_N5_AD8N_45_AF18	AF18	BANK1_DDR4_A08		BANK1_DDR4_A08 P39,40,41,42
IO_L20P_T3L_N2_AD1P_45_AF15	AF15	BANK1_DDR4_A10		BANK1_DDR4_A10 P39,40,41,42
IO_L20N_T3L_N3_AD1N_45_AF14	AF14	BANK1_DDR4_RAS_B		BANK1_DDR4_RAS_B P39,40,41,42
IO_L19P_T3L_N0_DBC_AD9P_45_AD19	AD19	BANK1_DDR4_A11		BANK1_DDR4_A11 P39,40,41,42
IO_L19N_T3L_N1_DBC_AD9N_45_AD18	AD18	BANK1_DDR4_PAR		BANK1_DDR4_PAR P39,40,41,42
IO_L18P_T2U_N10_AD2P_45_AG15	AG15	BANK1_DDR4_BG0		BANK1_DDR4_BG0 P39,40,41,42
IO_L18N_T2U_N11_AD2N_45_AG14	AG14	BANK1_DDR4_CAS_B		BANK1_DDR4_CAS_B P39,40,41,42
IO_L17P_T2U_N8_AD10P_45_AG19	AG19	BANK1_DDR4_A13		BANK1_DDR4_A13 P39,40,41,42
IO_L17N_T2U_N9_AD10N_45_AH19	AH19	BANK1_DDR4_A09		BANK1_DDR4_A09 P39,40,41,42
IO_L16P_T2U_N6_QBC_AD3P_45_AJ15	AJ15	BANK1_DDR4_A03		BANK1_DDR4_A03 P39,40,41,42
IO_L16N_T2U_N7_QBC_AD3N_45_AJ14	AJ14	BANK1_DDR4_A12		BANK1_DDR4_A12 P39,40,41,42
IO_L15P_T2L_N4_AD11P_45_AG17	AG17	BANK1_DDR4_A07		BANK1_DDR4_A07 P39,40,41,42
IO_L15N_T2L_N5_AD11N_45_AG16	AG16	BANK1_DDR4_A04		BANK1_DDR4_A04 P39,40,41,42
IO_L14P_T2L_N2_GC_45_AH16	AH16	BANK1_DDR4_TEN	DDR4_TEN:PD 499	BANK1_DDR4_TEN P39,40,41,42
IO_L14N_T2L_N3_GC_45_AJ16	AJ16	BANK1_DDR4_ALERT_B		BANK1_DDR4_ALERT_B P39,40,41,42
IO_T2U_N12_45_AH14	AH14	BANK1_DDR4_ACT_B		BANK1_DDR4_ACT_B P39,40,41,42
IO_L13P_T2L_N0_GC_QBC_45_AH18	AH18			
IO_L13N_T2L_N1_GC_QBC_45_AH17	AH17	BANK1_DDR4_A01		BANK1_DDR4_A01 P39,40,41,42
IO_L12P_T1U_N10_GC_45_AK17	AK17	CLK1_300MC_P		
IO_L12N_T1U_N11_GC_45_AK16	AK16	CLK1_300MC_N		
IO_T1U_N12_45_AJ19	AJ19			
IO_L11P_T1U_N8_GC_45_AJ18	AJ18	BANK1_DDR4_ODT		BANK1_DDR4_ODT P39,40,41,42
IO_L11N_T1U_N9_GC_45_AK18	AK18	BANK1_DDR4_A06		BANK1_DDR4_A06 P39,40,41,42
IO_L10P_T1U_N6_QBC_AD4P_45_AL18	AL18	BANK1_DDR4_RESET_B	DDR4_RST:PD 4.7K	BANK1_DDR4_RESET_B P39,40,41,42
IO_L10N_T1U_N7_QBC_AD4N_45_AL17	AL17	BANK1_DDR4_A05		BANK1_DDR4_A05 P39,40,41,42
IO_L9P_T1L_N4_AD12P_45_AK15	AK15			
IO_L9N_T1L_N5_AD12N_45_AL15	AL15	BANK1_DDR4_BA1		BANK1_DDR4_BA1 P39,40,41,42
IO_L8P_T1L_N2_AD5P_45_AL19	AL19	BANK1_DDR4_CS_B		BANK1_DDR4_CS_B P39,40,41,42
IO_L8N_T1L_N3_AD5N_45_AM19	AM19			
IO_L7P_T1L_N0_QBC_AD13P_45_AL14	AL14			
IO_L7N_T1L_N1_QBC_AD13N_45_AM14	AM14			
IO_L6P_T0U_N10_AD6P_45_AP16	AP16			
IO_L6N_T0U_N11_AD6N_45_AP15	AP15			
IO_L5P_T0U_N8_AD14P_45_AM16	AM16			
IO_L5N_T0U_N9_AD14N_45_AM15	AM15			
IO_L4P_T0U_N6_DBC_AD7P_45_AN18	AN18			
IO_L4N_T0U_N7_DBC_AD7N_45_AN17	AN17			
IO_L3P_T0L_N4_AD15P_45_AM17	AM17			
IO_L3N_T0L_N5_AD15N_45_AN16	AN16			
IO_L2P_T0L_N2_45_AN19	AN19			
IO_L2N_T0L_N3_45_AP18	AP18			
IO_T0U_N12_VRP_45_AP19	AP19	BANK1_DDR4_VRP_45	R704 240	
IO_L1P_T0L_N0_DBC_45_AN14	AN14	BANK1_DDR4_IO_AP14	R719 DNI	
IO_L1N_T0L_N1_DBC_45_AP14	AP14	BANK1_DDR4_VREF_45	R703 DNI	
VREF_45_AF19	AF19			

R706 100

CLK1_300MC_P P51

CLK1_300MC_N P51

LAYOUT NOTE:

PLACE THE 100 OHM TERMINATION CLOSE TO FPGA'S CLOCK PINS.

P1V2_DDR

AP17	VCCO_45_AP17	
AL16	VCCO_45_AL16	
AK19	VCCO_45_AK19	
AH15	VCCO_45_AH15	
AG18	VCCO_45_AG18	
AE14	VCCO_45_AE14	
AD17	VCCO_45_AD17	

XCKU040-2FFVA1156I
FFVA1156_35MM_35MM_1MM

P1V2_DDR

R701 DNI C702 DNI

R702 DNI C703 DNI

LAYOUT NOTES:
Place these capacitors and resistors for VREF underneath the FPGA via array right next to the the via.

DESIGN NOTES (Internal VREF)
Tying the VREF pin to ground with a 499 to 2.0 k resistor.

P1V2_DDR

C600 0.015UF 16V

BANK1_DDR4_CK_T	R642	36	
BANK1_DDR4_CK_C	R643	36	
BANK1_DDR4_TEN	R605	499	
BANK1_DDR4_RESET_B	R661	4.70K	

PAGE 14

PDDR4_VTT_BANK1

BANK1_DDR4_A00	R636	39.2
BANK1_DDR4_A01	R639	39.2
BANK1_DDR4_A02	R637	39.2
BANK1_DDR4_A03	R606	39.2
BANK1_DDR4_A04	R662	39.2
BANK1_DDR4_A05	R602	39.2
BANK1_DDR4_A06	R660	39.2
BANK1_DDR4_A07	R601	39.2
BANK1_DDR4_A08	R659	39.2
BANK1_DDR4_A09	R638	39.2
BANK1_DDR4_A10	R665	39.2
BANK1_DDR4_A11	R658	39.2
BANK1_DDR4_A12	R608	39.2
BANK1_DDR4_A13	R600	39.2
BANK1_DDR4_WE_B	R666	39.2
BANK1_DDR4_CAS_B	R607	39.2
BANK1_DDR4_RAS_B	R610	39.2
BANK1_DDR4_BA0	R663	39.2
BANK1_DDR4_BA1	R604	39.2
BANK1_DDR4_BG0	R664	39.2
BANK1_DDR4_CKE	R668	39.2
BANK1_DDR4_PAR	R657	39.2
BANK1_DDR4_ACT_B	R667	39.2
BANK1_DDR4_ALERT_B	R603	39.2
BANK1_DDR4_ODT	R669	39.2
BANK1_DDR4_CS_B	R611	39.2

C634 0.10uF 10V SMD-0201

C572 0.10uF 10V SMD-0201

C629 0.10uF 10V SMD-0201

C628 0.10uF 10V SMD-0201

C596 0.10uF 10V SMD-0201

C571 4.7uF 6.3V SMD-0402

C575 4.7uF 6.3V SMD-0402

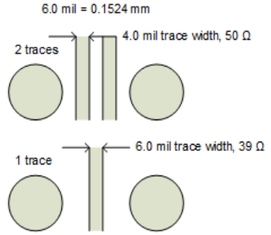
C597 4.7uF 6.3V SMD-0402

UG583 - Chapter 2 Memory Interface
For reference, this particular stackup results in an inner signal layer propagation time of 169.5 ps/in.

1. Include package delay in routing constraints when determining signal trace lengths, except where noted. Use the midpoint between the minimum and maximum values.
2. UltraScale device breakout specifications assume two signal routes between pads. If routing one signal between pads, traces can be 39 Ohms instead of 50 Ohms
3. The maximum breakout routing length is 0.8 inches when routing two signals between pads, and 1.2 inches when routing one signal between pads. If greater than 1.2 inches is needed in the breakout area, change to 3x spacing in the L1 trace area.

169.5 ps/in:
0.1695 ps ==> 1 mil
1 ps ==> 5.8997 mil
±5 ps ==> ±29 mil

3. PCB must be tuned to offset the difference in propagation times between the faster differential CK lines and the relatively slower single-ended address lines.



Title	PG28: FPGA DDR4#1 ADDRESS	
Size: Custom	Document Number: SCH-000012-00	Rev: 04.01
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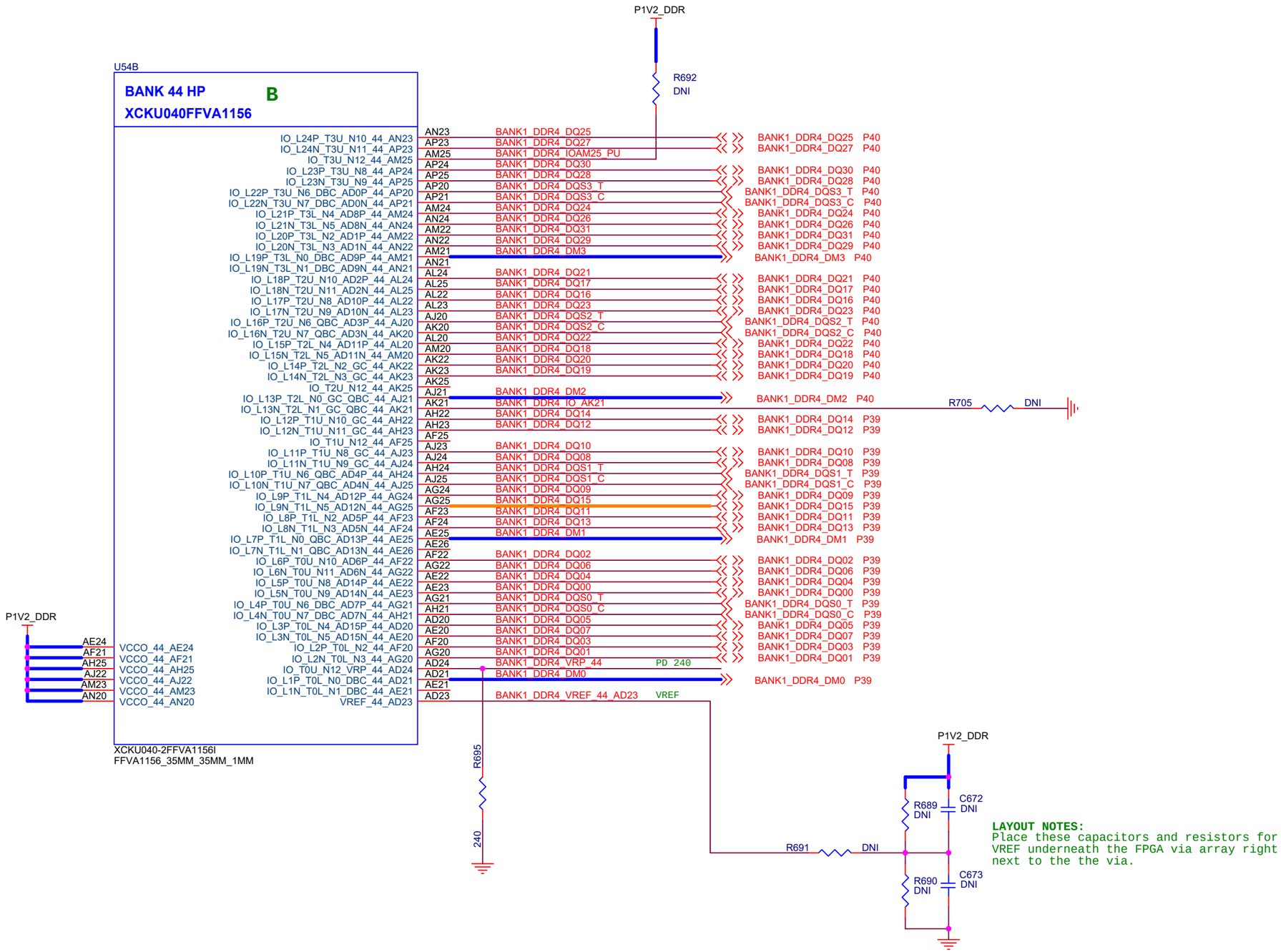

Title: PG29: FPGA DDR4#1 DQ[31:0]

Size: Custom | Document Number: SCH-000012-00 | Rev: 04.01

Date: Tuesday, June 19, 2018 | Sheet 29 of 55

U54D

BANK 46 HP **D**

XCKU040FFVA1156

IO_L24P_T3U_N10_46_AL34	AL34	BANK1_DDR4_DQ62		BANK1_DDR4_DQ62	P42
IO_L24N_T3U_N11_46_AM34	AM34	BANK1_DDR4_DQ58		BANK1_DDR4_DQ58	P42
IO_T3U_N12_46_AK33	AK33	BANK1_DDR4_IO_AK33	PU_DNI		
IO_L23P_T3U_N8_46_AM32	AM32	BANK1_DDR4_DQ60		BANK1_DDR4_DQ60	P42
IO_L23N_T3U_N9_46_AN32	AN32	BANK1_DDR4_DQ63		BANK1_DDR4_DQ63	P42
IO_L22P_T3U_N6_DBC_AD0P_46_AN34	AN34	BANK1_DDR4_DQS7_T		BANK1_DDR4_DQS7_T	P42
IO_L22N_T3U_N7_DBC_AD0N_46_AP34	AP34	BANK1_DDR4_DQS7_C		BANK1_DDR4_DQS7_C	P42
IO_L21P_T3L_N4_AD8P_46_AN31	AN31	BANK1_DDR4_DQ61		BANK1_DDR4_DQ61	P42
IO_L21N_T3L_N5_AD8N_46_AP31	AP31	BANK1_DDR4_DQ59		BANK1_DDR4_DQ59	P42
IO_L20P_T3L_N2_AD1P_46_AN33	AN33	BANK1_DDR4_DQ56		BANK1_DDR4_DQ56	P42
IO_L20N_T3L_N3_AD1N_46_AP33	AP33	BANK1_DDR4_DQ57		BANK1_DDR4_DQ57	P42
IO_L19P_T3L_N0_DBC_AD9P_46_AL32	AL32	BANK1_DDR4_DM7		BANK1_DDR4_DM7	P42
IO_L19N_T3L_N1_DBC_AD9N_46_AL33	AL33				
IO_L18P_T2U_N10_AD2P_46_AH34	AH34	BANK1_DDR4_DQ54		BANK1_DDR4_DQ54	P42
IO_L18N_T2U_N11_AD2N_46_AJ34	AJ34	BANK1_DDR4_DQ50		BANK1_DDR4_DQ50	P42
IO_L17P_T2U_N8_AD10P_46_AH31	AH31	BANK1_DDR4_DQ48		BANK1_DDR4_DQ48	P42
IO_L17N_T2U_N9_AD10N_46_AH32	AH32	BANK1_DDR4_DQ49		BANK1_DDR4_DQ49	P42
IO_L16P_T2U_N6_QBC_AD3P_46_AH33	AH33	BANK1_DDR4_DQS6_T		BANK1_DDR4_DQS6_T	P42
IO_L16N_T2U_N7_QBC_AD3N_46_AJ33	AJ33	BANK1_DDR4_DQS6_C		BANK1_DDR4_DQS6_C	P42
IO_L15P_T2L_N4_AD11P_46_AJ30	AJ30	BANK1_DDR4_DQ53		BANK1_DDR4_DQ53	P42
IO_L15N_T2L_N5_AD11N_46_AJ31	AJ31	BANK1_DDR4_DQ52		BANK1_DDR4_DQ52	P42
IO_L14P_T2L_N2_GC_46_AK31	AK31	BANK1_DDR4_DQ51		BANK1_DDR4_DQ51	P42
IO_L14N_T2L_N3_GC_46_AK32	AK32	BANK1_DDR4_DQ55		BANK1_DDR4_DQ55	P42
IO_T2U_N12_46_AH29	AH29				
IO_L13P_T2L_N0_GC_QBC_46_AJ29	AJ29	BANK1_DDR4_DM6		BANK1_DDR4_DM6	P42
IO_L13N_T2L_N1_GC_QBC_46_AK30	AK30				
IO_L12P_T1U_N10_GC_46_AL30	AL30	BANK1_DDR4_DQ40		BANK1_DDR4_DQ40	P41
IO_L12N_T1U_N11_GC_46_AM30	AM30	BANK1_DDR4_DQ42		BANK1_DDR4_DQ42	P41
IO_T1U_N12_46_AM31	AM31				
IO_L11P_T1U_N8_GC_46_AL29	AL29	BANK1_DDR4_DQ44		BANK1_DDR4_DQ44	P41
IO_L11N_T1U_N9_GC_46_AM29	AM29	BANK1_DDR4_DQ46		BANK1_DDR4_DQ46	P41
IO_L10P_T1U_N6_QBC_AD4P_46_AN29	AN29	BANK1_DDR4_DQS5_T		BANK1_DDR4_DQS5_T	P41
IO_L10N_T1U_N7_QBC_AD4N_46_AP30	AP30	BANK1_DDR4_DQS5_C		BANK1_DDR4_DQS5_C	P41
IO_L9P_T1L_N4_AD12P_46_AN27	AN27	BANK1_DDR4_DQ47		BANK1_DDR4_DQ47	P41
IO_L9N_T1L_N5_AD12N_46_AN28	AN28	BANK1_DDR4_DQ43		BANK1_DDR4_DQ43	P41
IO_L8P_T1L_N2_AD5P_46_AP28	AP28	BANK1_DDR4_DQ45		BANK1_DDR4_DQ45	P41
IO_L8N_T1L_N3_AD5N_46_AP29	AP29	BANK1_DDR4_DQ41		BANK1_DDR4_DQ41	P41
IO_L7P_T1L_N0_QBC_AD13P_46_AN26	AN26	BANK1_DDR4_DM5		BANK1_DDR4_DM5	P41
IO_L7N_T1L_N1_QBC_AD13N_46_AP26	AP26				
IO_L6P_T0U_N10_AD6P_46_AJ28	AJ28	BANK1_DDR4_DQ36		BANK1_DDR4_DQ36	P41
IO_L6N_T0U_N11_AD6N_46_AK28	AK28	BANK1_DDR4_DQ34		BANK1_DDR4_DQ34	P41
IO_L5P_T0U_N8_AD14P_46_AH27	AH27	BANK1_DDR4_DQ37		BANK1_DDR4_DQ37	P41
IO_L5N_T0U_N9_AD14N_46_AH28	AH28	BANK1_DDR4_DQ32		BANK1_DDR4_DQ32	P41
IO_L4P_T0U_N6_DBC_AD7P_46_AL27	AL27	BANK1_DDR4_DQS4_T		BANK1_DDR4_DQS4_T	P41
IO_L4N_T0U_N7_DBC_AD7N_46_AL28	AL28	BANK1_DDR4_DQS4_C		BANK1_DDR4_DQS4_C	P41
IO_L3P_T0L_N4_AD15P_46_AK26	AK26	BANK1_DDR4_DQ33		BANK1_DDR4_DQ33	P41
IO_L3N_T0L_N5_AD15N_46_AK27	AK27	BANK1_DDR4_DQ38		BANK1_DDR4_DQ38	P41
IO_L2P_T0L_N2_46_AM26	AM26	BANK1_DDR4_DQ39		BANK1_DDR4_DQ39	P41
IO_L2N_T0L_N3_46_AM27	AM27	BANK1_DDR4_DQ35		BANK1_DDR4_DQ35	P41
IO_T0U_N12_VRP_46_AG26	AG26	BANK1_DDR4_VRP_46	PD 240		
IO_L1P_T0L_N0_DBC_46_AH26	AH26	BANK1_DDR4_DM4		BANK1_DDR4_DM4	P41
IO_L1N_T0L_N1_DBC_46_AJ26	AJ26	BANK1_DDR4_IO_AJ26	PD_DNI		
VREF_46_AG27	AG27	BANK1_DDR4_VREF_46	VREF		

AG28	VCCO_46_AG28
AJ32	VCCO_46_AJ32
AK29	VCCO_46_AK29
AL26	VCCO_46_AL26
AM33	VCCO_46_AM33
AN30	VCCO_46_AN30
AP27	VCCO_46_AP27

XCKU040-2FFVA1156I

FFVA1156_35MM_35MM_1MM

P1V2_DDR

DNI R671

P1V2_DDR

DNI R694

VRP_46

R693 240

R645 DNI

P1V2_DDR

R644 DNI C605 DNI

R646 DNI C607 DNI

LAYOUT NOTES:

Place these capacitors and resistors for VREF underneath the FPGA via array right next to the the via.

Title: **PG30: FPGA DDR4#1 DQ[63:32]**

Size: Custom | Document Number: **SCH-000012-00** | Rev: 04.01

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U54I

BANK 66 HP

XCKU040FFVA1156

IO_L24P_T3U_N10_66_D13	D13	BANK2_DDR4_WE_B		BANK2_DDR4_WE_B P43,44,45,46
IO_L24N_T3U_N11_66_C13	C13	BANK2_DDR4_CKE		BANK2_DDR4_CKE P43,44,45,46
IO_T3U_N12_66_E12	E12	BANK2_DDR4_IO_H22		
IO_L23P_T3U_N8_66_A13	A13	BANK2_DDR4_A00		BANK2_DDR4_A00 P43,44,45,46
IO_L23N_T3U_N9_66_A12	A12	BANK2_DDR4_BA0		BANK2_DDR4_BA0 P43,44,45,46
IO_L22P_T3U_N6_DBC_AD0P_66_F13	F13	BANK2_DDR4_CK_T	AC PU 36	BANK2_DDR4_CK_T P43,44,45,46
IO_L22N_T3U_N7_DBC_AD0N_66_E13	E13	BANK2_DDR4_CK_C	AC PU 36	BANK2_DDR4_CK_C P43,44,45,46
IO_L21P_T3L_N4_AD8P_66_C11	C11	BANK2_DDR4_A02		BANK2_DDR4_A02 P43,44,45,46
IO_L21N_T3L_N5_AD8N_66_B11	B11	BANK2_DDR4_A08		BANK2_DDR4_A08 P43,44,45,46
IO_L20P_T3L_N2_AD1P_66_C12	C12	BANK2_DDR4_A10		BANK2_DDR4_A10 P43,44,45,46
IO_L20N_T3L_N3_AD1N_66_B12	B12	BANK2_DDR4_RAS_B		BANK2_DDR4_RAS_B P43,44,45,46
IO_L19P_T3L_N0_DBC_AD9P_66_E11	E11	BANK2_DDR4_A11		BANK2_DDR4_A11 P43,44,45,46
IO_L19N_T3L_N1_DBC_AD9N_66_D11	D11	BANK2_DDR4_PAR		BANK2_DDR4_PAR P43,44,45,46
IO_L18P_T2U_N10_AD2P_66_J13	J13	BANK2_DDR4_BG0		BANK2_DDR4_BG0 P43,44,45,46
IO_L18N_T2U_N11_AD2N_66_H13	H13	BANK2_DDR4_CAS_B		BANK2_DDR4_CAS_B P43,44,45,46
IO_L17P_T2U_N8_AD10P_66_L12	L12	BANK2_DDR4_A13		BANK2_DDR4_A13 P43,44,45,46
IO_L17N_T2U_N9_AD10N_66_K12	K12	BANK2_DDR4_A09		BANK2_DDR4_A09 P43,44,45,46
IO_L16P_T2U_N6_QBC_AD3P_66_L13	L13	BANK2_DDR4_A03		BANK2_DDR4_A03 P43,44,45,46
IO_L16N_T2U_N7_QBC_AD3N_66_K13	K13	BANK2_DDR4_A12		BANK2_DDR4_A12 P43,44,45,46
IO_L15P_T2L_N4_AD11P_66_K11	K11	BANK2_DDR4_A07		BANK2_DDR4_A07 P43,44,45,46
IO_L15N_T2L_N5_AD11N_66_J11	J11	BANK2_DDR4_A04		BANK2_DDR4_A04 P43,44,45,46
IO_L14P_T2L_N2_GC_66_H12	H12	BANK2_DDR4_TEN	DDR4_TEN:PD 499	BANK2_DDR4_TEN P43,44,45,46
IO_L14N_T2L_N3_GC_66_G12	G12	BANK2_DDR4_ALERT_B		BANK2_DDR4_ALERT_B P43,44,45,46
IO_T2U_N12_66_F12	F12	BANK2_DDR4_ACT_B		BANK2_DDR4_ACT_B P43,44,45,46
IO_L13P_T2L_N0_GC_QBC_66_H11	H11			
IO_L13N_T2L_N1_GC_QBC_66_G11	G11	BANK2_DDR4_A01		BANK2_DDR4_A01 P43,44,45,46
IO_L12P_T1U_N10_GC_66_G10	G10	CLK2_300MC_P		
IO_L12N_T1U_N11_GC_66_F10	F10	CLK2_300MC_N		
IO_T1U_N12_66_L9	L9			
IO_L11P_T1U_N8_GC_66_G9	G9	BANK2_DDR4_ODT		BANK2_DDR4_ODT P43,44,45,46
IO_L11N_T1U_N9_GC_66_F9	F9	BANK2_DDR4_A06		BANK2_DDR4_A06 P43,44,45,46
IO_L10P_T1U_N6_QBC_AD4P_66_K10	K10	BANK2_DDR4_RESET_B	DDR4_RST:PD 4.7K	BANK2_DDR4_RESET_B P43,44,45,46
IO_L10N_T1U_N7_QBC_AD4N_66_J10	J10	BANK2_DDR4_A05		BANK2_DDR4_A05 P43,44,45,46
IO_L9P_T1L_N4_AD12P_66_J8	J8			
IO_L9N_T1L_N5_AD12N_66_H8	H8	BANK2_DDR4_BA1		BANK2_DDR4_BA1 P43,44,45,46
IO_L8P_T1L_N2_AD5P_66_J9	J9	BANK2_DDR4_CS_B		BANK2_DDR4_CS_B P43,44,45,46
IO_L8N_T1L_N3_AD5N_66_H9	H9			
IO_L7P_T1L_N0_QBC_AD13P_66_L8	L8			
IO_L7N_T1L_N1_QBC_AD13N_66_K8	K8			
IO_L6P_T0U_N10_AD6P_66_E10	E10			
IO_L6N_T0U_N11_AD6N_66_D10	D10			
IO_L5P_T0U_N8_AD14P_66_D9	D9			
IO_L5N_T0U_N9_AD14N_66_C9	C9			
IO_L4P_T0U_N6_DBC_AD7P_66_B10	B10			
IO_L4N_T0U_N7_DBC_AD7N_66_A10	A10			
IO_L3P_T0L_N4_AD15P_66_D8	D8			
IO_L3N_T0L_N5_AD15N_66_C8	C8			
IO_L2P_T0L_N2_66_B9	B9			
IO_L2N_T0L_N3_66_A9	A9			
IO_T0U_N12_VRP_66_A8	A8	BANK2_DDR4_VRP_67		
IO_L1P_T0L_N0_DBC_66_F8	F8			
IO_L1N_T0L_N1_DBC_66_E8	E8	BANK2_DDR4_IO_B14		
VREF_66_L10	L10	BANK2_DDR4_VREF_67		

VCCO_66_B13	B13	P1V2_DDR
VCCO_66_C10	C10	P1V2_DDR
VCCO_66_F11	F11	P1V2_DDR
VCCO_66_G8	G8	P1V2_DDR
VCCO_66_J12	J12	P1V2_DDR
VCCO_66_K9	K9	P1V2_DDR

XCKU040-2FFVA1156I

FFVA1156_35MM_35MM_1MM

P1V2_DDR

R725 DNI

R724 100

CLK2_300MC_P P51

CLK2_300MC_N P51

LAYOUT NOTE:
PLACE THE 100 OHM TERMINATION CLOSE TO FPGA'S CLOCK PINS.

DESIGN NOTES:
Internal VREF ???

BANK2_DDR4_VRP_67 — R740 240

BANK2_DDR4_IO_B14 — R739 DNI

BANK2_DDR4_VREF_67 — R741 DNI

P1V2_DDR

R743 DNI — C824 DNI

R742 DNI — C823 DNI

LAYOUT NOTES:
Place these capacitors and resistors for VREF underneath the FPGA via array right next to the the via.

P1V2_DDR

C616 0.015UF 16V

BANK2_DDR4_CK_T — R648 36

BANK2_DDR4_CK_C — R647 36

BANK2_DDR4_TEN — R681 499

BANK2_DDR4_RESET_B — R632 4.70K

PDDR4_VTT_BANK2

BANK2_DDR4_A00	R654	39.2
BANK2_DDR4_A01	R655	39.2
BANK2_DDR4_A02	R653	39.2
BANK2_DDR4_A03	R682	39.2
BANK2_DDR4_A04	R631	39.2
BANK2_DDR4_A05	R684	39.2
BANK2_DDR4_A06	R633	39.2
BANK2_DDR4_A07	R686	39.2
BANK2_DDR4_A08	R634	39.2
BANK2_DDR4_A09	R656	39.2
BANK2_DDR4_A10	R629	39.2
BANK2_DDR4_A11	R651	39.2
BANK2_DDR4_A12	R675	39.2
BANK2_DDR4_A13	R685	39.2
BANK2_DDR4_WE_B	R626	39.2
BANK2_DDR4_CAS_B	R678	39.2
BANK2_DDR4_RAS_B	R676	39.2
BANK2_DDR4_BA0	R630	39.2
BANK2_DDR4_BA1	R679	39.2
BANK2_DDR4_BG0	R627	39.2
BANK2_DDR4_CKE	R624	39.2
BANK2_DDR4_PAR	R652	39.2
BANK2_DDR4_ACT_B	R625	39.2
BANK2_DDR4_ALERT_B	R683	39.2
BANK2_DDR4_ODT	R623	39.2
BANK2_DDR4_CS_B	R674	39.2

C584 0.10uF 10V SMD-0201

C619 0.10uF 10V SMD-0201

C659 0.10uF 10V SMD-0201

C590 0.10uF 10V SMD-0201

C587 0.10uF 10V SMD-0201

C591 4.7uF 6.3V SMD-0402

C620 4.7uF 6.3V SMD-0402

C621 4.7uF 6.3V SMD-0402

Title: **PG31: FPGA DDR4#2 ADDRESS**

Size: Custom | Document Number: **SCH-000012-00** | Rev: 04.01

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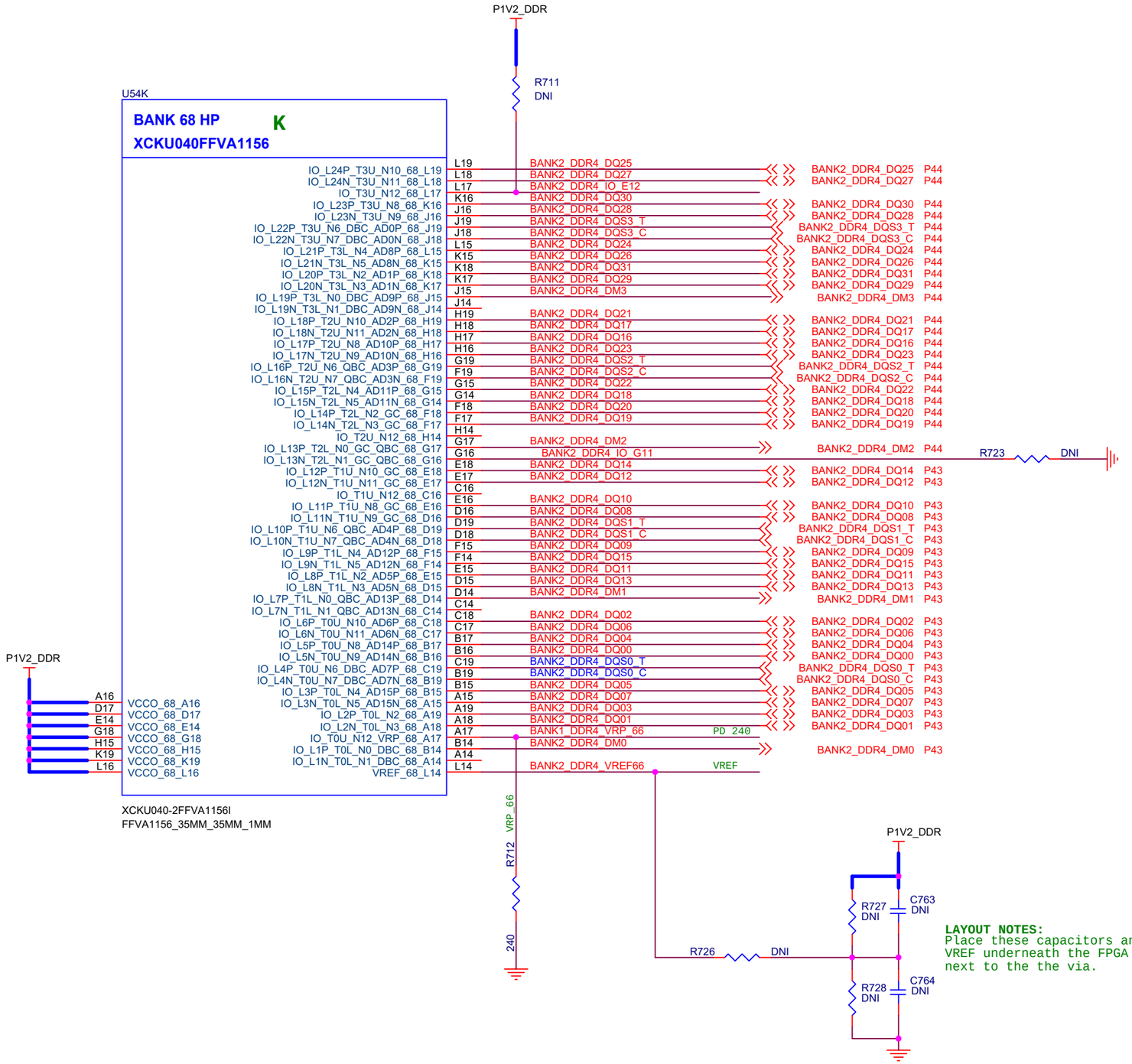

Title: PG32: FPGA DDR4#2 DQ[31:0]

Size	Document Number	Rev
Custom	SCH-000012-00	04.01

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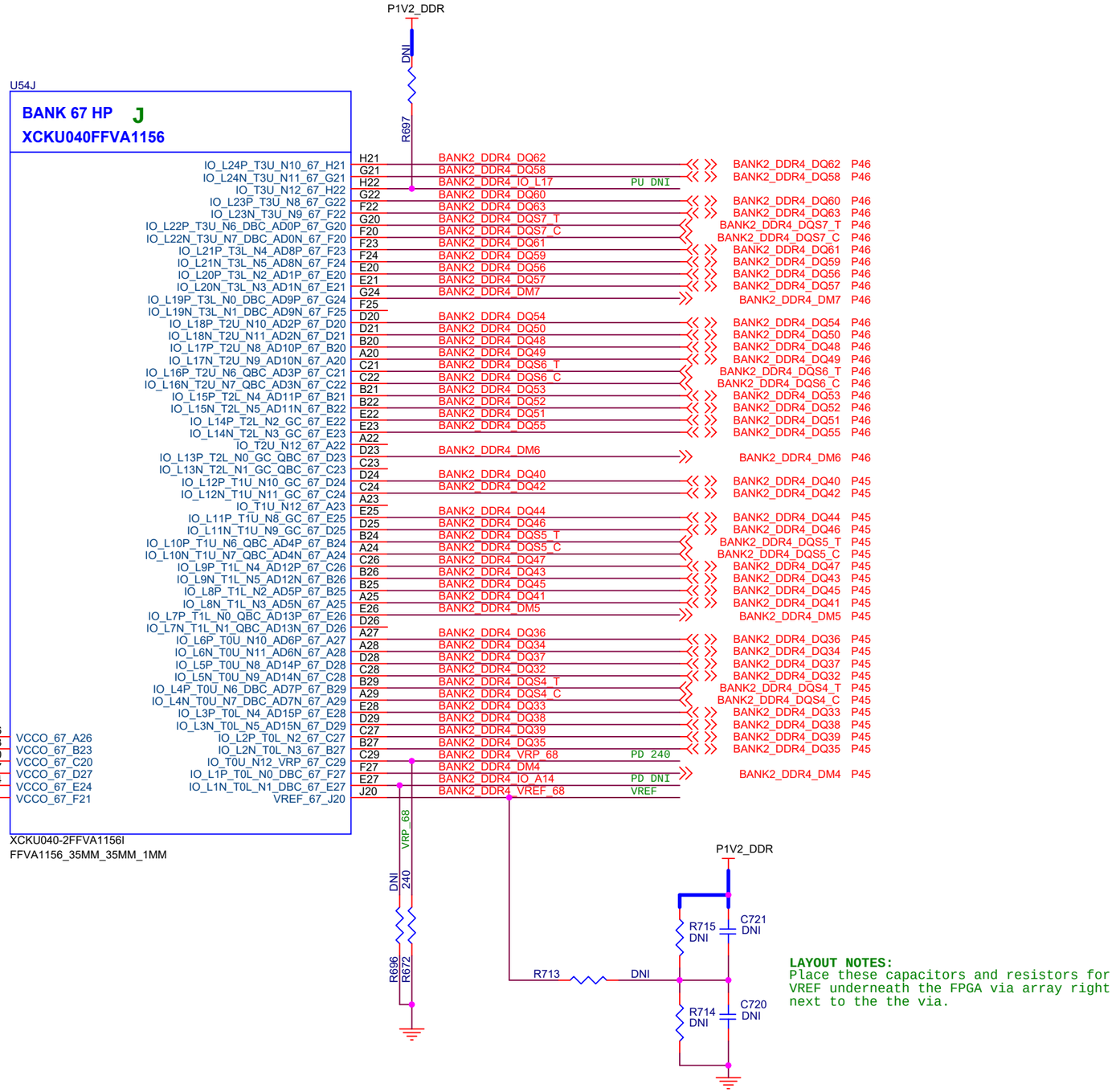


Title: PG33: FPGA DDR4#2 DQ[63:32]

Size: Custom | Document Number: SCH-000012-00 | Rev: 04.01

Date: Tuesday, June 19, 2018 | Sheet 33 of 55

U54E

BANK 47 HP **E**

XCKU040FFVA1156

IO_L24P_T3U_N10_47_V26	V26	
IO_L24N_T3U_N11_47_W26	W26	
IO_T3U_N12_47_U29	U29	EC1_LED1 P47
IO_L23P_T3U_N8_47_V29	V29	EC1_LED2 P47
IO_L23N_T3U_N9_47_W29	W29	EC2_LED1 P48
IO_L22P_T3U_N6_DBC_AD0P_47_U26	U26	EC2_LED2 P48
IO_L22N_T3U_N7_DBC_AD0N_47_U27	U27	EC3_LED1 P49
IO_L21P_T3L_N4_AD8P_47_W28	W28	EC3_LED2 P49
IO_L21N_T3L_N5_AD8N_47_Y28	Y28	
IO_L20P_T3L_N2_AD1P_47_U24	U24	R878 0 FPGA_IO_U24 P55
IO_L20N_T3L_N3_AD1N_47_U25	U25	
IO_L19P_T3L_N0_DBC_AD9P_47_V27	V27	R879 0 FPGA_IO_V27 P55
IO_L19N_T3L_N1_DBC_AD9N_47_V28	V28	
IO_L18P_T2U_N10_AD2P_47_V21	V21	
IO_L18N_T2U_N11_AD2N_47_W21	W21	
IO_L17P_T2U_N8_AD10P_47_T22	T22	FPGA_UART_SIN P52
IO_L17N_T2U_N9_AD10N_47_T23	T23	
IO_L16P_T2U_N6_QBC_AD3P_47_V22	V22	FPGA_UART_SOUT P52
IO_L16N_T2U_N7_QBC_AD3N_47_V23	V23	
IO_L15P_T2L_N4_AD11P_47_U21	U21	
IO_L15N_T2L_N5_AD11N_47_U22	U22	
IO_L14P_T2L_N2_GC_47_W25	W25	LS1021A_QSPI_B_CS0 P18
IO_L14N_T2L_N3_GC_47_Y25	Y25	
IO_T2U_N12_47_Y21	Y21	
IO_L13P_T2L_N0_GC_QBC_47_W23	W23	LS1021A_QSPI_B_CLK P18
IO_L13N_T2L_N1_GC_QBC_47_W24	W24	LS1021A_QSPI_B_IO0 P18
IO_L12P_T1U_N10_GC_47_AA24	AA24	LS1021A_QSPI_B_IO1 P18
IO_L12N_T1U_N11_GC_47_AA25	AA25	LS1021A_QSPI_B_IO2 P18
IO_T1U_N12_47_Y22	Y22	LS1021A_QSPI_B_IO3 P18
IO_L11P_T1U_N8_GC_47_Y23	Y23	CLK5R_100M_P P51
IO_L11N_T1U_N9_GC_47_AA23	AA23	CLK5R_100M_N P51
IO_L10P_T1U_N6_QBC_AD4P_47_AB21	AB21	
IO_L10N_T1U_N7_QBC_AD4N_47_AC21	AC21	
IO_L9P_T1L_N4_AD12P_47_AA20	AA20	**LS1021A_RSTREQ_RB P20**
IO_L9N_T1L_N5_AD12N_47_AB20	AB20	LS1021A_SLEEP P20
IO_L8P_T1L_N2_AD5P_47_AC22	AC22	
IO_L8N_T1L_N3_AD5N_47_AC23	AC23	
IO_L7P_T1L_N0_QBC_AD13P_47_AA22	AA22	
IO_L7N_T1L_N1_QBC_AD13N_47_AB22	AB22	
IO_L6P_T0U_N10_AD6P_47_AB25	AB25	
IO_L6N_T0U_N11_AD6N_47_AB26	AB26	
IO_L5P_T0U_N8_AD14P_47_AA27	AA27	
IO_L5N_T0U_N9_AD14N_47_AB27	AB27	
IO_L4P_T0U_N6_DBC_AD7P_47_AC26	AC26	
IO_L4N_T0U_N7_DBC_AD7N_47_AC27	AC27	LS1021A_IFC_ADDR26 P18
IO_L3P_T0L_N4_AD15P_47_AB24	AB24	LS1021A_IFC_ADDR27 P18
IO_L3N_T0L_N5_AD15N_47_AC24	AC24	
IO_L2P_T0L_N2_47_AD25	AD25	
IO_L2N_T0L_N3_47_AD26	AD26	
IO_T0U_N12_VRP_47_AA28	AA28	
IO_L1P_T0L_N0_DBC_47_Y26	Y26	
IO_L1N_T0L_N1_DBC_47_Y27	Y27	
VREF_47_V24	V24	

P1V8_FPGA

T21	VCCO_47_T21
U28	VCCO_47_U28
V25	VCCO_47_V25
W22	VCCO_47_W22
AA26	VCCO_47_AA26
AB23	VCCO_47_AB23
AC20	VCCO_47_AC20

XCKU040-2FFVA1156I

FFVA1156_35MM_35MM_1MM

U54F

BANK 48 HP **F**

XCKU040FFVA1156

IO_L24P_T3U_N10_48_V31	V31	
IO_L24N_T3U_N11_48_W31	W31	
IO_T3U_N12_48_V32	V32	
IO_L23P_T3U_N8_48_U34	U34	FPGA_LVDS_L23P P55
IO_L23N_T3U_N9_48_V34	V34	FPGA_LVDS_L23N P55
IO_L22P_T3U_N6_DBC_AD0P_48_Y31	Y31	FPGA_LVDS_L22P P55
IO_L22N_T3U_N7_DBC_AD0N_48_Y32	Y32	FPGA_LVDS_L22N P55
IO_L21P_T3L_N4_AD8P_48_V33	V33	FPGA_LVDS_L21P P55
IO_L21N_T3L_N5_AD8N_48_W34	W34	FPGA_LVDS_L21N P55
IO_L20P_T3L_N2_AD1P_48_W30	W30	FPGA_LVDS_L20P P55
IO_L20N_T3L_N3_AD1N_48_Y30	Y30	FPGA_LVDS_L20N P55
IO_L19P_T3L_N0_DBC_AD9P_48_W33	W33	FPGA_LVDS_L19P P55
IO_L19N_T3L_N1_DBC_AD9N_48_Y33	Y33	FPGA_LVDS_L19N P55
IO_L18P_T2U_N10_AD2P_48_AC33	AC33	FPGA_LVDS_L18P P55
IO_L18N_T2U_N11_AD2N_48_AD33	AD33	FPGA_LVDS_L18N P55
IO_L17P_T2U_N8_AD10P_48_AA34	AA34	LS1021A_GPIO1_18 P20
IO_L17N_T2U_N9_AD10N_48_AB34	AB34	LS1021A_GPIO1_16 P20
IO_L16P_T2U_N6_QBC_AD3P_48_AA29	AA29	LS1021A_GPIO1_21 P20
IO_L16N_T2U_N7_QBC_AD3N_48_AB29	AB29	LS1021A_GPIO1_19 P20
IO_L15P_T2L_N4_AD11P_48_AC34	AC34	
IO_L15N_T2L_N5_AD11N_48_AD34	AD34	
IO_L14P_T2L_N2_GC_48_AB30	AB30	1PPS_IN
IO_L14N_T2L_N3_GC_48_AB31	AB31	
IO_T2U_N12_48_AA33	AA33	
IO_L13P_T2L_N0_GC_QBC_48_AA32	AA32	1PPS_OUT1 1PPS_OUT1 P20
IO_L13N_T2L_N1_GC_QBC_48_AB32	AB32	
IO_L12P_T1U_N10_GC_48_AC31	AC31	RTC_32_768M P20
IO_L12N_T1U_N11_GC_48_AC32	AC32	
IO_T1U_N12_48_AE31	AE31	
IO_L11P_T1U_N8_GC_48_AD30	AD30	1PPS_OUT2 1PPS_OUT2 P55
IO_L11N_T1U_N9_GC_48_AD31	AD31	
IO_L10P_T1U_N6_QBC_AD4P_48_AE33	AE33	
IO_L10N_T1U_N7_QBC_AD4N_48_AF34	AF34	
IO_L9P_T1L_N4_AD12P_48_AE32	AE32	FPGA_OPAT_PWRCTL P55
IO_L9N_T1L_N5_AD12N_48_AF32	AF32	
IO_L8P_T1L_N2_AD5P_48_AF33	AF33	
IO_L8N_T1L_N3_AD5N_48_AG34	AG34	
IO_L7P_T1L_N0_QBC_AD13P_48_AG31	AG31	
IO_L7N_T1L_N1_QBC_AD13N_48_AG32	AG32	
IO_L6P_T0U_N10_AD6P_48_AF30	AF30	
IO_L6N_T0U_N11_AD6N_48_AG30	AG30	
IO_L5P_T0U_N8_AD14P_48_AD29	AD29	FPGA1V8_B48_W31 P20
IO_L5N_T0U_N9_AD14N_48_AE30	AE30	FPGA1V8_B48_V32 P20
IO_L4P_T0U_N6_DBC_AD7P_48_AF29	AF29	FPGA_GPIO0 P55
IO_L4N_T0U_N7_DBC_AD7N_48_AG29	AG29	FPGA_GPIO1 P55
IO_L3P_T0L_N4_AD15P_48_AC28	AC28	FPGA_GPIO2 P55
IO_L3N_T0L_N5_AD15N_48_AD28	AD28	FPGA_GPIO3 P55
IO_L2P_T0L_N2_48_AE28	AE28	FPGA_GPIO4 P55
IO_L2N_T0L_N3_48_AF28	AF28	FPGA_GPIO5 P55
IO_T0U_N12_VRP_48_AC29	AC29	FPGA_GPIO6 P55
IO_L1P_T0L_N0_DBC_48_AE27	AE27	FPGA_GPIO7 P55
IO_L1N_T0L_N1_DBC_48_AF27	AF27	FPGA_PBSW2
VREF_48_AA30	AA30	

6 LVDS PAIRS => PAT

=> ARM

P1V8_FPGA

W32	VCCO_48_W32
Y29	VCCO_48_Y29
AB33	VCCO_48_AB33
AC30	VCCO_48_AC30
AD27	VCCO_48_AD27
AE34	VCCO_48_AE34
AF31	VCCO_48_AF31

XCKU040-2FFVA1156I

FFVA1156_35MM_35MM_1MM

DNI
SW2
FSMSM
1 2 FPGA_PBSW2
R361 4.70K P1V8_ARM
C226 1uF 35V

P1V8_FPGA

C546 0.1UF 16V

DNI
J7
87437-0243
1 J7_1PPS_IN
2
87437_02_ST_SMD

DNI
U45
SN74LVC1G07DCKR
IN VCC
OUT
NC GND
SC-70-5

1PPS_IN

P1V8_FPGA

R591 4.70K

CNTR
1PPS_OUT1
FPGA_32K768

LS1021A
IRQ0
RTC

DESIGN NOTES (SN74LVCG07DCKR)
Vih (min) = 1.17V
Vil (max) = 0.63V
Isink(max) = 32mA
32.768 kHz

Title: **PG34: FPGA BOARD-BOARD INTERFACES**

Size: Custom | Document Number: **SCH-000012-00** | Rev: 04.01

Date: Tuesday, June 19, 2018 | Sheet 34 of 55

NOT USED

U54O

GTH B227 - Q-X0Y3 O
XCKU040FFVA1156

X0Y15	MGTHTXP3_227_G4	G4
	MGTHTXN3_227_G3	G3
	MGTHRXP3_227_F2	F2
	MGTHRXN3_227_F1	F1
X0Y14	MGTHTXP2_227_J4	J4
	MGTHTXN2_227_J3	J3
	MGTHRXP2_227_H2	H2
	MGTHRXN2_227_H1	H1
X0Y13	MGTHTXP1_227_L4	L4
	MGTHTXN1_227_L3	L3
	MGTHRXP1_227_K2	K2
	MGTHRXN1_227_K1	K1
X0Y12	MGTHTXP0_227_N4	N4
	MGTHTXN0_227_N3	N3
	MGTHRXP0_227_M2	M2
	MGTHRXN0_227_M1	M1
REFCLK	MGTREFCLK0P_227_P6	P6
	MGTREFCLK0N_227_P5	P5
	MGTREFCLK1P_227_M6	M6
	MGTREFCLK1N_227_M5	M5

XCKU040-2FFVA1156I
FFVA1156_35MM_35MM_1MM

PCIE x2

U54N

GTH B226 - Q-X0Y2 N
XCKU040FFVA1156

Replaced with High Q, Low Loss caps by ATC

X0Y11	MGTHTXP3_226_R4	R4	X0Y2_TX3_P	C886	0.1uF 16V	PCIE_X0Y2_TX3C_P P17	
	MGTHTXN3_226_R3	R3	X0Y2_TX3_N	C885	0.1uF 16V	PCIE_X0Y2_TX3C_N P17	
	MGTHRXP3_226_P2	P2	X0Y2_RX3_P	C294	0.1uF 16V	PCIE_X0Y2_RX3C_P P17	
	MGTHRXN3_226_P1	P1	X0Y2_RX3_N	C293	0.1uF 16V	PCIE_X0Y2_RX3C_N P17	
X0Y10	MGTHTXP2_226_U4	U4	X0Y2_TX2_P	C884	0.1uF 16V	PCIE_X0Y2_TX2C_P P17	
	MGTHTXN2_226_U3	U3	X0Y2_TX2_N	C883	0.1uF 16V	PCIE_X0Y2_TX2C_N P17	
	MGTHRXP2_226_T2	T2	X0Y2_RX2_P	C291	0.1uF 16V	PCIE_X0Y2_RX2C_P P17	
	MGTHRXN2_226_T1	T1	X0Y2_RX2_N	C292	0.1uF 16V	PCIE_X0Y2_RX2C_N P17	
X0Y9	MGTHTXP1_226_W4	W4	X0Y2_TX1_P	C881	0.1uF 16V	PCIE_X0Y2_TX1C_P P17	TO LS1021A SERDES
	MGTHTXN1_226_W3	W3	X0Y2_TX1_N	C882	0.1uF 16V	PCIE_X0Y2_TX1C_N P17	
	MGTHRXP1_226_V2	V2	X0Y2_RX1_P	C290	0.1uF 16V	PCIE_X0Y2_RX1C_P P17	
	MGTHRXN1_226_V1	V1	X0Y2_RX1_N	C289	0.1uF 16V	PCIE_X0Y2_RX1C_N P17	
X0Y8	MGTHTXP0_226_AA4	AA4	X0Y2_TX0_P	C879	0.1uF 16V	PCIE_X0Y2_TX0C_P P17	TO LS1021A SERDES
	MGTHTXN0_226_AA3	AA3	X0Y2_TX0_N	C880	0.1uF 16V	PCIE_X0Y2_TX0C_N P17	
	MGTHRXP0_226_Y2	Y2	X0Y2_RX0_P	C287	0.1uF 16V	PCIE_X0Y2_RX0C_P P17	
	MGTHRXN0_226_Y1	Y1	X0Y2_RX0_N	C288	0.1uF 16V	PCIE_X0Y2_RX0C_N P17	
REFCLK	MGTREFCLK0P_226_V6	V6	X0Y2_MGTREFCLK0_P	C70	0.01uF 16V	CLK0R_100M_P P51	DC COUPLED Fr LVDS driver
	MGTREFCLK0N_226_V5	V5	X0Y2_MGTREFCLK0_N	C71	0.01uF 16V	CLK0R_100M_N P51	
	MGTREFCLK1P_226_T6	T6					
	MGTREFCLK1N_226_T5	T5					

XCKU040-2FFVA1156I
FFVA1156_35MM_35MM_1MM

10GE - CHANNEL A & B

U54L

GTH B224 - Q-X0Y0 L
XCKU040FFVA1156

No need for AC coupled caps: R437-R440 and C442-R448, since SFP+ module's TX/RX signals are ac-coupled.

X0Y3	MGTHTXP3_224_AK6	AK6				CHB_10G_TX3_P P50	
	MGTHTXN3_224_AK5	AK5				CHB_10G_TX3_N P50	
	MGTHRXP3_224_AJ4	AJ4				CHB_10G_RX3_P P50	
	MGTHRXN3_224_AJ3	AJ3				CHB_10G_RX3_N P50	
X0Y2	MGTHTXP2_224_AL4	AL4				CHA_10G_TX2_P P50	
	MGTHTXN2_224_AL3	AL3				CHA_10G_TX2_N P50	
	MGTHRXP2_224_AK2	AK2				CHA_10G_RX2_P P50	
	MGTHRXN2_224_AK1	AK1				CHA_10G_RX2_N P50	
X0Y1	MGTHTXP1_224_AM6	AM6					
	MGTHTXN1_224_AM5	AM5					
	MGTHRXP1_224_AM2	AM2					
	MGTHRXN1_224_AM1	AM1					
X0Y0	MGTHTXP0_224_AN4	AN4	X0Y0_TX0_P	C909	0.01uF 16V	10GE_LPTX0_P	DESIGN NOTES: LOOP BACK TEST
	MGTHTXN0_224_AN3	AN3	X0Y0_TX0_N	C908	0.01uF 16V		
	MGTHRXP0_224_AP2	AP2	X0Y0_RX0_P	C906	0.01uF 16V		
	MGTHRXN0_224_AP1	AP1	X0Y0_RX0_N	C907	0.01uF 16V	10GE_LPTX0_N	
REFCLK	MGTREFCLK0P_224_AF6	AF6				CLK2_156MC_P P51	
	MGTREFCLK0N_224_AF5	AF5				CLK2_156MC_N P51	
	MGTREFCLK1P_224_AD6	AD6	X0Y0_MGTREFCLK1_P	C877	0.01uF 16V	AC COUPLED	
	MGTREFCLK1N_224_AD5	AD5	X0Y0_MGTREFCLK1_N	C878	0.01uF 16V		

XCKU040-2FFVA1156I
FFVA1156_35MM_35MM_1MM

11.3G

U54P

GTH B228 - Q-X0Y4 P
XCKU040FFVA1156

Replaced with High Q, Low Loss caps by ATC

TO PAT MOST CRITICAL

INTENTIONAL DIFF PAIR ORDERING

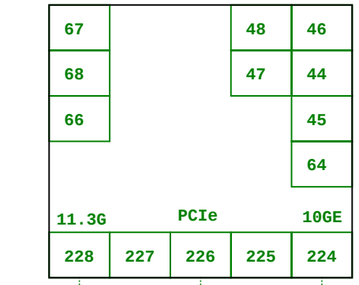
X0Y19	MGTHTXP3_228_B6	B6	X0Y4_TX3_P	C201	0.01uF 16V	MODEM_11G3_TX3_P P55	
	MGTHTXN3_228_B5	B5	X0Y4_TX3_N	C202	0.01uF 16V	MODEM_11G3_TX3_N P55	
	MGTHRXP3_228_A4	A4	X0Y4_RX3_P	C203	0.01uF 16V	MODEM_11G3_RX3_N P55	
	MGTHRXN3_228_A3	A3	X0Y4_RX3_N	C204	0.01uF 16V	MODEM_11G3_RX3_P P55	
X0Y18	MGTHTXP2_228_C4	C4					
	MGTHTXN2_228_C3	C3					
	MGTHRXP2_228_B2	B2					
	MGTHRXN2_228_B1	B1					
X0Y17	MGTHTXP1_228_D6	D6	X0Y4_TX1_P	C895	0.01uF 16V	SMA_TX1_P	
	MGTHTXN1_228_D5	D5	X0Y4_TX1_N	C894	0.01uF 16V	SMA_TX1_N	
	MGTHRXP1_228_D2	D2	X0Y4_RX1_P	C897	0.01uF 16V	SMA_RX1_P	
	MGTHRXN1_228_D1	D1	X0Y4_RX1_N	C896	0.01uF 16V	SMA_RX1_N	
X0Y16	MGTHTXP0_228_F6	F6	X0Y4_TX0_P	C891	0.01uF 16V	MODEM_LPTX0_P	
	MGTHTXN0_228_F5	F5	X0Y4_TX0_N	C889	0.01uF 16V	LOOP BACK TEST	
	MGTHRXP0_228_E4	E4	X0Y4_RX0_P	C892	0.01uF 16V		
	MGTHRXN0_228_E3	E3	X0Y4_RX0_N	C893	0.01uF 16V	MODEM_LPTX0_N	
REFCLK	MGTREFCLK0P_228_K6	K6				CLK1_200MC_P P51	
	MGTREFCLK0N_228_K5	K5				CLK1_200MC_N P51	
	MGTREFCLK1P_228_H6	H6	X0Y4_REFCLK1P	C888	0.01uF 16V	AC COUPLED	
	MGTREFCLK1N_228_H5	H5	X0Y4_REFCLK1N	C887	0.01uF 16V	Fr LVDS driver	

XCKU040-2FFVA1156I
FFVA1156_35MM_35MM_1MM

TEST ONLY

J16 DNI 142-0711-201 — SMA_RX1_P — SMD_SMA_ST
J15 DNI 142-0711-201 — SMA_RX1_N — SMD_SMA_ST
J13 DNI 142-0711-201 — SMA_TX1_P — SMD_SMA_ST
J12 DNI 142-0711-201 — SMA_TX1_N — SMD_SMA_ST
R764 DNI

SIGNAL CHARACTERIZATION



TEST ONLY

U54M

GTH B225 - Q-X0Y1 M
XCKU040FFVA1156

X0Y7	MGTHTXP3_225_AC4	AC4
	MGTHTXN3_225_AC3	AC3
	MGTHRXP3_225_AB2	AB2
	MGTHRXN3_225_AB1	AB1
X0Y6	MGTHTXP2_225_AE4	AE4
	MGTHTXN2_225_AE3	AE3
	MGTHRXP2_225_AD2	AD2
	MGTHRXN2_225_AD1	AD1
X0Y5	MGTHTXP1_225_AG4	AG4
	MGTHTXN1_225_AG3	AG3
	MGTHRXP1_225_AF2	AF2
	MGTHRXN1_225_AF1	AF1
X0Y4	MGTHTXP0_225_AH6	AH6
	MGTHTXN0_225_AH5	AH5
	MGTHRXP0_225_AH2	AH2
	MGTHRXN0_225_AH1	AH1
REFCLK	MGTREFCLK0P_225_AB6	AB6
	MGTREFCLK0N_225_AB5	AB5
	MGTREFCLK1P_225_Y6	Y6
	MGTREFCLK1N_225_Y5	Y5

XCKU040-2FFVA1156I
FFVA1156_35MM_35MM_1MM

GTH INPUT CLOCKS

	Min	Typ	Max	Units	Notes:
V_{IDIFF}	250	-	2000	mV	*Differential p-p input voltage (= single end p-p x 2)*
R_{IN}	-	100	-	Ω	*Differential input resistance*
C_{EXT}		10		nF	*Required external AC coupling capacitor*
$V_{CMOUTAC}$	-	-	800	mV	*Common Mode Output Voltage (AC coupled)*

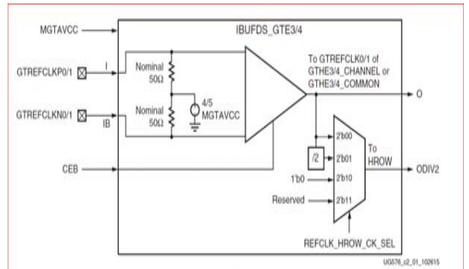


Figure 2-1: **Reference Clock Input Structure**

Title: **PG35: FPGA'S 11.3G/10GE/PCIE INTF**

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U54Q

BANK MGTAVCC Q
XCKU040FFVA1156

GTH ANALOG SUPPLY = 1.00V

MGTAVCC_R_AN6 AN6
MGTAVCC_R_AL6 AL6
MGTAVCC_R_AJ6 AJ6
MGTAVCC_R_AG6 AG6
MGTAVCC_R_AE6 AE6
MGTAVCC_R_AC6 AC6
MGTAVCC_R_W6 W6
MGTAVCC_R_U6 U6
MGTAVCC_R_C6 C6
MGTAVCC_R_E6 E6
MGTAVCC_R_G6 G6
MGTAVCC_R_J6 J6
MGTAVCC_R_N6 N6
MGTAVCC_R_L6 L6

GROUND

MGTAVCC_L_P29 P29
MGTAVCC_L_N31 N31
MGTAVCC_L_J31 J31
MGTAVCC_L_H29 H29
MGTAVCC_L_F30 F30
MGTAVCC_L_E31 E31

XCKU040-2FFVA1156I
FFVA1156_35MM_35MM_1MM

P1V0_MGTAVCC

MGTAVCC

C890 100UF 4V
C854 100UF 4V
C852 100UF 4V
C857 100UF 4V

Caps deleted due to lack of space:
C487,C488,C489,C490,C491,C492,C493,C494
MFG# C3216X6S0G107M160AC

BANK 224

C797 0.47UF 10V 0402_BGA
C801 0.22uF 16V 0402_BGA
C815 0.22uF 16V 0402_BGA

BANK 225

C796 4.7uF 6.3V 0402_BGA
C799 0.47UF 10V 0402_BGA
C808 0.22uF 16V 0402_BGA

BANK 226

C800 4.7uF 6.3V 0402_BGA
C794 0.47UF 10V 0402_BGA
C821 0.22uF 16V 0402_BGA

BANK 227

C817 4.7uF 6.3V 0402_BGA
C822 0.47UF 10V 0402_BGA
C806 0.22uF 16V 0402_BGA

BANK 228

C819 4.7uF 6.3V 0402_BGA
C818 0.47UF 10V 0402_BGA
C814 0.22uF 16V 0402_BGA

U54R

BANK MGTAVTT R
XCKU040FFVA1156

GTH VTT SUPPLY = 1.20V

MGTAVTT_R_AM3 AM3
MGTAVTT_R_AL2 AL2
MGTAVTT_R_AH3 AH3
MGTAVTT_R_AG2 AG2
MGTAVTT_R_AD3 AD3
MGTAVTT_R_AC2 AC2
MGTAVTT_R_Y3 Y3
MGTAVTT_R_W2 W2
MGTAVTT_R_T3 T3
MGTAVTT_R_R2 R2
MGTAVTT_R_M3 M3
MGTAVTT_R_L2 L2
MGTAVTT_R_H3 H3
MGTAVTT_R_G2 G2
MGTAVTT_R_D3 D3
MGTAVTT_R_C2 C2

GROUND

MGTAVTT_L_R32 R32
MGTAVTT_L_P33 P33
MGTAVTT_L_L32 L32
MGTAVTT_L_K33 K33
MGTAVTT_L_H33 H33
MGTAVTT_L_G32 G32
MGTAVTT_L_D33 D33
MGTAVTT_L_C32 C32

100Ohm to MGTAVTT

MGTRREF_R_225_AP5 AP5
MGTAVTTRCAL_R-225_AP6 AP6

R734 100

P1V2_MGTAVTT

XCKU040-2FFVA1156I
FFVA1156_35MM_35MM_1MM

P1V2_MGTAVTT

MGTAVTT

C859 100UF 4V
C850 100UF 4V
C847 100UF 4V
C861 100UF 4V
C876 100UF 4V

Caps deleted due to lack of space:
C521,C522,C523,C524,C525
MFG# C3216X6S0G107M160AC

BANK 224

C846 4.7uF 6.3V 0402_BGA
C848 0.22uF 16V 0402_BGA

BANK 225

C851 4.7uF 6.3V 0402_BGA
C853 0.22uF 16V 0402_BGA

BANK 226

C855 4.7uF 6.3V 0402_BGA
C858 0.22uF 16V 0402_BGA

BANK 227

C860 0.22uF 16V 0402_BGA
C816 0.22uF 16V 0402_BGA

BANK 228

C856 4.7uF 6.3V 0402_BGA
C849 0.22uF 16V 0402_BGA

U54S

BANK MGTVCCAUX S
XCKU040FFVA1156

QPLL = 1.8V

MGTVCCAUX_R_AA6 AA6
MGTVCCAUX_R_R6 R6

GROUND

MGTVCCAUX_L_M29 M29
MGTVCCAUX_L_K29 K29

XCKU040-2FFVA1156I
FFVA1156_35MM_35MM_1MM

P1V8_MGTVCCAUX
LDO

C804 4.7uF 6.3V 0402_BGA
C812 4.7uF 6.3V 0402_BGA
C809 4.7uF 6.3V 0402_BGA
C811 4.7uF 6.3V 0402_BGA
C803 4.7uF 6.3V 0402_BGA

DESIGN NOTES (VCCAUX)
For HP I/O banks with a VCCO of 1.8V and separated VCCO and VCCAUX_IO power supplies, the IL maximum current is 70 µA.

NEED SEPARATE PWR (OR FILTER) FOR THIS BANK POWER ???

GRM155R71C224KA12D

GRM155R61A474KE15D

U54V

BANK VCCAUX V
XCKU040FFVA1156

1.8V

VCCAUX_U8 U8
VCCAUX_W8 W8
VCCAUX_AA8 AA8
VCCAUX_AC8 AC8

1.8V

VCCAUX_IO_N18 N18
VCCAUX_IO_M19 M19
VCCAUX_IO_P19 P19
VCCAUX_IO_R20 R20
VCCAUX_IO_T19 T19
VCCAUX_IO_U20 U20
VCCAUX_IO_V19 V19
VCCAUX_IO_W20 W20
VCCAUX_IO_Y19 Y19
VCCAUX_IO_AB19 AB19
VCCAUX_IO_AC18 AC18

XCKU040-2FFVA1156I
FFVA1156_35MM_35MM_1MM

P1V8_FPGA

VCCAUX

C609 100UF 4V
C709 4.7uF 6.3V 0402_BGA
C712 4.7uF 6.3V 0402_BGA
C805 4.7uF 6.3V 0402_BGA
C717 4.7uF 6.3V 0402_BGA
C807 4.7uF 6.3V 0402_BGA

P1V2_DDR

VCCO_44 VCCO_45 VCCO_46 VCCO_66 VCCO_67 VCCO_68

C674 4.7uF 6.3V 0402_BGA
C679 4.7uF 6.3V 0402_BGA
C704 4.7uF 6.3V 0402_BGA
C675 4.7uF 6.3V 0402_BGA
C747 4.7uF 6.3V 0402_BGA
C719 4.7uF 6.3V 0402_BGA
C761 4.7uF 6.3V 0402_BGA
C820 4.7uF 6.3V 0402_BGA
C643 4.7uF 6.3V 0402_BGA
C745 4.7uF 6.3V 0402_BGA
C678 4.7uF 6.3V 0402_BGA
C762 4.7uF 6.3V 0402_BGA

P1V8_FPGA

VCCO_0 VCCO_65 VCCO_64 VCCO_47 VCCO_48

C716 4.7uF 6.3V 0402_BGA
C798 4.7uF 6.3V 0402_BGA
C708 4.7uF 6.3V 0402_BGA
C676 4.7uF 6.3V 0402_BGA
C644 4.7uF 6.3V 0402_BGA
C746 4.7uF 6.3V 0402_BGA
C795 4.7uF 6.3V 0402_BGA
C677 4.7uF 6.3V 0402_BGA
C706 4.7uF 6.3V 0402_BGA
C645 4.7uF 6.3V 0402_BGA
C646 4.7uF 6.3V 0402_BGA
C802 4.7uF 6.3V 0402_BGA

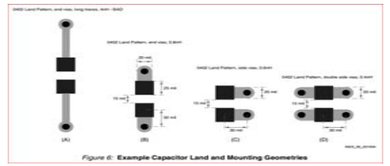

Figure 6: Example Capacitor Land and Mounting Geometries

Title: PG36: FPGA POWER 1/3

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U54T

BANK VCCINT T

XCKU040FFVA1156

1.00V

P1V0_FPGA

VCCINT_M9	M9
VCCINT_M11	M11
VCCINT_M13	M13
VCCINT_M15	M15
VCCINT_N10	N10
VCCINT_N12	N12
VCCINT_N14	N14
VCCINT_P9	P9
VCCINT_P11	P11
VCCINT_P13	P13
VCCINT_P15	P15
VCCINT_R10	R10
VCCINT_R12	R12
VCCINT_R14	R14
VCCINT_T9	T9
VCCINT_T11	T11
VCCINT_T13	T13
VCCINT_T15	T15
VCCINT_U10	U10
VCCINT_U14	U14
VCCINT_V13	V13
VCCINT_V15	V15
VCCINT_W10	W10
VCCINT_W14	W14
VCCINT_Y13	Y13
VCCINT_Y15	Y15
VCCINT_AA10	AA10
VCCINT_AA12	AA12
VCCINT_AA14	AA14
VCCINT_AB11	AB11
VCCINT_AB13	AB13
VCCINT_AB15	AB15
VCCINT_AC10	AC10
VCCINT_AC12	AC12
VCCINT_AC14	AC14
VCCINT_AC16	AC16
VCCINT_T17	T17
VCCINT_N8	N8
VCCINT_R8	R8
VCCINT_N16	N16
VCCINT_R16	R16
VCCINT_U16	U16
VCCINT_W16	W16
VCCINT_AA16	AA16

XCKU040-2FFVA1156I
FFVA1156_35MM_35MM_1MM

U54U

BANK VCCINT_IO U

XCKU040FFVA1156

1.00V

VCCINT_IO_W18	W18
VCCINT_IO_U18	U18
VCCINT_IO_R18	R18
VCCINT_IO_P17	P17
VCCINT_IO_M17	M17

XCKU040-2FFVA1156I
FFVA1156_35MM_35MM_1MM

U54W

BANK VCCBRAM W

XCKU040FFVA1156

1.0V

VCCBRAM_AA18	AA18
VCCBRAM_AB17	AB17
VCCBRAM_Y17	Y17
VCCBRAM_V17	V17

XCKU040-2FFVA1156I
FFVA1156_35MM_35MM_1MM

P1V0_FPGA

VCCINT

C127 470uF 2V, C527 470uF 2V, C526 470uF 2V, C536 470uF 2V, C96 470uF 2V, C512 470uF 2V, C128 470uF 2V, C540 470uF 2V

VCCINT

C122 100UF 4V, C578 100UF 4V, C606 100UF 4V, C610 100UF 4V, C647 100UF 4V

VCCBRAM

C107 100UF 4V, C608 100UF 4V, C95 100UF 4V

VCCINT

C752 4.7uF 6.3V 0402_BGA, C759 4.7uF 6.3V 0402_BGA, C748 4.7uF 6.3V 0402_BGA, C750 4.7uF 6.3V 0402_BGA, C757 4.7uF 6.3V 0402_BGA, C755 4.7uF 6.3V 0402_BGA, C810 4.7uF 6.3V 0402_BGA

VCCBRAM

C713 4.7uF 6.3V 0402_BGA, C705 4.7uF 6.3V 0402_BGA, C710 4.7uF 6.3V 0402_BGA, C760 4.7uF 6.3V 0402_BGA, C707 4.7uF 6.3V 0402_BGA, C749 4.7uF 6.3V 0402_BGA, C758 4.7uF 6.3V 0402_BGA

VCCINT

C751 0.47UF 10V 0402_BGA, C813 0.47UF 10V 0402_BGA, C756 0.47UF 10V 0402_BGA, C714 0.47UF 10V 0402_BGA, C711 0.47UF 10V 0402_BGA, C715 0.47UF 10V 0402_BGA

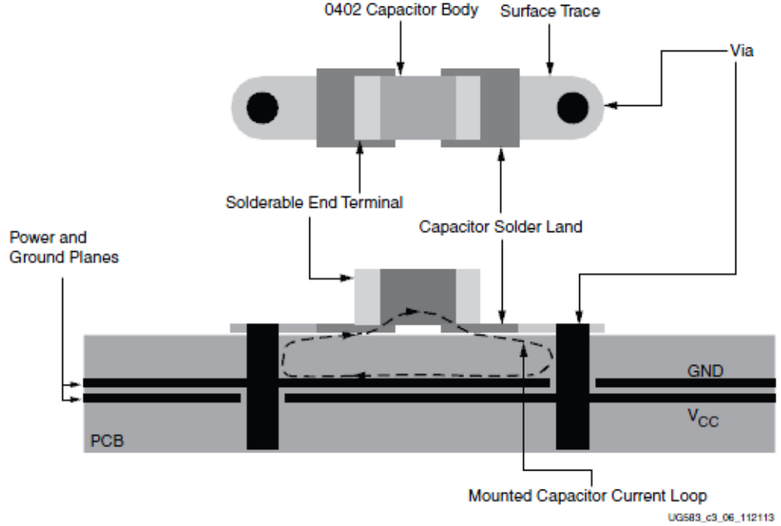

Figure 5-6: **Example Cutaway View of PCB with Capacitor Mounting**

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U54X XCKU040-2FFVA1156I FFVA1156_35MM_35MM_1MM

GROUND 1/2
XCKU040FFVA1156 **X**

GND_A1 GND_A2 GND_A5 GND_A6 GND_A7 GND_A11 GND_A21 GND_A30 GND_A31 GND_A32 GND_B3 GND_B4 GND_B7 GND_B8 GND_B18 GND_B28 GND_B30 GND_B33 GND_B34 GND_C1 GND_C5 GND_C7 GND_C15 GND_C25 GND_C30 GND_C31 GND_D4 GND_D7 GND_D12 GND_D22 GND_D30 GND_D34 GND_E1 GND_E2 GND_E5 GND_E7 GND_E9 GND_E19 GND_E29 GND_E30 GND_E32 GND_F3 GND_F4 GND_F7 GND_F16 GND_F26 GND_F28 GND_F29 GND_F33 GND_F34 GND_G1 GND_G5 GND_G7 GND_G13 GND_G23 GND_G28 GND_G31 GND_H4 GND_H7 GND_H10 GND_H20 GND_H28 GND_H30 GND_H34 GND_J1 GND_J2 GND_J5 GND_J7 GND_J17 GND_J27 GND_J28 GND_J32 GND_K3 GND_K4 GND_K14 GND_K24 GND_K28 GND_K30 GND_K34 GND_L1 GND_L5 GND_L11 GND_L21 GND_L28 GND_L31 GND_M4 GND_M8 GND_M10 GND_M12 GND_M14 GND_M16 GND_M18 GND_M28 GND_M30 GND_M33 GND_M34 GND_N1 GND_N2 GND_N5 GND_N9 GND_N11 GND_N13 GND_N15 GND_N17 GND_N19 GND_N25 GND_N28 GND_N32 GND_P3 GND_P4 GND_P10 GND_P12 GND_P14 GND_P16 GND_P18 GND_P22 GND_P28 GND_P30 GND_P34 GND_R1 GND_R5 GND_R9 GND_R11 GND_R13 GND_R15 GND_R17 GND_R19 GND_R28 GND_R31 GND_T4 GND_T8 GND_T10 GND_T12 GND_T14

A1 A2 A5 A6 A7 A11 A21 A30 A31 A32 B3 B4 B7 B8 B18 B28 B30 B33 B34 C1 C5 C7 C15 C25 C30 C31 D4 D7 D12 D22 D30 D34 E1 E2 E5 E7 E9 E19 E29 E30 E32 F3 F4 F7 F16 F26 F28 F29 F33 F34 G1 G5 G7 G13 G23 G28 G31 H4 H7 H10 H20 H28 H30 H34 J1 J2 J5 J7 J17 J27 J28 J32 K3 K4 K14 K24 K28 K30 K34 L1 L5 L11 L21 L28 L31 M4 M8 M10 M12 M14 M16 M18 M28 M30 M33 M34 N1 N2 N5 N9 N11 N13 N15 N17 N19 N25 N28 N32 P3 P4 P10 P12 P14 P16 P18 P22 P28 P30 P34 R1 R5 R9 R11 R13 R15 R17 R19 R28 R31 T4 T8 T10 T12 T14

U54Y XCKU040-2FFVA1156I FFVA1156_35MM_35MM_1MM

GROUND 2/2
XCKU040FFVA1156 **Y**

GND_T16 GND_T18 GND_T20 GND_T26 GND_T28 GND_T29 GND_T30 GND_T33 GND_T34 GND_U1 GND_U2 GND_U5 GND_Y8 GND_U13 GND_U15 GND_U17 GND_U19 GND_U23 GND_U30 GND_U31 GND_U32 GND_U33 GND_V3 GND_V4 GND_V10 GND_V14 GND_V16 GND_V18 GND_V20 GND_V30 GND_W1 GND_W5 GND_AB8 GND_W13 GND_W15 GND_W17 GND_W19 GND_W27 GND_Y4 GND_Y10 GND_Y14 GND_Y16 GND_Y18 GND_Y20 GND_Y24 GND_Y34 GND_AA1 GND_AA2 GND_AA5 GND_P8 GND_AA11 GND_AA13 GND_AA15 GND_AA17 GND_AA19 GND_AA21 GND_AA31 GND_AB3 GND_AB4 GND_AB10 GND_AB12 GND_AB14 GND_AB16 GND_AB18 GND_AB28 GND_AC1 GND_AC5 GND_V8 GND_AC11 GND_AC13 GND_AC15 GND_AC17 GND_AC19 GND_AC25 GND_AD4 GND_AD12 GND_AD22 GND_AD32 GND_AE1 GND_AE2 GND_AE5 GND_AE7 GND_AE9 GND_AE19 GND_AE29 GND_AF3 GND_AF4 GND_AF7 GND_AF16 GND_AF26 GND_AG1 GND_AG5 GND_AG7 GND_AG13 GND_AG23 GND_AG33 GND_AH4 GND_AH7 GND_AH10 GND_AH20 GND_AH30 GND_AJ1 GND_AJ2 GND_AJ5 GND_AJ7 GND_AJ17 GND_AJ27 GND_AK3 GND_AK4 GND_AK7 GND_AK14 GND_AK24 GND_AK34 GND_AL1 GND_AL5 GND_AL7 GND_AL11 GND_AL21 GND_AL31 GND_AM4 GND_AM7 GND_AM8 GND_AM18 GND_AM28 GND_AN1 GND_AN2 GND_AN5 GND_AN7 GND_AN15 GND_AN25 GND_AP3 GND_AP4 GND_AP7 GND_AP12 GND_AP22 GND_AP32

T16 T18 T20 T26 T28 T29 T30 T33 T34 U1 U2 U5 Y8 U13 U15 U17 U19 U23 U30 U31 U32 U33 V3 V4 V10 V14 V16 V18 V20 V30 W1 W5 AB8 W13 W15 W17 W19 W27 Y4 Y10 Y14 Y16 Y18 Y20 Y24 Y34 AA1 AA2 AA5 P8 AA11 AA13 AA15 AA17 AA19 AA21 AA31 AB3 AB4 AB10 AB12 AB14 AB16 AB18 AB28 AC1 AC5 V8 AC11 AC13 AC15 AC17 AC19 AC25 AD4 AD12 AD22 AD32 AE1 AE2 AE5 AE7 AE9 AE19 AE29 AF3 AF4 AF7 AF16 AF26 AG1 AG5 AG7 AG13 AG23 AG33 AH4 AH7 AH10 AH20 AH30 AJ1 AJ2 AJ5 AJ7 AJ17 AJ27 AK3 AK4 AK7 AK14 AK24 AK34 AL1 AL5 AL7 AL11 AL21 AL31 AM4 AM7 AM8 AM18 AM28 AN1 AN2 AN5 AN7 AN15 AN25 AP3 AP4 AP7 AP12 AP22 AP32

U54Z XCKU040-2FFVA1156I FFVA1156_35MM_35MM_1MM

NO CONNECTIONS
XCKU040FFVA1156 **Z**

NC_K31 NC_J33 NC_J34 NC_K32 NC_N29 NC_N30 NC_M31 NC_L33 NC_L34 NC_M32 NC_A34 NC_A33 NC_P31 NC_N33 NC_N34 NC_P32 NC_R29 NC_R30 NC_T31 NC_R33 NC_R34 NC_T32 NC_B31 NC_C33 NC_C34 NC_B32 NC_J29 NC_J30 NC_D31 NC_E33 NC_E34 NC_D32 NC_G29 NC_F31 NC_F32 NC_G30 NC_L29 NC_L30 NC_H31 NC_G33 NC_G34 NC_H32

K31 J33 J34 K32 N29 N30 M31 L33 L34 M32 A34 A33 P31 N33 N34 P32 R29 R30 T31 R33 R34 T32 B31 C33 C34 B32 J29 J30 D31 E33 E34 D32 G29 F31 F32 G30 L29 L30 H31 G33 G34 H32

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U49 BYPASS CAPS

P1V2_DDR

C694 0.022UF 6.3V CAP0201_BGA	C845 0.022UF 6.3V CAP0201_BGA	C693 0.022UF 6.3V CAP0201_BGA	C869 0.022UF 6.3V CAP0201_BGA	C765 0.022UF 6.3V CAP0201_BGA	C831 0.022UF 6.3V CAP0201_BGA	C788 0.022UF 6.3V CAP0201_BGA
C843 0.47uF 6.3V CAP0201_BGA	C615 0.47uF 6.3V CAP0201_BGA	C612 0.47uF 6.3V CAP0201_BGA	C681 0.47uF 6.3V CAP0201_BGA	C730 0.47uF 6.3V CAP0201_BGA	C722 0.47uF 6.3V CAP0201_BGA	C733 0.47uF 6.3V CAP0201_BGA
C904 4.7uF 6.3V SMD-0402	C901 4.7uF 6.3V SMD-0402					

BANK1 DDR4: MEMORY #1

DNI

U61

P1V2_DDR

VDDQ1 A1, VDDQ2 A9, VDDQ3 C1, VDDQ4 D9, VDDQ5 F2, VDDQ6 F8, VDDQ7 G1, VDDQ8 G9, VDDQ9 J2, VDDQ10 J8

VDD1 B3, VDD2 B9, VDD3 D1, VDD4 G7, VDD5 J1, VDD6 J9, VDD7 L1, VDD8 L9, VDD9 R1, VDD10 T9

P28,40,41,42 BANK1_DDR4_A00	BANK1_DDR4_A00	P3	A0
P28,40,41,42 BANK1_DDR4_A01	BANK1_DDR4_A01	P7	A1
P28,40,41,42 BANK1_DDR4_A02	BANK1_DDR4_A02	R3	A2
P28,40,41,42 BANK1_DDR4_A03	BANK1_DDR4_A03	N7	A3
P28,40,41,42 BANK1_DDR4_A04	BANK1_DDR4_A04	N3	A4
P28,40,41,42 BANK1_DDR4_A05	BANK1_DDR4_A05	P8	A5
P28,40,41,42 BANK1_DDR4_A06	BANK1_DDR4_A06	P2	A6
P28,40,41,42 BANK1_DDR4_A07	BANK1_DDR4_A07	R8	A7
P28,40,41,42 BANK1_DDR4_A08	BANK1_DDR4_A08	R2	A8
P28,40,41,42 BANK1_DDR4_A09	BANK1_DDR4_A09	R7	A9
P28,40,41,42 BANK1_DDR4_A10	BANK1_DDR4_A10	M3	A10/AP
P28,40,41,42 BANK1_DDR4_A11	BANK1_DDR4_A11	T2	A11
P28,40,41,42 BANK1_DDR4_A12	BANK1_DDR4_A12	M7	A12/BC_B
P28,40,41,42 BANK1_DDR4_A13	BANK1_DDR4_A13	T8	A13
		T7	A14/NC
P28,40,41,42 BANK1_DDR4_BA0	BANK1_DDR4_BA0	N2	BA0
P28,40,41,42 BANK1_DDR4_BA1	BANK1_DDR4_BA1	N8	BA1
P28,40,41,42 BANK1_DDR4_BG0	BANK1_DDR4_BG0	M2	BA2/BG0
P28,40,41,42 BANK1_DDR4_CAS_B	BANK1_DDR4_CAS_B	M8	CAS_B/A15
P28,40,41,42 BANK1_DDR4_RAS_B	BANK1_DDR4_RAS_B	L8	RAS_B/A16
P28,40,41,42 BANK1_DDR4_WE_B	BANK1_DDR4_WE_B	L2	WE_B/A14
P28,40,41,42 BANK1_DDR4_CK_T	BANK1_DDR4_CK_T	K7	CK_T
P28,40,41,42 BANK1_DDR4_CK_C	BANK1_DDR4_CK_C	K8	CK_C
P28,40,41,42 BANK1_DDR4_CKE	BANK1_DDR4_CKE	K2	CKE
P28,40,41,42 BANK1_DDR4_ACT_B	BANK1_DDR4_ACT_B	L3	ACT_B
P28,40,41,42 BANK1_DDR4_TEN	BANK1_DDR4_TEN	N9	TEN
P28,40,41,42 BANK1_DDR4_ALERT_B	BANK1_DDR4_ALERT_B	P9	ALERT_B
P28,40,41,42 BANK1_DDR4_PAR	BANK1_DDR4_PAR	T3	PAR
P28,40,41,42 BANK1_DDR4_RESET_B	BANK1_DDR4_RESET_B	P1	RESET_B
P28,40,41,42 BANK1_DDR4_ODT	BANK1_DDR4_ODT	K3	ODT
P28,40,41,42 BANK1_DDR4_CS_B	BANK1_DDR4_CS_B	L7	CS_B

DDR4
MT40A256M16GE-083E:B
4Gb, 256Mx16b,
1200MHz, 1.2V, 0~95C,
0.833ns@CL=16,
96Ball, 9MMX14MM

MT40A256M16GE-083E IT:B
FBGA96_9MMX14MM_08MM

VSSQ1 A2, VSSQ2 A8, VSSQ3 C9, VSSQ4 D2, VSSQ5 D8, VSSQ6 E3, VSSQ7 E8, VSSQ8 F1, VSSQ9 H1, VSSQ10 H9

VSS1 B2, VSS2 E1, VSS3 E9, VSS4 G8, VSS5 K1, VSS6 K9, VSS7 M9, VSS8 N1, VSS9 T1

ZQ F9 — R733 240

VREFCA M1

VPP1 B1, VPP2 R9

P1V2_DDR — C867 0.01uF 50V — R758 100; C866 0.01uF 50V — R757 100

P2V5_SYS

DESIGN NOTES (VREFCA)
VREFCA is a reference suppy input equal to VDD/2 and it does not draw biasing current.

DESIGN NOTES (VPP)
VPP must ramp at the same time or before VDD, and VPP must be equal to or higher than VDD at all times. After VDD has ramped and reached the stable level, the initialization sequence must be started within 64ms.

DQ0	G2	BANK1_DDR4_DQ04	BANK1_DDR4_DQ04 P29
DQ1	F7	BANK1_DDR4_DQ07	BANK1_DDR4_DQ07 P29
DQ2	H3	BANK1_DDR4_DQ05	BANK1_DDR4_DQ05 P29
DQ3	H7	BANK1_DDR4_DQ03	BANK1_DDR4_DQ03 P29
DQ4	H2	BANK1_DDR4_DQ00	BANK1_DDR4_DQ00 P29
DQ5	H8	BANK1_DDR4_DQ01	BANK1_DDR4_DQ01 P29
DQ6	J3	BANK1_DDR4_DQ02	BANK1_DDR4_DQ02 P29
DQ7	J7	BANK1_DDR4_DQ06	BANK1_DDR4_DQ06 P29
DQ8	A3	BANK1_DDR4_DQ13	BANK1_DDR4_DQ13 P29
DQ9	B8	BANK1_DDR4_DQ10	BANK1_DDR4_DQ10 P29
DQ10	C3	BANK1_DDR4_DQ11	BANK1_DDR4_DQ11 P29
DQ11	C7	BANK1_DDR4_DQ14	BANK1_DDR4_DQ14 P29
DQ12	C2	BANK1_DDR4_DQ15	BANK1_DDR4_DQ15 P29
DQ13	C8	BANK1_DDR4_DQ12	BANK1_DDR4_DQ12 P29
DQ14	D3	BANK1_DDR4_DQ09	BANK1_DDR4_DQ09 P29
DQ15	D7	BANK1_DDR4_DQ08	BANK1_DDR4_DQ08 P29
DQSL_T	G3	BANK1_DDR4_DQS0_T	BANK1_DDR4_DQS0_T P29
DQSL_C	F3	BANK1_DDR4_DQS0_C	BANK1_DDR4_DQS0_C P29
DQSU_T	B7	BANK1_DDR4_DQS1_T	BANK1_DDR4_DQS1_T P29
DQSU_C	A7	BANK1_DDR4_DQS1_C	BANK1_DDR4_DQS1_C P29
DML_B/DBIL	E7	BANK1_DDR4_DM0	BANK1_DDR4_DM0 P29
DMU_B/DBIU	E2	BANK1_DDR4_DM1	BANK1_DDR4_DM1 P29

Title: **PG39: DDR4#1 DQ[15:0]**

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U50 BYPASS CAPS

P1V2_DDR

C735 0.022UF 6.3V CAP0201_BGA
C741 0.022UF 6.3V CAP0201_BGA
C695 0.022UF 6.3V CAP0201_BGA
C840 0.022UF 6.3V CAP0201_BGA
C865 0.022UF 6.3V CAP0201_BGA
C871 0.022UF 6.3V CAP0201_BGA
C841 0.022UF 6.3V CAP0201_BGA

C767 0.47uF 6.3V CAP0201_BGA
C863 0.47uF 6.3V CAP0201_BGA
C731 0.47uF 6.3V CAP0201_BGA
C641 0.47uF 6.3V CAP0201_BGA
C718 0.47uF 6.3V CAP0201_BGA
C769 0.47uF 6.3V CAP0201_BGA
C613 0.47uF 6.3V CAP0201_BGA

C835 4.7uF 6.3V SMD-0402
C873 4.7uF 6.3V SMD-0402

BANK1 DDR4: MEMORY #2

P1V2_DDR

C783 0.01uF 50V — R732 100
C781 0.01uF 50V — R731 100

P1V2_DDR
P2V5_SYS

DNI
U56

VDDQ1 A1, VDDQ2 A9, VDDQ3 C1, VDDQ4 D9, VDDQ5 F2, VDDQ6 F8, VDDQ7 G1, VDDQ8 G9, VDDQ9 J2, VDDQ10 J8
VDD1 B3, VDD2 B9, VDD3 D1, VDD4 G7, VDD5 J1, VDD6 J9, VDD7 L1, VDD8 L9, VDD9 R1, VDD10 T9

ZQ F9 — R700 240
VREFCA M1
VPP1 B1
VPP2 R9

DDR4
MT40A256M16GE-083E:B
4Gb, 256Mx16b,
1200MHz, 1.2V, 0~95C,
0.833ns@CL=16,
96Ball, 9MMX14MM

P28,39,41,42 BANK1_DDR4_A00	BANK1_DDR4_A00	P3	A0
P28,39,41,42 BANK1_DDR4_A01	BANK1_DDR4_A01	P7	A1
P28,39,41,42 BANK1_DDR4_A02	BANK1_DDR4_A02	R3	A2
P28,39,41,42 BANK1_DDR4_A03	BANK1_DDR4_A03	N7	A3
P28,39,41,42 BANK1_DDR4_A04	BANK1_DDR4_A04	N3	A4
P28,39,41,42 BANK1_DDR4_A05	BANK1_DDR4_A05	P8	A5
P28,39,41,42 BANK1_DDR4_A06	BANK1_DDR4_A06	P2	A6
P28,39,41,42 BANK1_DDR4_A07	BANK1_DDR4_A07	R8	A7
P28,39,41,42 BANK1_DDR4_A08	BANK1_DDR4_A08	R2	A8
P28,39,41,42 BANK1_DDR4_A09	BANK1_DDR4_A09	R7	A9
P28,39,41,42 BANK1_DDR4_A10	BANK1_DDR4_A10	M3	A10/AP
P28,39,41,42 BANK1_DDR4_A11	BANK1_DDR4_A11	T2	A11
P28,39,41,42 BANK1_DDR4_A12	BANK1_DDR4_A12	M7	A12/BC_B
P28,39,41,42 BANK1_DDR4_A13	BANK1_DDR4_A13	T8	A13
		T7	A14/NC
P28,39,41,42 BANK1_DDR4_BA0	BANK1_DDR4_BA0	N2	BA0
P28,39,41,42 BANK1_DDR4_BA1	BANK1_DDR4_BA1	N8	BA1
P28,39,41,42 BANK1_DDR4_BG0	BANK1_DDR4_BG0	M2	BA2/BG0
P28,39,41,42 BANK1_DDR4_CAS_B	BANK1_DDR4_CAS_B	M8	CAS_B/A15
P28,39,41,42 BANK1_DDR4_RAS_B	BANK1_DDR4_RAS_B	L8	RAS_B/A16
P28,39,41,42 BANK1_DDR4_WE_B	BANK1_DDR4_WE_B	L2	WE_B/A14
P28,39,41,42 BANK1_DDR4_CK_T	BANK1_DDR4_CK_T	K7	CK_T
P28,39,41,42 BANK1_DDR4_CK_C	BANK1_DDR4_CK_C	K8	CK_C
P28,39,41,42 BANK1_DDR4_CKE	BANK1_DDR4_CKE	K2	CKE
P28,39,41,42 BANK1_DDR4_ACT_B	BANK1_DDR4_ACT_B	L3	ACT_B
P28,39,41,42 BANK1_DDR4_TEN	BANK1_DDR4_TEN	N9	TEN
P28,39,41,42 BANK1_DDR4_ALERT_B	BANK1_DDR4_ALERT_B	P9	ALERT_B
P28,39,41,42 BANK1_DDR4_PAR	BANK1_DDR4_PAR	T3	PAR
P28,39,41,42 BANK1_DDR4_RESET_B	BANK1_DDR4_RESET_B	P1	RESET_B
P28,39,41,42 BANK1_DDR4_ODT	BANK1_DDR4_ODT	K3	ODT
P28,39,41,42 BANK1_DDR4_CS_B	BANK1_DDR4_CS_B	L7	CS_B

DQ0	G2	BANK1_DDR4_DQ16	BANK1_DDR4_DQ16 P29
DQ1	F7	BANK1_DDR4_DQ19	BANK1_DDR4_DQ19 P29
DQ2	H3	BANK1_DDR4_DQ22	BANK1_DDR4_DQ22 P29
DQ3	H7	BANK1_DDR4_DQ23	BANK1_DDR4_DQ23 P29
DQ4	H2	BANK1_DDR4_DQ20	BANK1_DDR4_DQ20 P29
DQ5	H8	BANK1_DDR4_DQ21	BANK1_DDR4_DQ21 P29
DQ6	J3	BANK1_DDR4_DQ18	BANK1_DDR4_DQ18 P29
DQ7	J7	BANK1_DDR4_DQ17	BANK1_DDR4_DQ17 P29
DQ8	A3	BANK1_DDR4_DQ29	BANK1_DDR4_DQ29 P29
DQ9	B8	BANK1_DDR4_DQ25	BANK1_DDR4_DQ25 P29
DQ10	C3	BANK1_DDR4_DQ24	BANK1_DDR4_DQ24 P29
DQ11	C7	BANK1_DDR4_DQ26	BANK1_DDR4_DQ26 P29
DQ12	C2	BANK1_DDR4_DQ31	BANK1_DDR4_DQ31 P29
DQ13	C8	BANK1_DDR4_DQ27	BANK1_DDR4_DQ27 P29
DQ14	D3	BANK1_DDR4_DQ28	BANK1_DDR4_DQ28 P29
DQ15	D7	BANK1_DDR4_DQ30	BANK1_DDR4_DQ30 P29
DQSL_T	G3	BANK1_DDR4_DQS2_T	BANK1_DDR4_DQS2_T P29
DQSL_C	F3	BANK1_DDR4_DQS2_C	BANK1_DDR4_DQS2_C P29
DQSU_T	B7	BANK1_DDR4_DQS3_T	BANK1_DDR4_DQS3_T P29
DQSU_C	A7	BANK1_DDR4_DQS3_C	BANK1_DDR4_DQS3_C P29
DML_B/DBIL	E7	BANK1_DDR4_DM2	BANK1_DDR4_DM2 P29
DMU_B/DBIU	E2	BANK1_DDR4_DM3	BANK1_DDR4_DM3 P29

VSSQ1 A2, VSSQ2 A8, VSSQ3 C9, VSSQ4 D2, VSSQ5 D8, VSSQ6 E3, VSSQ7 E8, VSSQ8 F1, VSSQ9 H1, VSSQ10 H9
VSS1 B2, VSS2 E1, VSS3 E9, VSS4 G8, VSS5 K1, VSS6 K9, VSS7 M9, VSS8 N1, VSS9 T1

MT40A256M16GE-083E IT:B
FBGA96_9MMX14MM_08MM

Title: **PG40: DDR4#1 DQ[31:16]**
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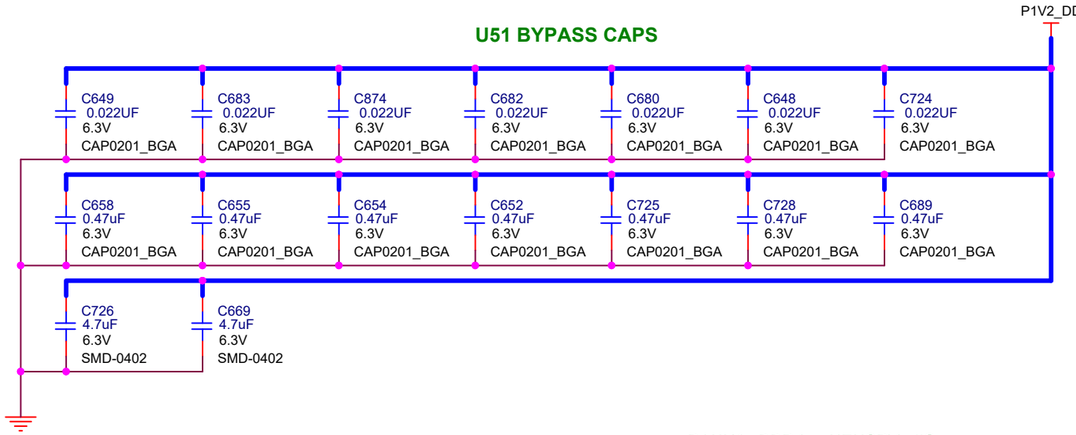
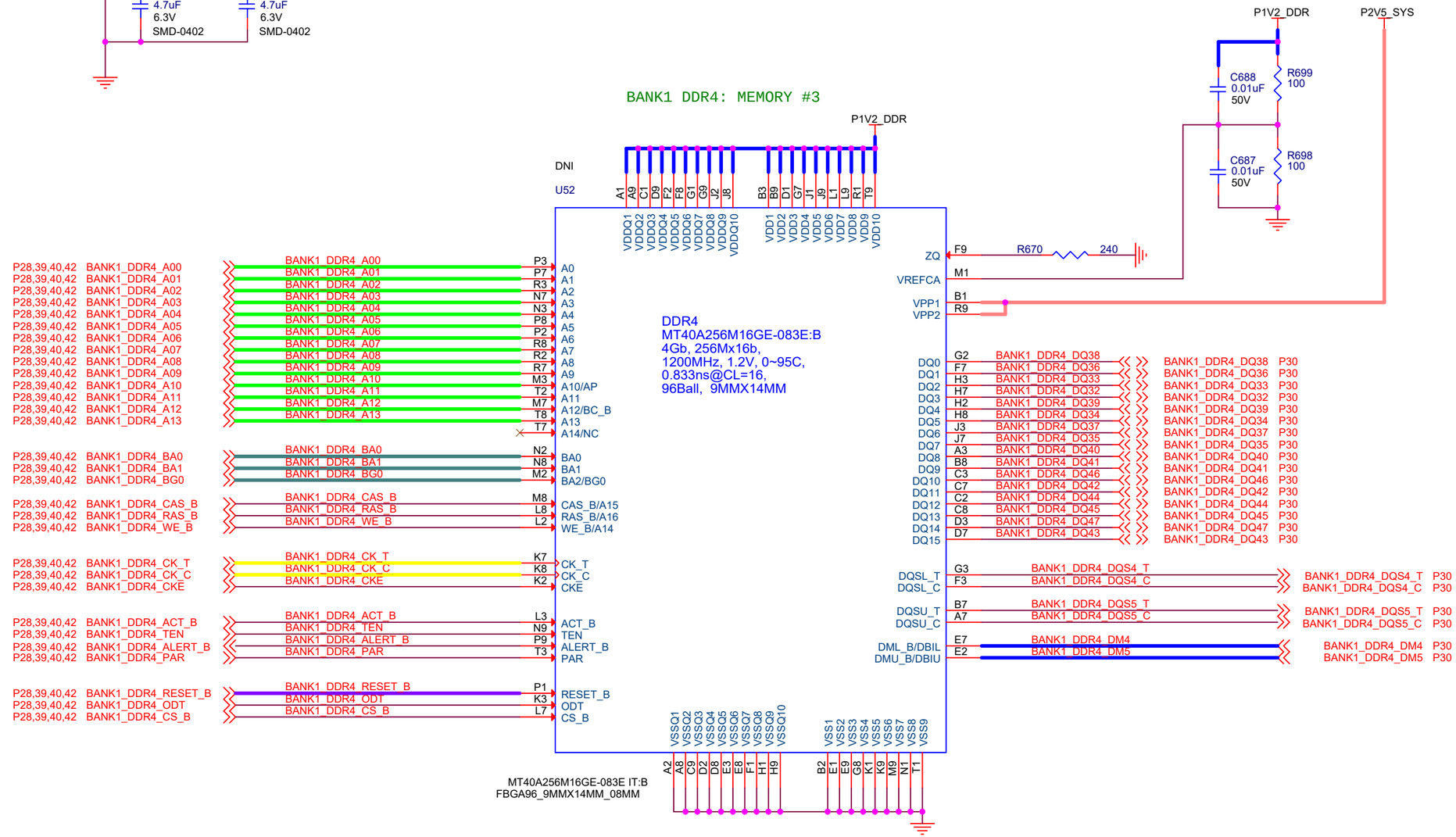
U51 BYPASS CAPS



BANK1 DDR4: MEMORY #3



Title: **PG41: DDR4#1 DQ[47:32]**

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U52 BYPASS CAPS

P1V2_DDR

C868 0.022UF 6.3V CAP0201_BGA
C898 0.022UF 6.3V CAP0201_BGA
C829 0.022UF 6.3V CAP0201_BGA
C872 0.022UF 6.3V CAP0201_BGA
C743 0.022UF 6.3V CAP0201_BGA
C670 0.022UF 6.3V CAP0201_BGA
C697 0.022UF 6.3V CAP0201_BGA

C744 0.47uF 6.3V CAP0201_BGA
C899 0.47uF 6.3V CAP0201_BGA
C642 0.47uF 6.3V CAP0201_BGA
C902 0.47uF 6.3V CAP0201_BGA
C640 0.47uF 6.3V CAP0201_BGA
C668 0.47uF 6.3V CAP0201_BGA
C686 0.47uF 6.3V CAP0201_BGA

C576 4.7uF 6.3V SMD-0402
C784 4.7uF 6.3V SMD-0402

BANK1 DDR4: MEMORY #4

DNI

U48

DDR4
MT40A256M16GE-083E:B
4Gb, 256Mx16b,
1200MHz, 1.2V, 0~95C,
0.833ns@CL=16,
96Ball, 9MMX14MM

MT40A256M16GE-083E IT:B
FBGA96_9MMX14MM_08MM

P28,39,40,41	BANK1_DDR4_A00	P3	A0
P28,39,40,41	BANK1_DDR4_A01	P7	A1
P28,39,40,41	BANK1_DDR4_A02	R3	A2
P28,39,40,41	BANK1_DDR4_A03	N7	A3
P28,39,40,41	BANK1_DDR4_A04	N3	A4
P28,39,40,41	BANK1_DDR4_A05	P8	A5
P28,39,40,41	BANK1_DDR4_A06	P2	A6
P28,39,40,41	BANK1_DDR4_A07	R8	A7
P28,39,40,41	BANK1_DDR4_A08	R2	A8
P28,39,40,41	BANK1_DDR4_A09	R7	A9
P28,39,40,41	BANK1_DDR4_A10	M3	A10/AP
P28,39,40,41	BANK1_DDR4_A11	T2	A11
P28,39,40,41	BANK1_DDR4_A12	M7	A12/BC_B
P28,39,40,41	BANK1_DDR4_A13	T8	A13
		T7	A14/NC
P28,39,40,41	BANK1_DDR4_BA0	N2	BA0
P28,39,40,41	BANK1_DDR4_BA1	N8	BA1
P28,39,40,41	BANK1_DDR4_BG0	M2	BA2/BG0
P28,39,40,41	BANK1_DDR4_CAS_B	M8	CAS_B/A15
P28,39,40,41	BANK1_DDR4_RAS_B	L8	RAS_B/A16
P28,39,40,41	BANK1_DDR4_WE_B	L2	WE_B/A14
P28,39,40,41	BANK1_DDR4_CK_T	K7	CK_T
P28,39,40,41	BANK1_DDR4_CK_C	K8	CK_C
P28,39,40,41	BANK1_DDR4_CKE	K2	CKE
P28,39,40,41	BANK1_DDR4_ACT_B	L3	ACT_B
P28,39,40,41	BANK1_DDR4_TEN	N9	TEN
P28,39,40,41	BANK1_DDR4_ALERT_B	P9	ALERT_B
P28,39,40,41	BANK1_DDR4_PAR	T3	PAR
P28,39,40,41	BANK1_DDR4_RESET_B	P1	RESET_B
P28,39,40,41	BANK1_DDR4_ODT	K3	ODT
P28,39,40,41	BANK1_DDR4_CS_B	L7	CS_B

VDDQ1 A1, VDDQ2 A9, VDDQ3 C1, VDDQ4 D9, VDDQ5 F2, VDDQ6 F8, VDDQ7 G1, VDDQ8 G9, VDDQ9 J2, VDDQ10 J8
VDD1 B3, VDD2 B9, VDD3 D1, VDD4 G7, VDD5 J1, VDD6 J9, VDD7 L1, VDD8 L9, VDD9 R1, VDD10 T9

VSSQ1 A2, VSSQ2 A8, VSSQ3 C9, VSSQ4 D2, VSSQ5 D8, VSSQ6 E3, VSSQ7 E8, VSSQ8 F1, VSSQ9 H1, VSSQ10 H9
VSS1 B2, VSS2 E1, VSS3 E9, VSS4 G8, VSS5 K1, VSS6 K9, VSS7 M9, VSS8 N1, VSS9 T1

P1V2_DDR

C599 0.01uF 50V
R641 100
C598 0.01uF 50V
R640 100

P2V5_SYS

ZQ F9 R612 240
VREFCA M1
VPP1 B1
VPP2 R9

DQ0	G2	BANK1_DDR4_DQ52	BANK1_DDR4_DQ52	P30
DQ1	F7	BANK1_DDR4_DQ53	BANK1_DDR4_DQ53	P30
DQ2	H3	BANK1_DDR4_DQ50	BANK1_DDR4_DQ50	P30
DQ3	H7	BANK1_DDR4_DQ49	BANK1_DDR4_DQ49	P30
DQ4	H2	BANK1_DDR4_DQ55	BANK1_DDR4_DQ55	P30
DQ5	H8	BANK1_DDR4_DQ48	BANK1_DDR4_DQ48	P30
DQ6	J3	BANK1_DDR4_DQ51	BANK1_DDR4_DQ51	P30
DQ7	J7	BANK1_DDR4_DQ54	BANK1_DDR4_DQ54	P30
DQ8	A3	BANK1_DDR4_DQ61	BANK1_DDR4_DQ61	P30
DQ9	B8	BANK1_DDR4_DQ58	BANK1_DDR4_DQ58	P30
DQ10	C3	BANK1_DDR4_DQ63	BANK1_DDR4_DQ63	P30
DQ11	C7	BANK1_DDR4_DQ56	BANK1_DDR4_DQ56	P30
DQ12	C2	BANK1_DDR4_DQ59	BANK1_DDR4_DQ59	P30
DQ13	C8	BANK1_DDR4_DQ60	BANK1_DDR4_DQ60	P30
DQ14	D3	BANK1_DDR4_DQ57	BANK1_DDR4_DQ57	P30
DQ15	D7	BANK1_DDR4_DQ62	BANK1_DDR4_DQ62	P30
DQSL_T	G3	BANK1_DDR4_DQS6_T	BANK1_DDR4_DQS6_T	P30
DQSL_C	F3	BANK1_DDR4_DQS6_C	BANK1_DDR4_DQS6_C	P30
DQSU_T	B7	BANK1_DDR4_DQS7_T	BANK1_DDR4_DQS7_T	P30
DQSU_C	A7	BANK1_DDR4_DQS7_C	BANK1_DDR4_DQS7_C	P30
DML_B/DBIL	E7	BANK1_DDR4_DM6	BANK1_DDR4_DM6	P30
DMU_B/DBIU	E2	BANK1_DDR4_DM7	BANK1_DDR4_DM7	P30

Title: **PG42: DDR4#1 DQ[63:48]**

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U53 BYPASS CAPS

P1V2_DDR

C577 0.022UF 6.3V CAP0201_BGA
C701 0.022UF 6.3V CAP0201_BGA
C604 0.022UF 6.3V CAP0201_BGA
C742 0.022UF 6.3V CAP0201_BGA
C782 0.022UF 6.3V CAP0201_BGA
C639 0.022UF 6.3V CAP0201_BGA
C826 0.022UF 6.3V CAP0201_BGA

C828 0.47uF 6.3V CAP0201_BGA
C785 0.47uF 6.3V CAP0201_BGA
C692 0.47uF 6.3V CAP0201_BGA
C832 0.47uF 6.3V CAP0201_BGA
C768 0.47uF 6.3V CAP0201_BGA
C633 0.47uF 6.3V CAP0201_BGA
C650 0.47uF 6.3V CAP0201_BGA

C791 4.7uF 6.3V SMD-0402
C651 4.7uF 6.3V SMD-0402

BANK2 DDR4: MEMORY #1

P1V2_DDR

U55

P31,44,45,46 BANK2_DDR4_A00	BANK2_DDR4_A00	P3	A0
P31,44,45,46 BANK2_DDR4_A01	BANK2_DDR4_A01	P7	A1
P31,44,45,46 BANK2_DDR4_A02	BANK2_DDR4_A02	R3	A2
P31,44,45,46 BANK2_DDR4_A03	BANK2_DDR4_A03	N7	A3
P31,44,45,46 BANK2_DDR4_A04	BANK2_DDR4_A04	N3	A4
P31,44,45,46 BANK2_DDR4_A05	BANK2_DDR4_A05	P8	A5
P31,44,45,46 BANK2_DDR4_A06	BANK2_DDR4_A06	P2	A6
P31,44,45,46 BANK2_DDR4_A07	BANK2_DDR4_A07	R8	A7
P31,44,45,46 BANK2_DDR4_A08	BANK2_DDR4_A08	R2	A8
P31,44,45,46 BANK2_DDR4_A09	BANK2_DDR4_A09	R7	A9
P31,44,45,46 BANK2_DDR4_A10	BANK2_DDR4_A10	M3	A10/AP
P31,44,45,46 BANK2_DDR4_A11	BANK2_DDR4_A11	T2	A11
P31,44,45,46 BANK2_DDR4_A12	BANK2_DDR4_A12	M7	A12/BC_B
P31,44,45,46 BANK2_DDR4_A13	BANK2_DDR4_A13	T8	A13
		T7	A14/NC
P31,44,45,46 BANK2_DDR4_BA0	BANK2_DDR4_BA0	N2	BA0
P31,44,45,46 BANK2_DDR4_BA1	BANK2_DDR4_BA1	N8	BA1
P31,44,45,46 BANK2_DDR4_BG0	BANK2_DDR4_BG0	M2	BA2/BG0
P31,44,45,46 BANK2_DDR4_CAS_B	BANK2_DDR4_CAS_B	M8	CAS_B/A15
P31,44,45,46 BANK2_DDR4_RAS_B	BANK2_DDR4_RAS_B	L8	RAS_B/A16
P31,44,45,46 BANK2_DDR4_WE_B	BANK2_DDR4_WE_B	L2	WE_B/A14
P31,44,45,46 BANK2_DDR4_CK_T	BANK2_DDR4_CK_T	K7	CK_T
P31,44,45,46 BANK2_DDR4_CK_C	BANK2_DDR4_CK_C	K8	CK_C
P31,44,45,46 BANK2_DDR4_CKE	BANK2_DDR4_CKE	K2	CKE
P31,44,45,46 BANK2_DDR4_ACT_B	BANK2_DDR4_ACT_B	L3	ACT_B
P31,44,45,46 BANK2_DDR4_TEN	BANK2_DDR4_TEN	N9	TEN
P31,44,45,46 BANK2_DDR4_ALERT_B	BANK2_DDR4_ALERT_B	P9	ALERT_B
P31,44,45,46 BANK2_DDR4_PAR	BANK2_DDR4_PAR	T3	PAR
P31,44,45,46 BANK2_DDR4_RESET_B	BANK2_DDR4_RESET_B	P1	RESET_B
P31,44,45,46 BANK2_DDR4_ODT	BANK2_DDR4_ODT	K3	ODT
P31,44,45,46 BANK2_DDR4_CS_B	BANK2_DDR4_CS_B	L7	CS_B

VDDQ1 VDDQ2 VDDQ3 VDDQ4 VDDQ5 VDDQ6 VDDQ7 VDDQ8 VDDQ9 VDDQ10 — A1 A9 C1 D9 F2 F8 G1 G9 J2 J8
VDD1 VDD2 VDD3 VDD4 VDD5 VDD6 VDD7 VDD8 VDD9 VDD10 — B3 B9 D1 G7 J1 J9 L1 L9 R1 T9

DDR4
MT40A256M16GE-083E:B
4Gb, 256Mx16b,
1200MHz, 1.2V, 0~95C,
0.833ns@CL=16,
96Ball, 9MMX14MM

MT40A256M16GE-083E IT:B
FBGA96_9MMX14MM_08MM

VSSQ1 VSSQ2 VSSQ3 VSSQ4 VSSQ5 VSSQ6 VSSQ7 VSSQ8 VSSQ9 VSSQ10 — A2 A8 C9 D2 D8 E3 E8 F1 H1 H9
VSS1 VSS2 VSS3 VSS4 VSS5 VSS6 VSS7 VSS8 VSS9 — B2 E1 E9 G8 K1 K9 M9 N1 T1

P1V2_DDR
C732 0.01uF 50V
C734 0.01uF 50V
R717 100
R718 100

P2V5_SYS

ZQ — F9 — R744 240
VREFCA — M1
VPP1 — B1
VPP2 — R9

VPP = (2.375V,2.500V,2.750V)

DQ0	G2	BANK2_DDR4_DQ03	BANK2_DDR4_DQ03 P32
DQ1	F7	BANK2_DDR4_DQ05	BANK2_DDR4_DQ05 P32
DQ2	H3	BANK2_DDR4_DQ02	BANK2_DDR4_DQ02 P32
DQ3	H7	BANK2_DDR4_DQ00	BANK2_DDR4_DQ00 P32
DQ4	H2	BANK2_DDR4_DQ01	BANK2_DDR4_DQ01 P32
DQ5	H8	BANK2_DDR4_DQ07	BANK2_DDR4_DQ07 P32
DQ6	J3	BANK2_DDR4_DQ06	BANK2_DDR4_DQ06 P32
DQ7	J7	BANK2_DDR4_DQ04	BANK2_DDR4_DQ04 P32
DQ8	A3	BANK2_DDR4_DQ13	BANK2_DDR4_DQ13 P32
DQ9	B8	BANK2_DDR4_DQ14	BANK2_DDR4_DQ14 P32
DQ10	C3	BANK2_DDR4_DQ09	BANK2_DDR4_DQ09 P32
DQ11	C7	BANK2_DDR4_DQ08	BANK2_DDR4_DQ08 P32
DQ12	C2	BANK2_DDR4_DQ15	BANK2_DDR4_DQ15 P32
DQ13	C8	BANK2_DDR4_DQ12	BANK2_DDR4_DQ12 P32
DQ14	D3	BANK2_DDR4_DQ11	BANK2_DDR4_DQ11 P32
DQ15	D7	BANK2_DDR4_DQ10	BANK2_DDR4_DQ10 P32
DQSL_T	G3	BANK2_DDR4_DQS0_T	BANK2_DDR4_DQS0_T P32
DQSL_C	F3	BANK2_DDR4_DQS0_C	BANK2_DDR4_DQS0_C P32
DQSU_T	B7	BANK2_DDR4_DQS1_T	BANK2_DDR4_DQS1_T P32
DQSU_C	A7	BANK2_DDR4_DQS1_C	BANK2_DDR4_DQS1_C P32
DML_B/DBIL	E7	BANK2_DDR4_DM0	BANK2_DDR4_DM0 P32
DMU_B/DBIU	E2	BANK2_DDR4_DM1	BANK2_DDR4_DM1 P32

DESIGN NOTES:

Apply power (RESET_n and TEN should be maintained below 0.2×VDD while supplies ramp up.

VPP must ramp at the same time or before VDD (1.2V), and
VPP must be equal to or higher than VDD at all times.

Title: **PG43: DDR4#2 DQ[15:0]**

Size: Custom | Document Number: **SCH-000012-00** | Rev: 04.01

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U54 BYPASS CAPS

P1V2_DDR

C614 0.022UF 6.3V CAP0201_BGA
C585 0.022UF 6.3V CAP0201_BGA
C653 0.022UF 6.3V CAP0201_BGA
C582 0.022UF 6.3V CAP0201_BGA
C870 0.022UF 6.3V CAP0201_BGA
C844 0.022UF 6.3V CAP0201_BGA
C611 0.022UF 6.3V CAP0201_BGA

C766 0.47uF 6.3V CAP0201_BGA
C727 0.47uF 6.3V CAP0201_BGA
C690 0.47uF 6.3V CAP0201_BGA
C864 0.47uF 6.3V CAP0201_BGA
C789 0.47uF 6.3V CAP0201_BGA
C631 0.47uF 6.3V CAP0201_BGA
C842 0.47uF 6.3V CAP0201_BGA

C583 4.7uF 6.3V SMD-0402
C827 4.7uF 6.3V SMD-0402

BANK2 DDR4: MEMORY #2

P1V2_DDR

U60

DDR4
MT40A256M16GE-083E:B
4Gb, 256Mx16b,
1200MHz, 1.2V, 0~95C,
0.833ns@CL=16,
96Ball, 9MMX14MM

P31,43,45,46	BANK2_DDR4_A00	BANK2_DDR4_A00	P3 A0
P31,43,45,46	BANK2_DDR4_A01	BANK2_DDR4_A01	P7 A1
P31,43,45,46	BANK2_DDR4_A02	BANK2_DDR4_A02	R3 A2
P31,43,45,46	BANK2_DDR4_A03	BANK2_DDR4_A03	N7 A3
P31,43,45,46	BANK2_DDR4_A04	BANK2_DDR4_A04	N3 A4
P31,43,45,46	BANK2_DDR4_A05	BANK2_DDR4_A05	P8 A5
P31,43,45,46	BANK2_DDR4_A06	BANK2_DDR4_A06	P2 A6
P31,43,45,46	BANK2_DDR4_A07	BANK2_DDR4_A07	R8 A7
P31,43,45,46	BANK2_DDR4_A08	BANK2_DDR4_A08	R2 A8
P31,43,45,46	BANK2_DDR4_A09	BANK2_DDR4_A09	R7 A9
P31,43,45,46	BANK2_DDR4_A10	BANK2_DDR4_A10	M3 A10/AP
P31,43,45,46	BANK2_DDR4_A11	BANK2_DDR4_A11	T2 A11
P31,43,45,46	BANK2_DDR4_A12	BANK2_DDR4_A12	M7 A12/BC_B
P31,43,45,46	BANK2_DDR4_A13	BANK2_DDR4_A13	T8 A13
			T7 A14/NC
P31,43,45,46	BANK2_DDR4_BA0	BANK2_DDR4_BA0	N2 BA0
P31,43,45,46	BANK2_DDR4_BA1	BANK2_DDR4_BA1	N8 BA1
P31,43,45,46	BANK2_DDR4_BG0	BANK2_DDR4_BG0	M2 BA2/BG0
P31,43,45,46	BANK2_DDR4_CAS_B	BANK2_DDR4_CAS_B	M8 CAS_B/A15
P31,43,45,46	BANK2_DDR4_RAS_B	BANK2_DDR4_RAS_B	L8 RAS_B/A16
P31,43,45,46	BANK2_DDR4_WE_B	BANK2_DDR4_WE_B	L2 WE_B/A14
P31,43,45,46	BANK2_DDR4_CK_T	BANK2_DDR4_CK_T	K7 CK_T
P31,43,45,46	BANK2_DDR4_CK_C	BANK2_DDR4_CK_C	K8 CK_C
P31,43,45,46	BANK2_DDR4_CKE	BANK2_DDR4_CKE	K2 CKE
P31,43,45,46	BANK2_DDR4_ACT_B	BANK2_DDR4_ACT_B	L3 ACT_B
P31,43,45,46	BANK2_DDR4_TEN	BANK2_DDR4_TEN	N9 TEN
P31,43,45,46	BANK2_DDR4_ALERT_B	BANK2_DDR4_ALERT_B	P9 ALERT_B
P31,43,45,46	BANK2_DDR4_PAR	BANK2_DDR4_PAR	T3 PAR
P31,43,45,46	BANK2_DDR4_RESET_B	BANK2_DDR4_RESET_B	P1 RESET_B
P31,43,45,46	BANK2_DDR4_ODT	BANK2_DDR4_ODT	K3 ODT
P31,43,45,46	BANK2_DDR4_CS_B	BANK2_DDR4_CS_B	L7 CS_B

A1 A9 C1 D9 F2 F8 G1 G9 J2 J8 — VDDQ1 VDDQ2 VDDQ3 VDDQ4 VDDQ5 VDDQ6 VDDQ7 VDDQ8 VDDQ9 VDDQ10
B3 B9 D1 G7 J1 J9 L1 L9 R1 T9 — VDD1 VDD2 VDD3 VDD4 VDD5 VDD6 VDD7 VDD8 VDD9 VDD10

ZQ F9 — R765 240 — P1V2_DDR
VREFCA M1 — C834 0.01uF 50V, C837 0.01uF 50V
VPP1 B1 — P2V5_SYS
VPP2 R9

DQ0	G2	BANK2_DDR4_DQ20	BANK2_DDR4_DQ20 P32
DQ1	F7	BANK2_DDR4_DQ23	BANK2_DDR4_DQ23 P32
DQ2	H3	BANK2_DDR4_DQ19	BANK2_DDR4_DQ19 P32
DQ3	H7	BANK2_DDR4_DQ17	BANK2_DDR4_DQ17 P32
DQ4	H2	BANK2_DDR4_DQ22	BANK2_DDR4_DQ22 P32
DQ5	H8	BANK2_DDR4_DQ16	BANK2_DDR4_DQ16 P32
DQ6	J3	BANK2_DDR4_DQ18	BANK2_DDR4_DQ18 P32
DQ7	J7	BANK2_DDR4_DQ21	BANK2_DDR4_DQ21 P32
DQ8	A3	BANK2_DDR4_DQ30	BANK2_DDR4_DQ30 P32
DQ9	B8	BANK2_DDR4_DQ27	BANK2_DDR4_DQ27 P32
DQ10	C3	BANK2_DDR4_DQ24	BANK2_DDR4_DQ24 P32
DQ11	C7	BANK2_DDR4_DQ31	BANK2_DDR4_DQ31 P32
DQ12	C2	BANK2_DDR4_DQ28	BANK2_DDR4_DQ28 P32
DQ13	C8	BANK2_DDR4_DQ25	BANK2_DDR4_DQ25 P32
DQ14	D3	BANK2_DDR4_DQ26	BANK2_DDR4_DQ26 P32
DQ15	D7	BANK2_DDR4_DQ29	BANK2_DDR4_DQ29 P32
DQSL_T	G3	BANK2_DDR4_DQS2_T	BANK2_DDR4_DQS2_T P32
DQSL_C	F3	BANK2_DDR4_DQS2_C	BANK2_DDR4_DQS2_C P32
DQSU_T	B7	BANK2_DDR4_DQS3_T	BANK2_DDR4_DQS3_T P32
DQSU_C	A7	BANK2_DDR4_DQS3_C	BANK2_DDR4_DQS3_C P32
DML_B/DBIL	E7	BANK2_DDR4_DM2	BANK2_DDR4_DM2 P32
DMU_B/DBIU	E2	BANK2_DDR4_DM3	BANK2_DDR4_DM3 P32

A2 A8 C9 D2 D8 E3 E8 F1 H1 H9 — VSSQ1 VSSQ2 VSSQ3 VSSQ4 VSSQ5 VSSQ6 VSSQ7 VSSQ8 VSSQ9 VSSQ10
B2 E1 E9 G8 K1 K9 M9 N1 T1 — VSS1 VSS2 VSS3 VSS4 VSS5 VSS6 VSS7 VSS8 VSS9

MT40A256M16GE-083E IT:B
FBGA96_9MMX14MM_08MM

Title: PG44: DDR4#2 DQ[31:16]
Size: Custom
Document Number: SCH-000012-00
Rev: 04.01
Date: Tuesday, June 19, 2018
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U55 BYPASS CAPS

P1V2_DDR

C786 0.022UF 6.3V CAP0201_BGA
C780 0.022UF 6.3V CAP0201_BGA
C637 0.022UF 6.3V CAP0201_BGA
C875 0.022UF 6.3V CAP0201_BGA
C601 0.022UF 6.3V CAP0201_BGA
C700 0.022UF 6.3V CAP0201_BGA
C729 0.022UF 6.3V CAP0201_BGA

C836 0.47uF 6.3V CAP0201_BGA
C833 0.47uF 6.3V CAP0201_BGA
C825 0.47uF 6.3V CAP0201_BGA
C792 0.47uF 6.3V CAP0201_BGA
C671 0.47uF 6.3V CAP0201_BGA
C698 0.47uF 6.3V CAP0201_BGA
C793 0.47uF 6.3V CAP0201_BGA

C723 4.7uF 6.3V SMD-0402
C638 4.7uF 6.3V SMD-0402

BANK1 DDR4: MEMORY #3

P1V2_DDR
P1V2_DDR
P2V5_SYS

C617 0.01uF 50V
R649 100
C618 0.01uF 50V
R650 100

U47

DDR4
MT40A256M16GE-083E:B
4Gb, 256Mx16b,
1200MHz, 1.2V, 0~95C,
0.833ns@CL=16,
96Ball, 9MMX14MM

P31,43,44,46	BANK2_DDR4_A00	BANK2_DDR4_A00	P3 A0
P31,43,44,46	BANK2_DDR4_A01	BANK2_DDR4_A01	P7 A1
P31,43,44,46	BANK2_DDR4_A02	BANK2_DDR4_A02	R3 A2
P31,43,44,46	BANK2_DDR4_A03	BANK2_DDR4_A03	N7 A3
P31,43,44,46	BANK2_DDR4_A04	BANK2_DDR4_A04	N3 A4
P31,43,44,46	BANK2_DDR4_A05	BANK2_DDR4_A05	P8 A5
P31,43,44,46	BANK2_DDR4_A06	BANK2_DDR4_A06	P2 A6
P31,43,44,46	BANK2_DDR4_A07	BANK2_DDR4_A07	R8 A7
P31,43,44,46	BANK2_DDR4_A08	BANK2_DDR4_A08	R2 A8
P31,43,44,46	BANK2_DDR4_A09	BANK2_DDR4_A09	R7 A9
P31,43,44,46	BANK2_DDR4_A10	BANK2_DDR4_A10	M3 A10/AP
P31,43,44,46	BANK2_DDR4_A11	BANK2_DDR4_A11	T2 A11
P31,43,44,46	BANK2_DDR4_A12	BANK2_DDR4_A12	M7 A12/BC_B
P31,43,44,46	BANK2_DDR4_A13	BANK2_DDR4_A13	T8 A13
			T7 A14/NC
P31,43,44,46	BANK2_DDR4_BA0	BANK2_DDR4_BA0	N2 BA0
P31,43,44,46	BANK2_DDR4_BA1	BANK2_DDR4_BA1	N8 BA1
P31,43,44,46	BANK2_DDR4_BG0	BANK2_DDR4_BG0	M2 BA2/BG0
P31,43,44,46	BANK2_DDR4_CAS_B	BANK2_DDR4_CAS_B	M8 CAS_B/A15
P31,43,44,46	BANK2_DDR4_RAS_B	BANK2_DDR4_RAS_B	L8 RAS_B/A16
P31,43,44,46	BANK2_DDR4_WE_B	BANK2_DDR4_WE_B	L2 WE_B/A14
P31,43,44,46	BANK2_DDR4_CK_T	BANK2_DDR4_CK_T	K7 CK_T
P31,43,44,46	BANK2_DDR4_CK_C	BANK2_DDR4_CK_C	K8 CK_C
P31,43,44,46	BANK2_DDR4_CKE	BANK2_DDR4_CKE	K2 CKE
P31,43,44,46	BANK2_DDR4_ACT_B	BANK2_DDR4_ACT_B	L3 ACT_B
P31,43,44,46	BANK2_DDR4_TEN	BANK2_DDR4_TEN	N9 TEN
P31,43,44,46	BANK2_DDR4_ALERT_B	BANK2_DDR4_ALERT_B	P9 ALERT_B
P31,43,44,46	BANK2_DDR4_PAR	BANK2_DDR4_PAR	T3 PAR
P31,43,44,46	BANK2_DDR4_RESET_B	BANK2_DDR4_RESET_B	P1 RESET_B
P31,43,44,46	BANK2_DDR4_ODT	BANK2_DDR4_ODT	K3 ODT
P31,43,44,46	BANK2_DDR4_CS_B	BANK2_DDR4_CS_B	L7 CS_B

ZQ	F9	R673 240	
VREFCA	M1		
VPP1	B1		
VPP2	R9		
DQ0	G2	BANK2_DDR4_DQ32	BANK2_DDR4_DQ32 P33
DQ1	F7	BANK2_DDR4_DQ34	BANK2_DDR4_DQ34 P33
DQ2	H3	BANK2_DDR4_DQ38	BANK2_DDR4_DQ38 P33
DQ3	H7	BANK2_DDR4_DQ36	BANK2_DDR4_DQ36 P33
DQ4	H2	BANK2_DDR4_DQ37	BANK2_DDR4_DQ37 P33
DQ5	H8	BANK2_DDR4_DQ39	BANK2_DDR4_DQ39 P33
DQ6	J3	BANK2_DDR4_DQ33	BANK2_DDR4_DQ33 P33
DQ7	J7	BANK2_DDR4_DQ35	BANK2_DDR4_DQ35 P33
DQ8	A3	BANK2_DDR4_DQ46	BANK2_DDR4_DQ46 P33
DQ9	B8	BANK2_DDR4_DQ41	BANK2_DDR4_DQ41 P33
DQ10	C3	BANK2_DDR4_DQ40	BANK2_DDR4_DQ40 P33
DQ11	C7	BANK2_DDR4_DQ45	BANK2_DDR4_DQ45 P33
DQ12	C2	BANK2_DDR4_DQ44	BANK2_DDR4_DQ44 P33
DQ13	C8	BANK2_DDR4_DQ42	BANK2_DDR4_DQ42 P33
DQ14	D3	BANK2_DDR4_DQ47	BANK2_DDR4_DQ47 P33
DQ15	D7	BANK2_DDR4_DQ43	BANK2_DDR4_DQ43 P33
DQSL_T	G3	BANK2_DDR4_DQS4_T	BANK2_DDR4_DQS4_T P33
DQSL_C	F3	BANK2_DDR4_DQS4_C	BANK2_DDR4_DQS4_C P33
DQSU_T	B7	BANK2_DDR4_DQS5_T	BANK2_DDR4_DQS5_T P33
DQSU_C	A7	BANK2_DDR4_DQS5_C	BANK2_DDR4_DQS5_C P33
DML_B/DBIL	E7	BANK2_DDR4_DM4	BANK2_DDR4_DM4 P33
DMU_B/DBIU	E2	BANK2_DDR4_DM5	BANK2_DDR4_DM5 P33

VSSQ1 VSSQ2 VSSQ3 VSSQ4 VSSQ5 VSSQ6 VSSQ7 VSSQ8 VSSQ9 VSSQ10
A2 A8 C9 D2 D8 E3 E8 F1 H1 H9

VSS1 VSS2 VSS3 VSS4 VSS5 VSS6 VSS7 VSS8 VSS9
B2 E1 E9 G8 K1 K9 M9 N1 T1

MT40A256M16GE-083E IT:B
FBGA96_9MMX14MM_08MM

Title: **PG45: DDR4#2 DQ[47:32]**

Size: Custom | Document Number: **SCH-000012-00** | Rev: 04.01

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U56 BYPASS CAPS

P1V2_DDR

C636 0.022UF 6.3V CAP0201_BGA
C787 0.022UF 6.3V CAP0201_BGA
C862 0.022UF 6.3V CAP0201_BGA
C635 0.022UF 6.3V CAP0201_BGA
C603 0.022UF 6.3V CAP0201_BGA
C602 0.022UF 6.3V CAP0201_BGA
C574 0.022UF 6.3V CAP0201_BGA

C691 0.47uF 6.3V CAP0201_BGA
C900 0.47uF 6.3V CAP0201_BGA
C903 0.47uF 6.3V CAP0201_BGA
C699 0.47uF 6.3V CAP0201_BGA
C630 0.47uF 6.3V CAP0201_BGA
C830 0.47uF 6.3V CAP0201_BGA
C790 0.47uF 6.3V CAP0201_BGA

C696 4.7uF 6.3V SMD-0402
C632 4.7uF 6.3V SMD-0402

BANK2 DDR4: MEMORY #4

P1V2_DDR

P1V2_DDR
C656 0.01uF 50V
R677 100
C657 0.01uF 50V
R680 100

P2V5_SYS

U51

VDDQ1 A1, VDDQ2 A9, VDDQ3 C1, VDDQ4 D9, VDDQ5 F2, VDDQ6 F8, VDDQ7 G1, VDDQ8 G9, VDDQ9 J2, VDDQ10 J8
VDD1 B3, VDD2 B9, VDD3 D1, VDD4 G7, VDD5 J1, VDD6 J9, VDD7 L1, VDD8 L9, VDD9 R1, VDD10 T9

ZQ F9 — R716 240
VREFCA M1
VPP1 B1
VPP2 R9

DDR4
MT40A256M16GE-083E:B
4Gb, 256Mx16b,
1200MHz, 1.2V, 0~95C,
0.833ns@CL=16,
96Ball, 9MMX14MM

P31,43,44,45 BANK2_DDR4_A00	BANK2_DDR4_A00	P3	A0
P31,43,44,45 BANK2_DDR4_A01	BANK2_DDR4_A01	P7	A1
P31,43,44,45 BANK2_DDR4_A02	BANK2_DDR4_A02	R3	A2
P31,43,44,45 BANK2_DDR4_A03	BANK2_DDR4_A03	N7	A3
P31,43,44,45 BANK2_DDR4_A04	BANK2_DDR4_A04	N3	A4
P31,43,44,45 BANK2_DDR4_A05	BANK2_DDR4_A05	P8	A5
P31,43,44,45 BANK2_DDR4_A06	BANK2_DDR4_A06	P2	A6
P31,43,44,45 BANK2_DDR4_A07	BANK2_DDR4_A07	R8	A7
P31,43,44,45 BANK2_DDR4_A08	BANK2_DDR4_A08	R2	A8
P31,43,44,45 BANK2_DDR4_A09	BANK2_DDR4_A09	R7	A9
P31,43,44,45 BANK2_DDR4_A10	BANK2_DDR4_A10	M3	A10/AP
P31,43,44,45 BANK2_DDR4_A11	BANK2_DDR4_A11	T2	A11
P31,43,44,45 BANK2_DDR4_A12	BANK2_DDR4_A12	M7	A12/BC_B
P31,43,44,45 BANK2_DDR4_A13	BANK2_DDR4_A13	T8	A13
		T7	A14/NC
P31,43,44,45 BANK2_DDR4_BA0	BANK2_DDR4_BA0	N2	BA0
P31,43,44,45 BANK2_DDR4_BA1	BANK2_DDR4_BA1	N8	BA1
P31,43,44,45 BANK2_DDR4_BG0	BANK2_DDR4_BG0	M2	BA2/BG0
P31,43,44,45 BANK2_DDR4_CAS_B	BANK2_DDR4_CAS_B	M8	CAS_B/A15
P31,43,44,45 BANK2_DDR4_RAS_B	BANK2_DDR4_RAS_B	L8	RAS_B/A16
P31,43,44,45 BANK2_DDR4_WE_B	BANK2_DDR4_WE_B	L2	WE_B/A14
P31,43,44,45 BANK2_DDR4_CK_T	BANK2_DDR4_CK_T	K7	CK_T
P31,43,44,45 BANK2_DDR4_CK_C	BANK2_DDR4_CK_C	K8	CK_C
P31,43,44,45 BANK2_DDR4_CKE	BANK2_DDR4_CKE	K2	CKE
P31,43,44,45 BANK2_DDR4_ACT_B	BANK2_DDR4_ACT_B	L3	ACT_B
P31,43,44,45 BANK2_DDR4_TEN	BANK2_DDR4_TEN	N9	TEN
P31,43,44,45 BANK2_DDR4_ALERT_B	BANK2_DDR4_ALERT_B	P9	ALERT_B
P31,43,44,45 BANK2_DDR4_PAR	BANK2_DDR4_PAR	T3	PAR
P31,43,44,45 BANK2_DDR4_RESET_B	BANK2_DDR4_RESET_B	P1	RESET_B
P31,43,44,45 BANK2_DDR4_ODT	BANK2_DDR4_ODT	K3	ODT
P31,43,44,45 BANK2_DDR4_CS_B	BANK2_DDR4_CS_B	L7	CS_B

DQ0	G2	BANK2_DDR4_DQ52	BANK2_DDR4_DQ52 P33
DQ1	F7	BANK2_DDR4_DQ50	BANK2_DDR4_DQ50 P33
DQ2	H3	BANK2_DDR4_DQ55	BANK2_DDR4_DQ55 P33
DQ3	H7	BANK2_DDR4_DQ49	BANK2_DDR4_DQ49 P33
DQ4	H2	BANK2_DDR4_DQ51	BANK2_DDR4_DQ51 P33
DQ5	H8	BANK2_DDR4_DQ48	BANK2_DDR4_DQ48 P33
DQ6	J3	BANK2_DDR4_DQ53	BANK2_DDR4_DQ53 P33
DQ7	J7	BANK2_DDR4_DQ54	BANK2_DDR4_DQ54 P33
DQ8	A3	BANK2_DDR4_DQ60	BANK2_DDR4_DQ60 P33
DQ9	B8	BANK2_DDR4_DQ56	BANK2_DDR4_DQ56 P33
DQ10	C3	BANK2_DDR4_DQ63	BANK2_DDR4_DQ63 P33
DQ11	C7	BANK2_DDR4_DQ62	BANK2_DDR4_DQ62 P33
DQ12	C2	BANK2_DDR4_DQ61	BANK2_DDR4_DQ61 P33
DQ13	C8	BANK2_DDR4_DQ57	BANK2_DDR4_DQ57 P33
DQ14	D3	BANK2_DDR4_DQ59	BANK2_DDR4_DQ59 P33
DQ15	D7	BANK2_DDR4_DQ58	BANK2_DDR4_DQ58 P33
DQSL_T	G3	BANK2_DDR4_DQS6_T	BANK2_DDR4_DQS6_T P33
DQSL_C	F3	BANK2_DDR4_DQS6_C	BANK2_DDR4_DQS6_C P33
DQSU_T	B7	BANK2_DDR4_DQS7_T	BANK2_DDR4_DQS7_T P33
DQSU_C	A7	BANK2_DDR4_DQS7_C	BANK2_DDR4_DQS7_C P33
DML_B/DBIL	E7	BANK2_DDR4_DM6	BANK2_DDR4_DM6 P33
DMU_B/DBIU	E2	BANK2_DDR4_DM7	BANK2_DDR4_DM7 P33

VSSQ1 A2, VSSQ2 A8, VSSQ3 C9, VSSQ4 D2, VSSQ5 D8, VSSQ6 E3, VSSQ7 E8, VSSQ8 F1, VSSQ9 H1, VSSQ10 H9
VSS1 B2, VSS2 E1, VSS3 E9, VSS4 G8, VSS5 K1, VSS6 K9, VSS7 M9, VSS8 N1, VSS9 T1

MT40A256M16GE-083E IT:B
FBGA96_9MMX14MM_08MM

Title: **PG44: DDR4#2 DQ[63:48]**
Size: Custom
Document Number: **SCH-000012-00**
Rev: 04.01
Date: Tuesday, June 19, 2018
Sheet 46 of 55

PHY ADD: 001

EC1 = 001 ==> PD + R50 + R53
EC2 = 011 ==> PD + R56 + R57
EC3 = 111 ==> PU + R188 + R191

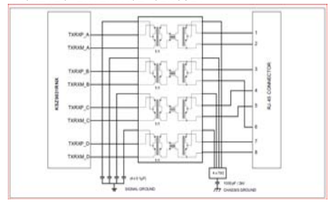
RX_CLK - PHYAD2 - 35 ==> R421 (add 10K PD)
E_LED2 - PHYAD1 - 15 ==> R50 = 0; R52 = X
E_LED1 - PHYAD0 - 17 ==> R53 = X; R51 = 1

LAYOUT NOTE:
Trace length match

DESIGN NOTES (CLK125 MHz)
CLK125_EN PIN 33
0 Disable 125MHz clock
1 Enable 125MHz clock

DESIGN NOTES (MODE)
1111 ==> RGMII
All capabilities (10/100/1000)
Speed: half/full duplex

KSZ9031RNXIA
MAGNETIC INTERFACE CIRCUIT



J18
SS71800-027F

EC1_MX1_P
EC1_MX1_N
EC1_MX2_P PIN3
EC1_MX3_P
EC1_MX3_N
EC1_MX2_N PIN6
EC1_MX4_P
EC1_MX4_N
CGND9
CGND10
SS71800-027F

U75
KSZ9031RNXIA
QFN-48_7MMX7MM_05MM_PAD

EC1

MDC
MDIO
TXD3
TXD2
TXD1
TXD0
TX_CLK
TX_CTL
RXD3
RXD2
RXD1
RXD0
RX_CLK
RX_CTL
XI
XO
CLK125_NDO
RESET_N
ISET
AVDDL_PLL
AVDDH1
AVDDH0
AVDDL1
AVDDL0
NC1
NC0
TXRXP_A
TXRXM_A
TXRXP_B
TXRXM_B
TXRXP_C
TXRXM_C
TXRXP_D
TXRXM_D
INT_N / PME_N2
LED1 / PME_N1
LED2
LDO_O
DVDDH2
DVDDH1
DVDDH0
DVDDL5
DVDDL4
DVDDL3
DVDDL2
DVDDL1
DVDDL0
VSS
P_GND

MODE0
MODE1
MODE2
MODE3
EC1_RX_CLK
PULL-UP: ENABLE CLK125

EC1_XI
EC1_XO
EC1_CLK125_SRC
EC1_RESET_N
EC1_ISET
EC1_TXRXA_P
EC1_TXRXA_N
EC1_TXRXB_P
EC1_TXRXB_M
EC1_TXRXC_P
EC1_TXRXC_M
EC1_TXRXD_P
EC1_TXRXD_M
EC1_INT_N
EC1_LED1
EC1_LED2

GIGA ETHERNET
DIFFERENTIAL PAIRS
100 OHMS IMPEDENCE

U8
HX5008NL
HX5008NL24_18_67MM_13_16MM_0_99MM

TCT1
TD1_P
TD1_N
TCT2
TD2_P
TD2_N
TCT3
TD3_P
TD3_N
TCT4
TD4_P
TD4_N
MCT1
MX1_P
MX1_N
MCT2
MX2_P
MX2_N
MCT3
MX3_P
MX3_N
MCT4
MX4_P
MX4_N

EC1_MCT1
EC1_MCT2
EC1_MCT3
EC1_MCT4
EC1_MX1_P
EC1_MX1_N
EC1_MX2_P PIN3
EC1_MX2_N PIN6
EC1_MX3_P
EC1_MX3_N
EC1_MX4_P
EC1_MX4_N

HX5008NL
AUTO TRANSFORMER
-40C ~ 85C

P19,48,49 LS1021A_EC123_MDC
P19,48,49 LS1021A_EC123_MDIO
P19 LS1021A_EC1_TXD3
P19 LS1021A_EC1_TXD2
P19 LS1021A_EC1_TXD1
P19 LS1021A_EC1_TXD0
P19 LS1021A_EC1_TX_CLK
P19 LS1021A_EC1_TX_EN
P19 LS1021A_EC1_RXD3
P19 LS1021A_EC1_RXD2
P19 LS1021A_EC1_RXD1
P19 LS1021A_EC1_RXD0
P19 LS1021A_EC1_RX_CLK
P19 LS1021A_EC1_RX_DV
P19 LS1021A_EC1_CLK125
P20,48,49 LS1021A_EC_RESET_N

P1V8_ARM
P1V2_DDR
P3V3_SYS

R421 33.0
R60 33.0
R404 0
R406 3.32K
R53 DNI
R50 3.32K
R51
R52
R405 3.32K
R407 3.32K
R836 DNI
R837 10K
R49 12.1K
R373 75
R372 75
R382 75
R383 75

C237 1000pF 2kV

C53 0.01uF 50V
C52 0.01uF 50V
C26 0.1UF 16V
C54 22uF 10V
C57 0.01uF 50V
C25 0.01uF 50V
C27 0.01uF 50V
C55 0.01uF 50V
C29 0.01uF 50V
C56 22uF 10V

FB6 600 OHM BLM15AG601SN1D
C19 10uF 6.3V
C17 0.1UF 16V
C16 0.01uF 50V
EC1_P1V2_AVDDPLL

FB3 600 OHM BLM15AG601SN1D
C11 22uF 10V
C20 0.1UF 16V
C24 0.01uF 50V
C28 0.01uF 50V
EC1_P3V3_AVDDH

FB2 600 OHM BLM15AG601SN1D
C23 10uF 6.3V
C21 0.1UF 16V
C22 0.01uF 50V
EC1_P1V2_AVDDL

Y2
EC1_XO
EC1_XI
C256 22PF 50V
C255 22PF 50V
DFN4_2MMX16MM
ABM11-25.000MHZ-D2X
25.000 MHz

C249 0.1uF 50V
C248 0.1uF 50V
C236 0.1uF 50V
C235 0.1uF 50V

R347 100.0K
R5 243
R355 100.0K
R16 243

D32 GREEN TLMG1100-GS08
D31 GREEN TLMG1100-GS08
EC1_LED2_ANODE
EC1_LED2_CATH
EC1_LED1_ANODE
EC1_LED1_CATH

SINGLE LED MODE	
LED2	1: LINK OFF
LED1	BLINK: ACTIVE

U74
SN74LVC1G07DCKR
SC-70-5
EC1_LED1 P34
EC1_LED1
EC1_LED1_CATH
OPEN DRAIN
C30 0.01uF 50V

U72
SN74LVC1G07DCKR
SC-70-5
EC1_LED2 P34
EC1_LED2
EC1_LED2_CATH
OPEN DRAIN
C31 0.01uF 50V

R65 DNI
R64 DNI
R63 DNI
R62 DNI
R61 DNI

R416 3.32K
R417 3.32K
R418 3.32K
R419 3.32K
R420 3.32K
R69 1.0K
R67 1.0K
R90 1.0K
R91 1.0K
R68 1.0K
R89 1.0K

Title
PG47: MAC PHY with EC1

Size: Custom
Document Number: **SCH-000012-00**
Rev: 04.01

Date: Tuesday, June 19, 2018
Sheet 47 of 55

PHY ADD: 011

LAYOUT NOTE:
Trace length match

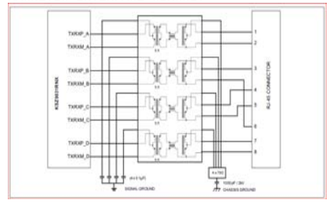
DESIGN NOTES (CLK125 MHz)
CLK125_EN PIN 33
0 Disable 125MHz clock
1 Enable 125MHz clock

DESIGN NOTES (MODE)
1111 ==> RGMII
All capabilities (10/100/1000)
Speed: half/full duplex

EC1 = 001 ==> PD + R50 + R53
EC2 = 011 ==> PD + R56 + R57
EC3 = 111 ==> PU + R188 + R191

RX_CLK - PHYAD2 - 35 ==> R839 = 0
E_LED2 - PHYAD1 - 15 ==> R58 = X; R56 = 1
E_LED1 - PHYAD0 - 17 ==> R55 = X; R57 = 1

KSZ9031RNXIA
MAGNETIC INTERFACE CIRCUIT



J17
SS71800-027F

EC2_MX1_P
EC2_MX1_N
EC2_MX2_P_PIN3
EC2_MX3_P
EC2_MX3_N
EC2_MX2_N_PIN6
EC2_MX4_P
EC2_MX4_N

U71
KSZ9031RNXIA
EC2

QFN-48_7MMX7MM_05MM_PAD

U9
HX5008NL
HX5008NL24_18_67MM_13_16MM_0_99MM
HX5008NL
AUTO TRANSFORMER
-40C ~ 85C

GIGA ETHERNET
DIFFERENTIAL PAIRS
100 OHMS IMPEDENCE

Y1
DFN4_2MMX16MM
ABM11-25.000MHZ-D2X
25.000 MHz

U70
SN74LVC1G07DCKR
U69
SN74LVC1G07DCKR
SC-70-5

SINGLE LED MODE	
LED2	1: LINK OFF
LED1	BLINK: ACTIVE

Title		
PG48: MAC PHY with EC2		
Size: Custom	Document Number: SCH-000012-00	Rev: 04.0
Date: Tuesday, June 19, 2018	Sheet 48 of 55	

PHY ADD: 111

DESIGN NOTES (CLK125 MHz)
CLK125_EN PIN 33
0 Disable 125MHz clock
1 Enable 125MHz clock

DESIGN NOTES (MODE)
1111 ==> RGMII
All capabilities (10/100/1000)
Speed: half/full duplex

LAYOUT NOTE:
Trace length match

EC1 = 001 ==> PD + R50 + R53
EC2 = 011 ==> PD + R56 + R57
EC3 = 111 ==> PU + R188 + R191

RX_CLK - PHYAD2 - 35 ==> R580
E_LED2 - PHYAD1 - 15 ==> R187 = X; R188 = 1
E_LED1 - PHYAD0 - 17 ==> R190 = X; R191 = 1

U81
KSZ9031RNXIA
EC3
QFN-48_7MMX7MM_05MM_PAD

U36
HX5008NL
HX5008NL24_18_67MM_13_16MM_0_99MM
HX5008NL
AUTO TRANSFORMER
-40C ~ 85C

GIGA ETHERNET
DIFFERENTIAL PAIRS
100 OHMS IMPEDENCE

DESIGN NOTES (During bring-up)
RESET_N must be pulsed, otherwise the
125MHz clock will not be active.

Y3
DFN4_2MMX16MM
ABM11-25.000MHZ-D2X
25.000 MHz

SINGLE LED MODE	
LED2	1: LINK OFF
LED1	BLINK: ACTIVE

KSZ9031RNXIA
MAGNETIC INTERFACE CIRCUIT

U79
SN74LVC1G07DCKR
SC-70-5

U80
SN74LVC1G07DCKR
SC-70-5

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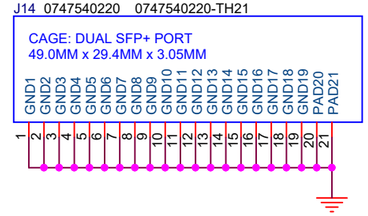
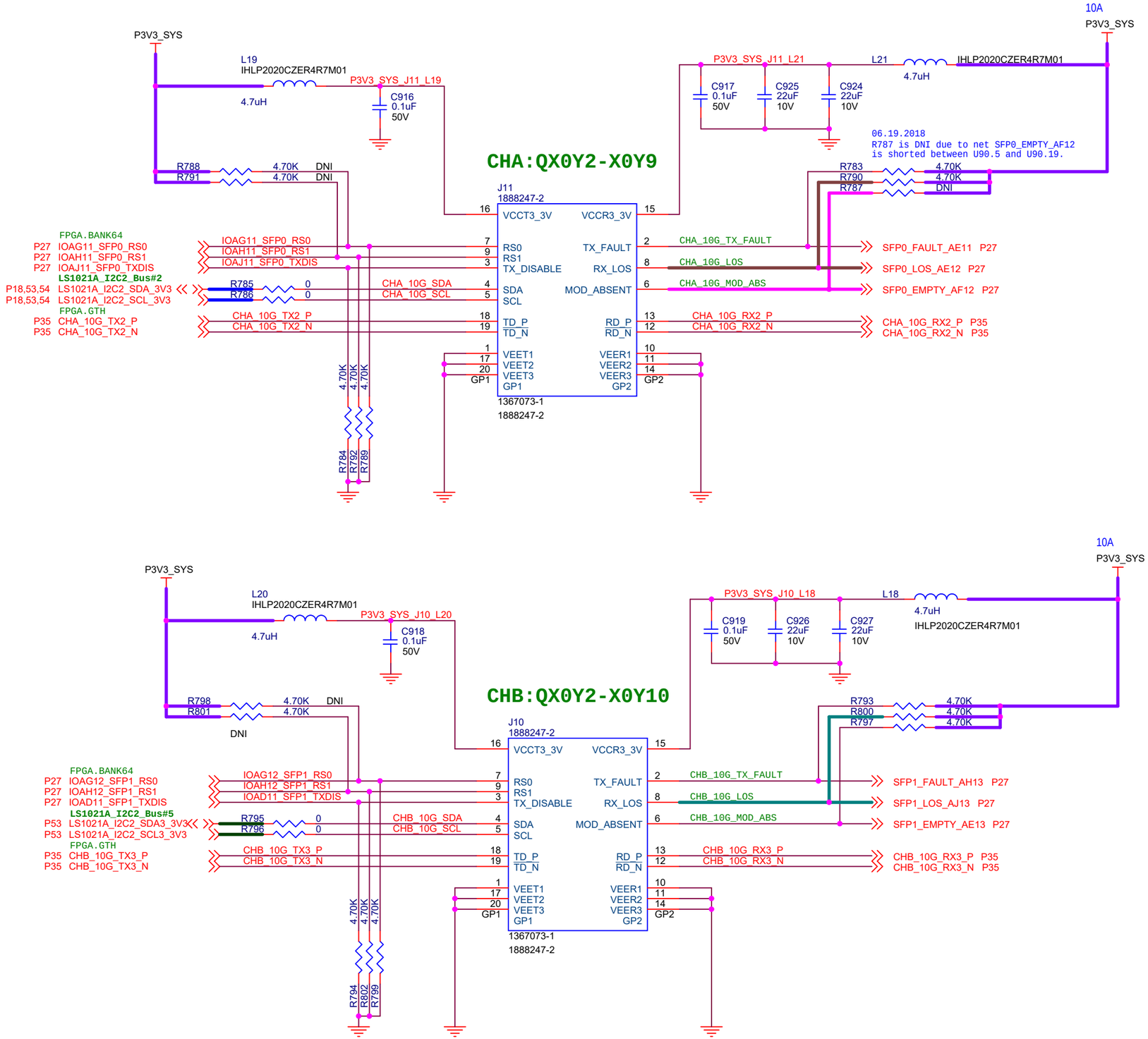
Title: PG49: MAC PHY with EC3
Size: Custom
Document Number: SCH-000012-00
Rev: 04.01
Date: Tuesday, June 19, 2018
Sheet 49 of 55

DUAL 10GE SFP CAGE





Title: PG50: 10GE SFP+		
Size: Custom	Document Number: SCH-000012-00	Rev: 04.01
Date: Tuesday, June 19, 2018	Sheet 50 of 55	

LS1021A - 100MHz Differential Clocks

100MHz LVDS

P3V3_SYS

C312 1.0uF 10V
C313 1.0nF 25V
R442 4.70K

U14
511BCA100M000BAG
R443 DNI
Si510
R444 0
NC, VCC, CLK_P, CLK_N, OE, GND
XO_5MMX3_2MMX1_28MM
100.0000 MHZ

OSC_100M_P
R98 100
OSC_100M_N

P1V8_FPGA

U15
8P34S1106NLGI
VDD5 (5), VDD11 (11), VDD20 (20)
C357 0.022uF 10V
C311 0.1UF 16V
C310 10uF 10V

CLK_P (6), CLK_N (7)
VREF (8)
NC (4)
GND EP (1, 21)
VFQFN20-EP_4MMX4MM_0_5MM

Q0_P (9) / Q0_N (10)	CLK0_100M_P / CLK0_100M_N	CLK0R_100M_P P35 / CLK0R_100M_N P35	FPGA PCIE REF CLOCK
Q1_P (12) / Q1_N (13)	CLK1_100M_P C72 0.01uF 16V / CLK1_100M_N C73 0.01uF 16V	CLK1R_100M_P P17 / CLK1R_100M_N P17	LS1021A's PCIE SD1_REF1_CLK SD1_REF2_CLK
Q2_P (14) / Q2_N (15)	CLK2_100M_P C74 0.01uF 16V / CLK2_100M_N C75 0.01uF 16V	CLK2R_100M_P P17 / CLK2R_100M_N P17	
Q3_P (16) / Q3_N (17)	CLK3_100M_P / CLK3_100M_N	CLK3R_100M_P P20 / CLK3R_100M_N P20	LS1021A SYSDIF+/-
Q4_P (18) / Q4_N (19)	CLK4_100M_P / CLK4_100M_N		
Q5_P (2) / Q5_N (3)	CLK5_100M_P R100 49.9 / CLK5_100M_N R99 49.9	CLK5R_100M_P P34 / CLK5R_100M_N P34	

NEED TO CHECK THE LS1021A's INPUT TERMINATION REQUIREMENTS ????

DESIGN NOTES (511BCA100M000BAG)
511: LVPECL,LVDS,HCSL,Dual CMOS
B: Power = 3.3V. Output format = LVDS
C: ±30ppm
A: OE Active high
100M000: 100MHz
B: 3.2x5mm
AG: -40°C to 85°C

DESIGN NOTES (8P34S1106)
Io = 10mA (Isurge = 15mA)
Vod = 350mV
Vcm = 1.23V

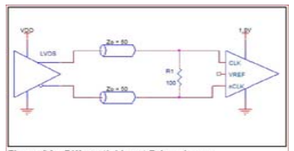


Figure 2A. Differential Input Driven by an LVDS Driver - DC Coupling

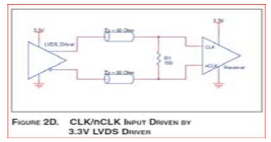


Figure 2D. CLK/nCLK Input Driven by 3.3V LVDS Driver

P3V3_SYS
C309 1.0uF 10V
C308 1.0nF 25V
P1V8_FPGA
C355 1.0uF 10V
C356 1.0nF 25V

LVDS/LVCOMS

U17
83026BGI-01LFT
VDD (1), CLK (2), CLK# (3), OE (4), VDDO (8), Q0 (7), Q1 (6), GND (5)
R842 22.0
R843 22.0
CLK1_CMOS_100M P20
CLK2_CMOS_100M P20
TSSOP8_3MMX6_4MM_0_65MM

R425 = 0
P3V3_SYS
R425 0
R426 DNI
R426 = DNI

DESIGN NOTES:
LS1021A is configured as single differential clock input mode

Alternative Part 530BC200M000DG

200MHz LVDS

P3V3_SYS

C914 1.0uF 10V
C915 1.0nF 25V
R810 4.70K

U62
531BC200M000DG
R811 DNI
Si510
R812 0
NC, VCC, CLK_P, CLK_N, OE, GND
OSC-7MM_5MM_6
200MHz

Replaced with High Q, Low Loss caps by ATC

CLK1_200M_P / CLK1_200M_N	C195 0.01uF 16V / C194 0.01uF 16V	CLK1_200MC_P P35 / CLK1_200MC_N P35	

FPGA - 11.3G MGTREFCLK

LVDS
Trise/fall = 350ps(min)/800ps(max)
Vcm = 1.23v
Vpp = 760mV

DESIGN NOTES (531BC200M000DG)
6-pad, 5 x 7 mm package
LVPECL,LVDS,HCSL,Dual CMOS
530: OE on pin 2
531: OE on pin 1
B: Power = 3.3V. Output format = LVDS
531 C: ±07ppm OverTemp / ±20ppm Total Stability.
511 C: ±20ppm OverTemp / ±30ppm Total Stability.
A: OE Active high
200M000: 200MHz / 156M250: 156.25MHz
D: Revision
G: -40°C to 85°C

From NXP FAE:
This possibly caused by the configuration from CW:
LS1021A (0 0x9b) (0x1000 1)
In this configuration, we used
DDR_REFCLK_SEL=2'b00

P1V2_DDR
1.0K R333 R331
1.0K R334 R332
CLK1_300MC_P P28
CLK1_300MC_N P28

LAYOUT NOTE:
100 Ohm Diff

LAYOUT NOTE:
PLACE THESE 4 BIAS RESISTORS AT THE FPGA

P1V8_FPGA
C928 1.0uF 10V
C929 1.0nF 25V

U65
8P34S1102NLGI
VDD (5), Q0 (9), Q0# (10), CLK (6), CLK# (7), Q1 (11), Q1# (12), VREF (8), GND01 (1), GND16 (16), EP (17)
NC02 (2), NC03 (3), NC04 (4), NC13 (13), NC14 (14), NC15 (15)
VFQFN16_EP_3MMX3MM_0_50MM

CLK1_300M_P C200 0.01uF 16V / CLK1_300M_N C199 0.01uF 16V		
CLK2_300M_P C198 0.01uF 16V / CLK2_300M_N C197 0.01uF 16V		

P1V2_DDR
1.0K R329 R327
1.0K R330 R328
CLK2_300MC_P P31
CLK2_300MC_N P31

LAYOUT NOTE:
100 Ohm Diff

LAYOUT NOTE:
PLACE THESE 4 BIAS RESISTORS AT THE FPGA

FPGA - DDR4 MIG CLOCKS

300MHz LVDS

P3V3_SYS

C930 1.0uF 10V
C931 1.0nF 25V
R817 4.70K

U66
591BB300M000DG
R816 DNI
Si510
R825 0
NC, VCC, CLK_P, CLK_N, OE, GND
XO_7MMX5MMX1_8MM
300.0000 MHZ

OSC_300M_P
OSC_300M_N

591BB: 3.3V,LVDS,50ppm
Vcm = 1.2V
Vpp = 0.7V

FPGA - 10GE MGTREFCLK

531BC156M250DG

156.25MHz LVDS

P3V3_SYS

C921 1.0uF 10V
C920 1.0nF 25V
R815 4.70K

U85
531BC156M250DG
R814 DNI
Si510
R813 0
NC, VCC, CLK_P, CLK_N, OE, GND
OSC-7MM_5MM_6
156.2500MHZ

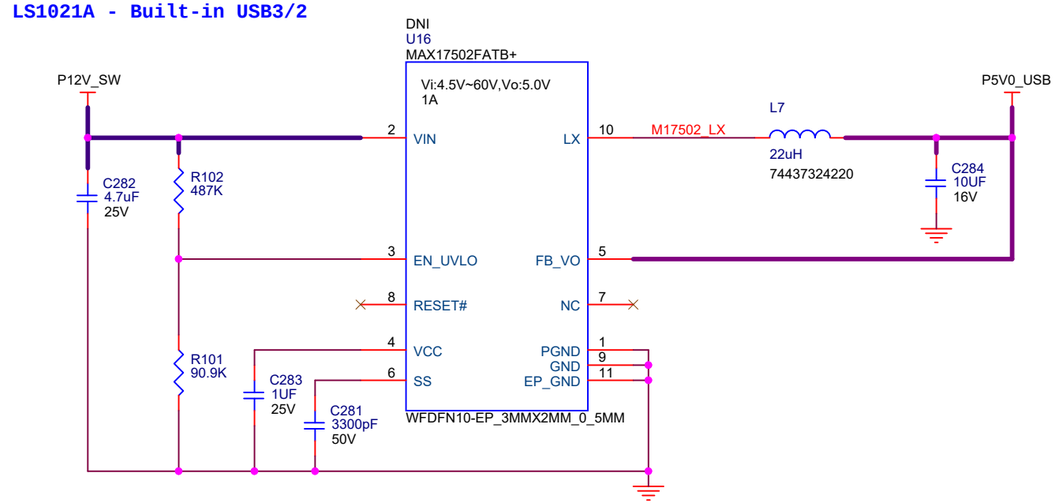
Replaced with High Q, Low Loss caps by ATC

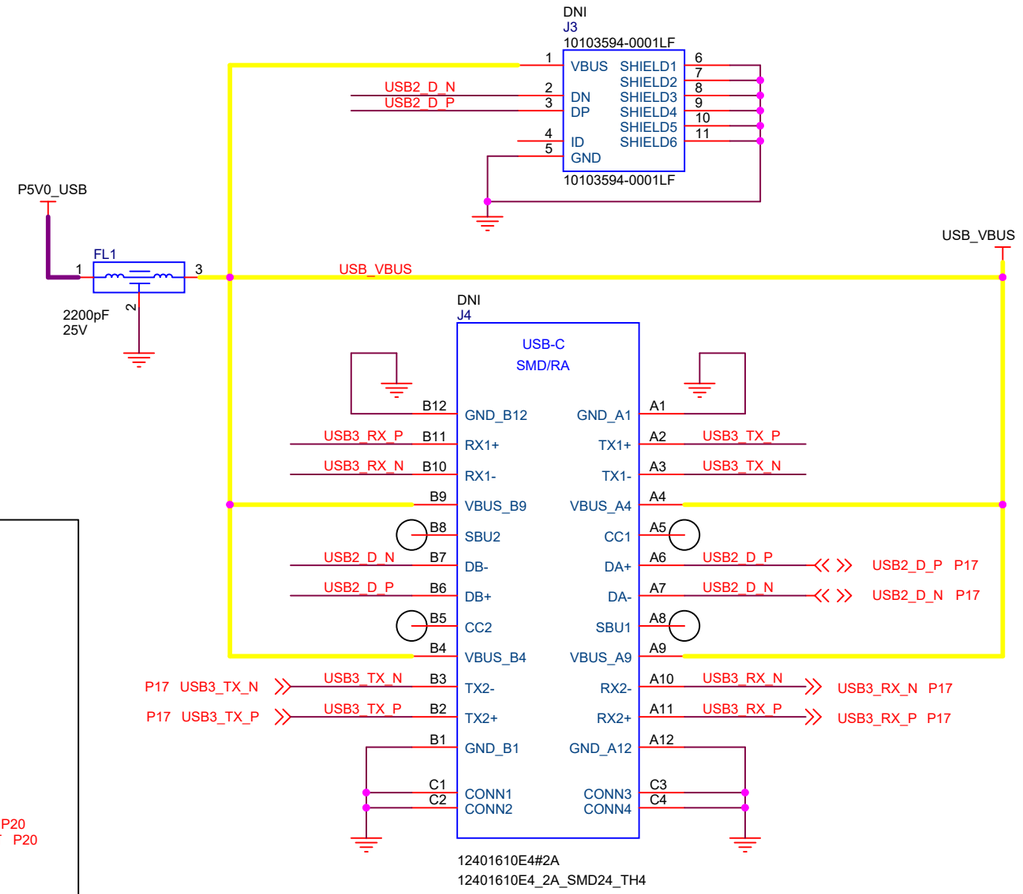
CLK2_156M_P / CLK2_156M_N	C923 0.01uF 16V / C922 0.01uF 16V	CLK2_156MC_P P35 / CLK2_156MC_N P35	

LVDS
Trise/fall = 350ps(min)/800ps(max)
Vcm = 1.23v
Vpp = 760mV

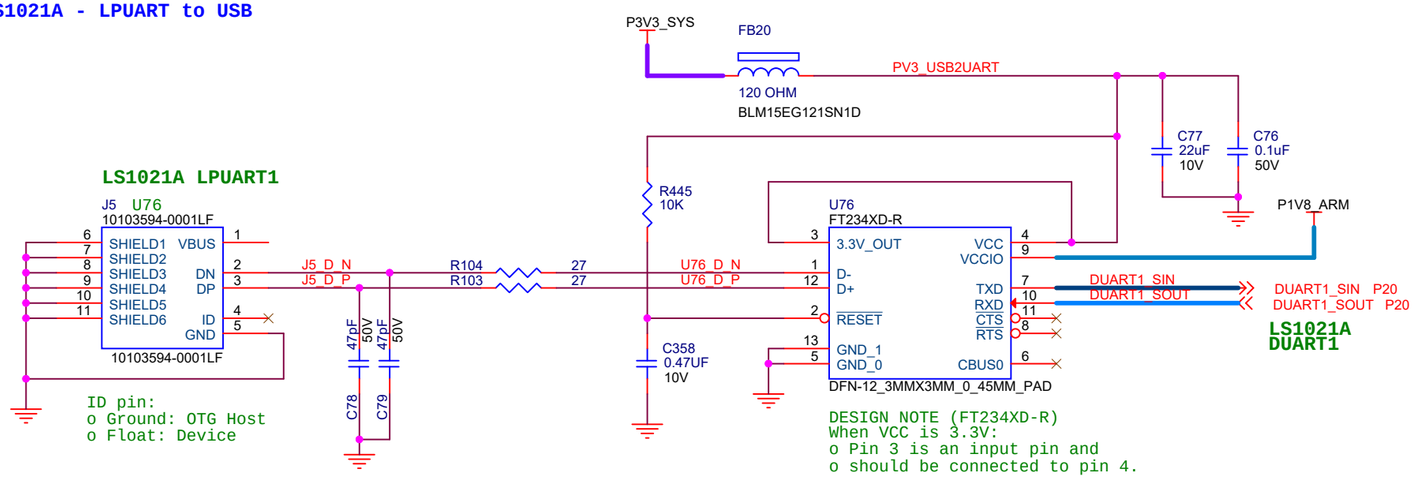
Title: **PG51: CLOCK OSCILLATORS**
Size: Custom
Document Number: **SCH-000012-00**
Rev: 04.01
Date: Tuesday, June 19, 2018
Sheet 51 of 55

LS1021A - Built-in USB3/2

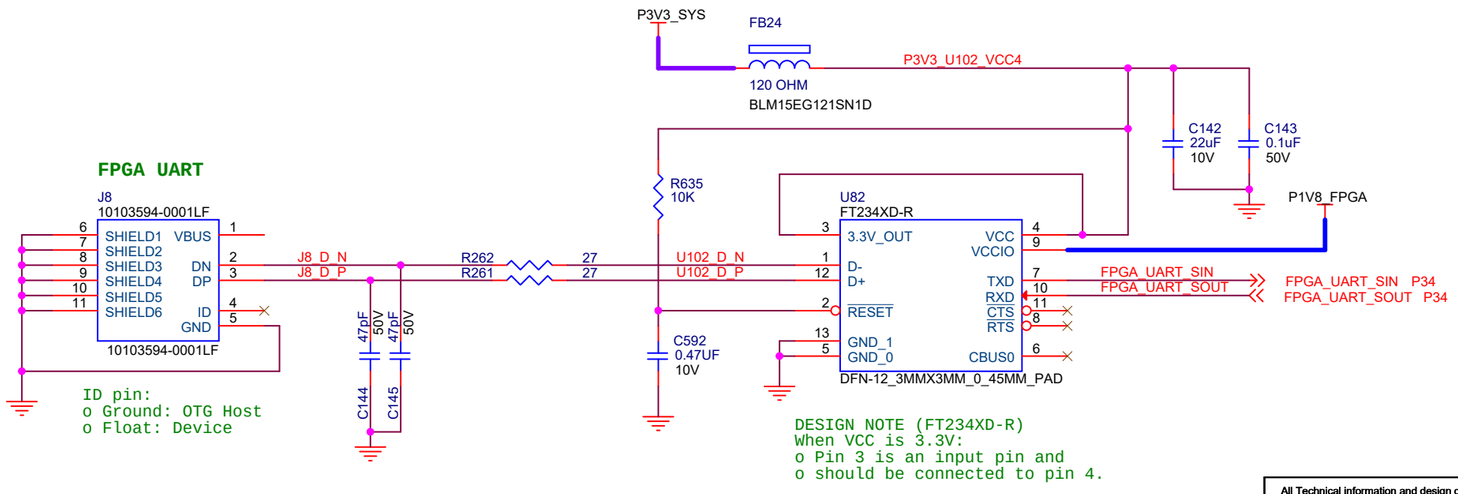




LS1021A - LPUART to USB



FPGA's UART



Title	PG52: USB/UART AND USB3	
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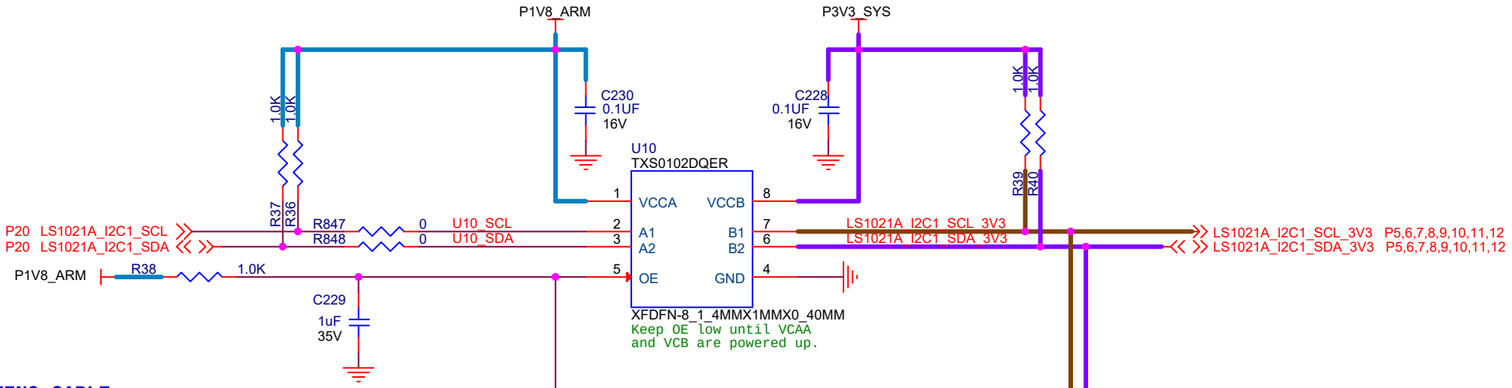
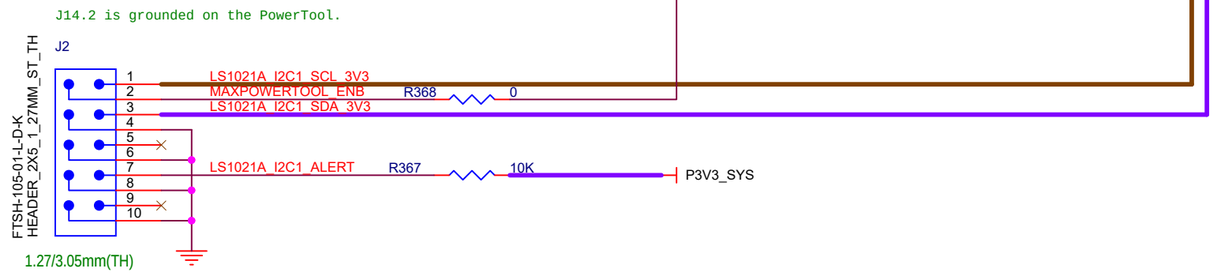
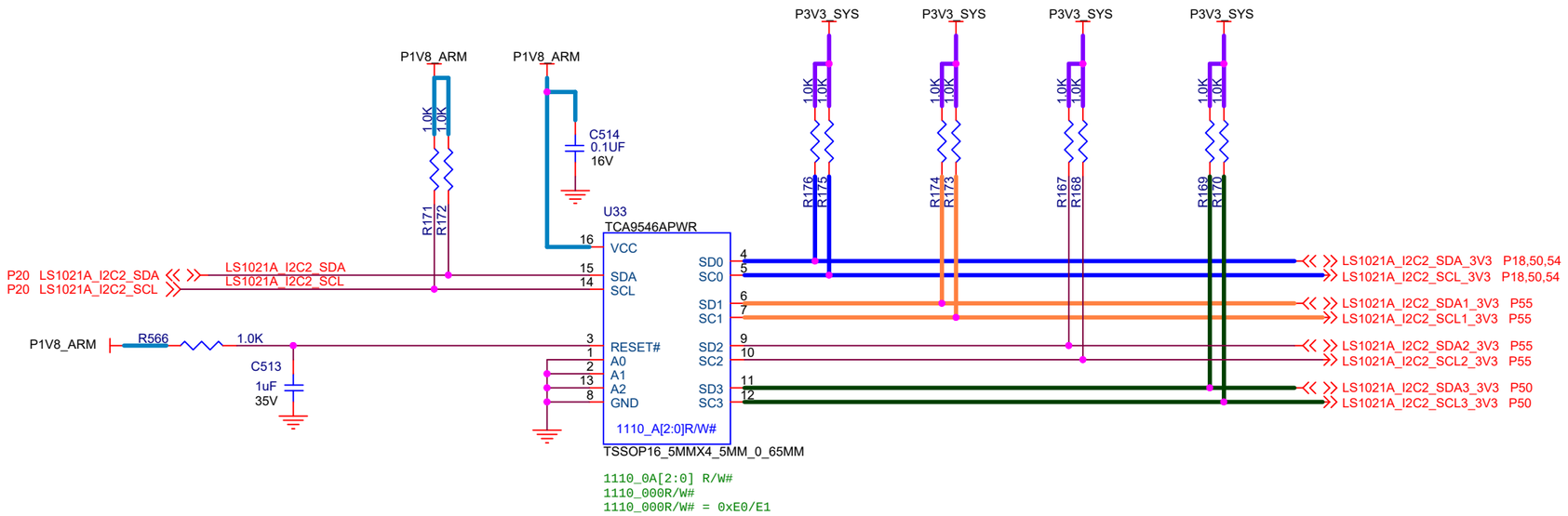
LS1021A - I2C



MAXIM PMBUS PROGRAMMING CABLE



DESIGN NOTES (PowerTools)
The PowerTool header is 16 pins, but only 4 pins
plus GNDs are used. The rest is N.C.
This design uses small 10-pin header via an adapter board.



1110_0A[2:0] R/W#
1110_000R/W#
1110_000R/W# = 0xE0/E1

Title: **PG53: I2C VOLTAGE TRANSLATORS**
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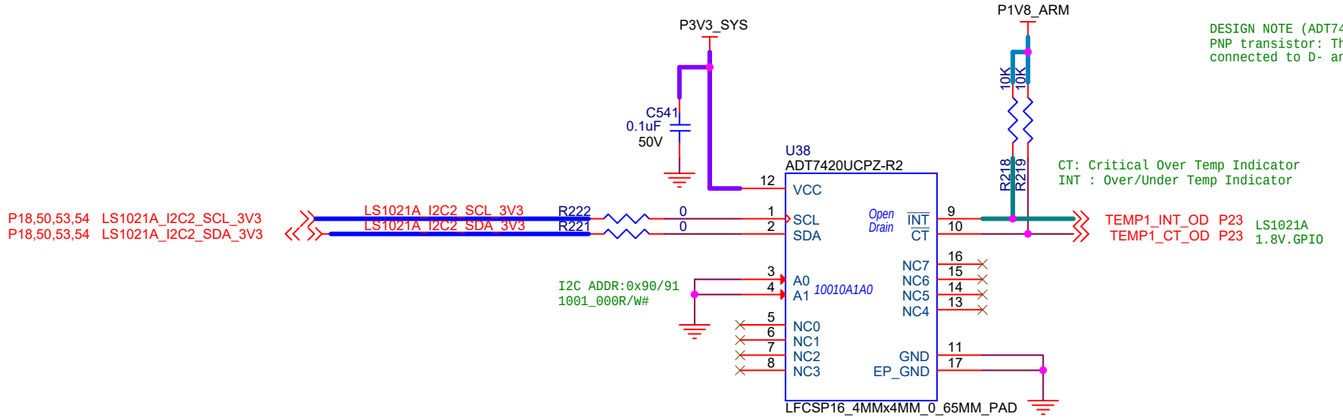
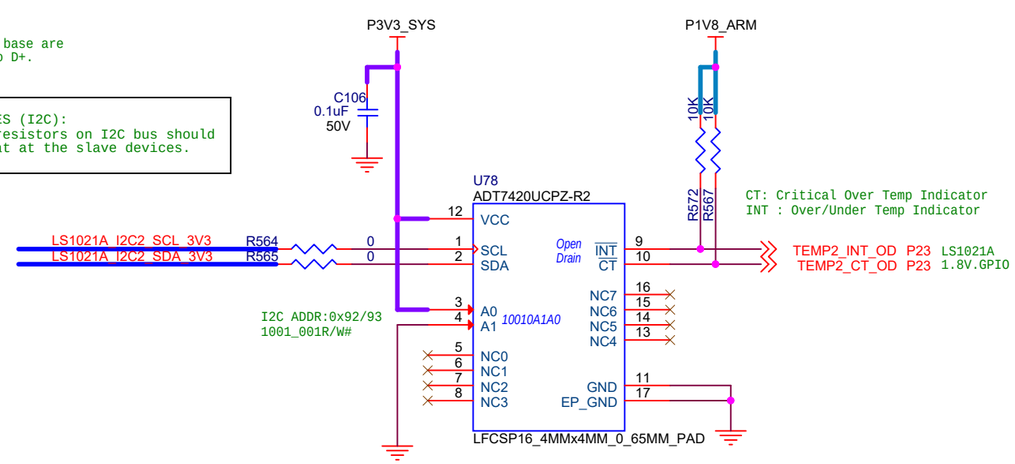
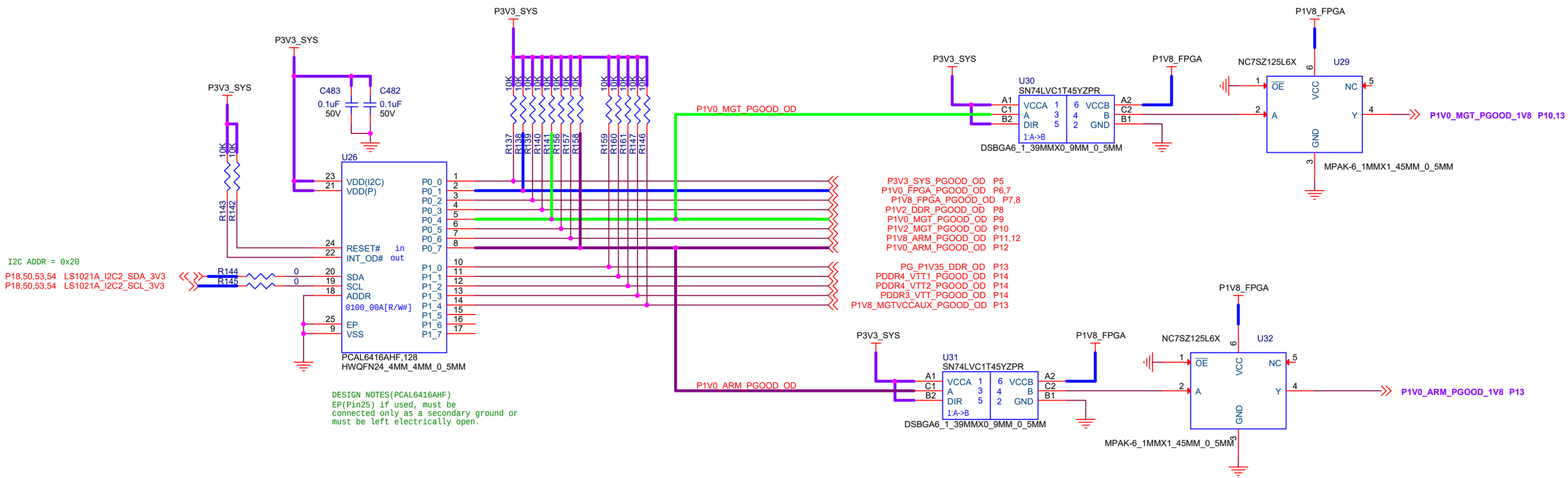


DESIGN NOTE (ADT7461ARMZ-R7)
PNP transistor: The collector and base are connected to D- and the emitter to D+.

LAYOUT NOTES (I2C):
All 0 Ohm resistors on I2C bus should be placed at at the slave devices.





P3V3_SYS_PGOOD_OD P5
P1V0_FPGA_PGOOD_OD P6,7
P1V8_FPGA_PGOOD_OD P7,8
P1V2_DDR_PGOOD_OD P8
P1V0_MGT_PGOOD_OD P9
P1V2_MGT_PGOOD_OD P10
P1V8_ARM_PGOOD_OD P11,12
P1V0_ARM_PGOOD_OD P12

PG_P1V35_DDR_OD P13
PDDR4_VTT1_PGOOD_OD P14
PDDR4_VTT2_PGOOD_OD P14
PDDR3_VTT_PGOOD_OD P14
P1V8_MGTVCCAUX_PGOOD_OD P13

DESIGN NOTES(PCAL6416AHF)
EP(Pin25) if used, must be connected only as a secondary ground or must be left electrically open.

Title
PG54: I2C#2: TEMP SENSORS AND PGOODS

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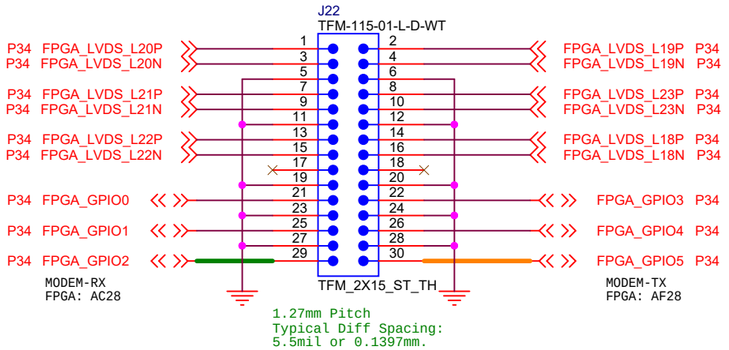
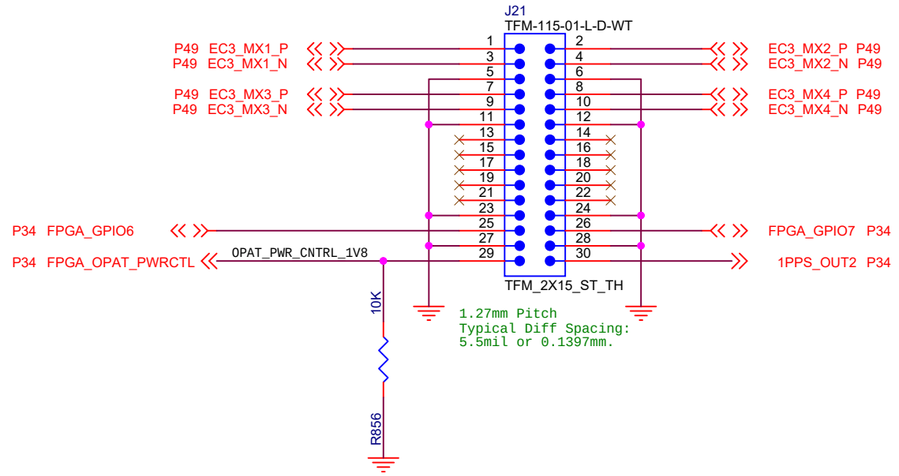
J22 (J9 on OPAT BOARD)
OPAT BOARD: LVDS/GPIO

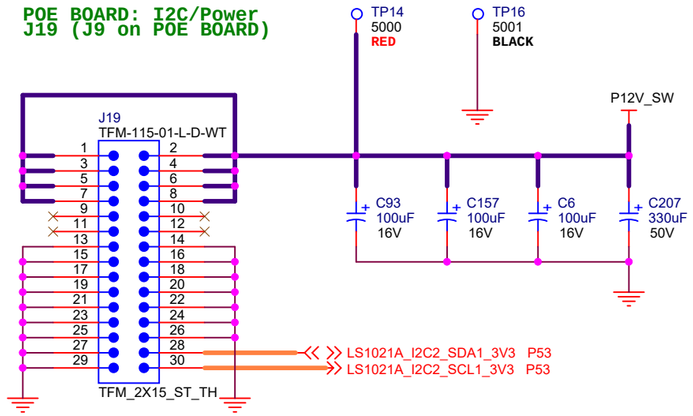


TP22 TP13 TP4 TP17 TP1 TP20 TP8 TP2 TP5 TP10 TP9 TP18 TP15 TP21 TP3 TP19

J21 (J7 on OPAT BOARD)
OPAT BOARD: RGMII/GPIO



POE BOARD: I2C/Power
J19 (J9 on POE BOARD)



FD7 FD1 FD5 FD4 FD2 FD3 FD9 FD8 FD10 FD6

NON-PLATED MOUNTING HOLES WITH FOOTPRINTS = NPTH_1457H_3013P

BOARD/CHASSIS MOUNTING HOLES

MTG17 MTG13 MTG10 MTG4 MTG1 MTG2 MTG3 MTG7 MTG16 MTG19 MTG18

PLATED MOUNTING HOLES WITH FOOTPRINTS = PTH_146H_315P.

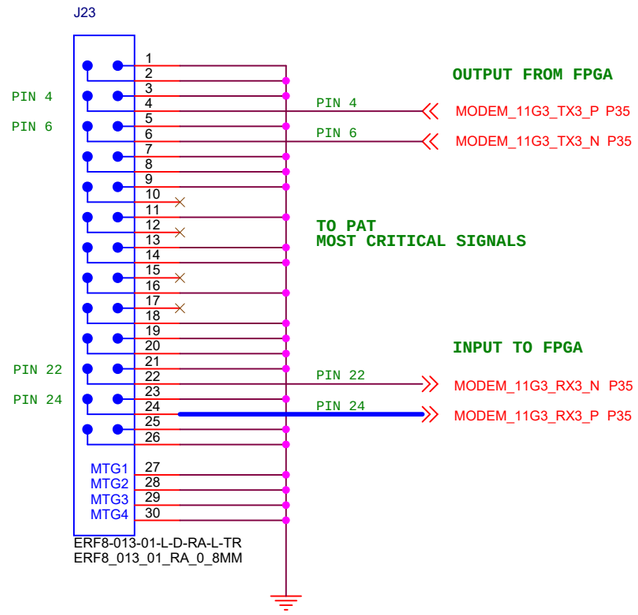
FPGA MOUTING HOLES

MTG14 MTG11 MTG15 MTG12

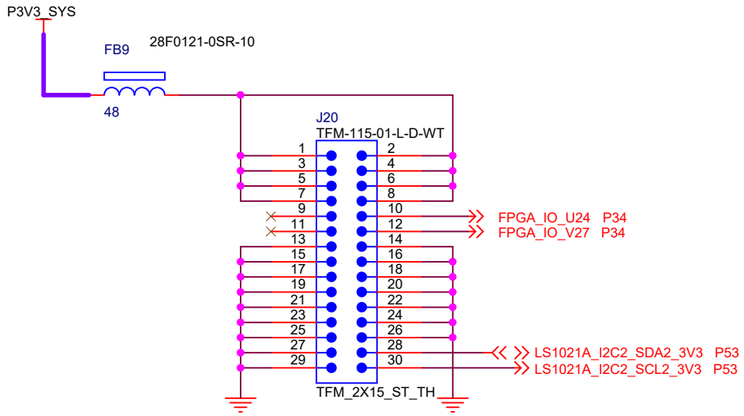
LS1021A MOUNTING HOLES

MTG8 MTG5 MTG9 MTG6

J23 (J8 on OPAT BOARD)
OPAT BOARD: 11.3G
EDGE CONN



J20 (J1 on DISPLAY BOARD)
LED/DISPLAY BOARD



Title	PG55: INTER-BOARD CONN	
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