AM62A STARTER KIT EVM

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VER	0.15

Designed for TI by Mistral Solutions Pvt Ltd

TEXAS INSTRUMENTS

MISTRAL

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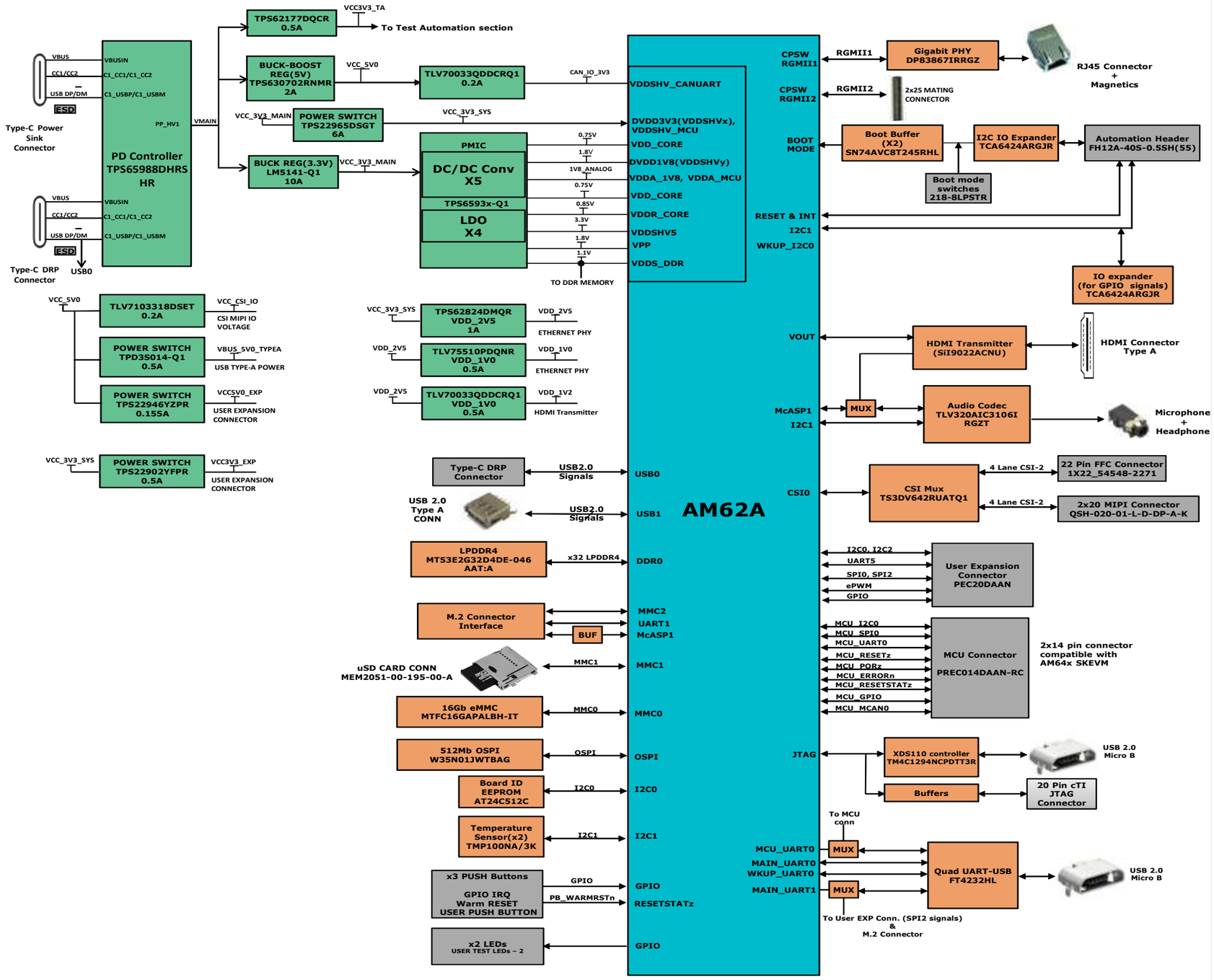
REVISION HISTORY

VER #	DATE	DESCRIPTION OF CHANGES	AUTHOR	REVIEWED BY	APPROVED BY
0.01	21 MARCH 2022	Initial Draft	Mistral Design Team		
0.02	30 MARCH 2022	Updated CSI , LPDDR4 & PD CONTROLLER SECTION	Mistral Design Team		
0.03	14 APR 2022	Updated PMIC section	Mistral Design Team		
0.04	02 MAY 2022	Updated Internal Review comments	Mistral Design Team		
0.05	04 MAY 2022	Updated SoC Decaps & CSI FET connections for routing ease	Mistral Design Team		
0.06	09 MAY 2022	Updated PMIC section	Mistral Design Team		
0.07	10 MAY 2022	Net swapping in OSPI and HDMI groups of signals	Mistral Design Team		
0.08	11 MAY 2022	Updated Power supply-2 (VCC_3V3_MAIN) section with new regulator, replaced RGMII2 PHY section for accomodating ethernet ADD-ON boards(Industrial and Automotive PHY based)	Mistral Design Team		
0.09	12 MAY 2022	Added Matting Connectors for ADD-ON boards and main board Updated power achitecture and I2C tree digrams	Mistral Design Team		
0.10	12 MAY 2022	Added Matting Connectors for ADD-ON boards and main board	Mistral Design Team		
0.11	13 MAY 2022	Added 3T caps for VDD_LPDDR4 SOC power rail	Mistral Design Team		
0.12	16 MAY 2022	TI Review Comments implemented	Mistral Design Team		
0.13	18 MAY 2022	Updated single port PD controller to Dual PD to match software requirements	Mistral Design Team		
0.14	19 MAY 2022	Separated RGMII Add On Boards to individual schematics	Mistral Design Team		
0.15	24 MAY 2022	Updated PMIC GPIO connections as per TI review comments	Mistral Design Team		

BLOCK DIAGRAM AM62A-SKEVM



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Title	BLOCK DIAGRAM AM62A_ SKEVM	
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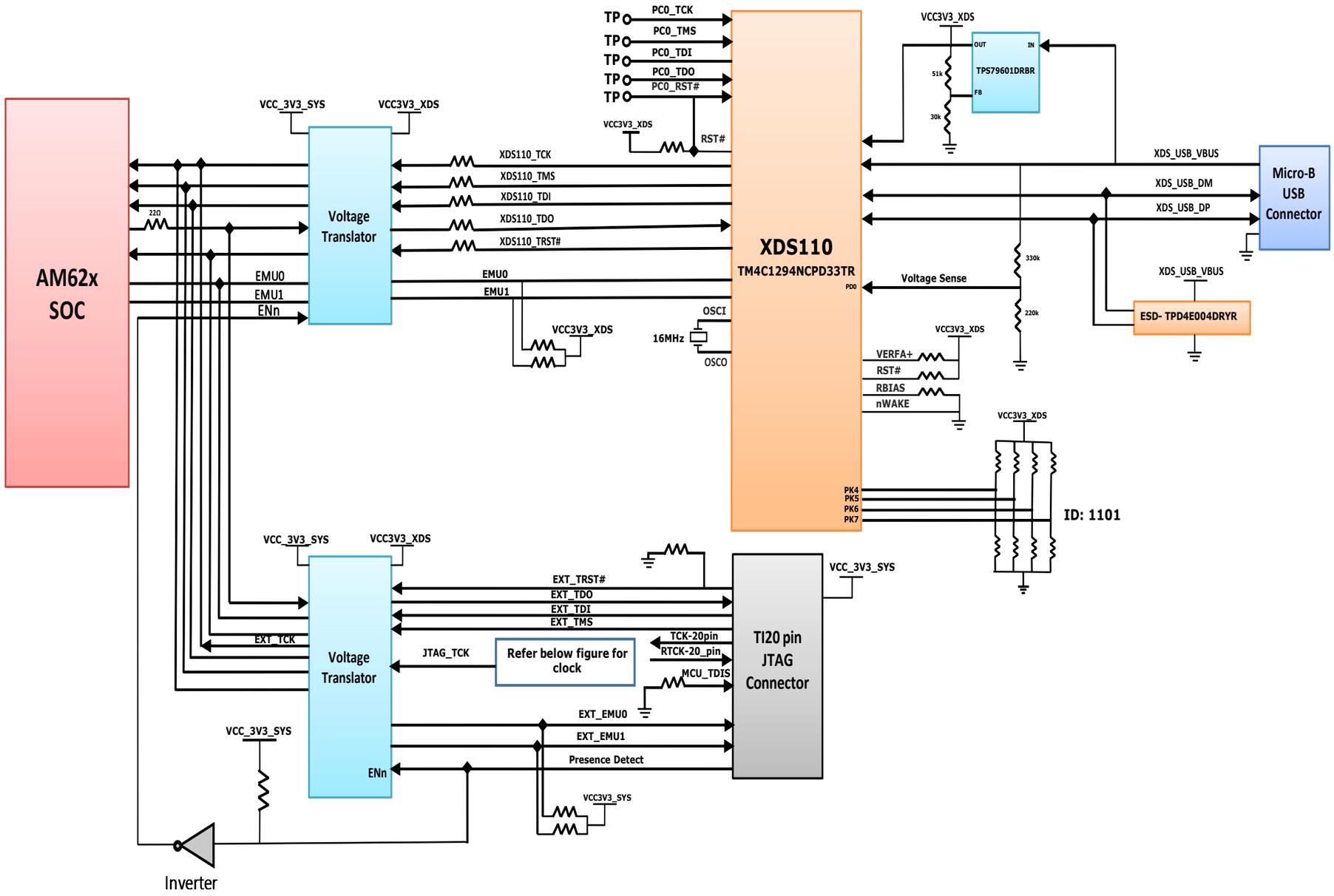
BLOCK DIAGRAM_XDS110



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Title	BLOCK DIAGRAM_XDS110		
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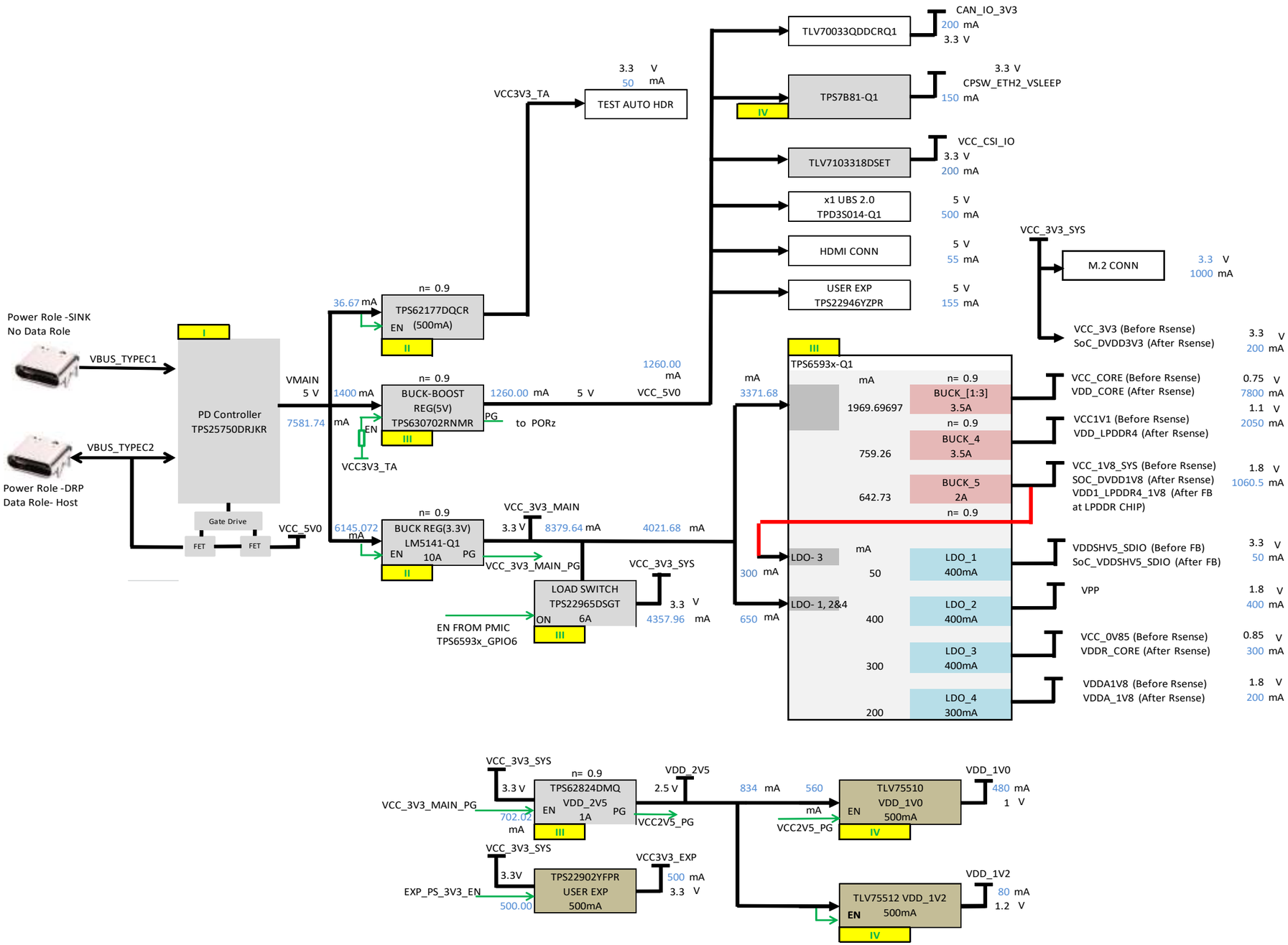
POWER BLOCK DGM



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Title	POWER BLOCK DGM		
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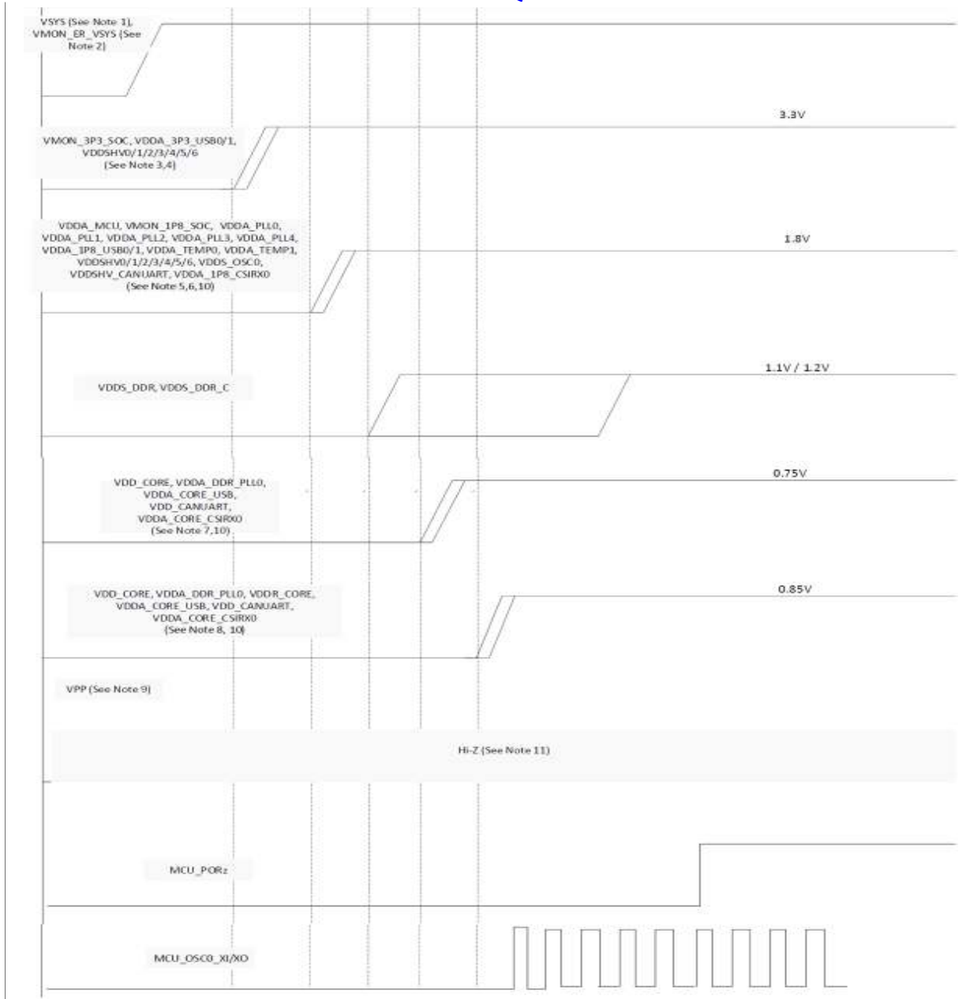
POWER SEQUENCE



Notes:

1. VSYS represents the name of a supply which sources power to the entire system. This supply is expected to be a pre-regulated supply that sources power management devices which source all other supplies.
2. VMON_ER_VSYS input is used to monitor VSYS via an external resistor divider circuit. For more information, see Section 7.3.4, System Power Supply Monitor Design Guidelines.
3. VDDSHV_MCU and VDDSHVx [x=0-6] are dual voltage IO supplies which can be operated at 1.8V or 3.3V depending on the application requirements. When any of the VDDSHV_MCU or VDDSHVx [x=0-6] IO supplies are operating at 3.3V, they shall be ramped up with other 3.3V supplies during the 3.3V ramp period defined by this waveform.
4. The VMON_3P3_SOC input is used to monitor supply voltage and shall be connected to the respective 3.3V supply source.
5. VDDSHV_MCU and VDDSHVx [x=0-6] are dual voltage IO supplies which can be operated at 1.8V or 3.3V depending on the application requirements. When any of the VDDSHV_MCU or VDDSHVx [x=0-6] IO supplies are operating at 1.8V, they shall be ramped up with other 1.8V supplies during the 1.8V ramp period defined by this waveform.
6. The VMON_1P8_SOC input is used to monitor supply voltage and shall be connected to the respective 1.8V supply source.
7. VDD_CORE, VDDA_DDR_PLL0, VDD_CANUART, VDDA_CORE_USB, and VDDA_CORE_CSIRX0 can be operate at 0.75V or 0.85V. When VDD_CORE is operating at 0.75V then VDDA_DDR_PLL0, VDD_CANUART, VDDA_CORE_USB0/1, and VDDA_CORE_CSIRX0 shall also operate 0.75V and shall be ramped up prior to all 0.85V supplies as shown in this waveform.
8. VDD_CORE, VDDA_DDR_PLL0, VDD_CANUART, VDDA_CORE_USB, and VDDA_CORE_CSIRX0 can be operated at 0.75V or 0.85V. When VDD_CORE is operating at 0.85V then VDDA_DDR_PLL0, VDD_CANUART, VDDA_CORE_USB, and VDDA_CORE_CSIRX0 shall also operate at 0.85V and shall be ramped up with other 0.85V supplies during the 0.85V ramp period defined by this waveform.
9. VPP is the 1.8V eFuse programming supply, which shall be left floating (HiZ) or grounded during power-up/down sequences and during normal device operation. This supply shall only be sourced while programming eFuse.
10. VDDA_CORE_CSIRX0 and VDDA_1P8_CSIRX0 are analog supplies that for the CSI DPHY. If CSI is not used then these supplies may be shorted to ground.

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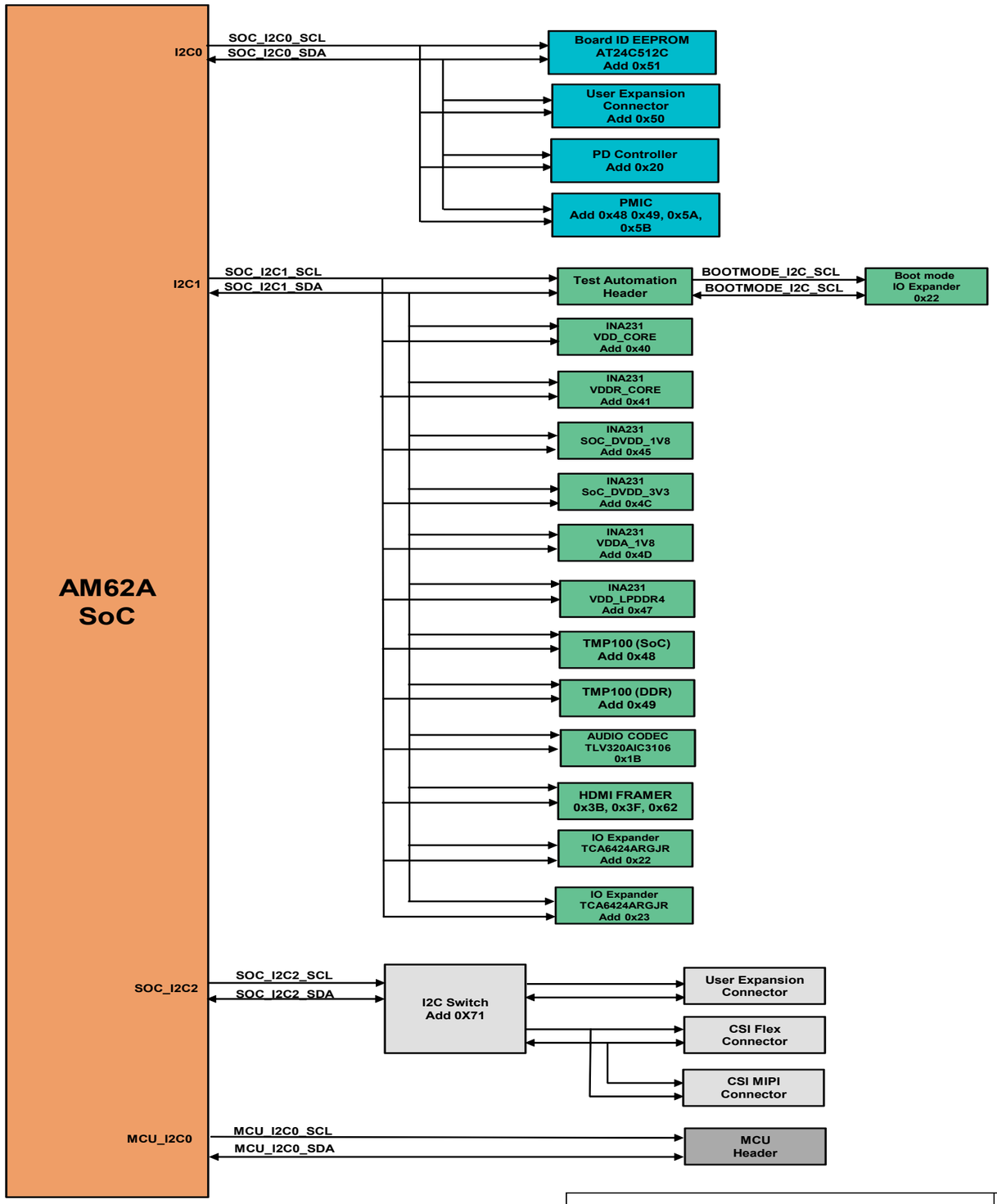
I2C TREE



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Title	I2C TREE		
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GPIO MAPPING TABLE

SL NO.	GPIO DESCRIPTION	GPIO NETNAME	FUNCTIONALITY	GPIO USED	PACKAGE SIGNAL NAME	DIRECTION WITH RESPECT TO CONTROL	DEFAULT STATE	ACTIVE STATE	VOLTAGE DOMAIN ON SOC SIDE	VOLTAGE RAIL CONNECTED ON SKEVM
1	Enable for WLAN Interface	WLAN_EN	ENABLE	GPIO0_71	MMC2_SDCD	OUTPUT	LOW	HIGH	VDDSHV6	SoC_DVDD1V8
2	WLAN Interrupt	WLAN_IRQ	INTERRUPT	GPIO0_72	MMC2_SDWP	INPUT	HIGH	LOW	VDDSHV6	SoC_DVDD1V8
3	Enable for BT Interface	BT_EN_SOC	ENABLE	MCU_GPIO0_0	MCU_SPI0_CS0	OUTPUT	LOW	HIGH	VDDSHV_MCU	SoC_DVDD3V3
4	CPSW Ethernet PHY Interrupt	CPSW_RGMII_INTn	INTERRUPT	GPIO1_31	EXTINTn	INPUT	HIGH	LOW	VDDSHV0	SoC_DVDD3V3
5	OSPI Reset Control GPIO	GPIO_OSPI_RSTn	RESET	GPIO0_12	OSPI0_CSn1	OUTPUT	HIGH	LOW	VDDSHV1	SoC_DVDD1V8
6	MCU Header GPIO0_16	MCU_GPIO0_16	GPIO	MCU_GPIO0_16	MCU_MCAN1_RX	NA	NA	NA	VDDSHV_CANUART	CAN_IO_3V3
7	MCU Header GPIO0_15	MCU_GPIO0_15	GPIO	MCU_GPIO0_15	MCU_MCAN1_TX	NA	NA	NA	VDDSHV_CANUART	CAN_IO_3V3
8	PMIC Interrupt	PMIC_INT_B	INTERRUPT	GPIO0_31	EXTINTn	INPUT	HIGH	LOW	VDDSHV3	SoC_DVDD3V3
9	CAN-FD fast wake up signal from switch	CAN_FD_WKUP_SW_INH	INTERRUPT	MCU_GPIO0_15	MCU_MCAN1_TX	INPUT	HIGH	LOW	VDDSHV_CANUART	CAN_IO_3V3
10	CAN-FD fast wake signal from MCU header	CAN_FD_WKUP_HDR_INH								
11	Interrupt signal from Automotive Ethernet ADD-ON board	CPSW_ETH2_INH								
12	User test LED control signal	SOC_GPIO1_49	GPIO	GPIO1_49	MMC1_SDWP	OUTPUT	LOW	HIGH	VDDSHV0	SoC_DVDD3V3
13	Watchdog trigger input signal for Watchdog Trigger mode	PMIC_WDOG_TRIGG	ENABLE	MCU_GPIO0_19	WKUP_I2C0_SCL	INPUT	LOW	HIGH	VDDSHV_MCU	SoC_DVDD3V3
14	WKUP Signal from RGMII2	CPSW_ETH2_WAKE	INTERRUPT	MCU_GPIO0_20	WKUP_I2C0_SDA	INPUT	LOW	HIGH	VDDSHV_MCU	SoC_DVDD3V3
15	User EXP Conn GPIO	EXP_GPIO1_22	GPIO	GPIO1_22	UART0_CTSn	NA	NA	NA	VDDSHV0	SoC_DVDD3V3
16	IO Expander Interrupt	GPIO1_23_INTn	INTERRUPT	GPIO1_23	UART0_RTSn	INPUT	HIGH	LOW	VDDSHV0	SoC_DVDD3V3
17	User Interrupt									
18	User EXP Conn GPIO	EXP_GPIO0_14_LT	GPIO	GPIO0_14	OSPI0_CSn3	NA	NA	NA	VDDSHV1	SoC_DVDD1V8
19	PMIC Standby Disable	PMIC_LPM_EN0	ENABLE	MCU_GPIO0_22	PMIC_LPM_EN0	OUTPUT	LOW	HIGH	VDDSHV_CANUART	CAN_IO_3V3
20	User EXP Conn GPIO	EXP_EHRPWM1_B	GPIO	GPIO1_10	MCASP0_AXR0	NA	NA	NA	VDDSHV0	SoC_DVDD3V3
	IO EXPANDER - 01									
1	eMMC Reset control GPIO	GPIO_EMMC_RSTN	RESET	IO EXPANDER-P11		OUTPUT	HIGH	LOW		VCC_3V3_SYS
2	CPSW Ethernet PHY-1 Reset Control GPIO	GPIO_CPSW1_RST	RESET	IO EXPANDER-P01		OUTPUT	HIGH	LOW		VCC_3V3_SYS
3	CPSW Ethernet PHY-2 Reset Control GPIO	GPIO_CPSW2_RST	RESET	IO EXPANDER-P00		OUTPUT	HIGH	LOW		VCC_3V3_SYS
4	SD Card Load Switch Enable	MMC1_SD_EN	ENABLE	IO EXPANDER-P03		OUTPUT	HIGH	LOW		VCC_3V3_SYS
5	SOC eFuse Voltage(VPP=1.8V) Regulator Enable	VPP_EN	ENABLE	IO EXPANDER-P04		OUTPUT	LOW	HIGH		VCC_3V3_SYS
6	EXP CONN 3.3V Power Switch Enable	EXP_PS_3V3_EN	ENABLE	IO EXPANDER-P05		OUTPUT	LOW	HIGH		VCC_3V3_SYS
7	EXP CONN 5V Power Switch Enable	EXP_PS_5V0_EN	ENABLE	IO EXPANDER-P06		OUTPUT	LOW	HIGH		VCC_3V3_SYS
8	Audio Codec Reset Control GPIO	GPIO_AUD_RSTN	RESET	IO EXPANDER-P10		OUTPUT	HIGH	LOW		VCC_3V3_SYS
9	EXP CONN HAT Board Detection	EXP_HAT_DETECT	DETECTION	IO EXPANDER-P07		INPUT	HIGH	LOW		VCC_3V3_SYS
10	SOC UART1 Mux Select	UART1_FET_BUF_EN	SELECT	IO EXPANDER-P12		OUTPUT	HIGH	LOW		VCC_3V3_SYS
11	BT UART WKUP Signal	BT_UART_WAKE_SOC	INTERRUPT	IO EXPANDER-P13		INPUT	HIGH	LOW		VCC_3V3_SYS
12	HDMI Transmitter Reset Control GPIO	GPIO_HDMI_RSTN	RESET	IO EXPANDER-P14		OUTPUT	HIGH	LOW		VCC_3V3_SYS
13	Raspberry Pi Camera CSI0 GPIO1	CSI_GPIO0	INPUT/OUTPUT	IO EXPANDER-P15		NA	NA	NA		VCC_3V3_SYS
14	Raspberry Pi Camera CSI0 GPIO2	CSI_GPIO1	INPUT/OUTPUT	IO EXPANDER-P16		NA	NA	NA		VCC_3V3_SYS
15	WLAN Alert Interrupt	WLAN_ALERTn	INTERRUPT	IO EXPANDER-P17		INPUT	LOW	HIGH		VCC_3V3_SYS
16	HDMI Interrupt	HDMI_INTN	INTERRUPT	IO EXPANDER-P20		INPUT	HIGH	LOW		VCC_3V3_SYS
17	TEST GPIO2 from Test Automation Connector	TEST_GPIO2	GPIO	IO EXPANDER-P21		INPUT	HIGH	LOW		VCC_3V3_SYS
18	MCASP1 Enable and Direction Control	MCASP1_FET_EN	ENABLE	IO EXPANDER-P22		OUTPUT	LOW	LOW		VCC_3V3_SYS
19		MCASP1_BUF_BT_EN	ENABLE	IO EXPANDER-P23		OUTPUT	LOW	HIGH		VCC_3V3_SYS
20		MCASP1_FET_SEL	DIRECTION CONTROL	IO EXPANDER-P24		OUTPUT	HIGH	LOW		VCC_3V3_SYS
21		UART1_FET_SEL	DIRECTION CONTROL	IO EXPANDER-P25		OUTPUT	HIGH	LOW		VCC_3V3_SYS
22	Power Delivery I2C Interrupt Request	PD_I2C_IRQ	INTERRUPT	IO EXPANDER-P26		INPUT	HIGH	LOW		VCC_3V3_SYS
23	User Test LED 2	IO_EXP_TEST_LED	GPIO	IO EXPANDER-P27		OUTPUT	LOW	HIGH		VCC_3V3_SYS
	IO EXPANDER – 02									
1	SoC SPI0 MUX Selection	SPI0_FET_SEL	ENABLE	IO EXPANDER-P20		OUTPUT	LOW	HIGH		VCC_3V3_SYS
2	SoC SPI0 MUX Enable	SPI0_FET_OE	CONTROL	IO EXPANDER-P21		OUTPUT	LOW	LOW		VCC_3V3_SYS
3	CSI Regulator Enable (VCC_CSI_IO)	CSI_VLDO_SEL	ENABLE	IO EXPANDER-P26		OUTPUT	LOW	HIGH		VCC_3V3_SYS
4	WLAN Reset control GPIO	SOC_WLAN_SDIO_RST	RESET	IO EXPANDER-P27		OUTPUT	HIGH	LOW		VCC_3V3_SYS
5	Wilink Enable	WL_LT_EN	ENABLE	IO EXPANDER-P10		OUTPUT	LOW	LOW		VCC_3V3_SYS
6	CSI Reset control GPIO	CSI_RSTZ	RESET	IO EXPANDER-P11		OUTPUT	LOW	HIGH		VCC_3V3_SYS
7	CSI flex and mipi MUX Selection	CSI_SEL2	ENABLE	IO EXPANDER-P23		OUTPUT	HIGH	HIGH		VCC_3V3_SYS
8	CSI MUX Enable	CSI_EN	ENABLE	IO EXPANDER-P24		OUTPUT	HIGH	HIGH		VCC_3V3_SYS

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Texas Instruments | MISTRAL

Title	GPIO MAPPING TABLE	
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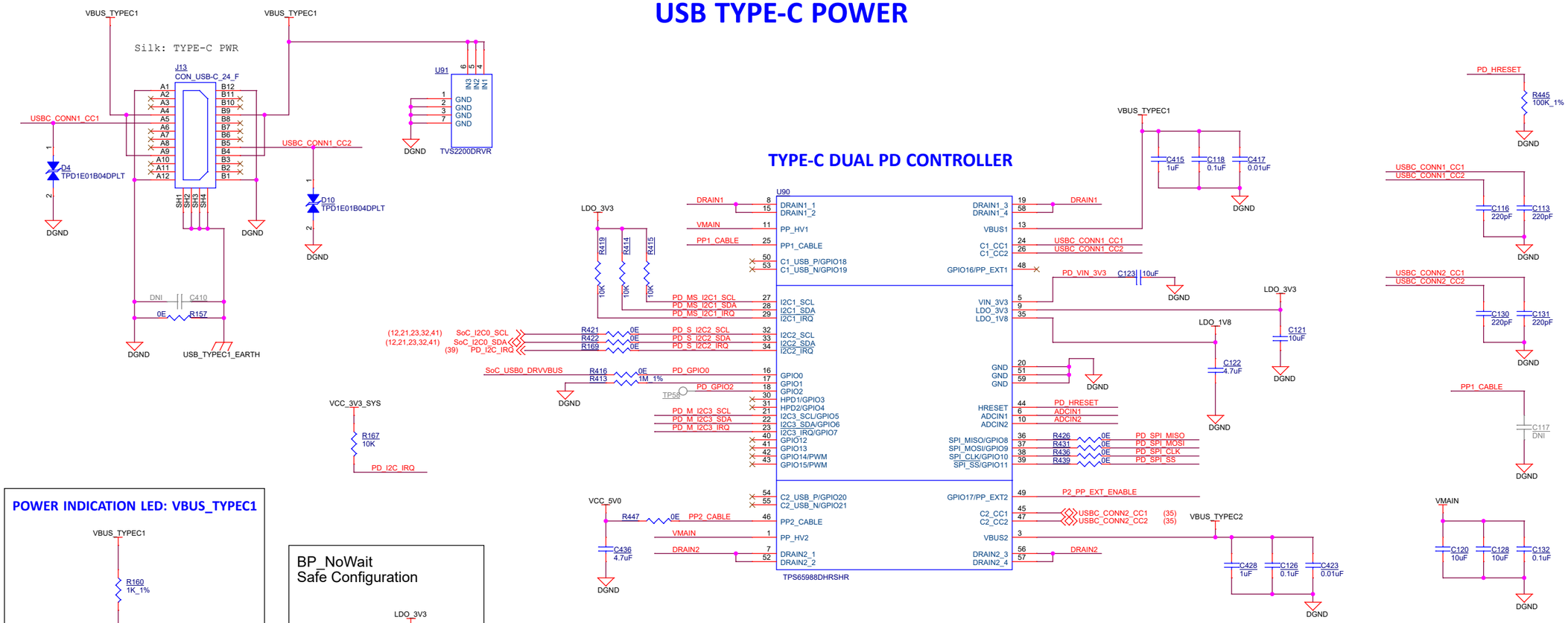
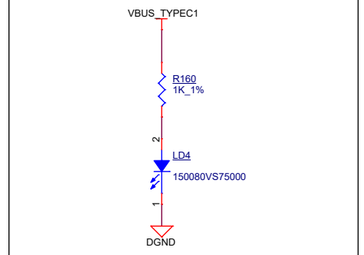
USB TYPE-C POWER

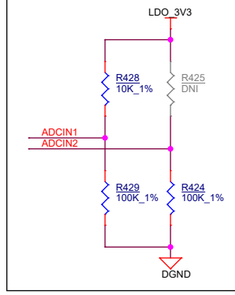
TYPE-C DUAL PD CONTROLLER



POWER INDICATION LED: VBUS_TYPEC1

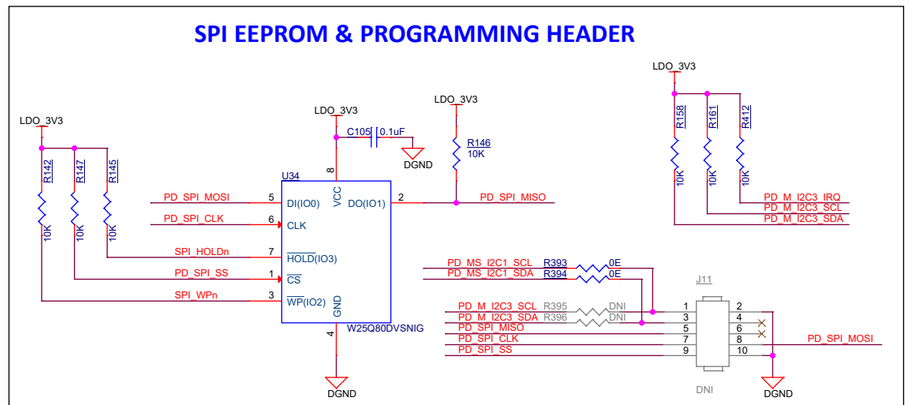


BP_NoWait
Safe Configuration

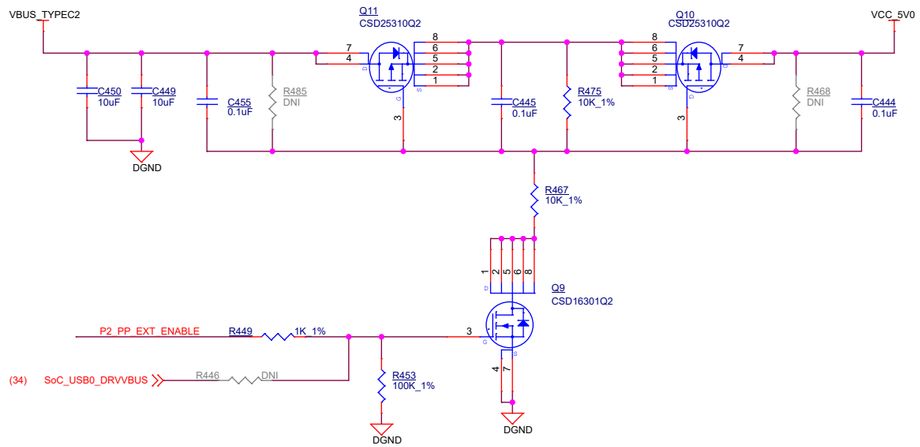


I2C Slave Address	Port1	Port2
I2C2(Default)	0x38	0x3F
I2C1	0x20	0x24

SPI EEPROM & PROGRAMMING HEADER



EXTERNAL POWER PATH FOR SOURCING, 5V/0.5A



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Title	USB TYPE-C		
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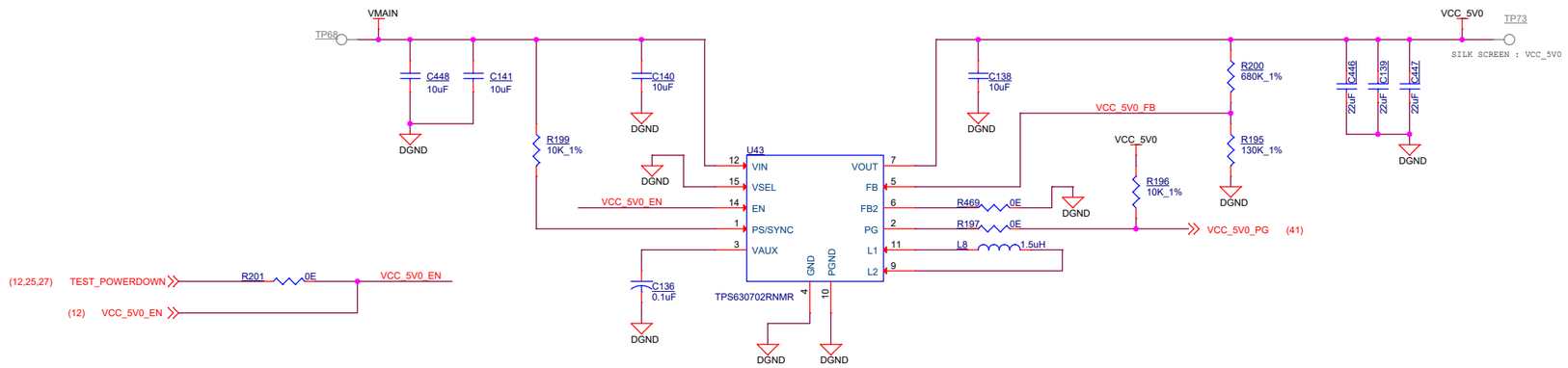
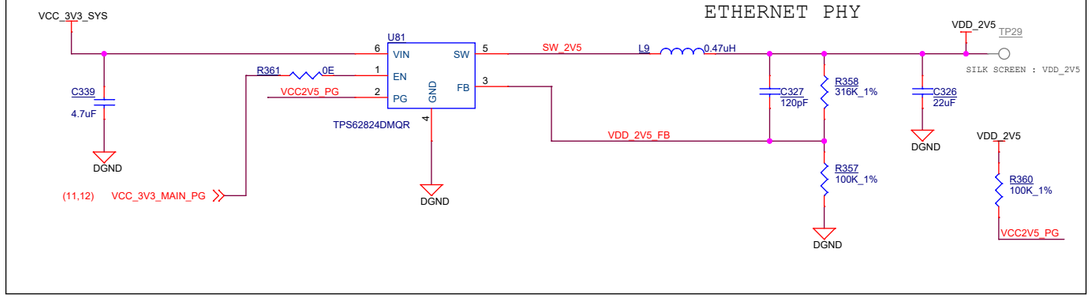
PERIPHERAL POWER SUPPLY-1

VinMin = 4.5V
VinMax = 15V
Vout = 5V @ 2A



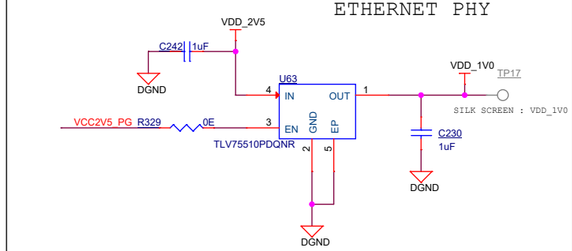
2.5V, 1.0AMPS SUPPLY

ETHERNET PHY

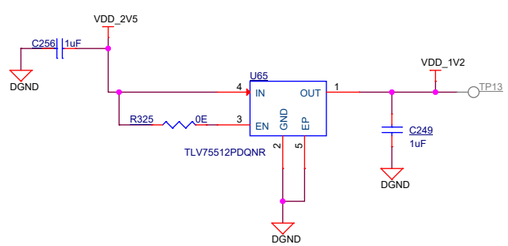


1.0V, 0.5AMPS SUPPLY

ETHERNET PHY



1.2V, 0.5AMPS SUPPLY



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Title	PERIPHERAL POWER SUPPLY -1	
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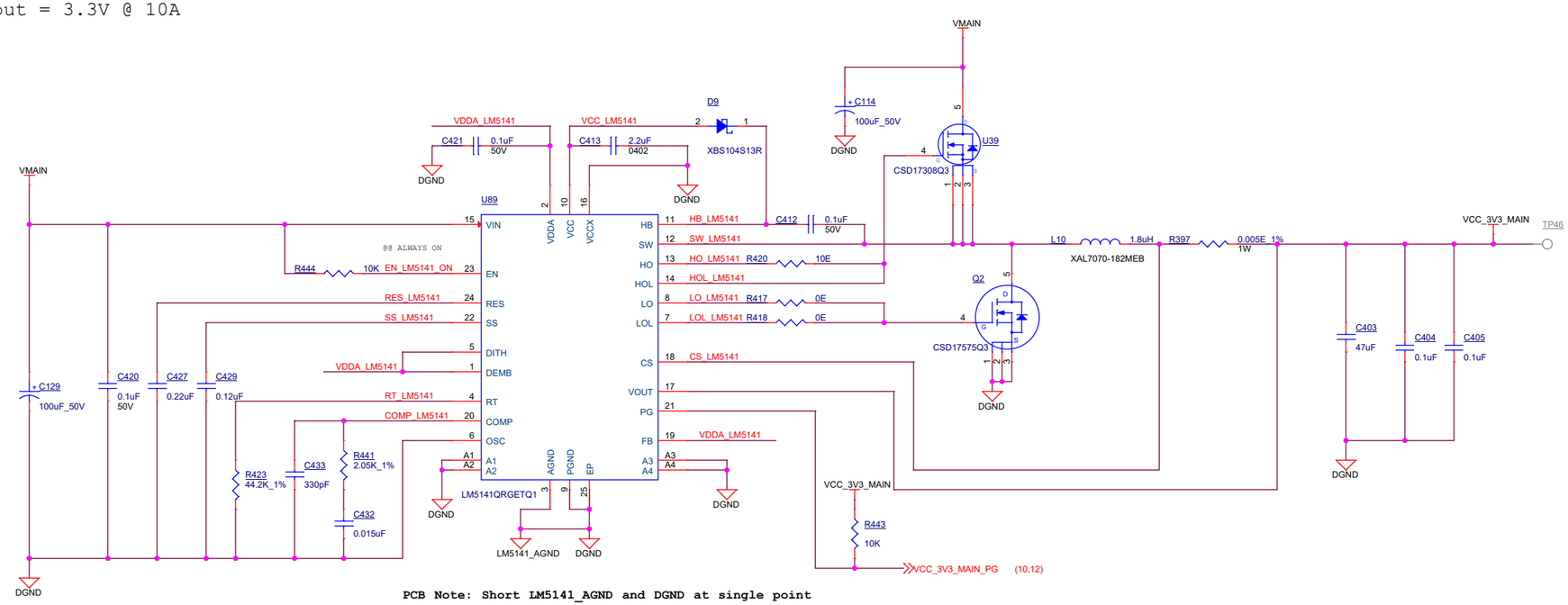
PERIPHERAL POWER SUPPLY-2

VinMin = 4.5V
VinMax = 15V
Vout = 3.3V @ 10A

3.3V, 10.0 AMPS SUPPLY



PCB Note: Short LM5141_AGND and DGND at single point

(33) ETH_CAN_INH_PREREG >> DNI R81 EN_LM5141_ON

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Title	PERIPHERAL POWER SUPPLY-2		
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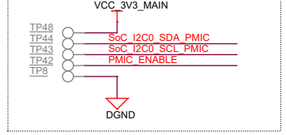
SOC POWER SUPPLY PMIC

PMIC Config option



Route as Pseudo differential pair trace

U27 (See "PCB Notes")

SN74LVC1G11DRYR

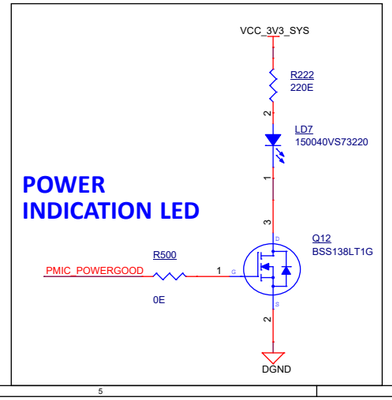
TMUX154EDGSR

PTPS65931211RWERQ1

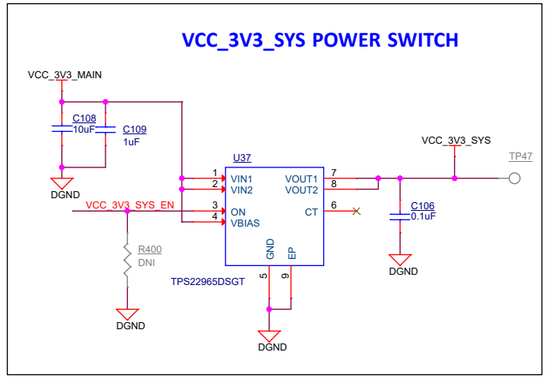
Capacitors C1047, C1074, C482, C494 & C1060 are marked DNP to meet PMIC output cap specifications

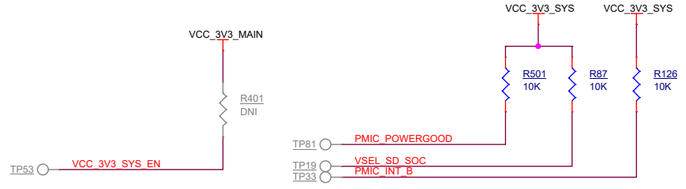
PMIC uses default I2C1 ADDR: 0x48,0x49, 0x5A, 0x5B

POWER INDICATION LED



VCC_3V3_SYS POWER SWITCH





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Title	SOC POWER SUPPLY PMIC	
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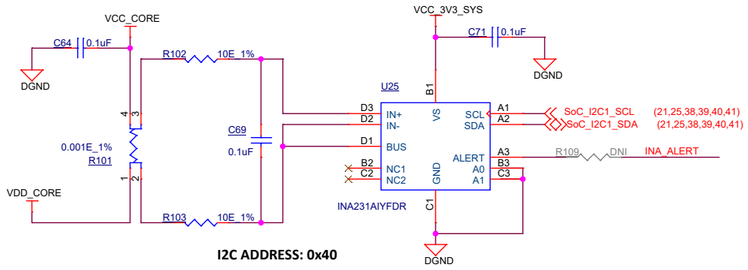
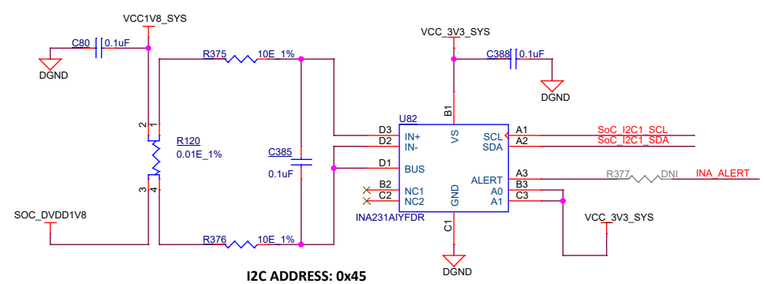
CURRENT MONITORING DEVICES

VDD_CORE



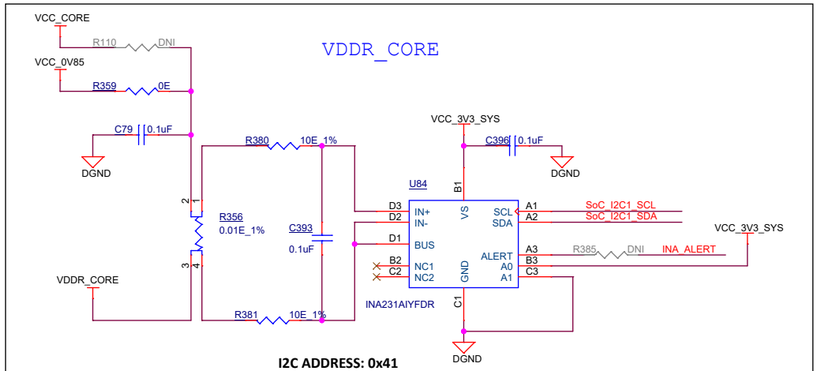
I2C ADDRESS: 0x40

SoC_DVDD1V8



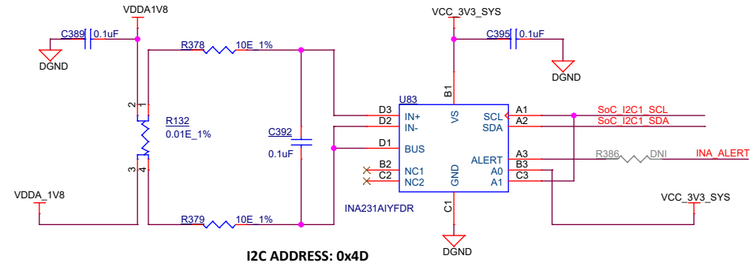
I2C ADDRESS: 0x45

VDDR_CORE



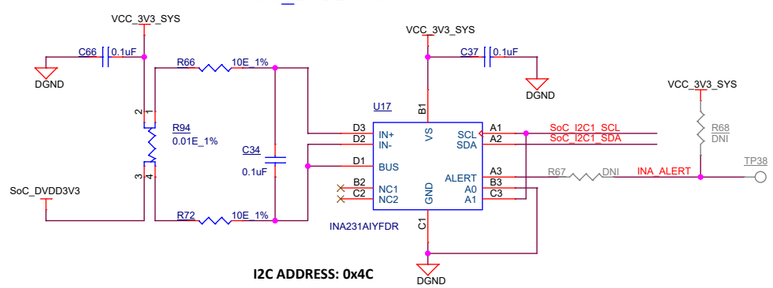
I2C ADDRESS: 0x41

VDDA_1V8



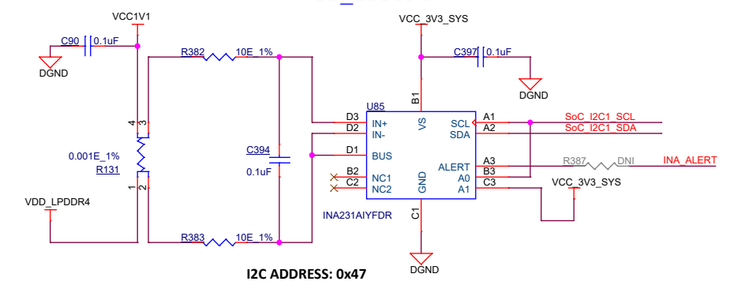
I2C ADDRESS: 0x4D

SoC_DVDD3V3



I2C ADDRESS: 0x4C

VDD_LPDDR4



I2C ADDRESS: 0x47

INA I2C SLAVE ADDRESS

POWER SOURCE	SUPPLY NET	SLAVE ADDRESS (IN HEX)
VCC_CORE	VDD_CORE	40
VCC_0V85	VDDR_CORE	41
VCC_3V3_SYS	SoC_DVDD3V3	4C
VCC_1V8	SoC_DVDD1V8	45
VDDA1V8	VDDA_1V8	4D
VCC1V1	VDD_LPDDR4	47

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Title	CURRENT MONITORING DEVICES	
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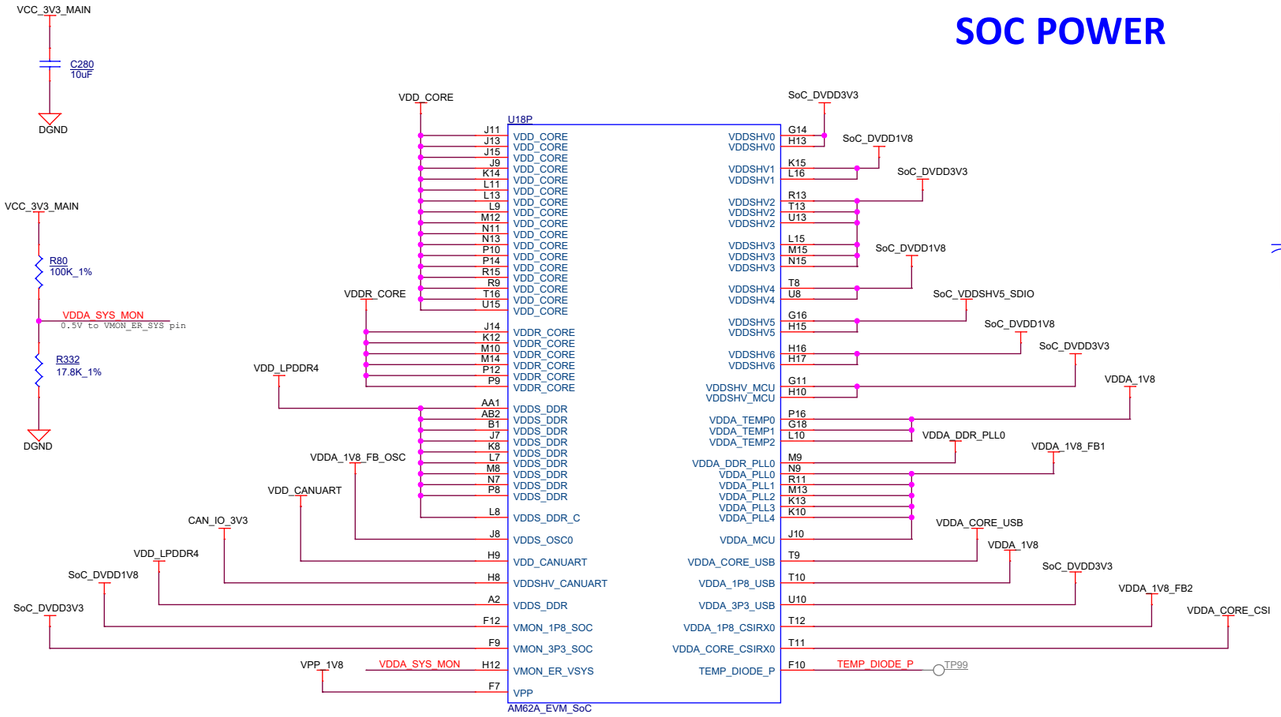
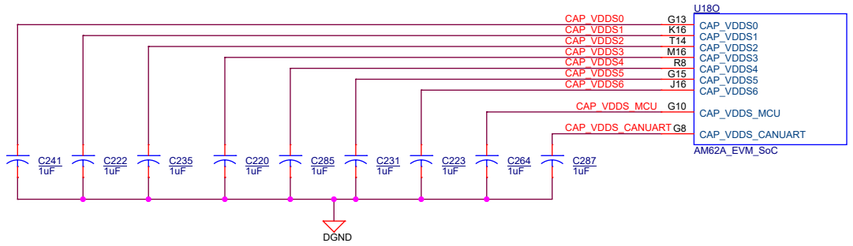
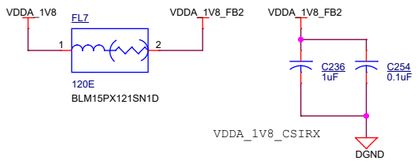
SOC POWER

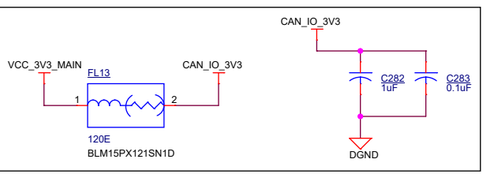


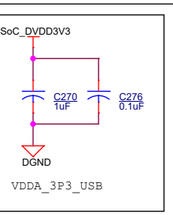


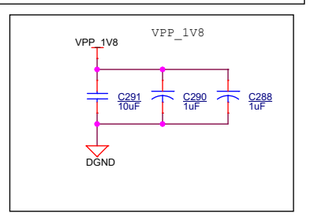
CORE SUPPLY

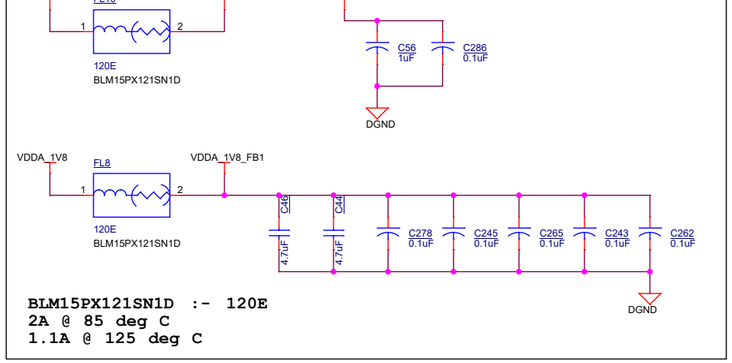
1.8V Analog SUPPLY



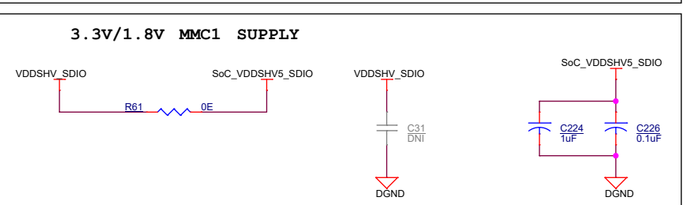


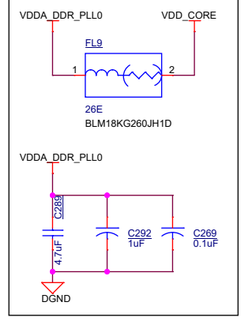


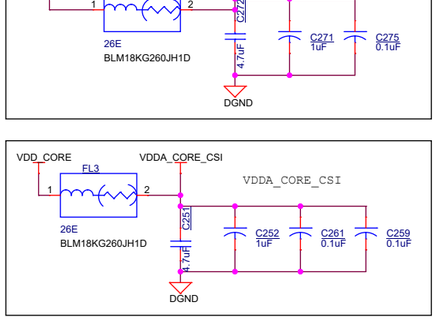


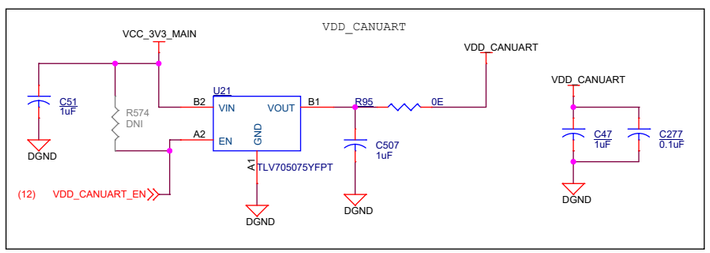


3.3V/1.8V MMC1 SUPPLY









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Title	SOC POWER	
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C		
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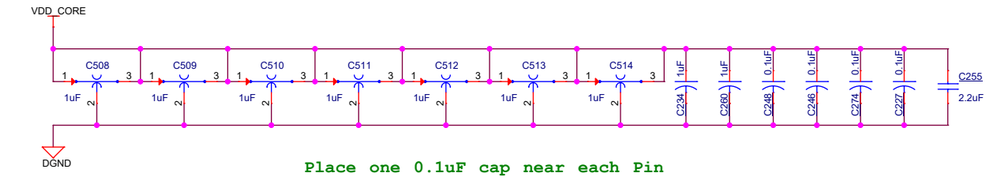
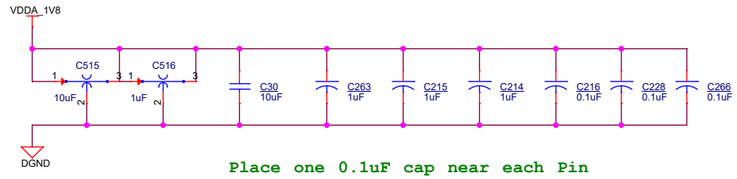
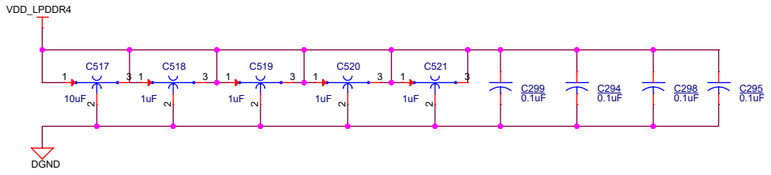
SOC POWER DECAPS



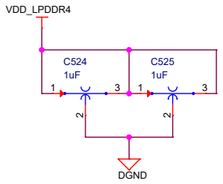
Place one 0.1uF cap near each Pin

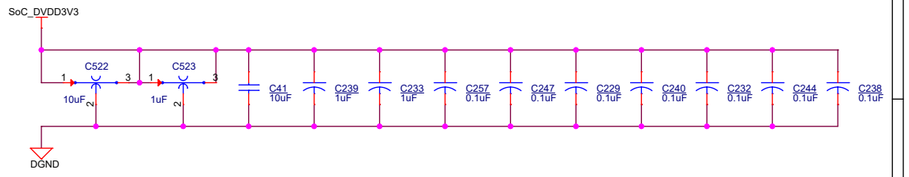


Place one 0.1uF cap near each Pin

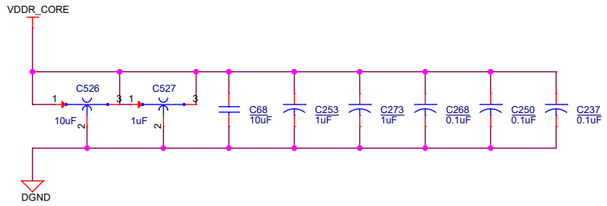


Place one 0.1uF cap near each Pin

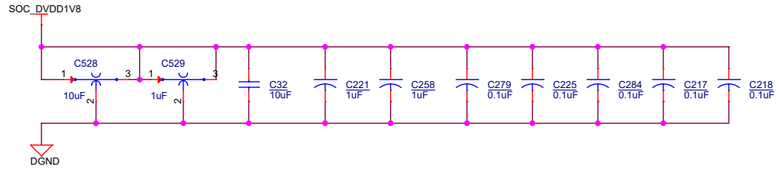




Place one 0.1uF cap near each Pin

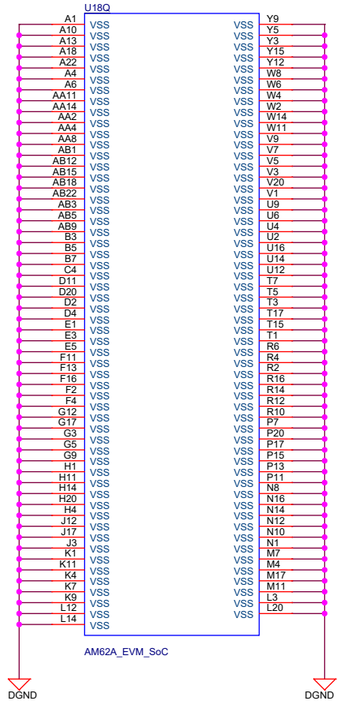


Place one 0.1uF cap near each Pin



Place one 0.1uF cap near each Pin

SOC VSS



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Title	SOC POWER CAPS & SOC VSS	
Size	PROC135E1	Rev
C		
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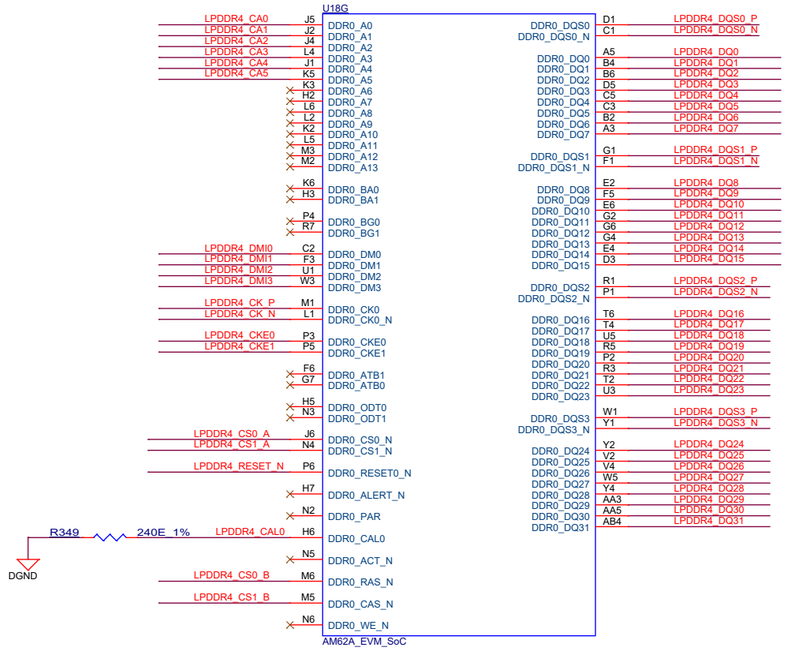
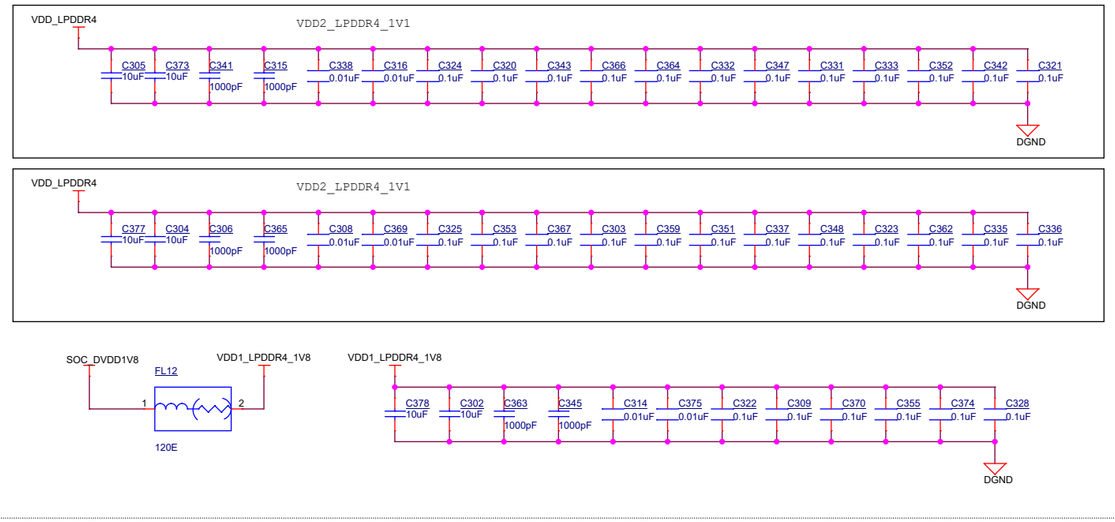
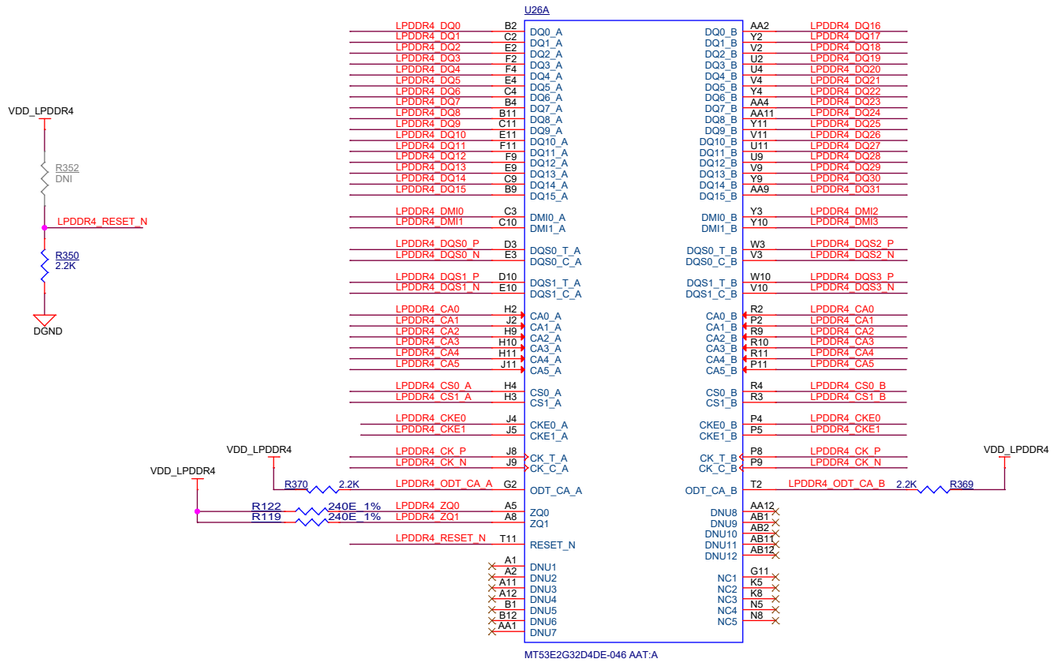
SOC LPDDR4 INTERFACE

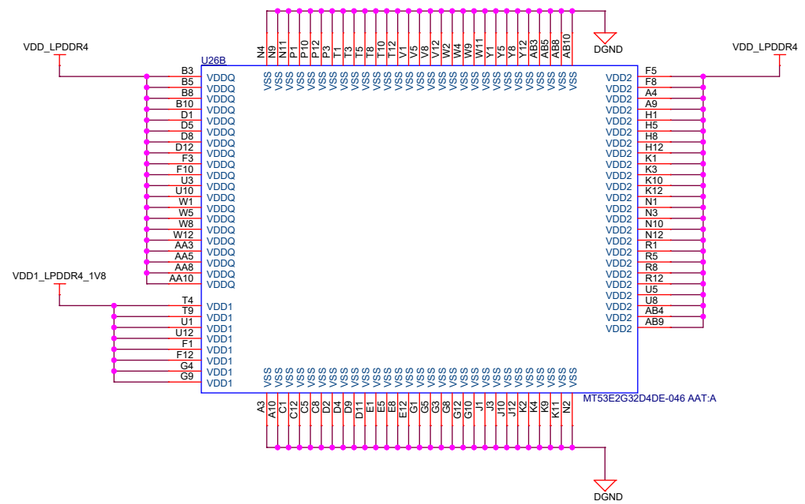


LPDDR4 POWER DECAPS



LPDDR4 DEVICE





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Title	SOC LPDDR4 INTERFACE	
Size		Rev
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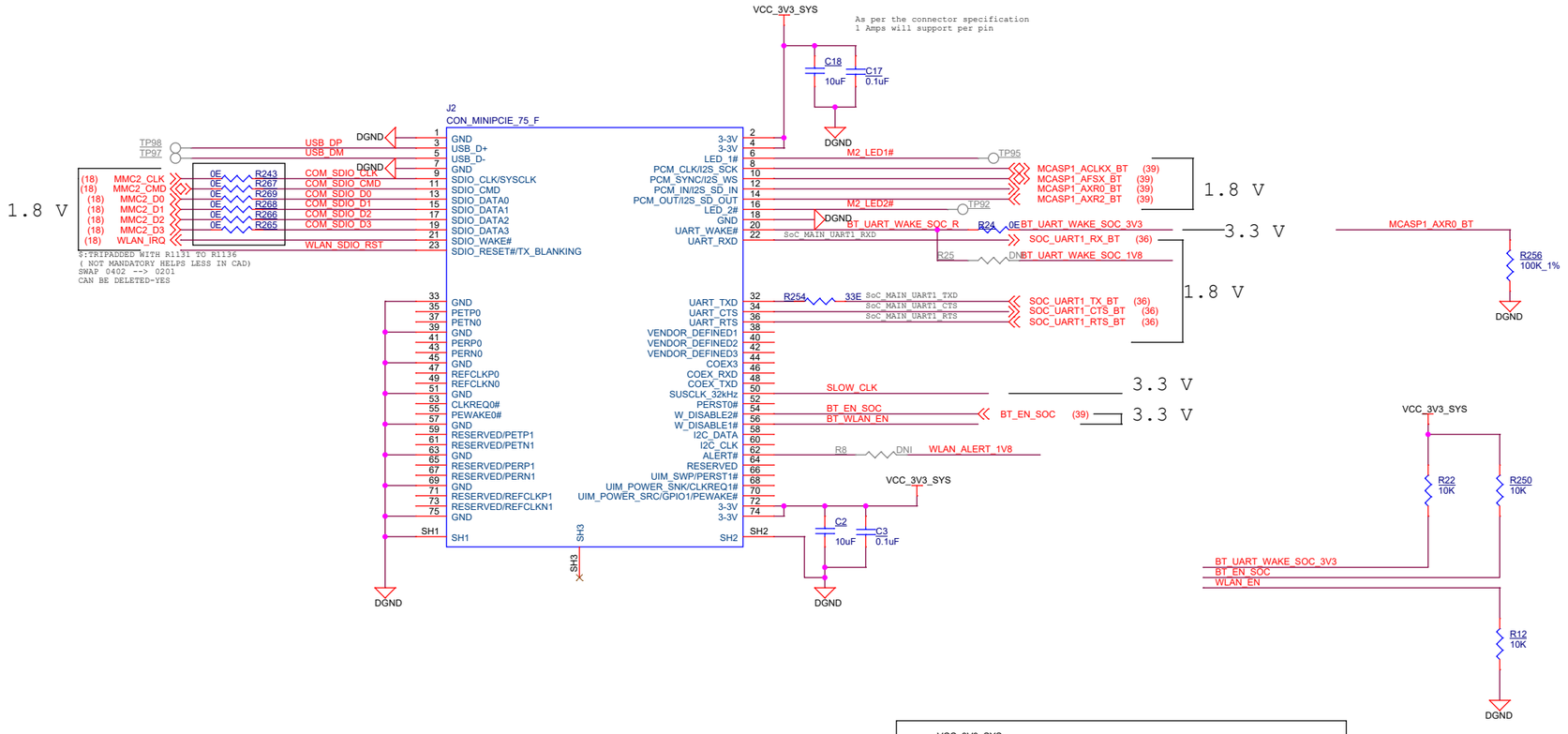
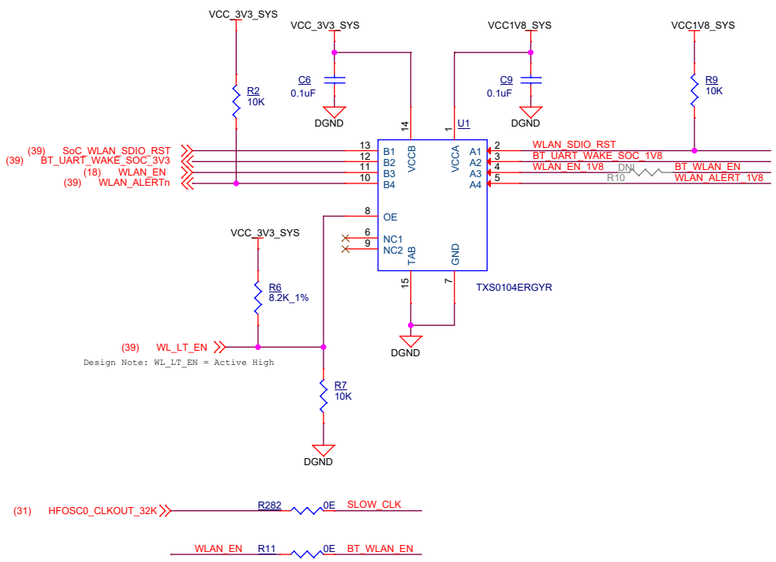
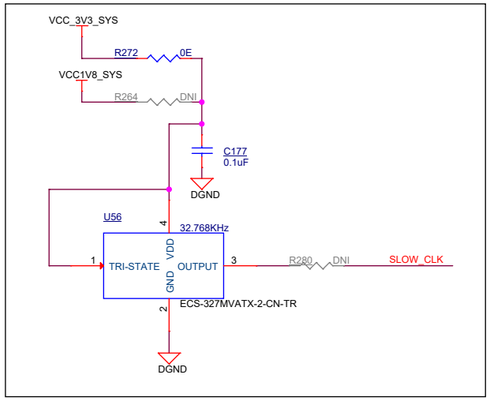
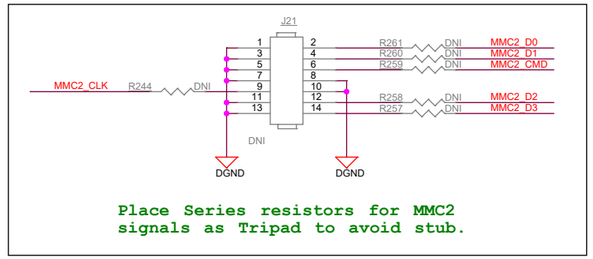
M.2 INTERFACE - SDIO

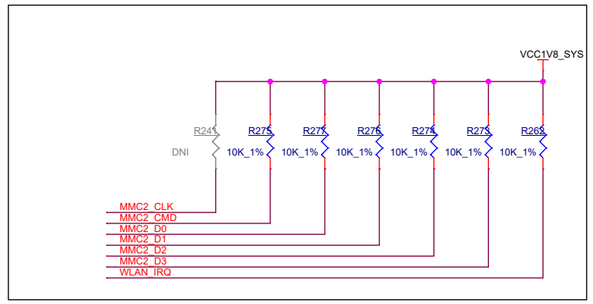


M.2 LEVEL TRANSLATOR









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Title	M.2 CONNECTOR I/F	
Size C	PROC135E1	Rev E2
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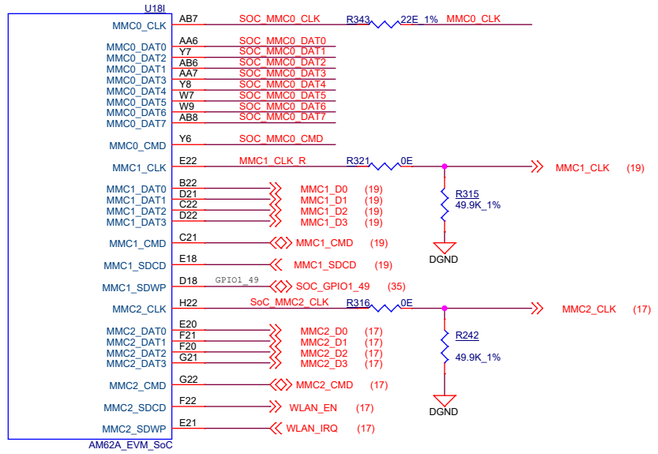
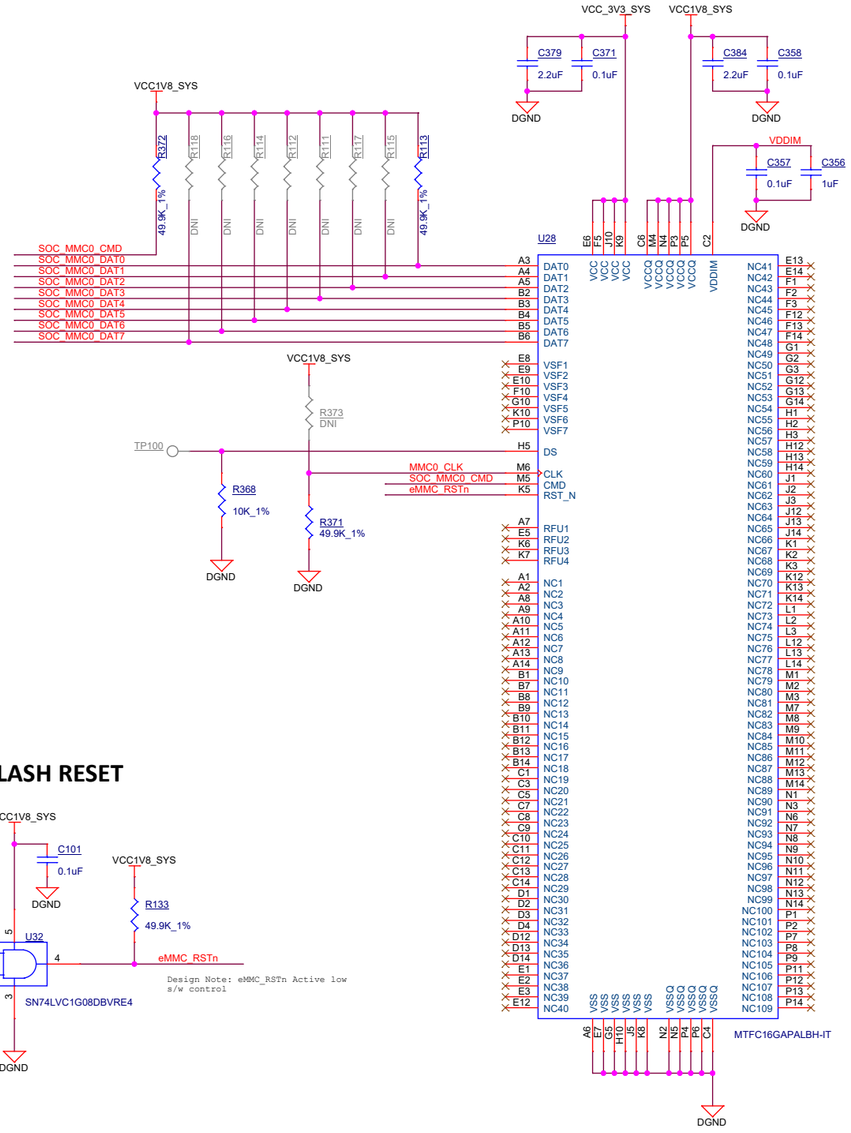
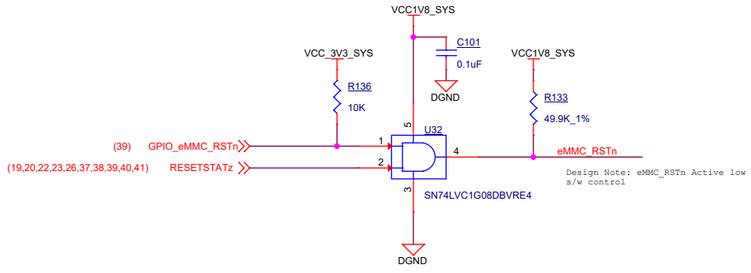
SOC - MMC Interface



eMMC FLASH



eMMC FLASH RESET



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Title	eMMC FLASH INTERFACE	
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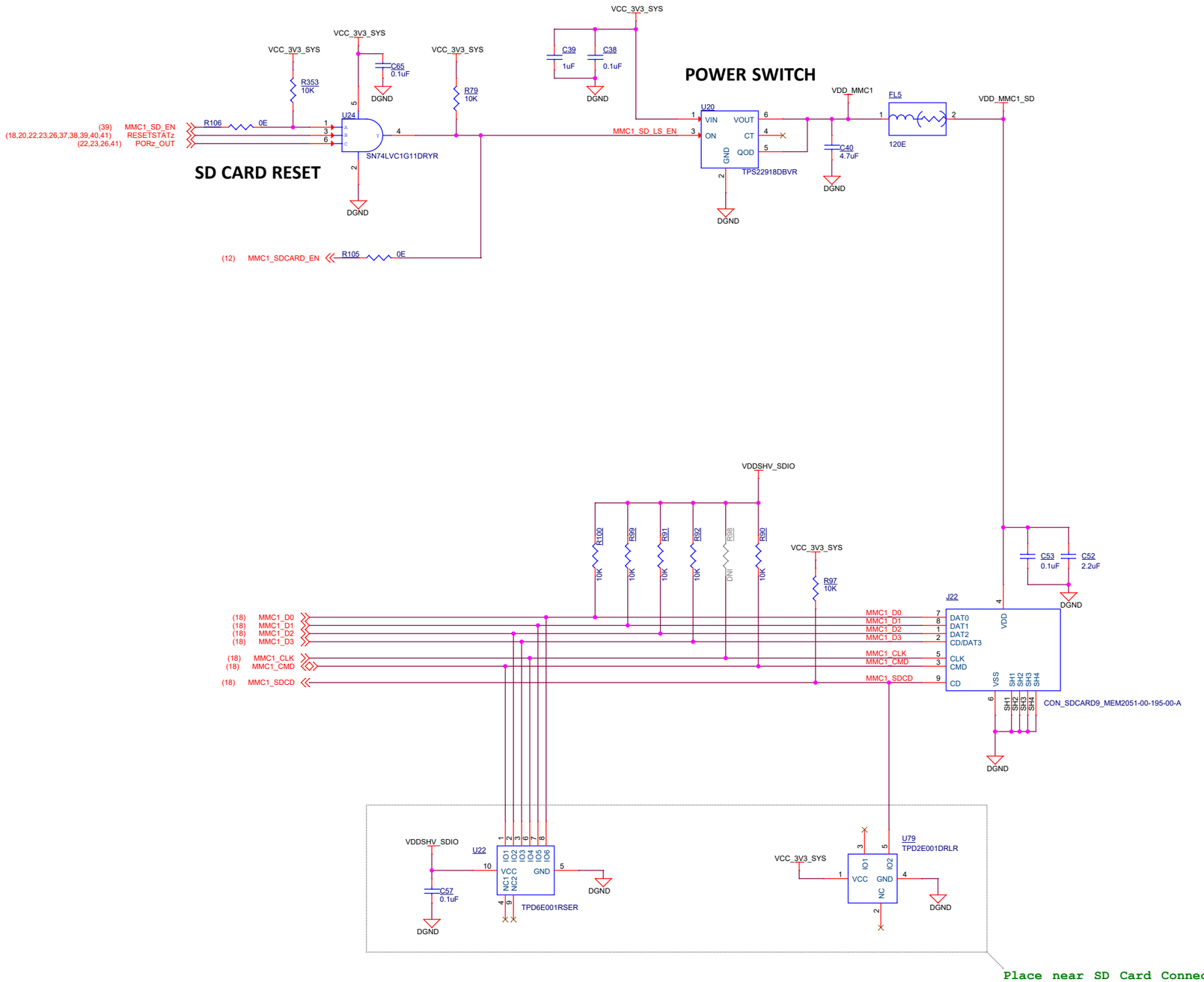
SD CARD INTERFACE



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Title	SD CARD INTERFACE	
Size: C	PROC135E1	Rev: E1
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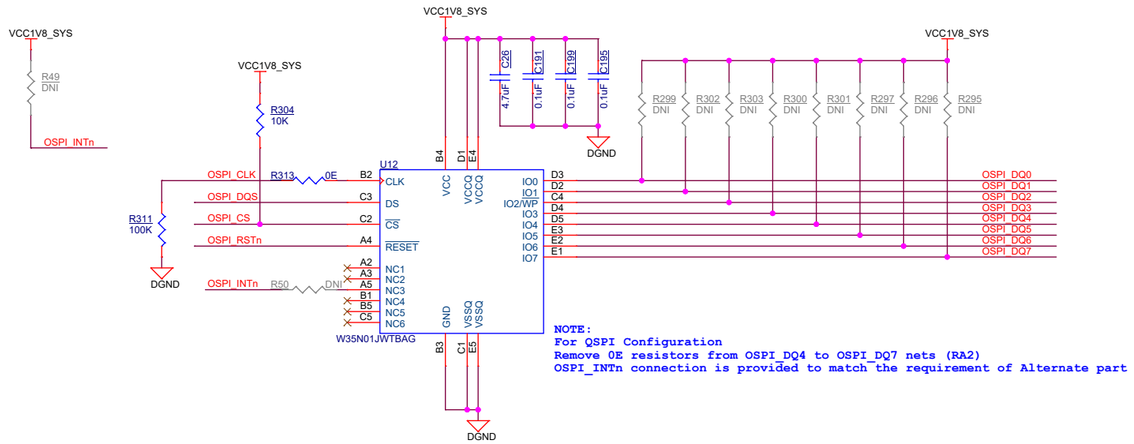
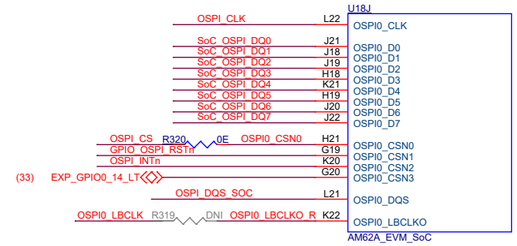
OSPI FLASH

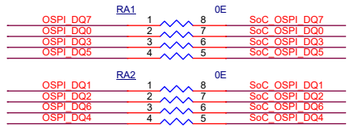


NOTE:
For QSPI Configuration
Remove 0E resistors from OSPI_DQ4 to OSPI_DQ7 nets (RA2)
OSPI_INTn connection is provided to match the requirement of Alternate part

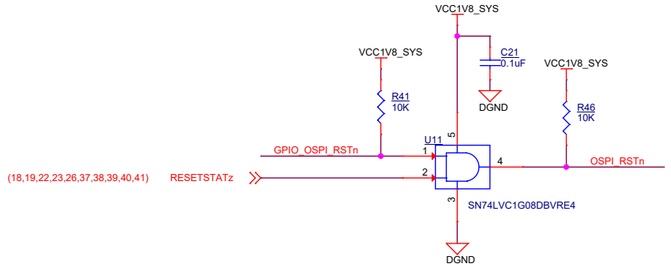
SOC OSPI INTERFACE

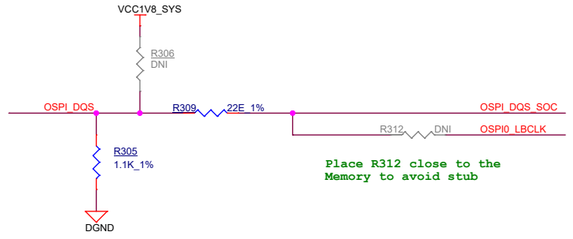


Place R319 close to the SOC Ball
with as little trace as possible



OSPI FLASH RESET





Place R312 close to the
Memory to avoid stub

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Size C	PROC135E1	Rev E1
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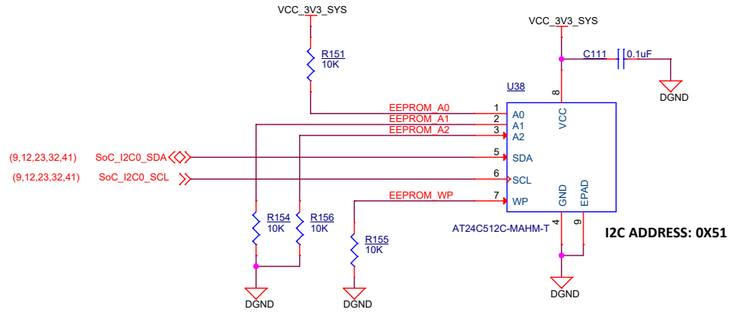
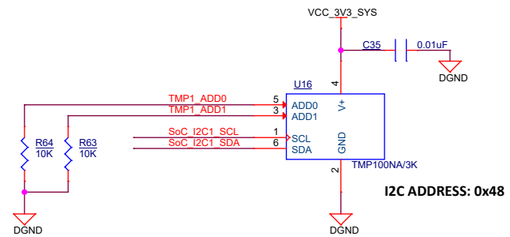
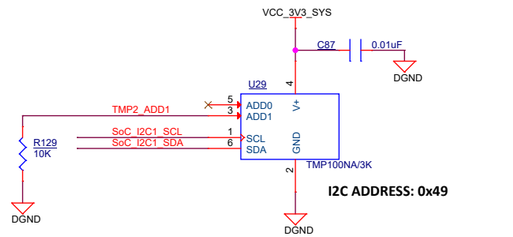
BOARD ID EEPROM



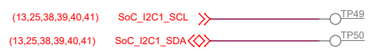
TEMPERATURE SENSORS





CAD NOTE: PLACE TEMP SENSOR U80 CLOSE TO SoC

CAD NOTE: PLACE TEMP SENSOR U81 CLOSE TO DDR4



Silk: SOC_I2C1

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Size: C	PROC135E1	Rev: E1
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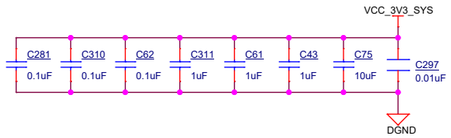
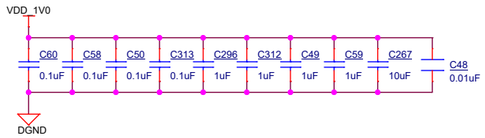
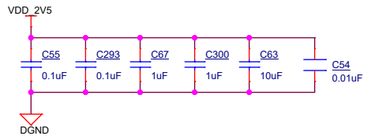
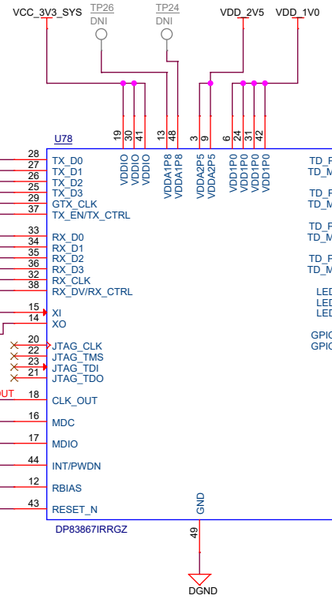
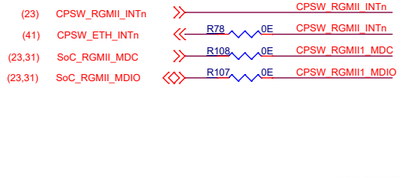
CPSW RGMII 1 - PHY



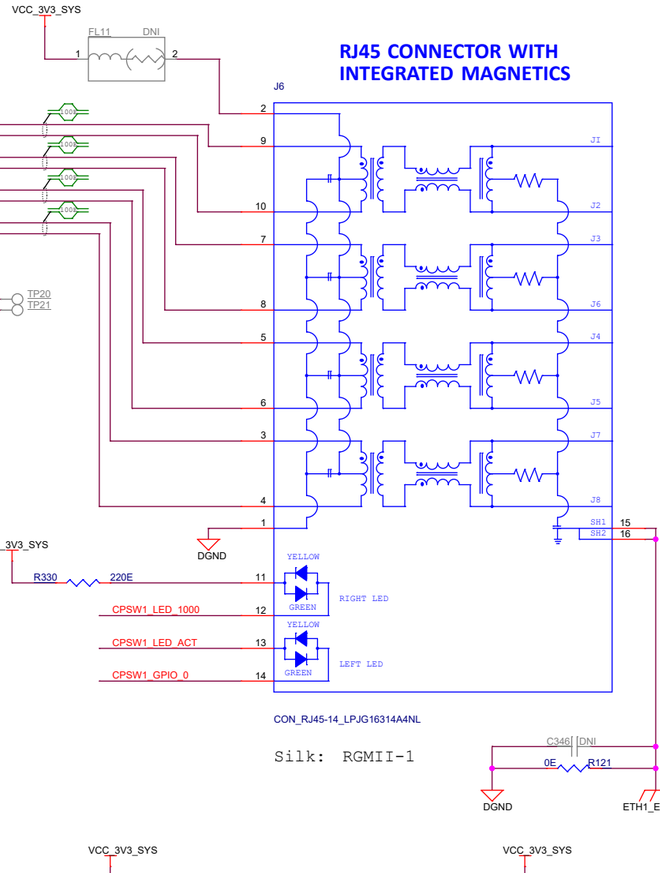


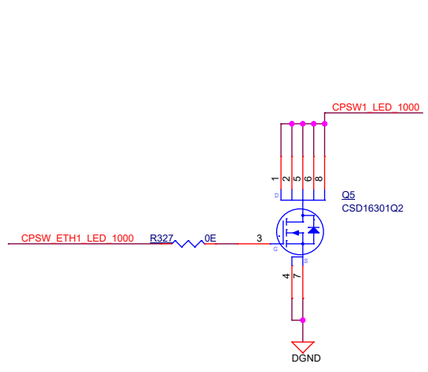


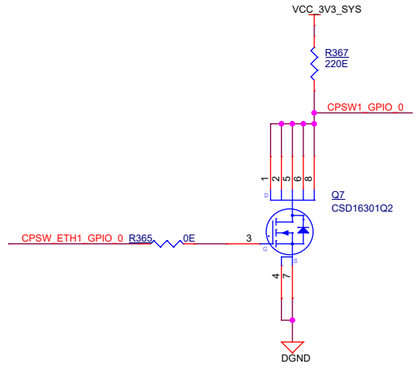


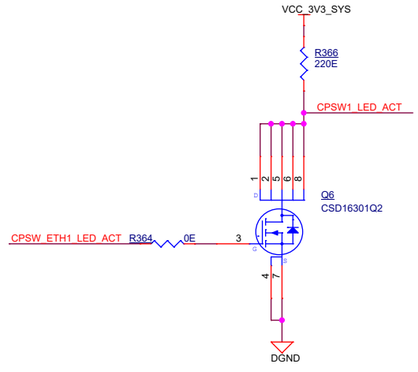


PHY ADDRESS = 00000
Auto-negotiation Enabled
10/100/1000 advertised, Auto-MDI-X
Tx Clock Skew = 0ns
Rx Clock Skew = 2ns









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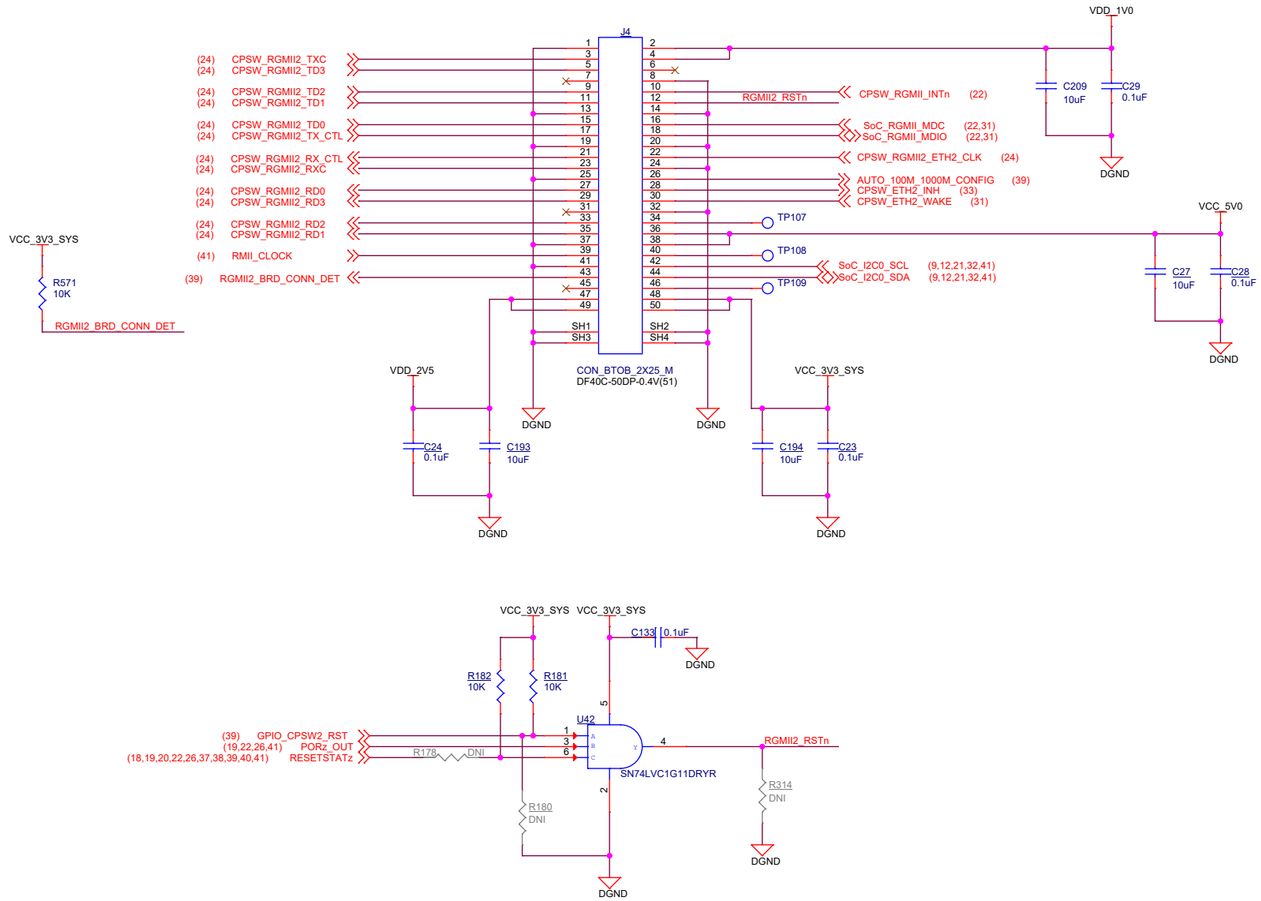
CPSW RGMII 2 - PHY



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Title	CPSW RMII_2 ETHERNET PHY		
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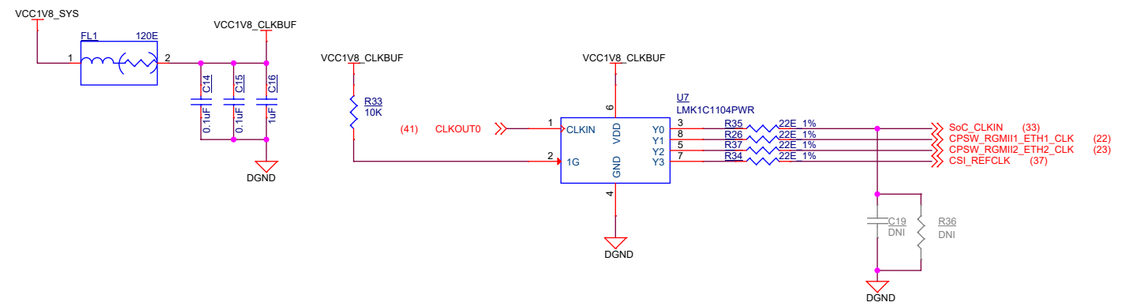
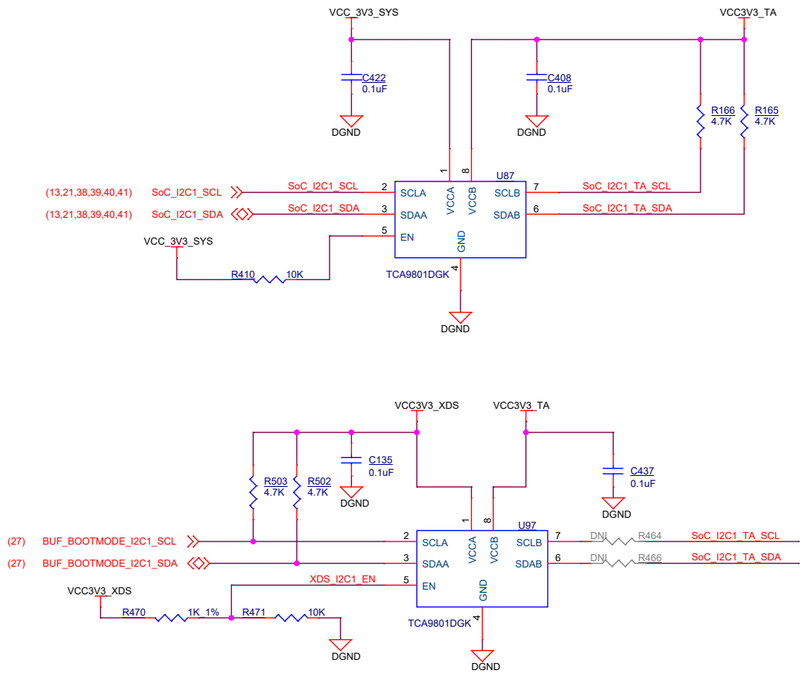
ETHERNET PHY CLOCK BUFFER



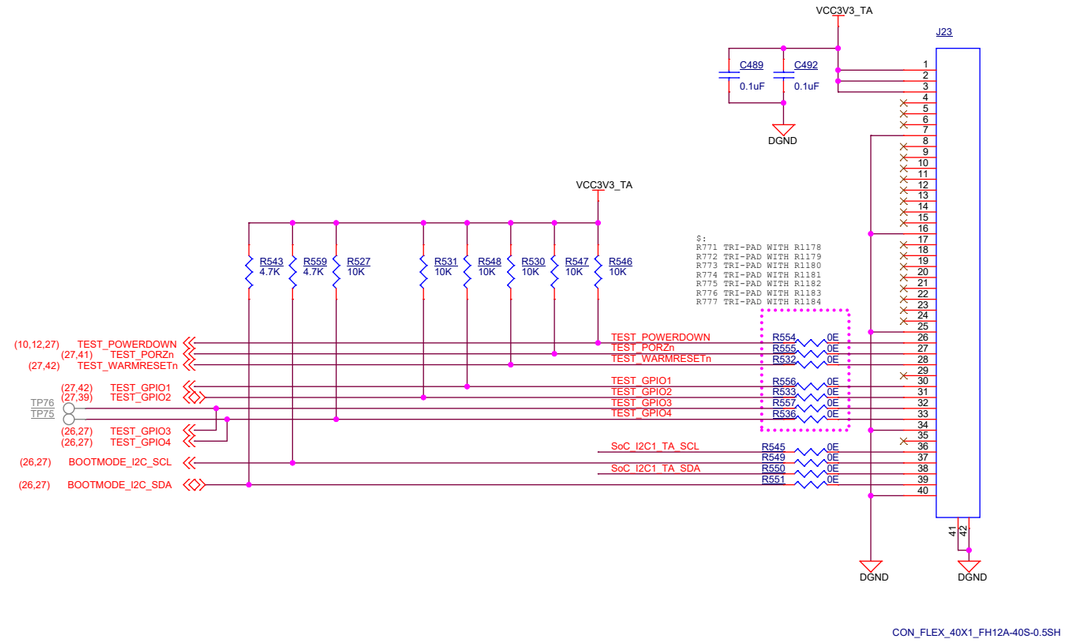
Designed for TI by Mistral Solutions Pvt Ltd

Title	ETHERNET PHY CLOCK BUFFER & LED DRIVER	
Size C	PROC135E1	Rev E1
Date: Wednesday, June 01, 2022	Sheet 24 of 44	

I2C BUS BUFFER



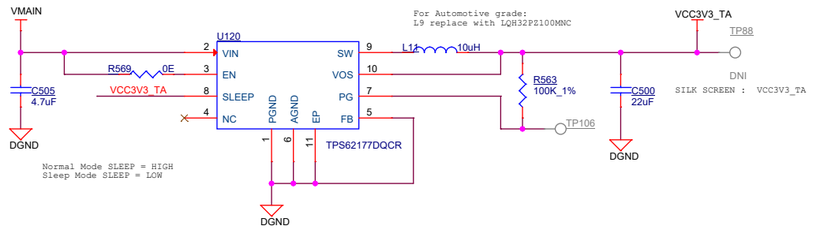
40-PIN TEST AUTOMATION HEADER



Silk: AUTOMATION HDR

TEST AUTOMATION BOARD POWER

VinMin = 4.75V
VinMax = 24V
Vout = 3.3V @ 0.5A



TEST AUTOMATION GPIO MAPPING

SIGNAL NAME	DESCRIPTION	Direction WRT CTRL	Internal/ External PU/PD states
TEST_POWERDOWN	Used to Power down the EVM	OUTPUT	External Pullup
TEST_PORZn	Used to Reset the SoC PORz	OUTPUT	External Pullup
TEST_WARMRESETn	Used to Reset the SoC Warmreset	OUTPUT	External Pullup
TEST_GPIO1	Used to Generate the interrupt on SOC_GPIO1_23 Pin	OUTPUT	External Pullup
TEST_GPIO2	Connected to IO Expander to Communicate with SOC	OUTPUT	External Pullup
TEST_GPIO3	Used to Enable the BOOTMODE Buffer	OUTPUT	External Pullup
TEST_GPIO4	Used to Reset the Bootmode I2C IO Expander	OUTPUT	External Pullup

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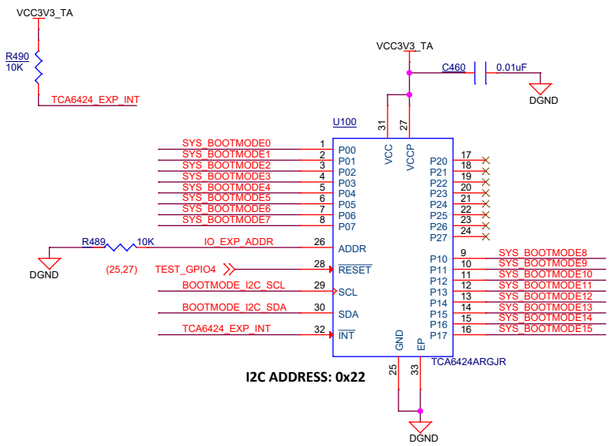
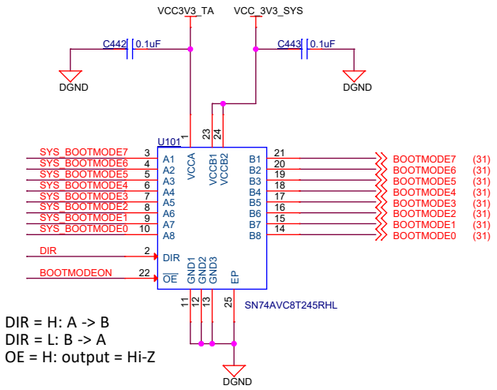
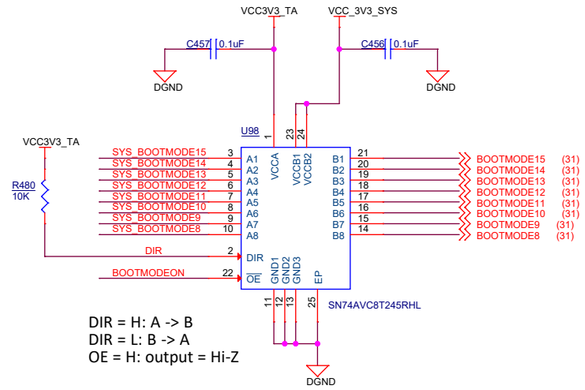
Title	TEST AUTOMATION	
Size C	PROC135E1	Rev E1
Date: Wednesday, June 01, 2022	Sheet 25 of 44	

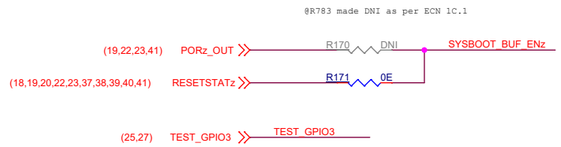
BOOTMODE IO EXPANDER

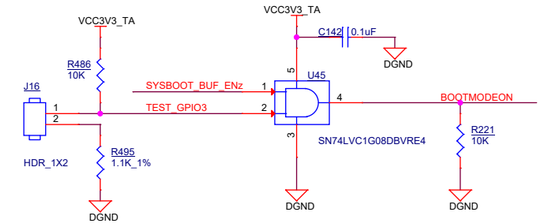


BOOT MODE BUFFERS

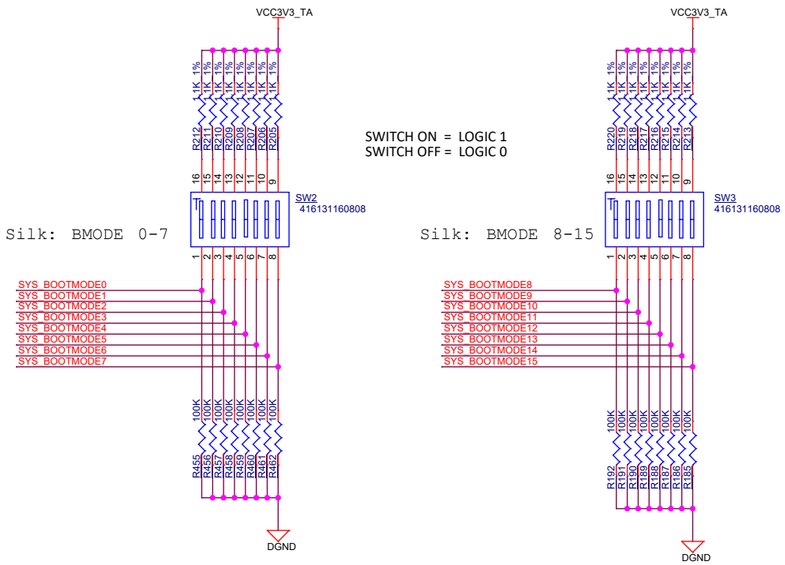








BOOT MODE SWITCHES



BOOT MODES SUPPORTED

1. OSPI
2. MMC1 - SD CARD
3. UART
4. eMMC
5. ETHERNET
6. USB0 DFU
7. USB0 MS

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Title	BOOT MODE BUFFER & SWITCHES		
Size C	PROC135E1		Rev E1
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XDS110 DEBUGGER

TP89 DNI
SILK SCREEN : XDS_USB_VBUS
XDS_USB_VBUS
C155 4.7uF
D8 TPD1E10B06DPYR
C470 2.2uF
R507 0E
U105
IN1 IN2 EN GND OUT1 OUT2 NR/FB NC PAD
TPS79601DRBR
R488 51K
C458 15pF
R487 30K
C461 1uF
VCC3V3_XDS
TP79 DNI
SILK SCREEN : VCC3V3_XDS
C469 1uF
C483 0.1uF
C147 0.1uF
C156 0.01uF
C150 0.01uF
C166 0.01uF
U47B
VDD GNDA VDDA VDDC VBAT
TM4C1294NCPDTT3R
C167 1uF
C164 0.01uF
VDDC_1V2
C154 2.2uF
C153 1uF
C464 0.1uF
R202 49.9E_1%
C144 0.1uF
DGND

Silk: JTAG

J18
VBUS D- D+ ID GND SH1 SH2 SH3 SH4
CON_MUSB-B_5_F
XDS_USB_DM
XDS_USB_DP
XDS_USB_ID
0E R226
C159 DNI
XDS_SHIELD
U115
IO1 IO2 IO3 IO4 VCC GND
TPD4E004DRYR

U47A
TM4C1294NCPDTT3R
PA0/U0RX PA1/U0TX PA2/SSI0CLK PA3/SSI0FSS PA4/SSI0XDAT0 PA5/SSI0XDAT1 PA6 PA7
(28) XDS110_TCK (28) XDS110_TMS (28) XDS110_TDO (28) XDS110_TDI (28) XDS110_TRST#
TP85 TP84 TP83 TP82 TM4C129_TCK TM4C129_TMS TM4C129_TDI TM4C129_TDO
PC0/TCK/SWCLK PC1/TMS/SWDIO PC2/TDI PC3/TDO/SWO PC4/C1- PC5/C1+ PC6/C0+ PC7/C0-
PE0/AIN3 PE1/AIN2 PE2/AIN1 PE3/AIN0 PE4/AIN9 PE5/AIN8
BUF_BOOTMODE_I2C_SCL BUF_BOOTMODE_I2C_SDA
PG0 PG1
PJ0 PJ1
(25) BUF_BOOTMODE_I2C1_SDA (25) BUF_BOOTMODE_I2C1_SCL
PL0 PL1 PL2 PL3 PL4 PL5
XDS_USB_DP XDS_USB_DM
PL6/USB0DP PL7/USB0DM
PN0 PN1 PN2 PN3 PN4 PN5
PQ0 PQ1 PQ2 PQ3 PQ4
PB0/USB0ID PB1/USB0VBUS PB2/I2C0SCL PB3/I2C0SDA PB4/AIN10 PB5/AIN11
PD0/AIN15 PD1/AIN14 PD2/AIN13 PD3/AIN12 PD4/AIN7 PD5/AIN6 PD6/AIN5 PD7/AIN4
PF0 PF1 PF2 PF3 PF4
PH0 PH1 PH2 PH3
PK0/AIN16 PK1/AIN17 PK2/AIN18 PK3/AIN19 PK4 PK5 PK6 PK7
PM0 PM1 PM2 PM3 PM4 PM5 PM6 PM7
PP0/C2+ PP1/C2- PP2 PP3 PP4 PP5
R496 100E_1% R204 DNI
C143 0.1uF
XDS_USB_ID XDS_USB_VBUS
R237 30K
R238 20K_1%
R236 220E R240 220E
LD9 150080VS75000 GREEN
LD10 150040RS73220 RED
XDS110_EMU0 XDS110_EMU1
BUF_TEST_GPIO1 BUF_TEST_GPIO3 BUF_TEST_GPIO4 BUF_TEST_PORZn BUF_TEST_WARMRESETn BUF_TEST_POWERDOWN
R493 DNI PMIC_WDOG_DISABLE (12)
VCC3V3_XDS
R233 4.7K R234 4.7K
XDS110_EMU0 XDS110_EMU1 (28)

VCC3V3_XDS
C137 0.1uF
U44
1Y 2Y 3Y 4Y 1A 2A 3A 4A 5A 6A VCC GND
SN74LVC07ADGVR
(25,42) TEST_GPIO1 R484 DNI XDS_GPIO1
(25,26) TEST_GPIO3 R483 DNI XDS_GPIO3
(25,26) TEST_GPIO4 R482 DNI XDS_GPIO4
(25,41) TEST_PORZn R472 DNI XDS_PORZn
(25,42) TEST_WARMRESETn R198 DNI XDS_WARMRESETn
(10,12,25) TEST_POWERDOWN R194 DNI XDS_POWERDOWN
BUF_TEST_GPIO1 BUF_TEST_GPIO3 BUF_TEST_GPIO4 BUF_TEST_PORZn BUF_TEST_WARMRESETn BUF_TEST_POWERDOWN

VCC3V3_TA VCC3V3_XDS
C453 0.1uF C454 0.1uF
U102
B1 B2 VCCB VCCA A1 A2 OE GND
TXS0102DQER
(25,39) TEST_GPIO2 R481 DNI XDS_GPIO2
TP104 TP105
BUF_TEST_GPIO2 GPIO2_BUF_EN
R494 1K_1% R491 10K

R506 10K TP78
R511 DNI
XDS_RSTn
U47C
RST WAKE OSC0 OSC1 XOSC0 XOSC1 RBAIS VREFA+ HIB EN0RXIP EN0RXIN EN0RX0P EN0RX0N
TM4C1294NCPDTT3R
C146 12pF C145 12pF
Y4 16.000MHz
OSC0 OSC1
R232 4.87K_1%
VCC3V3_XDS
R239 4.7K
XDS_VREF
C161 0.01uF C165 0.1uF
U49
LM4040B25IDCKR

VCC3V3_XDS VCC3V3_TA
R477 4.7K R479 4.7K C452 0.1uF C451 0.1uF
U99
SCLA SDAA EN SCLB SDAB VCCA VCCB GND
TCA9801DGK
BUF_BOOTMODE_I2C_SCL BUF_BOOTMODE_I2C_SDA
R478 DNI BOOTMODE_I2C_SCL (25,26)
R476 DNI BOOTMODE_I2C_SDA (25,26)
VCC3V3_XDS
R474 1K_1%
BOOTMODE_I2C_EN
R473 10K

VCC3V3_XDS
R525 1K_1% R522 1K_1% R518 1K_1% R514 1K_1%
R231 DNI R230 DNI R229 DNI R225 DNI

Sets the unique ID of the Debugger

Designed for TI by Mistral Solutions Pvt Ltd

Title	XDS110 DEBUGGER	
Size	PROC135E1	Rev
C		E1
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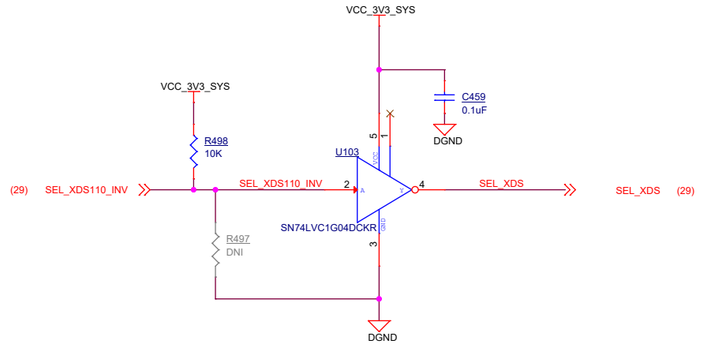
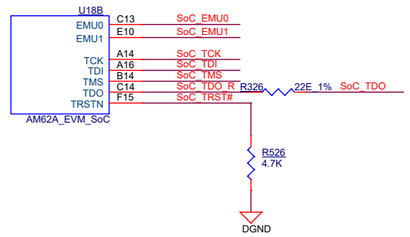
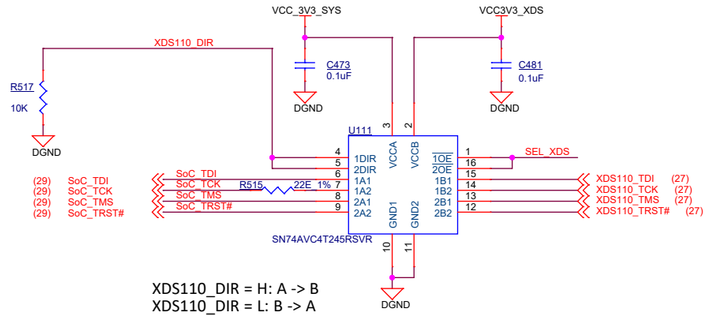
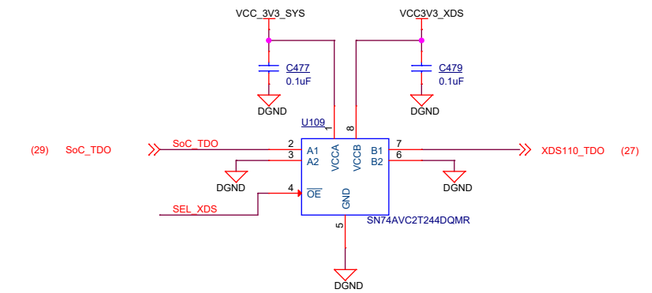


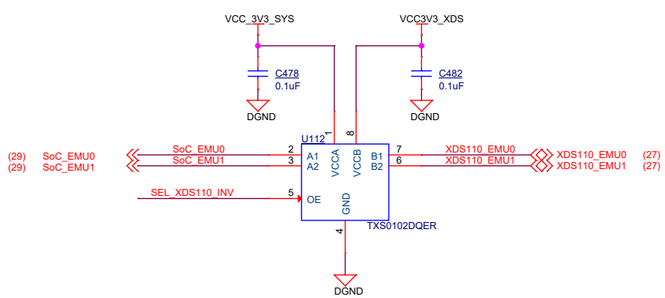
BUFFER XDS110

JTAG SOC SECTION





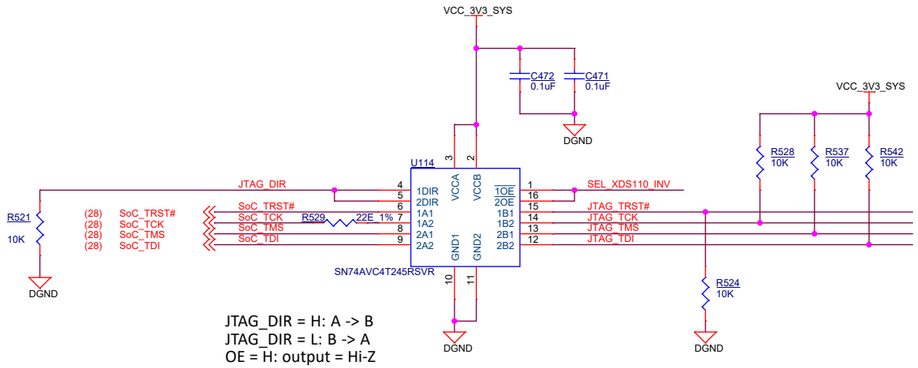




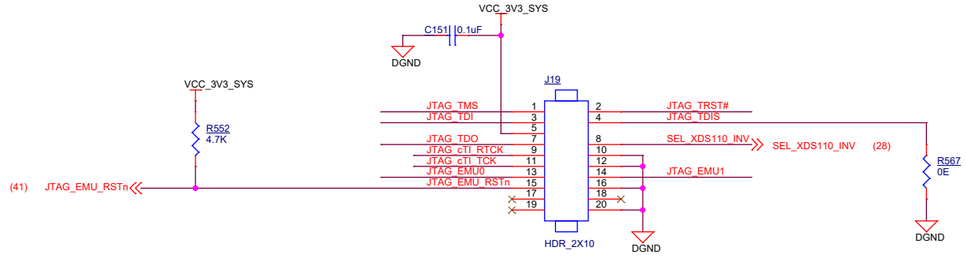
Designed for TI by Mistral Solutions Pvt Ltd

Title	JTAG BUFFER	
Size	PROC135E1	Rev
C		E1
Date:	Wednesday, June 01, 2022	Sheet 28 of 44

cTI20 JTAG BUFFERS

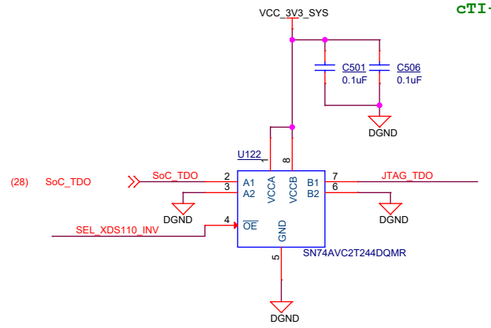


JTAG 20 PIN cTI CONNECTOR

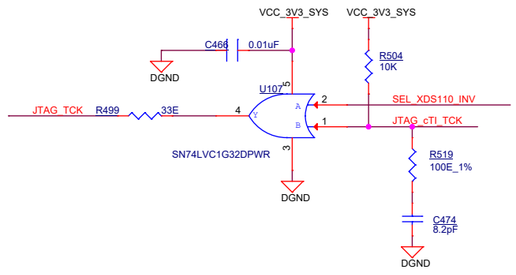


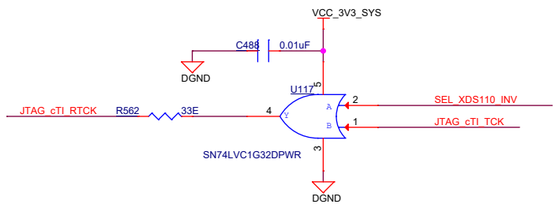
CAD NOTE: Buffers U99 and U101 need to be placed closer to the cTI-20pin connector J11 to reduce Stub length of the JTAG signals.

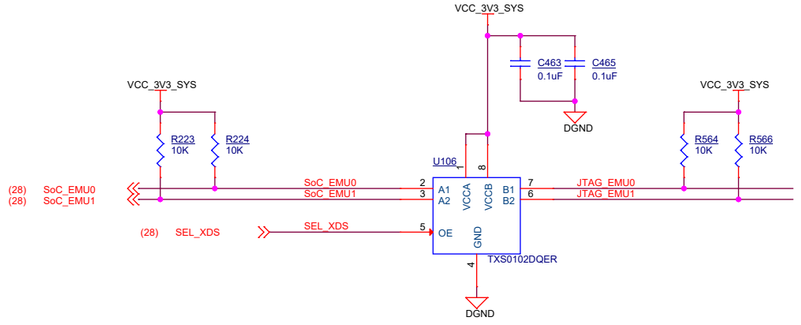
Silk: cTI



JTAG CLOCK BUFFER







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Title	JTAG 20 PIN cTI CONNECTOR	
Size C	PROC135E1	Rev E1
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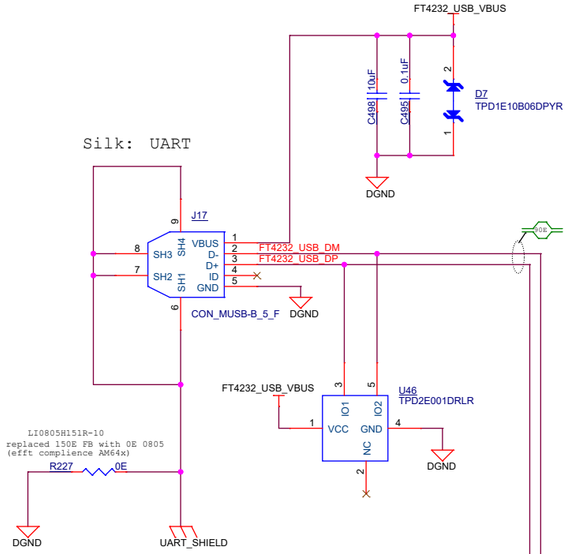
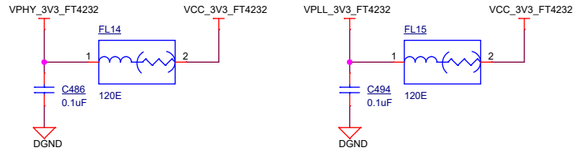
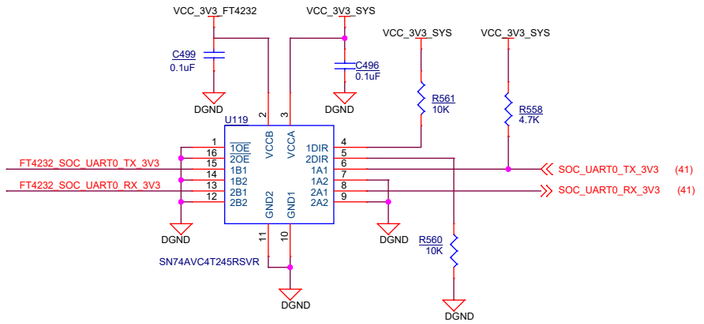
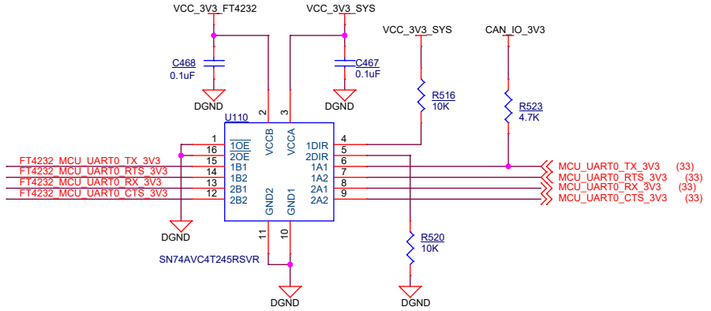
FT4232 UART

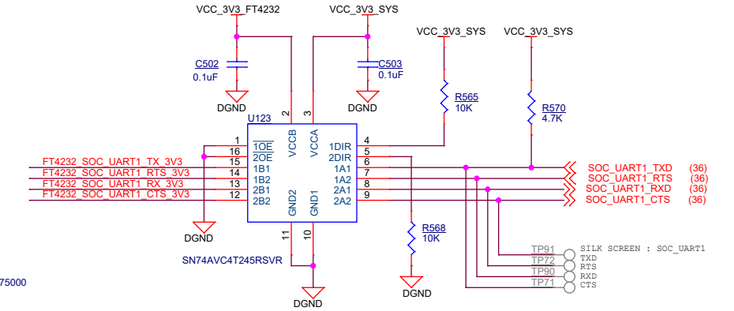
Silk: UART

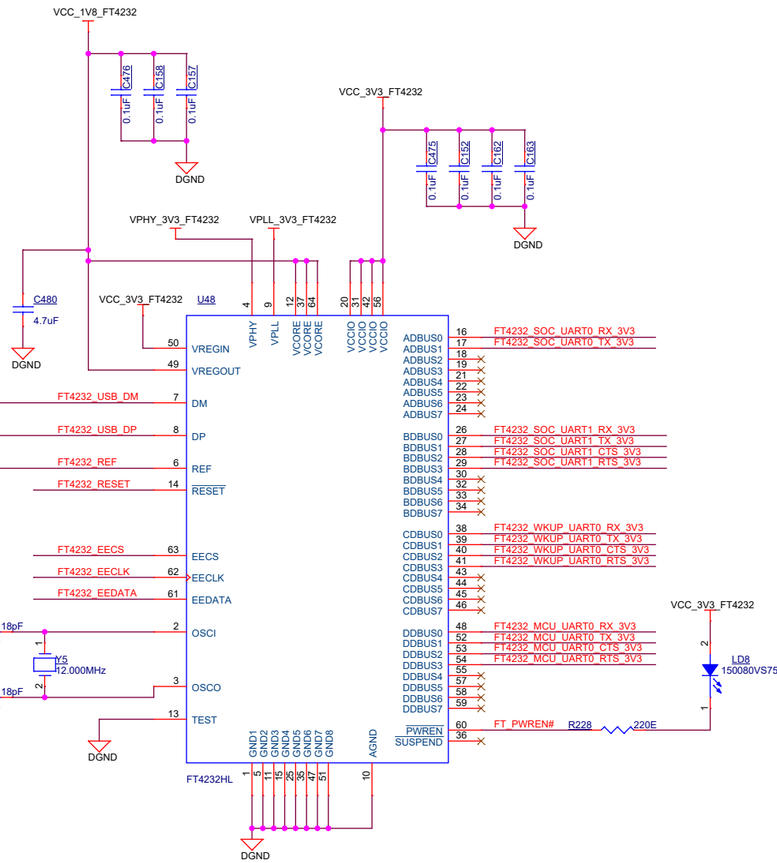


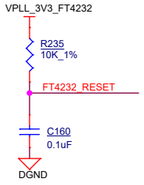


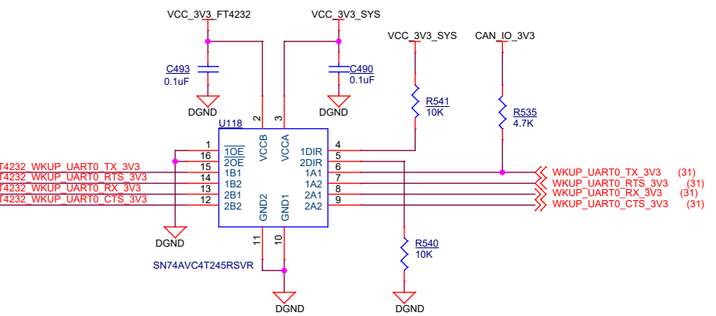




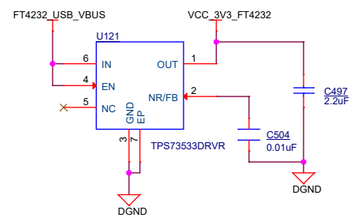




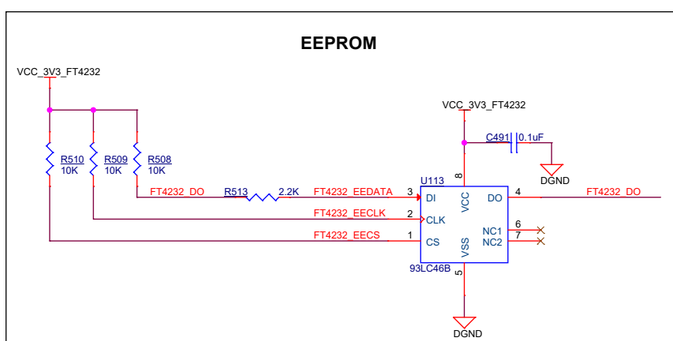




FT4232: 5V to 3.3V@500mA LDO



EEPROM



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Title	FT4232 UART TO USB BRIDGE	
Size C	PROC135E1	Rev E1
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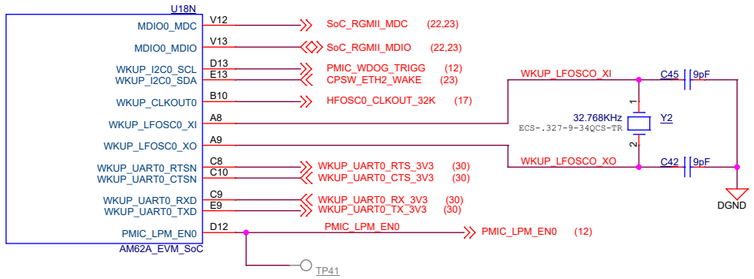
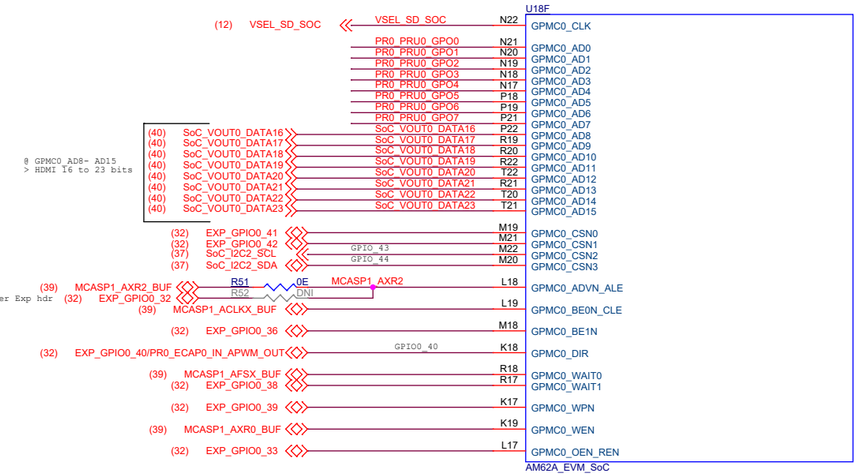
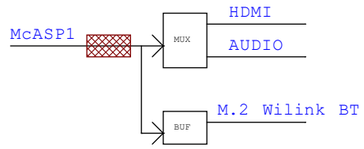
SOC WKUP DOMAIN

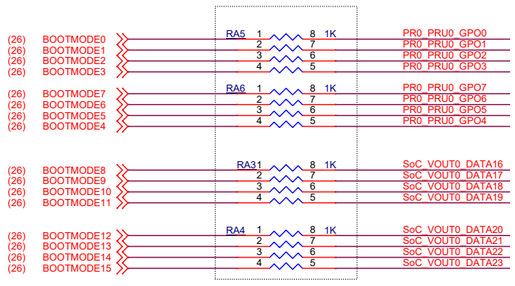


SOC GPMC





BOOTMODE PINS



NOTE: 1K Resistors are used to isolate the BOOTMODE control logic after the value is latched

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Title	SOC WKUP & GPMC		
Size	PROC135E1		Rev
C			E1
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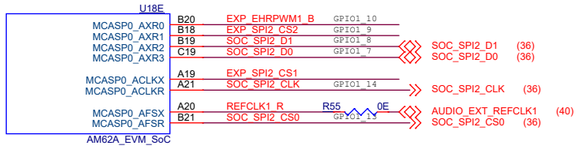
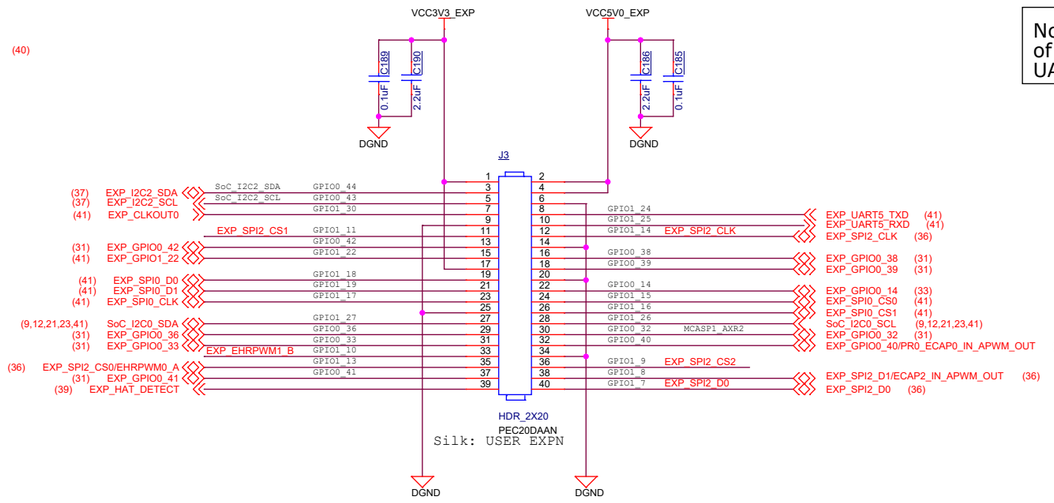
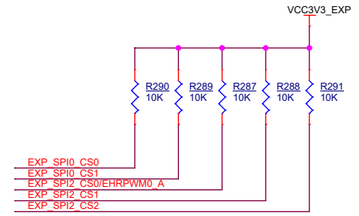
USER EXPANSION CONNECTOR



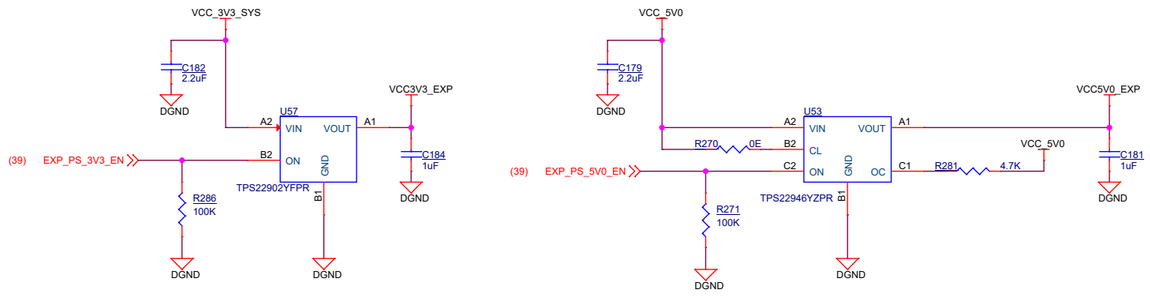
R32(Series damping resistor) should be placed close to SoC



Note: Expansion boards should take care of the null modem connectivity for the UART signals (cross-over of Rx and Tx)



POWER SWITCHES FOR USER EXPANSION CONNECTOR



NOTE:

AM62A Starter Kit shall not be powered through the 5V0 or 3V3 pins on the 40-pin User Expansion Connector.

User Expansion Connector I/O are not fail-safe and shall not be driven when AM62A Starter Kit is not powered.

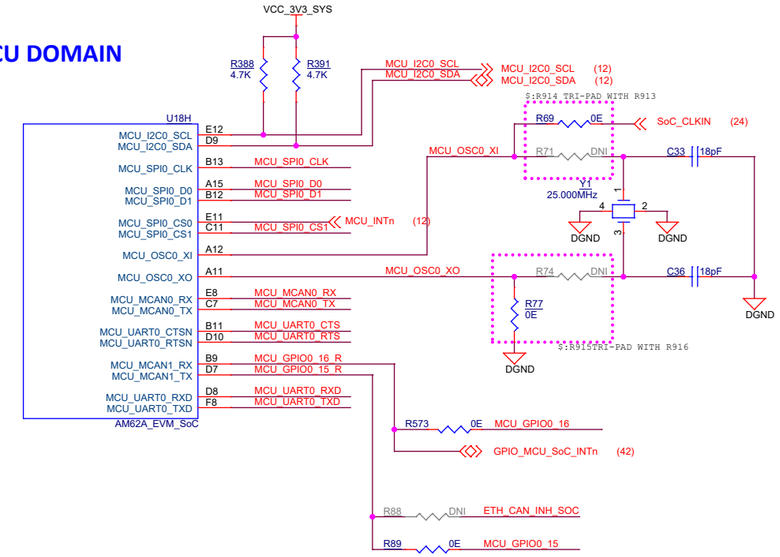
5V supply of User Expansion Connector is limited to sourcing 155mA max.

3V3 supply of User Expansion Connector is limited to sourcing 500mA max.

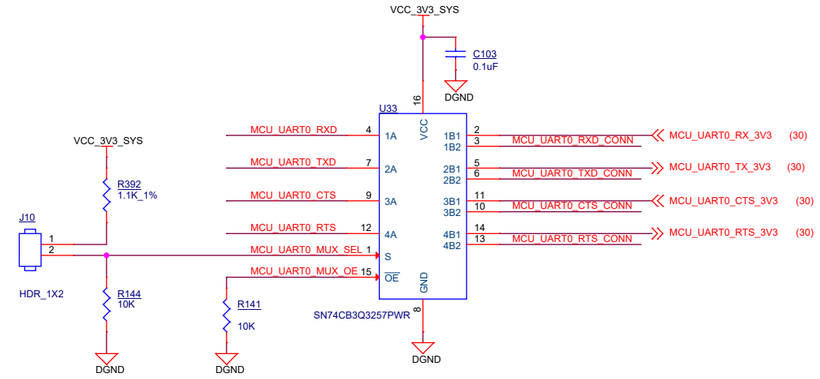
Designed for TI by Mistral Solutions Pvt Ltd

Title	USER EXPANSION CONNECTOR		
Size C	PROC135E1		Rev E1
Date: Wednesday, June 01, 2022		Sheet 32 of 44	

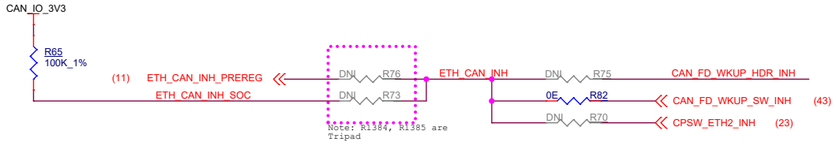
SOC - MCU DOMAIN



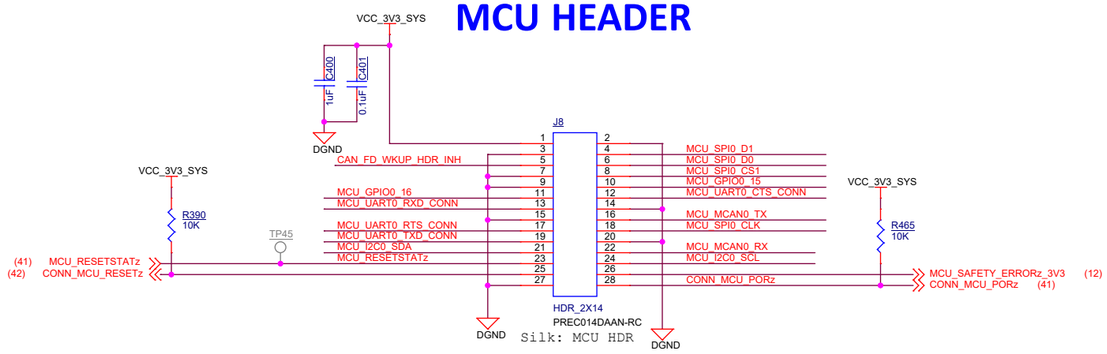
MCU_UART0 MUX

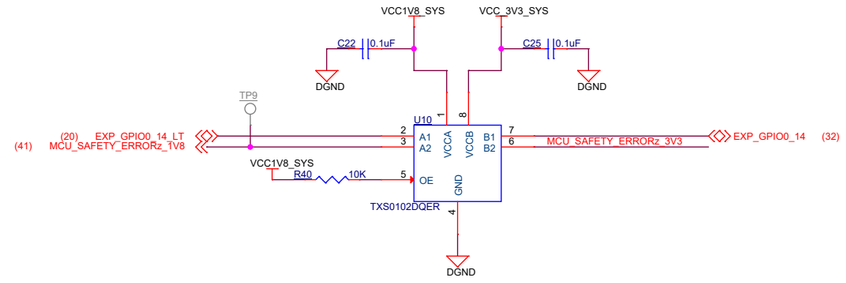


OEn	SEL	INPUT/OUTPUT An	
L	L(DEFAULT)	An=nB1	SOC - FT4232
L	H	An=nB2	SOC - MCU HEADER



MCU HEADER

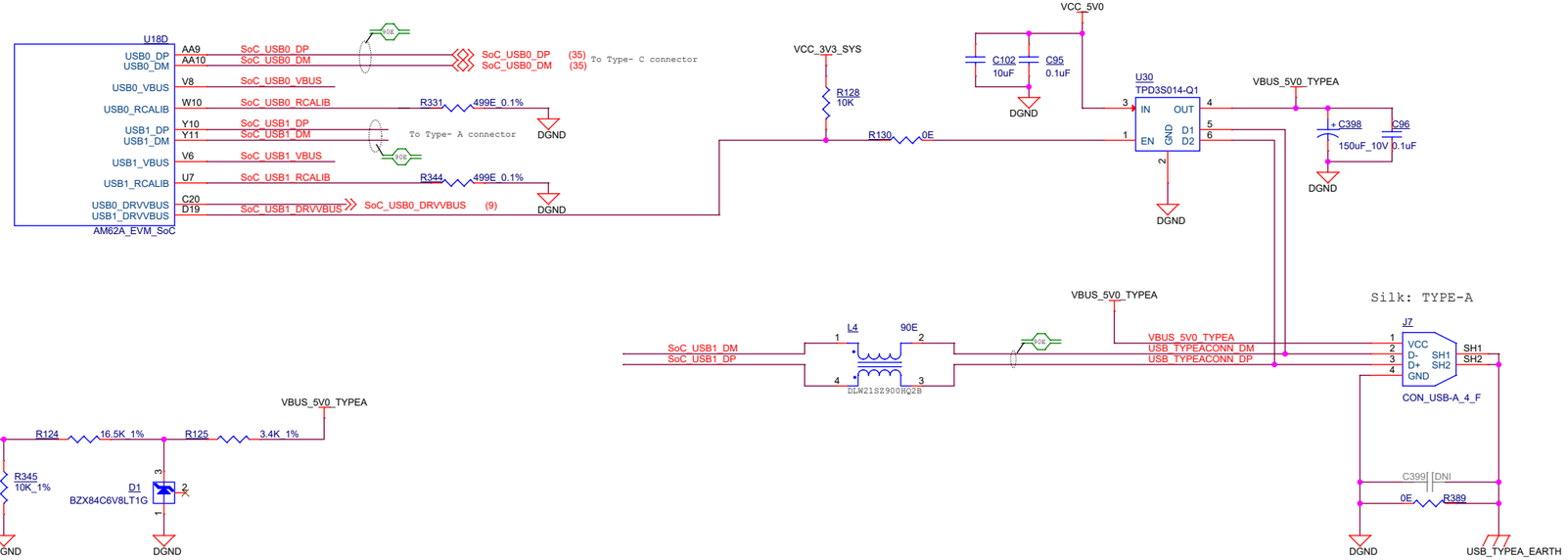




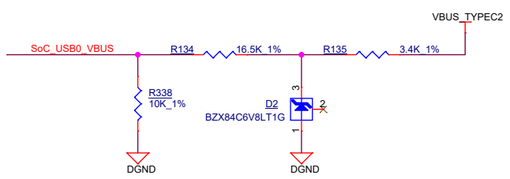
Designed for TI by Mistral Solutions Pvt Ltd

Title	MCU HEADER		
Size C	PROC135E1		Rev E1
Date: Wednesday, June 01, 2022		Sheet 33 of 44	

USB1 TYPE-A



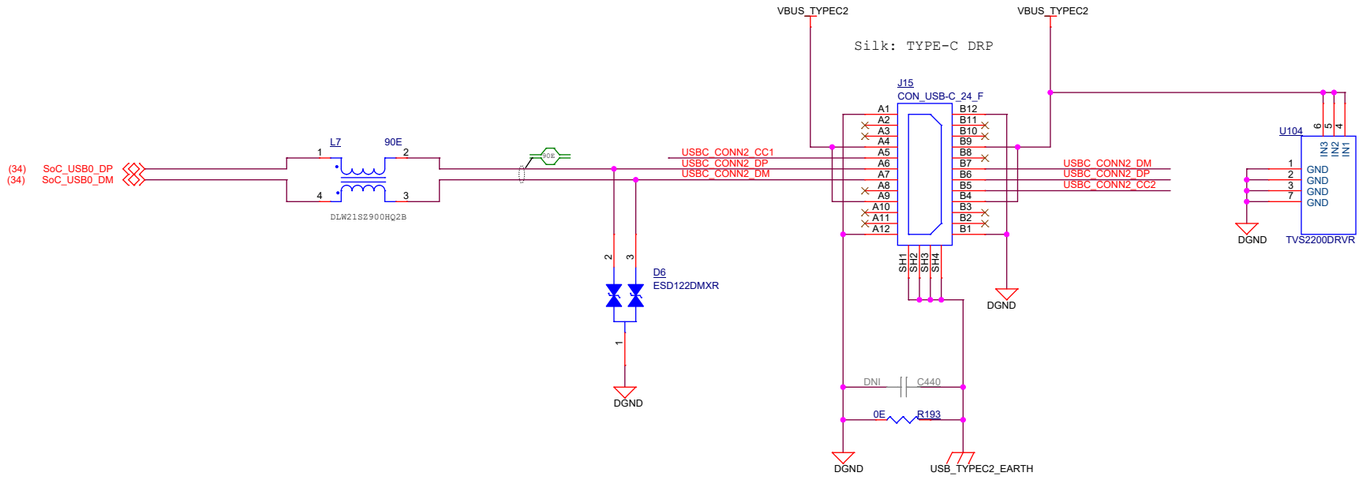
Note: Recommended VBUS circuit for USB connector. Supports 5V-30V VBUS

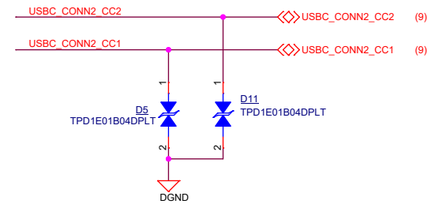


Designed for TI by Mistral Solutions Pvt Ltd

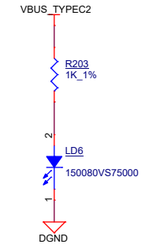
Title	USB1 TYPE-A	
Size C	PROC135E1	Rev E1
Date: Wednesday, June 01, 2022	Sheet 34 of 44	

USB0 TYPE-C DRP

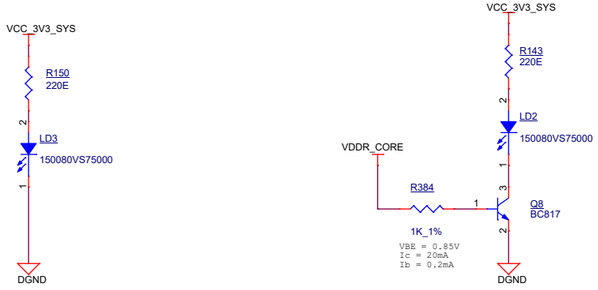




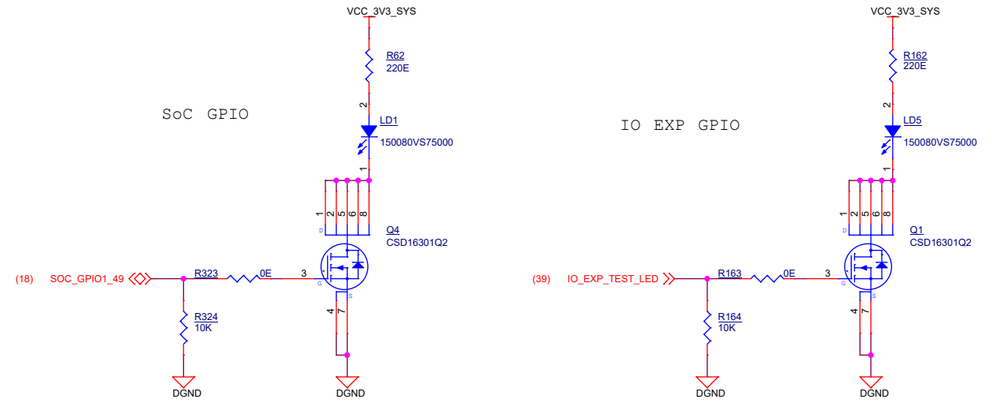
POWER INDICATION LED: VBUS_TYPEC2



POWER RAIL LEDS



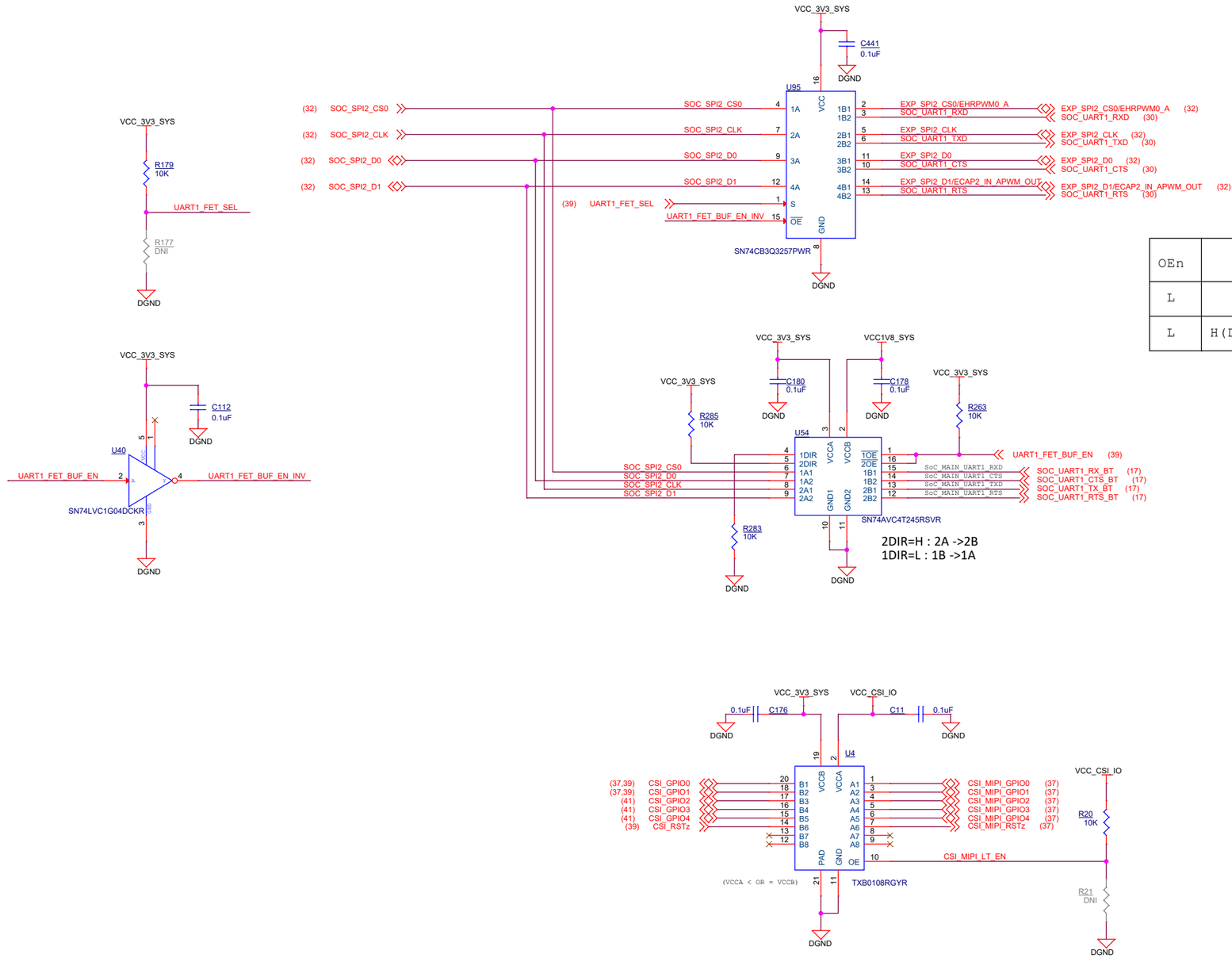
USER TEST LEDS



Designed for TI by Mistral Solutions Pvt Ltd

Title	USB0 TYPE-C DRP & USER TEST LED	
Size: C	PROC135E1	Rev: E1
Date: Wednesday, June 01, 2022	Sheet 35 of 44	

SoC UART1 FET SWITCH & BUFFER

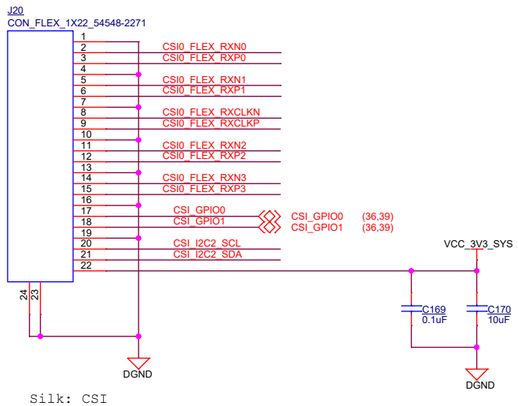


OEn	SEL	INPUT/OUTPUT An	
L	L	An=nB1	SOC - EXP CONN
L	H(DEFAULT)	An=nB2	SOC - FT4232

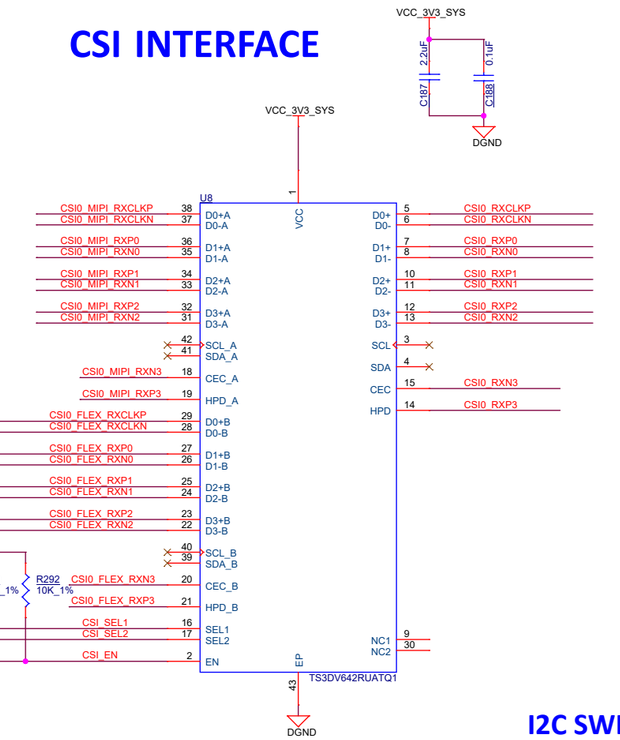
Designed for TI by Mistral Solutions Pvt Ltd

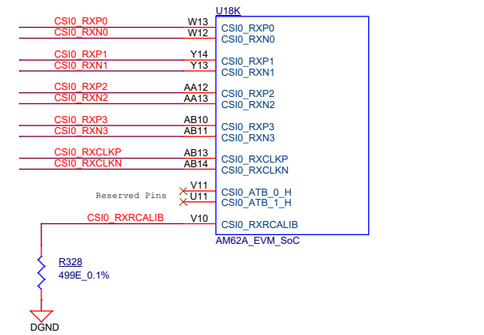
Title	SoC UART1 FET SWITCH & BUFFER		
Size C	PROC135E1		Rev E1
Date:	Wednesday, June 01, 2022	Sheet 36 of 44	

CSI INTERFACE



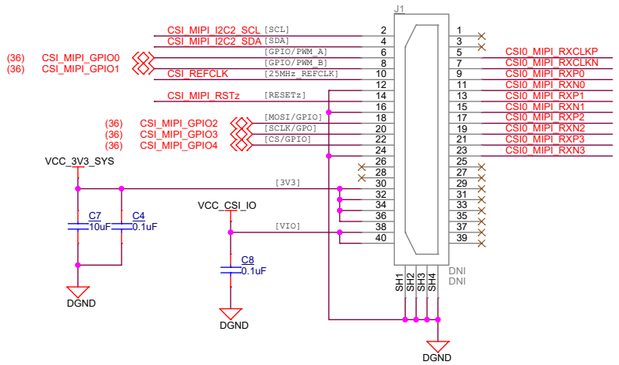
Silk: CSI

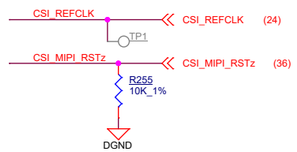


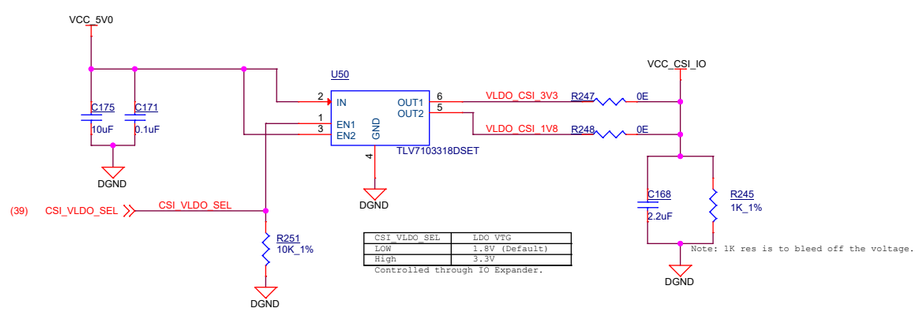


CSI - 1:2 MUX : Truth Table

MUX_SEL_2	FUNCTION	
LOW	INPUT<--A port [CSI2 Connector]	
HIGH	INPUT<--B port [Flex Camera Connector]	(default)





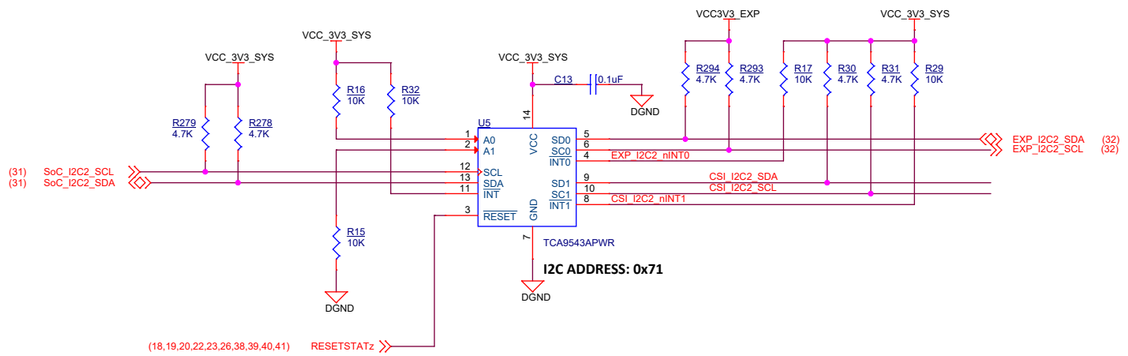


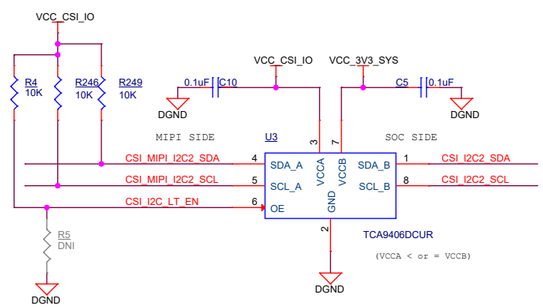
CSI_VLDO_SEL	LDO VTG
LOW	1.8V (Default)
High	3.3V

Controlled through IO Expander.

Note: 1K res is to bleed off the voltage.

I2C SWITCH FOR SoC_I2C2





Designed for TI by Mistral Solutions Pvt Ltd

Title	CSI INTERFACE & USER TEST LEDS	
Size C	PROC135E1	Rev E1
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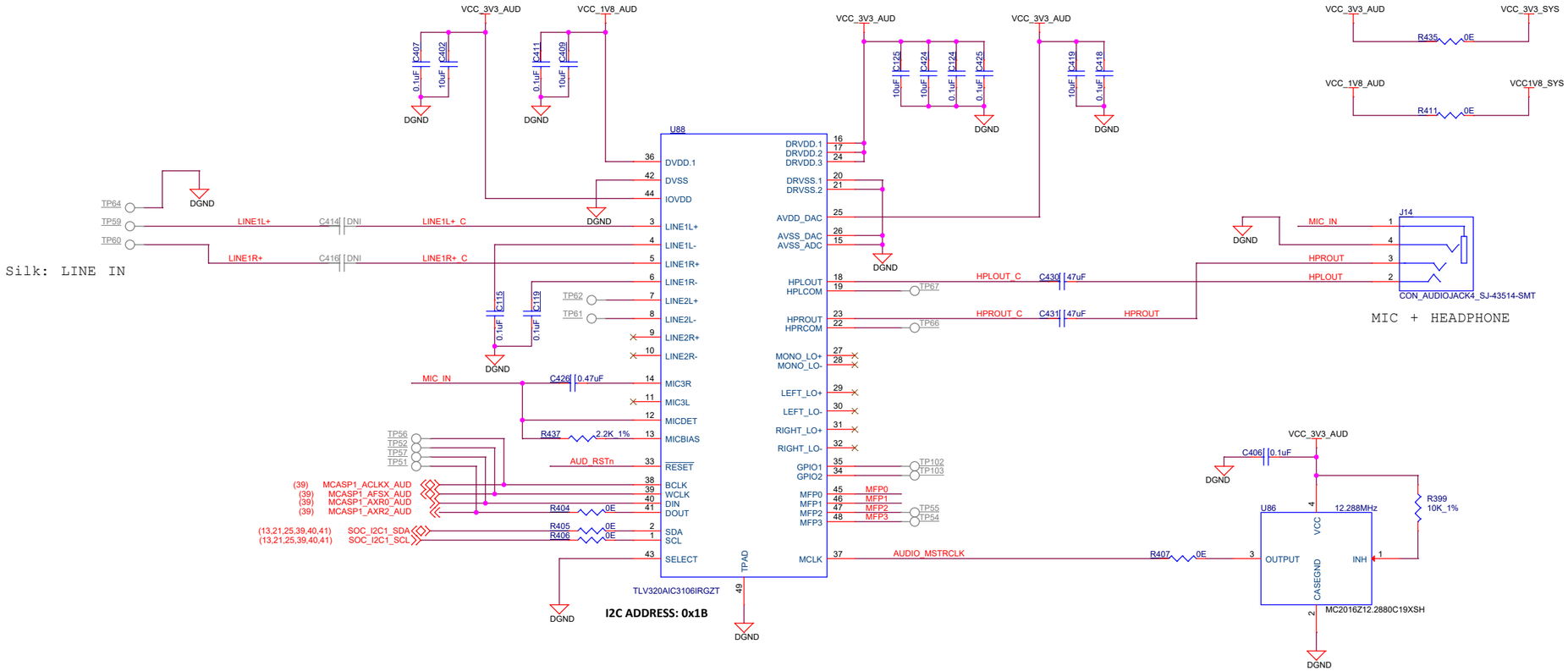
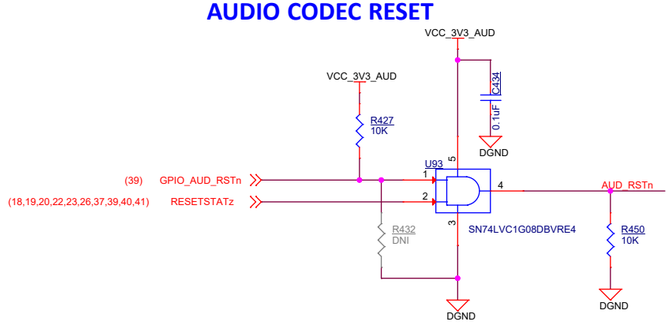
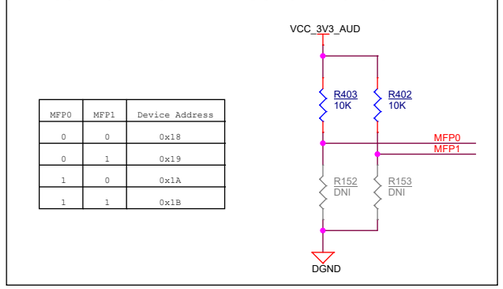
AUDIO CODEC



AUDIO CODEC RESET



CODEC I2C ADDRESS SELECTION

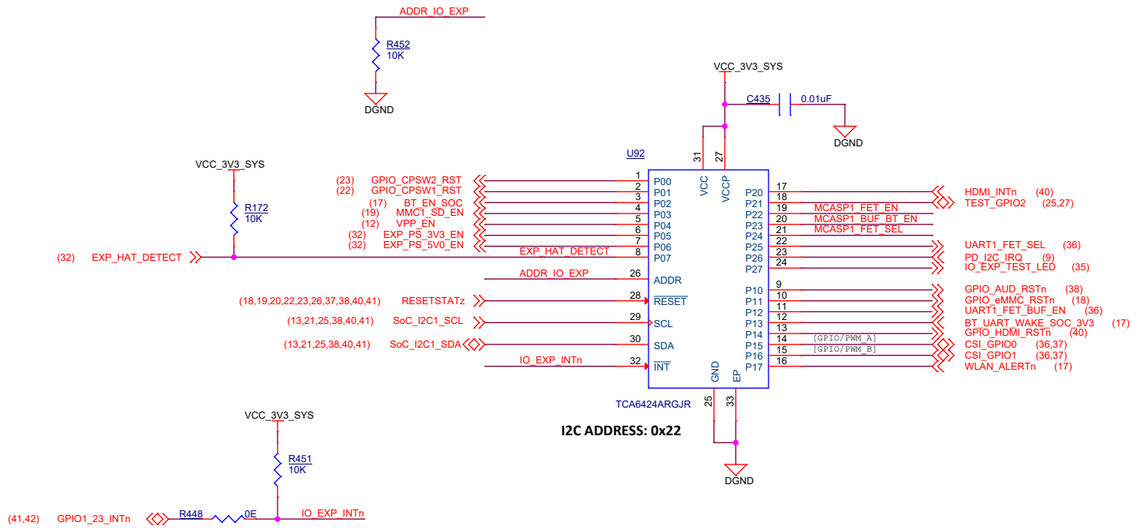


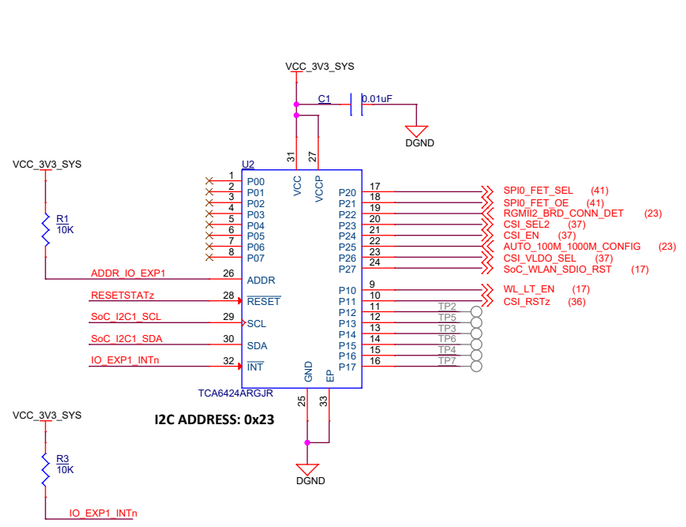
MFP0	MFP1	Device Address
0	0	0x18
0	1	0x19
1	0	0x1A
1	1	0x1B

Designed for TI by Mistral Solutions Pvt Ltd

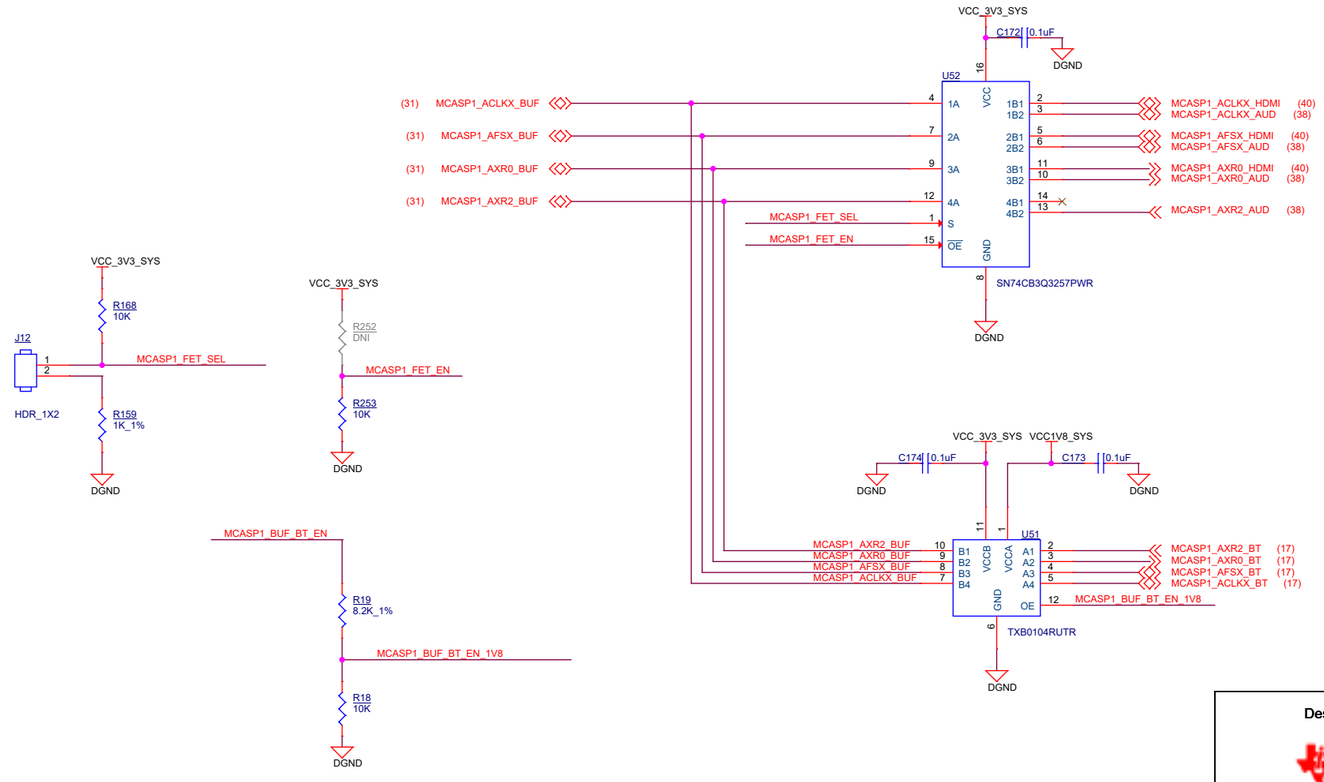
Title	AUDIO CODEC	
Size	PROC135E1	Rev
C		E1
Date:	Wednesday, June 01, 2022	Sheet 38 of 44

IO EXPANDER





McASP1 FET SWITCH & BUFFER

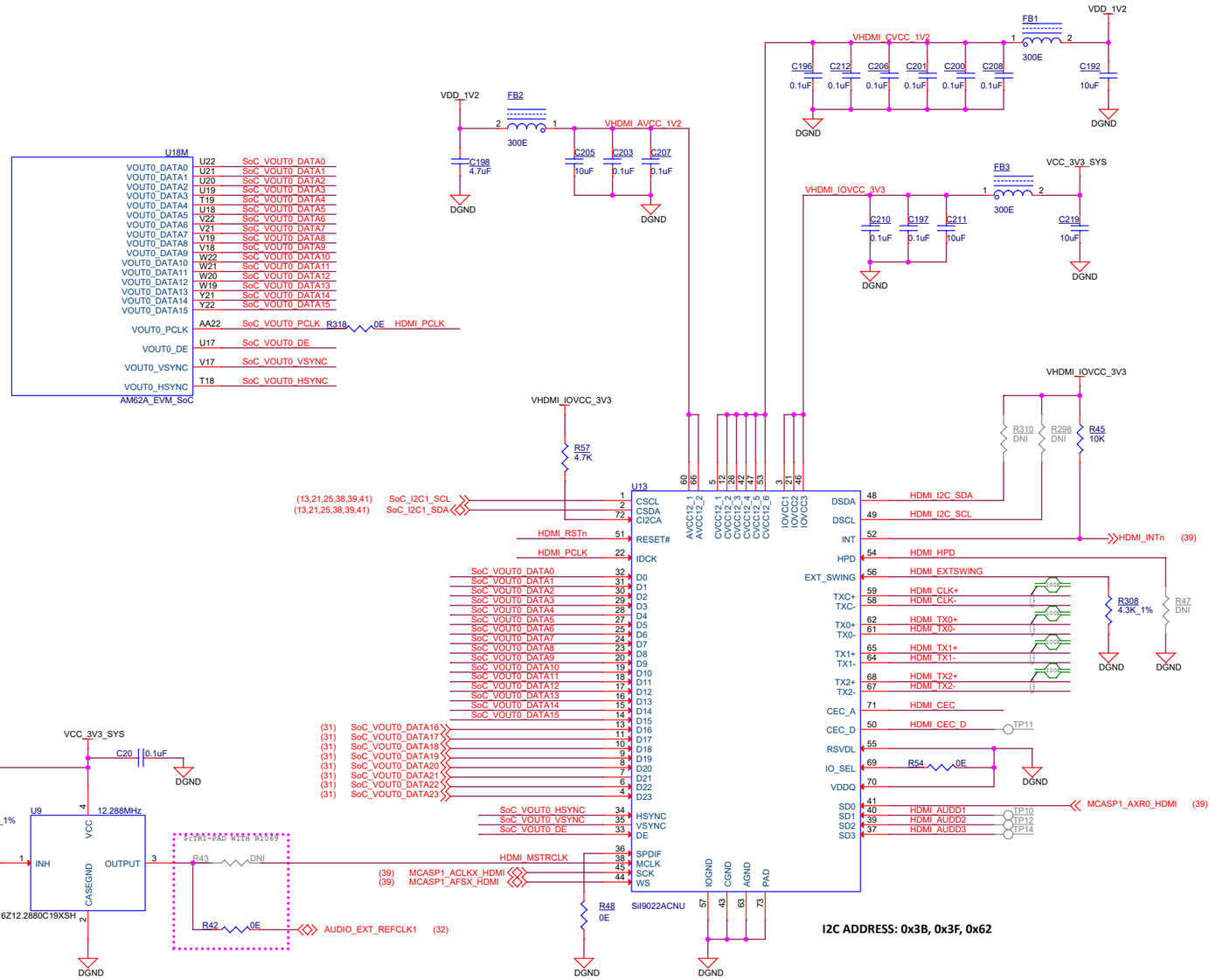


OEn	SEL	INPUT/OUTPUT An	
L	H(DEFAULT)	An=nB2	MCASP1 - CODEC
L	L	An=nB1	MCASP1 - HDMI

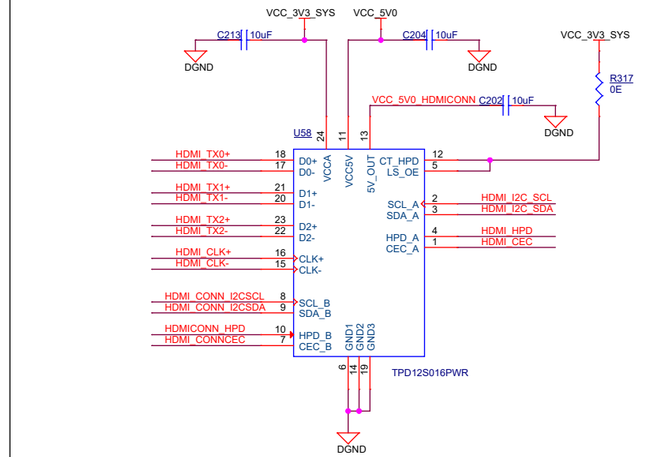
Designed for TI by Mistral Solutions Pvt Ltd

Title	IO EXPANDER	
Size C	PROC135E1	Rev E1
Date: Wednesday, June 01, 2022	Sheet 39 of 44	

HDMI INTERFACE

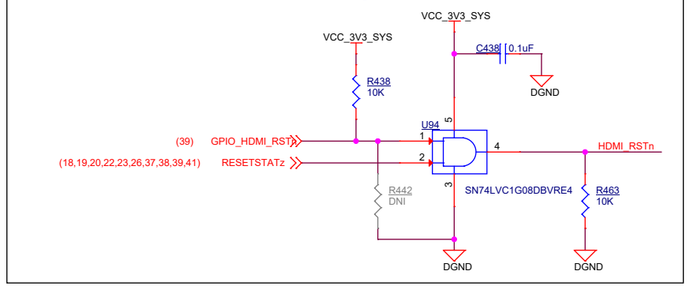


HDMI ESD DEVICE

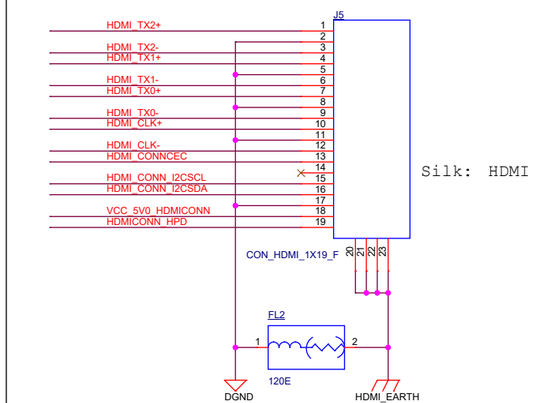


NOTE:
TPD12S016PWR has integrated pullup or pulldown resistors on the I2C and HPD lines hence no external pullup or pulldown required.

HDMI RESET



HDMI CONNECTOR



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Title	HDMI INTERFACE		
Size	C	PROC135E1	Rev E1
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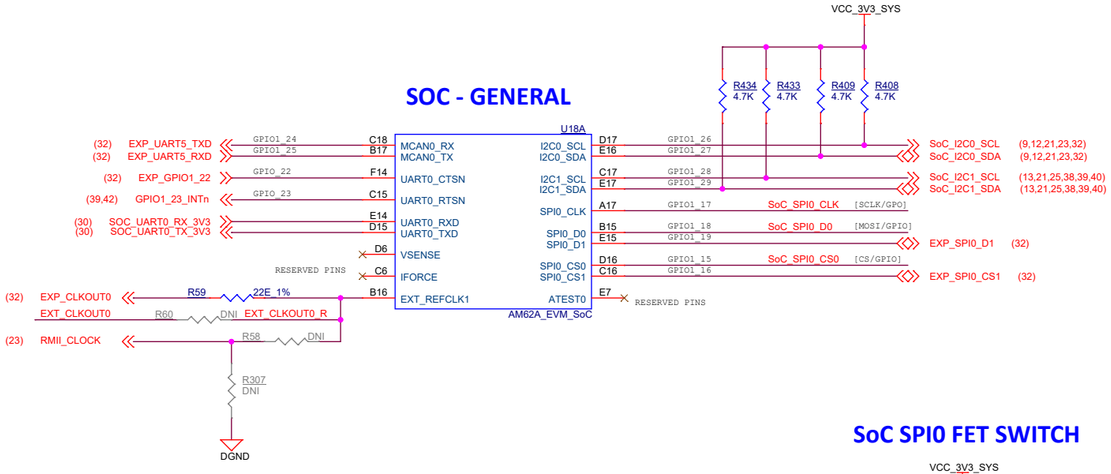
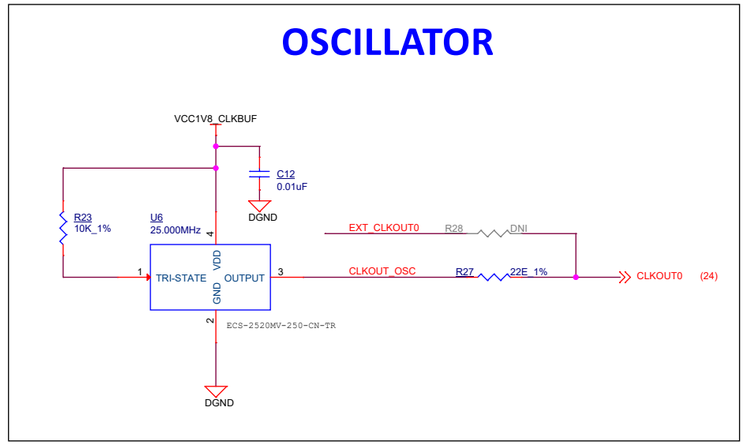
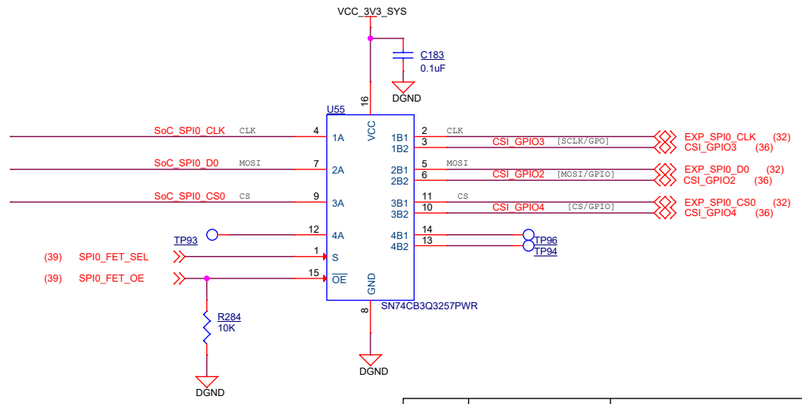
SOC - GENERAL

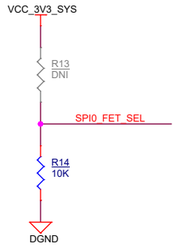


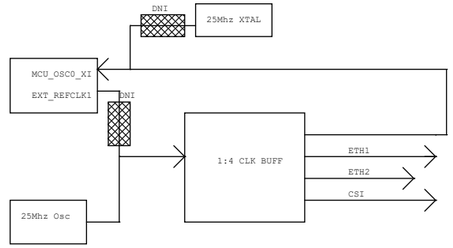
OSCILLATOR



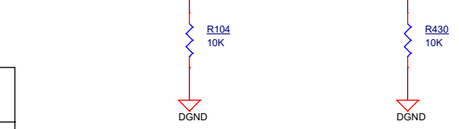
SoC SPI0 FET SWITCH





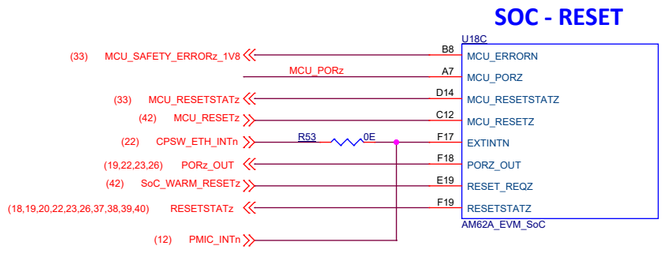


OEn	SEL	INPUT/OUTPUT An	
L	L(DEFAULT)	An=nB1	EXP HDR
L	H	An=nB2	MIPI CSI

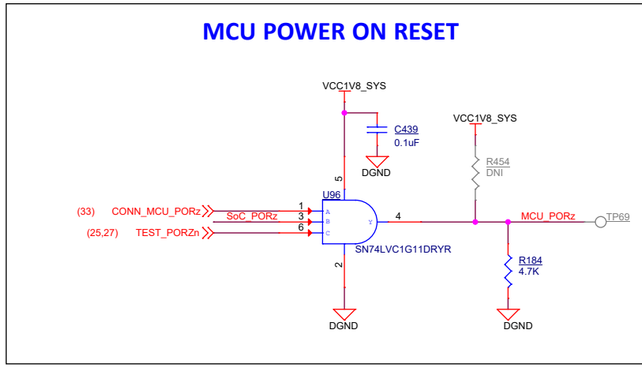


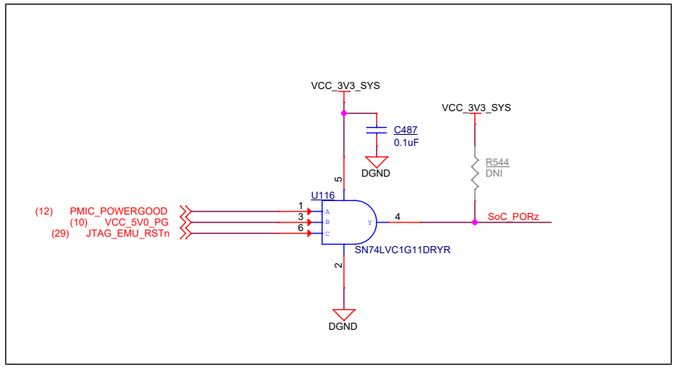
Pull-down resistor on PORz_OUT is provided to keep the signal low until the processor is released from reset during the power-up seqence

SOC - RESET



MCU POWER ON RESET





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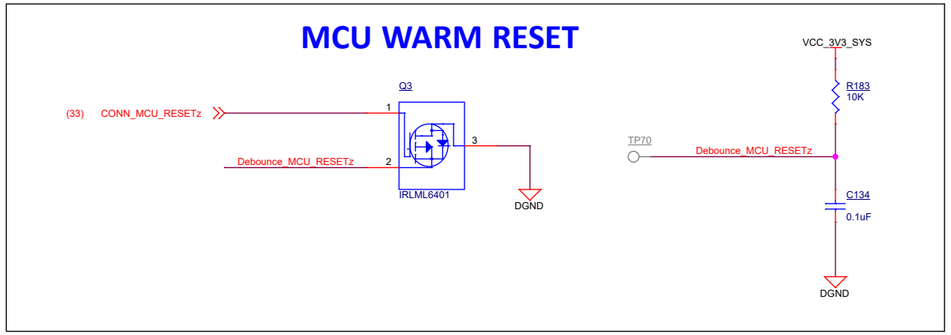
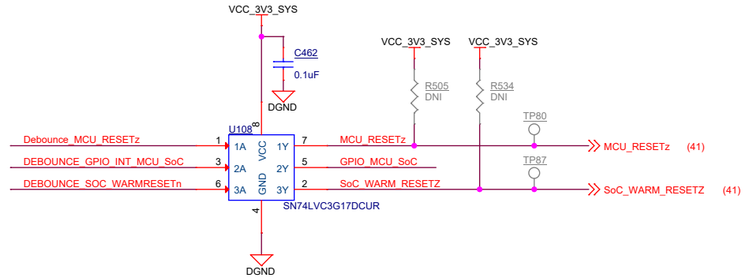
Title	OSCILLATOR		
Size C	PROC135E1		Rev E1
Date:	Wednesday, June 01, 2022	Sheet 41 of 44	

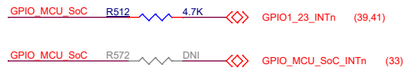
RESET

MCU WARM RESET

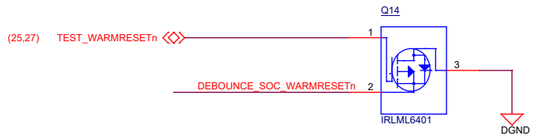


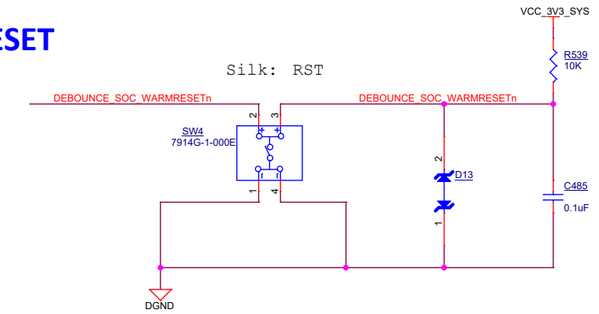
DEBOUNCE CIRCUIT



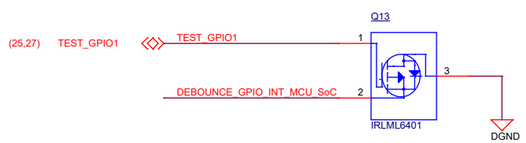


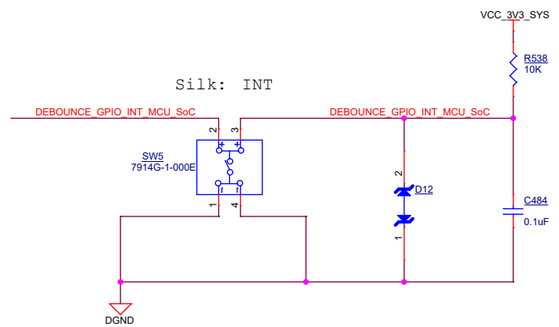
SOC WARM RESET





USER INTERRUPT





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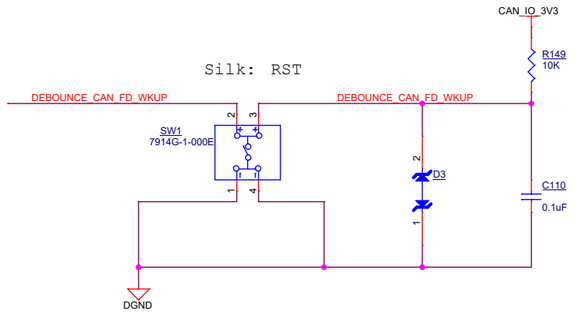
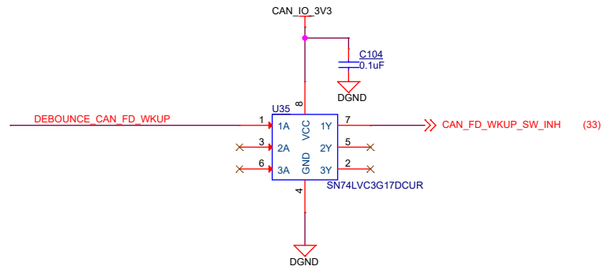
Title	RESET		
Size: C	PROC135E1		Rev: E1
Date: Wednesday, June 01, 2022		Sheet 42 of 44	

CAN-FD FAST WAKE UP SW





Designed for TI by Mistral Solutions Pvt Ltd

Title	CAN FD WKUP SW		
Size	PROC135E1		Rev
C			E1
Date:	Wednesday, June 01, 2022	Sheet 43 of 44	

HARDWARE SCHEMATICS(TBU)

ASSEMBLY NOTES

1. All MSL components should be baked as per JEDEC standard.

2. PCB should be baked at 120 degree for 8 hours.

3. Board assembly must comply with workmanship standards. IPC-A-610 Class 2, unless otherwise specified.

4. These assemblies are ESD sensitive, ESD precautions shall be observed.

5. These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.

6. Provide serial numbers to the assembled boards for identification.

7. The assembled board are wrapped in ESD Covers(individual) and packed securely before shipment.

BARE PCB(TBU)

PROC114

PROC124E1

AM62A SOCKET

ACC1

GT-BGA-2001

LOGOs

PCB LOGO DNI — Texas Intruments

PCB LOGO DNI — For Evaluation only; not FCC approved for resale

PCB LOGO DNI — WEEE Mark

PCB LOGO DNI — CE Mark

PCB LOGO DNI — High Temperature

JUMPERS

ACC2 — SPC02SYAN

ACC3 — SPC02SYAN

FIDUCIALS

FID1 DNI

FID2 DNI

FID3 DNI

FID4 DNI

FID5 DNI

FID6 DNI

LABELS(TBU)

Board Serial No.

LBL1 — PCB LABEL — DNI

Assembly Revision

LBL2 — PCB LABEL — DNI

SCREW & WASHER FOR PCIe M.2

ACC4 — 9774015243R

MH3 — 3356

MH5 — MPMS 002 0005 PH

ACC5 — 9774015243R

MH4 — 3356

MH6 — MPMS 002 0005 PH

Designed for TI by Mistral Solutions Pvt Ltd

Title	HARDWARE SCHEMATICS	
Size C	PROC135E1	Rev E1
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