1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

REV	ECN	DESCRIPTION OF REVISION	CK APPD / DATE
<REV>	<ECN>	<ECO_DESCRIPTION>	<ECODATE>

J44 MLB-4GB SCHEMATIC
08/20/2013

ALIASES RESOLVED

Schematic / PCB #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
051-0052	1	SCHEM,MLB-4GB,J44	SCH	CRITICAL	
820-3536	1	PCBF,MLB-4GB,J44	PCB	CRITICAL	

DRAWING TITLE: <PART_DESCRIPTION>

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

REVISION: <E4LABEL>

BRANCH: <BRANCH>

PAGE: 1 OF 120

SHEET: 1 OF 78

BOM Groups

BOM GROUP	BOM OPTIONS
J44_COMMON	ALTERNATE,COMMON,J44_COMMON1,J44_COMMON2,J44_COMMON3,J44_COMMON4,J44_PROGPARTS
J44_COMMON1	TBTHV:P15V,SKIP_5V3V3:AUDIBLE,SPI:DUAL_IO
J44_COMMON2	EDP,EDP_LS_CAP,CAMERA_3V3:S0,CAM_WAKE:NO,CAM_XTAL:NO,MEM_ODT:PU,VCORE_FETS
J44_COMMON3	XDP,LPCPLUS,BKLT:PROD,CPUTHRM:ALRT,LOADRC:NO,OTHERRC:NO,DDRRC:NO,TBTRC:NO,BMONRC:NO
J44_PROGPARTS	SMC_PROG:PVT,BOOTROM:PVT,TBTROM:PVT,TPAD_PSOC:PROG
ENGISNS	LOADISNS,OTHERISNS,DDRISNS,TBTISNS,BMONISNS

Module Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
337S4596	1	HSWULT,SR18A,PRQ,C0,2.4,28W,2+3,3M,BGA	U0500	CRITICAL	CPU_HSW:2.4G
337S4597	1	HSWULT,SR189,PRQ,C0,2.6,28W,2+3,3M,BGA	U0500	CRITICAL	CPU_HSW:2.6G
337S4598	1	HSWULT,SR188,PRQ,C0,2.8,28W,2+3,4M,BGA	U0500	CRITICAL	CPU_HSW:2.8G
338S1247	1	IC,TBT,FR-4C,A0,PRQ,CIO,SR1JC,FCBGA288	U2800	CRITICAL	
338S1186	1	IC,BCM15700A2,S2 PCIE CAMERA PROCESSOR	U3900	CRITICAL	
376S1194	2	MOSFET,N-CH,30V,15.3A,12M,8P 3.3X3.3 DFN	Q7310,Q7320	CRITICAL	VCORE_FET:VSHY
376S1193	2	MOSFET,N-CH,30V,22A,6.0M,8P 3.3X3.3 DFN	Q7311,Q7321	CRITICAL	VCORE_FET:VSHY
376S0964	2	MOSFET,N-CH,25V,30A,9.6M,8P 3.3X3.3 DFN	Q7310,Q7320	CRITICAL	VCORE_FET:REN
376S1104	2	MOSFET,N-CH,25V,30A,6.1M,8P 3.3X3.3 DFN	Q7311,Q7321	CRITICAL	VCORE_FET:REN

Programmables (All Builds)

TBT

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
341S3918	1	EPROM,FALCON RIDGE (V13.7) J44	U2890	CRITICAL	TBTROM:PVT

SMC

341S3922	1	IC,SMC-B1,EXT(V2.16F39),PVT,J44	U5000	CRITICAL	SMC_PROG:PVT

EFI ROM

341S3924	1	IC,EFI ROM (V0116),PVT,J44	U6100	CRITICAL	BOOTROM:PVT

PSOC

341S3862	1	IC,TRKPD/KYBD PSOC,CU ONLY(V224) J44	U4801	CRITICAL	TPAD_PSOC:PROG

Alternate Parts

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:	
376S1053	376S0604		ALL		Diodes alt to Fairchild
128S0311	128S0329		ALL		NEC alt to Sanyo
138S0739	138S0706		ALL		Samsung alt to Murata
197S0481	197S0480		ALL		Epson alt to NDK
152S0461	152S1645		ALL		Cyntec alt to Vishay
376S1080	376S0820		ALL		Diodes alt to On Semi
155S0667	155S0583		ALL		Panasonic alt to TDK
138S0725	138S0724		ALL		Samsung alt to Murata
376S1032	376S0855		ALL		Toshiba alt for Diodes Dual
376S1129	376S0855		ALL		NXP Alt for Diodes Dual
376S1089	376S1128		ALL		NXP Alt for Diodes Single
353S3452	353S1286		ALL		Maxim alt to Microchip
376S1180	376S0761		ALL		Renesas alt to Vishay
128S0364	128S0264		ALL		Sanyo 2nd Factory alt
107S0254	107S0241		ALL		Cyntec alt to TFT
138S0843	138S0674		ALL		Samsung alt to Murata (BKLT)
138S0803	138S0639		ALL		Samsung alt to Murata (BKLT)
138S0846	138S0811		ALL		Samsung alt to Murata (BKLT)
197S0542	197S0544		ALL		NDK alt to TXC
197S0545	197S0544		ALL		Epson alt to TXC
152S1876	152S1804		ALL		TDK alt to Toko
107S0255	107S0240		ALL		Cyntec alt to TFT
107S0250	107S0248		ALL		Cyntec alt to TFT
127S0164	127S0162		ALL		Rohm alt to Vishay
353S4070	353S4069		ALL		Pericom alt to TI DP Mux U9750
353S4068	353S4069		ALL		NXP alt to TI DP Mux U9750
353S3814	353S3812		ALL		TI alt to NXP
311S0649	311S0541		ALL		ONsemi alt to Toshiba
128S0436	128S0392		ALL		Kemet alt to Sanyo

SYNC_MASTER=J44 SYNC_DATE=08/20/2013

PAGE TITLE: BOM Configuration

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

REVISION: <E4LABEL>

BRANCH: <BRANCH>

PAGE: 2 OF 120

SHEET: 2 OF 78

BOM Variants

BOM NUMBER	BOM NAME	BOM OPTIONS
685-0054	COMMON,MLB-4GB,J44	J44_COMMON
985-0053	DEV,MLB-4GB,J44	XDP_CONN
639-4878	PCBA,MLB-4GB,2.4G,4GB-HYNIX,J44	BASE_BOM,CPU_HSW:2.4G,RAM_4G_HYNIX_H,CAMDRAM:HYNIX_H
639-4879	PCBA,MLB-4GB,2.4G,4GB-ELPIDA,J44	BASE_BOM,CPU_HSW:2.4G,RAM_4G_ELPIDA,CAMDRAM:ELPIDA
639-4880	PCBA,MLB-4GB,2.4G,4GB-MICRON,J44	BASE_BOM,CPU_HSW:2.4G,RAM_4G_MICRON,CAMDRAM:MICRON
639-5272	PCBA,MLB-4GB,2.6G,4GB-HYNIX,J44	BASE_BOM,CPU_HSW:2.6G,RAM_4G_HYNIX_H,CAMDRAM:HYNIX_H
639-5273	PCBA,MLB-4GB,2.6G,4GB-ELPIDA,J44	BASE_BOM,CPU_HSW:2.6G,RAM_4G_ELPIDA,CAMDRAM:ELPIDA
639-5274	PCBA,MLB-4GB,2.6G,4GB-MICRON,J44	BASE_BOM,CPU_HSW:2.6G,RAM_4G_MICRON,CAMDRAM:MICRON
639-5275	PCBA,MLB-4GB,2.8G,4GB-HYNIX,J44	BASE_BOM,CPU_HSW:2.8G,RAM_4G_HYNIX_H,CAMDRAM:HYNIX_H
639-5276	PCBA,MLB-4GB,2.8G,4GB-ELPIDA,J44	BASE_BOM,CPU_HSW:2.8G,RAM_4G_ELPIDA,CAMDRAM:ELPIDA
639-5277	PCBA,MLB-4GB,2.8G,4GB-MICRON,J44	BASE_BOM,CPU_HSW:2.8G,RAM_4G_MICRON,CAMDRAM:MICRON
685-0074	VCORE,FET,VSHY,J44	VCORE_FET:VSHY
685-0075	VCORE,FET,REN,J44	VCORE_FET:REN

DEVELOPMENT/BASE BOM

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
685-0054	1	J44 MLB COMMON BOM	BASE	CRITICAL	BASE_BOM
985-0053	1	J44 MLB DEVEL BOM	DEVEL	CRITICAL	DEVEL_BOM

SUB-BOMS

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
685-0074	1	VCORE,FET,VSHY,J44	VCOREFETS	CRITICAL	VCORE_FETS

Alternate Parts

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
685-0075	685-0074		ALL	RENESAS ALT TO VISHAY

DRAM PARTS

333S0704	8	IC,SDRAM,4GBIT,256MX16,DDR3-1600,F DIE,96FBGA	U2300,U2320,U2340,U2360,U2500,U2520,U2540,U2560	CRITICAL	4G_ELPIDA
333S0700	8	IC,SDRAM,4GBIT,256MX16,DDR3-1600,HUMA,96FBGA	U2300,U2320,U2340,U2360,U2500,U2520,U2540,U2560	CRITICAL	4G_HYNIX_H
333S0698	8	IC,SDRAM,4GBIT,256MX16,DDR3-1600,REV E,96FBGA	U2300,U2320,U2340,U2360,U2500,U2520,U2540,U2560	CRITICAL	4G_MICRON
333S0715	8	IC,SDRAM,4GBIT,256MX16,DDR3-1866,F DIE,96FBGA	U2300,U2320,U2340,U2360,U2500,U2520,U2540,U2560	CRITICAL	4G_ELPIDA_1866
333S0717	8	IC,SDRAM,4GBIT,256MX16,DDR3-1866,HUMA,96FBGA	U2300,U2320,U2340,U2360,U2500,U2520,U2540,U2560	CRITICAL	4G_HYNIX_H_1866
333S0720	8	IC,SDRAM,4GBIT,256MX16,DDR3-1866,REV E,96FBGA	U2300,U2320,U2340,U2360,U2500,U2520,U2540,U2560	CRITICAL	4G_MICRON_1866

DRAM SPD Straps

BOM GROUP	BOM OPTIONS
RAM_4G_ELPIDA	4G_ELPIDA,RAMCFG3:L,RAMCFG2:L,RAMCFG1:L,RAMCFG0:L,PPDDR:1V35
RAM_4G_HYNIX_H	4G_HYNIX_H,RAMCFG3:L,RAMCFG2:L,RAMCFG1:L,RAMCFG0:H,PPDDR:1V35
RAM_4G_MICRON	4G_MICRON,RAMCFG3:L,RAMCFG2:L,RAMCFG1:H,RAMCFG0:L,PPDDR:1V35
RAM_4G_ELPIDA_1866	4G_ELPIDA_1866,RAMCFG3:L,RAMCFG2:L,RAMCFG1:L,RAMCFG0:L,PPDDR:1V5
RAM_4G_HYNIX_H_1866	4G_HYNIX_H_1866,RAMCFG3:L,RAMCFG2:L,RAMCFG1:L,RAMCFG0:H,PPDDR:1V5
RAM_4G_MICRON_1866	4G_MICRON_1866,RAMCFG3:L,RAMCFG2:L,RAMCFG1:H,RAMCFG0:L,PPDDR:1V5

NOTE: 1866 PARTS BEING STRAPPED TO RUN AT 1600

13" MBP VARIABLE BOM GROUPS

BOM GROUP	BOM OPTIONS
J44_COMMON4	SMCBOARDID:8

DRAM SPD Straps

BOM GROUP	BOM OPTIONS
CAMDRAM:HYNIX_H	CAMDRAM_TYPE:HYNIX_H
CAMDRAM:ELPIDA	CAMDRAM_TYPE:ELPIDA
CAMDRAM:MICRON	CAMDRAM_TYPE:MICRON

DRAM Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
333S0700	1	IC,SDRAM,4GBIT,DDR3L-1600,HUMA,96B FBGA	U4000	CRITICAL	CAMDRAM_TYPE:HYNIX_H
333S0704	1	IC,SDRAM,4GBIT,DDR3L-1600,DIE F,96B FBGA	U4000	CRITICAL	CAMDRAM_TYPE:ELPIDA
333S0698	1	IC,SDRAM,4GBIT,DDR3L-1600,REV E,96B FBGA	U4000	CRITICAL	CAMDRAM_TYPE:MICRON

SYNC_MASTER=J44 SYNC_DATE=01/03/2013

PAGE TITLE: BOM Configuration

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

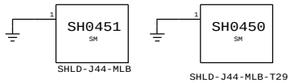
REVISION <E4LABEL>

BRANCH <BRANCH>

PAGE 3 OF 120

SHEET 3 OF 78

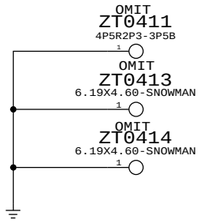
Shield Cans



USB Cage

TBT Cage

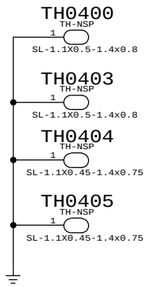
Mounting Holes & Slots



ABOVE GUMSTICK CARD IN MIDDLE OF BOARD
(998-1195)

SNOWMAN-SHAPED SLOT AT LEFT OF MEMORY BANK
(998-5879)

SNOWMAN-SHAPED SLOT AT RIGHT OF MEMORY BANK
(998-5879)



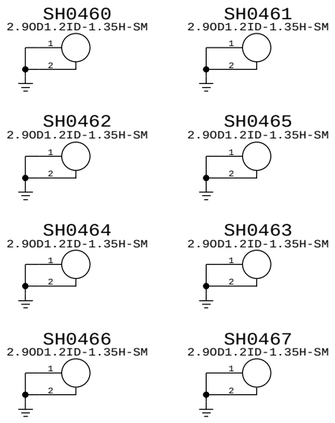
Upper TBT can Ground slot
(862-0118)

Lower TBT can Ground slot
(862-0118)

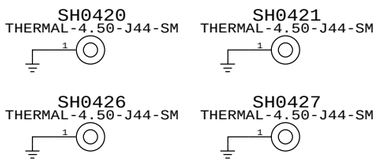
USB can Ground slot
(998-3975)

USB can Ground slot
(998-3975)

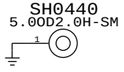
Rubber Mount Standoffs (860-1448)



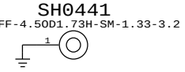
THERMAL MODULE STANDOFF (860-1645)



SSD STANDOFF (806-5375)



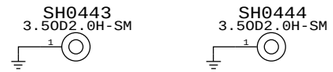
FAN STANDOFF (806-5376)



POGO PINS (870-2451)

SH0435 & SH0436 removed.

RIO FLEX BRACKET BOSSES (860-2354)



SYNC_MASTER=J44 SYNC_DATE=08/12/2013

PAGE TITLE: PD Parts

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

REVISION: <E4LABEL>

BRANCH: <BRANCH>

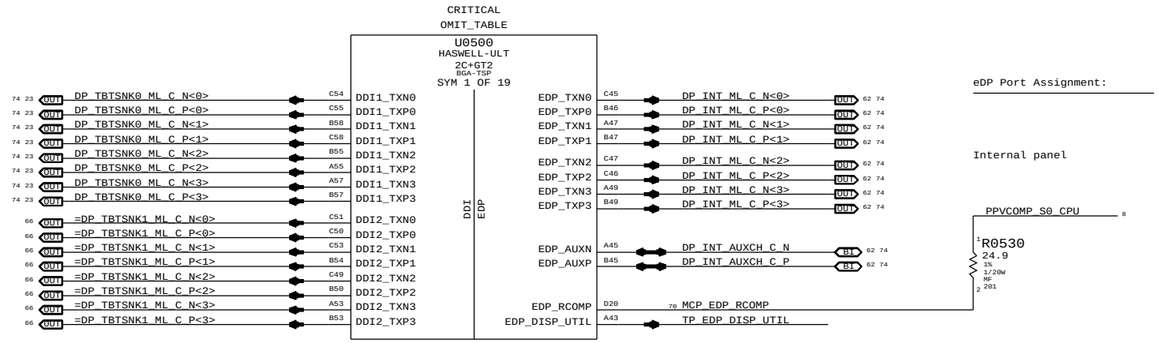
PAGE: 4 OF 120

SHEET: 4 OF 78

DDI Port Assignments:

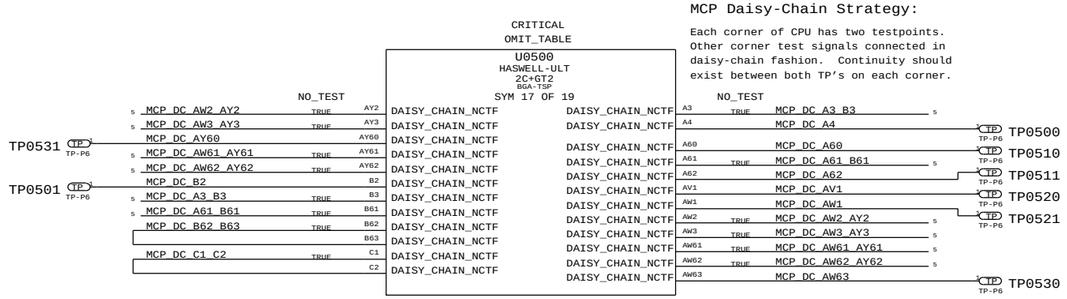
TBT Sink 0

TBT Sink 1
(MUXed with HDMI
if necessary)



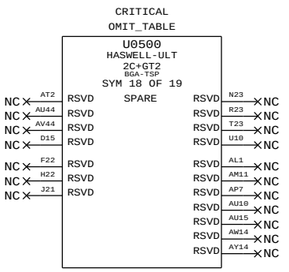
eDP Port Assignment:

Internal panel



MCP Daisy-Chain Strategy:

Each corner of CPU has two testpoints. Other corner test signals connected in daisy-chain fashion. Continuity should exist between both TP's on each corner.



SYNC_MASTER=J44 SYNC_DATE=08/12/2013

PAGE TITLE: CPU GFX/NCTF/RSVD

Apple Inc.

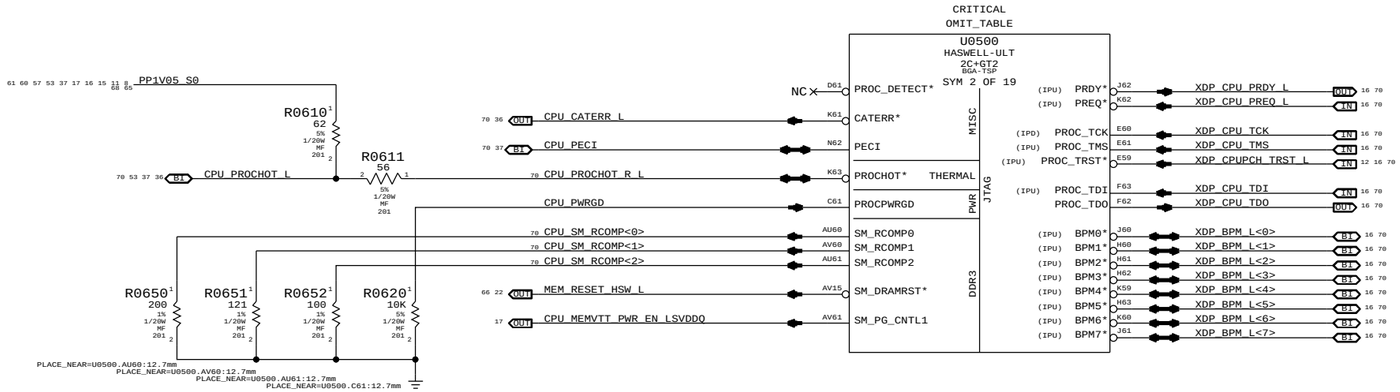
DRAWING NUMBER: <SCH_NUM> SIZE: D

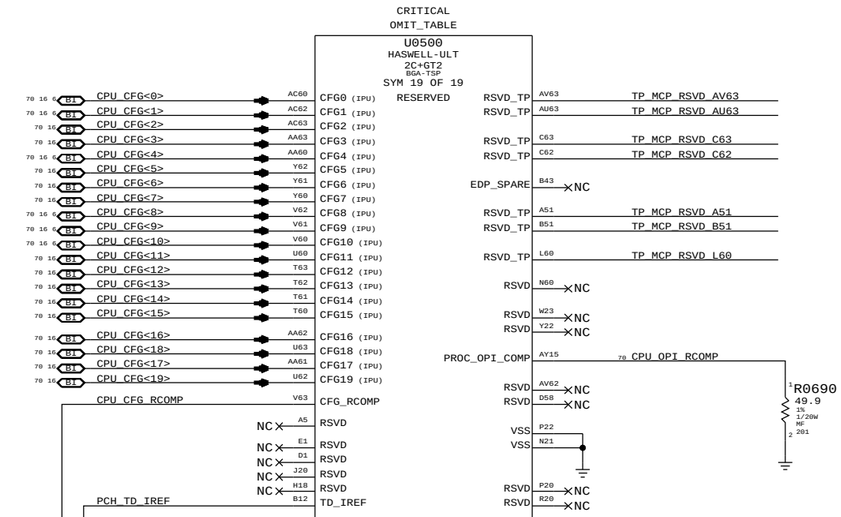
REVISION: <E4LABEL>

BRANCH: <BRANCH>

PAGE: 5 OF 120

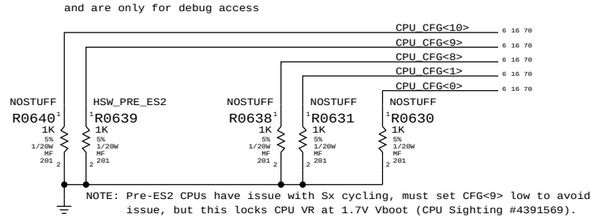
SHEET: 5 OF 78



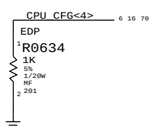


CFG<10>:SAFE MODE BOOT	1 = NORMAL OPERATION	0 = POWER FEATURES NOT ACTIVE
CFG<9> :NO SVID-CAPABLE VR	1 = VR SUPPORTS SVID	0 = VR DOES NOT SUPPORT SVID
CFG<8> :ALLOW NOA ON LOCKED UNITS	1 = NORMAL OPERATION	0 = NOA ALWAYS UNLOCKED
CFG<4> :eDP ENABLE/DISABLE	1 = DISABLED	0 = ENABLED
CFG<1> :PCH-LESS MODE	1 = NORMAL OPERATION	0 = PCH-LESS MODE
CFG<0> :RESET SEQUENCE STALL	1 = NORMAL OPERATION	0 = STALL AFTER PCU PLL LOCK

These can be placed close to J1800
and are only for debug access



NOTE: Pre-ES2 CPUs have issue with Sx cycling, must set CFG<9> low to avoid issue, but this locks CPU VR at 1.7V Vboot (CPU Sighting #4391569).



SYNC_MASTER=J44 SYNC_DATE=08/12/2013

PAGE TITLE

CPU Misc/JTAG/CFG/RSVD

Apple Inc.

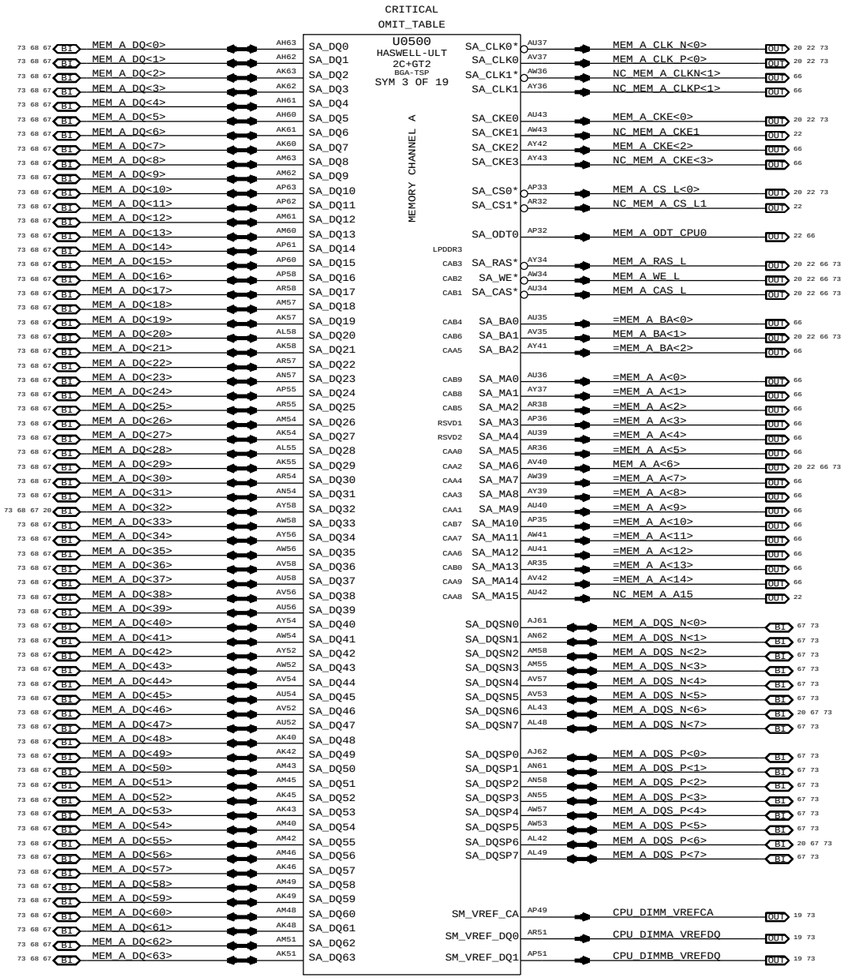
DRAWING NUMBER <SCH_NUM> SIZE D

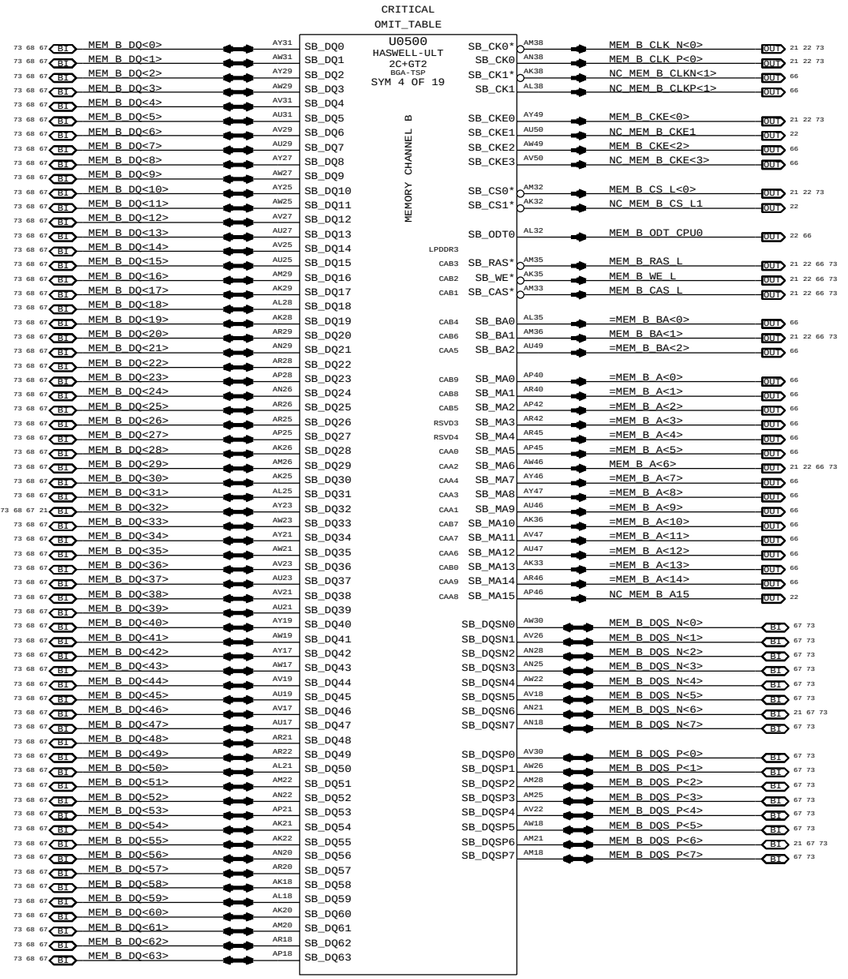
REVISION <E4LABEL>

BRANCH <BRANCH>

PAGE 6 OF 120

SHEET 6 OF 78





SYNC_MASTER=J44 SYNC_DATE=08/12/2013

PAGE TITLE

CPU DDR3/LPDDR3 Interfaces

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

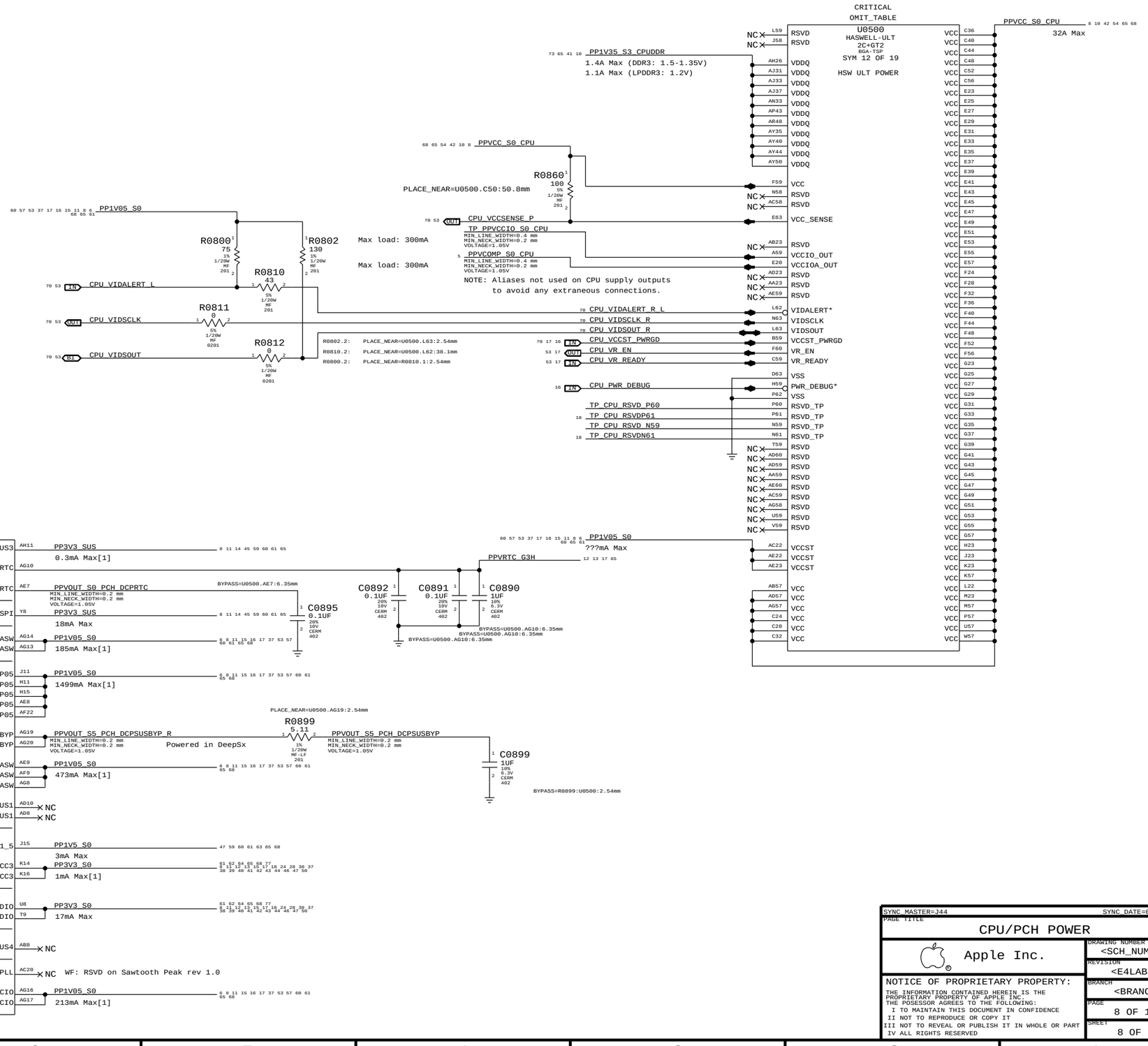
REVISION <E4LABEL>

BRANCH <BRANCH>

PAGE 7 OF 120

SHEET 7 OF 78

HSW-ULT current estimates from Haswell Mobile ULT Processor EDS vol 1, doc #502406, v0.9.
LPT-LP current estimates from Lynx Point-LP PCH EDS, doc #503118, v1.0.
Note [1] current numbers from clarification email, from Srini, dated 9/10/2012 2:11pm.



SYNC_MASTER=J44	SYNC_DATE=08/12/2013
PAGE TITLE	CPU/PCH POWER
	Apple Inc.
DRAWING NUMBER	<SCH_NUM>
SIZE	D
REVISION	<E4LABEL>
BRANCH	<BRANCH>
PAGE	8 OF 120
SHEET	8 OF 78

CRITICAL
OMIT_TABLE

U0500
HASWELL-ULT
2C+GT2
BGA-TSP
SYM 14 OF 19

A11	VSS	VSS	AJ35
A14	VSS	VSS	AJ39
A18	VSS	VSS	AJ41
A24	VSS	VSS	AJ43
A28	VSS	VSS	AJ45
A32	VSS	VSS	AJ47
A36	VSS	VSS	AJ50
A40	VSS	VSS	AJ52
A44	VSS	VSS	AJ54
A48	VSS	VSS	AJ56
A52	VSS	VSS	AJ58
A56	VSS	VSS	AJ60
AA1	VSS	VSS	AJ63
AA58	VSS	VSS	AK23
AB10	VSS	VSS	AK3
AB20	VSS	VSS	AK52
AB22	VSS	VSS	AL10
AB7	VSS	VSS	AL13
AC61	VSS	VSS	AL17
AD21	VSS	VSS	AL20
AD3	VSS	VSS	AL22
AD63	VSS	VSS	AL23
AE10	VSS	VSS	AL26
AE5	VSS	VSS	AL29
AE58	VSS	VSS	AL31
AF11	VSS	VSS	AL33
AF12	VSS	VSS	AL36
AF14	VSS	VSS	AL39
AF15	VSS	VSS	AL40
AF17	VSS	VSS	AL45
AF18	VSS	VSS	AL46
AG1	VSS	VSS	AL51
AG11	VSS	VSS	AL52
AG21	VSS	VSS	AL54
AG23	VSS	VSS	AL57
AG60	VSS	VSS	AL60
AG61	VSS	VSS	AL61
AG62	VSS	VSS	AM1
AG63	VSS	VSS	AM17
AH17	VSS	VSS	AM23
AH19	VSS	VSS	AM31
AH20	VSS	VSS	AM52
AH22	VSS	VSS	AN17
AH24	VSS	VSS	AN23
AH28	VSS	VSS	AN31
AH30	VSS	VSS	AN32
AH32	VSS	VSS	AN35
AH34	VSS	VSS	AN36
AH36	VSS	VSS	AN39
AH38	VSS	VSS	AN40
AH40	VSS	VSS	AN42
AH42	VSS	VSS	AN43
AH44	VSS	VSS	AN45
AH49	VSS	VSS	AN46
AH51	VSS	VSS	AN48
AH53	VSS	VSS	AN49
AH55	VSS	VSS	AN51
AH57	VSS	VSS	AN52
AJ13	VSS	VSS	AN60
AJ14	VSS	VSS	AN63
AJ23	VSS	VSS	AN7
AJ25	VSS	VSS	AP10
AJ27	VSS	VSS	AP17
AJ29	VSS	VSS	AP20

CRITICAL
OMIT_TABLE

U0500
HASWELL-ULT
2C+GT2
BGA-TSP
SYM 15 OF 19

AP22	VSS	VSS	AV59
AP23	VSS	VSS	AV8
AP26	VSS	VSS	AW16
AP29	VSS	VSS	AW24
AP3	VSS	VSS	AW33
AP31	VSS	VSS	AW35
AP38	VSS	VSS	AW37
AP39	VSS	VSS	AW4
AP48	VSS	VSS	AW40
AP52	VSS	VSS	AW42
AP54	VSS	VSS	AW44
AP57	VSS	VSS	AW47
AR11	VSS	VSS	AW50
AR15	VSS	VSS	AW51
AR17	VSS	VSS	AW59
AR23	VSS	VSS	AW60
AR31	VSS	VSS	AY11
AR33	VSS	VSS	AY16
AR39	VSS	VSS	AY18
AR43	VSS	VSS	AY22
AR49	VSS	VSS	AY24
AR5	VSS	VSS	AY26
AR52	VSS	VSS	AY30
AT13	VSS	VSS	AY33
AT35	VSS	VSS	AY4
AT37	VSS	VSS	AY51
AT40	VSS	VSS	AY53
AT42	VSS	VSS	AY57
AT43	VSS	VSS	AY59
AT46	VSS	VSS	AY6
AT49	VSS	VSS	B20
AT61	VSS	VSS	B24
AT62	VSS	VSS	B26
AT63	VSS	VSS	B28
AU1	VSS	VSS	B32
AU16	VSS	VSS	B36
AU18	VSS	VSS	B4
AU20	VSS	VSS	B40
AU22	VSS	VSS	B44
AU24	VSS	VSS	B48
AU26	VSS	VSS	B52
AU28	VSS	VSS	B56
AU30	VSS	VSS	B60
AU33	VSS	VSS	C11
AU51	VSS	VSS	C14
AU53	VSS	VSS	C18
AU55	VSS	VSS	C20
AU57	VSS	VSS	C25
AU59	VSS	VSS	C27
AV14	VSS	VSS	C38
AV16	VSS	VSS	C39
AV20	VSS	VSS	C57
AV24	VSS	VSS	D12
AV28	VSS	VSS	D14
AV33	VSS	VSS	D18
AV34	VSS	VSS	D2
AV36	VSS	VSS	D21
AV39	VSS	VSS	D23
AV41	VSS	VSS	D25
AV43	VSS	VSS	D26
AV46	VSS	VSS	D27
AV49	VSS	VSS	D29
AV51	VSS	VSS	D30
AV55	VSS	VSS	D31

CRITICAL
OMIT_TABLE

U0500
HASWELL-ULT
2C+GT2
BGA-TSP
SYM 16 OF 19

D33	VSS	VSS	H17
D34	VSS	VSS	H57
D35	VSS	VSS	J18
D37	VSS	VSS	J22
D38	VSS	VSS	J59
D39	VSS	VSS	J63
D41	VSS	VSS	K1
D42	VSS	VSS	K12
D43	VSS	VSS	L13
D45	VSS	VSS	L15
D46	VSS	VSS	L17
D47	VSS	VSS	L18
D49	VSS	VSS	L20
D5	VSS	VSS	L58
D50	VSS	VSS	L61
D51	VSS	VSS	L7
D53	VSS	VSS	M22
D54	VSS	VSS	M10
D55	VSS	VSS	N3
D57	VSS	VSS	P59
D59	VSS	VSS	P63
D62	VSS	VSS	R10
D8	VSS	VSS	R22
E11	VSS	VSS	R8
E17	VSS	VSS	T1
F20	VSS	VSS	T58
F26	VSS	VSS	U20
F30	VSS	VSS	U22
F34	VSS	VSS	U61
F38	VSS	VSS	U9
F42	VSS	VSS	V10
F46	VSS	VSS	V3
F50	VSS	VSS	V7
F54	VSS	VSS	W20
F58	VSS	VSS	W22
F61	VSS	VSS	Y10
G18	VSS	VSS	Y59
G22	VSS	VSS	Y63
G3	VSS		
G5	VSS	VSS	V58
G6	VSS	VSS	AH46
G8	VSS	VSS	V23
H13	VSS	VSS_SENSE	E62
		VSS	AH16

CPU_VCCSENSE_N → OUT 53 70

R0960
100
5%
1/20W
MF
201
1 2
PLACE_NEAR=U0500.E62:50.8mm

SYNC_MASTER=J44 SYNC_DATE=08/12/2013

PAGE TITLE
CPU/PCH GROUNDS

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D
REVISION <E4LABEL>
BRANCH <BRANCH>
PAGE 9 OF 120
SHEET 9 OF 78

All Intel recommendations from Intel doc #503160 Shark Bay Ultrabook Platform Power Delivery Design Guide Rev 0.9 unless stated otherwise

CPU VCC Decoupling

Intel recommendation (Table 5-1): 23x 22uF 0805 stuff, 7x 22uF 0805 nostuff
Apple implementation : 18x 22uF 0603 stuff, 80x 22uF 0603 nostuff

68 65 54 42 8 PPVCC_S0_CPU

CRITICAL C1000 10UF 20% 4V X6S 0402
CRITICAL C1001 10UF 20% 4V X6S 0402
CRITICAL C1002 10UF 20% 4V X6S 0402
CRITICAL C1003 10UF 20% 4V X6S 0402
CRITICAL C1004 10UF 20% 4V X6S 0402
CRITICAL C1008 10UF 20% 4V X6S 0402
CRITICAL C1009 10UF 20% 4V X6S 0402
CRITICAL C1010 10UF 20% 4V X6S 0402
CRITICAL C1011 10UF 20% 4V X6S 0402
CRITICAL C1012 10UF 20% 4V X6S 0402
CRITICAL C1014 10UF 20% 4V X6S 0402
CRITICAL C105A 10UF 20% 4V X6S 0402
CRITICAL C105B 10UF 20% 4V X6S 0402
CRITICAL C105C 10UF 20% 4V X6S 0402
CRITICAL C105D 10UF 20% 4V X6S 0402
CRITICAL C105E 10UF 20% 4V X6S 0402
CRITICAL C105F 10UF 20% 4V X6S 0402
CRITICAL C1018 10UF 20% 4V X6S 0402
CRITICAL C1019 10UF 20% 4V X6S 0402
CRITICAL C1020 10UF 20% 4V X6S 0402
CRITICAL C1021 10UF 20% 4V X6S 0402
CRITICAL C1030 10UF 20% 4V X6S 0402
CRITICAL C104E 10UF 20% 4V X6S 0402
CRITICAL C104F 10UF 20% 4V X6S 0402
CRITICAL C106D 10UF 20% 4V X6S 0402
CRITICAL C106E 10UF 20% 4V X6S 0402
CRITICAL C1070 10UF 20% 4V X6S 0402
CRITICAL C1072 10UF 20% 4V X6S 0402
CRITICAL C1073 10UF 20% 4V X6S 0402
CRITICAL C1074 10UF 20% 4V X6S 0402
CRITICAL C1075 10UF 20% 4V X6S 0402
CRITICAL C1077 10UF 20% 4V X6S 0402
CRITICAL C1081 10UF 20% 4V X6S 0402
CRITICAL C1082 10UF 20% 4V X6S 0402
CRITICAL C1083 10UF 20% 4V X6S 0402
CRITICAL C1084 10UF 20% 4V X6S 0402
CRITICAL C1085 10UF 20% 4V X6S 0402
CRITICAL C1086 10UF 20% 4V X6S 0402
CRITICAL C1087 10UF 20% 4V X6S 0402
CRITICAL C1088 10UF 20% 4V X6S 0402
CRITICAL C1089 10UF 20% 4V X6S 0402
CRITICAL C1090 10UF 20% 4V X6S 0402
CRITICAL C1091 10UF 20% 4V X6S 0402
CRITICAL C1092 10UF 20% 4V X6S 0402
CRITICAL C1093 10UF 20% 4V X6S 0402
CRITICAL C1094 10UF 20% 4V X6S 0402
CRITICAL C1095 10UF 20% 4V X6S 0402
CRITICAL C1096 10UF 20% 4V X6S 0402
CRITICAL C1097 10UF 20% 4V X6S 0402
CRITICAL C1022 10UF 20% 4V X6S 0402
NO STUFF C1023 10UF 20% 4V X6S 0402
NO STUFF C1024 10UF 20% 4V X6S 0402
NO STUFF C1025 10UF 20% 4V X6S 0402
CRITICAL C1026 10UF 20% 4V X6S 0402
NO STUFF C1027 10UF 20% 4V X6S 0402
NO STUFF C1028 10UF 20% 4V X6S 0402
NO STUFF C1029 10UF 20% 4V X6S 0402
NO STUFF C1032 10UF 20% 4V X6S 0402
NO STUFF C1033 10UF 20% 4V X6S 0402
CRITICAL C1034 10UF 20% 4V X6S 0402
NO STUFF C1035 10UF 20% 4V X6S 0402
NO STUFF C1036 10UF 20% 4V X6S 0402
NO STUFF C1037 10UF 20% 4V X6S 0402
NO STUFF C1038 10UF 20% 4V X6S 0402
NO STUFF C1039 10UF 20% 4V X6S 0402
NO STUFF C1044 10UF 20% 4V X6S 0402
NO STUFF C1045 10UF 20% 4V X6S 0402
NO STUFF C1046 10UF 20% 4V X6S 0402
NO STUFF C1047 10UF 20% 4V X6S 0402
NO STUFF C1048 10UF 20% 4V X6S 0402
NO STUFF C1049 10UF 20% 4V X6S 0402
NO STUFF C1056 10UF 20% 4V X6S 0402
NO STUFF C1057 10UF 20% 4V X6S 0402
NO STUFF C1058 10UF 20% 4V X6S 0402
NO STUFF C1059 10UF 20% 4V X6S 0402
NO STUFF C1062 10UF 20% 4V X6S 0402
NO STUFF C1063 10UF 20% 4V X6S 0402
NO STUFF C1064 10UF 20% 4V X6S 0402
CRITICAL C1065 10UF 20% 4V X6S 0402
NO STUFF C1066 10UF 20% 4V X6S 0402
NO STUFF C1067 10UF 20% 4V X6S 0402
NO STUFF C1068 10UF 20% 4V X6S 0402
NO STUFF C1069 10UF 20% 4V X6S 0402
NO STUFF C1098 10UF 20% 4V X6S 0402
NO STUFF C1099 10UF 20% 4V X6S 0402
NO STUFF C109A 10UF 20% 4V X6S 0402
NO STUFF C109B 10UF 20% 4V X6S 0402
NO STUFF C109C 10UF 20% 4V X6S 0402
NO STUFF C109D 10UF 20% 4V X6S 0402
NO STUFF C109E 10UF 20% 4V X6S 0402
NO STUFF C109F 10UF 20% 4V X6S 0402
NO STUFF C108A 10UF 20% 4V X6S 0402
NO STUFF C108B 10UF 20% 4V X6S 0402
NO STUFF C108C 10UF 20% 4V X6S 0402
NO STUFF C108D 10UF 20% 4V X6S 0402
NO STUFF C108E 10UF 20% 4V X6S 0402
NO STUFF C108F 10UF 20% 4V X6S 0402
NO STUFF C107A 10UF 20% 4V X6S 0402
NO STUFF C107B 10UF 20% 4V X6S 0402

CRITICAL C1031 470UF-0.0045OHM 20% 2.5V POLY-TANT SM

CPU VDDQ DECOUPLING

Intel recommendation (Table 5-4): 2x 2.2uF 0402, 6x 10uF 0603
Apple implementation : 2x 2.2uF 0402, 6x 10uF 0402

73 65 41 8 PP1V35_S3_CPUDDR

C1040 2.2UF 20% 6.3V CERM 402-LF
C1041 2.2UF 20% 6.3V CERM 402-LF
C1042 2.2UF 20% 6.3V CERM 402-LF
C1043 2.2UF 20% 6.3V CERM 402-LF

Added 2 extra 2.2uF per Harris Beach v0.9 schematic

C1050 10UF 20% 6.3V CERM-X5R 0402-1
C1051 10UF 20% 6.3V CERM-X5R 0402-1
C1052 10UF 20% 6.3V CERM-X5R 0402-1
C1053 10UF 20% 6.3V CERM-X5R 0402-1
C1054 10UF 20% 6.3V CERM-X5R 0402-1
C1055 10UF 20% 6.3V CERM-X5R 0402-1

C1060 270UF 20% 2V TANT CASE-B2-SM
NO STUFF C1061 270UF 20% 2V TANT CASE-B2-SM

1x Bulk nostuff, Harris Beach has 2x nostuff

CPU VCC Decoupling

SYNC_MASTER=J44 SYNC_DATE=08/12/2013
PAGE TITLE: CPU Decoupling
Apple Inc.
DRAWING NUMBER: <SCH_NUM> SIZE: D
REVISION: <E4LABEL>
BRANCH: <BRANCH>
PAGE: 10 OF 120
SHEET: 10 OF 78

PCH VCCDSW3_3 BYPASS
(PCH 3.3V DSW PWR)
PP3V3_S5
NO STUFF
C1200 1UF 10% 6.3V CERM 402
BYPASS=U0500.AH10:6.35mm

PCH VCCSPI BYPASS
(PCH 3.3V SPI PWR)
PP3V3_SUS
NO STUFF
C1202 0.1UF 20% 10V CERM 402
BYPASS=U0500.Y8:6.35mm

PCH VCCSUS3_3 BYPASS
(PCH 3.3V SUSPEND PWR)
PP3V3_SUS
C1204 22UF 20% 6.3V X5R-CERM-1 603
BYPASS=U0500.AC9:12.7mm

PCH VCCSUS3_3 BYPASS
(PCH 3.3V SUSPEND RTC PWR)
PP3V3_SUS
C1206 1UF 10% 6.3V CERM 402
BYPASS=U0500.AH11:6.35mm

PCH VCCSDIO BYPASS
(PCH 3.3V/1.8V SDIO PWR)
PP3V3_S0
C1208 1UF 10% 6.3V CERM 402
BYPASS=U0500.U8:6.35mm

PCH VCCSUSHDA BYPASS
(PCH 3.3V/1.5V HDA PWR)
PP1V5_S0SW_AUDIO_HDA
C1210 1UF 10% 6.3V CERM 402
BYPASS=U0500.AH14:6.35mm

PCH VCC3_3 BYPASS
(PCH 3.3V GPIO/LPC PWR)
PP3V3_S0
C1212 22UF 20% 6.3V X5R-CERM-1 603
BYPASS=U0500.V8:12.7mm

PCH VCC3_3 BYPASS
(PCH 3.3V THERMAL PWR)
PP3V3_S0
C1214 0.1UF 20% 10V CERM 402
BYPASS=U0500.K14:6.35mm

PCH VCCASW BYPASS
(PCH 1.05V ME CORE PWR)
PP1V05_S0
NO STUFF
C1250 22UF 20% 6.3V X5R-CERM-1 603
C1251 1UF 10% 6.3V CERM 402
BYPASS=U0500.AE9:12.7mm
BYPASS=U0500.AE9:6.35mm

PCH VCC BYPASS
(PCH 1.05V CORE PWR)
PP1V05_S0
C1255 10UF 20% 6.3V X5R 603
C1256 1UF 10% 6.3V CERM 402
C1257 1UF 10% 6.3V CERM 402
BYPASS=U0500.J11:12.7mm
BYPASS=U0500.J11:6.35mm
BYPASS=U0500.AE8:6.35mm

PCH VCCHSIO BYPASS
(PCH 1.05V PCIe/SATA/USB3 PWR)
PP1V05_S0SW_PCH_HSIO
C1260 1UF 10% 6.3V CERM 402
C1261 1UF 10% 6.3V CERM 402
C1262 10UF 20% 6.3V CERM-X5R 0402-1
BYPASS=U0500.K9:6.35mm
BYPASS=U0500.L10:6.35mm
BYPASS=U0500.M9:6.35mm

PCH VCCIO BYPASS
(PCH 1.05V USB2 PWR)
PP1V05_S0
C1264 1UF 10% 6.3V CERM 402
BYPASS=U0500.AG16:6.35mm

PCH VCCCLK BYPASS
(PCH 1.05V CLK PWR)
PP1V05_S0
C1266 1UF 10% 6.3V CERM 402
C1267 1UF 10% 6.3V CERM 402
BYPASS=U0500.J17:6.35mm
BYPASS=U0500.R21:6.35mm

PP1V05_S0
??mA Max
R1270 0 5% 1/10W MF-LF 402
PP1V05_S0_PCH_VCCACLKPLL_R
MIN_LINE_WIDTH=0.2 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
CRITICAL
L1270 2.2UH-240MA-0.221OHM 0603
C1270 47UF 20% 4V CERM-X5R 0805-1
C1271 47UF 20% 4V CERM-X5R 0805-1
C1272 1UF 10% 10V X5R 402
BYPASS=U0500.A20:12.7mm
BYPASS=U0500.A20:12.7mm
BYPASS=U0500.A20:6.35mm
PCH VCCACLKPLL FILTER/BYPASS
(PCH 1.05V ACLK PLL PWR)
PP1V05_S0_PCH_VCCACLKPLL
MIN_LINE_WIDTH=0.2 MM
MIN_NECK_WIDTH=0.075 MM
VOLTAGE=1.05V
31mA Max

R1275 0 5% 1/10W MF-LF 402
PP1V05_S0_PCH_VCC_ICC_R
MIN_LINE_WIDTH=0.2 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
CRITICAL
L1275 2.2UH-240MA-0.221OHM 0603
C1275 47UF 20% 4V CERM-X5R 0805-1
C1276 47UF 20% 4V CERM-X5R 0805-1
C1277 1UF 10% 10V X5R 402
BYPASS=U0500.J18:12.7mm
BYPASS=U0500.J18:12.7mm
BYPASS=U0500.J18:6.35mm
PCH VCCCLK FILTER/BYPASS
(PCH 1.05V VCCCLK PWR)
PP1V05_S0_PCH_VCC_ICC
MIN_LINE_WIDTH=0.2 MM
MIN_NECK_WIDTH=0.075 MM
VOLTAGE=1.05V
??mA Max

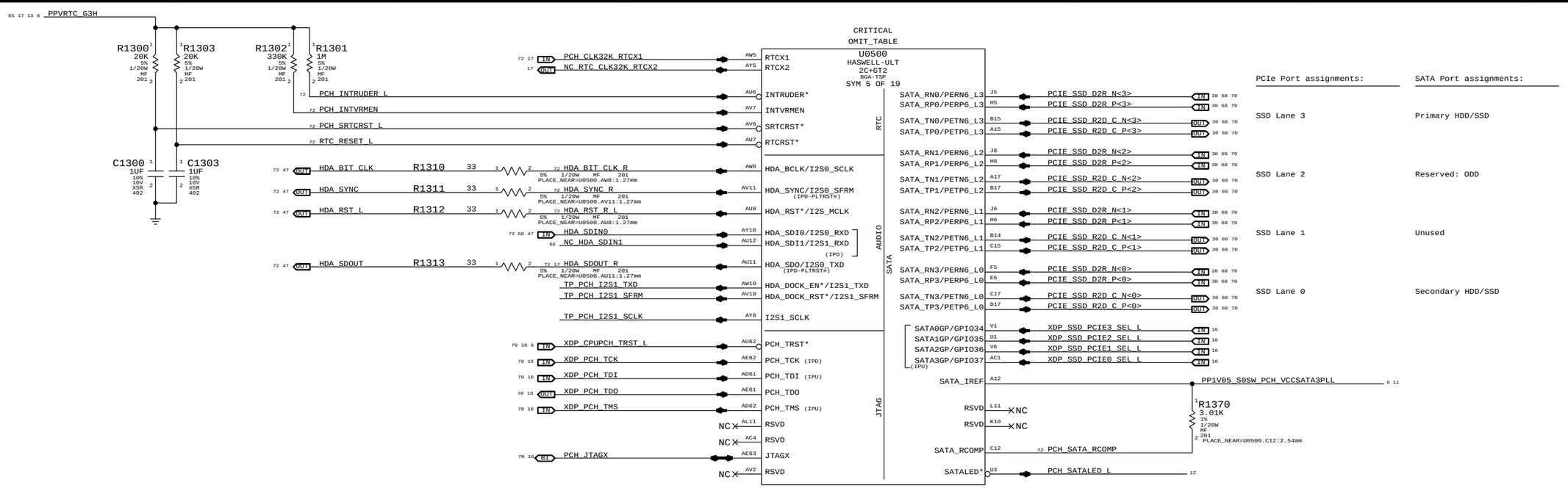
R1280 0 5% 1/10W MF-LF 402
CRITICAL
NO STUFF
L1280 2.2UH-240MA-0.221OHM 0603
C1280 47UF 20% 4V CERM-X5R 0805-1
C1281 47UF 20% 4V CERM-X5R 0805-1
C1282 1UF 10% 10V X5R 402
BYPASS=U0500.AA21:12.7mm
BYPASS=U0500.AA21:12.7mm
BYPASS=U0500.AA21:6.35mm
PCH OPI VCCAPLL FILTER/BYPASS
(PCH 1.05V OPI PLL PWR)
PP1V05_S0_PCH_VCCAPLL_OPI
MIN_LINE_WIDTH=0.2 MM
MIN_NECK_WIDTH=0.075 MM
VOLTAGE=1.05V
57mA Max

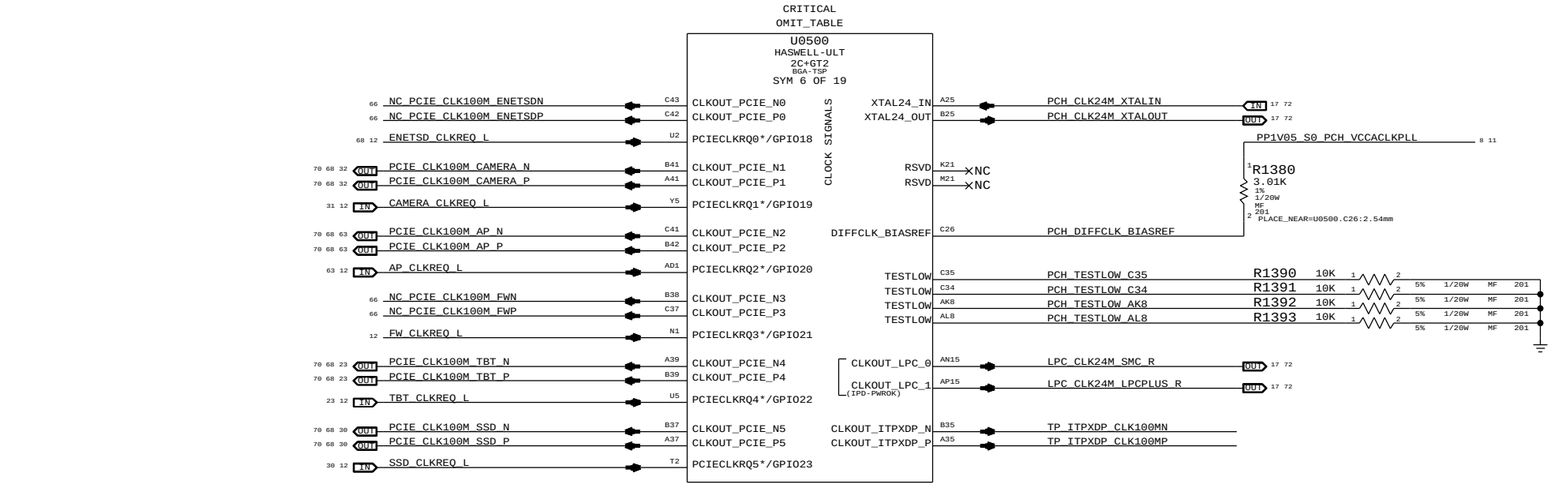
PP1V05_S0SW_PCH_HSIO
83mA Max
CRITICAL
L1290 2.2UH-240MA-0.221OHM 0603
C1290 47UF 20% 4V CERM-X5R 0805-1
C1291 47UF 20% 4V CERM-X5R 0805-1
C1292 1UF 10% 10V X5R 402
BYPASS=U0500.B11:12.7mm
BYPASS=U0500.B11:12.7mm
BYPASS=U0500.B11:6.35mm
PCH VCCSATA3PLL FILTER/BYPASS
(PCH 1.05V SATA3 PLL PWR)
PP1V05_S0SW_PCH_VCCSATA3PLL
MIN_LINE_WIDTH=0.2 MM
MIN_NECK_WIDTH=0.075 MM
VOLTAGE=1.05V
42mA Max

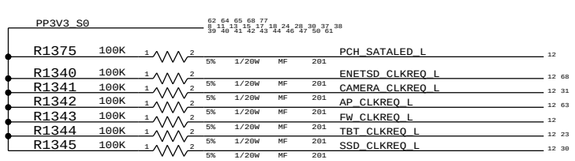
CRITICAL
L1295 2.2UH-240MA-0.221OHM 0603
C1295 47UF 20% 4V CERM-X5R 0805-1
C1296 47UF 20% 4V CERM-X5R 0805-1
C1297 1UF 10% 10V X5R 402
BYPASS=U0500.B18:12.7mm
BYPASS=U0500.B18:12.7mm
BYPASS=U0500.B18:6.35mm
PCH VCCUSB3PLL FILTER/BYPASS
(PCH 1.05V USB3 PLL PWR)
PP1V05_S0SW_PCH_VCCUSB3PLL
MIN_LINE_WIDTH=0.2 MM
MIN_NECK_WIDTH=0.075 MM
VOLTAGE=1.05V
41mA Max

LPT-LP current estimates from Lynx Point-LP PCH EDS, doc #503118, v1.0
as well as from clarification email, from Srini, dated 9/10/2012 2:11pm.

SYNC_MASTER=J44 SYNC_DATE=08/12/2013
PAGE TITLE: PCH Decoupling
Apple Inc.
DRAWING NUMBER: <SCH_NUM> SIZE: D
REVISION: <E4LABEL>
BRANCH: <BRANCH>
PAGE: 12 OF 120
SHEET: 11 OF 78





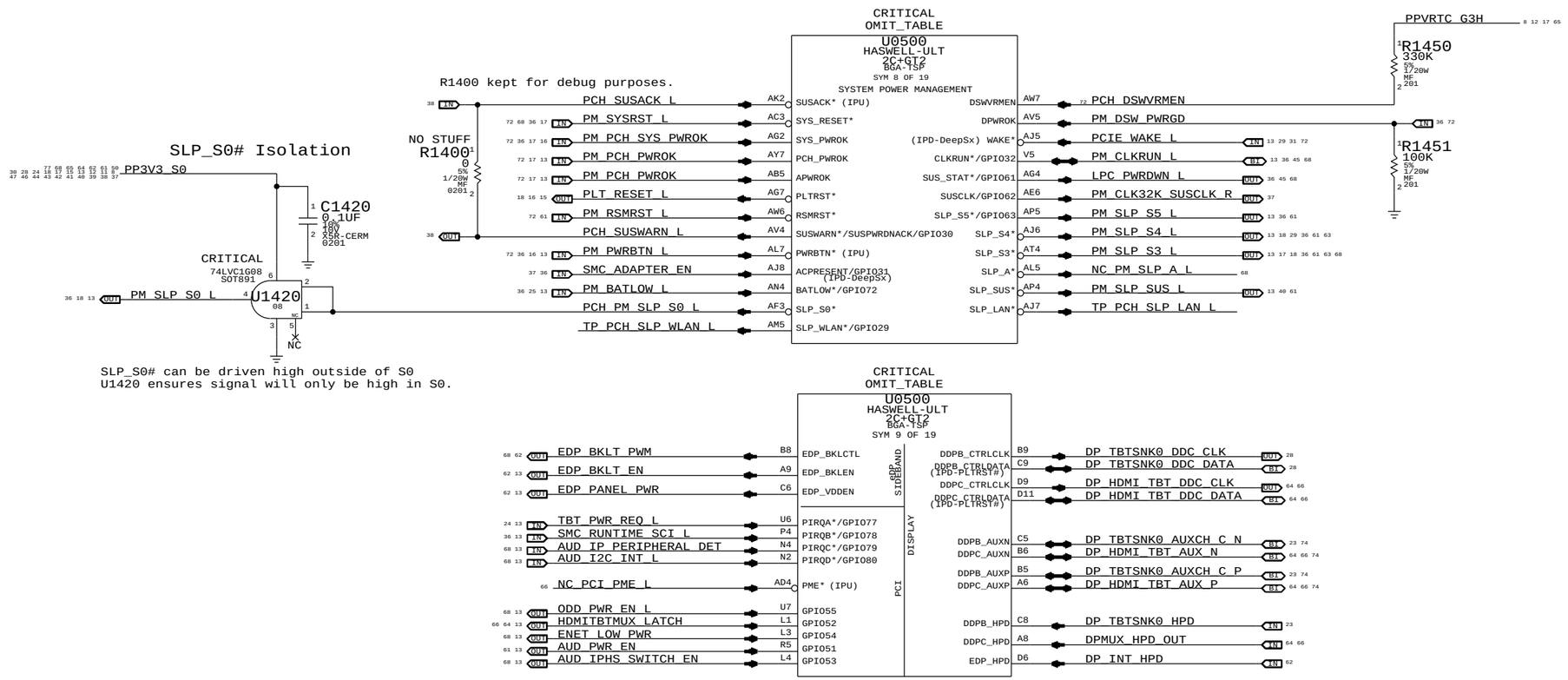


SYNC_MASTER=J44 SYNC_DATE=08/12/2013

PAGE TITLE: PCH Audio/JTAG/SATA/CLK

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D
REVISION: <E4LABEL>
BRANCH: <BRANCH>
PAGE: 13 OF 120
SHEET: 12 OF 78



SYNC_MASTER=J44 SYNC_DATE=08/12/2013

PAGE TITLE: PCH PM/PCI/GFX

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

REVISION: <E4LABEL>

BRANCH: <BRANCH>

PAGE: 14 OF 120

SHEET: 13 OF 78

PCIe Port Assignments:

Thunderbolt lane 0

Thunderbolt lane 1

Thunderbolt lane 2

Thunderbolt lane 3

AirPort

Reserved: FireWire

SD Card Reader
(& Ethernet if combo)

Camera

CRITICAL
OMIT_TABLE

U0500
HASWELL-ULT
2C+GT2
BGA-TSP
SYM 11 OF 19

PCI-E
USB

70 68 23 IN	PCIE_TBT_D2R_N<0>	F10	PERN5_L0
70 68 23 IN	PCIE_TBT_D2R_P<0>	E10	PERP5_L0
70 68 23 OUT	PCIE_TBT_R2D_C_N<0>	C23	PETN5_L0
70 68 23 OUT	PCIE_TBT_R2D_C_P<0>	C22	PETP5_L0
70 68 23 IN	PCIE_TBT_D2R_N<1>	F8	PERN5_L1
70 68 23 IN	PCIE_TBT_D2R_P<1>	E8	PERP5_L1
70 68 23 OUT	PCIE_TBT_R2D_C_N<1>	B23	PETN5_L1
70 68 23 OUT	PCIE_TBT_R2D_C_P<1>	A23	PETP5_L1
70 68 23 IN	PCIE_TBT_D2R_N<2>	H10	PERN5_L2
70 68 23 IN	PCIE_TBT_D2R_P<2>	G10	PERP5_L2
70 68 23 OUT	PCIE_TBT_R2D_C_N<2>	B21	PETN5_L2
70 68 23 OUT	PCIE_TBT_R2D_C_P<2>	C21	PETP5_L2
70 68 23 IN	PCIE_TBT_D2R_N<3>	E6	PERN5_L3
70 68 23 IN	PCIE_TBT_D2R_P<3>	F6	PERP5_L3
70 68 23 OUT	PCIE_TBT_R2D_C_N<3>	B22	PETN5_L3
70 68 23 OUT	PCIE_TBT_R2D_C_P<3>	A21	PETP5_L3
70 68 63 IN	PCIE_AP_D2R_N	G11	PERN3
70 68 63 IN	PCIE_AP_D2R_P	F11	PERP3
70 68 63 OUT	PCIE_AP_R2D_C_N	C29	PETN3
70 68 63 OUT	PCIE_AP_R2D_C_P	B30	PETP3
66	NC_PCIE_FW_D2RN	F13	PERN4
66	NC_PCIE_FW_D2RP	G13	PERP4
66	NC_PCIE_FW_R2D_CN	B29	PETN4
66	NC_PCIE_FW_R2D_CP	A29	PETP4
71 68 63 IN	USB3RPCIE_SD_D2R_N	G17	PERN1/USB3RN2
71 68 63 IN	USB3RPCIE_SD_D2R_P	F17	PERP1/USB3RP2
71 63 OUT	USB3RPCIE_SD_R2D_C_N	C30	PETN1/USB3TN2
71 63 OUT	USB3RPCIE_SD_R2D_C_P	C31	PETP1/USB3TP2
70 68 32 IN	PCIE_CAMERA_D2R_N	F15	PERN2/USB3RN3
70 68 32 IN	PCIE_CAMERA_D2R_P	G15	PERP2/USB3RP3
70 32 OUT	PCIE_CAMERA_R2D_C_N	B31	PETN2/USB3TN3
70 32 OUT	PCIE_CAMERA_R2D_C_P	A31	PETP2/USB3TP3
NC		E15	RSVD
NC		E13	RSVD
		A27	PCIE_RCOMP
		B27	PCIE_IREF

11 8 PP1V05_S0SW_PCH_VCCUSB3PLL

72 PCH_PCIE_RCOMP

R1500 3.01K 1% 1/20W MF 201
PLACE_NEAR=U0500.A27:2.54mm

USB Port Assignments:

Ext A (LS/FS/HS)

Ext B (LS/FS/HS)

BT

IR

Trackpad

Unused

Reserved: Camera

Reserved: SD (HS)

USB2N0	AN8	USB_EXTA_N	33 71 BI
USB2P0	AM8	USB_EXTA_P	33 71 BI
USB2N1	AR7	USB_EXTB_N	63 71 BI
USB2P1	AT7	USB_EXTB_P	63 71 BI
USB2N2	AR8	USB_BT_N	29 71 BI
USB2P2	AP8	USB_BT_P	29 71 BI
USB2N3	AR10	NC_USB_IRN	66 71 BI
USB2P3	AT10	NC_USB_IRP	66 71 BI
USB2N4	AM15	USB_TPAD_N	34 71 BI
USB2P4	AL15	USB_TPAD_P	34 71 BI
USB2N5	AM13	TP_USB_5N	71
USB2P5	AN13	TP_USB_5P	71
USB2N6	AP11	NC_USB_CAMERAN	66 71
USB2P6	AN11	NC_USB_CAMERAP	66 71
USB2N7	AR13	NC_USB_SDN	66 71
USB2P7 (IPD)	AP13	NC_USB_SDP	66 71

USB3 Port Assignments:

Ext A (SS)

Ext B (SS)

USB3RN0	G20	USB3_EXTA_D2R_N	33 68 71 IN
USB3RP0	H20	USB3_EXTA_D2R_P	33 68 71 IN
USB3TN0	C33	USB3_EXTA_R2D_C_N	33 68 71 OUT
USB3TP0	B34	USB3_EXTA_R2D_C_P	33 68 71 OUT
USB3RN1	E18	USB3_EXTB_D2R_N	63 68 71 IN
USB3RP1	F18	USB3_EXTB_D2R_P	63 68 71 IN
USB3TN1	B33	USB3_EXTB_R2D_C_N	63 68 71 OUT
USB3TP1	A33	USB3_EXTB_R2D_C_P	63 68 71 OUT

USBRBIAS*	AJ10	71 PCH_USB_RBIAS	
USBRBIAS	AJ11		
RSVD	AN10	NC	
RSVD	AM10	NC	
OC0*/GPIO40	AL3	XDP_USB_EXTA_OC_L	14 16 33 IN
OC1*/GPIO41	AT1	XDP_USB_EXTB_OC_L	14 16 63 IN
OC2*/GPIO42	AH2	XDP_USB_EXTC_OC_L	14 16 IN
OC3*/GPIO43	AV3	XDP_USB_EXTD_OC_L	14 16 IN

PLACE_NEAR=U0500.AJ10:2.54mm
R1570 22.6 1% 1/20W MF 201

CRITICAL
OMIT_TABLE

U0500
HASWELL-ULT
2C+GT2
BGA-TSP
SYM 7 OF 19

LPC
SMBUS
SPI
C-LINK

72 68 45 36 BI	LPC_AD<0>	R1540 33	AU14 (IPU) LAD0
72 68 45 36 BI	LPC_AD<1>	R1541 33	AW12 LAD1
72 68 45 36 BI	LPC_AD<2>	R1542 33	AY12 LAD2
72 68 45 36 BI	LPC_AD<3>	R1543 33	AW11 LAD3
72 68 45 36 OUT	LPC_FRAME_L	R1544 33	AV12 LFRAME*
72 45 OUT	SPI_CLK_R		AA3 SPI_CLK (IPU)
72 45 OUT	SPI_CS0_R_L		Y7 SPI_CS0* (IPU)
	TP_SPI_CS1_L		Y4 SPI_CS1* (IPU)
	TP_SPI_CS2_L		AC2 SPI_CS2* (IPU)
72 45 BI	SPI_MOSI_R		AA2 SPI_MOSI (IPU/IPD)
72 45 BI	SPI_MISO		AA4 SPI_MISO (IPU)
72 45 14 BI	SPI_IO<2>		Y6 SPI_IO2 (IPU)
72 45 14 BI	SPI_IO<3>		AF1 SPI_IO3 (IPU)

SMBALERT*/GPIO11	AN2	PCH_SMBALERT_L	14
SMBCLK	AP2	SMBUS_PCH_CLK	16 19 39 63 68 72 OUT
SMBDATA	AH1	SMBUS_PCH_DATA	16 19 39 63 68 72 BI
SML0ALERT*/GPIO60	AL2	WOL_EN	14 68 OUT
SML0CLK	AN1	SML_PCH_0_CLK	39 72 OUT
SML0DATA	AK1	SML_PCH_0_DATA	39 72 BI
SML1ALERT*/PCHHOT*/GPIO73	AU4	PCH_SML1ALERT_L	38 OUT
SML1CLK_GPIO75	AU3	SMBUS_SMC_1_S0_SCL	32 36 39 43 68 72 76 OUT
SML1DATA/GPIO74	AH3	SMBUS_SMC_1_S0_SDA	32 36 39 43 68 72 76 BI
(IPU/IPD) CL_CLK	AF2	NC_CLINK_CLK	66
(IPU/IPD) CL_DATA	AD2	NC_CLINK_DATA	66
CL_RST*	AF4	NC_CLINK_RESET_L	66

SML1ALERT# pull-up not provided on this page, may be wire-ORed into other signals. Otherwise, 100k pull-up to 3.3V SUS required.

PP3V3_SUS 8 11 14 45 59 60 61 65
PP3V3_SUS 8 11 14 45 59 60 61 65

R1580	100K	XDP_USB_EXTA_OC_L	14 16 33
R1581	100K	XDP_USB_EXTB_OC_L	14 16 63
R1582	100K	XDP_USB_EXTC_OC_L	14 16
R1583	100K	XDP_USB_EXTD_OC_L	14 16
R1548	1K	SPI_IO<2>	14 45 72
R1549	1K	SPI_IO<3>	14 45 72
R1590	100K	PCH_SMBALERT_L	14
R1591	100K	WOL_EN	14 68

All: 5% 1/20W MF 201

SYNC_MASTER=J44 SYNC_DATE=08/12/2013

PAGE TITLE
PCH PCIe/USB/LPC/SPI/SMBus

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D
REVISION <E4LABEL>
BRANCH <BRANCH>
PAGE 15 OF 120
SHEET 14 OF 78

BOM GROUP	BOM OPTIONS
RAMCFG_SLOT	RAMCFG3:H,RAMCFG2:H,RAMCFG1:H,RAMCFG0:H

PP3V3_S0

RAMCFG3:H R1631 100K 5% 1/20W MF 201
RAMCFG2:H R1636 100K 5% 1/20W MF 201
RAMCFG1:H R1635 100K 5% 1/20W MF 201
RAMCFG0:H R1611 100K 5% 1/20W MF 201

XDP_MLB_RAMCFG0
XDP_MLB_RAMCFG1
XDP_MLB_RAMCFG2
XDP_MLB_RAMCFG3

GPIO12:

CR: TBT_GO2SX_BIDIR, requires 100k pull-up to SUS
RR/FR: DPHDMIMUX_SEL_TBT, requires 100k pull-up to TBTLC

PLT_RESET_L → R1621 100K → PCH_TBT_PCIE_RESET_L

R1639 100K → SSD_RESET_L

PP3V3_S0 → R1641 1K → PCH_TCO_TIMER_DISABLE

CRITICAL
OMIT_TABLE
U0500
HASWELL-ULT
2C+GT2
BGA-1SF
SYM 10 OF 19

P1	BMBUSY*/GPIO76	XDP_PCH_GPIO76
AU2	GPIO8	XDP_MLB_RAMCFG0
AM7	LAN_PHY_PWR_CTRL/GPIO12	HDMITBTMUX_SEL_TBT
AD6	GPIO15 (IPD-RSMRST#)	MEM_VDD_SEL_1V5_L
Y1	GPIO16	XDP_LPCPLUS_GPIO
T3	GPIO17	XDP_PCH_GPIO17
AD5	GPIO24	SD_RESET_L
AN5	GPIO27 (IPD-DeepSx)	SMC_WAKE_SCI_L
AD7	GPIO28	TPAD_SPI_INT_L
AN3	GPIO26	TPAD_USB_IF_EN
AG6	GPIO56	SSD_PWR_EN
AP1	GPIO57	PCH_TBT_PCIE_RESET_L
AL4	GPIO58	HDD_PWR_EN
AT5	GPIO59	XDP_SDCONN_STATE_CHANGE_L
AK4	GPIO44	SD_PWR_EN
AB6	GPIO47	TBT_PWR_EN
U4	GPIO48	XDP_JTAG_ISP_TCK
Y3	GPIO49	XDP_JTAG_ISP_TDI
P3	GPIO50	JTAG_TBT_TMS_PCH
Y2	HSIOPC/GPIO71	PCH_HSIO_PWR_EN
AT3	GPIO13	TPAD_SPI_IF_EN
AH4	GPIO14	XDP_MLB_RAMCFG3
AM4	GPIO25	SPIROM_USE_MLB
AG5	GPIO45	CAMERA_PWR_EN_PCH
AG3	GPIO46	FW_PWR_EN
AM3	GPIO9	XDP_MLB_RAMCFG1
AM2	GPIO10	XDP_MLB_RAMCFG2
P2	DEVSLP0*/GPIO33	SSD_DEVSLP
C4	SDIO_POWER_EN/GPIO70	AP_S0IX_WAKE_SEL
L2	DEVSLP1*/GPIO38	SSD_RESET_L
N5	DEVSLP2*/GPIO39	FW_PME_L
V2	SPKR/GPIO81 (IPD-PLTRST#)	PCH_TCO_TIMER_DISABLE

CPU/MISC

D60	THRMTRIP*	PM_THRMTRIP_L
V4	RCIN*/GPIO82	TBT_CIO_PLUG_EVENT_L
T4	SERIRQ	LPC_SERIRQ
AW15	PCH_OPI_COMP	PCH_OPI_COMP
AF20	RSVD	NC
AB21	RSVD	NC

GPIO / LPIO

R6	GSPI0_CS*/GPIO83	PCH_GSPI0_CS_L
L6	GSPI0_CLK/GPIO84	PCH_GSPI0_CLK
N6	GSPI0_MISO/GPIO85 (IPD)	PCH_GSPI0_MISO
L8	GSPI0_MOSI/GPIO86 (IPD-PLTRST#)	PCH_GSPI0_MOSI
R7	GSPI1_CS*/GPIO87	TPAD_SPI_CS_L
L5	GSPI1_CLK/GPIO88	TPAD_SPI_CLK
N7	GSPI1_MISO/GPIO89 (IPD)	TPAD_SPI_MISO
K2	GSPI_MOSI/GPIO90	TPAD_SPI_MOSI
J1	UART0_RXD/GPIO91	AP_S0IX_WAKE_L
K3	UART0_TXD/GPIO92	HDMITBTMUX_FLAG_L
J2	UART0_RTS*/GPIO93	JTAG_ISP_TDO
G1	UART0_CTS*/GPIO94	AP_RESET_L
K4	UART1_RXD/GPIO0	PCH_UART1_RXD
G2	UART1_TXD/GPIO1	PCH_UART1_TXD
J3	UART1_RST*/GPIO2	PCH_UART1_RTS_L
J4	UART1_CTS*/GPIO3	PCH_UART1_CTS_L
F2	I2C0_SDA/GPIO4	PCH_I2C0_SDA
F3	I2C0_SCL/GPIO5	PCH_I2C0_SCL
G4	I2C1_SDA/GPIO6	PCH_I2C1_SDA
F1	I2C1_SCL/GPIO7	PCH_I2C1_SCL
E3	SDIO_CLK/GPIO64	TBT_POC_RESET_L
F4	SDIO_CMD/GPIO65	BT_PWRRST_L
D3	SDIO_D0/GPIO66 (IPD-PLTRST#)	PCH_STRP_TOPBLK_SWP_L
E4	SDIO_D1/GPIO67	ENET_MEDIA_SENSE
C3	SDIO_D2/GPIO68	LCD_IRQ_L
E2	SDIO_D3/GPIO69	LCD_PSR_EN

PP1V05_S0 → R1650 1K 5% 1/20W MF 201 → PM_THRMTRIP_L

Pull-up/down on chipset support page (depends on TBT controller)
Cactus Ridge: Alias to TBT_CIO_PLUG_EVENT, requires pull-down.
Redwood Ridge: Alias to TBT_CIO_PLUG_EVENT_L, requires pull-up (S0).

PLACE_NEAR=U0500.AW15:2.54mm
R1655 49.9 1% 1/20W MF 201

PLT_RESET_L → R1671 100K 5% 1/20W MF 201

Pull-up on TBT page

Requires connection to SMC via 1K series R

PP3V3_S0 → R1660 100K PCH_GSPI0_CS_L
R1661 100K PCH_GSPI0_CLK
R1662 100K PCH_GSPI0_MISO
R1663 100K PCH_GSPI0_MOSI
R1664 47K TPAD_SPI_CS_L
R1665 47K TPAD_SPI_CLK
R1666 47K TPAD_SPI_MISO
R1667 47K TPAD_SPI_MOSI
R1668 100K AP_S0IX_WAKE_L
R1669 100K HDMITBTMUX_FLAG_L
R1672 100K PCH_UART1_RXD
R1673 100K PCH_UART1_TXD
R1674 100K PCH_UART1_RTS_L
R1675 100K PCH_UART1_CTS_L
R1676 100K PCH_I2C0_SDA
R1677 100K PCH_I2C0_SCL
R1678 100K PCH_I2C1_SDA
R1679 100K PCH_I2C1_SCL
(all 5% 1/20W MF 201)

TBTLC for CR, S0 for RR

R1610 100K	XDP_PCH_GPIO76	
R1614 100K	XDP_LPCPLUS_GPIO	
R1615 100K	XDP_PCH_GPIO17	
SD_ON_MLB		
R1616 100K	SD_RESET_L	R1616 should also be stuffed if platform does not use SD card
R1617 100K	SMC_WAKE_SCI_L	
R1618 100K	TPAD_SPI_INT_L	
R1619 100K	TPAD_USB_IF_EN	
R1620 100K	SSD_PWR_EN	
R1622 100K	HDD_PWR_EN	
R1623 100K	XDP_SDCONN_STATE_CHANGE_L	
R1624 100K	SD_PWR_EN	
R1625 100K	TBT_PWR_EN	
R1626 100K	XDP_JTAG_ISP_TCK	
R1627 100K	XDP_JTAG_ISP_TDI	
R1628 100K	JTAG_TBT_TMS_PCH	
R1629 100K	PCH_HSIO_PWR_EN	
R1630 100K	TPAD_SPI_IF_EN	
NO STUFF		
R1632 100K	SPIROM_USE_MLB	
R1633 100K	CAMERA_PWR_EN_PCH	
R1634 100K	FW_PWR_EN	
R1637 100K	SSD_DEVSLP	
R1638 100K	AP_S0IX_WAKE_SEL	
R1640 100K	FW_PME_L	
R1652 10K	LPC_SERIRQ	
R1670 100K	JTAG_ISP_TDO	
R1691 100K	BT_PWRRST_L	
R1693 100K	ENET_MEDIA_SENSE	
R1694 10K	LCD_IRQ_L	
R1695 100K	LCD_PSR_EN	

PP3V3_S5
PP3V3_S3
PP3V3_S3
PP3V3_S3
PP3V3_S3RS0_CAMERA
PP3V3_S0
PP3V3_S0

SYNC_MASTER=J44 SYNC_DATE=08/12/2013

PAGE TITLE: PCH GPIO/MISC/LPIO

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D
REVISION: <E4LABEL>
BRANCH: <BRANCH>
PAGE: 16 OF 120
SHEET: 15 OF 78

Extra BPM Testpoints

XDP_BPM_L<2> → TP1802
XDP_BPM_L<3> → TP1803
XDP_BPM_L<4> → TP1804
XDP_BPM_L<5> → TP1805
XDP_BPM_L<6> → TP1806
XDP_BPM_L<7> → TP1807

Merged (CPU/PCH) Micro2-XDP

PP1V05_S0

CRITICAL XDP_CONN J1800 DF40RC-60DP-0.4V M-ST-SM1

NOTE: This is not the standard XDP pinout. Use with 921-0133 Adapter Flex to support chipset debug.

R1830 150 5% 1/16W MF-LF 402

XDP_CPU_PREQ_L	OBSEN_A0	OBSEN_C0	CPU_CFG<17>
XDP_CPU_PRDY_L	OBSEN_A1	OBSEN_C1	CPU_CFG<16>
CPU_CFG<0>	OBSDATA_A0	OBSDATA_C0	CPU_CFG<8>
CPU_CFG<1>	OBSDATA_A1	OBSDATA_C1	CPU_CFG<9>
CPU_CFG<2>	OBSDATA_A2	OBSDATA_C2	CPU_CFG<10>
CPU_CFG<3>	OBSDATA_A3	OBSDATA_C3	CPU_CFG<11>
XDP_BPM_L<0>	OBSEN_B0	OBSEN_D0	CPU_CFG<19>
XDP_BPM_L<1>	OBSEN_B1	OBSEN_D1	CPU_CFG<18>
CPU_CFG<4>	OBSDATA_B0	OBSDATA_D0	CPU_CFG<12>
CPU_CFG<5>	OBSDATA_B1	OBSDATA_D1	CPU_CFG<13>
CPU_CFG<6>	OBSDATA_B2	OBSDATA_D2	CPU_CFG<14>
CPU_CFG<7>	OBSDATA_B3	OBSDATA_D3	CPU_CFG<15>
XDP_CPU_VCCST_PWRGD	PWRGD/HOOK0	ITPCLK/HOOK4	NC
XDP_CPU_PWRBTN_L	HOOK1	ITPCLK#/HOOK5	NC
	VCC_OBS_AB	VCC_OBS_CD	
CPU_PWR_DEBUG	HOOK2	RESET#/HOOK6	XDP_CPURST_L
XDP_SYS_PWROK	HOOK3	DBR#/HOOK7	XDP_DBRESET_L
SMBUS_PCH_DATA	SDA	TDO	XDP_PCH_TDO
SMBUS_PCH_CLK	SCL	TRSTn	XDP_TRST_L
XDP_PCH_TCK	TCK1	TDI	XDP_PCH_TDI
	TCK0	TMS	XDP_PCH_TMS
		XDP_PRESENT#	XDP_CPU_PRESENT_L

518S0847

C1804 0.1UF 10% 10V CERM-X5R 0201
R1831 1K 5% 1/16W MF-LF 402
C1800 0.1UF 10% 10V CERM-X5R 0201
C1801 0.1UF 10% 10V CERM-X5R 0201
C1806 0.1UF 10% 10V CERM-X5R 0201

CPU_VCCST_PWRGD → R1800 1K 5% 1/20W MF 201 → XDP
PLACE_NEAR=U0500.C61:2.54mm

PM_PWRBTN_L → R1802 0 5% 1/20W MF 0201 → XDP
PLACE_NEAR=U5000.J3:2.54mm

PM_PCH_SYS_PWROK → R1804 0 5% 1/16W MF-LF 402 → XDP

XDP_CPU_TCK

PCH_JTAGX → R1835 0 5% 1/20W MF 0201 → XDP
PLACE_NEAR=J1800.58:28mm

R1805 1K 5% 1/20W MF 201 → XDP
PLT_RESET_L
PLACE_NEAR=U0500.AG7:2.54mm
NOTE: XDP_DBRESET_L pulled-up to 3.3V on PCH Support Page

XDP_PCH_TDO
XDP_PCH_TDI
XDP_PCH_TMS

CRITICAL XDP Q1840 DMN5L06VK-7 SOT-563
PLACE_NEAR=J1800.51:28mm
XDP_CPU_TDO

CRITICAL XDP Q1840 DMN5L06VK-7 SOT-563
PLACE_NEAR=J1800.53:28mm
XDP_CPUPCH_TRST_L
MAKE_BASE=TRUE
XDP_CPUPCH_TRST_L
XDP_CPUPCH_TRST_L

CRITICAL XDP Q1842 DMN5L06VK-7 SOT-563
PLACE_NEAR=J1800.55:28mm
XDP_CPU_TDI

CRITICAL XDP Q1842 DMN5L06VK-7 SOT-563
PLACE_NEAR=J1800.57:28mm
XDP_CPU_TMS

XDP_JTAG_CPU_ISOL_L

PP1V05_S0
XDP_CPU_TDO → R1810 51 → XDP
PLACE_NEAR=U0500.F62:28mm
XDP_CPU_TCK → R1813 51 → XDP
PLACE_NEAR=U0500.E60:28mm
TDI and TMS are terminated in CPU.

CPU JTAG Isolation

PP5V_S0
PP3V3_S5
ALL_SYS_PWRGD
C1845 0.1UF 10% 10V X5R-CERM 0201
U1845 74LVC1G07GF SOT891 (VCC, GND, NC)
R1845 330K 5% 1/20W MF 201

PP1V05_SUS

PCH_JTAGX	R1899 1K	NO STUFF
XDP_PCH_TDO	R1890 51	XDP
XDP_PCH_TDI	R1891 51	XDP
XDP_PCH_TMS	R1892 51	XDP
XDP_PCH_TCK	R1896 51	NO STUFF
XDP_CPUPCH_TRST_L	R1897 51	NO STUFF

All 5% 1/20W MF 201, PLACE_NEAR=U0500.AG63:28mm / AE61:28mm / AG61:28mm / AG62:28mm / AG62:28mm / AG62:28mm

PCH XDP Signals

These signals do not connect to XDP connector in this architecture, only accessible via Top-Side Probe. Nets are listed here to show XDP associations and to make clear what restrictions exist on PCH GPIOs when Top-Side Probe is used for PCH debug.

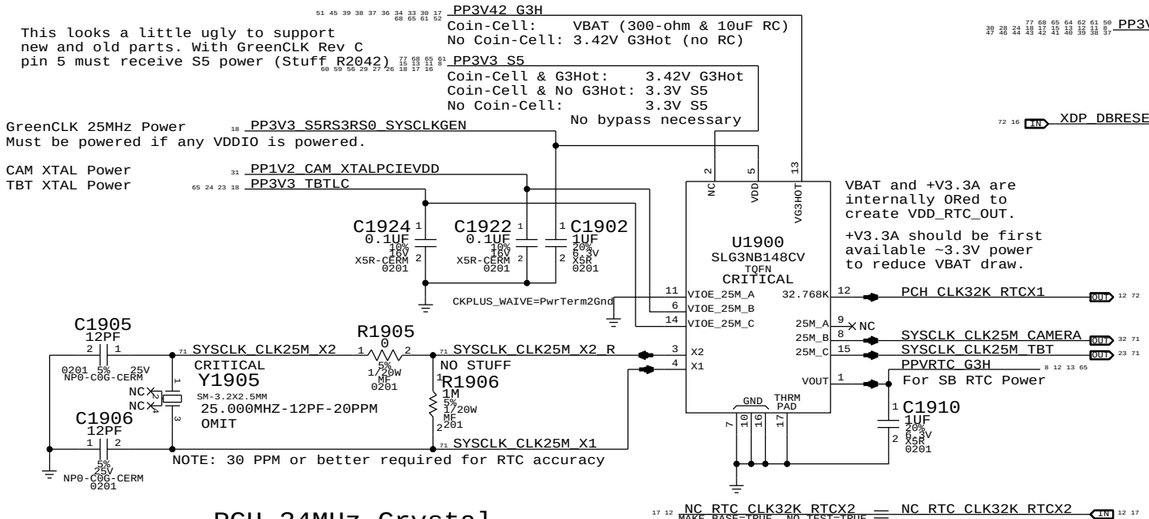
PCH/XDP Signals		Non-XDP Signals
XDP_MLB_RAMCFG0	TP1870	
XDP_USB_EXTA_OC_L	MAKE_BASE=TRUE	XDP_USB_EXTA_OC_L
XDP_USB_EXTB_OC_L	MAKE_BASE=TRUE	XDP_USB_EXTB_OC_L
XDP_USB_EXTC_OC_L	TP1873	
XDP_USB_EXTD_OC_L	TP1874	
XDP_SDCONN_STATE_CHANGE_L	MAKE_BASE=TRUE	XDP_SDCONN_STATE_CHANGE_L
XDP_MLB_RAMCFG1	TP1876	
XDP_MLB_RAMCFG2	TP1877	
XDP_MLB_RAMCFG3	TP1878	
XDP_JTAG_ISP_TCK	MAKE_BASE=TRUE	JTAG_ISP_TCK
XDP_SSD_PCIE3_SEL_L	R1881 1K	
XDP_SSD_PCIE2_SEL_L	R1882 1K	NOTE: Must not short XDP pins together!
XDP_SSD_PCIE1_SEL_L	R1883 1K	
XDP_SSD_PCIE0_SEL_L	R1884 1K	SSD_PCIE_SEL_L
XDP_LPCPLUS_GPIO	MAKE_BASE=TRUE	XDP_LPCPLUS_GPIO
XDP_PCH_GPIO17	TP1886	
XDP_PCH_GPIO76	TP1887	
XDP_JTAG_ISP_TDI	MAKE_BASE=TRUE	JTAG_ISP_TDI

Unused & MLB_RAMCFGx GPIOs have TPs.
USB Overcurrents are aliased, do not cause USB OC# events during PCH debug.
SDCONN_STATE_CHANGE_L is aliased, do not plug/unplug SD Cards during PCH debug.
JTAG_ISP (non-TMS) nets are aliased, do not attempt bit-banged JTAG during PCH debug.
NOTE: Should force PCH GPIO47 high to ensure TBT router powered to avoid leakage/clamping of signals.
SSD_PCIEx_SEL_L straps are connected via 1K to common net.
LPCPLUS_GPIO is aliased, do not attempt use during PCH debug.

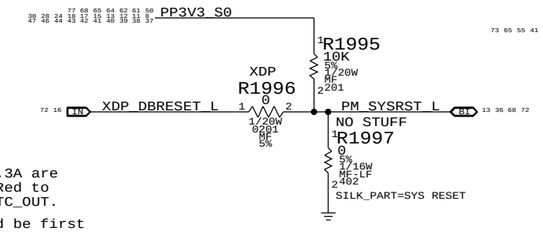
SYNC_MASTER=J44 SYNC_DATE=08/12/2013
PAGE TITLE: CPU/PCH Merged XDP
Apple Inc.
DRAWING NUMBER: <SCH_NUM> SIZE: D
REVISION: <E4LABEL>
BRANCH: <BRANCH>
PAGE: 18 OF 120
SHEET: 16 OF 78

System RTC Power Source & 32kHz / 25MHz Clock Generator

Chipset uses 24MHz crystal, GreenCLK kept to save 1x 25MHz crystal & 1x 32kHz crystal

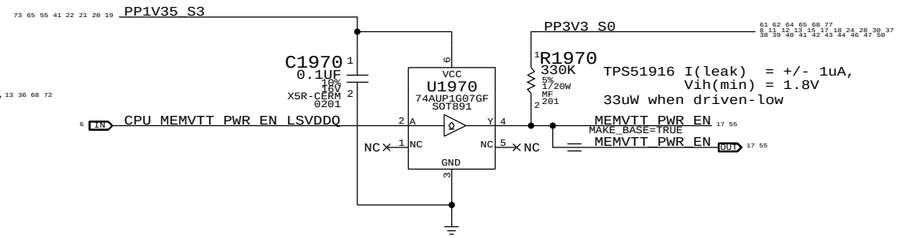


PCH Reset Button

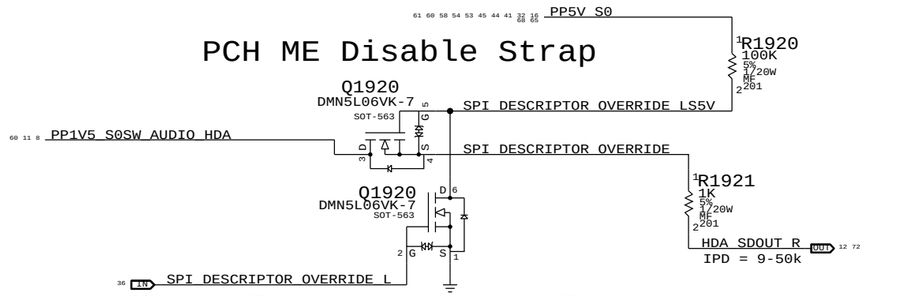


Memory VTT Enable Level-Shifter

CPU output is on VDDQ rail (1.2V), TPS51916 has 1.8V Vih(min).

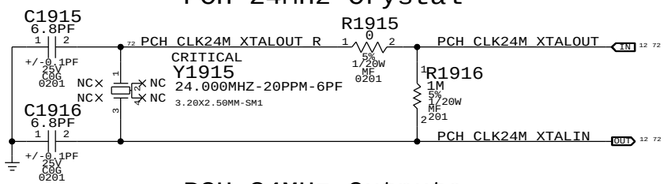


PCH ME Disable Strap

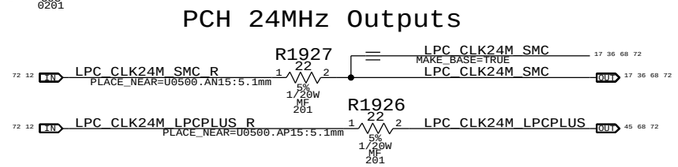


PCH uses HDA_SDO as a power-up strap. If low, ME functions normally. If high, ME is disabled. This allows for full re-flashing of SPI ROM. SMC controls strap enable to allow in-field control of strap setting. Q1920 & 5V pull-up allows circuit to work regardless of HDA voltage.

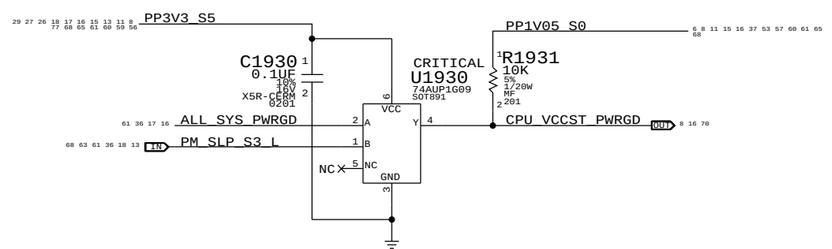
PCH 24MHz Crystal



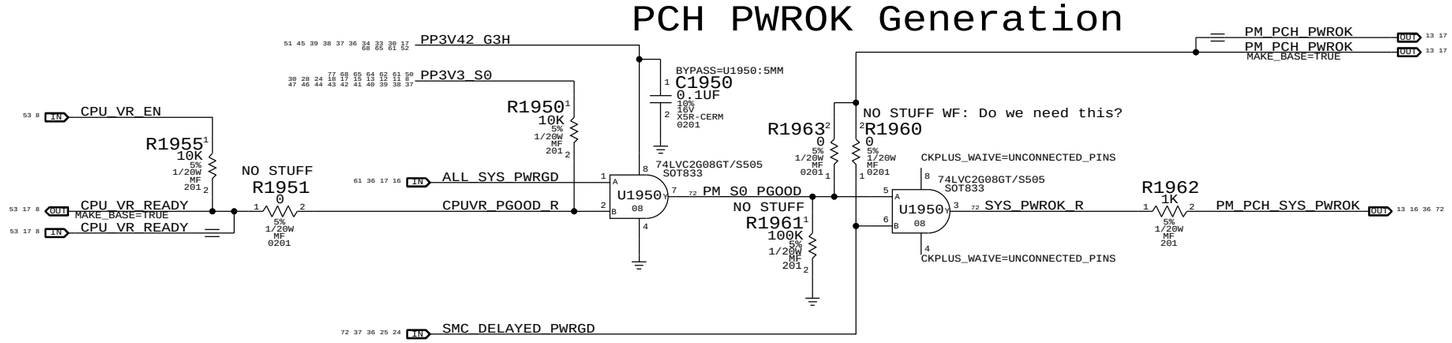
PCH 24MHz Outputs



VCCST (1.05V S0) PWRGD



PCH PWROK Generation



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
197S0480	1	XTAL,25MHZ,20PPM,12PF,3.2X2.5X.6MM,85C	Y1905		

SYNC_MASTER=J44 SYNC_DATE=08/12/2013

PAGE TITLE: Chipset Support

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D
REVISION: <E4LABEL>
BRANCH: <BRANCH>
PAGE: 19 OF 120
SHEET: 17 OF 78

Platform Reset Connections

Unbuffered

PLT_RESET_L (IN) → R2081 33 5% 1/20W MF 201 → LPCPLUS_RESET_L (OUT)

R2071 0 5% 1/20W MF 0201 → PCA9557D_RESET_L (OUT)

Buffered

PLT_RST_BUF_L

U2071 MC74VHC1G08 SC70-HF (CRITICAL)

C2071 0.1UF 10% 16V X5R-CERM 0201

R2070 100K 5% 1/20W MF 201

R2072 0 5% 1/20W MF 0201 → SMC_LRESET_L (OUT)

R2089 0 5% 1/20W MF 0201 → CAM_PCIE_RESET_L (OUT)

PCH_TBT_PCIE_RESET_L (IN, MAKE_BASE=TRUE) → PCH_TBT_PCIE_RESET_L (OUT)

GreenCLK 25MHz Power

PP3V3_S3 → R2040 0 5% 1/20W MF 0201 (NO STUFF) → I1608 → PP3V3_S5RS3RS0_SYSCLKGEN

PP3V3_S5RS3RS0_SYSCLKGEN (MIN_LINE_WIDTH=0.5 MM, MIN_NECK_WIDTH=0.2 MM, VOLTAGE=3.3V, MAKE_BASE=TRUE)

PP3V3_S0 → R2041 0 5% 1/20W MF 0201 (NO STUFF)

PP3V3_S5 → R2042 0 5% 1/20W MF 0201

R2041/2 should be stuffed for GreekCLK A or B depending on S2 rail

R2042 should be stuffed for GreenCLK C

THUNDERBOLT PULL-UP

PP3V3_S0 → R2015 100K 5% 1/20W MF 201

REDWOOD RIDGE PLUG_EVENT IS ACTIVE-LOW, ALWAYS DRIVEN (PULL-UP)

TBT_CIO_PLUG_EVENT_L (OUT) — MAKE_BASE=TRUE — TBT_CIO_PLUG_EVENT_L (IN)

Scrub for Layout Optimization

PP3V3_S0

SDCONN_STATE_CHANGE Isolation

PP3V3_S4 → R2032 470K 5% 1/20W MF 201 → Q2030 DMN5L06VK-7 SOT-563

R2031 470K 5% 1/20W MF 201

SMC_PME_S4_DARK_L → Q2030 → SMC_PME_SDCONN

To SMC: SMC_PME_S4_DARK_L

PP3V3_S3 → CRITICAL U2031 74AUP1G09 SOT891

XDP_SDCONN_STATE_CHANGE_L (OUT) → To PCH

BYPASS=U2030.5:5MM

C2031 0.1UF 10% 6.3V CERM-X5R 0201

NC

SDCONN_STATE_CHANGE_RIO (IN)

Redwood Ridge JTAG Isolation

TBTLC can be on when S0 is off, and vice-versa
Isolation ensures no leakage to RR or PCH

PP3V3_TBTLC

R2061 100K 5% 1/20W MF 201

C2060 0.1UF 20% 10V CERM 402

R2062 100K 5% 1/20W MF 201

U2060 74LVC2G07 SOT891 (VCC, GND)

From RR: JTAG_TBT_TDO (IN) → JTAG_ISP_TDO (OUT) → To PCH

From PCH: JTAG_TBT_TMS_PCH (IN) → JTAG_TBT_TMS (OUT) → To RR

S0 pull-up on PCH page

S0 pull-up on PCH page

NOTE: Solution shown is for LPT-LP. Other PCH's may require isolation on TCK and TDI as well for PCH glitch-prevention.

NOTE: This reference schematic assumes PCH JTAG GPIOs are only used for Thunderbolt. If other ASIC JTAG signals are wired into these GPIOs different isolation techniques will likely be necessary. Multi-router designs also require different circuitry.

JTAG_ISP_TCK (IN, MAKE_BASE=TRUE) — JTAG_ISP_TCK (OUT)

JTAG_ISP_TDI (IN, MAKE_BASE=TRUE) — JTAG_ISP_TDI (OUT)

Power State Debug LEDs

(For development only)

PP3V3_S5 → R2094 0 5% 1/10W MF-LF 402 (PLACE_SIDE=BOTTOM) → PP3V3_S5_DBGLED (MIN_LINE_WIDTH=0.5 MM, MIN_NECK_WIDTH=0.25 MM, VOLTAGE=3.3V)

DBGLED_S5	DBGLED_S4	DBGLED_S3	DBGLED_S0I3	DBGLED_S0
R2090 20K	R2091 20K	R2092 20K	R2093 20K	R2095 20K
D2090	D2091	D2092	D2093	D2095
GREEN-56MCD-2MA-2.65V LTQH9G-SM	GREEN-56MCD-2MA-2.65V LTQH9G-SM	GREEN-56MCD-2MA-2.65V LTQH9G-SM	GREEN-56MCD-2MA-2.65V LTQH9G-SM	GREEN-56MCD-2MA-2.65V LTQH9G-SM
PLACE_SIDE=BOTTOM SILK_PART=S5_ON	PLACE_SIDE=BOTTOM SILK_PART=STBY_ON	PLACE_SIDE=BOTTOM SILK_PART=S3_ON	PLACE_SIDE=BOTTOM SILK_PART=S0I3_ON	PLACE_SIDE=BOTTOM SILK_PART=S0_ON
DBGLED_S4_D		DBGLED_S3_D	DBGLED_S0I3_D	DBGLED_S0_D
Q2090 DMN5L06VK-7 SOT-563	Q2090 DMN5L06VK-7 SOT-563	Q2090 DMN5L06VK-7 SOT-563	Q2091 DMN5L06VK-7 SOT-563	Q2091 DMN5L06VK-7 SOT-563

S4_PWR_EN (IN)

PM_SLP_S4_L (IN)

PM_SLP_S3_L (IN)

PM_SLP_S0_L (IN)

Pin N61 needs a TP for Power to perform iFDIM test

Renaming the pins N61 and P61 to remove automatic diffpari property

TP_CPU_RSVDN61 — TP_CPU_RSVDN61 (MAKE_BASE=TRUE)

TP_CPU_RSVDP61 — TP_CPU_RSVDP61 (MAKE_BASE=TRUE)

PP3V3_S5 → NOSTUFF C2030 0.1UF 10% 10V X5R-CERM 0201 (BYPASS=U2030.3mm)

PM_SLP_S4_L (IN) → U2030 74LVC1G08 SOT891 (NOSTUFF, CRITICAL)

CAMERA_PWR_EN_PCH (IN) → U2030 → CAMERA_PWR_EN (OUT)

NC

R2030 0 5% 1/20W MF 0201

RAM Configuration Straps

Pull-downs for chip-down RAM systems

XDP_MLB_RAMCFG0 (OUT) → RAMCFG3:L R2050 10K 5% 1/20W MF 201

XDP_MLB_RAMCFG1 (OUT) → RAMCFG2:L R2051 10K 5% 1/20W MF 201

XDP_MLB_RAMCFG2 (OUT) → RAMCFG1:L R2052 10K 5% 1/20W MF 201

XDP_MLB_RAMCFG3 (OUT) → RAMCFG0:L R2053 10K 5% 1/20W MF 201

SYNC_MASTER=J44 SYNC_DATE=08/12/2013

PAGE TITLE: Project Chipset Support

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

REVISION: <E4LABEL>

BRANCH: <BRANCH>

PAGE: 20 OF 120

SHEET: 18 OF 78

Page Notes

Power aliases required by this page:
- =PP3V3_S3_VREFMRGN
- =PPDDR_S3_MEMVREF

Signal aliases required by this page:
- =I2C_VREFDACS_SCL
- =I2C_VREFDACS_SDA
- =I2C_PCA9557D_SCL
- =I2C_PCA9557D_SDA

BOM options provided by this page:
- DDRVREF_DAC - Stuffs DAC margining circuit.

CPU-Based Margining

FETs for CPU isolation during DAC margining

CPU_DIMMA_VREFDQ
CPU_DIMMB_VREFDQ
CPU_DIMM_VREFCA

CRITICAL Q2220 DMN5L06VK-7 SOT-563
CRITICAL Q2260 DMN5L06VK-7 SOT-563
CRITICAL Q2260 DMN5L06VK-7 SOT-563
CRITICAL Q2220 DMN5L06VK-7 SOT-563

NOTE: CPU DAC output step sizes:
DDR3 (1.5V) 7.70mV per step
DDR3L (1.35V) 6.99mV per step
LPDDR3 (1.2V) ?.??mV per step

NOTE: CPU has single output for VREFCA. Split into two signals for independent DAC margining support. When DAC margining VREFCA ensure VREFMRGN_CPU_EN is low to remove short due to CPU.

CPU_DIMMA_VREFDQ_A_ISOL
CPU_DIMMB_VREFDQ_B_ISOL
CPU_DIMM_VREFCA_A_ISOL
CPU_DIMM_VREFCA_B_ISOL

EN RC's to avoid drain glitches
May not be necessary due to C22x0

DDRVREF_DAC R2225 100K — VREFMRGN_DQ_A_EN_RC — DDRVREF_DAC C2225 0.1UF
DDRVREF_DAC R2245 100K — VREFMRGN_DQ_B_EN_RC — DDRVREF_DAC C2245 0.1UF
DDRVREF_DAC R2265 100K — VREFMRGN_CA_A_EN_RC — DDRVREF_DAC C2265 0.1UF
DDRVREF_DAC R2285 100K — VREFMRGN_CA_B_EN_RC — DDRVREF_DAC C2285 0.1UF

DDRVREF_DAC R2201 100K
DDRVREF_DAC R2202 100K
DDRVREF_DAC R2215 100K
DDRVREF_DAC R2207 100K

CRITICAL DDRVREF_DAC Q2225 DMN5L06VK-7 SOT-563
CRITICAL DDRVREF_DAC Q2265 DMN5L06VK-7 SOT-563
CRITICAL DDRVREF_DAC Q2265 DMN5L06VK-7 SOT-563
CRITICAL DDRVREF_DAC Q2225 DMN5L06VK-7 SOT-563

PLACE_NEAR=Q2220.6:2.54mm
PLACE_NEAR=Q2260.6:2.54mm

(All 4 R's) DDRVREF_DAC
R2226 332 — VREFMRGN_DQ_A_RDIV
R2246 332 — VREFMRGN_DQ_B_RDIV
R2266 332 — VREFMRGN_CA_A_RDIV
R2286 332 — VREFMRGN_CA_B_RDIV

R22x6 pin 2:
PLACE_NEAR=Q2225.1:2.54mm
PLACE_NEAR=Q2265.4:2.54mm
PLACE_NEAR=Q2265.1:2.54mm
PLACE_NEAR=Q2225.4:2.54mm

VRef Dividers

Always used, regardless of margining option.

PP1V35_S3

R2223 2 — PLACE_NEAR=Q2220.6:2mm — C2220 0.022UF — MEM_VREFDQ_A_RC
R2221 1K — PLACE_NEAR=Q2220.6:4mm — R2222 1K — R2220 24.9 — PP0V675_S3_MEM_VREFDQ_A
MIN_LINE_WIDTH=0.3 mm MIN_NECK_WIDTH=0.2 mm

R2243 2 — PLACE_NEAR=Q2260.3:2mm — C2240 0.022UF — MEM_VREFDQ_B_RC
R2241 1K — PLACE_NEAR=R2241.2:1mm — R2242 1K — R2240 24.9 — PP0V675_S3_MEM_VREFDQ_B
MIN_LINE_WIDTH=0.3 mm MIN_NECK_WIDTH=0.2 mm

R2263 2 — PLACE_NEAR=Q2260.6:2mm — C2260 0.022UF — MEM_VREFCA_A_RC
R2261 1K — PLACE_NEAR=R2261.2:1mm — R2262 1K — R2260 24.9 — PP0V675_S3_MEM_VREFCA_A
MIN_LINE_WIDTH=0.3 mm MIN_NECK_WIDTH=0.2 mm

R2283 2 — PLACE_NEAR=Q2220.3:2mm — C2280 0.022UF — MEM_VREFCA_B_RC
R2281 1K — PLACE_NEAR=R2281.2:1mm — R2282 1K — R2280 24.9 — PP0V675_S3_MEM_VREFCA_B
MIN_LINE_WIDTH=0.3 mm MIN_NECK_WIDTH=0.2 mm

DAC-Based Margining

DAC sets voltage level, PCA9557 & FETs enable outputs and disables margining after platform reset.

OMIT

PP3V3_S3 — R2218 SHORT — PP3V3_S3_VREFMRGN_DAC
MIN_LINE_WIDTH=0.3 mm MIN_NECK_WIDTH=0.2 mm VOLTAGE=3.3V

DDRVREF_DAC C2200 2.2UF 20% 6.3V CERM 402-LF
DDRVREF_DAC C2201 0.1UF 10% 6.3V CERM-X5R 0201

CRITICAL DDRVREF_DAC
U2200 MSOP DAC5574 — VDD, GND
SMBUS_PCH_CLK — SCL — VOUTA — VREFMRGN_DQ_A
SMBUS_PCH_DATA — SDA — VOUTB — VREFMRGN_DQ_B
A0 — VOUTC — VREFMRGN_CA_AB
A1 — VOUTD — VREFMRGN_MEMVREG

Addr=0x98(WR)/0x99(RD)

NOTE: MEMVREG and SPARE share a DAC output, cannot enable both at the same time!

DDRVREF_DAC C2202 0.1UF
CRITICAL DDRVREF_DAC
U2201 PCA9557 QFN — VCC
R2200 100K
(OD) P0 VREFMRGN_CPU_EN
P1 VREFMRGN_DQ_A_EN
P2 VREFMRGN_DQ_B_EN
P3 VREFMRGN_CA_A_EN
P4 VREFMRGN_CA_B_EN
P5 VREFMRGN_MEMVREG_EN
P6 VREFMRGN_SPARE_EN
P7 NC
RESET* — PCA9557D_RESET_L
A0, A1, A2
SMBUS_PCH_CLK, SMBUS_PCH_DATA
THRM PAD, GND

Addr=0x30(WR)/0x31(RD)

RST* on 'platform reset' so that system watchdog will disable margining.

NOTE: Margining will be disabled across all soft-resets and sleep/wake cycles.

PP3V3_S3
DDRVREF_DAC C2205 0.1UF
CRITICAL DDRVREF_DAC
U2204 MAX4253 UCSP — V+, V-
VREFMRGN_MEMVREG_BUF
DDRVREF_DAC R2214 33.2K — DDRREG_FB — PLACE_NEAR=R7415.2:1mm

DDRVREF_DAC R2213 100K
CRITICAL DDRVREF_DAC
U2204 MAX4253 UCSP — V+, V-
VREFMRGN_SPARE_BUF
DDRVREF_DAC R2217 1M

DDRVREF_DAC R2212 100K

Pins B1 & B4:
CKPLUS_WAIVE=unconnected_pins

NOTE: LPDDR3 assumes TPS51916 supply with 28.7k/57.6k divider
DDR3L assumes TPS51916 supply with 19.6k/57.6k divider

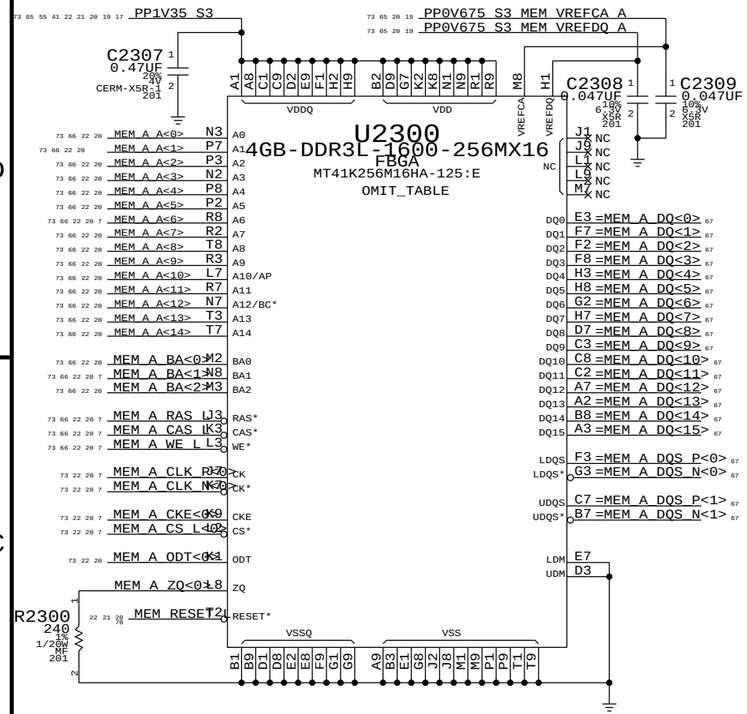
	MEM A VREF DQ	MEM B VREF DQ	MEM A VREF CA	MEM B VREF CA	MEM VREG	
DAC Channel:	A	B	C	C	D	
PCA9557D Pin:	1	2	3	4	5	
	LPDDR3 (1.2V)		DDR3L (1.35V)		LPDDR3 (1.2V)	DDR3L (1.35V)
Nominal value	0.600V (DAC: 0x2E.5)		0.675V (DAC: 0x34)		1.200V (DAC: 0x5D)	1.343V (DAC: 0x68)
Margined target:	0.300V - 0.900V (+/- 300mV)		0.337V - 1.013V (+/- 337.5mV)		0.800V - 1.600V (+/- 400mV)	0.972V - 1.714V (+/- 371mV)
DAC range:	0.000V - 1.199V (0x00 - 0x5D)		0.000V - 1.354V (0x00 - 0x69)		0.000V - 2.397V (0x00 - 0xBA)	0.000V - 2.694V (0x00 - 0xD1)
VRef current:	+73uA - -73uA (- = sourced)		+82uA - -82uA (- = sourced)		+21uA - -21uA (- = sourced)	+25uA - -25uA (- = sourced)
DAC step size:	6.36mV / step @ output		6.36mV / step @ output		4.28mV / step @ output	3.53mV / step @ output

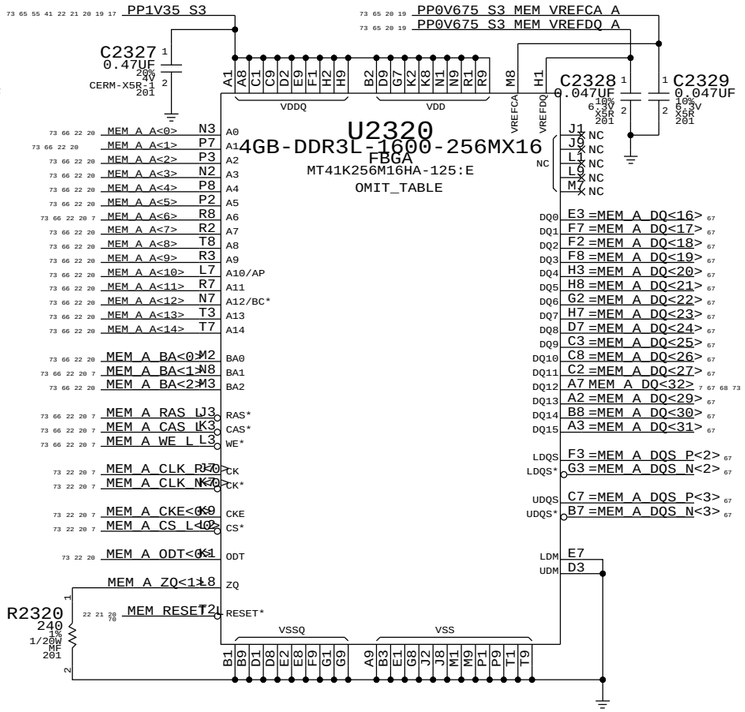
SYNC_MASTER=J44 SYNC_DATE=08/12/2013

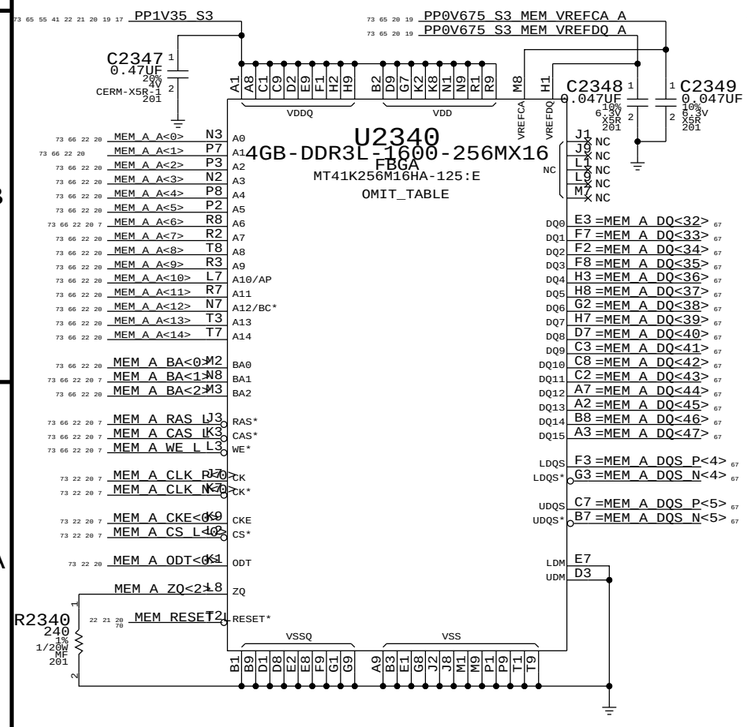
PAGE TITLE: DDR3 VREF MARGINING

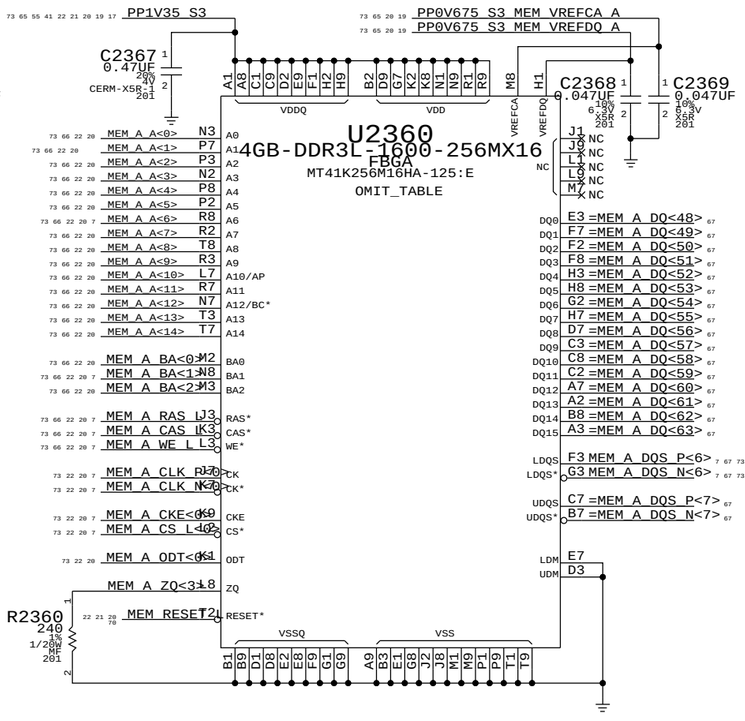
Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D
REVISION: <E4LABEL>
BRANCH: <BRANCH>
PAGE: 22 OF 120
SHEET: 19 OF 78

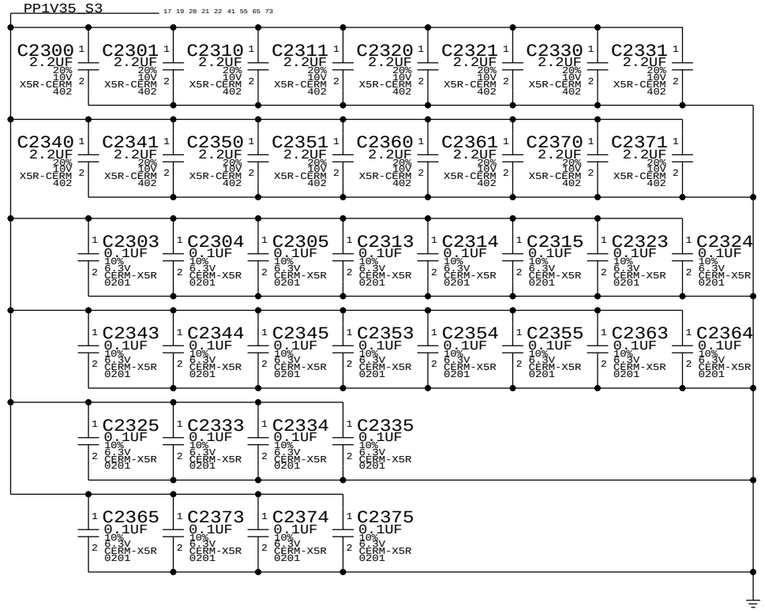








SDRAM BYPASSING (NOTE: 4X 2.2UF AND 6X 0.1UF PER CHIP)



SYNC_MASTER=MASTER SYNC_DATE=MASTER

PAGE TITLE: DDR3 SDRAM Bank A (Rank 0)

Apple Inc.

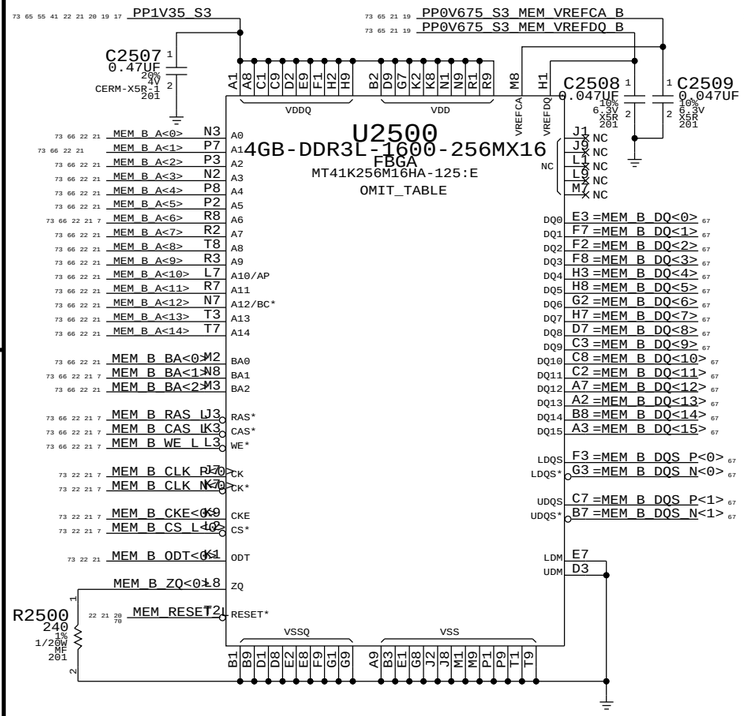
DRAWING NUMBER: <SCH_NUM> SIZE: D

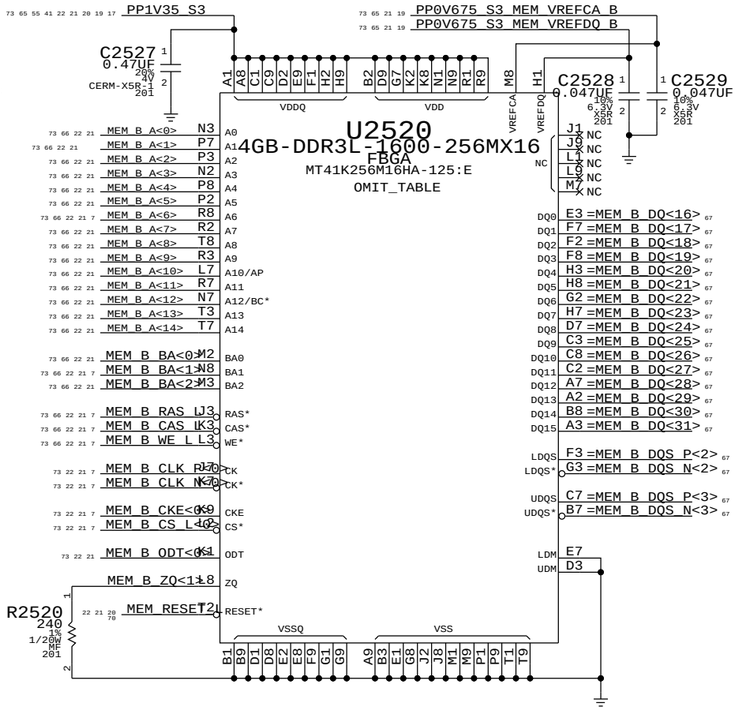
REVISION: <E4LABEL>

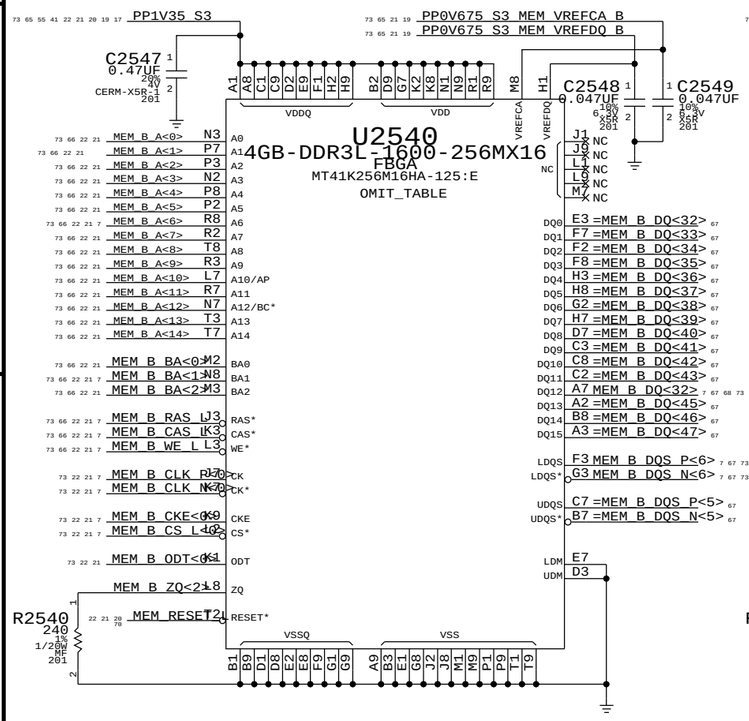
BRANCH: <BRANCH>

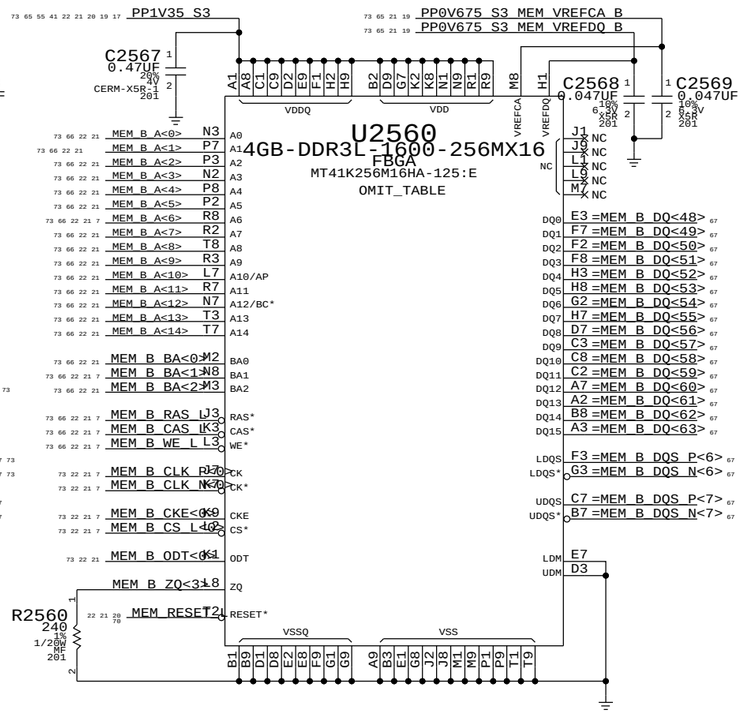
PAGE: 23 OF 120

SHEET: 20 OF 78

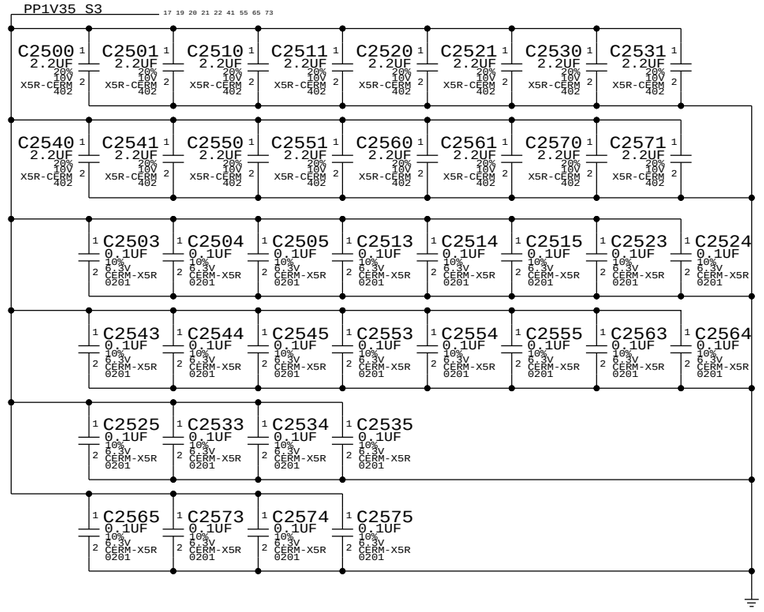








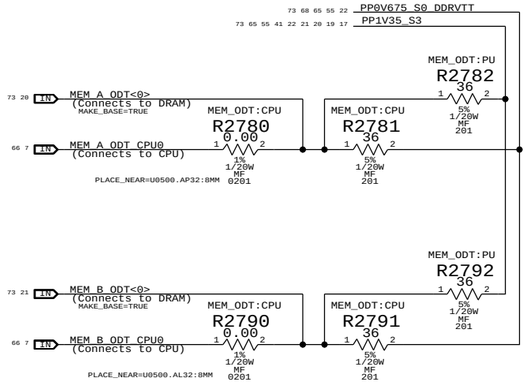
SDRAM BYPASSING (NOTE: 4X 2.2UF AND 6X 0.1UF PER CHIP)



SYNC_MASTER=MASTER	SYNC_DATE=MASTER
PAGE TITLE: DDR3 SDRAM BANK B (RANK 0)	
Apple Inc.	DRAWING NUMBER: <SCH_NUM> SIZE: D
	REVISION: <E4LABEL>
	BRANCH: <BRANCH>
	PAGE: 25 OF 120
	SHEET: 21 OF 78

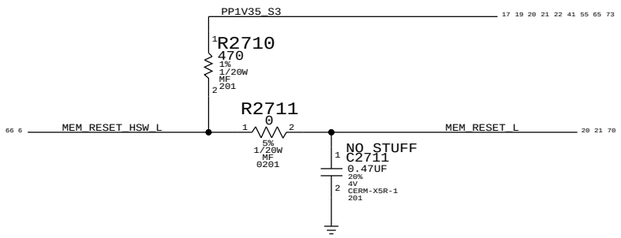
Memory ODT Option

MEM_ODT:CPU drives ODT from CPU, terminated to 0.675V VTT.
MEM_ODT:PU disconnect ODT from CPU, ODT pins on DRAM pulled up to 1.35V VDDQ.



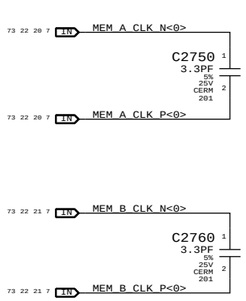
Memory Reset Pull Up

Reset is an open drain in Haswell ULT and needs pull up



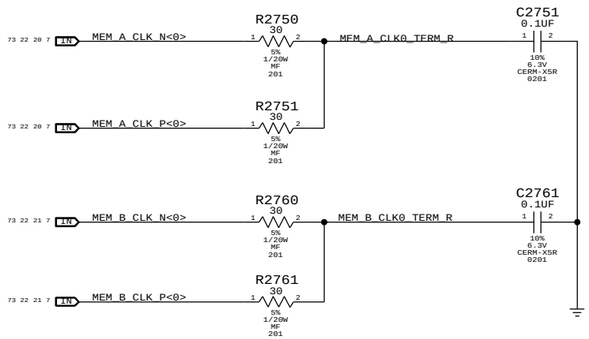
Memory Clock Near-End Termination

Place Source C termination before first DRAM

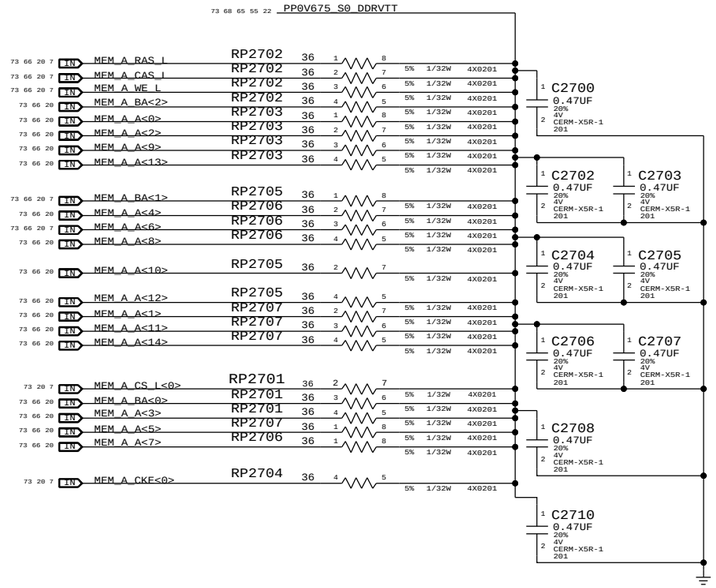


Memory Clock Far-End Termination

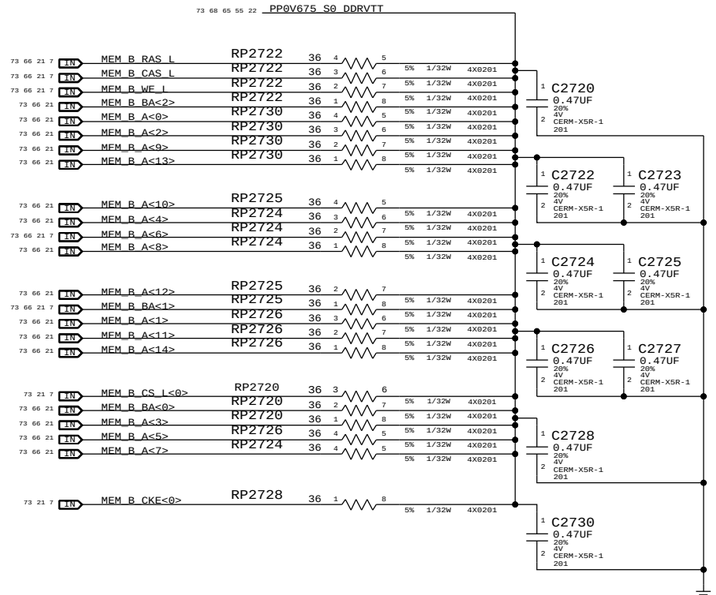
Place RC end termination after last DRAM



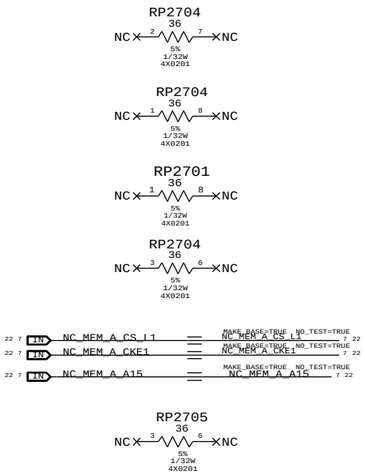
Memory CMD/CTL Termination - Channel A



Memory CMD/CTL Termination - Channel B



MEMORY RPACK SPARES



SYNC_MASTER=J44_YONAS-4GB	SYNC_DATE=04/02/2013
PAGE TITLE: DDR3 Termination	
Apple Inc.	DRAWING NUMBER: <SCH_NUM> SIZE: D
	REVISION: <E4LABEL>
NOTICE OF PROPRIETARY PROPERTY: THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. THE POSESSOR AGREES TO THE FOLLOWING: I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE II NOT TO REPRODUCE OR COPY IT III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART IV ALL RIGHTS RESERVED	BRANCH: <BRANCH>
	PAGE: 27 OF 120
	SHEET: 22 OF 78

CRITICAL
OMIT_TABLE

U2800
REDWOOD-RIDGE
FCBGA
(1 OF 2)

PCIE GEN2

PCIE_TBT_R2D_C_P<0>	C2800 0.1UF	PCIE_TBT_R2D_P<0>	AB9	PERP_0	
PCIE_TBT_R2D_C_N<0>	C2801 0.1UF	PCIE_TBT_R2D_N<0>	AA10	PERN_0	
PCIE_TBT_R2D_C_P<1>	C2802 0.1UF	PCIE_TBT_R2D_P<1>	AA12	PERP_1	
PCIE_TBT_R2D_C_N<1>	C2803 0.1UF	PCIE_TBT_R2D_N<1>	AB13	PERN_1	
PCIE_TBT_R2D_C_P<2>	C2804 0.1UF	PCIE_TBT_R2D_P<2>	AB15	PERP_2	
PCIE_TBT_R2D_C_N<2>	C2805 0.1UF	PCIE_TBT_R2D_N<2>	AA16	PERN_2	
PCIE_TBT_R2D_C_P<3>	C2806 0.1UF	PCIE_TBT_R2D_P<3>	AA18	PERP_3	
PCIE_TBT_R2D_C_N<3>	C2807 0.1UF	PCIE_TBT_R2D_N<3>	AB19	PERN_3	
		PCH_TBT_PCIE_RESET_L	P5	PERST_OD_N	
		TBT_PWR_ON_POC_RST_L	R4	PWR_ON_POC_RSTN	

PETP_0	AD5	PCIE_TBT_D2R_C_P<0>	C2840 0.1UF → PCIE_TBT_D2R_P<0>
PETN_0	AD7	PCIE_TBT_D2R_C_N<0>	C2841 0.1UF → PCIE_TBT_D2R_N<0>
PETP_1	AD9	PCIE_TBT_D2R_C_P<1>	C2842 0.1UF → PCIE_TBT_D2R_P<1>
PETN_1	AD11	PCIE_TBT_D2R_C_N<1>	C2843 0.1UF → PCIE_TBT_D2R_N<1>
PETP_2	AD13	PCIE_TBT_D2R_C_P<2>	C2844 0.1UF → PCIE_TBT_D2R_P<2>
PETN_2	AD15	PCIE_TBT_D2R_C_N<2>	C2845 0.1UF → PCIE_TBT_D2R_N<2>
PETP_3	AD17	PCIE_TBT_D2R_C_P<3>	C2846 0.1UF → PCIE_TBT_D2R_P<3>
PETN_3	AD19	PCIE_TBT_D2R_C_N<3>	C2847 0.1UF → PCIE_TBT_D2R_N<3>

MISC

PP3V3_TBTLC

R2890 3.3K 5% 1/20W MF 201
R2891 3.3K 5% 1/20W MF 201
C2890 1UF 10% 6.3V CERM 402
BYPASS=U2890:2mm
R2892 3.3K 5% 1/20W MF 201
R2893 3.3K 5% 1/20W MF 201

CRITICAL
OMIT_TABLE

U2890
4MBIT
W25X40CLXIG
USON

(TBT_SPI_MOSI)	5	DI/IO0	
(TBT_SPI_CLK)	6	CLK	
(TBT_SPI_CS_L)	1	CS*	
TBTROM_WP_L	3	WP*	
TBTROM_HOLD_L	7	HOLD*	
	8	VCC	
(TBT_SPI_MISO)	2	DO/IO1	
	4	GND	
	9	THRM_PAD	

OMIT
R2815 NOSTUFF 0201

DEBUG: For monitoring current/voltage
TBT_MONOBSP W18 MONOBSP
TBT_MONOBSN W16 MONOBSN

DEBUG: For monitoring clock
TBTTHMSNS_D1_P AB7 THERMDA
Use AA8 GND ball for THERM_DN

TBT_SPI_MOSI	AA2	EE_DI
TBT_SPI_MISO	Y3	EE_DO
TBT_SPI_CS_L	T5	EE_CS_N
TBT_SPI_CLK	U8	EE_CLK

R2829 10K 5% 1/20W MF 201

JTAG_ISP_TDI	W2	TDI
JTAG_TBT_TMS	AB1	TMS
JTAG_ISP_TCK	AA6	TCK
JTAG_TBT_TDO	U6	TDO
TBT_TEST_EN	R6	TEST_EN
TBT_TEST_PWR_GOOD	W8	TEST_PWR_GOOD

R2825 100 5% 1/20W MF 201

RSENSE	U20	TBT_RSENSE
RBIAS	W20	TBT_RBIAS
RSVD	AD1, L8	

R2855 1K 1% 1/20W MF 201

Used for straps in host mode

PCIE_RST_0_N	W6	TP_TBT_PCIE_RESET0_L
PCIE_RST_1_N	AB3	TBT_DFT_STRAP_1
PCIE_RST_2_N	AD3	TBT_ROM_SECURITY_XOR
PCIE_RST_3_N	V1	TBT_DFT_STRAP_3
PCIE_CLKREQ_OD_N	V3	TBT_CLKREQ_L → OUT 12

REFCLK_100_IN_P	AB21	PCIE_CLK100M_TBT_P → IN 12 68 70
REFCLK_100_IN_N	AD21	PCIE_CLK100M_TBT_N → IN 12 68 70
XTAL_25_IN	AA24	SYSCLK_CLK25M_TBT_R
XTAL_25_OUT	AB23	TP_TBT_XTAL25OUT
TMU_CLK_OUT	AA4	TBT_TMU_CLK_OUT

Security strap setting is XORed with bit in the flash, so the active-level depends on the code in the flash.

If strap != bit then security is enabled?

PP3V3_TBTLC
NO STUFF R2867 10K 5% 1/20W MF 201

R2861 10K 5% 1/20W MF 201
R2862 10K 5% 1/20W MF 201
R2863 10K 5% 1/20W MF 201

Divides 3.3V to 1.8V
R2895 806 1% 1/20W MF 201

SYSCLK_CLK25M_TBT → IN 17 71

PP3V3_TBTLC
PP3V3_S4_TBT

NO STUFF R2899 10K 5% 1/20W MF 201
R2896 1K 5% 1/20W MF 201
R2881 100K 5% 1/20W MF 201
R2880 100K 5% 1/20W MF 201
R2882 100K 5% 1/20W MF 201

TBT_EN_CIO_PWR_L
TBT_DDC_XBAR_EN_L
HDMITBTMUX_SEL_TBT
TBTDP_AUXIO_EN
DP_TBTSRC_HPD

PP3V3_TBTLC
R2878 100K 5% 1/20W MF 201
R2879 100K 5% 1/20W MF 201
R2832 100K 5% 1/20W MF 201
R2883 100K 5% 1/20W MF 201

PP3V3_S4_TBT
NO STUFF R2884 100K 5% 1/20W MF 201
NO STUFF R2885 10K 5% 1/20W MF 201
NO STUFF R2886 10K 5% 1/20W MF 201

TBT_BATLOW_L
TBT_A_DP_PWRDN
TBT_B_DP_PWRDN
TBT_A_HV_EN
TBT_B_HV_EN

R2888 10K 5% 1/20W MF 201
R2887 10K 5% 1/20W MF 201

NOTE: The following pins require testpoints:

0 - GPIO_13	8 - GPIO_15
1 - GPIO_1	9 - GPIO_11
2 - GPIO_2	10 - GPIO_14
3 - GPIO_3	11 - GPIO_0
4 - GPIO_5	12 - GPIO_12
5 - PCIE_RST_1_N	13 - GPIO_10
6 - PCIE_RST_2_N	14 - PB_LSTX
7 - PCIE_RST_3_N	15 - PB_LSRX

DISPLAY PORTS

DP_TBTSNK0_ML_P<3>	E14	DPSNK0_3_P	DPSRC_3_P A14 TP_DP_TBTSRC_ML_CP<3>
DP_TBTSNK0_ML_N<3>	D13	DPSNK0_3_N	DPSRC_3_N B15 TP_DP_TBTSRC_ML_CN<3>
DP_TBTSNK0_ML_P<2>	E16	DPSNK0_2_P	DPSRC_2_P A12 TP_DP_TBTSRC_ML_CP<2>
DP_TBTSNK0_ML_N<2>	D15	DPSNK0_2_N	DPSRC_2_N B13 TP_DP_TBTSRC_ML_CN<2>
DP_TBTSNK0_ML_P<1>	E18	DPSNK0_1_P	DPSRC_1_P A10 TP_DP_TBTSRC_ML_CP<1>
DP_TBTSNK0_ML_N<1>	D17	DPSNK0_1_N	DPSRC_1_N B11 TP_DP_TBTSRC_ML_CN<1>
DP_TBTSNK0_ML_P<0>	E20	DPSNK0_0_P	DPSRC_0_P A8 TP_DP_TBTSRC_ML_CP<0>
DP_TBTSNK0_ML_N<0>	D19	DPSNK0_0_N	DPSRC_0_N B9 TP_DP_TBTSRC_ML_CN<0>
DP_TBTSNK0_AUXCH_P	G4	DPSNK0_AUX_P	DPSRC_AUX_P J4 TP_DP_TBTSRC_AUXCH_CP
DP_TBTSNK0_AUXCH_N	G2	DPSNK0_AUX_N	DPSRC_AUX_N J2 TP_DP_TBTSRC_AUXCH_CN
DP_TBTSNK0_HPD	AB5	DPSNK0_HPD	DPSRC_HPD_OD AC2 DP_TBTSRC_HPD → 23

SNK0 AC Coupling

DP_TBTSNK0_ML_C_P<0>	C2820 0.1UF X5R-CERM	DP_TBTSNK0_ML_P<0>	
DP_TBTSNK0_ML_C_N<0>	C2821 0.1UF X5R-CERM	DP_TBTSNK0_ML_N<0>	
DP_TBTSNK0_ML_C_P<1>	C2822 0.1UF X5R-CERM	DP_TBTSNK0_ML_P<1>	
DP_TBTSNK0_ML_C_N<1>	C2823 0.1UF X5R-CERM	DP_TBTSNK0_ML_N<1>	
DP_TBTSNK0_ML_C_P<2>	C2824 0.1UF X5R-CERM	DP_TBTSNK0_ML_P<2>	
DP_TBTSNK0_ML_C_N<2>	C2825 0.1UF X5R-CERM	DP_TBTSNK0_ML_N<2>	
DP_TBTSNK0_ML_C_P<3>	C2826 0.1UF X5R-CERM	DP_TBTSNK0_ML_P<3>	
DP_TBTSNK0_ML_C_N<3>	C2827 0.1UF X5R-CERM	DP_TBTSNK0_ML_N<3>	
DP_TBTSNK0_AUXCH_C_P	C2828 0.1UF X5R-CERM	DP_TBTSNK0_AUXCH_P	
DP_TBTSNK0_AUXCH_C_N	C2829 0.1UF X5R-CERM	DP_TBTSNK0_AUXCH_N	

DP_TBTSNK1_ML_P<3>	E6	DPSNK1_3_P	
DP_TBTSNK1_ML_N<3>	D5	DPSNK1_3_N	
DP_TBTSNK1_ML_P<2>	E8	DPSNK1_2_P	
DP_TBTSNK1_ML_N<2>	D7	DPSNK1_2_N	
DP_TBTSNK1_ML_P<1>	E10	DPSNK1_1_P	
DP_TBTSNK1_ML_N<1>	D9	DPSNK1_1_N	
DP_TBTSNK1_ML_P<0>	E12	DPSNK1_0_P	
DP_TBTSNK1_ML_N<0>	D11	DPSNK1_0_N	
DP_TBTSNK1_AUXCH_P	H3	DPSNK1_AUX_P	
DP_TBTSNK1_AUXCH_N	H1	DPSNK1_AUX_N	
DP_TBTSNK1_HPD	U4	DPSNK1_HPD	

R2830 100K 5% 1/20W MF 201 ← OUT 13 DP_TBTSNK0_HPD

R2831 100K 5% 1/20W MF 201 ← OUT 64 DP_TBTSNK1_HPD

TBT_A_R2D_C_P<0>	G24	PA_CIO0_TX_P/DPSRC_0_P	PB_CIO2_TX_P/DPSRC_0_P R24 TBT_B_R2D_C_P<0>
TBT_A_R2D_C_N<0>	E24	PA_CIO0_TX_N/DPSRC_0_N	PB_CIO2_TX_N/DPSRC_0_N N24 TBT_B_R2D_C_N<0>
TBT_A_D2R_P<0>	G22	PA_CIO0_RX_P	PB_CIO2_RX_P R22 TBT_B_D2R_P<0> → IN
TBT_A_D2R_N<0>	E22	PA_CIO0_RX_N	PB_CIO2_RX_N N22 TBT_B_D2R_N<0> → IN
TBT_A_CONFIG1_BUF	P1	PA_CONFIG1/CIO_0_LSEO	PB_CONFIG1/CIO_2_LSEO D3 TBT_B_CONFIG1_BUF → IN
TBT_A_CONFIG2_RC	K5	PA_CONFIG2/CIO_0_LSOE	PB_CONFIG2/CIO_2_LSOE M1 TBT_B_CONFIG2_RC → IN
TBT_A_R2D_C_P<1>	L24	PA_CIO1_TX_P/DPSRC_2_P	PB_CIO3_TX_P/DPSRC_2_P W24 TBT_B_R2D_C_P<1>
TBT_A_R2D_C_N<1>	J24	PA_CIO1_TX_N/DPSRC_2_N	PB_CIO3_TX_N/DPSRC_2_N U24 TBT_B_R2D_C_N<1>
TBT_A_D2R_P<1>	L22	PA_CIO1_RX_P	PB_CIO3_RX_P W22 TBT_B_D2R_P<1> → IN
TBT_A_D2R_N<1>	J22	PA_CIO1_RX_N	PB_CIO3_RX_N U22 TBT_B_D2R_N<1> → IN
TBT_A_LSTX	N8	PA_LSTX/CIO_1_LSEO	PB_LSTX/CIO_3_LSEO M5 TBT_B_LSTX
TBT_A_LSRX	J6	PA_LSRX/CIO_1_LSOE	PB_LSRX/CIO_3_LSOE P7 TBT_B_LSRX → IN
DP_TBTPA_ML_C_P<1>	A16	PA_DPSRC_1_P	PB_DPSRC_1_P A20 DP_TBTPB_ML_C_P<1>
DP_TBTPA_ML_C_N<1>	B17	PA_DPSRC_1_N	PB_DPSRC_1_N B21 DP_TBTPB_ML_C_N<1>
DP_TBTPA_ML_C_P<3>	A18	PA_DPSRC_3_P	PB_DPSRC_3_P A22 DP_TBTPB_ML_C_P<3>
DP_TBTPA_ML_C_N<3>	B19	PA_DPSRC_3_N	PB_DPSRC_3_N B23 DP_TBTPB_ML_C_N<3>
DP_TBTPA_AUXCH_C_P	L4	PA_AUX_P	PB_AUX_P K3 DP_TBTPB_AUXCH_C_P
DP_TBTPA_AUXCH_C_N	L2	PA_AUX_N	PB_AUX_N K1 DP_TBTPB_AUXCH_C_N
DP_TBTPA_HPD	M3	PA_DPSRC_HPD	PB_DPSRC_HPD N6 DP_TBTPB_HPD → IN
TBT_A_HV_EN	R8	GPIO_0/PA_HV_EN/BYP0	GPIO_1/PB_HV_EN/BYP0 F1 TBT_B_HV_EN
TBT_A_CIO_SEL	N2	GPIO_10/PA_CIO_SEL/BYP1	GPIO_11/PB_CIO_SEL/BYP1 R2 TBT_B_CIO_SEL
TBT_A_DP_PWRDN	P3	GPIO_12/PA_DP_PWRDN/BYP2	GPIO_13/PB_DP_PWRDN/BYP2 F3 TBT_B_DP_PWRDN

		GPIO_2/TMU_CLK_IN/AC_PRESENT	U2 TBT_GPIO2
		GPIO_3/FORCE_PWR	L6 TBT_PWR_EN → IN 15
		GPIO_4/WAKE_OD_N	H5 SMC_PME_S4_DARK_L → OUT 18 36 37
		GPIO_5/CIO_PLUG_EVENT_N/HV_OK_OD	Y7 TBT_CIO_PLUG_EVENT_L → OUT 15 18 72
		GPIO_6_OD/CIO_SDA_OD	Y1 HDMITBTMUX_SEL_TBT → IN 15 23 64 66
		GPIO_7_OD/CIO_SCL_OD	T7 TBT_GPIO7
		GPIO_8/EN_CIO_PWR_OD*	V7 TBT_EN_CIO_PWR_L → OUT 23 24
		GPIO_9/SX_CTRL_OD*	M7 TBT_BATLOW_L → IN 23 25
		GPIO_14	T1 TBTDP_AUXIO_EN → OUT 23 26 27
		GPIO_15	T3 TBT_DDC_XBAR_EN_L → OUT 23 28

For unused port, pull CONFIG1, CONFIG2, LSRX, HPD and CIO_SEL low (10k). All other port signals can be NC.

SNK1 AC Coupling

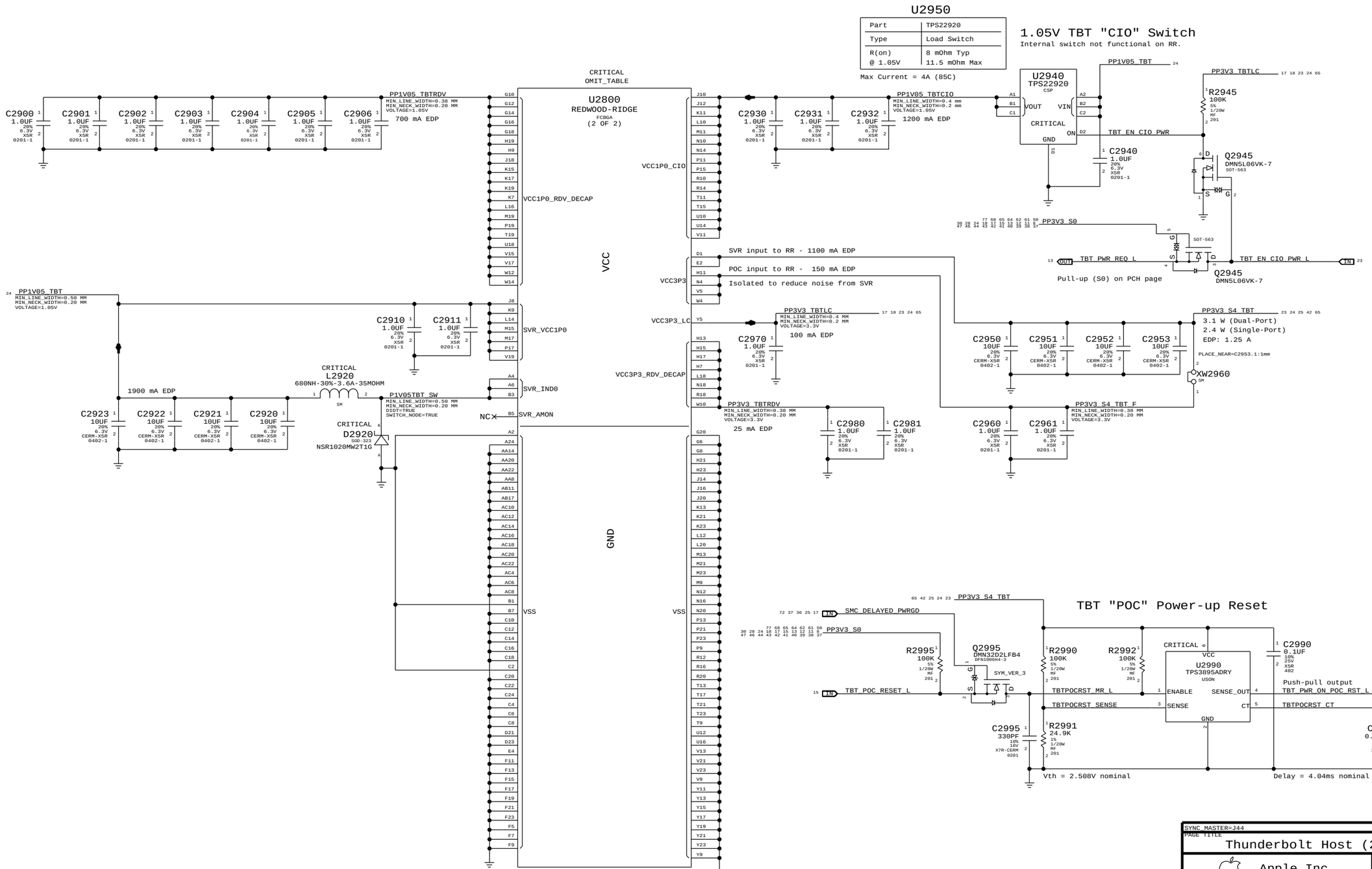
DP_TBTSNK1_ML_C_P<0>	C2830 0.1UF X5R-CERM	DP_TBTSNK1_ML_P<0>	
DP_TBTSNK1_ML_C_N<0>	C2831 0.1UF X5R-CERM	DP_TBTSNK1_ML_N<0>	
DP_TBTSNK1_ML_C_P<1>	C2832 0.1UF X5R-CERM	DP_TBTSNK1_ML_P<1>	
DP_TBTSNK1_ML_C_N<1>	C2833 0.1UF X5R-CERM	DP_TBTSNK1_ML_N<1>	
DP_TBTSNK1_ML_C_P<2>	C2834 0.1UF X5R-CERM	DP_TBTSNK1_ML_P<2>	
DP_TBTSNK1_ML_C_N<2>	C2835 0.1UF X5R-CERM	DP_TBTSNK1_ML_N<2>	
DP_TBTSNK1_ML_C_P<3>	C2836 0.1UF X5R-CERM	DP_TBTSNK1_ML_P<3>	
DP_TBTSNK1_ML_C_N<3>	C2837 0.1UF X5R-CERM	DP_TBTSNK1_ML_N<3>	
DP_TBTSNK1_AUXCH_C_P	C2838 0.1UF X5R-CERM	DP_TBTSNK1_AUXCH_P	
DP_TBTSNK1_AUXCH_C_N	C2839 0.1UF X5R-CERM	DP_TBTSNK1_AUXCH_N	

SYNC_MASTER=J44 SYNC_DATE=08/12/2013

PAGE TITLE
Thunderbolt Host (1 of 2)

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D
REVISION <E4LABEL>
BRANCH <BRANCH>
PAGE 28 OF 120
SHEET 23 OF 78



EDP current / power consumption figures copied from R68 schematic (Rev 2, dated October 28, 2012, not available on IBL).

SYNC_MASTER=J44 SYNC_DATE=08/12/2013

PAGE TITLE: Thunderbolt Host (2 of 2)

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D
REVISION: <E4LABEL>
BRANCH: <BRANCH>
PAGE: 29 OF 120
SHEET: 24 OF 78

Page Notes

Power aliases required by this page:
- =PPVIN_SW_TBTBST (8-13V Boost Input)
- =PP15V_TBT_REG (15V Boost Output)

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

Thunderbolt 15V Boost Regulator

68 65 58 52 51 40 PPBUS_G3H
8-13V Input
Changes required
for 2S.

CRITICAL
Q3080
SI8409DB
8GA

SI8409DB:
Vds(max): -30V
Vgs(max): +/-12V
Vgs(th): -1.4V
Rds(on): 46mOhm @ 4.5V Vgs
Id(max): 3.7A @ 70C

PPVIN_SW_TBTBST
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm

Voltage not specified here,
add property on another page.

R3080 470K 5% 1/10W MF-LF 402
C3080 0.1UF 10% 25V X5R 402
TBTBST_PWREN_DIV_L

R3081 330K 5% 1/16W MF-LF 402
TBTBST_PWREN_L

Q3005
DMN32D2LFB4
DFN1006H4-3
SYM_VER_2
TBT_A_HV_EN

Second FET needed for
dual-port designs.

R3092 73.2K 1% 1/16W MF-LF 402
<R2>

C3085 2.2UF 20% 10V X5R-CERM 402
C3086 2.2UF 20% 10V X5R-CERM 402
C3092 2.2UF 20% 10V X5R-CERM 402
C3087 68PF 5% 50V COG-CERM 0402
C3093 0.0033UF 10% 50V X7R-CERM 0402

R3091 200K 1% 1/10W MF-LF 402
<R1>

R3093 49.9K 1% 1/16W MF-LF 402
R3094 26.7K 1% 1/16W MF-LF 402

C3094 0.33UF 10% 6.3V CERM-X5R 402

GND_TBTBST_SGND
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=0V

UVLO(falling) = 1.22 * (R1 + R2) / R2
UVLO(rising) = UVLO(falling) + (2uA * R1)
UVLO = 4.55V (falling), 4.95 (rising)

C3090 10UF 20% 25V X5R-CERM 0603
C3091 10UF 20% 25V X5R-CERM 0603

CRITICAL
L3095
3.3UH-6.5A
PIM0063T-SM

TBTBST_BOOST
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
SWITCH_NODE=TRUE
DIDT=TRUE

CRITICAL
VIN
SW

U3090
LT3957
QFN

TBTBST_EN_UVLO
TBTBST_INTVCC
TBTBST_VC
TBTBST_RT
TBTBST_SS
TBTBST_VC_RC
SYNC
SGND
GND

SGND shorted to
GND inside package,
no XW necessary.

TBTBST_SNS1
TBTBST_SNS2
TBTBST_VSNS
TBTBST_FBX

R3089 0 5% 1/20W MF 0201
CRITICAL
D3095 PDS540XF PWRDI5

XW3095 SM
PLACE_NEAR=C3095.1:2 mm

NC
NC

C3088 10PF 5% 50V C0G-CERM 0402
R3095 137K 1% 1/16W MF-LF 402
<Ra>

NO STUFF
C3089 100PF 5% 50V CERM 402
R3096 15.8K 1% 1/16W MF-LF 402
<Rb>

C3095 33UF-0.060HM 20% 25V POLY-TANT CASE-D3L

PP15V_TBT
Vout = 15.47V
Max Current = 2A?
FREQ = 480KHZ

C3096 10UF 10% 25V X5R 1206-2
NO STUFF
C3097 10UF 10% 25V X5R 805
C3099 0.001UF 10% 50V X7R-CERM 0402

Vout = 1.6V * (1 + Ra / Rb)

Q3088
DMN5L06VK-7
SOT-563

Max Vgs: 10V

R3088 330K 5% 1/16W MF-LF 402
TBTBST_SHDN_DIV
R3087 330K 5% 1/16W MF-LF 402

Q3088
DMN5L06VK-7
SOT-563

SMC_DELAYED_PWRGD

BATLOW# Isolation

Q3000
DMN32D2LFB4
DFN1006H4-3
SYM_VER_3

PP3V3_S4_TBT
Pull-up on RR page
PM_BATLOW_L
TBT_BATLOW_L
TBT_BATLOW_L
MAKE_BASE=TRUE

SYNC_MASTER=J44	SYNC_DATE=08/12/2013
PAGE TITLE	Thunderbolt Mobile Support
Apple Inc.	DRAWING NUMBER <SCH_NUM> SIZE D
	REVISION <E4LABEL>
	BRANCH <BRANCH>
	PAGE 30 OF 120
	SHEET 25 OF 78

3.3V/HV Power MUX

V3P3 must be S4 to support
wake from Thunderbolt devices.

	Nominal	Min	Max	
IV3P3	1100mA	1030mA	1200mA	
IHVS0	890mA	830mA	930mA	(assumes 15V, 12W minimum)
IHVS3	890mA	830mA	930mA	(assumes 3S, 9-12.6V, 7.5-11.7W)

PP3V3_S5
CRITICAL
C3287 100UF 20% 6.3V POLY-TANT CASE-B2-SM
C3280 22UF 20% 6.3V X5R-CERM-1 603
C3281 0.1UF 10% 16V X5R-CERM 0201
PP15V_TBT
15.75V Max
C3215 4.7UF 10% 25V X5R-CERM 0603
C3210 0.1UF 10% 25V X5R 402
CRITICAL
U3210
CD3211A0RGPR
QFN
V3P3
V3P3OUT
VHV
OUT
ENHVU
FAULTZ
EN
ISET_V3P3
HV_EN
ISET_S0
S0
ISET_S3
GND
THRM PAD
C3285 0.1UF 10% 16V X5R-CERM 0201
C3286 10UF 20% 6.3V CERM-X5R 0402
C3211 0.1UF 10% 25V X5R 402
PP3V3_S4_TBTAPWR
MIN_LINE_WIDTH=0.38 MM
MIN_NECK_WIDTH=0.20 MM
VOLTAGE=3.3V
PP3V3RHV_S4_TBTAPWR
MIN_LINE_WIDTH=0.38 MM
MIN_NECK_WIDTH=0.20 MM
VOLTAGE=15V
S4_PWR_EN
TBT_A_HV_EN
PM_SLP_S3_BUF_L
TBTAPWRSW_ISET_V3P3
TBTAPWRSW_ISET_S0
TBTAPWRSW_ISET_S3
TBTHV:P15V
R3210 22.6K 1% 1/20W MF 201
R3211 22.6K 1% 1/20W MF 201
R3212 36.5K 1% 1/20W MF 201 <RV3P3>
12V: See below
TBTAPWRSW_ISET_S3_R
TBTAPWRSW_ISET_S0_R
R3213 22.6K 1% 1/20W MF 201 <RHVS3>
R3214 22.6K 1% 1/20W MF 201 <RHVS0>
Single-fault protection requires two R's per HV ISET_Sx with CD3210. Single R on ISET_V3P3 OK.
ILIM = 40000 / RISET

For 12V systems:

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
118S0145	2	RES,MTL FILM,1/20W,17.8K,1,0201,SMD,LF	R3210,R3213		TBTHV:P12V
118S0145	2	RES,MTL FILM,1/20W,17.8K,1,0201,SMD,LF	R3211,R3214		TBTHV:P12V

	Nominal	Min	Max	
IHVS0/S3	1120mA	1090mA	1170mA	(12W minimum)

Thunderbolt Connector A

CRITICAL
L3200 FERR-120-OHM-3A 0603
C3200 0.01UF 10% 50V X7R-CERM 0402
PP3V3RHV_S4_TBTAPWR_F
TBTACONN_20_RC
R3201 12 5% 1/20W MF 201
C3201 0.01UF 10% 50V X7R-CERM 0402
TBT Dir
DP Dir
TBT: RX_0
TBT: Unused
TBT: RX_1
DP Source must pull down HPD input with greater than or equal to 100K (DPv1.1a).
Sink HPD range:
High: 2.0 - 5.0V
Low: 0 - 0.8V
C3202 0.01UF 10% 16V X5R-CERM 0201
R3252 1M 5% 1/20W MF 201
R3251 1M 5% 1/20W MF 201
C3294 330PF 10% 16V X7R-CERM 0201
C3295 330PF 10% 16V X7R-CERM 0201
R3241 100K 5% 1/20W MF 201
R3294 1K 5% 1/20W MF 201
R3295 1K 5% 1/20W MF 201
R3279 470K 5% 1/20W MF 201
R3278 470K 5% 1/20W MF 201
GND_VOID=TRUE (Both C's)
C3274 0.47UF 20% 4V 201 CERM-X5R-1
C3275 0.47UF 20% 4V 201 CERM-X5R-1
C3278 0.22UF 20% 6.3V X5R 0201
C3279 0.22UF 20% 6.3V X5R 0201
TBT_A_D2R_P<0>
TBT_A_D2R_N<0>
TBT_A_D2R_C_P<0>
TBT_A_D2R_C_N<0>
DP_TBTPA_ML_C_P<3>
DP_TBTPA_ML_C_N<3>
DP_TBTPA_ML_P<3>
DP_TBTPA_ML_N<3>
TBT_A_D2R1_AUXDDC_P
TBT_A_D2R1_AUXDDC_N
TBT_A_HPD
TBT_A_CONFIG1_RC
TBT_A_CONFIG2_RC
NO_XNET_CONNECTION=TRUE

CRITICAL
J3200 MDP-J44 F-RT-TH
SHIELD PINS
S16 S15 S14 S13 S12
HPD CONFIG1 CONFIG2 GND2 ML_LANE3P ML_LANE3N GND4 AUX_CHP AUX_CHN DP_PWR
GND0 ML_LANE0P ML_LANE0N GND1 ML_LANE1P ML_LANE1N GND3 ML_LANE2P ML_LANE2N RETURN
PORT B
SHIELD PINS
S24 S23 S22 S21 S20 S19 S18 S17
514-0876

PP3V3_S4_TBTAPWR
C3220 0.1UF 10% 16V X5R-CERM 0201
SIGNAL_MODEL=TBT_MUX
VDD
CRITICAL
U3220
CBTL05024
HVQFN24-COMBO
GND_THMPAD
TB-
TB+
AUX-
AUX+ (IPU) AUXIO- (IPD) AUXIO+
DDC_DAT
DDC_CLK
CA_DETOUT
DP+
DP-
LSTX (IPU)
LSRX (IPD)
HPDOUT
TB_ENA
AUXIO_EN
DP_PD
CA_DET
DPML0+
DPML0-
HPD
TBT: RX_1
TBT: LSX_A_R2P/R2R (P/N)
GND_VOID=TRUE (Both C's)
C3277 0.47UF 20% 4V 201 CERM-X5R-1
C3276 0.47UF 20% 4V 201 CERM-X5R-1
C3230 0.1UF 10% 16V X5R-CERM 0201
C3231 0.1UF 10% 16V X5R-CERM 0201
C3232 0.22UF 20% 6.3V X5R 0201
C3233 0.22UF 20% 6.3V X5R 0201
TBT_A_D2R_C_N<1>
TBT_A_D2R_C_P<1>
DP_TBTPA_AUXCH_C_N
DP_TBTPA_AUXCH_C_P
DP_TBTPA_DDC_DATA
DP_TBTPA_DDC_CLK
TBT_A_CONFIG1_BUF
DP_TBTPA_ML_C_P<1>
DP_TBTPA_ML_C_N<1>
TBT_A_LSTX
TBT_A_LSRX
DP_TBTPA_HPD
TBT_A_CIO_SEL
TBTDP_AUXIO_EN
DP_PD_PWRDN
TBT_A_D2R1_AUXDDC_N
TBT_A_D2R1_AUXDDC_P
TBT_A_CONFIG1_RC
TBT_A_DP_PWRDN
TBT_A_HPD
DP_A_LSX_ML_P<1>
DP_A_LSX_ML_N<1>

TBTACONN_1_C
MIN_LINE_WIDTH=0.38 MM
MIN_NECK_WIDTH=0.20 MM
VOLTAGE=18.9V
(0-18.9V)
C3205 0.01UF 10% 25V X5R-CERM 0201
TBTACONN_7_C
C3206 0.01UF 10% 25V X5R-CERM 0201
GND_VOID=TRUE (Both C's)
C3270 0.22UF 20% 6.3V X5R 0201
C3271 0.22UF 20% 6.3V X5R 0201
C3272 0.22UF 20% 6.3V X5R 0201
C3273 0.22UF 20% 6.3V X5R 0201
R3270 470K 5% 1/20W MF 201
R3271 470K 5% 1/20W MF 201
R3272 470K 5% 1/20W MF 201
R3273 470K 5% 1/20W MF 201
TBT_A_R2D_C_P<0>
TBT_A_R2D_C_N<0>
TBT_A_R2D_P<0>
TBT_A_R2D_N<0>
TBT_A_R2D_C_P<1>
TBT_A_R2D_C_N<1>
TBT_A_R2D_P<1>
TBT_A_R2D_N<1>
TBT: TX_0
TBT: TX_1
470K R's for ESD protection on AC-coupled signals.

SYNC_MASTER=J44 SYNC_DATE=08/12/2013
PAGE TITLE
Thunderbolt Connector A
Apple Inc.
DRAWING NUMBER <SCH_NUM> SIZE D
REVISION <E4LABEL>
BRANCH <BRANCH>
PAGE 32 OF 120
SHEET 26 OF 78

3.3V/HV Power MUX

V3P3 must be S4 to support
wake from Thunderbolt devices.

PP3V3_S5

CRITICAL
C3387 100UF 20% 6.3V POLY-TANT CASE-B2-SM
C3380 22UF 20% 6.3V X5R-CERM-1 603
C3381 0.1UF 10% 16V X5R-CERM 0201

	Nominal	Min	Max	
IV3P3	1100mA	1030mA	1200mA	
IHVS0	890mA	830mA	930mA	(assumes 15V, 12W minimum)
IHVS3	890mA	830mA	930mA	(assumes 3S, 9-12.6V, 7.5-11.7W)

PP15V_TBT
15.75V Max

C3315 4.7UF 10% 25V X5R-CERM 0603
C3310 0.1UF 10% 25V X5R 402

CRITICAL
U3310
CD3211A0RGPR
QFN

19,20	V3P3	V3P3OUT	18
6,7	VHV	OUT	12,14
16	ENHVU	FAULTZ	4
5	EN	ISET_V3P3	8
11	HV_EN	ISET_S0	10
17	S0	ISET_S3	9
	GND	THRM PAD	21

C3385 0.1UF 10% 16V X5R-CERM 0201
C3386 10UF 20% 6.3V CERM-X5R 0402
C3311 0.1UF 10% 25V X5R 402

PP3V3_S4_TBTBPWR
MIN_LINE_WIDTH=0.38 MM
MIN_NECK_WIDTH=0.20 MM
VOLTAGE=3.3V

PP3V3RHV_S4_TBTBPWR
MIN_LINE_WIDTH=0.38 MM
MIN_NECK_WIDTH=0.20 MM
VOLTAGE=15V

S4_PWR_EN
TBT_B_HV_EN
PM_SLP_S3_BUF_L

TBTBPWRSW_ISET_V3P3
TBTBPWRSW_ISET_S0
TBTBPWRSW_ISET_S3
TBTBPWRSW_ISET_S3_R
TBTBPWRSW_ISET_S0_R

TBTHV:P15V
R3310 22.6K 1% 1/20W MF 201
R3311 22.6K 1% 1/20W MF 201
R3312 36.5K 1% 1/20W MF 201 <RV3P3>
12V: See below
R3313 22.6K 1% 1/20W MF 201 <RHVS3>
R3314 22.6K 1% 1/20W MF 201 <RHVS0>

Single-fault protection
requires two R's per HV
ISET_Sx with CD3210.
Single R on ISET_V3P3 OK.

ILIM = 40000 / RISET

For 12V systems:

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
118S0145	2	RES,MTL FILM,1/20W,17.8K,1,0201,SMD,LF	R3310,R3313		TBTHV:P12V
118S0145	2	RES,MTL FILM,1/20W,17.8K,1,0201,SMD,LF	R3311,R3314		TBTHV:P12V

	Nominal	Min	Max	
IHVS0/S3	1120mA	1090mA	1170mA	(12W minimum)

Thunderbolt Connector B

CRITICAL
L3300 FERR-120-OHM-3A 0603

C3300 0.01UF 10% 16V X7R-CERM 0402
C3301 0.01UF 10% 50V X7R-CERM 0402
C3302 0.01UF 10% 16V X5R-CERM 0201

TBTBCONN_20_RC
MIN_LINE_WIDTH=0.38 MM
MIN_NECK_WIDTH=0.20 MM
VOLTAGE=18V

R3301 12 5% 1/20W MF 201

TBT Dir / DP Dir

TBT: RX_0

GND_VOID=TRUE (Both C's)

C3374 0.47UF 20% 4V 201 CERM-X5R-1
C3375 0.47UF 20% 4V 201 CERM-X5R-1

TBT_B_D2R_P<0>
TBT_B_D2R_N<0>
TBT_B_D2R_C_P<0>
TBT_B_D2R_C_N<0>

R3394 1K 5% 1/20W MF 201 NO_XNET_CONNECTION=TRUE
R3395 1K 5% 1/20W MF 201 NO_XNET_CONNECTION=TRUE

C3378 0.22UF 20% 6.3V XSR 0201
C3379 0.22UF 20% 6.3V XSR 0201

DP_TBTPB_ML_C_P<3>
DP_TBTPB_ML_C_N<3>
DP_TBTPB_ML_P<3>
DP_TBTPB_ML_N<3>

TBT: Unused

R3379 470K 5% 1/20W MF 201
R3378 470K 5% 1/20W MF 201

TBT_B_D2R1_AUXDDC_P
TBT_B_D2R1_AUXDDC_N

TBT: RX_1

TBT_B_HPD
TBT_B_CONFIG1_RC
TBT_B_CONFIG2_RC

R3352 1M 5% 1/20W MF 201
R3351 1M 5% 1/20W MF 201
C3394 330PF 10% 16V X7R-CERM 0201
C3395 330PF 10% 16V X7R-CERM 0201
R3341 100K 5% 1/20W MF 201

DP Source must pull
down HPD input with
greater than or equal
to 100K (DPv1.1a).

Sink HPD range:
High: 2.0 - 5.0V
Low: 0 - 0.8V

CRITICAL
J3200
MDP-J44
F-RT-TH
SHIELD PINS
PORT A

A2	HPD	GND0	A1
A4	CONFIG1	ML_LANE0P	A3
A6	CONFIG2	ML_LANE0N	A5
A8	GND2	GND1	A7
A10	ML_LANE3P	ML_LANE1P	A9
A12	ML_LANE3N	ML_LANE1N	A11
A14	GND4	GND3	A13
A16	AUX_CHP	ML_LANE2P	A15
A18	AUX_CHN	ML_LANE2N	A17
A20	DP_PWR	RETURN	A19

SHIELD PINS: S5 S4 S3 S2 S1 / S23 S11 S10 S9 S8 S7 S6

514-0876

GND_VOID=TRUE (Both C's)

C3377 0.47UF 20% 4V 201 CERM-X5R-1
C3376 0.47UF 20% 4V 201 CERM-X5R-1
C3330 0.1UF 10% 16V X5R-CERM 0201
C3331 0.1UF 10% 16V X5R-CERM 0201

TBT_B_D2R_C_N<1>
TBT_B_D2R_C_P<1>
DP_TBTPB_AUXCH_N
DP_TBTPB_AUXCH_P

C3332 0.22UF 20% 6.3V X5R 0201
C3333 0.22UF 20% 6.3V X5R 0201

DP_TBTPB_ML_C_P<1>
DP_TBTPB_ML_C_N<1>
DP_TBTPB_ML_N<1>
TBT_B_LSTX
TBT_B_LSRX
DP_TBTPB_HPD

C3320 0.1UF 10% 16V X5R-CERM 0201

PP3V3_S4_TBTBPWR

CRITICAL
U3320
CBTL05024
HVQFN24-COMBO
SIGNAL_MODEL=TBT_MUX

TB-		TB_ENA	TBT_B_CIO_SEL
TB+		AUXIO_EN	TBTDP_AUXIO_EN
		DP_PD	TBT_B_DP_PWRDN
AUX-			
AUX+		(IPU) AUXIO-	TBT_B_D2R1_AUXDDC_N
		(IPD) AUXIO+	TBT_B_D2R1_AUXDDC_P
DDC_DAT			
DDC_CLK			
CA_DETOUT		CA_DET	TBT_B_CONFIG1_RC
DP+			
DP-			
		DPML0+	DP_B_LSX_ML_P<1>
		DPML0-	DP_B_LSX_ML_N<1>
LSTX (IPU)			
LSRX (IPD)			
HPDOUT		HPD	TBT_B_HPD
GND_THMPAD			

TBT: RX_1
TBT: LSX_A_R2P/P2R (P/N)

DP_TBTPB_DDC_DATA
DP_TBTPB_DDC_CLK
TBT_B_CONFIG1_BUF

TBTBCONN_1_C
MIN_LINE_WIDTH=0.38 MM
MIN_NECK_WIDTH=0.20 MM
VOLTAGE=18.9V
(0-18.9V)

C3305 0.01UF 10% 25V X5R-CERM 0201

TBTBCONN_7_C
MIN_LINE_WIDTH=0.38 MM
MIN_NECK_WIDTH=0.20 MM
VOLTAGE=18.9V
(0-18.9V)

C3306 0.01UF 10% 25V X5R-CERM 0201

TBT: TX_0

GND_VOID=TRUE (Both C's)

C3370 0.22UF 20% 6.3V XSR 0201
C3371 0.22UF 20% 6.3V XSR 0201

TBT_B_R2D_C_P<0>
TBT_B_R2D_C_N<0>

R3370 470K 5% 1/20W MF 201
R3371 470K 5% 1/20W MF 201

DP_B_LSX_ML_P<1>
DP_B_LSX_ML_N<1>

TBT: LSX_R2P/P2R (P/N)

C3372 0.22UF 20% 6.3V XSR 0201
C3373 0.22UF 20% 6.3V XSR 0201

TBT_B_R2D_C_P<1>
TBT_B_R2D_C_N<1>

R3372 470K 5% 1/20W MF 201
R3373 470K 5% 1/20W MF 201

TBT: TX_1

470k R's for ESD protection
on AC-coupled signals.

SYNC_MASTER=J44 SYNC_DATE=08/12/2013

PAGE TITLE: Thunderbolt Connector B

Apple Inc.

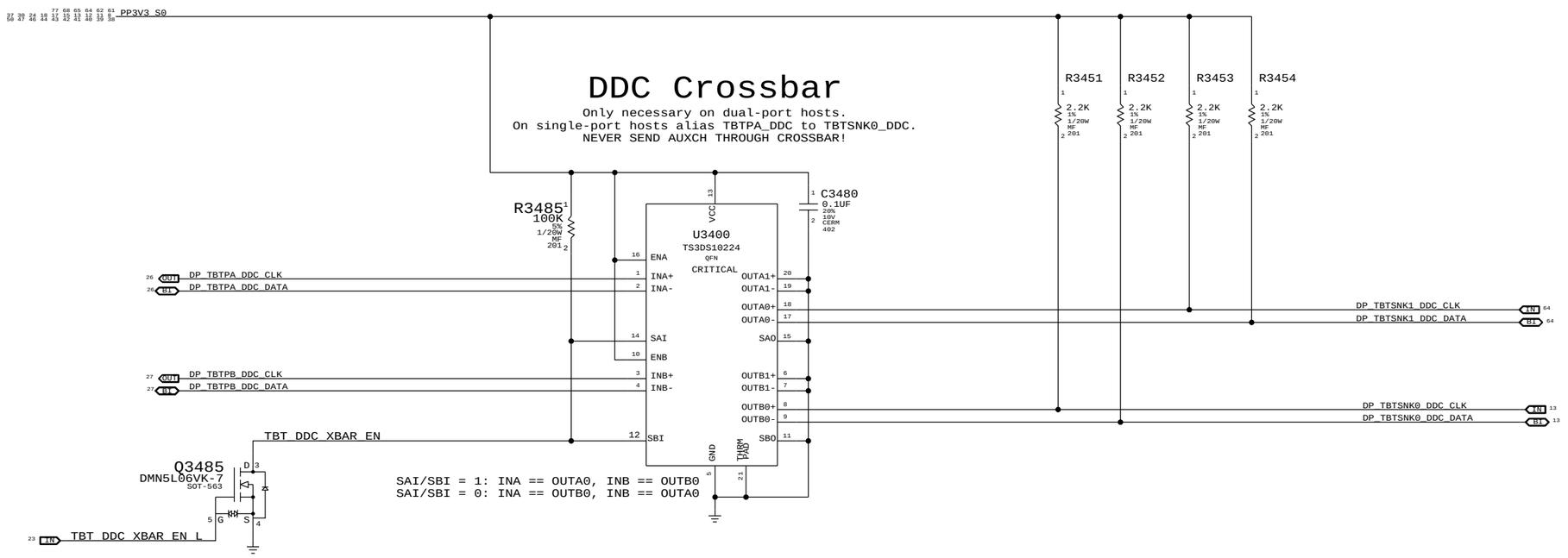
DRAWING NUMBER: <SCH_NUM> SIZE: D
REVISION: <E4LABEL>
BRANCH: <BRANCH>
PAGE: 33 OF 120
SHEET: 27 OF 78

DDC Pull-Ups

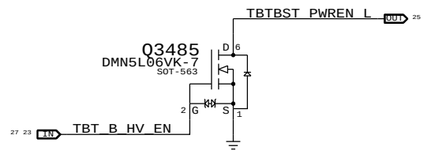
2.2k pull-ups are required by PCH
to indicate active display interface.

DP++ spec violation, should remove!

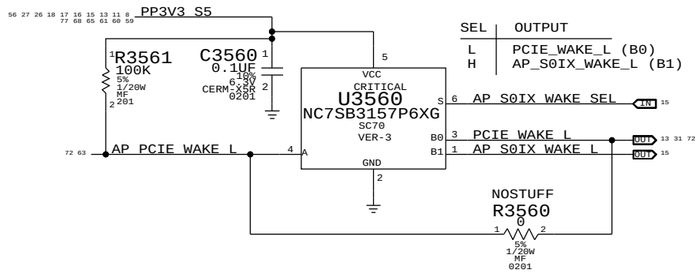
NOTE: Only DDC_DATA is sensed, so DDC_CLK
pull-ups are unstuffed.



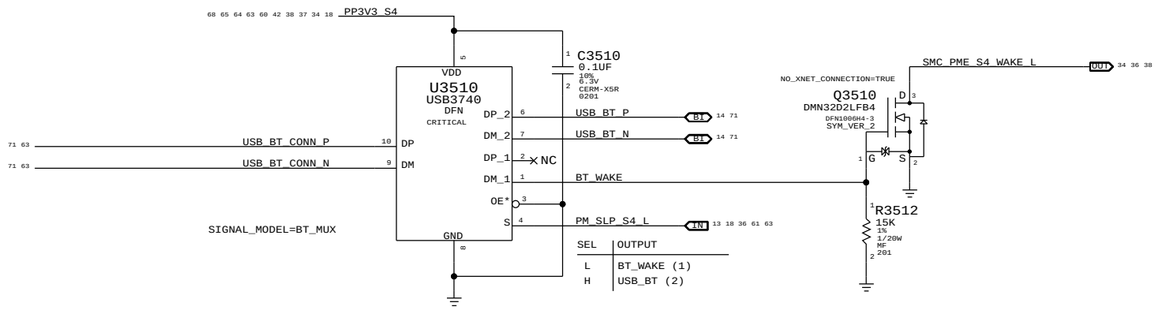
Second FET needed for
dual-port designs.
CONNECTS TO TBTBTS_PWREN_L ON PAGE 30.



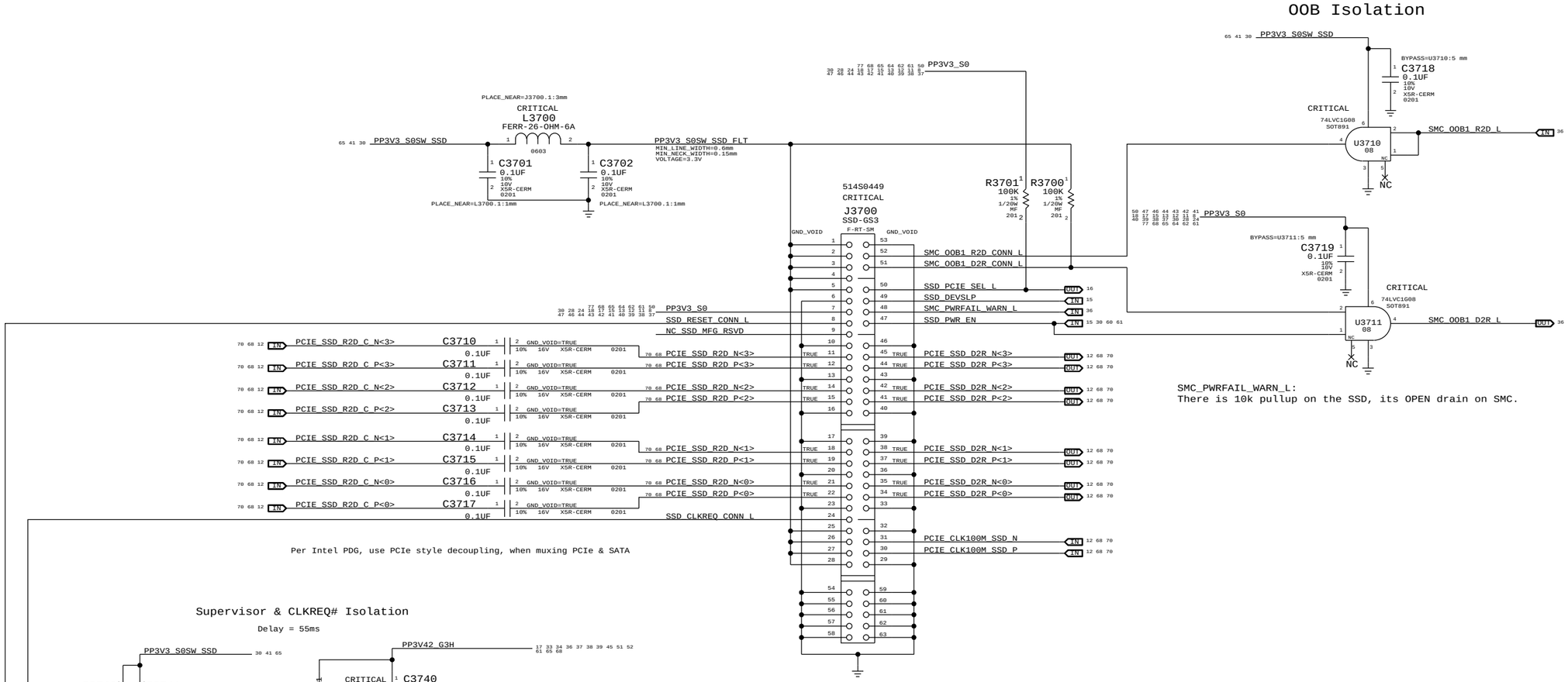
PCIe Wake Muxing



BLUETOOTH



SYNC_MASTER=J44	SYNC_DATE=08/12/2013
PAGE TITLE	WIRELESS SUPPORT
	Apple Inc.
DRAWING NUMBER	<SCH_NUM>
SIZE	D
REVISION	<E4LABEL>
BRANCH	<BRANCH>
PAGE	35 OF 120
SHEET	29 OF 78



SYNC_MASTER=J44 SYNC_DATE=08/12/2013

PAGE TITLE: SSD Connector

Apple Inc.

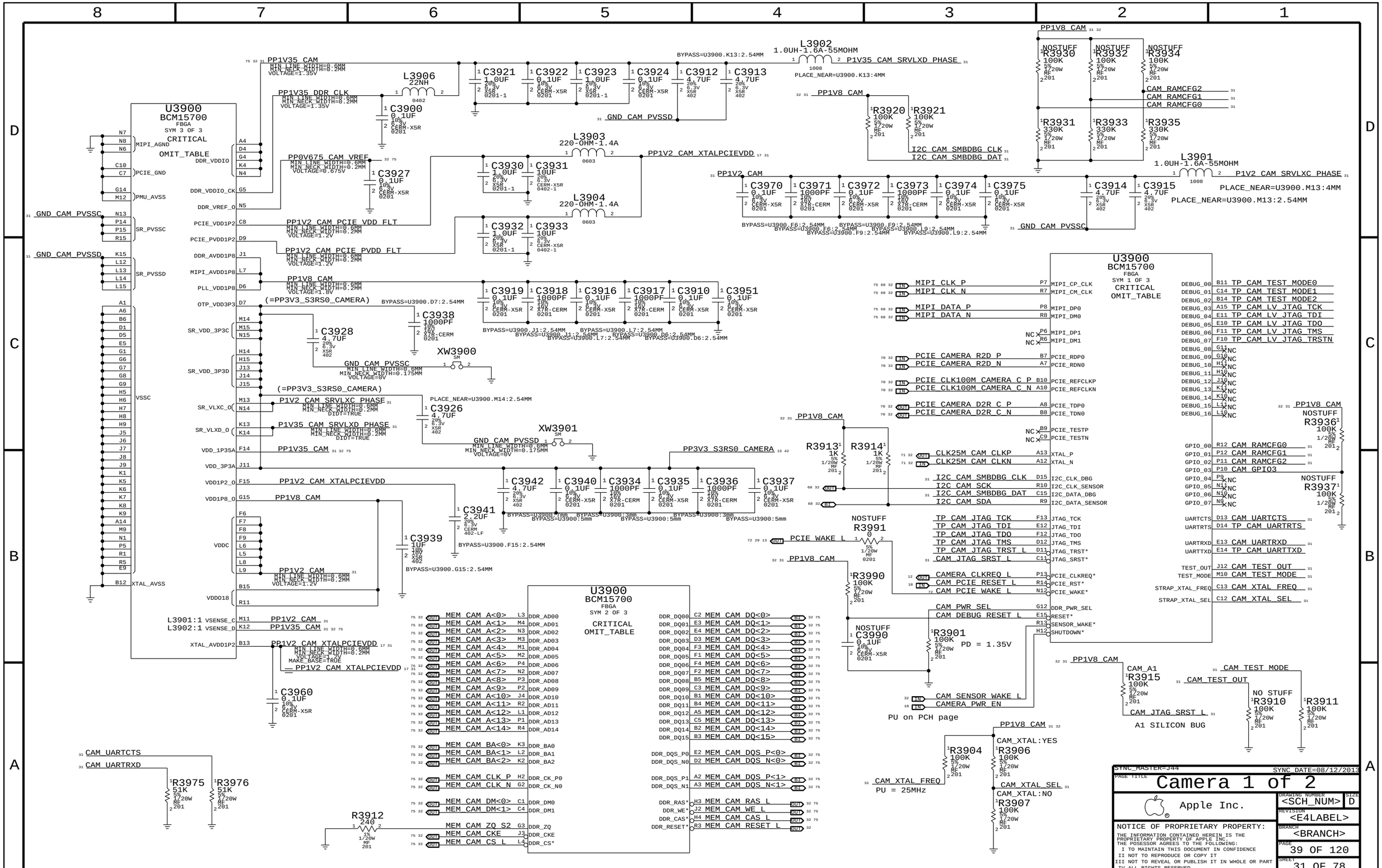
DRAWING NUMBER: <SCH_NUM> SIZE: D

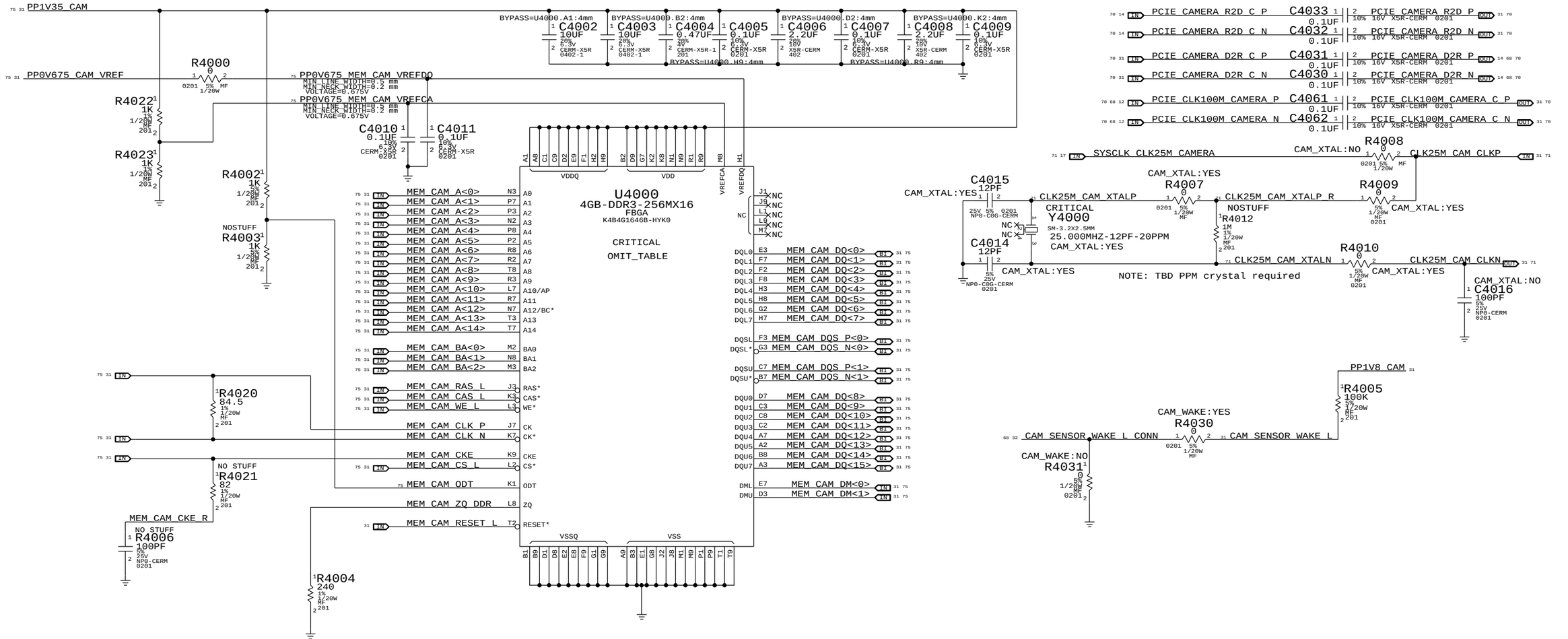
REVISION: <E4LABEL>

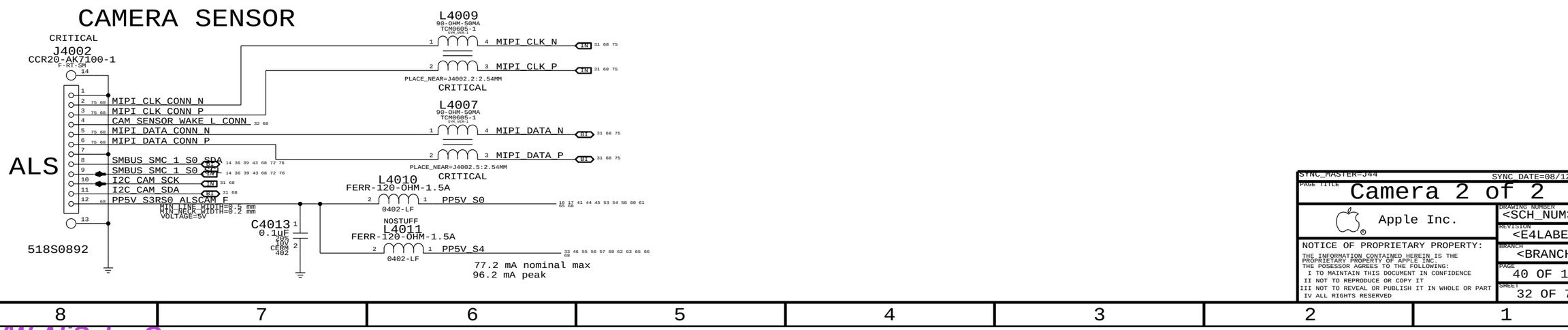
BRANCH: <BRANCH>

PAGE: 37 OF 120

SHEET: 30 OF 78







SYNC_MASTER=J44 SYNC_DATE=08/12/2013

PAGE TITLE: Camera 2 of 2

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

REVISION: <E4LABEL>

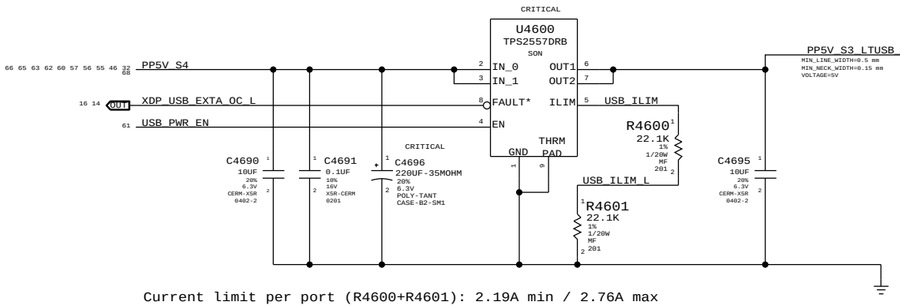
BRANCH: <BRANCH>

PAGE: 40 OF 120

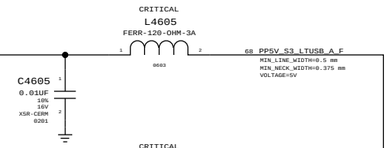
SHEET: 32 OF 78

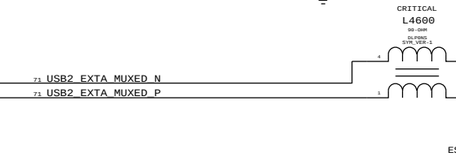
RIGHT USB PORT A

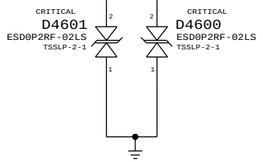
USB Port Power Switch

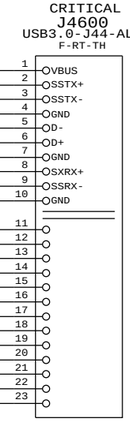


Current limit per port (R4600+R4601): 2.19A min / 2.76A max



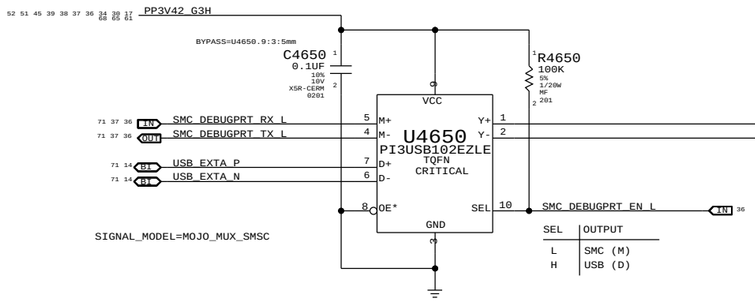


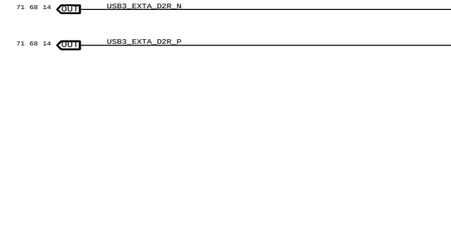


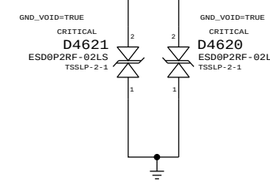


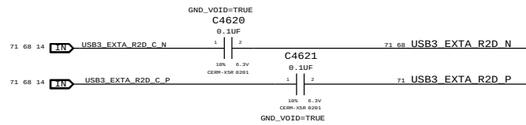
Mojo SMC Debug Mux

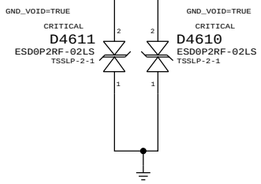
THE PI3USB102E CAN CLAMP VOLTAGE IN THE INTERNAL USB PINS











SYNC_MASTER=J44 SYNC_DATE=08/12/2013

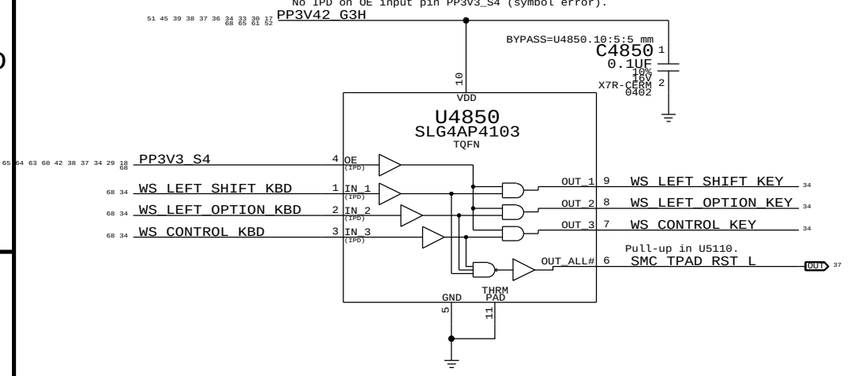
PAGE TITLE: External A USB3 Connector

Apple Inc.

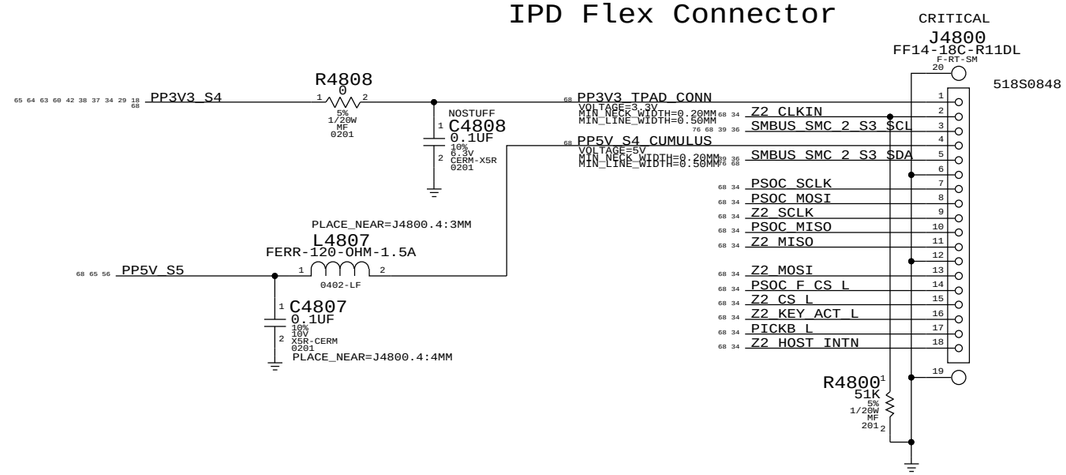
DRAWING NUMBER: <SCH_NUM> SIZE: D
REVISION: <E4LABEL>
BRANCH: <BRANCH>
PAGE: 46 OF 120
SHEET: 33 OF 78

SMC Manual Reset & Isolation

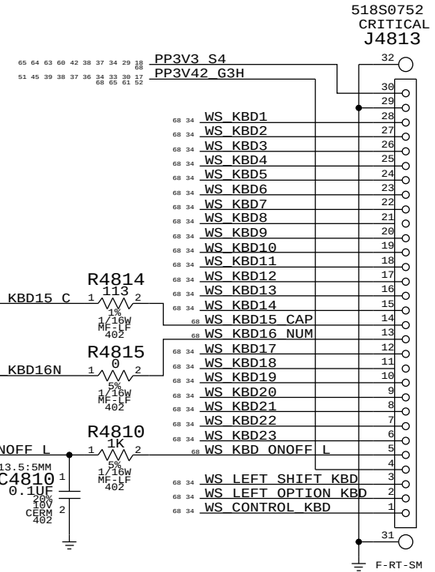
Left shift, option & control keys combined with power button cause SMC RESET# assertion.
Keys ANDed with PSoC power to isolate when PSoC is not powered.
No IPD on OE input pin PP3V3_S4 (symbol error).



IPD Flex Connector

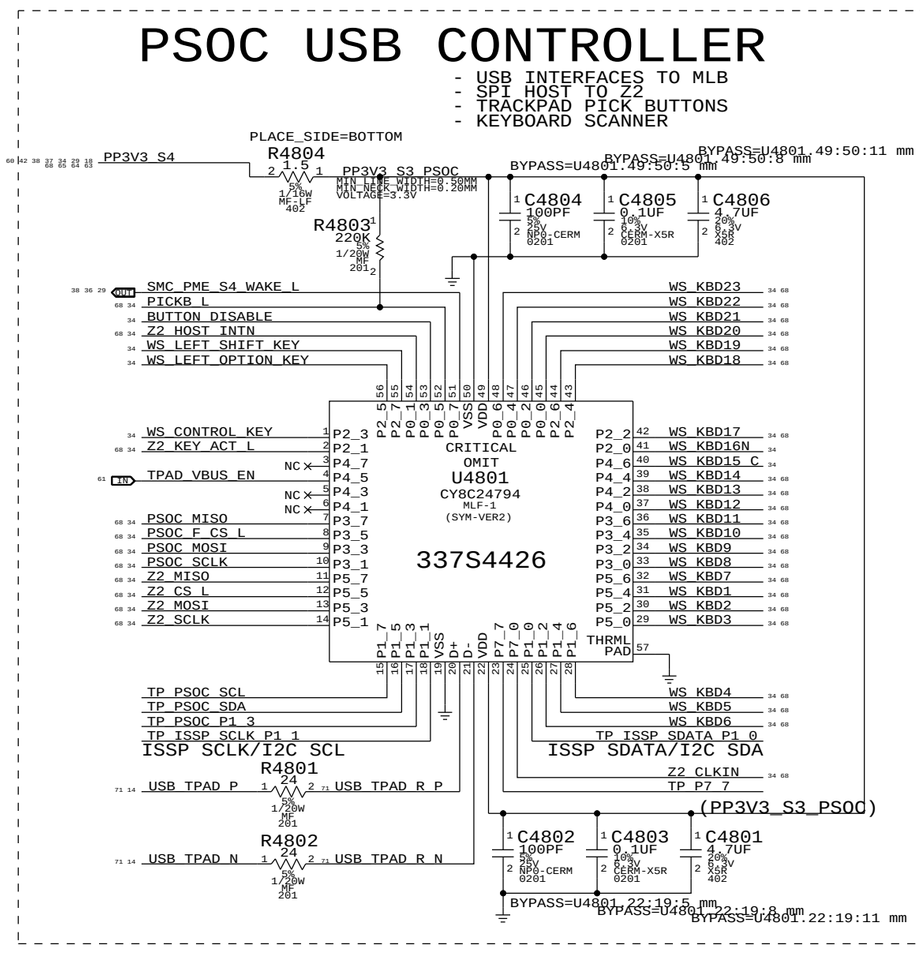


Keyboard Connector

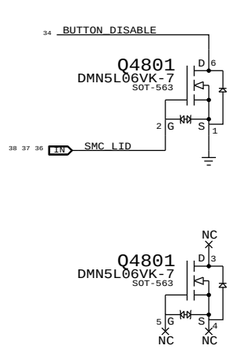


PSOC USB CONTROLLER

- USB INTERFACES TO MLB
- SPI HOST TO Z2
- TRACKPAD PICK BUTTONS
- KEYBOARD SCANNER



TPAD Buttons Disable



PLACE THESE COMPONENTS CLOSE TO J4800
THIS ASSUMES THERE'S A PP3V42_G3H PULL UP ON MLB

THE TPAD BUTTONS WILL BE DISABLE
WHEN THE LID IS CLOSED
LID OPEN => SMC_LID_LC ~ 3.42V
LID CLOSE => SMC_LID_LC < 0.50V

IC	PIN NAME	CURRENT	R_SNS	V_SNS	POWER
TMP102	V+	10UA	2.55 KOHM	0.0255 V	0.255E-6 W
		80UA		0.204 V	16.32E-6 W
3V3 LDO	VDD	60MA (MAX)	10 OHM	0.6 V	36E-3 W
	VOUT	60MA (MAX)	0.2 OHM	0.012 V	0.72E-3 W
PSOC	VDD	8MA (TYP)	1.5 OHM	0.012 V	96E-6 W
		14MA (MAX)		0.021 V	294E-6 W
18V BOOSTER	VIN	4MA (MAX)	4.7 OHM	0.0188 V	75.2E-6 W

SYNC_MASTER=J44 SYNC_DATE=08/12/2013

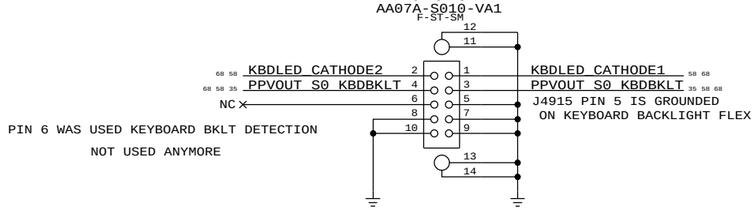
PAGE TITLE: KEYBOARD/TRACKPAD (1 OF 2)

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D
REVISION: <E4LABEL>
BRANCH: <BRANCH>
PAGE: 48 OF 120
SHEET: 34 OF 78

Keyboard Backlight Connector

516S0899
CRITICAL
J4915
AA07A-S010-VA1
F-ST-SM



PIN 6 WAS USED KEYBOARD BKLT DETECTION
NOT USED ANYMORE

J4915 PIN 5 IS GROUNDED
ON KEYBOARD BACKLIGHT FLEX

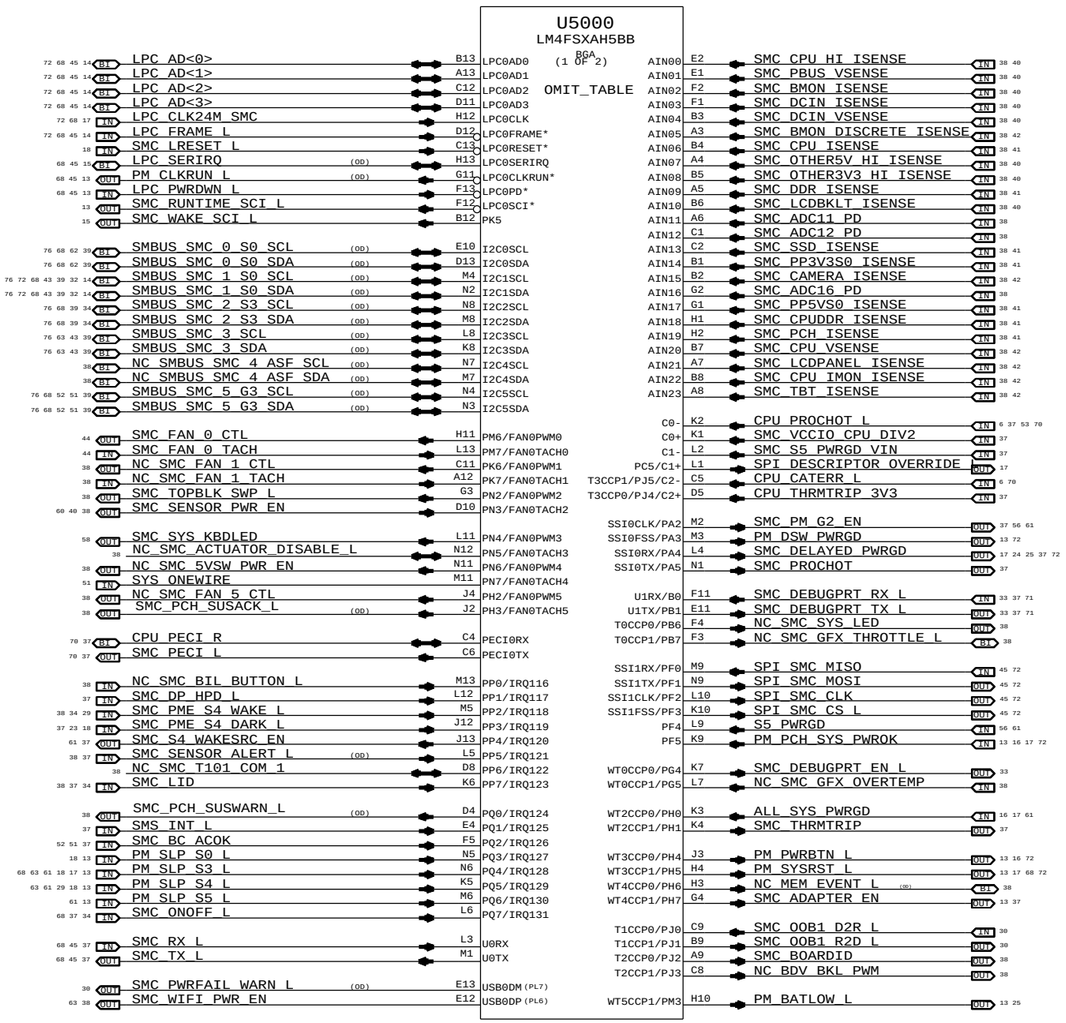
OUT

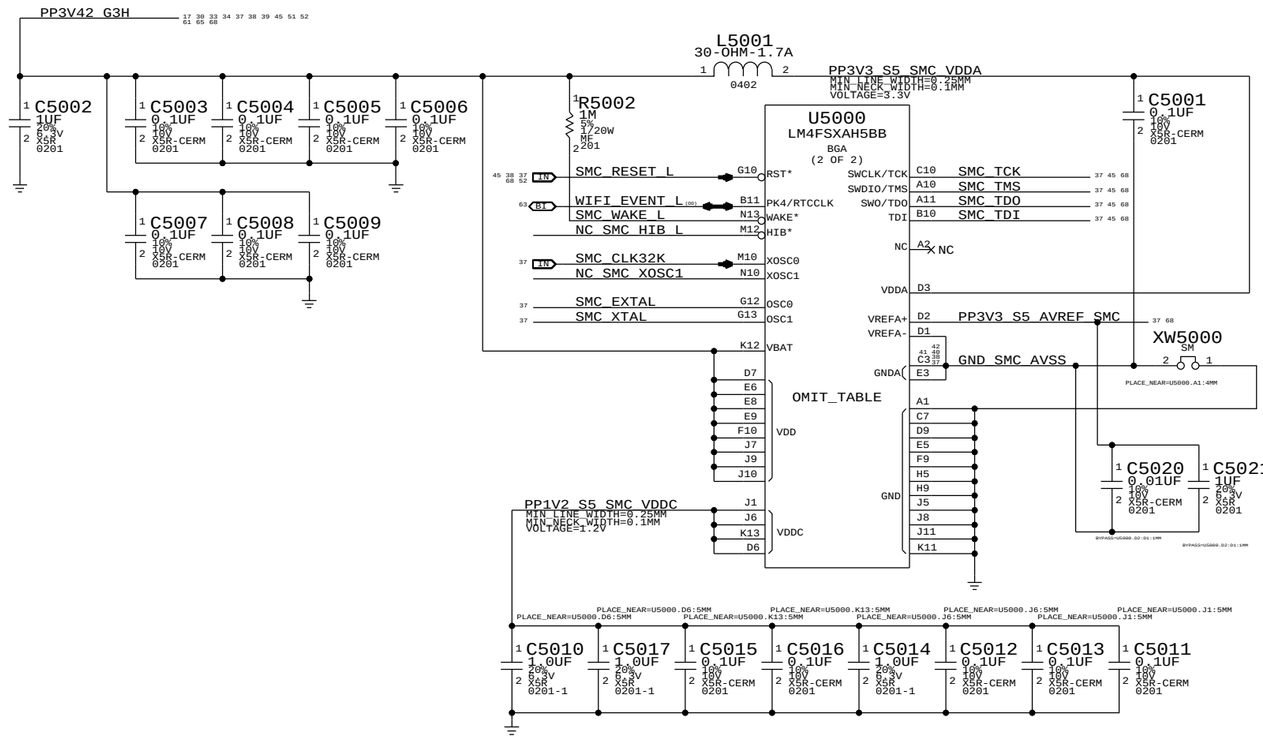
SYNC_MASTER=J44 SYNC_DATE=08/12/2013

PAGE TITLE
KEYBOARD/TRACKPAD (2 OF 2)

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D
REVISION <E4LABEL>
BRANCH <BRANCH>
PAGE 49 OF 120
SHEET 35 OF 78





NOTE:
SMS INTERRUPT IS NOT USED, PULL UP TO SMC RAIL.

NOTE:
Unused pins have "SMC_Pxx" names. Unused pins designed as outputs can be left floating, those designated as inputs require pull-ups.

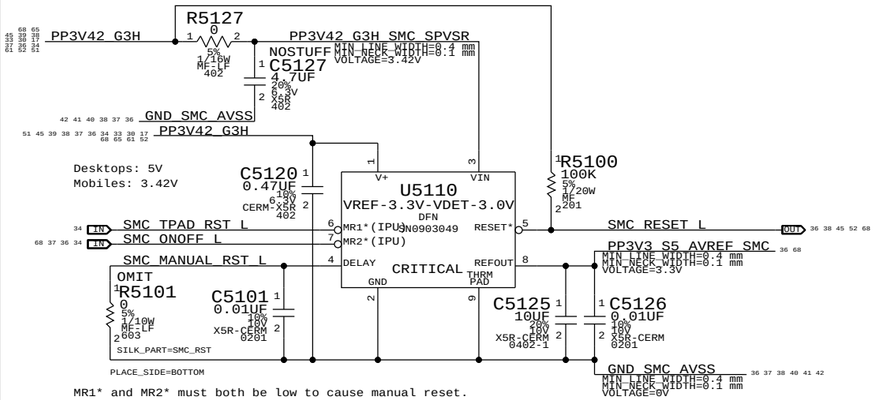
SYNC_MASTER=J44 SYNC_DATE=08/12/2013

PAGE TITLE: SMC

Apple Inc.

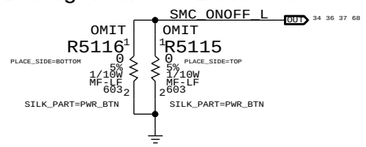
DRAWING NUMBER: <SCH_NUM> SIZE: D
REVISION: <E4LABEL>
BRANCH: <BRANCH>
PAGE: 50 OF 120
SHEET: 36 OF 78

SMC Reset "Button", Supervisor & AVREF Supply



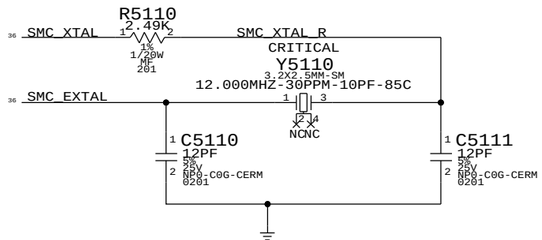
MR1* and MR2* must both be low to cause manual reset.
Used on mobiles to support SMC reset via keyboard.
NOTE: Internal pull-ups are to VIN, not V+.

Debug Power "Buttons"



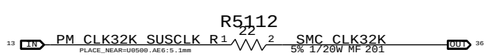
SMC Crystal Circuit

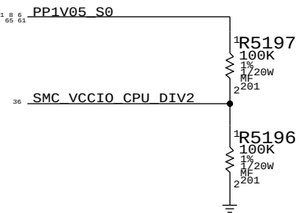
SMC USB Clock require these crystal
values:5,6,8,10,12,16,18,20,24,25 MHz

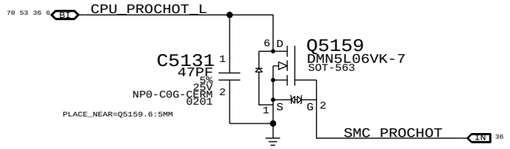


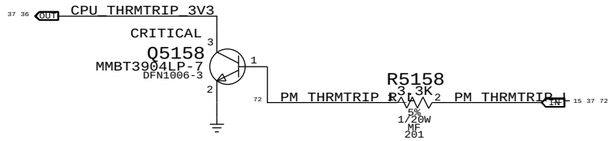
SMC_BC_ACOK — SMC_BC_ACOK (MAKE_BASE=TRUE)

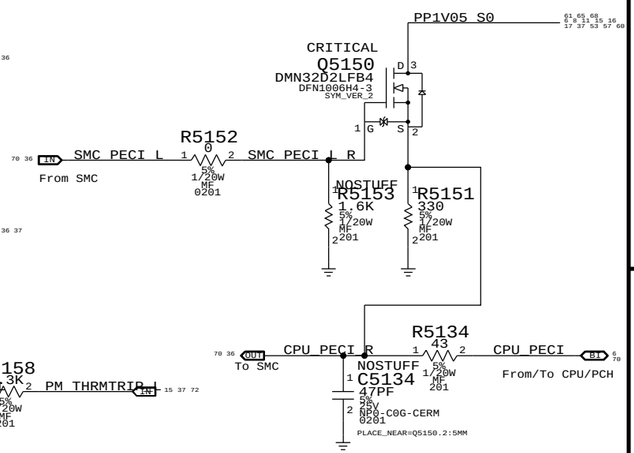
SMC_PME_S4_DARK_L — SMC_PME_S4_DARK_L (MAKE_BASE=TRUE)



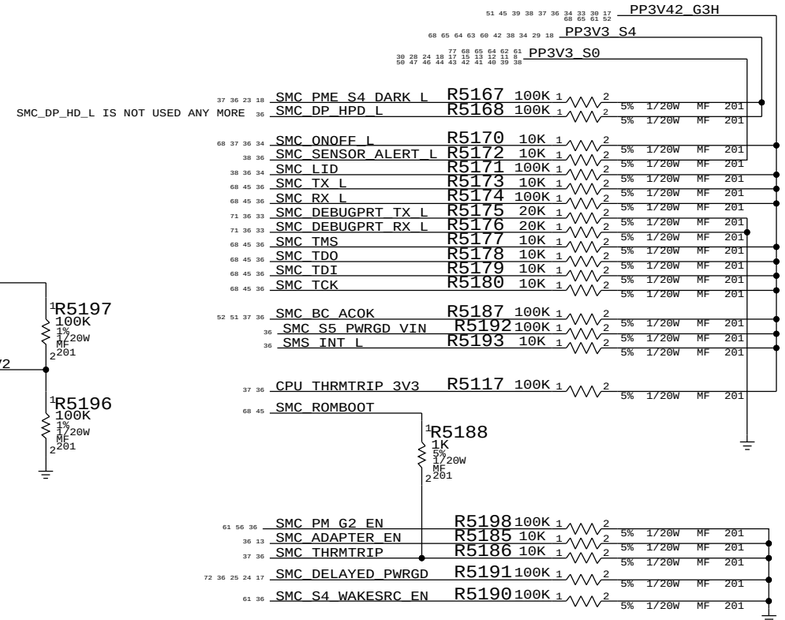








SMC_DP_HD_L IS NOT USED ANY MORE



SYNC MASTER=J44 SYNC DATE=08/12/2013

PAGE TITLE: SMC Shared Support

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D
REVISION: <E4LABEL>
BRANCH: <BRANCH>
PAGE: 51 OF 120
SHEET: 37 OF 78

SMC12 ADC Assignments

SMC_CPU_HI_ISENSE	SMC_CPU_HI_ISENSE	MAKE_BASE=TRUE
SMC_PBUS_VSENSE	SMC_PBUS_VSENSE	MAKE_BASE=TRUE
SMC_BMON_ISENSE	SMC_BMON_ISENSE	MAKE_BASE=TRUE
SMC_DCIN_ISENSE	SMC_DCIN_ISENSE	MAKE_BASE=TRUE
SMC_DCIN_VSENSE	SMC_DCIN_VSENSE	MAKE_BASE=TRUE
SMC_BMON_DISCRETE_ISENSE	SMC_BMON_DISCRETE_ISENSE	MAKE_BASE=TRUE
SMC_CPU_ISENSE	SMC_CPU_ISENSE	MAKE_BASE=TRUE
SMC_OTHER5V_HI_ISENSE	SMC_OTHER5V_HI_ISENSE	MAKE_BASE=TRUE
SMC_OTHER3V3_HI_ISENSE	SMC_OTHER3V3_HI_ISENSE	MAKE_BASE=TRUE
SMC_DDR_ISENSE	SMC_DDR_ISENSE	MAKE_BASE=TRUE
SMC_LCDBKLT_ISENSE	SMC_LCDBKLT_ISENSE	MAKE_BASE=TRUE
SMC_ADC11_PD	SMC_ADC11_PD	MAKE_BASE=TRUE
SMC_ADC12_PD	SMC_ADC12_PD	MAKE_BASE=TRUE
SMC_SSD_ISENSE	SMC_SSD_ISENSE	MAKE_BASE=TRUE
SMC_PP3V3S0_ISENSE	SMC_PP3V3S0_ISENSE	MAKE_BASE=TRUE
SMC_CAMERA_ISENSE	SMC_CAMERA_ISENSE	MAKE_BASE=TRUE
SMC_ADC16_PD	SMC_ADC16_PD	MAKE_BASE=TRUE
SMC_PP5VS0_ISENSE	SMC_PP5VS0_ISENSE	MAKE_BASE=TRUE
SMC_CPUDDR_ISENSE	SMC_CPUDDR_ISENSE	MAKE_BASE=TRUE
SMC_PCH_ISENSE	SMC_PCH_ISENSE	MAKE_BASE=TRUE
SMC_CPU_VSENSE	SMC_CPU_VSENSE	MAKE_BASE=TRUE
SMC_LCDPANEL_ISENSE	SMC_LCDPANEL_ISENSE	MAKE_BASE=TRUE
SMC_CPU_IMON_ISENSE	SMC_CPU_IMON_ISENSE	MAKE_BASE=TRUE
SMC_TBT_ISENSE	SMC_TBT_ISENSE	MAKE_BASE=TRUE

SMC12 Pin Assignments

NC_SMBUS_SMC_4_ASF_SCL	NC_SMBUS_SMC_4_ASF_SCL	MAKE_BASE=TRUE, NO_TEST=TRUE
NC_SMBUS_SMC_4_ASF_SDA	NC_SMBUS_SMC_4_ASF_SDA	MAKE_BASE=TRUE, NO_TEST=TRUE
NC_BDV_BKL_PWM	NC_BDV_BKL_PWM	MAKE_BASE=TRUE, NO_TEST=TRUE
NC_SMC_SYS_LED	NC_SMC_SYS_LED	MAKE_BASE=TRUE, NO_TEST=TRUE
NC_SMC_GFX_THROTTLE_L	NC_SMC_GFX_THROTTLE_L	MAKE_BASE=TRUE, NO_TEST=TRUE
NC_SMC_GFX_OVERTEMP	NC_SMC_GFX_OVERTEMP	MAKE_BASE=TRUE, NO_TEST=TRUE
NC_SMC_FAN_1_CTL	NC_SMC_FAN_1_CTL	MAKE_BASE=TRUE, NO_TEST=TRUE
NC_SMC_FAN_1_TACH	NC_SMC_FAN_1_TACH	MAKE_BASE=TRUE, NO_TEST=TRUE
NC_SMC_5VSW_PWR_EN	NC_SMC_5VSW_PWR_EN	MAKE_BASE=TRUE, NO_TEST=TRUE
NC_SMC_FAN_5_CTL	NC_SMC_FAN_5_CTL	MAKE_BASE=TRUE, NO_TEST=TRUE
NC_SMC_BIL_BUTTON_L	NC_SMC_BIL_BUTTON_L	MAKE_BASE=TRUE, NO_TEST=TRUE
NC_MEM_EVENT_L	NC_MEM_EVENT_L	MAKE_BASE=TRUE, NO_TEST=TRUE
NC_SMC_T101_COM_1	NC_SMC_T101_COM_1	MAKE_BASE=TRUE, NO_TEST=TRUE
NC_SMC_ACTUATOR_DISABLE_L	NC_SMC_ACTUATOR_DISABLE_L	MAKE_BASE=TRUE, NO_TEST=TRUE

Thermal Alerts

PCH_SML1ALERT_L — R5215 100 5% 1/20W MF 201 (NOSTUFF)

SMC_CPUHI_COMP_ALERT_L — R5217 100 5% 1/20W MF 201 (CPUHYS)

SMC_BMON_COMP_ALERT_L — R5213 100 5% 1/20W MF 201 (BMONHYS)

CPUTHMSNS_THM_L — R5216 100 5% 1/20W MF 201 — CPUTHRM_THRM:SMC

CPUTHMSNS_ALERT_L — R5214 100 5% 1/20W MF 201 — CPUTHRM_ALRT:SMC

TBTTHMSNS_THM_L — R5220 100 5% 1/20W MF 201 — TBTTHRM_THRM:SMC

TBTTHMSNS_ALERT_L — R5210 100 5% 1/20W MF 201 — TBTTHRM_ALRT:SMC

SMC_SENSOR_ALERT_L

PP3V42_G3H — R5232 10K 5% 1/20W MF 201 — SMC_BOARDID — SMCBOARDID:16

SMC_BOARDID — R5233 10K 5% 1/20W MF 201 — SMCBOARDID:8

Hall Effect Pads

APN: 998-4692
OMIT_TABLE
J5250
HALL-EFFECT-SENSOR-MLB-D1
SM

PP3V42_G3H — R5250 0 5% 1/10W MF-LF 402 — SMC_LID_R — SMC_LID

C5250 0.001UF 10% 50V X7R-CERM 0402

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
677-0912	1	SUBASSY,PCBA HALL EFFECT,J44	J5250	CRITICAL	

639-4502 (J44 HALL EFFECT BOARD) REPORTS TO 677-0912

Specify one of these BOM GROUPs.

BOM GROUP	BOM OPTIONS
CPUTHRM:BOTH	CPUTHRM_THRM:SMC,CPUTHRM_ALRT:SMC
CPUTHRM:THRM	CPUTHRM_THRM:SMC,CPUTHRM_ALRT:PU
CPUTHRM:ALRT	CPUTHRM_THRM:PU,CPUTHRM_ALRT:SMC
CPUTHRM:NONE	CPUTHRM_THRM:PU,CPUTHRM_ALRT:PU

Specify one of these BOM GROUPs.

BOM GROUP	BOM OPTIONS
TBTTHRM:BOTH	TBTTHRM_THRM:SMC,TBTTHRM_ALRT:SMC
TBTTHRM:THRM	TBTTHRM_THRM:SMC,TBTTHRM_ALRT:PU
TBTTHRM:ALRT	TBTTHRM_THRM:PU,TBTTHRM_ALRT:SMC
TBTTHRM:NONE	TBTTHRM_THRM:PU,TBTTHRM_ALRT:PU
TBTTHRM:GONE	

Requires EMC1412-1 or EMC1412-2 instead of EMC1412-A, new APN needs to be created.

S4 SMC Wake Sources

PP3V3_S4 — R5282 100K 5% 1/20W MF 201 — SMC_PME_S4_WAKE_L

SMC_PME_S4_WAKE_L — SMC_PME_S4_WAKE_L

R5230 0 5% 1/20W MF 0201: SMC_PCH_SUSWARN_L — PCH_SUSWARN_L

R5231 0 5% 1/20W MF 0201: SMC_PCH_SUSACK_L — PCH_SUSACK_L

SMC_SENSOR_PWR_EN — SMC_SENSOR_PWR_EN

SMC_WIFI_PWR_EN — SMC_WIFI_PWR_EN

PP3V3_S4 — R5295 10K 5% 1/20W MF 201 (NOSTUFF) — SMC_WIFI_PWR_EN

PP3V3_S4 — R5294 10K 5% 1/20W MF 201 (NOSTUFF) — SMC_SENSOR_PWR_EN

Top Block Swap

PP3V3_S0 — R5296 1K 5% 1/20W MF 201 — R5283 1K 5% 1/20W MF 201 — SMC_TOPBLK_SWP_L — PCH_STRP_TOPBLK_SWP_L

SMC_ADC16_PD — R5284 100K 5% 1/20W MF 201 (NOSTUFF)

SMC_ADC12_PD — R5285 100K 5% 1/20W MF 201 (NOSTUFF)

SMC_ADC11_PD — R5286 100K 5% 1/20W MF 201 (NOSTUFF)

GND_SMC_AVSS

SMC_RESET_L

NOSTUFF C5270 1000PF 10% 16V X7R-CERM 0201

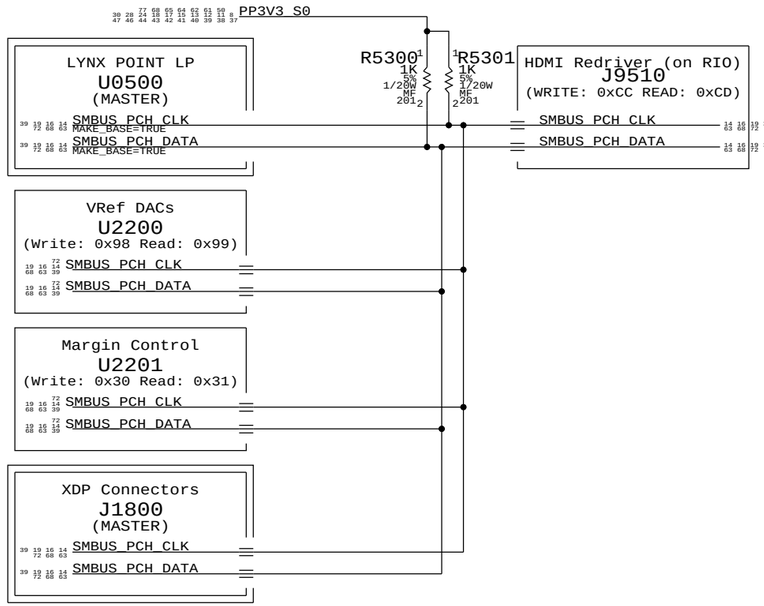
GND_SMC_AVSS

PAGE TITLE: SMC Project Support

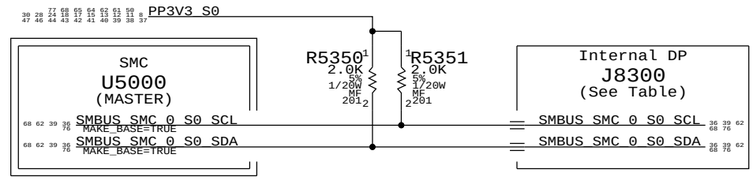
Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D
REVISION: <E4LABEL>
BRANCH: <BRANCH>
PAGE: 52 OF 120
SHEET: 38 OF 78

LYNX POINT LP S0 "SMBus 0" Connections



SMC SMBus "0" S0 Connections

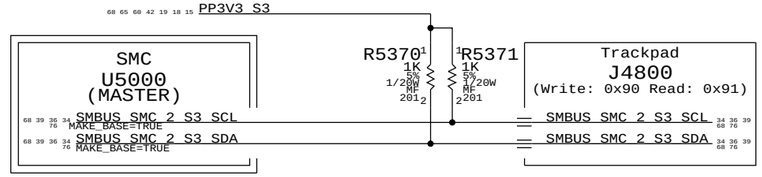


Internal DP

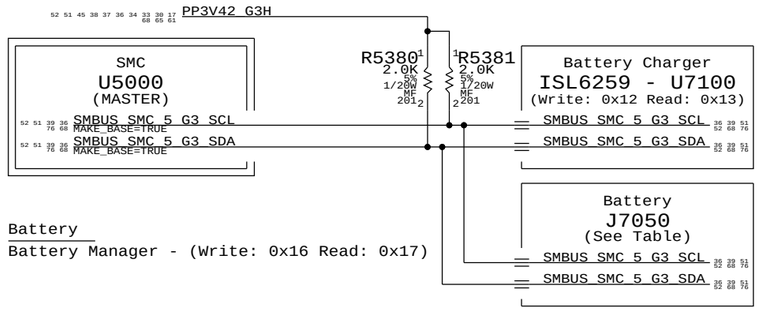
Parade T-con - (0x10-0x2F or 0x30-0x4F)

	J44
Samsung	Y
LGD	Y

SMC SMBus "2" S3 Connections



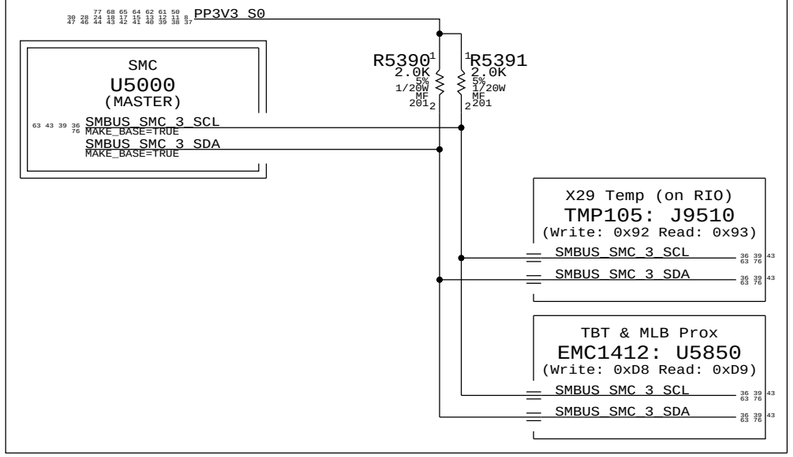
SMC SMBus "5" G3H Connections



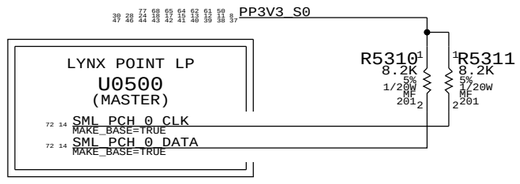
Battery

Battery Manager - (Write: 0x16 Read: 0x17)

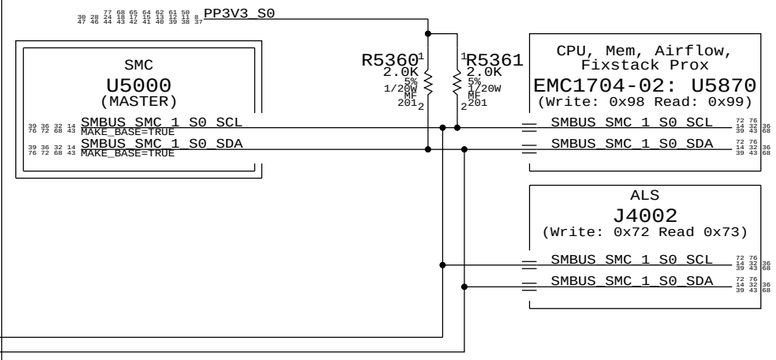
SMC SMBus "3" S0 Connections



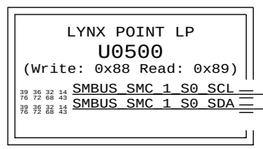
LYNX POINT LP S0 "SMLink 0" Connections



SMC SMBus "1" S0 Connections



LYNX POINT LP S0 "SMLink 1" Connections



SMLink 1 is slave port to access PCH.

SYNC_MASTER=J44 SYNC_DATE=08/12/2013

PAGE TITLE

SMBus Connections

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

REVISION <E4LABEL>

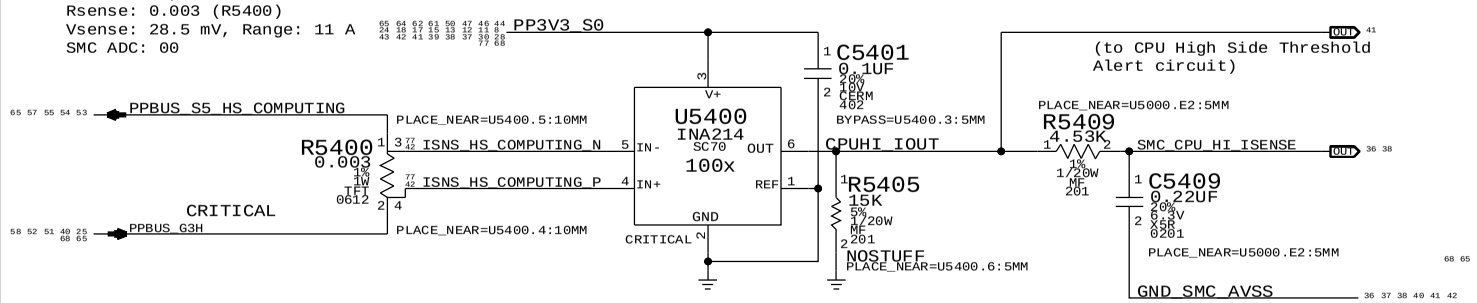
BRANCH <BRANCH>

PAGE 53 OF 120

SHEET 39 OF 78

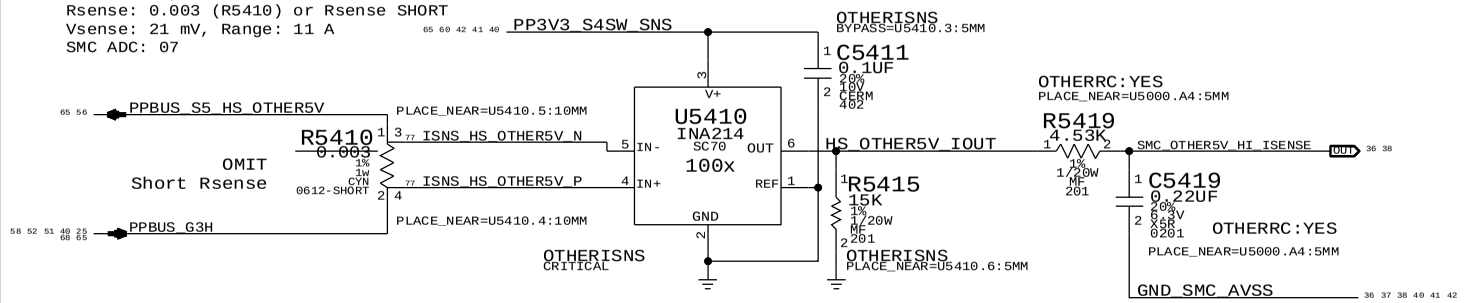
CPU High Side Current Sense (IC0R)

Gain: 100x, EDP: 9.5 A
Rsense: 0.003 (R5400)
Vsense: 28.5 mV, Range: 11 A
SMC ADC: 00



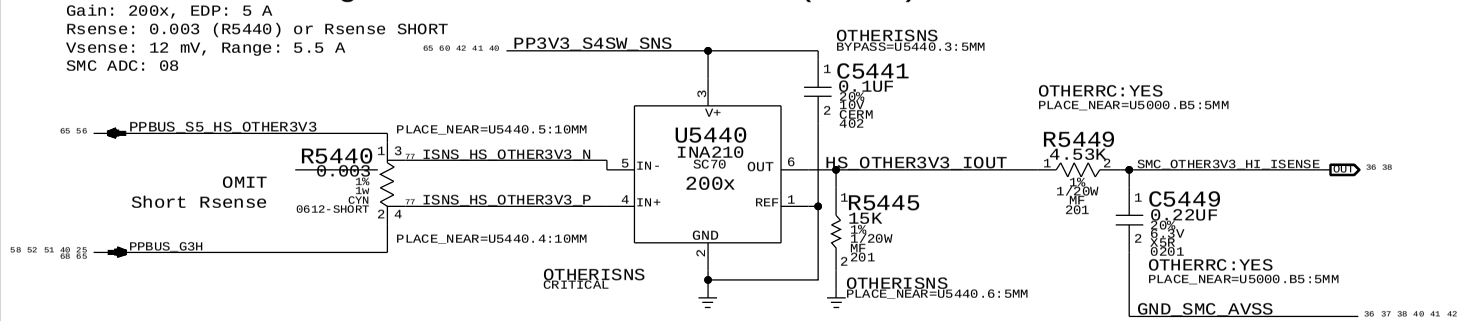
OTHER 5V High Side Current Sense (IO5R)

Gain: 100x, EDP: 7 A
Rsense: 0.003 (R5410) or Rsense SHORT
Vsense: 21 mV, Range: 11 A
SMC ADC: 07



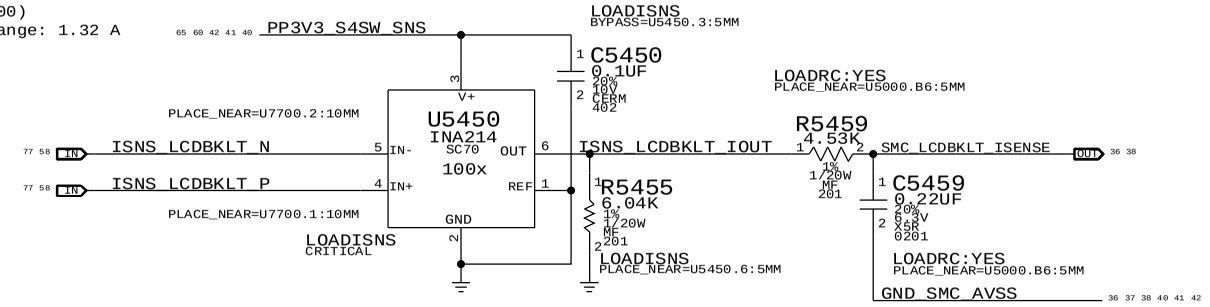
OTHER 3.3V High Side Current Sense (IO3R)

Gain: 200x, EDP: 5 A
Rsense: 0.003 (R5440) or Rsense SHORT
Vsense: 12 mV, Range: 5.5 A
SMC ADC: 08



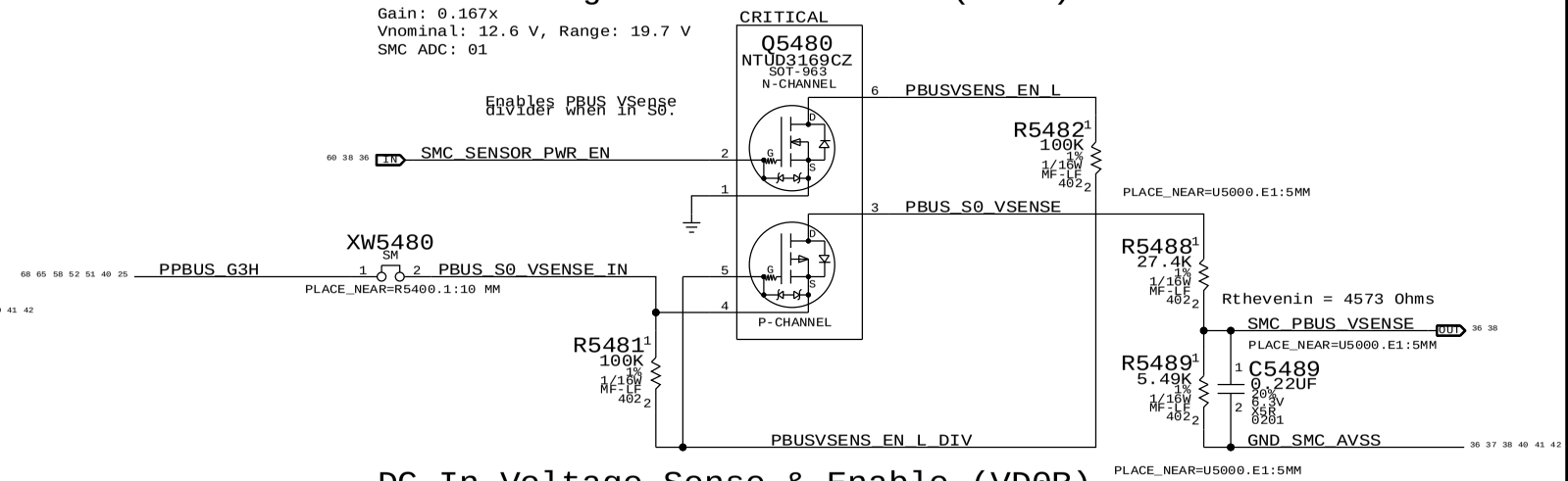
LCD Backlight Current Sense (IBLC)

Gain: 100x. EDP: 0.9 A
Rsense: 0.025 (R7700)
Vsense: 22.5 mV, Range: 1.32 A
SMC AD: 10



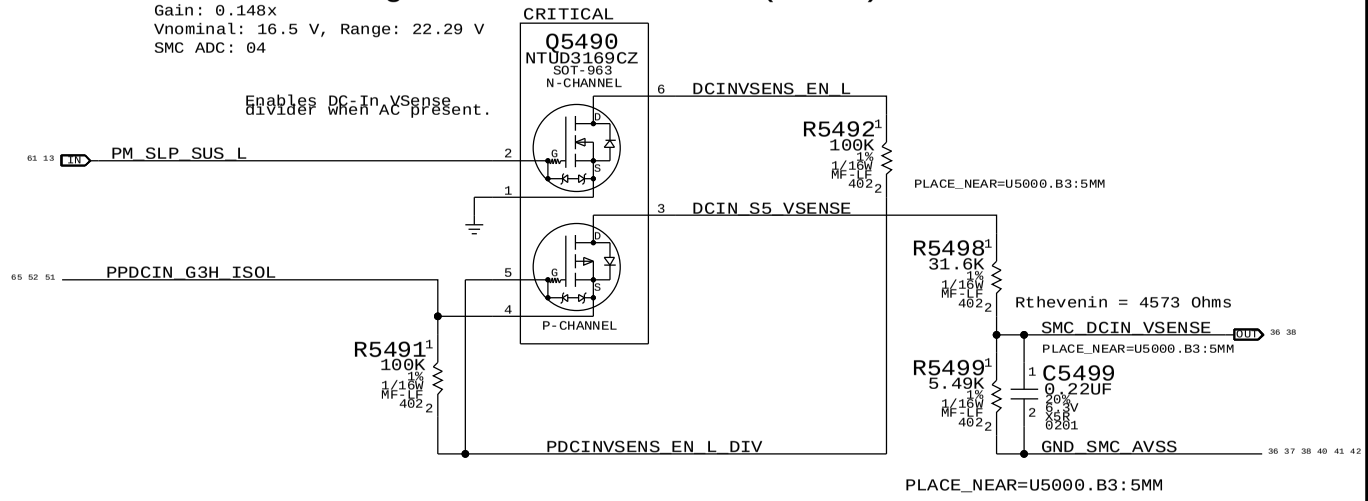
PBUS Voltage Sense & Enable (VP0R)

Gain: 0.167x
Vnominal: 12.6 V, Range: 19.7 V
SMC ADC: 01



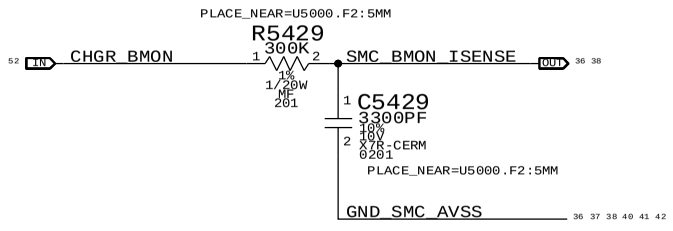
DC In Voltage Sense & Enable (VD0R)

Gain: 0.148x
Vnominal: 16.5 V, Range: 22.29 V
SMC ADC: 04



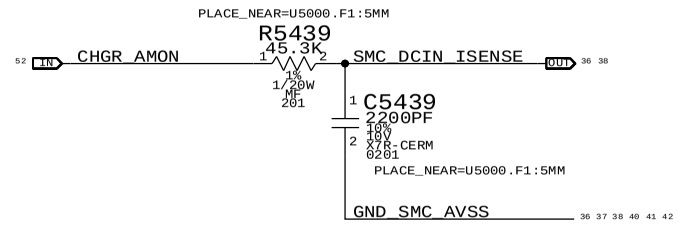
Charger (BMON) Current Sense (IPBR)

Charger Gain: 36x, EDP: 8 A
Rsense: 0.005 (R7150)
SMC ADC: 02



DC-IN (AMON) Current Sense (ID0R)

Charger Gain: 20x, EDP: 4.6 A
Rsense: 0.020 (R7120)
SMC ADC: 03



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
117S0008	1	RES,MTL FLIM,100K,1/16W,0201,SMD,LF	C5419,C5449		OTHERRC:NO
117S0008	1	RES,MTL FLIM,100K,1/16W,0201,SMD,LF	C5459		LOADRC:NO

SYNC_MASTER=J44 SYNC_DATE=08/12/2013

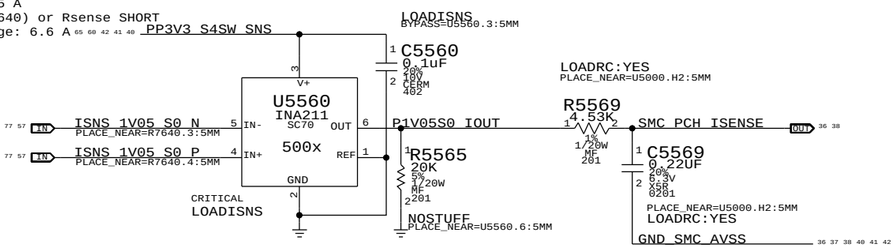
PAGE TITLE: Power Sensors: High Side

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D
REVISION: <E4LABEL>
BRANCH: <BRANCH>
PAGE: 54 OF 120
SHEET: 40 OF 78

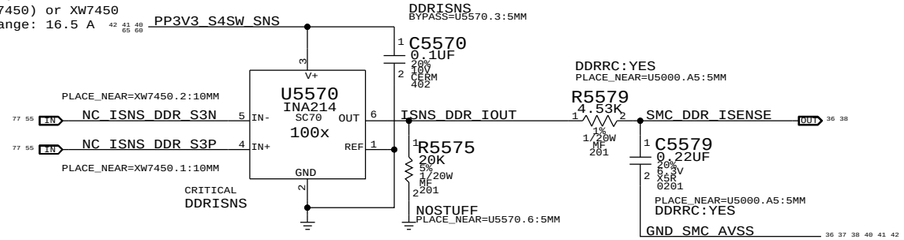
PCH 1.05V Current Sense (IC1C)

Gain: 500x, EDP: 5 A
Rsense: 0.001 (R7640) or Rsense SHORT
Vsense: 5 mV, Range: 6.6 A
SMC ADC: 19



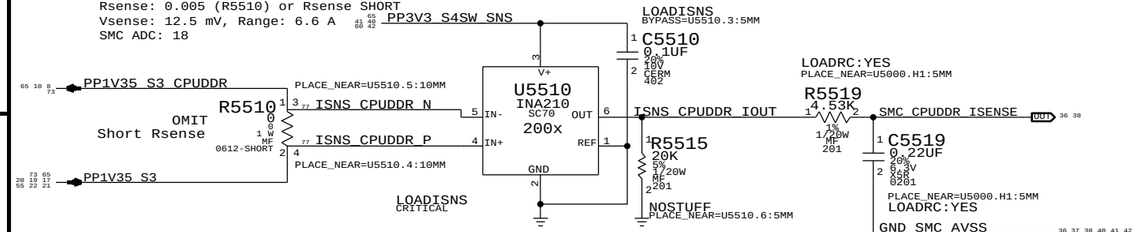
DDR 1.35V S3 (CPU & Memory) Current Sense (IM0C)

Gain: 100x, EDP: 9 A
Rsense: 0.002 (R7450) or XW7450
Vsense: 21 mV, Range: 16.5 A
SMC ADC: 09



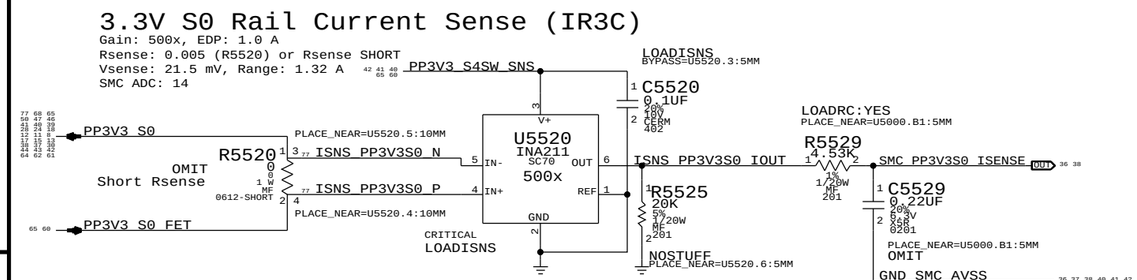
CPU DDR 1.35V S3 (CPU Only) Current Sense (IM1C)

Gain: 200x, EDP: 2.5 A
Rsense: 0.005 (R5510) or Rsense SHORT
Vsense: 12.5 mV, Range: 6.6 A
SMC ADC: 18



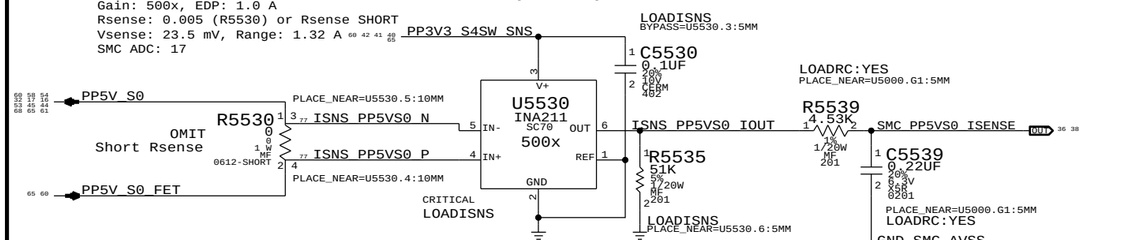
3.3V S0 Rail Current Sense (IR3C)

Gain: 500x, EDP: 1.0 A
Rsense: 0.005 (R5520) or Rsense SHORT
Vsense: 21.5 mV, Range: 1.32 A
SMC ADC: 14



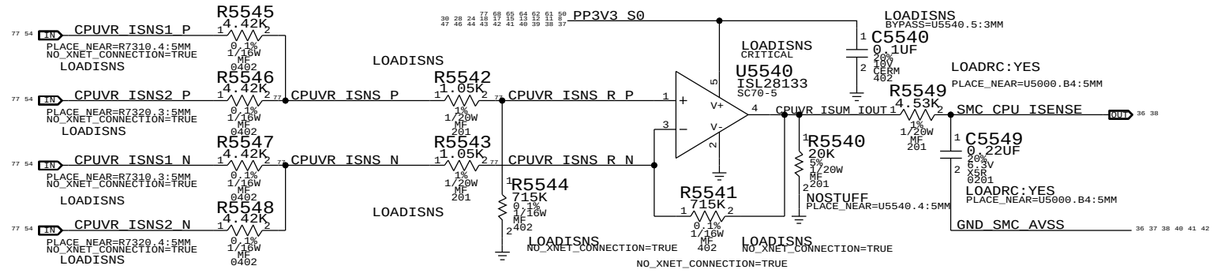
5V S0 Rail Current Sense (IR5C)

Gain: 500x, EDP: 1.0 A
Rsense: 0.005 (R5530) or Rsense SHORT
Vsense: 23.5 mV, Range: 1.32 A
SMC ADC: 17



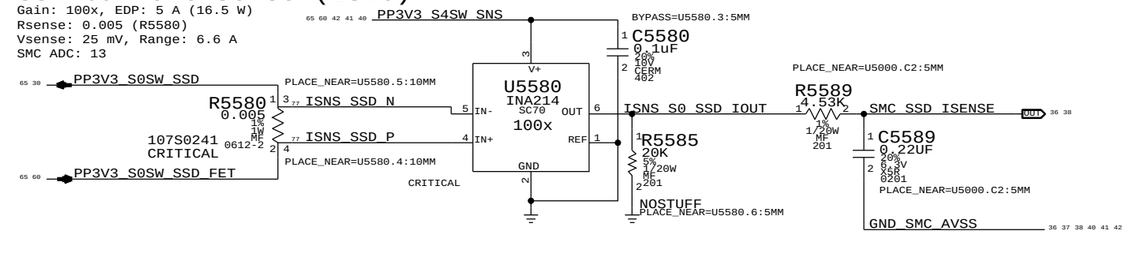
CPU Fixed Current Sense (IC0C)

Gain: 219.33x, EDP: 40 A
Rsense: 2x of 0.00075 (R7310, R7320), Rsum: 0.000375
Vsense: 15 mV, Range: 40.12 A
SMC ADC: 06



SSD Current Sense (ISDC)

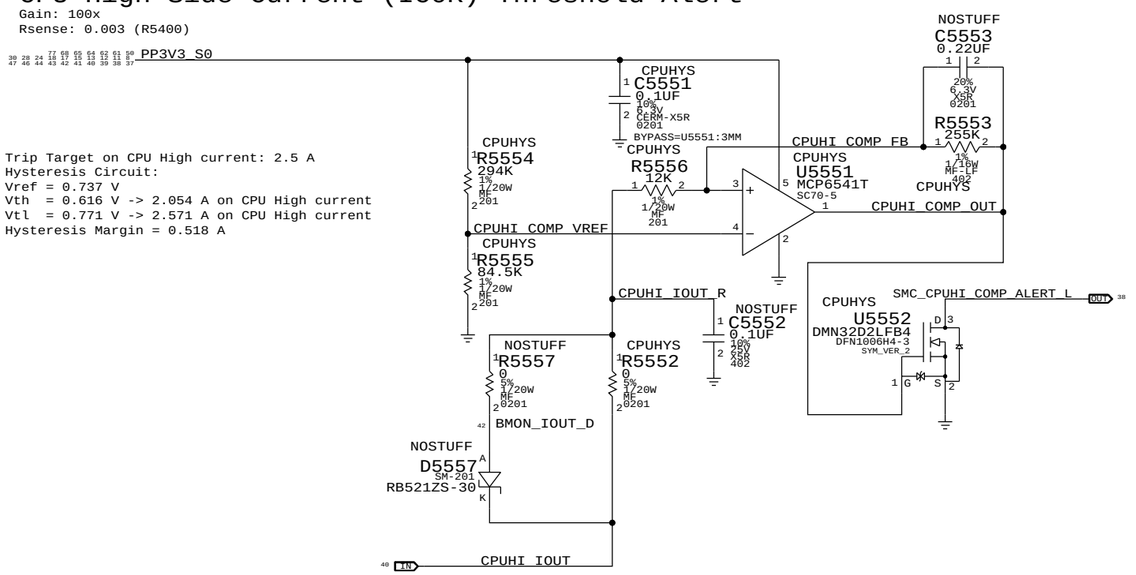
Gain: 100x, EDP: 5 A (16.5 W)
Rsense: 0.005 (R5580)
Vsense: 25 mV, Range: 6.6 A
SMC ADC: 13



CPU High Side Current (IC0R) Threshold Alert

Gain: 100x
Rsense: 0.003 (R5400)

Trip Target on CPU High current: 2.5 A
Hysteresis Circuit:
Vref = 0.737 V
Vth = 0.616 V -> 2.054 A on CPU High current
Vtl = 0.771 V -> 2.571 A on CPU High current
Hysteresis Margin = 0.518 A



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
117S0008	2	RES,MTL FLIM,100K,1/16W,0201,SMD,LF	C5569,C5519		LOADRC:NO
117S0008	3	RES,MTL FLIM,100K,1/16W,0201,SMD,LF	C5529,C5539,C5549		LOADRC:NO
117S0008	1	RES,MTL FLIM,100K,1/16W,0201,SMD,LF	C5579		DDRRC:NO

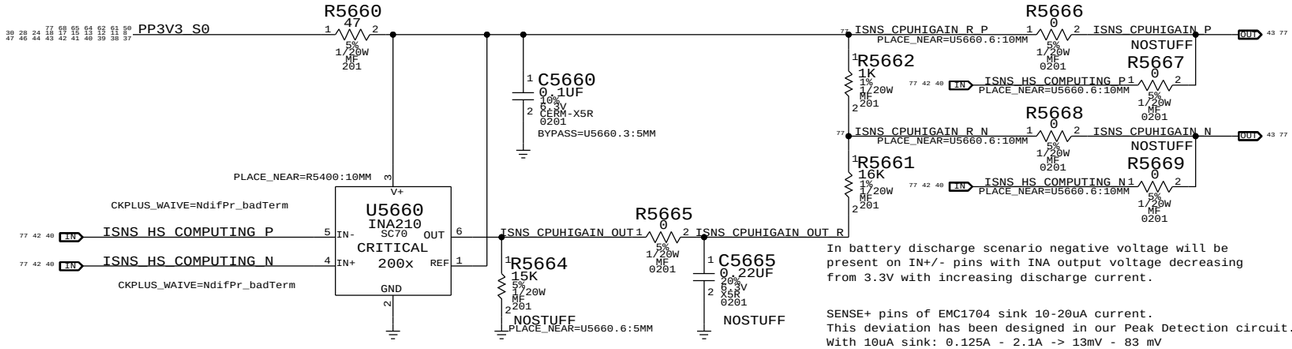
SYNC_MASTER=J44 SYNC_DATE=08/12/2013

PAGE TITLE
Power Sensors: Load Side

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D
REVISION <E4LABEL>
BRANCH <BRANCH>
PAGE 55 OF 120
SHEET 41 OF 78

CPU High Side (IC0R) Peak Detection Support

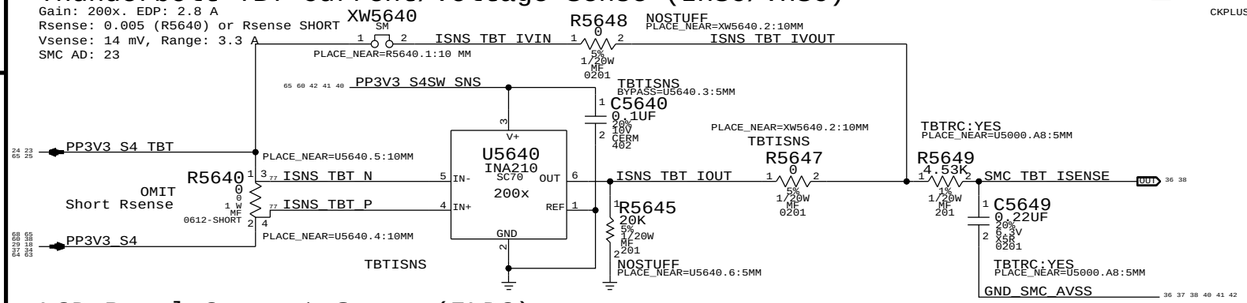


In battery discharge scenario negative voltage will be present on IN+/- pins with INA output voltage decreasing from 3.3V with increasing discharge current.

SENSE+ pins of EMC1704 sink 10-20uA current.
This deviation has been designed in our Peak Detection circuit.
With 10uA sink: 0.125A - 2.1A -> 13mV - 83 mV
With 20uA sink: 0.125A - 2.1A -> 23mV - 92 mV

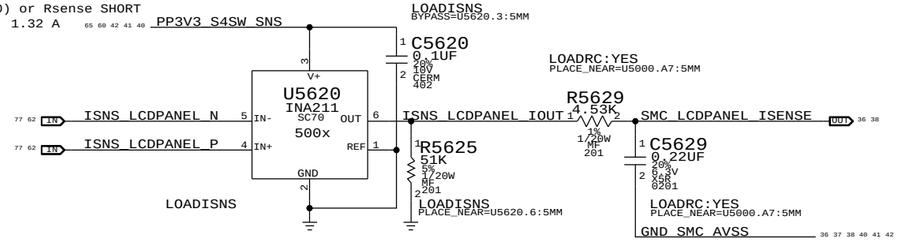
Thunderbolt TBT Current/Voltage Sense (IHSC/VHSC)

Gain: 200x. EDP: 2.8 A
Rsense: 0.005 (R5640) or Rsense SHORT
Vsense: 14 mV, Range: 3.3 A
SMC AD: 23



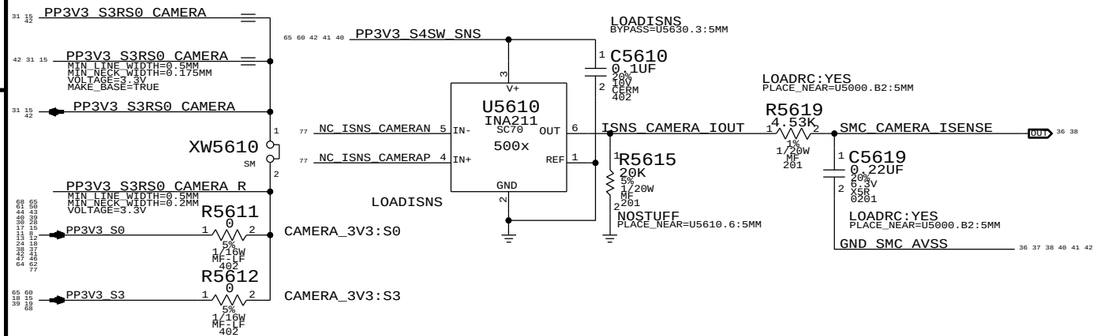
LCD Panel Current Sense (ILDC)

Gain: 500x. EDP: 1 A
RSENSE: 0.005 (R8320) or Rsense SHORT
Vsense: 5 mV, Range: 1.32 A
SMC AD: 21



Camera (S2 Controller) Current Sense (ICMC)

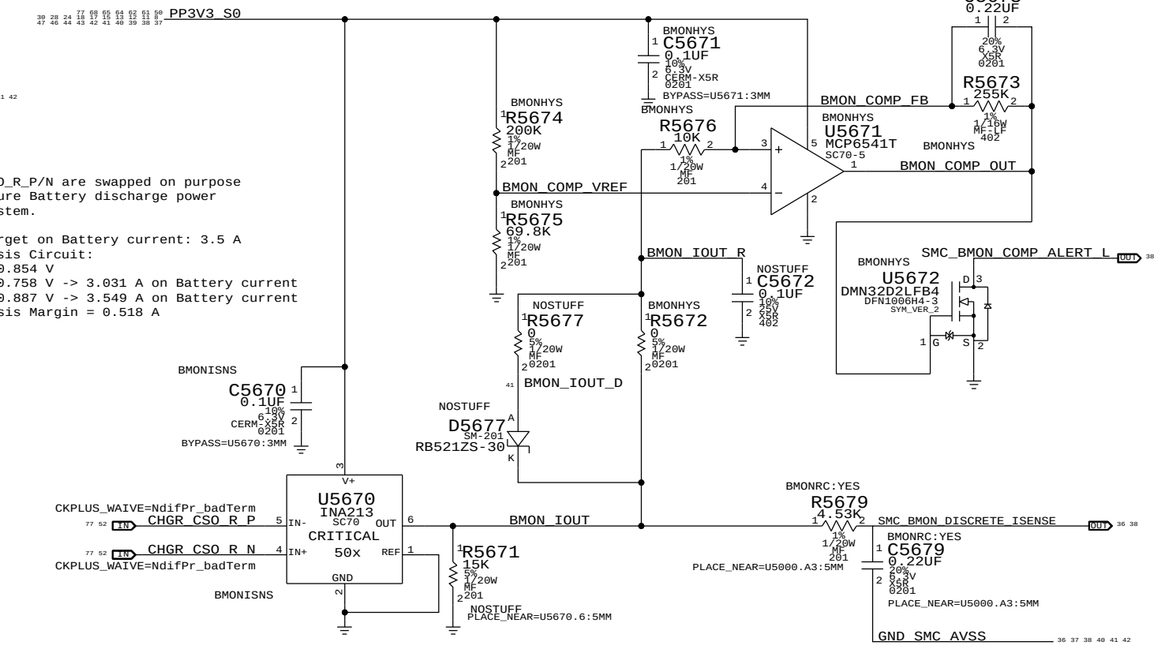
Gain: 500x. EDP: 0.82 A
Rsense: 0.005 (R5610) or XW5610
Vsense: 4.1 mV, Range: 1.32 A
SMC AD: 15



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
117S0008	4	RES,MTL FILM,100K,1/16W,0201,SMD,LF	C5619,C5629,C5649		
117S0008	1	RES,MTL FILM,100K,1/16W,0201,SMD,LF	C5679		

Battery BMON Discrete Current Sense (IP0R) & Threshold Alert

Gain: 50x. EDP: 8 A
Rsense: 0.005 (R7150)
Vsense: 50 mV, Range: 13.2 A
SMC AD: 05

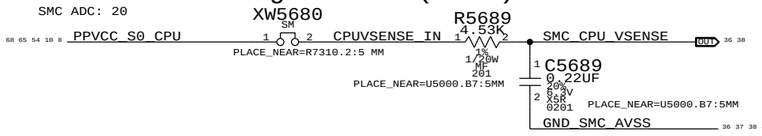


CHGR_CSO_R_P/N are swapped on purpose to measure Battery discharge power into system.

Trip Target on Battery current: 3.5 A
Hysteresis Circuit:
Vref = 0.854 V
Vth = 0.758 V -> 3.031 A on Battery current
Vtl = 0.887 V -> 3.549 A on Battery current
Hysteresis Margin = 0.518 A

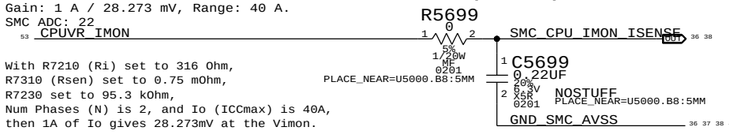
CPU Core Voltage Sense (VC0C)

SMC ADC: 20



CPU Core IMON Current Sense (IC2C)

Gain: 1 A / 28.273 mV, Range: 40 A.
SMC ADC: 22



With R7210 (Ri) set to 316 Ohm,
R7310 (Rsen) set to 0.75 mOhm,
R7230 set to 95.3 kOhm,
Num Phases (N) is 2, and Io (ICCmax) is 40A,
then 1A of Io gives 28.273mV at the Vimon.

SYNC_MASTER=J44 SYNC_DATE=08/12/2013

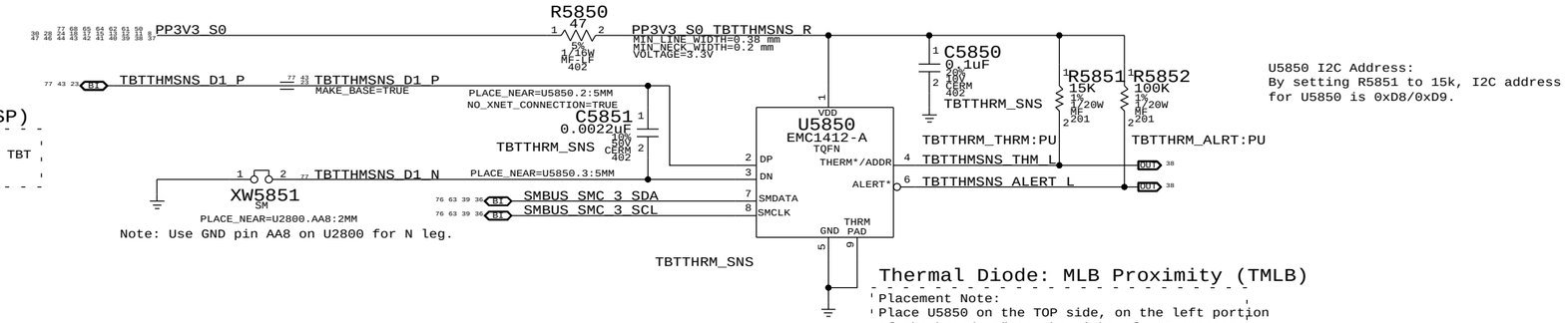
PAGE TITLE: Power Sensors: Extended

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D
REVISION: <E4LABEL>
BRANCH: <BRANCH>
PAGE: 56 OF 120
SHEET: 42 OF 78

Thermal Sensor A:
Thunderbolt Die, MLB Proximity

I2C Write: 0xD8, I2C Read: 0xD9



Note: Use GND pin AA8 on U2800 for N leg.

U5850 I2C Address:
By setting R5851 to 15k, I2C address for U5850 is 0xD8/0xD9.

Thermal Diode: TBT Die (THSP)

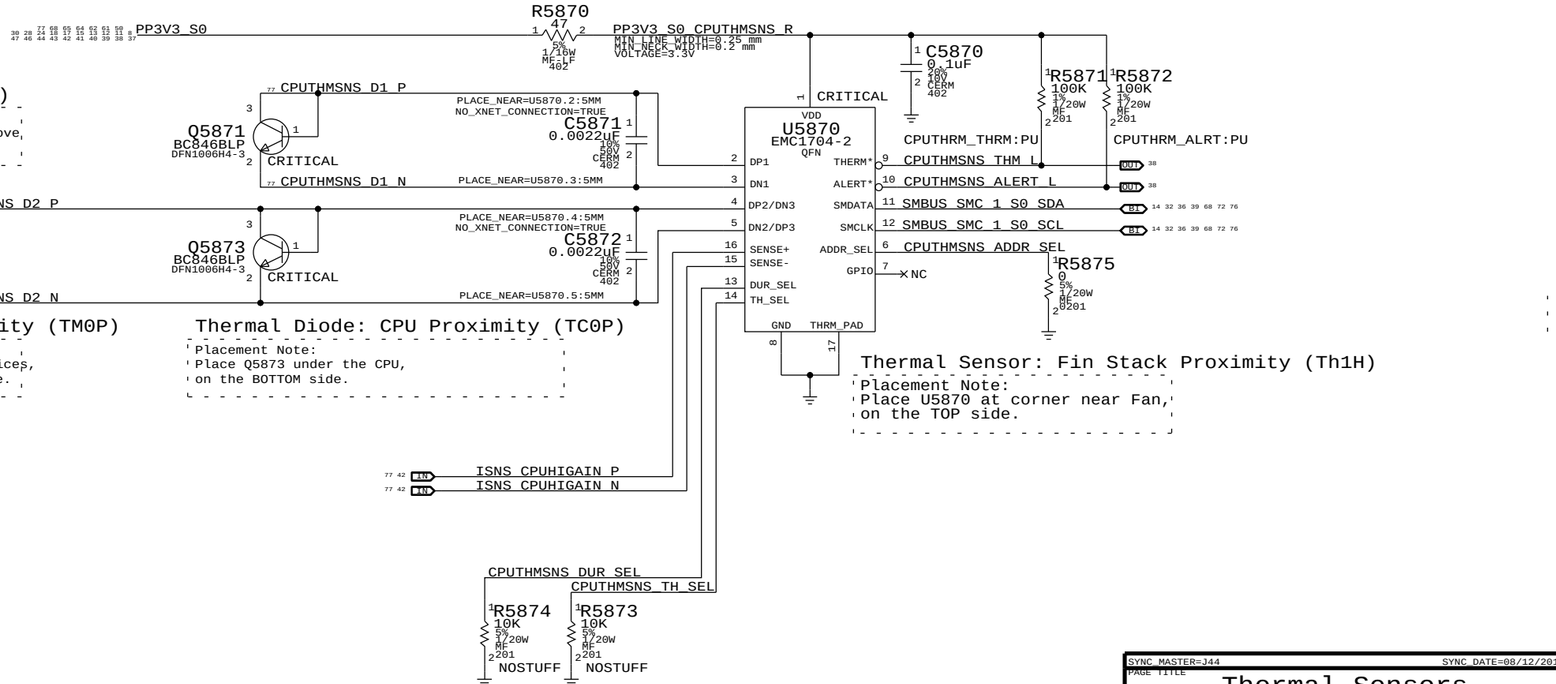
Placement Note:
The P leg connects to THERMDA pin of the TBT chip, the N leg connect to pin AA8.

Thermal Diode: MLB Proximity (TMLB)

Placement Note:
Place U5850 on the TOP side, on the left portion of the board, 1" to the right of USB connector.

Thermal Sensor B & CPU High Peak Detection:
CPU Proximity, Memory Proximity, Airflow, Fin Stack Proximity

I2C Write: 0x98, I2C Read: 0x99



Thermal Diode: Airflow (TA0P)

Placement Note:
Place Q5871, Airflow thermal indicator, above the SSD, on the BOTTOM side.

Thermal Diode: Memory Proximity (TM0P)

Placement Note:
Place Q5872 between two rows of Memory devices, between channel A and B, on the BOTTOM side.

Thermal Diode: CPU Proximity (TC0P)

Placement Note:
Place Q5873 under the CPU, on the BOTTOM side.

Thermal Sensor: Fin Stack Proximity (Th1H)

Placement Note:
Place U5870 at corner near Fan, on the TOP side.

SYNC_MASTER=J44 SYNC_DATE=08/12/2013

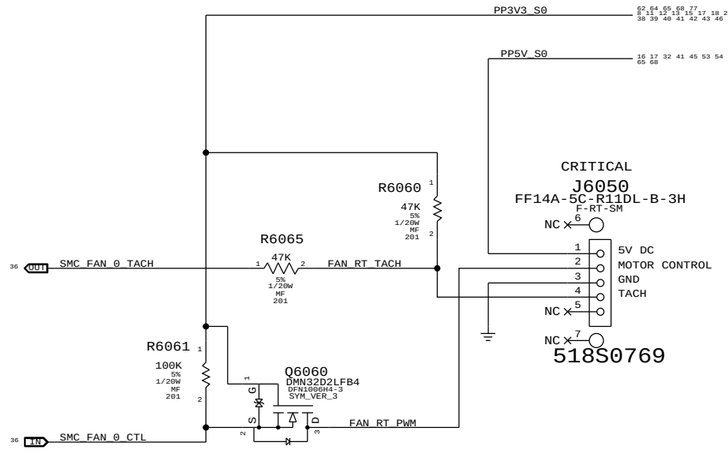
PAGE TITLE: Thermal Sensors

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D
REVISION: <E4LABEL>
BRANCH: <BRANCH>
PAGE: 58 OF 120
SHEET: 43 OF 78

FAN CONNECTOR

KEEP THE 5 PIN CONNECTOR FROM D1



SYNC_MASTER=J44 SYNC_DATE=08/12/2013

PAGE TITLE: Fan

Apple Inc.

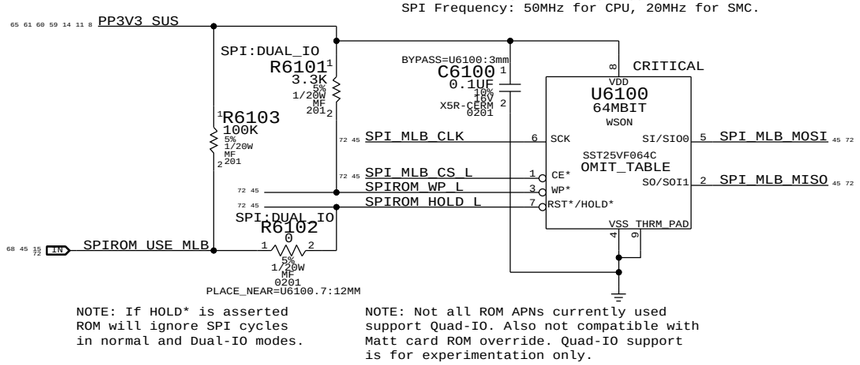
DRAWING NUMBER: <SCH_NUM> SIZE: D

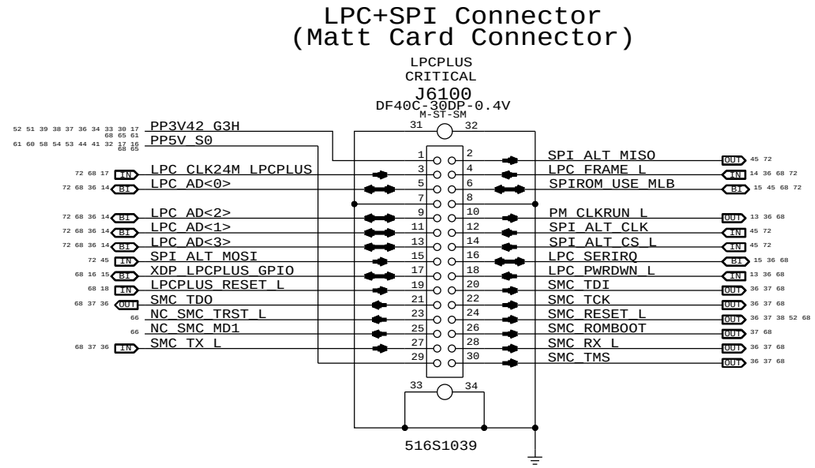
REVISION: <E4LABEL>

BRANCH: <BRANCH>

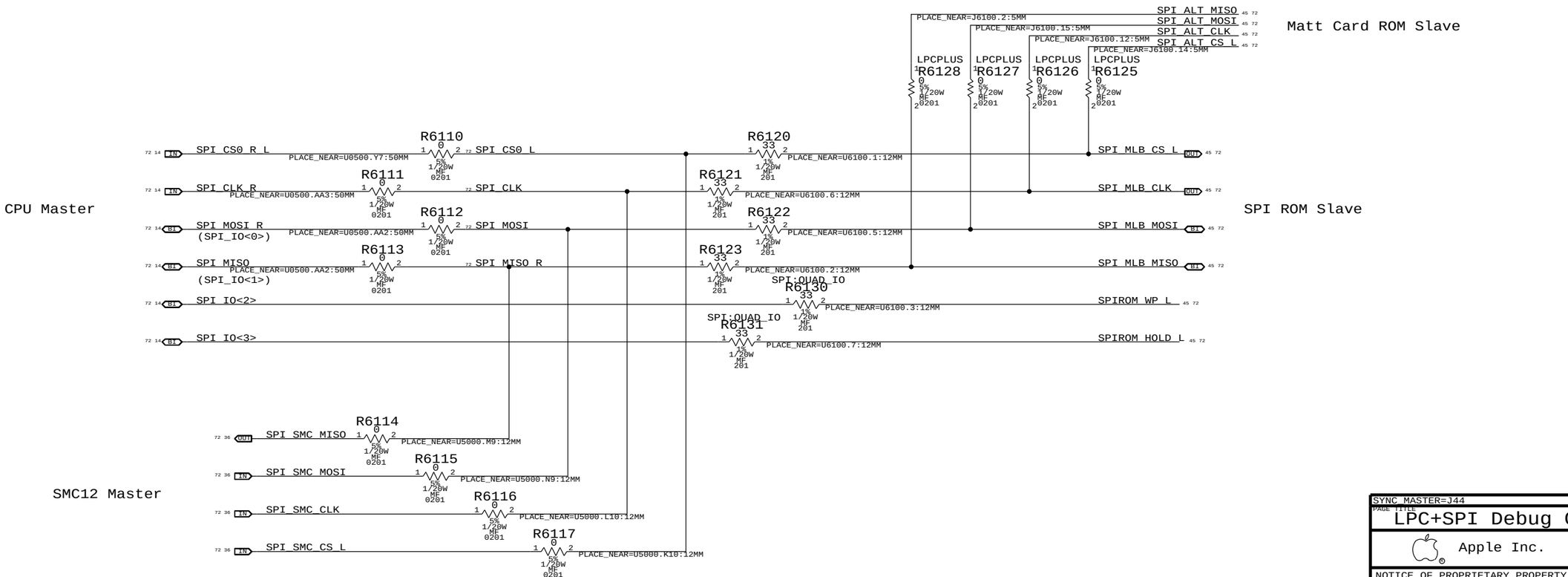
PAGE: 60 OF 120

SHEET: 44 OF 78





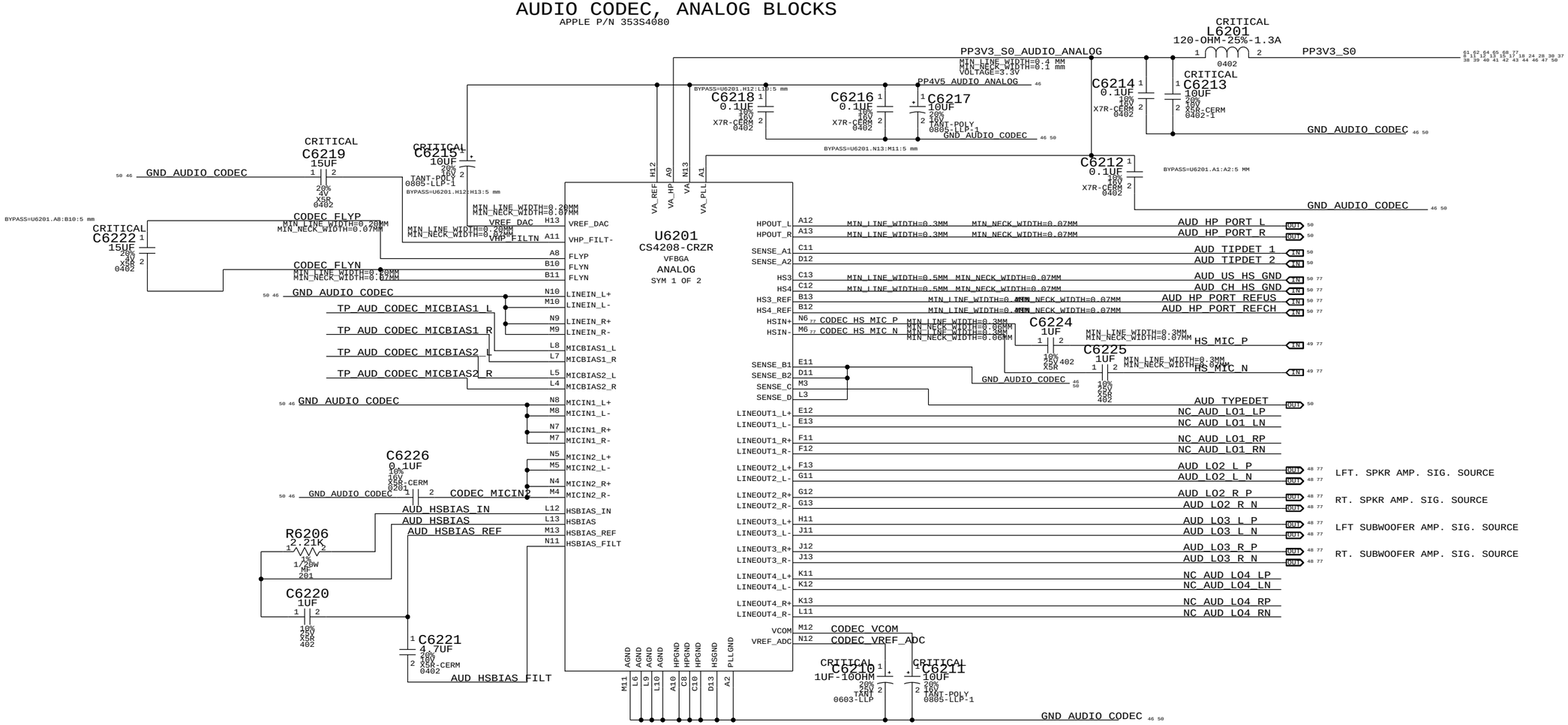
SPI Bus Series Termination



SYNC_MASTER=J44	SYNC_DATE=08/12/2013
PAGE TITLE	LPC+SPI Debug Connector
Apple Inc.	DRAWING NUMBER <SCH_NUM> SIZE D
	REVISION <E4LABEL>
	BRANCH <BRANCH>
	PAGE 61 OF 120
	SHEET 45 OF 78

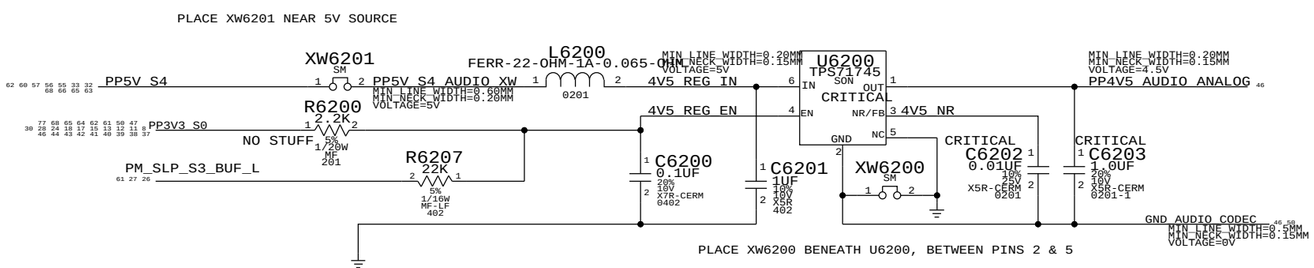
AUDIO CODEC, ANALOG BLOCKS

APPLE P/N 353S4080



4.5V POWER SUPPLY FOR CODEC

APPLE P/N 353S2456



SYNC_MASTER=J44 SYNC_DATE=08/12/2013

PAGE TITLE: AUDIO:CODEC, ANALOG

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

REVISION: <E4LABEL>

BRANCH: <BRANCH>

PAGE: 62 OF 120

SHEET: 46 OF 78

AUDIO CODEC, DIGITAL BLOCKS

APPLE P/N 353S4080

L6300
FERR-22-OHM-1A-0.065-OHM
PP1V5_S0
PP1V5_S0_AUDIO_DIG
MIN_LINE_WIDTH=0.5 MM
MIN_NECK_WIDTH=0.07MM
VOLTAGE=1.5V
C6300 4.7UF 20% 10V X5R-1 402
C6301 0.1UF 10% 16V X7R-CERM 0402
C6302 0.1UF 10% 16V X7R-CERM 0402
BYPASS=U6201.J2:J1:5 mm
BYPASS=U6201.E1:F1:5 mm
BYPASS=U6201.G1:F1:5 mm
BYPASS=U6201.K1:K3:5 mm
C6303 0.1UF 10% 6.3V X5R-CERM 0201
C6304 0.1UF 10% 6.3V X5R-CERM 0201
C6305 10UF 20% 6.3V X5R-CERM 0402-1
PP3V3_S0
C6306 10UF 20% 6.3V X5R-CERM 0402-1
C6307 0.1UF 10% 6.3V X5R-CERM 0201
BYPASS=U6201.A7:E3:5 mm
OMIT
R6302 SHORT 402
R6323 100K 5% 1/20W MF 201
R6324 100K 5% 1/20W MF 201
R6325 100K 5% 1/20W MF 201
NOSTUFF
R6322 100K 5% 1/20W MF 201
R6331 22 5% 1/20W MF 201
R6330 33 5% 1/10W MF-LF 402
R6332 75 1% 1/10W MF-LF 402
U6201
CS4208-CRZR
VFBGA
DIGITAL
SYM 2 OF 2

GPIO0_SPKR_SHUTDOWN
PD_CS4208_GPIO1
SPKRCONN_L_ID
SPKRCONN_R_ID
DFET_OPENUS
DFET_OPENCH
NC_CS4208_GPO0
NC_CS4208_GPO1
HDA_BIT_CLK
HDA_SYNC
HDA_SDIN0
HDA_SDOUT
HDA_RST_L
CS4208_HDA_SDOUT0_R
TP_CS4208_HDA_SDOUT1
NC_CS4208_MCLKA
NC_CS4208_SCLKA
NC_CS4208_LRCLKA
NC_CS4208_SDOUTA
NC_CS4208_MCLKB
NC_CS4208_SCLKB
NC_CS4208_LRCLKB
NC_CS4208_SDOUTB
CS4208_SPDIF_IN
CS4208_SPDIF_OUT
SPDIF_OUT_JACK
NC_DMIC_CLK0
NC_DMIC_CLK1
NC_DMIC_CLK2
DMIC_CLK3_R
DMIC_SDA3
DMIC_CLK3

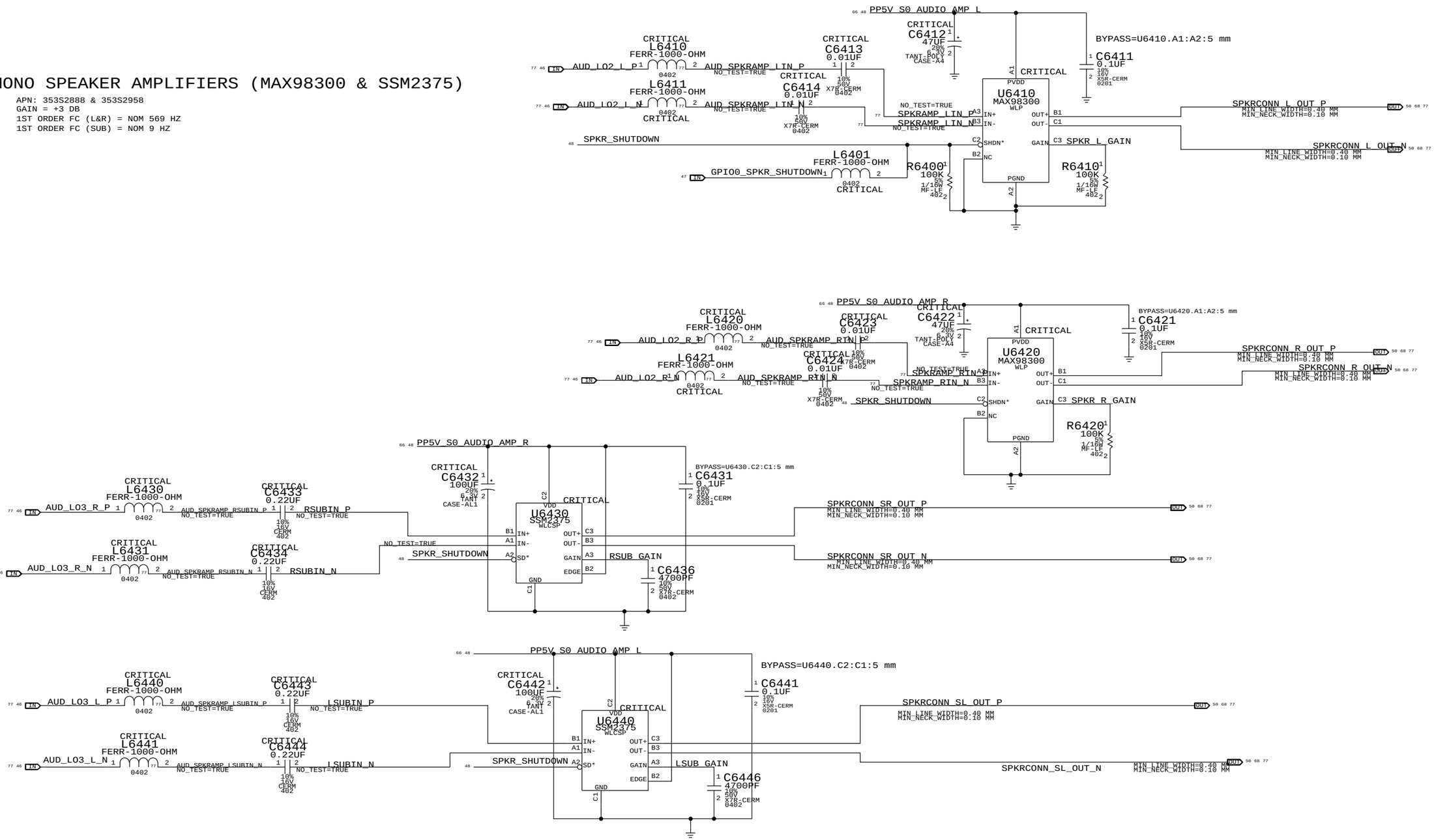
PP6301
P3MM SM
DMIC_SDA3
PLACE_NEAR=U6201.N3:5 mm

PP6304
P3MM SM
HDA_SDOUT
PLACE_NEAR=U6201.D2:5 mm

SYNC_MASTER=J44
SYNC_DATE=08/12/2013
PAGE TITLE: AUDIO:CODEC, DIGITAL
Apple Inc.
DRAWING NUMBER: <SCH_NUM>
SIZE: D
REVISION: <E4LABEL>
BRANCH: <BRANCH>
PAGE: 63 OF 120
SHEET: 47 OF 78

4X MONO SPEAKER AMPLIFIERS (MAX98300 & SSM2375)

APN: 353S2888 & 353S2958
GAIN = +3 DB
1ST ORDER FC (L&R) = NOM 569 HZ
1ST ORDER FC (SUB) = NOM 9 HZ

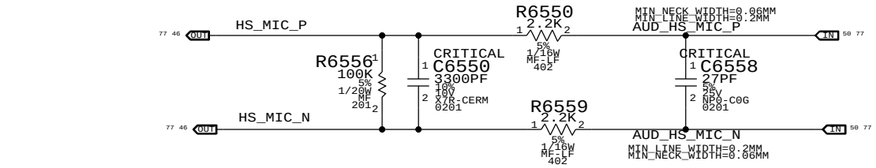


SYNC_MASTER=J44 SYNC_DATE=08/12/2013

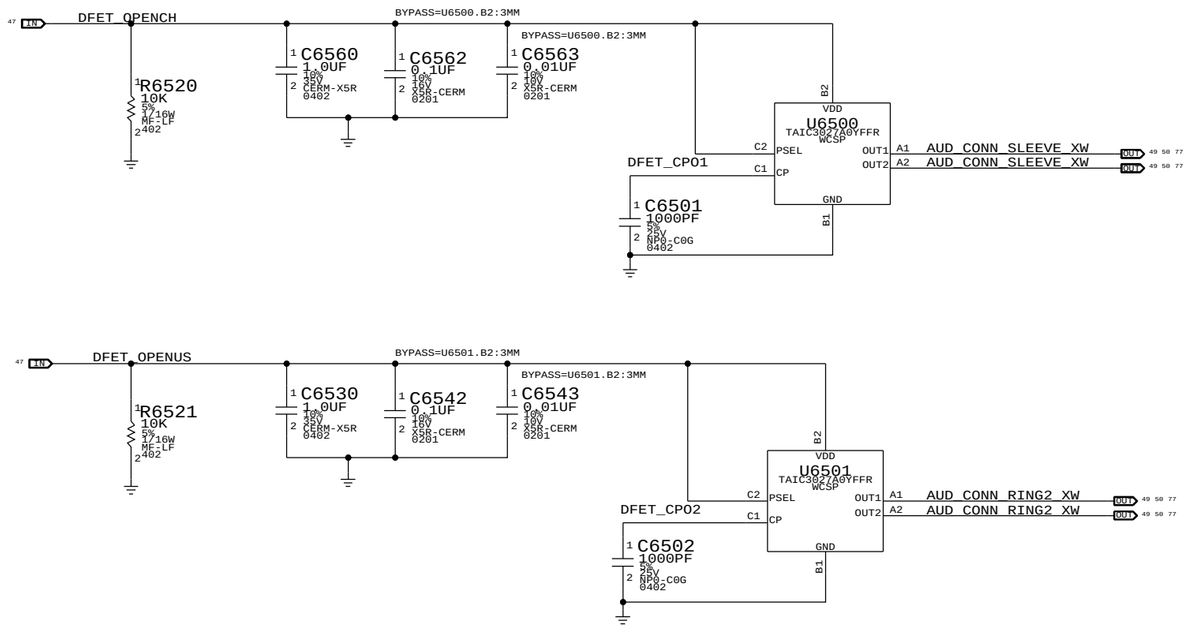
PAGE TITLE: AUDIO: SPEAKER AMP

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D
REVISION: <E4LABEL>
BRANCH: <BRANCH>
PAGE: 64 OF 120
SHEET: 48 OF 78



R/C6550 FILTER TO ADDRESS OUT-OF-BAND
NOISE ISSUE SEEN ON EARLY HEADSETS
(SEE RADAR # 6210118)



SYNC_MASTER=J44 SYNC_DATE=08/12/2013

PAGE TITLE

AUDIO: JACK

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

REVISION <E4LABEL>

BRANCH <BRANCH>

PAGE 65 OF 120

SHEET 49 OF 78

CODEC OUTPUT SIGNAL PATHS

FUNCTION	VOLUME	CONVERTER	PIN COMPLEX	MUTE CONTROL
HP/HS OUT	0X02 (2)	0X02 (2)	0X10 (16)	N/A
TWEETERS	0X03 (3)	0X03 (3)	0X12 (18)	CODEC GPIO0
SUB	0X04 (4)	0X04 (4)	0X13 (19)	CODEC GPIO0
SPDIF OUT	N/A	0X0E (14)	0X21 (33)	N/A

CODEC INPUT SIGNAL PATHS

FUNCTION	CONVERTER	PIN COMPLEX	VREF
DMIC 1	0X09 (9)	0X1C (28)	3.3V
DMIC 2	0X09 (9)	0X1C (28)	3.3V
HEADSET MIC	0X07 (7)	0X18 (24)	2.7V

OTHER CODEC GPIO LINES

LEFT SPEAKER ID	GPIO2 INPUT	HIGH = FG, LOW = MERRY
RIGHT SPEAKER ID	GPIO3 INPUT	HIGH = FG, LOW = MERRY
DFET CONTROL	GPIO4 OUTPUT	HIGH = DFETs OPEN

2-MIC CONNECTOR

APN: 518S0818

PP3V3_S0

CRITICAL J6601 FF14A-6C-R11DL-B-3H F-RT-SM

DMIC_SDA3 (OUT) → DMIC_SDA2 (68) via OMIT R6680 SHORT 402

DMIC_CLK3 (OUT)

SPEAKER CONNECTOR

HP=80HZ

APN: 518S0672

CRITICAL J6602 78171-6006 M-RT-SM

- SPKRCONN_L_OUT_P (IN)
- SPKRCONN_L_OUT_N (IN)
- SPKRCONN_L_ID (IN)
- SPKRCONN_SL_OUT_P (IN)
- SPKRCONN_SL_OUT_N (IN)

CRITICAL J6603 78171-6006 M-RT-SM

- SPKRCONN_R_OUT_P (IN)
- SPKRCONN_R_OUT_N (IN)
- SPKRCONN_R_ID (IN)
- SPKRCONN_SR_OUT_P (IN)
- SPKRCONN_SR_OUT_N (IN)

AUDIO JACK

CRITICAL L6611 120-OHM-25%-1.3A 0402: AUD_HP_PORT_REFCH (OUT) → AUD_CONN_SLEEVE (MIN_LINE_WIDTH=0.4MM, MIN_NECK_WIDTH=0.06MM) → XW6600 SM (PLACE_NEAR=J6600.5:5mm)

CRITICAL L6612 120-OHM-25%-1.3A 0402: AUD_CH_HS_GND (OUT) → AUD_CONN_SLEEVE_XW (MIN_LINE_WIDTH=0.5MM, MIN_NECK_WIDTH=0.1MM)

XW6601 SM: AUD_HS_MIC_P (OUT)

CRITICAL L6613 120-OHM-25%-1.3A 0402: AUD_HP_PORT_REFUS (OUT) → AUD_CONN_RING2 (MIN_LINE_WIDTH=0.4MM, MIN_NECK_WIDTH=0.06MM) → XW6602 SM (PLACE_NEAR=J6600.6:5mm)

CRITICAL L6614 120-OHM-25%-1.3A 0402: AUD_US_HS_GND (OUT) → AUD_CONN_RING2_XW (MIN_LINE_WIDTH=0.5MM, MIN_NECK_WIDTH=0.1MM)

XW6603 SM: AUD_HS_MIC_N (OUT)

CRITICAL L6604 120-OHM-25%-1.3A 0402: AUD_HP_PORT_L (IN) → AUD_CONN_HP_LEFT (MIN_LINE_WIDTH=0.3MM, MIN_NECK_WIDTH=0.06MM)

R6602 2.2K 5% 1/16W MF-LF 402 (2) — GND_AUDIO_CODEC — R6603 2.2K 5% 1/16W MF-LF 402 (2)

CRITICAL L6608 FERR-470-OHM 0201: AUD_TIPDET_2 (OUT) → AUD_CONN_TIPDET_2

CRITICAL L6607 FERR-470-OHM 0201: AUD_TIPDET_1 (OUT) → AUD_CONN_TIPDET_1

CRITICAL L6605 120-OHM-25%-1.3A 0402: AUD_HP_PORT_R (IN) → AUD_CONN_HP_RIGHT (MIN_LINE_WIDTH=0.3MM, MIN_NECK_WIDTH=0.06MM)

CRITICAL L6606 FERR-470-OHM 0201: AUD_TYPEDET (OUT) → AUD_CONN_TYPEDET

SPDIF_OUT_JACK (IN)

PP3V3_S0

R6601 10K 5% 1/16W MF-LF 402

C6602 100PF 5% 25V NP0-CERM 0201 — CRITICAL DZ6607 ESDALC5-1BM2 SOD882

C6603 100PF 5% 25V NP0-CERM 0201 — CRITICAL DZ6601 ESDALC5-1BM2 SOD882

C6604 100PF 5% 25V NP0-CERM 0201 — CRITICAL DZ6602 ESDALC5-1BM2 SOD882

C6605 100PF 5% 25V NP0-CERM 0201 — CRITICAL DZ6603 ESDALC5-1BM2 SOD882

C6606 100PF 5% 25V NP0-CERM 0201 — CRITICAL DZ6606 ESDALC5-1BM2 SOD882

C6607 100PF 5% 25V NP0-CERM 0201 — CRITICAL DZ6605 ESDALC5-1BM2 SOD882

C6608 100PF 5% 25V NP0-CERM 0201 — CRITICAL DZ6604 ESDALC5-1BM2 SOD882

APN: 514-0875

J6600 AUDIO-SPDIF-J44 F-RT-TH

5	MIC
6	AUDIO GND
2	2RTN
1	DET2
8	DET1
NC	
7	1RTN
3	R.AUDIO
4	AUDIO GND

AUDIO

9	VIN
10	VDD
11	GND

OPERATING VOLTAGE 3.3 POF

C6600 1UF 10% 10V X5R 402-1 — C6601 0.1UF 10% 6.3V CERM-X5R 0201

12	
13	
14	SHELL PINS
15	

SYNC_MASTER=J44 SYNC_DATE=08/12/2013

PAGE TITLE: AUDIO: JACK TRANSLATORS

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

REVISION: <E4LABEL>

BRANCH: <BRANCH>

PAGE: 66 OF 120

SHEET: 50 OF 78

MagSafe DC Power Jack

CRITICAL
F7005
6AMP-32V-0.0095OHM
0603

PPDCIN_G3H

CRITICAL
J7000
WTB-PWR-M82
M-RT-SM
518S0508

PP18V5_DCIN_FUSE
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.20MM
VOLTAGE=18.5V

NO STUFF
C7005
0.1UF
20%
100V
CERM
603-1

TP_TDM_ONEWIRE_MPM

ADAPTER_SENSE

1-Wire OverVoltage Protection
The chassis ground will otherwise float and can send transients onto ADAPTER_SENSE when AC is connected.

PP3V42_G3H

CRITICAL
U7001
TC7SZ08FEAPE
SOT665

C7008
0.1UF
20%
10V
CERM
402

SMC_BC_ACOK

SMC_BC_ACOK_VCC

C7000
0.1UF
20%
10V
CERM
402

U7000
MAX9940
SC70-5
CRITICAL
NC

R7029
2.0K
1%
1/10W
MF-LF
402

PPDCIN_G3H_ISOL

BLEEDER
CRITICAL
D7020
SBR0330CW
SOT-323

DCIN_ISOL_BLEEDER_PSRC
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.20MM

C7020
0.1UF
10%
50V
X7R
603-1

BLEEDER
R7030
1K
5%
1/10W
MF-LF
402

DCIN_ISOL_BLEEDER_R
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.20MM

BLEEDER
Q7030
2N7002
SOT23-HF1

DCIN_ISOL_BLEEDER_NGATE
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.20MM

BLEEDER
Q7020
AO3407A
SOT23

BLEEDER
R7021
10K
5%
1/16W
MF-LF
402

Q7010
SI5419DU
POWERPAK
5A

C7012
0.047UF
10%
25V
X5R
0402

R7011
10K
1%
1/20W
MF
201

DCIN_ISOL_GATE_R

R7012
68K
1%
1/20W
MF
201

Input impedance of 68K meets sparkitecture requirements for both MPM4 and MPM5.

R7010
100K
5%
1/20W
MF
201

When input voltage is 2V the FET will be off blocking the leakage path and 22.1K can be properly detected.

When input voltage is at 16V+, FET will conduct and power charger and 3.42V reg

DCIN_ISOL_GATE

D7010
GDZT2R6.8
GDZ-0201
6.8V Zener

3.425V "G3Hot" Supply

Supply needs to guarantee 3.31V delivered to SMC VRef generator

R7020
47
1%
1/8W
MF
805

PP18V5_DCIN_CONN_R
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=18.5V

CRITICAL
D7005
SBR0330CW
SOT-323

R7005
10
5%
1/8W
MF-LF
805

PPBUS_G3H
PPBUS_G3H_R
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=18.5V

PPVIN_G3H_P3V42G3H
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=18.5V

C7092
4.7UF
10%
25V
X6S-CERM
0603

C7091
4.7UF
10%
25V
X6S-CERM
0603

C7090
4.7UF
10%
25V
X6S-CERM
0603

U7090
LT3470AED
DFN

P3V42G3H_BOOST
DIDT=TRUE
NO_TEST=TRUE
SWITCH_NODE=TRUE

C7094
0.22UF
10%
16V
CERM
402

CRITICAL
L7095
10UH-20%-0.85A-0.460HM
2520

P3V42G3H_SW
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
SWITCH_NODE=TRUE
DIDT=TRUE

P3V42G3H_FB

R7080
0
5%
1/20W
MF
0201

P3V42G3H_SHDN_L

NO STUFF
R7081
49.9K
1%
1/20W
MF
201

NO STUFF
C7080
1000PF
5%
25V
CERM
0402

C7095
22PF
5%
50V
NP0-C0G-CERM
0201

R7095
348K
1%
1/20W
MF
201

R7096
200K
1%
1/20W
MF
201

CRITICAL
C7099
22UF
20%
6.3V
X5R
0603

Vout = 3.425V
300MA MAX OUTPUT
(Switcher limit)

Vout = 1.25V * (1 + Ra / Rb)

PP3V42_G3H

518-0394
CRITICAL
J7050
BAT-J44
F-ST-TH

PPVBAT_G3H_CONN

SMBUS_SMC_5_G3_SCL
SMBUS_SMC_5_G3_SDA
SYS_DETECT_L

CRITICAL
D7050
RCLAMP2402B
SC-75

C7050
0.1UF
10%
25V
X5R
402

C7060
1UF
10%
25V
X5R
603-1

R7050
10K
5%
1/16W
MF-LF
402

SYNC_MASTER=J44 SYNC_DATE=08/12/2017

PAGE TITLE
DC-In & Battery Connectors

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D
REVISION <E4LABEL>
BRANCH <BRANCH>
PAGE 70 OF 120
SHEET 51 OF 78

Reverse-Current Protection

Inrush Limiter

FROM ADAPTER

PPDCIN_G3H

C7185 0.1UF 10% 25V X5R 402

R7185 470K 1% 1/16W MF-LF 402

Q7180 IRF9395TRPBF DIRECTFET-MC

CRITICAL

C7180 4.7UF 10% 25V X6S-CERM 0603 NOSTUFF

PPDCIN_G3H_INRUSH
MIN_LINE_WIDTH=0.1 mm
MIN_LINE_WIDTH=0.1 mm
VOLTAGE=18.5V

R7180 100K 5% 1/16W MF-LF 402

CHGR_AGATE_DIV
MIN_LINE_WIDTH=0.3 mm
MIN_NECK_WIDTH=0.3 mm

CHGR_SGATE_DIV
MIN_LINE_WIDTH=0.3 mm
MIN_NECK_WIDTH=0.3 mm

R7186 332K 1% 1/16W MF-LF 402

R7181 62K 5% 1/16W MF-LF 402

PPDCIN_G3H_ISOL

CRITICAL
D7105 SBR0330CW SOT-323

(CHGR_AGATE)

(CHGR_SGATE)

R7105 20 5% 1/16W MF-LF 402

CHGR_DCIN_D_R

(CHGR_DCIN)

ACIN pin threshold is 3.2V, +/- 50mV

Divider sets ACIN threshold at 13.55V

Input impedance of ~90K meets sparkitecture requirements

30mA max load

PP5V1_CHGR_VDD
MIN_LINE_WIDTH=0.2 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=5.1V

PP3V42_G3H

R7101 4.7 5% 1/16W MF-LF 402

PP5V1_CHGR_VDDP
MIN_LINE_WIDTH=0.2 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=5.1V

C7101 1UF 10% 10V X5R 402

C7102 1UF 10% 10V X5R 402

NO STUFF
R7102 100K 5% 1/16W MF-LF 402

R7112 1K 1% 1/16W MF-LF 402

GND_CHGR_AGND

R7100 0 5% 1/16W MF-LF 402

SMC_RESET_L

CHGR_RST_L

SMBUS_SMC_5_G3_SCL

SMBUS_SMC_5_G3_SDA

CHGR_VFRQ

CHGR_CELL

Float CELL for 1S

R7110 68.1K 1% 1/16W MF-LF 402

CHGR_ACIN

R7111 21.5K 1% 1/16W MF-LF 402

CHGR_ICOMP

CHGR_VCOMP

CHGR_VNEG

CHGR_CSO_P

CHGR_CSO_N

R7115 100K 1% 1/16W MF-LF 402

C7150 1UF 10% 16V X5R 402

CHGR_VCOMP_R

C7115 330PF 5% 50V COG 402

R7142 1K 1% 1/16W MF-LF 402

R7116 3.01K 1% 1/16W MF-LF 402

CHGR_VNEG_R

C7116 470PF 10% 50V CERM 0402

CHGR_ICOMP_RC

C7142 0.068UF 10% 10V X5R-CERM 0402

U7100 ISL6259 TQFN

VHST	CRITICAL	DCIN	CHGR_DCIN
SMB_RST_N		SGATE	CHGR_SGATE
SCL		AGATE	CHGR_AGATE
SDA		CSIP	CHGR_CSI_P
VFRQ		CSIN	CHGR_CSI_N
CELL		BOOT	CHGR_BOOT
ACIN		UGATE	CHGR_UGATE
ICOMP		PHASE	
VCOMP		LGATE	CHGR_LGATE
VNEG		BGATE	CHGR_BGATE
CSOP		20V/V AMON	CHGR_AMON
CSON		36V/V BMON	CHGR_BMON
(AGND) THRM_PAD		(OD) ACOK	SMC_BC_ACOK
		(PGND)	

353S2929

C7111 0.01UF 10% 16V X7R-CERM 0402

C7100 1UF 10% 10V X5R 402-1

C7105 0.22UF 10% 50V X5R-CERM 0603-1

C7126 0.001UF 10% 50V X7R-CERM 0402

PLACE_NEAR=U7100.29:1MM

XW7100 SM

(GND)

PLACE_NEAR=U7100.22:1MM

GND_CHGR_AGND
MIN_LINE_WIDTH=0.2 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=0V

(CHGR_CSO_P)

(CHGR_CSO_N)

(PPVBAT_G3H_CHGR_R)

R7151 2.2 5% 1/16W MF-LF 402 CHGR_CSO_R_P

R7152 0 5% 1/16W MF-LF 402 CHGR_CSO_R_N

(PPVBAT_G3H_CHGR_R)

(CHGR_BGATE)

NO_XNET_CONNECTION=TRUE

C7120 0.047UF 10% 10V X5R-CERM 0402

R7121 10 5% 1/16W MF-LF 402

CHGR_CSI_R_P

R7122 10 5% 1/16W MF-LF 402

CHGR_CSI_R_N

C7122 0.1UF 10% 25V X5R 402

C7121 0.1UF 10% 25V X5R 402

NO_XNET_CONNECTION=TRUE

DIDT=TRUE
SWITCH_NODE=TRUE

CHGR_BOOT_R
MIN_LINE_WIDTH=0.2 mm
MIN_NECK_WIDTH=0.2 mm

R7125 0 5% 1/16W MF-LF 402

C7125 0.22UF 10% 10V CERM 402

PLACE_NEAR=U7100.23:1MM

CRITICAL
Q7130 RJK03P0DPA WPAK

MIN_LINE_WIDTH=0.2 mm
MIN_NECK_WIDTH=0.2 mm
SWITCH_NODE=TRUE
DIDT=TRUE

MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
GATE_NODE=TRUE
DIDT=TRUE

MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
SWITCH_NODE=TRUE
DIDT=TRUE

MIN_NECK_WIDTH=0.2 mm
MIN_LINE_WIDTH=0.6 mm
GATE_NODE=TRUE
DIDT=TRUE

CHGR_PHASE

CRITICAL
R7120 0.02 0.5% 1W MF RL1632W

PPDCIN_G3H_CHGR
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=18.5V

C7130 22UF 20% 25V POLY-TANT CASE-D2-SM

C7131 22UF 20% 25V POLY-TANT CASE-D2-SM

C7132 22UF 20% 25V POLY-TANT CASE-D2-SM

C7135 1.0UF 10% 50V X5R 0603

C7136 1.0UF 10% 50V X5R 0603

C7137 0.001UF 20% 50V CERM 0402

PLACE_NEAR=Q7130.2:1MM

PLACE_NEAR=C7136.1:3MM

Max Current = 8.5A
(L7130 limit)
f = 400 kHz

CRITICAL
L7130 4.7UH-20%-8.5A-18.3MOHM PIME103T-4R7MS

CRITICAL
F7140 12AMP-32V 1206

TO SYSTEM

PPBUS_G3H

PPVBAT_G3H_CHGR_REG
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=12.6V

CRITICAL
C7140 68UF 20% 16V POLY-TANT CASE-D2E-SM

C7145 0.001UF 10% 50V X7R-CERM 0402

CRITICAL
R7150 0.005 1% 1W MF 0612-2

PPVBAT_G3H_CHGR_R
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=12.6V

C7155 1UF 10% 25V X5R 402

C7156 0.1UF 10% 25V X5R 402

C7157 0.01UF 10% 50V X7R-CERM 0402

CRITICAL
Q7155 SI7137DP SO-8 SYM-VER-2

TO/FROM BATTERY

PPVBAT_G3H_CONN
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=12.6V

R7192 0 MF-LF 5% 402 1/16W

MIN_NECK_WIDTH=0.25 mm
MIN_LINE_WIDTH=0.5 mm

P5V1_VIN

For Erp Lot6 spec

P5V1_BOOST
DIDT=TRUE
NO_TEST=TRUE
SWITCH_NODE=TRUE

C7194 0.22UF 10% 10V CERM 402

C7190 4.7UF 10% 25V X6S-CERM 0603

U7190 LT3470A DFN

VIN BOOST SW BIAS FB GND SHDN* NC THRM PAD

CRITICAL

NC

P5V1_SW
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
SWITCH_NODE=TRUE
DIDT=TRUE

CRITICAL
L7195 33UH-20%-0.39A-0.435OHM DP418C-SM

MIN_NECK_WIDTH=0.25 mm
MIN_LINE_WIDTH=0.5 mm

P5V1_BIAS

C7195 22PF 5% 50V NP0-C0G-CERM 0201

<Ra>
R7195 681K 1% 1/20W MF 201

<Rb>
R7196 200K 1% 1/20W MF 201

P5V1_FB

Vout = 1.25V * (1 + Ra / Rb)

CRITICAL
C7198 10UF 20% 25V X5R-CERM 0603

CRITICAL
C7199 10UF 20% 25V X5R-CERM 0603

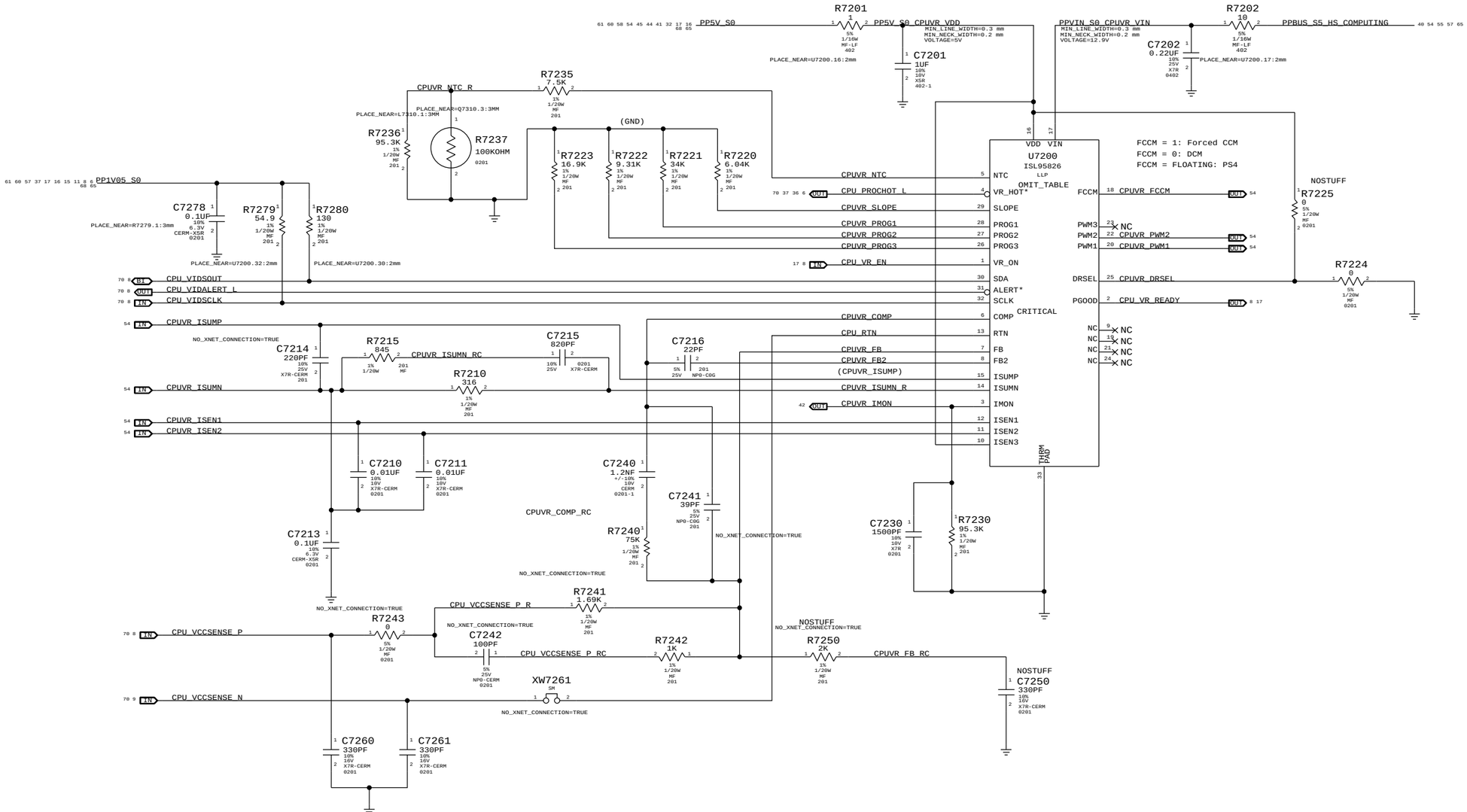
NOSTUFF
R7190 0 MF-LF 5% 402 1/16W
(P5V1_BIAS) CHGR_DCIN

R7191 0 MF-LF 5% 402 1/16W
PP5V1_CHGR_VDDP

Vout = 5.50V
250MA MAX OUTPUT
(Switcher limit)

SYNC MASTER=J44	SYNC DATE=08/12/2013
PAGE TITLE	PBus Supply & Battery Charger
Apple Inc.	DRAWING NUMBER <SCH_NUM> SIZE D
NOTICE OF PROPRIETARY PROPERTY: THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. THE POSESSOR AGREES TO THE FOLLOWING: I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE II NOT TO REPRODUCE OR COPY IT III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART IV ALL RIGHTS RESERVED	REVISION <E4LABEL>
	BRANCH <BRANCH>
	PAGE 71 OF 120
	SHEET 52 OF 78

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
353S4170	1	IC,ISL95826R6200,PWM,PGOOD,SCREN,32P,QFN	U7200	CRITICAL	



SYNC_MASTER=J44 SYNC_DATE=08/12/2013

PAGE TITLE

CPU VR12.6 VCC Regulator IC

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

REVISION <E4LABEL>

BRANCH <BRANCH>

PAGE 72 OF 120

SHEET 53 OF 78

PPBUS_S5_HS_COMPUTING

PP5V_S0

PHASE 1

U7310
ISL6208D
DFN
CRITICAL

CPUVR_PWM1
CPUVR_FCCM
CPUVR_UGATE1
CPUVR_LGATE1
CPUVR_BOOT1
CPUVR_BOOT1_RC

Q7310 SISA18DN PWRPAK-SM
Q7311 SISA12DN PWRPAK-SM

C7310 1UF
R7311 2.2
C7311 0.22UF

PHASE 2

U7320
ISL6208D
DFN
CRITICAL

CPUVR_PWM2
CPUVR_FCCM
CPUVR_UGATE2
CPUVR_LGATE2
CPUVR_BOOT2
CPUVR_BOOT2_RC

Q7320 SISA18DN PWRPAK-SM
Q7321 SISA12DN PWRPAK-SM

C7320 1UF
R7321 2.2
C7321 0.22UF

353S3942

C7313 68UF
C7314 68UF
C7315 10UF
C7316 10UF
C7317 1.0UF
C7318 0.001UF
C7319 0.001UF
R7310 0.00075

L7310 0.4UH-20%-23A
PILE063T-SM 152S1821
CPUVR_PHASE1
PPVCC_S0_CPU_PH1
R7312 2.2
C7312 0.001UF
R7314 1.00
R7315 1K
R7316 200K
R7317 NOSTUFF
CPUVR_ISNS1_P
CPUVR_ISNS1_N
CPUVR_ISUMN
CPUVR_ISUMP
CPUVR_ISEN1
CPUVR_ISNS2_N

C7323 68UF
C7324 68UF
C7325 10UF
C7326 10UF
C7327 1.0UF
C7328 0.001UF
C7329 0.001UF
R7320 0.00075

L7320 0.4UH-20%-23A
PILE063T-SM 152S1821
CPUVR_PHASE2
PPVCC_S0_CPU_PH2
R7322 2.2
C7322 0.001UF
R7324 1.00
R7325 1K
R7326 200K
R7327 NOSTUFF
CPUVR_ISNS2_P
CPUVR_ISNS2_N
CPUVR_ISUMN
CPUVR_ISUMP
CPUVR_ISEN2
CPUVR_ISNS1_N

Additonal Input Bulk Caps

C7370 33UF
C7371 33UF
C7376 33UF
C7378 33UF
C7380 33UF
C7372 68UF
C7373 68UF
C7374 68UF
C7375 68UF

Note: C7377, C7379, C7381 were removed. Area where the pads used to reside was preserved.

PPVCC_S0_CPU

Vout = 1.85V max
40A MAX OUTPUT
F = 800KHZ

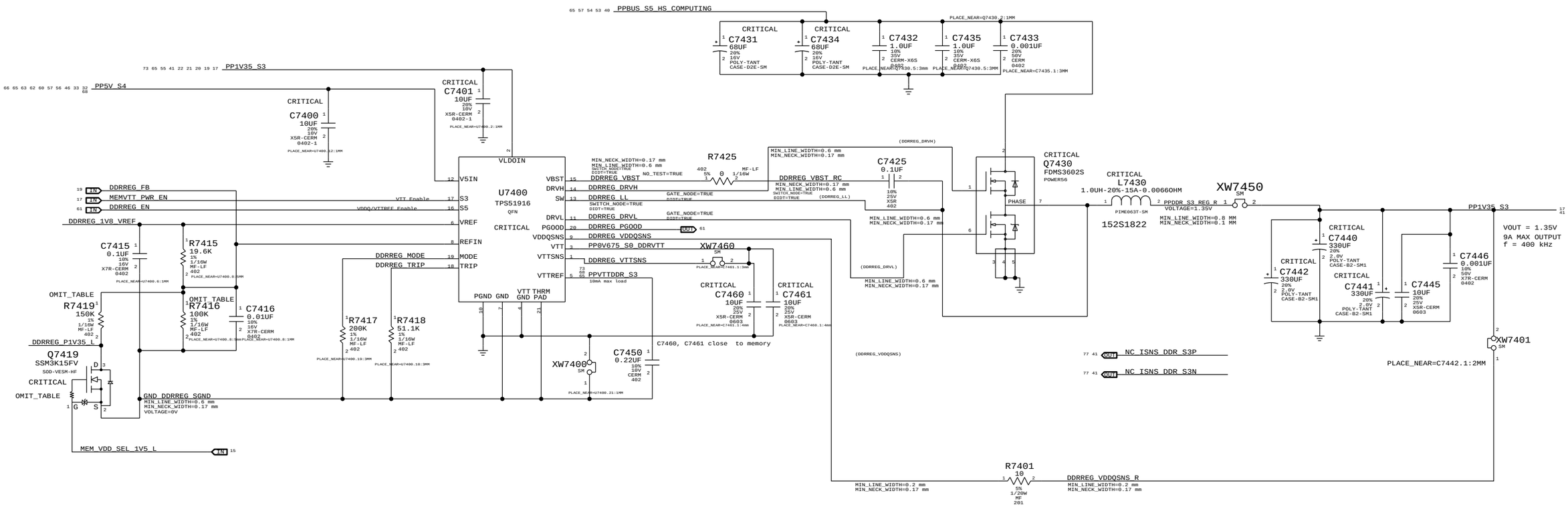
SYNC_MASTER=J44 SYNC_DATE=08/12/2013

PAGE TITLE
CPU VR12.5 VCC Power Stage

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D
REVISION <E4LABEL>
BRANCH <BRANCH>
PAGE 73 OF 120
SHEET 54 OF 78

DDR3L (1V35 S3) REGULATOR



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
114S0411	1	RES,MTL FILM,1/16W,100K,1,0402,SMD,LF	R7416	CRITICAL	PPDDR:1V5
114S0391	1	RES,MTL FILM,1/16W,60.4K,1,0402,SMD,LF	R7416	CRITICAL	PPDDR:1V35
376S0612	1	MOSFET,N-CH,30V,100MA,7.0OHM,SOT-723,HF	Q7419	CRITICAL	PPDDR:1V5
114S0428	1	RES, MTL FILM,1/16W,150k,0402,SMD,LF	R7419	CRITICAL	PPDDR:1V5

SYNC_MASTER=J44 SYNC_DATE=08/12/2013

PAGE TITLE

1.35V DDR3 SUPPLY

Apple Inc.

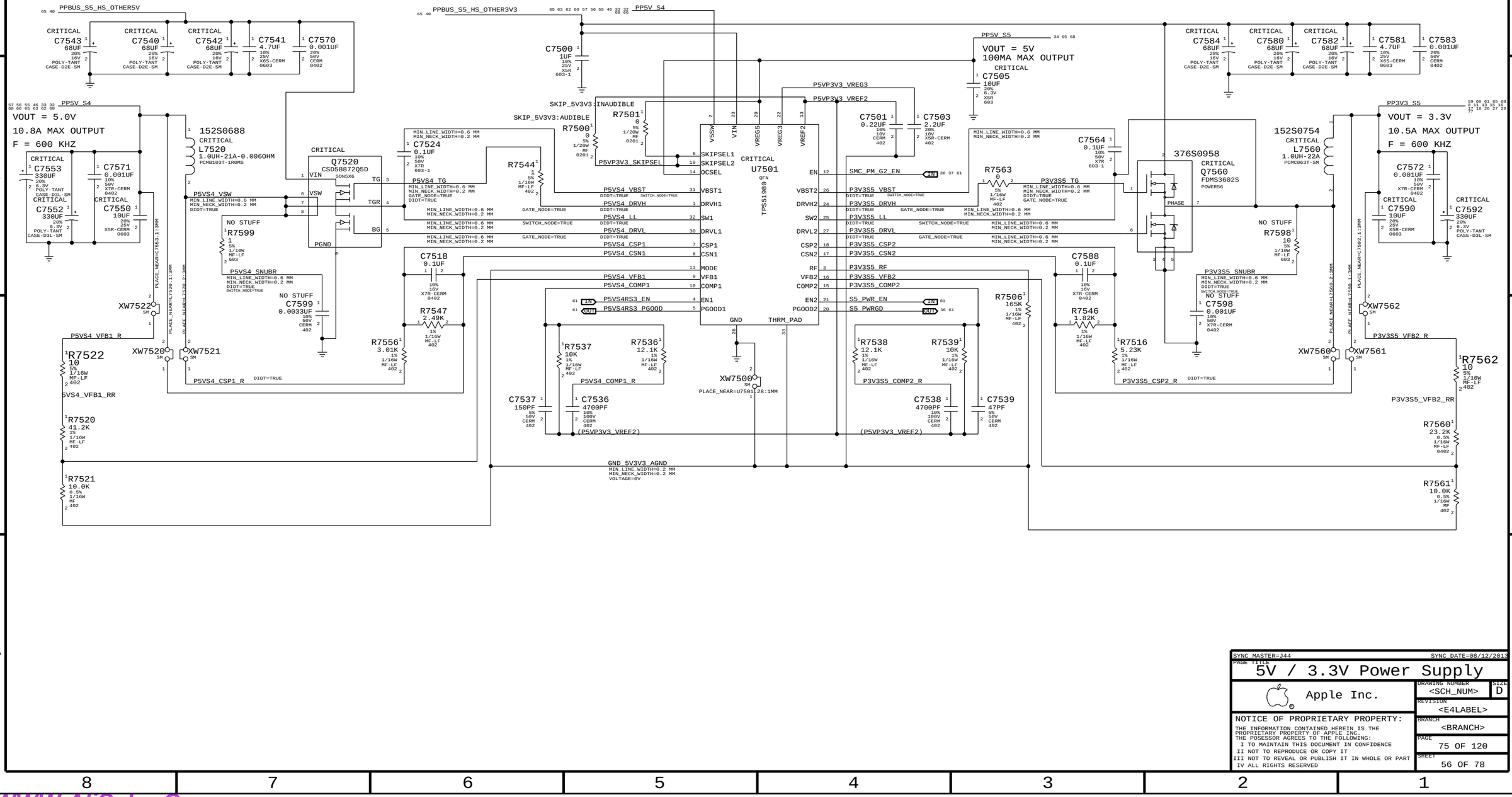
DRAWING NUMBER <SCH_NUM> SIZE D

REVISION <E4LABEL>

BRANCH <BRANCH>

PAGE 74 OF 120

SHEET 55 OF 78



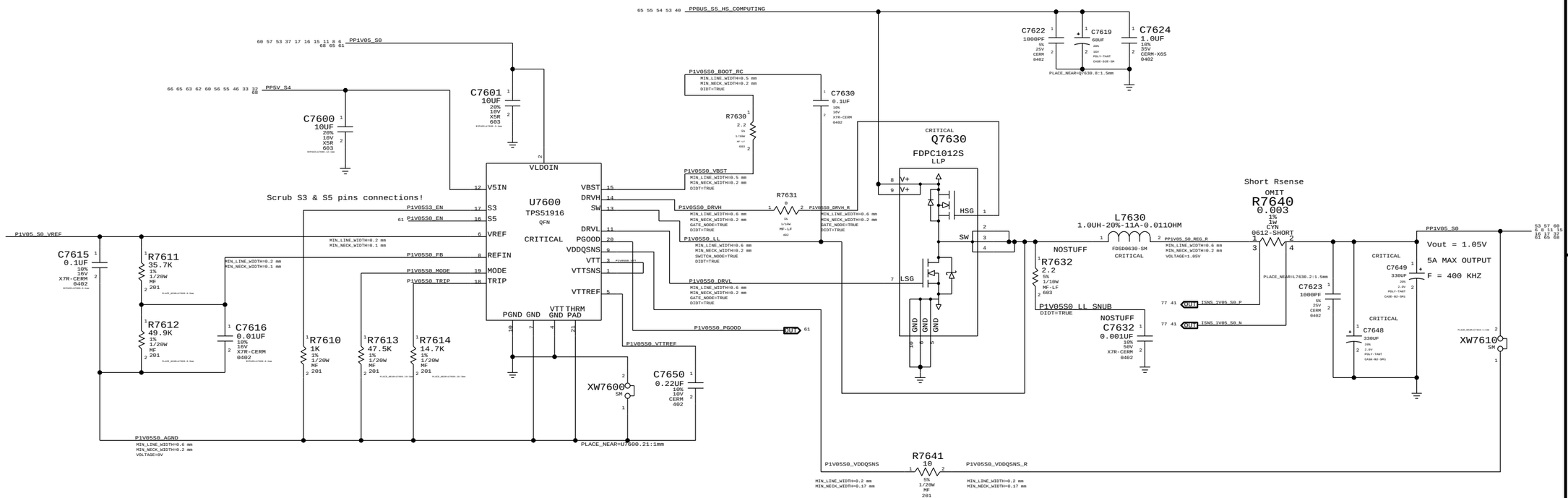
SYNC_MASTER=J44 SYNC_DATE=08/12/2013

PAGE TITLE
5V / 3.3V Power Supply

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D
REVISION <E4LABEL>
BRANCH <BRANCH>
PAGE 75 OF 120
SHEET 56 OF 78

1.05V S0 Regulator



SYNC_MASTER=J44 SYNC_DATE=08/12/2013

PAGE TITLE

1.05V S0 Power Supply

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

REVISION <E4LABEL>

BRANCH <BRANCH>

PAGE 76 OF 120

SHEET 57 OF 78

Page Notes

Power aliases required by this page:
- =PPVIN_S0SW_LCDBKLTFET (9-12.6V LCD BACKLIGHT INPUT)
- =PP5V_S0_BKLT (5V BACKLIGHT DRIVER INPUT)
- =PP5V_S0SW_KBDLED (5V KEYBOARD BACKLIGHT INPUT)

BOM options provided by this page:
BKLT:ENG - Stuffs 10.2 ohm series R for engineering builds
BKLT:PROD - Stuffs 0 ohm series R for production

SENSOR ON PAGE 54 USES R7700 TO MEASURE THE POWER GOING TO LCD BACKLIGHT

740S0159 CRITICAL F7700 3AMP-32V 0603

R7700 0.025 1% 1W MTL 0612

Q7700 FDC638APZ_SBMS001 SSOT6-HF CRITICAL

PPBUS_G3H → PPVIN_S0SW_LCDBKLT_F → PPVIN_S0SW_LCDBKLT_R

C7700 1000PF 10% 16V X7R-CERM 0201

R7701 80.6K 1% 1/16W MF-LF 402

NOSTUFF C7701 0.001UF 10% 50V CERM 402

PPVIN_S0SW_LCDBKLT: MIN_LINE_WIDTH=2 MM, MIN_NECK_WIDTH=0.25 MM, VOLTAGE=12.9V, MAKE_BASE=TRUE

ISNS_LCDBKLT_P (OUT)

ISNS_LCDBKLT_N (OUT)

LCDBKLT_EN_L

R7702 63.4K 1% 1/16W MF-LF 402

PP5V_S0

R7744 0 5% 1/16W MF-LF 402

R7745 0 5% 1/16W MF-LF 402

PP5V_S0_BKLT_A

PP5V_S0_BKLT_D

C7740 1UF 10% 10V X5R 402-1 PLACE_NEAR=U7700.5:5MM

C7741 1UF 10% 10V X5R 402-1 PLACE_NEAR=U7700.18:5MM

GND_BKLT_SGND

R7740 1M 5% 1/20W MF 201

U7700 LLP LP8548B1SQ_-04

SD, VSENSE_N, VSENSE_P, SENSE_OUT, ISET_KEYB, EN, PWM_KEYB, SCL (IPU), SDA (IPU), SW2, FB2, KEYB1, KEYB2, SW, FB, GD, VDDP, VDDA, GND_SW, GND_SW, GND_SW2, GNDD, GNDA, THRM PAD

BKLT_SD

BKLT_SENSE_OUT

R7742 0 5% 1/20W MF 0201 (EDP_BKLT_PSR_EN → BKLT_EN_R)

NO STUFF C7742 33PF 5% 25V NPO-C0G 0201

R7747 0 5% 1/20W MF 0201 (SMC_SYS_KBDLED → BKLT_PWM_KEYB)

NO STUFF C7747 33PF 5% 25V NPO-C0G 0201

GND_BKLT_SGND

XW7700 SM

R7720 10.2 0.1% 1/10W TF 402 BKLT:ENG PLACE_NEAR=U7700.13:10MM

R7721 10.2 0.1% 1/10W TF 402 BKLT:ENG PLACE_NEAR=U7700.14:10MM

R7741 31.6K 1% 1/20W MF 201 PLACE_NEAR=U7700.20:5MM

KBDLED_CATHODE1 MIN_LINE_WIDTH=0.3 MM, MIN_NECK_WIDTH=0.2 MM

KBDLED_CATHODE2 MIN_LINE_WIDTH=0.3 MM, MIN_NECK_WIDTH=0.2 MM

PPVOUT_BKLT_FB2

PP5V_S0_KBDBKLT_SW

XW7720 SM PLACE_NEAR=D7720.K:2MM

GND_BKLT_SGND MIN_LINE_WIDTH=0.4 MM, MIN_NECK_WIDTH=0.2 MM, VOLTAGE=0V

PLATFORM_RESET NO LONGER GATES THE BKLT_EN AS BOTH COME FROM PCH NOW

I2C ID DEDICATED.ONLY CONNECTS TO JERRY

R7752 2.4K 5% 1/20W MF 201

R7753 2.4K 5% 1/20W MF 201 PLACE_NEAR=U7700.15:10MM

R7750 0 5% 1/20W MF 0201 (I2C_BKLT_SCL → BKLT_SCL)

R7751 0 5% 1/20W MF 0201 (I2C_BKLT_SDA → BKLT_SDA) PLACE_NEAR=U7700.16:10MM

PP5V_S0 → 152S1701 CRITICAL L7720 10UH-20%-1.4A-0.17OHM PST041H-SM → PPVOUT_S0_KBDBKLT

C7720 2.2UF 10% 25V X5R-CERM 603

C7721 2.2UF 10% 25V X5R-CERM 603

C7722 0.1UF 10% 16V X5R-CERM 0201

RB160M-60G PLACE_NEAR=L7720.2:5MM

C7723 1.0UF 10% 50V X7R 0805

C7724 1.0UF 10% 50V X7R 0805

C7725 0.001UF 10% 50V X7R-CERM 0402

C7726 1.0UF 10% 50V X7R 0805

C7727 1.0UF 10% 50V X7R 0805

PLACEMENT_NOTE: SANDWICH C7720 AND C7721 PLACE_NEAR=L7720.1:5MM PLACE_NEAR=L7720.1:5MM PLACE_NEAR=L7720.1:5MM

PLACEMENT_NOTE: SANDWICH C7723 AND C7724 PLACE_NEAR=D7720.K:5MM PLACE_NEAR=D7720.K:5MM PLACE_NEAR=D7720.K:5MM

T-BONE C7726 AND C7727 PLACE_NEAR=D7720.K:9MM PLACE_NEAR=D7720.K:9MM

PPVIN_S0SW_LCDBKLT → 152S1527 CRITICAL L7710 22UH-20%-2.4A-0.105OHM DEM8030C-SM → PPVIN_SW_LCDBKLT_SW

C7710 4.7UF 10% 25V X6S-CERM 0603

C7711 4.7UF 10% 25V X6S-CERM 0603

C7712 0.1UF 10% 25V X5R 402

PLACEMENT_NOTE: SANDWICH C7710 AND C7711 PLACE_NEAR=L7710.1:5MM PLACE_NEAR=L7710.1:5MM PLACE_NEAR=L7710.1:5MM

371S0704 CRITICAL D7710 POWERDI-123 DFLS2100 PLACE_NEAR=L7710.2:3MM

PPVIN_SW_LCDBKLT_SW → LCDBKLT_TB_XWR

Q7701 CRITICAL SI7812DN PWRPK-1212-8 PLACE_NEAR=U7700.1:3MM

LCDBKLT_FET_DRV_R

R7733 0 5% 1/16W MF-LF 402

R7731 13.3K 1% 1/16W MF-LF 402

R7732 150K 1% 1/16W MF-LF 402

PPVOUT_S0_LCDBKLT → C7713 2.2UF 10% 10V X7R 1210-1; C7714 2.2UF 10% 10V X7R 1210-1; C7715 2.2UF 10% 10V X7R 1210-1; C7716 2.2UF 10% 10V X7R 1210-1; C7717 1000PF 10% 100V X7R-CERM 0603

PLACEMENT_NOTE: SANDWICH C7713 AND C7714 PLACE_NEAR=D7710.K:5MM; SANDWICH C7715 AND C7716 PLACE_NEAR=D7710.K:5MM PLACE_NEAR=D7710.K:5MM PLACE_NEAR=D7710.K:5MM PLACE_NEAR=D7710.K:5MM

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
116S0004	1	RES,MTL FILM,0 OHM,1A MAX,0402,SMD	R7720,R7721	CRITICAL	BKLT:PROD

PBUS LINE WIDTHS

PP5V_S0_BKLT_A: MIN_LINE_WIDTH=2 MM, MIN_NECK_WIDTH=0.25 MM, VOLTAGE=5V

PP5V_S0_BKLT_D: MIN_LINE_WIDTH=2 MM, MIN_NECK_WIDTH=0.25 MM, VOLTAGE=5V

PPVIN_S0SW_LCDBKLT_F: MIN_LINE_WIDTH=2 MM, MIN_NECK_WIDTH=0.25 MM, VOLTAGE=12.6V

PPVIN_S0SW_LCDBKLT_R: MIN_LINE_WIDTH=2 MM, MIN_NECK_WIDTH=0.25 MM, VOLTAGE=12.9V

PPVIN_S0SW_LCDBKLT_FET: MIN_LINE_WIDTH=2 MM, MIN_NECK_WIDTH=0.25 MM, VOLTAGE=12.9V

PPVIN_S0SW_LCDBKLT: MIN_LINE_WIDTH=2 MM, MIN_NECK_WIDTH=0.25 MM, VOLTAGE=12.9V

LCD BKLT LINE WIDTHS

LCDBKLT_FET_DRV_R: MIN_LINE_WIDTH=2 MM, MIN_NECK_WIDTH=0.25 MM, VOLTAGE=5V, GATE_NODE=TRUE, DIDT=TRUE

LCDBKLT_FET_DRV: MIN_LINE_WIDTH=2 MM, MIN_NECK_WIDTH=0.25 MM, VOLTAGE=5V, GATE_NODE=TRUE, DIDT=TRUE

LCDBKLT_SW: MIN_LINE_WIDTH=2 MM, MIN_NECK_WIDTH=0.25 MM, VOLTAGE=53V, SWITCH_NODE=TRUE, DIDT=TRUE

PPVIN_SW_LCDBKLT_SW: MIN_LINE_WIDTH=2 MM, MIN_NECK_WIDTH=0.25 MM, VOLTAGE=53V, SWITCH_NODE=TRUE, DIDT=TRUE

PPVOUT_S0_LCDBKLT: MIN_LINE_WIDTH=0.5 MM, MIN_NECK_WIDTH=0.25 MM, VOLTAGE=53V

PPVOUT_BKLT_FB: MIN_LINE_WIDTH=0.4 MM, MIN_NECK_WIDTH=0.25 MM, VOLTAGE=53V

KBD BKLT LINE WIDTHS

PP5V_S0_KBDBKLT_SW: MIN_LINE_WIDTH=0.5 MM, MIN_NECK_WIDTH=0.25 MM, VOLTAGE=40V, SWITCH_NODE=TRUE, DIDT=TRUE

PPVOUT_S0_KBDBKLT: MIN_LINE_WIDTH=0.5 MM, MIN_NECK_WIDTH=0.2 MM, VOLTAGE=40V

PPVOUT_BKLT_FB2: MIN_LINE_WIDTH=0.4 MM, MIN_NECK_WIDTH=0.25 MM, VOLTAGE=40V

SYNC_MASTER=J44 SYNC_DATE=08/12/2013

PAGE TITLE: LCD AND KBD BKLT DRIVER

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

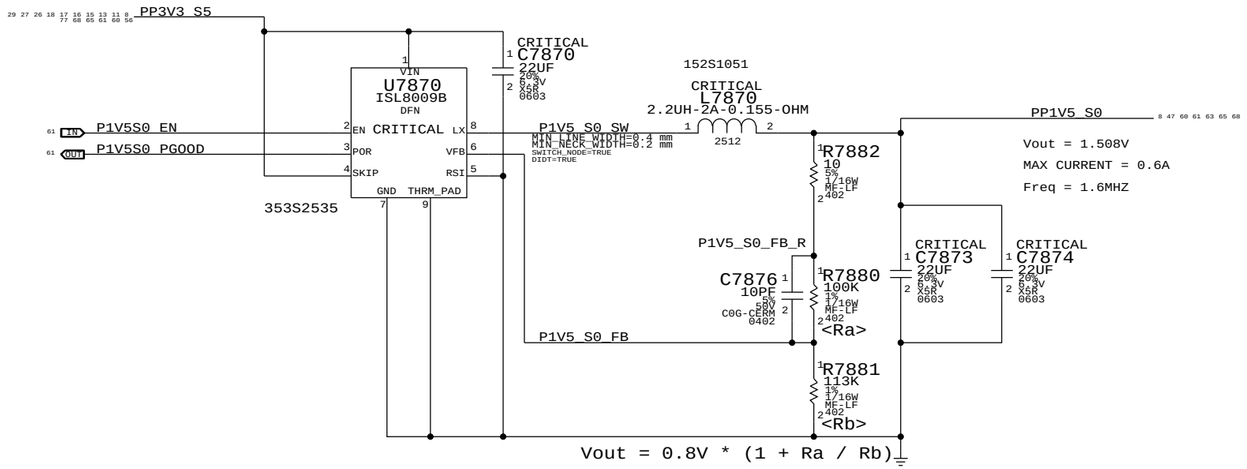
REVISION: <E4LABEL>

BRANCH: <BRANCH>

PAGE: 77 OF 120

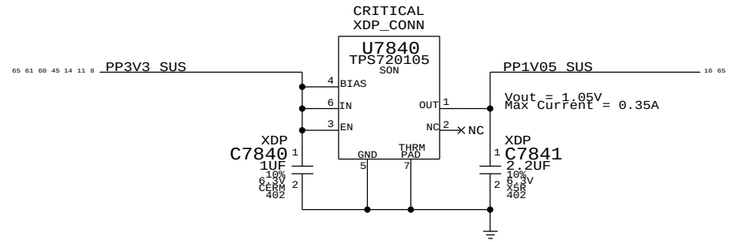
SHEET: 58 OF 78

1.5V S0 Switcher



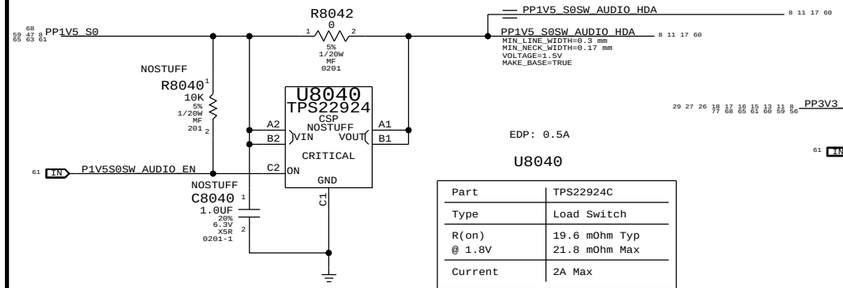
1.05V SUS LDO

Cougar Point requires JTAG pull-ups to be powered at 1.05V when SUS suspend well is active.
Pull-ups (3) must be 51 ohms to support XDP (not required in production).
70mA is required to support pull-ups. Alternative is strong voltage
dividers (200/100) to 3.3V S5, which burns 100mW in all S-states.



1.5V S0 Audio Switch (BYPASSED)

Loading specs per J41/43_PowerBudget_Riviera_rev0.99e

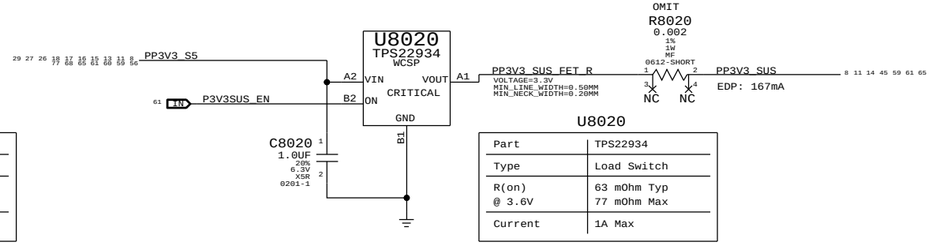


EDP: 0.5A

U8040

Part	TPS22924C
Type	Load Switch
R(on) @ 1.8V	19.6 mOhm Typ 21.8 mOhm Max
Current	2A Max

3.3V SUS Switch

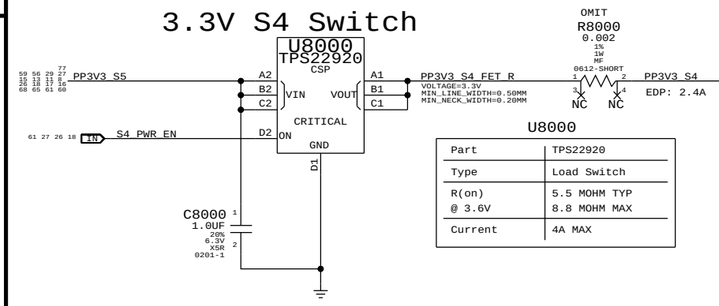


EDP: 167mA

U8020

Part	TPS22934
Type	Load Switch
R(on) @ 3.6V	63 mOhm Typ 77 mOhm Max
Current	1A Max

3.3V S4 Switch

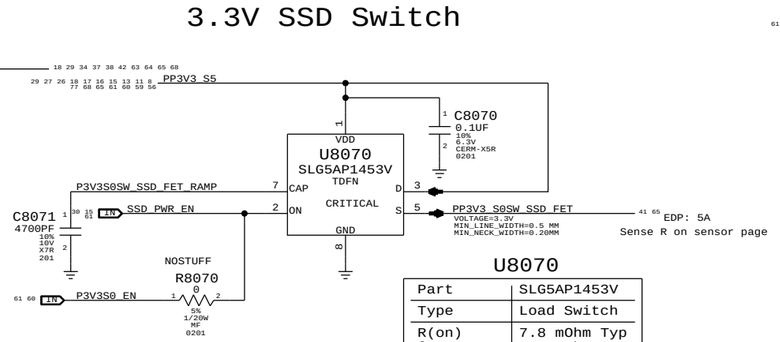


EDP: 2.4A

U8000

Part	TPS22920
Type	Load Switch
R(on) @ 3.6V	5.5 MOHM TYP 8.8 MOHM MAX
Current	4A MAX

3.3V SSD Switch



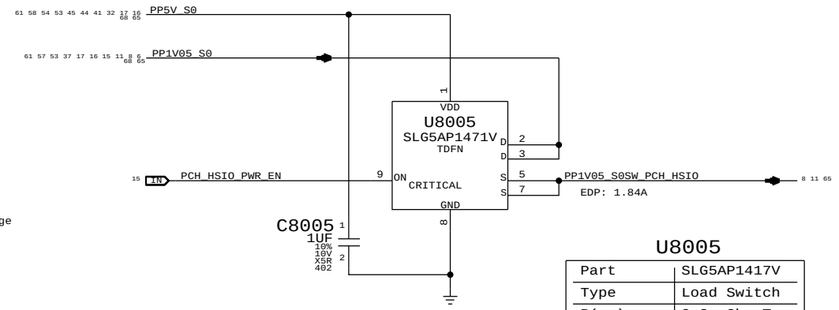
EDP: 5A

Sense R on sensor page

U8070

Part	SLG5AP1453V
Type	Load Switch
R(on) @ 25C	7.8 mOhm Typ 8.5 mOhm Max
Current	5.3A Max

1.05V PCH HSIO Switch

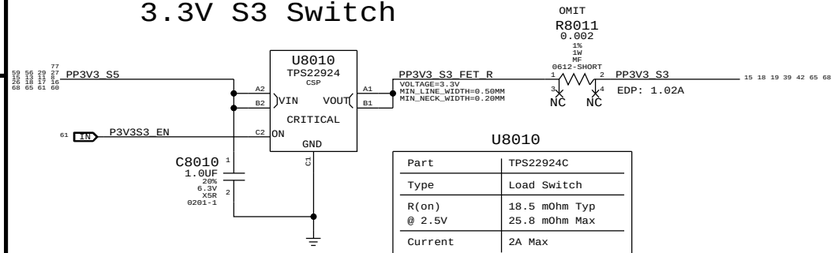


EDP: 1.84A

U8005

Part	SLG5AP1417V
Type	Load Switch
R(on) @ 4V Vgs	9.8 mOhm Typ TBD mOhm Max
Current	6A Max

3.3V S3 Switch



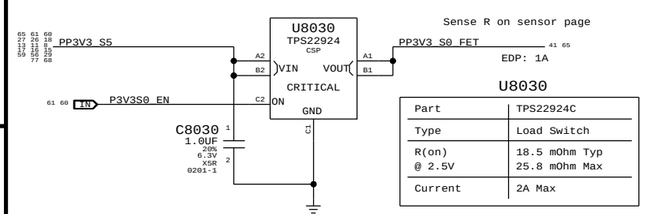
EDP: 1.02A

U8010

Part	TPS22924C
Type	Load Switch
R(on) @ 2.5V	18.5 mOhm Typ 25.8 mOhm Max
Current	2A Max

REMOVED THE ANALOG POWER GATE AS SLG5AP1471 SHOULD BE AVAILABLE BY THEN

3.3V S0 Switch



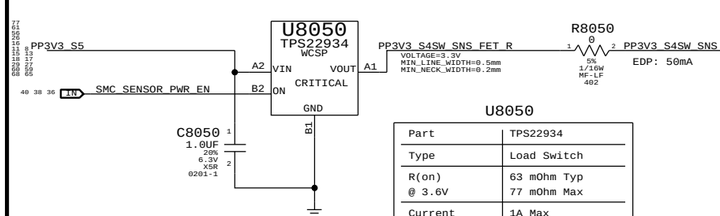
Sense R on sensor page

EDP: 1A

U8030

Part	TPS22924C
Type	Load Switch
R(on) @ 2.5V	18.5 mOhm Typ 25.8 mOhm Max
Current	2A Max

3.3V Sensor Switch

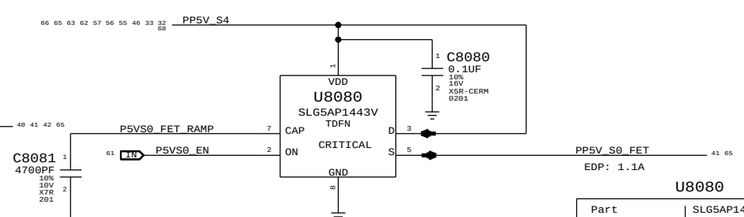


EDP: 50mA

U8050

Part	TPS22934
Type	Load Switch
R(on) @ 3.6V	63 mOhm Typ 77 mOhm Max
Current	1A Max

5V S0 Switch



EDP: 1.1A

U8080

Part	SLG5AP1443V
Type	Load Switch
R(on)	15 mOhm Typ 17 mOhm Max
Current	2.5A

SYNC_MASTER=J44 SYNC_DATE=08/12/2013

PAGE TITLE: Power FETs

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

REVISION: <E4LABEL>

BRANCH: <BRANCH>

PAGE: 80 OF 120

SHEET: 60 OF 78

S5 Enables

PLACE_NEAR=U7501.21:7mm

SMC_PM_G2_EN (OUT) → R8140 100 5% 1/20W MF 201 → S5_PWR_EN (IN), MAKE_BASE=TRUE → S5_PWR_EN (OUT)

NOSTUFF C8142 0.47UF 10% 6.3V CERM-X5R 402 PLACE_NEAR=U7501.21:7mm

S5 Power Good

PP3V42_G3H

PLACE_NEAR=U7501.20:7mm

R8141 100K 5% 1/20W MF 201

S5_PWRGD-->SMC

SMC-->PM_DSW_PWRGD

S5_PWRGD (IN) → S5_PWRGD (OUT), MAKE_BASE=TRUE

SSD Enable

SSD_PWR_EN (IN), MAKE_BASE=TRUE → SSD_PWR_EN (OUT)

Standby Enables

PP3V3_S5

NOSTUFF C8170 0.1UF 10% 6.3V CERM-X5R 0201

BYPASS=U8170.6:2.3mm

NOSTUFF U8170 74LVC1G32 SOT891

PM_SLP_S5_L (IN)

SMC_S4_WAKESRC_EN (IN)

S4_PWR_EN, MAKE_BASE=TRUE → S4_PWR_EN (OUT) ×3

R8115 0 5% 1/20W MF 0201

NCX

S3 Enables

PM_SLP_S4_L (IN)

R8111 20K 5% 1/20W MF 201

R8112 0 5% 1/20W MF 0201

R8113 3.3K 5% 1/20W MF 201

TPAD_VBUS_EN → (OUT) 34

P3V3S3_EN, MAKE_BASE=TRUE → (OUT) 60 61

DDRREG_EN, MAKE_BASE=TRUE → (OUT) 55 61

C8111 0.1UF 20% 10V CERM 402

NO STUFF C8112 0.47UF 10% 6.3V CERM-X5R 402

NO STUFF C8113 0.47UF 10% 6.3V CERM-X5R 402

R8117 100 5% 1/20W MF 201

USB_PWR_EN, MAKE_BASE=TRUE → USB_PWR_EN (OUT) 33 61

NO STUFF C8114 0.47UF 10% 6.3V CERM-X5R 402

Mobile System Power State Table

State	SMC_ADAPTER_EN	SMC_PM_G2_ENABLE	SMC_S4_WAKESRC_EN	PM_SUS_EN	PM_SLP_S3_L	PM_SLP_S4_L	PM_SLP_S5_L
Run (S0)	X	1	1	1	1	1	1
Sleep (S3AC)	1	1	1	1	1	1	0
Sleep (S3)	0	1	1	1	1	1	0
Deep Sleep (S4AC)	1	1	1	0	0	0	0
Deep Sleep (S4)	0	1	1	0	0	0	0
Deep Sleep (S5AC)	1	1	0	0	0	0	0
Deep Sleep (S5)	0	1	0	0	0	0	0
Battery Off (S5WithAC)	toggle 3Hz	0	0	0	0	0	0
Battery Off (S5Wo)	1	0	0	0	0	0	0

S0 Rail PGOOD (BJT Version)

PP5V_S0

R8151 54.9K 1% 1/20W MF 201

VMON_5V_DIV

5.0V Divider: 1.07V

R8152 15K 1% 1/20W MF 201

R8153 1K 5% 1/20W MF 201

C8159 1UF 10% 10V X5R 402

9ms RC delay

R8156 150K 1% 1/20W MF 201

S0PGD_C

PP3V3_S0

R8158 15K 1% 1/20W MF 201

VMON_3V3_DIV

3.3V Divider: 1.07V

R8159 7.15K 1% 1/20W MF 201

R8154 1K 5% 1/20W MF 201

VMON_Q2_BASE, VMON_Q3_BASE

Q8150 CRITICAL ASMCC0179 DFN2015H4-8 376S0854 (Q1, Q2, Q3, Q4)

NC

ALL_SYS_PWRGD → 16 17 36 61

S0PGD_BJT_GND_R

R8157 100 5% 1/20W MF 201

PP1V5_S0

R8155 1K 5% 1/20W MF 201

VMON_Q4_BASE

Vbe 0.7V max @ 2mA

Vce(sat) 0.1V max @ 1mA

Q1 Vth 0.7~1V @Id 250uA

1.5V Codec Enable(BYPASSED NOW)

PLACE_NEAR=U8040.C2:7mm

AUD_PWR_EN (IN) → R8145 100K 1% 1/20W MF 201 → P1V5S0SW_AUDIO_EN (OUT) 60

NOSTUFF D8146 SM-201 RB521ZS-30 PLACE_NEAR=U8040.C2:7mm

P1V5CODEC_EN_D

NOSTUFF R8146 1K 1% 1/20W MF 201

NOSTUFF C8146 0.1UF 10% 25V X5R 402 PLACE_NEAR=U8040.C2:7mm

S0 Enables

PP3V3_S5

C8180 0.1UF 10% 6.3V CERM-X5R 0201

BYPASS=U8180.6:3mm

PM_SLP_S3_L (IN) → R8178 100 5% 1/20W MF 201 → PM_SLP_S3_R_L

U8180 MC74VHC1G08 SC70-HF

PM_SLP_S3_BUF_L, MAKE_BASE=TRUE

NOSTUFF R8180 330K 5% 1/20W MF 201

P1V05_EN_D

NO STUFF D8185 SM-201 RB521ZS-30

NO STUFF R8138 820 5% 1/20W MF 201

R8185 0 5% 1/20W MF 0201

R8184 330 5% 1/20W MF 201

P3V3S0_EN_D

D8184 SM-201

R8186 39K 5% 1/20W MF 201

R8187 0 5% 1/20W MF 0201

R8183 330 5% 1/20W MF 201

P1V5S0_EN_D

D8183 SM-201

R8188 68K 5% 1/20W MF 201

PM_SLP_S3_BUF_L (OUT) 26 27 46 61

P1V5S0_EN, MAKE_BASE=TRUE → P1V5S0_EN (OUT) 59 61

P5VS0_EN, MAKE_BASE=TRUE → P5VS0_EN (OUT) 60 61

P3V3S0_EN, MAKE_BASE=TRUE → P3V3S0_EN (OUT) 60 61

P1V05S0_EN, MAKE_BASE=TRUE → P1V05S0_EN (OUT) 57 61

NO STUFF C8185 0.22UF 10% 10V CERM 402

NO STUFF C8186 0.1UF 20% 10V CERM 402

NO STUFF C8187 0.68UF 10% 6.3V CERM 402

C8188 0.1UF 20% 10V CERM 402

3.3V SUS Detect

PP3V3_S5

No stuff C8131, 12ms Min delay time

U8130 Sense input threhold is 3.07V

BYPASS=U8130.6:2.3mm

C8130 0.1UF 10% 6.3V CERM-X5R 0201

PP3V3_SUS → 8 11 14 45 59 60 61 65

R8133 100K 5% 1/20W MF 201

CRITICAL

U8130 TPS3808G33 QFN

PP3V3_SUS → SENSE

RESET* → PM_RSMRST_L (OUT) 13 72

CT → SUS_PGOOD_CT

MR* → TP_SUS_PGOOD_MR_L

GND, THRM PAD

NO STUFF C8131 1000PF 10% 16V X7R-CERM 0201

CHGR VFRQ Generation

PP3V42_G3H

R8131 330K 5% 1/20W MF 201

VFRQ Low: Fix Frequency

VFRQ High: Variable Frequency

CHGR_VFRQ (OUT) 52

Q8131 DMN32D2LFB4 DFN1006H4-3 SYM_VER_2

PM_SLP_S3_R_L (IN) 61

S0 Rail PGOOD Circuitry

(ISL version used for development)

Thresholds:

VDD: 2.734V-3.010V

V2MON: 2.815V-3.099V

V3MON: 0.572V-0.630V

V4MON: 0.572V-0.630V

PP1V05_S0, PP3V3_S0

PP1V5_S0

PP5V_S0

5V Divider: 3.19V @ 4.5Vmin

1.5V Divider: 0.718V @ 1.45Vmin

1.05V Divider: 0.723V @ 1.02Vmin

R8160 6.04K 1% 1/20W MF 201

R8170 15K 1% 1/20W MF 201

R8172 6.04K 1% 1/20W MF 201

R8161 15K 1% 1/20W MF 201

R8171 15K 1% 1/20W MF 201

R8173 15K 1% 1/20W MF 201

S0PGOOD_ISL

C8160 0.1UF 10% 6.3V CERM-X5R 0201

U8160 ISL88042IRTEZ TDFN CRITICAL

V2MON, V3MON, V4MON

P5V_DIV_VMON, P1V5_DIV_VMON, P1V05_DIV_VMON

(IPU) MR* → NC

353S2310

RST* → ALL_SYS_PWRGD_R

GND, THRM_PAD

R8162 330 5% 1/20W MF 201

ALL_SYS_PWRGD (OUT) 16 17 36 61

R8167 10K 5% 1/20W MF 201

R8169 100 5% 1/20W MF 201 ← P1V5S0_PGOOD (IN)

R8165 100 5% 1/20W MF 201 ← P5VS4RS3_PGOOD (IN) 56

R8164 100 5% 1/20W MF 201 ← P1V05S0_PGOOD (IN) 57

R8168 100 5% 1/20W MF 201 ← DDRREG_PGOOD (IN) 55

SUS Enables

PM_SLP_SUS_L (IN), MAKE_BASE=TRUE → PM_SLP_SUS_L (OUT) 13 40 61

R8190 0 5% 1/20W MF 0201

P3V3SUS_EN, MAKE_BASE=TRUE → P3V3SUS_EN (OUT) 60 61

NO STUFF C8190 0.1UF 10% 25V X5R 402

P5VS4RS3_EN Enable

PM_SLP_S4_L (IN) 63 61 36 29 18 13

R8179 0 5% 1/20W MF 0201

P5VS4RS3_EN_RC

NO STUFF D8175 SM-201 RB521ZS-30

R8175 0 5% 1/20W MF 0201

NO STUFF R8176 240 5% 1/20W MF 201

P5VS4RS3_EN_D

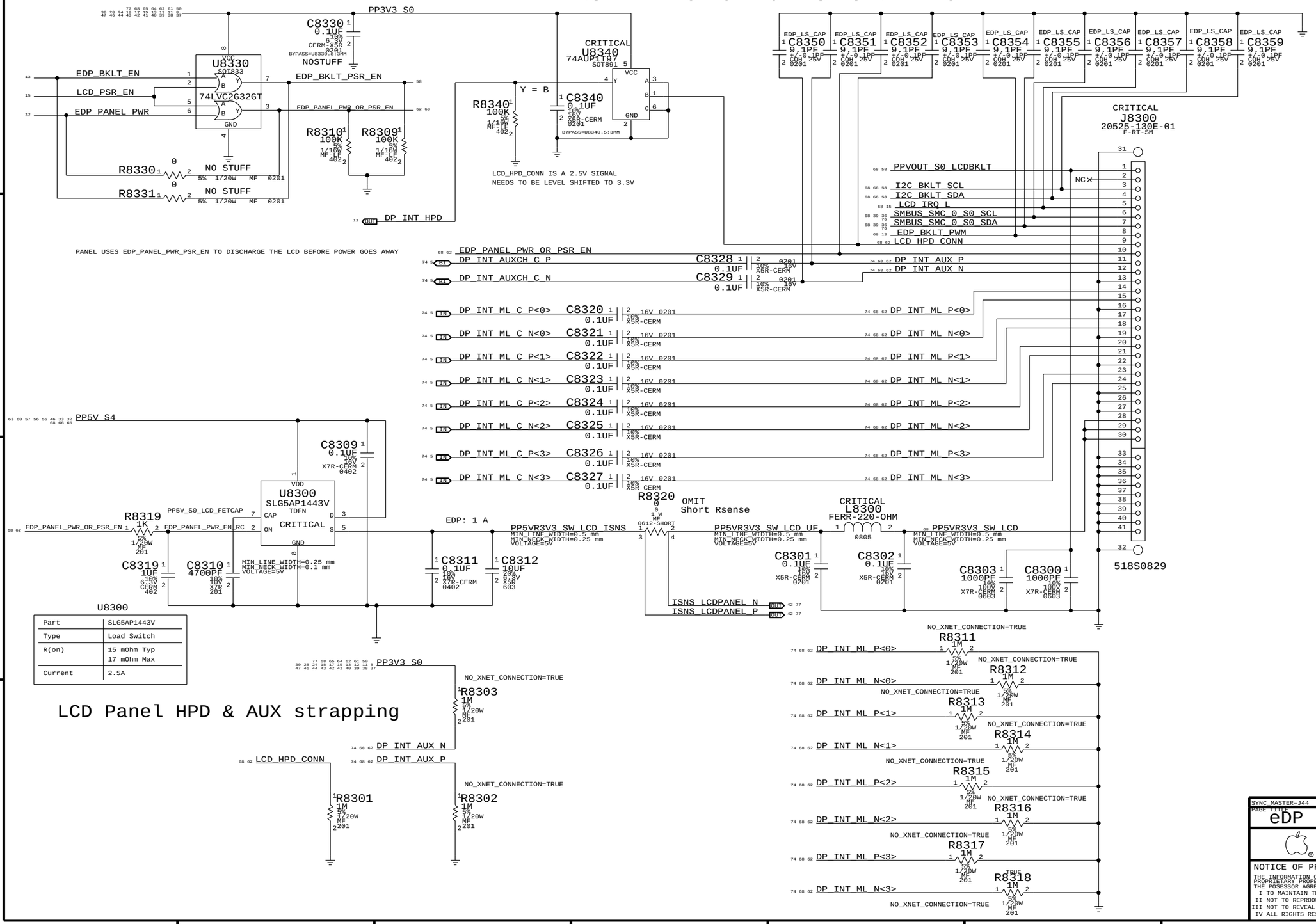
5V needs to be held up so 1.05V can fall after 1.5V

P5VS4RS3_EN (OUT) 56

NO STUFF C8175 2.2UF 10% 6.3V X5R 402

SYNC_MASTER=J44	SYNC_DATE=08/12/2012
PAGE TITLE	Power Control
Apple Inc.	DRAWING NUMBER <SCH_NUM> SIZE D
	REVISION <E4LABEL>
	BRANCH <BRANCH>
	PAGE 81 OF 120
	SHEET 61 OF 78

LCD PANEL INTERFACE (eDP)
NEEDS FINAL CHECK AGAINST UPDATE FOR NEW PANEL

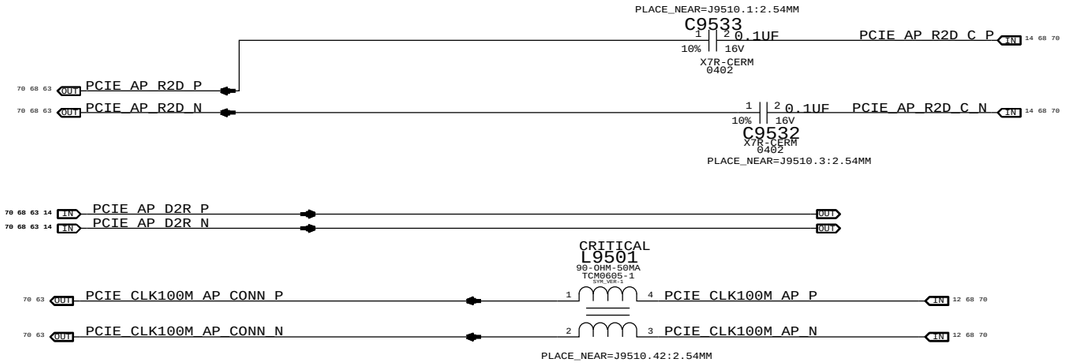


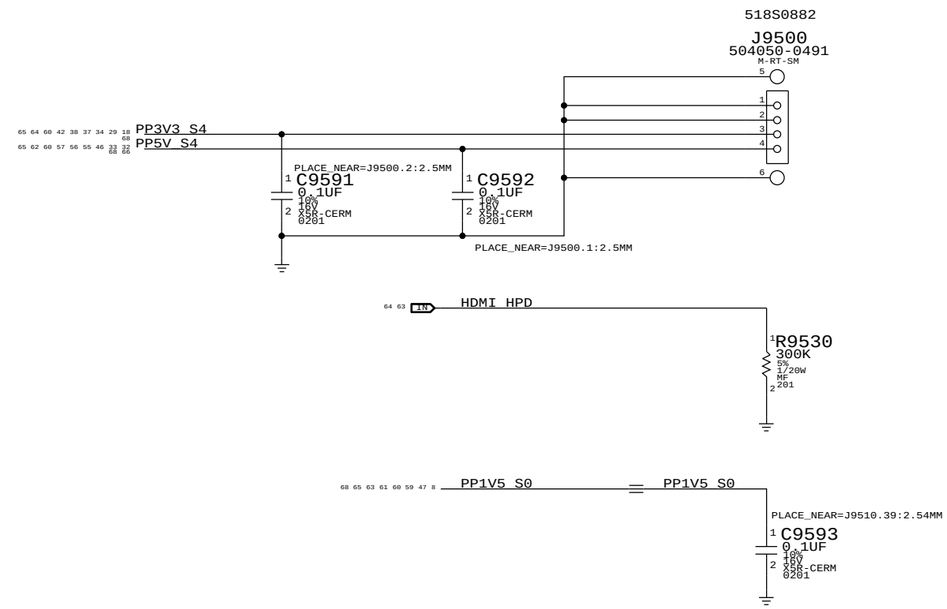
SYNC_MASTER=J44 SYNC_DATE=08/12/2013

PAGE TITLE
eDP Display Connector

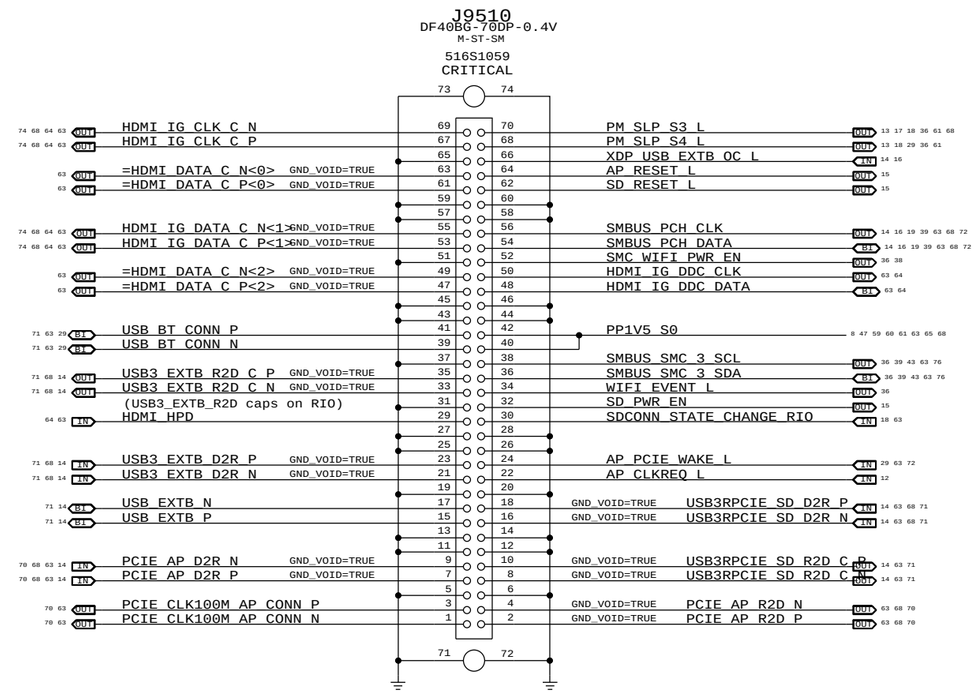
Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D
REVISION <E4LABEL>
BRANCH <BRANCH>
PAGE 83 OF 120
SHEET 62 OF 78

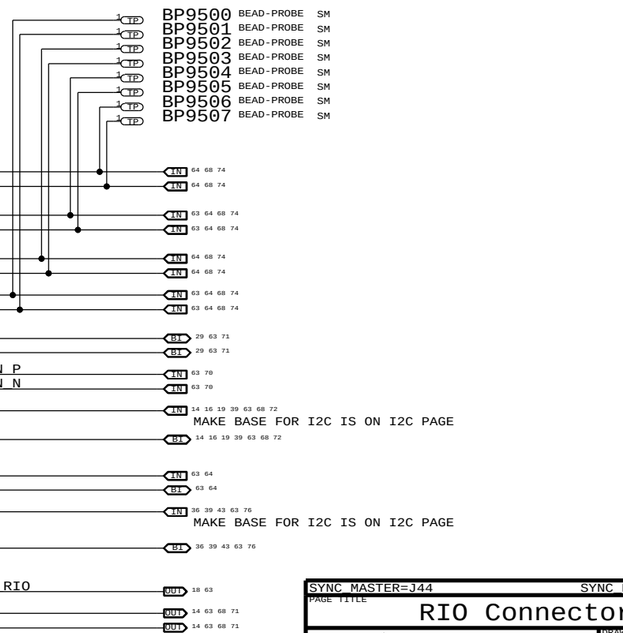




RIO FLEX CONNECTOR



NOTE: This connector is shielded 70P Hirose Plug APN 516S1059, mates with APN 516S1058.



SYNC_MASTER=J44 SYNC_DATE=08/12/2013

PAGE TITLE: RIO Connector

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

REVISION: <E4LABEL>

BRANCH: <BRANCH>

PAGE: 95 OF 120

SHEET: 63 OF 78

DISPLAY MUX: DP OR HDMI

DP 1:2 ANALOG DEMUX

PP3V3_S0

C9750 0.1UF 20% 10V X7S-CERM 0402

C9751 0.1UF 20% 10V X7S-CERM 0402

U9750 HD3SS213ZQE BGA CRITICAL

DP_TBTSNK1_ML_C_P<0>	B4	DA0(P)
DP_TBTSNK1_ML_C_N<0>	A4	DA0(N)
DP_TBTSNK1_ML_C_P<1>	B5	DA1(P)
DP_TBTSNK1_ML_C_N<1>	A5	DA1(N)
DP_TBTSNK1_ML_C_P<2>	B6	DA2(P)
DP_TBTSNK1_ML_C_N<2>	A6	DA2(N)
DP_TBTSNK1_ML_C_P<3>	A8	DA3(P)
DP_TBTSNK1_ML_C_N<3>	A9	DA3(N)
DP_TBTSNK1_AUXCH_C_P	H9	AUXA(P)
DP_TBTSNK1_AUXCH_C_N	J9	AUXA(N)
DP_TBTSNK1_DDC_CLK	H8	DDCCLK_A
DP_TBTSNK1_DDC_DATA	J8	DDCDAT_A
DP_TBTSNK1_HPD	J2	HPDA
HDMI_IG_DATA_C_P<2>	B8	DB0(P)
HDMI_IG_DATA_C_N<2>	B9	DB0(N)
HDMI_IG_DATA_C_P<1>	D8	DB1(P)
HDMI_IG_DATA_C_N<1>	D9	DB1(N)
HDMI_IG_DATA_C_P<0>	E8	DB2(P)
HDMI_IG_DATA_C_N<0>	E9	DB2(N)
HDMI_IG_CLK_C_P	F8	DB3(P)
HDMI_IG_CLK_C_N	F9	DB3(N)
NC	H6	AUXB(P)
NC	J6	AUXB(N)
HDMI_IG_DDC_CLK	H5	DDCCLK_B
HDMI_IG_DDC_DATA	J5	DDCDAT_B
HDMI_HPD	H3	HPDB
DISP_MUX_SEL_L	A1	DX_SEL
DISP_MUX_EN	B7	OE
	A2	VDD
	J4	VDD
	B3, C8, G8, H4, H7, C2	GND

TOWARDS PORTS

DP_HDMI_TBT_ML_P<0>	B2	DC0(P)
DP_HDMI_TBT_ML_N<0>	B1	DC0(N)
DP_HDMI_TBT_ML_P<1>	D2	DC1(P)
DP_HDMI_TBT_ML_N<1>	D1	DC1(N)
DP_HDMI_TBT_ML_P<2>	E2	DC2(P)
DP_HDMI_TBT_ML_N<2>	E1	DC2(N)
DP_HDMI_TBT_ML_P<3>	F2	DC3(P)
DP_HDMI_TBT_ML_N<3>	F1	DC3(N)
DP_HDMI_TBT_AUX_P	H2	AUXC(P)
DP_HDMI_TBT_AUX_N	H1	AUXC(N)
DPMUX_HPD_OUT	J1	HPDC
DP_HDMI_TBT_DDC_CLK	J3	DDCCLK_C
DP_HDMI_TBT_DDC_DATA	J7	DDCDAT_C
DPMUX_AUX_DDC_SEL	C2	AUX_SEL

TOWARDS CPU

R9752 100K 5% 1/20W MF 201

R9753 100K 5% 1/20W MF 201

Q9700 DMN32D2LFB4 DFN1006H4-3 SYM_VER_2

HDMITBTMUX_SEL_TBT

DISP MUX SEL_L
SEL_L 0 = DP
SEL_L 1 = HDMI

NOTE: HDMI ML SWIZZLED INTENTIONALLY AS PER TABLE 9-1 HASWELL-ULT PDG

PP3V3_S0

C9725 0.1UF 20% 10V X6S-CERM 0201

NO STUFF R9725 10K 5% 1/20W MF 201

R9726 10K 5% 1/20W MF 201

R9727 10K 5% 1/20W MF 201

TOWARDS PORTS

PP3V3_S0

NO STUFF R9755 100K 5% 1/20W MF 201

NO STUFF Q9701 DMN32D2LFB4 DFN1006H4-3 SYM_VER_2

DISP_MUX_EN

U9725 PI3USB102ZLE TQFN CRITICAL

VCC

NO STUFF

GND

SIGNAL_MODEL=MOJO_MUX

HDMI_IG_DDC_CLK	5	M+
HDMI_IG_DDC_DATA	4	M-
DP_TBTSNK1_DDC_CLK	7	D+
DP_TBTSNK1_DDC_DATA	6	D-
DISP_MUX_EN_L	8	OE*
	1	Y+
	2	Y-
HDMITBTMUX_SEL_TBT	10	SEL

DP_HDMI_TBT_DDC_CLK	13 64 66	TOWARDS CPU
DP_HDMI_TBT_DDC_DATA	13 64 66	

DISP MUX SEL
SEL 0 = HDMI
SEL 1 = DP

PP3V3_S0

C9700 0.1UF 10% 6.3V CERM-X5R 0201

OMIT_TABLE

U9700 SLG4APXXX TDFN

THRM PAD

DP_TBTSNK1_HPD	2	IO_2
HDMI_HPD	3	IO_3
HDMITBTMUX_LATCH	4	IO_4
	1	VDD
	8	IO_8
	7	IO_7
	6	IO_6
	5	GND
DISP_MUX_EN	64	
HDMITBTMUX_SEL_TBT	15 23 64 66	
HDMITBTMUX_FLAG_L	15 64	

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
343S0666	1	IC, SAK,AP4179,DP MUX CTRLR,TDFN-8	U9700	CRITICAL	

PP3V3_S0

NOSTUFF R9701 100K 5% 1/20W MF 201

R9703 510K 5% 1/20W MF 201

DISP_MUX_PRIORITY

DPMUX_AUX_DDC_SEL

R9702 100K 5% 1/20W MF 201

R9704 510K 5% 1/20W MF 201

PRIORITY 0 = HDMI WINS OVER DP
PRIORITY 1 = DP WINS OVER HDMI

AUX_SEL 0 = AUX ONLY
AUX_SEL 1 = DDC ONLY
AUX_SEL Vdd/2 = AUX & DDC

PP3V3_S4

PP3V3_S0

C9775 0.1UF 10% 6.3V CERM-X5R 0201

NOSTUFF CRITICAL U9775 SLG46400V TDFN

R9754 100K 5% 1/20W MF 201

HDMI_HPD	2	GPI(2)
DP_TBTSNK1_HPD	3	GPIO(3)
	4	GPIO(4)
NC	5	GPIO(5)
DISP_MUX_PRIORITY	6	GPIO(6)
HDMITBTMUX_LATCH		THRM_PAD
	1	VDD
	12	GPIO(12)
	11	GPIO(11)
	10	GPIO(10)
	9	GPIO(9)
	8	GPIO(8)
	7	GND
NC		
NC		
HDMITBTMUX_FLAG_L	15 64	
DISP_MUX_EN	64	
HDMITBTMUX_SEL_TBT	15 23 64 66	

DISP MUX SEL
SEL 0 = HDMI
SEL 1 = DP

SYNC_MASTER=J44 SYNC_DATE=08/12/2013

PAGE TITLE: Display Mux: HDMI vs DP

Apple Inc.

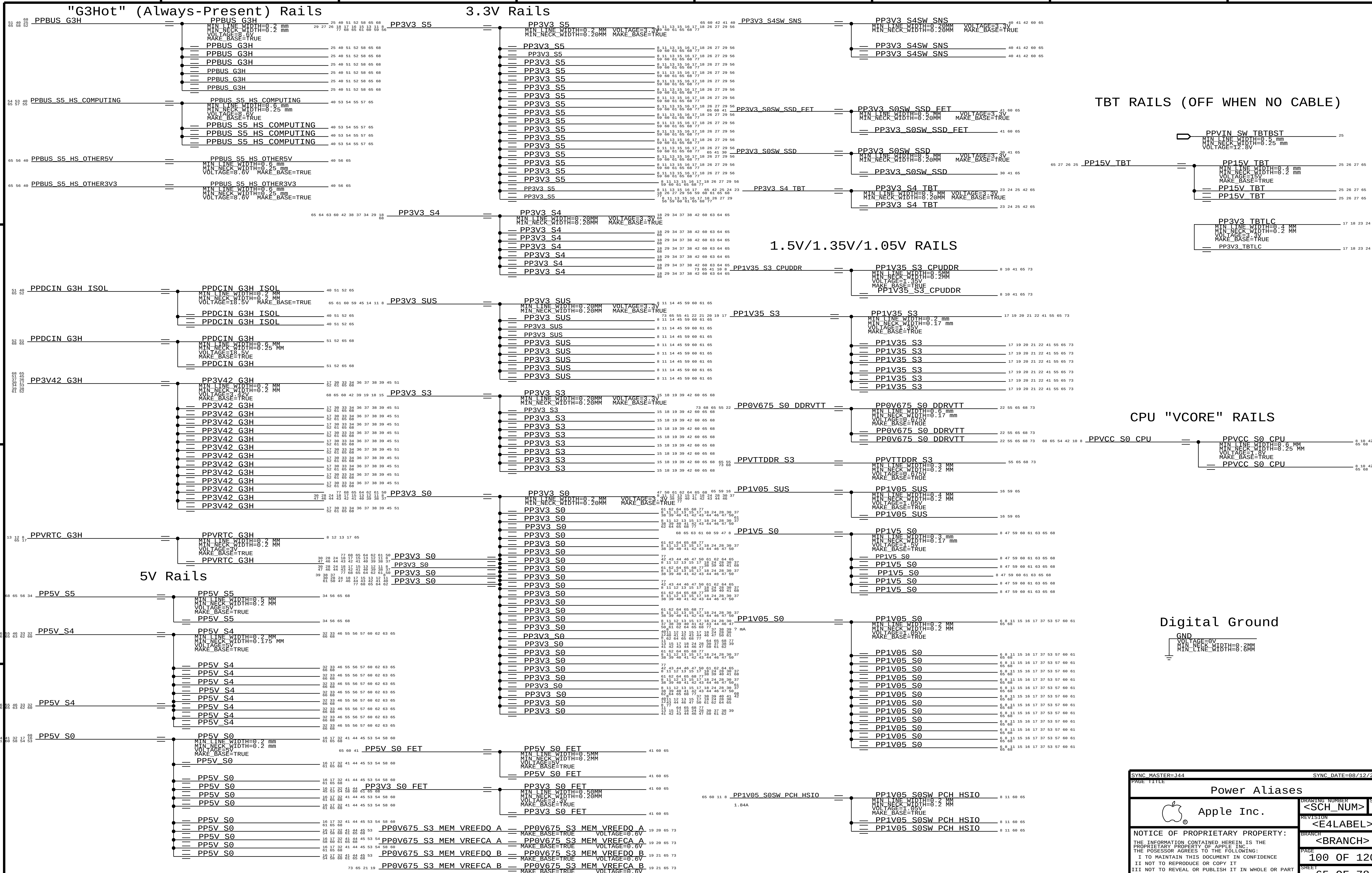
DRAWING NUMBER: <SCH_NUM> SIZE: D

REVISION: <E4LABEL>

BRANCH: <BRANCH>

PAGE: 97 OF 120

SHEET: 64 OF 78



SYNC_MASTER=J44 SYNC_DATE=08/12/2013

PAGE TITLE

Power Aliases

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

REVISION <E4LABEL>

BRANCH <BRANCH>

PAGE 100 OF 120

SHEET 65 OF 78

MEMORY ADDRESS/CTRL

MAKE_BASE

7	=MEM_A_A<0>	TRUE	MEM_A_A<0>	20 22 73	
7	=MEM_A_A<1>	TRUE	MEM_A_A<1>	20 22 73	
7	=MEM_A_A<2>	TRUE	MEM_A_A<2>	20 22 73	
7	=MEM_A_A<3>	TRUE	MEM_A_A<3>	20 22 73	
7	=MEM_A_A<4>	TRUE	MEM_A_A<4>	20 22 73	
7	=MEM_A_A<5>	TRUE	MEM_A_A<5>	20 22 73	
66 22 20 7 73	MEM_A_A<6>	TRUE	MEM_A_A<6>	7 20 22 66 73	
7	=MEM_A_A<7>	TRUE	MEM_A_A<7>	20 22 73	
7	=MEM_A_A<8>	TRUE	MEM_A_A<8>	20 22 73	
7	=MEM_A_A<9>	TRUE	MEM_A_A<9>	20 22 73	
7	=MEM_A_A<10>	TRUE	MEM_A_A<10>	20 22 73	
7	=MEM_A_A<11>	TRUE	MEM_A_A<11>	20 22 73	
7	=MEM_A_A<12>	TRUE	MEM_A_A<12>	20 22 73	
7	=MEM_A_A<13>	TRUE	MEM_A_A<13>	20 22 73	
7	=MEM_A_A<14>	TRUE	MEM_A_A<14>	20 22 73	

MAKE_BASE

7	=MEM_B_A<0>	TRUE	MEM_B_A<0>	21 22 73	
7	=MEM_B_A<1>	TRUE	MEM_B_A<1>	21 22 73	
7	=MEM_B_A<2>	TRUE	MEM_B_A<2>	21 22 73	
7	=MEM_B_A<3>	TRUE	MEM_B_A<3>	21 22 73	
7	=MEM_B_A<4>	TRUE	MEM_B_A<4>	21 22 73	
7	=MEM_B_A<5>	TRUE	MEM_B_A<5>	21 22 73	
66 22 21 7 73	MEM_B_A<6>	TRUE	MEM_B_A<6>	7 21 22 66 73	
7	=MEM_B_A<7>	TRUE	MEM_B_A<7>	21 22 73	
7	=MEM_B_A<8>	TRUE	MEM_B_A<8>	21 22 73	
7	=MEM_B_A<9>	TRUE	MEM_B_A<9>	21 22 73	
7	=MEM_B_A<10>	TRUE	MEM_B_A<10>	21 22 73	
7	=MEM_B_A<11>	TRUE	MEM_B_A<11>	21 22 73	
7	=MEM_B_A<12>	TRUE	MEM_B_A<12>	21 22 73	
7	=MEM_B_A<13>	TRUE	MEM_B_A<13>	21 22 73	
7	=MEM_B_A<14>	TRUE	MEM_B_A<14>	21 22 73	

MAKE_BASE

66 22 7	MEM_A_ODT_CPU0	TRUE	MEM_A_ODT_CPU0	7 22 66	
66 22 20 7 73	MEM_A_RAS_L	TRUE	MEM_A_RAS_L	7 20 22 66 73	
66 22 20 7 73	MEM_A_WE_L	TRUE	MEM_A_WE_L	7 20 22 66 73	
66 22 20 7 73	MEM_A_CAS_L	TRUE	MEM_A_CAS_L	7 20 22 66 73	
7	=MEM_A_BA<0>	TRUE	MEM_A_BA<0>	20 22 73	
66 22 20 7 73	MEM_A_BA<1>	TRUE	MEM_A_BA<1>	7 20 22 66 73	
7	=MEM_A_BA<2>	TRUE	MEM_A_BA<2>	20 22 73	

MAKE_BASE

66 22 7	MEM_B_ODT_CPU0	TRUE	MEM_B_ODT_CPU0	7 22 66	
66 22 21 7 73	MEM_B_RAS_L	TRUE	MEM_B_RAS_L	7 21 22 66 73	
66 22 21 7 73	MEM_B_WE_L	TRUE	MEM_B_WE_L	7 21 22 66 73	
66 22 21 7 73	MEM_B_CAS_L	TRUE	MEM_B_CAS_L	7 21 22 66 73	
7	=MEM_B_BA<0>	TRUE	MEM_B_BA<0>	21 22 73	
66 22 21 7 73	MEM_B_BA<1>	TRUE	MEM_B_BA<1>	7 21 22 66 73	
7	=MEM_B_BA<2>	TRUE	MEM_B_BA<2>	21 22 73	

MAKE_BASE

66 22 6	MEM_RESET_HSW_L	TRUE	MEM_RESET_HSW_L	6 22 66	

UNUSED MEMORY SIGNALS

NO_TEST

66 7	NC_MEM_A_CLKN<1>	TRUE	NC_MEM_A_CLKN<1>	7 66	
66 7	NC_MEM_A_CLKP<1>	MAKE_BASE=TRUE TRUE	NC_MEM_A_CLKP<1>	7 66	
7	MEM_A_CKE<2>	MAKE_BASE=TRUE TRUE	NC_MEM_A_CKE<2>		
66 7	NC_MEM_A_CKE<3>	MAKE_BASE=TRUE TRUE	NC_MEM_A_CKE<3>	7 66	
66 7	NC_MEM_B_CLKN<1>	MAKE_BASE=TRUE TRUE	NC_MEM_B_CLKN<1>	7 66	
66 7	NC_MEM_B_CLKP<1>	MAKE_BASE=TRUE TRUE	NC_MEM_B_CLKP<1>	7 66	
7	MEM_B_CKE<2>	MAKE_BASE=TRUE TRUE	NC_MEM_B_CKE<2>		
66 7	NC_MEM_B_CKE<3>	MAKE_BASE=TRUE TRUE MAKE_BASE=TRUE	NC_MEM_B_CKE<3>	7 66	

HDMI VS TBT

MAKE_BASE

5	=DP_TBTSNK1_ML_C_P<0>	TRUE	DP_HDMI_TBT_ML_P<0>	64 74	
5	=DP_TBTSNK1_ML_C_N<0>	TRUE	DP_HDMI_TBT_ML_N<0>	64 74	
5	=DP_TBTSNK1_ML_C_P<1>	TRUE	DP_HDMI_TBT_ML_P<1>	64 74	
5	=DP_TBTSNK1_ML_C_N<1>	TRUE	DP_HDMI_TBT_ML_N<1>	64 74	
5	=DP_TBTSNK1_ML_C_P<2>	TRUE	DP_HDMI_TBT_ML_P<2>	64 74	
5	=DP_TBTSNK1_ML_C_N<2>	TRUE	DP_HDMI_TBT_ML_N<2>	64 74	
5	=DP_TBTSNK1_ML_C_P<3>	TRUE	DP_HDMI_TBT_ML_P<3>	64 74	
5	=DP_TBTSNK1_ML_C_N<3>	TRUE	DP_HDMI_TBT_ML_N<3>	64 74	
74 66 64 13	DP_HDMI_TBT_AUX_P	TRUE	DP_HDMI_TBT_AUX_P	13 64 66 74	
74 66 64 13	DP_HDMI_TBT_AUX_N	TRUE	DP_HDMI_TBT_AUX_N	13 64 66 74	
66 64 13	DP_HDMI_TBT_DDC_CLK	TRUE	DP_HDMI_TBT_DDC_CLK	13 64 66	
66 64 13	DP_HDMI_TBT_DDC_DATA	TRUE	DP_HDMI_TBT_DDC_DATA	13 64 66	
66 64 13	DPMUX_HPD_OUT	TRUE	DPMUX_HPD_OUT	13 64 66	

66 64 23 15	HDMITBTMUX_SEL_TBT MAKE_BASE=TRUE	HDMITBTMUX_SEL_TBT	15 23 64 66	
		HDMITBTMUX_SEL_TBT	15 23 64 66	
66 64 13	HDMITBTMUX_LATCH	HDMITBTMUX_LATCH MAKE_BASE=TRUE	13 64 66	

EPD PANEL

MAKE_BASE

68 66 62 58	I2C_BKLT_SCL	TRUE	I2C_BKLT_SCL	58 62 66 68	
68 66 62 58	I2C_BKLT_SDA	TRUE	I2C_BKLT_SDA	58 62 66 68	

UNUSED SIGNALS

MAKE_BASE

66 12	NC_PCIE_CLK100M_FWP	TRUE NO_TEST=TRUE	NC_PCIE_CLK100M_FWP	12 66	
66 12	NC_PCIE_CLK100M_FWN	TRUE NO_TEST=TRUE	NC_PCIE_CLK100M_FWN	12 66	
66 14	NC_PCIE_FW_D2RP	TRUE NO_TEST=TRUE	NC_PCIE_FW_D2RP	14 66	
66 14	NC_PCIE_FW_D2RN	TRUE NO_TEST=TRUE	NC_PCIE_FW_D2RN	14 66	
66 14	NC_PCIE_FW_R2D_CP	TRUE NO_TEST=TRUE	NC_PCIE_FW_R2D_CP	14 66	
66 14	NC_PCIE_FW_R2D_CN	TRUE NO_TEST=TRUE	NC_PCIE_FW_R2D_CN	14 66	
66 12	NC_PCIE_CLK100M_ENETSDP	TRUE NO_TEST=TRUE	NC_PCIE_CLK100M_ENETSDP	12 66	
66 12	NC_PCIE_CLK100M_ENETSDN	TRUE NO_TEST=TRUE	NC_PCIE_CLK100M_ENETSDN	12 66	
71 66 14	NC_USB_IRP	TRUE NO_TEST=TRUE	NC_USB_IRP	14 66 71	
71 66 14	NC_USB_IRN	TRUE NO_TEST=TRUE	NC_USB_IRN	14 66 71	
71 66 14	NC_USB_CAMERAP	TRUE NO_TEST=TRUE	NC_USB_CAMERAP	14 66 71	
71 66 14	NC_USB_CAMERAN	TRUE NO_TEST=TRUE	NC_USB_CAMERAN	14 66 71	
71 66 14	NC_USB_SDP	TRUE NO_TEST=TRUE	NC_USB_SDP	14 66 71	
71 66 14	NC_USB_SDN	TRUE NO_TEST=TRUE	NC_USB_SDN	14 66 71	
66 12	NC_HDA_SDIN1	TRUE NO_TEST=TRUE	NC_HDA_SDIN1	12 66	
66 13	NC_PCI_PME_L	TRUE NO_TEST=TRUE	NC_PCI_PME_L	13 66	
66 14	NC_CLINK_CLK	TRUE NO_TEST=TRUE	NC_CLINK_CLK	14 66	
66 14	NC_CLINK_DATA	TRUE NO_TEST=TRUE	NC_CLINK_DATA	14 66	
66 14	NC_CLINK_RESET_L	TRUE NO_TEST=TRUE	NC_CLINK_RESET_L	14 66	

66 45	NC_SMC_TRST_L	TRUE NO_TEST=TRUE	NC_SMC_TRST_L	45 66	
66 45	NC_SMC_MD1	TRUE NO_TEST=TRUE	NC_SMC_MD1	45 66	

GND
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.2MM
VOLTAGE=0V

Digital Ground

65 63 62 60 57 56 55 46 33 32 68 PP5V_S4

XWA202
SM
1 2 PP5V_S0_AUDIO_AMP_L 48
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.2MM
VOLTAGE=5V

XWA203
SM
1 2 PP5V_S0_AUDIO_AMP_R 48
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.2MM
VOLTAGE=5V

SYNC_MASTER=MASTER SYNC_DATE=MASTER

PAGE TITLE
Signal Aliases

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D
REVISION <E4LABEL>
BRANCH <BRANCH>
PAGE 102 OF 120
SHEET 66 OF 78

Memory Bit/Byte Swizzle

MAKE_BASE

73 68 7	TRUE	MEM_A_DQ<0>	=MEM_A_DQ<60>	20
73 68 7	TRUE	MEM_A_DQ<1>	=MEM_A_DQ<56>	20
73 68 7	TRUE	MEM_A_DQ<2>	=MEM_A_DQ<57>	20
73 68 7	TRUE	MEM_A_DQ<3>	=MEM_A_DQ<61>	20
73 68 7	TRUE	MEM_A_DQ<4>	=MEM_A_DQ<62>	20
73 68 7	TRUE	MEM_A_DQ<5>	=MEM_A_DQ<58>	20
73 68 7	TRUE	MEM_A_DQ<6>	=MEM_A_DQ<59>	20
73 68 7	TRUE	MEM_A_DQ<7>	=MEM_A_DQ<63>	20
73 68 7	TRUE	MEM_A_DQ<8>	=MEM_A_DQ<44>	20
73 68 7	TRUE	MEM_A_DQ<9>	=MEM_A_DQ<40>	20
73 68 7	TRUE	MEM_A_DQ<10>	=MEM_A_DQ<45>	20
73 68 7	TRUE	MEM_A_DQ<11>	=MEM_A_DQ<47>	20
73 68 7	TRUE	MEM_A_DQ<12>	=MEM_A_DQ<46>	20
73 68 7	TRUE	MEM_A_DQ<13>	=MEM_A_DQ<42>	20
73 68 7	TRUE	MEM_A_DQ<14>	=MEM_A_DQ<41>	20
73 68 7	TRUE	MEM_A_DQ<15>	=MEM_A_DQ<43>	20
73 68 7	TRUE	MEM_A_DQ<16>	=MEM_A_DQ<20>	20
73 68 7	TRUE	MEM_A_DQ<17>	=MEM_A_DQ<18>	20
73 68 7	TRUE	MEM_A_DQ<18>	=MEM_A_DQ<23>	20
73 68 7	TRUE	MEM_A_DQ<19>	=MEM_A_DQ<19>	20
73 68 7	TRUE	MEM_A_DQ<20>	=MEM_A_DQ<17>	20
73 68 7	TRUE	MEM_A_DQ<21>	=MEM_A_DQ<21>	20
73 68 7	TRUE	MEM_A_DQ<22>	=MEM_A_DQ<22>	20
73 68 7	TRUE	MEM_A_DQ<23>	=MEM_A_DQ<16>	20
73 68 7	TRUE	MEM_A_DQ<24>	=MEM_A_DQ<38>	20
73 68 7	TRUE	MEM_A_DQ<25>	=MEM_A_DQ<36>	20
73 68 7	TRUE	MEM_A_DQ<26>	=MEM_A_DQ<37>	20
73 68 7	TRUE	MEM_A_DQ<27>	=MEM_A_DQ<39>	20
73 68 7	TRUE	MEM_A_DQ<28>	=MEM_A_DQ<34>	20
73 68 7	TRUE	MEM_A_DQ<29>	=MEM_A_DQ<32>	20
73 68 7	TRUE	MEM_A_DQ<30>	=MEM_A_DQ<35>	20
73 68 7	TRUE	MEM_A_DQ<31>	=MEM_A_DQ<33>	20
73 68 67 20 7	TRUE	MEM_A_DQ<32>	MEM_A_DQ<32>	7 20 67 68 73
73 68 7	TRUE	MEM_A_DQ<33>	=MEM_A_DQ<24>	20
73 68 7	TRUE	MEM_A_DQ<34>	=MEM_A_DQ<25>	20
73 68 7	TRUE	MEM_A_DQ<35>	=MEM_A_DQ<29>	20
73 68 7	TRUE	MEM_A_DQ<36>	=MEM_A_DQ<30>	20
73 68 7	TRUE	MEM_A_DQ<37>	=MEM_A_DQ<26>	20
73 68 7	TRUE	MEM_A_DQ<38>	=MEM_A_DQ<31>	20
73 68 7	TRUE	MEM_A_DQ<39>	=MEM_A_DQ<27>	20
73 68 7	TRUE	MEM_A_DQ<40>	=MEM_A_DQ<12>	20
73 68 7	TRUE	MEM_A_DQ<41>	=MEM_A_DQ<8>	20
73 68 7	TRUE	MEM_A_DQ<42>	=MEM_A_DQ<11>	20
73 68 7	TRUE	MEM_A_DQ<43>	=MEM_A_DQ<15>	20
73 68 7	TRUE	MEM_A_DQ<44>	=MEM_A_DQ<14>	20
73 68 7	TRUE	MEM_A_DQ<45>	=MEM_A_DQ<10>	20
73 68 7	TRUE	MEM_A_DQ<46>	=MEM_A_DQ<9>	20
73 68 7	TRUE	MEM_A_DQ<47>	=MEM_A_DQ<13>	20
73 68 7	TRUE	MEM_A_DQ<48>	=MEM_A_DQ<53>	20
73 68 7	TRUE	MEM_A_DQ<49>	=MEM_A_DQ<55>	20
73 68 7	TRUE	MEM_A_DQ<50>	=MEM_A_DQ<50>	20
73 68 7	TRUE	MEM_A_DQ<51>	=MEM_A_DQ<54>	20
73 68 7	TRUE	MEM_A_DQ<52>	=MEM_A_DQ<52>	20
73 68 7	TRUE	MEM_A_DQ<53>	=MEM_A_DQ<48>	20
73 68 7	TRUE	MEM_A_DQ<54>	=MEM_A_DQ<51>	20
73 68 7	TRUE	MEM_A_DQ<55>	=MEM_A_DQ<49>	20
73 68 7	TRUE	MEM_A_DQ<56>	=MEM_A_DQ<2>	20
73 68 7	TRUE	MEM_A_DQ<57>	=MEM_A_DQ<1>	20
73 68 7	TRUE	MEM_A_DQ<58>	=MEM_A_DQ<6>	20
73 68 7	TRUE	MEM_A_DQ<59>	=MEM_A_DQ<4>	20
73 68 7	TRUE	MEM_A_DQ<60>	=MEM_A_DQ<0>	20
73 68 7	TRUE	MEM_A_DQ<61>	=MEM_A_DQ<3>	20
73 68 7	TRUE	MEM_A_DQ<62>	=MEM_A_DQ<7>	20
73 68 7	TRUE	MEM_A_DQ<63>	=MEM_A_DQ<5>	20
73 7	TRUE	MEM_A_DQS_P<0>	=MEM_A_DQS_P<7>	20
73 7	TRUE	MEM_A_DQS_N<0>	=MEM_A_DQS_N<7>	20
73 7	TRUE	MEM_A_DQS_P<1>	=MEM_A_DQS_P<5>	20
73 7	TRUE	MEM_A_DQS_N<1>	=MEM_A_DQS_N<5>	20
73 7	TRUE	MEM_A_DQS_P<2>	=MEM_A_DQS_P<2>	20
73 7	TRUE	MEM_A_DQS_N<2>	=MEM_A_DQS_N<2>	20
73 7	TRUE	MEM_A_DQS_P<3>	=MEM_A_DQS_P<4>	20
73 7	TRUE	MEM_A_DQS_N<3>	=MEM_A_DQS_N<4>	20
73 7	TRUE	MEM_A_DQS_P<4>	=MEM_A_DQS_P<3>	20
73 7	TRUE	MEM_A_DQS_N<4>	=MEM_A_DQS_N<3>	20
73 7	TRUE	MEM_A_DQS_P<5>	=MEM_A_DQS_P<1>	20
73 7	TRUE	MEM_A_DQS_N<5>	=MEM_A_DQS_N<1>	20
73 67 20 7	TRUE	MEM_A_DQS_P<6>	MEM_A_DQS_P<6>	7 20 67 73
73 67 20 7	TRUE	MEM_A_DQS_N<6>	MEM_A_DQS_N<6>	7 20 67 73
73 7	TRUE	MEM_A_DQS_P<7>	=MEM_A_DQS_P<0>	20
73 7	TRUE	MEM_A_DQS_N<7>	=MEM_A_DQS_N<0>	20

MAKE_BASE

73 68 7	TRUE	MEM_B_DQ<0>	=MEM_B_DQ<8>	21
73 68 7	TRUE	MEM_B_DQ<1>	=MEM_B_DQ<14>	21
73 68 7	TRUE	MEM_B_DQ<2>	=MEM_B_DQ<11>	21
73 68 7	TRUE	MEM_B_DQ<3>	=MEM_B_DQ<9>	21
73 68 7	TRUE	MEM_B_DQ<4>	=MEM_B_DQ<12>	21
73 68 7	TRUE	MEM_B_DQ<5>	=MEM_B_DQ<10>	21
73 68 7	TRUE	MEM_B_DQ<6>	=MEM_B_DQ<15>	21
73 68 7	TRUE	MEM_B_DQ<7>	=MEM_B_DQ<13>	21
73 68 7	TRUE	MEM_B_DQ<8>	=MEM_B_DQ<24>	21
73 68 7	TRUE	MEM_B_DQ<9>	=MEM_B_DQ<30>	21
73 68 7	TRUE	MEM_B_DQ<10>	=MEM_B_DQ<29>	21
73 68 7	TRUE	MEM_B_DQ<11>	=MEM_B_DQ<27>	21
73 68 7	TRUE	MEM_B_DQ<12>	=MEM_B_DQ<28>	21
73 68 7	TRUE	MEM_B_DQ<13>	=MEM_B_DQ<26>	21
73 68 7	TRUE	MEM_B_DQ<14>	=MEM_B_DQ<25>	21
73 68 7	TRUE	MEM_B_DQ<15>	=MEM_B_DQ<31>	21
73 68 7	TRUE	MEM_B_DQ<16>	=MEM_B_DQ<5>	21
73 68 7	TRUE	MEM_B_DQ<17>	=MEM_B_DQ<1>	21
73 68 7	TRUE	MEM_B_DQ<18>	=MEM_B_DQ<6>	21
73 68 7	TRUE	MEM_B_DQ<19>	=MEM_B_DQ<3>	21
73 68 7	TRUE	MEM_B_DQ<20>	=MEM_B_DQ<4>	21
73 68 7	TRUE	MEM_B_DQ<21>	=MEM_B_DQ<7>	21
73 68 7	TRUE	MEM_B_DQ<22>	=MEM_B_DQ<0>	21
73 68 7	TRUE	MEM_B_DQ<23>	=MEM_B_DQ<2>	21
73 68 7	TRUE	MEM_B_DQ<24>	=MEM_B_DQ<21>	21
73 68 7	TRUE	MEM_B_DQ<25>	=MEM_B_DQ<17>	21
73 68 7	TRUE	MEM_B_DQ<26>	=MEM_B_DQ<20>	21
73 68 7	TRUE	MEM_B_DQ<27>	=MEM_B_DQ<22>	21
73 68 7	TRUE	MEM_B_DQ<28>	=MEM_B_DQ<23>	21
73 68 7	TRUE	MEM_B_DQ<29>	=MEM_B_DQ<19>	21
73 68 7	TRUE	MEM_B_DQ<30>	=MEM_B_DQ<18>	21
73 68 7	TRUE	MEM_B_DQ<31>	=MEM_B_DQ<16>	21
73 68 67 21 7	TRUE	MEM_B_DQ<32>	MEM_B_DQ<32>	7 21 67 68 73
73 68 7	TRUE	MEM_B_DQ<33>	=MEM_B_DQ<40>	21
73 68 7	TRUE	MEM_B_DQ<34>	=MEM_B_DQ<45>	21
73 68 7	TRUE	MEM_B_DQ<35>	=MEM_B_DQ<43>	21
73 68 7	TRUE	MEM_B_DQ<36>	=MEM_B_DQ<46>	21
73 68 7	TRUE	MEM_B_DQ<37>	=MEM_B_DQ<42>	21
73 68 7	TRUE	MEM_B_DQ<38>	=MEM_B_DQ<47>	21
73 68 7	TRUE	MEM_B_DQ<39>	=MEM_B_DQ<41>	21
73 68 7	TRUE	MEM_B_DQ<40>	=MEM_B_DQ<60>	21
73 68 7	TRUE	MEM_B_DQ<41>	=MEM_B_DQ<56>	21
73 68 7	TRUE	MEM_B_DQ<42>	=MEM_B_DQ<63>	21
73 68 7	TRUE	MEM_B_DQ<43>	=MEM_B_DQ<61>	21
73 68 7	TRUE	MEM_B_DQ<44>	=MEM_B_DQ<62>	21
73 68 7	TRUE	MEM_B_DQ<45>	=MEM_B_DQ<58>	21
73 68 7	TRUE	MEM_B_DQ<46>	=MEM_B_DQ<59>	21
73 68 7	TRUE	MEM_B_DQ<47>	=MEM_B_DQ<57>	21
73 68 7	TRUE	MEM_B_DQ<48>	=MEM_B_DQ<38>	21
73 68 7	TRUE	MEM_B_DQ<49>	=MEM_B_DQ<37>	21
73 68 7	TRUE	MEM_B_DQ<50>	=MEM_B_DQ<32>	21
73 68 7	TRUE	MEM_B_DQ<51>	=MEM_B_DQ<33>	21
73 68 7	TRUE	MEM_B_DQ<52>	=MEM_B_DQ<35>	21
73 68 7	TRUE	MEM_B_DQ<53>	=MEM_B_DQ<36>	21
73 68 7	TRUE	MEM_B_DQ<54>	=MEM_B_DQ<34>	21
73 68 7	TRUE	MEM_B_DQ<55>	=MEM_B_DQ<39>	21
73 68 7	TRUE	MEM_B_DQ<56>	=MEM_B_DQ<51>	21
73 68 7	TRUE	MEM_B_DQ<57>	=MEM_B_DQ<53>	21
73 68 7	TRUE	MEM_B_DQ<58>	=MEM_B_DQ<48>	21
73 68 7	TRUE	MEM_B_DQ<59>	=MEM_B_DQ<55>	21
73 68 7	TRUE	MEM_B_DQ<60>	=MEM_B_DQ<50>	21
73 68 7	TRUE	MEM_B_DQ<61>	=MEM_B_DQ<49>	21
73 68 7	TRUE	MEM_B_DQ<62>	=MEM_B_DQ<54>	21
73 68 7	TRUE	MEM_B_DQ<63>	=MEM_B_DQ<52>	21
73 7	TRUE	MEM_B_DQS_P<0>	=MEM_B_DQS_P<1>	21
73 7	TRUE	MEM_B_DQS_N<0>	=MEM_B_DQS_N<1>	21
73 7	TRUE	MEM_B_DQS_P<1>	=MEM_B_DQS_P<3>	21
73 7	TRUE	MEM_B_DQS_N<1>	=MEM_B_DQS_N<3>	21
73 7	TRUE	MEM_B_DQS_P<2>	=MEM_B_DQS_P<0>	21
73 7	TRUE	MEM_B_DQS_N<2>	=MEM_B_DQS_N<0>	21
73 7	TRUE	MEM_B_DQS_P<3>	=MEM_B_DQS_P<2>	21
73 7	TRUE	MEM_B_DQS_N<3>	=MEM_B_DQS_N<2>	21
73 7	TRUE	MEM_B_DQS_P<4>	=MEM_B_DQS_P<5>	21
73 7	TRUE	MEM_B_DQS_N<4>	=MEM_B_DQS_N<5>	21
73 7	TRUE	MEM_B_DQS_P<5>	=MEM_B_DQS_P<7>	21
73 7	TRUE	MEM_B_DQS_N<5>	=MEM_B_DQS_N<7>	21
73 67 21 7	TRUE	MEM_B_DQS_P<6>	MEM_B_DQS_P<6>	7 21 67 73
73 67 21 7	TRUE	MEM_B_DQS_N<6>	MEM_B_DQS_N<6>	7 21 67 73
73 7	TRUE	MEM_B_DQS_P<7>	=MEM_B_DQS_P<6>	21
73 7	TRUE	MEM_B_DQS_N<7>	=MEM_B_DQS_N<6>	21

SYNC_MASTER=J44 SYNC_DATE=01/03/2013

PAGE TITLE

Memory Bit/Byte Swizzle

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

REVISION <E4LABEL>

BRANCH <BRANCH>

PAGE 103 OF 120

SHEET 67 OF 78

Functional Test Points

J6050 (LEFT FAN CONN)

FUNC_TEST
- TRUE — PP5V_S0 — 3 TPs per Fan
- TRUE — FAN_LT_PWM
- TRUE — FAN_LT_TACH

J4002 (ALS/CAMERA CONN)
- TRUE — SMBUS_SMC_1_S0_SCL — 14 32 36 39 43 72 76
- TRUE — SMBUS_SMC_1_S0_SDA — 14 32 36 39 43 72 76
- TRUE — PP5V_S3RS0_ALSCAM_F — 32
- TRUE — MIPI_CLK_CONN_N — 32 75
- TRUE — MIPI_CLK_CONN_P — 32 75
- TRUE — CAM_SENSOR_WAKE_L_CONN — 32
- TRUE — MIPI_DATA_CONN_N — 32 75
- TRUE — MIPI_DATA_CONN_P — 32 75
- TRUE — I2C_CAM_SCK — 31 32
- TRUE — I2C_CAM_SDA — 31 32

J9500 (RIO POWER PINS)
- TRUE — PP3V3_S4 — 18 29 34 37 38 42 60 63 64 65 68
- TRUE — PP5V_S4 — 32 33 46 55 56 57 60 62 63 65 66 68
- TRUE — PP1V5_S0 — 8 47 59 60 61 63 65

TRUE — GND

U0500 CHARZ TPS

70 23 14	PCIE_TBT_D2R_P<0>	P2MM SM	PPA400
70 23 14	PCIE_TBT_D2R_N<0>	P2MM SM	PPA401
70 68 23 32	PCIE_CLK100M_TBT_P	P2MM SM	PPA423
	PCIE_CLK100M_TBT_N	P2MM SM	PPA424
70 32 14	PCIE_CAMERA_D2R_P	P2MM SM	PPA402
70 32 14	PCIE_CAMERA_D2R_N	P2MM SM	PPA403
70 68 30 12	PCIE_SSD_D2R_P<0>	P2MM SM	PPA404
70 68 30 12	PCIE_SSD_D2R_N<0>	P2MM SM	PPA405
70 68 63 14	PCIE_AP_D2R_P	P2MM SM	PPA410
70 68 63 14	PCIE_AP_D2R_N	P2MM SM	PPA411
71 63 14	USB3RPCIE_SD_D2R_P	P2MM SM	PPA420
71 63 14	USB3RPCIE_SD_D2R_N	P2MM SM	PPA421
72 47 12	HDA_SDIN0	1 SM	PPA408
		PLACE_NEAR=U0500.AY10:6MM	
75 32 31	MIPI_CLK_N	P2MM SM	PPA441
	MIPI_CLK_P	P2MM SM	PPA442
75 32 31	MIPI_DATA_N	P2MM SM	PPA443
	MIPI_DATA_P	P2MM SM	PPA444

U5000 CHARZ TPS

72 36 17	LPC_CLK24M_SMC	P2MM SM	PPA419

J4813 (KEY BOARD CONN)
- TRUE — PP3V3_S4 — 18 29 34 37 38 42 60 63 64 65 68
- TRUE — PP3V42_G3H — 17 30 33 34 36 37 38 39 45 51 52 61 65 68
- TRUE — WS_KBD1 — 34
- TRUE — WS_KBD2 — 34
- TRUE — WS_KBD3 — 34
- TRUE — WS_KBD4 — 34
- TRUE — WS_KBD5 — 34
- TRUE — WS_KBD6 — 34
- TRUE — WS_KBD7 — 34
- TRUE — WS_KBD8 — 34
- TRUE — WS_KBD9 — 34
- TRUE — WS_KBD10 — 34
- TRUE — WS_KBD11 — 34
- TRUE — WS_KBD12 — 34
- TRUE — WS_KBD13 — 34
- TRUE — WS_KBD14 — 34
- TRUE — WS_KBD15_CAP — 34
- TRUE — WS_KBD16_NUM — 34
- TRUE — WS_KBD17 — 34
- TRUE — WS_KBD18 — 34
- TRUE — WS_KBD19 — 34
- TRUE — WS_KBD20 — 34
- TRUE — WS_KBD21 — 34
- TRUE — WS_KBD22 — 34
- TRUE — WS_KBD23 — 34
- TRUE — WS_KBD_ONOFF_L — 34
- TRUE — WS_LEFT_SHIFT_KBD — 34
- TRUE — WS_LEFT_OPTION_KBD — 34
- TRUE — WS_CONTROL_KBD — 34

J4800 (TPAD CONN)
- TRUE — SMBUS_SMC_2_S3_SDA — 34 36 39 76
- TRUE — SMBUS_SMC_2_S3_SCL — 34 36 39 76
- TRUE — PP3V3_TPAD_CONN — 34
- TRUE — PP5V_S4_CUMULUS — 34
- TRUE — Z2_CLKIN — 34
- TRUE — PSOC_SCLK — 34
- TRUE — PSOC_MOSI — 34
- TRUE — Z2_SCLK — 34
- TRUE — PSOC_MISO — 34
- TRUE — Z2_MISO — 34
- TRUE — Z2_MOSI — 34
- TRUE — PSOC_F_CS_L — 34
- TRUE — Z2_CS_L — 34
- TRUE — Z2_KEY_ACT_L — 34
- TRUE — PICKB_L — 34
- TRUE — Z2_HOST_INTN — 34

J7000 (DC POWER CONN)
- TRUE — TDM_ONEWIRE_MPM
- TRUE — ADAPTER_SENSE — 51
- TRUE — PP18V5_DCIN_FUSE — 51

TRUE — GND

- TRUE — PM_CLKRUN_L — 13 36 45 68
- TRUE — PM_SYSRST_L — 13 17 36 72
- TRUE — SMC_ONOFF_L — 34 36 37

J6100 (LPC + SPI CONN)
- TRUE — PP3V42_G3H — 65 68
- TRUE — PP5V_S0 — 16 17 32 41 44 45 53 54 58 60 61 65 68
- TRUE — LPC_CLK24M_LPCPLUS — 17 45 72
- TRUE — LPC_AD<0> — 14 36 45 72
- TRUE — LPC_AD<2> — 14 36 45 72
- TRUE — LPC_AD<1> — 14 36 45 72
- TRUE — LPC_AD<3> — 14 36 45 72
- TRUE — XDP_LPCPLUS_GPIO — 15 16 45
- TRUE — LPCPLUS_RESET_L — 18 45
- TRUE — SMC_TDO — 36 37 45
- TRUE — SMC_TX_L — 36 37 45
- TRUE — LPC_FRAME_L — 14 36 45 72
- TRUE — SPIROM_USE_MLB — 15 45 72
- TRUE — PM_CLKRUN_L — 13 36 45 68
- TRUE — LPC_SERIRQ — 15 36 45
- TRUE — LPC_PWRDWN_L — 13 36 45
- TRUE — SMC_TDI — 36 37 45
- TRUE — SMC_TCK — 36 37 45
- TRUE — SMC_RESET_L — 36 37 38 45 52
- TRUE — SMC_ROMBOOT — 37 45
- TRUE — SMC_RX_L — 36 37 45
- TRUE — SMC_TMS — 36 37 45

J6601 (AUDIO 2-MIKE CONN)
- TRUE — SMBUS_PCH_CLK — 14 16 19 39 63 72
- TRUE — SMBUS_PCH_DATA — 14 16 19 39 63 72
- TRUE — DMIC_SDA3 — 47 50
- TRUE — DMIC_SDA2 — 50
- TRUE — DMIC_CLK3 — 47 50

J6602 (AUDIO LEFT SPEAKER CONN)
- TRUE — SPKRCONN_L_OUT_P — 48 50 77
- TRUE — SPKRCONN_L_OUT_N — 48 50 77
- TRUE — SPKRCONN_L_ID — 47 50
- TRUE — SPKRCONN_SL_OUT_P — 48 50 77
- TRUE — SPKRCONN_SL_OUT_N — 48 50 77

J6603 (AUDIO RIGHT SPEAKER CONN)
- TRUE — SPKRCONN_R_OUT_P — 48 50 77
- TRUE — SPKRCONN_R_OUT_N — 48 50 77
- TRUE — SPKRCONN_R_ID — 47 50
- TRUE — SPKRCONN_SR_OUT_P — 48 50 77
- TRUE — SPKRCONN_SR_OUT_N — 48 50 77
- TRUE — GND

J7715 (KBD BACKLIGHT CONN)
- TRUE — PPVOUT_S0_KBDBKLT — 35 58
- TRUE — KBDLED_CATHODE1 — 35 58
- TRUE — KBDLED_CATHODE2 — 35 58

J8300 (EDP CONN)
- TRUE — PP5VR3V3_SW_LCD — 62
- TRUE — PPVOUT_S0_LCDBKLT — 58 62 — 2 TP needed
- TRUE — I2C_BKLT_SCL — 58 62 66
- TRUE — I2C_BKLT_SDA — 58 62 66
- TRUE — LCD_HPD_CONN — 62
- TRUE — LCD_IRQ_L — 15 62
- TRUE — EDP_BKLT_PWM — 13 62
- TRUE — SMBUS_SMC_0_S0_SCL — 36 39 62 76
- TRUE — SMBUS_SMC_0_S0_SDA — 36 39 62 76
- TRUE — EDP_PANEL_PWR_OR_PSR_EN — 62
- TRUE — DP_INT_AUX_P — 62 74
- TRUE — DP_INT_AUX_N — 62 74
- TRUE — DP_INT_ML_P<0> — 62 74
- TRUE — DP_INT_ML_N<0> — 62 74
- TRUE — DP_INT_ML_P<1> — 62 74
- TRUE — DP_INT_ML_N<1> — 62 74
- TRUE — DP_INT_ML_P<2> — 62 74
- TRUE — DP_INT_ML_N<2> — 62 74
- TRUE — DP_INT_ML_P<3> — 62 74
- TRUE — DP_INT_ML_N<3> — 62 74

J7050 (MAIN BATT CONN)
- TRUE — PPVBAT_G3H_CONN — 51 52
- TRUE — SMBUS_SMC_5_G3_SCL — 36 39 51 52 76
- TRUE — SMBUS_SMC_5_G3_SDA — 36 39 51 52 76
- TRUE — SYS_DETECT_L — 51

J6601 (2 MIC CONN)
- TRUE — CON_DMIC_PWR
- TRUE — CON_DMIC_SDA1
- TRUE — CON_DMIC_CLK

- TRUE — PCH_VSS_NCTF<19> — 68
- TRUE — PCH_VSS_NCTF<19> — 68

J4600 (LEFT USB CONN)
- TRUE — PP5V_S3_LTUSB_A_F — 33
- TRUE — USB_LT1_N — 71
- TRUE — USB_LT1_P — 71

FUNC_TEST
- TRUE — GND
- TRUE — GND
- TRUE — GND — 6 TPs

POWER RAILS

FUNC_TEST
- TRUE — PM_SLP_S3_L — 13 17 18 36 61 63
- TRUE — PP0V675_S0_DDRVTT — 22 55 65 73
- TRUE — PP1V05_S0 — 6 8 11 15 16 17 37 53 57 60 61 65

TRUE — GND — 4 TPs

- TRUE — PP3V3_S0 — 61 62 64 65 77 — 6 15 16 17 18 24 28 30 37 38 39 40 41 42 43 44 46 47 58
- TRUE — PP3V3_S3 — 15 18 19 39 42 60 65
- TRUE — PP3V3_S5 — 8 11 13 15 16 17 18 26 27 29 56 59 60 61 65 77
- TRUE — PP3V3_S5_AVREF_SMC — 36 37
- TRUE — PP3V42_G3H — 17 30 33 34 36 37 38 39 45 51 52 61 65 68
- TRUE — PP5V_S0 — 16 17 32 41 44 45 53 54 58 60 61 65 68
- TRUE — PP5V_S4 — 32 33 46 55 56 57 60 62 63 65 66 68
- TRUE — PP5V_S5 — 34 56 65
- TRUE — PPBUS_G3H — 25 40 51 52 58 65
- TRUE — PPDCIN_G3H — 51 52 65
- TRUE — PPVCC_S0_CPU — 8 10 42 54 65
- TRUE — PPVTTDDR_S3 — 55 65 68 73 — NC_PM_SLP_A_L — TRUE — MAKE_BASE=TRUE — NC_PM_SLP_A_L — 13 68

NO_TESTs

- TBTBPWRSW_ISET_V3P3 — 27 — TRUE
- TBTBPWRSW_ISET_S0_R — 27 — TRUE
- TBTBPWRSW_ISET_S3 — 27 — TRUE
- TBTAPWRSW_ISET_V3P3 — 26 — TRUE
- TBTAPWRSW_ISET_S0 — 26 — TRUE
- TBTAPWRSW_ISET_S3 — 26 — TRUE
- TBTAPWRSW_ISET_S3_R — 26 — TRUE
- TBT_A_R2D_C_P<1..0> — 23 26 74 — TRUE
- TBT_A_R2D_C_N<1..0> — 23 26 74 — TRUE
- TBT_A_R2D_P<1..0> — 26 74 — TRUE
- TBT_A_R2D_N<1..0> — 26 74 — TRUE
- TBT_A_D2R_C_P<1> — 26 74 — TRUE
- TBT_A_D2R_C_N<1> — 26 74 — TRUE
- TBT_A_D2R_C_P<0> — 26 74 — TRUE
- TBT_A_D2R_C_N<0> — 26 74 — TRUE
- TBT_A_D2R_P<1> — 23 26 74 — TRUE
- TBT_A_D2R_N<1> — 23 26 74 — TRUE
- TBT_A_D2R_P<0> — 23 26 74 — TRUE
- TBT_A_D2R_N<0> — 23 26 74 — TRUE
- TBT_B_R2D_C_P<1..0> — 23 27 74 — TRUE
- TBT_B_R2D_C_N<1..0> — 23 27 74 — TRUE
- TBT_B_R2D_P<1..0> — 27 74 — TRUE
- TBT_B_R2D_N<1..0> — 27 74 — TRUE
- TBT_B_D2R_C_P<0> — 27 74 — TRUE
- TBT_B_D2R_C_N<0> — 27 74 — TRUE
- TBT_B_D2R_C_P<1> — 27 74 — TRUE
- TBT_B_D2R_C_N<1> — 27 74 — TRUE
- TBT_B_D2R_P<0> — 23 27 74 — TRUE
- TBT_B_D2R_N<0> — 23 27 74 — TRUE
- TBT_B_D2R_P<1> — 23 27 74 — TRUE
- TBT_B_D2R_N<1> — 23 27 74 — TRUE
- PCIE_AP_D2R_P — 14 63 68 70 — TRUE
- PCIE_AP_D2R_N — 14 63 68 70 — TRUE
- PCIE_AP_R2D_P — 63 70 — TRUE
- PCIE_AP_R2D_N — 63 70 — TRUE

- MEM_A_DQ<63..0> — 7 20 67 73 — TRUE
- PPVTTDDR_S3 — 55 65 68 73 — TRUE
- MEM_B_DQ<63..0> — 7 21 67 73 — TRUE

- HDMI_IG_CLK_C_P — 63 64 74 — TRUE
- HDMI_IG_CLK_C_N — 63 64 74 — TRUE
- HDMI_IG_DATA_C_P<2..0> — 63 64 74 — TRUE
- HDMI_IG_DATA_C_N<2..0> — 63 64 74 — TRUE

68	NC_XDP_PCH_HOOK4	TRUE MAKE_BASE=TRUE	NC_XDP_PCH_HOOK4	68
68	NC_XDP_PCH_HOOK5	TRUE MAKE_BASE=TRUE	NC_XDP_PCH_HOOK5	68
	TP_XDP_PCH_OBSFN_B<0>	TRUE MAKE_BASE=TRUE	NC_XDP_PCH_OBSFN_B<0>	
68	NC_XDP_PCH_OBSFN_B<1>	TRUE MAKE_BASE=TRUE	NC_XDP_PCH_OBSFN_B<1>	68
	TP_XDP_PCH_OBSFN_A<0>	TRUE MAKE_BASE=TRUE	NC_XDP_PCH_OBSFN_A<0>	
68	NC_XDP_PCH_OBSFN_A<1>	TRUE MAKE_BASE=TRUE	NC_XDP_PCH_OBSFN_A<1>	68
	TP_XDP_PCH_OBSFN_D<0>	TRUE MAKE_BASE=TRUE	NC_XDP_PCH_OBSFN_D<0>	
68	NC_XDP_PCH_OBSFN_D<1>	TRUE MAKE_BASE=TRUE	NC_XDP_PCH_OBSFN_D<1>	68
68	NC_XDP_PCH_TRST_L	TRUE MAKE_BASE=TRUE	NC_XDP_PCH_TRST_L	68
68	NC_1V05_S0_PCH_VCCAPLLEXP	TRUE MAKE_BASE=TRUE	NC_1V05_S0_PCH_VCCAPLLEXP	68
68	NC_AUD_CODEC_MICBIAS	TRUE MAKE_BASE=TRUE	NC_AUD_CODEC_MICBIAS	68
68	NC_AUD_MIC_INRP	TRUE MAKE_BASE=TRUE	NC_AUD_MIC_INRP	68
68	NC_AUD_MIC_INRN	TRUE MAKE_BASE=TRUE	NC_AUD_MIC_INRN	68

ICT Test Points

NC NO_TEST

High Speed NO_TEST

- PCIE_AP_R2D_C_P — TRUE — 14 63 70
- PCIE_AP_R2D_C_N — TRUE — 14 63 70
- PCIE_AP_D2R_P — TRUE — 14 63 68 70
- PCIE_AP_D2R_N — TRUE — 14 63 68 70
- PCIE_SSD_R2D_C_P<3..0> — TRUE — 12 30 70
- PCIE_SSD_R2D_C_N<3..0> — TRUE — 12 30 70
- PCIE_SSD_R2D_P<3..0> — TRUE — 30 70
- PCIE_SSD_R2D_N<3..0> — TRUE — 30 70
- PCIE_SSD_D2R_P<3..0> — TRUE — 12 30 68 70
- PCIE_SSD_D2R_N<3..0> — TRUE — 12 30 68 70
- PCIE_TBT_R2D_C_P<3..0> — TRUE — 14 23 70
- PCIE_TBT_R2D_C_N<3..0> — TRUE — 14 23 70
- PCIE_TBT_R2D_P<3..0> — TRUE — 23 70
- PCIE_TBT_R2D_N<3..0> — TRUE — 23 70
- PCIE_TBT_D2R_P<3..1> — TRUE — 14 23 70
- PCIE_TBT_D2R_N<3..1> — TRUE — 14 23 70
- PCIE_TBT_D2R_C_P<3..1> — TRUE — 23 70
- PCIE_TBT_D2R_C_N<3..1> — TRUE — 23 70
- USB3_EXTA_D2R_P — TRUE — 14 33 71
- USB3_EXTA_D2R_N — TRUE — 14 33 71
- USB3_EXTA_R2D_C_P — TRUE — 14 33 71
- USB3_EXTA_R2D_C_N — TRUE — 14 33 71
- USB3_EXTA_R2D_N — TRUE — 33 68 71
- USB3_EXTA_R2D_N — TRUE — 33 68 71
- USB3_EXTB_D2R_P — TRUE — 14 63 71
- USB3_EXTB_D2R_N — TRUE — 14 63 71
- USB3_EXTB_R2D_C_P — TRUE — 14 63 71
- USB3_EXTB_R2D_C_N — TRUE — 14 63 71
- PCIE_CLK100M_SSD_P — TRUE — 12 30 70
- PCIE_CLK100M_SSD_N — TRUE — 12 30 70
- PCIE_CLK100M_TBT_P — TRUE — 12 23 68 70
- PCIE_CLK100M_TBT_N — TRUE — 12 23 68 70
- PCIE_CLK100M_AP_P — TRUE — 12 63 70
- PCIE_CLK100M_AP_N — TRUE — 12 63 70
- PCIE_CLK100M_CAMERA_P — TRUE — 12 32 70
- PCIE_CLK100M_CAMERA_N — TRUE — 12 32 70

Unused nets with offpage

(Nets with offpages not used on this project)
- HDD_PWR_EN — 15
- WOL_EN — 14
- BT_PWRRST_L — 15
- FW_PWR_EN — 15
- FW_PME_L — 15
- ENET_MEDIA_SENSE — 15
- ODD_PWR_EN_L — 13
- ENET_LOW_PWR — 13
- AUD_IP_PERIPHERAL_DET — 13
- AUD_I2C_INT_L — 13
- AUD_IPHS_SWITCH_EN — 13
- ENETSD_CLKREQ_L — 12

SYNC_MASTER=J44 — SYNC_DATE=08/12/2013

PAGE TITLE: Functional / ICT Test

Apple Inc.

DRAWING NUMBER: <SCH_NUM> — SIZE: D
REVISION: <E4LABEL>
BRANCH: <BRANCH>
PAGE: 104 OF 120
SHEET: 68 OF 78

J44 BOARD-SPECIFIC SPACING & PHYSICAL CONSTRAINTS

BOARD LAYERS	BOARD AREAS	BOARD UNITS (MIL or MM)	ALLEGRO VERSION
TOP,ISL2,ISL3,ISL4,ISL5,ISL6,ISL7,ISL8,ISL9,ISL10,ISL11,BOTTOM	NO_TYPE,BGA,P65BGA,BGA_MEM	MM	16.5

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DEFAULT	*	Y	=45_OHM_SE	=45_OHM_SE	10 MM	0 MM	0 MM
STANDARD	*	Y	=DEFAULT	=DEFAULT	10 MM	=DEFAULT	=DEFAULT

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
50_OHM_SE	TOP,BOTTOM	Y	0.095 MM	0.095 MM			
50_OHM_SE	*	Y	0.066 MM	0.066 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
45_OHM_SE	TOP,BOTTOM	Y	0.116 MM	0.116 MM			
45_OHM_SE	*	Y	0.083 MM	0.083 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
40_OHM_SE	TOP,BOTTOM	Y	0.145 MM	0.095 MM			
40_OHM_SE	*	Y	0.102 MM	0.090 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
37_OHM_SE	TOP,BOTTOM	Y	0.165 MM	0.095 MM			
37_OHM_SE	*	Y	0.118 MM	0.090 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
27P4_OHM_SE	TOP,BOTTOM	Y	0.265 MM	0.095 MM			
27P4_OHM_SE	*	Y	0.186 MM	0.090 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
72_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
72_OHM_DIFF	ISL3,ISL4,ISL9,ISL10	Y	0.105 MM	0.105 MM		0.120 MM	0.120 MM
72_OHM_DIFF	ISL2,ISL11	Y	0.105 MM	0.105 MM		0.120 MM	0.120 MM
72_OHM_DIFF	TOP,BOTTOM	Y	0.146 MM	0.146 MM		0.120 MM	0.120 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
80_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
80_OHM_DIFF	ISL3,ISL4,ISL9,ISL10	Y	0.092 MM	0.092 MM		0.120 MM	0.120 MM
80_OHM_DIFF	ISL2,ISL11	Y	0.092 MM	0.092 MM		0.120 MM	0.120 MM
80_OHM_DIFF	TOP,BOTTOM	Y	0.125 MM	0.125 MM		0.155 MM	0.155 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
85_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
85_OHM_DIFF	ISL3,ISL4,ISL9,ISL10	Y	0.080 MM	0.080 MM		0.120 MM	0.120 MM
85_OHM_DIFF	ISL2,ISL11	Y	0.080 MM	0.080 MM		0.120 MM	0.120 MM
85_OHM_DIFF	TOP,BOTTOM	Y	0.105 MM	0.105 MM		0.125 MM	0.125 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
90_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
90_OHM_DIFF	ISL3,ISL4,ISL9,ISL10	Y	0.078 MM	0.078 MM		0.200 MM	0.200 MM
90_OHM_DIFF	ISL2,ISL11	Y	0.078 MM	0.078 MM		0.200 MM	0.200 MM
90_OHM_DIFF	TOP,BOTTOM	Y	0.101 MM	0.101 MM		0.180 MM	0.180 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
P65_BGA	*	Y	0.071MM	0.071MM		0.075MM	0.126MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1TO1_DIFFPAIR	*	Y	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.1 MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
*	*	BGA	P072_SPACE
*	*	P65BGA	P075_SPACE

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DEFAULT	*	0.1 MM	?
STANDARD	*	=DEFAULT	?
P072_SPACE	*	0.071 MM	?
P075_SPACE	*	0.075 MM	?

Stackup-Defined Spacing Rules

Note: Outer dielectric is 0.058 mm nominal,
Inner dielectric is 0.053 mm nominal.

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1:1_SPACING	.	0.1 MM	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1x_DIELECTRIC	TOP,BOTTOM	0.058 MM	?
1x_DIELECTRIC	ISL3,ISL4,ISL9,ISL10	0.053 MM	?
1x_DIELECTRIC	ISL2,ISL5,ISL6,ISL7,ISL8,ISL11	0.101 MM	?

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
*	P65BGA	P65_BGA

SYNC_MASTER=J44 SYNC_DATE=08/12/2013

PAGE TITLE: PCB Rule Definitions

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

REVISION: <E4LABEL>

BRANCH: <BRANCH>

PAGE: 110 OF 120

SHEET: 69 OF 78

CPU Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CPU_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
CPU_27P4S	*	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	7 MIL	7 MIL

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_VCCSENSE	*	25 MIL	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_08MIL	*	0.203 MM	?
CPU_12MIL	*	0.305 MM	?
CPU_18MIL	*	0.457 MM	?
CPU_25MIL	*	0.635 MM	?

PCI Express Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCIE_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF
CLK_PCIE_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE_2SAME	*	=3X_DIELECTRIC	?
PCIE_TXRX	*	=6X_DIELECTRIC	?
PCIE_2OTHER	*	=4X_DIELECTRIC	?
PCIE_2CLK	*	=7X_DIELECTRIC	?
PCIECLK_2OTHER	*	=7X_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE_2SAME	TOP,BOTTOM	=4X_DIELECTRIC	?
PCIE_TXRX	TOP,BOTTOM	=10X_DIELECTRIC	?
PCIE_2OTHER	TOP,BOTTOM	=6X_DIELECTRIC	?
PCIE_2CLK	TOP,BOTTOM	=10X_DIELECTRIC	?
PCIECLK_2OTHER	TOP,BOTTOM	=10X_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
PCIE_*	*	*	PCIE_2OTHER
PCIE_*	=SAME	*	PCIE_2SAME
PCIE_*	CLK_*	*	PCIE_2CLK
CLK_PCIE	*	*	PCIECLK_2OTHER
PCIE_TX	*_RX	*	PCIE_TXRX
PCIE_RX	*_TX	*	PCIE_TXRX

CPU Signal Properties

ELECTRICAL CONST SET	NET TYPE PHYSICAL	NET TYPE SPACING		
XDP_TCK0	CPU_45S	CPU_18MIL	XDP_CPU_TCK	6 16
XDP_TCK0	CPU_45S	CPU_18MIL	PCH_JTAGX	12 16
XDP_TCK1	CPU_45S	CPU_18MIL	XDP_PCH_TCK	12 16
XDP_TDO	CPU_45S		XDP_CPU_TDO	6 16
XDP_TDO	CPU_45S		XDP_PCH_TDO	12 16
XDP_TDI	CPU_45S		XDP_CPU_TDI	6 16
XDP_TDI	CPU_45S		XDP_PCH_TDI	12 16
XDP_TMS	CPU_45S		XDP_CPU_TMS	6 16
XDP_TMS	CPU_45S		XDP_PCH_TMS	12 16
XDP_TRST_L	CPU_45S		XDP_TRST_L	16
XDP_TRST_L	CPU_45S		XDP_CPUPCH_TRST_L	6 12 16
XDP_PRDY_L	CPU_45S		XDP_CPU_PRDY_L	6 16
XDP_PREQ_L	CPU_45S		XDP_CPU_PREQ_L	6 16
CPU_VCCST_PWRGD	CPU_45S	CPU_08MIL	CPU_VCCST_PWRGD	8 16 17
CPU_VCCST_PWRGD	CPU_45S	CPU_08MIL	XDP_CPU_VCCST_PWRGD	16
CPU_BPM	CPU_45S	CPU_08MIL	XDP_BPM_L<1..0>	6 16
CPU_BPM_TP	CPU_45S		XDP_BPM_L<7..2>	6 16
CPU_RCOMP_SM	CPU_27P4S	CPU_25MIL	CPU_SM_RCOMP<2..0>	6
CPU_RCOMP_EDP	CPU_27P4S	CPU_25MIL	MCP_EDP_RCOMP	5
CPU_RCOMP_OPI	CPU_27P4S	CPU_12MIL	CPU_OPI_RCOMP	6
CPU_PROCHOT	CPU_45S	CPU_08MIL	CPU_PROCHOT_L	6 36 37 53
CPU_PROCHOT	CPU_45S	CPU_08MIL	CPU_PROCHOT_R_L	6
CPU_CATERR	CPU_45S	CPU_08MIL	CPU_CATERR_L	6 36
CPU_VIDALERT	CPU_45S	CPU_18MIL	CPU_VIDALERT_L	8 53
CPU_VIDALERT	CPU_45S	CPU_18MIL	CPU_VIDALERT_R_L	8
CPU_VIDSCLK	CPU_45S	CPU_18MIL	CPU_VIDSCLK	8 53
CPU_VIDSCLK	CPU_45S	CPU_18MIL	CPU_VIDSCLK_R	8
CPU_VIDSOUT	CPU_45S	CPU_18MIL	CPU_VIDSOUT	8 53
CPU_VIDSOUT	CPU_45S	CPU_18MIL	CPU_VIDSOUT_R	8
CPU_PECI	CPU_45S	CPU_18MIL	CPU_PECI	6 37
CPU_PECI	CPU_45S	CPU_18MIL	CPU_PECI_R	36 37
CPU_PECI_SMC	CPU_45S	CPU_18MIL	SMC_PECI_L	36 37
CPU_PECI_SMC	CPU_45S	CPU_18MIL	SMC_PECI_L_R	37
CPU_CFG	CPU_45S		CPU_CFG<19..11>	6 16
CPU_CFG_PD	CPU_45S		CPU_CFG<10..8>	6 16
CPU_CFG	CPU_45S		CPU_CFG<7..5>	6 16
CPU_CFG_PD	CPU_45S		CPU_CFG<4>	6 16
CPU_CFG_3	CPU_45S		CPU_CFG<3>	6 16
CPU_CFG	CPU_45S		CPU_CFG<2>	6 16
CPU_CFG_PD	CPU_45S		CPU_CFG<1..0>	6 16
CPU_MEM_RESET	CPU_45S	CPU_08MIL	MEM_RESET_L	20 21 22
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCCSENSE_P	8 53
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCCSENSE_N	9 53

PCI Express Properties

ELECTRICAL CONST SET	NET TYPE PHYSICAL	NET TYPE SPACING		
PCIE_SSD_D2R	PCIE_85D	PCIE_RX	PCIE_SSD_D2R_P<3..1>	12 30 68
PCIE_SSD_D2R	PCIE_85D	PCIE_RX	PCIE_SSD_D2R_N<3..1>	12 30 68
PCIE_SSD_D2R_PP	PCIE_85D	PCIE_RX	PCIE_SSD_D2R_P<0>	12 30 68
PCIE_SSD_D2R_PP	PCIE_85D	PCIE_RX	PCIE_SSD_D2R_N<0>	12 30 68
PCIE_SSD_R2D	PCIE_85D	PCIE_TX	PCIE_SSD_R2D_C_P<3..0>	12 30 68
PCIE_SSD_R2D	PCIE_85D	PCIE_TX	PCIE_SSD_R2D_C_N<3..0>	12 30 68
PCIE_SSD_R2D	PCIE_85D	PCIE_TX	PCIE_SSD_R2D_P<3..0>	30 68
PCIE_SSD_R2D	PCIE_85D	PCIE_TX	PCIE_SSD_R2D_N<3..0>	30 68
PCIE_TBT_D2R_0	PCIE_85D	PCIE_RX	PCIE_TBT_D2R_P<0>	14 23 68
PCIE_TBT_D2R_0	PCIE_85D	PCIE_RX	PCIE_TBT_D2R_N<0>	14 23 68
PCIE_TBT_D2R_0	PCIE_85D	PCIE_RX	PCIE_TBT_D2R_C_P<0>	23
PCIE_TBT_D2R_0	PCIE_85D	PCIE_RX	PCIE_TBT_D2R_C_N<0>	23
PCIE_TBT_D2R	PCIE_85D	PCIE_RX	PCIE_TBT_D2R_P<3..1>	14 23 68
PCIE_TBT_D2R	PCIE_85D	PCIE_RX	PCIE_TBT_D2R_N<3..1>	14 23 68
PCIE_TBT_D2R	PCIE_85D	PCIE_RX	PCIE_TBT_D2R_C_P<3..1>	23 68
PCIE_TBT_D2R	PCIE_85D	PCIE_RX	PCIE_TBT_D2R_C_N<3..1>	23 68
PCIE_TBT_R2D	PCIE_85D	PCIE_TX	PCIE_TBT_R2D_P<3..0>	23 68
PCIE_TBT_R2D	PCIE_85D	PCIE_TX	PCIE_TBT_R2D_N<3..0>	23 68
PCIE_TBT_R2D	PCIE_85D	PCIE_TX	PCIE_TBT_R2D_C_P<3..0>	14 23 68
PCIE_TBT_R2D	PCIE_85D	PCIE_TX	PCIE_TBT_R2D_C_N<3..0>	14 23 68
PCIE_AP_R2D	PCIE_85D	PCIE_TX	PCIE_AP_R2D_P	63 68
PCIE_AP_R2D	PCIE_85D	PCIE_TX	PCIE_AP_R2D_N	63 68
PCIE_AP_R2D	PCIE_85D	PCIE_TX	PCIE_AP_R2D_C_P	14 63 68
PCIE_AP_R2D	PCIE_85D	PCIE_TX	PCIE_AP_R2D_C_N	14 63 68
PCIE_AP_D2R	PCIE_85D	PCIE_RX	PCIE_AP_D2R_P	14 63 68
PCIE_AP_D2R	PCIE_85D	PCIE_RX	PCIE_AP_D2R_N	14 63 68
PCIE_CLK100M_AP	CLK_PCIE_85D	CLK_PCIE	PCIE_CLK100M_AP_CONN_P	63
PCIE_CLK100M_AP	CLK_PCIE_85D	CLK_PCIE	PCIE_CLK100M_AP_CONN_N	63
PCIE_CLK100M_AP	CLK_PCIE_85D	CLK_PCIE	PCIE_CLK100M_AP_P	12 63 68
PCIE_CLK100M_AP	CLK_PCIE_85D	CLK_PCIE	PCIE_CLK100M_AP_N	12 63 68
PCIE_CLK100M_CAM	CLK_PCIE_85D	CLK_PCIE	PCIE_CLK100M_CAMERA_P	12 32 68
PCIE_CLK100M_CAM	CLK_PCIE_85D	CLK_PCIE	PCIE_CLK100M_CAMERA_N	12 32 68
PCIE_CLK100M_CAM	CLK_PCIE_85D	CLK_PCIE	PCIE_CLK100M_CAMERA_C_P	31 32
PCIE_CLK100M_CAM	CLK_PCIE_85D	CLK_PCIE	PCIE_CLK100M_CAMERA_C_N	31 32
PCIE_CLK100M_SSD	CLK_PCIE_85D	CLK_PCIE	PCIE_CLK100M_SSD_P	12 30 68
PCIE_CLK100M_SSD	CLK_PCIE_85D	CLK_PCIE	PCIE_CLK100M_SSD_N	12 30 68
PCIE_CLK100M_TBT	CLK_PCIE_85D	CLK_PCIE	PCIE_CLK100M_TBT_P	12 23 68
PCIE_CLK100M_TBT	CLK_PCIE_85D	CLK_PCIE	PCIE_CLK100M_TBT_N	12 23 68
PCIE_CAMERA_D2R	PCIE_85D	PCIE_RX	PCIE_CAMERA_D2R_P	14 32 68
PCIE_CAMERA_D2R	PCIE_85D	PCIE_RX	PCIE_CAMERA_D2R_N	14 32 68
PCIE_CAMERA_D2R	PCIE_85D	PCIE_RX	PCIE_CAMERA_D2R_C_P	31 32
PCIE_CAMERA_D2R	PCIE_85D	PCIE_RX	PCIE_CAMERA_D2R_C_N	31 32
PCIE_CAMERA_R2D	PCIE_85D	PCIE_TX	PCIE_CAMERA_R2D_P	31 32
PCIE_CAMERA_R2D	PCIE_85D	PCIE_TX	PCIE_CAMERA_R2D_N	31 32
PCIE_CAMERA_R2D	PCIE_85D	PCIE_TX	PCIE_CAMERA_R2D_C_P	14 32
PCIE_CAMERA_R2D	PCIE_85D	PCIE_TX	PCIE_CAMERA_R2D_C_N	14 32

SYNC_MASTER=J44 SYNC_DATE=08/12/2013

PAGE TITLE: CPU & PCIe Constraints

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

REVISION: <E4LABEL>

BRANCH: <BRANCH>

PAGE: 111 OF 120

SHEET: 70 OF 78

USB 2 Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCH_USB_RBIAS	*	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
USB_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	*	=4X_DIELECTRIC	?
USB_RBIAS	*	=6X_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	TOP,BOTTOM	=6X_DIELECTRIC	?
USB_RBIAS	TOP,BOTTOM	=10X_DIELECTRIC	?

USB 3 Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
USB3_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB3_2SAME	*	=3X_DIELECTRIC	?
USB3_TXRX	*	=6X_DIELECTRIC	?
USB3_2OTHER	*	=4X_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB3_2SAME	TOP,BOTTOM	=4x_DIELECTRIC	?
USB3_TXRX	TOP,BOTTOM	=10X_DIELECTRIC	?
USB3_2OTHER	TOP,BOTTOM	=6X_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
USB3_*	*	*	USB3_2OTHER
USB3_*	=SAME	*	USB3_2SAME
USB3_TX	*_RX	*	USB3_TXRX
USB3_RX	*_TX	*	USB3_TXRX

System Clock Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_25M_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_25M	*	=5x_DIELECTRIC	?

SATA Interface Constraints (Not Used)

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SATA_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF
SATA_45SE	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA_2SAME	*	=3X_DIELECTRIC	?
SATA_TXRX	*	=6X_DIELECTRIC	?
SATA_2OTHER	*	=4X_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA_2SAME	TOP,BOTTOM	=4x_DIELECTRIC	?
SATA_TXRX	TOP,BOTTOM	=10X_DIELECTRIC	?
SATA_2OTHER	TOP,BOTTOM	=6X_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
SATA_*	*	*	SATA_2OTHER
SATA_*	=SAME	*	SATA_2SAME
SATA_TX	*_RX	*	SATA_TXRX
SATA_RX	*_TX	*	SATA_TXRX

USB Constraints

ELECTRICAL CONST SET	NET TYPE: PHYSICAL	NET TYPE: SPACING		
USB_BT	USB_85D	USB	USB_BT_P	14 29
USB_BT	USB_85D	USB	USB_BT_N	14 29
USB_BT	USB_85D	USB	USB_BT_CONN_P	29 63
USB_BT	USB_85D	USB	USB_BT_CONN_N	29 63
USB_EXTA	USB_85D	USB	USB_EXTA_P	14 33
USB_EXTA	USB_85D	USB	USB_EXTA_N	14 33
	DEFAULT	DEFAULT	SMC_DEBUGPRT_RX_L	33 36 37
	DEFAULT	DEFAULT	SMC_DEBUGPRT_TX_L	33 36 37
USB_EXTA	USB_85D	USB	USB2_EXTA_MUXED_P	33
USB_EXTA	USB_85D	USB	USB2_EXTA_MUXED_N	33
USB_EXTA	USB_85D	USB	USB2_EXTA_MUXED_F_P	33
USB_EXTA	USB_85D	USB	USB2_EXTA_MUXED_F_N	33
USB_EXTA	USB_85D	USB	USB_LT1_P	68
USB_EXTA	USB_85D	USB	USB_LT1_N	68
USB_EXTB	USB_85D	USB	USB_EXTB_P	14 63
USB_EXTB	USB_85D	USB	USB_EXTB_N	14 63
USB_TPAD	USB_85D	USB	USB_TPAD_P	14 34
USB_TPAD	USB_85D	USB	USB_TPAD_N	14 34
USB_TPAD	USB_85D	USB	USB_TPAD_R_P	34
USB_TPAD	USB_85D	USB	USB_TPAD_R_N	34
USB3_EXTA_D2R	USB_85D	USB3_RX	USB3_EXTA_D2R_P	14 33 68
USB3_EXTA_D2R	USB_85D	USB3_RX	USB3_EXTA_D2R_N	14 33 68
USB3_EXTA_R2D	USB_85D	USB3_TX	USB3_EXTA_R2D_P	33
USB3_EXTA_R2D	USB_85D	USB3_TX	USB3_EXTA_R2D_N	33 68
USB3_EXTA_R2D	USB_85D	USB3_TX	USB3_EXTA_R2D_C_P	14 33 68
USB3_EXTA_R2D	USB_85D	USB3_TX	USB3_EXTA_R2D_C_N	14 33 68
USB3_EXTB_D2R	USB_85D	USB3_RX	USB3_EXTB_D2R_P	14 63 68
USB3_EXTB_D2R	USB_85D	USB3_RX	USB3_EXTB_D2R_N	14 63 68
USB3_EXTB_R2D	USB_85D	USB3_TX	USB3_EXTB_R2D_C_P	14 63 68
USB3_EXTB_R2D	USB_85D	USB3_TX	USB3_EXTB_R2D_C_N	14 63 68
USB3_SD_D2R	USB3_85D	USB3_RX	USB3RPCIE_SD_D2R_P	14 63 68
USB3_SD_D2R	USB3_85D	USB3_RX	USB3RPCIE_SD_D2R_N	14 63 68
USB3_SD_R2D	USB3_85D	USB3_TX	USB3RPCIE_SD_R2D_C_P	14 63
USB3_SD_R2D	USB3_85D	USB3_TX	USB3RPCIE_SD_R2D_C_N	14 63
USB_NC	USB_85D	USB	NC_USB_IRP	14 66
USB_NC	USB_85D	USB	NC_USB_IRN	14 66
USB_NC	USB_85D	USB	TP_USB_5P	14
USB_NC	USB_85D	USB	TP_USB_5N	14
USB_NC	USB_85D	USB	NC_USB_SDP	14 66
USB_NC	USB_85D	USB	NC_USB_SDN	14 66
USB_NC	USB_85D	USB	NC_USB_CAMERAP	14 66
USB_NC	USB_85D	USB	NC_USB_CAMERAN	14 66
PCH_USB_RBIAS	PCH_USB_RBIAS	USB_RBIAS	PCH_USB_RBIAS	14
	SATA_85D	SATA_RX	DUMMY_SATA_D2R_P	
	SATA_85D	SATA_RX	DUMMY_SATA_D2R_N	
	SATA_85D	SATA_TX	DUMMY_SATA_R2D_P	
	SATA_85D	SATA_TX	DUMMY_SATA_R2D_N	
SYSCLK_CLK25M	CLK_25M_45S	CLK_25M	SYSCLK_CLK25M_X1	17
SYSCLK_CLK25M	CLK_25M_45S	CLK_25M	SYSCLK_CLK25M_X2	17
SYSCLK_CLK25M	CLK_25M_45S	CLK_25M	SYSCLK_CLK25M_X2_R	17
SYSCLK_CLK25M_CAM	CLK_25M_45S	CLK_25M	SYSCLK_CLK25M_CAMERA	17 32
SYSCLK_CLK25M_CAM	CLK_25M_45S	CLK_25M	CLK25M_CAM_CLKP	31 32
SYSCLK_CLK25M_CAM	CLK_25M_45S	CLK_25M	CLK25M_CAM_XTALP_R	32
SYSCLK_CLK25M_CAM	CLK_25M_45S	CLK_25M	CLK25M_CAM_XTALP	32
SYSCLK_CLK25M_CAM	CLK_25M_45S	CLK_25M	CLK25M_CAM_XTALN	32
SYSCLK_CLK25M_CAM	CLK_25M_45S	CLK_25M	CLK25M_CAM_CLKN	31 32
SYSCLK_CLK25M_TBT	CLK_25M_45S	CLK_25M	SYSCLK_CLK25M_TBT	17 23
SYSCLK_CLK25M_TBT	CLK_25M_45S	CLK_25M	SYSCLK_CLK25M_TBT_R	23

Notes:
This is here to keep the SATA rules.

SYNC_MASTER=J44 SYNC_DATE=08/12/2013

PAGE TITLE: USB Constraints

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D
REVISION: <E4LABEL>
BRANCH: <BRANCH>
PAGE: 112 OF 120
SHEET: 71 OF 78

LPC Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
LPC_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
CLK_LPC_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
LPC	*	6 MIL	?
CLK_LPC	*	8 MIL	?

SMBus Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SMB_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SMB	*	=2x_DIELECTRIC	?

HD Audio Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
HDA_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
HDA	*	=2x_DIELECTRIC	?

SPI Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SPI_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SPI	*	8 MIL	?

PCH Single Net Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCH_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
PCH_27P4S	*	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	7 MIL	7 MIL

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCH_12MIL	*	0.305 MM	?
PCH_15MIL	*	0.381 MM	?
PCH_18MIL	*	0.457 MM	?
PCH_20MIL	*	0.508 MM	?

PCH Net Properties

ELECTRICAL CONST SET	NET TYPE: PHYSICAL	NET TYPE: SPACING		
LPC_AD	LPC_45S	LPC	LPC_AD<3..0>	14 36 45 68
LPC_AD	LPC_45S	LPC	LPC_FRAME_L	14 36 45 68
LPC_CLK24M_SMC	CLK_LPC_45S	CLK_LPC	LPC_CLK24M_SMC_R	12 17
LPC_CLK24M_SMC	CLK_LPC_45S	CLK_LPC	LPC_CLK24M_SMC	17 36 68
LPC_CLK24M_LPCPLUS	CLK_LPC_45S	CLK_LPC	LPC_CLK24M_LPCPLUS	17 45 68
LPC_CLK24M_LPCPLUS	CLK_LPC_45S	CLK_LPC	LPC_CLK24M_LPCPLUS_R	12 17
SMBUS_PCH	SMB_45S	SMB	SMBUS_PCH_CLK	14 16 19 39 63 68
SMBUS_PCH	SMB_45S	SMB	SMBUS_PCH_DATA	14 16 19 39 63 68
SML_PCH_0	SMB_45S	SMB	SML_PCH_0_CLK	14 39
SML_PCH_0	SMB_45S	SMB	SML_PCH_0_DATA	14 39
	SMB_45S	SMB	SMBUS_SMC_1_S0_SCL	14 32 36 39 43 68 76
	SMB_45S	SMB	SMBUS_SMC_1_S0_SDA	14 32 36 39 43 68 76
HDA_BIT_CLK	HDA_45S	HDA	HDA_BIT_CLK	12 47
HDA_BIT_CLK	HDA_45S	HDA	HDA_BIT_CLK_R	12
HDA_SYNC	HDA_45S	HDA	HDA_SYNC	12 47
HDA_SYNC	HDA_45S	HDA	HDA_SYNC_R	12
HDA_RST	HDA_45S	HDA	HDA_RST_R_L	12
HDA_RST	HDA_45S	HDA	HDA_RST_L	12 47
HDA_SDIN	HDA_45S	HDA	HDA_SDIN0	12 47 68
HDA_SDIN	HDA_45S	HDA	CS4208_HDA_SDOUT0_R	47
HDA_SDOUT	HDA_45S	HDA	HDA_SDOUT	12 47
HDA_SDOUT	HDA_45S	HDA	HDA_SDOUT_R	12 17
SPI_MLB	SPI_45S	SPI	SPI_ALT_CLK	45
SPI_MLB	SPI_45S	SPI	SPI_CLK	45
SPI_MLB	SPI_45S	SPI	SPI_CLK_R	14 45
SPI_MLB	SPI_45S	SPI	SPI_MLB_CLK	45
SPI_MLB	SPI_45S	SPI	SPI_SMC_CLK	36 45
SPI_MLB	SPI_45S	SPI	SPI_ALT_CS_L	45
SPI_MLB	SPI_45S	SPI	SPI_CS0_L	45
SPI_MLB	SPI_45S	SPI	SPI_CS0_R_L	14 45
SPI_MLB	SPI_45S	SPI	SPI_MLB_CS_L	45
SPI_MLB	SPI_45S	SPI	SPI_SMC_CS_L	36 45
SPI_MLB	SPI_45S	SPI	SPI_ALT_MISO	45
SPI_MLB	SPI_45S	SPI	SPI_MISO	14 45
SPI_MLB	SPI_45S	SPI	SPI_MISO_R	45
SPI_MLB	SPI_45S	SPI	SPI_MLB_MISO	45
SPI_MLB	SPI_45S	SPI	SPI_SMC_MISO	36 45
SPI_MLB	SPI_45S	SPI	SPI_ALT_MOSI	45
SPI_MLB	SPI_45S	SPI	SPI_MOSI	45
SPI_MLB	SPI_45S	SPI	SPI_MOSI_R	14 45
SPI_MLB	SPI_45S	SPI	SPI_MLB_MOSI	45
SPI_MLB	SPI_45S	SPI	SPI_SMC_MOSI	36 45
SPI_MLB_IO2	SPI_45S	SPI	SPI_IO<2>	14 45
SPI_MLB_IO2	SPI_45S	SPI	SPIROM_WP_L	45
SPI_MLB_IO3	SPI_45S	SPI	SPI_IO<3>	14 45
SPI_MLB_IO3	SPI_45S	SPI	SPIROM_HOLD_L	45
SPI_MLB_IO3	SPI_45S	SPI	SPIROM_USE_MLB	15 45 68
PCH_RTCX	PCH_45S	PCH_15MIL	PCH_CLK32K_RTCX1	12 17
PCH_SRTCRST	PCH_45S	PCH_15MIL	PCH_SRTCRST_L	12
PCH_RTCRST	PCH_45S	PCH_15MIL	RTC_RESET_L	12
PCH_THRMTRIP	PCH_45S	PCH_18MIL	PM_THRMTRIP_L	15 37
PCH_THRMTRIP	PCH_45S	PCH_18MIL	PM_THRMTRIP_R_L	37
	PCH_45S	PCH_15MIL	PCH_INTRUDER_L	12
	PCH_45S	PCH_15MIL	PCH_INTVRMEN	12
	PCH_45S	PCH_15MIL	PCH_DSWVRMEN	13
	PCH_45S	PCH_15MIL	PM_RSMRST_L	13 61
	PCH_45S	PCH_15MIL	PM_SYSRST_L	13 17 36 68
	PCH_45S	PCH_15MIL	XDP_DBRESET_L	16 17
	PCH_45S	PCH_15MIL	PM_PCH_SYS_PWROK	13 16 17 36
	PCH_45S	PCH_15MIL	XDP_SYS_PWROK	16
	PCH_45S	PCH_15MIL	SYS_PWROK_R	17
	PCH_45S	PCH_15MIL	PM_PCH_PWROK	13 17
	PCH_45S	PCH_15MIL	PM_S0_PGOOD	17
	PCH_45S	PCH_15MIL	SMC_DELAYED_PWRGD	17 24 25 36 37
	PCH_45S	PCH_15MIL	PM_DSW_PWRGD	13 36
	PCH_45S	PCH_15MIL	PM_PWRBTN_L	13 16 36
	PCH_45S	PCH_15MIL	XDP_CPU_PWRBTN_L	16
	PCH_45S	PCH_15MIL	PCIE_WAKE_L	13 29 31
	PCH_45S	PCH_15MIL	AP_PCIE_WAKE_L	29 63
	PCH_45S	PCH_15MIL	CAM_PCIE_WAKE_L	31
	PCH_45S	PCH_15MIL	TBT_CIO_PLUG_EVENT_L	15 18 23
PCH_CLK24M_XTAL	PCH_45S	PCH_20MIL	PCH_CLK24M_XTALIN	12 17
PCH_CLK24M_XTAL	PCH_45S	PCH_20MIL	PCH_CLK24M_XTALOUT	12 17
PCH_CLK24M_XTAL	PCH_45S	PCH_20MIL	PCH_CLK24M_XTALOUT_R	17
PCH_RCOMP_PCIE	PCH_27P4S	PCH_12MIL	PCH_PCIE_RCOMP	14
PCH_RCOMP_OPI	PCH_27P4S	PCH_12MIL	PCH_OPI_COMP	15
PCH_RCOMP_SATA	PCH_27P4S	PCH_12MIL	PCH_SATA_RCOMP	12

SYNC_MASTER=J44 SYNC_DATE=08/12/2013

PAGE TITLE: PCH Constraints

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

REVISION: <E4LABEL>

BRANCH: <BRANCH>

PAGE: 113 OF 120

SHEET: 72 OF 78

Memory Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_40S	*	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=STANDARD	=STANDARD
MEM_72D	*	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF
MEM_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
MEM_80D	*	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF
MEM_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
MEM_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

Spacing Rule Sets

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MEM_DATA2SELF	*	=2x_DIELECTRIC	?
MEM_DQS2OWNDATA	*	=2x_DIELECTRIC	?
MEM_CMD2CMD	*	=2x_DIELECTRIC	?
MEM_CMD2CTL	*	=2x_DIELECTRIC	?
MEM_CTL2CTL	*	=2x_DIELECTRIC	?
MEM_CLK2CLK	*	=4x_DIELECTRIC	?
MEM_2OTHERMEM	*	=4x_DIELECTRIC	?
MEM_2PWR	*	=2x_DIELECTRIC	?
MEM_2GND	*	=2x_DIELECTRIC	?
MEM_2OTHER	*	=6x_DIELECTRIC	?
MEM_CMD2CMD_BM	*	=2x_DIELECTRIC	?
MEM_CMD2CTL_BM	*	=2x_DIELECTRIC	?
MEM_CTL2CTL_BM	*	=2x_DIELECTRIC	?
MEM_12MIL	*	0.305 MM	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MEM_DATA2SELF	TOP,BOTTOM	=5x_DIELECTRIC	?
MEM_DQS2OWNDATA	TOP,BOTTOM	=5x_DIELECTRIC	?
MEM_CMD2CMD	TOP,BOTTOM	=5x_DIELECTRIC	?
MEM_CMD2CTL	TOP,BOTTOM	=5x_DIELECTRIC	?
MEM_CTL2CTL	TOP,BOTTOM	=5x_DIELECTRIC	?
MEM_CLK2CLK	TOP,BOTTOM	=8x_DIELECTRIC	?
MEM_2OTHERMEM	TOP,BOTTOM	=8x_DIELECTRIC	?
MEM_2PWR	TOP,BOTTOM	=4x_DIELECTRIC	?
MEM_2GND	TOP,BOTTOM	=4x_DIELECTRIC	?
MEM_2OTHER	TOP,BOTTOM	=10x_DIELECTRIC	?
MEM_CMD2CMD_BM	TOP,BOTTOM	=3x_DIELECTRIC	?
MEM_CMD2CTL_BM	TOP,BOTTOM	=3x_DIELECTRIC	?
MEM_CTL2CTL_BM	TOP,BOTTOM	=3x_DIELECTRIC	?

Memory Bus Spacing Group Assignments

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_*_DQBYTE_*	*	*	MEM_2OTHER
MEM_*_DQS_*	*	*	MEM_2OTHER
MEM_CMD	*	*	MEM_2OTHER
MEM_CTL	*	*	MEM_2OTHER
MEM_CLK	*	*	MEM_2OTHER

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_A_DQS_0	MEM_A_DQBYTE_0	*	MEM_DQS2OWNDATA
MEM_A_DQS_1	MEM_A_DQBYTE_1	*	MEM_DQS2OWNDATA
MEM_A_DQS_2	MEM_A_DQBYTE_2	*	MEM_DQS2OWNDATA
MEM_A_DQS_3	MEM_A_DQBYTE_3	*	MEM_DQS2OWNDATA
MEM_A_DQS_4	MEM_A_DQBYTE_4	*	MEM_DQS2OWNDATA
MEM_A_DQS_5	MEM_A_DQBYTE_5	*	MEM_DQS2OWNDATA
MEM_A_DQS_6	MEM_A_DQBYTE_6	*	MEM_DQS2OWNDATA
MEM_A_DQS_7	MEM_A_DQBYTE_7	*	MEM_DQS2OWNDATA
MEM_B_DQS_0	MEM_B_DQBYTE_0	*	MEM_DQS2OWNDATA
MEM_B_DQS_1	MEM_B_DQBYTE_1	*	MEM_DQS2OWNDATA
MEM_B_DQS_2	MEM_B_DQBYTE_2	*	MEM_DQS2OWNDATA
MEM_B_DQS_3	MEM_B_DQBYTE_3	*	MEM_DQS2OWNDATA
MEM_B_DQS_4	MEM_B_DQBYTE_4	*	MEM_DQS2OWNDATA
MEM_B_DQS_5	MEM_B_DQBYTE_5	*	MEM_DQS2OWNDATA
MEM_B_DQS_6	MEM_B_DQBYTE_6	*	MEM_DQS2OWNDATA
MEM_B_DQS_7	MEM_B_DQBYTE_7	*	MEM_DQS2OWNDATA

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_*_DQBYTE_*	=SAME	*	MEM_DATA2SELF

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CMD	MEM_CMD	*	MEM_CMD2CMD
MEM_CMD	MEM_CTL	*	MEM_CMD2CTL
MEM_CTL	MEM_CTL	*	MEM_CTL2CTL
MEM_CLK	MEM_CLK	*	MEM_CLK2CLK
MEM_*	MEM_*	*	MEM_2OTHERMEM
MEM_CMD	MEM_CMD	BGA_MEM	MEM_CMD2CMD_BM
MEM_CMD	MEM_CTL	BGA_MEM	MEM_CMD2CTL_BM
MEM_CTL	MEM_CTL	BGA_MEM	MEM_CTL2CTL_BM

Haswell ULT Memory Down DDR3L 1x8 Length Matching

DDR3 Signal Group	Unit	Min Length	Max Length
CTLmax - CTLmin	mils	0	100
CTL to CLK	mils	CLK - 500	CLK + 500
CMDi to CMDj	mils	CMDj - 100	CMDj + 100
CMD to CLK	mils	CLK - 500	CLK + 500
(DQmax - DQmin) per byte	mils	0	250
(DQS - DQmax) per byte	mils	-100	150
DQS to DQS#	mils	-5	5
DQS to CLK (Rule 1)	mils	CLK - 6500	CLK + 500
Max(CLK-DQS) - Min(CLK-DQS)	mils	0	5500
CLK to CLK#	mils	-5	5

Memory to Power Spacing

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_PWR	MEM_*	*	MEM_2PWR
MEM_PWR	*	*	DEFAULT

Memory to GND Spacing

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
GND	MEM_*	*	MEM_2GND

Memory Net Properties

ELECTRICAL CONST SET	NET TYPE: PHYSICAL	NET TYPE: SPACING		
MEM_A_CLK	MEM_72D	MEM_CLK	MEM_A_CLK_P<0>	7 20 22
MEM_A_CLK	MEM_72D	MEM_CLK	MEM_A_CLK_N<0>	7 20 22
MEM_A_CTL	MEM_40S	MEM_CTL	MEM_A_CKE<0>	7 20 22
MEM_A_CTL	MEM_40S	MEM_CTL	MEM_A_CS_L<0>	7 20 22
MEM_A_ODT0	MEM_40S	MEM_CTL	MEM_A_ODT<0>	20 22
MEM_A_CMD	MEM_40S	MEM_CMD	MEM_A_A<15..0>	7 20 22 66
MEM_A_CMD	MEM_40S	MEM_CMD	MEM_A_BA<2..0>	7 20 22 66
MEM_A_CMD	MEM_40S	MEM_CMD	MEM_A_RAS_L	7 20 22 66
MEM_A_CMD	MEM_40S	MEM_CMD	MEM_A_CAS_L	7 20 22 66
MEM_A_CMD	MEM_40S	MEM_CMD	MEM_A_WE_L	7 20 22 66
MEM_A_DQBYTE0	MEM_45S	MEM_A_DQBYTE_0	MEM_A_DQ<7..0>	7 67 68
MEM_A_DQBYTE1	MEM_45S	MEM_A_DQBYTE_1	MEM_A_DQ<15..8>	7 67 68
MEM_A_DQBYTE2	MEM_45S	MEM_A_DQBYTE_2	MEM_A_DQ<23..16>	7 67 68
MEM_A_DQBYTE3	MEM_45S	MEM_A_DQBYTE_3	MEM_A_DQ<31..24>	7 67 68
MEM_A_DQBYTE4	MEM_45S	MEM_A_DQBYTE_4	MEM_A_DQ<39..32>	7 20 67 68
MEM_A_DQBYTE5	MEM_45S	MEM_A_DQBYTE_5	MEM_A_DQ<47..40>	7 67 68
MEM_A_DQBYTE6	MEM_45S	MEM_A_DQBYTE_6	MEM_A_DQ<55..48>	7 67 68
MEM_A_DQBYTE7	MEM_45S	MEM_A_DQBYTE_7	MEM_A_DQ<63..56>	7 67 68
MEM_A_DQS0	MEM_80D	MEM_A_DQS_0	MEM_A_DQS_P<0>	7 67
MEM_A_DQS0	MEM_80D	MEM_A_DQS_0	MEM_A_DQS_N<0>	7 67
MEM_A_DQS1	MEM_80D	MEM_A_DQS_1	MEM_A_DQS_P<1>	7 67
MEM_A_DQS1	MEM_80D	MEM_A_DQS_1	MEM_A_DQS_N<1>	7 67
MEM_A_DQS2	MEM_80D	MEM_A_DQS_2	MEM_A_DQS_P<2>	7 67
MEM_A_DQS2	MEM_80D	MEM_A_DQS_2	MEM_A_DQS_N<2>	7 67
MEM_A_DQS3	MEM_80D	MEM_A_DQS_3	MEM_A_DQS_P<3>	7 67
MEM_A_DQS3	MEM_80D	MEM_A_DQS_3	MEM_A_DQS_N<3>	7 67
MEM_A_DQS4	MEM_80D	MEM_A_DQS_4	MEM_A_DQS_P<4>	7 67
MEM_A_DQS4	MEM_80D	MEM_A_DQS_4	MEM_A_DQS_N<4>	7 67
MEM_A_DQS5	MEM_80D	MEM_A_DQS_5	MEM_A_DQS_P<5>	7 67
MEM_A_DQS5	MEM_80D	MEM_A_DQS_5	MEM_A_DQS_N<5>	7 67
MEM_A_DQS6	MEM_80D	MEM_A_DQS_6	MEM_A_DQS_P<6>	7 20 67
MEM_A_DQS6	MEM_80D	MEM_A_DQS_6	MEM_A_DQS_N<6>	7 20 67
MEM_A_DQS7	MEM_80D	MEM_A_DQS_7	MEM_A_DQS_P<7>	7 67
MEM_A_DQS7	MEM_80D	MEM_A_DQS_7	MEM_A_DQS_N<7>	7 67
MEM_B_CLK	MEM_72D	MEM_CLK	MEM_B_CLK_P<0>	7 21 22
MEM_B_CLK	MEM_72D	MEM_CLK	MEM_B_CLK_N<0>	7 21 22
MEM_B_CTL	MEM_40S	MEM_CTL	MEM_B_CKE<0>	7 21 22
MEM_B_CTL	MEM_40S	MEM_CTL	MEM_B_CS_L<0>	7 21 22
MEM_B_ODT0	MEM_40S	MEM_CTL	MEM_B_ODT<0>	21 22
MEM_B_CMD	MEM_40S	MEM_CMD	MEM_B_A<15..0>	7 21 22 66
MEM_B_CMD	MEM_40S	MEM_CMD	MEM_B_BA<2..0>	7 21 22 66
MEM_B_CMD	MEM_40S	MEM_CMD	MEM_B_RAS_L	7 21 22 66
MEM_B_CMD	MEM_40S	MEM_CMD	MEM_B_CAS_L	7 21 22 66
MEM_B_CMD	MEM_40S	MEM_CMD	MEM_B_WE_L	7 21 22 66
MEM_B_DQBYTE0	MEM_45S	MEM_B_DQBYTE_0	MEM_B_DQ<7..0>	7 67 68
MEM_B_DQBYTE1	MEM_45S	MEM_B_DQBYTE_1	MEM_B_DQ<15..8>	7 67 68
MEM_B_DQBYTE2	MEM_45S	MEM_B_DQBYTE_2	MEM_B_DQ<23..16>	7 67 68
MEM_B_DQBYTE3	MEM_45S	MEM_B_DQBYTE_3	MEM_B_DQ<31..24>	7 67 68
MEM_B_DQBYTE4	MEM_45S	MEM_B_DQBYTE_4	MEM_B_DQ<39..32>	7 21 67 68
MEM_B_DQBYTE5	MEM_45S	MEM_B_DQBYTE_5	MEM_B_DQ<47..40>	7 67 68
MEM_B_DQBYTE6	MEM_45S	MEM_B_DQBYTE_6	MEM_B_DQ<55..48>	7 67 68
MEM_B_DQBYTE7	MEM_45S	MEM_B_DQBYTE_7	MEM_B_DQ<63..56>	7 67 68
MEM_B_DQS0	MEM_80D	MEM_B_DQS_0	MEM_B_DQS_P<0>	7 67
MEM_B_DQS0	MEM_80D	MEM_B_DQS_0	MEM_B_DQS_N<0>	7 67
MEM_B_DQS1	MEM_80D	MEM_B_DQS_1	MEM_B_DQS_P<1>	7 67
MEM_B_DQS1	MEM_80D	MEM_B_DQS_1	MEM_B_DQS_N<1>	7 67
MEM_B_DQS2	MEM_80D	MEM_B_DQS_2	MEM_B_DQS_P<2>	7 67
MEM_B_DQS2	MEM_80D	MEM_B_DQS_2	MEM_B_DQS_N<2>	7 67
MEM_B_DQS3	MEM_80D	MEM_B_DQS_3	MEM_B_DQS_P<3>	7 67
MEM_B_DQS3	MEM_80D	MEM_B_DQS_3	MEM_B_DQS_N<3>	7 67
MEM_B_DQS4	MEM_80D	MEM_B_DQS_4	MEM_B_DQS_P<4>	7 67
MEM_B_DQS4	MEM_80D	MEM_B_DQS_4	MEM_B_DQS_N<4>	7 67
MEM_B_DQS5	MEM_80D	MEM_B_DQS_5	MEM_B_DQS_P<5>	7 67
MEM_B_DQS5	MEM_80D	MEM_B_DQS_5	MEM_B_DQS_N<5>	7 67
MEM_B_DQS6	MEM_80D	MEM_B_DQS_6	MEM_B_DQS_P<6>	7 21 67
MEM_B_DQS6	MEM_80D	MEM_B_DQS_6	MEM_B_DQS_N<6>	7 21 67
MEM_B_DQS7	MEM_80D	MEM_B_DQS_7	MEM_B_DQS_P<7>	7 67
MEM_B_DQS7	MEM_80D	MEM_B_DQS_7	MEM_B_DQS_N<7>	7 67
		MEM_PWR	PP1V35_S3	17 19 20 21 22 41 55 65
		MEM_PWR	PP1V35_S3_CPUDDR	8 10 41 65
		MEM_PWR	PP0V675_S0_DDRVTT	22 55 65 68
		MEM_PWR	PPVTTDDR_S3	55 65 68
		MEM_12MIL	CPU_DIMMA_VREFDQ	7 19
		MEM_12MIL	CPU_DIMMA_VREFDQ_A_ISOL	19
		MEM_12MIL	CPU_DIMMB_VREFDQ	7 19
		MEM_12MIL	CPU_DIMMB_VREFDQ_B_ISOL	19
		MEM_12MIL	CPU_DIMM_VREFCA	7 19
		MEM_12MIL	CPU_DIMM_VREFCA_A_ISOL	19
I140		MEM_12MIL	CPU_DIMM_VREFCA_B_ISOL	19
		MEM_12MIL	PP0V675_S3_MEM_VREFDQ_A	19 20 65
		MEM_12MIL	PP0V675_S3_MEM_VREFDQ_B	19 21 65
		MEM_12MIL	PP0V675_S3_MEM_VREFCA_A	19 20 65
		MEM_12MIL	PP0V675_S3_MEM_VREFCA_B	19 21 65

SYNC_MASTER=J44 SYNC_DATE=01/03/2013

PAGE TITLE: Memory Constraints

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

REVISION: <E4LABEL>

BRANCH: <BRANCH>

PAGE: 114 OF 120

SHEET: 73 OF 78

Thunderbolt, DP, HDMI Constraints

Thunderbolt SPI Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
TBT_SPI_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
TBT_SPI	*	=2x_DIELECTRIC	?

Thunderbolt & DisplayPort Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
TBTDP_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
TBTDP_2SAME	*	=3X_DIELECTRIC	?
TBTDP_TXRX	*	=6X_DIELECTRIC	?
TBTDP_2OTHER	*	=4X_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
TBTDP_2SAME	TOP,BOTTOM	=4x_DIELECTRIC	?
TBTDP_TXRX	TOP,BOTTOM	=10X_DIELECTRIC	?
TBTDP_2OTHER	TOP,BOTTOM	=6X_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
TBTDP_*	*	*	TBTDP_2OTHER
TBTDP_*	=SAME	*	TBTDP_2SAME
TBTDP_TX	*_RX	*	TBTDP_TXRX
TBTDP_RX	*_TX	*	TBTDP_TXRX

DisplayPort & HDMI Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DP_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF
HDMI_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DP_2SAME	*	=3x_DIELECTRIC	?
DP_2OTHER	*	=4x_DIELECTRIC	?
HDMICLK_2OTHER	*	=7x_DIELECTRIC	?
HDMICLK_2DPHDMI	*	=4x_DIELECTRIC	?
HDMIDATA_2SAME	*	=3x_DIELECTRIC	?
HDMIDATA_2OTHER	*	=4x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DP_2SAME	TOP,BOTTOM	=4x_DIELECTRIC	?
DP_2OTHER	TOP,BOTTOM	=6x_DIELECTRIC	?
HDMICLK_2OTHER	TOP,BOTTOM	=10x_DIELECTRIC	?
HDMICLK_2DPHDMI	TOP,BOTTOM	=6x_DIELECTRIC	?
HDMIDATA_2SAME	TOP,BOTTOM	=4x_DIELECTRIC	?
HDMIDATA_2OTHER	TOP,BOTTOM	=6x_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
HDMI_DATA	*	*	HDMIDATA_2OTHER
HDMI_DATA	=SAME	*	HDMIDATA_2SAME
HDMI_DATA	TBTDP_TX	*	HDMIDATA_2SAME
HDMI_DATA	TBTDP_RX	*	TBTDP_TXRX
HDMI_CLK	*	*	HDMICLK_2OTHER
HDMI_CLK	HDMI_DATA	*	HDMICLK_2DPHDMI
HDMI_CLK	DISPLAYPORT	*	HDMICLK_2DPHDMI
HDMI_CLK	TBTDP_TX	*	HDMICLK_2DPHDMI

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
DISPLAYPORT	*	*	DP_2OTHER
DISPLAYPORT	=SAME	*	DP_2SAME
DISPLAYPORT	HDMI_DATA	*	DP_2SAME
DISPLAYPORT	TBTDP_TX	*	DP_2SAME
DISPLAYPORT	TBTDP_RX	*	TBTDP_TXRX

DisplayPort/TMDS intra-pair matching should be 0.127mm. Inter-pair matching should be within 2.54cm. Max Length 241.3mm.
DisplayPort AUX CH intra-pair matching should be 0.127mm. Max length 330.2mm.
SOURCE: Calpella SFF DG Rev 1.5 (407364) and Family GPU DG-04202-001-v04.
MAX LENGTH OF DISPLAYPORT/TMDS TRACES: 13 INCHES.

ELECTRICAL CONST SET	NET TYPE PHYSICAL	NET TYPE SPACING		
	DP_85D	DISPLAYPORT	DP_TBTSRC_ML_C_P<3..0>	Only used on hosts supporting Thunderbolt video-in
	DP_85D	DISPLAYPORT	DP_TBTSRC_ML_C_N<3..0>	
	DP_85D	DISPLAYPORT	DP_TBTSRC_AUXCH_C_P	
	DP_85D	DISPLAYPORT	DP_TBTSRC_AUXCH_C_N	
SPI_TBT_CLK	TBT_SPI_45S	TBT_SPI	TBT_SPI_CLK	23
SPI_TBT_MOSI	TBT_SPI_45S	TBT_SPI	TBT_SPI_MOSI	23
SPI_TBT_MISO	TBT_SPI_45S	TBT_SPI	TBT_SPI_MISO	23
SPI_TBT_CS_L	TBT_SPI_45S	TBT_SPI	TBT_SPI_CS_L	23
1320 DP_HDMI_TBT_ML	DP_85D	DISPLAYPORT	DP_HDMI_TBT_ML_P<3..0>	64 66
1321 DP_HDMI_TBT_ML	DP_85D	DISPLAYPORT	DP_HDMI_TBT_ML_N<3..0>	64 66
1316 DP_HDMI_TBT_AUX	DP_85D		DP_HDMI_TBT_AUX_P	13 64 66
1317 DP_HDMI_TBT_AUX	DP_85D		DP_HDMI_TBT_AUX_N	13 64 66
1309 HDMI_CLOCK	HDMI_85D	HDMI_CLK	HDMI_IG_CLK_C_P	63 64 68
1308 HDMI_CLOCK	HDMI_85D	HDMI_CLK	HDMI_IG_CLK_C_N	63 64 68
1315 HDMI_DATA	HDMI_85D	HDMI_DATA	HDMI_IG_DATA_C_P<2..0>	63 64 68
1314 HDMI_DATA	HDMI_85D	HDMI_DATA	HDMI_IG_DATA_C_N<2..0>	63 64 68

Thunderbolt, DP, HDMI Net Properties

ELECTRICAL CONST SET	NET TYPE PHYSICAL	NET TYPE SPACING		
TBT_A_R2D	TBTDP_85D	TBTDP_TX	TBT_A_R2D_C_P<1..0>	23 26 68
TBT_A_R2D	TBTDP_85D	TBTDP_TX	TBT_A_R2D_C_N<1..0>	23 26 68
TBT_A_R2D	TBTDP_85D	TBTDP_TX	TBT_A_R2D_P<1..0>	26 68
TBT_A_R2D	TBTDP_85D	TBTDP_TX	TBT_A_R2D_N<1..0>	26 68
DP_A_LSX_ML	DP_85D	DISPLAYPORT	DP_TBTPA_ML_C_P<1>	23 26
DP_A_LSX_ML	DP_85D	DISPLAYPORT	DP_TBTPA_ML_C_N<1>	23 26
DP_A_LSX_ML	DP_85D	DISPLAYPORT	DP_TBTPA_ML_P<1>	26
DP_A_LSX_ML	DP_85D	DISPLAYPORT	DP_TBTPA_ML_N<1>	26
DP_A_LSX_ML	DP_85D	DISPLAYPORT	DP_A_LSX_ML_P<1>	26
DP_A_LSX_ML	DP_85D	DISPLAYPORT	DP_A_LSX_ML_N<1>	26
DP_TBTPA_ML	DP_85D	DISPLAYPORT	DP_TBTPA_ML_C_P<3>	23 26
1355 DP_TBTPA_ML	DP_85D	DISPLAYPORT	DP_TBTPA_ML_C_N<3>	23 26
1354 DP_TBTPA_ML	DP_85D	DISPLAYPORT	DP_TBTPA_ML_P<3>	26
1353 DP_TBTPA_ML	DP_85D	DISPLAYPORT	DP_TBTPA_ML_N<3>	26
1352 DP_TBTPA_ML	DP_85D			
TBT_A_D2R_0	TBTDP_85D	TBTDP_RX	TBT_A_D2R_C_P<0>	26 68
TBT_A_D2R_0	TBTDP_85D	TBTDP_RX	TBT_A_D2R_C_N<0>	26 68
TBT_A_D2R_0	TBTDP_85D	TBTDP_RX	TBT_A_D2R_P<0>	23 26 68
TBT_A_D2R_0	TBTDP_85D	TBTDP_RX	TBT_A_D2R_N<0>	23 26 68
1343 TBT_A_D2R_1	TBTDP_85D	TBTDP_RX	TBT_A_D2R_C_P<1>	26 68
1342 TBT_A_D2R_1	TBTDP_85D	TBTDP_RX	TBT_A_D2R_C_N<1>	26 68
1341 TBT_A_D2R_1	TBTDP_85D	TBTDP_RX	TBT_A_D2R_P<1>	23 26 68
1340 TBT_A_D2R_1	TBTDP_85D	TBTDP_RX	TBT_A_D2R_N<1>	23 26 68
TBT_A_D2R_1	TBTDP_85D	TBTDP_RX	TBT_A_D2R1_AUXDDC_P	26
TBT_A_D2R_1	TBTDP_85D	TBTDP_RX	TBT_A_D2R1_AUXDDC_N	26
DP_TBTPA_AUXCH	DP_85D		DP_TBTPA_AUXCH_C_P	23 26
DP_TBTPA_AUXCH	DP_85D		DP_TBTPA_AUXCH_C_N	23 26
DP_TBTPA_AUXCH	DP_85D		DP_TBTPA_AUXCH_P	26
DP_TBTPA_AUXCH	DP_85D		DP_TBTPA_AUXCH_N	26
TBT_B_R2D	TBTDP_85D	TBTDP_TX	TBT_B_R2D_C_P<1..0>	23 27 68
TBT_B_R2D	TBTDP_85D	TBTDP_TX	TBT_B_R2D_C_N<1..0>	23 27 68
TBT_B_R2D	TBTDP_85D	TBTDP_TX	TBT_B_R2D_P<1..0>	27 68
TBT_B_R2D	TBTDP_85D	TBTDP_TX	TBT_B_R2D_N<1..0>	27 68
DP_B_LSX_ML	DP_85D	DISPLAYPORT	DP_TBTPB_ML_C_P<1>	23 27
DP_B_LSX_ML	DP_85D	DISPLAYPORT	DP_TBTPB_ML_C_N<1>	23 27
DP_B_LSX_ML	DP_85D	DISPLAYPORT	DP_TBTPB_ML_P<1>	27
DP_B_LSX_ML	DP_85D	DISPLAYPORT	DP_TBTPB_ML_N<1>	27
DP_B_LSX_ML	DP_85D	DISPLAYPORT	DP_B_LSX_ML_P<1>	27
DP_B_LSX_ML	DP_85D	DISPLAYPORT	DP_B_LSX_ML_N<1>	27
1351 DP_TBTPB_ML	DP_85D	DISPLAYPORT	DP_TBTPB_ML_C_P<3>	23 27
1350 DP_TBTPB_ML	DP_85D	DISPLAYPORT	DP_TBTPB_ML_C_N<3>	23 27
1348 DP_TBTPB_ML	DP_85D	DISPLAYPORT	DP_TBTPB_ML_P<3>	27
1349 DP_TBTPB_ML	DP_85D	DISPLAYPORT	DP_TBTPB_ML_N<3>	27
TBT_B_D2R_0	TBTDP_85D	TBTDP_RX	TBT_B_D2R_C_P<0>	27 68
TBT_B_D2R_0	TBTDP_85D	TBTDP_RX	TBT_B_D2R_C_N<0>	27 68
TBT_B_D2R_0	TBTDP_85D	TBTDP_RX	TBT_B_D2R_P<0>	23 27 68
TBT_B_D2R_0	TBTDP_85D	TBTDP_RX	TBT_B_D2R_N<0>	23 27 68
1347 TBT_B_D2R_1	TBTDP_85D	TBTDP_RX	TBT_B_D2R_C_P<1>	27 68
1346 TBT_B_D2R_1	TBTDP_85D	TBTDP_RX	TBT_B_D2R_C_N<1>	27 68
1344 TBT_B_D2R_1	TBTDP_85D	TBTDP_RX	TBT_B_D2R_P<1>	23 27 68
1345 TBT_B_D2R_1	TBTDP_85D	TBTDP_RX	TBT_B_D2R_N<1>	23 27 68
TBT_B_D2R_1	TBTDP_85D	TBTDP_RX	TBT_B_D2R1_AUXDDC_P	27
TBT_B_D2R_1	TBTDP_85D	TBTDP_RX	TBT_B_D2R1_AUXDDC_N	27
DP_TBTPB_AUXCH	DP_85D		DP_TBTPB_AUXCH_C_P	23 27
DP_TBTPB_AUXCH	DP_85D		DP_TBTPB_AUXCH_C_N	23 27
DP_TBTPB_AUXCH	DP_85D		DP_TBTPB_AUXCH_P	27
DP_TBTPB_AUXCH	DP_85D		DP_TBTPB_AUXCH_N	27
1338 DP_TBTSNK0_ML	DP_85D	DISPLAYPORT	DP_TBTSNK0_ML_C_P<3..0>	5 23
1339 DP_TBTSNK0_ML	DP_85D	DISPLAYPORT	DP_TBTSNK0_ML_C_N<3..0>	5 23
1336 DP_TBTSNK0_ML	DP_85D	DISPLAYPORT	DP_TBTSNK0_ML_P<3..0>	23
1337 DP_TBTSNK0_ML	DP_85D	DISPLAYPORT	DP_TBTSNK0_ML_N<3..0>	23
1335 DP_TBTSNK_AUXCH	DP_85D		DP_TBTSNK0_AUXCH_C_P	13 23
1334 DP_TBTSNK_AUXCH	DP_85D		DP_TBTSNK0_AUXCH_C_N	13 23
1324 DP_TBTSNK_AUXCH	DP_85D		DP_TBTSNK0_AUXCH_P	23
1333 DP_TBTSNK_AUXCH	DP_85D		DP_TBTSNK0_AUXCH_N	23
1332 DP_TBTSNK1_ML	DP_85D	DISPLAYPORT	DP_TBTSNK1_ML_C_P<3..0>	23 64
1330 DP_TBTSNK1_ML	DP_85D	DISPLAYPORT	DP_TBTSNK1_ML_C_N<3..0>	23 64
1331 DP_TBTSNK1_ML	DP_85D	DISPLAYPORT	DP_TBTSNK1_ML_P<3..0>	23
1328 DP_TBTSNK1_ML	DP_85D	DISPLAYPORT	DP_TBTSNK1_ML_N<3..0>	23
1329 DP_TBTSNK_AUXCH	DP_85D		DP_TBTSNK1_AUXCH_C_P	23 64
1327 DP_TBTSNK_AUXCH	DP_85D		DP_TBTSNK1_AUXCH_C_N	23 64
1325 DP_TBTSNK_AUXCH	DP_85D		DP_TBTSNK1_AUXCH_P	23
1326 DP_TBTSNK_AUXCH	DP_85D		DP_TBTSNK1_AUXCH_N	23
1316 DP_INT_ML	DP_85D	DISPLAYPORT	DP_INT_ML_C_P<3..0>	5 62
1317 DP_INT_ML	DP_85D	DISPLAYPORT	DP_INT_ML_C_N<3..0>	5 62
1318 DP_INT_ML	DP_85D	DISPLAYPORT	DP_INT_ML_P<3..0>	62 68
1319 DP_INT_ML	DP_85D	DISPLAYPORT	DP_INT_ML_N<3..0>	62 68
1320 DP_INT_AUXCH	DP_85D		DP_INT_AUXCH_C_P	5 62
1321 DP_INT_AUXCH	DP_85D		DP_INT_AUXCH_C_N	5 62
1322 DP_INT_AUXCH	DP_85D		DP_INT_AUX_P	62 68
1323 DP_INT_AUXCH	DP_85D		DP_INT_AUX_N	62 68

Only used on dual-port hosts.

Notes:
AUX and DDC was removed from DISPLAYPORT or TBTDP_RX/TX because it's not high speed, and to save routing space.

SYNC_MASTER=J44 SYNC_DATE=08/12/2013

PAGE TITLE: TBT,DP,HDMI Constraints

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D
REVISION: <E4LABEL>
BRANCH: <BRANCH>
PAGE: 115 OF 120
SHEET: 74 OF 78

MIPI Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MIPI_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MIPI_2OTHER	*	=4X_DIELECTRIC	?
MIPI_2CLK	*	=6X_DIELECTRIC	?
MIPICLK_2OTHER	*	=7X_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MIPI_2OTHER	TOP,BOTTOM	=6X_DIELECTRIC	?
MIPI_2CLK	TOP,BOTTOM	=8X_DIELECTRIC	?
MIPICLK_2OTHER	TOP,BOTTOM	=10X_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MIPI_DATA	*	*	MIPI_2OTHER
MIPI_DATA	CLK_MIPI	*	MIPI_2CLK
CLK_MIPI	*	*	MIPICLK_2OTHER

Memory Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
S2_MEM_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
S2_MEM_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

Spacing Rule Sets

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
S2_DATA2SELF	*	=2x_DIELECTRIC	?
S2_DQS2OWNDATA	*	=2x_DIELECTRIC	?
S2_CMD2CMD	*	=2x_DIELECTRIC	?
S2_CMD2CTRL	*	=2x_DIELECTRIC	?
S2_CTRL2CTRL	*	=2x_DIELECTRIC	?
S2_2OTHERMEM	*	=4x_DIELECTRIC	?
S2MEM_2PWR	*	=2x_DIELECTRIC	?
S2MEM_2GND	*	=2x_DIELECTRIC	?
S2MEM_2OTHER	*	=6x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
S2_DATA2SELF	TOP,BOTTOM	=4x_DIELECTRIC	?
S2_DQS2OWNDATA	TOP,BOTTOM	=4x_DIELECTRIC	?
S2_CMD2CMD	TOP,BOTTOM	=4x_DIELECTRIC	?
S2_CMD2CTRL	TOP,BOTTOM	=4x_DIELECTRIC	?
S2_CTRL2CTRL	TOP,BOTTOM	=4x_DIELECTRIC	?
S2_2OTHERMEM	TOP,BOTTOM	=6x_DIELECTRIC	?
S2MEM_2PWR	TOP,BOTTOM	=4x_DIELECTRIC	?
S2MEM_2GND	TOP,BOTTOM	=4x_DIELECTRIC	?
S2MEM_2OTHER	TOP,BOTTOM	=10x_DIELECTRIC	?

Memory Bus Spacing Group Assignments

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
S2_MEM_DATA*	*	*	S2MEM_2OTHER
S2_MEM_DQS*	*	*	S2MEM_2OTHER
S2_MEM_CMD	*	*	S2MEM_2OTHER
S2_MEM_CTRL	*	*	S2MEM_2OTHER
S2_MEM_CLK	*	*	S2MEM_2OTHER
S2_MEM_DATA*	=SAME	*	S2_DATA2SELF
S2_MEM_CMD	S2_MEM_CMD	*	S2_CMD2CMD
S2_MEM_CMD	S2_MEM_CTRL	*	S2_CMD2CTRL
S2_MEM_CTRL	S2_MEM_CTRL	*	S2_CTRL2CTRL
S2_MEM_*	S2_MEM_*	*	S2_2OTHERMEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
S2_MEM_DQS1	S2_MEM_DATA1	*	S2_DQS2OWNDATA
S2_MEM_DQS0	S2_MEM_DATA0	*	S2_DQS2OWNDATA

Memory to Power Spacing

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
S2_MEM_PWR	S2_MEM_*	*	S2MEM_2PWR
S2_MEM_PWR	*	*	DEFAULT

Memory to GND Spacing

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
GND	S2_MEM_*	*	S2MEM_2GND

Camera Net Properties

ELECTRICAL CONST SET	NET TYPE: PHYSICAL	NET TYPE: SPACING	
S2_MEM_CLK	S2_MEM_85D	S2_MEM_CLK	MEM_CAM_CLK_P 31 32
S2_MEM_CLK	S2_MEM_85D	S2_MEM_CLK	MEM_CAM_CLK_N 31 32
S2_MEM_CKE	S2_MEM_45S	S2_MEM_CTRL	MEM_CAM_CKE 31 32
S2_MEM_CS	S2_MEM_45S	S2_MEM_CTRL	MEM_CAM_CS_L 31 32
	S2_MEM_45S	S2_MEM_CTRL	MEM_CAM_ODT 32
S2_MEM_CMD	S2_MEM_45S	S2_MEM_CTRL	MEM_CAM_CAS_L 31 32
S2_MEM_CMD	S2_MEM_45S	S2_MEM_CTRL	MEM_CAM_RAS_L 31 32
S2_MEM_CMD	S2_MEM_45S	S2_MEM_CMD	MEM_CAM_WE_L 31 32
S2_MEM_CMD	S2_MEM_45S	S2_MEM_CMD	MEM_CAM_BA<0> 31 32
S2_MEM_CMD	S2_MEM_45S	S2_MEM_CMD	MEM_CAM_BA<1> 31 32
S2_MEM_CMD	S2_MEM_45S	S2_MEM_CMD	MEM_CAM_BA<2> 31 32
S2_MEM_DQS0	S2_MEM_85D	S2_MEM_DQS0	MEM_CAM_DQS_P<0> 31 32
S2_MEM_DQS0	S2_MEM_85D	S2_MEM_DQS0	MEM_CAM_DQS_N<0> 31 32
S2_MEM_DQS1	S2_MEM_85D	S2_MEM_DQS1	MEM_CAM_DQS_P<1> 31 32
S2_MEM_DQS1	S2_MEM_85D	S2_MEM_DQS1	MEM_CAM_DQS_N<1> 31 32
S2_MEM_DATA_0	S2_MEM_45S	S2_MEM_DATA0	MEM_CAM_DM<0> 31 32
S2_MEM_DATA_1	S2_MEM_45S	S2_MEM_DATA1	MEM_CAM_DM<1> 31 32
S2_MEM_A	S2_MEM_45S	S2_MEM_CMD	MEM_CAM_A<14..0> 31 32
S2_MEM_DATA_0	S2_MEM_45S	S2_MEM_DATA0	MEM_CAM_DQ<7..0> 31 32
S2_MEM_DATA_1	S2_MEM_45S	S2_MEM_DATA1	MEM_CAM_DQ<15..8> 31 32
MIPI_DATA_S2	MIPI_85D	MIPI_DATA	MIPI_DATA_P 31 32 68
MIPI_DATA_S2	MIPI_85D	MIPI_DATA	MIPI_DATA_N 31 32 68
MIPI_DATA_S2	MIPI_85D	MIPI_DATA	MIPI_DATA_CONN_P 32 68
MIPI_DATA_S2	MIPI_85D	MIPI_DATA	MIPI_DATA_CONN_N 32 68
MIPI_CLK_S2	MIPI_85D	CLK_MIPI	MIPI_CLK_P 31 32 68
MIPI_CLK_S2	MIPI_85D	CLK_MIPI	MIPI_CLK_N 31 32 68
MIPI_CLK_S2	MIPI_85D	CLK_MIPI	MIPI_CLK_CONN_P 32 68
MIPI_CLK_S2	MIPI_85D	CLK_MIPI	MIPI_CLK_CONN_N 32 68
		S2_MEM_PWR	PP1V35_CAM 31 32
		S2_MEM_PWR	PP0V675_CAM_VREF 31 32
		S2_MEM_PWR	PP0V675_MEM_CAM_VREFCA 32
		S2_MEM_PWR	PP0V675_MEM_CAM_VREFDQ 32

SYNC_MASTER=J44 SYNC_DATE=08/12/2013

PAGE TITLE: Camera Constraints

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

REVISION: <E4LABEL>

BRANCH: <BRANCH>

PAGE: 116 OF 120

SHEET: 75 OF 78

SMC SMBus & Charger Net Properties

ELECTRICAL CONST SET	NET TYPE PHYSICAL	NET TYPE SPACING		
SMBUS_SMC_2	SMB_45S	SMB	SMBUS_SMC_2_S3_SCL	34 36 39 68
SMBUS_SMC_2	SMB_45S	SMB	SMBUS_SMC_2_S3_SDA	34 36 39 68
SMBUS_SMC_1	SMB_45S	SMB	SMBUS_SMC_1_S0_SCL	14 32 36 39 43 68 72
SMBUS_SMC_1	SMB_45S	SMB	SMBUS_SMC_1_S0_SDA	14 32 36 39 43 68 72
SMBUS_SMC_0	SMB_45S	SMB	SMBUS_SMC_0_S0_SCL	36 39 62 68
SMBUS_SMC_0	SMB_45S	SMB	SMBUS_SMC_0_S0_SDA	36 39 62 68
SMBUS_SMC_5	SMB_45S	SMB	SMBUS_SMC_5_G3_SCL	36 39 51 52 68
SMBUS_SMC_5	SMB_45S	SMB	SMBUS_SMC_5_G3_SDA	36 39 51 52 68
SMBUS_SMC_3	SMB_45S	SMB	SMBUS_SMC_3_SCL	36 39 43 63
SMBUS_SMC_3	SMB_45S	SMB	SMBUS_SMC_3_SDA	36 39 43 63

SYNC_MASTER=J44 SYNC_DATE=08/12/2013

PAGE TITLE

SMC Constraints

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

REVISION <E4LABEL>

BRANCH <BRANCH>

PAGE 117 OF 120

SHEET 76 OF 78

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SENSE_45S	*	=1TO1_DIFFPAIR	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	0.1 MM	0.1 MM
THERM_45S	*	=1TO1_DIFFPAIR	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	0.1 MM	0.1 MM
DIG_AUDIO	*	=1TO1_DIFFPAIR	=1TO1_DIFFPAIR	=1TO1_DIFFPAIR	=1TO1_DIFFPAIR	0.1 MM	0.1 MM
ANL_AUDIO	*	=1TO1_DIFFPAIR	0.1 MM	0.1 MM	10 MM	0.1 MM	0.1 MM
ANL_AUDIO_WIDE	*	=1TO1_DIFFPAIR	0.3 MM	0.3 MM	10 MM	0.1 MM	0.1 MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SENSE	*	=2X_DIELECTRIC	?
THERM	*	=2X_DIELECTRIC	?
AUDIO	*	=2X_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CPU_VCCSENSE	GND	*	GND_P2MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND	*	=STANDARD	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLK_PCIE	GND	*	GND_P2MM
GND	PCIE_*	*	GND_P2MM
GND	SATA_*	*	GND_P2MM
USB	GND	*	GND_P2MM
CLK_PCIE	SB_POWER	*	PWR_P2MM
SB_POWER	SATA_*	*	PWR_P2MM
USB	SB_POWER	*	PWR_P2MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND_P2MM	*	0.20 MM	1000
PWR_P2MM	*	0.20 MM	1000

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_45S OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.070 MM OVERRIDE	100 MIL OVERRIDE	OVERRIDE	OVERRIDE
MEM_40S OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.090 MM OVERRIDE	100 MIL OVERRIDE	OVERRIDE	OVERRIDE
MEM_72D OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.090 MM OVERRIDE	100 MIL OVERRIDE	OVERRIDE	OVERRIDE
MEM_85D OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.090 MM OVERRIDE	100 MIL OVERRIDE	OVERRIDE	OVERRIDE
PCIE_85D OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.090 MM OVERRIDE	10 MM OVERRIDE	OVERRIDE	OVERRIDE
USB_85D	TOP			0.100 MM	500 MIL		
CPU_27P4S	BOTTOM			0.230 MM	100 MIL		
USB3_85D	TOP			0.100 MM	500 MIL		
USB3_85D	ISL10			0.075 MM			0.090 MM
DP_85D	ISL9			0.075 MM			0.090 MM
PCIE_85D	ISL10			0.075 MM			0.090 MM

DDR3 Loaded Segment Constraint Relaxations

Alternate single ended and differential impedances between devices.

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
MEM_40S	BGA_MEM	MEM_45S
MEM_72D	BGA_MEM	MEM_85D

Allow 0.127 mm necks for >0.127 mm lines for ARD fanout.

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_72D	BOTTOM			0.127 MM	6.35 MM		
MEM_85D	TOP			0.100 MM	6.35 MM		

DP, SATA, HDMI, PCIE CONSTRAINT RELAXATIONS

Alternate diffpair width/gap through BGA fanout areas (95-ohm diff)

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
DP_85D	BGA	P65_BGA
PCIE_85D	BGA	P65_BGA
CLK_PCIE_85D	BGA	P65_BGA
HDMI_85D	BGA	P65_BGA

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
SENSE_45S	*	SENSE_45S
THERM_45S	*	THERM_45S
DIG_AUDIO	*	DIG_AUDIO
ANL_AUDIO	*	ANL_AUDIO
1TO1_DIFFPAIR	*	1TO1_DIFFPAIR

J44 Specific Net Properties

ELECTRICAL CONST SET	NET TYPE PHYSICAL	NET TYPE SPACING	
THERM_DP_TBT_D1	THERM_45S	THERM	TBTTHMSNS_D1_P 23 43
THERM_DP_TBT_D1	THERM_45S	THERM	TBTTHMSNS_D1_N 43
THERM_DP_CPU_D1	THERM_45S	THERM	CPUTHMSNS_D1_P 43
THERM_DP_CPU_D1	THERM_45S	THERM	CPUTHMSNS_D1_N 43
THERM_DP_CPU_D2	THERM_45S	THERM	CPUTHMSNS_D2_P 43
THERM_DP_CPU_D2	THERM_45S	THERM	CPUTHMSNS_D2_N 43
	SENSE_45S	SENSE	NC_ISNS_CAMERAP 42
	SENSE_45S	SENSE	NC_ISNS_CAMERAN 42
SENSE_DP	SENSE_45S	SENSE	ISNS_CPUDDR_P 41
SENSE_DP	SENSE_45S	SENSE	ISNS_CPUDDR_N 41
SENSE_DP_LCDBKLT	SENSE_45S	SENSE	ISNS_LCDBKLT_P 40 58
SENSE_DP_LCDBKLT	SENSE_45S	SENSE	ISNS_LCDBKLT_N 40 58
SENSE_DP_TBT	SENSE_45S	SENSE	ISNS_TBT_P 42
SENSE_DP_TBT	SENSE_45S	SENSE	ISNS_TBT_N 42
SENSE_DP	SENSE_45S	SENSE	ISNS_LCDPANEL_P 42 62
SENSE_DP	SENSE_45S	SENSE	ISNS_LCDPANEL_N 42 62
SENSE_DP	SENSE_45S	SENSE	ISNS_HS_COMPUTING_P 40 42
SENSE_DP	SENSE_45S	SENSE	ISNS_HS_COMPUTING_N 40 42
SENSE_DP	SENSE_45S	SENSE	ISNS_HS_OTHER5V_P 40
SENSE_DP	SENSE_45S	SENSE	ISNS_HS_OTHER5V_N 40
SENSE_DP	SENSE_45S	SENSE	ISNS_HS_OTHER3V3_P 40
SENSE_DP	SENSE_45S	SENSE	ISNS_HS_OTHER3V3_N 40
SENSE_DP_CPUVR	SENSE_45S	SENSE	CPUVR_ISNS_P 41
SENSE_DP_CPUVR	SENSE_45S	SENSE	CPUVR_ISNS_N 41
SENSE_DP_CPUVR	SENSE_45S	SENSE	CPUVR_ISNS_R_P 41
SENSE_DP_CPUVR	SENSE_45S	SENSE	CPUVR_ISNS_R_N 41
	SENSE_45S	SENSE	CPUVR_ISNS1_P 41 54
	SENSE_45S	SENSE	CPUVR_ISNS1_N 41 54
	SENSE_45S	SENSE	CPUVR_ISNS2_P 41 54
	SENSE_45S	SENSE	CPUVR_ISNS2_N 41 54
SENSE_DP	SENSE_45S	SENSE	ISNS_1V05_S0_P 41 57
SENSE_DP	SENSE_45S	SENSE	ISNS_1V05_S0_N 41 57
SENSE_DP	SENSE_45S	SENSE	ISNS_SSD_P 41
SENSE_DP	SENSE_45S	SENSE	ISNS_SSD_N 41
SENSE_DP	SENSE_45S	SENSE	ISNS_TPAD_P
SENSE_DP	SENSE_45S	SENSE	ISNS_TPAD_N
	SENSE_45S	SENSE	NC_ISNS_DDR_S3P 41 55
	SENSE_45S	SENSE	NC_ISNS_DDR_S3N 41 55
SENSE_DP	SENSE_45S	SENSE	ISNS_PP3V3S0_P 41
SENSE_DP	SENSE_45S	SENSE	ISNS_PP3V3S0_N 41
SENSE_DP	SENSE_45S	SENSE	ISNS_PP5VS0_P 41
SENSE_DP	SENSE_45S	SENSE	ISNS_PP5VS0_N 41
SENSE_DP_CPUHIGAIN	SENSE_45S	SENSE	ISNS_CPUHIGAIN_P 42 43
SENSE_DP_CPUHIGAIN	SENSE_45S	SENSE	ISNS_CPUHIGAIN_N 42 43
SENSE_DP_CPUHIGAIN	SENSE_45S	SENSE	ISNS_CPUHIGAIN_R_P 42
SENSE_DP_CPUHIGAIN	SENSE_45S	SENSE	ISNS_CPUHIGAIN_R_N 42
SENSE_DP_CHGR_CSI	SENSE_45S	SENSE	CHGR_CSI_P 52
SENSE_DP_CHGR_CSI	SENSE_45S	SENSE	CHGR_CSI_N 52
SENSE_DP_CHGR_CSI	SENSE_45S	SENSE	CHGR_CSI_R_P 52
SENSE_DP_CHGR_CSI	SENSE_45S	SENSE	CHGR_CSI_R_N 52
SENSE_DP_CHGR_CSO	SENSE_45S	SENSE	CHGR_CSO_P 52
SENSE_DP_CHGR_CSO	SENSE_45S	SENSE	CHGR_CSO_N 52
SENSE_DP_CHGR_CSO	SENSE_45S	SENSE	CHGR_CSO_R_P 42 52
SENSE_DP_CHGR_CSO	SENSE_45S	SENSE	CHGR_CSO_R_N 42 52

J44 Specific Net Properties

ELECTRICAL CONST SET	NET TYPE PHYSICAL	NET TYPE SPACING	
AUDIO_DP_AMPTWT	ANL_AUDIO	AUDIO	AUD_LO2_L_P 46 48
AUDIO_DP_AMPTWT	ANL_AUDIO	AUDIO	AUD_LO2_L_N 46 48
AUDIO_DP_AMPTWT	ANL_AUDIO	AUDIO	AUD_SPKRAMP_LIN_P 48
AUDIO_DP_AMPTWT	ANL_AUDIO	AUDIO	AUD_SPKRAMP_LIN_N 48
AUDIO_DP_AMPTWT	ANL_AUDIO	AUDIO	SPKRAMP_LIN_P 48
AUDIO_DP_AMPTWT	ANL_AUDIO	AUDIO	SPKRAMP_LIN_N 48
AUDIO_DP_AMPTWT	ANL_AUDIO	AUDIO	AUD_LO2_R_P 46 48
AUDIO_DP_AMPTWT	ANL_AUDIO	AUDIO	AUD_LO2_R_N 46 48
AUDIO_DP_AMPTWT	ANL_AUDIO	AUDIO	AUD_SPKRAMP_RIN_P 48
AUDIO_DP_AMPTWT	ANL_AUDIO	AUDIO	AUD_SPKRAMP_RIN_N 48
AUDIO_DP_AMPTWT	ANL_AUDIO	AUDIO	SPKRAMP_RIN_P 48
AUDIO_DP_AMPTWT	ANL_AUDIO	AUDIO	SPKRAMP_RIN_N 48
AUDIO_DP_AMPSUB	ANL_AUDIO	AUDIO	AUD_LO3_L_P 46 48
AUDIO_DP_AMPSUB	ANL_AUDIO	AUDIO	AUD_LO3_L_N 46 48
AUDIO_DP_AMPSUB	ANL_AUDIO	AUDIO	AUD_SPKRAMP_LSUBIN_P 48
AUDIO_DP_AMPSUB	ANL_AUDIO	AUDIO	AUD_SPKRAMP_LSUBIN_N 48
AUDIO_DP_AMPSUB	ANL_AUDIO	AUDIO	LSUBIN_P 48
AUDIO_DP_AMPSUB	ANL_AUDIO	AUDIO	LSUBIN_N 48
AUDIO_DP_AMPSUB	ANL_AUDIO	AUDIO	AUD_LO3_R_P 46 48
AUDIO_DP_AMPSUB	ANL_AUDIO	AUDIO	AUD_LO3_R_N 46 48
AUDIO_DP_AMPSUB	ANL_AUDIO	AUDIO	AUD_SPKRAMP_RSUBIN_P 48
AUDIO_DP_AMPSUB	ANL_AUDIO	AUDIO	AUD_SPKRAMP_RSUBIN_N 48
AUDIO_DP_AMPSUB	ANL_AUDIO	AUDIO	RSUBIN_P 48
AUDIO_DP_AMPSUB	ANL_AUDIO	AUDIO	RSUBIN_N 48
AUDIO_DP_SPKSUB	DIG_AUDIO	AUDIO	SPKRCONN_SL_OUT_P 48 50 68
AUDIO_DP_SPKSUB	DIG_AUDIO	AUDIO	SPKRCONN_SL_OUT_N 48 50 68
AUDIO_DP_SPKSUB	DIG_AUDIO	AUDIO	SPKRCONN_SR_OUT_P 48 50 68
AUDIO_DP_SPKSUB	DIG_AUDIO	AUDIO	SPKRCONN_SR_OUT_N 48 50 68
AUDIO_DP_SPKTWT	DIG_AUDIO	AUDIO	SPKRCONN_L_OUT_P 48 50 68
AUDIO_DP_SPKTWT	DIG_AUDIO	AUDIO	SPKRCONN_L_OUT_N 48 50 68
AUDIO_DP_SPKTWT	DIG_AUDIO	AUDIO	SPKRCONN_R_OUT_P 48 50 68
AUDIO_DP_SPKTWT	DIG_AUDIO	AUDIO	SPKRCONN_R_OUT_N 48 50 68
AUDIO_DP_MIC	ANL_AUDIO_WIDE	AUDIO	AUD_CH_HS_GND 46 50
AUDIO_DP_MIC	ANL_AUDIO_WIDE	AUDIO	AUD_CONN_HS_MIC_P
AUDIO_DP_MIC	ANL_AUDIO_WIDE	AUDIO	AUD_CONN_SLEEVE 50
AUDIO_DP_MIC	ANL_AUDIO_WIDE	AUDIO	AUD_CONN_SLEEVE_XW 49 50
AUDIO_DP_MIC	ANL_AUDIO_WIDE	AUDIO	AUD_HP_PORT_REFCH 46 50
AUDIO_DP_MIC	ANL_AUDIO_WIDE	AUDIO	AUD_HS_MIC_P 49 50
AUDIO_DP_MIC	ANL_AUDIO_WIDE	AUDIO	CODEC_HS_MIC_P 46
AUDIO_DP_MIC	ANL_AUDIO_WIDE	AUDIO	HS_MIC_P 46 49
AUDIO_DP_MIC	ANL_AUDIO_WIDE	AUDIO	AUD_CONN_HS_MIC_N
AUDIO_DP_MIC	ANL_AUDIO_WIDE	AUDIO	AUD_CONN_RING2 50
AUDIO_DP_MIC	ANL_AUDIO_WIDE	AUDIO	AUD_CONN_RING2_XW 49 50
AUDIO_DP_MIC	ANL_AUDIO_WIDE	AUDIO	AUD_HP_PORT_REFUS 46 50
AUDIO_DP_MIC	ANL_AUDIO_WIDE	AUDIO	AUD_HS_MIC_N 49 50
AUDIO_DP_MIC	ANL_AUDIO_WIDE	AUDIO	AUD_US_HS_GND 46 50
AUDIO_DP_MIC	ANL_AUDIO_WIDE	AUDIO	HS_MIC_N 46 49
AUDIO_DP_MIC	ANL_AUDIO_WIDE	AUDIO	CODEC_HS_MIC_N 46
		SB_POWER	PP3V3_S5 8 11 13 15 16 17 18 20 27 29 56 59 60 61 65 68
		SB_POWER	PP3V3_S0 61 62 64 65 68 8 11 13 15 16 17 18 24 28 30 37 38 39 40 41 42 43 44 46 47 50
		GND	GND

SYNC_MASTER=J44 SYNC_DATE=08/12/2013

PAGE TITLE

Project Specific Constraints

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

REVISION <E4LABEL>

BRANCH <BRANCH>

PAGE 118 OF 120

SHEET 77 OF 78

Change List:
<RDAR://COMPONENT/XXXXXX> J44 HW EE SCHEMATIC | PROTO 0

Kismet:
AFP://KISMET.APPLE.COM/KISMET-PROJECTS/J44

Useful Wiki Links:
Schematic Conventions - https://hmts.ecs.apple.com/wiki/index.php/User:Wferry/SchConventions
Schematic Design Wiki - https://hmts.ecs.apple.com/wiki/index.php/Schematic_Design

MobileMac HW Radar:
<rdar://component/497591> MobileMac HW | Task
<rdar://component/497587> MobileMac HW | Schematic
<rdar://component/497585> MobileMac HW | New Bugs
<rdar://component/497588> MobileMac HW | Layout
<rdar://component/497590> MobileMac HW | Investigation
<rdar://component/497589> MobileMac HW | Architecture

Other Info:
Page Allocations - <rdar://problem/11791318> 2012 Schematic Page Allocations

SYNC_MASTER=J44 SYNC_DATE=08/12/2013

PAGE TITLE: Reference

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D
REVISION: <E4LABEL>
BRANCH: <BRANCH>
PAGE: 120 OF 120
SHEET: 78 OF 78