

TS256MLQ64V5U TS128MLQ64V6U
TS256MLQ64V6U TS128MLQ64V8U
TS256MLQ64V8U

240Pin DDR2 533/667/800 UDIMM
1GB~2GB Based on 128Mx8

Description

DDR2 Unbuffered DIMM is high-speed, low power memory module that use 128Mx8bits DDR2 SDRAM in FBGA package and a 2048 bits serial EEPROM on a 240-pin printed circuit board. DDR2 Unbuffered DIMM is a Dual In-Line Memory Module and is intended for mounting into 240-pin edge connector sockets.

Synchronous design allows precise cycle control with the use of system clock. Data I/O transactions are possible on both edges of DQS. Range of operation frequencies, programmable latencies allow the same device to be useful for a variety of high bandwidth, high performance memory system applications.

Features

- RoHS compliant products.
- JEDEC standard 1.8V ± 0.1V Power supply
- VDDQ=1.8V ± 0.1V
- Max clock Freq: 266MHZ; 533Mb/s/Pin.
- Max clock Freq: 333MHZ; 667Mb/s/Pin.
- Max clock Freq: 400MHZ; 800Mb/s/Pin.
- Posted CAS
- Programmable CAS Latency: 3,4,5,6
- Programmable Additive Latency : :0, 1, 2, 3, 4, 5
- Write Latency (WL) = Read Latency (RL)-1
- Burst Length: 4,8(Interleave/nibble sequential)
- Programmable sequential / Interleave Burst Mode
- Bi-directional Differential Data-Strobe (Single-ended data-strobe is an optional feature)
- Off-Chip Driver (OCD) Impedance Adjustment
- MRS cycle with address key programs.
- On Die Termination
- Serial presence detect with EEPROM

Pin Identification

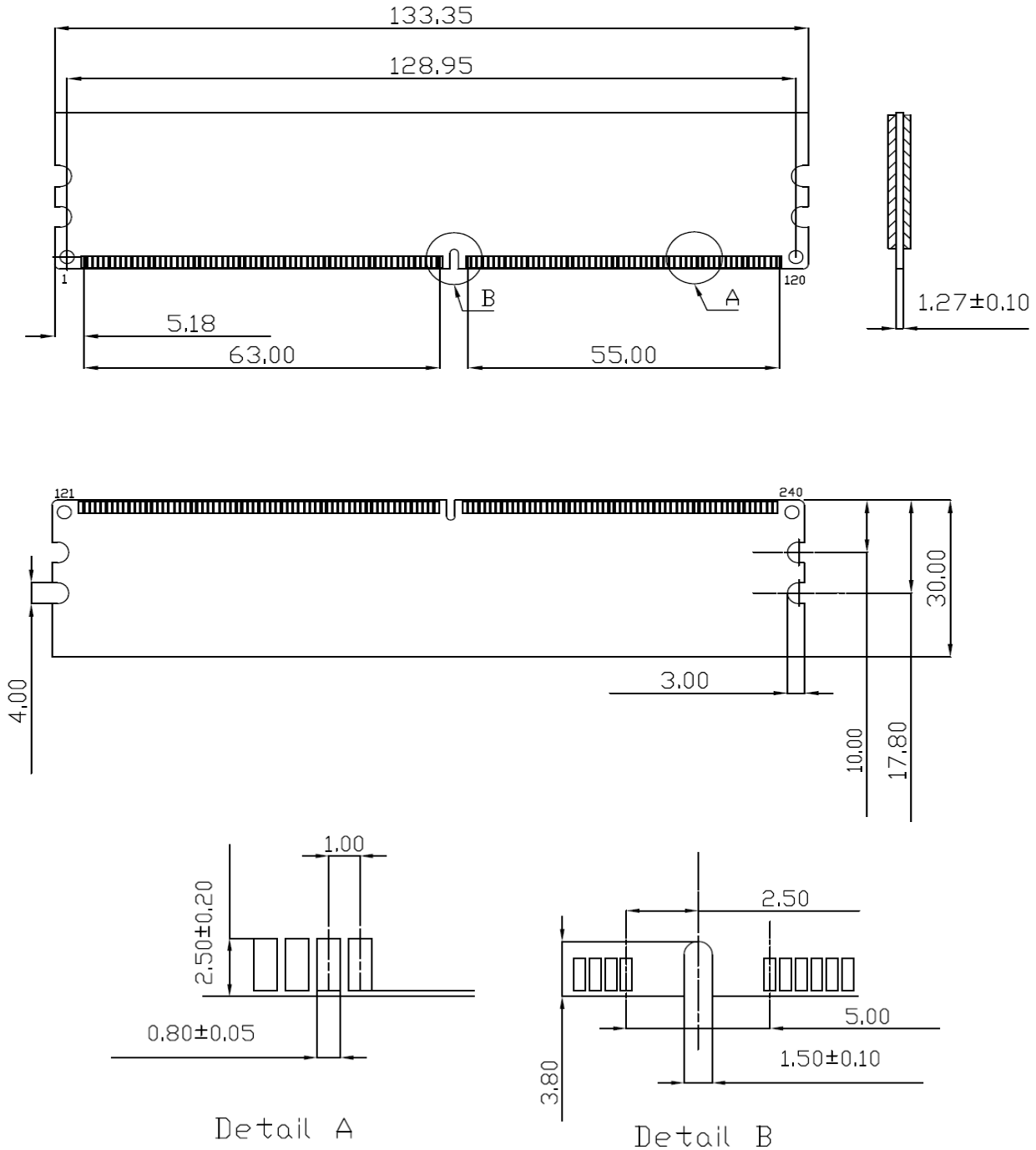
Symbol	Function
A0~A13, BA0~BA2	Address input
DQ0~DQ63	Data Input / Output.
DQS0~DQS8	Data strobe
/DQS0~/DQS8	Differential Data strobe
CK0, /CK0 CK1, /CK1 CK2, /CK2	Clock Input.
CKE0, CKE1	Clock Enable Input.
ODT0, ODT1	On-die termination control line
/CS0, /CS1	Chip Select Input.
/RAS	Row Address Strobe
/CAS	Column Address Strobe
/WE	Write Enable
DM0~DM8	Data-in Mask
VDD	+1.8 Voltage power supply
VDDQ	+1.8 Voltage Power Supply for DQS
VREF	Power Supply for Reference
VDDSPD	Serial EEPROM Positive Power Supply
SA0~SA2	Address select for EEPROM
SCL	Serial PD Clock
SDA	Serial PD Add/Data input/output
VSS	Ground
NC	No Connection

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Dimensions (Normal Profile, Unit: millimeter)



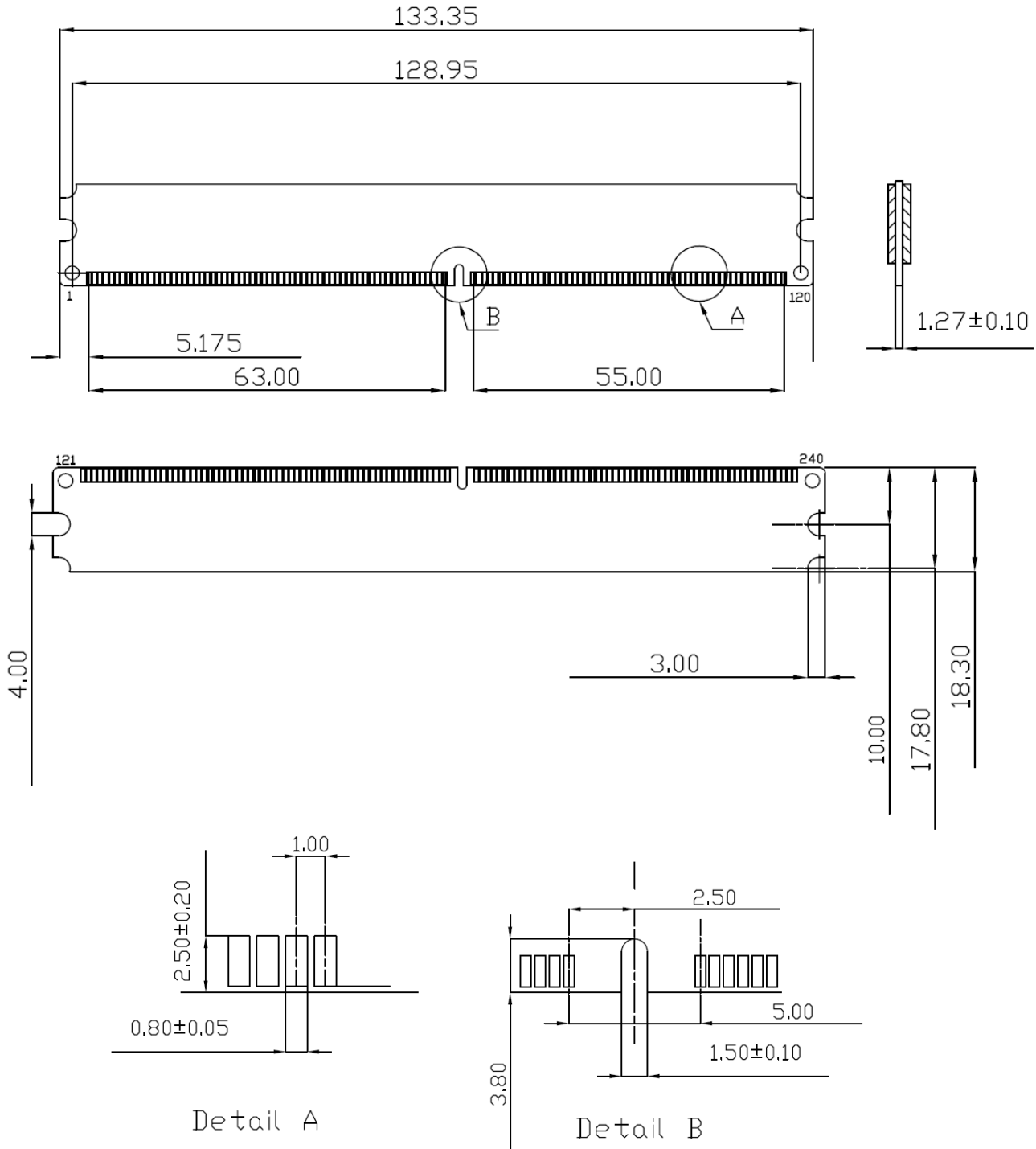
Note:
 1. Tolerances on all dimensions +/-0.15mm unless otherwise specified.

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Dimensions (Very Low Profile, Unit: millimeter)



Note:

1. Tolerances on all dimensions +/-0.15mm unless otherwise specified.

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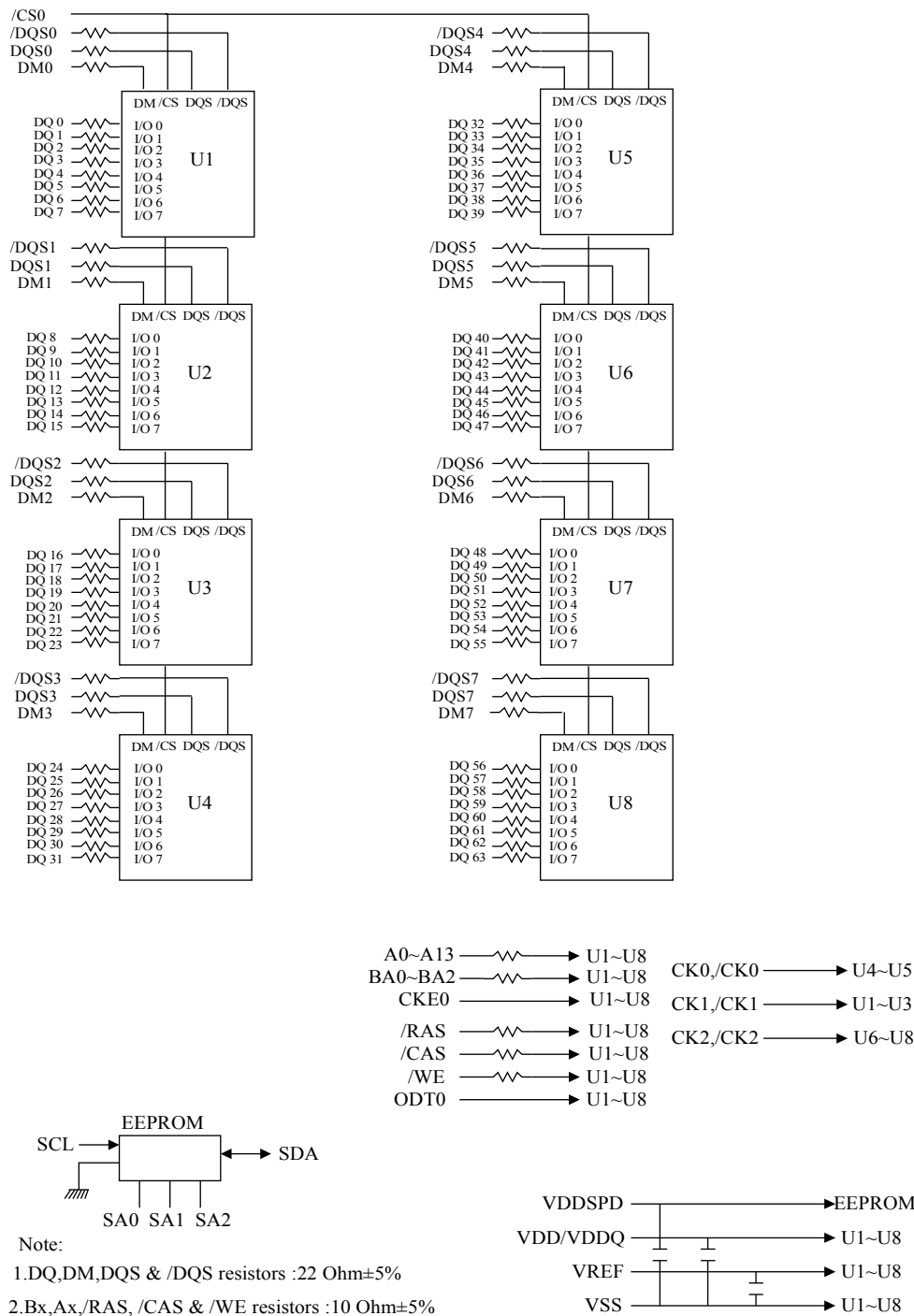
Pin Assignments

Pin No	Pin Name	Pin No	Pin Name	Pin No	Pin Name	Pin No	Pin Name	Pin No	Pin Name	Pin No	Pin Name
01	VREF	41	VSS	81	DQ33	121	VSS	161	NC	201	VSS
02	VSS	42	NC	82	VSS	122	DQ4	162	NC	202	DM4
03	DQ0	43	NC	83	/DQS4	123	DQ5	163	VSS	203	NC
04	DQ1	44	VSS	84	DQS4	124	VSS	164	NC	204	VSS
05	VSS	45	NC	85	VSS	125	DM0	165	NC	205	DQ38
06	/DQS0	46	NC	86	DQ34	126	NC	166	VSS	206	DQ39
07	DQS0	47	VSS	87	DQ35	127	VSS	167	NC	207	VSS
08	VSS	48	NC	88	VSS	128	DQ6	168	NC	208	DQ44
09	DQ2	49	NC	89	DQ40	129	DQ7	169	VSS	209	DQ45
10	DQ3	50	VSS	90	DQ41	130	VSS	170	VDDQ	210	VSS
11	VSS	51	VDDQ	91	VSS	131	DQ12	171	CKE1	211	DM5
12	DQ8	52	CKE0	92	/DQS5	132	DQ13	172	VDD	212	NC
13	DQ9	53	VDD	93	DQS5	133	VSS	173	NC	213	VSS
14	VSS	54	BA2	94	VSS	134	DM1	174	NC	214	DQ46
15	/DQS1	55	NC	95	DQ42	135	NC	175	VDDQ	215	DQ47
16	DQS1	56	VDDQ	96	DQ43	136	VSS	176	A12	216	VSS
17	VSS	57	A11	97	VSS	137	CK1	177	A9	217	DQ52
18	NC	58	A7	98	DQ48	138	/CK1	178	VDD	218	DQ53
19	NC	59	VDD	99	DQ49	139	VSS	179	A8	219	VSS
20	VSS	60	A5	100	VSS	140	DQ14	180	A6	220	CK2
21	DQ10	61	A4	101	SA2	141	DQ15	181	VDDQ	221	/CK2
22	DQ11	62	VDDQ	102	NC	142	VSS	182	A3	222	VSS
23	VSS	63	A2	103	VSS	143	DQ20	183	A1	223	DM6
24	DQ16	64	VDD	104	/DQS6	144	DQ21	184	VDD	224	NC
25	DQ17	65	VSS	105	DQS6	145	VSS	185	CK0	225	VSS
26	VSS	66	VSS	106	VSS	146	DM2	186	/CK0	226	DQ54
27	/DQS2	67	VDD	107	DQ50	147	NC	187	VDD	227	DQ55
28	DQS2	68	NC	108	DQ51	148	VSS	188	A0	228	VSS
29	VSS	69	VDD	109	VSS	149	DQ22	189	VDD	229	DQ60
30	DQ18	70	A10/AP	110	DQ56	150	DQ23	190	BA1	230	DQ61
31	DQ19	71	BA0	111	DQ57	151	VSS	191	VDDQ	231	VSS
32	VSS	72	VDDQ	112	VSS	152	DQ28	192	/RAS	232	DM7
33	DQ24	73	/WE	113	/DQS7	153	DQ29	193	/CS0	233	NC
34	DQ25	74	/CAS	114	DQS7	154	VSS	194	VDDQ	234	VSS
35	VSS	75	VDDQ	115	VSS	155	DM3	195	ODT0	235	DQ62
36	/DQS3	76	/CS1	116	DQ58	156	NC	196	A13	236	DQ63
37	DQS3	77	ODT1	117	DQ59	157	VSS	197	VDD	237	VSS
38	VSS	78	VDDQ	118	VSS	158	DQ30	198	VSS	238	VDDSPD
39	DQ26	79	VSS	119	SDA	159	DQ31	199	DQ36	239	SA0
40	DQ27	80	DQ32	120	SCL	160	VSS	200	DQ37	240	SA1

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Block Diagram
1GB, 128Mx64 Module(1 Rank x8)

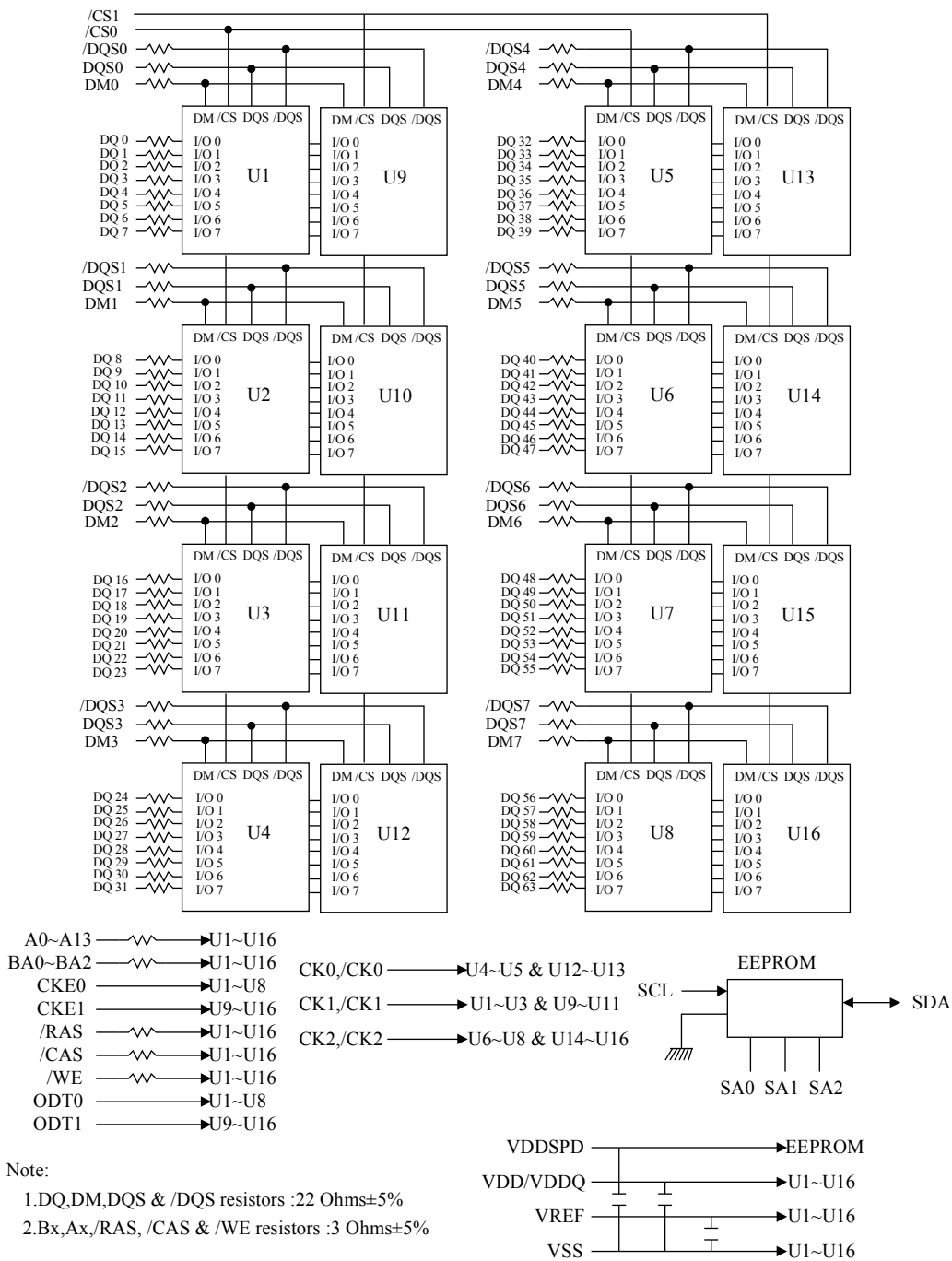


This technical information is based on industry standard data and tests believed to be reliable. However, Transcend makes no warranties, either expressed or implied, as to its accuracy and assume no liability in connection with the use of this product. Transcend reserves the right to make changes in specifications at any time without prior notice.

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Block Diagram
2GB, 256Mx64 Module(2 Rank x8)



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Absolute Maximum DC Ratings

Parameter	Symbol	Value	Unit	Notes
Voltage on VDD relative to Vss	VDD	-1.0 ~ 2.3	V	1
Voltage on VDDQ pin relative to Vss	VDDQ	-0.5 ~ 2.3	V	1
Voltage on VDDL pin relative to Vss	VDDL	-0.5 ~ 2.3	V	1
Voltage on any pin relative to Vss	VIN, VOUT	-0.5 ~ 2.3	V	1
Storage temperature	TSTG	-55~+100	°C	1,2

Note: 1. Stress greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
 2. Storage Temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JEDEC51-2 standard.

AC & DC Operating Conditions

Recommended DC operating conditions (SSTL –1.8)

Parameter	Symbol	Rating			Unit	Notes
		Min	Typ.	Max		
Supply voltage	VDD	1.7	1.8	1.9	V	
Supply voltage for DLL	VDDL	1.7	1.8	1.9	V	4
Supply voltage for Output	VDDQ	1.7	1.8	1.9	V	4
I/O Reference voltage	VREF	0.49*VDDQ	0.50*VDDQ	0.51*VDDQ	V	1,2
I/O Termination voltage	VTT	VREF-0.04	VREF	VREF+0.04	V	3
DC Input logic high	VIH(DC)	VREF+0.125	-	VDDQ+0.3	V	
DC Input logic low	VIL(DC)	-0.3	-	VREF-0.125	V	

Note: There is no specific device VDD supply voltage requirement for SSTL-1.8 compliance. However under all conditions VDDQ must be less than or equal to VDD.
 1. The value of VREF may be selected by the user to provide optimum noise margin in the system. Typically the value of VREF is expected to be about 0.5 x VDDQ of the transmitting device and VREF is expected to track variations in VDDQ.
 2. Peak to peak AC noise on VREF may not exceed +/-2% VREF (DC).
 3. VTT of transmitting device must track VREF of receiving device.
 4. AC parameters are measured with VDD, VDDQ and VDDL tied together.

Operating Temperature Condition

Parameter	Symbol	Rating	Unit	Note
Operating Temperature	TOPER	0 to 85	°C	1,2

Note: 1. Operating Temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JEDEC51.2 standard.
 2. At 0 - 85°C, operation temperature range are the temperature which all DRAM specification will be supported.

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**IDD Specification parameters Definition(IDD values are for full operating range of Voltage and Temperature)
 1GB, 128Mx64 Module(1 Rank x8)**

Parameter	Symbol	DDR2 667 CL5	DDR2 800 CL6	Unit
Operating One bank Active-Precharge current; tCK = tCK(IDD), tRC = tRC(IDD), tRAS = tRASmin(IDD); CKE is HIGH, CS\ is HIGH between valid commands;Address bus inputs are SWITCHING; Data bus inputs are SWITCHING	IDD0	280	296	mA
Operating One bank Active-read-Precharge current; IOUT = 0mA; BL = 4, CL = CL(IDD), AL = 0; tCK = tCK(IDD), tRC = tRC (IDD), tRAS = tRASmin(IDD), tRCD = tRCD(IDD); CKE is HIGH, CS\ is HIGH between valid commands; Address bus inputs are SWITCHING; Data pattern is same as IDD4W	IDD1	320	360	mA
Precharge power-down current; All banks idle; tCK = tCK(IDD); CKE is LOW; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING	IDD2P	80	80	mA
Precharge quiet standby current; All banks idle; tCK = tCK(IDD); CKE is HIGH, CS\ is HIGH; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING	IDD2Q	152	160	mA
Precharge standby current; All banks idle; tCK = tCK(IDD); CKE is HIGH, CS\ is HIGH; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING	IDD2N	176	200	mA
Active power - down current; All banks open; tCK = tCK(IDD); CKE is LOW; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING	Fast PDN Exit MRS(12) = 0mA	IDD3P-F	144	mA
	Slow PDN Exit MRS(12) = 1mA	IDD3P-S	136	
Active standby current; All banks open; tCK = tCK(IDD), tRAS = tRASmax(IDD), tRP = tRP(IDD); CKE is HIGH, CS\ is HIGH between valid commands; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING	IDD3N	240	240	mA
Operating burst read current; All banks open, Continuous burst reads, IOUT = 0mA; BL = 4, CL = CL(IDD), AL = 0; tCK = tCK(IDD), tRAS = tRASmax(IDD), tRP = tRP(IDD); CKE is HIGH, CS\ is HIGH between valid commands; Address bus inputs are SWITCHING; Data pattern is same as IDD4W	IDD4R	520	560	mA
Operating burst write current; All banks open, Continuous burst writes; BL = 4, CL = CL(IDD), AL = 0; tCK = tCK(IDD), tRAS = tRASmax(IDD), tRP = tRP(IDD); CKE is HIGH, CS\ is HIGH between valid commands; Address bus inputs are SWITCHING; Data bus inputs are SWITCHING IDD4R	IDD4W	440	480	mA
Burst refresh current; tCK = tCK(IDD); Refresh command at every tRFC(IDD) interval; CKE is HIGH, CS\ is HIGH between valid commands; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING	IDD5	680	720	mA
Self refresh current; CK and CK\ at 0V; CKE = 0.2V; Other control and address bus inputs are FLOATING; Data bus inputs are FLOATING	IDD6	80	80	mA
Operating bank interleave read current; All bank interleaving reads, IOUT = 0mA; BL = 4, CL = CL(IDD), AL = tRCD(IDD)-1*tCK(IDD); tCK = tCK(IDD), tRC = tRC(IDD), tRRD = tRRD(IDD), tRCD = 1*tCK(IDD); CKE is HIGH, CS\ is HIGH between valid commands; Address bus inputs are STABLE during Deselects; Data pattern is same as IDD4R; Refer to the following page for detailed timing conditions	IDD7	1000	1080	mA

Note: 1. Module IDD was calculated on the specific brand DRAM(3Xnm) component IDD and can be differently measured according to DQ loading capacitor.

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2GB, 256Mx64 Module(2 Rank x8)

Parameter	Symbol	DDR2 533 CL4	DDR2 667 CL5	DDR2 800 CL6	Unit
Operating One bank Active-Precharge current; tCK = tCK(IDD), tRC = tRC(IDD), tRAS = tRASmin(IDD); CKE is HIGH, CS\ is HIGH between valid commands; Address bus inputs are SWITCHING; Data bus inputs are SWITCHING	IDD0	417	436	460	mA
Operating One bank Active-read-Precharge current; IOU _T = 0mA; BL = 4, CL = CL(IDD), AL = 0; tCK = tCK(IDD), tRC = tRC(IDD), tRAS = tRASmin(IDD), tRCD = tRCD(IDD); CKE is HIGH, CS\ is HIGH between valid commands; Address bus inputs are SWITCHING; Data pattern is same as IDD4W	IDD1	455	480	536	mA
Precharge power-down current; All banks idle; tCK = tCK(IDD); CKE is LOW; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING	IDD2P	160	160	160	mA
Precharge quiet standby current; All banks idle; tCK = tCK(IDD); CKE is HIGH, CS\ is HIGH; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING	IDD2Q	304	304	320	mA
Precharge standby current; All banks idle; tCK = tCK(IDD); CKE is HIGH, CS\ is HIGH; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING	IDD2N	338	352	400	mA
Active power - down current; All banks open; tCK = tCK(IDD); CKE is LOW; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING	Fast PDN Exit MRS(12) = 0mA	IDD3P-F	276	288	mA
	Slow PDN Exit MRS(12) = 1mA	IDD3P-S	272	272	
Active standby current; All banks open; tCK = tCK(IDD), tRAS = tRASmax(IDD), tRP = tRP(IDD); CKE is HIGH, CS\ is HIGH between valid commands; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING	IDD3N	385	405	405	mA
Operating burst read current; All banks open, Continuous burst reads, IOU _T = 0mA; BL = 4, CL = CL(IDD), AL = 0; tCK = tCK(IDD), tRAS = tRASmax(IDD), tRP = tRP(IDD); CKE is HIGH, CS\ is HIGH between valid commands; Address bus inputs are SWITCHING; Data pattern is same as IDD4W	IDD4R	625	698	735	mA
Operating burst write current; All banks open, Continuous burst writes; BL = 4, CL = CL(IDD), AL = 0; tCK = tCK(IDD), tRAS = tRASmax(IDD), tRP = tRP(IDD); CKE is HIGH, CS\ is HIGH between valid commands; Address bus inputs are SWITCHING; Data bus inputs are SWITCHING IDD4R	IDD4W	552	602	647	mA
Burst refresh current; tCK = tCK(IDD); Refresh command at every tRFC(IDD) interval; CKE is HIGH, CS\ is HIGH between valid commands; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING	IDD5	804	843	891	mA
Self refresh current; CK and CK\ at 0V; CKE = 0.2V; Other control and address bus inputs are FLOATING; Data bus inputs are FLOATING	IDD6	160	160	160	mA
Operating bank interleave read current; All bank interleaving reads, IOU _T = 0mA; BL = 4, CL = CL(IDD), AL = tRCD(IDD)-1*tCK(IDD); tCK = tCK(IDD), tRC = tRC(IDD), tRRD = tRRD(IDD), tRCD = 1*tCK(IDD); CKE is HIGH, CS\ is HIGH between valid commands; Address bus inputs are STABLE during Deselects; Data pattern is same as IDD4R; Refer to the following page for detailed timing conditions	IDD7	1065	1166	1249	mA

Note: 1. Module IDD was calculated on the specific brand DRAM(3Xnm) component IDD and can be differently measured according to DQ loading capacitor.

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Timing Parameters & Specifications

Speed		DDR2 533		DDR2 667		DDR2 800		Unit
Parameter	Symbol	Min	Max	Min	Max	Min	Max	
DQ output access time from CK & /CK	tAC	-500	+500	-450	+450	-400	+400	ps
DQS output access time from CK & /CK	tDQSCK	-450	+450	-400	+400	-350	+350	ps
CK high-level width	tCH	0.45	0.55	0.48	0.52	0.48	0.52	tCK
CK low-level width	tCL	0.45	0.55	0.48	0.52	0.48	0.52	tCK
CK half period	tHP	min(tCL,tCH)	X	min(tCL,tCH)	X	min(tCL,tCH)	X	ps
Clock cycle time, CL=x	tCK	3750	8000	3000	8000	2500	8000	ps
DQ and DM input hold time	tDH	225	x	175	x	125	x	ps
DQ and DM input setup time	tDS	100	X	100	X	50	X	ps
Control & Address input pulse width for each input	tIPW	0.6	x	0.6	x	0.6	x	tCK
DQ and DM input pulse width for each input	tDIPW	0.35	X	0.35	X	0.35	X	tCK
Data-out high-impedance time from CK/CK	tHZ	X	tAC max	X	tAC max	X	tAC max	ps
DQS low-impedance time from CK/CK	tLZ(DQS)	tAC min	tAC max	tAC min	tAC max	tAC min	tAC max	ps
DQ low-impedance time from CK/CK	tLZ(DQ)	2*tAC min	TAC max	2*tAC min	TAC max	2*tAC min	TAC max	ps
DQS-DQ skew for DQS and associated DQ signals	tDQSQ	X	300	X	240	X	200	ps
DQ hold skew factor	tQHS	X	400	X	340	X	300	ps
DQ/DQS output hold time from DQS	tQH	tHP - tQHS	X	tHP - tQHS	X	tHP - tQHS	X	ps
Write command to first DQS latching transition	tDQSS	-0.25	+0.25	-0.25	+0.25	-0.25	+0.25	tCK
DQS input high pulse width	tDQSH	0.35	X	0.35	X	0.35	X	tCK
DQS input low pulse width	tDQSL	0.35	X	0.35	X	0.35	X	tCK
DQS falling edge to CK setup time	tDSS	0.2	X	0.2	X	0.2	X	tCK
DQS falling edge hold time from CK	tDSH	0.2	X	0.2	X	0.2	X	tCK
Mode register set command cycle time	tMRD	2	X	2	X	2	X	tCK
Write postamble	tWPST	0.4	0.6	0.4	0.6	0.4	0.6	tCK
Write preamble	tWPRE	0.35	X	0.35	X	0.35	X	tCK
Address and control input hold time	tIH	375	X	275	X	250	X	ps
Address and control input setup time	tIS	250	X	200	X	175	X	ps
Read preamble	tRPRE	0.9	1.1	0.9	1.1	0.9	1.1	tCK

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Speed		DDR2 533		DDR2 667		DDR2 800		Unit
Parameter	Symbol	Min	Max	Min	Max	Min	Max	
Read postamble	tRPST	0.4	0.6	0.4	0.6	0.4	0.6	tCK
Active to active command period for 1KB page size products	tRRD	7.5	X	7.5	X	7.5	X	ns
Active to active command period for 2KB page size products	tRRD	10	X	10	X	10	X	ns
Four Activate Window for 1KB page size products	tFAW	37.5	X	37.5	X	35	X	ns
Four Activate Window for 2KB page size products	tFAW	50	X	50	X	45	X	ns
/CAS to /CAS command delay	tCCD	2	X	2	X	2	X	tCK
Write recovery time	tWR	15	X	15	X	15	X	ns
Auto precharge write recovery + precharge time	tDAL	tWR+tRP	X	tWR+tRP	X	tWR+tRP	X	tCK
Internal write to read command delay	tWTR	7.5	X	7.5	X	7.5	X	ns
Internal read to precharge command delay	tRTP	7.5	X	7.5	X	7.5	X	ns
Exit self refresh to a non-read command	tXSNR	tRFC + 10	X	tRFC + 10	X	tRFC + 10	X	ns
Exit self refresh to a read command	tXSRD	200	X	200	X	200	X	tCK
Exit precharge power down to any non-read command	tXP	2	X	2	X	2	X	tCK
Exit active power down to read command	tXARD	2	X	2	X	2	X	tCK
Exit active power down to read command (Slow exit, Lower power)	tXARDS	6 - AL	X	7 - AL	X	8 - AL	X	tCK
CKE minimum pulse width (high and low pulse width)	tCKE	3	X	3	X	3	X	tCK
ODT turn-on delay	tAOND	2	2	2	2	2	2	tCK
ODT turn-on	tAON	tAC(min)	tAC(max)+1	tAC(min)	tAC(max)+0.7	tAC(min)	tAC(max)+0.7	ns
ODT turn-on(Power-Down mode)	tAONPD	tAC(min)+2	2tCK+tAC(max)+1	tAC(min)+2	2tCK+tAC(max)+1	tAC(min)+2	2tCK+tAC(max)+1	ns
ODT turn-off delay	tAOFD	2.5	2.5	2.5	2.5	2.5	2.5	tCK
ODT turn-off	tAOF	tAC(min)	tAC(max)+0.6	tAC(min)	tAC(max)+0.6	tAC(min)	tAC(max)+0.6	ns
ODT turn-off (Power-Down mode)	tAOFPD	tAC(min)+2	2.5tCK+tAC(max)+1	tAC(min)+2	2.5tCK+tAC(max)+1	tAC(min)+2	2.5tCK+tAC(max)+1	ns
ODT to power down entry latency	tANPD	3	X	3	X	3	X	tCK
ODT power down exit latency	tAXPD	8	X	8	X	8	X	tCK
OCD drive mode output delay	tOIT	0	12	0	12	0	12	ns
Minimum time clocks remains ON after CKE asynchronously drops LOW	tDelay	tIS+tCK+tIH	X	tIS+tCK+tIH	X	tIS+tCK+tIH	X	ns

TS256MLQ64V5U TS128MLQ64V6U
 TS256MLQ64V6U TS128MLQ64V8U
 TS256MLQ64V8U

240Pin DDR2 533/667/800 UDIMM
 1GB~2GB Based on 128Mx8

SERIAL PRESENCE DETECT SPECIFICATION

TS128MLQ64V6U Serial Presence Detect					
Byte No.	Function Described	Standard Specification		Vendor Part	
0	# of Serial PD Bytes written during module production	128bytes		80	
1	Total # of Bytes of S.P.D Memory Device	256bytes		08	
2	Fundamental Memory Type	DDR2 SDRAM		08	
3	# of Row Addresses on this Assembly	13		0E	
4	# of Column Addresses on this Assembly	10		0A	
5	# of Module Rows on this Assembly	1 ROW, Planar, 18.3mm	1 ROW, Planar, 30.0mm	00	60
6	Data Width of this Assembly	64bits		40	
7	Reserved	-		00	
8	VDDQ and Interface Standard of this Assembly	SSTL 1.8V		05	
9	DDR2 SDRAM cycle time at Max. Supported CAS latency=X	3.0ns		30	
10	DDR2 SDRAM Access time from clock at CL=X	±0.45ns		45	
11	DIMM configuration type (non-parity, Parity, ECC)	Non parity/ECC		00	
12	Refresh Rate	7.8us		82	
13	Primary DDR2 SDRAM Width	X8		08	
14	Error Checking DDR2 SDRAM Width	-		00	
15	Reserved	-		00	
16	DDR2 SDRAM device attributes: Burst lengths supported	4, 8		0C	
17	DDR2 SDRAM device attributes: # of banks on each DDR2 SDRAM device	8 banks		08	
18	DDR2 SDRAM device attributes: CAS Latency supported	5,4,3		38	
19	Reserved	-		01	
20	DIMM type information	Regular UDIMM		02	
21	DDR2 SDRAM Module Attributes	Analysis probe not installed, FET switch external not enable		00	
22	DDR2 SDRAM Device Attributes: General	Supports weak driver, 50ohm ODT	Supports weak driver, 50ohm ODT, PASR	03	07
23	DDR2 SDRAM Cycle Time CL=X-1	3.75ns		3D	
24	DDR SDRAM Access from Clock CL=X-1	±0.5ns		50	
25	DDR SDRAM Cycle Time CL=X-2	5.0ns		50	
26	DDR SDRAM Access from Clock CL=X-2	±0.6ns		60	
27	Minimum Row Precharge Time (tRP)	15ns		3C	
28	Minimum Row Active to Row Activate delay (tRRD)	7.5ns		1E	

TS256MLQ64V5U TS128MLQ64V6U
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29	Minimum RAS to CAS Delay (tRCD)	15ns	3C					
30	Minimum active to Precharge time (tRAS)	45ns	2D					
31	Module ROW density	1GB	01					
32	Command and address setup time before clock(=tIS)	0.2ns	20					
33	Command and address hold time after clock(=tIH)	0.27ns	27					
34	Data input setup time before strobe(=tDS)	0.1ns	10					
35	Data input hold time after strobe(=tDH)	0.17ns	17					
36	Write recovery time(=tWR)	15ns	3C					
37	Internal write to read command delay(=tWTR)	7.5ns	1E					
38	Internal read to precharge command delay(=tRTP)	7.5ns	1E					
39	Memory analysis probe characteristics	-	00					
40	Extension of Byte41 tRC and Byte42 tRFC	TRFC(127.5ns)	06					
41	DDR SDRAM Minimum Active to Active/Auto Refresh Time(tRC)	60ns	3C					
42	DDR SDRAM Minimum Auto-Refresh to Active/Auto-Refresh Command Period (tRFC)	127.5ns	7F					
43	DDR SDRAM Maximum Device Cycle Time (tCK max)	8ns	80					
44	DDR SDRAM DQS-DQ Skew for DQS and associated DQ signals (tDQSQ max)	0.24ns	18					
45	DDR SDRAM Read Data Hold Skew Factor (tQHS)	0.34ns	22					
46	PLL Relock Time	-	00					
47~48	DT in SPD	-	00					
49	High Temp. Self Refresh	-	00					
50~61	Superset Information	-	00					
62	SPD Data Revision Code	REV 1.2	12					
63	Checksum for Bytes 0-62	- -	B2	16				
64-71	Manufacturers JEDEC ID	Transcend	7F, 4F					
72	Manufacturing Location	T	54					
73-90	Manufacturers Part Number	TS128MLQ64V6U	54	53	31	32	38	4D
			4C	51	36	34	56	36
			55	20	20	20	20	20
91-92	Revision Code	-	-					
93-94	Manufacturing Date	By Manufacturer	Variable					
95-98	Assembly Serial Number	By Manufacturer	Variable					
99-127	Manufacturer Specific Data	-	-					
128~255	Open for customer use	Undefined	-					

TS256MLQ64V5U TS128MLQ64V6U
 TS256MLQ64V6U TS128MLQ64V8U
 TS256MLQ64V8U

240Pin DDR2 533/667/800 UDIMM
 1GB~2GB Based on 128Mx8

TS128MLQ64V8U Serial Presence Detect					
Byte No.	Function Described	Standard Specification		Vendor Part	
0	# of Serial PD Bytes written during module production	128bytes		80	
1	Total # of Bytes of S.P.D Memory Device	256bytes		08	
2	Fundamental Memory Type	DDR2 SDRAM		08	
3	# of Row Addresses on this Assembly	14		0E	
4	# of Column Addresses on this Assembly	10		0A	
5	# of Module Rows on this Assembly	1 ROW, Planar, 18.3mm	1 ROW, Planar, 30.0mm	00	60
6	Data Width of this Assembly	64bits		40	
7	Reserved	-		00	
8	VDDQ and Interface Standard of this Assembly	SSTL 1.8V		05	
9	DDR2 SDRAM cycle time at Max. Supported CAS latency=X	2.5ns		25	
10	DDR2 SDRAM Access time from clock at CL=X	±0.4ns		40	
11	DIMM configuration type (non-parity, Parity, ECC)	Non parity/ECC		00	
12	Refresh Rate	7.8us		82	
13	Primary DDR2 SDRAM Width	X8		08	
14	Error Checking DDR2 SDRAM Width	-		00	
15	Reserved	-		00	
16	DDR2 SDRAM device attributes: Burst lengths supported	4, 8		0C	
17	DDR2 SDRAM device attributes: # of banks on each DDR2 SDRAM device	8 banks		08	
18	DDR2 SDRAM device attributes: CAS Latency supported	6, 5, 4		70	
19	DIMM Mechanical Characteristics	X =<4.10		01	
20	DIMM type information	Regular UDIMM		02	
21	DDR2 SDRAM Module Attributes	Analysis probe not installed, FET switch external not enable		00	
22	DDR2 SDRAM Device Attributes: General	Supports weak driver, 50ohm ODT	Supports weak driver, 50Ohm ODT, PASR	03	07
23	DDR2 SDRAM Cycle Time CL=X-1	3.0ns		30	
24	DDR2 SDRAM Access from Clock CL=X-1	±0.45ns		45	
25	DDR2 SDRAM Cycle Time CL=X-2	3.75ns		3D	
26	DDR2 SDRAM Access from Clock CL=X-2	±0.5ns		50	
27	Minimum Row Precharge Time (tRP)	15ns		3C	
28	Minimum Row Active to Row Activate delay (tRRD)	7.5ns		1E	
29	Minimum RAS to CAS Delay (tRCD)	15ns		3C	

TS256MLQ64V5U TS128MLQ64V6U
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30	Minimum active to Precharge time (tRAS)	45ns	2D					
31	Module ROW density	1GB	01					
32	Command and address setup time before clock(=tIS)	0.175ns	17					
33	Command and address hold time after clock(=tIH)	0.25ns	25					
34	Data input setup time before strobe(=tDS)	0.05ns	05					
35	Data input hold time after strobe(=tDH)	0.125ns	12					
36	Write recovery time(=tWR)	15ns	3C					
37	Internal write to read command delay(=tWTR)	7.5ns	1E					
38	Internal read to precharge command delay(=tRTP)	7.5ns	1E					
39	Memory analysis probe characteristics	-	00					
40	Extension of Byte41 tRC and Byte42 tRFC	tRFC(127.5ns)	06					
41	DDR2 SDRAM Minimum Active to Active/Auto Refresh Time(tRC)	60ns	3C					
42	DDR2 SDRAM Minimum Auto-Refresh to Active/Auto-Refresh Command Period (tRFC)	127.5ns	7F					
43	DDR2 SDRAM Maximum Device Cycle Time (tCK max)	8ns	80					
44	DDR2 SDRAM DQS-DQ Skew for DQS and associated DQ signals (tDQSQ max)	0.20ns	14					
45	DDR2 SDRAM Read Data Hold Skew Factor (tQHS)	0.3ns	1E					
46	PLL Relock Time	-	00					
47~48	DT in SPD	-	00					
49	High Temp. Self Refresh	Support	03					
50~61	Superset Information	-	00					
62	SPD Data Revision Code	REV 1.2	12					
63	Checksum for Bytes 0-62	- -	7C	E3				
64-71	Manufacturers JEDEC ID	Transcend	7F, 4F					
72	Manufacturing Location	T	54					
73-90	Manufacturers Part Number	TS128MLQ64V8U	54	53	31	32	38	4D
			4C	51	36	34	56	38
			55	20	20	20	20	20
91-92	Revision Code	-	-					
93-94	Manufacturing Date	By Manufacturer	Variable					
95-98	Assembly Serial Number	By Manufacturer	Variable					
99-127	Manufacturer Specific Data	-	-					
128~255	Open for customer use	Undefined	-					

TS256MLQ64V5U TS128MLQ64V6U
 TS256MLQ64V6U TS128MLQ64V8U
 TS256MLQ64V8U

240Pin DDR2 533/667/800 UDIMM
 1GB~2GB Based on 128Mx8

TS256MLQ64V5U Serial Presence Detect					
Byte No.	Function Described	Standard Specification		Vendor Part	
0	# of Serial PD Bytes written during module production	128bytes		80	
1	Total # of Bytes of S.P.D Memory Device	256bytes		08	
2	Fundamental Memory Type	DDR2 SDRAM		08	
3	# of Row Addresses on this Assembly	13		0E	
4	# of Column Addresses on this Assembly	10		0A	
5	# of Module Rows on this Assembly	2 ROW, Planar, 18.3mm	2 ROW, Planar, 30.0mm	01	61
6	Data Width of this Assembly	64bits		40	
7	Reserved	-		00	
8	VDDQ and Interface Standard of this Assembly	SSTL 1.8V		05	
9	DDR2 SDRAM cycle time at Max. Supported CAS latency=X	3.75ns		3D	
10	DDR2 SDRAM Access time from clock at CL=X	±0.5ns		50	
11	DIMM configuration type (non-parity, Parity, ECC)	Non ECC		00	
12	Refresh Rate	7.8us		82	
13	Primary DDR2 SDRAM Width	X8		08	
14	Error Checking DDR2 SDRAM Width	N/A		00	
15	Reserved	-		00	
16	DDR2 SDRAM device attributes: Burst lengths supported	4,8		0C	
17	DDR2 SDRAM device attributes: # of banks on each DDR2 SDRAM device	8 banks		08	
18	DDR2 SDRAM device attributes: CAS Latency supported	5,4,3		38	
19	DIMM Mechanical Characteristics	X=<4.10	-	01	00
20	DIMM type information	Regular UDIMM		02	
21	DDR2 SDRAM Module Attributes	Analysis probe not installed, FET switch external not enable		00	
22	DDR2 SDRAM Device Attributes: General	Supports weak driver, 50ohm ODT	Supports weak driver	03	01
23	DDR2 SDRAM Cycle Time CL=X-1	3.75ns		3D	
24	DDR SDRAM Access from Clock CL=X-1	±0.5ns		50	
25	DDR SDRAM Cycle Time CL=X-2	5.0ns		50	
26	DDR SDRAM Access from Clock CL=X-2	±0.6ns		60	
27	Minimum Row Precharge Time (tRP)	15ns		3C	
28	Minimum Row Active to Row Activate delay (tRRD)	7.5ns		1E	
29	Minimum RAS to CAS Delay (tRCD)	15ns		3C	
30	Minimum active to Precharge time (tRAS)	40ns		2D	

TS256MLQ64V5U TS128MLQ64V6U
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TS256MLQ64V8U

240Pin DDR2 533/667/800 UDIMM
1GB~2GB Based on 128Mx8

31	Module ROW density	2 GB		01					
32	Command and address setup time before clock(=tIS)	0.25ns		25					
33	Command and address hold time after clock(=tIH)	0.37ns		37					
34	Data input setup time before strobe(=tDS)	0.10ns		10					
35	Data input hold time after strobe(=tDH)	0.22ns		22					
36	Write recovery time(=tWR)	15ns		3C					
37	Internal write to read command delay(=tWTR)	7.5ns		1E					
38	Internal read to precharge command delay(=tRTP)	7.5ns		1E					
39	Memory analysis probe characteristics	-		00					
40	Reserved	-		06					
41	DDR SDRAM Minimum Active to Active/Auto Refresh Time(tRC)	55ns		3C					
42	DDR SDRAM Minimum Auto-Refresh to Active/Auto-Refresh Command Period (tRFC)	127.5ns		7F					
43	DDR SDRAM Maximum Device Cycle Time (tCK max)	8ns		80					
44	DDR SDRAM DQS-DQ Skew for DQS and associated DQ signals (tDQSQ max)	0.3ns		1E					
45	DDR SDRAM Read Data Hold Skew Factor (tQHS)	0.4ns		28					
46	PLL Relock Time	-		00					
47~61	Superset Information	-		00					
62	SPD Data Revision Code	REV 1.2	REV 1.1	12	11				
63	Checksum for Bytes 0-62	-	-	F7	53				
64-71	Manufacturers JEDEC ID	Transcend		7F, 4F					
72	Manufacturing Location	T		54					
73-90	Manufacturers Part Number	TS256MLQ64V5U		54	53	32	35	36	4D
				4C	51	36	34	56	35
				55	20	20	20	20	20
91-92	Revision Code	-		-					
93-94	Manufacturing Date	By Manufacturer		Variable					
95-98	Assembly Serial Number	By Manufacturer		Variable					
99-127	Manufacturer Specific Data	-		-					
128~255	Open for customer use	Undefined		-					

TS256MLQ64V5U TS128MLQ64V6U
TS256MLQ64V6U TS128MLQ64V8U
TS256MLQ64V8U

240Pin DDR2 533/667/800 UDIMM
1GB~2GB Based on 128Mx8

TS256MLQ64V6U Serial Presence Detect					
Byte No.	Function Described	Standard Specification		Vendor Part	
0	# of Serial PD Bytes written during module production	128bytes		80	
1	Total # of Bytes of S.P.D Memory Device	256bytes		08	
2	Fundamental Memory Type	DDR2 SDRAM		08	
3	# of Row Addresses on this Assembly	13		0E	
4	# of Column Addresses on this Assembly	10		0A	
5	# of Module Rows on this Assembly	2 ROW, Planar, 18.3mm	2 ROW, Planar, 30.0mm	01	61
6	Data Width of this Assembly	64bits		40	
7	Reserved	-		00	
8	VDDQ and Interface Standard of this Assembly	SSTL 1.8V		05	
9	DDR2 SDRAM cycle time at Max. Supported CAS latency=X	3.0ns		30	
10	DDR2 SDRAM Access time from clock at CL=X	±0.4ns		45	
11	DIMM configuration type (non-parity, Parity, ECC)	Non ECC		00	
12	Refresh Rate	7.8us		82	
13	Primary DDR2 SDRAM Width	X8		08	
14	Error Checking DDR2 SDRAM Width	N/A		00	
15	Reserved	-		00	
16	DDR2 SDRAM device attributes: Burst lengths supported	4,8		0C	
17	DDR2 SDRAM device attributes: # of banks on each DDR2 SDRAM device	8 banks		08	
18	DDR2 SDRAM device attributes: CAS Latency supported	5,4,3		38	
19	DIMM Mechanical Characteristics	X=<4.10		01	
20	DIMM type information	Regular UDIMM		02	
21	DDR2 SDRAM Module Attributes	Analysis probe not installed, FET switch external not enable		00	
22	DDR2 SDRAM Device Attributes: General	Supports weak driver, 50ohm ODT		03	
23	DDR2 SDRAM Cycle Time CL=X-1	3.75ns		3D	
24	DDR SDRAM Access from Clock CL=X-1	±0.5ns		50	
25	DDR SDRAM Cycle Time CL=X-2	5.0ns		50	
26	DDR SDRAM Access from Clock CL=X-2	±0.6ns		60	
27	Minimum Row Precharge Time (tRP)	15ns		3C	
28	Minimum Row Active to Row Activate delay (tRRD)	7.5ns		1E	
29	Minimum RAS to CAS Delay (tRCD)	15ns		3C	
30	Minimum active to Precharge time (tRAS)	45ns		2D	
31	Module ROW density	1 GB		01	
32	Command and address setup time before clock(=tIS)	0.20ns		20	
33	Command and address hold time after clock(=tIH)	0.27ns		27	

TS256MLQ64V5U TS128MLQ64V6U
TS256MLQ64V6U TS128MLQ64V8U
TS256MLQ64V8U

240Pin DDR2 533/667/800 UDIMM
1GB~2GB Based on 128Mx8

34	Data input setup time before strobe(=tDS)	0.10ns	10					
35	Data input hold time after strobe(=tDH)	0.17ns	17					
36	Write recovery time(=tWR)	15ns	3C					
37	Internal write to read command delay(=tWTR)	7.5ns	1E					
38	Internal read to precharge command delay(=tRTP)	7.5ns	1E					
39	Memory analysis probe characteristics	-	00					
40	Extension of Byte41 tRC and Byte42 tRFC	tRFC(1.27.5ns)	06					
41	DDR SDRAM Minimum Active to Active/Auto Refresh Time(tRC)	60ns	3C					
42	DDR SDRAM Minimum Auto-Refresh to Active/Auto-Refresh Command Period (tRFC)	195ns	7F					
43	DDR SDRAM Maximum Device Cycle Time (tCK max)	8ns	80					
44	DDR SDRAM DQS-DQ Skew for DQS and associated DQ signals (tDQSQ max)	0.24ns	18					
45	DDR SDRAM Read Data Hold Skew Factor (tQHS)	0.34ns	22					
46	PLL Relock Time	-	00					
47~61	Superset Information	-	00					
62	SPD Data Revision Code	REV 1.2	12					
63	Checksum for Bytes 0-62	- -	B3	13				
64-71	Manufacturers JEDEC ID	Transcend	7F, 4F					
72	Manufacturing Location	T	54					
73-90	Manufacturers Part Number	TS256MLQ64V6U	54	53	32	35	36	4D
			4C	51	36	34	56	36
			55	20	20	20	20	20
91-92	Revision Code	-	-					
93-94	Manufacturing Date	By Manufacturer	Variable					
95-98	Assembly Serial Number	By Manufacturer	Variable					
99-127	Manufacturer Specific Data	-	-					
128~255	Open for customer use	Undefined	-					

TS256MLQ64V5U TS128MLQ64V6U
TS256MLQ64V6U TS128MLQ64V8U
TS256MLQ64V8U

240Pin DDR2 533/667/800 UDIMM
1GB~2GB Based on 128Mx8

TS256MLQ64V8U Serial Presence Detect					
Byte No.	Function Described	Standard Specification		Vendor Part	
0	# of Serial PD Bytes written during module production	128bytes		80	
1	Total # of Bytes of S.P.D Memory Device	256bytes		08	
2	Fundamental Memory Type	DDR2 SDRAM		08	
3	# of Row Addresses on this Assembly	14		0E	
4	# of Column Addresses on this Assembly	10		0A	
5	# of Module Rows on this Assembly	2 ROW, Planar, 18.3.0mm	2 ROW, Planar, 30.0mm	01	61
6	Data Width of this Assembly	64bits		40	
7	Reserved	-		00	
8	VDDQ and Interface Standard of this Assembly	SSTL 1.8V		05	
9	DDR2 SDRAM cycle time at Max. Supported CAS latency=X	2.50ns		25	
10	DDR2 SDRAM Access time from clock at CL=X	±0.40ns		40	
11	DIMM configuration type (non-parity, Parity, ECC)	Non ECC		00	
12	Refresh Rate	7.8us		82	
13	Primary DDR2 SDRAM Width	X8		08	
14	Error Checking DDR2 SDRAM Width	N/A		00	
15	Reserved	-		00	
16	DDR2 SDRAM device attributes: Burst lengths supported	4,8		0C	
17	DDR2 SDRAM device attributes: # of banks on each DDR2 SDRAM device	8 banks		08	
18	DDR2 SDRAM device attributes: CAS Latency supported	6,5,4		70	
19	DIMM Mechanical Characteristics	X=< 4.10		01	
20	DIMM type information	Regular UDIMM		02	
21	DDR2 SDRAM Module Attributes	Analysis probe not installed, FET switch external not enable		00	
22	DDR2 SDRAM Device Attributes: General	Supports weak driver		07	
23	DDR2 SDRAM Cycle Time CL=X-1	3.0ns		30	
24	DDR2 SDRAM Access from Clock CL=X-1	±0.45ns		45	
25	DDR2 SDRAM Cycle Time CL=X-2	3.75ns		3D	
26	DDR2 SDRAM Access from Clock CL=X-2	±0.5ns		50	
27	Minimum Row Precharge Time (tRP)	15ns		3C	
28	Minimum Row Active to Row Activate delay (tRRD)	7.5ns		1E	
29	Minimum RAS to CAS Delay (tRCD)	15ns		3C	
30	Minimum active to Precharge time (tRAS)	45ns		2D	
31	Module ROW density	1GB		01	
32	Command and address setup time before clock(=tIS)	0.175ns		17	
33	Command and address hold time after clock(=tIH)	0.25ns		25	

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TS256MLQ64V8U

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1GB~2GB Based on 128Mx8

34	Data input setup time before strobe(=tDS)	0.05ns	05					
35	Data input hold time after strobe(=tDH)	0.125ns	12					
36	Write recovery time(=tWR)	15ns	3C					
37	Internal write to read command delay(=tWTR)	7.5ns	1E					
38	Internal read to precharge command delay(=tRTP)	7.5ns	1E					
39	Memory analysis probe characteristics	-	00					
40	Extension of Byte41 tRC and Byte42 tRFC	tRC(57.5ns)	06					
41	DDR2 SDRAM Minimum Active to Active/Auto Refresh Time(tRC)	60ns	3C					
42	DDR2 SDRAM Minimum Auto-Refresh to Active/Auto-Refresh Command Period (tRFC)	127.5ns	7F					
43	DDR2 SDRAM Maximum Device Cycle Time (tCK max)	8ns	80					
44	DDR2 SDRAM DQS-DQ Skew for DQS and associated DQ signals (tDQSQ max)	0.20ns	14					
45	DDR2 SDRAM Read Data Hold Skew Factor (tQHS)	0.3ns	1E					
46	PLL Relock Time	-	00					
47~61	Superset Information	-	00					
62	SPD Data Revision Code	REV 1.2	12					
63	Checksum for Bytes 0-62	- -	81	E1				
64-71	Manufacturers JEDEC ID	Transcend	7F, 4F					
72	Manufacturing Location	T	54					
73-90	Manufacturers Part Number	TS256MLQ64V8U	54	53	32	35	36	4D
			4C	51	36	34	56	38
			55	20	20	20	20	20
91-92	Revision Code	-	-					
93-94	Manufacturing Date	By Manufacturer	Variable					
95-98	Assembly Serial Number	By Manufacturer	Variable					
99-127	Manufacturer Specific Data	-	-					
128~255	Open for customer use	Undefined	-					