TS512MSK64W6H
TS1GSK64W6H

204Pin DDR3L 1600 1.35V SO-DIMM
4~8GB Based on 512Mx8

Description

DDR3 1.35V SO-DIMM is high-speed, low power memory module that use 512Mx8bits DDR3 SDRAM in FBGA package and a 2048 bits serial EEPROM on a 204-pin printed circuit board. DDR3 1.35V SO-DIMM is a Dual In-Line Memory Module and is intended for mounting into 204-pin edge connector sockets.

Synchronous design allows precise cycle control with the use of system clock. Data I/O transactions are possible on both edges of DQS. Range of operation frequencies, programmable latencies allow the same device to be useful for a variety of high bandwidth, high performance memory system applications.

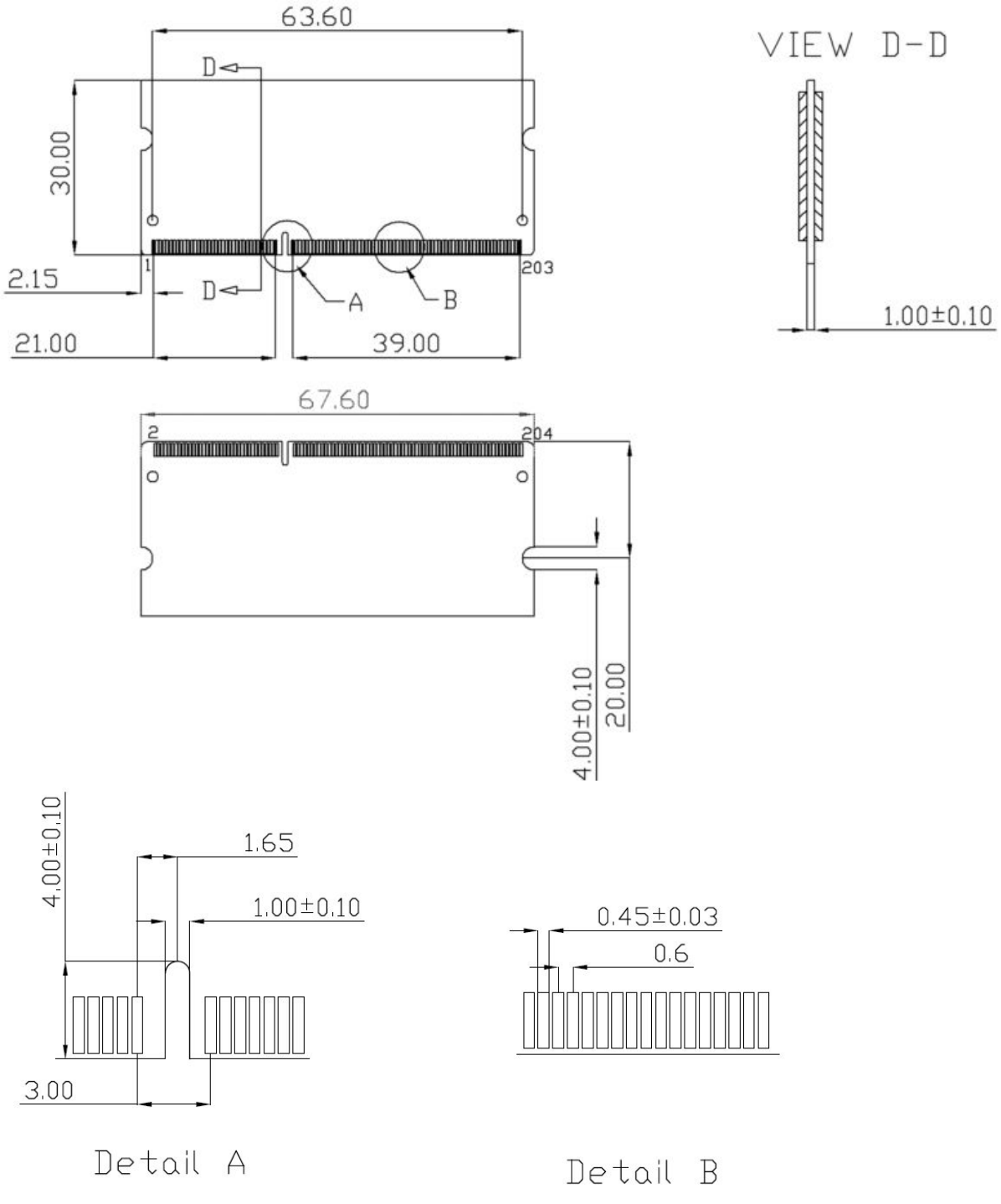
Features

- RoHS compliant products.
- JEDEC standard 1.35V(1.28V~1.45V) Power supply
- JEDEC standard 1.5V(1.425V~1.575V) Power supply
- VDDQ=1.35V(1.28V~1.45V) & 1.5V(1.425V~1.575V)
- Clock Freq: 800MHZ for 1600Mb/s/Pin.
- Programmable CAS Latency: 5, 6, 7, 8, 9, 10, 11
- Programmable Additive Latency (Posted /CAS): 0,CL-2 or CL-1 clock
- Programmable /CAS Write Latency (CWL) = 8(DDR3-1600)
- 8 bit pre-fetch
- Burst Length: 4, 8
- Bi-directional Differential Data-Strobe
- Internal calibration through ZQ pin
- On Die Termination with ODT pin
- Serial presence detect with EEPROM
- Asynchronous reset

- **Pin Identification**

Symbol	Function
A0~A15, BA0~BA2	Address/Bank input
DQ0~DQ63	Data Input / Output.
DQS0~DQS7	Data strobes
/DQS0~/DQS7	Differential Data strobes
CK0, /CK0,CK1, /CK1	Clock Input. (Differential pair)
CKE0, CKE1	Clock Enable Input.
ODT0, ODT1	On-die termination control line
/CS0, /CS1	DIMM Rank Select Lines.
/RAS	Row Address Strobe
/CAS	Column Address Strobe
/WE	Write Enable
DM0~DM7	Data masks/high data strobes
VDD	Voltage power supply
V_{REF}DQ/ V_{REF}CA	Power Supply for Reference
VDDSPD	SPD EEPROM Power Supply
SA0~SA2	I2C serial bus address select for EEPROM
SCL	I2C serial bus clock for EEPROM
SDA	I2C serial bus data for EEPROM
VSS	Ground
/RESET	Set DRAMs Known State
VTT	SDRAM I/O termination supply
NC	No Connection

Dimensions (Unit: millimeter)



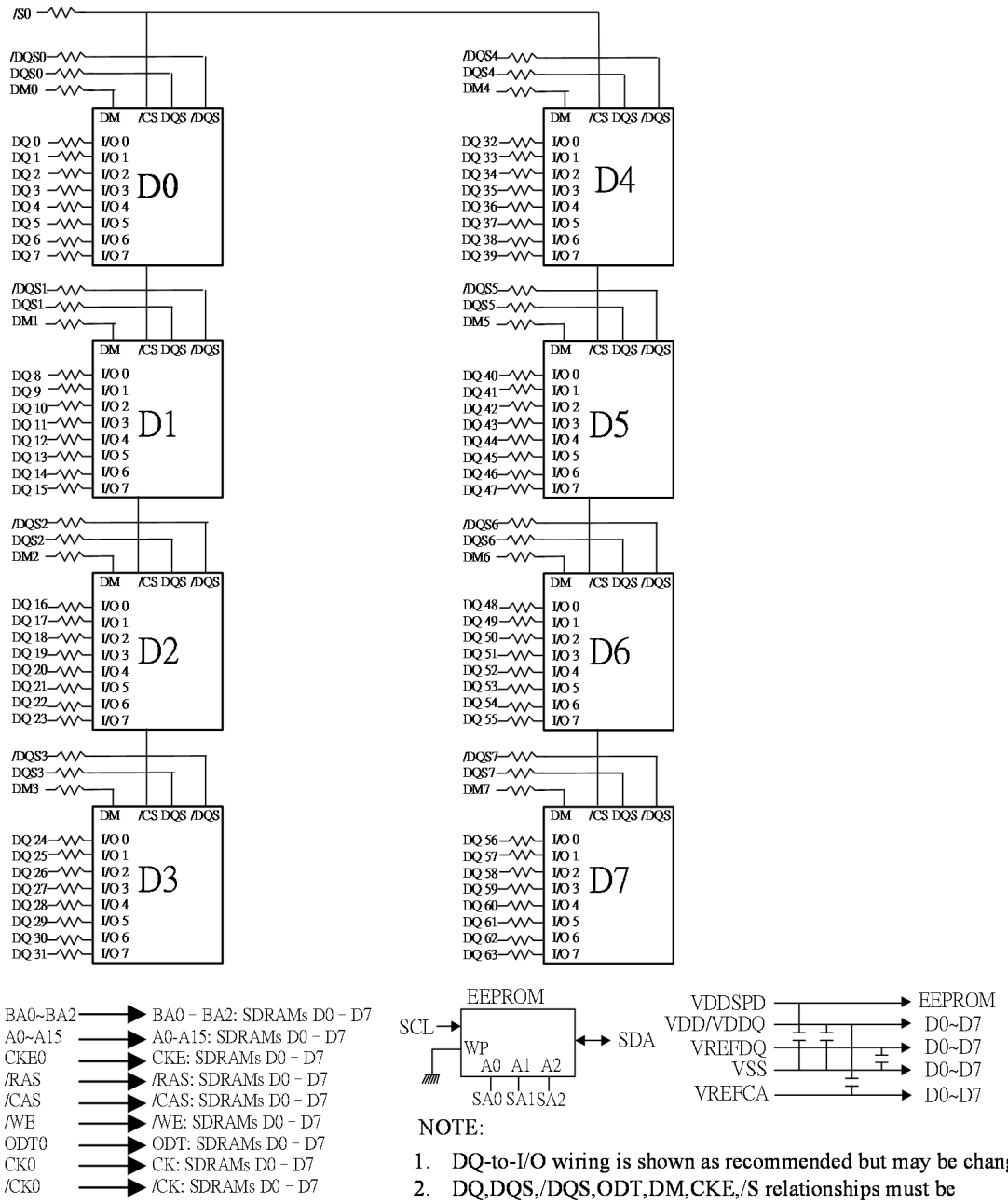
Note:
1. Tolerances on all dimensions +/-0.15mm unless otherwise specified.

Pin Assignments

Pin No	Pin Name	Pin No	Pin Name	Pin No	Pin Name	Pin No	Pin Name	Pin No	Pin Name	Pin No	Pin Name
01	VREFDQ	69	DQ27	137	DQS4	02	VSS	70	DQ31	138	VSS
03	VSS	71	VSS	139	VSS	04	DQ4	72	VSS	140	DQ38
05	DQ0	73	CKE0	141	DQ34	06	DQ5	74	CKE1,NC	142	DQ39
07	DQ1	75	VDD	143	DQ35	08	VSS	76	VDD	144	VSS
09	VSS	77	NC	145	VSS	10	/DQS0	78	A15	146	DQ44
11	DM0	79	BA2	147	DQ40	12	DQS0	80	A14	148	DQ45
13	VSS	81	VDD	149	DQ41	14	VSS	82	VDD	150	VSS
15	DQ2	83	A12	151	VSS	16	DQ6	84	A11	152	/DQS5
17	DQ3	85	A9	153	DM5	18	DQ7	86	A7	154	DQS5
19	VSS	87	VDD	155	VSS	20	VSS	88	VDD	156	VSS
21	DQ8	89	A8	157	DQ42	22	DQ12	90	A6	158	DQ46
23	DQ9	91	A5	159	DQ43	24	DQ13	92	A4	160	DQ47
25	VSS	93	VDD	161	VSS	26	VSS	94	VDD	162	VSS
27	/DQS1	95	A3	163	DQ48	28	DM1	96	A2	164	DQ52
29	DQS1	97	A1	165	DQ49	30	/RESET	98	A0	166	DQ53
31	VSS	99	VDD	167	VSS	32	VSS	100	VDD	168	VSS
33	DQ10	101	CK0	169	/DQS6	34	DQ14	102	CK1,NC	170	DM6
35	DQ11	103	/CK0	171	DQS6	36	DQ15	104	/CK1,NC	172	VSS
37	VSS	105	VDD	173	VSS	38	VSS	106	VDD	174	DQ54
39	DQ16	107	A10/AP	175	DQ50	40	DQ20	108	BA1	176	DQ55
41	DQ17	109	BA0	177	DQ51	42	DQ21	110	/RAS	178	VSS
43	VSS	111	VDD	179	VSS	44	VSS	112	VDD	180	DQ60
45	/DQS2	113	/WE	181	DQ56	46	DM2	114	/CS0	182	DQ61
47	DQS2	115	/CAS	183	DQ57	48	VSS	116	ODT0	184	VSS
49	VSS	117	VDD	185	VSS	50	DQ22	118	VDD	186	/DQS7
51	DQ18	119	A13	187	DM7	52	DQ23	120	ODT1,NC	188	DQS7
53	DQ19	121	/CS1,NC	189	VSS	54	VSS	122	NC	190	VSS
55	VSS	123	VDD	191	DQ58	56	DQ28	124	VDD	192	DQ62
57	DQ24	125	TEST	193	DQ59	58	DQ29	126	VREFCA	194	DQ63
59	DQ25	127	VSS	195	VSS	60	VSS	128	VSS	196	VSS
61	VSS	129	DQ32	197	SA0	62	/DQS3	130	DQ36	198	NC
63	DM3	131	DQ33	199	VDDSPD	64	DQS3	132	DQ37	200	SDA
65	VSS	133	VSS	201	SA1	66	VSS	134	VSS	202	SCL
67	DQ26	135	/DQS4	203	Vtt	68	DQ30	136	DM4	204	Vtt

/CS1,ODT1,CKE1：Used for dual-rank SO-DIMMs; NC on single-rank SO-DIMMs.
CK1 and /CK1：Used for dual-rank SO-DIMMs; not used on single-rank SO-DIMMs but terminated.

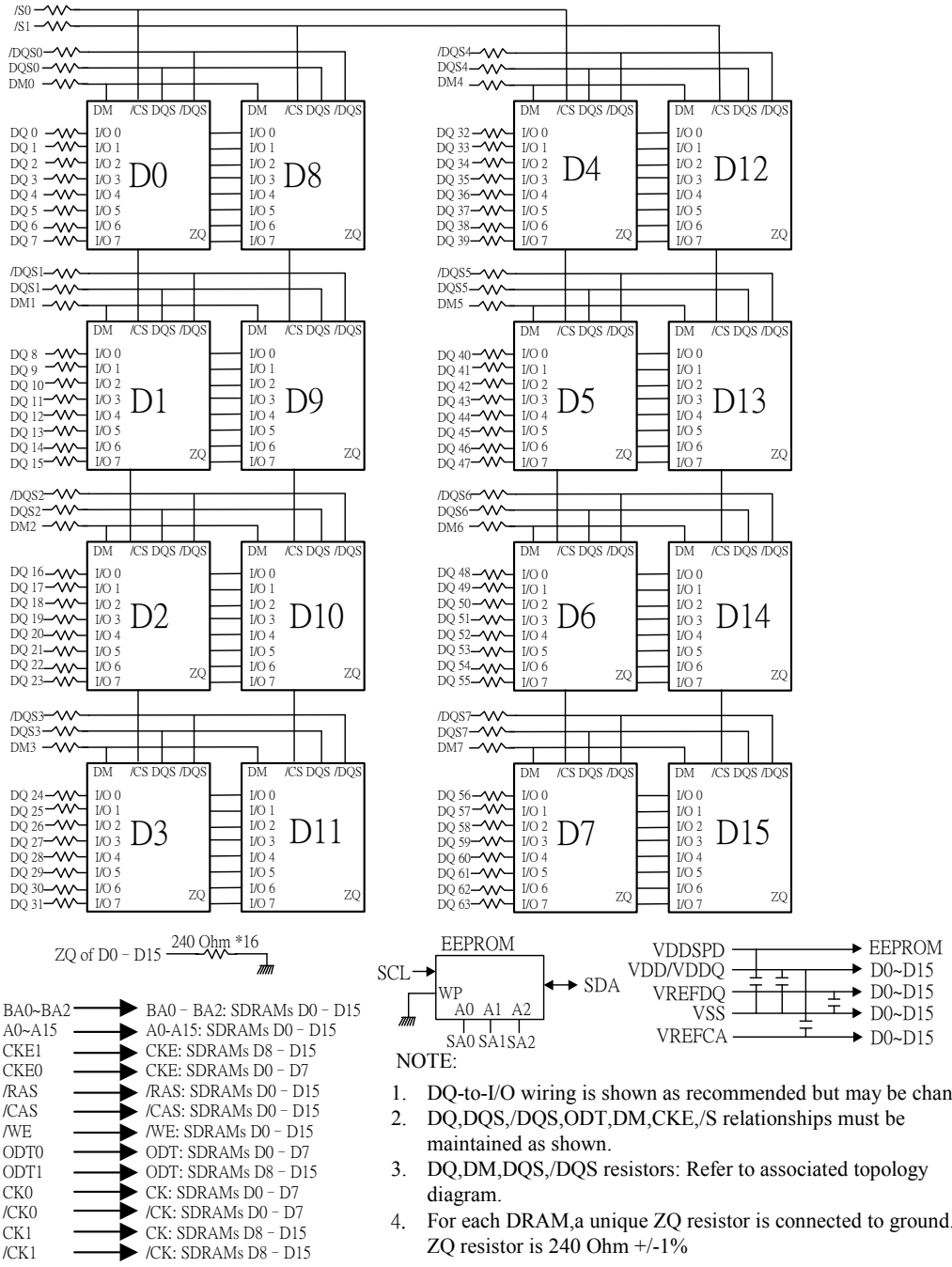
Block Diagram
4GB, 512Mx64 Module(1 Rank x8)



NOTE:

1. DQ-to-I/O wiring is shown as recommended but may be changed.
2. DQ,DQS,/DQS,ODT,DM,CKE,/S relationships must be maintained as shown.
3. DQ,DM,DQS,/DQS resistors: Refer to associated topology diagram.

8GB, 1Gx64 Module(2 Rank x8)



NOTE:

1. DQ-to-I/O wiring is shown as recommended but may be changed.
2. DQ,DQS,/DQS,ODT,DM,CKE,/S relationships must be maintained as shown.
3. DQ,DM,DQS,/DQS resistors: Refer to associated topology diagram.
4. For each DRAM,a unique ZQ resistor is connected to ground. The ZQ resistor is 240 Ohm +/-1%

Operating Temperature Condition

Parameter	Symbol	Rating	Unit	Note
Operating Temperature	TOPER	0 to 85	℃	1,2

Note:
1. Operating Temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JESD51-2 standard.
2. At 0 - 85°C, operation temperature range are the temperature which all DRAM specification will be supported.

Absolute Maximum DC Ratings

Parameter	Symbol	Value	Unit	Note
Voltage on V_{DD} relative to Vss	VDD	-0.4 ~ 1.80	V	1
Voltage on V_{DDQ} pin relative to Vss	VDDQ	-0.4 ~ 1.80	V	1
Voltage on any pin relative to Vss	VIN, VOUT	-0.4 ~ 1.80	V	1
Storage temperature	T_{STG}	-55~+100	℃	1,2

Note:
1. Stress greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Storage Temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JESD51-2 standard.

AC & DC Operating Conditions

Recommended DC operating conditions

Parameter	Symbol	Voltage	Rating			Unit	Notes
			Min	Typ.	Max		
Supply voltage	VDD	1.35V	1.283	1.35	1.45	V	1, 2
Supply voltage for Output	VDDQ	1.35V	1.283	1.35	1.45	V	
I/O Reference Voltage (DQ)	$VREF_{DQ}$(DC)	1.35V	0.49*VDD		0.51*VDD	V	3
AC Input Logic High	VIH(AC)	1.35V	VREF+0.135	-	-	V	
AC Input Logic Low	VIL(AC)	1.35V	-	-	VREF-0.135	V	
DC Input Logic High	VIH(DC)	1.35V	V_{REF}+0.09	-	VDD	V	
DC Input Logic Low	VIL(DC)	1.35V	VSS	-	V_{REF}-0.09	V	

Note:
1.Under all conditions VDDQ must be less than or equal to VDD.
2.VDDQ tracks with VDD, AC parameters are measured with VDD and VDDQ tied together.
3.Peak to peak AC noise on VREF may not allow deviate from VREF(DC) by more than +/-1% VDD.

AC Input Level for Differential Signals

Parameter	Symbol	Value		Unit	Note
Differential Input Logical High	V_{IHdiff}	+200	-	mV	
Differential Input Logical Low	V_{ILdiff}	-	-200		

IDD Specification parameters Definition(IDD values are for full operating range of Voltage and Temperature)
4GB, 512Mx64 Module(1 Rank x8)

Parameter	Symbol	DDR3L 1600 CL11	Unit
Operating One bank Active-Precharge current; tCK = tCK(IDD), tRC = tRC(IDD), tRAS = tRASmin(IDD); CKE is HIGH, /CS is HIGH between valid commands;Address bus inputs are SWITCHING; Data bus inputs are SWITCHING	IDD0	208	mA
Operating One bank Active-read-Precharge current; IOUT = 0mA; BL = 8, CL = CL(IDD), AL = 0; tCK = tCK(IDD), tRC = tRC (IDD), tRAS = tRASmin(IDD), tRCD = tRCD(IDD); CKE is HIGH, /CS is HIGH between valid commands; Address bus inputs are SWITCHING; Data pattern is same as IDD4W	IDD1	288	mA
Precharge power-down current; All banks idle; tCK = tCK(IDD); CKE is LOW; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING	IDD2P	64	mA
Precharge quiet standby current; All banks idle; tCK = tCK(IDD); CKE is HIGH, /CS is HIGH; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING	IDD2Q	80	mA
Precharge standby current; All banks idle; tCK = tCK(IDD); CKE is HIGH, /CS is HIGH; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING	IDD2N	88	mA
Active power - down current; All banks open; tCK = tCK(IDD); CKE is LOW; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING	IDD3P	80	mA
Active standby current; All banks open; tCK = tCK(IDD), tRAS = tRASmax(IDD), tRP = tRP(IDD); CKE is HIGH, /CS is HIGH between valid commands; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING	IDD3N	168	mA
Operating burst read current; All banks open, Continuous burst reads, IOUT = 0mA; BL = 4, CL = CL(IDD), AL = 0; tCK = tCK(IDD), tRAS = tRASmax(IDD), tRP = tRP(IDD); CKE is HIGH, /CS is HIGH between valid commands; Address bus inputs are SWITCHING; Data pattern is same as IDD4W	IDD4R	512	mA
Operating burst write current; All banks open, Continuous burst writes; BL = 8, CL = CL(IDD), AL = 0; tCK = tCK(IDD), tRAS = tRASmax(IDD), tRP = tRP(IDD); CKE is HIGH, /CS is HIGH between valid commands; Address bus inputs are SWITCHING; Data bus inputs are SWITCHING IDD4R	IDD4W	504	mA
Burst refresh current; tCK = tCK(IDD); Refresh command at every tRFC(IDD) interval; CKE is HIGH, /CS is HIGH between valid commands; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING	IDD5	1520	mA
Self refresh current; CK and /CK at 0V; CKE ≒ 0.2V; Other control and address bus inputs are FLOATING; Data bus inputs are FLOATING	IDD6	96	mA
Operating bank interleave read current; All bank interleaving reads, IOUT = 0mA; BL = 8, CL = CL(IDD), AL = tRCD(IDD)-1*tCK(IDD); tCK = tCK(IDD), Trc = tRC(IDD), tRRD = tRRD(IDD), tRCD = 1*tCK(IDD); CKE is HIGH, CS is HIGH between valid commands;Address bus inputs are STABLE during DESELECTs; Data pattern is same as IDD4R;	IDD7	968	mA

Note: 1.Module IDD was calculated on the specific brand DRAM component IDD and can be differently measured according to DQ loading capacitor.

IDD Specification parameters Definition(IDD values are for full operating range of Voltage and Temperature)
8GB, 1Gx64 Module(2 Rank x8)

Parameter	Symbol	DDR3L 1600 CL11	Unit
Operating One bank Active-Precharge current; tCK = tCK(IDD), tRC = tRC(IDD), tRAS = tRASmin(IDD); CKE is HIGH, /CS is HIGH between valid commands;Address bus inputs are SWITCHING; Data bus inputs are SWITCHING	IDD0	296	mA
Operating One bank Active-read-Precharge current; IOUT = 0mA; BL = 8, CL = CL(IDD), AL = 0; tCK = tCK(IDD), tRC = tRC (IDD), tRAS = tRASmin(IDD), tRCD = tRCD(IDD); CKE is HIGH, /CS is HIGH between valid commands; Address bus inputs are SWITCHING; Data pattern is same as IDD4W	IDD1	376	mA
Precharge power-down current; All banks idle; tCK = tCK(IDD); CKE is LOW; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING	IDD2P	128	mA
Precharge quiet standby current; All banks idle; tCK = tCK(IDD); CKE is HIGH, /CS is HIGH; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING	IDD2Q	160	mA
Precharge standby current; All banks idle; tCK = tCK(IDD); CKE is HIGH, /CS is HIGH; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING	IDD2N	176	mA
Active power - down current; All banks open; tCK = tCK(IDD); CKE is LOW; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING	IDD3P	160	mA
Active standby current; All banks open; tCK = tCK(IDD), tRAS = tRASmax(IDD), tRP = tRP(IDD); CKE is HIGH, /CS is HIGH between valid commands; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING	IDD3N	336	mA
Operating burst read current; All banks open, Continuous burst reads, IOUT = 0mA; BL = 4, CL = CL(IDD), AL = 0; tCK = tCK(IDD), tRAS = tRASmax(IDD), tRP = tRP(IDD); CKE is HIGH, /CS is HIGH between valid commands; Address bus inputs are SWITCHING; Data pattern is same as IDD4W	IDD4R	600	mA
Operating burst write current; All banks open, Continuous burst writes; BL = 8, CL = CL(IDD), AL = 0; tCK = tCK(IDD), tRAS = tRASmax(IDD), tRP = tRP(IDD); CKE is HIGH, /CS is HIGH between valid commands; Address bus inputs are SWITCHING; Data bus inputs are SWITCHING IDD4R	IDD4W	592	mA
Burst refresh current; tCK = tCK(IDD); Refresh command at every tRFC(IDD) interval; CKE is HIGH, /CS is HIGH between valid commands; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING	IDD5	1608	mA
Self refresh current; CK and /CK at 0V; CKE ≒ 0.2V; Other control and address bus inputs are FLOATING; Data bus inputs are FLOATING	IDD6	192	mA
Operating bank interleave read current; All bank interleaving reads, IOUT = 0mA; BL = 8, CL = CL(IDD), AL = tRCD(IDD)-1*tCK(IDD); tCK = tCK(IDD), Trc = tRC(IDD), tRRD = tRRD(IDD), tRCD = 1*tCK(IDD); CKE is HIGH, CS is HIGH between valid commands;Address bus inputs are STABLE during DESELECTs; Data pattern is same as IDD4R;	IDD7	1056	mA

Note: 1.Module IDD was calculated on the specific brand DRAM component IDD and can be differently measured according to DQ loading capacitor.

Timing Parameters & Specifications

Speed		DDR3-800		DDR3-1066		DDR3-1333		DDR3-1600		DDR3-1866		Units
Parameter	**Symbol**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	
Average Clock Period	tCK(avg)	2.5	3.3	1.875	<2.5	1.5	<1.875	1.25	<1.5	1.071	<1.25	ns
Average high pulse width	tCH(avg)	0.47	0.53	0.47	0.53	0.47	0.53	0.47	0.53	0.47	0.53	tCK(avg)
Average low pulse width	tCL(avg)	0.47	0.53	0.47	0.53	0.47	0.53	0.47	0.53	0.47	0.53	tCK(avg)
Absolute clock HIGH pulse width	tCH(abs)	0.43	-	0.43	-	0.43	-	0.43	-	0.43	-	tCK(avg)
Absolute clock Low pulse width	tCL(abs)	0.43	-	0.43	-	0.43	-	0.43	-	0.43	-	tCK(avg)
DQS,$\overline{DQS}$ to DQ skew, per group, per access	tDQSQ	-	200	-	150	-	125	-	100	-	85	ps
DQ output hold time from DQS, $\overline{DQS}$	tQH	0.38	-	0.38	-	0.38	-	0.38	-	0.38	-	tCK(avg)
DQ low-impedance time from CK, $\overline{CK}$	tLZ(DQ)	-800	400	-600	300	-500	250	-450	225	-390	195	ps
DQ high-impedance time from CK, $\overline{CK}$	tHZ(DQ)	-	400	-	300	-	250	-	225	-	195	ps
Data setup time to DQS, DQS referenced to $V_{IH}(AC)V_{IL}(AC)$ levels	tDS	125	-	75	-	30	-	10	-	-	-	ps
Data hold time from DQS, DQS referenced to $V_{IH}(DC)V_{IL}(DC)$ levels	tDH	150	-	100	-	65	-	45	-	20	-	ps
DQ and DM Input pulse width for each input	tDIPW	600	-	490	-	400	-	360	-	320	-	ps
DQS, $\overline{DQS}$ differential READ Preamble	tRPRE	0.9	-	0.9	-	0.9	-	0.9	-	0.9	-	tCK(avg)
DQS, $\overline{DQS}$ differential READ Postamble	tRPST	0.3	-	0.3	-	0.3	-	0.3	-	0.3	-	tCK(avg)
DQS, $\overline{DQS}$ differential output high time	tQSH	0.38	-	0.38	-	0.4	-	0.4	-	0.4	-	tCK(avg)
DQS, $\overline{DQS}$ differential output low time	tQSL	0.38	-	0.38	-	0.4	-	0.4	-	0.4	-	tCK(avg)
DQS, $\overline{DQS}$ differential WRITE Preamble	tWPRE	0.9	-	0.9	-	0.9	-	0.9	-	0.9	-	tCK(avg)
DQS, $\overline{DQS}$ differential WRITE Postamble	tWPST	0.3	-	0.3	-	0.3	-	0.3	-	0.3	-	tCK(avg)
DQS, $\overline{DQS}$ rising edge output access time from rising CK, $\overline{CK}$	tDQSCK	-400	400	-300	300	-255	255	-225	225	-195	195	ps
DQS, $\overline{DQS}$ low-impedance time (Referenced from RL-1)	tLZ(DQS)	-800	400	-600	300	-500	250	-450	225	-390	195	ps
DQS, $\overline{DQS}$ high-impedance time (Referenced from RL+BL/2)	tHZ(DQS)	-	400	-	300	-	250	-	225	-	195	ps
DQS, $\overline{DQS}$ differential input low pulse width	tDQSL	0.45	0.55	0.45	0.55	0.45	0.55	0.45	0.55	0.45	0.55	tCK(avg)
DQS, $\overline{DQS}$ differential input high pulse width	tDQSH	0.45	0.55	0.45	0.55	0.45	0.55	0.45	0.55	0.45	0.55	tCK(avg)
DQS, $\overline{DQS}$ rising edge to CK, $\overline{CK}$ rising edge	tDQSS	-0.25	0.25	-0.25	0.25	-0.25	0.25	-0.27	0.27	-0.27	0.27	tCK(avg)
DQS,$\overline{DQS}$ falling edge setup time to CK, $\overline{CK}$ rising edge	tDSS	0.2	-	0.2	-	0.2	-	0.18	-	0.18	-	tCK(avg)
DQS,$\overline{DQS}$ falling edge hold time to CK, $\overline{CK}$ rising edge	tDSH	0.2	-	0.2	-	0.2	-	0.18	-	0.18	-	tCK(avg)
DLL locking time	tDLLK	512	-	512	-	512	-	512	-	512	-	nCK
internal READ Command to PRECHARGE Command delay	tRTP	max (4nCK,7.5 ns)	-	max (4nCK,7.5 ns)	-	max (4nCK,7.5ns)	-	max (4nCK,7.5 ns)	-	max (4nCK,7.5 ns)	-	
Delay from start of internal write transaction to internal read command	tWTR	max (4nCK,7.5 ns)	-	max (4nCK,7.5 ns)	-	max (4nCK,7.5ns)	-	max (4nCK,7.5 ns)	-	max (4nCK,7.5 ns)	-	
WRITE recovery time	tWR	15	-	15	-	15	-	15	-	15	-	ns
Mode Register Set command cycle time	tMRD	4	-	4	-	4	-	4	-	4	-	nCK
Mode Register Set command update delay	tMOD	max (12nCK,15 ns)	-	max (12nCK,15 ns)	-	max (12nCK, 15 ns)	-	max (12nCK,15 ns)	-	max (12nCK,15 ns)	-	

Speed		DDR3-800		DDR3-1066		DDR3-1333		DDR3-1600		DDR3-1866		Units
Parameter	Symbol	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
Auto precharge write recovery + precharge time	tDAL(min)	WR + roundup (tRP / tCK(AVG))										nCK
Multi-Purpose Register Recovery Time	tMPRR	1	-	1	-	1	-	1	-	1	-	nCK
ACTIVE to ACTIVE command period for 1KB page size	tRRD	max (4nCK,10ns)	-	max (4nCK,7.5 ns)	-	max (4nCK,6ns)	-	max (4nCK,6ns)	-	max (4nCK, 5ns)	-	
ACTIVE to ACTIVE command period for 2KB page size	tRRD	max (4nCK,10ns)	-	max (4nCK,10ns)	-	max (4nCK,7.5ns)	-	max (4nCK,7.5 ns)	-	max (4nCK, 6ns)	-	
Four activate window for 1KB page size	tFAW	40	-	37.5	-	30	-	30	-	27	-	ns
Four activate window for 2KB page size	tFAW	50	-	50	-	45	-	40	-	35	-	ns
Command and Address setup time to CK, CK referenced to V_{IH}(AC) / V_{IL}(AC) levels	tIS	350	-	275	-	190	-	170	-	-	-	ps
Command and Address hold time from CK, CK referenced to V_{IH}(DC) / V_{IL}(DC) levels	tIH	275		200		140		120	-	100	-	ps
Control & Address Input pulse width for each input	tIPW	900	-	780	-	620	-	560	-	535	-	ps
Power-up and RESET calibration time	tZQinitI	512	-	512	-	512	-	512	-	max(512nCK,640ns)	-	nCK
Exit Reset from CKE HIGH to a valid command	tXPR	max(5nCK, tRFC + 10ns)	-	max(5nCK, tRFC + 10ns)	-	max(5nCK, tRFC + 10ns)	-	max(5nCK, tRFC + 10ns)	-	max(5nCK, tRFC(min) + 10ns)	-	
Exit Self Refresh to commands not requiring a locked DLL	tXS	max(5nCK,tRFC + 10ns)	-	max(5nCK,tRFC + 10ns)	-	max(5nCK,tRFC + 10ns)	-	max(5nCK,tRFC + 10ns)	-	max(5nCK,tRFC(min) +10ns)	-	
Exit Self Refresh to commands requiring a locked DLL	tXSDLL	tDLLK(min)	-	tDLLK(min)	-	tDLLK(min)	-	tDLLK(min)	-	tDLLK(min)	-	nCK
Minimum CKE low width for Self refresh entry to exit timing	tCKESR	tCKE(min) + 1tCK	-	tCKE(min) + 1tCK	-	tCKE(min) + 1tCK	-	tCKE(min) + 1tCK	-	tCKE(min) + 1nCK	-	
Valid Clock Requirement after Self Refresh Entry (SRE) or Power-Down Entry (PDE)	tCKSRE	max(5nCK, 10ns)	-	max(5nCK, 10ns)	-	max(5nCK, 10ns)	-	max(5nCK, 10ns)	-	max(5nCK, 10ns)	-	
Valid Clock Requirement before Self Refresh Exit (SRX) or Power-Down Exit (PDX) or Reset Exit	tCKSRX	max(5nCK, 10ns)	-	max(5nCK, 10ns)	-	max(5nCK, 10ns)	-	max(5nCK, 10ns)	-	max(5nCK, 10ns)	-	
Exit Power Down with DLL on to any valid command;Exit Precharge Power Down with DLL frozen to commands not requiring a locked DLL	tXP	max (3nCK, 7.5ns)	-	max (3nCK, 7.5ns)	-	max (3nCK,6ns)	-	max (3nCK,6ns)	-	max(3nCK,6ns)	-	
Exit Precharge Power Down with DLL frozen to commands requiring a locked DLL	tXPDLL	max (10nCK, 24ns)	-	max (10nCK, 24ns)	-	max (10nCK, 24ns)	-	max (10nCK, 24ns)	-	max(10nCK,24ns)	-	
CKE minimum pulse width	tCKE	max (3nCK, 7.5ns)	-	max (3nCK, 5.625ns)	-	max (3nCK, 5.625ns)	-	max (3nCK,5ns)	-	max(3nCK,5ns)	-	
Asynchronous RTT turn-on delay (Power-Down with DLL frozen)	tAONPD	2	8.5	2	8.5	2	8.5	2	8.5	2	8.5	ns
Asynchronous RTT turn-off delay (Power-Down with DLL frozen)	tAOFPD	2	8.5	2	8.5	2	8.5	2	8.5	2	8.5	ns
RTT turn-on	tAON	-400	400	-300	300	-250	250	-225	225	-195	195	ps
RTT_NOM and RTT_WR turn-off time from ODTLoff reference	tAOF	0.3	0.7	0.3	0.7	0.3	0.7	0.3	0.7	0.3	0.7	tCK(avg)

SERIAL PRESENCE DETECT SPECIFICATION

TS512MSK64W6H Serial Presence Detect			
Byte No.	**Function Described**	**Standard Specification**	**Vendor Part**
0	Number of SPD Bytes written / SPD device size / CRC coverage during module production	CRC:0-116Byte SPD Byte use: 176Byte SPD Byte total: 256Byte	92
1	SPD Revision	Version 1.0	10
2	Key Byte / DRAM Device Type	DDR3 SDRAM	0B
3	Key Byte / Module Type	SO-DIMM	03
4	SDRAM Density and Banks	4Gb 8banks	04
5	SDRAM Addressing	ROW:16, Column:10	21
6	Module Nominal Voltage, VDD	1.35V and 1.5V	02
7	Module Organization	1 Rank / x8	01
8	Module Memory Bus Width	Non ECC, 64 bits	03
9	Fine Timebase Dividend and Divisor	2.5 ps	52
10-11	Medium Timebase Dividend and Divisor	0.125 ns	01, 08
12	SDRAM Minimum Cycle Time (tCKmin)	1.25 ns	0A
13	Reserved	-	00
14-15	CAS Latencies Supported	5, 6, 7, 8, 9, 10, 11	FE, 00
16	Minimum CAS Latency Time (tAAmin)	13.125 ns	69
17	Minimum Write Recovery Time (tWRmin)	15 ns	78
18	Minimum /RAS to /CAS Delay Time (tRCDmin)	13.125 ns	69
19	Minimum Row Active to Row Active Delay Time (tRRDmin)	6 ns	30
20	Minimum Row Precharge Time (tRPmin)	13.125 ns	69
21	Upper Nibble for tRAS and tRC	See byte 23, 23	11
22	Minimum Active to Precharge Time (tRASmin)	35 ns	18
23	Minimum Active to Active/Refresh Time (tRCmin)	48.125 ns	81
24-25	Minimum Refresh Recovery Time (tRFCmin)	260 ns	20,08
26	Minimum Internal Write to Read Command Delay Time (tWTmin)	7.5 ns	3C
27	Minimum Internal Read to Precharge Command Delay Time (tRTPmin)	7.5 ns	3C
28-29	Minimum Four Active Window Delay Time (tFAWmin)	30 ns	00, F0
30	SDRAM Optional Features	DLL-Off Mode, RZQ/6, RZQ/7	83
31	SDRAM Thermal and Refresh Options	No ODTS, No ASR	01
32	Module thermal sensor	Not support TS	00

33	SDRAM device type	Standard	00
34	Fine Offset for Minimum Cycle Time(tCKmin)	0 ps	00
35	Fine Offset for Minimum CAS Latency Time (tAAmin)	0 ps	00
36	Fine Offset for Minimum RAS# to CAS# Delay Time (tRCDmin)	0 ps	00
37	Minimum Row Precharge Delay Time (tRPmin)	0 ps	00
38	Fine Offset for Minimum Active to Active/Refresh Delay Time (tRCmin)	0 ps	00
39-40	Reserved	-	00
41	SDRAM Maximum Active Count (MAC) Value	Untested MAC	00
42-59	Reserved	-	00
60	Module Nominal Height	29 < Height ≤ 30 mm	0F
61	Module Max Thickness	Planar Double Sides	11
62	Reference Raw Card Used	Revision 1, R/C B	21
63	Address Mapping from Edge Connector to DRAM	Standard	00
64-116	Reserved	-	00
117-118	Module Manufacturer ID Code	Transcend Information	01, 4F
119	Module Manufacturing Location	Taipei	54
120-121	Module Manufacturing Date	Year, Week	Variable
122-125	Module Serial Number	By Manufacturer	Variable
126-127	Cyclical Redundancy Code	Cyclical Redundancy Code	4A,3E
128-145	Module Part Number	TS512MSK64W6H	54 53 35 31 32 4D 53 4B 36 34 57 36 48 20 20 20 20 20
146-147	Revision Code	-	00
148-149	DRAM Manufacturer ID Code	By Manufacturer	Variable
150-175	Manufacturer Specific Data	By Manufacturer	Variable
176-255	Open for customer use	By Manufacturer	Variable

TS1GSK64W6H Serial Presence Detect			
Byte No.	**Function Described**	**Standard Specification**	**Vendor Part**
0	Number of SPD Bytes written / SPD device size / CRC coverage during module production	CRC:0-116Byte SPD Byte use: 176Byte SPD Byte total: 256Byte	92
1	SPD Revision	Version 1.0	10
2	Key Byte / DRAM Device Type	DDR3 SDRAM	0B
3	Key Byte / Module Type	SO-DIMM	03
4	SDRAM Density and Banks	4Gb 8banks	04
5	SDRAM Addressing	ROW:16, Column:10	21
6	Module Nominal Voltage, VDD	1.35V and 1.5V	02
7	Module Organization	2 Ranks / x8	09
8	Module Memory Bus Width	Non ECC, 64 bits	03
9	Fine Timebase Dividend and Divisor	2.5 ps	52
10-11	Medium Timebase Dividend and Divisor	0.125 ns	01, 08
12	SDRAM Minimum Cycle Time (tCKmin)	1.25 ns	0A
13	Reserved	-	00
14-15	CAS Latencies Supported	5, 6, 7, 8, 9, 10, 11	FE, 00
16	Minimum CAS Latency Time (tAAmin)	13.125 ns	69
17	Minimum Write Recovery Time (tWRmin)	15 ns	78
18	Minimum /RAS to /CAS Delay Time (tRCDmin)	13.125 ns	69
19	Minimum Row Active to Row Active Delay Time (tRRDmin)	6 ns	30
20	Minimum Row Precharge Time (tRPmin)	13.125 ns	69
21	Upper Nibble for tRAS and tRC	See byte 23, 23	11
22	Minimum Active to Precharge Time (tRASmin)	35 ns	18
23	Minimum Active to Active/Refresh Time (tRCmin)	47.125ns	79
24-25	Minimum Refresh Recovery Time (tRFCmin)	260 ns	20, 08
26	Minimum Internal Write to Read Command Delay Time (tWTmin)	7.5 ns	3C
27	Minimum Internal Read to Precharge Command Delay Time (tRTPmin)	7.5 ns	3C
28-29	Minimum Four Active Window Delay Time (tFAWmin)	30 ns	00, F0
30	SDRAM Optional Features	DLL-Off Mode, RZQ/6, RZQ/7	83
31	SDRAM Thermal and Refresh Options	No ODTS, No ASR	01
32	Module thermal sensor	Not support TS	00

33	SDRAM device type	Standard	00
34	Fine Offset for Minimum Cycle Time(tCKmin)	0 ps	00
35	Fine Offset for Minimum CAS Latency Time (tAAmin)	0 ps	00
36	Fine Offset for Minimum RAS# to CAS# Delay Time (tRCDmin)	0 ps	00
37	Minimum Row Precharge Delay Time (tRPmin)	0 ps	00
38	Fine Offset for Minimum Active to Active/Refresh Delay Time (tRCmin)	0 ps	00
39-40	Reserved	-	00
41	SDRAM Maximum Active Count (MAC) Value	Untested MAC	00
42-59	Reserved	-	00
60	Module Nominal Height	29 < Height ≤ 30 mm	0F
61	Module Max Thickness	Planar Double Sides	11
62	Reference Raw Card Used	Revision 1, R/C F	25
63	Address Mapping from Edge Connector to DRAM	Standard	00
64-116	Reserved	-	00
117-118	Module Manufacturer ID Code	Transcend Information	01, 4F
119	Module Manufacturing Location	Taipei	54
120-121	Module Manufacturing Date	Year, Week	Variable
122-125	Module Serial Number	By Manufacturer	Variable
126-127	Cyclical Redundancy Code	Cyclical Redundancy Code	45, 86
128-145	Module Part Number	TS1GSK64W6H	54 53 31 47 53 4B 36 34 57 36 48 20 20 20 20 20 20 20
146-147	Revision Code	-	00
148-149	DRAM Manufacturer ID Code	By Manufacturer	Variable
150-175	Manufacturer Specific Data	By Manufacturer	Variable
176-255	Open for customer use	By Manufacturer	Variable