TS512MLK64V3H TS1GLK64V3H
TS512MLK64V6H TS1GLK64V6H

240Pin DDR3 1333/1600 UDIMM
4GB~8GB Based on 512Mx8

Description

DDR3 Unbuffered DIMM is high-speed, low power memory module that use 512Mx8bits DDR3 SDRAM in FBGA package and a 2048 bits serial EEPROM on a 240-pin printed circuit board. DDR3 Unbuffered DIMM is a Dual In-Line Memory Module and is intended for mounting into 240-pin edge connector sockets.
Synchronous design allows precise cycle control with the use of system clock. Data I/O transactions are possible on both edges of DQS. Range of operation frequencies, programmable latencies allow the same device to be useful for a variety of high bandwidth, high performance memory system applications.

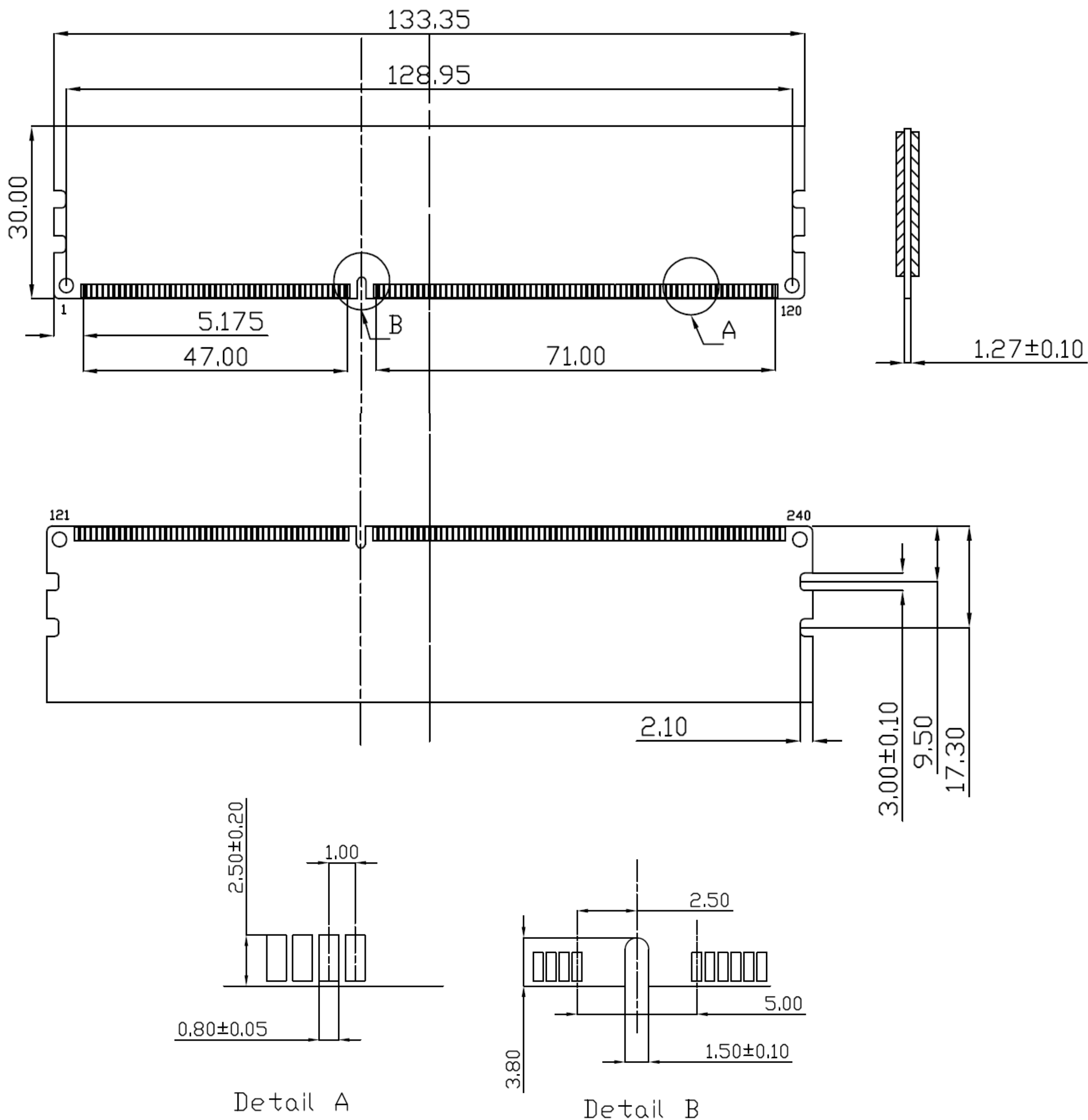
Features

- RoHS compliant products.
- JEDEC standard 1.5V ± 0.075V Power supply
- VDDQ=1.5V ± 0.075V
- Clock Freq: 667MHZ for 1333Mb/s/Pin.
- Clock Freq: 800MHZ for 1600Mb/s/Pin.
- Programmable CAS Latency: 6, 7, 8, 9, 10, 11
- Programmable Additive Latency (Posted /CAS): 0,CL-2 or CL-1 clock
- Programmable /CAS Write Latency (CWL) = 7 (DDR3-1333), 8(DDR3-1600)
- 8 bit pre-fetch
- Burst Length: 4, 8
- Bi-directional Differential Data-Strobe
- Internal calibration through ZQ pin
- On Die Termination with ODT pin
- Serial presence detect with EEPROM
- Asynchronous reset

Pin Identification

Symbol	Function
A0~A15, BA0~BA2	Address/Bank input
DQ0~DQ63	Bi-direction data bus.
DQS0~DQS7	Data strobes
/DQS0~/DQS7	Differential Data strobes
CK0, /CK0,CK1, /CK1	Clock Input. (Differential pair)
CKE0, CKE1	Clock Enable Input.
ODT0, ODT1	On-die termination control line
/S0, /S1	DIMM rank select lines.
/RAS	Row address strobe
/CAS	Column address strobe
/WE	Write Enable
DM0~DM7	Data masks/high data strobes
VDD	Core power supply
VDDQ	I/O driver power supply
V_{REF}DQ	I/O reference supply
V_{REF}CA	Command/address reference supply
V_{DD}SPD	SPD EEPROM power supply
SA0~SA2	I2C serial bus address select for EEPROM
SCL	I2C serial bus clock for EEPROM
SDA	I2C serial bus data for EEPROM
VSS	Ground
/RESET	Set DRAMs Known State
VTT	SDRAM I/O termination supply
NC	No Connection

Dimensions (Unit: millimeter)



Note:
1. Tolerances on all dimensions +/-0.15mm unless otherwise specified.
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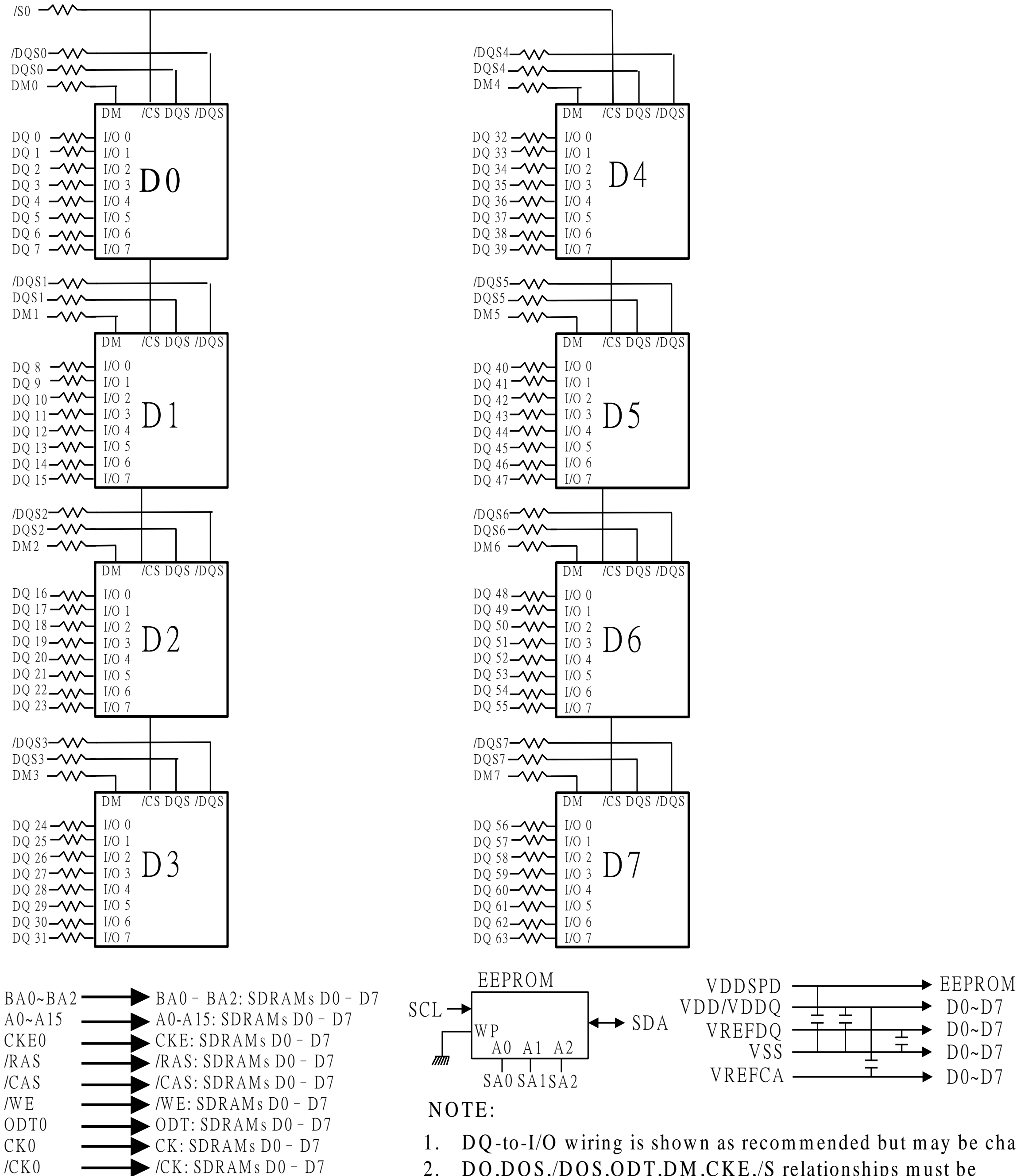
Pin Assignments

Pin No	Pin Name	Pin No	Pin Name	Pin No	Pin Name	Pin No	Pin Name	Pin No	Pin Name	Pin No	Pin Name
01	VREFDQ	41	VSS	81	DQ32	121	VSS	161	NC	201	DQ37
02	VSS	42	NC	82	DQ33	122	DQ4	162	NC	202	VSS
03	DQ0	43	NC	83	VSS	123	DQ5	163	VSS	203	DM4
04	DQ1	44	VSS	84	/DQS4	124	VSS	164	NC	204	NC
05	VSS	45	NC	85	DQS4	125	DM0	165	NC	205	VSS
06	/DQS0	46	NC	86	VSS	126	NC	166	VSS	206	DQ38
07	DQS0	47	VSS	87	DQ34	127	VSS	167	NC	207	DQ39
08	VSS	48	NC	88	DQ35	128	DQ6	168	/RESET	208	VSS
09	DQ2	49	NC	89	VSS	129	DQ7	169	CKE1,NC	209	DQ44
10	DQ3	50	CKE0	90	DQ40	130	VSS	170	VDD	210	DQ45
11	VSS	51	VDD	91	DQ41	131	DQ12	171	A15	211	VSS
12	DQ8	52	BA2	92	VSS	132	DQ13	172	A14	212	DM5
13	DQ9	53	NC	93	/DQS5	133	VSS	173	VDD	213	NC
14	VSS	54	VDD	94	DQS5	134	DM1	174	A12	214	VSS
15	/DQS1	55	A11	95	VSS	135	NC	175	A9	215	DQ46
16	DQS1	56	A7	96	DQ42	136	VSS	176	VDD	216	DQ47
17	VSS	57	VDD	97	DQ43	137	DQ14	177	A8	217	VSS
18	DQ10	58	A5	98	VSS	138	DQ15	178	A6	218	DQ52
19	DQ11	59	A4	99	DQ48	139	VSS	179	VDD	219	DQ53
20	VSS	60	VDD	100	DQ49	140	DQ20	180	A3	220	VSS
21	DQ16	61	A2	101	VSS	141	DQ21	181	A1	221	DM6
22	DQ17	62	VDD	102	/DQS6	142	VSS	182	VDD	222	NC
23	VSS	63	CK1,NC	103	DQS6	143	DM2	183	VDD	223	VSS
24	/DQS2	64	/CK1,NC	104	VSS	144	NC	184	CK0	224	DQ54
25	DQS2	65	VDD	105	DQ50	145	VSS	185	/CK0	225	DQ55
26	VSS	66	VDD	106	DQ51	146	DQ22	186	VDD	226	VSS
27	DQ18	67	VREFCA	107	VSS	147	DQ23	187	NC	227	DQ60
28	DQ19	68	NC	108	DQ56	148	VSS	188	A0	228	DQ61
29	VSS	69	VDD	109	DQ57	149	DQ28	189	VDD	229	VSS
30	DQ24	70	A10/AP	110	VSS	150	DQ29	190	BA1	230	DM7
31	DQ25	71	BA0	111	/DQS7	151	VSS	191	VDD	231	NC
32	VSS	72	VDD	112	DQS7	152	DM3	192	/RAS	232	VSS
33	/DQS3	73	/WE	113	VSS	153	NC	193	/S0	233	DQ62
34	DQS3	74	/CAS	114	DQ58	154	VSS	194	VDD	234	DQ63
35	VSS	75	VDD	115	DQ59	155	DQ30	195	ODT0	235	VSS
36	DQ26	76	/S1,NC	116	VSS	156	DQ31	196	A13	236	VDDSPD
37	DQ27	77	ODT1,NC	117	SA0	157	VSS	197	VDD	237	SA1
38	VSS	78	VDD	118	SCL	158	NC	198	NC	238	SDA
39	NC	79	NC	119	SA2	159	NC	199	VSS	239	VSS
40	NC	80	VSS	120	VTT	160	VSS	200	DQ36	240	VTT

/S1,ODT1,CKE1：Used for dual-rank UDIMMs; NC on single-rank UDIMMs.
CK1 and /CK1：Used for dual-rank UDIMMs; not used on single-rank UDIMMs but terminated.

Block Diagram
4GB, 512Mx64 Module(1 Rank x8)

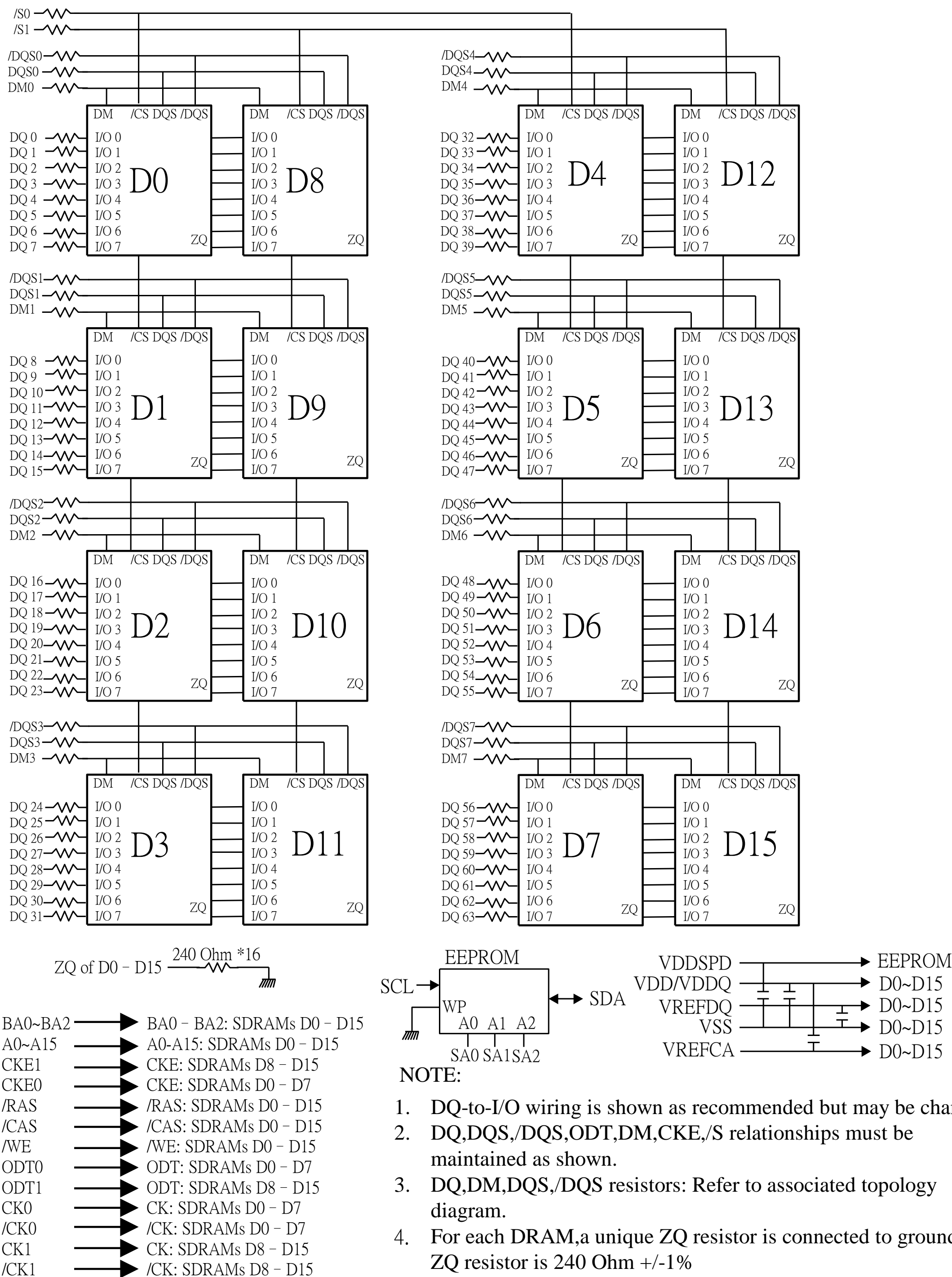


NOTE:

1. DQ-to-I/O wiring is shown as recommended but may be changed.
2. DQ,DQS,/DQS,ODT,DM,CKE,/S relationships must be maintained as shown.
3. DQ,DM,DQS,/DQS resistors: Refer to associated topology diagram.

This technical information is based on industry standard data and tests believed to be reliable. However, Transcend makes no warranties, either expressed or implied, as to its accuracy and assume no liability in connection with the use of this product. Transcend reserves the right to make changes in specifications at any time without prior notice.

8GB, 1Gx64 Module(2 Rank x8)



NOTE:

1. DQ-to-I/O wiring is shown as recommended but may be changed.
2. DQ,DQS,/DQS,ODT,DM,CKE,/S relationships must be maintained as shown.
3. DQ,DM,DQS,/DQS resistors: Refer to associated topology diagram.
4. For each DRAM,a unique ZQ resistor is connected to ground. The ZQ resistor is 240 Ohm +/-1%

This technical information is based on industry standard data and tests believed to be reliable. However, Transcend makes no warranties, either expressed or implied, as to its accuracy and assume no liability in connection with the use of this product. Transcend reserves the right to make changes in specifications at any time without prior notice.

Operating Temperature Condition

Parameter	Symbol	Rating	Unit	Note
Operating Temperature	TOPER	0 to 85	°C	1,2

Note:
1. Operating Temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JESD51-2 standard.
2. At 0 - 85°C, operation temperature range are the temperature which all DRAM specification will be supported.

Absolute Maximum DC Ratings

Parameter	Symbol	Value	Unit	Note
Voltage on VDD relative to Vss	VDD	-0.4 ~ 1.975	V	1
Voltage on VDDQ pin relative to Vss	VDDQ	-0.4 ~ 1.975	V	1
Voltage on any pin relative to Vss	VIN, VOUT	-0.4 ~ 1.975	V	1
Storage temperature	TSTG	-55~+100	°C	1,2

Note:
1. Stress greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Storage Temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JESD51-2 standard.

AC & DC Operating Conditions

Recommended DC operating conditions (SSTL –1.5)

Parameter	Symbol	Rating			Unit	Note
		Min	Typ.	Max		
Supply voltage	VDD	1.425	1.5	1.575	V	1, 2
Supply voltage for Output	VDDQ	1.425	1.5	1.575	V	1, 2
I/O Reference Voltage (DQ)	$VREF_{DQ}$(DC)	0.49*VDDQ	0.50*VDDQ	0.51*VDDQ	V	3
I/O Reference Voltage (CMD/ADD)	$VREF_{CA}$(DC)	0.49*VDDQ	0.50*VDDQ	0.51*VDDQ	V	3
AC Input Logic High	VIH(AC)	VREF+0.175	-	-	V	
AC Input Logic Low	VIL(AC)	-	-	VREF-0.175	V	
DC Input Logic High	VIH(DC)	VREF+0.1	-	VDD	V	
DC Input Logic Low	VIL(DC)	VSS	-	VREF-0.1	V	

Note: There is no specific device VDD supply voltage requirement for SSTL-1.5 compliance.
1. Under all conditions VDDQ must be less than or equal to VDD.
2. VDDQ tracks with VDD, AC parameters are measured with VDD and VDDQ tied together.
3. Peak to peak AC noise on VREF may not allow deviate from VREF(DC) by more than +/-1% VDD.

AC Input Level for Differential Signals

Parameter	Symbol	Value		Unit	Note
Differential Input Logical High	VIHdiff	+200	-	mV	
Differential Input Logical Low	VILdiff	-	-200		

IDD Specification parameters Definition

(IDD values are for full operating range of Voltage and Temperature)

4GB, 512Mx64 Module(1 Rank x8)

Parameter	Symbol	DDR3 1333 CL9	DDR3 1600 CL11	Unit
Operating One bank Active-Precharge current; tCK = tCK(IDD), tRC = tRC(IDD), tRAS = tRASmin(IDD); CKE is HIGH, /CS is HIGH between valid commands;Address bus inputs are SWITCHING; Data bus inputs are SWITCHING	IDD0	400	400	mA
Operating One bank Active-read-Precharge current; IOUT = 0mA; BL = 8, CL = CL(IDD), AL = 0; tCK = tCK(IDD), tRC = tRC (IDD), tRAS = tRASmin(IDD), tRCD = tRCD(IDD); CKE is HIGH, /CS is HIGH between valid commands; Address bus inputs are SWITCHING; Data pattern is same as IDD4W	IDD1	480	480	mA
Precharge power-down current; All banks idle; tCK = tCK(IDD); CKE is LOW; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING	IDD2P	176	176	mA
Precharge quiet standby current; All banks idle; tCK = tCK(IDD); CKE is HIGH, /CS is HIGH; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING	IDD2Q	240	240	mA
Precharge standby current; All banks idle; tCK = tCK(IDD); CKE is HIGH, /CS is HIGH; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING	IDD2N	240	240	mA
Active power - down current; All banks open; tCK = tCK(IDD); CKE is LOW; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING	IDD3P	200	200	mA
Active standby current; All banks open; tCK = tCK(IDD), tRAS = tRASmax(IDD), tRP = tRP(IDD); CKE is HIGH, /CS is HIGH between valid commands; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING	IDD3N	280	280	mA
Operating burst read current; All banks open, Continuous burst reads, IOUT = 0mA; BL = 4, CL = CL(IDD), AL = 0; tCK = tCK(IDD), tRAS = tRASmax(IDD), tRP = tRP(IDD); CKE is HIGH, /CS is HIGH between valid commands; Address bus inputs are SWITCHING; Data pattern is same as IDD4W	IDD4R	880	1000	mA
Operating burst write current; All banks open, Continuous burst writes; BL = 8, CL = CL(IDD), AL = 0; tCK = tCK(IDD), tRAS = tRASmax(IDD), tRP = tRP(IDD); CKE is HIGH, /CS is HIGH between valid commands; Address bus inputs are SWITCHING; Data bus inputs are SWITCHING IDD4R	IDD4W	920	1040	mA
Burst refresh current; tCK = tCK(IDD); Refresh command at every tRFC(IDD) interval; CKE is HIGH, /CS is HIGH between valid commands; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING	IDD5	1160	1160	mA
Self refresh current; CK and /CK at 0V; CKE ≒ 0.2V; Other control and address bus inputs are FLOATING; Data bus inputs are FLOATING	IDD6	160	160	mA
Operating bank interleave read current; All bank interleaving reads, IOUT = 0mA; BL = 8, CL = CL(IDD), AL = tRCD(IDD)-1*tCK(IDD); tCK = tCK(IDD), Trc = tRC(IDD), tRRD = tRRD(IDD), tRCD = 1*tCK(IDD); CKE is HIGH, CS is HIGH between valid commands;Address bus inputs are STABLE during DESELECTs; Data pattern is same as IDD4R;	IDD7	1400	1440	mA

Note: 1.Module IDD was calculated on the specific brand DRAM(3xnm) component IDD and can be differently measured according to DQ loading capacitor.

8GB, 1Gx64 Module(2 Rank x8)

Parameter	Symbol	DDR3 1333 CL9	DDR3 1600 CL11	Unit
Operating One bank Active-Precharge current; tCK = tCK(IDD), tRC = tRC(IDD), tRAS = tRASmin(IDD); CKE is HIGH, /CS is HIGH between valid commands;Address bus inputs are SWITCHING; Data bus inputs are SWITCHING	IDD0	640	680	mA
Operating One bank Active-read-Precharge current; IOUT = 0mA; BL = 8, CL = CL(IDD), AL = 0; tCK = tCK(IDD), tRC = tRC (IDD), tRAS = tRASmin(IDD), tRCD = tRCD(IDD); CKE is HIGH, /CS is HIGH between valid commands; Address bus inputs are SWITCHING; Data pattern is same as IDD4W	IDD1	720	760	mA
Precharge power-down current; All banks idle; tCK = tCK(IDD); CKE is LOW; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING	IDD2P	352	352	mA
Precharge quiet standby current; All banks idle; tCK = tCK(IDD); CKE is HIGH, /CS is HIGH; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING	IDD2Q	480	480	mA
Precharge standby current; All banks idle; tCK = tCK(IDD); CKE is HIGH, /CS is HIGH; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING	IDD2N	480	480	mA
Active power - down current; All banks open; tCK = tCK(IDD); CKE is LOW; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING	IDD3P	400	400	mA
Active standby current; All banks open; tCK = tCK(IDD), tRAS = tRASmax(IDD), tRP = tRP(IDD); CKE is HIGH, /CS is HIGH between valid commands; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING	IDD3N	560	560	mA
Operating burst read current; All banks open, Continuous burst reads, IOUT = 0mA; BL = 4, CL = CL(IDD), AL = 0; tCK = tCK(IDD), tRAS = tRASmax(IDD), tRP = tRP(IDD); CKE is HIGH, /CS is HIGH between valid commands; Address bus inputs are SWITCHING; Data pattern is same as IDD4W	IDD4R	1120	1280	mA
Operating burst write current; All banks open, Continuous burst writes; BL = 8, CL = CL(IDD), AL = 0; tCK = tCK(IDD), tRAS = tRASmax(IDD), tRP = tRP(IDD); CKE is HIGH, /CS is HIGH between valid commands; Address bus inputs are SWITCHING; Data bus inputs are SWITCHING IDD4R	IDD4W	1160	1320	mA
Burst refresh current; tCK = tCK(IDD); Refresh command at every tRFC(IDD) interval; CKE is HIGH, /CS is HIGH between valid commands; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING	IDD5	1400	1440	mA
Self refresh current; CK and /CK at 0V; CKE ≒ 0.2V; Other control and address bus inputs are FLOATING; Data bus inputs are FLOATING	IDD6	320	320	mA
Operating bank interleave read current; All bank interleaving reads, IOUT = 0mA; BL = 8, CL = CL(IDD), AL = tRCD(IDD)-1*tCK(IDD); tCK = tCK(IDD), Trc = tRC(IDD), tRRD = tRRD(IDD), tRCD = 1*tCK(IDD); CKE is HIGH, CS is HIGH between valid commands;Address bus inputs are STABLE during DESELECTs; Data pattern is same as IDD4R;	IDD7	1640	1720	mA

Note: 1.Module IDD was calculated on the specific brand DRAM(3X nm) component IDD and can be differently measured according to DQ loading capacitor.

Timing Parameters & Specifications

Speed		DDR3 1333		DDR3 1600		Unit
Parameter	Symbol	Min	Max	Min	Max	
Average Clock Period	tCK	1.5	<1.875	1.25	<1.5	ns
CK high-level width	tCH	0.47	0.53	0.47	0.53	tCK
CK low-level width	tCL	0.47	0.53	0.47	0.53	tCK
DQS, /DQS to DQ skew, per group, per access	tDQSQ	-	125	-	100	ps
DQ output hold time from DQS, /DQS	tQH	0.38	-	0.38	-	tCK
DQ low-impedance time from CK, /CK	tLZ(DQ)	-500	250	-450	225	ps
DQ high-impedance time from CK, /CK	tHZ(DQ)	-	250	-	225	ps
Data setup time to DQS, /DQS reference to Vih(ac)Vil(ac) levels	tDS	30	-	10	-	ps
Data hold time to DQS, /DQS reference to Vih(ac)Vil(ac) levels	tDH	65	-	45		ps
DQ and DM input pulse width for each input	tDIPW	400	-	360	-	ps
DQS, /DQS Read preamble	tRPRE	0.9	-	0.9	-	tCK
DQS, /DQS differential Read postamble	tRPST	0.3	-	0.3	-	tCK
DQS, /DQS Write preamble	tWPRE	0.9	-	0.9	-	tCK
DQS, /DQS Write postamble	tWPST	0.3	-	0.3	-	tCK
DQS, /DQS low-impedance time	tLZ(DQS)	-500	250	-450	225	ps
DQS, /DQS high-impedance time	tHZ(DQS)	-	250	-	225	ps
DQS, /DQS differential input low pulse width	tDQSL	0.45	0.55	0.45	0.55	tCK
DQS, /DQS differential input high pulse width	tDQSH	0.45	0.55	0.45	0.55	tCK
DQS, /DQS rising edge to CK, /CK rising edge	tDQSS	-0.25	+0.25	-0.27	+0.27	tCK
DQS, /DQS falling edge setup time to CK, /CK rising edge	tDSS	0.2	-	0.18	-	tCK
DQS, /DQS falling edge hold time to CK, /CK rising edge	tDSH	0.2	-	0.18	-	tCK
Delay from start of Internal write transaction to Internal read command	tWTR	Max (4tck, 7.5ns)	-	Max (4tck, 7.5ns)	-	
Write recovery time	tWR	15	-	15	-	ns
Mode register set command cycle time	tMRD	4	-	4	-	tCK
/CAS to /CAS command delay	tCCD	4	-	4	-	nCK
Auto precharge write recovery + precharge time	tDAL	tWR+tRP/tck		tWR+tRP/tck		nCK
Active to active command period for 1KB page size	tRRD	Max (4tck, 6ns)	-	Max (4tck, 6ns)	-	ns

Speed		DDR3 1333		DDR3 1600		Unit
Parameter	Symbol	Min	Max	Min	Max	
Active to active command period for 2KB page size	tRRD	Max (4tck, 7.5ns)	-	Max (4tck, 7.5ns)	-	
Four Activate Window for 1KB page size	tFAW	30	-	30	-	ns
Four Activate Window for 2KB page size products	tFAW	45	-	40	-	ns
Power-up and RESET calibration time	tZQinitl	512	-	512	-	tCK
Normal operation Full calibration time	tZQoper	256	-	256	-	tCK
Normal operation short calibration time	tZQcs	64	-	64	-	tCK
Exit self refresh to commands not requiring a locked DLL	tXS	Max (5tCK, tRFC+10)	-	Max (5tCK, tRFC+10ns)	-	
Exit self refresh to commands requiring a locked DLL	tXSDLL	tDLL(min)	-	tDLL(min)	-	tCK
Internal read to precharge command delay	tRTP	Max (4tCK, 7.5ns)	-	Max (4tck, 7.5ns)	-	
Minimum CKE low width for Self refresh entry to exit timing	tCKESR	tCK(min)+1tCK	-	tCK(min)+1tCK	-	
Exit power down with DLL to any valid command: Exit Precharge Power Down with DLL	tXP	Max (3tCK, 6ns)	-	Max (3tCK, 6ns)	-	
CKE minimum pulse width (high and low pulse width)	tCKE	Max (3tCK,5.625ns)		Max (3tCK, 5ns)		
Asynchronous RTT turn-on delay (Power-Down mode)	tAONPD	2	8.5	2	8.5	ns
Asynchronous RTT turn-off delay (Power-Down mode)	tAOFPD	2	8.5	2	8.5	ns
ODT turn-on	tAON	-250	250	-225	225	ps
ODT turn-off	tAOF	0.3	0.7	0.3	0.7	tCK

SERIAL PRESENCE DETECT SPECIFICATION

TS512MLK64V3H Serial Presence Detect

Byte No.	Function Described	Standard Specification	Vendor Part
0	Number of SPD Bytes written / SPD device size / CRC coverage during module production	CRC:0-116Byte SPD Byte use: 176Byte SPD Byte total: 256Byte	92
1	SPD Revision	Version 1.0	10
2	Key Byte / DRAM Device Type	DDR3 SDRAM	0B
3	Key Byte / Module Type	UDIMM	02
4	SDRAM Density and Banks	4GB 8banks	04
5	SDRAM Addressing	ROW:16, Column:10	21
6	Reserved	1.5V	00
7	Module Organization	1Rank / x8	01
8	Module Memory Bus Width	Non ECC, 64bit	03
9	Fine Timebase Dividend and Divisor	2.5ps	52
10	Medium Timebase Dividend	0.125ns	01
11	Medium Timebase Divisor	0.125ns	08
12	SDRAM Minimum Cycle Time (tCKmin)	1.5ns	0C
13	Reserved	-	00
14	CAS Latencies Supported, Least Significant Byte	6, 7, 8, 9	3C
15	CAS Latencies Supported, Most Significant Byte	-	00
16	Minimum CAS Latency Time (tAAmin)	13.125ns	69
17	Minimum Write Recovery Time (tWRmin)	15ns	78
18	Minimum /RAS to /CAS Delay Time (tRCDmin)	13.125ns	69
19	Minimum Row Active to Row Active Delay Time (tRRDmin)	6ns	30
20	Minimum Row Precharge Time (tRPmin)	13.125ns	69
21	Upper Nibble for tRAS and tRC	-	11
22	Minmum Active to Precharge Time (tRASmin)	36ns	20
23	Minmum Active to Active/Refresh Time (tRCmin)	49.125ns	89
24	Minmum Refresh Recovery Time (tRFCmin), Least Significant Byte	260ns	20
25	Minmum Refresh Recovery Time (tRFCmin), Most Significant Byte	260ns	08
26	Minmum Internal Write to Read Command Delay Time (tWTmin)	7.5ns	3C
27	Minimum Internal Read to Precharge Command Delay Time (tRTPmin)	7.5ns	3C
28	Upper Nibble for tFAW	30ns	00
29	Minmum Four Active Window Delay Time (tFAWmin)	30ns	F0
30	SDRAM Optional Features	DLL off Mode, RZQ/6, RZQ/7	83
31	SDRAM Thermal and Refresh Options	No ODTs, No ASR	01
32-59	Reserved	-	00
60	Module Nominal Height	30mm	0F
61	Module Max Thickness	Planar Double Sides	01

62	Reference Raw Card Used	R/C A	00
63	Address Mapping from Edge Connector to DRAM	Mirrored	00
64-116	Reserved	-	00
117	Module Manufacturer ID Code, Least Significant Byte	Transcend	01
118	Module Manufacturer ID Code, Most Significant Byte	Transcend	4F
119	Module Manufacturing Location	Taipei	54
120-121	Module Manufacturing Date	-	00
122-125	Module Serial Number	-	00
126-127	Cyclical Redundancy Code	-	19, CE
128-145	Module Part Number	TS512MLK64V3H	54 53 35 31 32 4D 4C 4B 36 34 56 33 48 20 20 20 20 20
146-147	Revision Code	-	00
148-149	DRAM Manufacturer ID Code	By Manufacturer	Variable
150-175	Manufacturer Specific Data	By Manufacturer	Variable
176-255	Open for customer use	Undefined	00

TS512MLK64V6H Serial Presence Detect			
Byte No.	**Function Described**	**Standard Specification**	**Vendor Part**
0	Number of SPD Bytes written / SPD device size / CRC coverage during module production	CRC:0-116Byte SPD Byte use: 176Byte SPD Byte total: 256Byte	92
1	SPD Revision	Version 1.0	10
2	Key Byte / DRAM Device Type	DDR3 SDRAM	0B
3	Key Byte / Module Type	UDIMM	02
4	SDRAM Density and Banks	4GB 8banks	04
5	SDRAM Addressing	ROW:16, Column:10	21
6	Reserved	1.5V	00
7	Module Organization	1Rank / x8	01
8	Module Memory Bus Width	Non ECC, 64bit	03
9	Fine Timebase Dividend and Divisor	2.5ps	52
10	Medium Timebase Dividend	0.125ns	01
11	Medium Timebase Divisor	0.125ns	08
12	SDRAM Minimum Cycle Time (tCKmin)	1.25ns	0A
13	Reserved	-	00
14	CAS Latencies Supported, Least Significant Byte	6, 7, 8, 9,10,11	FC
15	CAS Latencies Supported, Most Significant Byte	6, 7, 8, 9,10,11	00
16	Minimum CAS Latency Time (tAAmin)	13.125ns	69
17	Minimum Write Recovery Time (tWRmin)	15ns	78
18	Minimum /RAS to /CAS Delay Time (tRCDmin)	13.125ns	69
19	Minimum Row Active to Row Active Delay Time (tRRDmin)	6ns	30
20	Minimum Row Precharge Time (tRPmin)	13.125ns	69
21	Upper Nibble for tRAS and tRC	-	11
22	Minmum Active to Precharge Time (tRASmin)	35ns	18
23	Minmum Active to Active/Refresh Time (tRCmin)	48.125ns	81
24	Minmum Refresh Recovery Time (tRFCmin), Least Significant Byte	260ns	20
25	Minmum Refresh Recovery Time (tRFCmin), Most Significant Byte	260ns	08
26	Minmum Internal Write to Read Command Delay Time (tWTmin)	7.5ns	3C
27	Minimum Internal Read to Precharge Command Delay Time (tRTPmin)	7.5ns	3C
28	Upper Nibble for tFAW	30ns	00
29	Minmum Four Active Window Delay Time (tFAWmin)	30ns	F0
30	SDRAM Optional Features	DLL off Mode, RZQ/6, RZQ/7	83
31	SDRAM Thermal and Refresh Options	No ODTs, No ASR	01
32-59	Reserved	-	00
60	Module Nominal Height	30mm	0F
61	Module Max Thickness	Planar Double Sides	01
62	Reference Raw Card Used	R/C A	00

<table>
<tr><td>63</td><td>Address Mapping from Edge Connector to DRAM</td><td>Mirrored</td><td colspan="6">00</td></tr>
<tr><td>64-116</td><td>Reserved</td><td>-</td><td colspan="6">00</td></tr>
<tr><td>117</td><td>Module Manufacturer ID Code, Least Significant Byte</td><td>Transcend</td><td colspan="6">01</td></tr>
<tr><td>118</td><td>Module Manufacturer ID Code, Most Significant Byte</td><td>Transcend</td><td colspan="6">4F</td></tr>
<tr><td>119</td><td>Module Manufacturing Location</td><td>Taipei</td><td colspan="6">54</td></tr>
<tr><td>120-121</td><td>Module Manufacturing Date</td><td>-</td><td colspan="6">00</td></tr>
<tr><td>122-125</td><td>Module Serial Number</td><td>-</td><td colspan="6">00</td></tr>
<tr><td>126-127</td><td>Cyclical Redundancy Code</td><td>-</td><td colspan="6">2D, 11</td></tr>
<tr><td rowspan="3">128-145</td><td rowspan="3">Module Part Number</td><td rowspan="3">TS512MLK64V6H</td><td>54</td><td>53</td><td>35</td><td>31</td><td>32</td><td>4D</td></tr>
<tr><td>4C</td><td>4B</td><td>36</td><td>34</td><td>56</td><td>36</td></tr>
<tr><td>48</td><td>20</td><td>20</td><td>20</td><td>20</td><td>20</td></tr>
<tr><td>146-147</td><td>Revision Code</td><td>-</td><td colspan="6">00</td></tr>
<tr><td>148-149</td><td>DRAM Manufacturer ID Code</td><td>By Manufacturer</td><td colspan="6">Variable</td></tr>
<tr><td>150-175</td><td>Manufacturer Specific Data</td><td>By Manufacturer</td><td colspan="6">Variable</td></tr>
<tr><td>176-255</td><td>Open for customer use</td><td>Undefined</td><td colspan="6">00</td></tr>
</table>

TS1GLK64V3H Serial Presence Detect			
Byte No.	**Function Described**	**Standard Specification**	**Vendor Part**
0	Number of SPD Bytes written / SPD device size / CRC coverage	CRC:0-116Byte SPD Byte total: 256Byte SPD Byte use: 176Byte	92
1	SPD Revision	Version 1.0	10
2	Key Byte / DRAM Device Type	DDR3 SDRAM	0B
3	Key Byte / Module Type	UDIMM	02
4	SDRAM Density and Banks	4Gb 8banks	04
5	SDRAM Addressing	ROW:16, Column:10	21
6	Reserved	--	00
7	Module Organization	2Rank / x8	09
8	Module Memory Bus Width	Non ECC, 64bit	03
9	Fine Timebase Dividend and Divisor	2.5ps	52
10	Medium Timebase Dividend	0.125ns	01
11	Medium Timebase Divisor	0.125ns	08
12	SDRAM Minimum Cycle Time (tCKmin)	1. 5ns	0C
13	Reserved	--	00
14	CAS Latencies Supported, Low Byte	6, 7, 8, 9	3C
15	CAS Latencies Supported, High Byte	--	00
16	Minimum CAS Latency Time (tAAmin)	13.125ns	69
17	Minimum Write Recovery Time (tWRmin)	15ns	78
18	Minimum /RAS to /CAS Delay Time (tRCDmin)	13.125ns	69
19	Minimum Row Active to Row Active Delay Time (tRRDmin)	6ns	30
20	Minimum Row Precharge Time (tRPmin)	13.125ns	69
21	Upper Nibble for tRAS and tRC	-	11
22	Minmum Active to Precharge Time (tRASmin)	36ns	20
23	Minmum Active to Active/Refresh Time (tRCmin)	49.125ns	89
24	Minmum Refresh Recovery Time (tRFCmin), Least Significant Byte	260ns	20
25	Minmum Refresh Recovery Time (tRFCmin), Most Significant Byte	260ns	08
26	Minmum Internal Write to Read Command Delay Time (tWTmin)	7.5ns	3C
27	Minimum Internal Read to Precharge Command Delay Time (tRTPmin)	7.5ns	3C
28	Upper Nibble for tFAW	30ns	00
29	Minmum Four Active Window Delay Time (tFAWmin)	30ns	F0
30	SDRAM Optional Features	DLL off Mode, RZQ/6, RZQ/7	83
31	SDRAM Thermal and Refresh Options	No ODTs, No ASR	01
32-59	Reserved	--	00
60	Module Nominal Height	30mm	0F
61	Module Max Thickness	Planar Double Sides	11
62	Reference Raw Card Used	R/C B	01

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<tr><td>63</td><td>Address Mapping from Edge Connector to DRAM</td><td>Mirrored</td><td colspan="6">01</td></tr>
<tr><td>64-116</td><td>Reserved</td><td>--</td><td colspan="6">00</td></tr>
<tr><td>117</td><td>Module Manufacturer ID Code, Least Significant Byte</td><td>Transcend</td><td colspan="6">01</td></tr>
<tr><td>118</td><td>Module Manufacturer ID Code, Most Significant Byte</td><td>Transcend</td><td colspan="6">4F</td></tr>
<tr><td>119</td><td>Module Manufacturing Location</td><td>Taipei</td><td colspan="6">54</td></tr>
<tr><td>120-121</td><td>Module Manufacturing Date</td><td>--</td><td colspan="6">00</td></tr>
<tr><td>122-125</td><td>Module Serial Number</td><td>--</td><td colspan="6">00</td></tr>
<tr><td>126-127</td><td>Cyclical Redundancy Code</td><td>--</td><td colspan="6">64, 07</td></tr>
<tr><td rowspan="3">128-145</td><td rowspan="3">Module Part Number</td><td rowspan="3">TS1GLK64V3H</td><td>54</td><td>53</td><td>31</td><td>47</td><td>4C</td><td>4B</td></tr>
<tr><td>36</td><td>34</td><td>56</td><td>33</td><td>48</td><td>20</td></tr>
<tr><td>20</td><td>20</td><td>20</td><td>20</td><td>20</td><td>20</td></tr>
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<tr><td>148-149</td><td>DRAM Manufacturer ID Code</td><td>By Manufacturer</td><td colspan="6">Variable</td></tr>
<tr><td>150-175</td><td>Manufacturer Specific Data</td><td>By Manufacturer</td><td colspan="6">Variable</td></tr>
<tr><td>176-255</td><td>Open for customer use</td><td>Undefined</td><td colspan="6">00</td></tr>
</table>

TS1GLK64V6H Serial Presence Detect			
Byte No.	**Function Described**	**Standard Specification**	**Vendor Part**
0	Number of SPD Bytes written / SPD device size / CRC coverage during module production	CRC:0-116Byte SPD Byte use: 176Byte SPD Byte total: 256Byte	92
1	SPD Revision	Version 1.0	10
2	Key Byte / DRAM Device Type	DDR3 SDRAM	0B
3	Key Byte / Module Type	UDIMM	02
4	SDRAM Density and Banks	4GB 8banks	04
5	SDRAM Addressing	ROW:16, Column:10	21
6	Reserved	-	00
7	Module Organization	2Rank / x8	09
8	Module Memory Bus Width	Non ECC, 64bit	03
9	Fine Timebase Dividend and Divisor	2.5ps	52
10	Medium Timebase Dividend	0.125ns	01
11	Medium Timebase Divisor	0.125ns	08
12	SDRAM Minimum Cycle Time (tCKmin)	1.25ns	0A
13	Reserved	-	00
14	CAS Latencies Supported, Least Significant Byte	6, 7, 8, 9,10,11	FC
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23	Minmum Active to Active/Refresh Time (tRCmin)	48.125ns	81
24	Minmum Refresh Recovery Time (tRFCmin), Least Significant Byte	260ns	20
25	Minmum Refresh Recovery Time (tRFCmin), Most Significant Byte	260ns	08
26	Minmum Internal Write to Read Command Delay Time (tWTmin)	7.5ns	3C
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28	Upper Nibble for tFAW	30ns	00
29	Minmum Four Active Window Delay Time (tFAWmin)	30ns	F0
30	SDRAM Optional Features	DLL off Mode, RZQ/6, RZQ/7	83
31	SDRAM Thermal and Refresh Options	No ODTs, No ASR	01
32-59	Reserved	-	00
60	Module Nominal Height	30mm	0F
61	Module Max Thickness	Planar Double Sides	11
62	Reference Raw Card Used	R/C B	01

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<tr><td>126-127</td><td>Cyclical Redundancy Code</td><td>-</td><td colspan="6">50, D8</td></tr>
<tr><td rowspan="3">128-145</td><td rowspan="3">Module Part Number</td><td rowspan="3">TS1GLK64V6H</td><td>54</td><td>53</td><td>31</td><td>47</td><td>4C</td><td>4B</td></tr>
<tr><td>36</td><td>34</td><td>56</td><td>36</td><td>48</td><td>20</td></tr>
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Revision History

Rev	Draft/Changes	Date
1.0	New	2012/2/22
1.1	tRFC change to 260ns from 300ns	2012/3/18