MODEL
372XXC/373XXC
VECTOR NETWORK ANALYZER

MAINTENANCE MANUAL

Anritsu

490 JARVIS DRIVE I MORGAN HILL, CA 95037-2809

P/N: 10410-00228
REVISION: D
PRINTED: AUGUST 2004

WARRANTY

The Anritsu product(s) listed on the title page is (are) warranted against defects in materials and workmanship for three years from the date of shipment.
Anritsu's obligation covers repairing or replacing products which prove to be defective during the warranty period. Buyers shall prepay transportation charges for equipment returned to Anritsu for warranty repairs. Obligation is limited to the original purchaser. Anritsu is not liable for consequential damages.

LIMITATION OF WARRANTY

The foregoing warranty does not apply to Anritsu connectors that have failed due to normal wear. Also, the warranty does not apply to defects resulting from improper or inadequate maintenance by the Buyer, unauthorized modification or misuse, or operation outside of the environmental specifications of the product. No other warranty is expressed or implied, and the remedies provided herein are the Buyer's sole and exclusive remedies.

TRADEMARK ACKNOWLEDGEMENTS

V Connector and K Connector are registered trademarks of Anritsu Company.
MS-DOS is a registered trademark of Microsoft Corporation.
Acrobat and Acrobat Reader are registered trademarks of Adobe Systems Incorporated.

NOTICE

Anritsu Company has prepared this manual for use by Anritsu Company personnel and customers as a guide for the proper installation, operation and maintenance of Anritsu Company equipment and computer programs. The drawings, specifications, and information contained herein are the property of Anritsu Company, and any unauthorized use or disclosure of these drawings, specifications, and information is prohibited; they shall not be reproduced, copied, or used in whole or in part

DECLARATION OF CONFORMITY

Manufacturer's Name: ANRITSU COMPANY

Manufacturer's Address: Microwave Measurements Division
490 Jarvis Drive
Morgan Hill, CA 95037-2809
USA

declares that the product specified below:

Product Name: Vector Network Analyzer

Model Number: 371XXA, 372XXA, 373XXA, 371XXB, 372XXB, 373XXB
371XXC, 3722XXC, 373XXC

conforms to the requirement of:

EMC Directive 89/336/EEC as amended by Council Directive 92/31/EEC & 93/68/EEC
Low Voltage Directive 73/23/EEC as amended by Council directive 93/68/EEC

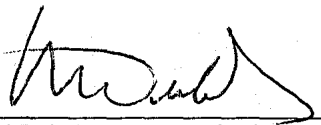
Electromagnetic Interference:

Emissions:
CISPR 11:1990/EN55011: 1991 Group 1 Class A
EN 61000-3-2:1995 Class A
EN 61000-3-3:1995 Class A

Immunity:
EN 61000-4-2:1995/EN50082-1: 1997 - 4kV CD, 8kV AD
EN 61000-4-3:1997/EN50082-1: 1997 - 3V/m
ENV 50204/EN50082-1: 1997 – 3V/m
EN 61000-4-4:1995/EN50082-1: 1997 - 0.5kV SL, 1kV PL
EN 61000-4-5:1995/EN50082-1: 1997 - 1kV L-L, 2kV L-E
EN 61000-4-6:1994/EN61326: 1998 – 3V
EN 61000-4-8:1994/EN61326: 1998 – 3A/m
EN 61000-4-11:1994/EN61326: 1998 – 100% @ 20msec

Electrical Safety Requirement:

Product Safety: EN 61010-1:2001



Marcel Dubois, Corporate Quality Director

Morgan Hill, CA

22 DEC 2003
Date

European Contact: For Anritsu product EMC & LVD information, contact Anritsu LTD, Rutherford Close, Stevenage Herts, SG1 2EF UK, (FAX 44-1438-740202)

Table of Contents, Narrative

Table of Contents

Table of Contents (Continued)

Chapter 3 Theory of Operation

Chapter 4 Operational Performance Tests

Table of Contents (Continued)

Chapter 5 System Performance Verification

Chapter 6 Adjustments

Chapter 7 Troubleshooting

Chapter 8 Removal and Replacement Procedures

Appendix A Error Messages

Appendix B Connector Care and Handling

Table of Contents (Continued)

Chapter 1
General Information

Table of Contents

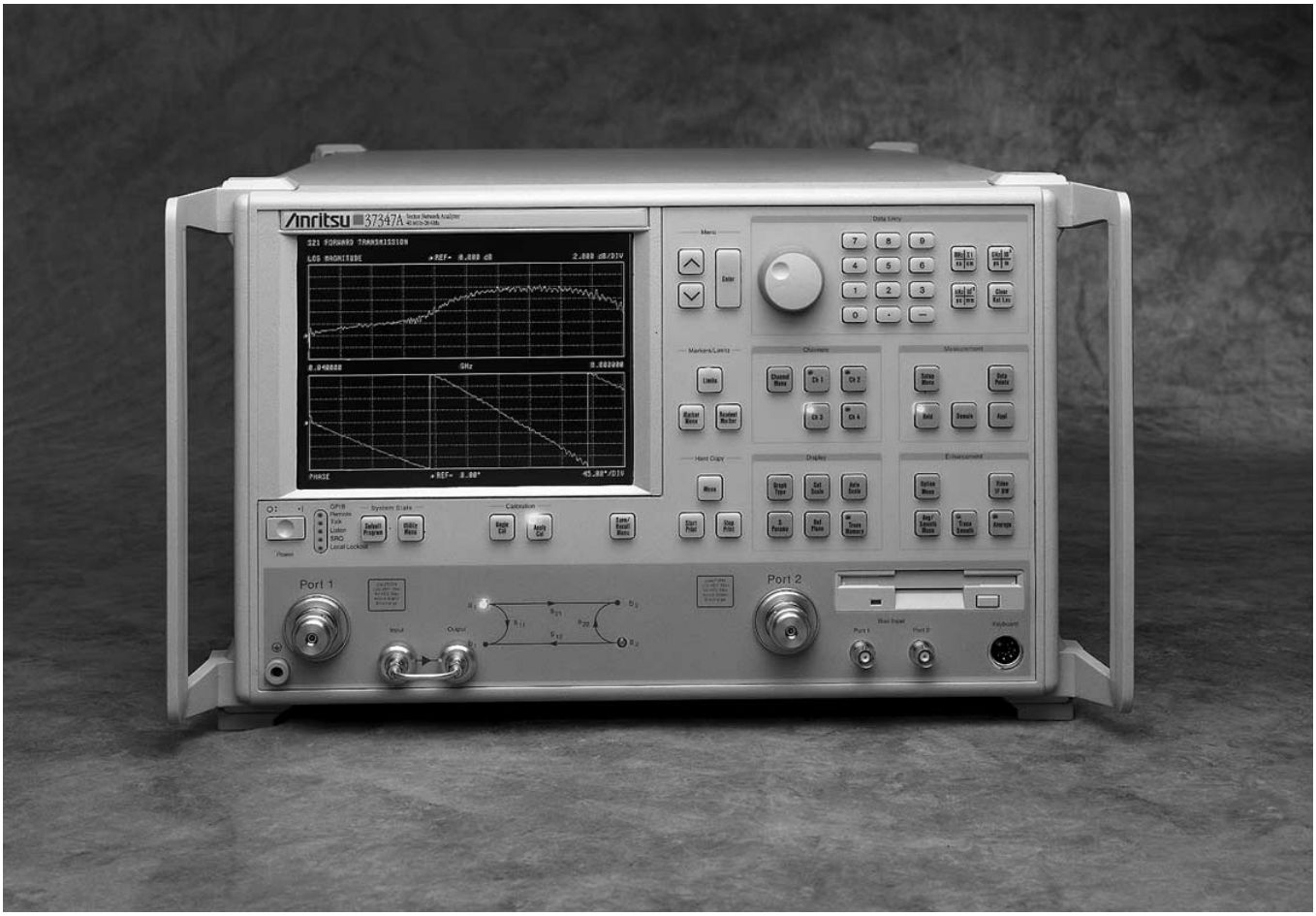


Figure 1-1. *Series 372XXC/373XXC Vector Network Analyzer System*

Chapter 1
General Information

1-1 SCOPE OF MANUAL

This manual provides general service and preventive maintenance information for the Anritsu 372XXC/373XXC models of Vector Network Analyzer (VNA) systems. It contains procedures for:

- Testing the instrument for proper operation.
- Verifying measurement accuracy and traceability to National Institute of Standards and Technology (NIST).
- Troubleshooting a failed instrument to the exchange subassembly level or the subsystem requiring adjustment.
- Adjusting instrument internal sub-systems.
- Locating and replacing failed parts.

Throughout this manual, the terms “37XXXC” and “VNA” will be used interchangeably to refer to all Models of 372XXC and 373XXC VNA, unless otherwise noted.

1-2 INTRODUCTION

This chapter provides a general description of VNA systems, system serial numbers, frequency ranges, and related manuals. It also includes service strategy, available service facilities, and static-sensitive component handling precautions, and a list of recommended test equipment.

1-3 IDENTIFICATION NUMBER

All Anritsu instruments are assigned a six-digit ID number, such as “401001”. This number appears on a decal affixed to the rear panel. Please use this identification number during any correspondence with Anritsu Customer Service about this instrument.

1-4 ONLINE MANUAL

This manual is available on CD ROM as an Adobe Acrobat™ (*.pdf) file. The file can be viewed using Acrobat Reader™, a free program that is also available on the CD ROM. This file is “linked” such that the viewer can choose a topic to view from the displayed “bookmark” list and “jump” to the manual page on which the topic resides. The text can also be word-searched. A copy of this CD ROM, part number 10920-00034, can be ordered from Anritsu customer service.

1-5 SYSTEM DESCRIPTION

The 37XXXC Analyzers are microprocessor controlled Vector Network Analyzers. Each is a single-instrument system that contains a built-in signal source, a test set, and an analyzer subsystem. A typical model (37369C) is shown in Figure 1-1. These analyzers are produced in five models that cover a range of from 22.5 MHz to 65 GHz. The table below lists the frequencies for each model:

37XXXC Models and Frequency Ranges

Model	Freq Range	Model	Freq Range
37217C	22.5 MHz to 8.6 GHz	37317C	22.5 MHz to 8.6 GHz
37225C	40.0 MHz to 13.5 GHz	37325C	40.0 MHz to 13.5 GHz
37247C	40.0 MHz to 20.0 GHz	37347C	40.0 MHz to 20.0 GHz
37269C	40.0 MHz to 40.0 GHz	37369C	40.0 MHz to 40.0 GHz
37277C	40.0 MHz to 50.0 GHz	37377C	40.0 MHz to 50.0 GHz
37297C	40.0 MHz to 65.0 GHz	37397C	40.0 MHz to 65.0 GHz

1-6 RELATED MANUALS

The 37XXXC Vector Network Analyzer Operation Manual (10410-00226) describes the front panel operation for all 37XXXC models. It also contains general information, specifications, and Performance Verification procedures for all models.

The 37XXXC Series Vector Network Analyzer Programming Manual (10410-00227) describes all 37XXXC GPIB commands and provides programming information for operation of the VNA remotely via the IEEE-488 General Purpose Interface Bus. Included at the rear of that manual is the 37XXXC Series Vector Network Analyzer GPIB Quick Reference Guide (10410-00229).

1-7 STANDARD OPTIONS

The standard VNA options and their respective Upgrade Kit part numbers are:

Option*	Description	Upgrade Kit
Opt 1	Rack Mount with slides	ND39486
Opt 1A	Rack Mount	ND40916
Opt 2A	Time Domain (Microwave Units)	ND39477
Opt 2B	Time Domain (RF Units)	ND40914
Opt 10A	High Stability Ovenized Time Base and 1 Hz Resolution	ND45045
Opt 11	Rear panel access to the a1 Reference line, for 37200C only	Contact Factory
Opt 12	Rear Panel IF Inputs for interface with Anritsu 374X millimeter wave modules	Contact Factory

*All options can be installed at Anritsu Service Centers

1-8 SERVICE STRATEGY

This section provides an overview of the VNA service strategy and available service facilities. It also provides references to the information in various locations in this manual needed to accomplish the required service functions.

Appendices - Refer to the Appendices at the rear of this manual for detailed descriptions of the following:

- Diagnostics Menus and GPIB Commands.
- Error Messages.
- System Block Diagrams.
- Parts Locator Diagrams.

Functional Assembly Level Troubleshooting

The VNA modular design, extensive built-in diagnostics, and automated service tools are designed to support fast exchange of functional assembly level repairs.

Failed assemblies are not field repairable. Once an assembly is found to be faulty, it should be returned to an authorized Anritsu Service Center for exchange. Refer to the description of the Exchange Assembly Program in Chapter 2, Replaceable Parts.

The procedures for troubleshooting a failed VNA are described in Chapter 7, Troubleshooting.

Internal Hardware Adjustments and Calibrations

There are five automated internal hardware field calibrations. Two of them are used to characterize the VNA frequency and power generation sub-systems. These calibrations insure fast, consistent phase lock of system frequencies and proper compensation, leveling, and flatness of system power at the front panel test ports.

To conduct these calibrations, you need only connect the appropriate test equipment (counter or power meter) to the VNA and initiate the calibration. The VNA will control itself and the externally connected test equipment to perform measurements and store calibration constants in its internal battery backed RAM (BBRAM).

The procedures for adjusting the VNA are described in this manual in Chapter 6, Adjustments.

Internal Service Log

The VNA continuously monitors itself for proper operation. Should a failure occur, it notifies the user via a failure message on the display screen. (In remote-only operation, it also sets the GPIB Status Byte, if enabled.) It also writes the error message along with some data pertinent to the failure to an internal service log stored in battery backed memory.

The service log can be checked at any time to view (without erasing) all error messages that were written into it. It is capable of storing more than 30 pages of service messages and data. The VNA will automatically remove the oldest errors first to make room for new errors, if necessary. To check the contents of the service log, use the procedure described in Chapter 4, Operational Performance Tests.

> ***NOTE***
>
> A printed or disk file copy of the Service Log (with the failure in question) must be made available to Anritsu when exchanging a failed assembly, or when requesting service support. Refer to Chapter 2, Replaceable Parts, for further information.

System Test/Certification

Quick operational checkout of the system may be accomplished by the system user or for incoming inspection purposes using the "Operational Checkout" chapter in the 37XXXC Operation Manual. Those procedures are useful in quickly verifying that the instrument's primary measurement functions are operational and stable.

Full operational testing of the system is detailed in Chapter 4, Operational Performance Tests (or Appendix F for ME7808A systems). These tests should be performed annually, or more often depending on system use.

Verification of the system's measurement accuracy and other key performance parameters may be done using the procedures in Chapter 5, System Performance Verification (or Appendix D for ME7808A systems). This should be performed annually, or more often depending on system use.

Servicing Specially Modified Instruments

Instruments with customer requested special modifications performed by Anritsu will have an identifying Specials Modification number printed on the rear panel. This number will be preceded with the letters SM, that is, SM1234 is special modification number 1234.

Special instruments may have service requirements different from those specified in this manual. Contact your local Service Center if you need more information when servicing such instruments.

1-9 SERVICE SUPPORT

The following sections briefly describe the various service support services and aids available to you to help you maintain your VNA.

Technical Support

Technical service support is available by contacting any Anritsu Worldwide Service Center (refer to Table 2-1), or service support may be obtained directly from the factory by contacting:

Anritsu Company
ATTN: Customer Service
490 Jarvis Drive
Morgan Hill, CA 95037-2809

Telephone: (408)-778-2000
FAX: (408)-778-0239

If servicing or repairing your own system and you need technical support, you will need to FAX or email a printout of the items listed below to the Anritsu Customer Support Engineer:

- Measurement data in question
- Operational test results
- System State (from UTILITY menu)
- Service Log (from DIAGNOSTICS menu)

Field Service Kits The field service kit listed below is available through your local Anritsu Sales or Service Center:

ND37200A-2, Field Service Kit

This kit provides for automated field test and performance verification of the 372XXB and 373XXA VNA, only. It is packaged in a hardened rolling case that also has space for two, user supplied, verification and calibration kits and other accessories. The ND37200A-2, Field Service Kit is comprised of all major subassemblies of all models 40 GHz and below high-end frequency.

ND54996, Field Service Kit

This kit has additional parts to support most C models (it excludes 50 and 65 GHz units)

ND53269, Field Service Kit

This kit provides for automated field test and performance verification of the VNA 50 and 65 GHz models. It supplements kit ND37200A-2.

NDME7808A-1, Field Service Kit

This kit supports the model 3738A and Option 12 used in the ME7808A Broadband system.

Service Software The service software listed below is contained on the diskette located at the rear of this manual:

Anritsu 37XXX Test Software (2300-178).

This software contains a series of automated tests designed to insure the VNA signal paths are functioning properly and capable of supporting stable calibrations and measurements. See the “Operational Performance Tests” chapter for details.

Anritsu 37XXX Performance Verification Software (2300-496 or 2300-237).

This software is used to verify the VNA’s published measurement accuracy and traceability to the U.S. National Institute of Standards and Technology (NIST). See the “System Performance Verification” chapter for details.

> ***NOTE***
> Use of 2300-496 is required to verification of broadband systems using W1 coaxial connectors

Verification Kits The Anritsu Verification Kits listed below are used in conjunction with the 37XXX Performance Verification Software.

N Verification Kit (Model 3663)

Contains precision N Connector components with characteristics that are traceable to the NIST.
Use for Models 37317C and below with Option 7N and 7 NF.

3.5 mm Verification Kit (Model 3666)

Contains precision 3.5 mm Connector components with characteristics that are traceable to the NIST.
Use for Models 37347C and below with Option 7A.

GPC-7 Verification Kit (Model 3667)

Contains precision GPC-7 Connector components with characteristics that are traceable to the NIST.
Use for Models 37317C and below with Option 7A.

K Verification Kit (Model 3668)

Contains precision K Connector components that are traceable to the NIST.

V Verification Kit (Model 3669B)

Contains precision V Connector components that are traceable to the NIST.

W1 Calibration/Verification Kit (Model 3656)

Contains calibration and verification W1 connector components for use with the ME7808A Broadband System (refer to Appendix D).

Test Fixtures/Aids The test fixtures and test aids listed below are available through your local Anritsu Sales or Service Center:

Rear Panel Printer Port Test Fixture (B39553).

This test fixture is used to check out digital printer interface circuits on the rear panel assembly.

GPIB Cable (2100-2).

This cable is used to check out digital GPIB interface circuits on the rear panel assembly.

Failed Assembly Exchange Program

The exchange program allows a customer to quickly exchange a failed subassembly for a factory refurbished, fully system-tested unit that is under warranty. This results in significant time and price savings as compared with ordering a new assembly. Refer to Chapter 2, Replaceable Parts, for a complete list of exchangeable assemblies for all series 37XXXC models.

> **NOTE**
> When sending a failed assembly to the factory for exchange, a copy of the Service Log *must always* accompany the failed assembly. Refer to Chapter 2, Replaceable Parts, for further information.

1-10 PERFORMANCE SPECIFICATIONS

The performance specifications for all Series 37XXXC models are contained in the technical data sheet located in Appendix C, Performance Specifications.

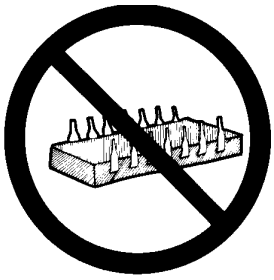
1-11 SERVICE CENTERS

Anritsu Company offers a full range of repair and calibration services at fully staffed and equipped service centers throughout the world. Table 2-1, located on page 2-2, lists all Anritsu services centers.

1-12 STATIC SENSITIVE COMPONENT HANDLING PROCEDURES

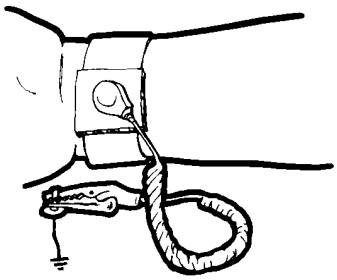
The VNA contains components that can be damaged by static electricity. Figure 1-2 illustrates the precautions that should be followed when handling static-sensitive subassemblies and components. If followed, these precautions will minimize the possibilities of static-shock damage to these items.

1. Do not touch exposed contacts on any static sensitive component.



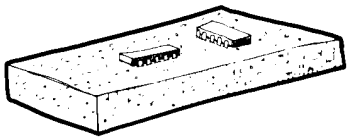
2. Do not slide static sensitive component across any surface.

3. Do not handle static sensitive components in areas where the floor or work surface covering is capable of generating a static charge.

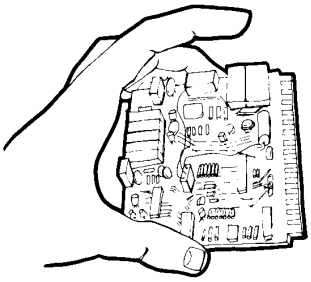


4. Wear a static-discharge wristband when working with static sensitive components.

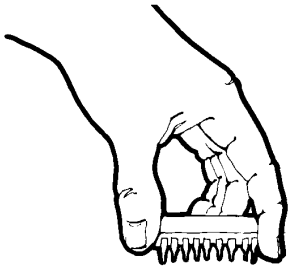
5. Label all static sensitive devices.



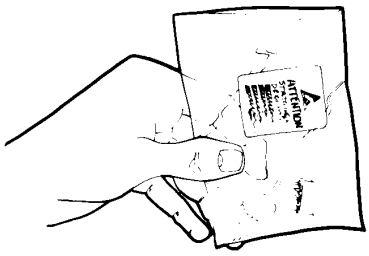
6. Keep component leads shorted together whenever possible.



7. Handle PCBs only by their edges. Do not handle by the edge connectors.



8. Lift & handle solid state devices by their bodies – never by their leads.



9. Transport and store PCBs and other static sensitive devices in static-shielded containers.

10. ADDITIONAL PRECAUTIONS:

- Keep workspaces clean and free of any objects capable of holding or storing a static charge.
- Connect soldering tools to an earth ground.
- Use only special anti-static suction or wick-type desoldering tools.

Figure 1-2. *Static Sensitive Component Handling Procedures*

1-13 RECOMMENDED TEST EQUIPMENT

Table 1-1 lists the recommended test equipment to be used for all maintenance activities for all Series 37XXXC models. Note the "Use" codes listed in the right hand column of the table. These codes list the applicable maintenance activities for the equipment listed.

Table 1-1. *Recommended Test Equipment (1 of 2)*

INSTRUMENT	CRITICAL SPECIFICATION	RECOMMENDED MANUFACTURER/MODEL	USE**
Computer/Controller	PC with Windows 95 or later and National Instruments GPIB hardware and software.	Any	O, P
Test Software	Automates testing of VNA, Software Version 4.01 and subsequent	Anritsu 2300-178	O
Floppy Disk	Formatted, IBM PC format	DS/HD 1.44 Mbyte	A
GPIB Cable	IEEE 488-2 compliant	Anritsu 2100-2, or equivalent	O, P, A
Adapter	Anritsu K to V	Anritsu 34VFK50	A
BNC Cable	Length, 4 ft., 2 each	Any	O
Printer Port Test Fixture	Provides print services	Anritsu B39553	O
Thru Line	For instruments with GPC-7 connector Test Ports: For instruments with K connector Test Ports: For instruments with V connector Test Ports:	Anritsu 3670A50-2, 3671A50-2 Anritsu 3670K50-2, 3671K50-2 Anritsu 3670V50-2	O, P
Calibration Kit	For instruments with Option 7A: For instruments with Option 7N or 7NF: For instruments with Option 7S: For instruments without Option 7: For models 37X77C, 37X97C	Anritsu 3651-1* Anritsu 3653 Anritsu 3650-1* Anritsu 3652-1* Anritsu 3654B	O, P
Performance Verification Software	Automates performance verification testing	Anritsu 2300-496 (for ME7808A system only) or Anritsu 2300-237 (excludes W1 connector support)	P
Verification Kit	For instruments with Option 7A: For instruments with Option 7N or 7NF: For instruments with Option 7S: For instruments without Option 7: For models 37X77C, 37X97C	Anritsu 3667 Anritsu 3663 Anritsu 3666 Anritsu 3668 Anritsu 3669B	P

* Calibration Kit sliding load (Option {-1}), required for Performance Verification only.

** USE CODES:
- A Adjustment / Internal Hardware Calibration
- O Operational Testing
- P Performance Verification
- T Troubleshooting

Table 1-1. *Recommended Test Equipment (2 of 2)*

INSTRUMENT	CRITICAL SPECIFICATION	RECOMMENDED MANUFACTURER/MODEL	USE**
Assurance Air Line	*None*	Anritsu model T2023 (K connector) or Anritsu model T2025-2 (V connector)	O
Offset Termination	For models 37X17C and below w/Opt 7A, 7N, 7NF: Other instruments 40 GHz and below 50 and 65 GHz models	Anritsu 29A50-20 Anritsu 29KF50-15 Contact Factory	O
Frequency Counter	*Frequency:* 0.1 to 26.5 GHz *Input Impedance*: 50Ω	EIP Microwave, Inc., Model 578B (Must be EIP brand with Band 3 input to 26.5 GHz and GPIB interface) or Anritsu MF2413B	A, O O
Digital Multimeter	*None*	Any	T
Oscilloscope	*None*	Tektronix, Inc. Model 2445	T
Power Meter 1, with:	*Power Range:* –30 to +20 dBm (1 mW to 100 mW) *Other:* GPIB controllable	Anritsu Model ML243xA Power Meter	A, O
Power Sensor 1 ***or:***	*Frequency Range:* Useable to the full frequency range of the VNA	MA2474A (40 GHz and below) Model SC6230 (to 65 GHz)	A, O
Power Meter 2, with: Power Sensor 2	*Power Range:* –70 to +47 dBm (100 pW to 50 W) *Other:* GPIB controllable *Frequency Range:* 0.01 to 40 GHz	Gigatronics 8541 or 8542 Gigatronics 80304A	

** USE CODES:
- A Adjustment / Internal Hardware Calibration
- O Operational Testing
- P Performance Verification
- T Troubleshooting

Chapter 2
Replaceable Parts

Table of Contents

Table 2-1. *Anritsu Service Centers*

UNITED STATES

ANRITSU COMPANY
490 Jarvis Drive
Morgan Hill, CA 95037-2809
Telephone: (408) 776-8300
1-800-ANRITSU
FAX: 408-776-1744

ANRITSU COMPANY
10 New Maple Ave., Unit 305
Pine Brook, NJ 07058
Telephone: (201) 227-8999,
1-800-ANRITSU
FAX: 201-575-0092

ANRITSU COMPANY
1155 E. Collins Blvd
Richardson, TX 75081
Telephone: 1-800-ANRITSU
FAX: 972-671-1877

AUSTRALIA

ANRITSU PTY. LTD.
Unit 3, 170 Foster Road
Mt Waverley, VIC 3149
Australia
Telephone: 03-9558-8177
FAX: 03-9558-8255

BRAZIL

ANRITSU ELECTRONICA LTDA.
Praia de Botafogo, 440, Sala 2401
CEP22250-040, Rio de Janeiro, RJ,
Brasil
Telephone: 021-527-6922
FAX: 021-53-71-456

CANADA

ANRITSU INSTRUMENTS LTD.
215 Stafford Road, Unit 102
Nepean, Ontario K2H 9C1
Telephone: (613) 828-4090
FAX: (613) 828-5400

CHINA

ANRITSU ELECTRONICS (SHANGHAI)
CO. LTD.
2F, Rm B, 52 Section Factory Building

No. 516 Fu Te Rd (N)
Shanghai 200131 P.R. China
Telephone: 21-58680226, 58680227,
58680228
FAX: 21-58680588

FRANCE

ANRITSU S.A
9 Avenue du Quebec
Zone de Courtaboeuf
91951 Les Ulis Cedex
Telephone: 016-09-21-550
FAX: 016-44-61-065

GERMANY

ANRITSU GmbH
Grafenberger Allee 54-56
D-40237 Dusseldorf, Germany
Telephone: 0211-968550
FAX: 0211-9685555

INDIA

MEERA AGENCIES (P) LTD.
A23 Hauz Khas
New Delhi, India 110016
Telephone: 011-685-3959
FAX: 011-686-6720

ISRAEL

TECH-CENT, LTD.
4 Raul Valenberg St
Tel-Aviv 69719
Telephone: (03) 64-78-563
FAX: (03) 64-78-334

ITALY

ANRITSU Sp.A
Roma Office
Via E. Vittorini, 129
00144 Roma EUR
Telephone: (06) 50-99-711
FAX: (06) 50-22-4252

KOREA

ANRITSU CORPORATION LTD.
8F Samwon Building
1329-8, Seocho-Dong
Seocho-Ku
Seoul, South Korea 137-070
Telephone: 02-581-6603
FAX: 02-582-6603

JAPAN

ANRITSU CUSTOMER SERVICES LTD.
1800 Onna Atsugi-shi
Kanagawa-Prf. 243 Japan
Telephone: 0462-96-6688
FAX: 0462-25-8379

SINGAPORE

ANRITSU (SINGAPORE) PTE LTD.
10, Hoe Chiang Road
#07-01/02 Keppel Towers
Singapore 089315
Telephone: 282-2400
FAX: 282-2533

SOUTH AFRICA

ETECSA
12 Surrey Square Office Park
330 Surrey Avenue
Ferndale, Randburt, 2194
South Africa
Telephone: 011-27-11-787-7200
FAX: 011-27-11-787-0446

SWEDEN

ANRITSU AB
Borgafjordsgatan 13
164 40 Kista
Telephone: +46-8-534-70700
FAX: +46-8-53470730

TAIWAN

ANRITSU CO., LTD.
6F, No. 96, Section 3
Chien Kuo N. Road
Taipei, Taiwan, R.O.C.
Telephone: (02) 515-6050
FAX: (02) 509-5519

UNITED KINGDOM

ANRITSU LTD.
200 Capability Green
Luton, Bedfordshire
LU1 3LU, England
Telephone: 015-82-433200
FAX: 015-82-731303

Chapter 2
Replaceable Parts

2-1 INTRODUCTION

This chapter provides replaceable parts information for all 37XXXC models. The major replaceable VNA assemblies and parts are listed and locations shown in this chapter. Parts and assemblies that are found on on the ME7808A Broadband systems are itemized in Appendix D.

2-2 EXCHANGE ASSEMBLY PROGRAM

Anritsu maintains a module exchange program for selected subassemblies. If a malfunction occurs in one of these subassemblies, the defective item can be exchanged. Upon receiving your request, Anritsu will ship the exchange subassembly to you, typically within 24 hours. You then have 45 days in which to return the defective item. All exchange subassemblies or RF assemblies are warranted for 90 days from the date of shipment, or for the balance of the original equipment warranty, whichever is longer.

> ***NOTE***
> When sending a failed assembly to the factory for exchange, a copy of the Service Log *must always* accompany the failed assembly. This copy may be a printout, or a saved disk copy. Due to the importance of the service log information to the Anritsu factory Service Engineers, the exchange prices are only valid if the service log data is included with the failed assembly.

Please have the exact model number and serial number of your unit available when requesting this service, as the information about your unit is filed according to the instrument's model and serial number. For more information about the program, contact your local sales representative (Table 2-1) or call Anritsu Customer Service direct (refer to Section 2-4.

2-3 REPLACEABLE SUBASSEMBLIES AND PARTS

Most assemblies listed on Tables 2-2 through 2-6 are available on the exchange program. Items found on Tables 2-7 and 2-9 are non-exchange parts

2-4 PARTS ORDERING INFORMATION

All parts listed in Tables 2-2 through 2- 9 may be ordered from your local Anritsu service center (Table 2-1, page 2-2). Or, they may be ordered directly from the factory at the following address:

Anritsu Company
ATTN: Customer Service
490 Jarvis Drive
Morgan Hill, CA 95037-2809

Telephone: (408)-778-2000
FAX: (408)-778-0239

Table 2-2. *Printed Circuit Board Assemblies**

Reference Designator	37XXXC Option	Assembly / Part	Part Number**
A1		LO1	D46866-7
A2		LO2	50725-3
A3		Test A IF	D38503-4
A4		Reference IF	D41794-4
A5		A/D	D38505-4
A6		Test B IF	D38503-5
A7	Without Opt 10A	10 MHz/LO3	D38507-3
A7	With Opt 10A	10 MHz/LO3	D38507-4
A8		Source Lock/ Separation Control	49334-4 or 53971-3*
A9		Main Processor	ND55009
A13		I/O #1	D38513-3
A14		I/O #2	D38514-3
A15		Graphics Processor	D44281-3
A16		Hard Disk (w/ PCB)	ND55506
A18		Rear Panel PCB	D44255-3
A19		Front Panel Switch PCB	D44279-3
A20		Front Panel Control PCB	D44280-3
A21A1		Source YIG/Bias Control (p/o Signal Source Module)	48512-3
A21A2		Source Control (p/o Signal Source Module)	48513-3
A24		VME Bus Terminator	D38524-3

* A8 model 53971-3 on ME7808A Broadband instruments.
** Part numbers shown in this column are suitable for use in most 37XXXC models. However, to ensure compatibility with other assemblies in the VNA, order the part number shown the PCB that is being replaced. In many cases, a kit containing the PCB and replacement instructions will be sent by Anritsu.

NOTE
The VNA A17 Motherboard PCB Assembly is not a field-replaceable item.

Table 2-3. *Test Set Assembly RF/Microwave Components, 37X17C, 37X25C, 37X47C, 37X69C (Excluding 50 and 65 GHz models)*

Assembly / Part	37XXXC Model / Option	Part Number
Transfer Switch	All	46535
Step Attenuator, 70 dB	All	4612K
Low Frequency Bridge w/ Bias Tee	37X17C	D28985
Coupler	37X25C and higher	D29422
Buffer Amp/Power Amplifier	All	See Table 2-5
Switched Doubler Module (SDM)	37269C only	D28540
Switched Doubler Module (SDM)	37369C only	D28685 or 47520
Port 2 Step Attenuator	All	4612K
RF Access Loops (front and rear panel)	All	ND54936
Bias Tee	37325C, 347C, 369C	48383

Table 2-4. *Test Set Assembly RF/Microwave Components, 50 and 65 GHz Models*

Assembly / Part	Part Number
SPDT switch	29855
Switched Doubler Module (SDM)	47520
Quadrupler (SQM)	48998
37 GHz High Pass Filter	49247
Mux Coupler (Port 1)	49470
Mux Coupler (Port 2)	49480
Shaped Pad	52956
Bias Tee	53409
16.8 GHz Lowpass Filter	B28612
RF Access Loops (Front and Rear Panel)	ND54918
Transfer Switch	D27030-2
3 dB Fixed Attenuator	ND26178
Step Attenuator	ND52564
Coupler	ND52929
Buffer Amplifier/Power Amplifier	See Table 2-5

Table 2-5. *Buffer/Power Amp Replacement Kits*

Buffer Amp Part	Replacement Kit
D44362	ND47532
D44364	ND47533
D44364 with MC002460 label	ND54995
ND54966	ND54995
54966	ND54995
54277	ND53793
44733	ND53249
53005	ND54940
58437	ND61660

Table 2-6. *Miscellaneous /Integrated Assemblies*

Assembly / Part	37XXXC Model / Option	Part Number
10 MHz Ovenized Oscillator (mounted on rear panel)	Opt 10A only	ND39476
Floppy Disk Assy	All	ND54926
Fan Assembly, Rear Panel	All	B38533
Power Supply (mounted on rear panel)	All	40-114
Power Supply (mounted on left side of chassis)	All	ND63006
Liquid Crystal Display (LCD)	All	15-100

Table 2-7. *Consumable Parts/Software*

Assembly / Part	37XXXC Model / Option	Part Number
System Software	All	2300-212
Front Panel Encoder Knob	All	2000-557
Fuse, 8A, Fast Blow 3AG Cartridge type (F1 Line fuse for power supply assembly)	All	631-72
Battery Backed RAM	All	54-1350*
Back-Up Battery	All	633-20*
LCD Back Light Driver PCB	All	ND63007
System Firmware (A9 bootup)	All	58-1321

* If A9 PCB is part number 54347. Contact factory if A9 is part number 55355 or above.

Table 2-8. *Signal Source Module RF/Microwave Components*

Assembly / Part	37XXXC Model / Option	Part Number
YIG Oscillator (2 to 20 GHz)	All	C21620-1
Down Converter	All	D27532
Switched Filter	37317C, 37217C, 37225C, 37247C, 37269C	D45243
Switched Filter	All models not listed above	D45244

Table 2-9. *Factory Repairable Non-Exchangeable Parts*

Assembly / Part	37XXXC Model / Option	Part Number
Test Port Connector, K-Male	All	34UK50
Test Port Connector, GPC-7	Opt 7A only	34UA50
Test Port Connector, 3.5 mm	Opt 7S only	34US50
Test Port Connector, type N	Opt 7N only	34UN50
Test Port Connector, type NF	Opt 7NF only	34UNF50
Test Port Connector, V	50 and 65 GHz models	34YV50 or 34YV50B

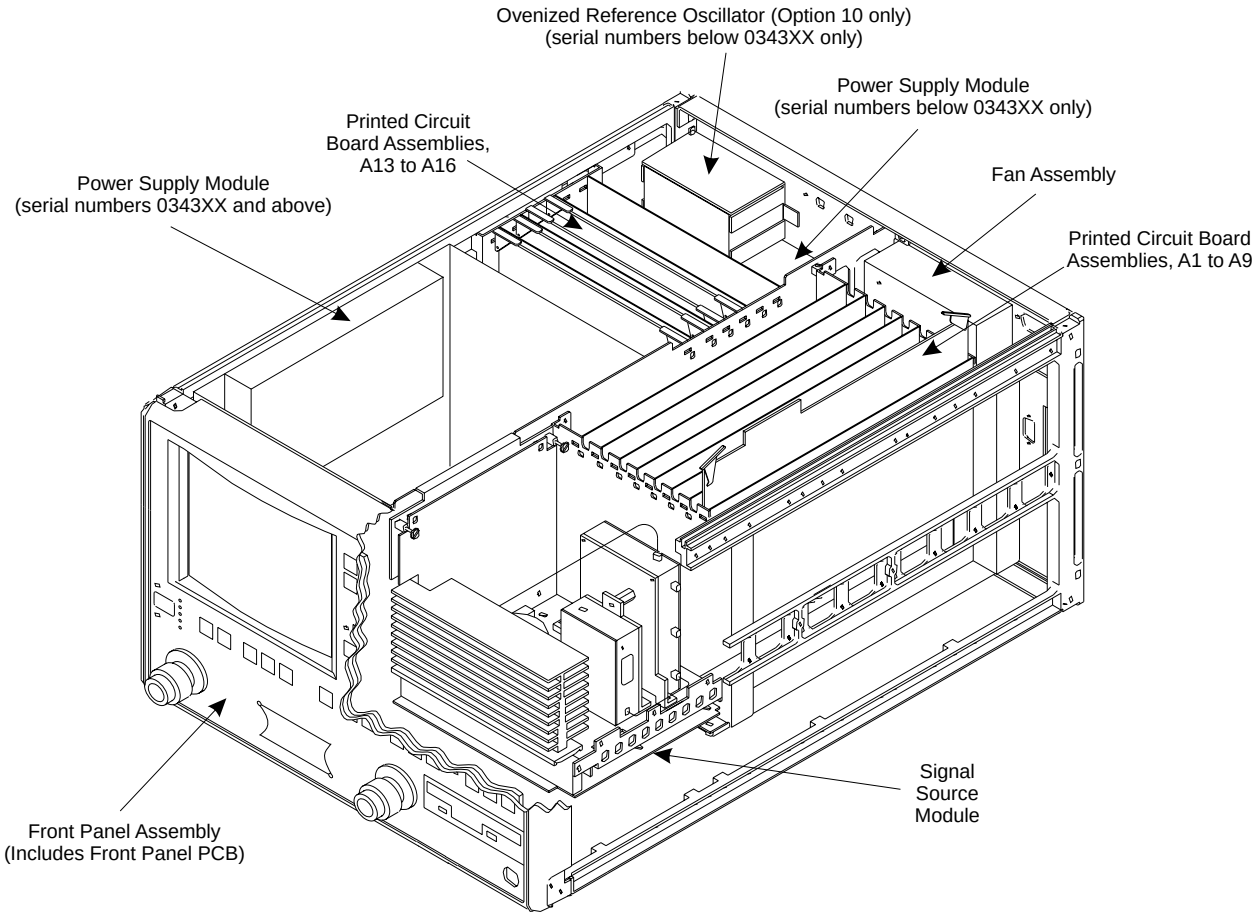


Figure 2-1. *Major Assemblies Location Diagram (Top View)*

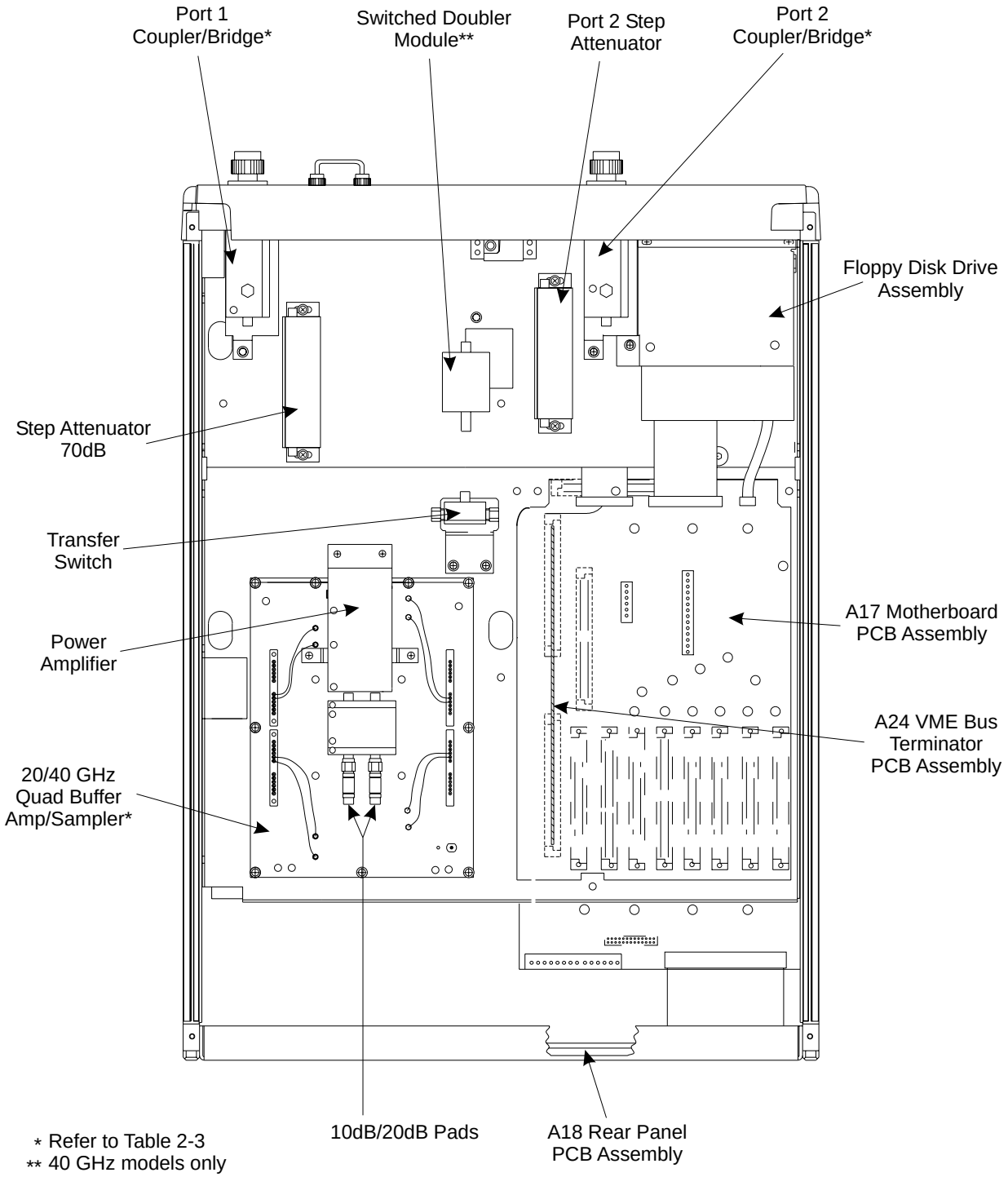


Figure 2-2. *Major Assemblies Location Diagram (Bottom View) (Excluding 50 and 65 GHz models)*

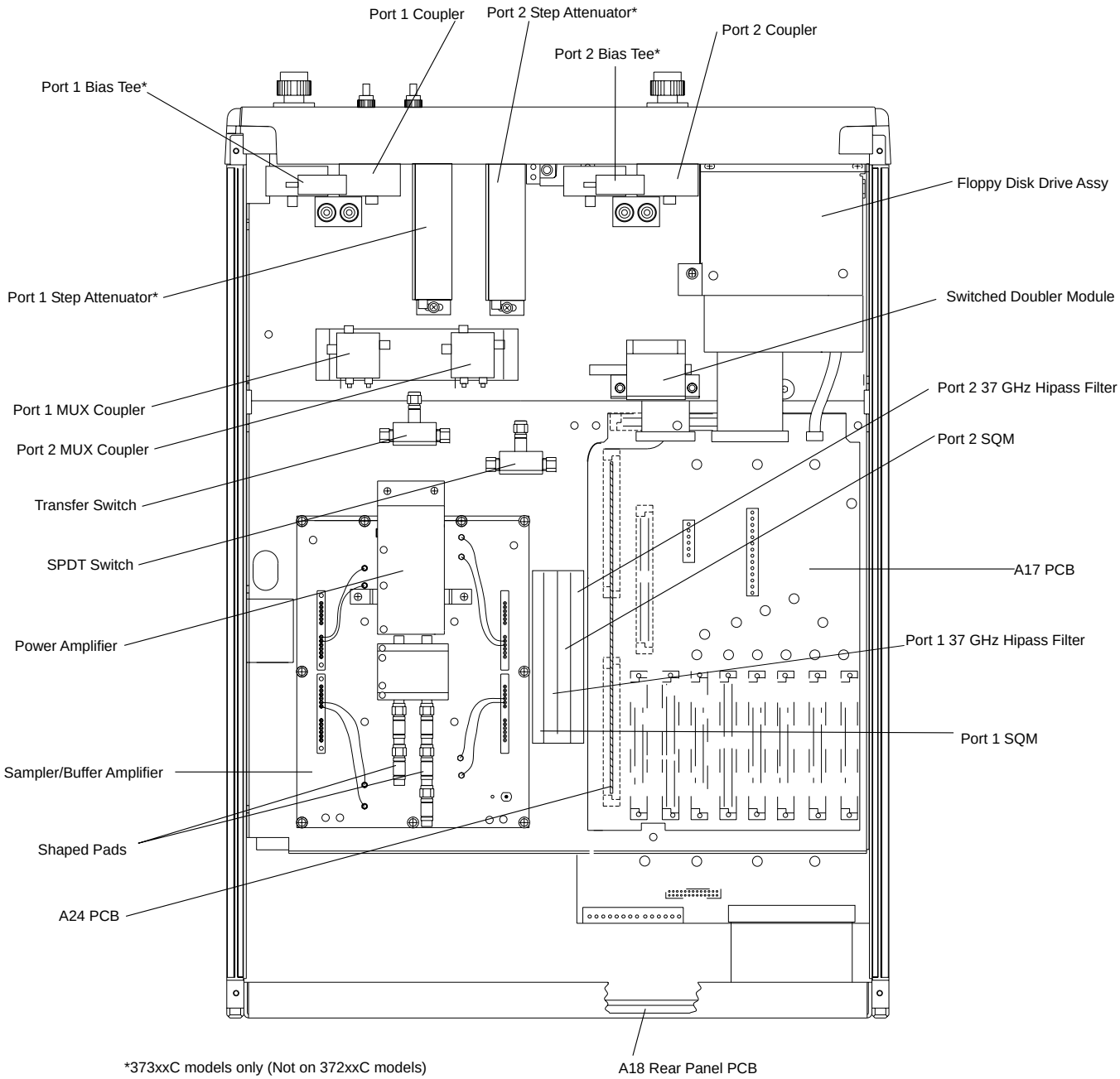


Figure 2-3. *Major Assemblies Location Diagram (Bottom View) (50 and 65 GHz models only)*

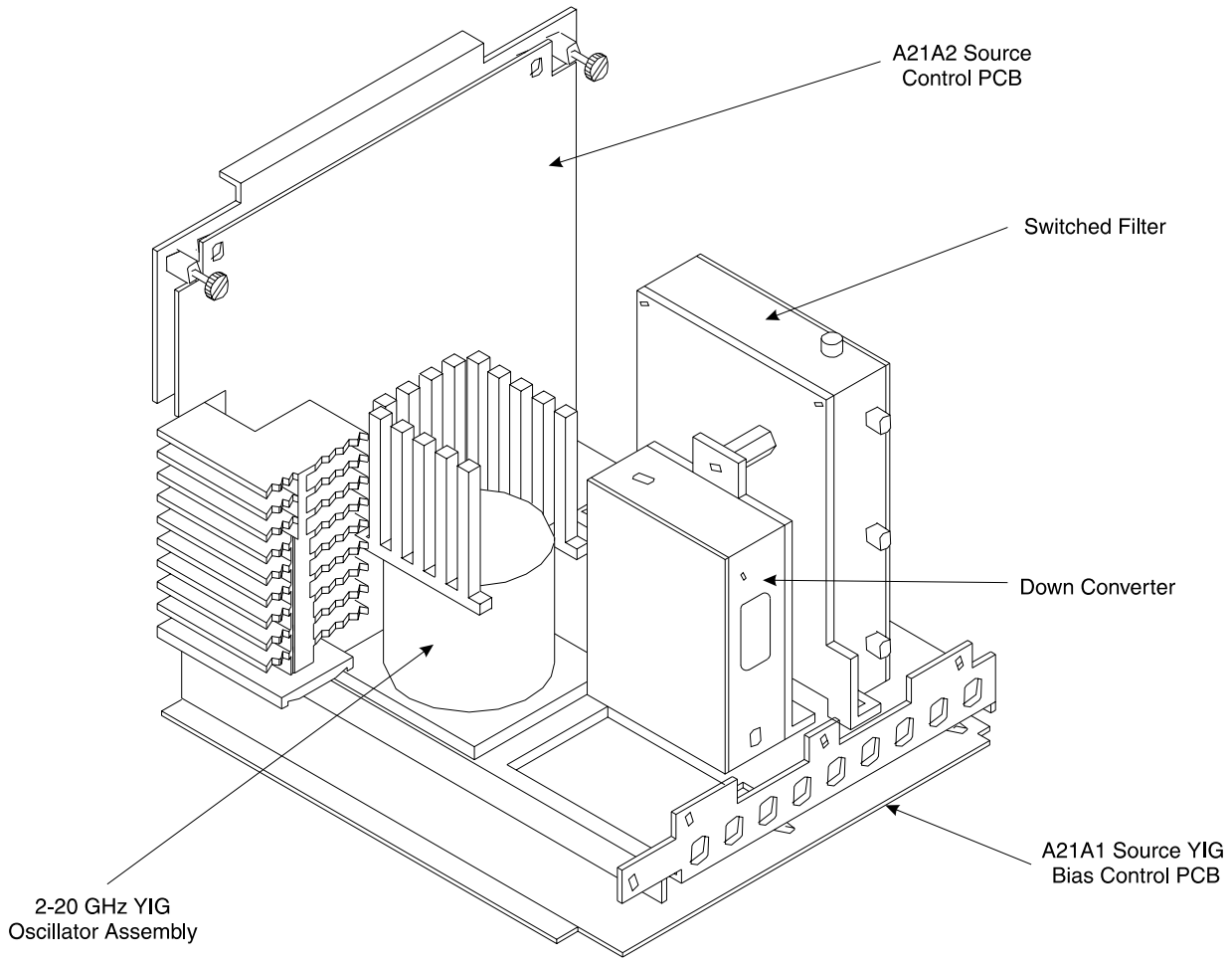


Figure 2-4. *Signal Source Parts Location Diagram*

Chapter 3
Theory of Operation

Table of Contents

Chapter 3
Theory of Operation

3-1 INTRODUCTION

This chapter provides a brief overview of the functional assemblies and major parts that comprise a typical 37XXXC VNA system. It also briefly describes the operation of each major assembly. Further details of the ME7808A Broadband system are found in Appendix D.

3-2 SYSTEM OVERVIEW

37XXXC Vector Network Analyzers are ratio measurement systems used to measure complex vector signal characteristics (real/imaginary, magnitude/phase, etc) of devices and systems in the 22.5 MHz to 65 GHz frequency range.

The VNA performs these measurements by sourcing a stimulus signal to the Device Under Test (DUT) that is connected to the front panel Port 1 and/or Port2 connectors. (See Figure 3-1 or 3-2). It simultaneously measures the DUT response, which consists of reflected and/or transmitted (attenuated, or amplified) signals at the connectors of the DUT. The reflected and/or transmitted signal(s), and a sample of the stimulus signal, are down converted and then transformed into their real and imaginary vector components. The resultant vector components are measured and converted into digital information. This digital information is sent to the Main Processor PCB where the desired S-parameter data is normalized and then presented to the user via the front panel color display. The display information is also sent to the rear panel VGA Out connector for use with an external VGA monitor.

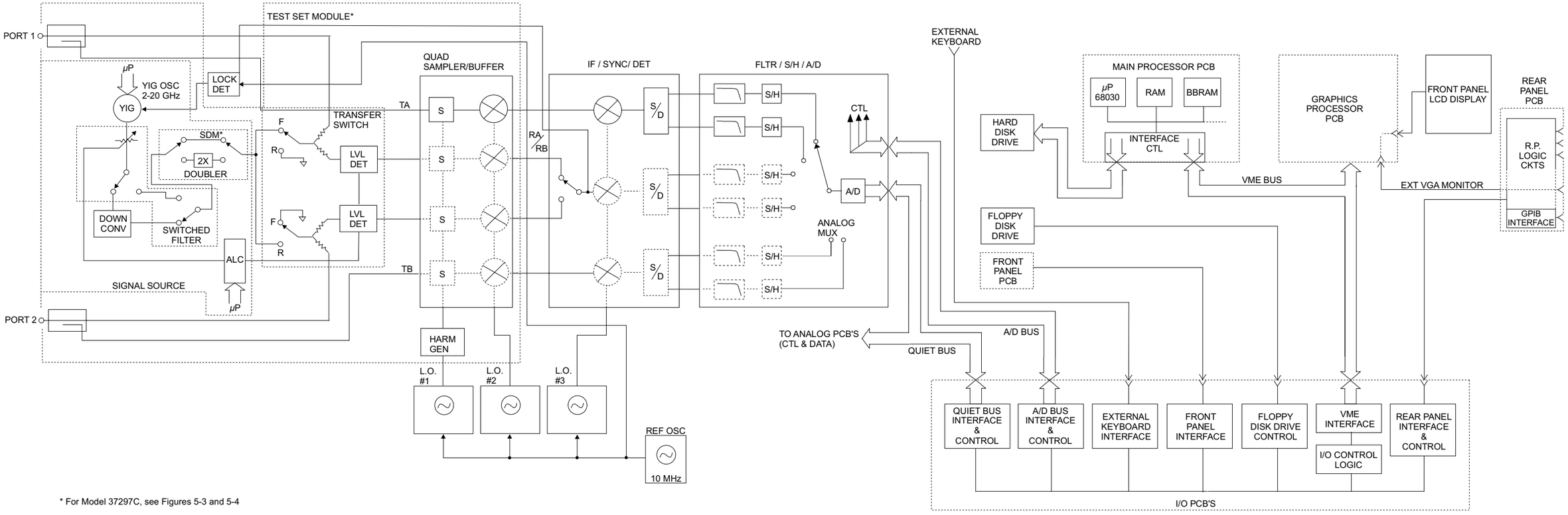
The normalized measurement information is also sent to the rear panel Printer Out connector for use with an external printer and/or plotter.

A front panel keypad, a rotary knob, and an IBM compatible keyboard interface provide user interaction with VNA Main Processor PCB.

The system is equipped with internal hard disk and floppy disk drives and battery backed internal memories for storage and retrieval of data and front panel setup information.

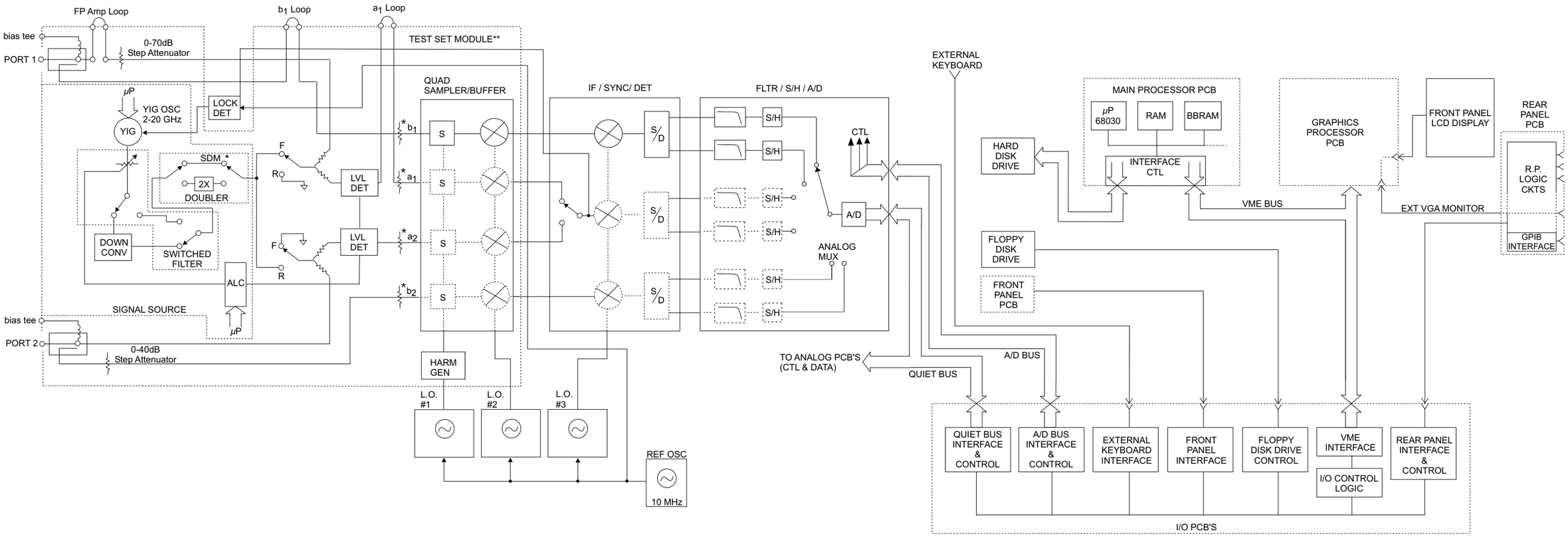
The VNA implements an IEEE 488.2 interface. This GPIB interface allows an externally connected instrument controller to control the VNA system in the “Remote-Only” mode. All VNA measurement and input/output operations may be controlled remotely in this mode.

An internal service log stores a record of system failures, data about the failures, and other key system service information. The service log is implemented using internal battery-backed SRAM memory.



* For Model 37297C, see Figures 5-3 and 5-4

Figure 3-1. *Overall Block Digram of 372XXC Models*



*Model shown is a 37369C. SDM/Transfer Switch section various greatly from model to model.

Figure 3-2. *Overall Block Digram of 373XXC VNA System*

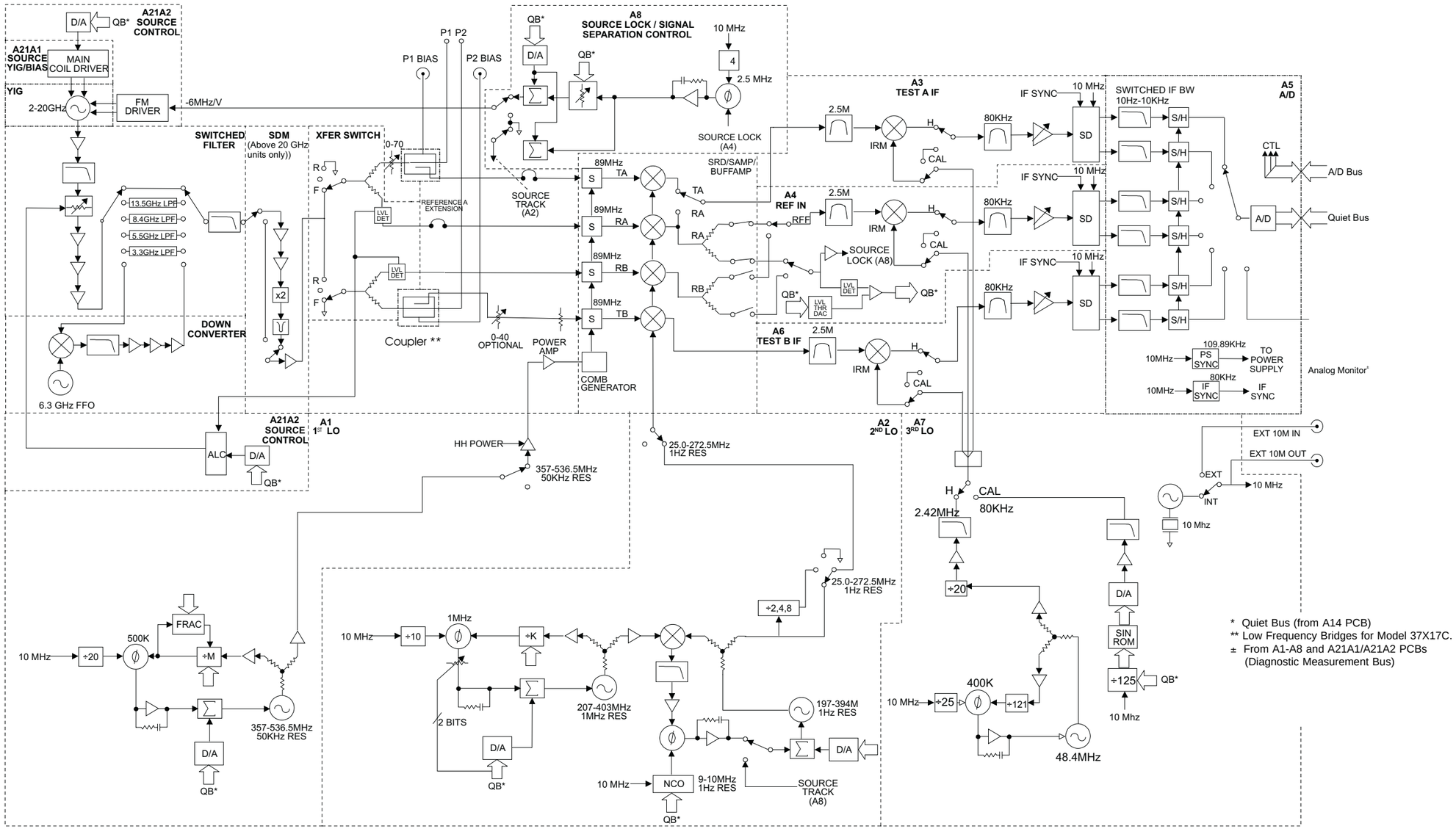


Figure 3-3. *Analog Subsystem Block Diagram*

3-3 ANALOG SUBSYSTEM ASSEMBLIES

The following sections briefly describe the major assemblies that comprise the VNA Analog Subsystem. Descriptions of the functions performed by each assembly are also included.

Signal Source Module

The Signal Source Module consists of the items listed below; refer to the block diagram of the Analog Subsystem (Figure 3-3).

- 2-20 GHz YIG Oscillator Assembly
- A21A1 YIG/Bias Controller PCB
- A21A2 Source Control PCB
- Switched Filter Assembly
- Down Converter Assembly

The Signal Source Module is a swept frequency signal generator that produces a phase locked (and leveled) output signal within a range of 22.5 MHz to 20 GHz. All 37XXXC models employ phase-lock control of the signal source module so that the output frequency is accurate and stable. The output signal is phase locked by the –6 MHz/volt control signal fed back from the A8 Source Lock/Separation Control PCB Assembly (which is described in following sections).

All Series 37XXXC VNA models use a single YIG-tuned oscillator to produce fundamental frequency source signals from 2.0 to 20 GHz. All other output frequencies are derived from the fundamental frequencies generated by the YIG-tuned oscillator. The signal source output frequencies for the low end portion of the frequency range (22.5 MHz to 2.0 GHz) are produced by down converting YIG fundamental signals in the range of 6.3225 to 8.3 GHz.

For 40 GHz models, the signal source output frequencies for the high end portion of the frequency range (20 to 40 GHz) are produced by the Switched Doubler Module that doubles the YIG fundamental signals in the range of 10 to 20 GHz. The Switched Doubler Module (SDM) is located in the Test Set Module (described below.) The A21A2 Source Control PCB assembly provides all bias and control signals for the SDM. 50 and 65 GHz models use an SDM to create frequencies from 20 to 38 GHz, and they use Source Quadrupler Modules (SQM's) to create frequencies above 38 GHz.

The YIG-tuned oscillator generates a high-power RF output signal that has low broadband noise and low spurious content. The frequency of the YIG-tuned oscillator is controlled by means of :

- The YIG main tuning coil
- The YIG FM (fine tuning) coil

The system A9 Main Microprocessor PCB sends the data that represents the desired operating frequency to the A21A2 (Source Control) PCB, which converts the frequency data to analog signals. These signals are then sent to the A21A1 YIG/Bias Controller PCB. This PCB converts the analog signals to YIG main tuning coil current.

The main tuning coil current from A21A1 YIG/Bias Controller PCB coarsely tunes the YIG-tuned Oscillator to within a few megahertz of the final output frequency. The YIG phase-lock loop then fine tunes the YIG-tuned oscillator to the exact output frequency via the FM (fine tuning) coil.

The fundamental frequency source signal is leveled by a PIN Diode attenuator that is part of the Switched Filter Assembly. This attenuator is controlled by the Automatic Leveling Control (ALC) circuits that are located on the A21A2 Source Control PCB. The input to the ALC circuits is the DC feed-back signal from the leveling detectors located in the Test Set Module.

Depending on the frequency of operation, the fundamental signal is passed through one of four low-pass filters located in the Switched Filter Assembly. The cut-off frequencies for these filters are 3.3 GHz, 5.5 GHz, 8.4 GHz, and 13.5 GHz, respectively. The signal is then passed through a 20 GHz high pass filter before being routed either directly to the Test Set Module, or to the Down-Converter Assembly.

The signal is switched to the Down-Converter Assembly only when the VNA is operating in the low end portion of its frequency range. The frequency of the output signal from the Down-Converter Assembly is 22.5 MHz to 2 GHz for Model 37X17C and 40 MHz to 2 GHz for Models 37X25C and above. The output signal from the Down-Converter Assembly is routed to the Test Set Module.

Test Set Module

The Test Set Module (excluding 50 and 65 GHz models) consists of the items listed below (refer to Figure 3-2):

- Transfer Switch assembly
- Two Couplers (Models 37X25C and above) or two Low Frequency Bridges (Models 37C17C and below)
- Switched Doubler Module for 20 to 40 GHz operation (Model 37X69C)

In the Test Set Module, the 22.5 MHz to 20 GHz signal from the signal source module is switched (via the Transfer Switch) between the front panel Port 1 and Port 2 connectors. The Transfer Switch is controlled by the A8 Source Lock/Signal Separation PCB to set the direction of signal flow for the desired test (Port 1 = Forward; Port 2 = reverse). For operation between 20 GHz and 40 GHz, the stimulus signal is routed to the Switched Doubler Module before being sent to the Transfer Switch.

The stimulus signal is output to the DUT via directional couplers mounted directly to the Port 1 and Port 2 front panel connectors. Note that bridges are used instead of couplers in RF Models 37X17C.

Each output circuit path from the Transfer Switch contains a splitter. One path from each splitter goes to the associated directional coupler (Port 1/Port 2) and the other path feeds the associated "Reference" input of the Receiver Module (RA/RB) via level detectors, which are contained inside the transfer switch. The output generated by the two parallel configured level detectors is a DC signal that corresponds to the output level of the stimulus signal. This signal is the input signal for the ALC circuits located in the signal source module. Only the detector in the currently selected sweep direction actually generates the ALC control signal.

The Test Set simultaneously receives the reflected and transmitted device-under-test (DUT) signals via the Port 1/Port 2 directional couplers. These two test signals, along with a sample of the output RF stimulus (Reference) signal, are sent to the Receiver Module.

A7 PCB 10 MHz Timebase

Depending on the age of the VNA and the presence of Option 10A, the A7 PCB may have a 10 MHz TCXO Reference Time Base crystal mounted on the PCB or mounted to the instrument rear panel (details described below).

This 10 MHz signal is the master time base for the system and is routed to most PCBs in the VNA. The A7 PCB also contains a fixed 2.42 MHz Local Oscillator and an 80 kHz calibration signal. The 80 kHz calibration signal is periodically sent to the A3, A4, and A6 PCBs for self-calibration of IF amplifier circuits. (This occurs during the time when the message, "Calibrating IF, please wait" is displayed on the VNA.)

Note that after instrument serial number 0236XX (approximately), Option 10A is installed on all 37XXXC instruments. The location of the 10 MHz TCXO crystal is summarized below:

- **Option 10A Not Installed:** Crystal is mounted on the A7 (D38507-3) PCB
- **Option 10A Installed (instrument serial number 0342XX and below):** Crystal is mounted on the rear panel and is powered by +24 VDC from the A7 PCB
- **Option 10A Installed (instrument serial number 0342XX and above):** Crystal is mounted on the A7 PCB

Receiver Module

The Receiver Module consists of the items listed below (refer to Figure 3-3):

- Quad Sampler/Buffer Amplifier with integrated SRD (step recovery diode)
- Power Amplifier
- A1, LO1 PCB
- A2, LO2 PCB

The Receiver Module is a four channel two stage Sampler/Buffer Amplifier and Down Conversion unit. It simultaneously converts the four 22.5 MHz to 65 GHz signals from the Test Set Module into three 2.5 MHz IF signals that are output to the IF Section.

The first stage of the Receiver Module uses harmonic sampling to down-convert the four 22.5 MHz to 65 GHz output signals from the Test Set Module down to 89 MHz signals. Any input signals below 270 MHz are passed directly through the four harmonic samplers to the second stage without down-conversion. The drive signal to each of the harmonic samplers is a comb of harmonics generated by a step recovery diode (SRD).

The Power Amplifier provides the signal that drives the SRD. The input to the Power Amplifier is the 357 to 536.5 MHz signal from the A1 First Local Oscillator (LO1) PCB. Regardless of the operating frequency, the Power Amplifier is biased on at all times to insure optimum thermal stability.

The second stage of the Receiver Module uses the 25.0 to 272.5 MHz signal from the A2 Second Local Oscillator (LO2) PCB to down-convert the 89 MHz signals into four 2.5 MHz IF signals TA, TB, RA, RB (two test signals and two reference signals). Either the Reference A or the Reference B IF signal is selected, as is appropriate for Forward/Reverse operation. The resultant three 2.5 MHz IF signals (Test A, Test B, and Reference A/B) are output to the IF Section. A buffered version of the Reference A/B signal is also fed to the A8 Source Lock/Signal Separation Control PCB as the Source Lock signal.

The Receiver Module can also select the Reference A IF signal that is output to the IF Section via the Test A switch path. This IF signal is used during Line Reflect Line (LRL) Calibrations to ratio the Reference A and Reference B signals.

A8, Source Lock/Signal Separation and Control PCB

The Source Lock Phase Comparator circuit on the A8 Source Lock/ Signal Separation Control PCB compares the Source Lock (Reference A/B) signal from the Receiver Module with a signal derived from the 10 MHz reference oscillator. The output of this circuit is the –6 MHz/V correction signal, which is routed to the circuit on the A21A2 Source Control PCB that generates the FM coil tuning current signal. This signal is output to the A21A1 YIG/Bias Controller PCB to fine tune the YIG-tuned oscillator to the exact output frequency. When the YIG-tuned oscillator outputs the exact frequency, the two inputs to the phase comparator circuit on the A8 PCB match and the phase-lock loop is locked.

The A8 PCB Assembly also provides bias and control signals to the Test Set and Receiver Modules for operating the following circuits:

- Transfer Switch
- Power Amplifier
- Quad/Sampler Buffer Amplifier
- Front Panel Forward/Reverse LEDs
- Step Attenuators
- Control Signals to Model 3738A Test Set (Broadband Millimeter Wave Systems)

IF Section

The IF Section consists of the items listed below (refer to Figure 3-2):

- A3 Test A IF PCB
- A4, Reference IF PCB
- A5, A/D Converter PCB
- A6, Test B IF PCB
- A7, Third Local Oscillator, LO3, PCB

The IF Section converts the three 2.5 MHz IF signals from the Receiver Module into six DC output signals. The A3 (Test A), A4 (Reference A/B), and A6 (Test B) PCBs down-convert the 2.5 MHz input IF signals to 80 kHz IF signals and then adjust their amplitude for input to the synchronous detector stage of each PCB. Each 80 kHz IF signal is synchronously detected and converted into a pair of DC signals that contain the information for the real and imaginary portions of the original 80 kHz IF signal. Thus, the three IF signals (two test signals and the reference signal) yield six DC signals that fully represent the real and imaginary vector components of the DUT's S-parameters.

The IF Section also checks the 2.5 MHz phase lock signal for proper power level by comparing it to a known reference level on the A4 PCB. A sample of the 2.5 MHz Reference A/B IF signal is sent to the A8 Source Lock/Separation Control PCB assembly for phase locking the signal source module. The A3 and A6 PCBs are functionally identical and physically interchangeable.

A7 PCB, LO3 The A7, Third Local Oscillator (LO3) Assembly, provides a fixed 2.42 MHz Local Oscillator signal that is used on the A3, A4, and A6 PCBs to down-convert the 2.5 MHz IF signals to 80 kHz. It also provides an 80 kHz standard signal for the IF Section Calibration process that occurs automatically approximately every six minutes. This automatic IF Section Calibration is one of the VNA features that ensures rated measurement accuracy. Automatic IF Calibration can be turned off and/or invoked at any time during measurement sweeps.

A5 A/D Converter PCB The A5 A/D Converter PCB contains a six-channel, two stage, switched-filter sample-and-hold circuit and a 20 bit A/D converter. Each of the six DC signals from the A3, A4, and A6 PCBs are input to a separate channel of the PCB. The first stage of each channel is a low-pass filter with four selectable cutoff frequencies of 10 kHz, 1 kHz, 100 Hz, and 10 Hz. The second stage of each channel is a sample-and-hold amplifier that stores the signals during the A/D conversion process. Each channel is sequentially selected for input to the 20 bit A/D converter.

The A5 A/D Converter PCB also derives the 109.89 kHz Power Supply Synchronization Signal and the 80 kHz IF Synchronization Signal from the 10 MHz Reference Timebase. Additional functions of the A5, A/D Converter Assembly include:

- Measurement of power supply voltages and other internal nodes of the 372XXB for diagnostic purposes.
- Measurement of an externally applied analog input signal. This function is used for service purposes only.
- External Trigger Input signal processing (from rear panel)
- External Analog Output signal generation (to rear panel)

The A/D converter circuitry located on the A/5 PCB is used as a DVM to measure various internal system analog monitor points on the A1 to A8 and A21A1/ A21A2 PCBs. It is also used to monitor power supply voltages and other critical points throughout the VNA, which can be readout via the Diagnostics Menus. DVM readings are also recorded in the service log for certain system failures.

> ***NOTE***
> If this PCB is replaced, switch settings on the new PCB must be changed to match settings of the old PCB.

3-4 DIGITAL SUBSYSTEM ASSEMBLIES

The following sections briefly describe the major assemblies that comprise the VNA Digital Subsystem. The digital subsystem provides all system control, I/O interface, digital signal processing, and data presentation functions. The major assemblies that comprise the VNA digital PCB subsystem are listed below (refer to Figure 3-4):

- A9, Main Processor PCB
- A13, I/O Interface #1 PCB
- A14, I/O Interface #2 PCB
- A15, Graphics Processor PCB
- A16, Hard Disk PCB
- A18, Rear Panel Interface
- Rear Panel Assembly
- Front Panel Assembly
- Floppy Disk Assembly
- A24, VME Bus Terminator PCB

A9 Main Processor PCB Assembly

The major components that comprise the A9 Main Processor PCB are:

- 68040 Microprocessor (w/ integrated co-processor)—This is the CPU for the 37XXXC system.
- 16 MB SDRAM—This is the main system memory. This memory is volatile (non-battery backed). During normal operation, it stores the 37XXXC software that is loaded from disk at power-up.
- 8 KB BBRAM—This auxiliary memory chip contains a back-up battery that is continuously recharged whenever power is applied. (The back-up battery has a four year minimum life span.) This chip also contains real time and date clock functions. It is used to store low level boot-up parameters, ALC calibration data, source frequency calibration data, and service log header data.
- 512 KB SRAM—This auxiliary memory is backed-up by a non-rechargeable Lithium battery that provides 200 days (maximum) of power-off protection. It is used to store current and saved front panel setups, trace/normalization data, current RF calibration data, current sweep frequency data, flat power calibration data, and the service log error list.
- VME Bus interface chip—This chip is used to interface the Main Processor PCB to the A13, A14, and A15 digital PCBs (via the VME bus interface).
- SCSI Bus interface—This chip is used to interface the Main Processor PCB to the A16 Hard Disk PCB.
- System boot-up EPROM—This chip contains the boot-up instructions used by the system CPU at power-up.

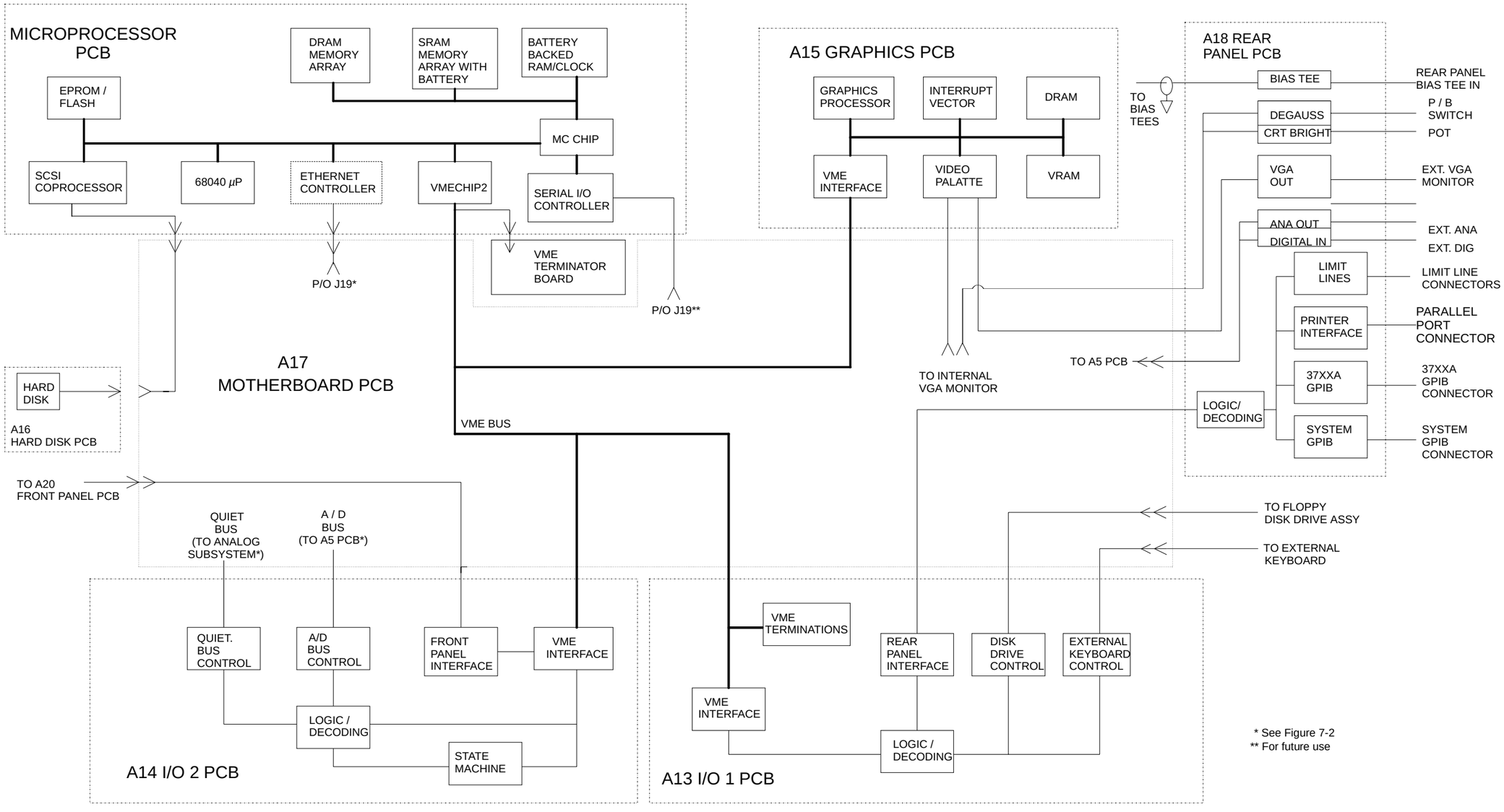


Figure 3-4. *DigitalSubsystem Block Diagram*

A13 I/O Interface #1 PCB Assembly

This PCB assembly performs the following functions:

- Floppy drive control—interface for the Floppy Drive Assembly
- External Keyboard control—interface for the front panel Keyboard connector
- Interface for the A18 Rear Panel PCB Assembly (below)
- Interface and control for the rear panel IEEE 488.2 GPIB and Dedicated GPIB interface connectors

A14 I/O Interface #2 PCB Assembly

This PCB assembly contains a State Machine controller, decode logic, and bus interface control circuits that perform the following functions:

- Quiet Bus interface control—The Quiet Bus passes control and data signals from the A9 Main Processor PCB to the A1 through A8, and A21 PCBs and returns status and data signals back to the A9 PCB. This bus is managed by the control circuits on the A14 PCB such that it is inactive during the the time that a measurement is being taken.

> ***NOTE***
> The output data from the A5 PCB A/D converter is sent to the A9 Main Processor PCB via the Quiet Bus, the A14 PCB, and the VME Bus.

- A/D Bus interface control—During the measurement process, all A/D selection and conversion functions on the A5 PCB are controlled exclusively by the A14 PCB State Machine Controller. This is accomplished via the command lines of the A/D Bus.
- Measurement control functions—the A14 PCB State Machine Controller manages many of the VNA functions during a measurement, as follows:
  - Quiet Bus interface control
  - A/D Bus interface control:
    - Sample and Hold control for A5 PCB
    - A/D selection and conversion control for A5 PCB
  - Check for phase lock condition
  - Gain ranging
  - Delay generation for IF Bandwidth setting function

The A14 PCB also provides the interface to the Front Panel A19 and A20 PCBs.

A15 Graphics Processor PCB Assembly

This PCB assembly contains circuitry that simultaneously drives both the LCD display and an external VGA monitor (if used) as follows:

- Receives measurement and display information from the A9 Main Processor PCB and generates screen display (video) information.
- Provides interface and control for the LCD display assembly.
- Provides interface for an external monitor via the rear panel VGA Out connector.

A16 Hard Disk PCB Assembly

The PCB assembly contains a pre-formatted hard disk drive assembly and associated interface circuitry. The A16 PCB interfaces directly with the A9 Main Processor PCB via the (A9) SCSI interface.

Instrument serial numbers 0342XX and below use a thermal shutdown switch on the A16 PCB to shut the VNA off in the event that the instrument overheats. Above instrument serial number 0343XX, the thermal shutdown switch is mounted on the power supply module.

Floppy Disk Drive Assembly

This unit is a standard 1.44 MByte DOS compatible format floppy disk drive. It is physically mounted to the test set tray (not to the Front Panel Assembly). It interfaces with the system via the A13 I/O Interface #1 PCB.

A24 VME Bus Terminator PCB

This PCB assembly terminates the VME bus to insure stable digital data transfer on the bus. It plugs into the VME bus structure on the bottom surface of the A17 Motherboard Assembly.

3-5 MAIN CHASSIS ASSEMBLIES

The assemblies described below are the major assemblies mounted to the basic frame of the VNA.

A17 System Motherboard Assembly

The motherboard assembly provides signal routing and D.C. power distribution paths for all major PCB assemblies of the Analog Subsystem (A1 to A8) and the Digital Subsystem (A9 to A16). It also contains the VME Bus, Quiet Bus, A/D Bus structures, and other signal routing paths. It does not contain any active components.

> ***NOTE***
> The motherboard assembly is an integral part of the VNA chassis. It is not a field replaceable unit.

Front Panel Assembly

The Front Panel Assembly consists of the following assemblies and parts:

- A19 Front Panel Switch PCB—this assembly contains all of the front panel switches for the VNA.
- A20 Front Panel Control PCB—this assembly contains the decode logic for the switches located on the A19 Front Panel Switch PCB. This PCB interfaces with the A14 I/O Interface #2 PCB Assembly.
- Front Panel LEDs, beeper, keys, controls, and connectors
- Front panel overlay
- Front panel casting

A18 Rear Panel Interface PCB

This PCB assembly contains the rear panel connectors listed below. It also includes the associated circuitry and cabling interfaces that link these connectors (and the rear panel fan assembly) to the A17 Motherboard PCB and other assemblies within the VNA.

- IEEE 488.2 GPIB connector (with associated interface circuits)
- Dedicated GPIB connector (with associated interface circuits)
- Printer Out connector (with associated interface circuits)
- VGA Out connector
- I/O Connector (and associated interface circuits)—This 25 pin miniature D-sub connector contains:
  - Limits Testing Status TTL outputs
  - Port 1 and Port 2 Bias inputs.
  - Ext Dig In signal (same as External Trigger BNC)
  - Ext Ana Out signal (same as External Analog Output BNC)

The A18 PCB also contains:

- Routing of –24 Vdc power to the rear panel system fan.
- Routing of External Analog Out and External Trigger Input signals to the Mother Board.

Power Supply Module

The Power Supply Module is a single self contained assembly mounted either on the rear panel or the left side of the chassis. This module provides:

- Unregulated +5, +9, ±18, and ±27 Vdc supply voltages to the other assemblies of the 372XXB
- Thermal and over-current shutdown protection circuitry
- Sensing and input power regulation for operation with 85 to 264 VAC, 48 to 63 Hz, universal AC line input power
- Internal fan cooling (for power supply module)
- Supply voltages distribution

Table 3-1 identifies all 37XXXC DC power supply voltages and lists their usage by the various PCB assemblies. Unless otherwise indicated, supply voltages are regulated on the assembly using them. The analog and digital power supply grounds are isolated.

> ***NOTE***
> All power supply voltages listed in Table 3-1 can be accessed via the A/D bus for measurement by the the A/D converter circuitry (for example, DVM) located on the A5 A/D PCB assembly.

Table 3-1. *37XXXC Power Supply Voltages and Usages*

Voltage	Assemblies Where Used
+5V	A1, A2, A3, A4, A5, A6, A7, A9, A13, A14, A15, A16, A18, A19/A20 (P.O. Front Panel), A21A1/A21A2 (P.O. Source Module), A24, External Keyboard
+9V	A1, A2, A7, A8
+18V	A1, A2, A3, A4, A5, A6, A7, A8, A13
-18V	A1, A2, A3, A4, A5, A6, A7, A8, A13
+27V	A1, A2, A5, A7
-27V	A5, A18
The following supply voltages are derived from the ±18 Vdc supply voltages on the A13 I/O #1 PCB:	
+12V	A9, A15
-12V	A9, A15

Chapter 4
Operational Performance Tests

Table of Contents

Chapter 4
Operational Performance Tests

4-1 INTRODUCTION

The tests in this chapter provide a means of fully testing the 37XXXC VNA system for proper operation and signal stability. These tests are intended to be used as a periodic check of the operational functionality of the VNA.

The tests should be performed in their entirety at least once annually. Although there is no requirement to do so, the tests should generally be run in the sequence presented.

> ***NOTE***
> The procedures presented in Chapter 5, System Performance Verification, provide the means to test the *accuracy* of the measurements performed by the VNA.

Please ensure you have read and fully understand the servicing concepts for the VNA presented in Chapter 1 prior to continuing with this chapter.

Operational tests for the VNA consist of the following:

- Checking the Service Log
- Self Test
- Peripherals and Interface Testing
- Signal Path tests (includes Checking the Service Log and Self Test)

These tests are described in Sections 4-2 through 4-5, which start on the next page.

4-2 CHECKING THE SERVICE LOG

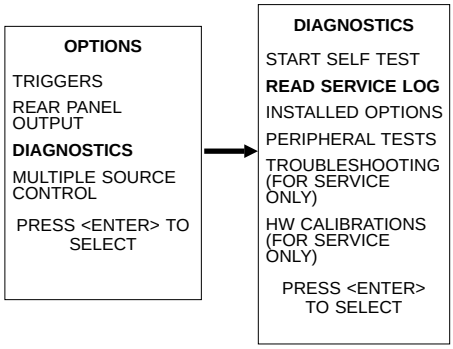
Checking the service log consists of viewing the entries written into the log.

> ***CAUTION***
>
> The service log contains historical information about instrument condition and any failures that may have occurred. It should be cleared only by a qualified service engineer. Such clearing should be accomplished only upon determining that the errors need not be saved to disk, or printed out for service purposes.

Procedure:

Step 1. Press the Option Menu key (Enhancement key group) to display the OPTIONS menu.

Step 2. Select **DIAGNOSTICS** from menu (left); then select **READ SERVICE LOG** from the DIAGNOSTICS menu.



The VNA will now display the contents of the service log. The display consists of a header and an error listing. The header contains a variety of system service information. The error listing contains error messages for failures that may have occurred during operation.

> ***NOTES***
>
> - Errors 7201 to 7209, GPIB remote operation programming errors, report that one or more external GPIB programming errors has been detected. These messages do not indicate a VNA system fault.
> - Informational messages 0000 to 0099 report the pass/fail status of a peripheral access. These messages do not indicate a VNA system fault.

Any other error messages in the service log may indicate an instrument problem and should be investigated. Refer to Chapter 7, Troubleshooting, for further information.

> ***CAUTION***
>
> The **CLEAR SERVICE LOG** menu selection will immediately and permanently clear all the error message entries from the service log. (However, it will not clear the header information.) See Caution message at top of page.

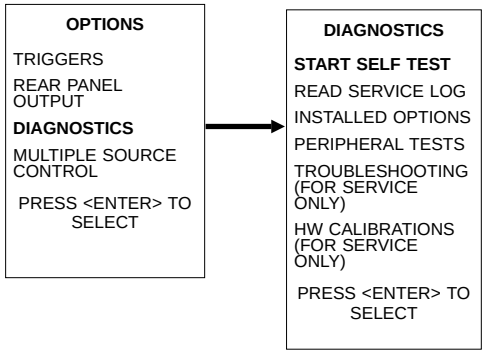
4-3 SELF TEST

The self test performs a series of tests that verify that various internal VNA circuits are functional and operating properly.

To start the self test:

Step 1. Press the Option Menu key (Enhancement key group) to display the OPTIONS menu.

Step 2. Select **DIAGNOSTICS** from menu; then select **START SELF TEST** (below).



Step 3. Wait for test sequence to complete. (Once invoked, this test requires no user interaction or external equipment.)

Upon completion, the net pass/fail result of the self test is shown on the display. If the VNA is in remote-only operation, the results are reported via the GPIB output buffer. If the self test fails, detailed error messages will be written into the service log.

If self test fails:

- ❑ Check the service log to view failure messages.
- ❑ Proceed to Chapter 7, Troubleshooting.

4-4 PERFORMANCE TESTS

The 37XXXC performance tests are contained within one executable program (3700TEST.EXE), Anritsu Software Part Number 2300-178. This includes approximately 15 different tests that cover nearly all of the RF devices and circuits within the VNA and is applicable for all 37XXXA/B/C model instruments.

The user interface consists of a single display from which the operator can control all aspects of the test program. It is suggested that the tests be performed in the sequence that they are shown on the display (top-to-bottom sequence), but this is not required. Any test may be performed multiple times or in any sequence. These tests should be performed prior to the verification tests described in Chapter 5, System Performance Verification.

The test program determines the model of the VNA and displays the applicable tests. One general test record and several data files will be created on the PC in a folder labeled 37000. This general test record records only Pass, Fail, Not Applicable, or Not Performed for each test. Other data files will record numerical data, if you so choose. All data files are readable and printable by a text reader such as Notepad.

Each test displays instructions for the operator. Some tests will prompt the operator for frequency characteristics of external test equipment connected.

Test Specifications

Beginning with version 4.20, specifications are clearly labeled as being "Typical" or "Guaranteed." The following tests have specifications that are guaranteed (repairable at no charge by Anritsu during the warranty period):

- Low Power Phase Lock
- Port 1 Power
- Source Match
- Directivity
- System Dynamic Range

All tests that are designated guaranteed allow the operator to store numerical test data to a file. Tests having guaranteed specifications must be performed under test program control.

Specifications that are typical are identical to factory specifications for new instruments. Anritsu does not guarantee the VNA will meet these specifications. If a test fails by a small margin, this does not indicate a problem with the instrument.

Required Equipment

- Windows-based PC with Windows 95 or higher.
- National Instruments GPIB interface card and associated software driver compatible with the installed Windows operating system.
- Standard GPIB interface cable, such as Anritsu part number 2100-2, must be connected between the VNA and the PC.
- Anritsu 365X calibration kit that matches the test port connectors of the VNA must be used. A sliding termination is required only if the Source Match or Directivity tests are to be performed. Only the female components of the calibration kit will be used.
- High quality RF cable suitable for the frequency range of the instrument. Anritsu 3670 or 3671 series throughlines are strongly recommended.
- High quality female to female adapter, such as Anritsu part number 33KFKF50B. Necessary if the above cable does not have a female connector on both ends.

> ***NOTE***
> SMA adapters (with a white teflon dielectric) are too poor in quality even for the lowest frequency VNAs.

Additional Required Equipment

- The Frequency Accuracy test requires an EIP brand frequency counter. Most models are acceptable, but GPIB, Band 3, and External 10 MHz reference input capabilities are required.
- The Port 1 Power test requires an Anritsu model ML24XX power meter with an appropriate power sensor. Other meters and sensors, as shown in Table 1-1, are also useable.
- The Source Match test requires an Anritsu Assurance Airline, such as model T1149 or T2025-2, typically available only from Anritsu Service Centers.
- The Directivity test requires an Anritsu Assurance Airline and offset termination, such as model 29KF50-15 or 29VF50-15, typically available only from Anritsu Service Centers.

Installation and Launching the Test Program

The program is a stand alone executable requiring that the National Instruments GPIB software parameters all be set to default conditions. The user will be asked to create the folder “C:\37000” for data storage, if that folder does not already exist on the PC. Additionally, the GPIB settings that are required for the 2300-496 Verification Software will also work with the 3700TEST.EXE program.

From your Windows-based PC, run the program (3700Test.exe). The program's interface will appear similar to the display below:

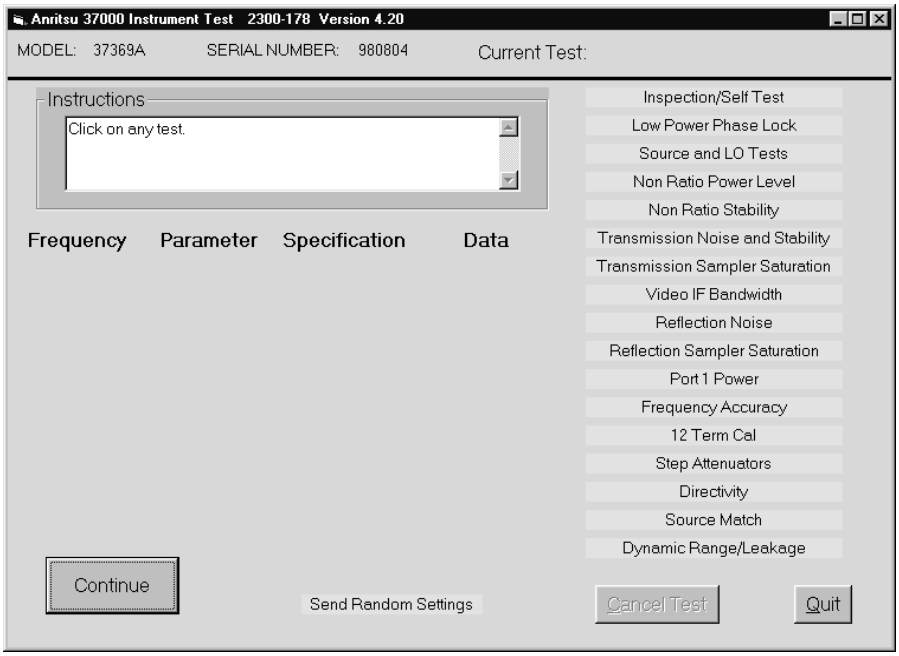


Figure 4-1. *2300-178 Software Interface*

Connect the GPIB cable between the PC and the upper GPIB connector of the VNA rear panel (labeled IEEE 488.2 GPIB). Turn on the VNA and verify the instrument address is 6 (found under the Utility Menu Key |GPIB ADDRESSES).

The Program will locate the VNA, and query the operator regarding his/her name, customer name, and Test Port type.

The program will create a file for Pass/Fail information named "123456.SVC" (where 123456 is the serial number of the VNA). If the program locates an existing .SVC file of the same instrument in the 37000 folder, the operator must decide whether to continue storing data to the existing .SVC test record or start a new .SVC record.

Labels of incomplete tests have a yellow background. A green background indicates that the test passed; a red background indicates that the test failed. (Some versions of the program do not use red to indicate failed tests.)

Running the Tests

To launch any test, simply click on the label of the test. In all tests, except the Front Panel floppy drive test, the operator should not remove the instrument from the Remote condition. Doing so will require restarting the program.

The text box will display instructions to the user. To continue with any test, click on the Continue button, press the space bar, or press <Enter>. To quit any test, press the <ESC> key or click on the Cancel button.

At the completion of the selected test, a Pass or Fail result will be displayed in the text box and written to the .SVC file. If the operator has chosen to record numerical data, it will be saved to the appropriate file. Select Continue to move to the next test.

Description of Tests

Inspection/Self Test:

This test performs the extended internal self test, launches the VNA front panel keyboard/knob test, starts the external keyboard test, and guides the user through a floppy drive test. It also prompts the user to check the pin depth of the Test Ports and to check the fuses in the bias tee circuits.

Low Power Phase Lock:

This test checks the ability of the instrument to maintain source phase lock at minimum source power.

If the test fails, performing a Source Lock Threshold calibration may solve the problem. If this does not solve the problem, it must be corrected by a trained Anritsu Service Engineer.

Source and LO Tests:

These tests use built-in VNA diagnostics to check all phase lock loop error voltages of the RF source, LO1, and LO2 of the down conversion section. Each display should fall within the prescribed limit lines.

If the test fails, a minor deviation outside of the limit lines will not cause any performance problem or measurement error. Performing a new Source Frequency calibration, LO1 calibration, or LO2 calibration will typically bring these voltages back into optimum range.

Non-Ratio Power:

This test checks the RF power level of the four individual RF paths in the VNA. The complete paths are checked beginning with the RF source and continuing out of the VNA Test Ports through the Down Conversion and A/D circuits. The RF reference paths passing through the rear panel RF cable (a1 IN and a1 OUT) are also checked.

If the test fails and depending on the severity of the power loss, the RF Source in the VNA may fail to phase lock (in worst cases) or the VNA's system dynamic range may be degraded. Ensure the the RF cable between the Test Ports is of good quality and all external cables (front and rear panels) are connected properly. If this does not solve the problem, it must be corrected by a trained Anritsu Service Engineer.

Non-Ratio Stability:

This test checks the general stabilty of the Non-Ratio channels. Raw data is displayed, stored to memory, then divided by itself resulting in a very smooth RF display at high resolution. The quality of this display is checked after 10 sweeps.

If the test fails, a problem seen in both Test Channels (channels 2 and 3 on the VNA) could be caused by a defective RF cable between the Test Ports. A problem seen on Reference A could be caused by an improperly connected RF cable on the rear panel (373XXC models only). A problem seen on all four channels could be caused by an insufficient warm-up period. If the problem still exists after these checks, it must be corrected by a trained Anritsu Service Engineer.

Transmission Noise and Stability:

This test displays the system noise while measuring the default source power (+5 dBm to –15 dBm, depending on model). A short drift test is also performed, testing both Log Magnitude and Phase. The instrument must not be disturbed during the drift test.

If the test fails, the RF cable between the Test Ports is the most likely cause of failure when the problem appears in both S21 and S12. If only S21 or S12 fails, it must be corrected by a trained Anritsu Service Engineer.

Transmission Sampler Saturation:

This test ensures that the samplers of the Down Conversion (buffer amplifier) section are operating within their linear range by checking at default and reduced VNA power.

If the test fails, interior attenuators on the VNA RF deck may have been removed or be the incorrect values. The sampler(s) may have degraded requiring replacement of the buffer amplifier.

Video IF Bandwidth:

This performs a test on each IF bandwidth filter found on the A4, A3, and A6 PCBs. The operator must perform a Transmission-Only calibration using the calibration kit.

If the test fails in both S21 and S12, the A4 board is suspect. If only S21 fails, the A6 board is suspect. If only S12 fails, the A3 board is suspect.

Reflection Noise:

This is identical to Transmission Noise and Stability except that full reflections are installed on the Test Ports, rather than an RF cable.

If the test fails, the problem must be corrected by a trained Anritsu Service Engineer.

Reflection Sampler Saturation:

This test ensures that the samplers of the Down Conversion (buffer ampifier) section are operating within their linear range by testing with default and lowered source power.

If the test fails, interior attenuators on the VNA RF deck may have been removed or be the incorrect values. The sampler(s) may have degraded requiring replacement of the buffer amplifier.

Port 1 Power:

This test measures the RF power present at Port 1 using the VNA default power setting. An Anritsu ML24XX power meter with the appropriate sensor is required. The power data are taken every few hundred MHz, depending on VNA model, so that the test time is 3 to 5 minutes. Data will be written to a file if the operator specifies to do so.

If the test fails, the results may be improved by performing a Port 1 ALC calibration. If this solves the problem, a Port 2 ALC calibration and Source Lock Threshold Calibrations should also be performed. If the test continues to fail, it must be corrected by a trained Anritsu Service Engineer.

Frequency Accuracy:

This test checks the frequency accuracy of the VNA source. An RF counter with several features is required (see Additoinal Required Equipment at the beginning of this section). A precision 10 MHz reference signal (such as that found on an Anritsu MG369XA series synthesizer) should be connected to the rear panel of the counter. Do not use the 37XXXX 10 MHz OUT as a reference for the counter.

If the test fails, it is likely that the VNA's internal 10 MHz crystal has drifted. If a precision 10 MHz signal is present on the counter, the VNA's 10 MHz crystal can be adjusted. The VNA's 10 MHz crystal is mounted either on the rear panel on the left side frame, or on the top of the A7 PCB. The 10 MHz OUT connector on the rear panel of the VNA provides the access point for monitoring the frequency of the VNA's 10 MHz crystal. After crystal re-adjustment, re-run the Frequency Accuracy test. If the test still fails, the following calibrations will need to be performed (in this order):

1. Source Frequency Cal
2. Port 1 ALC Cal
3. Port 2 ALC Cal
4. Source Lock Threshold Cal

12 Term Cal:

This is a standard OSL measurement calibration, which is required to perform most of the subsequent tests (Step Attenuators, Directivity, Source Match, and System Dynamic Range). The appropriate Anritsu calibration kit with a high density coefficients disk is required. The program selects specific frequencies, using discrete fill, and selects other settings for the calibration required by the System Dynamic Range test. The user must have a female sliding termination if the Directivity or Source Match will be tested.

After the calibration is set up by the program, the operator performs the calibration by connecting the required devices and pressing Enter on the VNA to begin the measurement. After the calibration is complete, the operator selects Continue on the program display and the calibration is saved to the VNA's hard drive. Saving the calibration to the hard drive allows the user to perform other tests (which default the VNA) at any time and recall the calibration as needed.

Step Attenuators:

This will test the accuracy and repeatability of the internal step attenuators. The 12-term calibration must have been performed using the program. This calibration file will be recalled from the VNA's hard drive by the program.

If the test fails, minor failures may occasionally be improved simply by stepping the attenuators up and down for a few minutes to remove oxidation from internal contacts. Major failures of the step attenuators are primarily caused by faults within the attenuators themselves, or perhaps the A8 PCB.

Directivity:

As stated above, the following are required before performing this test:

- Sliding Load calibration performed under control of the 12 Term Cal Test
- Assurance Airline
- Offset Short

Ensure that no RF cables are attached during the test. The assurance airline and offset short are typically available only from Anritsu Service Centers. The test program will use the ripple extraction technique to derive the corrected directivity of both Test Ports. Numeric data may be saved.

If the test fails, ensure that the pin depth of the Test Ports are within specification and that the center pins are not misaligned. The coupler or bias tee for each Test Port is also a possible cause of failure.

Source Match:

The following is required to perform this test:

- Sliding Load calibration performed under control of the 12 Term Cal Test
- Assurance Airline
- Short

Ensure that no RF cables are attached during the test. The assurance airline is typically available only from Anritsu Service Centers. The test program will use the ripple extraction technique to derive the corrected source match of both Test Ports. Numeric data may be saved.

If the test fails, ensure that the pin depth of the Test Ports are within specification and that the center pins are not misaligned. The coupler or bias tee for each Test Port is also a possible cause of failure.

System Dynamic Range/Leakage:

The 12-term calibration test must have been performed before beginning these tests. The Leakage test is performed immediately after the System Dynamic Range test. The specifications of the S21 System Dynamic Range test are guaranteed, while the Leakage test specifications are typical. System dynamic range is tested using the default source power at several CW frequencies (S21 only), all with 10 Hz IF bandwidth. Numeric data may be saved. A swept S21 measurement is also performed. The Leakage test measures the S21 dynamic range of the system with a maximum reflection (0 dB return loss) present at Port 1.

If this test fails, it typically indicates that the Down Conversion module (buffer amplifier) has failed. This can only be replaced by a trained Anritsu Service Engineer.

Send Random Settings:

This test sends random start and stop frequencies and reduces source power in an attempt to expose intermittent failures. If failures occur, details are written to the VNA's service log for evaluation by a trained Anritsu Service Engineer. This test will continue indefinitely until stopped by the operator (using the Escape key or Cancel button) or when 20 errors have occurred.

If the test fails, due to the extreme nature of this test, a very intermittent error may appear (for example, once in several days), which cannot be duplicated by manual testing. If this is the case, it may or may not be prudent (in the view of the user) or successful to attempt a repair. If several errors appear in one day, a significant problem exists and a repair should be performed by an Anritsu Service Engineer.

Chapter 5
System Performance Verification

Table of Contents

Chapter 5
System Performance Verification

5-1 INTRODUCTION

This chapter provides specific procedures to be used to verify that the VNA is making accurate, traceable S-parameter measurements. The operational performance tests described in Chapter 4 should be performed at least once anually, and prior to verifying the system performance test procedures in this chapter.

Please ensure that you have read and fully understand the servicing concepts for the VNA presented in Chapter 1 prior to continuing with this chapter.

The ME7808A broadband system verification is described in Appendix D.

5-2 CALIBRATION AND MEASUREMENT CONDITIONS

The surrounding environmental conditions and the condition and stability of the test port connectors, through-cable, and calibration kit determine the system measurement integrity to a large extent.

These are all user controlled conditions, and as such, should be evaluated periodically for impact on system performance. If these conditions vary significantly with time, the system verification procedures should be performed more often than the recommended annual cycle.

Standard Conditions

The standard conditions specified below must be observed when performing any of the operations in this chapter—both during calibration and during measurement.

- Warm-up Time:
  One hour minimum
- Environmental Conditions:
  Temperature: 23 ±3 deg C
  Relative Humidity: 20% to 50% recommended
- Error Correction:
  Perform software-guided 12-term calibration

Special Precautions: When performing the procedures in this chapter, observe the following precautions:

- Minimize vibration and movement of the system, attached components, and through-cable.
- Clean and check the pin depth and condition of all adapters, through-cable(s), and calibration components.
- Pre-shape the through-cable(s) so as to minimize their movement during calibration and measurement activities.

5-3 MEASUREMENT ACCURACY

The verification procedures described in the following sections verify the published measurement accuracy and measurement traceability* for the VNA.

Verification Software

These procedures use the Anritsu VNA Verification Software, APN: 2300-237, which does not support 1mm W1 connectors, and the NIST traceable impedance transfer standards contained in the appropriate Anritsu Verification Kit. The Standard Conditions and Special Precautions described in Section 5-2 should be observed when performing these procedures.

The appropriate Anritsu Verification Kit to be used for performing these procedures is model dependent, as follows:

- Models 37X47C and below, with Opt 7A**: Verification Kit 3667
- All Models using K Connector test ports: Verification Kit 3668
- 50 and 65 GHz models: Verification Kit 3669B

The impedance transfer standards contained in these kits are:

- 20 dB Attenuation Standard
- 50 dB Attenuation Standard
- 50 Ohm Air Line Standard
- 25 Ohm Mismatch (Beatty) Standard

The verification software performs the following functions:

- It guides the user through a full 12-term calibration of the VNA.
- It guides the user through measurements of the S-parameters of the NIST traceable impedance transfer standards (below).
- It verifies that the measured values are within the specified measurement uncertainty limits.
- It indicates the pass/fail status of the measurements on the display.
- It can also provide a hard copy printout of the measured data, measurement uncertainties, and the impedance transfer standards used.

> ***NOTE***
>
> The total verification uncertainty in these VNA measurements includes the measurement uncertainty of the verification standards and of the VNA measurement uncertainty.

* Traceability to the U.S. National Institute of Standards and Technology (NIST)
** Veriified system performance up to 18 GHz only due to frequency limitation of GPC-7 connector.

Verification Result Determination

The software verification process compares the measured S-parameter data of the impedance transfer standards against the original standard data for those devices that was obtained using the Factory Standard 37XXXC Vector Network Analyzer System (at Anritsu). The factory Standard 37XXXC system is traceable to NIST through the Anritsu Calibration Laboratory's Impedance Standards. These standards are traceable to NIST through precision mechanical measurements, NIST approved microwave theory impedance derivation methods, and electrical impedance comparison measurements.

The quality of the verification results is very dependent on the degree of care taken by the user in maintaining, calibrating, and using the system. The most critical factors are:

- The stability and quality of the devices in the calibration and verification kits.
- The condition of the VNA test port connectors and through cables.
- The pin depths of all connectors and the proper torquing of connections. These same factors also affect the VNA's measurement quality.

Consult the Operating Manuals supplied with the Anritsu Calibration and Verification Kits for proper use, care, and maintenance of the devices contained in these kits.

5-4 VERIFICATION PROCEDURE

The performance verification procedure for the Anritsu 37XXXC VNA is described below. Refer also to the Model 360X/37XXX VNA Performance Verification Software Users Guide, which is located on the CD ROM. This Software Users Guide explains in detail the procedures to be used for the installation and operation of the Verification Software on your computer/controller.

Equipment Required:

- Anritsu 3700 Verification Software, APN: 2300-237
- External computer/controller; refer to Table 1-1
- Anritsu Calibration Kit identical to the Test Port connectors of the VNA
- Anritsu Verification Kit identical to the Test Port connectors of the VNA; refer to Section 5-3
- GPIB cable (Anritsu PN: 2100-2), or equivalent

> ***NOTE***
> Use of non-Anritsu calibration or verification kits is not supported.

Procedure:

Step 1. Using the GPIB cable, connect the external computer/controller to the IEEE 488.2 GPIB Interface port on the VNA's rear panel.

Step 2. Insert the CD ROM into the computer's drive and install the verification software.

Step 3. Follow the directions displayed on the computer screen to perform all tests.

If any failures are indicated, check the connectors of the calibration kit devices and the impedance transfer standards for damage, cleanliness, proper connection, and torquing. These are the most common causes for verification failures.

If failures persist, run all of the tests in the 2300-178 program, described in Chapter 4.

5-5 VNA TRACEABILITY

According to the *International Vocabulary of Basic and General Terms in Metrology (VIM), BIPM, IEC, IFCC, ISO, IUPAC, IUPAP, OIML*, 2nd ed., 1993, definition 6.10, traceability is defined as the property of the result of a measurement or the value of a standard that can be related to *stated references* through an *unbroken chain of comparisons* all having *stated uncertainties.*

The *stated references* are *stated reference standards. Stated* means explicitly set forth in supporting documentation. *Reference standard* is a standard generally having the highest metrological quality available at a given location or in a given organization from which measurements are derived. The *stated references* are usually national or international standards.

The *unbroken chain of comparisons* are the complete, explicitly described, and documented series of comparisons that successively link the value and uncertainty of a result of a measurement with the values and uncertainties of each of the intermediate reference standards to the highest reference standard of which traceability for the result of measurement is claimed.

The *stated uncertainties* are the uncertainties of measurement that fulfill the VIM definition as the parameter and is associated with the result of a measurement that characterizes the dispersion of values that could reasonably be attributed to the measurand. The stated uncertainty is evaluated and expressed according to the general rules given in the *ISO Guide to the Expression of Uncertainty in Measurement*.

The Vector Network Analyzer (VNA) is one of the most modern and accurate measurement tools for microwave and RF applications, but VNA requires calibration to enhance its measurement accuracy. There are many ways to define proper measurement traceability for the VNA in lieu of its system complexity and calibration schemes. Scattering Parameters (S-Parameters) are the most common measurands of the vector network analyzer.

In the chart below, a widely used traceability path for making scattering parameter measurements is presented. The basic elements in this chart include a calibration kit, a VNA, and a verification kit for each user. The calibration kit is characterized and traceable mainly through impedance standards, for example airlines and proper circuit modeling.

The vertical path is a process that is used by most of the manufacturers and primary standards laboratories. It is impractical for regular users to demonstrate the system traceablity before every use; therefore, a verification kit consisting of an airline, mismatch airline, and two fixed attenuators was introduced to perform a routine check for the calibrated system. These components were characterized by their manufacturers or by a standards laboratory, and they have excellent repeatability characteristics.

The horizontal path shows the conventional traceability chain for the verification kit. The stated uncertainty in the verification program comes from three major sources:

- NIST Report
- Anritsu Reference Standards
- Device-under-test

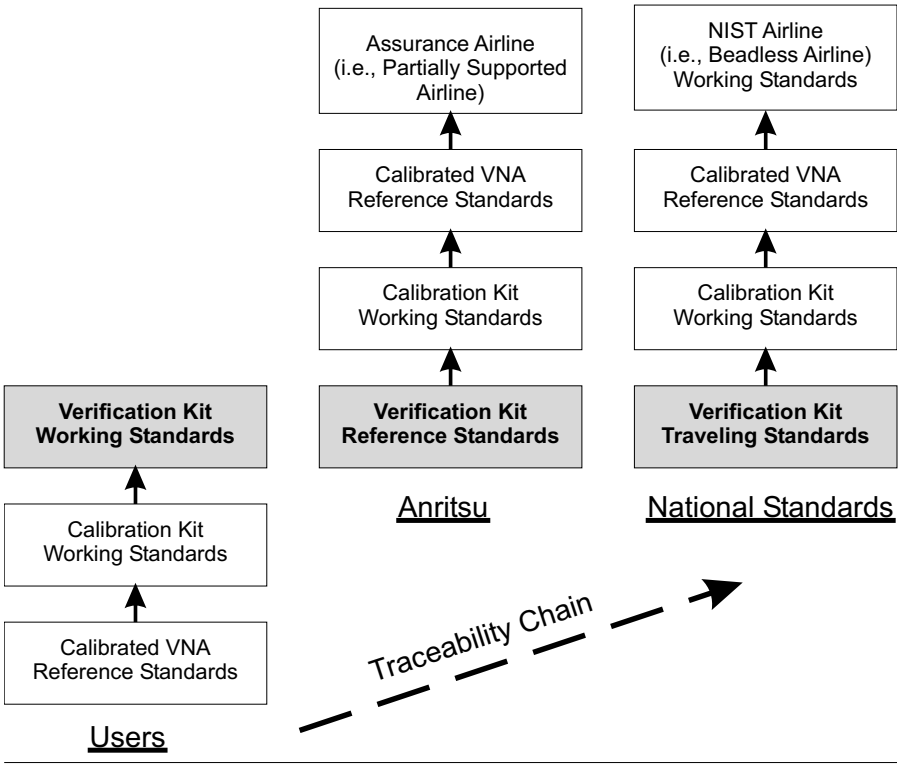


Figure 5-1. *VNA Traceability Chart*

Chapter 6
Adjustments

Table of Contents

Chapter 6
Adjustments

6-1 INTRODUCTION

This chapter contains procedures that are used to restore the calibration of the VNA signal source and the related source lock system assemblies. Use these procedures after various signal source related assemblies have been replaced due to troubleshooting or repair activities.

Please insure that you have read and fully understand the servicing concepts for the VNA presented in Chapter 1 prior to continuing with this chapter.

6-2 LO1 CALIBRATION

This procedure uses the VNA internal diagnostics and calibration menus to adjust the A1 1st LO PCB assembly. Perform this calibation procedure if:

- The A1 PCB is replaced.
- Display of DIAGNOSTICS/TROUBLESHOOTING/LO1 MAIN PHASELOCK VOLTAGE is outside of the limit lines.

Calibration Procedure

Perform the following steps:

Equipment Required

None

> ***NOTE***
> Allow the VNA to warm-up at least 30 minutes prior to performing calibration.

Procedure

Step 1. Press the Option Menu key (Enhancement key group) to display the OPTIONS menu.

Step 2. Select **DIAGNOSTICS** from the menu, then select in sequence: **H/W CALIBRATIONS** | **LO1 CALIBRATION.**

Step 3. Follow the directions displayed on the VNA screen until the calibration is completed.

Post Calibration Actions

After the calibration process is completed, perform the following actions, as appropriate:

If calibration passes:

Save the calibration data to (hard) disk, as follows:

Step 1. Press the Option Menu key (Enhancement key group) to display the OPTIONS menu.

Step 2. Select **DIAGNOSTICS** from the menu, then select in sequence: **H/W CALIBRATIONS | DISK OPERATIONS | SAVE TO HARD DISK | HW_CAL.LO1.**

If calibration fails:

Step 1. Repeat the calibration.

Step 2. If the calibration still fails, proceed to Chapter 7, Troubleshooting.

6-3 LO2 CALIBRATION

This procedure uses the VNA's internal diagnostics and calibration menus to adjust the A2 second LO PCB assembly. Perform this calibation procedure if:

- The A2 PCB is replaced.
- Display of DIAGNOSTICS/TROUBLESHOOTING/LO2 MAIN PHASELOCK VOLTAGE is outside of the limit lines.

Calibration Procedure

Perform the following steps:

Equipment Required

None

> **NOTE**
> Allow the VNA to warm-up for at least 30 minutes prior to performing this calibration.

Procedure

Step 1. Press the Option Menu key (Enhancement key group) to display the OPTIONS menu.

Step 2. Select **DIAGNOSTICS** from the menu, then select in sequence: **H/W CALIBRATIONS** | **LO2 CALIBRATION.**

Step 3. Follow the directions displayed on the VNA screen until the calibration is completed.

Post Calibration Actions

After the calibration process is completed, perform the following actions, as appropriate:

If the calibration passes:

Save the calibration data to (hard) disk, as follows:

Step 1. Press the Option Menu key (Enhancement key group) to display the OPTIONS menu.

Step 2. Select **DIAGNOSTICS** from menu, then select in sequence: **H/W CALIBRATIONS | DISK OPERATIONS | SAVE TO HARD DISK | HW_CAL.LO2.**

If the calibration fails:

Step 1. Repeat the calibration.

Step 2. If the calibration still fails, proceed to Chapter 7, Troubleshooting.

6-4 FREQUENCY CALIBRATION

This procedure uses the internal VNA diagnostics and calibration menus, in conjunction with a suitable frequency counter (refer to Table 1-1), to adjust the signal source frequencies throughout the range of the VNA model being calibrated. Perform this calibration procedure if:

- The Source FM/Lock Linearity test in Chapter 4, Operational Performance Tests, fails.
- Other testing or troubleshooting reveals a possible problem with the signal source frequency accuracy or phase lock loop.
- Any of the following assemblies are replaced:
  - A21A1 Source YIG/Bias
  - A21A2 Source Controller
  - Down Converter
  - YIG Oscillator
  - Switched Filter
- BBRAM chip on the A9 Processor PCB is replaced and the Source Calibration Data was not previously saved on disk (thus data could not be recalled from disk).

Calibration Procedure

Perform the following steps:

Equipment Required

Refer to Table 1-1 for further information about the following equipment:

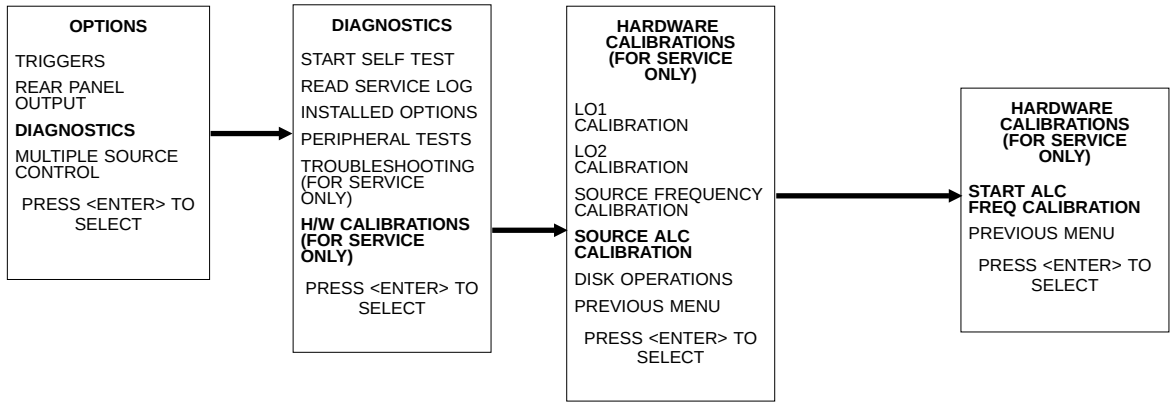
- Anritsu MF241XB Frequency Counter or equivalent EIP brand counter equipped with Band 3 Input and GPIB capability
- RF/Microwave Cable
- GPIB cable (Anritsu 2100-2, or equivalent)

> **NOTE**
> Allow the VNA and Frequency Counter to warm-up for at least 30 minutes prior to performing this calibration.

Procedure

Step 1. Press the Option Menu key (Enhancement key group) to display the OPTIONS menu.

Step 2. Select **DIAGNOSTICS** from the menu, then select in sequence: **H/W CALIBRATION** | **SOURCE FREQUENCY CALIBRATION** (below).



Step 3. Follow the directions displayed on the screen to set-up and connect the frequency counter to the VNA. Refer also to Figure 6-1. Select **START SOURCE FREQ CALIBRATION** from the menu (above).

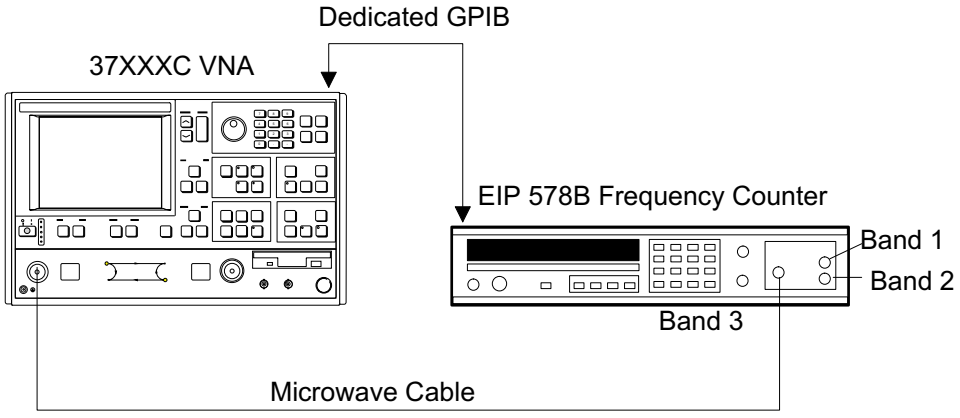


Figure 6-1. *Test Setup for Frequency Calibration*

Step 4. Follow the directions displayed on the VNA screen until the calibration is completed.

Post Calibration Actions

After the calibration process is completed, perform the following actions, as appropriate:

If calibration passes:

Save the calibration data to (hard) disk, as follows:

Step 1. Press the Option Menu key (Enhancement key group) to display the OPTIONS menu.

Step 2. Select **DIAGNOSTICS** from the menu, then select in sequence: **H/W CALIBRATIONS | DISK OPERATIONS | SAVE TO HARD DISK | HW_CAL.FRE.**

If calibration fails:

- Verify that the GPIB cable is connected to the Dedicated GPIB (bottom) connector on the VNA's rear panel.
- Verify that the frequency counter is functioning correctly, the cable is in good condition, and all connections are secure.
- Repeat the calibration. If it still fails, then go to Chapter 7, Troubleshooting.

6-5 RF POWER/ALC CALIBRATION

This procedure uses the VNA's internal diagnostics and calibration menus, in conjunction with a suitable power meter, to adjust the output power level of the signal source throughout the range of the VNA model being calibrated. Perform this calibration procedure if:

- The Port 1 Power test in Chapter 4, Operational Performance Tests, fails.
- Other testing or troubleshooting reveals a possible problem with the RF Power accuracy or the ALC loop.
- Any of the following assemblies are replaced:
  - A21A1 Source YIG/Bias
  - A21A2 Source Controller
  - Down Converter
  - YIG Oscillator
  - Switched Filter
  - Transfer Switch
  - SDM or SQM
  - Coupler
  - Bridge
  - Port 1 Source Step Attenuator
- The BBRAM chip on the A9 Processor PCB is replaced and the Source Calibration Data was not previously saved on disk (thus data could not be recalled from disk).

Calibration Procedure

Perform the following steps:

Equipment Required

Refer to Table 1-1 for further information about the following equipment:

- Anritsu ML24XXA with Version 2.02 or later, with Anritsu Power Sensors MA2474A (use sensor SC6230 for 50 and 65 GHz models)
- GPIB cable (Anritsu 2100-2, or equivalent)

> **NOTE**
> Allow the VNA and power meter to warm-up for at least 30 minutes prior to performing this calibration.

65 GHz Power Sensor Setup Procedure

The Anritsu SC6230 Power Sensor has an internal frequency calibration factors table. The ML24XX meter settings must be changed so that the table will be used for frequencies above 50 GHz. To configure the meter for the new calibration factors table, proceed as follows:

Step 1. Press the Sensor key, then the **Cal Factor** soft key.

Step 2. Press the **More** soft key.

Step 3. Press the **Use Table** soft key. Cursor will start blinking.

Step 4. Press 1, then the **Enter** soft key.

Step 5. Press the System key to exit.

Procedure

Step 1. Press the Option Menu key (Enhancement key group) to display the OPTIONS menu.

Step 2. Select **DIAGNOSTICS** from menu, then select in sequence: **H/W CALIBRATIONS | SOURCE ALC CALIBRATION** (next page).

Step 3. Follow the directions displayed on the screen to set-up and connect the power meter to the VNA. Refer also to Figure 6-2. Select **START ALC CALIBRATION** from the menu.

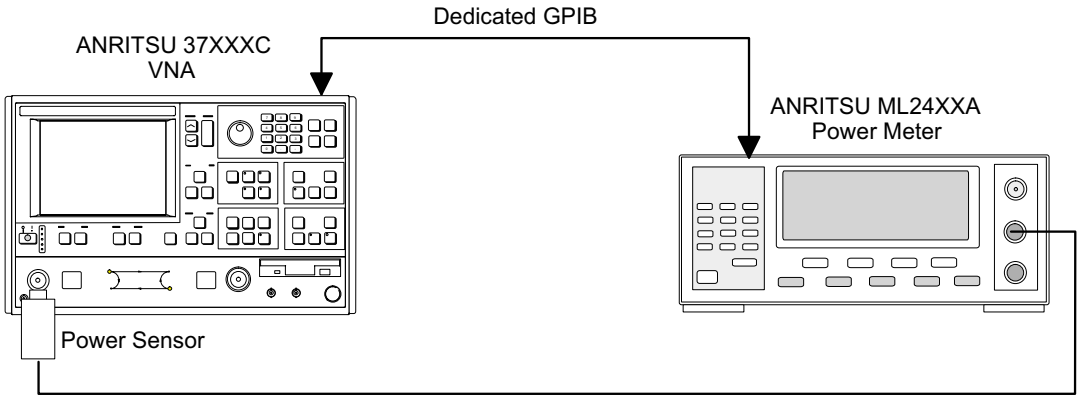


Figure 6-2. *Equipment Set-Up for RF Power / ALC Calibration*

Step 4. Follow the directions displayed on the VNA screen until the calibration is completed.

Step 5. When Port 1 has been calibrated, connect the Power Sensor to Port 2 and Calibrate Port 2.

Post Calibration Actions

After the calibration process is completed, perform the following actions, as appropriate:

If calibration passes:

Save the calibration data to (hard) disk, as follows:

Step 1. Press the Option Menu key (Enhancement key group) to display the OPTIONS menu.

Step 2. Select **DIAGNOSTICS** from the menu, then select in sequence: **H/W CALIBRATIONS | DISK OPERATIONS | SAVE TO HARD DISK | HW_CAL.ALC.**

Perform the Port 1 Power test in Chapter 4, Operational Performance Tests. If the test fails, proceed to Chapter 7, Troubleshooting.

If calibration fails:

- Verify that the GPIB cable is connected to the Dedicated GPIB (bottom) connector on the VNA's rear panel.
- Verify that the power meter and sensor are functioning correctly, the cables are in good condition, and all connections are secure.
- Verify the correct power sensor data exists in the power meter.
- Repeat the calibration. If it still fails, then proceed to Chapter 7, Troubleshooting.

6-6 SOURCE LOCK THRESHOLD

This procedure uses the VNA internal diagnostics and calibration menus to adjust the source lock threshold of the phase-lock loop. Perform this calibation procedure:

- If the Low Power Phase Lock Test (Chapter 4) fails.
- Anytime the Port 1 ALC Calibration is done.
- If the A4 PCB is replaced.
- If the A8 is part number 53971-3 or above and is replaced.
- If the BBRAM chip on the A9 Processor PCB is replaced and the Source Lock Threshold calibration data was not previously saved on disk (that is, data is not available for recall from a floppy disk).
- If the Buffer/Power amp assembly is replaced.

Calibration Procedure

Perform the following steps:

Equipment Required

None

> ***NOTE***
> Allow the VNA to warm-up for at least 30 minutes and perform the ALC calibration (Section 6-5) prior to performing this calibration.

Procedure

Step 1. If recalibrating a 50 or 65 GHz model , install broadband terminations to both ports or install a throughline between ports.

Step 2. Press the Option Menu key (Enhancement key group) to display the OPTIONS menu.

Step 3. Select **DIAGNOSTICS** from the menu, then select in sequence: **H/W CALIBRATIONS | SOURCE LOCK THRESHOLD CALIBRATION.**

Step 4. Follow the directions displayed on the VNA's screen, until the calibration is completed. (If the instrument is a 65 GHz model, the calibration may take over one hour.)

Post Calibration Actions

After the calibration process is completed, perform the following actions, as appropriate:

If calibration passes:

Save the calibration data to (hard) disk, as follows:

Step 1. Press the Option Menu key (Enhancement key group) to display the OPTIONS menu.

Step 2. Select **DIAGNOSTICS** from the menu, then select in sequence: **H/W CALIBRATIONS |DISK OPERATIONS |SAVE TO HARD DISK|HW_CAL.SLT.**

If calibration fails:

Step 1. Repeat the calibration.

Step 2. If the calibration still fails, proceed to Chapter 7, Troubleshooting.

6-7 A8 PCB (65 GHz models only)

This adjustment needs to be performed only on 65 GHz models, if the A8 PCB is part number 49334-3. The adjustments are important to the operation of the VNA above 56 GHz. Improperly adjusted A8 Potentiometers may cause lock failures. Perform these adjustments if:

- The A8 PCB is replaced and the new PCB is part number 49334-3
- The Buffer/Power amp assembly is replaced

Calibration Procedure

Perform the following steps:

Equipment Required

None

> **NOTE**
> Allow the VNA to warm-up for at least 30 minutes.

Procedure

Step 1. Connect a V Throughline (3670V50-2 with FF Adapter) between Ports 1 and 2.

Step 2. Set the VNA to sweep from 50 to 65 GHz.

Step 3. Set RF power to 0 dB (default value).

Step 4. Using Diagnostics menu, view Non-Ratio parameters.

Step 5. View Channel 1 (Ref A) only, and activate Autoscale.

Step 6. Adjust the “RA” potentiometer on top of A8 for the flattest trace display. A small discontinuity at 56 GHz is normal.

Step 7. Perform Step 6 for each of the other three Non-Ratio channels.

6-8 A21A2 ADJUSTMENT (50 and 65 GHz models only)

This adjustment ensures that the correct RF power level will be available to drive the source quadrupler modules (SQMs). Perform these adjustments if:

- The D45244 Switched Filter is replaced
- The A21A2 PCB is replaced
- The C21620 YIG Oscillator is replaced

> ***NOTE***
> Failure to perform this adjustment may result in intermittent operation.

Calibration Procedure

Perform the following steps:

Equipment Required

Refer to Table 1-1 for further information about the following equipment:

- Anritsu ML24XXA with Version 2.02 or later, with Anritsu Power Sensors MA2474 and a 10 dB pad

> ***NOTE***
> Allow the VNA and power meter to warm-up at least 30 minutes prior to performing calibration.

Procedure

Step 1. With power off and the new part installed, disconnect the RF cable from J4 of the Switched Filter.

Step 2. Install Power Sensor (use the 10 dB pad for protection) to Switched Filter J4.

Step 3. Turn on the VNA and set it to 38.1 GHz, CW.

Step 4. Adjust R238 on the A21A2 board for +25 dBm to +27 dBm (+15 dBm to +17 dBm on the power meter display).

Step 5. Remove the pad and sensor and reconnect the RF cable to J4.

Step 6. Perform the procedures in Section 6-4, 6-5, and 6-6 (frequency, ALC and SLT calibrations).

Chapter 7
Troubleshooting

Table of Contents

Many of the troubleshooting procedures presented in this chapter require the removal of instrument covers to gain access to printed circuit assemblies and other major assemblies.

WARNING

Hazardous voltages are present inside the instrument when ac line power is connected. Turn off the instrument and remove the line cord before removing any covers or panels. Trouble shooting or repair procedures should only be performed by service personnel who are fully aware of the potential hazards.

CAUTION

Many assemblies in the VNA contain static-sensitive components. Improper handling of these assemblies may result in damage to the assemblies. ***Always*** observe the static-sensitive component handling precautions described in Chapter 1, Figure 1-2.

Chapter 7
Troubleshooting

7-1 INTRODUCTION

This chapter provides brief information on most failure modes of the 37XXXC instrument family. Only the most basic repairs should be attempted by non-factory-trained technicians. Insufficient care or training will often result in damage to the instrument and cause increased expense and down time. Note that every Anritsu Service Center has factory-trained Service Engineers who can solve all 37XXXC operation problems quickly and reliably, often with warranted repairs.

Before removing the covers of the 37XXXC VNA, be sure that static safety guidelines are followed as detailed in Section 1-12.

7-2 POWER-UP PROBLEMS

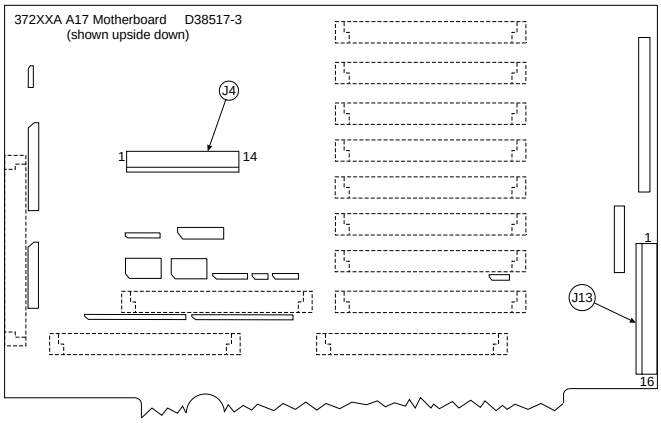
If the instrument is non-functional when power-up is attempted, proceed as follows:

> ***WARNING***
>
> Hazardous voltages are present inside the 37XXXC power supplies. Do not remove the covers of the power supplies, whether side panel mounted or rear panel mounted. The supplies are not repairable. Side mounted supplies are particularly hazardous if the clear plastic safety cover (over the AC input wires) is removed while the power cord is plugged into AC power.

Step 1. Remove the bottom cover as described in Section 8-3.

Step 2. Check the power supply voltages at J4 and J13 of the motherboard. The correct voltages and acceptable AC ripple are listed below:

Table 7-1. *DC Power Supply Voltage Checks*



Connect To:			DC Supply Voltage		AC Ripple and Noise
Conn	Com (Pin)	Meas (Pin)			
J13	8	16	0 Vdc		50 mVpp
J13	8	1	+4.8 Vdc	+1% / –0%	50 mVpp
J4	4	1	+9 Vdc	+5% / –0%	100 mVpp
J4	4	6	+18 Vdc	+10% / –0%	100 mVpp
J4	4	10	–18 Vdc	+10% / –0%	100 mVpp
J4	4	12	+27 Vdc	+5% / –0%	100 mVpp
J4	4	14	–27 Vdc	+5% / –0%	100 mVpp

Figure 7-1. *Location of Connectors for Power Supply Voltage Checks*

Step 3. If the instrument continuously power cycles approximately once per second, it is possible that a PCB or RF component has developed a short. To troubleshoot this type of problem, lift each PCB (one by one) out of its enclosure and try to restart.

Step 4. If a problem PCB is not found, disconnect each RF component by **gently** unplugging the bias connector from the motherboard connector. Do not disconnect RF cables.

Step 5. When the faulty PCB or RF component is disconnected, the VNA will power-up, but other error messages will appear. After the defective assembly is identified, it can then be replaced.

7-3 HARD/FLOPPY DISK AND DISPLAY PROBLEMS

Refer to the following paragraphs for the associated type of problem that you may be having.

Failure To Boot-up from the Hard Disk

If the system does not boot-up from the hard disk, you will need to boot-up the system from the floppy disk and format the hard drive as follows:

> ***WARNING***
> Reformatting the hard drive will erase all saved files. You may continue to boot from floppy disks if deleting these files is not acceptable. A software utility to archive saved 37XXXC files on a PC is available on the Anritsu VNA Software Utilities CD (Anritsu part number 2300-481).

Step 1. Locate the extra set of Operating Software disks that is included with each 37XXXC Operation Manual.

Step 2. Insert Disk 1 into the floppy drive and turn on the VNA.

Step 3. Load the other disks when prompted on the VNA display.

Step 4. After the VNA is operational, the hard drive may be formatted via the **Utility** / General Disk Utilities key sequence. (Note the warning above before formatting).

Step 5. After the drive is reformatted, turn off the 37XXXC, insert Disk 1 in the floppy drive, and load all disks again. The Operating software will be saved automatically to the hard drive.

Step 6. If the problem is not solved using this method, install a new A16 PCB. Detailed instructions are packaged with the replacement A16 PCB.

Floppy Disk Drive Problems

Floppy disk drive problems may be caused by dust buildup, excessive twist of the drive by the mounting bracket, general floppy drive failure, or A13 PCB failure.

If the mounting bracket is a single-part design, slight loosening of the mounting screws may be enough to restore an intermittent drive to normal operation. Depending on instrument serial number, replacement floppy drives from Anritsu may be sent with a 2-part mounting bracket which cannot twist the drive.

Anritsu does not recommend purchasing a replacement drive from sources other than Anritsu since the VNA A13 PCB supports only a limited number of floppy drive types.

Display Problems

The cause of display failures is typically either the A15 PCB, the LCD backlight driver PCB, or the LCD display itself. Replacement part numbers are shown in Chapter 2.

It may be useful to connect an external VGA monitor to the rear panel of the 37XXXC so that the instrument is useable if the LCD display is inoperative. If the external VGA monitor also does not produce a display, then the problem is caused by an A15 PCB failure.

7-4 OTHER BOOT-UP PROBLEMS

As the VNA boots, communication with several subsystems is attempted. If the process stops before boot-up is complete, the last item displayed on the LCD is typically the failing assembly. For example, if the instrument does not boot-up beyond the "Initializing GPIB (A13/A18)" line, then this would indicate a failure of the A13 or A18 PCB.

Error messages having a numerical prefix of 01xx through 21xx indicate which PC board is likely to have failed. For example, "0311 TA IF COMM FAIL" indicates that the A3 PCB is not communicating correctly.

IF calibration failures usually require analysis of the Service Log. See the "Error Messages During Measurements" section below.

7-5 UNDERSTANDING THE SERVICE LOG

The VNA Service Log may be viewed under the **Option Menu** / Diagnostics / Read Service Log key sequence. This log displays general instrument configurations, factory calibration dates, and a list of messages. These messages show instrument problems and other informational messages, such as GPIB programming errors and operator setup problems.

As mentioned in the previous section, error messages having a numerical prefix of 01xx through 21xx indicate which PC board is likely to have failed. For example, "0311 TA IF COMM FAIL" indicates that the A3 PCB is not communicating correctly.

Messages that are labeled "Informational" or those that describe a GPIB command fault or GPIB response time out do not indicate problems with the instrument functionality.

Messages containing the words "Phase Lock Failure" are discussed in Section 7-7.

Messages relating to "warming-up" indicate that the instrument is not source-locking correctly when cold. The 37XXXC is not malfunctioning in this cold condition since the specified warm-up time has not been achieved.

Messages of "RF Unleveled" are frequently caused by the operator setting the RF Source power above Default. To correct this situation, lower the RF power of the Source (**Setup Menu** / Test Signals key sequence). If the message, "RF Unleveled" appears with the Source Power set to 0 dB (Default) or lower, a problem exists with the 37XXXC.

Numerical data with no easily understood identifying labels is of use only to Anritsu Service personnel in the process of PC board repair. PCB repair is a factory-only function.

The following items of information found in the Service Log are highly useful to Service Engineers when troubleshooting errors:

SWP=R or SWP=F

This indicates whether the instrument was in forward or reverse sweep when the problem occurred, and is useful in Phase Lock Failure troubleshooting and RF Unleveled problems.

PWR –x.x

This indicates the Port 1 power setting in dBm. Most 37000C instruments have a Port 1 default power of –7dBm or –15 dBm (shown under the **Setup Menu** / Test Signals key sequence). Default Source power is always labeled as "0 dB".

SYS x.xxxx

This indicates the approximate frequency at which the problem occurred.

<OVL>

This indicates "out-of-range". The internal 37000C DVM was not able to measure the voltage. This is particularly useful information when troubleshooting IF Calibration errors.

7-6 DIAGNOSTIC DISPLAYS

The Diagnostic displays listed below are useful in troubleshooting the 37XXXC problems to the replaceable subassembly level. These displays are found under the **Option Menu** / Diagnostics / Troubleshooting key sequence. Other troubleshooting displays are for component-level troubleshooting by factory technicians only.

- Non-Ratio Parameters
- LO1 Phase Lock Voltage
- LO2 Main Phase Lock Voltage
- Source Linearity Voltage
- GPIB Test (found under the **Diagnostics** / Peripheral Tests menu key sequence)

These displays are identical to those shown automatically in the 2300-178 Operational Tests program described in Chapter 4. Information regarding failures of each test is also included in Chapter 4.

After the desired tests have been performed, the user must select "Finished, Recover from Troubleshooting" or press the Default Program key to exit this mode.

7-7 ERROR MESSAGES DURING MEASUREMENTS

Lock Failure D or DE (60xx)

The Lock Failure D or DE error message will be seen if the rear panel RF cable between a1 IN and a1 OUT is damaged (373XXC models only). If the cable is undamaged and is connected correctly, this problem may occasionally be solved by performing new recalibrations as described in Chapter 6. If the condition persists, the difficult nature of this problem means the 37XXXC should be returned to an Anritsu Service Center where factory-trained Service Engineers and replacement parts are available.

> **NOTE**
> If the error message also contains the prefixes A, B, or C, the corrective action is found in paragraphs farther down in this section.

The following additonal information sources are useful to solve this problem:

- Service Log Information
- Troubleshooting Flowcharts (Figures 7-2 or 7-3)
- Block Diagram of Source Lock Signal path for 50 and 65 GHz models (Figure 7-5)
- DC Voltage Tables 7-2 through 7-4
- Power Meter
- DC Voltmeter
- Oscilloscope
- Spectrum analyzer

Other Lock Failures

Lock Failure A, B...

The “A” indicates a failure of the 10 MHz system clock and all other prefixes and error messages are a result of the 10 MHz clock failure. Replace the A7 PCB.

> **NOTES**
> The 10 MHz crystal found on the rear panel or left side panel is typically no longer available. Different PCBs will be required depending on whether Option 10A is installed.

Lock Failure B, D, E

This indicates that the LO1 (A1 PCB) has failed. Replace the A1 PCB and recalibrate the LO1 as described in Chapter 6.

Lock Failure C, D, E

This indicates that the LO2 (A2 PCB) has failed. Replace the A2 PCB and recalibrate the LO2 as described in Chapter 6.

RF Unleveled

This problem is usually caused by setting the Source power above the instrument capabilities for the frequency range selected. If the Source power is set above default value (0 dB) and reducing the source power causes the message to disappear, the 37XXXC is not malfunctioning.

If the message appears and the Source power is at default power or lower, the 37XXXC is not operating correctly. Performing the Source ALC Calibrations (Chapter 6) may solve the problem. If the problem persists, the difficult nature of this problem means the best solution is to return the VNA to an Anritsu Service Center for repair.

IF Cal Failures (during self-test or measurement)

If only "Test A" is noted on the front panel error message(s) or **<OVL>** is present in the Service Log only in the "A" voltages section, the problem is most likely a fault of the A3 PCB.

If only "Test B" is noted on the front panel error message(s) or **<OVL>** is present in the Service Log only in the "B" voltages section, the problem is most likely a fault of the A6 PCB.

If only "Ref" is noted on the front panel error message(s) or **<OVL>** is present in the Service Log only in the "R" voltages section, the problem is most likely a fault of the A4 PCB.

If there are multiple (usually 3) "IF Cal Failure" error messages on the 37XXXC front panel or **<OVL>** appears in the "A," "B," and "R" voltages sections of the Service Log, the problem is most likely a failure of the 10 MHz internal time base. Replace the A7 PCB.

Trace Data-Data Points Overflows...

If this message appears (often many instances will appear on the display at the same time), the problem is usually caused by turning on Smoothing in Time Domain. It may be difficult to remove this error message.

If the 37XXXC front panel keyboard is responding, press the Default Program key. Do not engage smoothing while in Time Domain, or upgrade the system software to version 4.00 or above to prevent this error.

If the front panel keyboard does not respond, power cycle the VNA. During bootup, while the instrument displays "Initializing Software...," press the "0" key 2 or 3 times quickly. This will perform a master reset and the VNA will beep 5 times. After boot-up, reload the coefficients disks from all Calibration Kits. Upgrade the system software to version 4.00 or above to prevent this error.

7-8 MEASUREMENT ACCURACY PROBLEMS

S11 and S12 Data is Inaccurate

Ensure that the RF cable mounted to the VNA rear panel between the b1 IN and b1 OUT connectors is connected and undamaged (373XXC models only).

All Data on All Channels is Greatly Inaccurate

Check all of the calibration kit components and all of the measurement cables for damage.

For 50 and 65 GHz models, refer to the block diagram of the Test Signal paths (Figure 7-4). Also, refer to Tables 7-2 through 7-4. Use of a spectrum analyzer, oscilloscope, and DVM will be useful to find the defective assembly.

The instrument may be in an unusual setup, such as a non-phase-locked "Receiver" mode, or the internal memory buffers may have corrupt data due to a process that was started, but incorrectly terminated. To correct this problem, press the **Default Program** key, then the 0 key to return the instrument to normal measurement condition and clear the memory buffers. Reload all of the coefficient disks from the Calibration Kits.

Excessive Ripple in the Display of Low-Loss Devices

Ensure that all of the calibration coefficients are loaded into the VNA. The coefficients may have been erased by a **Default Program** / 0 reset.

The calibration selected should be 12 Term. Also perform the calibration using sliding terminations rather than broadband fixed terminations.

Insufficient System Dynamic Range

Select "Include Isolation" and increase the RF Source power during the calibration setup.

Before measuring the Isolation Devices during the calibration, press the Video IFBW key and select "10 Hz Minimum".

During the measurement of the DUT, select "10 Hz IF Bandwidth."

Perform the automated "System Dynamic Range" test found in the 3700Test Program (described in Chapter 4). If this test fails, the problem is typically solved by replacement of the buffer amplifier.

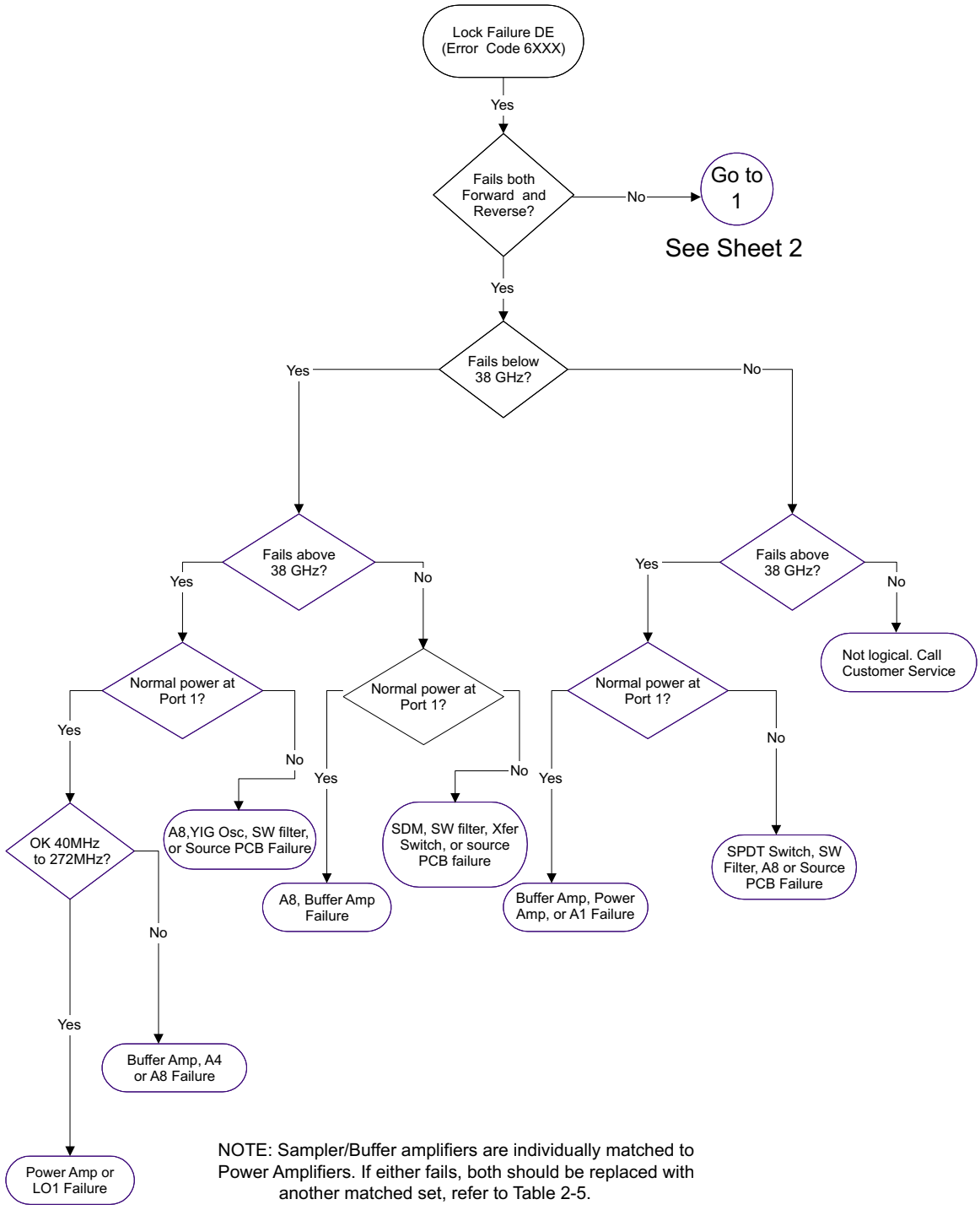


Figure 7-2. *Error Code DE Lock Failure Troubleshooting (50 and 65 GHz models only) (1 of 3)*

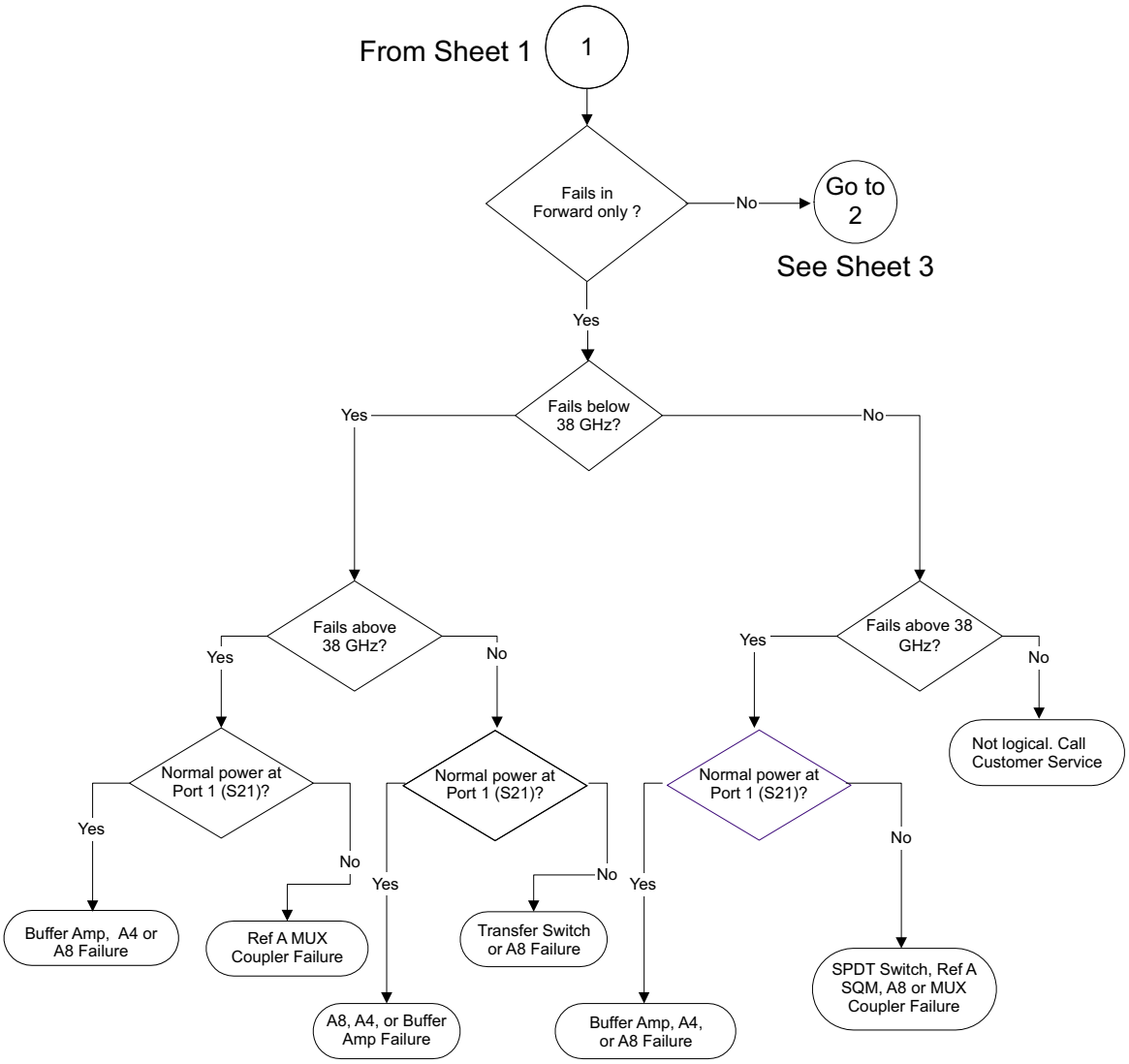


Figure 7-2. *Error Code DE Lock Failure Troubleshooting (50 and 65 GHz models only) (2 of 3)*

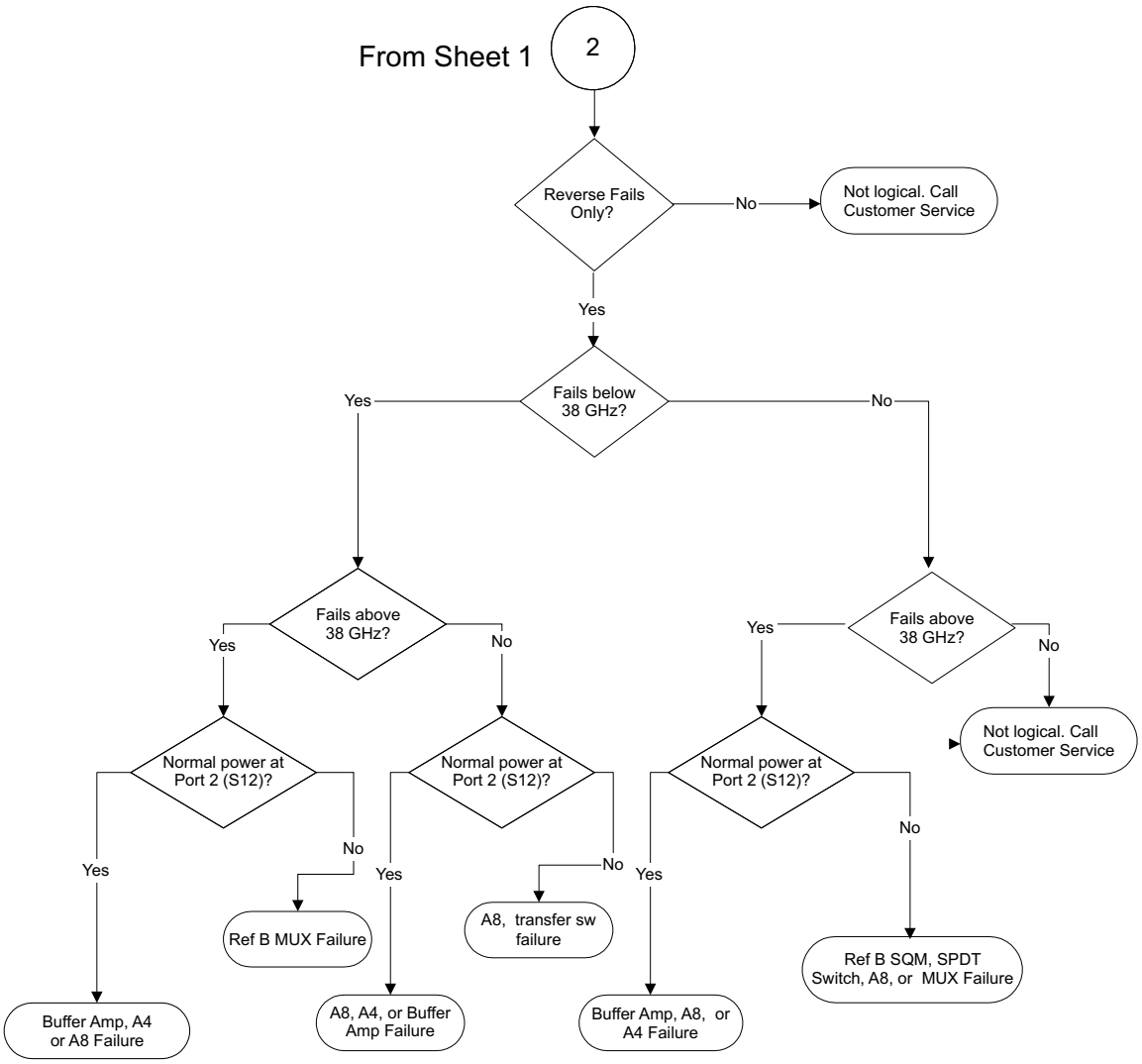


Figure 7-2. *Error Code DE Lock Failure Troubleshooting (50 and 65 GHz models only) (3 of 3)*

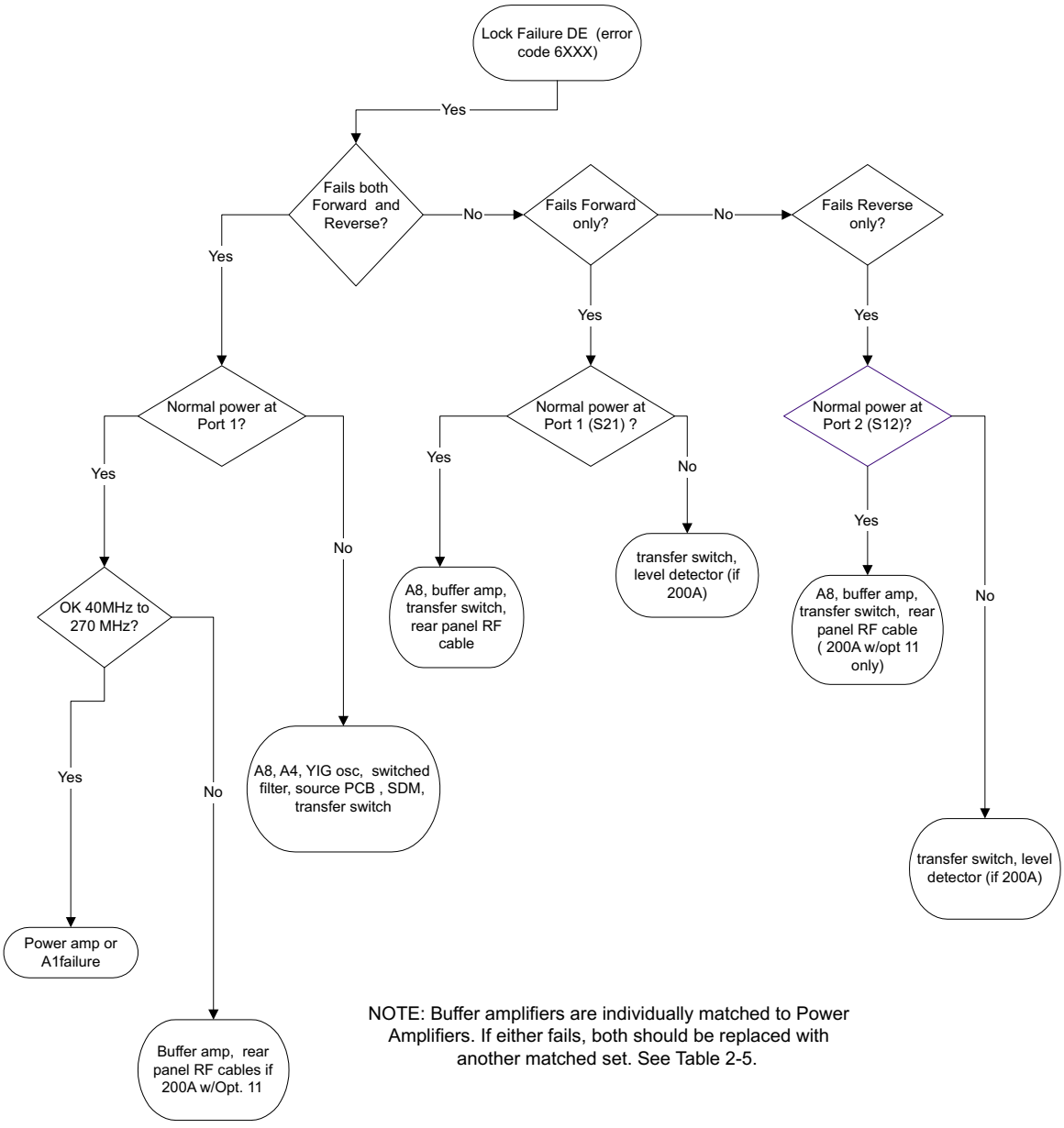


Figure 7-3. *Error Code DE Lock Failure Troubleshooting (40 GHz and lower models only) (1 of 1)*

Table 7-2. *Typical Reference Signal Values in dBm (50 and 65 GHz models only)*

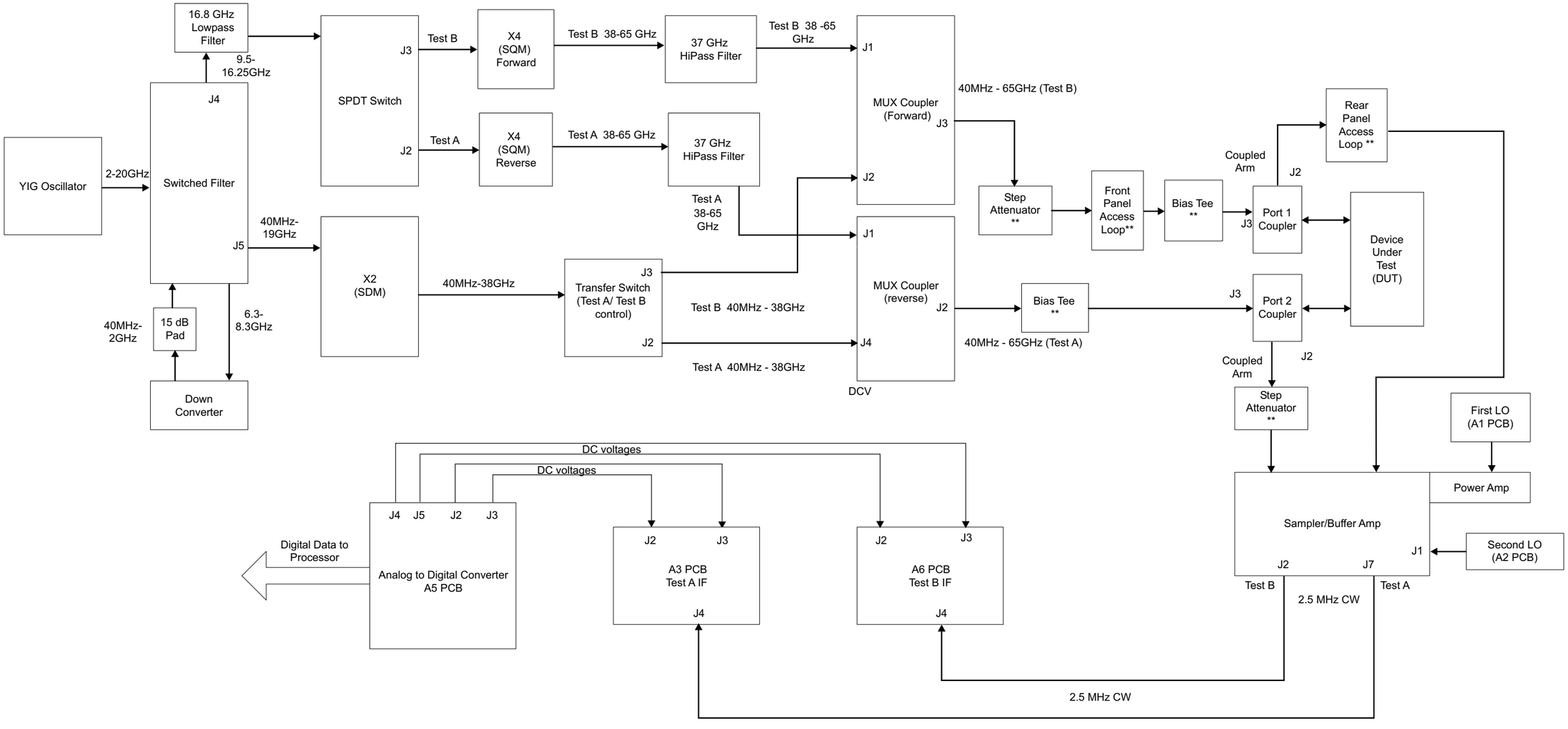
Frequency	SQM In	SDM Out	MUX J4	MUX J1	Buffer Amp In
20 GHz	NA	+18	+6	NA	–26
37 GHz	NA	+20	+4	NA	-28
40 GHz	+19	NA	NA	+14	-28
50 GHz	+18	NA	NA	+14	-23
65 GHz	+16	NA	NA	+10	-26

Table 7-3. *Typical Transfer Switch (D27030) Voltages (CW, Single Channel Display, 50 GHz and above models only)*

Wire Color	Below 38 GHz		Above 38 GHz	
	S21	S12	S21	S12
Brown	+2.0	–3.3	+2.0	+2.0
Black	–6.7	+1.6	+1.6	+1.6
White	+1.6	–6.8	+1.6	+1.6
Grey	–3.3	+2.0	+2.0	+2.0

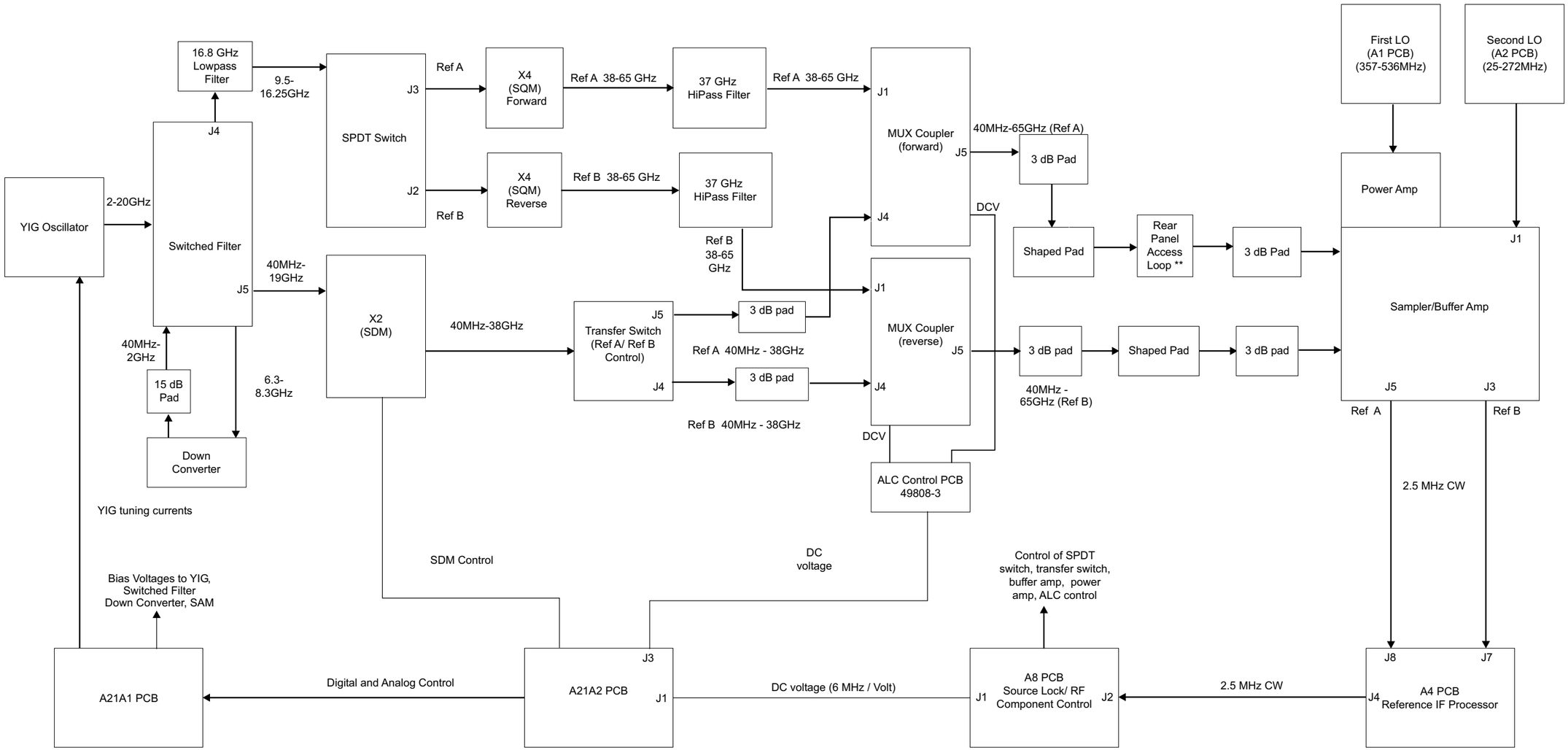
Table 7-4. *Typical SPDT Switch (part number 29855) Voltages (CW, Single Channel Display, 50 GHz and above model only)*

Wire Color	Forward	Reverse
Brown	+1.2	–3.7
Grey	–3.7	+1.2



NOTE: Buffer amplifiers are individually matched to Power Amplifiers.
If either fails, both should be replaced with another matched set (refer to Table 2-5).
** Indicates not present on model 37297C or 37277C

Figure 7-4. *50 and 65 GHz Model Test Signal Path Diagram*



NOTE: Buffer amplifiers are individually matched to Power Amplifiers.
If either fails, both should be replaced with another matched set
(refer to Table 2-5).
** Indicates not present on model 37297C or 37277C

Figure 7-5. *50 and 65 GHz Model Source Lock Signal Path Diagram*

Chapter 8
Removal and Replacement Procedures

Table of Contents

Chapter 8
Removal and Replacement Procedures

8-1 INTRODUCTION

This chapter provides procedures for removing and replacing the 37XXXC field exchangeable assemblies and components. When using these procedures, please observe the warning and caution notices below.

> ***WARNING***
> Hazardous voltages are present inside the instrument when ac line power is connected. Turn off the instrument and remove the line cord before removing any covers or panels.

> ***CAUTION***
> Many assemblies in the VNA contain static-sensitive components. Improper handling of these assemblies may result in damage to the assemblies. *Always* observe the static-sensitive component handling precautions described in Chapter 1, Figure 1-2.

8-2 EQUIPMENT REQUIRED

All procedures in this chapter require the use of either a #1 or #2 size Phillips type screw driver. Most procedures require the use of a 5/16 inch wrench and the Anritsu 01-201 (8 inch/pounds) Torque Wrench.

8-3 COVERS

Adjustment and troubleshooting operations require removal of the top cover. Replacement of some VNA assemblies and parts require removal of all covers. The following procedures describe this process.

> ***NOTE***
> It is only necessary to loosen the VNA handle assemblies to remove the top, bottom, or side covers. However, if the front panel is to be removed, remove the handle assemblies at this time.

Preliminary:

❑ Switch the VNA power **off**. Remove the power cord.

Procedure:

Step 1. Loosen (or remove) the right and left handle assemblies, as follows:

- Place the VNA on its top (bottom-side up).
- Loosen/remove the screws at the sides of the handle assemblies.
- If removing handles, pull them away from unit and set aside.

> ***CAUTION***
> The green headed screws have Metric threads.

Step 2. To remove the top cover:

- Place the VNA in normal (top-side up) position.
- Remove the feet from the two top corners at the rear of the VNA (Figure 8-1).
- Remove the center screw from the rear of the top cover.
- Lift and slide the top cover away from the VNA.

Step 3. To remove the bottom cover:

- Place the VNA on its top (bottom-side up).
- Remove the feet from the two bottom corners at the rear of the VNA.
- Remove the center screw from the rear of the bottom cover.
- Lift and slide the top cover away from the VNA.

Step 4. To remove the left cover:

- Place the VNA on its right side (monitor down).
- If not already done, remove the feet from the two left-side corners at the rear of the VNA.
- Remove two center screws from the left cover.
- Remove the center screw from rear of the left side cover.
- Lift and slide the side cover away from the VNA.

Step 5. To remove the right cover:

- Place the VNA its left side (monitor up).
- If not already done, remove the feet from the two right-side corners at the rear of the VNA.
- Remove the center screw from the rear of the right side cover.
- Remove the center screw from the rear of the right side cover.
- Lift and slide the side cover away from the VNA.

To replace the instrument covers, perform the steps above in the reverse order.

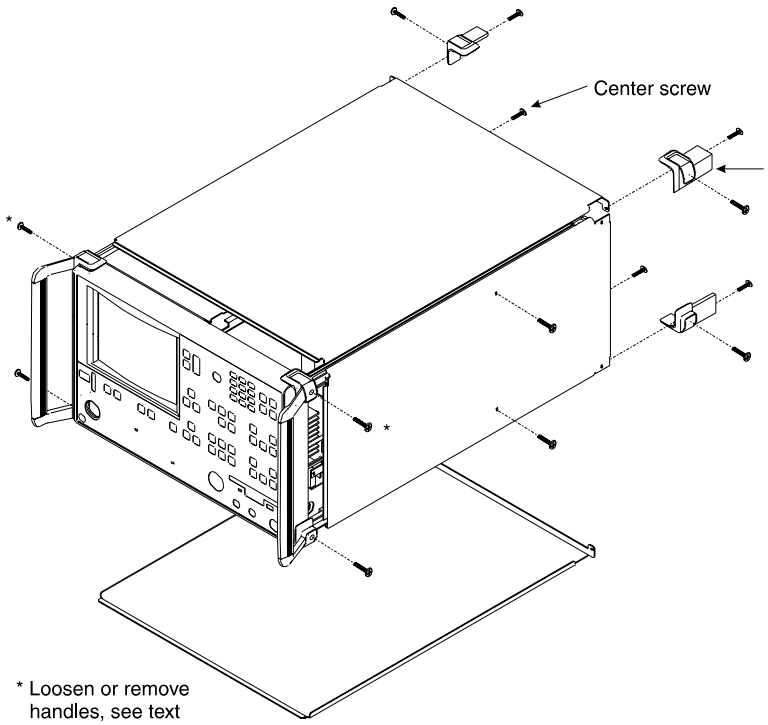


Figure 8-1. *Exploded View of 37XXXC Chassis Covers*

8-4 A1 TO A9 AND A13 TO A16 PCBS

This section provides instructions for removing and replacing the A1 through A9 and A13 through A16 PCBs, which are located underneath the covers of the large and small card-cages, respectively.

Preliminary:

- ❑ Switch the VNA power to **off**. Remove the power cord.

Remove the top cover (Section 8-3).

A1 to A9 PCBs

Procedure:

Step 1. Place the VNA in normal (top-side up) position.

Step 2. Remove the two screws that secure the large card-cage cover (Figure 8-2).

Step 3. Remove the large card-cage cover and set it aside.

Step 4. Lift up on the edge tabs of the selected PCB(s) and lift straight up.

To replace the PCB(s) and covers, perform the steps above in the reverse order.

A13 to A16 PCBs

Procedure:

Step 1. Place the VNA in normal (top-side up) position.

Step 2. Remove the two screws that secure the large card-cage cover (Figure 8-2).

Step 3. Remove the large card-cage cover, then remove the small card-cage cover and set aside.

Step 4. Lift up on the edge tabs of the selected PCB(s) and lift straight up.

To replace the PCB(s) and covers, perform the steps above in the reverse order.

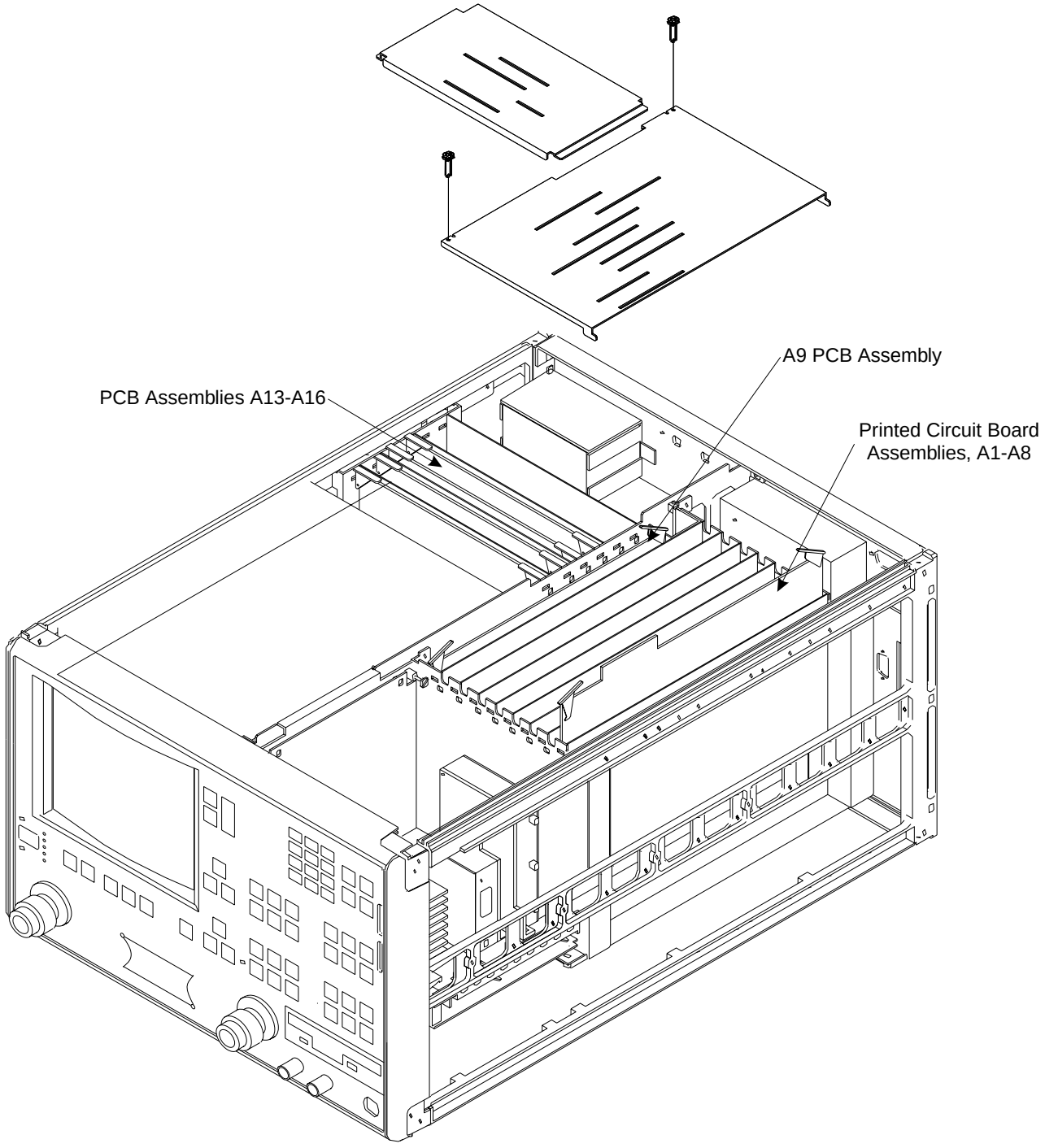


Figure 8-2. *A1-A9 and A13-A16 PCB Assemblies Removal Diagram*

8-5 A24 VME BUS TERMINATOR PCB

This section provides instructions for removing and replacing the A24 VME Bus Terminator PCB assembly.

Preliminary:

- ❑ Switch VNA power **off**. Remove the power cord.
- ❑ Remove bottom cover (Section 8-3).

Remove/Replace Procedure

Step 1. Place the VNA on its top (bottom-side up).

Step 2. Locate the A24 PCB assembly (Figure 8-5). Unplug A24 PCB assembly from the A17 Motherboard PCB by gently pulling straight up on each side.

> ***CAUTION***
>
> Be careful not bend or disturb the hard coax lines located near the right edge of the A24 PCB.

8-6 FRONT PANEL ASSEMBLY

This section provides instructions for removing and replacing the VNA Front Panel assembly.

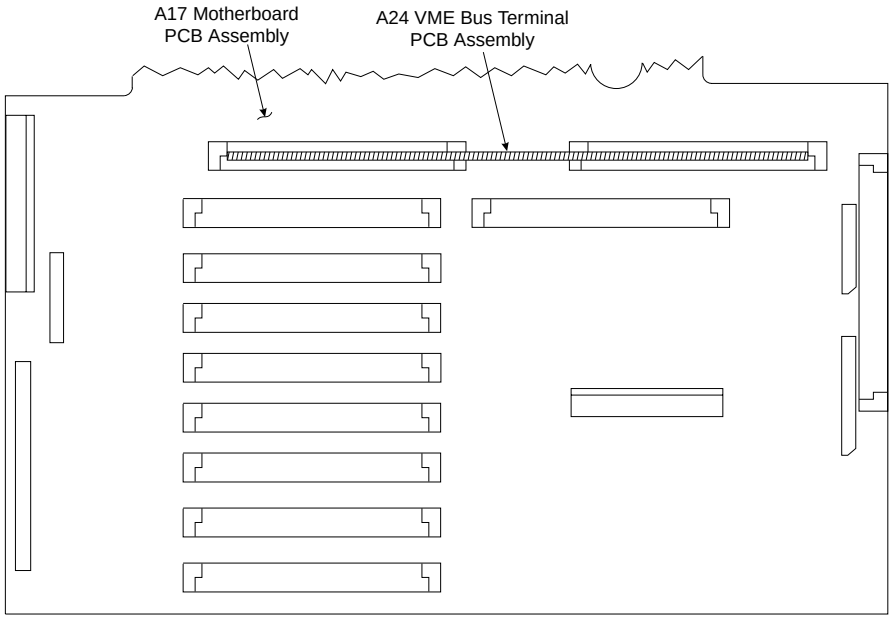


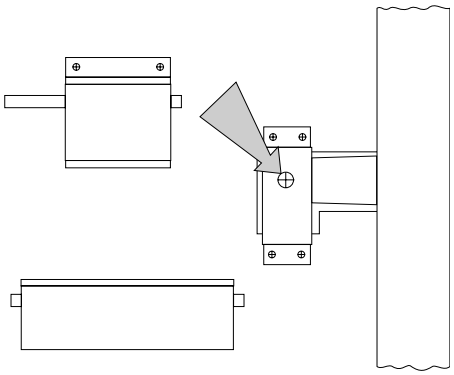
Figure 8-3. *Location of the A24 VME Bus Terminator PCB Assembly*

Equipment Required:

- ❑ Open-end wrench, 1 inch

Preliminary:

- ❑ Switch the VNA power to **off** and remove the power cord.
- ❑ Remove the handle assembles and all covers (Section 8-3).



Remove/Replace Procedure:

Step 1. Place the VNA in normal (top-side up) position.

Step 2. Remove the four corner screws and the top center screw that secure the front panel assembly to the chassis (see Figure 8-4).

Step 3. Place the VNA on its top (bottom-side up).

Step 4. Remove the screw that fastens the front panel casting extension lip to the Test Set Module tray. (See diagram at left.)

Step 5. Using a 1 inch open-end wrench, remove the nuts and washers that secure the Port 1 and Port 2 couplers/bridges to the front panel casting.

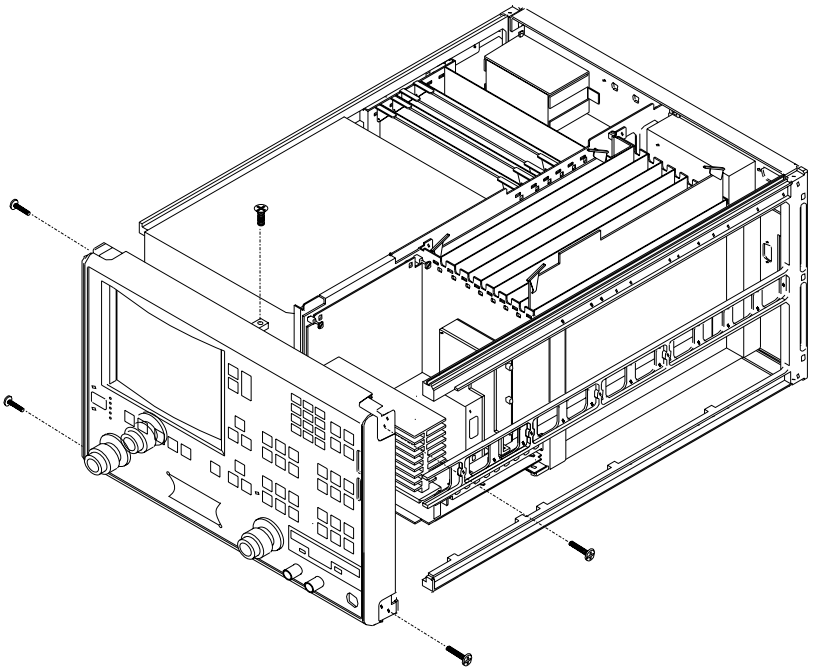


Figure 8-4. *Removal of Front Panel Assembly*

Step 6. Locate the cable from the front panel Power switch to connector J20 on the A17 Motherboard PCB. Disconnect the cable at A17, J20 end.

Step 7. Locate the cable from the front panel Keyboard interface connector to connector J16 on the A17 Motherboard PCB. Disconnect the cable at A17, J16 end.

Step 8. Locate the cables from the front panel Bias Input BNC connectors to connector P2 on the A18 Rear Panel PCB. Disconnect the cables at A18, P2 end. (A18, P2 is the connector nearest to the bottom lip of the rear panel.)

Step 9. Gently pull the front panel assembly several inches away from chassis. Locate the cable from the A17 Motherboard PCB to connector J1 on the A20 Front Panel PCB. Disconnect the cable at A20, J1 end.

Step 10. Separate the bias input cables (Step 8) from the cable harnesses as necessary for removal. Pull the front panel assembly free and set it aside.

To replace the front panel assembly, perform the steps above in the reverse order.

8-7 LIQUID CRYSTAL DISPLAY (LCD)

This section provides instructions for removing and replacing the internal LCD assembly. This LCD display needs no periodic maintenance. Its life is estimated to be 50,000 hours by the manufacturer. Contact Anritsu Company for more information.

> ***CAUTION***
> Anritsu advises to NOT remove the front panel of ***50 and 65 GHz instruments*** to perform this repair, due to the likelihood of damage to RF components and cables.

Preliminary:

- ❑ Switch the VNA power to **off** and remove the power cord.
- ❑ Remove the right handle, top and bottom covers, and right side cover (Section 8-3).

Remove/Replace Procedure:

Step 1. Turn the instrument upside-down and remove the W87 cable (20 GHz and below units), or the W81 cable (40 GHz units), or the W179 and W180 cables (50 and 65 GHz units).

Step 2. Return the instrument to the normal operating position and, using steps below, remove the Source Module.

Step 3. Disconnect the two cables from the A21A2 PCB.

Step 4. Loosen the two captivated metal screws that attach the A21A2 bracket to the instrument frame.

Step 5. Disconnect the ribbon cable from the Frequency Converter.

Step 6. If the instrument is a 50 or 65 GHz model, loosen the W206 cable from the Switched Filter.

Step 7. Remove the three screws on the right side of the instrument frame from the Source Module frame.

Step 8. Lift the Source Module up, and remove by tipping the top to the right to clear the instrument frame.

Step 9. Disconnect the small connector from the LCD display, by prying very carefully with flatblade screwdriver.

Step 10. Unplug the (unlabeled) connector holding the red and white wires from the top of the LCD EMI shield.

Step 11. Remove the four screws from the EMI shield and the LCD to the front panel.

Step 12. Set aside the EMI shield and remove the LCD display.

Install the new display by reversing the above order.

> ***NOTE***
> All RF connections (at the Wxxx cables) should be torqued to 8 in/lbs using the 01-201 wrench from a Calibration Kit. Check for RF discontinuities and other failures using the first six to eight tests in the 2300-178 program.

8-8 FLOPPY DISK DRIVE

Replacement instructions are included with the replacement floppy disk drive.

8-9 REAR PANEL ASSEMBLY

This section provides instructions for removing and replacing the Rear Panel Assembly.

Equipment Required (Option 11 only):

- ❑ Connector torque wrench ($\frac{5}{16}$ inch), Anritsu Model 01-201, or equivalent.

Preliminary:

- ❑ Switch the VNA power to **off** and remove the power cord.
- ❑ Remove all covers (Section 8-3).

Remove/Replace Procedure:

Step 1. Place the VNA in normal (top-side up) position.

Step 2. Remove the three screws on each side of the chassis that fasten to the rear panel assembly. See Figure 8-5.

Step 3. Remove the two screws located near top and middle of rear panel (near fan-mounting screws).

Step 4. Locate cable from the rear-panel 10 MHz Ref In BNC connector to connector J2 of A7 PCB. Disconnect at A7, J2 end. (Pull up gently to disconnect.)

Step 5. Locate cable from the rear-panel 10 MHz Ref Out BNC connector to connector J3 of A7 PCB. Disconnect at A7, J3 end.

Step 6. Locate cable from the rear-panel Ext Anlg In BNC connector to connector J1 of A5 PCB. Disconnect at A5, J1 end.

Step 7. Place the VNA on its right side (monitor down).

Step 8. Locate the cables from the rear-panel Ext Trigger and Ext Anlg Out BNC connectors to connector P13 of the A18 Rear Panel PCB. Disconnect at A18, P13 end. (A18, P3 is the fourth connector away from the rear panel bottom lip.)

Step 9. Disconnect the large ribbon cable from connector P1 of the A18 PCB at motherboard connector J12.

Step 10. Disconnect the two cables from the Power Supply Module at motherboard connectors J4 and J13.

Step 11. If the VNA is equipped with Option 11, Reference Loop Extension Cables:

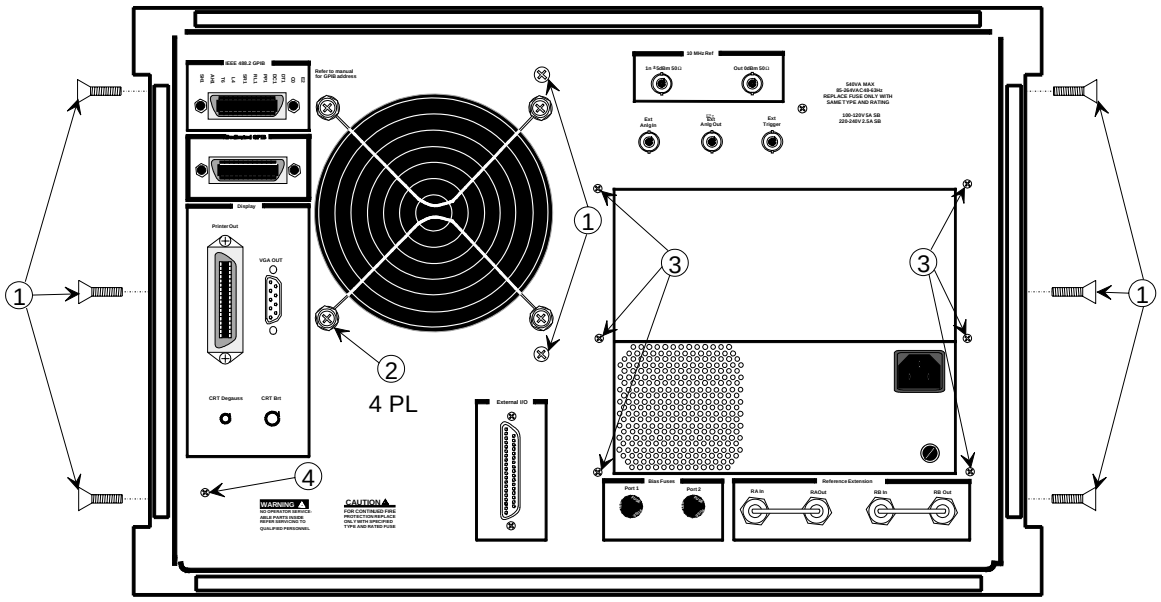
- Using a 5/16 inch wrench, disconnect the external cable Loops from the rear panel connectors.
- Using a 5/16 inch wrench, disconnect the semi-rigid coaxial lines W141 and W145 at the inside of the rear panel.

Step 12. If the VNA is equipped with Option 10, High Stability Time Base:

- Locate the output cable from the high stability oscillator assembly (mounted above Power supply Module) to connector J1 of A7 PCB. Disconnect at A7, J1 end.
- Locate power cable from the high stability oscillator assembly to A17 Motherboard connector, J18. Disconnect at A17, J18 end.

Step 13. Place the VNA in normal (top-side up) position. Gently pull rear panel assembly away from chassis and lay flat on work surface. Remove cables from cable harnesses, as required.

To replace the Rear Panel Assembly, perform the steps above in the reverse order.



①Rear Panel Assembly screws (par 8-11)
②Fan Assembly screws (par 8-12)
③Power Supply Assembly screws (par 8-13)
④A18 Rear Panel PCB screw (par 8-14)

Figure 8-5. *Location of Mounting Screws for Rear Panel Assemblies*

8-10 FAN ASSEMBLY

This section provides instructions for removing and replacing the Rear Panel Fan Assembly.

Preliminary:

- ❑ Switch the VNA power to **off** and remove the power cord.
- ❑ Remove all covers (Section 8-3).
- ❑ Remove the Rear Panel (Section 8-9).

Remove/Replace Procedure:

Step 1. Place the Rear Panel Assembly on the work surface with the A18 Rear Panel PCB up.

Step 2. Disconnect the two conductor fan power cable at connector P6 of the A18 PCB.

Step 3. Turn the Rear Panel Assembly over, and remove the four screws that fasten the fan guard and fan assembly to the rear panel. See Figure 8-5.

Step 4. Remove the fan guard and separate the fan from the rear panel.

To replace the Rear Panel Fan Assembly, perform the steps above in the reverse order.

8-11 POWER SUPPLY MODULE

This section provides instructions for removing and replacing only the rear panel mounted Power Supply Module. Replacement instructions for the left side mounted Power Supply Module are included with the replacement supply kit.

Preliminary:

- ❑ Switch the VNA power to **off** and remove the power cord.
- ❑ Remove all covers (Section 8-3).
- ❑ Remove the Rear Panel (Section 8-9).

Remove/Replace Procedure:

Step 1. Place the Rear Panel Assembly on the work surface with the Power Supply Module down.

Step 2. Remove the six screws from the rear panel that fasten it to the left and right edges of the Power Supply Module (see Figure 8-5). Gently separate the two units.

To replace the Power Supply Module, perform the steps above in the reverse order.

8-12 A18 REAR PANEL PCB

This section provides instructions for removing and replacing the A18 Rear Panel PCB assembly.

Equipment Required:

- ❑ Nut Driver, 9/32 inch
- ❑ Nut Driver, 3/16 inch

Preliminary:

- ❑ Switch the VNA power to **off** and remove the power cord.
- ❑ Remove all covers (Section 8-3).
- ❑ Remove the Rear Panel (Section 8-9).

Remove/Replace Procedure:

Step 1. Place the Rear Panel Assembly on the work surface with the A18 Rear Panel PCB up.

Step 2. Disconnect the two-conductor fan power cable at connector P6 of the A18 PCB.

Step 3. Disconnect the wiring for the rear panel Bias Fuses at connector P4 of the A18 PCB.

Step 4. Turn the Rear Panel Assembly over. Remove the screw located at lower left corner of the rear panel that fastens the A18 PCB to the Rear Panel Assembly (see Figure 8-5).

Step 5. Using a 9/32 inch nut driver, remove the standoffs that fasten the IEEE 488.2 GPIB and Dedicated GPIB connectors to the rear panel.

Step 6. Using a 3/16 inch nut driver, remove the standoffs that fasten the Printer Out, VGA Out, and External/IO connectors to the rear panel. Set standoffs aside for re-use.

Step 7. Carefully separate the A18 PCB from the rear panel.

To replace the A18 Rear Panel PCB assembly, perform the steps above in the reverse order.

8-13 TEST SET MODULE ASSEMBLIES

The following sections provide instructions for removing and replacing the RF/microwave components that comprise the Test Set Module (excluding 50 and 65 GHz models).

Equipment Required:

- ❑ Connector torque wrench (5/16 inch), Anritsu Model 01-201, or equivalent.
- ❑ Open-end wrench, 1 inch

> ***CAUTION***
>
> Throughout these procedures, *always* use the 5/16 inch connector torque wrench for connecting the Test Set Module semi-rigid coaxial lines and RF/microwave components. Use of improper tools may damage the connectors, resulting in degraded instrument performance.

Preliminary:

- ❑ Switch the VNA power to **off** and remove the power cord.
- ❑ Remove all covers (Section 8-3).

Transfer Switch

Use the following procedure to remove/replace the Transfer Switch, which is common to all VNA models.

Procedure:

Step 1. For all models below 40 GHz: disconnect the semi-rigid coaxial line W87 from the input connector of the Transfer Switch. See Figure 8-11 for component locations. (Wxx numbers are affixed to semi-rigid cables.)

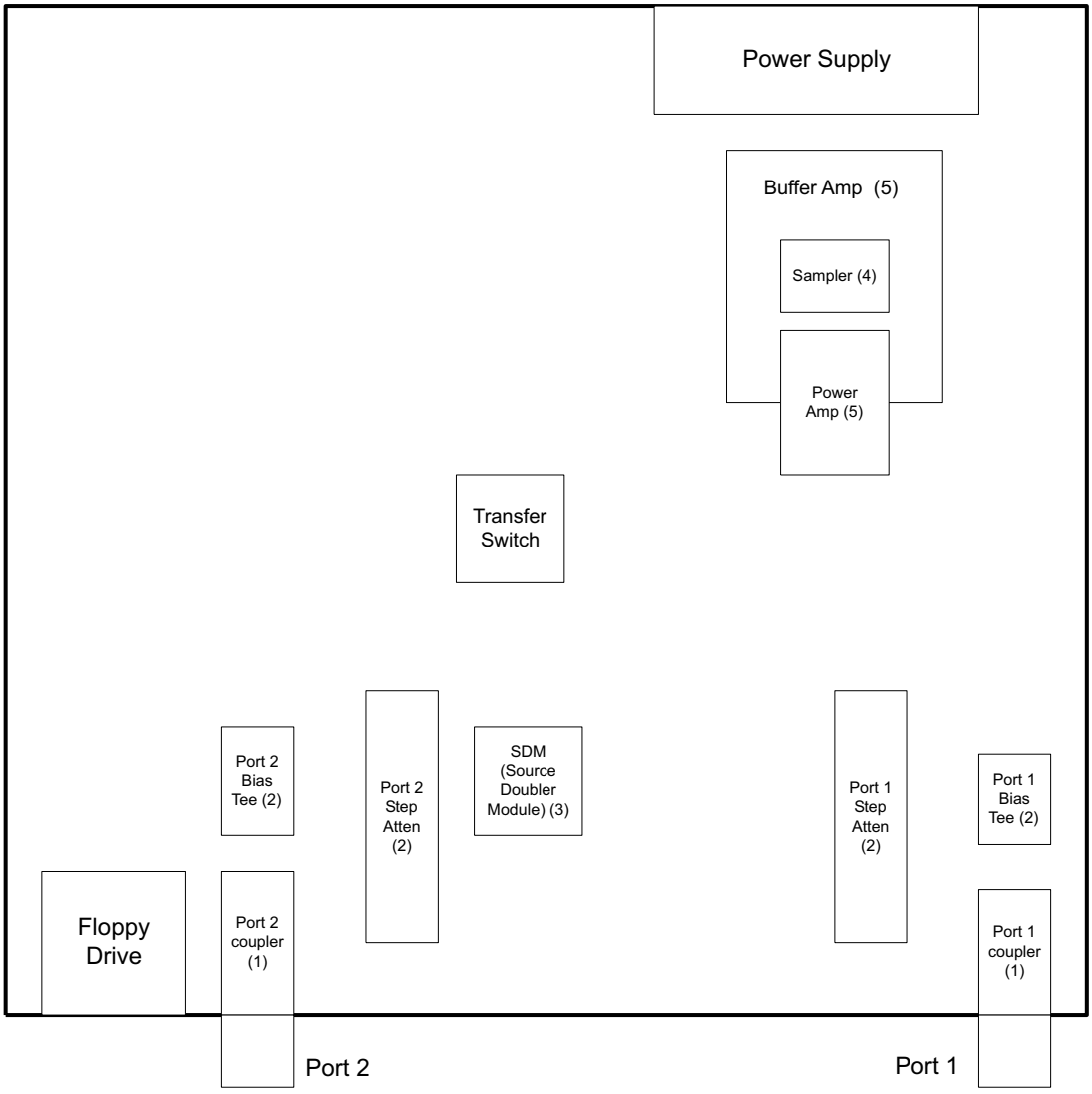
For 40 GHz models: loosen the two screws that fasten the Transfer Switch mounting plate to the test set tray before disconnecting the semi-rigid coaxial line (W80).

Step 2. Disconnect the Transfer switch.

Step 3. Carefully flex (do **not** bend) the semi-rigid-coaxial lines to gain access to the lower connectors of the Transfer Switch.

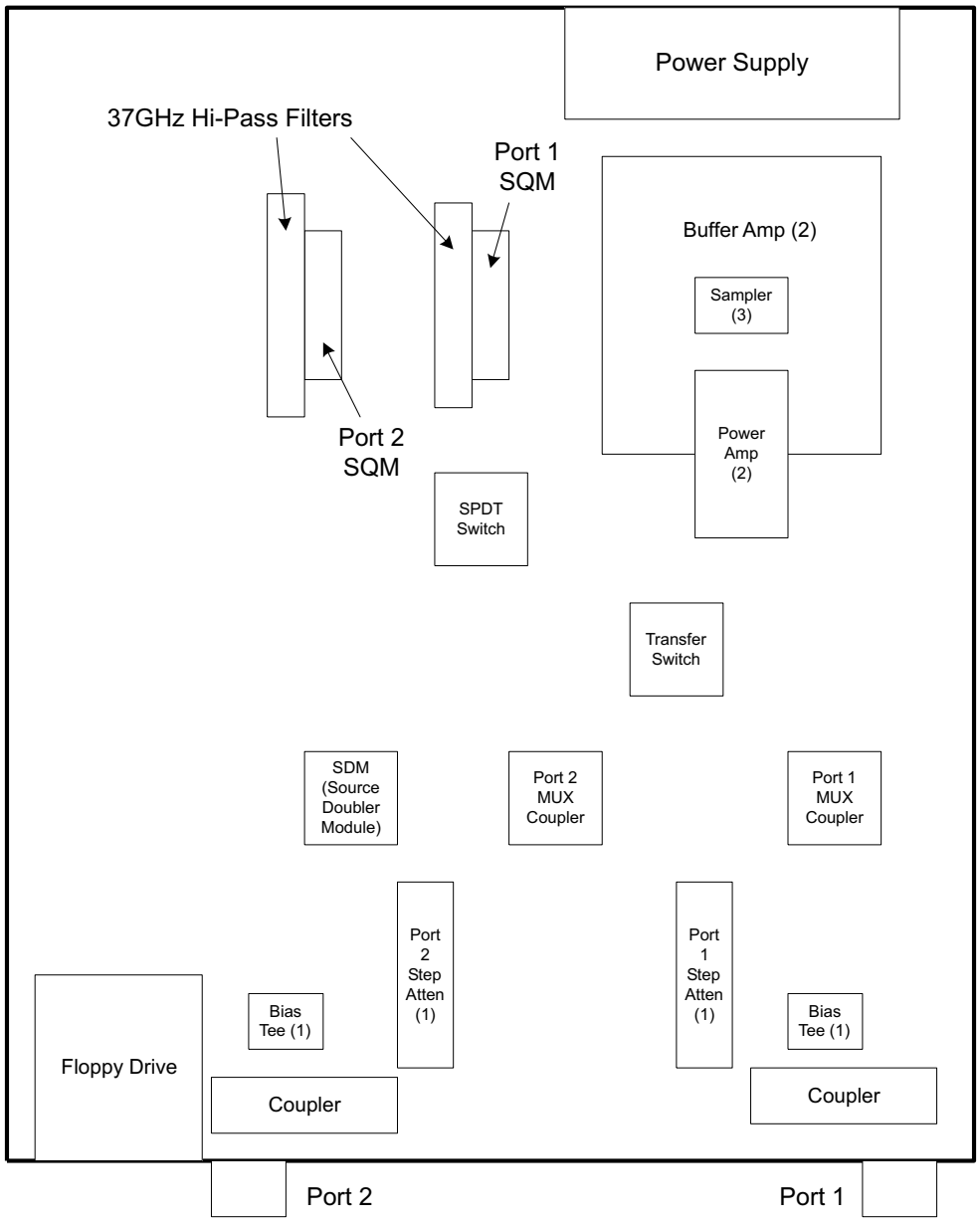
Step 4. Disconnect the Transfer Switch power cable at connector J5 of the A17 Motherboard PCB. Free the cable by separating it from the cable harness and by temporarily removing the A24 VME Terminator PCB.

Step 5. Remove the two screws that fasten the Transfer Switch mounting plate to the test set tray, and lift the Transfer Switch assembly from the Test Set Module.



Notes:
1. Couplers are replaced by bridges on Models 37217C and 37317C
2. Step Attenuators and Bias Tees are not present on 372xxC models
3. SDM's are present only on 40GHz and above models
4. Do not disconnect the sampler from the buffer amp
5. Buffer amp and Power amps are replaced only as a matched set.

Figure 8-11. *Test Set Module Components Layout Diagram for non 50 and 65 GHz Models*



Notes: **1. Not present on 372xxC models**
2. Buffer Amp and Power Amp are replaced only as a matched set
3. Do not disconnect the sampler from the buffer amp

Figure 8-12. *Test Set Module Components Layout Diagram for 50 and 65 GHz Models*

To replace the Transfer Switch assembly, perform the steps above in the reverse order.

Input Coupler(s)/Low Frequency Bridge(s)

Use the following procedure to remove/replace the Input Coupler(s) of all Models 37X25C through 37X69C and the Low Frequency Bridges of Models 37X17C.

Procedure:

Step 1. Using a 1 inch open-end wrench, remove the front panel nut and washer of the Port1 or Port2 coupler/bridge that is to be removed.

Step 2. Disconnect the two semi-rigid coaxial lines associated with the coupler/bridge (see Figure 8-11).

Step 3. Remove the two screws that fasten the coupler/bridge bracket to the test set tray. Move coupler/bridge to the rear and up to remove it from the Test Set Module.

To replace the coupler/bridge, perform the steps above in the reverse order.

Buffer Amplifier (A31)

Use the following procedure to remove/replace the Buffer Amplifier/ Power Amp assemblies of all models.

Preliminary:

- ❑ Remove the Power Amplifier assembly that is mounted beside the Buffer Amp.

Procedure:

Step 1. Disconnect the semi-rigid coaxial lines, W83 and W84, from the 20 dB pads that are part of the Buffer Amplifier assembly; see Figure 8-13. (For units with Option 11, the semi-rigid coaxial lines are W46 and W47.) (Wxx numbers are affixed to semi-rigid cables.)

Step 2. Disconnect the cables from connectors J1 through J7 of the A31 Buffer Amplifier assembly. (Pull up gently to disconnect.) Note that the connector end of each cable is marked with the associated A31 connector number.

Step 3. Disconnect the two cable connectors from the TEST A connector body on the Buffer Amplifier assembly (see Figure 8-13). Similarly, disconnect the two cable connectors from the REF A connector body.

> ***NOTE***
> The matching pin numbers are identified on the cable connectors and on the connector body.)

Step 4. Repeat Step 3 for the TEST B and REF B cable connectors.

Step 5. Remove the nine screws that fasten the Buffer Amplifier assembly to the test set tray, and lift the assembly from the Test Set Module.

To replace the Buffer Amplifier assembly, perform the steps above in the reverse order.

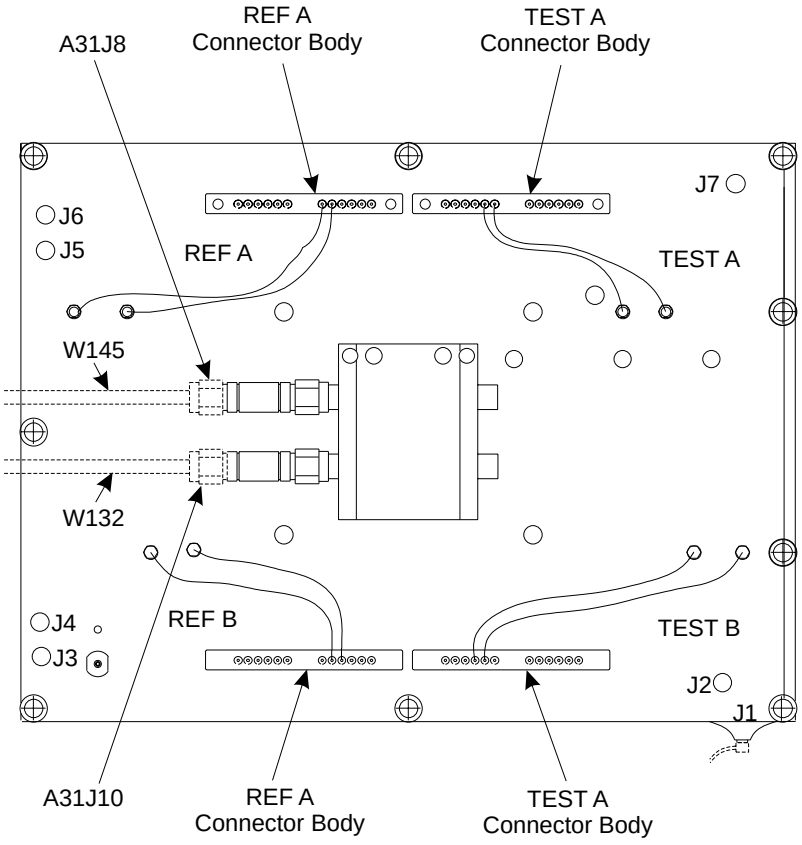


Figure 8-13. *A31 Buffer Amplifier Assembly, Details*

Switched Doubler Module Assembly

Use the following procedure to remove/replace the Switched Doubler Module (SDM) assembly for Model 37X69C.

Procedure:

Step 1. Disconnect the SDM power cable from connector J17 of the A17 Motherboard PCB. Free cable from cable clip, as necessary.

Step 2. Disconnect the semi-rigid coaxial line W81 from the input connector of the SDM; see Figure 8-12. (Wxx numbers are affixed to semi-rigid cables.)

Step 3. Remove the two screws that fasten the SDM to the Test Set Module tray.

Step 4. Disconnect the semi-rigid coaxial line W80 from the output connector of the SDM; see Figure 8-12. Carefully lift the assembly from the Test Set Module.

To replace the Switched Doubler Module assembly, perform the steps above in the reverse order.

8-14 SIGNAL SOURCE MODULES

The following sections provide instructions for removing the signal Source Module for replacement of individual components. (See the next section for removal of the A21A2 PCB without removing the entire Source Module assembly.) Removal of individual Source components is covered in the next sections

Equipment Required:

- ❑ Connector torque wrench (5/16 inch), Anritsu Model 01-201, or equivalent.

> ***CAUTION***
>
> Throughout these procedures, *always* use the 5/16 inch connector torque wrench for connecting the Signal Source Module semi-rigid coaxial lines and RF/microwave components. Use of improper tools may damage the connectors, resulting in degraded instrument performance.

Preliminary:

- ❑ Switch the VNA power to **off** and remove the power cord.
- ❑ Remove all covers (Section 8-3).

Removal of Signal Source Module

Use the following procedure to remove the Signal Source Module from the chassis. This step is necessary before any of the module components can be removed/replaced.

Procedure:

Step 1. Turn the instrument upside-down and remove the W87 cable (20 GHz and below units), or the W81 cable (40 GHz units), or the W179 and W180 cables (50 and 65 GHz units).

Step 2. Return the instrument to the normal operating position and, using steps below, remove the Source Module.

Step 3. Disconnect the two cables from the A21A2 PCB.

Step 4. Loosen the two captivated metal screws that attach the A21A2 bracket to the instrument frame.

Step 5. Disconnect the ribbon cable from the Frequency Converter.

Step 6. If the instrument is a 50 or 65 GHz model, loosen the W206 cable from the Switched Filter.

Step 7. Remove the three screws on the right side of the instrument frame from the Source Module frame.

Step 8. Lift the Source Module up, and remove by tipping the top to the right to clear the instrument frame.

To replace the Signal Source Module, perform the steps above in the reverse order.

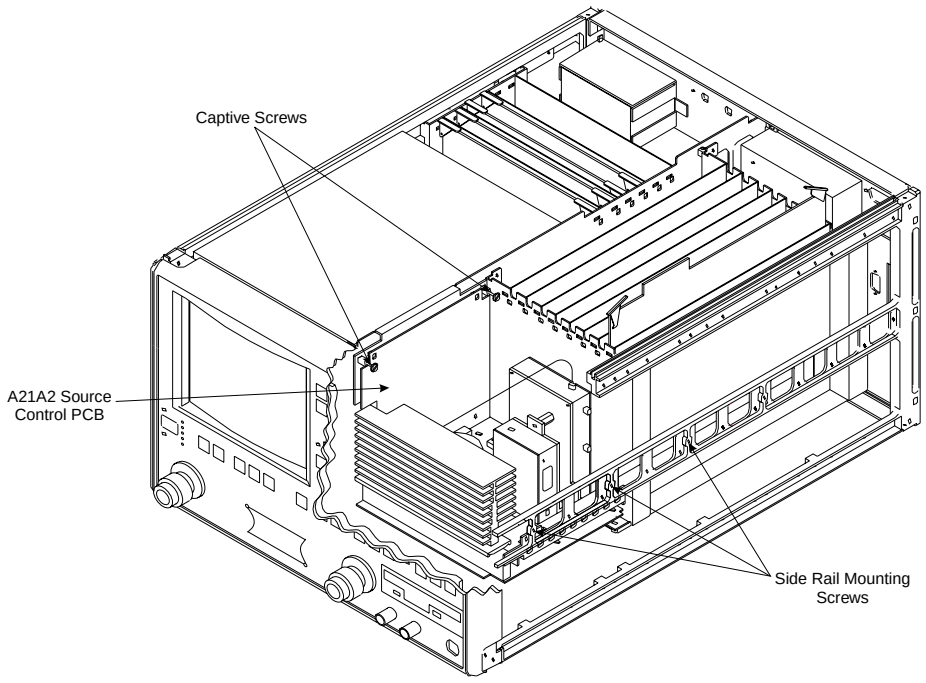


Figure 8-14. *Signal Source Module Removal Details*

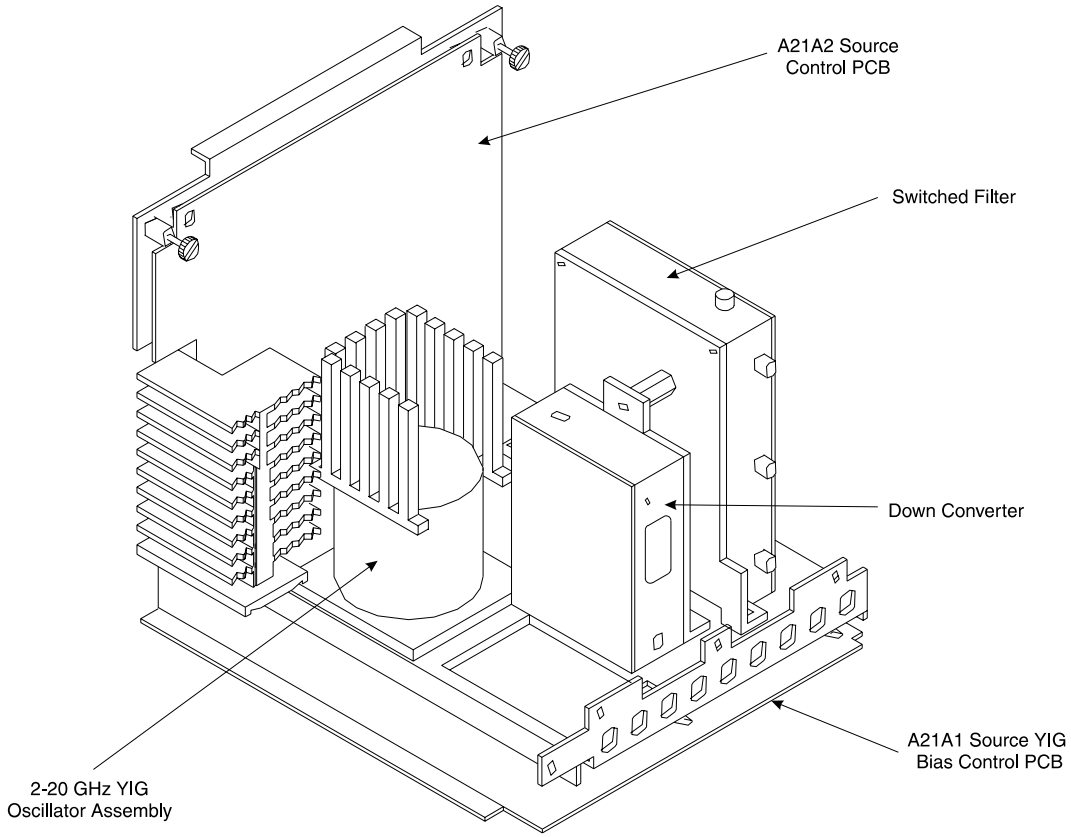


Figure 8-15. *Signal Source Module Assemblies Removal Details*

A21A2 Source Control PCB

Use the following procedure to remove/replace the A21A2 Source Control PCB assembly.

Procedure:

Step 1. Unfasten two black plastic PCB retainers at the top corners of the A21A2 Source Control PCB (see Figure 8-18). To unfasten, turn screwdriver slot ¼ turn *counter-clockwise.*

Step 2. Pull the top of the A21A2 PCB away from the source module chassis back plate to clear PCB retainers. Gently pull up to disconnect the A21A2 PCB from the socket on the A21A1 Source YIG Bias Control PC. Remove from Source Module.

To replace the A21A2 Source Control PCB assembly, perform the steps above in the reverse order.

A21A1 Source YIG Bias Control PCB

Use the following procedure to remove/replace the A21A1 Source YIG Bias Control PCB assembly.

Procedure:

Step 1. Disconnect the Switched Filter assembly power cable from connector J1 of the A21A1 Source YIG Bias Control PCB. (Pull up gently on ribbon cable to disconnect.)

Step 2. Similarly, disconnect the Down Converter assembly power cable from connector J4 of the A21A1 PCB.

Step 3. Disconnect the YIG Oscillator assembly power cable from connector J3 of the A21A1 PCB. Pull up on the flexible circuit connector handle to disconnect.

Step 4. Remove the screw that fastens the front apron of the source module chassis to the heatsink of the A21A1 PCB. See Figure 8-15.

Step 5. Remove the four screws that fastens the back plate of the source module chassis to the heatsink of the A21A1 PCB.

Step 6. Place the Signal Source Module on its‘ back plate.

Step 7. Unfasten the six PCB retainers on the bottom of the A21A1 PCB. (To unfasten, turn screwdriver slot ¼ turn *counter-clockwise.*) Gently separate the A21A1 PCB (including the heat sink) from the Signal Source Module.

To replace the A21A1 Source YIG Bias Control PCB assembly, perform the steps above in the reverse order.

Switched Filter Assembly

Use the following procedure to remove/replace the Switched Filter assembly.

Procedure:

Step 1. Disconnect the power cable from connector P1 at the rear of the Switched Filter assembly. (Use a small screw driver to pry up gently at each end of the connector, as necessary.)

Step 2. Disconnect the semi-rigid coaxial lines from connector J6 (top) and connector J3 (lower-front) of the Switched Filter assembly.

Step 3. Disconnect the semi-rigid coaxial line from the RF INPUT (top) connector of the *Down Converter* assembly.

Step 4. Remove the two screws that fasten the Switched Filter assembly to the source module chassis and lift the assembly from the Signal Source Module.

Step 5. Disconnect the semi-rigid coaxial line from connector J1 (bottom) of the Switched Filter assembly. Put this coaxial line aside for re-use.

> ***NOTE***
> When replacing the Switched Filter assembly, connect the semi-rigid coaxial line to the bottom connector (J1), before attaching the assembly to the Signal Source Module.

To replace the Switched Filter assembly, perform the steps above in the reverse order.

Down Converter Assembly

Use the following procedure to remove/replace the Down Converter assembly.

Procedure:

Step 1. Disconnect the power cable from connector P1 at the front of the Down Converter assembly.

Step 2. Disconnect the semi-rigid coaxial lines from the RF INPUT connector and RF OUTPUT connector of the Down Converter assembly.

Step 3. Remove the two screws that fasten the Down Converter assembly to the source module chassis and lift the assembly from the Signal Source Module.

To replace the Down Converter assembly, perform the steps above in the reverse order.

YIG Oscillator Assembly

Use the following procedure to remove/replace the YIG Oscillator assembly.

Procedure:

Step 1. Disconnect the YIG Oscillator assembly power cable from connector J3 of the A21A1 PCB. Pull up on the flexible circuit connector handle to disconnect.

Step 2. Disconnect the semi-rigid coaxial line from the connector J6 (top) of the *Switched Filter* assembly.

Step 3. Remove the four screws that fasten the YIG Oscillator assembly to the source module chassis and lift the assembly from the Signal Source Module.

Step 4. Disconnect the semi-rigid coaxial line from the output connector of the YIG Oscillator assembly. Put this coaxial line aside for re-use.

> ***NOTE***
> When replacing the YIG Oscillator assembly, connect the semi-rigid coaxial line removed in Step 4 to the output connector of the YIG Oscillator before attaching it to the Signal Source Module.

To replace the YIG Oscillator assembly, perform the steps above in the reverse order.

Appendix A
Error Messages

Table of Contents

Appendix A
Error Messages

A-1 INTRODUCTION

This appendix provides a listing of error messages that appear on the VNA display or that are written to the internal software Service Log.

A-2 OPERATIONAL ERROR MESSAGES

Table A-1 provides a listing and description of the operational error messages. For the most part, these errors are displayed only on the VNA display and are caused by incorrectly operating the VNA.

A-3 DISK RELATED ERROR MESSAGES

Table A-2 provides a listing and description of the disk-related-error messages. The numbered errors in this group are also written to the Service Log, since they may indicate system problems.

A-4 GPIB RELATED ERROR MESSAGES

Table A-3 provides a listing and description of GPIB-related error messages. These errors are entered in the Service Log and output as part of the response of OGE/OGL commands.

A-5 SERVICE LOG ERROR MESSAGES

Table A-4 provides a listing of the error messages that are written to the internal system service log. Some of these messages may occur as a result of incorrectly programming the VNA. This includes the GPIB errors, 7204 through 7207, and errors in the 5000 range, RF Power. The RF Power errors may be triggered when setting the VNA power to a value greater than its reset level. This feature of the VNA lets you take advantage of all available power; however, accuracy cannot be guaranteed when power is unleveled. Refer to Chapter 7, Section 7-6 for additional guidance in interpreting these error codes.

The error messages in Table A-4 are numbered and organized as follows:

0000 to 0099 These messages generally indicate status or a pass/fail result of a Peripheral or Self test.

0100 to 3999 These messages primarily indicate a self-test failure with the suspect assembly number being the two high-order digits. For example, error 0111 indicates test 11 for the A1 assembly has failed, similarly, error 0814 is related to the A8 assembly test #14, and error 2138 is related to the A21 assembly test #38.

Since these errors are primarily self-test errors, they do not get displayed but only get written to the service log. Any exceptions to this rule will be an assembly error code between xx00 through xx09, where xx is the assembly that is suspected of failing during normal operation. For example, error 0500 is a run-time error related to the A5 A/D assembly.

4000 to 4999 These messages indicate internal H/W calibration problems.

5000 to 5999 These messages indicate run-time RF power problems.

6000 to 6999 These messages indicate run-time phase lock problems. A letter or sequence of letters following the error message depict the suspect assembly(ies) as follows:

- A = 10 MHz Reference
- B = LO1 unlocked
- C = LO2 unlocked
- D = Source unlocked
- E = IF lock signal level too low
- F = External synthesizer unlocked
- G = LO3 unlocked
- None = Unknown

7000 to 7999 These messages indicate a run-time digital section problem.

8000 to 8999 These messages indicate a run-time processing system problem.

Table A-1. *Operational Error Messages (1 of 2)*

Error Message	Description	Corrective Action
ATTENUATOR UNAVAILABLE	Option 6 Port 2 Test Step Attenuator is not installed.	Install Option 6 Step Attenuator,
DIFFERENT H/W SETUP. RECALL ABORTED	Model and/or options is (are) different from the recalled setup.	Reconfigure system to duplicate the hardware setup that was used to store the saved data.
DIFFERENT S/W VERSION, RECALL ABORTED	Saved state not compatible with software version or options.	Load compatible software (S/W) version and retry.
FREQUENCIES HAVE REACHED UPPER LIMIT	Frequencies being defined in Multiple Source mode have reached upper limits of Sources.	Redefine frequencies to not exceed limits of Sources.
MEMORY LOCATION CORRUPTED	Requested memory location is corrupted.	None. If problem reoccurs after storing a new setup, contact Anritsu Customer Service.
NO BANDS ARE STORED	No frequency bands have been defined and stored.	Define and store frequency bands to turn on Multiple Source mode.
NO STORED MEMORY DATA	No data is stored in memory for display or trace math.	Store or re-save measurement data.
OPTION NOT INSTALLED	Selected an option that is not installed.	None.
OUT OF CAL RANGE	Entered values out of the selected calibration range.	Change calibration range or re-enter values that are within the current range.
OUT OF H/W RANGE	Entered value is out of the instrument's hardware range.	Re-enter values that are within range.
OUT OF RANGE	Entered value is out of range.	Re-enter values that are within range.
RECEIVER OUT OF RANGE BY EQUATION	Equation defined in Multiple Source mode places receiver frequency out of range when attempting to store band.	Redefine frequency.
SOURCE 1 OUT OF RANGE BY EQUATION	Equation defined in Multiple Source mode places Source 1 frequency out of range when attempting to store band.	Redefine frequency.
SOURCE 2 OUT OF RANGE BY EQUATION	Equation defined in Multiple Source mode places Source 2 frequency out of range when attempting to store band.	Redefine frequency.

Table A-1. *Operational Error Messages (2 of 2)*

Error Message	Description	Corrective Action
STANDARD CAL NOT VALID FOR WAVEGUIDE	Cannot use the standard method when calibrating with waveguide.	Use the Offset Short method with waveguide.
START F FOLLOWS PREVIOUS STOP F	Start frequency of current band immediately follows stop frequency of previous band. Cannot be modified.	None.
START MUST BE LESS THAN STOP	Entered start frequency is greater than the stop frequency.	Re-enter frequency values such that the start frequency is lower than the stop frequency.
STEP IS TOO LARGE	Entered harmonic frequency extends the stop out of range.	Re-enter so that harmonic frequency is within range.
STOP IS OVER RANGE	Entered value exceeds the instrument's stop frequency.	Re-enter stop frequency.
SYSTEM NOT CALIBRATED	VNA is uncalibrated for the selected measurement values.	Perform a measurement calibration.
TOO FEW POINTS, 2 MINIMUM	Entered too few discrete fill points, 2 is minimum.	Re-enter data points.
TOO MANY POINTS, 1601 MAXIMUM	Entered too many discrete fill points, 1601 points are the maximum allowed.	Re-enter data points.
UNDEFINED DIVIDE BY ZERO	Denominator cannot be zero in equation.	Make denominator a value other than zero.
WINDOW TOO SMALL	Attempted to set time domain range smaller than allowed	Re-enter larger time range.
OUT OF WINDOW RANGE	Attempted to set time domain range larger than allowed	Re-enter values within allowed range.

Table A-2. *Disk-Related-Error Messages (1 of 1)*

Error Message	Description	Corrective Action
7140 GENERAL FLOPPY DRIVE FAIL	Invalid disk media or format.	Use 1.44 MB diskette and/or format in the VNA.
7142 FLOPPY DISK READ ERROR	Read error when accessing disk file.	Use 1.44 MB diskette and/or format in the VNA.
7143: FLOPPY DISK WRITE ERROR	Error in writing to disk file.	Use 1.44 MB diskette and/or format in the VNA.
7147 FLOPPY DISK UNAVAILABLE	Floppy disk is not available.	Install floppy diskette and/or check floppy disk drive.
7170: GENERAL HARD DISK FAIL	General error in accessing hard disk.	Retry and if still fails, reformat the hard disk drive and/or check floppy disk drive.
7172: HARD DISK READ ERROR	Read error when accessing disk file.	Retry and if still fails, reformat the hard disk drive and/or check floppy disk drive.
7173: HARD DISK WRITE ERROR	Error in writing to disk file.	Retry and if still fails, reformat the hard disk drive and/or check floppy disk drive.
7177: HARD DISK UNAVAILABLE	Hard disk is not available.	Install hard disk drive and/or check operation of hard disk.
8140: GENERAL DISK BUFFER ERROR	Out of RAM.	Press the System State, Default Program key, and retry. This will reset the VNA to the factory default state.
FILE NOT FOUND	Disk file not found.	None.
FLOPPY DISK HAS NO ROOM FOR FILE	Floppy diskette is full.	Delete files or install new diskette.
FLOPPY DISK NOT READY	Floppy disk is not ready (or not installed.).	Install diskette in floppy drive.
FLOPPY DISK WRITE PROTECTED	Write protect tab in place on floppy diskette.	Remove write-protect tab.
HARD DISK HAS NO ROOM FOR FILE, DELETE EXISTING FILES(S) TO CREATE SPACE	Hard disk is full.	Delete unneeded files.

Table A-3. *GPIB-Related Error Messages (1 of 8)*

Error Message	Description
These errors are entered in the Service Log and output as part of the response of OGE/OGL commands for GPIB commands. The list is subdivided into the type of GPIB error: 7204..., 7205..., 7206..., and 7207.	
	7204 GPIB COMMAND ERROR DESCRIPTIONS
Faulty program mnemonic syntax	Generated when the program mnemonic found was not one of the currently defined program mnemonics for the VNA.
Faulty suffix mnemonic syntax	Generated when the suffix mnemonic found was not one of the currently defined suffix mnemonics for the VNA.
Faulty mnemonic syntax	Generated when the mnemonic found was not one of the currently defined program or suffix mnemonics for the VNA.
Missing Program Message Separator	Generated when the required semicolon preceding the next program mnemonic was not found.
Expected NRf data	Generated when a mnemonic is used that requires a trailing NRf numeric data element. The data element was either missing or the first character of the data element was not one of the acceptable NRf characters.
NRf mantissa too long	The maximum allowable number of characters in the NRf numeric element mantissa is 255.
Exponent magnitude too large	The maximum allowable exponent magnitude in an NRf element is +/— 32000.
Faulty NRf syntax	Can be any number of syntactical errors such as more than one decimal point, inclusion of a decimal point in the exponent field, an invalid character imbedded in the numeric or no exponent value following the ‘E’.
Expected String Program Data	Generated when a mnemonic is used that requires a trailing string data element. The date element was either missing or no open quote character was found.
Missing close quote character	Generated when a mnemonic is used that requires a trailing string data element. The open quote character was found, but the close quote character was not.
Expected Arbitrary Block data	Generated when a mnemonic is used that requires a trailing arbitrary block data element and the trailing element was not an arbitrary block data element. Or in some cases, the arbitrary block was empty.
Faulty Arbitrary Block	Generated when a defined length arbitrary block data element is terminated early with an EOI or an indefinite length arbitrary block data element is not properly terminated.
Missing Program Data Separator	Two data elements of a program mnemonic that requires multiple program data elements, are not properly separated from each other by a comma.

Table A-3. *GPIB-Related Error Messages (2 of 8)*

Error Message	Description
GET received during PM reception	Generated when the GPIB Command 'Group Execute Trigger' is received during the reception of a program message but before its proper termination with the end message. The partial program message up to but not including the 'Group Execute Trigger' will be executed. Execution of the Group Execute Trigger and any subsequent program message elements received before the end message will be skipped.
	7205 GPIB EXECUTION ERROR DESCRIPTIONS
Not permitted in a DDT command sequence	When executing a defined device trigger command sequence, a forbidden command was detected.
Too much Arbitrary Block data	The arbitrary block supplied contained more data than was necessary for the currently defined VNA state. This can occur when graph types, start/stop frequencies or data points are changed.
Insufficient Arbitrary Block data	The arbitrary block supplied did not have enough data for the currently defined VNA state. This can occur when graph types, start/stop frequencies or data points are changed.
Invalid parameter for current graph type	An attempt was made to program a non-existent parameter for the current graph type. For instance, a Smith chart does not have a reference or reference line position (mnemonics OFF and REF).
Parameter out of range	An attempt was made to program an out of integer range value for a parameter. This error is detected by the GPIB MANAGER when converting and rounding to the appropriate integral size (signed/unsigned char/short or long).
Parameter value not permitted	A parameter value was not found in the list of permissible values for that parameter.
CW marker sweep not permitted in time domain	The mnemonics M1C, M2C, M3C, M4C, M5C and M6C are forbidden in time domain.
Parameter unavailable in frequency domain	The mnemonic ODV and OTV are forbidden in frequency domain.
Port 2 Test Attenuator (OPT 6) not installed	The mnemonic TA2 is forbidden when the attenuator is not installed.
Time Domain (OPT 2) not installed	An attempt was made to use one of the time domain mnemonics when the option is not installed.
Return to Local not permitted in Local Lockout	The mnemonic RTL failed due to being in the Local Lockout mode.
Calibration does not exist	An attempt was made to turn on flat power correction or vector error correction when the corresponding calibration does not exist.
Cal term not available	An attempt was made to get a calibration term which does not exist for the current calibration type.

Table A-3. *GPIB-Related Error Messages (3 of 8)*

Error Message	Description
Invalid cal term for calibration type	An attempt was made to program a calibration term which does not exist for the current calibration type.
Front panel setup not valid	An attempt was made to get a front panel setup that did not contain a correct/valid state.
Normalization data not valid	An attempt was made to reference normalization data when there was no normalization data currently stored.
Command sequence too long	An attempt was made to define a device trigger command sequence which had more than 255 characters.
Unable to display menu	An attempt was made to display a menu which could not be displayed for the current VNA state.
String too long	An attempt was made to enter a string for the following mnemonics which exceeded the specified maximum length. LTD, LID, LMS and LNM - maximum length is 15 characters. LOC - maximum length is 79 characters.
Must specify a calibration type first	In order to perform a calibration, the calibration type must be specified by the use of one of the Cxx mnemonics (i.e. C12, C8T, etc.) PRIOR to the issuance of the mnemonics CWC, TDC or BEG.
Parameter value unchanged	An attempt was made to change a start/stop frequency or number of data points to a value outside of the current calibrated range with correction turned on.
Parameter change not permitted	An attempt was made to perform an illegal state change or action based on the current VNA state. This includes attempting to store an undefined band definition. Or certain changes from the calibration state or the calibration define state when defining discrete frequencies.
Parameter value out of range Parameter out of hardware range	An attempt was made to set a parameter to a value outside of the permissible range of values for the parameter.
Standard cal method not valid for waveguide	In a waveguide type of calibration, the standard (OSL) cal method is forbidden.
Out of calibrated range	An attempt was made to change a parameter not permitted to be changed with correction on.
Start must be must be less than stop	An attempt was made to set a new start frequency, distance or time greater than or equal to the current stop frequency, distance or time. Or to set a new stop frequency, distance or time less than or equal to the current start frequency, distance or time.
Tune mode requires a 12 term calibration	Perform a 12 term calibration prior to turning on tune mode.

Table A-3. *GPIB-Related Error Messages (4 of 8)*

Error Message	Description
Current and cal frequencies different	The flat power calibration setup does not match the current setup.
Stored data is invalid	An attempt was made to reference normalized data when normalized data was invalid.
Parameter change not permitted on current state	An attempt was made to change a parameter while IF cal was active. It is not expected that this message will ever be seen. If you see this message, notify the factory.
Calibration may not be valid	An attempt was made to repeat the previous calibration when there was no record of a previous calibration.
Calibration does not exist	An attempt was made to turn on flat power correction or vector error correction when the corresponding calibration does not exist.
Current calibration is erased	When turning on Multiple Source Mode with vector error correction on, the calibration is destroyed. Not really an error. Message is issued as a warning.
Time Domain and CW mode not permitted	An attempt was made to turn on a time domain mode in CW. This is not permitted.
Not permitted in Time Domain	An attempt was made to select a group delay display or CW mode when in time domain mode or to select a dual overlay display with a frequency/time domain mismatch.
Time Domain not allowed	An attempt was made to turn on a time domain mode but the current VNA state does not permit it.
Permitted only in diagnostic mode	Must put the VNA into the diagnostics mode via the SDG command before using this mnemonic.
Graph types not appropriate for dual overlay	While in dual overlay mode, and attempt was made to change one of the active graph types to a type which conflicts with dual overlay, or to change one of the active channels into or out of time domain which sets up a dual overlay conflict. Or an attempt was made to select dual overlay mode when there would be a graph type conflict for a frequency/time domain conflict.
New Discrete Fill not allowed in current state	Cannot set up a new discrete fill definition while performing a calibration or when correction is turned on. Also cannot do this when group delay is the graph type on the active channel.
Low Pass mode requires a harmonic sweep	Perform a TD harmonic sweep calibration prior to using this mnemonic.
Receiver out of range by equation	Problems with the internal source, external source or receiver equations in multiple source mode.
New start less than previous stop	An attempt was made to set the start frequency for the new multiple source mode band definition to a frequency less than the stop frequency of the previous band.

Table A-3. *GPIB-Related Error Messages (5 of 8)*

Error Message	Description
Bad filename	The supplied filename was bad. The filename can have 8 characters maximum. No extensions. The filename must start with and alpha type character (A thru Z). After that the allowable characters are alpha, numeric (0 thru 9) and underscore (_).
Conflict with rotary knob	You should not be using the rotary knob and the GPIB at the same time.
Too many data points for external source	A 6700B series external source can handle 501 data points. A 68000 series external source can handle 999 data points.
Recalled setup corrupted Hardware mismatch in recalled setup Software mismatch in recalled setup	These are problems with the recalled setup.
Too many data points for Discrete Fill	The maximum number of data points in discrete fill is 1601.
Not enough data points for Discrete Fill	The minimum number or data points in discrete fill is 2.
Discrete Fill end frequency out of range	The number of points for discrete fill puts the end frequency out of range.
Step is too large	When setting up a time domain harmonic sweep, cannot get 2 data points because the start frequency is too high for the approximate stop frequency. In a group delay display, the delay aperture percent of sweep is less than one step size.
Range too small	An attempt was made to set a distance or time span value too small. This can also be done via inappropriate values for start and stop.
Start or stop out of range	An attempt was made to set a distance or time start or stop value out of range. This can also be done via inappropriate values for center and span.
No bands defined	An attempt was made to turn on multiple source mode with no band definitions.
Out of frequencies for new band definition Source out of range by equation External source out of range by equation	The current set of multiple source mode bands use up all the frequency range of the VNA. Therefore, no more bands can be defined.
File is read only	An attempt was made to write to a write protected file.
File not found	An attempt was made to access a non-existent file.
Floppy drive not ready	An attempt was made to access the floppy drive with no floppy disk installed.
Floppy disk full Hard disk full	An attempt was made to write to a floppy disk or the hard disk when no space was left on the disk.

Table A-3. *GPIB-Related Error Messages (6 of 8)*

Error Message	Description
Floppy disk write protected	An attempt was made to write to a write protected floppy disk.
Recalled setup or data file corrupt	An attempt to recall a setup from internal memory, the GPIB or disk failed due to software revision or hardware mismatch or checksum error.
New frequency list not allowed in current state	Cannot set up a new discrete fill definition while performing a calibration or when correction is turned on. Also, cannot do this when group delay is the graph type on the active channel.
State change not permitted	An attempt was made to perform an illegal state change or action based on the current instrument state. This includes attempting to store (1) an undefined band definition, (2) certain changes from the calibration state, or (3) the cal define state when defining discrete frequencies.
Faulty label or file name	The label or file name associated with the current mnemonic is faulty.
Illegal characters in filename	The first character in a filename must be an alpha type. The remaining characters can be alpha, numeric, or underscores. An extension is not permitted.
Filename too long	The maximum lendngth for filenames is 8 characters. An extension is not permitted.
Floppy disk read error Floppy disk write error Hard disk read error Hard disk write error	Read or write error(s) occurred while attempting to access the indicated disk.
Floppy disk not found Hard disk not found General disk buffer error General floppy drive failure Floppy disk init failure General hard disk failure Hard disk control failure Hard disk init failure Unknown disk error	Other error messages which suggest that the indicated drive is in need of service.
7205 GPIB QUERY ERROR DESCRIPTIONS	
No Response data available	Generated if the controller attempts to read response data from the VNA and none is available.
No Response data after PM completion	This is the same as the 'no response data available' case above except that a program message was currently being parsed and executed when the controller attempted to read data. Detection of this error was deferred until the parser/execution block was finished with the current program message and it was observed that no response data was generated.

Table A-3. *GPIB-Related Error Messages (7 of 8)*

Error Message	Description
Response after Indefinite Response discarded	This error is generated when the VNA's output queue has already received an Arbitrary ASCII response data element and an attempt is made to place another response data element of any kind into the queue. The new response data element is discarded.
Interrupted - Response data discarded	This error is detected when the output queue contains unread response data and the controller sends a new program message. The response data is discarded.
Unterminated - Partial PM will be executed	This error is detected when the VNA's input queue is currently receiving a program message but has not yet received the end message, and the controller attempts to read response data from the VNA. The partial program message in the input queue is executed as if it were properly terminated.
Deadlock - Response data discarded	This error is detected when both of the VNA's input and output queues are full and the controller attempts to send another data byte. In order to prevent bus deadlock, the contents of the output queue are discarded.
	7205 GPIB DEVICE DEPENDENT ERROR DESCRIPTIONS
Q_SEND failure in [a procedure name]	An unsuccessful attempt was made to send a message to a task. The procedure name is the place in the software where the error was detected.
Q_RECEIVE failure in [a procedure name]	A failure was detected while waiting for the reception of a message from a task. The procedure name is the place in the software where the error was detected.
Unable to allocate memory in [a procedure name]	An attempt was made to allocate some temporary memory in order to accomplish a task directed in the program message. The procedure name is the place in the software where the error was detected.
Unable to release memory in [a procedure name]	An attempt was made to return some temporary memory within a task and the return failed for some reason. The procedure name is the place in the software where the error was detected.
Unable to get service/error log	An unsuccessful attempt was made to get a copy of the service or error log.
Unable to get calibration term	An unsuccessful attempt was made to get a calibration term.
Unable to get raw or corrected data	An unsuccessful attempt was made to get raw or corrected data.
Unable to get final data	An unsuccessful attempt was made to get final data.
Unable to get setup or data	An unsuccessful attempt was made to get the frequency list from the database.
Unable to get setup	An unsuccessful attempt was made to get a front panel setup.

Table A-3. *GPIB-Related Error Messages (8 of 8)*

Error Message	Description
Unable to store setup	An unsuccessful attempt was made to save a front panel setup.
Unable to get frequency list	An unsuccessful attempt was made to get setup, trace, or tabular datat from the database.
Unable to store label	An unsuccessful attempt was made to store a label in the database.
Calibration step failure	An error occurred while waiting for completion of a data collection sequence in calibration.

Table A-4. *Service Log Error Messages (1 of 3)*

0000 INFORMATIONAL MESSAGE	0511 A TO D COMM FAIL
0000 SELF TEST INFO MESSAGE	0512 A TO D 8 BIT D TO A FAIL
0094 PRNT INTERFACE TEST PASSED	0513 A TO D 12 BIT A TO D FAIL
0095 PRNT INTERFACE TEST FAILED	0514 A TO D STEERING DAC FAIL
0096 GPIB INTERFACE TEST PASSED	0515 A TO D CONV ACCURACY FAIL
0097 GPIB INTERFACE TEST FAILED	0516 A TO D SAMPL HOLD FAIL
0098 SELF TEST PASSED	0517 IF SYNC FAIL
0099 SELF TEST FAILED	0518 PWR SUPPLY SYNC FAIL
0111 LO1 COMM FAIL	0519 A TO D EXT ANAL OUTP FAIL
0112 LO1 PRE TUNE DAC FAIL	0520 PWR SUPPLY +5V FAIL
0113 LO1 PHS LCK IND FAIL	0521 PWR SUPPLY +9V FAIL
0114 PHS LCK ERR VOL OUT OF TOL	0522 PWR SUPPLY +12V FAIL
0115 LO1 LCK TIME FAIL	0524 PWR SUPPLY +18V FAIL
0211 LO2 COMM FAIL	0525 PWR SUPPLY -18V FAIL
0212 LO2 MAIN PREST DAC FAIL	0526 PWR SUPPLY +27V FAIL
0213 LO2 OFFS PREST DAC FAIL	0527 PWR SUPPLY -27V FAIL
0214 MAIN PHS LCK ERR VOL FAIL	0611 TB IF COMM FAIL
0215 OFFST PHS LCK ERR VOL FAIL	0612 TB IF 10V REF FAIL
0216 DDS PHS LCK ERR VOL FAIL	0613 TB IF LEVEL STATUS FAIL
0217 MAIN PHS LCK IND FAIL	0614 TB PHS CONTROL FAIL
0218 OFFST PHS LCK IND FAIL	0711 LO3 COMM FAIL
0219 DDS PHS LCK IND FAIL	0712 LO3 REF OSC FAIL
0220 LO2 LCK TIME FAIL	0713 LO3 48.4 LCK IND FAIL
0221 LO2 SRC TRACKING FAIL	0714 LO3 48.4 LCK ERR VOL FAIL
0311 TA IF COMM FAIL	0715 LO3 CAL REF PHS FAIL
0312 TA IF 10V REF FAIL	0811 SL SIG SEP COMM FAIL
0313 TA IF LEVEL STATUS FAIL	0812 DAC ADJUSTMENT FAIL
0314 TA PHS CONTROL FAIL	0813 TRANSFER SWITCH CNTRL FAIL
0411 REF IF COMM FAIL	0814 SRC LCK POL CONTROL FAIL
0412 REF IF 10V REF FAIL	0815 DIRECT MODE ATTEN FAIL
0413 REF IF LEV STATUS FAIL	0911 A9 VME BUS INTERFACE FAIL
0414 REF PHS CONTROL FAIL	0912 BBRAM CHECK FAIL
0500 A TO D CONVERSION FAIL	0913 SRAM CHECK FAIL

Table A-4. *Service Log Error Messages (2 of 3)*

0914 SCSI DEVICE FAIL	2127 SRC ALC CAL BND1 FAIL
0915 MCCHIP FAIL	2128 SRC ALC CAL BND2 FAIL
0915 MCCHIP TIMER 1 FAIL	2129 SRC ALC CAL BND3 FAIL
0916 MCCHIP TIMER 2 FAIL	2130 SRC ALC CAL BND4 FAIL
0917 MCCHIP TIMER 3 FAIL	2131 SRC ALC CAL BND5 FAIL
0918 MCCHIP TIMER 4 FAIL	2132 SRC ALC CAL BND6 FAIL
0919 CLOCK NOT RUNNING	2133 SRC ALC CAL BND7 FAIL
1311 A13 VME BUS INTERFACE FAIL	2134 SRC ALC CAL BND8 FAIL
1312 EXT KEYBD CNTRL FAIL	2135 SRC ALC CAL BND9 FAIL
1313 FLOPPY DISK CNTRL FAIL	2136 SRC ALC CAL BND10 FAIL
1411 A14 VME BUS INTERFACE FAIL	2137 SRC A1 FM PATH TUNE FAIL
1511 A15 VME BUS INTERFACE FAIL	2138 SRC A2 FM PATH TUNE FAIL
1512 VRAM CHECK FAIL	4100 LO1 CAL FAIL
1611 HARD DISK CONTROL FAIL	4200 LO2 CAL FAIL
1811 AUXILLARY IO FAIL	4301 SRC FREQ CAL MEAS UNSTABLE
1912 FRONT PANEL CNTRL FAIL	4302 SRC FREQ FM MAIN CAL FAIL
1913 ROTARY KNOB FAIL	4303 SRC FREQ FM SENS CAL FAIL
2111 SRC COMM FAIL	4304 SRC FREQ CAL VERIFY FAIL
2112 SRC FTUNE DAC FAIL	4401 SRC ALC LOG AMP CAL FAIL
2113 SRC STATE MACHINE DAC FAIL	4402 SRC ALC CAL VERIFY FAIL
2114 SRC FM CAL FAIL	4500 IF CAL FAIL
2115 SRC F TUNE PATH BND1 FAIL	4600 GAIN RANGING ERROR
2116 SRC F TUNE PATH BND2 FAIL	4700 STATE MACHINE FAIL
2117 SRC F TUNE PATH BND3 FAIL	5110 RF PWR UNLEVELED
2118 SRC F TUNE PATH BND4 FAIL	5210 REF A CHAN RF OVERLOAD
2119 SRC F TUNE PATH BND5 FAIL	5220 REF B CHAN RF OVERLOAD
2120 SRC F TUNE PATH BND6 FAIL	5230 TA CHAN RF OVERLOAD
2121 SRC F TUNE PATH BND7 FAIL	5240 TB CHAN RF OVERLOAD
2122 SRC F TUNE PATH BND8 FAIL	6001 - 6128 PHASE LOCK FAILURE
2123 SRC F TUNE PATH BND9 FAIL	7100 FILE MARKED READ ONLY
2124 SRC F TUNE PATH BND10 FAIL	7140 GENERAL FLOPPY DRIVE FAIL
2125 SRC PWR LEVEL DAC FAIL	7142 FLOPPY DISK READ ERROR
2126 SRC DETECTOR ZERO CAL FAIL	7143 FLOPPY DISK WRITE ERROR

Table A-4. *Service Log Error Messages (3 of 3)*

7146 FLOPPY DISK CHANGED	7222 PLOTTER OUT OF PAPER
7147 FLOPPY DISK UNAVAILABLE	7223 PLOTTER PEN UP
7169 FLOPPY INIT FAIL	7230 POWER METER NOT RESPONDING
7170 GENERAL HARD DISK FAIL	7240 FRQ COUNTER NOT RESPONDING
7172 HARD DISK READ ERROR	7250 EXT SOURCE NOT RESPONDING
7173 HARD DISK WRITE ERROR	7310 PRINTER NOT RESPONDING
7177 HARD DISK UNAVAILABLE	7311 PRINTER NOT READY
7199 HARD DISK INIT FAIL	7312 PRINTER OUT OF PAPER
7200 IEEE 488.2 GPIB BUS ERROR	7320 AUX I/O PORT ERROR
7201 ABORTED MESSAGES	7330 SERIAL PORT ERROR
7202 NOTHING TO SAY	7340 ETHERNET PORT ERROR
7203 NO LISTENER ON BUS	7350 EXT TRIG RATE TOO FAST
7204 GPIB COMMAND ERROR	7410 EXT KYBD ERROR
7205 GPIB EXECUTION ERROR	8100 PWR FAIL
7206 GPIB DEVICE SPECIFIC ERROR	8110 GENERAL VME BUS FAIL
7207 GPIB QUERY ERROR	8120 GENERAL MEMORY FAIL
7210 DEDICATED GPIB BUS ERROR	8121 NON-VOLATILE MEMORY FAIL
7220 PLOTTER NOT RESPONDING	8130 PROCESSING FAIL
7221 PLOTTER NOT READY	8140 GENERAL DISK BUFFER ERR

Appendix B
Connector Care and Handling

Table of Contents

Appendix B
Connector Care and Handling

B-1 INTRODUCTION

This appendix provides general, precautionary information and instructions pertaining to precision connectors.

B-2 PRECAUTIONS

The following paragraphs are precautionary notes relating to maintenance considerations for precision connectors

Pin Depth Problems

Based on Anritsu precision components returned for repair, destructive pin depth of mating connectors is the major cause of failure in the field. When a precision component is mated with a connector having a destructive pin depth, damage will likely occur to the precision component's connector. A connector is considered to have destructive pin depth when the center pin is too long in respect to the connector's reference plane (Figure B-1).

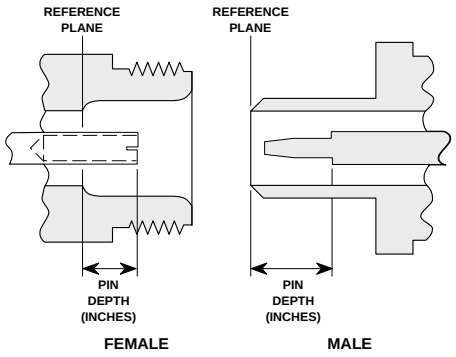


Figure B-1. *N Connector Pin Depth Definition*

Before mating an unknown or new device with your VNA Port connectors or calibration devices, always measure the pin depth of the device's connectors. Use a Anritsu Pin Depth Gauge, or equivalent, for these measurements (Figure B-2). Also, measure the connector pin-depth of a device when intermittent or degraded performance is suspected.

Gauging sets for measuring the pin-depth of precision connectors are available from your nearest Anritsu Service center, or from the factory. Instructions for measuring connector pin-depth are included with the gauging set(s).

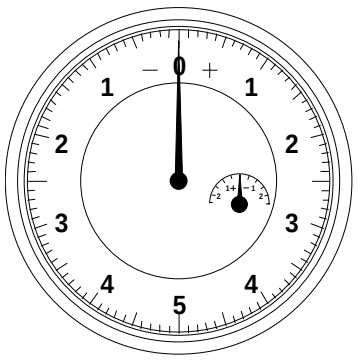


Figure B-2. *Pin Depth Gauge*

Pin-Depth Tolerance

The center pin of a precision connector has a tolerances measured in mils (one mil = 1/1000 inch). The connectors of test devices may not be precision types and they may not have the proper pin-depth. These connectors should be measured before mating to ensure suitability.

When gauging pin depth, if the connector being measured indicates out of tolerance in the "+" region of the gauge (Table B-1), the center pin is too long. *Mating under this condition will likely damage the mating connector.* On the other hand, if the test device connector indicates out of tolerance in the "–" region, the center pin is too short. While this will not cause any damage, it will result in a poor connection and a consequent degradation in performance.

Table B-1. *Connector Pin-Depth Tolerance*

Port/ Conn. Type	Pin Depth (MILS)	Gauge Reading
GPC-7	+0.000 –0.003	Same As Pin Depth
N Male	207 –0.000 +0.004	207 +0.000 –0.004
N Female	207 –0.004 +0.000	Same As Pin Depth
3.5 mm Male, Female	–0.000 +0.002	
K Male, Female	+0.0000 –0.0035	
V Male	+0.000 to –0.001	
V Female	+0.000 to –0.001	

Avoid Over Torquing Connectors

Over-torquing connectors is destructive; it may damage the connector center pin. Finger-tight is usually sufficient, especially on Type N connectors. Should it be necessary to use a wrench to tighten SMA or WSMA connectors, use a torque wrench that breaks at 8 inch-pounds. As a general rule, *never use pliers* to tighten connectors.

Teflon Tuning Washers

The center conductor on many precision connectors contains a small teflon tuning washer located near the point of mating (interface). This washer compensates for minor impedance discontinuities at the interface. The washer's location is critical to the connector's performance. *Do not disturb it*.

Avoid Mechanical Shock

Precision connectors are designed to withstand years of normal bench handling. Do not drop or otherwise treat them roughly. They are laboratory-quality devices, and like other such devices, they require careful handling.

Keep Connectors Clean

The precise geometry that makes a precision connector's high performance possible can be disturbed by dirt and other contamination adhering to connector interfaces. When not in use, keep the connectors covered.

Visual Inspection

Precision connectors should be inspected periodically. Check for the following:

- Bent or broken center pin
- Damaged threads
- Other bent or damaged connector parts
- Dirt or foreign material in connector cavity.

B-3 REPAIR/MAINTENANCE

Anritsu recommends that no maintenance other than cleaning be attempted by the customer. Any device with a suspected defective connector should be returned to Anritsu for repair and/or service when needed.

Appendix C
Performance Specifications

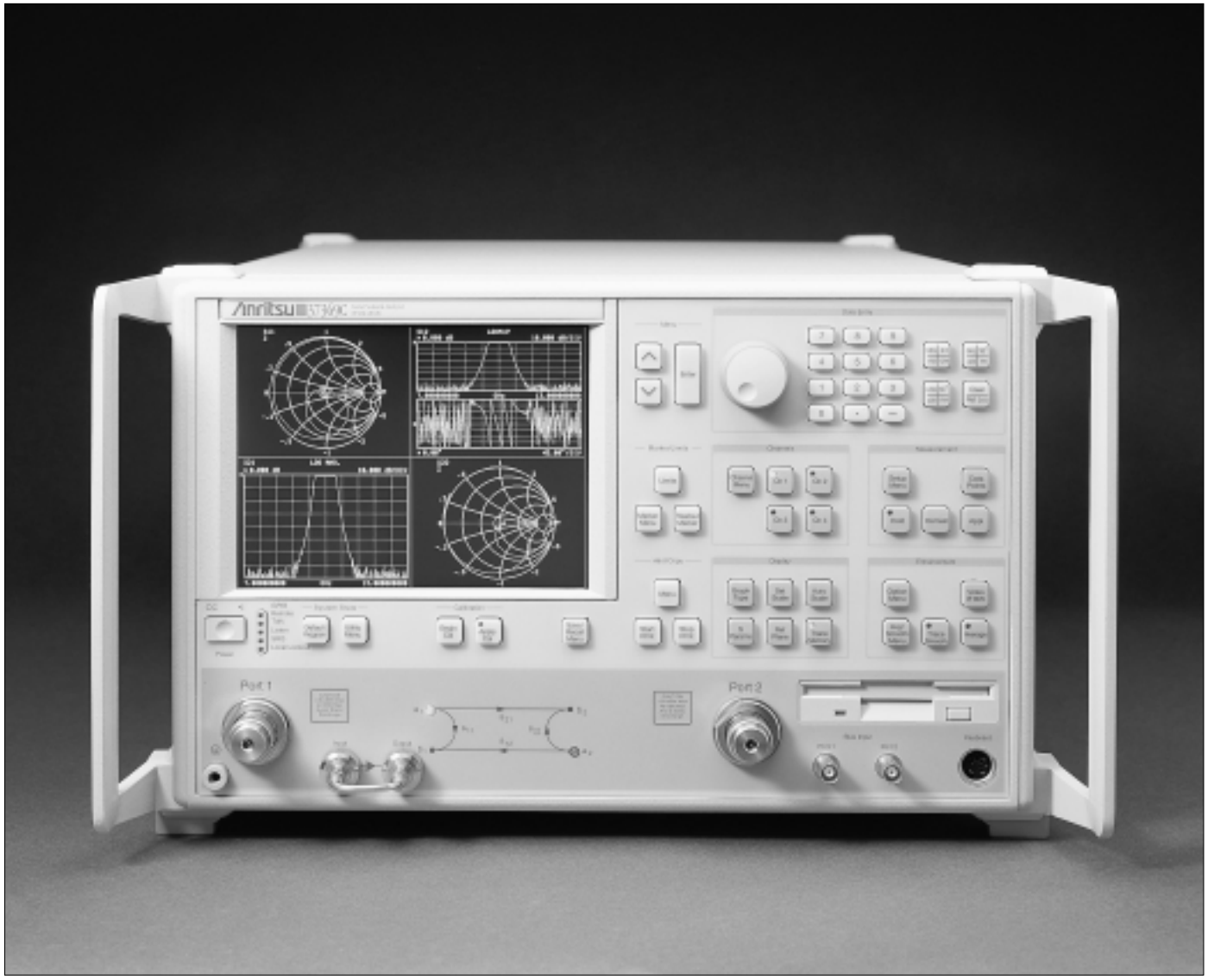
This appendix contains a copy of the 37100C/37200C/*37300C Vector Network Analyzers Technical Data Sheet*, Anritsu part number 11410-00247. This data sheet provides performance specifications for all of the various models in the series.

Anritsu

37100C/37200C/37300C

Vector Network Analyzers

Technical Data Sheet



Vector Network Analysis up to 65 GHz

SYSTEM DESCRIPTION

The Lightning 37200C/37300C Vector Network Analyzers (VNAs) are high performance tools designed to make fast and accurate S-parameter measurements of active and passive devices across the 22.5 MHz to 65 GHz range. These network analyzers integrate a synthesized source, S-parameter test set and tuned receiver into a single compact package that is ideal for bench-top testing.

The Lightning 37100C VNAs are configured as Direct-Access Receivers for antenna, frequency conversion, and multiple output device measurements. These network analyzers consist of a synthesized source and tuned receiver in a single compact unit, with direct access provided to all four receiver samplers via the front panel. The 37100C offers the ultimate flexibility to meet most receiver measurement needs, while maintaining the ability to measure all four S-parameters with the addition of a reflectometer setup at the front end of the receiver.

Specifications for the 37100C/37200C/37300C models are detailed on the following pages.

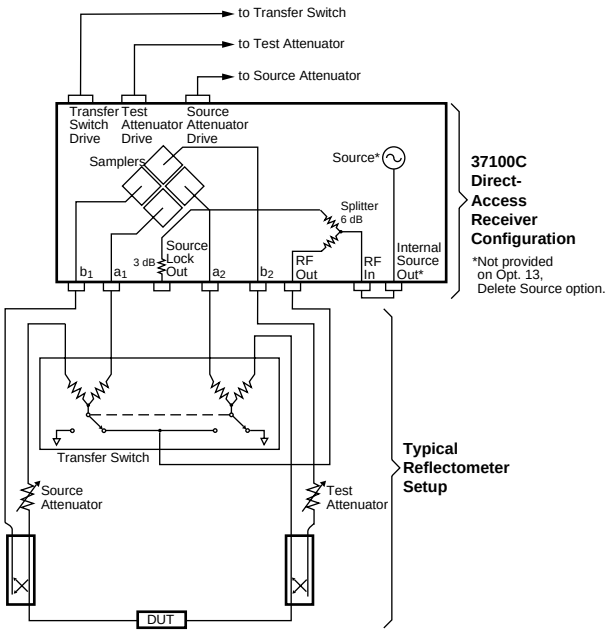
Model Numbers	Frequency Range
37225C, 37325C	40 MHz to 13.5 GHz
37147C	22.5 MHz to 20 GHz
37247C, 37347C	40 MHz to 20 GHz
37169C	22.5 MHz to 40 GHz
37269C, 37369C	40 MHz to 40 GHz
37277C, 37377C	40 MHz to 50 GHz
37297C, 37397C	40 MHz to 65 GHz

High throughput measurements are achieved in each model through the use of fast, 12-term error corrected sweeps, fast GPIB data transfers and an intuitive user interface. All measurement results are displayed on a large LCD color display or on an external VGA monitor.

For maximum productivity, the VNAs include as standard features:

- ✓ Fast Sweeping Synthesized Source
- ✓ Auto Reversing Test Set (37200C/37300C models only)
- ✓ Solid-State Transfer Switch (37200C/37300C models only)
- ✓ Four Independent Display Channels
- ✓ Multiple Source Control of Two External Sources
- ✓ Four Channel Receiver
- ✓ Internal Hard and Floppy Disk Drives
- ✓ LRL/LRM Calibration
- ✓ Adapter Removal Calibrations
- ✓ Fast Measurement Throughput via GPIB
- ✓ Built-In AutoCal® Control

Each of the network analyzers is designed for easy upgradeability. Any version of the 37000C VNA can be upgraded to accommodate new capabilities or additional frequency ranges by ordering the appropriate upgrade kit. 37100C to 37200C or 37200C to 37300C upgrades are also supported.



A Reflectometer test set is available as a special option for the 37100C. It contains the transfer switch, both attenuators and couplers. It also offers two bias tees and a front panel amplifier loop for active device testing. As compared to a 37300C VNA, the output power and hence the dynamic range are degraded by 10 dB typically.

SYSTEM PERFORMANCE

Dynamic Range:

The tables on the next page provide two definitions of dynamic range:

"Receiver Dynamic Range" is defined as the difference between the maximum signal level at Port 2 (or at any sampler input: a_1, a_2, b_1, or b_2 for a 37100C) for 0.1 dB compression and the noise floor.

"System Dynamic Range" is defined as the difference between the power incident on Port 2 in a through line connection and the noise floor.

In preparing the tables, 10 Hz IF bandwidth and 512 averages were used in calibration and measurement.

High Level Noise (typical): <0.04 dB and <0.5 degrees peak-to-peak variation in a 1 kHz IF bandwidth up to 20 GHz, <0.08 dB and <1.0 degrees peak-to-peak variation up to 40 GHz, <0.25 dB and <2.5 degrees peak-to-peak variation up to 65 GHz.

Dynamic Range (37100C)

Model	Frequency (GHz)	Maximum Signal Into a_x, b_x (dBm)	Noise Floor (dBm)	Receiver Dynamic Range (dB)	Source Power (dBm, Typical)
37147C	0.0225 2 20	-18 -12 -12	-122 -106 -103	104 94 91	10 8 5
37169C	0.0225 2 20 40	-18 -12 -12 -15	-122 -106 -103 -100	104 94 91 85	10 8 3 -3

Dynamic Range (37200C/37300C)

Model	Frequency (GHz)	Max. Signal Into Port 2 (dBm)	Noise Floor (dBm)	Receiver Dynamic Range (dB)	Port 1 Power (dBm, Typical)	System Dynamic Range (dB)*
37225C	0.04 2 13.5	+20 +3 +3	-70 -98 -98	90 101 101	0 0 0	70 98 98
37247C	0.04 2 20	+20 +3 +3	-70 -98 -96	90 101 99	0 0 0	70 98 96
37269C	0.04 2 20 40	+20 +3 +3 +3	-70 -98 -95 -93	90 101 98 96	0 0 -5 -15	70 98 90 78
37277C	0.04 2 20 40 50	+20 +3 +3 +3 +3	-77 -105 -97 -95 -87	97 108 100 98 90	0 +5 -2 -7 -2	77 110 95 88 85
37297C	0.04 2 20 40 50 65	+20 +3 +3 +3 +3 +3	-77 -105 -97 -95 -87 -77	97 108 100 98 90 80	0 +5 -2 -7 -2 -2	77 110 95 88 85 75
37325C	0.04 2 13.5	+30 +30 +30	-65 -93 -93	95 123 123	+5 +5 +5	70 98 98
37347C	0.04 2 20	+30 +30 +30	-65 -93 -91	95 123 121	+5 +5 +5	70 98 96
37369C	0.04 2 20 40	+30 +30 +30 +30	-65 -93 -90 -83	95 123 120 113	0 +5 0 -7	70 98 90 76
37377C	0.04 2 20 40 50	+30 +30 +30 +30 +30	-77 -105 -97 -95 -87	107 135 127 125 117	0 +5 -2 -7 -2	77 110 95 88 85
37397C	0.04 2 20 40 50 65	+30 +30 +30 +30 +30 +30	-77 -105 -97 -95 -87 -77	107 135 127 125 117 107	0 +5 -2 -7 -2 -2	77 110 95 88 85 75

*System Dynamic Range is based on the typical Port 1 power and specified noise floor at the indicated frequency range.

Test Port Characteristics

The specifications in the table below apply when the proper Model 34U Universal Test Port Adapters are connected, with or without phase equal insertables, to the test set ports and calibrated with the appropriate calibration kit at 23 ± 3°C using the OSL calibration method with a sliding load to achieve 12-term error correction (90 min. warm-up time is recommended).

Connector	Frequency (GHz)	Directivity (dB)	Source Match (dB)	Load Match (dB)	Reflection Frequency Tracking (dB)	Transmission Frequency Tracking (dB)	Isolation (dB)
GPC-7	0.0225 2 18	>52 >52 >52	>44 >44 >42	>52 >52 >52	±0.003 ±0.003 ±0.004	±0.004 ±0.004 ±0.012	>105 >115 >112
GPC-7 LRL Calibration	2 8	>60 >60	>60 >60	>60 >60	±0.001 ±0.001	±0.001 ±0.001	>115 >112
N-Type*	0.0225 2 18	>46 >44 >40	>36 >36 >32	>46 >44 >40	±0.004 ±0.004 ±0.005	±0.004 ±0.004 ±0.012	>105 >115 >112
3.5mm	0.0225 2 20 26.5	>44 >44 >44 >44	>40 >40 >38 >34	>44 >44 >44 >44	±0.005 ±0.005 ±0.006 ±0.006	±0.030 ±0.030 ±0.050 ±0.070	>105 >115 >110 >102
K	0.0225 2 20 40	>42 >42 >42 >38	>40 >40 >38 >34	>42 >42 >42 >38	±0.005 ±0.005 ±0.006 ±0.006	±0.030 ±0.050 ±0.070 ±0.080	>105 >115 >110 >100
V	0.04 2 20 40 50 65	>40 >40 >40 >36 >34 >34	>36 >36 >36 >32 >30 >28	>40 >40 >40 >36 >34 >34	±0.050 ±0.050 ±0.060 ±0.060 ±0.080 ±0.100	±0.030 ±0.050 ±0.070 ±0.080 ±0.100 ±0.120	>105 >115 >110 >100 >90 >80

*Standard OSL calibration, sliding load not required.

Measurement Throughput: Measurement times are based on a single 40 MHz to 20 GHz sweep with 10 kHz IF bandwidth (no averages) after a full 12-term calibration. Sweep times include retrace and band switch times.

Measurement Time (ms) vs. Data Points (typical)

Calibration Type	Data Points				
	3	51	101	401	1601
1 Port (3 Term)	75	270	350	920	3000
2 Port (12 Term)	60	250	340	920	3000

Measurement Time vs. Sweep Mode for 101 Data Points (typical)

Sweep Mode	Time (ms)
Linear	350
List	350
CW	190

Measurement Time vs. IF BW for 101 Data Points (typical)

IF Bandwidth	Time (ms)
10 kHz	180
1 kHz	270
100 Hz	1100
10 Hz	7300

Measurement Time vs. Span for 101 Data Points (typical)

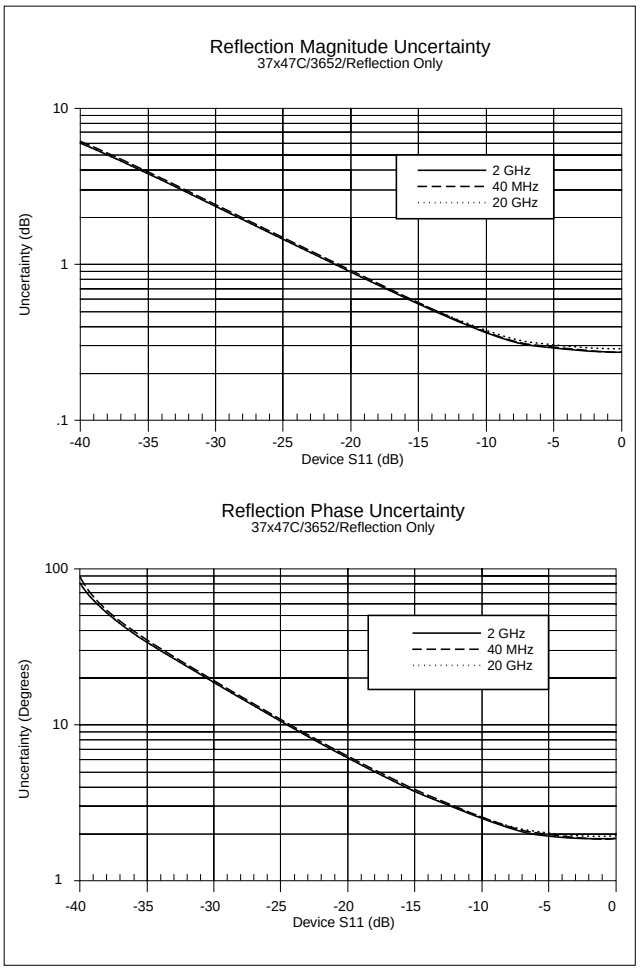
Frequency Span	Time (ms)
40 MHz to 65 GHz	900
40 MHz to 40 GHz	450
20 GHz to 40 GHz	340
10 GHz to 11 GHz	220

MEASUREMENT UNCERTAINTY

The following graphs give measurement uncertainty after 12-Term vector error correction. The errors are worst case contributions of residual directivity, load and source match, frequency response, isolation, network analyzer dynamic accuracy, and connector repeatability. In preparing the following graphs, 10 Hz IF bandwidth and averaging of 512 points were used. Changes in the IF bandwidth or averaging can result in variations at low levels.

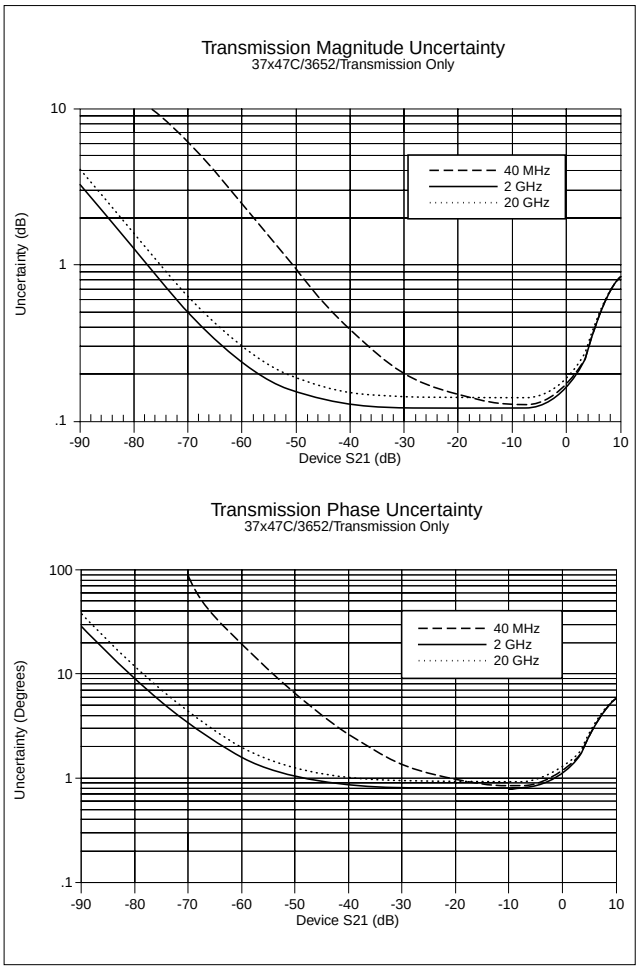
Models 37x47C Series (K-Connectors)

Reflection Measurements:



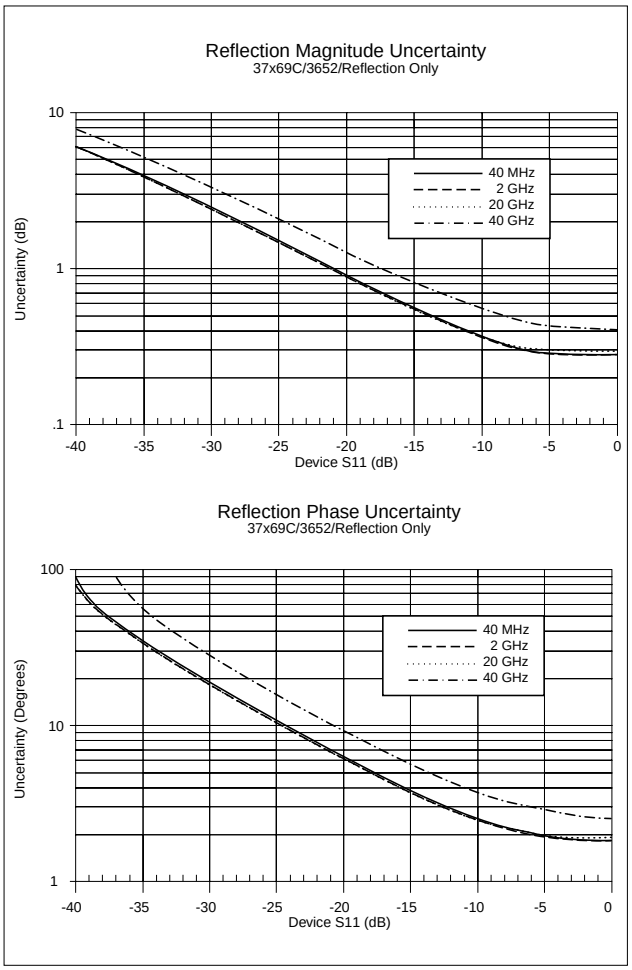
Models 37x47C Series (K-Connectors)

Transmission Measurements:



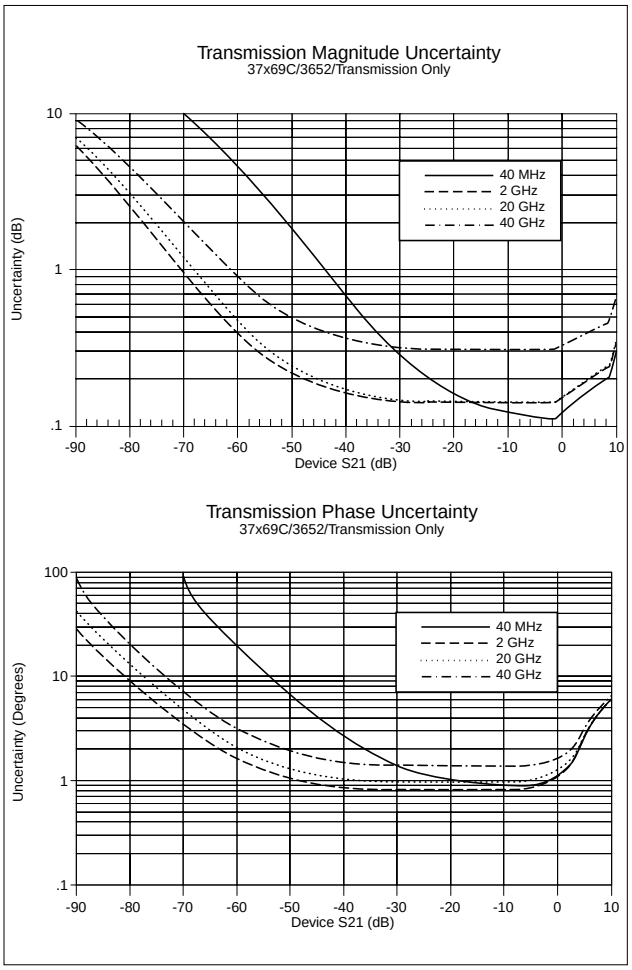
Models 37x69C Series (K-Connectors)

Reflection Measurements:



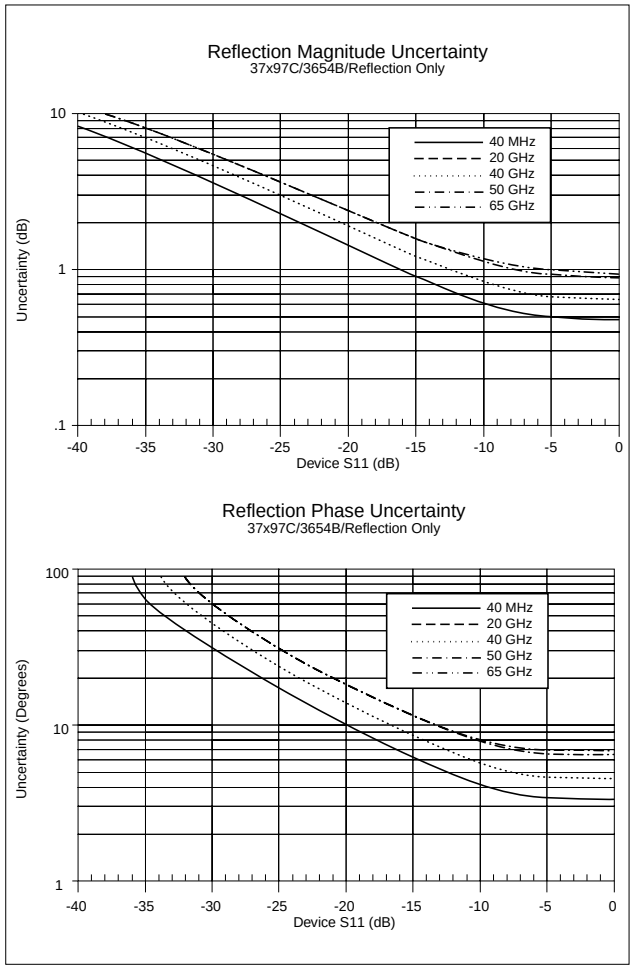
Models 37x69C Series (K-Connectors)

Transmission Measurements:



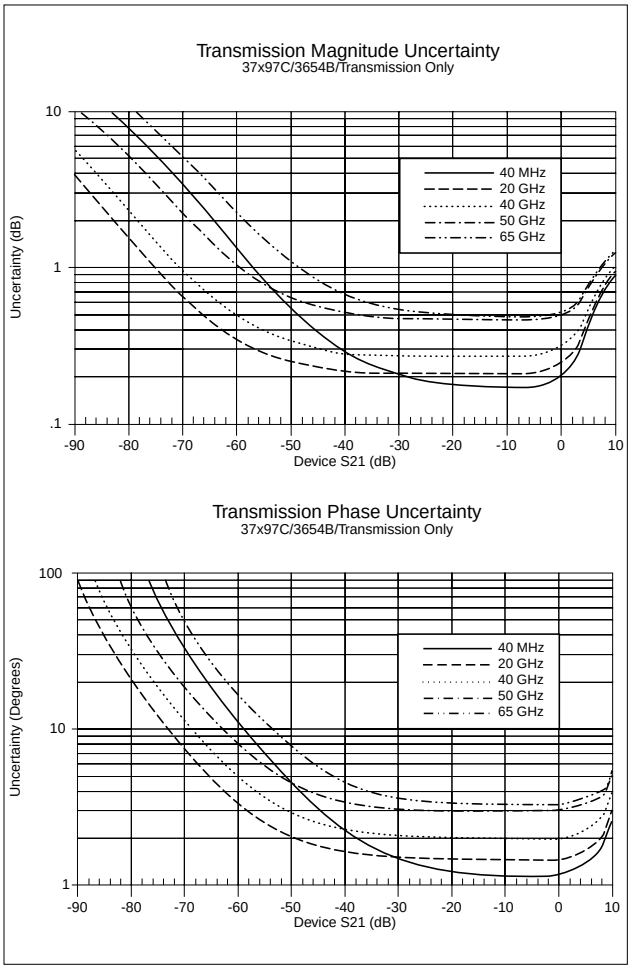
Model 37x77C and 37x97C (V-Connectors)

Reflection Measurements:



Model 37x77C and 37x97C (V-Connectors)

Transmission Measurements:



MEASUREMENT CAPABILITIES

Number of Channels: Four independent measurement channels.

Parameters: S11, S21, S22, S12, or user defined combinations of a1, a2, b1, and b2. All measurements are made without the need to manually reverse the test device. For the 37100C models, a reflectometer setup at the front end of the receiver is required for S-measurements (See diagram on page 2).

Measurement Frequency Range: Frequency range of the measurement can be narrowed within the calibration range without recalibration. CW mode permits single frequency measurements, also without recalibration.

Domains: Frequency Domain, CW Draw, and optional High Speed Time (Distance) Domain.

Formats: Log Magnitude, Phase, Log Magnitude and Phase, Smith Chart (Impedance), Smith Chart (Admittance), Linear Polar, Log Polar, Group Delay, Linear Magnitude, Linear Magnitude and Phase, Real, Imaginary, Real and Imaginary, SWR and Power.

Data Points: 1601 maximum. Data points can be switched to a value of 801, 401, 201, 101 or 51 points without recalibration (if 1601 points were used in the calibration). In addition, the system accepts an arbitrary set of N discrete data points where $2 \leq N \leq 1601$. CW mode permits selection of a single data point without recalibration.

Reference Plane: Can be entered in time or in distance (when the dielectric constant is entered). Automatic reference plane feature adds the correct electrical length (delay) compensation at the push of a button. Software compensation for the electrical length difference between reference and test is always accurate and stable since measurement frequencies are always synthesized. In addition, the system compensates reference phase delay for dispersive transmission media, such as waveguide and microstrip.

Markers: Six independent markers can be used to read out measurement data. In delta-reference mode, any one marker can be selected as the reference for the other five. Markers can be directed automatically to the minimum or maximum of a data trace.

Enhanced Markers: Marker search for a level or bandwidth, displaying an active marker for each channel, and discrete or continuous (interpolated) markers.

Marker Sweep: Sweeps upward in frequency between any two markers. Recalibration is not required during the marker sweep.

Limit Lines: Either single or segmented limit lines can be displayed. Two limit lines are available for each trace.

Single Limit Readouts: Interpolation algorithm determines the exact intersection frequencies of test data and limit lines.

Segmented Limits: A total of 20 segments (10 upper and 10 lower) can be generated per data trace. Complete segmented traces can be offset in both frequency and amplitude.

Test Limits: Both single and segmented limits can be used for PASS/FAIL testing. The active channel's PASS or FAIL status is indicated on the display after each sweep. In addition, PASS/FAIL status is output through the rear panel I/O connector as selectable TTL levels (PASS=0V, FAIL=+5V or PASS=+5V, FAIL=0V).

Tune Mode: Tune Mode optimizes sweep speed in tuning applications by updating forward S-parameters more frequently than reverse ones. This mode allows the user to select the ratio of forward sweeps to reverse sweeps after a full 12-term calibration. The ratio of forward sweeps to reverse sweeps can be set anywhere between 1:1 and 10,000:1.

Data Averaging: 1 to 4096 averages can be selected. A front-panel button turns data averaging on/off, and an LED indicates when averaging is active.

Video IF Bandwidth: Front panel button selects four levels of video IF bandwidth: MAXIMUM (10 kHz), NORMAL (1 kHz), REDUCED (100 Hz) and MINIMUM (10 Hz).

Trace Smoothing: Computes an average over a percentage range of the data trace. The percentage of trace to be smoothed can be selected from 0 to 20%. Front-panel button turns smoothing on/off, and an LED indicates when smoothing is active.

Group Delay Aperture: Defined as the frequency span over which the phase change is computed at a given frequency point. The aperture can be changed without recalibration. The minimum aperture is the frequency range divided by the number of points in calibration and can be increased to 20% of the frequency range without recalibration. The frequency width of the aperture and the percent of the frequency range are displayed automatically.

Group Delay Range: The maximum delay range is limited to measuring no more than +180° of phase change within the aperture set by the number of frequency points. A frequency step size of 100 kHz corresponds to 10 ms.

DISPLAY CAPABILITIES

Measurement Channels: Four independent channels are available to display any S-parameter or user defined parameter, in any format, with up to two traces per channel for a maximum of eight traces simultaneously. A single channel, two channels (1 and 3, or 2 and 4), or all four channels can be displayed simultaneously. Channels 1 and 3, or channels 2 and 4 can be overlaid.

Display: Color LCD, 8.5" diagonal.

Display Colors: The color of data traces, memory, text, markers and limit lines are all user definable.

Trace Overlay: Displays two data traces on the active channel's graticule simultaneously.

Trace Memory: A separate memory for each channel can be used to store measurement data for later display or subtraction, addition, multiplication or division with current measurement data.

Scale Resolution (minimum per division):

Log Magnitude: 0.001 dB
Linear Magnitude: 1 pU
Phase: 0.01°
Group Delay: 0.001 ps
Time: 0.001 ms
Distance: 0.1 μm
SWR: 1 pU
Power: 0.01 dB

Autoscale: Automatically sets Resolution and Offset to fully display measurement data.

Reference Position: Can be set at any graticule line.

Annotation: Type of measurement, vertical and horizontal scale resolution, start/stop or center/span frequencies, and reference position.

Blank Frequency Information: Blanking function removes all references to frequencies on the display. Frequency references can only be restored through a system reset or GPIB command.

SIGNAL SOURCE CAPABILITIES

Frequency Resolution: 1 kHz (standard on all models)

Frequency Stability:

Aging: <1 x 10^{-9}/day
Stability: <5 x 10^{-9} over 0˚ to +55˚C range

Source Power Level: The source power (dBm) may be set from the front panel menu or via GPIB. Check the graphs and tables on the following pages for the range.

In addition, on 37300C models, the port 1 power may be attenuated in 10 dB steps, using the internal 70 dB (60 dB for 37377C and 37397C) step attenuator. Similarly, high input signals into port 2, not exceeding 1 watt, can be attenuated up to 40 dB, using the internal port 2 step attenuator.

Power Accuracy: ±0.5 dB at 2 GHz at default power

Power Meter Correction: The 37000C offers a user-selectable feature that corrects for test port power variations and slope (on Port 1) using an external power meter. Power meter correction is available at a user-selectable power level, if it is within the power adjustment range of the internal source. Once the test port power has been flattened, its level may be changed within the remaining power adjustment range of the signal source.

Set-On Receiver Mode: The 37300C can be configured to measure the relative harmonic level of test devices with Set-On Receiver Mode capability. The 37300C's unique phase locking scheme allows it to operate as a tuned receiver by locking all of its local oscillators to its internal crystal reference oscillator. Set-On Receiver Mode capability significantly increases the versatility of the 37300C VNA in applications that check for harmonics, intermodulation products, and signals of known frequency.

Multiple Source Control Capability: Multiple Source Control capability allows a user to independently control the frequencies of two sources and the receiver without the need for an external controller. The frequency ranges and output powers of the two sources may be specified. A frequency sweep may be comprised of up to five separate bands, each with independent source and receiver settings, for convenient testing of frequency translation devices such as mixers. Up to five sub-bands may be tested in one sweep. This feature enables users to easily test mixers, up/down converters, multipliers, and other frequency conversion devices.

Source #1: The 37000's internal source, or any of the 68XXXC, 69XXXB, 6700B or MG369XA synthesizers

Source #2: Any of the 68XXXC, 69XXXB, 6700B or MG369XA synthesizers

Sweep Type: Linear, CW, Marker, or N-Discrete point sweep

Spurious Response (Harmonics):

15 dBc (37277C, 37297C, 37325C, 37347C, 37369C, 37377C, 37397C) at maximum rated power
35 dBc (all other models) at maximum rated power

Spurious Response (Nonharmonics):

35 dBc at maximum rated power

Phase Noise:

>60 dBc/Hz at 10 kHz offset and 20 GHz center frequency

Power Range*

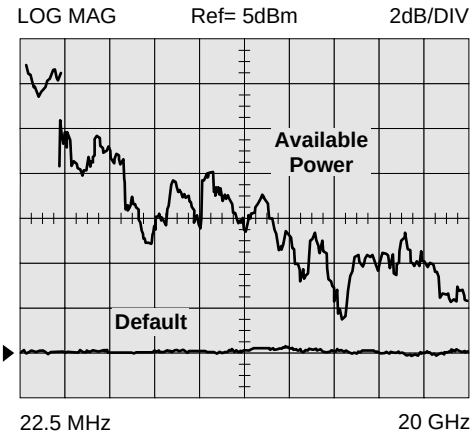
Model	Rated Power (dBm)	Minimum Power (dBm)	Resolution (dB)
37147C	+5	-15	0.05
37169C	-3	-23	0.05
37225C	0	-20	0.05
37247C	0	-20	0.05
37269C	-15	-27	0.05
37277C	-7	-27	0.05
37297C	-7	-19	0.05
37325C	+5	-90	0.05
37347C	+5	-90	0.05
37369C	-7	-97	0.05
37377C	-7	-87	0.05
37397C	-7	-79	0.05

Power Flatness

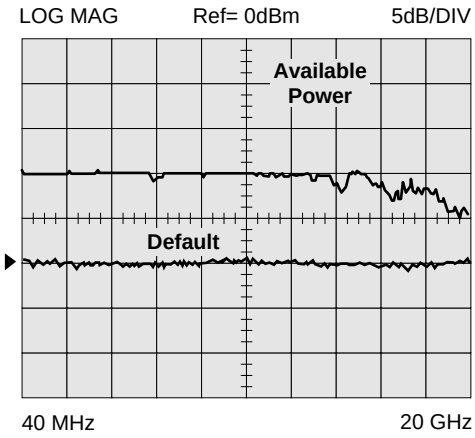
Frequency Range (GHz)	Flatness (dB)
0.0225 to 13.5	±1.5
13.5 to 20	±2.0
20 to 40	±3.0
40 to 65	±5.0

*Control Power for 37x25C, and 37x47C can be set to +10 dB but is not guaranteed. Similarly Control Power on the 37x69C, 37x77C, and 37x97C can be set to +20 dB but not guaranteed. Complete Control Power range also not guaranteed over temperature.

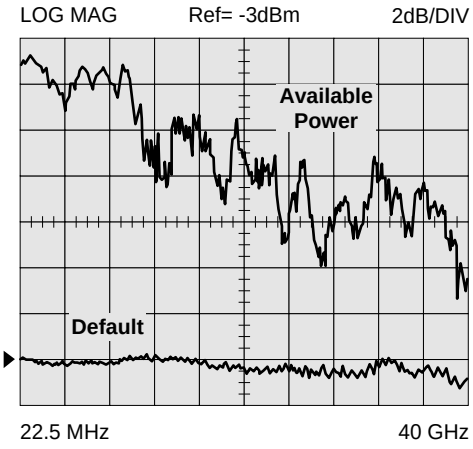
Available Source Power



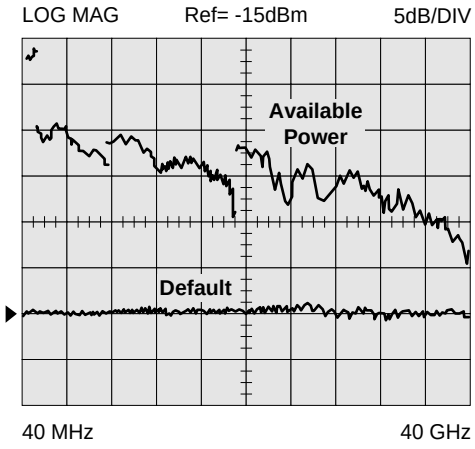
Model 37147C Source Power



Model 37225C and 37247C Source Power

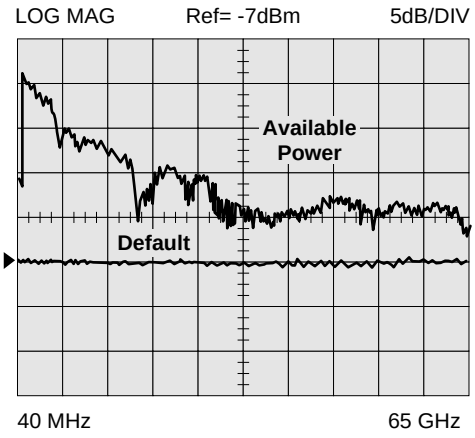


Model 37169C Source Power

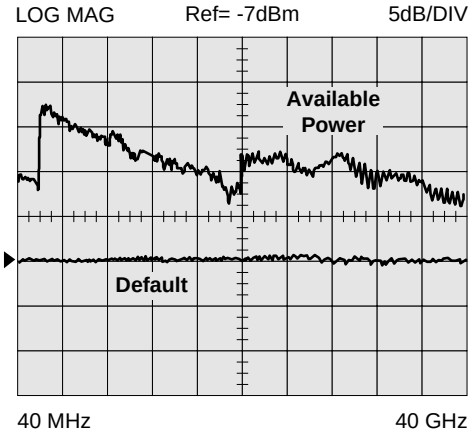


Model 37269C Source Power

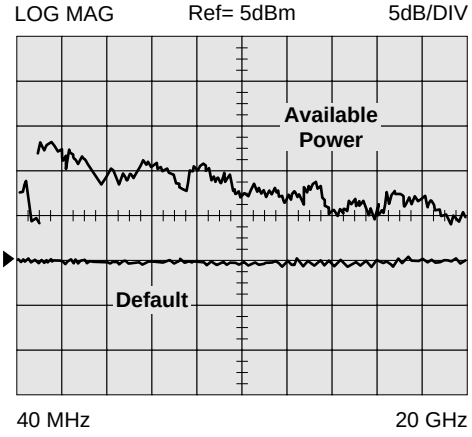
Available Source Power



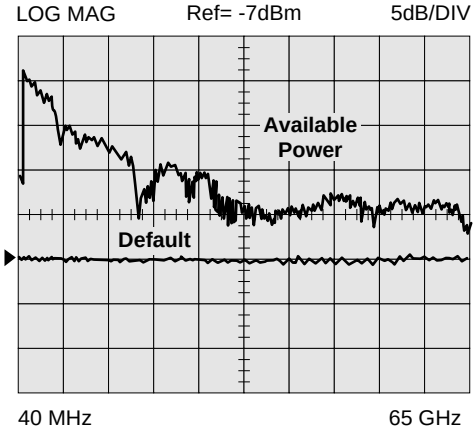
Model 37277C and 37297C Source Power



Model 37369C Source Power



Model 37325C and 37347C Source Power



Model 37377C and 37397C Source Power

VECTOR ERROR CORRECTION

There are five built-in methods of calibration:

1) **Open-Short-Load-Thru (OSLT):** This calibration method uses short circuits, open circuits, and terminations (fixed or sliding).
2) **Offset-Short (waveguide):** This calibration method uses short circuits and terminations.
3) **LRL/LRM:** The Line-Reflect-Line (LRL) or Line-Reflect-Match (LRM) calibration uses transmission lines and a reflective device or termination (LRM).
4) **TRM:** The Thru-Reflect-Match calibration uses short circuits and fixed termination.
5) **AutoCal®:** This calibration method uses an automatic calibrator module.

There are four vector error correction models available for calibration:

1) **Full 12-Term**
2) **One Path/Two Port**
3) **Frequency Response**
4) **Reflection Only**

Full 12-Term can be used for all models that automatically reverse the test signal. The front-panel display indicates the type of calibration stored in memory. A front-panel button selects whether calibration is to be applied, and an LED lights when error correction data is being applied.

Calibration Sequence: Prompts the user to connect the appropriate calibration standard to Port 1 and/or Port 2. Calibration standards may be measured simultaneously or one at a time.

Calibration Standards: For coaxial calibrations the user selects SMA, 3.5 mm, GPC-7, Type N, 2.4 mm, TNC, K, V connector or special type from the calibration menu. Use of fixed or sliding loads can be selected for each connector type. User defined calibration standards allow for entry of open capacitance, load and short inductances, load impedance, and reflection standard offset lengths.

Reference Impedance: It is possible to modify the reference impedance of the measurement to other than 50Ω (but not 0).

AutoCal®: The VNA can internally control an external AutoCal module to perform a 2-port OSLT calibration. AutoCal is a single two port calibration module with built-in, switched, and characterized OSLT standards. AutoCal provides quick, reliable, and accurate calibrations that exceed the performance of a standard broadband load OSLT calibration.

LRL/LRM Calibration: The LRL calibration technique uses the characteristic impedance of a length of transmission line as the calibration standard. A full LRL calibration consists merely of two transmission line measurements, a high reflection measurement, and an isolation measurement. The LRM calibration technique is a variation of the LRL technique that utilizes a precision termination rather than a second length of transmission line. A third optional standard, either Line or Match, may be measured in order to extend the frequency range of the calibration. This extended calibration range is achieved by mathematically concatenating either two LRL, two LRM, or one LRL and one LRM calibration(s). Using these techniques, full 12-Term error correction can be performed on the 37000C models.

Adapter Removal Calibration: Built-in Adapter Removal application software accurately characterizes and "removes" any adapter used during calibration that will not be used for subsequent device measurements. This technique allows for accurate measurement of non-insertable devices.

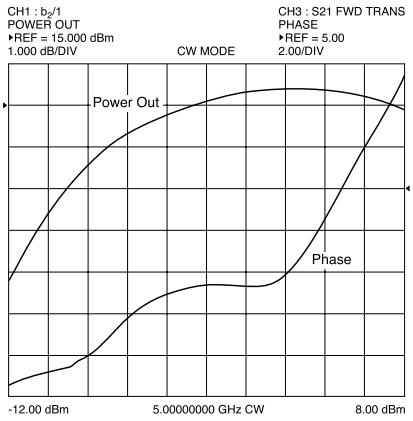
Dispersion Compensation: Selectable as Coaxial (non-dispersive), Waveguide, or Microstrip (dispersive).

GAIN COMPRESSION MEASUREMENT CAPABILITY (37300C models only)

The 37300C simplifies amplifier Gain Compression and AM/PM measurements. Once an appropriate power and frequency schedule is selected, a power meter calibration, at a set level, will calibrate the linear VNA receiver channels, to accurately measure power in dBm. The 37300C supports the Anritsu, Giga-tronics, and Agilent power meters. To measure power, $b_2/1$, a user defined parameter, is automatically selected.

Swept Power Gain Compression: The 37300C will display traditional Power out vs. Power in or Phase vs. Power in, at one of up to 10 selectable frequencies. A separate screen will easily show Power out and Power in at 1 dB, or selected level Gain Compression, for all entered frequencies (See figure below).

Swept Frequency Gain Compression: Once Gain is measured at the starting power, the user increments Power in, observing Normalized Gain vs. Frequency. This aids in analyzing the most critical compression frequencies of a broadband amplifier.



Power Out and Phase performance as a function of Input Power at a CW frequency.

HIGH SPEED TIME (DISTANCE) DOMAIN MEASUREMENT CAPABILITY (OPTION 2)

Option 2A, High Speed Time (Distance) Domain software allows the conversion of reflection or transmission measurements from the frequency domain to the time domain. Measured S-parameter data is converted to the time domain by application of a Fast Fourier Transform (FFT) using the Chirp Z-Transform technique. Prior to conversion, any one of several selectable windowing functions may be applied. Once the data is converted to the time domain, a gating function may be applied to select the data of interest. The processed data may then be displayed in the time domain with display start and stop times selected by the user or in the distance domain with display start and stop distance selected by the user. The data may also be converted back to the frequency domain with a time gate to view the frequency response of the gated data.

Lowpass Mode: This mode displays a response equivalent to the classic "TDR" (Time Domain Reflectometer) response of the device under test. Lowpass response may be displayed in either the impulse or step mode. This type of processing requires a sweep over a harmonic series of frequencies and an extrapolated or user-entered DC value.

Bandpass Mode: This mode displays a response equivalent to the time response of the device under test to a band limited impulse. This type of processing may be used with any arbitrary frequency sweep range, limited only by the test set range or device under test response.

Phasor Impulse Mode: This mode displays a response similar to the Lowpass impulse response, using data taken over an arbitrary (band limited) sweep range. Detailed information, similar to that contained in the lowpass impulse response may be used to identify the nature of impedance discontinuities in the device under test. Now, with Phasor Impulse, it is possible to characterize complex impedances on band-limited devices.

Windowing: Any one of four window functions may be applied to the initial frequency data, to counteract the effects of processing data with a finite bandwidth. These windows provide a range of trade offs of main lobe width versus sidelobe level (ringing). The general type of function used is the Blackman-Harris window with the number of terms being varied from one to four. Typical performance follows:

Type of Window (Number of Terms)	First Side Lobe Relative to Peak	Impulse Width[1]
Rectangle (1)	-13 dB	1.2W
Nominal-Hamming (2)	-43 dB	1.8W
Low Side Lobe, Blackman-Harris (3)	-67 dB	2.1W
Minimum Side Lobe, Blackman-Harris (4)	-92 dB	2.7W

[1]W(Bin Width) = 1/2Δf sweep width.
Example. When Δf = 40 MHz to 40 GHz, W = 12.5 ps
When Δf = 40 MHz to 65 GHz, W = 7.7 ps

Gating: A selective gating function may be applied to the time domain data to remove unwanted responses, either in a pass-band or reject-band (mask). This gating function may be chosen as the convolution of any of the above window types with a rectangular gate of user defined position and width. The gate may be specified by entering start and stop times or center and span. The gated data may be displayed in the time domain, or converted back to the frequency domain.

Time Domain Display: Data processed to time domain may be displayed as a function of time or as a function of distance, provided the dielectric constant of the transmission media is entered correctly. In the case of dispersive media such as waveguide or microstrip, the true distance to a discontinuity is displayed in the distance mode. The time display may be set to any arbitrary range by specifying either the start and stop times or the center time and span. The unaliased (non-repeating) time range is given by the formula:

$$\text{Unaliased Range (ns)} = \frac{\text{Number of Frequency Data Points}}{\text{Frequency Sweep Range (GHz)}}$$

The resolution is given by the formula:

$$\text{Main Lobe Width (null–null) in ns} = \frac{kW}{\text{Freq. Sweep Range (GHz)}}$$

where kW is two times the number of window terms (for example, four for a two-term window)

For a 40 GHz sweep range with 1601 data points, the unaliased range is 40.025 nanoseconds. For a 65 GHz sweep with 1601 data points, the unaliased range is 24.646 nanoseconds.

Frequency with Time Gate: Data that has been converted to time domain and selected by the application of gating function may be converted back to the frequency domain. This allows the display of the frequency response of a single element contained in the device under test. Frequency response accuracy is a function of window and gate type, and gate width. For a full reflection, minimum gate and window accuracy is within 0.2 dB of the ungated response over a 40 GHz range.

ELECTRO-OPTICAL MEASUREMENT CAPABILITY (standard on all 37200/37300 models)

The 37200C/37300C series incorporated a de-embedding function that simplifies VNA calibration when measuring E/O and O/E devices. Characterize the transfer function, group delay, and return loss of optical modulators (E/O) and photo-receivers (O/E) using the built-in application.

E/O Measurements: The application menus guide the user through the entire calibration and setup. A characterized photo-diode (O/E) reference and a laser source are required to complete the test setup. The internal VNA application de-embeds the response of the photo-diode reference to allow direct measurement of the bandwidth and return loss of the modulator.

O/E Measurements: Photo-receiver measurements can be made by characterizing a modulator first and then using it as a transfer standard for the O/E measurement. The internal application de-embeds the response of the modulator to allow characterization of the photo-receiver.

GPIB

GPIB INTERFACES: 2 Ports, system GPIB and dedicated GPIB

System GPIB (IEEE-488.2): Connects to an external controller for use in remote programming of the network analyzer. Address can be set from the front panel and can range from 1 to 30.

Dedicated GPIB: Connects to external peripherals for network analyzer controlled operations (e.g., GPIB plotters, frequency counters, frequency synthesizers and power meters).

Interface Function Codes: SH1, AH1, T6, TE0, L4, LE0, SR1, RL1, PP1, DT1, DC0, and C0.

GPIB Data Transfer Formats: ASCII, 32-bit floating point, or 64-bit floating point. 32-bit and 64-bit floating point data can be transferred with LSB or MSB first.

GPIB Data Transfer Speed (with or without cal): 150 kbyte/sec

GPIB Data Throughput Time: Throughput measurements for both tables were made as follows: start the timer, trigger a sweep, wait for a full sweep, transfer data across the GPIB and stop the timer. Data throughput times are shown separately for measurements made without calibration and with full two-port, 12-Term calibration. Measurement conditions: 40 MHz to 20 GHz sweep, single channel, log magnitude display, 10 kHz IF bandwidth, and output final data.

Throughput Times (ms) without Correction (typical)

Data Format	3 Points*	101 Points	401 Points	1601 Points
32 Bit	150	500	1200	3600
64 Bit	150	500	1200	3600
ASCII	150	600	1500	4400

*3 data point sweeps taken at 2, 4, and 6 GHz

Throughput Times (ms) with 12-Term Correction (typical)

Data Format	3 Points*	101 Points	401 Points	1601 Points
32 Bit	190	950	2300	6900
64 Bit	190	950	2300	6900
ASCII	190	1000	2500	7400

*3 data point sweeps taken at 2, 4, and 6 GHz

Fast CW Operation: Fast CW is an ideal mode of operation for rapid data taking over GPIB. To achieve a fast measurement rate the display is not updated and only the raw S-parameter or user-defined parameter of the active channel is measured.

Fast CW Typical Performance

Trigger Mode	Measurement Speed (ms/point)
GPIB	1.5
External TTL	1.2
Internal	0.8

Internal Buffer Data Collection: Internal Buffer Data Collection is provided to allow saving active channel measurement data from multiple sweeps without having to synchronize and collect data at the end of each sweep. The 37000C can store up to 50,000 data point measurements, each consisting of two (real and imaginary) IEEE 754 4-byte floating point numbers. GPIB transfer speed for the 50,000 data points is typically 2.2 seconds.

STORAGE

Internal Memory: Ten front panel states (no calibration) can be stored and recalled from non-volatile memory locations. The current front panel setup is automatically stored in non-volatile memory at instrument power-down. When power is applied, the instrument returns to its last front panel setup.

Internal Hard Disk Drive: 340 MB mininum, used to store and recall measurement and calibration data and front-panel setups. All files are MS-DOS® compatible. File names can be 1 to 8 characters long, and must begin with a character, not a number. Extensions are automatically assigned.

External SCSI Interface: Option 4 deletes the internal hard disk drive, and adds a SCSI Interface connector to the rear panel for connecting a SCSI-2 formatted hard disk drive.

Internal Floppy Disk Drive: A 3.5-inch diskette drive with 1.44 Mbytes formatted capacity is used to load measurement programs and to store and recall measurement and calibration data and front-panel setups. Measurement data can be stored in text, S2P or bitmap format. All files are MS-DOS compatible. File names can be 1 to 8 characters long and must begin with a character, not a number. Extensions are automatically assigned.

Measurement Data: 102.8 kbytes per 1601 point S-parameter data file.

Calibration Data: 187.3 kbytes per 1601 point S-parameter data file (12-Term cal plus setup).

Trace Memory File: 12.8 kbytes per 1601 point channel.

HARD COPY

Printer: A menu selects full screen, graphical, tabular data, and printer type. The number of data points of tabular data can be selected as well as data at markers only. Compatible with most HP and Epson printers with parallel (Centronics) interfaces.

GPIB Plotter: The 37000 is compatible with most HP and Tektronix plotters. A menu selects plotting of full or user-selected portions of graphical data. The plotter is connected to the dedicated GPIB bus.

Performance: After selecting the Start Print button, front panel operation and measurement capability is restored to the user within two seconds.

INTERFACES

37000C Front Panel Connectors and Controls:

Keyboard Input: An IBM-AT compatible keyboard can be connected to the front panel for navigating through front panel menus, annotation of data files and display labels, printing displays and pausing instrument sweeps.

Test Ports (37200C and 37300C): Universal K male test ports are standard on all models except for the >40 GHz models which have Universal V male test ports as standard. For additional configurations check Test Port Converters (Option 7).

Bias Inputs, Port 1 and 2 (37300C): 0.5 amps maximum through BNC connectors.

Source Input Loop (37100C): Provides external source input capability, replacing the internal source.

RF Output (37100C): K, female, provides source RF output.

a_1, a_2, b_1, b_2 Inputs (37100C): K, female, provide inputs to the samplers.

Source Lock Output (37100C): Provides a sample of the internal source, at -9 dB (typical) relative to the internal source power.

Port 1 Amplifier Loop (37300C): Provides access to insert an external amplifier, ahead of the port 1 coupler or bridge, to increase port 1 power output, up to +30 dBm (1 watt) maximum.

37000C Rear Panel Connectors and Controls:

PRINTER OUT: Centronics interface for an external printer.

VGA OUT: Provides VGA output of 37000C video display.

SERIAL: 9-Pin male DSUB connector. Provides RS-232 serial port control for an AutoCal® module (3658 series).

10 MHz REF IN: Connects to external reference frequency standard, 10 MHz, +5 to -5 dBm, 50Ω, BNC female.

10 MHz REF OUT: Connects to internal reference frequency standard, 10 MHz, 0 dBm, 50Ω, BNC female.

EXT ANALOG OUT: -10V to +10V with 5 mV resolution, varying in proportion to user-selected data (e.g., frequency, amplitude). BNC female.

EXT ANALOG IN: ±50 volt input for displaying external signals on the LCD. BNC female.

LINE SELECTION: Power supply automatically senses 100V, 120V, 220V or 240V lines.

EXTERNAL TRIGGER: External TTL triggering for 37000C measurement. 10 kΩ input impedance, BNC female.

REFERENCE EXTENSION: The 37300C provides access to the a_1 and b_1 samplers as standard. The 37200C provides access to a_1 as an option. K female connectors are used, except for >40 GHz models where V female connectors are used.

EXTERNAL SCSI: Provides SCSI-2 connector for connection of an external SCSI hard disk drive (Option 4).

EXTERNAL I/O: 25-pin DSUB connector.

LIMITS PASS/FAIL: Selectable TTL levels (Pass=0V, Fail=+5V or Pass=+5V, Fail=0V. Additionally, 0 volts (all displayed channels pass) or +5V (any one of four displayed channels fail) output pass/fail status (1 line).

PORT 1 SOURCE ATTENUATOR (37100C): Drive signal for a source external programmable step attenuator.

PORT 2 TEST ATTENUATOR (37100C): Drive signal for a test external programmable step attenuator.

TRANSFER SWITCH (37100C): Drive signal for an external transfer switch.

GENERAL

Power Requirements: 85-240 volts, 48-63 Hz, 540 VA maximum

Dimensions: 267 H x 432 W x 585 D mm (10.5 H x 17 W x 23 D in.)

Weight: 27 kg (60 lb)-(2-man lift required)

Storage Temperature Range: -40°C to +75°C

Operating Temperature Range: 0°C to +50°C

Relative Humidity: 5% to 95% at +40°C

EMI: Meets the emissions and immunity requirements of EN55011/1991 Class A/CISPR-11 Class A

EN50082-1/1993

IEC 801-2/1984 (4 kV CD, 8 kV AD)
IEC 1000-4-3/1995 (3 V/m, 80-1000 MHz)
IEC 801-4/1988 (500V SL, 1000V PL)
IEC 1000-4-5/1995 (2 kV L-E, 1 kV L-L)

LRL/LRM-Calibration method of Rohde & Schwarz, Germany
GPC–7 is a registered trademark of Amphenol Corporation.
K Connector and V Connector are registered trademarks of Anritsu Company.
AutoCal is a registered trademark of Anritsu Company.



Sales Centers:
United States (800) ANRITSU
Canada (800) ANRITSU
South America 55 (21) 286-9141

Anritsu
Discover What's Possible®

Sales Centers:
Europe 44 (0) 1582 433433
Japan 81 (03) 3446-1111
Asia-Pacific 65-2822400

Microwave Measurements Division • 490 Jarvis Drive • Morgan Hill, CA 95037-2809
http://www.us.anritsu.com • FAX (408) 778-0239

Appendix D
ME7808A Broadband Measurement System Maintenance

Table of Contents

Appendix D ME7808A Broadband Measurement System Maintenance

D-1 INTRODUCTION

This appendix provides maintenance instructions for the ME7808A Broadband Measurement System. It describes Maintenance and Performance Verification of the ME7808A Broadband VNA system. This maintenance and verification is performed independently of any wafer-probe station. Models 37397C and 37297C are completely interchangeable in this system, and several models of synthesizers may be used with this system. All have identical operating characteristics within the ME7808A system, regardless of the labels in this appendix.

On early systems, many instruments were labeled with SM numbers, rather than typical Anritsu model designations. The operating characteristics of the SM units are identical in most cases to the operation of the newer models. The following SM numbers are supported by this appendix:

- SM5621 (modifications to the 37397C)
- SM5645 (3742A-EW Millimeter Module)
- SM5620 (3738A Test Set)
- SC6195 (57215, 57216 Couplers)

D-2 ME7808A OPERATING SOFTWARE

On early ME7808A systems, software installed into the 37397C was labeled as various versions of 3.6x. This was intended to be temporary software only and the 37397C BMS should be upgraded to at least version 4.00 to achieve best system performance.

D-3 SYSTEM DESCRIPTION

Figure D-3 (next page) shows the functional block diagram of the entire ME7808A system (excluding probe station). See Section D-8 Troubleshooting for more detailed information.

D-4 SYSTEM ADJUSTMENTS

Anritsu recommends that the system be readjusted and the performance be verified every 12 months. The 37397C instrument and the Synthesizers require adjustment (recalibration). The 3742A modules and the 3738A Test Set are not adjustable.

The 37397C instrument adjustments are performed with the system operating in the Internal mode (40 MHz to 65 GHz only). Refer to Chapter 6 of this manual for complete instructions on readjustment of the 37397C instrument.

Refer to the 68000C Maintenance Manual (part number 10370-10336) for adjustment and verification of those synthesizers.

Refer to the MG3690A Maintenance Manual (part number 10370-10355) for adjustment and verification of those synthesizers.

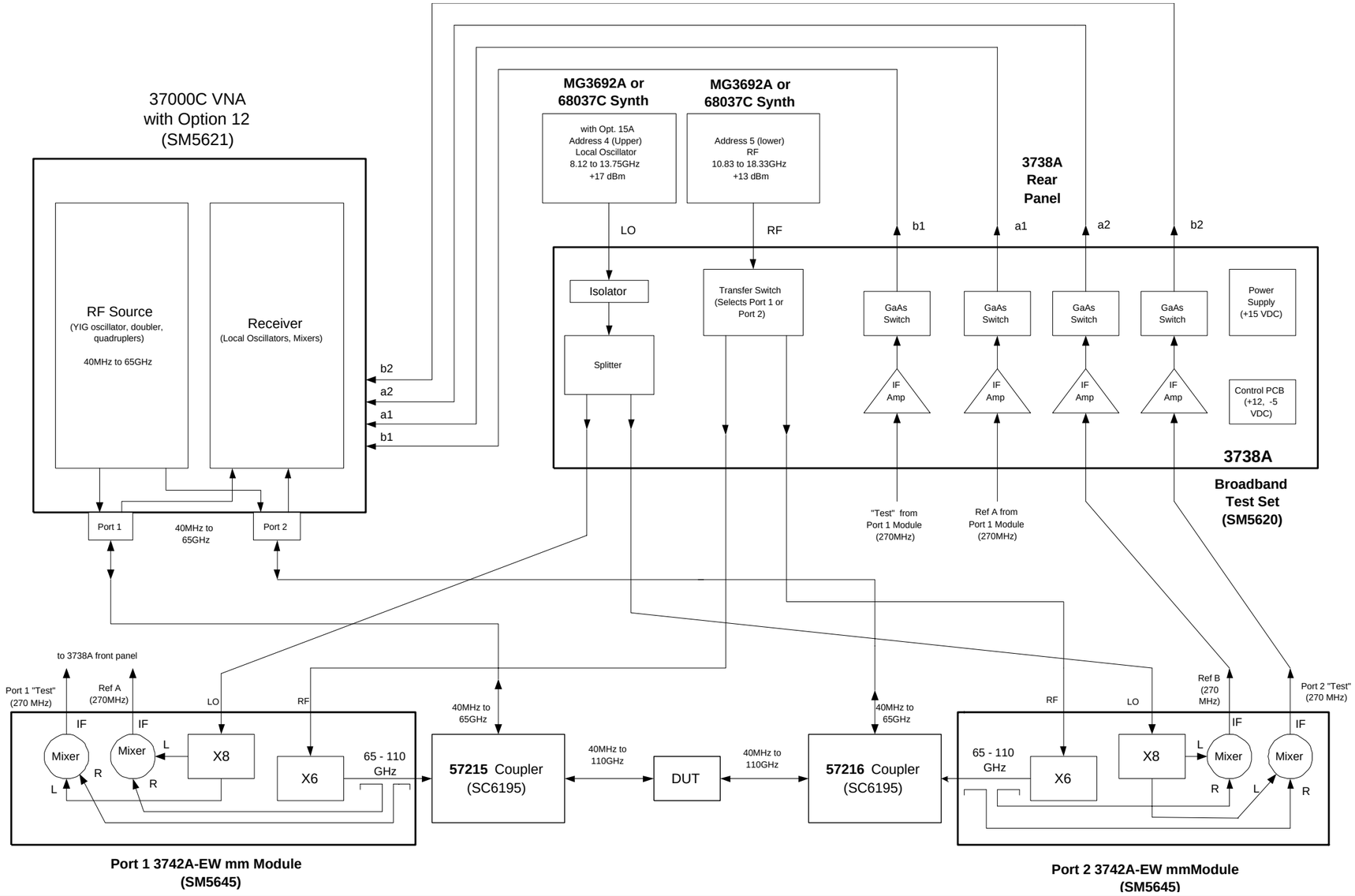


Figure D-3. *ME7808A Block Diagram*

D-5 REPLACEABLE ITEMS

Part numbers and descriptions of ME7808A replaceable system cables and parts and shown in Tables D-2 and D-3. Replacement parts and subassemblies for the 37000C VNA are shown in Chapter 2 of this manual. Replacement parts and subassemblies for the MG3690 or 68000 Synthesizers are shown in the applicable synthesizer maintenance manual.

> ***NOTE***
> There are no serviceable components or subassemblies in the 3742A modules or in the 57215/57216 couplers. These items must be returned to Anritsu Customer Service for repair or replacement.

Table D-2. *System Cables*

Description	Part Number
RF Cable, Ruggedized, Synthesizer to 3738A LO IN	ND46621 (68000 series synthesizers only)
RF Cable, Ruggedized, Synthesizer to 3738A RF IN	ND46620 (68000 series synthesizers only)
RF Cable, Coupler to 37000	806-101
Cable Set, rear panel, 37000	ND58267
Cable Set, 3742A to 3738A	ND58268
Cable, GPIB	2100-2
RF Cable, Ruggedized, Synthesizer to 3738A LO IN	C34429-7 (MG series synthesizers only)
RF Cable, Ruggedized, Synthesizer to 3738A RF IN	C34429-8 (MG series synthesizers only)
Multiplexing Coupler, Left (Port 1)	57215
Multiplexing Coupler, Right (Port 2)	57216

Table D-3. *Model 3738A Replaceable Parts*

Description	Part Number
Power Supply (+15VDC)	40-130
Fan Assembly	ND58282
IF Amplifiers	60-136
IF Switches	1020-44
Isolator	1000-49
RF Splitter	1091-87
PCB Assembly	54074-3
Transfer Switch	ND57971

D-6 PERFORMANCE VERIFICATION/SYSTEM OPERATIONAL TESTS

This chapter describes a series of manually performed tests that will ensure that the system meets many factory specifications. Many of these tests are also duplicated in the 2300-178 software package (version 4.10 and above).

Two automated methods are also available for S-parameter measurement accuracy testing (Performance Verification). The test port type being utilized will determine which method is appropriate.

> ***NOTE***
> Anritsu does not support tests or verification processes for wafer probe equipment. Contact the vendor of the wafer probe equipment if such support is desired.

For systems utilizing the W1 coaxial test ports (57215/57216 or SC6195 couplers), performance verification of the system is accomplished by use of the Anritsu Model 3656 calibration/verification kit and the 2300-496 software (packaged with the kit). This series of automated tests will verify that the system S-parameter measurement accuracy meets factory specifications. Instructions are packaged within the software as an Adobe Acrobat file.

For systems using only WR10 waveguide test ports, NIST traceable verification of S-parameter measurement accuracy may be performed for the system (including a WR10 calibration kit). Contact Anritsu Customer Service in Morgan Hill, California for information about this service.

The balance of this section is dedicated to operational performance tests of the complete ME7808A system.

Required Equipment for ME7808A System Performance Tests

- PC with Windows 95 or equivalent operating system
- National Instruments GPIB hardware and software installed in the PC
- Anritsu 2300-178 (3700TEST) Software
- Anritsu 3654B Calibration Kit
- Anritsu 3670V50-2 RF Cable (Throughline)
- Anritsu 3655W (WR10) Calibration Kit or
  Maury Z7005G19 (WR10) Calibration Kit

Optional Equipment

- HP Model 432A Power Meter with power sensor(s) covering 65 to 110 GHz
- Anritsu model SC6291 Male-Male adapter (for verifying the Couplers)
- Voltmeter (for troubleshooting only)
- Anritsu ML24xx Power Meter with 20 GHz Power Sensor (for troubleshooting only)

Preliminary

Step 1. Move millimeter modules and cables to another location so that the PC keyboard and the 37000C front panel are easily accessible.

Step 2. Press the Option Menu key.

Step 3. Select **TEST SET CONFIG / INTERNAL**, then press <Enter> to accept.

Step 4. On the rear panel of the 37000C, remove the cable set which connects to the 3738A, and install the small terminations (hanging from the chains) to the SMA connectors on the back of the 37000C.

Step 5. Load and run the 2300-178 test software, then the 2300-496 Veriication software. More complete instructions, such as required GPIB settings, are found in the Users' Guide contained within the 2300-496 software.

Synthesizer Verification

Refer to the appropriate Maintenance Manual for the synthesizers installed in the system for detailed Verification instructions. No further checks are necessary in the ME7808A system.

Millimeter Wave Module Verification

Most specifications for the system when operating from 65 to 110 GHz are not published (guaranteed) but are typical values. Systems which pass the following tests are operating in the expected manner and are capable of making accurate measurements.

Assemble the complete system with the 3742A modules installed, with all front and rear panel cables reconnected. Then perform the following steps.

Step 1. Configure system as a 65-110 GHz system. To do this, press the Utility Menu and select **TEST SET CONFIG / MILLIMETER WAVE** and press the <Enter> key. Select the WR-10 Extended band.

Step 2. Set the power vernier knobs on the 3742A modules fully CW to set maximum power at the test ports.

Step 3. Remove the 57215 and 57216 Couplers from the mmWave modules. Insure the 2 inch gold waveguide sections are installed to the test ports of the mmWave modules.

Step 4. Connect the two modules together.

Step 5. View S21 and S12.

Step 6. Ensure the system sweeps normally in this mode.

Step 7. Ensure both power control knobs on the mmWave modules are functional. It is normal for Lock Failures to appear at lower power. Return power control knobs to maximum power settings.

Step 8. Clear the errors from the Service Log.

IF Power Level Test

This test verifies that each individual receiver channel operates properly. Measurement calibration of the system is not required for this test. Ensure the system has warmed up for at least 1 hour before performing this test.

Step 1. Install a flush short on the test port of the Port 1 mmWave module.

Step 2. Set up the network analyzer as shown below:

Key	Menu Choice
SETUP MENU	Start: 65 GHz
	Stop: 110 GHz
CHANNEL MENU	Dual Channels 1 & 3
GRAPH TYPE	Log Magnitude (both channels)
S PARAMS	Channel 1
	User Ratio: a1/1
	User Phase Lock: a1
	Channel 3
	User Ratio: b1/1
	User Phase Lock: a1
SET SCALE	Resolution: 10 dB/Div (both channels)
	Reference Value: -10 dB
LIMITS	Channel 1 (a1/1)
	Upper Limit: ON (-1 dB)
	Lower Limit: ON (-28 dB)
	Channel 3 (b1/1)
	Upper Limit: ON (-1 dB)
	Lower Limit: ON (-38 dB)

Step 3. Ensure that the displays for Channels 1 and 3 fall between the limit lines, and that no error messages appear on the display.

Step 4. Install a flush short to the Port 2 mmWave module.

Step 5. Set up the network analyzer as shown below:

Key	Menu Choice
SETUP MENU	Start: 65 GHz
	Stop: 110 GHz
CHANNEL MENU	Dual Channels 2 & 4
GRAPH TYPE	Log Magnitude (both channels)
S PARAMS	Channel 2
	User Ratio: a2/1
	User Phase Lock: a2
	Channel 4
	User Ratio: b2/1
	User Phase Lock: a2
SET SCALE	Resolution: 10 dB/Div (both channels)
	Reference Value: -10 dB
LIMITS	Channel 2 (a2/1)
	Upper Limit: ON (-1 dB)
	Lower Limit: ON (-28 dB)
	Channel 4 (b2/1)
	Upper Limit: ON (-1 dB)
	Lower Limit: ON (-38 dB)

Step 6. Ensure that the displays for Channels 2 and 4 fall between the limit lines, and that no error messages appear on the display.

Test Port Power Test

Step 1. Default the system (Press Default Program key two times). Display Single Channel, S11.

Step 2. Connect the HP432A Power Meter and sensor to the Port 1 mmWave module test port.

Step 3. For each frequency on the power sensor, read the power at the Port 1. The power should be 0 to -10 dBm for each frequency.

Step 4. Display Single Channel, S22. Connect the power sensor to Port 2. Repeat steps 2 and 3 for the Port 2 module.

Performance Verification- High Level Noise (Reflection) Test

The following test verifies that the high level noise in the system will not significantly affect the accuracy of subsequent measurements. High level noise is the random noise that exists in the system, and cannot be accurately predicted or measured, thus it cannot be removed by conventional error-correction techniques. Measurement calibration is not required for these tests. Ensure the system has warmed up for at least 1 hour before performing this test.

Step 1. Connect flush shorts to both test ports of the mmWave modules.

Step 2. Default the system (press DEFAULT PROGRAM two times).

Step 3. Set the system as shown below:

Key	Menu Choice
SETUP MENU	Start: 65 GHz
	Stop: 110 GHz
CHANNEL MENU	Dual Channels 1 & 3
GRAPH TYPE	Log Magnitude (both channels)
S PARAMS	Channel 1: S11
	Channel 3: S22
SET SCALE	Resolution: 0.05 dB/division (both channels)
LIMITS	Channel 1
	Upper Limit: ON (0.04 dB)
	Lower Limit: ON (-0.04 dB)
	Channel 3
	Upper Limit: ON (0.04 dB)
	Lower Limit: ON (-0.04 dB)

Step 4. Be careful not to bump any system components (especially cables) during this test. Select Channel 1. After several sweeps, press TRACE MEMORY, and select Store Data to Memory. Select View Data/Memory.

Step 5. Be sure the RF display remains between the limit lines for approximately 5 sweeps. (It is normal for the data to drift out of the limit lines after a short period of time).

Step 6. Repeat steps 4 and 5 for Channel 3.

Performance Verification- High Level Noise (Transmission) Test

The following test verifies that the high level noise in the system will not significantly affect the accuracy of subsequent measurements. High level noise is the random noise that exists in the system. It cannot be accurately predicted or measured, thus it cannot be removed by conventional error-correction techniques. Measurement calibration is not required for these tests. Ensure the system has warmed up for at least 1 hour before performing this test.

Step 1. Remove the flush shorts and connect the mmWave modules together.

Step 2. Set the system as shown below:

Key	Menu Choice
SETUP MENU	Start: 65 GHz
	Stop: 110 GHz
CHANNEL MENU	Dual Channels 1 & 3
GRAPH TYPE	Log Magnitude (both channels)
S PARAMS	Channel 1: S12
	Channel 3: S21
SET SCALE	Resolution: 0.05 dB/division (both channels)
LIMITS	Channel 1
	Upper Limit: ON (0.04 dB)
	Lower Limit: ON (-0.04 dB)
	Channel 3
	Upper Limit: ON (0.04 dB)
	Lower Limit: ON (-0.04 dB)

Step 3. Be careful not to bump any system components (especially cables) during this test. Select Channel 1.

Step 4. After several sweeps, press TRACE MEMORY, and select Store Data to Memory. Select View Data/Memory.

Step 5. Be sure the RF display remains between the limit lines for approximately 5 sweeps. (It is normal for the data to drift out of the limit lines after a short period of time).

Step 6. Repeat steps 3 and 4 for Channel 3.

Drift Test

Step 1. Leave the equipment connected as described in the previous test (High Level Noise Transmission). Ensure the system has warmed up for 2 hours.

Step 2. Change Graph Type to Log Mag and Phase for both channels.

Step 3. Store Data to Memory and View Data/Memory for both channels.

> ***CAUTION***
>
> Do not move any part of the system after this point. Be especially careful to not bump the cables.

Step 4. At the end of 1/2 hours, Autoscale both channels.

Step 5. Set Limit Lines to +/- 0.2 dB, and +/- 2 Degrees for both channels. Ensure displays fall within the limit lines.

Performance Verification- 12 Term OSL Calibration

This calibration is required to perform the System Dynamic Range, Source Match, and Directivity tests. Ensure the system has warmed up for at least 1 hour before performing this test, and that the precision 2 inch waveguide sections are installed to the test ports of the mmWave modules.

Step 1. Insert the Calibration Coefficient disk from the WR-10 calibration kit into the floppy drive of the 37397C and load the coefficients via the UTILITY MENU key.

Step 2. Press BEGIN CAL.

Step 3. Make the following selections from the menus to perform a full band 12 Term Calibration:

- ❑ Change Cal Method and Line Type
- ❑ Waveguide
- ❑ Full 12 Term
- ❑ Include Isolation (required for System Dynamic Range test)
- ❑ Sliding Load (required for Directivity and Source Match tests)
- ❑ Use Installed Kit

Step 4. Before measuring the Isolation Devices (terminations), make the following changes to the setup:

- ❑ AVERAGE/SMOOTH MENU key: Change to 512 averages
- ❑ IFBW key: Change to Minimum (10 Hz)
- ❑ Measure the Isolation Devices.

Step 5. Finish the calibration using the instructions on the VNA display.

Performance Verification- Source Match and Directivity Tests

Ensure the 12 Term Calibration was performed as described above (sliding loads were used) and the calibration is active (APPLY CAL LED is ON). During this test, do not disconnect the gold waveguide sections which were used during the 12 Term Calibration.

Source Match Test

Step 1. Set up system as shown below:

Key	Menu Choice
SETUP MENU	Start: 65 GHz Stop: 110 GHz
CHANNEL MENU	Single Channel Channel 1
GRAPH TYPE	Log Magnitude
SET SCALE	Resolution: 0.1 dB/DIV Ref Value: 0.0 dB Reference Line: TOP
S-PARAMS	S11

Step 2. Attach a second high-precision waveguide section to the module on Port 1.

Step 3. Attach a flush short to the end of the high-precision waveguide section.

Step 4. While observing the sweep indicator, allow at least one complete sweep to occur. Press Autoscale to center the trace.

Step 5. Press Marker Menu, and select MARKER 1, MARKER 2, and MARKER 3, to be ON.

Step 6. Using the rotary knob, position marker 1 and marker 2 to adjacent peaks of the ripple with the greatest negative trough (or adjacent troughs if the ripple has the greatest positive peak); position marker 3 to the bottom of the trough (or the top of the peak if the ripple has the greatest positive peak). Refer to Figure D-3 (following page).

Step 7. Using the Marker Menu and Readout Marker key menus, record the absolute value of markers 1 and 2 as follows:

- Subtract one from the other.
- Halve the difference
- Add the resultant to the value of the marker at the lowest peak (or the deepest trough).

This is the average value of the two peaks (or troughs).

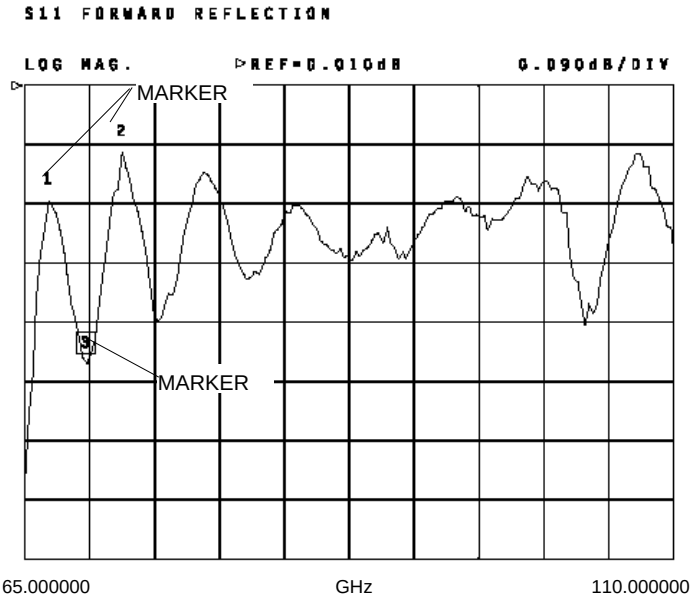


Figure D-3. *Markers*

Step 8. Record the marker 3 value.

Step 9. Find the absolute difference of the values recorded in step 7 and step 8. This is the Peak-to-Peak Ripple value. Use the RF Measurement Chart (Table D-3) to find the corresponding Return Loss value. This value is the Effective Source Match. Insure Source Match measures at least 30 dB.

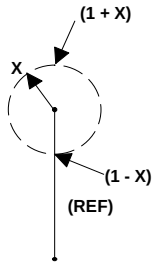
Step 10. Change the S Parameter to S22. Move the outside waveguide section with the short attached to the Port 2 module.

Step 11. Repeat Steps 4 through 9 to compute Port 2 Source Match. Verify Port 2 Source Match is 30 dB minimum.

Table D-3. *Microwave Measurement Chart*

IMPORTANT NOTE

Conversion tables for Return Loss, Reflection Coefficient, and SWR with tabular values for interaction of a small phasor x with a large phasor (unity reference) expressed in dB related to reference.



TERM002.DRW

SWR	Reflection Coefficient	Return Loss (dB)	Relative to Unity Reference			
			X dB Below Reference	REF + X dB	REF – X dB	REF / X Peak to Peak Ripple dB
17.3910	0.8913	1	1	5.5350	–19.2715	24.8065
8.7242	0.7943	2	2	5.0780	–13.7365	18.8145
5.8480	0.7079	3	3	4.6495	–10.6907	15.3402
4.4194	0.6310	4	4	4.2489	–8.6585	12.9073
3.5698	0.5623	5	5	3.8755	–7.1773	11.0528
3.0095	0.5012	6	6	3.5287	–6.0412	9.5699
2.6146	0.4467	7	7	3.2075	–5.1405	8.3480
2.3229	0.3981	8	8	2.9108	–4.4096	7.3204
2.0999	0.3548	9	9	2.6376	–3.8063	6.4439
1.9250	0.3162	10	10	2.3866	–3.3018	5.6884
1.7849	0.2818	11	11	2.1567	–2.8756	5.0322
1.6709	0.2512	12	12	1.9465	–2.5126	4.4590
1.5769	0.2239	13	13	1.7547	–2.2013	3.9561
1.4985	0.1995	14	14	1.5802	–1.9331	3.5133
1.4326	0.1778	15	15	1.4216	–1.7007	3.1224
1.3767	0.1585	16	16	1.2778	–1.4988	2.7766
1.3290	0.1413	17	17	1.1476	–1.3227	2.4703
1.2880	0.1259	18	18	1.0299	–1.1687	2.1986
1.2528	0.1122	19	19	0.9237	–1.0337	1.9574
1.2222	0.1000	20	20	0.8279	–0.9151	1.7430
1.1957	0.0891	21	21	0.7416	–0.8108	1.5524
1.1726	0.0794	22	22	0.6639	–0.7189	1.3828
1.1524	0.0708	23	23	0.5941	–0.6378	1.2319
1.1347	0.0631	24	24	0.5314	–0.5661	1.0975
1.1192	0.0562	25	25	0.4752	–0.5027	0.9779
1.1055	0.0501	26	26	0.4248	–0.4466	0.8714
1.0935	0.0447	27	27	0.3796	–0.3969	0.7765
1.0829	0.0398	28	28	0.3391	–0.3529	0.6919
1.0736	0.0355	29	29	0.3028	–0.3138	0.6166
1.0653	0.0316	30	30	0.2704	–0.2791	0.5495
1.0580	0.0282	31	31	0.2414	–0.2483	0.4897
1.0515	0.0251	32	32	0.2155	–0.2210	0.4365
1.0458	0.0224	33	33	0.1923	–0.1967	0.3890
1.0407	0.0200	34	34	0.1716	–0.1751	0.3467
1.0362	0.0178	35	35	0.1531	–0.1558	0.3090
1.0322	0.0158	36	36	0.1366	–0.1388	0.2753
1.0287	0.0141	37	37	0.1218	–0.1236	0.2454
1.0255	0.0126	38	38	0.1087	–0.1100	0.2187
1.0227	0.0112	39	39	0.0969	–0.0980	0.1949
1.0202	0.0100	40	40	0.0864	–0.0873	0.1737
1.0180	0.0089	41	41	0.0771	–0.0778	0.1548
1.0160	0.0079	42	42	0.0687	–0.0693	0.1380
1.0143	0.0071	43	43	0.0613	–0.0617	0.1230
1.0127	0.0063	44	44	0.0546	–0.0550	0.1096
1.0113	0.0056	45	45	0.0487	–0.0490	0.0977
1.0101	0.0050	46	46	0.0434	–0.0436	0.0871
1.0090	0.0045	47	47	0.0387	–0.0389	0.0776
1.0080	0.0040	48	48	0.0345	–0.0346	0.0692
1.0071	0.0035	49	49	0.0308	–0.0309	0.0616
1.0063	0.0032	50	50	0.0274	–0.0275	0.0549
1.0057	0.0028	51	51	0.0244	–0.0245	0.0490
1.0050	0.0025	52	52	0.0218	–0.0218	0.0436
1.0045	0.0022	53	53	0.0194	–0.0195	0.0389
1.0040	0.0020	54	54	0.0173	–0.0173	0.0347
1.0036	0.0018	55	55	0.0154	–0.0155	0.0309
1.0032	0.0016	56	56	0.0138	–0.0138	0.0275
1.0028	0.0014	57	57	0.0123	–0.0123	0.0245
1.0025	0.0013	58	58	0.0109	–0.0109	0.0219
1.0022	0.0011	59	59	0.0097	–0.0098	0.0195
1.0020	0.0010	60	60	0.0087	–0.0087	0.0174

Effective Directivity Test

Step 1. Remove the flush short from the end of the high-precision waveguide section. Point the test ports away from all reflective objects.

Step 2. Press Autoscale key to center the trace.

Step 3. Repeat step 6 through 8.

Step 4. Find the absolute difference of the values recorded in step 7 and step 8. This is the Peak-to-Peak Ripple value. Use the RF Measurement Chart to find the corresponding Return Loss value.

Step 5. Find the corresponding REF + X or REF - X value from the RF Measurement Chart. Use the following formula to calculate the effective directivity value:

For ripple with negative trough:

Effective Directivity =
Return Loss value + (Absolute Value of Marker 3)-(REF - X)

For ripple with positive peak:

Effective Directivity =
Return Loss value +(Absolute Value of Marker 3)+(REF + X)

Step 6. Verify the Effective Directivity is >35 dB from 65 to 75 GHz, and >40 dB from 75 to 110 GHz.

Step 7. Change the S Parameter back to S11, and move the outside waveguide section back to the Port 1 module.

Step 8. After 2 sweeps, press AUTOSCALE.

Step 9. Repeat steps 4, 5 and 6 to calculate Port 1 Directivity. Verify the Effective Directivity is >35 dB from 65 to 75 GHz, and >40 dB from 75 to 110 GHz.

Performance Verification-System Dynamic Range

System Dynamic Range is defined as the ratio of the typical power at Port 1 and the System Noise Floor. A 12 Term Calibration (performed exactly as described in this Appendix) must be activated. *Video IF Bandwidth and Averaging must be set as shown in the chart below.*

Step 1. Attach a broadband termination to both test ports of the 3742A mmWave modules.

Step 2. Set up the VNA display as shown below:

Key	Menu Choice
SETUP MENU	Start: 65 GHz Stop: 110 GHz CW Mode: ON
CHANNEL MENU	Dual Channels 1 & 3
GRAPH TYPE	Log Magnitude (both Channels)
SET SCALE	Resolution: 10 dB/division Reference Value: -50 dB Reference Line: 7
S-PARAMS	Channel 1: S12 Channel 3: S21
DATA POINTS	401
VIDEO IFBW	10 Hz (Minimum)
AVG/SMOOTH MENU	512 Averages (ON)
LIMITS:	Lower Limit ON (see chart below, both channels)
DATA POINTS	50 Points in CW

Step 3. Allow the system to sweep both forward and reverse. Ensure the data does not go above the limit line on either channel. Check each frequency in the chart below.

CW Freq (GHz)	Specification (dB)
65	67
75	80
85	80
100	77
110	70

Coupler Verification

Simple operational tests may be performed on-site as stated in Section D-7.

D-7 MULTIPLEXING COUPLER CHECK

This test verifies that the multiplexing Couplers are operational.

Equipment Required:

- Anritsu SC6291 W1(m) to W1(m) Adapter
- Anritsu 3654B Calibration Kit
- Anritsu 3670V50-2 Test Port Cables (Two each)
- Anritsu 3655W Cal Kit or Maury Microwave Model Z7005G19 WR-10 Waveguide Calibration Kit

Coupler Low Frequency Test (Coaxial – V connector)

Step 1. Remove the multiplexing Couplers from the mmWave modules and then use the SC6291 Adapter to connector the W1(f) connector of the Couplers together.

Step 2. Remove the mmWave modules from the test area and set the 37397C Test Set Configuration (Option Menu key) to Internal

Step 3. Set up the VNA as shown in the table below:

Key	Menu Choice
SETUP MENU	Start: 40 GHz Stop: 65 GHz
CHANNEL MENU	Single Channel: Channel 3
GRAPH TYPE	Log Magnitude
SET SCALE	Resolution: 10 dB/division Reference Value: 0 dB Reference Line: 8
S-PARAMS	S21

Step 4. Attach the throughlines to the VNA (Port 1 and Port 2). Use the 3654B Calibration Kit to perform a 12 Term calibration at the ends of the throughlines.

Step 5. Leave the waveguide ports of the couplers open, attach the couplers between the throughlines, then measure the S21 insertion loss of the couplers.

Step 6. Verify that the insertion loss is less than 15 dB and there are no sharp discontinuities.

Coupler High Frequency Test (Waveguide – WR10)

Step 1. Reconnect the 3742A-EW mmWave modules to the system and set the Test Set Configuration to the 3742A-EW Millimeter (or Broadband) mode.

Step 2. Set the VNA as shown below.

Key	Menu Choice
SETUP MENU	Start: 65 GHz Stop: 110 GHz
CHANNEL MENU	Single Channel: Channel 3
GRAPH TYPE	Log Magnitude
SET SCALE	Resolution: 10 dB/division Reference Value: 0 dB Reference Line: 8
S-PARAMS	S21

Step 3. Use the WR-10 Waveguide Calibration Kit to perform a 12 Term Broadband load calibration.

Step 4. Connect coupler pair between the two mmWave modules. The V(f) connectors of the couplers need to be terminated with the 28V50B terminations from the 3654B Calibration Kit.

Step 5. Verify that the insertion loss is less than 20 dB and there are no sharp discontinuities.

D-8 TROUBLESHOOTING

Troubleshooting this system is accomplished by first ensuring no set-up error exists, then determining which instrument has failed.

Front Panel and Cabling Checks

Step 1. Ensure the following:

- ❑ The power control knobs on the top of the 3742A modules are set fully CW.
- ❑ The small RF cables on the front and rear panels of the 37000C are not damaged.
- ❑ No error messages are shown on the front panels of the synthesizers.
- ❑ The top synthesizer is GPIB address 4, and it has Option 15A installed.
- ❑ The lower synthesizer is GPIB address 5.
- ❑ All cables are on securely and are connected to the right positions.

Step 2. Press the Utility Menu key then select **DISPLAY INSTRUMENT PARAMETERS / SYSTEM** and ensure that both synthesizers are shown.

General Troubleshooting of the System

Step 1. After determining that the problem is not caused by cabling, synthesizer, or GPIB setup errors, isolate the problem instrument using the a process of elimination. The critical information to know is direction (only forward, only reverse, or both) and frequency (all frequencies, or only below 38 GHz, only from 38 to 65 GHz, or only above 65 GHz).

Step 2. To determine direction, be sure to display only one channel at a time.

Step 3. If the problem occurs at any frequency below 65 GHz, you can assume the fault lies in the 37XXXC. Refer to Chapter 7 for troubleshooting help on this instrument.

Step 4. If the problem occurs in only one direction (forward or reverse), you can eliminate both synthesizers as cause.

Step 5. If the problem is only in one direction, and only above 65 GHz, the problem is in the 3742A or the 3738A test set or 372XXC or 373XXC.

Step 6. If you swap the 3742A's, and the problem moves, one 3742A is defective. If you swap the 3742A's and the problem does not move, the failure is in the 3738A or the 372xxC or 373xxC.

3738A Checks

Step 1. If it is possible that the 3738A is defective, ensure the system is in the Millimeter Mode (not Broadband or Internal), remove the cover of the 3738A and make the checks described below to verify proper operation.

Step 2. Note that many DC voltages will change as the system changes between forward and reverse measurement, so be sure to set the system as indicated.

DC Power Supplies and General PCB Tests:

On the following test points of the 54074-3 PC board, verify the following DC voltages from TP8 ground (+/- approximately 10%). All supplies except the TP5 voltage are derived from regulators found on the PCB.

- TP5: +15 VDC (provides power for all other DC supplies*)
- TP3: +12 VDC (IF Amp bias)
- TP4: +5VDC (for PCB internal circuits)
- TP6: +5 VDC (not used)
- TP7: +12VDC (fan power)
- TP11: –5VDC (not used)

* If TP5 has an incorrect voltage, replace the power supply with the part number shown on Table D-2.

PCB Control Signals

Step 1. With the system still in the Millimeter mode, set the instrument to display Single Channel, S21. Make the following checks, and note the probable failed part. Be sure to use the sequence shown below when diagnosing and determining which part to replace.

Location	Required Signal	Replace if Required Signal Fails
TP 14	TTL low	37000 A8 PCB
TP 9	–5V	37000 A8 PCB or 3738A control PCB
TP 10	0V	37000 A8 PCB or 3738A control PCB
Port 1 LED	ON	*Port 1 LED
TP 1	+12 VDC	Entire PCB
TP 2	0 VDC	Entire PCB
J9 pin 1 on PCB	~ -3.8 VDC	Entire PCB or transfer switch
J9 pin 2 on PCB	~ +2.2 VDC	Entire PCB or transfer switch

*Note that if the LED fails, the PCB will not operate, and forward only will fail.

Step 2. Set the instrument to display Single Channel, S12. Make the following checks on the 54074-3 PCB, and note the probable failed part. Be sure to use the sequence shown below when diagnosing and determining which part to replace.

Location	Required Signal	Replace if Required Signal Fails
TP 14	TTL low	37000 A8 PCB
TP 9	-5V	37000 A8 PCB or 3738A control PCB
TP 10	0V	37000 A8 PCB or 3738A control PCB
Port 2 LED	ON	*Port 2 LED
TP1	0 VDC	Entire PCB
TP2	+12 VDC	Entire PCB
J9 pin 1 on PCB	~ +2.2 VDC	Entire PCB or transfer switch
J9 pin 2 on PCB	~ –3.8 VDC	Entire PCB or transfer switch

*Note that if the LED fails, the PCB will not operate, and reverse only will fail.

3738A LO Path

As shown on Figure D-3, there are no switching or active components in this signal path once the signal has left the synthesizer. Inside the 3738A, the signal from the synthesizer is routed through an isolator, through a splitter, and then out the Port 1 and Port 2 LO connectors for use by the modules.

The total insertion loss through the 3738A is about 5 dB, therefore the power out of the front panel Port 1 and Port 2 LO connectors should measure approximately +11 dBm, regardless of sweep direction. Use the ML24xx Power Meter to verify this power.

3738A RF Path Description and Checks:

As shown on Figure D-3, a transfer switch controls the presence of RF signal at the 3738A RF OUT ports. If the VNA is making a forward measurement, approximately +11 dBm is present at the Port 1 RF OUT. If the measurement is reverse, the same power is present only at the Port 2 RF OUT. Use the ML24xx Power Meter to verify this power.

3738A IF Path Description and Checks:

As shown on Figure D-3, there are four separate IF paths in the 3728A. Each path is composed of an ampifier (gain is approximately 20 dB) and a GaAs switch. The signal through these paths is fixed at 270 MHz, which is the down-converted signal from the 3742A modules.

Regardless of sweep direction, the GaAs switches and the IF amplifiers are biased ON (pass RF) when the system frequency is above 65 GHz, and are OFF when the system frequency is below 65 GHz. Correct bias voltages at TP3, TP9, and TP10 are shown on the chart above.

Subject Index

N

O

P

R

T

V

W

Y