Product Brochure

Anritsu

MP1800A Series

Signal Quality Analyzer

Compact and High-performance BERT
64.2 Gbit/s Signal Quality Analyzer

MP1800A Signal Quality Analyzer is a modular BERT with plug-in modules;

- Pulse Pattern Generator (PPG) supporting high quality output and high amplitude signals
- Error Detector (ED) with high input sensitivity supporting signal analysis, such as Bathtub and Eye Diagram measurements
- Jitter Modulation Source (JMS) for generating various types of jitter, such as SJ/RJ/BUJ/SSC, and supporting Jitter Tolerance tests

MP1800A supports physical layers testing for optical modules and high speed devices up to 64.2 Gbit/s. Combined use with the MP1861A 56G/64G bit/s MUX and MP1862A 56G/64G bit/s DEMUX supports BER tests up to 64.2 Gbit/s. Additionally, combining the 4Tap Emphasis MP1825B supporting up to 32.1 Gbit/s with the PAM4 Converter MZ1834A/B, PAM8 Converter MZ1838A, 32Gbaud Power PAM4 Converter G0375A, and 32Gbaud PAM4 Decoder with CTLE G0376A supports PAM signal generation and BER measurement, while tracking using the 64Gbaud PAM4 DAC G0374A adds strong support for signal integrity tests, including PAM signal generation.

Wide Bandwidth 0.1 Gbit/s to 64.2 Gbit/s

High-quality, Low-jitter Waveforms

64.2 Gbit/s Jitter Tolerance Test (SJ, RJ, BUJ, SSC)

High Input Sensitivity & Wide Phase Margin

Signal Quality Analysis

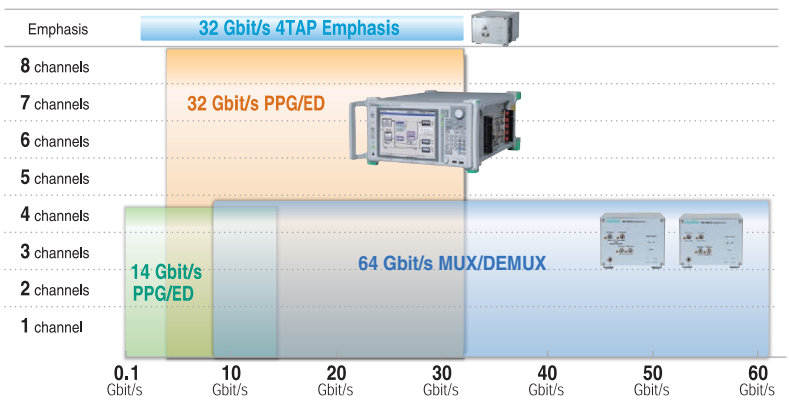
Burst Measurement

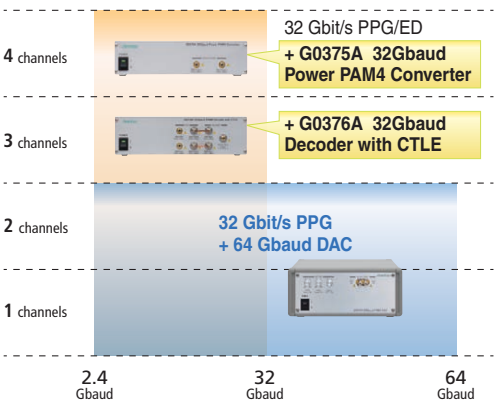
Clock Recovery

Multi-channel Configuration (Up to 8ch)

Wide Bandwidth 0.1 Gbit/s to 32.1 Gbit/s, 8 Gbit/s to 64.2 Gbit/s

Bit rates from 0.1 Gbit/s to 32.1 Gbit/s are supported, depending on the selected module. Furthermore, PAM signals can be generated by combining the MZ1834A/B, MZ1838A, and G0375A, while adding the G0376A supports PAM signal BER measurements. Combination with the 56G/64G MUX/DEMUX supports bit rates up to 64.2 Gbit/s. Additionally, PAM4 signals up to 64.2 Gbaud can be generated when used in combination with the G0374A 64Gbaud PAM4 DAC.





■ 32 Gbit/s PPG/ED Module
- 2.4 Gbit/s to 32.1 Gbit/s: MU183020A/21A, MU183040B/41B (Option-001)
- 2.4 Gbit/s to 28.1 Gbit/s: MU183020A/21A, MU183040B/41B

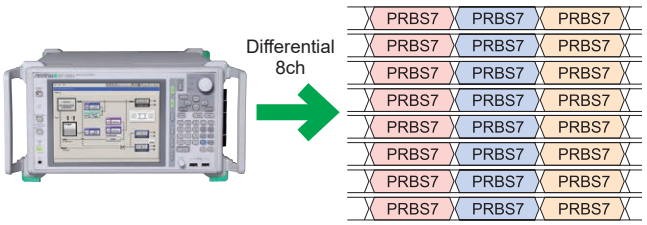
■ 14 Gbit/s PPG/ED Module
- 0.1 Gbit/s to 14.1 Gbit/s: MU181020B, MU181040B (Option-002/005)
- 0.1 Gbit/s to 14 Gbit/s: MU181020B, MU181040B (Option-002)

■ 56/64G MUX/DEMUX
- 8 Gbit/s to 56.2 Gbit/s: MP1861A, MP1862A
- 8 Gbit/s to 64.2 Gbit/s: MP1861A, MP1862A (Option-001)
- DC to 64 Gbaud: G0374A

Synchronous operation of up to four MP1800A units generates 32G × 32ch (32G PPG module) and 64G × 16ch (64G MUX) signals.

Synchronization up to 8ch

Due to the modular platform design, the PPG/ED modules can be configured with various other modules to configure custom systems. The number of channels per 28G/32G PPG/ED module can be selected from 1, 2, or 4 and PPG/ED modules can be installed to support up to 8ch. Moreover, since each channel pattern can be synchronized, D/A converters, MUX/DEMUX, crosstalk, and skew tolerance can be evaluated.



∗: For details about possible module combinations, see the Option Selection Guide for the MP1800A series.

High Sensitivity Error Detector (ED)

MU183040B/MU183041B 28 G/32 Gbit/s High Sensitivity ED extends the performance of the earlier A-type ED to offer world's best Rx sensitivity* with the world's fastest Auto Adjust* (auto-align of threshold level and phase points).
The MU183040B/41B supports simultaneous multichannel measurements of low-amplitude, low Eye Opening DUTs such as Highs Speed Backplane devices and Active Optical Cable (AOC) to achieve more-accurate, ideal signal quality analysis.

Eye Amplitude Sensitivity:
15 mVp-p (typ.) (28.1 Gbit/s, Single-end)
≤25 mVp-p (28.1 Gbit/s, Single-end)
Eye Height Sensitivity:
10 mVp-p (typ.) (28.1 Gbit/s, Single-end)

∗As of September, 2013

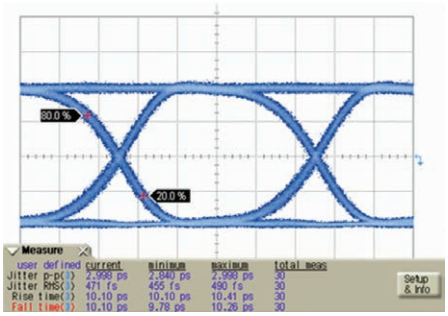
Passive Equalizer

In high speed serial transmission such as 28 Gbit/s, transmission losses of printed-circuits boards causes the Eye Opening to become narrower.
The J1621A and J1622A Passive Linear Equalizers can be connected to the ED to compensate for PCB trace losses and improve the Eye Opening. Combination with the MU183040B/MU183041B High Sensitivity ED supports Jitter Tolerance tests of PHY devices with a narrow Eye Opening.

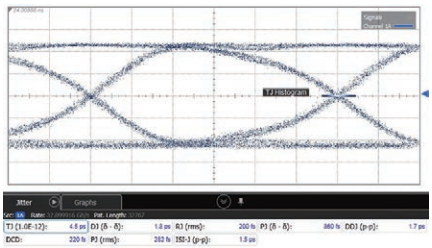
Low-jitter, High-quality Waveform

The PPG module supports low-jitter and high-quality waveforms. The output amplitude can be customized to application needs.

Low-jitter: RJ 300 fs rms (typ.)
Total RMS Jitter 700 fs rms (typ.)
High amplitude: 0.5 Vp-p to 3.5 Vp-p
[MU183020A-013/023, MU183021A-013]



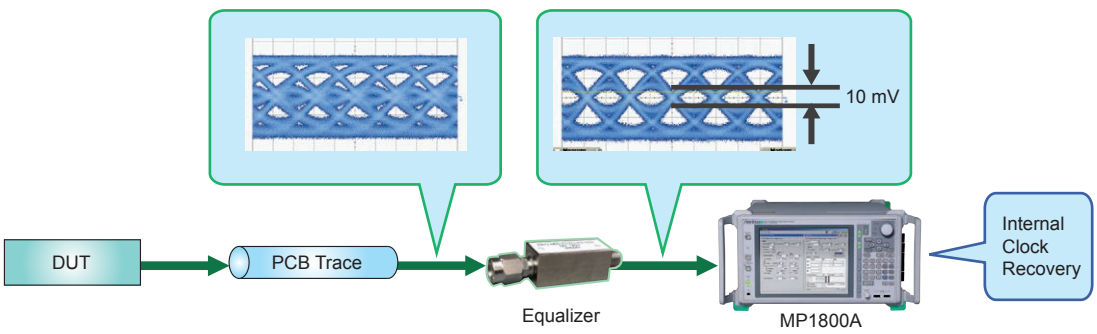
Output Waveform at 28 Gbit/s, 3.5 Vp-p (MU183020A-013) using Sampling oscilloscope with 70 GHz bandwidth



28 Gbit/s, PPG Intrinsic TJ (1E-12) = 4.5 psp-p, RJ rms = 200 fs Nominal measured data.
Using Sampling Oscilloscope with 50 GHz bandwidth and <100 fs rms intrinsic jitter.

Clock Recovery

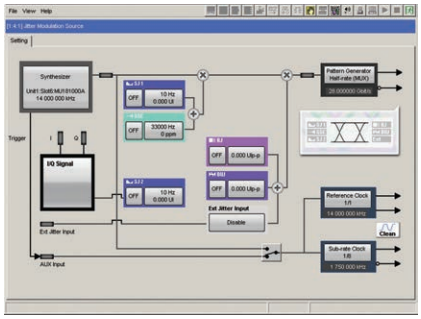
Internal Clock Recovery option can be installed in to MU183040B/41B. Physical layer (PHY) devices, such as SERDES, sometimes have different Tx and Rx Clock systems and Clock Recovery is required at the Error Detector for jitter tolerance tests. Additionally, since transmission using Multi-Mode Fiber (MMF) causes generation of jitter and wander components in the Rx module, Clock Recovery at the Error Detector is similarly required.
Installing this Clock Recovery option supports stress jitter tolerance tests of PHY devices with different Tx and Rx clocks, BER measurements of AOC devices, and simultaneous multichannel measurements, offering even more accurate and ideal signal integrity analyses.



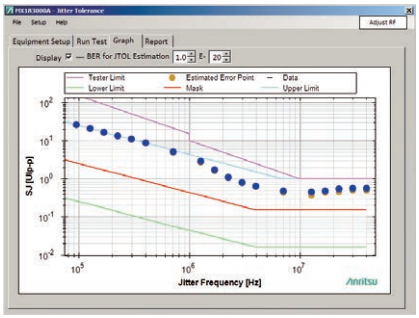
SJ, RJ, BUJ, SSC and Half Period Jitter (F/2 Jitter) Generation

The MU181500B Jitter Modulation Source generates wide-amplitude SJ up to 1 UI at a Jitter Frequency of 250 MHz and a maximum 2000 UI, ensuring sufficient margin for receiver Jitter Tolerance tests. Additionally, the Intrinsic Jitter of 275 fs rms (nom.)* is extremely low, not only when Jitter modulation is OFF but also when 0 UI is set at Jitter modulation ON, ensuring accurate measurements even at low Jitter amplitudes. The combination of low intrinsic jitter waveform with excellent jitter transparency supports high-accuracy Jitter Tolerance tests. Moreover, simultaneous injection of RJ, BUJ and SSC as well as dual SJ for two-tone supports various Jitter Tolerance tests. Additionally, the MX183000A High-Speed Serial Data Test Software supports multi-mask tables as well as easy mask editing to support next-generation standards.

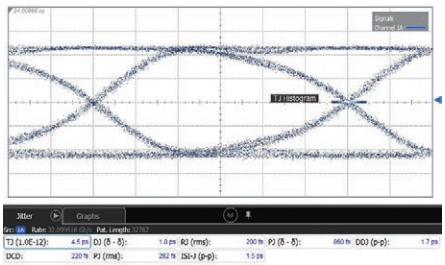
*: Phase noise measurement with using Spectrum Analyzer and 1010…repetition signal.



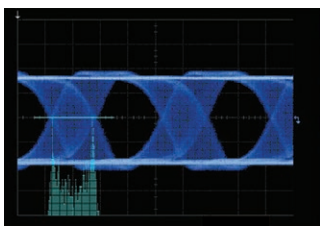
MU181500B Jitter Modulation Source Setting Screen



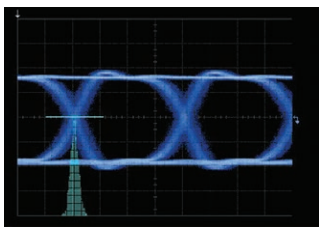
MX183000A High-Speed Serial Data Test Software Measurement Screen



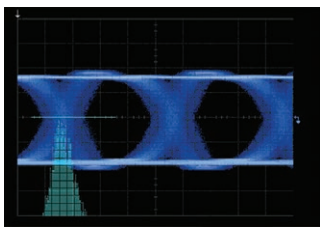
28 Gbit/s, PPG Intrinsic RJ rms Using Sampling oscilloscope with 50 GHz bandwidth and <100 fs rms intrinsic jitter



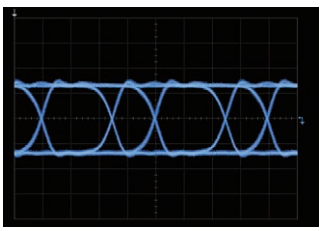
Sinusoidal Jitter (SJ)



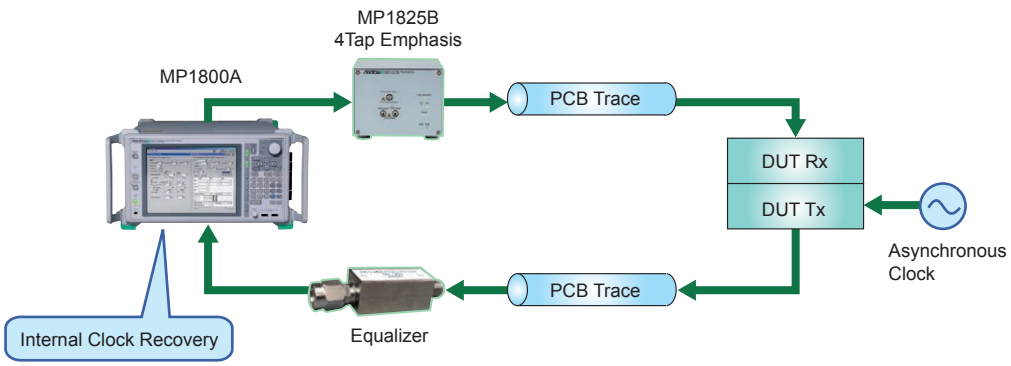
Random Jitter (RJ)



Bounded Uncorrelated Jitter (BUJ)

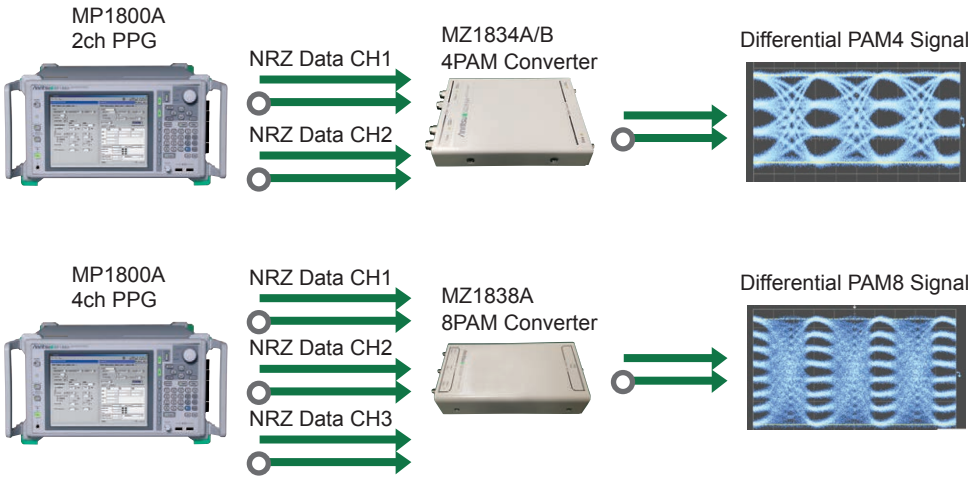


Half Period Jitter (F/2 Jitter)



PAM4/PAM8 Signal Generation

Combining the Anritsu MZ1834A/B 4PAM Converter, MZ1838A 8PAM Converter and G0375A 32Gbaud Power PAM4 Converter with the MP1800A Signal Quality Analyzer supports generation of both PAM4 and PAM8 signals for R&D High Speed Backplane and 400 GbE R&D. The MP1800A high-quality NRZ waveform and wideband passive PAM converter generate high-quality PAM signals with assured S/N.



In addition, combining the MP1800A and 32Gbaud Power PAM4 Converter G0375A supports output of high-amplitude PAM4 signals and independent 3 Eye level control.

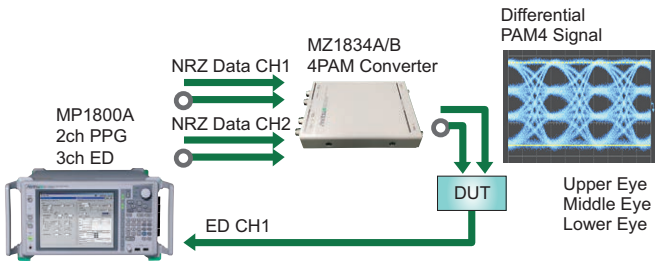
- High-amplitude PAM 4ch output
- Wideband 32.1-Gbaud rate
- High quality and low Jitter
- PAM4 Linearity control

True BER Measurement of 32Gbaud PAM4 Signal

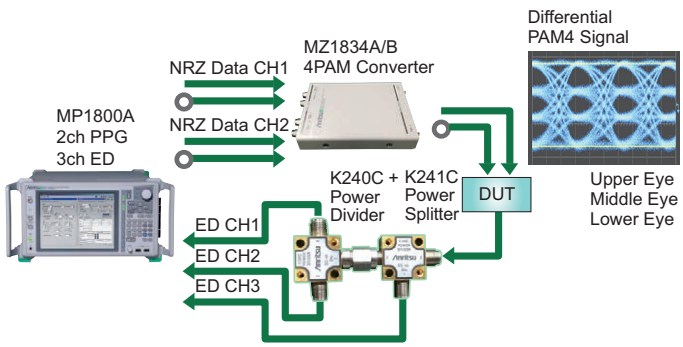
BER measurement of PAM4 signals requires accurate measurement of bit error rates in each of three Eye patterns using a 3-ch Error Detector (ED). However, each Eye data pattern must be a programmable pattern due to differences in regular PRBS. Moreover, since 2-bit data is split between three Eye patterns, errors may be counted twice by mistake at simple error measurements for each Eye, so the true BER cannot be measured.
The BER of the three Eye patterns of a PAM4 data signal can be measured simultaneously by combining the K240C Power Divider and K241C Power Splitter with the MU18304xB High-Sensitivity ED. Additionally, the True BER of PAM4 signals can be measured using both the MP1800A long-memory programmable pattern function and the error mask function for removing unwanted errors.
In addition, the standard built-in functions support separate BER measurements for each of the Top/Middle/Bottom Eye parts, repeated Auto Search and BER measurements using ED 1ch, and calculation and display of PAM4 total BER results from measured results.
Moreover, versatile automatic measurement functions* enable easy and efficient testing.

- Auto Search function automatically detects each decision point (both the amplitude and phase) of Upper, Middle and Lower Eye.
- Simultaneous Bathtub Jitter measurement for PAM 3Eyes
- Eye Margin, Eye Diagram and Q-value measurement

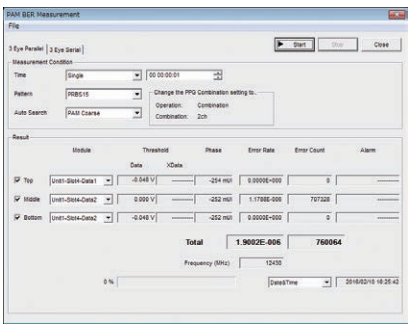
*: MP1800A Software Version 7.9 or later.
Eye Height >50 mV at the input of ED is required for PAM4 automatic measurement function.



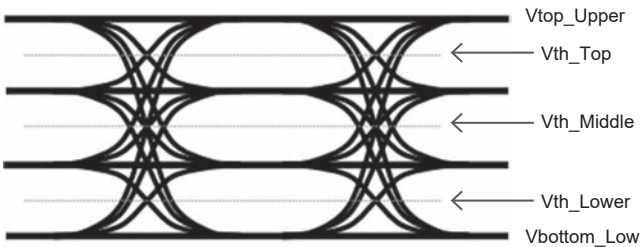
PAM4 Total BER Measurement



True BER Measurement at PAM4 signal



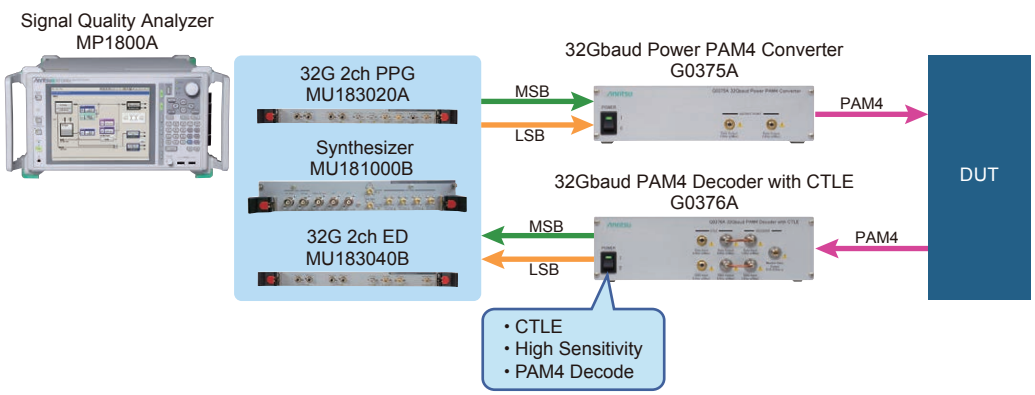
PAM4 Total BER Measurement Screen



Sampling Measurement of PAM4 Signal at 1ch ED

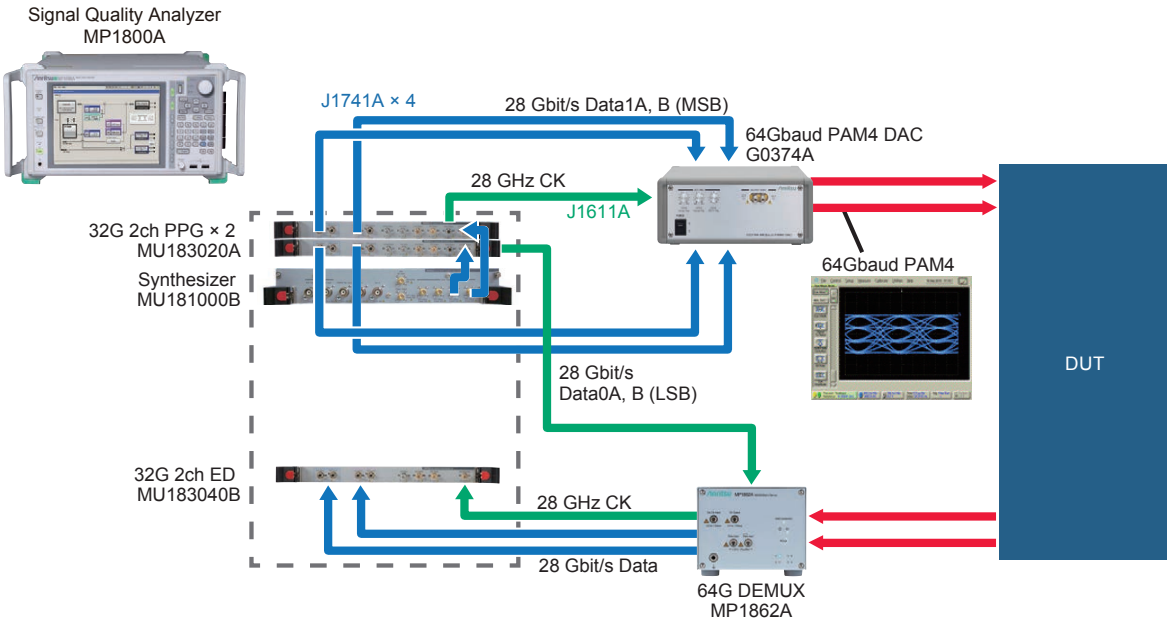
Moreover, the MSB and LSB can be measured separately, and the BER can be measured in real-time using the high input sensitivity of the 32Gbaud PAM4 Decoder with CTLE G0376A and PAM4 Decode function.

- Baud Rate of 10 to 32.1 Gbaud
- High Input Sensitivity of 40 mV typ. (per Eye, Single-end, G0376A Data input)
- Continuously Variable CTLE Gain of –12 to 0 dB for PAM4 BER Measurement after Adjustment of Eye Opening
- Real-time PAM4 BER Measurement using PAM4 Decoder + 2ch Error Detector
- CDR function (with MU183040B-022)
- Compact Remote Head for Close DUT Measurement (Remote Control between G0376A and MP1800A)



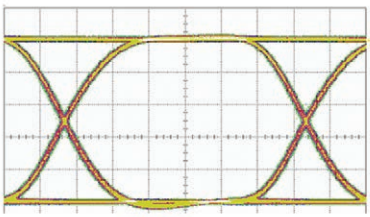
64Gbaud PAM4 BER Measurements

The G0374A 64Gbaud PAM4 DAC has two built-in 64G 2:1 multiplexers for generating 64-Gbaud PAM4 signals simply by using a 32-Gbit/s NRZ signal source (PPG). The compact, all-in-one G0374A connects to the DUT using a Remote Head with short cable to minimize loss and provide high-quality waveform PAM4 signals.
Moreover, BER measurements of PAM4 signals up to 56Gbaud are supported by combining the 56G/64G bit/s DEMUX MP1862A and 32G ED.

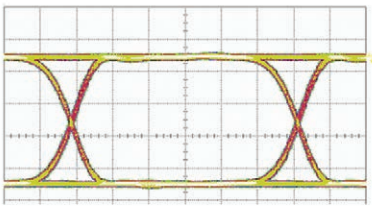


Low-jitter High-quality Waveforms

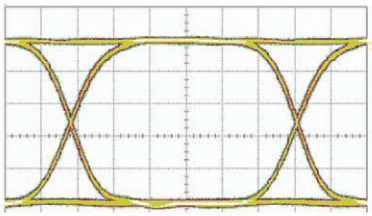
The combination of low-jitter, high-quality output waveform, and high-amplitude output PPG modules can be tailored to the application.
• Low Jitter: 8 ps p-p (MU181020B-012)
• High Amplitude: 0.5 Vp-p to 3.5 Vp-p (MU181020B-013)



MU181020B-011



MU181020B-012

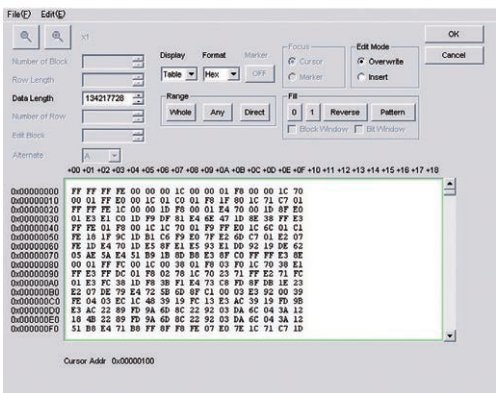


MU181020B-013

10 Gbit/s, PRBS31, Maximum amplitude

Versatile Pattern Generation

• Pseudorandom patterns (PRBS)
Because all PRBS rates required by the standards are supported up to PRBS $2^{31} - 1$, all BER are supported.
$2^n - 1$ (n = 7, 9, 10, 11, 15, 20, 23, 31)
• Zero Substitution Pattern
All 0s and All 1s patterns can be added to PRBS patterns for performing CDR tolerance tests.
2^n, $2^n - 1$ (n = 7, 9, 10, 11, 15, 20, 23)
• Data Pattern
Patterns required by each application can be created with flexibility.
128 Mbits max. (Steps: 1-bit)
• Alternate Pattern
Two patterns (A and B) can be set and the A/B pattern can be output at any timing.
• Mixed Pattern
A mixed data and PRBS pattern can be output. At creation of SONET/SDH frames, adding a PRBS $2^{31} - 1$, etc., pattern to the payload allows setting of a continuous pattern across frames.
• Sequence Pattern
A variety of programmable patterns can be output in any sequence and combining various patterns offers effective support for applications requiring sequence processing.
• PAM4 Pattern
J03A, J03B, Linearity test pattern, SSPR, PRQS 10, 13, PRBS 13Q, Gray PRBS 13Q



Data Pattern Setting Screen

High Input Sensitivity & Wide Phase Margin

Using the high-input sensitivity ED Rx function supports direct input and evaluation of low-amplitude data.
• Input Sensitivity
MU181040B-002: 10 mVp-p (typ.)
• Phase Margin
MU181040B-002: 60 ps (typ.) (12.5 Gbit/s)

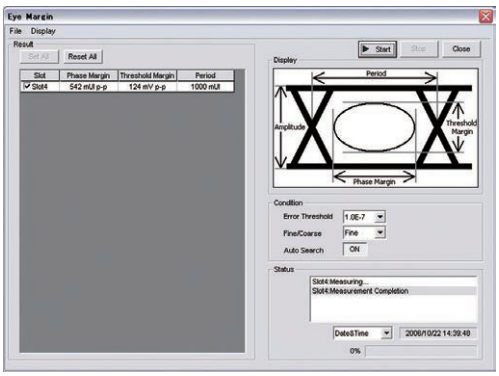
Burst Measurement

The following application evaluations using burst signals are supported.
• E-PON, G-PON, 10GE-PON Upstream Test
• Optical Loop Test
• Transmission Test using Quantum Noise Technology

∗: Functions and specifications are different according to the module. Refer to the Specification and Brochure for each module.

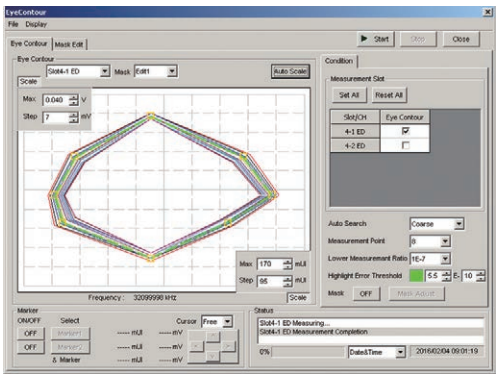
Eye Margin

For confirming DATA threshold and phase margins.



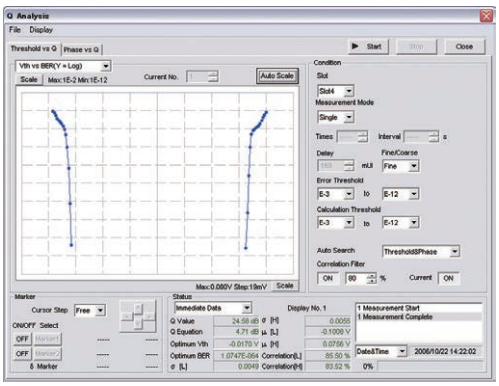
Eye Contour Function

Contours can be estimated quickly up to BER 1E-20 based on the Bathtub estimate.
Any of the Upper/Middle/Lower part of the Eye of either NRZ or PAM4 signals can be specified and measured.



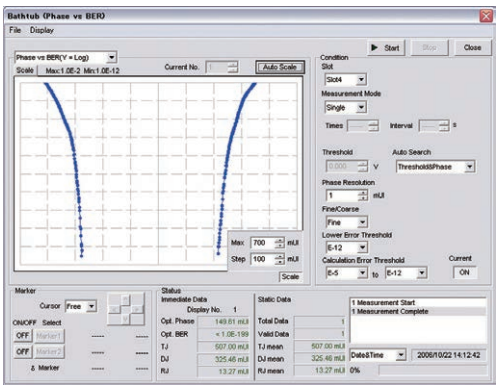
Q Measurement

Calculates Q value from bit error rate using change in threshold value. Can be used to check change in Q value for clock phase.



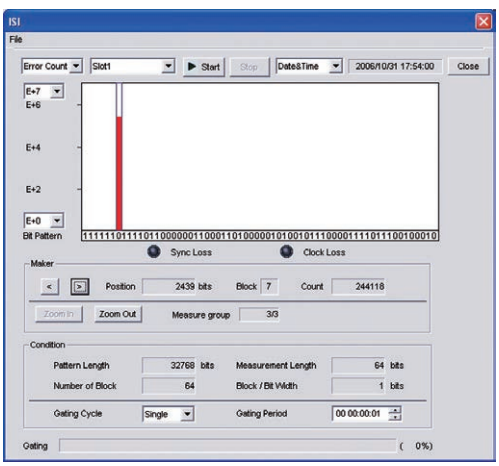
Bathtub

Performs optimum bit error rate based on changes in bit error rate relative to phase. And performs jitter analysis (TJ, DJ, RJ).



Bit Error Analysis using ISI

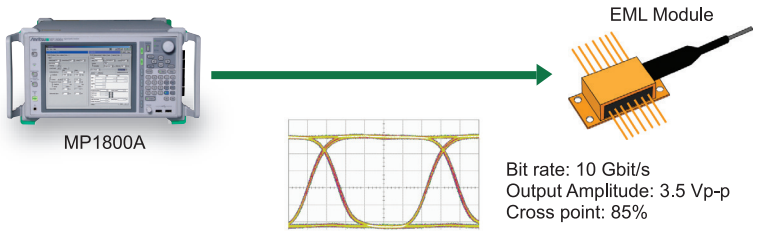
Used to confirm bit error rate in each specified block or bit position and for bit error rate correlation with inter-symbol interference.



∗: Functions and specifications are different according to the module.
Refer to the Specification and Brochure for each module.

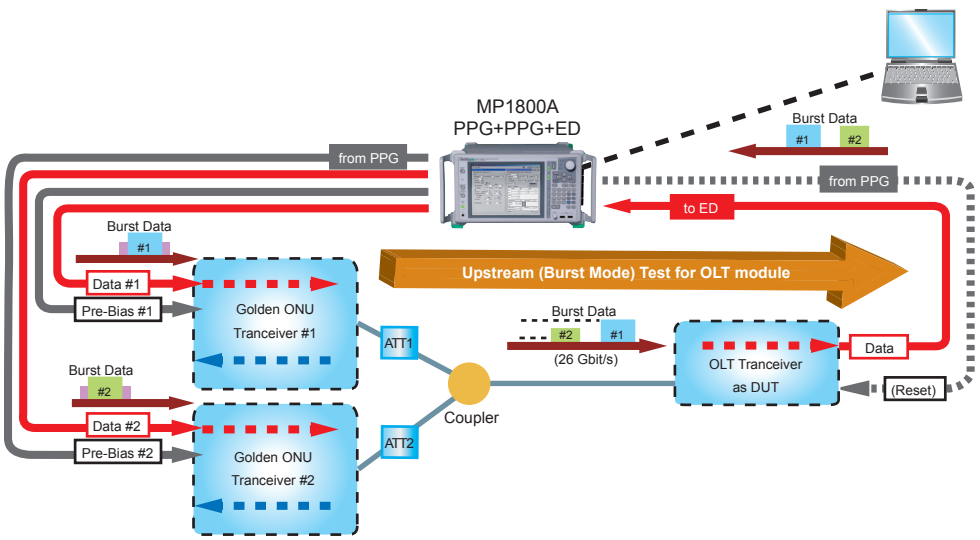
Applications

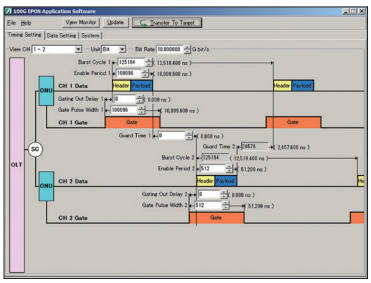
Application 1: EA/EML Module Evaluation



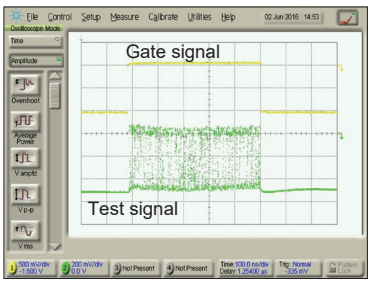
- Direct driving of EML and EA module using 3.5 Vp-p high-amplitude waveform
- Wide cross point adjustment function: 20 to 90% [MU181020B-013]

Application 2: 25G/100G PON OLT Module Evaluation





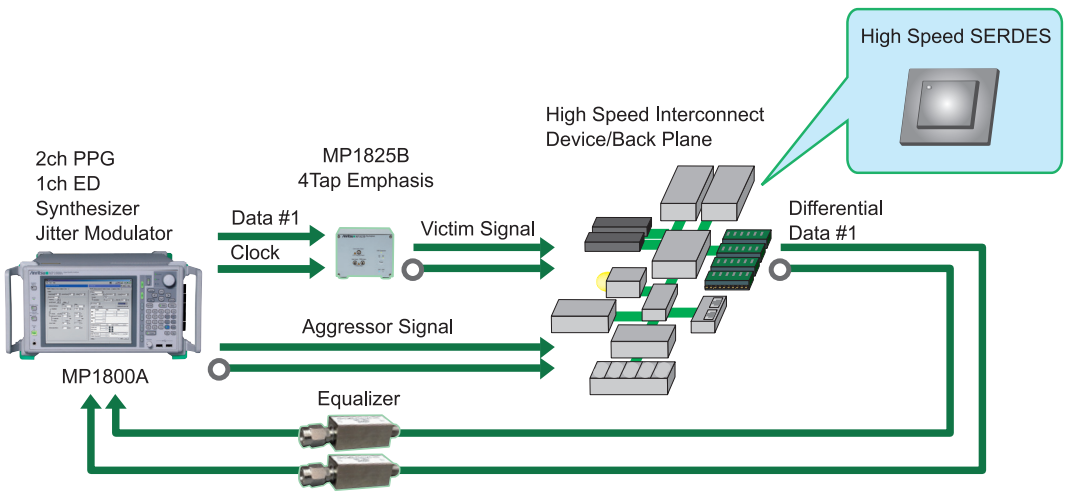
Example of control screen



Reference burst signals

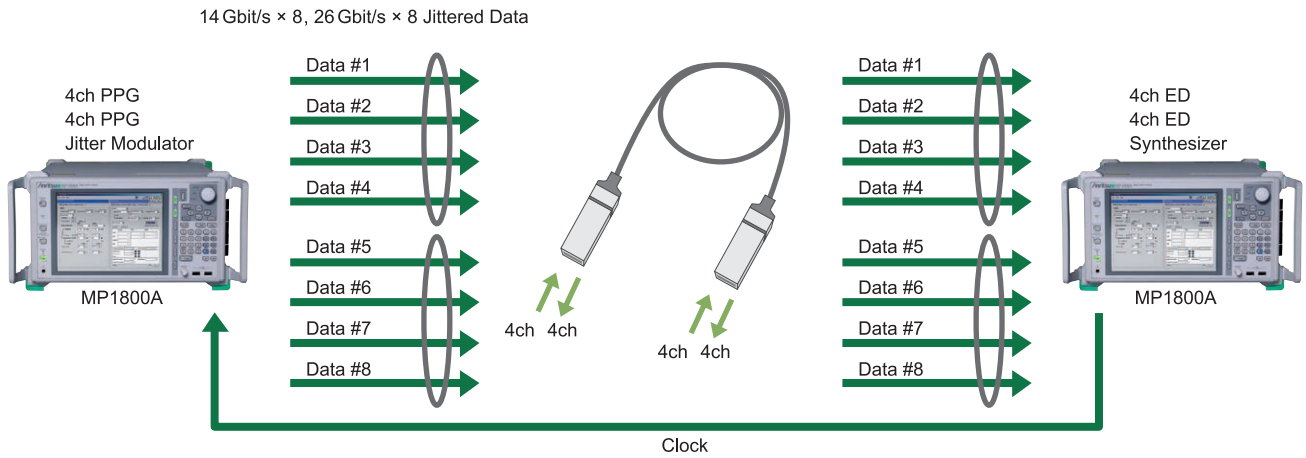
- The PON OLT Upstream test can be performed using one MP1800A and MX180014A 100G EPON Application Software

Application 3: 32 Gbit/s Band Ultrafast Interconnect Evaluation



- 32.1 Gbit/s Multi-channel signal generation
- Jitter Tolerance test
- Emphasis efficiency check
- Crosstalk test

Application 4: AOC (Active Optical Cable) Evaluation

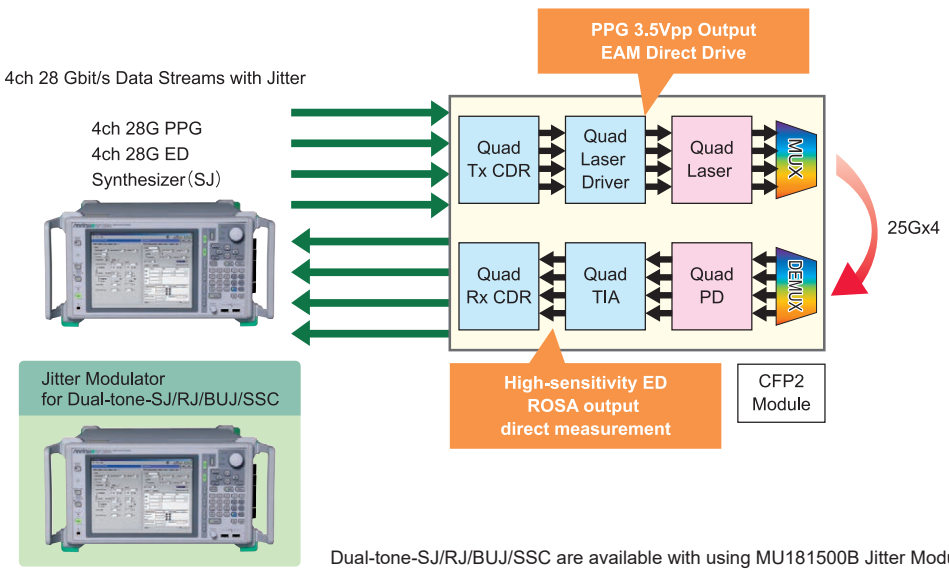


- Simultaneous 8ch (2 × 4ch end-to-end) BER measurement
- Crosstalk test
- Jitter Tolerance test
- Bathtub Jitter, Eye Diagram analysis

INFINIBAND™
TRADE ASSOCIATION MEMBER

Anritsu MP1800A is recognized to test equipment for IBTA Integrators' List.

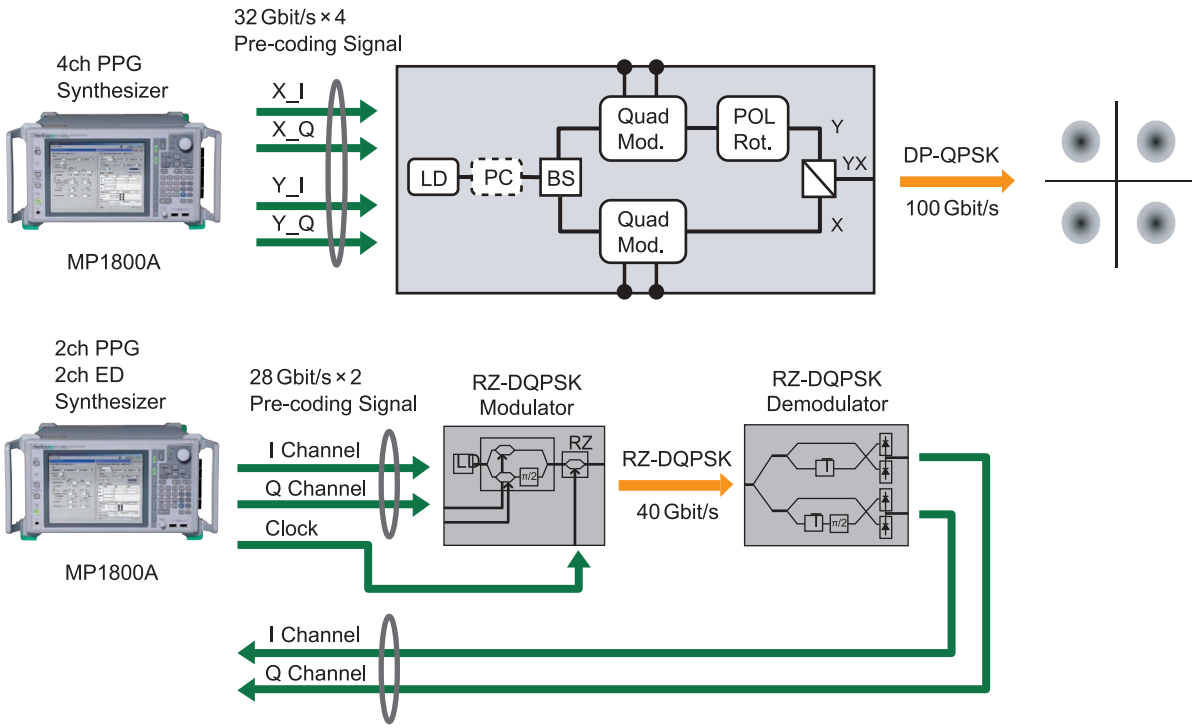
Application 5: 100 GbE/400 GbE Devices CFP2/CFP4/CFP8 Evaluation



Dual-tone-SJ/RJ/BUJ/SSC are available with using MU181500B Jitter Modulation Unit.

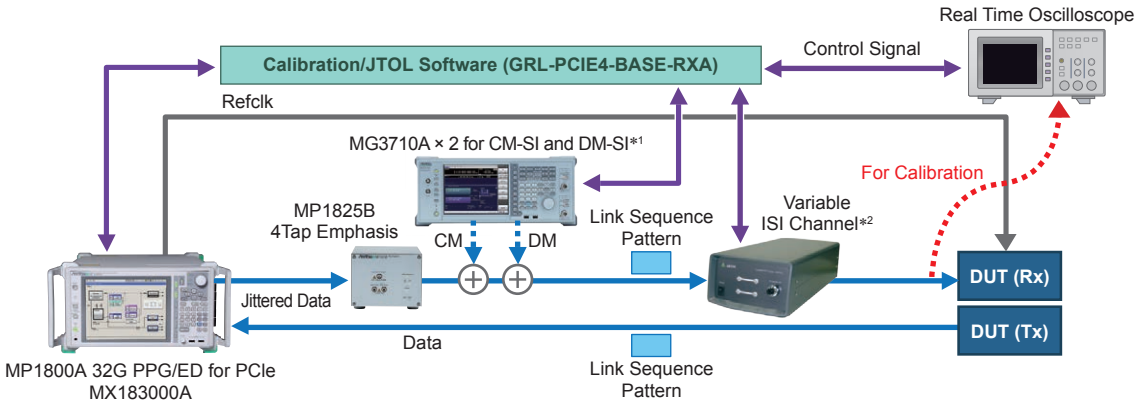
- Simultaneous 4ch BER measurement
- Optical output waveform optimization using cross-point adjustment
- Inter-lane timing and skew control
- Jitter Tolerance test
- High-quality and high-amplitude waveform ideal for EML module evaluation (3.5 Vp-p option)

Application 6: 100 Gbit/s Band DP-QPSK and 40 Gbit/s Band DQPSK Evaluation



- Pre-coding signal generator synchronized between channels
- Optical output waveform optimization using cross-point adjustment
- Timing control and skew control between channels
- Modulator input level tolerance

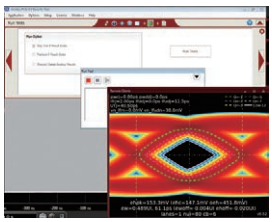
PCI Express Device Evaluation Setup



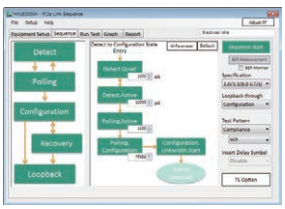
*1: The MG3710A is used at common mode noise and differential mode noise loads.
*2: The Variable ISI Channel is used at the ISI (Inter Symbol Interference) load test.

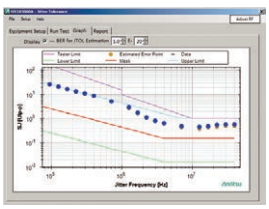
Required Functions

- Loopback State Setting Function
- Jitter Tolerance Function
- Automatic Receiver Test Function



Automated Stressed Rx Eye Calibration with Seasim





PCIe Link Sequence Generate Screen

Measurement Item	Supported Software
Stressed Signal Calibration	GRL-PCIE4-BASE-RXA(PCI Express 4.0 Rx Base Spec)
Transition to Loopback State	MX183000A (Option PL011)
Jitter Tolerance Test	MX183000A (Option PL011, Jitter Tolerance Margin Measurement) GRL-PCIE4-BASE-RXA (Pass/Fail Evaluation)

Supported Standards: PCI Express (1.x/2.0/3.x/4.0)

DUT	Link Sequence Generation	Jitter Tolerance Test
When both Common Clock Architecture and DUT Loopback data SSC OFF	Supported	Supported
When both Common Clock Architecture and DUT Loopback data not SSC OFF	Not supported	Not supported

Link Sequence Generation

The Link status required for measurement can be configured automatically using the MX183000A and options.

- Controls status of PCI Express Rev 1.x/2.0/3.x/4.0 devices and evaluates Logical Sub Block

Jitter Tolerance Tests

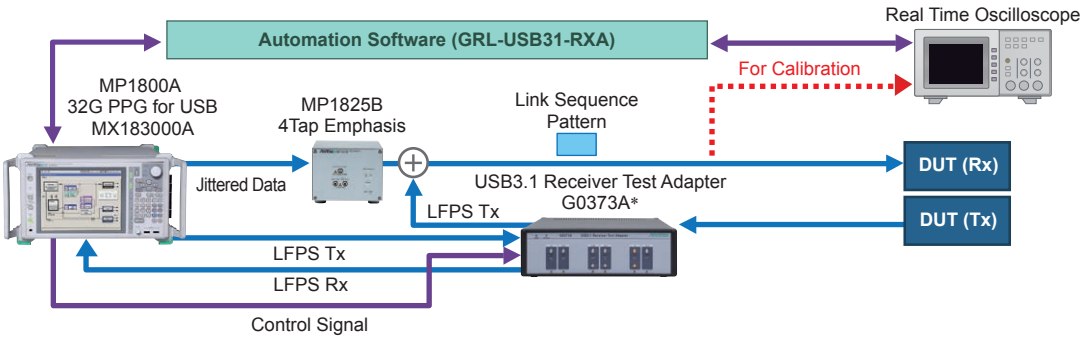
- SJ/RJ required for evaluating PCI Express 4.0 devices can be impressed to support PHY device Jitter tolerance tests.
- Device margins can be verified using low-rate BER estimates.
- Measurement results can be saved as HTML or CSV format reports.

Receiver Test

Calibration and the Jitter Tolerance test can both be automated using the GRL-PCIE4-BASE-RXA software. Automation helps cut design verification times.

* The GRL-PCIE4-BASE-RXA software is a Granite River Labs product.

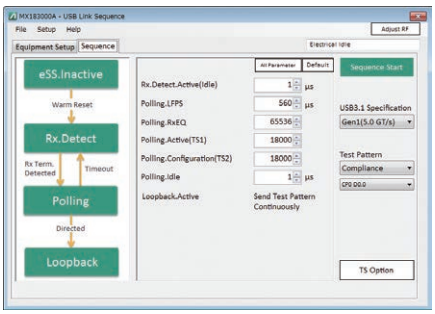
USB Device Evaluation Setup



*: G0373A is used for LFPS (Low Frequency Periodic Signal) generation and BER measurement.

Required Functions

- Loopback State Setting Function
- Jitter Tolerance Function
- Automatic Receiver Test Function



USB Link Sequence Setting Screen

Measurement Item	Supported Software
Stressed Signal Calibration	GRL-USB31-RXA
Transition to Loopback State	MX183000A (Option PL012)
Jitter Tolerance Test	MX183000A (Option PL012), GRL-USB31-RXA

Supported Standards: USB (3.0/3.1 Gen1 and Gen2)

DUT	Link Sequence Generation	Jitter Tolerance Test
Host Device	Supported	Supported

Link Sequence Generation

The Link status required for measurement can be configured automatically using the MX183000A and options.

- The test mode can be transitioned to the Loopback mode required for evaluating USB3.1 Gen1 and Gen2 devices. (MX183000A-PL012)

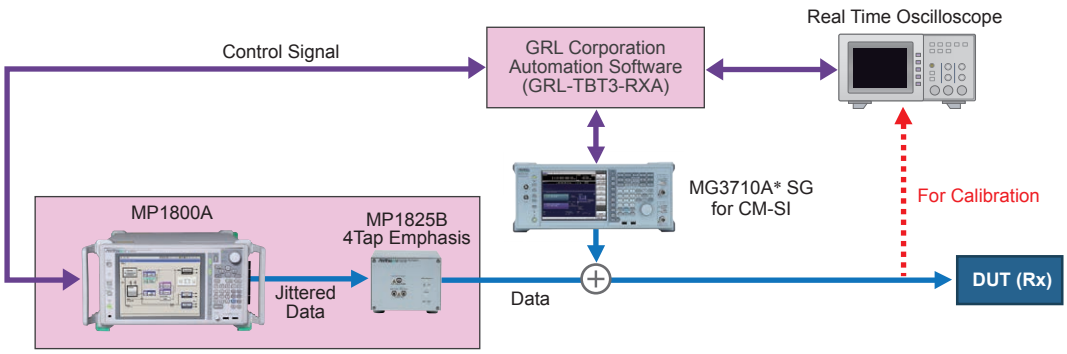
BER Measurements

The BER of USB3.1 Gen1 and Gen2 devices can be measured from the Link status probability.

Receiver Test

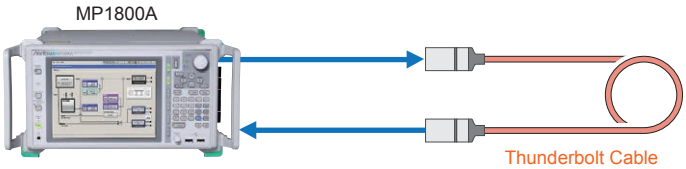
Calibration and the Jitter Tolerance test can both be automated using the GRL-USB31-RXA. Automation helps cut design verification times.

Thunderbolt Device Evaluation Setup



∗: The MG3710A is used at common mode noise loads.

Thunderbolt Cable Evaluation Setup



Required Functions

- 20 Gbit/s PPG
- Stressed Signal Calibration Function
- Jitter Tolerance Function

Anritsu MP1800A is recognized to recommended test equipment for Thunderbolt Compliance Test.

Measurement Item	Supported Software
Stressed Signal Calibration	GRL-TBT3-RXA (Thunderbolt 3)
Jitter Tolerance Test	GRL-TBT3-RXA (Pass/Fail) Evaluation

Supported Standards: Thunderbolt (2/3)

DUT	Jitter Tolerance Test
Host Device	Supported

Supports Thunderbolt 3

Supports Thunderbolt 3 specified bit rates (20G)

Stressed Signal Calibration

GRL Automation Software supports automatic stressed signal calibration as specified by Thunderbolt 3 (USB Type-C Thunderbolt Alternate Mode Electrical Host/Device Compliance Test Specification).

Stressed Signal Input Test

- Supports Rx BER measurements required by Host/Device compliance test
- Supports automatic Rx test using Tenlira scripts
- Supports automatic Pass/Fail measurement for Rx stressed signal tests

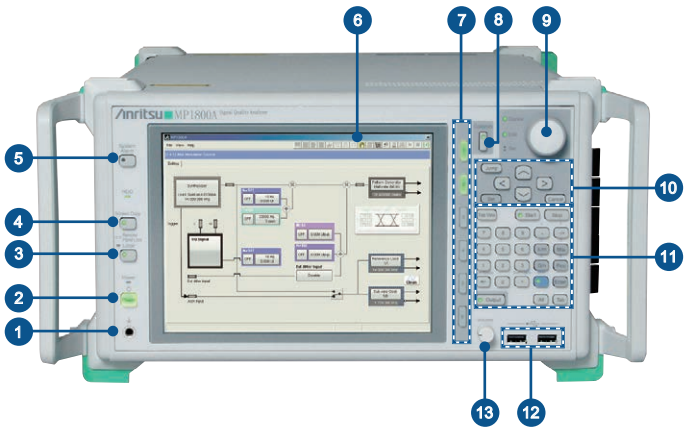
Receiver Test

Calibration and the Jitter Tolerance test can both be automated using the GRL-TBT3-RXA software. Automation helps cut design verification times.

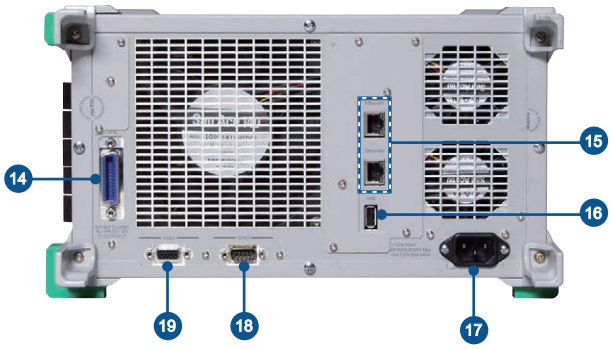
∗ The GRL-PCIE4-BASE-RXA and GRL-TBT3-RXA software are Granite River Labs products.

Panel Layout

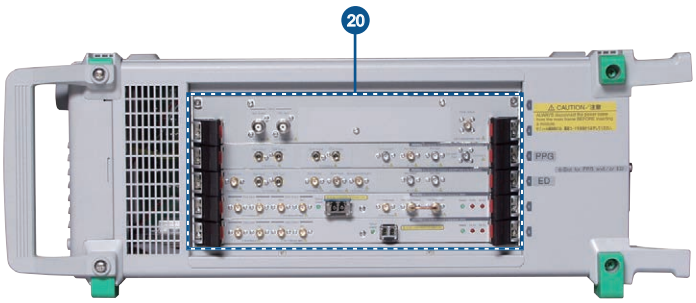
MP1800A Signal Quality Analyzer (6-Slot)



Front



Rear



Side (Right)

1 **Ground**
This terminal is used to discharge static electricity.

2 **Power**

3 **Panel Lock/Remote**
This key locks the panel operation keys.

4 **Screen Copy**
This key copies the currently displayed screen.

5 **System Alarm**
The key LED lights at a system error and a dialog explaining the error contents is displayed.

6 **Display**
8.4-inch Color TFT 800 × 600 pixels

7 **Slot Keys**
These keys correspond to the operation screen for each installed module.

8 **Customize Key**
This key is used to call up to eighteen commonly used screens.

9 **Rotary Encoder**
When the [Edit] key lamp is lit, turning this rotary encoder increases or decreases numeric values. When the [Cursor] key lamp is lit, the operation item can be set. Press the rotary encoder to switch between the [Edit] and [Cursor] functions.

10 **Cursor Key**
These keys move the screen cursor up, down, left and right on screen.

11 **Ten Key**
These ten keys are for inputting numeric values, units, etc.

12 **USB**
Two Rev. 1.1 USB ports

13 **Volume**
This knob increases and decreases the volume of the measurement error alarm.

14 **GPIB**
This connector is used when the MP1800A-001 GPIB option is installed.

15 **Ethernet**
This unit has two RJ45 Ethernet jacks supporting connection to 10 BASE-T or 100 BASE-TX cables.

16 **USB**
Rev. 1.1 USB port

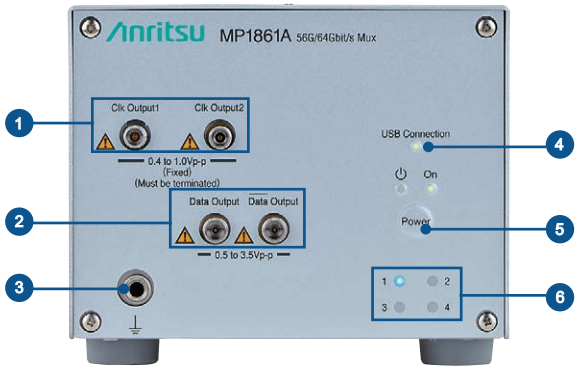
17 **AC Inlet**
This socket is for connecting the 3-wire power cord.

18 **GPIO**
Reserved for future use.

19 **VIDEO**
This connector is for an external display.

20 **Slots for Modules**
These slots are for installing up to six modules.

MP1861A 56G/64G bit/s MUX



Front

Rear

1 **Clock Output 1 Connector**
Clock Output 2 Connector
Outputs Clock reference for DUT and MP1862A

2 **Data Output Connector**
Data Output Connector
Output 2:1 MUXed differential Data signals

3 **Ground Jack**
Grounds connected wrist strap and Ground on a DUT to discharge static charges

4 **USB Connection LED**
Indicates connection status with MP1800A or PC controller

5 **Power Switch**
Switches power between on and standby

6 **Channel LEDs**
Indicate channel numbers

7 **DC Input Connector**
Connects to AC adapter

8 **Ext. Clock Input Connector**
Inputs Clock reference signal for this instrument

9 **Ground Jack**
Grounds connected wrist strap and Ground on a DUT to discharge static charges

10 **Data Input 1 Connector**
Data Input 2 Connector
Inputs Data signal from MU18302 xA

11 **1/2 Clock Output Connector**
Outputs 1/2 frequency divided Clock of Clock input to Ext. Clock Input connector

12 **USB Port**
Connects MP1800A or PC to this instrument

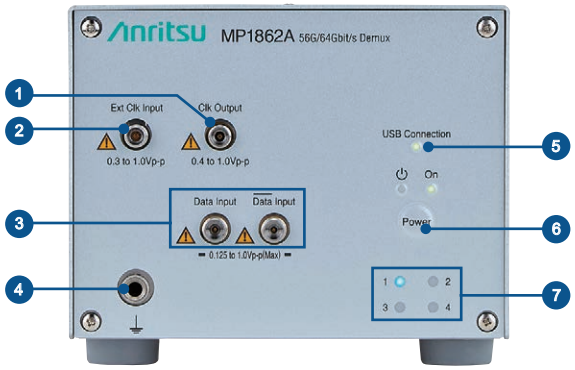
13 **Buffered Clock Output Connector**
Outputs same Clock frequency as Clock input to Ext. Clock Input connector

14 **Channel Setting Switch**
Sets instrument channel number

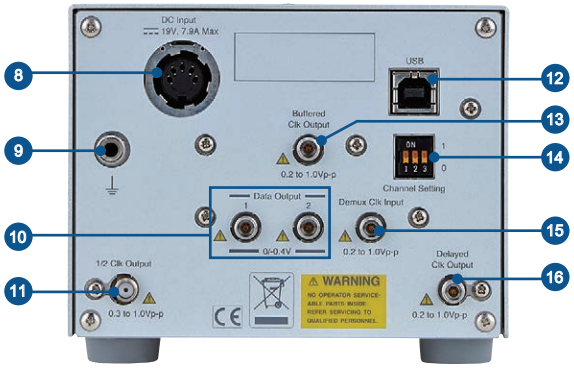
15 **Mux Clock Input Connector**
For input of Clock with same frequency as Clock input to Ext. Clock input connector

16 **Delayed Clock Output Connector**
Outputs Clock with same frequency as Clock input to Ext. Clock input connector

MP1862A 56G/64G bit/s DEMUX



Front



Rear

1 **Clock Output Connector**
Outputs same Clock frequency as Clock input to Ext. Clock Input connector

2 **Ext. Clock Input Connector**
Inputs Clock reference signal for this instrument

3 **Data Input Connector**
Data Input Connector
Inputs differential data signal

4 **Ground Jack**
Grounds connected wrist strap and Ground on a DUT to discharge static charges

5 **USB Connection LED**
Indicates connection status with MP1800A or PC controller

6 **Power Switch**
Switches power between on and standby

7 **Channel LEDs**
Indicate channel numbers

8 **DC Input Connector**
Connects to AC adapter

9 **Ground Jack**
Grounds connected wrist strap and Ground on a DUT to discharge static charges

10 **Data Output 1 Connector**
Data Output 2 Connector
Outputs 1:2 divided Data/Input signal.
Outputs Data signal to MU18304xA/B

11 **1/2 Clock Output Connector**
Outputs 1/2 frequency divided Clock of Clock input to Ext. Clock Input connector.
Outputs Clock signal to MU18304xA/B

12 **USB Port**
Connects MP1800A or PC to this instrument

13 **Buffered Clock Output Connector**
Outputs same Clock frequency as Clock input to Ext. Clock Input connector

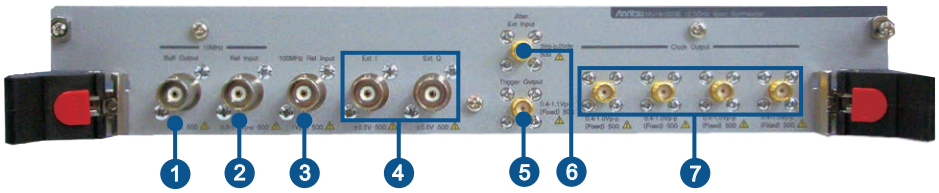
14 **Channel Setting Switch**
Sets instrument channel number

15 **Demux Clock Input Connector**
For input of same frequency as Clock input to Ext. Clock input connector when necessary

16 **Delayed Clock Output Connector**
Outputs Clock with same frequency as Clock input to Ext. Clock input connector

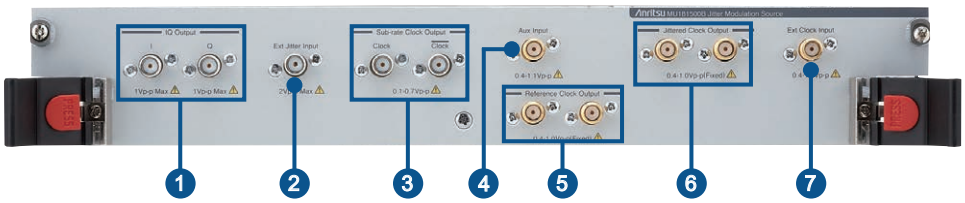
MP1800 Series Modules

• MU181000B 12.5 GHz 4port Synthesizer



1	10 MHz Buff Output	Output for 10 MHz reference clock	5	Trigger Output*1	Output for 1/64 clock or 1/1 clock
2	10 MHz Ref Input	Input for 10 MHz reference clock			
3	100 MHz Ref Input*1	Input for 100 MHz reference clock	6	Jitter Ext Input*1	Input for jitter modulation signal
4	Ext I, Q*1	Input for I, Q signal	7	Clock Output 1 to 4	Clock output 1 to 4

• MU181500B Jitter Modulation Source



1	IQ Output	Outputs IQ signals	5	Reference Clock Output	Outputs two 1/1, 1/2, or 1/4 frequency-divided clocks based on either of following inputs: • Ext Clock Input • Aux Input
2	Ext Jitter Input	Input for modulation signal source			
3	Sub-rate Clock Output	Outputs frequency-divided clock (1/8 to 1/256) based on either of following inputs: • Ext Clock Input • Aux Input	6	Jittered Clock Output	Outputs two jitter-modulated clock signals
4	Aux Input	Input clock signals	7	Ext Clock Input	Input for external clock

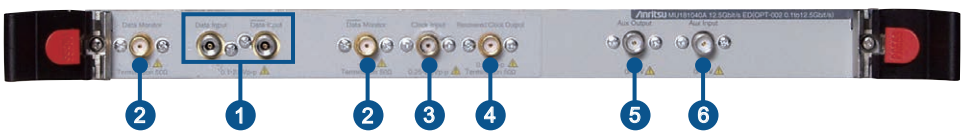
• MU181800B 14 GHz Clock Distributor

1	Clock Output 1 to 5	Outputs for divided clock of Clock Input	2	Clock Input	Clock input

• MU181020B 14 Gbit/s PPG

1	Data/$\overline{\text{Data}}$ Output	Output for differential data signal	4	Aux Output	Output for auxiliary signal
2	Clock/$\overline{\text{Clock}}$ Output*2	Output for differential clock signal	5	Aux Input	Input for auxiliary signal
3	Gating Output	Output for burst timing signal	6	Ext. Clock Input	Clock input

• MU181040B 14 Gbit/s ED

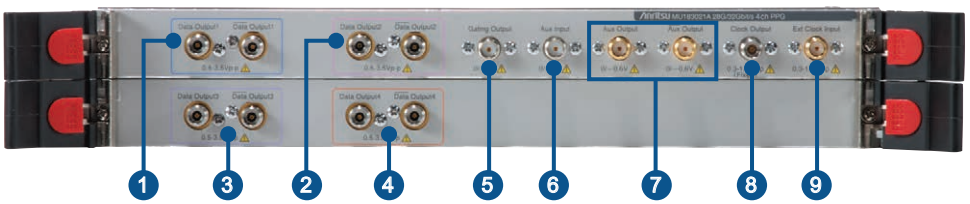


1	Data/$\overline{\text{Data}}$ Input	Input for differential data signal	4	Recovered Clock Output*4	Output for regenerated clock from input data
2	Data/$\overline{\text{Data}}$ Monitor*3	Output for divided clock of input data	5	Aux Output	Output for auxiliary signal
3	Clock Input*3	Clock input	6	Aux Input	Input for auxiliary signal

- **MU183020A 28G/32G bit/s PPG (1ch or 2ch)**

1	Data1/XData1 Output*5	Output for 1ch differential data signal	5	Aux/XAux Output	Output for differential auxiliary signal
2	Data2/XData2 Output*6	Output for 2ch differential data signal	6	Clock Output	Output for clock signal
3	Gating Output	Output for burst timing signal	7	Ext Clock Input	Input for external clock signal
4	Aux Input	Input for auxiliary signal			

- **MU183021A 28G/32G bit/s 4ch PPG**

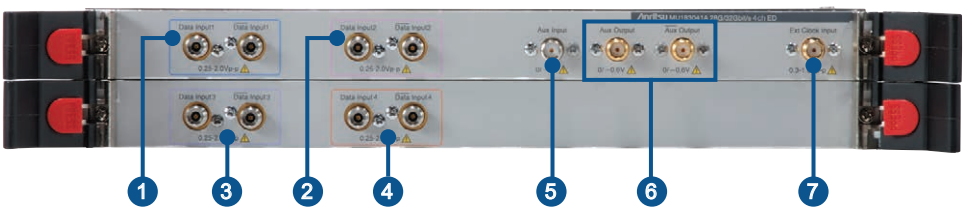


1	Data1/XData1 Output	Output for 1ch differential data signal	6	Aux Input	Input for auxiliary signal
2	Data2/XData2 Output	Output for 2ch differential data signal	7	Aux/XAux Output	Output for differential auxiliary signal
3	Data3/XData3 Output	Output for 3ch differential data signal	8	Clock Output	Output for clock signal
4	Data4/XData4 Output	Output for 4ch differential data signal	9	Ext Clock Input	Input for external clock signal
5	Gating Output	Output for burst timing signal			

- **MU183040B 28G/32G bit/s High Sensitivity ED (1ch or 2ch)**

1	Data1/XData1 Input*5	Input for 1ch differential data signal	4	Aux/XAux Output	Output for differential auxiliary signal
2	Data2/XData2 Input*6	Input for 2ch differential data signal	5	Ext Clock Input	Input for external clock signal
3	Aux Input	Input for auxiliary signal			

- **MU183041B 28G/32G bit/s 4ch High Sensitivity ED**



1	Data1/XData1 Input	Input for 1ch differential data signal	5	Aux Input	Input for auxiliary signal
2	Data2/XData2 Input	Input for 2ch differential data signal	6	Aux/XAux Output	Output for differential auxiliary signal
3	Data3/XData3 Input	Input for 3ch differential data signal	7	Ext Clock Input	Input for external clock signal
4	Data4/XData4 Input	Input for 4ch differential data signal			

∗1: Only enabled when Jitter Modulation option (MU181000B-001) installed
∗2: Single-end outputs
∗3: Only enabled when 0.1 Gbit/s to 14 Gbit/s option (MU181040B-002) installed
∗4: Only enabled when MU181040B-020/120 installed
∗5: Data/XData when 1ch option was selected.
∗6: Not implemented when 1ch option was selected.

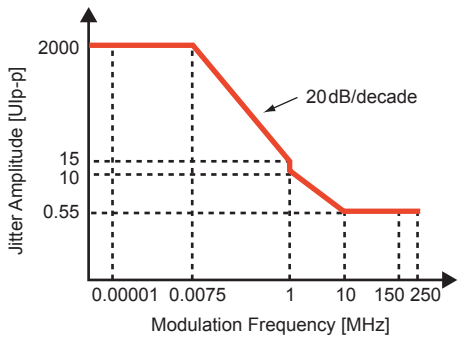
Specifications

● MP1800A Signal Quality Analyzer

LCD Display		8.4-inch Color TFT, 800 × 600 pixels
Peripheral Interface		VGA out (SVGA), USB 1.1 (3 Ports)
Remote Interface		GPIB [MP1800A-001], LAN (2 ports) [MP1800A-002]
Options		4-slot PPG and/or ED [MP1800A-015]
Power Supply		100 V(ac) to 120 V(ac)/200 V(ac) to 240 V(ac) [auto-switching between 100 V(ac)/200 V(ac)], 47.5 Hz to 63 Hz
Power Consumption		≤600 VA
Operating Temperature		5° to 40°C
Dimensions and Mass		320 (W) × 177 (H) × 450 mm (D), ≤13 kg (without modules)
CE	EMC	2014/30/EU, EN61326-1, EN61000-3-2
	LVD	2014/35/EU, EN61010-1
	RoHS	2011/65/EU, EN50581

● MP1861A 56G/64G bit/s MUX

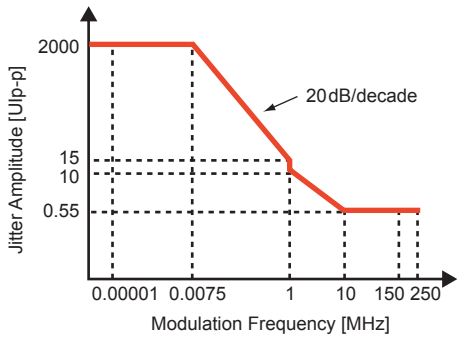
Operational Bit-rate Range	8 Gbit/s to 56.2 Gbit/s 8 Gbit/s to 64.2 Gbit/s (with Option 01 installed)
External Clock Input (Half-rate Clock Input)	Number of Input: 1 Frequency: 4 GHz to 28.1 GHz 4 GHz to 32.1 GHz (with Option 01 installed) Amplitude: 0.3 Vp-p to 1.0 Vp-p Termination: 50Ω/AC Coupling Connector: K (f)
Data Input	Number of Input: 2 (Data Input1, Data Input2) Input level: 0/–0.7 V (H: –0.15 to +0.05, L: –0.85 to –0.55) Termination: 50Ω/GND Connector: K (f)
1/2 Clock Output	Number of Output: 1 Frequency: 2 GHz to 14.05 GHz 2 GHz to 16.05 GHz (with Option 01 installed) Output amplitude: 0.3 Vp-p to 1.0 Vp-p Termination: 50Ω/AC Coupling Connector: SMA (f)
Clock Output 1, 2	Number of Output: 2 (Clock Output1, Clock Output2) Frequency: 4 GHz to 28.1 GHz 4 GHz to 32.1 GHz (with Option 01 installed) Output amplitude: 0.4 Vp-p to 1.0 Vp-p Termination: 50Ω/AC Coupling Connector: K (f)
Buffered Clock Output	Number of Output: 1 Frequency: 4 GHz to 28.1 GHz 4 GHz to 32.1 GHz (with Option 01 installed) Output amplitude: 0.2 Vp-p to 1.0 Vp-p Termination: 50Ω/AC Coupling Connector: K (f)
Delayed Clock Output	Number of Output: 1 Frequency: 4 GHz to 28.1 GHz 4 GHz to 32.1 GHz (with Option 01 installed) Output amplitude: 0.2 Vp-p to 1.0 Vp-p Termination: 50Ω/AC Coupling Connector: K (f)
MUX Clock Input	Number of Input: 1 Frequency: 4 GHz to 28.1 GHz 4 GHz to 32.1 GHz (with Option 01 installed) Amplitude: 0.2 Vp-p to 1.0 Vp-p Termination: 50Ω/AC Coupling Connector: K (f)

<table>
<tr><td rowspan="4">Data Output*1</td><td>Option x11</td><td>Option x13</td></tr>
<tr><td colspan="2">Number of Output: 2 (Data Output/ Data Output)</td></tr>
<tr><td>Amplitude: 0.5 Vp-p to 2.5 Vp-p/2 mV Step (@≤56.2 Gbit/s)
1.0 Vp-p to 2.5 Vp-p/2 mV Step (@>56.2 Gbit/s)</td><td>Amplitude: 0.5 Vp-p to 3.5 Vp-p/2 mV Step (@≤56.2 Gbit/s)
1.0 Vp-p to 3.5 Vp-p/2 mV Step (@>56.2 Gbit/s)</td></tr>
<tr><td colspan="2">Setting Error: ±50 mV ±17% of Amplitude*2, *3, *4
Offset: –2.0 to +3.3 Voh/1-mV Step, min.: –4.0 Vol
Setting Error: ±65 mV ±10% of Offset (Vth) ± (Output amplitude setting error/2)
Current Limit: Source 100 mA/Sink 100 mA
Crosspoint: 45 to 55%/0.1% Step (≤56.2 Gbit/s)
>56.2 Gbit/s, with MP1861A-x 01 installed: Since >50% is not assured, displays Overload
Tr/Tf: Typ. 8 ps (20 to 80%)*2, *3, *4
Half Period Jitter: –20 to 20/1 Step
Jitter (rms): 450 fs typ., ≤550 fs*2, *4, *5
Jitter (rms): 650 fs typ.*3, *4, *5
Random Jitter (rms): 200 fs typ.*2, *4, *5
Waveform Distortion (0-peak): ±25 mV ±10% of Amplitude typ.*2, *3, *4, *6
ON/OFF Output Switch Function
Termination: AC/DC switchable, 50Ω/GND, –2 V, +1.3 V (at DC selection)
Connector: V (f)</td></tr>
<tr><td>Jitter Tolerance</td><td colspan="2">56.2 Gbit/s, 64.2 Gbit/s (with Option 01 installed), at PRBS 2^{31} – 1, Mark ratio 1/2,
Crosspoint 50%, MP1861A – MP1862A Loopback, Temperature: +20° to +30°C
56.2 Gbit/s up to 250 MHz modulation frequency; 64.2 Gbit/s up to 150 MHz modulation frequency
 
</td></tr>
<tr><td>Variable Data Delay</td><td colspan="2">Variable Phase Range: –64000 mUI to +64000 mUI/4 mUI Step
Phase Setting Error: ±50 mUIp-p typ.*5</td></tr>
<tr><td>Control Interface</td><td colspan="2">USB 2.0 or 1.1 Type B × 1</td></tr>
<tr><td>Channel Setting</td><td colspan="2">1ch to 4ch Selectable</td></tr>
<tr><td>Power Supply (AC adapter)</td><td colspan="2">Input Voltage: 100 V(ac) to 240 V(ac)*7
Input Frequency: 50 Hz to 60 Hz
Output power: 19 V(dc), 7.9 A (max.)</td></tr>
<tr><td>Power Consumption</td><td colspan="2">19 V(dc), 4 A</td></tr>
<tr><td>Dimensions and Mass</td><td colspan="2">120 (W) × 90.9 (H) × 140 (D) mm (Excluding protrusions), ≤5 kg</td></tr>
<tr><td>Temperature</td><td colspan="2">Operation: +15° to +35°C (with options installed)
Storage: –20° to +60°C</td></tr>
</table>

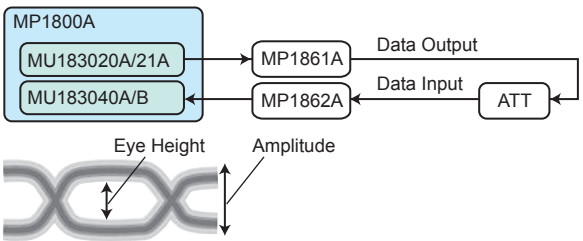
∗1: Unless otherwise described, at PRBS 2^{31} – 1, Mark Ratio 1/2. Values observed using J1656A coaxial cable and 70-GHz band sampling oscilloscope
∗2: At 56.2 Gbit/s
∗3: 64.2 Gbit/s (with MP1861A Option x01 installed)
∗4: Crosspoint: 50%
∗5: Jitter Standard values when oscilloscope intrinsic jitter ≤200 fs
∗6: Output Amplitude: 2.5 Vp-p
∗7: Operation voltage: +10% and –15% of specified voltage

● MP1862A 56G/64G bit/s DEMUX

Operational Bit-rate Range	8 Gbit/s to 56.2 Gbit/s 8 Gbit/s to 64.2 Gbit/s (with Option 01 installed)
External Clock Input (Half-rate Clock Input)	Number of Input: 1 Frequency: 4 GHz to 28.1 GHz 4 GHz to 32.1 GHz (with Option 01 installed) Amplitude: 0.3 Vp-p to 1.0 Vp-p Termination: 50Ω/AC Coupling Connector: K (f)
Data Output	Number of Output: 2 (Data Output1, Data Output2) Output Level: 0/–0.4 V (H: –0.1 to +0.1, L: –0.6 to –0.3) Termination: 50Ω/GND Connector: K (f)
1/2 Clock Output	Number of Output: 1 Frequency: 2 GHz to 14.05 GHz 2 GHz to 16.05 GHz (with Option 01 installed) Output amplitude: 0.3 Vp-p to 1.0 Vp-p Termination: 50Ω/AC Coupling Connector: SMA (f)
Clock Output	Number of Output: 1 Frequency: 4 GHz to 28.1 GHz 4 GHz to 32.1 GHz (with Option 01 installed) Output amplitude: 0.4 Vp-p to 1.0 Vp-p Termination: 50Ω/AC Coupling Connector: K (f)
Buffered Clock Output	Number of Output: 1 Frequency: 4 GHz to 28.1 GHz 4 GHz to 32.1 GHz (with Option 01 installed) Output amplitude: 0.2 Vp-p to 1.0 Vp-p Termination: 50Ω/AC Coupling Connector: K (f)
Delayed Clock Output	Number of Output: 1 Frequency: 4 GHz to 28.1 GHz 4 GHz to 32.1 GHz (with Option 01 installed) Output amplitude: 0.2 Vp-p to 1.0 Vp-p Termination: 50Ω/AC Coupling Connector: K (f)
DEMUX Clock Input	Number of Input: 1 Frequency: 4 GHz to 28.1 GHz 4 GHz to 32.1 GHz (with Option 01 installed) Amplitude: 0.2 Vp-p to 1.0 Vp-p Termination: 50Ω/AC Coupling Connector: K (f)
Data Input	Number of Input: 2 (Data Input/ $\overline{\text{Data}}$ Input), Differential Amplifier: Single-ended, 50Ω, Differential 50Ω, Differential 100Ω selectable Data, XData selectable Tracking, Independent, Alternate selectable At Alternate setting: Data-XData, XData-Data selectable (Absolute value of Data, XData Threshold Difference: 3.0 V max.) Input Data Format: NRZ Amplitude: 0.125 Vp-p to 1.0 Vp-p*1, *2 Threshold Voltage: –3.5 V to +3.3 V/1-mV step (independently settable Data, selectable. Absolute value of Data, XData Threshold Difference: 3.0 V max.) Input Sensitivity: 25 mV typ., ≤40 mV*1, *3, *4, *5 30 mV typ.*1, *4, *5, *6 Phase Margin: 200° typ.*3, *6, *7 Termination: 50Ω/GND, Variable Termination Voltage: –2.5 V to +3.5 V/0.01-V step at Variable setting Connector: V (f)

Jitter Tolerance	56.2 Gbit/s, 64.2 Gbit/s (with Option 01 installed), PRBS 2^{31} – 1, Mark ratio 1/2, Crosspoint 50%, MP1861A – MP1862A Loopback, Temperature: +20° to +30°C 56.2 Gbit/s up to 250 MHz modulation frequency; 64.2 Gbit/s up to 150 MHz modulation frequency 
Variable Clock Phase	Variable Phase Range: –1000 mUI to +1000 mUI/4 mUI Step Phase Setting Error: ±50 mUIp-p typ.*8
Automatic Measurement	Auto Search, Eye Margin, Eye Diagram, Bathtub
BER Measurement Result Display	With indication screens
Control Interface	USB 2.0 or 1.1 Type B × 1
Channel Setting	1ch to 4ch Selectable
Power Supply (AC adapter)	Input Voltage: 100 V(ac) to 240 V(ac)*9 Input Frequency: 50 Hz to 60 Hz Output power: 19 V(dc), 7.9 A (max.)
Power Consumption	19 V(dc), 4 A
Dimensions and Mass	120 (W) × 90.9 (H) × 140 (D) mm (Excluding protrusions), ≤5 kg
Temperature	Operation: +15° to +35°C (with options installed) Storage: –20° to +60°C

∗1: At single-ended, 50Ω
∗2: Amplitude range using Auto Search and Auto Measurement functions. Sensitivity at minimum error-free input amplitude.
∗3: At 56.2 Gbit/s
∗4: At PRBS 2^{31} – 1, Mark Ratio 1/2, +20° to +30°C, using J1656A coaxial cable
∗5: Standard at Eye Height. Using the measurement system shown in the following diagram (output amplitude monitored using sampling oscilloscope with bandwidth of better than 70 GHz and intrinsic jitter of less than 200 fs), Eye Height (total measurement count of 30) is the value of the amplitude measured by the oscilloscope when the BER becomes 1E-9 when the amplitude is decreased using the MP1861A + ATT.



∗6: 64.2 Gbit/s (with MP1862A Option x01 installed)
∗7: Standard with Tx intrinsic jitter component deducted
∗8: Jitter standard value when oscilloscope intrinsic jitter ≤200 fs
∗9: Operation voltage: +10% and –15% of specified voltage

● MU181000B 12.5 GHz 4port Synthesizer

Clock Output	Number of Output: 4 Frequency Range: 0.1 GHz to 12.5 GHz, Steps: 1 kHz/1 MHz Offset from Set Frequency: –1000 ppm to +1000 ppm, Steps: 1 ppm, 1 Hz (Min) Level: 0.4 Vp-p to 1 Vp-p (AC) SSB Phase Noise: ≤–80 dBc/Hz (10 kHz offset) Intrinsic Jitter: ≤20 ps p-p, ≤20 ps p-p (fc>400 MHz) Waveform: Square wave (<1 GHz), Square wave or Sine wave (≥1 GHz) Duty: 50 ±10% Inter-channel Skew: ≤10 ps (12.5 GHz) Connector: SMA(f.), Termination: 50Ω/GND
10 MHz Input	Frequency: 10 MHz ±10 ppm Level: 0.5 Vp-p to 2.0 Vp-p Waveform: Square wave or Sine wave Duty: 50 ±10% Connector: BNC, Termination: 50Ω/GND
10 MHz Output	Level: 1.0 Vp-p ±30% (AC) Waveform: Square wave Duty: 50 ±10% Connector: BNC, Termination: 50Ω/GND

● MU181000B-001 Jitter Modulation

External Modulation Input

Frequency Range: 9 Hz to 1 GHz
Level Range: 3 Vp-p, 0 V(dc) (Max.)
Waveform: Sine wave
Connector: SMA(f.), Termination: 50Ω/GND

External I, Q Input

Frequency Range: DC to 320 MHz (–3 dB)
Bandwidth Limit: 5 MHz (0.1 GHz ≤fc ≤0.4 GHz), 10 MHz (0.4 GHz <fc ≤0.65 GHz), 20 MHz (0.65 GHz <fc ≤1.4 GHz), 100 MHz (1.4 GHz <fc ≤2.4 GHz), 320 MHz (2.4 GHz <fc ≤4.0 GHz)
Level Range: ±0.5 V
Connector: BNC, Termination: 50Ω/GND

100 MHz Reference Signal Input (SSC)

Output Center Frequency is × 25 or × 50 of Reference Input Frequency
Modulation Frequency: 30 kHz to 33 kHz
Frequency Deviation: 50 kHz
Level: 1.0 Vp-p ±30% (AC)
Waveform: Square wave or Sine wave
Duty: 50 ±10%
Connector: BNC, Termination: 50Ω/GND

Trigger Output

Available from 800 MHz to 12.5 GHz of Center frequency (fc)
Frequency: 1/64 (800 MHz <fc ≤6.4 GHz), 1/1 or 1/64 selectable (6.4 GHz <fc ≤12.5 GHz)
Level: 0.4 Vp-p to 1.1 Vp-p (AC)
Connector: SMA(f.), Termination: 50Ω/GND

Internal Jitter Function

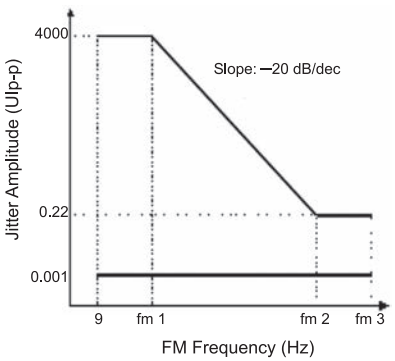
Modulation Frequency Range

Center Frequency (fc)	fm1	fm2	fm3
0.1 GHz to 0.8 GHz	13.75 Hz	250 kHz	5 MHz
0.8 GHz to 1.6 GHz	27.5 Hz	500 kHz	10 MHz
1.6 GHz to 3.2 GHz	55 Hz	1 MHz	20 MHz
3.2 GHz to 6.4 GHz	110 Hz	2 MHz	40 MHz
6.4 GHz to 12.5 GHz	220 Hz	4 MHz	80 MHz

Modulation Frequency Accuracy: ±100 ppm
Jitter Amplitude Accuracy*1:
±0.01 UI ±Q% (0.001 UIp-p to 2.19 UIp-p, fc <1 GHz)
±0.02 UI ±Q% (0.001 UIp-p to 2.19 UIp-p, fc ≥1 GHz)
±0.2 UI ±Q% (2.2 UIp-p to 21.99 UIp-p)
±2 UI ±Q% (22 UIp-p to 4000 UIp-p)

FM	Q
9 Hz≤fm≤500 kHz	7
500 kHz<fm≤2 MHz	12
2 MHz<fm≤80 MHz	15

Jitter Mask*1



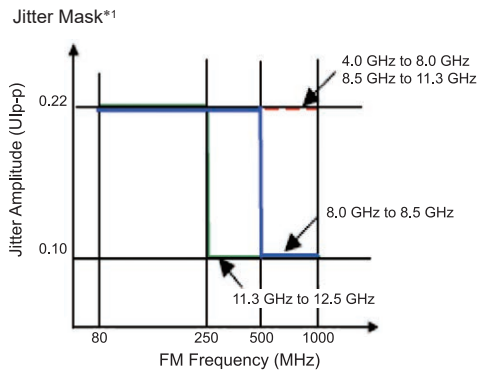
External Jitter Function

Modulation Frequency Range:
9 Hz to 5 MHz (0.1 GHz ≤fc ≤0.4 GHz)
9 Hz to 10 MHz (0.4 GHz <fc ≤0.65 GHz)
9 Hz to 20 MHz (0.65 GHz <fc ≤1.4 GHz)
9 Hz to 100 MHz (1.4 GHz <fc ≤2.4 GHz)
9 Hz to 500 MHz (2.4 GHz <fc ≤4.0 GHz)
9 Hz to 1 GHz (4.0 GHz <fc ≤12.5 GHz)
UI Range: 0.22, 2.0, 20, 200, 4000 UI

Modulation Frequency Range*1

Center Frequency	Input Frequency	Jitter Amplitude
1.4 GHz to 2.4 GHz	80 MHz to 100 MHz	Max. 0.22 UI
2.4 GHz to 4.0 GHz	80 MHz to 500 MHz	
4.0 GHz to 8.0 GHz	80 MHz to 1 GHz	
8.0 GHz to 8.5 GHz	80 MHz to 500 MHz	
	500 MHz to 1 GHz	Max. 0.10 UI
8.5 GHz to 11.3 GHz	80 MHz to 1 GHz	Max. 0.22 UI
11.3 GHz to 12.5 GHz	80 MHz to 250 MHz	Max. 0.22 UI
	250 MHz to 1 GHz	Max. 0.10 UI

Jitter Mask*1



Modulation Sensitivity: 0.22 UI Range, Input level: 0.5 Vp-p

Output Clock Frequency	FM Frequency	Input Frequency	Jitter Amplitude
0.1 GHz ≤fc ≤12.5 GHz	4 MHz	9 Hz to 4 MHz	0.1 UIp-p ±0.03 UI
	80 MHz	4 MHz to 80 MHz	
	500 MHz	80 MHz to 500 MHz	
2.4 GHz <fc ≤12.5 GHz	1 GHz	500 MHz to 1 GHz	

<table>
<tr><td>External Jitter Function</td><td>
Modulation Sensitivity: 2, 20, 200, 4000 UI Range, Input level: 0.5 Vp-p
Clock Frequency: 0.1 GHz ≤fc ≤0.8 GHz
<table>
<tr><th>Jitter Amplitude</th><th>FM Frequency</th><th>Input Frequency</th><th>Jitter Amplitude</th></tr>
<tr><td>2 UI</td><td>250 kHz</td><td>27.5 kHz</td><td>1 UIp-p ±0.3 UI</td></tr>
<tr><td>20 UI</td><td>27.5 kHz</td><td>2.75 kHz</td><td>10 UIp-p ±3 UI</td></tr>
<tr><td>200 UI</td><td>2.75 kHz</td><td>275 Hz</td><td>100 UIp-p ±30 UI</td></tr>
<tr><td>4000 UI</td><td>275 Hz</td><td>13.75 Hz</td><td>1000 UIp-p ±300 UI</td></tr>
</table>
Clock Frequency: 0.8 GHz <fc ≤1.6 GHz
<table>
<tr><th>Jitter Amplitude</th><th>FM Frequency</th><th>Input Frequency</th><th>Jitter Amplitude</th></tr>
<tr><td>2 UI</td><td>500 kHz</td><td>55 kHz</td><td>1 UIp-p ±0.3 UI</td></tr>
<tr><td>20 UI</td><td>55 kHz</td><td>5.5 kHz</td><td>10 UIp-p ±3 UI</td></tr>
<tr><td>200 UI</td><td>5.5 kHz</td><td>550 Hz</td><td>100 UIp-p ±30 UI</td></tr>
<tr><td>4000 UI</td><td>550 Hz</td><td>27.5 Hz</td><td>1000 UIp-p ±300 UI</td></tr>
</table>
Clock Frequency: 1.6 GHz <fc ≤3.2 GHz
<table>
<tr><th>Jitter Amplitude</th><th>FM Frequency</th><th>Input Frequency</th><th>Jitter Amplitude</th></tr>
<tr><td>2 UI</td><td>1 MHz</td><td>110 kHz</td><td>1 UIp-p ±0.3 UI</td></tr>
<tr><td>20 UI</td><td>110 kHz</td><td>11 kHz</td><td>10 UIp-p ±3 UI</td></tr>
<tr><td>200 UI</td><td>11 kHz</td><td>1.1 kHz</td><td>100 UIp-p ±30 UI</td></tr>
<tr><td>4000 UI</td><td>1.1 kHz</td><td>55 Hz</td><td>1000 UIp-p ±300 UI</td></tr>
</table>
Clock Frequency: 3.2 GHz <fc ≤6.4 GHz
<table>
<tr><th>Jitter Amplitude</th><th>FM Frequency</th><th>Input Frequency</th><th>Jitter Amplitude</th></tr>
<tr><td>2 UI</td><td>2 MHz</td><td>220 kHz</td><td>1 UIp-p ±0.3 UI</td></tr>
<tr><td>20 UI</td><td>220 kHz</td><td>22 kHz</td><td>10 UIp-p ±3 UI</td></tr>
<tr><td>200 UI</td><td>22 kHz</td><td>2.2 kHz</td><td>100 UIp-p ±30 UI</td></tr>
<tr><td>4000 UI</td><td>2.2 kHz</td><td>110 Hz</td><td>1000 UIp-p ±300 UI</td></tr>
</table>
Clock Frequency: 6.4 GHz <fc ≤12.5 GHz
<table>
<tr><th>Jitter Amplitude</th><th>FM Frequency</th><th>Input Frequency</th><th>Jitter Amplitude</th></tr>
<tr><td>2 UI</td><td>4 MHz</td><td>440 kHz</td><td>1 UIp-p ±0.3 UI</td></tr>
<tr><td>20 UI</td><td>440 kHz</td><td>44 kHz</td><td>10 UIp-p ±3 UI</td></tr>
<tr><td>200 UI</td><td>44 kHz</td><td>4.4 kHz</td><td>100 UIp-p ±30 UI</td></tr>
<tr><td>4000 UI</td><td>4.4 kHz</td><td>220 Hz</td><td>1000 UIp-p ±300 UI</td></tr>
</table>
</td></tr>
<tr><td>Triangle Wave Modulation</td><td>PCIe-Gen I (2.5 GHz) or PCIe-Gen II (5 GHz)
Clock Output Frequency Setting: Spread Method Center/Spread Method Down selectable
Frequency Offset: –1000 ppm to +1000 ppm, Steps: 1 ppm
Modulation Frequency Accuracy: 31.25 kHz ±1000 ppm
Frequency Deviation: ±6.25 MHz (PCIe-Gen I, 2.5 GHz), ±12.5 MHz (PCIe-Gen II, 5 GHz)
Deviation Accuracy: ±10%</td></tr>
</table>

∗1: The maximum jitter amplitude is limited according to the jitter tolerance of PPG or ED modules. Refer to the jitter tolerance specification of PPG/ED modules.

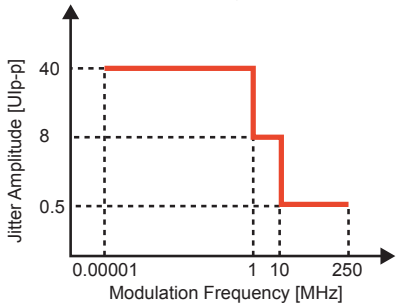
● MU181500B Jitter Modulation Source

External Clock Input	Number of Input: 1 Frequency Range: 6.400 001 GHz to 12.500 000 GHz (MU181000B, Combination: On) 0.800 000 GHz to 15.000 000 GHz (MU181000B, Combination: Off, or External synthesizer) Amplitude: 0.4 Vp-p to 1.0 Vp-p Connector: SMA(f.), Termination: 50Ω/AC Coupling
External Jitter Input	Number of Input: 1 Frequency Range: 10 kHz to 1 GHz Amplitude: 0 to 2.0 Vp-p Connector: SMA(f.), Termination: 50Ω/GND
Jittered Clock Output	Number of Output: 2 Frequency Range: 0.800 001 GHz to 1.562 500 GHz (MU181000B, Combination: On), Steps: 0.000 001 GHz 1.600 001 GHz to 3.125 000 GHz (MU181000B, Combination: On), Steps: 0.000 001 GHz 3.200 001 GHz to 6.250 000 GHz (MU181000B, Combination: On), Steps: 0.000 001 GHz 6.400 001 GHz to 12.500 000 GHz (MU181000B, Combination: On), Steps: 0.000 001 GHz 12.800 002 GHz to 15.000 000 GHz (MU181000B, Combination: On), Steps: 0.000 002 GHz 0.8 GHz to 15 GHz (MU181000B, Combination: Off, or External synthesizer) Frequency Offset: –1000 ppm to +1000 ppm (MU181000B, Combination: On), Steps: 1 ppm None (MU181000B, Combination: Off, or External synthesizer) Amplitude: 0.4 Vp-p (Min.), 1.0 Vp-p (Max.) Intrinsic Jitter: ≤350 fs (4.25, 7.0125, 10, 12.5, 14, 15 GHz) Connector: SMA(f.), Termination: 50Ω/AC Coupling
IQ Output	Number of Output: 2 (I, Q) Amplitude: 1 Vp-p (Max.) Connector: SMA(f.), Termination: 50Ω/GND
AUX Input	Number of Input: 1 Frequency Range: Same frequency with External Clock Input Amplitude: 0.4 Vp-p (Min.), 1.1 Vp-p (Max.) Connector: SMA(f.), Termination: 50Ω/AC Coupling
Reference Clock Output	Number of Output: 2 Reference Clock: External Clock Input or AUX Input (MU181000B, Combination: On) External Clock Input (MU181000B, Combination: Off, or External synthesizer) Frequency Range: 1/N of Jittered Clock Output Frequency (N: 1, 2, or 4) Amplitude: 0.4 Vp-p (Min.), 1.0 Vp-p (Max.) (Jittered Clock Output Frequency: ≥4 GHz) 0.4 Vp-p (Min.), 1.2 Vp-p (Max.) (Jittered Clock Output Frequency: <4 GHz) Connector: SMA(f.), Termination: 50Ω/AC Coupling
Sub-rate Clock Output	Number of Output: 2 (Differential) Frequency Range: 1/N of Jittered Clock Output Frequency (N: 8 to 256, Steps: 1) Amplitude: 0.1 Vp-p to 0.7 Vp-p, Steps: 10 mV Accuracy: ±70 mV ±20% of Amplitude (N: 8) Connector: SMA(f.), Termination: 50Ω/AC Coupling

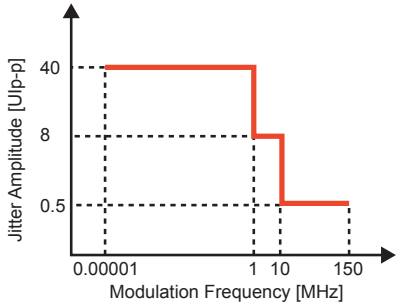
Internal Sinusoidal Jitter (SJ1)

Jitter Setting Mask*1

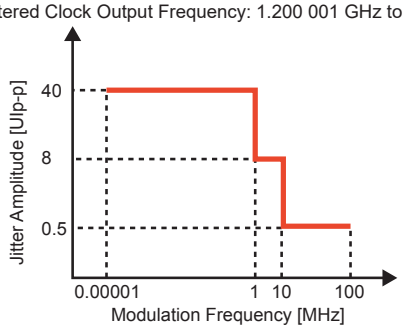
Jittered Clock Output Frequency: 8.500 001 GHz to 15 GHz



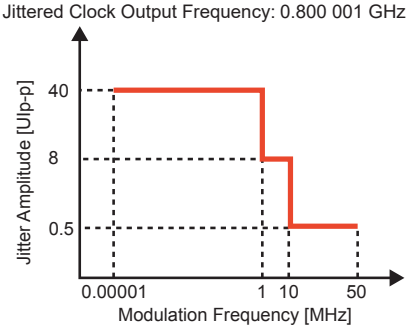
Jittered Clock Output Frequency: 4.000 001 GHz to 8.5 GHz



Jittered Clock Output Frequency: 1.200 001 GHz to 4 GHz



Jittered Clock Output Frequency: 0.800 001 GHz to 1.2 GHz



Modulation Frequency (FM): 10 Hz to 10 kHz, Steps: 1 Hz
10 kHz to 100 kHz, Steps: 10 Hz
100 kHz to 1 MHz, Steps: 100 Hz
1 MHz to 10 MHz, Steps: 1 kHz
10 MHz to 100 MHz, Steps: 10 kHz
100 MHz to 250 MHz, Steps: 100 kHz

Accuracy: ±100 ppm

Amplitude*1:

Jittered Clock Output Frequency: 8.500 001 GHz to 15 GHz
0 to 40 UIp-p (FM: 10 Hz to 1 MHz), Steps: 0.01 UI
0 to 8 UIp-p (FM: 1.001 MHz to 10 MHz), Steps: 0.01 UI
0 to 0.5 UIp-p (FM: 10.01 MHz to 250 MHz), Steps: 0.001 UI

Jittered Clock Output Frequency: 4.000 001 GHz to 8.5 GHz
0 to 40 UIp-p (FM: 10 Hz to 1 MHz), Steps: 0.01 UI
0 to 8 UIp-p (FM: 1.001 MHz to 10 MHz), Steps: 0.01 UI
0 to 0.5 UIp-p (FM: 10.01 MHz to 150 MHz), Steps: 0.001 UI

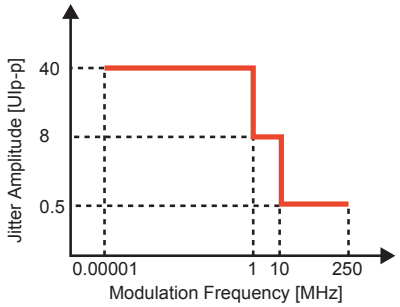
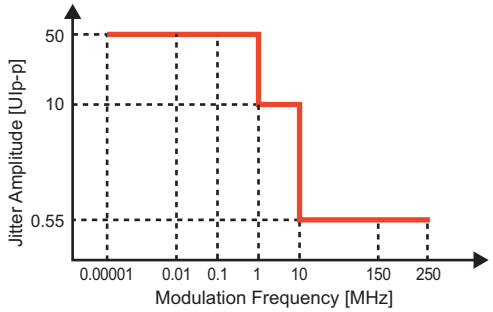
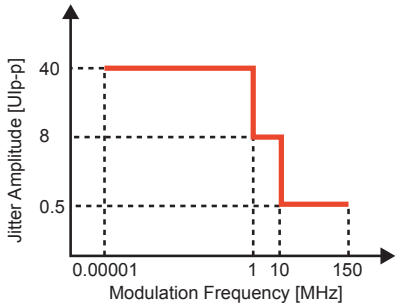
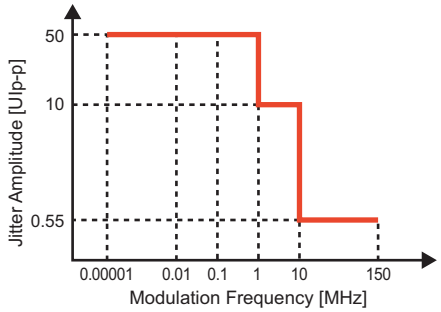
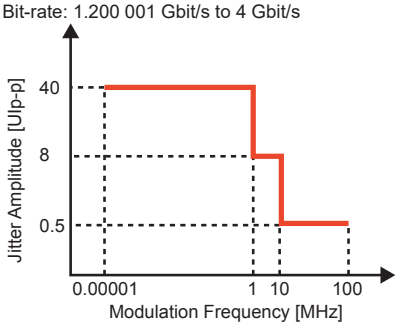
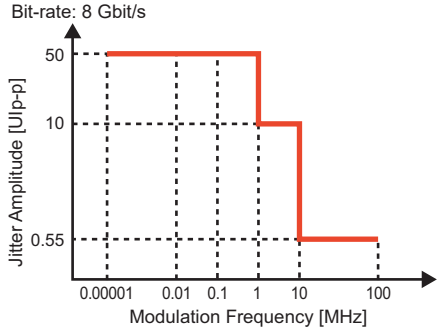
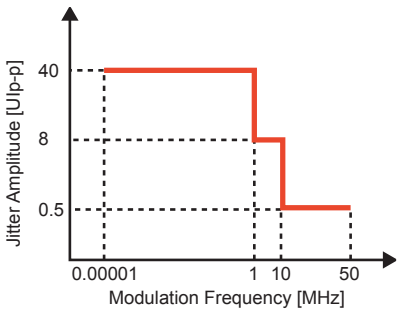
Jittered Clock Output Frequency: 1.200 001 GHz to 4 GHz
0 to 40 UIp-p (FM: 10 Hz to 1 MHz), Steps: 0.01 UI
0 to 8 UIp-p (FM: 1.001 MHz to 10 MHz), Steps: 0.01 UI
0 to 0.5 UIp-p (FM: 10.01 MHz to 100 MHz), Steps: 0.001 UI

Jittered Clock Output Frequency: 1.800 001 GHz to 1.2 GHz
0 to 40 UIp-p (FM: 10 Hz to 1 MHz), Steps: 0.01 UI
0 to 8 UIp-p (FM: 1.001 MHz to 10 MHz), Steps: 0.01 UI
0 to 0.5 UIp-p (FM: 10.01 MHz to 50 MHz), Steps: 0.001 UI

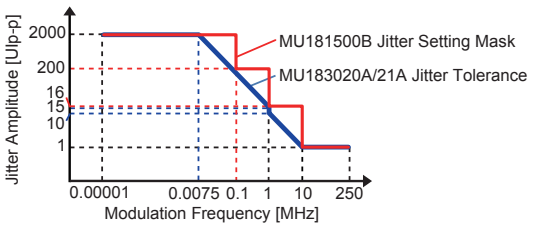
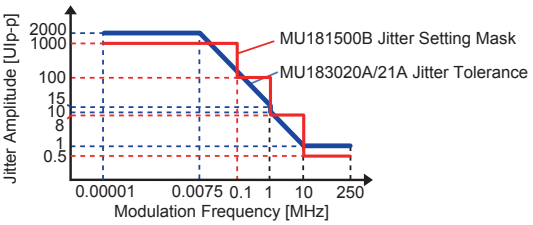
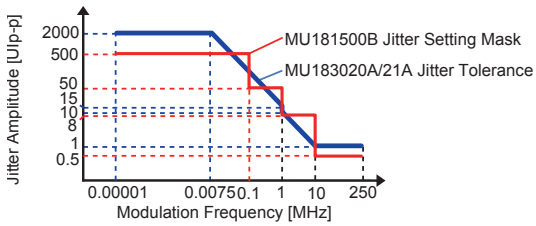
Accuracy: ±0.03 UI ±Q% (Amplitude: 0.002 UIp-p to 2.19 UIp-p)
±0.2 UI ±Q% (Amplitude: 2.2 UIp-p to 21.9 UIp-p)
±2 UI ±Q% (Amplitude: 22 UIp-p to 50 UIp-p)

FM	Q
10 Hz ≤ fm ≤ 500 kHz	7
500 kHz < fm ≤ 2 MHz	10
2 MHz < fm ≤ 80 MHz	13
80 MHz < fm ≤ 250 MHz	15

On/Off Function: Supported

Internal Sinusoidal Jitter (SJ1) [using MU181020B]	Jitter Setting Mask*1 Jittered Clock Output Frequency: 8.500 001 GHz to 15 GHz Full Rate Mode*2 Bit-rate: 8.500 001 Gbit/s to 15 Gbit/s  Half Rate Mode*2 Bit-rate: 17.000 002 Gbit/s to 28.1 Gbit/s  Jittered Clock Output Frequency: 4.000 001 GHz to 8.5 GHz Full Rate Mode*2 Bit-rate: 4.000 001 Gbit/s to 8.5 Gbit/s  Half Rate Mode*2 Bit-rate: 8.000 002 Gbit/s to 17 Gbit/s  Jittered Clock Output Frequency: 1.200 001 GHz to 4 GHz Full Rate Mode*2 Bit-rate: 1.200 001 Gbit/s to 4 Gbit/s  Half Rate Mode*2 Bit-rate: 8 Gbit/s  Jittered Clock Output Frequency: 0.800 001 GHz to 1.2 GHz Full Rate Mode*2 Bit-rate: 0.800 001 Gbit/s to 1.2 Gbit/s 

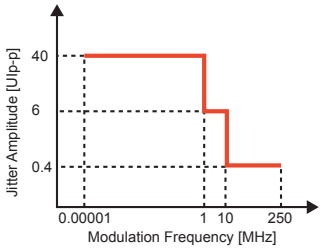
<table>
<tr>
<td>Internal Sinusoidal Jitter (SJ1)
[using MU181020B]</td>
<td>
Modulation Frequency (FM): 10 Hz to 10 kHz, Steps: 1 Hz
10 kHz to 100 kHz, Steps: 10 Hz
100 kHz to 1 MHz, Steps: 100 Hz
1 MHz to 10 MHz, Steps: 1 kHz
10 MHz to 100 MHz, Steps: 10 kHz
100 MHz to 250 MHz, Steps: 100 kHz
Accuracy: ±100 ppm
Amplitude*1:
Full Rate Mode*2 (Using MU181020B)
Bit-rate: 8.500 001 Gbit/s to 15 Gbit/s
0 to 40 UIp-p (FM: 10 Hz to 1 MHz), Steps: 0.001 UI
0 to 8 UIp-p (FM: 1.001 MHz to 10 MHz), Steps: 0.001 UI
0 to 0.5 UIp-p (FM: 10.01 MHz to 250 MHz), Steps: 0.001 UI
Bit-rate: 4.000 001 Gbit/s to 8.5 Gbit/s
0 to 40 UIp-p (FM: 10 Hz to 1 MHz), Steps: 0.001 UI
0 to 8 UIp-p (FM: 1.001 MHz to 10 MHz), Steps: 0.001 UI
0 to 0.5 UIp-p (FM: 10.01 MHz to 150 MHz), Steps: 0.001 UI
Bit-rate: 1.200 001 Gbit/s to 4 Gbit/s
0 to 40 UIp-p (FM: 10 Hz to 1 MHz), Steps: 0.001 UI
0 to 8 UIp-p (FM: 1.001 MHz to 10 MHz), Steps: 0.001 UI
0 to 0.5 UIp-p (FM: 10.01 MHz to 100 MHz), Steps: 0.001 UI
Bit-rate: 0.800 001 Gbit/s to 1.2 Gbit/s
0 to 40 UIp-p (FM: 10 Hz to 1 MHz), Steps: 0.001 UI
0 to 8 UIp-p (FM: 1.001 MHz to 10 MHz), Steps: 0.001 UI
0 to 0.5 UIp-p (FM: 10.01 MHz to 50 MHz), Steps: 0.001 UI
Accuracy: ±0.03 UI ±Q% (Amplitude: 0.002 UIp-p to 2.19 UIp-p)
±0.2 UI ±Q% (Amplitude: 2.2 UIp-p to 21.9 UIp-p)
±2 UI ±Q% (Amplitude: 22 UIp-p to 50 UIp-p)
<table>
<tr><th>FM</th><th>Q</th></tr>
<tr><td>10 Hz ≤fm ≤500 kHz</td><td>7</td></tr>
<tr><td>500 kHz <fm ≤2 MHz</td><td>10</td></tr>
<tr><td>2 MHz <fm ≤80 MHz</td><td>13</td></tr>
<tr><td>80 MHz <fm ≤250 MHz</td><td>15</td></tr>
</table>
On/Off Function: Supported
</td>
</tr>
</table>

External Sinusoidal Jitter (SJ1) [using MU183020A/21A]	32G PPG Full rate Clock Out setting, Bit-rate: 15 Gbit/s to 32.1 Gbit/s Half rate Clock Out setting, Bit-rate: 2.4 Gbit/s to 32.1 Gbit/s  Full rate Clock Out setting, Bit-rate: 4 Gbit/s to 15 Gbit/s  Full rate Clock Out setting, Bit-rate: 2.4 Gbit/s to 4 Gbit/s  32G PPG (Full rate Clock Out, Bit-rate: 4 Gbit/s to 15 Gbit/s) 0 to 1000 UIp-p (FM: 10 Hz to 100 kHz), Steps: 0.001 UI 0 to 100 UIp-p (FM: 100.1 kHz to 1 MHz), Steps: 0.001 UI 0 to 8 UIp-p (FM: 1.001 MHz to 10 MHz), Steps: 0.001 UI 0 to 0.5 UIp-p (FM: 10.01 MHz to 250 MHz), Steps: 0.001 UI 32G PPG (Full rate Clock Out, Bit-rate: 2.4 Gbit/s to 4 Gbit/s) 0 to 500 UIp-p (FM: 10 Hz to 100 kHz), Steps: 0.001 UI 0 to 50 UIp-p (FM: 100.1 kHz to 1 MHz), Steps: 0.001 UI 0 to 8 UIp-p (FM: 1.001 MHz to 10 MHz), Steps: 0.001 UI 0 to 0.5 UIp-p (FM: 10.01 MHz to 250 MHz), Steps: 0.001 UI 32G PPG (Full rate Clock Out, Bit-rate: 15 Gbit/s to 30 Gbit/s, Half rate Clock Out, Bit-rate: 2.4 Gbit/s to 30 Gbit/s) 0 to 2000 UIp-p (FM: 10 Hz to 100 kHz), Steps: 0.002 UI 0 to 50 UIp-p (FM: 100.1 kHz to 1 MHz), Steps: 0.002 UI 0 to 8 UIp-p (FM: 1.001 MHz to 10 MHz), Steps: 0.002 UI 0 to 0.5 UIp-p (FM: 10.01 MHz to 250 MHz), Steps: 0.002 UI 32G PPG (Full rate Clock Out, Half rate Clock Out, Bit-rate: 30 Gbit/s to 32.1 Gbit/s) 0 to 2000 UIp-p (FM: 10 Hz to 100 kHz), Steps: 0.004 UI 0 to 200 UIp-p (FM: 100.1 kHz to 1 MHz), Steps: 0.004 UI 0 to 16 UIp-p (FM: 1.001 MHz to 10 MHz), Steps: 0.004 UI 0 to 1 UIp-p (FM: 10.01 MHz to 250 MHz), Steps: 0.004 UI Accuracy: ±0.03 UI ±Q% (Amplitude: 0.001 to 2.199 UIp-p) ±0.2 UI ±Q% (Amplitude: 2.2 to 21.999 UIp-p) ±2 UI ±Q% (Amplitude: 22 to 219.999 UIp-p) ±20 UI ±Q% (Amplitude: 220 to 2000 UIp-p) FW / Q 10 Hz to 500 kHz / 7 500.1k Hz to 2 MHz / 10 2.01 MHz to 80 MHz / 13 80.01 MHz to 250 MHz / 15 On/Off Function: supported

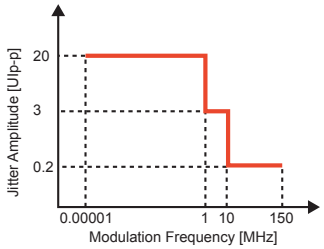
External Sinusoidal Jitter (SJ2)
[MU181000B-001]

Jitter Setting Mask*1

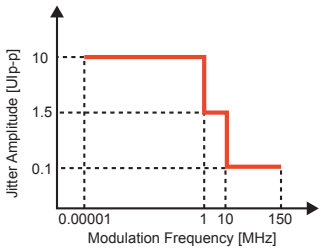
Jittered Clock Output Frequency: 6.400 001 GHz to 15 GHz
Full Rate Mode*2



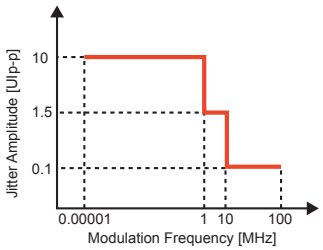
Jittered Clock Output Frequency: 3.200 001 GHz to 6.25 GHz
Full Rate Mode*2



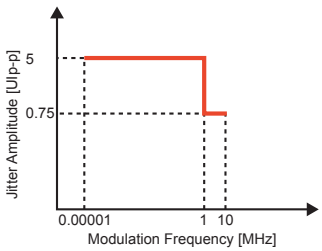
Jittered Clock Output Frequency: 1.800 001 GHz to 3.125 GHz
Full Rate Mode*2



Jittered Clock Output Frequency: 1.600 001 GHz to 1.8 GHz
Full Rate Mode*2



Jittered Clock Output Frequency: 0.800 001 GHz to 1.562 5 GHz
Full Rate Mode*2



Modulation Frequency (FM): 10 Hz to 10 kHz, Steps: 1 Hz
10 kHz to 100 kHz, Steps: 10 Hz
100 kHz to 1 MHz, Steps: 100 Hz
1 MHz to 10 MHz, Steps: 1 kHz
10 MHz to 100 MHz, Steps: 10 kHz
100 MHz to 250 MHz, Steps: 100 kHz

Accuracy: ±100 ppm

Amplitude*1:

Full Rate Mode*2

Jittered Clock Output Frequency: 6.400 001 GHz to 15 GHz
0 to 40 UIp-p (FM: 10 Hz to 1 MHz), Steps: 0.01 UI
0 to 6 UIp-p (FM: 1.001 MHz to 10 MHz), Steps: 0.01 UI
0 to 0.4 UIp-p (FM: 10.01 MHz to 250 MHz), Steps: 0.001 UI

Jittered Clock Output Frequency: 3.200 001 GHz to 6.25 GHz
0 to 20 UIp-p (FM: 10 Hz to 1 MHz), Steps: 0.01 UI
0 to 3 UIp-p (FM: 1.001 MHz to 10 MHz), Steps: 0.01 UI
0 to 0.2 UIp-p (FM: 10.01 MHz to 150 MHz), Steps: 0.001 UI

Jittered Clock Output Frequency: 1.800 001 GHz to 3.125 GHz
0 to 10 UIp-p (FM: 10 Hz to 1 MHz), Steps: 0.01 UI
0 to 1.5 UIp-p (FM: 1.001 MHz to 10 MHz), Steps: 0.01 UI
0 to 0.1 UIp-p (FM: 10.01 MHz to 150 MHz), Steps: 0.001 UI

Jittered Clock Output Frequency: 1.600 001 GHz to 1.8 GHz
0 to 10 UIp-p (FM: 10 Hz to 1 MHz), Steps: 0.01 UI
0 to 1.5 UIp-p (FM: 1.001 MHz to 10 MHz), Steps: 0.01 UI
0 to 0.1 UIp-p (FM: 10.01 MHz to 100 MHz), Steps: 0.001 UI

Jittered Clock Output Frequency: 0.800 001 GHz to 1.562 5 GHz
0 to 5 UIp-p (FM: 10 Hz to 1 MHz), Steps: 0.01 UI
0 to 0.75 UIp-p (FM: 1.001 MHz to 10 MHz), Steps: 0.01 UI

Accuracy: ±0.03 UI ±Q% (Amplitude: 0.002 UIp-p to 2.19 UIp-p)
±0.2 UI ±Q% (Amplitude: 2.2 UIp-p to 21.9 UIp-p)
±2 UI ±Q% (Amplitude: 22 UIp-p to 50 UIp-p)

FM	Q
10 Hz ≤fm ≤500 kHz	10
500 kHz <fm ≤2 MHz	13
2 MHz <fm ≤80 MHz	15
80 MHz <fm ≤250 MHz	18

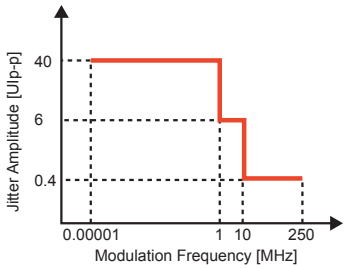
On/Off Function: Supported

External Sinusoidal Jitter (SJ2)
[using MU181000B-001
MU181020B
MU183020A/21A]

Jitter Setting Mask*1

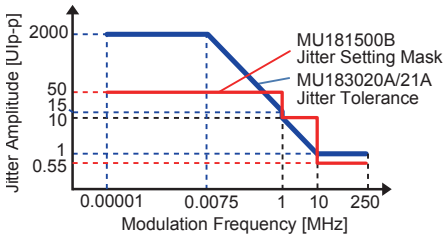
Jittered Clock Output Frequency: 6.400 001 GHz to 15 GHz

Full Rate Mode*2
Bit-rate: 6.400 001 Gbit/s to 15 Gbit/s



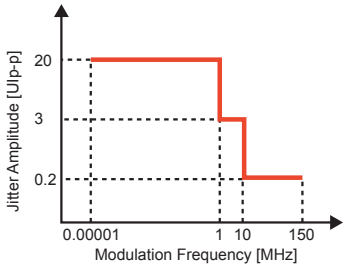
Half Rate Mode*2
Bit-rate: 12.800 001 Gbit/s to 30 Gbit/s

Quarter Rate Mode
Bit-rate: 25.600 004 Gbit/s to 32.1 Gbit/s

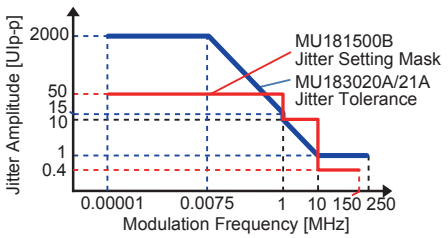


Jittered Clock Output Frequency: 3.200 001 GHz to 6.25 GHz

Full Rate Mode*2
Bit-rate: 3.200 001 Gbit/s to 6.25 Gbit/s

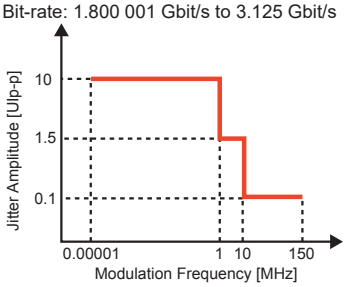


Half Rate Mode*2
Bit-rate: 8 Gbit/s to 12.5 Gbit/s

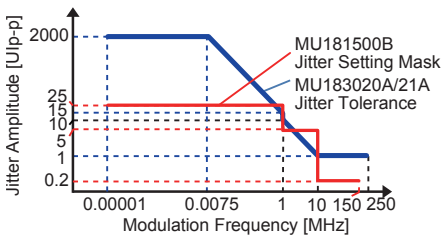


Jittered Clock Output Frequency: 1.800 001 GHz to 3.125 GHz

Full Rate Mode*2
Bit-rate: 1.800 001 Gbit/s to 3.125 Gbit/s

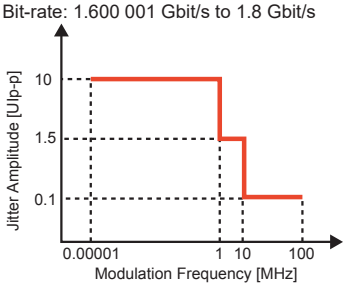


Half Rate Mode*2
Bit-rate: 3.600 002 Gbit/s to 6.25 Gbit/s

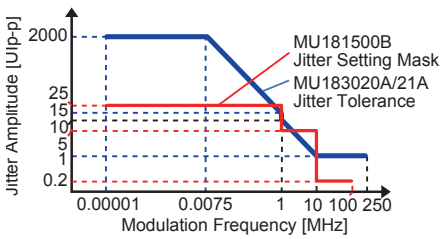


Jittered Clock Output Frequency: 1.600 001 GHz to 1.8 GHz

Full Rate Mode*2
Bit-rate: 1.600 001 Gbit/s to 1.8 Gbit/s

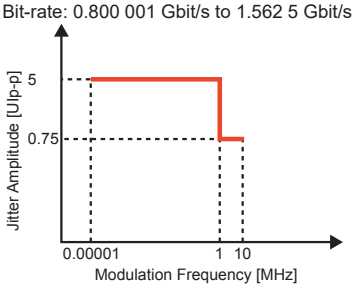


Half Rate Mode*2
Bit-rate: 3.200 002 Gbit/s to 3.6 Gbit/s

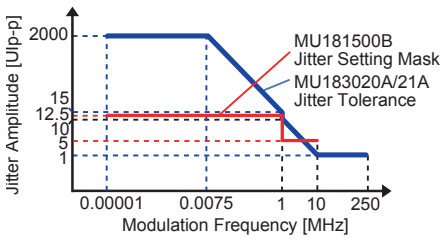


Jittered Clock Output Frequency: 0.800 001 GHz to 1.562 5 GHz

Full Rate Mode*2
Bit-rate: 0.800 001 Gbit/s to 1.562 5 Gbit/s



Half Rate Mode*2
Bit-rate: 1.600 002 Gbit/s to 3.125 Gbit/s



<table>
<tr>
<td>External Sinusoidal Jitter (SJ2)
[using MU181000B-001
MU181020B
MU183020A/21A]</td>
<td>
Modulation Frequency (FM): 10 Hz to 10 kHz, Steps: 1 Hz
10 kHz to 100 kHz, Steps: 10 Hz
100 kHz to 1 MHz, Steps: 100 Hz
1 MHz to 10 MHz, Steps: 1 kHz
10 MHz to 100 MHz, Steps: 10 kHz
100 MHz to 250 MHz, Steps: 100 kHz
Accuracy: ±100 ppm
Amplitude*1:
Full Rate Mode*2
Bit-rate: 6.400 001 Gbit/s to 15 Gbit/s
0 to 40 UIp-p (FM: 10 Hz to 1 MHz), Steps: 0.001 UI
0 to 6 UIp-p (FM: 1.001 MHz to 10 MHz), Steps: 0.001 UI
0 to 0.4 UIp-p (FM: 10.01 MHz to 250 MHz), Steps: 0.001 UI
Bit-rate: 3.200 001 Gbit/s to 6.25 Gbit/s
0 to 20 UIp-p (FM: 10 Hz to 1 MHz), Steps: 0.001 UI
0 to 3 UIp-p (FM: 1.001 MHz to 10 MHz), Steps: 0.001 UI
0 to 0.2 UIp-p (FM: 10.01 MHz to 150 MHz), Steps: 0.001 UI
Bit-rate: 1.800 001 Gbit/s to 3.125 Gbit/s
0 to 10 UIp-p (FM: 10 Hz to 1 MHz), Steps: 0.001 UI
0 to 1.5 UIp-p (FM: 1.001 MHz to 10 MHz), Steps: 0.001 UI
0 to 0.1 UIp-p (FM: 10.01 MHz to 150 MHz), Steps: 0.001 UI
Bit-rate: 1.600 001 Gbit/s to 1.8 Gbit/s
0 to 10 UIp-p (FM: 10 Hz to 1 MHz), Steps: 0.001 UI
0 to 1.5 UIp-p (FM: 1.001 MHz to 10 MHz), Steps: 0.001 UI
0 to 0.1 UIp-p (FM: 10.01 MHz to 100 MHz), Steps: 0.001 UI
Bit-rate: 0.800 001 Gbit/s to 1.562 5 Gbit/s
0 to 5 UIp-p (FM: 10 Hz to 1 MHz), Steps: 0.001 UI
0 to 0.75 UIp-p (FM: 1.001 MHz to 10 MHz), Steps: 0.001 UI
Half Rate Mode*2
Bit-rate: 12.800 001 Gbit/s to 30 Gbit/s
0 to 50 UIp-p (FM: 10 Hz to 1 MHz), Steps: 0.2 UI
0 to 10 UIp-p (FM: 1.001 MHz to 10 MHz), Steps: 0.02 UI
0 to 0.55 UIp-p (FM: 10.01 MHz to 250 MHz), Steps: 0.002 UI
Bit-rate: 8 Gbit/s to 12.5 Gbit/s
0 to 50 UIp-p (FM: 10 Hz to 1 MHz), Steps: 0.2 UI
0 to 10 UIp-p (FM: 1.001 MHz to 10 MHz), Steps: 0.02 UI
0 to 0.4 UIp-p (FM: 10.01 MHz to 150 MHz), Steps: 0.002 UI
Bit-rate: 3.600 002 Gbit/s to 6.25 Gbit/s
0 to 25 UIp-p (FM: 10 Hz to 1 MHz), Steps: 0.2 UI
0 to 5 UIp-p (FM: 1.001 MHz to 10 MHz), Steps: 0.02 UI
0 to 0.2 UIp-p (FM: 10.01 MHz to 150 MHz), Steps: 0.002 UI
Bit-rate: 3.200 002 Gbit/s to 3.6 Gbit/s
0 to 25 UIp-p (FM: 10 Hz to 1 MHz), Steps: 0.2 UI
0 to 5 UIp-p (FM: 1.001 MHz to 10 MHz), Steps: 0.02 UI
0 to 0.2 UIp-p (FM: 10.01 MHz to 100 MHz), Steps: 0.002 UI
Bit-rate: 1.600 002 Gbit/s to 3.125 Gbit/s
0 to 12.5 UIp-p (FM: 10 Hz to 1 MHz), Steps: 0.2 UI
0 to 2.5 UIp-p (FM: 1.001 MHz to 10 MHz), Steps: 0.02 UI
Quarter Rate Mode*2
Bit-rate: 25.600 004 Gbit/s to 32.1 Gbit/s
0 to 50 UIp-p (FM: 10 Hz to 1 MHz), Steps: 0.004 UI
0 to 10 UIp-p (FM: 1.001 MHz to 10 MHz), Steps: 0.004 UI
0 to 0.548 UIp-p (FM: 10.01 MHz to 250 MHz), Steps: 0.004 UI
Accuracy: ±0.03 UI ±Q% (Amplitude: 0.002 UIp-p to 2.19 UIp-p)
±0.2 UI ±Q% (Amplitude: 2.2 UIp-p to 21.9 UIp-p)
±2 UI ±Q% (Amplitude: 22 UIp-p to 50 UIp-p)
<table>
<tr><th>FM</th><th>Q</th></tr>
<tr><td>10 Hz ≤fm ≤500 kHz</td><td>10</td></tr>
<tr><td>500 kHz <fm ≤2 MHz</td><td>13</td></tr>
<tr><td>2 MHz <fm ≤80 MHz</td><td>15</td></tr>
<tr><td>80 MHz <fm ≤250 MHz</td><td>18</td></tr>
</table>
On/Off Function: Supported
</td>
</tr>
<tr>
<td>Spread Spectrum Clocking
(SSC)</td>
<td>
Type: Down-Spread, Center-Spread, Up-Spread
Modulation Frequency: 28 kHz to 34 kHz, Steps: 1 Hz
Accuracy: ±100 ppm
Deviation: 0 to 7000 ppm, Steps: 1 ppm
On/Off Function: Supported
</td>
</tr>
</table>

<table>
<tr><td>Random Jitter (RJ)</td><td>
Bandwidth: 10 kHz to 1 GHz
Crest Factor: 16 dB
Filter Type
User Filter
Filter: 10 MHz, 20 MHz, Through (HPF 3 dB bandwidth)
100 MHz, Through (LPF 3 dB bandwidth)
Amplitude*1
Full Rate Mode*2
<table>
<tr><th>Jittered Clock Output Frequency [GHz]</th><th>Setting Range [UIp-p]</th><th>Steps [mUI]</th></tr>
<tr><td>≥2.5</td><td>0 to 0.5</td><td>2</td></tr>
<tr><td><2.5</td><td>0 to 0.2f</td><td>2</td></tr>
</table>
Half Rate Mode*3
<table>
<tr><th>Jittered Clock Output Frequency [GHz]</th><th>Setting Range [UIp-p]</th><th>Steps [mUI]</th></tr>
<tr><td>≥2.5</td><td>0 to 0.5</td><td>4</td></tr>
<tr><td><2.5</td><td>0 to 0.2f</td><td>4</td></tr>
</table>
Quarter Rate Mode
<table>
<tr><th>Jittered Clock Output Frequency [GHz]</th><th>Setting Range [UIp-p]</th><th>Steps [mUI]</th></tr>
<tr><td>≥2.5</td><td>0 to 0.496</td><td>4</td></tr>
<tr><td><2.5</td><td>0 to 0.2f</td><td>4</td></tr>
</table>
f: Jittered Clock Output Frequency [GHz]
Accuracy: ±4.9 ps ±15% (Jittered Clock Output Frequency: ≥4 GHz)
±7.0 ps ±15% (Jittered Clock Output Frequency: <4 GHz)
PCIe (Data clocked) or PCIe (Common Ref. clock) Filter
Filter: LF (10 kHz to 1.5 MHz) or HF (1.5 MHz to 100 MHz) for PCIe
Amplitude*1
Full Rate Mode*2
<table>
<tr><th>Jittered Clock Output Frequency [GHz]</th><th>LF and HF Setting Range [ps rms]</th><th>Steps [ps rms]</th></tr>
<tr><td>≥4</td><td>0 to 8.8</td><td>0.1</td></tr>
</table>
Half Rate Mode*2
<table>
<tr><th>Jittered Clock Output Frequency [GHz]</th><th>LF and HF Setting Range [ps rms]</th><th>Steps [ps rms]</th></tr>
<tr><td>≥4</td><td>0 to 8.8</td><td>0.2</td></tr>
</table>
Quarter Rate Mode
<table>
<tr><th>Jittered Clock Output Frequency [GHz]</th><th>LF and HF Setting Range [ps rms]</th><th>Steps [ps rms]</th></tr>
<tr><td>≥4</td><td>0 to 8.8</td><td>0.4</td></tr>
</table>
LF Amplitude ≥ HF Amplitude
Accuracy: ±0.6 ps ±10%
On/Off Function: Supported
</td></tr>
<tr><td>Bounded Uncorrelated Jitter (BUJ)</td><td>
PRBS Pattern Length: $2^n - 1$ (n = 7, 9, 11, 15, 23, or 31)
BUJ Rate: 0.1 Gbit/s to 3.2 Gbit/s, Steps: 1 kbit/s
4.9 Gbit/s to 6.25 Gbit/s, Steps: 1 kbit/s (Jittered Clock Output Frequency: >4 GHz)
9.8 Gbit/s to 12.5 Gbit/s, Steps: 1 kbit/s (Jittered Clock Output Frequency: >4 GHz)
Filter Type (LPF 3 dB Bandwidth): 50, 100, 200, 300, 500 MHz, Through (Jittered Clock Output Frequency: >4 GHz)
50, 100, 200, 300 MHz, Through (Jittered Clock Output Frequency: ≤4 GHz)
Amplitude*1:
Full Rate Mode*2
<table>
<tr><th>Jittered Clock Output Frequency [GHz]</th><th>Setting Range [UIp-p]</th><th>Steps [mUI]</th></tr>
<tr><td>≥2.5</td><td>0 to 0.5</td><td>2</td></tr>
<tr><td><2.5</td><td>0 to 0.2f</td><td>2</td></tr>
</table>
Half Rate Mode*2
<table>
<tr><th>Jittered Clock Output Frequency [GHz]</th><th>Setting Range [UIp-p]</th><th>Steps [mUI]</th></tr>
<tr><td>≥2.5</td><td>0 to 0.5</td><td>4</td></tr>
<tr><td><2.5</td><td>0 to 0.2f</td><td>4</td></tr>
</table>
f: Jittered Clock Output Frequency [GHz]
Accuracy: ±4.9 ps ±15% (Jittered Clock Output Frequency: ≥4 GHz)
±7.0 ps ±15% (Jittered Clock Output Frequency: <4 GHz)
PRBS Pattern Length: $2^n - 1$ (n = 7, 9)
BUJ Rate: 6, 5.5, 4.9 Gbit/s, LPF 500 MHz
BUJ Rate: 3.2 Gbit/s, 3 Gbit/s, LPF 300 MHz
BUJ Rate: 3.2 Gbit/s, 2 Gbit/s, LPF 200 MHz
BUJ Rate: 2 Gbit/s, 1.1 Gbit/s, LPF 100 MHz
On/Off Function: Supported
</td></tr>
<tr><td>External Jitter</td><td>
Bandwidth: 10 kHz to 1 GHz
Accuracy*3: 0.5 UI ±10% (2 Vp-p)
Linearity*3: ±6 ps ±10%
On/Off Function: Supported
</td></tr>
</table>

∗1: The maximum jitter amplitude is limited according to the jitter tolerance of PPG or ED modules. Refer to the jitter tolerance specification of PPG/ED modules.
∗2: Full Rate Mode: MU181020B PPG
∗3: Jittered Clock Output Frequency: Specified as 5 GHz, Modulation Frequency: 0.5 GHz, Sinusoidal Jitter

● MU181800B 14 GHz Clock Distributor

Frequency Range	0.1 GHz to 14 GHz 0.1 GHz to 14.1 GHz [MU181800B-005]
Clock Input	Level: 0.4 Vp-p to 2.0 Vp-p Waveform: Square wave (<0.5 GHz), Square wave or Sine wave (≥0.5 GHz) Connector: SMA(f.), Termination: 50Ω/GND
Clock Output	5ch Single-end Level: 0.4 Vp-p (Min.), 1.0 Vp-p (Max.) Duty: 50 ±10% (50% Clock Input Duty) Channel Skew: ≤10 ps (14 GHz) Connector: SMA(f.), Termination: 50Ω/GND

● MU181020B 14 Gbit/s PPG

	MU181020B-002 0.1 Gbit/s to 14 Gbit/s
Bit Rate	0.1 Gbit/s to 14 Gbit/s 0.1 Gbit/s to 14.1 Gbit/s [MU181020B-005]
External Clock Input	Frequency Range: 0.1 GHz to 14 GHz 0.1 GHz to 14.1 GHz [MU181020B-005] Level: 0.4 Vp-p (Min.), 1.5 Vp-p (Max.) (–4 to +7.5 dBm) Waveform: Square wave (<0.5 GHz), Square wave or Sine wave (≥0.5 GHz) Duty: 50% Connector: SMA(f.), Termination: 50Ω/AC Coupling
Generation Pattern	PRBS Steps: $2^n - 1$ (n = 7, 9, 10, 11, 15, 20, 23, 31) Mark Ratio: 1/2, 1/4, 1/8, 0/8; $\overline{1/2}$, 3/4, 7/8, 8/8 supported at reverse logic AND Bit Shift: 1 bit, 3 bits (Prohibited at 1/2, $\overline{1/2}$, 0/8, 8/8 mark ratio) Zero Substitution Pattern with continuous 0s appended to M-sequence signal + 1 bit Pattern: 2^n or $2^n - 1$ (n = 7, 9, 10, 11, 15, 20, 23) 0 continuous substitution count: 1 to (pattern length – 1) bits Other: 0 at next bit after 0 substitution changed to 1 Data Data Length: 2 to 134217728 bits/ch, Steps: 1 bit Alternate Data Length: 128 to 67108864 bits/ch (independent bits for A/B), Steps: 128 bits Loop Count: 511 times (A/B set independently) A/B Switching: Auto-switching by A/B loop times setting (Internal) Controlled by external signal (External) Editing: Pattern editing for A/B independently Mixed Pattern Pattern: PRBS, Data – 1 to Data – 511 Data+PRBS Length: 768 to 2^{31} + 134217728, Steps: 128 bits Data Length: 512 to 134217728 bits Sequence Pattern Block Count: 1 to 128 Block Length: 16384 to 1048576 bits, Steps: 128 bits Loop Count: 1 to 1024 times, Repeat Block Transition Conditions: A pattern match, B pattern match, Manual, Loop Time complete, External trigger (rising edge) Next Destination: Specified Block No. or Stop
Error Insertion	Error Event: Repeat, Single Error rate: #E–n (# = 1 to 9, n = 2 to 12) Timing: Internal/External
Auxiliary Input	ALTN Trigger/Sequence Trigger/Error Injection/Burst Enable (Switchable) Minimum Pulse Width: ≥64 bit width Level: H: 0 V, L: –1 V Connector: SMA(f.), Termination: 50Ω/GND
Auxiliary Output	1/n Clock (n = 2, 4, 8, 9, 10, 11……., 510, 511) Pattern Sync, Burst Trigger Level: H: 0 V, L: –1 V Connector: SMA(f.), Termination: 50Ω/GND
Gating Output	Burst Output Signal at Burst, Timing Signal at Repeat 1ch Output Level: H: 0 V, L: –1 V Connector: SMA(f.), Termination: 50Ω/GND
Variable Data Delay [MU181020B-030/130]	Independent Mode Phase Setting Range: –1 UI to +1 UI, Steps: 1 mUI, Unit: UI/ps CH Synchronization or Combination Mode Phase Setting Range: –64 UI to +64 UI, Steps: 1 mUI, Unit: UI/ps
Operation Temperatures	15° to 35°C

● MU181020B 14 Gbit/s PPG Amplitude Option

		No Option	MU181020B-011	MU181020B-012	MU181020B-013
Number of Output		2 (Data/$\overline{\text{Data}}$)			
Data Output	Amplitude	—	0.25 Vp-p to 2.5 Vp-p Steps: 2 mV Setting Accuracy: ±50 mV ±17%	0.05 Vp-p to 2.0 Vp-p Steps: 2 mV Setting Accuracy: ±50 mV ±17%	0.5 Vp-p to 3.5 Vp-p Steps: 2 mV Setting Accuracy: ±50 mV ±17%
	Offset	—	–2.0 Voh to +3.3 Voh Steps: 1 mV		
	Current Limiting	—	Sourcing 50 mA, Sinking 80 mA		
	Level	H: 0 V, L: –1.0 V	—	—	—
	Fixed Interface	—	NECL, SCFL, NCML, PCML, LVPECL (+3.3 V), LVDS		NECL, SCFL, NCML, PCML, LVPECL
	Crosspoint	50 ±15%	30 to 70%, Steps: 1%	20 to 80%, Steps: 1%	20 to 90%, Steps: 0.1%
	Tr/Tf	35 ps (typ.) (20 to 80%) (≥5 Gbit/s)	28 ps (typ.) (20 to 80%) (≥5 Gbit/s)	20 ps (typ.) (20 to 80%) (10, 12.5, 14 Gbit/s, Amplitude: 2 Vp-p)	25 ps (typ.) (20 to 80%) (10 Gbit/s, Amplitude: ≥1 Vp-p)
	Total Jitter	10 ps (typ.)	10 ps p-p (typ.)	8 ps p-p (typ.)	
	Distortion (0-peak)	—	±25 mV ±6% (typ.)		±25 mV ±10% (typ.)
	Connector	SMA(f.)	K(f.)		
	Termination	GND/50Ω	AC, DC DC: GND, –2 V, +1.3 V, +3.3 V, Open (LVDS)/50Ω		AC, DC DC: GND, –2 V, +1.3 V, +3.3 V/50Ω
	On/Off Function	Always On	Supported		

● MU181020B 14 Gbit/s PPG Clock Option

		No Option
Clock Output	Number of Output	1 (Clock)
	Amplitude	0.25 Vp-p (Min.), 0.9 Vp-p (Max.) (AC)
	Duty	50 ±15%
	Offset	—
	Current Limiting	—
	Fixed Interface	—
	Tr/Tf	30 ps (typ.) (20 to 80%)
	Total Jitter	1 ps (typ.) (RMS)
	Connector	SMA(f.)
	Termination	GND/50Ω
	On/Off Function	Always On

● MU181040B 14 Gbit/s ED

		MU181040B-002 0.1 Gbit/s to 14 Gbit/s	
Bit Rate		0.1 Gbit/s to 14 Gbit/s 0.1 Gbit/s to 14.1 Gbit/s [MU181040B-005]	
Reception Pattern		PRBS Steps: $2^n - 1$ (n = 7, 9, 10, 11, 15, 20, 23, 31) Mark Ratio: 1/2, 1/4, 1/8, 0/8; $\overline{1/2}$, 3/4, 7/8, 8/8 supported at reverse logic AND Bit Shift: 1 bit, 3 bits (Prohibited at 1/2, $\overline{1/2}$, 0/8, 8/8 mark ratio) Zero Substitution Pattern with continuous 0s appended to M-sequence signal +1 bit Pattern: 2^n or $2^n - 1$ (n = 7, 9, 10, 11, 15, 20, 23) 0 continuous substitution count: 1 to (pattern length – 1) bits Other: 0 at next bit after 0 substitution changed to 1 Data Data Length: 2 to 134217728 bits/ch, Steps: 1 bit Mixed Pattern Pattern: PRBS, Data – 1 to Data – 511 Data+PRBS Length: 768 to 2^{31} + 134217728, Steps: 128 bits Data Length: 512 to 134217728 bits Sequence Pattern Block Count: 1 to 128	
Detection Item		Total Error, Insertion Error, Omission Error, Transition Error, Non-Transition Error	
Display Item		Bit Error Rate, Bit Error Count, Input Signal Frequency	
Input Signal Synchronization		Auto Sync.: On/Off	
Error Analysis		Input Signal Capture (128 Mbits), Eye Margin, Eye Diagram, Q Measurement, Bathtub, ISI Analysis	
Burst Signal Measurement		Burst Trigger: Internal/External Input	
Option Number		No Option	MU181040B-020*
Clock Recovery	Frequency Range	—	0.1 GHz, 0.125 GHz to 0.2 GHz, 0.25 GHz to 0.4 GHz, 0.5 GHz to 0.8 GHz, 1 GHz to 1.6 GHz, 2 GHz to 3.2 GHz, 4.25 GHz, 4.9 GHz to 6.25 GHz, 9.8 GHz to 12.5 GHz
	Recovered Clock Output	—	POS/NEG reversible [without MU181040B-030] Amplitude: 0.55 ±0.15 Vp-p Connector: SMA(f.)
Clock Input		Frequency Range: 0.1 GHz to 14 GHz 0.1 GHz to 14.1 GHz [MU181040B-005] Clock Source Waveform: Internal/External [MU181040B-020] Waveform: Square wave (<0.5 GHz), Square wave or Sine wave (≥0.5 GHz) Duty 50% Number of Input: 1 Level: 0.25 Vp-p (Min.), 1.5 Vp-p (Max.) Connector: SMA(f.) Termination: GND/50Ω, Variable/50Ω, Differential/100Ω NECL, PCML (+3.3 V), LVPECL (+3.3 V), GND Variable: –2.5 V to +3.5 V, Steps: 10 mV	
Data Input		Number of Input: 2 (Data, $\overline{\text{Data}}$) Signal Format: NRZ Amplitude: 0.1 Vp-p (Min.), 2.0 Vp-p (Max.) Threshold: –3.5 V to +3.3 V, Steps: 1 mV Input Sensitivity: 20 mVp-p (typ.) (14 Gbit/s PRBS $2^{31} - 1$) Phase Margin: 50 ps p-p (typ.) (14 Gbit/s PRBS $2^{31} - 1$) Connector: K(f.) Termination: GND/50Ω, Variable/50Ω, Differential/100Ω NECL, PCML (+3.3 V), LVPECL (+3.3 V), GND Variable: –2.5 V to +3.5 V, Steps: 10 mV	
Auxiliary Input		Sequence Trigger/Capture Trigger/Burst Enable (switchable) Minimum Pulse Width: ≥64 bit width Level: H: 0 V, L: –1 V Connector: SMA(f.), Termination: 50Ω/GND	
Auxiliary Output		1/N Clock (N = 8 to 511), Steps: 1 Pattern Sync, Error, Sync Gain Level: H: 0 V, L: –1 V	
Data Monitor Output		Number of Output: 2 (Data, $\overline{\text{Data}}$) Insertion Loss: –6 dB +1/–2.5 dB Connector: SMA(f.), Termination: 50Ω/AC Coupling	
Variable Clock Delay [MU181040B-030/130]		Phase Setting Range: –1 UI to +1 UI, Steps: 1 mUI, Unit: UI/ps	
Operation Temperatures		15° to 35°C	

*: The MU181040B-030/130 Variable Clock Phase option is required when using the MU181040B-020/120 Clock Recovery option.

● MU183020A 28G/32G bit/s PPG, MU183021A 28G/32G bit/s 4ch PPG

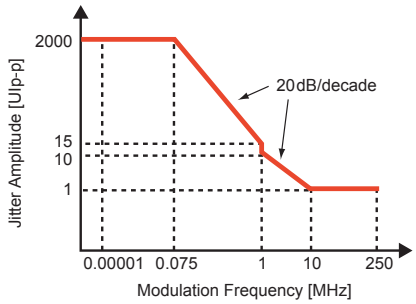
<table>
<tr><td>Bit Rate</td><td>Operational Bit-rate Range: 2.4 Gbit/s to 28.1 Gbit/s
2.4 Gbit/s to 32.1 Gbit/s (with Option-x01)</td></tr>
<tr><td>Bit-rate Setting Range
(MU181000B synchronized operation)</td><td>This item is specified when MU181000B is installed into the same main frame.
When Full Rate Clock Output is selected:
2.400 000 Gbit/s to 12.500 000 Gbit/s, 0.000 001 Gbit/s step
12.500 002 Gbit/s to 25.000 000 Gbit/s, 0.000 002 Gbit/s step
25.000 004 Gbit/s to 28.100 000 Gbit/s, 0.000 004 Gbit/s step
25.000 004 Gbit/s to 32.100 000 Gbit/s, 0.000 004 Gbit/s step (with Option-x01)
Offset: –1000 ppm to +1000 ppm, 1 ppm step
(Offset setting range is changed depends on Bit-rate.
Offset range is–1000 ppm to 0 ppm with following Bit-rate range.
Full Rate: 12.500 000 Gbit/s, 25.000 000 Gbit/s, Half Rate: 25.000 000 Gbit/s)
When Half Rate Clock Output is selected:
2.400 000 Gbit/s to 25.000 000 Gbit/s, 0.000 002 Gbit/s step
25.000 004 Gbit/s to 28.100 000 Gbit/s, 0.000 004 Gbit/s step
25.000 004 Gbit/s to 32.100 000 Gbit/s, 0.000 004 Gbit/s step (with Option-x01)
Offset: –1000 ppm to +1000 ppm, 1 ppm step
(Offset setting range is changed depends on Bit-rate.
Offset range is –1000 ppm to 0 ppm with following Bit-rate range.
Full Rate: 12.500 000 Gbit/s, 25.000 000 Gbit/s, Half Rate: 25.000 000 Gbit/s)</td></tr>
<tr><td>Bit-rate Setting Range
(MU181000B and MU181500B synchronized operation)</td><td>This item is specified when MU181500B are installed to the same main frame.
When Full Rate Clock Output is selected:
2.400 000 Gbit/s to 3.125 000 Gbit/s, 0.000 001 Gbit/s step
3.200 001 Gbit/s to 6.250 000 Gbit/s, 0.000 001 Gbit/s step
6.400 001 Gbit/s to 12.500 000 Gbit/s, 0.000 001 Gbit/s step
12.800 002 Gbit/s to 25.000 000 Gbit/s, 0.000 002 Gbit/s step
25.600 004 Gbit/s to 28.100 000 Gbit/s, 0.000 004 Gbit/s step
25.600 004 Gbit/s to 32.100 000 Gbit/s, 0.000 004 Gbit/s step (with Option-x01)
Offset: –1000 ppm to +1000 ppm, 1 ppm step
(Offset setting range is changed depends on Bit-rate.
Offset range is –1000 ppm to 0 ppm with following Bit-rate range.
Full Rate: 12.500 000 Gbit/s, 25.000 000 Gbit/s, Half Rate: 25.000 000 Gbit/s)
When Half Rate Clock Output is selected:
2.400 000 Gbit/s to 3.125 000 Gbit/s, 0.000 002 Gbit/s step
3.200 002 Gbit/s to 6.250 000 Gbit/s, 0.000 002 Gbit/s step
6.400 002 Gbit/s to 12.500 000 Gbit/s, 0.000 002 Gbit/s step
12.800 002 Gbit/s to 25.000 000 Gbit/s, 0.000 002 Gbit/s step
25.600 004 Gbit/s to 28.100 000 Gbit/s, 0.000 004 Gbit/s step
25.600 004 Gbit/s to 32.100 000 Gbit/s, 0.000 004 Gbit/s step (with Option-x01)
Offset: –1000 ppm to +1000 ppm, 1 ppm step
(Offset setting range is changed depends on Bit-rate.
Offset range is –1000 ppm to 0 ppm with following Bit-rate range.
Full Rate: 12.500 000 Gbit/s, 25.000 000 Gbit/s, Half Rate: 25.000 000 Gbit/s)</td></tr>
<tr><td>Bit-rate Setting Range
(with external clock source)</td><td>This item is specified when external clock source is used.
When Full Rate Clock Output is selected:
<table>
<tr><th>Operating Bit-rate Range</th><th>Input Clock Frequency</th><th>Bit-rate/Clock Divide Ratio</th></tr>
<tr><td>2.4 Gbit/s to 16.0 Gbit/s</td><td>2.4 GHz to 16.0 GHz</td><td>1/1 Clock</td></tr>
<tr><td>16.0 Gbit/s to 20.4 Gbit/s</td><td>8.0 GHz to 10.2 GHz</td><td>1/2 Clock</td></tr>
<tr><td>20.0 Gbit/s to 28.1 Gbit/s*1</td><td>10.0 GHz to 14.05 GHz</td><td>1/2 Clock</td></tr>
<tr><td>20.0 Gbit/s to 32.1 Gbit/s*2</td><td>10.0 GHz to 16.05 GHz</td><td>1/2 Clock</td></tr>
<tr><td>25.0 Gbit/s to 28.1 Gbit/s*1</td><td>6.25 GHz to 7.025 GHz</td><td>1/4 Clock</td></tr>
<tr><td>25.0 Gbit/s to 32.1 Gbit/s*2</td><td>6.25 GHz to 8.025 GHz</td><td>1/4 Clock</td></tr>
</table>
When Half Rate Clock Output is selected:
<table>
<tr><th>Operating Bit-rate Range</th><th>Input Clock Frequency</th><th>Bit-rate/Clock Divide Ratio</th></tr>
<tr><td>2.4 Gbit/s to 28.1 Gbit/s*1</td><td>1.2 GHz to 14.05 GHz</td><td>1/2 Clock</td></tr>
<tr><td>2.4 Gbit/s to 32.1 Gbit/s*2</td><td>1.2 GHz to 16.05 GHz</td><td>1/2 Clock</td></tr>
<tr><td>25.0 Gbit/s to 28.1 Gbit/s*1</td><td>6.25 GHz to 7.025 GHz</td><td>1/4 Clock</td></tr>
<tr><td>25.0 Gbit/s to 32.1 Gbit/s*2</td><td>6.25 GHz to 8.025 GHz</td><td>1/4 Clock</td></tr>
</table>
∗1: Up to 28.1 Gbit/s when Option-x01 is not installed.
∗2: Option-x01 must be installed.</td></tr>
<tr><td>Bit-rate Setting Range
(MU181500B synchronized operation with external clock source)</td><td>This item is specified when MU181000B is installed into the same mainframe and external clock source is used.
When Full Rate Clock Output is selected:
<table>
<tr><th>Operating Bit-rate Range</th><th>Input Clock Frequency</th><th>Bit-rate/Clock Divide Ratio</th></tr>
<tr><td>2.4 Gbit/s to 15.0 Gbit/s</td><td>2.4 GHz to 15.0 GHz</td><td>1/1 Clock</td></tr>
<tr><td>15.0 Gbit/s to 20.0 Gbit/s</td><td>7.5 GHz to 10.0 GHz</td><td>1/2 Clock</td></tr>
<tr><td>20.0 Gbit/s to 28.1 Gbit/s*1</td><td>10.0 GHz to 14.05 GHz</td><td>1/2 Clock</td></tr>
<tr><td>20.0 Gbit/s to 30.0 Gbit/s*2</td><td>10.0 GHz to 16.05 GHz</td><td>1/2 Clock</td></tr>
<tr><td>30.0 Gbit/s to 32.1 Gbit/s*2</td><td>7.5 GHz to 8.025 GHz</td><td>1/4 Clock</td></tr>
</table>
When Half Rate Clock Output is selected:
<table>
<tr><th>Operating Bit-rate Range</th><th>Input Clock Frequency</th><th>Bit-rate/Clock Divide Ratio</th></tr>
<tr><td>2.4 Gbit/s to 28.1 Gbit/s*1</td><td>1.2 GHz to 14.05 GHz</td><td>1/2 Clock</td></tr>
<tr><td>2.4 Gbit/s to 30.0 Gbit/s*2</td><td>1.2 GHz to 15.0 GHz</td><td>1/2 Clock</td></tr>
<tr><td>30.0 Gbit/s to 32.1 Gbit/s*2</td><td>7.5 GHz to 8.025 GHz</td><td>1/4 Clock</td></tr>
</table>
∗1: Up to 28.1 Gbit/s when Option-x01 is not installed.
∗2: Option-x01 must be installed.</td></tr>
</table>

External Clock Input	Number of Input: 1 (Single end) Frequency: 1.2 GHz to 16.05 GHz* Amplitude: 0.3 Vp-p to 1.0 Vp-p (–6.5 to +4.0 dBm) Termination: 50Ω/AC Coupling Connector: SMA (f.)
Aux Input	Number of Input: 1 (Single end) Signal Type: Error Injection, Burst Minimum Pulse Width: 1/128 Input level: 0/–1 V (H: –0.25 V to 0.05 V, L: –1.1 V to –0.8 V) Termination: 50Ω/GND Connector: SMA (f.)
Aux Output	Number of Output: 2 (Differential) Signal Type: 1/n Clock (n = 4, 6, 8, 10 · · · 510, 512), Pattern Sync, Burst Out2 Output level: 0/–0.6 V (H: –0.25 V to 0.05 V, L: –0.80 V to –0.45 V) Termination: 50Ω/GND Connector: SMA (f.)
Gating Output	Burst, Repeat Timing Signal Output level: 0/–1 V (H: –0.25 V to 0.05 V, L: –1.25 V to –0.8 V) Termination: 50Ω/GND Connector: SMA (f.)
Pattern Generation	PRBS Pattern length: 2^n – 1 (n = 7, 9, 10, 11, 15, 20, 23, 31) Mark ratio: 1/2 (1/2INV is supported by a logic inversion) Zero-Substitution: Pattern with continuous 0 s appended to M-sequence signal + 1 bit Pattern: 2^n or 2^n – 1 (n = 7, 9, 10, 11, 15, 20, 23) 0 continuous substitution count: 1 to (pattern length – 1) bits 0 at next bit after 0 substitution changed to 1 Data Data length: 2 bits to 268 435 456 bits, 1 bit step Mixed Pattern Pattern: PRBS, Data – 1 to Data – 511 Mixed Row Length (Data + PRBS Length): 1 536 to 2 415 919 104, 256 bits step Data length: 1 024 bits to 268 435 456 bits, 1 bit step PRBS length/Mark Ratio: Same as PRBS PRBS Sequence: Restart, Consecutive
Pattern Sequence	Repeat: Continuous Pattern Burst Burst Cycle: 25 600 bits to 2 147 483 648 bits, 256 bits step Enable period Internal: 12 800 bits to 2 147 483 392 bits, 256 bits step Ext Trigger, Enable: 12 800 bits to 2 147 483 648 bits, 256 bits step
Pre-code	Pre-code function: ON and OFF Type: DQPSK (MU183020A, MU183021A) DP-QPSK (MU183021A) Initial Data: 0 or 1 selectable
Error Addition	Timing: Internal, external trigger Error event: Repeat, Single Error rate: a × 10^{-b} (a = 1 to 9, b = 3 to 12), Upper limit: 5E-3

∗: The clock frequency from external clock source shall be changed depends on the Bit-rate setting. Please see Bit-rate setting range.

<table>
<tr><td>Data Output*1</td><td>
<table>
<tr><th></th><th>MU183020A-x12</th><th>MU183020A-x13</th><th>MU183021A-x22</th><th>MU183021A-x23</th></tr>
<tr><td>Number of Outputs</td><td colspan="2">2: Data, XData (Independent)</td><td colspan="2">4: Data1, XData1, Data2, XData2 (Independent)</td></tr>
<tr><td>Output Amplitude</td><td>0.5 Vp-p to 2.0 Vp-p
2 mV step</td><td>0.5 Vp-p to 3.5 Vp-p
2 mV step</td><td>0.5 Vp-p to 2.0 Vp-p
2 mV step</td><td>0.5 Vp-p to 3.5 Vp-p
2 mV step</td></tr>
</table>
<table>
<tr><th></th><th>MU183021A-x12</th><th>MU183021A-x13</th></tr>
<tr><td>Number of Outputs</td><td colspan="2">8: Data, XData (Independent)</td></tr>
<tr><td>Output Amplitude</td><td>0.5 Vp-p to 2.0 Vp-p
2 mV step</td><td>0.5 Vp-p to 3.5 Vp-p
2 mV step</td></tr>
</table>
Output amplitude setting error: ±50 mV ±17% of setting amplitude*2
Offset: –2.0 Voh to +3.3 Voh, 1 mV step
Current limitation: Sourcing 50 mA, Sinking 80 mA
Cross point setting range:
20 to 80%/0.1% step: at 1.0 Vp-p to upper limit of output amplitude setting
30 to 70%/0.1% step: at 0.5 Vp-p to 0.998 Vp-p
Tr/Tf 12 ps (20 to 80%)*3, *4, *5
Jitter (p-p): 8 ps p-p*3, *4, *5, *6, *10
Jitter (RMS): 700 fs*3, *4, *5, *6
Waveform Distortion (0-peak): ±25 mV ±15%*3, *4, *5, *11
Output: On/Off selectable
Inter channel skew: ±0.25 UI*6, *7, *8
Termination: AC/DC 50Ω
Connector: K (f.)
</td></tr>
<tr><td>Clock Output*9</td><td>
Number of output: 1
Full Rate : Clock frequency is same as bit-rate when Full Rate Clock Output is selected.
2.4 GHz to 28.1 GHz
2.4 GHz to 32.1 GHz (Option-x01)
Half Rate: Clock frequency is half of bit-rate when Half Rate Clock Output is selected.
1.2 GHz to 14.05 GHz
1.2 GHz to 16.05 GHz (Option-x01)
Ampligude: 0.3 Vp-p to 1.0 Vp-p
Output: On/Off selectable
Termination: 50Ω/AC Coupling
Connector: K (f.)
</td></tr>
<tr><td>Delay
(MU183020A-x30, x31
MU183021A-x30)</td><td>
Phase variable range: –1 000 mUI to +1 000 mUI, 2 mUI step
Phase setting error: ±50 mUIp-p*5, *6 (Bit rate ≤28.1 Gbit/s), ±75 mUIp-p*5, *6 (Bit rate >28.1 Gbit/s)
</td></tr>
</table>

∗1: Unless otherwise specified , these are defined with PRBS 2^{31} – 1, Mark Ratio 1/2, Cross-point 50%, using an optional accessories (J1439A coaxial cable, 0.8 m, K connector) and a sampling oscilloscope which has 70 GHz bandwidth.
∗2: This value is assured when Cross point is set to 50% or within the range of 30 to 80% and Bit rate is set to 25 or 28.1 Gbit/s.
∗3: Without Option-x01: at 28.1 Gbit/s
With Option-x01: at 32.1 Gbit/s
∗4: With Option-x12 or x22: at amplitude 2.0 Vp-p,
With Option-x13 or x23: at amplitude 3.5 Vp-p
∗5: Typical value
∗6: Using oscilloscope with intrinsic jitter of less than 200 fs (RMS).
∗7: With MU183020A-x22 or MU183020A-x23. Or, when MU183021A is used.
∗8: With Option-x30 or x31.
∗9: These values are monitored using an applicable part (J1439A coaxial cable, 0.8 m, K connector) at a sampling oscilloscope bandwidth of 70 GHz.
∗10: This value is the peak-to-peak jitter of the crossing point on Eye pattern measured at 1k Jitter total samples and 30 counts, and is not the estimated TJ at BER 1E-12 using DR/RJ decomposition.
∗11: Sometimes, performance may exceed the standards for undescribed settings, such as burst lengths of >1 µs (reference value), and contiguous patterns of 0 s (or 1 s).

Jitter Tolerance*7	Bit-rate: 16 Gbit/s, 28.1 Gbit/s*1 16 Gbit/s, 28.1 Gbit/s, 32.1 Gbit/s*2 Test Pattern: PRBS $2^{31} - 1$ 
Multi-Channel Operation	MU183020A Combination*1, *2: 2ch (Bit shifted test pattern as 56 Gbit/s, 64 Gbit/s band signal source) CH Sync.: 2 to 4ch*3, *6 Phase variable range*5: –64 000 mUI to +64 000 mUI, Steps: 2 mUI MU183021A Combination*2: 2ch (Bit shifted test pattern as 56G/64 Gbit/s band signal source) 4ch (Bit shifted test pattern as 112G/128 Gbit/s band signal source) CH Sync.: 2 to 8ch*3, *4 Phase variable range*5: –64 000 mUI to +64 000 mUI, Steps: 2 mUI
Operating Temperature	15° to 35°C

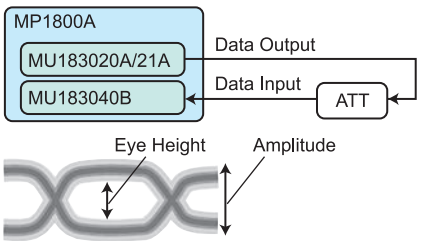
∗1: Option-x31 is required for target channels.
∗2: Combination extending over multiple slots cannot be set.
∗3: When target channels are installed successively from Slot 1.
∗4: Option-x30 is required for target channels.
∗5: A separate value can be set for each channel. This value is common to both Channel Combination and Channel Synchronization.
∗6: Option-x30 or x31 is required for target channels.
∗7: Combined operation with MU181500B and MU181000B. SJ applied. Looped back with MU183040B.

● MU183040B 28G/32G bit/s High Sensitivity ED, MU183041B 28G/32G bit/s 4ch High Sensitivity ED

<table>
<tr><td colspan="2">Bit-rate</td><td>Operational Bit-rate Range: 2.4 Gbit/s to 28.1 Gbit/s
2.4 Gbit/s to 32.1 Gbit/s (with Option-x01)</td></tr>
<tr><td colspan="2">Data Input</td><td>Number of Input
MU183040B-010 · · · 2 (Data , XData)
MU183040B-020 · · · 4 (Data1 to Data2, XData1 to XData2)
MU183041B · · · 8 (Data1 to Data4, XData1 to XData4)
Amplifier:
Single-ended 50Ω, Differential 50Ω, Differential 100Ω can be set.
Data, XData can be set.
Tracking, Independent, Alternate can be set.
(Data-XData or XData-Data can be set when Alternate is selected.*1)
Format: NRZ
<table><tr><th colspan="2"></th><th>MU183040B/MU183041B</th></tr><tr><td colspan="2">Input Amplitude*8</td><td>0.05 Vp-p to 1.0 Vp-p</td></tr><tr><td rowspan="2">Sensitivity*8</td><td>Eye Amplitude</td><td>15 mVp-p*2, *3, *4
≤25 mVp-p*4</td></tr><tr><td>Eye Height</td><td>10 mV*2, *3, *4, *9</td></tr></table>Note: Be careful about the maximum input amplitude. 2 Vp-p Max. for A-type, and 1 Vp-p Max. for B-type.
Threshold voltage:
–3.5 V to +3.3 V, 1 mV step (Can be set individually for Data and XData.)
Absolute value of difference between Data and XData Threshold values shall be 3 V or less.
Phase Margin: 20 ps*2, *4, *5, *7
28 ps*4, *5, *6, *7
Termination: GND/50Ω, Variable/50Ω
Termination voltage: –2.5 V to +3.5 V, 10 mV step (When termination variable is selected)
Connector: K (f.)</td></tr>
<tr><td colspan="2">Clock Input</td><td>Number of Input: 1 (Single-end)
Frequency: 1.2 GHz to 16.05 GHz
Amplitude: 0.3 Vp-p to 1.0 Vp-p (–6.5 to +4.0 dBm)
Termination: 50Ω/AC Coupling
Connector: SMA (f.)</td></tr>
<tr><td colspan="2">Clock Recovery</td><td>Clock Recovery from 1ch Data input, internal distribution to each channel*10</td></tr>
<tr><td></td><td>Operating Bit-rate</td><td>2.4 Gbit/s to 28.1 Gbit/s, 1 kbit/s step (Option-x22)
25.5 Gbit/s to 32.1 Gbit/s*11, 1 kbit/s step (Option-x23)</td></tr>
<tr><td></td><td>Maximum Number of Consecutive Zeros*12</td><td>72 bit (Zero Substitution 2^{15})</td></tr>
<tr><td></td><td>Lock Range for Clock Data Recovery*12</td><td>±200 ppm (Option-x22)
±100 ppm (Option-x23)</td></tr>
<tr><td></td><td>Target Loop Band</td><td>Available options are Bit rate/1667, Bit rate/2578, Jitter Tolerance*13 and Variable (Option-x22)
If the Variable option is selected, the following settings are available:
<table><tr><th>Bit rate [Gbit/s]</th><th>Setting Range [MHz]/Step [MHz]</th></tr><tr><td>2.400 000 to 5.500 000</td><td>3/–</td></tr><tr><td>5.500 001 to 7.500 000</td><td>3 to 4/1</td></tr><tr><td>7.500 001 to 9.500 000</td><td>3 to 5/1</td></tr><tr><td>9.500 001 to 10.500 000</td><td>3 to 6/1</td></tr><tr><td>10.500 001 to 12.500 000</td><td>3 to 7/1</td></tr><tr><td>12.500 001 to 14.500 000</td><td>3 to 8/1</td></tr><tr><td>14.500 001 to 15.500 000</td><td>3 to 9/1</td></tr><tr><td>15.500 001 to 17.500 000</td><td>3 to 10/1</td></tr><tr><td>17.500 001 to 19.500 000</td><td>3 to 11/1</td></tr><tr><td>19.500 001 to 20.500 000</td><td>3 to 12/1</td></tr><tr><td>20.500 001 to 22.500 000</td><td>3 to 13/1</td></tr><tr><td>22.500 001 to 24.500 000</td><td>3 to 14/1</td></tr><tr><td>24.500 001 to 25.500 000</td><td>3 to 15/1</td></tr><tr><td>25.500 001 to 27.500 000</td><td>3 to 16/1</td></tr><tr><td>27.500 001 to 28.100 000</td><td>3 to 17/1</td></tr></table>Available options are Bit rate/1667, Bit rate/2578 and Jitter Tolerance*13 (Option-x23)</td></tr>
<tr><td></td><td>Jitter Tolerance</td><td>Comply 16G FC, 32G FC, 100 GbE (25.78x4), InfiniBand FDR, Jitter Tolerance Mask (Option-x22)
Comply 32G FC, 100 GbE (25.78x4), Jitter Tolerance Mask (Option-x23)</td></tr>
<tr><td colspan="2">Aux Input</td><td>Number of Input: 1 (Single-end)
Input Signal: External Mask, Burst
Minimum Pulse Width: 1/128 of Bit-rate
Input Level: 0/–1 V (H: –0.25 V to 0.05 V, L: –1.1 V to –0.8 V)
Termination: GND/50Ω
Connector: SMA (f.)</td></tr>
</table>

Aux Output	Number of Output: 2 (Differential) Input Signal: 1/n Clock (n = 4, 6, 8, 10 · · · 510, 512), Pattern Sync, Error, Sync. gain Pattern Sync. PRBS, PRGM: Position: (Least common multiple of 1 to Pattern Length and 128) − 135, 8 step Mixed Data: Block No. setting: 1 to the Block No. specified for Mixed Data, in single steps Row No. setting: 1 to the Row No. specified for Mixed Data, in single steps Output Level: 0/–0.6 V (H: –0.25 V to 0.05 V, L: –0.80 V to –0.45 V) Termination: GND/50Ω Connector: SMA (f.)
Pattern Detection	PRBS Pattern length: 2^n – 1 (n = 7, 9, 10, 11, 15, 20, 23, 31) Mark ratio: 1/2 (1/2INV is supported by a logic inversion) Zero-Substitution: Pattern with continuous 0 s appended to M-sequence signal + 1 bit Pattern: 2^n or 2^n – 1 (n = 7, 9, 10, 11, 15, 20, 23) 0 continuous substitution count: 1 to (pattern length – 1) bits 0 at next bit after 0 substitution changed to 1 Data Data length: 2 bits to 268 435 456 bits, 1 bit step Mixed Pattern Pattern: PRBS, Data – 1 to Data – 511 Mixed Row Length (Data + PRBS Length): 1 536 to 2 415 919 104, 256 bits step Data length: 1 024 bits to 268 435 456 bits, 1 bit step PRBS length/Mark Ratio: Same as PRBS PRBS Sequence: Restart, Consecutive
Pattern Sequence	Repeat: Continuous Pattern Burst Burst Cycle: 25 600 bits to 2 147 483 648 bits, 256 bits step Enable period Internal: 12 800 bits to 2 147 483 392 bits, 256 bits step Ext Trigger, Enable: 12 800 bits to 2 147 483 648 bits, 256 bits step
Measurement Type	Error Rate, Error Count, Error Interval, Error Free Interval (%), Frequency Clock Count, Sync Loss Interval, Clock Loss Interval
Error Detection Mode	Total error, Insertion Error, Omission Error, Transition Error, Non Transition Error
Error Analysis	Eye Margin, Eye Diagram, Bathtub Jitter, Auto Adjust, Auto Search, Capture, Eye Contour, PAM BER Measurement
Burst Measurement Signal	Burst Trigger: Internal, External
Variable Clock Delay	Phase variable range: –1 000 mUI to +1 000 mUI, 2 mUI step Phase setting error: ±50 mUIp-p*1, *4 mUI - ps selectable
Multi-channel Operation	MU183040B (with Option-x20): 2ch combination (Combination extending over multiple slots cannot be set) MU183041B (4ch): 2ch or 4ch combination (Combination extending over multiple slots cannot be set)
Operating Temperature	15° to 35°C

∗1: Absolute value of difference between Data and XData Threshold values shall be 1.5 V or less.
∗2: 28.1 Gbit/s
∗3: PRBS31, Single-ended, Mark Ratio 1/2, 20° to 30°C
∗4: Typical value
∗5: 0.5 Vp-p Input
∗6: 25 Gbit/s
∗7: PRBS31, Single-ended, Mark ratio 1/2
∗8: Input amplitude is a range where Auto Adjust function operates. Input sensitivity is the minimum input amplitude which becomes error-free.
∗9: Sensitivity of eye height. Eye Height is the internal amplitude of Eye when the output amplitude of the MU183020A/21A + ATT is set to 15 mV with the measurement system as the figure below (A sampling oscilloscope with the bandwidth of 70 GHz or more is used.).
The number of samples with Sampling Oscilloscope is equivalent to BER 1E–9 or less at this internal amplitude.



∗10: MU183041B-023 recovers Clock from 1ch Data input and distributes to 1ch and 2ch. Also recovers Clock from 3ch Data input and distributes to 3ch and 4ch.
∗11: MU183040B/41B-001 must be installed.
∗12: When the MU183040B/MU183041B-x22 option is installed: The target loop band is specified by the maximum setting value of each bit rate.
When the MU183040B/MU183041B-x23 option is installed: The target loop band is specified by (Bit rate/1667) and (Bit rate/2578).
∗13: The Jitter Tolerance option makes the loop band wider than the other options and enables the Jitter Tolerance measurement.

● MZ1834A 4PAM Converter

Data Output	Number of Outputs: 2 (Data, xData) Modulation Format: PAM4 Output Amplitude*1: 0.238 Vp-p to 0.475 Vp-p (nom.) (with using MU183020A-022 or MU183021A-012) 0.238 Vp-p to 0.832 Vp-p (nom.) (with using MU183020A-023 or MU183021A-013) Tr/Tf: 12 ps (typ.) (20 to 80%, with using MU18302xA) Connector: K (f.)
Data Input	Number of Inputs: 4 (Data1, xData1, Data2, xData2) Input Amplitude: 0.5 Vp-p to 3.5 Vp-p Connector: K (m.)
Insertion Loss	–16 dB (nom.)*2
General	Temperature: +15° to +35°C (Operating), –20° to +60°C (Storage) Dimensions and Mass: 92.2 (W) × 20.4 (H) × 121.7 (D) mm*3, ≤2 kg

∗1: 0 to 3 Level
∗2: Data_n input to Data output
∗3: Excluding protrusions

● MZ1834B 4PAM Converter

Data Output	Number of Outputs: 2 (Data, xData) Modulation Format: PAM4 Output Amplitude*1: 0.376 Vp-p to 0.753 Vp-p (nom.) (with using MU183020A-022 or MU183021A-012) 0.756 Vp-p to 1.318 Vp-p (nom.) (with using MU183020A-023 or MU183021A-013) Tr/Tf: 12 ps (typ.) (20 to 80%, with using MU18302xA) Connector: K (f.)
Data Input	Number of Inputs: 4 (Data1, xData1, Data2, xData2) Input Amplitude: 0.5 Vp-p to 3.5 Vp-p Connector: K (m.)
Insertion Loss	–12 dB (nom.)*2
General	Temperature: +15° to +35°C (Operating), –20° to +60°C (Storage) Dimensions and Mass: 92.2 (W) × 20.4 (H) × 121.7 (D) mm*3, ≤2 kg

∗1: 0 to 3 Level
∗2: Data_n input to Data output
∗3: Excluding protrusions

● MZ1838A 8PAM Converter

Data Output	Number of Outputs: 2 (Data, xData) Modulation Format: PAM8 Output Amplitude*2: 0.139 Vp-p to 0.441 Vp-p (nom.) (with using MU183021A-012) 0.139 Vp-p to 0.772 Vp-p (nom.) (with using MU183021A-013) Tr/Tf: 12 ps (typ.) (20 to 80%, with using MU18302xA) Connector: K (f.)
Data Input	Number of Inputs: 6 (Data1, xData1, Data2, xData2, Data3, xData3) Input Amplitude: 0.5 Vp-p to 3.5 Vp-p Connector: K (m.)
Insertion Loss	Data1: –16 dB, Data2: –24 dB, Data3: –28 dB (nom.)*2
General	Temperature: +15° to +35°C (Operating), –20° to +60°C (Storage) Dimensions and Mass: 96.8 (W) × 40 (H) × 181.2 (D) mm*3, ≤3 kg

∗1: 0 to 7 Level
∗2: Data_n input to Data output
∗3: Excluding protrusions

● MZ1854A Data Signal Combiner

Data Output	Number of Output: 2 (Data, XData) Output Amplitude*1: 0.238 Vp-p to 0.594 Vp-p (with using MP1861A-011) 0.238 Vp-p to 0.832 Vp-p (with usingMP1861A-013) Connector: V (f)
Data Input	Number of Input: 4 (Data1, XData1, Data2, XData2) Input Amplitude: 0.5 Vp-p to 3.5 Vp-p Connector: V (m)
Insertion Loss	–16 dBm (nom.)*2
General	Temperature Operation: +15° to +35°C Storage: –20° to +60°C Dimensions and Mass: 60.2 (W) × 104.7 (H) × 23.5 (D) mm (Excluding protrusions), ≤2 kg

∗1: Level 0 to 3
∗2: Data_n input to Data output

● J1621A Passive Equalizer 3 dB, J1622A Passive Equalizer 6 dB

Frequency Range	DC to 14.0 GHz (25 Gbit/s to 28 Gbit/s)
Slope	3.0 ±0.5 dB (J1621A) 6.0 ±0.5 dB (J1622A)
Insertion Loss	At 14 GHz ≤1.2 dB (J1621A) ≤1.4 dB (J1622A)
Return Loss	12 dB (min.)
General	Connectors: SMA Impedance: 50Ω (nom.) Dimensions: 44 (W) × 12 (H) × 11(D) mm

● J1646A Passive Equalizer 6 dB (V connector)

Frequency Range	DC to 28 GHz (56 Gbit/s band)
Slope	6.0 dB ±1.0 dB
Insertion Loss	At 28 GHz ≤2.8 dB
Return Loss	11 dB (min.)
General	Connector: V Impedance: 50Ω Dimensions: 44 (W) × 12 (H) × 11 (D) mm

● G0361A 64Gbaud 2-bit DAC with MUX

Operating baud-rate	DC to 64Gbaud
Data Output	Number of Outputs: 2 (Data, xData) Output Amplitude: 0.7 Vp-p (typ. Single-end), 1.4 Vp-p (typ. Differential) Connector: V (f.)
Data Input	Number of Inputs: 4 (D0A, D0B, D1A, D1B) Input Amplitude: 0.5 Vp-p (typ.) Connector: K (f.)
Clock Input	Number of Inputs: 1 Input Amplitude: 0.5 Vp-p (typ.) Connector: K (f.)
Power Supply	VEE: –3.7 V, 2.1 W (typ.) Vamp1, 2: –3.4 V (typ.) for Amplitude Control CLKref: Clock Reference Voltage, Dref: Data Input Reference Voltage

● G0373A USB3.1 Receiver Test Adapter

Bit Rate	5G (USB3.1G1), 10G (USB3.1G2)
Data Output	LFPS Rx Amplitude: –1 V to +0.5 V LFPS Tx Amplitude: 3 Vp-p (typ., Differential)
Data Input	Rx Amplitude: 0.8 V to 1.2 V AUX Amplitude: –1 V to +0.5 V Gating Amplitude: –1.25 V to +0.8 V External Frequency: 4 GHz Connector: SMA (f.)
Power Supply	100 V(ac) to 120 V(ac)/200 V(ac) to 240 V(ac) [auto-switching between 100 V(ac)/200 V(ac)], 50 Hz to 60 Hz

● G0374A 64Gbaud PAM4 DAC

Baud Rate	DC to 64Gbaud
Data Output	Number of Outputs: 2 (Data, xData) Output Amplitude: 0.7 Vp-p (typ. Single-end), 1.4 Vp-p (typ. Differential) Connector: V (f.)
Data Input	Number of Inputs: 4 (D0A, D0B, D1A, D1B) Input Amplitude: 1 Vp-p (typ.) Connector: K (f.)
Clock Input	Number of Inputs: 1 Input Amplitude: 0.5 Vp-p (typ.) Connector: K (f.)
Power Supply	100 V(ac) to 120 V(ac)/200 V(ac) to 240 V(ac) [auto-switching between 100 V(ac)/200 V(ac)], 50 Hz to 60 Hz

● G0375A 32Gbaud Power PAM4 Converter

Number of Outputs	2 (Data, xData)
Baud Rate	10 to 32.1 Gbaud
Output Amplitude	2.2 Vp-p (Single-end, maximum) 4.4 Vp-p (Differential, maximum)
Amplitude Gain Control	–6 to 0 dB
RJ (rms)	200 fs (typ.)
Tr/Tf (20 - 80%)	12 ps (typ.)
Number of Inputs	4 (Data1, xData1, Data2, xData2) Uses J1735A at PAM4 Linearity control
In/Out Connector	K (f.)

● G0376A 32 Gbaud PAM4 Decoder with CTLE

Number of Data inputs	5 (CTLE Input (diff.), Decoder Input (diff.), Clock Input)
Number of Data outputs	5 (CTLE Output (diff.), Decoder Data Output1, 2, Monitor Output)
PAM4 Decoder Baud-rate	10 to 32.1 Gbaud (DFF On) 10 to 28 Gbaud (DFF Off)
Input Amplitude	0.4 V (CTLE input, max.) 0.5 V (Decoder input, max.)
Decoder Input Sensitivity	40 mV (typ.) Eye Height, Single-end
Decoder Output Amplitude	0.3 Vp-p (typ.)
CTLE gain	–12 to 0 dB, adjustable
CTLE peak Frequency	14 GHz
In/Out Connector	K (f.)

Ordering Information

Please specify the model/order number, name and quantity when ordering.
The names listed in the chart below are Order Names. The actual name of the item may differ from the Order Name.

● MP1800A

Model/Order No.	Name	
Main Frame		
MP1800A	Signal Quality Analyzer	
Standard Accessories		
J0491	Shield Power Cord (13 A):	1 pc
Z0306A	Wrist Strap:	1 pc
Z0541A	USB Mouse:	1 pc
B0329G	Front Cover for 3/4MW 4U:	1 pc
G0342A	ESD DISCHARGER:	1 pc
J1627A	GND Connection Cable:	1 pc
B0574A	MP1800A Protect Cover:	1 pc
MX180000A	Signal Quality Analyzer Control Software:	1 pc
Z0897A	MP1800A Manual CD:	1 pc
Options		
MP1800A-001	GPIB	
MP1800A-002	LAN	
MP1800A-007	OS Upgrade to Windows7	
MP1800A-015	4-Slot for PPG and/or ED	
MP1800A-032	32 Gbit/s PPG and/or ED Support	
Retrofit Options		
MP1800A-101	GPIB Retrofit	
MP1800A-102	LAN Retrofit	
MP1800A-107	OS Upgrade to Windows7 Retrofit	
MP1800A-132	32 Gbit/s PPG and/or ED Support Retrofit	
Calibration Service		
MP1800A-190	25G Calibration of PPG and MUX Retrofit	
Maintenance Service		
MP1800A-ES310	Three Years Extended Warranty Service	
MP1800A-ES510	Five Years Extended Warranty Service	

● MP1862A

Model/Order No.	Name	
Main Frame		
MP1862A	56G/64G bit/s DEMUX	
Standard Accessories		
J1657A	Coaxial Skew Match Pair Cable (1.3 m, K Connector):	2 pcs
J1668A	Coaxial Cable (0.8 m, K connector):	1 pc
J1654A	U Link Cable B:	1 pc
J1363A	Protection Cap:	2 pcs
41V-6	Precision Fixed Attenuator 6 dB:	2 pcs
J1632A	Terminator:	5 pcs
J1341A	Open:	1 pc
J1475A	USB Cable:	1 pc
Z1312A	AC Adapter:	1 pc
G0342A	ESD DISCHARGER:	1 pc
J0017	POWER CORD, 2.5M:	1 pc
Z0897A	MP1800A Manual CD:	1 pc
Z0918A	MX180000A Software CD:	1 pc
Options		
MP1862A-001	64G bit/s Extension	
Retrofit Options		
MP1862A-101	64G bit/s Extension Retrofit	
Optional Accessories		
J1600A	Skew Match Pair Cable (0.2 m, V connector)	
J1656A	Coaxial Cable Set (MP1861A – MP1862A)	
J1646A	Passive Equalizer 6 dB (V connector)	
Maintenance Service		
MP1862A-ES310	Three Years Extended Warranty Service	
MP1862A-ES510	Five Years Extended Warranty Service	

● MP1861A

Model/Order No.	Name	
Main Frame		
MP1861A	56G/64G bit/s MUX	
Standard Accessories		
J1658A	Coaxial Skew Match Pair Cable (1.3 m, K Connector):	1 set
J1652A	Coaxial Cable (0.5 m, K Connector):	1 pc
J1654A	U Link Cable B:	1 pc
J1363A	Protection Cap:	2 pcs
41V-6	Precision Fixed Attenuator 6 dB:	2 pcs
J1632A	Terminator:	4 pcs
J1341A	Open:	3 pcs
J1655A	Semi-rigid Cable (0.2 m, V):	1 pc
J1475A	USB Cable:	1 pc
Z1312A	AC Adapter:	1 pc
G0342A	ESD DISCHARGER:	1 pc
J0017	POWER CORD, 2.5M:	1 pc
Z0897A	MP1800A Manual CD:	1 pc
Z0918A	MX180000A Software CD:	1 pc
Options		
MP1861A-001	64G bit/s Extension	
MP1861A-011	Variable Data Output (0.5 to 2.5 Vp-p)	
MP1861A-013	Variable Data Output (0.5 to 3.5 Vp-p)	
MP1861A-030	Variable Data Delay	
Retrofit Options		
MP1861A-101	64G bit/s Extension Retrofit	
MP1861A-111	Variable Data Output (0.5 to 2.5 Vp-p) Retrofit	
MP1861A-113	Variable Data Output (0.5 to 3.5 Vp-p) Retrofit	
MP1861A-130	Variable Data Delay Retrofit	
Optional Accessories		
J1600A	Skew Match Pair Cable (0.2 m, V connector)	
J1656A	Coaxial Cable Set (MP1861A – MP1862A)	
J1646A	Passive Equalizer 6 dB (V connector)	
Maintenance Service		
MP1861A-ES310	Three Years Extended Warranty Service	
MP1861A-ES510	Five Years Extended Warranty Service	

● MP1825B

Model/Order No.	Name	
Main Frame		
MP1825B*1	4Tap Emphasis	
Standard Accessories		
J1137	Terminator:	3 pcs
J1341A	Open:	2 pcs
J1359A*2	Coaxial Adaptor (K-P, K-J, SMA compatible):	2 pcs/3 pcs
J1507A*3	Semirigid Cable:	1 pc
J1475A	USB Cable:	1 pc
Z1312A	AC Adaptor:	1 pc
	Power Cord:	1 pc
Z0897A	MP1800A Manual CD:	1 pc
Z0918A	MX180000A Software CD:	1 pc
Options		
MP1825B-001	14 Gbit/s Operation	
MP1825B-002	28 Gbit/s Operation	
MP1825B-003	14 Gbit/s Variable Data Delay	
MP1825B-004	28 Gbit/s Variable Data Delay	
MP1825B-005	14.1 Gbit/s Extension	
MP1825B-006	32.1 Gbit/s Extension	
Retrofit Options		
MP1825B-103	14 Gbit/s Variable Data Delay Retrofit	
MP1825B-104	28 Gbit/s Variable Data Delay Retrofit	
MP1825B-105	14.1 Gbit/s Extension Retrofit	
MP1825B-106	32.1 Gbit/s Extension Retrofit	

∗1: MP1825B is not RoHS compliant.
∗2: MP1825B-001: 2 pcs, MP1825B-002: 3 pcs
∗3: Select MP1825B-002

● MU181000B

Model/Order No.	Name	
Unit/Module		
MU181000B	12.5 GHz 4port Synthesizer	
Standard Accessories		
J1349A	Coaxial Cable 0.3 m (SMA, DC to 18 GHz):	4 pcs
Option		
MU181000B-001	Jitter Modulation	
Retrofit Option		
MU181000B-101	Jitter Modulation Retrofit	
Maintenance Service		
MU181000B-ES310	Three Years Extended Warranty Service	
MU181000B-ES510	Five Years Extended Warranty Service	

● MU181500B

Model/Order No.	Name	
Unit/Module		
MU181500B	Jitter Modulation Source	
Standard Accessories		
J1349A	Coaxial Cable 0.3 m (SMA, DC to 18 GHz):	1 pc
J1508A	BNC-SMA Connector Cable (30 cm):	2 pcs
J1137	Terminator:	6 pcs
J1341A	Open:	2 pcs
Z0897A	MP1800A Manual CD:	1 pc
Z0918A	MX180000A Software CD:	1 pc
Maintenance Service		
MU181500B-ES310	Three Years Extended Warranty Service	
MU181500B-ES510	Five Years Extended Warranty Service	

● MU181800B

Model/Order No.	Name
Unit/Module	
MU181800B	14 GHz Clock Distributor
Option	
MU181800B-005	14.1 GHz Extension
Retrofit Option	
MU181800B-105	14.1 GHz Extension Retrofit
Maintenance Service	
MU181800B-ES310	Three Years Extended Warranty Service
MU181800B-ES510	Five Years Extended Warranty Service

● MU181020B

Model/Order No.	Name	
Unit/Module		
MU181020B*4	14 Gbit/s PPG	
Standard Accessories		
J1137	Terminator (50Ω):	3 pcs
J1341A	Open:	1 pc
Options		
MU181020B-002	0.1 to 14 Gbit/s	
MU181020B-005	14.1 Gbit/s Extension	
MU181020B-011	Variable Data Output (0.25 to 2.5 Vp-p)	
MU181020B-012	High Performance Data Output (0.05 to 2.0 Vp-p)	
MU181020B-013	Variable Data Output (0.5 to 3.5 Vp-p)	
MU181020B-030	Variable Data Delay	
Retrofit Options		
MU181020B-105	14.1 Gbit/s Extension Retrofit	
MU181020B-111	Variable Data Output (0.25 to 2.5 Vp-p) Retrofit	
MU181020B-112	High Performance Data Output (0.05 to 2.0 Vp-p) Retrofit	
MU181020B-113	Variable Data Output (0.5 to 3.5 Vp-p) Retrofit	
MU181020B-130	Variable Data Delay Retrofit	
Standard Accessories for MU181020B-011/111		
J1359A	Coaxial Adapter (K-P, K-J, SMA):	2 pcs
Standard Accessories for MU181020B-012/112		
J1359A	Coaxial Adapter (K-P, K-J, SMA):	2 pcs
Standard Accessories for MU181020B-013/113		
J1359A	Coaxial Adapter (K-P, K-J, SMA):	2 pcs
Maintenance Service		
MU181020B-ES310	Three Years Extended Warranty Service	
MU181020B-ES510	Five Years Extended Warranty Service	

∗4: MU181020B is not RoHS compliant.

● MU181040B

Model/Order No.	Name	
Unit/Module		
MU181040B*5	14 Gbit/s ED	
Options		
MU181040B-002	0.1 to 14 Gbit/s	
MU181040B-005	14.1 Gbit/s Extension	
MU181040B-020	Clock Recovery	
MU181040B-030	Variable Clock Delay	
Retrofit Options		
MU181040B-105	14.1 Gbit/s Extension Retrofit	
MU181040B-120	Clock Recovery Retrofit	
MU181040B-130	Variable Clock Delay Retrofit	
Standard Accessories for MU181040B-002		
J1341A	Open:	3 pcs
J1359A	Coaxial Adapter (K-P, K-J, SMA):	2 pcs
J1137	Terminator (50Ω):	2 pcs
Standard Accessories for MU181040B-020/120		
J1137	Terminator (50Ω):	1 pc
Maintenance Service		
MU181040B-ES310	Three Years Extended Warranty Service	
MU181040B-ES510	Five Years Extended Warranty Service	

∗5: MU181040B is not RoHS compliant.

• MU183020A

Model/Order No.	Name	
Unit/Module		
MU183020A	28G/32G bit/s PPG	
Standard Accessories		
J1137	Terminator:	3 pcs
J1359A	Coaxial Adaptor (K-P, K-J, SMA):	1 pc
J1341A	Open:	1 pc
J0541E	6 dB Fixed Attenuator:	1 pc
Z0897A	MP1800A Manual CD:	1 pc
Z0918A	MX180000A Software CD:	1 pc
Options		
MU183020A-001	32G bit/s Extension	
MU183020A-012	1ch 2 V Data Output	
MU183020A-013	1ch 3.5 V Data Output	
MU183020A-022	2ch 2 V Data Output	
MU183020A-023	2ch 3.5 V Data Output	
MU183020A-030	1ch Data Delay	
MU183020A-031	2ch Data Delay	
Retrofit Options		
MU183020A-101	32G bit/s Extension Retrofit	
MU183020A-112	1ch 2 V Data Output Retrofit	
MU183020A-113	1ch 3.5 V Data Output Retrofit	
MU183020A-122	2ch 2 V Data Output Retrofit	
MU183020A-123	2ch 3.5 V Data Output Retrofit	
MU183020A-130	1ch Data Delay Retrofit	
MU183020A-131	2ch Data Delay Retrofit	
Standard Accessories for MU183020A-x12, x13		
J1137	Terminator:	2 pcs
J1359A	Coaxial Adaptor (K-P, K-J, SMA):	2 pcs
Standard Accessories for MU183020A-x22, x23		
J1137	Terminator:	4 pcs
J1359A	Coaxial Adaptor (K-P, K-J, SMA):	4 pcs
Maintenance Service		
MU183020A-ES310	Three Years Extended Warranty Service	
MU183020A-ES510	Five Years Extended Warranty Service	

• MU183040B

Model/Order No.	Name	
Unit/Module		
MU183040B	28G/32G bit/s High Sensitivity ED	
Standard Accessories		
J1137	Terminator:	2 pcs
J1341A	Open:	1 pc
Z0897A	MP1800A Manual CD:	1 pc
Z0918A	MX180000A Software CD:	1 pc
Options		
MU183040B-001	32 Gbit/s Extension	
MU183040B-010	1ch ED	
MU183040B-020	2ch ED	
MU183040B-022	2.4G to 28.1G bit/s Clock Recovery	
MU183040B-023	25.5G to 32.1G bit/s Clock Recovery	
Retrofit Options		
MU183040B-101	32 Gbit/s Extension Retrofit	
MU183040B-110	1ch ED Retrofit	
MU183040B-120	2ch ED Retrofit	
MU183040B-122	2.4G to 28.1G bit/s Clock Recover Retrofit	
MU183040B-123	25.5G to 32.1G bit/s Clock Recovery Retrofit	
Standard Accessories for MU183040B-x10		
J1341A	Open:	2 pcs
J1359A	Coaxial Adaptor (K-P, K-J, SMA):	2 pcs
41KC-6	Precision Fixed Attenuator 6 dB:	2 pcs
Standard Accessories for MU183040B-x20		
J1341A	Open:	4 pcs
J1359A	Coaxial Adaptor (K-P, K-J, SMA):	4 pcs
41KC-6	Precision Fixed Attenuator 6 dB:	4 pcs
Maintenance Service		
MU183040B-ES310	Three Years Extended Warranty Service	
MU183040B-ES510	Five Years Extended Warranty Service	

• MU183021A

Model/Order No.	Name	
Unit/Module		
MU183021A	28G/32G bit/s 4ch PPG	
Standard Accessories		
J1137	Terminator:	3 pcs
J1359A	Coaxial Adaptor (K-P, K-J, SMA):	1 pc
J1341A	Open:	1 pc
J0541E	6 dB Fixed Attenuator:	1 pc
Z0897A	MP1800A Manual CD:	1 pc
Z0918A	MX180000A Software CD:	1 pc
Options		
MU183021A-001	32G bit/s Extension	
MU183021A-012	4ch 2.0 V Data Output	
MU183021A-013	4ch 3.5 V Data Output	
MU183021A-030	4ch Data Delay	
Retrofit Options		
MU183021A-101	32G bit/s Extension Retrofit	
MU183021A-112	4ch 2.0 V Data Output Retrofit	
MU183021A-113	4ch 3.5 V Data Output Retrofit	
MU183021A-130	4ch Data Delay Retrofit	
Standard Accessories for MU183021A-x12, x13		
J1137	Terminator:	8 pcs
J1359A	Coaxial Adaptor (K-P, K-J, SMA):	8 pcs
Maintenance Service		
MU183021A-ES310	Three Years Extended Warranty Service	
MU183021A-ES510	Five Years Extended Warranty Service	

• MU183041B

Model/Order No.	Name	
Unit/Module		
MU183041B	28G/32G bit/s 4ch High Sensitivity ED	
Standard Accessories		
J1137	Terminator:	3 pcs
J1341A	Open:	9 pcs
J1359A	Coaxial Adaptor (K-P, K-J, SMA):	8 pcs
41KC-6	Precision Fixed Attenuator 6 dB:	8 pcs
Z0897A	MP1800A Manual CD:	1 pc
Z0918A	MX180000A Software CD:	1 pc
Options		
MU183041B-001	32 Gbit/s Extension	
MU183041B-022	2.4G to 28.1G bit/s Clock Recovery	
MU183041B-023	25.5G to 32.1G bit/s Clock Recovery	
Retrofit Options		
MU183041B-101	32 Gbit/s Extension Retrofit	
MU183041B-122	2.4G to 28.1G bit/s Clock Recovery Retrofit	
MU183041B-123	25.5G to 32.1G bit/s Clock Recovery Retrofit	
Maintenance Service		
MU183041B-ES310	Three Years Extended Warranty Service	
MU183041B-ES510	Five Years Extended Warranty Service	

● MZ1834A

Model/Order No.	Name	
Main Frame		
MZ1834A	4PAM Converter	
Standard Accessories		
J1359A	Coaxial Adaptor (K-P, K-J, SMA):	2 pcs
Z0897A	MP1800A Manual CD:	1 pc

● MZ1834B

Model/Order No.	Name	
Main Frame		
MZ1834B	4PAM Converter	
Standard Accessories		
J1359A	Coaxial Adaptor (K-P, K-J, SMA):	2 pcs
Z0897A	MP1800A Manual CD:	1 pc

● MZ1838A

Model/Order No.	Name	
Main Frame		
MZ1838A	8PAM Converter	
Standard Accessories		
J1359A	Coaxial Adaptor (K-P, K-J, SMA):	2 pcs
Z0897A	MP1800A Manual CD:	1 pc

● MZ1854A

Model/Order No.	Name
Main Frame	
MZ1854A	Data Signal Combiner
Standard Accessory	
Z0897A	MP1800A Manual CD

● G0373A*6

Model/Order No.	Name
Main Frame	
G0373A	USB3.1 Receiver Test Adapter

● G0374A*6

Model/Order No.	Name	
Main Frame		
G0374A	64Gbaud PAM4 DAC	
Standard Accessories		
J1611A	Coaxial Cable (1.3 m, K connector):	1 pc
J1741A	Electrical Length Specified Coaxial Cable (0.8 m, K Connector):	4 pc
V210	Coaxial Terminator:	1 pc
J0017F	POWER CORD, 2.6M:	1 pc
G0342A	ESD DISCHARGER:	1 pc

● G0375A*6

Model/Order No.	Name	
Main Frame		
G0375A	32 Gbaud Power PAM4 Converter	
Standard Accessories		
J1741A	Electrical Length Specified Coaxial Cable (0.8 m, K Connector):	4 pc
J1475A	USB Cable:	1 pc

● G0376A*6

Model/Order No.	Name	
Main Frame		
G0376A	32 Gbaud PAM4 Decoder with CTLE	
Standard Accessories		
J1728A	Electrical Length Specified Coaxial Cable (0.4 m, K connector):	2 pc
J1475A	USB Cable:	1 pc

● Software

Model/Order No.	Name
MX180000A	Signal Quality Analyzer Control Software
MX180001A	SDH/SONET Pattern Editor
MX180003A	GbE/10 GbE Pattern Editor
MX180004A	PON Application Software
MX180014A*7	100G EPON Application Software
MX180005A	Jitter Application Software
MX181500A	Jitter/Noise Tolerance Test Software
MX183000A*7, *8	High-Speed Serial Data Test Software
MX183000A-PL001*7	Jitter Tolerance Test
MX183000A-PL011*7	PCIe Link Sequence
MX183000A-PL012*7	USB Link Sequence

∗7: Supports Windows 7 OS Only
∗8: MP1800A is shipped with MX183000A installed

● Before Using VISA*9

For Those Who Use MP1800A

To use the MX183000A High-Speed Serial Data Test Software (hereafter MX183000A), you are required to install National Instruments™ (hereafter NI™) NI-VISA™*10 on the PC controller. We recommend using NI-VISA™ provided in the USB memory stick that contains MX183000A.
You are allowed to use NI-VISA™ contained in the USB memory stick only for the purpose of using it for MX183000A. Use of NI-VISA™ for any other product or purpose is prohibited.
When uninstalling MX183000A from the PC controller, uninstall NI-VISA™ that was installed from the USB memory stick as well.

∗9: Virtual Instrument Software Architecture I/O software specification for remote control of measuring instruments using interfaces such as GPIB, Ethernet, USB, etc.
∗10: World de facto standard I/O software interface developed by NI and standardized by the VXI Plug&Play Alliance.

● Optional Accessories

Model/Order No.	Name
J1621A	Passive Equalizer 3 dB
J1622A	Passive Equalizer 6 dB
J0008	GPIB Cable 2 m
J1137	Terminator (50 Ω)
J1341A	Open
J1342A	Coaxial Cable 0.8 m (APC-3.5, DC to 27.5 GHz)
J1349A	Coaxial Cable 0.3 m (SMA, DC to 18 GHz)
J1439A	Coaxial Cable 0.8 m (K connector, DC to 40 GHz)
J1620A	Coaxial Cable (0.9 m, K connector)
J1550A	Coaxial Skew Match Cable (0.8 m, APC3.5, DC to 27.5 GHz, Skew <3 ps, pair cable)
J1551A	Coaxial Skew Match Cable (0.8 m, K connector, DC to 40 GHz, Skew <3 ps, pair cable)
J1611A	Coaxial Cable (1.3 m, K connector)
J1615A	Coaxial Cable Set (PPG-Emphasis, for jitter tolerance measurement, 2 pcs)
J1618A	Coaxial Cable Set (Jitter-2chPPG-2chEmphasis, for jitter tolerance measurement, 6 pcs)
J1359A	Coaxial Adapter (K-P, K-J, SMA)
J1360A	Measurement Kit <J1342A × 2, J1625A × 1>
J1449A	Measurement Kit (K connector) <J1439A × 2, J1342A × 2, J1625A × 1>
J1678A	ESD Protection Adapter-K
J1679A	ESD Protection Adapter-V
J1600A	Skew Match Pair Cable (0.2 m, V connector)
J1656A	Coaxial Cable Set (MP1861A – MP1862A)
J1646A	Passive Equalizer 6 dB (V connector)
Z0897A	MP1800A Manual CD
Z0917A	Shielded LAN Cable, 5 m (CAT5, Straight)
Z0918A	MX180000A Software CD
Z0922A	English USB Keyboard (104 key)
B0588A	Rack Mount Kit (MP1800A)
B0576A	Blank Panel
B0566A	MP1800A Hard Carrying Case (MP1800A)
W2745AE	MP1800A Operation Manual
W2747AE	MP1800A Installation Guide
W2746AE	MT1810A Operation Manual
W2748AE	MT1810A Installation Guide
W2750AE	MU181000A/B Operation Manual
W2752AE	MU181020B Operation Manual
W2753AE	MU181040B Operation Manual
W3481AE	MU181500B Operation Manual
W2751AE	MU181800A/B Operation Manual
W3594AE	MU183020A/MU183021A Operation Manual
W2749AE	MX180000A Operation Manual
W2799AE	MX180000A Remote Control Operation Manual
W2884AE	MX180001A Operation Manual
W2886AE	MX180003A Operation Manual
W2887AE	MX180004A Operation Manual
W2926AE	MX180005A Operation Manual
M-W3864AE	MX180014A Operation Manual
W3480AE	MX181500A Operation Manual
W3813AE	MX183000A Operation Manual

Model/Order No.	Name
41KC-3	Precision Fixed Attenuator 3 dB
41KC-6	Precision Fixed Attenuator 6 dB
41KC-10	Precision Fixed Attenuator 10 dB
41KC-20	Precision Fixed Attenuator 20 dB
K240C	Precision Power Divider
K241C	Precision Power Splitter
Z0306A	Wrist Strap
P0047A	Frequency Doublers
Z1340A	13 GHz BPF
G0361A*6	64Gbaud 2-bit DAC with MUX
J1398A	N-SMA ADAPTOR
J1508A	BNC-SMA Connector Cable (30 cm)
J1510A	Pick OFF Tee
J1627A	GND Connection Cable
J1624A	Coaxial Cable 0.3 m (SMA Connector)
J1625A	COAXIAL CABLE 1M (SMA Connector)
J1632A	Terminator (SMA)
J1715A	Coaxial Skew Match Cable (0.1M, SMP-J,SMA-J)
K220B	Coaxial Adapter
K261	DC Block
K250	Bias T
Z1927A	USB Measurement Kit
J1721A	USB Measurement Component Set
J1722A	PCIe Measurement Component Set
J1723A	TBT Measurement Component Set
J1724A	Compliance Test Component Set
J1735A	Combiner
J1728A	Electrical Length Specified Coaxial Cable (0.4 m, K connector)
J1741A	Electrical Length Specified Coaxial Cable (0.8 m, K Connector)
J1742A	Electrical Length Specified Coaxial Cable (0.84 m, K Connector)

∗6: The warranty period shall be 1 year under normal use.
Repair by exchange for new during the warranty period shall be limited to one instance.
Repair using new spare parts shall be charged after the warranty period has expired.

Moreover, Anritsu Corporation will deem this warranty void when:

- When new spare parts can no longer be easily obtained when more than 5 years have elapsed after manufacture.

Anritsu

Specifications are subject to change without notice.

● **United States**
Anritsu Americas Sales Company
450 Century Parkway, Suite 190, Allen,
TX 75013 U.S.A.
Phone: +1-800-Anritsu (1-800-267-4878)

● **Canada**
Anritsu Electronics Ltd.
700 Silver Seven Road, Suite 120, Kanata,
Ontario K2V 1C3, Canada
Phone: +1-613-591-2003
Fax: +1-613-591-1006

● **Brazil**
Anritsu Eletronica Ltda.
Praça Amadeu Amaral, 27 - 1 Andar
01327-010 - Bela Vista - Sao Paulo - SP
Brazil
Phone: +55-11-3283-2511
Fax: +55-11-3288-6940

● **Mexico**
Anritsu Company, S.A. de C.V.
Blvd Miguel de Cervantes Saavedra #169 Piso 1, Col. Granada
Mexico, Ciudad de Mexico, 11520, MEXICO
Phone: +52-55-4169-7104

● **United Kingdom**
Anritsu EMEA Ltd.
200 Capability Green, Luton, Bedfordshire, LU1 3LU, U.K.
Phone: +44-1582-433200
Fax: +44-1582-731303

● **France**
Anritsu S.A.
12 avenue du Québec, Bâtiment Iris 1- Silic 612,
91140 VILLEBON SUR YVETTE, France
Phone: +33-1-60-92-15-50
Fax: +33-1-64-46-10-65

● **Germany**
Anritsu GmbH
Nemetschek Haus, Konrad-Zuse-Platz 1
81829 München, Germany
Phone: +49-89-442308-0
Fax: +49-89-442308-55

● **Italy**
Anritsu S.r.l.
Via Elio Vittorini 129, 00144 Roma, Italy
Phone: +39-6-509-9711
Fax: +39-6-502-2425

● **Sweden**
Anritsu AB
Isafjordsgatan 32C, 164 40 KISTA, Sweden
Phone: +46-8-534-707-00

● **Finland**
Anritsu AB
Teknobulevardi 3-5, FI-01530 VANTAA, Finland
Phone: +358-20-741-8100
Fax: +358-20-741-8111

● **Denmark**
Anritsu A/S
Torveporten 2, 2500 Valby, Denmark
Phone: +45-7211-2200
Fax: +45-7211-2210

● **Russia**
Anritsu EMEA Ltd.
Representation Office in Russia
Tverskaya str. 16/2, bld. 1, 7th floor.
Moscow, 125009, Russia
Phone: +7-495-363-1694
Fax: +7-495-935-8962

● **Spain**
Anritsu EMEA Ltd.
Representation Office in Spain
Edificio Cuzco IV, Po. de la Castellana, 141, Pta. 5
28046, Madrid, Spain
Phone: +34-915-726-761
Fax: +34-915-726-621

● **United Arab E**
Anritsu EMEA Ltd.
Dubai Liaison Office
902, Aurora Tower,
P O Box: 500311- Dubai Internet City
Dubai, United Arab Emirates
Phone: +971-4-3758479
Fax: +971-4-4249036

● **India**
Anritsu India Private Limited
6th Floor, Indiqube ETA, No.38/4, Adjacent to EMC2,
Doddanekundi, Outer Ring Road, Bengaluru – 560048, India
Phone: +91-80-6728-1300
Fax: +91-80-6728-1301

● **Singapore**
Anritsu Pte. Ltd.
11 Chang Charn Road, #04-01, Shriro House
Singapore 159640
Phone: +65-6282-2400
Fax: +65-6282-2533

● **P.R. China (Shanghai)**
Anritsu (China) Co., Ltd.
Room 2701-2705, Tower A,
New Caohejing International Business Center
No. 391 Gui Ping Road Shanghai, 200233, P.R. China
Phone: +86-21-6237-0898
Fax: +86-21-6237-0899

● **P.R. China (Hong Kong)**
Anritsu Company Ltd.
Unit 1006-7, 10/F., Greenfield Tower, Concordia Plaza,
No. 1 Science Museum Road, Tsim Sha Tsui East,
Kowloon, Hong Kong, P.R. China
Phone: +852-2301-4980
Fax: +852-2301-3545

● **Japan**
Anritsu Corporation
8-5, Tamura-cho, Atsugi-shi, Kanagawa, 243-0016 Japan
Phone: +81-46-296-6509
Fax: +81-46-225-8352

● **Korea**
Anritsu Corporation, Ltd.
5FL, 235 Pangyoyeok-ro, Bundang-gu, Seongnam-si,
Gyeonggi-do, 13494 Korea
Phone: +82-31-696-7750
Fax: +82-31-696-7751

● **Australia**
Anritsu Pty. Ltd.
Unit 20, 21-35 Ricketts Road,
Mount Waverley, Victoria 3149, Australia
Phone: +61-3-9558-8177
Fax: +61-3-9558-8255

● **Taiwan**
Anritsu Company Inc.
7F, No. 316, Sec. 1, NeiHu Rd., Taipei 114, Taiwan
Phone: +886-2-8751-1816
Fax: +886-2-8751-1817

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Please Contact: