Anritsu Advancing beyond

PCIe SSC Test using MP1900A

Signal Quality Analyzer-R MP1900A Series

Contents

1 Introduction

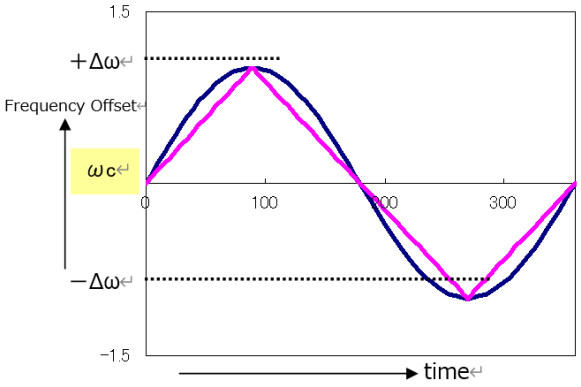
Spread Spectrum Clocking (SSC) is a signal modulation technology used by interfaces for connecting various electronic parts within a product and by external equipment connections.
To reduce electromagnetic interference (EMI), the U.S. FCC and EU guidelines establish the following rigorous rules concerning clock signal modulation, or in other words jitter addition, frequency distribution scatter, and the concentration of energy at specific EMI frequencies.
Since PCIe also uses SSC technology, the above guidelines also explain the required standards.
On the other hand, SSC is a factor causing jitter components degrading overall system communications quality. For example, confirming interconnectivity while applying SSC is a key subject because problems such as data loss occur when equipment peers cannot link-up due to interconnectivity issues.

2 SSC Outline

SSC standardized by PCIe is triangular-shaped modulation waveform. Generally, frequency modulation is applied as phase-modulation components, which are large stress components for electronic parts.
When converting frequency modulation to phase modulation, the phase displacement ΔTTpp at the triangular-shaped frequency modulation is defined as follows:

$$\Delta TT_{PP} = \frac{\pi}{4} \cdot \frac{1}{2 \cdot \pi \cdot fc} \cdot \frac{\Delta f_{PP}}{fm}$$

fc : Center Frequency
fm : Modulation Frequency
Δf_{PP} : Frequency Deviation (Peak to Peak)
$\Delta \theta_{PP}$: Phase Deviation (Peak to Peak) ・・・ [rad]
ΔT_{PP} : Phase Deviation (Peak to Peak) ・・・ [s]



As defined by PCIe, 5000 ppm frequency modulation at 30 to 33 kHz is equivalent to phase modulation of about 20 ns and is clearly a major high-stress source.

3 PCI-SIG Activities

The PCI-SIG Base Specification regulates the following SSC modulation requirements.

Table 1. Base Specification Rev 5.0 Ver 1.0

Symbol	Description	Limits	Units	Notes
F_{REFCLK}	Refclk Frequency	99.97 (min) 100.03 (max)	MHz	
F_{REFCLK_32G}	Refclk Frequency for devices that support 32.0 GT/s	99.99 (min) 100.01 (max)	MHz	
F_{SSC}	SSC frequency range	30 (min) 33 (max)	kHz	3
$T_{SSC\text{-}FREQ\text{-}DEVIATION}$	SSC deviation	-0.5 (min) 0.0 (max)	%	3
$T_{SSC\text{-}FREQ\text{-}DEVIATION\_32G\_SRIS}$	SSC deviation for devices that support 32.0 GT/s and SRIS when operating in SRIS mode at all speeds	-0.3 (min) 0.0 (max)	%	3
$T_{TRANSPORT\text{-}DELAY}$	Tx-Rx transport delay	12 (max)	ns	1, 4
$T_{SSC\text{-}MAX\text{-}FREQ\text{-}SLEW}$	Max SSC df/dt	1250	ppm/ µs	2, 3

Notes:

1. Parameter is relevant only for Common Refclk architecture.
2. Measurement is made over 0.5 µs time interval with a 1st order LPF with an f_c of 60x the modulation frequency.
3. When testing the a device configured for the IR reference clock architecture the SSC related parameters must be tested with the Tx output data instead of the reference clock.
4. There are form factors (for example topologies including long cables) that may exceed the transport delay limit. Extra jitter from the large transport delay must be accounted by these form factor specifications.

Although the Base Specification regulates electrical requirements at the chip level, SSC was not a required item in the Compliance Test prior to Gen4. As a result, although the Receiver Test in the Compliance Test defines the worst-case conditions for other types of stress tests (SJ, RJ, DM-I, CM-I, Insertion Loss), there were no requirements concerning application of SSC.
On the other hand, the many PCIe systems on the market support SSC application from the perspective of reducing EMI. As a result, although many systems validated by the Compliance Test claim to support application of SSC, since SSC application tests have not actually been executed, sometimes, there are SSC-related problems in the commercial market.
In these circumstances, PCI-SIG revised the PHY Test Specification regulating the Compliance Test electrical test methods to specify worst-case conditions for SSC application and added clear SSC Application requirements to Draft 0.7 of the PCIe 5.0 PHY Test Specification.

2.15.6 Add-in Card Receiver Link Equalization Test for 32.0 GT/s

The test is performed by following these steps:

1. Insert the Add-in Card under test into the CEM 5.0 CBB without power. The signal source should be connected to the Rx lane under test on the CBB, the receiver of the protocol aware test equipment should be connected to the Tx lane under test on the CBB. Other TX lanes can be terminated with 50-ohm terminations or unterminated – as requested by the device under test operator.

~~2.~~ Connect 100MHz SSC enabled (-0.5% down-spread) REF CLK from BERT into the CLK IN connectors on CBB.

AIC (Add-In Card) Receiver Test Procedure

2.16.6 System Board Receiver Link Equalization Test for 32.0 GT/s

1. Insert the CEM 5.0 CLB into the system under test without power. The signal source should be connected to the Rx lane under test on the CLB, the receiver of the protocol aware test equipment should be connected to the Tx lane under test on the CLB. The CLB 100 MHz clock output from the system under test shall be connected to the test equipment and drive the test equipment transmissions after being filtered by a *PCI Express Base Specification* compliant PLL or equivalent. The system will use SSC enabled or SSC disabled reference clock to be consistent with settings for the system during normal operation. Other TX lanes must be unterminated on the CLB.

System Receiver Test Procedure

4 Anritsu Solution

4.1 Product Setup and Jitter Tolerance Standards

For the Receiver test, the Anritsu solution uses a Pulse Pattern Generator (PPG) to apply SSC and measures the BER of the signal with applied SSC using an Error Detector (ED).

SI PPG MU195020A Specifications

Jitter Tolerance

Jitter Tolerance Mask*	Bit rate: 16, 28.1*, 32.1 Gbit/s* Pattern: PRBS $2^{31} - 1$ SSC with a 7000 ppm amplitude and RJ of 0.3 UI can be simultaneously applied by using MU181500B. These specifications are defined assuming the following conditions: Loopback connection to the MU195040A, defined by one specific temperature in the range of 20°C to 30°C. When RJ + BUJ is bigger than 0.5 UIp-p or SJ + RJ + BUJ is bigger than the standard value + 0.3 UIp-p, "Overload" is displayed on the MU181500B screen..

PPG Jitter Tolerance Specification

SI ED MU195040A Specifications

Jitter Tolerance

Jitter Tolerance	Bit rate: 16 Gbit/s, 28.1 Gbit/s*, 32.1 Gbit/s* Pattern: PRBS $2^{31} - 1$ SSC with a 7000 ppm amplitude and RJ of 0.3 UI can be simultaneously applied by using MU181500B. These specifications are defined assuming the following conditions: Loopback connection to the MU195020A, defined by one specific temperature in the range of 20°C to 30°C. When RJ + BUJ is bigger than 0.5 UIp-p or SJ + RJ + BUJ is bigger than the standard value + 0.3 UIp-p, "Overload" is displayed on the MU181500B screen.

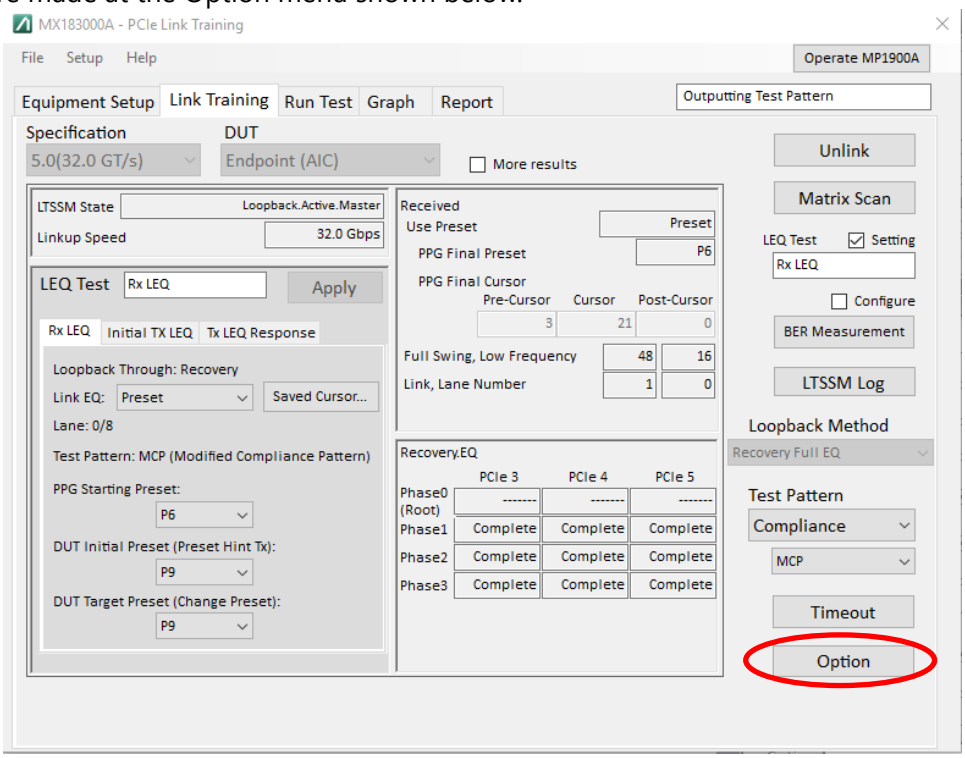
ED Jitter Tolerance Specification

4.2 Rx LEQ Test Support

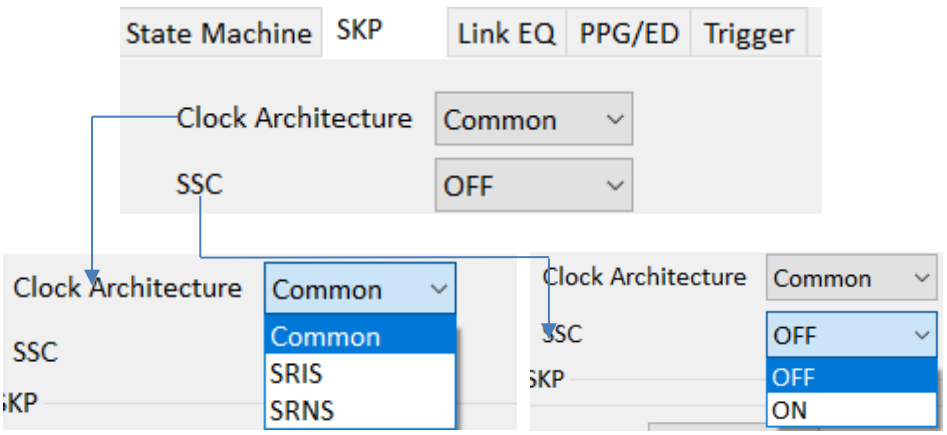
The Signal Quality Analyzer-R MP1900A supports tests with the following clock architectures

- Common Clock with SSC
- Common Clock without SSC
- SRIS (Separate Reference Independent SSC)
- SRNS (Separate Reference Clock Non SSC)

Settings are made at the Option menu shown below.



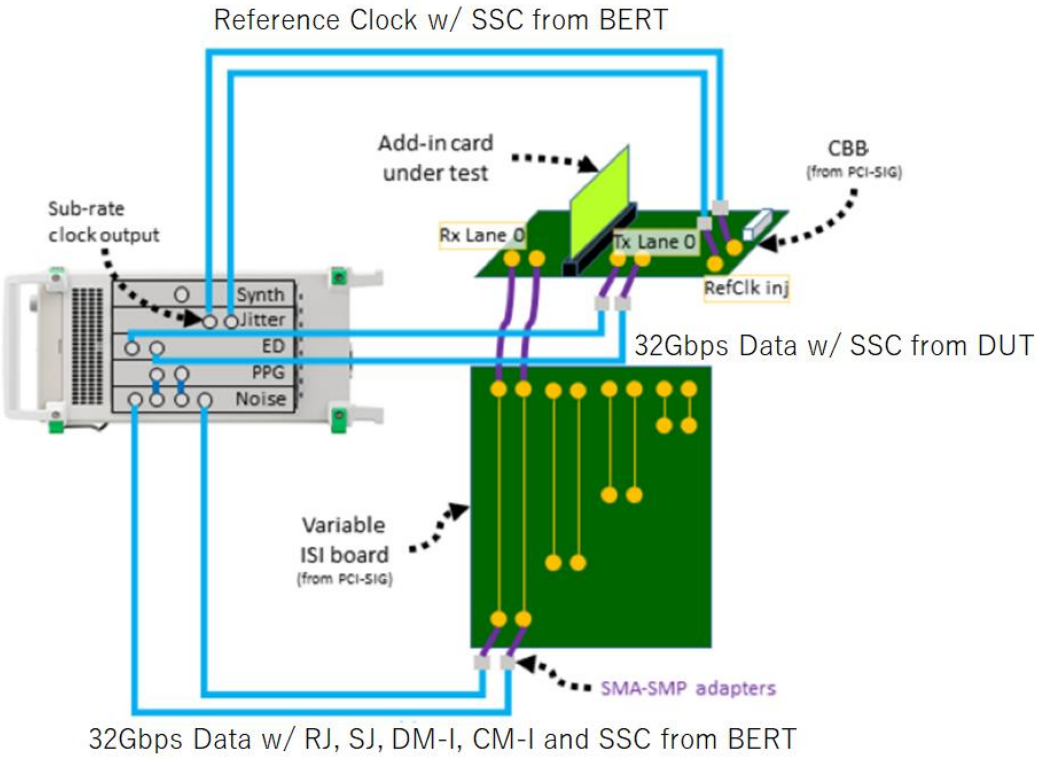
Rx LEQ Test Application



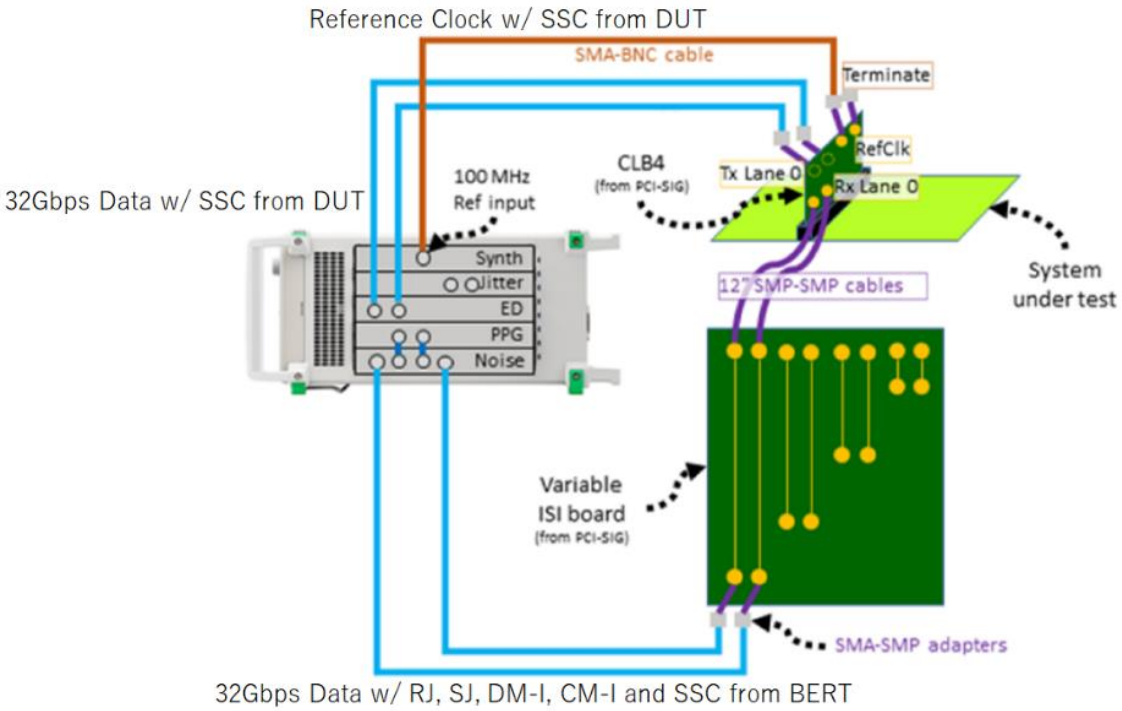
Clock Architecture Settings

4.3 Rx LEQ Compliance Test Setup

The Compliance Test specifies testing with a Common Clock.
Although the measurement target can be either the Add in Card (AIC) or System, as shown in the following setup diagrams, the MP1900A supports SSC stress tests of both as the target DUT.



AIC Receiver Test Setup



System Receiver Test Setup

5 Conclusion

This application note has introduced the use of SSC in the PCIe market and the importance of testing under these environments.
Sometimes, latent errors that are not a problem may occur at conventional Compliance Tests with applied SSC. At testing under these environments, pretesting to discover latent error factors is important to improve and assure product quality.
These requirements dictate the specifications for a Bit Error Rate Tester (BERT) used for these particular tests. The measuring instrument itself must also be able to withstand higher stress signals than specified by the test. Anritsu's MP1900A is currently the only measuring instrument supporting these conditions.
Anritsu supports worst-case testing with timely solutions helping to improve customers' product quality and contributing to the industry's development

References

PCI-Express Base Specification 5.0 Ver 1.0
PCI-Express PHY Test Specification 5.0 Ver 0.7 (Draft)

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210422

Printed in Japan 2021-6 MJM No. MP1900A_PCIeSSC-E-F-1-(1.00)