FPGA Setup for LL10GEMAC-IP Loopback Test

Rev1.0 29-Apr-21

This document describes how to setup FPGA board and prepare the test environment for running LL10GEMAC-IP loopback demo and measuring the latency time. User sets test parameters on FPGA board and monitors the hardware status via Serial console. More details of the demo are described as follows.

1 Test environment List

To run loopback demo of LL10GEMAC IP, please prepare following test environment.

- FPGA development board: ZCU102
- (Optional) SFP+ Loopback cable for external loopback mode
- Two micro USB cables for programming FPGA and Serial console monitoring, connecting between FPGA board and PC
- Serial console software such as TeraTerm installed on PC. The setting on the console is Baudrate=115,200, Data=8-bit, Non-parity, and Stop=1.
- Vivado tool for programming FPGA, installed on PC

Note: The latency time in the test depends on clock phase shift characteristic when the board boots up. Reset button is designed to reset the system which will change clock phase shift characteristic. Therefore, the user can press Reset button and may get the different latency time on the test.

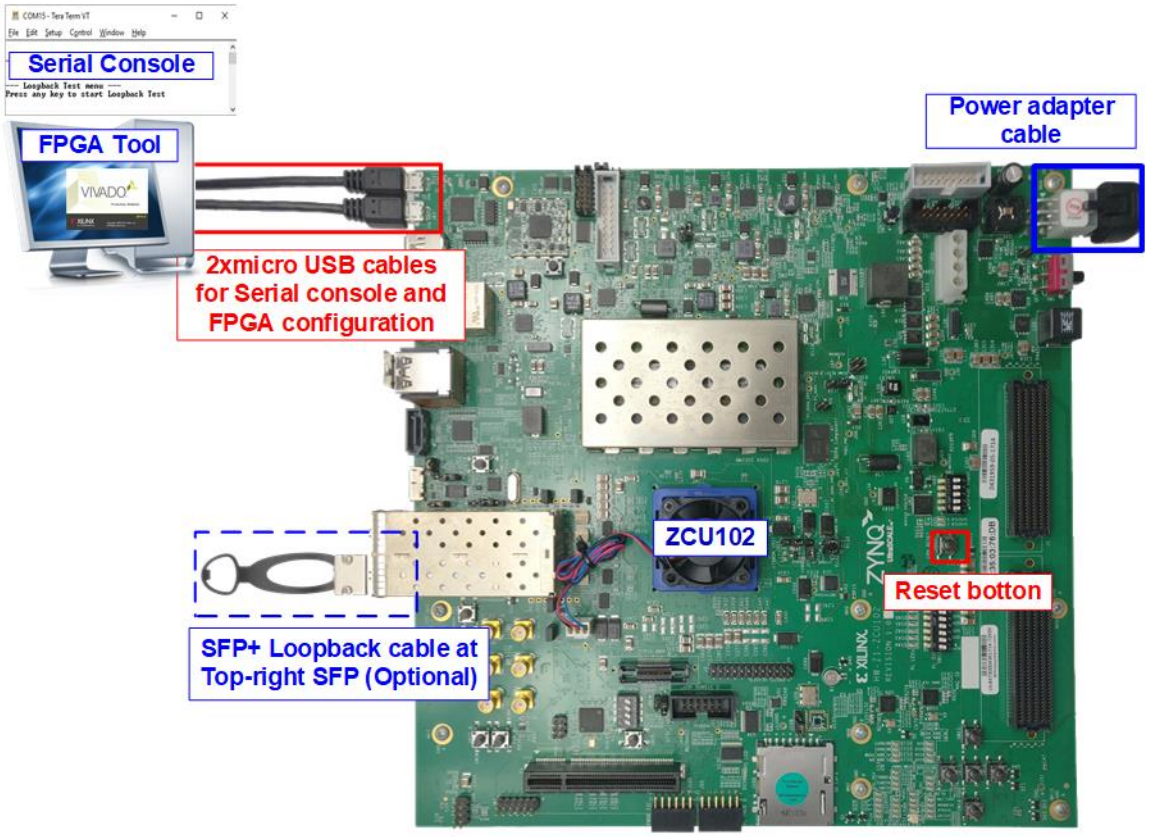

Figure 1-1 LL10GEMAC demo on ZC102

2 Test environment Setup

The step to setup test environment by using FPGA and PC is described in more details as follows.

1) Check DIPSW and jumper setting on FPGA board as shown in Figure 2-1.
   i) Insert jumper to J16 to enable Tx SFP+.
   ii) Set SW6=all ONs to use USB-JTAG.

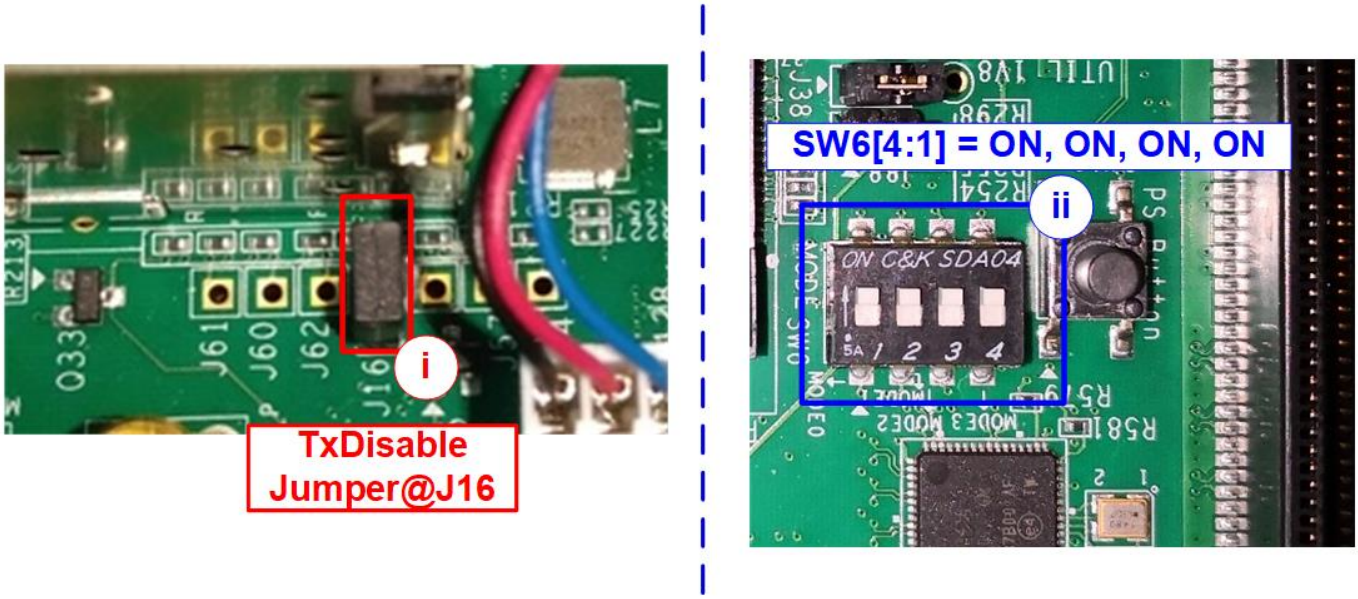

Figure 2-1 ZCU102 board setting

2) Connect two micro USB cables from FPGA board to PC for JTAG programming and USB UART.
3) Connect power supply to FPGA development board.
4) (Optional for running external loopback mode) Connect SFP+ Loopback cable at the top-right SFP+ channel, as shown in Figure 2-2.

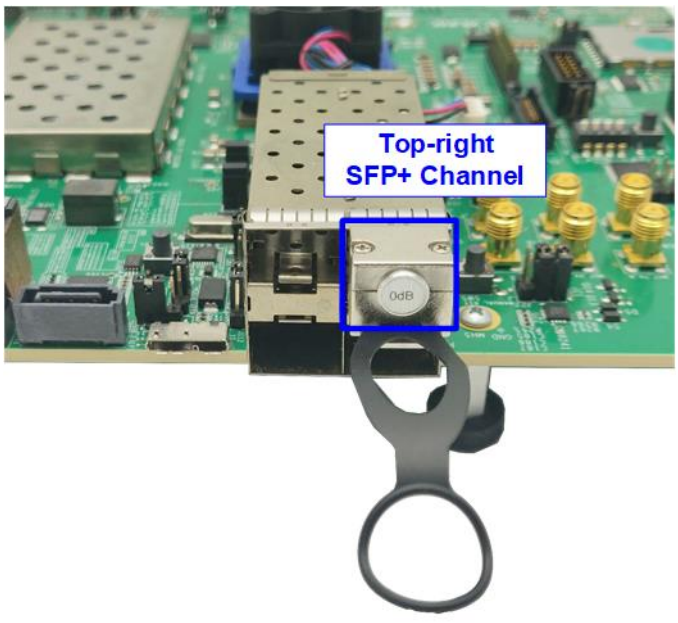

Figure 2-2 Loopback cable on ZCU102 board

5) Power on FPGA board.
6) Open Serial console. When connecting FPGA board to PC, many COM ports from FPGA connection are detected and displayed on Device Manager.

   For ZCU102, select COM port number of Interface0 to be Serial console.

   On Serial console, use following setting: Buad rate=115,200, Data=8-bit, Non-Parity, and Stop = 1.

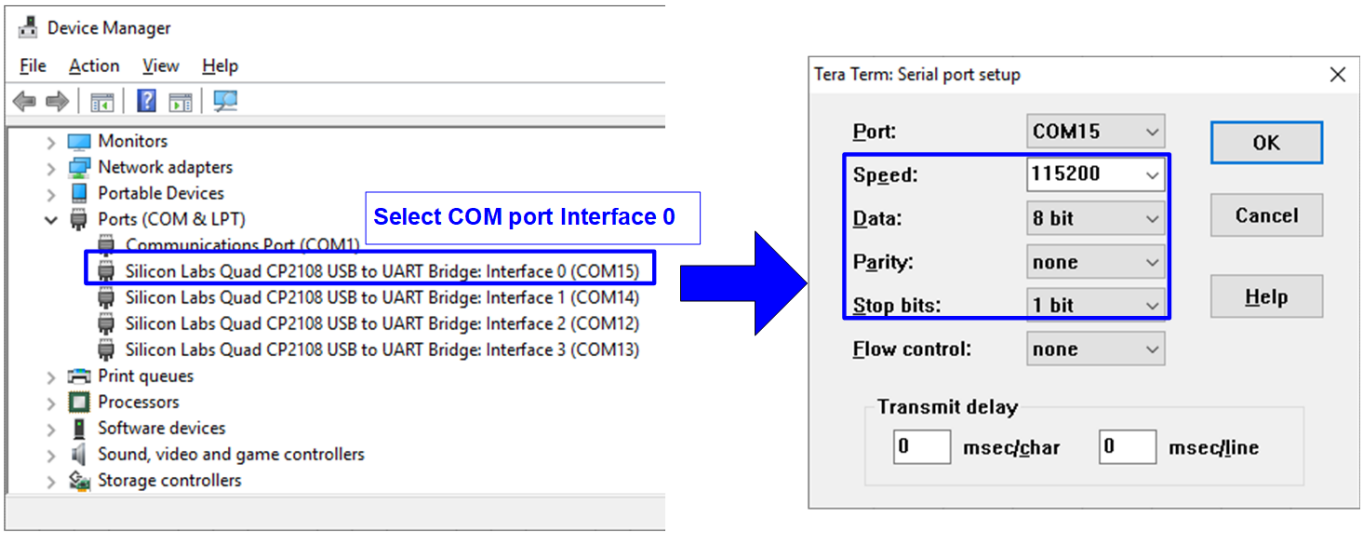

Figure 2-3 COM port number for Serial console

7) Download configuration file and firmware to FPGA board.
   i) Open Vivado TCL shell and change current directory to download folder which includes demo configuration file and command script file for download.
   ii) Type “ll10gemaclptest_zcu102.bat” to configure FPGA and download firmware, as shown in Figure 2-4.

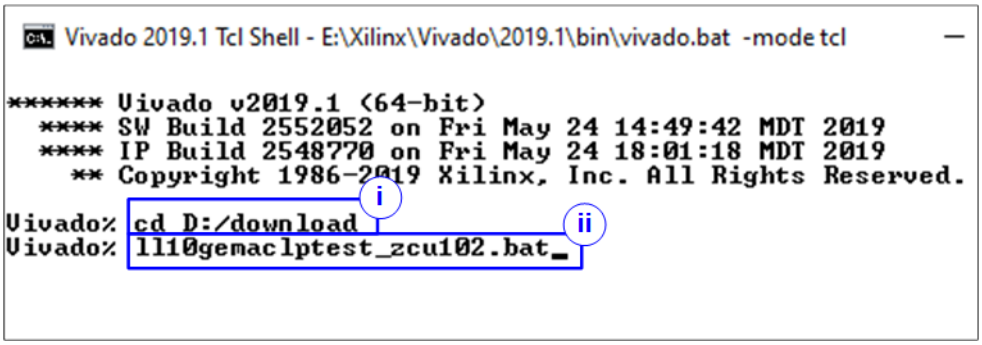

Figure 2-4 Example command script for download to ZCU102 by Vivado tool

8) On Serial console,
   i) Input '0' or '1' to initialize demo in external loopback mode or internal loopback mode.
   ii) After User select mode, the system initialization begins. The main menu is displayed on Serial console after the initialization is finished.

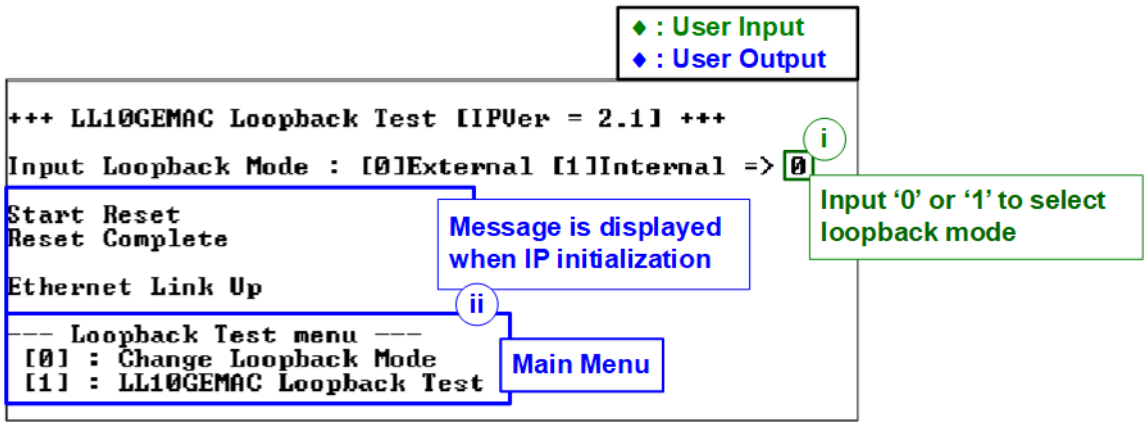

Figure 2-5 Main menu after system boot-up

Note: When running Internal loopback mode, SFP+ Loopback module is not used.

3 Revision History

Revision	Date	Description
1.0	29-Apr-21	Initial version release