Intel® Server D50DNP Family

Intel® Server Board D50DNP
Intel® D50DNP Modules
Intel® Server System D50DNP

Technical Product Specification

An overview of product features, functions, architecture, and support specifications.

Rev. 2.0

July 2023

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Document Revision History

Date	Revision	Changes
January 2023	1.0	Initial production release.
July 2023	1.1	• Updated Figure 74 60-mm System Fan Dimensions with correct dimensions • Added data for last two columns of Table 30. System Volumetric Airflow • Updated Thermal Tables in Appendix E with results of Silver units testing: • Added information about Intel® VROC support and software license key • Moved KVM function into BMC advanced features section • Removed support for Intel® Optane™ PMem 300 series modules • Added pictures of IEC C20 and C22 connectors to section 11.6.2 • Added Appendix I “Software License Key” • Corrected trademarked names (PCIe, NVMe and MCIO) to follow guideline • Added illustration for Intel® Xeon® Max CPU clip release mechanism • Updated Regulatory table in Appendix K with new certificates obtained • Added comment regarding system status LED behavior when power supply cold redundancy is disabled, and the power cord is unplugged (Page 70)
July 2023	2.0	• Reduced for AXG SDP DNP PVC PCIe program.

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Table of Contents

List of Figures

List of Tables

1. Introduction

The Intel® Server D50DNP Family includes products that support demanding high-performance computing (HPC) and artificial intelligence (AI) applications and workloads. The building blocks in the product family allow custom development of server systems using an Intel-developed server board or density-optimized Intel® D50DNP Modules.

The product family also includes fully integrated 2U rack mount, multi-module systems. The product family supports the 4th Gen Intel® Xeon® Scalable processors family or Intel® Xeon® CPU Max Series processors. Previous generations of Intel® Xeon® processor families are not supported.

This document will focus on the 2u Air Cooled PCIe Accelerator system. The original source of this document is located at: https://www.intel.com/content/www/us/en/content-details/783318/intel-server-d50dnp-family-technical-product-specification-1-1.html?wapkw=D50DNP%20TPS&DocID=783318 . The document is divided into two main parts. The first four chapters provide feature information about the server board, modules, and system. The remaining chapters provide information about the technologies behind these features.

Notes for this Document:

- The **Intel® D50DNP Modules** term refers to all module types supported by the **Intel® Server D50DNP Family**: **compute module**, **management module**, **Intel® Data Center GPU Max Series accelerator module**, and **PCIe* accelerator module**.
- The product name **Intel® Server D50DNP Family** refers to **Intel® Server Board D50DNP**, **Intel® D50DNP Modules**, and **Intel® Server System D50DNP**.
- The 4th Gen Intel® Xeon® Scalable processor family may be referred to simply as “processor”.
- DDR5 DIMMs are commonly referred to as “memory module”.
- This document includes several references to Intel websites where additional product information can be downloaded. However, these public Intel sites do not include content for products in development. Content for these products is available on the public Intel websites after their public launch.

1.1 Product Family Overview

The core products that define the high-performance, density-optimized Intel® Server D50DNP Family include:

- Intel® Server Board D50DNP1SB
- Intel® D50DNP Modules
- Intel® Server Systems D50DNP

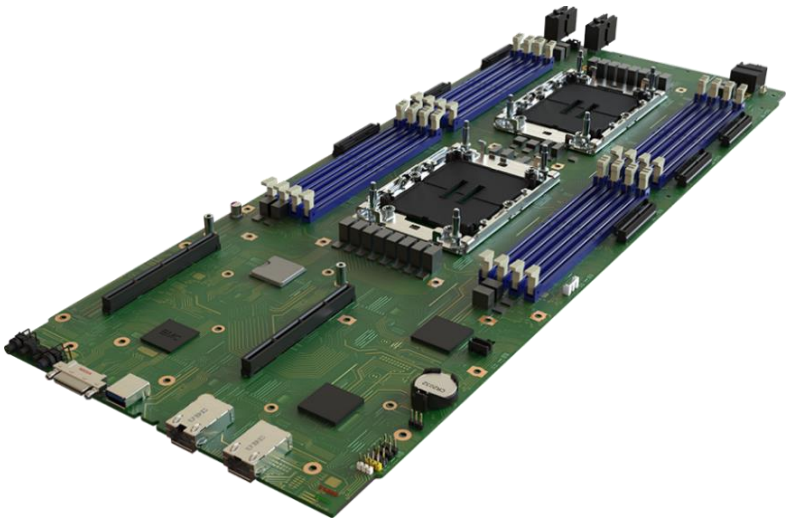


Figure 1. Intel® Server Board D50DNP1SB

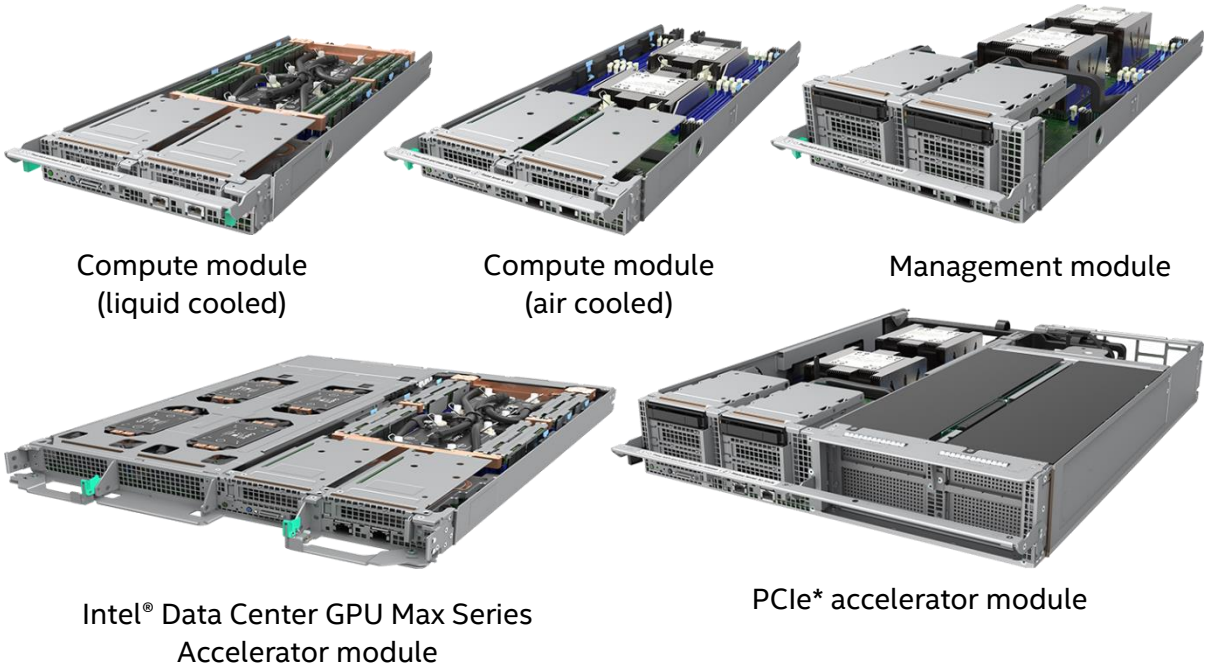


Figure 2. Intel® D50DNP Modules

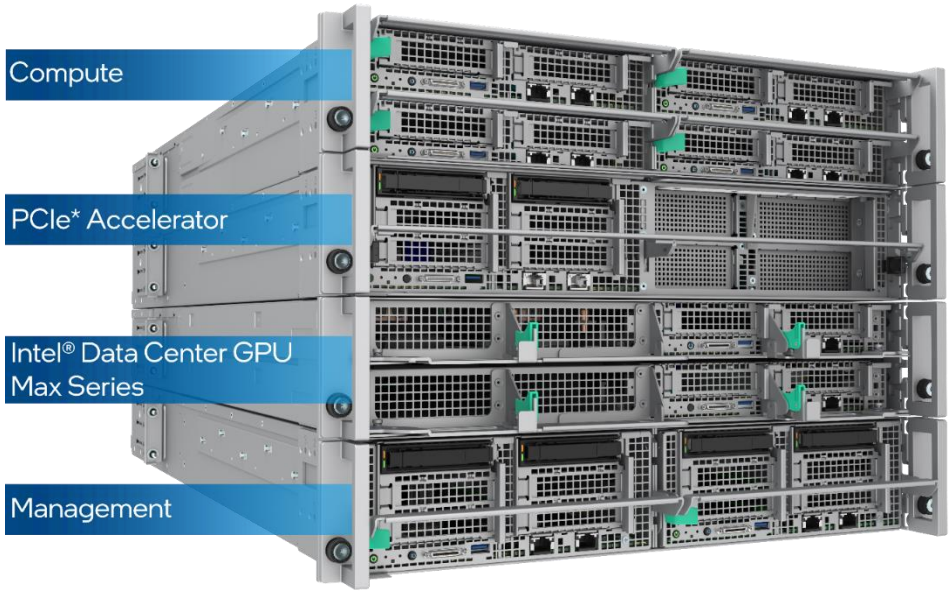


Figure 3. Intel® Server D50DNP Family

The following options are available for ordering the board, modules, and systems.

L3 = Server board building block option.
L6 = Modules building block option with an integrated Intel® Server Board D50DNP1SB. The base configuration is non-functional out of the box. Additional integration of chassis and components is required.
L9 = Fully integrated system. Pre-configured. Base configuration is power-on ready. No operating system is installed.

Important Note: Fully configured (operation ready, no operating system) L9 systems are only orderable from Intel using its online configure-to-order (CTO) tool at the Configure to Order Portal (Intel NDA required). Or contact an Intel field sales representative.

1.2 Reference Documents and Support Collaterals

For additional information, see the product support collaterals in the following table.

Table 1. Intel® Server D50DNP Family Reference Documents and Support Collaterals

Topic	Document Title or Support Collateral	Document Classification
Technical information about this product family	*Intel® Server D50DNP Family Technical Product Specification.*	Public
System integration instructions and service guidance	*Intel® Server D50DNP Family Integration and Service Guide.*	Public
Server configuration guidance and compatibility	*Intel® Server D50DNP Family Configuration Guide.*	Public
BMC technical information of product family	*Integrated Baseboard Management Controller Firmware External Product Specification (EPS). Document ID: 682839*	Intel Confidential
Information about the Integrated BMC Web Console	*Integrated Baseboard Management Controller Web Console (Integrated BMC Web Console) User Guide.*	Public
BIOS technical information of product family	*4th Gen Intel® Xeon® Scalable Processor Family BIOS Firmware External Product Specification.*	Public
BIOS setup utility information of product family	*Intel* Server Board D50DNP and M50FCP Family BIOS Setup Utility User Guide.*	Public
Base specifications for the IPMI architecture and interfaces	*Intelligent Platform Management Interface Specification Second Generation v2.0*	Public
Specifications for PCIe* interfaces	*PCIe Base Specification, Revision 3.0, Revision 4.0, Revision 5.0*	Public
TPM for PC Client specifications	*TPM PC Client Specifications, Revision 2.0*	Public
Specifications of 4th Gen Intel® Xeon® Scalable processor family	*Sapphire Rapids External Design Specification (EDS):* Document IDs: 630161, 612246, 612172, 633350, 611488	Intel Confidential
Processor design specifications and recommendations	*Eagle Stream Server and Fishhawk Falls Workstation Platforms Thermal Mechanical Specification (TMS)*: Document ID: 609847	Intel Confidential
BIOS and BMC Security Best Practices	*Intel® Server Systems Baseboard Management Controller (BMC) and BIOS Security Best Practices White Paper*	Public
Managing an Intel® Server Overview	*Managing an Intel® Server System 2020*	Public
Latest system software updates: BIOS and Firmware	*Intel® System Update Package (SUP) for Intel® Server D50DNP Family.*	Public
System update utility	*Intel® Server Firmware Update Utility and User Guide*	Public
To obtain full system information	*Intel® Server Information Retrieval Utility and User Guide*	Public
To configure, save, and restore various system options	*Intel® Server Configuration Utility and User Guide*	Public
Product Warranty Information	*Warranty Terms and Conditions*	Public
Intel® Data Center Manager (Intel® DCM) information	*Intel® Data Center Manager (Intel® DCM) Product Brief*	Public
	Intel® Data Center Manager (Intel® DCM) Console User Guide	Public

Note: Intel Confidential documents are made available under a nondisclosure agreement (NDA) with Intel and must be ordered through a local Intel representative.

2. Server Board Overview

This chapter provides an overview of the Intel® Server Board D50DNP1SB features and architecture. The server board is a purpose built, rack-optimized board ideal for use in HPC and AI applications. The architecture of the server board is developed around the features and functions of the 4th Gen Intel® Xeon® Scalable processor family and Intel® Xeon® CPU Max Series processors.

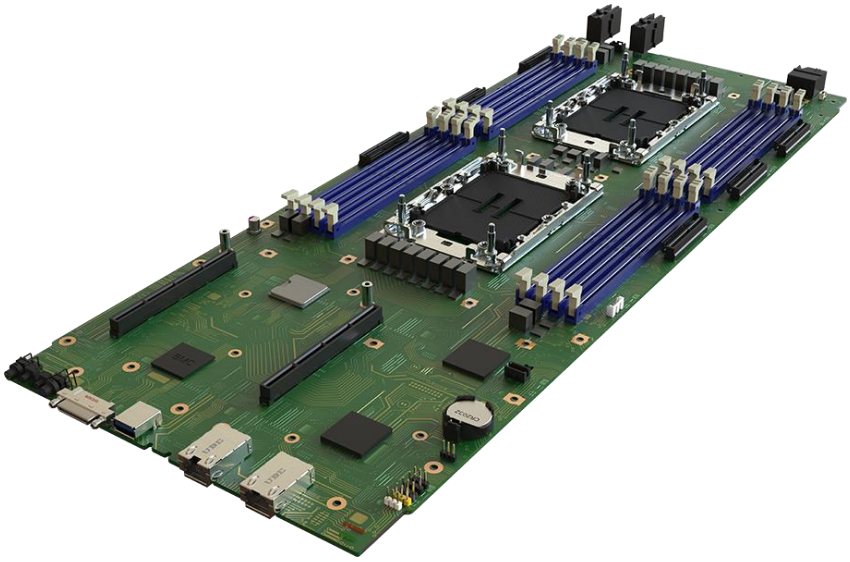


Figure 4. Intel® Server Board D50DNP1SB

2.1 Server Board Features Overview

See Table 2 for feature set specifications and Figure 5 for feature identification.

Table 2. Intel® Server Board D50DNP1SB Feature Set

Feature	Description
Processor Support	• Dual-socket E LGA4677 • 4th Gen Intel® Xeon® Scalable processors family SKUs: o Intel® Xeon® Platinum 84xx processor o Intel® Xeon® Gold 64xx processor o Intel® Xeon® Gold 54xx processor • Intel® Xeon® CPU Max Series processors • Intel® Ultra Path Interconnect (Intel® UPI) links: three at 16 GT/s (all processor SKUs) **Notes:** • Supported 4th Gen Intel® Xeon® Scalable processor SKUs must not end in “N” or “U”. All other processor SKUs are supported. • Previous generations of Intel® Xeon® processor and Intel® Xeon® processors Scalable families are not supported.
Maximum Processor Thermal Design Power (TDP)	• 4th Gen Intel® Xeon® Scalable processors up to 350 W (server board only). See Section 5.2. • Intel® Xeon® CPU Max Series processors up to 350 W (server board only). See Section 5.2. **Note:** The maximum supported processor TDP at the system level may be lower than what the server board can support. Supported power, thermal, and configuration limits of the chosen server chassis need to be considered to determine if the system can support the maximum processor TDP limit of the server board. Refer to the server chassis/system documentation for additional guidance.
PCH Chipset	• Intel® C741 chipset • Features enabled on this server board: o SATA III support o USB 3.0 support o PCIe* 3.0 support

Feature	Description
Memory Support	• Up to 16 DDR5 RDIMMs. See Chapter 6 for details. • Registered DDR5 DIMM (standard RDIMM, 3DS-RDIMM, and 9x4 RDIMM) **Note:** 3DS = three-dimensional stacking. • All DDR5 RDIMMs must support ECC • Up to 4800 MT/s memory data transfer rates • Up to 2 TB DDR5 memory capacity for both processors (1 TB per processor), for all processor SKUs • DDR5 standard voltage of 1.1 V **Note:** The supported memory speed depends on the installed processor. See Chapter 6 for details.
Video Support	• Integrated 2D video controller • 16 MB of DDR4 Memory • One VGA DE-15 external connector through I/O breakout cable
Front Panel Support	
I/O Ports	• One USB 3.0 port • One I/O breakout cable connector, supporting the following: o Two USB 3.0 port connectors (dual-stack) o One VGA connector o One serial port connector compliant with the Advanced Technology (AT) pinout specifications. **Note:** The I/O breakout cable is available as an accessory option (iPC **AXXCONNTDBG**).
Networking	• One external 10GBASE-T Ethernet port (RJ45) • One external 1000BASE-T Ethernet port (RJ45) dedicated to server management
LEDs	• Board status • Board ID
Buttons	• Power • Board ID • Cold reset • Non-maskable interrupt (NMI)
Expansion Options	
Riser Slots	Two riser slots are available to connect PCIe* add-in cards and storage devices. See module specific tables for riser options.
Supported Onboard Connectors and Headers	
Mini Cool Edge I/O (MCIO*) PCIe Interface Support	• Two MCIO connectors each with x16 PCIe 5.0 lanes are routed from CPU 0 • Four MCIO connectors each with x16 PCIe 5.0 lanes are routed from CPU 1
Security and Serviceability	
Security	Supported security technologies: • Intel® Platform Firmware Resilience (Intel® PFR) technology 3.0 • Intel® Total Memory Encryption – Multi-Key (Intel® TME-MK) Technology • Intel® Software Guard Extensions (Intel® SGX) Technology • Intel® Converged Boot Guard and Trusted Execution (Intel® CBnT) Technology • Trusted platform module 2.0 (China version) – iPC **AXXTPMCHNE8** (accessory option) • Trusted platform module 2.0 (rest of the world – iPC **AXXTPMENC9** (accessory option)
Server Management	• Integrated Baseboard Management Controller (BMC) based on the ASPEED* AST2600 Advanced PCIe Graphics and Remote Management Processor • Compliant with the Intelligent Platform Management Interface (IPMI) 2.0 • Compliant with Redfish* • Supports OpenBMC • Supports Intel® Data Center Manager (Intel® DCM) • Supports Intel® Server Debug and Provisioning Tool (Intel® SDP Tool) • One external 1000BASE-T Ethernet port (RJ45) dedicated to server management • Intel® Light-Guided Diagnostics included with onboard LEDs

Feature	Description
Onboard Configuration and Service Jumpers	• BIOS load defaults • BIOS password clear • Intel® Management Engine (Intel® ME) firmware force update • BIOS SVN downgrade • BMC SVN downgrade For more information, see Chapter 15.
BIOS	• Unified Extensible Firmware Interface (UEFI)-based BIOS (legacy boot is not supported)
Module Support	• D50DNP1MHCPAC • D50DNP1MHEVAC • D50DNP1MHCPLC • D50DNP2MHSVAC • D50DNP1MFALLC • D50DNP2MFALAC See Table 3 for more information on the Intel® D50DNP Modules.

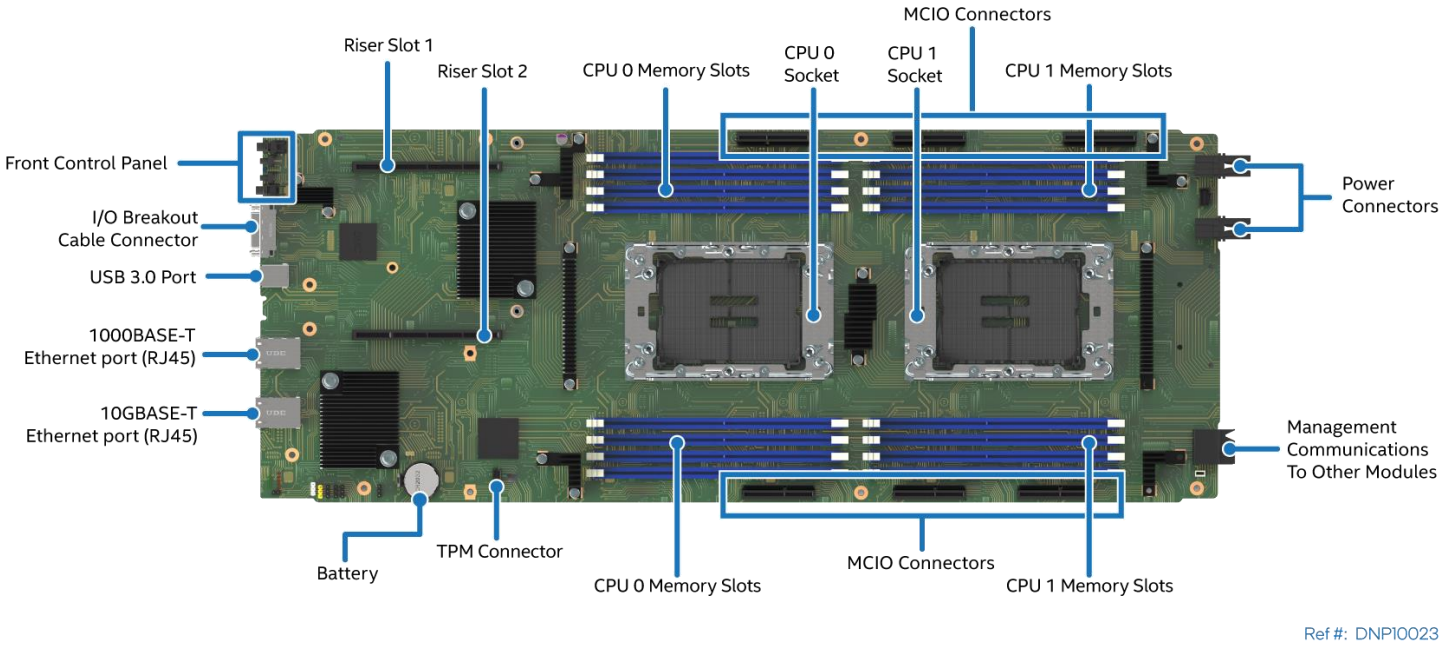


Figure 5. Intel® Server Board D50DNP1SB Feature Identification

2.2 PCI Express* (PCIe*)

The PCI Express (PCIe) interfaces originated from the CPUs are fully compliant with the *PCIe Base Specification, Revision 5.0.* supporting 32 GT/s. They are also backward compatible with the previous PCIe specifications, supporting the following bit rates: 16 GT/s (PCIe 4.0), 8.0 GT/s (PCIe 3.0), 5.0 GT/s (PCIe 2.0), and 2.5 GT/s (PCIe 1.0).

The PCIe interfaces routed from the platform controller hub (PCH) to the M.2 connectors are fully compliant with the *PCIe Base Specification, Revision 3.0*, supporting 8.0 GT/s. They are also backward compatible with the previous PCIe specifications, supporting the following PCIe bit rates: 5.0 GT/s (PCIe 2.0), and 2.5 GT/s (PCIe 1.0). For PCI Express details, see Chapter 7.

2.3 Server Board Architecture

The architecture of the Intel® Server Board D50DNP1SB is developed around the features and functions of the 4th Gen Intel® Xeon® Scalable processor family, Intel® C741 chipset PCH, Intel® Ethernet Controller X710-AT2, and the Aspeed AST2600* Server Management Processor (SMP).

The following figure provides an overview of the Intel® Server Board D50DNP1SB architecture, showing the features and interconnects of each of the major subsystem components.

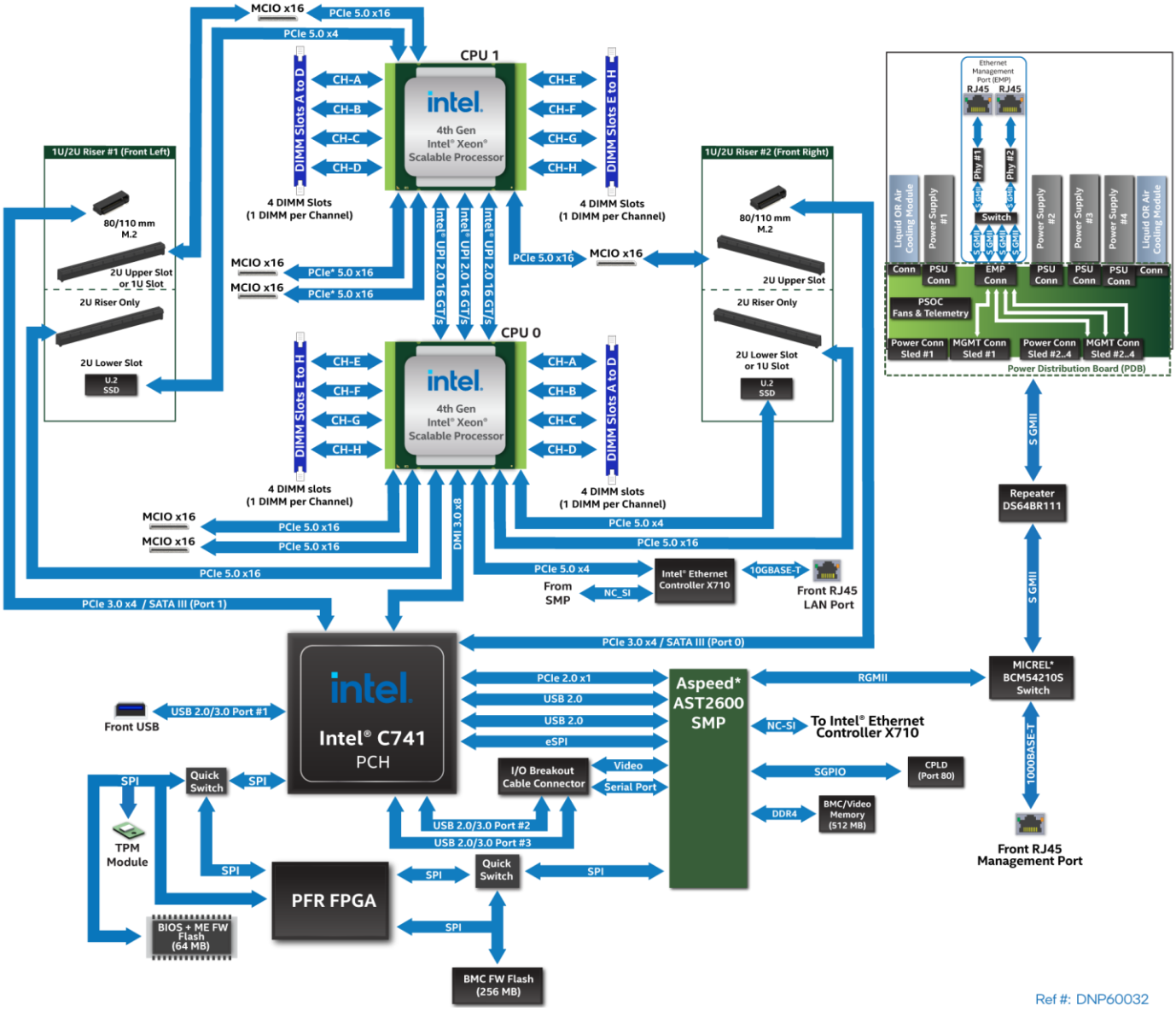


Figure 6. Intel® Server Board D50DNP1SB Architectural Block Diagram

2.4 Server Board Additional Information

Additional board-only information is in the following appendices.

- Mechanical dimension diagrams (see Appendix B)
- Server board mechanical drawings (see Appendix F)
- Server board installation and component replacement (see Appendix H)

Pinout definitions for server board connectors and headers are only made available by obtaining the board schematics directly from Intel (an NDA is required).

3. Intel® D50DNP Modules Overview

The Intel® Server D50DNP Family offers a variety of modules that address different workloads in today's modern data centers. From processor hungry workloads such as artificial intelligence (AI) accelerations and high-performance computing (HPC), Intel® D50DNP Modules are available to support each of these workload requirements. This chapter provides an overview of the functions and features of each module supported by the Intel® Server D50DNP Family.

Figure 7. Chassis with Empty Module Bay

Each module in a system operates independently from the others. The installed modules in a system chassis share resources like power and cooling. The following table describes the different ways in which an Intel® Server System D50DNP can be configured.

For additional information regarding configuration options, see the *Intel® Server D50DNP Family Configuration Guide*. For detailed information on thermal limitations, see Appendix E.

Table 3. Intel® D50DNP Modules

Module Type	iPC	Height	Width	Cooling	Maximum Processor Thermal Design Power (TDP)	Modules per Chassis
PCIe* Accelerator	D50DNP2MFALAC	2U	Full width	Air Cooled	350 W	One

For mixed module configurations, the customer must consider the lowest ambient temperature required by the installed processors in the modules. The module requiring the lowest ambient temperature will define the ambient requirements for the whole system even if other installed modules allow higher ambient temperature.

The Intel® Server Board D50DNP1SB is the heart of the modules in the product family, supporting 4th Gen Intel® Xeon® Scalable processors and Intel® Xeon® CPU Max Series processors. Each module type supports a different feature set in terms of type of cooling, storage options, memory options, and PCIe* add-in card support. The following subsections provide details about the differentiation that each module provides.

3.1 2U PCIe* Accelerator Module

The PCIe accelerator modules are 2U, full-width modules intended to address acceleration solutions. An acceleration solution is comprised of the compute module on one side of the chassis, and up to four add-in cards (used to accelerate a specific workload) on the other side of the chassis. Refer to the Tested Hardware and Operating Systems List for details on supported add-in cards. The PCIe accelerator modules are air-cooled.

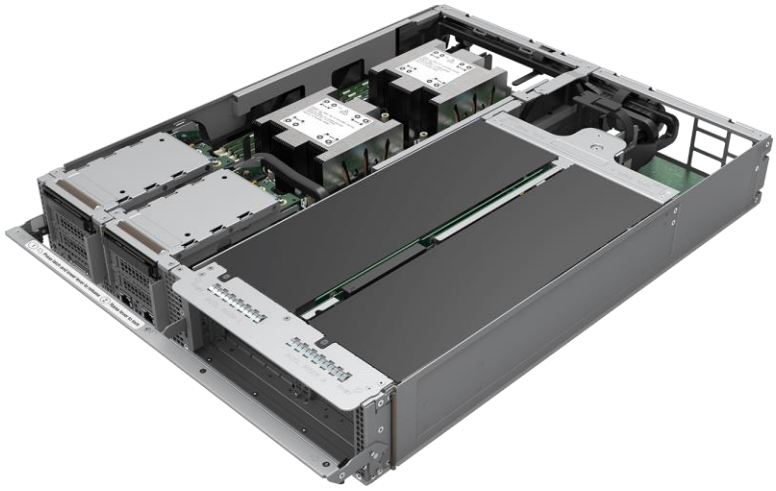


Figure 8. Air-Cooled 2U PCIe* Accelerator Module

The PCIe accelerator module supports up to eight PCIe add-in cards. Two riser assemblies support four low profile x16 PCIe add-in cards and two additional accelerator riser cards support four full length / full height, double width X16 PCIe add-in cards. The following figure shows the front view of the accelerator riser card 1.

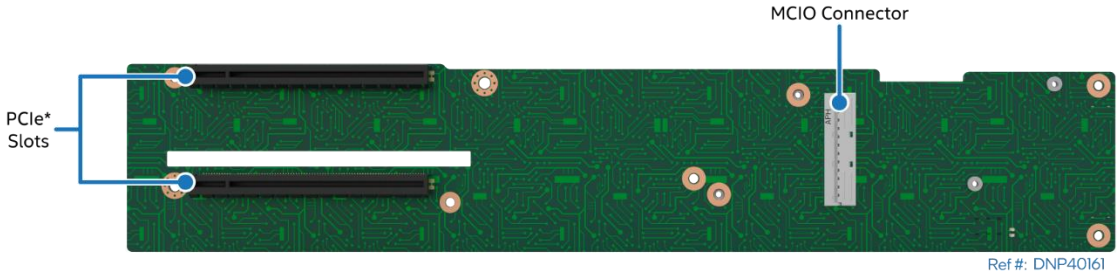


Figure 9. 2U PCIe Accelerator Module Riser Card 1 – Front View

The accelerator riser cards have MCIO* connectors that are cabled to the MCIO connectors on the server board.

The following types of add-in cards are supported in the accelerator riser card slots:

- Nvidia* Tesla* A100
- Programmable acceleration card with the Intel® Stratix® 10 SX FPGA
- Intel® Data Center GPU Max Series-based PCIe x16 add-in card
- Intel® Ethernet Network Adapter E810 Series

Note: Mixing types of PCIe cards in a single module is not supported.

All four PCIe add-in cards are connected directly to the server system power supplies using a power connector board. The power connector board contains a spare power connector for add-in cards. The same power connector board also supplies the power to the two accelerator riser cards. The following figure shows the power connector board in the 2U accelerator module.

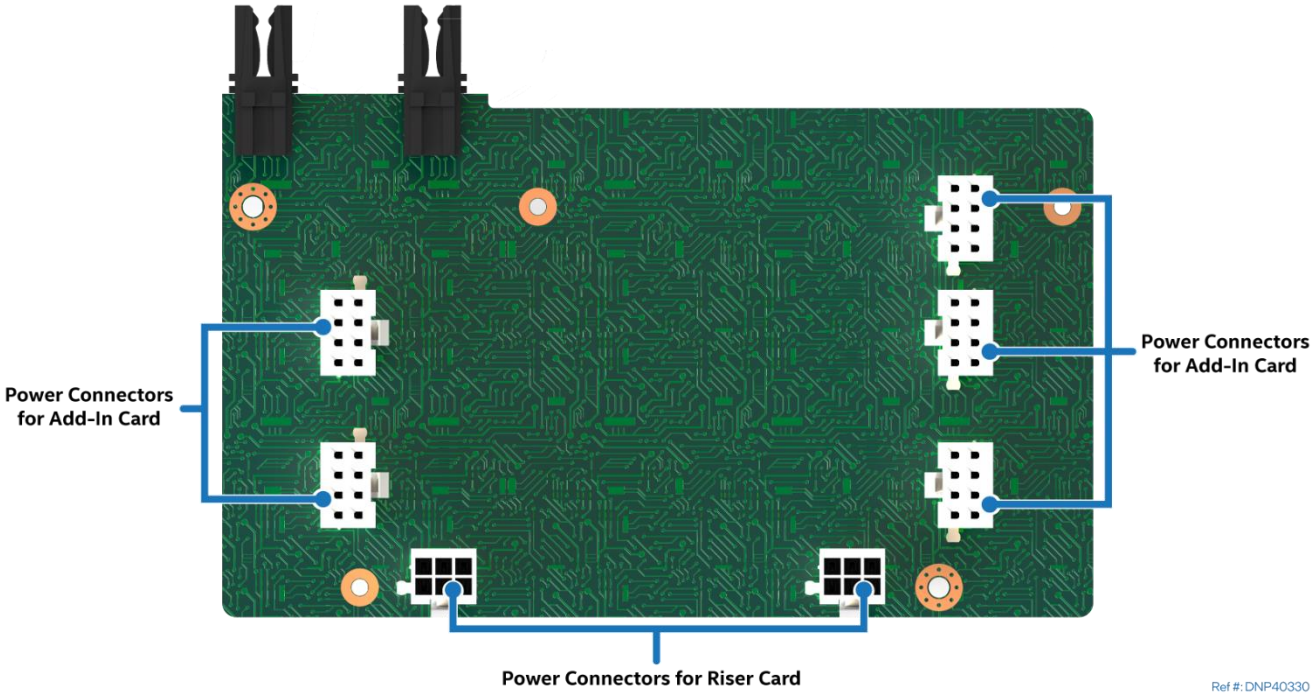


Figure 10. Power Connector Board for 2U PCIe* Accelerator Module

The PCIe accelerator modules include the Intel® Server Board D50DNP1SB with support for dual 4th Gen Intel® Xeon® Scalable processors and up to 16 DDR5 DIMMs.

Each module includes two 2U riser cards. Unlike 1U riser cards, where two types of cards are available, the 2U riser cards are of the same type. They can go interchangeably in the riser slot 1 or riser slot 2 on the server board. The 2U riser card has a Mini Cool Edge I/O (MCIO*) connector that is cabled to the MCIO connector on the server board routed from CPU1.

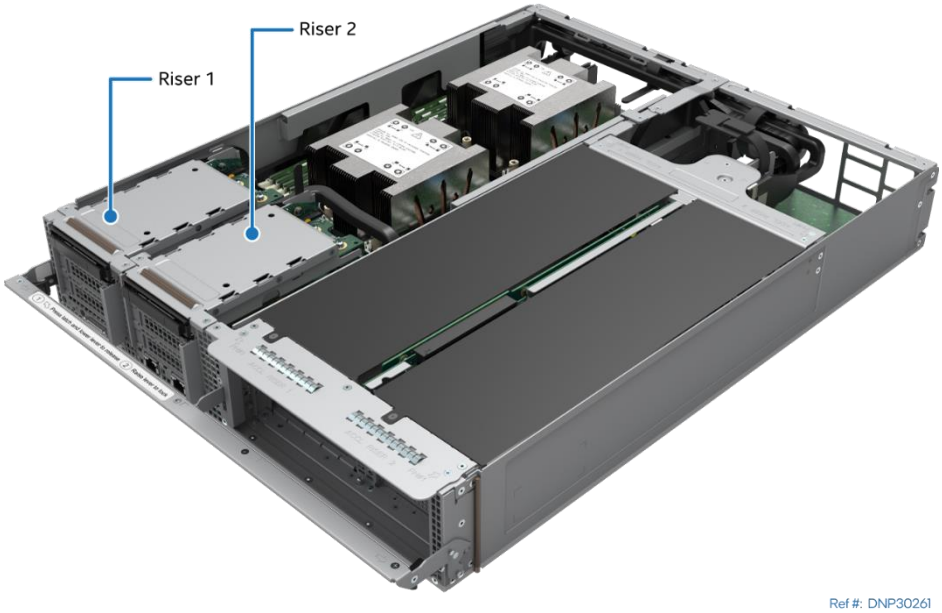


Figure 11. Riser Slot 1 and Riser Slot 2 in the 2U PCIe Accelerator Module

Each of the two 2U riser card assemblies have:

- Two PCIe* 5.0 slots (x16 electrical, x16 mechanical) compatible with low-profile PCIe add-in cards and a maximum power of 25 W for each slot. PCIe* lanes for the lower slot are routed from CPU0. PCIe lanes for the upper slot are routed from CPU1.
- One M.2 connector supporting 80/110-mm PCIe or SATA SSD storage device.
- One slot for 2.5" U.2 hot-swappable NVMe* SSD drive connected to the riser card via U.2 adapter card
- One MCIO* connector to route PCIe lanes from CPU1 via MCIO cable

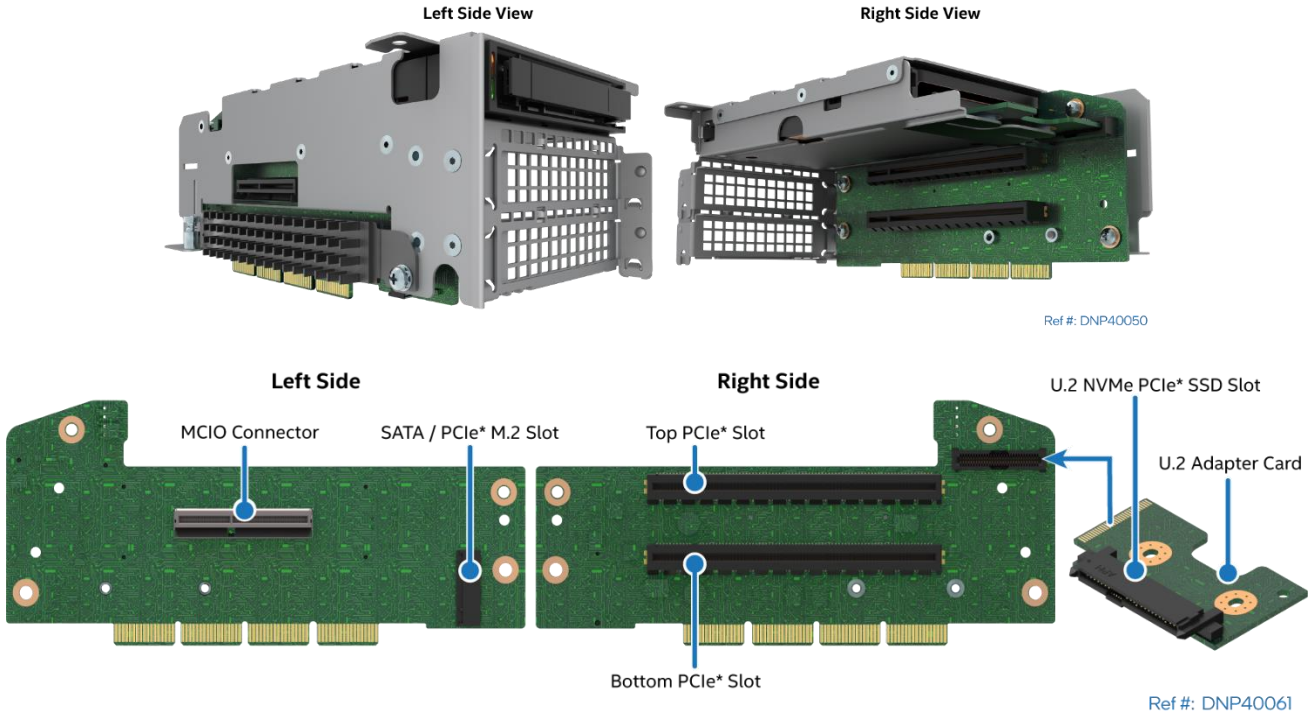


Figure 12. 2U Riser Card Assembly

3.1.1 2U PCIe* Accelerator Module Specific Features

Intel® Server Board D50DNP1SB defines many characteristics of the modules. The table below shows PCIe* accelerator module specific characteristics only. Refer to Table 2 for common family features.

Table 4. PCIe Accelerator Module Specific Features

Feature	Description
Maximum Processor TDP	• Up to 350 W. • See Appendix E for details.
Riser Slots	**Riser Slot 1 supports 2U dual PCIe slot riser card assembly (iPC DNP2UMRISER)** • with two PCIe 5.0 x16 slots, each supporting one low profile PCIe add-in card. • PCIe lanes for the bottom slot are routed from CPU 0. • PCIe lanes for the top slot are routed from the CPU 1 through an MCIO* cable. • PCIe lanes for the U.2 SSD are routed from the CPU 1. **Riser Slot 2 supports 2U dual PCIe slot riser card assembly (iPC DNP2UMRISER)** • with two PCIe 5.0 x16 slots, each supporting one low profile PCIe add-in card. • PCIe lanes for the bottom slot are routed from CPU 0. • PCIe lanes for the top slot are routed from the CPU 1 through an MCIO cable. • PCIe lanes for the U.2 SSD are routed from the CPU 0. • The PCIe slots in 2U riser cards provide up to 25 W of power.

Feature	Description
Accelerator Riser Slots	**Riser Slot 1 supports 2U full-length, dual PCIe* slot riser card assembly (iPC DNPACCLRISER1)** • With two full-height, full-length, double-width PCIe 5.0 (x16 mechanical, x16 electrical) slots routed from CPU 0 through MCIO* cable **Riser Slot 2 supports 2U full-length, dual PCIe slot riser card assembly (iPC DNPACCLRISER2)** • With two full-height, full-length, double-width PCIe 5.0 (x16 mechanical, x16 electrical) slots routed from CPU 1 through MCIO cable
Storage Support	**Via riser assemblies:** • Each 2U riser can accommodate one SATA or PCIe 3.0 NVMe* 80/110mm M.2 SSD drive. SATA and PCIe lanes are routed from the Intel® C741 chipset. • Each 2U riser assembly can accommodate one 2.5" U.2 NVMe SSD. • PCIe lanes routed from processor/chipset support Intel® VMD and Intel® VROC 8.0 (NVMe-based RAID). VROC support requires installation of the Intel® VROC license key (accessory option, iPC **VROCSTANKEY**).

3.1.2 2U PCIe Accelerator Module Feature Identification

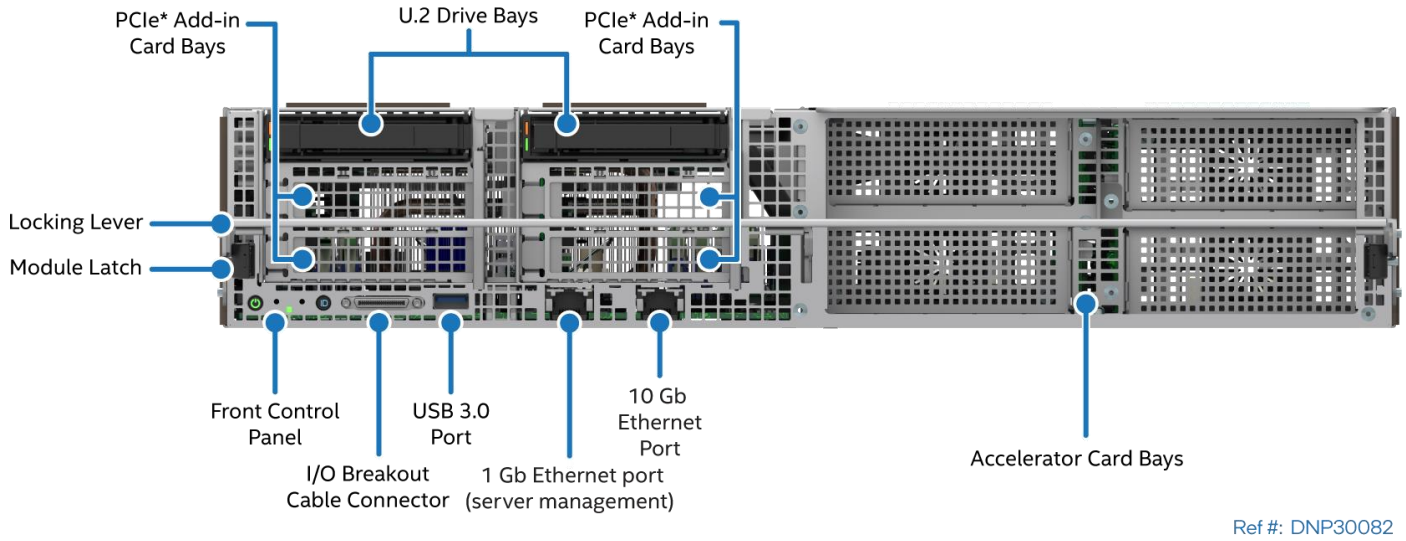


Figure 13. 2U PCIe Accelerator Module Front Panel Features

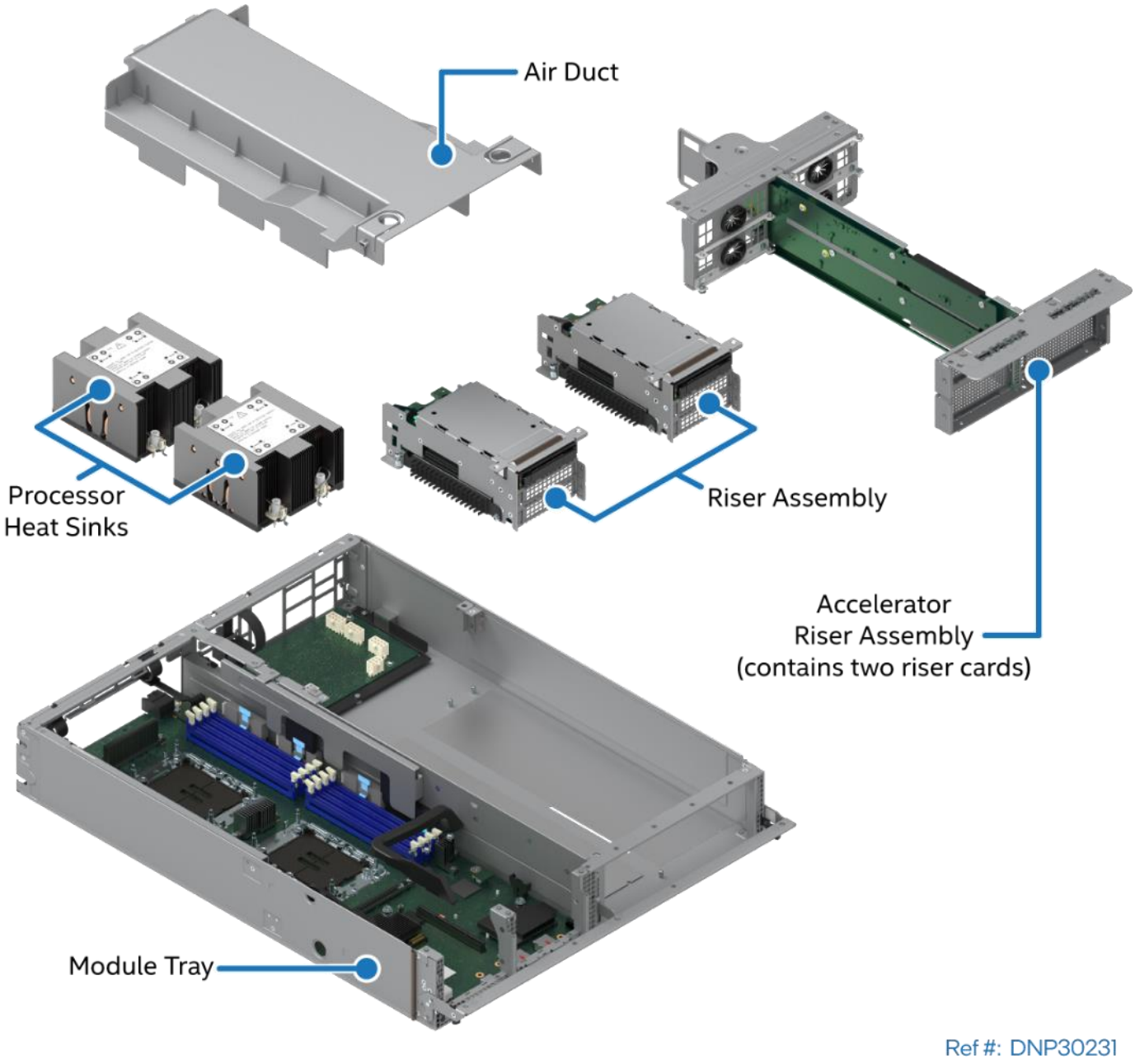


Figure 14. 2U PCIe* Accelerator Module Components

4. System / Chassis Overview

This chapter provides an overview of the system and chassis features, dimensions, and environmental and packaging specifications.

4.1 System / Chassis Features

The Intel® Server D50DNP Family offers options for custom configuration and self-integration of fully configured and integrated power-on ready system solutions. The following options are available:

- An Intel® Server Board D50DNP1SB building block option. (L3 integration level)
- A module building block option with integrated Intel® Server Board D50DNP1SB. The base configuration is non-functional out of the box. Additional integration of components like is memory, storage and network components and chassis is required. (L6 integration level).
- A fully integrated and pre-configured system including chassis, modules, power supplies, cooling components, and rails for rack or cabinet mounting. Base configuration is power-on ready. No operating system is installed. (L9 integration level).

The Intel® Server D50DNP Family offers air-cooled systems. See the *Intel® Server D50DNP Family Configuration Guide* for a complete list of available options.

As a building block, the Intel® Server D50DNP Family includes this Intel® Server Chassis FC2000 v2 products:

- 2U full-width configuration, air cooled – iPC **FC2FAC27W0**
  - Supports one 2U full-width air cooled module

Note: Power supply units (PSUs) are sold separately.

See Table 5 for a feature list of system and chassis-only features.

Table 5. Intel® Server Chassis / Intel® Server System D50DNP Feature Set

Feature	Description			
	Chassis SKU iPC FC2HLC30W0	**Chassis SKU iPC FC2FLC30W0**	**Chassis SKU iPC FC2HAC27W0**	**Chassis SKU iPC FC2FAC27W0**
Chassis Definition	FC2000 half-width configuration, liquid cooled	FC2000 full-width configuration, liquid cooled	FC2000 half-width configuration, air cooled	FC2000 full-width configuration, air cooled
Chassis Type	2U, rack-mount, multi-module			2U rack-mount, single module
Chassis Dimensions	• 865 x 442 x 86.8 mm			
Packaging Dimensions	• 1192 x 758 x 317 mm (L x W x H)			
Supported Intel® D50DNP Modules	• Up to four 1U half-width modules (liquid cooled)	• Up to two 1U Intel® Data Center GPU Max Series Accelerator full-width modules (liquid cooled)	• Up to four 1U half-width modules (air cooled) • One 2U half-width module and two 1U half-width modules (air cooled) • Up to two 2U half-width modules (air cooled)	• One PCIe* accelerator module 2U full-width (air cooled)

Feature	Description			
	Chassis SKU iPC FC2HLC30W0	**Chassis SKU iPC FC2FLC30W0**	**Chassis SKU iPC FC2HAC27W0**	**Chassis SKU iPC FC2FAC27W0**
Cooling	**Liquid-cooled configurations:** • Liquid-cooling loop (per module) • Liquid-cooling plumbing connections on the back of the chassis • Two 40 x 40 x 40 mm fans		**Air-cooled configurations:** • Eight dual-rotor hot-swap system fans with support for fan redundancy o Four 60 x 60 x 56 mm fans o **Important Note:** Only install 60-mm system fans that are designed for the Intel® Server Chassis D50DNP (iPC **FCXX60MMACFAN**). Do not install 60-mm system fans from previous Intel server product generations. o Four 40 x 40 x 40 mm fans • One 40-mm fan per installed power supply unit (PSU)	
Power	Supports four 3000 W AC liquid-cooled power supplies with power redundancy support (dependent on system configuration). PSUs are sold separately.		Supports four 2700 W AC power supplies with power redundancy support (dependent on system configuration). PSUs are sold separately.	
Rack Mount Kit (FCXXRAILKIT)	• Tool-less installation • Fixed position **Note:** Rack mount kit is included with the chassis.			
Serviceability	Modular chassis features for simplified serviceability: • Fully independent Intel® D50DNP Modules • Hot-swap power supplies • Hot-swap system fans • Hot-swap U.2 solid state drive (SSD) storage (2U Intel® D50DNP Modules)			
Operating Temperature	10–35 °C ambient temperature			
Server Management	Optional Ethernet Management Port (EMP) that allows to aggregate management ports on each module and daisy-chain chassis to minimize number of cables.			

4.2 System Feature Identification

All systems are designed to insert modules from the front. The following illustrations provide system views for all supported system configurations.

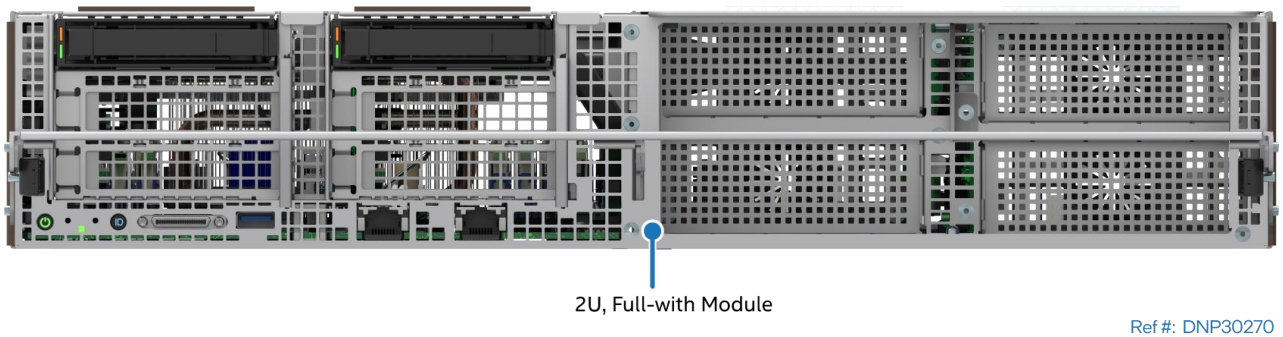


Figure 15. One Full-Width Module System Configuration Chassis – iPC FC2FAC27W0

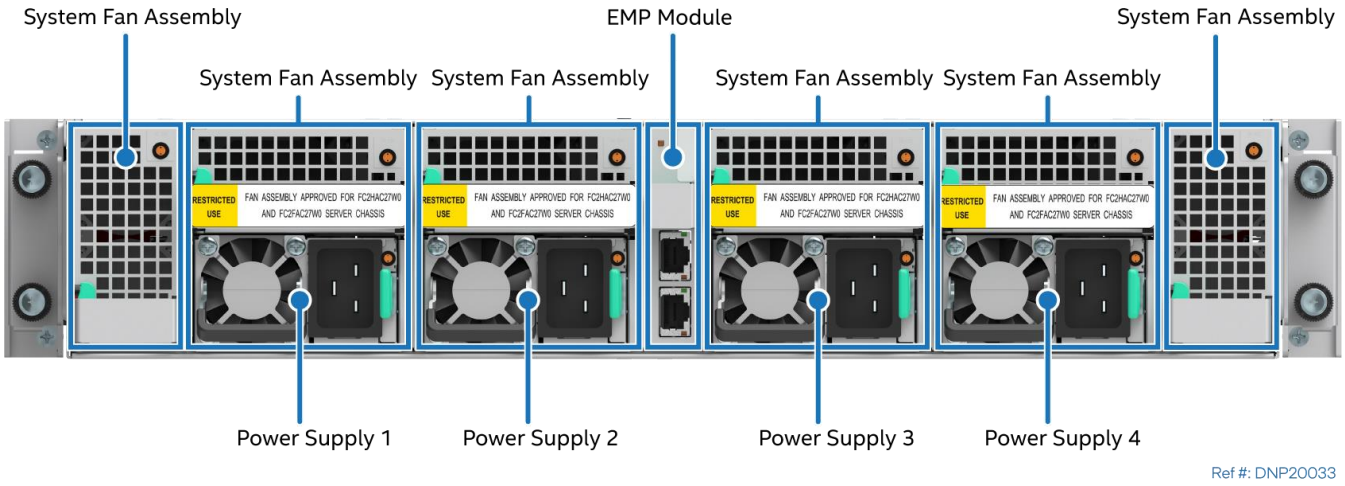


Figure 16. Air-Cooled System Rear View

4.3 Rack and Cabinet Mounting Kit

The Intel® Server System D50DNP supports a fixed rail kit for installation into a four-post rack or cabinet. Features and specifications for the rail kit are:

- iPC **FCXXRAILKIT** – Fixed rail kit
  - Tool-less installation
  - Maximum supported weight: 150 kg (330 lbs.)

Safety Note: Due to the weight of a fully configured system, Intel recommends the following: Use a mechanical lift to aid with the installation of the system into the rack, and/or involve at least two people to install the system into the rack. Another option is to remove all installed modules from the system before attempting to install the system into a rack or cabinet.

4.4 System / Chassis Level Environmental Limits

The following table defines the system level operating and non-operating environmental limits.

Table 6. System Environmental Limits Summary

Parameter		Limits
Temperature	Operating	ASHRAE Class A2: Continuous operation. 10–35 °C (50–95 °F) with the maximum rate of change not to exceed 10 °C per hour. ASHRAE Class A3: Includes operation up to 40 °C for up to 900 hrs. per year.[1] ASHRAE Class A4: Includes operation up to 45 °C for up to 90 hrs. per year.[1]
	Non-operating	-40 through 70 °C (-40 through 158 °F)
Altitude	Operating	Support operation up to 3050 m with ASHRAE class de-ratings
Humidity	Shipping	50% to 90%, non-condensing with a maximum wet bulb of 28 °C (at temperatures 25–35 °C)
Shock	Operating	Half sine, 2 g, 11 msec
	Unpackaged	Trapezoidal, 25 g, velocity change is based on packaged weight
	Packaged	ISTA (International Safe Transit Association) Test Procedure 3A 2018
Vibration	Unpackaged	5–500 Hz, 2.20 g RMS random
	Packaged	ISTA (International Safe Transit Association) Test Procedure 3A 2018

Parameter		Limits		
Input Power	Voltage	200–240 V AC		
	Frequency	47–63 Hz		
	Source interrupt	No loss of data for power line drop-out of 12 msec		
	Surge non-operating and operating	Unidirectional		
	Line to earth only	AC Leads 2.0 kV I/O Leads 1.0 kV DC Leads 0.5 kV		
ESD	Air discharged	12.0 kV		
	Contact discharge	8.0 kV		
Sound Power Measured at (23 °C ±2 °C)	Workload	idle	medium	high
	$L_{WA,m}$ $L_{WA,c}$	6.6 BA 7.0 BA	7.7 BA 8.1 BA	8.5 BA 8.9 BA

Note 1: For system configuration requirements and limitations, see Appendix E in this document and refer to the online power calculator tool accessible at the following Intel web site: https://servertools.intel.com/tools/power-calculator/.

Disclaimer: Intel server boards contain and support several high-density VLSI and power delivery components that need adequate airflow to cool and remain within their thermal operating limits. Intel ensures through its own chassis development and testing that when an Intel server board and Intel chassis are used together, the fully integrated system meets the thermal requirements of these components.

It is the responsibility of the system architect or system integrator who chooses to develop their own server system using an Intel server board and a non-Intel chassis, to consult relevant specifications and datasheets to determine thermal operating limits and necessary airflow to support the intended system configurations and workloads when the system is operating within target ambient temperature limits.

It is also their responsibility to perform adequate environmental validation testing to ensure reliable system operation. Intel cannot be held responsible if components fail or the server board does not operate correctly when published operating and nonoperating limits are exceeded.

4.5 System / Chassis Packaging

The original Intel packaging provides protection to a fully configured system and is tested to meet the International Safe Transit Association (ISTA) Test Procedure 3A (2018). The packaging is designed to be reused for shipment after system integration has been completed.

The original packaging includes two layers of boxes (an inner box and outer shipping box) and various protective inner packaging components. The boxes and packaging components function together as a protective packaging system.

When reused, all of the original packaging materials must be used, including both boxes and each inner packaging component. In addition, all inner packaging components must be reinstalled in the proper location to ensure adequate protection of the system for subsequent shipment.

Notes:

- The design of the inner packaging components does not prevent improper placement in the packaging assembly. Only one correct packaging assembly allows the package to meet the ISTA Test Procedure 3A (2018) limits. See the *Intel® Server D50DNP Family Integration and Service Guide* for complete packaging assembly instructions.
- Failure to follow the specified packaging assembly instructions may result in damage to the system during shipment.

- **External dimensions for outer shipping box:**
  - Length: 46.93″ (1192 mm)
  - Breadth: 29.84″ (758 mm)
  - Height: 12.48″ (317 mm)
- **Internal dimensions for inner box:**
  - Length: 46.38″ (1178 mm)
  - Breadth: 29.29″ (744 mm)
  - Height: 11.38″ (289 mm)

5. Processor Support

As part of the Intel® Server D50DNP Family, the Intel® Server Board D50DNP1SB includes two E LGA4677 processor sockets compatible with the 4th Gen Intel® Xeon® Scalable processors family or Intel® Xeon® CPU Max Series processors. This chapter provides information on processor heat sinks, thermal design power (TDP), and population rules. The chapter also provides a processor family overview.

Note: Previous-generation Intel® Xeon® processors and Intel® Xeon® Scalable processors families, including their supported processor heat sinks, are not compatible with the server board described in this document.

5.1 Processor Cooling Overview

The server board includes two processor socket assemblies, each consisting of a processor socket and bolster plate. The factory-installed bolster plate is secured to the server board and is used to align the processor cooling hardware over the processor socket and secure it to the server board.

Processor cooling options in a server system may use a passive heat sink that use airflow to dissipate heat generated by the processors.

For air-cooled systems, the processor and heat sink are generally preassembled into a single processor heat sink module (PHM) before being installed onto the processor socket assembly. The PHM concept reduces the risk of damaging pins in the processor socket during the processor installation process.

A PHM assembly consists of a processor, a processor carrier clip, and the processor heat sink. The following figure identifies each component associated with the PHM and processor socket assembly (1U heat sink is shown in the figure).

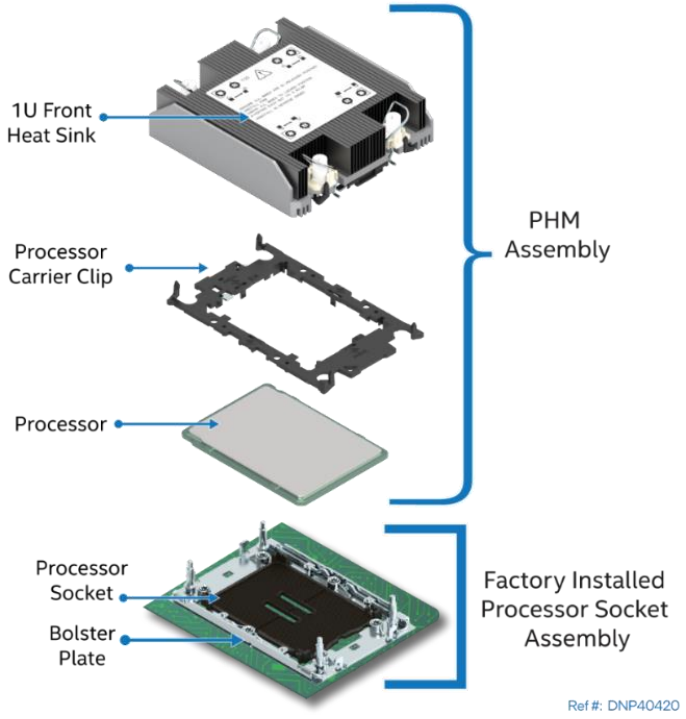


Figure 17. PHM Components and Processor Socket Reference Diagram

Note: For detailed processor assembly and installation instructions, see the *Intel® Server D50DNP Family Integration and Service Guide*.

5.1.1 Processor Cooling Requirements

For the server system to support optimal operation and long-term reliability, the thermal management solution of the selected server chassis and module must dissipate the heat generated in the chassis to keep the processors and other system components within their specified thermal limits.

For optimal operation and long-term reliability, processors in the 4th Gen Intel® Xeon® Scalable processor family or Intel® Xeon® CPU Max Series processors must operate within their defined minimum and maximum case temperature (T_{CASE}) limits. Refer to the *Sapphire Rapids Thermal and Mechanical Specifications and Design Guide (TMSDG)* for additional information concerning processor thermal limits.

Note: It is the responsibility of the system and components architects to ensure compliance with the processor thermal specifications. Compromising processor thermal requirements impacts the processor performance and reliability.

For air-cooled heat sink solutions, see the following section.

5.1.2 Processor Heat Sink (Air Cooled)

The Intel® Server D50DNP Family supports 1U height heat sinks and 2U height heat sinks as shown in the following figures. The compute module uses 1U height heat sinks. The management module and accelerator module use 2U height heat sinks.

As the following figures show, two types of 2U heat sinks and three types of 1U heat sinks are available: front heat sink, back heat sink, and enhanced volume air cooling (EVAC) heat sink (front position only). The front heat sink type is used for CPU 0 and the back heat sink type is used for CPU 1. The exploded views in the figures show the difference. The back heat sink types have more heat venting fins.

Note: Heat sinks are not interchangeable. The descriptions above must be followed.

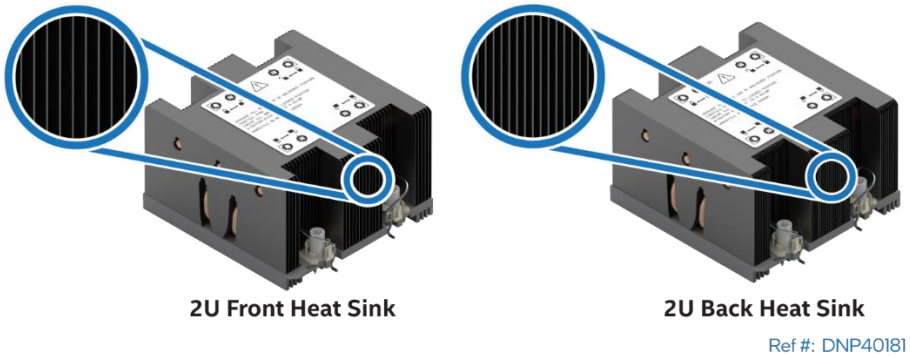


Figure 18. 2U Supported Processor Heat Sinks

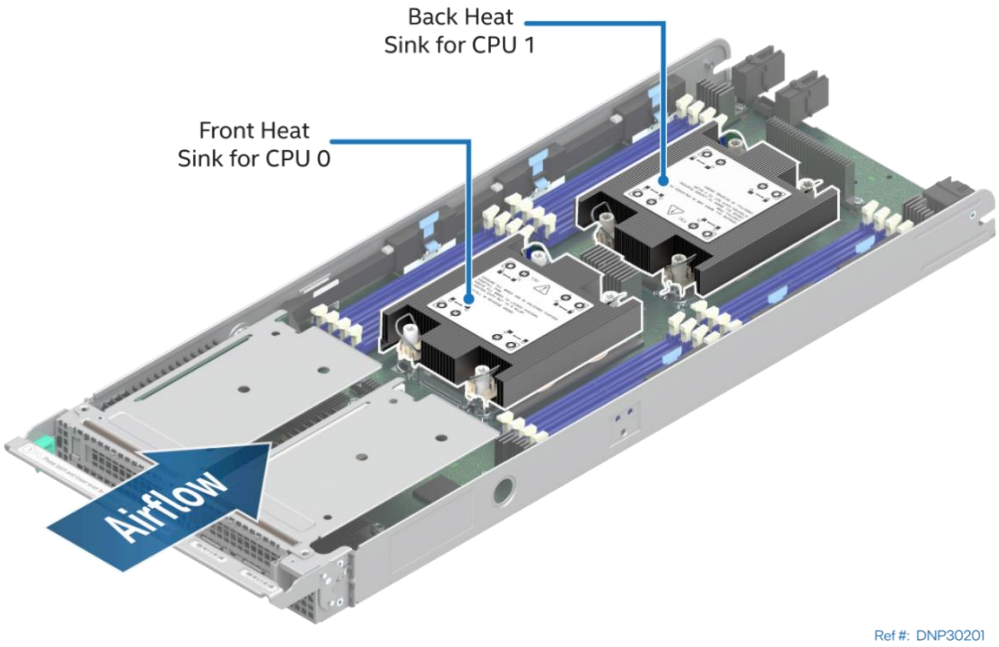
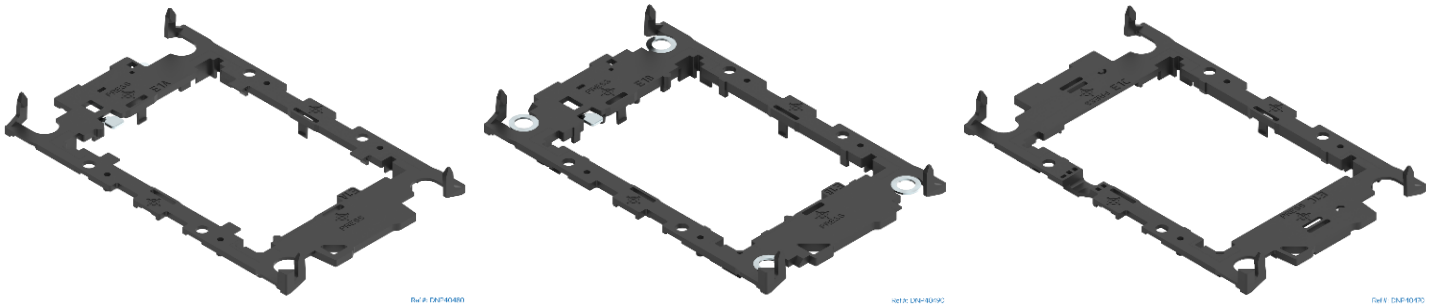


Figure 19. 1U Heat Sinks Installed in Module

5.1.3 Processor Carrier Clips

Two carrier clips are available for the 4th Gen Intel® Xeon® Scalable processor family and one for Intel® Xeon® CPU Max Series processors family (see Figure 20). The choice of carrier clip depends on the processor type.

- 4th Gen Intel® Xeon® Scalable processor family XCC models use the E1A carrier clip.
- 4th Gen Intel® Xeon® Scalable processor family MCC models use the E1B carrier clip.
- Intel® Xeon® CPU Max Series processor family models use the E1C carrier clip.



Carrier Clip E1A | Carrier Clip E1B | Carrier Clip E1C

Figure 20. Processor Carrier Clips

The carrier clip designation (E1A, E1B, or E1C) is marked on each carrier clip. The designation for the needed carrier clip is also marked on each processor package. The heat sinks for the Intel® Server D50DNP Family are compatible with all three carrier clips.

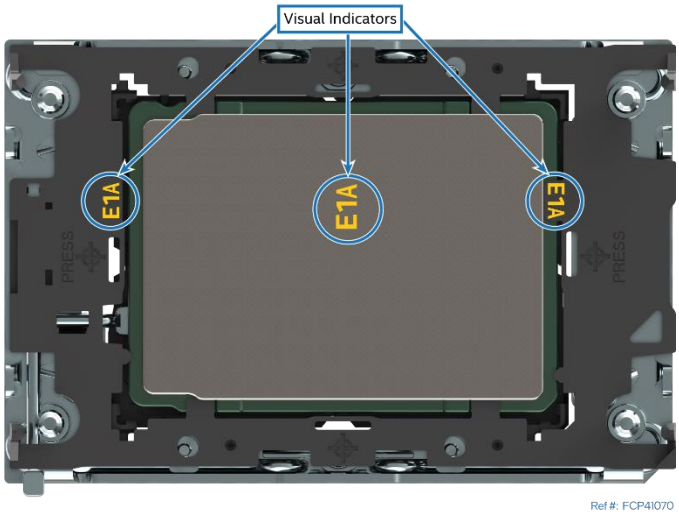


Figure 21. Processor Carrier Clips Identifier Markings

5.2 Processor Thermal Design Power (TDP) Support

Electrically, the Intel® Server Board D50DNP1SB supports processors in the 4th Gen Intel® Xeon® Scalable processor family or Intel® Xeon® CPU Max Series with a maximum thermal design power (TDP) of 350 W.

Note: The maximum supported processor TDP at the system level may be lower than what the server board can support. Supported power, thermal, and configuration limits of the chosen server chassis / system need to be considered to determine if the system can support the maximum processor TDP limit of the server board or not. Refer to the chosen server chassis/system documentation for additional processor support guidance.

Depending on the system module and configuration, the Intel® Server System D50DNP may support a TDP up to and including 350 W. For details, see Appendix E.

5.3 Processor Family Overview

The supported 4th Gen Intel® Xeon® Scalable processor family processor shelves are identified as shown in the following figure.

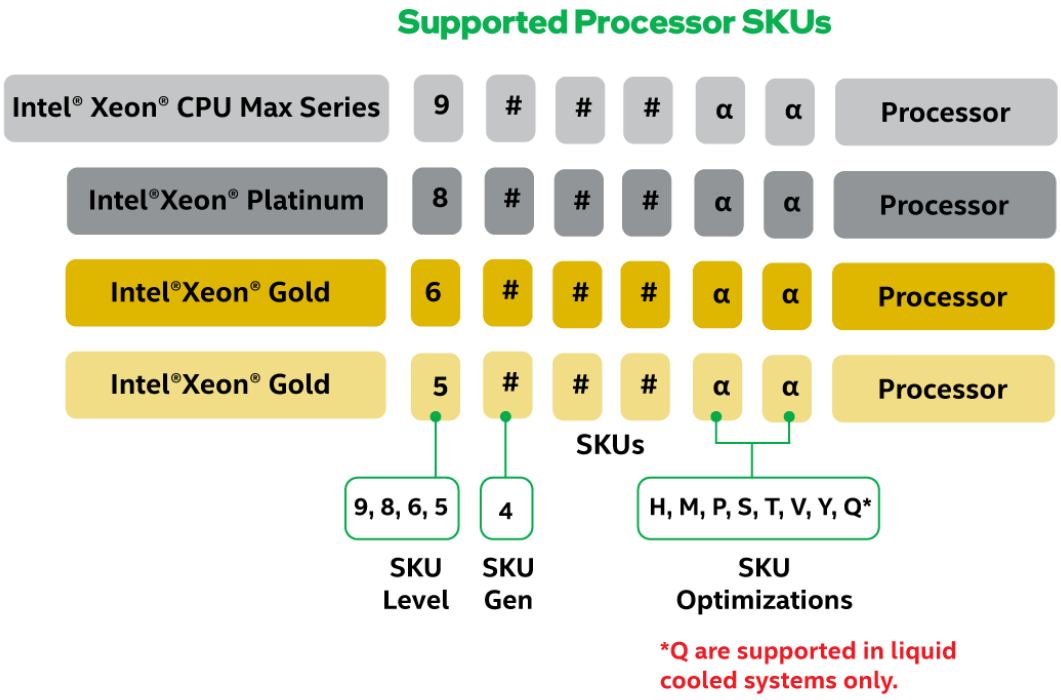


Figure 22. Supported Processor models

Notes:

- Supported 4th Gen Intel® Xeon® Scalable processors SKUs must not end in "N" or "U". All other processor SKUs are supported.

Table 7. 4th Gen Intel® Xeon® Scalable Processors Family Feature Comparison

Feature[1]	Platinum 84xx Processors	Gold 64xx Processors	Gold 54xx Processors
Two-Socket Scalability	Yes	Yes	Yes
# of Intel® UPI 2.0 Links	4[2]	3	3
Intel® UPI 2.0 Speed	16 GT/s	16 GT/s	16 GT/s
# of DDR5 Integrated Memory Controllers (IMC)	4	4	4
# of DDR5 Channels	8	8	8
# of PCIe* 5.0/CXL Lanes	80	80	80
Intel® Turbo Boost Technology	Yes	Yes	Yes
Intel® Hyper-Threading Technology (Intel® HT Technology)	Yes	Yes	Yes
Intel® Advanced Vector Extensions 512 (Intel® AVX-512) ISA Support	Yes	Yes	Yes
Intel® AVX-512 – # of 512b FMA Units	2	2	2
Processor RAS Capability	Advanced	Advanced	Advanced
Intel® VMD 3.0	Yes	Yes	Yes

Notes: (1) Features may vary between processor SKUs. **(2)** The Intel® Server Board D50DNP1SB can only support up to 3 Intel® UPI 2.0 links.

Table 8. Intel® Xeon® CPU Max Series Processor Family Features

Feature[1]	Intel® Xeon® CPU MAX Processors
HBM2e Capacity per Socket[2]	64 GB

Feature[1]	Intel® Xeon® CPU MAX Processors
Two-Socket Scalability	Yes
# of Intel® UPI 2.0 Links	4[3]
Intel® UPI 2.0 Speed	16 GT/s
# of DDR5 Integrated Memory Controllers (IMC)	4
# of DDR5 Channels	8
# of PCIe*/CXL Lanes	80
Intel® DL Boost – Advanced Matrix Extensions (AMX)	Yes
Intel® Turbo Boost Technology	Yes
Intel® Hyper-Threading Technology	Yes
Intel® Data Streaming Accelerator (DSA), 4 devices	Yes
Intel® AVX-512 - # of 512b FMA Units	2
SGX enclave size up to (GB)[4]	512GB
Processor RAS Capability	Advanced
Intel® VMD 3.0	Yes

Notes: (1) Features may vary between processor SKUs. **(2)** Indicates new capabilities relative to 4th Gen Intel® Xeon® Scalable processors. **(3)** The Intel® Server Board D50DNP1SB can only support up to 3 Intel® UPI 2.0 links, **(4)** SGX available only for DDR5 in Flat mode

Refer to the 4th Gen Intel® Xeon® Scalable processor or the Intel® Xeon® CPU Max Series processor specifications and product briefs for additional information.

5.4 Processor Population Rules

When two processors are installed, the following rules apply:

- Both processors must have identical extended family, extended model number, and processor type
- Both processors must have the same number of cores
- Both processors must have the same cache sizes for all levels of processor cache memory
- Both processors must support identical DDR5 memory frequencies

Note: Processors with different steppings can be mixed in a system as long as the rules mentioned in the previous list of bullets are met.

Population rules are applicable to any combination of processors in the 4th Gen Intel® Xeon® Scalable processor family.

For additional information on processor population rules, see the *BIOS Firmware External Product Specification (EPS).*

Note: The server board may support dual-processor configurations consisting of different processors that meet the defined criteria. However, Intel does not perform validation testing of this configuration. In addition, Intel does not ensure that a server system configured with unmatched processors operates reliably. The system BIOS attempts to operate with processors that are not matched but are generally compatible. For optimal system performance in dual-processor configurations, Intel recommends that identical processors be installed.

6. System Memory

This chapter describes the memory subsystem, supported memory types, memory population rules, and supported memory RAS features.

6.1 Supported Memory

The server board supports DDR5 SDRAM RDIMMs. The following figure shows a DDR5 SDRAM DIMM.

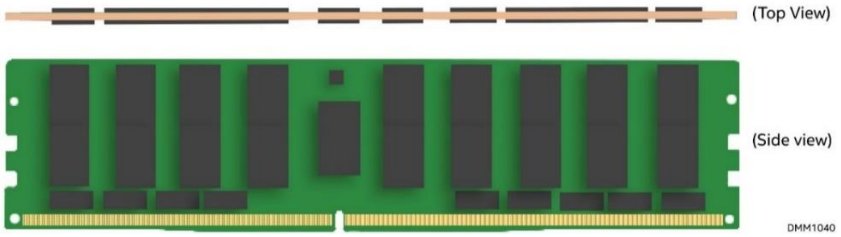


Figure 23. Standard DDR5 SDRAM DIMM

The Intel® Server Board D50DNP1SB supports DDR5 SDRAM DIMMs with the following features:

- Registered DDR5 DIMM (standard RDIMM, 3DS-RDIMM, and 9x4 RDIMM)
  Note: 3DS = three-dimensional stacking.
- All DDR5 RDIMMs must support ECC
- RDIMMs with thermal sensor on-DIMM (TSOD)
- RDIMM speeds of up to 4800 MT/s (for 1 DPC)
- RDIMM capacities of 8 GB, 16 GB, 32 GB, 64 GB, and 128 GB
- RDIMMs organized as single rank (SR), dual rank (DR)
- 3DS-RDIMM organized as quadruple rank (QR), or octuple rank (OR)

The following tables list the DDR5 DIMM support guidelines.

Table 9. Supported DDR5 DIMM Memory

Type	Ranks per DIMM and Data Width	DIMM Capacity (GB) (16 Gb DDR5 Density)	Maximum Speed (MT/s) at 1.1 V (1 DPC)
RDIMM	SR x8	16	4800
	SR x4	32	
	9x4 SR x4	32	
	DR x8	32	
	DR x4	64	
	9x4 DR x4	64	
RDIMM–3DS	QR/OR x4	128 (2H)	

Notes: SR = single rank, DR = dual rank, QR = quadruple rank, OR = octuple rank, H = stack height, DPC = DIMMs per channel.

The maximum supported SDRAM DIMM speed depends on the processor tier as shown in the following table.

Table 10. Maximum Supported DDR5 SDRAM DIMM Speed by Processor Shelves

Processor Family	Maximum DIMM Speed (MT/s) by processor Shelf		
	Platinum 84xx Processors	Gold 64xx Processors	Gold 54xx Processors
4th Gen Intel® Xeon® Scalable processors	4800 1DPC	4800 1DPC	4400 1DPC

6.2 Memory Subsystem Architecture

The Intel® Server Board D50DNP1SB includes eight memory slots per processor as shown in the following figure.

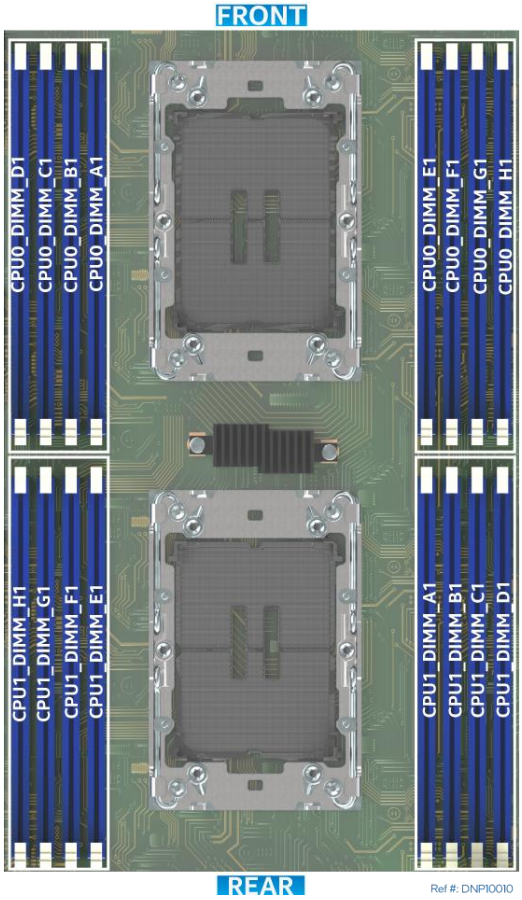


Figure 24. Intel® Server Board D50DNP1SB Memory Slot Layout

As shown in the following figure, each processor has four integrated memory controllers (IMCs), each supporting two memory channels. Memory channels are identified A–H. Each memory channel supports one memory slot.

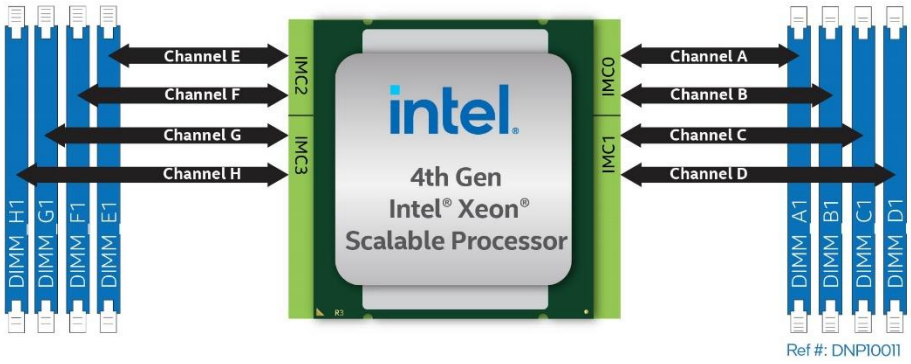


Figure 25. Memory Slot Connectivity for the Intel® Server Board D50DNP1SB

6.3 Memory Population

This section provides memory population rules and recommendations for DDR5 SDRAM DIMMs.

6.3.1 DDR5 SDRAM DIMM Population Rules

Notes:

- Intel does not provide support for systems populated with “Un-like” (non-matching) DIMMs. However, the system may still operate if all the mixed DDR5 DIMM population rules are followed. Validation and support of these configurations is the sole responsibility of the original system integrator.
- For best compatibility and system operation, Intel highly recommends that all installed DIMMs have “identical” or “like” attributes as defined in the Intel DDR5 support disclaimer.

- DDR5 DIMM can be installed in any slot.
- Mixed DDR5 DIMM rules:
  - Mixing DDR5 DIMMs of different speeds and latencies is not supported within or across processors. If a mixed configuration is encountered, the BIOS attempts to operate at the highest common speed and the lowest latency possible.
  - Mixing DDR5 DIMM types (standard RDIMM, 3DS-RDIMM, 9x4 RDIMM) within or across processors is not supported. This will result in a fatal error halt during memory initialization.
- For RDIMM or 3DS RDIMM, same DIMM construction should be used across all slots on a socket
  - No x4 mixing with x8 across a socket
  - No 16Gb / 24Gb mixing
- DDR5 DIMM capacity must be the same for all populated slots.
- Memory slots associated with a given processor are unavailable if the corresponding processor socket is not populated.
- Processor sockets are self-contained and autonomous. However, all memory subsystem support (such as memory RAS and error management) in the BIOS Setup utility are applied commonly for both installed processors.
- For best system performance, memory must be installed in all eight channels for each installed processor.
- For best system performance in dual processor configurations, installed DDR5 DIMM type and population for DDR5 DIMMs configured to CPU 1 must match DDR5 DIMM type and population configured to CPU 0. For additional information, see Section **Error! Reference source not found.**.

Intel DDR5 DIMM Support Disclaimer:

Intel validates and only supports system configurations where all installed DDR5 DIMMs have matching “Identical” or “Like” attributes (see the following table). A system configured concurrently with DDR5 DIMMs from different vendors are supported by Intel if all other DDR5 “Like” DIMM attributes match.

Intel does not perform system validation testing. Intel does not support system configurations where all populated DDR5 DIMMs do not have matching “Like” DIMM attributes as listed in the following table.

Intel only supports Intel server systems configured with DDR5 DIMMs that have been validated by Intel and are listed on Intel’s Tested Memory list for the given Intel server product family.

Intel configures and ships pre-integrated L9 server systems. All DDR5 DIMMs in each L9 server system as shipped by Intel are identical. All installed DIMMs have matching attributes as the attributes listed in the *“Identical” DDR5 DIMM Attributes* column in the following table.

When purchasing more than one integrated L9 server system with the same configuration from Intel, Intel reserves the right to use “Like” DIMMs between server systems. At a minimum, “Like” DIMMS have matching DIMM attributes as listed in the following table. However, the DIMM model #, revision #, or vendor may be different.

For warranty replacement, Intel makes every effort to ship back an exact match to the one returned. However, Intel may ship back a validated “Like” DIMM. A “Like” DIMM may be from the same vendor but may not be the same revision # or model #, or it may be an Intel validated DIMM from a different vendor. At a minimum, all “Like” DIMMs shipped from Intel match attributes of the original part according to the definition of “Like” DIMMs in the following table

Table 11. DDR5 DIMM Attributes Table for “Identical” and “Like” DIMMs

• DDR5 DIMMs are considered “Identical” when ALL listed attributes between the DIMMs match. • Two or more DDR5 DIMMs are considered “Like” DIMMs when all attributes minus the Vendor, and/or DIMM Part # and/or DIMM Revision#, are the same.			
Attribute	**“Identical” DDR5 DIMM Attributes**	**“Like” DDR5 DIMM Attributes**	**Possible DDR5 Attribute Values**
Vendor	**Match**	**Maybe Different**	Memory vendor name
DIMM Part #	**Match**	**Maybe Different**	Memory vendor part #
DIMM Revision #	**Match**	**Maybe Different**	Memory vendor part revision #
SDRAM Type	**Match**	**Match**	DDR5
DIMM Type	**Match**	**Match**	RDIMM, 9x4 RDIMM
Speed (MT/s)	**Match**	**Match**	4000, 4400, 4800
Voltage	**Match**	**Match**	1.1 V
DIMM Size (GB)	**Match**	**Match**	16 GB, 32 GB, 64 GB, 128 GB, 256 GB
Organization	**Match**	**Match**	2Gx80; 4Gx80; 8Gx80; 16Gx80; 32Gx80
DIMM Rank	**Match**	**Match**	1R, 2R, 4R, 8R
DIMM Raw Card (RC)	**Match**	**Match**	RC A, RC B, RC C, RC D, RC E, RC F
DRAM Width	**Match**	**Match**	x4, x8
DRAM Density	**Match**	**Match**	16Gb

6.4 Memory RAS Support

Processors in the 4th Gen Intel® Xeon® Scalable processor family or Intel® Xeon® CPU Max Series processors support standard or advanced memory RAS features, depending on processor SKU, defined in the Table 12. This table lists the RAS features pertaining to system memory that consists of DDR5 SDRAM DIMMs. These features are managed by the processor's IMC.

Table 12. Memory RAS Features

Memory RAS Feature	Description	Standard	Advanced
Device Data Correction	Single Device Data Correction (SDDC) via static virtual lockstep. Supported with x4 DIMMs only.	√	√
	Adaptive Data Correction: Single Region (ADC-SR) via adaptive virtual lockstep (applicable to x4 DDR5 DIMMs). Cannot be enabled with Memory Multi-Rank Sparing or Write Data CRC Check and Retry options enabled.	√	√
	Adaptive Double Data Correction: Multiple Regions (ADDDC-MR, + 1). Supported with x4 DIMMs only.	–	√
DDR5 Command/Address (CMD/ADDR) Parity Check and Retry	DDR5 technology based CMD/ADDR parity check and retry with CMD/ADDR parity error "address" logging and CMD/ADDR retry.	√	√
Memory Demand and Patrol Scrubbing	Demand scrubbing is the ability to write corrected data back to the memory once a correctable error is detected on a read transaction. Patrol scrubbing proactively searches the system memory, repairing correctable errors. Prevents accumulation of single-bit errors.	√	√
Memory Mirroring	Full memory mirroring: an intra-IMC method of keeping a duplicate (secondary or mirrored) copy of the contents of memory as a redundant backup for use if the primary memory fails. The mirrored copy of the memory is stored in memory of the same processor socket's IMC. Dynamic (without reboot) failover to the mirrored DIMMs is transparent to the operating system and applications.	√	√
	Address range/partial memory mirroring: Provides further intra-socket granularity to mirroring of memory. It provides this by allowing the firmware or operating system to determine a range of memory addresses to be mirrored, leaving the rest of the memory in the socket in non-mirror mode.	–	√
Memory Data Scrambling with Command and Address	Scrambles the data with address and command in "write cycle" and unscrambles the data in "read cycle". Addresses reliability by improving signal integrity at the physical layer. Additionally, assists with detection of an address bit error.	√	√
DDR Memory Multi-Rank Memory Sparing	Up to two ranks out of a maximum of eight ranks can be assigned as spare ranks. Cannot be enabled with ADC-SR, ADDDC-MR, +1, and Memory Mirroring options enabled.	√	√
Post Package Repair (PPR)	PPR utilizes additional spare capacity in the DDR5 that can be used to replace faulty cell areas detected during system boot time.	√	√
Partial Cache-Line Sparing (PCLS) for HBM only	Allows replacing failed single bit within a device using spare capacity available within the processor's integrated memory controller (IMC). Up to 16 failures allowed per memory channel and no more than one failure per cache line. After failure is detected, replacement is performed at a nibble level. Supported with x4 DIMMs only.	√	√
Memory Disable and Map Out for Fault Resilient Boot (FRB)	Allows memory initialization and booting to an operating system even when memory fault occurs.	√	√

Memory RAS Feature	Description	Standard	Advanced
Memory Thermal Throttling	Management controller monitors the memory DIMM temperature and can temporarily slow down the memory access rates to reduce the DIMM temperature if needed.	√	√
MEMHOT Pin Support for Error Reporting	The MEMHOT pin can be configured as an output and used to notify if DIMM is operating outside of the target temperature range. Used to implement the memory thermal throttling feature.	√	√

Notes on Population Rules and BIOS Setup Utility for Memory RAS:

- Memory sparing and memory mirroring options are enabled using the BIOS setup utility.
- Memory sparing and memory mirroring options are mutually exclusive in this product. Only one operating mode at a time may be selected in the BIOS setup utility.
- If a RAS mode has been enabled and the memory configuration is not able to support it during boot, the system falls back to independent channel mode and logs and displays errors.
- Rank sparing mode is only possible when all channels populated with memory have at least two single-rank or double-rank DIMMs installed, or at least one quad-rank DIMM installed.
- Memory mirroring mode requires that for any channel pair that is populated with memory, the memory population on both channels of the pair must be identically sized.

The Intel® Server M50DNP Family supports Intel® Software Guard Extensions (Intel® SGX) and Intel® Total Memory Encryption – Multi-Key (Intel® TME-MK) technologies. Intel® SGX works with all basic memory RAS features, but some advanced memory RAS features are not supported together with Intel® SGX as indicated in the following table.

Table 13. Compatibility of RAS Features Intel® SGX and Intel® TME-MK

Feature / Technology	Intel® SGX	Intel® TME-MT
ADC(SR)/ADDDC(MR)	√	√
Memory mirroring	-	√
Machine Check Architecture (MCA) recovery	√	√
Enhanced Machine Check Architecture generation 2 (EMCA2) recovery	-	√

7. PCI Express* (PCIe*) Support

The PCI Express (PCIe) interfaces originated from the CPUs are fully compliant with the *PCIe Base Specification, Revision 5.0.* supporting 32 GT/s bit rate. They are also backward compatible with the previous PCIe specifications, supporting the following bit rates: 16 GT/s (PCIe 4.0), 8.0 GT/s (PCIe 3.0), 5.0 GT/s (PCIe 2.0), and 2.5 GT/s (PCIe 1.0).

The PCIe interfaces routed from the platform controller hub (PCH) to the M.2 connectors are fully compliant with the *PCIe Base Specification, Revision 3.0*, supporting 8.0 GT/s bitrate. They are also backward compatible with the previous PCIe specifications, supporting the following PCIe bit rates: 5.0 GT/s (PCIe 2.0), and 2.5 GT/s (PCIe 1.0).

7.1 PCIe Port Routing

The following table provides the PCIe port routing for the supported riser slots, network interface, and onboard MCIO* connectors.

Table 14. PCIe Port Routing

Host	Port	Width	Gen.	Server Board Connector	Server System Usage	Module Used
CPU 0	Port 0A	x4	4.0	Riser slot 2	U.2 SSD	Management, PCIe accelerator
	Port 0B	x4	3.0	10 Gb Ethernet RJ45	X710-AT2	All modules
	Port 1A-1D	x16	5.0	1 x16 MCIO connector	MCIO	Intel® Data Center GPU Max Series Accelerator – GPU 2 PCIe accelerator riser 1 – slot 2
	Port 2A-2D	x16	5.0	1 x16 MCIO connector	MCIO	Intel® Data Center GPU Max Series Accelerator – GPU 1 PCIe accelerator riser 1 – slot 1
	Port 3A-3D	x16	5.0	Riser slot 1	2U bottom PCIe slot	Management, PCIe accelerator
	Port 4A-4D	x16	5.0	Riser slot 2	1U PCIe slot or 2U bottom PCIe slot	All modules
CPU 1	Port 0A-0D	x16	5.0	1 x16 MCIO connector	MCIO	Intel® Data Center GPU Max Series Accelerator – GPU 3 PCIe accelerator riser 2 – slot 1
	Port 1D	x4	4.0	Riser slot 1	U.2 SSD	Management, PCIe accelerator
	Port 2A-2D	x16	5.0	Riser slot 2 x16 MCIO	2U top PCIe slot	Management, PCIe accelerator
	Port 3A-3D	x16	5.0	1 x16 MCIO connector	MCIO	Intel® Data Center GPU Max Series Accelerator – GPU 4 PCIe accelerator riser 2 – slot 2
	Port 4A-4D	x16	5.0	Riser slot 1 x16 MCIO	1U PCIe slot or 2U top PCIe slot	All modules
PCH Chipset	Port 0–3	x4	3.0	Riser slot 2	M.2 SSD	All modules
	Port 12–15	x4	3.0	Riser slot 1	M.2 SSD	

7.2 PCIe* Enumeration and Allocation

The BIOS assigns PCIe bus numbers in a depth-first hierarchy, in accordance with the *PCIe Base Specification, Revision 5.0*. The bus number is incremented when the BIOS encounters a PCI-PCI bridge device.

The scanning continues on the secondary side of the bridge until all subordinate buses are assigned numbers. PCIe bus number assignments may vary from boot to boot with varying presence of PCIe devices with PCI-PCI bridges.

If a bridge device with a single bus behind it is inserted into a PCIe bus, all subsequent PCIe bus numbers below the current bus are increased by one. The bus assignments occur once, early in the BIOS boot process, and never change during the post-boot phase.

7.3 PCIe Bifurcation

All modules in the Intel® Server D50DNP Family support the following bifurcation of x16 PCIe data lanes into smaller PCIe groups:

- Riser slot 1: 1U PCIe slot riser card / 2U top PCIe slot riser card: x16/x8x8/x8x4x4/x4x4x8/x4x4x4x4
- Riser slot 1: 2U bottom PCIe slot riser card: x16/x8x8/x8x4x4/x4x4x8/x4x4x4x4
- Riser slot 2: 1U PCIe slot riser card / 2U bottom PCIe slot riser card: x16/x8x8/x8x4x4/x4x4x8/x4x4x4x4
- Riser slot 2: 2U top PCIe slot riser card: x16/x8x8/x8x4x4/x4x4x8/x4x4x4x4

In addition, the accelerator module also supports the following bifurcation of x16 PCIe data lanes into smaller PCIe groups:

- Accelerator riser card 1 slot 1: x16/x8x8/x4x4x4x4
- Accelerator riser card 1 slot 2: x16/x8x8/x4x4x4x4
- Accelerator riser card 2 slot 1: x16/x8x8/x4x4x4x4
- Accelerator riser card 2 slot 2: x16/x8x8/x4x4x4x4

Note: The server board includes a clock signal for each PCIe riser slot that is used when the PCIe slot is configured to work at full link width. When a PCIe riser slot is configured with any of the available bifurcation options above, this clock signal is used for one of the PCIe groups. The installed PCIe add-in card must provide clock signals for the remaining PCIe groups and all devices exposed to the system.

To change PCIe bifurcation settings, access the BIOS setup utility by pressing **<F2>** key during POST. Navigate to the following menu: **Advanced > Integrated IO Configuration > PCIe Slot Bifurcation Setting**.

7.4 Non-Transparent Bridge

The PCIe Non-Transparent Bridge (NTB) acts as a gateway that enables high-performance, low-latency communication between two PCIe hierarchies, such as local and remote systems. The NTB allows a local processor to independently configure and control the local system and provides isolation of the local host memory domain from the remote host memory domain, while enabling status and data exchange between the two domains.

The Intel® Server D50DNP Family supports the NTB configuration with NTB port to NTB port connection (back-to-back) on the following PCIe* ports:

- Port 3A on CPU socket 0
- Port 4A on CPU socket 0
- Port 2A on CPU socket 1
- Port 4A on CPU socket 1

NTB port to root port connection is not supported.

Note: When NTB is enabled, the Spread Spectrum Clocking (SSC) option must be disabled at each NTB link.

To enable NTB, access the BIOS setup utility by pressing the **<F2>** key during POST. Navigate to the following menu: **Advanced > Integrated IO Configuration > NTB Configuration**.

8. Storage Options

This chapter provides an overview of the available storage options for the Intel® D50DNP Modules. See Chapter 3 for details on the storage options supported by each Intel® D50DNP Module type.

8.1 M.2 SSD Storage Support

All modules include support for up to two M.2 storage devices using riser assemblies as shown in the following figure. The M.2 slots are labeled `M.2_x4_PCIE*/SATA` on risers 1 and 2. Each M.2 slot supports a PCIe NVMe* or SATA drive that conforms to a 2280 (80-mm) or 22110 (110-mm) form factor.

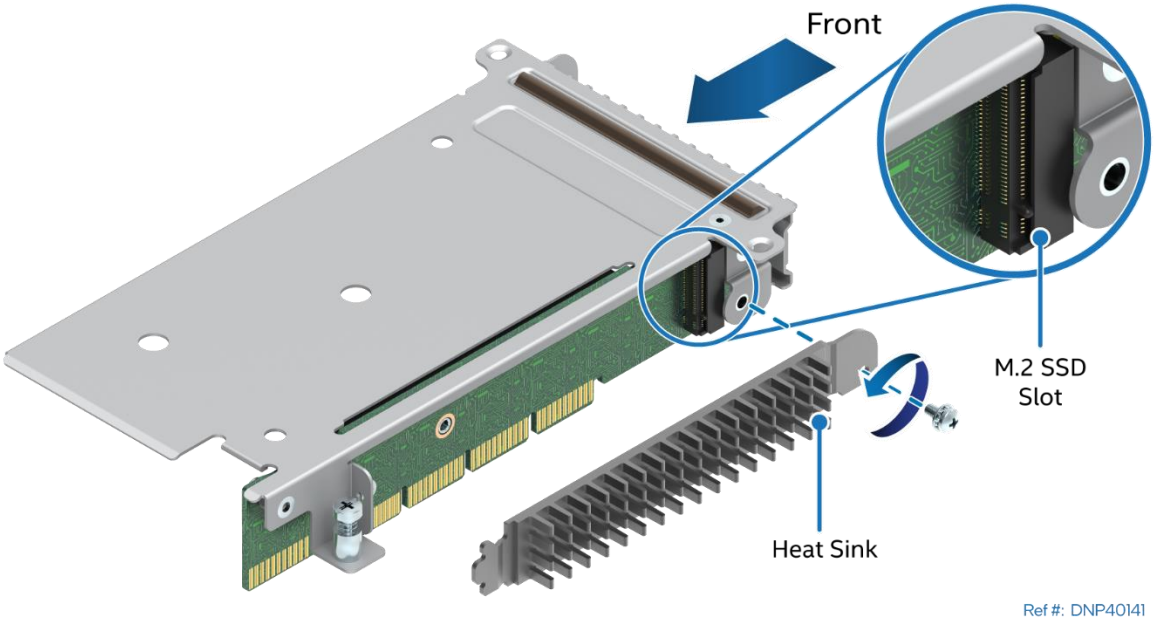


Figure 26. M.2 Slot Location on Riser Card

Note: Riser slot locations are the same for 1U and 2U modules.

The M.2 slots on both risers have four PCIe 3.0 lanes routed from the PCH chipset embedded controller. PCIe NVMe M.2 storage devices support Intel® Volume Management Device (VMD) and Intel® Virtual RAID On CPU (VROC). See Section 8.3 for more information on Intel® VMD and Intel® VROC.

The M.2 slot can support SATA storage devices operating in SATA III mode, providing up to 6 Gb/sec data transfer rate. The M.2 slot on riser #1 uses the PCH chipset embedded SATA-1 controller. The M.2 slot on riser #2 uses the PCH chipset embedded SATA-0 controller. Intel® VROC SATA RAID is not supported on the M.2 storage devices.

M.2 SSDs require a heat sink to maintain proper working temperature. For air cooled systems the M.2 heat sink is not installed on the PCIe riser at the factory. It is an accessory and should be ordered separately for each M.2 SSD (iPC DNPM2HS).

Note: The Intel® Server D50DNP Family only supports SATA SSDs in M.2. slots

8.2 U.2 SSD Storage Support

Up to two hot-swappable 2.5" U.2 PCIe* 4.0 NVMe* SSDs are supported on the 2U management module and 2U PCIe accelerator module. The drive bays are in the front of the module as shown in the following figures.

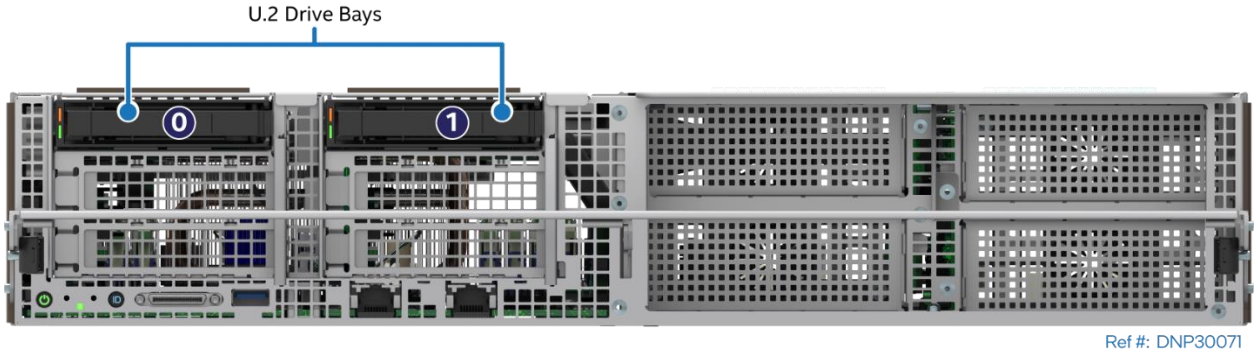


Figure 27. U.2 Drive Bay Identification – 2U PCIe Accelerator Module

Each installed NVMe drive is connected to the PCIe bus through a dedicated U.2 connector attached to the riser assemblies in the 2U management module and 2U PCIe accelerator module.

The U.2 NVMe SSD devices support Intel® VMD and Intel® VROC. See Section 8.3 for more information on Intel® VMD and Intel® VROC.

Each drive carrier includes separate LED indicators for drive activity and drive status. Two LEDs for each drive carrier are amber status LED and green activity LED. The following tables provide the LED states.

Figure 28. Drive Carrier LED Identification

Table 15. Drive Activity LED States

	LED State	Condition
Green	On	Drive present, no activity
	Blinking	LED blinks off when drive is processing a command
	Off	Drive not present
	Blinking 4 Hz	Locate drive (identify)

Note: The drive activity LED is driven by signals coming from the drive itself. Drive vendors may choose to operate the activity LED different from what is described in the previous table. If the activity LED on a given drive type behaves differently than described, customers should reference the drive vendor specifications to determine the expected drive activity LED operation.

Table 16. Drive Status LED States

	LED State	Drive Status
Amber	Off	No fault, OK
	Blinking 4 Hz	Locate (identify)
	Solid on	Fault/fail
	Blinking 1 Hz	Rebuild

Note: The drive status LED state for Rebuild status in the previous table assumes that Intel® Volume Management Device (Intel® VMD) is enabled. If Intel® VMD is disabled, then the drive status LED for the Rebuild status is always off.

8.3 Intel® Volume Management Device (Intel® VMD) 3.0 for NVMe*

Intel® Volume Management Device (Intel® VMD) is a hardware logic inside the processor root complex to help manage PCIe* NVMe SSDs. Intel® VMD provides robust hot plug support and status LED management. This capability allows servicing of storage system NVMe SSD media without the fear of system crashes or hangs when ejecting or inserting NVMe SSD devices on the PCIe bus.

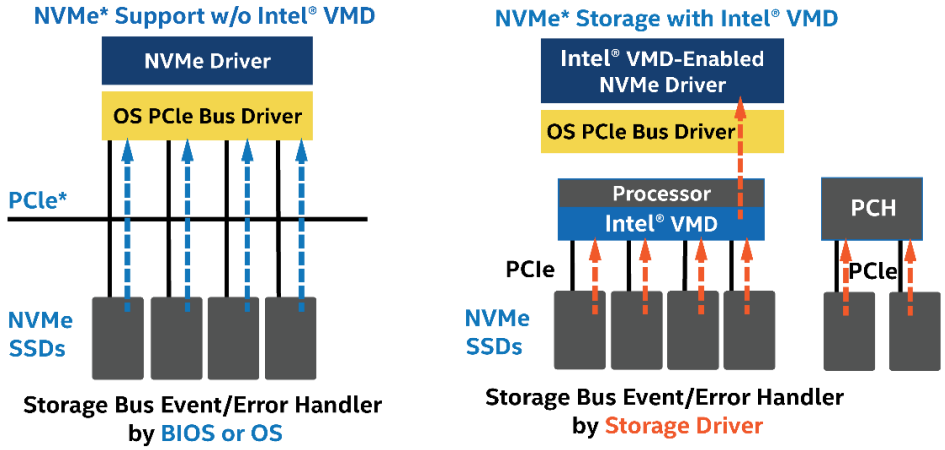


Figure 29. NVMe Storage Bus Event / Error Handling

Intel® VMD handles the physical management of NVMe storage devices as a stand-alone function but can be enhanced when Intel® VROC support options are enabled to implement RAID based storage systems. See Section 8.4 for more information.

8.3.1 Intel® VMD 3.0 Features

The Intel® D50DNP Modules support the following Intel® VMD 3.0 features and capabilities:

- Intel® VMD hardware is integrated inside the processor PCIe root complex.
- Entire PCIe trees are mapped into their own address spaces (domains).
- Each domain manages x16 PCIe lanes.
- Can be enabled/disabled in the BIOS setup utility at x4 lane granularity.
- Driver sets up and manages the domain (enumerate, event/error handling).
- May load an additional child device driver that is Intel® VMD aware.
- Hot plug support – hot insert array of PCIe NVMe SSDs.
- Support for PCIe* NVMe* SSDs only – no network interface controllers (NICs), graphics cards, and so on.
- Does not support NTB, Intel® QuickData Technology, Intel® Omni-Path Architecture (Intel® OPA), or SR-IOV.
- Correctable errors do not bring down the system.
- Intel® VMD only manages devices on PCIe lanes routed directly from the processor or chipset PCH.
- When Intel® VMD is enabled, the BIOS does not enumerate devices that are behind Intel® VMD. The driver enabled for Intel® VMD enumerates these devices and exposes them to the host.

8.3.2 Enabling Intel® VMD 3.0 Support

By default, Intel® VMD support is disabled on all processor PCIe root ports. For installed NVMe devices to use the supported Intel® VMD features, Intel® VMD must be enabled on the appropriate PCIe ports in the BIOS setup utility.

To enable VMD, access the BIOS setup utility by pressing **<F2>** key during POST. Navigate to the following menu: **Advanced > Integrated IO Configuration > Volume Management Device**. Options are available in the menu to enable or disable all or individual PCIe root ports.

Table 14 provides the PCIe root port mapping for all onboard PCIe devices and riser card slots.

8.4 Intel® Virtual RAID on CPU (Intel® VROC) for NVMe SSDs

The Intel® Server D50DNP family can use embedded Intel® Virtual RAID on CPU (Intel® VROC for NVMe) 8.0 technology to provide RAID support for both Intel and non-Intel NVMe SSDs. The Intel® D50DNP Modules support the following Intel® VROC features:

- Bootable RAID volume
- Self-encrypting drive (SED) key management in UEFI
- RAID controller sparring for data volumes
- Management tools (UEFI HII, UEFI CLI utility, OS CLI and GUI utilities)
- Surprise hot-plug
- Status LED manipulation
- Hot spare and auto-rebuild
- E-mail notification for RAID events
- RAID 5 power-loss protection for degraded volumes (double-fault protection)
- Bad block management
- Configurable strip sizes (4k, 8k, 16k, 32k, 64k, 128k)

Intel® VROC offers several options for RAID to meet the needs of the end user. Supported RAID levels on all Intel® D50DNP Modules include RAID 0 and RAID 1.

- **RAID 0**: Uses striping to provide high data throughput, especially for large files in an environment that does not require fault tolerance.
- **RAID 1**: Uses mirroring so that data written to one SSD drive are simultaneously written to another SSD drive. This capability is good for small databases or other applications that require small capacity but complete data redundancy.

Table 17 identifies the features supported by the optional VROC license key.

Table 17. NVMe* RAID Features Supported by Optional VROC License Key

NVMe RAID Major Features	Standard Intel® VROC Key (iPC VROCSTANKEY)
Processor/Chipset-Attached NVMe SSD	√
Bootable RAID Volume	√
Third Party Vendor SSD Support	√
RAID 0/1	√
RAID Write Hole Closure	–
Hot plug/ surprise removal (2.5" SSD Form Factor Only)	√
Enclosure LED Management	√

Enabling Intel® VROC support requires the installation of an optional Intel® VROC License Activation key (iPC **VROCSTANKEY**). A key can be pre-loaded onto the system by Intel when ordering a fully integrated L9 server system using Intel's online Configure-to-Order (CTO) tool, or it can be purchased separately from the system and installed later using the system's Integrated BMC Web Console, Redfish* API, or the Intel® Server Configuration utility. Full installation instructions are provided when the activation license key is ordered separately.

8.5 Server Board SATA Support

The SATA controller can be enabled, disabled, and configured through the BIOS setup utility under the **Mass Storage Controller Configuration** menu screen. The following table lists the supported features by the embedded SATA controller

Table 18. SATA Controller Feature Support

Feature	Description
Native Command Queuing (NCQ)	Allows the device to reorder commands for more efficient data transfers
Auto Activate for DMA	Improves efficiency of data transfer by skipping `DMA Activate` command after `DMA Setup` command
Asynchronous Signal Recovery	Provides a recovery from a loss of signal or establishing communication after hot plug
6 Gb/s Transfer Rate	Capable of data transfers up to 6 Gb/s
ATAPI Asynchronous Notification	A mechanism for a device to send a notification to the host that the device requires attention
Host and Link Initiated Power Management	Capability for the host controller or device to request Partial and Slumber interface power states
Staggered Spin-Up	Enables the host to spin up hard drives sequentially to prevent power load problems on boot
Command Completion Coalescing	Reduces interrupt and completion overhead by allowing a specified number of commands to complete and then generating an interrupt to process the commands

9. Front Control Panel and I/O

This chapter provides information on the control panel and I/O available on the front of the Intel® D50DNP Modules.

9.1 Control Panel Features

The control panel provides push button controls and LED indicators. This section provides a description for each front control panel feature.

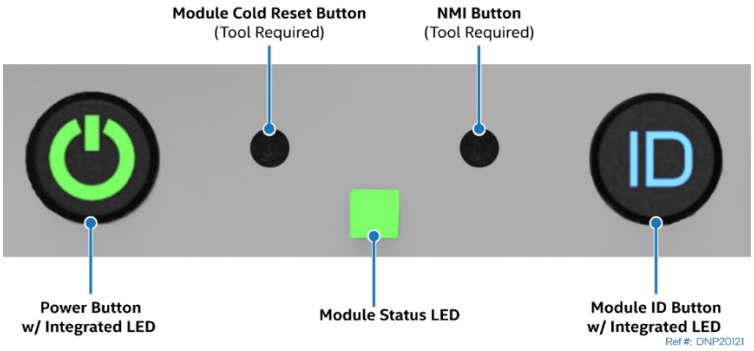


Figure 30. Front Control Panel Features

- **Power button with integrated LED**: Toggles the module power on and off. This button also functions as a sleep button if enabled by an ACPI-compliant operating system. Pressing this button sends a signal to the integrated BMC that either powers on or powers off the module. The integrated LED is a single color (green) and supports different indicator states as defined in the following table.

Note: After AC power is connected, several subsystems are initialized and low-level FRU discovery is performed. This process can take up to 90 seconds. When this process is completed, the Status LED turns solid on, indicating that the system is ready to be powered on.

Table 19. Power / Sleep LED Functional States

Power Mode	LED	Module State	Description
Non-ACPI	Off	Power-off	Module power is off, and the BIOS has not initialized the chipset.
	On	Power-on	Module power is on.
ACPI	Off	S5	Mechanical is off and the operating system has not saved any context to the storage drive.
	On	S0	Module and the operating system are up and running.

- **Module ID button with integrated LED:** Toggles the integrated blue ID LED on and off. The module ID LED is used to identify an Intel® D50DNP Module in a chassis for maintenance when installed in a rack of similar server systems. The module ID LED can also be toggled on and off remotely using the IPMI `Chassis Identify` command that causes the LED to blink for 15 seconds.
- **NMI button:** When the NMI button is pressed, it puts the Intel® D50DNP Module in a halt state and issues a non-maskable interrupt (NMI). This process can be useful when performing diagnostics for a given issue where a memory download is necessary to help determine the cause of the problem. To prevent an inadvertent module halt, the actual NMI button is located behind the front control panel faceplate. The NMI button is only accessible by using a small-tipped tool like a pin or paper clip.

- **Module cold reset button:** When pressed, this button reboots and re-initializes the Intel® D50DNP Module. Unlike the power button, the reset button does not disconnect the power to the module. It just starts the module's power-on self-test (POST) sequence over again.
- **Module status LED:** The module status LED is a bicolor (green/amber) indicator that shows the current health of the module. The module status LED states are driven by the integrated platform management subsystem. Table 20 provides a description of each supported LED state.

Table 20. Intel® D50DNP Module Status LED State Definitions

LED State	Module State	BIOS Status Description
Off	No AC power to system.	• System power is not present. • Module is in EuP Lot6 off mode.
Solid green	Module is operating normally.	• Module is in S5 soft-off state. • Module is running (in S0 State) and its status is healthy. The module is not exhibiting any errors. Source power is present, the BMC has booted, and manageability functionality is up and running. • After a BMC reset, and with the module ID LED solid on, the BMC is booting Linux*. Control has been passed from BMC U-Boot to BMC Linux*. The BMC is in this state for roughly 10–20 seconds.
Blinking green	Module is operating in a degraded state although still functioning; or module is operating in a redundant state but with an impending failure warning.	• Redundancy loss such as fan or power-supply (when Power Cold Redundancy is enabled). Applies only if the associated platform subsystem has redundancy capabilities. • Fan warning or failure when the number of fully operational fans is more than the minimum number needed to cool the system. • Non-critical threshold crossed: temperature, voltage, input power to power supply, output current for main power rail from power supply and processor thermal control (Therm Ctrl) sensors. • Power supply predictive failure occurred while redundant power supply configuration was present. • Cannot use all installed memory (more than 1 memory module installed). • Correctable errors over a threshold and migrating to a spare memory module (memory sparing). This situation indicates that the module no longer has spared memory modules (a redundancy lost condition). • In mirrored configuration, when memory mirroring takes place and the module loses memory redundancy. • Battery failure. • BMC executing in U-Boot (this is indicated by module ID LED blinking at 3 Hz while status blinking at 1 Hz). Module is in degraded state (no manageability). BMC U-Boot is running but has not transferred control to BMC Linux*. The module is in this state 6–8 seconds after BMC reset while it pulls the Linux* image into flash. • BMC watchdog has reset the BMC. • Power unit sensor offset for configuration error is asserted. • SSD hot swap controller (HSC) is off-line or degraded.
Blinking green and amber alternatively	Module is initializing after AC power is applied.	• PFR in the process of updating/authenticating/recovering when AC power is connected, module firmware being updated. • Module not ready to take power button event/signal.

LED State	Module State	BIOS Status Description
Blinking amber	Module is operating in a degraded state with an impending failure warning, although still functioning. Module is likely to fail.	• Critical threshold crossed: voltage, temperature, input power to power supply, output current for main power rail from power supply and PROCHOT (Therm Ctrl) sensors. • VRD hot asserted. • Minimum number of fans to cool the system not present. • Storage drive fault. • Power unit redundancy sensor: Insufficient resources offset (indicates not enough power supplies present). • In non-sparing and non-mirroring mode, if the threshold of correctable errors is crossed within the window. • Invalid firmware image detected during boot or firmware update.

Solid amber	Critical/non-recoverable: module is halted.
	Fatal alarm: module has failed or shut down.
		• CPU `CATERR` signal asserted.
		• MSID mismatch detected (`CATERR` also asserts for this case).
		• CPU 0 is missing.
		• CPU thermal trip.
		• No power good: power fault.
		• Memory module failure when there is only 1 memory module present and hence no good memory is present.
		• Runtime memory uncorrectable error in non-redundant mode.
		• DIMM thermal trip or equivalent.
		• SSB thermal trip or equivalent.
		• Processor `ERR2` signal asserted.
		• BMC/video memory test failed (module ID LED shows blue/solid-on for this condition).
		• Both U-Boot BMC firmware images are bad (module ID LED shows blue/solid-on for this condition).
		• 240 VA fault.
		• Fatal error in processor initialization:
		  ◦ Processor family not identical
		  ◦ Processor model not identical
		  ◦ Processor core/thread counts not identical
		  ◦ Processor cache size not identical
		  ◦ Cannot synchronize processor frequency
		  ◦ Cannot synchronize Intel® UPI link frequency
		• BMC fail authentication with nonrecoverable condition, system hangs at T-1; boot PCH only, system hang; PIT failed, system lockdown

9.2 Front I/O

There are several connectors on the front panel. The following sections describe each of the available connectors.

9.2.1 Networking

The server modules include two RJ45 connectors:

- 10 Gb Ethernet network port
- 1 Gb Ethernet network port dedicated to server management

The following figures show the location of the ports on the Intel® D50DNP Modules.

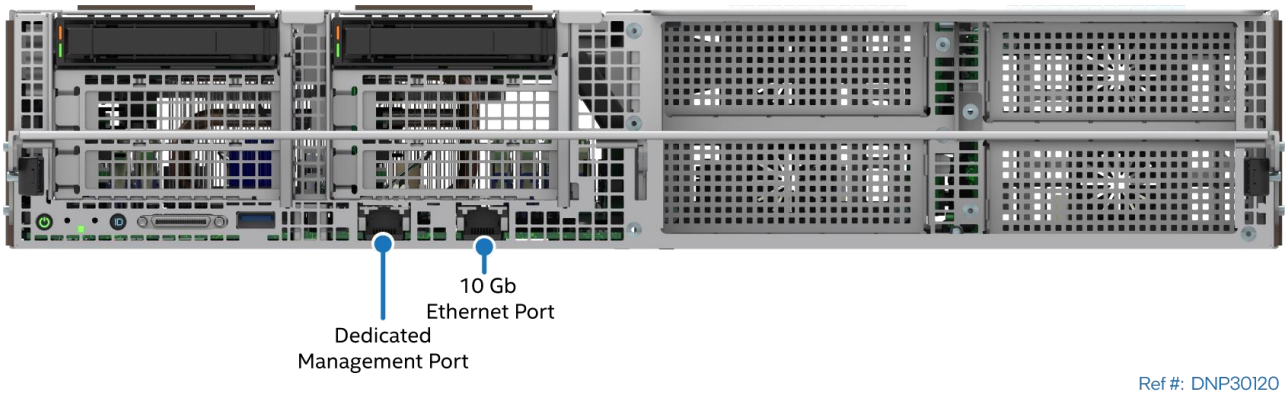


Figure 31. RJ45 Connector Identification – 2U PCIe* Accelerator Module

9.2.1.1 10Gb Network Interface

Network connectivity is provided by the onboard Intel® Ethernet Controller X710-AT2 supporting 1/2.5/5/10 Gb Ethernet. The Intel® Ethernet Controller X710-AT2 is a single, compact, low-power component that offers a fully-integrated 10 gigabit Ethernet media access control (MAC) and physical layer (PHY) port. The Intel® Ethernet Controller X710-AT2 uses the PCIe architecture routed from the processor and provides a single-port implementation.

See the respective product datasheet for a complete list of supported features.

The RJ45 network interface connector includes two LEDs. The LED at the left of the connector is the link/activity LED and indicates a network connection when on and transmit/receive activity when blinking. The LED at the right of the connector indicates link speed as defined in Table 21.

Figure 32. RJ45 Network Interface Connector LEDs

Table 21. 10Gb Ethernet Network Port LED Definition

LED	LED State	NIC State
Link/activity (left)	Off	LAN link not established
	Solid green	LAN link is established
	Blinking green	Transmit/receive activity
Transmit/receive (right)	Solid amber	1 Gb data rate
	Solid green	10 Gb data rate

9.2.1.2 1Gb Network Interface dedicated to server management

Each module includes a 1Gb Ethernet network port dedicated to server management. See Chapter 12 for additional information about server management support.

1Gb Ethernet network port includes two LEDs. The behavior of the LEDs is defined in Table 22.

Figure 33. Dedicated Management Port LEDs

Table 22. 1Gb Ethernet Network Port LED Definition

LED	LED State	NIC State
Link/activity (left)	Off	LAN link not established
	Solid green	LAN link is established
	Blinking green	Transmit/receive activity
Transmit/receive (right)	Off	10 Mb data rate
	Solid amber	100 Mb data rate
	Solid green	1 Gb data rate

9.2.1.3 Network Controller Sideband Interface

In addition to the two network interfaces described above there is a Network Controller Sideband Interface (NC-SI) link between the integrated BMC and the Intel® Ethernet Controller X710-AT2. This allows the integrated BMC to use the network connection of the X710-AT2 NIC port for the management traffic, in addition to the regular host traffic.

9.2.1.4 MAC Address Definition

The server modules have the following MAC addresses assigned at the factory:

- 10Gb Ethernet network port (base MAC address printed on the label attached to the board)
- Network Controller Sideband Interface (base MAC address + 1)
- 1Gb Ethernet network port dedicated to server management (base MAC address + 2)

9.2.2 I/O Breakout Cable

The front panel of each server module has a 40-pin connector supporting an I/O breakout cable as shown in the next figure. The I/O breakout cable provides one serial port, one VGA port, and two USB 3.0 ports.

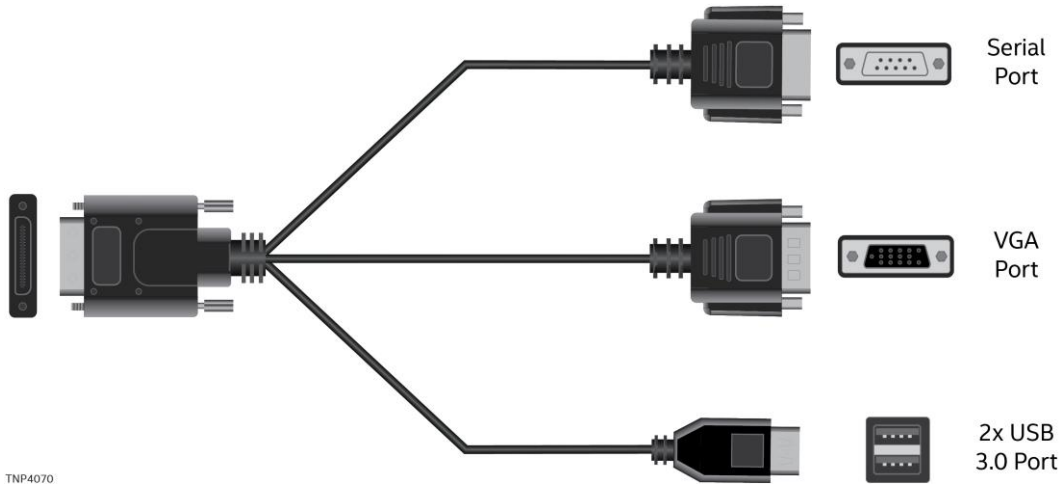


Figure 34. I/O Breakout Cable Port Identification

9.2.3 USB Support

Each server module provides one USB 3.0 port on the front panel. The system also provides two USB 3.0 ports through the dedicated I/O breakout cable (see Section 9.2.2). The following figures show the location of the front USB port.

Figure 65. USB Port Location – 2U PCIe* Accelerator Module

10. Thermal Management

This chapter provides an overview of the thermal management features and capabilities.

Air-cooled configurations are supported for the compute module, management module, and PCIe* accelerator module. The module requiring the lowest ambient temperature will define the ambient requirements for the whole system even if other installed modules allow higher ambient temperature. The fully integrated system is designed to operate at external ambient temperatures of 10–35 °C. Working with integrated platform management, several features move air from the front to the back of the system and over critical components to prevent them from overheating, allowing the system to operate optimally.

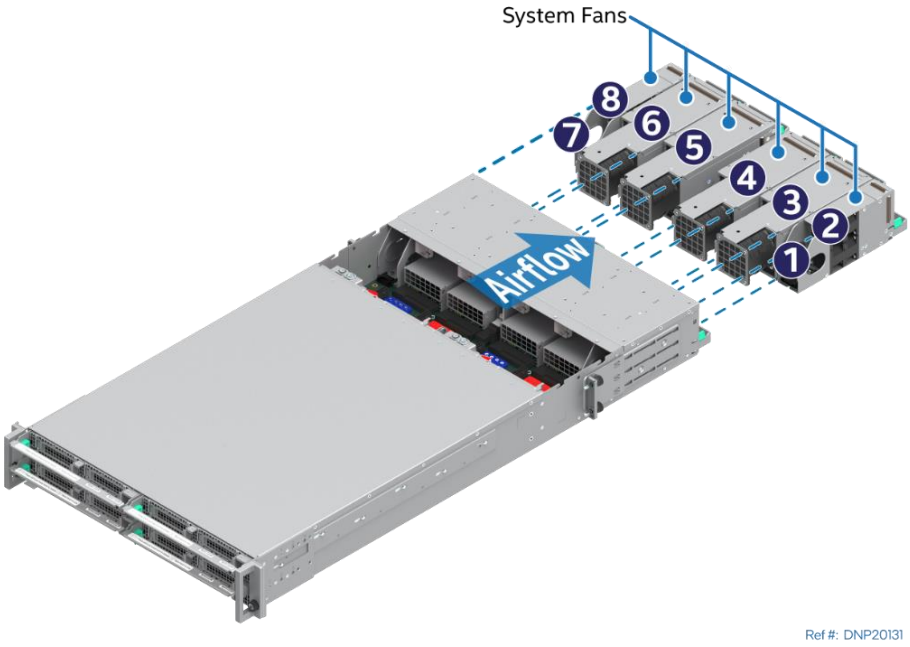


Figure 35. Air-Cooled System Airflow and Fan Identification

The following table provides airflow data associated with the Intel® Server System D50DNP and is provided for reference purposes only. The data was derived from actual wind tunnel test methods and measurements using fully configured (worst case) system configurations. Different system configurations may produce slightly different data results. In addition, the cubic feet per minute (CFM) data provided using server management utilities that use platform sensor data may vary slightly from the data listed in the tables.

Note: For system thermal data, see Appendix E in this document and an online power calculator tool accessible at the following Intel web site: https://servertools.intel.com/tools/power-calculator/.

Table 23. System Volumetric Airflow, Intel® Server D50DNP Family

System Fan Speed	PSU Fan Speed	2U PCIe* Accelerator (CFM)
100%	Auto	296.1
50%		158.0
30%		97.0

The installation and functionality of several system components are used to maintain system thermals. Depending on system cooling configurations, the components are:

- Air-cooled configuration
  - Four managed 60-mm dual rotor hot-swap system fans

    Important Note: Only install 60-mm system fans that are designed for Intel® Server Chassis D50DNP (iPC **FCXX60MMACFAN**). Do not install 60-mm system fans from previous Intel server product generations.
  - Four managed 40-mm dual rotor hot-swap system fans
  - 40-mm fans integrated into each installed power supply module
  - Populated drive carriers (for 2U Intel® D50DNP Modules)
  - Add-in card bays
  - Installed memory modules and DIMM blanks
  - Board component heat sinks
  - Processor heat sinks
  - Air duct

It is necessary to populate all memory slots with either memory modules or supplied DIMM blanks for air-cooled configurations. Preinstalled DIMM blanks must only be removed when installing a memory module in its place.

10.1 Thermal Operation and Configuration Requirements

To keep the system operating within supported maximum thermal limits, the system must meet the following operating and configuration guidelines:

- For air-cooled configurations:
  - The system is designed to sustain operation at an ambient temperature of up to 35 °C (ASHRAE Class A2) with short term excursion-based operation up to 45 °C (ASHRAE Class A4).
  - The system is designed to support long term reliability targets when operated at an external ambient temperature of up to 35 °C (ASHRAE A2).
  - The system can operate up to 40 °C (ASHRAE Class A3) for up to 900 hours per year.
  - The system can operate up to 45 °C (ASHRAE Class A4) for up to 90 hours per year.
  - No long-term system reliability impact when operating at the extended temperature range within the documented limits.
  - System performance may be impacted when operating within the extended operating temperature range.
  - The system is designed to support facility coolant supply temperature of 2–45 °C (ASHRAE Class W45).

Specific configuration requirements and limitations are documented in the system configuration table for thermal compatibility in Appendix E and an online power calculator tool accessible at the following Intel web site: https://servertools.intel.com/tools/power-calculator/.

10.2 Thermal Management Overview

To maintain the necessary airflow in the system, the previously listed components need to be properly installed. For optimal system performance, the external ambient temperature should remain below 35 °C and all system fans must be operational. System fan rotor failure can be supported with limited performance for some components in the system. See Appendix E for performance impact in fan failed mode.

For system configurations that support fan redundancy, if a single fan rotor failure occurs (system fan or power supply fan), integrated platform management does the following:

- Changes the state of the system status LED to blinking green.

- Reports an error to the system event log (SEL).
- Automatically adjusts fan speeds of operational fans as needed to maintain system temperatures below maximum thermal limits.

Note: All system fans are controlled independently of each other. The fan control system may adjust fan speeds for different fans based on increasing/decreasing temperatures in different chassis thermal zones.

Fan redundancy is lost if more than one fan rotor in the same fan or in different fans is in a failed state.

If system temperatures continue to increase with the system fans operating at their maximum speed, platform management may begin to throttle bandwidth of either the memory subsystems, the processors, or both to prevent components overheating and keep the system operational. Throttling of these subsystems continues until system temperatures are reduced below preprogrammed limits.

If system thermals increase to a point beyond the maximum thermal limits, the system shuts down, the system status LED changes to solid amber, and the event is logged to the SEL.

If power supply thermals increase to a point beyond their maximum thermal limits or if a power supply fan fails, the power supply shuts down.

Note: For proper system thermal management, correct Field Replaceable Unit (FRU) information for any given system configuration must be loaded by the system integrator as part of the initial system integration process. FRU data is loaded using the firmware update utility that is part of the system update package (SUP) that can be downloaded from http://downloadcenter.intel.com.

10.3 System Fans

The system includes different fans depending on the following cooling configurations:

- Air-cooled configuration
  - Four managed 60-mm dual rotor hot-swap system fans

    Important Note: Only install 60-mm system fans (iPC **FCXX60MMACFAN**) that are designed for Intel® Server Chassis D50DNP (iPCs **FC2HAC27W0**). See the following figure. Do not install 60-mm system fans from previous Intel® Server Products generations.

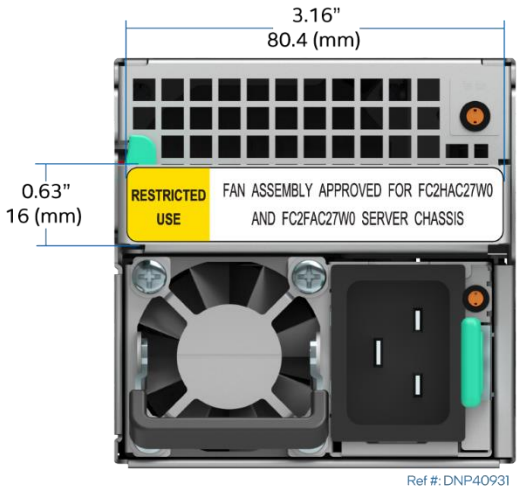


Figure 36. 60-mm System Fan Dimensions

  - Four managed 40-mm dual rotor hot-swap system fans. The fans are contained in two fan assemblies, two fans per assembly.
  - 40-mm fan integrated into each installed power supply module

The system fans and power supply module fans provide the primary airflow for the system. The system is designed for fan redundancy with the condition that all system fan rotors are operational and ambient air remains at or below ASHRAE Class 2 limits.

Should a single system fan rotor fail, platform management adjusts airflow of the remaining system fans and manages other platform features to maintain system thermals. Fan redundancy is lost if more than one fan rotor in the same fan or in different fans is in a failed state.

The system supports eight system fans in air-cooled configurations. All system fans are mounted in an individual fan assembly module. Each system fan:

- Is hot-swappable.
- Is designed for tool-less insertion and extraction from the system chassis.
- Has a tachometer signal that allows the integrated BMC to monitor its status.
- Is controlled by integrated platform management. As system thermals fluctuate high and low, the integrated BMC firmware increases and decreases the speeds to specific fans in the fan assembly to regulate system thermals.
- Is mounted inside a fan cage assembly that can be removed from the back of the system chassis. The fan cage assembly includes a fan fail LED visible from the back of the system chassis.
- Connects to the power distribution board through a pin connector. The following three tables list the connector pinout for each fan type.

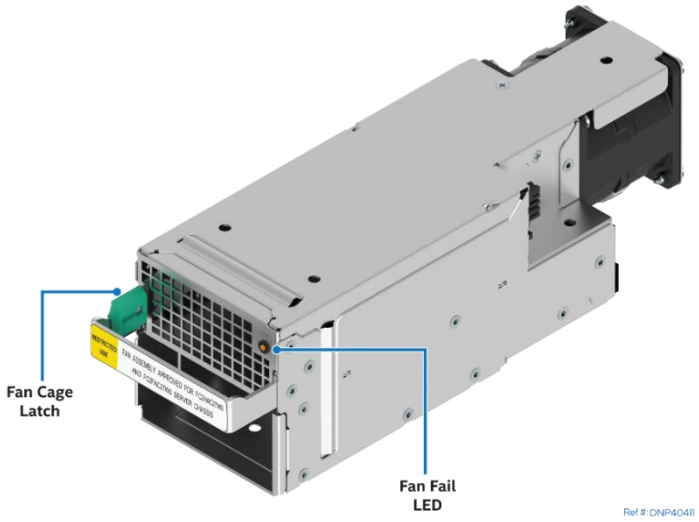


Figure 37. 60-mm System Fan Cage Assembly

Table 24. 60-mm System Fan Connector Pinout

Pin #	Signal Name	Pin #	Signal Name
1	P12V_FAN_ROTOR1	6	FAN_PRSNT_N
2	GND	7	FAN_CATH_LED
3	FAN_TACH1_FLT	8	FAN_ANODE_LED
4	FAN_TACH2_FLT	9	P12V_FAN_ROTOR2
5	FAN_PWM_FLT	10	GND

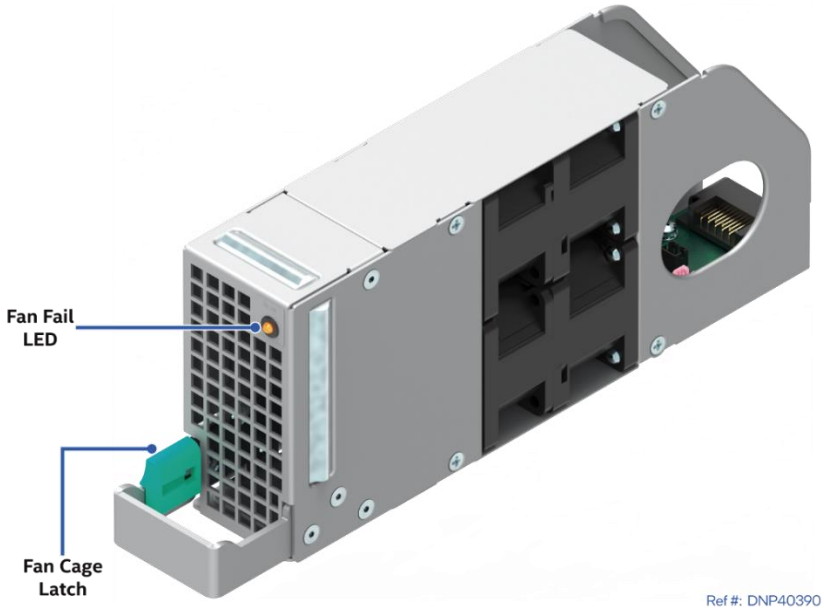


Figure 38. 40-mm System Fan Cage Assembly Air Cooled

Table 25. 40-mm System Fan Cage Assembly Air Cooled Pinout

Pin #	Signal Name	Pin #	Signal Name
1	P12V_FAN	9	P12V_FAN
2	P12V_FAN	10	P12V_FAN
3	FAN1_TACH1_FLT	11	FAN2_TACH1_FLT
4	FAN1_TACH2_FLT	12	FAN2_TACH2_FLT
5	FAN1_PWM_FLT	13	FAN2_PWM_FLT
6	GND	14	GND
7	GND	15	GND
8	GND	16	GND

10.4 Power Supply Module Fans

Each installed power supply in an air-cooled configuration includes an embedded (nonremovable) 40-mm fan. These fans regulate the airflow through the power supply module and are managed by the fan control system of the power supply. Should a fan fail, the power supply shuts down.

10.5 Fan Speed Control

The BMC controls and monitors the system fans. Each fan is associated with a fan speed sensor that detects fan failure and may also be associated with a series of events in format of Redfish logs for hot-swap support. For redundant fan configurations, the fan failure and presence status will contribute to system events in format of Redfish log.

The system fans are divided into fan zones or domains, each of which has a separate fan speed control signal and a separate configurable fan control policy. A fan domain can have a set of temperature and fan sensors associated with it. These are used to determine the current fan zone state.

A fan domain has two states: nominal, and failsafe. The failsafe state has a fixed (but configurable through Redfish) fan speeds associated with them. The nominal state has a variable speed determined by the fan

domain policy. A redfish configurable entity-manager configuration is used to configure the fan domain policy.

The fan domain state is controlled by several factors, listed below in order of precedence from high to low. If any of these conditions apply, the fans are set to a fail-safe state speed.

- Associated fan is in a critical state or missing. The configuration describes which fan domains are boosted in response to a fan failure or removal in each domain.
- Any associated temperature sensor is in a critical state. The configuration describes which temperature-threshold violations cause fan boost for each fan domain.
- The BMC is in firmware update mode, or the operational firmware is corrupted.

For more information on nominal fan speed, see Section 10.5.4.

10.5.1 Hot-Swappable Fans Handling

Intel® Server Board D50DNP1SB supports hot-swappable fans that can be removed and replaced while the system is powered on and operating. The BMC implements fan presence sensors for each hot-swappable fan.

When a fan is not present, the associated fan speed sensor is put into the reading/unavailable state, and any associated fan domains are put into the boost state. The fans may already be boosted due to a previous fan failure or fan removal.

When a removed fan is inserted, the associated fan speed sensor is rearmed. If there are no other critical conditions causing a fan boost condition, the fan speed returns to the nominal state. Power cycling or resetting the system rearms the fan speed sensors and clears fan failure conditions. If the failure condition is still present, the fan returns to its boosted state once the sensor has reinitialized and the threshold violation is detected again.

10.5.2 Fan Redundancy Detection

The BMC supports redundant fan monitoring and implements a fan redundancy sensor. A fan redundancy sensor generates events when its associated set of fans transitions between redundant and nonredundant states, as determined by the number and health of the fans.

Note: The definition of fan redundancy is server system configuration dependent. The BMC allows for redundancy to be configured on a per-fan redundancy sensor basis.

A fan failure or removal of hot-swap fans up to the number of redundant fans specified in a fan configuration is a noncritical failure and is reflected in the front panel status. A fan failure or removal that exceeds the number of redundant fans is a nonfatal, insufficient-resources condition and is reflected in the front panel status as a nonfatal error. In the front control panel, a blinking green system status LED indicates noncritical error and a blinking amber LED indicates nonfatal error.

Redundancy is checked only when the system is in the DC-on state. Fan redundancy changes that occur when the system is DC-off or when AC is removed are not logged until the system is turned on.

10.5.3 Fan Control Mechanism

System fan speeds are controlled through pulse width modulation (PWM) signals that are driven separately for each domain by integrated PWM hardware. Fan speed is changed by adjusting the duty cycle that is the percentage of time the signal is driven high in each pulse.

The BMC controls the average duty cycle of each PWM signal through direct manipulation of the integrated PWM control registers.

The same device may drive multiple PWM signals.

10.5.4 Nominal Fan Speed

A fan domain's nominal fan speed can be configured as static (fixed value) or controlled by the state of one or more associated temperature sensors.

Redfish modifiable JSON records are used to configure which temperature sensors are associated with which fan control domains and the algorithmic relationship between the temperature and fan speed. Configurations can reference or control the same fan control domains and multiple configurations can reference the same temperature sensors.

The PWM duty-cycle value for a domain is computed as a percentage using one or more instances of a stepwise linear algorithm and a PID algorithm. The transition from one computed nominal fan speed (PWM value) to another is ramped over time to minimize audible transitions. The ramp rate can be modified in the configuration.

Multiple stepwise linear and PID controls can be defined for each fan domain and used simultaneously. For each domain, the BMC uses the maximum of the domain's stepwise linear control contributions and PID control contributions to compute the domain's PWM value, except that a stepwise linear instance can be configured to provide the domain maximum.

Hysteresis can be specified to minimize fan speed oscillation and to smooth fan speed transitions.

10.5.5 Increasing Fan Speed

The system provides a BIOS setup utility option to boost the system fan speed by a programmable fan pulse width modulation (PWM) positive offset setting. Enabling the **Fan PWM Offset** option causes the BMC to add the offset to the fan speeds to which it would otherwise be driving the fans. This setting causes the BMC to replace the domain minimum speed with alternate domain minimums.

This capability is offered to provide system administrators the option to manually configure fan speeds in instances where the fan speed optimized for a given platform may not be sufficient when a high-power add-in adapter is installed into the system. This capability enables easier usage of the fan speed control to support Intel and non-Intel chassis and better support of ambient temperatures higher than 35 °C.

10.5.6 Thermal and Acoustic Management

This feature allows for enhanced fan management to keep the system optimally cooled while reducing the amount of noise generated by the system fans. Aggressive acoustics standards might require a trade-off between fan speed and system performance parameters that contribute to the cooling requirements, primarily memory bandwidth. The BIOS, BMC, and SDRs work together to provide control over how this trade-off is determined.

This capability requires the BMC to access temperature sensors on individual memory modules. Additionally, closed-loop thermal throttling is only supported with memory modules containing temperature sensors.

10.5.7 Thermal Sensor Input to Fan Speed Control

The BMC uses various sensors as input to the fan speed control. Some of the sensors are actual physical sensors whereas some are "virtual" sensors whose values are derived from physical sensors using calculations and/or tabular information.

The following IPMI thermal sensors are used as input to fan speed control:

- Front panel temperature sensor [1]
- Processor margin sensors [2, 4, 5]
- DIMM thermal margin sensors [2, 4]
- Exit air temperature sensor [1, 7, 9]
- PCH temperature sensor [3, 5]

- Onboard Ethernet controller temperature sensors [3, 5]
- PSU thermal sensor [3, 8]
- Processor VR temperature sensors [3, 5]
- DIMM VR temperature sensors [3, 6]
- BMC temperature sensor [3, 6]
- Global aggregate thermal margin sensors [7]
- Riser card temperature sensors

Notes:
[1] For fan speed control in an Intel server chassis
[2] Temperature margin to max junction temp
[3] Absolute temperature
[4] PECI value or margin value
[5] On-die sensor
[6] Onboard sensor
[7] Virtual sensor
[8] Available only when PSU has PMBus*
[9] Calculated estimate

The following figure shows a high-level representation of the fan speed control model that determines fan speed.

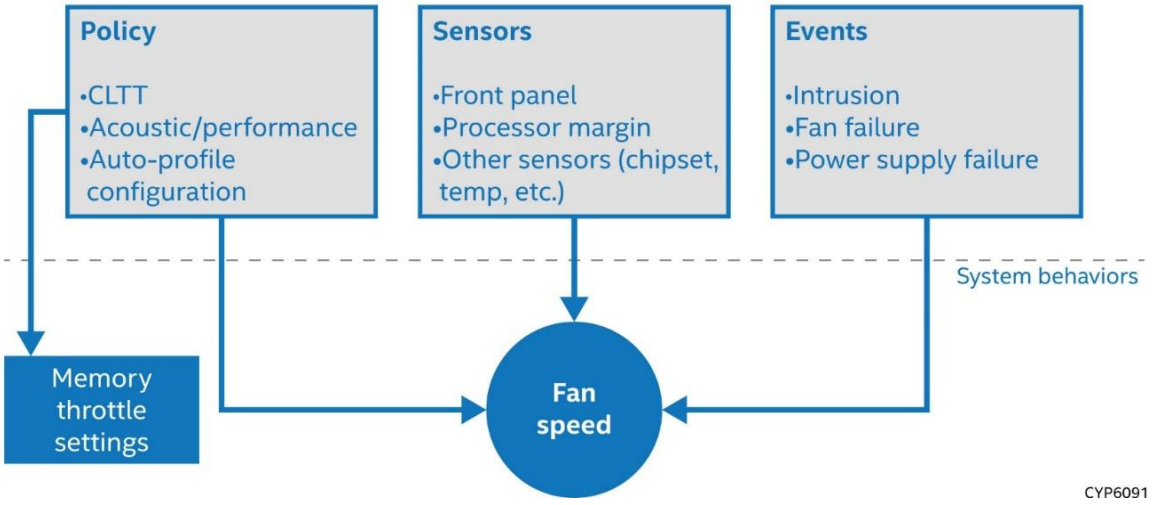


Figure 39. High-Level Fan Speed Control Model

11. System Power

The Intel® Server System D50DNP supports the following power supply options:

- AC 2700 W (80 Plus Titanium) for air-cooled configurations

The server system can support up to four power supplies. Each power supply is hot-swappable and allows tool-less insertion and extraction from the rear of the chassis. Depending on the shipping configuration from Intel, systems may or may not have power supplies preinstalled.

Disclaimer: The Intel® Server D50DNP Family is designed to operate as described in this technical product specification when connected to a 200–240 V power source. Connecting to a lower voltage power line is not supported and may result in unreliable system operation. If a 200–240 V power source is not available, it is the responsibility of the system integrator to recalculate the total power consumption of the system.

Note: All power supplies must be identical. Using different power supply options concurrently is not supported. This invalid configuration does not provide power supply redundancy and results in multiple errors being logged by the system.

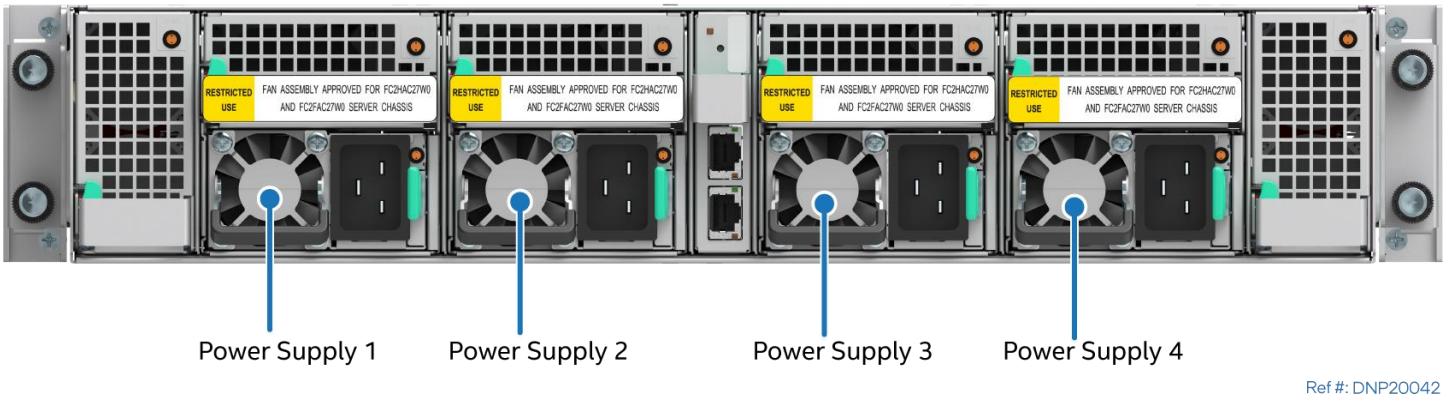
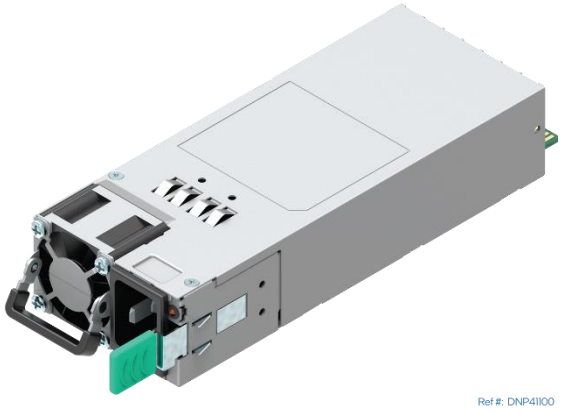


Figure 40. Power Supply Module Identification – Air Cooled



2700 W Power Supply Module

Figure 41. 2700 W Power Supply Modules

11.1 Power Supply Configurations

The Intel® Server Chassis D50DNP can have up to four power supply modules installed. The Integrated BMC calculates the total power demand at the chassis level and distributes the power load among the

installed power supply modules. A fully configured 4-module system supports the following power supply configurations:

- 4+0 combined power (non-redundant)
- 3+1 redundant power (module dependent)
- 2+2 redundant power (module dependent)

Redundant power and combined power configurations are automatically configured depending on the number of modules in the system. Should system thermal levels exceed programmed limits, platform management attempts to keep the system operational. For details, see Section 11.3 and Chapter 10.

If a power supply failure occurs, the redundant power configuration supports hot-swap extraction and replacement of the failed power supply. If a power supply failure occurs in a 4+0 configuration, the other three power supplies provide the power and the system may throttle.

11.2 Intel® Power Calculator Tool

For system integrators that would like to determine the system power draw and heat dissipation for a specific system configuration, Intel makes available an online power calculator tool accessible at the following Intel webpage: https://servertools.intel.com/tools/power-calculator/

11.3 Closed Loop System Throttling (CLST)

Closed-loop system throttling (CLST) prevents the system from crashing if a power supply module is overloaded or overheats. If the system power reaches a pre-programmed power limit, CLST throttles system memory and/or processors to reduce power consumption. System performance is degraded if throttling occurs.

11.4 Smart Ride Through (SmaRT) Throttling

Smart Ride Through (SmaRT) throttling increases the reliability of a system operating in a heavy power load condition and contributes to remain operational during an AC line dropout event.

When AC voltage goes low, a fast AC loss detection circuit inside each installed power supply asserts an `SMBALERT#` signal to initiate a throttle condition in the system. System throttling reduces the bandwidth to both system memory and processors, which, in turn, reduces the power load during the AC line drop out event.

11.5 Cold Redundancy Support

Power supplies that support cold redundancy can be enabled to go into a low-power state, like a cold redundant state. This kind of low-power state provides increased power usage efficiency when system loads are such that all power supplies are not needed. When the power subsystem is in cold redundant mode, only the needed power supplies to support the best power delivery efficiency are on. Any additional power supplies, including the redundant power supply, are in cold standby state.

11.5.1 Powering on Cold Standby Supplies to Maintain Best Efficiency

Enabling power supplies to maintain optimal efficiency is achieved by looking at the load share bus voltage and comparing it to a programmed voltage level.

Power supplies in Cold Standby state monitor the shared voltage level of the load share signal to sense when they need to power on. Depending on the position (1, 2, 3, or 4) of the power supply assigned by the system, the Cold Standby configuration slightly changes the load share threshold that turns on the power supply.

A cold-redundant-capable power supply will start up with cold redundancy **disabled** when it is first plugged in (that is, it starts up in an active state) and remains that way until the BMC explicitly sends it a PMBus command to enable a cold redundancy state.

Table 26. Power Supply Operational Modes

Operational Mode	Description
Standard redundancy	This is the standard redundant load sharing mode (that is, cold redundancy is disabled).
Cold redundant active	The power supply is always on in a cold redundancy configuration.
Cold standby 1	Defines the power supply that is first to turn on in a cold redundant configuration as the load increases.
Cold standby 2	Defines the power supply that is second to turn on in a cold redundant configuration as the load increases.
Cold standby 3	Defines the power supply that is third to turn on in a cold redundant configuration as the load increases.

11.5.2 Automatic Cycling of Redundancy Ranking

The BMC firmware provides a configurable cycling capability to allow for equal loading across power supply lifetime. The BMC uses the `Set Cold Redundancy Configuration` command to define or configure the power supply's role in cold redundancy and to turn on/off cold redundancy.

If rotation is enabled, then the BMC periodically rotates the rank assignments to distribute the workload over the lifetime of the system power supplies.

The BMC Cold Redundancy configuration has the following default settings:

- Cold redundancy is enabled.
- Automatic rank cycling is enabled.
- Rotation timeout reached.

The following events trigger BMC reconfiguration of the power supplies' cold redundancy rankings:

- Power supply inserted or removed from the system.
- AC power restored in power supply.

The BMC reverts to BMC static rank ordering if a user-specified rank order is chosen and there is a change in the power supply population. Examples of power supply population changes are: a power supply is removed or inserted, or a power supply fails, or AC is lost in power supply.

11.5.3 BMC support for Cold Redundancy

The BMC provides an OEM IPMI command that allows management software to control the behavior of the cold redundancy feature as follows:

- Ability to turn off/on the cold redundancy feature.
- Ability to turn off/on the automatic rank cycling.
- Ability to set a specified rank order.
- Ability to configure the cycling period for automatic rank cycling.

These settings are stored in BMC non-volatile memory and are therefore persistent across BMC resets, but not across AC cycles because an AC power-on/off event is a trigger for reconfiguring the power supply rankings. In the multi node system, Master node is allowed to access the management software to control the behavior of the Cold Redundancy feature, and Slave nodes are not.

11.6 Power Supply Specification Overview

The Intel® Server System D50DNP supports the following power supply options:

- AC 2700 W (80 Plus Titanium)

AC power supplies are auto-ranging and power factor corrected.

The following sections provide an overview of select power supply features and functions.

Note: Full power supply specification documents are available upon request. Power supply specification documents are classified as Intel Confidential and require a signed nondisclosure agreement (NDA) with Intel before being made available.

11.6.1 Power Supply Module Efficiency

Each power supply option is rated to meet specific power efficiency limits based on their 80 PLUS power efficiency rating.

The following tables define the required minimum power efficiency levels based on their 80 PLUS efficiency rating at specified power load conditions: 100%, 50%, 20%, and 10%

The AC power supply efficiency is tested over an AC input voltage range of 115 VAC to 220 VAC.

Table 27. 2700 W AC Power Supply Option Efficiency (80 PLUS* Titanium)

	Loading	100% of Maximum	50% of Maximum	20% of Maximum	10% of Maximum
	Minimum Efficiency	94%	96%	95%	94%

11.6.2 AC Power Cord Specifications

The power connector on a 2700 W AC power supply follows the International Electrotechnical Commission (IEC) 320 C20 standard.

Figure 42. IEC C20 Connector

Figure 43. IEC C22 Connector

The AC power cords are not included with systems. The AC power cord attached to the 2700 W AC power supply must meet the following specifications.

Table 28. AC Power Cord Specifications

Characteristic	Value
Cable Type	SJT
Wire Size	12 AWG
Temperature Rating	105 ºC
Amperage Rating	15 A at 240 V
Voltage Rating	240 VAC

11.7 Power Supply Features

The following sections describe features supported by the AC power supply options.

11.7.1 Power Supply Status LED

A single bicolor LED indicates power supply status. The operational states of this bicolor LED are defined in the following table.

Table 29. LED Indicators

LED State	Power Supply Condition
Off	No source power to all power supplies.
Solid green	Output ON and OK.
1 Hz blinking green	Source power present/only 12 VSB on (PS off) or PS in cold redundant state.
Solid amber	Source power cord unplugged, or source power lost; with another power supply in parallel still with AC input power. Or power supply critical event causing a shutdown; failure, OCP, OVP, fan fail.
1 Hz blinking amber	Power supply warning events where the power supply continues to operate; high temperature, high power, high current, slow fan.
2 Hz blinking green	Power supply firmware updating.

11.7.2 Protection Circuits

Each installed power supply module includes several protection circuits that shut down the power supply if a defined operating threshold is exceeded.

11.7.2.1 Over Current Protection (OCP) and Over Voltage Protection (OVP)

Each installed power supply is protected against over current. The power supply unit shuts down after a specific time period after crossing current thresholds. A power supply that is shut down due to an exceeded protection circuit threshold can be reset by removing source power for 15 seconds.

Table 30. Over Current Protection, 2700 W Power Supply

Output Voltage	Input Voltage Range	Over Current Limits	OCP Delay
+12 V	180–264 VAC	326 A minimum / 332 A maximum	50 msec minimum / 200 msec maximum
		358 A minimum / 366 A maximum	5 msec minimum / 20 msec maximum
12 VSB	90–264 VAC	3.6 A minimum / 4.0 A maximum	5 msec minimum / 20 msec maximum

Table 31. Over Voltage Protection, 2700 W Power Supply

Output Voltage	Minimum (V)	Maximum (V)
+12 V	13.5	14.5
+12 VSB	13.5	14.5

11.7.2.2 Over Temperature Protection (OTP)

Each installed power supply is protected against over temperature conditions caused by loss of fan cooling capability or excessive ambient temperature. The power supply unit shuts down during an OTP condition. Once the power supply temperature drops to within specified limits, the power supply restores power automatically.

Note: The 12 VSB always remains on while the power supply is connected to the power source.

11.8 Power Distribution Board (PDB)

The Intel® Server System D50DNP includes a power distribution board in the back of the chassis that provides power and management connections for several components in the system. The following figure shows the location of the PDB in the system.

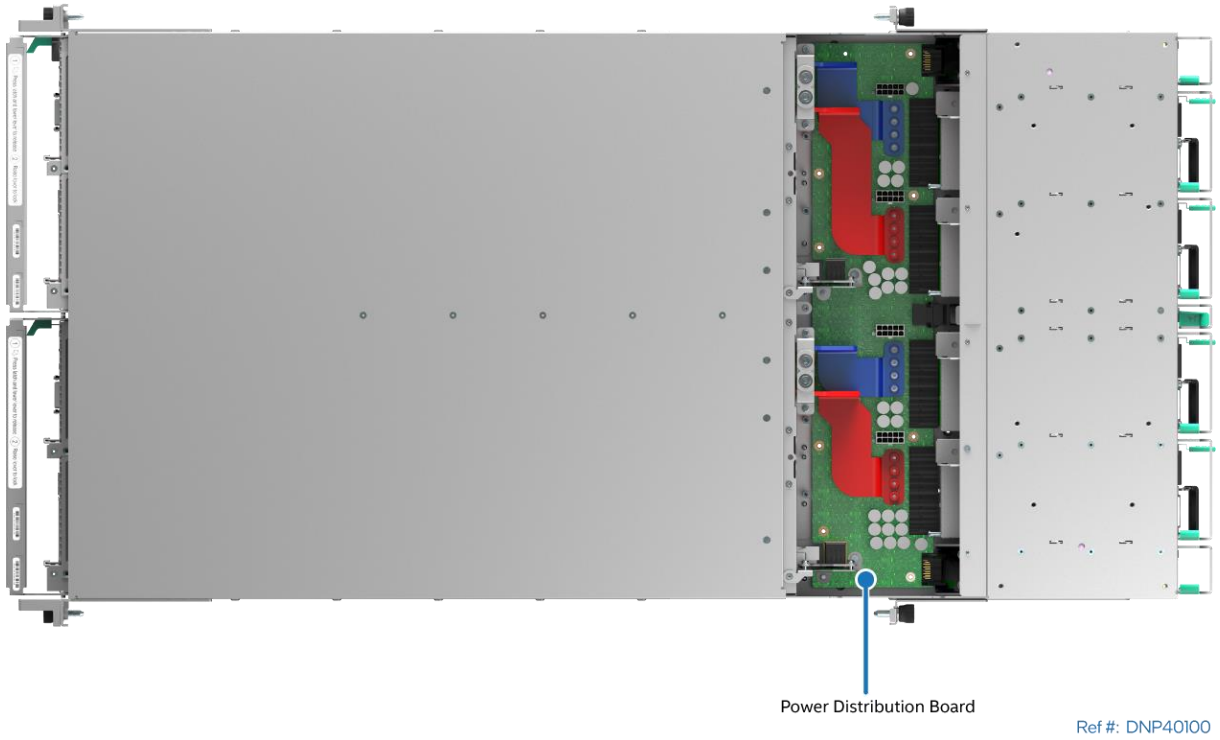


Figure 44. Power Distribution Board Identification

The power distribution board includes the following connectors:

- Six system fan connectors on top
- Four power supply interface connectors at the rear edge
- One EMP module docking port in the rear
- Four power connectors in the front, for providing power to the Intel® D50DNP Modules
- Two management risers with high-speed management ports, for communication between the Intel® D50DNP Modules, the EMP module, and system fans

The following figure identifies the different connectors in the power distribution board.

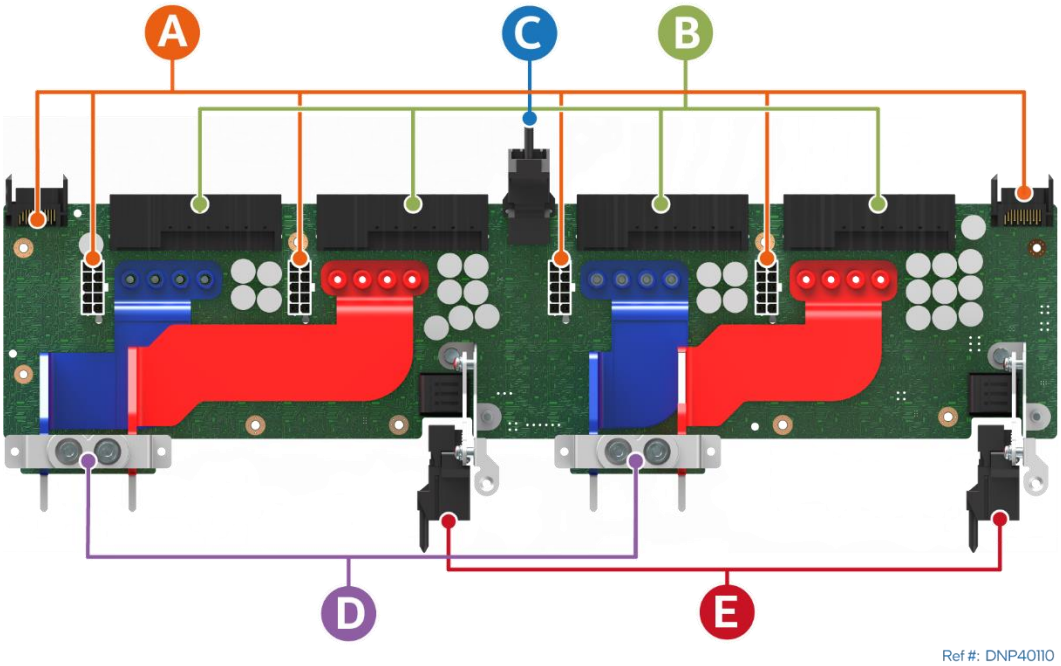


Figure 45. Power Distribution Board Connector Identification

Table 32. Power Distribution Board Connector Identifiers

Connector Identifier	Description
A	System fan connectors
B	Power supply connectors
C	EMP module docking port
D	Compute module power connectors
E	Management risers

12. Platform Management

The Intel® Server D50DNP Family uses the baseboard management controller (BMC) features of an Aspeed AST2600* server management processor (SMP). The BMC supports multiple system management functions including intra-system sensor monitoring, fan speed control, system power management, and system error handling and messaging. It also provides remote platform management capabilities including remote access, monitoring, logging, and alerting features.

All server management capabilities can be split in two groups:

- Standard management features (Included)
- Optional advanced management features that can be enabled with the purchase of advanced management license

In addition, BMC integrates with the Intel® Data Center Manager (DCM) software to provide unified management at Data Center level.

The following subsections provide a brief description of each.

12.1 Management Port

The Intel® D50DNP Modules include a 1 Gb Ethernet RJ45 port used to access embedded system management features remotely.

Note: The management port is dedicated for system management access purposes only. The port is not intended or designed to support standard LAN data traffic.

For more information on the server management port, including LED definition, see Section 9.2.1.2.

Figure 46. Dedicated Management Port – 2U PCIe* Accelerator Module

12.1.1 Configuring System Management Port Using BIOS Setup Utility

Before the 1 Gb Ethernet port can be used for remote management, it must be configured in the BIOS Setup Utility.

1. After the server completes the POST process, press the <F2> key on the keyboard to go to the BIOS Setup utility.
2. Navigate to the **Server Management** tab and select **BMC LAN Configuration** to enter the BMC LAN Configuration screen.

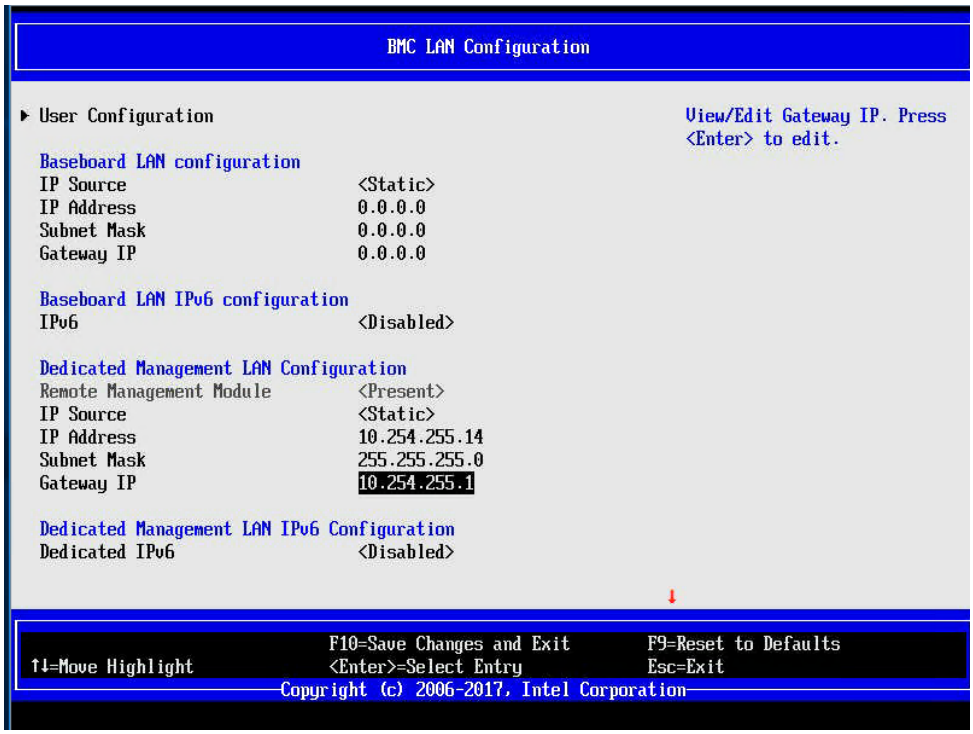


Figure 47. BMC LAN Configuration Screen of the BIOS Setup Utility

3. Use the **Dedicated Management LAN Configuration** section to set parameters for an IPv4 network:
   - If Static is selected as the IP source, enter the IP address, Subnet mask, and Gateway IP as needed.
4. Use the **Dedicated Management LAN IPv6 Configuration** section to set parameters for an IPv6 network:
   - Navigate to the Dedicated IPv6 field and then select Enabled. Then scroll to IPV6 source and select either Static or Dynamic. If Static is selected, configure the IPV6 address, Gateway IPV6, and IPV6 Prefix Length as needed.

Note: The IP parameters entered at the steps above will not be shown in the BIOS Setup Utility after server is restarted if the 1Gb Ethernet port is not connected to the live network. The IP parameters are retained and will be visible again after the port gets connected. They also can be visible in the BMC Web Console.

---

5. Select **User Configuration** to enter the User Configuration screen.

Figure 48. User Configuration Screen of the BIOS Setup Utility

6. Under vacant **User ID**, enter desired username.
7. Press **<F10>** key and **Y** to save changes and restart the server.
8. After the server completes the POST process, press the **<F2>** key on keyboard to go to the BIOS Setup utility.
9. Navigate to the **Server Management > BMC LAN Configuration > User Configuration**
10. Enter the following settings for the new user as desired:
    - **Privilege** – Select the privilege to be used. (Administrator privilege is required to use KVM or media redirection).
    - **User Status** – Select **Enabled**.
    - **User password** – Enter the desired password twice.
11. Press **<F10>** and **Y** to save the configured settings and exit BIOS Setup. The server reboots with the new user account settings.

Note: `Root` word is reserved and cannot be used as a username.

Password must have a length of 8–20 characters. It must contain both upper and lower case letters, numbers, and special characters.

Once the management port is configured, the server can be accessed remotely to perform system management functions defined in the following sections.

12.2 Standard System Management Features

The following system management features are supported on the Intel® Server D50DNP Family by default.

- Integrated BMC Web Console
- Redfish* interface
- Support for IPMI 2.0 protocol and Intel® Dynamic Power Node Manager
- Out-of-band BIOS/BMC Update and Configuration
- System Inventory

- Autonomous Debug Log

The following subsections provide a brief description for each feature.

12.2.1 Integrated BMC Web Console

The BMC firmware includes an embedded web server that can serve web pages to any supported browser. This web console is designed to be a fully functional server administration tool and allows a system administrator to:

- View system information including firmware versions, server health, diagnostic information, and power statistics.
- Configure BMC options
- Perform power actions (power on, power off, etc.)
- Launch the KVM and media redirection application

To access Integrated BMC Web Console over secure connection, enter the configured IP address of the BMC management port into the web browser to open the Integrated BMC Web Console module login page.

```
https://<IPaddress_of_BMC_management_port>/
```

Enter the username and password, then select a language option from the drop-down list. For example, English.

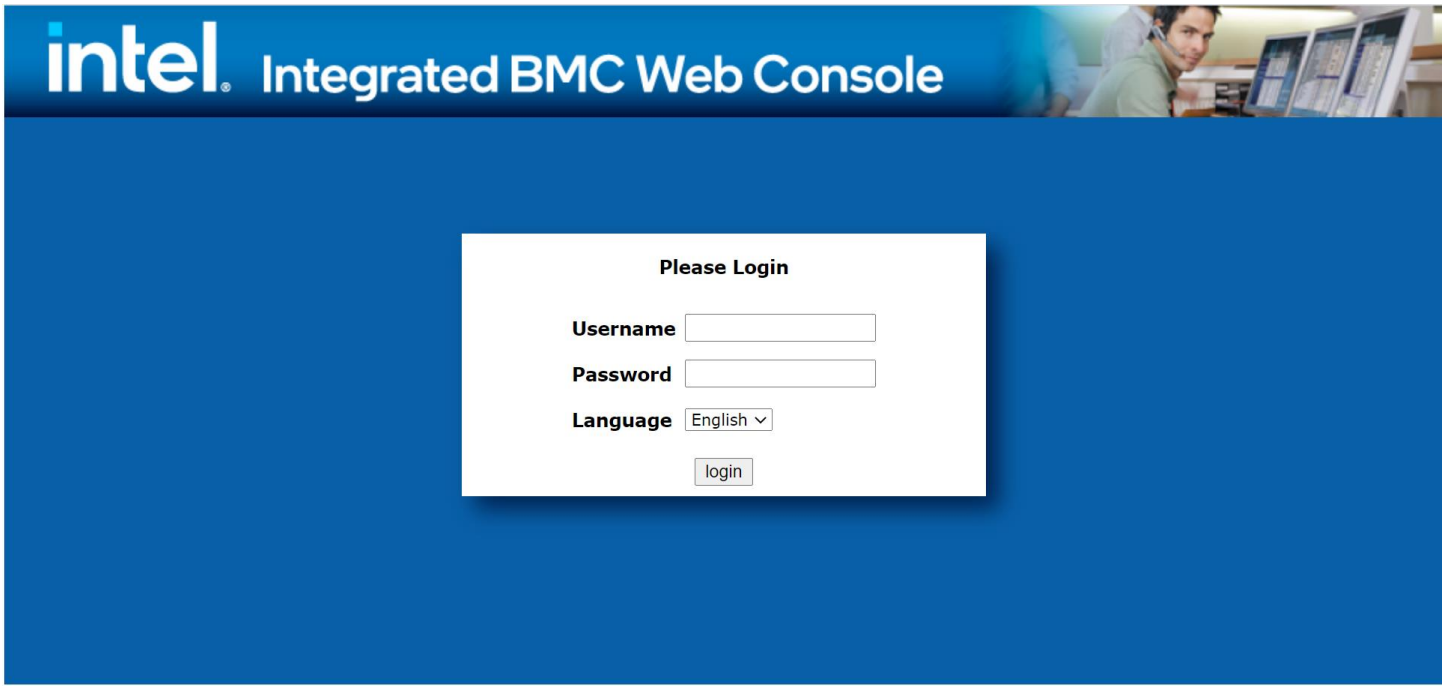


Figure 49. Integrated BMC Web Console Login Page

Click the **Login** button to view the “System” page.

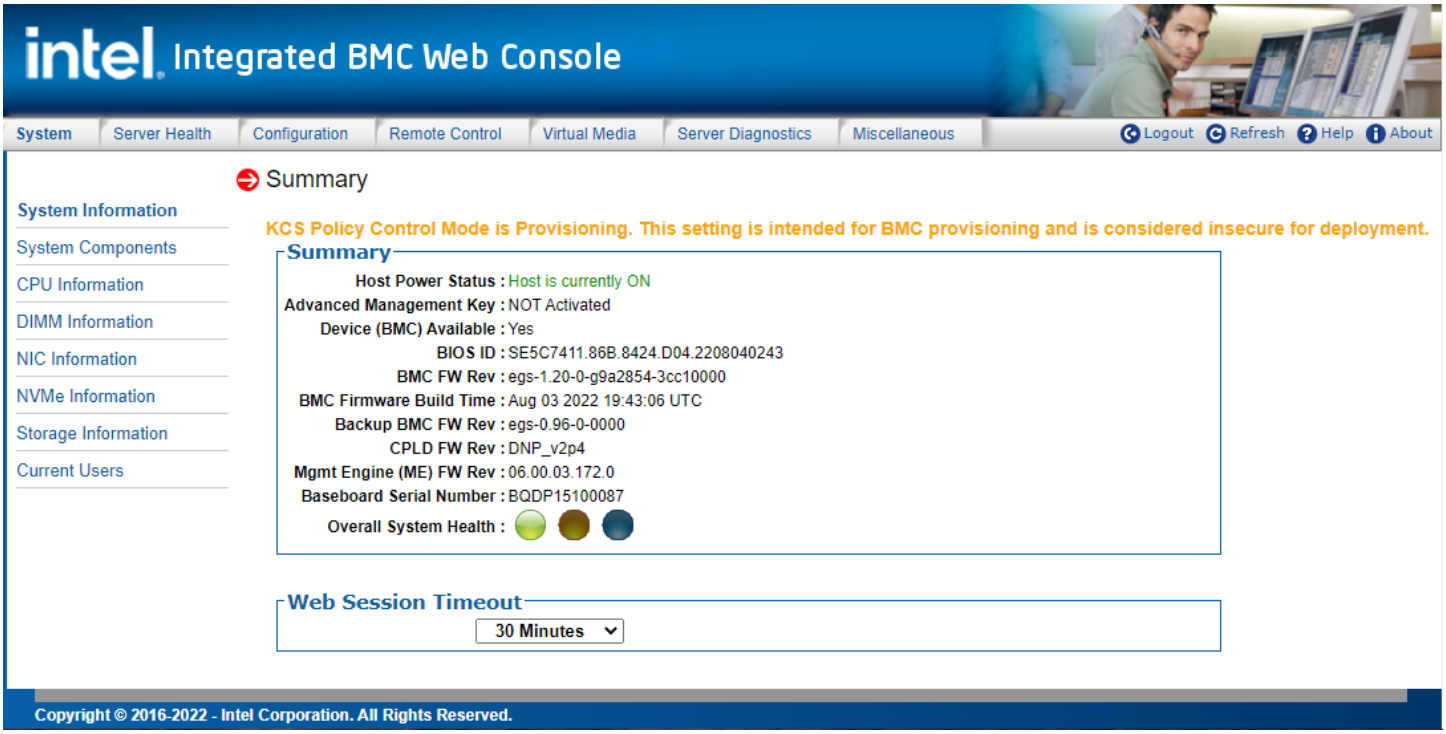


Figure 50. Integrated BMC Web Console – System Information View

For additional information about BMC Web Console, refer to the *Integrated Baseboard Management Controller Web Console User Guide for Intel® Server Systems based on the 4th Gen of Intel® Xeon® Scalable Processors Family*.

12.2.2 Redfish* Support

DMTF's Redfish* is a standard designed to deliver simple and secure management for converged, hybrid IT and the Software Defined Data Center (SDDC). Both human readable and machine capable, Redfish* leverages common Internet and web services standards to expose information directly to the modern tool chain. The BMC currently supports API version 1.15 and schema version 2021.4.

12.2.3 IPMI 2.0 Support

The BMC is IPMI 2.0 compliant, including support for Intel® Dynamic Power Node Manager. IPMI defines a set of interfaces used by system administrators for out-of-band management of computer systems and monitoring of their operation.

12.2.4 Out-of-Band BIOS / BMC Update and Configuration

The BMC allows administrators to update the CPLD, BMC, and BIOS firmware using either Redfish* schemas or embedded web console. The BMC firmware also includes firmware modules for server Power Supplies and PCIe* retimers. The firmware images are loaded into BMC staging area and programmed into a SPI flash under control of PFR on next reboot.

The BMC also supports Redfish schemas to view and modify BIOS settings. On each boot, the BIOS provides all its settings and active value to the BMC to be displayed. BIOS also checks if any changes are requested and performs those changes.

12.2.5 System Inventory

The BMC supports Redfish schemas and embedded web console pages to display system inventory. This inventory includes FRU information, processor, memory, NVMe*, networking, and storage. When applicable, the firmware version is also provided.

12.2.6 Autonomous Debug Log

The BMC collects and stores information from different server subsystems:

- configuration data about BMC, PCIe, power supply including power supply “black box” data
- SMBIOS data
- Redfish Event Log (SEL)
- POST codes from the last two system boots

When the system has a catastrophic error condition leading to a system shutdown, the BMC will hold the CPU in reset long enough to collect processor machine check registers, memory controller machine check registers, I/O global error registers, and other processor state info.
All this information can be retrieved as a single archive called Debug Log from the Redfish, embedded web console or using the Intel® Server Configuration Utility and Intel® Server Debug and Provisioning Tool (Intel® SDP Tool) utilities.

12.2.7 Security Features

The BMC supports several security features including ecurity logs, ability to turn off any remote port, Secure Sockets Layer (SSL) certificate upload, VLAN support, and KCS control. The BMC also supports full user management with the ability to define password complexity rules. Each BMC release is given a security version number to prevent firmware downgrades from going to lower security versions. Intel provides a best practices security guide, available at:

https://www.intel.com/content/www/us/en/support/articles/000055785/server-products.html

12.3 Advanced System Management Features

Installation of an optional Advanced System Management product key (iPC **ADVSYSMGMTKEY**), unlocks these advanced system management features:

- Virtual KVM over HTML5
- Virtual media - redirection of image file stored on local drive of administrator’s workstation
- Virtual media - redirection of files and folders hosted on network share
- Out-of-band hardware RAID management
- Included single system license for Intel® Data Center Manager (Intel® DCM)
  - Intel® DCM is a software solution that collects and analyzes the real-time health, power, and thermals of a variety of devices in data centers, helping the user to improve the efficiency and uptime. For more information, go to https://www.intel.com/content/www/us/en/software/intel-dcm-product-detail.html.

There are two options available to order the Advanced Management License Key (iPC **ADVSYSMGMTKEY**):

- **CTO/L9:** When ordering a fully integrated system from Intel using its on-line Configure-to-Order (CTO) tool, select the **AdvSysMgmtKey** as an additional option. The Intel factory will then automatically upload the license key on to the system during the system integration process.
- **Add-on Accessory:** The Advanced Management License Key (iPC **ADVSYSMGMTKEY**) can be ordered separately from the system as an add-on accessory. This option requires that the license key be manually installed on the system. See Appendix I for ordering and installation details.

12.3.1 KVM Redirection

The BMC firmware supports keyboard, video, and mouse redirection (KVM) over LAN. This feature allows a user to interactively use the keyboard, video, and mouse (KVM) functions of his local workstation as if the user were physically present at the managed server. This feature is available from the embedded web server

as an HTML5 application and supports USB1.1 or USB 2.0-based mouse and keyboard. The KVM-redirection (KVM-r) session can be used concurrently with media-redirection (media-r).

KVM redirection supports the following keyboard layouts: English, Chinese (traditional), Japanese, German, French, Spanish, Korean, Italian, and United Kingdom. KVM redirection application includes a “soft keyboard” function. The soft keyboard is used to simulate an entire keyboard on the screen. The soft keyboard supports the following layouts: English, Dutch, French, German, Italian, Russian, and Spanish.

The KVM-redirection feature automatically senses video resolution for best possible screenshot and provides high-precision mouse tracking and synchronization. It allows interaction with a remote managed server during pre-boot POST and in the BIOS setup utility once BIOS has initialized video.

12.3.2 Local Media Redirection

The BMC supports media redirection of local `.IMG` or `.ISO` image files. When a user selects the “Launch Window to Mount Local Image” option, a new web page is displayed.

The page provides the user interface to select which type of image file (.IMG/.IMA or .ISO) to mount. The page then allows the user to select the desired image file to make it available to the managed server. After the type and specific file are selected, the interface provides a plug/unplug function so the user can connect the media to or disconnect the media from the remote server system.

Once connected, the selected image file is presented to the server system as a read-only removable media and may be interacted with like with a CD-ROM drive.

This feature provides system administrators the ability to install software (including operating system), copy files, perform firmware updates, and so on, on a remote server from local media on their workstation.

The following capabilities are supported:

- The operation of remotely mounted devices is independent of the local devices on the server. Both remote and local devices are useable in parallel.
- The image file can be located on different types of devices (CD\DVD-ROM, floppy, USB Flash).
- It is possible to boot all supported operating systems from the remotely mounted disk image (*.IMG) and CD-ROM or DVD-ROM image (*.ISO) files. See the Tested/supported Operating System List for more information.
- A remote media session is maintained even when the server is powered-off (in standby mode). No restart of the remote media session is required during a server reset or power on/off. A BMC reset (for example, due to a BMC reset after BMC firmware update) will require the session to be re-established
- The mounted device is visible to (and useable by) managed system’s OS and BIOS in both pre-boot and post-boot states.
- The mounted device shows up in the BIOS boot order and it is possible to change the BIOS boot order to boot from this remote device.
- The mounted device is presented to a server as a read-only device.

12.3.3 Redirection of files hosted on Network File Server

In addition to supporting virtual media redirection from the administrator’s workstation (see Section 12.3.2), the BMC also supports media redirection of files and folders hosted on a network file server, accessible to the BMC network interface. The current version supports Samba* shares (Microsoft Windows* file shares) and NFS shares.

This virtual media redirection is more effective for mounting virtual media at scale, instead of processing all files from the workstation’s drive through the HTML5 application and over the workstation’s network. Each

BMC makes a direct network file share connection to the file server and accesses files across that network share directly.

12.3.4 Intel® Data Center Manager (Intel® DCM) Support

Intel® DCM is a solution for out-of-band monitoring and managing the health, power, and thermals of servers and a variety of other types of devices.

Intel® DCM allows the user to:

- Automate health monitoring
- Improve system manageability
- Simplify capacity planning
- Identify underutilized servers
- Measure energy use by device
- Pinpoint power/thermal issues
- Create power-aware job scheduling tasks
- Increase rack densities
- Set power policies and caps
- Improve data center thermal profile
- Optimize application power consumption
- Avoid expensive PDUs and smart power strips

For more information, go to:

https://www.intel.com/content/www/us/en/software/intel-dcm-product-detail.html

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Note: See Section 1.2 for references to the *Intel® Data Center Manager (Intel® DCM) Product Brief* and *Intel® Data Center Manager (Intel® DCM) Console User Guide*.

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13. System Firmware and Utilities

The Intel® Server D50DNP Family includes a system software stack that consists of the following components:

- Complex Programmable Logic Device (CPLD) controlling low level board functions
- System BIOS
- BMC firmware
- Intel® Management Engine (Intel® ME) firmware / Intel® Server Platform Services (Intel® SPS) / Intel® Platform Controller Hub Ignition Firmware (Intel® PCH Ignition Firmware)
- Field-replaceable unit (FRU) data

Together, they configure and manage features and functions of the server system.

Many features and functions of the server system are managed jointly by the system BIOS and the BMC firmware, including:

- Intelligent Platform Management Interface (IPMI) watchdog timer
- Messaging support, including command bridging and user/session support
- BIOS boot flags support
- Event receiver device: The BMC receives and processes events from the BIOS.
- Serial-over-LAN (SOL)
- ACPI state synchronization: The BMC tracks ACPI state changes that are provided by the BIOS.
- Fault resilient booting (FRB): Fault resilient boot level 2 (FRB-2) is supported by the watchdog timer functionality.
- Front panel management: The BMC controls the system status LED and system ID LED. It supports secure lockout of certain front panel functionality and monitors button presses. The system ID LED can be turned on using a front panel button or a command.
- DIMM temperature monitoring: new sensors and improved acoustic management using closed-loop fan control algorithm comprehending DIMM temperature readings.
- Intel® Intelligent Power Node Manager support
- Integrated KVM (keyboard, video, and mouse)
- Integrated remote media redirection
- Additions/enhancements to the system event log (SEL) logging (for example, additional thermal monitoring capability)
- Embedded platform debug feature that allows capture of detailed data for later analysis by Intel
- Intel® PCH Ignition Firmware featuring a small footprint with support for platform boot and security features for PCH Intel® ME. Delivered as configurable binary.

A factory installed system software stack is pre-programmed on each server module. However, later revisions may be available. To ensure optimal system operation, Intel recommends the following:

- Power up the module and access the onboard BIOS setup utility to verify the version numbers of the installed system software stack: CPLD, BIOS, BMC firmware, Intel® ME firmware, and FRU.
- Check the following Intel website for possible updates: http://downloadcenter.intel.com.
- Download and update the software stack if later revisions are available.

System updates can be performed in several operating environments, including the UEFI shell using the UEFI-only system update package (SUP); or, under different operating systems, using Redfish schemas and online tools.

See the following Intel documents for more in-depth information concerning the system software stack and its functions:

- *BIOS Firmware External Product Specification (EPS)* – Intel NDA is required
- *Integrated Baseboard Management Controller Firmware External Product Specification* – Intel NDA is required

13.1 Hot Keys Supported during POST

Certain hot keys are recognized during power-on self-test (POST). A hot key is a key or key combination that is recognized as an unprompted command input. In most cases, hot keys are recognized even while other processing is in progress.

Hot keys supported by the BIOS are only recognized by the system BIOS during the system boot time POST process. Once the POST process has completed and transitions the system boot process to the operating system, BIOS-supported hot keys are no longer recognized. The time period when POST accepts a hot key is defined by the value in the System Boot Timeout parameter of the BIOS Setup Utility. To change the value, navigate to **Boot Maintenance Manager > Advanced Boot Options > System Boot Timeout** and set desired value

The following table provides a list of available POST hot keys along with a description for each.

Table 33. POST Hot Keys

Hot Key	Function
<F2>	Enter the BIOS setup utility
<F6>	Invoke BIOS boot menu
<F12>	Network boot
<Esc>	Switch from logo screen to diagnostic screen
<Pause>	Stop POST temporarily (press any key to resume)

13.1.1 POST Logo/Diagnostic Screen

If the Quiet Boot item is enabled in the BIOS setup utility, a splash screen is displayed with the standard Intel logo screen; or a customized original equipment manufacturer (OEM) logo screen if one is present in the designated flash memory location. By default, Quiet Boot is enabled in the BIOS setup utility and the logo screen is the default POST display. However, pressing **<Esc>** hides the logo screen and displays the diagnostic screen instead during the current boot.

If a logo is not present in the BIOS flash memory space, or if Quiet Boot is disabled in the system configuration, the POST diagnostic screen is displayed with a summary of system configuration information. The POST diagnostic screen is purely a text mode screen, as opposed to the graphics mode logo screen.

If console redirection is enabled in the BIOS setup utility, the Quiet Boot setting is disregarded, and the text mode diagnostic screen is displayed unconditionally. This situation is due to the limitations of console redirection that transfers data in a mode that is not graphics-compatible.

13.1.2 BIOS Boot Pop-Up Menu

The BIOS boot selection (BBS) menu provides a boot device dialog menu that is invoked by pressing the **<F6>** key during POST. The BBS dialog menu displays all available boot devices. The boot order in the dialog menu is different from the boot order in the BIOS setup utility. The dialog menu simply lists all the available devices from which the system can be booted and allows a manual selection of the desired boot device.

When an administrator password is configured in the BIOS setup utility, the administrator password is required to access the boot dialog menu. If a user password is entered, the user is taken directly to the boot manager in the BIOS setup utility, only allowing booting in the order previously defined by the administrator.

13.1.3 Entering the BIOS Setup Utility

To enter the BIOS setup utility using a keyboard (or emulated keyboard), press the **<F2>** function key during boot time when the OEM, or Intel logo screen, or the POST diagnostic screen is displayed.

The following instructional message is displayed on the diagnostic screen or above the quiet boot logo screen:

Press [Enter] to directly boot.
Press [F2] to enter setup and select boot options.
Press [F6] to show boot menu options.
Press [F12] to boot from network.

Note: With a USB keyboard, it is important to wait until the BIOS discovers the keyboard. Until the USB controller has been initialized and the keyboard activated, key presses are not read by the system.

The top-level menu of the BIOS Setup utility is displayed initially. However, if a serious error occurs during POST, the system enters the error manager screen instead of the top-level menu screen.

For additional BIOS setup utility information, see the *BIOS Setup Utility User Guide*.

13.1.4 BIOS Update Capability

To bring BIOS fixes or new features into the system, it is necessary to replace the current installed BIOS image with an updated one. Full BIOS update instructions are provided with update packages downloaded from the Intel website.

13.2 Field-Replaceable Unit (FRU) Data

As part of the manufacturing process, FRU data is loaded into the Intel® D50DNP Modules. This action ensures that the embedded platform management system can monitor the appropriate sensor data and operate the system with the best cooling and performance. This process also ensures that auto-configuration occurs without the need to perform additional SDR updates or provide other user input to the system when any of the following components are added or removed:

- Module
- Memory
- Power supply
- Fan
- Power distribution board

Intel recommends updating the FRU data to the latest available version whenever a system software update is performed.

13.2.1 Loading FRU Data

The FRU data can be updated using a stand-alone sysfwupdt utility in the UEFI shell or under a supported operating system.

Full FRU update instructions are provided with the appropriate SUP that can be downloaded from: http://downloadcenter.intel.com.

13.3 System Update Package (SUP) for Intel® Server D50DNP Family

The SUP is a set of utilities and firmware files bundled together and used to update the system BIOS and other embedded system firmware. Included in the compressed file package is a “Read Me” file providing complete system update instructions and a `STARTUP.NSH` script file that automates the entire system

update process with little or no user intervention. There are two versions of the package: one for the UEFI shell and another for Linux and Windows operating systems.

The latest SUP can be downloaded from: http://downloadcenter.intel.com.

13.4 Intel® Server Configuration Utility

The Intel® Server Configuration Utility is a command-line interface that supports the following features:

- Save selective BIOS and/or firmware settings to a file
- Write BIOS and firmware settings from a file to a server
- Configure selected firmware settings
- Configure selected BIOS settings
- Configure selected system settings
- Display selected firmware settings
- Display selected BIOS settings

For further Intel® Server Configuration Utility information, refer to the *Intel® Server Configuration Utility User Guide.*

13.5 Intel® Server Firmware Update Utility

The Intel® Server Firmware Update Utility provides the ability to update the system BIOS and firmware while the server is running its host operating system. This utility is a command-line tool and it requires users to have administrator (Windows*) or root (Linux*) privileges.

The Intel® Server Firmware Update Utility supports the following features:

- BIOS update – the tool transfers the bin file to the BMC staging area. The real update starts on next reboot by default.
- BMC update – updates server management (SM) firmware of the baseboard management controller (BMC), and on the next BMC reset the new BMC firmware is loaded.
- Recovery update
- Modify specific FRU field
- Display BIOS/Intel® ME/BMC/base board/system/FRU/ SMBIOS information
- Restore BIOS default settings

For further Intel® Server Firmware Update Utility information, refer to the *Intel® Server Firmware Update Utility User Guide.*

13.6 Intel® Server Information Retrieval Utility

The Intel® Server Information Retrieval Utility is a command-line interface that provides the ability to collect system information, as fully described in the IPMI and BMC specifications. Running the utility requires that the user have Windows* administrator or Linux* root permissions.

The Intel® Server Information Retrieval Utility collects the following system information and writes the data to a log file:

- Platform firmware inventory
- Sensors
- Sensor data records (SDRs)
- Baseboard FRU
- System boot order
- BMC user settings
- BMC LAN channel settings
- BMC SOL channel settings
- BMC power restore policy settings

- BMC channel settings
- SMBIOS type 1, type 2, type 3
- Memory
- Processor
- Storage devices
- Operating system information
- Device manager information (such as drivers)
- List of software installed
- Operating system event log
- PCI bus device information
- RAID settings and RAID log
- BIOS settings (per the BIOS setup)
- Power telemetry (if available)

For further Intel® Server Information Retrieval Utility information, refer to the *Intel® Server Information Retrieval Utility User Guide.*

13.7 Intel® Server Debug and Provisioning Tool (Intel® SDP Tool)

The Intel® Server Debug and Provisioning Tool (Intel® SDP Tool) is a single server command-line tool that communicates with the BMC out-of-band to perform debug and provisioning tasks. It does not require any agents, operating system, or host network on the remote server and can be scripted to run on multiple systems at the same time. The Intel® SDP Tool is also used by Intel® Data Center Manager and other software plugins to perform provisioning tasks.

Supported features include:

- Update BMC, BIOS, Intel® ME, and FRU.
- Deploy an EFI-based custom payload. Custom payloads can perform firmware updates of other components, configure RAID, or collect logs.
- Configure BIOS and BMC settings.
- Download/view SEL, sensors, and debug log.
- Mount virtual media images (ISO and USB).
- Check online for latest BIOS and BMC versions for a given platform.
- View system inventory (CPU, memory, storage, networking).
- View firmware versions.
- Perform power actions.

14. System Security

The Intel® Server D50DNP Family supports a variety of security options designed to prevent unauthorized access to or tampering with system settings. Security options supported include:

- Password protection
- Front panel lockout
- Intel® Platform Firmware Resilience (Intel® PFR) Technology
- Intel® Software Guard Extensions (Intel® SGX) Technology
- Intel® Total Memory Encryption – Multi-Key (Intel® TME-MK) Technology
- Trusted platform module (TPM) support
- Intel® CBnT - Converged Boot Guard and Intel® Trusted Execution Technology (Intel® TXT)
- Unified Extensible Firmware Interface (UEFI) secure boot technology

14.1 Password Protection

The BIOS setup utility includes a Security tab where options to configure passwords, front panel lockout, and TPM settings are found.

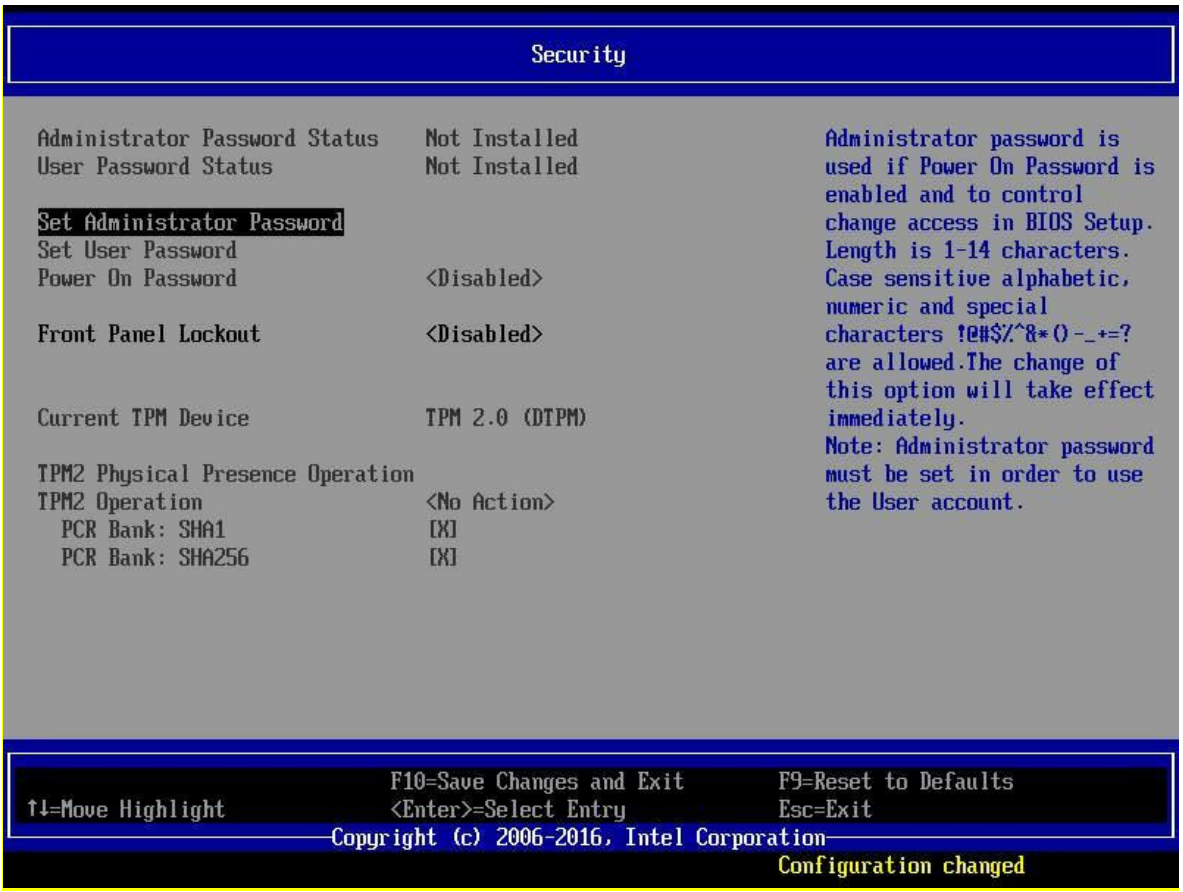


Figure 51. Security Tab of the BIOS Setup Utility

14.1.1 Password Setup

The BIOS uses passwords to prevent unauthorized access to the server modules. Passwords can restrict entry to the BIOS setup utility, restrict use of the Boot Device menu during POST, suppress automatic USB device reordering, and prevent unauthorized system power-on.

Intel strongly recommends that an administrator password is set. A system with no administrator password set allows anyone who has access to the server module to change BIOS settings. An administrator password must be set before the user password can be set.

The maximum length of a password is 14 characters. The minimum length is one character. Passwords are case sensitive. The password can be made up of a combination of alphanumeric (a-z, A-Z, 0–9) characters and any of the following special characters:

```
! @ # $ % ^ & * ( ) - _ + = ?
```

Passwords are case-sensitive.

The administrator and user passwords must be different from each other. An error message is displayed, and a different password must be entered if there is an attempt to enter the same password for both.

The use of strong passwords is encouraged, but not required. To meet the criteria for a strong password, the password entered must be at least eight characters in length, it also must include at least one each of alphabetical, numeric, and special characters. If a weak password is entered, a warning message is displayed, and the weak password is accepted.

Once set, a password can be cleared by changing it to a null string. This procedure requires the administrator password and must be done through the BIOS setup utility. Clearing the administrator password also clears the user password. Passwords can also be cleared by using the password clear jumper on the server board. For more information on the password clear jumper, see Section 15.2.

Resetting the BIOS configuration settings to default values (by any method) has no effect on neither the administrator password nor the user password.

As a security measure, if a user or administrator enters an incorrect password three times in a row during the boot sequence, the system is placed into a halt state. A system reset is required to exit out of the halt state. This feature makes it more difficult to guess or break a password.

In addition, on the next successful reboot, the Error Manager displays the major error code `0048`. An Redfish event is also logged to alert the authorized user or administrator that a password access failure has occurred.

14.1.2 System Administrator Password Rights

When the correct administrator password is entered, the user may perform the following actions:

- Access the BIOS setup utility.
- Configure all BIOS setup utility options in the BIOS setup utility.
- Clear both the administrator and user passwords.
- Access the Boot Menu during POST.

If the Power On Password function is enabled in the BIOS setup utility, the BIOS halts early during POST to request a password (administrator or user) before continuing the POST.

14.1.3 User Password Rights and Restrictions

When the correct user password is entered, the user can perform the following actions:

- Access the BIOS setup utility.
- View, but not change, any BIOS setup utility options in the BIOS setup utility.
- Modify system time and date in the BIOS setup utility.

If the Power On Password function is enabled in the BIOS setup utility, the BIOS halts early in POST to request a password (administrator or user) before continuing POST.

Configuring an administrator password imposes restrictions on booting the system and configures most setup fields to read-only if the administrator password is not provided. The boot dialog menu requires the administrator password to function, and the USB reordering is suppressed as long as the administrator

password is enabled. Users are restricted from booting in anything other than the boot order defined in setup by an administrator.

14.2 Front Panel Lockout

If enabled in the BIOS setup utility from the Security screen, this option disables the following front panel features:

- The off function of the power button.
- System reset button.

If the Front Panel Lockout item is enabled, power off and reset must be controlled through a system management interface.

14.3 Intel® Platform Firmware Resilience (Intel® PFR) 3.0

As the intensity, sophistication, and disruptive impact of security attacks continue to escalate, data centers are driving a holistic approach to protect their critical infrastructure. This approach includes protecting server systems at the firmware level, the lowest layers of the platform, where threats are most difficult to detect.

To address this situation, Intel has developed the Intel® Platform Firmware Resilience (Intel® PFR) technology. With Intel® PFR, platforms can provide security starting with power-on, system boot, and operating system load activities.

The Intel® Server D50DNP Family supports the Intel® PFR technology, a hardware-enhanced platform security that uses an Intel® FPGA to protect, detect, and recover platform firmware.

- **Protect:** Monitors and filters malicious traffic on system buses. All platform firmware is attested safe before code execution.
- **Detect:** Verifies integrity of platform firmware images before executing. Performs boot and runtime monitoring to assure that the server is running a known good firmware.
- **Recover:** Automatically restores corrupted firmware from a protected gold recovery image within minutes.

Critical firmware elements protected in an Intel® Server D50DNP Family include: BIOS, SPI descriptor, BMC, Intel® Management Engine (Intel® ME), and power supply firmware. This capability to mitigate firmware corruption is an important industry innovation and provides an optimal solution for security-sensitive organizations.

Intel® PFR fully supports the firmware resiliency guidelines (SP800-193) proposed by the National Institute of Standards and Technology (NIST*). These firmware resiliency guidelines have wide industry support.

14.4 Intel® Total Memory Encryption – Multi-Key (Intel® TME-MK)

To better protect computer system memory, the 4th Gen Intel® Xeon® Scalable processor has a security feature called Intel® Total Memory Encryption – Multi-Key (Intel® TME-MK). This feature is supported on the Intel® Server D50DNP Family. Intel® TME-MK helps to ensure that all memory accessed from the Intel® processors is encrypted, including customer credentials, encryption keys, and other IP or personal information.

Intel developed this feature to provide greater protection for system memory against hardware attacks, such as removing and reading the dual in-line memory module after spraying it with liquid nitrogen or installing purpose-built attack hardware. Using the NIST storage encryption standard AES XTS, an encryption key is

generated using a hardened random number generator in the processor without exposure to software. This procedure allows existing software to run unmodified while better protecting memory.

Intel® TME-MK builds on Intel® TME and adds support for multiple encryption keys. The system on chip (SoC) implementation supports a fixed number of encryption keys. Software can configure the SoC to use a subset of available keys. Software manages the use of keys and can use each of the available keys for encrypting any page of the memory. Thus, Intel® TME-MK allows page granular encryption of memory. Intel® TME-MK can be enabled directly in the server BIOS and is compatible with Intel® Software Guard Extensions (Intel® SGX) application enclave solutions.

Intel® TME-MK has the following characteristics:

- **Encrypts** the entire memory using AES-XTS, a NIST standard "storage-class" algorithm for encryption.
- **Transparent to software**, it encrypts data before writing to server memory and then decrypts on read.
- **Easy enablement** that requires no operating system or application enabling and is applicable to all operating systems.

To enable/disable Intel® TME-MK, access the BIOS setup utility menu by pressing **<F2>** key during POST. Navigate to the following menu: **Advanced > Processor Configuration**

Important Note: When Intel® TME-MK is enabled, some memory RAS features are disabled. See Table 13 for details.

For more information on Intel® TME-MK, see the *BIOS Setup Utility User Guide* and the *BIOS Firmware External Product Specification).*

14.5 Intel® Software Guard Extensions (Intel® SGX)

Intel® Software Guard Extensions (Intel® SGX) is a set of instructions that increases the security of application code and data, giving them more protection from disclosure or modification. Developers can partition sensitive information into enclaves that are areas of execution in memory with more security protection.

Intel® SGX helps protect selected code and data from disclosure or modification. Intel® SGX helps partition applications into enclaves in memory that increase security. Enclaves have hardware-assisted confidentiality and integrity-added protections to help prevent access from processes at higher privilege levels. Through attestation services, a relying party can receive some verification on the identity of an application enclave before launch.

The Intel® Server D50DNP Family provides Intel® SGX as part of the platform system security. Intel® SGX provides fine grain data protection via application isolation in memory. Data protected includes: code, transactions, IDs, keys, key material, private data, algorithms. Intel® SGX provides enhanced security protections for application data independent of operating system or hardware configuration.

Intel® SGX provides the following security features:

- **Helps protect against attacks on software**, even if operating system, drivers, BIOS, VMM, or SMM are compromised.
- **Increases protections for secrets**, even when the attacker has full control of the platform.
- **Helps prevent attacks**, such as memory bus snooping, memory tampering, and cold boot attacks, against memory contents in RAM.
- **Provides an option for hardware-based attestation** capabilities to measure and verify valid code and data signatures.

Intel® SGX for Intel® Xeon® Scalable processors is optimized to meet the application isolation needs of server systems in cloud environments:

- Massively increased enclave page cache (EPC) size (up to 1 TB for a typical dual-socket server system).
- Significant performance improvements: minimal impact versus built-in, non-encrypted execution (significantly reduced overhead depending on the workload).
- Fully software and binary-compatibility with applications written on other variants of Intel® SGX.
- Support for deployers to control which enclaves can be launched.
- Provides deployers full control over attestation stack, compatible with Intel® Software Guard Extensions Data Center Attestation Primitives (Intel® SGX DCAP).
- Full protection against cyber (software) attacks, some reduction in protection against physical attacks (no integrity/anti-replay protections) versus other Intel® SGX variants.
- Designed for environments where the physical environment is still trusted.

Note: Intel® SGX can only be enabled when Intel® TME is enabled. See Section 14.4 to enable Intel® TME.

To enable/disable Intel® SGX, access the BIOS setup utility menu by pressing the **<F2>** key during POST. Navigate to the following menu: **Advanced > Processor Configuration**.

Important Note: When Intel® TME is enabled, a subset of memory RAS features is disabled. See Table 13 for details.

For more information about Intel® SGX, see the *BIOS Setup Utility User Guide* and *BIOS Firmware External Product Specification.*

14.6 Trusted Platform Module (TPM) 2.0 Support

The trusted platform module (TPM) option is a hardware-based security device that addresses the growing concern about boot process integrity and offers better data protection. A TPM protects the system startup process by ensuring that it is tamper-free before releasing system control to the operating system.

A TPM device provides secured storage to store data, such as security keys and passwords. In addition, a TPM device has encryption and hash functions. The Intel® D50DNP Modules support TPM in compliance with the *TPM PC Client Specifications, Revision 2.0*, published by the Trusted Computing Group (TCG).

A TPM device can be optionally installed on the Intel® D50DNP Modules. The TPM device is installed on to a connector on the server board and is secured using a tamper resistant screw to prevent physical theft and tampering of the device.

A pre-boot environment, such as the BIOS and operating system loader, uses the TPM to collect and store unique measurements from multiple factors in the boot process to create a system fingerprint. This unique fingerprint remains the same unless the pre-boot environment is tampered with. Therefore, it is used to compare to future measurements to verify the integrity of the boot process.

After the BIOS completes the measurement of its boot process, it hands off control to the operating system loader and, in turn, to the operating system. If the operating system is TPM-enabled, it compares the BIOS TPM measurements to the measurements of previous boots to make sure that the system was not tampered with before continuing the operating system boot process.

Once the operating system is in operation, it optionally uses the TPM to provide additional system and data security (for example, the BitLocker* drive encryption utility in Microsoft Windows* uses the TPM to store cryptographic keys).

Intel offers the following TPM kits for Intel® D50DNP Modules:

- Trusted platform module 2.0 (China version) – iPC **AXXTPMCHNE8** (accessory part)
- Trusted platform module 2.0 (rest of world) – iPC **AXXTPMENC9** (accessory part)

14.6.1 BIOS Support for Trusted Platform Module (TPM)

The BIOS TPM support conforms to the *TCG PC Client Specific Implementation Specification for Conventional BIOS*, the *TCG PC Client Specific TPM Interface Specification*, and the *Microsoft Windows BitLocker Requirements*.

The TPM support by BIOS includes the following:

- Measures and stores the fingerprint of the boot process in the TPM microcontroller allowing an operating system to verify system boot integrity.
- Provides UEFI-compliant APIs to a TPM-enabled operating system for using TPM.
- Generates ACPI table for TPM device allowing a TPM-enabled operating system to administer TPM through the BIOS.
- Verifies operator physical presence.
- Provides BIOS Setup options to change TPM security states and to clear TPM ownership.

For additional details, consult the *TCG PC Client Specific Implementation Specification*, the *TCG PC Client Platform Physical Presence Interface Specification*, and the *Microsoft Windows BitLocker Requirements* documents.

14.6.2 Physical Presence

Before administrative operations to the TPM can be executed, the operator must confirm TPM ownership by verifying his physical presence. The BIOS implements the operator presence indication by verifying the administrator password.

A TPM administrative sequence invoked from the operating system proceeds as follows:

1. A user makes a TPM administrative request through the operating system's security software.
2. The operating system requests the BIOS to execute the TPM administrative command through TPM ACPI methods and then resets the system.
3. The BIOS verifies the physical presence and confirms the command with the operator.
4. The BIOS executes TPM administrative command, inhibits BIOS setup utility entry, and boots directly to the operating system that requested the TPM command.

14.6.3 TPM Security Setup Options

The Security page in the BIOS setup utility allows the operator to view the current TPM state and to carry out rudimentary TPM administrative operations. Performing TPM administrative options through the BIOS Setup requires TPM physical presence verification.

The operator can turn TPM functionality on or off and clear the TPM ownership contents. After the requested TPM BIOS Setup operation is carried out, the **TPM2 Operation** field in the BIOS Setup utility reverts to "No Operation".

The BIOS TPM setup also displays the current state of the TPM, whether TPM is enabled or disabled and activated or deactivated. While using TPM, a TPM-enabled operating system or application may change the TPM state independently of the BIOS Setup. When an operating system modifies the TPM state, the BIOS Setup displays the updated TPM state.

The BIOS Setup **TPM Clear** option allows the operator to clear the TPM ownership key and allows the operator to take control of the system with TPM. This option is used to clear security settings for a newly initialized system or to clear a system for which the TPM ownership security key was lost.

14.7 Intel® CBnT – Converged Intel® Boot Guard and Intel® Trusted Execution Technology (Intel® TXT)

Previous generations of Intel server products supported Intel® Boot Guard and Intel® Trusted Execution Technology (Intel® TXT).

Intel® Boot Guard

- Provides mechanism to authenticate the initial BIOS code, before the BIOS starts.
- Hardware-based Static Root of Trust for Measurement (SRTM).
- Defends against attackers replacing or modifying the platform firmware.

Intel® TXT

- Provides the ability to attest the authenticity of a platform configuration and operating system environment; establishes trust.
- Hardware-based Dynamic Root of Trust for Measurement (DRTM).
- Defends against software-based attacks aimed at stealing sensitive information.

The two security features combined included some redundancies and inefficiencies between them. With this product generation, Intel rearchitected and fused together the two technologies into Converged Intel® Boot Guard and Intel® Trusted Execution Technology. Combining the two technologies into one made them more efficient, eliminated redundancies between them, simplified their implementation, and provided stronger protections.

For more information, visit:

https://www.intel.com/content/www/us/en/support/articles/000025873/technologies.html

14.8 Unified Extensible Firmware Interface (UEFI) Secure Boot Technology

UEFI secure boot technology defines how a platform's firmware can authenticate a digitally signed UEFI image, such as an operating system loader or a UEFI driver stored in an option ROM. This feature provides the capability to ensure that those UEFI images are only loaded in an owner-authorized fashion and provides a common means to ensure platform security and integrity over systems running UEFI-based firmware.

The Intel® Server D50DNP Family BIOS is compliant with the *UEFI Specification 2.3.1* Errata C for the UEFI secure boot feature.

UEFI secure boot requires native UEFI boot mode and it disables the legacy option ROM dispatch. By default, secure boot on the Intel® Server D50DNP Family is disabled.

To enable / disable the UEFI Secure Boot item navigate to: **Boot Maintenance Manager** > **Advanced Boot Options** > **Secure Boot Configuration**.

For more information on UEFI secure boot technology, see the *BIOS Setup Utility User Guide* and the *BIOS Firmware External Product Specification.*

15. Onboard Configuration and Service Jumpers

The server board includes several jumper blocks to configure, protect, or recover specific features of the server board. The following figure identifies the location of each jumper block on the server board. Pin 1 of each jumper is identified by an arrowhead (▼) silkscreened on the server board next to the pin. The following sections describe how each jumper is used.

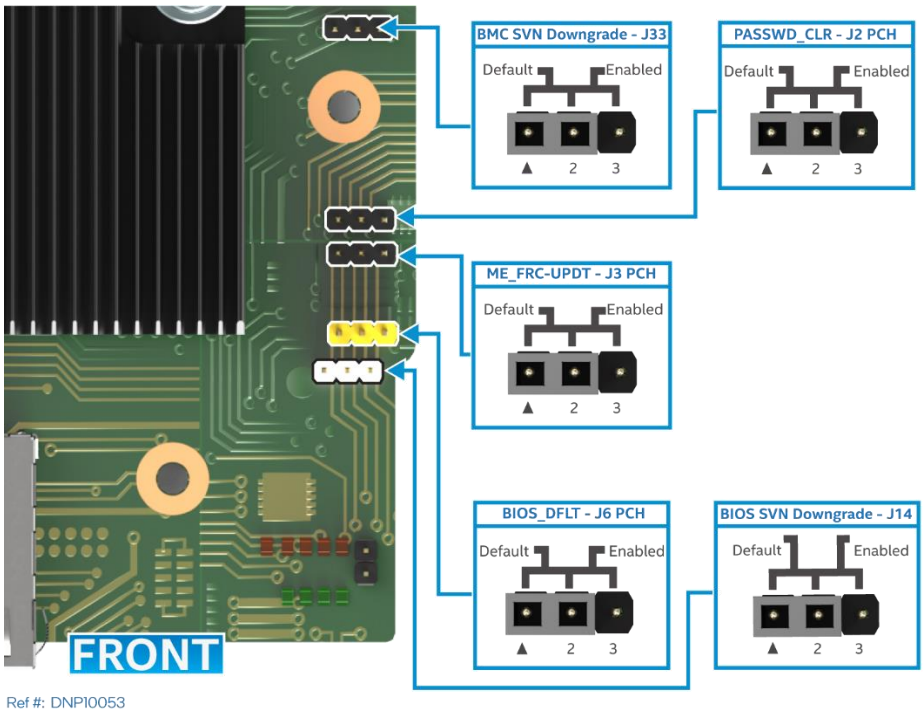


Figure 52. Jumper Block Location

15.1 BIOS Load Defaults Jumper (BIOS_DFLT – J6_PCH)

BIOS options previously configured using the BIOS setup utility are reset back to their original default factory settings when this jumper is used.

Note: This jumper does not reset administrator or user passwords. To reset passwords, the password clear jumper must be used.

To use the BIOS default jumper, perform the following steps:

1. Power down the server module.
2. Remove the server module from the chassis
3. Remove the riser assembly #2 from the server module.
   See the *Intel® Server D50DNP Family Installation and Service Guide* for instructions.
4. Move the `BIOS_DFLT (J6_PCH)` jumper from pins 1–2 (normal operation) to pins 2–3 (set BIOS defaults).
5. Wait five seconds, then move the `BIOS_DFLT (J6_PCH)` jumper back to pins 1–2.
6. Reinstall the riser assembly.
7. Reinstall the server module in the chassis.

Note: The system automatically powers on after AC is applied to the system.

8. When BIOS completes the POST, press **<F2>** to access the BIOS setup utility. Configure and save the desired BIOS options.

After resetting BIOS options using the BIOS default jumper, the Error Manager Screen in the BIOS setup utility displays two errors:

- `0012` System RTC date/time not set
- `5220` BIOS Settings reset to default settings

The system time and date need to be set.

15.2 BIOS Password Clear Jumper (PASSWD_CLR – J2_PCH)

This jumper causes both the user password and the administrator password to be cleared if they were set. The operator must be aware that this situation creates a security gap until passwords have been configured again through the BIOS setup utility.

This jumper is the only method by which the administrator and user passwords can be cleared unconditionally. Other than this jumper, passwords can only be set or cleared by changing them explicitly in the BIOS setup utility. No method of resetting BIOS configuration settings to default values affects neither the administrator password nor user password.

To use the password clear jumper, perform the following steps:

1. Power down the server module.
2. Remove the server module from the chassis
3. Remove the riser assembly #2 from the server module.
   See the *Intel® Server D50DNP Family Installation and Service Guide* for instructions.
4. Move the `PASSWD_CLR (J2_PCH)` jumper from pins 1–2 (default) to pins 2–3 (password clear position).
5. Reinstall the server module in the chassis.
6. Power on the server module and press **<F2>** during POST to access the BIOS setup utility.
7. Verify the password clear operation was successful by viewing the Error Manager screen. Two errors should be logged:
   - `5221` Passwords cleared by jumper
   - `5224` Password clear jumper is set
8. Power down the server module.
9. Remove the server module from the chassis
   See the *Intel® Server D50DNP Family Installation and Service Guide* for instructions.
10. Move the `PASSWD_CLR (J2_PCH)` jumper back to pins 1–2 (default).
11. Reinstall the riser assembly.
12. Reinstall the server module in the chassis.
13. Power up the server module.
14. Intel strongly recommends booting into the BIOS setup utility immediately, navigate to the Security tab, and set the administrator and user passwords if intending to use BIOS password protection.

15.3 Intel® Management Engine (Intel® ME) Force Update Jumper (ME_FRC_UPDT – J3_PCH)

When the Intel® ME firmware force update jumper is moved from its default position, the Intel® ME is forced to operate in a reduced capacity. This jumper must only be used if the Intel® ME firmware has gotten corrupted and requires reinstallation.

Note: The Intel® ME firmware update files are included in the system update packages (SUP) posted to Intel's download center. See Section 1.2.

To use the Intel® ME firmware force update jumper, perform the following steps:

1. Power down the server module.
2. Remove the server module from the chassis
3. Remove the riser assembly #2 from the server module.
   See the *Intel® Server D50DNP Family Installation and Service Guide* for instructions.
4. Move the `ME_FRC_UPDT (J3_PCH)` jumper from pins 1–2 (default) to pins 2–3 (force update position).
5. Reinstall the server module in the chassis.
6. Power on the server module.
7. Boot to the EFI shell.
8. Navigate to the folder containing the update files.
9. Update the Intel® ME firmware using the following command:

   ```
   Sysfwupdt –u <version#>_UpdateCapsule.bin
   ```

10. When the update has successfully completed, power off the server module.
11. Remove the server module from the chassis
12. Move the `ME_FRC_UPDT (J3_PCH)` jumper back to pins 1–2 (default).
13. Reinstall the riser assembly.
14. Reinstall the server module in the chassis.
15. Power on the server module.

15.4 BIOS SVN Downgrade (BIOS SVN Downgrade – J14)

When this jumper is moved from its default pin position (pins 1–2), it allows the module firmware (including BIOS) in the PFR-controlled PCH capsule file to be downgraded to a lower security version number (SVN). This jumper is used when there is a need for the module to power on using a BIOS revision with lower SVN.

Caution:

- Downgrading to an older version of BIOS may result in the loss of functionality and security features that are present in a higher SVN.
- When downgrading to an older version of the BIOS, modules may end up with a firmware stack combination that is not supported, and therefore could experience unpredictable behavior.

Note: Latest system update packages are included in the SUP posted to Intel's download center. For details, see Section 1.2.

To use the SVN downgrade jumper, perform the following steps:

1. Power down the server module.

2. Remove the server module from the chassis.
3. Remove the riser assembly #2 from the server module.
   See the *Intel® Server D50DNP Family Installation and Service Guide* for instructions.
4. Move the `BIOS SVN Downgrade` (`J14`) jumper from pins 1–2 (default) to pins 2–3 (SVN downgrade).
5. Reinstall the server module in the chassis.
6. Power on the server module and boot into the UEFI Shell.
7. Update the BIOS using the BIOS recovery update instructions provided with the system update package.
8. After the BIOS update is successfully completed, power down the server module.
9. Remove the server module from the chassis.
10. Move the `BIOS SVN Downgrade` (`J14`) jumper back to pins 1–2 (default).
11. Reinstall the riser assembly.
12. Reinstall the server module in the chassis.
13. Power on the server module. During POST, press **<F2>** to access the BIOS setup utility. Configure and save desired BIOS options.

15.5 BMC SVN Downgrade (BMC SVN Downgrade – J33)

When this jumper is moved from its default pin position (pins 1–2), it allows the module BMC firmware in the PFR-controlled BMC capsule file to be downgraded to a lower security version number (SVN). This jumper is used when there is a need for the module to power on using a BMC revision with lower SVN.

- **Caution:**
- Downgrading to a BMC version with lower SVN may result in the loss of functionality and security features that are present in a higher SVN but were not implemented in the lower SVN.
- When downgrading to an older version of BMC, modules may end up with a firmware stack combination that is not supported, and therefore could experience unpredictable behavior.

Note: Latest system update packages are included in the SUP posted to Intel's download center. For details, see Section 1.2.

To use the BMC SVN Downgrade jumper, perform the following steps:

1. Power down the server module.
2. Remove the server module from the chassis.
3. Remove the riser assembly #2 from the server module.
   See the *Intel® Server D50DNP Family Installation and Service Guide* for instructions.
4. Move the `BMC SVN downgrade jumper` (`J33`) from pins 1–2 (default) to pins 2–3 (Enabled).
5. Reinstall the server module in the chassis.
6. Power on the server module and boot into the UEFI Shell.
7. Update the BMC using the recovery BMC update instructions provided with the system update package.
8. After the BMC update is successfully completed, power down the server module.
9. Remove the server module from the chassis.
10. Using tweezers, move the `BMC SVN Downgrade jumper` (`J33`) back to pins 1–2 (default).
11. Reinstall the riser assembly.
12. Reinstall the server module in the chassis.
13. Power on the server module.

Appendix A. Getting Help

Available Intel support options with your Intel® Server System:

1. 24x7 support through Intel's support webpage at:
   https://www.intel.com/content/www/us/en/support/products/1201/server-products.html

   Information available at the support site includes:

   - Latest BIOS, firmware, drivers, and utilities
   - Product documentation, setup, and service guides
   - Full product specifications, technical advisories, and errata
   - Compatibility documentation for memory, hardware add-in cards, and operating systems
   - Server and chassis accessory parts list for ordering upgrades or spare parts
   - A searchable knowledge base to search for product information throughout the support site

Quick Links

Use the following links for support on Intel® Server Boards and Intel® Server Systems	**Download Center** http://www.intel.com/support/downloadserversw	**BIOS Support Page** http://www.intel.com/support/serverbios	**Troubleshooting Boot Issue** http://www.intel.com/support/tsboot
Use the following links for support on Intel® Data Center Block (DCB) Integrated Systems. **Note:** Intel® DCB comes pre-populated with processors, memory, storage, and peripherals based on how it was ordered through the Intel Configure to Order tool.	**Download Center** http://www.intel.com/support/downloaddcbsw	**Technical Support Documents** http://www.intel.com/support/dcb	**Warranty and Support Info** http://www.intel.com/support/dcbwarranty

2. If a solution cannot be found at Intel's support site, submit a service request via Intel's online service center at https://supporttickets.intel.com/servicecenter?lang=en-US. In addition, you can also view previous support requests. (Login required to access previous support requests.)
3. Contact an Intel support representative using one of the support phone numbers available at https://www.intel.com/content/www/us/en/support/contact-support.html (charges may apply).

Intel also offers to Intel® Partner Alliance program members around-the-clock 24x7 technical phone support on Intel server boards, server chassis, server RAID controller cards, and Intel® Server Management at https://www.intel.com/content/www/us/en/partner-alliance/overview.html.

Note: The 24x7 support number is available after logging in to the Intel® Partner Alliance website.

Warranty Information

To obtain warranty information, visit http://www.intel.com/p/en_US/support/warranty.

Appendix B. Mechanical Dimension Diagrams

This appendix provides server board, server modules, and server system dimensions. Location and dimensions of the chassis pull-out tab is also in this appendix.

B.1 Intel® Server Board D50DNP1SB Mechanical Dimension Diagrams

The following figure provides the Intel® Server Board D50DNP1SB dimensions.

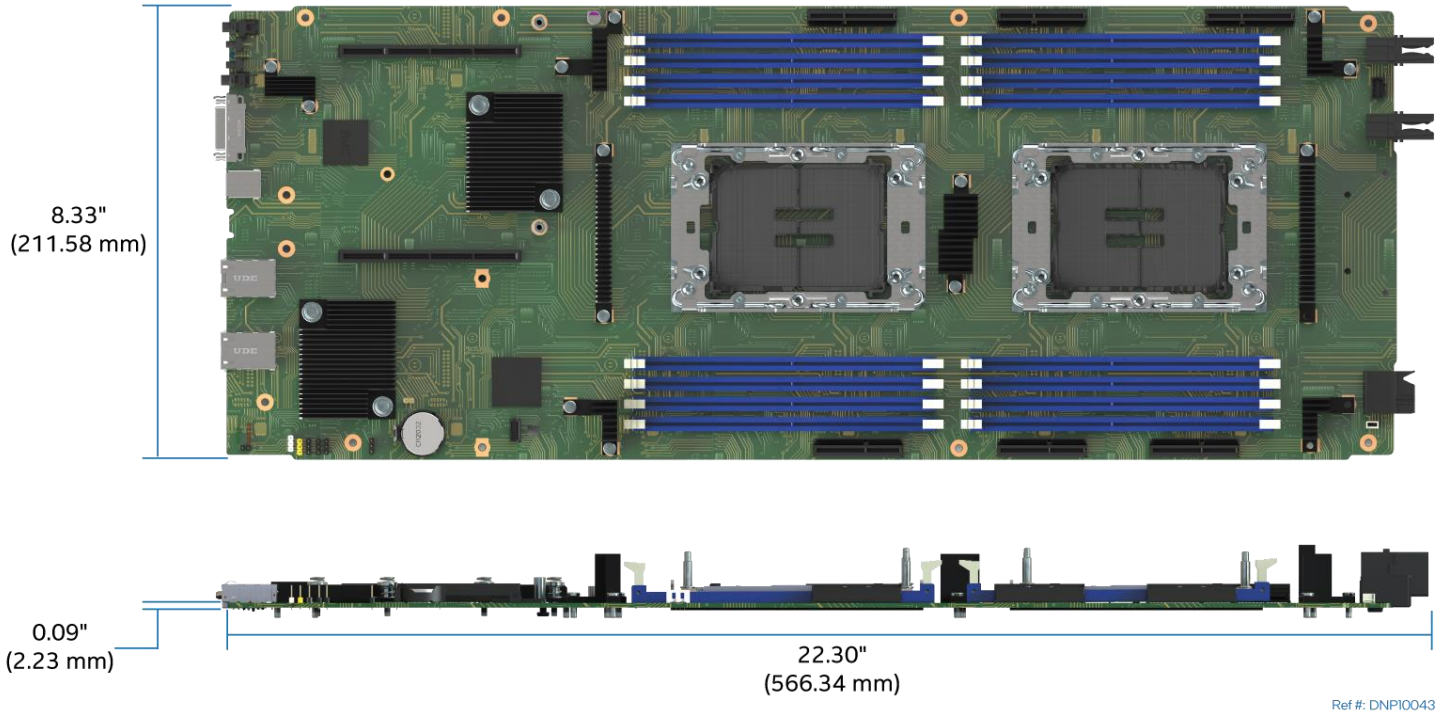


Figure 53. Intel® Server Board D50DNP1SB Dimensions

B.2 Intel® D50DNP Module Dimension Diagrams

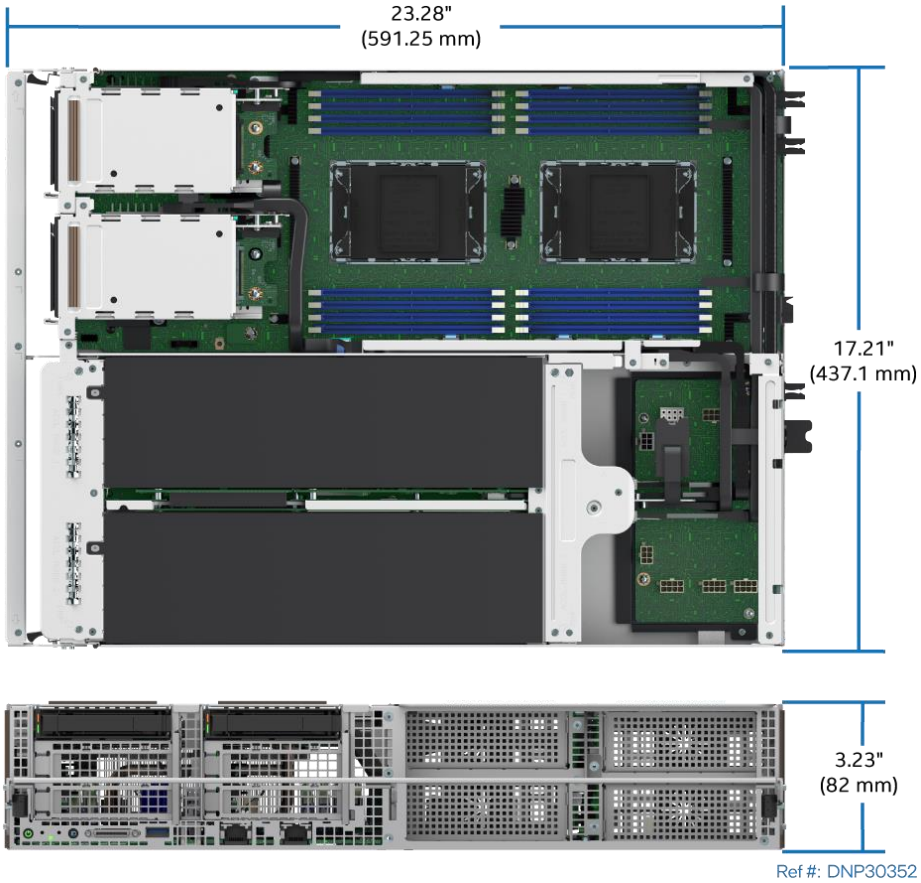


Figure 54. 2U PCIe* Accelerator Module Dimensions

B.3 System Chassis Dimension Diagrams

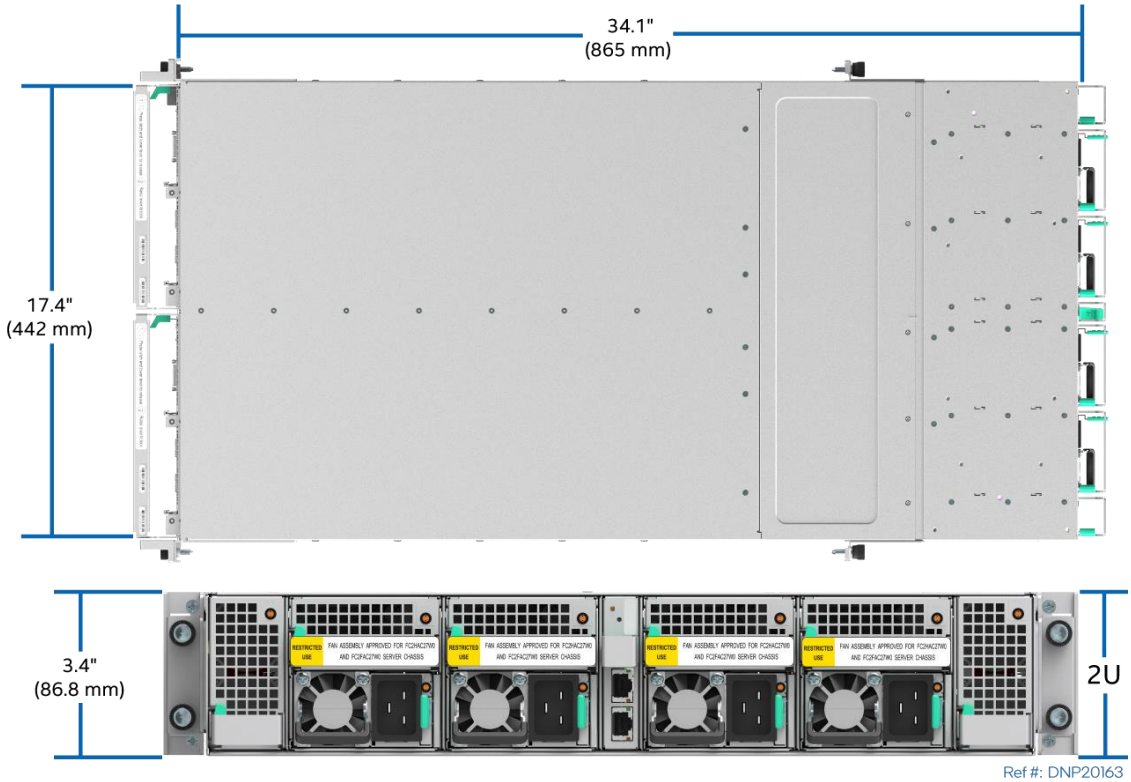


Figure 55. Air-Cooled System Chassis Dimensions

B.4 Pull-Out Tab

The chassis includes a pull-out tab that can be used for asset information. Figure 56 shows the location of the pull-out tab and Figure 57 shows its dimensions.

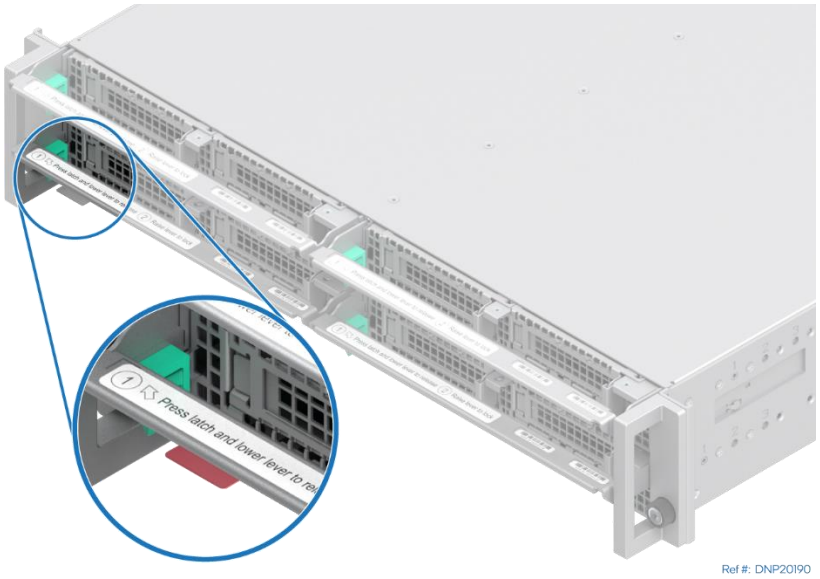


Figure 56. Pull-Out Tab Location

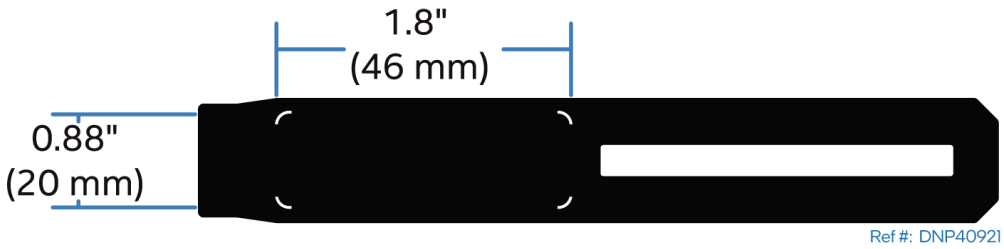


Figure 57. Pull-Out Tab Dimensions

Appendix C. POST Code Diagnostic LEDs

As an aid in troubleshooting a system hang that occurs during a system POST process, the server board includes a bank of eight diagnostic LEDs on the front edge of the board. These diagnostic LEDs are used during POST to represent halt error codes or POST progress codes.

During the system boot process, memory reference code (MRC) and system BIOS execute several memory initialization and platform configuration routines, each of which is assigned a hexadecimal POST progress code number. As each routine is started, the given POST progress code number is displayed on the diagnostic LEDs. If a system hangs during POST execution, the displayed POST progress code can be used to identify the last POST routine that was run before the error occurred, helping to isolate the possible cause of the hang condition even when video is not available.

These diagnostic LEDs are equivalent to the legacy "Port 80 POST Codes", and a Legacy I/O Port 80 output will be displayed as a Diagnostic LED code. Each POST progress code or halt error code is represented by eight LEDs, four green LEDs and four amber LEDs. The codes are divided into two nibbles, an upper nibble and a lower nibble. The upper nibble bits are represented by amber diagnostic LEDs and the lower nibble bits are represented by green diagnostic LEDs. If the bit is set, the corresponding LED is lit. If the bit is clear, the corresponding LED is off. For each set of nibble bits, LED with lowest number represents the least significant bit (LSB) and LED with highest number represents the most significant bit (MSB).

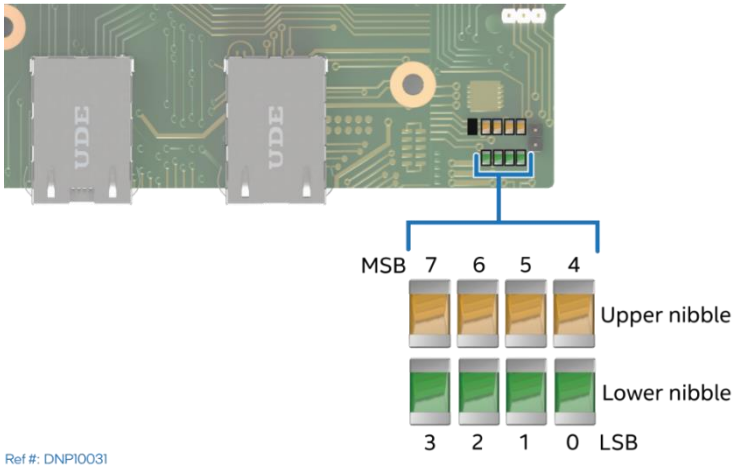


Figure 58. Intel® Light-Guided Diagnostics – POST Code LED Location

In the following example, the BIOS sends a hexadecimal value of AC to the diagnostic LEDs. The LEDs are decoded as shown in the following table.

Table 34. Diagnostic LED Code Example

LEDs		Upper Nibble Amber LEDs				Lower Nibble Green LEDs			
		MSB							LSB
		LED #7	LED #6	LED #5	LED #4	LED #3	LED #2	LED #1	LED #0
		8h	4h	2h	1h	8h	4h	2h	1h
Status		**ON**	OFF	**ON**	OFF	**ON**	**ON**	OFF	OFF
Read Value	Binary	1	0	1	0	1	1	0	0
	Hexadecimal	**A**h				**C**h			
Result		**AC**h							

Notes: Upper nibble bits = 1010b = **A**h; lower nibble bits = 1100b = **C**h; the two hexadecimal nibble values are combined to create a single **AC**h POST progress code.

C.1 Early Memory Initialization Progress Codes

Memory initialization at the beginning of POST includes multiple functions: discovery, channel training, validation that the DIMM population is acceptable and functional, initialization of the IMC and other hardware settings, and initialization of applicable RAS configurations.

The MRC progress codes are displayed to the diagnostic LEDs that show the execution point in the MRC operational path at each step.

Table 35. Memory Reference Code (MRC) Progress Codes

MRC Progress Code (Hex)	Upper Nibble				Lower Nibble				Description
	8h	4h	2h	1h	8h	4h	2h	1h	
70	0	1	1	1	0	0	0	0	HBM Training
71	0	1	1	1	0	0	0	1	HBM internal use.
72	0	1	1	1	0	0	1	0	HBM internal use.
73	0	1	1	1	0	0	1	1	NVRAM sync.
7E	0	1	1	1	1	1	1	0	MRC internal sync.
B0	1	0	1	1	0	0	0	0	Detect DIMM population
B1	1	0	1	1	0	0	0	1	Initialize clock
B2	1	0	1	1	0	0	1	0	Gather remaining SPD data
B3	1	0	1	1	0	0	1	1	Gets memory ready to be written and read.
B4	1	0	1	1	0	1	0	0	Evaluate RAS modes and save rank information.
B5	1	0	1	1	0	1	0	1	MRC internal dispatch.
B6	1	0	1	1	0	1	1	0	DDRIO initialize.
B7	1	0	1	1	0	1	1	1	Train DDR5 channels
0	0	0	0	0	0	0	0	0	Train DDR5 channels: Receive enable training
3	0	0	0	0	0	0	1	1	Train DDR5 channels: Read DQ/DQS training
4	0	0	0	0	0	1	0	0	Train DDR5 channels: Write DQ/DQS training
11	0	0	0	1	0	0	0	1	Train DDR5 channels: End of channel training.
77	0	1	1	1	0	1	1	1	Train DDR5 channels: Write leveling training.
B8	1	0	1	1	1	0	0	0	Initialize CLTT/OLTT
B9	1	0	1	1	1	0	0	1	Hardware memory test and initialization
BA	1	0	1	1	1	0	1	0	Execute software memory initialization
BB	1	0	1	1	1	0	1	1	Program memory map and interleaving
BC	1	0	1	1	1	1	0	0	Program RAS configuration
BE	1	0	1	1	1	1	1	0	Execute BSSA RMT
BF	1	0	1	1	1	1	1	1	MRC is done

If a major memory initialization error occurs, preventing the system from booting with data integrity, the MRC displays a fatal error code on the diagnostic LEDs, and a system halt command is executed. Fatal MRC error halts do not change the state of the system status LED and they do not get logged as SEL events. Table 36 lists all MRC fatal errors that are displayed to the diagnostic LEDs.

Note: Fatal MRC errors display codes that may be the same as BIOS POST progress codes displayed later in the POST process.

Table 36. MRC Fatal Error Codes

MRC fatal error code (Hex)	Upper Nibble				Lower Nibble				MRC fatal error code explanation (with MRC internal minor code)
	8h	4h	2h	1h	8h	4h	2h	1h	
E8	1	1	1	0	1	0	0	0	No usable memory error. 01h = No memory was detected from SPD read, or invalid configuration that causes no operable memory. 02h = Memory DIMMs on all channels of all sockets are disabled due to hardware memory test error. 03h = No memory installed. All channels are disabled.
E9	1	1	1	0	1	0	0	1	Memory is locked by Intel® TXT and is inaccessible.
EA	1	1	1	0	1	0	1	0	DDR5 channel training error. 01h = Error on read DQ/DQS (Data/Data Strobe) initialization. 02h = Error on receive enable. 03h = Error on write leveling. 04h = Error on write DQ/DQS (Data/Data Strobe.
EB	1	1	1	0	1	0	1	1	Memory test failure. 01h = Software memory test failure. 02h = Hardware memory test failed.
ED	1	1	1	0	1	1	0	1	DIMM configuration population error. 01h = Different DIMM types (RDIMM, 3DS-RDIMM) are detected installed in the system. 02h = Violation of DIMM population rules. 03h = The third DIMM slot cannot be populated when QR DIMMs are installed. 04h = UDIMMs are not supported. 05h = Unsupported DIMM voltage.
EF	1	1	1	0	1	1	1	1	Indicates a CLTT table structure error.

C.2 BIOS POST Progress Codes

The following table provides a list of all POST progress codes.

Table 37. POST Progress Codes

Post progress code (Hex)	Upper Nibble				Lower Nibble				Description
	8h	4h	2h	1h	8h	4h	2h	1h	
Security (SEC) Phase									
01	0	0	0	0	0	0	0	1	First POST code after CPU reset
02	0	0	0	0	0	0	1	0	Microcode load begins
03	0	0	0	0	0	0	1	1	CRAM initialization begins
04	0	0	0	0	0	1	0	0	PEI cache when disabled
05	0	0	0	0	0	1	0	1	SEC core at power-on start
06	0	0	0	0	0	1	1	0	Early CPU initialization during SEC phase
Intel® UPI RC (fully leverage without platform change)									
A1	1	0	1	0	0	0	0	1	Collect information such as SBSP, boot mode, reset type, etc.
A3	1	0	1	0	0	0	1	1	Setup minimum path between SBSP and other sockets
A6	1	0	1	0	0	1	1	0	Sync up with PBSPs
A7	1	0	1	0	0	1	1	1	Topology discovery and route calculation
A8	1	0	1	0	1	0	0	0	Program final route
A9	1	0	1	0	1	0	0	1	Program final IO SAD setting

Post progress code (Hex)	Upper Nibble				Lower Nibble				Description
	8h	4h	2h	1h	8h	4h	2h	1h	
AA	1	0	1	0	1	0	1	0	Protocol layer and other uncore settings
AB	1	0	1	0	1	0	1	1	Transition links to full speed operation
AE	1	0	1	0	1	1	1	0	Coherency settings
AF	1	0	1	0	1	1	1	1	Intel® UPI initialization is done
Pre-EFI Initialization (PEI) Phase									
10	0	0	0	1	0	0	0	0	PEI core
11	0	0	0	1	0	0	0	1	CPU PEIM
15	0	0	0	1	0	1	0	1	Platform type initialization
19	0	0	0	1	1	0	0	1	Platform PEIM initialization
Integrated I/O (IIO) Progress Codes									
E0	1	1	1	0	0	0	0	0	IIO early initialization entry
E1	1	1	1	0	0	0	0	1	IIO pre-link training
E2	1	1	1	0	0		1	0	IIO EQ programming
E3	1	1	1	0	0	0	1	1	IIO link training
E4	1	1	1	0	0	1	0	0	Internal use
E5	1	1	1	0	0	1	0	1	IIO early initialization exit
E6	1	1	1	0	0	1	1	0	IIO late initialization entry
E7	1	1	1	0	0	1	1	1	IIO PCIe* ports initialization
E8	1	1	1	0	1	0	0	0	IIO IOAPIC initialization
E9	1	1	1	0	1	0	0	1	IIO VTD initialization
EA	1	1	1	0	1	0	1	0	IIO IOAT initialization
EB	1	1	1	0	1	0	1	1	IIO DXF initialization
EC	1	1	1	0	1	1	0	0	IIO NTB initialization
ED	1	1	1	0	1	1	0	1	IIO security initialization
EE	1	1	1	0	1	1	1	0	IIO late initialization exit
EF	1	1	1	0	1	1	1	1	IIO ready to boot
MRC Progress Codes – At this point, the MRC progress code sequence is executed									
31	0	0	1	1	0	0	0	1	Memory installed
32	0	0	1	1	0	0	1	0	CPU PEIM (CPU initialization)
33	0	0	1	1	0	0	1	1	CPU PEIM (cache initialization)
34	0	0	1	1	0	1	0	0	CPU BSP select
35	0	0	1	1	0	1	0	1	CPU AP initialization
36	0	0	1	1	0	1	1	0	CPU SMM initialization
4F	0	1	0	0	1	1	1	1	DXE IPL started
Memory Feature Progress Codes									
C1	1	1	0	0	0	0	0	1	Memory POR check
C2	1	1	0	0	0	0	1	0	Internal use
C3	1	1	0	0	0	0	1	1	Internal use
C4	1	1	0	0	0	1	0	0	Internal use
C5	1	1	0	0	0	1	0	1	Memory early initialization
C6	1	1	0	0	0	1	1	0	Display DIMM information in debug mode
C7	1	1	0	0	0	1	1	1	JEDEC NVDIMM training
C9	1	1	0	0	1	0	0	1	Setup SVL and scrambling
CA	1	1	0	0	1	0	1	0	Internal use
CB	1	1	0	0	1	0	1	1	Check RAS support

Post progress code (Hex)	Upper Nibble				Lower Nibble				Description
	8h	4h	2h	1h	8h	4h	2h	1h	
CC	1	1	0	0	1	1	0	0	PMem ADR initialization
CD	1	1	0	0	1	1	0	1	Internal use
CE	1	1	0	0	1	1	1	0	Memory late initialization
CF	1	1	0	0	1	1	1	1	Determine MRC boot mode
D0	1	1	0	1	0	0	0	0	MKTME early initialization
D1	1	1	0	1	0	0	0	1	SGX early initialization
D2	1	1	0	1	0	0	1	0	Memory margin test
D3	1	1	0	1	0	0	1	1	Internal use
D5	1	1	0	1	0	1	0	1	Internal use
D6	1	1	0	1	0	1	1	0	Offset training result
Driver Execution Environment (DXE) Phase									
60	0	1	1	0	0	0	0	0	DXE core started
62	0	1	1	0	0	0	1	0	DXE setup initialization
68	0	1	1	0	1	0	0	0	DXE PCI host bridge initialization
69	0	1	1	0	1	0	0	1	DXE NB initialization
6A	0	1	1	0	1	0	1	0	DXE NB SMM initialization
70	0	1	1	1	0	0	0	0	DXE SB initialization
71	0	1	1	1	0	0	0	1	DXE SB SMM initialization
72	0	1	1	1	0	0	1	0	DXE SB devices initialization
78	0	1	1	1	1	0	0	0	DXE ACPI initialization
79	0	1	1	1	1	0	0	1	DXE CSM initialization
7D	0	1	1	1	1	1	0	1	DXE removable media detect
7E	0	1	1	1	1	1	1	0	DXE removable media detected
90	1	0	0	1	0	0	0	0	DXE BDS started
91	1	0	0	1	0	0	0	1	DXE BDS connect drivers
92	1	0	0	1	0	0	1	0	DXE PCI bus start
93	1	0	0	1	0	0	1	1	DXE PCI bus HPC initialization
94	1	0	0	1	0	1	0	0	DXE PCI bus enumeration
95	1	0	0	1	0	1	0	1	DXE PCI bus resource requested
96	1	0	0	1	0	1	1	0	DXE PCI bus assign resource
97	1	0	0	1	0	1	1	1	DXE CON_OUT connect
98	1	0	0	1	1	0	0	0	DXE CON_IN connect
99	1	0	0	1	1	0	0	1	DXE SIO initialization
9A	1	0	0	1	1	0	1	0	DXE USB start
9B	1	0	0	1	1	0	1	1	DXE USB reset
9C	1	0	0	1	1	1	0	0	DXE USB detected
9D	1	0	0	1	1	1	0	1	DXE USB enabled
A1	1	0	1	0	0	0	0	1	DXE IDE start
A2	1	0	1	0	0	0	1	0	DXE IDE reset
A3	1	0	1	0	0	0	1	1	DXE IDE detected
A4	1	0	1	0	0	1	0	0	DXE IDE enabled
A5	1	0	1	0	0	1	0	1	DXE SCSI start
A6	1	0	1	0	0	1	1	0	DXE SCSI reset
A7	1	0	1	0	0	1	1	1	DXE SCSI detected
A8	1	0	1	0	1	0	0	0	DXE SCSI enabled

Post progress code (Hex)	Upper Nibble				Lower Nibble				Description
	8h	4h	2h	1h	8h	4h	2h	1h	
AB	1	0	1	0	1	0	1	1	DXE SETUP start
AC	1	0	1	0	1	1	0	0	DXE SETUP input wait
AD	1	0	1	0	1	1	0	1	DXE ready to boot
AE	1	0	1	0	1	1	1	0	DXE legacy boot
AF	1	0	1	0	1	1	1	1	DXE exit boot services
B0	1	0	1	1	0	0	0	0	RT set virtual address map start
B1	1	0	1	1	0	0	0	1	RT set virtual address map end
B2	1	0	1	1	0	0	1	0	DXE legacy option ROM initialization
B3	1	0	1	1	0	0	1	1	DXE reset system
B4	1	0	1	1	0	1	0	0	DXE USB hot plug
B5	1	0	1	1	0	1	0	1	DXE PCI bus hot plug
B8	1	0	1	1	1	0	0	0	PWRBTN shutdown
B9	1	0	1	1	1	0	0	1	SLEEP shutdown
C0	1	1	0	0	0	0	0	0	End of DXE
C7	1	1	0	0	0	1	1	1	DXE ACPI enable
0	0	0	0	0	0	0	0	0	Clear POST code
BDS Phase									
51	0	1	0	1	0	0	0	1	BDS select video.
52	0	1	0	1	0	0	1	0	BDS after trust console.
53	0	1	0	1	0	0	1	1	BDS end of DXE.
54	0	1	0	1	0	1	0	0	BDS ready to lock.
55	0	1	0	1	0	1	0	1	BDS connect device.
56	0	1	0	1	0	1	1	0	BDS before enter setup.
57	0	1	0	1	0	1	1	1	BDS load boot options.
58	0	1	0	1	1	0	0	0	BDS exit boot services.
S3 Resume									
E0	1	1	1	0	0	0	0	0	S3 resume PEIM (S3 started)
E1	1	1	1	0	0	0	0	1	S3 resume PEIM (S3 boot script)
E2	1	1	1	0	0	0	1	0	S3 resume PEIM (S3 video repost)
E3	1	1	1	0	0	0	1	1	S3 resume PEIM (S3 operating system wake)

Appendix D. POST Errors Codes

Most error conditions encountered during POST are reported using POST error codes. These codes represent specific failures, warnings, or information. POST error codes may be displayed in the Error Manager display screen in the BIOS Setup utility and are always logged to the System Event Log (SEL). Logged events are available to system management applications, including remote and Out of Band (OOB) management.

There are exception cases in early initialization where system resources are not adequately initialized for handling POST Error Code reporting. These cases are primarily fatal error conditions resulting from initialization of processors and memory, and they are handled by a diagnostic LED display with a system halt.

Table 38 lists the supported POST error codes. Each error code is assigned an error type that determines the action the BIOS takes when the error is encountered. Error types include minor, major, and fatal. The BIOS action for each is defined as follows:

- **Minor:** An error message may be displayed on the POST screen or in the BIOS setup utility Error Manager and the POST error code is logged to the SEL. The system continues booting in a degraded state. The user may want to replace the erroneous unit. The POST Error Pause option setting in the BIOS setup utility does not have any effect on this error.
- **Major:** An error message is posted to the Error Manager screen and an error is logged to the SEL. If the BIOS setup utility “Post Error Pause” option is enabled, operator intervention is required to continue booting the system. If the BIOS setup utility “POST Error Pause” option is disabled, the system continues to boot.

  Note: For `0048` (password check failed), the system halts and then, after the next reset/reboot, displays the error code on the error manager screen.

  Fatal: If the system cannot boot, POST halts the system with a halt error code on the diagnostic LEDs. The system cannot boot unless the error is resolved. The faulty component must be replaced.

Note: The POST error codes in the following table are common to all current generation Intel server platforms. Features present on a given server board/system determine which of the listed error codes are supported.

Table 38. POST Error Codes, Messages and Corrective Actions

POST Error Code	Error Message	Corrective Action	Type
0012	System RTC date/time not set	Set date and time	Major
0048	Password check failed	Put right password.	Major
0140	PCI component encountered a PERR error		Major
0141	PCI resource conflict		Major
0146	PCI out of resources error	Enable Memory Mapped I/O above 4 GB item at SETUP to use 64-bit MMIO.	Major
0147	Some option ROMs are not loaded because the verification fails when the Secure Boot option is enabled.	Option ROM code must be signed with a certificate recognized by BIOS	Minor
0191	Processor core/thread count mismatch detected	Use identical CPU type.	Fatal
0192	Processor cache size mismatch detected	Use identical CPU type.	Fatal
0194	Processor family mismatch detected	Use identical CPU type.	Fatal
0195	Processor Intel® UPI link frequencies unable to synchronize		Fatal
0196	Processor model mismatch detected	Use identical CPU type.	Fatal
0197	Processor frequencies unable to synchronize	Use identical CPU type.	Fatal
5220	BIOS Settings reset to default settings		Major
5221	Passwords cleared by jumper		Major
5224	Password clear jumper is Set	Recommend reminding user to install BIOS password as BIOS admin password is the main keys for several BIOS security features.	Major
8130	CPU 0 disabled		Major
8131	CPU 1 disabled		Major
8160	CPU 0 unable to apply microcode update		Major
8161	CPU 1 unable to apply microcode update		Major
8170	CPU 0 failed Self-Test (BIST)		Major
8171	CPU 1 failed Self-Test (BIST)		Major
8180	CPU 0 microcode update not found		Minor
8181	CPU 1 microcode update not found		Minor
8190	Watchdog timer failed on last boot.		Major
8198	OS boot watchdog timer failure.		Major
8300	Baseboard Management Controller failed self-test.		Major
8305	Hot Swap Controller failure		Major
83A0	Management Engine (ME) failed self-test.		Major
83A1	Management Engine (ME) Failed to respond.		Major
84F2	Baseboard management controller failed to respond		Major
84F3	Baseboard Management Controller in Update Mode.		Major
84F4	Baseboard Management Controller Sensor Data Record empty.	Update right SDR.	Major
84FF	System Event Log full	Clear SEL through EWS or SELVIEW utility.	Minor
85FC	Memory component could not be configured in the selected RAS mode		Major
8501	Memory Population Error	Plug DIMM at right population.	Major
8502	PMem invalid DIMM population found on the system.	Follow valid POR for PMem DIMM.	Major
8520	Memory failed test/initialization CPU0_DIMM_A1	Remove the disabled DIMM.	Major

POST Error Code	Error Message	Corrective Action	Type
8521	Memory failed test/initialization CPU0_DIMM_A2	Remove the disabled DIMM.	Major
8522	Memory failed test/initialization CPU0_DIMM_A3	Remove the disabled DIMM.	Major
8523	Memory failed test/initialization CPU0_DIMM_B1	Remove the disabled DIMM.	Major
8524	Memory failed test/initialization CPU0_DIMM_B2	Remove the disabled DIMM.	Major
8525	Memory failed test/initialization CPU0_DIMM_B3	Remove the disabled DIMM.	Major
8526	Memory failed test/initialization CPU0_DIMM_C1	Remove the disabled DIMM.	Major
8527	Memory failed test/initialization CPU0_DIMM_C2	Remove the disabled DIMM.	Major
8528	Memory failed test/initialization CPU0_DIMM_C3	Remove the disabled DIMM.	Major
8529	Memory failed test/initialization CPU0_DIMM_D1	Remove the disabled DIMM.	Major
852A	Memory failed test/initialization CPU0_DIMM_D2	Remove the disabled DIMM.	Major
852B	Memory failed test/initialization CPU0_DIMM_D3	Remove the disabled DIMM.	Major
852C	Memory failed test/initialization CPU0_DIMM_E1	Remove the disabled DIMM.	Major
852D	Memory failed test/initialization CPU0_DIMM_E2	Remove the disabled DIMM.	Major
852E	Memory failed test/initialization CPU0_DIMM_E3	Remove the disabled DIMM.	Major
852F	Memory failed test/initialization CPU0_DIMM_F1	Remove the disabled DIMM.	Major
8530	Memory failed test/initialization CPU0_DIMM_F2	Remove the disabled DIMM.	Major
8531	Memory failed test/initialization CPU0_DIMM_F3	Remove the disabled DIMM.	Major
8532	Memory failed test/initialization CPU0_DIMM_G1	Remove the disabled DIMM.	Major
8533	Memory failed test/initialization CPU0_DIMM_G2	Remove the disabled DIMM.	Major
8534	Memory failed test/initialization CPU0_DIMM_G3	Remove the disabled DIMM.	Major
8535	Memory failed test/initialization CPU0_DIMM_H1	Remove the disabled DIMM.	Major
8536	Memory failed test/initialization CPU0_DIMM_H2	Remove the disabled DIMM.	Major
8537	Memory failed test/initialization CPU0_DIMM_H3	Remove the disabled DIMM.	Major
8538	Memory failed test/initialization CPU1_DIMM_A1	Remove the disabled DIMM.	Major
8539	Memory failed test/initialization CPU1_DIMM_A2	Remove the disabled DIMM.	Major
853A	Memory failed test/initialization CPU1_DIMM_A3	Remove the disabled DIMM.	Major
853B	Memory failed test/initialization CPU1_DIMM_B1	Remove the disabled DIMM.	Major
853C	Memory failed test/initialization CPU1_DIMM_B2	Remove the disabled DIMM.	Major
853D	Memory failed test/initialization CPU1_DIMM_B3	Remove the disabled DIMM.	Major
853E	Memory failed test/initialization CPU1_DIMM_C1	Remove the disabled DIMM.	Major
853F (Go to 85C0)	Memory failed test/initialization CPU1_DIMM_C2	Remove the disabled DIMM.	Major
8540	Memory disabled.CPU0_DIMM_A1	Remove the disabled DIMM.	Major
8541	Memory disabled.CPU0_DIMM_A2	Remove the disabled DIMM.	Major
8542	Memory disabled.CPU0_DIMM_A3	Remove the disabled DIMM.	Major
8543	Memory disabled.CPU0_DIMM_B1	Remove the disabled DIMM.	Major
8544	Memory disabled.CPU0_DIMM_B2	Remove the disabled DIMM.	Major
8545	Memory disabled.CPU0_DIMM_B3	Remove the disabled DIMM.	Major
8546	Memory disabled.CPU0_DIMM_C1	Remove the disabled DIMM.	Major
8547	Memory disabled.CPU0_DIMM_C2	Remove the disabled DIMM.	Major
8548	Memory disabled.CPU0_DIMM_C3	Remove the disabled DIMM.	Major
8549	Memory disabled.CPU0_DIMM_D1	Remove the disabled DIMM.	Major
854A	Memory disabled.CPU0_DIMM_D2	Remove the disabled DIMM.	Major
854B	Memory disabled.CPU0_DIMM_D3	Remove the disabled DIMM.	Major
854C	Memory disabled.CPU0_DIMM_E1	Remove the disabled DIMM.	Major

POST Error Code	Error Message	Corrective Action	Type
854D	Memory disabled.CPU0_DIMM_E2	Remove the disabled DIMM.	Major
854E	Memory disabled.CPU0_DIMM_E3	Remove the disabled DIMM.	Major
854F	Memory disabled.CPU0_DIMM_F1	Remove the disabled DIMM.	Major
8550	Memory disabled.CPU0_DIMM_F2	Remove the disabled DIMM.	Major
8551	Memory disabled.CPU0_DIMM_F3	Remove the disabled DIMM.	Major
8552	Memory disabled.CPU0_DIMM_G1	Remove the disabled DIMM.	Major
8553	Memory disabled.CPU0_DIMM_G2	Remove the disabled DIMM.	Major
8554	Memory disabled.CPU0_DIMM_G3	Remove the disabled DIMM.	Major
8555	Memory disabled.CPU0_DIMM_H1	Remove the disabled DIMM.	Major
8556	Memory disabled.CPU0_DIMM_H2	Remove the disabled DIMM.	Major
8557	Memory disabled.CPU0_DIMM_H3	Remove the disabled DIMM.	Major
8558	Memory disabled.CPU1_DIMM_A1	Remove the disabled DIMM.	Major
8559	Memory disabled.CPU1_DIMM_A2	Remove the disabled DIMM.	Major
855A	Memory disabled.CPU1_DIMM_A3	Remove the disabled DIMM.	Major
855B	Memory disabled.CPU1_DIMM_B1	Remove the disabled DIMM.	Major
855C	Memory disabled.CPU1_DIMM_B2	Remove the disabled DIMM.	Major
855D	Memory disabled.CPU1_DIMM_B3	Remove the disabled DIMM.	Major
855E	Memory disabled.CPU1_DIMM_C1	Remove the disabled DIMM.	Major
855F (Go to 85D0)	Memory disabled.CPU1_DIMM_C2	Remove the disabled DIMM.	Major
8560	Memory encountered a Serial Presence Detection(SPD) failure.CPU0_DIMM_A1		Major
8561	Memory encountered a Serial Presence Detection(SPD) failure.CPU0_DIMM_A2		Major
8562	Memory encountered a Serial Presence Detection(SPD) failure.CPU0_DIMM_A3		Major
8563	Memory encountered a Serial Presence Detection(SPD) failure.CPU0_DIMM_B1		Major
8564	Memory encountered a Serial Presence Detection(SPD) failure.CPU0_DIMM_B2		Major
8565	Memory encountered a Serial Presence Detection(SPD) failure.CPU0_DIMM_B3		Major
8566	Memory encountered a Serial Presence Detection(SPD) failure.CPU0_DIMM_C1		Major
8567	Memory encountered a Serial Presence Detection (SPD) failure.CPU0_DIMM_C2		Major
8568	Memory encountered a Serial Presence Detection (SPD) failure.CPU0_DIMM_C3		Major
8569	Memory encountered a Serial Presence Detection(SPD) failure.CPU0_DIMM_D1		Major
856A	Memory encountered a Serial Presence Detection(SPD) failure.CPU0_DIMM_D2		Major
856B	Memory encountered a Serial Presence Detection(SPD) failure.CPU0_DIMM_D3		Major
856C	Memory encountered a Serial Presence Detection(SPD) failure.CPU0_DIMM_E1		Major
856D	Memory encountered a Serial Presence Detection(SPD) failure.CPU0_DIMM_E2		Major

POST Error Code	Error Message	Corrective Action	Type
856E	Memory encountered a Serial Presence Detection(SPD) failure.CPU0_DIMM_E3		Major
856F	Memory encountered a Serial Presence Detection(SPD) failure.CPU0_DIMM_F1		Major
8570	Memory encountered a Serial Presence Detection(SPD) failure.CPU0_DIMM_F2		Major
8571	Memory encountered a Serial Presence Detection(SPD) failure.CPU0_DIMM_F3		Major
8572	Memory encountered a Serial Presence Detection(SPD) failure.CPU0_DIMM_G1		Major
8573	Memory encountered a Serial Presence Detection(SPD) failure.CPU0_DIMM_G2		Major
8574	Memory encountered a Serial Presence Detection(SPD) failure.CPU0_DIMM_G3		Major
8575	Memory encountered a Serial Presence Detection(SPD) failure.CPU0_DIMM_H1		Major
8576	Memory encountered a Serial Presence Detection(SPD) failure.CPU0_DIMM_H2		Major
8577	Memory encountered a Serial Presence Detection(SPD) failure.CPU0_DIMM_H3		Major
8578	Memory encountered a Serial Presence Detection(SPD) failure.CPU1_DIMM_A1		Major
8579	Memory encountered a Serial Presence Detection(SPD) failure.CPU1_DIMM_A2		Major
857A	Memory encountered a Serial Presence Detection(SPD) failure.CPU1_DIMM_A3		Major
857B	Memory encountered a Serial Presence Detection(SPD) failure.CPU1_DIMM_B1		Major
857C	Memory encountered a Serial Presence Detection(SPD) failure.CPU1_DIMM_B2		Major
857D	Memory encountered a Serial Presence Detection(SPD) failure.CPU1_DIMM_B3		Major
857E	Memory encountered a Serial Presence Detection(SPD) failure.CPU1_DIMM_C1		Major
857F (Go to 85E0)	Memory encountered a Serial Presence Detection(SPD) failure.CPU1_DIMM_C2		Major
85C0	Memory failed test/initialization CPU1_DIMM_C3	Remove the disabled DIMM.	Major
85C1	Memory failed test/initialization CPU1_DIMM_D1	Remove the disabled DIMM.	Major
85C2	Memory failed test/initialization CPU1_DIMM_D2	Remove the disabled DIMM.	Major
85C3	Memory failed test/initialization CPU1_DIMM_D3	Remove the disabled DIMM.	Major
85C4	Memory failed test/initialization CPU1_DIMM_E1	Remove the disabled DIMM.	Major
85C5	Memory failed test/initialization CPU1_DIMM_E2	Remove the disabled DIMM.	Major
85C6	Memory failed test/initialization CPU1_DIMM_E3	Remove the disabled DIMM.	Major
85C7	Memory failed test/initialization CPU1_DIMM_F1	Remove the disabled DIMM.	Major
85C8	Memory failed test/initialization CPU1_DIMM_F2	Remove the disabled DIMM.	Major
85C9	Memory failed test/initialization CPU1_DIMM_F3	Remove the disabled DIMM.	Major
85CA	Memory failed test/initialization CPU1_DIMM_G1	Remove the disabled DIMM.	Major
85CB	Memory failed test/initialization CPU1_DIMM_G2	Remove the disabled DIMM.	Major
85CC	Memory failed test/initialization CPU1_DIMM_G3	Remove the disabled DIMM.	Major

POST Error Code	Error Message	Corrective Action	Type
85CD	Memory failed test/initialization CPU1_DIMM_H1	Remove the disabled DIMM.	Major
85CE	Memory failed test/initialization CPU1_DIMM_H2	Remove the disabled DIMM.	Major
85CF	Memory failed test/initialization CPU1_DIMM_H3	Remove the disabled DIMM.	Major
85D0	Memory disabled.CPU1_DIMM_C3	Remove the disabled DIMM.	Major
85D1	Memory disabled.CPU1_DIMM_D1	Remove the disabled DIMM.	Major
85D2	Memory disabled.CPU1_DIMM_D2	Remove the disabled DIMM.	Major
85D3	Memory disabled.CPU1_DIMM_D3	Remove the disabled DIMM.	Major
85D4	Memory disabled.CPU1_DIMM_E1	Remove the disabled DIMM.	Major
85D5	Memory disabled.CPU1_DIMM_E2	Remove the disabled DIMM.	Major
85D6	Memory disabled.CPU1_DIMM_E3	Remove the disabled DIMM.	Major
85D7	Memory disabled.CPU1_DIMM_F1	Remove the disabled DIMM.	Major
85D8	Memory disabled.CPU1_DIMM_F2	Remove the disabled DIMM.	Major
85D9	Memory disabled.CPU1_DIMM_F3	Remove the disabled DIMM.	Major
85DA	Memory disabled.CPU1_DIMM_G1	Remove the disabled DIMM.	Major
85DB	Memory disabled.CPU1_DIMM_G2	Remove the disabled DIMM.	Major
85DC	Memory disabled.CPU1_DIMM_G3	Remove the disabled DIMM.	Major
85DD	Memory disabled.CPU1_DIMM_H1	Remove the disabled DIMM.	Major
85DE	Memory disabled.CPU1_DIMM_H2	Remove the disabled DIMM.	Major
85DF	Memory disabled.CPU1_DIMM_H3	Remove the disabled DIMM.	Major
85E0	Memory encountered a Serial Presence Detection(SPD) failure.CPU1_DIMM_C3		Major
85E1	Memory encountered a Serial Presence Detection (SPD) failure. CPU1_DIMM_D1		Major
85E2	Memory encountered a Serial Presence Detection (SPD) failure.CPU1_DIMM_D2		Major
85E3	Memory encountered a Serial Presence Detection(SPD) failure.CPU1_DIMM_D3		Major
85E4	Memory encountered a Serial Presence Detection(SPD) failure.CPU1_DIMM_E1		Major
85E5	Memory encountered a Serial Presence Detection(SPD) failure.CPU1_DIMM_E2		Major
85E6	Memory encountered a Serial Presence Detection(SPD) failure.CPU1_DIMM_E3		Major
85E7	Memory encountered a Serial Presence Detection (SPD) failure.CPU1_DIMM_F1		Major
85E8	Memory encountered a Serial Presence Detection(SPD) failure.CPU1_DIMM_F2		Major
85E9	Memory encountered a Serial Presence Detection(SPD) failure.CPU1_DIMM_F3		Major
85EA	Memory encountered a Serial Presence Detection(SPD) failure.CPU1_DIMM_G1		Major
85EB	Memory encountered a Serial Presence Detection (SPD) failure. CPU1_DIMM_G2		Major
85EC	Memory encountered a Serial Presence Detection(SPD) failure.CPU1_DIMM_G3		Major
85ED	Memory encountered a Serial Presence Detection(SPD) failure.CPU1_DIMM_H1		Major
85EE	Memory encountered a Serial Presence Detection(SPD) failure.CPU1_DIMM_H2		Major

POST Error Code	Error Message	Corrective Action	Type
85EF	Memory encountered a Serial Presence Detection(SPD) failure.CPU1_DIMM_H3		Major
8604	POST Reclaim of non-critical NVRAM variables		Minor
8605	BIOS Settings are corrupted		Major
8606	NVRAM variable space was corrupted and has been reinitialized		Major
8607	Recovery boot has been initiated. **Note:** The primary BIOS image may be corrupted, or the system may hang during POST. A BIOS update is required.		Fatal
A100	BIOS ACM Error		Major
A421	PCI component encountered a SERR error		Fatal
A5A0	PCI Express component encountered a PERR error		Minor
A5A1	PCI Express component encountered an SERR error		Fatal
A6A0	DXE Boot Services driver: Not enough memory available to shadow a Legacy Option ROM.	Disable option ROM at setup to save runtime memory.	Minor

D.1 POST Error LED Codes

Before system video initialization, the BIOS and BMC use POST error LED codes to inform users on error conditions. These POST error LED codes may be displayed alongside other codes on the diagnostic LEDs. This LED is the replacement of the beeper that was used to emit auditable error codes on the previous generation platforms. See the following figure for POST error LED location. The BIOS POST error LED code descriptions are listed in Table 53 and the BMC POST error LED code descriptions are listed in Table 54.

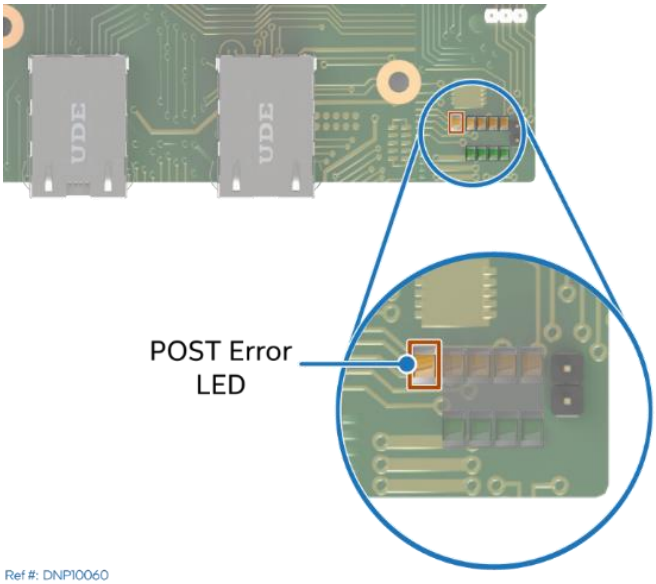


Figure 59. POST Error LED Location

Table 39. BIOS POST Error LED Codes

POST Error LED Sequence	Error Message	POST Progress Code	Description
3 short	Memory error	Multiple	System halted because a fatal error related to the memory was detected.
3 long and 1 short	CPU mismatch error	E5	System halted because a fatal error related to the CPU family/model/cache/UPI speed mismatch was detected.

The integrated BMC may generate LED codes based on detection of failure conditions. These LED codes are translated into visual LED sequences each time the problem is discovered, such as on each power-up attempt, but are not lit continuously.

Codes that are common across Intel server boards and systems that use same generation chipset are listed in the following table. Each digit in the code is represented by corresponding number of LED flashes.

Table 40. BMC POST Error LED Codes

LED Sequence	Reason for LED Blink	Associated Sensors
1-5-1-2	VR watchdog timer sensor assertion.	VR watchdog timer
1-5-1-4	A PSU reports a failure, or the BMC detects the presence of a PSU model that is incompatible with one or more other PSUs in the system.	PS status
1-5-2-1	No CPUs installed or the first CPU socket is empty.	CPU missing sensor
1-5-2-2	CPU CAT Error (IERR) assertion.	CPU Status sensor.
1-5-2-3	CPU ERR2 timeout assertion.	CPU ERR2 Timeout sensor.
1-5-2-4	MSID mismatch occurs if a processor is installed into a system board that has incompatible power capabilities.	MSID mismatch sensor
1-5-2-5	CPU population error.	CPU 0 Status sensor.
1-5-4-2	DC power unexpectedly lost (power good dropout): Power unit sensors report power unit failure offset.	Power fault
1-5-4-4	Power control fault (power good assertion timeout).	Power unit: Soft power control failure offset

D.2 Processor Initialization Error Summary

The table below describes mixed processor conditions and actions for all Intel server boards and Intel server systems designed with the Intel® Xeon® Scalable processor family architecture. The errors fall into one of the following categories:

- **Fatal**: The system halts with a halt error code on the diagnostic LEDs and a corresponding sequence consisting of three long flashes and one short flash is sent to the POST Error Code LED. The system cannot boot unless the error is resolved. The faulty component must be replaced.
- **Major**: If the BIOS Setup option “POST Error Pause” is enabled, the system goes directly to the BIOS setup Error Manager to display the error and logs the POST error code to SEL. User intervention is required to continue booting the system. If the BIOS Setup option “POST Error Pause” is disabled, the system continues to boot and no prompt for the error is given, although the POST error code is logged to the BIOS Setup Error Manager and to the SEL.
- **Minor:** An error message may be displayed on the POST screen or in the BIOS Setup Error Manager screen and the POST error code is logged to the SEL. The system continues booting in a degraded state. The user may want to replace the erroneous unit. The “POST Error Pause” option setting in the BIOS setup utility does not affect this error.

Table 41. Mixed Processor Configurations Error Summary

Error	Severity	System Action when BIOS Detects the Error Condition
Processor family not identical	Fatal	• Halts with error code “0xE5” on the diagnostic LED. • Sends three long flashes and one short flash to the POST Error LED. • Does not boot until the fault condition is remediated.
Processor model not identical	Fatal	• Halts with error code “0xE5” on the diagnostic LED. • Sends three long flashes and one short flash to the POST Error LED. • Does not boot until the fault condition is remediated.
Processor cache or home agent not identical	Fatal	• Halts with error code “0xE5” on the diagnostic LED. • Sends three long flashes and one short flash to the POST Error LED. • Does not boot until the fault condition is remediated.
Processor frequency (speed) not identical	Fatal	• Halts with error code “0xE5” on the diagnostic LED. • Sends three long flashes and one short flash to the POST Error LED. • Does not boot until the fault condition is remediated.
Processor Intel® UPI link frequencies not identical	Fatal	• Halts with error code “0xE5” on the diagnostic LED. • Sends three long flashes and one short flash to the POST Error LED. • Does not boot until the fault condition is remediated.
Processor microcode update failed	Major	• Logs the POST error code “81 6x” into the SEL. • If the “POST Error Pause” is enabled in the BIOS Setup, loads the BIOS Error Manager to present error message “816x: Processor 0x unable to apply microcode update” on the screen. • If the “POST Error Pause” is disabled in the BIOS Setup continues to boot in a degraded state.
Processor microcode update missing	Minor	• Logs the POST error code “81 8x” into the SEL. • The system continues to boot in a degraded state, regardless of the “POST Error Pause” setting in the BIOS setup. • The Error Manager in BIOS Setup will present the message “818x: Processor microcode update not found”

Appendix E. Supported System Configurations for Thermal Compatibility

E1. Thermal Configuration Tables for air-cooled systems

Intel® Server D50DNP Family is thermally designed in compliance with ASHRAE Class A2 environment guidance. Multiple systems configurations were thermally tested with different ambient temperatures ranged from 15℃ to 35℃ at lab environment below 300 meter altitude with different stress modes.

To maintain proper airflow inside the chassis, each chassis slot not occupied by a module must be filed with 1U module blank.

It is necessary to populate all memory slots with either memory modules or DIMM blanks for air-cooled configurations.

It is necessary to install PSU blank in each empty PSU slot of the system.

Mixing different types of modules in the same chassis can only be done as follows:

- Up to two 1U air-cooled compute modules with one 2U management module.

For mixed module configurations, the customer must consider the lowest ambient temperature required by the installed processors in the modules.

Fan failure mode means that more than one fan rotor in the same fan or different fans are no longer operational and fan redundancy is lost.

SSD throughput throttling is expected when SSD SMART thermal sensor exceeds 70°C.

M.2 SSD drives are intended to store and boot an OS and may experience performance degradation under heavy workload.

If a user installs any U.2 NVMe SSD that does not allow BMC to read value of its thermal sensor, the user should manually switch fan profile to “Performance” mode in BIOS Setup utility.

If a user installs any GPGPU add-in card that does not allow BMC to read value of its thermal sensor, the user should manually switch fan profile to “Performance” mode in BIOS Setup utility.

Air velocity requirements for PCIe* add-in cards defined by the PCIe SIG are shown on the next picture.

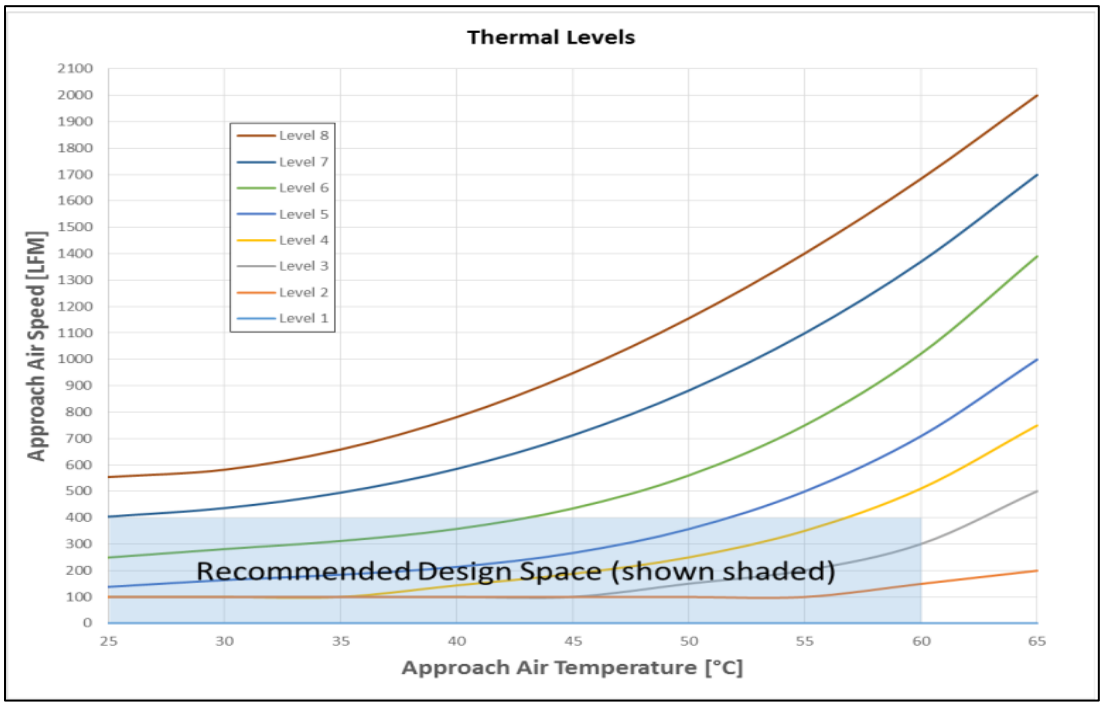


Figure 60. PCIe SIG Add-in cards thermal levels

Table 42. Thermal testing results interpretation for air-cooled systems

● ●	System is capable of full performance
● ○	System is capable of full performance but may throttle in fan failure mode
○ ○	System may experience some performance loss at high workloads
● -	System capable of full performance but system cooling is not redundant
○ -	System may experience some performance loss and cooling is not redundant
-	Configuration is not supported

Table 43. Supported Configurations for Intel® Server D50DNP1MHCPAC, 1U Compute Module, Air-cooled

Intel® Server D50DNP1MHCPAC, 1U Compute Modules, Air-cooled								
Max Ambient Temperature	**15°C**	**20°C**	**25°C**	**27°C**	**32°C**	**35°C**	**40°C**	**45°C**
CPU Model	**CPU Support**							
Intel® Xeon® Gold 5415+ , 150W , 8C	● ●	● ●	● ●	● ●	● ●	● ○	● -	-
Intel® Xeon® Gold 5416S , 150W , 16C	● ●	● ●	● ●	● ●	● ●	● ○	● -	-
Intel® Xeon® Gold 6416H , 165W , 18C	● ●	● ●	● ●	● ●	● ●	● ○	● -	-
Intel® Xeon® Gold 6426Y , 185W , 16C	● ●	● ●	● ●	● ●	● ○	● -	-	-
Intel® Xeon® Gold 5418Y , 185W , 24C	● ●	● ●	● ●	● ●	● ○	● -	-	-
Intel® Xeon® Gold 6418H , 185W , 24C	● ●	● ●	● ●	● ●	● ○	● -	-	-
Intel® Xeon® Gold 6434 , 195W , 8C	● ●	● ●	○ ○	○ ○	-	-	-	-
Intel® Xeon® Gold 6434H , 195W , 8C	● ●	● ●	○ ○	○ ○	-	-	-	-
Intel® Xeon® Gold 5420+ , 205W , 28C	● ●	● ●	● ●	● ●	● ○	● -	-	-
Intel® Xeon® Gold 6438M , 205W , 32C	● ●	● ●	● ●	● ●	● ○	● -	-	-
Intel® Xeon® Gold 6438Y+ , 205W , 32C	● ●	● ●	● ●	● ●	● ○	○ -	-	-
Intel® Xeon® Gold 6442Y , 225W , 24C	● ●	● ●	● ●	● ○	○ -	-	-	-
Intel® Xeon® Gold 6448Y , 225W , 32C	● ●	● ●	● ●	● ○	○ -	-	-	-
Intel® Xeon® Platinum 8450H , 250W , 28C	● ●	● ●	● ○	● ○	-	-	-	-
Intel® Xeon® Gold 6448H , 250W , 32C	● ●	● ●	● ○	● ○	-	-	-	-
Memory Type	**Memory Support**							
DDR5, DRx8, 1x, 1DPC	● ●	● ●	● ●	● ●	● ●	● ●	● ●	● ●
DDR5, DRx4, 1x, 1DPC	● ●	● ●	● ●	● ●	● ●	● ●	○ ○	-
DDR5, QRx4, 1x, 1DPC	● ●	● ●	● ●	● ●	● ○	○ ○	-	-
DDR5, DRx8, 1x, 2DPC	● ●	● ●	● ●	● ●	● ●	● ●	● ●	● ●
DDR5, DRx4, 1x, 2DPC	● ●	● ●	● ●	● ●	● ●	● ●	● ●	● ●
DDR5, QRx4, 1x, 2DPC	● ●	● ●	● ●	● ●	● ●	● ●	● ●	● ○
DDR5, DRx8, 2x, 1DPC	● ●	● ●	● ●	● ●	● ●	● ●	● ●	● ●
DDR5, DRx4, 2x, 1DPC	● ●	● ●	● ●	● ●	● ●	● ●	● ●	● ○
DDR5, QRx4, 2x, 1DPC	● ●	● ●	● ●	● ●	● ●	● ●	● ○	○ ○
DDR5, DRx8, 2x, 2DPC	● ●	● ●	● ●	● ●	● ●	● ●	● ●	● ●
DDR5, DRx4, 2x, 2DPC	● ●	● ●	● ●	● ●	● ●	● ●	● ●	● ●
DDR5, QRx4, 2x, 2DPC	● ●	● ●	● ●	● ●	● ●	● ●	● ●	● ●
M.2 NVMe* SSD	**M.2 NVMe SSD Support**							
Micron* 7400 PRO 960GB (rated to 70° C)	● ●	● ●	● ●	● ●	● ●	● ●	● ○	○ -
2700W PSU FCXX27CRPSA	**PSU Support**							
with CPUs 150W to 165W TDP installed	● ●	● ●	● ●	● ●	● ●	● ○	● -	-

with CPUs 185W to 205W TDP installed	● ●	● ●	● ●	● ●	● ○	● -	-	-
with CPUs 225W to 250W TDP installed	● ●	● ●	● ●	● ●	-	-	-	-
PCIe* Add-in Cards Cooling Capacity	**Supported PCIe SIG Airflow Levels**							
PCIe Slot 1	8 / 8	8 / 8	8 / 8	8 / 8	8 / 8	8 / 8	8 / 8	8 / 7
PCIe Slot 2	8 / 8	8 / 8	8 / 8	8 / 8	8 / 8	8 / 8	8 / 8	8 / 7

Table 44. Supported Configurations for Intel® Server D50DNP1MHEVAC, 1U Compute Module, Air-cooled with EVAC Heat Sink

Intel® Server D50DNP1MHEVAC, 1U Compute Module, Air-cooled, EVAC								
Max Ambient Temperature	**15°C**	**20°C**	**25°C**	**27°C**	**32°C**	**35°C**	**40°C**	**45°C**
CPU Model	**CPU Support**							
Intel® Xeon® Gold 5415+ , 150W , 8C	● ●	● ●	● ●	● ●	● ●	● ●	● ●	-
Intel® Xeon® Gold 5416S , 150W , 16C	● ●	● ●	● ●	● ●	● ●	● ●	● ●	-
Intel® Xeon® Gold 6416H , 165W , 18C	● ●	● ●	● ●	● ●	● ●	● ○	● -	-
Intel® Xeon® Gold 6426Y , 185W , 16C	● ●	● ●	● ●	● ●	● ●	● ○	-	-
Intel® Xeon® Gold 5418Y , 185W , 24C	● ●	● ●	● ●	● ●	● ●	● ○	-	-
Intel® Xeon® Gold 6418H , 185W , 24C	● ●	● ●	● ●	● ●	● ●	● ○	-	-
Intel® Xeon® Gold 6434 , 195W , 8C	● ●	● ●	● ○	○ ○	○ ○	-	-	-
Intel® Xeon® Gold 6434H , 195W , 8C	● ●	● ●	● ○	○ ○	○ ○	-	-	-
Intel® Xeon® Gold 5420+ , 205W , 28C	● ●	● ●	● ●	● ●	● ●	● ○	-	-
Intel® Xeon® Gold 6438M , 205W , 32C	● ●	● ●	● ●	● ●	● ●	● ○	-	-
Intel® Xeon® Gold 6438Y+ , 205W , 32C	● ●	● ●	● ●	● ●	● ○	○ ○	-	-
Intel® Xeon® Gold 6442Y , 225W , 24C	● ●	● ●	● ●	● ●	● ○	-	-	-
Intel® Xeon® Gold 6448Y , 225W , 32C	● ●	● ●	● ●	● ●	● ○	-	-	-
Intel® Xeon® Platinum 8450H , 250W , 28C	● ●	● ●	● ●	● ●	-	-	-	-
Intel® Xeon® Gold 6448H , 250W , 32C	● ●	● ●	● ●	● ●	-	-	-	-
Intel® Xeon® Platinum 8444H, 270W, 16C	● ●	● ●	● ○	-	-	-	-	-
Intel® Xeon® Gold 6444Y , 270W , 16C	● ●	● ○	○ ○	-	-	-	-	-
Intel® Xeon® Gold 6430 , 270W , 32C	● ●	● ●	● ○	-	-	-	-	-
Intel® Xeon® Gold 6454S , 270W , 32C	● ●	● ●	● ○	-	-	-	-	-
Intel® Xeon® Platinum 8454H , 270W , 32C	● ●	● ●	● ○	-	-	-	-	-
Memory Type	**Memory Support**							
DDR5, DRx8, 1x, 1DPC	● ●	● ●	● ●	● ●	● ●	● ●	● ●	● ○
DDR5, DRx4, 1x, 1DPC	● ●	● ●	● ●	● ●	● ○	● ○	○ ○	-
DDR5, QRx4, 1x, 1DPC	● ●	● ●	● ●	● ○	○ ○	-	-	-
DDR5, DRx8, 1x, 2DPC	● ●	● ●	● ●	● ●	● ●	● ●	● ●	● ●
DDR5, DRx4, 1x, 2DPC	● ●	● ●	● ●	● ●	● ●	● ●	● ●	● ○
DDR5, QRx4, 1x, 2DPC	● ●	● ●	● ●	● ●	● ●	● ●	● ○	○ ○
DDR5, DRx8, 2x, 1DPC	● ●	● ●	● ●	● ●	● ●	● ●	● ●	● ●
DDR5, DRx4, 2x, 1DPC	● ●	● ●	● ●	● ●	● ●	● ●	● ○	○ ○
DDR5, QRx4, 2x, 1DPC	● ●	● ●	● ●	● ●	● ●	● ○	○ ○	-
DDR5, DRx8, 2x, 2DPC	● ●	● ●	● ●	● ●	● ●	● ●	● ●	● ●
DDR5, DRx4, 2x, 2DPC	● ●	● ●	● ●	● ●	● ●	● ●	● ●	● ●
DDR5, QRx4, 2x, 2DPC	● ●	● ●	● ●	● ●	● ●	● ●	● ●	● ●
M.2 NVMe* SSD	**M.2 NVMe SSD Support**							
Micron* 7400 PRO 960GB (rated to 70° C)	● ●	● ●	● ●	● ●	● ●	● ●	● ○	○ -
2700W PSU FCXX27CRPSA	**PSU Support**							
with CPUs 150W to 165W TDP installed	● ●	● ●	● ●	● ●	● ●	● ○	● -	-
with CPUs 185W to 205W TDP installed	● ●	● ●	● ●	● ●	● ○	● -	-	-
with CPUs 225W to 250W TDP installed	● ●	● ●	● ●	● ●	-	-	-	-
with CPUs 270W TDP installed	● ●	● ●	● ○	-	-	-	-	-

PCIe* Add-in Cards Cooling Capacity	Supported PCIe SIG Airflow Levels							
PCIe Slot 1	8 / 8	8 / 8	8 / 8	8 / 8	8 / 8	8 / 8	8 / 8	8 / 8

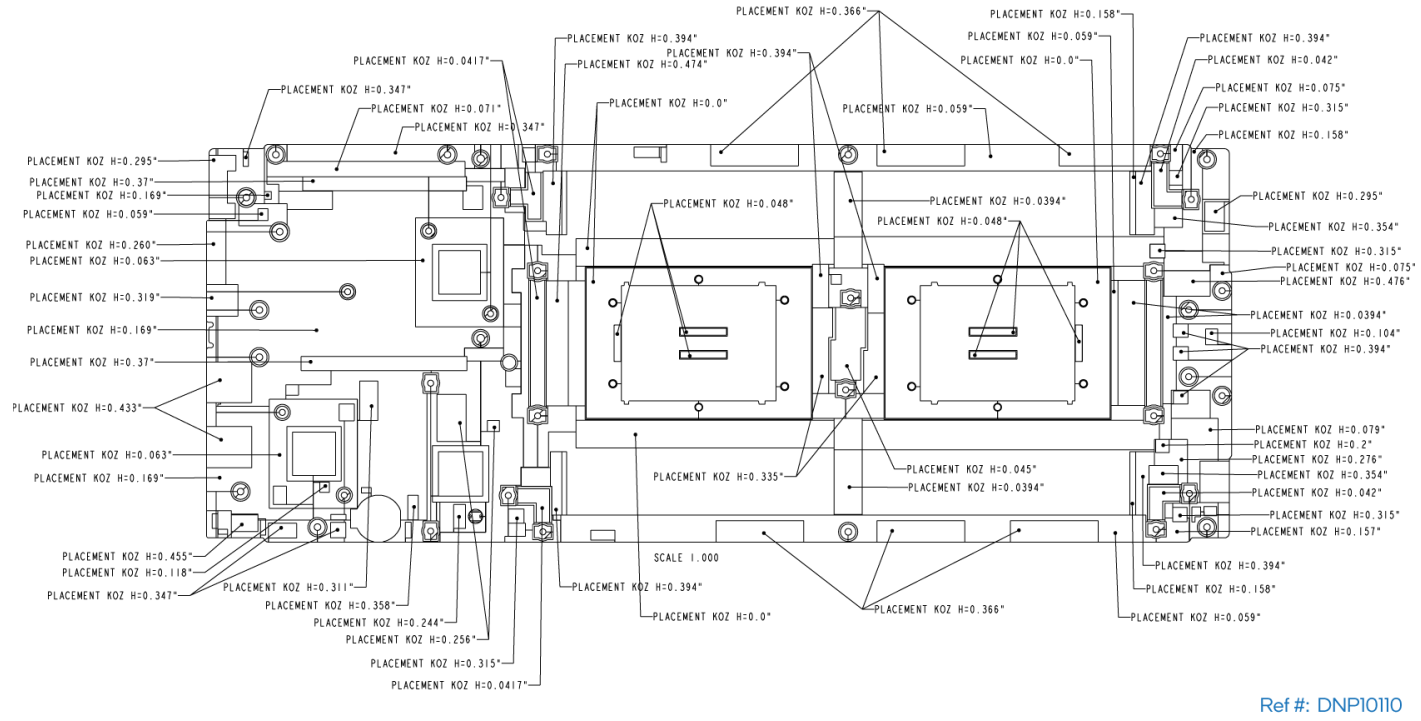
Table 45. Supported Configurations for Intel® Server D50DNP2MFALAC, 2U PCIe* Accelerator Module, Air-cooled

Intel® Server D50DNP2MFALAC, 2U PCIe* Accelerator Module, Air-cooled								
Max Ambient Temperature	**15°C**	**20°C**	**25°C**	**27°C**	**32°C**	**35°C**	**40°C**	**45°C**
CPU Model	**CPU Support**							
Intel® Xeon® Gold 5415+ , 150W , 8C	● ●	● ●	● ●	● ●	● ●	● ●	● ●	● ●
Intel® Xeon® Gold 5416S , 150W , 16C	● ●	● ●	● ●	● ●	● ●	● ●	● ●	● ●
Intel® Xeon® Gold 6416H , 165W , 18C	● ●	● ●	● ●	● ●	● ●	● ●	● ●	● ●
Intel® Xeon® Gold 6426Y , 185W , 16C	● ●	● ●	● ●	● ●	● ●	● ●	● ●	● ●
Intel® Xeon® Gold 5418Y , 185W , 24C	● ●	● ●	● ●	● ●	● ●	● ●	● ●	● ●
Intel® Xeon® Gold 6418H , 185W , 24C	● ●	● ●	● ●	● ●	● ●	● ●	● ●	● ●
Intel® Xeon® Gold 6434 , 195W , 8C	● ●	● ●	● ●	● ●	● ○	● ○	-	-
Intel® Xeon® Gold 6434H , 195W , 8C	● ●	● ●	● ●	● ●	● ○	● ○	-	-
Intel® Xeon® Gold 5420+ , 205W , 28C	● ●	● ●	● ●	● ●	● ●	● ●	● ●	● ●
Intel® Xeon® Gold 6438M , 205W , 32C	● ●	● ●	● ●	● ●	● ●	● ●	● ●	● ●
Intel® Xeon® Gold 6438Y+ , 205W , 32C	● ●	● ●	● ●	● ●	● ●	● ●	● ●	○ ○
Intel® Xeon® Gold 6442Y , 225W , 24C	● ●	● ●	● ●	● ●	● ●	● ●	● ●	● ○
Intel® Xeon® Gold 6448Y , 225W , 32C	● ●	● ●	● ●	● ●	● ●	● ●	● ●	● ○
Intel® Xeon® Platinum 8450H , 250W , 28C	● ●	● ○	● ●	● ●	● ●	● ●	● ●	● -
Intel® Xeon® Gold 6448H , 250W , 32C	● ●	● ●	● ●	● ●	● ●	● ●	● ●	● -
Intel® Xeon® Platinum 8444H, 270W, 16C	● ●	● ●	● ●	● ●	● ●	● ●	● ○	-
Intel® Xeon® Gold 6444Y , 270W , 16C	● ●	● ●	● ●	● ●	● ●	● ○	○ ○	-
Intel® Xeon® Gold 6430 , 270W , 32C	● ●	● ●	● ●	● ●	● ●	● ●	● ○	-
Intel® Xeon® Gold 6454S , 270W , 32C	● ●	● ●	● ●	● ●	● ●	● ●	● ○	-
Intel® Xeon® Platinum 8454H , 270W , 32C	● ●	● ●	● ●	● ●	● ●	● ●	● ○	-
Intel® Xeon® Platinum 8462Y+ , 300W , 32C	● ●	● ●	● ●	● ●	● ●	● ○	● -	-
Intel® Xeon® Platinum 8452Y , 300W , 36C	● ●	● ●	● ●	● ●	● ●	● ○	● -	-
Intel® Xeon® Platinum 8460Y+ , 300W , 40C	● ●	● ●	● ●	● ●	● ●	● ○	● -	-
Intel® Xeon® Platinum 8461V , 300W , 48C	● ●	● ●	● ●	● ●	● ●	● ○	● -	-
Intel® Xeon® Platinum 8460H , 330W , 40C	● ●	● ●	● ●	● ●	● ○	● ○	-	-
Intel® Xeon® Platinum 8468V , 330W , 48C	● ●	● ●	● ●	● ●	● ○	● -	-	-
Intel® Xeon® Platinum 8468H , 330W , 48C	● ●	● ●	● ●	● ●	● ○	● ○	-	-
Intel® Xeon® Platinum 8458P , 350W , 44C	● ●	● ●	● ●	● ●	● ○	● ○	-	-
Intel® Xeon® Platinum 8468 , 350W , 48C	● ●	● ●	● ●	● ●	● ○	● ○	-	-
Intel® Xeon® Platinum 8470 , 350W , 52C	● ●	● ●	● ●	● ●	● ○	● ○	-	-
Intel® Xeon® Platinum 8480+ , 350W , 56C	● ●	● ●	● ●	● ●	● ○	● ○	-	-
Intel® Xeon® Platinum 8490H , 350W , 60C	● ●	● ●	● ●	● ●	● ○	● ○	-	-
Intel® Xeon® Max 9462, 350W, 32C	● ●	● ●	● ●	● ●	● ○	● ○	-	-
Intel® Xeon® Max 9460, 350W, 40C	● ●	● ●	● ●	● ●	● ○	● ○	-	-
Intel® Xeon® Max 9468, 350W, 48C	● ●	● ●	● ●	● ●	● ○	● ○	-	-

Intel® Xeon® Max 9470, 350W, 52C	● ●	● ●	● ●	● ○	○ ○	○ ○	-	-
Intel® Xeon® Max 9480, 350W, 56C	● ●	● ●	● ●	● ○	○ ○	○ ○	-	-
Intel® Xeon® Gold 6458Q , 350W , 32C	● ●	● ○	○ ○	-	-	-	-	-
Intel® Xeon® Platinum 8470Q , 350W , 52C	● ●	● ○	○ ○	○ ○	-	-	-	-
Memory Type	**Memory Support**							
DDR5, DRx8, 1x, 1DPC	● ●	● ●	● ●	● ●	● ●	● ●	● ●	● ●
DDR5, DRx4, 1x, 1DPC	● ●	● ●	● ●	● ●	● ●	● ●	● ●	○ ○
DDR5, QRx4, 1x, 1DPC	● ●	● ●	● ●	● ●	● ●	● ●	○ ○	-
DDR5, DRx8, 1x, 2DPC	● ●	● ●	● ●	● ●	● ●	● ●	● ●	● ●
DDR5, DRx4, 1x, 2DPC	● ●	● ●	● ●	● ●	● ●	● ●	● ●	● ●
DDR5, QRx4, 1x, 2DPC	● ●	● ●	● ●	● ●	● ●	● ●	● ●	● ●
DDR5, DRx8, 2x, 1DPC	● ●	● ●	● ●	● ●	● ●	● ●	● ●	● ●
DDR5, DRx4, 2x, 1DPC	● ●	● ●	● ●	● ●	● ●	● ●	● ●	● ●
DDR5, QRx4, 2x, 1DPC	● ●	● ●	● ●	● ●	● ●	● ●	● ●	● ○
DDR5, DRx8, 2x, 2DPC	● ●	● ●	● ●	● ●	● ●	● ●	● ●	● ●
DDR5, DRx4, 2x, 2DPC	● ●	● ●	● ●	● ●	● ●	● ●	● ●	● ●
DDR5, QRx4, 2x, 2DPC	● ●	● ●	● ●	● ●	● ●	● ●	● ●	● ●
2.5" PCIe* NVMe* SSD	**2.5" PCIe NVMe SSD Support**							
Intel® Optane™ SSD DC P5800X 1.6TB (TDP=23W)	● ●	● ●	● ●	● ●	● ●	● ○	○ -	-
Intel® SSD D7-P5510 7.68TB (TDP=23W)	● ●	● ●	● ●	● ●	● ●	● ○	○ -	-
Intel® SSD D5-P5316 30.72TB (TDP=25W)	● ●	● ●	● ●	● ●	● ●	● ○	○ -	-
M.2 NVMe SSD	**M.2 NVMe SSD Support**							
Micron* 7400 PRO 960GB (rated to 70° C)	● ●	● ●	● ●	● ●	● ●	● ●	● ○	○ -
2700W PSU FCXX27CRPSA	**PSU Support**							
with CPUs 350W TDP installed	● ●	● ●	● ●	● ●	● ●	● ○	-	-
PCIe Add-in Cards Cooling Capacity	**Supported PCIe* SIG Airflow Levels**							
Riser 1, lower PCIe Slot	8 / 8	8 / 8	8 / 8	8 / 8	8 / 8	8 / 8	7 / 7	7 / 7
Riser 1, upper PCIe Slot	8 / 8	8 / 8	8 / 8	8 / 8	8 / 8	8 / 8	7 / 7	7 / 7
Riser 2, lower PCIe Slot	8 / 8	8 / 8	8 / 8	8 / 8	8 / 8	8 / 8	7 / 7	7 / 7
Riser 2, upper PCIe Slot	8 / 8	8 / 8	8 / 8	8 / 8	8 / 8	8 / 8	7 / 7	7 / 7
GPGPU card type	**GPGPU card Support**							
Nvidia* A100-80GB	● ●	● ●	● ●	● ●	● ●	● ●	○ ○	-
Nvidia* A100-40GB	● ●	● ●	● ●	● ●	● ●	● ●	● ○	-
Intel® Data Center GPU Max 300W	● ●	● ●	● ●	● ●	● ●	● ●	● ○	-

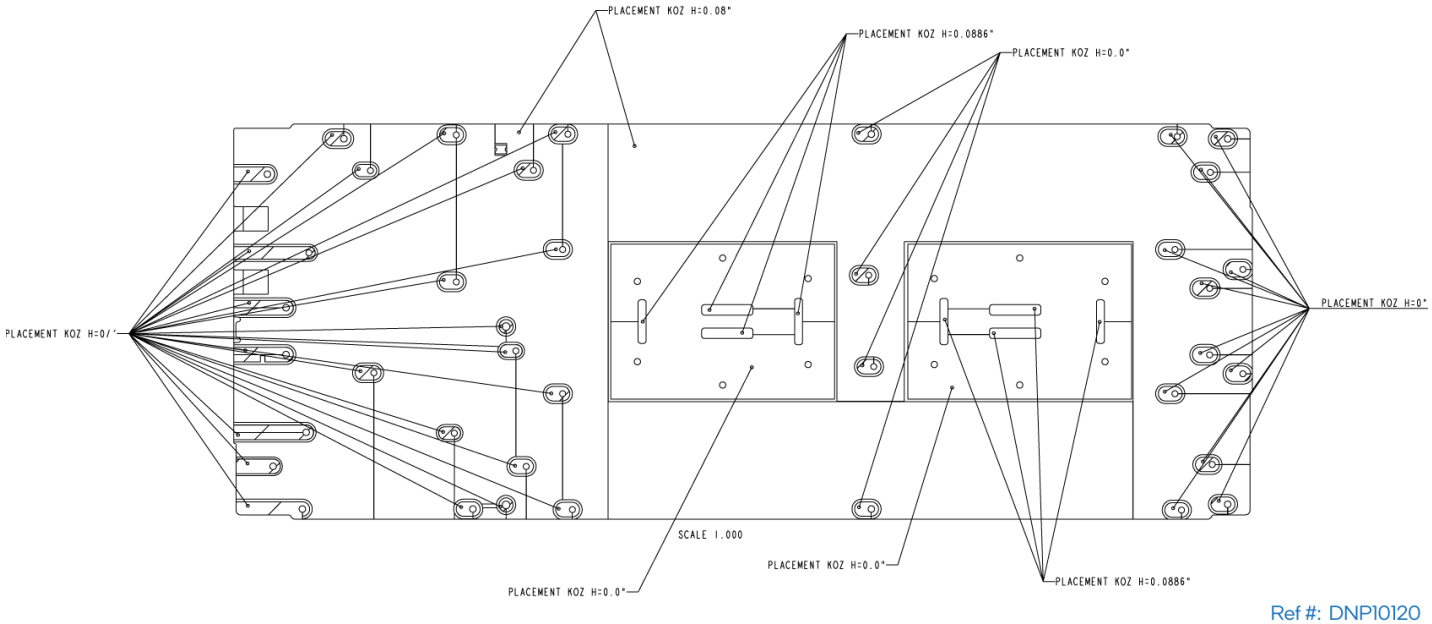
Appendix F. Server Board Mechanical Drawings

The following figures provide the server board components and holes positions and keep-out zones.



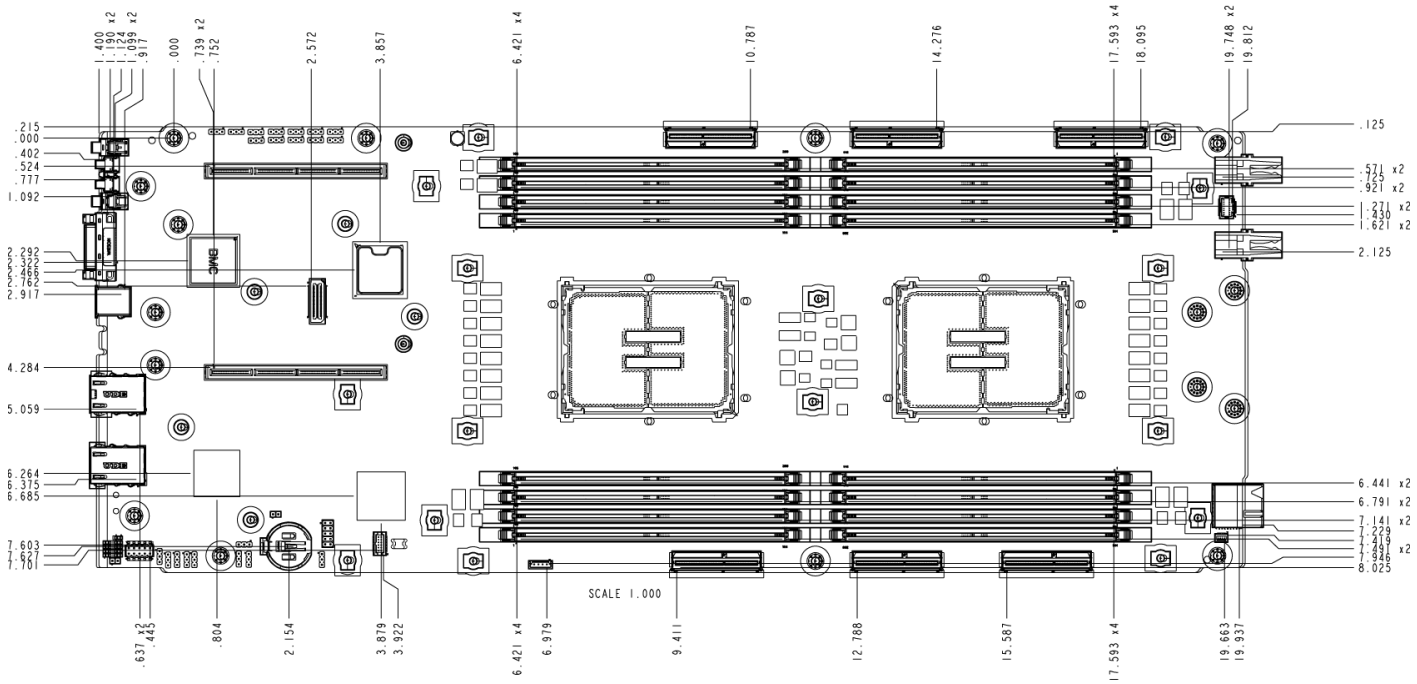
Ref #: DNP10110

Figure 61. Intel® Server Board D50DNP1SB Top Surface Keep-Out Zone



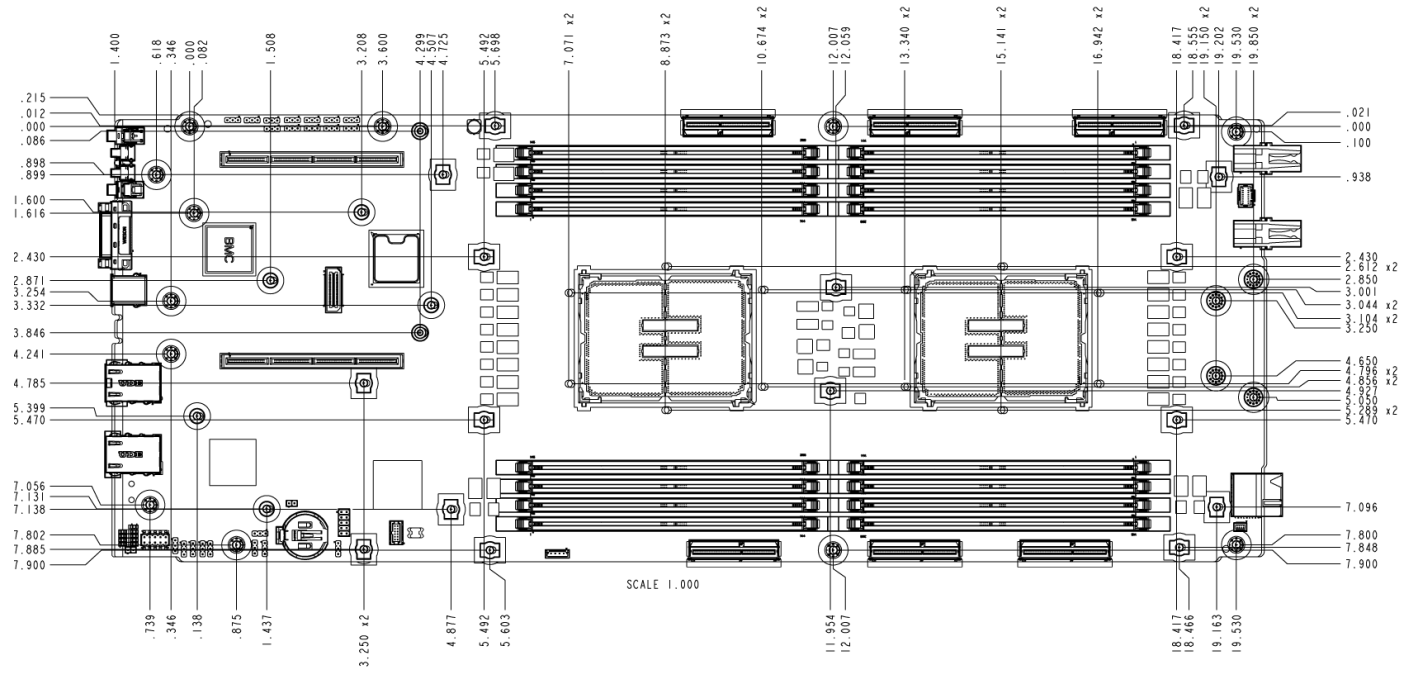
Ref #: DNP10120

Figure 62. Intel® Server Board D50DNP1SB Bottom Surface Keep-Out Zone



Ref #: DNP10130

Figure 63. Intel® Server Board D50DNP1SB Components Position



Ref #: DNP10140

Figure 64. Intel® Server Board D50DNP1SB Holes Position

Appendix G. Board Sensors

The following figure provides the location of the sensors on the Intel® Server Board D50DNP1SB. The following table provides a list of the sensors.

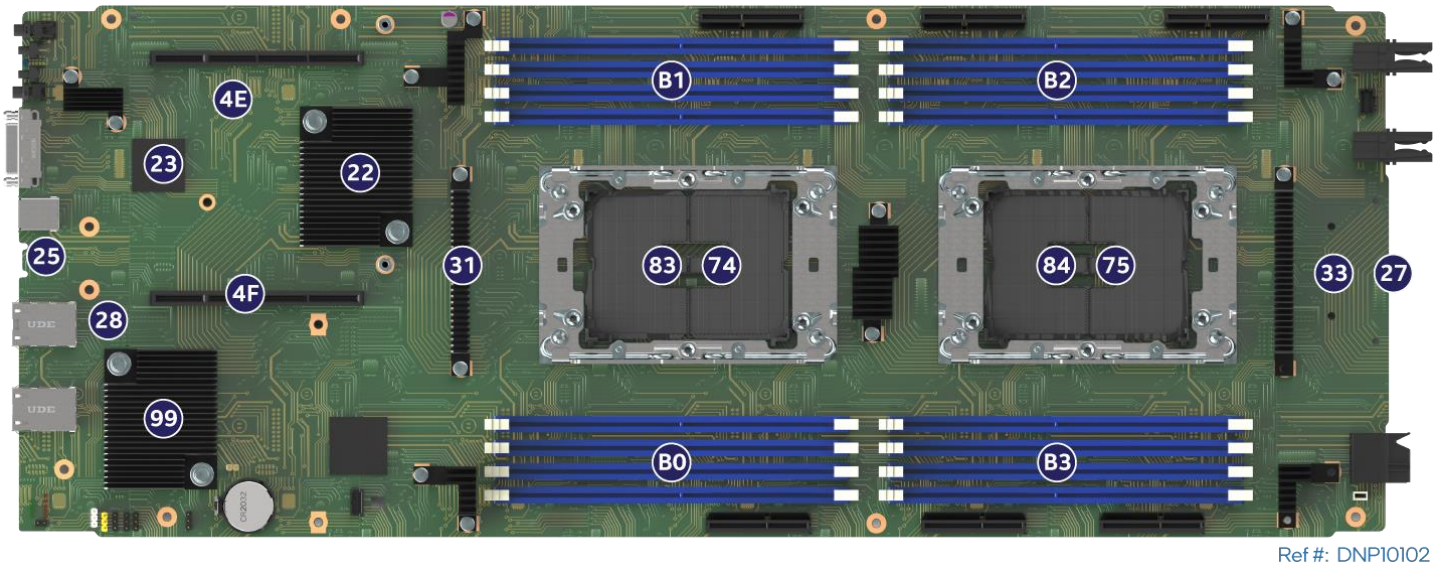


Figure 65. Intel® Server Board D50DNP1SB Sensor Map

Note: Numbers in the figure are hexadecimal numbers.

Table 46. Available Sensors Monitored by the BMC

Sensor Number	Sensor Name
22h	PCH Temp
23h	Baseboard Management Controller
25h	Baseboard Inlet Temperature
27h	Baseboard Outlet Temperature
28h	BMC LAN Temperature
31h	CPU0 VCCIN
33h	CPU1 VCCIN
4Eh	PCI Riser 1 Temperature
4Fh	PCI Riser 2 Temperature
74h	CPU0 Therm Margin
75h	CPU1 Therm Margin
83h	CPU0 DTS Therm Margin
84h	CPU1 DTS Therm Margin
B0h	DIMM Aggregate Margin CPU0 ABCD
B1h	DIMM Aggregate Margin CPU0 EFGH
B2h	DIMM Aggregate Margin CPU1 ABCD
B3h	DIMM Aggregate Margin CPU1 EFGH
99h	x710 Integrated LAN Controller Temperature

Appendix H. Server Board Installation and Component Replacement

This appendix provides general information necessary to install the server board into a server chassis. The system integrator should reference and follow all available system assembly instructions provided by the chassis manufacturer for full system assembly instructions.

This appendix also provides instructions for processor and memory replacement. Replacement instructions for all other system options should be provided by the chassis or system manufacturer.

H.1 Safety Warnings

Heed safety instructions: Before working with your server product, whether you are using this guide or any other resource as a reference, pay close attention to the safety instructions. You must adhere to the assembly instructions in this guide to ensure and maintain compliance with existing product certifications and approvals. Use only the described, regulated components specified in this guide. Use of other products/components voids the UL listing and other regulatory approvals of the product and, most likely, results in noncompliance with product regulations in one or more regions in which the product is sold.

System power on/off: The power button DOES NOT turn off the system AC power. To remove power from the system, you must unplug the AC power cord. Make sure that the AC power cord is unplugged before you open the chassis, add, or remove any components.

Hazardous conditions, devices, and cables: Hazardous electrical conditions may be present on power, telephone, and communication cables. Turn off the server and disconnect the power cord, telecommunications systems, networks, and modems attached to the server before opening it. Otherwise, personal injury or equipment damage can result.

Installing or removing jumpers: A jumper is a small plastic encased conductor that slips over two jumper pins. Some jumpers have a small tab on top that you can grip with your fingertips or with a pair of fine needle nosed pliers. If your jumpers do not have such a tab, take care when using needle nosed pliers to remove or install a jumper; grip the narrow sides of the jumper with the pliers, never the wide sides. Gripping the wide sides can damage the contacts inside the jumper, causing intermittent problems with the function controlled by that jumper. Take care to grip with, but not squeeze, the pliers or other tool you use to remove a jumper, or you may bend or break the pins on the board.

Electrostatic Discharge (ESD)

Electrostatic discharge can damage the computer or the components within it. ESD can occur without the user feeling a shock while working inside the system chassis or while improperly handling electronic devices like processors, memory or other storage devices, and add-in cards.

Intel recommends that the following steps be taken when performing any procedures described in this document or while performing service to any computer system.

- Where available, all system integration and/or service must be performed at a properly equipped ESD workstation.
- Wear ESD protective gear like a grounded antistatic wrist strap, sole grounders, and/or conductive shoes.

- Wear an anti-static smock or gown to cover any clothing that may generate an electrostatic charge
- Remove all jewelry.
- Disconnect all power cables and cords attached to the server before performing any integration or service.
- Touch any unpainted metal surface of the chassis before performing any integration or service.
- Hold all circuit boards and other electronic components by their edges only.
- After removing electronic devices from the system or from their protective packaging, place them component side up onto a grounded anti-static surface or conductive workbench pad. Do not place electronic devices onto the outside of any protective packaging.

H.2 Server Board Installation Guidelines

This section provides general guidelines and recommendations for installing the server board into a server chassis. However, Intel highly recommends that system integrators follow all installation guidelines and instructions provided by the chassis manufacturer when integrating the server board into the chosen chassis.

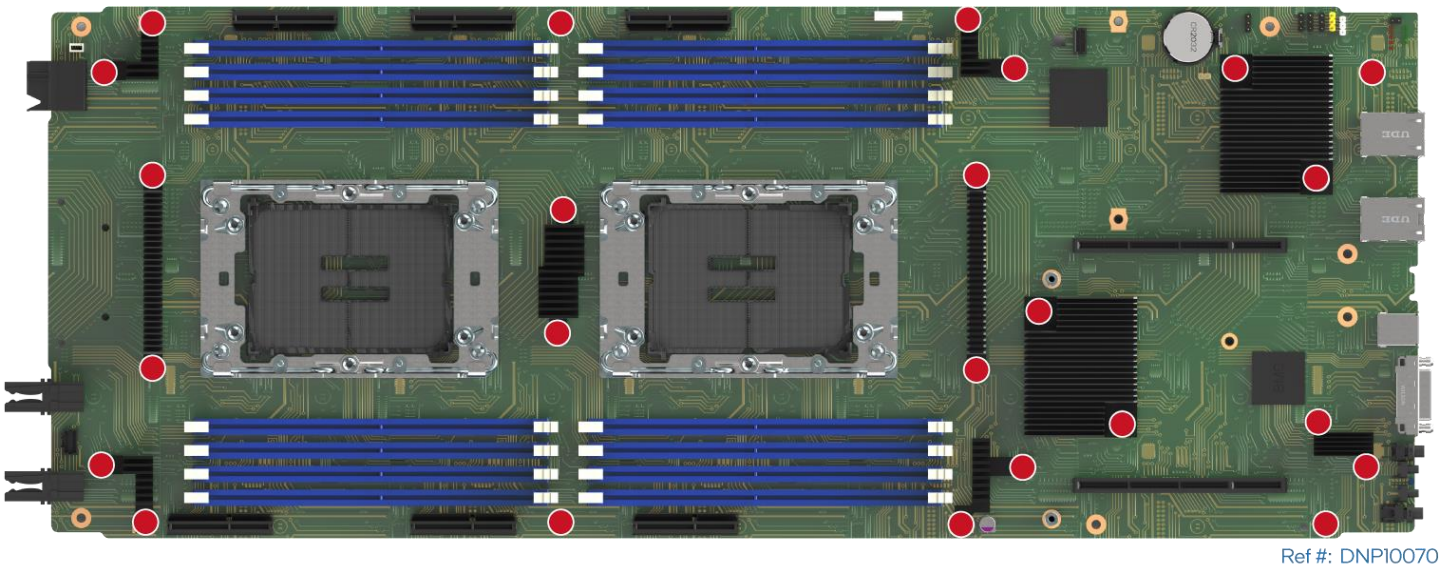


Figure 66. Server Board Mounting Hole Locations

Server chassis may use different methods for securing the server board to the chassis. The selected chassis may have integrated mounting features or they may include separate mounting stand-offs that must be installed. The following illustration identifies possible mounting options that can be used.

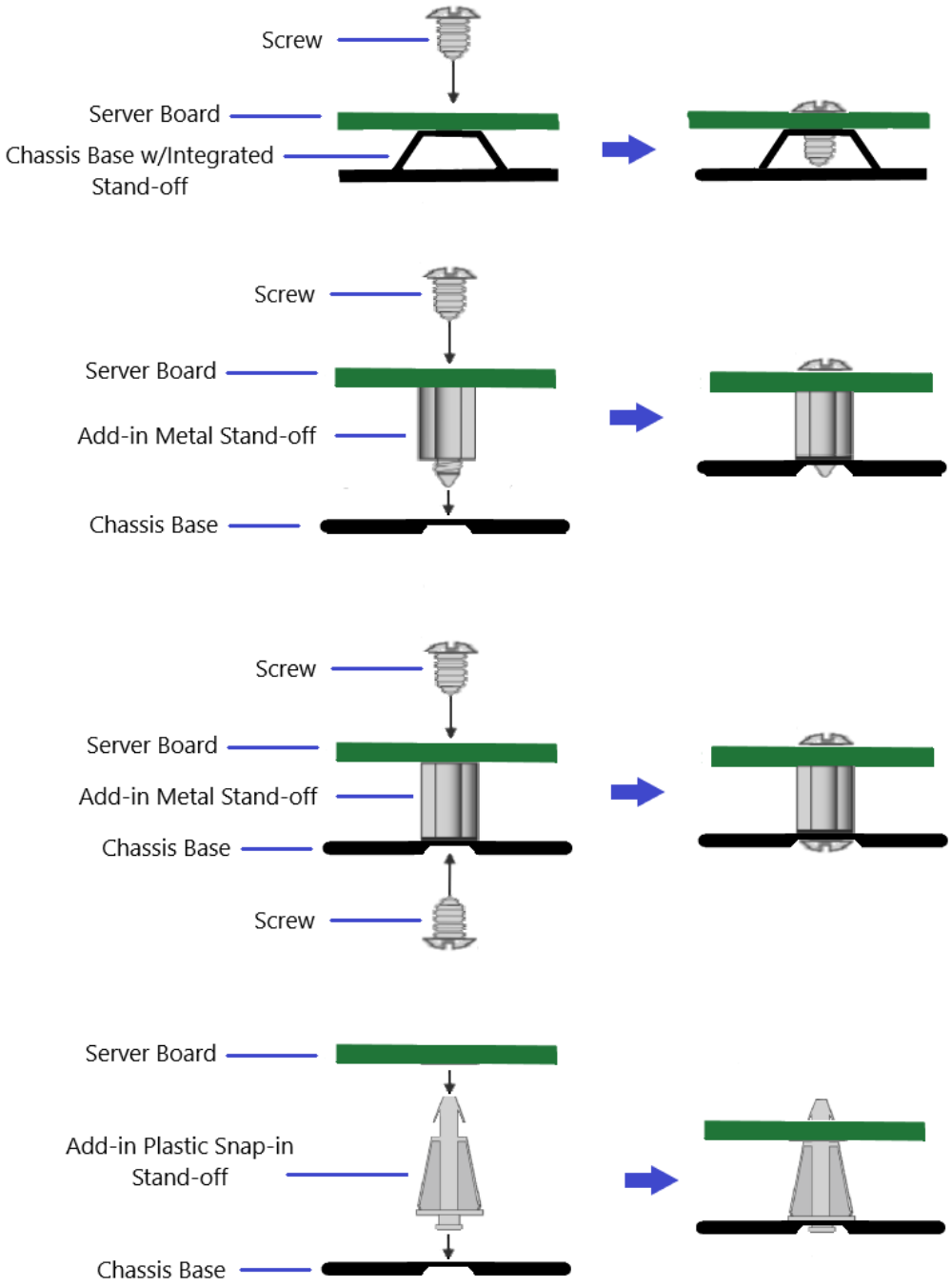


Figure 67. Possible Server Board Mounting Options

For mounting options that require the server board to be secured to the server chassis using screws, Intel recommends tightening the screws using a torque or pneumatic screwdriver. The recommended torque setting is dependent on the screw type used. See the following table.

Table 47. Server Board Mounting Screw Torque Requirements

Screw Size	Torque Value	Tolerance ±
6–32	8 in-lb.	1
M3	5 in-lb.	1

H.3 Processor Replacement

Processors are part of an assembly referred to as a processor heat sink module (PHM). A PHM consists of a processor, a processor carrier clip, and the processor heat sink that are preassembled into a single module before placement onto the processor socket assembly on the server board. The PHM concept reduces the risk of damaging pins in the processor socket during the replacement process.

The system may use 1U (low-profile) or 2U size processor heat sinks. The following procedures can be applied to either option. The following procedures apply to processor heat sinks that are used by Intel in its server systems. If the processor heat sink is different from those depicted in the next procedures, then Intel recommends following the processor replacement procedures included in documentation supplied with the chosen non-Intel server system.

H.3.1 Processor Replacement for Standard Air-Cooled Heat Sinks

Components required for each processor:

- New 4th Gen Intel® Xeon® Scalable processor in shipping tray
- Existing processor carrier clip
- New processor heat sink or existing processor clean heat sink with new thermal interface material (TIM) applied

Required tools and supplies:

- Anti-static wrist strap and conductive workbench pad (recommended)
- ESD gloves (recommended)
- Adjustable torque T-30 Torx* screwdriver

Note: The installation figures in this section only display the 1U front heat sink and processor carrier clip E1A. However, the processor installation procedure is the same, regardless of the size of the heat sink and type of processor carrier clip.

Caution:

- Fin edges of the processor heat sink are very sharp. Intel recommends wearing thin ESD protective gloves when handling the PHM during the following procedures.
- Processor heat sinks are easily damaged if handled improperly. See the following figure for proper handling.

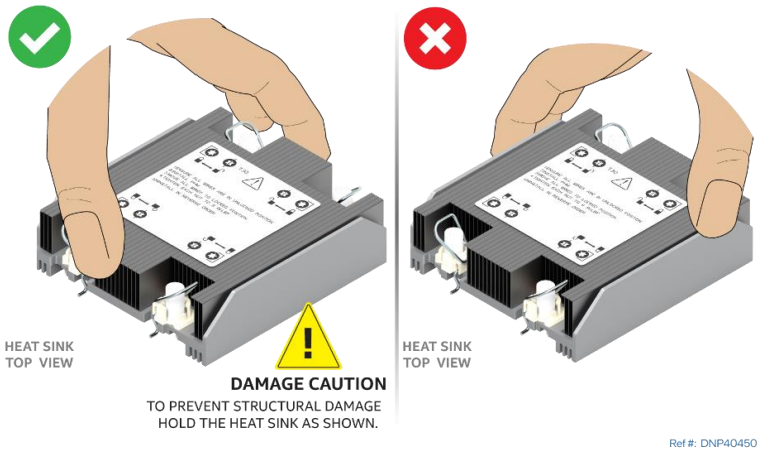


Figure 68. Processor Heat Sink Handling

H.3.1 Processor Heat Sink Module (PHM) Removal

1. Identify and locate the processor to be replaced.

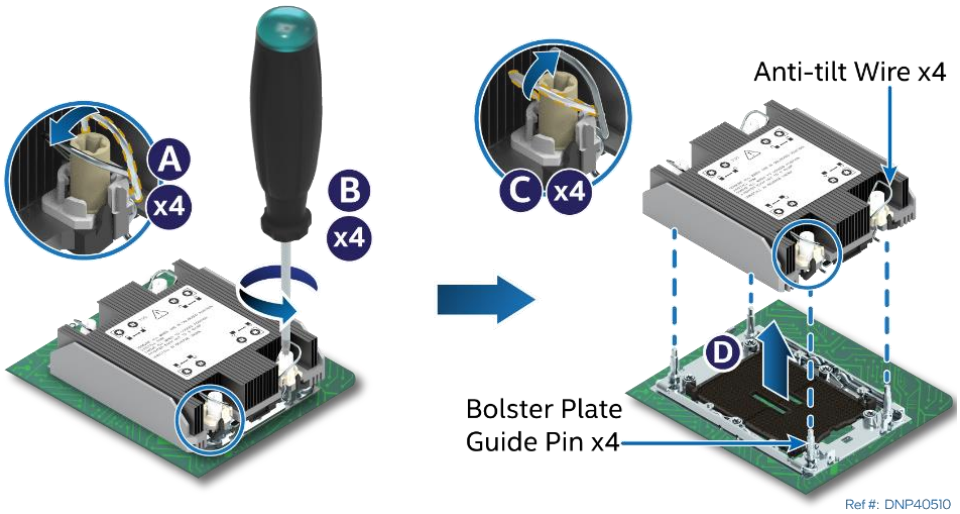


Figure 69. PHM Assembly Removal from Processor Socket

2. Ensure that the four heat sink anti-tilt wires (one located over each of the four heat sink fasteners) are in the outward position (see Letter A).
3. Using T-30 Torx* screwdriver, fully loosen all four heat sink fasteners in any order (see Letter B). General bolt loosening order, such as diagonal sequence, can be used.
4. Set all four anti-tilt wires on the heat sink to the inward position (see Letter C).
5. Carefully grasp the PHM and lift it straight up and off the server board (see Letter D).
6. With the processor facing up, set the PHM down onto a flat surface.
7. Visually inspect that the processor socket is free of damage or contamination.

Caution: If debris is observed, blow it away gently with an air blower. Do not use tweezers or any other hard tools to remove the debris.

8. If not replacing the processor, install the original plastic socket cover over the processor socket.

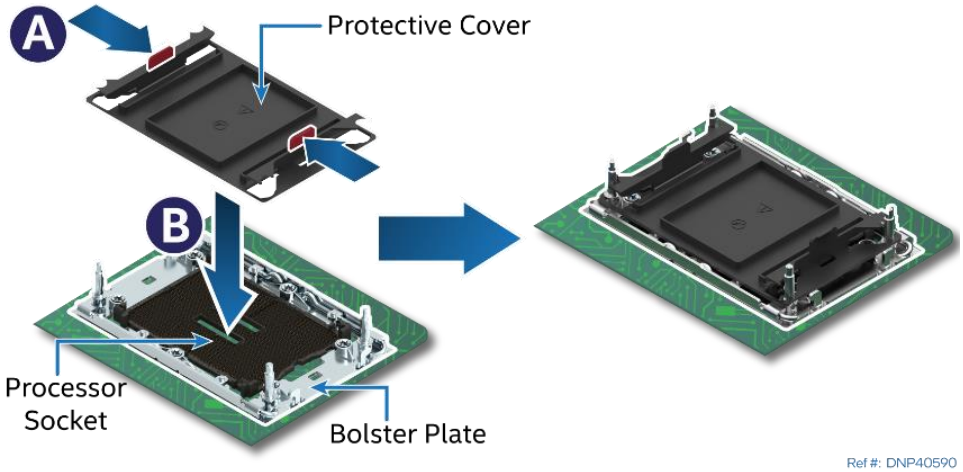


Figure 70. Reinstall the Socket Cover

- Squeeze the finger grips at each end of the cover (see Letter A).
- Carefully lower the cover over the four alignment pins of the bolster plate and onto the processor socket (see Letter B).
- Release finger grips to lock the cover in place.

- Ensure that the socket cover is locked in place.

Caution: Do not press down on the center of the socket cover.

H.3.2 PHM Disassembly

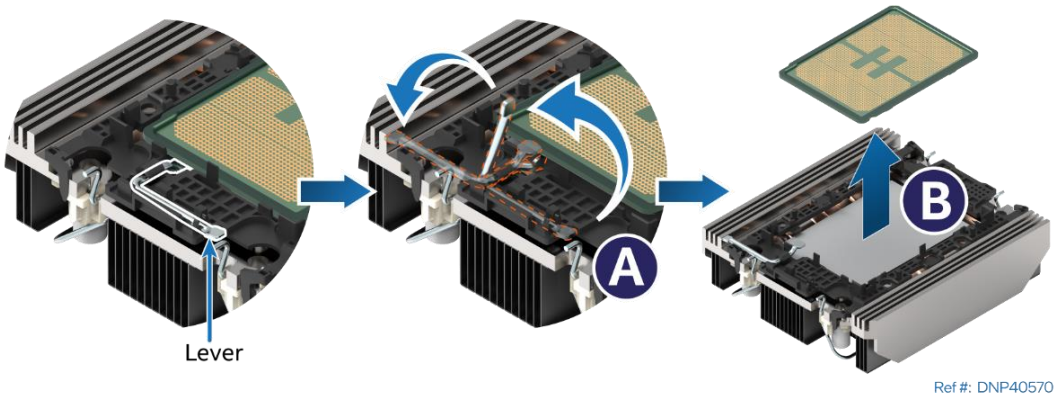


Figure 71. Processor Removal from PHM Assembly

1. While holding down the PHM, rotate the lever (see Letter A) from right to left until the processor lifts free from the processor carrier clip.
2. Holding down the processor carrier clip, carefully lift the processor out of the processor carrier clip (see Letter B).

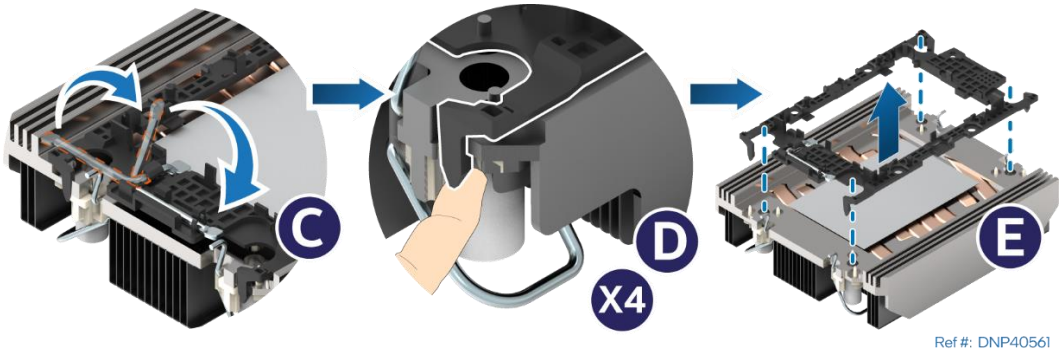


Figure 72. Processor Carrier Clip Removal from PHM Assembly

3. Return the lever to the original position (see Letter C).
4. Detach the processor carrier clip from the heat sink.
   - Unlatch the hook on each corner of the processor carrier clip (see Letter D).
   - Lift it from the heat sink (see Letter E).

The processor carrier clip for an Intel® Xeon® CPU Max series processor has slightly different mechanism to separate the processor from the heat sink. Instead of the lever, the clip has a cam mechanism on the long side on the clip. To separate an Intel® Xeon® CPU Max series processor from the heat sink and the processor carrier clip, rotate the cam with a flat head screwdriver in any direction not more than 60 degrees. After the processor is removed from the carrier clip, return the cam into its original position with the screwdriver slot in the vertical position.

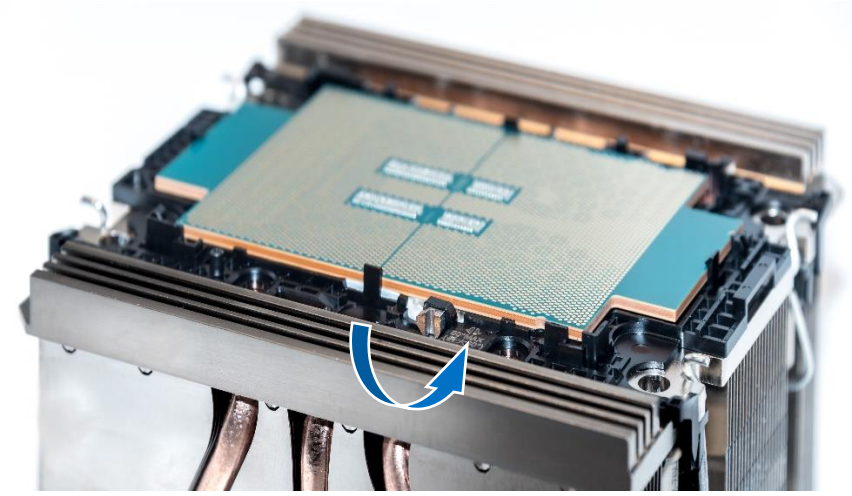


Figure 73. Intel® Xeon® CPU Max series processor removal

H.3.3 PHM Reassembly

To properly reassemble the PHM and install it onto the server board, the procedures described in the following sections must be followed in the order specified. These instructions assume that the processor heat sink (new or an existing one) has the necessary thermal interface material (TIM) Honeywell PTM7000* already applied to the clean bottom of the heat sink.

Caution: Full ESD precautions should be followed to perform reassembly of the PHM and reinstallation of the PHM to the server board. The processor itself must not be handled.

Each component in the PHM assembly includes a Pin 1 indicator. Pin 1 indicator alignment between all components is required throughout the assembly process.

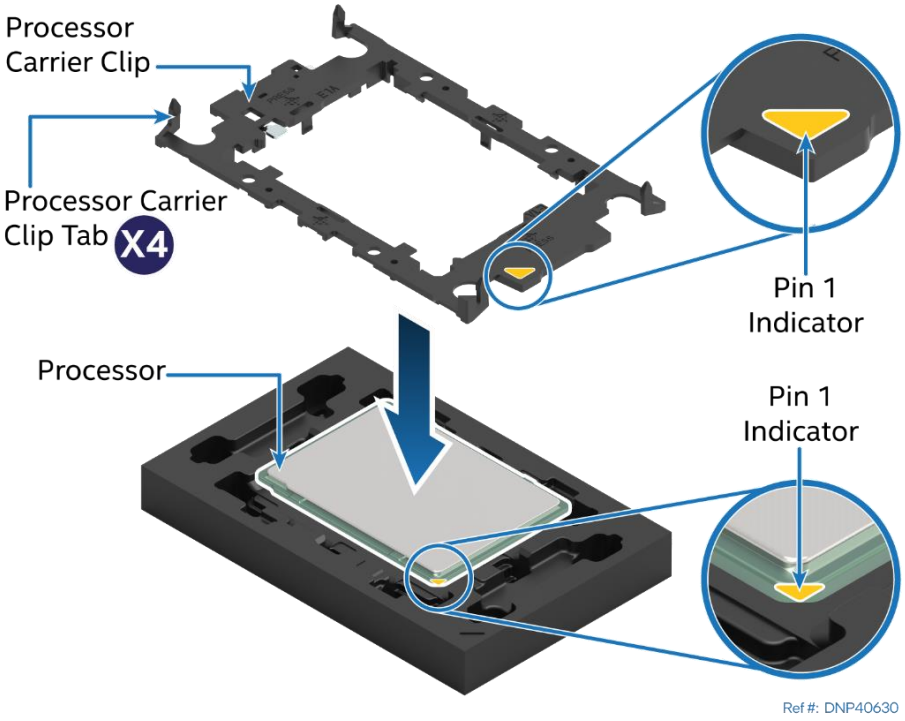


Figure 74. Installing Processor Carrier Clip onto Processor – Part 1

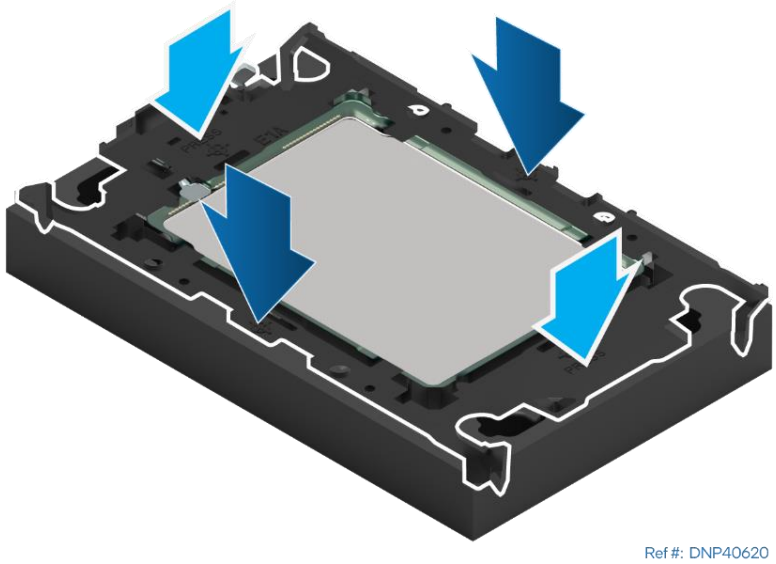


Figure 75. Installing Processor Carrier Clip onto Processor – Part 2

1. Align the Pin 1 indicator on the processor carrier clip with the Pin 1 indicator of the processor.
2. With the processor still in its shipping tray, place the processor carrier clip over the processor.
3. Gently press down simultaneously on two opposite sides of the processor carrier clip until it clicks in place.
4. Repeat step 3 for the other two sides.
5. Locate the processor heat sink. To avoid damage, grasp it by its narrower sides as shown below.

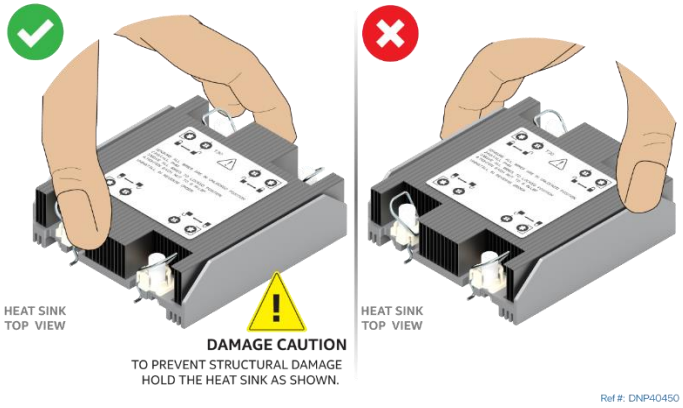


Figure 76. Processor Heat Sink Handling

6. Place the heat sink bottom side up onto a flat surface.

   If reusing an existing heat sink:

   - Thoroughly clean off existing TIM from the bottom of the heat sink.
   - Apply new TIM (Honeywell PTM7000*).

   If using a new heat sink with TIM already applied, remove the plastic protective film from the TIM pad.

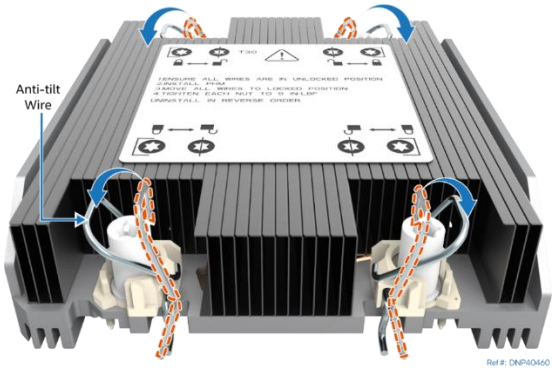


Figure 77. Processor Heat Sink Anti-Tilt Wires in the Outward Position

7. Set the anti-tilt wire over each of the four heat sink fasteners to their outward position.

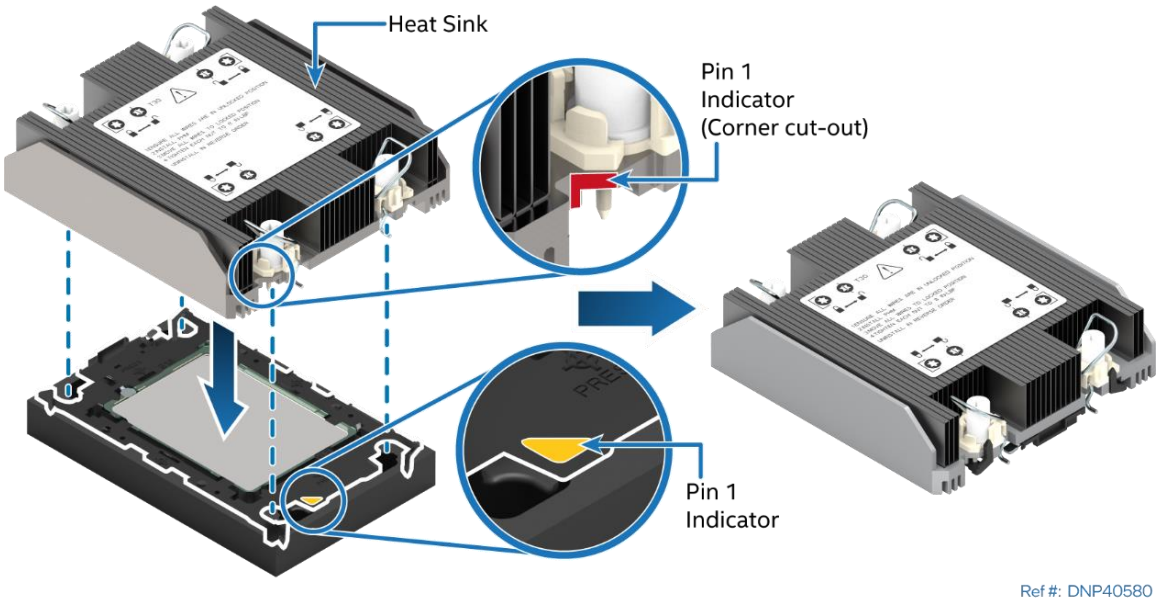


Figure 78. Pin 1 Indicator of Processor Carrier Clip

8. Align the Pin 1 indicator of processor carrier clip with one of the diagonally cut corners on the base of the heat sink. Or (if present) look for the Pin 1 indicator on the corner of the heat sink label.
9. Gently put the heat sink onto the processor carrier clip and press down until it clicks into place.
10. Ensure that all four heat sink corners are securely latched to the processor carrier clip tabs.

H.3.4 PHM Installation

1. If installed, remove the plastic cover from the processor socket.

Caution: Do not touch the socket pins. The pins inside the processor socket are extremely sensitive. A damaged processor socket may produce unpredictable system errors.

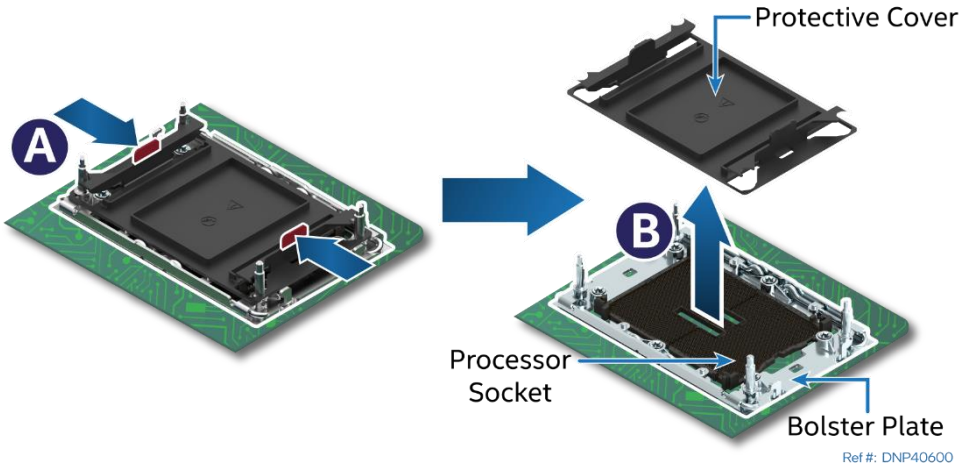


Figure 79. Socket Protective Cover Removal

2. Remove the protective cover by squeezing the finger grips (see Letter A) and pulling the cover up (see Letter B).
3. Ensure that the socket is free of damage or contamination before installing the PHM.

Caution: If debris is observed, blow it away gently with an air blower. Do not use tweezers or any other hard tools to remove the debris.

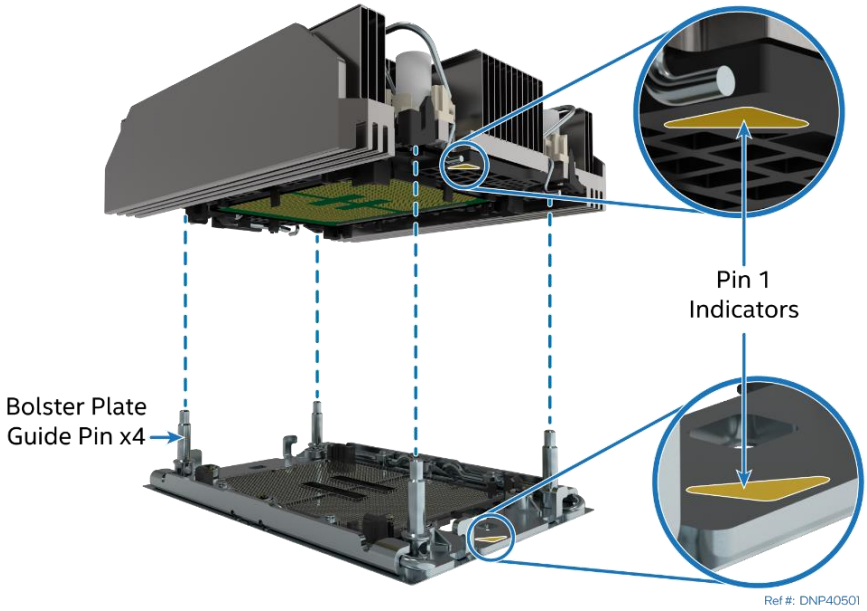


Figure 80. PHM Alignment with Socket Assembly

Caution: Processor socket pins are delicate and bend easily. Use extreme care when placing the PHM onto the processor socket. Do not drop it.

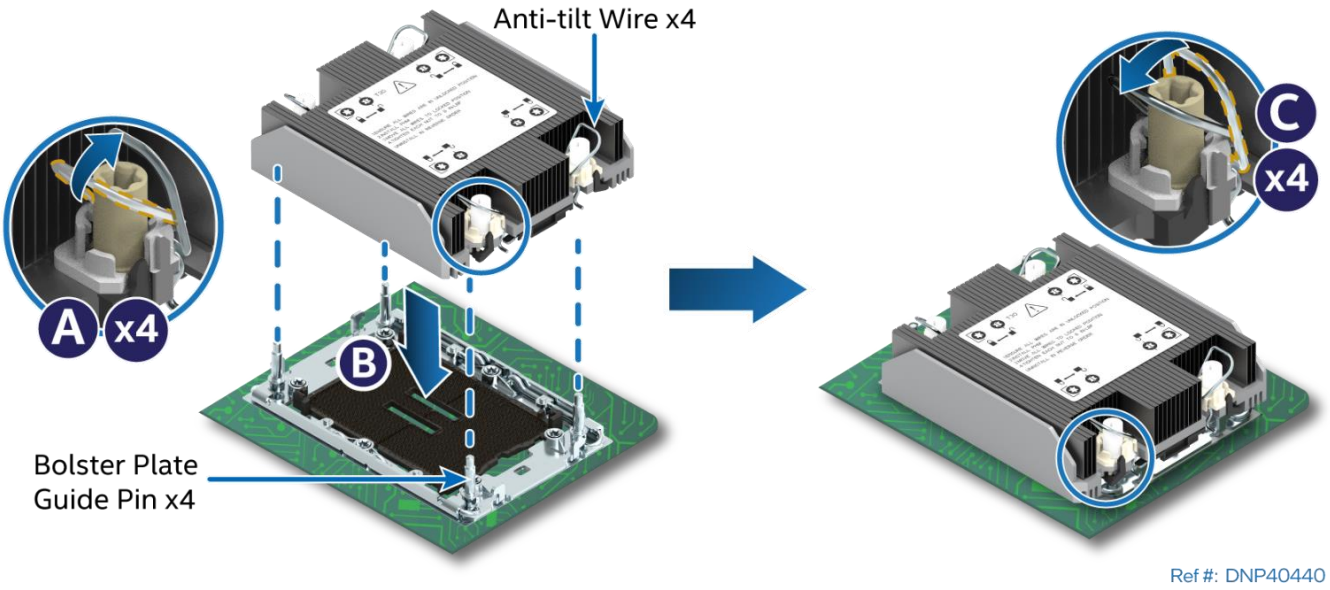


Figure 81. PHM Installation onto Server Board

4. Set all four anti-tilt wires on the heat sink to the inward position (see Letter A).
5. Align the Pin 1 indicators of the processor carrier clip and processor with the Pin 1 indicator on the socket assembly bolster plate.
6. Carefully lower the PHM over the four bolster plate alignment pins (see Letter B).
7. Ensure that the PHM is sitting flat and even on the bolster plate.
8. Set all four anti-tilt wires on the heat sink to the outward position (see Letter C).

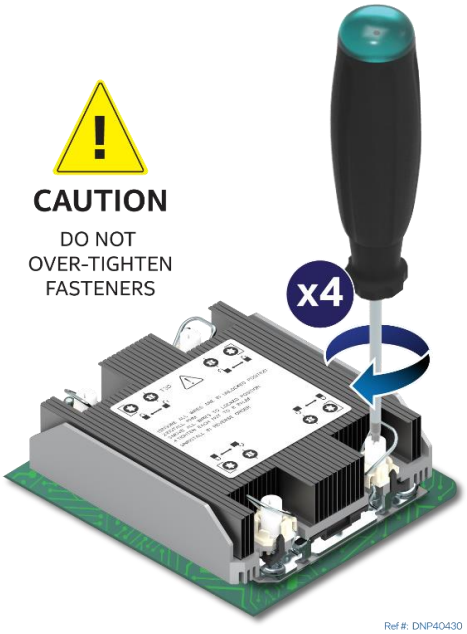


Figure 82. Tighten Heat Sink Fasteners

9. Using an adjustable torque T30 Torx* screwdriver, tighten the heat sink fasteners to 8 in-lb. No specific sequence is needed for tightening. General bolt tightening order, such as diagonal sequence, can be used.

Note: Intel strongly recommends that both processors are installed. If only one processor is installed, do not install a processor heat sink on an empty socket.

H.4 Memory Module Replacement

The Intel® Server Board D50DNP1SB supports DDR5 SDRAM RDIMMs, 3DS-RDIMMs, and 9x4 DIMMs.

Required tools and supplies:

- Anti-static wrist strap and conductive workbench pad (recommended)
- Replacement equivalent memory device

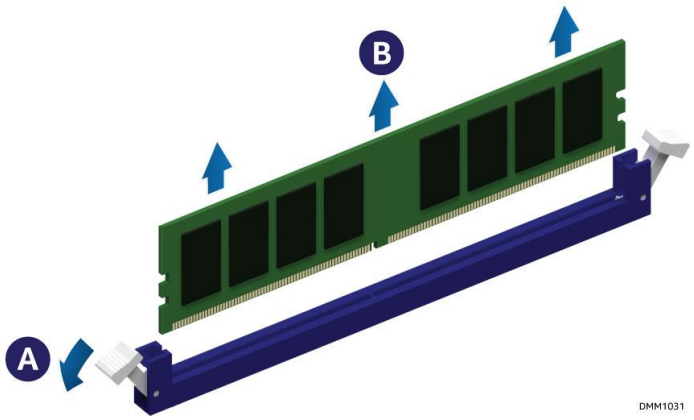


Figure 83. Removing the Memory Module from an Air-Cooled System

1. Identify and locate the memory module to be replaced.
2. Ensure that the ejection tabs of adjacent memory slots are closed.
3. Open the ejection tabs at both ends of the selected memory slot (see Letter A). The memory module slightly lifts from the slot.
4. Holding the memory module by its edges, lift it away from the slot (see Letter B).

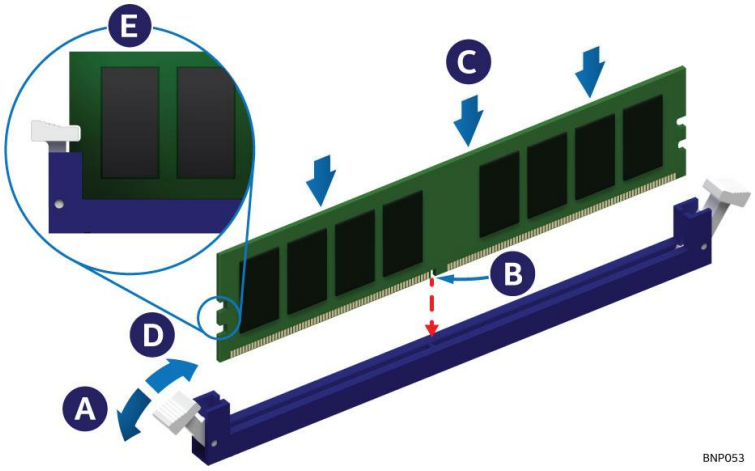


Figure 84. Installing the Memory Module in an Air-Cooled System

5. Ensure that the ejection tabs at both ends of the memory slot are in the open position (see Letter A).
6. Carefully unpack the replacement memory module, taking care to only handle the device by its outer edges.
7. Align the notch at the bottom edge of the memory module with the key in the memory slot (see Letter B).
8. Insert the memory module into the memory slot:
   a. Using even pressure along the top edge, push down on the memory module (see letter C) until the ejection tabs of the memory slot snap into place (see Letter D).
9. Ensure that the ejection tabs are firmly in place (see Letter E).

Appendix I. Software License Key Management

Some additional server features are activated by license keys. Examples are the BMC Advanced Server Management features and support of RAID volumes. There are two options available to order a software license key:

- **CTO/L9:** When ordering a fully integrated system from Intel using its on-line Configure-to-Order (CTO) tool, select the required license key (**AdvSysMgmtKey, VROCStanKey** or **VROCPremKey**) as an additional option. The Intel factory will then automatically upload the license key on to the system during the system integration process.
- **Add-on Accessory:** A software license key can be ordered separately from the system as an add-on accessory. This option requires that the license key be manually installed on the system. See the following sections for complete ordering and installation instructions.

I.1 Order and Register a License Key as an Add-on Accessory (Not via CTO)

1. Place an order for the required software license key with electronic delivery. Intel Product Codes:
   ADVSYSMGMTKEY for the Advanced System Management (ASM)
   VROCSTANKEY for the Intel® Virtual RAID on CPU Standard Software Key
   VROCPREMKEY for the Intel® Virtual RAID on CPU Premium Software Key
2. Receive an email with instructions to download the product key.
3. From the email, Click the **Register** link (see Figure 85) to go to https://lemcenter.intel.com

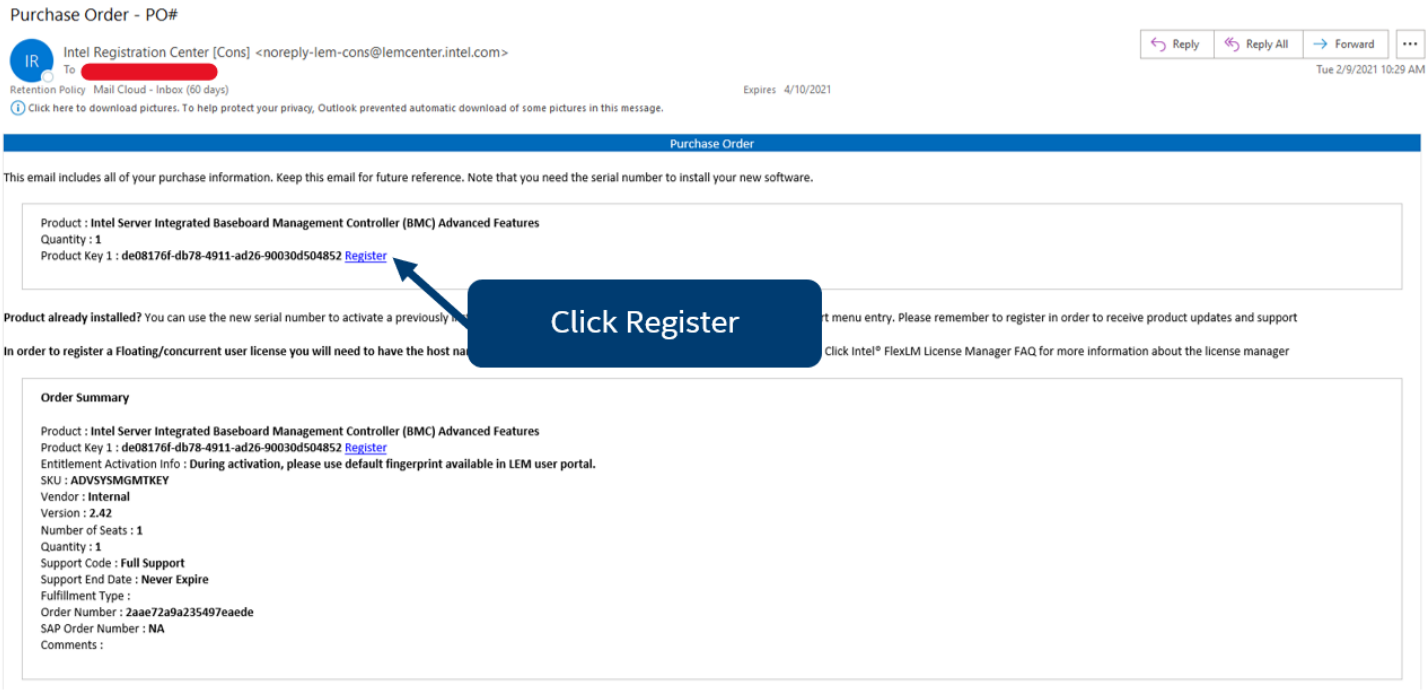


Figure 85. Example Email

4. Login using an existing Intel account or Create a new one. An email address is required

5. On the Registration Screen, Click the “Register” button to register the pre-entered license key number (see Figure 86)

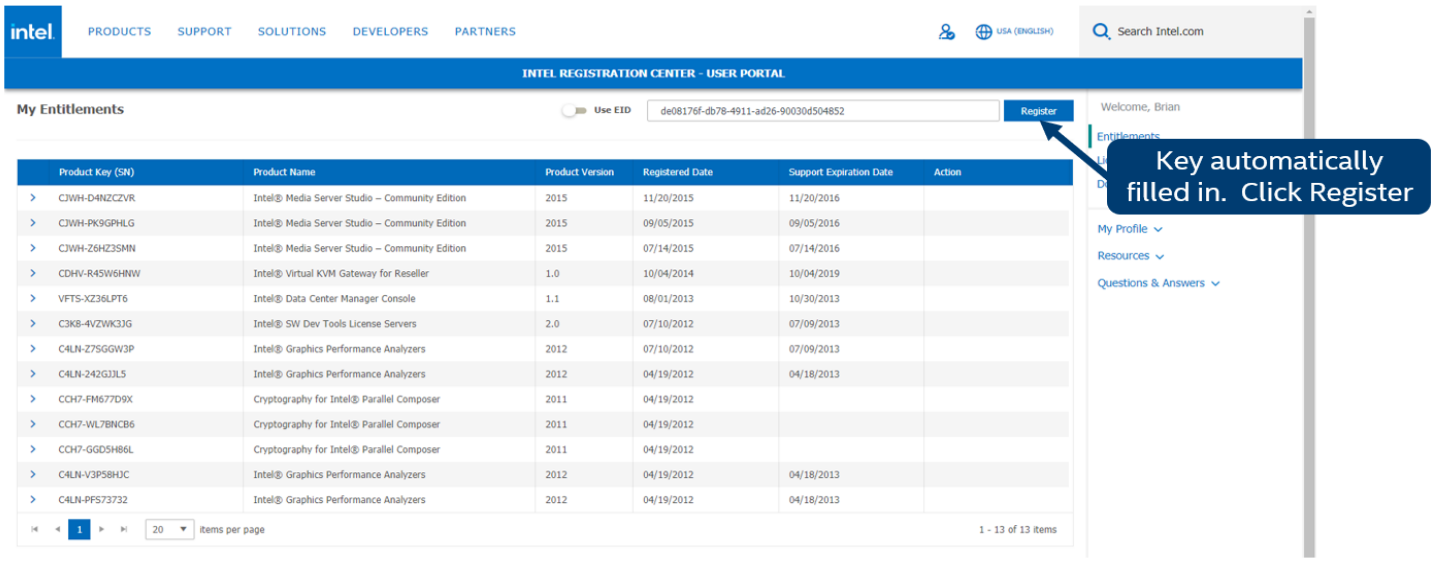


Figure 86. Register Key

6. To activate the license, click on the right arrow symbol to expand the view, scroll to the bottom and click on the Activate button. (see Figure 87)

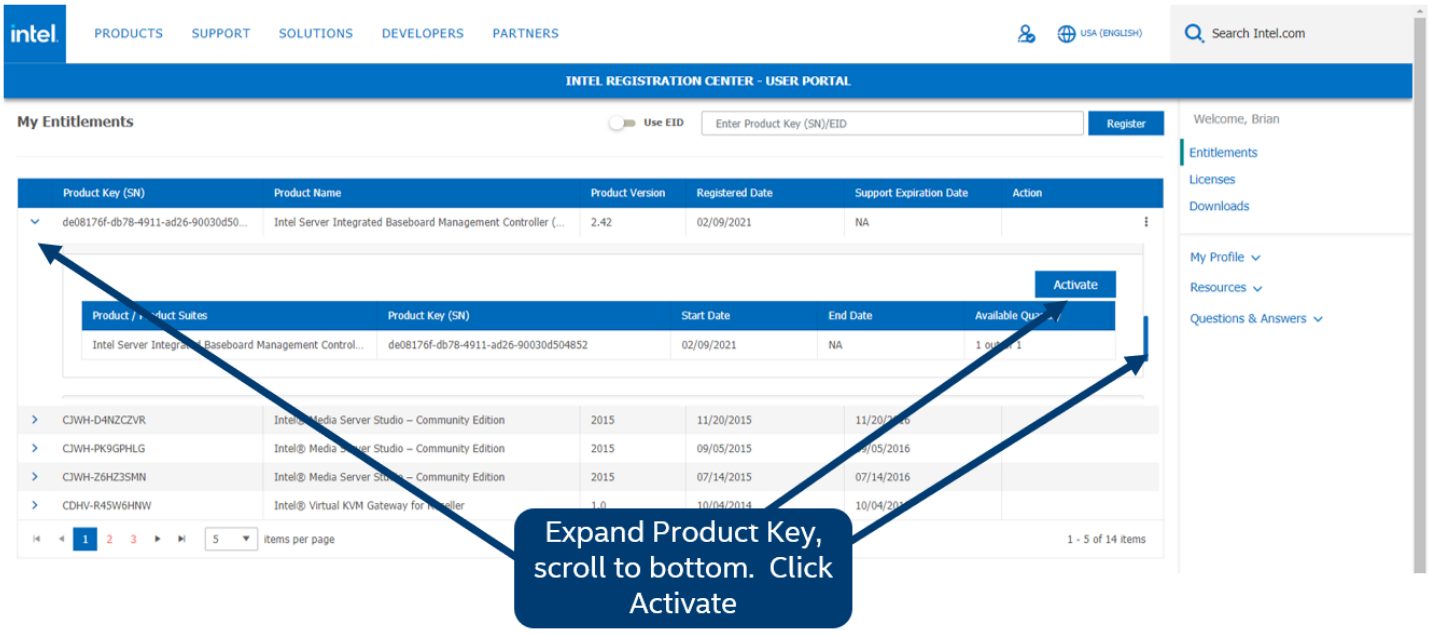


Figure 87. Activate Key

7. Download the license associated with the specified product key (see Figure 88)

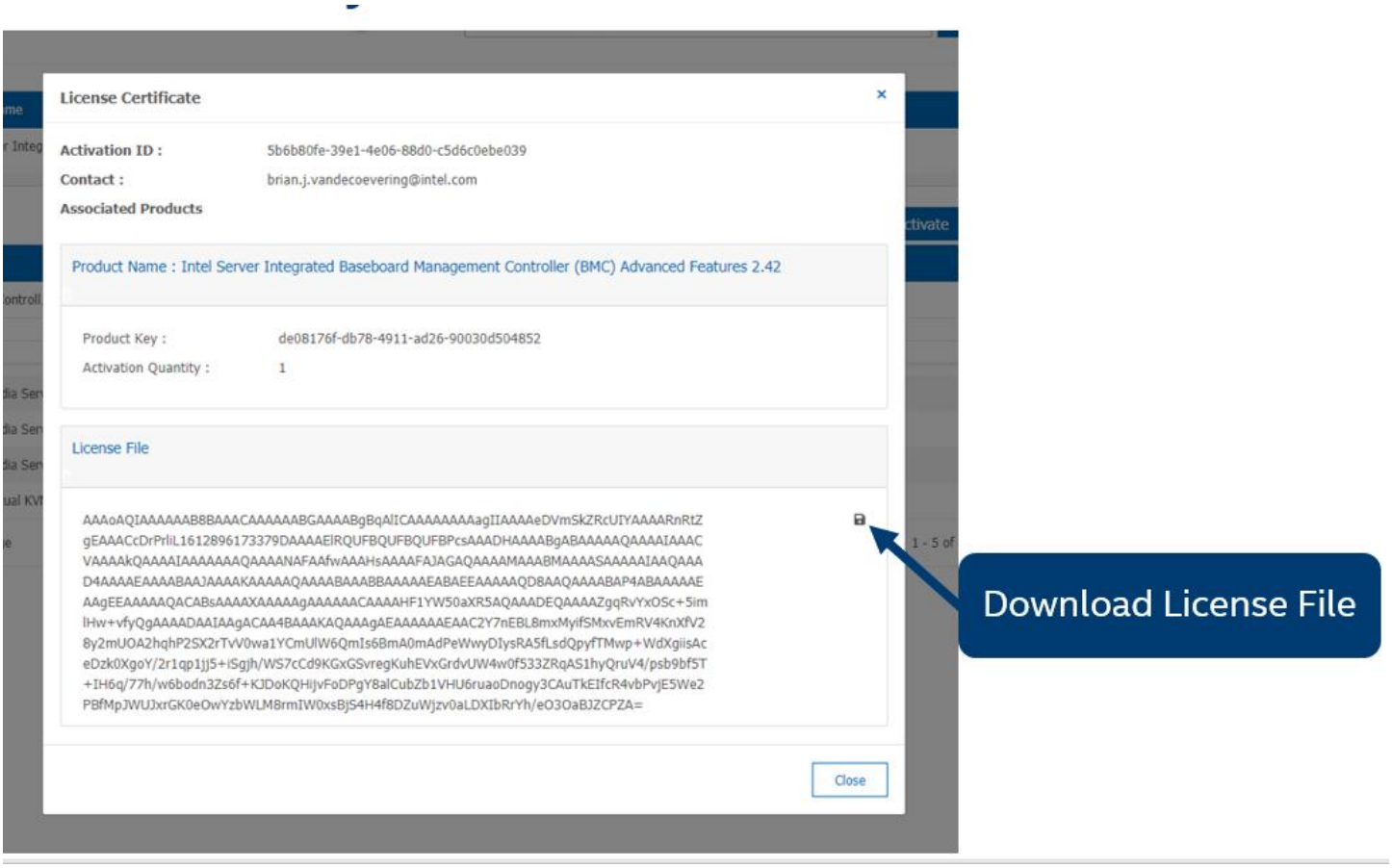


Figure 88. Download Key

8. Upload the license key file to the BMC.

Note: Only single license file per order is needed to activate multiple systems. If any key or email is lost, Intel can generate new product keys as needed.

I.2 Software License Key Installation

Three available options can be used to upload a software license onto a server:

- Integrated BMC Web Console
- Intel® Server Configuration Utility
- Redfish* Interface

I.2.1 Installation Using the Integrated BMC Web Console

The following procedure may be used to upload and confirm activation of a software license key. The example below illustrates the process of uploading the Advanced System Management (ASM) license using the Integrated BMC Web Console. Exactly the same process can be used to upload VROC software license key.

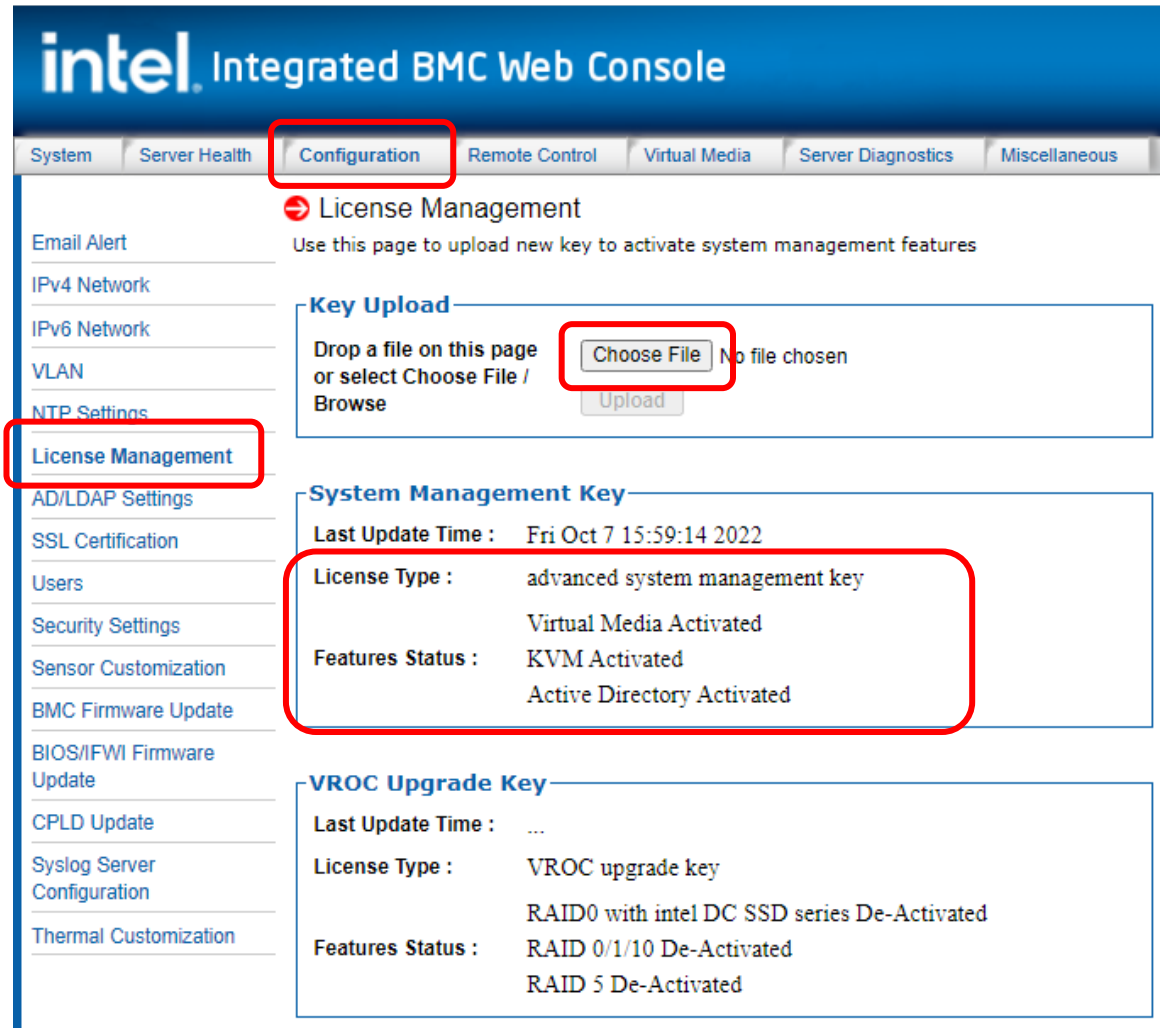


Figure 89. Integrated BMC Web Console Advanced System Management Key Page

1. Login to the Integrated BMC Web Console
2. Navigate to the **Configuration** > **License Management** page
3. Click the **Choose File** button to select the license key file
4. Select the **.v2c** license key file, then click the **Open** button
5. Click the **Upload** button to upload the ASM License Key to the BMC
6. The **System Management Key** section will show the license type and activated features
7. Navigate back to the **System** Tab. On the **System Information** page, view the **System Summary** information box to confirm the **Advanced Management Key** was successfully **Activated**.

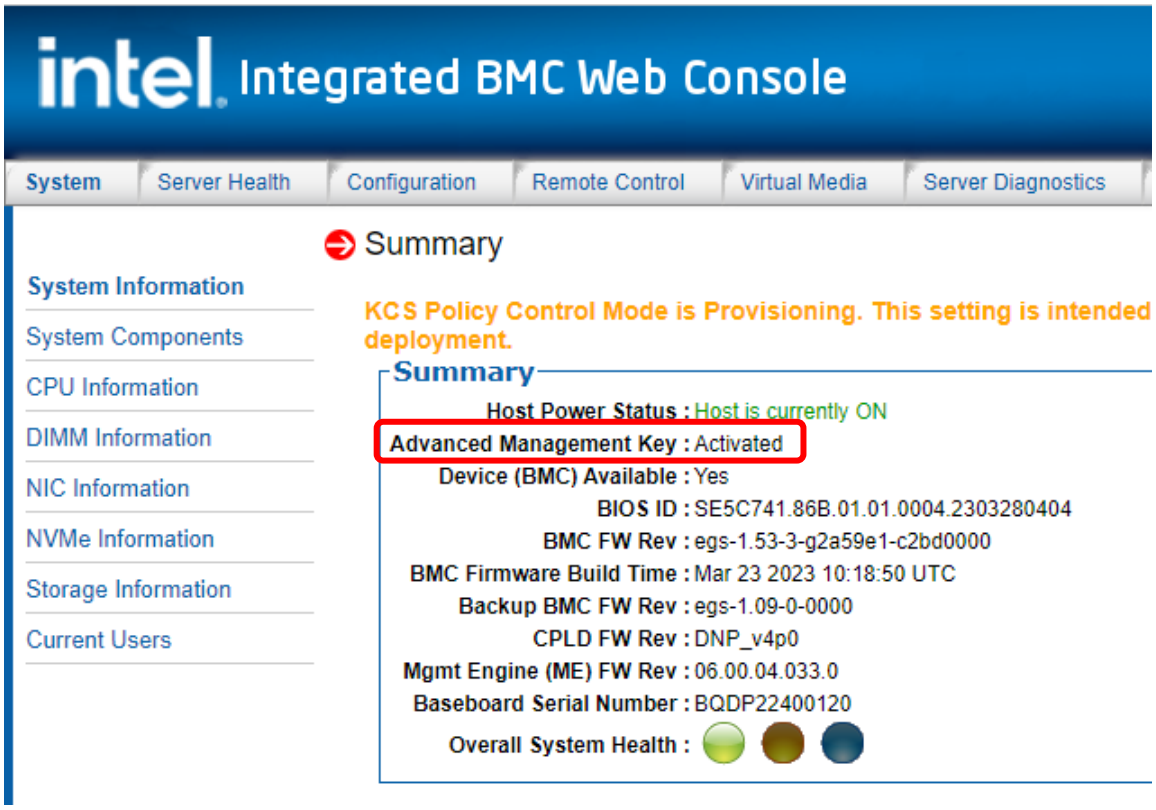


Figure 90. BMC Web Console System Information Page

I.2.2 Installation Using the Intel® Server Configuration Utility

The following procedure may be used to upload and confirm activation of the license keys using the syscfg command line utility.

To download the latest utility package, go to https://downloadcenter.intel.com/ and search for the "Intel Server Configuration Utility".

Prerequisites:

- Ensure the user has Administrator or Root privileges for the chosen operating system
- Ensure the KCS Policy Control Mode is set to "**Provisioning**"

Procedure:

1. Install the Intel® Server Configuration Utility on to the target server system. See the Intel® Server Configuration Utility User Guide for installation instructions.
2. Navigate to the sub-directory where the Server Configuration Utility was installed
3. From a command prompt run the following command

   syscfg /lic <key file name>

   where "file name" can be just the name of the license file if copied to the same directory as the syscfg command file, or the complete path of where the license key was copied can be entered along with the file name.

   Example below illustrates the process of uploading the VROC standard software license key. The same process can be used to upload the Advanced Server Management license key.

```
C:\SYSCFG 16.0.9>syscfg.exe /lic VROCSTANKEY.v2c

        Server Configuration Utility Version 16.0.9
        Copyright (c) 2023 Intel Corporation

Key Transfer...
Starting key upload:
Key Upload done

VROC license is uploaded successfully

C:\SYSCFG 16.0.9>
```

Figure 91. Upload VROC Standard License Key Using SYSCFG Utility

4. To confirm activation of the VROC license key, type the following command:
   syscfg /d lic

```
C:\SYSCFG 16.0.9>syscfg.exe /d lic

                        License Status
-------------------------------------------------------------------------------
Type                            |        Status         |       Time Stamp
-------------------------------------------------------------------------------
ASM key                         |       Activated       |       04/16/2023-11:37:04

VROC standard key               |       Activated       |       04/16/2023-11:41:27

VROC premium upgrade key        |       Not Activated   |
-------------------------------------------------------------------------------


C:\SYSCFG 16.0.9>
```

Figure 92. Confirm Activation of VROC Standard License Key Using SYSCFG Utility

I.2.3 Installation Using Redfish*

The following steps may be used to upload and confirm activation of a software license key using Redfish*.

Prerequisites:

- If not already present, install the “curl” and “grep” utilities onto the system from which the commands will be run.

Issue the following command to upload a software license key to the BMC

curl -k -u **username**:**password** https://**BMC_IP**/redfish/v1/UpdateService/SoftwareInventory/LicenseManagement/Actions/Oem/Intel.Oem.Upload -H "Content-Type: multipart/form-data" -F “updateFile=@**filepath**” -X POST

Notes:

- The command line above is a single command line, no return after “password ” and “ https…”
- username:password in the command line above should be replaced with the name of the user and their password

See the example below where:

- username = admin
- password = password
- BMC_IP = 192.168.0.102
- filepath = VROCPREMKEY.v2c

```
C:\SYSCFG 16.0.9>curl -k -u admin:password
https://192.168.0.102/redfish/v1/UpdateService/SoftwareInventory/LicenseManagement/Actions/Oem/Intel.Oem.Upload -H
"Content-Type: multipart/form-data"  -F "file=@VROCPREMKEY.v2c" -X POST
{
  "@odata.id": "/redfish/v1/TaskService/Tasks/2",
  "@odata.type": "#Task.v1_4_3.Task",
  "Id": "2",
  "TaskState": "Running",
  "TaskStatus": "OK"
}
C:\SYSCFG 16.0.9>
```

Figure 93. Redfish Command to Upload the VROC Premium Software License Key

Issue the following command to verify the activation status of the license keys.

curl -k -u **username**:**password** https://**BMC_IP**/redfish/v1/UpdateService/SoftwareInventory/LicenseManagement#Oem/LicenseInventory/Licenses -H "content-type: application/json" -X GET | grep -A1 LicenseStatus

```
C:\SYSCFG 16.0.9>curl -k -u admin:password
https://192.168.0.102/redfish/v1/UpdateService/SoftwareInventory/LicenseManagement#Oem/LicenseInventory/Licenses -H
"content-type: application/json" -X GET | grep -A1 LicenseStatus
  % Total    % Received % Xferd  Average Speed   Time    Time     Time  Current
                                 Dload  Upload   Total   Spent    Left  Speed
100  3306  100  3306    0     0   6480      0 --:--:-- --:--:-- --:--:--  6507
         "LicenseStatus": "ACTIVATED",
         "LicenseType": "advanced system management key",
--
         "LicenseStatus": "ACTIVATED",
         "LicenseType": "VROC premium upgrade key",
```

Figure 94. Redfish Command to Verify Activation of License Keys

Appendix J. Statement of Volatility

This appendix describes the volatile and non-volatile components on the Intel® Server System D50DNP. It is not the intention of this document to include any components not directly mounted to the server board in the Intel® D50DNP Module or riser cards used in the Intel® D50DNP Modules or supported Intel server chassis. These may include processors, memory, storage devices, or add-in cards.

The tables in this appendix provide the following data for each identified component.

Component Type

Three types of memory components are used on the compute module server board assembly. These include:

- **Non-volatile:** Non-volatile memory is persistent and is not cleared when power is removed from the system. Non-volatile memory must be erased to clear data. The exact method of clearing these areas varies by the specific component. Some areas are required for normal operation of the server and clearing these areas may render the server board inoperable.
- **Volatile:** Volatile memory is cleared automatically when power is removed from the system.
- **Battery-powered RAM:** Battery-powered RAM is similar to volatile memory; however, is powered by a battery on the server board. Data in battery-powered RAM is persistent until the battery is removed from the server board.

Size

The size of each component includes sizes in bits, Kbits, bytes, kilobytes (KB), or megabytes (MB).

Board Location

The physical location of each component is specified in the Board Location column. The board location information corresponds to information on the silkscreen in the compute module server board.

User Data

The flash components on the Intel® Server D50DNP Family do not store user data from the operating system. No operating system level data is retained in any listed components after AC power is removed. The persistence of information written to each component is determined by its type as described in the table.

Each component stores data specific to its function. Some components may contain passwords that provide access to that device's configuration or functionality. These passwords are specific to the device and are unique and unrelated to operating system passwords. The specific components that may contain password data are:

- **BIOS:** The BIOS provides the capability to prevent unauthorized users from configuring BIOS settings when a BIOS password is set. This password is stored in BIOS flash and is only used to set BIOS configuration access restrictions.
- **BMC:** The Intel® Server D50DNP Family supports an Intelligent Platform Management Interface (IPMI) 2.0 compliant baseboard management controller (BMC). The BMC provides health monitoring, alerting, and remote power control capabilities for the Intel® D50DNP Module. The BMC does not have access to operating system level data.

The BMC supports the capability for remote software to connect over the network to perform health monitoring and power control. This access can be configured to require authentication by a password. If configured, the BMC maintains user passwords to control this access. These passwords are stored in the BMC flash.

A list of the components that can be used to store data is included in the following table.

Table 48. Intel® Server Board D50DNP1SB Components

Component Type	Size	Board Location	Stores User Data	Name
Non-Volatile	64 MB	U11	No (BIOS)	BIOS flash
Non-Volatile	256 MB	U19	No (BMC FW)	BMC flash
Non-Volatile	4 MB	U5_NIC	No	LAN flash
Non-Volatile	6962 B	J16	No (TPM)	TPM
Non-Volatile	CFM 9670 KB	U1_FPGA	No	FPGA
Volatile	1 GB	U1_BMC	No	BMC SDRAM

Other boards inside Intel® D50DNP Modules may include components used to store data. The following tables provide a list of components associated with specific system boards supported by this product family.

Table 49. Intel® D50DNP Module Components

Component Type	Size	Board Location	Stores User Data	Name
Non-Volatile	256 B	U1	No	1U MCIO* riser card FRU
Non-Volatile	256 B	U1	No	1U standard riser card FRU
Non-Volatile	256 B	U1	No	2U riser card FRU
Non-Volatile	256 KB	U12	No	2U riser card re-timer EEPROM
Non-Volatile	256 B	U1	No	PCIe* accelerator riser card 1 FRU
Non-Volatile	256 KB	U11	No	PCIe accelerator riser card 1 re-timer EEPROM1
Non-Volatile	256 KB	U18	No	PCIe accelerator riser card 1 re-timer EEPROM2
Non-Volatile	256 B	U1	No	PCIe accelerator riser card 2 FRU
Non-Volatile	256 KB	U11	No	PCIe accelerator riser card 2 re-timer EEPROM1
Non-Volatile	256 KB	U18	No	PCIe accelerator riser card 2 re-timer EEPROM2
Non-Volatile	128 KB + 16384 B (Words)	U901	No	Intel® Data Center GPU Max Series Accelerator power converter bottom board PIC MCU

Some boards in the Intel® Server Chassis D50DNP contain components used to store data. A list of components for the system boards in the chassis is included in the following table.

Table 50. Intel® Server Chassis D50DNP Components

Component Type	Size	Board Location	Stores User Data	Name
Non-Volatile	256 B	U25	No	Power distribution board FRU
Non-Volatile	128 K + 3 KB (boot)	U19	No	Power distribution board PIC MCU
Non-Volatile	4 KB	U18	No	Ethernet management port SW EEPROM
Non-Volatile	256 B	U25	No	Ethernet management port FRU

Appendix K. Product Regulatory Compliance

This product has been evaluated and certified as information technology equipment (ITE) that may be installed in offices, schools, computer rooms, and similar commercial type locations. The suitability of this product for other product certification categories and/or environments (such as: medical, industrial, telecommunications, NEBS, residential, alarm systems, test equipment, and so on), other than an ITE application, requires further evaluation and may require additional regulatory approvals.

Intel has verified that all L3, L6, and L9 server products[1] **as configured and sold by Intel** to its customers comply with the requirements for all regulatory certifications defined in the following table. It is the Intel customer's responsibility to ensure their final server system configurations are tested and certified to meet the regulatory requirements for the countries to which they plan to ship and/or deploy server systems into

Table 51. Regulatory Certification Availability

Intel Product Name and Model	Intel® Server Board D50DNP1SB	Intel® Server Chassis FC2HAC27W0 FC2FAC27W0	Intel® Server Chassis FC2HLC30W0 FC2FLC30W0
Product integration level	**L3 Board**	**L6/L9 System [1]**	
Product family identified in certification	**D50DNP**	**FC2000**	
Regulatory Certification			
RCM DoC Australia & New Zealand	Y	Y	Y
CB Certification & Report (International - report to include all CB country national deviations)	Y	Y	Y
China CCC Certification	Out of CCC Scope (PSU > 1300 W)		
CU Certification (Russia/Belarus/Kazakhstan)	Not done	Not done	Not done
Europe CE Declaration of Conformity	Y	Y	Y
United Kingdom UKCA DoC	Y	Y	Y
FCC Part 15 Emissions Verification (USA & Canada)	Y	Y	Y
Germany GS Certification	Not in scope (component)	Y	Y
India BIS Certification	Not in scope (component)	Y	Y
International Compliance – CISPR32 & CISPR35	Y	Y	Y
Japan VCCI Certification	Not in scope (component)	Y	Y
Korea KC Certification	Y	Y	Y
Mexico Certification	Not in scope(component)	Y	Y
NRTL Certification (USA & Canada)	Y	Y	Y
South Africa Certification	Not in scope (distributor responsibility)	Not in scope (distributor responsibility)	Not in scope (distributor responsibility)
Taiwan BSMI Certification	Y	Y	Y
Ukraine Certification	Not done	Not done	Not done

[1]An L9 system configuration is a power-on ready server system with NO operating system installed.
An L6 system configuration requires additional components to be installed to make it power-on ready.
L3 are component building block options that require integration into a chassis to create a functional server system

EU Directive 2019/424 (Lot 9)

Beginning on March 1, 2020, an additional component of the European Union (EU) regulatory CE marking scheme, identified as EU Directive 2019/424 (Lot 9), went into effect. After this date, all new server systems shipped into or deployed within the EU must meet the full CE marking requirements including those defined by the additional EU Lot 9 regulations.

Intel has verified that all L3, L6, and L9 server products **as configured and sold by Intel** to its customers comply with the full CE regulatory requirements for the given product type, including those defined by EU Lot 9. It is the Intel customer's responsibility to ensure their final server system configurations are SPEC® SERT™ tested and meet the new CE regulatory requirements.

Visit the following website for additional EU Directive 2019/424 (Lot9) information:

https://eur-lex.europa.eu/legal-content/EN/TXT/?uri=CELEX:32019R0424

In compliance with the EU Directive 2019/424 (Lot 9) materials efficiency requirements, Intel makes available all necessary product collaterals as identified below:

- **System Disassembly Instructions**
  - *Intel® Server D50DNP Family System Integration and Service Guide*
  - See Table 1 for reference
- **Product Specifications**
  - *Intel® Server D50DNP Family Technical Product Specification (TPS)*
  - This document.
- **System BIOS/Firmware and Security Updates – Intel® Server D50DNP family**
  - System Update Package (SUP)
  - See Table 1 for reference
- **Intel® Solid State Drive (SSD) Secure Data Deletion and Firmware Updates**
  - **Note**: for system configurations that may be configured with an Intel SSD
  - The Intel® Memory and Storage Tool (Intel® MAS) https://www.intel.com/content/www/us/en/support/products/202249/memory-and-storage/ssd-software/intel-memory-and-storage-tool.html https://www.intel.com/content/www/us/en/download/19543/intel-memory-and-storage-tool-gui.html

EU Lot9 Support Summary for Intel® Server FC2000 Family (2U2N & 2N4N)

***DISCLAIMER** – The information contained within the following tables is for reference purposes only and is intended to provide Intel customers with a template to report product information necessary for (EU) 2019/424 (Lot 9) server conformity assessment. The information provided herein does not represent any final shipping server system test results, and customer's actual test results for shipping server configurations may differ from the information provided. Use of this information is at the sole risk of the user, and Intel assumes no responsibility for customers server system level regulation compliance with EU 2019/424 (Lot 9).*

Table 52. EU Lot9 Support Summary for Intel® Server FC2000 Family

Product Info	
Product Type	Server
Manufacturer Name	Intel Corporation
Registered trade name and address	Intel 2200 Mission College Blvd, Santa Clara, CA 95054-1594, USA
Product model number and model numbers for low end performance and high-end performance configure if applicable	FC2000
Year Of Manufacture	2022
PSU efficiency at 10%, 20%, 50% and 100% of rated output power	2700W Air-Cooled Power Supply FCXX27CRPSAC Model / 10% / 20% / 50% / 100% FCXX27CRPSAC / 94.21% / 95.37% / 96.32% / 94.14%
PSU factor at 50% of rated load level	
PSU Rated Power Output (Server Only)	3000W, 2700W
Idle state power (Server only) (Watts)	Refer to the following table
List of all components for additional idle power allowances (server only)	Refer to the following table
Maximum power (Server only)	Refer to the following table
Declared operating condition class	ASHRAE Class A2-Continuous Operation 10 ℃ to 35 ℃ with the maximum rate of change not to exceed 10 ℃ per hour
Idle State Power (watts) at the higher boundary temp (Server Only)	Refer to the following table
the active state efficiency and the performance in active state of the server (server only)	Refer to the following table
Information on the secure data deletion functionality	Refer to the following table
for blade server, a list of recommended combinations with compatible chassis (Server only)	Not Applicable
If Product Model Is Part of A Server Product Family, a list of all model configurations that are represented by the model shall be supplied (Server only)	Not Applicable

Chemical Declaration

Neodymium	Not Applicable. (No HDD offered by Intel)
Cobalt	Not Applicable. (No BBUs. Coin battery is out of scope)

Appendix L. Glossary

Term	Definition
ACPI	Advanced Configuration and Power Interface
ADR	Asynchronous DRAM refresh
Intel® AES-NI	Intel® Advanced Encryption Standard New Instructions
AI	Artificial intelligence
ARS	Address range scrub
ASHRAE	American Society of Heating, Refrigerating, and Air Conditioning Engineers
Intel® AVX-512	Intel® Advanced Vector Extensions 512
ATAPI	Advanced Technology Attachment Packet Interface
BBS	BIOS boot selection
BMC	Baseboard management controller
BIOS	Basic input/output system
CBB	Carrier baseboard
CDU	Coolant distribution unit
CFM	Cubic feet per minute
CLST	Closed loop system throttling
CMOS	Complementary metal-oxide-semiconductor
DDR5	Double data rate 5
DIMM	Dual in-line memory module
DMI	Direct media interface
DPC	DIMMs per channel
DR	Dual rank
ECC	Error correction code
EFI	Extensible Firmware Interface
EMP	Ethernet management port
EPS	External product specification
fADR	Fast asynchronous DRAM refresh
FRB	Fault resilient boot
FRU	Field-replaceable unit
GPIO	General purpose input/output
GPU	Graphics processing unit
GUI	Graphical user interface
HPC	High-performance computing
Intel® HT Technology	Intel® Hyper-Threading Technology
IDE	Integrated Drive Electronics
IMC	Integrated memory controller
IIO	Integrated input/output
iPC	Intel Product Code
IPMB	Intelligent Platform Management Bus
IPMI	Intelligent Platform Management Interface
ISTA	International Safe Transit Association
ITE	Information technology equipment
KVM	Keyboard, video, and mouse
KVM-r	Keyboard/video/mouse redirection

Term	Definition
JRE*	Java Runtime Environment*
LFM	Linear feet per minute (airflow measurement)
LLC	Last level cache
LSB	Least significant bit
MCIO*	Mini Cool Edge I/O
Intel® ME	Intel® Management Engine
Memory module	DDR5 DIMM are commonly referred to as “memory module”
MKTME	Intel® Total Memory Encryption – Multi-Key (Intel® TME-MK)
MLE	Measured launch environment
MRC	Memory reference code
MSB	Most significant bit
NAT	Network address translation
NFS	Network file system
NIC	Network interface controller
NIST	National Institute of Standards and Technology
NMI	Non-maskable Interrupt
NTB	Non-transparent bridge
OAM	Open Compute Project Accelerator Module
OCP*	Open Compute Project
OCuLink	Optical copper link
OEM	Original equipment manufacturer
OR	Octuple rank, eight ranks
OTP	Over-temperature protection
OVP	Over-voltage protection
PCH	Platform controller hub
PCI	Peripheral Component Interconnect
PCIe*	Peripheral Component Interconnect Express
PDB	Power distribution board
PECI	Platform Environment Control Interface
Intel® PFR	Intel® Platform Firmware Resilience
PHM	Processor heat sink module
PMBus*	Power Management Bus
PMem	Persistent memory
PMIC	Power management integrated circuit
POST	Power-on self-test
PSU	Power supply unit
PWM	Pulse width modulation
QR	Quadruple rank, four ranks
RAID	Redundant array of independent disks
RAS	Reliability, availability, and serviceability
RCiEP	Root complex integrated endpoint
RDIMM	Registered DIMM
RMCP	Remote Management Control Protocol
SATA	Serial Advanced Technology Attachment
SEL	System event log
SDR	Sensor data record

Term	Definition
SmaRT	Smart Ride Through
Intel® SGX	Intel® Software Guard Extensions
Intel® SGX DCAP	Intel® Software Guard Extensions Data Center Attestation Primitives
SMBus*	System Management Bus
SMM	Server management mode
SMS	System management software
SMTP	Simple Mail Transfer Protocol
SNMP	Simple Network Management Protocol
SoC	System on chip
SOL	Serial-over-LAN
SPD	Serial presence detection
SR	Single Rank
SSD	Solid state device
SSL	Secure Sockets Layer
TCG	Trusted Computing Group
TDP	Thermal design power
TIM	Thermal interface material
Intel® TME	Intel® Total Memory Encryption
Intel® TME-MK	Intel® Total Memory Encryption – Multi-Key
TPM	Trusted platform module
Intel® TXT	Intel® Trusted Execution Technology
UDF	Universal Disk Format
UEFI	Unified Extensible Firmware Interface
Intel® UPI	Intel® Ultra Path Interconnect
VLSI	Very large scale integration
VNNI	Vector Neural Network Instructions
Intel® VROC	Intel® Virtual RAID on CPU
VSB	Voltage standby
Intel® VT-d	Intel® Virtualization Technology for Directed I/O
Intel® VT-x	Intel® Virtualization Technology for IA-32, Intel® 64 and Intel® Architecture