Data Sheet

VPF2

MPC8641D & Dual Xilinx® Virtex®-5 FPGA VXS Processor Card

Applications

- Electronic Warfare
- Signal Intelligence (SigInt)
- Surveillance

Features

- FPGA and PowerPC™ based processing
- Freescale Power Architecture™ MPC8641D
- Dual Xilinx® Virtex®-5 LX110T/SX95T FPGAs
- 6U VXS/VITA 41 form factor
- XMC/PMC Site
- Air- or conduction-cooled rugged versions

Benefits

- Balance of performance with ease of programming
- Powerful and sophisticated dual core processing power
- FPGA options for optimal DSP or logic-centric designs with high-bandwidth communications
- Industry standard form factors
- For use in deployed or commercial environments

Overview

The VPF2 is a high-performance heterogeneous processing engine coupling a dual PowerPC™ AltiVec™ CPU with two powerful Xilinx Virtex-5 FPGAs. The combination of devices provides leading edge performance with flexible high-bandwidth I/O. This VXS board is available in both air-cooled and conduction cooled versions, with VxWorks® or Linux® board support packages. The VPF2 is supported by the FusionXF HDK which provides HDL blocks to facilitate implementing customer applications in the FPGA.

At its most simple, the VPF2 is a quad processor DSP engine. Two of these processor elements are combined into a single, highly integrated, Freescale MPC8641D CPU. The other two processors are the Xilinx Virtex-5 FPGA devices. It is this hybrid CPU/FPGA combination that makes the VPF2 so powerful through leveraging the advantages of each technology. The FPGAs also provide the VXS/VITA 41 multi-gigabit serial communications. Both FPGAs are fully user programmable and Curtiss-Wright provides tools, examples and utilities to simplify code development.

Input/output is provided through a number of channels including copper or fiber Ethernet ports, XMC/PMC for a wide choice of I/O options, RS232 ports or VXS serial I/O for inter-board communications along with a VME64 bus. Direct FPGA I/O is also provided through a parallel port, via the backplane, for high bandwidth I/O.

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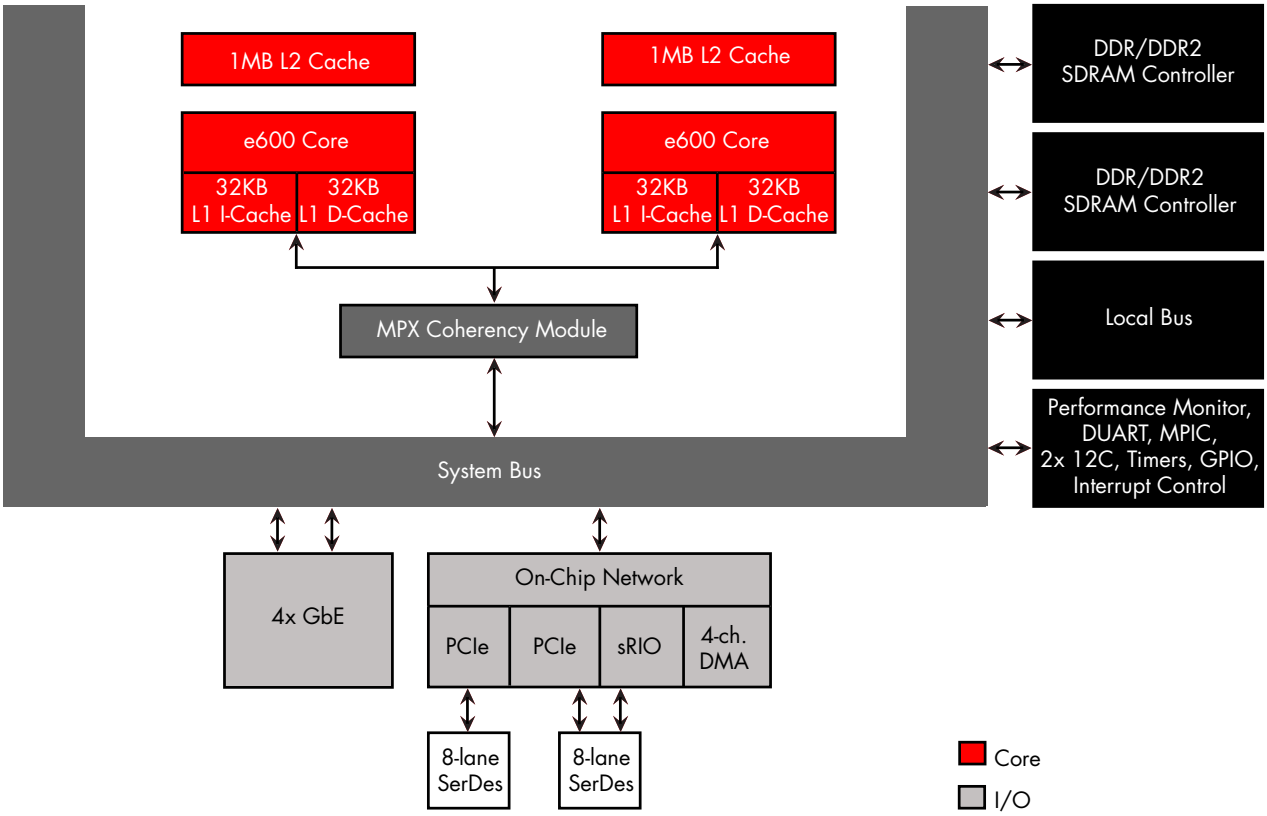
PowerPC Processor

Dual CPU

The Freescale MPC8641D forms a fully integrated processor node with dual PowerPC CPUs, memory controllers, DUART, Ethernet controllers and PCI Express® (PCIe) channels. The e600 Power Architecture™ CPU cores include floating-point units for high performance DSP processing.

Figure 1: Freescale MPC8641D Architecture



Memory

Two 1GB DDR2 SDRAM memory banks are provided including ECC. Each e600 core has its own 1MB L2 cache.

Ethernet

The VPF2, by default, incorporates two gigabit Ethernet channels controlled by the MPC8641D. These are available through the front panel. One is optical, the second is available in optical or copper. One of these channels is shared via the VME P2 connector. An auto-detection mechanism determines which route is active. Additional Ethernet options are available through VXS P0 - contact the factory for details.

Serial I/O

The MPC8641D includes two UART controllers supporting RS232. Both channels are routed to the VME P2 connector. A VME P2 I/O adaptor module can be provided to simplify connections to these signals.

PCI Express Infrastructure

The primary high bandwidth communications to the PowerPC processor on the MPC8641D is through two x8 PCIe ports, each with up to 2GB/s of full-duplex bandwidth available. These ports are used to connect to the FPGA devices and the board's I/O infrastructure.

FLASH

128MB of FLASH memory is fitted to store the VPF2's bootloader and applications which are addressable by filename. The VPF2 has a switch to protect the bootloader image and/or data from being accidentally overwritten.

PMC/XMC

One mezzanine site is provided and supports both the PMC and XMC formats. The PMC site supports both 32/64-bit PCI (up to 66MHz) and 133MHz PCI-X. This bus is bridged to both the VME64 bus interface and the PCIe bridge linking into both the PowerPC and FPGA processing structure. Neither the PowerPC processor nor the FPGAs on a VPF2 support PCI, so the PCIe/PCI-X bridge is the data path for the PMC. This is controlled by the PowerPC CPU. The XMC site supports PCIe and links via a x8 link into the PCIe switch; the hub of the VPF2. An XMC P16 connector is not supported.

Real-Time Clock and Elapsed Time Recorder

A real-time clock is fitted. Although interfaced to the MPC8641D via an I2C bus, interrupts and clock outputs are also routed to both of the FPGAs. A Goldcap capacitor (build option) can provide standby power for the FPGA to maintain the encryption key.

Integrated within the VPF2 is an elapsed time recorder that has two functions; power and event counters. The power counter is used to record the total time power has been applied to the board and is useful for logging service hours. The event counter counts inputs on the VPF2's 'event' pin.

Temperature Sensors

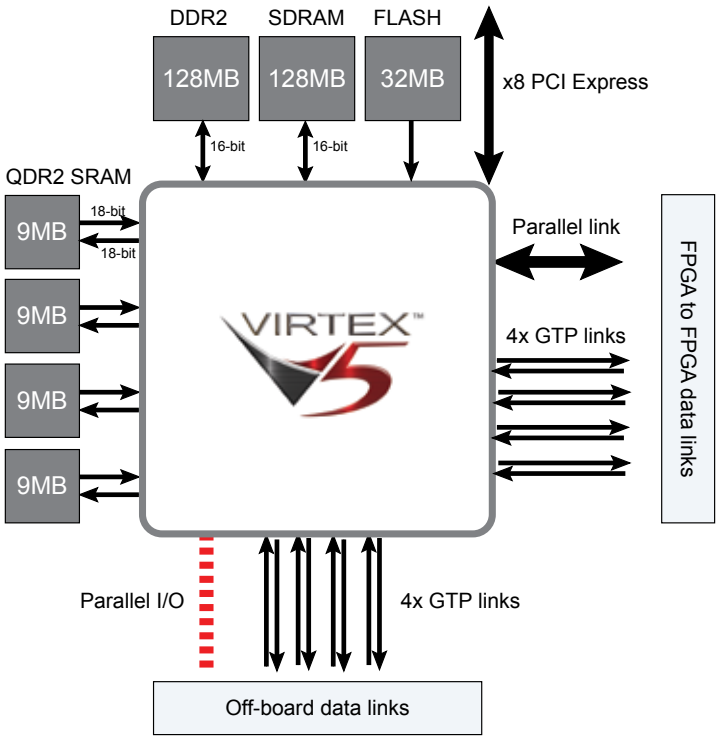
The VPF2 includes six temperature sensors with provision for raising alarms. These are located on or at both FPGA junctions and four other places around the PCB for even coverage.

Virtex-5 FPGA Nodes

Dual Xilinx Virtex-5 FPGAs

The VPF2 can be provided with Xilinx Virtex-5 LX110T or SX95T FPGAs. The LX110T offer the maximum number of logic cells while the SX95T is optimized for DSP applications. By default speed grade 2 devices are used. Virtex-5 FPGAs provide higher performance at lower power than previous generation FPGAs. The Virtex-5 FPGAs fulfill two roles; DSP processing and VXS I/O sub-system.

Figure 2: FPGA Processor Node



The FPGAs are directly linked using four full-duplex GTPs and by 36 single-ended signals.

Table 1: Virtex-5 LX110T and SX95T Resource Comparison

Resource	LX110T	SX95T
Slices	17,280	14,720
Logic Cells	110,592	94,208
CLB Flip-flops	69,120	58,880
Distributed RAM (kbits)	1,120	1,520
Block RAM/FIFO (36kbits each)	148	244
Total Block RAM (kbits)	5,328	8,784
DSP48E Slices	64	640
GTP Channels RocketIO	16	16
PCIe Subsystem blocks	1	1
10/100/1000 EMACs	4	4

Memory

Each FPGA has multiple banks of both DDR2 SDRAM and QDR2 SRAM to ensure that the full performances advantages can be realized. Two 128MB banks of SDRAM are useful as large data buffers, while the four 9MB SRAM banks are useful for holding complete frame buffer for video processing, large FFTs or general purpose processing.

The two DDR2 SDRAM banks can be clocked at speeds of up to 250MHz. This results in a bandwidth of up to 1GB/s per bank. The four QDR2 SRAM banks can be clocked at speeds of up to 250MHz resulting in 1GB/s in each direction per bank.

VXS Serial I/O Communications

The primary method for high-bandwidth off-board input/output is via the RocketIO™ GTP transceivers linked to the VXS P0 connector. Each FPGA provides four full-duplex GTP channels. These channels are typically configured as four 1x links, but can also be used as a single 4x link. All VXS links are AC coupled and they are able to run at up to 3.125Gbps per 1x link. See table 3 for on-board clock sources.

Table 2: VXS P0 Payload Connection

pin	row A	row B	row C	row D	row E	row F	row G
1	RX0P_A	RX0N_A	GND	TX0P_A	TX0N_A	GND	SCL_A
2	GND	RX1P_A	RX1N_A	GND	TX1P_A	TX1N_A	GND
3	RX2P_A	RX2N_A	GND	TX2P_A	TX2N_A	GND	SDA_A
4	GND	RX3P_A	RX3N_A	GND	TX3P_A	TX3N_A	GND
5	SIN_P[0]	SIN_N[0]	GND	SOUT_P[0]	SOUT_N[0]	GND	NC
6	GND	NC	NC	GND	NC	NC	GND
7	NC	NC	GND	NC	NC	GND	NC
8	GND	NC	NC	GND	NC	NC	GND
9	NC	NC	GND	NC	NC	GND	NC
10	GND	NC	NC	GND	NC	NC	GND
11	SIN_P[1]	SIN_N[1]	GND	SOUT_P[1]	SOUT_N[1]	GND	PWR_EN
12	GND	RX0P_B	RX0N_B	GND	TX0P_B	TX0N_B	GND
13	RX1P_B	RX1N_B	GND	TX1P_B	TX1N_B	GND	SCL_B
14	GND	RX2P_B	RX2N_B	GND	TX2P_B	TX2N_B	GND
15	RX3P_B	RX3N_B	GND	TX3P_B	TX3N_B	GND	SDA_B

GTP Reference Clocks

The VPF2 has three reference clocks that can be used to determine the GTP clock speeds. The appropriate clock source for the protocol being used is determined by the FPGA configuration file.

Table 3: GTP Speed/Clock Sources

Speed	Protocol	Clock Source
3.125Gbps	Serial RapidIO type 3, Aurora	156.25MHz
2.5Gbps	Serial RapidIO type 2, Aurora, Serial FPDP, PCIe	125MHz
2.125Gbps	2x Fibre Channel, Aurora, Serial FPDP	106.25MHz
1.25Gbps	1x Gigabit Ethernet, Aurora	125MHz
1.0625Gbps	1x FibreChannel, Aurora, Serial FPDP	106.25MHz

FPGA Configuration

The FPGA can be configured in three ways: from FLASH during boot, under software control from the MPC8641D (without updating FLASH) or through the JTAG/ChipScope™. There is a FLASH device associated with each FPGA. The FLASH is programmed by one of the PowerPC CPUs through an on-board controller. Consequently, the FLASH is used only for configuration and cannot be used by the FPGAs for non-volatile storage.

Software and HDL

Overview

The VPF2 is a highly versatile processing engine with applicability across a range of operational requirements. To enable developers to take advantage of the board's functionality without constricting them to a rigid programming model, the software support is provided through a flexible, multi-faceted approach. The fixed functionality of the board is supported by a BSP which provides the driver suite enabling the PowerPC processors to boot and run either the VxWorks or Linux operating system. The reconfigurable (FPGA based) functionality is supported by the FusionXF package which provides the PowerPC processors with a 'Plug and Play' like discovery mechanism that examines the features and services offered by the FPGAs, allowing them to be mapped by the processors and allocated the appropriate drivers.

Board Support Package

The VPF2 is supported by either a WindRiver VxWorks 6.5 BSP or a Linux 2.6 (DENX Distribution) BSP. The MPC8641D is supported in two modes: Dual Core mode (the default setting) or Single Core mode. When using Dual Cores, Linux is supported in SMP mode only, whereas VxWorks runs a separate instance of the operating system on each core (ASMP).

The BSP also provides command line utilities for accessing the FPGA FLASH and configuring the FPGAs:

pxflash - allows images in the FLASH to be listed, created, deleted and viewed by address and filename.

pxcfg - facilitates configuration of the FPGA from a host file or a FLASH object.

Figure 3: VPF2 Software and HDL support Structure

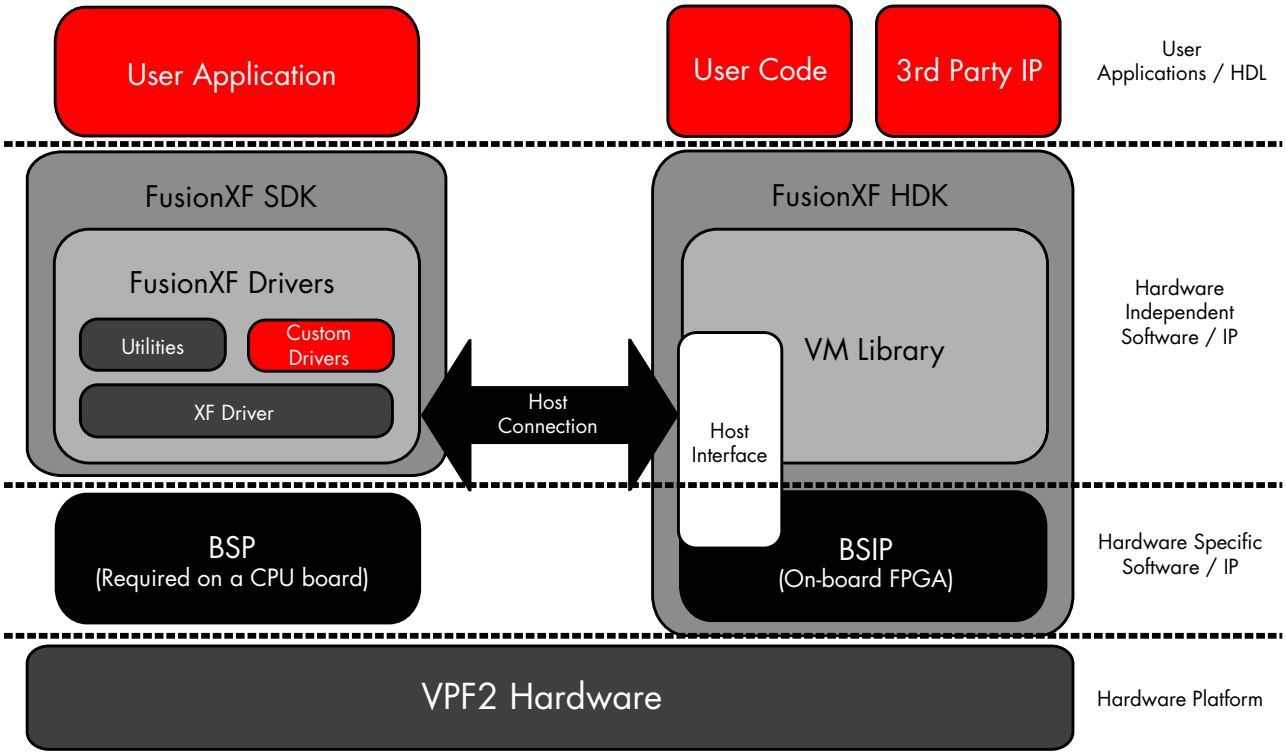
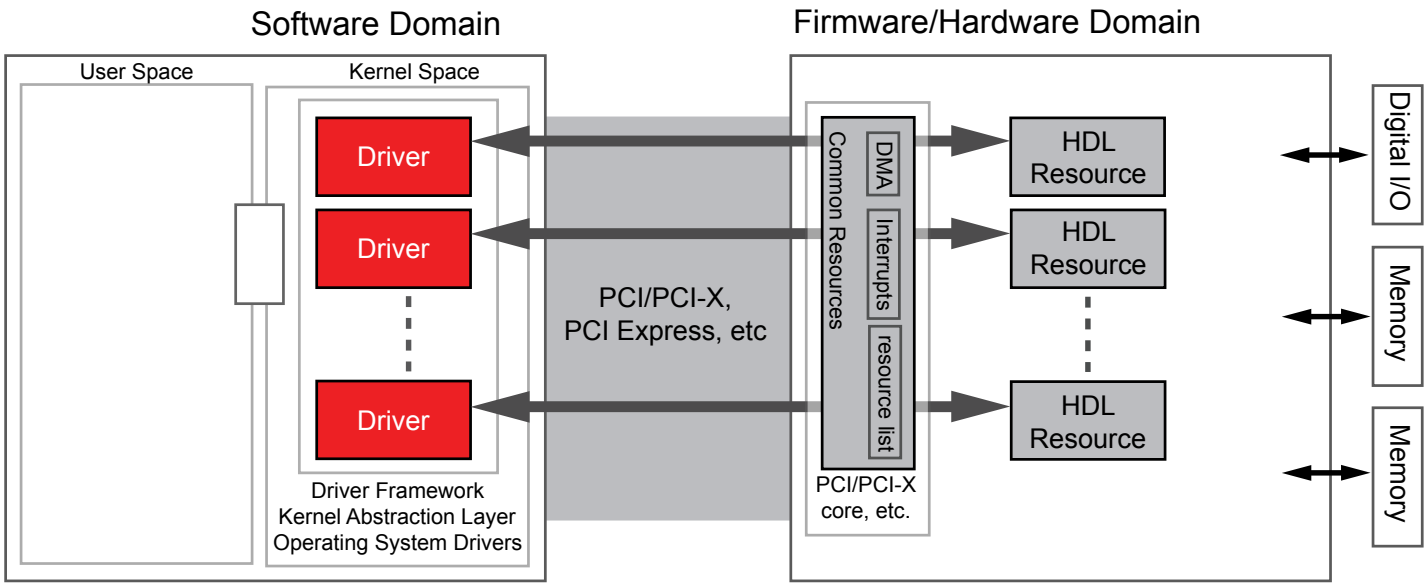


Figure 4: The FusionXF discovery process matches Drivers to HDL resources



FusionXF

As a large proportion of the functionality of the VPF2 is dependant on the behavior of the logic configured into the user-programmable FPGAs, it is imperative that application software is able to determine what FPGA resources are available and act accordingly. FusionXF is a collection of software and HDL libraries which standardize this process while providing a platform onto which custom designs may be built. The FusionXF package is optimized towards aiding developers control system-wide data flow allowing them to concentrate their development time on implementing project-specific functionality, such as optimized compute algorithms. FusionXF does not force fixed functionality onto the FPGA but provides building blocks that can be amalgamated into fully functional FPGA designs. The blocks are provided as HDL libraries. FusionXF provides software discovery functions to determine which HDL blocks have been included and matches these blocks with corresponding drivers. The functionality of these blocks is then available to the user application, running on a CPU, through a standard API which is common to all FusionXF enabled products.

Capabilities

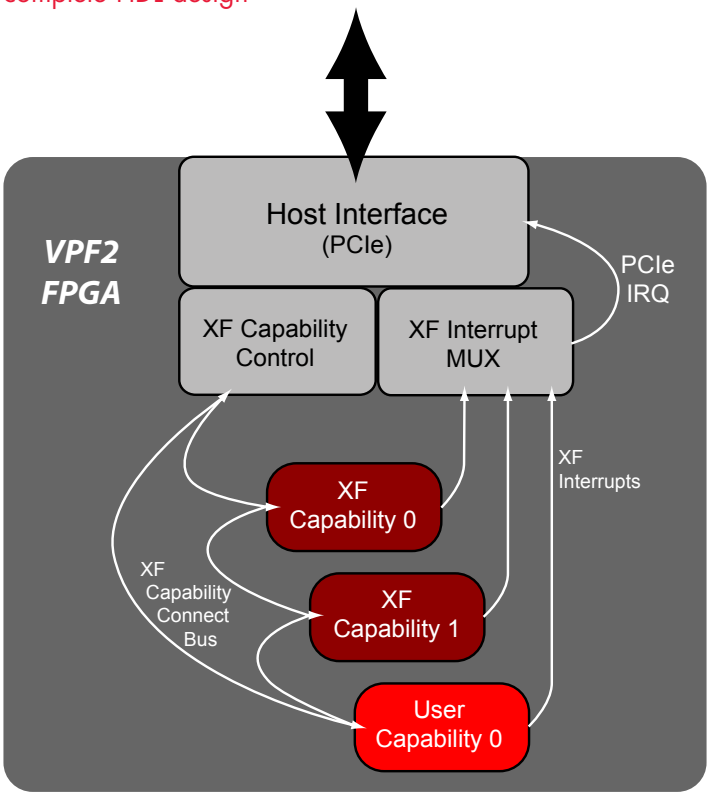
Functional HDL elements such as I/O interfaces, register banks, DMA controllers, etc. are referred to as capabilities in FusionXF . The discovery process creates a capabilities list. This list is used to optimize the collection of drivers used in the run-time environment: only the drivers that map to the corresponding capability are loaded rather than the entire list of existing drivers.

The HDL Capability structure is connected in a linked-list fashion . This daisy chaining mechanism allows the CPU to access the control and status registers for each individual capability via the host interface. In software (and address space), the capability list is structured as sequential addresses. The capability registers point at addresses for each of the HDL control register blocks.

As well as providing a broad Software and HDL library of standard features, FusionXF also provides a platform for adding custom-designed user capabilities (e.g. a DSP compute block) into the capabilities list.

Interrupts are supported for each individual capability which connect to a specialized capability called IMUX. This capability multiplexes the interrupts to the host interface.

Figure 5: FusionXF Capabilities interconnect forming a complete HDL design



One of the more advanced features of FusionXF is Remote Register Access (RRA) which provides the VPF2 CPUs with the ability to access non-local capability trees remotely across a communication fabric. This feature allows remote FPGAs to be controlled and accessed as though they were local to the VPF2 board.

SDK

The Software Development Kit extends the BSP to include an API for accessing FusionXF capabilities from a user application running on the CPUs. The SDK includes a framework for developing custom drivers that support custom HDL IP implemented using FusionXF.

The SDK also provides a number of examples demonstrating the use of API functionality (including RRA) and a set of reference utilities that facilitate development by allowing the user to perform functions such as manipulating registers in the FPGA and outputing the capability list. The SDK is common across all FusionXF capable products.

HDK

The HDL Development Kit contains the HDL libraries used to implement FusionXF. It also includes HDL functionality which is not strictly part of the Capabilities such as memory interfaces as well as hardware related features for FPGA pin definitions, clocks and timing constraints. The HDK includes reference designs showing how the HDK functionality can be used in real applications. The HDK is specific to the board that it supports.

ToolChain

FusionXF does not require any special development tools outside of those that would normally be required to develop a software and HDL application.

Software Tools

Linux – The standard GNU toolchain is used. Makefiles are provided to rebuild all software.

VxWorks – WindRiver WorkBench is recommended.

HDL Tools

Simulation – Examples provided with FusionXF are developed with Mentor Graphics Sim PE. Simulation scripts are provided. Note that a SWIFT license is required for simulating high speed serial interfaces, including the PCIe host interface.

Synthesis – All examples and library functions are synthesized using Xilinx XST. Synthesis scripts are included. Note that other synthesis tools (e.g. Synplicity Synplify) may be used but have not been tested.

Implementation – All .bit files are generated using Xilinx ISE. Implementations scripts and ISE project files are included.

VME P2 I/O and Breakout Module

Most of the VPF2 board's I/O is available via the backplane. System I/O is routed to the VME P2 connector while the GTP serial I/O is routed to the VXS P0 connector. To access the system I/O, an optional breakout module is available. For conduction-cooled variants, the backplane can incorporate these signals directly for a more robust configuration.

RS232 (EIA-232)

The MPC8641D processors have access to RS232 serial port I/O through the breakout module. The connectors are male (plug) right angle 9-way 'D' subminiature.

Table 4: Pin-out for RS232 Header

Pin	Signal Name	Signal Name	Pin
1	-	-	6
2	RXD	-	7
3	TXD	-	8
4	-	-	9
5	GND		

1000Base-T

A gigabit Ethernet channel is routed to the VME P2 user I/O connector. The PHY and magnetics are built into the VPF2 so the P2 breakout module routes this to a convenient connector.

Figure 6: 1000Base-T Ethernet

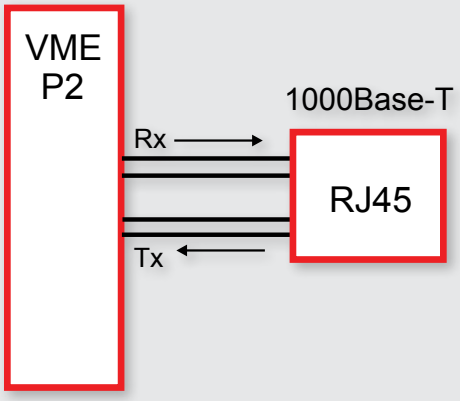


Figure 7: VPF2 VME P2 Breakout Module

JTAG

Two connectors on the breakout module provide access to JTAG boundary scan signals. P3 provides JTAG access to the module's PHY devices. P7 provides access to VPF2 JTAG signals routed to VME P2. Both connectors are 14-way 0.1" pitch shrouded headers.

VME64ext

The VXS specification (VITA 41) is based on the ANSI/IEEE VME64 specification with extensions requiring 3.3V power supply. This provides backwards compatibility with a wide range of third party vendors and products. This is a strength of the VXS specification; without the VXS connector fitted, boards like the VPF2 can be plugged into any VME64 compliant system. Conversely, VME64 boards without the VME P0 fitted can be plugged into a VXS system. Alternatively, backplanes including a mix of VME64 and VXS slots are available.



Table 5: Specifications

PowerPC CPU	
Device	Freescale MPC8641D
Speed	1.25GHz
Memory	2GB DDR2 SDRAM (inc. ECC)
FLASH	128MB
FPGA Nodes	
Device	Xilinx Virtex-5 LX110T or SX95T (speed grade 2)
Number of FPGAs	2
Memory (per FPGA)	4x 9 MB QDR-II SRAM (18-bit data paths at up to 250MHz) 2x 128MB DDR2 SDRAM (16-bit data paths at up to 250MHz) 32MB FLASH (for storing FPGA images only)
Connectivity	x8 PCIe to CPU per FPGA 4x RocketIO between FPGAs 4x RocketIO per FPGA for VXS 36 signals between FPGAs (single-ended) VME P2 (user defined I/O - 64 signals)
Clock References	3 sources: 156.25, 125 and 106.25MHz
Configuration	JTAG, MPC8641D and on-board FLASH
Ethernet	
Device	Embedded within MPC8641D
Speed	10/100/1000Mbps
Channel A	1000-SX (front panel optical) or 10/100-TX, 1000-T via VME P2, auto select
Channel B	1000-SX (front panel optical) or 10/100-TX, 1000-T (front panel RJ45) Note: this is defined as a build option

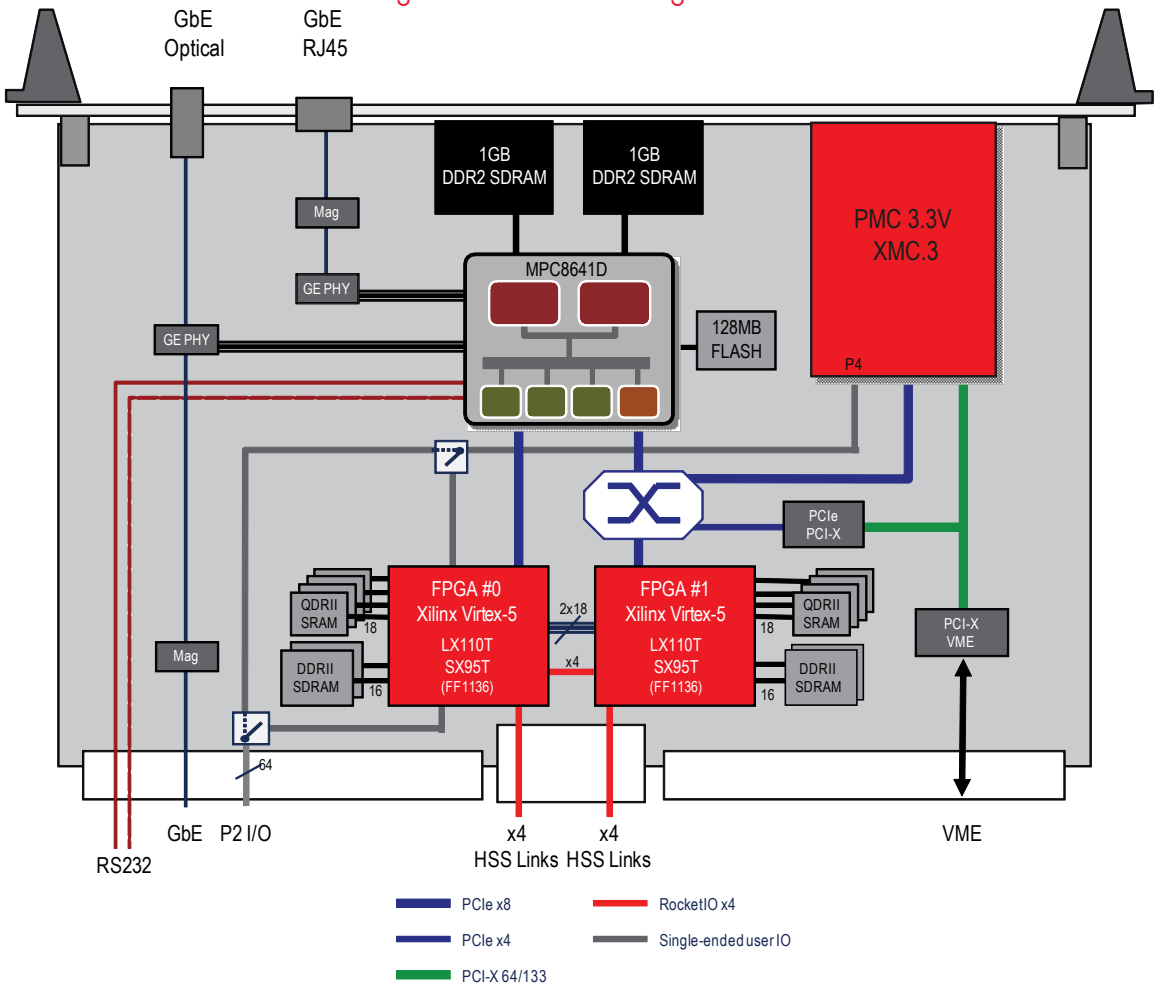
Serial I/O	
Device	DUART embedded within MPC8641D
Channels	2x RS232 (routed to VME P2)
PCI Express	
Device	PEX8532
Connectivity	FPGA #1 (x8), MPC8641D (x8), XMC (x8) and PCIe/ PCI-X bridge (x4)
VME	
Device	Tundra Tsi148
Compliance	2eSST, VME64, master/slave
VXS	
Compliance	VITA 41.0, payload
Protocol	FPGA defined
PMC/XMC Site	
PCI Compliance	PCI (33/66MHz), PCI-X (66/100/133MHz), 3.3V signaling
XMC (VITA 42)	P15 x8 PCIe channel
Software/HDL Code	
Operating System	VxWorks 6.5, Linux 2.6 (DENX Distribution)
Utilities	FLASH programming, diagnostics
Software/HDL examples	Examples (memory, PCIe, VXS) FusionXF FPGA Design Kit
Miscellaneous	
Power	VXS/VME64x 3.3V (TBA W), 5V (TBA W), +12V (TBA W), -12V (TBA W)

Table 6: Environmental Specifications

		Air-cooled		Conduction-cooled
		Level 1	Level 3	Level 3
Part number extension		- blank -	-C2H	-D3H
Temperature	Operational[1] (at sea level)	0°C to +50°C, 300 lfm air flow	-40°C to +75°C, 600 lfm air flow	-40°C to +75°C, (Card Edge Temp)
	Non-operational	-55°C to +85°C	-55°C to +85°C	-55°C to +85°C
Vibration	Operational (Sinus)	-	10G peak, 15-2,000Hz	10G peak, 15-2,000Hz
	Operational (Random)	-	0.04 g2/Hz (15- 1000Hz flat then 6dB/oct to 2000Hz)	0.1 g2/Hz (15-2000Hz)
Shock	Operational	-	30 g peak, 11ms half sine	40 g peak
Humidity	Operational	5-95% non-condensing	5-95% non-condensing	5-95% non-condensing
Altitude	Operational	10,000ft[2]	30,000ft[2]	75,000ft
Conformal Coat		No	Yes[3]	Yes[3]

Notes
1. Additional airflow might be required if the card is mounted together with, or next to, cards that dissipate excessive amounts of heat.
2. Operating altitudes may be reached by lowering the inlet air temperature and/or increasing the air-flow.
3. Coated with Humiseal 1B31. (ref. http://www.humiseal.com/ for details.)

Figure 6: VPF2 Block Diagram



Warranty

This product has a one year warranty.

Contact Information

To find your appropriate sales representative, please visit:

Website: www.cwcembedded.com/sales

Email: sales@cwcembedded.com

For technical support, please visit:

Website: www.cwcembedded.com/support1

Email: support1@cwcembedded.com

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