Product Reliability Qualification Strategy

TJA1101 in HVQFN36

Revision 2.0 — Mar, 8, 2018

Document information

Info	Content
Author / Department	Mathilde van Lieshout / Global Quality
BU / BL	BU Automotive / BL AAA / PL-IVN
Mag No / PL / Location	MAG-R16 / PL In-Vehicle Networking / Nijmegen
Customer, Market	Automotive
Distribution list	Project Core team Marcel Rijnsburger (Quality Manager PL IVN)

Revision history

Revision	Author	Date	Status	Description
2.0	Mathilde van Lieshout	Mar, 8, 2018	Approved	PPAP Reliability Qualification Strategy & Results

Contents

1. Summary

This report describes the reliability qualification strategy for the release of TJA1101 die in sub package HVQFN36 with Cu-wire, SOT1092FA14 at ATKH,.

1.1 Strategy

TJA1101 is based on the TJA1102, but it has single PHY transceivers instead of a dual PHY, all IP is equal. To a big extend the TJA1101 can be released based on data from TJA1102.

This strategy is defined according to the Quality and Reliability Specification [1], the copper mandatory way-of-working [9], AEC-Q100 rev G [4] & AEC-Q006 [5] and customer requirements[9].

The package & product will be released to the A1 package & product grade.

Based on the assessment of reliability risks, the application mission profile, and the re-use of generic data according to the rules of structural similarity [2], it is concluded that a very limited reliability test program is needed. The die/diffusion related items are structural similar with TJA1102/SOT684RB30.

A list of abbreviations and short descriptions of reliability test methods is given in the appendix.

1.2 Results

No package related issues are observed at package qualification on all material.

The TJA1101 package qualification at A grade is meeting all requirements.

All inspection for AEC-Q006 copper wire have been performed and meet the requirements.

For die related items, no relevant fails were observed during reliability qualification on TJA1102 material. For TJA1101 material qualification on ESD and LU were done and pass. The reliability qualification is pass and meets Q100 grade1 and the datasheet required mission profile.

The qualification has proven that the TJA1101 is an intrinsically robust product and meets all reliability release criteria.

Therefor this product can be released for automotive Grade 1 applications

1.3 Conclusion and gate recommendation

Package R-gate was granted, wk1806 in ATKH

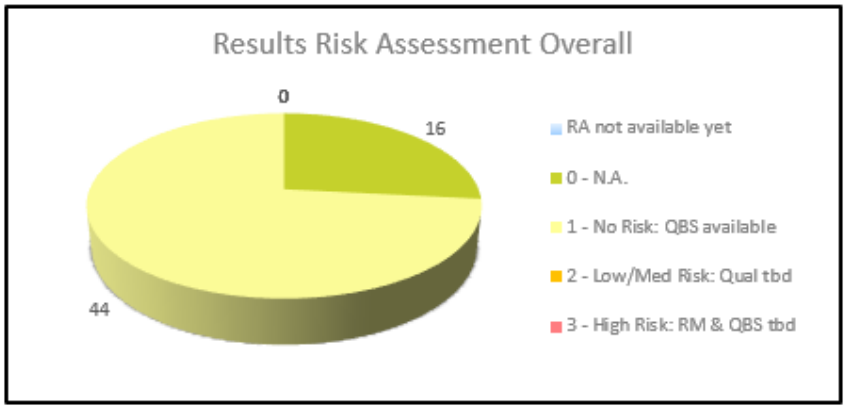
Based on the results, theTJA1101 in package HVQFN36/ SOT1092 can be released for Q100 automotive grade 1.

2. Introduction

2.1 Project description

The product TJA1101 is a derivative of TJA1102, with same IP but 1 PHY block less. Due to reduced pin count it is set into a smaller package with the same bill of materials.

The report is a qualification for a product release for a smaller die in a smaller package, which results in a different sub package and therefore also a sub package release.



The overall risk assessment on the reliability aspects of this project is very low: no risk identified.

2.2 Product description

The product TJA1101 is a derivative of TJA1102, with same IP but 1 PHY block less. Due to reduced pin count it is set into a smaller package with the same BOM.

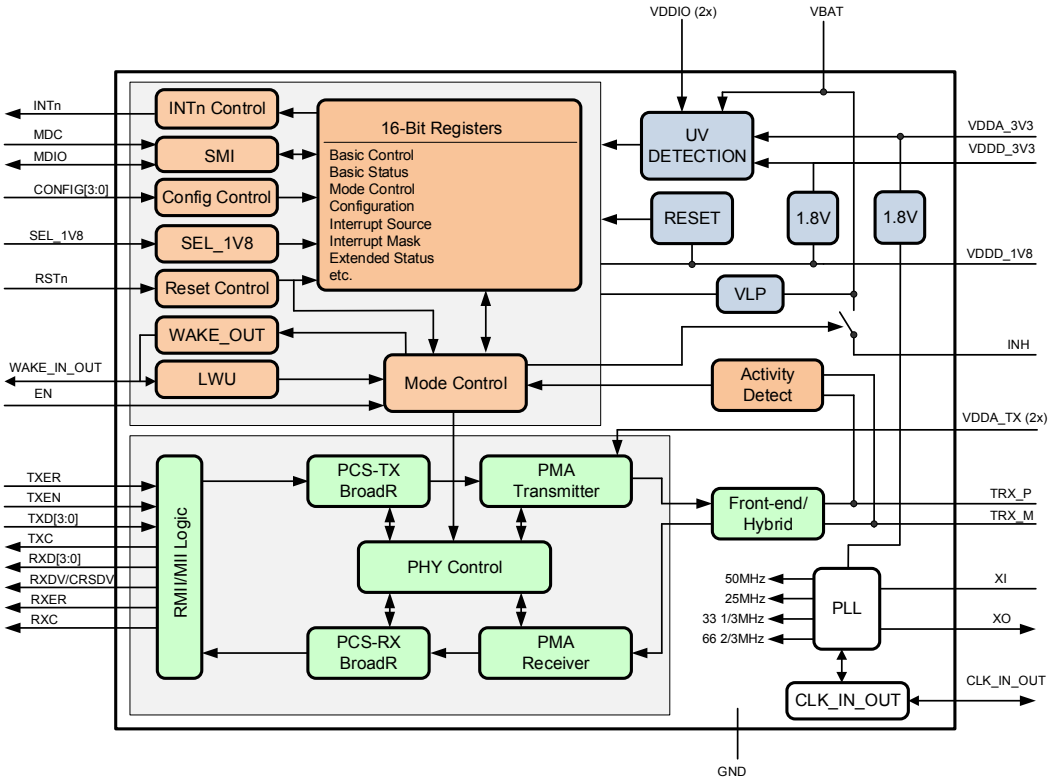


Fig 1. TJA1101 architecture. All IP is re-use from TJA1102

2.3 Detailed product information

Table 1. Product functionality application and construction details.

Product	
Product type	TJA1101 Ethernet transceiver, single PHY
Customer specific requirements	Yes HVQFN36 package with 0.5mm pitch terminals Dark Green Wettable sides Zero de-lamination for die top (die – EMC interface) and stitch bonding area Customer quality contracts [9]
Product specific components used	No

Do the used design library blocks have the status 'Silicon Validated?	Yes all IP from TJA1102
Does the product include bond-on-active (BonA) bond-pads?	No

Wafer-fabrication process	
Wafer-fabrication process grouping / Sub-capacity	ZABCD9FLVX (A-BCD9)
Wafer-fabrication process + Center	SSMC
Status and TCL of wafer-fabrication process	RFP since 16 Febr. 2012, , TCL AEC-Q100 grade 0
Wafer-fabrication mother fab	n/a
Acceleration models for wafer-level reliability available	yes

Package and Assembly	
Die size (Width x Length) / Thickness after grinding [mm]	2.404 x 2.52 (6.06 mm2) / 0.25mm
Subpackage / Outline / SOT# / Center	HVQFN36 / SOT1092/ ATKH
Status / Technology capability level of subpackage	Proven capability is grade1
Body size [mm´mm´mm]	6x6x0.85
WiDi blank number	W5486
Bond wire Diameter [µm] / material	20um / Cu 99.99
Wiring bonding method	Thermosonic. BPO=65 x 63µm probe & 65 x 54µm bonding.
Die-pad size [mm´mm]	4.1x4.1
Molding compound	G700LTD
Die attach	QMI-519
Lead frame material / plating	$CuFe_2P$ / RT-UPG (HDS)
Lead pitch [mm]	0.5
Heat-spreader / heat-sink material	-
Die protection material	Wafer coat (part of A-BCD9 process)
Moisture sensitivity level	Proven & released MSL1
Center for grinding and sawing	ATKH
Maximum E-field between any metal parts [V/mm]	327V/mm (@leads: 36V operating voltage over 0.11mm minimal space terminal ends, after sawing at package)

2.4 Application mission profile

For the application mission profile, both international standards and customer specific profiles are applicable. This covers AEC-Q100 grade 1.

Table 2. Mission profile.

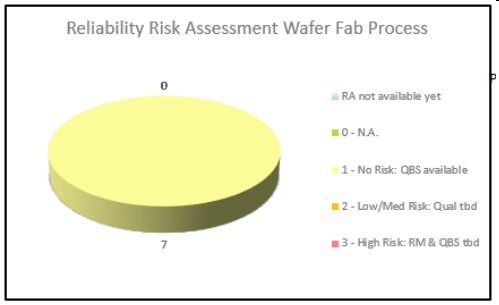
Mission Profile ' A1 ' : In line with AEC Q100 Grade 1					
Simplified Mission Profile					
Operation					
Field Lifetime	**Power-On-Hours (POH)**		**Relevant Temperatures**		**Stimuli**
years	**hours/day**	**hours/field life**	$T_{J,max-eff}$	T_a	**(V, I, f, loading)**
15 years	2.2 h	12000 h	109 °C	-40 to 125 °C	Application Specific
Thermo Mechanical Loading					
Field Lifetime	**Power Cycles**		**Relevant Temperatures**		**Effective Temperature Cycle**
years	**cycles/day**	**cycles/field life**	$T_{J,max-eff}$	$T_{a,min-eff}$	ΔT_{eff}
15 years	2 c	10950 c	109 °C	-3 °C	112 °C
Device Only	0 c				
Humid Environment					
Field Lifetime	**Time Standby (with bias)**		**Relevant Temperatures**		**Relative Humidity**
years	**hours/day**		$T_{trop,day}$	$T_{trop,night}$	
15 years	21.8 h	119400 h	30 °C	15 °C	95%
Hot Environment					
Field Lifetime	**POH + Time Standby + Time Off**		**Relevant Temperatures**		
years	**hours/day**	**hours/field life**	$T_{J,max-eff}$	$T_{trop,day}$	
15 years	2.2 + 21.8 + 0 h	131400 h	109 °C	30 °C	

3. Reliability Strategy

3.1 Risk assessment

The risk assessment is based on a review of the Reliability Knowledge Matrix, the Cu mandatory Way of Working, the assembly process FMEA, and knowledge built up during other product qualifications.

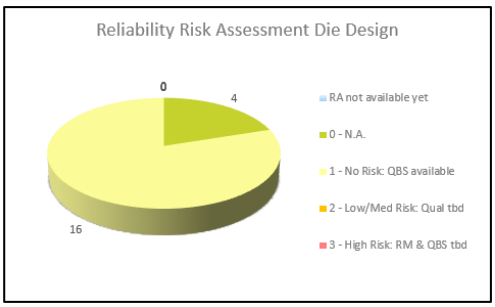
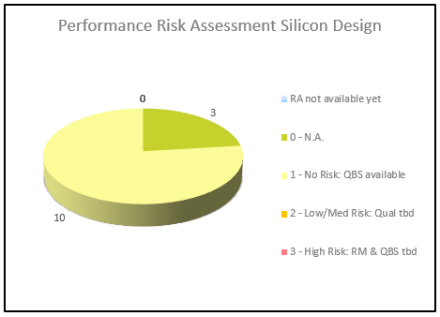
3.1.1 Wafer fab process risk assessment



No risk on wafer fab process	

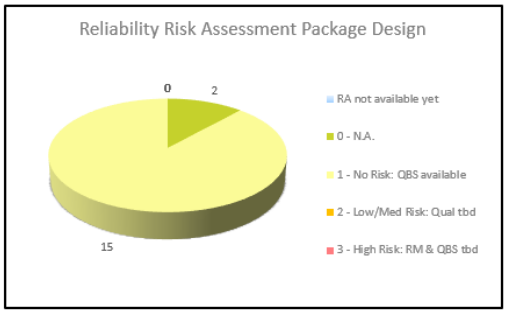
The A-BCD9 base line process has been qualified for Automotive Grade 1. The RFP status has been granted in wk1207. The TJA1101 will be the third Ethernet PHY product to be qualified in A-BCD9. Many other automotive product (KMA210 /Vanquish sensor: 4mm2, UJA113x green CAN SBC: 13mm2, UJA116x system basis chip: 5mm2 and ASL1010 LED driver: 1.5mm2) have been released.

3.1.2 Die design risk assessment

	
No risk on die design	No risk on silicon design

All IP of TJA1101 is exact copy of TJA1102.

3.1.3 Package design risk assessment

	
No risk on package design reliability, as the TJA1102 BOM is chosen	

3.1.4 Cu wire risk assessment

The BoM is copied from TJA1102.

Cu wire is especially suited for higher temperature application since the Cu-Al intermetallic ages slowly as compared to Au-Al intermetallic.

- Use the specially designed bond pads as indicated in the A-BCD9 design rule manual

- Wafer coat openings as indicated in the design rule manual
- PL IVN Cu requirement: HAST required for customer acceptance
- Molding compound was evaluated and released in a study at ATBK and proven on TJA1102 qualification.

Cu enabled bond pads

The die design has Cu enabled bond pads implemented with a separate area for probing and bonding. The control limits for Cu bonding (time, pressure, force) have been established by a backend manufacturing capability study (BMC). In line with the copper mandatory way-of-working each new product requires a BMC. Spec and control limits should be defined. Focus areas for the BMC are: (1) IMC contact size (2) control limits for buy-off & specification limits on indirect responses (3) stitch break

A BMC on TJA1102 is available and same settings should be applied.

Intermetallic aging Cu and Au wire

The activation energy for the IMC aging is about 1.0 eV both for Cu and Au wire. This means there is a distinct difference between the HTOL and HTSL testing. For HTOL testing the generic activation energy of 0.7eV is taken. For HTSL testing the activation energy was verified during the pre development of the BOM.

The IMC contact area is calculated based on the degradation model for G700LTD. For 30.000 h at 115 °C, the required diameter of homogenous IMC is 30 µm. To cover this Customer specific Mission Profile, the required test HTSL duration at 175 °C is 650 h.

Molding compound limits ionic transport (halogens)

The glass point of the Molding Compound might have a large impact on the (free) (chlorine) ion mobility in the molding compound matrix. The pre development study in ATBK selected G700LTD for automotive grade0. The G700LTD was released for technology capability level automotive using HAST testing at 130°C.

Board Level Reliability

Board level thermal cycling (BL TMCL) test robustness of the TJA1101 is proven by TJA1100 (same size) and TJA1102 (larger, same BoM).

Delamination and moisture

Delamination is seen as highest risk by the assembly center. An MSLA-1 investigation will be performed at risk mitigation.

In this exposed pad package the penetration path should be assessed via MSLA and if delamination on die pad exists it should be followed by dye/water penetration test.

3.2 Risk Mitigation

3.2.1 Copper mandatory way of working

The Copper mandatory way of working shows a large qualification program to evaluate all risks. Additional inspections at read points are added.

3.2.2 Built-in Reliability

The BOM with G700LTD is released for grade1 in ATBK and ATKH.

The Cu-bond pads are used as defined in the design rule manual with separate probing and bonding area's etc.

4. Structural similarity and generic data

4.1.1 Structural similarity

TJA1101 is structural similar to the larger TJA1102.

There is full structural similarity: a very limited qualification is required to release with G700LTD.

4.1.2 Generic data

Table 3. TJA1102 HTOL results

Product Name / Qual Batch number				S64816 Qualification Batch 1	S64817 Qualification Batch 2	S9A718 Qualification Batch 3	S66118 Qualification Batch 4
Reliability Tests	**Min. Size**	**Readpoints**		**Rejects / Size**	**Rejects / Size**	**Rejects / Size**	**Rejects / SS**
HTOL 170 degrC (Tj)	77	0 Hrs	3T	0 / 77	0 / 77	0 / 77	0 / 77
		168 Hrs	3T	0 / 77	0 / 77	0 / 77	0 / 77
		696 Hrs	3T	0 / 77	0 / 77	0 / 77	0 / 77
		1176 Hrs	3T	0 / 77			0 / 77
		1860 Hrs	3T	0 / 77			0 / 77

Table 4. TJA1102 package reliability test results

Product Name Qual Batch number				S64816 Qualification Batch 1	S64817 Qualification Batch 2	S9A718 Qualification Batch 3
Reliability T	**Min. S.S.**	**Readpoints**		**Rejects / SS**	**Rejects / SS**	**Rejects / SS**
PCON L.1 + HAST 130 degrC/ 85%RH.	77	0 Hrs.	3T	0 / 77	0 / 77	0 / 77
		PCON	3T	0 / 77	0 / 77	0 / 77
		96 Hrs	3T	0 / 77	0 / 77	0 / 77
		192 hrs	3T	0 / 77	0 / 77	0 / 77
		288 Hrs	3T	0 / 77		
		384 Hrs.	3T	0 / 77		
		FA	NA	Pass	Pass	Pass
PCON L.1 + TMCL -65/150 degrC	77	0 Hrs.	3T	0 / 77	0 / 77	0 / 77
		PCON	3T	0 / 77	0 / 77	0 / 77
		500 cycles	3T	0 / 77	0 / 77	0 / 77
		1000 cycles	3T	0 / 77	0 / 77	0 / 77
		1500 cycles	3T	0 / 77		
		FA	NA	Pass	Pass	Pass
HTSL 175 degrC	77	0 Hrs	2T	0 / 77	0 / 77	0 / 77
		504 Hrs	2T	0 / 77	0 / 77	0 / 77
		1008 Hrs	2T	0 / 77	0 / 77	0 / 77
		1500 Hrs	2T	0 / 77		
		FA	NA	Pass	Pass	Pass
BL TMCL		1000cls	Insitu	Pass	x	x
		2000cls	Insitu	Pass	x	x
		first fail		10035	x	x
		62% point	NA	> 10035	x	x
BL DROP		10 drops	NA	Pass	x	x
		20 drops	NA	Pass	x	x

Table 5. UJA113x ELFR results

Device				UJA1132HW/5V0	UJA1132HW/5V0	UJA1132HW/5V0
die version				MRA3	MRA3+MF1	MRA3+MF1
Batch id / date code				S63127 / ZsD1301	S63147 / ZsD1304	S98852 / ZsD1310
Design Version				tf1591C	tf1591C	tf1591C
Reliability Tests	**Min. S.S.**	**Conditions**	**Readpoints**			
6. ELFR Tjunction = 175C	800	150 deg.C (Tj)	0 hrs. 2T	0 / 800	0 / 800	0 / 800
			48 hrs. 2T	0 / 800	0 / 800	0 / 800

5. Reliability qualification test program

5.1 Test program

The qualification program is in agreement with the NXP Semiconductors Reliability Policy & Requirements [1], the NXP copper wire Way-of-Working [9], the Automotive Electronics Council

AEC-Q100-006 requirements for copper wire interconnections [5], and the Automotive Electronics Council 'Stress Test Qualification for Integrated Circuits' Q100 (AEC Q100) rev. G rules [4]. The relevant customer specific requirements (CSR) [8] have been reviewed and taken into consideration.

Table 6. IC reliability qualification test program

Stress Test	Abbr	#	Reference	Test conditions	ATE Temperature	Requirement	Lots CQS	Lots R	sample size (per lot)	Extra Samples (per lot)	Total number of samples	Product (s) to be tested	Comment
Moisture Sensitivity Level Assessment	MSLA	A0	NX4-00097	Level:	Room+Hot	Target Level:	1	1	14	0	14	TJA1101	MSL1
Pre Conditioning	PC	A1	NX4-00096	MSL	Room+Hot	Precon				0	0	TJA1101	Not required
ESD Human Body Model	ESD-HBM	E2	NX4-00057	Waveform according to test specification	Room+Hot	2 kV (standard)	1	1	3	0	3	TJA1101	
						2.5 kV (robust)		1	3	0	3		
ESD Charged Device Model	ESD-CDM	E3	NX4-00099	Waveform according to test specification	Room+Hot	500 V (standard)	1	1	3	0	3	TJA1101	
						650 V (robust)		1	3	0	3		
Latch-up	LU	E4	NX4-00100	Pulse according to test specification	Room+Hot	VDD,max ± 100 mA @ 85 °C (standard)	1	1	6	0	6	TJA1101	
						VDD,max ± 100 mA @ 125 °C (robust)		1	6	0	6		
Electrical Distributions	ED	E5	AEC Q100-009	Tj = 108.883268691752 Device specification	Room+Cold+Hot		1	3	3	0	9	TJA1101	
Electrical Characterization	CHAR	E7	Local Document	Covering MP conditions (T, V, I, f)		Tj = -40 to 125°C Device specification	1	3	3	0	9	TJA1101	
Thermal Characterization	THERM	E7	NX4-00109	According to test specification		Device specification	1	1	3	0	3	TJA1101	
Electrical Overstress	AMR		NX4-00101	Pulse according to test specification	Room+Hot	Characterization	1	1	3	0	3	TJA1101	

Notes:

[a] The 168-h read point is sufficient to pass CQS-Milestone for product release.

[b] robust read points need to be completed and reported before R-Gate.

Table 7. – Integrated Circuit Qualification Test Requirements based on Q006.

Complemented with NXP Cu WoW and Customer requirements in blue

Sequence #	Stress test Qualification step	TC	HAST / THB	HTSL
1	**Initial sampling**	Sample sizes per Q100 as required		
2	**SCAT @ T0 (1)**	Sample sizes per Q100 as required		
3	**Preconditioning to MSL 1**	3x94	3x96	
	Stitch Inspection (+ X-section)	3x2		
4	**SCAT after PC (1)**	3x14	3x14	
5	**ATE Test**	3x92	3x96	3x88
6	**Stress 1x**	3x92	3x96	3x88
7	**SCAT post-1x stress (1)**	3x14	3x14	n/a
8	**ATE Test**	3x92	3x96	3x88
9a	**Wire pull**	3x3 (4)	3x3 (4)	n/a
9b	**Ball shear**	3x3 (4)	3x3 (4)	n/a
10	**Cross-section**	3x1	3x1	3x1
	IMC Coverage (crack length)		3x2	3x2
	Store	3 x 5	3 x 5	3 x 5
11	**Stress 2x**	3x80 (2)	3x82	3x80
12	**SCAT post-2x stress (1)**	3x14(2)	3x14	n/a

13	**ATE Test**	3x80 (2,3)	3x82 (3)	3x80 (3)
14a	**Wire pull**	3x2 (2,4)	3x2 (4)	n/a
14b	**Ball shear**	3x2 (2,4)	3x2 (4)	n/a
15	**Cross-section**	3x1 (2)	3x1	3x1
	IMC Coverage (crack length)		3x2	3x2
	Store	3 x 5	3 x 5	

Notes:
(1) 14 marked samples per lot
(2) Performed even though board level reliability testing is performed, to be in line with the NXP MWoW.
(3) Any failures beyond 1X must directly relate to the Cu wire bonding system for them to count as a legitimate failure requiring further evaluation (i.e., the projected lifetime of failure, effect of fail mode on product lifetime, corrective/preventive action). The method of approval is determined between the user and supplier.
(4) Pull/shear as many as is possible per the number of wires per device to be qualified up to a maximum of 30 wires/balls from the total sample size specified. Follow Cu-mWoW: 2 samples (one for wire pull & one for ball shear with 3 wires & balls from each side , total 3 x 4 = 12 wires or balls) per read point to be taken.
Samples size numbers have been adjusted to meet about 70 samples on the last readpoints

5.2 Temperatures for final test at read points

Table 8. Final-test temperatures at read points for ICs with Automotive product grades [g].

Test	Abbr.	Cold (-40ºC)	Room (25ºC)	Hot (125 ºC)
ESD	ESD		X	X

Table also covers final testing after preconditioning prior to PPOT, UHST, HAST, THB, TMCL, TFAT, and PTC tests.

5.3 Parameter shift analysis

Not applicable. No HTOL, HAST and TMCL planned.

5.4 Product quality

A BMC is available on TJA1102. A small verification will be done (bond pull, ball shear, IMC)

The physical and construction analyses focusses on tests dedicated for wire, wire bond and mold.

Table 9. Physical and construction analysis qualification test requirements for ICs

Physical & Construction Analysis Qualification Tests for Plastic Packages				
	Test	Abbr.	Specification	Sample size (ICs) [1]
Physical	Flammability	FLAM	UL 94 / V0 1/8"	Supplier Certificate
	Thermal Characterization	THERM	NX4-00109	3
	Glueability	GLUE	NX4-00073	5
Construction Analysis	Dimensional Test	PD	Package Drawing	3x10 [2]
	Solderability with pre-aging [5]	SD	NX4-00068	11
	Decap Inspection	DECAP	Local Document	3
	Bond Pull Strength / Bond Shear [7]	BPS/BS	NX4-00012	5
	Cross Section (on selected relevant feature or location)	CROSS	NX4-00007	3
	Visual/mechanical inspection	V/M	NX4-0008/43/75	45
	X-Ray inspection	XRAY	NX4-00006	10
	SCAT inspection	SCAT	NX4-00105	22
	0hrs IMC inspection, Q006	IMC	AEC-Q006	3x2

6. Reliability qualification test implementation

6.1 HTOL / LTOL test implementation

See TJA1102 qualification.

6.2 HAST / THB test implementation

See TJA1102 qualification.

6.3 BLR test implementation

See TJA1102 & TJA1100 qualification.

7. Reliability in production

Production safe launch: For copper wire an extensive safe launch plan is advised. This has been created at V-gate, based on data available at that moment.

Burn-in was considered at safe launch plan creation. As considerable products are running production, it is not required.

Reliability monitoring is covered by the production standard monitoring.

8. Results of required reliability program

8.1 Overview lots used for TJA1101 Reliability Qualification

The used qualification batches are listed below.

Table 10. Qualification batch details.

Diffusion id	Wafer(s)	Date Code	Design
S66206	5	ZS7470X	tf2071A
S66221	1	ZS7490X	tf2071A
S66222	2	ZS7500X	tf2071A

8.2 Package reliability test results

These are the results of the required number of qualification batches at V-gate and R-gate of the product for package qualification.

Table 11. Package reliability results.

Product Name / Qual Batch number			TJA1101 S66206	TJA1101 S66221	TJA1101 S66222
Reliability Tests	**Min. S.S.**	**Readpoints**	**Rejects / RF / SS**	**Rejects / RF / SS**	**Rejects / RF / SS**
ConAna			Pass	Pass	Pass
MSLA	MSL1		Pass	Pass	Pass

8.3 Package Physical inspections

8.3.1 Construction Analysis

The construction analysis (ConAna) for the HVQFN36 package has been carried out at ATKH. The detailed results are stored in the Reliability Database. The conclusion is that all of the specified requirements are met.

The MSLA for the HVQFN36 package has been carried out at ATKH. The results are pass for MSL1.

8.3.1 Package conclusion SOT1092

No package related issues are observed at package qualification on all material.

The TJA1101 package qualification at A grade is meeting all requirements.

Final conclusion:

HVQFN36/ SOT1092 can be released for A T.C. grade / Q100 A1 T.C. grade.

Package R-gate was granted, wk1806 in ATKH.

8.4 Product reliability test results

These are the results of the required number of qualification batches at V-gate and R-gate of the product for product qualification

Table 12. Product reliability results.

Product Name				TJA1101
Qual Batch number				S66206
Reliability Tests	**Min. S.S.**	**Readpoints**		**Rejects / RF / SS**
ESD HBM		0 Hrs.	2T	Pass
2kV-pins		2kV	2T	Pass
2kV-pins		3kV	2T	Pass
6kV-pins		6kV	2T	Pass
6kV-pins		7kV	2T	Pass
ESD CDM		0 Hrs.	2T	Pass
		500V	2T	Pass
		750V	2T	Pass
		1000V	2T	Pass
Latch-up		0 Hrs.	2T	0/6
		VDDmax ±100mA@Tjmax	2T	0/6

8.5 Electrical verification tests

Table 13. Electrical verification test results.

Test	Description
ED	Pass. There is a small number of parameters with low Cpk, due to non-normal distribution, caused by trimming. Distribution evaluation shows no impact on yield or quality.
ESD-HBM	Pass The 2kV pins pass upto and including 3kV The 6kV pins pass upto and including 7kV No shift analysis was performed, as all products pass upto 2 levels above the required level
ESD-CDM	Pass. Requirement is 500V for all pins. All pins were stressed and pass upto and including 1000V

Test	Description
	No shift analysis was performed, as all products pass upto 2 levels above the required level
LU	Pass. Autonomous Normal Mode, 125C Covers Q100 requirement HAST mode. 125C

Conclusion: the electrical verification tests meet the requirements.

8.6 Conclusion for TJA1101 Reliability Qualification

No relevant fails were observed during reliability qualification on a TJA1101 material. The reliability qualification is pass and meets Q100 grade1 and the datasheet required mission profile.

With this qualification also package HVQFN36, SOT1092 is qualified and released for Q100, grade1.

The qualification has proven that the TJA1101 is an intrinsically robust product and meets all reliability release criteria.

Therefor this product can be released for automotive Grade 1 applications.

9. References

1. Quality and Reliability Specification, NXPOMS-1719007347-2410, November 2016.
2. Structural Similarity Procedure, NX3-00113, April 2015.
3. QSRB web-page,

   http://nww.new.nxp.com/sites/business/how-we-work/ops/ssc/quality/rqc/rlt/wg-policy/Pages/QSRB.aspx
4. Failure mechanism based stress test qualification for integrated circuits, AEC-Q100 – Rev-G.
5. Qualification Requirements for Components using Copper (Cu) Wire Interconnections, AEC-Q006, June 8, 2015.
6. TJA1102 ADS
7. Product Reliability Qualification Strategy TJA1102 in HVQFN, Mathilde van Lieshout, June 2015
8. Customer quality contracts
   https://nxp1.sharepoint.com/teams/36_2/teams/QualitySales/SitePages/Customer%20Quality%20Contracts%20-%20Automotive.aspx

9. Requirements and Way of Working for Cu- and Ag-Alloy-Wire Bonding Development, Qualification and Release, NXPOMS-1719007347-1969 version Aug 2016

10. Appendix 1

10.1 Operational stress test methods

Test	Abbreviation	Description
Early Lifetime Failure Rate	ELFR	Stress test accelerating the operational **early lifetime** of semiconductor devices. Operation means that the device is in an application like environment: supply voltage, supply and output current, input signals, output loads. The acceleration is mainly achieved by temperature (Si or junction temperature inside the packaged device is 150 °C), but supply voltage and sometimes current can be used too. Failure modes are typically particle (in gate oxide or intermetal dielectric) or latent defect related (intermitting contacts both in vias as well as bondball to bondpad). Note that also major design errors can be revealed via this test.
High Temperature Operating Life	HTOL	Stress test accelerating the operational **intrinsic lifetime** of semiconductor devices. Also in this case operation means that the device is in an application like environment: supply voltage, supply and output current, input signals, output loads. The acceleration is mainly achieved by temperature (Si or junction temperature inside the packaged device is 150 °C), but supply voltage and sometimes current can be used too. Failure modes are typically wearout related: electromigration, gate oxide breakdown, Vt-shift or transistor characteristic degradation due to hot carriers or negative bias instability, mobile ions.
Power Temperature Cycling	PTC	Alternative acceleration test (compare with TMCL) to investigate thermo-mechanical failure modes (related to degradation in bond wiring or die bonding, be it glue or alloy). Test is performed only on devices with a total dissipation above 1 Watt and Delta T (on vs. off) higher than 40 ºC. Two conditions: -40 ºC to +125 ºC for 1000 cycles or -65 ºC to +150 ºC for 500 cycles while simultaneously powering the device on and off.
Thermal Fatigue	TFAT	Alternative acceleration (compare with TMCL) test to investigate thermo-mechanical failure modes (related to degradation in bond wiring or die bonding, be it glue or alloy). In this case the environment is stable (room temperature) and the device is switched on and off with a temperature rise of 50 °C for 10 kcls. This test is only for (discrete) power devices (P_{diss} >> 1 W).
Soft Error Rate	SER	This characterization is to be used to evaluate robustness CMOS processes with gate lengths of 0.18 mm and lower as well as libraries containing SRAM memories against soft errors (flipping but recoverable bits). Soft errors in semiconductor products are caused by emission of alpha particles from die and package materials, and by cosmic rays, particularly neutrons.
Erase-Write Cycling	ERWR	This test is intended to confirm the ability of EEPROM/FLASH devices to withstand the specified number of ERASE/WRITE EEPROM/FLASH reprogramming cycles.
Data retention	DRET	This test is intended to confirm the data retention performance of EEPROM/FLASH devices. The data retention is verified on products, which have been subjected to the specified number of erase/write cycles (“preconditioning”). Typical ambient test temperature is 150 °C on package level and 250 °C on wafer level.

Test	Abbreviation	Description
Electro-Thermally Induced Parasitic Gate Leakage	GL	Test to characterize circuit performance disruption due to charge accumulation at moulding-compound-to-die interface due to high electrical field and/or ions sources in the neighborhood of the device. Typical exposure is 400 V for 10 minutes at 155 °C.

10.2 Environmental stress test methods

Test	Abbreviation	Description
Moisture Sensitivity Level Assessment	MSLA	Methodology to determine the moisture sensitivity for Surface Mount Devices (SMD) in relation to PCB assembly by Hot Convection reflow.
Preconditioning	PCON / PC	Simulation and Acceleration of shipment and board assembly of semiconductor devices in epoxy moulding compounds. Mandatory to be executed before typical environmental endurance tests like TMCL, PPOT/AC, UHST, HAST, THB for SMD products according to moisture sensitivity levels. Special preconditioning for Through Hole Devices (THD) prior to PPOT/AC, UHST, HAST, THB is described in NX4-00095
Highly Accelerated Steam Test	HAST	Preferred biased humidity stress test at 130 °C and 85 % RH to investigate endurance of the product regarding internal corrosion and leakage formation by transport of ions/water. Typical for standby with V_{supply} on.
Temperature Humidity Bias	THB	Alternative biased humidity stress test at 85 % °C and 85 % RH to investigate endurance of the product regarding internal corrosion and leakage formation by transport of ions/water. Typical for standby with V_{supply} on.
Unbiased Highly Accelerated Steam Test	UHAST	Preferred unbiased humidity stress test at 130 °C and 85 % RH to investigate endurance of the product regarding internal corrosion and leakage formation by transport of ions/water. Typical for standby without V_{supply}.
Autoclave	PPOT / AC	Alternative unbiased humidity stress test at 121 °C and 100 % RH to investigate endurance of the product regarding internal corrosion and leakage formation by transport of ions/water. Typical for standby without V_{supply}.
Temperature Humidity Unbiased	THNB	Alternative unbiased humidity stress test at 85 °C and 85 % RH to investigate endurance of the product regarding internal corrosion and leakage formation by transport of ions/water. Typical for standby without V_{supply}.
Temperature Cycling	TMCL / TC	Acceleration test to investigate thermo-mechanical failure modes (like delamination, die lift, wire break, bond ball lift, die crack, pattern shift, passivation crack etc) due to both ambient and internal temperature changes during device or application power up and switching off as well as ambient storage. Two standard JEDEC conditions are used: -65 to 150 °C (the preferred condition C) and -55 to 125 °C (the alternative condition B).
High Temperature Storage Life	HTSL	Environment stress simulating storage and accelerating intermetallic bond fracture failures at high temperatures (without V_{supply}). Typical test temperature is 150 °C while no bias is applied. Test temperatures of 175 °C can be used as well.