SUBJECT: i.MX6DL

DATE: 12/10/2012

USB 2.0 High Speed Certification Report

Customer:
Freescale Semiconductors Inc.
6501, William Cannon Drive West
Austin, Texas
USA

Device:
i.MX6DL

TID 40001472
USBD660

Supplier:
Testronic Labs Belgium nv.
Wetenschapspark 7
B-3590 Diepenbeek

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1. CUSTOMER

Freescale Semiconductors Inc.
6501, William Cannon Drive West
Austin, Texas
USA

2. SUPPLIED HARDWARE AND SOFTWARE

2.1. ASSETS

Description	Manufacturer	Model
Device Under Test	Freescale	i.MX6DL

Comment:
Device under test has one High Speed device and one High Speed embedded host port.

2.2. GENERAL EMBEDDED HOST INFORMATION

Item	Info
Maximum rated current	500mA
Hub support	True (5tier)
How messages are displayed	Terminal
Support remote wakeup	False
TPL	MSC, Mouse, Keyboard, Hub

2.3. USED MEASUREMENT EQUIPMENT BY TESTRONIC LABS

Description	Manufacturer	Identity	Serial Nr
USB 2.0 Automated Software	Agilent	N5416A	
Differential Probe	Agilent	1169A	N10149
Pulse/Pattern generator	Agilent	81134A	MY42801040
Digital real-time oscilloscope	Agilent	DSA91304	MY50140172
Probe	Agilent	E2697A	MY43005817
Probe	Agilent	E2697A	MY50091034
Current probe	Tektronix	TCP202	B019512

2.4. TEST TOOLS

Description	Version
USB Electrical Analysis Tool "USBET20"	1.13
USB20CV	1.4.9.2
USB30CV	1.0.1.1

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2.5. TEST PROCEDURES

Procedure		Version
Tools(USBET, USBCV)	http://www.usb.org/developers/tools/	
Updates	http://compliance.usb.org	
High Speed Device Electrical	http://www.usb.org/developers/compliance/	1.0
Low/Full Speed Test Procedure	http://www.usb.org/developers/USB-IFTestProc_1_3.pdf	1.3

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3. SUMMARY OF THE PERFORMED TESTS

ELECTRICAL LEGACY

Upstream Full Speed Signal Quality	passed
Device Inrush	passed
Device Back Voltage	passed
Downstream Full Speed Signal Quality	passed
Downstream Low Speed Signal Quality	passed
Drop	passed

ELECTRICAL HIGH SPEED

Upstream High Speed Signal Quality	passed
Device Packet Parameters	passed
Device CHIRP Timing	passed
Device Suspend/Resume/Reset Timing	passed
Device Test J/K, SE0_NAK	passed
Device Receiver Sensitivity	passed
Downstream High Speed Signal Quality	passed
Host Packet Parameters	passed
Host CHIRP Timing	passed
Host Suspend/Resume/Reset Timing	passed
Host Test J/K, SE0_NAK	passed

DEVICE FRAMEWORK USBCV

USB20CV Chapter 9	passed
USB20CV MSC	passed
USB30CV Chapter 9	passed

DEVICE POWER MEASUREMENTS

Power Measurements	passed

DEVICE GOLDEN TREE

Interoperability	passed

EMBEDDED HOST INTEROPERABILITY

Functionality with TPL	passed

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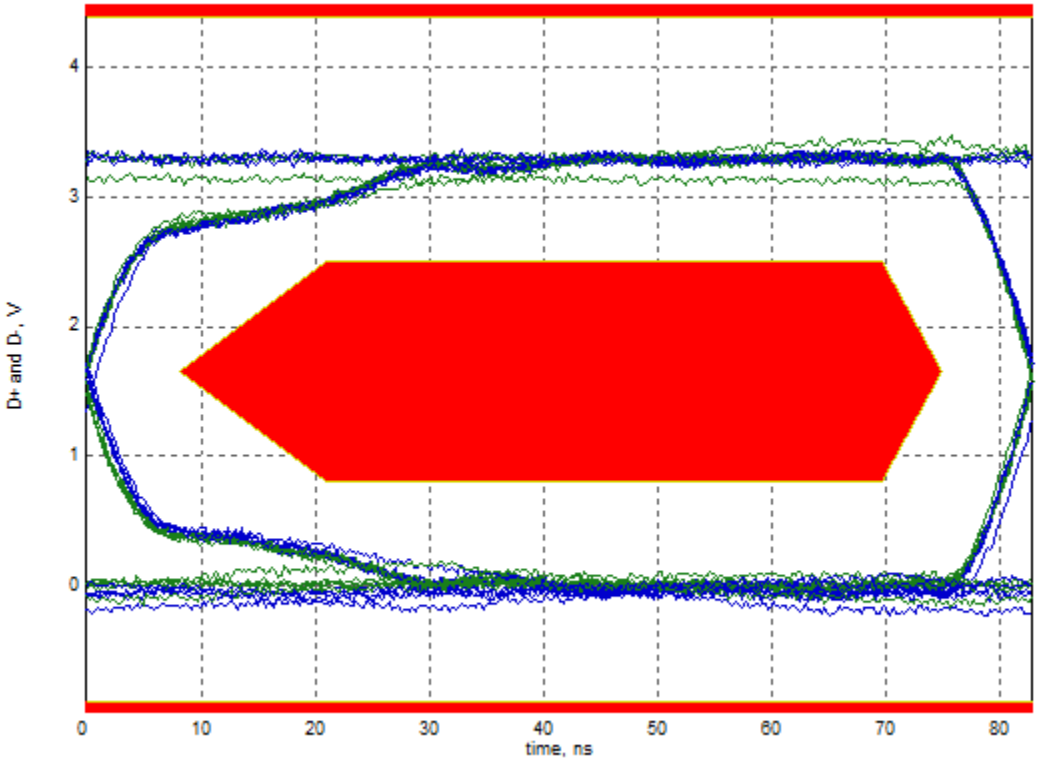
4. RESULTS

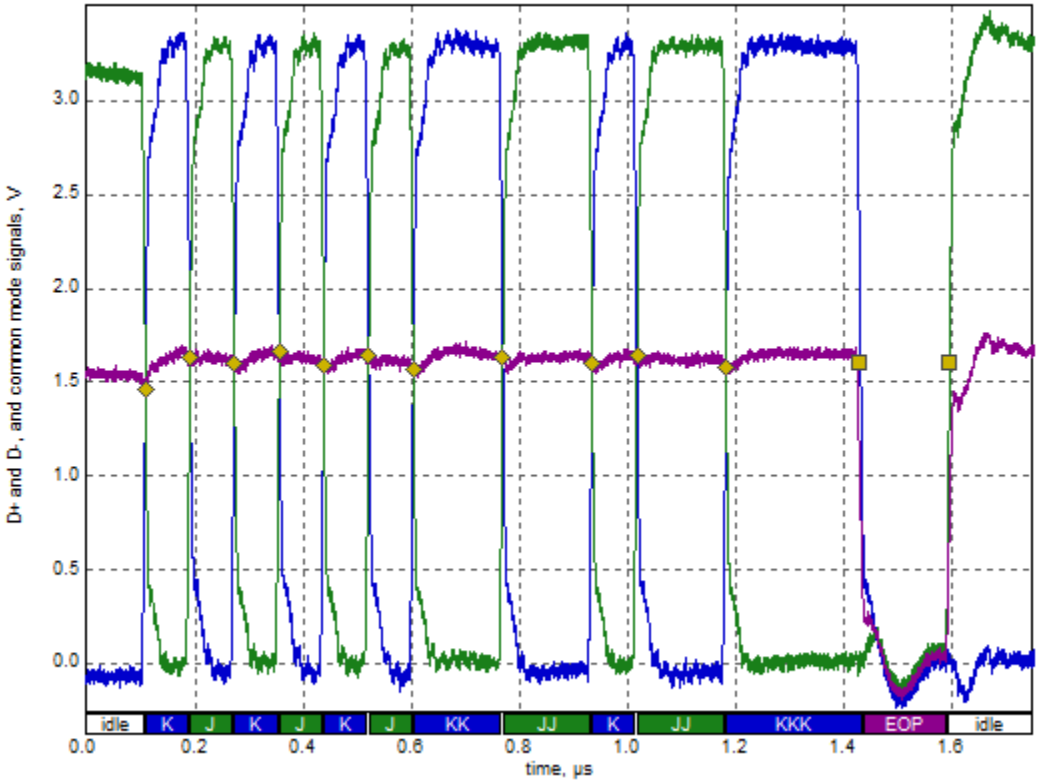
4.1. ELECTRICAL LEGACY

4.1.1. UPSTREAM FULL SPEED SIGNAL QUALITY

The Freescale Semiconductors Inc. i.MX6DL passed the Full Speed Upstream Signal Quality test.



Signal Eye



Date and Common Mode Voltage

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- eye passes
- EOP width: 165.59 ns
  EOP width passes
- Measured signaling rate: 11.9993 MHz
  signal rate passes
- Edge Monotonicity: 17 mV
  Monotonic Edge passes
- Crossover voltage range: 1.46 V to 1.66 V, mean crossover 1.60 V
  (first crossover at 1.46 V, 10 other differential crossovers checked)
  crossover voltages pass
- Consecutive jitter range: -253.821 ps to 191.769 ps, RMS jitter 176.435 ps
- Paired JK jitter range: -5.690 ps to -5.359 ps, RMS jitter 5.527 ps
- Paired KJ jitter range: -154.690 ps to 152.275 ps, RMS jitter 111.807 ps
  jitter passes

Additional Information

- Rising Edge Rate: 250.68 V/us (Equivalent risetime = 10.53 ns)
  (minimum 132.00 V/us, maximum 660.00 V/us)
- Falling Edge Rate: 267.24 V/us (Equivalent falltime = 9.88 ns)
  (minimum 132.00 V/us, maximum 660.00 V/us)
- Edge Rate Match: 6.39% (limit +/-10%)

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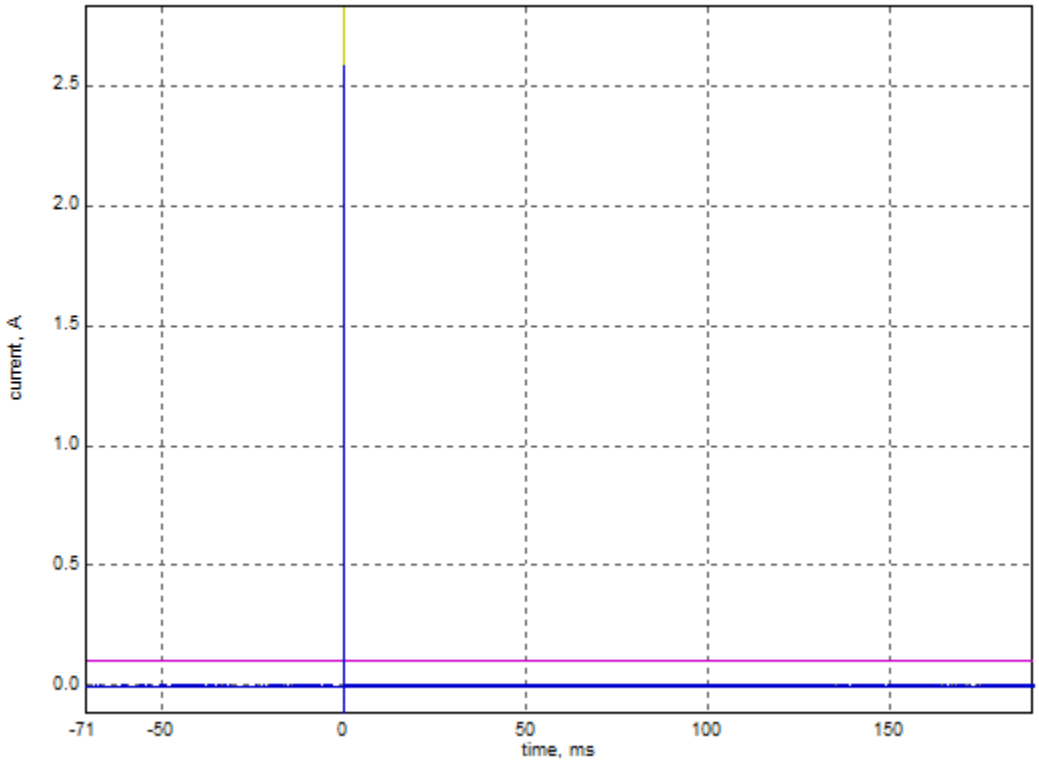
4.1.2. DEVICE INRUSH CURRENT

The measured Inrush current of the Freescale Semiconductors Inc. i.MX6DL is 14.89 µC. The USB spec allows up to 10µF to be hard started, which represents an allowed load of approximately 50 µC. With a measured load of 14.89 µC, the device passed the inrush current test.



Inrush Current

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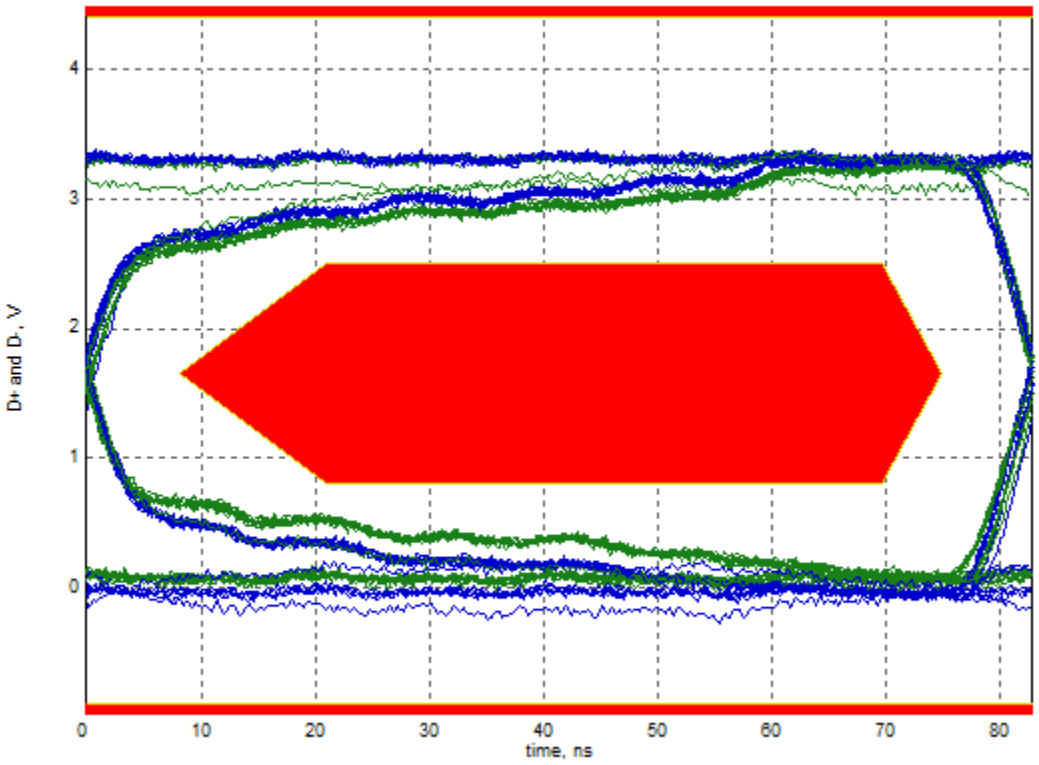
4.1.3. DOWNSTREAM FULL SPEED SIGNAL QUALITY

The Freescale Semiconductors Inc. i.MX6DL passed the Full Speed Downstream Signal Quality test.



Signal Eye

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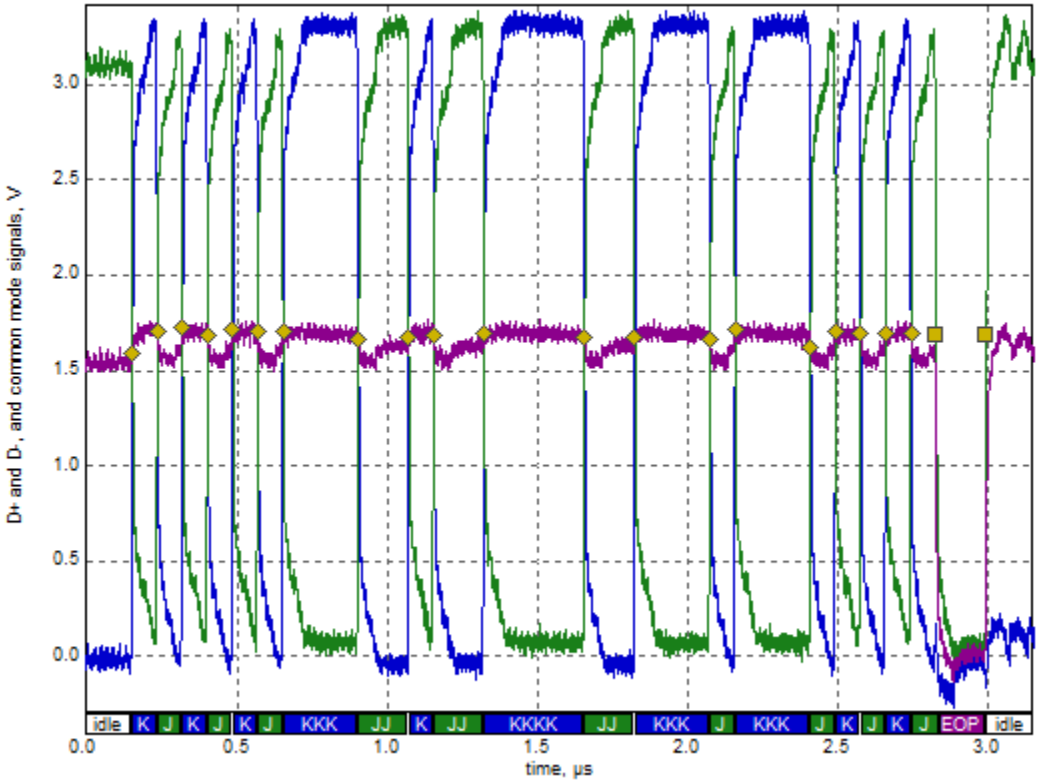

Date and Common Mode Voltage

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- eye passes
- EOP width: 167.06 ns
  EOP width passes
- Measured signaling rate: 12.0002 MHz
  signal rate passes
- Edge Monotonicity: 13 mV
  Monotonic Edge passes
- Crossover voltage range: 1.59 V to 1.73 V, mean crossover 1.68 V
  (first crossover at 1.59 V, 19 other differential crossovers checked)
  crossover voltages pass
- Consecutive jitter range: -466.161 ps to 374.799 ps, RMS jitter 255.837 ps
- Paired JK jitter range: -467.206 ps to 380.207 ps, RMS jitter 220.525 ps
- Paired KJ jitter range: -511.883 ps to 457.412 ps, RMS jitter 328.679 ps
  jitter passes

Additional Information

- Rising Edge Rate: 257.42 V/us (Equivalent risetime = 10.26 ns)
  (minimum 132.00 V/us, maximum 660.00 V/us)
- Falling Edge Rate: 138.74 V/us (Equivalent falltime = 19.03 ns)
  (minimum 132.00 V/us, maximum 660.00 V/us)
- Edge Rate Match: 59.91% (limit +/-10%)

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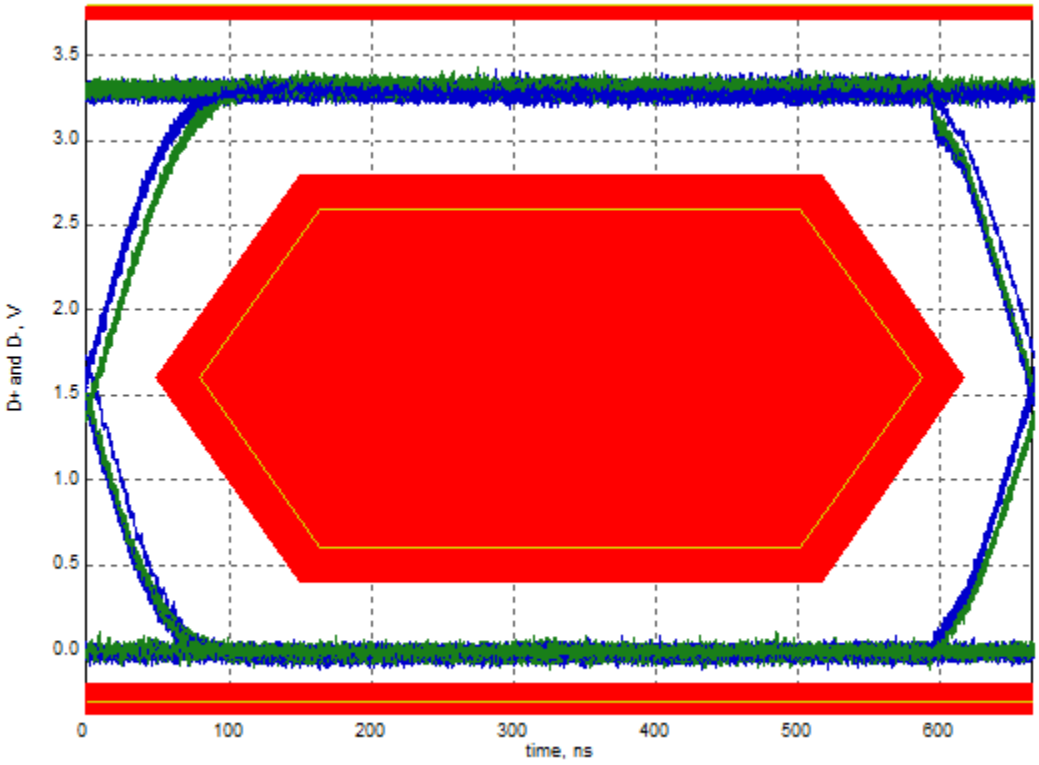
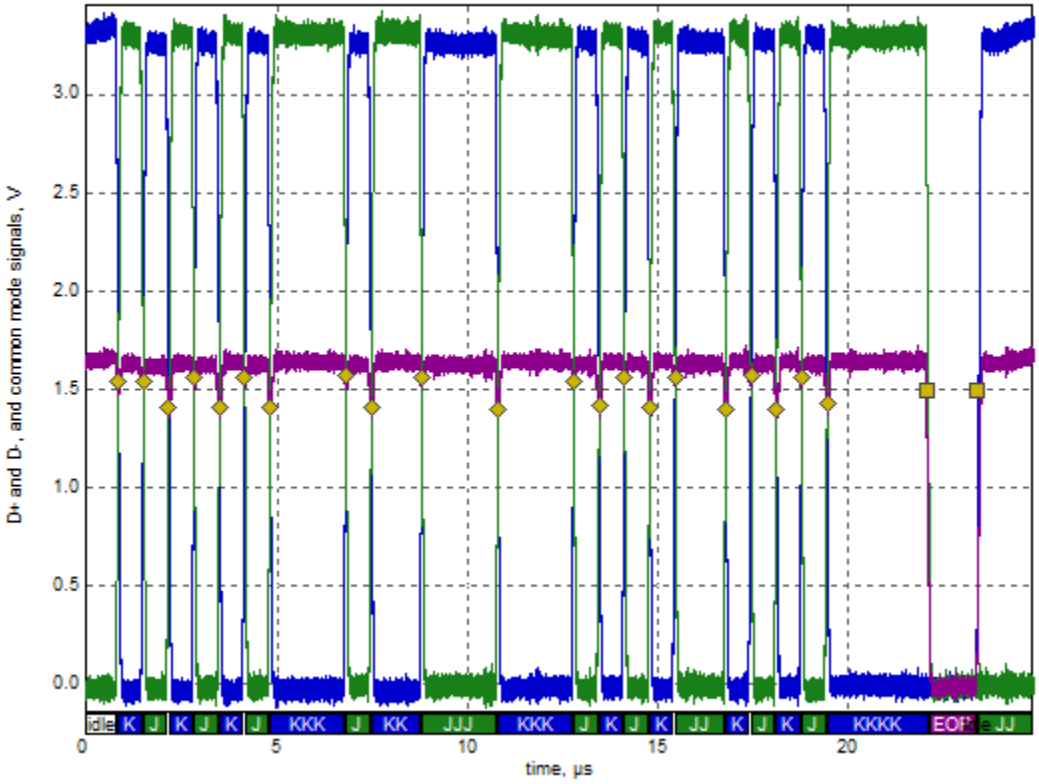
4.1.4. DOWNSTREAM LOW SPEED SIGNAL QUALITY

The Freescale Semiconductors Inc. i.MX6DL passed the Low Speed Downstream Signal Quality test.



Signal Eye



Date and Common Mode Voltage

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- eye passes
- EOP width: 1.33 us
  EOP width passes
- Measured signaling rate: 1.4999 MHz
  signal rate passes
- Edge Monotonicity: 84 mV
  Monotonic Edge passes
- Crossover voltage range: 1.40 V to 1.57 V, mean crossover 1.49 V
  (first crossover at 1.55 V, 20 other differential crossovers checked)
  crossover voltages pass
- Consecutive jitter range: -2.371 ns to 1.532 ns, RMS jitter 1.482 ns
- Paired JK jitter range: -0.872 ns to 0.972 ns, RMS jitter 0.522 ns
- Paired KJ jitter range: -0.906 ns to 0.522 ns, RMS jitter 0.434 ns
  jitter passes

Additional Information

- Rising Edge Rate: 25.81 V/us (Equivalent risetime = 102.29 ns)
  (minimum 8.80 V/us, maximum 35.20 V/us)
- Falling Edge Rate: 26.98 V/us (Equivalent falltime = 97.86 ns)
  (minimum 8.80 V/us, maximum 35.20 V/us)
- Edge Rate Match: 4.43% (limit +/-20%)

4.1.5. HOST DROP TEST

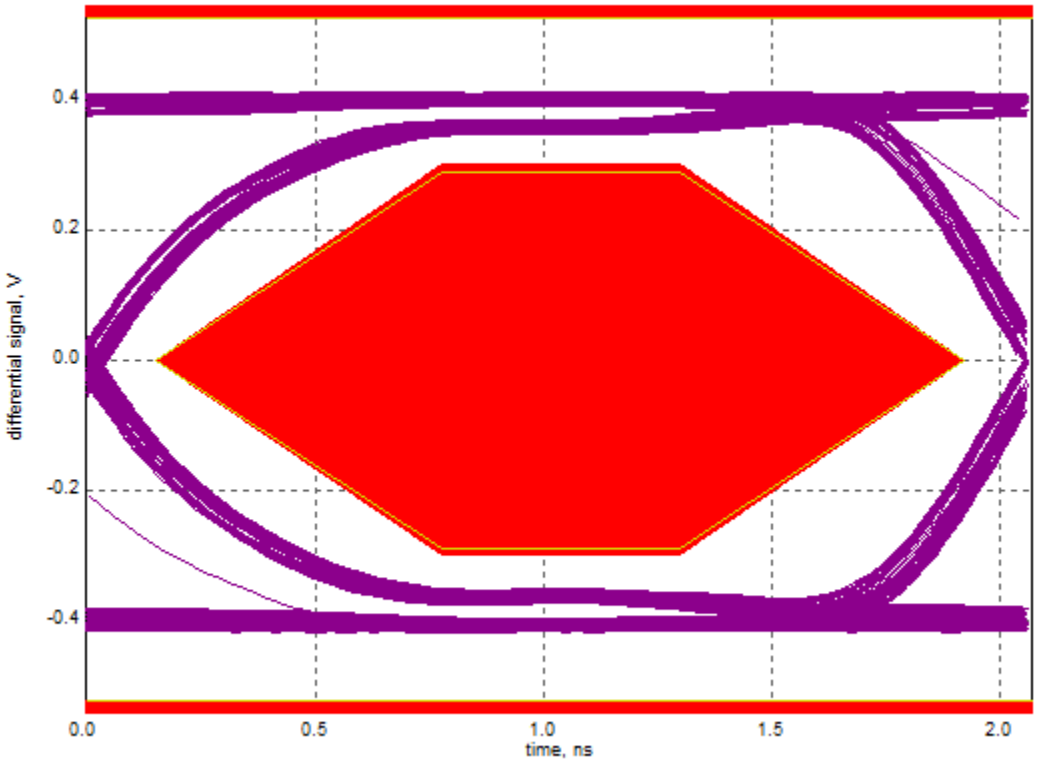
The Freescale Semiconductors Inc. i.MX6DL passed the Drop test.

Load	Vbus (V)
No Load	5.02
500mA Load	4.90

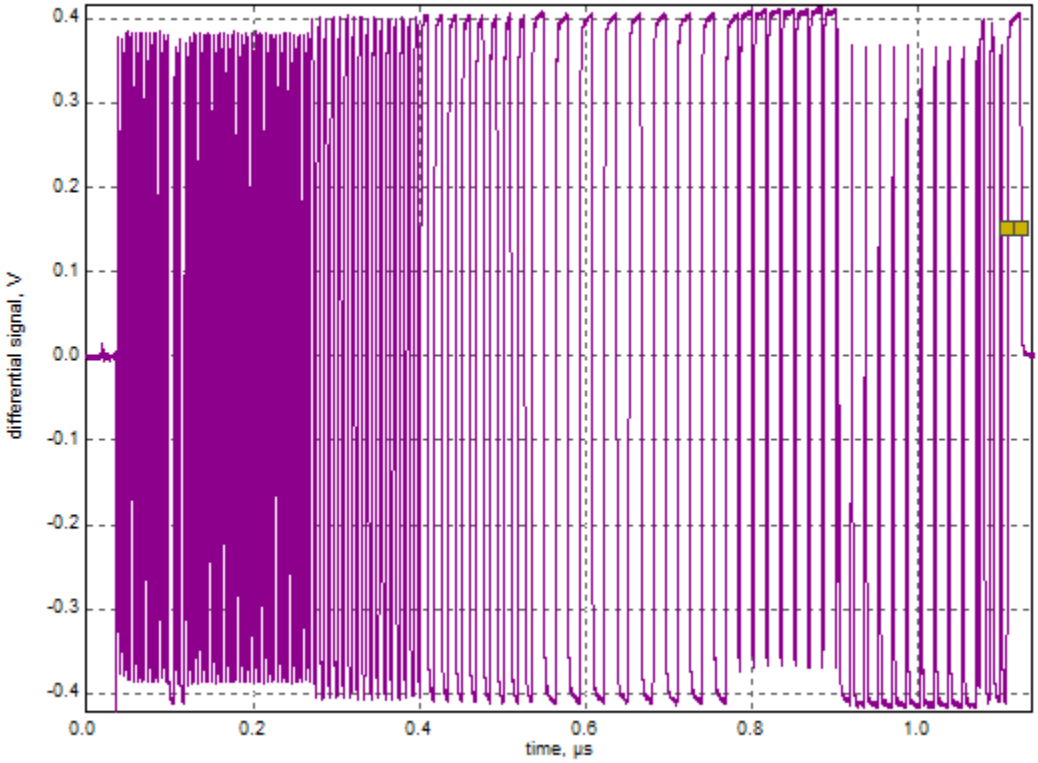
4.2. ELECTRICAL HIGH SPEED

4.2.1. UPSTREAM HIGH SPEED SIGNAL QUALITY

The Freescale Semiconductors Inc. i.MX6DL passed the High Speed Upstream Signal Quality test.



High Speed Signal Eye



Date and Common Mode Voltage

- Overall result: pass!
- Signal eye:
  eye passes
- EOP width: 7.96 bits
  EOP width passes
- Measured signaling rate: 479.9701 MHz
  signal rate passes
- Edge Monotonicity: 0 mV
  Monotonic Edge passes
- Rising Edge Rate: 1024.17 V/us (624.89 ps equivalent risetime)
  passes
- Falling Edge Rate: 1026.39 V/us (623.54 ps equivalent falltime)
  passes

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Additional Information

- Consecutive jitter range: -31.418 ps to 49.599 ps, RMS jitter 21.677 ps
- Paired JK jitter range: -59.313 ps to 49.760 ps, RMS jitter 11.846 ps
- Paired KJ jitter range: -41.789 ps to 40.593 ps, RMS jitter 8.086 ps

EL_2 USB 2.0 High-Speed transmitter data rate must be 480 Mb/s +-0.05%
Data rate: 479.9701 MHz
Passed

EL_4 USB 2.0 upstream facing port on a device without a captive cable must meet Template 1 transform waveform requirements measured at TP3
Passed

EL_6 USB 2.0 HS Driver must have 10 to 90% differential rise and fall times of greater than 500 ps.
Passed

EL_7 USB 2.0 HS Driver must have monotonic data transitions over the vertical openings specified in the appropriate eye pattern template.
Passed

4.2.2. DEVICE PACKET PARAMETERS

EL_21 The SYNC field for all transmitted packets (not repeated packets) must begin with a 32-bit SYNC field. Data Packets SYNC field: 64.60 ns
Passed

EL_22 When transmitting after receiving a packet, hosts and devices must provide an inter-packet gap of at least 8 bit times and no more than 192 bit times.
Inter-packet gap: 336.58 ns
Inter-packet gap: 336.00 ns
Passed

EL_25 The EOP for all transmitted packets (except SOFs) must be an 8-bit NRZ byte of 01111111 without bit stuffing.
NRZ byte: 16.78 ns
Passed

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4.2.3. DEVICE CHIRP TIMING

EL_28 Devices must transmit a chirp handshake no sooner than 2.5µs and no later than 6ms when being reset from suspend or full-speed state.
Chirp handshake: 1503 µs
Passed

EL_29 The chirp handshake generated by a device must be at least 1ms and not more than 7ms in duration.
Chirp handshake: 2.00 ms
Passed

EL_31 During device speed detection, when a device detects a valid chirp K-J-K-J-K-J sequence, the device must disconnect its 1.5K pull-up resistor and enable its high speed terminations within 500µs. Disconnect time pull-up resistor: 3.70 µs
Passed

4.2.4. DEVICE SUSPEND/RESET/RESUME

EL_38 A device must revert to full-speed termination no later than 125µs after there is a 3ms idle period on the bus.
Full-speed revert time: 3.003 ms
Passed

EL_39 A device must support the suspend state.
Passed

EL_40 If a device is in the suspend state and was operating in high-speed before being suspended, then the device must transition back to high speed operation within two bit times from the end of resume time signaling
Note: It is not feasible to measure the device transition back to high-speed operation within two bit time from the end of the resume signaling. The presence of SOF at nominal 400mV amplitude following the resume signaling is sufficient for this test.
Passed

EL_27 Devices must transmit a chirp handshake no sooner than 3.1ms and no later than 6ms when being reset from a non-suspended high-speed mode. The timing is measured from the beginning of the last SOF transmitted before the reset begins.
Chirp handshake: 3.50 ms
Passed

EL_28 Devices must transmit a chirp handshake no sooner than 2.5µs and no later than 6ms when being reset from suspend or a full-speed state.
Chirp handshake: 1503 µs
Passed

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4.2.5. DEVICE TEST J/K, SE0_NAK

EL_8 When either D+ or D- are driven high, the output voltage must be 400mV +-10% when terminated with precision 450 Ohm resistors to the ground

Test	D+ Voltage (mV)	D- Voltage (mV)
J	413	6
K	6	425

Passed

EL_9 When either D+ or D- are not being driven, the output voltage must be 0V +-10mV when terminated with precision 450 Ohm resistors to the ground.

Test	Voltage (mV)
D+	1
D-	1

Passed

4.2.6. DEVICE RECEIVER SENSITIVITY

EL_18 A high-speed capable device's Transmission Envelope Detector must be fast enough to allow the HS receiver to detect data transmission, active DLL lock, and detect the end of the SYNC field within 12 bit times.
Passed

EL_17 A high-speed capable device must implement a transmission envelope detector that does not indicate squelch (i.e. reliably receives packets) when a receiver exceeds 150mV differential amplitude.
Note: A waiver may be granted if the receiver indicates Squelch at +-50mV of 100mV differential amplitude. This is to compensate for the oscilloscope probe point away from the receiver pins.
Squelch:
134 mV
-138 mV
Passed

EL_16 A high-speed capable device must implement a transmission envelope detector that indicates squelch (i.e. never receives packets) when a receiver's input falls below 100mV differential amplitude.
Note: A waiver may be granted if the receiver's input falls below 100mV differential amplitude. This is to compensate for the oscilloscope probe point away from the receiver pins.
Squelch:
131 mV
-137 mV
Passed

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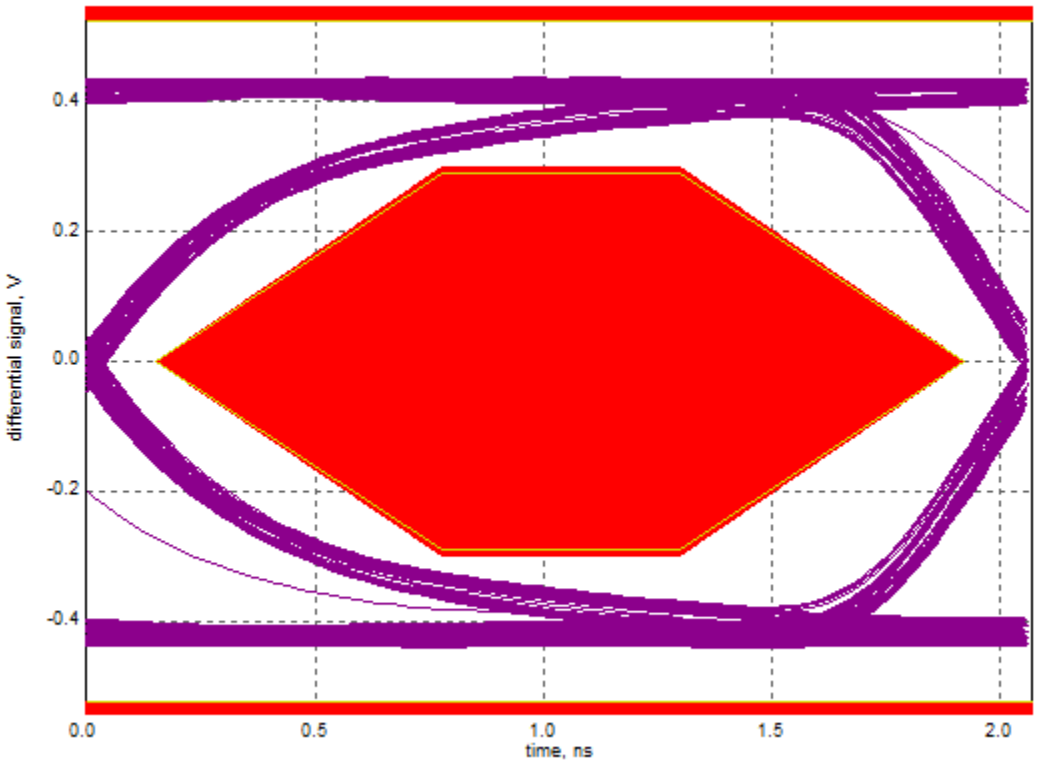
4.2.7. DOWNSTREAM HIGH SPEED SIGNAL QUALITY

The Freescale Semiconductors Inc. i.MX6DL passed the High Speed Downstream Signal Quality test.



High Speed Signal Eye

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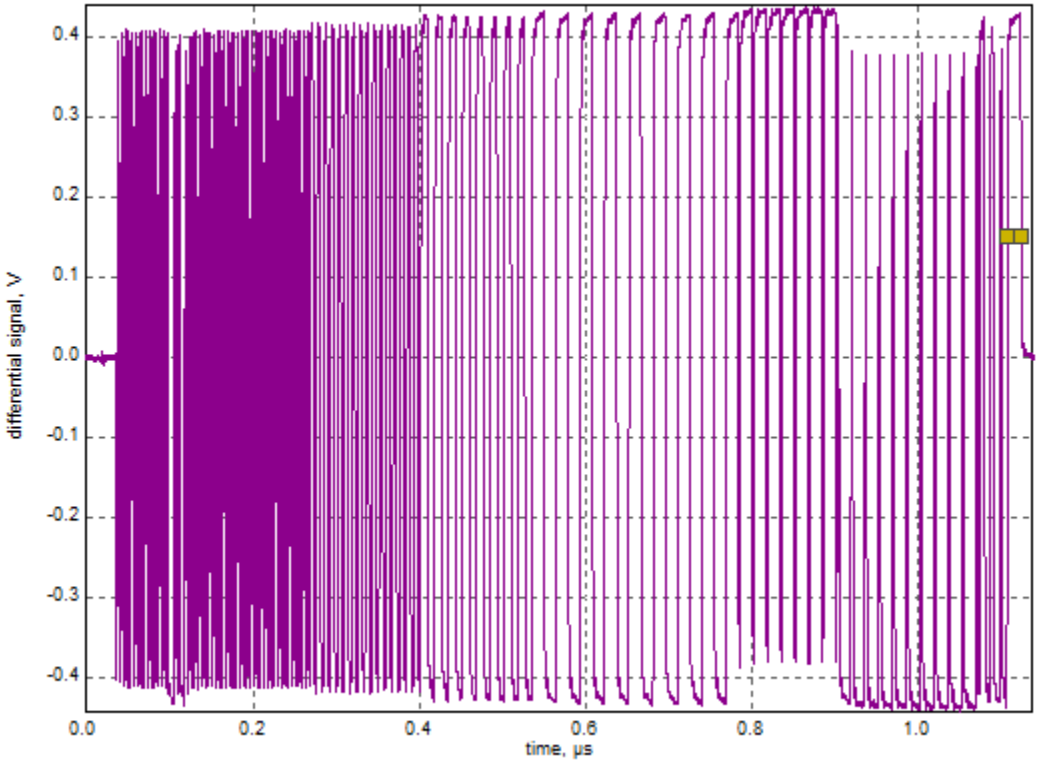

Date and Common Mode Voltage

- Overall result: pass!
- Signal eye:
  eye passes
- EOP width: 7.97 bits
  EOP width passes
- Measured signaling rate: 479.9752 MHz
  signal rate passes
- Edge Monotonicity: 0 mV
  Monotonic Edge passes
- Rising Edge Rate: 936.74 V/us (683.22 ps equivalent risetime)
  passes
- Falling Edge Rate: 940.45 V/us (680.52 ps equivalent falltime)
  passes

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Additional Information

- Consecutive jitter range: -34.346 ps to 48.171 ps, RMS jitter 19.917 ps
- Paired JK jitter range: -56.660 ps to 58.645 ps, RMS jitter 12.005 ps
- Paired KJ jitter range: -42.510 ps to 33.397 ps, RMS jitter 8.296 ps

EL_2 USB 2.0 High-Speed transmitter data rate must be 480 Mb/s +-0.05%
Data rate: 479.9752 MHz
passed

EL_3 USB 2.0 downstream facing port on a device without a captive cable must meet Template 1 transform waveform requirements measured at TP2
passed

EL_6 USB 2.0 HS Driver must have 10 to 90% differential rise and fall times of greater than 500 ps.
passed

EL_7 USB 2.0 HS Driver must have monotonic data transitions over the vertical openings specified in the appropriate eye pattern template.
passed

4.2.8. HOST PACKET PARAMETERS

EL_21 The SYNC field for all transmitted packets (not repeated packets) must begin with a 32-bit SYNC field. Since there is an internal hub it's allowed to truncate maximum 4 bits. SOF SYNC field and Data Packets SYNC both have 67.00 ns
Passed

EL_25 The EOP for all transmitted packets (except SOFs) must ben an 8-bit NRZ byte of 01111111 without bit stuffing. Since there is an internal hub it's allowed to add 4 random bits.
The EOP is 16.86 ns
Passed

EL_23 Host transmitting two packets in a row must have an inter-packet gap of at least 88 bit times and not more than 192 bit times.
Inter-packet gap internally of the host is: 266.00 ns
Passed

EL_22 When transmitting after receiving a packet, hosts and devices must provide an inter-packet gap at least 8 bit times and not more than 192 bit times. Since there is an internal hub an additional delay is allowed with a maximum of 292 bit.
Inter-packet gap respond of a host packet is 316.00 ns
Passed

EL_55 Host transmitting SOF packets must provide a 40-bit without bit stuffing where the first symbol of the EOP is a transition from the last data symbol. Since there is an internal hub it's allowed to add 4 random bits.
SOF EOP: 83.60 ns
Passed

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4.2.9. HOST CHIRP TIMING

EL_33 Downstream port start sending and alternating sequence of Chirp K's and Chirp J's within 100µs after the device Chirp K stops.
Measured value is 1.1 µs
Passed

EL_34 Downstream port Chirp K and Chirp J durations must be between 40µs and 60µs duration.
Measured value is Chirp K 50.10 µs - Chirp J 50.10 µs
Passed

EL_35 Downstream ports begin sending SOF's within 500µs and not sooner than 100µs from transmission of the last Chirp(J or K).
Measured value is: 300 µs
Passed

4.2.10. HOST SUSPEND/RESET/RESUME TIMING

EL_39 A device must support the Suspend state.
Passed

EL_41 After resuming a port, the host must begin sending SOF's within 3ms of the start of the idle state. When repeating the test of the SOD's never exceed the 3ms
The SOFs never exceed the 3ms when performing the test several times.
Passed

4.2.11. HOST TEST J/K, SE0_NAK

EL_8 When either D+ or D- are driven high, the output voltage must be 400mV +-10% when terminated with precision 45 Ohm resistors to the ground

	D+ Voltage (mV)	D- Voltage (mV)
J	426	8
K	8	435

Passed

EL_9 When either D+ or D- are not being driven, the output voltage must be 0V +-10mV when terminated with precision 45 Ohm resistors to the ground.

	Voltage (mV)
D+	1
D-	1

Passed

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4.3. DEVICE FRAMEWORK

The following tests were performed using the USB20CV & USB30CV test tool.

4.3.1. USB20CV CHAPTER 9

The Freescale Semiconductors Inc. i.MX6DL passed the Chapter 9 test of USB20CV.

Description	Full & High Speed
Vendor ID	15a2
Product ID	6f
CFG's	1
Interfaces	1
USB Spec.	2.0
Max. Power	2
Result	passed

4.3.2. USB30CV

The Freescale Semiconductors Inc. i.MX6DL passed the USB30CV Chapter 9 test on Renesas and Fresco Logic xHCI.

4.3.3. USBCV MSC TEST

The Freescale Semiconductors Inc. i.MX6DL passed the MSC test of USB20CV and USB30CV.

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4.4. POWER MEASUREMENTS DEVICE MODE

4.4.1. WINDOWS 7 SP1 POWER MEASUREMENT

The Freescale Semiconductors Inc. i.MX6DL passed the power measurement tests.

4.4.1.1. FULL SPEED MODE

Device State	Measurement	Status
Unconfigured State	0.08 mA	passed
Configured State	0.08 mA	passed
Operating State	0.12 mA	passed
Suspended State	80.00 µA	passed

4.4.1.2. HIGH SPEED MODE

Device State	Measurement	Status
Unconfigured State	0.08 mA	passed
Configured State	0.08 mA	passed
Operating State	0.13 mA	passed
Suspended State	80.00 µA	passed

4.5. BACK VOLTAGE

The Freescale Semiconductors Inc. i.MX6DL passed the back voltage tests.

	DC Voltage Before Enumeration	DC Voltage After Enumeration and Removal
Vbus	64 mV	64 mV
D+	0 mV	0 mV
D-	0 mV	0 mV

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4.6. GOLD TREE (INTEROPERABILITY)

For more information about the test guides used by Testronic Labs Belgium n.v., please see the procedure that can be found at http://compliance.usb.org.

4.6.1. WINDOWS 7 SP1 INTEROPERABILITY

The Freescale Semiconductors Inc. i.MX6DL passed the interoperability tests.

Test No.	Test description	Result
1	Enumeration and driver installation test on EHCI	passed
2	Remove External Power Supply	passed
3	DUT demonstrates correct using default drivers	passed
4	Update driver	n.a
5	Install Software	n.a
6	Demonstrates functionality with update driver and/or application	n.a
7	Interoperability (operates all the devices in Gold Tree)	passed
8	Hot Detach & Reattach	passed
9	Warm boot	passed
10	Inactive S1 Suspend (Remote wake-up test)	passed
11	Inactive S1 Resume (Remote wake-up test)	passed
12	Active S3 Suspend	passed
13	Active S3 Resume	passed
14	UHCI Root port test	passed
15	Active S4 Suspend(Hibernate)	passed
16	Active S4 Resume(Hibernate)	passed
17	Topology change UHCI	passed
18	Topology change OHCI	passed
19	Topology change XHCI	passed

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4.7. EMBEDDED HOST INTEROPERABILITY

The Freescale Semiconductors Inc. i.MX6DL passed the manual testing part (Chapter 7) of the USB On-The-Go and Embedded Host Automated Compliance Plan for the On-The-Go & Embedded Host Supplement Revision 2.0.

Test No.	Test Description	Result
7.3.1	Functionality B-device (specific TPL device(s))	n.a
7.3.2	Category Functionality B-device Device 1	passed
	Device 2 (composite)	passed
7.3.3	Boot test	passed
7.3.4	Legacy Speed Test	passed
7.3.5	Concurrent and Independently test	passed
7.3.6	A-UUT Unsupported device message Test	passed
	Low Speed Device	passed
	Full Speed Device	passed
	High Speed Device	passed
	Super Speed Device	passed
	Composite Device	passed
7.3.7	A-UUT Hub Error Message test	n.a
	Device behind Hub not enumerated	n.a
7.3.8	A-UUT Hub functionality test	passed
	High Speed Device	passed
	Full Speed Device	passed
7.3.9	A-UUT Hub maximum tier test	passed
7.3.10	A-UUT Hub concurrent and independent test	passed
7.3.11	A-UUT Bus powered hub power exceeded test	passed
7.3.12	A-UUT Maximum concurrently device exceed message test	n.a
7.3.13	A-UUT Suspend/Resume test	n.a
7.3.14	A-UUT Suspend Disconnect test	n.a
7.3.15	A-UUT Suspend Attach test	n.a
7.3.16	A-UUT Suspend Topology Change test	n.a
7.3.17	A-UUT Suspend Remote Wakeup test	n.a
7.3.18	OTH to OTG Test	n.a

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5. OTHER TESTRONIC LABS SERVICES

Testronic Labs, Your hardware test centre.

Testronic Labs operates as an independent Belgian based test centre for the validation and release of multimedia peripheral equipment and interfaces.
Testronic Labs offers a wide range of testing activities and has become a professional test center for numerous companies all over the world, a test house known for its quality of testing and its dynamic approach.

Thanks to the independence of the test laboraties, Testronic Labs is ideally placed to offer an objective, third party opinion on overall quality of the products in development.

Currently, Testronic Labs experience is located in the following application areas:
Services:

- Alpha Testing
- Beta Testing
- Pre-WHQL Testing
- Compatibility Testing
- Functionality Testing
- Localisation Testing
- Spec Compliance
- Consultancy

Technologies:

- Optical Storage Drives
- Firewire IEEE1394 Certification
- PC, MAC systems and peripherals
- USB
- USB On-The-Go
- Serial-ATA
- Ethernet
- DLNA
- DVB
- PCI-Express
- HDMI, DVI
- Bluetooth
- WIFI
- ...

Tools:

- Ch8ck tool
- Traffic Lab

Please visit our web site at http://www.testroniclabs.com for detailed information regarding Testronic Labs testing services.

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