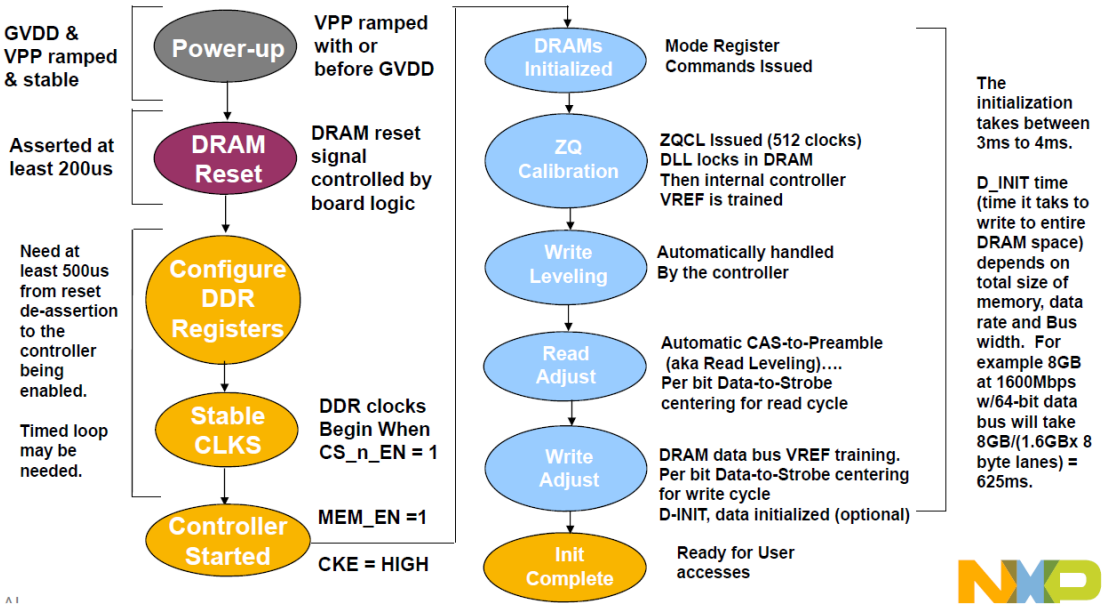
DDR Bringing up and validation with QCVS DDRv Tool

DDR4 Initialization Flow



DDR Bring up HW and SW checklist

DDR Bring up HW checklist:
Schematics review
Design checklist document
Layout/HW guideline application note AN5097
HW specs
Check all voltages: GVDD, VREF, VTT, AND VPP
Check input and output DDR clocks
Verify DRAM reset signal is matched to HRESET for UDIMM,
SoDIMM, and discrete DRAM. AN5097 appendix B.
Verify correct DRAM type strap
Verify DQ pin swapping is per allowed limitation
Have more than one board for bring up
Check for manufacturing/fabrication/assembly issues

DDR Bring up SW checklist:
Generate the setting via QCVS
Use SPD if available, otherwise Auto generation
Select the DDR data rate based on the measured output clock
RCW needs to be valid and correct
Enter MCK to DQS skews in the DDR wizard
Verify the DQn_MAP registers are correct

Verify all related errata are implemented

DDR Bringing up issues

Confirm it is not a DDR issue.

1. DDR_SDRAM_CFG[ECC_EN] is 1

ECC Enable. Note that uncorrectable read errors may cause an interrupt.
If this bit is set to 1, DDR_SDRAM_CFG[ACC_ECC_EN] must be set to 1 as well.
0b - No ECC errors are reported. No ECC interrupts are generated.
1b - ECC is enabled.

2. ERR_DETECT = 0x0

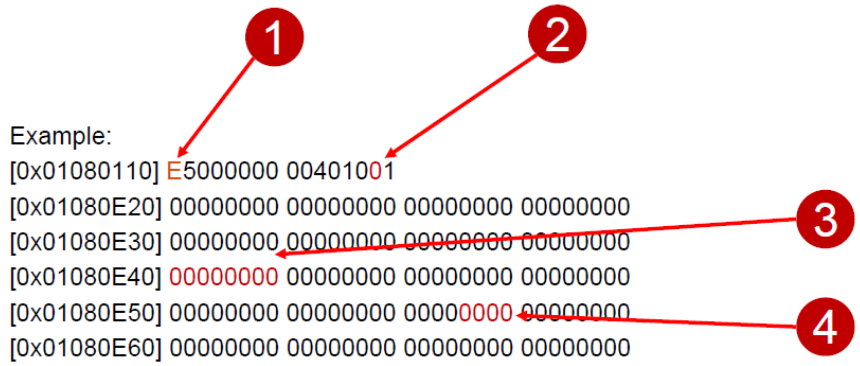
The memory error detect register stores the detection bits for multiple memory errors, single- and multiple-bit ECC errors, and memory select errors. It is a read/write register. A bit can be cleared by writing a one to the bit. System software can determine the type of memory error by examining the contents of this register. If an error is disabled with ERR_DISABLE, the corresponding error is never detected or captured in ERR_DETECT.

3. ERR_SBE[SBEC] = 0x0

Single-bit error counter. Indicates the number of single-bit errors detected and corrected since the last error report. If single-bit error reporting is enabled, an error is reported and an interrupt is generated when this value equals SBET. SBEC is automatically cleared when the threshold value is reached. This counter is only incremented when single-bit errors which are not automatically fixed by the controller are detected.

4. SDRAM_CFG_2[D_INIT] = 0x0

DRAM data initialization.
This bit is set by software, and it is cleared by hardware. If software sets this bit before the memory controller is enabled, the controller will automatically initialize DRAM after it is enabled. This bit will be automatically cleared by hardware once the initialization is completed. This data initialization bit should only be set when the controller is idle.
0b - There is not data initialization in progress, and no data initialization is scheduled
1b - The memory controller will initialize memory once it is enabled. This bit will remain asserted until the initialization is complete. The value in DDR_DATA_INIT register will be used to initialize memory.



Memory controller initialization failure.

1) ERR_DETECT[ACE] is set

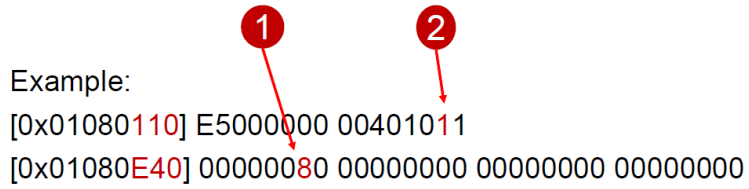
   Automatic calibration error.

   This bit is cleared by software writing a 1.

   0b - An automatic calibration error has not been detected.

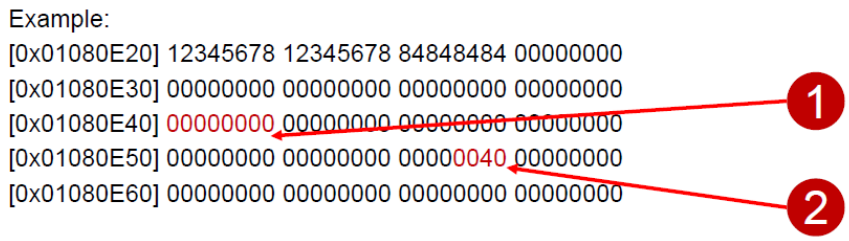
   1b - An automatic calibration error has been detected.

2) SDRAM_CFG_2[D_INIT] does not clear



Memory controller ECC errors

1. ERR_DETECT<>0
2. ERR_SBE[SBEC]<>0



Registers dump via CCS

Open a CCS window from C:\Freescale\CW4NET_v2020.06\Common\CCS\bin\ccs.exe, connect CodeWarrior TAP to PC through USB or Ethernet connection. In CCS window, type the following command.

(for LS2088)

delete all

config cc cwtap

ccs::config_chain {ls2085a dap}

display ccs::read_mem 326 0x1080000 4 0 1024

ccs::write_mem 326 0x1080FB0 4 0 0x10000000

display ccs::read_mem 326 0x1080000 4 0 1024

(for LS1088)

delete all

config cc cwtap

ccs::config_chain {ls1088a dap}

display ccs::read_mem 119 0x1080000 4 0 1024

ccs::write_mem 119 0x1080FB0 4 0 0x10000000

display ccs::read_mem 119 0x1080000 4 0 1024

(for LS1043 or LS1046)

delete all
config cc cwtap
ccs::config_chain {ls1043a dap sap2}
display ccs::read_mem 32 0x1080000 4 0 1024
ccs::write_mem 32 0x1080FB0 4 0 0x10000000
display ccs::read_mem 32 0x1080000 4 0 1024

(for LS1021A)
delete all
config cc cwtap
ccs::config_chain {ls1020a dap sap2}
display ccs::read_mem 17 0x1080000 4 0 1024
ccs::write_mem 17 0x1080FB0 4 0 0x10000000
display ccs::read_mem 17 0x1080000 4 0 1024

(for T1)
delete all
config cc cwtap
ccs::config_chain t1040
display ccs::read_mem 0 0x30000 0x8000 4 2 1024
ccs::write_mem 0 0x30000 0x8FB0 4 2 0x10000000
display ccs::read_mem 0 0x30000 0x8000 4 2 1024

Configuration and Validation via QCVS tool

Two general types of registers to be configured in the memory controller:
First register type are set to the DRAM related parameter values, that are provided via SPD or DRAM datasheet. Over 100 register fields fall under this category.
Second register type are the Non-SPD values that are set based on customer's application. For example:
− On-die-termination (ODT) settings for DRAM and controller
− Driver impedance setting for DRAM and controller
− Clock adjust value selection
− Write leveling start value (WRLVL_START)

Use QCVS DDRv tool configure and optimize the DDR interface.
1. Use the tool to generate the DDR register settings
  Select the SPD option in configuration wizard when DIMM is used
  Select Auto Configuration when Discrete DRAM is used
2. Optimize the DDR register setting on your QorIQ board
Run the clock centering test
Optimize the ODT and drive strength for read and write

DDR Interface ADD/CMND Bus Margins via QCVS Tool
Clock signal is stepped cross the address bus eye unit

interval and tool regenerate a pass/fail address bus eye.

In the example below the address eye is passing from 1/8 clk to 7/8 of clock. This is 80% of open eye from maximum available address bus.

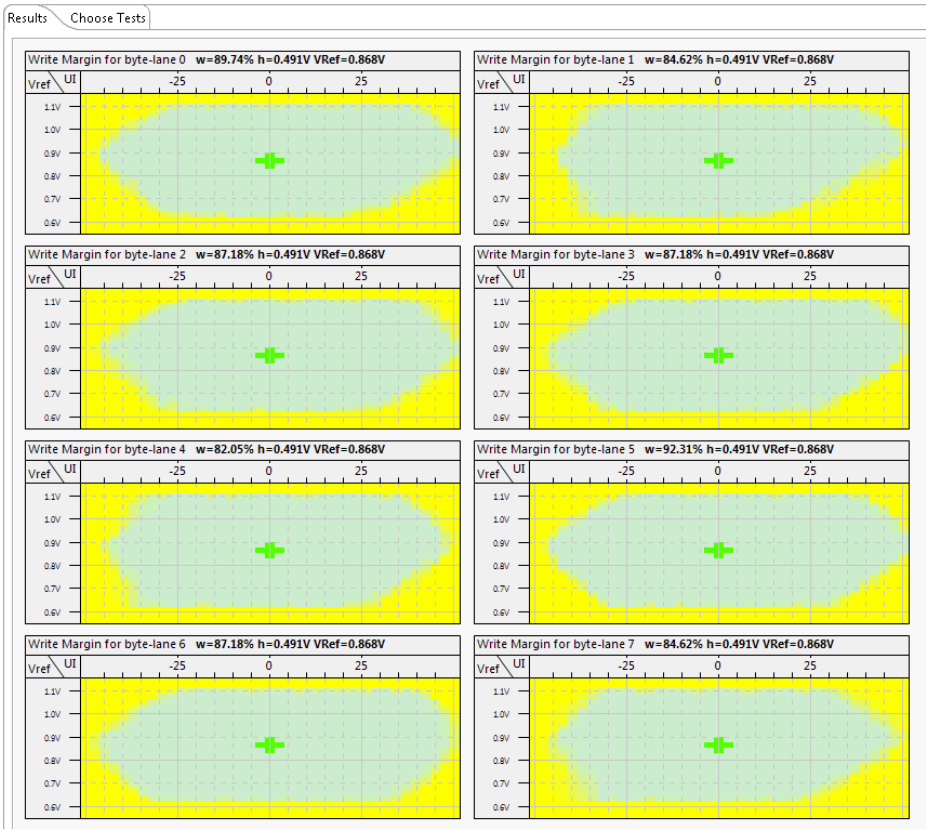
CLK_ADJ																
0	1/16	1/8	3/16	1/4	5/16	3/8	7/16	1/2	9/16	5/8	11/16	3/4	13/16	7/8	15/16	1
0/1	0/1	1/1	1/1	1/1	1/1	1/1	1/1	1/1	1/1	1/1	1/1	1/1	1/1	1/1	0/1	0/1

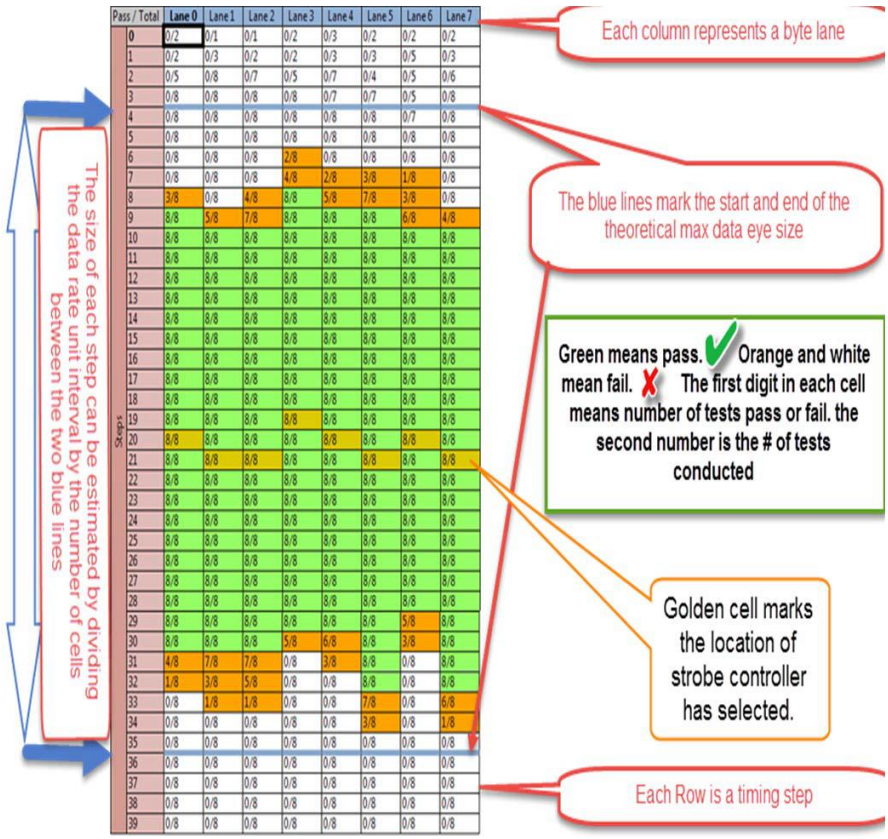
Determine WRLVL margin per byte lane

WRLVL_START	Pass / Total	Lane 0	Lane 1	Lane 2	Lane 3	Lane 4	Lane 5	Lane 6	Lane 7	Lane 8 (ECC)
	1/8 clocks									
	1/4 clocks									
	3/8 clocks									
	1/2 clocks	1/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1
	5/8 clocks	1/1	1/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1
	3/4 clocks	1/1	1/1	1/1	1/1	0/1	0/1	0/1	0/1	0/1
	7/8 clocks	1/1	1/1	1/1	1/1	0/1	0/1	0/1	0/1	1/1
	1 clocks	1/1	1/1	1/1	1/1	1/1	0/1	0/1	0/1	1/1
	9/8 clocks	1/1	1/1	1/1	1/1	1/1	1/1	0/1	0/1	1/1
	5/4 clocks	1/1	1/1	1/1	1/1	1/1	1/1	1/1	0/1	1/1
	11/8 clocks	1/1	1/1	1/1	1/1	1/1	1/1	1/1	1/1	1/1
	3/2 clocks	0/1	1/1	1/1	1/1	1/1	1/1	1/1	1/1	1/1
	13/8 clocks	0/1	0/1	1/1	1/1	1/1	1/1	1/1	1/1	1/1
	7/4 clocks	0/1	0/1	0/1	0/1	1/1	1/1	1/1	1/1	1/1
	15/8 clocks	0/1	0/1	0/1	0/1	1/1	1/1	1/1	1/1	0/1
	2 clocks	0/1	0/1	0/1	0/1	0/1	1/1	1/1	1/1	0/1
	17/8 clocks	0/1	0/1	0/1	0/1	0/1	0/1	1/1	1/1	0/1
	9/4 clocks	0/1	0/1	0/1	0/1	0/1	0/1	0/1	1/1	0/1

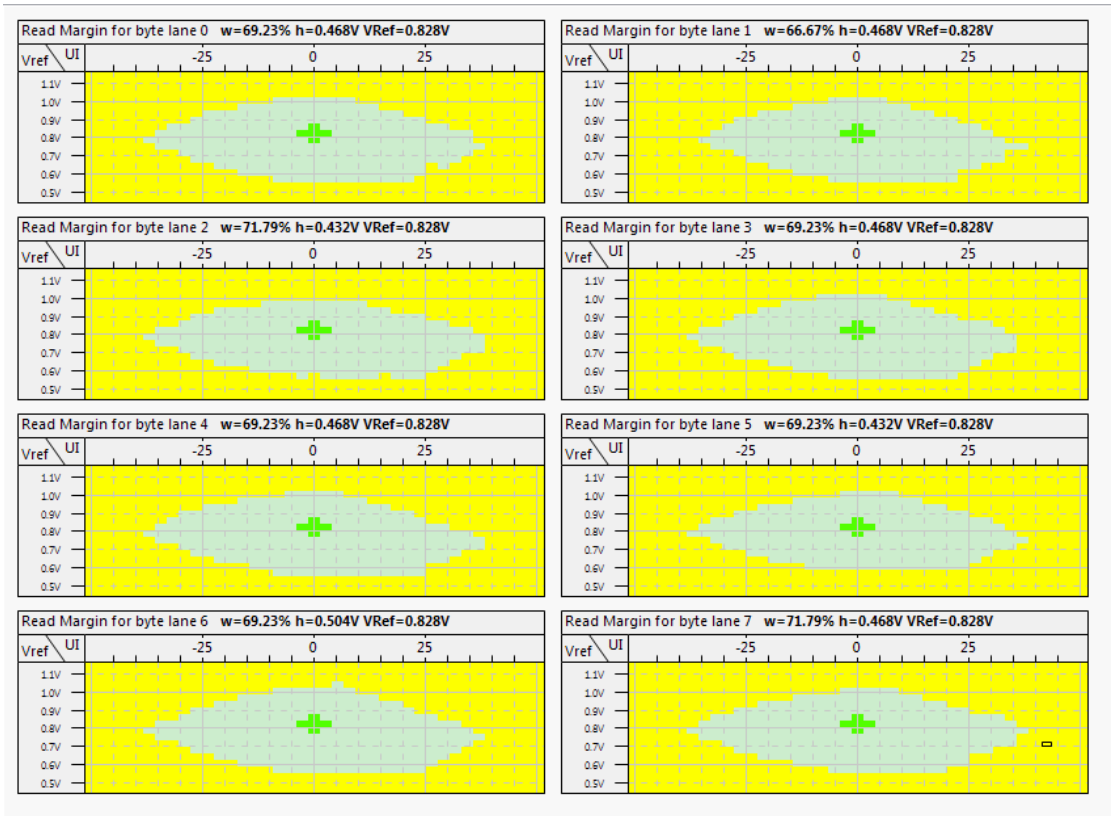
Write level margin table provides the reconstruction pass fail margins for each byte lane.

Write Margin Table in QCVS Tool





Read Margin Table in QCVS Tool



- Blue line indicates the beginning and end of the theoretical data eye
- Estimated timing for each step = theoretical-data-eye / number of steps

On the left are the data eyes for each byte lane. This is available for LS2, LS1088, and LS1046.