Features
- Saturated Output Power: 24 dBm
- Gain: 12 dB
- Input Return Loss: >15 dB
- Output Return Loss: >15 dB
- Reverse Isolation: >30 dB
- Dimension: 1800 x 2000 x 50 µm
- RoHS* Compliant
- Bare Die

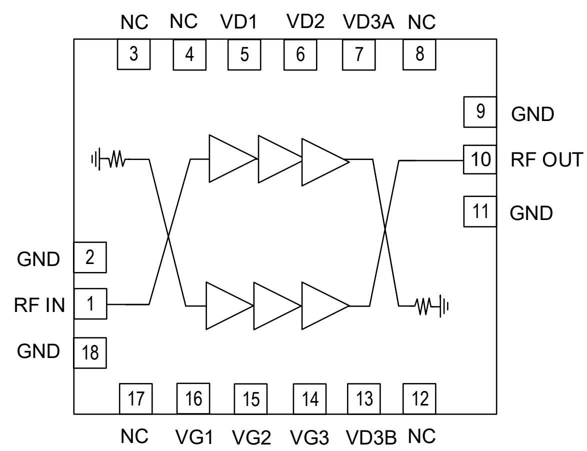
Applications
- Point-to-Point Communications / Short Haul
- High Resolution Radar
- Sensing
- Narrow bandwidth Millimeter Wave Imaging

Description
The MAAP-011199-DIE is a balanced 3 stage GaAs pHEMT MMIC power amplifier. The device operates from 80 to 100 GHz and provides typically 24 dBm of output power. The power amplifier's balanced architecture results in excellent input and output match to 50 Ω across the entire 80 - 100 GHz frequency band and the multi-stage design provides high gain of 12 dB.

Ordering Information

Part Number	Package
MAAP-011199-DIE	Die in Gel Pack

Functional Schematic



Pad Configuration[1]

Pad #	Function
1	RF IN
2, 9, 11, 18	GND
3, 4, 8, 12, 17	NC[2]
5	VD1
6	VD2
7	VD3A
10	RF OUT
13	VD3B
14	VG3
15	VG2
16	VG1

1. Backside of die must be connected to RF, DC and thermal ground.
2. These pins do not need to be connected. They are grounded on the MMIC.

* Restrictions on Hazardous Substances, compliant to current RoHS EU directive.

Electrical Specifications[3]: Freq. = 80 - 100 GHz, T_A = 25°C, V_D = 4 V, Z_0 = 50 Ω

Parameter	Freq.	Units	Min.	Typ.	Max.
Gain	80 GHz 85 GHz 90 GHz 95 GHz 100 GHz	dB	7.5 9.0 9.0 9.0 9.0	10.5 12.0 12.0 12.0 12.0	—
Input Return Loss	—	dB	—	15	—
Output Return Loss	—	dB	—	15	—
Quiescent Drain Current	—	mA	—	400	—
P_{1dB}	—	dBm	—	22	—
Saturated Output Power	—	dBm	—	24	—

3. Quiescent DC Bias: I_D1 = 100 mA, I_D2 = 100 mA, I_D3 = 200 mA. Total DC power = 1.6 W.

Absolute Maximum Ratings[4,5,6,7]

Parameter	Absolute Maximum
Input Power	17 dBm
Drain Voltage	4.3 V
Drain Current	670 mA
Gate Bias Voltage (V_G1,2,3)	-1.5 V < V_G < 0.3 V
Storage Temperature	-55°C to +150°C
Operating Temperature	-40°C to +85°C
Junction Temperature[7,8]	150°C

4. Exceeding any one or combination of these limits may cause permanent damage to this device.
5. MACOM does not recommend sustained operation near these survivability limits.
6. Operating at nominal conditions with $T_J \leq$ +150°C will ensure MTTF > 1 x 10^6 hours.
7. Junction Temperature (T_J) = T_C + Θ_{JC} * ((V * I) - (P_{OUT} - P_{IN}))
   Typical thermal resistance (Θjc) = 22.5°C/W.
   a) For T_C = +85°C, IDSQ = 400 mA, defined as backside of die.
   T_J = 132°C @ 4 V, 580 mA, P_{OUT} = 24 dBm, P_{IN} = 12 dBm, @ 94 GHz.

Handling Procedures

Please observe the following precautions to avoid damage:

Static Sensitivity

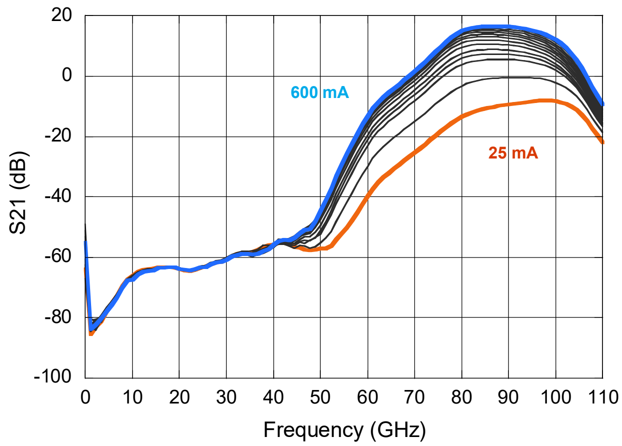
These electronic devices are sensitive to electrostatic discharge (ESD) and can be damaged by static electricity. Proper ESD control techniques should be used when handling these devices. This device is classified as Class 1C for HBM test and Class II for CDM test.

Calibration Plane

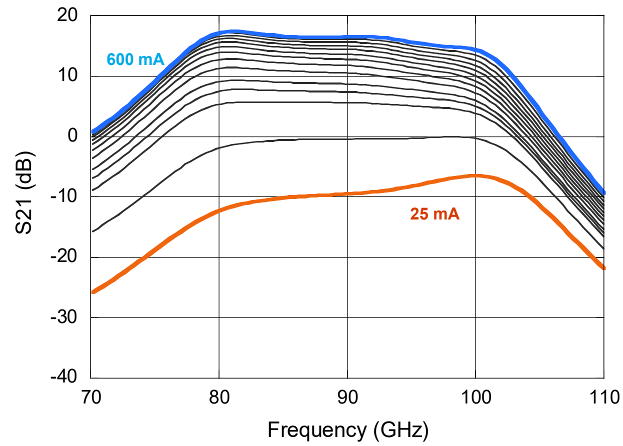
All data was measured in a 50 Ω environment with an ISS calibration to the probe tip.

Typical Performance Curves @ +25°C, V_D = 4 V, Z_0 = 50 Ω (I_D = 25, 50, 100, 150, 200, 250, 300, 350, 400, 450, 500, 550, 600 mA)

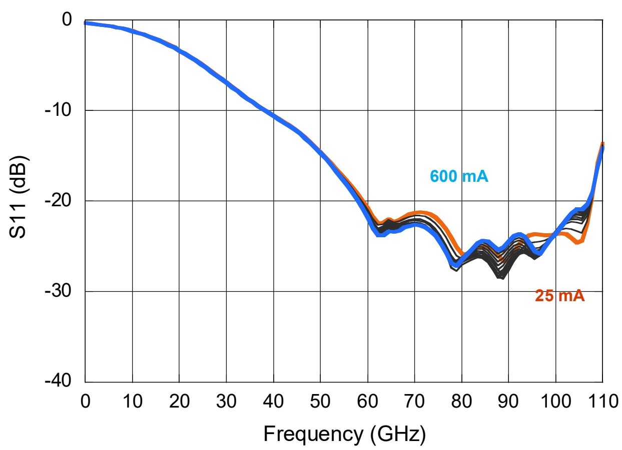
Gain



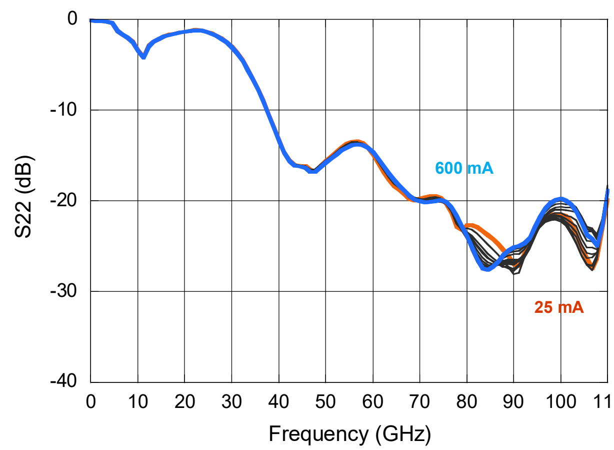
Gain 70 - 110 GHz



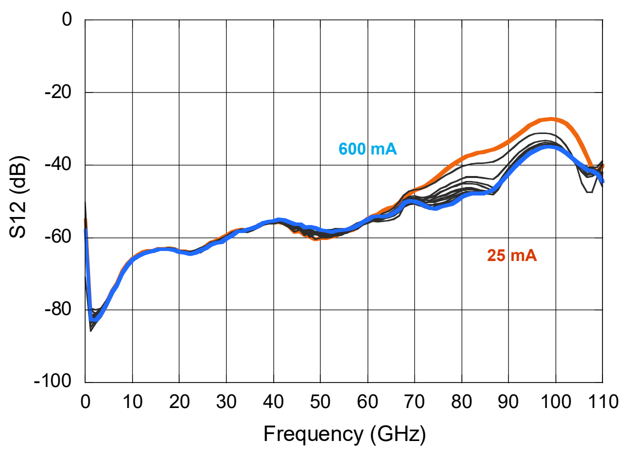
Input Return Loss



Output Return Loss

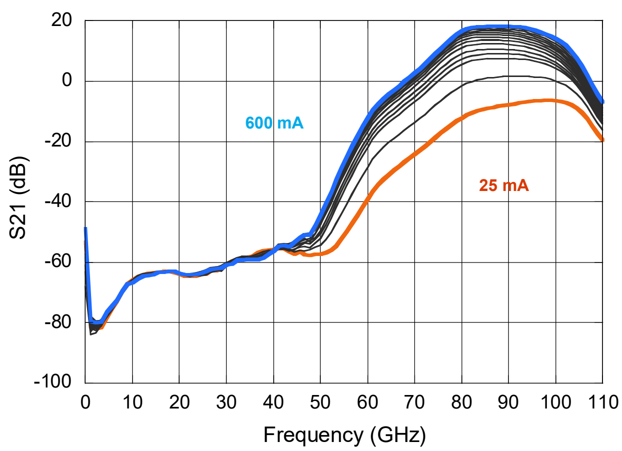


Reverse Isolation

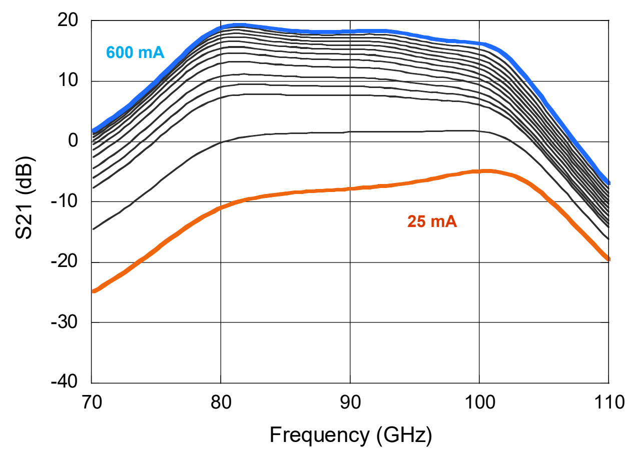


Typical Performance Curves @ -40°C, V_D = 4 V, Z_0 = 50 Ω (I_D = 25, 50, 100, 150, 200, 250, 300, 350, 400, 450, 500, 550, 600 mA)

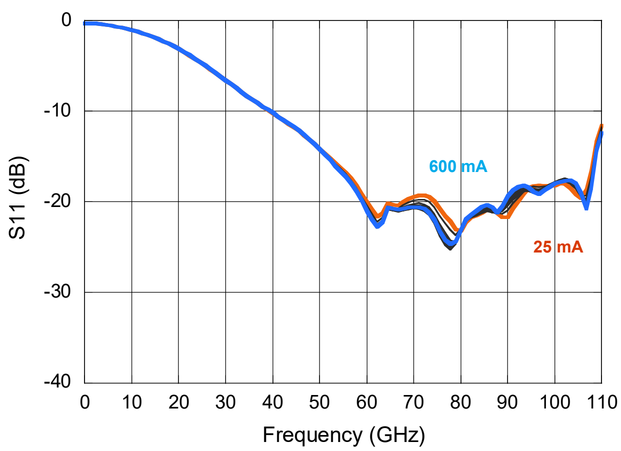
Gain



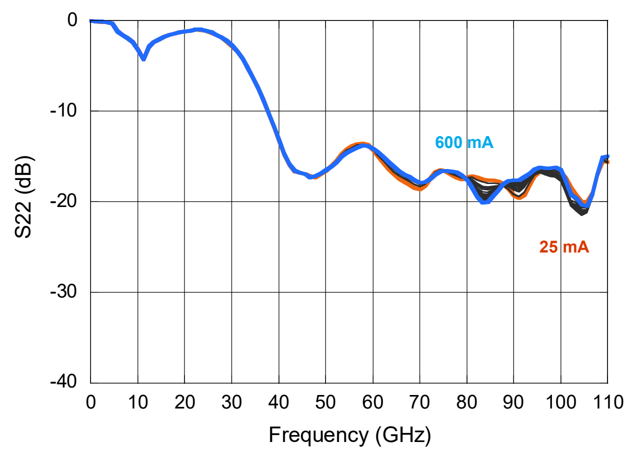
Gain 70 - 110 GHz



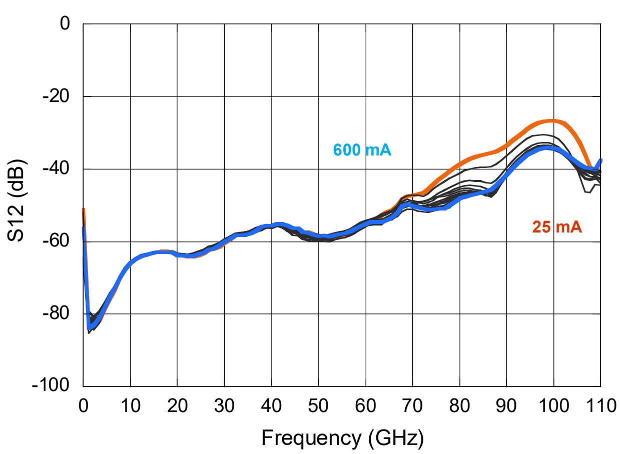
Input Return Loss



Output Return Loss

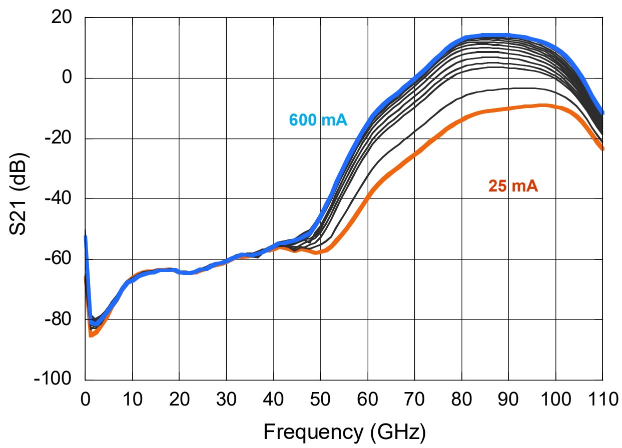


Reverse Isolation

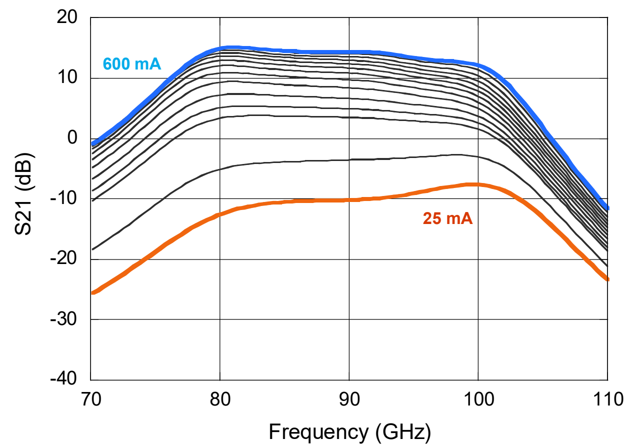


Typical Performance Curves @ +85°C, V_D = 4 V, Z_0 = 50 Ω (I_D = 25, 50, 100, 150, 200, 250, 300, 350, 400, 450, 500, 550, 600 mA)

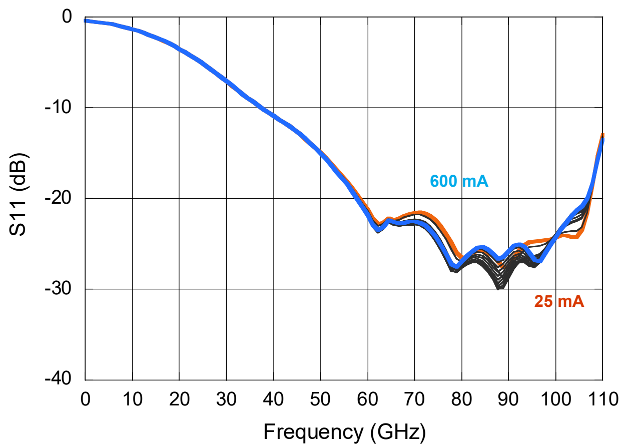
Gain



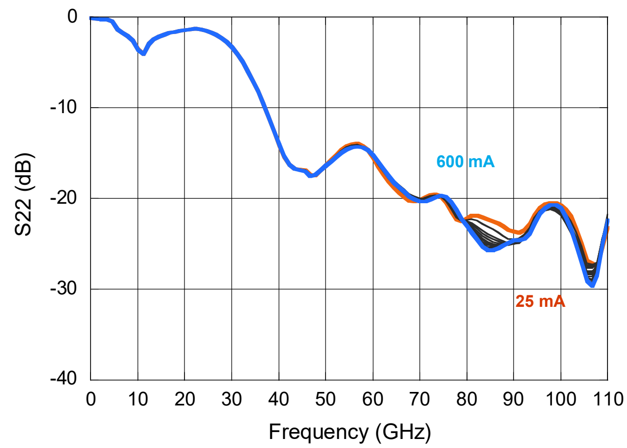
Gain 70 - 110 GHz



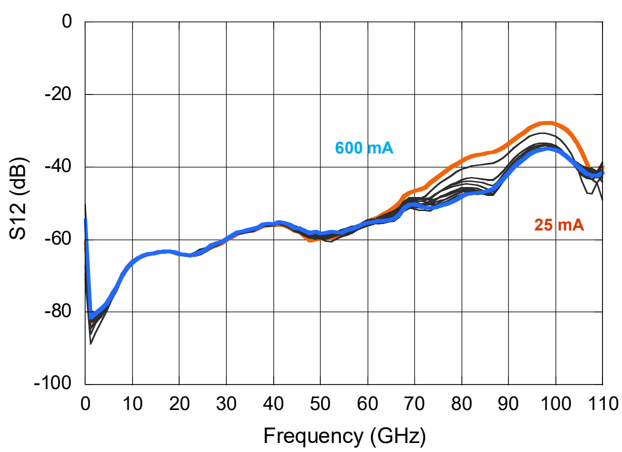
Input Return Loss



Output Return Loss

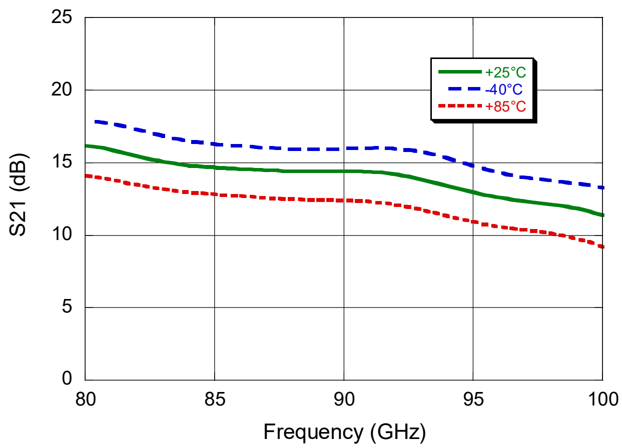


Reverse Isolation

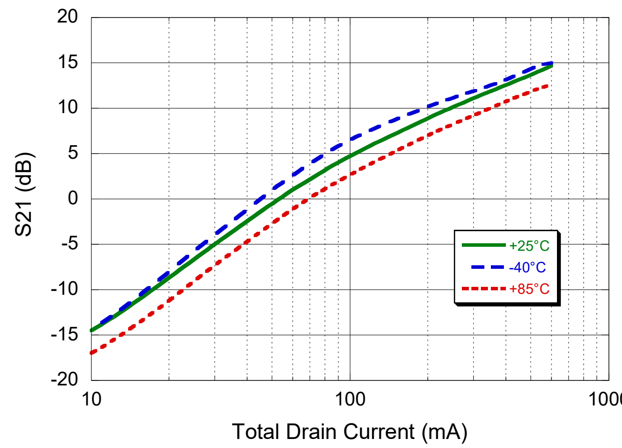


Typical Performance Curves V_D = 4 V, Z_0 = 50 Ω

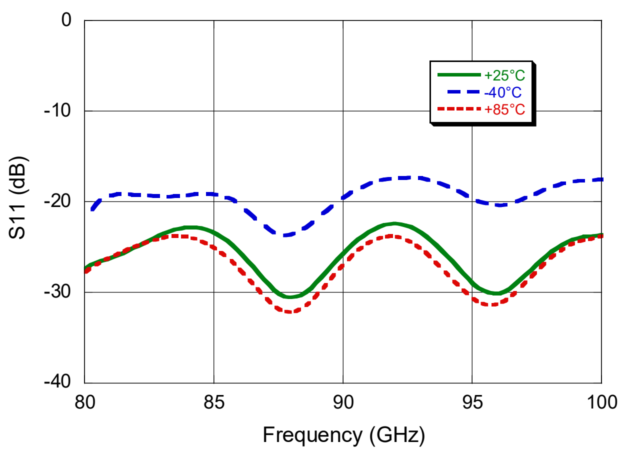
Gain vs. Frequency @ 400 mA



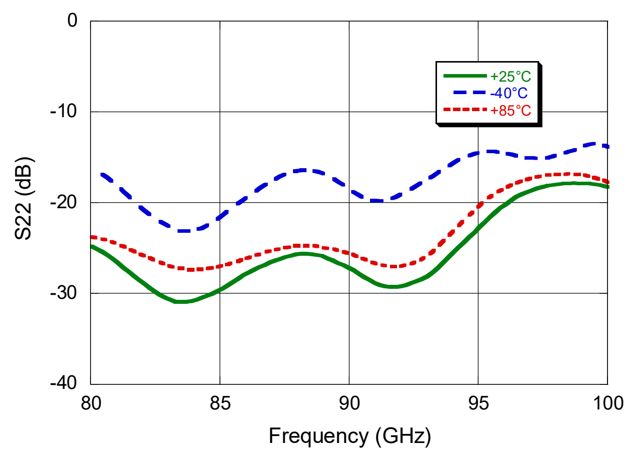
Gain vs. Drain Current @ 94 GHz



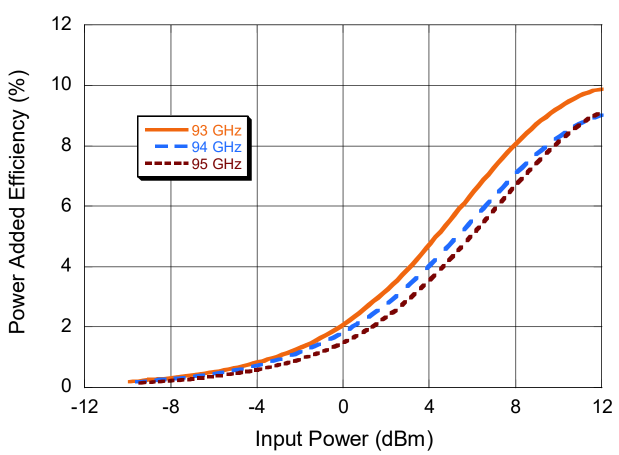
Input Return Loss vs. Frequency @ 400 mA



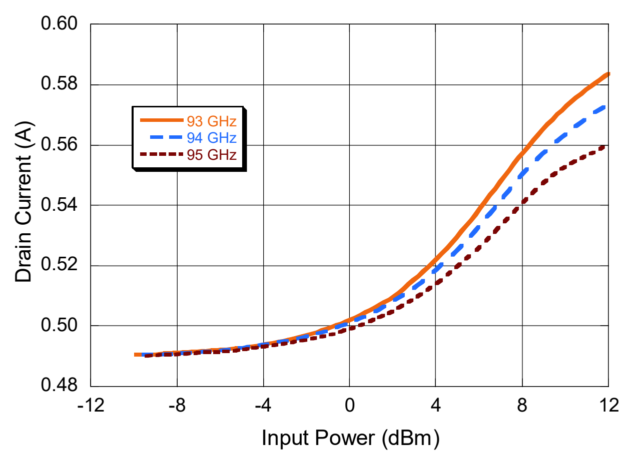
Output Return Loss vs. Frequency @ 400 mA



PAE vs. Input Power @ 25 ºC



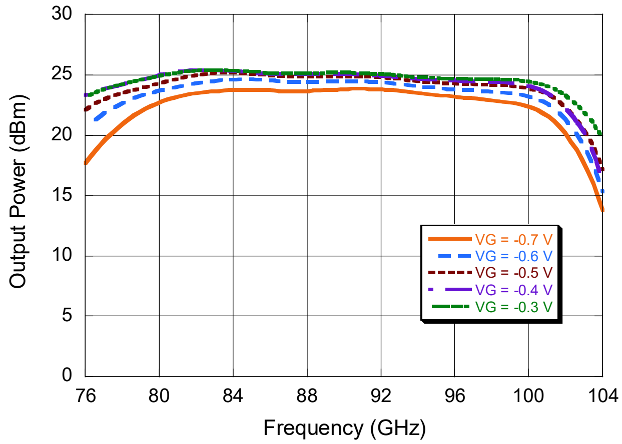
Drain Current vs. Input Power @ 25 ºC



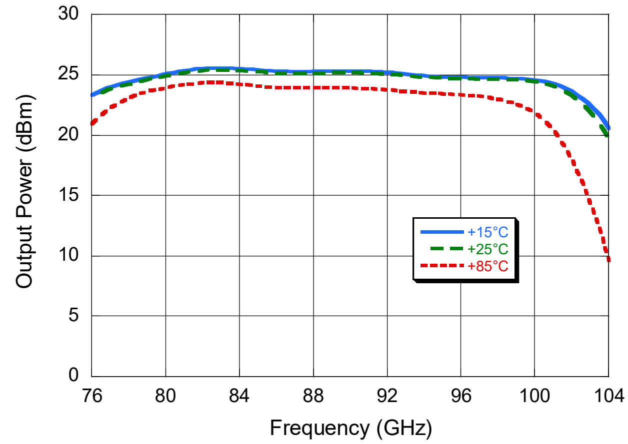
Typical Performance Curves V_D = 4 V, Z_0 = 50 Ω

P

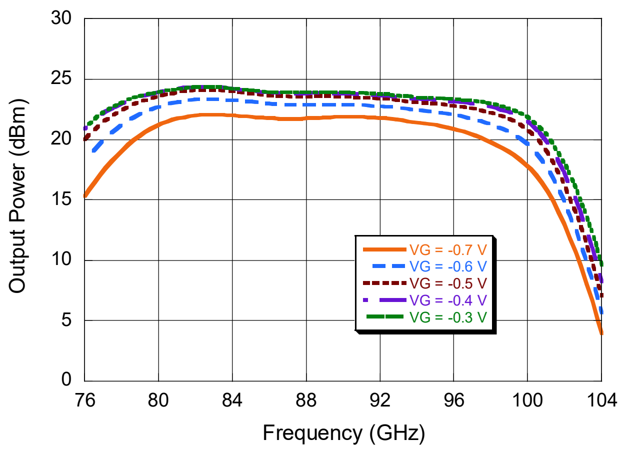
P_{SAT} vs. Frequency over Gate Voltage @ +25°C



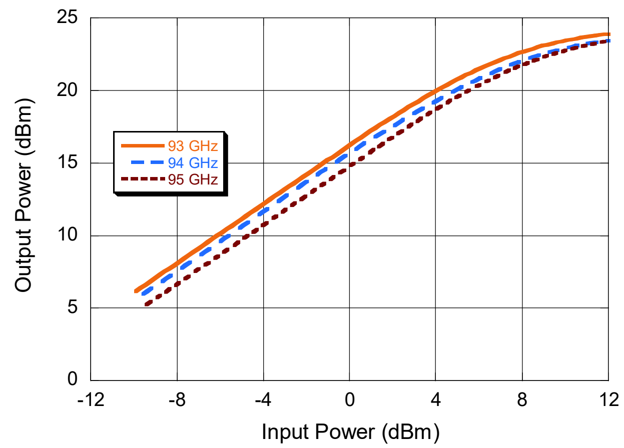
P_{SAT} vs. Frequency over Backside Temp. @ Vg = -0.3 V



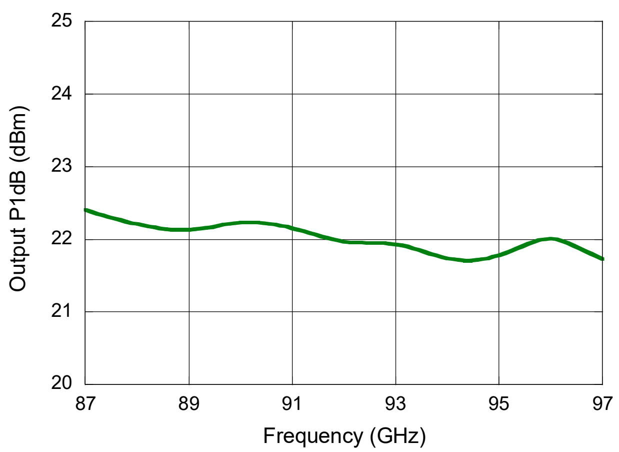
P_{SAT} vs. Frequency over Gate Voltage @ +85°C



Output Power vs. Input Power

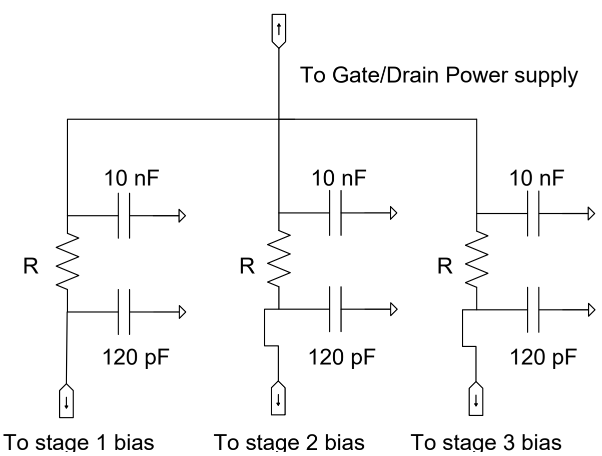


Output P1dB vs. Frequency



App Note [1] Biasing -
All gates should be pinched-off (V_G < -1 V) before applying drain voltage (V_D = 4 V). Then the gate voltages can be increased until the desired quiescent drain current is reached in each stage. The recommended quiescent bias is V_D = 4 V, I_D1 = 100 mA, I_D2 = 100 mA, and I_D3 = 200 mA. The performance in this datasheet has been measured with fixed gate voltage and no drain current regulation under large signal operation. It is also possible to regulate the drain current dynamically, to limit the DC power dissipation under RF drive. To turn off the device, the turn on bias sequence should be followed in reverse.

App Note [2] Bias Arrangement -
Each DC pin (V_{D1}, V_{D2}, V_{D3A}, V_{D3B}, and V_{G1}, V_{G2}, V_{G3}) needs to have bypass capacitance (120 pF and 10 nF) mounted as close to the MMIC as possible.



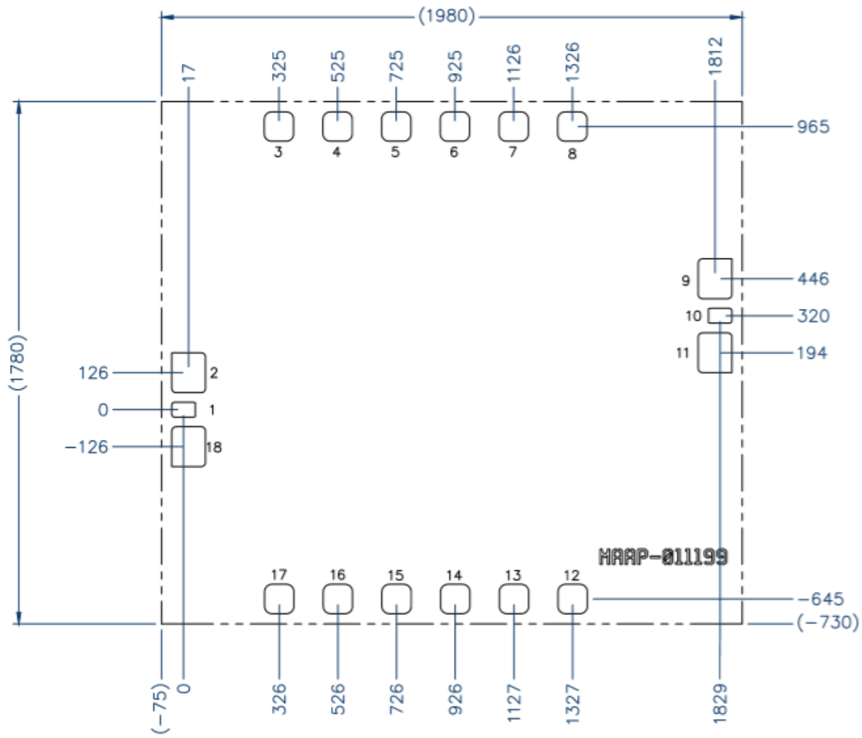
App Note [3] Common Gates and Drains -
When biasing the device with only a single gate or drain source additional isolation is required. On the gate side a 10 Ω resistor should be placed in series and tied together in a star to a common supply. The drain side resistance should be reduced to less than 5 Ω to minimize any voltage drop across the resistor. Suitable bias pass capacitance should still be applied to each stage as per App Note [2].

App Note [4] Handling the Die -
This MMIC has fragile exposed airbridges on its surface and must be handled on the edges only using a vacuum collet or suitable tweezers. Do not touch the surface of the chip with a vacuum collet, tweezers, or fingers.

App Note [5] Die Attach -
For mounting the die either an electrically conductive epoxy, or an AuSn eutectic preform can be used.

If using eutectic, an 80% Au/20% Sn preform is recommended. If using epoxy, a high thermal conductivity epoxy is required and a silver sintering type epoxy is recommended.

Die Outline



Unless otherwise specified, all dimensions shown are µm, with a tolerance of ± 5 µm.
Die thickness is 50 µm ± 10 µm.
Bondpad backside metallization: Gold
Die size reflects final dimensions.

Bond Pad Dimensions (µm)

Pad #	X	Y	Pin Label
1	80	51	RF IN
2	100	100	GND
3, 4, 8, 12, 17	100	100	NC[2]
5	92	142	VD1
6	92	142	VD2
7	92	92	VD3A
9	115	136	GND
10	80	51	RF OUT
11	115	136	GND
13	100	100	VD3B
14	100	100	VG3
15	100	100	VG2
16	100	100	VG1
18	115	136	GND