

Cover page

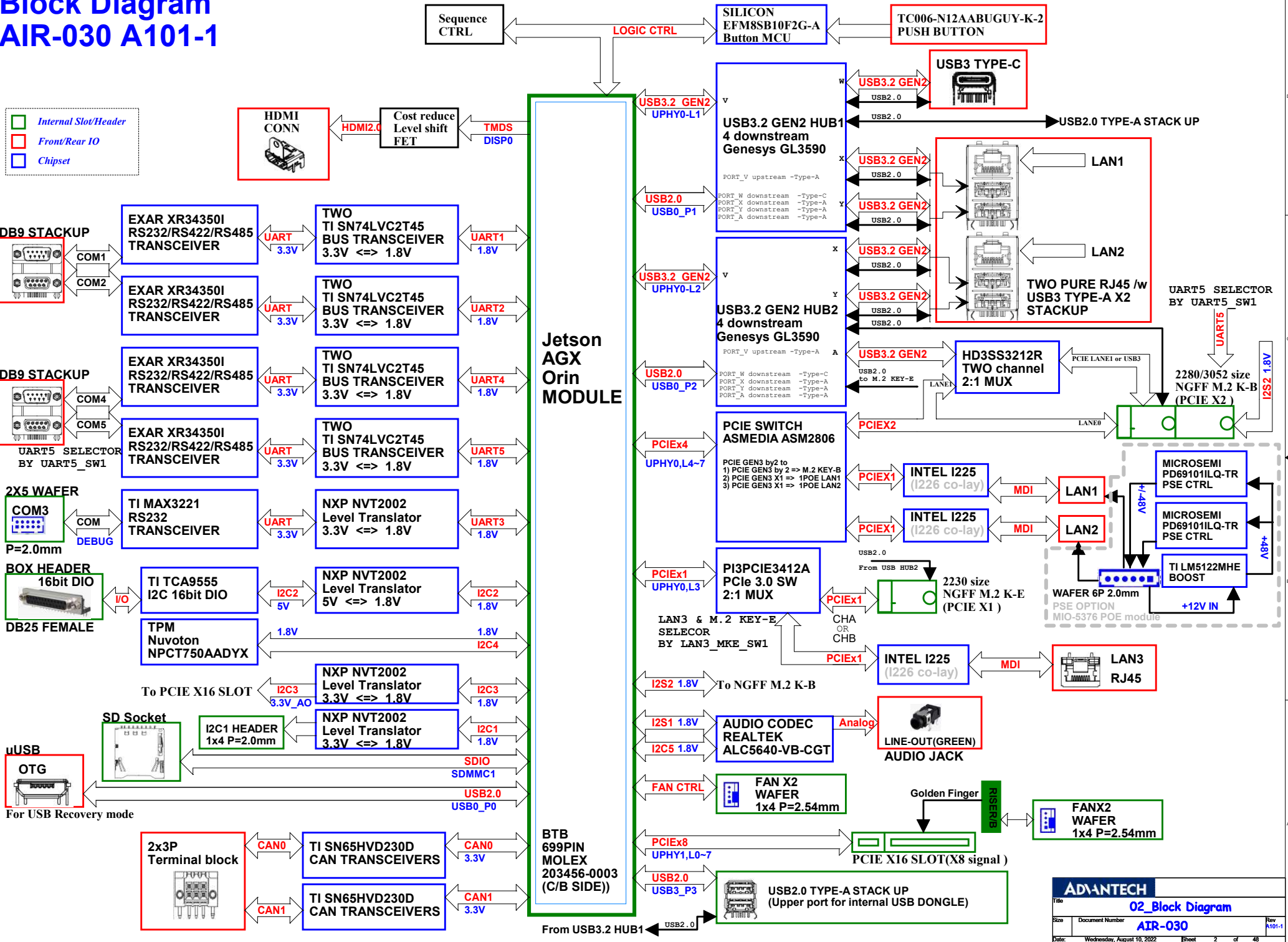
Model Name: AIR-030

Version:	A101-1	PCB P/N:	19A60003000-01	Update Date:	2022/08/04
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Block Diagram AIR-030 A101-1

- Internal Slot/Header
- Front/Rear IO
- Chipset



AIR-030 config function #1

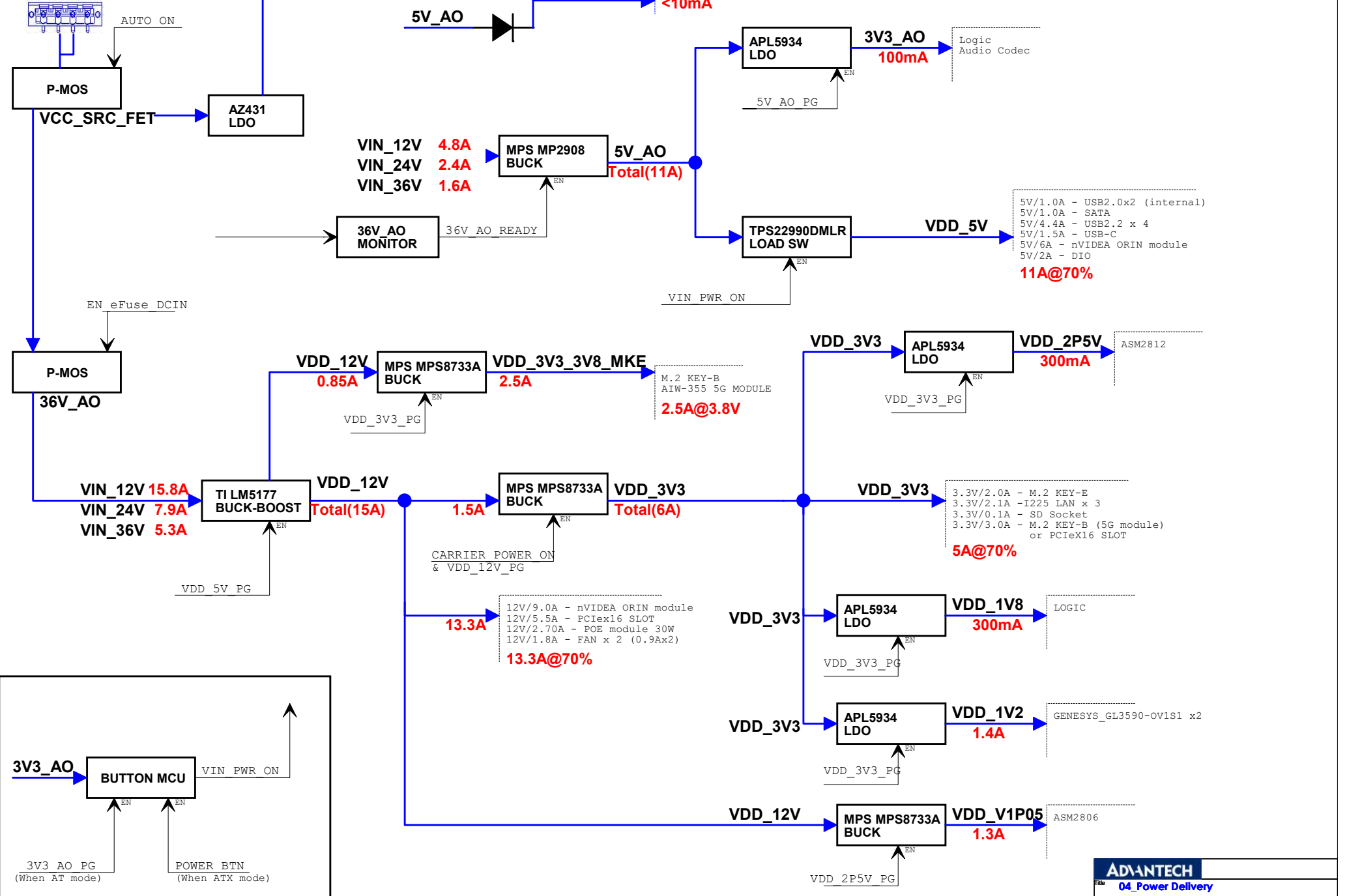
PCIE CLOCK MAP

Pin #	Module Pin Name	SoC Signal	Usage/Description
E14	PEX_CLK0_N	SF_PCIE7_CLK_N	PCIe output Reference Clock for controller
E15	PEX_CLK0_P	SF_PCIE7_CLK_P	#7.
F17	PEX_CLK1_N	SF_PCIE0_CLK_N	PCIe output Reference Clock for controller
F16	PEX_CLK1_P	SF_PCIE0_CLK_P	#0.
E22	PEX_CLK4_N	SF_PCIE4_CLK_N	PCIe output Reference Clock for controller
E23	PEX_CLK4_P	SF_PCIE4_CLK_P	#4.
F25	PEX_CLK5_N	SF_PCIE5_CLK_N	PCIe output Reference Clock for controller
F24	PEX_CLK5_P	SF_PCIE5_CLK_P	#5.
D48	PEX_CLK6_N	SF_PCIE1_CLK_N	PCIe output Reference Clock for controller
D49	PEX_CLK6_P	SF_PCIE1_CLK_P	#1.
E11	PEX_C0_CLKREQ_N	GP187_PCIE7_CLKREQ_N	PCIe Clock Request for controller #7. 47Kohm pull-up to 3.3V on module
D9	PEX_C1_CLKREQ_N	GP175_PCIE0_CLKREQ_N	PCIe Clock Request for controller #0. 47Kohm pull-up to 3.3V on module
G8	PEX_C4_CLKREQ_N	GP183_PCIE4_CLKREQ_N	PCIe Clock Request for controller #4. 47Kohm pull-up to 3.3V on module
C8	PEX_C5_CLKREQ_N	GP210_PCIE5_CLKREQ_N	PCIe Clock Request for controller #5. 47Kohm pull-up to 3.3V on module
B37	PEX_C7_CLKREQ_N	GP177_PCIE1_CLKREQ_N	PCIe Clock Request for controller #1. 47Kohm pull-up to 3.3V on module
D10	PEX_C0_RST_N	GP188_PCIE7_RST_N	PCIe Reset for controller #7. 47Kohm pull-up to 3.3V on module
B9	PEX_C1_RST_N	GP176_PCIE0_RST_N	PCIe Reset for controller #0.
J9	PEX_C4_RST_N	GP184_PCIE4_RST_N	PCIe Reset for controller #4. 47Kohm pull-up to 3.3V on module
H10	PEX_C5_RST_N	GP211_PCIE5_RST_N	PCIe Reset for controller #5. 47Kohm pull-up to 3.3V on module
B36	PEX_C7_RST_N	GP178_PCIE1_RST_N	PCIe Reset for controller #1. 47Kohm pull-up to 3.3V on module

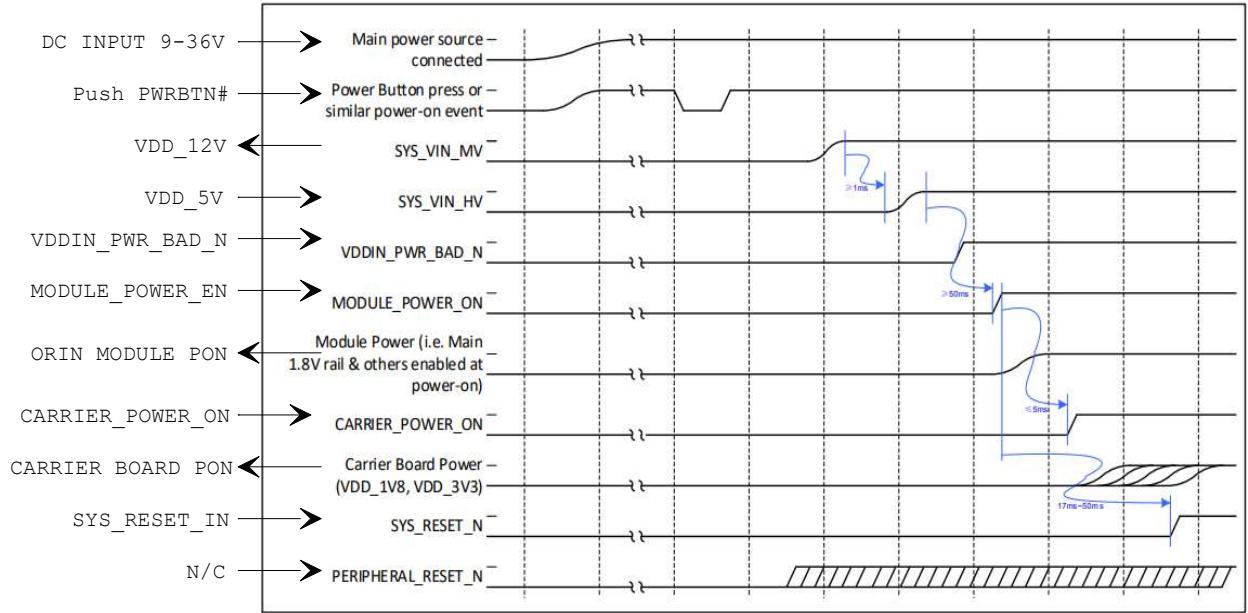
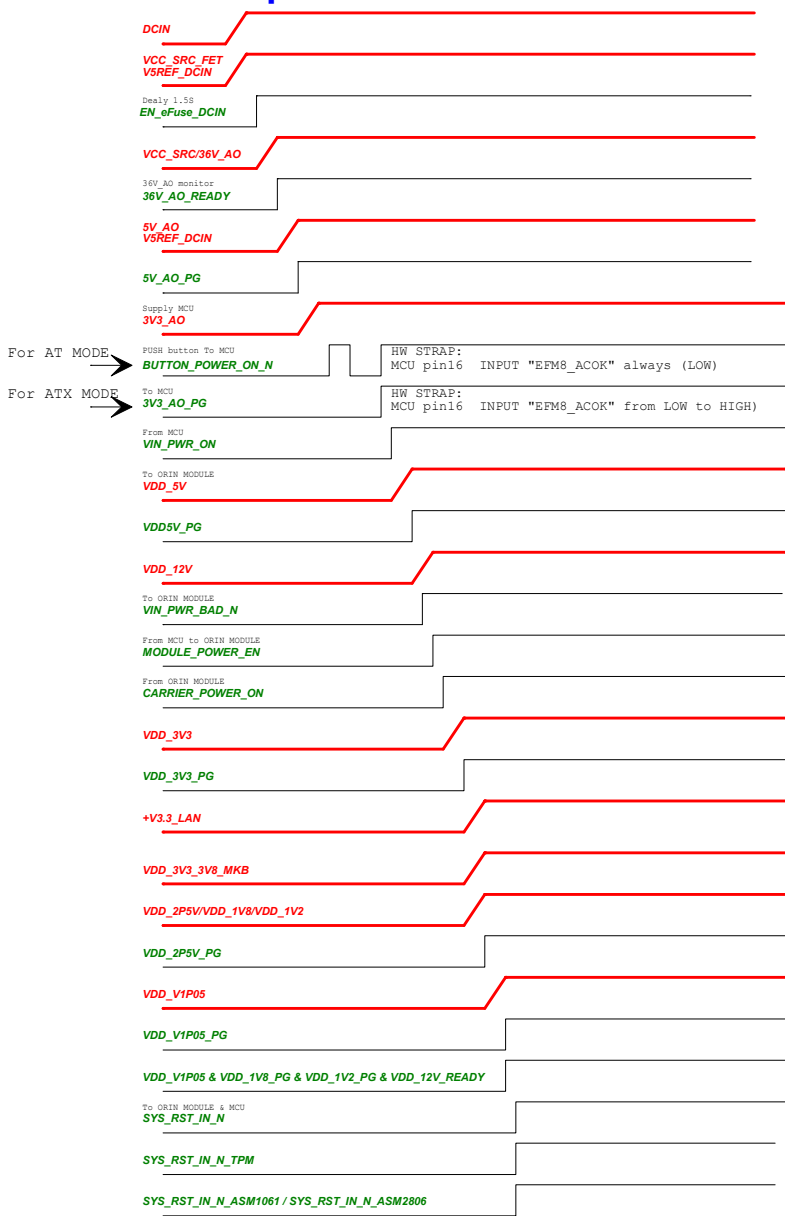
Jetson AGX Orin Connector Pin Names	Reference Schematic Symbol Connector Pin Names	Orin UPHY Block and Lane	Jetson AGX Orin Functions		AIR-030 SPEC (Newest design)
			Function #1	Function #2	Function #1
UPHY_RX0/TX0	UPHY_RX0/TX0	UPHY0, Lane 0	USB 3.2 (P0)	PCIe x1 (C0), RP	
UPHY_RX1/TX1	UPHY_RX1/TX1	UPHY0, Lane 1	USB 3.2 (P1)	USB 3.2 (P1)	USB3 HUB GL3590 4*USB3 downstream=> 1) TYPE-C (USB3.2) 2),3)One USB3.2 TYPE-A X2 STACKUP
UPHY_RX20/TX20	NVHS1_RX0/TX0	UPHY0, Lane 2	USB 3.2 (P2)	USB 3.2 (P2)	USB3 HUB GL3590 4*USB3 downstream=> 1),2) One USB3.2 TYPE-A X2 STACKUP 3) KEY-B (USB3.2)
UPHY_RX21/TX21	NVHS1_RX1/TX1	UPHY0, Lane 3	PCIe x1 (C1), RP	PCIe x1 (C1), RP	PCIe mux/demux (either one) (1)M.2 KEY-E or (2)LAN3
UPHY_RX22/TX22	NVHS1_RX2/TX2	UPHY0, Lane 4	PCIe x4 (C4), RP	PCIe x4 (C4), RP	ASM2806 (PCIEx2) PCIe GEN3 x2=> 1) PCIe GEN3 by 2 =>M.2 KEY-B 2) PCIe GEN3 X1 => IPOE LAN1 3) PCIe GEN3 X1 => IPOE LAN2
UPHY_RX23/TX23	NVHS1_RX3/TX3	UPHY0, Lane 5			
UPHY_RX10/TX10	UPHY_RX10/TX10	UPHY0, Lane 6			
UPHY_RX11/TX11	UPHY_RX11/TX11	UPHY0, Lane 7			
UPHY_RX12/TX12	NVHS0_SLVS_RX0/TX0	UPHY1, Lane 0	PCIe x8 (C5), RP/EP	PCIe x8 (C5), RP/EP	PCIEX16 SLOT (PCIe GEN4 x8 signal)
UPHY_RX13/TX13	NVHS0_SLVS_RX1/TX1	UPHY1, Lane 1			
UPHY_RX14/TX14	NVHS0_SLVS_RX2/TX2	UPHY1, Lane 2			
UPHY_RX15/TX15	NVHS0_SLVS_RX3/TX3	UPHY1, Lane 3			
UPHY_RX16/TX16	NVHS0_SLVS_RX4/TX4	UPHY1, Lane 4			
UPHY_RX17/TX17	NVHS0_SLVS_RX5/TX5	UPHY1, Lane 5			
UPHY_RX18/TX18	NVHS0_SLVS_RX6/TX6	UPHY1, Lane 6			
UPHY_RX19/TX19	NVHS0_SLVS_RX7/TX7	UPHY1, Lane 7			
UPHY_RX2/TX2	UPHY_RX2/TX2	UPHY2, Lane 0		PCIe x8 (C7), RP/EP	N.C
UPHY_RX3/TX3	UPHY_RX3/TX3	UPHY2, Lane 1			
UPHY_RX4/TX4	UPHY_RX4/TX4	UPHY2, Lane 2			
UPHY_RX5/TX5	UPHY_RX5/TX5	UPHY2, Lane 3			
UPHY_RX6/TX6	UPHY_RX6/TX6	UPHY2, Lane 4	MGBE (C0)		
UPHY_RX7/TX7	UPHY_RX7/TX7	UPHY2, Lane 5			
UPHY_RX8/TX8	UPHY_RX8/TX8	UPHY2, Lane 6			
UPHY_RX9/TX9	UPHY_RX9/TX9	UPHY2, Lane 7			

Power Delivery

DCIN 9-36



Power On Sequence



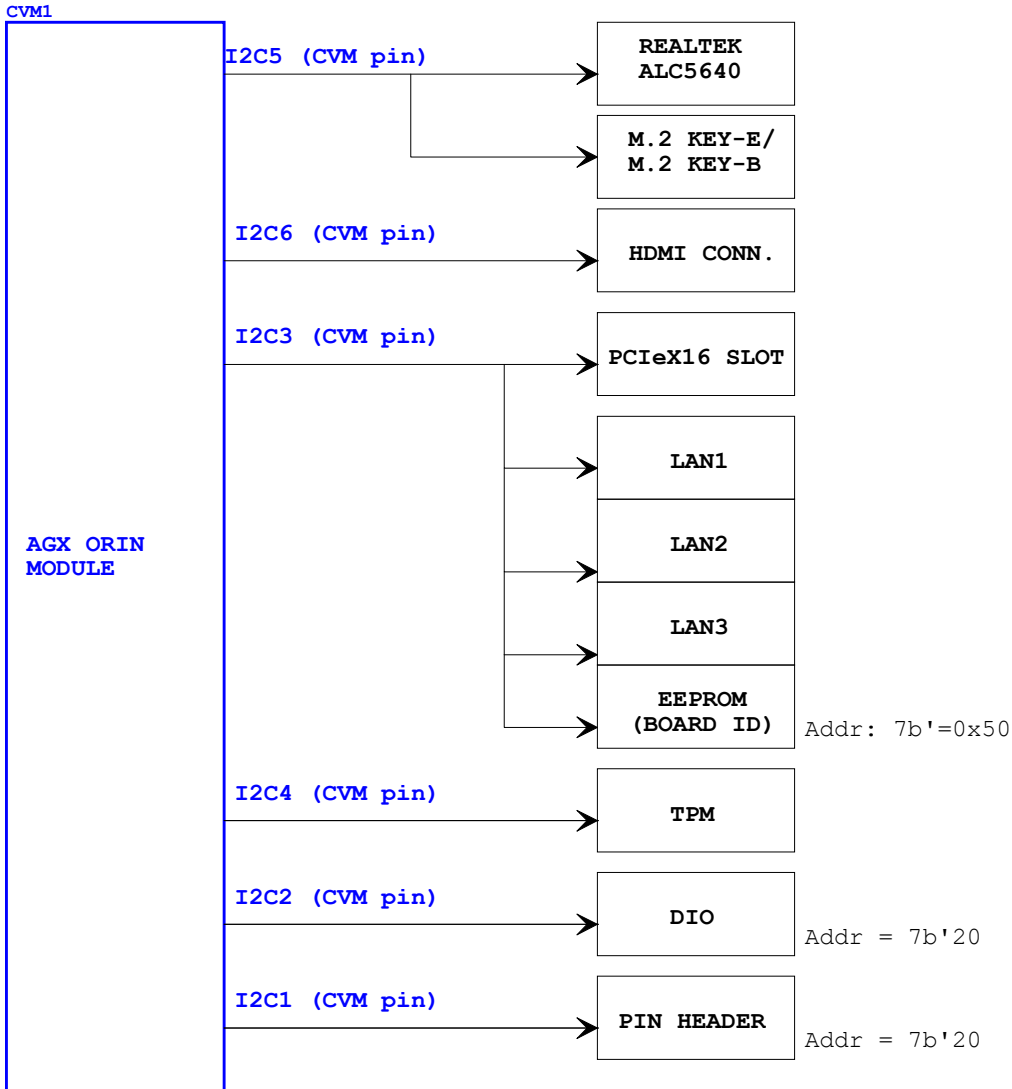
Clocks Distribution

CVM1



AGX ORIN
MODULE

SMBUS Distribution



GPIO LIST

ADVANTECH		
Title	08_GPIO LIST	
Size	Document Number	Rev
	AIR-030	A101-1
Date:	Wednesday, August 10, 2022	Sheet 8 of 48

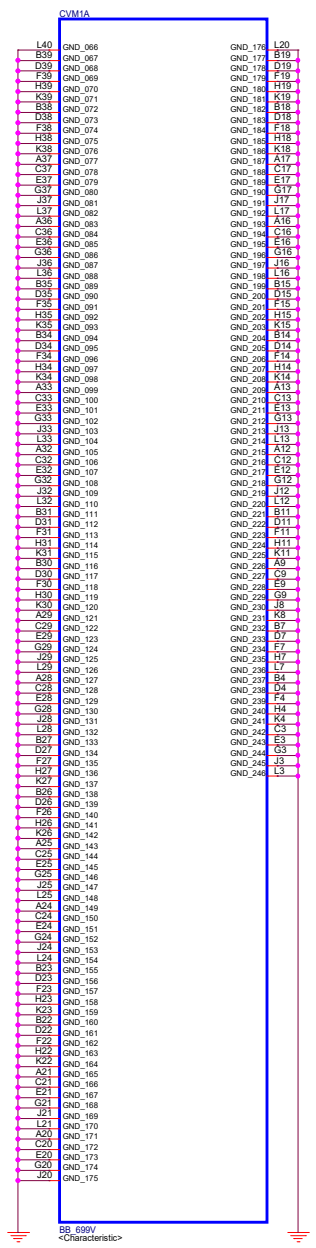
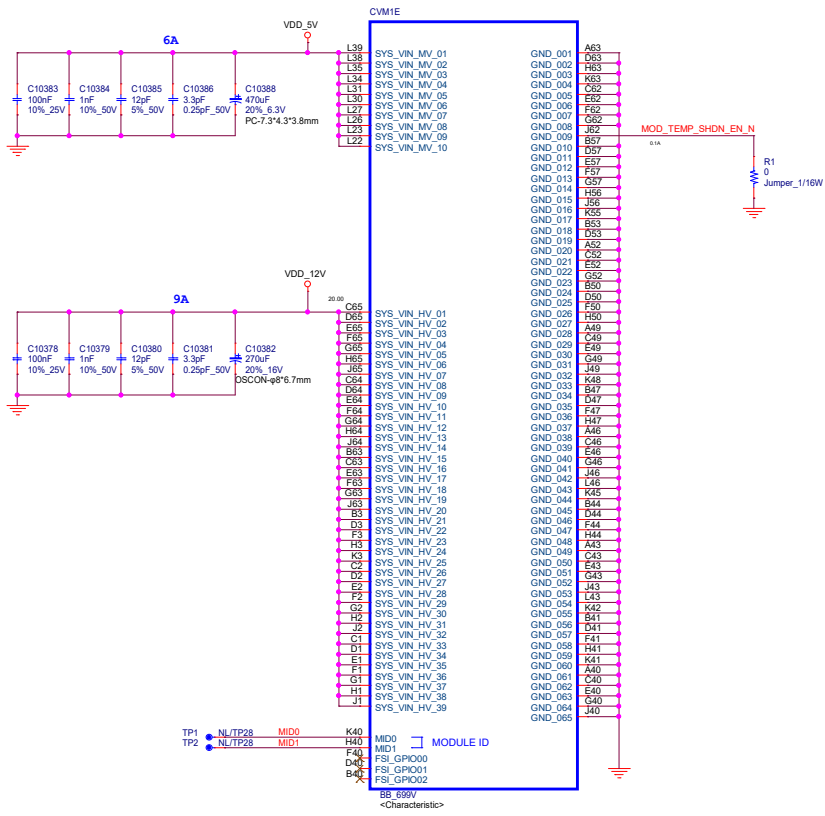


Table 7-1. Maximum Ratings

Symbol	Parameter	Min	Max	Unit	Notes
VIN	SYS_VIN_HV	-0.5	22.5	V	
	SYS_VIN_MV	-0.5	6.0	V	
	PMIC_BBATT	-0.3	5.4	V	
IDDMAX	VIN I _{max} (SYS_VIN_HV)		5.4	A	Software limited. IDDMAX (HV/MV current) reflects EDPp based on a 6 uS moving window. 5.4A is for VIN [20V] on SYS_VIN_HV. 6.0A is for VIN [5V] on SYS_VIN_MV. Actual IDDMAX is dependent on VIN [VINMIN].
	VIN I _{max} (SYS_VIN_MV)		6.0	A	
VM_PIN	Voltage applied to any powered I/O pin	-0.5	VDD + 0.5	V	
	DD pads configured as open drain	-0.5	3.63	V	Pad's output driver must be set to open drain mode

Table 7-2. Recommended Operating Conditions

Symbol	Parameter	Min	Typical	Max	Unit	Notes
VDDdc	SYS_VIN_HV	7	12	20	V	
	SYS_VIN_MV	4.75	5	5.25	V	
	PMIC_BBATT	1.65	3.3	3.45	V	Input Only

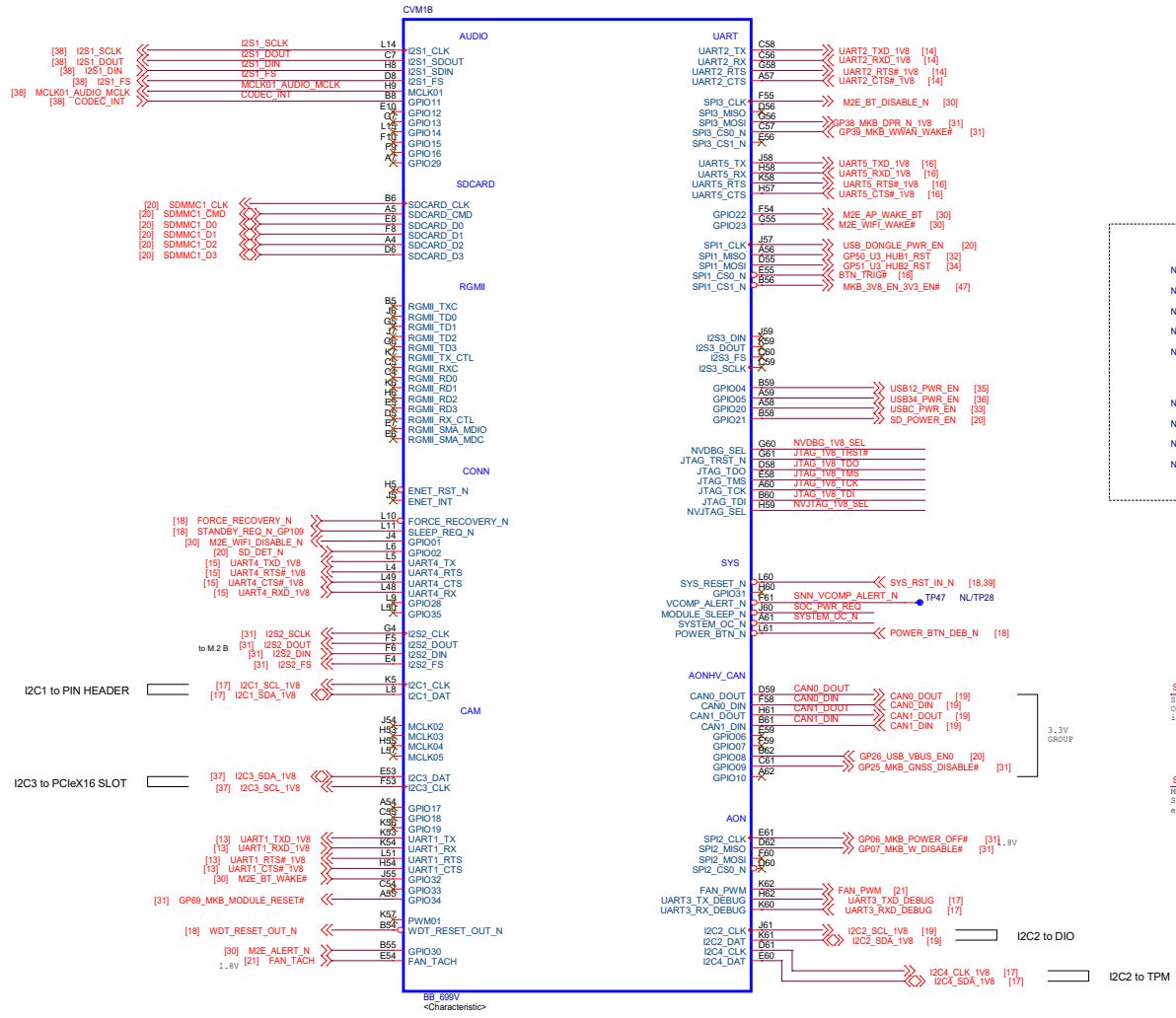
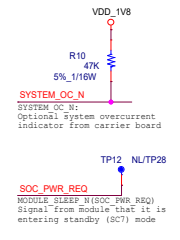
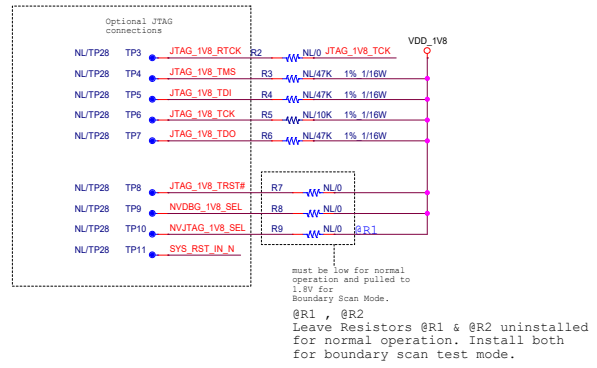
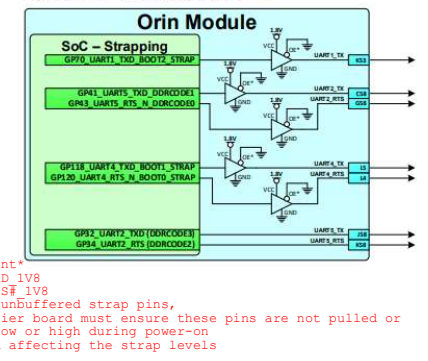
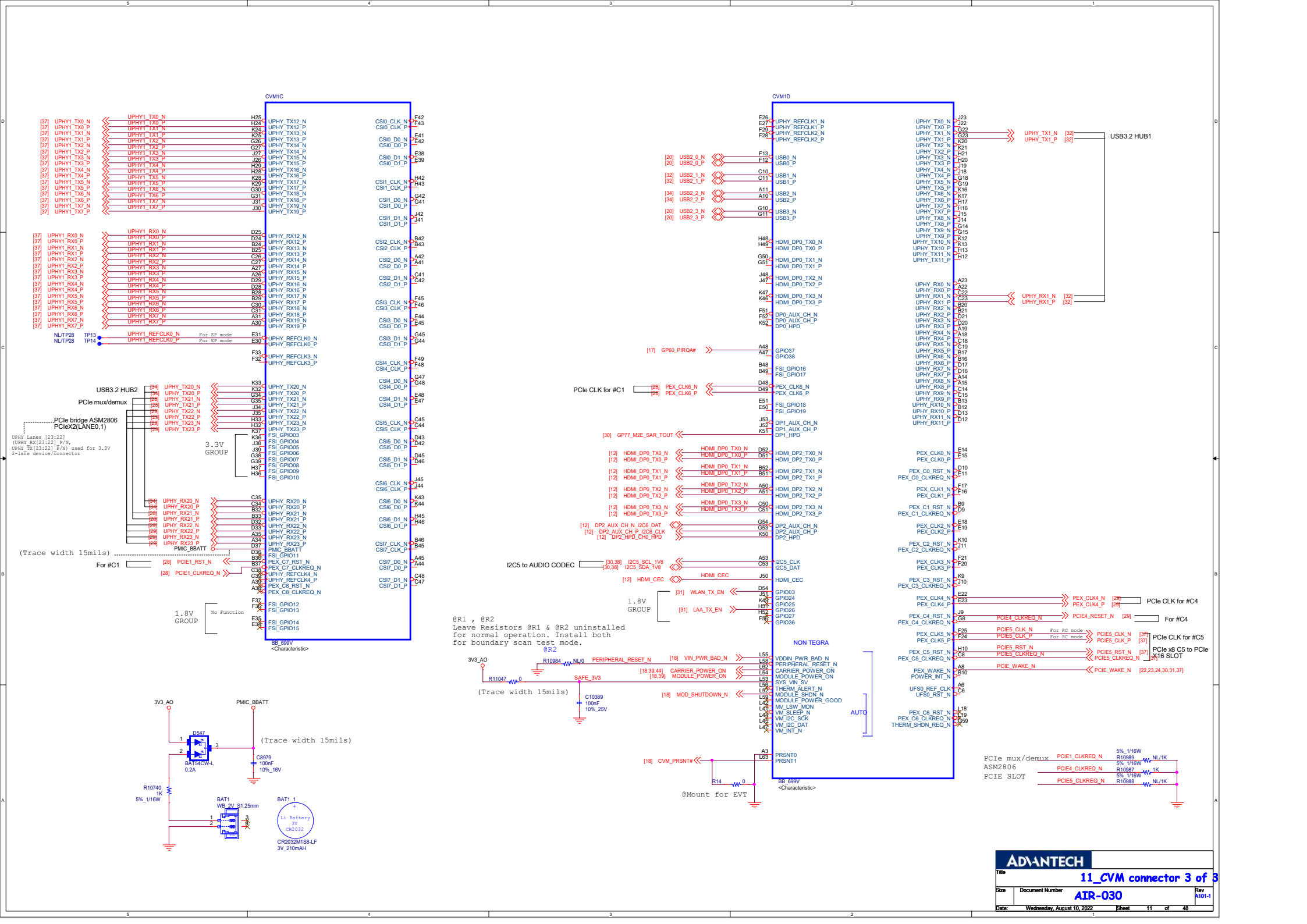


Figure 18-2. Orin Module Strap Pins

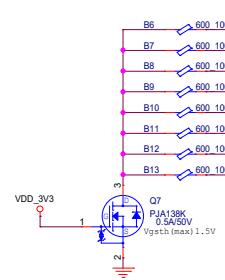
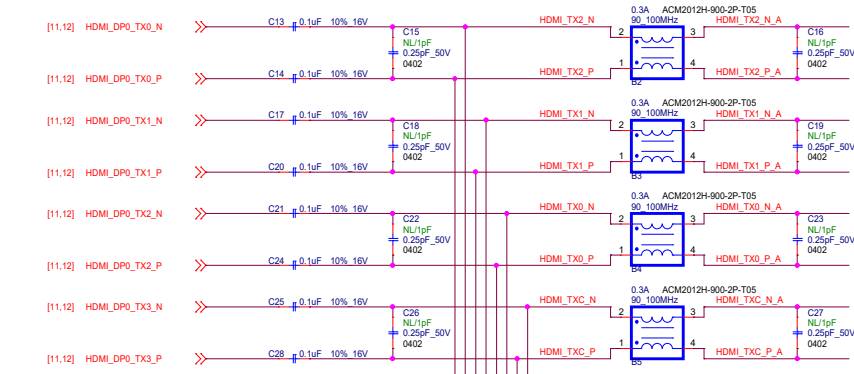
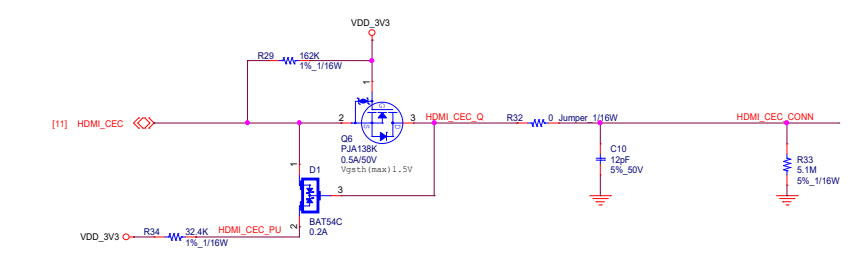
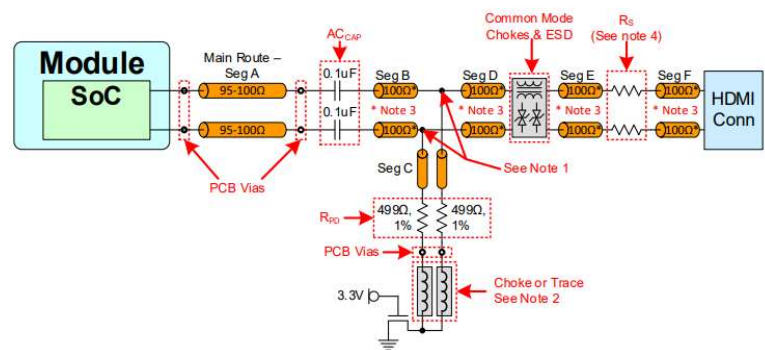




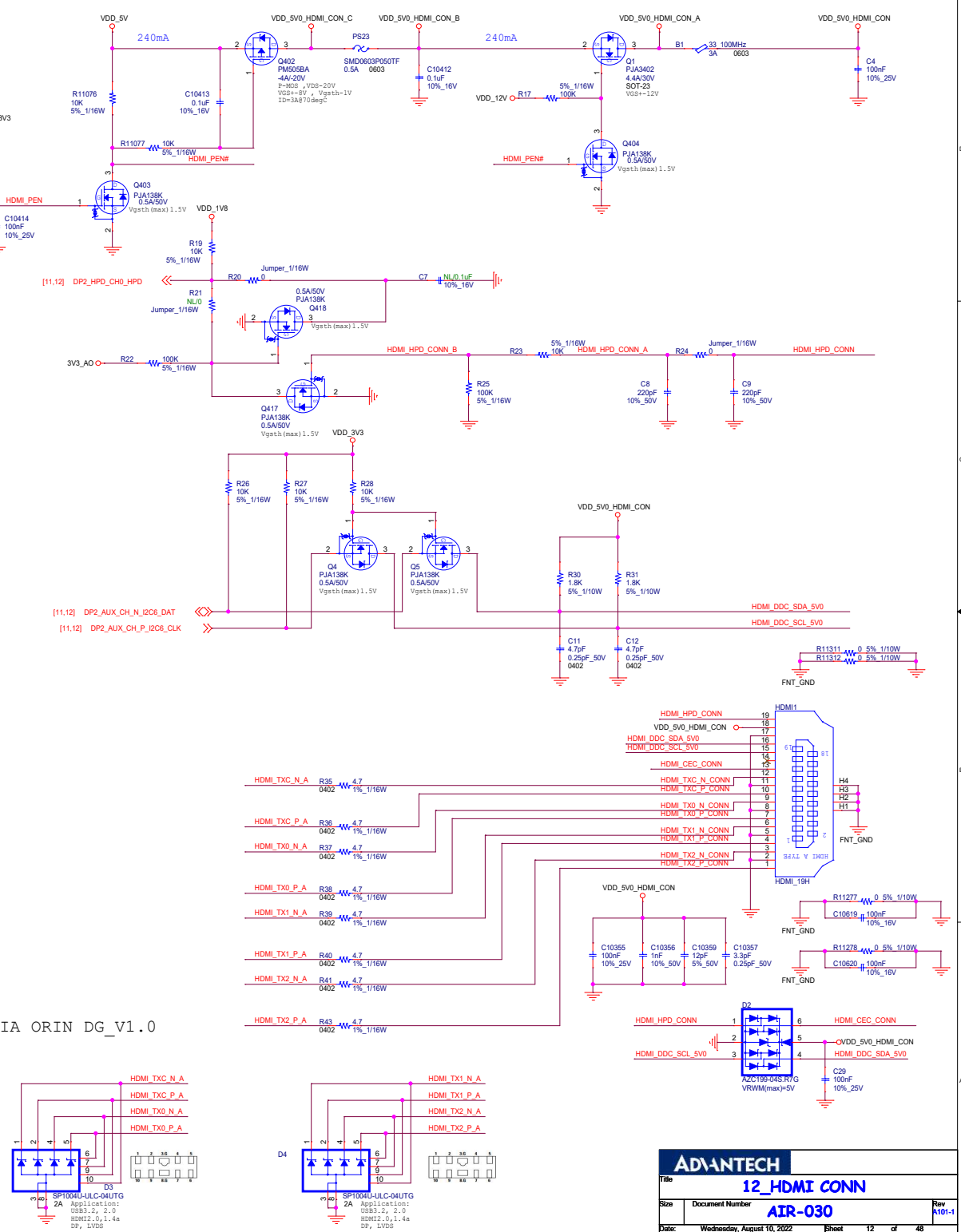
- HDMI_DP0_TX0_N $=$ HDMI_DP0_TX0_P [11,12]
- HDMI_DP0_TX1_N $=$ HDMI_DP0_TX1_P [11,12]
- HDMI_DP0_TX2_N $=$ HDMI_DP0_TX2_P [11,12]
- HDMI_DP0_TX3_N $=$ HDMI_DP0_TX3_P [11,12]
- DP2_AUX_CH_N_I2C6_DAT $=$ DP2_AUX_CH_P_I2C6_DAT [11,12]
- DP2_AUX_CH_P_I2C6_CLK $=$ DP2_AUX_CH_P_I2C6_CLK [11,12]
- DP2_HPD_CH0_HPD $=$ DP2_HPD_CH0_HPD [11,12]

Document: Jetson_AGX_Orin_Design_Guide_DG-10653-001_v1.0

Figure 8-4. HDMI CLK and Data Topology

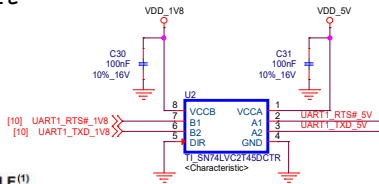


Common Choke follow NVIDIA ORIN DG_V1.0



COM1 : RS232/422/485

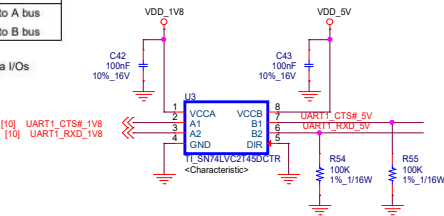
Level Shift



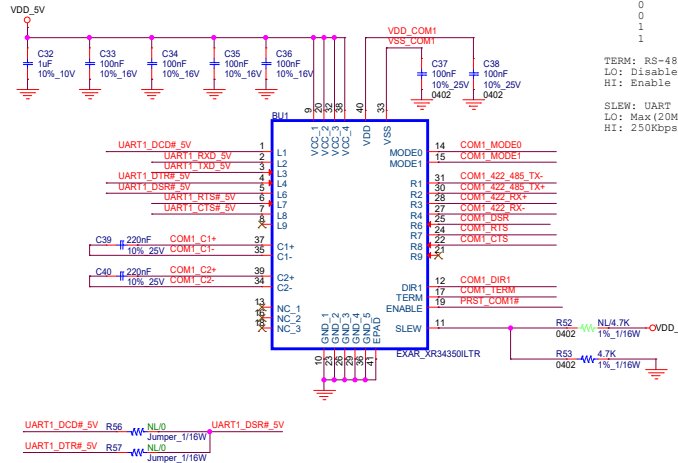
FUNCTION TABLE⁽¹⁾
(EACH TRANSCEIVER)

INPUT DIR	OPERATION
L	B data to A bus
H	A data to B bus

(1) Input circuits of the data I/Os always are active.



TRANSCEIVER



EXAR_XR34350LTR
(MODE1) (MODE0) | Function

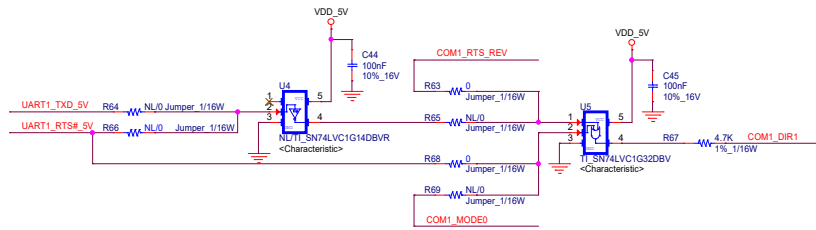
0	0	Loopback
0	1	RS-232
1	0	RS-485 Half Duplex(auto flow)
1	1	RS-422 Full Duplex

TERM: RS-485/422 receiver termination
LO: Disable
HI: Enable, default

SLEW: UART slew limiting
LO: Max(20M/422/485, 1M/232), default
HI: 250Kbps

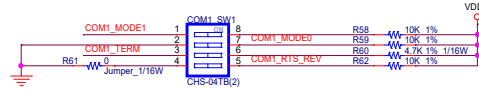
While the normal PC hardware might well run with just Tx, Rx and Ground connected, most driver software will wait forever for one of the handshaking lines to go to the correct level. Depending on the signal state it might sometimes work, other times it might not. The reliable solution is to loop back the handshake lines if they are not used.

(AUTO FLOW CIRCUIT NO USE)

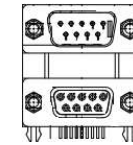


Mode Selection

(DIP SW place BOT side)



SW1	SW2	SW3	SW4	Function
OFF	OFF	X	X	RS232
ON	OFF	OFF	OFF	RS422 (Dis_Terminal)
ON	OFF	ON	OFF	RS422 (En_Terminal)
ON	ON	OFF	OFF	RS485 (Dis_Terminal, Receiver)
ON	ON	ON	OFF	RS485 (En_Terminal, Receiver)
ON	ON	ON	ON	RS485 (En_Terminal, transmitter)
OFF	ON	X	X	LOOPBACK



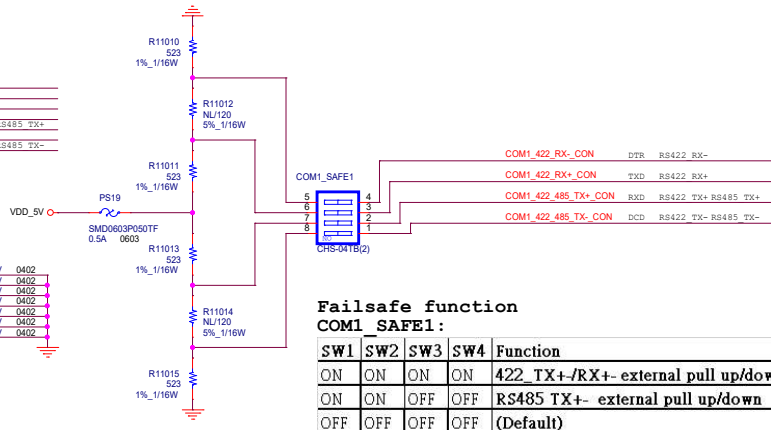
COM1 , UPPER

COM2 , LOWER

COM1 (DB9)

COM1_422_RX-	B14	0.3A	600	100MHz	0402	COM1_422_RX- CON	DTR	RS422_RX-
COM1_CTS	B15	0.3A	600	100MHz	0402	COM1_CTS CON	CTS	RS422_RX+
COM1_422_RX+	B16	0.3A	600	100MHz	0402	COM1_422_RX+ CON	TXD	RS422_RX+
COM1_RTS	B17	0.3A	600	100MHz	0402	COM1_RTS CON	RTS	RS422_TX-
COM1_422_485_TX-	B18	0.3A	600	100MHz	0402	COM1_422_485_TX- CON	RXD	RS422_TX+ RS485_TX+
COM1_DSR	B19	0.3A	600	100MHz	0402	COM1_DSR CON	DSR	RS422_TX-
COM1_422_485_TX+	B20	0.3A	600	100MHz	0402	COM1_422_485_TX+ CON	DCD	RS422_TX- RS485_TX-

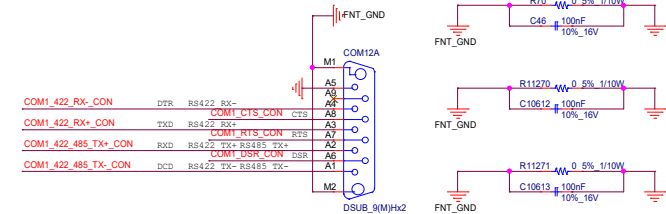
COM1_422_RX- CON	C47	180pF	10%	50V	0402
COM1_CTS CON	C48	180pF	10%	50V	0402
COM1_422_RX+ CON	C49	180pF	10%	50V	0402
COM1_RTS CON	C50	180pF	10%	50V	0402
COM1_422_485_TX- CON	C51	180pF	10%	50V	0402
COM1_DSR CON	C52	180pF	10%	50V	0402
COM1_422_485_TX+ CON	C53	180pF	10%	50V	0402



Failsafe function

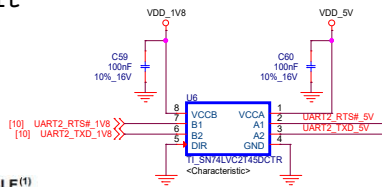
COM1_SAFE1:

SW1	SW2	SW3	SW4	Function
ON	ON	ON	ON	422_TX+/-RX+ external pull up/down
ON	ON	OFF	OFF	RS485 TX+ external pull up/down
OFF	OFF	OFF	OFF	(Default)



COM2 : RS232/422/485

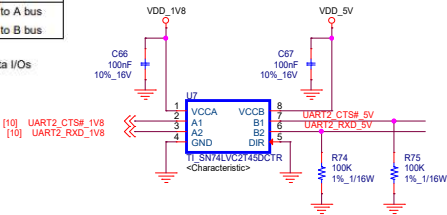
Level Shift



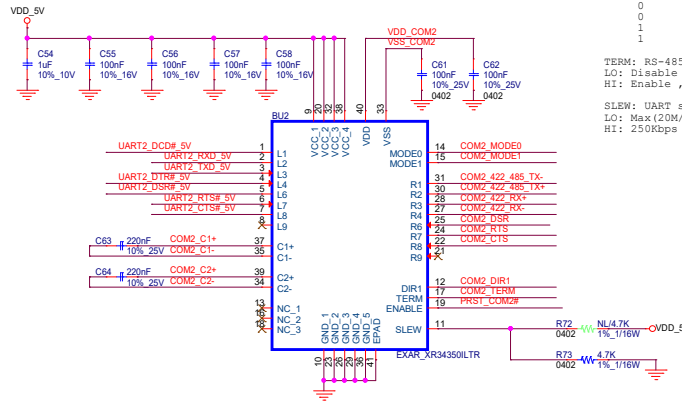
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TRANSCEIVER

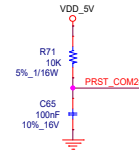


EXAR XR34350L1TR
(MODE1) (MODE0) | Function

0	0	Loopback
0	1	RS-232
1	0	RS-485 Half Duplex (auto flow)
1	1	RS-422 Full Duplex

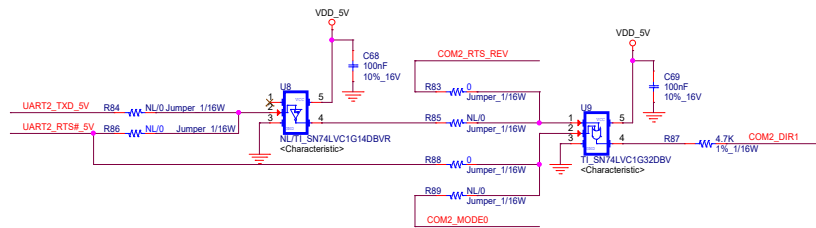
TERM: RS-485/422 receiver termination
LO: Disable
HI: Enable, default

SLEW: UART slew limiting
LO: Max (20M/422/485, 1M/232), default
HI: 250Kbps

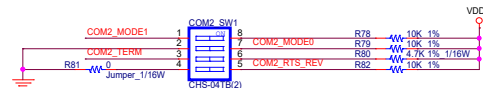


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(AUTO FLOW CIRCUIT NO USE)

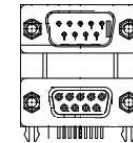


Mode Selection (DIP SW place BOT side)



Default

SW1	SW2	SW3	SW4	Function
OFF	OFF	X	X	RS232
ON	OFF	OFF	OFF	RS422 (Dis_Terminal)
ON	OFF	ON	OFF	RS422 (En_Terminal)
ON	ON	OFF	OFF	RS485 (Dis_Terminal, Receiver)
ON	ON	ON	OFF	RS485 (En_Terminal, Receiver)
ON	ON	ON	ON	RS485 (En_Terminal, transmitter)
OFF	ON	X	X	LOOPBACK



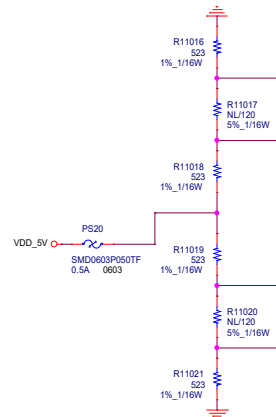
COM1 , UPPER

COM2 , LOWER

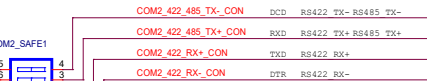
COM2 (DB9)

COM2_422_RX-	B21	0.3A	600	100MHz	0402	COM2_422_RX- CON	DTR	RS422_RX-
COM2_CTS	B22	0.3A	600	100MHz	0402	COM2_CTS+ CON	CTS	RS422_CTS+
COM2_422_RX+	B23	0.3A	600	100MHz	0402	COM2_422_RX+ CON	RXD	RS422_RX+
COM2_RTS	B24	0.3A	600	100MHz	0402	COM2_RTS CON	RTS	RS422_TX-
COM2_422_485_TX+	B25	0.3A	600	100MHz	0402	COM2_422_485_TX+ CON	RXD	RS422_TX+ RS485_TX+
COM2_DSR	B26	0.3A	600	100MHz	0402	COM2_DSR CON	DSR	RS422_DSR
COM2_422_485_TX-	B27	0.3A	600	100MHz	0402	COM2_422_485_TX- CON	DCD	RS422_TX- RS485_TX-

COM2_422_RX- CON	C71	180pF	10%	50V	0402
COM2_CTS CON	C72	180pF	10%	50V	0402
COM2_422_RX+ CON	C73	180pF	10%	50V	0402
COM2_RTS CON	C74	180pF	10%	50V	0402
COM2_422_485_TX+ CON	C75	180pF	10%	50V	0402
COM2_DSR CON	C76	180pF	10%	50V	0402
COM2_422_485_TX- CON	C77	180pF	10%	50V	0402



Failsafe function
COM1_SAFE1:
Default: OFF , OFF , OFF



Failsafe function
COM2_SAFE1:

SW1	SW2	SW3	SW4	Function
ON	ON	ON	ON	422_TX+ /RX+- external pull up/down
ON	ON	OFF	OFF	RS485 TX+- external pull up/down
OFF	OFF	OFF	OFF	(Default)

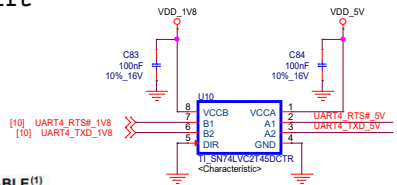


ADVANTECH

Title		14_COM2(RS232/422/485)	
Size	Document Number	AIR-030	
Date:	Wednesday, August 10, 2022	Sheet	14 of 48

COM4 : RS232/422/485

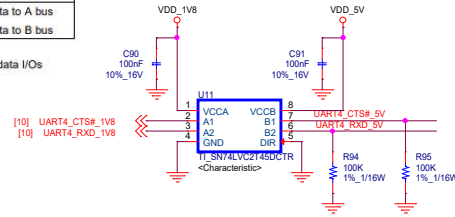
Level Shift



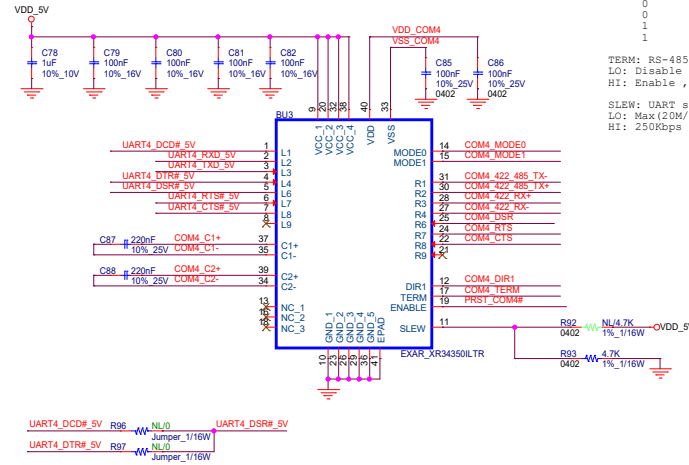
FUNCTION TABLE⁽¹⁾
(EACH TRANSCEIVER)

INPUT DIR	OPERATION
L	B data to A bus
H	A data to B bus

(1) Input circuits of the data I/Os always are active.



TRANSCEIVER



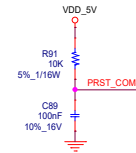
```

EXAR_XR34350ILTTR
(MODE1) (MODE0) | Function
0 0 Loopback
0 1 RS-232
1 0 RS-485 Half Duplex(auto flow)
1 1 RS-422 Full Duplex
    
```

```

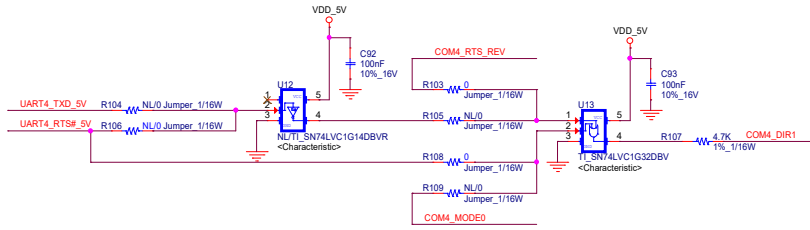
TERM: RS-485/422 receiver termination
LO: Disable
HI: Enable , default

SLEW: UART slew limiting
LO: Max(20M/422/485, 1M/232) ,default
HI: 250Kbps
    
```

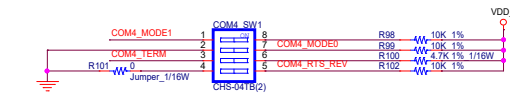


While the normal PC hardware might well run with just Tx, Rx and Ground connected, most driver software will wait forever for one of the handshaking lines to go to the correct level. Depending on the signal state it might sometimes work, other times it might not. The reliable solution is to loop back the handshake lines if they are not used.

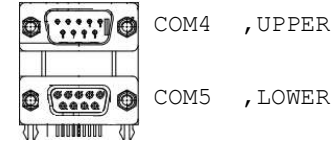
(AUTO FLOW CIRCUIT NO USE)



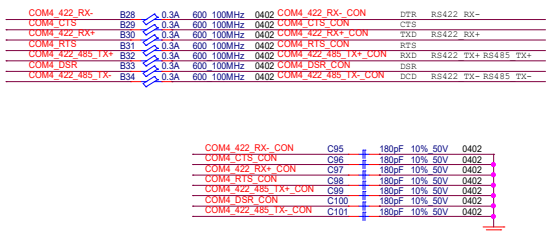
Mode Selection (DIP SW place BOT side)



SW1	SW2	SW3	SW4	Function
OFF	OFF	X	X	RS232
ON	OFF	OFF	OFF	RS422 (Dis_Terminal)
ON	OFF	ON	OFF	RS422 (En_Terminal)
ON	ON	OFF	OFF	RS485 (Dis_Terminal, Receiver)
ON	ON	ON	OFF	RS485 (En_Terminal, Receiver)
ON	ON	ON	ON	RS485 (En_Terminal, transmitter)
OFF	ON	X	X	LOOPBACK



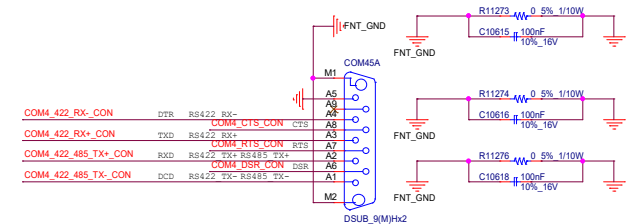
COM4 (DB9)



Failsafe function
COM4_SAFE1:
Default: OFF ,OFF ,OFF ,OFF

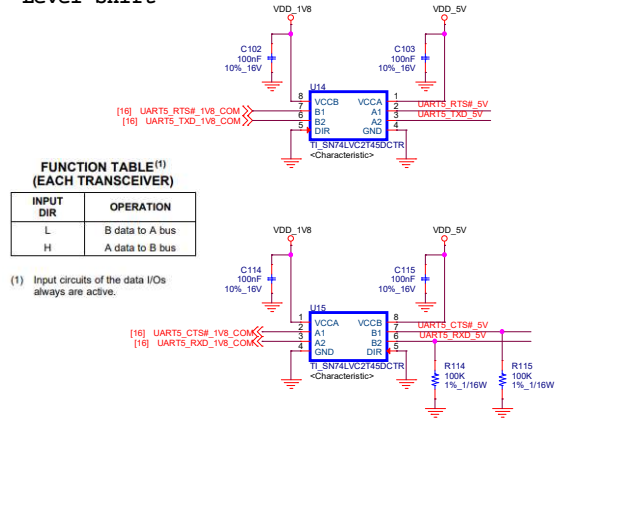
Failsafe function
COM4_SAFE1:

SW1	SW2	SW3	SW4	Function
ON	ON	ON	ON	422_TX+ /RX+ - external pull up/down
ON	ON	OFF	OFF	RS485 TX+ - external pull up/down
OFF	OFF	OFF	OFF	(Default)

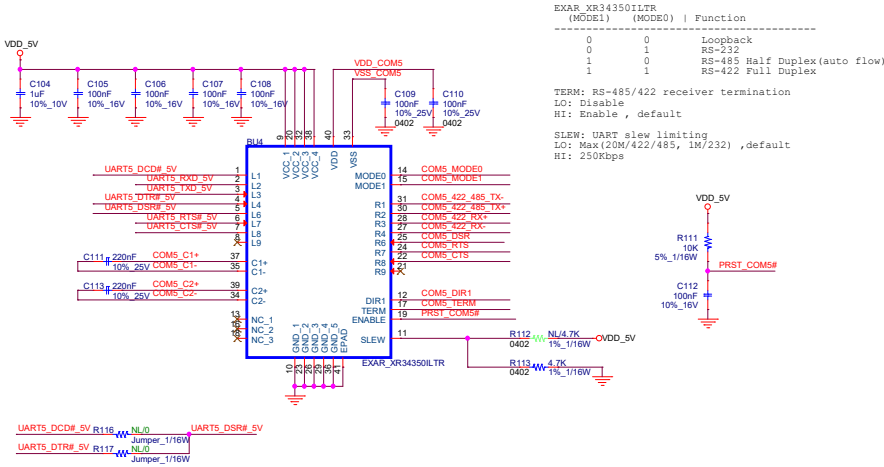


COM5 : RS232/422/485

Level Shift

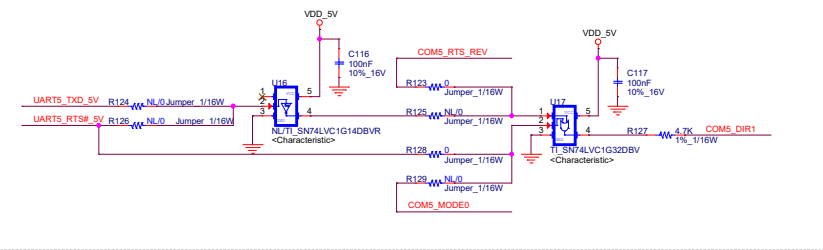


TRANSCEIVER

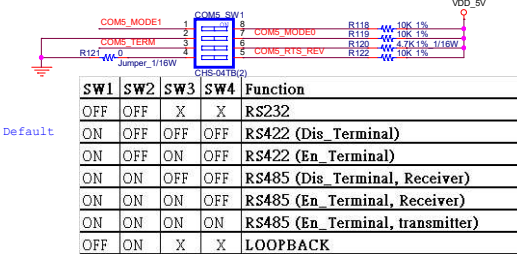


While the normal PC hardware might well run with just Tx, Rx and Ground connected, most driver software will wait forever for one of the handshaking lines to go to the correct level. Depending on the signal state it might sometimes work, other times it might not. The reliable solution is to loop back the handshake lines if they are not used.

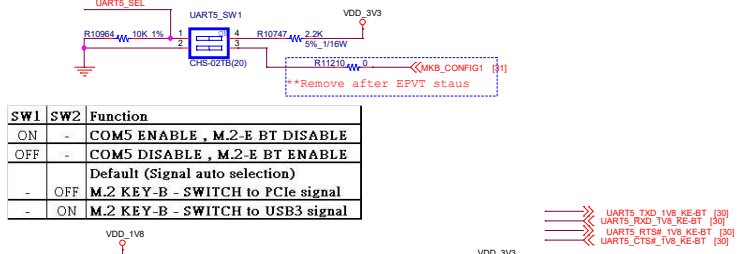
(AUTO FLOW CIRCUIT NO USE)



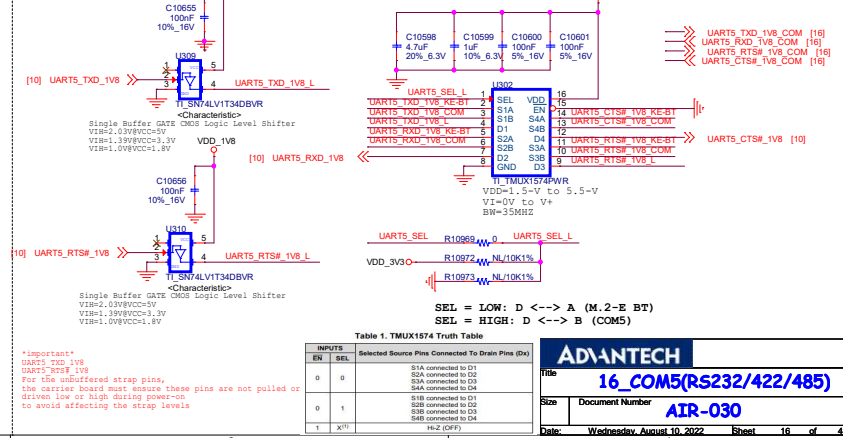
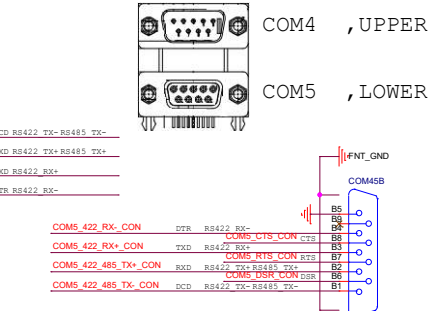
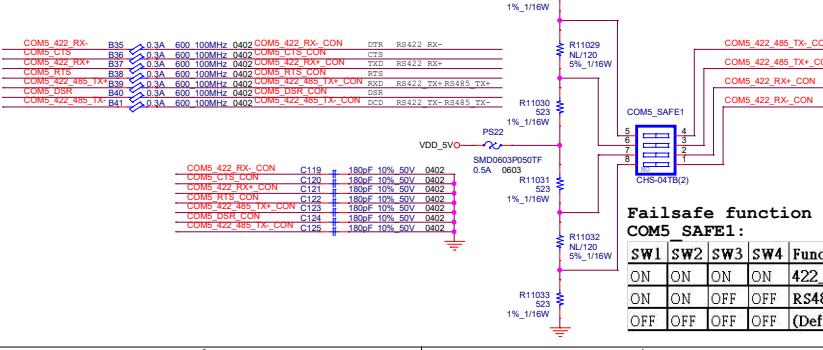
Mode Selection



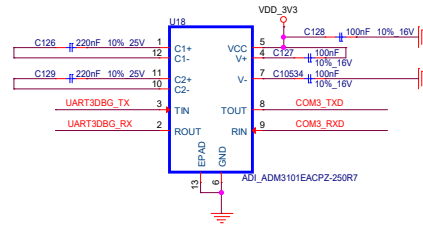
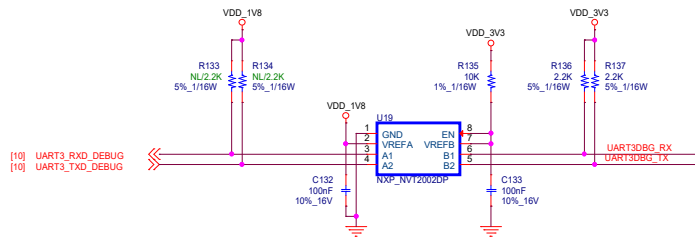
UART5 Selection (DIP SW place BOT side)



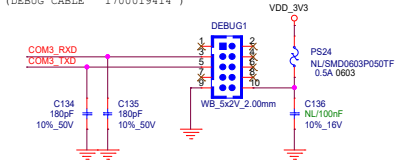
COM5 (DB9)



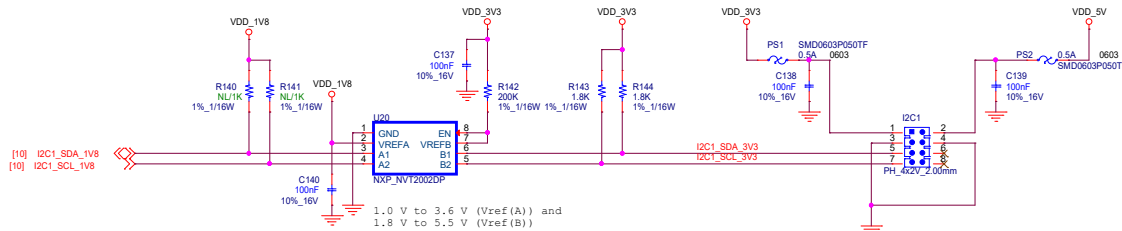
COM3: DEBUG PORT



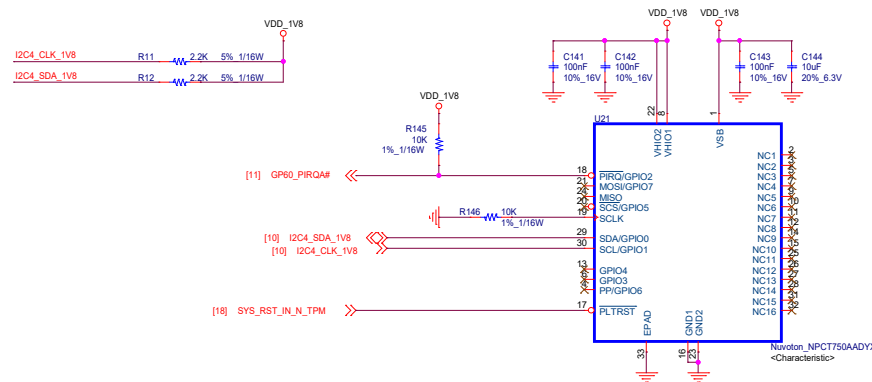
(DEBUG1 place BOT side)
(DEBUG CABLE 1700019414)



I2C1 HEADER



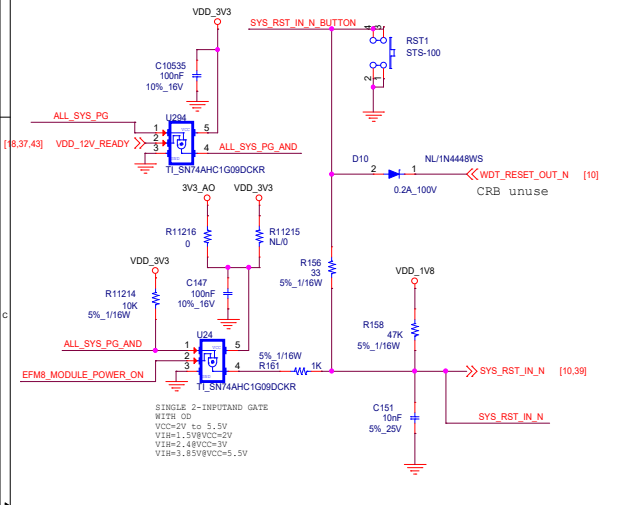
TPM 2.0



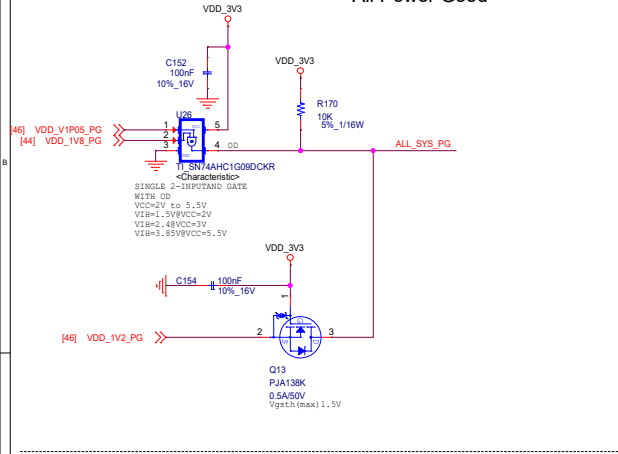
MISC Button

(RST1 & RCOVY1 place BOT side)

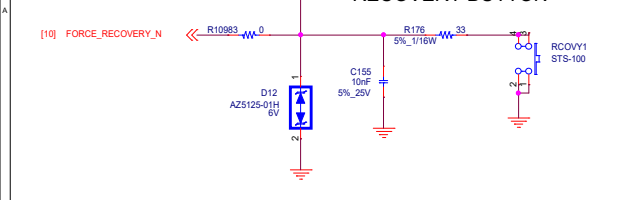
RESET BUTTON



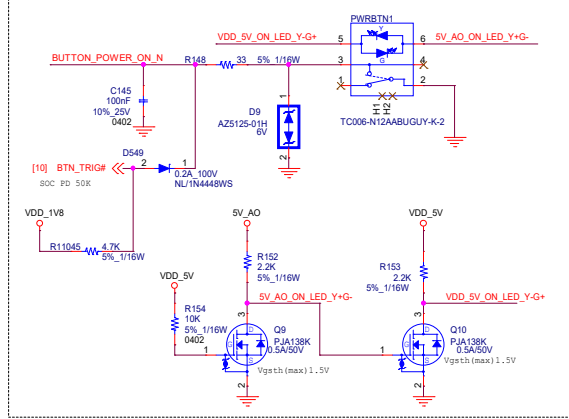
All Power Good



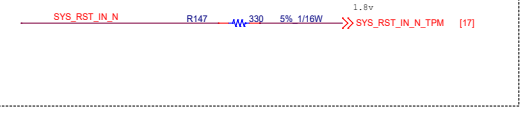
RECOVERY BUTTON



POWER BUTTON



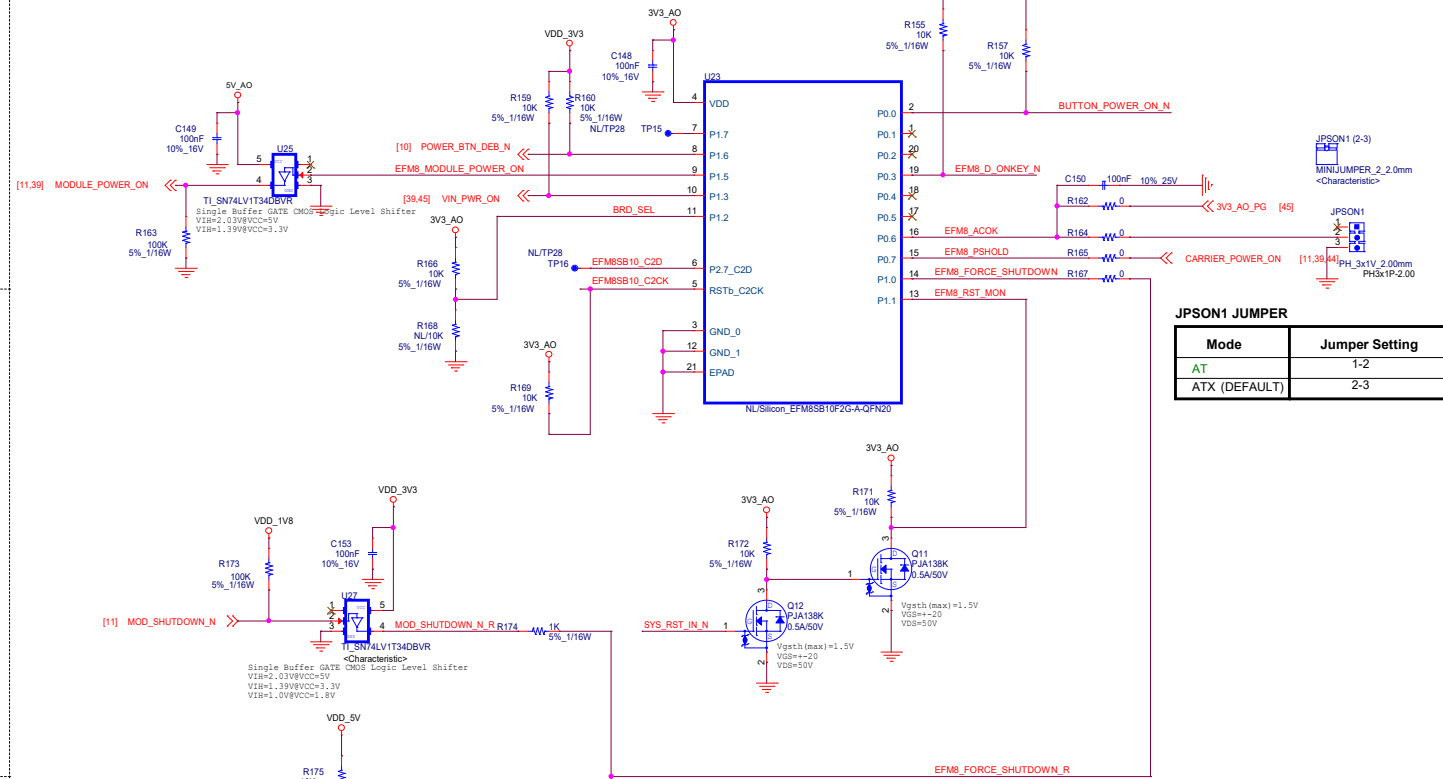
System Reset



@U23 FW check



U23 IMG1
MCU AIR-030 V100 CS:7888 EFM8SB10F2G-A-QFN20

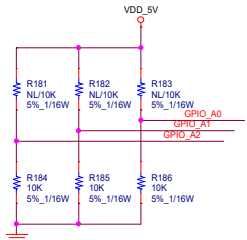


JPSON1 JUMPER

Mode	Jumper Setting
AT	1-2
ATX (DEFAULT)	2-3

Jetson AGX Orin Series Design Guide_DG-10653-001 v1.1:
VDDIN_PWR_BAD_N should stay active (low) until both SYS_VIN_HV/MV are valid (and not gated).

DIO 16bit



Addr = 7b'20

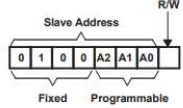
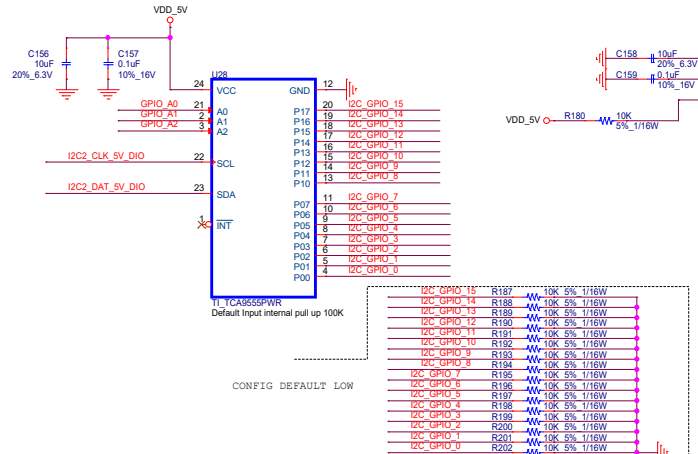


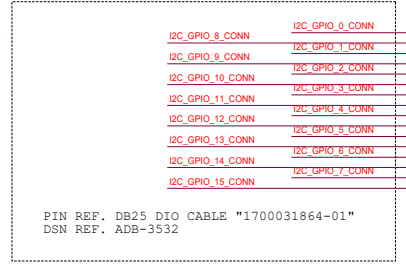
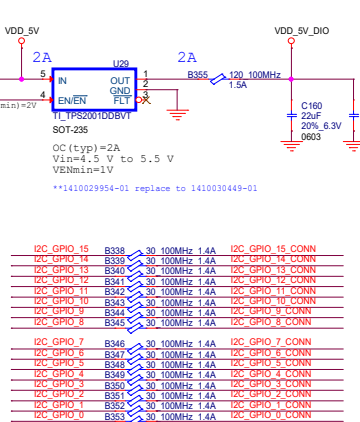
Figure 4. TCA9555 Address

Address Reference

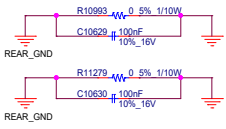
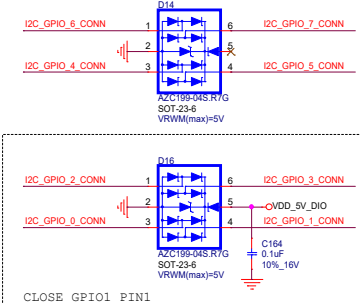
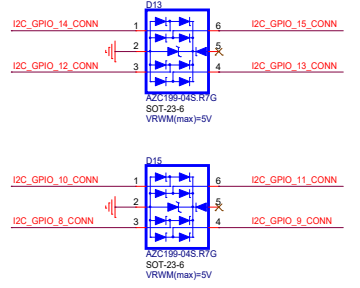
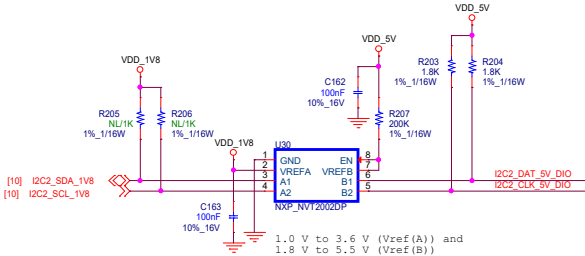
INPUTS			I ² C BUS SLAVE ADDRESS	
A2	A1	A0	32 (decimal), 20 (hexadecimal)	33 (decimal), 21 (hexadecimal)
L	L	L	32 (decimal), 20 (hexadecimal)	33 (decimal), 21 (hexadecimal)
L	L	H	34 (decimal), 22 (hexadecimal)	35 (decimal), 23 (hexadecimal)
L	H	L	36 (decimal), 24 (hexadecimal)	37 (decimal), 25 (hexadecimal)
L	H	H	38 (decimal), 26 (hexadecimal)	39 (decimal), 27 (hexadecimal)
H	L	L		
H	L	H		
H	H	L		
H	H	H		



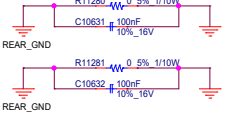
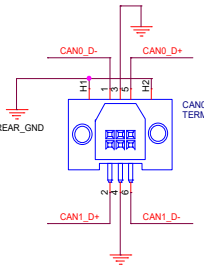
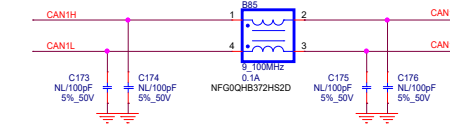
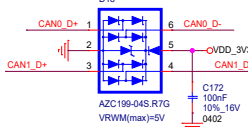
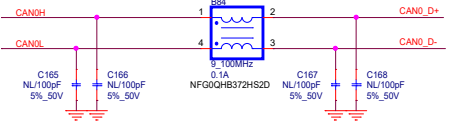
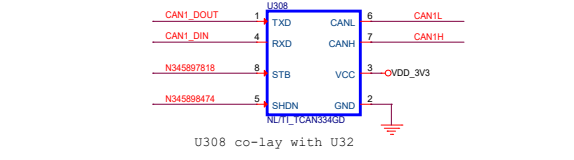
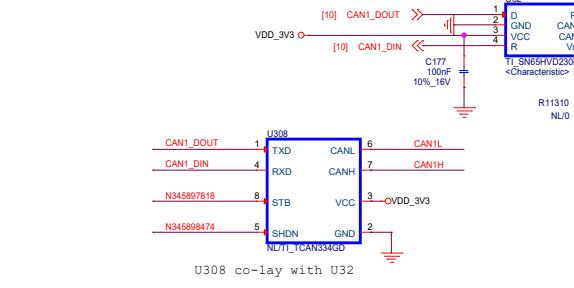
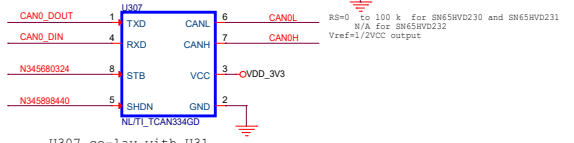
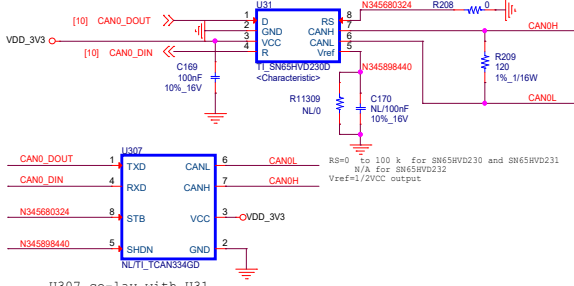
CONFIG DEFAULT LOW



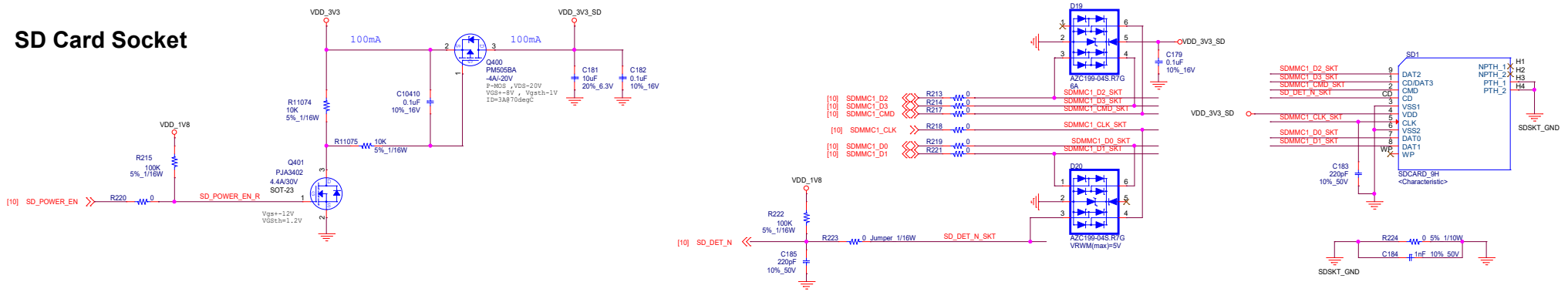
PIN REF. DB25 DIO CABLE "1700031864-01"
DSN REF. ADB-3532



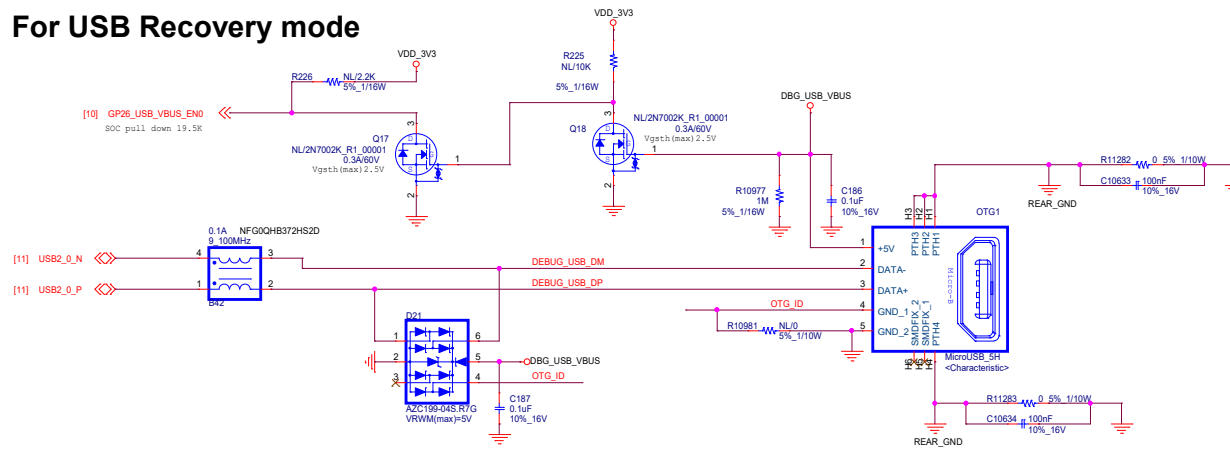
CAN BUS x2 (DB9)



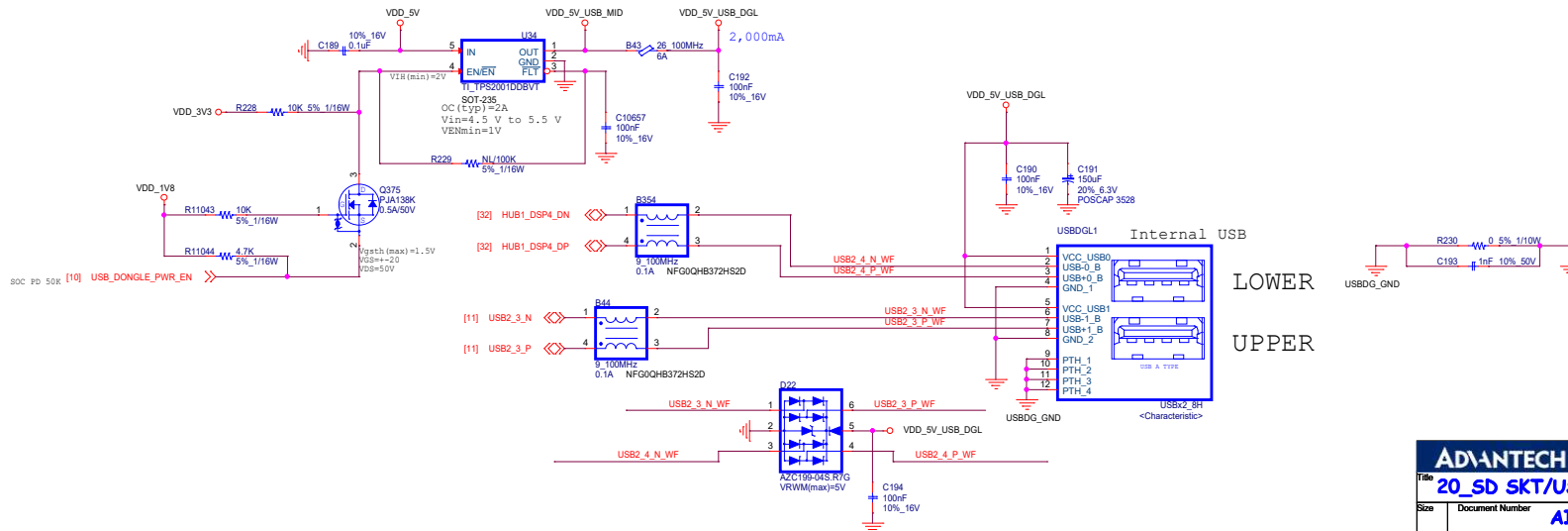
SD Card Socket



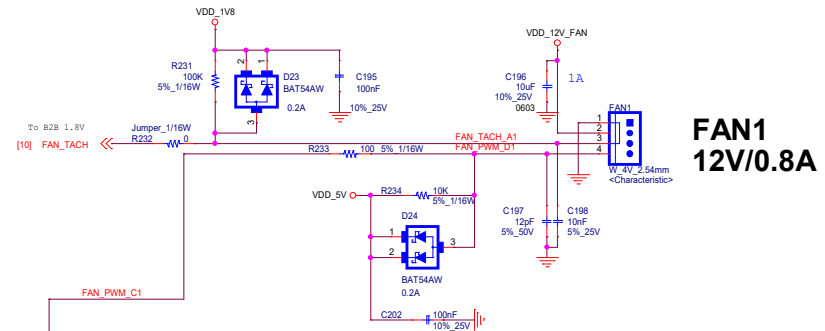
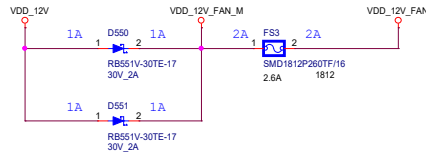
Micro USB (OTG) For USB Recovery mode



USB2.0 TYPE-A

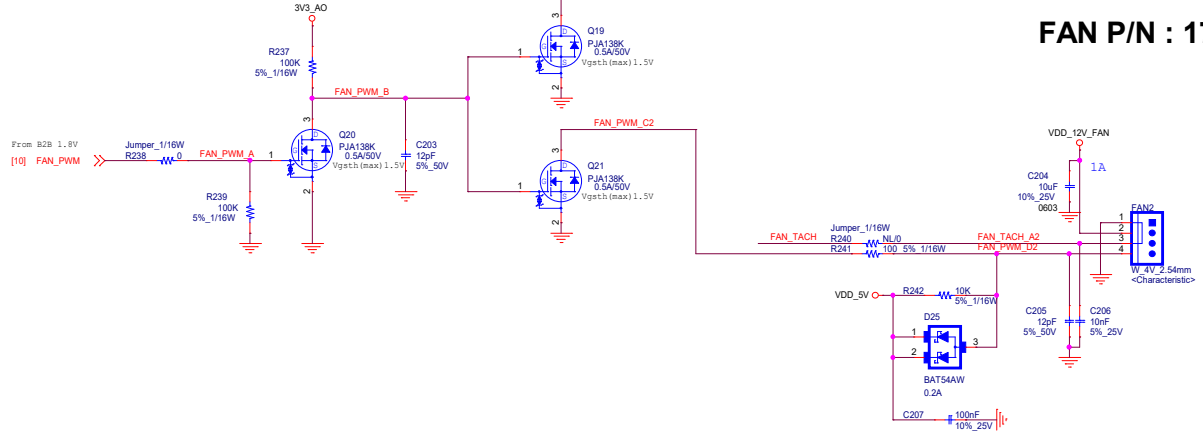


FAN CONN x2



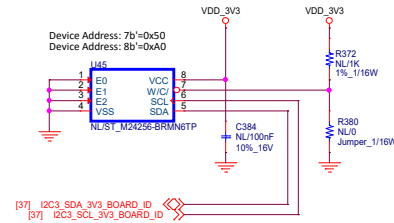
FAN1
12V/0.8A

FAN P/N : 1750007554-01



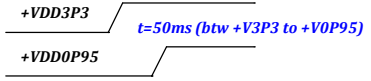
FAN2
12V/0.8A

BOARD ID



Ethernet Controller1: INTEL I225-LM [Co-Lay I226]

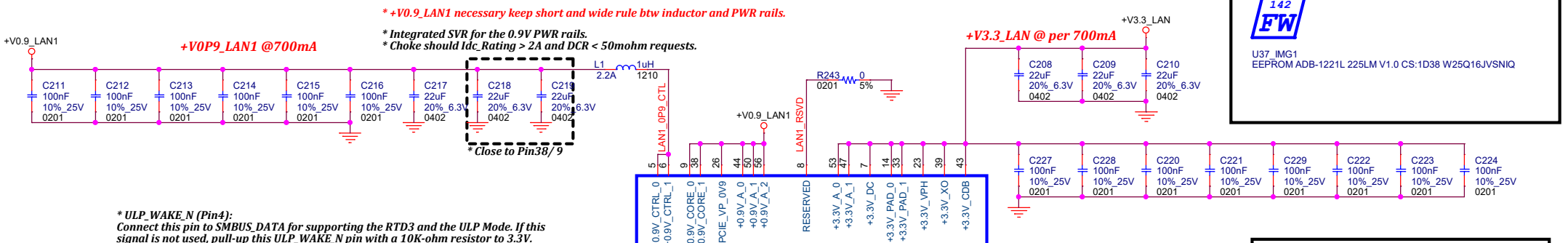
- * I211-AT: PN 1410023117-01 (Temp: 0~70C) / I225*: PN 1410029502-01 (Temp: -40~70C)
- * I210-IT: PN 1410022540-01 (Temp: -40~85C) / I210-AT: PN 1410022540-02 (Temp: 0~70C)
- > integrated Non-Volatile Memory (iNVM) / External Flash*
- > Package [P2P]: I210 / I211 - 9.0*9.0mm; I225 / I226 - 7.0*7.0mm*



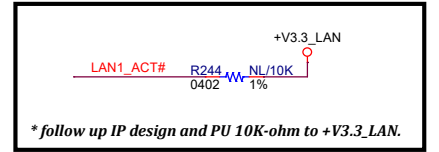
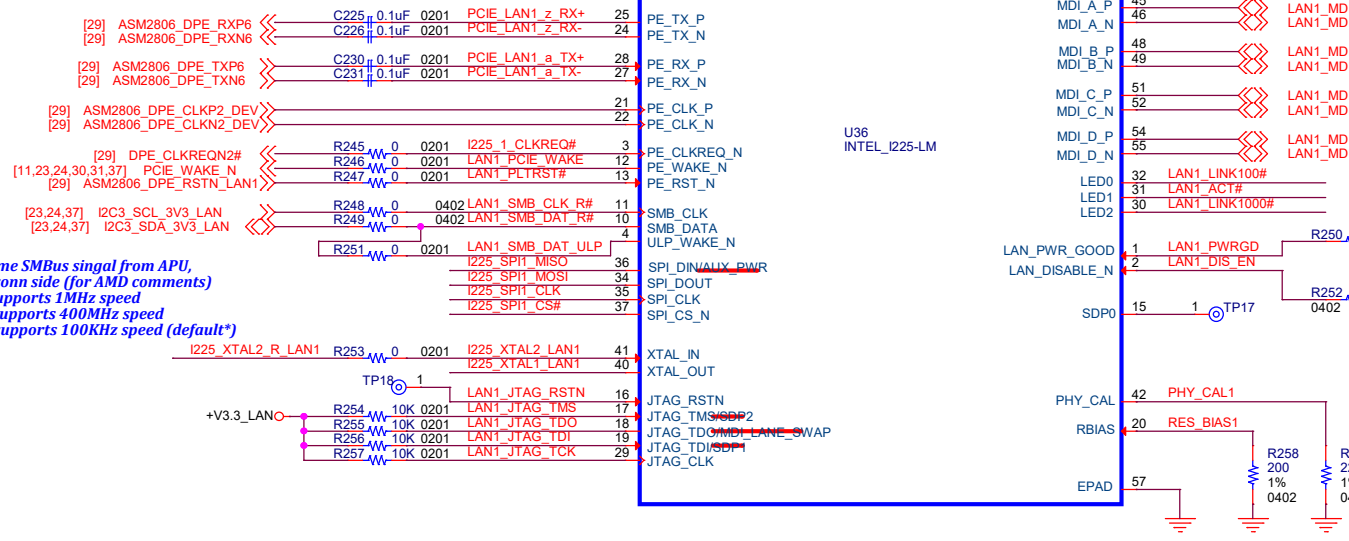
LAN Firmware Image

Ref 3534 I225-LM bin file version 1420054819

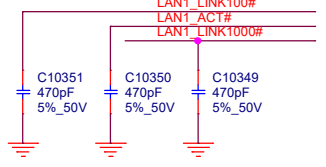
U37_IMG1
EEPROM ADB-1221.L 225LM V1.0 CS:1D38 W25Q16JVSNIQ



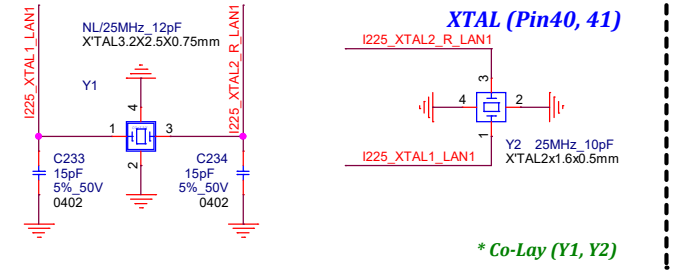
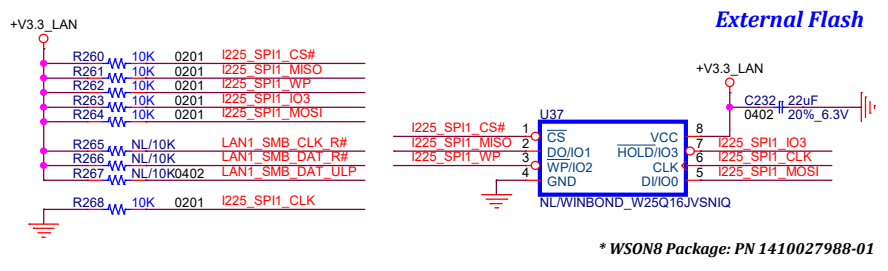
*** ULP_WAKE_N (Pin4):**
Connect this pin to SMBUS_DATA for supporting the RTD3 and the ULP Mode. If this signal is not used, pull-up this ULP_WAKE_N pin with a 10K-ohm resistor to 3.3V.



*** Intel 10/100 or 1GHz LAN Active/Link**
-> 2.5G/ 1G: Orange, 100: Green, 10: Dark



*** RBIAS (Pin20):**
-> The 22Kohm is required, an incorrect value impacts the PCIe interface.
*** PHY_CAL (Pin42):**
-> The 200ohm is required, an incorrect value impacts the PHY interface.



*** I225 vs. I226 different:**
Power reduction, optimization for test for supply, better BER cable performance, and enhanced temp range for IT-sku.
-> Temperature: -40 to 70C, but I226 can up to 85C. [2.5G]
-> I226 can dramatically reduced power consumption (20-50% reduction)
-> Resolution for minor bug fixes, and enhancements

ADVANTECH

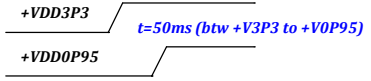
Title: **22_INTEL FOXVILLE I225-LM (1)**

Size: B PCB Name: **AIR-030_A101-1** Rev: **A101-1**

Date: Wednesday, August 10, 2022 Sheet: 22 of 48

Ethernet Controller2: INTEL I225-LM [Co-Lay I226]

* I211-AT: PN 1410023117-01 (Temp: 0~70C) / I225*: PN 1410029502-01 (Temp: -40~70C)
 * I210-IT: PN 1410022540-01 (Temp: -40~85C) / I210-AT: PN 1410022540-02 (Temp: 0~70C)
 -> integrated Non-Volatile Memory (iNVM) / External Flash*
 -> Package [P2P]: I210 / I211 - 9.0*9.0mm; I225 / I226 - 7.0*7.0mm*

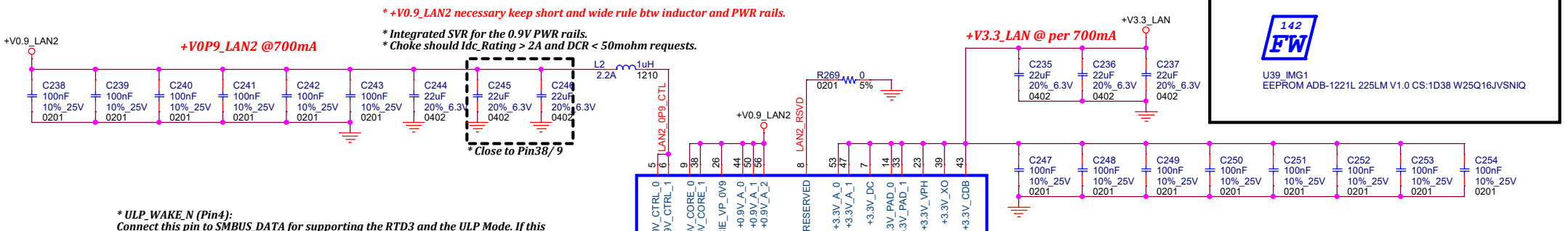


LAN Firmware Image

Ref 3534 I225-LM bin file version 1420054819



U39_IMG1
EEPROM ADB-1221L 225LM V1.0 CS:1D38 W25Q16JVSNIQ

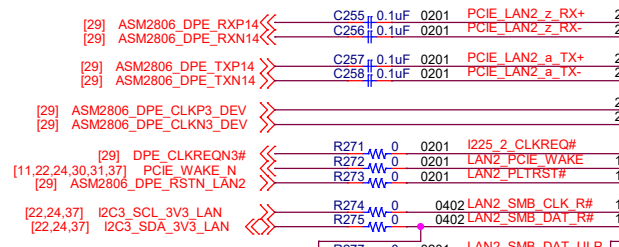


* +V0.9_LAN2 necessary keep short and wide rule btw inductor and PWR rails.

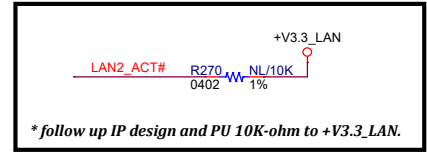
* Integrated SVR for the 0.9V PWR rails.
 * Choke should Idc_Rating > 2A and DCR < 50mohm requests.

+V3.3_LAN @ per 700mA

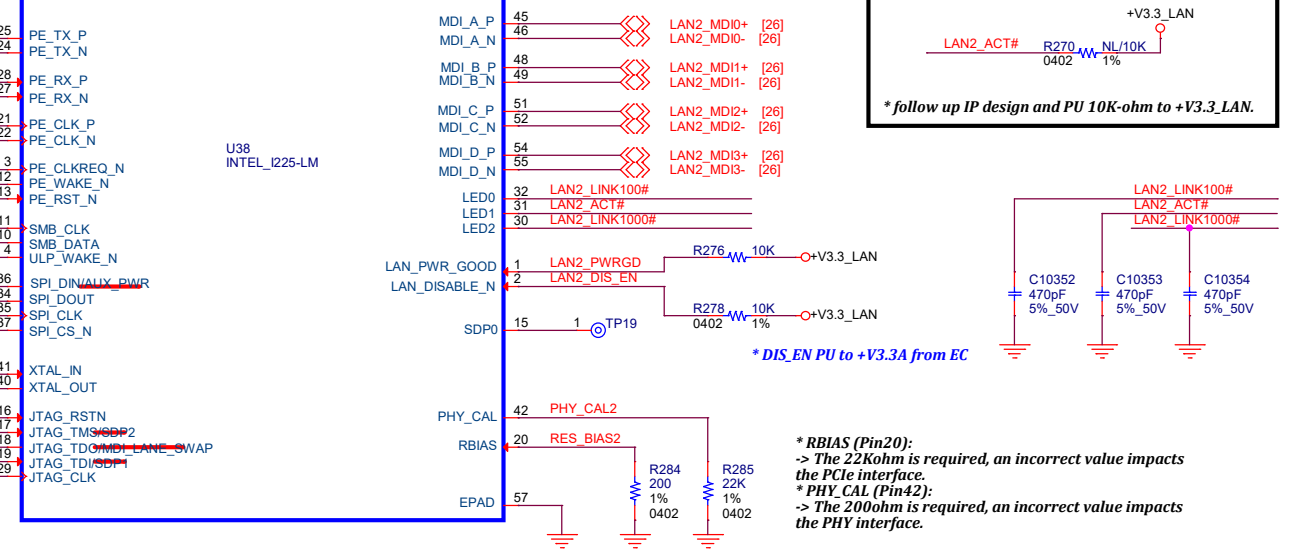
* ULP_WAKE_N (Pin4):
 Connect this pin to SMBUS_DATA for supporting the RTD3 and the ULP Mode. If this signal is not used, pull-up this ULP_WAKE_N pin with a 10K-ohm resistor to 3.3 V.



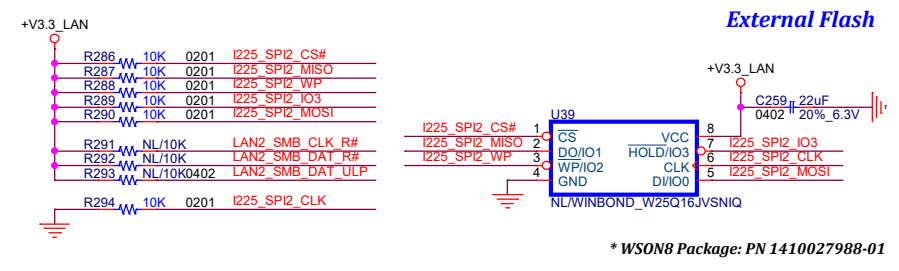
* Because LAN/ HDMI connect same SMBus signal from APU, therefore setup DNI part of LAN conn side (for AMD comments)
 -> 499-ohm (PN: 100000647) supports 1MHz speed
 -> 2.2K-ohm (PN: 100000642) supports 400MHz speed
 -> 10K-ohm (PN: 105A50103A) supports 100KHz speed (default)



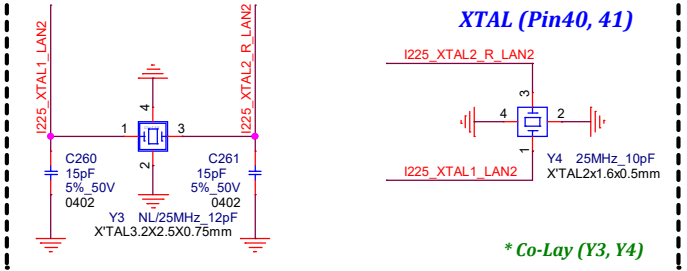
* follow up IP design and PU 10K-ohm to +V3.3_LAN.



* R_BIAS (Pin20):
 -> The 22Kohm is required, an incorrect value impacts the PCIe interface.
 * PHY_CAL (Pin42):
 -> The 200ohm is required, an incorrect value impacts the PHY interface.



* WSON8 Package: PN 1410027988-01



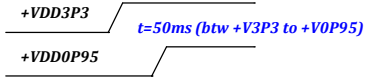
* Co-Lay (Y3, Y4)

* I225 vs. I226 different:
 Power reduction, optimization for test for supply, better BER cable performance, and enhanced temp range for IT-sku.
 -> Temperature: -40 to 70C, but I226 can up to 85C. [2.5G]
 -> I226 can dramatically reduced power consumption (20-50% reduction)
 -> Resolution for minor bug fixes, and enhancements

ADVANTECH		
23_INTEL FOXVILLE I225-LM (2)		
Size B	PCB Name	Rev
	AIR-030_A101-1	A101-1
Date:	Wednesday, August 10, 2022	Sheet 23 of 48

Ethernet Controller3: INTEL I225-LM [Co-Lay I226]

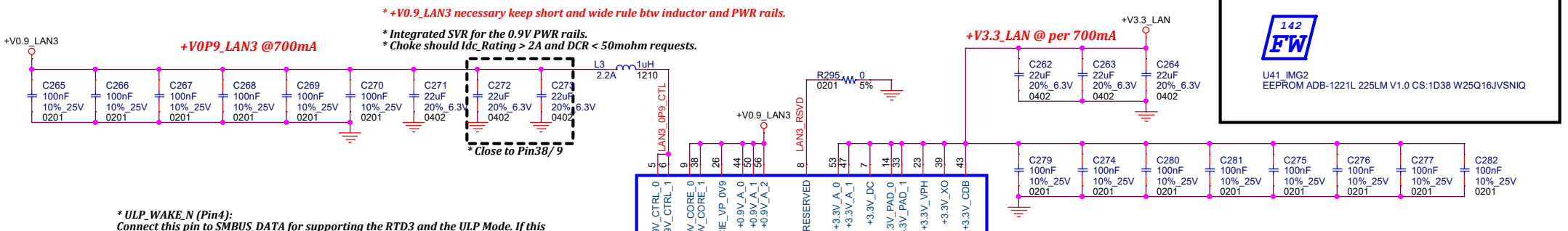
* I211-AT: PN 1410023117-01 (Temp: 0~70C) / I225*: PN 1410029502-01 (Temp: -40~70C)
 * I210-IT: PN 1410022540-01 (Temp: -40~85C) / I210-AT: PN 1410022540-02 (Temp: 0~70C)
 -> integrated Non-Volatile Memory (iNVM) / External Flash*
 -> Package [P2P]: I210 / I211 - 9.0*9.0mm; I225 / I226 - 7.0*7.0mm*



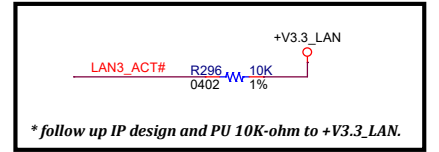
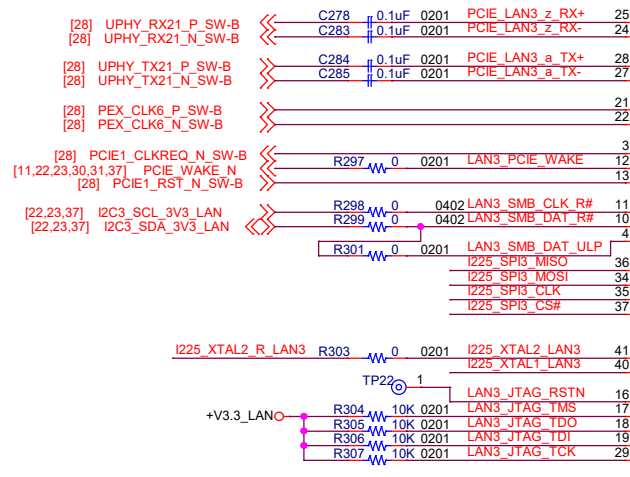
LAN Firmware Image

Ref 3534 I225-LM bin file version 1420054819

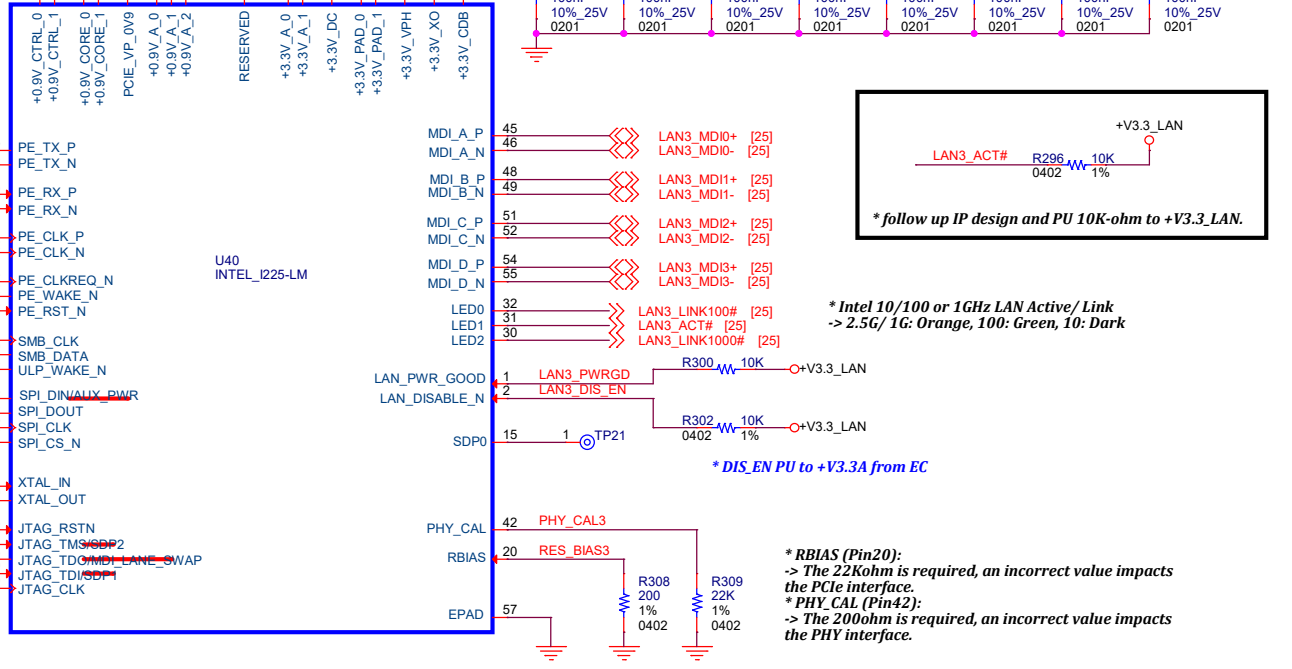
U41_IMG2
 EEPROM ADB-1221L 225LM V1.0 CS:1D38 W25Q16JVSNIQ



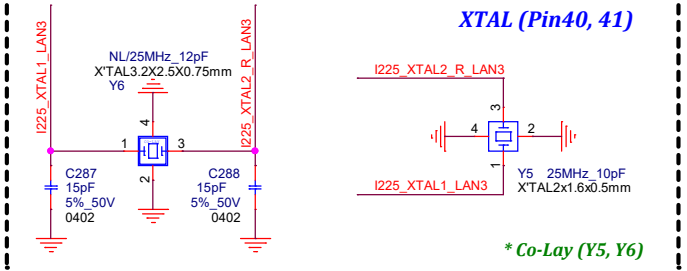
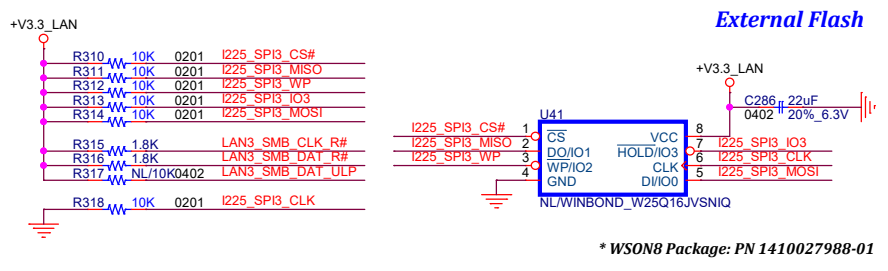
* ULP_WAKE_N (Pin4):
 Connect this pin to SMBUS_DATA for supporting the RTD3 and the ULP Mode. If this signal is not used, pull-up this ULP_WAKE_N pin with a 10K-ohm resistor to 3.3 V.



* Intel 10/100 or 1GHz LAN Active/Link
 -> 2.5G: 1G: Orange, 100: Green, 10: Dark



>> ASM2806_DPE_RSTN_LAN2 [23,29]



* I225 vs. I226 different:
 Power reduction, optimization for test for supply, better BER cable performance, and enhanced temp range for IT-sku.
 -> Temperature: -40 to 70C, but I226 can up to 85C. [2.5G]
 -> I226 can dramatically reduced power consumption (20-50% reduction)
 -> Resolution for minor bug fixes, and enhancements

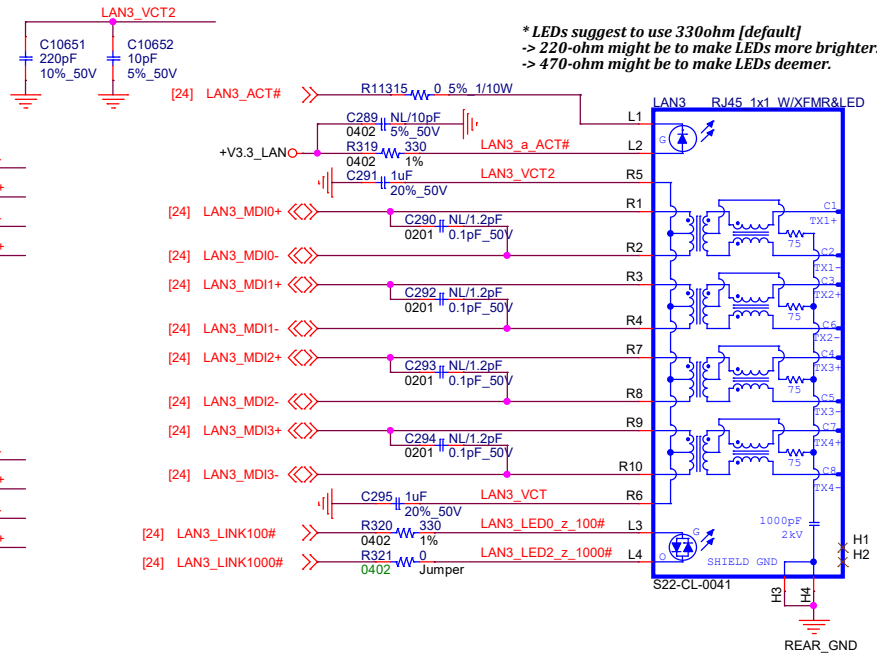
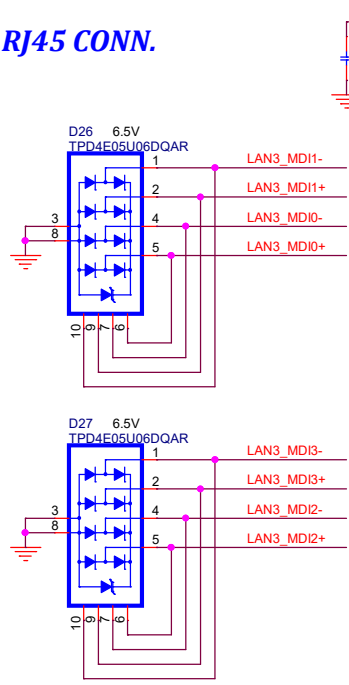
ADVANTECH

Title: **24_INTEL FOXVILLE I225-LM (3)**

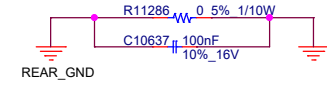
Size: B PCB Name: **AIR-030_A101-1** Rev: **A101-1**

Date: Wednesday, August 10, 2022 Sheet: 24 of 48

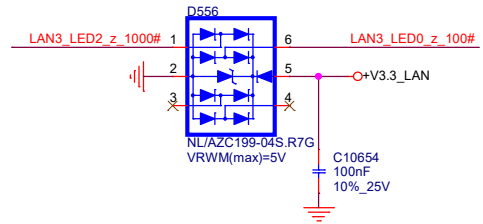
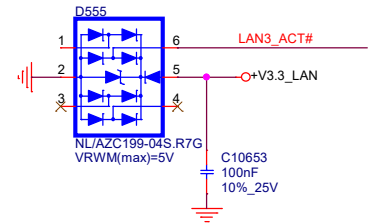
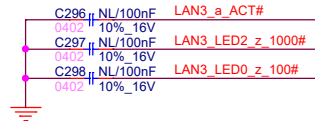
LAN3 RJ45 CONN.



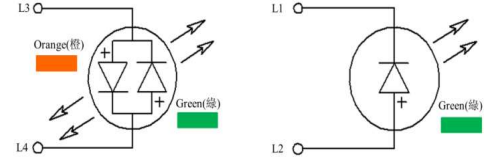
* LEDs suggest to use 330ohm [default]
-> 220-ohm might be to make LEDs more brighter.
-> 470-ohm might be to make LEDs deemer.



EMI design by connector side

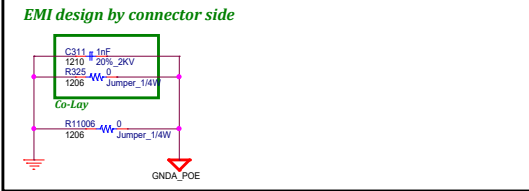
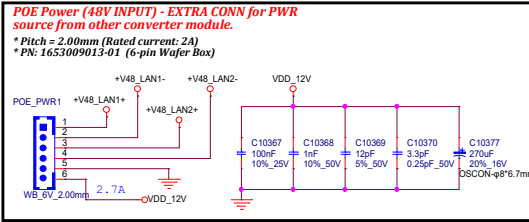


* LAN1 PN: 1654015170-01, up to 2.5GHz

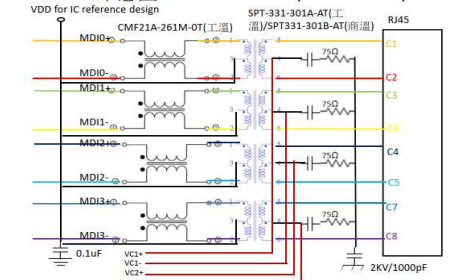


ADVANTECH		
Title 25_LAN3 CONN [RJ45]		
Size B	PCB Name AIR-030_A101-1	Rev A101-1
Date:	Wednesday, August 10, 2022	Sheet 25 of 48

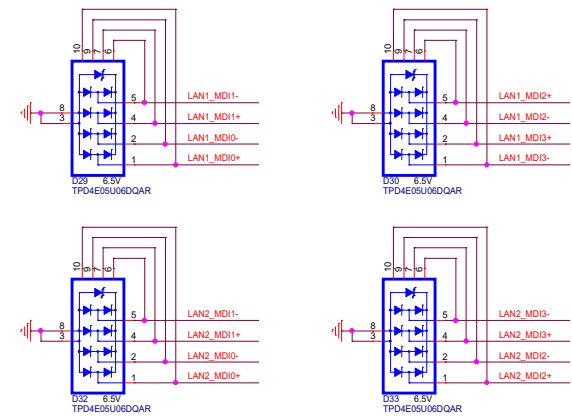
LAN2/ LAN3 RJ45 CONN. (Alt. POE) - Only choose one LAN for PoE Application



POE (PSE) module , 96965376010 ASS'Y MIO-5376 POE BD A101-1 for PWR Boost



EMI Design by connector side



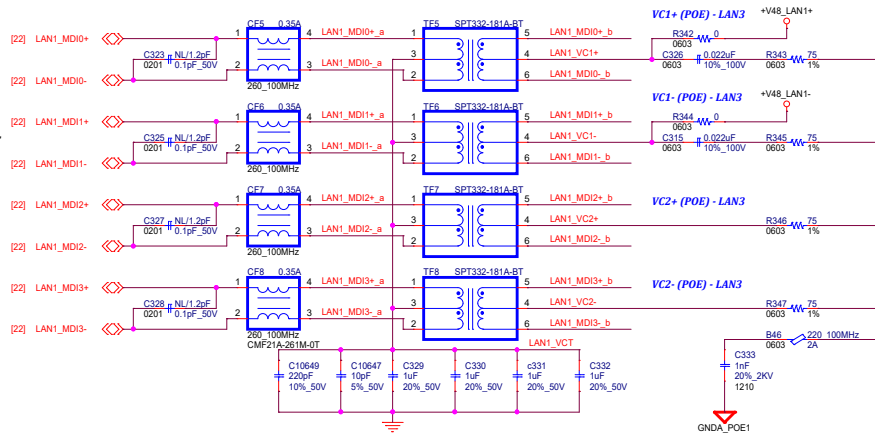
* The ESD protection should connect to digital GND!
 -> the ESD line to GND could cause "Hi-Pot" fail if connect to GND_POE signal.

[CMF(PN: 1212004436-01) + SPT(PN: 1252003343-01)] Design Parts -> for Bob Smith Termination

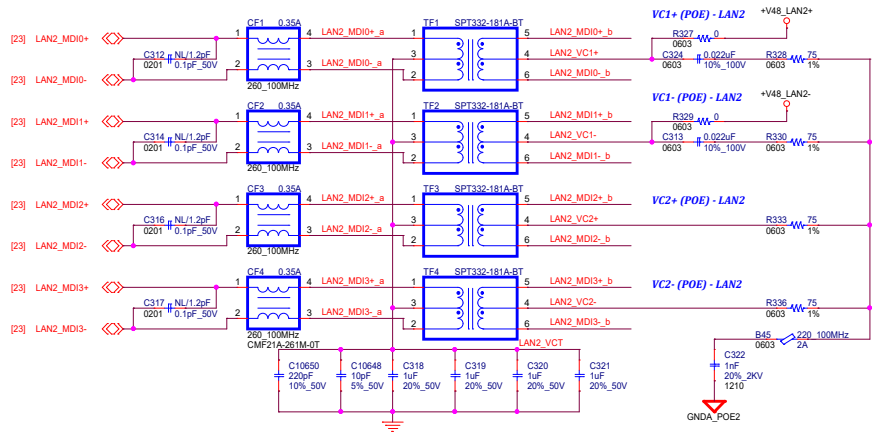
* [First solution] integrated "xfrm + common-mode filter" size: 10.00*15.10*5.80mm (PN: 1252003031-01) -> but met placement issue.
 * [Second solution] Divide to single CMF & SPT designs schematic - for Bob's Smith Theory.
 * IEEE 802.3AT Compliant Performance for POE application with 720mA capability

* while +V48_PoE PWR will not connect by external conn (power source), then the LAN2/ LAN3 become to normal RJ45 LAN functional.

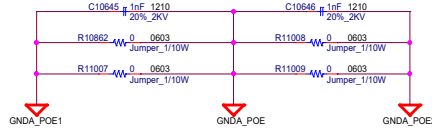
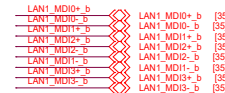
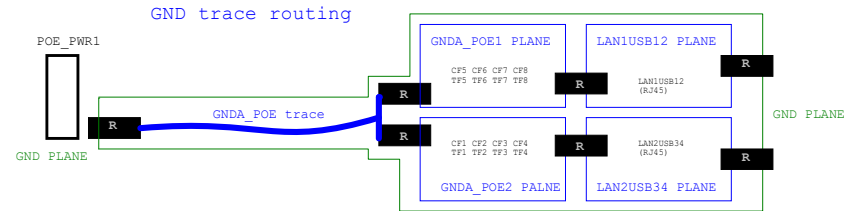
* Reference Rails for 1225-LM (LAN Chip)



* Reference Rails for 1225-LM (LAN Chip)



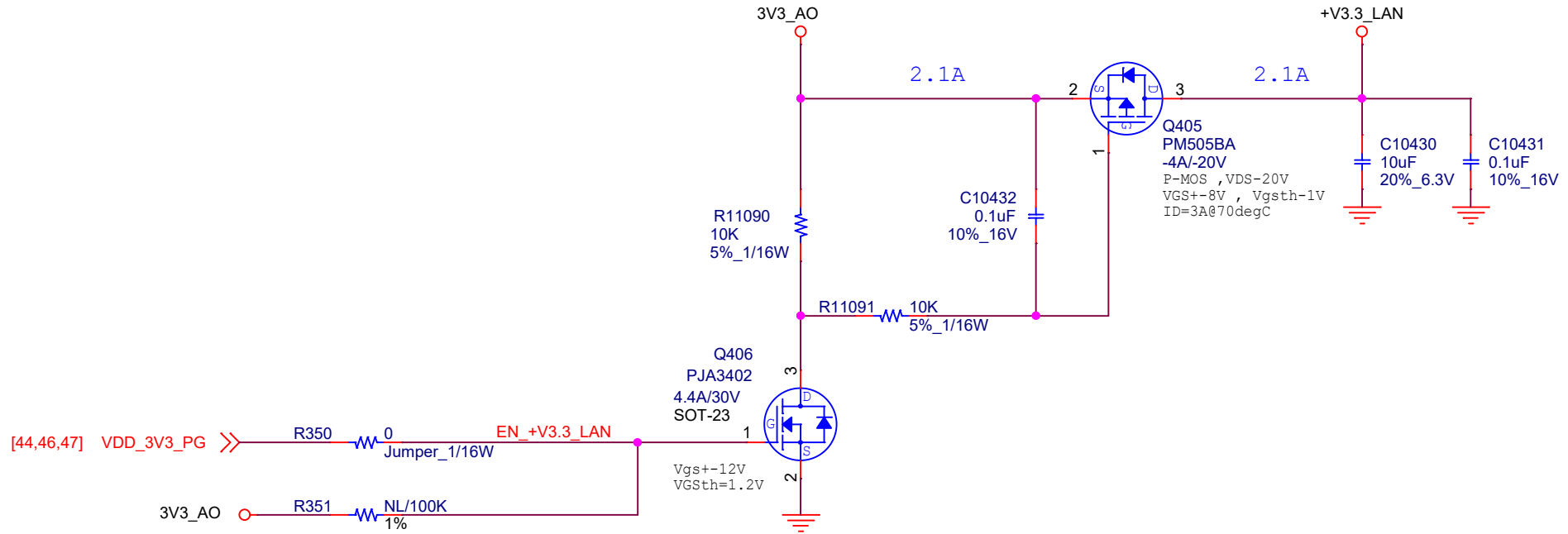
Pure LAN CONN /w TWO USB3.2 GEN2. - 1654015250-01



ADVANTECH			
Title	26_LAN1/2 CONN [RJ45 Alt.PoE]		
Size	PCB Name	AIR-030_A101-1	
Date:	Wednesday, August 10, 2022	Sheet	26 of 48

+V3.3_LAN (per 700mA) @2.1A

PWR - +V3.3_LAN



PWR Consumption	I225 (B-Step)	I226 (C-Step)
TDP (@2.5Gbps)	2200mW	TBD
Active (@1Gbps)	817mW	675mW
EEE @2500Mbps	934mW	625mW
EEE @1000Mbps	313mW	250mW
EEE @100Mbps	227mW	185mW
No Link	5mW	5mW

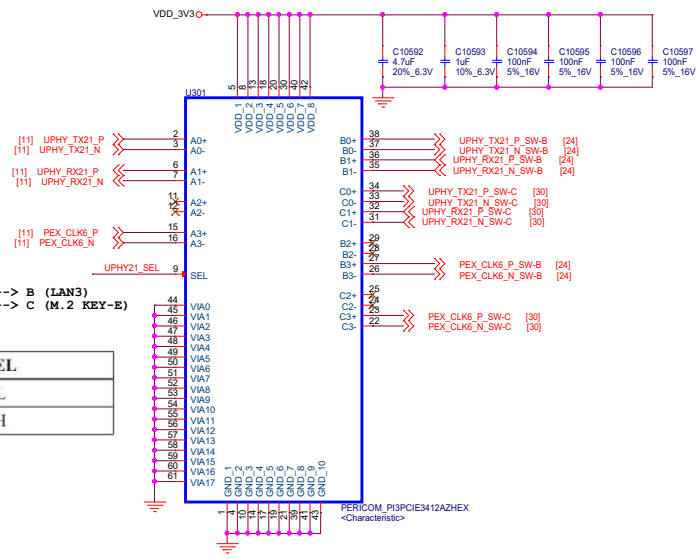
ADVANTECH

Title: **27_PWR +V3.3_LAN Rails**

Size A PCB Name: **AIR-030_A101-1** Rev: **A101-1**

Date: Wednesday, August 10, 2022 Sheet 27 of 48

PCIEx1 MUX_DEMUX



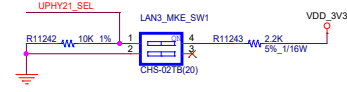
Truth Table

Function	SEL
A _N to B _N	L
A _N to C _N	H

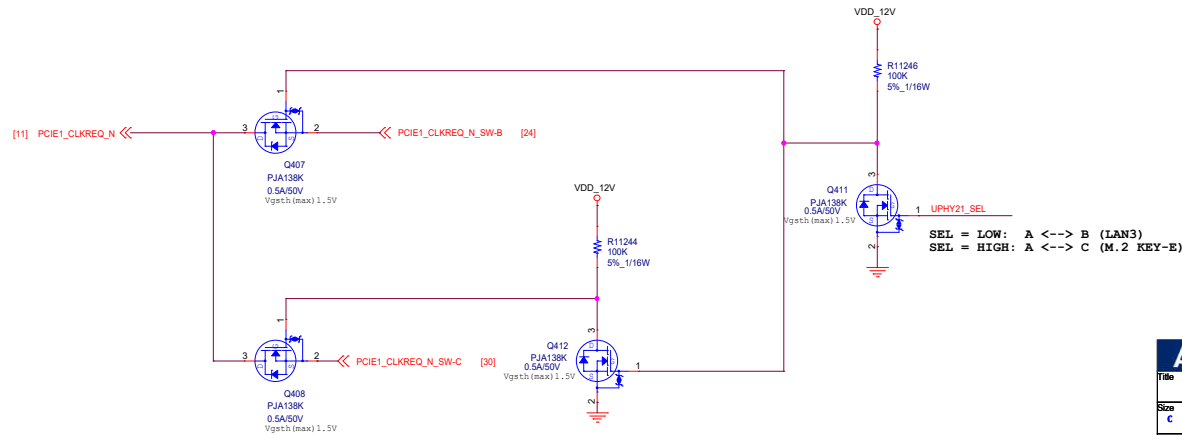
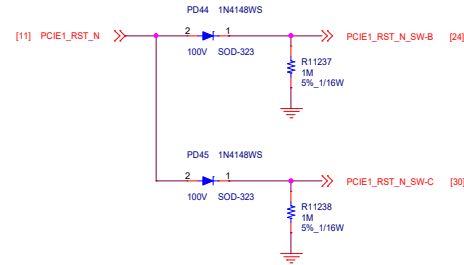
SEL = LOW: A <-> B (LAN3)
 SEL = HIGH: A <-> C (M.2 KEY-E)

LAN3 & M.2 KEY-E PCIe Selector

(DIP SW place BOT side)

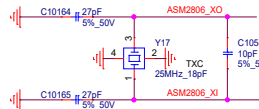


SW1	SW2	PCIe Function
ON	-	PCIe switch to M.2-E (LAN3 disable)
OFF	-	PCIe switch to LAN3 (M.2-E disable)

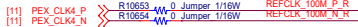


PCIe Bridge (ASM2806)

Crystal 3225 SMD



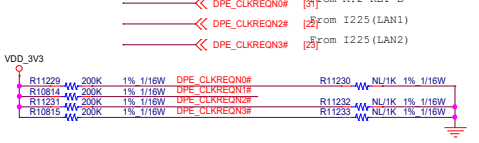
CLOCK INPUT



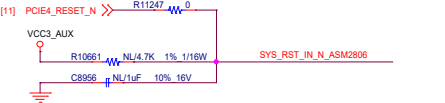
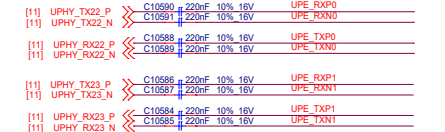
CLOCK OUTPUT



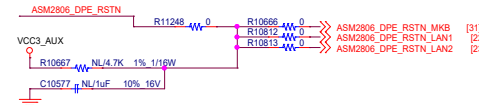
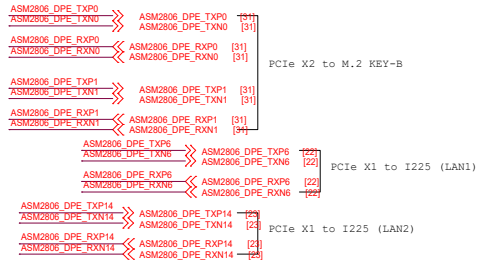
CLOCK REQUEST



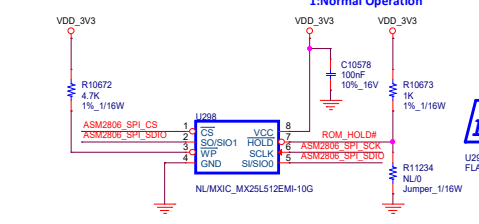
PCIe Upstream



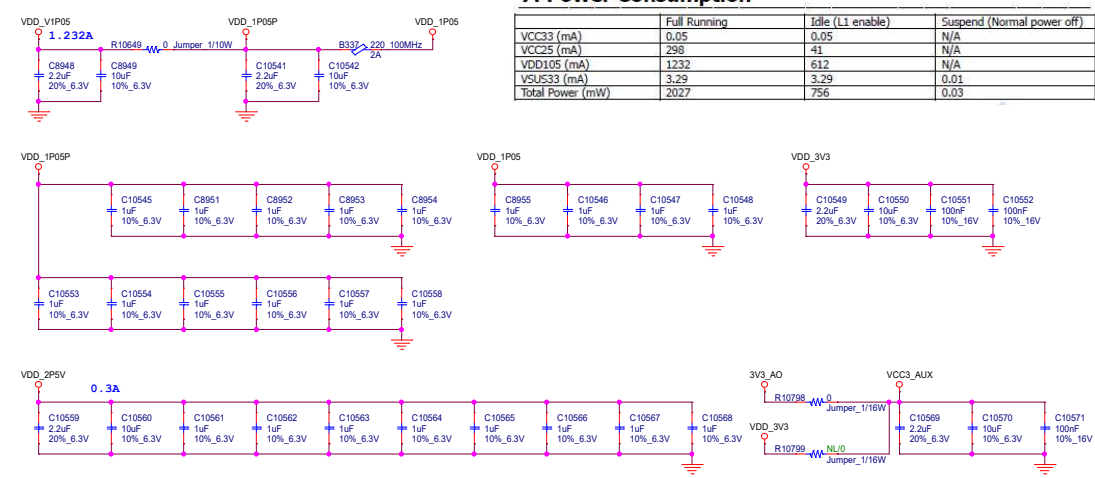
PCIe Downstream



SPI FLASH



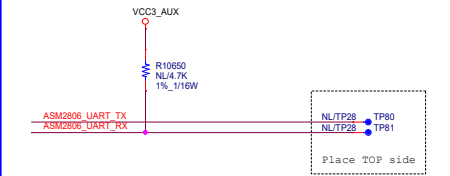
Power



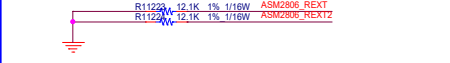
7. Power Consumption

	Full Running	Idle (L1 enable)	Suspend (Normal power off)
VCC33 (mA)	0.05	0.05	N/A
VCC25 (mA)	298	41	N/A
VDD105 (mA)	1232	612	N/A
V5US33 (mA)	3.29	3.29	0.01
Total Power (mW)	2027	756	0.03

UART For Debug

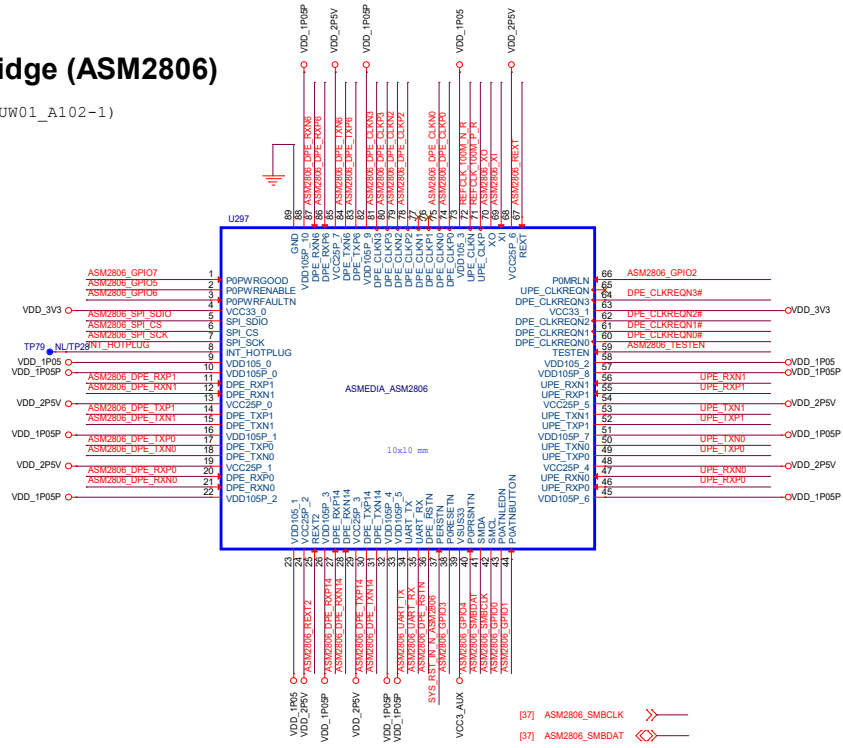


External Reference Resistor 12.1K Ohm



PCIe Bridge (ASM2806)

(Refer NMC-UW01_A102-1)



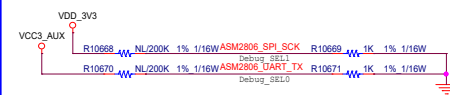
HW STRAPPING ASM2806 PCIe Lane Configuration :



ASM2806 PCIe lane configuration:

STRAPPING BIT	GPIO5	SPI_SDIO	LANE0	LANE1	LANE6	LANE14
PECLK Mapping	LANE0	LANE1	LANE2	LANE3		
1	1	x1	x1	x1	x1	
0	0		x2	x1	x1	

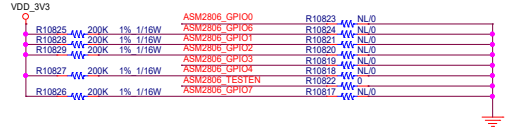
HW STRAPPING ASM2806 CLOCK MODE SELECT: SPI_SCK, UART_TX



Clock mode select: SPI_SCK, UART_TX

Strapping bit	Upstream Clock
SPI_SCK	0 : 100MHz diff 1 : OSC
Strapping bit	Downstream Clock
UART_TX	0 : 100MHz diff 1 : OSC

GPIO/MISC Config



M.2 KEY-E (2230)

UART5 path selector

UART5_SW1 , PAGE16

SW1	SW2	Function
ON	X	COM5 ENABLE , M.2-E BT DISABLE
OFF	X	COM5 DISABLE , M.2-E BT ENABLE

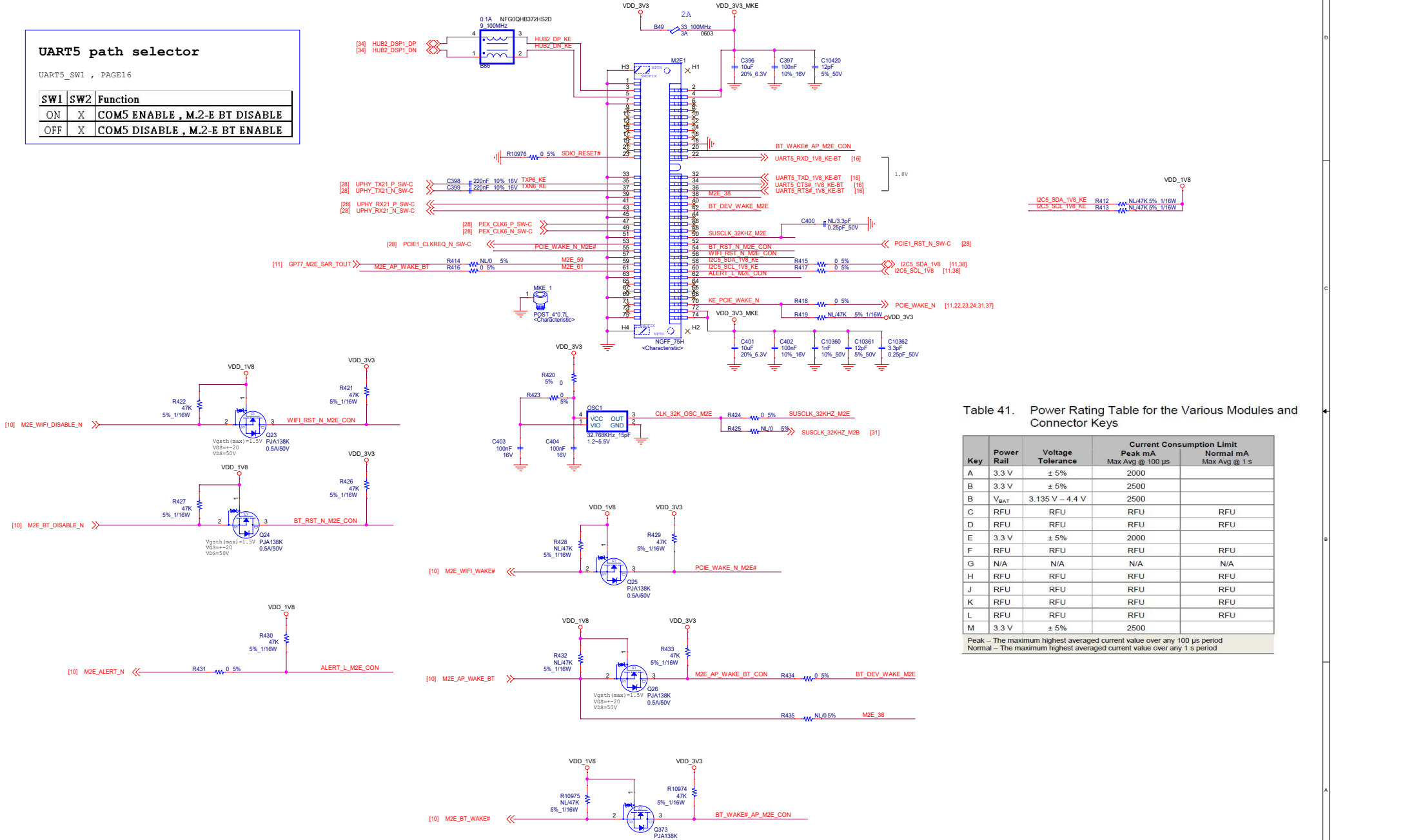


Table 41. Power Rating Table for the Various Modules and Connector Keys

Key	Power Rail	Voltage Tolerance	Current Consumption Limit	
			Peak mA Max Avg @ 100 μs	Normal mA Max Avg @ 1 s
A	3.3 V	± 5%	2000	
B	3.3 V	± 5%	2500	
B	V _{BAT}	3.135 V – 4.4 V	2500	
C	RFU	RFU	RFU	RFU
D	RFU	RFU	RFU	RFU
E	3.3 V	± 5%	2000	
F	RFU	RFU	RFU	RFU
G	N/A	N/A	N/A	N/A
H	RFU	RFU	RFU	RFU
J	RFU	RFU	RFU	RFU
K	RFU	RFU	RFU	RFU
L	RFU	RFU	RFU	RFU
M	3.3 V	± 5%	2500	

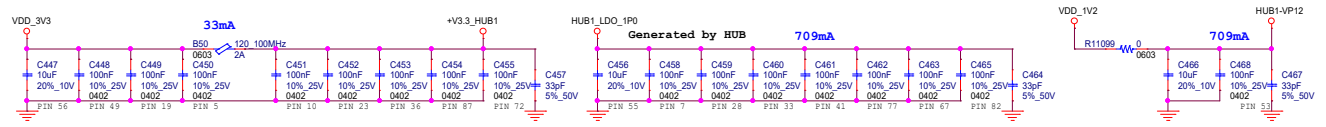
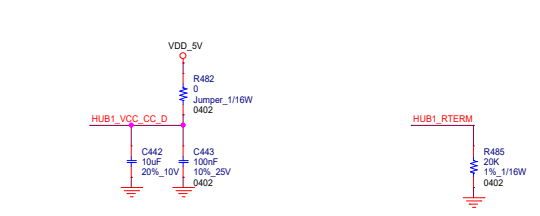
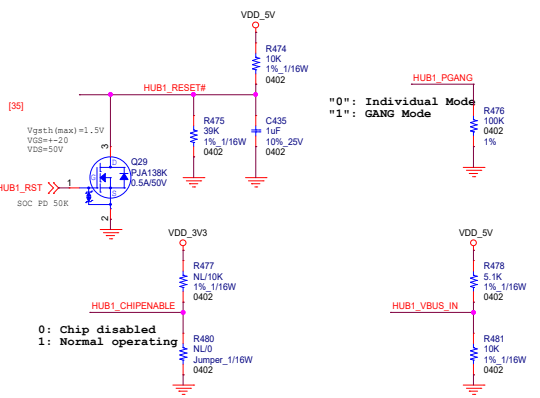
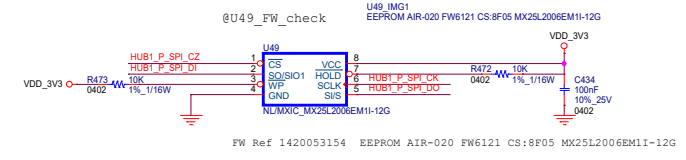
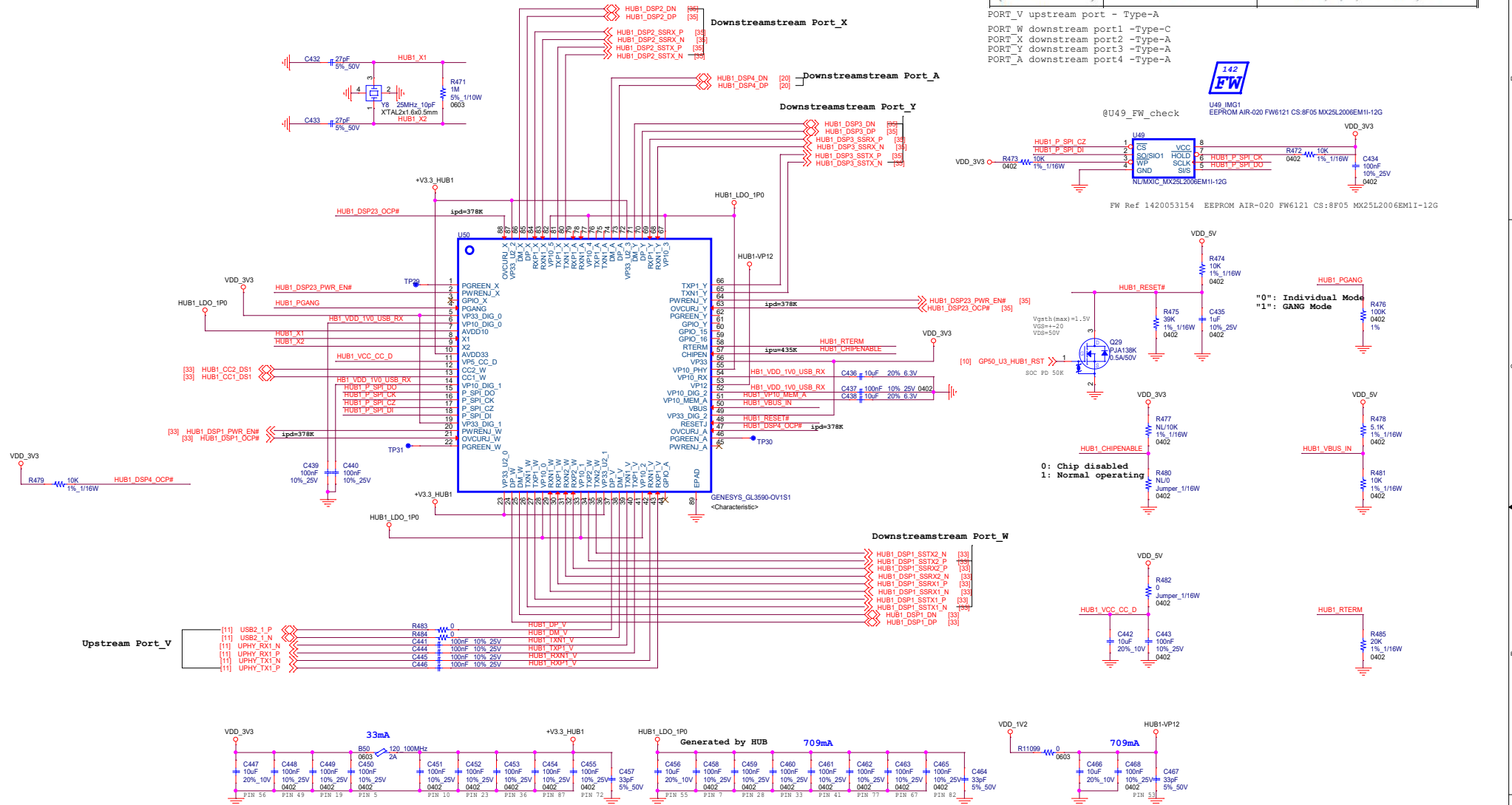
Peak – The maximum highest averaged current value over any 100 μs period
 Normal – The maximum highest averaged current value over any 1 s period

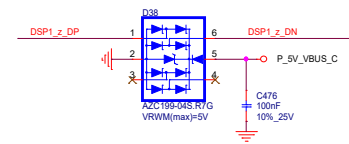
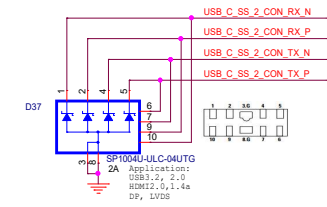
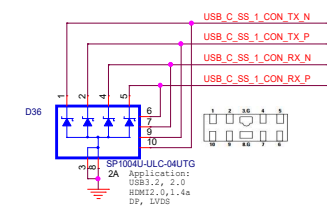
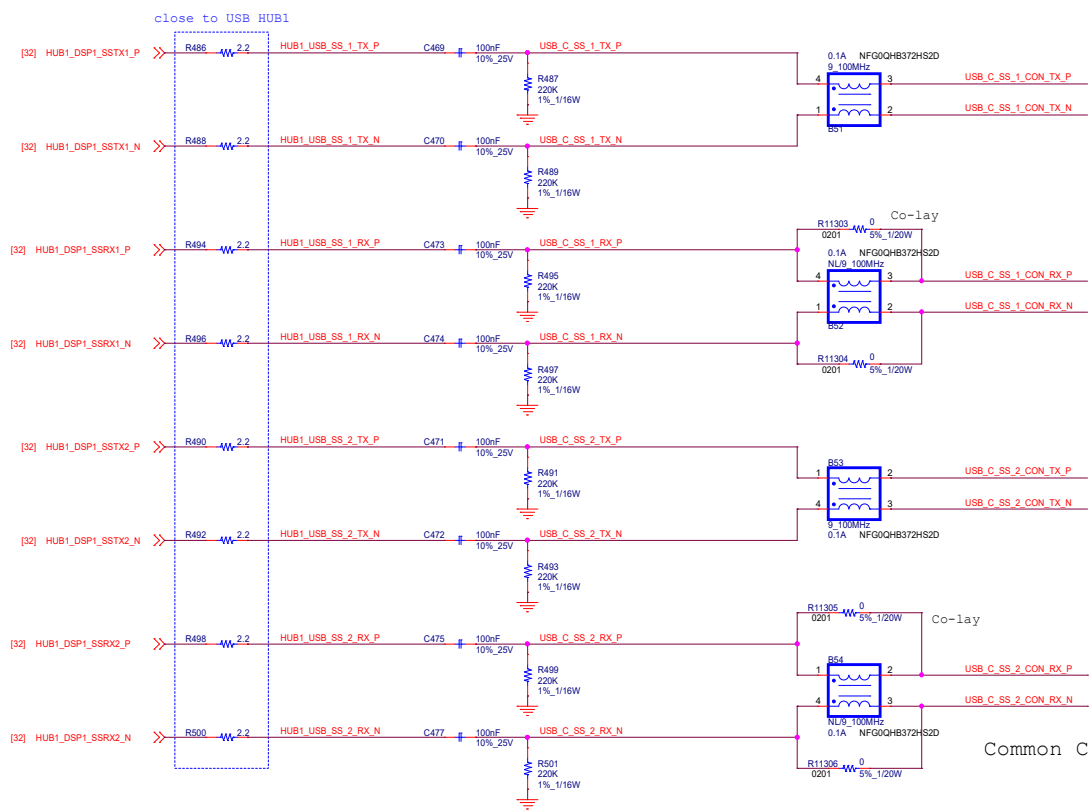
USB3.2 HUB1 GL3590

(Refer AIR-020)

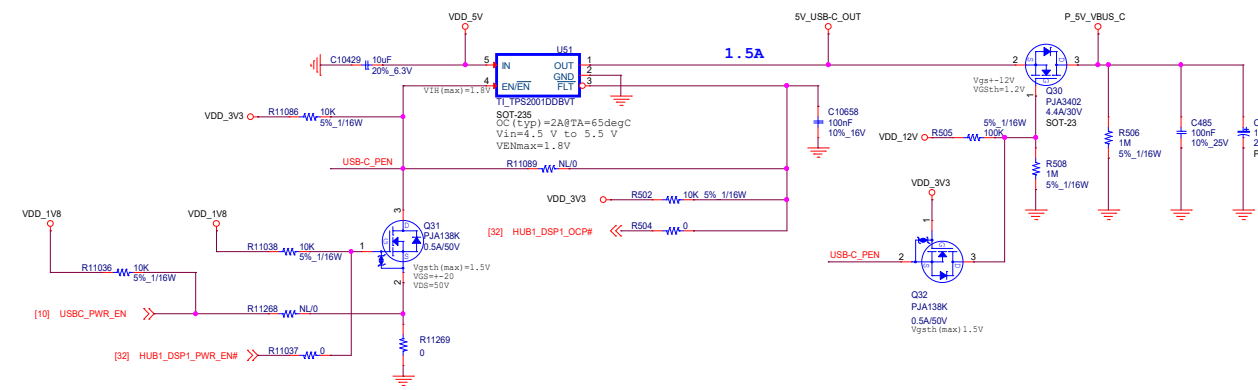
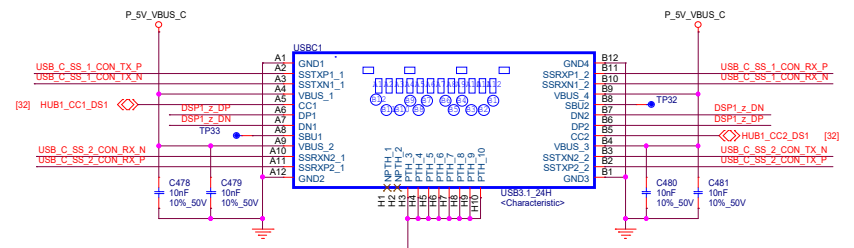
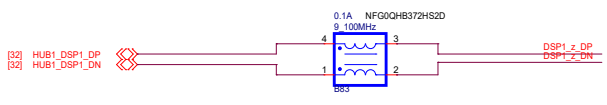
Package Type	Total Ports (UFP+DFP)	Port Type and Operating Speed
QFN88 (GL3590-OV1S1)	1 USB-C SS+ 4 USB-A SS+	Port W: USB-C, SS+ Port V, X, Y, A: USB-A, SS+

PORT_V upstream port - Type-A
 PORT_W downstream port1 -Type-C
 PORT_X downstream port2 -Type-A
 PORT_Y downstream port3 -Type-A
 PORT_A downstream port4 -Type-A





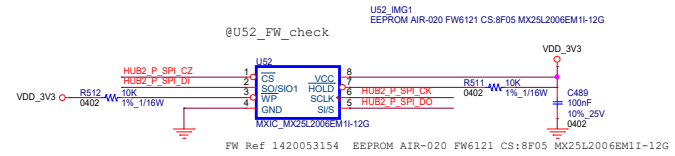
Common Choke follow NVIDIA ORIN DG_V1.0



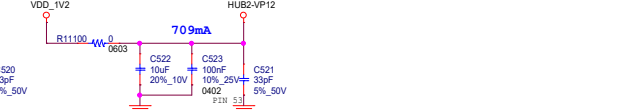
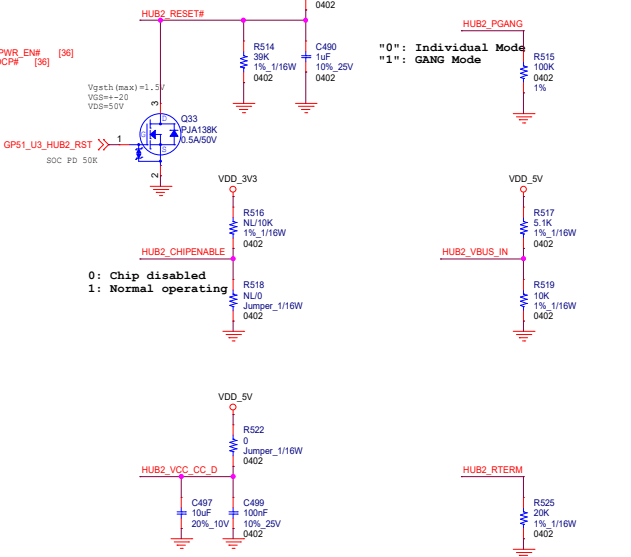
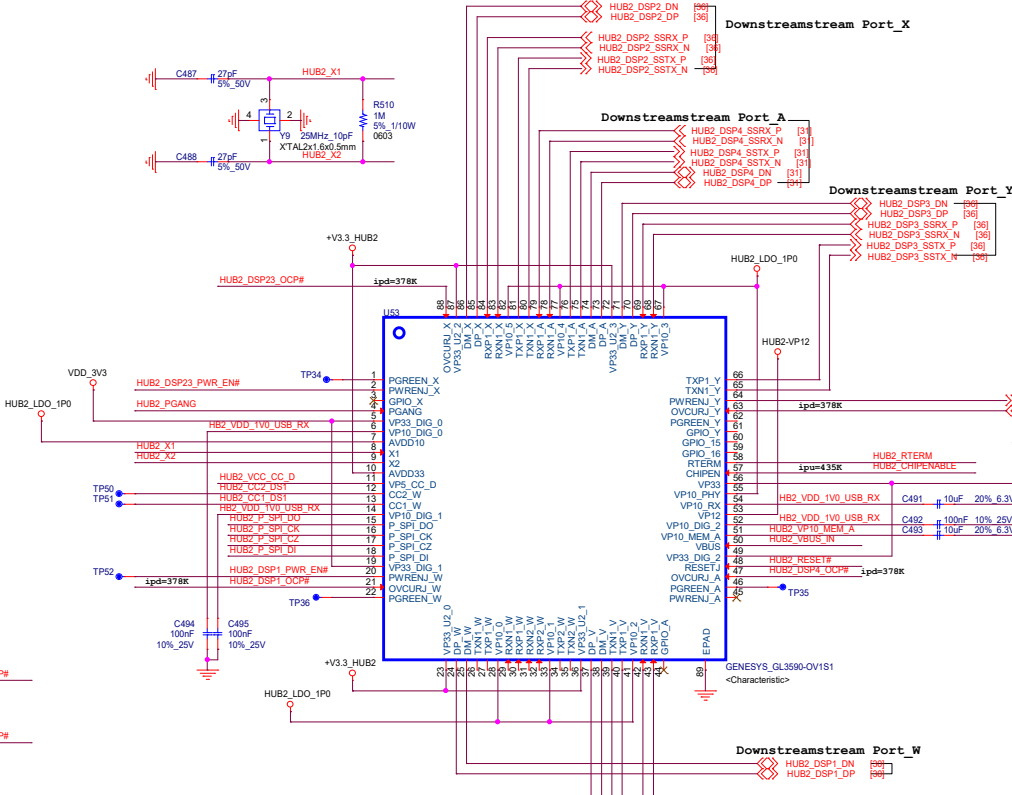
USB3.2 HUB2 GL3590

Package Type	Total Ports (UFP+DFP)	Port Type and Operating Speed
QFN88 (GL3590-OV1S1)	1 USB-C SS+ 4 USB-A SS+	Port W: USB-C, SS+ Port V, X, Y, A: USB-A, SS+

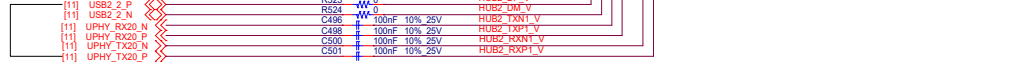
PORT_V upstream port - Type-A
 PORT_W downstream port1 -Type-C
 PORT_X downstream port2 -Type-A
 PORT_Y downstream port3 -Type-A
 PORT_A downstream port4 -Type-A



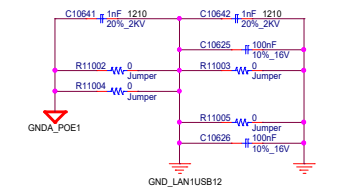
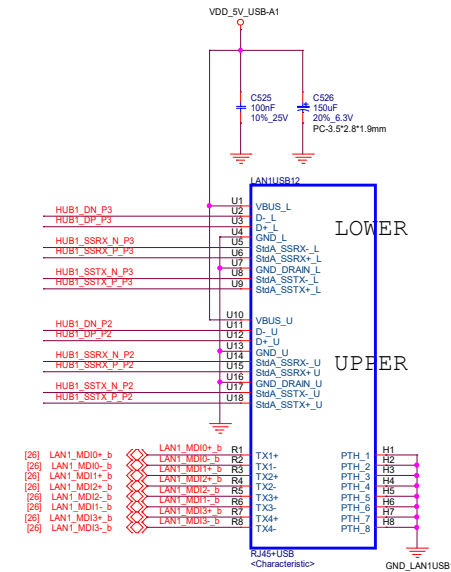
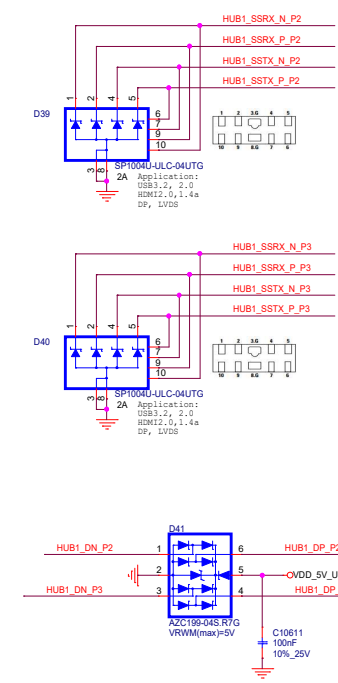
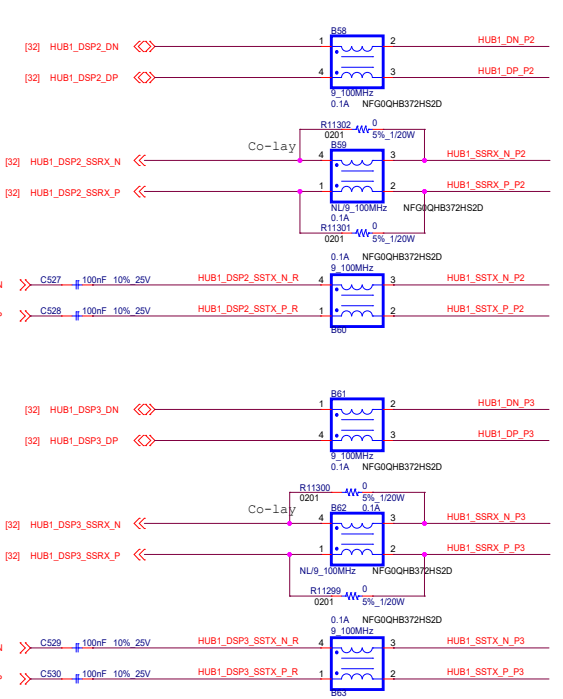
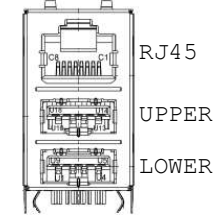
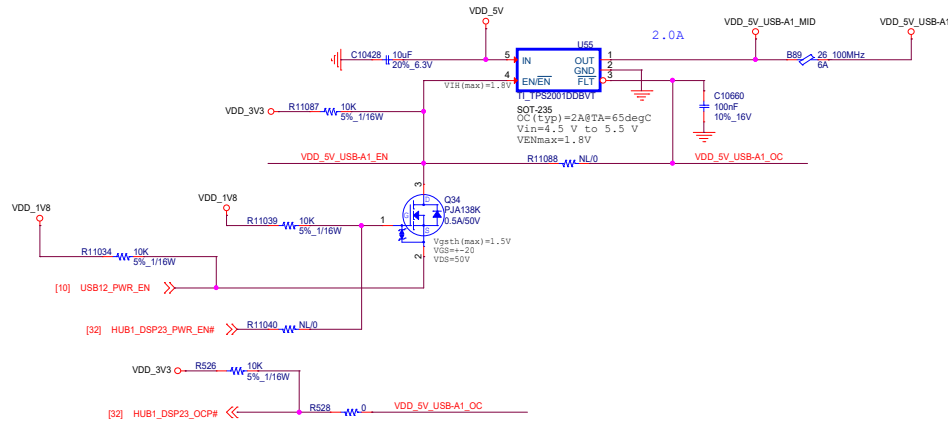
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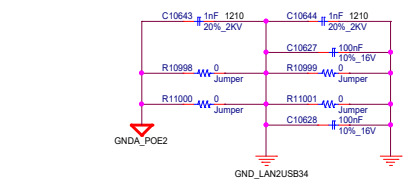
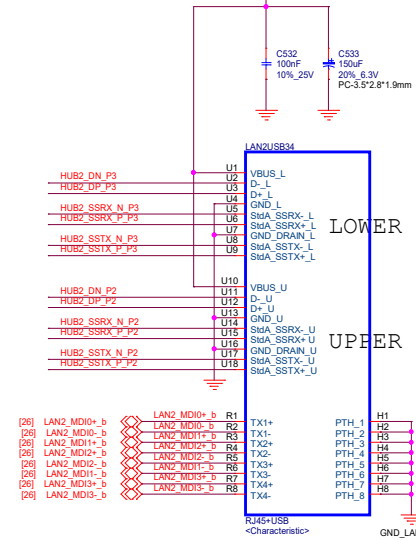
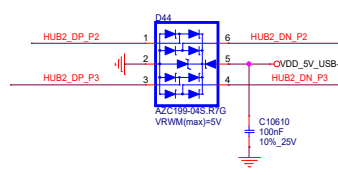
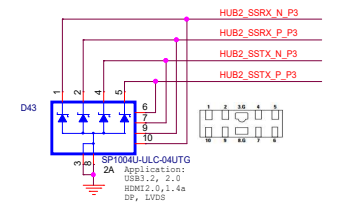
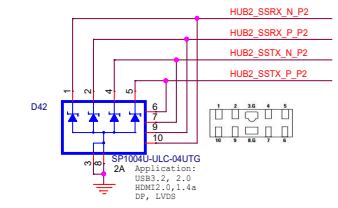
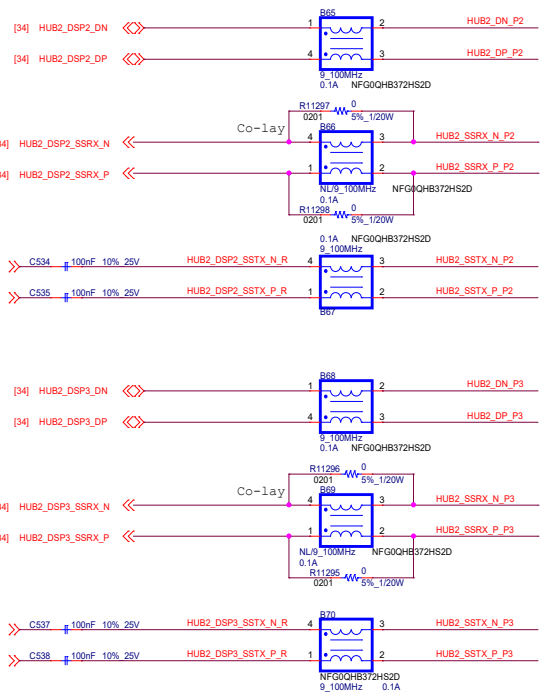
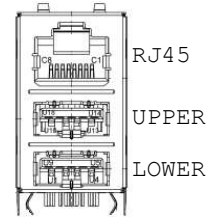
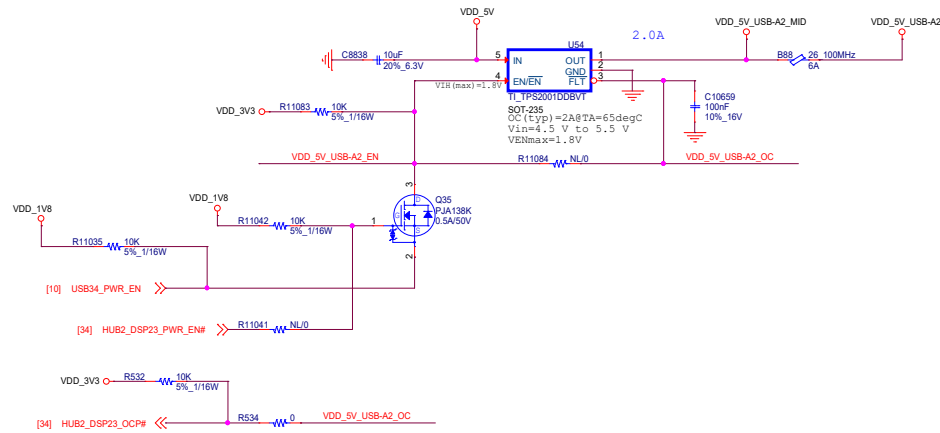
Upstream Port_V



USB3.1 TYPE-A x2 (A)



USB3.1 TYPE-A x2 (A)



PCIe4.0 X16 CONN (X8 SIGNAL)

(IP NO:28 / IP VER: 1)

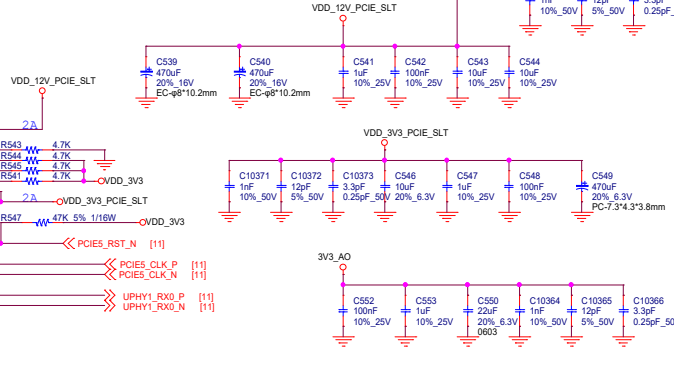
PCI EXPRESS CARD ELECTROMECHANICAL SPECIFICATION, REV. 2.0

Table 4-1: Power Supply Rail Requirements

Power Rail	10 W Slot	25 W Slot	75 W Slot
+3.3V			
Voltage tolerance	± 9% (max)	± 9% (max)	± 9% (max)
Supply Current	3.0 A (max)	3.0 A (max)	3.0 A (max)
Capacitive Load	1000 µF (max)	1000 µF (max)	1000 µF (max)
+12V			
Voltage tolerance	± 8%	± 8%	± 8%
Supply Current	0.5 A (max)	2.1 A (max)	5.5 A (max)
Capacitive Load	300 µF (max)	1000 µF (max)	2000 µF (max)
+3.3Vaux			
Voltage tolerance	± 9% (max)	± 9% (max)	± 9% (max)
Supply Current	375 mA (max)	375 mA (max)	375 mA (max)
Wakeup Enabled	20 mA (max)	20 mA (max)	20 mA (max)
Non-wakeup Enabled	20 mA (max)	20 mA (max)	20 mA (max)
Capacitive Load	150 µF (max)	150 µF (max)	150 µF (max)

Table 4-2: Add-in Card Power Dissipation

Standard height	X1		x4/x8		x16	
	10 W ¹ (max)	25 W ¹ (max)	25 W (max)	25 W ² (max)	75 W ² (max)	75 W ² (max)
Low profile card ³	10 W (max)	25 W (max)	25 W (max)	25 W (max)	25 W (max)	25 W (max)



PCIe 75W SLOT
 3.3V request 1000uF,
 470uF on carrier board, 470uF on riser card
 12V request 2000uF,
 1000uF on carrier board, 1000uF on riser card

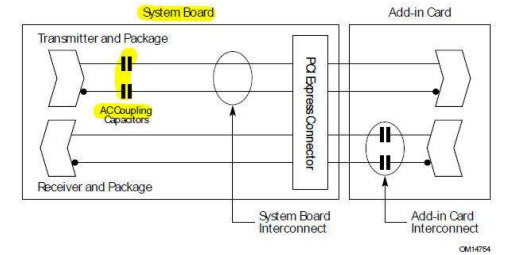
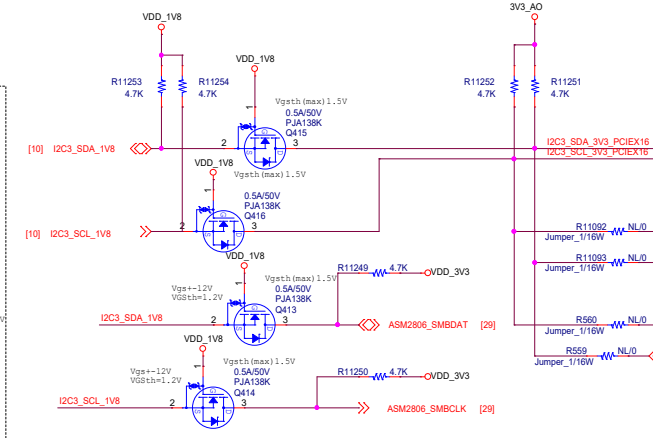
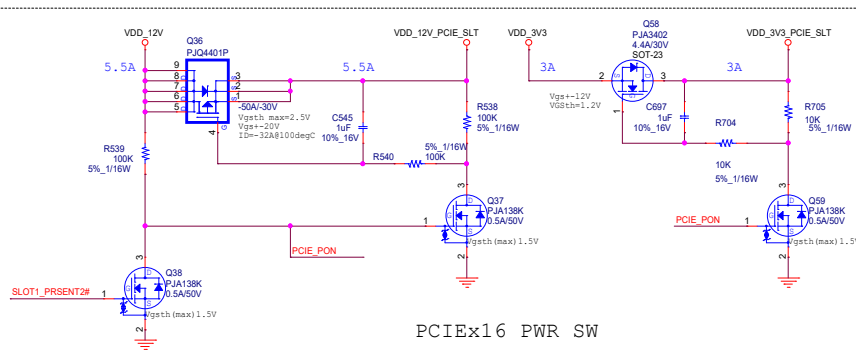
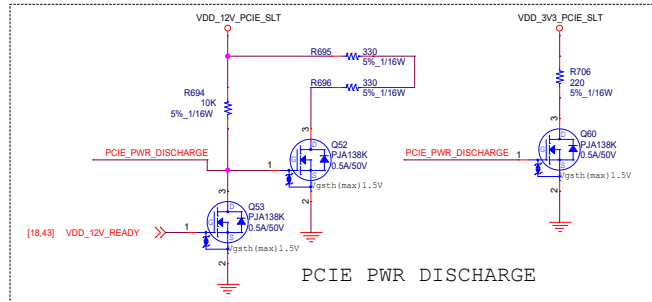


Figure 1848: Link Definition for Two Components

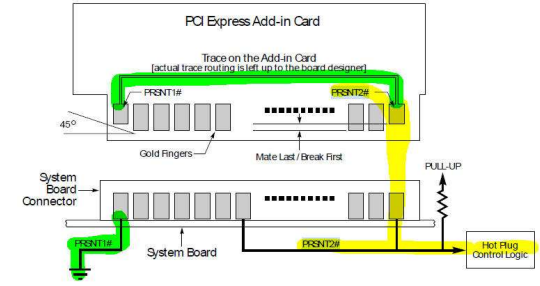


Figure 1444: Presence Detect in a Hot-Plug Environment

ADVANTECH

Title: **37_PCIE4.0 X16 CONN (X8 SIGNAL)**

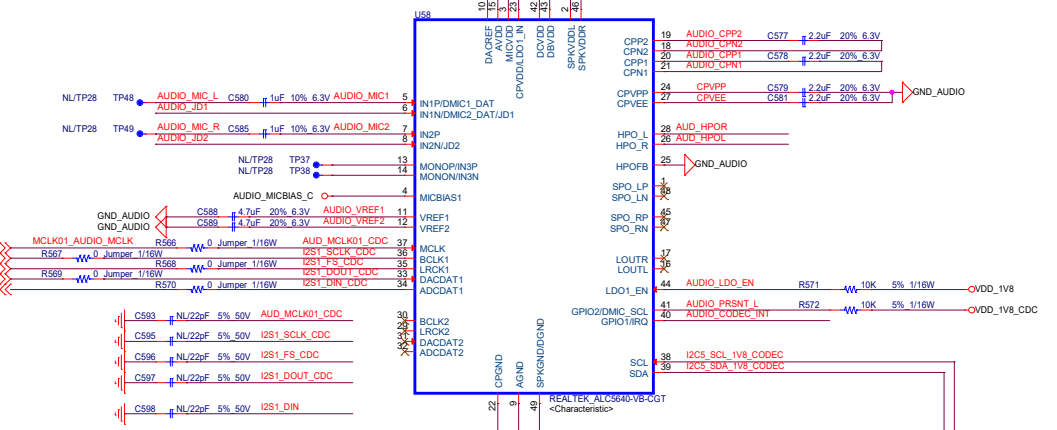
Size: Document Number **AIR-030** Rev: **A101-1**

Date: Wednesday, August 10, 2022 Sheet 37 of 48

AUDIO CODEC REALTEK ALC5640

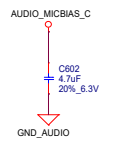
(Refer Jetson_AGX_Orin_Developer_Kit_Carrier_Board_Design_Files_A04)

DBVDD, AVDD, DACREF, CPVDD => 1.8V
 DCVDD => 1.2V
 MICVDD = 3.3V
 SPKVDD = 5V



[10] MCLK01_AUDIO_MCLK
 [10] I2S1_SCLK
 [10] I2S1_FS
 [10] I2S1_DOUT
 [10] I2S1_DIN

ALC5640 I2S level follow by DBVDD power rail



[10] CODEC_INT

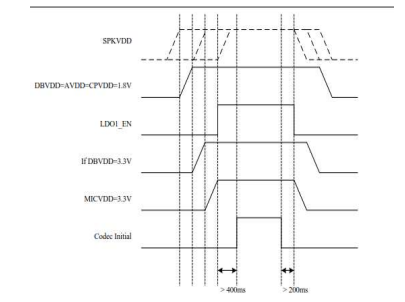
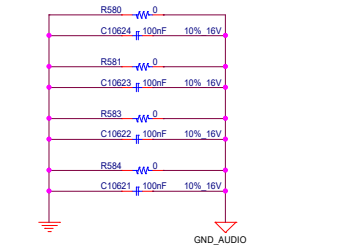
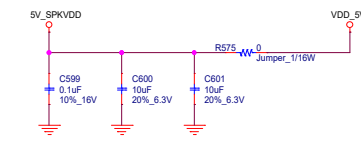
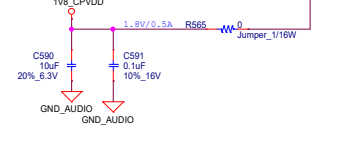
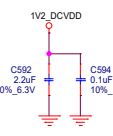
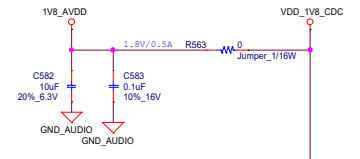
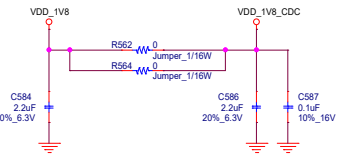
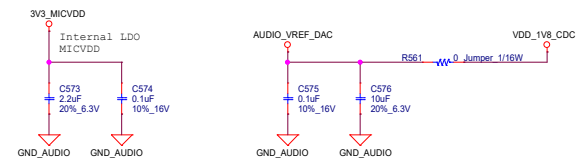
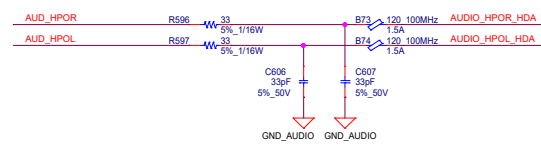
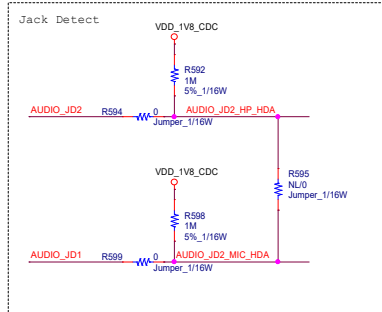
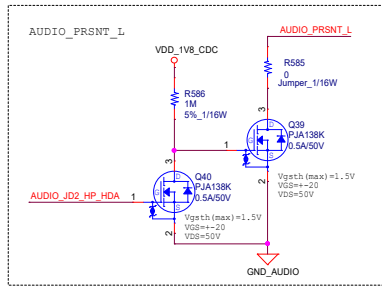
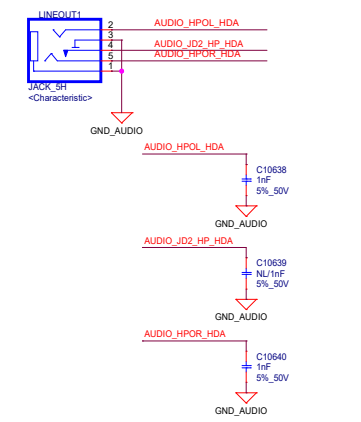
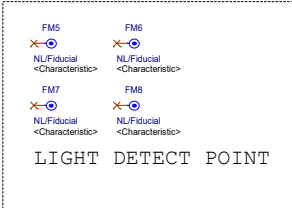
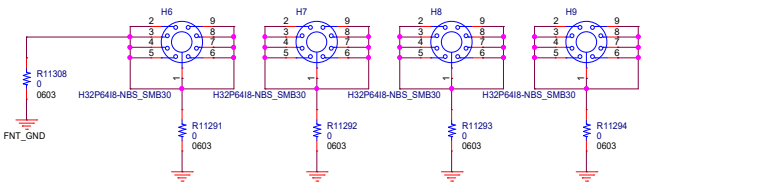
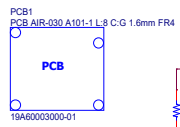
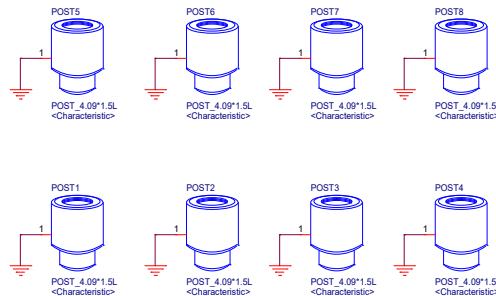
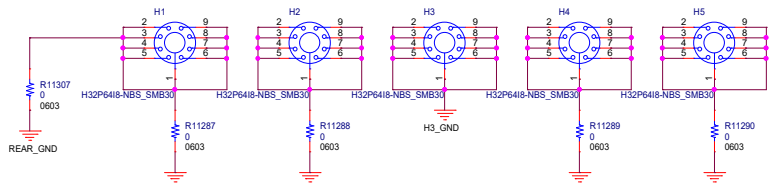


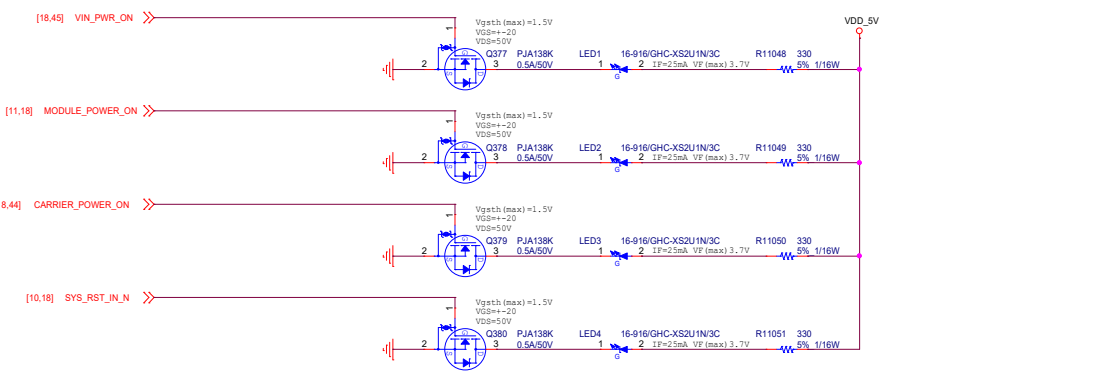
Figure 5. Power On/Off Sequence





Debug LEDs

**Only install in EVT status



5

4

3

2

1

D

D

C

C

B

B

A

A

ADVANTECH		
Title 40_RESERVE#1		
Size A	PCB Name AIR-030_A101-1	Rev A101-1
Date:	Wednesday, August 10, 2022	Sheet 40 of 48

5

4

3

2

1

5

4

3

2

1

D

D

C

C

B

B

A

A

ADVANTECH		
Title 41_RESERVE#2		
Size A	PCB Name AIR-030_A101-1	Rev A101-1
Date:	Wednesday, August 10, 2022	Sheet 41 of 48

5

4

3

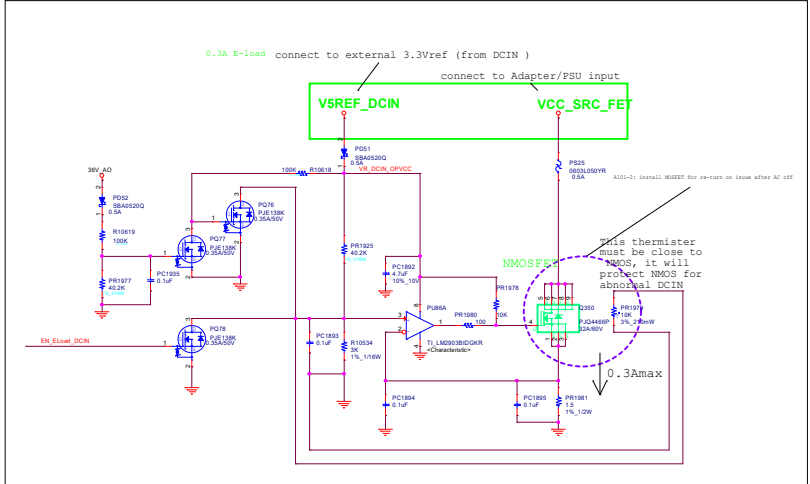
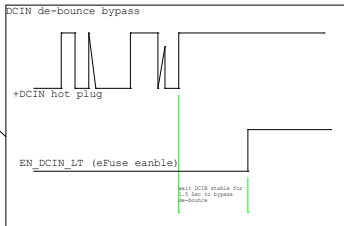
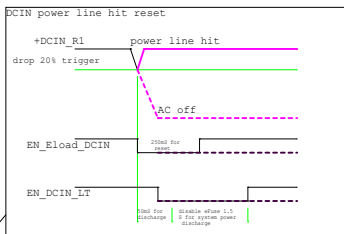
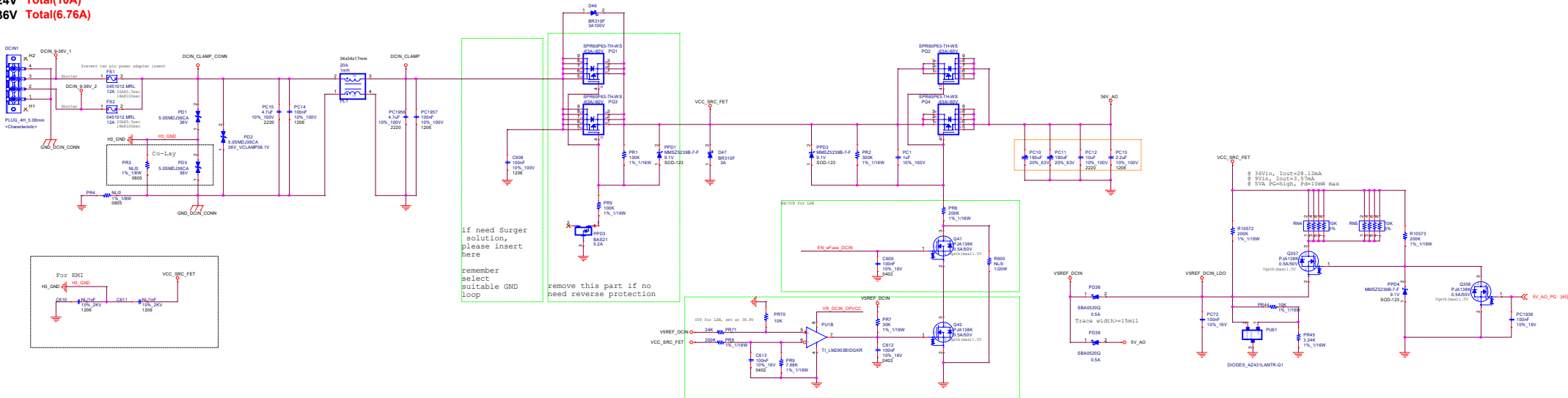
2

1

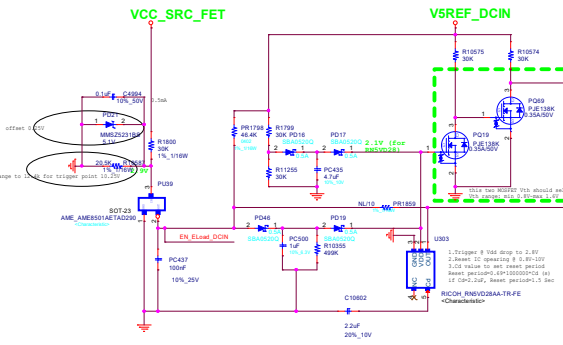
DCIN 9-36 (Refer ADB-3534

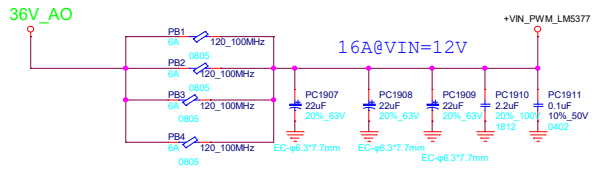
VIN_12V Total(20A)
VIN_24V Total(10A)
VIN_36V Total(6.76A)

Wide Range DCIN (default 9-36V)
 Default max 20Apk current supplied
 default reverse input protect
 OVP-38.3V, UVP-7.5V

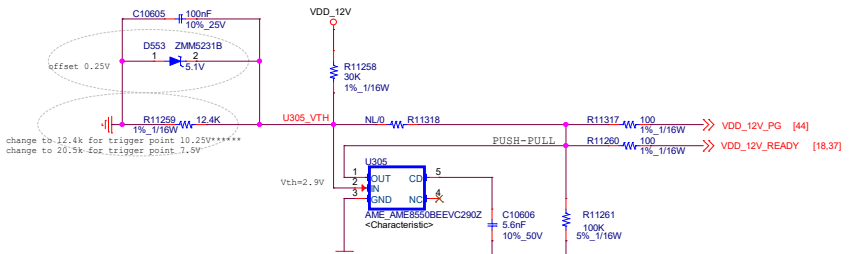
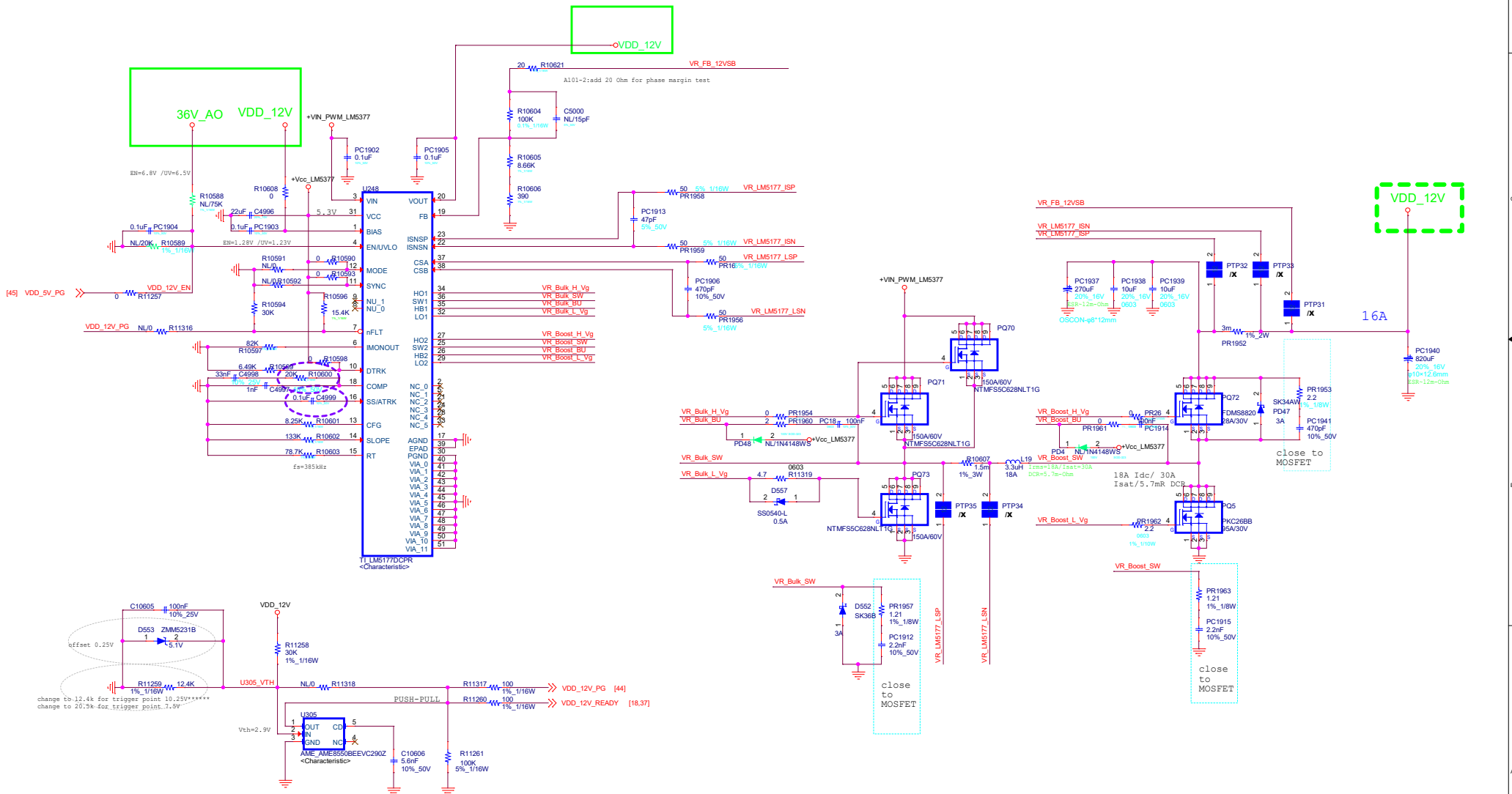


Optional part (7.45V trigger, setting at 7.2V +offset 0.25V)
 Optional part (7.45V trigger, setting at 7.2V +offset 0.25V)





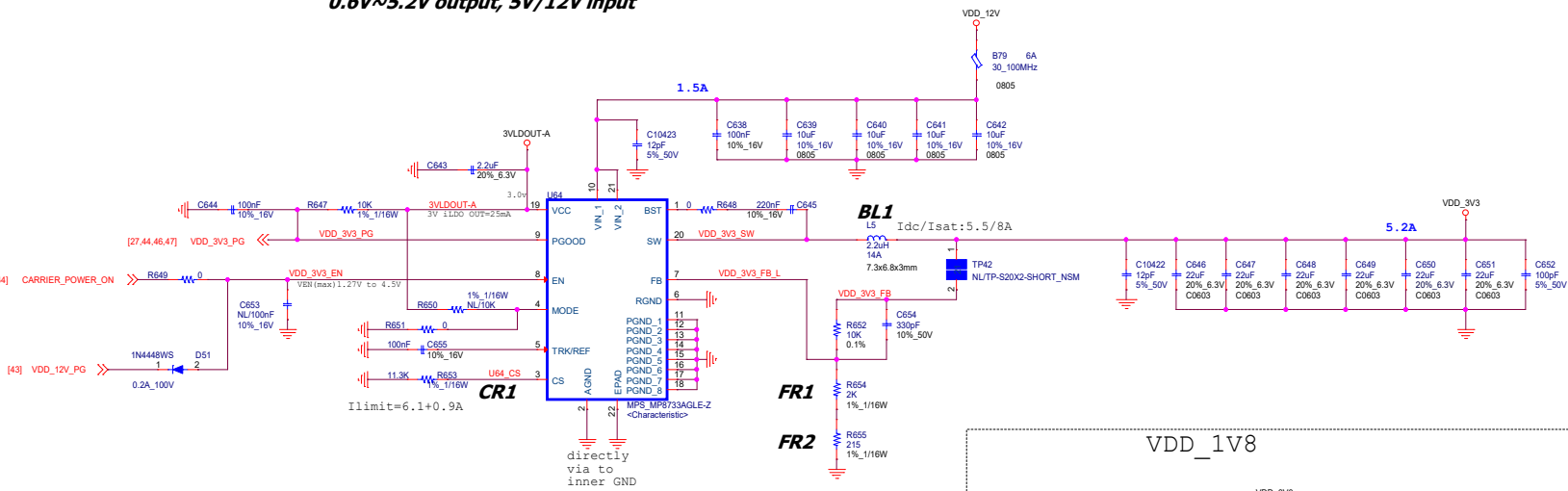
Vin: 9~36V
 I_{tdc}/I_{pk}: 10A/15A
 OCP~23A , F_{sw}~400kHz



V_{in}: 1.2V to 6.5V
 V_{th}=2.9V
 Delay time=(2.9V * nF) / 75nA
 =2.9*4.7/75=216ms

VDD_3V3

IP_TYPE: Converter (POL) 0.6V~5.2V output, 5V/12V input



Ilimit=5.2*1.5=7A
 Imax=12A
 Output Adjustable from 0.6V to 90%* VIN,
 up to 5.5V Max

Input		
VIN	12	V
VOUT	3.3	V
FSW	600	kHz
L	2.2	uH
GCS	20	uA
VOCP	1.2	V
ILIM	7.83	A
RCS	8.6658	Kohm

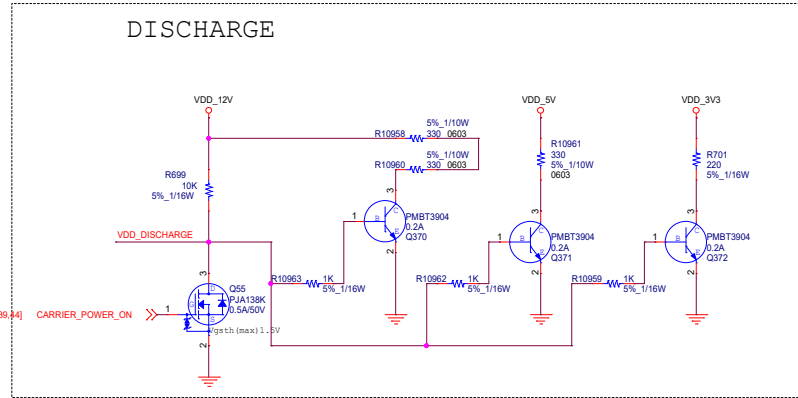
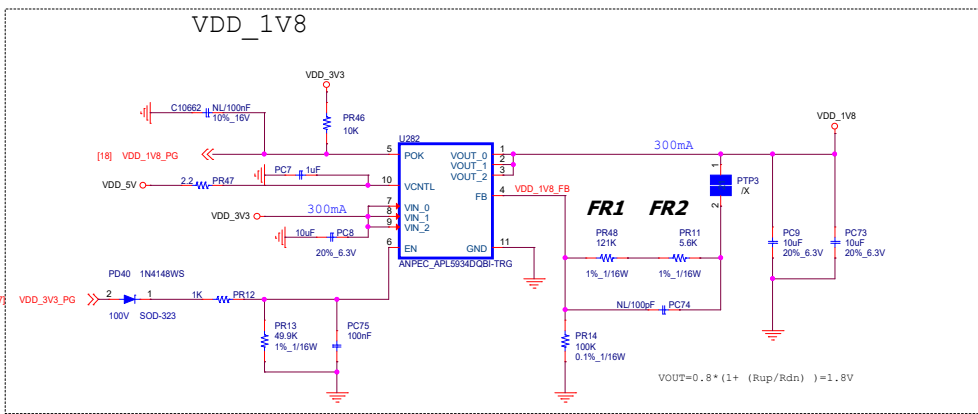
Calculator tool

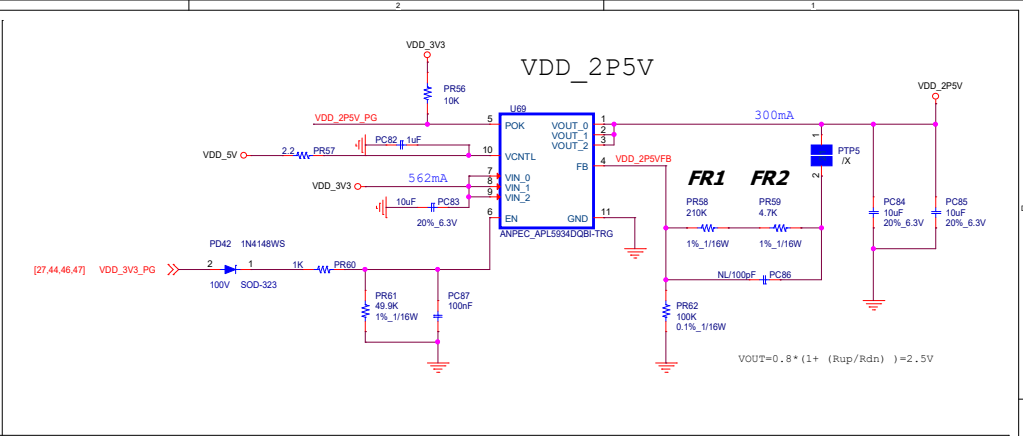
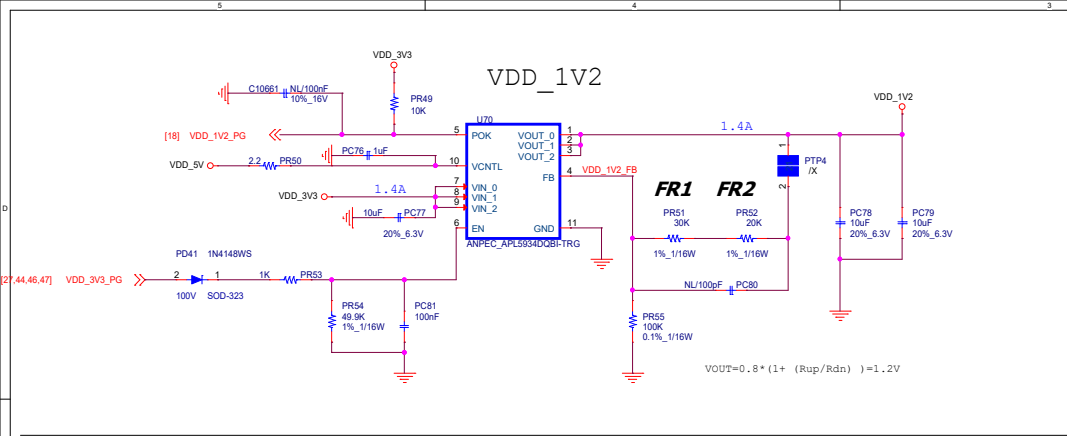
Default setting
 1.FCCM
 2.SS time= 2.0mS

- adjust CR1 for OCP setting
 But Inductor (BL1) Isat must > OCP
- adjust FR1 & FR2 for Vout setting
 Vout range from 0.6V to 5.25V
- add input bead current rating to cover OCP setting
 for example: Vin=12V,Vout=5V, OCP=14.4A==> Iin= 6.7A, use 6A bead*2

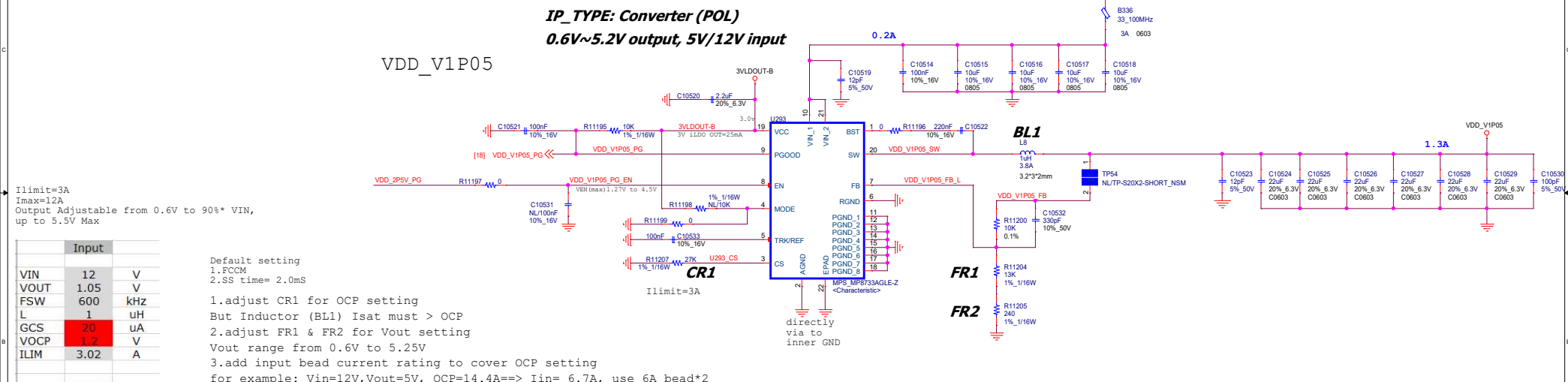
Vin	Vout	FR1	FR2	Ipk (adj CR1)	BL1
6.5~12V	5V	1.2K	0.140k	1~10.0A	2.2uH
5/12V	3.3V	2K	0.215K	1~10.0A	1.5uH
5/12V	2.50V	3k	0.15k	1~10.0A	1.5uH
5/12V	1.80V	4.87k	0.1k	1~10.0A	1.0uH
5/12V	1.35V	7.87k	0.0909k	1~10.0A	1.0uH
5/12V	1.20V	9.76k	0.15k	1~10.0A	1.0uH
5/12V	1.05V	13k	0.24k	1~10.0A	1.0uH
5/12V	1.00V	14.7k	0.2k	1~10.0A	1.0uH
5/12V	0.95V	16.5k	0.499k	1~10.0A	1.0uH
5/12V	0.8V	28.7k	0.604k	1~10.0A	1.0uH

- Vin >> enable ,power-up sequence: (before " >> " ,before or equal " >= ")
- 100nF CAP should be closed to Pin-21(same side & <100mils), line width (>15mils)
- 2.2uF CAP should be closed to Pin-19(same side & <100mils), line width (>15mils)





**IP_TYPE: Converter (POL)
0.6V~5.2V output, 5V/12V input**



Ilimit=3A
Imax=12A
Output Adjustable from 0.6V to 90%* VIN,
up to 5.5V Max

Input	Value	Unit
VIN	12	V
VOUT	1.05	V
FSW	600	KHz
L	1	uH
GCS	20	uA
VOCP	1.2	V
ILIM	3.02	A
RCS	27.008	Kohm

Calculator tool

Default setting
1.FCCM
2.SS time= 2.0ms

1.adjust CR1 for OCP setting
But Inductor (BL1) Isat must > OCP
2.adjust FR1 & FR2 for Vout setting
Vout range from 0.6V to 5.25V
3.add input bead current rating to cover OCP setting
for example: Vin=12V,Vout=5V, OCP=14.4A==> Iin= 6.7A, use 6A bead*2

Vin	Vout	FR1	FR2	Ipk (adj CR1)	BL1
6.5~12V	5V	1.2K	0.140k	1~10.0A	2.2uH
5/12V	3.3V	2K	0.215K	1~10.0A	1.5uH
5/12V	2.50V	3k	0.15k	1~10.0A	1.5uH
5/12V	1.80V	4.87k	0.1k	1~10.0A	1.0uH
5/12V	1.35V	7.87k	0.0909k	1~10.0A	1.0uH
5/12V	1.20V	9.76k	0.15k	1~10.0A	1.0uH
5/12V	1.05V	13k	0.24k	1~10.0A	1.0uH
5/12V	1.00V	14.7k	0.2k	1~10.0A	1.0uH
5/12V	0.95V	16.5k	0.499k	1~10.0A	1.0uH
5/12V	0.8V	28.7k	0.604k	1~10.0A	1.0uH

- 1). Vin >> enable ,power-up sequence: (before " >> " ,before or equal ">=")
- 2). 100nF CAP should be closed to Pin-21(same side & <100mils), line width (>15mils)
- 3). 2.2uF CAP should be closed to Pin-19(same side & <100mils), line width (>15mils)

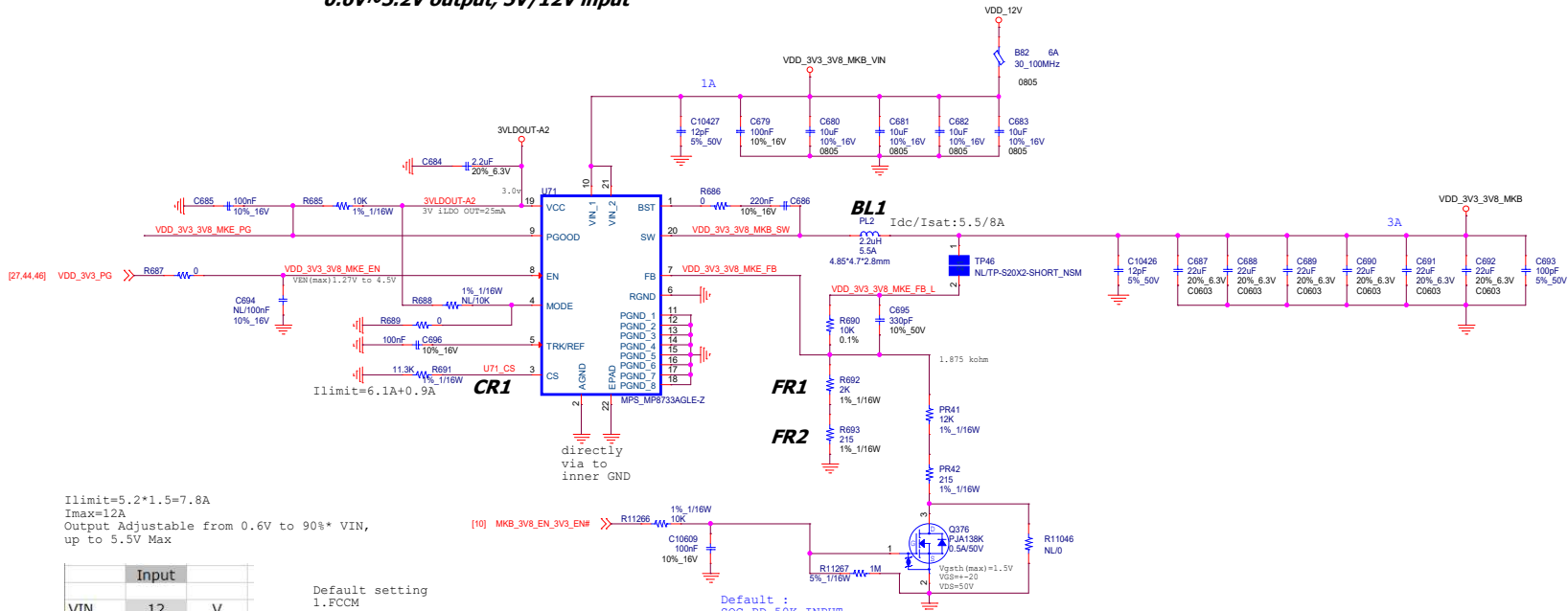
ADVANTECH

46_VDD_V1P05/VDD_2P5V/VDD_1V2

Size	Document Number	Rev
	AIR-030	R101-1
Date:	Wednesday, August 10, 2022	Sheet 46 of 48

VDD_3V3

IP_TYPE: Converter (POL)
0.6V~5.2V output, 5V/12V input



Ilimit=5.2*1.5=7.8A
 Imax=12A
 Output Adjustable from 0.6V to 90%* VIN,
 up to 5.5V Max

Input		
VIN	12	V
VOUT	3.3	V
FSW	600	kHz
L	2.2	uH
GCS	20	uA
VOCP	1.2	V
ILIM	7.83	A
RCS	8.6658	Kohm
Calculator tool		

Default setting
 1.FCCM
 2.SS time= 2.0mS
 1.adjust CR1 for OCP setting
 But Inductor (BL1) Isat must > OCP
 2.adjust FR1 & FR2 for Vout setting
 Vout range from 0.6V to 5.25V
 3.add input bead current rating to cover OCP setting
 for example: Vin=12V,Vout=5V, OCP=14.4A==> Iin= 6.7A, use 6A bead*2

Vin	Vout	FR1	FR2	Ipk (adj CR1)	BL1
6.5~12V	5V	1.2K	0.140k	1~10.0A	2.2uH
5/12V	3.3V	2K	0.215K	1~10.0A	1.5uH
5/12V	2.50V	3k	0.15k	1~10.0A	1.5uH
5/12V	1.80V	4.87k	0.1k	1~10.0A	1.0uH
5/12V	1.35V	7.87k	0.0909k	1~10.0A	1.0uH
5/12V	1.20V	9.76k	0.15k	1~10.0A	1.0uH
5/12V	1.05V	13k	0.24k	1~10.0A	1.0uH
5/12V	1.00V	14.7k	0.2k	1~10.0A	1.0uH
5/12V	0.95V	16.5k	0.499k	1~10.0A	1.0uH
5/12V	0.8V	28.7k	0.604k	1~10.0A	1.0uH

- 1). Vin >> enable ,power-up sequence: (before " >> " ,before or equal " >= ")
- 2). 100nF CAP should be closed to Pin-21(same side & <100mils), line width (>15mils)
- 3). 2.2uF CAP should be closed to Pin-19(same side & <100mils), line width (>15mils)

History

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