ONR Short Pulse Research, Evaluation, and non-SWaP Demonstration for C-sUAV Study (OSPRES)

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14. ABSTRACT

The technical objective of the ONR Short Pulse Research, Evaluation, and non-SWaP Demonstration for C-sUAS Study (OSPRES) Grant program is to execute high-risk, high-payoff efforts that address elementary gaps to achieving a modular, scalable & electronically steerable high power microwave (HPM) based defense system for the counter UAS mission, with focus on the short-pulse high-average-power space, as well as the responsivity of the target to RF stimuli, while educating the next generation of pulsed power and defense-minded scientists, engineers, and innovators.

15. SUBJECT TERMS

high power microwaves, photoconductive semiconductor switches, fiber laser, drift-step-recovery diodes, pulse forming networks, antennas, RF coupling, thermal management, diode-based nonlinear transmission lines; magnetic pulse compression

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1 OVERVIEW

OSPRES Grant Goal: Address and transition technologies and capabilities that enable the OSPRES Grant Objective using the OSPRES Grant Approach, while educating the next generation of pulsed power and defense minded, stewards and innovators.

OSPRES Grant Objective: To execute high-risk, high-payoff efforts that mitigate, fill or rectify one or more grand-challenge or elementary gaps or deficiencies needed to achieve a modular, scalable and electronically steerable high-power microwave (HPM) based defense system for the counter unmanned aerial system (cUAS) mission. The OSPRES HPM system and sub-system development/evaluation efforts are focused on the short-pulse high-average-power space and includes the kill chain considerations including the target and its responsivity to radiofrequency stimuli.

OSPRES Metrics of Success: Developed technologies and capabilities that are published in the peer review, protected as intellectual property, and/or, transitioned to the OSPRES Contract effort and beyond for integration with other DoD needs or dual-commercial-use, as enabling/integrable capability(ies).

OSPRES Grant Approach: A fail-fast philosophy is maintained, where if a technology or capability is deemed infeasible to be demonstrated or validated during the project period-of-performance, it shall be culled, results to date and basis of infeasibility documented, and the next major gap/deficiency area addressed by that part of the project sub-team. Students whose thesis depends on following through with a full answer during the life of the award will be given special dispensation to continue their work.

OSPRES Grant Security: All efforts should be fundamental and publicly releasable in nature when taken individually. This report has been reviewed for operational security, compilation, proprietary and pre-decisional information concerns.

Contents of this Report: This report compiles monthly status reports (MSRs) from October 2021 through September 2022.

ONR HPM Program – Monthly Status Report (MSR) – NOVEMBER 2021

Anthony Caruso – Univ. Missouri – Kansas City

N00014-17-1-3016 [OSPRES Grant]

ONR Short Pulse Research, Evaluation and non-SWaP Demonstration for C-sUAS Study

15 DECEMBER 2021

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1 Contents

2 Executive Summary

2.1 Progress, Significant Findings, and Impact

HV Switch. A 10 kV breakdown capacity was achieved using the modular HV switch architecture; the breakdown was made possible by altering the component placement and using a new optical TX-RX unit.

Fiber Laser and Optical Amplifiers. We found that the optoisolator, which protects our signal laser diode from reflections, also diminishes the noise in our optical pulses by over 10 dB. We identified different beam quality requirements for the optical power tube in photoconductive semiconductor switch (PCSS) vs high energy laser (HEL) applications in that they prefer a uniform vs Gaussian profile, respectively. We interfaced COMSOL data into far-field calculations in Mathematica and achieved the HEL beam quality metric (of M2 < 1.3). A simple lens solution to our entrance optics problem came within a factor of 10 of meeting our objective power for the PCSS application.

Laser Diode Array Driver. To mitigate the reflected path pulse train overlap issue in the unbalanced load configuration of the frozen wave generator (FWG), a chirp-capable, dynamically tunable 12-segment FWG prototype has been designed with optimized reflective path and tested up to 350 V. While this latest iteration has partially resolved the pulse overlap issue, with increase in number of transmission line segments, a consistent drop in the peak voltages has been observed under balanced load.

On-State Resistance in GaN:X PCSS. It was determined that linear mode operation is preferential over non-linear mode for this project due to reduced jitter and increased device lifespan (reliability). Towards minimizing on-state resistance through maximizing optical efficiency, intrinsic mode operation offers increased quantum and optical efficiency over extrinsic mode; however, this limits PCSS geometry to lateral devices due to the shallow absorption depth using UV photon sources.

DSRD Optimization Simulations. An automated fitting procedure for the LTSPICE drift-step recovery diode (DSRD) models was developed that is faster to perform and allows for a closer curve fit to the forward I(V) and reverse C(V) response. More advanced diode models with Smartspice (Philips and HiSIM) are being explored for improved DSRD modeling in reverse IV, breakdown, and recovery.

DSRD Processing and Manufacturing: The processing of Gen2 and Gen3 DSRD lots was continued. Both Gen2 and Gen3 are epitaxy-based processes, as opposed to all previously made diffusion-based DSRDs. Several wafers from the Gen2 lot are finished single die and were submitted to the DSRD characterization team for pulsed performance tests, the results of which have been used to adjust processing recipes on the rest of the Gen2 wafers. Several new process steps—diode side termination by v-groove anisotropic etch and diode side passivation by stain etch and by SiOF room temperature deposition—were significantly developed. Technical feasibility of electroless, selective, seedless deposition of contact metal onto Si was experimentally confirmed for the first time.

DSRD Design of Experiments. A qualitative assessment of capacitance–voltage measurements highlighted the Gen 2 diodes as having the greatest variability, initiating a repeatability study to determine root causes in measurement variations. A Levene's

Variance test produced p-values of 0.8416 (maximum voltage at 10 mA) and 0.8548 (zero junction bias capacitance), indicating that the noise has a normal distribution and is not due to inconsistencies in data collection.

IES Pulsed Power Source Technology Leveraging DSRDs. Hundreds of diode characterization tests (e.g., I(V), C(V), RRT) are nearing completion to compare 7-, 13-, and 26-stack "legacy" deep-diffusion diodes to the new epitaxially-grown variants. Results indicate epitaxial DSRDs proved a significant reduction in performance variation between diodes, enabling up to 4 kV peak voltage out of a single diode when used in the 1×1 pulse generator. Closing the gap between experimental results obtained using the completed 4×2 pulse generator utilizing well-matched epitaxial diodes, and those simulated, the desired $\geq$3 MW peak power pulse is now achievable.

Semiconductor Pulse Sharpeners. The p^+–p–n profile DSRDs we are testing are structurally identical to SAS. However, the initiation of the impact ionization needed for a SAS at >2 kV/ns input pulse depends on the presence of certain types of defects states. Even in the absence of these defect states, DSRDs are expected to show SAS-like behavior at >5–10 kV/ns input pulse. We have begun testing DSRDs as sub-nanosecond pulse sharpeners using a custom-built test fixture and Megaimpulse PPM-0731 pulse generator (58 kV/ns output); however, no change has been observed in the output so far.

Thermal Management. Geometry and microchannel techniques for the ultra-compact thermal management system (UC-TMS) were thoroughly reviewed based on manufacturing tolerances and techniques, which resulted in a 3 x 3 mm preliminary jet impingement microchannel design. The model was simulated in ANSYS with a heat flux of 1 kW/cm^2 applied to a surface representing the semiconductor, causing a 100 kPa pressure drop and negative back pressure at the outlet of the device, while reaching a max temperature of 40 °C higher than the threshold of the device. Therefore, improved jet impingement designs capable of reducing the pressure drop and device temperature by improving the fluid to solid interactions are currently being tested.

Continuous Wave Diode-NLTL Based Comb Generator. Both the K100F and K50F D-NLTLs were tested with a 700 MHz 120 W signal from a R&S amplifier, and both exhibited frequency doubling behavior, producing a waveform containing a frequency peak of 1.4 GHz. Significant amplitude attenuation was observed on the output of the D-NLTLs due to the reflection caused by line-load impedance mismatch, indicating little effect on reducing the degree of impedance mismatch at the source–line interface.

Antennas. A narrowband microstrip patch ESA element and a 2×2 array of narrowband microstrip patch ESAs have been simulated, manufactured, and tested. In both cases, the S_{11}-parameters show good agreement across the 800–1000 MHz range, however, the gain values showed poor agreement throughout the band and the discrepancies are being investigated.

To identify an optimum source antenna combination, we performed pulse source waveform studies using the optimized Koshelev and Shark antenna arrays. Results showed the 'MI0731' source waveform performing exceptionally well (in terms of rE/V) compared to other sources. The 5-element diamond Koshelev antenna array achieved a rE/V of 3.1 while the 8-element elliptical Shark array achieved a value of 2.5. On the

machine learning (ML) side, the prediction accuracy of a ML model to determine the time-domain electric field has been improved by obtaining a RMSE of 0.22 compared to earlier RMSE values >1.

RF Coupling. This month, we expanded the capabilities of our RF predictive tool, PECNEC, in two directions: (1) We are increasing the complexity of the UAV wires model by adding more connections to better represent the different electronic components, and (2) we added the capability to import the waveforms generated by the different sources developed in OSPRES in addition to the canonical waveforms already incorporated in the previous reports.

UAS Engagement Modeling and Simulation. Engagement simulations using the time to effect (TTE) treatment were continued to determine whether the float data type with the ability to store 6–9 significant figures is sufficient or if the more precise double data type with the ability to store 15–17 significant figures is necessary. To add another type of effector to the C# simulation toolkit, which currently only consists of high-powered microwave (HPM) effectors, a literature review on radio frequency (RF) jamming was initiated.

2.2 Completed, Ongoing, and Cancelled Sub-Efforts

	Start	End
2.2.1 Ongoing Sub-Efforts		
GaN:C Modeling and Optimization	OCT 2017	Present
Diode-Based Non-Linear Transmission Lines	FEB 2018	Present
HV Switch Pulsed Chargers	DEC 2018	Present
Trade Space Analysis of Microstrip Patch Arrays	FEB 2019	Present
Enclosure Effects on RF Coupling	OCT2019	Present
Lasers and Optics	FEB 2020	Present
UWB Antenna Element Tradespace for Arrays	MAY 2020	Present
WBG-PCSS Enabled Laser Diode Array Driver	NOV 2020	Present
Si-PCSS Contact and Cooling Optimization	JAN 2021	Present
Drift-Step Recovery Diode Optimization	JAN 2021	Present
UAS Engagement M&S	MAR 2021	Present
DSRD-Based IES Pulse Generator Development	APR 2021	Present
Drift-Step Recovery Diode Manufacturing	MAY 2021	Present
IES Diode Characterization	MAY 2021	Present
Sub-Nanosecond Megawatt Pulse Shaper Alternatives	MAY 2021	Present
Ultra-Compact Integrated Cooling System Development	MAY 2021	Present
GaN-Based Power Amplifier RF Source	AUG 2021	Present
Reconfigurable RF Pulsed-Power Source	AUG 2021	Present
RF Driver Unit for GaN SD-MPM Power Amplifier	SEPT 2021	Present
Reconfigurable RF Antenna for SD-MPM Sources	SEPT 2021	Present
Continuous Wave Diode-NLTL Based Comb Generator	SEPT 2021	Present
2.2.2 Completed Sub-Efforts		
Adaptive Design-of-Experiments	OCT 2017	APR 2019
Non-perturbing UAV Diagnostics	OCT 2017	OCT 2018
Noise Injection as HPM Surrogate	OCT 2017	MAR 2019
SiC:N,V Properties (w/ LLNL)	APR 2018	MAR 2019
Helical Antennas and the Fidelity Factor	JUL 2018	SEPT 2019
Si-PCSS Top Contact Optimization	APR 2020	OCT 2020
Nanofluid Heat Transfer Fluid	NOV 2020	JUL 2021
2.2.3 Cancelled/Suspended Sub-Efforts		
Ab Initio Informed TCAD	OCT 2017	OCT 2020
Positive Feedback Non-Linear Transmission Line	NOV 2017	DEC 2018
Minimally Dispersive Waves	FEB 2018	SEPT 2018
Multiferroic-Non-linear Transmission Line	NOV 2018	APR 2019
Avalanche-based PCSS	SEPT 2018	SEPT 2019
Gyromagnetic-NLTL	DEC 2017	NOV 2020
Multi-Stage BPFTL	APR 2020	JUL 2020
Heat Transfer by Jet Impingement	MAY 2018	FEB 2021
Si, SiC, and GaN Modeling and Optimization	NOV 2018	FEB 2021
Bistable Operation of GaN	FEB 2021	MAR 2021
IES Pulser Machine Learning Optimization	MAY 2021	AUG 2021

2.3 Running Total of Academic and IP Program Output

See Appendix for authors, titles and inventors (this list is continuously being updated)

Students Graduated	*5 BS, 8 MS, 3 PhD*
Journal Publications	*5 (6 submitted/under revision)*
Conference Publications	*33 (4 submitted/accepted)*
External Presentations/Briefings	*17 (23 submitted/accepted)*
Theses and Dissertations	*4*
IP Disclosures Filed	*10*
Provisional Patents Filed	*4*
Non-Provisional Patents Filed	*0*

3 Prime Power and Conditioning

3.1 HV Switch Pulsed Chargers

(Sarwar Islam and Faisal Khan)

3.1.1 Problem Statement, Approach, and Context

Primary Problem: Commercially available high-voltage solid-state switches made by BEHLKE are the best in SWaP-cooling, but are expensive, have long lead times (2–3 months), and are made outside of the US. For the Navy afloat mission to be successful, we need a sustainable supply of US-manufactured switches at a much lower cost.

Solution Space: Design and demonstrate modular high-voltage (~10 kV) and fast (repetition frequency = 100 kHz) solid-state switches using a combination of series- and parallel-connected commercially available inexpensive discrete MOSFETs and custom high-voltage (~10 kV) isolated gate drivers.

Sub-Problem: Voltage balancing among the series-connected MOSFETs, minimization of gate signal delays, cooling of the individual MOSFETs, balancing resistors, high-voltage isolation required for the power supplies, and the controlling pulse width modulated (PWM) signal as well as differential voltage feedback measurement across individual MOSFETs.

State-of-the-Art (SOTA): Direct liquid-cooled solid-state switch from BEHLKE (e.g., HTS-151-30).

Deficiency in the SOTA:

1. BEHLKE-made switches are expensive. For instance, a single HTS-151-30 switch costs around $5,000.
2. BEHLKE switches along with direct liquid cooling units occupy a considerable amount of space. For instance, an HTS-151-30 switch from BEHLKE has a footprint of approximately 225*85*75 mm without considering the liquid cooling system. Some key parameters of this switch are as follows.

   i) Maximum operating voltage = 15 kV

   ii) Maximum continuous load current = 2.52 A (without cooling), 30 A (with liquid cooling)

   iii) Maximum turn-ON peak current = 300 A (pulse width = 200 µs, duty cycle <1%)

   iv) Turn-ON resistance = 1.3 Ω
3. Once the switching frequency is greater than 10 kHz, a liquid cooling system is required to operate the BEHLKE switch.
4. Without liquid cooling, the maximum continuous power dissipation (P_{cont}) of the BEHLKE switch is limited (e.g., for HTS-151-30, P_{cont} is 10 W without liquid cooling).
5. At a higher switching frequency (>20 kHz), the BEHLKE switch requires multiple ancillary DC power supplies, i.e., 5, 15, and 60 V.

6. The switches made by BEHLKE cannot be reconfigured to withstand a higher voltage exceeding their recommended rating. BEHLKE offers separate products to operate them at higher voltage/currents.

Solution Proposed: Designing a modular high-voltage (~10 kV) switch using a single custom isolated gate driver for each module and having a construction cost lower than the BEHLKE switch with equivalent or better performance in all specification categories (Specifications for the BEHLKE switches can be found in the following link: http://www.behlke.com/separations/separation_c4.htm).

Relevance to OSPRES Grant Objective: The proposed modular high-voltage switch is expected to facilitate controlled hundreds-of-nanosecond charging of an array of transmission lines of pulse forming networks to drive an array of PCSSs, thereby producing controlled hundreds-of-picosecond scale high-voltage pulses.

Risks, Payoffs, and Challenges:

I. Lack of rigid control over voltage balancing can lead to a cascaded failure among the series-connected MOSFETs.

II. In the absence of an adequate mitigation scheme, voltage overshoot due to the fast-switching speed can exceed the voltage rating of an individual MOSFET, thereby damaging the switch.

III. At high voltage (~10 kV) and high repetition rate (>100 kHz), mitigating EMI to safeguard the individual MOSFETs from false turn-ON is a major challenge.

3.1.2 Tasks and Milestones / Timeline / Status

(A) Design a surface-mount MOSFET-based four-stage switch (6.8 kV rated) and control it using the in-house gate driver, then test its voltage-withstanding ability with a DC supply voltage up to 4–5 kV and evaluate the effectiveness of the thermal management at its current state / DEC 2020 / Completed.

(B) Design and develop a modular HV switch (~10 kV rated) using the concept of the tested four-stage high-voltage switch module and an in-house modular gate driver to drive the modular switch /JAN–FEB 2021 / Completed.

(C) Test the voltage withstanding ability of the modular HV switch with a DC supply voltage up to 10 kV and switching frequency up to 50 kHz using a resistive load (5–10 kΩ) and evaluate the effectiveness of the thermal management at its current state / FEB–SEP 2021 / Ongoing.

(D) Test the isolation capability and evaluate the synchronization accuracy of the gate drive signal generated from the modular in-house gate driver / FEB–SEP 2021 / Completed.

(E) Encapsulate the gate driver board with potting material with a high (~15–20 kV) breakdown voltage rating to prevent possible flashover/arcing in between the HV switch and this board / MAR–SEP 2021 / Ongoing.

(F) Design and fabricate a compact power conditioner circuit based on a 12 kV rated SiC switch made by BEHLKE (HTS 121-15) / APR–MAY 2021 / Completed.

(G) Test this modular HV switch coupled with a Si PCSS device up to a DC supply voltage of 5–6 kV and a switching frequency of 50 kHz / SEP 2021/Ongoing.

(H) Design and develop a 20 kV rated modular (two modules, each with four MOSFETs) HV switch based on the design concept of the 10 kV rated modular switch using 3.3 kV rated SiC MOSFETs (new product made by GeneSiC Semi) / Ongoing.

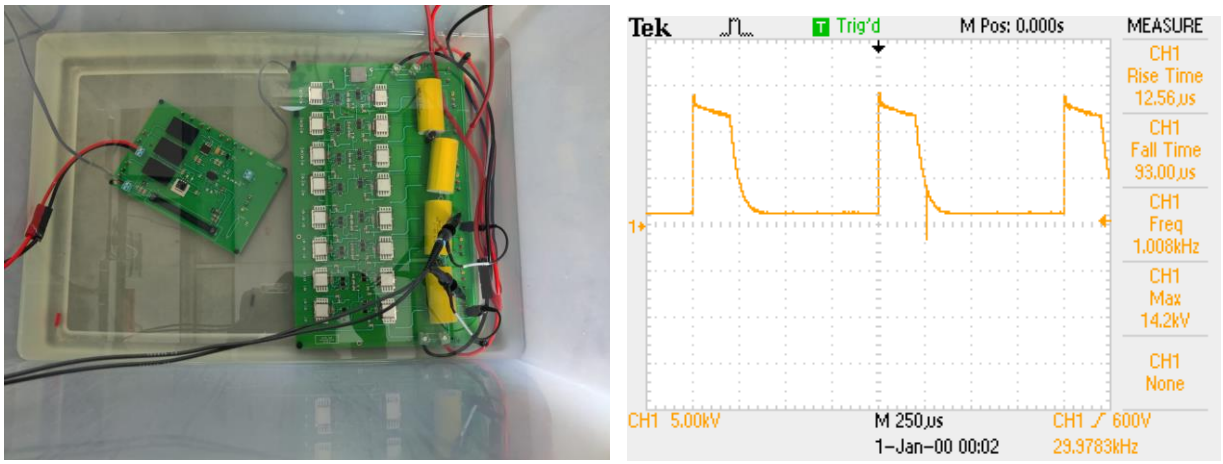
(E) Design and develop a 20 kV rated modular gate driver based on a WPT based planar transformer topology to ensure adequate galvanic isolation (~30–40 kV) for the power supplies of the gate driver / Ongoing.

3.1.3 Progress Made Since Last Report

(C) Achieving the necessary 10 kV breakdown voltage was a challenge in our previous version of the HV switch. Although the previous version was designed for 10 kV or higher, the gate driver circuit suffered from voltage breakdown on the PCB. We have identified the problem, and it was caused by narrow spacing between two traces carrying a voltage gradient equal to the high voltage (HV) supply. Since we experienced this failure, we have redesigned the PCB and used a new optical fiber TX-RX assembly to eliminate this problem.

(E) In addition, the entire circuit assembly including the driver PCB was immersed in dielectric oil to prevent any unwanted arcing through air, although the final design will use some sort of potting materials for packaging ease. This technique does not only resolve the arcing issue, but it also improves the thermal distribution of the system.

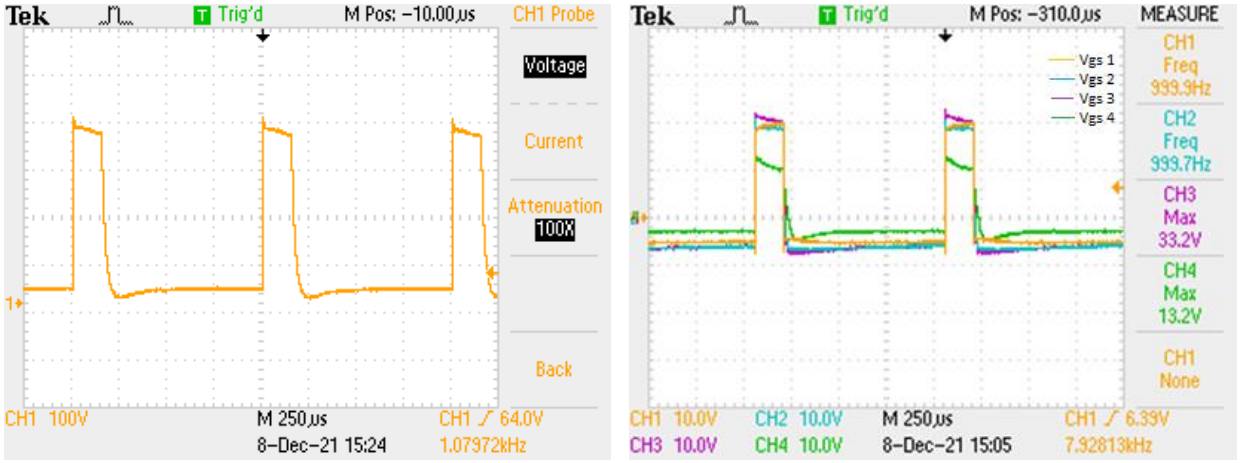
A complete system has been tested at 1 kV, and it successfully withstands this voltage. A repetition rate of 1 kHz was used during testing. The load impedance was 300 kΩ.



(b) (b)

Figure 1. (a) The modified 10 kV switching module immersed in dielectric oil, (b) switching characteristics of the module using a voltage divider probe. The output voltage swing is 10 kV (5 kV/division).

(D) A second test was conducted at a lower voltage using a different loading condition. The load was a series combination of a 200 kΩ resistor and a 9.6 kΩ resistor. Therefore, this combination worked as a voltage divider, and we measured the voltage across the 9.6 kΩ resistor. The results are shown in Figure 2. The divider ratio was 21.833:1.



(a) (b)

Figure 2. (a) Voltage across the load, the voltage swing was 7.64 kV (b) Gate to source voltages of the four MOSFETs used in a module.

3.1.4 Summary of Significant Findings and Mission Impact

(A) The 6.8 kV rated four-stage surface-mount MOSFET developed in-house was successfully tested up to a DC supply voltage of 4 kV and at a switching frequency up to 20 kHz with a 3.2 kΩ resistive load. The proposed voltage balancing method achieves <1.1% voltage mismatch under steady-state and switching transitions.

(B) A modular (two modules) 10 kV rated HV switch has been designed and a prototype has been developed using 1.7 kV rated SMD MOSFETs (C2M1000170J). An in-house 10 kV rated HV gate driver has been designed and incorporated with the HV switch to drive it. A manuscript on the HV switch and the custom isolated gate driver has been submitted to IEEE Transaction on Power Electronics.

(C) An insulating naphthenic dielectric oil has been acquired that meets the ASTM D-3487 specification. With the use of this dielectric oil, altered component placement and new TX-RX optical module, the newly designed gate driver and MOSFET PCB can safely withstand 10 kV. At present, the prototype runs at Fsw = 1 kHz, d = 15%, V_{DC} = 10 kV, and R_{load} = 300 kΩ. We are yet to test the circuit at 50 kHz switching to complete Task (C). We need to test the circuit at much higher load current (load impedance = 5–10 kΩ), and we plan to do so in January. Our present setup, especially the HV power supply, limits us to test the circuit at significantly smaller load current.

(D) At 10 kV, the gate driver circuit operates flawlessly, and the gate-source signals have the necessary integrity to avoid malfunctions.

(E) The entire circuit assembly including the driver PCB was immersed in naphthenic dielectric oil to prevent any unwanted arcing through air, although the final design will use some sort of potting materials for packaging ease. The system has been tested up to 10 kV, and we are yet to test the oil's dielectric strength at 20 kV.

4 Laser Development

4.1 Fiber Lasers and Optical Amplifiers

(Scott Shepard)

4.1.1 Problem Statement, Approach, and Context

Primary Problem: High-average-power 1064-nm picosecond lasers are too large (over 1100 cm^3/W) and too expensive (over \$1000/μJ per pulse) for PCSS (photoconductive semiconductor switch) embodiments of HPM-based defense systems. For example, a laser of this class might occupy a volume of 1 m x 30 cm x 30 cm = 90,000 cm^3 and provide an average power of 50 W (thus, 1800 cm^3/W). Costs in this class range from \$100K to \$300K to drive our Si-PCSS applications.

Solution Space: Optically pumped ytterbium-doped optical fiber amplifiers, fed by a low-power stable seed laser diode, can offer a cost-effective, low-weight, and small-volume solution (with respect to traditional fiber and traditional free-space laser designs). Moreover, our novel optical amplifier tubes, might operate at far higher power levels (over 1000 times greater), thus driving an entire array of PCSS with a single amplifier and thereby reducing the overall system costs and eliminating the optical pulse-to-pulse jitter constraints.

Sub-Problem (1): Optical pump power system costs account for over 50% of the budget for each laser (in this class, for normal/free-space, optical fiber, and tubular embodiments).

Sub-Problem (2): Fiber (as well as power tube) optical amplifier performance is degraded primarily by amplified spontaneous emission (ASE) noise, which limits the operating power point, and by nonlinearities, which distort the optical pulse shapes.

State-of-the-Art (SOTA): Free-space NdYAG lasers or Ytterbium-doped fiber amplifiers optimized for LIDAR, cutting, and other applications.

Deficiency in the SOTA: Optical pump power system costs (in either free-space or fiber lasers) are prohibitive for the PCSS applications until reduced by a factor of at least two.

Solution Proposed: Fiber lasers permit a pre-burst optical pumping technique (wherein we pump at a lower level over a longer time) which can reduce pumping costs by a factor of at least ten. To address the ASE and nonlinear impairments, we are pursuing the use of gain saturation and a staged design of different fiber diameters. We also apply these techniques to fiber amplifiers which incorporate our power amplifier tube in the final stage. The inclusion of our novel tubular-core power amplifier stage should permit a single laser to trigger an array of several PCSS (reducing system cost and mitigating timing jitter).

Relevance to OSPRES Grant Objective: The enhancement in SWaP-C^2 for the laser system enables PCSS systems for viable deployment via: a factor of 40 in pumping cost reduction of each laser; and a factor of *N* in system cost reductions as a single laser could drive *N* (at least 12) PCSS in an array, while also eliminating the optical jitter constraints.

Risks, Payoffs, and Challenges: Optically pumping outside the laser pulse burst time can enhance the ASE; pump costs could be reduced by 40, but ASE in the presence of dispersion and/or nonlinearities could enhance timing jitter thereby limiting steerability. The main challenge for power tube implementation is the entrance optics design.

4.1.2 Tasks and Milestones / Timeline / Status

(A) Devise a pre-burst optical pumping scheme by which we can reduce the costs of the laser by a factor of two or more and calculate the resulting increase in ASE. / FEB–JUL 2020 / Completed.

(B) Reduce the ASE via gain saturation. / Oct 2020 / Completed.

(C) Design saturable gain devices which avoid nonlinear damage. / Ongoing.

(D) Calculate and ensure that timing jitter remains less than +/-15 ps with a probability greater than 0.9. / Ongoing.

(E) Demonstrate a cost-reduced fiber laser. / Ongoing.

(E1) **March 2021** Finalize design. / Completed.
(E2) **April 2021** Assemble and test-check seed LD (laser diode)/driver. / Completed.
(E3) **April 2021** Measure power vs current transfer function of seed LD/driver. / Completed.
(E4) **May–July 2021** Measure ASE and jitter of 1064 nm seed LD/driver. / Completed.
(E5) **May–July 2021** Measure ASE and jitter of 1030 nm seed LD/driver. / Completed.
(E6) **June–July 2021** Assemble and test-check pump LDs/drivers. / Completed.
(E7) **June–July 2021** Measure power vs current transfer function of pump LDs/drivers. / Completed.
/ (E8) – (E14) Delayed due to vendor issues (see MAY MSR).
(E8) **September 2021** Splice power combiners to Yb doped preamp fiber. /Completed.
(E9) **September 2021** Connect seed and pumps to power combiners and test-check. / Completed.

(E10) **September–October 2021** Measure gain, ASE and jitter of 1064 nm preamp assembly (forward, backward and bidirectional pumping) as a function of pump power and duty cycle. / Partially complete.

(E11) **September–October 2021** Measure gain, ASE and jitter of 1030 nm preamp assembly (forward, backward and bidirectional pumping) as a function of pump power and duty cycle. / Partially complete.

(E12) **November 2021** Splice power amplifier and its power combiner to best preamp. / Ongoing (delay due to vendor error).

(E13) **November–December 2021** Measure gain, ASE and jitter of entire amp assembly.

(E14) **December 2021** Analyze data and document.

4.1.3 Progress Made Since Last Report

(E10–E12) A vendor error resulted in a revised plan. Our Yb-doped fiber vendor (Coherent, which supplies fiber from Nufern) assured our team that we would receive 2

sections as requested: one of 2 meters (for a pre-amp) and one of 6 meters (for a power amp); instead they shipped one fiber of 8 meters to the company which spliced this fiber into our power combiner (comprised of other fibers with connectors for signal and pump). The fastest way to compensate for their error is our revised plan of progressively cutting the 8 meter fiber down to shorter lengths. This incurs a delay of only one month (to receive an expensive fiber cleaver) rather than having the vendor partners rework the parts (which would take at least four months). The revised plan will still accomplish the original goal of demonstrating the pre-bust pumping scheme. Moreover, we will obtain more data while we experiment at progressively shorter lengths. We found that the optoisolator, which protects our signal laser diode from reflections, also diminishes noise in our optical pulses by over 10 dB – as described in 4.1.4.

(F) NDAs have been signed between UMKC and NKT Photonics – a top international manufacturer of fiber lasers and photonic crystal fibers (PCF), which has expressed an interest in our tubular-core optical power amplifier effort. Hollow-core PCF are similar to our optical power tube (but with more complex and smaller cross-sections). Our hope is that NKT will gear up to Yb dope our larger tubes and possibly partner with us in their development. An overview of our results has been disseminated and is currently under review.

(F) Two MIDE consultants and I met with two NRL fiber laser experts and discussed our tubular-core optical power amplifier effort. NRL expressed an interest in partnering on this technology, which they deemed as “viable.” We all agreed that there are two applications for the optical power tube: one in HEL (high energy lasers, wherein a Gaussian output beam profile is desired; the other in PCSS (wherein the output beam profile is preferred to be more uniform, as it makes the passive power splitting easier). Recent results, as detailed in 4.1.4, show that both applications can be covered by the same power tube since the output beam profile can change to be more Gaussian or more uniform simply by adjusting its operating power level. Funding sources are said to appreciate the covering of two applications via a “single product” development.

(F) In the HEL application we want the output beam to diffract as little as possible. The subject is referred to as “beam quality” with the 2 main metrics being “M2” (pronounced “M-squared”) and “power in the bucket.” For either metric we must calculate the far-field diffraction pattern but that is incompatible with the current simulations (which use the paraxial beam envelope approach to cut computation times in our waveguides/fibers). We solve this problem by doing the far-field calculation “separately” by exporting the waveguide output planes, out of COMSOL, and importing them into Mathematica where the diffraction integrals are calculated, as detailed in 4.1.4. This also increases the capability of our COMSOLs to assess field uniformity for the PCSS application (see 4.1.4).

(F1) The main challenge for power tube implementation is the entrance optics design. Therein it would be ideal to map a circular spot of tens of microns in diameter to an annular ring of a few mm in diameter. We consider a suboptimal but simple approach in which we use a lens to magnify the tens of microns circular input spot. We find that the break-point power (i.e., the operating point at which roughly half the tubular amplifier’s energy is in air) is diminished to MW power levels (instead of GW) inside the glass/cladding, yet in the

air-core we can still carry power levels of 1/10 GW, as shown in Fig. 4.1.5. Thus, this simple approach might lead to the GW target objective with further optimization.

4.1.4 Technical Results

(E10–E11) An optoisolator permits optical propagation in one direction (in our case, down an optical fiber) but blocks any reflections from propagating in the opposite direction. The primary purpose of our optoisolator is to prevent reflections from damaging our signal laser diode. We find that this also diminishes noise in our optical pulse shape, as shown in Fig.4.1.1 at a pulse rep-rate frequency of 1kHz.

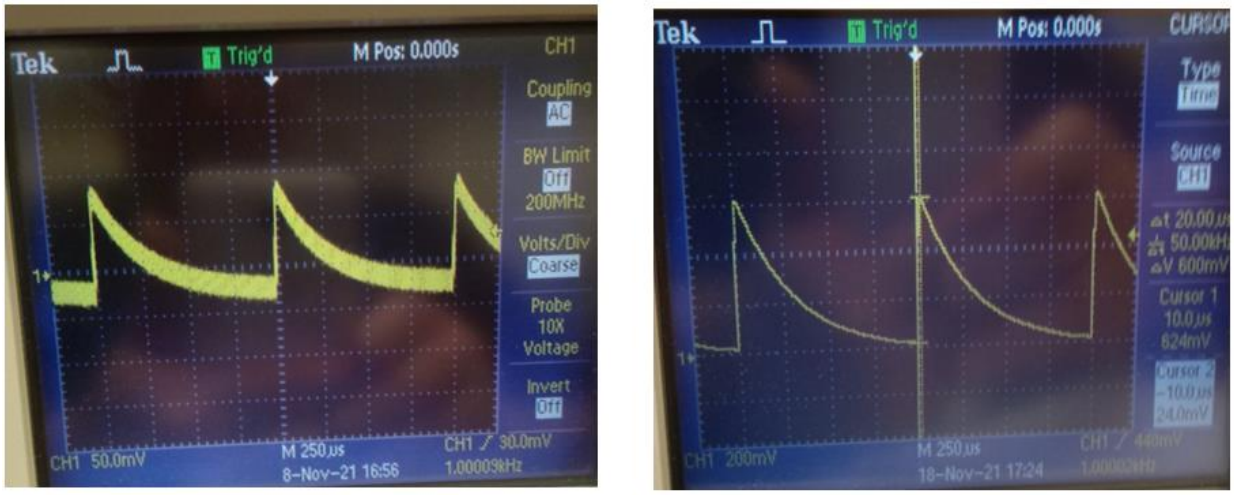


Fig. 4.1.1. Photodetected optical signal pulse shape: without optoisolator (left); with optoisolator (right).

The reduction in noise for the optoisolated case could be due to preventing the reflections' influence in carrier dynamics inside the laser diode or within the photodetector or both. The long-tail (slow falling edge) aspect exhibited is likely because the photodetector is a diode (without any transimpedance amplifier) and hence more like an ideal current source which in this case is driving a high impedance scope input. A 50 ohm terminated coax cable will resolve this in the near future. Similar long-tail laser pulse responses were identified in BAE experiments to be due to modal dispersion in a fiber optic splitter. PCSS response times however have been shown to depend exclusively on leading-edge time scales of the laser pulse (which herein are clearly faster).

(F) The optical power tube for HEL applications require a low diffraction (M2 < 1.3) output beam; where the "beam quality" metric M2 is defined via $W0\ W(z) = M2\ z\lambda/\pi$, where W0 is the minimal beam waist and W(z) is the beam waist in the far-field. The lower bound for M2 is 1 – obtained only for the TEM_{00} mode, which has a Gaussian profile. Calculation of the far-field diffraction pattern however is not possible within our COMSOL simulations (which use the paraxial beam envelope approach to reduce computation time in our

waveguide/fiber geometries). We solved this problem by exporting the 2D electric field values at the waveguide output plane into Mathematica where the diffraction integrals are calculated. In most cases our field distribution is invariant under rotation about the direction of propagation (because our source is) thus a 1D line-cut of the field is sufficient.

An example of such data imported into Mathematica is shown in Fig. 4.1.2 (red points) to closely resemble an LMS fit of the data to a Gaussian function (solid blue line). The M2 for this case was 1.13.

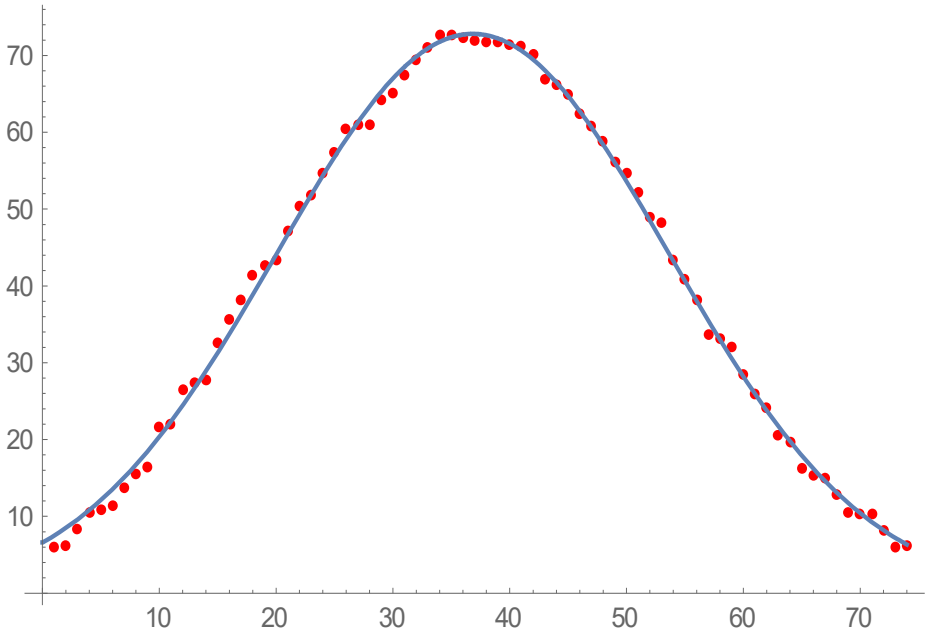


Fig. 4.1.2. A 74 point sample of the electric field [arbitrary units] across the output of an optical power tube (in red) resulting in M2 = 1.13; and its fit to a Gaussian (in blue) for comparison.

We often produce output beam profiles which resemble Gaussians, as exemplified in the COMSOL line-cuts of Fig. 4.1.3. This also increases the capability of our COMSOLs to assess field uniformity for the PCSS application (as in Fig. 4.1.4).

(F1) In an attempt to simplify the entrance-optics design for the optical power tube we consider simply using a lens and find that we can achieve Gaussian-like profiles with cladding powers, P_{clad} , on the order of MW as exemplified in the COMSOL line-cuts of Fig. 4.1.3 (for three different values of input intensity I0, in [W/cm^2]) .

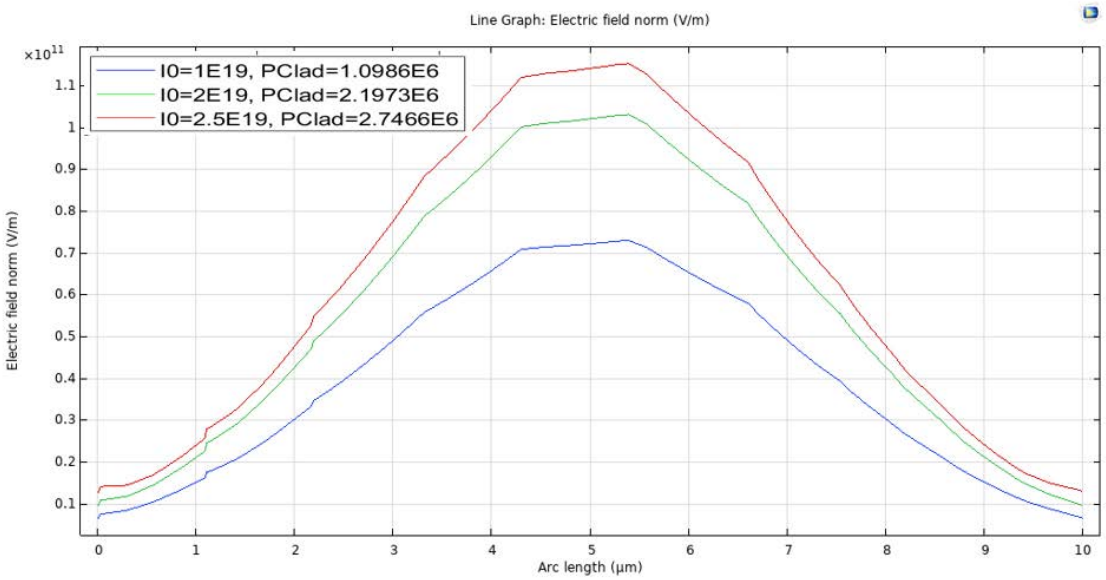


Fig. 4.1.3. Electric field output distribution for a lens fed power tube.

The lensed approach was not as successful at producing more uniform field distributions at these power levels, yet the COMSOL line-cut of Fig. 4.1.3 in blue, is fairly flat.

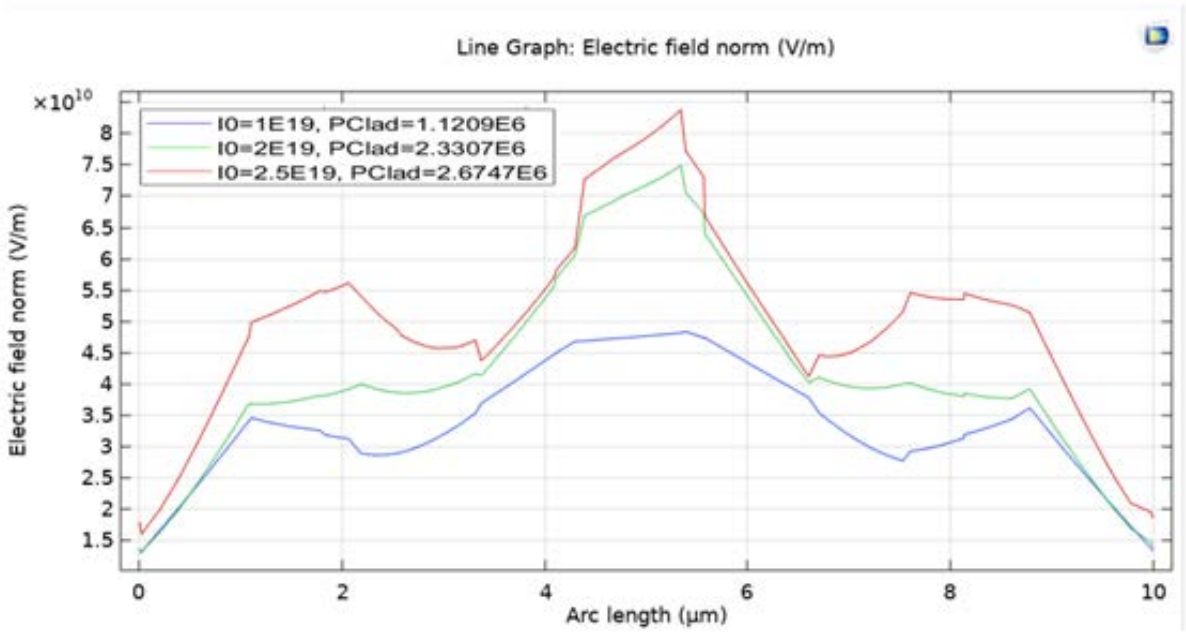


Fig. 4.1.4. Electric field output distribution for a lens fed power tube.

We find that in this lensed approach, the break-point power (i.e., the operating point at which roughly half the tubular amplifier's energy is in air) is diminished to MW power levels

(instead of GW) inside the glass/cladding, yet in the air-core we can still carry power levels of 1/10 GW, as shown in Fig. 4.1.5. Thus, this simple approach might lead to the GW target objective with further optimization.

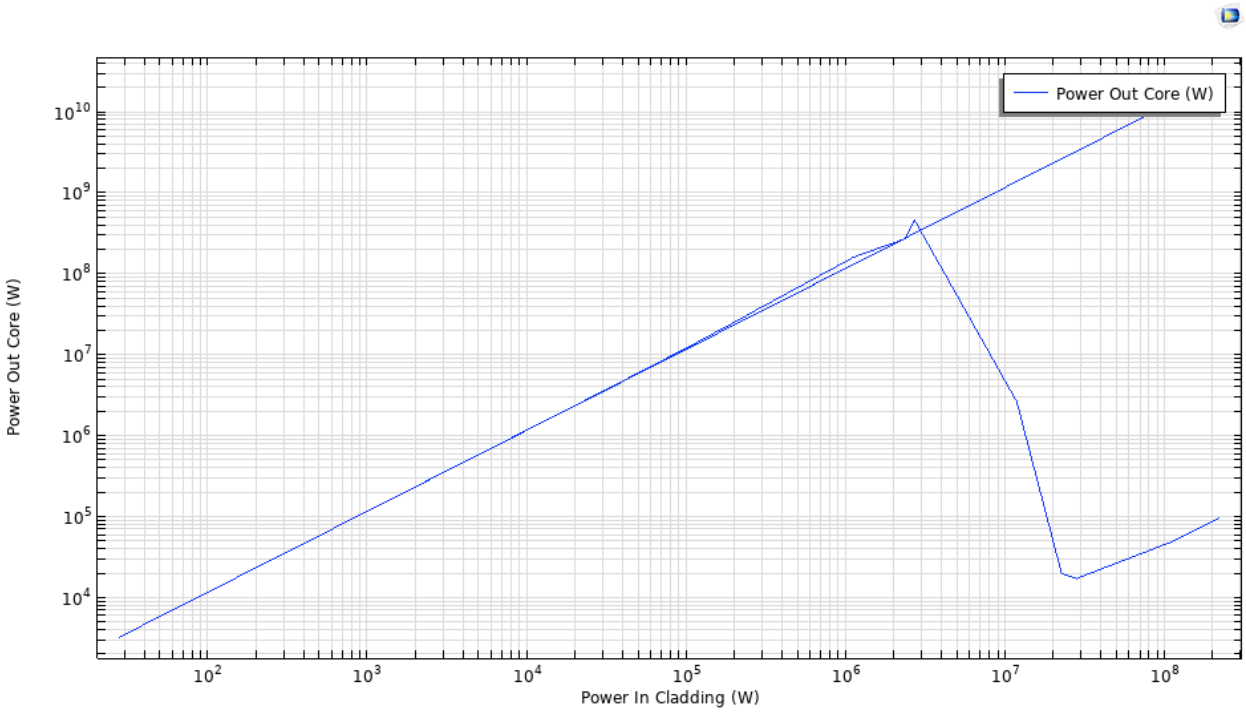


Fig. 4.1.5. Air-core power vs the glass/cladding power of the amplifier. The straight line is for gamma = 0 (no Kerr nonlinearity).

4.1.5 Summary of Significant Findings and Mission Impact

(A) Our pre-burst optical pumping scheme simulations showed that we can drop the pump power costs by a factor of 40 with pre-burst ASE power levels below the heating level tolerance of 100 μW. UMKC invention disclosure filed 02JUN2020.

(B) For a proposed system gain of 8 million, a linear gain theory predicted the in-burst ASE would be over our heating level spec. by a factor of 3960, but by exploiting the nonlinearity of gain saturation we find that we can suppress the ASE by over 7000. UMKC invention disclosure filed 14SEP2020.

(C) Achieved initial practical device designs that exploit gain saturation, which remained below damage thresholds, via staged designs of different mode diameters NOV2020.

(D) Models of the impact of ASE on timing jitter in the presence of dispersion and/or nonlinearities were established JUL2020.

(E) The design of a proof-of-concept experiment demonstrating a cost-reduced optical pumping scheme was finalized MAR2021.

(F) We made (to our knowledge) the first observation of self-focusing effects that are not determined by beam power alone. We found instead that these can also be controlled via the geometric factors within a waveguide (such as fiber core diameter) MAY2021.

We additionally made (to our knowledge) the first observation that a mode exists in the air within a simple glass tube into which we can couple energy from the mode in the glass. Thus, an amplifier (in the doped and pumped glass) can operate at higher powers JUNE2021.

We found conditions under which 0.25 GW of power can exist in the tube's air-core mode when its glass-cladding mode is at a power level near 0.5 GW JULY2021.

Advancements in the very high-power operating point (tens of GW) of our tubular optical amplifier (and the existence, size and spatial uniformity of its air-core mode) were shown to permit a single laser to trigger an array of several (up to 100) Si-PCSS – reducing the laser system cost and eliminating the optical timing jitter constraint. The symmetry breaking of the scattering from self-focusing in a curved waveguide was shown to enable such AUG2021.

4.2 WBG-PCSS Enabled Laser Diode Array Driver

(John Bhamidipati)

4.2.1 Problem Statement, Approach, and Context

Primary Problem: Need for heavy (~125 lbs.), bulky (~10 cu-ft), and expensive (~$120,000) conventional laser systems (1064 nm) in PCSS-based HPM applications, with an additional need for second and third harmonic generation (SHG/THG) optics to trigger wide bandgap (WBG) solids (GaN/SiC).

Solution Space: Design and implement a compact, lightweight , and inexpensive alternative for conventional high average power optical trigger (laser) system using component-level optical source(s) enabled by nonlinear solid-state source drivers to improve SWaP-C^2 index of HPM systems.

Sub-Problem: Unavailability of commercial-off-the-shelf (COTS) optical sources capable of sub-nanosecond pulse widths and tens-of-μm beam width, delivering >1-Watt power to implement as a makeshift/turnkey solution for the laser system.

State-of-the-Art (SOTA): Industrial SOTA Nd:YAG master oscillator power amplifier (MOPA) based 1064 nm picosecond lasers for high average power picosecond pulsed lasers available up to 50 W output power with a gain factor up to 40 dB (~10,000x power) with laser amplifier. On the other hand, 1030 nm fiber lasers in the same power class are available up to 200 W output power.

Deficiency in the SOTA: While high average power MOPA-based lasers and fiber lasers are capable of delivering >200 μJ pulse energies at sub-ns pulse widths, they are bulky, expensive, and nonmodular in terms of wavelength (1064/1030/2050 nm), raising a need for either total laser swap or additional optics for SHG/THG generation when alternative wavelengths are needed by the application.

Solution Proposed: Multi-stage laser diode array (LDA) driver enabled by a seed-laser-diode-driven avalanche WBG-PCSS as a compact (~1.1 cu-ft), lightweight (10–15 lbs.), and inexpensive (<$15,000) optical source replacement. This enables wavelength modularity in the optical source by facilitating the LDA module swap to accommodate the wavelength requirement of the application.

Relevance to OSPRES Grant Objective: Provides an enhanced SWaP-C^2 compliant solution for the laser (optical trigger) subsystem, with a subsequent impact on overall HPM system cost, volume, and power (optical and electrical) requirements.

Risks, Payoffs, and Challenges: Complex interconnect and thermal management system (TMS) design at high temperature (130–175°C) operation; unavailability of COTS high power pulsed laser diodes could potentially raise a need for research in laser diodes (arrays).

4.2.2 Tasks and Milestones / Timeline / Status

(A) Complete initial feasibility study for the cascaded multi-stage optical amplifier design and determine functional requirements for the laser diodes (arrays) and source driver [DEC–JAN 2020 / completed].

(B) Complete initial stage experimental implementation of the PCSS-based driver and demonstrate positive current gain using GaN-PCSS, triggered with a 404 nm laser diode. [SEP–OCT 2021 / in progress].

(C) In addition to (B), investigate potential alternatives to GaN-PCSS in both PCSS and non-PCSS domains. [SEP–OCT 2021 / in progress].

(D) Define performance metrics for PCSS-based driver and complete numerical calculations for required output current at each stage and corresponding PCSS (GaN/GaAs) operating voltages in light of electric fields required for lock-on/avalanche mode, establish real-time implementation timeline, cost estimates, jitter limitation, and explore ways to protect LDA from PCSS ringing. [MAR 2021 / partially complete / revisit after completing (B)].

(E) Demonstrate a SiC-MOSFET-powered frozen wave generator (FWG) prototype on a custom-built PCB with Cree/Wolfspeed MOSFET(s), and 50 Ω coaxial cables and/or microstrip transmission lines capable of generating chirped pulse widths. [JUL–AUG 2021 / complete].

(F) Demonstrate a MOSFET-enabled motorized FWG on a 4″ ´ 5″ PCB to enable dynamic pulse width tunability using lumped-element-based transmission lines [NOV–DEC 2021 / partially complete].

(G) Proof of concept testing of the two-stage PCSS-enabled driver system with a 50 Ω load at 1 kHz pulse repetition rate (PRR) [NOV–DEC 2021].

(H) Working prototype demonstration at ~MHz PRR with laser diode array/stack and ancillary optics based on HPM source driver needs including thermal management system (TMS). [JAN–FEB 2021].

4.2.3 Progress Made Since Last Report

(F) To address the pulse train overlap issue reported last month due to parasitic(s) along the reflected path, a chirp-capable, dynamically tunable 12-segment lumped-element-based FWG prototype with optimized reflective path has been designed and tested up to 350 V charge voltage. While the pulse overlap issue under unbalanced load configuration has been partially addressed, partial pulse train overlap still exists along the reflective path under unbalanced load conditions. Reflected path and LC tunability parameters need to be further optimized to facilitate complete discharge of a transmission line before the successive pulse propagates.

4.2.4 Technical Results

(F) A 12-segment lumped-element-based FWG has been designed with chirp-capability and dynamic pulse width tunability, facilitated by a tunable inductor–capacitor pair in each transmission line (TL) segment. Limited by the rated voltage of the tunable components, the tunable version of the prototype shown in figure 4.2.1 was tested up to 160 V, while the prototype with only fixed components has been tested up to 350 V under balanced and unbalanced load configurations.

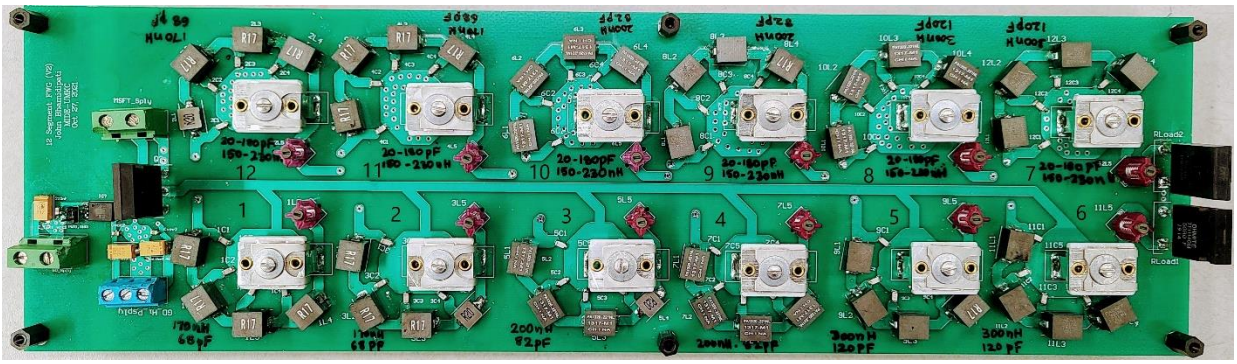


Figure 4.2.1. 12-segment lumped-element-based dynamically tunable FWG prototype with one pair of tunable L–C components per transmission line.

The characteristic impedance of the LC ladder networks was set to 50 Ω and the fixed LC components were selected to generate pulse widths between ~13 and ~24 ns, and additional tunable LC components in each segment add 2 – 5 ns. Anticipated pulse width(s) from each segment for balanced (50 Ω and 50 Ω) and unbalanced (50 Ω and 0.1 Ω) load configurations are shown in Table 4.2.1 below.

Table 4.2.1. Table showing the arrangement of lumped elements used in the TL segments and their anticipated pulse widths under balanced and unbalanced loads. *(Refer to figure 4.2.1 for TL segment layout)*

Balanced Load		
TL segments	**Lumped elements used**	**Anticipated pulse width**
1, 12	4 × (170 nH - 68 pF)	13.2 ns
2, 11	4 × (170 nH - 68 pF)	13.2 ns
3, 10	4 × (200 nH - 82 pF)	16.2 ns
4, 9	4 × (200 nH - 82 pF)	16.2 ns
5, 8	4 × (300 nH - 120 pF)	24 ns
6, 7	4 × (300 nH - 120 pF)	24 ns

Unbalanced load		
TL segments	**Lumped elements used**	**Anticipated pulse width**
1,11	3 × (170 nH - 68 pF) + 1× (200 nH - 82 pF)	14.25 ns
2,12	4 × (170 nH - 68 pF)	13.2 ns
3, 9	4 × (200 nH - 82 pF)	16.2 ns
4, 10	4 × (200 nH - 82 pF)	16.2 ns
5,7	4 × (300 nH - 120 pF)	24ns
6,8	3 × (300 nH - 120 pF) + 1 × (170 nH - 68 pF)	21.4 ns

While the experimental results with balanced 50 Ω load configuration agreed with the simulated results with up to ~50–55% power transfer, a direct impact of LC parameter tuning on peak voltage output has been observed, which needs to be studied further. On the other hand, with increase in number of transmission line segments, a consistent drop in the peak voltages has been observed from TL #1 to TL #6 under balanced load. The simultaneous switching ability of the MOSFET needs to be evaluated to validate simultaneous switching of the transmission lines. If the MOSFET is unable to simultaneously switch the lines, an alternative switch technology will be considered.

The pulse overlap issue under unbalanced load reported last month has been partially addressed. However, the delay in transmission line discharge still needs to be addressed to avoid pulse overlap completely. Parasitic(s) along the reflected path could have potentially caused a delay in the LC segment discharge that led to the pulse overlap. This effect will be studied and mitigated in the next reporting cycle along with tunable LC section implementation.

4.2.5 Summary of Significant Findings and Mission Impact

(A) The state-of-the-art COTS laser driver specifications and limitations have been comprehensively studied, and target performance metrics have been determined in terms of output current (>120-A), pulse repetition rate (>1-MHz), transient response (<200-ps risetime and <1-ns pulse width), and volume (<0.75 cu-ft). A preliminary feasibility study has signified the need for lock-on conduction mode with ~$10^{2.6}$ gain factor to drive at >1-MHz pulse repetition rate while limiting the amplification stages to 2. This reduces monetary costs to 10–12% of the conventional laser system, while achieving the expected goal of miniaturizing the optical subsystem by 90%.

(B) Pulse trigger requirements for the LDA/LDS have been identified based on Jenoptik's actively cooled quasi continuous wave vertical diode laser stacks to tailor the device parameters of the enabling switch accordingly.

(C) Silicon optodiodes have been evaluated against the identified performance metrics for the enabling switch. The testing was performed at 200 V charge voltage with laser illumination energies between 20-µJ and 200-µJ. The device performance at low optical energies (~20-µJ) did not satisfy the expected metrics in terms of R_{on} and t_{rise}. Alternative switch technologies like avalanche transistors and silicon avalanche shapers will be evaluated in the next report cycle.

(D) Numerical calculations have been completed to estimate the electric fields and corresponding voltage bias required to induce lock-on operation while exploring ways to minimize the potential risks of high jitter at ~MHz order PRR switching, power reflections due to impedance mismatch, and negative ringing currents during PCSS recovery. Expected on-state resistance and power dissipation for 50 µm and 100 µm devices in lock-on conduction mode have been calculated to estimate cooling system requirements while retaining the expected SWaP-C^2 factor.

(E) A MOSFET-switched FWG prototype implementing coaxial transmission lines has been fabricated and tested with a goal to demonstrate a tunable pulse generator capable of demonstrating chirped pulse-widths. The primary operation of a FWG has been demonstrated with up to 8 transmission line segments under balanced and unbalanced load configurations. The experimental implementation results on pulse chirp were found to be in agreement with the simulation results. However, pulse overlap, and deconstructive interference were observed in the 8-segment configuration, which will be addressed using a different transmission line topology/configuration.

(F) Tunable lumped-element-based (LC) ladder networks were considered as a potential alternative to overcome the non-ideal characteristics of coaxial lines in terms of size and weight. This also provides an advantage of integrating the transmission lines into the PCB, minimizing the distance between the switch (MOSFET) and charged lines. A 12-segment FWG capable of dynamic tunability has been demonstrated with LC ladder networks as lumped-element-based transmission lines on a 4.1″ × 14.1″ PCB under balanced and unbalanced load conditions. Multiples of 75 nH and 30 pF were used in the LC ladder networks to generate pulse widths between 13.2 ns and 24 ns. With balanced load configuration, anticipated pulse widths have been observed as

shown in table 4.2.1. However, the peak voltage output has linearly decreased as the pulse train progresses. The MOSFET with 11 ns rise-time is suspected of not being able to switch all 6 pairs of transmission lines simultaneously. If this is validated, it brings forth the need for a faster switch/technology alternative to facilitate simul-switching. Negative pulse train reflected from the 0.1 Ω load in unbalanced load configuration appeared to partially overlap with each other at voltages >75 V. This overlap could be due to the charge/discharge cycles of the parasitic(s) along the signal path that result in delays and leading to pulse overlap. This issue will be addressed in the next report cycle.

4.2.6 References

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5 Photoconductive Switch Innovation

1.1 Characterizing and Optimizing On-State Resistance in GaN:X PCSS

(Heather Thompson)

5.1.1 Problem Statement, Approach, and Context

Primary Problem: Traditionally, RF generation using photoconductive semiconductor switches (PCSS) rely on materials such as silicon (Si) or gallium arsenide (GaAs), due to their availability and low cost; however, as these applications begin to require higher operating frequencies, powers, and temperatures, with the same or reduced system form-factor, the theoretical operating limits of these materials are being reached.

Solution Space: By exploiting the 3.4 eV bandgap, 1000 cm^2/Vs electron mobility, and thermal properties of GaN, it is possible to realize pulsed-power applications requiring up to a 5 MV/cm critical field, high-frequency operation, and ~400 °C operating temperature, respectively.

Sub-Problem: One of the most important problems in minimizing conduction losses, maximizing efficiency, and reducing thermal issues in compensated, semi-insulating GaN:X (i.e., GaN:X with X=C, Fe…) PCSS-based systems is achieving <1 Ω on-state resistance by optimizing the modifiable parameters of GaN:X at the material, device, and system levels, while still maintaining quick switch turn-off time and low turn-off losses.

***State-of-the-Art (SOTA*)**: PCSS-based RF generation systems using Si, SiC, or GaAs can achieve MW-range output power, ones-of-gigawatts frequency content, and electrical efficiency of ~60% that require increased laser energies and device size to reach maximum efficiency and necessary operating power limits, respectively.

Deficiency in the SOTA**:** Si-, SiC-, and GaAs-based PCSS require ones-of-mJ of incident laser energy to achieve <1 Ω on-state resistance, leading to increased incident laser requirements, increased heating in devices, and devices that are ones-of-cm^2 in area for the necessary peak power and operating temperatures.

Solution Proposed**:** Use simulation and available experimental results, from literature and collected results at UMKC, to optimize the variable parameters of GaN:X PCSS to achieve <1 Ω on-state resistance with increased electrical and optical efficiency while maintaining a quick switch turn-off time and low turn-off losses.

Risks, Payoffs, and Challenges:

Challenges**:** The high cost of material leads to a limited number of devices available for experimental testing and analysis, requiring a majority of the optimization studies to be performed using simulation software (COMSOL and TCAD).

Risks**:** Simulation results may vary from experimental results for certain PCSS parameters due to certain photogeneration and recombination parameters not being included in models along with non-ideal, real-world experiments requiring additions such as encapsulation material or other changes not fully addressed in simulation.

***Payoffs*:** By minimizing the conduction losses in GaN PCSS, a compact, tunable RF source can be realized with increased efficiency and SWAP-C^2 capabilities.

5.1.2 Tasks and Milestones / Timeline / Status

(A) Milestone – Determine material, device, and system parameters affect on-state resistance and which of these can be best leveraged to reduce on-state losses and heating [*Estimated completion by DEC 21*].

1. Task – Literature study of photoelectric on-state resistance to understand how this parameter can be optimized to reduce conduction and on-state losses during PCSS operation *[ongoing].*
2. Task – Literature review of on-state resistance studies performed using GaN-based photoelectric devices to determine areas to further study *[ongoing].*
3. Task – Determine project milestones, tasks, and timeline for optimizing on-state resistance in GaN PCSS *[DEC 21]*.

(B) Milestone – Build model of GaN PCSS in TCAD and/or COMSOL to begin simulation studies *[OCT–NOV21].*

1. Task – Build simple, working GaN PCSS model to alter for more complex analysis of on-state resistance *[DEC 21–JAN 22]*.
2. Task – Compare simulation results with available experimental results to determine validity of models using COMSOL *[JAN–FEB 22]*.
3. Task – Set up parametric sweep studies in COMSOL *[MARCH 22]*.
4. Task – Build a working, simple GaN PCSS model in COMSOL as a starting point for more advanced modeling efforts.

(C) Completion of manuscript on optimizing on-state resistance in GaN:C PCSS *[Ongoing]*

5.1.3 Progress Made Since Last Report

(A) Literature pertaining to on-state resistance in opto-electric devices, of various semiconductor materials, has been collected and is being analyzed to determine the parameters at the material, device, and system levels that affect on-state resistance.

(B) Modeling of GaN PCSS initiated in COMSOL by using existing COMSOL PCSS application files that can be altered to model GaN PCSS devices. Work started with very simple models that can be further modified, once errors are fixed, towards completing parametric studies of minimizing on-state resistance in GaN:C PCSS.

(C) Manuscript on minimizing on-state resistance in GaN:C PCSS has been started and will serve to direct needed simulation and experimental analysis throughout the project.

5.1.4 Technical Results.

(A) There are several parameters (Figure 5.1.1) that affect the on-state resistance of opto-electric devices at the material (bandgap, necessary activation energy, compensation concentrations, etc.), device (geometry, illumination location, etc.), and system (incident photon source characteristics, encapsulation material, etc.) levels that can be altered to minimize on-state resistance, with certain parameters being more easily manipulated than others. Along with these parameters, there are also different operating and photogeneration methods used for GaN PCSS which will limit some of the device geometry and system (laser) options available for analysis.

a. Two modes of operation exist for GaN:C PCSS: linear (one carrier generated per absorbed photon) and non-linear (impact ionization utilized generating multiple carriers per absorbed photon). Linear operation is preferred due to decreased jitter and increased device lifespan (reliability)[1]. While non-linear mode would allow for reduced laser energy needs and increased responsivity, non-linear mode has not been fully demonstrated in GaN-based PCSS devices thus far, leading to project focus on linear mode operation.

b. Two photogeneration methods are available for GaN PCSS, intrinsic and extrinsic. Intrinsic generation relies on incident photons at or above the bandgap energy to activate electrons from the conduction band while extrinsic generation relies on mid-gap impurities and defects that can be activated using a photon energy below the bandgap energy. Intrinsic operation offers lower on-state resistance due to higher quantum and optical efficiency but because the absorption depth is so shallow (ones-of-microns), lateral devices must be used [2], so for this program, focus will be on lateral GaN PCSS devices relying on intrinsic photogeneration with future work possibly encompassing vertical devices activated using compact laser diode photon sources with extrinsic operation.

Figure 5.1.1. Chart of parameters affecting on-state resistance in PCSS, which will be iterated upon as the literature study progresses.

(B) Modeling of GaN:C PCSS using COMSOL has been initiated by building a simple model based off a GaAs PCSS application model available from COMSOL. This model is being modified to represent the material and geometry of the GaN:C PCSS devices that are being studied. Currently, the material properties and geometry have been altered and mitigation of errors within the simulation are being worked on. Once working models are available, parametric studies towards optimizing GaN:C PCSS parameters to minimize on-state resistance can be accomplished.

(C) A manuscript describing the parameters which affect on-state resistance in GaN:C PCSS, and how to minimize these, has been started and will serve to determine the direction of experimental and simulation analysis done as this paper progresses.

5.1.5 Summary of Significant Findings and Mission Impact

(A) A preliminary literature study of the on-state resistance of opto-electric devices began to find the parameters that affect the on-state resistance of GaN PCSS and similar devices of differing materials which will lead to the determination of what parameters can be manipulated to optimize on-state resistance in GaN PCSS, leading to a material option that provides increased efficiency and SWAP-C^2 capabilities of a PCSS-based RF generation system.

During literature review, it was found that publications in this area typically focus on vertical GaN-based PCSS devices and this has led to the conclusion that assumptions used in evaluating vertical devices need to be studied to determine their validity in lateral devices.

Due to the minimal jitter operation and increased device lifespan, focus will be restricted to linear mode PCSS operation, which limits devices to lateral geometries. Focus will also be placed on intrinsic carrier activation due to increased optical efficiency this allows for over extrinsic activation.

(B) Work began towards building a working GaN:C PCSS model using COMSOL multi-physics which would allow for parametric sweep studies to be performed efficiently.

(C) Work towards a manuscript based on optimizing on-state resistance in GaN:C PCSS has been started with the first version of the introduction written and currently being edited.

5.1.6 References

[1] J. S. Sullivan and J. R. Stanley, “Wide bandgap extrinsic photoconductive switches,” *PPPS-2007 - Pulsed Power Plasma Sci. 2007*, vol. 2, pp. 1040–1043, 2007.

[2] A. D. Koehler *et al.*, “High Voltage GaN Lateral Photoconductive Semiconductor Switches,” *ECS J. Solid State Sci. Technol.*, vol. 6, no. 11, pp. S3099–S3102, 2017.

6 Drift-Step-Recovery-Diode-Based Source Alternatives

6.1 Drift-Step Recovery Diode and Pulse Shaping Device Optimization

(Jay Eifler)

6.1.1 Problem Statement, Approach, and Context

Primary Problem: Drift-step recovery diodes (DSRDs) and DSRD-based pulsed power systems are competitive with PCSS-based systems for HPM cUAS, with the benefit of not requiring a laser. Maximizing peak power while maintaining characteristic ns-order DSRD rise times requires optimization of the DSRD device design and pulser. Other considerations are for compactness, low-jitter, cooling required, and additional pulse-sharpening device within the pulse shaping head circuit. Additional goals for pulse repetition frequency are also to be satisfied for various applications.

Solution Space: By altering DSRD device parameters (geometry, doping, irradiation), optimize single-die and stack designs for peak power and risetime within various inductive pulser circuit topologies. Also optimize the pulse sharpening device (PSD) within the pulse shaping head circuit.

Sub-Problem 1: TCAD and SPICE models of the DSRD are 40% accurate and must be improved. PSD models have not been developed.

Sub-Problem 2: Inductive pulser designs are complicated by the DSRD (and PSD) parameter variability. Use TCAD and/or SPICE models to account for variability and improve pulser design.

State-of-the-Art (SOTA): MW peak power and ns-order risetimes have been achieved in DSRD-based pulsed-power systems employing DSRD stacks for higher voltage holding and parallel lines of DSRD to increase current. PSD have sharpened DSRD pulses to 100 ps-order.

Deficiency in the SOTA: A lack of accurate TCAD and SPICE models make design of DSRD and DSRD-based inductive pulser circuit topologies (with or without PSDs) difficult to the level of tens of MW of peak power while maintaining ns-order risetime (or sharpened 100 ps-order). In addition, DSRD (and PSD) fabrication variabilities further complicate pulser design.

Solution Proposed: Develop further modeling capabilities in TCAD and SPICE for DSRD and DSRD-based inductive pulser circuit topologies to optimize DSRD and inductive pulser designs, especially for maximum peak power and minimum risetime, but also for low-jitter, reduced cooling, and compactness. Additionally, optimize pulser with PSD and pulse shaping head circuit.

Relevance to OSPRES Grant Objective: DSRD-based systems eliminate laser requirements necessary for PCSSs and are competitive in terms of thermal requirements and peak power. With sharpening, the DSRD-based systems can produce comparable risetimes. The SWaPC^2 cooling requirements of HPM cUAS systems can be solved with DSRD-based pulsed power systems, and low-jitter DSRD-based systems can be used for beam-steering in phased-arrays.

Risks, Payoffs, and Challenges: DSRD must be arrayed and staged to increase current since DSRD are limited in their ability to operate at high current densities. DSRD and PSD must also be stacked to operate at high voltages necessary for high peak power and maintain low risetimes. The stacking methods can damage dies and produce variable results in risetime and DSRD diffused doping profiles can be difficult to achieve and may require epitaxial methods. SPICE device models for DSRD are unavailable and must be developed, and questions remain about TCAD limitations for DSRD and PSD modeling.

6.1.2 Tasks and Milestones / Timeline / Status

(A) Milestone – Develop TCAD and SPICE models of the DSRD and MOSFET, respectively, that match experimental values of both the diode and circuit within 5% accuracy [*Estimated completion by AUG21*].

1. Task – Develop baseline DSRD model in TCAD [*completed JAN–APR21*];
2. Task – Develop SPICE model of DSRD within LTSPICE, an automated model parameter fitting procedure, and LTSPICE parameters for DSRD inventory [*Estimated completion AUG-NOV 2021*];
3. Task – Develop SPICE model of MOSFET within Silvaco [*JUL–SEP21*];
4. Task – Compare results of models developed in TCAD to the simulation values achieved using LTSPICE and experimentally (see Section 4.5) [*JUL–SEP21*];
5. Task – Incorporate parasitic capacitance, inductance, and resistance models for both single die and DSRD diode stacks (multiple dies in series) as well as for the DSRD-based pulser circuits [*discontinued after MAR–JUN21*];

(B) Milestone – Optimal characteristics of epitaxially-grown DSRD pinpointed from parametric study which produce the maximum waveform fidelity characteristics (e.g., maximum peak voltage, shortest risetime, highest dV/dt) [*Estimated completion by AUG21*].

1. Task – Determine carrier lifetime effect on risetime [*completed FEB–APR21*];
2. Task – Determine effect of including avalanche modeling on DSRD performance [*completed FEB–MAY21*];
3. Task – Determine effect of the width of outer edge contact on current density and breakdown in device [*discontinued after MAR–MAY21*];
4. Task – Model TCAD process in Silvaco Athena and Victory Process for DSRD diffused and epitaxial processes (and pulse sharpening devices) used for DSRD fabrication and DSRD device modeling [*discontinued after MAR–JUN21*];
5. Task – Determine optimal doping profile for Semiconductor Power Technologies (SPT) DSRD epitaxial designs [*completed MAY–JUL21*];
6. Task – Determine best doping profile from fabricated and optimal conceptual designs by comparing performance in the 2x2 DSRD pulser [***completed JUL21***];
7. Task – Complete DSRD performance study on epitaxial doping profile (n-side) variation manufactured by SPT in conjunction with LSRL [***completed JUL21***];

8. Task – Complete gain study for DSRD stack height and gain staging design [***completed JUL21***];
9. Task – Verify accuracy of TCAD simulations by comparing to experiment for DSRD-based pulser circuit topologies [*JUL–AUG21*];
10. Task – Perform first semiconductor opening switch (SOS) TCAD simulations for DSRD vs SOS mode of operation [SEP21];

(C) Milestone – Pulse sharpening devices developed within TCAD which improve the risetime and peak voltage of the IES pulse generator developed in Section 4.5 [***transitioned to Section 4.7 JUL21***].

1. Task – Develop preliminary pulse sharpening devices (PSD) models within TCAD [*discontinued after DEC20*];
2. Task – Develop standard PSD models within TCAD to reproduce results from published work [*discontinued APR–JUN20*];
3. Task – PSD simulated with DSRD 3-stack for more complete DSRD-based system modeling excluding only the primary switch model [*APR–JUN20*];
4. Task – Determine current carrying capacity of PSD and DSRD stacks [*discontinued MAR–JUN21*];

6.1.3 Progress Made Since Last Report

(A.2) The LTSPICE DSRD model parameters have been extracted with an automated system to improve the accuracy and development time for the model parameters. Both forward IV and reverse CV curves have been accurately fit for legacy, SPT generation 2, and epitaxially grown (from an outside vendor) DSRD in our inventory and will be applied to more incoming DSRDs. SPT gen2 DSRD have undergone a repeatability study on measurements and these measurements have been averaged and used to develop LTSPICE model parameters. Reverse recovery test (RRT) curve fitting has been automated for both a transit time for each forward/reverse voltage pairing in the RRT and a constant transit time for all voltages. A constant transit time can be used that accurately models the experimental RRT in simulation.

6.1.4 Technical Results

(A.2) An automated procedure for extracting model parameters for the LTSPICE DSRD model was developed and employed. Model parameters for the forward IV response were extracted and included: saturation current (IS), emission coefficient (N), forward knee current (IKF) and series resistance (RS). Model parameters were also extracted for the reverse CV and included: zero-bias junction capacitance (CJO) and grading coefficient (M). Data from the reverse recovery tests allows the transit time (TT) parameter to be set for each RRT forward and reverse voltage. Also, a constant transit time can be set for all voltages with little error. These are all the parameters necessary for the LTSPICE standard Berkeley style level 1 diode model and completes the parameterization of the model which next needs to be studied in pulser simulations with comparison to experiment.

For extracting parameters from the forward IV, the IKF and RS parameters are set to 0.01 initially as these have shown to be reasonable values from previous parameter extractions without an automated method. Next the IS and N parameters are swept through some range of values and used in LTSPICE simulations to generate the forward IV curves with the automated method (generates thousands of LTSPICE simulations). The simulated and experimental forward IV curves are compared by using the average absolute deviation (AAD). Working values of AAD are determined through visual inspection of the experimental and simulation forward IV curves. Total AAD lower than 1×10^{-4} resulted in close forward IV curves. RS is then adjusted to better fit the curve and values of 0.01, 0.05 and 0.1 Ω were used to reduce the number of simulations and resulted in better fit forward IV curves. Additional fitting using a larger range of RS values and IKF can fit the forward IV even more closely and will be performed in the future as newer DSRD are tested and simulated. In Table 6.1.1 are shown the legacy diode numbers, their fitting error (AAD), and DSRD forward IV parameters.

Table 6.1.1. Table of legacy DSRD, their fitting error, and their forward IV parameters using the automated procedure.

diode	error	is	n	ikf	rs
d509	9.08E-05	4.20E-08	1.46	0.01	0.1
d508	3.62E-05	1.50E-09	1.08	0.01	0.05
d506	5.90E-05	1.10E-08	1.3	0.01	0.1
d505	2.73E-05	1.10E-09	1.08	0.01	0.01
d504	2.70E-04	1.89E-07	1.74	0.01	0.05
d381	3.34E-05	6.70E-08	1.38	0.01	0.1
d380	4.88E-05	1.21E-07	1.44	0.01	0.01
d366	7.01E-05	1.10E-07	1.52	0.01	0.01
d513	9.07E-05	4.70E-10	1.05	0.01	0.01
d512	1.57E-04	1.3E-09	1.1	0.01	0.01
d364	3.21E-05	1.90E-08	1.24	0.01	0.1
d1	3.41E-05	2.10E-08	1.24	0.01	0.1
d363	6.77E-05	3.40E-08	1.33	0.01	0.01
d319	6.92E-05	1.70E-08	1.34	0.01	0.1

The green highlighted rows in Table 6.1.1 are for fitting error that is low enough for forward IV curves to be close upon visual inspection. The white highlight is for a device that is close to being fit well and the red highlight is for a diode that must have the parameter space more closely explored to fit well, possibly including a larger range of RS and IKF with IKF mostly necessary for very close fits.

In Figure 6.1.1 are shown the forward IV curves for two experiments (blue and yellow), average of experiments (black, open), and fitted LTSPICE simulation (orange). This

curve fitting is for generation 2 DSRD 2-2 and is only up to the maximum 3.4 V used in experimental testing. Such close fitting can allow for diode specific parameter fitting but is especially useful for somewhat different batches of diodes. The error bars show the measurement accuracy and/or variability in single device operation in measurement. The result is for a forward IV with only 2 out of 4 good measurements that showed higher forward IV variability in current and was selected for ease of viewing the error bars.

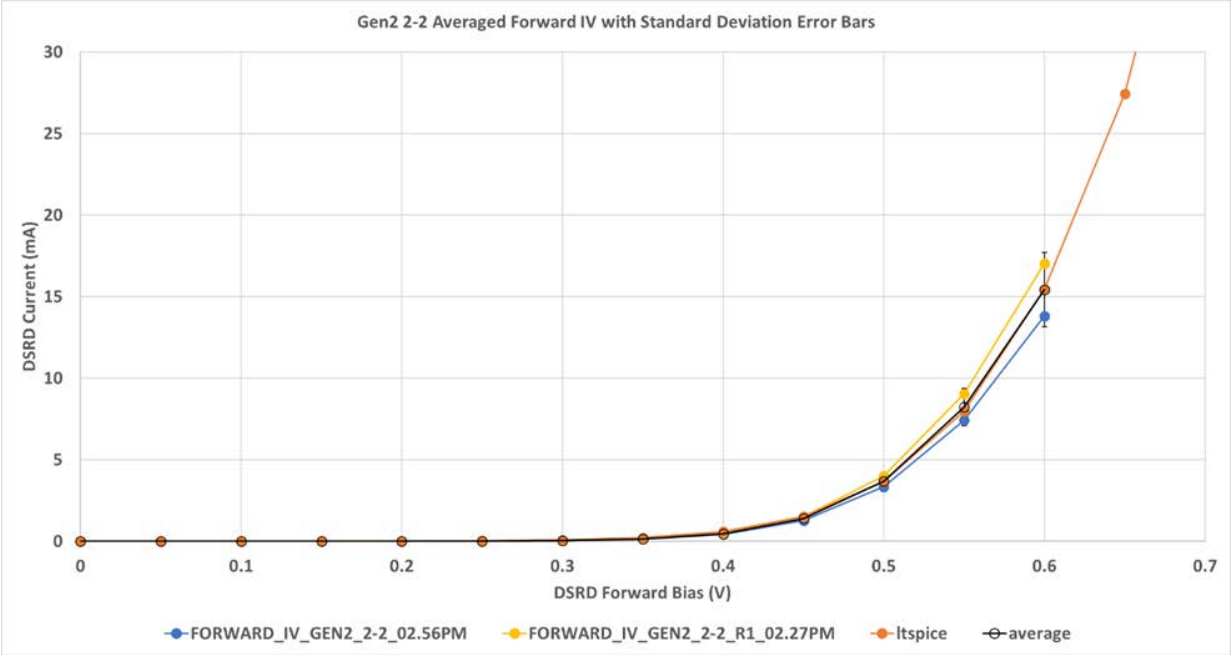

Figure 6.1.1. Forward IV comparison between experiment and simulation. This fitting is for generation 2 DSRD 2-2 and shows the possibility of device specific parameterizations.

The reverse CV curves were fit after the forward IV since the forward IV parameters affect the capacitance fitting. The CJO parameter comes directly from the impedance spectroscopy measurement of the reverse CV curve. The grading coefficient M is then fit using the experimental CJO and the junction potential (VJ) is set to the default 0.75 value. Simulations to adjust VJ show only small fitting improvements are possible. LTSPICE simulations for the reverse CV are costly and the M parameter is varied from 0.2 to 0.5 with ~0.1 steps. In Figure 6.1.2 is shown the reverse CV fit for SPT DSRD generation 2 1-1.

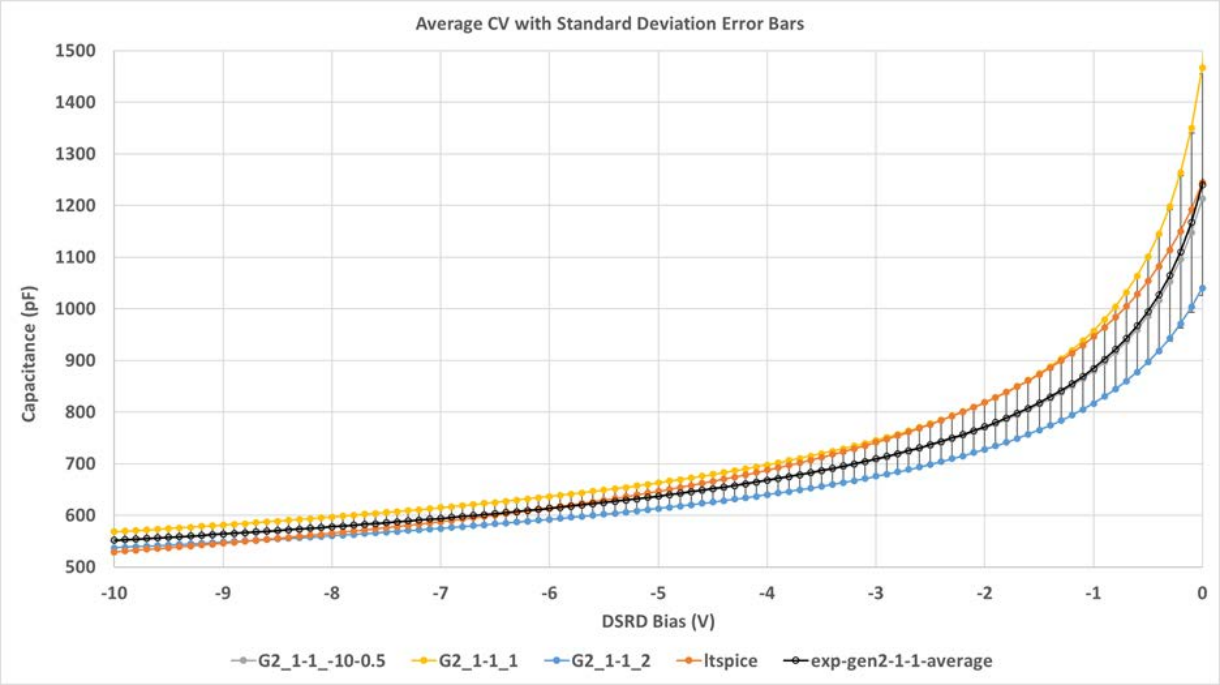

Figure 6.1.2. Reverse CV comparison between averaged experiment (black, open) and LTSPICE simulation (orange). The three experiments are shown in (grey, yellow and blue).

The lower reverse bias portion of the reverse CV curve is not fit as well in all the CV curves between experiment and simulation although CJO is set to the experimental value. An improved model may be necessary to have a very close fit to the experimental reverse CV since the LTSPICE level 1 model uses a simple graded capacitance model, but such a model has not been located yet.

The reverse recovery testing (RRT) can be fit with the transit time (TT) LTSPICE parameter in the diode model. The experimental RRT has been performed over a range of forward and reverse voltages. For each forward and reverse voltage pairing used in a RRT, a unique TT value can be derived from LTSPICE simulations. In addition, a constant TT can be used for all forward and reverse voltages that is still a close fit in recovery time to the RRT curve. In fact, the constant TT used can be varied and still be reasonably accurate over some range. This allows one LTSPICE DSRD model to be used for all the standard diode RRTs. Further studies can show if a constant TT in the DSRD model can predict pulser performance over a range of trigger durations and prime voltages used, using the same methods as used for RRT fitting. It may be that a constant TT is not usable (RS complicates in pulser performance) and the TT varies with trigger duration and prime voltage in some observable manner.

More DSRD will be fit with the automated procedure including larger stack sizes (legacy 7- and 13-stack, and SPT gen2 1-stacks have been fit), SPT generation 2-round 2 epitaxy

DSRD, and newer 1600 series 7-stack epitaxy DSRD. The new model parameter fits can then be simulated in the single bar pulsers and compared with experiment to determine the value of device specific parameterizations with the currently used models that will fit pulser experiments. Some work has begun in employing the more advanced Philips diode model in core-Smartspice of Silvaco TCAD but it lacks a recovery time model, while the HiSIM diode model in Smartspice does have a recovery time model (programmed HiSIM core-Smartspice model buggy). These are only usable for 1-stacks due to convergence issues in the programmed models and therefore can be used for the 1-stack SPT generation 2 DSRDs.

6.1.5 Summary of Significant Findings and Mission Impact

DSRD TCAD simulation started by replicating published TCAD DSRD results and then simulating devices similar with actual in-house DSRD. The variation of the sinewave pulse voltage input magnitude and period on DSRD charge storage were collected. Charge storage timing (when the diode empties charge stored from forward pulsing) of ~50% was achievable with sufficiently long voltage input period which is necessary for maximum reverse current cutoff.

DSRD stacks, as opposed to individual die DSRD, were simulated showing reduced risetime from single die to 5-stacked DSRDs consistent with published and earlier in-house data. Series resistance to model metal resistance between DSRD in stacks and doping variability in stacks was also modeled in TCAD showing metal resistance must be large to have an impact on peak voltage and risetime and that doping variations proportionally effect risetime.

(A.1) Accurate DSRD TCAD models have been developed that include both carrier-carrier scattering and Selberherr breakdown and are suitable for DSRD operation below the dynamic breakdown threshold. Peak voltage and risetime were limited by the breakdown model and more closely match experimental pulse data.

(A.2) A new DSRD LTSPICE model has been developed following the method used for developing a TCAD SPICE MOSFET model and by matching too experimental standard diode tests. The forward I-V and reverse C-V have been well matched using a 7-diode model for a 7-stack DSRD, as opposed to using only a 1-diode model for all DSRD stack heights. The reverse I-V and forward C-V are generally more problematic to fit to and proved to be so. More research and effort will be necessary to improve these matches and understand the impact on pulser simulation. The reverse recovery experiments have also been well matched (even for a single transit time over different reverse recovery testing voltages) and complete the matching of all the standard diode tests. Pulser performance has been difficult to assess due to the experimental data gathered thus far. The new DSRD LTSPICE model will also enable improvements in the TCAD SPICE MOSFET model. Overall, the new DSRD model represents a vast improvement over the previous model but has yet to include breakdown effects possible in the TCAD DSRD model and therefore breakdown limits of DSRD operation. A new automated fitting procedure now allows the model parameters to be more closely

and quickly fit, has been used to fit various batches of different DSRD, and has used averaged curves (for improved measurement) when available.(A.3) Work on TCAD SPICE MOSFET models has been done for the primary switch model (MOSFET) with conversion of the code to TCAD SPICE being partly completed to allow for modeling the complete DSRD-based pulser system (except driver). However, the conversion to TCAD of the MOSFET primary switch model, developed by CREE, to TCAD SPICE is complicated by having to develop custom behavioral models in TCAD SPICE which would be high-risk. Instead, a published model usable in TCAD SPICE was implemented and fit to the datasheet and then tested in a DSRD pulser simulation. The new MOSFET SPICE model usable in TCAD showed improvement in not having a first output pulse peak that was higher. This higher pulse had occurred in the TCAD MOSFET model (not SPICE model) and had not occurred in the voltage-controlled resistor MOSFET model (inaccurate model). Further refinement and testing of the new MOSFET SPICE model for use in TCAD has been more closely fit with the Cree LTSPICE model and compared to the Cree datasheet. The model can also be adapted to a new MOSFET in use within current DSRD pulsers. Further fitting can still be accomplished and matching both the Cree datasheet and LTSPICE model for gate charge and switching characteristics can be completed with more research into the test circuits used which are commonly not well explained in datasheets.

(A.4) LTSPICE, TCAD and experiment have been compared for the single bar pulser using a 7-stack DSRD, however there is some discrepancy for these experiments with earlier experiments (which the LTSPICE and TCAD simulations match better with) most likely due to the variability in DSRD and some to the new DSRD switch integration used for ease of switching out DSRD of various stack heights and combinations. As more experimental data is acquired for the pulsers the comparisons with simulation will yield more useful results. The 2x2 DSRD pulsers have been compared to TCAD simulation incorporating the latest TCAD SPICE MOSFET models showing some similarities in predicted peak voltage and risetime, but the most significant result is the matching of the experimental optimum trigger duration of 340 ns with TCAD results. LTSPICE simulationshave been performed with the new DSRD LTSPICE models and show the standard diode model used can match experimental peak voltages and risetimes but only by adjusting mainly CJO parameter. Without adjust there is considerable error in simulated results. Better diode models exist that incorporate impact ionization effects and recovery time modeling the later of which circumvents CJO adjustment. With further experiments and simulation refinement it is expected that the models will be predictive of experiment within the quality of the experimental data and models used.

(B.1) DSRD risetime performance was collected from TCAD simulations for variable carrier lifetime. Changes in lifetime had no significant effect on risetime other than the output pulse starting earlier.

(B.2) DSRD peak voltage and risetime were simulated in TCAD to include avalanche modeling or not. TCAD avalanche models limited peak voltage and risetime at the

load over a range of voltage input magnitudes. A TCAD parameter study for DSRD stack height and DSRD area for several doping profiles with and without avalanche modeling was performed (Spring 2021 UMKC OSPRES Grant Review and Technical Exchange). The avalanche model and model parameters were also modified to account for dynamic breakdown rather than static and then compared to the no avalanche case and experimental data. From the improved avalanche modeling and TCAD parameter study, the optimal area of the DSRD can be obtained. However, for the 500 V voltage input magnitude used, the DSRD output were all in breakdown and are not predictive of non-breakdown behavior. Future studies for optimal area will include a range of voltage magnitudes to study DSRD performance and breakdown.

(B.4) TCAD process and device modeling for the development of process steps and their resultant doping profiles and device operation was begun. This modeling will enable a connection between the fabrication parameters and the device operation for DSRD (and PSD).

(B.5) Exponential doping profiles were shown (via TCAD) to outperform Gaussian and error function profiles slightly. Exponential profiles have an optimal minimum doping of 5×10^{13}–$1x10^{14}$ dopant atoms/cm^3, while Gaussian and error function profiles have an optimal minimum doping of 1×10^{13}-5×10^{13} dopant atoms/cm^3. Further exponential doping parameter studies were carried out in circuits A and B of Figure 4.2.1 (see JUN 2021 Grant Report) which included a broader doping parameter space for minimum doping, junction placement, basewidth and peak doping over a wider range of voltage input magnitudes (for breakdown limitations). The results are similar to before and show the optimally performing doping profile has a minimum doping of 5×10^{13}, no basewidth, junction placement of 95 µm, and peak doping of 1×10^{18} (p-side) and 1×10^{19} (n-side) dopant atoms/cm^3. A comparison was made for the optimal exponential doping profiles to optimal error function, LLNL and SPT DSRD designs within the 2x2 DSRD pulser system. The TCAD study showed the exponential doping profile performs the best overall when considering peak voltage, risetime, voltage riserate, maximum reverse current, FWHM pulsewidth, prepulse and gain. Epitaxy designs with realistic deviations from the ideal exponential profile from the SRP data were shown in TCAD to not significantly affect the performance.

(B.7) A more complete gain study for varying prime voltage input and stack height was completed. The results show a variety of considerations must be made for determining the better stack heights to use in DSRD pulsers. The design of the pulsers can be improved when considering the gain staging in multi-staged DSRD pulsers as caused by the DSRD stack heights used. The 7- and 13-stacks showed the best gain. However, the peak voltages were best for the 13-stack while the 26-stack required unrealistic MOSFET currents to achieve its maximal peak voltage (or gain). For gain per die within a DSRD stack, 1-stacks showed the best gain per single and showed that gain ‘efficiency’ drops with stack height. Still, higher 7- and 13-stacks had the highest gain. How best to use this new data for DSRD pulsers is under discussion.

(B.10) First semiconductor opening switch (SOS) TCAD simulations have been performed for demonstrating a hgiher current density mode of operation. Future SOS TCAD simulations can help delineate the difference in DSRD and SOS for current density snappy recovery according to doping profile and mode of device operation.

(C.1) Pulse sharpening has been verified for PSD devices for the standard design and another non-conventional design. The PSD was also modeled within a DSRD-based pulser circuit combining for the first time TCAD modeling of both DSRD and PSD together within the same circuit with only the primary switch model not included.

(E) DSRD pulser circuits for the single-bar (Circuit B of Figure 4.2.1) and 2x2 (circuit C of Figure 4.2.1) have been simulated within TCAD allowing the use of a TCAD DSRD model, whereas in SPICE no accurate DSRD SPICE model is available. Currently, the primary switch MOSFET is modeled in TCAD, as well, but SPICE models can also be developed for the SPICE within TCAD as and will allow for better use of computational resources within TCAD. The MOSFET model and pulse repetition are being studied in detail to more closely match experiment and TCAD.

6.2 Pioneering Drift-Step Recovery Diode Processing and Manufacturing

(Alex Usenko)

6.2.1 Problem Statement, Approach, and Context

Primary Problem: DSRDs have not increased in performance due to deep diffusion manufacturing since the 60's. Their voltage-to-risetime, dV/dt remains on the order of 10^{12} V/s. To achieve the 10^{13} V/s (10 kV/ns) voltage-to-risetime required by an all-solid-state HPM pulse generator in support of the Naval afloat mission, improving DSRD manufacturing techniques is critical.

Solution Space: Leverage applicable concepts from the mainstream silicon chipmaking industry and apply new manufacturing methods to DSRD processing.

Sub-Problem 1 – Diode silicon surface termination/passivation: The SOTA uses a diode termination by a vertical wall. This design results in low breakdown voltage as it is limited by surface breakdown. To increase the diode breakdown voltage closer to the bulk silicon breakdown voltage value, the vertical side wall design must be avoided.

Sub-Problem 2 – Stacking of DSRD dies: The SOTA is based on soldering of diode dies into a stack, which limits the stack lifetime to below 10^{12} pulses. Also, the SOTA did not apply the methodology of stacking wafers first, then cutting into dies. Switching to wafer level stacking will decrease the number of stacking operations by more than 100x.

Sub-Problem 3 – Packaging of stacked dies: *The* SOTA uses bare stacked DSRDs. Mounting the bare stack into a press-pack type package will improve long term stability, such that the stack will survive a much higher number of pulses before it burns out.

State-of-the-Art (SOTA): In a recently published paper (2019),[1] the Russian St. Petersburg team at the Ioffe institute reported achieving a peak current density of 5 kA/cm^2 with a rise time of the output pulse front of ~2.3 ns, and a peak voltage across the load of 900 V (i.e., the peak switching power is 4.5×10^6 W/cm^2). The St. Petersburg team utilized deep diffusion technology. A competing team at Ekaterinburg, Russia [2] reports similar pulse performance. Both teams use outdated deep diffusion technology. As one can see, there has not been any significant improvement in DSRD pulse performance since the pioneering work done in 1960 [3].

Deficiency in the SOTA: First, no DSRDs have been manufactured using epitaxy technology with doping profile optimization. Second, no DSRD processing method exists that integrates side passivation with silicon dioxide. Finally, an acceptable DSRD stacking process has yet to be developed.

Solution Proposed: Manufacture DSRDs within the continental United States using an epitaxial growth process leveraging the optimal characteristics (e.g., doping profile, carrier concentration) determined through the work performed in Section 6.1 and through working with industry partners at Semiconductor Power Technologies (SPT), Livermore Semiconductor Research Laboratories (LSRL) and Lawrence Livermore National Laboratory (LLNL – Voss Group).

Relevance to OSPRES Grant Objective: DSRD manufacturing technology is a major building block of short-pulse high-peak-power defense systems. Our new disruptive process flow for DSRDs enables not only manufacturing of DSRDs at scale, but within the continental United States (CONUS). In doing so we will redefine the SOTA by producing optimal DSRDs. Further, DSRDs will be used within best-in-class HPM pulse generators which become part of more advanced defense systems within the Navy arsenal.

Risks, Payoffs, and Challenges:

Risks: As the process of producing DSRDs using epitaxial growth with doping profile design is novel, uncharted territory, there is inherent risk to its success. Additionally, post-processing methods based on the discussions provided in the ***Sub-Problems*** section are not well-established.

Payoffs: Replacing traditional deep diffusion technology with a new process integration scheme would allow better DSRD pulse performance. Electrical breakdown voltage, reliability, and lifetime are expected to increase, and rise time on a load is expected to decrease.

6.2.2 Tasks and Milestones / Timeline / Status

(A) Milestone – Produce epitaxial DSRDs that contain optimal exponential doping profiles and carrier concentrations /estimated *FEB22*.

1. Task – Design of experiment on 25 wafers through negotiations with vendors / *MAY–JUL21* / CompletedTask – Perform DSRD stack epitaxy on 13 wafers at SVM Inc., and 25 wafers at LSRL / *JUN–AUG21* / Completed.

2. Develop process integration scheme that uses epitaxy instead of deep diffusion / *JUL–OCT21 /* Completed.
3. Compare traditional DSRD technology and suggested integration scheme. List disadvantages of traditional processes and define potential advantages of new processes / MAY–NOV21 / Completed.
4. Run Gen2 and Gen3 lots. Gen2 is on wafers with epi from SVM, Inc., Gen3 is on wafers with epi from LSRL. Gen2 uses the same BEOL as Gen1. Run BEOL of Gen3 – using our new patented processing scheme – Si_3N_4 masking, TMAH etch, oxidation, selective electroless metal deposition, wafer bonding, sawing into diode stacks / OCT–FEB22.
5. Submit Gen2 and Gen3 diode lots to UMKC team for pulsed performance measurements; collaborate with team on determining optimal doping profile through DoE analysis by Minitab software / OCT21–FEB22.

(B) Milestone – Develop diode separation technique while keeping wafer integrity / Estimated completion FEB22.

1. Design lithography masks for short loop experiment, submit order to vendor. / MAR–APR21 / Completed.
2. Design short loop experiment for V-groove etching for diode separation. / MAR–APR21 / Completed.
3. Run short loop experiment for the diode separation by anisotropic etch; analyze results / MAY–OCT21 / Completed.
4. Based on results of previous short loop run, adjust equipment and process recipes to achieve sufficient etch uniformity across the wafer. Run on updated equipment and recipe to prove etch uniformity. / Estimated JAN22.
5. Design lithography masks for epi DSRD run; submit order to vendor. / OCT21 / Completed.
6. Run Gen3 lot through V-groove etch step; transfer lot to next process step. / estimated DEC21.

(C) Develop Ohmic contact deposition technique integrable with epitaxy, diode side termination/passivation, and wafer bonding steps / estimated AUG–NOV21.

1. Design short loop experiment to determine technical feasibility of selective electroless deposition of metal stack as a method of Ohmic contact forming in the DSRD process integration scheme. / OCT21 / Completed.
2. Determine vendor from which to order electroless deposition kits; obtain quotes, order, receive the kits. / OCT21 / Completed.
3. Run short loop experiment – nickel-copper-tin stack electroless deposition on a blanket wafer. Analyze results. / Estimated NOV21.
4. Develop process recipe for the metal stack deposition to use in Gen3 DSRD lot manufacturing / estimated NOV21.

5. Run the selective metallization step on Gen3 lot; transfer the lot to next processing step. / estimated NOV21.

(D) Develop wafer stack bonding technique integrable with the rest of Gen3 process flow / estimated SEP–NOV21.

1. Design short loop experiment for bonding 2 blanket wafers with Ni-Cu-Sn layers by solid–liquid interdiffusion. / SEP21 / Completed.
2. Run 2-wafers short loop experiment. Analyze results. / estimated OCT–NOV21.
3. Test technical feasibility of multiple wafer bonding by bonding 10-wafer stack / estimated NOV21.
4. Upon proof of technical feasibility of 10-wafer stacking, develop process recipe to use for processing of Gen3 DSRD lot / estimated NOV21.
5. Run wafer bonding step on Gen3 lot, transfer the lot to next processing step. / estimated DEC21.

(E) Develop wafer stack sawing technique into DSRD stacks, integrable with the rest of Gen3 process flow / estimated NOV–DEC21.

1. Design sawing process using Disco saw available at Semiconductor Power Technologies for cutting 10-wafer stack / estimated DEC21.
2. Run short loop cutting of blanket bonded 10-wafer stack. Analyze results. / estimated DEC21.
3. Develop process recipe for Disco saw tool to use for Gen3 lot. / estimated DEC21.
4. Run sawing step on Gen3 lot / DEC21]

(F) Develop diode side passivation process integrable with the rest of DSRD process flow.

1. Test compatibility of thermal oxidation for the diode side passivation with preceding anisotropic etch step / NOV21.
2. Alternative diode side passivation process: design short loop experiment on room temperature oxidation by forming porous Si film and oxidizing the porous film / APR–OCT21 / Completed
3. Run part of Gen3 lot using the oxidized porous Si as diode side passivation.
4. Second alternative diode side passivation process: Design short loop experiment on room temperature oxide deposition from oversaturated fluorosilicic acid / MAY–JAN22.
5. Run part of Gen3 lot using the oxidized porous Si as diode side passivation / DEC21.
6. Choose the best from 3 methods of diode side surface passivation techniques / JAN22.

(G) Develop a DSRD process based on out-diffusion (opposite to traditional in-diffusion process).

1. Process Gen4 lot based on process integration scheme described in our patent application filed in Aug. 21.

(H) Find vendor that manufactures press-pack parts, order the parts, and encapsulate the DSRD stacks into the press-packs.

6.2.3 Progress Made Since Last Report

(A4) Traditional DSRD technology and suggested integration scheme were described and compared. Results presented at 3 conferences [4], [5], [6]. Disadvantages of traditional processing advantages of new process scheme were also described.

(A5). In Gen3 process flow, 24-wafer lot passed processing through several next steps: Silicon nitride mask have been deposited using vendor Nova, mask for lithography have been designed, mask ordered to vendor, finished masks received from vendor, Gen3 wafer lot is currently being processed at lithography step – wafer dehydration baking, priming with adhesion promoter, photoresist spinning, photoresist soft baking, exposure, resist development, post litho inspection.

(A6) Several more wafer from 13-wafers Gen2 lot were fully processed. Non-stacked DSRDs were manufactured.

(A7) Non-stacked Gen2 DSRDs were submitted to the UMKC pulse performance measuring team. The team will first characterize single diodes, then characterize a “loose stack”.

(B3) Samples with V-grooves were analyzed with SEM. Significant non-uniformity of anisotropic etch across the wafer were discovered on grooves in 400-micron windows. To improve uniformity in next runs, new labware – advanced wafer dippers were ordered.

(C2) Technical featurability run on electroless plating with Palladium seed and Nickel film finished. Pd/Ni stack successfully deposited. Now samples are under material properties analysis.

(A) Setup for pulsed performance of DSRD have been fully assembled at industrial partner SPT, Inc (Semiconductor Power Technologies) in Manhattan, KS. This will allow much faster measurement turnaround of DSRD manufactured by SPT, Inc. Thus eventually will allow faster DSRD manufacturing process development.

6.2.4 Technical Results

(F4)

Technical feasibility run for room temperature deposition of fluorinated SiO2 have been successfully finished. Having both – room temperature and fluorine bring advantages over the diode surface passivation techniques known in the art. Room temperature – as opposed to thermal oxidation - bring an advantage of easy integration into total diode

process flow, it is compatible with the rest of diode manufacturing steps. Fluorine brings similar advantage as adding hydrogen – both are extremely active in passivating of silicon surface dangling bonds. Though, as Fluorine is heavier than H, its effect is stable up to about 700C. Thus, thermal processing needed at the end of diode manufacturing – forming metal silicide contacts, etc. – are compatible with SiO2:F deposition. By implementing this novel process for diode side surface passivation we expect significant reduction on reverse bias leakage current, and increased breakdown voltage.

The SiOF deposition have been performed the following way. Mixture of hexafluorosilicic acid and silicic acid have been stirred overnight to get saturated solution. Then the mixture was filtered to remove unsoluble part. Then the mixture turned into oversaturated conditions by heating to 60C and adding boric acid. Wafer was dipped into oversaturated solution for 2 hours.

Ellipsometry shown that the thickness of the native oxide was found to be 1.48 nm whereas that of the grown layer was found to be 6.84 nm. Elemental composition by XPS on Fig. 6.2.1 shows expected Fluorine in the grown film.

Even though the SiOF room temperature deposition is experimentally confirmed, the deposition rate found to be much slower than expected. Next run being planned with an adjusted recipe – to achieve deposition rate on order of 100 nm/hr.

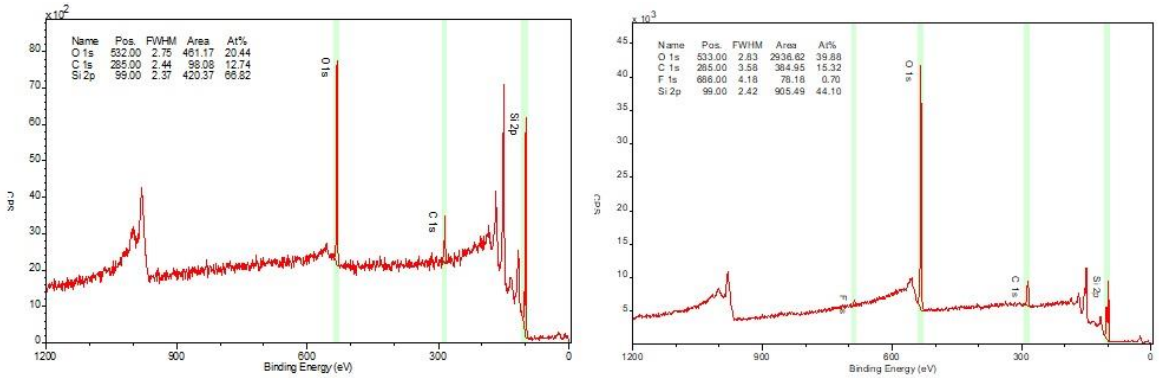

Figure 6.2.1. Elemental composition by XPS from the same wafer. Left – area with just native oxide. Right – area with fluorinated oxide deposited at room temperature from supersaturated fluorosilicic acid. Courtesy S.Dhungana.

(A4). An additional run was performed to further develop anisotropic etch of V-groves in TMAH. For TMAH concentration and etch temperature, previously used recipe – 5% at 75C looks optimal. Though comparison of SEM images Fig.6.2.2 shows that for 200 um and 250 um mask windows, the shape of the v-grooves is near perfect, but for wider windows we see truncated triangles, and the grove depth is significantly different from one location to another. It indicated spatial etch nonuniformity. One of reason is – labware used is not good for uniformity. Another reason is – masking by hydrogen bubbles sticking to etched surface. Next run being planned – to solve these issues – buy better labware, and adding surfactants – Triton-100, acetic acid, IPA, etc.

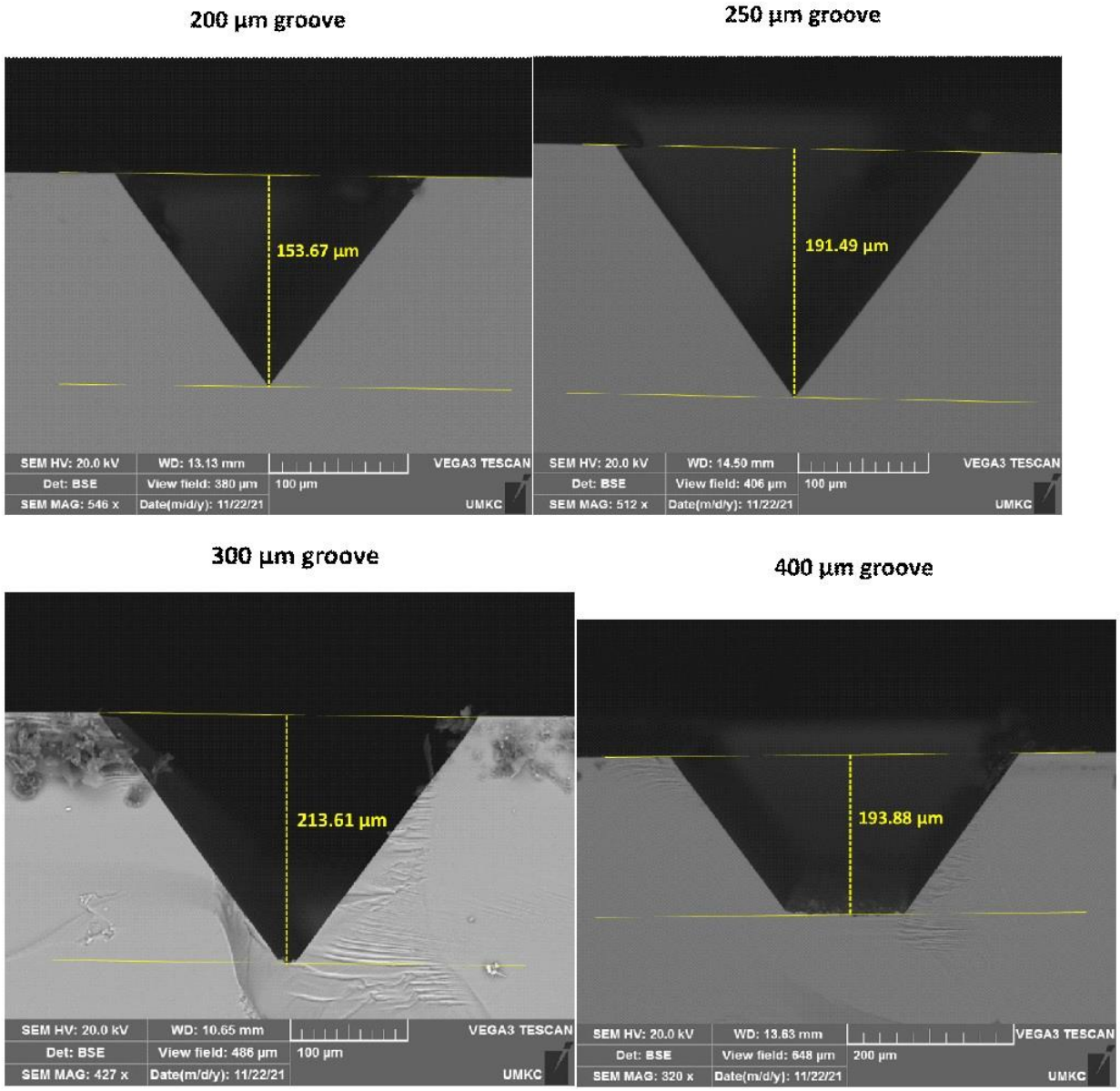

Figure 6.2.2.V-groove shape for various mask window width – 200, 300, and 400 microns. Courtesy S.Dhungana.

(F.4) Stain etches. The stain silicon etch (sometimes called “black silicon”) is another method to improve the diode side surface passivation. Technically it is performed by pouring wafer into 1000:1 mixture of concentrated HF and HNO3. In this run, only <111> wafers were used. The reason is, we need to cover side slopes ofV-grooves. And these are <111> facets. Experimental split included 1, 5, and 25 minutes etch time, and wafer with various dopants, and dopant concentrations. The groove surface has p+ Si at the top, gradually lowering p concentration toward p-n junction, some intrinsic Si, gradually increasing n-doped Si, and eventually heavy Arsenic doped Si near the groove bottom.

Thus, the goal was – whether we can form stained Si layer over all these types of silicon, while using the same process recipe.

Figure 6.2.3. Example of stained silicon wafer.

Run confirmed that stains form successfully on all variously doped wafers. Which mean, it likely can be used as new method of diode surface passivation, with potential to significantly lower leakage current and increase breakdown voltage. Extreme simplicity of the method and compatibility with the rest of our process flow is also significant advantage. Fig.6.2.3. shows an example of stained wafer after just 1 minute etch. Observation of various colors means the method has very fast growth rate – near 0.5 micron/minute, thus process is very inexpensive.

Seeing the rainbow picture though indicates the thickness is quite non-uniform. And unlikely there is a method to improve the uniformity. The matter is, all HF/HNO3 etch is autocatalytic. So, say, stirring will unlikely help, rather halt the process. The autocatalytic reaction randomly creates anode and cathode areas, current discharges in this “battery” forming oxide on one side, and dissolving oxide on another side. On the other side, thickness uniformity is not much of requirement for this – surface passivation application.

Let us consider the stain layer composition and see whether it bring us advantages. Fig 6.2.4 shows typical XPS elemental spectra across thickness of the stain layer. We see, that Oxygen tail propagates to about 0.5 microns. Likely, this is the thickness of our stain layer. Structurally, the stain layer is porous silicon. When we do HF/HNO3 etch, pores mostly continue to grow on very bottom of each pore. When we take the wafer from the acid, rinse and dry, oxidation pore walls start. The total surface area of pores is very high, therefore just forming native oxide on the pore walls can result in sealing of the pores near layer surface, thus converting it into the continuous SiO2. Which is good for our purpose – we are getting a good protective layer. Below 200 nm on the Fig.6.2.4 we observe drastic drop of Oxygen content. Tentatively, we can hypothesize that between 200 and 500 nm we have sealed pores. Notice, each pore is surrounded by depleted region. It means we do not have any material interface between porous Si and bulk Si.

No interface is – no interface states – an ideal diode surface passivation. Though, to either confirm or deny the hypothesis, very high resolution FIB-SEM imaging is required.

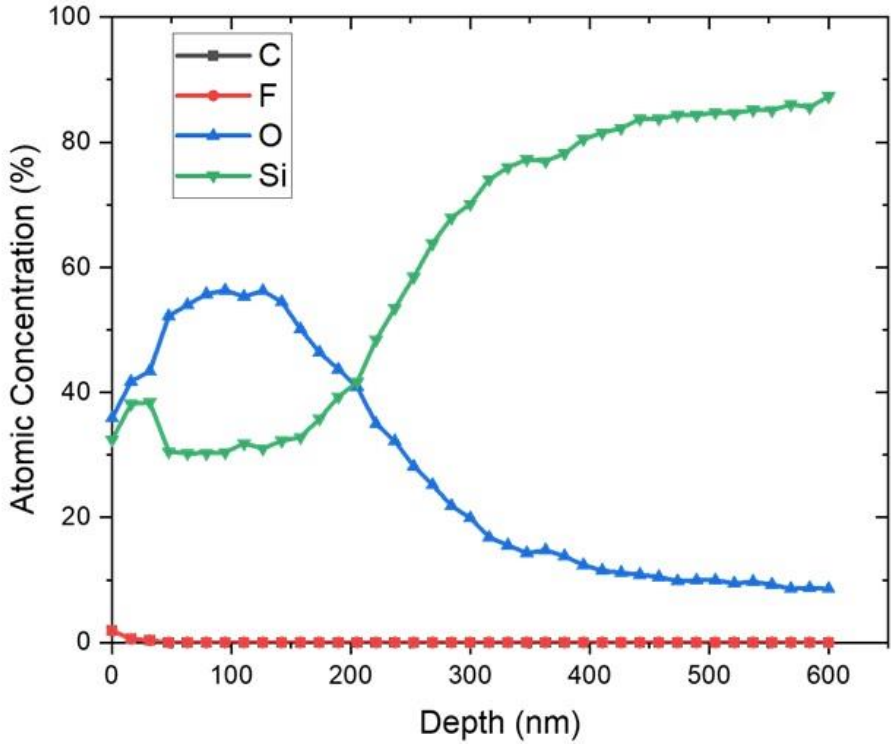

Figure 6.2.4. Typical elemental composition of black Silicon layer. Courtesy S.Dhungana.

Figure 6.2.5. Typical sample upon Palladium-than-Nickel electroless plating.

An electroless plating process recipe have been developed on base of original recipe by Val Dubin. As known from literature, seedless metal plating directly onto Silicon was successful for 2 metals only – Platinum and Palladium. Generally accepted theory is that catalytic reaction is required to plate on Si, therefore traditional catalysts Pd and Pt are the most efficient. Though, both Pd and Pt are refractive metals, and they require annealing above 900C to form silicide. Without forming the silicide, it is not possible to achieve high adhesion of the metal to Si. 900C is not acceptable for metallization step, as it will cause dopant diffusion in the p-n junction, distorting an optimal doping profile after epitaxy. To overcome this, to a traditional Pd plating solution - HCl hydrochloric acid 1-5% Palladium chloride 1-5%, some amount of HF is added. HCl serves as oxidation agent making local islands of SiO2, and HF dissolves them. The small dips on Si surface becomes preferable sites for Pd deposition. Eventually the Si surface gets covered by Pd islands semi-dipped into Si. This process step is fast, 2 to 5 second, and goes at room temperature. Then wafer is retrieved from Pd bath and after short rinse moved in Ni bath: Citric acid monohydrate <1%, Ammonium hydroxide 1-5%, Hydrochloric acid 1-5%, Nickel sulfate 1-5%, Sodium hypophosphite <1%. The bath is kept at 60C for optimal Ni plating. By adding of acetic acid and ammonia, the pH of 60C bath is adjusted to 11.5, and plating proceeds for several minutes. Sample on Fig 6.2.3 show successful deposition. For Ni, the wafer was shallower in the bath, thus one can observe non-plated area, area plated with Pd only, and are plated with Pd-then-Ni.

Next run is planned with a goal to get uniform metal coating across the wafer. Required labware purchased. As gas bubbles are produced by the plating reaction, recipe is adjusted by adding Triton-100 surfactant.

6.2.5 Summary of Significant Findings and Mission Impact

(A) Feedback from UMKC pulsed measurement team received - on Gen2 dies – see chapters 6.1 and 6.3 for details. The feedback has been thoroughly analyzed to improve the DSRD fabrication process. Several process adjustments have been implemented in processing of next Gen2 die lots. Die-to-die excessive variability is noticed. Process recipes and some equipment have been adjusted to achieve better uniformity and repeatability.

(B) Improving side termination of diodes. Upon analysis of etched v-grove shapes, decision made to purchase new labware including advanced wafer dippers. To prevent detrimental non-uniformity due to hydrogen bubbles sticking to wafer surface, several new process recipes have been developed. Next etch run will show whether sufficient uniformity achieved.

(C) Replacement of unreliable metal contact deposition technique (by electron beam sputtering in vacuum chamber). Technical feasibility run on direct electroless plating of the Palladium/Nickel stack was successful. Process recipe developed for next run, plate uniform stack of Pd/Ni/Cu/Sn .

(D) Diode side surface passivation by 2 new methods – stain etch, and SiOF deposition have been tried, and technical feasibility confirmed.

6.2.6 References

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[3] Boff, A., J. Moll, and R. Shen. "A new high-speed effect in solid-state diodes." in 1960 IEEE International Solid-State Circuits Conference. Digest of Technical Papers, vol. 3, pp. 50-51. IEEE, 1960

[4] 6. S.Bellinger, A.Caruso, A.Usenko, “Stacked Diodes for Pulsed Power Applications: New Process Integration Scheme”, presented at 240th Electrochemical Society Meeting, Oct. 10-14, 2021, Orlando, FL.

[5] A.Usenko, J. Eifler, S. Roy, G. Bhattarai, M. Hyde, M. Paquette, A. Caruso, S. Bellinger, L. Voss, R.Allen, “New Paradigm in Fabrication of Semiconductor Opening Switches for Pulsed Power” poster presented at 2021 DEPS Systems Symposium, Oct.25-29, 2021, Washington, D.C.

[6] Alex Usenko, Anthony Caruso, Steven Bellinger “New Paradigm on Making Semiconductor Opening Switches for Pulsed Power” presented at, 23th IEEE Pulsed Power Conference 12-16 December, 2021, Denver, CO

6.3 Characterization of SOS Diode Performance through DOE Augmentation

(Megan Hyde)

6.3.1 Problem Statement, Approach, and Context

Primary Problem: Drift step recovery diodes (DSRDs) are planar diodes that are capable of nanosecond, high frequency (10–10^3 kHz) pulses [1] with applications as opening switches in inductive energy storage (IES) pulse generation circuits. The theory provided by Benda et al is the primary physical explanation for DSRDs, but it does not provide explanations for either the current interruption mechanism or the current loop inductance [3]. This discrepancy within the physical model of the diode reduces the ability to design and produce IES pulse generating circuits. In addition to the incomplete theory on DSRDs, there is no characterization process for assessing diode performances, leaving the entire DSRD lifecycle riddled with systemic uncertainties.

Solution Space: We will develop a methodology for assessing diode performance to provide an empirical solution to the IES pulse generating circuit designer in Section 6.5. Our diode assessment methodology will leverage data analytics coupled with a design of experiments (DOE) to process the parametric information provided by fabrication design (Section 6.2), to align the diode performance with simulation modeling (Section 6.1), and finally to provide an output for an optimized DSRD that meets the specific needs of the designer for the IES pulse generating circuit (Section 6.4).

***Sub-Problem 1*:** We do not yet understand how the diode parameters are tied to the diode performances.

Sub-Problem 2: There is no standardized method for correlating the diode key performance indicators (KPIs) to the IES pulser generator performance.

Sub-Problem 3: The non-linear separable data generated from the DOE is too complex to leverage traditional data analytics.

State-of-the-Art (SOTA): Standard diode measurements include curve tracers for forward and reverse IV, impedance spectroscopy for forward and reverse CV, and function generators or, for example, the Avtech pulser for reverse recovery with high voltage and/or high current when necessary. These measurements are used to generate commonly available datasheets for COTS diodes. These standard diode measurements can then be correlated to pulser performance using traditional data analytics.

Deficiency in the SOTA: The standard diode measurements and datasheets do not include pulser performance necessary to evaluate DSRDs. The datasets generated with doping profile assessment (for example spreading resistance profiling), standard diode measurements and pulser performance are too large and complex to leverage traditional data analytics and will benefit from machine learning techniques.

Solution Proposed: Develop a holistic evaluation network to characterize the KPIs of DSRDs. This network will include a DOE that will be a continuously evolving model as new KPIs are discovered between each of the stages within the network (Sections 6.1 to 6.5) referred to as the "augmented DOE". Machine learning will be used as the primary decision-making tool for augmenting the DOE. Once the network is established, it will be used to outline the optimal parameters for stacks of DSRDs within an IES pulse generator.

Relevance to OSPRES Grant Objective: Bridging the gap between the theoretical and the physical performance of DSRDs enables closing the gap between a low fidelity TRL3 breadboard pulse generation system, and one which is at high fidelity TRL4 prototype level. At the TRL4 level, the DSRD-IES pulse generator system would be sufficient to replace the costly laser-based Si-PCSS HPM generator without compromise to scalability required to support the Naval afloat mission.

Risks, Payoffs, and Challenges:

Challenges: Traditional predictive analytics will be difficult to correlate with the augmented DOE due to the large volume of data. Machine learning is expected to assist with decision making processes for the DOE, but only if the proper KPIs have been established and good data has been used to train the machine learning model.

6.3.2 Tasks and Milestones / Timeline / Status

(A) Milestone – Establish preliminary DOE and SOP for identifying KPIs of DSRDs [*estimated completion by DEC21*].

1. Task – Ascertain current KPIs used to optimize diodes simulated, manufactured, and utilized within the IES pulse generating circuit (from Sections 6.2–6) [JUN–AUG21];
2. Task – Construct preliminary DOE to acquire data on all KPIs based on Task 1 to produce an optimal output for the IES pulse generating circuit (Section 6.5) [AUG–SEP21];
3. Task – Leverage existing Python scripts to process legacy DSRD KPI data [*AUG—SEP21*];

4. Task – Develop new and review existing SOPs for experimental testing apparatuses used to evaluate individual KPIs and measure their performance [*AUG–OCT21*];
5. Task – Identify gaps/deficiencies in legacy KPI data, evaluate existing theoretical relationships to bridge gap and minimize DOE if possible [*SEP–OCT21*];
6. Task – Using SOPs developed in Task 4, acquire experimental data from legacy DSRDs, refine SOP(s) *pro re nata,* and assess repeatability and reproducibility [*SEP–OCT21*];
7. Task – Begin training machine learning model with legacy data to determine statistical correlations and significance of KPIs, and their interdependent relationships [*OCT–DEC21*];

(B) Milestone – Evaluate DSRD performance by the developed SOPs and facilitated by the preliminary DOE [*on hold until Milestone A is completed*].

1. Task – Augment DOE to include previously unidentified yet relevant KPIs based on new findings [*Est. Spring22*];
2. Task – Acquire data on newly manufactured epitaxial DSRDs from Section 6.3 using refined SOPs from Milestone A [*Est. Spring22*];
3. Task – Correlate KPIs to TCAD simulation model, manufactured diode characteristics, and 'M×N' IES pulser's performance to aid in simulation model development, fabrication procedures, and circuit topology development [*Est. Spring22*];

(C) Milestone – SOS diode network evaluation [*on hold until Milestone B is completed*].

1. Task – Refine Python script to incorporate new correlations based on findings from Milestones A&B [*Est. Fall22*];
2. Task – Amend ML training model with data acquired on new DSRDs (as characterized by Sections 6.2-3) to investigate statistical correlation of diode performance [*Est. Summer22*];
3. Task – Work with TCAD simulation team to address discrepancies between the DSRD's performance obtained experimentally, and that achieved within simulations [*Est. Summer22*];
4. Task – Collaborate with DSRD manufacturing team to address discrepancies between the DSRD's characteristics evaluated experimentally, and that desired by manufacturing process [*Est. Summer22*];
5. Task – Investigate relationships between statistical significance of individual diode KPIs to the peak performance of the IES pulser with the pulse generator team. [*Est. Summer22*];
6. Task – Incorporate findings from Tasks 1–5 into ML model, pinpoint KPI correlations of interest, and provide recommendations to IES sub-teams accordingly [*Est. Summer22*];

(D) Milestone – SOS diode network evaluation [*on hold until Milestone C is completed*].

1. Task – Augment DOE network to streamline diode evaluation and identify checkpoints/gaps within simulation, manufacturing, and circuit development process to ensure optimal diodes are selected and utilized to produced robust high-fidelity IES pulse generator prototypes [*Est. Fall22*];

6.3.3 Progress Made Since Last Report

(A.1) A new test tracking document has been implemented to track the tests performed on each diode to help visualize which tests have been completed, and which tests need to be repeated (Figure 6.3.1).

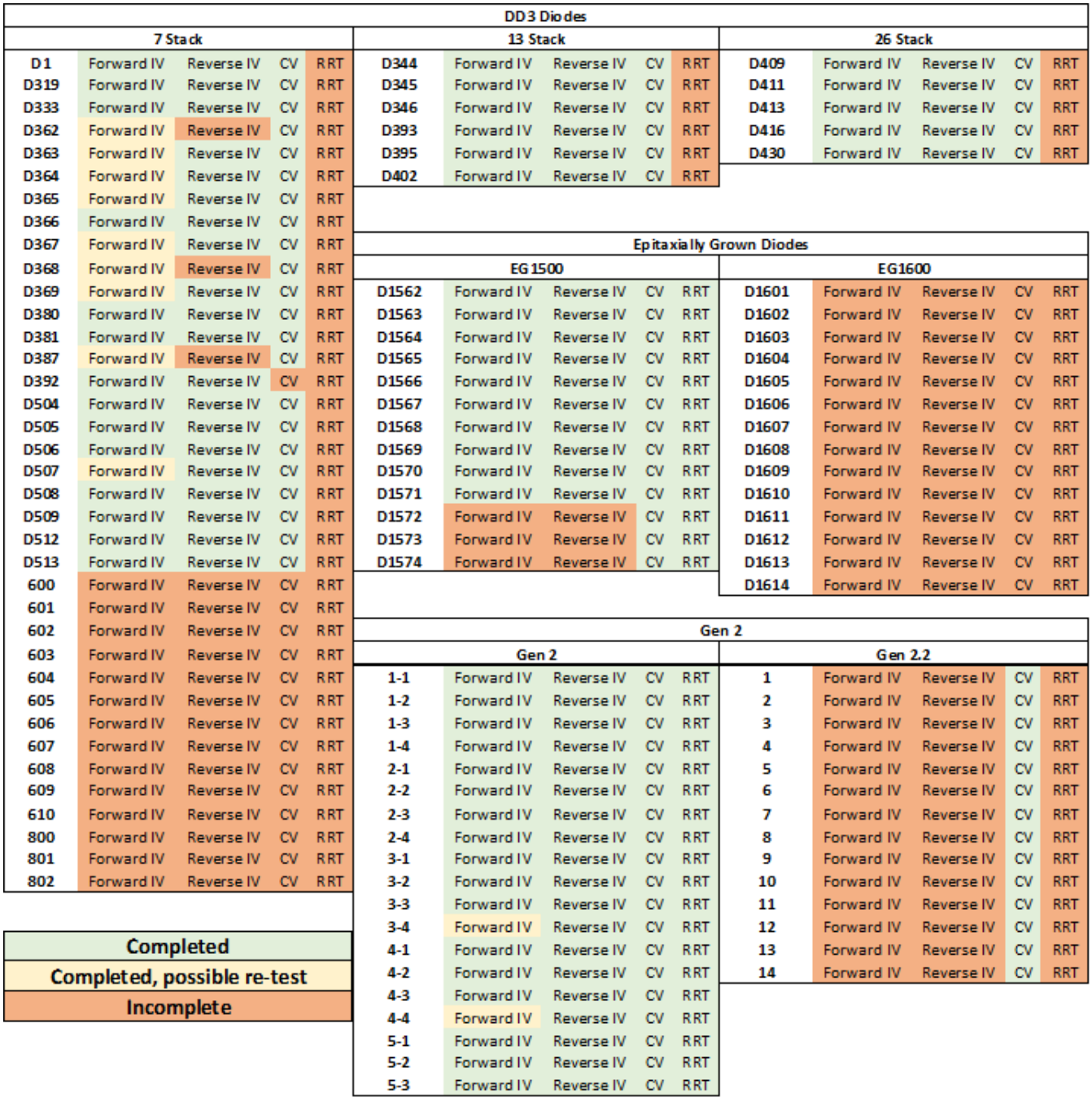
(A.4) Development of a new SOP for reverse recovery time (RRT) measurements is currently under review. Several epitaxially grown 1500 (EG1500) and 19 Gen 2 series DSRDs have been tested under a variety of test conditions (refer to Figure 6.3.2). Resolving the ideal testing conditions for RRT tests will enable us to calculate the minority carrier lifetime. The present challenge is verifying the calculated time is the carrier lifetime, rather than the transient lifetime.

Modification of the IV and CV measurement SOPs were required for testing the Gen 2 DSRDs since they are a single stack, where voltages over 1 V can damage the diode.

(A.6) Of the DD3 (DD3 refers to a naming convention for deep diffusion diodes) DSRDs, 34 out of 48 have completed the IV (forward and reverse) and CV testing. RRT testing is still in the beginning stages as the ideal testing conditions for extracting minority carrier lifetimes has not yet been established. The remaining DSRDs to be tested are on hold until the RRT SOP has been finalized as well as the repeatability and reproducibility studies have been completed. Refer to Figure 6.3.3 for the comparisons between each type of DSRD and their completion status for each test.

All Gen2 DSRDs have completed their IV (forward and reverse) testing as well as the CV testing. The zero bias junction capacitance measurements from these diodes showed the greatest variability between each type, so the Gen2 diodes were selected to conduct the first round of repeatability and reproducibility studies. All Gen2 DSRDs have since been tested in the exact specifications according to the SOP an additional 3 times for IV and CV testing. Results of the study will be published the next section.

Every EG1500 DSRD has been tested in IV (forward and reverse), CV, and RRT. Alongside 19 of the Gen2 DSRDs, the EG1500s are a part of the method development for the RRT test. None of the EG1600 DSRDs have been tested yet. Refer to Table 6.3.1 for a summary of the testing status of each category of DSRD.



DD3 Diodes															
7 Stack					13 Stack					26 Stack				
D1	Forward IV	Reverse IV	CV	RRT	D344	Forward IV	Reverse IV	CV	RRT	D409	Forward IV	Reverse IV	CV	RRT
D319	Forward IV	Reverse IV	CV	RRT	D345	Forward IV	Reverse IV	CV	RRT	D411	Forward IV	Reverse IV	CV	RRT
D333	Forward IV	Reverse IV	CV	RRT	D346	Forward IV	Reverse IV	CV	RRT	D413	Forward IV	Reverse IV	CV	RRT
D362	Forward IV	Reverse IV	CV	RRT	D393	Forward IV	Reverse IV	CV	RRT	D416	Forward IV	Reverse IV	CV	RRT
D363	Forward IV	Reverse IV	CV	RRT	D395	Forward IV	Reverse IV	CV	RRT	D430	Forward IV	Reverse IV	CV	RRT
D364	Forward IV	Reverse IV	CV	RRT	D402	Forward IV	Reverse IV	CV	RRT					
D365	Forward IV	Reverse IV	CV	RRT										
D366	Forward IV	Reverse IV	CV	RRT										
D367	Forward IV	Reverse IV	CV	RRT	Epitaxially Grown Diodes									
D368	Forward IV	Reverse IV	CV	RRT	EG1500					EG1600				
D369	Forward IV	Reverse IV	CV	RRT	D1562	Forward IV	Reverse IV	CV	RRT	D1601	Forward IV	Reverse IV	CV	RRT
D380	Forward IV	Reverse IV	CV	RRT	D1563	Forward IV	Reverse IV	CV	RRT	D1602	Forward IV	Reverse IV	CV	RRT
D381	Forward IV	Reverse IV	CV	RRT	D1564	Forward IV	Reverse IV	CV	RRT	D1603	Forward IV	Reverse IV	CV	RRT
D387	Forward IV	Reverse IV	CV	RRT	D1565	Forward IV	Reverse IV	CV	RRT	D1604	Forward IV	Reverse IV	CV	RRT
D392	Forward IV	Reverse IV	CV	RRT	D1566	Forward IV	Reverse IV	CV	RRT	D1605	Forward IV	Reverse IV	CV	RRT
D504	Forward IV	Reverse IV	CV	RRT	D1567	Forward IV	Reverse IV	CV	RRT	D1606	Forward IV	Reverse IV	CV	RRT
D505	Forward IV	Reverse IV	CV	RRT	D1568	Forward IV	Reverse IV	CV	RRT	D1607	Forward IV	Reverse IV	CV	RRT
D506	Forward IV	Reverse IV	CV	RRT	D1569	Forward IV	Reverse IV	CV	RRT	D1608	Forward IV	Reverse IV	CV	RRT
D507	Forward IV	Reverse IV	CV	RRT	D1570	Forward IV	Reverse IV	CV	RRT	D1609	Forward IV	Reverse IV	CV	RRT
D508	Forward IV	Reverse IV	CV	RRT	D1571	Forward IV	Reverse IV	CV	RRT	D1610	Forward IV	Reverse IV	CV	RRT
D509	Forward IV	Reverse IV	CV	RRT	D1572	Forward IV	Reverse IV	CV	RRT	D1611	Forward IV	Reverse IV	CV	RRT
D512	Forward IV	Reverse IV	CV	RRT	D1573	Forward IV	Reverse IV	CV	RRT	D1612	Forward IV	Reverse IV	CV	RRT
D513	Forward IV	Reverse IV	CV	RRT	D1574	Forward IV	Reverse IV	CV	RRT	D1613	Forward IV	Reverse IV	CV	RRT
600	Forward IV	Reverse IV	CV	RRT						D1614	Forward IV	Reverse IV	CV	RRT
601	Forward IV	Reverse IV	CV	RRT										
602	Forward IV	Reverse IV	CV	RRT	Gen 2									
603	Forward IV	Reverse IV	CV	RRT	Gen 2					Gen 2.2				
604	Forward IV	Reverse IV	CV	RRT	1-1	Forward IV	Reverse IV	CV	RRT	1	Forward IV	Reverse IV	CV	RRT
605	Forward IV	Reverse IV	CV	RRT	1-2	Forward IV	Reverse IV	CV	RRT	2	Forward IV	Reverse IV	CV	RRT
606	Forward IV	Reverse IV	CV	RRT	1-3	Forward IV	Reverse IV	CV	RRT	3	Forward IV	Reverse IV	CV	RRT
607	Forward IV	Reverse IV	CV	RRT	1-4	Forward IV	Reverse IV	CV	RRT	4	Forward IV	Reverse IV	CV	RRT
608	Forward IV	Reverse IV	CV	RRT	2-1	Forward IV	Reverse IV	CV	RRT	5	Forward IV	Reverse IV	CV	RRT
609	Forward IV	Reverse IV	CV	RRT	2-2	Forward IV	Reverse IV	CV	RRT	6	Forward IV	Reverse IV	CV	RRT
610	Forward IV	Reverse IV	CV	RRT	2-3	Forward IV	Reverse IV	CV	RRT	7	Forward IV	Reverse IV	CV	RRT
800	Forward IV	Reverse IV	CV	RRT	2-4	Forward IV	Reverse IV	CV	RRT	8	Forward IV	Reverse IV	CV	RRT
801	Forward IV	Reverse IV	CV	RRT	3-1	Forward IV	Reverse IV	CV	RRT	9	Forward IV	Reverse IV	CV	RRT
802	Forward IV	Reverse IV	CV	RRT	3-2	Forward IV	Reverse IV	CV	RRT	10	Forward IV	Reverse IV	CV	RRT
					3-3	Forward IV	Reverse IV	CV	RRT	11	Forward IV	Reverse IV	CV	RRT
					3-4	Forward IV	Reverse IV	CV	RRT	12	Forward IV	Reverse IV	CV	RRT
					4-1	Forward IV	Reverse IV	CV	RRT	13	Forward IV	Reverse IV	CV	RRT
					4-2	Forward IV	Reverse IV	CV	RRT	14	Forward IV	Reverse IV	CV	RRT
					4-3	Forward IV	Reverse IV	CV	RRT					
					4-4	Forward IV	Reverse IV	CV	RRT					
					5-1	Forward IV	Reverse IV	CV	RRT					
					5-2	Forward IV	Reverse IV	CV	RRT					
					5-3	Forward IV	Reverse IV	CV	RRT					

Completed
Completed, possible re-test
Incomplete

Figure 6.3.1. Shown is the summary of each test performed on each diode. Each test is color coded to assist in identifying missing or incomplete data. Note that "DD3" is a naming convention for deep diffusion DSRDs. The tests included in the table are the forward and reverse IV, CV, and the RRT.

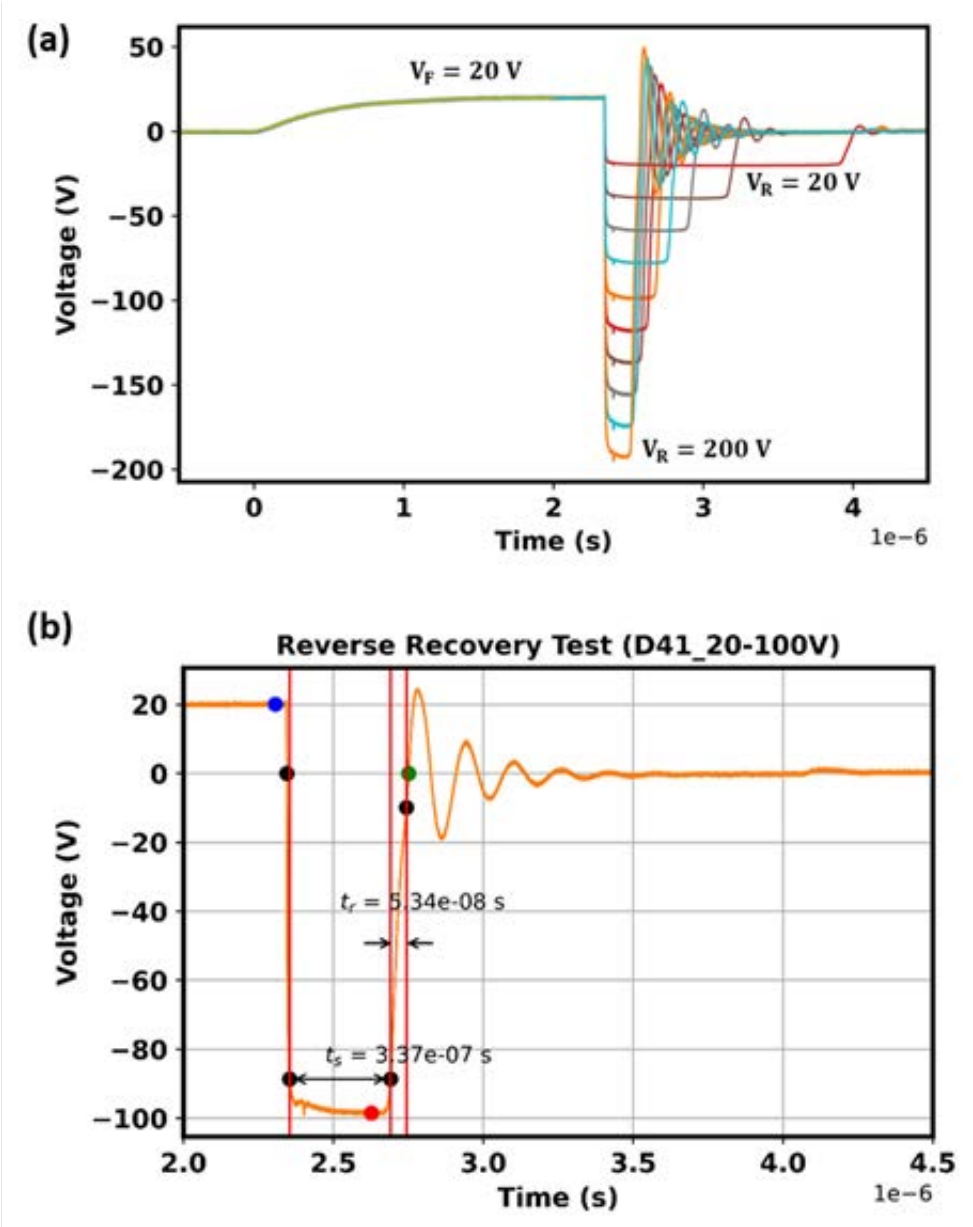


Figure 6.3.2. (a) A typical reverse recovery test data of a single-stack Gen 2 DSRD with forward voltage of 20 V and reverse voltage from 20 V to 200 V. Both forward and reverse voltage pulses were applied for 2 µs. (b) Reverse recovery test of Diode D4-1 showing the charge storage time t_s and transition time t_r.

6.3.4 Technical Results

(A.6) The zero bias junction capacitance measurements were performed and qualitatively compared against each diode type (e.g., DD3, Gen2, EG1500). A qualitative comparison between each diode (refer to Figure 6.3.3) showed that the Gen 2 diodes had the greatest variability, so became the focus of a repeatability study.

Each Gen 2 diode was tested a total of three times for both CV and IV (forward and reverse) tests. Each test was performed by the same operator and under the same testing conditions as outline by their respective SOPs.

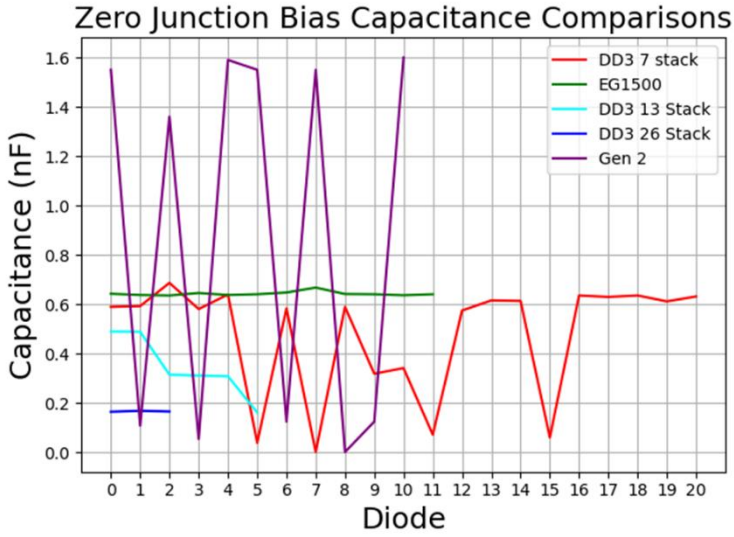
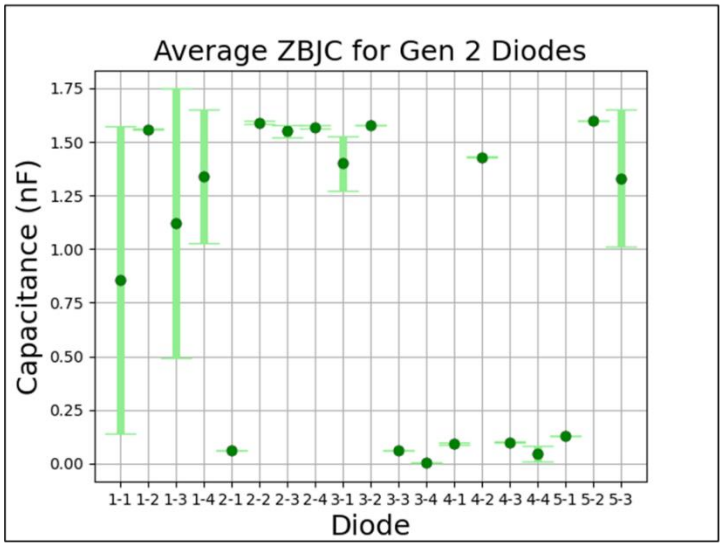


Figure 6.3.3. Zero junction bias capacitance plot that enables a qualitative comparison of the measurements against each type of diode. It was decided to begin a repeatability study on the Gen 2 diodes due to the variability of measurements found from this plot.

Figure 6.3.4 highlights the findings of the repeatability study found for the CV test. So far, there does not appear to be a correlation between the metallicity (color of diode) to overall performance. Other sources of variation are currently under investigation.

In addition to the CV test, a repeatability study was performed on the Gen 2 diodes for the IV test. Figure 6.3.5 shows the results of that study. The measurement plotted is the voltage of each diode at 10mA. As can be seen from the figure, two diodes did not provide any useable data (corresponds to the “Completed, possible re-test” label used in Table 6.3.1). Since the diodes never achieved breakdown voltages, the results of the reverse IV test showed little variation in the testing, so alternative testing conditions are under consideration.

A Levene’s Variability test was performed on the results for both the forward IV and CV testing. The p-value validates the consistency of the testing performed ($p = 0.8548$ for CV and $p = 0.8416$ for IV).



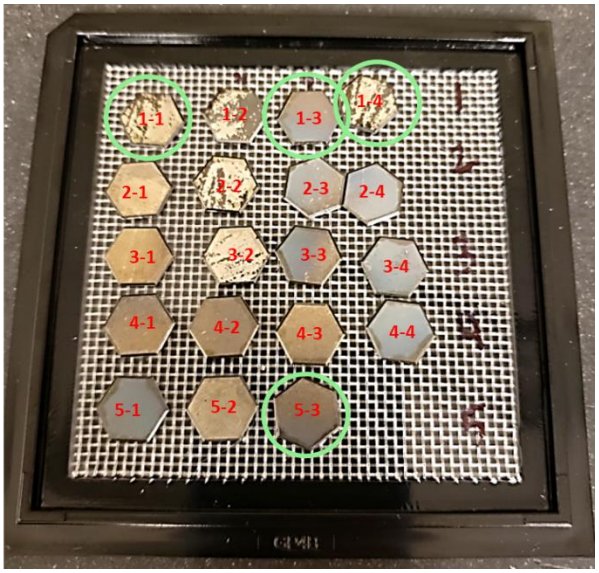
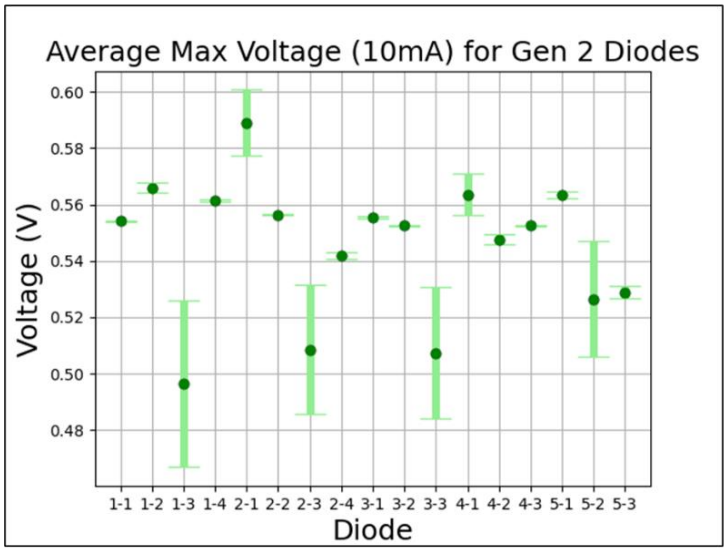


Figure 6.3.4. Results of the repeatability study for the zero junction bias capacitance measurements. On the left are the measurement averages with their respective standard deviations. On the right is an image of the Gen 2 diodes. Each diode has been labeled with its name in red, and each diode circled in green represents the diodes with the greatest variability from this study.



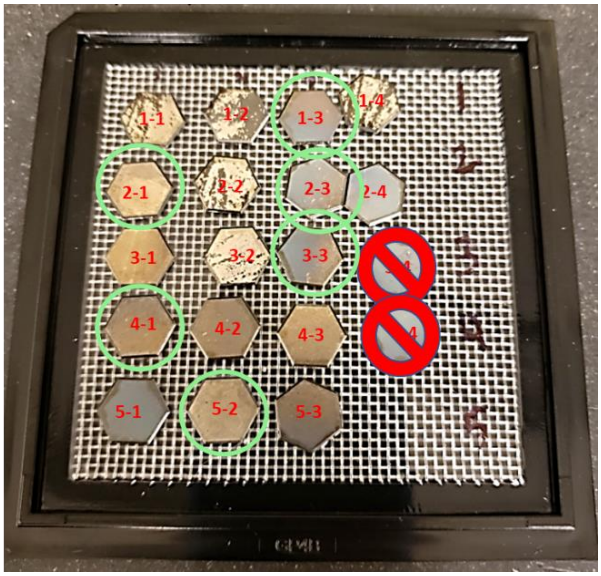


Figure 6.3.5. Results of the repeatability study for the forward voltage at 10mA measurements. On the left are the measurement averages with their respective standard deviations. On the right is an image of the Gen 2 diodes. Each diode has been labeled with its name in red. Circled in green represents the diodes with the greatest variability from this study. The two diodes that are crossed out never produced any useable data. These two diodes correspond to the “Complete, possible re-test” label found in Table 6.3.1.

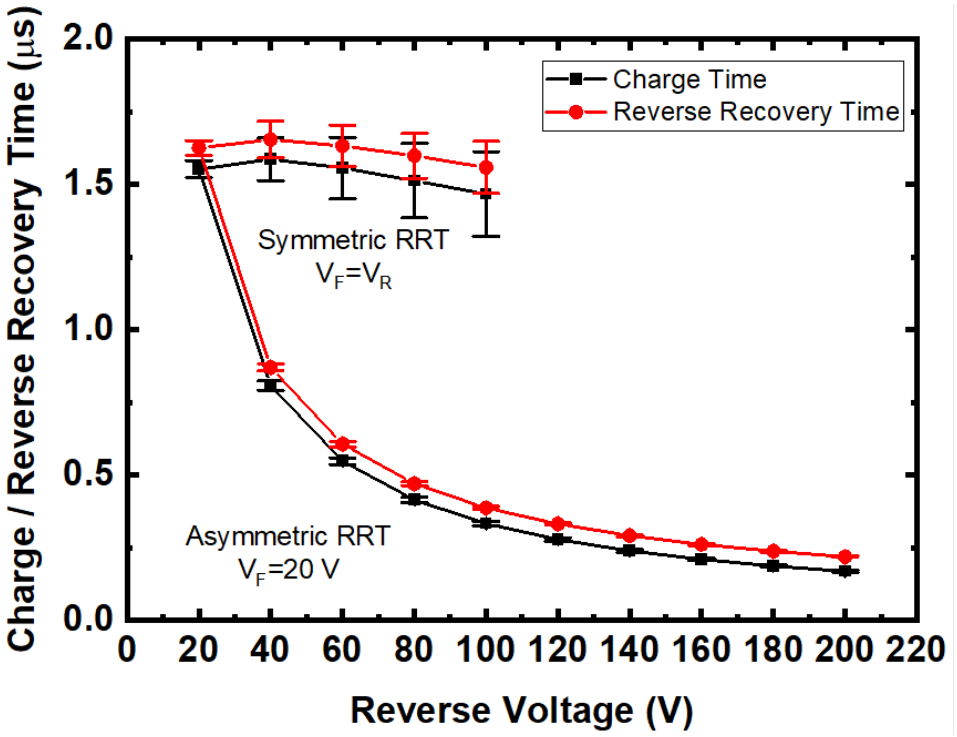


Figure 6.3.6. Charge storage and Reverse recovery time of single stack Gen-2 DSRD diodes as a function of reverse pulse voltage. The symmetric RRT is for test conditions where forward and reverse pulses were of equal amplitude, while asymmetric RRT is for increasing reverse voltage for 20 V forward pulse amplitude. Reverse recovery time is the sum of the charge storage time and the transition time (see figure 6.3.2 (b)).

Development of a standardized procedure for RRT measurements is still under investigation since the ideal testing conditions for calculating minority carrier lifetimes are still in progress. However, the measurement results found thus far from the Gen2 and EG1500 DSRDs have shown greater consistency in testing results than the DC measurements (refer to Figure 6.3.6).

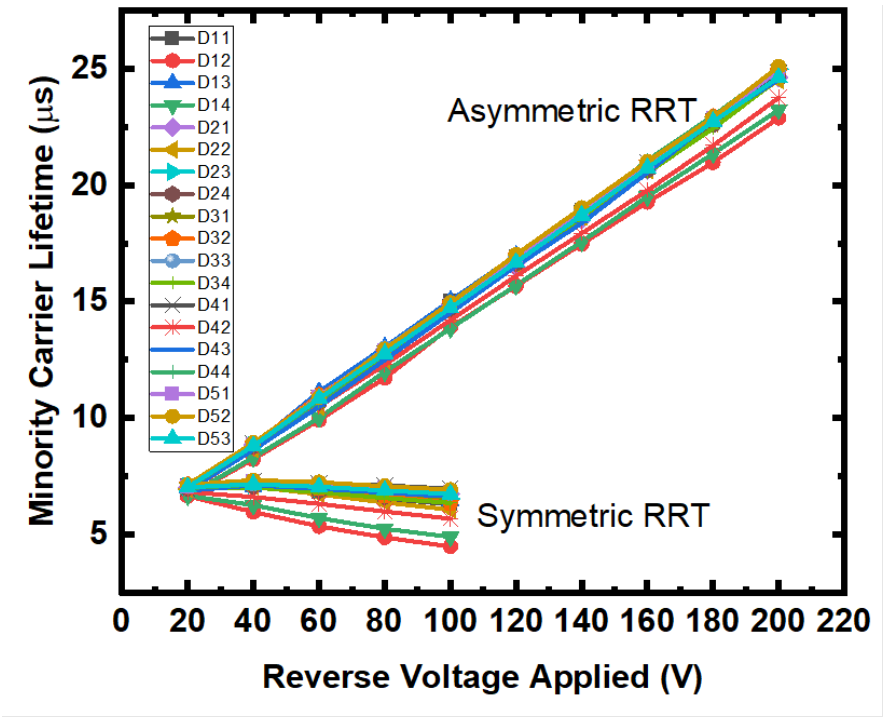


Figure 6.3.7. Minority carrier lifetime obtained for single-stack Gen-2 diodes as a function of applied reverse voltage.

The minority carrier lifetime in the DSRDs were calculated using the Kingstone [5] equation given by:

$$\frac{1}{1 + I_R/I_F} = erf\left(\frac{t_s}{\tau_{eff}}\right)^{1/2}$$

where I_R, I_F, and τ_{eff} represent the reverse current, forward current, and the minority carrier lifetime, respectively. Since the carrier lifetime is expected to be independent of the reverse voltage applied, the observed linear relationship between them may indicate that the calculated parameter is not actually the carrier lifetime as the depending on the diode thickness, the calculated time can also represent the carrier transit time [5].

6.3.5 Summary of Significant Findings and Mission Impact

(A.1) We have identified several KPIs pertaining to the diode characterization procedures. These KPIs have been stored within a matrix template that will also serve as a logistical catalog of legacy diodes and testing procedures.

(A.4) Several diode characterization procedures have been updated. These procedures include both the IV and CV measurements. Both methods now have newly updated SOPs that track and catalog any changes made to the processes. Refer to Table 6.3.1 for a summary of the testing performed on each diode. Several testing issues have presented

themselves during this process. One issue is the large variability between each IV measurement. Several DSRDs had to be measured multiple times to get data that did not appear to be noise. The IV measurement procedure is still in progress since the current equipment is only capable of achieving –200 V, which is far too low for measuring breakdown voltages.

A standardized testing procedure for RRT measurements is still in progress. However, several Gen2 and all the EG1500 diodes have been tested (reference Table 6.3.1). Development of this test will lead to an increased understanding in minority carrier lifetime measurements and how they relate to the forward pumping time for pulsing.

(A.6) The results of the repeatability study showed that there is variation within the IV and CV measurements, however, the reverse recovery test showed the least variability among the tests performed. Several factors can be attributed to this variation, including the diode being damaged.

The Gen2 and the EG1500 diodes that have completed RRT testing have shown lower deviations than the other DC measurements (refer to Figure 6.3.6). A repeatability study, similar to the IV and CV tests, will need to be performed to confirm this result.

6.3.6 References

[1] Benda, H., & Spenke, E. (1967). Reverse recovery processes in silicon power rectifiers. Proceedings of the IEEE, 55(8), 1331-1354.

[2] Kozlov, V. A., Smirnova, I. A., Moryakova, S. A., & Kardo-Sysoev, A. F. (2002, June). New generation of drift step recovery diodes (DSRD) for subnanosecond switching and high repetition rate operation. In Conference Record of the Twenty-Fifth International Power Modulator Symposium, 2002 and 2002 High-Voltage Workshop. (pp. 441-444). IEEE.

[3] Sharabani, Y., Rosenwaks, Y., & Eger, D. (2015). Mechanism of Fast Current Interruption in p− π− n Diodes for Nanosecond Opening Switches in High-Voltage-Pulse Applications. Physical Review Applied, 4(1), 014015.

[4] Foll, H. (n.d.). *Reverse Recovery Time of Junction Diodes*. Retrieved from Semiconductors:https://www.tf.unikiel.de/matwis/amat/semi_en/kap_8/advanced/t8_1_1.html

6.4 DSRD-Based Pulsed Power Source Systematic Topological Optimization

(Roy Allen)

6.4.1 Problem Statement, Approach, and Context

Primary Problem: Drift step recovery diodes used in inductive energy storage (IES) and release pulse generators, when able to achieve ones of gigawatts in ones of nanoseconds, are large, heavy, and require liquid-based cooling systems to dissipate the excess heat they generate during operation; therefore, rendering them impracticable for Navy afloat missions.

Solution Space: Systematically develop a modular architecture of a pulser circuit using DSRDs by determining the optimal permutation of series and parallel combinations of the base pulser unit, and its component parameters, in order to maximize the peak voltage,

peak power, and volumetric power density without sacrificing the desired nanosecond risetime of the pulses generated nor requiring liquid-based cooling.

***Sub-Problem*:** DSRDs are not domestically available COTs available components. The small-batch quantities that are manufactured have statistically significant variations in their performance parameters. In addition, SPICE models of these diodes are not accurate and do not account for their sample-to-sample parameter variability. The above-mentioned reasons may lead to an inaccurate simulation model of the pulser that may result in a difference between the simulation and experimental results.

State-of-the-Art (SOTA): DSRD-based pulsers (equivalent in size to the pulse generators developed for this effort, i.e., ~0.01-m^3, ~2-kg) can achieve 6-kV, 200-ps risetime, and <500 ps FWHM across a 50 Ω load.

Deficiency in the SOTA: DSRD-based air-cooled versions are limited to PRFs of < 15 kHz. Additionally, current studies on SOS-IES pulse generators attempt to present only the best-case circuit configurations meaning a comprehensive study on optimizing the number and ratio of parallel branches and series-connected stages aiming to achieve maximum gain and efficiency (reducing thermal load) is missing in the SOTA.

Solution Proposed: Systematically determine topological SOS-IES circuit configurations and the necessary components therein that maximize voltage gain and efficiency and minimize the rise-time achieved by the pulser.

Relevance to OSPRES Grant Objective: IES pulse generators using DSRDs can remove the need for photo-triggered switches and their laser sub-systems. They are ideal for triggering sub-nanosecond rise-time sharpeners (SAS, D-NLTL, etc.), reducing overall cost, volume, and weight.

Risks, Payoffs, and Challenges:

Risks: Domestically manufactured (U.S.-based) DSRDs which possess sub-optimal doping profiles may lead to sub-optimal pulse generators with sub-optimal performance. The data gathered from these sub-optimal circuits would then be used to train the genetic/machine learning algorithms developed and the redesign of future topologies constructed; ultimately leading to spurious conclusions regarding ideal topological circuit configurations with ‘N’ number of series-connected stages, each containing ‘M’ parallel branches.

Payoffs: Leveraging collaborative partnerships with U.S.-based manufacturers of DSRDs, the ability to refine and control the performance characteristics of the diodes themselves, along with the ability to simulate and manufacture the DSRD pulsers in-house, enables a holistic soup-to-nuts capability to optimize, produce, and evaluate these nanosecond pulse generators.

Challenges: Determining the superlative ratio of design/development (through numerical analysis) to the effort put towards experimental testing/evaluation of the DSRD pulser is challenging due to the novelty of the approach. The complexity of the theoretical model is extreme given the M×N number of DSRD base unit stages within the pulse forming network along with inaccurate DSRD spice model and large sample-to-sample variability.

6.4.2 Tasks and Milestones / Timeline / Status

(A) Milestone – Construct/demonstrate a DSRD-based 2×2 IES pulse generator prototype capable of producing ≥4 kV peak voltage, ≤1 ns risetime, ≤5 ns FWHM, ≥320 kW peak-power, ≥1 kHz PRF, ≥100 shots-per-burst, ≥5 number of bursts [***Completed JUL21***].

(B) Milestone – Construct/demonstrate a DSRD-based 1×1 IES pulse generator prototype capable of testing individual and combinations of diode stacks to acquire performance data [***Completed AUG21***].

(C) Milestone – Construct/demonstrate a DSRD-based 4×2 IES pulse generator prototype capable of producing ≥12 kV peak voltage, ≤1 ns risetime, ≤5 ns FWHM, ≥3 MW peak-power, ≥100 kHz PRF, ≥1,000 shots-per-burst, ≥500 number of bursts [*Ongoing, estimated completion by OCT21*].

1. Task – Develop revised layout in Altium and order PCB and components. [***Completed – SEP21***];
2. Task – Populated pulse generator and begin testing & evaluation phase [***Completed – NOV21***];

(D) Milestone – Develop waveform inverter which, when combined with the pulser from Milestone C, enables a balanced differential waveform output with > 90 % inverted signal fidelity. [***Completed – DEC21***].

(E) Milestone – Construct/demonstrate a M×N pulse generator prototype capable of producing ≥20 kV peak voltage, ≤1 ns risetime, ≤2 ns FWHM, ≥8 MW peak-power, ≥100 kHz PRF, and $\geq 2\sigma_{Vpeak}$, which operates in continuous-burst mode as a viable candidate for OSPRES Contract source alternative [*on hold until Milestone C & D are completed*].

6.4.3 Progress Made Since Last Report

(C) The 4×2 DSRD-based pulse generator has been populated and is currently being tested and evaluated.

6.4.4 Technical Results

(C) The 4×2 DSRD-based pulse generator has been populated and is undergoing testing and analysis. Preliminary results show the gate driver and DC booster circuit is fully operational and able to synchronously trigger the four MOSFETs in parallel used for the first stage's power combining. The majority of the work performed this month has focused on utilizing the systematic experimental evaluation developed for testing the 1×1 and 2×2 variants where multiple diode stacks are used in various combinations to evaluate the peak voltages achieved as a function of trigger length and bias voltages. Next month's report will provide an analysis of the results acquired once testing is completed.

(D) Working with ASR Corporation as a joint research effort (funded through ONR Contract No. N68335-19-C-0255), a 50-kV rated capacitive inverter has been prototyped and provided to MIDE for the OSPRES Grant Effort. It will be used to invert the DSRD pulse generator's output from a positive, monopolar, output signal, to a negative (inverted)

monopolar impulse. Once the time alignment of the trigger signal inputs for each the positive and negative signals are demonstrated, a second 4×2 pulse generator will be assembled to then generate a combined balanced differential output signal at 2× the peak voltage (4× in peak power) in comparison to a standalone monopolar impulse. Summary of Significant Findings and Mission Impact

6.4.5 Summary of Significant Findings and Mission Impact

(A) Successful construction and operation of a 2×2 DSRD-based IES pulse generator prototype has been completed which meets or exceeds the milestone's required key performance metrics. Shown in Table 6.4.1 are the previous and current pulse generator's performance specifications in comparison to a similar 2×2 pulser developed by Kesar et al. [1] using DSRDs, and to that of a commercial off-the-shelf (COTS) DSRD pulser of similar space and weight developed by Megaimpulse (i.e., PPM-0731) which also uses DSRDs with silicon avalanche shapers (SAS) [2]. Although the Megaimpulse pulser utilizes a SAS with a <500 ps risetime (a threshold we do not intend to go below due to Commerce Controlled List limitations), it is interesting to compare the results of linear voltage gain and peak power of this system, to that of one that utilizes a SAS. The current permutation of the 2×2 SOS-IES pulser developed by MIDE under the ONR OSPRES Grant is able to achieve a higher peak voltage and shorter risetime than DSRD-based pulsers reported in the literature of comparable space and weight as well as those commercially available. The ability to generate a linear voltage gain of 40.8 to produce over a Megawatt of peak power into a 50 Ω load while achieving a peak voltage output standard deviation of 2σ when operating at a PRF of at least 100 kHz, brings this technology to the forefront of viable options to potentially support the Naval afloat mission.

Table 6.4.1. Comparison of DSRD-based IES Pulse Generator Performance.

KPM	Units	MIDE - V1 Previous	MIDE - V2 Current	Kesar *et al.* SOTA	MI-PPM0731 COTS
V_{supply}	V	225	180	300	160
T_{ON}	ns	100	340	?	200
V_{peak}	kV	5.59	**7.35**	5	6.3
Gain	V/V	24.8	**40.8**	16.7	39.4
$\tau_{rise,20\text{-}90\%}$	ns	1.2	1.142	1.96	0.12
dV/dτ	kV/ns	4.66	6.44	2.55	**52.50**
FWHM	ns	2	5.48	2.27	0.35
PW	ns	5	7	3.5	2.5
Z_{LOAD}	Ω	50	50	50	50
P_{peak}	MW	0.625	**1.080**	0.500	0.794
E_{pp}	mJ	0.125	0.154	0.143	0.318
PRF_{max}	kHz	100	100	100	15
Burst	shots	100	100	*N/A*	100
	%	100	100	*N/A*	100
SD_{Vpeak}	σ	> 2	**> 2**	*N/A*	*N/A*
	%	96.5	**97.8**	*N/A*	*N/A*

(B) Discrepancies exist in the obtained data for different series combinations and different samples of 7-stack DSRDs which may be attributed to the inconsistencies in their manufacturing process. Future works in the coming months include carrying out further testing on the 1×1 DSRD-based pulse generator (base-unit) circuit using more combinations of series-connected as well as parallel-connected DSRD stacks.

6.4.6 References

[1] https://www.onsemi.com/pdf/datasheet/nvh4l020n120sc1-d.pdf

[2] https://cms.wolfspeed.com/app/uploads/2020/12/C2M0045170P.pdf

6.5 All-Solid-State Sub-ns MW Pulse Generators with Semiconductor Sharpeners

(Gyanendra Bhattarai)

6.5.1 Problem Statement, Approach, and Context

***Primary Problem*:** Broadband high-power microwave (HPM) systems need sub-nanosecond tens-of-MW pulses. Hydrogen spark gaps (HSG), traditionally used for such purposes, are severely limited by their low pulse repetition frequency (PRF ~1 kHz) and

poor device lifetime (shot life ~1000 pulses), ill-suited to achieve the SWaP metrics necessary for HPM pulse generators for the Navy afloat mission. Competitive solid-state solutions, such as inductive energy storage (IES) systems, utilizing a series stack of fast-opening diodes (drift-step recovery diodes (DSRD) and semiconductor opening switches (SOS)), have not been shown to break nanosecond barriers.

***Solution Space*:** Use viable pulse shaping/compression technologies based on semiconductor closing switches (e.g., delayed breakdown diodes (DBD), and fast ionization dynistors (FID)) to increase the peak power and shorten the rise time of the pulses produced by the DSRD-based pulse generator. Pulse sharpening/compression reduces the otherwise additional complexity of increased M×N stages within the pulser topology; a desired result towards achieving optimal SWaP metrics of the pulse generation system without sacrificing PRF, shot lifetime, and thermal management requirements. (*Please refer to the June 2021 MSR for full problem and solution space description).*

***Sub-Problem 1*:** Achieving an order of magnitude increase in peak power (1-to-10 MW) through compression/sharpening methods requires series and parallel stacks of semiconductor closing switches (SCS), ultimately resulting in increased pulse risetime. Determining the optimal combination of diode stacks to decrease pulse risetime and increase output power requires additional SPICE circuit simulations. However, device models for SCS are not commercially available and thus require maturing SCS device models based on experimental results and physics-based simulations, such as using packages such as T-CAD, which can be time consuming.

***Sub-Problem 2 (Fundamental Physics)*:** Sub-nanosecond high-power pulse sharpening using semiconductor devices is based on ultrafast delayed avalanche breakdown under steeply increasing reverse voltage applied, thereby initiating an impact ionization front. However, the phenomenon behind the origin of free carriers that trigger the impact ionization at higher-than-breakdown fields is not completely known. Further, it is not clear whether the switching (generation of electron–hole plasma) is uniform across the device area or is localized (filamentary). Such different mechanisms are believed to be dependent on device geometry and doping concentration, and are detrimental to the switching speed. A University of New Mexico study [1] has concluded that the operation of a silicon avalanche shaper (SAS) is inconsistent with the theory described by Russian scientists. More understanding of device operation from a fundamental physics perspective is necessary to enhance their performances.

***State-of-the-Art (SOTA)*:** Prototype sub-nanosecond solid-state pulsers based on semiconductor opening switches (SOS) and semiconductor sharpeners are shown to produce peak voltages (~500 kV), and peak power outputs (~5 GW). Solid-state power supplies providing peak power up to 800 MW are available to purchase from FID Technologies, Germany. *Please refer to Table 4.7.1 of the June MSR for list of devices and their performance metrics.*

***Deficiency in the SOTA*:** Prototype ~5 GW power supplies, such as SOS based S-500 system with semiconductor sharpeners, are large (>1 m^3). Commercially available moderate-power (~1 GW) all-solid-state pulsers utilizing semiconductor sharpeners have

long purchase lead time (~4 months). Their PRF capability is limited to ~1 kHz due to physical constraints in thermal management.

***Solution Proposed*:** Downselect viable pulse compression/shaping technologies which meet or exceed the performance parameters set forth in Section 6.3's Milestones A-D towards producing an all-solid-state, tens-of-megawatts, sub-nanosecond pulse generator with semiconductor sharpener without sacrificing PRF, shot lifetime, and thermal management requirements.

***Relevance to OSPRES Grant Objective*:** The alternative all-solid-state technologies discussed could individually, or in combination, provide the means to produce order(s) of magnitude greater peak power, without severe limitation to PRF, as SWaP-centric means to increase the capability and extent of protecting naval assets.

Risks, Payoffs, and Challenges:

***Risks*:** Semiconductor closing switches, such as DBD and FID are not available to purchase within the United States. Procuring devices from abroad could lead to significant delay in experiments and development of device fabrication technology. Undergoing time-intensive and complex simulations to then down-select one technology based on peak power output alone presents risk to other secondary or tertiary performance metrics such as PRF and pulse energy, which risks developing ill-suited technologies to support the float mission. Additionally, as new technology emerges via research, scope creep to numerically and experimentally evaluate new technologies may delay transitioning these technologies into viable systems.

***Payoffs*:** The SWaP tradeoff of generating a non-laser-based system with any number of these systems can yield a higher fidelity pulsed-power waveform output. Determining which technology is viable and feasible in terms of the key performance metrics should yield a more ultracompact form factor pulse generator with order(s) of magnitude greater power density without compromise to overall size and weight to the system.

***Challenges*:** Determining the true performance metrics of interest based on these highly different devices is challenging. Without a more robust and deep understanding of their operation, and how to utilize them within a pulse generator topology, in a swappable configuration or otherwise, requires additional time and consideration. Managing the tradeoff between the academic understanding of the technologies of interest presented in the foregoing table, and the transition to prototype effort/mentality, will require both a delicate balance and leveraging the pulsed-power team's combined effort.

6.5.2 Tasks and Milestones / Timeline / Status

(A) Milestone – Downselect viable pulse compression/shaping technology to be used in addition to currently utilized DSRD, which increases at least one of the key performance metrics by an order of magnitude without compromise to the overall volume of the system [*AUG21*].

1. Task – Finalize literature study of different technologies and topologies of SCS based pulse generators and compare SWaP tradeoff evaluation to PCSS- and DSRD/SOS-based pulse generators [*JUN–JUL21* / *Ongoing*].

2. Task – Determine commercially available technologies that could be used as pulse shaper/sharpening devices to improve pulse generator performance, and select appropriate devices for further experimental verification of their performance metrics [*JUN–AUG21* / *behind schedule*].

(B) Milestone – Model and experimentally verify the performance of the downselected technology as an additional component to the DSRDs utilized within a SOS-IES pulse generator. [*NOV21*].

1. Task – Develop T-CAD device model for the selected devices (DBD/DLD) based on available device information from the literature and perform device simulations for their performance under nanosecond input pulse conditions. *[In progress]*;
2. Task – Develop SPICE device model for the selected device based on T-CAD simulation. [*SEP–OCT21*];
3. Task – Design experimental circuit with one selected diode or dynistor and obtain theoretical performance metrics using standard electronic simulation tools such as LT-Spice using the device model developed in task 2. [*SEP–NOV21*];
4. Task – Experimentally verify whether the selected device topology can produce peak power and pulse risetime equivalent to or better than that of the SOTA. [*OCT–NOV21*].

(C) Milestone – Use Semiconductor Power Technologies (SPT) developed DSRDs and Voltage Multiplier Inc. developed Axial-lead Glass-body Diodes as alternatives to delayed breakdown diodes for pulse sharpening. [*Alternative to Milestone B, OCT–NOV21]*].

1. Task – Fabricate test fixtures for connecting DSRD and VMI diodes to DSRD–IES pulse generator, as described in **Section 6.4** or MegaImpulse PP10731 pulse generator. [*OCT–NOV21*];
2. Task – Test pulse sharpening using single, 2-stack, and 3-stack SPT DSRD and/or VMI diodes using the fixtures developed in Task 1. [*OCT–NOV21*]
3. Task – Prepare a performance matrix of DSRD and VMI diodes as pulse sharpeners as a function of variations in DSRD test parameters discussed in **Section 6.3**.

(D) Milestone – Model diode/dynistor topologies and fabrication process. [*on hold until Milestones A and B are completed*].

1. Task – Model silicon diode and dynistors, with optimized device cross section (size, geometry) based on theory and simulations to increase current and thermal dissipation. [*On hold*];
2. Task – Model/design fabrication process with optimum device topology and doping concentration. [*On hold*].

6.5.3 Progress Made Since Last Report

(A.1) Additional scientific literature on semiconductor pulse sharpeners has been reviewed.

(B.1) Our Silvaco TCAD license is being renewed and a simulation workstation is being configured. TCAD simulation and device modeling materials are being reviewed.

(C.1) Test fixture for pulse sharpening using DSRD as SAS/DBD has been designed and fabricated.

Figure 6.5.1 shows a schematic of a DSRD–IES pulse generator with a DSRD (DBD) connected as the pulse sharpener, and Figure 6.5.2 shows a fixture being made to test DSRD as sharpener. The output pulse from the DSRD–IES pulse generator is fed into the sharpener (DBD) through the output capacitor C_{out}.

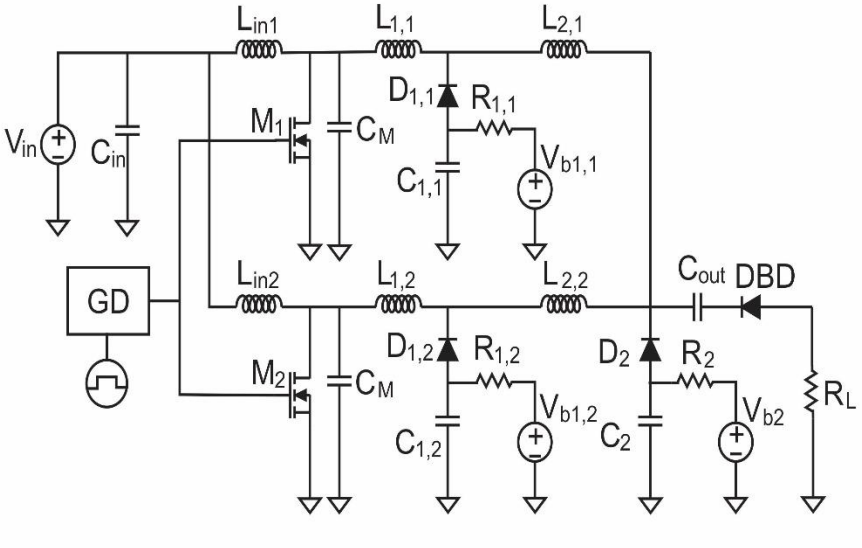


Figure 6.5.1. A schematic of a DSRD-IES pulse generator with a DSRD diode as SAS/DBD pulse sharpener.

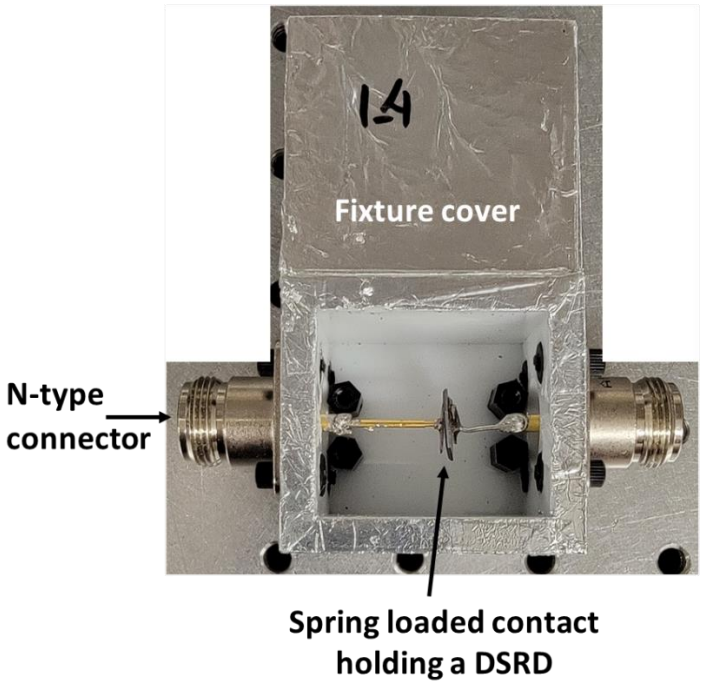


Figure 6.5.2 Test fixture for DSRD as SAS. A single DSRD or multiple stacks of DSRDs sit in between the spring-loaded contacts inside an insulating housing.

(C.2) Preliminary tests of SPT Gen2 diodes and COTS diodes from VMI as SAS have been performed using the test fixture described in C.1. However, the obtained output voltage was not affected by whether the diode was connected or not. This suggested an unmatched impedance between the source and the fixture. Further design of the fixture is underway.

6.5.4 Technical Results

(A) Based on the review materials [2], [3], [12]–[18], [4]–[11], the ranges of peak power and risetime of different switches is presented in Figure 6.5.3.

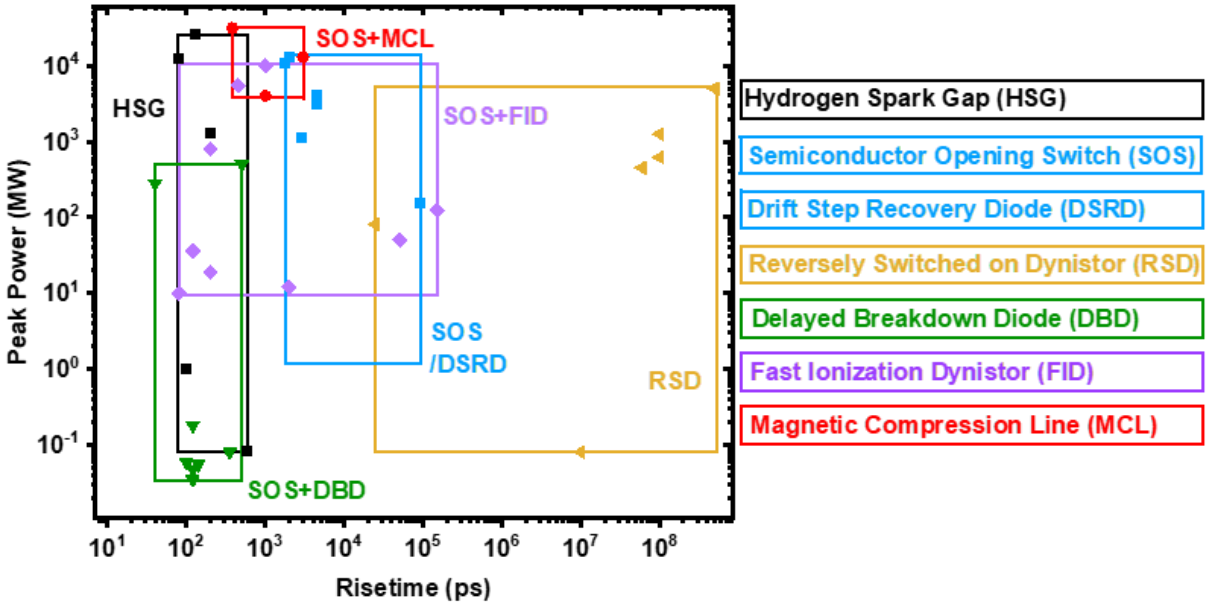


Figure 6.5.3. Ranges of peak power and pulse risetime of different types of high-power switches.

(B) DSRD (p^+–n–n^+) and SOS (p^+–p–n–n^+) are [ideally] similar to different structures of delayed breakdown diodes (DBD). The only difference between them is their working principles. DSRD and SOS pulsers need a forward pumping current and their switching is based on extracting the injected charge, while DBDs work completely on reverse bias by switching these devices due to the delayed impact ionization by a steep reverse voltage rise rate of ~10 kV/ns. In the presence of certain defect states in silicon, they are switched by voltage pulses with rise rate of ~1–2 kV/ns. Therefore, we can at least try a single DSRD or SOS die in a DBD configuration to test the pulse sharpening performance given that power switches producing about 3 kV with 10 kV/ns rise rate are available.

6.5.5 Summary of Significant Findings and Mission Impact

(A) We have reviewed a number of literature reports on different approaches for pulse power generation and sub-nanosecond pulse sharpening, such as hydrogen spark-gap (HSG), solid-state pulse generators including SOS–IES based generator with semiconductor sharpener, diode-based non-linear transmission line, pulse generator based on Si and GaN photoconductive switches, and pulse generators with magnetic compression line. No single technology appears to meet or exceed the key performance metric requirements across the board. Where HSG lead in peak voltage and peak power, in comparison to the other technologies of interest, they lack in their ability to meet the required PRF, device lifetime, and SWaP-C metrics. All solid-state switching power supplies utilizing SOS and semiconductor sharpeners seem to be potentially viable technologies to compete against HSG with comparable or better SWaP-C metrics.

6.5.6 References

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7 GaN-Based Source Alternatives

7.1 Development of a GaN-Based Power Amplifier RF Source

(Feyza Berber Halmen, Abu Hanif)

7.1.1 Problem Statement, Approach, and Context

Primary Problem: To achieve the SWAP-C2 performance metrics necessary to support the cUAV Naval afloat mission, gallium-nitride-based high electron mobility transistors (GaN HEMT) require multiple amplification stages in series to transition a low voltage/power signal (1-V, 1-GHz), to the high-power levels. Even the best high-power GaN HEMTs are limited to 2–3 kW of peak power. Achieving the necessary effective radiated power (ERP) out of a high gain (≥ 10-dBi) narrow-band antenna requires input power increase of two to three orders of magnitude and thus multiple parallel branches of HEMTs and/or power combining and pulse compression to achieve ERP at the MW scale.

Solution Space: Pulse compression and power combination techniques are used to increase the peak power and lessen the pulse width in high power microwave (HPM) applications. Adapting multiple pre-amplification stages to increase the power levels to the appropriate inputs required by GaN HEMTs in a reconfigurable fashion facilitates leveraging commercially available off the shelf (COTS) devices and combiners to be pulse compressed and thus achieve sufficient ERP with an optimal radiating element.

***Sub-Problem 1*:** Pulse compression is generally used to generate a pulsed output with a high peak output power (P_{out_peak}) and a wideband frequency content from a DC input voltage. The main challenge lies in identifying a pulse compression technique that can be used to amplify a narrowband RF input signal. Some of the circuit elements for common pulse compression techniques, such as the saturable inductors used for energy storage in magnetic pulse compression (MPC), exhibit increasingly lossy behavior with high frequency. Another challenge will be to determine, if any, the operating frequency limits of the suitable pulse compression technique for high-frequency, high-power signals.

Sub-Problem 2: SPICE models for state of the art (SOTA) high power GaN HEMT power amplifiers (PAs) which can produce higher than 1-kW peak power, that can be used with our currently available simulation platforms, are not available from the GaN vendors. Die and packaged device level GaN models are only offered for use in two highly specialized non-linear circuit simulators, Keysight's ADS and Cadence's AWR, used especially for power amplifier design. Lack of access to internal GaN device nodes represents a challenge in optimizing GaN PA design for SWAP-C2 performance metrics.

Sub-Problem 3: A custom built prime power unit with adjustable output power needs to be developed to supply the necessary voltage and current for the PA unit. For example, MACOM MAPC-A1500 requires 65 V, 1.3 A prime power unit for an efficient operation whereas INTEGRA IGN1011S3600 requires 100 V 150 mA unit. Therefore, the design needs to be dynamic since the required power will vary depending on the number of series and parallel stages of the GaN HEMTs PAs as well as the module to be used since different manufacturer require different power levels for their respective PA module.

State-of-the-Art (SOTA): Large modular RF pulse generators (>1-m^3, >1000-lbs) which are comprised of at least 8 parallel-combiners, have demonstrated peak output power up to a few GWs. All these prototypes are stationary and rack mounted. Smaller versions (~0.125-m^3, 50-lbs to 100-lbs) can achieve 50 kV peak voltage with PCR of 667 at 70 ns FWHM terminated at 307 Ω load [1]. Another power amplifier manufactured by Amplifier Research has an output of only 800 W peak power which weighs 70 lbs [2]. However, none of them are suitable for Navy afloat missions due to weight to peak output power ratio.

Deficiency in the SOTA: Large RF pulse generators are traditionally limited by mechanical design constraints and power supply limitations. They are large (few meters long), leverage huge transformers, and require liquid coolant such as transformer oil for cooling purposes, which lead to undesirable system mass values even more than 1000 lbs. In addition, a comprehensive analytical study on pulse compression and peak output power is missing in SOTA; specifically, as it pertains to GaN-based RF sources.

Solution Proposed: Developing a highly efficient and cost effective GaN-based power amplifier RF source capable of achieving 1–5 W/cm^2 at a distance of 10–50 m with the minimum number of series connected modules (i.e., M×N) with maximum volumetric power density. Therefore, methodically the optimum peak output power and maximum pulse compression ratio through topological GaN based power amplifier design including the power combination including reconfigurable antenna design and the necessary components therein that maximize power/voltage gain and efficiency achieved by the RF source as well as the output parameters such as peak power, pulse width, etc., are adjustable in real time at will to meet the mission needs.

Relevance to OSPRES Grant Objective: Reconfigurable RF source with adjustable RF parameters (e.g., output power, pulse width, bandwidth, frequency) will enable the system to exercise dynamic MPM missions (i.e., multi mission) with optimal SWaP-C2 parameters.

Risks, Payoffs, and Challenges:

Risks: Existing GaN based high output peak power yielding amplifiers such as MAPC-A1500 (peak power of 2600 W) and IGN1011S3600 (peak power of 3600 W) are out of stock. Lower-power versions produced by the same manufacturer that have been quoted have long lead times (26-weeks ARO) and require minimum of 50 to order making them thousands of dollars to purchase. Alternatively, building the amplifier module from scratch will take its toll in time as well as the performance of the built prototype might be poor in terms of efficiency and form factor.

Payoffs: Building the amplifier module from scratch will payoff in terms of utilizing the lead time to find the most suitable pulse compression method that can achieve 2–3 orders of peak power and compression gain which will eventually meet the mission needs and therefore, the appropriate compression method can be immediately deployed with the COTS GaN amplifiers once they are received.

Challenges: High power PAs and pulse compression methods are usually lossy in nature and generate considerable amount of heat, therefore, designing a proper cooling method

must be carried out which may inadvertently increase the volume (size and weight) of the overall design.

7.1.2 Tasks and Milestones / Timeline / Status

(A) Milestone – Achieve 2–3 times increase in peak power and compression gain using magnetic pulse compression (MPC) [*estimated completion by JAN22*].

1. Subtask – Model saturable inductors in LTSpice or Matlab/Simulink in order to be able to develop MPC simulations / NOV21 / Ongoing.
2. Subtask – Design of MPC circuit with RF input and simulation in LTSpice or Matlab/Simulink to evaluate the resulting amplification and frequency content. / [On hold until the saturable inductor simulation model is realized].
3. Subtask – Model the high frequency behavior of MPC circuit / NOV21 / Ongoing.
4. Subtask – Build and test the MPC prototype using bench top power supply / OCT–*DEC21 / Ongoing*.

(B) Milestone – Achieve peak power level of 1.8 kW using QORVO QPD1025L and QORVO evaluation board / NOV21 / Ongoing.

(C) Milestone – Obtaining 2–3 times increase in peak power and compression gain using QORVO QPD1025L GaN HEMT PA and MPC prototype built in milestone A [on hold until milestone A and B are complete]

7.1.3 Progress Made Since Last Report

(A.1) Vendors for the purchased magnetic cores were contacted to obtain B–H curve data needed for saturable inductor modeling. Even though the B–H curves for current magnetic cores were not obtained as they are considered proprietary information by their vendors, sample B–H curve for another magnetic core was acquired and will be used in the initial model of the saturable inductor.

(A.3) High frequency losses for different magnetic core materials were investigated.

(A.4) A basic MPC prototype for DC input was built and tested in lab using a bench top power supply to provide insight into circuit operation and challenges.

(B) GaN gain stages were determined based on the required input drive for the 1.8 kW QORVO QPD1025L GaN HEMT PA, the highest output power GaN PA available at the moment. Supply chain problems are causing delays in finalizing the GaN PA module design. Methods for pulsed operation were investigated and RF input pulsing was chosen for the initial prototype. Due to lack of GaN PA simulation tools, vendor-provided evaluation boards that are not suitable for drain or gate pulsing will be used. Bias up/down sequence required to ensure GaN PA stability was established to plan the timing sequence for the prime power unit.

7.1.4 Technical Results

(A.4) Basic magnetic pulse compression circuit and the expected voltage and current waveforms are depicted in Figure 7.1.1 [3]. For a given DC voltage input, the voltage level

is preserved while consecutive capacitors are being charged and discharged and the discharge current is time compressed – hence, the increased peak value – by scaling the inductance value of saturable inductors at saturation. As a result, the peak power is increased at each stage by a factor determined by the ratio of corresponding saturation inductances.

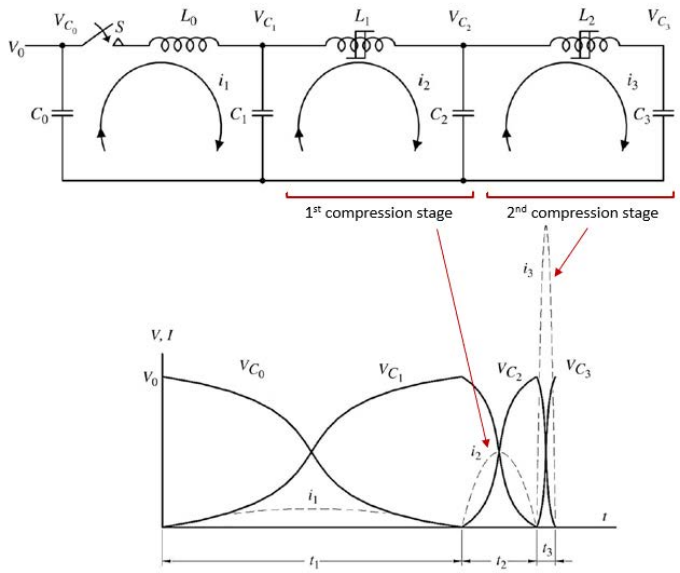

Figure 7.1.1. Schematic and expected waveforms of a 2-stage MPC unit for DC input.

Figure 7.1.2 depicts the prototype MPC circuit built with available circuit components. L0 is an 'air-core' inductor whereas L1 and L2 are built using NiZn toroid magnetic core. As the core permeability data was not available for NiZn toroid, it was calculated from the measurement results to estimate the change in inductance during saturation.

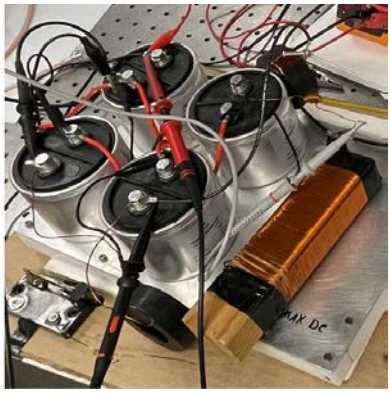

Figure 7.1.2. 2-stage MPC prototype for DC input.

Measured voltage waveforms for the first stage of MPC are given in Figure 7.1.3 along with the depiction of circuit operation during consecutive time periods. The current waveforms were not measured due to lack of Rogowski current probe. However, the

voltage waveforms provide great insight into the circuit operation and the possible challenges.

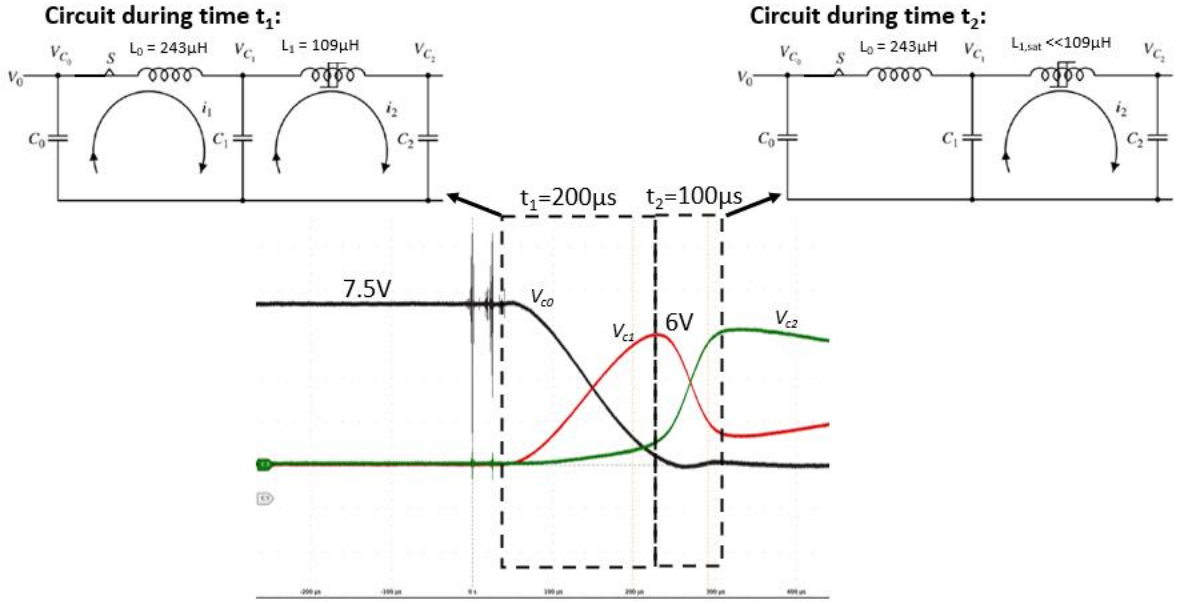

Figure 7.1.3. 1-stage MPC voltage waveforms and circuit operation for DC input.

As the input switch is closed, C0 is discharged and C1 is charged during time t1. Increase in VC2 during time t1 suggests a pre-mature current i2 flow which prevents VC1 to increase to VC0 level. This can be prevented by an increase in L1 inductance value. As VC1 increases, inductor L1 starts to saturate, causing its inductance value to decrease and C1 to discharge through the saturated inductor L1 during time t2. Saturation inductance for L1 is calculated as 51uH, approximately half of the initial L1 inductance, from the t2 duration of 100us. This value is much higher than the expected saturation inductance and suggests that inductor L1 might not be fully saturated with input voltage of 7.5V.

For the next set of measurements, 2-stage MPC was used with the input voltage initially increased to 9V and then to 27V to ensure saturation of the inductors. The resulting voltage waveforms are depicted in Figure 7.1.4. The decrease in time duration t2 to 65us and 30us with 9V and 27V input, respectively, suggest an improvement in the saturation of inductors with increasing voltage. The leakage currents through the inductors, suggested by the pre-mature charging of the capacitors, does not permit further meaningful analysis of the circuit. The measurements with the prototype provided invaluable insight into MPC circuit operation, especially in terms of inductance scaling and saturable inductor operation. Availability of magnetic core B-H curves, either through vendors or through data collection in lab, will enable the design of the second prototype.

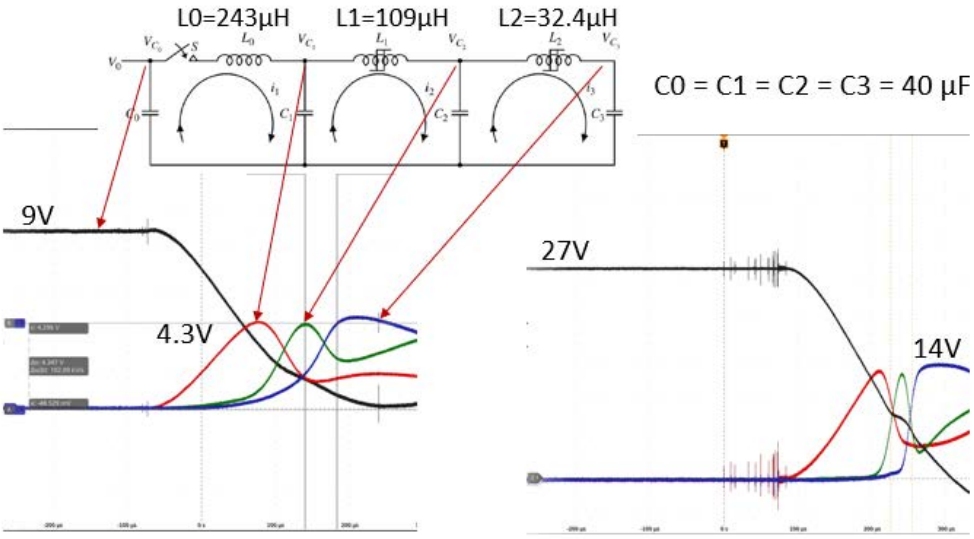

Figure 7.1.4. 2-stage MPC voltage waveforms for DC input of 9 V and 27 V.

(B) GaN power amplifier gain stages were designed to accommodate the QORVO QPD1025L GaN HEMT PA to output a peak power of 1.8kW. GaN PAs, especially when operated at compression to obtain the highest output power possible, have RF gains of less than 20dB. This necessitates the use of multiple stages of PAs, connected in series, to achieve the required amplification of the mV level RF signal obtained from a frequency synthesizer or a voltage-controlled oscillator (VCO). Figure 7.1.5 depicts the power budget for the designed amplifier chain. A maximum interstage loss of 2dB is included in the power budget to account for any losses due to matching or isolation elements between the amplifiers.

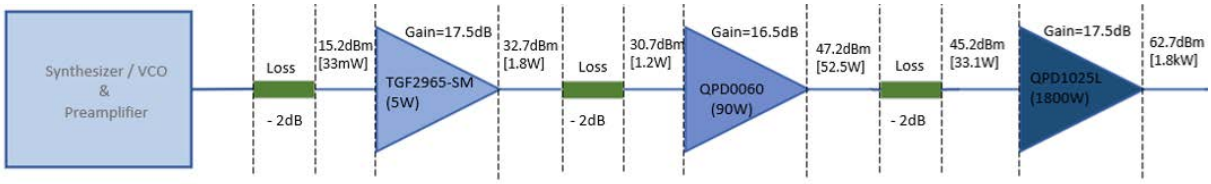

Figure 7.1.5. Power budget for the GaN PA gain stages.

DC bias conditions, as well as the maximum and minimum allowable gate voltage values, are summarized in Table 7.1 for the GaN PAs. A bias network that will provide the required DC voltages is being designed. GaN PAs used in the design are all depletion mode devices which draw excessive current at 0V DC gate input which can lead to device failure. Stability of the GaN PA is also very sensitive to the gate and drain voltage combinations. Therefore, the bias network design will also incorporate a bias-up/down sequence as depicted in Figure 7.1.6 to ensure the stability of the GaN PAs as well as limitation of excessive currents.

Table 7.1. GaN PA DC bias conditions and limits.

	TGF2965-SM (5W)	QPD0060 (90W)	QPD1025L (1.8kW)
Operating Voltage	32 V	48 V	65 V
Minimum V_G	-7 V	-7 V	-7 V
Pinch off V_G	-5 V	-4 V	-5 V
Maximum V_G	+2 V	+2 V	+2 V
Typical V_G (Class AB)	-2.7 V (I_{DQ} =30 mA)	-2.7 V (I_{DQ} =130 mA)	-2.8 V (I_{DQ} =1.5 A)

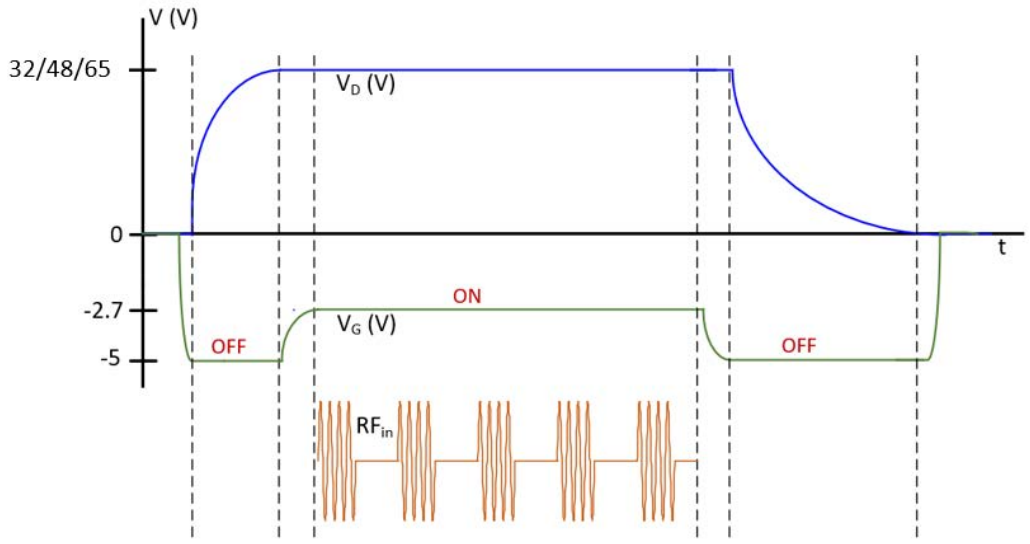

Figure 7.1.5. GaN PA bias up/down sequence to ensure GaN stability & limit excessive currents

Different pulsed operations techniques were investigated for the GaN PA. Commercial evaluation boards from vendors, which will be used for the initial prototype, do not permit drain or gate pulsing due to large storage capacitors, in the order of uF and mF, used in the bias line designs. Therefore, RF input pulsing will be used for the pulsed power operation of the GaN PA. Control circuit to provide bias and RF input sequencing as depicted in Figure 7.1.5 is also being designed.

7.1.5 Summary of Significant Findings and Mission Impact

(A) A basic 2-stage magnetic pulse compression was built and tested with DC input. Observations were made on the inductor sizing to minimize leakage currents and the voltages required to saturate the inductors. These considerations will be taken into account for the design of magnetic pulse compression circuit at RF frequencies.

(B) GaN power amplifier gain stages were determined based on the gain and output voltage levels of commercially available GaN PAs. The initial considerations for bias and pulsed power operation were investigated to provide a guideline for the bias network and the timing control design. GaN HEMTs employed in this design are depletion-mode transistors. Negative voltage should be applied to the gate to avoid excessive currents and the gate should be kept at pinch off during drain voltage turn on and off to ensure stability. Due to large bias line capacitors of the vendor-provided evaluation boards, RF input pulsing will be used for the pulsed operation.

7.1.6 References

[1] D. Zhang, Y. Zhou, J. Wang and P. Yan, "A compact, high repetition-rate, nanosecond pulse generator based on magnetic pulse compression system," in IEEE Transactions on Dielectrics and Electrical Insulation, vol. 18, no. 4, pp. 1151-1157, August 2011, doi: 10.1109/TDEI.2011.5976109.

[2] https://www.arww-modularrf.com/rack-mount-amplifiers.cfm

[3] Jane Lehr, Pralhad Ron, Chapter 6.3: Magnetic Pulse Compression in *Foundations of Pulsed Power Technology*,Wiley-IEEE press, 2018, pp. 313-314

8 Thermal Management

8.1 Ultra-Compact Integrated Cooling System Development

(Justin Clark, Roy Allen, and Sarvenaz Sobhansarbandi)

8.1.1 Problem Statement, Approach, and Context

Primary Problem: A thermal management system (TMS) is required for cooling semiconductor-based pulse-power devices, with the goal of maintaining the semiconductor device temperature below 80 °C. The proposed system must increase cooling densities, while decreasing pumping power requirements, in-line with the SWaP-C[2] objective.

Solution Space: To achieve such high cooling densities, an ultra-compact TMS (UC-TMS) directly integrated onto the semiconductor is proposed. Such a design is capable of creating turbulent flow in order to enhance the heat transfer rate. The proposed UC-TMS is restricted to 1 cm^2 surface area, therefore, the required pumping power should be kept to a minimum. An array of micro-sized jet nozzles will provide a turbulent flow onto a microchannel section directly on the semiconductor device. The UC-TMS design will reach turbulency at a faster rate while requiring less energy consumption.

Sub-Problem: The turbulency formed from the array of nozzles creates an extreme pressure loss from the large amount of jet nozzles (over 200) and a flow diameter of 100 microns. The pressure must be sustained to enable proper cooling and circulation processes.

State-of-the-Art (SOTA): Integrated chip cooling is being widely used to dramatically increase the operational power of high voltage silicon-based power devices. However, the current SOTA devices include individual parts which attach to a high-power device, causing less interaction between the semiconductor and coolant, degrading the heat removal rate.

Objective: The proposed UC-TMS design is based on refining in-chip jet-impingement geometry through leveraging theory and a parametric evaluation of nozzle geometry and flow channel arrangements. A Si-base unit will be prototyped to maneuver a higher capacity of heat removal. Moreover, to sustain the pressure, the application of different working fluids is suggested. Several types of coolant will be simulated to determine effects from fluid density and viscosity.

Anticipated Outcome(s): To create a UC-TMS with the ability to rapidly remove 1 kW/cm^2 of heat. A design capable of such high heat removal can be implemented on many applications such as high-power batteries.

Challenges: The manufacturing techniques of the semiconductor devices have not yet been adopted for integrated chip cooling systems. The proposed compact design is restricted due to low tolerance of the manufacturing process, as this process must be capable of layering the silicon TMS onto the semiconductor.

Risks: With a system so compact, the pressure drop could be a large issue regarding the objective heat dissipation rate. An extreme pressure drop would potentially cause the coolant to flow backwards, causing less fluid-to-solid interaction.

8.1.2 Tasks and Milestones / Timeline / Status

(A) Design a Si base 1 cm^2 UC-TMS, applying manufacturing tolerances, to achieve a heat dissipation rate of 1 kW/cm^2. The design must be able to be produced by manufacturing techniques such as etching and lithographic layering processes. To confirm the device can be manufactured as proposed, each section of the model will be layered step by step. / MAY21–AUG21 / Completed

(B) Using the optimal design, perform ANSYS simulations using either water or Si-C nanofluid. Other fluid types may be researched as pressure drop is a large factor / JUL21–DEC21 / In Progress

(C) Improve design parameters and sizing to have a lower pressure drop while having a high heat dissipation capability. Prove simulations from previous literature to show capable design configurations with acceptable pressure drop and steady temperature. / NOV21–JAN22 / In Progress

(D) With proper simulation results, manufacture a prototype to begin experimental testing and evaluation / JAN22–APR22 / Upcoming

8.1.3 Progress Made Since Last Report

(B) We began the simulation process in Ansys Design Modeler for the chosen design to simulate the fluid interaction within the device. Following this step, using Ansys fluent the design was given a heat flux on the lower surface to represent the pulse-power device. The device being capable of maintaining temperature while a large amount of heat is applied proves the capability of either jet impingement or microchannel fins. However, simulations determined there to be a negative pressure in the outlet of the device, causing the device to not function properly.

(C) From previous experiments on jet-impingement methods, a large pressure drop is expected. Other techniques and methodology were reviewed following a representation of the simulation results. A parallel flow TMS was chosen to validate and optimize which type of cooling technique would help reduce the pressure drop. The results showed a very minimal pressure drop compared to any jet impingement technique, although this device used the method of a hot spot instead of the whole surface having an applied heat flux.

8.1.4 Technical Results

(A) A large pressure drop was predicted from the current UC-TMS design. However, simulation showed a negative pressure on the outlet. Therefore, the fluid would reverse flow and not properly recirculate to maintain the device temperature of 80 °C.

(B) Using ANSYS Fluent, a simulation was conducted to determine pressure drop of the preliminary design using 0.5 m/s fluid inlet velocity. The results showed a 100 kPa pressure drop throughout the system. Other techniques involving types of coolant or dimensional optimization will be thoroughly investigated and applied to the model to compare the effects to pressure. Applying a 1 kW/cm^2 heat flux at the simulated heat source using plain silicon fluid as the coolant enabled the device to reach up to 129°C. Since this temperature is greater than the melting point of the semiconductor, a second simulation was conducted applying a 600 W/cm^2 heat flux to the surface. This resulted in a maximum temperature of 86°C, which is just at the melting point of the switch.

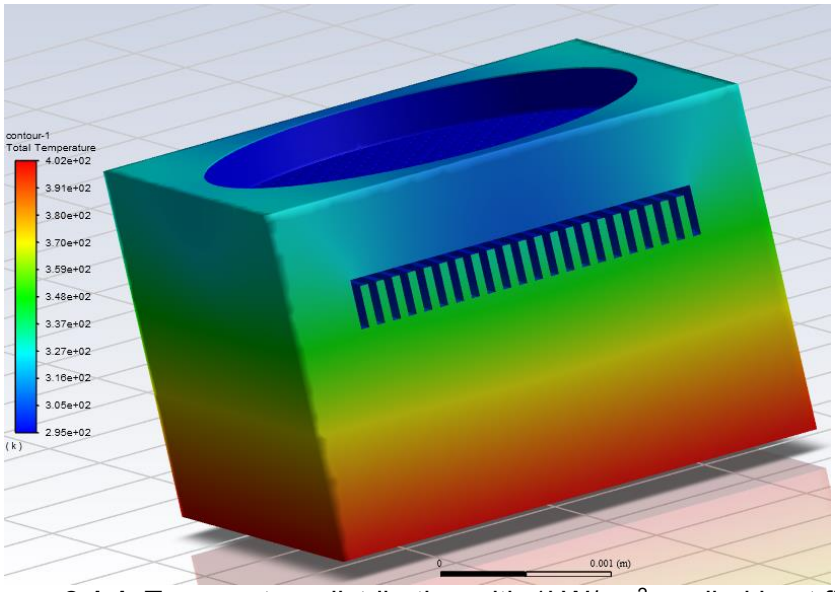

Figure 8.1.1. Temperature distribution with 1kW/cm^2 applied heat flux

(C) A model was drawn representing a 3 mm x 3 mm parallel TMS with an active 0.5 mm x 0.5 mm hot spot. A heat flux of 1 kW/cm^2 was applied to the hot spot with a fluid inlet velocity of 0.5 m/s. The literature this model was used in did not denote the velocity inlet, therefore the same velocity was applied to it as the jet-impingement design to compare pressure drop. The pressure drop reached only 1.8 kPa which is significantly lower than the preliminary JI-TMS design. Therefore, further research will be needed to determine the optimal design and fluid flow configuration.

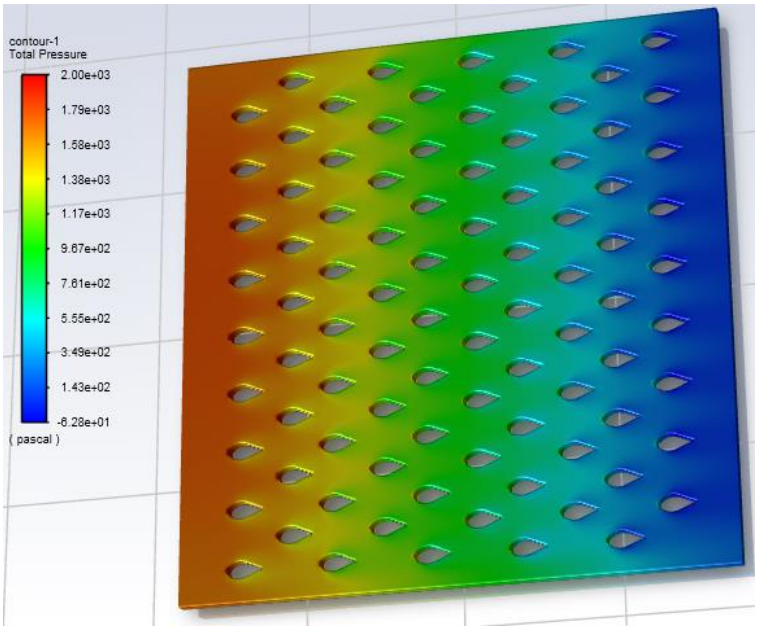

Figure 8.1.2. Parallel Flow Pressure Drop using 0.5 m/s inlet velocity.

8.1.5 Summary of Significant Findings and Mission Impact

(A) From a literature review, similar designs were analyzed including a water-cooled, crossflow microchannel cooling system with various microchannel widths has been previously designed. The design achieved a simulated heat flux of 1.7 kW/cm^2 using 0.056 W of pumping power. Although this design is not the best fit when including the manufacturing constraints, the results using micro channel heat sinks are remarkable and design considerations are further analyzed. A similar design implemented the idea of having jets confined in their own individual spaces, experimentally reaching up to 900 W/ cm^2 with 0.83 W of pumping power. A third design analyzed two types of heat sinks with flat and oblique angled fins which were experimentally tested with a constant heat flux of 100 W/cm^2. The temperature difference was from 60 °C to 35 °C which proposed giving the design more power. The oblique angled fins caused 20 percent greater heat transfer than flat fins.

(B) To achieve a higher quality mesh around the nozzles and microchannels, the nozzles element size was initially set to 20 microns, or until the shape of the nozzles were more profound in a cylindrical shape. The surface which connects to the nozzles resulted with an element size of 15 microns and the nozzle sizing resulted in 13 microns. These values had to maintain an equivalent size to reduce the skewness and maintain mesh quality. Each surface with inadequate quality was selected and set to individual face sizing and is currently undergoing simulation.

To reduce the pressure loss while maintaining an effective turbulent flow produced by the jet nozzles, the microchannel fin designs did not effectively enhance the rate of heat transfer. The combination of micro channels and jet impingement caused too high of a pressure loss, causing the fluid to reverse its flow; therefore further enhancement of the UC-TMS will be based explicitly on jet impingement theory.Pulse Forming Networks

9 Pulse-Forming Networks

9.1 Diode-Based Nonlinear Transmission Lines

(Nicholas Gardner)

9.1.1 Problem Statement, Approach, and Context

Primary Problem: The size, weight, and cost of pulse forming/shaping networks (PFNs) need to be reduced and optimized for Navy afloat missions.

Solution Space: Develop a diode-based nonlinear transmission line (D-NLTL) as a pulse shaping network for the conversion of energy to the ultra-high frequency (UHF) band (0.3–3 GHz) at single MW peak power.

Sub-Problem: Metrics used for component selection are designed for D-NLTLs operating at sub 0.1 GHz frequencies. Using such metrics alone to design D-NLTLs capable of single GHz frequency generation introduces a trial by error nature to the design process wherein frequency/power generation predictions and measurements can differ by a few hundred MHz or the design potentially fails to operate at all.

State-of-the-Art (SOTA): D-NLTL prototypes have been shown to generate center frequencies of 0.2–0.5 GHz at kV amplitudes in a light-weight small-footprint circuit. Simulations of LE-NLTLs indicate achievable frequencies in the single GHz range.

Deficiency in the SOTA: Simulation/measurement agreement becomes increasingly sensitive to parameters and factors outside of inductive and capacitive element choice alone at frequencies above ~100 MHz. Disparities between measurement and simulation above contribute to a trial by error design process for D-NLTL networks.

Solution Proposed: Identify and characterize diode parameters affecting frequency generation in the context of a NLTL application via simulation and experiment, and identify limits/desired ranges required for UHF generation. Such parameters include, but are not limited to: diode frequency response, diode reverse bias hold-off voltage, diode small signal capacitance, diode chip/package parasitics, and diode relaxation time. The improved understanding of the explored parameters will be used to design and fabricate a D-NLTL capable of GHz center frequency generation at single MW peak powers.

Relevance to OSPRES Grant Objective: The SWaP-C^2 capabilities of D-NLTLs (shown in Figure 9.1.1) represent a potential solution to the size, weight, and cost optimization issue for PFNs on Navy afloat missions.

Figure 9.1.1. 20 cell D-NLTL of dimensions 1.1 x 23.45 cm constructed with commercial off the shelf components.

Risks, Payoffs, and Challenges: There exists a potential tradeoff between power and frequency generation. Devices such as ceramic capacitors may be used in a D-NLTL to generate high peak power due to their break down potentials in the 10s of kV, however,

such devices become highly resistive at 0.1–0.2 GHz frequencies. Diodes have been shown to be operational at frequencies upwards of 0.4 GHz, however, possess low hold-off potentials limiting peak output power. The payoff to overcoming these challenges is significant reductions in PFN size and cost.

9.1.2 Tasks and Milestones / Timeline / Status

(A) Milestone – Construct/demonstrate a prototype capable of UHF generation at low voltages (1–100 V excitation amplitude)

(A1) Break a low-voltage pulse into a sequence of solitons (SEP20)

(A2) Increase frequency generation past 200 MHz (NOV20)

(A3) Select diode candidate (junction capacitance <50 pF) and simulate expected results (Ongoing)

(A4) Design/fabricate/test line (Ongoing)

(A5) Write/Submit manuscript on D-NLTL design processes (**Ongoing/In Revision**)

(B) Milestone – Demonstrate tuning of waveform at low voltages using electrical or mechanical means (Completed with voltage biasing APR21)

(B1) Write/Submit manuscript on LV D-NLTL tuning circuit (**Ongoing/In Revision**)

(C) Milestone – Construct/demonstrate a prototype capable of frequency generation above 1 GHz at single MW peak powers (Completed MW peak power but not GHz center frequency – Ongoing)

(C1) Identify diode candidates with a hold-off voltage of several kV and a low signal junction capacitance under 100 pF (Completed JAN21)

(C2) Design/fabricate single diode prototypes (Completed JAN21)

(C3) Perform initial tests using half-barrel pulse source (Completed FEB21)

(C4) Refine simulation using measurements (Completed FEB21)

(C5) Test a prototype using two diodes in series (Completed FEB–MAR21)

(C6) Test lines using Mega Impulse source (Completed MAY21**)**

(C7) Test K50F D-NLTL using PCSS as a source (Completed JUN21)

(C8) Use simulations and tests to refine line for increased frequency generation (Completed JULY21)

(C9) Rebuild lines for negative polarity pulses (Completed JULY21)

(C10) Test lines using PCSS as a source with various cell inductances (Completed JULY**)**

(C11) Test lines using Marx Generator as a source (Completed AUG21)

(C12) Reconstruct PCSS strip line to produce a pulse similar to 5.1.2 (left) and retest (Ongoing AUG21)

(C13) Write/Submit manuscript on the GHz MW D-NLTL Prototype (**Ongoing/In Revision**)

(D) Milestone – Demonstrate power scalability using an array of D-NLTLs (On Hold – Prioritizing Milestone C)

(D1) Design a prototype capable of running two D-NLTLs simultaneously off of the same excitation pulse (Completed JUN21)

(D2) Build a circuit capable of measuring the CV curve of low-voltage diodes and measure the CV curves of unused diodes and heavily used diodes (Completed JUN21)

9.1.3 Progress Made Since Last Report

Experimental D-NLTL work focused primarily on the continuous wave D-NLTL based comb generator application. See section 9.2. Work also progressed on the 3 D-NLTL manuscripts currently under revision tied to milestones A, B, and C.

The manuscript tied to milestone A covers the D-NLTL design process. Rules of thumb are presented for producing a D-NLTL for a desired power and frequency range. The rules of thumb cover diode selection, device simulation, and prototype fabrication.

The manuscript tied to milestone B documents results from a low voltage prototype capable of electrically altering diode CV properties through the application of a DC bias. Results presented include the ability to electrically tune the center frequency as well as use of a bipolar excitation pulse to increase frequency generation and mitigate effects from the source-line impedance mismatch.

The manuscript tied to milestone C documents two high voltage D-NLTLs capable of MW peak power generation, center frequencies in the UHF band, and Bragg frequencies in the L-band. Three pulsed sources of varying rise time, amplitude, and full with at half max are used to further demonstrate the need to consider excitation pulse geometry when designing a D-NLTL.

9.1.4 Technical Results

9.1.5 Summary of Significant Findings and Mission Impact

(A) After a failure of the high-voltage diode-based nonlinear transmission lines (D-NLTLs) to reproduce simulated results, work refocused on low-voltage D-NLTLs to determine the source of the discrepancy. In NOV2020 a center frequency of ~250 MHz was achieved using a D-NLTL design based on the diode model SMV1702.

(B) Following the success of the SMV1702 D-NLTL, a circuit was designed, capable of electrically tuning the center frequency utilizing DC biasing of the diodes. In FEB–APR2021 the circuit demonstrated a linear relationship between DC bias up to a limiting potential. Negative DC biases decreased center frequency while positive DC biases increased center frequency.

(C) In JAN2021 two diode candidates (models K100F and K50F) were identified for a HV D-NLTL design. FEB2021 saw successful tests of both D-NLTLs with each

sharpening the rise time of a pulse produced by a DSRD based source down from ~1 ns to ~600 ps. In AUG2021 the first major variation between the K50F and K100 F D-NLTLs were observed with the K50F line breaking the pulse into solitons while the K100F line primarily sharpened the rising edge of the pulse. In SEPT2021 comparisons between measured and simulated results for Marx+K50F measurements indicate further success in modeling inductor and diode parasitics to predict frequency generation.

(D) During MAY2021 a line topology capable of feeding two identical D-NLTLs with the same pulsed source at the same time was fabricated. Initial results were collected, and a prototype is currently being designed to test the ability to parallelize D-NLTLs.

9.2 Continuous Wave Diode-NLTL based Comb Generator

(Nicholas Gardner and John Bhamidipati)

9.2.1 Problem Statement, Approach, and Context

Primary Problem: When used as a pulse shaping network (PSN), diode-based nonlinear transmission lines are promising solutions towards reducing the size, weight, and cost of RF and microwave sources on Navy. However, D-NLTLs have a dynamic impedance leading to signal/power reflection, standing wave generation, and return power losses at both the source-line and line-load interfaces leading to difficulties in practical D-NLTL applications.

Sub-Problem: Design parameters for COTS high-frequency D-NLTL based comb generators capable of generating up to ~50 GHz output frequencies are limited to <1 Watt output powers, which is <0.1% of the power handling capability required for navy afloat missions. Using such metrics alone to design D-NLTLs capable of generating ~1–2 GHz frequency with capability to handle MW-order peak powers could potentially introduce design errors resulting in frequency/power prediction-measurement discrepancies on the order of few hundred MHz.

Solution Space: Use a D-NLTL as a pulse shaping network (PSN) to convert continuous wave (CW) signals from low frequency–very high frequency (LF–VHF) bands (0.03 MHz–30 MHz) to the ultra-high frequency (UHF) band (0.3–3 GHz) at ones-of-MW peak power.

State-of-the-Art (SOTA): Commercial-off-the-shelf (COTS) GaAs varactor diode-based monolithic microwave integrated circuit (MMIC) D-NLTL comb generators are capable of operating at input and output frequencies up to 600 MHz and 30 GHz, respectively. However, these comb generators are not capable of handling powers higher than 27 dBm (0.51 W). In-house pulsed D-NLTL prototypes have been shown to generate center frequencies of 0.2–0.5 GHz at kV amplitudes in a light-weight small-footprint circuit.

Objective: Demonstrate both reduced parasitic effects of the dynamic source-line impedance mismatch presented by a D-NLTL, as well as L-Band output frequencies at powers of 0.1 – 5 MW.

Anticipated Outcome(s): A successful demonstration of improvements to impedance matching at the source-line interface using a CW signal measured as a reduction in signal amplitude loss between the source and D-NLTL.

Challenges: Nonlinear signal dependent behavior provided by a reverse bias diode produces difficulties in predicting generated waveform behavior. Further D-NLTL performance is limited in both frequency and power generation by the availability and variety of COTS Schottky and epoxy diodes.

Risks: The reverse bias hold off potential (V_R) of a chosen diode limits the power generation capabilities of the system. If an excitation is used that exceeds V_R diodes risk being damaged. Further reflections produced at the source-line interface caused by a signal dependent impedance can damage a CW source sensitive to such reflections.

9.2.2 Tasks and Milestones / Timeline / Status

(A) Demonstrate an ability of a CW excitation signal to reduce the source–line impedance mismatch effect on signal amplitude present in D-NLTLs when compared to pulsed excitation signal, first through simulations and then by validating the results experimentally using low voltage (LV) and high voltage (HV) prototypes.

(A1) Show the potential to improve source–line impedance mismatch in simulation (**Completed SEP21)**

(A2) Experimentally demonstrate a low voltage (LV) prototype receiving a CW input (**Completed SEP21**)

(A3) Compare measured results with simulation behavior (**Ongoing**)

(A4) Determine if there are improvements to system behavior if D-NLTL diodes are biased when receiving a CW input (**Ongoing**)

(A5) Demonstrate improvements to the source–line impedance mismatch in a LV prototype (**Ongoing**)

(A6) Demonstrate a high voltage (HV) prototype receiving a CW input (**Completed NOV21**)

(A7) Demonstrate improvements to the source–line impedance mismatch in a LV prototype

(B) Demonstrate UHF – L-band (0.3 – 2 GHz frequency) generation with a CW D-NLTL.

(B1) Excitation of K100F and K50F D-NLTLs using a 700 MHz signal from the R&S amplifier (**Completed NOV21**)

(C) Demonstrate UHF Generation at Single MW Power levels with a CW D-NLTL.

9.2.3 Progress Made Since Last Report

(A6 & B1) D-NLTLs based on high voltage epoxy diodes (models K100F and K50F) were sent excitation signals from a R&S amplification system. Each D-NLTL demonstrated frequency doubling of the 700 MHz signal, producing a signal with a frequency component of 1.4 GHz.

9.2.4 Technical Results

(A6 & B1) Two D-NLTLs based on high voltage epoxy diodes of model K50F and K100F were excited using a continuous sine wave signal of 700 MHz via a R&S amplifier. The resulting waveforms from each D-NLTL (shown in Fig. 9.2.1) demonstrated frequency doubling behavior, increasing signal frequency from 700 MHz to 1.4 GHz. However, significant signal attenuation is still observed in the generated signal of each D-NLTL. The amplifier produced a 87 W (66 V on a 50 Ω load) signal for the K50F line and 123 W (78 V on a 50 Ω) for the K100F line. With peak amplitudes of 2–4 V for both D-NLTLs, significant attenuation is still observed indicating little effect on the source line impedance mismatch. The signal attenuation can be partially explained by the low saturation provided by the sub 100 V signals produced by the R&S amplifier. At such amplitudes the average capacitance of the lines will be near the low signal junction capacitance of 35 pF, resulting in an average impedance of 10 Ω. To further test the ability of a CW to minimize the impedance mismatch at the source–line interface and amplitudes above 100 V will be required to ensure the average impedance is closer to 50 Ω.

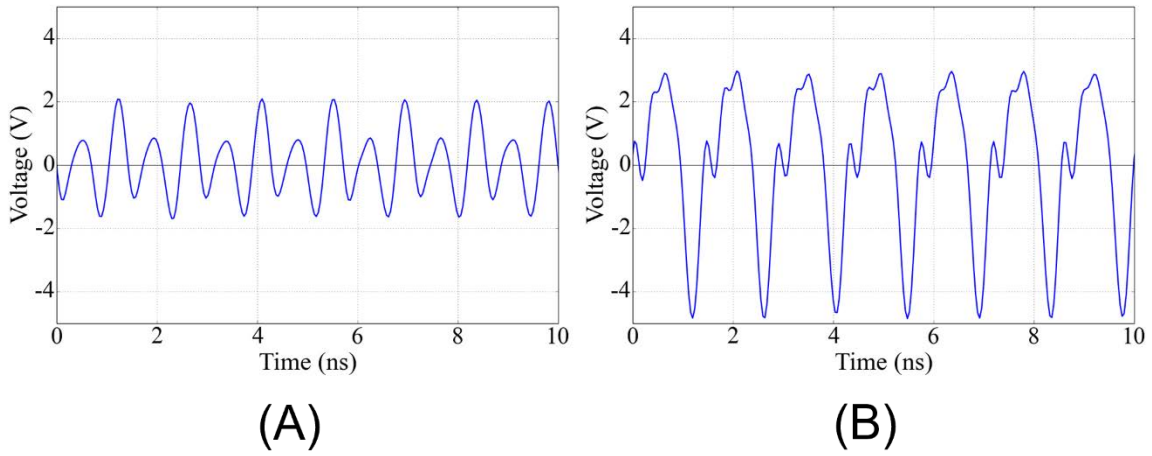

Figure 9.2.1. Continuous wave results for the K50F (A) and K100F (B) D-NLTLs. Each D-NLTL was fed a sine wave signal with a frequency of 700 MHz. Frequency doubling was observed in both D-NLTLs with a generated frequency of 1.4 GHz.

9.2.5 Summary of Significant Findings and Mission Impact

(A) In the month of September, a LV prototype was given several continuous waveforms to observe initial behavior of a D-NLTL with a CW source. The LV D-NLTL demonstrated a capability to receive a CW based source. No effect on the source–line impedance mismatch was observed for the LV tests. During the month of November two high voltage D-NLTLs based on epoxy diodes were tested using a sinusoidal waveform amplified by an R&S amplifier. Each D-NLTL demonstrated a capability to function with a CW source, however little to no effect was observed on the source–line impedance mismatch.

(B) Two high voltage D-NLTLs based on epoxy diodes of model K50F and K100F were tested using a 700 MHz sinusoidal signal amplified by an R&S Amplifier. Both D-NLTLs demonstrated frequency doubling behavior, producing a 1.4 GHz frequency in the generated waveform.

10 Antenna Development

10.1 Tradespace Analysis of an Array of Electrically Small Antennas (ESAs)

(Bidisha Barman and Deb Chatterjee)

10.1.1 Problem Statement, Approach, and Context

Primary Problem: Determine the extent to which the physical aperture size of an antenna array, composed of patch elements, can be reduced, while maintaining performance in peak power density, bandwidth, and electronic beam steerability over the UHF range (0.4–1 GHz), compared with present-art high-power-microwave-capable antenna arrays.

Solution Space: An array of patch antenna elements whose feed, two-dimensional shape, and relative placement (i.e., intra-, and inter-element design) allow for the physical aperture size to be reduced by more than 20% compared with the present-art.

Sub-Problem: To overcome scan blindness (as the main beam is electronically steered), due to the excitation of surface waves (SW). (Note: scan blindness is a common phenomenon in electrically small microstrip patch antenna arrays).

State-of-the-Art (SOTA): Horn, reflector, Vivaldi, valentine, etc. are some of the commonly used ultra-wideband (UWB) antenna elements in a phased array for high-power microwave (HPM) transmissions.

Deficiency in SOTA: Large physical aperture size of the antennas.

Solution Proposed: Using electrically small antennas (ESAs) as array elements and optimizing their performance in terms of both near-field (bandwidth) and far-field (directivity) parameters, followed by arrangement of the ESAs in suitable lattice structures (preferably, hexagonal/triangular) to reduce the overall array aperture area. Using stochastic and machine learning (ML) algorithms to optimize antenna element and array performance.

Relevance to OSPRES Grant Objective: Provides design and optimization guidelines for UWB ESA elements, especially coaxial probe-fed microstrip patch antennas, and arrays for HPM applications.

10.1.2 Tasks and Milestones / Timeline / Status

(A) Develop an Array Pattern Tool in the context of lightweight calculations of large antenna arrays / JAN–MAY 2021 / Completed code.

(B) Investigate the effects of array aperture area reduction on different array parameters (such as gain, beamwidth, electronic beam steerability) and present a comparative study of antenna array parameters as a function of array aperture area / JAN–MAY 2021 / Completed investigations of arrays on infinite ground planes.

(C) Build minimum viable validation prototypes of single ESA elements on substrates that have good power handling capabilities for HPM transmissions at UHF range (such as polyethylene, FR-4, TMM-10i, TMM-6) / JAN 2021–MAR 2022 / Completed fabrication and preliminary testing of a polyethylene-based narrowband ESA.

(D) Optimization of ESA (single element) performance using regular and ML based stochastic search algorithms / JUN 2021–JAN 2022 / Completed ML based bandwidth maximization study of a single ESA element; initiated multi-objective optimization of an ESA element.

(E) Build minimum viable validation prototypes for arrays of ESA elements / JUN 2021–OCT 2022 / Completed fabrication and preliminary testing of a 2×2 array of ESAs; fabrication of larger arrays to be initiated.

(F) Optimization of array performance using ML algorithms / SEP 2021–MAY 2022 / Ongoing.

10.1.3 Progress Made Since Last Report

(C) Build minimum viable validation prototypes of single ESA elements:

a. Manufactured and tested S_{11}-parameter and gain of a narrowband, coaxial probe-fed, microstrip patch, ESA element, on a polyethylene substrate.

b. While good agreement was achieved between the measured and the simulated S_{11}-parameters, discrepancies were observed between the measured and the simulated gain values.

(D) Optimization of ESA (single element) performance using ML algorithms:

a. Used Altair HyperStudy and MATLAB neural network toolbox to maximize the bandwidth of an ESA element via optimization of its design parameters.

(E) Build minimum viable validation prototypes for arrays of ESA elements:

a. Manufactured a 2×2 array of microstrip patch ESA elements (0.9–1 GHz) on a 6.35 mm thick TMM-10i substrate.

b. Tested the S_{11}-parameters of individual array elements with good agreement achieved between the measurements and simulation.

10.1.4 Technical Results

(C) Build minimum viable validation prototypes of single ESA elements:

<u>Design and characterization of UWB microstrip ESA elements at the UHF range:</u>

It has been shown, in earlier reports, that a simple coaxial probe-fed microstrip patch ESA element can yield ≥30% 2:1 VSWR bandwidth, by strategically placing the feed-probe along 2/3rd of the patch diagonal. One of the major requirements of such designs is that the feed-probe must have a radius, $r_p \geq 0.005\times$wavelength (where, wavelength is calculated at the center frequency f_c of the antenna's operating band). Therefore, at the desired UHF range (0.6–1.0 GHz) the probe radius must be: $r_p \geq 2$ mm. The commercially available SMA connectors are not suitable to feed the wideband, single layer, microstrip patch ESA designs at the UHF range, as they have $r_p = 0.65$ mm.

A solution to this problem is the use of 3D printed customized connectors (with $r_p \geq 2$ mm). Before manufacturing the customized connectors, it was decided to validate the design

approach, at the UHF range, using a standard, commercially available, SMA connector (r_p = 0.65 mm). For this purpose, a simple coaxial probe-fed microstrip patch antenna element was modeled, via FEKO and CST, on a 0.65-inch-thick polyethylene (dielectric constant = 2.3) substrate, at the upper UHF range (800-1000 MHz). As expected, due to smaller probe-radius (r_p = 0.65 mm), the antenna shows narrowband characteristics.

The antenna prototype has been manufactured, and its S_{11}-parameter and gain values are tested. Although good agreement has been achieved between the measured and simulated S_{11}-parameters, discrepancies were observed between the simulated and experimental gain data. This discrepancy may be attributed to multipath reflections from the surrounding walls and reflections from metal objects in the vicinity. Figure 10.1.1 shows the manufactured prototype of the polyethylene-based ESA element and its S11 and gain performances are shown in Figure 10.1.2.

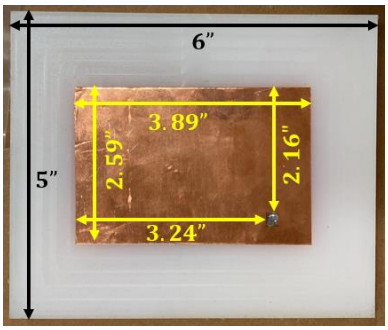

Figure 10.1.1. Manufactured prototype of the ESA on a 0.65-inch-thick polyethylene substrate.

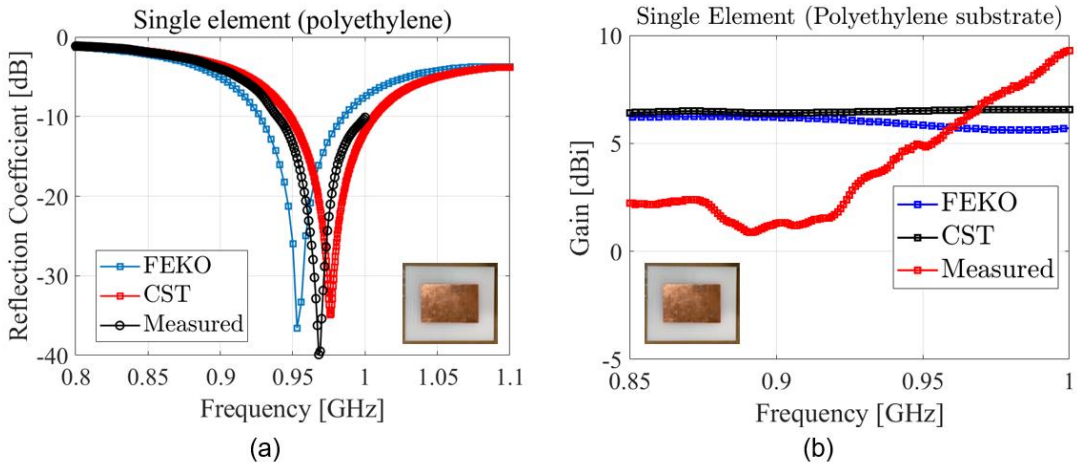

Figure 10.1.2. Simulated and measured (a) S_{11}-parameter and (b) gain of the ESA element on a 0.65-inch-thick polyethylene substrate.

(E) Build minimum viable validation prototypes for arrays of ESA elements:

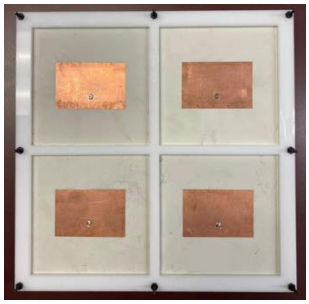

Figure 10.1.3. Manufactured prototype of the 2×2 array of narrowband, coaxial probe-fed, microstrip patch antennas, on 0.25-inch-thick TMM-10i substrates.

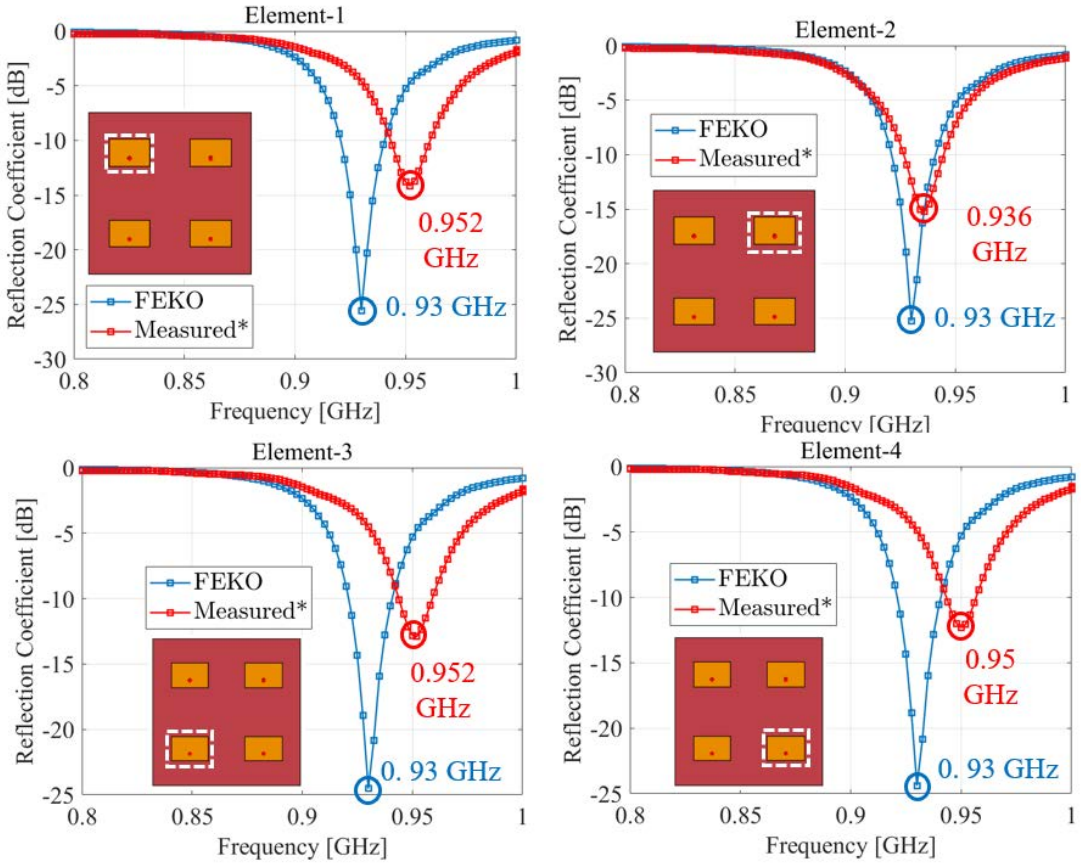

Figure 10.1.4. Comparison of the simulated and the measured S_{11}-parameters of the individual elements in the 2×2 array. In each case, the antenna elements, that are marked in white dotted lines, are excited, while all other elements are terminated in matched loads.

To experimentally validate the array design approach at the UHF range (0.6−1 GHz), a 2×2 array of single resonant microstrip patch antennas has been modeled to operate at ≈ 930 MHz, on a 0.25-inch-thick TMM-10i substrate (dielectric constant = 9.8). Like the single element validation approach, followed in (C), standard SMA connectors (r_p = 0.65 mm) have been used to feed the patches. The array prototype has been manufactured and its overall gain and individual element S_{11}-parameters were tested.

The manufactured prototype is shown in Figure 10.1.3. Due to unavailability of a single large (10”×10”) TMM-10i board, four ESA elements were fabricated on four separate and smaller boards (5”×5”), which were later attached side-by-side, using a plastic frame, to form the overall array architecture.

Very good agreement, between the measured and the simulated S_{11}-parameters of the individual array elements has been achieved, as shown in Figure 10.1.4. The disagreement between the measured and the simulated gain values, as shown in Figure 10.1.5, is due to the same reasons, as discussed in (C).

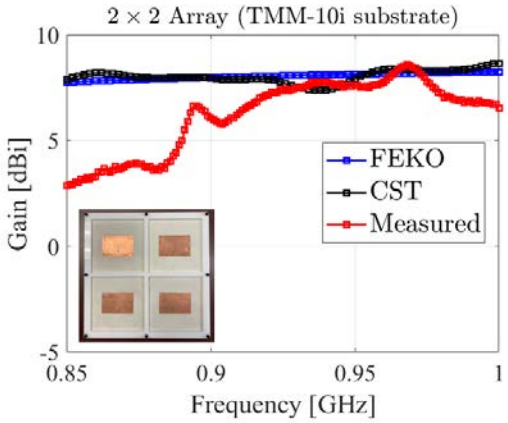

Figure 10.1.5. Comparison of the simulated and the measured array gain.

Future work involves accurate gain, radiation pattern, and time-domain testing of the single ESA element and the array, followed by manufacturing of a 4×4 array, composed of wideband ESA elements, operable in the UHF region.

10.1.5 Summary of Significant Findings and Mission Impact

(A) Developing Array Pattern Tool for large arrays calculations:

A MATLAB code has been developed for faster approximation of the radiation pattern of a linear/planar array of any size and composed of any type of antenna elements. The code requires the center element pattern of a small array (say, 3×3) composed of the same type of antenna elements, desired lattice arrangement, and total number of array elements, as user inputs. This work will be included in future publications.

(B) Investigate the effects of array aperture area reduction on different array parameters:

The effect of different array aperture area and lattice arrangements on the array parameters (such as array gain, beamwidth, electronic beam steerability, etc.) have been reported for arrays modeled on infinite ground planes (DEC 2020 ONR-OSPRES-Grant MSR). The results show that, with 30% reduction in the aperture area ($\approx 50\%$ reduction in # of elements), the gain drops by < 3.5 dBi without any scan blindness spotted as the main beam is steered from boresight to $\pm 60°$ in the $640-990$ MHz range.

The array parameters for large arrays ($\geq 15 \times 15$) on finite ground planes could not be computed using the commercial EM solvers (FEKO and CST) due to excessive memory and time consumption. This work will be resumed after developing a method to estimate array performances on finite ground planes, either through ML or conventional approaches.

(C) Build minimum viable validation prototypes of single ESA elements:

Investigated different bandwidth enhancement techniques applicable to single layer microstrip patch ESAs:

a. Method I: Bandwidth enhancement by strategically placing the coaxial probe along 2/3rd of the patch diagonal – This method is proposed and experimentally validated using prototypes manufactured on TMM-6 and TMM-10i substrates at $2.5-5$ GHz. Antennas have been modeled on various substrates (polyethylene, G10/FR-4, TMM-10i) at the UHF range ($0.6-1$ GHz) and are being considered for manufacturing.
b. Method II: Coaxial probe-fed U-slot loaded rectangular microstrip ESAs – A prototype is manufactured on a G10/FR-4 substrate ($0.9-1.3$ GHz) and tested.
c. Method III: L-probe-fed U-slot-loaded rectangular microstrip ESAs – An antenna has been modeled on a TMM-4 substrate that operates in the $0.52-1.17$ GHz range ($\approx 77\%$ 2:1 VSWR bandwidth). Due to the fabrication complexity of the L-probe proximity coupled feed, this antenna will not be manufactured.

(D) Optimization of ESA (single element) performance using regular, and ML based stochastic search algorithms:

Investigated the bandwidth enhancement of the coaxial probe-fed microstrip patch antennas, using regular and ML based stochastic search algorithms (GA, PSO, and Simplex methods), by optimizing the feed-probe location and ground plane shape and size. Compared to regular search algorithms, ML algorithms are found to be less computationally intensive (in terms of time and memory consumption).

(E) Build minimum viable validation prototypes for arrays of ESA elements:

A wideband 3×3 array (2.5-5 GHz) and a narrowband 2×2 array (900 MHz), of coaxial probe-fed microstrip patch ESA elements, on 0.25-inch-thick TMM-10i substrates, have been manufactured. The S11-parameters of the individual elements, in each array prototype, have been tested, with good agreement achieved between the simulated and the measured data. We have initiated modeling and characterization of a 5×5 square and a 17-element hexagonal array of wideband ESA elements for future prototyping.

(F) Optimization of array performance using ML algorithms:

Initiated investigations into the reduction of mutual coupling between individual elements in a small array (5×5) by seeking the best inter-element spacing using radial basis function algorithm.

10.2 Tradespace Analysis of Ultra-Wide-Band (UWB) Koshelev Antenna

(Alex Dowell and Kalyan Durbhakula)

10.2.1 Problem Statement, Approach, and Context

Primary Problem: Determine the extent to which the physical aperture area of an antenna array, composed of antenna elements, can be reduced, while maintaining performance in peak power density, bandwidth, and electronic beam steerability over the UHF range (0.4–1 GHz), compared with present-art high-power-microwave-capable antenna arrays.

Solution Space: The Koshelev antenna has a unique design that is capable of generating an UWB response by effectively merging radiation characteristics from a transverse electromagnetic (TEM) horn antenna with exponentially tapered flares, an electric monopole, and magnetic dipoles over a wide frequency range [1]. This opens up an opportunity to investigate the design parameter space and understand parameter effects on impedance bandwidth, radiation pattern, electric field distribution, and other metrics via a tradespace study.

Sub-Problem:

(i) The integration of an impedance transformer to a single element Koshelev antenna to simulate and test the combined (transformer–antenna) performance is currently not feasible using commercial EM simulators.

(ii)The total surface currents on the Koshelev antenna over the desired frequency range arising from the present positioning of TEM exponential flares, an electric monopole, and magnetic dipoles is not yet clearly understood.

State-of-the-Art (SOTA): The balanced antipodal Vivaldi antenna (BAVA) is considered to be the SOTA antenna element due to its exceptional 20:1 impedance bandwidth ratio as well as the ability to handle tens-of-MW input power.

Deficiency in the SOTA: The BAVA design parameter space has been exhausted over the past couple of decades. The physical aperture area still remains very large and there is no viable path through tradespace study for further physical aperture area reduction.

Solution Proposed: Design, simulate, validate, and perform a tradespace study on the important design parameters of the Koshelev antenna array that effectively reduce its physical aperture area while maintaining its UWB properties, in both the frequency and time domains. The Koshelev antenna has been shown in the literature to withstand higher voltage levels (over 200 kV peak voltage), thereby making it a viable antenna element for detailed tradespace study and analysis.

Relevance to OSPRES Grant Objective: From the literature, it was shown that the Koshelev antenna can handle high input voltages (and therefore high power with 50 Ω input impedance), which satisfies the specific OSPRES objective related to high input voltage/power. In addition, this work can yield a center-frequency-dependent, bandwidth-controlled, and electronically steerable Koshelev antenna design that can be quickly modified to the spectrum properties of the ultra-fast rise time input pulse.

Risks, Payoffs, Challenges:

(i) The electrical size of the Koshelev antenna is approximately λ/4 at its lowest operating frequency. Further reduction of electrical size to λ/10 could considerably reduce frequency dependent gain, thereby decreasing the power spectral density.

(ii) Payoffs include the development of a library of antenna metrics data for different shapes and sizes of the individual parts within the Koshelev antenna.

(iii) The large electrical size (>5λ) of the Koshelev antenna at its highest operating frequency poses huge computational challenges.

10.2.2 Tasks and Milestones / Timeline / Status

(A) Complete literature search to identify and list antenna elements that satisfy UWB properties and HPM requirements, and down-select accordingly / NOV–DEC20 / Complete.

(B) Complete initial design, simulation, and validation of Koshelev antenna [1] / JAN21 / Complete.

(C) Perform a preliminary parameter study to identify design parameters that considerably reduce the physical aperture area / FEB–MAR21 / Complete.

- Milestone: Using FEKO and/or CST electromagnetic (EM) simulators, reduce the physical aperture size of the Koshelev antenna to at least 95% of its original design and show minimal to no variation in the bandwidth, gain and increased aperture efficiency / Complete.

(D) Determine the full-width half-maximum (FWHM) and ringing metrics from the envelope of the time domain impulse response ($h_{rx/tx}(t, \phi, \theta)$) in receive or transmit mode / MAR–APR21 / Complete.

- Milestone: Produce a generalized code that calculates the impulse response envelope of the Koshelev antenna and plots the rate of change in FWHM and ringing values as a function of physical aperture size.

(E) Perform tradespace studies on design parameters such as feed position (*F*), length (*L*), and alpha (α). Obtain various antenna metrics data, compare, and analyze / MAR21/ Complete.

- Milestone: Identify Koshelev antenna design parameters that significantly alter the bandwidth, rE/V, peak gain over the desired bandwidth, and aperture efficiency.

(F) Reduce Koshelev antenna aperture size (H×W) to equal to or less than 90 mm × 90 mm, equal to that of the SOTA BAVA, for direct antenna metrics comparison / MAR–APR21 / Complete.

- Milestone: Provide a recommendation on the optimum design parameters and the resulting metrics, with comparison to SOTA BAVA. The optimized design parameters must yield 900 MHz ± 200 MHz bandwidth, rE/V greater than 1, peak gain around 3 dBi at 900 MHz, aperture efficiency equal to or greater than 130% at 900 MHz.

(G) Using the optimized model from (F), build various array simulation models/topologies to perform a tradespace study and report tradeoffs between array antenna metrics such as center element reflection coefficient (S11) value, gain vs theta at constant phi, physical aperture area, aperture efficiency, and rE/V / MAY–JULY21 / Complete.

- Milestone: Develop/showcase an optimized Koshelev array model that exceeds an aperture efficiency of 130% with a high rE/V.

(H) Perform literature search to investigate, understand, and determine the applicability of special electromagnetic (EM) techniques to the antennas under consideration. / JAN–APR21 / Complete.

(I) Explore impedance taper (microstrip based and coax based) designs that can interface well (both mechanically and electrically) to transition the signal from a coax cable to the input of the Koshelev antenna element / JULY21–AUG21 / Complete.

- Milestone: Recommend the optimum impedance taper design (with minimum reflections and maximum power transfer) with the optimum dimensions to successfully convert the high-voltage, short-rise time input signal from a coax cable to the feed of the Koshelev antenna array.

(J) Study response from optimized Koshelev antenna array when excited with different monopolar, differential, and bipolar pulse signals of significant interest / AUG21–NOV21 / Ongoing.

- Milestone: Provide a table comparing the Koshelev antenna array response metrics and narrow down the suitable pulse signals. Recommend (if any) changes to the downselected pulse signal(s) that can further improve the radiation efficiency, and/or transient gain.

(K) Prototype single element Koshelev antenna and test for reflection coefficient, gain as a function of frequency, radiated electric field at 1-m, 2.5-m, 5-m and 10-m (if feasible) distances. / AUG21–DEC21 / Ongoing.

- Milestone: Report measured data and recommend any improvements to the fabrication/prototyping/testing methods.

10.2.3 Progress Made Since Last Report

(J) Six different high-voltage pulse waveforms were considered to study the response from the optimized Koshelev antenna. All 6 pulse waveforms considered were monopolar (unipolar) in nature which were taken directly from the measurements (except for DSRD 4x2) or recreated from manufacturer’s datasheet. The 6 pulse waveforms were studied individually and were distributed equally to all elements in the optimized Koshelev antenna array. The 6 pulse waveforms with proper legend are shown in Fig. 10.2.1.

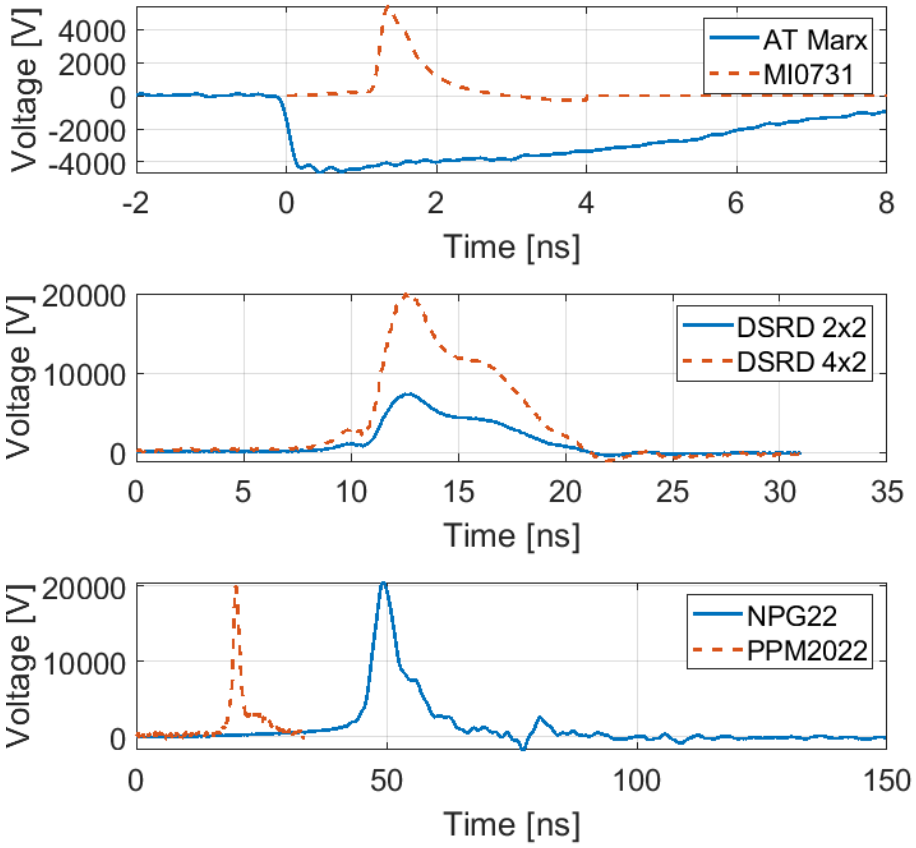

Figure 10.2.1. Six monopolar pulses (AT Marx, MI0731, DSRD 2x2, DSRD 4x2, NPG22, and PPM2022) fed to the Koshelev antenna array.

(K) The Koshelev antenna's, 2-part 1mm thick, frame was 3D printed in PLA plastic. Each half was metallized by applying copper foil with adhesive backing; they were then connected to each other with epoxy. More copper foil was applied to the inside and the outside of the rear wall to cover the seam between the two halves. Holes were drilled in the rear section of the transformer, then a female N-Type connector was attached with nylon screws and solder. Nearly RF transparent foam was cut and placed in the hallow sections of the antenna to improve structural integrity. Initial testing is scheduled 12/17/2021.

(a) (b) (c)

Figure 10.2.2. 3D printed and metallized single element Koshelev antenna with an integrated impedance transformer and a N-type connector.

10.2.4 Technical Results

(J) We have studied the electric field response from the optimized Koshelev antenna array (diamond topology) at 10 meters, which is determined to be the far field. The study has been carried out in time-domain and the frequency spectrum has also been computed. Each element in the antenna array is fed equally with the pulses shown in Fig. 10.2.1. The pulses in Fig. 10.2.1 have different peak voltage, full-width half-maximum (FWHM) and rise time. The values are provided in Table 10.2.1.

Table 10.2.1. Pulse source waveform properties.

Pulse Source	Peak Voltage [kV]	FWHM [ns]	Rise Time [ns]
AT Marx	4.2	5.8	0.2
MI0731	6.2	0.4	0.15
DSRD 2x2	7.35	5.48	0.57
DSRD 4x2	20	2.78	0.57
NPG22	20	5.35	4.4
PPM2022	20	1.5	1.55

ATMarx, MI0731, and DSRD 2x2 have peak voltages of 4.5 kV, 6.2 kV, and 7.35 kV, respectively. On the other hand, DSRD 4x2, NPG22 and PPM2022 have peak voltages of 20 kV each. The full-width half-maximum of all the pulses are also different. Note that the pulse study for each pulse was done separately, i.e., all elements were fed with AT Marx pulse equally and no mix and match technique was employed. Fig. 10.2.3 shows the time-domain electric field response at 10 m. The E-field response between different pulse waveforms can be clearly noticed in Fig. 10.2.3. The response from feeding

'ATMarx' and 'MI0731' looks eerily similar from the Fig. 10.2.3, however that is not enough to draw any conclusions. Similarly, the response from 'DSRD 2x2' and 'DSRD 4x2' appears to be same except for the peak electric field. On the other hand, the response from 'NPG22' is relatively low in peak electric field when compared against the response from 'PPM2022'. To understand these results quantitatively, the peak-to-peak electric field, rE/V (transient gain) and energy density were computed and compared in Table 10.2.2.

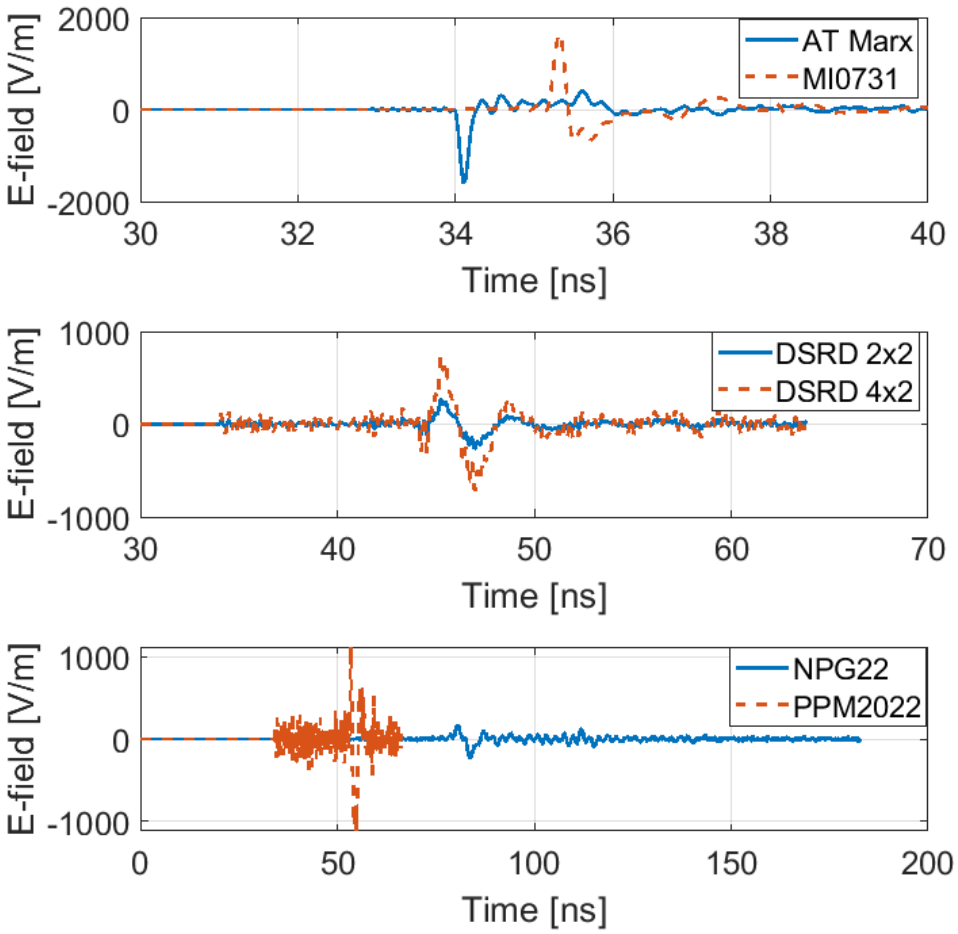

Figure 10.2.3. Radiated electric field at 10 meters distance from the antenna array aperture when fed with different monopolar pulse source signals/waveforms.

Table 10.2.2. Diamond Koshelev antenna array response with different pulse source waveforms at 10 meters distance.

Pulse source	Epeak [kV/m]	rE/V	Ed [uJ/m2]
AT Marx	1.6	3.8	0.9
MI0731	1.64	3.1	1.46
DSRD 2x2	0.27	0.36	0.2
DSRD 4x2	0.74	0.36	2.15
NPG22	0.17	0.08	0.4
PPM2022	1.12	0.56	6.25

In addition to the time-domain results, it is equally important to compute, plot and analyze the frequency spectrum of the time-domain electric field. Fig. 10.2.4 shows and compares the frequency spectrum of the time-domain electric field radiated at 10 m distance from the aperture of the antenna array. Some interesting observations can be noticed. The Koshelev antenna has been designed to work from 500 MHz and upwards, however, that does not indicate that the antenna does not work below 500 MHz. The antenna can still radiate signals below 500 MHz, although not very effectively. From Fig. 10.2.4 we can notice that the frequency spectrum of the antenna array from feeding the ‘DSRD 2x2’, ‘DSRD 4x2’, ‘NPG22’ or ‘PPM2022’ lie below 500 MHz because of their extremely short rise time and long FWHM. On the other hand, the frequency spectrum of the antenna array from feeding either ‘ATMarx’ or ‘MI0731’ has frequency content around 900 MHz and some below 500 MHz. It is also clear that between ‘AT Marx’ and ‘MI0731’, the pulse source ‘MI0731’ yields the highest frequency content. This confirms that it is ideal to use the ‘MI0731’ pulse waveform in conjunction with the optimized Koshelev antenna array.

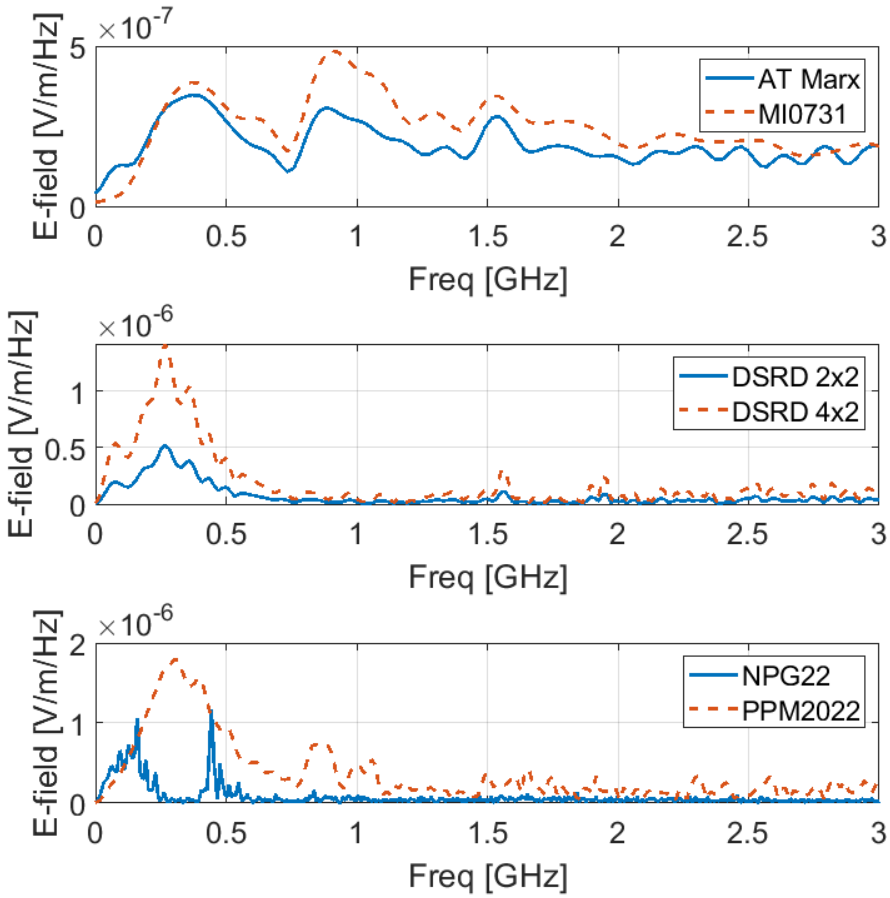

Figure 10.2.4. Frequency spectrum of the radiated electric field at 10 meters distance from the antenna array aperture when fed with different monopolar pulse source signals/waveforms.

10.2.5 Summary of Significant Findings and Mission Impact

(A) An extensive literature search on various UWB antenna elements has resulted in finding three promising options. The down-selected elements are the Koshelev, Shark, and Fractal antennas, which will be extensively studied using their individual design parameter space, which could result in physical aperture area reduction of the single antenna element. Later, the single antenna element will be converted into a planar array.

(B) Initial validation of the Koshelev antenna simulated using CST software agreed well with the antenna metrics published in the open literature [1]. A UWB bandwidth response (10:1 bandwidth) and rE/V > 1 has been observed from our initial simulations of the Koshelev antenna. This validation ensured that the Koshelev antenna can be subjected to further tradespace studies to understand its performance followed by optimizing the design according to OSPRES grant requirements.

(C) The initial tradespace study and analysis of the Koshelev antenna design yielded promising outputs to carry forward the investigation. A comparison of important antenna metrics between the Koshelev antenna in [1] and aperture reduced Koshelev antenna are shown in Table 5.2.1 of the APR 21 MSR.

(D) An in-house code has been developed to calculate important UWB time domain antenna metrics such as full-width half maximum (FWHM) and ringing. These metrics have been calculated using in-house MATLAB code using the excitation voltage and radiated electric field information obtained from CST simulations. FWHM and ringing antenna metrics help with assessing or characterizing an antenna's UWB response.

(E) The tradespace study of feed position provided a deeper understanding of how its position impacts the S11 value bandwidth. An optimum value for feed position i.e., $F = 1/20 < L < 1/10$ is recommended to achieve maximum bandwidth. The tradespace study of the antenna length (L) is straightforward. A longer antenna length will radiate better at lower frequencies. However, physical size restrictions/requirements must be kept in mind in determining the antenna length. Finally, a larger α value (>120°) is recommended to avoid unnecessary reflections from the electric monopole.

(F) From a thorough tradespace study, the aperture size of the Koshelev antenna (single element) is determined to be 90 mm × 100 mm in order to achieve desired antenna metrics performance proposed in the milestone. All metrics described in the milestone have been successfully achieved except the desired bandwidth (200 MHz on both sides) at 900 MHz center frequency. The bandwidth achieved is 900 ± 100 MHz.

(G) The physical aperture area of the Koshelev array antenna largely depends on the interelement spacing and the shape of the array. We were able to determine that the diamond topology is the optimum shape for the Koshelev array antenna. We were also able to obtain similar gain profile (peak gain and pattern) from making certain elements within the array passive (off state) when compared against regular active array (all elements in on state). From the non-symmetric interelement spacing values, we found that S_y has the least effect on the output; therefore a small spacing value can be chosen to reduce the physical aperture area of the Koshelev array.

(H) The literature search on the special EM techniques expanded our knowledge and opened the door to opportunities to apply some of those techniques to the antennas under study. EM techniques such as non-symmetric and non-square array topologies have been applied to the development and study of the Koshelev array antenna.

(I) The first impedance taper design under consideration has shown good S11 values (< -10 dB) over the frequency range of interest. In addition, we have shown that the shape of the pulse can be easily retained at the output of the taper with less than 5% amplitude losses.

(J) The Koshelev antenna array response from feeding a monopolar vs bipolar signal has demonstrated a clear winner: that is, a bipolar signal will radiate at least 10 times better than a monopolar signal. A comparison of the frequency spectrum of the radiated electric field from the optimized Koshelev antenna array between different monopolar pulse sources has identified the 'MI0731' pulse to be the optimum pulse.

10.2.6 References

[1] Gubanov, V. P., et al. "Sources of high-power ultrawideband radiation pulses with a single antenna and a multielement array." *Instruments and Experimental Techniques* 48.3 (2005): 312-320.

10.3 Tradespace Analysis of Ultra-Wide-Band (UWB) Shark Antenna

(Kasey Norris and Kalyan Durbhakula)

1.1.1 Problem Statement, Approach, and Context

Primary Problem: Determine the extent to which the physical aperture area of an antenna array, composed of antenna elements, can be reduced, while maintaining performance in peak power density, bandwidth, and electronic beam steerability over the UHF range (0.4–1 GHz), compared with present-art high-power-microwave-capable antenna arrays.

Solution Space: An array of Shark antenna elements with an emphasis on inter-element and intra-element spacing effects is a good candidate for UWB HPM systems while having a reduced aperture area with respect to the current state-of-the-art. In the literature, the Shark antenna has already been shown to achieve a wide 20:1 impedance bandwidth, low dispersion, and a sectoral (also referred to as directional) radiation pattern.

Sub-Problem: The design parameter space of the Shark antenna has not been studied rigorously in the literature and therefore the effect of these parameters on the antenna metrics is not understood. In addition, the Shark antenna has been shown to be not very directive in the H-Plane. Preliminary studies have shown that aperture efficiencies at low frequencies are much better than at higher frequencies.

State-of-the-Art (SOTA): The balanced antipodal Vivaldi antenna (BAVA) is considered to be the SOTA antenna element due to its exceptional 20:1 impedance bandwidth ratio as well as the ability to handle tens-of-MW input power.

Deficiency in the SOTA: The BAVA design parameter space has been exhausted over the past couple of decades. The physical aperture area still remains very large and there is no viable path through tradespace study for further physical aperture area reduction.

Solution Proposed: Explore the array tradespace by generating different array topologies/lattices (hexagonal, octagon, square, elliptical) and with different intra and interelement spacing combinations.

Relevance to OSPRES Grant Objective: The Shark antenna dimensions were established to be frequency dependent and can be readily modulated to fit the spectrum characteristics of an ultra-fast rise time input pulse.

Risks, Payoffs and Challenges:

(i) The Shark antenna is comprised of flare-angle-dependent bicones that are truncated in the azimuthal angle. This still yields considerably higher half power beam width

(HPBW) than other antenna elements under investigation. The significant reduction of HPBW in the H-plane may be unattainable and can be considered a major risk.

(ii) Payoffs include the development of a library of antenna metrics data for various shapes and sizes of the bicones and reflector plates in the shark antenna.

(iii) Computational challenges remain present with respect to automation of design parameter space on our currently used supercomputer (LEWIS). Design challenges persist in obtaining lower operating frequencies while not increasing the height of the antenna and surpassing the 90 mm × 90 mm size requirement.

10.3.1 Tasks and Milestones / Timeline / Status

(A) Complete initial design, simulation, and validation of the Shark antenna / JAN21 / Complete.

(B) Validate Shark antenna design using the LEWIS supercomputer over a wider range of frequency results (up to 20 GHz) / FEB–MAR21 / Complete.

(C) Identify Shark antenna design parameters which contribute significantly to bandwidth, gain, and physical aperture area. Determine which parameters contribute most to performance improvement/size reduction/ FEB–MAR21 / Complete.

(D) Perform a tradespace study by simulating the Shark antenna with varying cases of flare angle, cone length, and distance to backplane. Gain a general understanding of how these parameters affect impedance bandwidth, rE/V, gain and HPBW / FEB–MAY21 / Complete.

- Milestone: produce a detailed summary of change in impedance bandwidth, rE/V, HPBW in H-plane and E-plane as a function of flare angle (α), cone height (h), and distance to backplane (d) / Complete.
- Milestone: Choose optimal Shark antenna design that has the lowest operating frequency within size requirements based on tradespace study / Complete.

(E) Using the optimal Shark antenna design in (D), simulate various array geometries including hexagonal, rectangular, and circular arrays. Determine which array geometries are optimal and analyze aperture fields and aperture efficiencies. Further study the effect of different time-domain waveforms in the far-field radiated by the optimized Shark antenna array / MAY–NOV2 / Ongoing.

- Milestone: Produce a report which states the effects of various array geometries for the Shark antenna. The optimal array geometry chosen should have the least interference between elements, therefore yielding higher impedance bandwidth and higher aperture efficiency. Overall, the optimal Shark array geometry should have at least 20% impedance bandwidth at 900 MHz center frequency for the centermost element with 130% array aperture efficiency, ± 60 degrees beam steering capability, and rE/V equal to or greater than 4. Identify a waveform that combines well with the optimized Shark antenna array in terms of peak electric field, rE/V, and energy density.

(F) Begin prototyping and validation of optimal Shark antenna single element. / JUN–OCT21 / Ongoing.

- Milestone: Have a finished Shark antenna prototype. Compare S11 and radiation pattern with simulated Shark antenna.

10.3.2 Progress Made Since Last Report

(E) The optimized Shark antenna array topology i.e., the elliptical topology has been subjected to 6 different pulse source waveforms. These waveforms and their time-domain properties were shown in Table 10.2.1.

(F) The cones of single element Shark antenna are fabricated using 3D printing technology and later metallized is shown in Fig. 10.3.1. While the reflector is cut out of an aluminum sheet, the cones are 3D printed and metallized with nickel paint. A tapered coax transformer has been inserted into the coax cable to transform the impedance from 50 ohms to 150 ohms.

Figure 10.3.1. 3D printed and metallized prototype of single element Shark antenna.

10.3.3 Technical Results

(D) The elements in the elliptical Shark antenna array were inputted with 6 different pulse source waveforms and the time-domain electric field at 10 m distance is calculated for all waveforms. In the case of the Shark antenna array, we found that designing a shared reflector (instead of separate/individual reflectors) for all elements in an antenna array would help with improved gain (by at least 1 dBi beyond 10 dBi) at 900 MHz. The Shark elements in the antenna array were equally fed with those waveforms mentioned in Table 10.2.1 and the radiated time-domain electric field at 10 m is shown in Fig. 10.3.2. The observations noticed in the case of Koshelev antenna array can also be noticed here in the case of the Shark antenna array. In Fig. 10.3.2, we can differentiate the electric field response when fed with an ‘AT Marx’ vs. ‘MI0731’. The response from feeding a ‘MI0731’ waveform appears to have more shorter time period as well as slightly higher peak field values. In the case of DSRD, no significant pulse shape deviation can be noticed besides the difference in peak field value, which is expected. Finally, ‘NPG22’ is the least favorable waveform to use because of its extremely slow rise time and wide FWHM. Table 10.3.1 shows some quantitative comparisons in terms of peak field value, rE/V, and energy density.

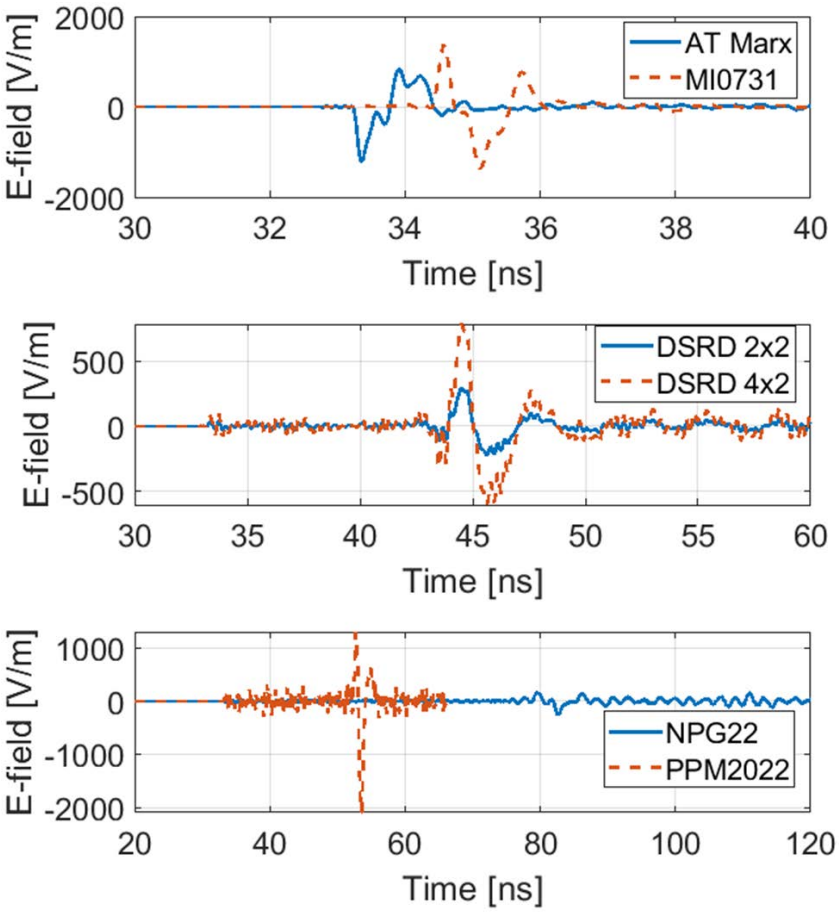

Figure 10.3.2. Radiated electric field at 10 meters distance from the antenna array aperture when fed with different monopolar pulse source signals/waveforms.

Table 10.3.1. Elliptical Shark antenna array response with different pulse source waveforms at 10 meters distance.

Pulse source	Epeak [kV/m]	rE/V	Ed [uJ/m2]
AT Marx	1.2	2.6	1.26
MI0731	1.3	2.5	2.33
DSRD 2x2	0.3	0.4	0.31
DSRD 4x2	0.78	0.4	2.25
NPG22	0.16	0.08	0.54
PPM2022	1.3	0.6	9.1

The frequency spectrum of the radiated time-domain electric field is also shown in Fig. 10.3.3. The comparison of frequency spectrum shows that 'MI0731' as the right choice to radiate fields at around 900 MHz while all others have fields relatively at lower frequency values than 900 MHz. It is important to emphasize and improve on the 'MI0731' waveform properties to further improve the electric field in the far-field.

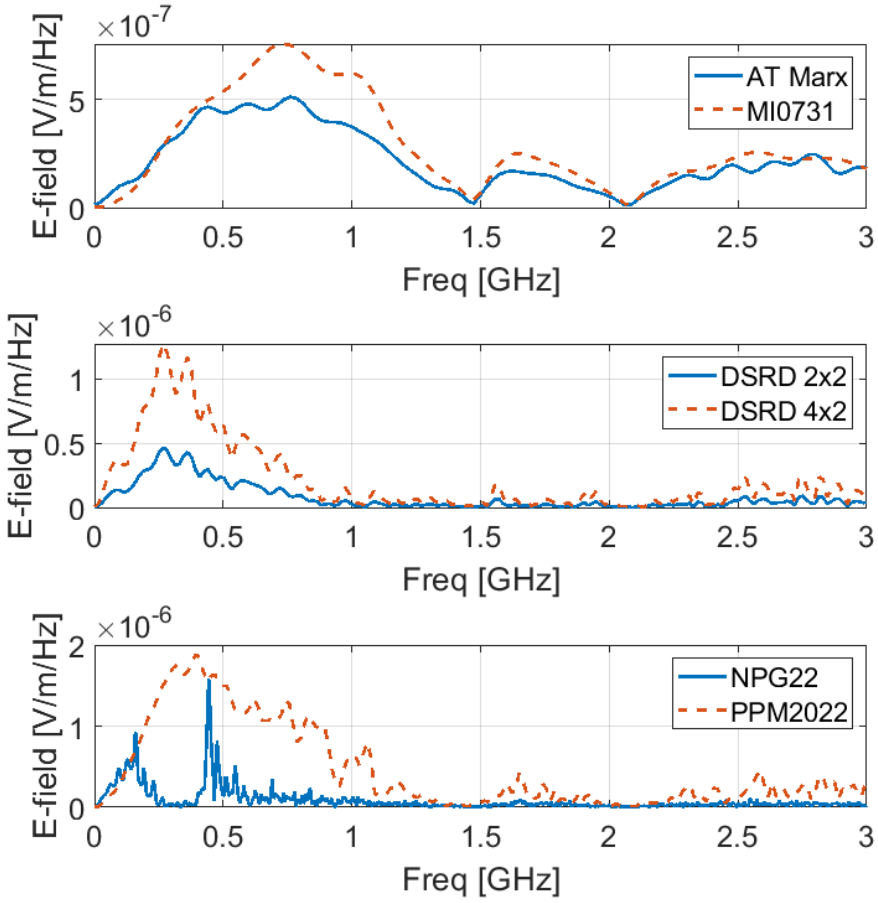

Figure 10.3.3. Frequency spectrum of the radiated electric field at 10 meters distance from the antenna array aperture when fed with different monopolar pulse source signals/waveforms.

10.3.4 Summary of Significant Findings and Mission Impact

(A-B) The Shark antenna has been designed, simulated, and validated according to [1]. (Figure 6.3.1)

(C) The Shark antenna design parameters that have been found to contribute significantly to bandwidth performance, directivity, and gain are the cone height (*h*) and distance to backplane (*d*).

(D) The Shark antenna tradespace study has been completed and has provided insight into the Shark antenna design space. Increasing the cone height *h* yields better

impedance bandwidth at low frequencies and is more directive in the *e* and *h* planes. However, increasing *h* results in a larger aperture area. To remain within 90 x 90 mm, the maximum *h* value is 45 mm; with this a lowest operating frequency of 815 MHz is achievable.

(E) The elliptical Shark antenna has the optimum metrics, which can be found in Table 6.3.1 in July 2021 MSR. The metrics from elliptical Shark antenna are closer to desired metrics provided in milestone 6.3.2 (E). The interelement spacing variable study has provided insight into the workings of Shark antenna array. The Shark antenna array is more sensitive to the interelement spacing variable in x-axis than in the y-axis. The elliptical topology has significantly smaller sidelobe level values and similar frequency-domain gain or transient gain values when compared against square and hexagonal topologies. If the input is a monopolar signal, a hexagonal or an elliptical topology is preferred. If the input is a bipolar signal, an elliptical topology is recommended for its decent transient gain value with significantly smaller sidelobe levels.

10.3.5 References:

[1] L. Desrumaux, A. Godard, M. Lalande, V. Bertrand, J. Andrieu and B. Jecko, "An Original Antenna for Transient High Power UWB Arrays: The Shark Antenna," in IEEE Transactions on Antennas and Propagation, vol. 58, no. 8, pp. 2515- 2522, Aug. 2010, doi: 10.1109/TAP.2010.2050418.

10.4 Machine Learning Inspired Tradespace Analysis of UWB Antenna Arrays

(Sai Indharapu and Kalyan Durbhakula)

10.4.1 Problem Statement, Approach, and Context

Primary Problem: Determine the extent to which the physical aperture area of an antenna array, composed of antenna elements, can be reduced while maintaining performance in peak power density, bandwidth, and electronic beam steerability over the UHF range (0.4–1 GHz), compared with present-art high-power-microwave-capable antenna arrays.

Solution Space: Fractal antennas possess exceptional fidelity factor values (>0.9), which describe how well the shape of the input pulse is retained at an observation point in the far-field. Their high degree of freedom provides an opportunity to develop systematically modified patch shapes, which in turn leads to improved bandwidth while retaining high fidelity factor values. Machine learning (ML) can be leveraged to predict the antenna array response for an arbitrary design parameter space upon sufficient training and validation.

Sub-Problem:

(i) Fractal antennas generate omni-directional radiation patterns in the H-plane over the desired frequency range.

(ii) ML can suffer from underfitting or overfitting the training model which in turn leads to deviations in the predicted output.

State-of-the-Art (SOTA): Conventional full-wave EM solvers such as method of moments (MoM), multi-level fast multipole method (MLFMM), finite element method (FEM), and finite difference time domain (FDTD) method are currently being used to study, analyze and assess the performance of UWB antennas.

Deficiency in the SOTA: UWB antenna optimization using conventional EM solvers utilizes significant computational time and memory resource.

Solution Proposed:

(i) Design, simulate, validate, and perform a tradespace study on the design parameter space of the selected fractal antenna element using commercially available electromagnetic (EM) wave solvers.

(ii) Train, validate, test and compare multiple ML models for quicker and accurate prediction of antenna array response for different physical aperture areas.

Relevance to OSPRES Grant Objective: The fractal antenna achieves an UWB response, a mandatory requirement of the OSPRES grant objective, in a small volume footprint and similar physical aperture area when compared against the SOTA BAVA, dual ridge horn antennas etc. Furthermore, the microstrip-design-based fractal antenna can efficiently handle electronic steering by integrating the feed network on the same board. This eliminates the need to build a separate feed network external to the fractal antenna using bulky coaxial cables.

Risks, Payoffs, and Challenges:

(i) A majority of the fractal antenna geometries yield an omni-directional pattern in the H-plane, which can be a risk. However, efforts are underway to mitigate this pattern without deteriorating bandwidth.

(ii) Payoffs include developing a library of antenna metrics data for various fractal shapes and sizes.

(iii) Design challenges and numerical calculations with respect to specific fractal shapes could arise after performing a certain number of iterations to further improve the bandwidth.

(iv) Fractal antennas were known to generate gain loss at random frequencies over their operating frequencies. Achieving gain stability over the desired frequency range can be a significant challenge.

10.4.2 Tasks and Milestones / Timeline / Status

(A) Perform tradespace analysis of the fractal element radius *b* over the desired frequency range (4 to 12 GHz) using the genetic algorithm (GA) optimization tool available in the commercial electromagnetic (EM) solver FEKO / FEB21 / Complete.

- Milestone: Provide a recommendation of an optimum value of *b* using OPTFEKO to minimize reflection coefficient or S11 (< –10 dB).

(B) Perform tradespace study on different fractal shapes by changing the number of fractal segments to understand the effect of this change on the impedance bandwidth / FEB21 / Complete.

- Milestone: Produce a detailed study of the antenna response such as S11, gain, and bandwidth by varying the number fractal segments.

(C) Apply the GA optimization tool on the fractal side length *b* over a wide frequency range (2 to 12 GHz with 201 discrete frequency points) and number of fractal segments using OPTFEKO on the LEWIS cluster / MAR21 / Complete.

- Milestone: Reduce physical aperture area by 10% of its present design, reported in the FEB MSR, and demonstrate minimal or no change in S11, gain, and fidelity factor values.

(D) Perform a parametric study and analysis of antenna response by varying hexagon radius, *a* / MAR–APR21 / Complete.

- Milestone: Recommend a value of *a* to reduce the physical aperture area and increase aperture efficiency (>50%) with no variation in other antenna metrics.

(E) Frequency scale fractal antenna design such that the center frequency of the resulting antenna equals 1.3 GHz / MAY21 / Complete.

- Milestone: Modify antenna design with a center frequency equal to 1.3 GHz and achieve similar results (3:1 bandwidth at fc = 1.3 GHz, 3 dBi gain and >130% aperture efficiency at 900 MHz) to antenna design at center frequency ~7 GHz.

(F) Design and simulate various array antenna geometries composed of optimized fractal antenna elements (obtained from (E)) to analyze the effect of overall array antenna geometry on the desired array antenna response metrics (i.e., gain vs. frequency, gain vs. elevation angle at constant phi, rE/V, half-power beamwidth and side-lobe level.) / MAY–JUL21 / Complete

- Milestone: Recommend a best possible structure with reduced aperture area and minimal loss in gain.

(G) Apply ML models available in Altair Hyperstudy (2021) on the fractal antenna to try and understand the possibilities and limitations of ML models for fast and efficient antenna metrics prediction and optimization. Through successful testing, a ML model can replace conventional EM simulators for faster optimization and prediction. / MAY–NOV21 / Complete.

- Milestone: Recommend most accurate and efficient ML model available in Altair Hyperstudy (2021) for a fractal antenna.

(H) Apply ML models on the octagon fractal antenna array lattice to extend the prediction capabilities of ML models. / SEP21–JAN22 / Ongoing.

- Milestone: Recommend the best suitable ML model implemented/developed using Python programming language for array antenna metrics prediction.

10.4.3 Progress Made Since Last Report

(G) Previously, each of the selected ML models were trained and tested for the prediction of the electric field in the frequency domain. Now, a new custom time-domain Gaussian pulse has been generated whose frequency content lies from 700 MHz to 3 GHz. The time-domain Gaussian pulse is used as the input signal for time-domain analysis of the fractal antenna. The obtained results are then used as the training data for the ML model. Due to limitations of hyperstudy, a new ML model k-nearest neighbor (kNN) regression, which is available in scikit learn in Python has been used for this study.

(H) Unlike the single element, Altair FEKO doesn't directly export the antenna output response (reflection coefficient or s11) in the output file (*. outfile) for an antenna array design. To resolve this issue, a new approach is proposed to validate the performance of the ML model in the prediction of antenna array response metrics by using the kNN ML model available in scikit learn. For this study, the reflection coefficient response of the antenna array is exported from postfeko as a *.dat file to further use it as the training data.

10.4.4 Technical Results

(G) The complete process of generating Gaussian pulse and using it as input to perform a time-domain analysis is performed using CST microwave studio. Fig 10.4.1 (a) illustrates the custom generated Gaussian pulse (Fmin = 700 MHz and Fmax = 3 GHz) and Fig 10.4.2 (b) is the comparison of kNN and CST response for the test data. The training data is selected in such a way that it covers extremes points of the antenna design variable values used to generate the training data, which is shown in Table 10.4.1. The RMSE value for the kNN is as low as 0.2246 indicating a good generalization capability of the ML model.

Table 10.4.1. Training data variable values.

	Pair-1	Pair-2	Pair-3	Pair-4	Pair-5
a (mm)	38.5	39.5	40.5	41.5	42.5
b (mm)	8	8.5	9	9.5	10
d (mm)	36	36.75	37.5	38.25	39
g (mm)	0.8	1	1.2	1.4	1.6

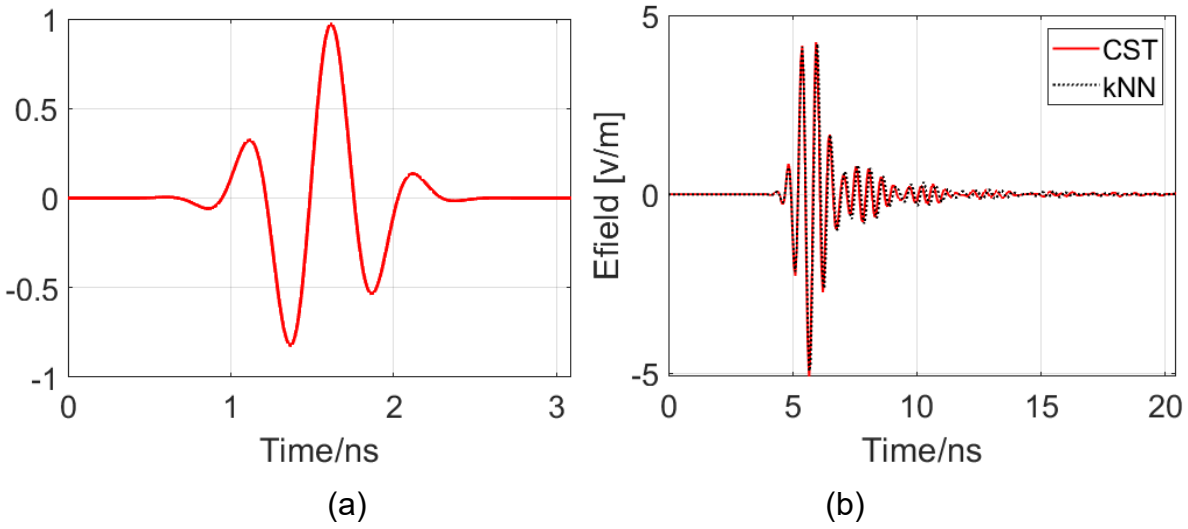

Figure 10.4.1. (a) Input gaussian pulse, (b) Comparison of E-field response calculated from CST and predicted by kNN ML model.

(H) From the analysis in (F), it is evident that antenna array with octagonal topology has shown high gain value with minimum sidelobe levels. Antenna array simulation on a regular laptop/desktop is a computationally expensive process therefore the training data has been generated using Lewis supercomputer. Five samples of training data are generated by changing the interelement (IE) spacing of the antenna array topology between 90 mm to 130 mm with the step size of 10 mm and corresponding reflection coefficient at 101 discrete frequency points between the range of 0 to 3 GHz is recorded for a center and a corner element in an antenna array (as shown in figure 10.4.2). As hyperstudy cannot be used for antenna array prediction, kNN algorithm available in scikit learn has been employed. Figure 10.4.3 illustrates the prediction of kNN for corner and center elements for test data (i.e., IE = 125 mm). The RMSE for a central element is 2.2340 and for a corner, element is 1.7352.

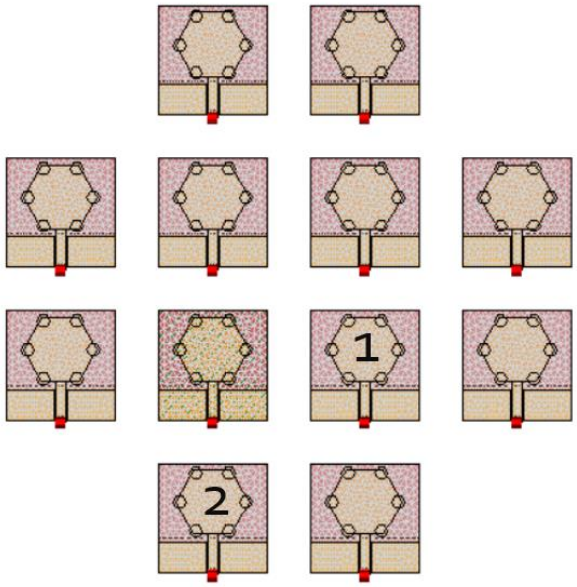

Figure 10.4.2. Center element is indicated ‘1’ and Corner element is indicated ‘2’.

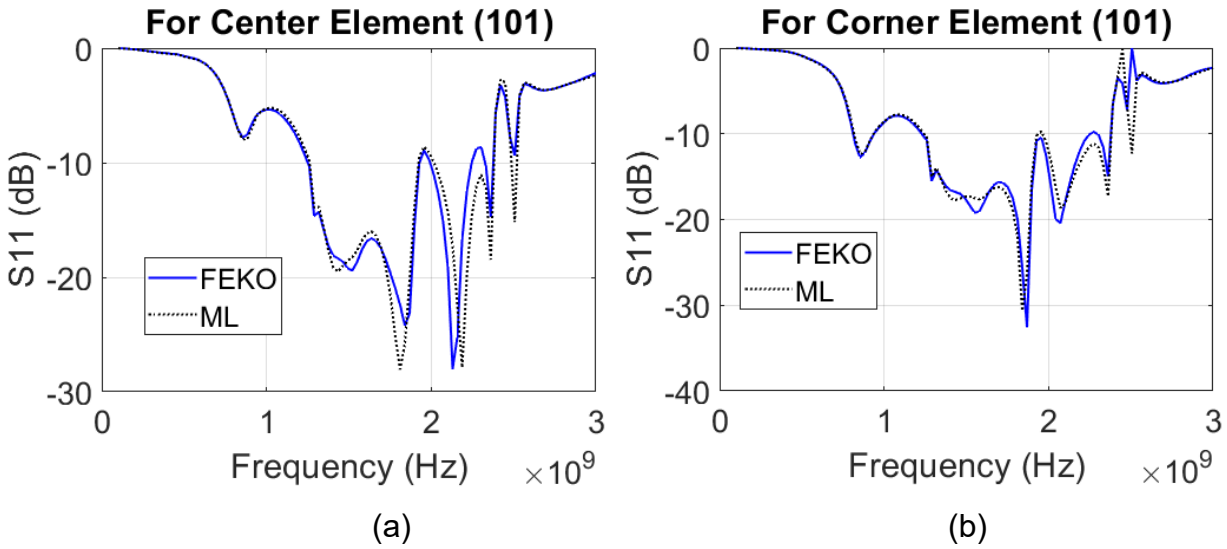

Figure 10.4.3. Comparison of reflection coefficient (a) FEKO with kNN for a center element of antenna array (ML), (b) FEKO with kNN for a corner element of antenna array (ML).

10.4.5 Summary of Significant Findings and Mission Impact

(A) The initial analysis of the simulation results with fractal radius *b* equal to 1.8 mm yielded multiple resonant frequencies with enhanced bandwidth. To further increase the bandwidth, OPTFEKO has been used as an optimization tool with fractal radius *b* as the optimization variable. The optimum value for *b* is found to be 1.66 mm. A

comparison between reflection coefficient for initial *b* (= 1.8 mm) value and the optimized *b* (= 1.66 mm) can be found in Figure. 6.4.6. The optimization is carried out over 51 discrete frequency points.

(B) The addition of fractal elements (*N*) to the simple hexagon improved antenna metrics such as S11. To further investigate and understand the fractal elements, the number of segments in the fractal geometry has been varied. The improvement in bandwidth is observed as the value of *N* is increased from 6 to 14.

(C) The initial optimum value of *b* over 51 discrete frequency points is reported as 1.66 mm in task (A). To further increase the accuracy of the optimization algorithm and to find a more precise value for *b*, optimization is further performed over wider frequency points (201 discrete points between 2 GHz to 12 GHz) which yielded the optimum value of b as 1.368 mm. The S11 response of antenna design with newly found *b* (i.e., 1.368 mm) hasn't produced any better bandwidth with respect to *b* (= 1.66 mm). Thus, *b* is set to be 1.66 mm for further research.

(D) The hexagonal patch radius *a* has a significant effect on the physical aperture area of the antenna. Therefore, Altair OPTFEKO has been utilized to find an optimum *a* value, which was found to be 8 mm over the range 7.2 to 9 mm. Antenna metrics such as S11, gain, and bandwidth have shown desired performance with the optimized *a* value.

(E) The initial antenna design has been modified to achieve a center frequency of ~1.3 GHz. The gain value at 900 MHz is 3.5 dBi and, with the modified antenna design, we were able to achieve an impedance bandwidth ratio of 3.3:1. The designed antenna has been fabricated and tested, and the S11 response of the fabricated antenna agrees well when compared against FEKO, CST.

(F) To summarize, four different fractal antenna array geometries (i.e., square, diamond, hexagon, and octagon) have been designed and simulated. Upon comparing antenna array metrics, octagonal fractal antenna array has yielded minimal sidelobe levels with a gain of 15.7 dBi at 900 MHz close to that of square geometry with 32.27% lower physical aperture area than that of square geometry. The octagonal fractal antenna array has been chosen as the optimum geometry with reduced aperture area and reduced side lobes while retaining the bandwidth and gain milestone metrics.

(G) Radial basis function (RBF) and least square regression (LSR) were down selected from the initial three ML models based upon their generalization capability for prediction of reflection coefficient (S11), gain, and electric field. Further analysis of increasing training data set size has shown no improvement in prediction accuracy. Trained ML models were tested for design variable values outside the training range. The resulting RMSE increased as the values drifted away from the mid-point of the training range. RBF performed well in the prediction of S11, while LSR performed slightly better for gain and electric field predictions. In addition, for time-domain electric field prediction, we recommend using k-nearest neighbors (kNN) ML algorithm for accurate prediction.

(H) Initial application of kNN ML model for the prediction of antenna array bandwidth response of center and corner element yielded positive results with a good agreement between traditional EM solver (FEKO) and trained kNN ML model.

10.4.6 References

[1] H. Fallahi and Z. Atlasbaf, "Study of a Class of UWB CPW-Fed Monopole Antenna With Fractal Elements," in IEEE Antennas and Wireless Propagation Letters, vol. 12, pp. 1484-1487, 2013, doi: 10.1109/LAWP.2013.2289868.

11 RF Coupling

11.1 Enclosure Effects on RF Coupling

(Mohamed Hamdalla and Ahmed Hassan)

11.1.1 Problem Statement, Approach, and Context

Primary Problem: UAVs are typically considered metallic/dielectric enclosures depending on their frame material. The shielding effectiveness of such enclosures might be compromised due to the slots and gaps on these enclosures, creating upset susceptibility to the enclosed electronics. The goal of this work is to quantify how the thresholds for upset susceptibility of enclosed wires and integrated circuits differ from those in free space.

Solution Space: Study enclosures with different shapes, material compositions, and slots to quantify their effect on RF coupling to the enclosed wires and electronics typically used in UAVs. The study will focus on the low-frequency range where the incident wavelength is comparable to the size of the enclosure or larger.

Sub-Problem: UAVs are manufactured with a wide variety of shapes and composites to accomplish an exponentially expanding list of missions. The configurations previously reported in the literature have simplistic assumptions regarding the shape and material composition of UAV enclosures that might overestimate or underestimate susceptibility.

State-of-the-Art (SOTA): Simple statistical analysis of specific enclosure configurations using either brute force simulations/measurements or pure statistical methods. Also, simplified UAV wire distributions are assumed.

Deficiency in the SOTA: Brute force simulations/measurements of the voltages and currents induced in wires and integrated circuits contained in enclosures are computationally or experimentally complex and have several limitations. The computations are complicated by the multiscale nature of the simulations, and the experiments are complicated by the cost of the equipment and the extensive time needed to measure every variation to cover all possible scenarios. Statistical methods, such as the Random Coupling Model (RCM) for example [1], are only accurate for high frequencies where the wavelength is much smaller than the size of the enclosure. Another main deficiency of the RCM is that it can't predict the exact induced voltages and currents for a specific well-characterized system but it only provides the statistical properties of these induced currents and voltages.

Solution Proposed: Apply Characteristic Mode Analysis (CMA) to identify the fundamental modes of the enclosure, current distribution, and the field pattern of each mode. This will allow us to predict the worst-case RF coupling scenarios without the need for lengthy simulations and/or expensive experimental measurements. The proposed approach can predict measurements at a fraction of the cost/time. Moreover, we propose to study RF coupling to realistic UAV wire distributions, experimentally reconstructed, when they are placed inside metallic/dielectric UAV enclosures.

Relevance to OSPRES Grant Objective: Provide general guidelines on how the environment, in this case, the enclosure, affects RF coupling and subsequent electromagnetic absorption to UAV wires and integrated circuits.

Risks, Payoffs, and Challenges: The modes depend mainly on the shape and material of the enclosure. Since UAVs have a wide variety of shapes and material compositions, a library of several UAVs needs to be studied before general quantitative conclusions can be drawn. Challenges can be mitigated by the use of the classification techniques of Machine Learning (ML). That is, different ML techniques will be evoked to detect hidden patterns on how the shape, material composition, and the shape/size location of slots correlate with the field enhancement inside the enclosure.

11.1.2 Tasks and Milestones / Timeline / Status

A. Complete the CMA implementation for studying the shielding effectiveness of metallic enclosures. Validate whether CMA can predict the worst-case shielding effectiveness of metallic enclosures as a function of their shapes. / JAN21 / Complete.

   A1. Prepare a manuscript for IEEE AWPL to document the progress done in A. / Ongoing.

B. Progressively build an accurate representation of the UAV wiring system with all of the integrated circuit (ICs) and electronics to test assist the predictions of (c) and the experimental measurement of the actual UAV. / JUL21 / Complete.

C. Address the 2021 UAV's semi-annual review recommendations to study arbitrarily shaped UAV wire distribution. / JUNE21 / Complete.

D. Define the main RF coupling pathways to UAVs, i.e. is RF coupling to the wires/traces the dominant pathway or is it the direct coupling to the electronics, and also quantify the sensitivity of these coupling pathways to load and wire variations. / December 21 / Ongoing.

11.1.3 Progress Made Since Last Report

Results from this reporting period will be provided in more detail in the next MSR.

11.1.4 Summary of Significant Findings and Mission Impact

A. A fast full-wave tool that facilitates studying the effect of a metallic enclosure on shielding effectiveness has been developed using CMA.

B. Developed an accurate model for the complete wiring system of an UAV, integrated the model with PECNEC, and validated the implementation with rigorous full-wave simulations.

C. Two Second series equivalent circuit branches/resonance is the best combination for the RLC circuit to accurately represent Zin of the system.

12 UAS Engagement Wargaming & Modeling and Simulation (M&S)

12.1 Fixed-Effector Wargaming Simulation Toolkit Development

(Nolan Petersen and Travis Fields)

12.1.1 Problem Statement, Approach, and Context

Primary Problem: Wargaming simulations enable rapid evaluation of different weapon systems and strategies. However, the lack of easy to use, high-fidelity software tools makes producing and studying different engagement scenarios (e.g., one friendly system versus five hostile agents) difficult and time-consuming.

Solution Space: We propose developing a simulation environment using the Unity real-time development platform to offer an easy-to-use, medium-fidelity environment for the purpose of studying different blue vs. red engagement scenarios. Unity is a well-established game development software, with a strong community base for tutorials, training, and software assistance. This makes Unity an ideal solution for a medium-fidelity simulation environment to narrow down optimal fixed effector configurations, which could then be studied further in a higher fidelity environment.

State-of-the-Art (SOTA): Current software tools (e.g. AFSIM) for this purpose are tedious to adapt and/or modify for running different scenarios due to a lack of documentation and support.

Relevance to OSPRES Grant Objective: Wargaming simulations are relevant to the OSPRES Grant Objective because the ability to simulate and benchmark performance of different scenarios, such as different fixed-effector positions, types, and targeting strategies could provide insight into the ideal utilization of HPM-related systems.

Anticipated Outcome(s): The anticipated outcome of development of a wargaming simulation is a medium-fidelity user friendly wargaming simulation tool capable of simulating realistic engagement scenarios with the ability to easily manipulate the scenario and quickly obtain results.

Challenges: Capturing sufficient realism without significantly reducing performance.

Risks: The risk involved with wargaming simulations is the infinite number of scenarios and configurations, making generalizing difficult from within a simulation environment.

12.1.2 Tasks and Milestones / Timeline / Status

(A) Reproduction of results obtained from the previously used wargame software Modern Air Power by John Tiller Software, which is no longer in development, using the Unity environment / MAY21 – JUN21 / Completed.

(B) Implementation of radar uncertainty into simulation environment, enabling increased realism to better simulate current targeting capabilities / JUN21 – JUL21 / Completed.

(C) Trade-space study of microwave, tracking, and hostile agent performance to identify key limitations and low-risk, low-cost improvements, enabling increased weapon efficacy / JUL21 – DEC21 / In Progress.

(D) Optimization of current simulation framework to facilitate more quickly obtaining results / SEP21 – OCT21 / Completed.

(E) Implementation of more effector models such as kinetic weapons and radio jammers to better simulate a layered defense / OCT21 – FEB22 / In Progress.

(F) Implementation of electro-optical/infra-red and lidar sensor capabilities into simulation environment, enabling increased realism to better simulate current targeting capabilities / FEB22 – MAR22 / Upcoming.

12.1.3 Progress Made Since Last Report

(C) Through comparing trade-space study results obtained using both the C# simulation and MATLAB, a higher level of fidelity using the C# simulation was achieved.

(E) A literature review was started concerning radio frequency (RF) jamming to inform the implementation of a jammer model into the C# simulation.

12.1.4 Technical Results

(C) After finding disagreement in the results from the trade-space study described in the October 2021 Grant MSR, the issue was investigated further. To better understand the behavior of the C# simulation, the same trade-space study performed in the October 2021 Grant MSR was performed, this time however, the time to effect (TTE) parameters were fixed, and half of the UAVs began on an outer radius, and the other half began on an inner radius. These two concentric circles were then offset from each other such that no UAV is blocking another and the angle between each UAV is 3.6°. The scenario described is pictured in Figure 12.1.1 below.

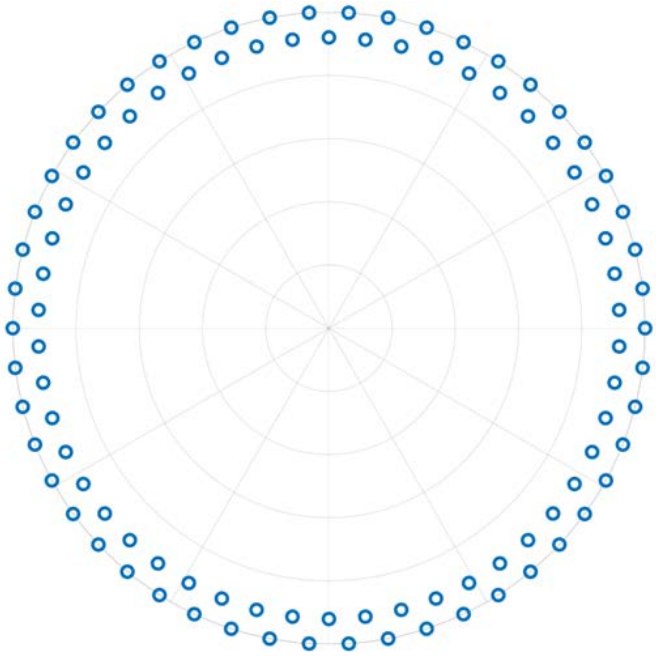

Figure 12.1.1. UAV starting locations for the previously described scenario.

Instead of recording the radius at which the final UAV was killed, as was previously done, the locations at which each UAV was killed was instead recorded. This provided a much clearer understanding of why there was disagreement between the MATLAB results and the C# simulation results. The locations at which each UAV was killed are provided in Figure 12.1.2 below.

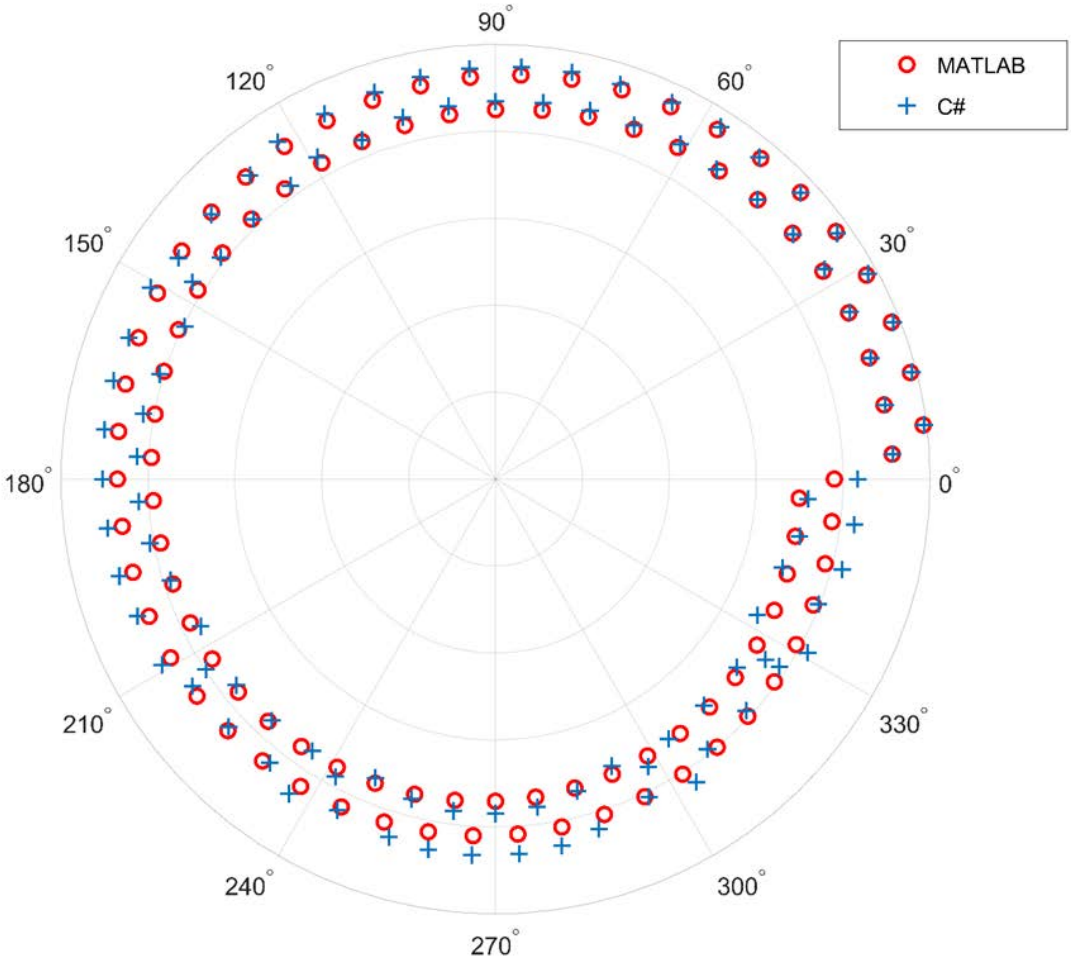

Figure 12.1.2. Locations at which each UAV was killed in the MATLAB and C# simulation where the C# simulation is using floats.

From Figure 12.1.2 it was found that the UAVs were not always moving in a straight line as intended. They were instead deviating from their straight-line paths. After further investigation, these deviations were attributed to floating point rounding errors. The method by which a UAV is moved in the C# simulation is by calculating the change in each component (dx, dy, dz) every time the code runs and adding these components to the UAV's current position. If the UAV's current position is large, e.g. (70000, 70000, 70000), in combination with the change in each component for a given run being small, e.g. (0.0002, 0.0002, 0.0002), the C# float data type cannot keep track of enough significant figures and the new position is simply rounded up to the smallest significant

figure that the C# float data type can keep track of. This problem could arise from running the simulation at a small time-step, the UAVs moving very slowly, or from the UAVs being extremely far from the origin. Because there were so many ways this could affect results, it was deemed prudent to use a data type that could store twice the number of significant figures to make the simulation more robust and more reliable in any given scenario. Below in Figure 12.1.3 are results from the same trade-space study performed using doubles rather than floats to store UAV locations.

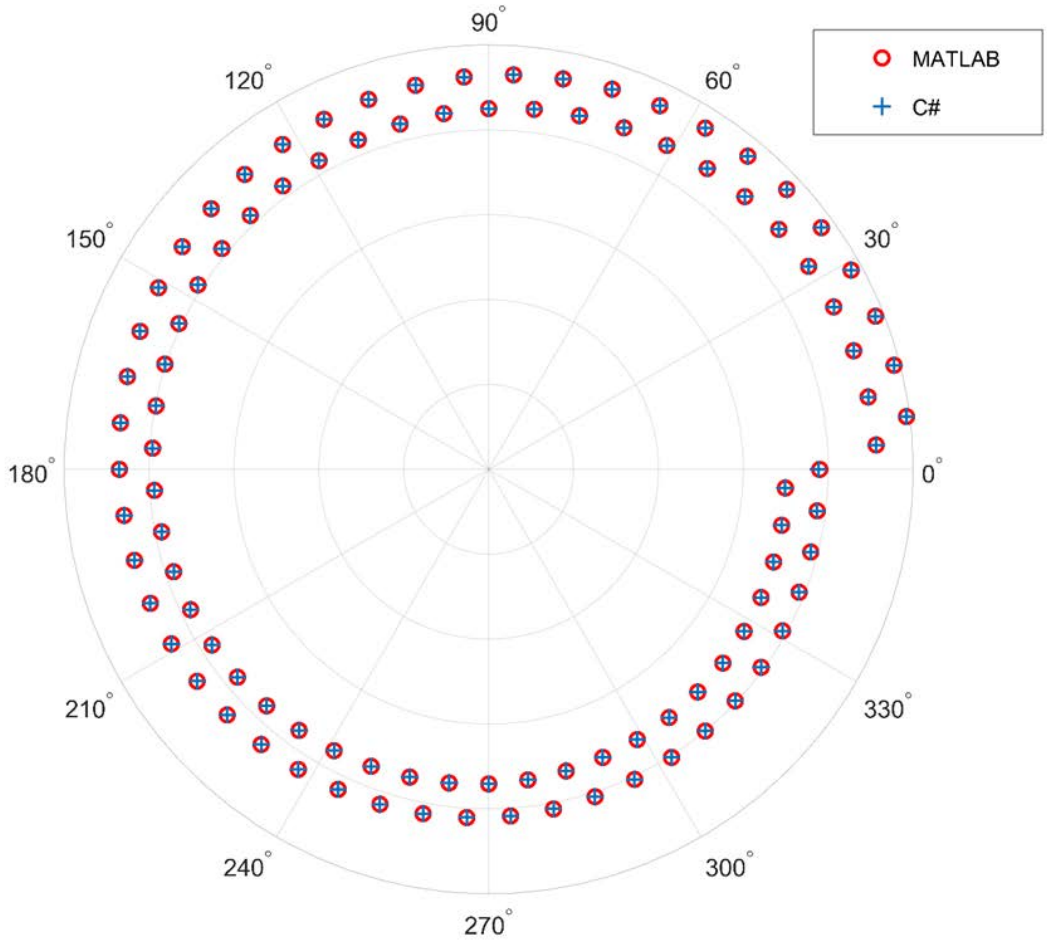

Figure 12.1.3. Locations at which each UAV was killed in the MATLAB and C# simulation where the C# simulation is using doubles.

From Figure 12.1.3, the agreement is much better, and the C# simulation is now behaving as expected.

(E) To implement different types of effectors into the C# simulation, a literature search must be done for existing models of each type of effector. The first effector that will be implemented into the C# simulation are jammers. To clarify, the type of jamming that will

be implemented into the C# simulation is the jamming of a Remote Control (RC) or GPS signal to the UAV such that the UAV either lands on the ground or returns to the last known controller location. This is not to be confused with electronic countermeasures where a red aircraft is jamming blue's radar capabilities. This may be implemented in the future, but for now the focus is on blue jamming red UAV signals.

There are generally two types of jammers used for jamming UAVs. The first being jammers that use an omni-directional antenna, the second being jammers that use antennas that focus the radio waves into lobes. The shape of these lobes varies with antenna shape. The first type of jammer is omni-directional at the cost of range of effectiveness, while the second type of jammer is more suited to targeting UAVs over a long distance.

For simplicity, only jammers utilizing an omni-directional antenna will be implemented into the C# simulation. However, with a radiation diagram of an existing antenna, or something close, the same omni-directional RF jamming model could be extended to include directed jamming.

For specific equations pertaining to jammer performance, radio frequency (RF) jammers work similar to radar in that their effectiveness is highly dependent on the signal-to-noise ratio (SNR). However, in the context of jamming, this measure of performance is typically expressed as the inverse of the SNR as the jamming-to-signal (JSR) ratio where the jammer is creating noise at the UAV's receiving antenna(s) thus degrading the SNR of the GPS signal as well as any RC signal. The equation commonly used for the JSR [1] in units of dB is shown in equation (1).

$$JSR = \frac{J}{S} = P_J + G_J + G_r - P_T - 2G_T + 20\log d_S + 20\log \lambda_J - 20\log d_J - 20\log \lambda_S \qquad (1)$$

Where J (dB) is the power of the noise created at the target antenna(s), S (dB) is the power of the signal being jammed at the target antenna(s) (e.g., GPS, RC), P_J (dBW) is the power output by the jammer, G_J (dBi) is the antenna gain of the jammer, G_r (dBi) is the receiver gain on the jamming signal, P_T (dBW) is the power output by the transmitter, G_T (dBi) is the antenna gain of the transmitter, d_S (m) is the distance between the transmitter and the target antenna(s), λ_J (m) is the wavelength of the jamming signal, d_J (m) is the distance between the jammer and the target antenna(s), and λ_S (m) is the wavelength of the signal being jammed. For a high-level model, using the JSR in equation (1) in combination with the fact that for any given wireless device, there is a threshold SNR at which the device will not function properly may suffice. However, the uncertainty in where that SNR threshold is located is not yet clear, but seems to be associated with something called the bit-error rate (BER) which will be reviewed further.

12.1.5 Summary of Significant Finding and Mission Impact

(A) Reproduction of previous results obtained from Modern Air Power by John Tiller Software was completed in Unity, which provided a framework to implement new features.

(B) Implementation of radar uncertainty into the Unity simulation environment was completed.

(C) A trade-space study of the effect of slew-rate on HPM effectors with and without radar uncertainty and off-boresight effects was performed. This study showed that beyond a threshold slew-rate, additional kills are not possible without decreasing firing delay. It also showed that the performance of energy weapons without off-boresight effects is susceptible to the effects of radar uncertainty, while energy weapons with off-boresight effects may mitigate the effects of radar uncertainty on performance.

A trade-space study around a specific type of high-powered microwave (HPM) effector modeled by the time to effect treatment was performed in both MATLAB and the C# simulation to both compare results and understand the behavior of the C# simulation. This provided insight into possible issues with the C# simulation which will be explored in the future.

The previous comparison between trade-space study results obtained using MATLAB and the C# simulation showed that the C# “float” data type used for storing object positions had an insufficient number of significant figures and was replaced with a more precise “double” data type for more accurate and robust results.

(D) Optimization of the simulation through development of a custom C# library was completed.

(E) A literature review on radio jamming was started.

12.1.6 References

[1] F. Lu, Z. Qiu, X. Gu, B. Zhang and Z. Xin, "Efficiency Analysis of High Power Microwaves Jamming Digital Communication System," 2020 23rd International Microwave and Radar Conference (MIKON), 2020, pp. 136-139, doi: 10.23919/MIKON48703.2020.9253907.

13 Program Management

13.1 Issues

i. Scope – No issues
ii. Budget – 12-month NCTE submitted/pending
iii. Schedule – No issues

13.2 Interactions with Others

Agency/Org	Performer	Project Name	Purpose of Research/ Collaboration

13.3 Major Procurement Actions

13.4 Travel

Destination	Purpose	Attendees	Estimated Costs

13.5 Pending or Upcoming Public Release Requests

14 Appendix A: Academic and IP Output

14.1 Students Graduated

Name	Degree	Currently
Al-Shaikhli, Waleed Azad, Wasekul	MS Spring 19 PhD Summer 21	Kansas City National Security Campus, Honeywell Applied Materials, Sunnyvale, CA
Berg, Jordan	MS Spring 21	MRI Global
Bissen, Bear	MS Spring 19	Kansas City National Security Campus, Honeywell
Floyd, Dennis	BS	Naval Air Warfare Center Weapons Division
Hanif, Abu	PhD Spring 21	UMKC/MIDE (Postdoc)
Harmon, Aaron	BS	Missouri University of Science & Technology
Harp, Joshua	MS	UMKC/MIDE (Senior Engineer)
Hauptman, Cash	BS Spring 18	University of Nebraska-Lincoln
Klappa, Paul	MS Spring 21	
Labrada, Dario	BS Spring 20	Honeywell Aerospace, Florida
Lancaster, John	MS Spring 17	Lawrence Livermore National Laboratory
Renzelman, Jeff	MS Spring 18	Kansas City National Security Campus, Honeywell
Roy, Sourov	PhD Spring21	
Wagner, Adam	MS Fall 20	Kansas City National Security Campus, Honeywell
Xia, Shengxuan	BS	Missouri University of Science & Technology

14.2 Journal Publications

14.2.1 In Preparation

[1] N. Gardner, K. C. Durbhakula, and A. N. Caruso, “UHF and L-Band Frequency Generation at MW Peak Power using Diode-based Nonlinear Transmission Lines as Pulse Forming Networks,” *Transactions on Plasma Science*, In Preparation, **2021**.

[2] N. Gardner, K. C. Durbhakula, and A. N. Caruso, “Electrically Tunable Diode-based Nonlinear Transmission Line,” *TBD*, In Preparation, **2021**.

[3] N. Gardner, A. N. Caruso, K. C. Durbhakula and P. Doynov, “Diode-Based Non-Linear Transmission Line Design Considerations,” *Journal of Applied Physics*, In Preparation, **2021**.

[4] B. Barman, D. Chatterjee, and A. N. Caruso, “Tradespace Analysis of Wideband, Electrically Small Microstrip Patch Antenna Elements for Phased Array Applications,” *IEEE Antennas and Propagation Magazine,* In preparation, **2021**.

[5] S. Xia, J. Hunter, A. Harmon, M. Hamdalla, A. Hassan, V. Khilkevich, D. Beetner, “Simulation Driven Statistical Analysis of the Electro-magnetic Coupling to Microstriplines,” *IEEE Transactions on Electromagnetic Compatibility*, In Preparation, **2020**.

[6] M. Hamdalla, V. Khilkevich, D. G. Beetner, A. N. Caruso, A. M. Hassan, “Characteristic Mode Analysis Justification of the Stochastic Electromagnetic Field

Coupling to Randomly Shaped Wires," *IEEE Transactions on Electromagnetic Compatibility*, In Preparation, **2020**.

14.2.2 Submitted / Under Revision

[7] B. Barman, K. C. Durbhakula, D. Chatterjee, and A. N. Caruso, "Comparison of Machine Learning Algorithms for Bandwidth Enhancement of a Coaxial Probe-fed Microstrip Patch Antenna," *Applied Computational Electromagnetics Society (ACES)*, Submitted, **2021**.

[8] B. K. Lau, M. Capek, and A. M. Hassan, "Characteristic Modes–Progress, Overview, and Future Perspectives," *IEEE Antennas and Propagation Magazine*, Submitted, **2021**.

[9] K. Alsultan, M. Z. M. Hamdalla, S. Dey, P. Rao, and A. M. Hassan, "Scalable and Fast Characteristic Mode Analysis Implementation Using a Hybrid CPU/GPU Platform," *ACES*, Submitted, **2021**.

[10] M. Z. M. Hamdalla, B. Bissen, J. Hunter, L. Yuanzhuo, V. Khilkevich, D. G. Beetner, A. N. Caruso, and A. M. Hassan, "Prediction of Experimental Electromagnetic Coupling to a UAV Model Using Characteristic Mode Analysis," *IEEE Access*, Submitted, **2021**.

[11] W. Azad, F. Khan, and A. N. Caruso, "A Scalable Multilevel-Modular 10 kV Silicon Carbide MOSFET Module Featuring Custom Isolated Gate Driver Circuit Combined with Coupling and Snubber Circuits," *IEEE Transactions on Power Electronics*, Submitted, **2021.**

[12] John Keerthi Paul Bhamidipati, Eliot R. Myers, Adam M. Conway, Lars F. Voss, and Anthony N. Caruso, "Figure of Merit Development for Linear-Mode Photoconductive Solid-State Switches," *IEEE Transactions on Electronic Devices*, Under Revision, **2020**.

14.2.3 Published / In Press

[13] M. Z. M. Hamdalla, B. Bissen, J. Hunter, Y. Liu, V. Khilkevich, D. G. Beetner, A. N. Caruso, and A. M. Hassan, "Prediction of Experimental Electromagnetic Coupling to a UAV Model Using Characteristic Mode Analysis," *IEEE Access*, In Press, **2021**.

[14] J. N. Berg, R. C. Allen, and S. Sobhansarbandi. "A Novel Method of Cooling a Semiconductor Device through a Jet Impingement Thermal Management System: CFD Modeling and Experimental Evaluation." *International Journal of Thermal Sciences*, 172, 107254, **Feb 2022** [doi].

[15] W. Azad, F. Khan, and A. N. Caruso, "A Medium Power, Self-Sustaining, Configurable RF Pulse Generation Circuit Using a Nonlinear Transmission Line and Power Amplifier in a Closed Loop Configuration, *IEEE Transactions on Plasma Science*, vol. 49, no. 7, pp. 2183–2194, **July 2021** [doi].

[16] S. Roy, W. Azad, S. Baidya and F. Khan, "A Comprehensive Review on Rectifiers, Linear Regulators and Switched-Mode Power Processing Techniques for Biomedical Sensors and Implants utilizing In-body Energy Harvesting and External

Power Delivery," *IEEE Transactions on Power Electronics*, vol. 36, no. 11, pp. 12721–12745, **Nov 2021** [doi].

[17] K. C. Durbhakula, D. Chatterjee, and A. M. Hassan, "An Efficient Algorithm for Locating TE and TM Poles for a Class of Multiscale Inhomogeneous Media Problems," *IEEE Journal on Multiscale and Multiphysics Computational Techniques*, vol. 4, no. 1, pp. 364–373, **2019** [doi].

14.3 Conference Publications

14.3.1 Submitted / Accepted

[1] S. R. Shepard and H. A. Thompson, "Self-focusing in Guided and Un-guided Media," submitted to the *2021 OSA Nonlinear Optics Topical Meeting, Virtual Event*, August 9-13, 2021.

14.3.2 Presented

[2] B. Barman, D. Chatterjee and A. N. Caruso, "Probe-location Optimization in a Wideband Microstrip Patch Antenna using Genetic Algorithm, Particle Swarm and Nelder-Mead Optimization Methods," *2021 International Applied Computational Electromagnetics Society Symposium (ACES)*, 2021, pp. 1-3 [doi].

[3] W. Azad, S. Roy, and F. Khan, "A Single Gate Driver-based Four-stage High-voltage SiC Switch Having Dynamic Voltage Balancing Capability," *2021 IEEE Applied Power Electronics Conference and Exposition* (APEC), Phoenix, AZ, USA, June 9-12, 2021.

[4] W. Azad, S. Roy, F. Khan and A. N. Caruso, "A Multilevel-Modular 10 kV Silicon Carbide MOSFET Module using Custom High-Voltage Isolated Gate Driver, Coupling, and Snubber Circuits," *2021 IEEE Kansas Power and Energy Conference* (KPEC), Manhattan, KS, USA, April 19-20, 2021 [doi].

[5] T. Layman, T. D. Fields, and O. A. Yakimenko, "Evaluation of Proportional Navigation for Multirotor Pursuit," AIAA SciTech Forum, Virtual Event, January 11-21, 2021 [doi].

[6] P. J. Klappa, and T. D. Fields, "Assessment of Fixed-Wing UAV System Identification Models during Actuator and Payload Drop Failures," AIAA Atmospheric Flight Mechanics Conference, Virtual Event, January 11-21, 2021 [doi].

[7] J. Hunter, S. Xia, A. Harmon, A. M. Hassan, V. Khilkevich, and D. Beetner, "Modeling and Statistical Characterization of Electromagnetic Coupling to Electronic Devices," *IEEE International Symposium on Antennas and Propagation and NSRM USNC-URSI National Radio Science Meeting*, Boulder, CO, January 4-9, 2021 [doi].

[8] B. Barman, K. C. Durbhakula, B. Bissen, D. Chatterjee, and A. N. Caruso, "Performance Optimization of a Microstrip Patch Antenna using Characteristic Mode and D/Q Analysis," *2020 XXXIIIrd General Assembly and Scientific Symposium of*

the International Union of Radio Science, Rome, Italy (online conference), Aug 29-Sept 5, 2020, pp. 1-4 [doi].

[9] J. Berg, and S. Sobhansarbandi. “CFD Modeling of Thermal Management Systems for a Silicon Semiconductor Switch.” *ASME 2020 Heat Transfer Summer Conference collocated with the ASME 2020 Fluids Engineering Division Summer Meeting and the ASME 2020 18th International Conference on Nanochannels, Microchannels, and Minichannels*, Virtual, July 13–15, 2020, American Society of Mechanical Engineers Digital Collection [doi].

[10] B. Barman, D. Chatterjee, and A. N. Caruso, “Performance Optimization of Electrically Small Microstrip Patch Antennas on Finite Ground Planes,” 2020 *IEEE International Symposium on Antennas and Propagation and North American Radio Science Meeting*, Montreal, Quebec, Canada, July 5-10, 2020, pp. 1–2 (online conference) [doi].

[11] M. Hamdalla, B. Bissen, A. N. Caruso, and A. M. Hassan, “Experimental Validations of Characteristic Mode Analysis Predictions Using GTEM Measurements,” *IEEE International Symposium on Antennas and Propagation and USNC-URSI Radio Science Meeting,* Montréal, Québec, Canada, July 5-10, 2020 [doi].

[12] K. Alsultan, P. Rao, A. N. Caruso, and A. M. Hassan, “Scalable Characteristic Mode Analysis: Requirements and Challenges (White Paper),” *Large Scale Networking (LSN) Workshop on Huge Data: A Computing, Networking and Distributed Systems Perspective Sponsored by NSF*, Chicago, IL, April 13-14, 2020.

[13] M. Hamdalla, A. N. Caruso, and A. M. Hassan, “Predicting Electromagnetic Interference to a Terminated Wire Using Characteristic Mode Analysis,” *Proceedings of the Annual Review of Progress in Applied Computational Electromagnetics (ACES)*, Monterey, CA, March 22-26, 2020. [doi]

[14] W. Azad, F. Khan, and A. Caruso, "Self-sustaining High-power RF Signal Generation Using LDMOS Based Power Amplifier and Nonlinear Transmission Line," *2020 IEEE Applied Power Electronics Conference and Exposition (APEC)*, New Orleans, LA, USA, March 15-19 2020, pp. 3567-3572 [doi].

[15] A. Hanif, W. Azad, and F. Khan, "Detection of Bond Wire Lift Off in IGBT Power Modules Using Ultrasound Resonators," *2020 IEEE Applied Power Electronics Conference and Exposition (APEC)*, New Orleans, LA, USA, March 15-19 2020, pp. 345-350 [doi].

[16] B. Barman, D. Chatterjee, and A. N. Caruso, “Some Investigations into Mutual Coupling Analysis for Trade Space Studies of Linear Arrays,” *2019 IEEE International Symposium on Phased Array Systems and Technology (PAST)*, Waltham, MA, October 2019, pp. 1-8 [doi].

[17] B. Barman, D. Chatterjee, and A. N. Caruso, “Characteristic Mode Analysis of a straight and an L-probe fed Microstrip Patch,” *2019 IEEE Indian Conference on Antennas and Propogation (InCAP)*, Ahmedabad, India, Dec 2019, pp. 1-3 [doi].

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Symposium on Antennas and Propagation and USNC-URSI Radio Science Meeting at Atlanta (2 pages), Georgia, USA, July 7-12, 2019 [doi].

[19] M. Hamdalla, J. Hunter, Y. Liu, V. Khilkevich, D. Beetner, A. Caruso, and A. M. Hassan, "Electromagnetic Interference of Unmanned Aerial Vehicles: A Characteristic Mode Analysis Approach," *IEEE International Symposium on Antennas and Propagation and USNC-URSI Radio Science Meeting at Atlanta (2 pages)*, Georgia, USA, July 7-12, 2019 [doi].

[20] K. C. Durbhakula, J. Lancaster, A. M. Hassan, D. Chatterjee, A. N. Caruso, J. D. Hunter, Y. Liu, D. Beetner, and V. Khilkevich, "Electromagnetic Coupling Analysis of Printed Circuit Board Traces using Characteristic Mode Analysis," *IEEE International Symposium on Antennas and Propagation and USNC-URSI Radio Science Meeting (2 pages)*, Atlanta, Georgia, USA, July 7-12 2019 [doi].

[21] K. C. Durbhakula, D. Chatterjee, and A. M. Hassan, "On the Location of Transverse Electric Surface Wave Poles for Electrically Thick Substrates," Proceedings of the *IEEE Antennas and Propagation International Symposium and National Radio Science Meeting*, Atlanta, Georgia, USA, July 7-12, 2019 [doi].

[22] W. Azad and F. Khan, "Sustaining High-power RF Signal Generation in a Positive Feedback Network," *2019 IEEE Pulsed Power and Plasma Science Conference (PPPS)*, Orlando, FL, USA, June 23-28 2019.

[23] K. Alsultan, P. Rao, A. N. Caruso, and A. M. Hassan, "Scalable characteristic mode analysis using big data techniques," *International Symposium on Electromagnetic Theory (EMTS 2019)*, San Diego, CA, USA, May 27-31, 2019.

[24] M. Hamdalla, W. Al-Shaikhli, J. Lancaster, J. D. Hunter, L. Yuanzhuo, V. Khilkevich, D. G. Beetner, A. N. Caruso, and A. M. Hassan, "Characteristic Mode Analysis of Electromagnetic Coupling to Wires with Realistic Shapes," *International Symposium on Electromagnetic Theory (EMTS 2019)*, San Diego, CA, USA, May 27-31, 2019.

[25] K. C. Durbhakula, D. Chatterjee, and A. M. Hassan, "Location of Surface Wave Poles in Sommerfeld Integrals: A Mittag-Leffler Expansion Approach," *Proceedings of the URSI-B International Symposium on Electromagnetic Theory*, URSI Commission, San Diego, USA, May 2019 [doi].

[26] K. C. Durbhakula, D. Chatterjee and A. M. Hassan, "Analytical Evaluation of Sommerfeld Integral Tails Present in Two-layered Media Green's Functions," *Proceedings of the Indian Conference on Antennas and Propagation* (InCAP), Hyderabad, India, December 2018 [doi].

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[28] C. Hartshorn, K. Durbhakula, D. Welty, D. Chatterjee, J. Lancaster, A. M. Hassan, and A. N. Caruso, "Crosstalk and Coupling to Printed Circuit Board Metallic Traces with Arbitrary Shapes," *Proceedings of the AMEREM 2018 Conference*, Santa Barbra, CA, Aug 27-31, 2018.

[29] M. Hamdalla, J. Roacho-Valles, J. Hunter, D. Beetner, A. M. Hassan, and A. N. Caruso, "Electromagnetic Analysis of Unmanned Aerial Vehicles Using

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[32] J. Lancaster, D. Chatterjee, and A. N. Caruso, "Some Investigations into the Dispersion Characteristics of Localized Bessel Beams," published in the *IEEE Antennas and Propagation International Symposium and National Radio Science Meeting*, Boston, Mass., USA, July 7-12, 2018 (1 page URSI Abstract).

[33] M. Hamdalla, A. M. Hassan, and A. N. Caruso "Characteristic Mode Analysis of Unmanned Aerial Vehicles with Realistic Shapes and Material Composition," *IEEE International Symposium on Antennas and Propagation and USNC-URSI Radio Science Meeting,* Boston, MA, July 8-13, 2018.

[34] W. Azad, S. Roy, A. S. Imtiaz, and F. Khan, "Microelectromechanical System (MEMS) Resonator: A New Element in Power Converter Circuits Featuring Reduced EMI," *2018 International Power Electronics Conference (IPEC-Niigata 2018-ECCE Asia)*, Niigata, May 20-24, 2018, pp. 2416-2420 [doi].

[35] J. Hunter, Y. Liu, D. Floyd, A. Hassan, V. Khilkevich, and D. Beetner, "Characterization of the Electromagnetic Coupling to UAVs," *Annual Directed Energy Science and Technology Symposium*, Feb 26-March 2, 2018.

14.4 Conference Presentations

14.4.1 Submitted / Accepted

[1] S. Bellinger, A. Caruso, A. Usenko, "Stacked Diodes for Pulsed Power Applications," GOMACTech-22, Miami, FL, March 21–24 2022 (submitted, oral).

[2] S. Bellinger, A. Caruso, A. Usenko, "New Paradigm on Making Semiconductor Opening Switches for Pulsed Power," 2021 23rd IEEE Pulsed Power Conference, Denver, CO, Dec. 12–16, 2021 (accepted, oral).

Directed Energy Professional Society, Directed Energy Systems Symposium, Washington DC, October 25-29 2021 (submitted):

[3] B. Barman, D. Chatterjee, A. Caruso, and K. Durbhakula, "Tradespace Analysis of a Phased Array of Microstrip Patch Electrically Small Antennas (ESAs)" (Poster)

[4] J. N. Berg, R. C. Allen, and S. Sobhansarbandi, "A Novel Method of Cooling a Semiconductor Device through a Jet Impingement Thermal Management System: CFD Modeling and Experimental Evaluation" (Poster)

[5] J. N. Berg, R. C. Allen, and S. Sobhansarbandi, “Heat Transfer Enhancement of a Jet Impingement Thermal Management System: A Comparison of Various Nanofluid Mixtures” (Poster)

[6] J. Bhamidipati, M. Paquette, R. Allen, and A. Caruso, “Photoconductive Semiconductor Switch Enabled Multi-Stage Optical Source Driver” (Poster)

[7] G. Bhattarai, J. Eifler, S. Roy, M. Hyde, J. Bhamidipati, A. Usenko, M. Pederson, M. Paquette, A. Caruso, S. Bellinger, L. Voss, and R. Allen, “All Solid-State High-Power Pulse Sharpeners” (Poster)

[8] S. Brasel, K. Norris, R. Allen, A. Caruso, and K. Durbhakula, “Efforts to Reduce Physical Aperture Area of Ultra-Wideband Arrays” (Poster)

[9] A Caruso, “ONR Short Pulse Research and Evaluation for c-sUAV: Supporting and Sub-Programs Overview” (Oral)

[10] J. Clark, R. C. Allen, and S. Sobhansarbandi, “Ultra-Compact Integrated Cooling System Development” (Poster)

[11] J. Eifler, S. Roy, M. Hyde, G. Bhattarai, J. Bhamidipati, A. Usenko, M. Pederson, M. Paquette, A. Caruso, S. Bellinger, L. Voss, and R. Allen, “TCAD Optimization of Epitaxially Grown Drift-Step Recovery Diodes and Pulser Performance” (Poster)

[12] N. Gardner, M. Paquette, and A. Caruso, “Diode-Based Nonlinear Transmission Lines Capable of GHz Frequency Generation at Single MW Peak Powers” (Poster)

[13] M. Hamdalla, A. Caruso, and A. Hassan, “The Shielding Effectiveness of UAV Frames to External RF Interference” (Poster)

[14] M. Hamdalla, A. Caruso, and A. Hassan, “A Predictive-Package for Electromagnetic Coupling to Nonlinear-Electronics using Equivalent-Circuits and Characteristic-Modes (PECNEC)” (Poster)

[15] M. Hyde, J. Eifler, S. Roy, G. Bhattarai, A. Usenko, M. Paquette, A. Caruso, S. Bellinger, L. Voss, and R. Allen, “Development of an Evaluation Network for Drift Step Recovered Diodes through and Augmented Design of Experiment” (Poster)

[16] S. Indharapu, A. Caruso, and K. Durbhakula, “Machine Learning Based Ultra-Wideband Antenna Array Optimization and Prediction” (Poster)

[17] F. Khan, W. Azad, and A. Caruso, “A Scalable Multilevel-Modular 10 kV Silicon Carbide MOSFET Architecture for Pulsed Power Applications” (Poser)

[18] D. F. Noor, J. Eifler, M. Hyde, G. Bhattarai, S. Roy, J. Bhamidipati, A. Usenko, M. Pederson, M. Paquette, A. Caruso, S. Bellinger, L. Voss, and R. Allen, “DSRD-IES Pulsed-Power Generator Topology Study Using Machine-Learning-Based Feature Selection Optimization and Predictive Learning” (Poster)

[19] S. Roy, J. Eifler, M. Hyde, G. Bhattarai, D. Noor, J. Bhamidipati, A. Usenko, M. Pederson, M. Paquette, A. Caruso, S. Bellinger, L. Voss, and R. Allen, “Systematic Topological Optimization of DSRD-Based IES Pulse Generator” (Poster)

[20] S. Shepard and A. Caruso, “Tubular Core Optical Power Amplifier” (Poster)

[21] H. Thompson, M. Paquette, and A. Caruso, “Minimizing On-State Resistance in GaN:X Photoconductive Semiconductor Switches (PCSSs) for Direct Modulation (Poster)

[22] A. Usenko, J. Eifler, S. Roy, G. Bhattarai, M. Hyde, M. Paquette, A. Caruso, S. Bellinger, L. Voss, and R. Allen, “New Paradigm in Fabrication of Semiconductor Opening Switches for Pulsed Power” (Poster)

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[23] S. Bellinger, A. Caruso, A. Usenko, “Stacked Diodes for Pulsed Power Applications: New Process Integration Scheme,” 240th Electrochemical Society Meeting, Orlando, FL, Oct. 10–14, 2021 (submitted, oral).

14.4.2 Presented

[24] W. Azad, S. Roy, and F. Khan, “A Four-State Capacitively Coupled High-Voltage Switch Powered by a Single Gate Driver,” *47th IEEE Conference on Plasma Science*, Singapore, December 6-10, 2020 (oral).

[25] J. Hunter, S. Xia, A. Harmon, A. Hassan, V. Khilkevich, and D. Beetner, “Simulation-Driven Statistical Characterization of Electromagnetic Coupling to UAVS,” *Annual Directed Energy Science and Technology Symposium*, March 2020 (abstract appeared, but talk cancelled due to pandemic).

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DEPS Posters and Presentations 2020

[26] William Spaeth, Wideband Parallel Plate to Coaxial Cable Taper

[27] Stefan Wagner, Quickly Determining Minimum HPC Source Requirements Using Binary Search

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GOMAC 2019

[28] Cash Hauptmann, Reduced Recovery Time in SiPCSS Photoconductive Switches

[29] Eliot Myers, Picosecond High Power Switching Technologies

[30] Heather Thompson, GaN Optimization for Use in Photoconductive Switch

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[28] B. Barman, D. Chatterjee, and A. N. Caruso, “Analytical Models for L-Probe fed Microstrip Antennas,” *Proceedings of the IEEE Antennas and Propagation International Symposium and National Radio Science Meeting*, Atlanta, Georgia, USA, July 7-12, 2019 (1 page URSI Abstract).

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Directed Energy Professional Society (DEPS) Annual Science and Technology Symposium, Destin, Florida, USA, April 2019:

[29] Ryan Butler, Mechanical Challenges of Modular Photoconductive Semiconductor Based HPM Sources

[30] Steve Young, Two-Dimensional Optoelectronic Pulsed Power Switches: Initial Effort

[31] Adam Wagner, Rapid Cost Effective RF Component Prototyping Using 3D Printers

[32] Heather Thompson, Cost to benefit analysis of GaN for Photoconductive Semiconductor Switches

[33] Colby Landwehr, Low Leakage Electroluminescence For Improving SiPCSS Hold Off

[34] James Kovarik, Some Investigations Into Applications Of Electrically Small Antennas As Phased Array Elements

[35] Spencer Fry, Maximizing SiPCSS Efficiency For HPM Sources

[36] Deb Chatterjee, Studies On Antenna Characterization And Propagation Of High Power Pulsed Electromagnetic Waves With Minimal Dispersion

***

DEPS Posters and Presentations 2018

[37] Jeff Scully, ElectroLuminescence Studies of Silicon Based Photo-Switches

[38] Cash Hauptmann, Thermal Anlaysis of a PCSS through TCAD Simulation

[39] Nicholas Flippin, Fast Rise Time Switches: Drift Step Recovery Diode

***

DEPS Posters and Presentations 2017

[40] Noah Kramer, Recent Results of Silicon Based Photoconductive Solid State Switches for 500kHz Continuous Pulse Repetition Frequency

14.5 Theses and Dissertations

[1] Jordan N. Berg, “Development of a Jet Impingement Thermal Management System for a Semiconductor Device with the Implementation of Dielectric Nanofluids,” MS Thesis in Mechanical Engineering, University of Missouri-Kansas City, **2021** [mospace].

[2] James C. Kovarik, “Wideband High-Power Transmission Line Pulse Transformers,” MS Thesis in Electrical Engineering, **2021** [mospace].

[3] Wasekul Azad, “Development of Pulsed Power Sources Using Self-Sustaining Nonlinear Transmission Lines and High-Voltage Solid-State Switches,” PhD Dissertation in Electrical Engineering, **2021** [mospace].

[4] Paul Klappa, “Implementation and Assessment of State Estimation Algorithms in Simulation and Real-World Applications,” MS Thesis in Mechanical Engineering, **2021** [mospace].

14.6 IP Disclosures Filed

[1] S. Bellinger, A. Caruso, A. Usenko, US Provisional Patent Application “Stacked Diode with Side Passivation and Method of Making the Same,” 12AUG2021.

[2] S. Bellinger, A. Caruso, A. Usenko, “Diode and Method of Making the Same,” 28JUNE2021.

[3] Bhamidipati, Myers, Caruso, “Multi-Stage Photo-Stimulated WBG-PCSS Driven RF Pulse Generation System Implementing Miniature Optical Sources,” 21UMK009, 04NOV2020.

[4] Shepard, “A Low Noise Optical Amplifier,” 21UMK007, 14SEPT2020.

[5] Shepard, “A Novel Optical Fiber Amplifier,” 20UMK012, 02JUN2020.

[6] Doynov, “High-power High Repetition Rate Microwaves Generation with Differentially Driven Antenna,” 20UMK011, 19APR2020.

[7] Doynov, “Scalable Modular System for High-power Microwaves Generation,” 20UMK010, 19APR2020.

[8] Doynov, “Pulse Differential High-power Microwave Generation,” 19UMK007, 02JAN2019.

[9] Doynov, “Non-linear Network Topologies with Reutilized DC and Low-frequency Signal,” 19UMK008, 28DEC2018.

[10] Doynov, Caruso, “Non-Linear Transmission Line Topologies for Improved Output,” 19UMK005, 28SEPT2018

14.7 Provisional Patents Filed

[1] S. Bellinger, A. Caruso, A. Usenko, US Provisional Patent Application “Stacked Diode with Side Passivation and Method of Making the Same,” filed 09/10/2021.

[2] S. Bellinger, A. Caruso, A. Usenko, “Diode and Method of Making the Same” US Provisional Patent Application 63/216,550, filed June 30, 2021.

[3] P. Doynov, A. Caruso, “High-Efficiency High-Power Microwave Generation using Multipass Non-Linear Network Topologies,” filed 26NOV2019.

[4] Plamen Doynov, James Prager, Tim Ziemba, Anthony N. Caruso, “Non-Linear Transmission Line Topologies for Improved Output”, USPTO Provisional Serial No. 62/737,185, filed 27SEPT2018.

14.8 Non-Provisional Patents Filed

None to date

ONR HPM Program – Monthly Status Report (MSR) – DECEMBER 2021

Anthony Caruso – Univ. Missouri – Kansas City

N00014-17-1-3016 [OSPRES Grant]

ONR Short Pulse Research, Evaluation and non-SWaP Demonstration for C-sUAS Study

15 JANUARY 2021

OSPRES Grant Goal: address and transition technologies and capabilities that enable the OSPRES Grant Objective using the OSPRES Grant Approach, while educating the next generation of pulsed power and defense minded, stewards and innovators.

OSPRES Grant Objective: to execute high-risk, high-payoff efforts that mitigate, fill or rectify one or more grand-challenge or elementary gaps or deficiencies needed to achieve a modular, scalable and electronically steerable high-power microwave (HPM) based defense system for the counter unmanned aerial system (cUAS) mission. The OSPRES HPM system and sub-system development/evaluation efforts are focused on the short-pulse high-average-power space and includes the kill chain considerations including the target and its responsivity to radiofrequency stimuli.

OSPRES Metrics of Success: developed technologies and capabilities that are published in the peer review, protected as intellectual property, and/or, transitioned to the OSPRES Contract effort and beyond for integration with other DoD needs or dual-commercial-use, as enabling/integrable capability(ies).

OSPRES Grant Approach: A fail-fast philosophy is maintained, where if a technology or capability is deemed infeasible to be demonstrated or validated during the project period-of-performance, it shall be culled, results to date and basis of infeasibility documented, and the next major gap/deficiency area addressed by that part of the project sub-team. Students whose thesis depends on following through with a full answer during the life of the award will be given special dispensation to continue their work.

OSPRES Grant Security: All efforts should be fundamental and publicly releasable in nature when taken individually. This report has been reviewed for operational security, compilation, proprietary and pre-decisional information concerns.

1 Contents

2 Executive Summary

2.1 Progress, Significant Findings, and Impact

HV Switch. This subeffort is being closed. Please see the appendix summary report.

Fiber Laser and Optical Amplifiers. Our optical power amplifier tubes enable peak optical power levels on the order of tens of GW (via self-focusing management and by diminishing thermal effects via surface areas of 100x SOTA). We show that smaller diameter (100 micron) optical power tubes, which would be flexible like fiber, can still push the limit imposed by self-focusing to roughly 1/10 GW (10x SOTA) when we use water (rather than air) in the core to compensate for the increased thermal-load caused by the reduction in surface area. Lens and power level optimizations improved the uniformity of the output beam profile for the HPM application; SWaP-C calculations show a laser system cost reduction factor of 83 and 21 (respectively) for a 100 and 12 element Si-PCSS array (at 1 MW optical peak power per switch: 100 μJ/pulse in a 100 ps pulse width).

Laser Diode Array Driver. Avalanche transistors (ATs) have been evaluated to potentially replace GaN-PCSS as the enabling switch for the LDA driver. Due to the current rating and device failure rates, ATs have been deemed unfit to replace GaN-PCSSs. Due to the unavailability of GaN-PCSSs and lack of promising results in finding an alternative switch technology, the LDA driver effort will not be pursued any further. A closeout report will be submitted in the next reporting cycle. On the other hand, the pulse overlaps and peak voltage reduction issues reported in NOV2021 for the 12-segment dynamically tunable FWG have been investigated and will be reported in FEB2022.

On-State Resistance in GaN:X PCSS. A simple, working GaN PCSS model has been built in COMSOL and errors mentioned in last month's report fixed. This model allows for parametric sweep analysis towards minimizing on-state resistance in GaN PCSS devices.

DSRD Optimization Simulations. An automated fitting procedure (processing thousands of LTSPICE simulations) for the LTSPICE DSRD models was developed and used. The automated method: (1) allows a closer curve fitting (ten times less total error over curve) for the forward IV, reverse CV, and reverse recovery tests that is faster to performe (reduced from days to hours per device) and (2) results in device specific (old fittings overlapped devices) model parameterizations that will next be tested in pulser simulations and compared to experiment. More advanced diode models within Smartspice (Philips and HiSIM) are being studied for improved DSRD modeling in reverse IV, breakdown, and recovery.

DSRD Processing and Manufacturing. The processing of Gen2 and Gen3 epitaxy-based DSRD lots continued, with the Gen3 lot reaching the TMAH anisotropic etch step. Several more wafers from the Gen2 lot are finished and have been submitted to the DSRD characterization team for pulsed performance tests. Samples with Pd/Ni electroless plated layers were analyzed with SEM, and the technical feasibility of the electroless plating thus confirmed. Upon analysis of the data, the plating recipes have been adjusted. Samples processed with stain etch for diode side surface passivation have been analyzed

with SEM. Non-uniformity due to hydrogen bubbles sticking to the surface was observed. New experiments to improve uniformity have been planned.

DSRD Design of Experiments. Standard diode testing has been completed for EG1500 and Gen2.1 and most of the deep diffusion DSRDs. A preliminary study showed that repeated measurements will be required due to the variability found within the testing results. The Gen 2.1 DSRDs displayed a higher maximum forward voltage drop and a lower zero-bias capacitance than the EG1500 and the deep diffusion DSRDs. More recovery testing will be necessary to determine better recovery calculations for stacked diodes.

DSRD-Based Pulsed Power Source Optimization. A simplified analytic theory of a MOSFET-driven 1×1 DSRD pulse generator has been presented, which significantly reduced the circuit parameter space to optimize the performance of the pulse generator. With the help of this theory, we demonstrated a simulated output pulse of >26 kV from a single bar pulse generator.

Development of a GaN-Based Power Amplifier RF Source. Reporting on this section has been moved to the PTERA contract.

Diode-Based Nonlinear Transmission lines. A voltage-tunable topology of a high-voltage D-NLTL based on the K100F epoxy diode was simulated in LTspice. Simulations indicate center frequency tuning capabilities from ~1 GHz to ~1.5 GHz using a DC bias range of 0 to +200 V.

Continuous Wave Diode-NLTL Based Comb Generator. Focus in December was placed on simulated line topologies. Simulations were aimed at comparisons with measured results from the R&S amplifier tests in NOV as well as developing line topologies capable of better utilizing both the positive and negative polarity portions of bipolar waveforms. Comparison results indicate that more simulation refinement is required for HV simulations.

Pulse-Compression-Based Signal Amplification. Saturable inductor modeling was explored and initial simulations were realized in LTspice. Magnetic core materials to be used in high-frequency saturable inductors and Rogowski current probes for MPC testing are being investigated.

Antennas. The gain of the previously manufactured 2×2 array of narrowband microstrip patch electrically small antennas (ESAs) was re-measured using carefully calibrated cables, resulting in improved agreement between the simulated and experimental realized gain data. Having achieved a reasonable proof-of-concept, this array design technique will now be implemented for building the final demonstrable prototype at the UHF range.

Seven unique array excitation patterns have been applied to the optimized diamond Koshelev array and the uniform and Gaussian excitation patterns were found to be optimal. The Gaussian pattern yields the optimum field intensity with low-side lobes. The single-element Shark and Koshelev 3D printed prototype testing resulted in good performance at low frequencies (<2 GHz) with problems at high frequencies (>2 GHz) due to fabrication inaccuracies at the feed. On the ML side, we extended the prediction

capability to determine electric fields for monopolar input waveforms of interest as well as improved the RMSE values (<1) for k-nearest neighbor and linear regression ML models for predicting S11 and frequency domain antenna gain of arrays.

RF Coupling. So far, we have used the equivalent circuit approach to study RF coupling to the wiring system of the UAV when the source of excitation is a plane wave originating far from the UAV. However, in many practical scenarios, the UAV carries a payload that contains a radiating antenna. The radiation from this antenna might induce significant coupling to the UAV wires since it is physically much closer. Therefore, this report uses the equivalent circuit approach to study RF coupling to the UAV due to an antenna in its proximity.

UAS Engagement Modeling and Simulation. A high-level model of a close-in weapon system (CIWS) kinetic defender was implemented into the C# library and can now be used to study how kinetic and high-powered microwave (HPM) effectors could be used together.

2.2 Completed, Ongoing, and Cancelled Sub-Efforts

	Start	End
2.2.1 *Ongoing Sub-Efforts*		
GaN:C Modeling and Optimization	OCT 2017	Present
Diode-Based Non-Linear Transmission Lines	FEB 2018	Present
HV Switch Pulsed Chargers	DEC 2018	Present
Trade Space Analysis of Microstrip Patch Arrays	FEB 2019	Present
Enclosure Effects on RF Coupling	OCT2019	Present
Lasers and Optics	FEB 2020	Present
UWB Antenna Element Tradespace for Arrays	MAY 2020	Present
WBG-PCSS Enabled Laser Diode Array Driver	NOV 2020	Present
Si-PCSS Contact and Cooling Optimization	JAN 2021	Present
Drift-Step Recovery Diode Optimization	JAN 2021	Present
UAS Engagement M&S	MAR 2021	Present
DSRD-Based IES Pulse Generator Development	APR 2021	Present
Drift-Step Recovery Diode Manufacturing	MAY 2021	Present
IES Diode Characterization	MAY 2021	Present
Sub-Nanosecond Megawatt Pulse Shaper Alternatives	MAY 2021	Present
Ultra-Compact Integrated Cooling System Development	MAY 2021	Present
GaN-Based Power Amplifier RF Source	AUG 2021	Present
Reconfigurable RF Pulsed-Power Source	AUG 2021	Present
RF Driver Unit for GaN SD-MPM Power Amplifier	SEPT 2021	Present
Reconfigurable RF Antenna for SD-MPM Sources	SEPT 2021	Present
Continuous Wave Diode-NLTL Based Comb Generator	SEPT 2021	Present
2.2.2 *Completed Sub-Efforts*		
Adaptive Design-of-Experiments	OCT 2017	APR 2019
Non-perturbing UAV Diagnostics	OCT 2017	OCT 2018
Noise Injection as HPM Surrogate	OCT 2017	MAR 2019
SiC:N,V Properties (w/ LLNL)	APR 2018	MAR 2019
Helical Antennas and the Fidelity Factor	JUL 2018	SEPT 2019
Si-PCSS Top Contact Optimization	APR 2020	OCT 2020
Nanofluid Heat Transfer Fluid	NOV 2020	JUL 2021
2.2.3 *Cancelled/Suspended Sub-Efforts*		
Ab Initio Informed TCAD	OCT 2017	OCT 2020
Positive Feedback Non-Linear Transmission Line	NOV 2017	DEC 2018
Minimally Dispersive Waves	FEB 2018	SEPT 2018
Multiferroic-Non-linear Transmission Line	NOV 2018	APR 2019
Avalanche-based PCSS	SEPT 2018	SEPT 2019
Gyromagnetic-NLTL	DEC 2017	NOV 2020
Multi-Stage BPFTL	APR 2020	JUL 2020
Heat Transfer by Jet Impingement	MAY 2018	FEB 2021
Si, SiC, and GaN Modeling and Optimization	NOV 2018	FEB 2021
Bistable Operation of GaN	FEB 2021	MAR 2021
IES Pulser Machine Learning Optimization	MAY 2021	AUG 2021

2.3 Running Total of Academic and IP Program Output

See Appendix for authors, titles and inventors (this list is continuously being updated)

Students Graduated	*5 BS, 8 MS, 3 PhD*
Journal Publications	*5 (6 submitted/under revision)*
Conference Publications	*33 (4 submitted/accepted)*
External Presentations/Briefings	*17 (23 submitted/accepted)*
Theses and Dissertations	*4*
IP Disclosures Filed	*10*
Provisional Patents Filed	*4*
Non-Provisional Patents Filed	*0*

3 Prime Power and Conditioning

3.1 HV Switch Pulsed Chargers

(Sarwar Islam and Faisal Khan)

3.1.1 *Problem Statement, Approach, and Context*

Primary Problem: Commercially available high-voltage solid-state switches made by BEHLKE are the best in SWaP-cooling, but are expensive, have long lead times (2–3 months), and are made outside of the US. For the Navy afloat mission to be successful, we need a sustainable supply of US-manufactured switches at a much lower cost.

Solution Space: Design and demonstrate modular high-voltage (~10 kV) and fast (repetition frequency = 100 kHz) solid-state switches using a combination of series- and parallel-connected commercially available inexpensive discrete MOSFETs and custom high-voltage (~10 kV) isolated gate drivers.

Sub-Problem: Voltage balancing among the series-connected MOSFETs, minimization of gate signal delays, cooling of the individual MOSFETs, balancing resistors, high-voltage isolation required for the power supplies, and the controlling pulse width modulated (PWM) signal as well as differential voltage feedback measurement across individual MOSFETs.

State-of-the-Art (SOTA): Direct liquid-cooled solid-state switch from BEHLKE (e.g., HTS-151-30).

Deficiency in the SOTA:

1. BEHLKE-made switches are expensive. For instance, a single HTS-151-30 switch costs around $5,000.
2. BEHLKE switches along with direct liquid cooling units occupy a considerable amount of space. For instance, an HTS-151-30 switch from BEHLKE has a footprint of approximately 225*85*75 mm without considering the liquid cooling system. Some key parameters of this switch are as follows.

   i) Maximum operating voltage = 15 kV

   ii) Maximum continuous load current = 2.52 A (without cooling), 30 A (with liquid cooling)

   iii) Maximum turn-ON peak current = 300 A (pulse width = 200 µs, duty cycle <1%)

   iv) Turn-ON resistance = 1.3 Ω
3. Once the switching frequency is greater than 10 kHz, a liquid cooling system is required to operate the BEHLKE switch.
4. Without liquid cooling, the maximum continuous power dissipation (P_{cont}) of the BEHLKE switch is limited (e.g., for HTS-151-30, P_{cont} is 10 W without liquid cooling).
5. At a higher switching frequency (>20 kHz), the BEHLKE switch requires multiple ancillary DC power supplies, i.e., 5, 15, and 60 V.

6. The switches made by BEHLKE cannot be reconfigured to withstand a higher voltage exceeding their recommended rating. BEHLKE offers separate products to operate them at higher voltage/currents.

Solution Proposed: Designing a modular high-voltage (~10 kV) switch using a single custom isolated gate driver for each module and having a construction cost lower than the BEHLKE switch with equivalent or better performance in all specification categories (Specifications for the BEHLKE switches can be found in the following link: http://www.behlke.com/separations/separation_c4.htm).

Relevance to OSPRES Grant Objective: The proposed modular high-voltage switch is expected to facilitate controlled hundreds-of-nanosecond charging of an array of transmission lines of pulse forming networks to drive an array of PCSSs, thereby producing controlled hundreds-of-picosecond scale high-voltage pulses.

Risks, Payoffs, and Challenges:

I. Lack of rigid control over voltage balancing can lead to a cascaded failure among the series-connected MOSFETs.

II. In the absence of an adequate mitigation scheme, voltage overshoot due to the fast-switching speed can exceed the voltage rating of an individual MOSFET, thereby damaging the switch.

III. At high voltage (~10 kV) and high repetition rate (>100 kHz), mitigating EMI to safeguard the individual MOSFETs from false turn-ON is a major challenge.

3.1.2 *Tasks and Milestones / Timeline / Status*

(A) Design a surface-mount MOSFET-based four-stage switch (6.8 kV rated) and control it using the in-house gate driver, then test its voltage-withstanding ability with a DC supply voltage up to 4–5 kV and evaluate the effectiveness of the thermal management at its current state / DEC 2020 / Completed.

(B) Design and develop a modular HV switch (~10 kV rated) using the concept of the tested four-stage high-voltage switch module and an in-house modular gate driver to drive the modular switch /JAN–FEB 2021 / Completed.

(C) Test the voltage withstanding ability of the modular HV switch with a DC supply voltage up to 10 kV and switching frequency up to 50 kHz using a resistive load (5–10 kΩ) and evaluate the effectiveness of the thermal management at its current state / FEB–SEP 2021 / Ongoing.

(D) Test the isolation capability and evaluate the synchronization accuracy of the gate drive signal generated from the modular in-house gate driver / FEB–SEP 2021 / Completed.

(E) Encapsulate the gate driver board with potting material with a high (~15–20 kV) breakdown voltage rating to prevent possible flashover/arcing in between the HV switch and this board / MAR–SEP 2021 / Ongoing.

(F) Design and fabricate a compact power conditioner circuit based on a 12 kV rated SiC switch made by BEHLKE (HTS 121-15) / APR–MAY 2021 / Completed.

(G) Test this modular HV switch coupled with a Si PCSS device up to a DC supply voltage of 5–6 kV and a switching frequency of 50 kHz / SEP 2021/Ongoing.

(H) Design and develop a 20 kV rated modular (two modules, each with four MOSFETs) HV switch based on the design concept of the 10 kV rated modular switch using 3.3 kV rated SiC MOSFETs (new product made by GeneSiC Semi) / Ongoing.

(E) Design and develop a 20 kV rated modular gate driver based on a WPT based planar transformer topology to ensure adequate galvanic isolation (~30–40 kV) for the power supplies of the gate driver / Ongoing.

3.1.3 *Progress Made Since Last Report*

(A) After successfully testing the system at 10 kV we began redesigning the MOSFET board with 3300V MOSFETs (G2R1000MT33J) to achieve 13.2kV per module and 26.4 kV for the complete setup.

(B) We plan to redesign the gate driver unit to withstand such voltage levels. A few parts of the gate driver of the prior design were directly taken from the literature. Additionally, we started to simulate gate drivers under different operational conditions in order to achieve optimum performance.

3.1.4 *Summary of Significant Findings and Mission Impact*

(A) The 6.8 kV rated four-stage surface-mount MOSFET developed in-house was successfully tested up to a DC supply voltage of 4 kV and at a switching frequency up to 20 kHz with a 3.2 kΩ resistive load. The proposed voltage balancing method achieves <1.1% voltage mismatch under steady-state and switching transitions.

(B) A modular (two modules) 10 kV rated HV switch has been designed and a prototype has been developed using 1.7 kV rated SMD MOSFETs (C2M1000170J). An in-house 10 kV rated HV gate driver has been designed and incorporated with the HV switch to drive it. A manuscript on the HV switch and the custom isolated gate driver has been submitted to IEEE Transaction on Power Electronics.

(C) An insulating naphthenic dielectric oil has been acquired that meets the ASTM D-3487 specification. With the use of this dielectric oil, altered component placement and new TX-RX optical module, the newly designed gate driver and MOSFET PCB can safely withstand 10 kV. At present, the prototype runs at Fsw = 1 kHz, d = 15%, V_{DC} = 10 kV, and R_{load} = 300 kΩ. We are yet to test the circuit at 50 kHz switching to complete Task (C). We need to test the circuit at much higher load current (load impedance = 5–10 kΩ), and we plan to do so in January. Our present setup, especially the HV power supply, limits us to test the circuit at significantly smaller load current.

(D) At 10 kV, the gate driver circuit operates flawlessly, and the gate-source signals have the necessary integrity to avoid malfunctions.

(E) The entire circuit assembly including the driver PCB was immersed in naphthenic dielectric oil to prevent any unwanted arcing through air, although the final design will use some sort of potting materials for packaging ease. The system has been tested up to 10 kV, and we are yet to test the oil's dielectric strength at 20 kV.

4 Laser Development

4.1 Fiber Lasers and Optical Amplifiers

(Scott Shepard)

4.1.1 *Problem Statement, Approach, and Context*

Primary Problem: High-average-power 1064-nm picosecond lasers are too large (over 1100 cm^3/W) and too expensive (over \$1000/μJ per pulse) for PCSS (photoconductive semiconductor switch) embodiments of HPM-based defense systems. For example, a laser of this class might occupy a volume of 1 m x 30 cm x 30 cm = 90,000 cm^3 and provide an average power of 50 W (thus, 1800 cm^3/W). Costs in this class range from \$100K to \$300K to drive our Si-PCSS applications.

Solution Space: Optically pumped ytterbium-doped optical fiber amplifiers, fed by a low-power stable seed laser diode, can offer a cost-effective, low-weight, and small-volume solution (with respect to traditional fiber and traditional free-space laser designs). Moreover, our novel optical amplifier tubes, might operate at far higher power levels (over 1000 times greater), thus driving an entire array of PCSS with a single amplifier and thereby reducing the overall system costs and eliminating the optical pulse-to-pulse jitter constraints.

Sub-Problem (1): Optical pump power system costs account for over 50% of the budget for each laser (in this class, for normal/free-space, optical fiber, and tubular embodiments).

Sub-Problem (2): Fiber (as well as power tube) optical amplifier performance is degraded primarily by amplified spontaneous emission (ASE) noise, which limits the operating power point, and by nonlinearities, which distort the optical pulse shapes.

State-of-the-Art (SOTA): Free-space NdYAG lasers or Ytterbium-doped fiber amplifiers optimized for LIDAR, cutting, and other applications.

Deficiency in the SOTA: Optical pump power system costs (in either free-space or fiber lasers) are prohibitive for the PCSS applications until reduced by a factor of at least two.

Solution Proposed: Fiber lasers permit a pre-burst optical pumping technique (wherein we pump at a lower level over a longer time) which can reduce pumping costs by a factor of at least ten. To address the ASE and nonlinear impairments, we are pursuing the use of gain saturation and a staged design of different fiber diameters. We also apply these techniques to fiber amplifiers which incorporate our power amplifier tube in the final stage. The inclusion of our novel tubular-core power amplifier stage should permit a single laser to trigger an array of several PCSS (reducing system cost and mitigating timing jitter).

Relevance to OSPRES Grant Objective: The enhancement in SWaP-C^2 for the laser system enables PCSS systems for viable deployment via: a factor of 40 in pumping cost reduction of each laser; and a factor of *N* in system cost reductions as a single laser could drive *N* (at least 12) PCSS in an array, while also eliminating the optical jitter constraints.

Risks, Payoffs, and Challenges: Optically pumping outside the laser pulse burst time can enhance the ASE; pump costs could be reduced by 40, but ASE in the presence of dispersion and/or nonlinearities could enhance timing jitter thereby limiting steerability. The main challenge for power tube implementation is the entrance optics design.

4.1.2 *Tasks and Milestones / Timeline / Status*

(A) Devise a pre-burst optical pumping scheme by which we can reduce the costs of the laser by a factor of two or more and calculate the resulting increase in ASE. / FEB–JUL 2020 / Completed.

(B) Reduce the ASE via gain saturation. / Oct 2020 / Completed.

(C) Design saturable gain devices which avoid nonlinear damage. / Ongoing.

(D) Calculate and ensure that timing jitter remains less than +/-15 ps with a probability greater than 0.9. / Ongoing.

(E) Demonstrate a cost-reduced fiber laser. / Ongoing.

(E1) **March 2021** Finalize design. / Completed.
(E2) **April 2021** Assemble and test-check seed LD (laser diode)/driver. / Completed.
(E3) **April 2021** Measure power vs current transfer function of seed LD/driver. / Completed.
(E4) **May–July 2021** Measure ASE and jitter of 1064 nm seed LD/driver. / Completed.
(E5) **May–July 2021** Measure ASE and jitter of 1030 nm seed LD/driver. / Completed.
(E6) **June–July 2021** Assemble and test-check pump LDs/drivers. / Completed.
(E7) **June–July 2021** Measure power vs current transfer function of pump LDs/drivers. / Completed.
/ (E8) – (E14) Delayed due to vendor issues (see MAY MSR).
(E8) **September 2021** Splice power combiners to Yb doped preamp fiber. /Completed.
(E9) **September 2021** Connect seed and pumps to power combiners and test-check. / Completed.
(E10) **September–October 2021** Measure gain, ASE and jitter of 1064 nm preamp assembly (forward, backward and bidirectional pumping) as a function of pump power and duty cycle. / Partially complete.
(E11) **September–October 2021** Measure gain, ASE and jitter of 1030 nm preamp assembly (forward, backward and bidirectional pumping) as a function of pump power and duty cycle. / Partially complete.
(E12) **November 2021** Splice power amplifier and its power combiner to best preamp. / Ongoing (delay due to vendor error).
(E13) **November–December 2021** Measure gain, ASE and jitter of entire amp assembly. / Ongoing (delay due to vendor).
(E14) **December 2021** Analyze data and document. / Ongoing (delay due to vendor).

(F) Design a new type of higher power, tubular core fiber amplifier. / Ongoing.

(F1) Apply one high-power tubular amplifier to a system comprised of an array of several (say N) PCSS. For example: N=12 in a 3x4 array (or 4x4 array with corners omitted) N=16

in a 4x4 array, etc.; thereby eliminating jitter constraints and reducing laser system cost by more than a factor of 100 (independent of burst profile). / Ongoing.

4.1.3 *Progress Made Since Last Report*

(E13–E14) The fastest way to compensate for a vendor (Coherent/Nufern) error is our revised plan of progressively cutting the 8 meter fiber down to shorter lengths. The fiber cleaver required to do this however has been delayed in shipping. Considerable effort was spent (involving four different sales reps) in trying to remedy this, but Thorlabs insists that the supply chain failure due to Covid means that part cannot be shipped per the original schedule. Rather than risk damage to the entire fiber amplifier (which could occur from reflections off an improper cleave) we have decided to wait the remaining two weeks.

(F) Since hollow-core photonic crystal fibers (PCFs) are similar to (but of smaller diameter than) our optical power tube we considered smaller diameter tubes. Smaller diameter tubes would be flexible like fiber and fit the tooling of current manufacturing (without customization) but these would diminish the thermal benefits of increased surface area (by 50). To compensate for the loss of thermal advantage we consider the use of water (rather than air) in the core of smaller diameter tubes. We find the limit imposed by self-focusing is roughly 1/10 GW in the core and 1 MW in the cladding (for the smaller, 100 micron, water-core diameter) compared to tens of GW (achievable in a 5 mm air-core diameter).

(F1) In the HPM application we want the output beam profile to be more uniform than Gaussian (to simplify a passive power splitter design – the multiple legs of which further aid in uniformly illuminating a PCSS). We improved uniformity by adjusting the operating point (power level of the tube) with a simple lens implementation of the entrance optics.

(F1) For the HPM application of the optical power tube as a single laser to drive an array of Si-PCSS (in linear gain mode, requiring an optical peak power of 1 MW/switch) we calculated the SWaPC improvement factors, for a 100 element and 12 element array.

Relative to SOTA (a system of free-space lasers) we find:

at 100 elements => laser cost reduced by a factor of 83; size and weight reduced by 290

at 12 elements => laser cost reduced by a factor of 21; size and weight reduced by 35.

(F1) We disseminated recent results to NRL fiber laser experts (with whom we have already met) and they again expressed an interest in partnering on this technology.

4.1.4 *Technical Results*

(F) We considered smaller diameter power tubes (50 to 90 micron core radius, rather than 2.5 mm) because these would be flexible like fiber and would immediately match the tooling of current manufacturing. But these would greatly diminish the thermal benefits of increased surface area (reducing our factor of 100 to a factor of 2). To compensate for the reduced thermal advantage we consider the use of water (rather than air) in the core of smaller diameter tubes. Water is a natural choice when designing for Si-PCSS since it has a transmission window near 900 nm where the responsivity of silicon has its peak (as

shown in the refractive index plot of Fig. 4.1.1, where the red curve is proportional to the attenuation of light in room temperature water).

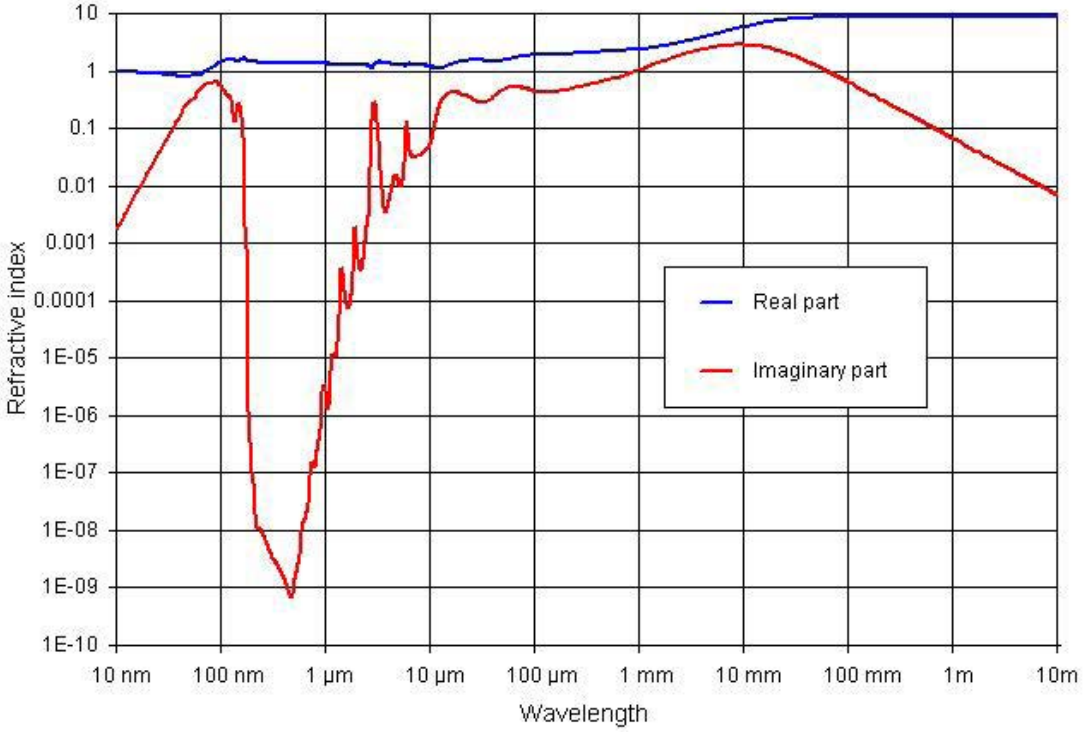

Fig. 4.1.1. Refractive index of room temperature water (absorption proportional to imaginary part in red).

The operating point of the glass tube amplifier, Pin.clad, has a breakpoint (a half-power point, beyond which the power in the amplifier drops) which is shown in Fig. 4.1.2 for various core radius and entrance-optics lens focal lengths, f (in mm). We see that for Rcore = 50 microns we can achieve a 1 MW operating point, which drops to below 1 kW at Rcore = 90 microns. The effects of the lens on this mode-coupled nonlinear device are not yet fully understood (although we are analyzing cutline data along the longitudinal direction in attempts to do so) but in most cases the longer focal length is preferable.

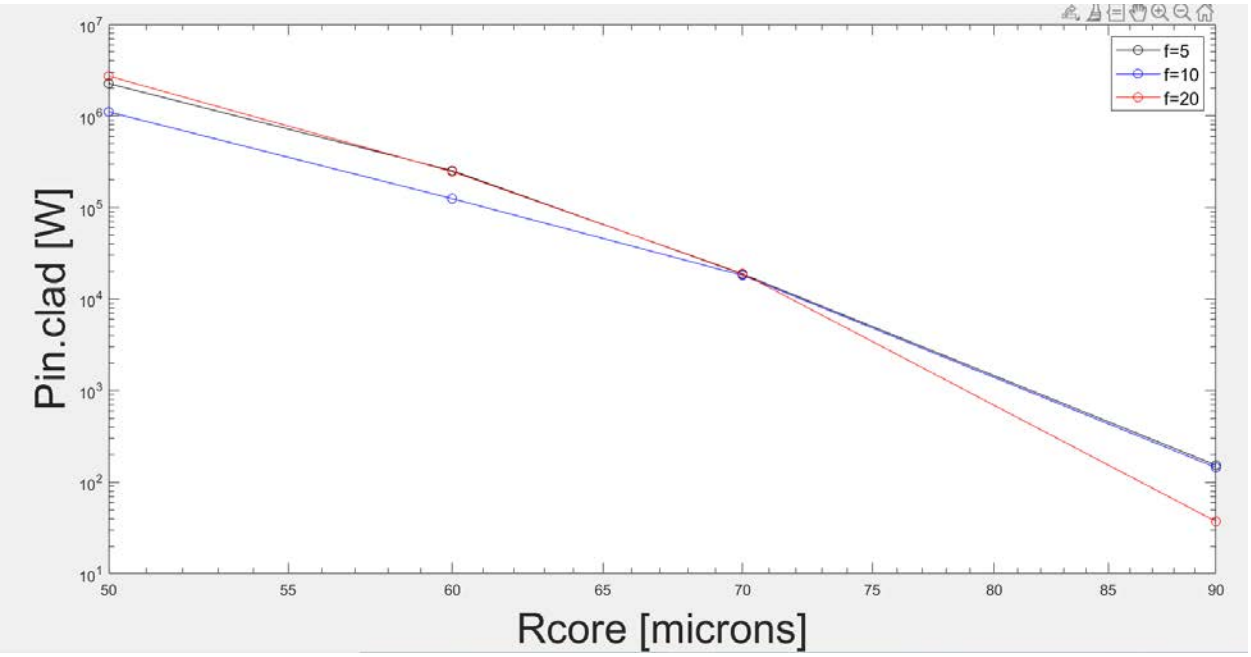

Fig. 4.1.2. Amplifier breakpoints vs core radius of a water filled glass tube.

Fig. 4.1.3 shows the optical power coming out of the water filled glass tube, Pout.core, corresponding to each of the breakpoints of Fig. 4.1.2 and we see that the core can deliver powers above 1/10 GW for Rcore = 50 microns (dropping to 6 MW at Rcore = 90 microns). These results indicate the potential exists for such embodiments, which could become competitive with respect to the larger diameter tubes if the heat transfer into flowing water can compete with the heat transfer from their larger surface area (which remains to be seen).

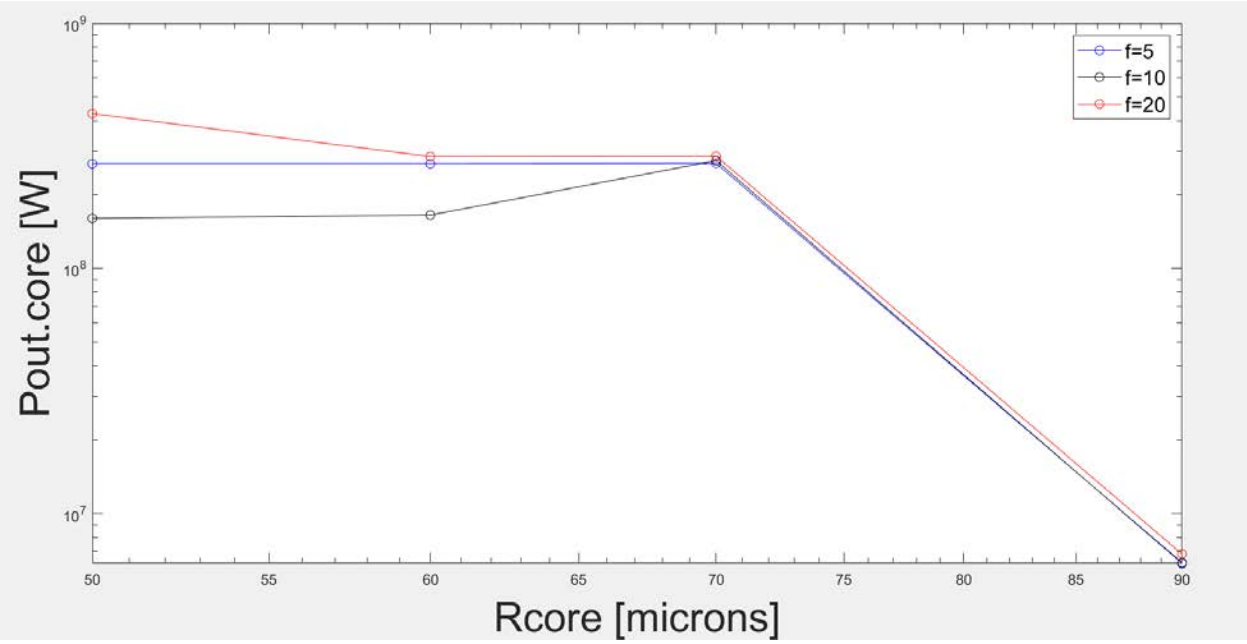

Fig. 4.1.3. Core output power vs core radius of a water filled glass tube.

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(F1) In the HPM application we want the output beam profile to be more uniform than Gaussian (to simplify a passive power splitter design – the multiple legs of which further aid in uniformly illuminating a PCSS). In a continued effort to also use a simple lens implementation of the entrance optics, we found an improved uniformity as shown in the red curve (at input intensity I0 = 2.5E19 [W/cm^2]) of Fig. 4.1.4. Note that the intensity can control the beam profile. In many such cases we obtain a flat-top Gaussian by operating slightly above breakpoint – which unfortunately also reduces the output power. We have yet to obtain the combination of uniformity and power desired, but progress is being made.

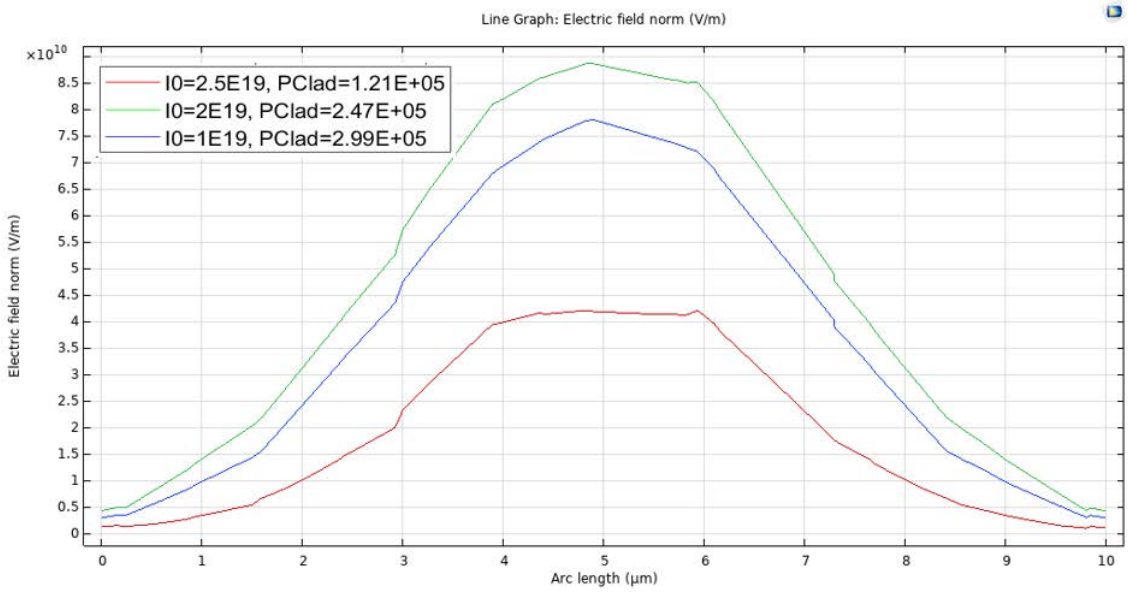

Fig. 4.1.4. Electric field output distribution for a lens fed power tube.

(F1) To calculate specific SWaPC improvement examples for the use of a single optical power tube to drive an array of PCSS (relative to a normal free-space implementation of the laser system) we must consider the PCSS technology and the optical pump powers. The PCSS technology used will set the laser requirements, which often border on the prohibitive. Avalanche mode (a.k.a. high gain or lock on) GaAs PCSS have been pioneered at Sandia [1] to address the laser cost issue. Although these can be triggered with less energy per pulse (which also diminishes the SWaPC of the laser) avalanche breakdown is a statistical process which leads to jitter and it creates filaments (preferred current paths) which diminish the lifetime of the switch in terms of shots fired before failure. Modeling and performance of wideband gap materials (SiC and GaN) continues to progress [2] but these are plagued by manufacturability issues. Thus, we design our power tube for linear mode Si-PCSS at 1064 nm, requiring 100 [μJ/pulse] in a 100 [ps] pulse width, resulting in peak power of 1 [MW] per Si-PCSS. Although simulations predict our power tubes can operate at ones to tens of GW, we will conservatively calculate the improved SWaPC for a 100 MW peak power (100 element array) and a 12 MW peak power (12 element) system. We also assume a pulse rep. rate of 500 kHz (so the average

laser power for each element is 50 [W]). One such normal (free-space) laser could cost ~ $144,000 and occupy ~ 900,000 [m^3].
Relative to SOTA (a system of free-space lasers) we find:
at 100 elements => laser cost reduced by a factor of 83; size and weight reduced by 290
at 12 elements => laser cost reduced by a factor of 21; size and weight reduced by 35.

4.1.5 *Summary of Significant Findings and Mission Impact*

(A) Our pre-burst optical pumping scheme simulations showed that we can drop the pump power costs by a factor of 40 with pre-burst ASE power levels below the heating level tolerance of 100 μW. UMKC invention disclosure filed 02JUN2020.

(B) For a proposed system gain of 8 million, a linear gain theory predicted the in-burst ASE would be over our heating level spec. by a factor of 3960, but by exploiting the nonlinearity of gain saturation we find that we can suppress the ASE by over 7000. UMKC invention disclosure filed 14SEP2020.

(C) Achieved initial practical device designs that exploit gain saturation, which remained below damage thresholds, via staged designs of different mode diameters NOV2020.

(D) Models of the impact of ASE on timing jitter in the presence of dispersion and/or nonlinearities were established JUL2020.

(E) The design of a proof-of-concept experiment demonstrating a cost-reduced optical pumping scheme was finalized MAR2021.

(F) We made (to our knowledge) the first observation of self-focusing effects that are not determined by beam power alone. We found instead that these can also be controlled via the geometric factors within a waveguide (such as fiber core diameter) MAY2021.

We additionally made (to our knowledge) the first observation that a mode exists in the air within a simple glass tube into which we can couple energy from the mode in the glass. Thus, an amplifier (in the doped and pumped glass) can operate at higher powers JUNE2021.

We found conditions under which 0.25 GW of power can exist in the tube's air-core mode when its glass-cladding mode is at a power level near 0.5 GW JULY2021.

Advancements in the very high-power operating point (tens of GW) of our tubular optical amplifier (and the existence, size and spatial uniformity of its air-core mode) were shown to permit a single laser to trigger an array of several (up to 100) Si-PCSS – reducing the laser system cost and eliminating the optical timing jitter constraint. The symmetry breaking of the scattering from self-focusing in a curved waveguide was shown to enable such AUG2021.

4.1.6 *References*

[1] F. J. Zutavern, et al., "Photoconductive Semiconductor Switch (PCSS) Recovery," Distro A, ADA639129 (1989).

[2] J. S. Sullivan et al., "Wide Bandgap Extrinsic Photoconductive Switches," IEEE J. Plasma Sci., **36**, 5 (2008).

4.2 WBG-PCSS Enabled Laser Diode Array Driver

(John Bhamidipati)

4.2.1 *Problem Statement, Approach, and Context*

Primary Problem: Need for heavy (~125 lbs.), bulky (~10 cu-ft), and expensive (~$120,000) conventional laser systems (1064 nm) in photoconductive-semiconductor-switch (PCSS)-based HPM applications, with an additional need for second and third harmonic generation (SHG/THG) optics to trigger wide bandgap (WBG) solids (GaN/SiC).

Solution Space: Design and implement a compact, lightweight, and inexpensive alternative for conventional high average power optical trigger (laser) system using component-level optical source(s) enabled by nonlinear solid-state source drivers to improve SWaP-C^2 index of HPM systems.

Sub-Problem: Unavailability of commercial-off-the-shelf (COTS) optical sources capable of sub-nanosecond pulse widths and tens-of-μm beam width, delivering >1-Watt power to implement as a makeshift/turnkey solution for the laser system.

State-of-the-Art (SOTA): Industrial SOTA Nd:YAG master oscillator power amplifier (MOPA) based 1064 nm picosecond lasers for high average power picosecond pulsed lasers available up to 50 W output power with a gain factor up to 40 dB (~10,000x power) with laser amplifier. On the other hand, 1030 nm fiber lasers in the same power class are available up to 200 W output power.

Deficiency in the SOTA: While high average power MOPA-based lasers and fiber lasers are capable of delivering >200 μJ pulse energies at sub-ns pulse widths, they are bulky, expensive, and nonmodular in terms of wavelength (1064/1030/2050 nm), raising a need for either total laser swap or additional optics for SHG/THG generation when alternative wavelengths are needed by the application.

Solution Proposed: Multi-stage laser diode array (LDA) driver enabled by a seed-laser-diode-driven avalanche WBG-PCSS as a compact (~1.1 cu-ft), lightweight (10–15 lbs.), and inexpensive (<$15,000) optical source replacement. This enables wavelength modularity in the optical source by facilitating the LDA module swap to accommodate the wavelength requirement of the application.

Relevance to OSPRES Grant Objective: Provides an enhanced SWaP-C^2 compliant solution for the laser (optical trigger) subsystem, with a subsequent impact on overall HPM system cost, volume, and power (optical and electrical) requirements.

Risks, Payoffs, and Challenges: Complex interconnect and thermal management system (TMS) design at high temperature (130–175°C) operation; unavailability of COTS high power pulsed laser diodes could potentially raise a need for research in laser diodes (arrays).

4.2.2 *Tasks and Milestones / Timeline / Status*

(A) Complete initial feasibility study for the cascaded multi-stage optical amplifier design and determine functional requirements for the laser diodes (arrays) and source driver [DEC–JAN 2020 / completed].

(B) Complete initial stage experimental implementation of the PCSS-based driver and demonstrate positive current gain using GaN-PCSS, triggered with a 404 nm laser diode. [DEC 2021–JAN 2022 / in progress].

(C) In addition to (B), investigate potential alternatives to GaN-PCSS in both PCSS and non-PCSS domains. [NOV–DEC 2021 / completed].

(D) Define performance metrics for PCSS-based driver and complete numerical calculations for required output current at each stage and corresponding PCSS (GaN/GaAs) operating voltages in light of electric fields required for lock-on/avalanche mode, establish real-time implementation timeline, cost estimates, jitter limitation, and explore ways to protect LDA from PCSS ringing. [MAR 2021 / partially complete / revisit after completing (B)].

(E) Demonstrate a SiC-MOSFET-powered frozen wave generator (FWG) prototype on a custom-built PCB with Cree/Wolfspeed MOSFET(s), and 50 Ω coaxial cables and/or microstrip transmission lines capable of generating chirped pulse widths. [JUL–AUG 2021 / complete].

(F) Demonstrate a MOSFET-enabled motorized FWG on a 4″ ´ 5″ PCB to enable dynamic pulse width tunability using lumped-element-based transmission lines [NOV–DEC 2021 / partially complete].

(G) Proof of concept testing of the two-stage PCSS-enabled driver system with a 50 Ω load at 1 kHz pulse repetition rate (PRR) [NOV–DEC 2021 / incomplete].

(H) Working prototype demonstration at ~MHz PRR with laser diode array/stack and ancillary optics based on HPM source driver needs including thermal management system (TMS). [JAN–FEB 2022].

4.2.3 *Progress Made Since Last Report*

(C) Avalanche transistors (ATs) rated for 80 V and capable of 80 A maximum peak avalanche currents have been evaluated against the identified performance metrics for the enabling switch in terms of on-state resistance, rise-time, and output current. Though the current rating of the AT is comparable to the application needs, the devices exhibit high failure rates due to thermal runaway, limiting the operational PRR to a few kHz.

(F) We continued testing the dynamically tunable 12-segment lumped-element-based FWG prototype to investigate the root cause(s) for partial pulse overlap as well as the consistent drop in peak voltages from TL #1 to TL #6 under balanced load. The root cause for the pulse overlap was determined and a hypothesis has been made for the observed voltage drop. Based on the hypothesis, a design change in the FWG will be implemented in the next prototype.

4.2.4 *Technical Results*

(C) ATs have been evaluated against the performance metrics determined for the enabling switch of the LDA driver in terms of output current, risetime, and pulsewidth. Though the transistors are rated for 60 A peak currents with 80 V hold-off, the ATs are

highly susceptible to device failure due to thermal runaway owing to their packaging and <150°C safe operating temperature. Furthermore, the requirement of 120 A by the LDA requires paralleling the ATs with capacitive coupling, increasing the chances of device failure.

(F) The chirp-capable and dynamically tunable 12-segment lumped-element-based FWG shown in Figure 4.2.1 has been tested to investigate the root cause(s) for the pulse overlap, consistent drop in the peak voltages from TL #1 to TL #6 under balanced load, and direct impact of LC parameter tuning on peak voltage observed and reported in the previous cycle. Upon troubleshooting, it was noticed that a few variable capacitors used in the transmission line segments were damaged due to overvoltage during the initial testing, which could have potentially caused short circuits that led to delayed charge/discharge of transmission lines, resulting in pulse overlap. The damaged capacitors, however, are obsolete in the market, raising a need to look for alternatives to address the issue. The voltage drop across the pulse train was initially attributed to the inability of the MOSFET to switch the transmission lines simultaneously. However, another hypothesis about the effect of the distance to the transmission line segments from the MOSFET is also being considered. A design change will be implemented in the next prototype iteration to address these issues. Despite the design modification, if the MOSFET is unable to simultaneously switch the lines, an alternative switch technology will be considered.

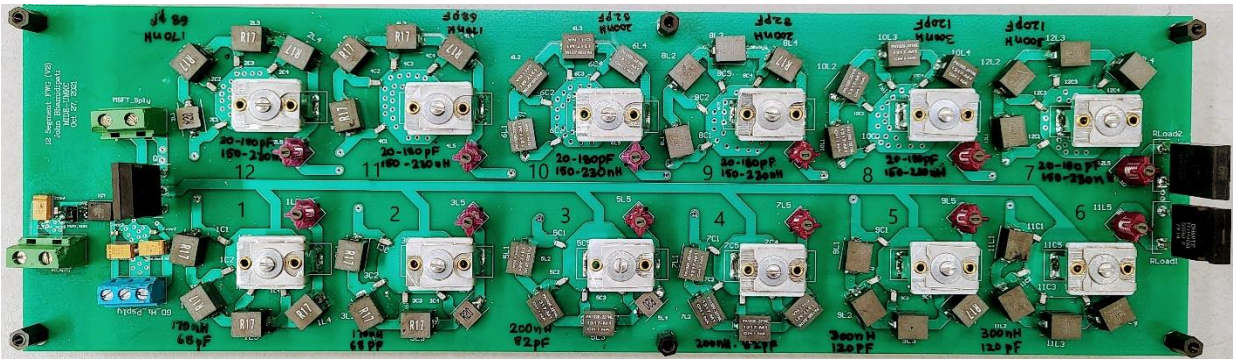

Figure 4.2.1. 12-segment lumped-element-based dynamically tunable FWG prototype with one pair of tunable L–C components per transmission line.

4.2.5 *Summary of Significant Findings and Mission Impact*

(A) The state-of-the-art COTS laser driver specifications and limitations have been comprehensively studied, and target performance metrics have been determined in terms of output current (>120-A), pulse repetition rate (>1-MHz), transient response (<200-ps risetime and <1-ns pulse width), and volume (<0.75 cu-ft). A preliminary feasibility study has signified the need for lock-on conduction mode with ~$10^{2.6}$ gain factor to drive at >1-MHz pulse repetition rate while limiting the amplification stages to 2. This reduces monetary costs to 10–12% of the conventional laser system, while achieving the expected goal of miniaturizing the optical subsystem by 90%.

(B) Pulse trigger requirements for the LDA/LDS have been identified based on Jenoptik's actively cooled quasi continuous wave vertical diode laser stacks to tailor the device parameters of the enabling switch accordingly.

(C) Si optodiodes, Si-PCSS, and ATs have been evaluated against the identified performance metrics for the enabling switch. The photoconductive device testing was performed at ≤200 V charge voltage with laser illumination energies between 20-μJ and 200-μJ and AT testing was performed at 80 V bias (rated voltage). The PCSS and AT performance at low optical energies (~20-μJ) and <100 V bias, respectively, did not satisfy the expected metrics in terms of on-state resistance, output current, and risetime. We continue to study GaN-PCSSs theoretically to understand factors contributing to avalanche (current gain) conduction and in parallel experimentally evaluate electrically triggered switch technologies like silicon avalanche shapers to determine their ability to meet the target metrics. Due to lack of promising results and it not being on the critical path for OSPRES, this sub-project will not be pursued further. A comprehensive report of the effort will be submitted in the next report cycle.

(D) Numerical calculations have been completed to estimate the electric fields and corresponding voltage bias required to induce lock-on operation while exploring ways to minimize the potential risks of high jitter at ~MHz order PRR switching, power reflections due to impedance mismatch, and negative ringing currents during PCSS recovery. Expected on-state resistance and power dissipation for 50 μm and 100 μm devices in lock-on conduction mode have been calculated to estimate cooling system requirements while retaining the expected SWaP-C^2 factor.

(E) A MOSFET-switched FWG prototype implementing coaxial transmission lines has been fabricated and tested with a goal to demonstrate a tunable pulse generator capable of demonstrating chirped pulse-widths. The primary operation of a FWG has been demonstrated with up to 8 transmission line segments under balanced and unbalanced load configurations. The experimental implementation results on pulse chirp were found to be in agreement with the simulation results. However, pulse overlap, and deconstructive interference were observed in the 8-segment configuration, which will be addressed using a different transmission line topology/configuration.

(F) Tunable lumped-element-based (LC) ladder networks were considered as a potential alternative to overcome the non-ideal characteristics of coaxial lines in terms of size and weight. This also provides an advantage of integrating the transmission lines into the PCB, minimizing the distance between the switch (MOSFET) and charged lines. A 12-segment FWG capable of dynamic tunability has been demonstrated with LC ladder networks as lumped-element-based transmission lines on a 4.1″ × 14.1″ PCB under balanced and unbalanced load conditions. Upon testing, consistent reductions in peak voltage across the pulse train as well as pulse overlap have been observed. A reduction in the peak voltage output has been observed as the pulse train progresses, which has been attributed to the ability of the MOSFET to switch all 6 pairs of transmission lines simultaneously. Also, the distance to the transmission line segments from the MOSFET is also considered a potential reason. If this is validated, creates the need for a faster switch/technology alternative to facilitate simul-

switching. Upon troubleshooting, it was determined that the damaged variable capacitors due to overvoltage during initial testing may have potentially caused short circuits that impacted transmission line charge–discharge cycles, resulting in pulse overlap. Variable capacitors with higher voltage rating will be implemented in the next prototype to address this issue.

4.2.6 *References*

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[3] C. V. Reddy, K. Balakrishnan, H. Okumura, *and* S. Yoshida , "The origin of persistent photoconductivity and its relationship with yellow luminescence in molecular beam epitaxy grown undoped GaN" , Applied Physics Letters 73 , 244-246 (1998) https://doi-org.proxy.library.umkc.edu/10.1063/1.1

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[6] M. L. Forcier, M. F. Rose, L. F. Rinehart, and R. J. Gripshover, "Frozen-Wave Hertzian generators - Theory and applications", in 2nd International Pulsed Power Conference, 1979, pp. 221–225.

5 Photoconductive Switch Innovation

5.1 Characterizing and Optimizing On-State Resistance in GaN:X PCSS

(Heather Thompson)

5.1.1 *Problem Statement, Approach, and Context*

***Primary Problem*:** Traditionally, RF generation using photoconductive semiconductor switches (PCSS) relies on materials such as silicon (Si) or gallium arsenide (GaAs), due to their availability and low cost; however, as these applications begin to require higher operating frequencies, powers, and temperatures, with the same or reduced system form-factor, the theoretical operating limits of these materials are being reached.

***Solution Space*:** By exploiting the 3.4 eV bandgap, 1000 cm^2/Vs electron mobility, and thermal properties of GaN, it is possible to realize pulsed-power applications requiring up to a 5 MV/cm critical field, high-frequency operation, and ~400 °C operating temperature, respectively.

Sub-Problem: One of the most important problems in minimizing conduction losses, maximizing efficiency, and reducing thermal issues in compensated, semi-insulating GaN:X (i.e., GaN:X with X=C, Fe…) PCSS-based systems is achieving <1 Ω on-state resistance by optimizing the modifiable parameters of GaN:X at the material, device, and system levels, while still maintaining quick switch turn-off time and low turn-off losses.

***State-of-the-Art (SOTA*):** PCSS-based RF generation systems using Si, SiC, or GaAs can achieve MW-range output power, ones-of-gigawatts frequency content, and electrical efficiency of ~60% that require increased laser energies and device size to reach maximum efficiency and necessary operating power limits, respectively.

***Deficiency in the SOTA*:** Si-, SiC-, and GaAs-based PCSS require ones-of-mJ of incident laser energy to achieve <1 Ω on-state resistance, leading to increased incident laser requirements, increased heating in devices, and devices that are ones-of-cm^2 in area for the necessary peak power and operating temperatures.

***Solution Proposed*:** Use simulation and available experimental results, from literature and collected results at UMKC, to optimize the variable parameters of GaN:X PCSS to achieve <1 Ω on-state resistance with increased electrical and optical efficiency while maintaining a quick switch turn-off time and low turn-off losses.

Risks, Payoffs, and Challenges:

***Challenges*:** The high cost of material leads to a limited number of devices available for experimental testing and analysis, requiring a majority of the optimization studies to be performed using simulation software (COMSOL and TCAD).

***Risks*:** Simulation results may vary from experimental results for certain PCSS parameters due to certain photogeneration and recombination parameters not being included in models along with non-ideal, real-world experiments requiring additions such as encapsulation material or other changes not fully addressed in simulation.

***Payoffs*:** By minimizing the conduction losses in GaN PCSS, a compact, tunable RF source can be realized with increased efficiency and SWAP-C^2 capabilities.

5.1.2 Tasks and Milestones / Timeline / Status

(A) Milestone – Determine material, device, and system parameters that affect on-state resistance and which of these can be best leveraged to reduce on-state losses and heating [*Estimated completion by DEC 21*].

1. Task – Literature study of photoelectric on-state resistance to understand how this parameter can be optimized to reduce conduction and on-state losses during PCSS operation *[ongoing].*
2. Task – Literature review of on-state resistance studies performed using GaN-based photoelectric devices to determine areas to further study *[ongoing].*
3. Task – Determine project milestones, tasks, and timeline for optimizing on-state resistance in GaN PCSS *[JAN 21]*.

(B) Milestone – Build model of GaN PCSS in TCAD and/or COMSOL to begin simulation studies *[OCT–NOV21].*

1. Task – Build simple, working GaN PCSS model to alter for more complex analysis of on-state resistance *[Complete]*.
2. Task – Compare simulation results with available experimental results to determine validity of models using COMSOL *[JAN–FEB 22]*.
3. Task – Set up parametric sweep studies in COMSOL *[MARCH 22]*.

(C) Completion of manuscript on optimizing on-state resistance in GaN:C PCSS *[Ongoing]*

5.1.3 *Progress Made Since Last Report*

(A) Literature pertaining to on-state resistance in opto-electric devices, of various semiconductor materials is being analyzed to determine the parameters at the material, device, and system levels that affect on-state resistance and how these can be altered towards minimizing on-state resistance in GaN:C PCSS thus reducing on-state losses and improving efficiency. A collection of experimental results from on-state resistance studies, of both GaN and non-GaN based PCSS devices, found in the literature is being organized in Excel to allow for analysis and for use in comparison to simulation results.

(B) Errors in COMSOL modeling of GaN PCSS have been fixed, and a simple, working model achieved. This model will be further altered to accurately simulate the correct doping scheme and optical transitions within the device towards allowing for parametric sweep studies showing how device and material alterations (i.e. incident wavelength, doping concentration, device geometry…) affect PCSS performance.

(C) Work on a manuscript focused on minimizing on-state resistance in GaN:C PCSS continued and will serve to direct needed simulation and experimental analysis throughout the project.

5.1.4 *Technical Results.*

(A) There are several parameters (Figure 5.1.1) that affect the on-state resistance of opto-electric devices at the material (bandgap, necessary activation energy, compensation concentrations, etc.), device (geometry, illumination location, etc.), and system (incident photon source characteristics, encapsulation material, etc.) levels that can be altered to minimize on-state resistance, with certain parameters being more easily manipulated than others. Review of on-state state resistance in non-optically gated GaN-based devices is being analyzed as more work towards minimizing on-state resistance has been done in HEMT and MOSFET GaN devices and many of the same current collapse mechanisms occurring in these devices that lead to degradation in on-state resistance must be considered in GaN:C PCSS, such as surface trapping (especially in experimental studies requiring passivation to prevent flashover) and buffer trapping.

Figure 5.1.1. Chart of parameters affecting on-state resistance in PCSS, which will be iterated upon as the literature study progresses.

(B) Modeling of GaN:C PCSS using COMSOL has been initiated by building a simple model based off a GaAs PCSS application model available from COMSOL. This model was modified to represent the material and geometry of the GaN:C PCSS devices that are being studied. Errors mentioned in the November report have been fixed and a simple, working model achieved (Figure 5.1.2). This model will be further altered to accurately represent GaN PCSS devices allowing for parametric studies towards optimizing GaN:C PCSS parameters to minimize on-state resistance.

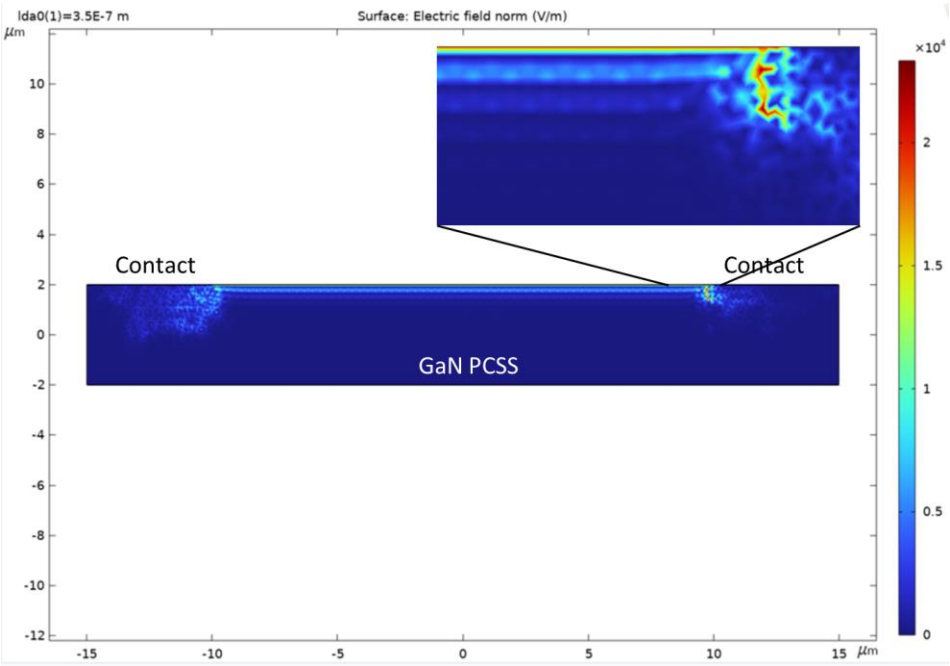

Figure 5.1.2: Simple COMSOL model of GaN PCSS device.

(C) A manuscript describing the parameters which affect on-state resistance in GaN:C PCSS, and how to minimize this, has been started and will serve to determine the direction of experimental and simulation analysis done as this paper progresses.

5.1.5 *Summary of Significant Findings and Mission Impact*

(A) A preliminary literature study of the on-state resistance of opto-electric devices began to find the parameters that affect the on-state resistance of GaN PCSS and similar devices of differing materials which will lead to the determination of what parameters can be manipulated to optimize on-state resistance in GaN PCSS, leading to a material option that provides increased efficiency and SWAP-C[2] capabilities of a PCSS-based RF generation system.

During literature review, it was found that publications in this area typically focus on vertical GaN-based PCSS devices and this has led to the conclusion that assumptions used in evaluating vertical devices need to be studied to determine their validity in lateral devices.

Due to the minimal jitter operation and increased device lifespan, focus will be restricted to linear mode PCSS operation, which limits devices to lateral geometries. Focus will also be placed on intrinsic carrier activation due to increased optical efficiency over extrinsic activation.

(B) Work continued towards building a working GaN:C PCSS model using COMSOL multi-physics which would allow for parametric sweep studies to be performed efficiently.

A simple, working model has been generated in COMSOL and errors mentioned in the November report fixed.

(C) Work towards a manuscript based on optimizing on-state resistance in GaN:C PCSS has been started with the first version of the introduction written and currently being edited.

5.1.6 References

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6 Drift-Step-Recovery-Diode-Based Source Alternatives

6.1 Drift-Step Recovery Diode and Pulse Shaping Device Optimization

(Jay Eifler)

6.1.1 *Problem Statement, Approach, and Context*

Primary Problem: Drift-step recovery diodes (DSRDs) and DSRD-based pulsed power systems are competitive with PCSS-based systems for HPM cUAS, with the benefit of not requiring a laser. Maximizing peak power while maintaining characteristic ns-order DSRD rise times requires optimization of the DSRD device design and pulser. Other considerations are for compactness, low-jitter, cooling required, and additional pulse-sharpening device within the pulse shaping head circuit. Additional goals for pulse repetition frequency are also to be satisfied for various applications.

Solution Space: By altering DSRD device parameters (geometry, doping, irradiation), optimize single-die and stack designs for peak power and risetime within various inductive pulser circuit topologies. Also optimize the pulse sharpening device (PSD) within the pulse shaping head circuit.

Sub-Problem 1: TCAD and SPICE models of the DSRD are inaccurate and must be improved. PSD models have not been developed.

Sub-Problem 2: Inductive pulser designs are complicated by the DSRD (and PSD) parameter variability. Use TCAD and/or SPICE models to account for variability and improve pulser design.

State-of-the-Art (SOTA): MW peak power and ns-order risetimes have been achieved in DSRD-based pulsed-power systems employing DSRD stacks for higher voltage holding and parallel lines of DSRD to increase current. PSD have sharpened DSRD pulses to 100 ps-order.

Deficiency in the SOTA: A lack of accurate TCAD and SPICE models make design of DSRD and DSRD-based inductive pulser circuit topologies (with or without PSDs) difficult to the level of tens of MW of peak power while maintaining ns-order risetime (or sharpened 100 ps-order). In addition, DSRD (and PSD) fabrication variabilities further complicate pulser design.

Solution Proposed: Develop further modeling capabilities in TCAD and SPICE for DSRD and DSRD-based inductive pulser circuit topologies to optimize DSRD and inductive pulser designs, especially for maximum peak power and minimum risetime, but also for low-jitter, reduced cooling, and compactness. Additionally, optimize pulser with PSD and pulse shaping head circuit.

Relevance to OSPRES Grant Objective: DSRD-based systems eliminate laser requirements necessary for PCSSs and are competitive in terms of thermal requirements and peak power. With sharpening, the DSRD-based systems can produce comparable risetimes. The SWaPC^2 cooling requirements of HPM cUAS systems can be solved with DSRD-based pulsed power systems, and low-jitter DSRD-based systems can be used for beam-steering in phased-arrays.

Risks, Payoffs, and Challenges: DSRD must be arrayed and staged to increase current since DSRD are limited in their ability to operate at high current densities. DSRD and PSD must also be stacked to operate at high voltages necessary for high peak power and maintain low risetimes. The stacking methods can damage dies and produce variable results in risetime and DSRD diffused doping profiles can be difficult to achieve and may require epitaxial methods. SPICE device models for DSRD are unavailable and must be developed, and questions remain about TCAD limitations for DSRD and PSD modeling.

6.1.2 Tasks and Milestones / Timeline / Status

(A) Milestone – Develop TCAD and SPICE models of the DSRD and MOSFET, respectively, that match experimental values of both the diode and circuit within 5% accuracy [*Estimated completion by AUG21*].

1. Task – Develop baseline DSRD model in TCAD [*completed JAN–APR21*];
2. Task – Develop SPICE model of DSRD within LTSPICE, an automated model parameter fitting procedure, and LTSPICE parameters for DSRD inventory [*Estimated completion AUG-NOV 2021 (continued effort as new DSRD arrive)*];
3. Task – Develop SPICE model of MOSFET within Silvaco [*JUL–SEP21*];
4. Task – Compare results of models developed in TCAD to the simulation values achieved using LTSPICE and experimentally (see Section 4.5) [*JUL–SEP21*];
5. Task – Incorporate parasitic capacitance, inductance, and resistance models for both single die and DSRD diode stacks (multiple dies in series) as well as for the DSRD-based pulser circuits [*discontinued after MAR–JUN21*];

(B) Milestone – Optimal characteristics of epitaxially-grown DSRD pinpointed from parametric study which produce the maximum waveform fidelity characteristics (e.g., maximum peak voltage, shortest risetime, highest dV/dt) [*Estimated completion by AUG21*].

1. Task – Determine carrier lifetime effect on risetime [*completed FEB–APR21*];
2. Task – Determine effect of including avalanche modeling on DSRD performance [*completed FEB–MAY21*];
3. Task – Determine effect of the width of outer edge contact on current density and breakdown in device [*discontinued after MAR–MAY21*];
4. Task – Model TCAD process in Silvaco Athena and Victory Process for DSRD diffused and epitaxial processes (and pulse sharpening devices) used for DSRD fabrication and DSRD device modeling [*discontinued after MAR–JUN21*];
5. Task – Determine optimal doping profile for Semiconductor Power Technologies (SPT) DSRD epitaxial designs [*completed MAY–JUL21*];
6. Task – Determine best doping profile from fabricated and optimal conceptual designs by comparing performance in the 2x2 DSRD pulser [***completed JUL21***];
7. Task – Complete DSRD performance study on epitaxial doping profile (n-side) variation manufactured by SPT in conjunction with LSRL [***completed JUL21***];

8. Task – Complete gain study for DSRD stack height and gain staging design [***completed JUL21***];
9. Task – Verify accuracy of TCAD simulations by comparing to experiment for DSRD-based pulser circuit topologies [*JUL–AUG21*];
10. Task – Perform first semiconductor opening switch (SOS) TCAD simulations for DSRD vs SOS mode of operation [SEP21];

(C) Milestone – Pulse sharpening devices developed within TCAD which improve the risetime and peak voltage of the IES pulse generator developed in Section 4.5 [***transitioned to Section 4.7 JUL21***].

1. Task – Develop preliminary pulse sharpening devices (PSD) models within TCAD [*discontinued after DEC20*];
2. Task – Develop standard PSD models within TCAD to reproduce results from published work [*discontinued APR–JUN20*];
3. Task – PSD simulated with DSRD 3-stack for more complete DSRD-based system modeling excluding only the primary switch model [*APR–JUN20*];
4. Task – Determine current carrying capacity of PSD and DSRD stacks [*discontinued MAR–JUN21*];

6.1.3 *Progress Made Since Last Report*

(A.2) Reverse recovery test (RRT) curve fitting has been automated for both a transit time for each forward/reverse voltage pairing in the RRT and a constant transit time for all the voltages. A constant transit time can be used that accurately models the experimental RRT recovery time in simulation.

(A.4) New LTSPICE simulations for the 4x2 DSRD-based pulser showed an inconsistency in the results between computers used likely due to convergence or possibly another issue. Standard diode test LTSPICE simulations and results for the 1x1 pulser have been shown to be consistent. Convergence issues can cause both the result to vary between computers and contribute to inaccurate pulser simulations. The 2x2 pulser produced in simulation a similar result with small differences in calculated numbers, and the 4x2 pulser in simulation produced a different result entirely. The 2x2 and 4x2 pulsers simulations are still being tested for consistency and accuracy.

6.1.4 *Technical Results*

(A.2) An automated procedure for extracting the transit time (TT) was also used to fit recovery time of reverse recovery test (RRT) curves between experiment and LTSPICE simulation. RRTs use a constant 20 V forward voltage and a reverse voltage varied from 20 V to 200 V in 20 V increments (anti-symmetric). As well, some RRTs use different forward voltages but have the same (symmetric) forward and reverse voltage (as for the legacy diode RRTs). A unique TT for each RRT can be fit but a single, constant TT can also be used to fit all of the recovery times and still fit well. In Figure 6.1.1. are shown recovery times using both unique TT and a constant TT for the generation 2, round 1, diode 1-1.

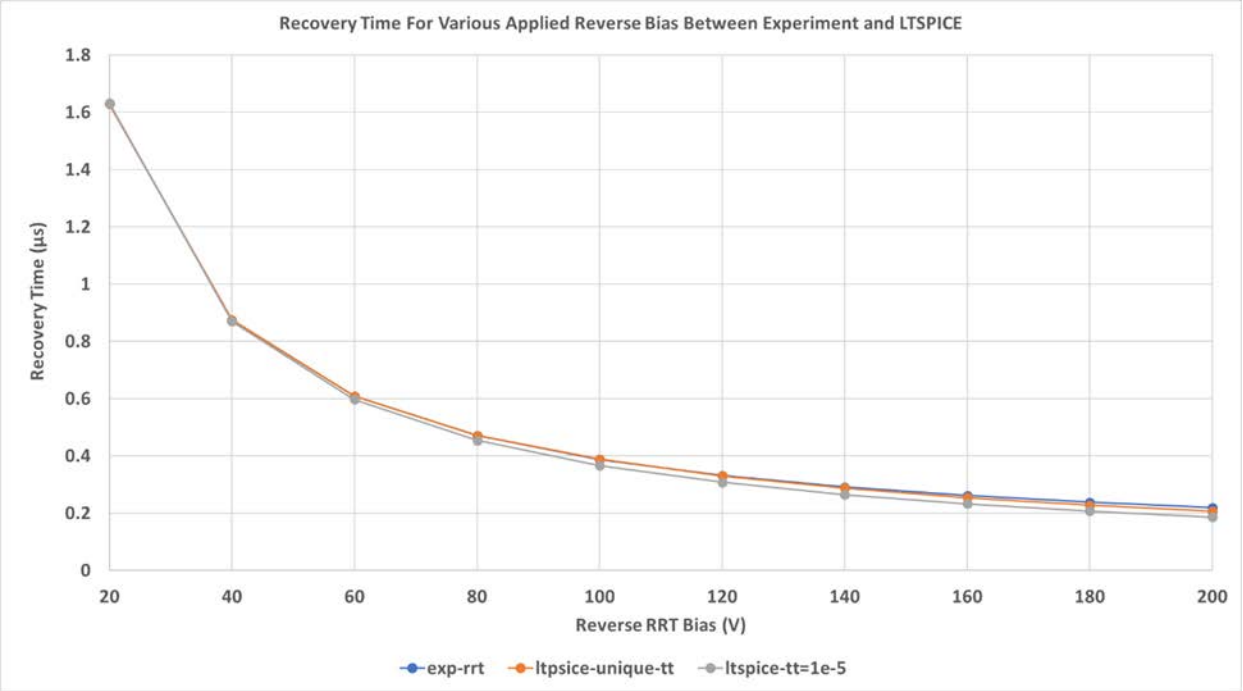

Figure 6.1.1. Recovery times vs reverse bias used and for 20 V forward voltage used. The experiment, unique and constant (1×10^{-5} s) transit times used all produce similar recovery times.

The result shows that a constant TT prodcues nearly the same recovery times than with a unique TT when compared to experiment. The result implies a constant TT can be used to accurately simulate RRTs. The application of TT however is for modeling in the DSRD-based pulser that has a different set of forward and reverse vltages applied for much shorter times than in the RRT and these RRT-dervied TT have not reproduced experimental pulser peak load voltages or especially risetimes. The TT vs total time difference error is shown in Figure 6.1.2. The legacy 7-stack results use a different set of RRT (symmetric as opposed to anti-symmetric) and would have different error and TT from such a fitting. Disregarding the higher error result for Gen2.1, the EG1500 and Gen2.1 results have similar TT with EG1500 having more of a spread. The Gen2.1 result is higher in error and error spread in the fitting.

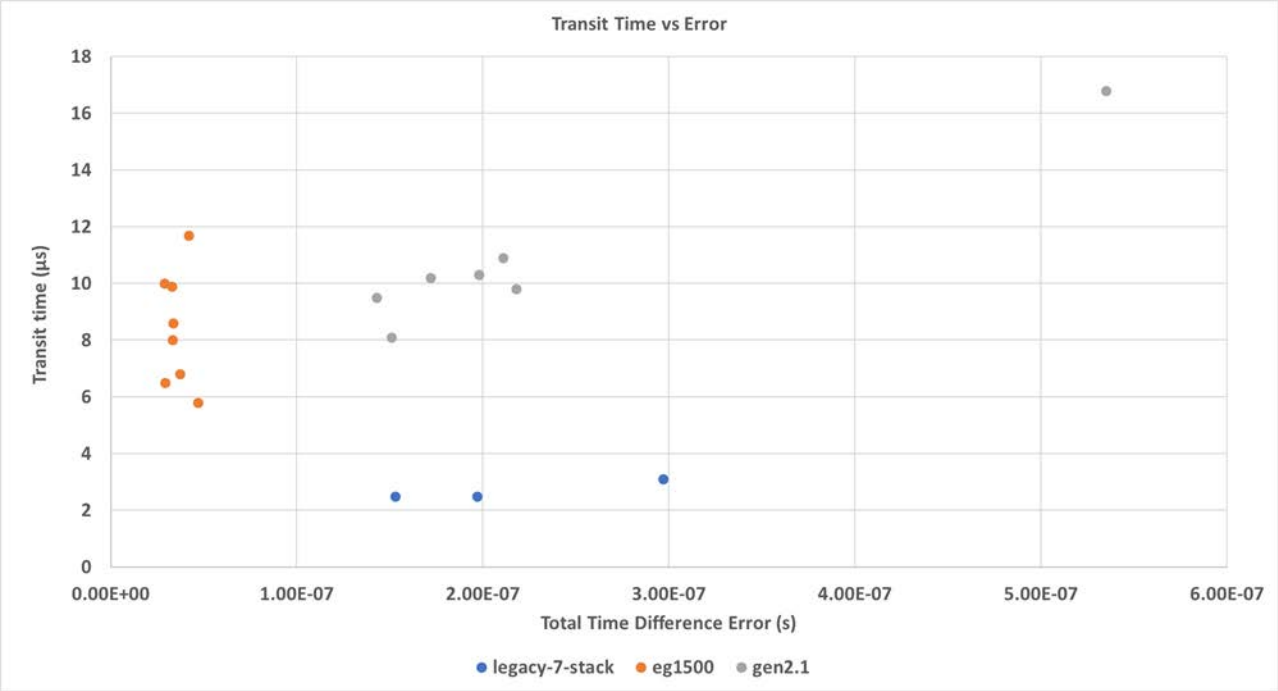

Figure 6.1.2. Transit time vs error for legacy, Gen2.1 and EG1500 DSRD. The legacy results use a different set of RRT and are not comparable in error or TT fitting.

6.1.5 *Summary of Significant Findings and Mission Impact*

DSRD TCAD simulation started by replicating published TCAD DSRD results and then simulating devices similar with actual in-house DSRD. The variation of the sinewave pulse voltage input magnitude and period on DSRD charge storage were collected. Charge storage timing (when the diode empties charge stored from forward pulsing) of ~50% was achievable with sufficiently long voltage input period which is necessary for maximum reverse current cutoff.

DSRD stacks, as opposed to individual die DSRD, were simulated showing reduced risetime from single die to 5-stacked DSRDs consistent with published and earlier in-house data. Series resistance to model metal resistance between DSRD in stacks and doping variability in stacks was also modeled in TCAD showing metal resistance must be large to have an impact on peak voltage and risetime and that doping variations proportionally effect risetime.

(A.1) Accurate DSRD TCAD models have been developed that include both carrier-carrier scattering and Selberherr breakdown and are suitable for DSRD operation below the dynamic breakdown threshold. Peak voltage and risetime were limited by the breakdown model and more closely match experimental pulse data.

(A.2) A new DSRD LTSPICE model has been developed following the method used for developing a TCAD SPICE MOSFET model and by matching too experimental standard diode tests. The forward I-V and reverse C-V have been well matched using a 7-diode model for a 7-stack DSRD, as opposed to using only a 1-diode

model for all DSRD stack heights. The reverse I-V and forward C-V are generally more problematic to fit to and proved to be so. More research and effort will be necessary to improve these matches and understand the impact on pulser simulation. The reverse recovery experiments have also been well matched (even for a single transit time over different reverse recovery testing voltages) and complete the matching of all the standard diode tests. New diodes are arriving and being tested and parameterized and tested in simulation and compared with experiment. Pulser performance has been difficult to assess due to the experimental data gathered thus far. The new DSRD LTSPICE model will also enable improvements in the TCAD SPICE MOSFET model. Overall, the new DSRD model represents a vast improvement over the previous model but has yet to include breakdown effects possible in the TCAD DSRD model and therefore breakdown limits of DSRD operation. A new automated fitting procedure now allows the model parameters to be more closely and quickly fit, has been used to fit various batches of different DSRD, and has used averaged curves (for improved measurement) when available.

(A.3) Work on TCAD SPICE MOSFET models has been done for the primary switch model (MOSFET) with conversion of the code to TCAD SPICE being partly completed to allow for modeling the complete DSRD-based pulser system (except driver). However, the conversion to TCAD of the MOSFET primary switch model, developed by CREE, to TCAD SPICE is complicated by having to develop custom behavioral models in TCAD SPICE which would be high-risk. Instead, a published model usable in TCAD SPICE was implemented and fit to the datasheet and then tested in a DSRD pulser simulation. The new MOSFET SPICE model usable in TCAD showed improvement in not having a first output pulse peak that was higher. This higher pulse had occurred in the TCAD MOSFET model (not SPICE model) and had not occurred in the voltage-controlled resistor MOSFET model (inaccurate model). Further refinement and testing of the new MOSFET SPICE model for use in TCAD has been more closely fit with the Cree LTSPICE model and compared to the Cree datasheet. The model can also be adapted to a new MOSFET in use within current DSRD pulsers. Further fitting can still be accomplished and matching both the Cree datasheet and LTSPICE model for gate charge and switching characteristics can be completed with more research into the test circuits used which are commonly not well explained in datasheets.

(A.4) LTSPICE, TCAD and experiment have been compared for the single bar pulser using a 7-stack DSRD, however there is some discrepancy for these experiments with earlier experiments (which the LTSPICE and TCAD simulations match better with) most likely due to the variability in DSRD and some to the new DSRD switch integration used for ease of switching out DSRD of various stack heights and combinations. As more experimental data is acquired for the pulsers the comparisons with simulation will yield more useful results. The 2x2 DSRD pulsers have been compared to TCAD simulation incorporating the latest TCAD SPICE MOSFET models showing some similarities in predicted peak voltage and risetime, but the most significant result is the matching of the experimental optimum trigger duration of 340 ns with TCAD results. LTSPICE simulations have been performed

with the new DSRD LTSPICE models and show the standard diode model used can match experimental peak voltages and risetimes but only by adjusting mainly the CJO parameter. Without adjustment there is considerable error in simulated results. Better diode models exist that incorporate impact ionization effects and recovery time modeling the latter of which circumvents CJO adjustment. With further experiments and simulation refinement it is expected that the models will be predictive of experiment within the quality of the experimental data and models used. Some inconsistency between computers for LTSPICE, having to do most likely with convergence in the pulser simulations, is being studied for the 2x2 and 4x2 DSRD-based pulsers.

(B.1) DSRD risetime performance was collected from TCAD simulations for variable carrier lifetime. Changes in lifetime had no significant effect on risetime other than the output pulse starting earlier.

(B.2) DSRD peak voltage and risetime were simulated in TCAD to include avalanche modeling or not. TCAD avalanche models limited peak voltage and risetime at the load over a range of voltage input magnitudes. A TCAD parameter study for DSRD stack height and DSRD area for several doping profiles with and without avalanche modeling was performed (Spring 2021 UMKC OSPRES Grant Review and Technical Exchange). The avalanche model and model parameters were also modified to account for dynamic breakdown rather than static and then compared to the no avalanche case and experimental data. From the improved avalanche modeling and TCAD parameter study, the optimal area of the DSRD can be obtained. However, for the 500 V voltage input magnitude used, the DSRD output were all in breakdown and are not predictive of non-breakdown behavior. Future studies for optimal area will include a range of voltage magnitudes to study DSRD performance and breakdown.

(B.4) TCAD process and device modeling for the development of process steps and their resultant doping profiles and device operation was begun. This modeling will enable a connection between the fabrication parameters and the device operation for DSRD (and PSD).

(B.5) Exponential doping profiles were shown (via TCAD) to outperform Gaussian and error function profiles slightly. Exponential profiles have an optimal minimum doping of 5×10^{13}–$1\text{x}10^{14}$ dopant atoms/cm^3, while Gaussian and error function profiles have an optimal minimum doping of 1×10^{13}-5×10^{13} dopant atoms/cm^3. Further exponential doping parameter studies were carried out in circuits A and B of Figure 4.2.1 (see JUN 2021 Grant Report) which included a broader doping parameter space for minimum doping, junction placement, basewidth and peak doping over a wider range of voltage input magnitudes (for breakdown limitations). The results are similar to before and show the optimally performing doping profile has a minimum doping of 5×10^{13}, no basewidth, junction placement of 95 μm, and peak doping of 1×10^{18} (p-side) and 1×10^{19} (n-side) dopant atoms/cm^3. A comparison was made for the optimal exponential doping profiles to optimal error function, LLNL and SPT DSRD designs within the 2x2 DSRD pulser system. The TCAD study showed the exponential doping profile performs the best overall when

considering peak voltage, risetime, voltage riserate, maximum reverse current, FWHM pulsewidth, prepulse and gain. Epitaxy designs with realistic deviations from the ideal exponential profile from the SRP data were shown in TCAD to not significantly affect the performance.

(B.7) A more complete gain study for varying prime voltage input and stack height was completed. The results show a variety of considerations must be made for determining the better stack heights to use in DSRD pulsers. The design of the pulsers can be improved when considering the gain staging in multi-staged DSRD pulsers as caused by the DSRD stack heights used. The 7- and 13-stacks showed the best gain. However, the peak voltages were best for the 13-stack while the 26-stack required unrealistic MOSFET currents to achieve its maximal peak voltage (or gain). For gain per die within a DSRD stack, 1-stacks showed the best gain per single and showed that gain 'efficiency' drops with stack height. Still, higher 7- and 13-stacks had the highest gain. How best to use this new data for DSRD pulsers is under discussion.

(B.10) First semiconductor opening switch (SOS) TCAD simulations have been performed for demonstrating a hgiher current density mode of operation. Future SOS TCAD simulations can help delineate the difference in DSRD and SOS for current density snappy recovery according to doping profile and mode of device operation.

(C.1) Pulse sharpening has been verified for PSD devices for the standard design and another non-conventional design. The PSD was also modeled within a DSRD-based pulser circuit combining for the first time TCAD modeling of both DSRD and PSD together within the same circuit with only the primary switch model not included.

(E) DSRD pulser circuits for the single-bar (Circuit B of Figure 4.2.1) and 2x2 (circuit C of Figure 4.2.1) have been simulated within TCAD allowing the use of a TCAD DSRD model, whereas in SPICE no accurate DSRD SPICE model is available. Currently, the primary switch MOSFET is modeled in TCAD, as well, but SPICE models can also be developed for the SPICE within TCAD as and will allow for better use of computational resources within TCAD. The MOSFET model and pulse repetition are being studied in detail to more closely match experiment and TCAD.

6.2 Pioneering Drift-Step Recovery Diode Processing and Manufacturing

(Alex Usenko)

6.2.1 *Problem Statement, Approach, and Context*

Primary Problem: DSRDs have not increased in performance since the 1960's due to reliance on deep diffusion manufacturing Their voltage-to-risetime, dV/dt, remains about 10^{12} V/s. To achieve the 10^{13} V/s (10 kV/ns) voltage-to-risetime required by an all-solid-

state HPM pulse generator in support of the Naval afloat mission, improving DSRD manufacturing techniques is critical.

Solution Space: Leverage applicable concepts from the mainstream silicon chipmaking industry and apply new manufacturing methods to DSRD processing.

Sub-Problem 1 – Diode silicon surface termination/passivation: The SOTA uses diode termination by a vertical wall. This design results in low breakdown voltage as it is limited by surface breakdown. To increase the diode breakdown voltage to closer to that of the bulk silicon breakdown voltage value, the vertical side wall design must be avoided.

Sub-Problem 2 – Stacking of DSRD dies: The SOTA is based on soldering of diode dies into a stack, which limits the stack lifetime to below 10^{12} pulses. Also, the SOTA did not apply the methodology of stacking wafers first, then cutting into dies. Switching to wafer level stacking will decrease the number of stacking operations by more than 100x.

Sub-Problem 3 – Packaging of stacked dies: *The* SOTA uses bare stacked DSRDs. Mounting the bare stack into a press-pack type package will improve long-term stability, such that the stack will survive a much higher number of pulses before it burns out.

State-of-the-Art (SOTA): In a recently published paper (2019),[1] the Russian St. Petersburg team at the Ioffe institute reported achieving a peak current density of 5 kA/cm^2 with a rise time of the output pulse front of ~2.3 ns, and a peak voltage across the load of 900 V (i.e., the peak switching power is 4.5×10^6 W/cm^2). The St. Petersburg team utilized deep diffusion technology. A competing team at Ekaterinburg, Russia [2] reports similar pulse performance. Both teams use outdated deep diffusion technology. As one can see, there has not been any significant improvement in DSRD pulse performance since the pioneering work done in 1960 [3].

Deficiency in the SOTA: First, no DSRDs have been manufactured using epitaxy technology with doping profile optimization. Second, no DSRD processing method exists that integrates side passivation with silicon dioxide. Finally, an acceptable DSRD stacking process has yet to be developed.

Solution Proposed: Manufacture DSRDs within the continental United States using an epitaxial growth process leveraging the optimal characteristics (e.g., doping profile, carrier concentration) determined through the work performed in Section 6.1 and through working with industry partners at Semiconductor Power Technologies (SPT), Livermore Semiconductor Research Laboratories (LSRL) and Lawrence Livermore National Laboratory (LLNL – Voss Group).

Relevance to OSPRES Grant Objective: DSRD manufacturing technology is a major building block of short-pulse high-peak-power defense systems. Our new disruptive process flow for DSRDs enables not only manufacturing of DSRDs at scale, but within the continental United States (CONUS). In doing so we will redefine the SOTA by producing optimal DSRDs. Further, DSRDs will be used within best-in-class HPM pulse generators which become part of more advanced defense systems within the Navy arsenal.

Risks, Payoffs, and Challenges:

Risks: As the process of producing DSRDs using epitaxial growth with doping profile design is novel, uncharted territory, there is inherent risk to its success. Additionally, post-processing methods based on the discussions provided in the ***Sub-Problems*** section are not well-established.

Payoffs: Replacing traditional deep diffusion technology with a new process integration scheme would allow better DSRD pulse performance. Electrical breakdown voltage, reliability, and lifetime are expected to increase, and rise time on a load is expected to decrease.

6.2.2 Tasks and Milestones / Timeline / Status

(A) Milestone – Produce epitaxial DSRDs that contain optimal exponential doping profiles and carrier concentrations /estimated MAR*22*.

1. Task – Design of experiment on 25 wafers through negotiations with vendors / *MAY–JUL21* / Completed
2. Task – Perform DSRD stack epitaxy on 13 wafers at SVM Inc., and 25 wafers at LSRL / *JUN–AUG21* / Completed.
3. Develop process integration scheme that uses epitaxy instead of deep diffusion / *JUL–OCT21 /* Completed.
4. Compare traditional DSRD technology and suggested integration scheme. List disadvantages of traditional processes and define potential advantages of new processes / MAY–NOV21 / Completed.
5. Run Gen2 and Gen3 lots. Gen2 is on wafers with epi from SVM, Inc., Gen3 is on wafers with epi from LSRL. Gen2 uses the same BEOL as Gen1. Run BEOL of Gen3 – using our new patented processing scheme – Si_3N_4 masking, TMAH etch, oxidation, selective electroless metal deposition, wafer bonding, sawing into diode stacks / OCT–MAR22.
6. Submit Gen2 and Gen3 diode lots to UMKC team for pulsed performance measurements; collaborate with team on determining optimal doping profile through DoE (design of experiments) analysis by Minitab software / OCT21–MAR22.

(B) Milestone – Develop diode separation technique while keeping wafer integrity / Estimated completion FEB22.

1. Design lithography masks for short loop experiment, submit order to vendor. / MAR–APR21 / Completed.
2. Design short loop experiment for V-groove etching for diode separation. / MAR–APR21 / Completed.
3. Run short loop experiment for the diode separation by anisotropic etch; analyze results / MAY–OCT21 / Completed.

4. Based on results of previous short loop run, adjust equipment, and process recipes to achieve sufficient etch uniformity across the wafer. Run on updated equipment and recipe to prove etch uniformity. / Estimated JAN22.
5. Design lithography masks for epi DSRD run; submit order to vendor. / OCT21 / Completed.
6. Run Gen3 lot through V-groove etch step, transfer lot to next process step. / Estimated JAN22.

(C) Develop Ohmic contact deposition technique integrable with epitaxy, diode side termination/passivation, and wafer bonding steps / estimated AUG–JAN22.

1. Design short loop experiment to determine technical feasibility of selective electroless deposition of metal stack as a method of Ohmic contact forming in the DSRD process integration scheme. / OCT21 / Completed.
2. Determine vendor from which to order electroless deposition kits; obtain quotes, order, receive the kits. / OCT21 / Completed.
3. Run short loop experiment – nickel-copper-tin stack electroless deposition on a blanket wafer. Analyze results. / DEC21 / Completed.
4. Develop process recipe for the metal stack deposition to use in Gen3 DSRD lot manufacturing / estimated JAN22.
5. Run the selective metallization step on Gen3 lot; transfer the lot to next processing step. / Estimated FEB22.

(D) Develop wafer stack bonding technique integrable with the rest of Gen3 process flow / estimated SEP–FEB22.

1. Design short loop experiment for bonding 2 blanket wafers with Ni-Cu-Sn layers by solid–liquid interdiffusion. / SEP21 / Completed.
2. Run 2-wafers short loop experiment. Analyze results. / Estimated OCT–FEB22.
3. Test technical feasibility of multiple wafer bonding by bonding 10-wafer stack / estimated FEB22.
4. Upon proof of technical feasibility of 10-wafer stacking, develop process recipe to use for processing of Gen3 DSRD lot / estimated FEB22.
5. Run wafer bonding step on Gen3 lot, transfer the lot to next processing step. / Estimated MAR22.

(E) Develop wafer stack sawing technique into DSRD stacks, integrable with the rest of Gen3 process flow / estimated NOV–FEB22.

1. Design sawing process using Disco saw available at Semiconductor Power Technologies for cutting 10-wafer stack / estimated JAN22.
2. Run short loop cutting of blanket bonded 10-wafer stack. Analyze results. / Estimated FEB22.

3. Develop process recipe for Disco saw tool to use for Gen3 lot. / Estimated FEB22.
4. Run sawing step on Gen3 lot / estimated FEB22

(F) Develop diode side passivation process integrable with the rest of DSRD process flow.

1. Test compatibility of thermal oxidation for the diode side passivation with preceding anisotropic etch step / estimated FEB22.
2. Alternative diode side passivation process: design short loop experiment on room temperature oxidation by forming porous Si film and oxidizing the porous film / APR–OCT21 / Completed
3. Run part of Gen3 lot using the oxidized porous Si as diode side passivation / estimated FEB22.
4. Second alternative diode side passivation process: Design short loop experiment on room temperature oxide deposition from oversaturated fluorosilicic acid / estimated MAY–JAN22.
5. Run part of Gen3 lot using the oxidized porous Si as diode side passivation / estimated FEB22.
6. Choose the best from 3 methods of diode side surface passivation techniques / estimated FEB22.

(G) Develop a DSRD process based on out-diffusion (opposite to traditional in-diffusion process).

1. Process Gen4 lot based on process integration scheme described in our patent application filed in / estimated FEB22.

(H) Find vendor that manufactures press-pack parts, order the parts, and encapsulate the DSRD stacks into the press-packs / estimated FEB22.

6.2.3 *Progress Made Since Last Report*

(A5) For the Gen3 process flow, due to increasing delays with processing steps by outside vendors, decisions have been made to process 2 wafers only from the 24-wafer lot.

(A5) Several more wafers from the 13-wafer Gen2 lot were fully processed. Non-stacked DSRDs were manufactured.

(A6) The next lot of non-stacked Gen2 DSRDs was submitted to the UMKC pulse performance measuring team. The team will first characterize single diodes, then characterize a “loose stack”.

(C3) SEM analysis was performed on samples with electroless deposited palladium and nickel layers.

(F3) SEM analysis was performed on samples with porous passivating layer.

6.2.4 *Technical Results*

(C) Development of Ohmic contact deposition process step. Figure 6.2.1. shows the surface of a silicon wafer sample after palladium electroless plating. The sample is a <100> P-type heavy Boron doped 0.01–0.02 Ohm-cm silicon wafer. The wafer orientation and doping have been chosen to be like the top surface of the epitaxial layer in the Gen3 lot. The left image exhibits continuous net and island cells. The brighter areas (net) indicate thicker Pd. The cells are distorted rounds from gas bubbles sticking to the surface. They are all elongated in the same direction, as the wafer was placed vertically in a beaker with plating solution. The darker color inside of the cells indicates a thinner palladium layer. Altogether this means that hydrogen bubbles formed during the plating reaction interfere with the deposition process, and either bubble forming or bubble sticking to surface must be mitigated in the next run. The relevant adjustment to the process recipe has been designed.

Dark lines on the left image are scratches due to handling of the sample. This indicates low adhesion of the metal to silicon. The adhesion will be improved by post-plating anneal of the wafer at 400–600 °C. Nickel silicide is formed during this anneal thus improving adhesion.

The right image is higher magnification taken from the “net” location (thicker Pd). It shows near 100% Pd coverage. This is more than optimal ~50% coverage. Though we note that “cell” areas had near optimal Pd coverage. Adjustment will be made in the next run: to lower Pd coverage, the time in the Pd plating solution will be decreased. The image also shows that individual Pd drops are of spherical shape with an average size of ~0.3 microns, as expected.

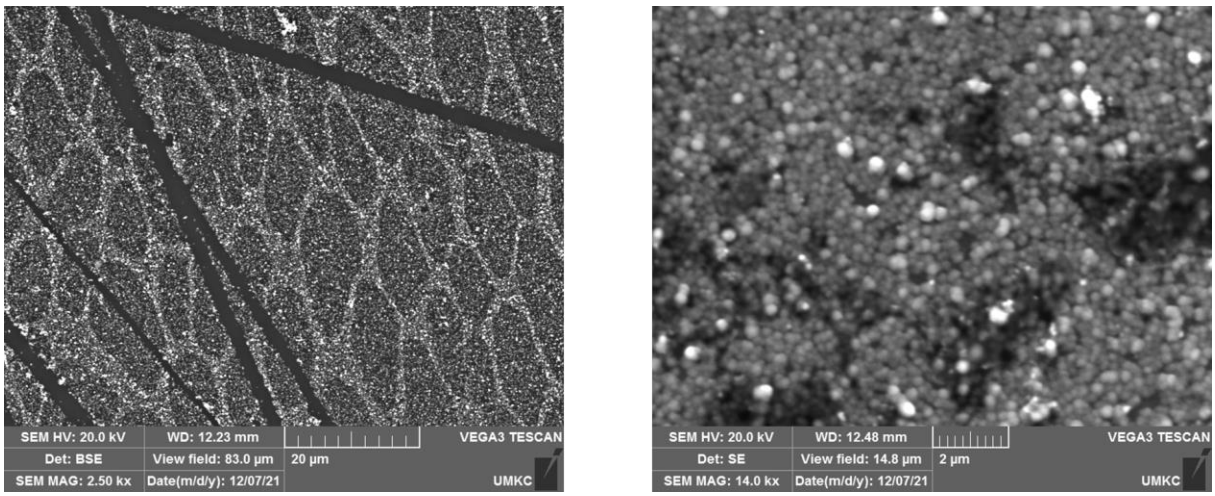

Figure 6.2.1. Palladium surface under SEM, various magnifications. Courtesy S.Dhungana.

(C) Figure 6.2.2. shows a nickel surface on the same sample. Palladium plating here is needed only to enable the subsequent nickel plating step. Pd has autocatalytic activity on Si surfaces, therefore making it possible for direct plating onto Si. Ni is not autocatalytic here, thus needs the additional Pd sublayer.

The left image in Fig.6.2.2 shows continuous coverage of the Si surface with nickel, as desired. This means that the featurability run is successful, and we can now switch to the next level: recipe development. Notice that the net-and-cell pattern disappeared; this means that Ni plating does not depend much on variations of the previous Pd plating step. Thus, we expect a robust high yield Ni plating process to be developed.

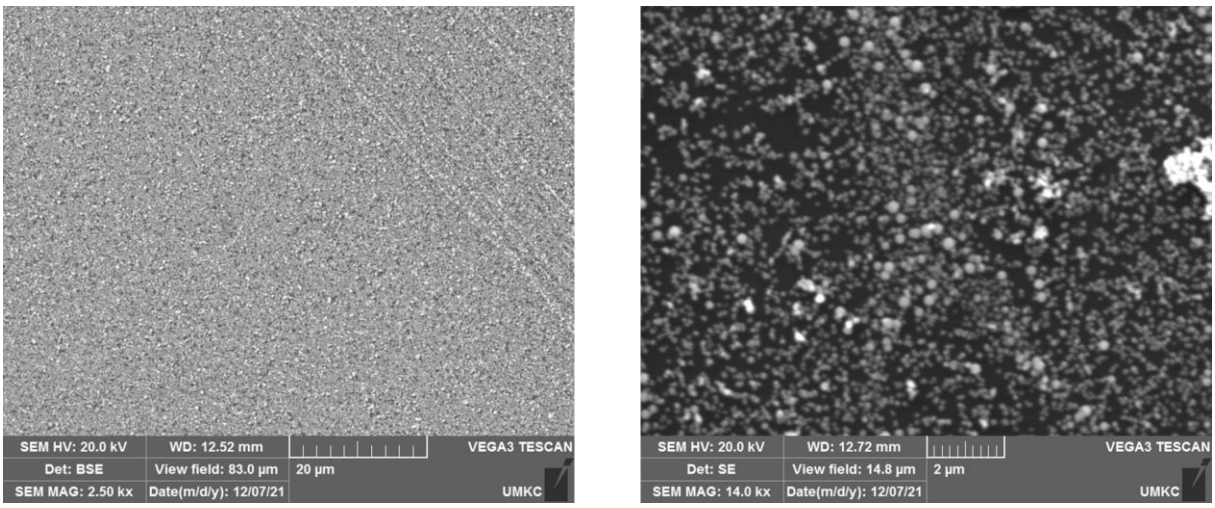

Figure 6.2.2. Nickel surface under SEM, various magnifications. Courtesy S.Dhungana.

(C) Figure 6.2.3 shows a cross section of a Pd/Ni layer on the same sample. The quality of the image is sufficient to see that the Pd/Ni layer is continuous, but not enough to measure its thickness.

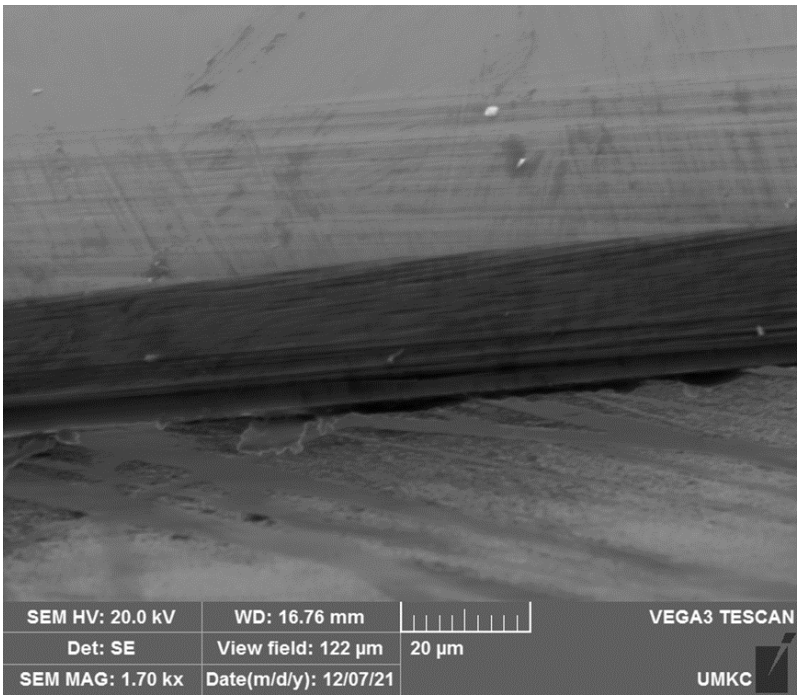

Figure 6.2.3. Cross section of Si wafer with Pd/Ni layer. Courtesy S.Dhungana.

(C) Figure 6.2.4 shows the surface of Pd on <100> high resistivity P-type 850–900 Ohm-cm Si. It was expected from the literature that plating on high resistivity Si is not possible, even for palladium. Though we see that Pd deposition still happens, the difference is that the layer is thinner.

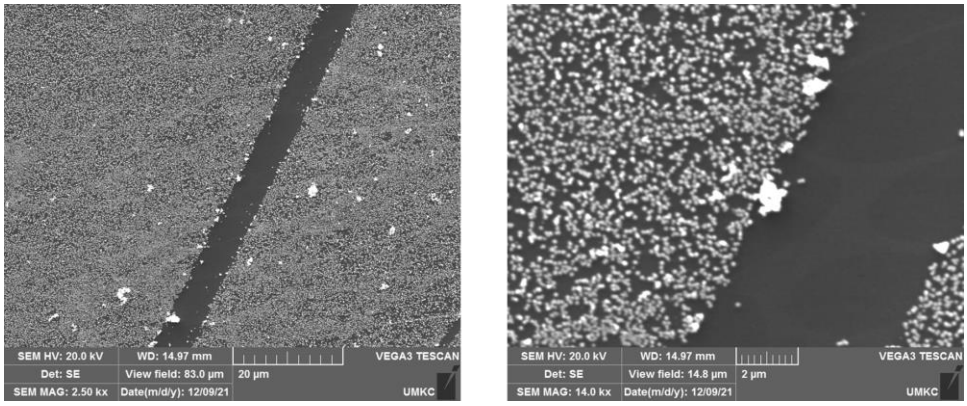

Figure 6.2.4. SEM image of palladium plated over high resistivity wafer. Courtesy S.Dhungana.

(C) Figure 6.2.5 shows the nickel surface on the same <100> high resistivity P-type 850–900 Ohm-cm Si. It shows a non-continuous Ni layer. Thus, we see, the requirement for highly doped Si for metallization is in force, as expected from the literature.

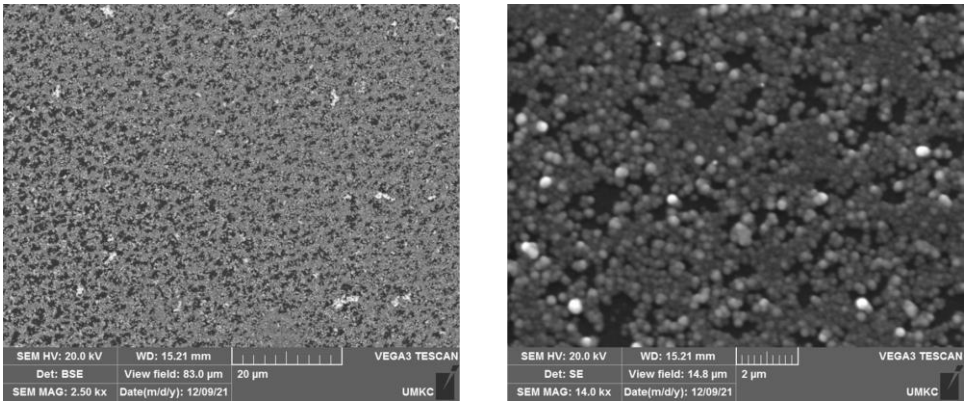

Figure 6.2.5. SEM image of Nickel plated over high resistivity wafer. Courtesy S.Dhungana.

(C) Figure 6.2.6 shows a cross section of plated metals over the same heavy doped sample. The nickel layer is about 1 micron thick, and the palladium sublayer is about 60 nm thick, as expected.

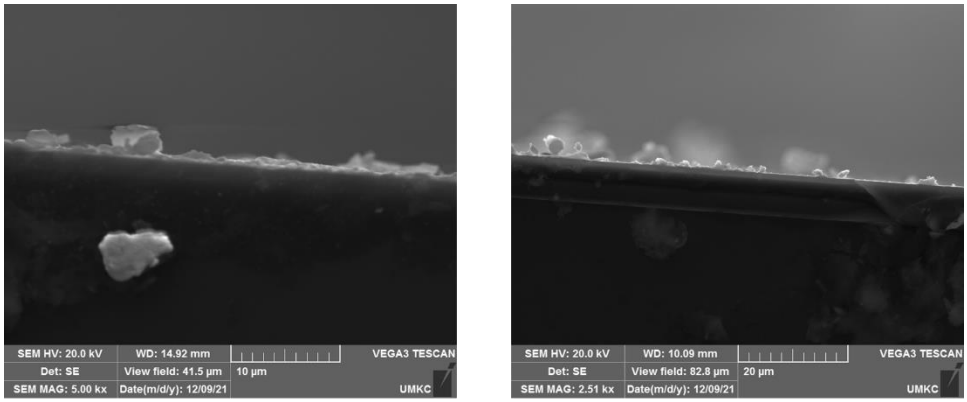

Figure 6.2.6. SEM cross section image of heavily doped wafer electrolessly plated with Pd and Ni. Courtesy S.Dhungana.

(F) Diode side surface passivation development. We consider 3 potential side surface passivation techniques: thermal oxidation, fluorinated oxide from oversaturated fluorosilicic acid, and stain etch. Figure 6.2.7 shows the surface of <111> 0.0015–0.003 Ohm-cm Si wafer after stain etch in a 1000:1 HF/HNO_3 mixture. On the left image, rounds are visible. These are from hydrogen bubbles. This image indicates that the stain etch process must be improved to exclude masking effects of bubbles stuck to surface. A new experiment had been planned.

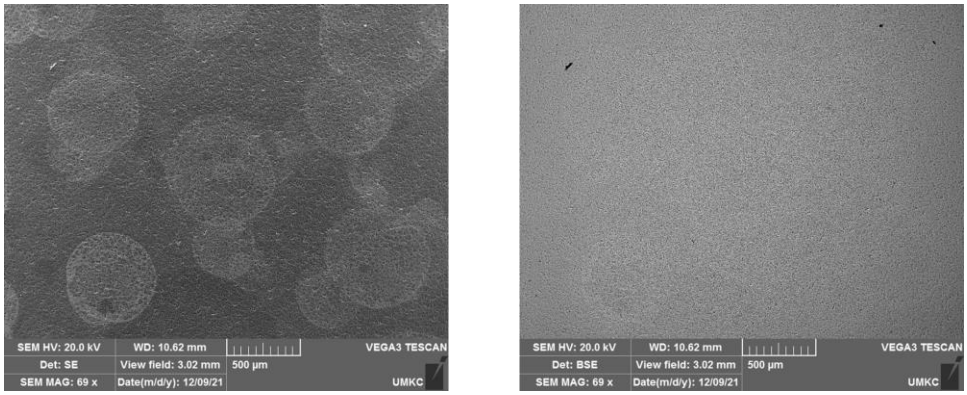

Figure 6.2.7. SEM image of heavily doped Si wafer after stain etch. Courtesy S.Dhungana.

(F) Figure 6.2.8 shows the surface of the same sample under higher magnification. Triangle shapes are visible with average size of 10 microns. The triangle geometry is as expected, as samples are <111>. Currently the samples are analyzed with SEM cross-section, to see morphology of the porous Si layer formed by the stain etch.

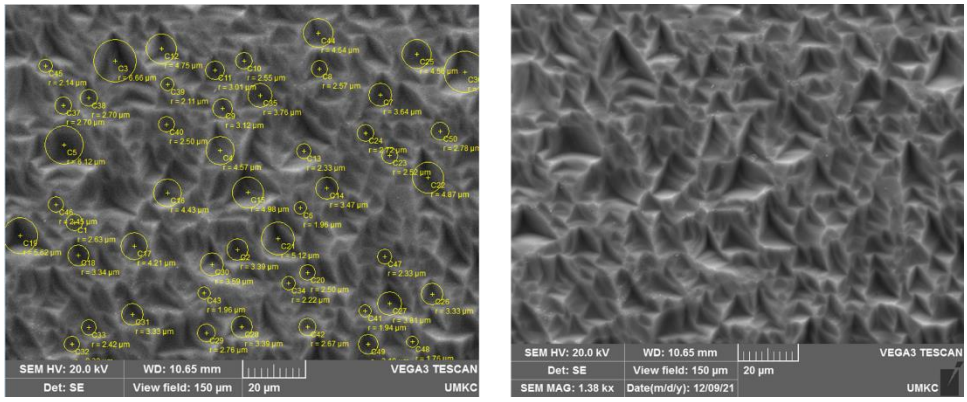

Figure 6.2.8. Higher magnification image of the same sample as previous figure. Courtesy S.Dhungana.

6.2.5 *Summary of Significant Findings and Mission Impact*

(A) Feedback from UMKC pulsed measurement team received - on Gen2 dies – see chapters 6.1 and 6.3 for details. The feedback has been thoroughly analyzed to improve the DSRD fabrication process. Several process adjustments have been implemented in processing of next Gen2 die lots. Die-to-die excessive variability is noticed. Process recipes and some equipment have been adjusted to achieve better uniformity and repeatability.

(B) Improving side termination of diodes. Upon analysis of etched v-grove shapes, decision made to purchase new labware including advanced wafer dippers. To prevent detrimental non-uniformity due to hydrogen bubbles sticking to wafer surface, several new process recipes have been developed. Next etch run will show whether sufficient uniformity achieved.

(C) Replacement of unreliable metal contact deposition technique (by electron beam sputtering in vacuum chamber). Technical feasibility run on direct electroless plating of the Palladium/Nickel stack was successful. Process recipe developed for next run, plate uniform stack of Pd/Ni/Cu/Sn .

(D) Diode side surface passivation by 2 new methods – stain etch, and SiOF deposition have been tried, and technical feasibility confirmed.

(C) The thickness and plating rate for the palladium and nickel in the electroless plating process have been determined from SEM cross section images of the samples.

(F) Improving side passivation of diodes. Upon analysis of SEM images of wafers after stain etch, process recipes for porous silicon growth in 1000:1 mixture of concentrated HF and HNO_3 have been adjusted. Optimal etch time were determined. Surface masking by hydrogen bubbles has been observed through analysis of the SEM images, and experimental plans to suppress the bubbling have been developed.

6.3 Characterization of SOS Diode Performance through DOE Augmentation

(Megan Hyde)

6.3.1 *Problem Statement, Approach, and Context*

Primary Problem: Drift step recovery diodes (DSRDs) are planar diodes that are capable of nanosecond, high-frequency (10–10^3 kHz) pulses [1] with applications as opening switches in inductive energy storage (IES) pulse generation circuits. There is not a clear understanding of the effects DSRD parameters have on overall IES pulser performance. The purpose of this project is to tie the DSRD parameters to its tailored performance requirements.

Solution Space: Leveraging both design of experiment (DOE) and machine learning (ML) capabilities, we will develop a methodology of characterizing DSRDs in order to provide fabrication recommendations in the context of application targets.

***Sub-Problem 1*:** We do not yet understand how the diode parameters are tied to the diode performances.

Sub-Problem 2: There is no standardized method for correlating the diode key performance indicators (KPIs) to the IES pulser generator performance.

Sub-Problem 3: The number of possible inputs for the DOE is expected to be too large, so ML will need to be leveraged in order to guide decision-making processes.

State-of-the-Art (SOTA): Standard diode measurements include curve tracers for forward and reverse IV, impedance spectroscopy for forward and reverse CV, and function generators or, for example, the Avtech pulser for reverse recovery with high voltage and/or high current when necessary. These measurements are used to generate commonly available datasheets for COTS diodes. These standard diode measurements can then be correlated to pulser performance using traditional data analytics.

Deficiency in the SOTA: The standard diode measurements and datasheets do not include pulser performance necessary to evaluate DSRDs. The datasets generated with doping profile assessment (for example spreading resistance profiling), standard diode measurements and pulser performance are too large and complex to leverage traditional data analytics and will benefit from machine learning techniques.

Solution Proposed: Develop a holistic evaluation network to characterize the KPIs of DSRDs. This network will include a DOE that will be a continuously evolving model as new KPIs are discovered between each of the stages within the network (Sections 6.1 to 6.5) referred to as the “augmented DOE”. Machine learning will be used as the primary decision-making tool for augmenting the DOE. Once the network is established, it will be used to outline the optimal parameters for stacks of DSRDs within an IES pulse generator.

Relevance to OSPRES Grant Objective: Bridging the gap between the theoretical and the physical performance of DSRDs enables closing the gap between a low fidelity TRL3 breadboard pulse generation system, and one which is at high fidelity TRL4 prototype level. At the TRL4 level, the DSRD-IES pulse generator system would be sufficient to replace the costly laser-based Si-PCSS HPM generator without compromise to scalability required to support the Naval afloat mission.

Risks, Payoffs, and Challenges:

Challenges: Traditional predictive analytics will be difficult to correlate with the augmented DOE due to the large volume of data. Machine learning is expected to assist with decision making processes for the DOE, but only if the proper KPIs have been established and good data has been used to train the machine learning model.

6.3.2 Tasks and Milestones / Timeline / Status

(A) Milestone – Establish preliminary DOE and SOP for identifying KPIs of DSRDs [*estimated completion by DEC21*].

1. Task – Ascertain current KPIs used to optimize diodes simulated, manufactured, and utilized within the IES pulse generating circuit (from Sections 6.2–6) [completed AUG21];
2. Task – Construct preliminary DOE to acquire data on all KPIs based on Task 1 to produce an optimal output for the IES pulse generating circuit (Section 6.5) [AUG21–MAR22];
3. Task – Leverage existing Python scripts to process legacy DSRD KPI data [*completed SEP21*];
4. Task – Develop new and review existing SOPs for experimental testing apparatuses used to evaluate individual KPIs and measure their performance [*completed OCT21*];
5. Task – Identify gaps/deficiencies in legacy KPI data, evaluate existing theoretical relationships to bridge gap and minimize DOE if possible [*SEP–OCT21*];
6. Task – Using SOPs developed in Task 4, acquire experimental data from legacy DSRDs, refine SOP(s) *pro re nata,* and assess repeatability and reproducibility [*SEP21–FEB22*];
7. Task – Begin training machine learning model with legacy data to determine statistical correlations and significance of KPIs, and their interdependent relationships [*OCT21–MAR22*];

(B) Milestone – Evaluate DSRD performance by the developed SOPs and facilitated by the preliminary DOE [*on hold until Milestone A is completed*].

1. Task – Augment DOE to include previously unidentified yet relevant KPIs based on new findings [*Est. Spring22*];
2. Task – Acquire data on newly manufactured epitaxial DSRDs from Section 6.3 using refined SOPs from Milestone A [*Est. Spring22*];
3. Task – Correlate KPIs to TCAD simulation model, manufactured diode characteristics, and 'M×N' IES pulser's performance to aid in simulation model development, fabrication procedures, and circuit topology development [*Est. Spring22*];

(C) Milestone – SOS diode network evaluation [*on hold until Milestone B is completed*].

1. Task – Refine Python script to incorporate new correlations based on findings from Milestones A&B [*Est. Fall22*];
2. Task – Amend ML training model with data acquired on new DSRDs (as characterized by Sections 6.2-3) to investigate statistical correlation of diode performance [*Est. Summer22*];
3. Task – Work with TCAD simulation team to address discrepancies between the DSRD's performance obtained experimentally, and that achieved within simulations [*Est. Summer22*];
4. Task – Collaborate with DSRD manufacturing team to address discrepancies between the DSRD's characteristics evaluated experimentally, and that desired by manufacturing process [*Est. Summer22*];
5. Task – Investigate relationships between statistical significance of individual diode KPIs to the peak performance of the IES pulser with the pulse generator team. [*Est. Summer22*];
6. Task – Incorporate findings from Tasks 1–5 into ML model, pinpoint KPI correlations of interest, and provide recommendations to IES sub-teams accordingly [*Est. Summer22*];

(D) Milestone – SOS diode network evaluation [*on hold until Milestone C is completed*].

1. Task – Augment DOE network to streamline diode evaluation and identify checkpoints/gaps within simulation, manufacturing, and circuit development process to ensure optimal diodes are selected and utilized to produced robust high-fidelity IES pulse generator prototypes [*Est. Fall22*];

6.3.3 *Progress Made Since Last Report*

(A.1) A new test tracking document has been implemented to track the tests performed on each diode to help visualize which tests have been completed, and which tests need to be repeated.

DD3 Diodes																				
7 Stack					13 Stack					26 Stack				
D1	Forward IV	Reverse IV	CV	RRT	D344	Forward IV	Reverse IV	CV	RRT	D409	Forward IV	Reverse IV	CV	RRT
D319	Forward IV	Reverse IV	CV	RRT	D345	Forward IV	Reverse IV	CV	RRT	D411	Forward IV	Reverse IV	CV	RRT
D333	Forward IV	Reverse IV	CV	RRT	D346	Forward IV	Reverse IV	CV	RRT	D413	Forward IV	Reverse IV	CV	RRT
D362	Forward IV	Reverse IV	CV	RRT	D393	Forward IV	Reverse IV	CV	RRT	D416	Forward IV	Reverse IV	CV	RRT
D363	Forward IV	Reverse IV	CV	RRT	D395	Forward IV	Reverse IV	CV	RRT	D430	Forward IV	Reverse IV	CV	RRT
D364	Forward IV	Reverse IV	CV	RRT	D402	Forward IV	Reverse IV	CV	RRT					
D365	Forward IV	Reverse IV	CV	RRT										
D366	Forward IV	Reverse IV	CV	RRT										
D367	Forward IV	Reverse IV	CV	RRT	Epitaxially Grown Diodes									
D368	Forward IV	Reverse IV	CV	RRT	EG1500					EG1600				
D369	Forward IV	Reverse IV	CV	RRT	D1562	Forward IV	Reverse IV	CV	RRT	D1601	Forward IV	Reverse IV	CV	RRT
D380	Forward IV	Reverse IV	CV	RRT	D1563	Forward IV	Reverse IV	CV	RRT	D1602	Forward IV	Reverse IV	CV	RRT
D381	Forward IV	Reverse IV	CV	RRT	D1564	Forward IV	Reverse IV	CV	RRT	D1603	Forward IV	Reverse IV	CV	RRT
D387	Forward IV	Reverse IV	CV	RRT	D1565	Forward IV	Reverse IV	CV	RRT	D1604	Forward IV	Reverse IV	CV	RRT
D392	Forward IV	Reverse IV	CV	RRT	D1566	Forward IV	Reverse IV	CV	RRT	D1605	Forward IV	Reverse IV	CV	RRT
D504	Forward IV	Reverse IV	CV	RRT	D1567	Forward IV	Reverse IV	CV	RRT	D1606	Forward IV	Reverse IV	CV	RRT
D505	Forward IV	Reverse IV	CV	RRT	D1568	Forward IV	Reverse IV	CV	RRT	D1607	Forward IV	Reverse IV	CV	RRT
D506	Forward IV	Reverse IV	CV	RRT	D1569	Forward IV	Reverse IV	CV	RRT	D1608	Forward IV	Reverse IV	CV	RRT
D507	Forward IV	Reverse IV	CV	RRT	D1570	Forward IV	Reverse IV	CV	RRT	D1609	Forward IV	Reverse IV	CV	RRT
D508	Forward IV	Reverse IV	CV	RRT	D1571	Forward IV	Reverse IV	CV	RRT	D1610	Forward IV	Reverse IV	CV	RRT
D509	Forward IV	Reverse IV	CV	RRT	D1572	Forward IV	Reverse IV	CV	RRT	D1611	Forward IV	Reverse IV	CV	RRT
D512	Forward IV	Reverse IV	CV	RRT	D1573	Forward IV	Reverse IV	CV	RRT	D1612	Forward IV	Reverse IV	CV	RRT
D513	Forward IV	Reverse IV	CV	RRT	D1574	Forward IV	Reverse IV	CV	RRT	D1613	Forward IV	Reverse IV	CV	RRT
600	Forward IV	Reverse IV	CV	RRT						D1614	Forward IV	Reverse IV	CV	RRT
601	Forward IV	Reverse IV	CV	RRT										
602	Forward IV	Reverse IV	CV	RRT	Gen 2									
603	Forward IV	Reverse IV	CV	RRT	Gen 2					Gen 2.2				
604	Forward IV	Reverse IV	CV	RRT	1-1	Forward IV	Reverse IV	CV	RRT	1	Forward IV	Reverse IV	CV	RRT
605	Forward IV	Reverse IV	CV	RRT	1-2	Forward IV	Reverse IV	CV	RRT	2	Forward IV	Reverse IV	CV	RRT
606	Forward IV	Reverse IV	CV	RRT	1-3	Forward IV	Reverse IV	CV	RRT	3	Forward IV	Reverse IV	CV	RRT
607	Forward IV	Reverse IV	CV	RRT	1-4	Forward IV	Reverse IV	CV	RRT	4	Forward IV	Reverse IV	CV	RRT
608	Forward IV	Reverse IV	CV	RRT	2-1	Forward IV	Reverse IV	CV	RRT	5	Forward IV	Reverse IV	CV	RRT
609	Forward IV	Reverse IV	CV	RRT	2-2	Forward IV	Reverse IV	CV	RRT	6	Forward IV	Reverse IV	CV	RRT
610	Forward IV	Reverse IV	CV	RRT	2-3	Forward IV	Reverse IV	CV	RRT	7	Forward IV	Reverse IV	CV	RRT
800	Forward IV	Reverse IV	CV	RRT	2-4	Forward IV	Reverse IV	CV	RRT	8	Forward IV	Reverse IV	CV	RRT
801	Forward IV	Reverse IV	CV	RRT	3-1	Forward IV	Reverse IV	CV	RRT	9	Forward IV	Reverse IV	CV	RRT
802	Forward IV	Reverse IV	CV	RRT	3-2	Forward IV	Reverse IV	CV	RRT	10	Forward IV	Reverse IV	CV	RRT
					3-3	Forward IV	Reverse IV	CV	RRT	11	Forward IV	Reverse IV	CV	RRT
					3-4	Forward IV	Reverse IV	CV	RRT	12	Forward IV	Reverse IV	CV	RRT
					4-1	Forward IV	Reverse IV	CV	RRT	13	Forward IV	Reverse IV	CV	RRT
					4-2	Forward IV	Reverse IV	CV	RRT	14	Forward IV	Reverse IV	CV	RRT
					4-3	Forward IV	Reverse IV	CV	RRT					
					4-4	Forward IV	Reverse IV	CV	RRT					
					5-1	Forward IV	Reverse IV	CV	RRT					
					5-2	Forward IV	Reverse IV	CV	RRT					
					5-3	Forward IV	Reverse IV	CV	RRT					

Completed
Completed, possible re-test
Incomplete

Table 6.3.1. Shown is the summary of each test performed on each diode. Each test is color coded to assist in identifying missing or incomplete data. Note that "DD3" is a naming convention for deep diffusion DSRDs. The tests included in the table are the forward and reverse IV, CV, and the RRT.

(A.4) Development of a new SOP for reverse recovery time (RRT) measurements are currently under review. Several epitaxially grown 1500 (EG1500) and 19 Gen 2 series DSRDs have been tested under a variety of test conditions (refer to Figure 6.3.2). Resolving the ideal testing conditions for RRT tests will enable us to

calculate the minority carrier lifetime. The present challenge is verifying the calculated time is the carrier lifetime, rather than the transient lifetime.

Modification of the IV and CV measurement SOPs were required for testing the Gen 2 DSRDs since they are a single stack, where voltages over 1 V can damage the diode.

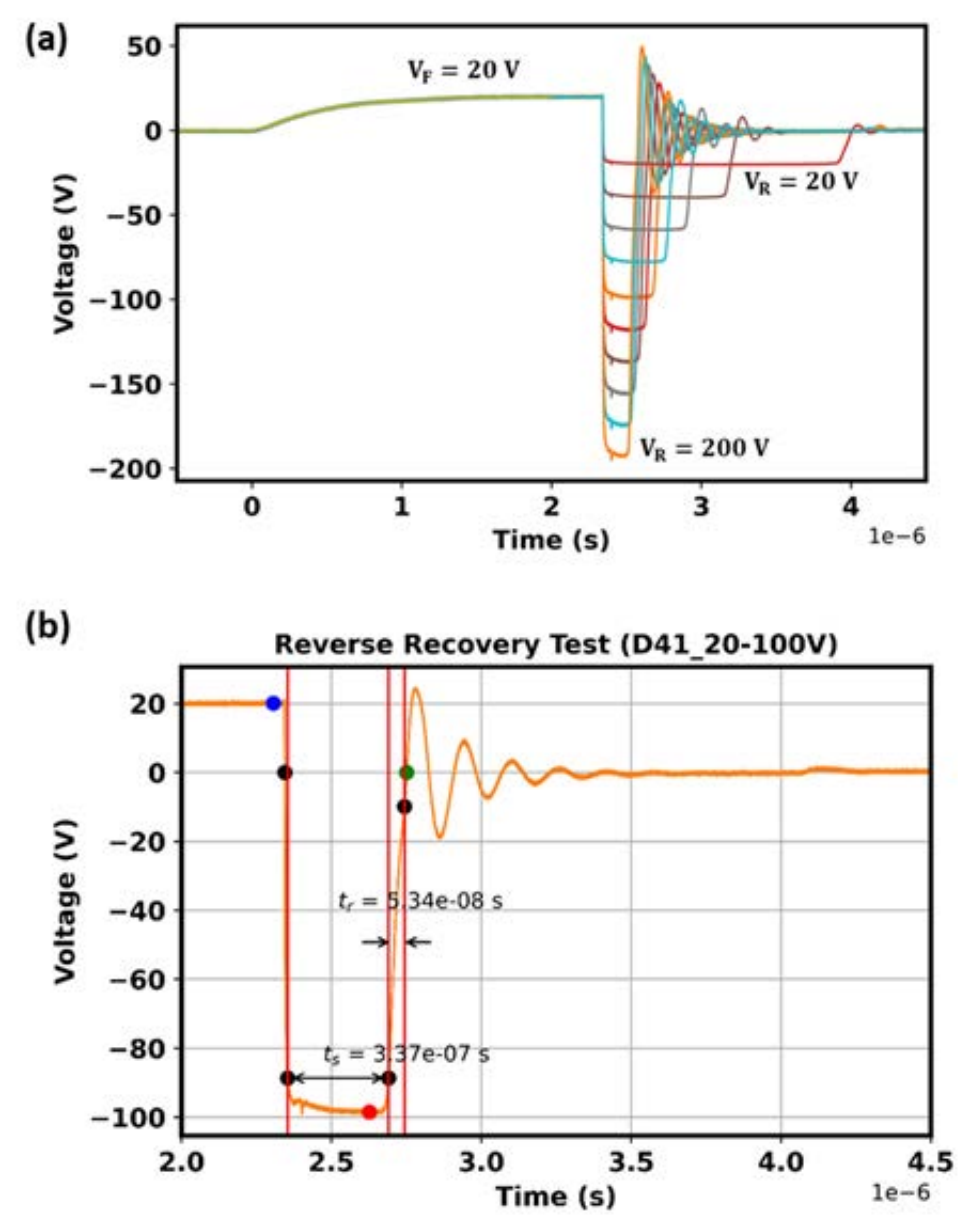

Figure 6.3.2. (a) A typical reverse recovery test data of a single-stack Gen 2 DSRD with forward voltage of 20 V and reverse voltage from 20 V to 200 V. Both forward and reverse voltage pulses were applied for 2 µs. (b) Reverse recovery test of Diode D4-1 showing the charge storage time t_s and transition time t_r.

(A.6) Of the DD3 (DD3 refers to a naming convention for deep diffusion diodes) DSRDs, 34 out of 48 have completed the IV (forward and reverse) and CV testing. RRT testing is still in the beginning stages as the ideal testing conditions for extracting minority carrier lifetimes has not yet been established. The remaining DSRDs to be tested are on hold until the RRT SOP has been finalized as well as the repeatability and reproducibility studies have been completed. Refer to Figure 6.3.3 for the comparisons between each type of DSRD and their completion status for each test.

All Gen2 DSRDs have completed their IV (forward and reverse) testing as well as the CV testing. The zero bias junction capacitance measurements from these diodes showed the greatest variability between each type, so the Gen2 diodes were selected to conduct the first round of repeatability and reproducibility studies. All Gen2 DSRDs have since been tested in the exact specifications according to the SOP an additional 3 times for IV and CV testing. Results of the study will be published the next section.

Every EG1500 DSRD has been tested in IV (forward and reverse), CV, and RRT. Alongside 19 of the Gen2 DSRDs, the EG1500s are a part of the method development for the RRT test. None of the EG1600 DSRDs have been tested yet. Refer to Table 6.3.1 for a summary of the testing status of each category of DSRD.

6.3.4 *Technical Results*

(A.6) The zero bias junction capacitance measurements were performed and qualitatively compared against each diode type (e.g., DD3, Gen2, EG1500). A qualitative comparison between each diode (refer to Figure 6.3.3) showed that the Gen 2 diodes had the greatest variability, so became the focus of a repeatability study.

Each Gen 2 diode was tested a total of three times for both CV and IV (forward and reverse) tests. Each test was performed by the same operator and under the same testing conditions as outline by their respective SOPs.

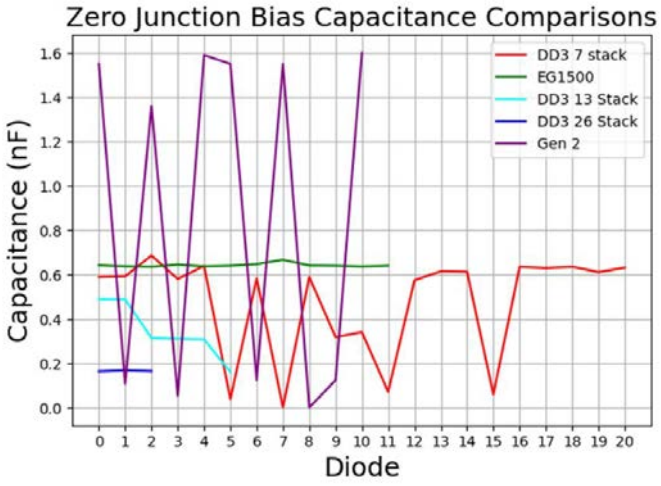

Figure 6.3.3. Zero junction bias capacitance plot that enables a qualitative comparison of the measurements against each type of diode. It was decided to begin a repeatability study on the Gen 2 diodes due to the variability of measurements found from this plot.

Figure 6.3.4 highlights the findings of the repeatability study found for the CV test. So far, there does not appear to be a correlation between the metallicity (color of diode) to overall performance. Other sources of variation are currently under investigation.

In addition to the CV test, a repeatability study was performed on the Gen 2 diodes for the IV test. Figure 6.3.5 shows the results of that study. The measurement plotted is the voltage of each diode at 10mA. As can be seen from the figure, two diodes did not provide any useable data (corresponds to the "Completed, possible re-test" label used in Table 6.3.1). Since the diodes never achieved breakdown voltages, the results of the reverse IV test showed little variation in the testing, so alternative testing conditions are under consideration.

A Levene's Variability test was performed on the results for both the forward IV and CV testing. The p-value validates the consistency of the testing performed ($p = 0.8548$ for CV and $p = 0.8416$ for IV).

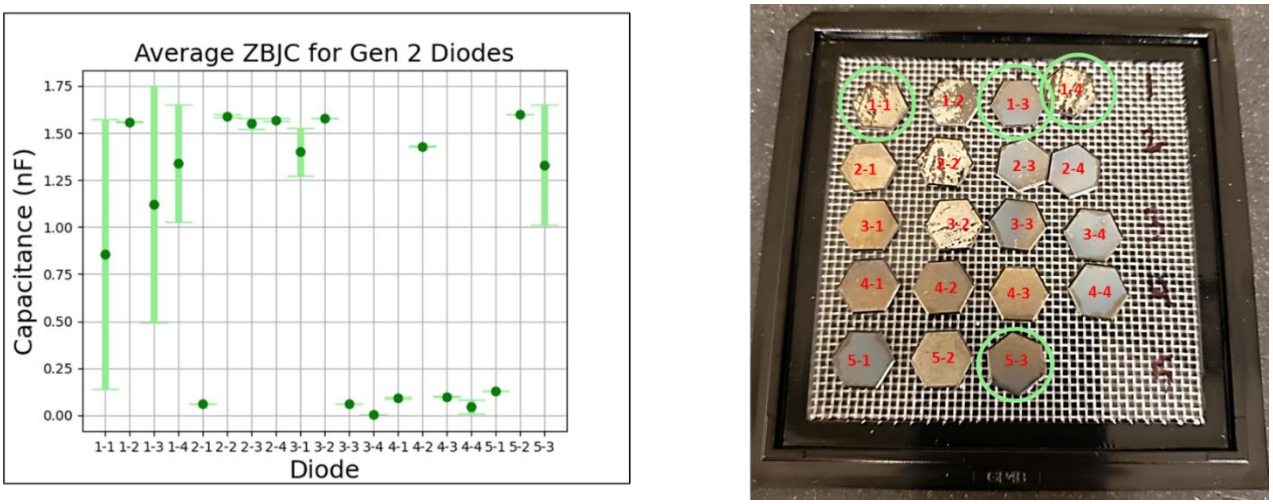

Figure 6.3.4. Results of the repeatability study for the zero junction bias capacitance measurements. On the left are the measurement averages with their respective standard deviations. On the right is an image of the Gen 2 diodes. Each diode has been labeled with its name in red, and each diode circled in green represents the diodes with the greatest variability from this study.

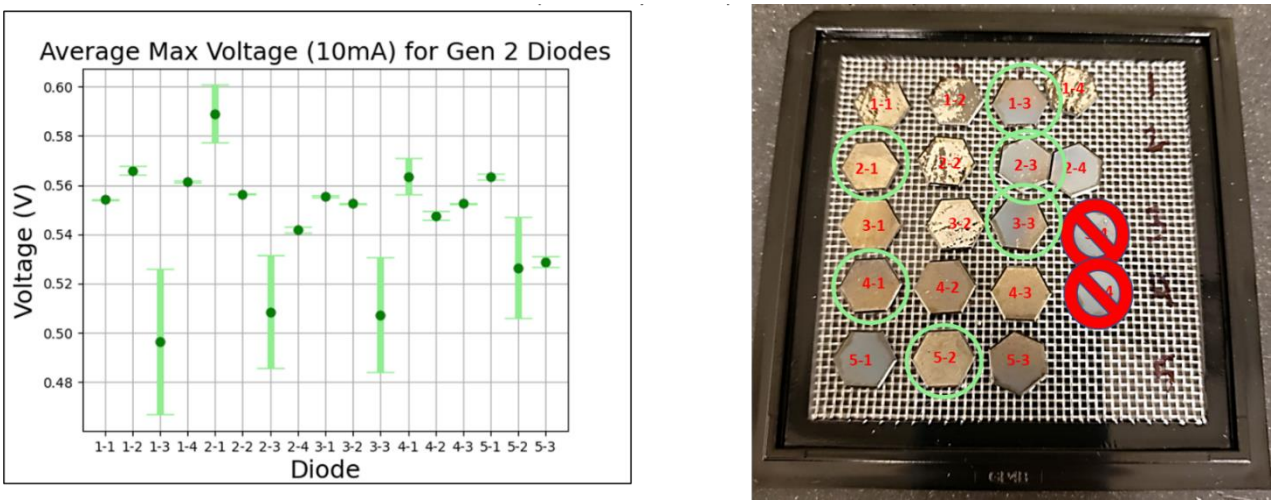

Figure 6.3.5. Results of the repeatability study for the forward voltage at 10mA measurements. On the left are the measurement averages with their respective standard deviations. On the right is an image of the Gen 2 diodes. Each diode has been labeled with its name in red. Circled in green represents the diodes with the greatest variability from this study. The two diodes that are crossed out never produced any useable data. These two diodes correspond to the "Complete, possible re-test" label found in Table 6.3.1.

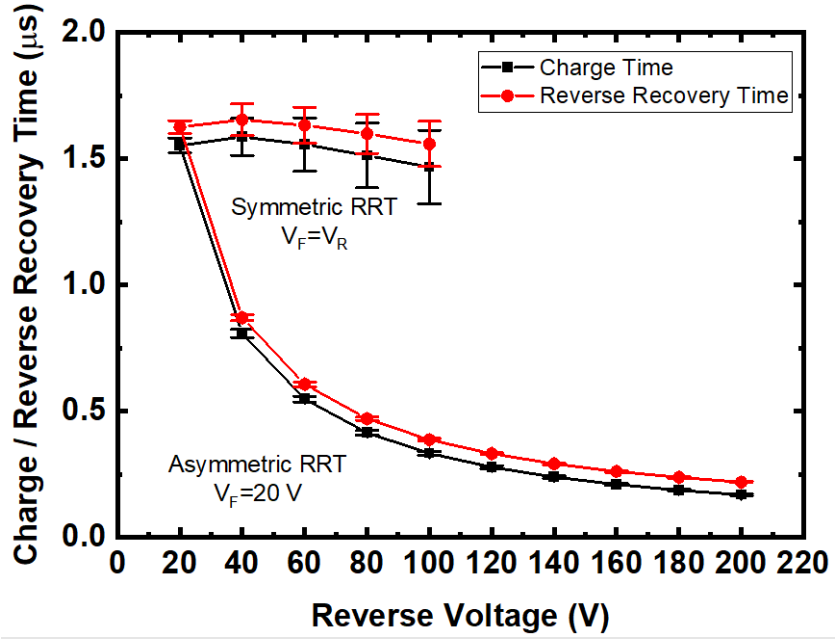

Figure 6.3.6. Charge storage and Reverse recovery time of single stack Gen-2 DSRD diodes as a function of reverse pulse voltage. The symmetric RRT is for test conditions where forward and reverse pulses were of equal amplitude, while asymmetric RRT is for increasing reverse voltage for 20 V forward pulse amplitude. Reverse recovery time is the sum of the charge storage time and the transition time (see figure 6.3.2 (b)).

Development of a standardized procedure for RRT measurements is still under investigation since the ideal testing conditions for calculating minority carrier lifetimes are still in progress. However, the measurement results found thus far from the Gen2 and EG1500 DSRDs have shown greater consistency in testing results than the DC measurements (refer to Figure 6.3.6).

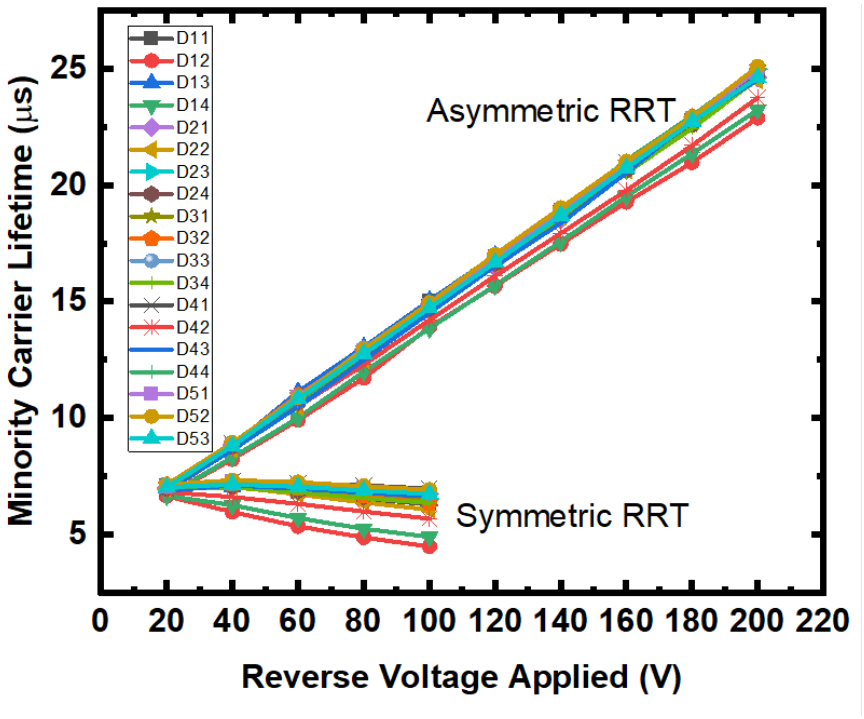

Figure 6.3.7. Minority carrier lifetime obtained for single-stack Gen-2 diodes as a function of applied reverse voltage.

The minority carrier lifetime in the DSRDs were calculated using the Kingstone [5] equation given by:

$$\frac{1}{1 + I_R/I_F} = erf\left(\frac{t_s}{\tau_{eff}}\right)^{1/2}$$

where I_R, I_F, and τ_{eff} represent the reverse current, forward current, and the minority carrier lifetime, respectively. Since the carrier lifetime is expected to be independent of the reverse voltage applied, the observed linear relationship between them may indicate that the calculated parameter is not actually the carrier lifetime as the depending on the diode thickness, the calculated time can also represent the carrier transit time [5].

6.3.5 *Summary of Significant Findings and Mission Impact*

(A.1) We have identified several KPIs pertaining to the diode characterization procedures. These KPIs have been stored within a matrix template that will also serve as a logistical catalog of legacy diodes and testing procedures.

(A.4) Several diode characterization procedures have been updated. These procedures include both the IV and CV measurements. Both methods now have newly updated SOPs that track and catalog any changes made to the processes. Refer to Table 6.3.1 for a summary of the testing performed on each diode. Several testing issues have presented themselves during this process. One issue is the large variability between each IV measurement. Several DSRDs had to be measured multiple times to get data that did not appear to be noise. The IV measurement procedure is still in progress since the current equipment is only capable of achieving –200 V, which is far too low for measuring breakdown voltages.

A standardized testing procedure for RRT measurements is still in progress. However, several Gen2 and all the EG1500 diodes have been tested (reference Table 6.3.1). Development of this test will lead to an increased understanding in minority carrier lifetime measurements and how they relate to the forward pumping time for pulsing.

(A.6) The results of the repeatability study showed that there is variation within the IV and CV measurements, however, the reverse recovery test showed the least variability among the tests performed. Several factors can be attributed to this variation, including the diode being damaged.

The Gen2 and the EG1500 diodes that have completed RRT testing have shown lower deviations than the other DC measurements (refer to Figure 6.3.6). A repeatability study, similar to the IV and CV tests, will need to be performed to confirm this result.

6.3.6 *References*

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6.4 DSRD-Based Pulsed Power Source Systematic Topological Optimization

(Gyanendra Bhattarai & Roy Allen)

6.4.1 *Problem Statement, Approach, and Context*

Primary Problem: Inductive energy storage (IES) and release pulse generators that use drift-step recovery diodes (DSRDs), when able to achieve ones of gigawatts in ones of nanoseconds, are large, heavy, and require liquid-based cooling systems to dissipate the excess heat they generate during operation; therefore, rendering them impracticable for Navy afloat missions.

Solution Space: Systematically develop a modular architecture of a pulser circuit using DSRDs by determining the optimal permutation of series and parallel combinations of the base pulser unit, and its component parameters, in order to maximize the peak voltage, peak power, and volumetric power density without sacrificing the desired nanosecond risetime of the pulses generated or requiring liquid-based cooling.

***Sub-Problem*:** DSRDs are not domestically available COTs components. The small-batch quantities that are manufactured have statistically significant variations in their performance parameters. In addition, SPICE models of these diodes are not accurate and do not account for their sample-to-sample parameter variability. The above-mentioned reasons may lead to an inaccurate simulation model of the pulser that may result in a difference between the simulation and experimental results.

State-of-the-Art (SOTA): DSRD-based pulsers (equivalent in size to the pulse generators developed for this effort, i.e., ~0.01-m^3, ~2-kg) can achieve 6-kV, 200-ps risetime, and <500 ps FWHM across a 50 Ω load.

Deficiency in the SOTA: DSRD-based air-cooled versions are limited to PRFs of < 15 kHz. Additionally, current studies on SOS-IES pulse generators attempt to present only the best-case circuit configurations, meaning a comprehensive study on optimizing the number and ratio of parallel branches and series-connected stages aiming to achieve maximum gain and efficiency (reducing thermal load) is missing in the SOTA.

Solution Proposed: Systematically determine topological SOS-IES circuit configurations and the necessary components therein that maximize voltage gain and efficiency and minimize the rise-time achieved by the pulser.

Relevance to OSPRES Grant Objective: IES pulse generators using DSRDs can remove the need for photo-triggered switches and their laser sub-systems. They are ideal for triggering sub-nanosecond rise-time sharpeners (SAS, D-NLTL, etc.), reducing overall cost, volume, and weight.

Risks, Payoffs, and Challenges:

Risks: Domestically manufactured (U.S.-based) DSRDs which possess sub-optimal doping profiles may lead to sub-optimal pulse generators with sub-optimal performance. The data gathered from these sub-optimal circuits would then be used to train the genetic/machine learning algorithms developed and the redesign of future topologies constructed; ultimately leading to spurious conclusions regarding ideal topological circuit

configurations with ‘N’ number of series-connected stages, each containing ‘M’ parallel branches.

Payoffs: Leveraging collaborative partnerships with U.S.-based manufacturers of DSRDs, the ability to refine and control the performance characteristics of the diodes themselves, along with the ability to simulate and manufacture the DSRD pulsers in-house, enables a holistic soup-to-nuts capability to optimize, produce, and evaluate these nanosecond pulse generators.

Challenges: Determining the superlative ratio of design/development (through numerical analysis) to the effort put towards experimental testing/evaluation of the DSRD pulser is challenging due to the novelty of the approach. The complexity of the theoretical model is extreme given the M×N number of DSRD base unit stages within the pulse forming network along with inaccurate DSRD spice model and large sample-to-sample variability.

6.4.2 Tasks and Milestones / Timeline / Status

(A) Milestone – Develop theory of DSRD pulse generator to facilitate optimization of 1×1 and M×N pulse generator [***Ongoing***].

(B) Milestone – Construct/demonstrate a DSRD-based 2×2 IES pulse generator prototype capable of producing $\geq$4 kV peak voltage, $\leq$1 ns risetime, $\leq$5 ns FWHM, $\geq$320 kW peak-power, $\geq$1 kHz PRF, $\geq$100 shots-per-burst, $\geq$5 number of bursts [***Completed JUL21***].

(C) Milestone – Construct/demonstrate a DSRD-based 1×1 IES pulse generator prototype capable of testing individual and combinations of diode stacks to acquire performance data [***Completed AUG21***].

(D) Milestone – Construct/demonstrate a DSRD-based 4×2 IES pulse generator prototype capable of producing $\geq$12 kV peak voltage, $\leq$1 ns risetime, $\leq$5 ns FWHM, $\geq$3 MW peak-power, $\geq$100 kHz PRF, $\geq$1,000 shots-per-burst, $\geq$500 number of bursts [*Ongoing, estimated completion by OCT21*].

1. Task – Develop revised layout in Altium and order PCB and components. [***Completed – SEP21***];
2. Task – Populate pulse generator and begin testing & evaluation phase [***Completed – NOV21***];

(E) Milestone – Develop waveform inverter which, when combined with the pulser from Milestone C, enables a balanced differential waveform output with >90% inverted signal fidelity. [***Completed – DEC21***].

(F) Milestone – Construct/demonstrate a M×N pulse generator prototype capable of producing $\geq$20 kV peak voltage, $\leq$1 ns risetime, $\leq$2 ns FWHM, $\geq$8 MW peak-power, $\geq$100 kHz PRF, and $\geq 2\sigma_{V_{peak}}$, which operates in continuous-burst mode as a viable candidate for OSPRES Contract source alternative [*on hold until Milestone C & D are completed*].

6.4.3 *Progress Made Since Last Report*

(A) There were outstanding questions regarding the working principle of a DSRD pulse generator, for which the answers could help optimize circuit components for better performance. A circuit analysis for a single-bar (1×1) DSRD pulser is presented, and pulser design with simulated output voltage >26 kV is demonstrated given that the driving MOSFET can handle ~600 A of current for ~500 ns.

(B) The 4×2 DSRD-based pulse generator has been populated and is currently being tested and evaluated.

6.4.4 *Technical Results*

6.4.4.1 Working Principle of a DSRD pulse generator

A DSRD pulser works under a simple principle, which we will explain below. When an asymmetric biasing source (Reverse bias voltage is much higher than the forward bias voltage) is applied to a DSRD through an inductor, as shown in Figure 6.4.1, the diode conducts during the forward cycle with a minimal resistance and stores a certain quantity of charge within it. If the diode is then quickly reverse biased by the high-voltage reverse cycle within a time such that the stored charge carriers are still free (not recombined), the diode remains conducting with a very small resistance as long as the stored charge in the diode are not extracted completely. If the time period of the reverse bias is set such that the stored charge carriers are extracted completely before the reverse bias returns to zero, the DSRD quickly turns off and the diode current drops to zero within a couple of nanoseconds. Due to this large dI/dt, a large voltage pulse $V = L\,dI/dt$ appears across the inductor with risetime equal to the diode snap-off time.

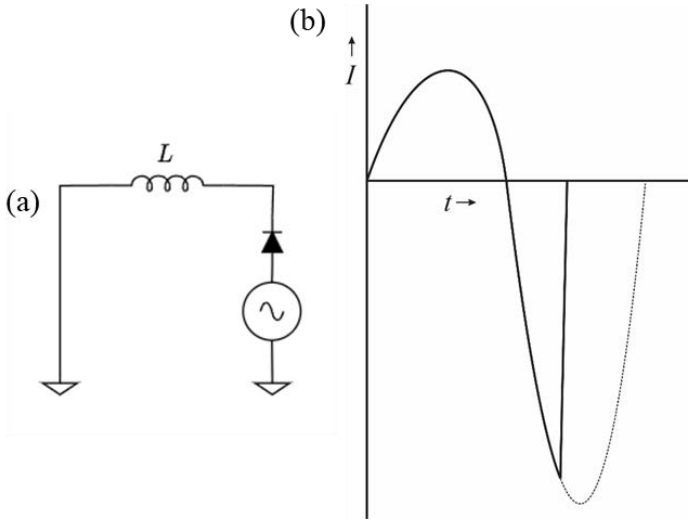


Figure 6.4.1. a) A simple DSRD pulser circuit with asymmetric biasing source and b) current in the circuit in absence of diode (dashed line) and current through the diode (solid line). The time period of the reverse cycle should be long enough so that the DSRD snaps off before the current (dashed line) returns back to zero.

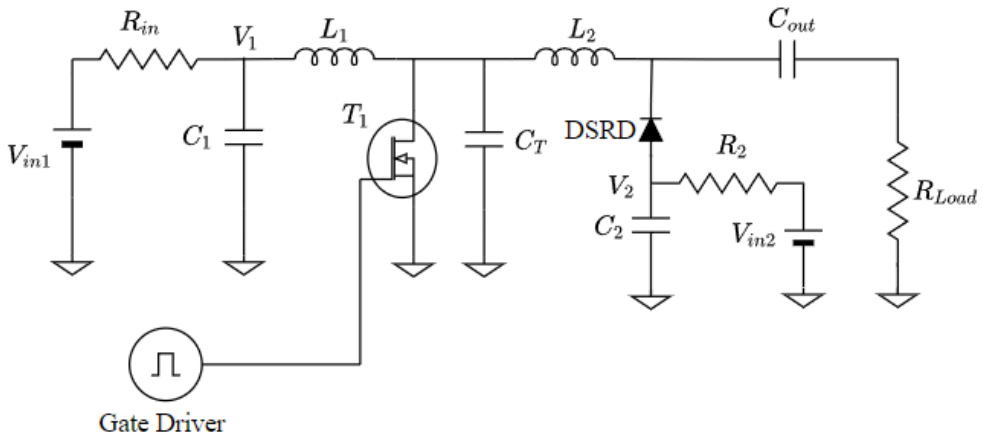


Figure 6.4.2. A schematic of a MOSFET-driven single-bar DSRD pulser circuit currently being used for study.

A simple circuit diagram of a MOSFET-driven single-bar DSRD pulser circuit is shown in Figure 6.4.2. Although different circuit topologies could be possible to achieve the asymmetric biasing, here in this circuit, the forward and reverse biasing (pumping) of the diode is achieved by two different time regimes corresponding to the ON and OF state of the MOSFET. When the circuit is in initial state, i.e., the MOSFET is off, the inductors L_1 and L_2 are short and the prime voltage sources V_{in1} and V_{in2} of equal potential charge the capacitor C_1, C_2 and C_T to the voltage $V_1 = V_2 = V_{in1} = V_{in2}$. If one wants to ensure that the DSRD remains in OFF state, the voltage V_{in2} can be made slightly smaller than V_{in1} so the DSRD remains in reverse bias.

Forward pumping Circuit Analysis

When the MOSFET is turned ON at $t = 0$, the capacitor C_T is shorted through the MOSFET and the DSRD gets forward biased with the voltage V_2. Although the MOSFET and the diode have small series resistances and parallel capacitances, it is reasonable to assume that the series resistances are negligible, and the parallel capacitances are shorted. The capacitors C_1 and C_2 are then discharged through the inductors L_1 and L_2 respectively initiating independent circuit oscillations. Because the resonance frequencies of the two circuits are made very high and the charging time of C_1 and C_2 through the resistors R_1 and R_2 are very long, for high frequency operations, the capacitors can be assumed to be disconnected from the biasing sources. Figure 6.4.3 shows the simple equivalent circuit diagram of the pulser during forward pumping.

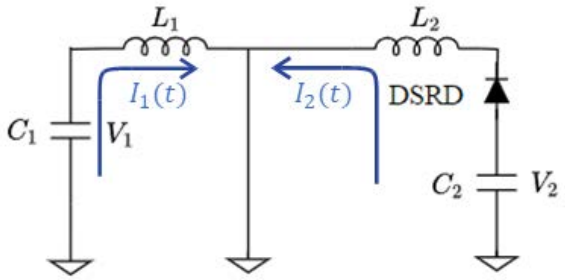


Figure 6.4.3. Equivalent circuit diagram of forward pumping stage of DSRD pulser circuit.

The oscillating current through the inductors L_1 and L_2 during the forward pumping of diode are obtained by solving the Kirchhoff's voltage equations

$$\frac{Q_1(t)}{C_1} - L_1 \frac{\mathrm{d}I_1(t)}{\mathrm{d}t} = 0 \tag{1}$$

And

$$\frac{Q_2(t)}{C_2} - L_2 \frac{\mathrm{d}I_2(t)}{\mathrm{d}t} = 0 \tag{2}$$

Realizing that $I_1(t) = -\mathrm{d}Q_1(t)/\mathrm{d}t$ and $I_2 = -\mathrm{d}Q_2(t)/\mathrm{d}t$, it is easy to find that

$$I_1(t) = \sqrt{\frac{C_1}{L_1}}\, V_1 \sin \frac{1}{\sqrt{L_1 C_1}} t \tag{3}$$

and

$$I_2(t) = \sqrt{\frac{C_2}{L_2}}\, V_2 \sin \frac{1}{\sqrt{L_2 C_2}} t \tag{4}$$

Effect of L_2 and C_2 in forward pumping and injected charge on diode

The current $I_2(t)$ represents the forward pumping current. The optimum charging time of a diode at a certain current level is a property of the diode itself, which fundamentally depends on the carrier recombination time and the free carrier distribution over the diode volume. Experiments, such as reverse recovery test (RRT), can be used to extract an optimum charging/pumping time for a given current input level. As the current through the diode is oscillatory, the current pumping time is equal to the half of the time period of its oscillation. Thus, the total charge injected into the diode is

$$Q_{\text{inj}} = \int_0^{\pi\sqrt{L_2C_2}} I_2(t)\,\mathrm{d}t = 2C_2V_2 \tag{5}$$

This shows that the injected charge does not depend on the inductance L_2, but can be increased by increasing the capacitance C_2 or by increasing the voltage V_2. However, there are limitations on increasing these values, which we will discuss later.

Preparing for the reverse pumping and optimum trigger length, T_{ON}

For the reverse pumping, we turn the MOSFET off after turning it on for a total time of T_{ON}, the trigger length. However, before we describe the circuit action during reverse pumping, it is important to analyze what happens in the current through the inductor L_1 during forward pumping, which has a major contribution on the reverse pumping of the DSRD. The current through inductor L_1 is

$$I_1(t) = \sqrt{\frac{C_1}{L_1}}V_1 \sin\frac{1}{\sqrt{L_1C_1}}t$$

If we set the time period of the oscillation of $I_1(t)$ to be equal to that of the forward pumping current, i.e., $\sqrt{L_1C_1} = \sqrt{L_2C_2}$, the current through the inductor L_1 drops to zero when the diode has just completed the forward pumping stage. At this point, an ideal condition is achieved where there is no current through the entire circuit. The two current loops are exactly mirror image of each other. If the MOSFET is turned off at this time, the diode does not get any reverse potential to extract the injected charge (see Equation (21) later). To reverse bias the DSRD quickly, we need a high voltage pulse across the MOSFET when it is turned off. This can be achieved by interrupting a large current $I_1(t)$ through the inductor L_1. The quick turn OFF of the MOSFET provides such fast current interruption, but we need to select the components L_1 and C_1 such that the pulse reverse voltage is at maximum possible value when the MOSFET turns off.

The total turn-on time of the MOSFET, T_{ON}, is another important parameter to reverse bias the DSRD effectively. Due to the oscillatory nature, the diode current naturally drops to zero and reverses its direction at $t = \pi\sqrt{L_2C_2}$. Thus, the best time for the additional reverse voltage pulse due to the interruption of current $I_1(t)$ to appear is between $t = \pi\sqrt{L_2C_2}$ and $t = (3/2)\pi\sqrt{L_2C_2}$. A graphical visualization of the reverse bias current for different choice of trigger length is shown in Figure 6.4.4.

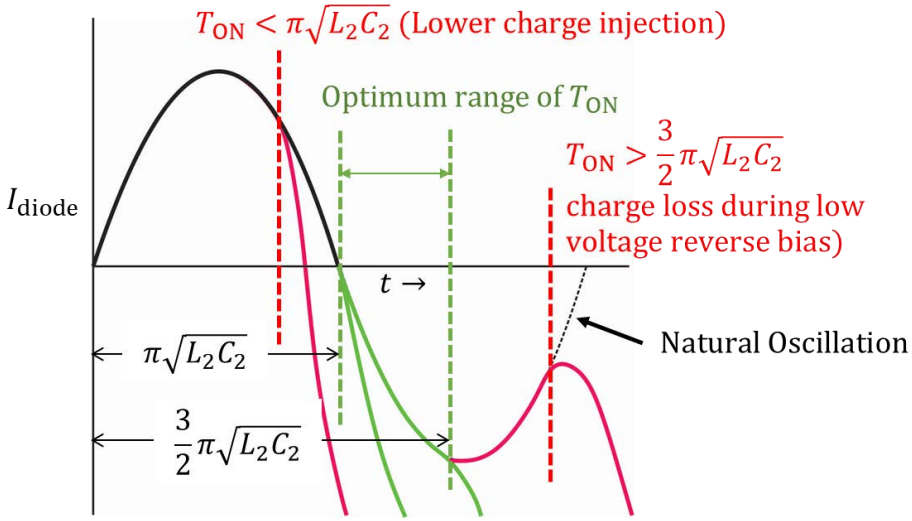


Figure 6.4.4. Representation of reverse current through DSRD for different MOSFET trigger length, T_{ON}. $T_{ON} < \pi\sqrt{L_2C_2}$ results in lower charge injection while $T_{ON} > \frac{3}{2}\pi\sqrt{L_2C_2}$ results in loss of injected charge during low voltage reverse bias.

It can be seen from Figure 6.4.4 that shorter trigger length results in lower charge injection while longer trigger length causes the injected charge to be extracted with lower reverse voltage (which cannot initiate the sharp cut-off of diode current). Thus, for optimum charge injection and efficient charge extraction, we need

$$\pi\sqrt{L_2C_2} \leq T_{ON} \leq \frac{3}{2}\pi\sqrt{L_2C_2} \tag{6}$$

This will ensure that the additional reverse pulse voltage constructively adds to the reverse voltage due to circuit's natural oscillation while keeping the total injected charge during the forward pumping time unaffected.

Reverse Pumping Circuit analysis

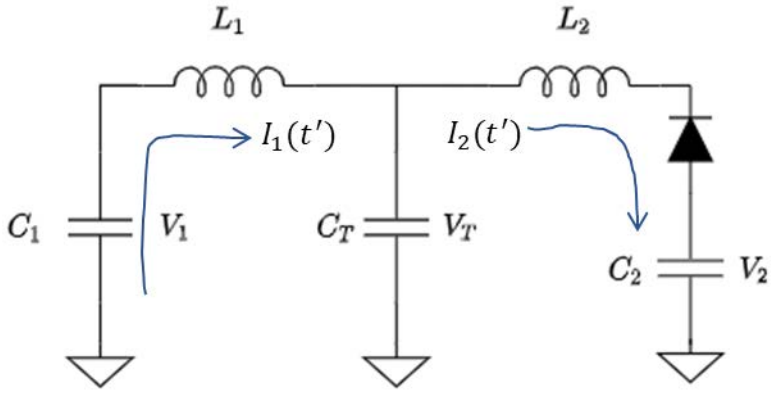


Figure 6.4.5. Equivalent circuit diagram of DSRD pulse generator when the MOSFET is turned off. The directions of currents show the actual direction of current immediately after turning off the MOSFET

An equivalent circuit diagram for the reverse pumping stage of the DSRD pulser circuit is shown in Figure 6.4.5 where the MOSFET is turned off. The direction of currents shown are the actual direction of current immediately after the MOSFET is turned off.

Exactly at $t = T_{\mathrm{ON}}$, the MOSFET is only triggered to turn off but is not completely off. The time that the MOSFET needs to change its state from ON to OFF is independent of the circuit elements, and it cannot be predicted. If t_{off} is the time required for the MOSFET to turn off, then $t = T_{\mathrm{ON}} + t_{\mathrm{off}}$ is the true initial condition for the reverse pumping circuit. Thus, for reverse circuit, we define the time variable as $t' = t + T_{\mathrm{ON}} + t_{\mathrm{off}}$

For any time t', the voltage and current Kirchhoff's law for reverse pumping circuit can be written as

$$\frac{Q_1(t')}{C_1} - L_1\frac{dI_1(t')}{dt'} - \frac{Q_T(t')}{C_T} = 0 \tag{7}$$

and

$$\frac{Q_T(t')}{C_T} - L_2\frac{dI_2(t')}{dt} - \frac{Q_2(t')}{C_2} = 0 \tag{8}$$

Differentiating both of the equation above w.r.t time and noting $-dQ_1(t')/dt' = I_1(t')$, $dQ_T/dt' = I_T(t') = I_1(t') - I_2(t')$, and $dQ_2(t')/dt' = I_2(t')$, we can write

$$\frac{d^2I_1(t')}{dt'^2} = -\frac{1}{L_1C_{1T}}I_1(t') + \frac{1}{L_1C_T}I_2(t') \tag{9}$$

and

$$\frac{d^2I_2(t')}{dt'^2} = \frac{1}{L_2C_T}I_1(t') - \frac{1}{L_2C_2T}I_2(t') \tag{10}$$

where

$$C_{1T} = \frac{C_1C_T}{C_1 + C_T}\ ; \qquad C_{2T} = \frac{C_2C_T}{C_2 + C_T} \tag{11}$$

The set of differential equations (9) and (10) can be written in terms of a matrix equation as

$$\frac{d^2\vec{X}}{dt^2} = A\,\vec{X} \tag{12}$$

where

$$A = \begin{bmatrix} -\dfrac{1}{L_1C_{1T}} & \dfrac{1}{L_1C_T} \\ \dfrac{1}{L_2C_T} & -\dfrac{1}{L_2C_{2T}} \end{bmatrix}; \quad \vec{X} = \begin{bmatrix} I_1(t') \\ I_2(t') \end{bmatrix} \tag{13}$$

As the circuit elements contain only inductors and capacitors, we know that the currents in the circuit oscillate, and the oscillation frequencies are given by the eigenvalues of the matrix A obtained by solving the characteristic equation as

$$\begin{vmatrix} -\frac{1}{L_1 C_{1T}} - \lambda & \frac{1}{L_1 C_T} \\ \frac{1}{L_2 C_T} & -\frac{1}{L_2 C_{2T}} - \lambda \end{vmatrix} = 0$$

or,

$$\lambda^2 + \left[\omega_1^2 \frac{C_1 + C_T}{C_T} + \omega_2^2 \frac{C_2 + C_T}{C_T}\right]\lambda + \omega_1^2 \omega_2^2 \frac{C_1 + C_2 + C_T}{C_T} = 0 \tag{14}$$

The discriminant of the quadratic equation (14) can be shown to be positive which gives real eigenvalues for the matrix. The eigenvalues are

$$\lambda_{\pm} = -\frac{1}{2}[\omega_1^2(1+a) + \omega_2^2(1+b)] \pm \frac{1}{2}\sqrt{\left(\omega_1^2(1+a) - \omega_2^2(1+b)\right)^2 + 4ab\omega_1^2\omega_2^2} \tag{15}$$

where

$$a = \frac{C_1}{C_T}; \qquad b = \frac{C_2}{C_T} \tag{16}$$

Because the circuit contains capacitors and inductors only, we can expect the solution for the currents to be oscillatory. The general solutions for the current are then written as

$$I_1(t') = A\cos\sqrt{\lambda_1}t' + B\sin\sqrt{\lambda_2}t' \tag{17}$$

And

$$I_2(t') = C\cos\sqrt{\lambda_1}t' + D\sin\sqrt{\lambda_2}\,t' \tag{18}$$

where the constants A, B, C, and D are to be determined using the initial conditions.

Although it is not completely analytical, it is reasonable to assume that $I_1(t)$ drops to zero when the MOSFET is completely off ($t' = 0$), i.e.,

$$I_1(t' = 0) = 0 \tag{19}$$

and the rate of change of $I_1(t)$ is

$$\left[\frac{\Delta I_1(t')}{\Delta t'}\right]_{t'=0} = \frac{\sqrt{\frac{C_1}{L_1}}V_1 \sin\left(\frac{1}{\sqrt{L_1 C_1}}\,T_{\mathrm{ON}}\right)}{t_{\mathrm{off}}} \tag{20}$$

The voltage across the inductor L_1 at this time is then

$$V_{L1}(t' = 0) = L_1\frac{\Delta I_1(t')}{\Delta t'} = \frac{\sqrt{L_1 C_1}}{t_{\mathrm{off}}}\,V_1 \sin\left(\frac{1}{\sqrt{L_1 C_1}}\,T_{\mathrm{ON}}\right)$$

or

$$V_{L1}(t'=0) = \frac{T_{ON}}{t_{off}} V_1 \left[\frac{\sqrt{L_1C_1}}{T_{ON}} \sin\left(\frac{T_{ON}}{\sqrt{L_1C_1}}\right)\right] \quad (21)$$

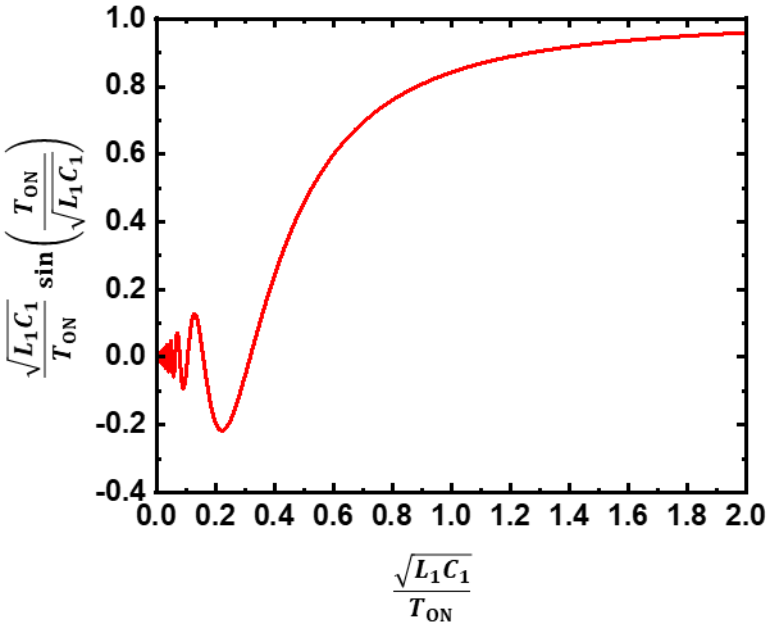


Figure 6.4.6. Variation of the oscillating part of Equation (21) as a function of $\sqrt{L_1C_1}/T_{\mathrm{ON}}$.

Figure 6.4.6 shows the variation of amplitude of the reverse voltage pulse as a function of time period of oscillation $\sqrt{L_1C_1}$. Although the amplitude keeps increasing for increasing time period, we can see that it attains >95% of the maximum value for

$$\frac{\sqrt{L_1C_1}}{T_{\mathrm{ON}}} \geq 2$$

or

$$L_1C_1 \geq 4T_{\mathrm{ON}}^2 \quad (22)$$

And the corresponding reverse voltage amplitude in this condition becomes

$$V_{L1}(t'=0) \geq 0.95V_1.\frac{T_{\mathrm{ON}}}{t_{\mathrm{off}}}$$

Increasing the time period beyond this value does not increase the reverse voltage amplitude significantly. Because the MOSFET turn-off times are on the order of tens of nanoseconds, it is possible to achieve a very high reverse bias voltage compared to the prime source voltage V_{in1}.

High voltage pulse generation

As the high reverse bias voltage pulse appears across the diode at $t' = 0$ (within couple of nanoseconds after $t = T_{\mathrm{ON}}$), the injected charge carriers are extracted rapidly, and a sharp decrease in the reverse current observed once the carriers are completely

extracted. If $\mathrm{d}I_D/\mathrm{d}t$ is the rate of change of the DSRD reverse current when it snaps off, the pulse voltage appeared across the diode (or load) is given by

$$V_{\mathrm{out}} \approx L_2 \frac{\mathrm{d}I_D}{\mathrm{d}t} \tag{22}$$

Although we have not presented the total solution for the currents in the reverse pumping stage, it can be seen that the currents at $t' > 0$ do not significantly alter the output pulse voltage as it is generated immediately after the MOSFET is turned off. However, the current oscillation in this time regime can initiate multiple high voltage pulses, which are undesirable. We will present the complete analysis in the next month's report.

Optimization Sequence

The very first step in optimizing the DSRD pulse generator circuit parameters is to determine the optimum charge pumping time for a given amplitude of forward pumping current. This process is not straight forward as the total quantity of free charge carrier remaining within the diode after the forward pumping cycle depends on the carrier recombination time. Experiments such as reverse recovery test (RRT) with varying pulse duration can be used to find the optimum combination for a given diode. Once the optimum forward pumping time and current is determined, we choose the circuit parameters as

$$t_{\mathrm{pump}} = \pi\sqrt{L_2 C_2} \tag{i}$$

and the amplitude of the diode forward current

$$I_{20} = \sqrt{\frac{C_2}{L_2}} V_{in2} \tag{ii}$$

Because we don't have any restriction on the voltage source V_{in2} yet, we choose C_2 and L_2 to satisfy Equations (i) and (ii). This gives

$$C_2 = \frac{I_{20} t_{\mathrm{pump}}}{\pi V_{in2}} \tag{iii}$$

and

$$L_2 = \frac{V_{in2} t_{\mathrm{pump}}}{\pi I_{20}} \tag{iv}$$

Once V_{in2} is chosen, it is reasonable to choose $V_{in1} \geq V_{in2}$ as this allows higher reverse pumping voltage.

For efficient reverse biasing, we recall Equation (6) to choose the MOSFET trigger length

$$t_{\mathrm{pump}} \leq T_{\mathrm{ON}} \leq \frac{3}{2} t_{\mathrm{pump}}$$

And for optimum reverse voltage pulse amplitude, we recal Equations (21) and (22) to get

$$L_1 C_1 \geq 4T_{\mathrm{ON}}^2 \qquad (v)$$

Visualizing Optimal Pulser Performance with LTspice Simulations

Applying the foregoing theory to the 1×1 pulser circuit in LTspice enables visualizing the working principle of the slow, low amplitude forward pumping current of inductor in stage one, followed by the high reverse current with a sharp “spike” (snap-off) at the time of carrier extraction within the DSRD.

Figure 6.4.7 presents the current through and voltages across some circuit elements of an optimized MOSFET-driven 1x1 DSRD pulse generator circuit. The ancillary component circuit parameters utilized in this circuit were determined by the theoretical analysis presented, and then performing a brute-force parameter sweep optimization through changing one variable per optimization step while holding others constant. The optimized circuit parameters are listed below. Refer to Figure 6.4.2 for circuit components.

$$\begin{aligned} V_{in1} &= V_{in2} = 300\ \mathrm{V} \\ C_2 &= 120\ \mathrm{nF} \\ L_2 &= 150\ \mathrm{nH} \\ t_{\mathrm{pump}} &= \pi\sqrt{L_2 C_2} = 420\ \mathrm{ns} \\ T_{\mathrm{ON}} &= 530\ \mathrm{ns}; \qquad 420\ \mathrm{ns} < 530\ \mathrm{ns} < 630\ \mathrm{ns} \\ L_1 &= 175\ \mathrm{ns} \\ C_1 &= 10 - 400\ \mu\mathrm{F} \\ C_T &= C_{\mathrm{out}} = 15\ \mathrm{nF} \end{aligned}$$

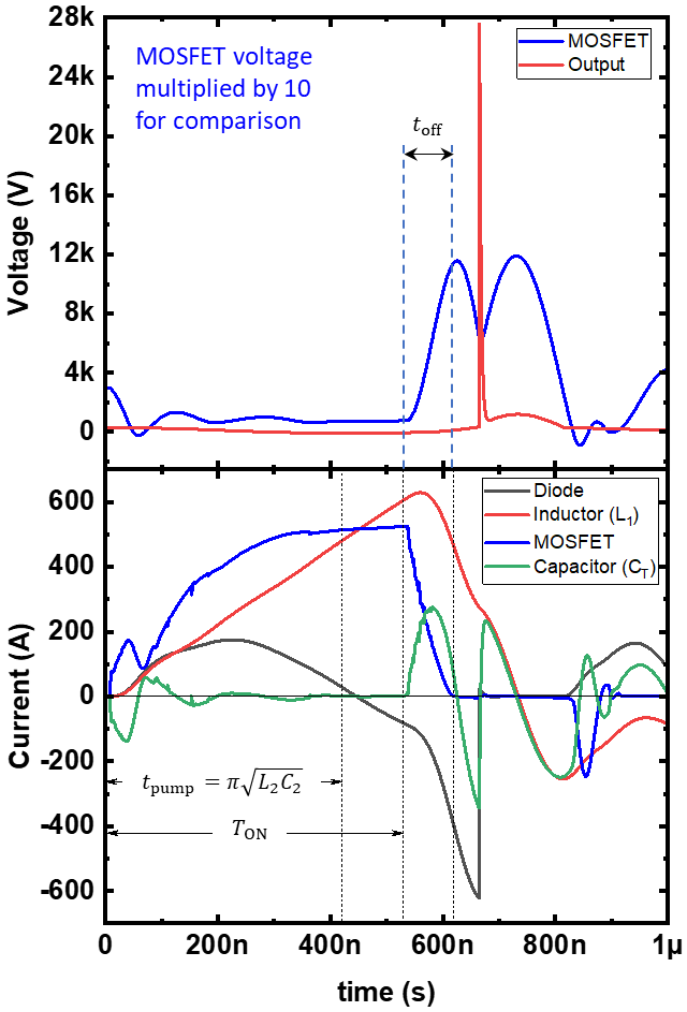


Figure 6.4.7. Simulated current and voltages through different circuit elements and across them for an optimized MOSFET-driven DSRD pulse generator.

We can see from the figure that the diode current (I_2) during forward pumping (black curve) follows nearly a sinusoidal wave form with its time period nearly equal to double of the pumping time t_{pump}. During the same time, current (I_1) through the inductor L_1 increases almost linearly, which is due to the very long time period of the L_1C_1 resonance circuit. The current through the capacitor C_T is observed only for a small time because of its short discharge time. The trigger length (T_{ON}) for the MOSFET is set to 530 ns which lies between t_{pump} and 3 ($t_{\text{pump}}/2$) according to the theory presented above. When the MOSFET is triggered to turn OFF at $t = T_{\text{ON}}$, it turns off quickly within the turn off time t_{off} causing an interruption in the inductor current I_1. This interruption induces a large reverse bias (~1.2 kV) across the diode. We can see from the figure that the large reverse bias appears at a time very close to when the MOSFET current drops to zero because this is the time when the rate of decrease of current is maximum. The large reverse bias then

sweeps out the charge injected during forward pumping, setting a large reverse current (~600A) through the diode. Once the injected charges are completely swept out, the diode returns to its reverse biased "OFF" state instantaneously (within couple of nanoseconds) showing a near vertical current profile. This large current decrease rate then sets a large output voltage ($V_{out} = L_2 \, \mathrm{d}I_2/\mathrm{d}t$).

6.4.5 *Summary of Significant Findings and Mission Impact*

(A) A simplified theory of a MOSFET-driven 1×1 DSRD pulse generator has been presented. The theory guides the optimization of pulse generator performance systematically based on what actually happens in the circuit with changing circuit parameters. A 1×1 DSRD pulse generator with optimized circuit components that can theoretically produce an output voltage of ~28 kV is presented.

(B) Successful construction and operation of a 2×2 DSRD-based IES pulse generator prototype has been completed which meets or exceeds the milestone's required key performance metrics. Shown in Table 6.4.1 are the previous and current pulse generator's performance specifications in comparison to a similar 2×2 pulser developed by Kesar et al. [1] using DSRDs, and to that of a commercial off-the-shelf (COTS) DSRD pulser of similar space and weight developed by Megaimpulse (i.e., PPM-0731) which also uses DSRDs with silicon avalanche shapers (SAS) [2]. Although the Megaimpulse pulser utilizes a SAS with a <500 ps risetime (a threshold we do not intend to go below due to Commerce Controlled List limitations), it is interesting to compare the results of linear voltage gain and peak power of this system, to that of one that utilizes a SAS. The current permutation of the 2×2 DSRD-IES pulser developed by MIDE under the ONR OSPRES Grant is able to achieve a higher peak voltage and shorter risetime than DSRD-based pulsers reported in the literature of comparable space and weight as well as those commercially available. The ability to generate a linear voltage gain of 40.8 to produce over a Megawatt of peak power into a 50 Ω load while achieving a peak voltage output standard deviation of 2σ when operating at a PRF of at least 100 kHz, brings this technology to the forefront of viable options to potentially support the Naval afloat mission.

Table 6.4.1. Comparison of DSRD-based IES Pulse Generator Performance.

KPM	Units	MIDE - V1 Previous	MIDE - V2 Current	Kesar *et al.* SOTA	MI-PPM0731 COTS
V_{supply}	V	225	180	300	160
T_{ON}	ns	100	340	?	200
V_{peak}	kV	5.59	**7.35**	5	6.3
Gain	V/V	24.8	**40.8**	16.7	39.4
$\tau_{rise,20\text{-}90\%}$	ns	1.2	1.142	1.96	0.12
dV/dτ	kV/ns	4.66	6.44	2.55	**52.50**
FWHM	ns	2	5.48	2.27	0.35
PW	ns	5	7	3.5	2.5
Z_{LOAD}	Ω	50	50	50	50
P_{peak}	MW	0.625	**1.080**	0.500	0.794
E_{pp}	mJ	0.125	0.154	0.143	0.318
PRF_{max}	kHz	100	100	100	15
Burst	shots	100	100	*N/A*	100
	%	100	100	*N/A*	100
SD_{Vpeak}	σ	> 2	**> 2**	*N/A*	*N/A*
	%	96.5	**97.8**	*N/A*	*N/A*

(C) Discrepancies exist in the obtained data for different series combinations and different samples of 7-stack DSRDs, which may be attributed to the inconsistencies in their manufacturing process. Future works in the coming months include carrying out further testing on the 1×1 DSRD-based pulse generator (base-unit) circuit using more combinations of series-connected as well as parallel-connected DSRD stacks.

6.4.6 *References*

[1] https://www.onsemi.com/pdf/datasheet/nvh4l020n120sc1-d.pdf

[2] https://cms.wolfspeed.com/app/uploads/2020/12/C2M0045170P.pdf

6.5 All-Solid-State Sub-ns MW Pulse Generators with Semiconductor Sharpeners

(Gyanendra Bhattarai)

6.5.1 *Problem Statement, Approach, and Context*

***Primary Problem*:** Broadband high-power microwave (HPM) systems need sub-nanosecond tens-of-MW pulses. Hydrogen spark gaps (HSG), traditionally used for such purposes, are severely limited by their low pulse repetition frequency (PRF ~1 kHz) and poor device lifetime (shot life ~1000 pulses), ill-suited to achieve the SWaP metrics

necessary for HPM pulse generators for the Navy afloat mission. Competitive solid-state solutions, such as inductive energy storage (IES) systems, utilizing a series stack of fast-opening diodes (drift-step recovery diodes (DSRD) and semiconductor opening switches (SOS)), have not been shown to break nanosecond barriers.

***Solution Space*:** Use viable pulse shaping/compression technologies based on semiconductor closing switches (e.g., delayed breakdown diodes (DBD), and fast ionization dynistors (FID)) to increase the peak power and shorten the rise time of the pulses produced by the DSRD-based pulse generator. Pulse sharpening/compression reduces the otherwise additional complexity of increased M×N stages within the pulser topology; a desired result towards achieving optimal SWaP metrics of the pulse generation system without sacrificing PRF, shot lifetime, and thermal management requirements. (*Please refer to the June 2021 MSR for full problem and solution space description).*

***Sub-Problem 1*:** Achieving an order of magnitude increase in peak power (1-to-10 MW) through compression/sharpening methods requires series and parallel stacks of semiconductor closing switches (SCS), ultimately resulting in increased pulse risetime. Determining the optimal combination of diode stacks to decrease pulse risetime and increase output power requires additional SPICE circuit simulations. However, device models for SCS are not commercially available and thus require maturing SCS device models based on experimental results and physics-based simulations, such as using packages such as T-CAD, which can be time consuming.

***Sub-Problem 2 (Fundamental Physics)*:** Sub-nanosecond high-power pulse sharpening using semiconductor devices is based on ultrafast delayed avalanche breakdown under steeply increasing reverse voltage applied, thereby initiating an impact ionization front. However, the phenomenon behind the origin of free carriers that trigger the impact ionization at higher-than-breakdown fields is not completely known. Further, it is not clear whether the switching (generation of electron–hole plasma) is uniform across the device area or is localized (filamentary). Such different mechanisms are believed to be dependent on device geometry and doping concentration, and are detrimental to the switching speed. A University of New Mexico study [1] has concluded that the operation of a silicon avalanche shaper (SAS) is inconsistent with the theory described by Russian scientists. More understanding of device operation from a fundamental physics perspective is necessary to enhance their performances.

***State-of-the-Art (SOTA)*:** Prototype sub-nanosecond solid-state pulsers based on semiconductor opening switches (SOS) and semiconductor sharpeners are shown to produce peak voltages (~500 kV), and peak power outputs (~5 GW). Solid-state power supplies providing peak power up to 800 MW are available to purchase from FID Technologies, Germany. *Please refer to Table 4.7.1 of the June MSR for list of devices and their performance metrics.*

***Deficiency in the SOTA*:** Prototype ~5 GW power supplies, such as SOS based S-500 system with semiconductor sharpeners, are large (>1 m^3). Commercially available moderate-power (~1 GW) all-solid-state pulsers utilizing semiconductor sharpeners have

long purchase lead time (~4 months). Their PRF capability is limited to ~1 kHz due to physical constraints in thermal management.

***Solution Proposed*:** Downselect viable pulse compression/shaping technologies which meet or exceed the performance parameters set forth in Section 6.3's Milestones A-D towards producing an all-solid-state, tens-of-megawatts, sub-nanosecond pulse generator with semiconductor sharpener without sacrificing PRF, shot lifetime, and thermal management requirements.

***Relevance to OSPRES Grant Objective*:** The alternative all-solid-state technologies discussed could individually, or in combination, provide the means to produce order(s) of magnitude greater peak power, without severe limitation to PRF, as SWaP-centric means to increase the capability and extent of protecting naval assets.

Risks, Payoffs, and Challenges:

***Risks*:** Semiconductor closing switches, such as DBD and FID are not available to purchase within the United States. Procuring devices from abroad could lead to significant delay in experiments and development of device fabrication technology. Undergoing time-intensive and complex simulations to then down-select one technology based on peak power output alone presents risk to other secondary or tertiary performance metrics such as PRF and pulse energy, which risks developing ill-suited technologies to support the float mission. Additionally, as new technology emerges via research, scope creep to numerically and experimentally evaluate new technologies may delay transitioning these technologies into viable systems.

***Payoffs*:** The SWaP tradeoff of generating a non-laser-based system with any number of these systems can yield a higher fidelity pulsed-power waveform output. Determining which technology is viable and feasible in terms of the key performance metrics should yield a more ultracompact form factor pulse generator with order(s) of magnitude greater power density without compromise to overall size and weight to the system.

***Challenges*:** Determining the true performance metrics of interest based on these highly different devices is challenging. Without a more robust and deep understanding of their operation, and how to utilize them within a pulse generator topology, in a swappable configuration or otherwise, requires additional time and consideration. Managing the tradeoff between the academic understanding of the technologies of interest presented in the foregoing table, and the transition to prototype effort/mentality, will require both a delicate balance and leveraging the pulsed-power team's combined effort.

6.5.2 Tasks and Milestones / Timeline / Status

(A) Milestone – Downselect viable pulse compression/shaping technology to be used in addition to currently utilized DSRD, which increases at least one of the key performance metrics by an order of magnitude without compromise to the overall volume of the system [*AUG21*].

1. Task – Finalize literature study of different technologies and topologies of SCS based pulse generators and compare SWaP tradeoff evaluation to PCSS- and DSRD/SOS-based pulse generators [*JUN–JUL21* / *Ongoing*].

2. Task – Determine commercially available technologies that could be used as pulse shaper/sharpening devices to improve pulse generator performance, and select appropriate devices for further experimental verification of their performance metrics [*JUN–AUG21* / *behind schedule*].

(B) Milestone – Model and experimentally verify the performance of the downselected technology as an additional component to the DSRDs utilized within a SOS-IES pulse generator. [*NOV21*].

1. Task – Develop T-CAD device model for the selected devices (DBD/DLD) based on available device information from the literature and perform device simulations for their performance under nanosecond input pulse conditions. *[In progress]*;
2. Task – Develop SPICE device model for the selected device based on T-CAD simulation. [*SEP–OCT21*];
3. Task – Design experimental circuit with one selected diode or dynistor and obtain theoretical performance metrics using standard electronic simulation tools such as LT-Spice using the device model developed in task 2. [*SEP–NOV21*];
4. Task – Experimentally verify whether the selected device topology can produce peak power and pulse risetime equivalent to or better than that of the SOTA. [*OCT–NOV21*].

(C) Milestone – Use Semiconductor Power Technologies (SPT) developed DSRDs and Voltage Multiplier Inc. developed Axial-lead Glass-body Diodes as alternatives to delayed breakdown diodes for pulse sharpening. [*Alternative to Milestone B, OCT–NOV21]*].

1. Task – Fabricate test fixtures for connecting DSRD and VMI diodes to DSRD–IES pulse generator, as described in **Section 6.4** or MegaImpulse PP10731 pulse generator. [*OCT–NOV21*];
2. Task – Test pulse sharpening using single, 2-stack, and 3-stack SPT DSRD and/or VMI diodes using the fixtures developed in Task 1. [*OCT–NOV21*]
3. Task – Prepare a performance matrix of DSRD and VMI diodes as pulse sharpeners as a function of variations in DSRD test parameters discussed in **Section 6.3**.

(D) Milestone – Model diode/dynistor topologies and fabrication process. [*on hold until Milestones A and B are completed*].

1. Task – Model silicon diode and dynistors, with optimized device cross section (size, geometry) based on theory and simulations to increase current and thermal dissipation. [*On hold*];
2. Task – Model/design fabrication process with optimum device topology and doping concentration. [*On hold*].

6.5.3 *Progress Made Since Last Report*

Focus this month was dedicated to developing a simple theory of operation of a DSRD pulse generator, as described in Section 6.4.

6.5.4 *Summary of Significant Findings and Mission Impact*

(A) We have reviewed a number of literature reports on different approaches for pulse power generation and sub-nanosecond pulse sharpening, such as hydrogen spark-gap (HSG), solid-state pulse generators including SOS–IES based generator with semiconductor sharpener, diode-based non-linear transmission line, pulse generator based on Si and GaN photoconductive switches, and pulse generators with magnetic compression line. No single technology appears to meet or exceed the key performance metric requirements across the board. Where HSG lead in peak voltage and peak power, in comparison to the other technologies of interest, they lack in their ability to meet the required PRF, device lifetime, and SWaP-C metrics. All solid-state switching power supplies utilizing SOS and semiconductor sharpeners seem to be potentially viable technologies to compete against HSG with comparable or better SWaP-C metrics.

6.5.5 *References*

[1] E. Schamiloglu, C. B. Fleddermann, R. Focia, and J. Gaudet, “A STUDY OF ADVANCED SEMICONDUCTOR SWITCH PHYSICS AND TECHNOLOGY PHILLIPS LABORATORY Advanced Weapons and Survivability Directorate AIR FORCE MATERIEL COMMAND KIRTLAND AIR FORCE BASE, NM 87117-5776,” 1997.

7 Thermal Management

7.1 Ultra-Compact Integrated Cooling System Development

(Justin Clark, Roy Allen, and Sarvenaz Sobhansarbandi)

7.1.1 *Problem Statement, Approach, and Context*

Primary Problem: A thermal management system (TMS) is required for cooling semiconductor-based pulse-power devices, with the goal of maintaining the semiconductor device temperature below 80 °C. The proposed system must increase cooling densities, while decreasing pumping power requirements, in-line with the SWaP-C^2 objective.

Solution Space: To achieve such high cooling densities, an ultra-compact TMS (UC-TMS) directly integrated onto the semiconductor is proposed. Such a design is capable of creating turbulent flow in order to enhance the heat transfer rate. The proposed UC-TMS is restricted to 1 cm^2 surface area, therefore, the required pumping power should be kept to a minimum. An array of micro-sized jet nozzles will provide a turbulent flow onto a microchannel section directly on the semiconductor device. The UC-TMS design will reach turbulency at a faster rate while requiring less energy consumption.

Sub-Problem: The turbulency formed from the array of nozzles creates an extreme pressure loss from the large amount of jet nozzles (over 200) and a flow diameter of 100 microns. The pressure must be sustained to enable proper cooling and circulation processes.

State-of-the-Art (SOTA): Integrated chip cooling is being widely used to dramatically increase the operational power of high voltage silicon-based power devices. However, the current SOTA devices include individual parts which attach to a high-power device, causing less interaction between the semiconductor and coolant, degrading the heat removal rate.

Objective: The proposed UC-TMS design is based on refining in-chip jet-impingement geometry through leveraging theory and a parametric evaluation of nozzle geometry and flow channel arrangements. A Si-base unit will be prototyped to maneuver a higher capacity of heat removal. Moreover, to sustain the pressure, the application of different working fluids is suggested. Several types of coolant will be simulated to determine effects from fluid density and viscosity.

Anticipated Outcome(s): To create a UC-TMS with the ability to rapidly remove 1 kW/cm^2 of heat. A design capable of such high heat removal can be implemented on many applications such as high-power batteries.

Challenges: The manufacturing techniques of the semiconductor devices have not yet been adopted for integrated chip cooling systems. The proposed compact design is restricted due to low tolerance of the manufacturing process, as this process must be capable of layering the silicon TMS onto the semiconductor.

Risks: With a system so compact, the pressure drop could be a large issue regarding the objective heat dissipation rate. An extreme pressure drop would potentially cause the coolant to flow backwards, causing less fluid-to-solid interaction.

7.1.2 *Tasks and Milestones / Timeline / Status*

(A) Design a Si base 1 cm^2 UC-TMS, applying manufacturing tolerances, to achieve a heat dissipation rate of 1 kW/cm^2. The design must be able to be produced by manufacturing techniques such as etching and lithographic layering processes. To confirm the device can be manufactured as proposed, each section of the model will be layered step by step. / MAY21–AUG21 / Completed

(B) Using the optimal design, perform ANSYS simulations using either water or Si-C nanofluid. Other fluid types may be researched as pressure drop is a large factor / JUL21–DEC21 / In Progress

(C) Improve design parameters and sizing to have a lower pressure drop while having a high heat dissipation capability. Prove simulations from previous literature to show capable design configurations with acceptable pressure drop and steady temperature. / NOV21–JAN22 / In Progress

(D) With proper simulation results, manufacture a prototype to begin experimental testing and evaluation / JAN22–APR22 / Upcoming

7.1.3 *Progress Made Since Last Report*

This section is currently on hold due to staffing changes.

7.1.4 *Summary of Significant Findings and Mission Impact*

(A) From a literature review, similar designs were analyzed including a water-cooled, crossflow microchannel cooling system with various microchannel widths has been previously designed. The design achieved a simulated heat flux of 1.7 kW/cm^2 using 0.056 W of pumping power. Although this design is not the best fit when including the manufacturing constraints, the results using micro channel heat sinks are remarkable and design considerations are further analyzed. A similar design implemented the idea of having jets confined in their own individual spaces, experimentally reaching up to 900 W/ cm^2 with 0.83 W of pumping power. A third design analyzed two types of heat sinks with flat and oblique angled fins which were experimentally tested with a constant heat flux of 100 W/cm^2. The temperature difference was from 60 °C to 35 °C which proposed giving the design more power. The oblique angled fins caused 20 percent greater heat transfer than flat fins.

(B) To achieve a higher quality mesh around the nozzles and microchannels, the nozzles element size was initially set to 20 microns, or until the shape of the nozzles were more profound in a cylindrical shape. The surface which connects to the nozzles resulted with an element size of 15 microns and the nozzle sizing resulted in 13 microns. These values had to maintain an equivalent size to reduce the skewness and maintain mesh quality. Each surface with inadequate quality was selected and set to individual face sizing and is currently undergoing simulation.

To reduce the pressure loss while maintaining an effective turbulent flow produced by the jet nozzles, the microchannel fin designs did not effectively enhance the rate of heat transfer. The combination of micro channels and jet impingement caused too high of a pressure loss, causing the fluid to reverse its flow; therefore further enhancement of the UC-TMS will be based explicitly on jet impingement theory.

8 Pulse-Forming Networks

8.1 Diode-Based Nonlinear Transmission Lines

(Nicholas Gardner)

8.1.1 *Problem Statement, Approach, and Context*

Primary Problem: The size, weight, and cost of pulse forming/shaping networks (PFNs) need to be reduced and optimized for Navy afloat missions.

Solution Space: Develop a diode-based nonlinear transmission line (D-NLTL) as a pulse shaping network for the conversion of energy to the ultra-high frequency (UHF) band (0.3–3 GHz) at single MW peak power.

Sub-Problem: Metrics used for component selection are designed for D-NLTLs operating at sub 0.1 GHz frequencies. Using such metrics alone to design D-NLTLs capable of single GHz frequency generation introduces a trial by error nature to the design process wherein frequency/power generation predictions and measurements can differ by a few hundred MHz or the design potentially fails to operate at all.

State-of-the-Art (SOTA): D-NLTL prototypes have been shown to generate center frequencies of 0.2–0.5 GHz at kV amplitudes in a light-weight small-footprint circuit. Simulations of LE-NLTLs indicate achievable frequencies in the single GHz range.

Deficiency in the SOTA: Simulation/measurement agreement becomes increasingly sensitive to parameters and factors outside of inductive and capacitive element choice alone at frequencies above ~100 MHz. Disparities between measurement and simulation above contribute to a trial by error design process for D-NLTL networks.

Solution Proposed: Identify and characterize diode parameters affecting frequency generation in the context of a NLTL application via simulation and experiment, and identify limits/desired ranges required for UHF generation. Such parameters include, but are not limited to: diode frequency response, diode reverse bias hold-off voltage, diode small signal capacitance, diode chip/package parasitics, and diode relaxation time. The improved understanding of the explored parameters will be used to design and fabricate a D-NLTL capable of GHz center frequency generation at single MW peak powers.

Relevance to OSPRES Grant Objective: The SWaP-C^2 capabilities of D-NLTLs (shown in Figure 8.1.1) represent a potential solution to the size, weight, and cost optimization issue for PFNs on Navy afloat missions.

Figure 8.1.1. 20 cell D-NLTL of dimensions 1.1 x 23.45 cm constructed with commercial off the shelf components.

Risks, Payoffs, and Challenges: There exists a potential tradeoff between power and frequency generation. Devices such as ceramic capacitors may be used in a D-NLTL to generate high peak power due to their break down potentials in the 10s of kV, however,

such devices become highly resistive at 0.1–0.2 GHz frequencies. Diodes have been shown to be operational at frequencies upwards of 0.4 GHz, however, possess low hold-off potentials limiting peak output power. The payoff to overcoming these challenges is significant reductions in PFN size and cost.

8.1.2 *Tasks and Milestones / Timeline / Status*

(A) Milestone – Construct/demonstrate a prototype capable of UHF generation at low voltages (1–100 V excitation amplitude)

(A1) Break a low-voltage pulse into a sequence of solitons (SEP20)

(A2) Increase frequency generation past 200 MHz (NOV20)

(A3) Select diode candidate (junction capacitance <50 pF) and simulate expected results (Ongoing)

(A4) Design/fabricate/test line (Ongoing)

(A5) Write/Submit manuscript on D-NLTL design processes (Ongoing/In Revision)

(B) Milestone – Demonstrate tuning of waveform at low voltages using electrical or mechanical means (Completed with voltage biasing APR21)

(B1) Write/Submit manuscript on LV D-NLTL tuning circuit (Ongoing/In Revision)

(B2) Simulate a HV tunable D-NLTL topology using the K series epoxy diodes (**Completed DEC21**)

(B3) Design a PCB prototype HV Tunable D-NLTL

(B4) Demonstrate electrical tuning on a HV D-NLTL

(C) Milestone – Construct/demonstrate a prototype capable of frequency generation above 1 GHz at single MW peak powers (Completed MW peak power but not GHz center frequency – Ongoing)

(C1) Identify diode candidates with a hold-off voltage of several kV and a low signal junction capacitance under 100 pF (Completed JAN21)

(C2) Design/fabricate single diode prototypes (Completed JAN21)

(C3) Perform initial tests using half-barrel pulse source (Completed FEB21)

(C4) Refine simulation using measurements (Completed FEB21)

(C5) Test a prototype using two diodes in series (Completed FEB–MAR21)

(C6) Test lines using Mega Impulse source (Completed MAY21**)**

(C7) Test K50F D-NLTL using PCSS as a source (Completed JUN21)

(C8) Use simulations and tests to refine line for increased frequency generation (Completed JULY21)

(C9) Rebuild lines for negative polarity pulses (Completed JULY21)

(C10) Test lines using PCSS as a source with various cell inductances (Completed JULY**)**

(C11) Test lines using Marx Generator as a source (Completed AUG21)

(C12) Reconstruct PCSS strip line to produce a pulse similar to 5.1.2 (left) and retest (Ongoing AUG21)

(C13) Write/Submit manuscript on the GHz MW D-NLTL Prototype (Ongoing/In Revision)

(D) Milestone – Demonstrate power scalability using an array of D-NLTLs (On Hold – Prioritizing Milestone C)

(D1) Design a prototype capable of running two D-NLTLs simultaneously off of the same excitation pulse (Completed JUN21)

(D2) Demonstrate simultaneous operation of parallel D-NLTLs

(D3) Build a circuit capable of measuring the CV curve of low-voltage diodes and measure the CV curves of unused diodes and heavily used diodes (Completed JUN21)

(D4) Measure SMV1702 diode C(V) curve and compare against manufacturer specs

(D5) Measure C(V) curves for a sample of SMV1702 diodes for determination of degree of variability between diodes

8.1.3 *Progress Made Since Last Report*

(B) A voltage tunable topology of D-NLTL based on a HV epoxy diode of model K100F was simulated in LTspice to determine feasibility and expected voltage biases and results. Resulting simulation measurements indicate the center frequency can be tuned up by upwards of 50% of its un-biased center frequency using a voltage range of 0 to 200 V. Negative polarity DC biases demonstrated little effect on center frequency

8.1.4 *Technical Results*

(B) A 20-cell high voltage D-NLTL topology based on the K100F epoxy diode with the ability to voltage bias the diodes was simulated in LTspice. Figure 8.1.2 displays the first few cells of the schematic. The D-NLTL is designed for negative polarity pulses and in each case is excited with a square pulse of amplitude 4 kV, rise time of 1 ns, fall time of 1 ns, and pulse width of 5 ns. The DC bias was altered in 25 V increments from –200 V to +200 V applied to the cathode of each diode. Results are displayed in Figure 8.1.3a with waveform examples in Figure 8.1.3b. Results show a positive polarity DC bias increasing center frequency from ~1.1 GHz to ~1.5 GHz over a voltage range of 0 to 200 V while a negative polarity DC bias had little effect on the center frequency. With the D-NLTL set up to receive negative polarity pulses, the greater observed effect from a positive polarity DC bias indicates electrical tuning increasing center frequency by tuning D-NLTL average impedance. Increasing positive DC bias on the cathode of a diode would increase diode depletion zone and with it average capacitance. Increasing the average capacitance decreases average impedance from an unbiased value of 70 Ω allowing for

an improved source-line impedance match with a 50 Ω source or connector. Next steps are aimed at determining the best method for connecting a DC bias to the D-NLTL. Challenges to prototype fabrication are primarily aimed at determining the safest way of connecting a 100–200 V DC bias as the line is receiving a pulse with an amplitude of several kV.

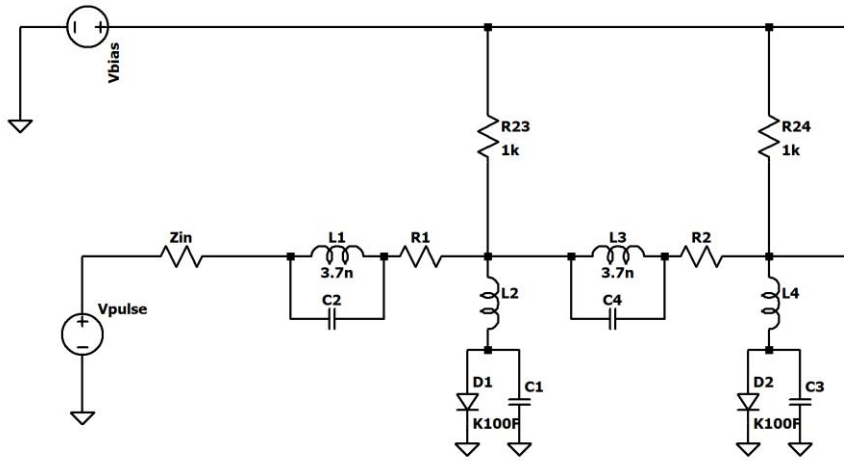


Figure 8.1.2. The first 2 cells of a 20 cell electrically tunable HV D-NLTL based on the K100F epoxy diode.

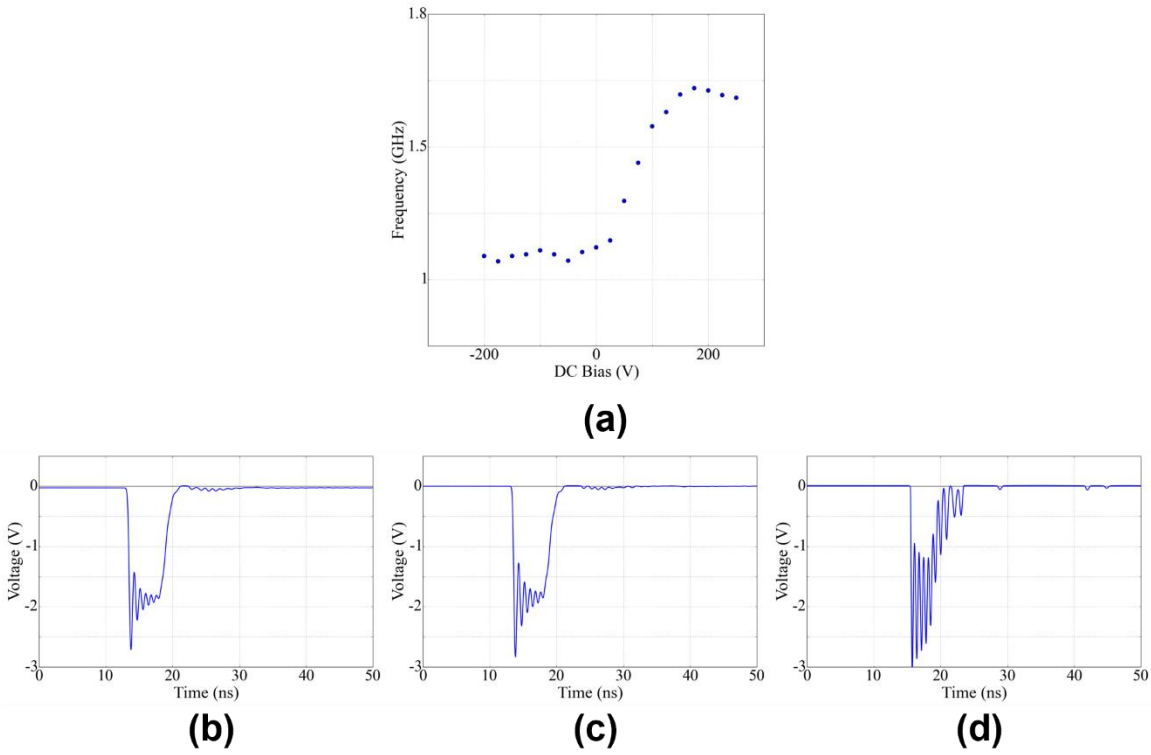


Figure 8.1.3. (a) Center frequency measurements as a function of DC bias. (b) Waveform results for a –100 V DC bias, (c) waveform results for a 0 V DC bias, (d) waveform results for a 100 V DC bias.

8.1.5 *Summary of Significant Findings and Mission Impact*

(A) After a failure of the high-voltage diode-based nonlinear transmission lines (D-NLTLs) to reproduce simulated results, work refocused on low-voltage D-NLTLs to determine the source of the discrepancy. In NOV2020 a center frequency of ~250 MHz was achieved using a D-NLTL design based on the diode model SMV1702.

(B) Following the success of the SMV1702 D-NLTL, a circuit was designed, capable of electrically tuning the center frequency utilizing DC biasing of the diodes. In FEB–APR2021 the circuit demonstrated a linear relationship between DC bias up to a limiting potential. Negative DC biases decreased center frequency while positive DC biases increased center frequency. A HV voltage tunable topology was simulated in the month of December indicating the center frequency can be altered by up to 50% of the unbiased center frequency with a voltage bias under 200 V.

(C) In JAN2021 two diode candidates (models K100F and K50F) were identified for a HV D-NLTL design. FEB2021 saw successful tests of both D-NLTLs with each sharpening the rise time of a pulse produced by a DSRD based source down from ~1 ns to ~600 ps. In AUG2021 the first major variation between the K50F and K100 F D-NLTLs was observed with the K50F line breaking the pulse into solitons while the K100F line primarily sharpened the rising edge of the pulse. In SEPT2021 comparisons between measured and simulated results for Marx+K50F measurements indicate further success in modeling inductor and diode parasitics to predict frequency generation.

(D) During MAY2021 a line topology capable of feeding two identical D-NLTLs with the same pulsed source at the same time was fabricated. Initial results were collected, and a prototype is currently being designed to test the ability to parallelize D-NLTLs.

8.2 Continuous Wave Diode-NLTL based Comb Generator

(Nicholas Gardner and John Bhamidipati)

8.2.1 *Problem Statement, Approach, and Context*

Primary Problem: When used as a pulse shaping network (PSN), diode-based nonlinear transmission lines are promising solutions towards reducing the size, weight, and cost of RF and microwave sources on Navy afloat missions. However, D-NLTLs have a dynamic impedance, leading to signal/power reflection, standing wave generation, and return power losses at both the source–line and line–load interfaces, leading to difficulties in practical D-NLTL applications.

Sub-Problem: Design parameters for COTS high-frequency D-NLTL based comb generators capable of generating up to ~50 GHz output frequencies are limited to <1 Watt output powers, which is <0.1% of the power handling capability required for navy afloat missions. Using such metrics alone to design D-NLTLs capable of generating ~1–2 GHz frequency with capability to handle MW-order peak powers could potentially introduce design errors resulting in frequency/power prediction–measurement discrepancies on the order of a few hundred MHz.

Solution Space: Use a D-NLTL as a pulse shaping network (PSN) to convert continuous wave (CW) signals from low frequency–very high frequency (LF–VHF) bands (0.03 MHz–30 MHz) to the ultra-high frequency (UHF) band (0.3–3 GHz) at ones-of-MW peak power. Such an application will reduce impedance mismatch effects at the source–line interface by continuously oscillating D-NLTL impedance between the same two values. Use of MW D-NLTLs in the comb generator will push output frequency up to ranges required for Navy afloat missions.

State-of-the-Art (SOTA): Commercial-off-the-shelf (COTS) GaAs varactor diode-based monolithic microwave integrated circuit (MMIC) D-NLTL comb generators are capable of operating at input and output frequencies up to 600 MHz and 30 GHz, respectively. However, these comb generators are not capable of handling powers higher than 27 dBm (0.51 W). In-house pulsed D-NLTL prototypes have been shown to generate center frequencies of 0.2–0.5 GHz at kV amplitudes in a light-weight small-footprint circuit. Further D-NLTL network efficiency is hindered by a signal depended impedance characteristic to the network leaving reported efficiencies of RF content generation at 10% or less of incident pulse energy.

Objective 1: Design and demonstrate a high voltage D-NLTL based comb generator capable of L-Band Frequency generation and 0.1–5 MW power generation.

Objective 2: Increase D-NLTL network efficiency above the reported 10% threshold through use of CW sources suppressing impedance mismatch effects presented by the signal dependent impedance characteristic to D-NLTLs.

Anticipated Outcome(s): A successful demonstration of improvements to impedance matching at the source–line interface using a CW signal measured as a reduction in signal amplitude loss between the source and D-NLTL.

Challenges: Nonlinear signal-dependent behavior provided by a reverse bias diode produces difficulties in predicting generated waveform behavior. Further D-NLTL performance is limited in both frequency and power generation by the availability and variety of COTS Schottky and epoxy diodes.

Risks: The reverse bias hold off potential (V_R) of a chosen diode limits the power generation capabilities of the system. If an excitation is used that exceeds V_R, diodes risk being damaged. Further reflections produced at the source–line interface caused by a signal dependent impedance can damage a CW source sensitive to such reflections.

8.2.2 *Tasks and Milestones / Timeline / Status*

(A) Demonstrate an ability of a CW excitation signal to reduce the source–line impedance mismatch effect on signal amplitude present in D-NLTLs when compared to a pulsed excitation signal, first through simulations and then by validating the results experimentally using low voltage (LV) and high voltage (HV) prototypes.

(A1) Show the potential to improve source–line impedance mismatch in simulation (Completed SEP21)

(A2) Experimentally demonstrate a low voltage (LV) prototype receiving a CW input (Completed SEP21)

(A3) Compare measured results with simulation behavior, comparison of results will be used to further refine D-NLTL simulation techniques (Ongoing)

(A4) Determine if there are improvements to system behavior if D-NLTL diodes are biased when receiving a CW input (Ongoing)

(A5) Demonstrate improvements to the source–line impedance mismatch in a LV prototype (Ongoing)

(A6) Demonstrate a HV prototype receiving a CW input (Completed NOV21)

(B) Demonstrate UHF – L-band (0.3–2 GHz frequency) generation with a CW D-NLTL.

(B1) Excitation of K100F and K50F D-NLTLs using a 700 MHz signal from the R&S amplifier (Completed NOV21)

(B2) Compare measurement with simulation to further refine simulation measurements. (**Ongoing**)

(B3) Simulate topologies capable of utilizing a bipolar pulse for CW applications. (**Ongoing**)

(C) Demonstrate UHF generation at single MW power levels with a CW D-NLTL.

8.2.3 *Progress Made Since Last Report*

(B2) Simulations were performed on 20 cell lossy D-NLTL topologies based on the K100F and K50F epoxy diodes to compare against physical measurements performed with the R&S amplifier from the November report. Results are discussed in section 8.2.4 and shown for both lines in Figure 8.2.1a. Simulated results showed little agreement with the measured results, which is a notable break from LV simulations which used similar simulation topologies.

(B3) A D-NLTL topology based on the SMV diode, shown in Figure 8.2.2a, was simulated with the aim of better using the bipolar nature of a CW signal. The line topology used two D-NLTLs in parallel with the diode anodes connected to ground in one line and diode cathodes connected to ground in the other. Both lines are excited by the same source and terminated at the same load. The topology did demonstrate an ability to use both the positive polarity and negative polarity portions of the signal but at a cost to pulse amplitude when compared to a single line receiving the same signal.

8.2.4 *Technical Results*

(B2) LTspice was used to simulate two 20 cell D-NLTL topologies based on the K50F and K100F diodes. Each line was excited with a 700 MHz 100 V sine wave aimed at giving a similar excitation to the R&S amplifier measurements from November, which had a frequency of 700 MHz and amplitude of 100–120 W. Results shown in Figure 8.2.1a–b indicate work needs to be done in terms of simulation refinement. For comparison, R&S amplifier results are shown in Figure 8.2.1c–d. While measured amplitudes are in a similar range (–5 V to 5 V for simulation, –4 V to 4V for R&S measurements). The simulated line produced a frequency of 500 MHz, differing from the frequency doubling observed in the R&S measurements. HV simulated results represent a notable break from LV

measurements where similar waveforms were observed in both simulation and measurement. Further simulation efforts will focus on finding the source of the disagreement.

(B3) A twin D-NLTL topology based on the SMV1702 Schottky diode was simulated with the goal of improving bipolar signal usage by a D-NLTL. Both lines were excited by the same source and terminated across the same load in parallel. Line topology is shown in Figure 8.2.2a where one line has the anodes of the diodes connected to ground and the other has the cathodes of the diodes connected to ground. The simulated signal was a 100 MHz 40 V sine wave. Measurements are shown in Figure 8.2.2b with a comparison to a single monopolar SMV1702 line shown in Figure 8.2.2c. Results demonstrate an ability to use both positive and negative polarity portions of the CW signal, however at a large cost to amplitude when compared to the single line results. The amplitude reductions could be explained through variations in each line. Ideally one line would modify the positive polarity portion of the signal while the other modifies the negative polarity portion of the signal and both would be recombined over the load. However, due to the amplitude-dependent nature of signal propagation in D-NLTLs, small variations in signal propagation such as reflections or variance in diode or inductor model can lead to enough signal variation in each line to cause substantial destructive interference when the signals are combined. More work needs to be done to determine a feasible way to utilize a bipolar CW signal. Avenues to follow in this regard could be reverse diodes in a single line (i.e., connecting anode to anode or cathode to cathode in a single cell), or use of a diode model with both a positive and negative polarity portion of its CV curve.

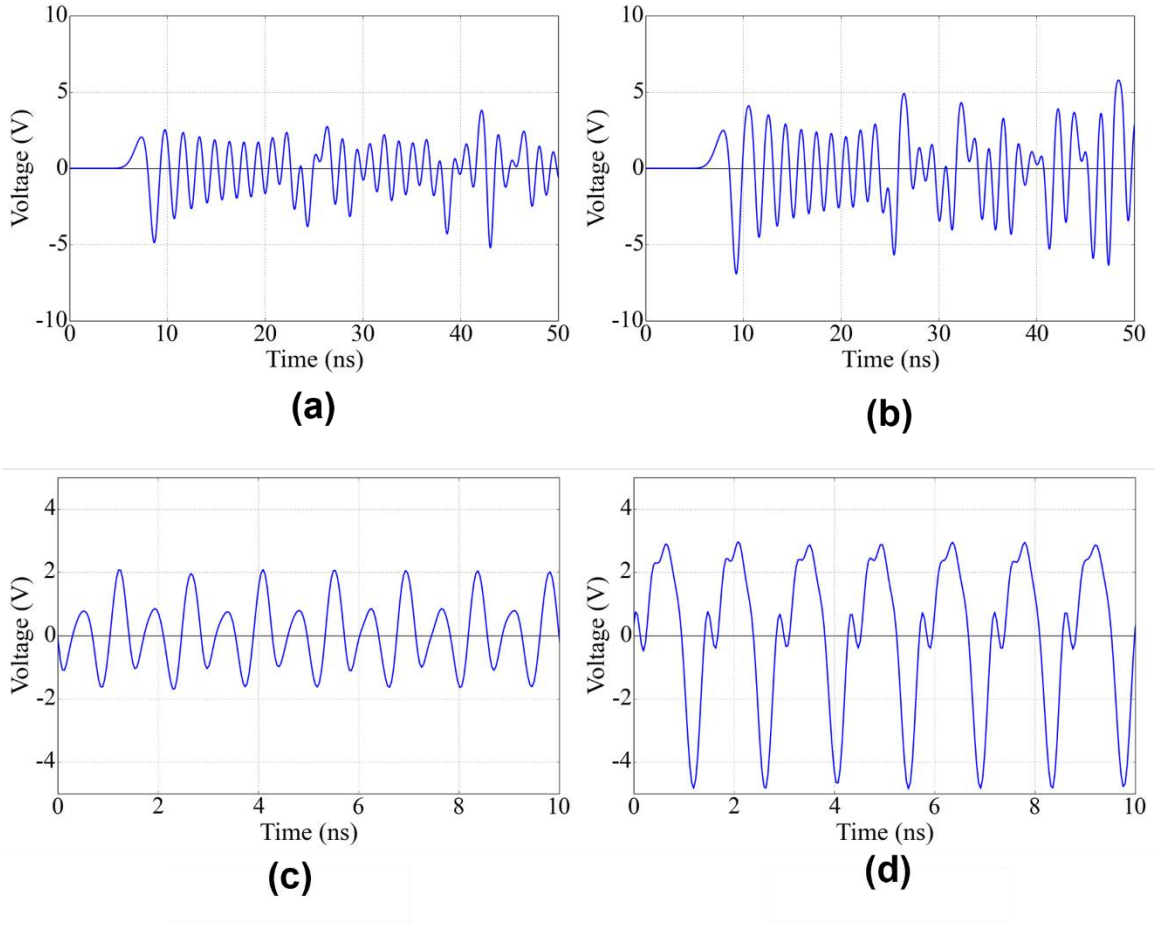


Figure 8.2.1. (a) K50F simulated results, (b) K100F simulated results, (c) K50F measured results, (d) K100F measured results. Simulated results use a 700 MHz 100 V sine wave in LTspice. Measured results use a 700 MHz sine wave amplified to ~100 W.

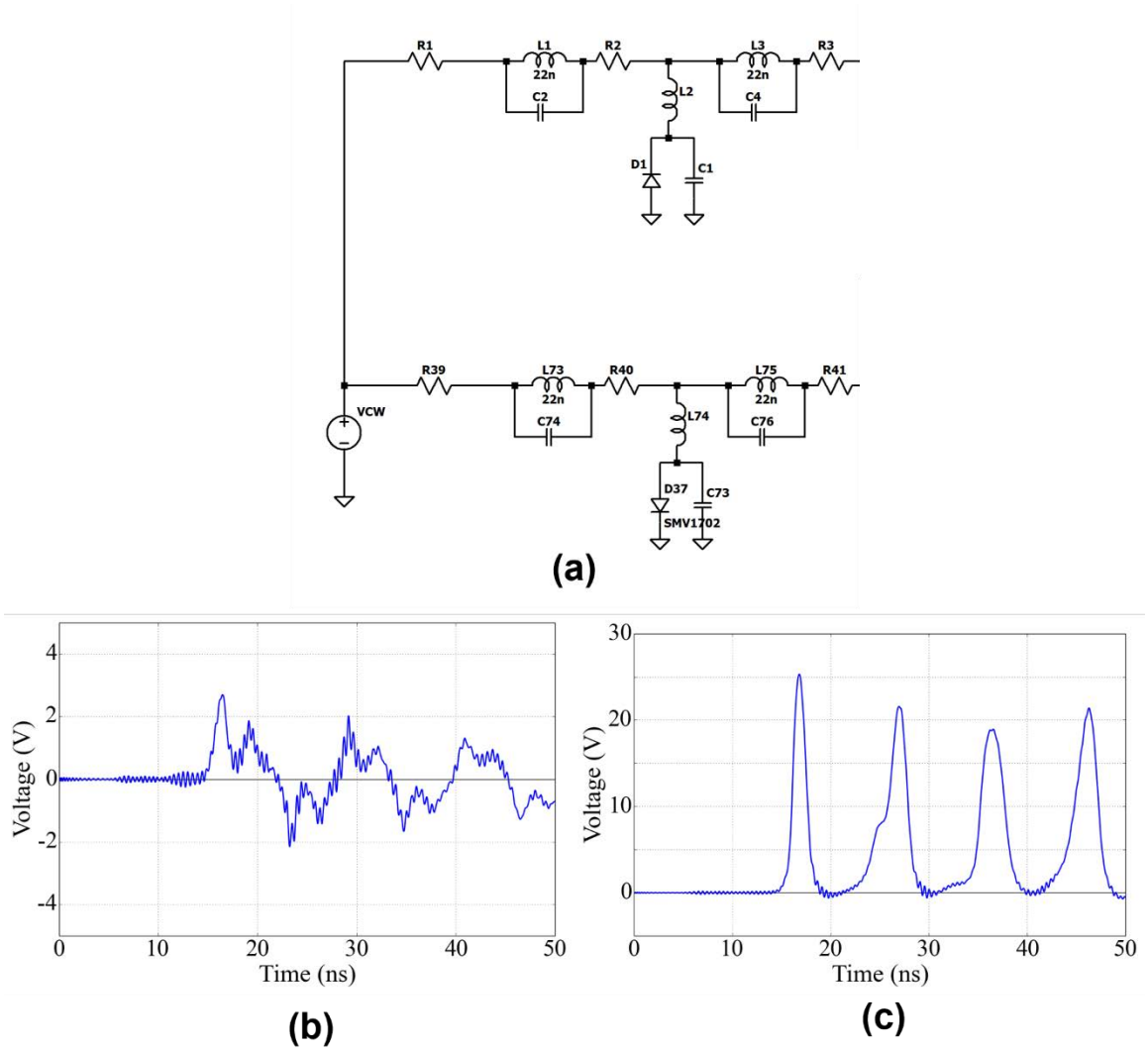


Figure 8.2.2. (a) Dual D-NLTL schematic in LTspice. (b) Transient results measured across a 50 Ω resistive load for the dual lines. (c) Transient results measured across a 50 Ω resistive load for a single D-NLTL. Each D-NLTL topology uses a 100 MHz 40 V sine wave.

8.2.5 *Summary of Significant Findings and Mission Impact*

(A) In the month of September, a LV prototype was given several continuous waveforms to observe initial behavior of a D-NLTL with a CW source. The LV D-NLTL demonstrated a capability to receive a CW based source. No effect on the source–line impedance mismatch was observed for the LV tests. During the month of November two high voltage D-NLTLs based on epoxy diodes were tested using a sinusoidal waveform amplified by an R&S amplifier. Each D-NLTL demonstrated a capability to function with a CW source, however little to no effect was observed on the source–line impedance mismatch.

(B) Two high voltage D-NLTLs based on epoxy diodes of model K50F and K100F were tested using a 700 MHz sinusoidal signal amplified by an R&S Amplifier. Both D-NLTLs demonstrated frequency doubling behavior, producing a 1.4 GHz frequency

in the generated waveform. In December 2021 simulations were performed for the purposes of comparison with R&S amplifier measurements as well as simulations on novel line topologies for the purposes of better utilizing both negative and positive polarity portions of a CW pulse.

8.3 Pulse-Compression-Based Signal Amplification

(Feyza Berber Halmen)

8.3.1 *Problem Statement, Approach, and Context*

Primary Problem: Sources such as gallium-nitride-based high electron mobility transistors (GaN HEMT) can be used as high power microwave (HPM) to achieve the SWAP-C2 performance metrics necessary to support the cUAV Naval afloat mission. Even the best high-power GaN HEMTs are limited to 2–3 kW of peak power. Achieving the necessary effective radiated power (ERP) out of a high gain (≥ 10-dBi) narrow-band antenna requires input power increase of two to three orders of magnitude. Power combination methods to achieve an ERP at MW scale require 10s to 100s of GaN HEMTs, compromising the SWAP-C2 performance.

Solution Space: Pulse compression techniques are used to increase the peak power and lessen the pulse width in HPM applications. Adapting pulse compression at the GaN HEMT or any other SWAP-C2 compatible source output can achieve sufficient ERP with an optimal radiating element.

Sub-Problem**:** Pulse compression is generally used to generate a pulsed output with a high peak output power (P_{out_peak}) and a wideband frequency content from a DC input voltage. The main challenge lies in identifying a pulse compression technique that can be used to amplify a narrowband RF input signal. Some of the circuit elements for common pulse compression techniques, such as the saturable inductors used for energy storage in magnetic pulse compression (MPC), exhibit increasingly lossy behavior with high frequency. Another challenge will be to determine, if any, the operating frequency limits of the suitable pulse compression technique for high-frequency, high-power signals.

State-of-the-Art (SOTA): Large magnetic pulse compression circuits (>1-m^3, >1000-lbs) have demonstrated peak output power up to a few GWs. Smaller versions (~0.125-m^3, 50-lbs to 100-lbs) can achieve 50 kV peak voltage [1].

Deficiency in the SOTA: Traditional MPC sytems are large (few meters long), leverage huge transformers, and require liquid coolant such as transformer oil, which leads to undesirable system mass values of ≥1000 lbs. They are used for generating medium or high pulse power traditionally from dc or ac (50/60Hz) high voltage supply. There is no known example of high frequency signal amplification utilizing MPC.

Solution Proposed: Developing a pulse compression circuit that will act as a high-power signal amplifier with a gain of ≥10. Utilizing magnetic pulse compression, or any other suitable pulse compression method, for high power signal amplification with source fidelity.

Relevance to OSPRES Grant Objective: Pulse compression will enable size and cost efficient solution to high power signal amplification which will lead to HPM source

development with optimal SWaP-C2 parameters. Achieving a pulse compression method with 2–3 orders of signal amplification will result in significant reduction in size and cost of HPM source.

Risks, Payoffs, and Challenges:

Challenges: Modeling pulse compression circuits for high-frequency operation can present a challenge. Pulse compression circuits are generally evaluated in SPICE simulators with low frequency ac / transient simulations. SPICE is a lumped-element model simulator and cannot solve for the distributed-element model required at high frequencies where the wavelengths become comparable to the physical dimensions of the circuit. Some circuit components, such as the saturable inductor in the MPC, are not available in SPICE or many other simulators and need to be modeled using behavioral models and proprietary material data. Pulse compression circuit modeling, especially at high frequencies, needs to be investigated.

Risks: Pulse compression methods are usually lossy in nature and generate considerable amount of heat, therefore, designing a proper cooling method must be carried out which may inadvertently increase the volume (size and weight) of the overall design.

8.3.2 *Tasks and Milestones / Timeline / Status*

(A) Milestone – Achieve 2–3 times increase in peak power and compression gain using magnetic pulse compression (MPC) [*estimated completion by JAN22*].

1. Subtask – Model saturable inductors in LTSpice or Matlab/Simulink in order to be able to develop MPC simulations / NOV21 / Ongoing.
2. Subtask – Design of MPC circuit with RF input and simulation in LTSpice or Matlab/Simulink to evaluate the resulting amplification and frequency content. / [On hold until the saturable inductor simulation model is realized].
3. Subtask – Model the high frequency behavior of MPC circuit / NOV21 / Ongoing.
4. Subtask – Build and test the MPC prototype using bench top power supply / OCT–*DEC21 / Ongoing*.

(B) Milestone – Increase the compression gain available from MPC.

(C) Milestone – Build and test high-frequency MPC prototype.

8.3.3 *Progress Made Since Last Report*

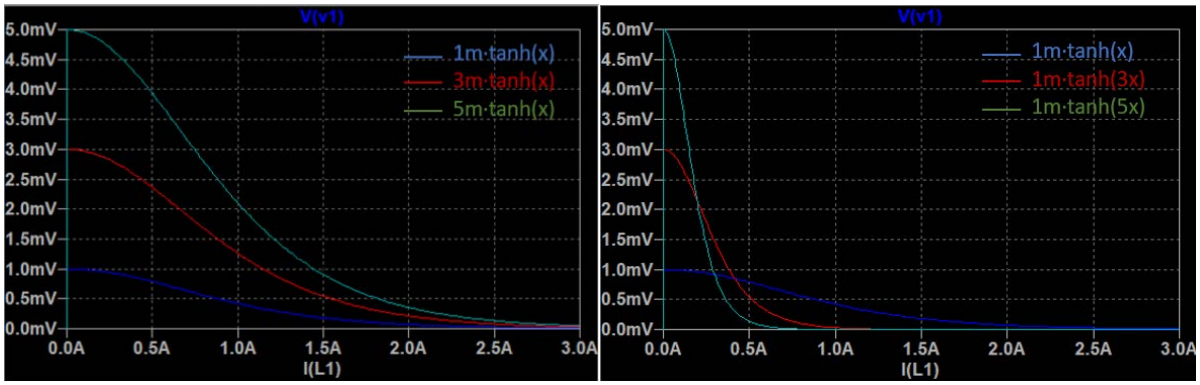
(A.1) Saturable inductor modeling methods in LTSpice were investigated. Initial modeling is realized using random B-H curve values. Matlab simulation capabilities for saturable inductors were investigated, and purchase of related Simulink add-on was initiated.

(A.3) High frequency losses for different magnetic core materials are still being investigated.

(A.4) Rogowski current probes for MPC testing are being investigated.

8.3.4 *Technical Results*

(A.1) Saturable inductor modeling is possible both in LTSpice and Matlab Simscape using magnetic core behavioral models. One method of simulating saturable inductors with LTspice is to include the inductor flux expression as the component parameter. If the flux expression is not known, it can be approximated with hyperbolic tangent or arc tangent functions which pass through the origin and settle to ±1 or ±π/2, respectively. Arc tangent function is a slower function and can be used for softer saturation characteristics. For an inductor with flux A*tanh(B*x), where x is the LTSpice parameter for inductor current, the saturation characteristics can also be altered through coefficients A and B as depicted in Figure 1. LTSpice simulations are set to yield dI/dt=1 and, therefore, the voltage over the inductor indicates the inductance. Figures 8.3.1 (a) and (b) show the maximum inductance value for I=0 and decreasing inductance as current increases and saturation is approached. This is a simple method to simulate the effects of inductance change with saturation and can be used for initial simulations for MPC. However, this model does not include hysteresis behavior of magnetic cores.



(a) (b)

Figure 8.3.1. Change in saturation characteristics with coefficients (a) A and (b) B for LTSpice saturable inductor modeled with Flux=A*tanh(B*x).

A more realistic approach to simulating magnetic cores with hysteresis in LTSpice utilizes the Chan model [3]. The inductor is modeled using the geometric parameters for the magnetic core and the number of windings, as well as some magnetic core parameters that are used according to the Chan Model to calculate the B-H curves. The magnetic core parameters required are the coercive force Hc, remnant flux density, Br, and the B-axis intersection of the asymptotic line for saturation flux density, Bs. These three parameters are used to calculate the upper and lower branches of the major hysteresis loop, the initial magnetization curve, and the minor hysteresis loops. Figure 8.3.2 shows voltage vs. current waveforms for a single winding magnetic core simulated with the Chan model. Voltage axis also depicts the inductance as dI/dt=1 for the transient simulation. Figure 8.3.2(a) shows the maximum inductance decreasing in value and occurring at higher currents as Hc increases. Hysteresis slope change with increasing saturating flux but same coercivity is observed as decrease in peak inductance and slower saturation in

Figure 8.3.2(b). These plots suggest the accurate modeling of the upper branch of major hysteresis loop with the Chan model.

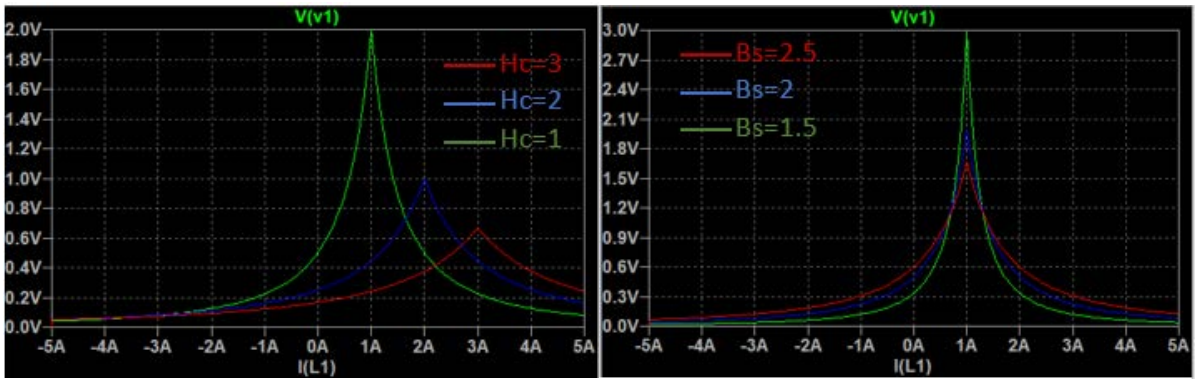


Figure 8.3.2. Change in saturation characteristics with (a) Hc and (b) Bs for single winding magnetic core modeled with the Chan model in LTSpice

Further simulations are required to verify the accuracy of the LTSpice magnetic core simulations. Efforts will next be focused on B-H curve simulation of the magnetic cores and comparing the simulated B-H curves with vendor provided data. LTSpice simulation metrics and their effects on the non-linear element analysis also need to be better studied.

8.3.5 *Summary of Significant Findings and Mission Impact*

(A) Initial saturable magnetic core modeling is done in LTSpice with two different methods available. This is the first step at saturable inductor simulations essential to MPC design.

8.3.6 *References*

[1] D. Zhang, Y. Zhou, J. Wang and P. Yan, "A compact, high repetition-rate, nanosecond pulse generator based on magnetic pulse compression system," in IEEE Transactions on Dielectrics and Electrical Insulation, vol. 18, no. 4, pp. 1151-1157, August 2011, doi: 10.1109/TDEI.2011.5976109.

[2] J J. H. Chan, A. Vladimirescu, X.-C. Gao, P. Liebmann and J. Valainis, "Nonlinear transformer model for circuit simulation," in *IEEE Transactions on Computer-Aided Design,* vol. 10, no. 4, pp. 476-482, 1991

9 Antenna Development

9.1 Tradespace Analysis of an Array of Electrically Small Antennas (ESAs)

(Bidisha Barman and Deb Chatterjee)

9.1.1 *Problem Statement, Approach, and Context*

Primary Problem: Determine the extent to which the physical aperture size of an antenna array, composed of patch elements, can be reduced, while maintaining performance in peak power density, bandwidth, and electronic beam steerability over the UHF range (0.4–1 GHz), compared with present-art high-power-microwave-capable antenna arrays.

Solution Space: An array of patch antenna elements whose feed, two-dimensional shape, and relative placement (i.e., intra-, and inter-element design) allow for the physical aperture size to be reduced by more than 20% compared with the present-art.

Sub-Problem: To overcome scan blindness (as the main beam is electronically steered), due to the excitation of surface waves (SW). (Note: scan blindness is a common phenomenon in electrically small microstrip patch antenna arrays).

State-of-the-Art (SOTA): Horn, reflector, Vivaldi, valentine, etc. are some of the commonly used ultra-wideband (UWB) antenna elements in a phased array for high-power microwave (HPM) transmissions.

Deficiency in SOTA: Large physical aperture size of the antennas.

Solution Proposed: Using electrically small antennas (ESAs) as array elements and optimizing their performance in terms of both near-field (bandwidth) and far-field (directivity) parameters, followed by arrangement of the ESAs in suitable lattice structures (preferably, hexagonal/triangular) to reduce the overall array aperture area. Using stochastic and machine learning (ML) algorithms to optimize antenna element and array performance.

Relevance to OSPRES Grant Objective: Provides design and optimization guidelines for UWB ESA elements, especially coaxial probe-fed microstrip patch antennas, and arrays for HPM applications.

9.1.2 *Tasks and Milestones / Timeline / Status*

(A) Develop an Array Pattern Tool in the context of lightweight calculations of large antenna arrays / JAN–MAY 2021 / Completed code.

(B) Investigate the effects of array aperture area reduction on different array parameters (such as gain, beamwidth, electronic beam steerability) and present a comparative study of antenna array parameters as a function of array aperture area / JAN–MAY 2021 / Completed investigations of arrays on infinite ground planes.

(C) Build minimum viable validation prototypes of single ESA elements on substrates that have good power handling capabilities for HPM transmissions at UHF range (such as polyethylene, FR-4, TMM-10i, TMM-6) / JAN 2021–MAR 2022 / Time-domain simulations of ESA elements performed.

(D) Optimization of ESA (single element) performance using ML based stochastic search algorithms / JUN 2021–JAN 2022 / Ongoing ML-based multi-objective-optimization (MOO) of ESA elements.

(E) Build minimum viable validation prototypes for arrays of ESA elements/ JUN 2021–MAY 2022/ Repeated gain measurement of the previously manufactured 2x2 array antenna prototype.

(F) Optimization of array performance using ML algorithms / SEP 2021–MAY 2022 / Ongoing ML-based MOO of antenna array parameters.

9.1.3 *Progress Made Since Last Report*

(C) Build minimum viable validation prototypes of single ESA elements:

a. Performed time-domain analysis of a previously designed UWB, polyethylene substrate based, microstrip patch, ESA element, in the UHF range (0.7–1.05 GHz), subjected to various input pulses, using CST microwave studio.

(D) Multi-objective-optimization of single ESA elements using ML algorithms:

a. Initiated ML-based multi-objective optimization of single ESA elements, via Altair HyperStudy, for simultaneous maximization of gain and bandwidth.

(E) Build minimum viable validation prototypes for arrays of ESA elements:

a. Earlier it was reported that the experimental gain data of the manufactured 2×2 array of microstrip patch ESA elements did not agree with the simulated results.

b. The gain was re-tested with different set of cables, but with the same experimental setup, and an improved agreement with the simulated data has been achieved.

(F) Optimization of array performance using ML algorithms:

a. Initiated optimization of a 5×5 array by seeking the best array design parameters, including inter-element spacing, ground plane size, feed-probe locations, etc., with the objective of mutual coupling reduction between individual array elements.

9.1.4 *Technical Results*

(C) Build minimum viable validation prototypes of single ESA elements:

To perform time-domain analysis, a previously designed UWB ESA element on a 1.25-inch-thick polyethylene substrate (shown in Figure 9.1.1), in the UHF range (0.7–1.05 GHz), was subjected to different input pulses. Two different high-voltage monopolar input pulses, namely DSRD 2×2 and PPM0731, have been considered to study the response 10 m away from the antenna. The input pulses are shown in Figure 9.1.2, and the corresponding time- and frequency-domain E-fields, from the ESA element, are shown in Figures 9.1.3 and 10.1.4, respectively. It is to be noted that the input pulses used here were either taken from measurements or from the manufacturer's datasheet.

The rE/V values of the antenna at 10 m are calculated and listed in Table 9.1.1. The results show that the PPM0731 is more suitable for transmission, using the antenna

element, compared to the DSRD 2×2 input pulse. Future work involves improving the rE/V values of the antenna, subjected to various short input pulses.

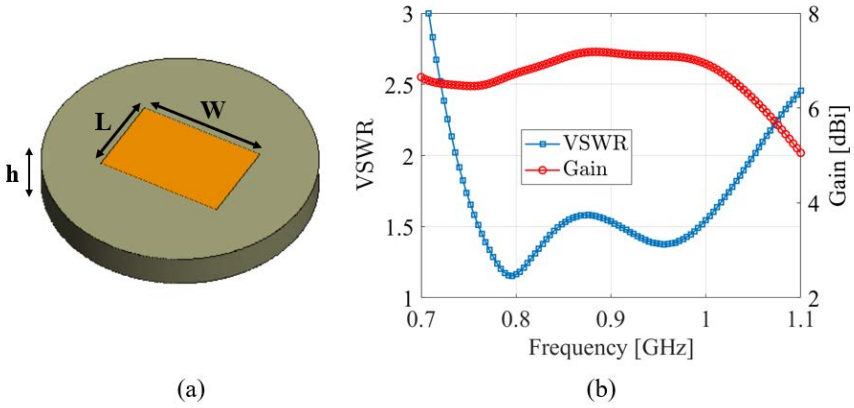


Figure 9.1.1. (a) FEKO simulation model of the microstrip patch antenna designed on polyethylene substrate (L = 80.54 mm, W = 120.81 mm, h = 31.75 mm), and (b) simulated VSWR and gain response.

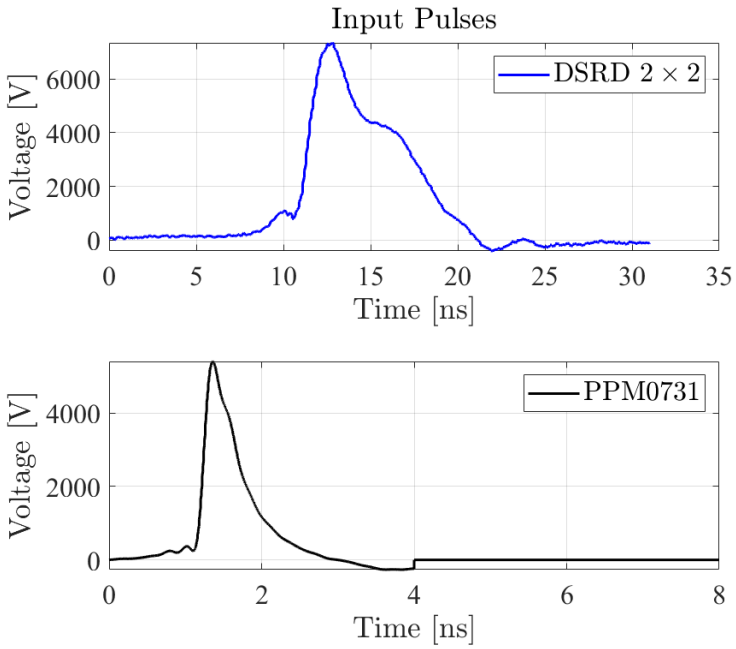


Figure 9.1.2. Input monopolar pulses used for the study.

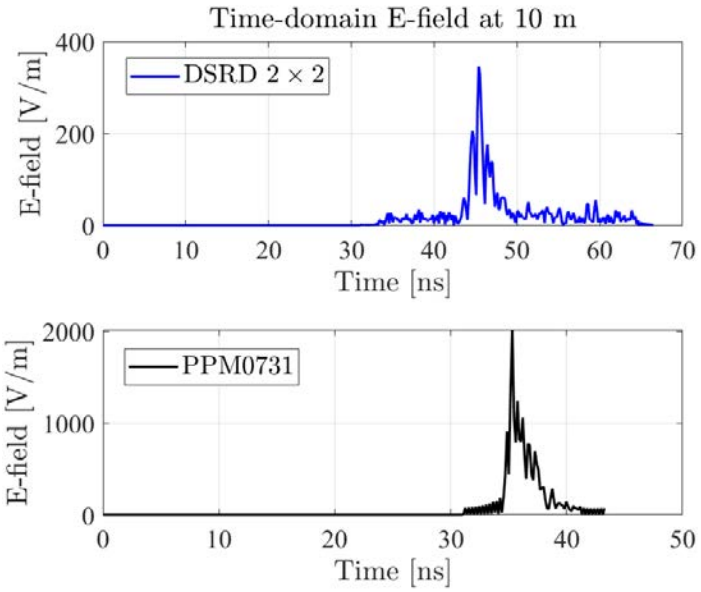


Figure 9.1.3. Time-domain electric field of the ESA, at a distance of 10 meters from the antenna element, subjected to monopolar pulses from Figure 10.1.2.

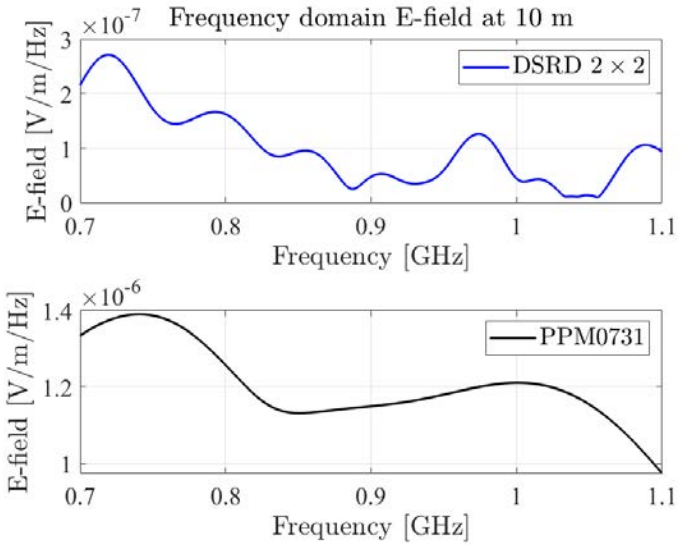


Figure 9.1.4. Frequency domain electric field of the ESA, at a distamce of 10 meters from the antenna element, subjected to monopolar pulses of Figure 10.1.2.

Table 9.1.1. The rE/V values calculated at 10 m from the antenna.

Input Pulse	rE/V at 10 m
DSRD 2×2	0.0471
PPM0731	0.3726

(E) Build minimum viable validation prototypes for arrays of ESA elements:

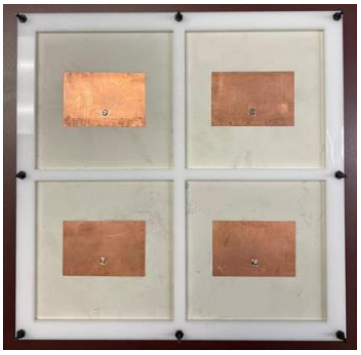


Figure 9.1.5. Manufactured prototype of the 2×2 array of narrowband, coaxial probe-fed, microstrip patch antennas, on an augmented 0.25-inch-thick, PEC-backed, TMM-10i panel.

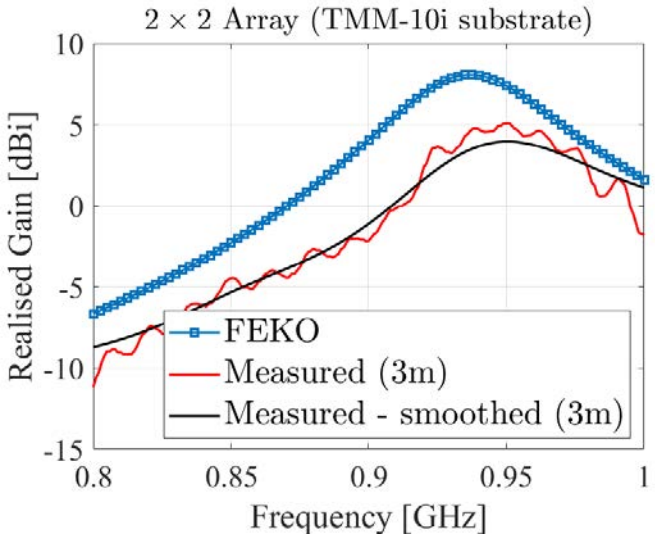


Figure 9.1.6. Comparison of the simulated and measured realized gain of the 2×2 array of ESA elements.

The experimental gain data of the 2×2 array (prototype shown in Figure 9.1.5), of narrowband microstrip patch antennas that was reported earlier in the Nov-2021 MSR showed disagreement with the FEKO-simulated gain data. It was noted that the disagreements were due to improperly matched cables and multipath reflections from nearby metal objects (as the measurements were conducted in the absence of a perfectly anechoic chamber).

To improve the agreement between the measured and simulated gain data, the testing was repeated with a different set of carefully calibrated cables. A better agreement, between the measured and simulated realized gain results has been achieved, as illustrated in Figure 9.1.6. The average 2 dBi difference that can still be observed between the newly measured and the simulated data is expected to reduce further on the elimination of multipath reflections from surrounding objects.

9.1.5 *Summary of Significant Findings and Mission Impact*

(A) Developing Array Pattern Tool for large arrays calculations:

A MATLAB code has been developed for faster approximation of the radiation pattern of a linear/planar array of any size and composed of any type of antenna elements. The code requires the center element pattern of a small array (say, 3×3) composed of the same type of antenna elements, desired lattice arrangement, and total number of array elements, as user inputs. This work will be included in future publications.

(B) Investigate the effects of array aperture area reduction on different array parameters:

The effect of different array aperture area and lattice arrangements on the array parameters (such as array gain, beamwidth, electronic beam steerability, etc.) have been reported for arrays modeled on infinite ground planes (DEC 2020 ONR-OSPRES-Grant MSR). The results show that, with 30% reduction in the aperture area ($\approx 50\%$ reduction in # of elements), the gain drops by < 3.5 dBi without any scan blindness spotted as the main beam is steered from boresight to $\pm 60°$ in the $640-990$ MHz range.

The array parameters for large arrays ($\geq 15 \times 15$) on finite ground planes could not be computed using the commercial EM solvers (FEKO and CST) due to excessive memory and time consumption. This work will be resumed after developing a method to estimate array performances on finite ground planes, either through ML or conventional approaches.

(C) Build minimum viable validation prototypes of single ESA elements:

Investigated different bandwidth enhancement techniques applicable to single layer microstrip patch ESAs:

a. Method I: Bandwidth enhancement by strategically placing the coaxial probe along 2/3rd of the patch diagonal – This method is proposed and experimentally validated using prototypes manufactured on TMM-6 and TMM-10i substrates at $2.5-5$ GHz. Antennas have been modeled on various substrates (polyethylene, G10/FR-4, TMM-10i) at the UHF range ($0.6-1$ GHz) and are being considered for manufacturing.
b. Method II: Coaxial probe-fed U-slot loaded rectangular microstrip ESAs – A prototype is manufactured on a G10/FR-4 substrate ($0.9-1.3$ GHz) and tested.
c. Method III: L-probe-fed U-slot-loaded rectangular microstrip ESAs – An antenna has been modeled on a TMM-4 substrate that operates in the $0.52-1.17$ GHz range ($\approx 77\%$ 2:1 VSWR bandwidth). Due to the fabrication complexity of the L-probe proximity coupled feed, this antenna will not be manufactured.

(D) Optimization of ESA (single element) performance using regular and ML based stochastic search algorithms:

Investigated the bandwidth enhancement of the coaxial probe-fed microstrip patch antennas, using regular and ML based stochastic search algorithms (GA, PSO, and Simplex methods), by optimizing the feed-probe location and ground plane shape and size. Compared to regular search algorithms, ML algorithms are found to be less computationally intensive (in terms of time and memory consumption).

(E) Build minimum viable validation prototypes for arrays of ESA elements:

A wideband 3×3 array (2.5-5 GHz) and a narrowband 2×2 array (900 MHz), of coaxial probe-fed microstrip patch ESA elements, on 0.25-inch-thick TMM-10i substrates, have been manufactured. The S11-parameters of the individual elements, in each array prototype, have been tested, with good agreement achieved between the simulated and the measured data. Modeling and characterization of a 4×4 square array, of wideband ESA elements in the UHF region, has been initiated for future prototyping.

(F) Optimization of array performance using ML algorithms:

(F) Initiated multi-objective optimization of a small 5×5 array by seeking the best array design parameters, including inter-element spacing, ground plane size, feed-probe locations, etc.

9.2 Tradespace Analysis of Ultra-Wide-Band (UWB) Koshelev Antenna

(Alex Dowell and Kalyan Durbhakula)

9.2.1 *Problem Statement, Approach, and Context*

Primary Problem: Determine the extent to which the physical aperture area of an antenna array, composed of antenna elements, can be reduced, while maintaining performance in peak power density, bandwidth, and electronic beam steerability over the UHF range (0.4–1 GHz), compared with present-art high-power-microwave-capable antenna arrays.

Solution Space: The Koshelev antenna has a unique design that is capable of generating an UWB response by effectively merging radiation characteristics from a transverse electromagnetic (TEM) horn antenna with exponentially tapered flares, an electric monopole, and magnetic dipoles over a wide frequency range [1]. This opens up an opportunity to investigate the design parameter space and understand parameter effects on impedance bandwidth, radiation pattern, electric field distribution, and other metrics via a tradespace study.

Sub-Problem:

(i) The integration of an impedance transformer to a single element Koshelev antenna to simulate and test the combined (transformer–antenna) performance is currently not feasible using commercial EM simulators.

(ii)The total surface currents on the Koshelev antenna over the desired frequency range arising from the present positioning of TEM exponential flares, an electric monopole, and magnetic dipoles is not yet clearly understood.

State-of-the-Art (SOTA): The balanced antipodal Vivaldi antenna (BAVA) is considered to be the SOTA antenna element due to its exceptional 20:1 impedance bandwidth ratio as well as the ability to handle tens-of-MW input power.

Deficiency in the SOTA: The BAVA design parameter space has been exhausted over the past couple of decades. The physical aperture area still remains very large and there is no viable path through tradespace study for further physical aperture area reduction.

Solution Proposed: Design, simulate, validate, and perform a tradespace study on the important design parameters of the Koshelev antenna array that effectively reduce its physical aperture area while maintaining its UWB properties, in both the frequency and time domains. The Koshelev antenna has been shown in the literature to withstand higher voltage levels (over 200 kV peak voltage), thereby making it a viable antenna element for detailed tradespace study and analysis.

Relevance to OSPRES Grant Objective: From the literature, it was shown that the Koshelev antenna can handle high input voltages (and therefore high power with 50 Ω input impedance), which satisfies the specific OSPRES objective related to high input voltage/power. In addition, this work can yield a center-frequency-dependent, bandwidth-controlled, and electronically steerable Koshelev antenna design that can be quickly modified to the spectrum properties of the ultra-fast rise time input pulse.

Risks, Payoffs, Challenges:

(i) The electrical size of the Koshelev antenna is approximately λ/4 at its lowest operating frequency. Further reduction of electrical size to λ/10 could considerably reduce frequency dependent gain, thereby decreasing the power spectral density.

(ii) Payoffs include the development of a library of antenna metrics data for different shapes and sizes of the individual parts within the Koshelev antenna.

(iii) The large electrical size (>5λ) of the Koshelev antenna at its highest operating frequency poses huge computational challenges.

9.2.2 *Tasks and Milestones / Timeline / Status*

(A) Complete literature search to identify and list antenna elements that satisfy UWB properties and HPM requirements, and down-select accordingly / NOV–DEC20 / Complete.

(B) Complete initial design, simulation, and validation of Koshelev antenna [1] / JAN21 / Complete.

(C) Perform a preliminary parameter study to identify design parameters that considerably reduce the physical aperture area / FEB–MAR21 / Complete.

- Milestone: Using FEKO and/or CST electromagnetic (EM) simulators, reduce the physical aperture size of the Koshelev antenna to at least 95% of its original design and show minimal to no variation in the bandwidth, gain and increased aperture efficiency / Complete.

(D) Determine the full-width half-maximum (FWHM) and ringing metrics from the envelope of the time domain impulse response ($h_{rx/tx}(t, \phi, \theta)$) in receive or transmit mode / MAR–APR21 / Complete.

- Milestone: Produce a generalized code that calculates the impulse response envelope of the Koshelev antenna and plots the rate of change in FWHM and ringing values as a function of physical aperture size.

(E) Perform tradespace studies on design parameters such as feed position (*F*), length (*L*), and alpha (α). Obtain various antenna metrics data, compare, and analyze / MAR21/ Complete.

- Milestone: Identify Koshelev antenna design parameters that significantly alter the bandwidth, rE/V, peak gain over the desired bandwidth, and aperture efficiency.

(F) Reduce Koshelev antenna aperture size (H×W) to equal to or less than 90 mm × 90 mm, equal to that of the SOTA BAVA, for direct antenna metrics comparison / MAR–APR21 / Complete.

- Milestone: Provide a recommendation on the optimum design parameters and the resulting metrics, with comparison to SOTA BAVA. The optimized design parameters must yield 900 MHz ± 200 MHz bandwidth, rE/V greater than 1, peak gain around 3 dBi at 900 MHz, aperture efficiency equal to or greater than 130% at 900 MHz.

(G) Using the optimized model from (F), build various array simulation models/topologies to perform a tradespace study and report tradeoffs between array antenna metrics such as center element reflection coefficient (S11) value, gain vs theta at constant phi, physical aperture area, aperture efficiency, and rE/V / MAY–JULY21 / Complete.

- Milestone: Develop/showcase an optimized Koshelev array model that exceeds an aperture efficiency of 130% with a high rE/V.

(H) Perform literature search to investigate, understand, and determine the applicability of special electromagnetic (EM) techniques to the antennas under consideration. / JAN–APR21 / Complete.

(I) Explore impedance taper (microstrip based and coax based) designs that can interface well (both mechanically and electrically) to transition the signal from a coax cable to the input of the Koshelev antenna element / JULY21–AUG21 / Complete.

- Milestone: Recommend the optimum impedance taper design (with minimum reflections and maximum power transfer) with the optimum dimensions to successfully convert the high-voltage, short-rise time input signal from a coax cable to the feed of the Koshelev antenna array.

(J) Study response from optimized Koshelev antenna array when excited with different monopolar, differential, and bipolar pulse signals of significant interest / AUG21–NOV21 / Ongoing.

- Milestone: Provide a table comparing the Koshelev antenna array response metrics and narrow down the suitable pulse signals. Recommend (if any) changes to the downselected pulse signal(s) that can further improve the radiation efficiency, and/or transient gain.

(K) Investigate and analyze the response from the optimized Koshelev antenna array when excited by different excitation patterns **(NEW)** /DEC 21/Complete.

- Milestone: Compare and recommend an appropriate excitation method to yield maximum boresight gain, maximum half-power beamwidth (HPWB), minimum side lobe levels, and maximum electric field, rE/V.

(L) Prototype single element Koshelev antenna and test for reflection coefficient, gain as a function of frequency, radiated electric field at 1-m, 2.5-m, 5-m and 10-m (if feasible) distances. / AUG21–DEC21 / Ongoing.

- Milestone: Report measured data and recommend any improvements to the fabrication/prototyping/testing methods.

9.2.3 *Progress Made Since Last Report*

(K)

In the last month, the optimized Koshelev antenna array has been subjected to different excitation patterns available in CST microwave studio. Seven excitation patterns are available for this study: 1) Uniform, 2) Cosine, 3) Cosine-square, 4) Taylor, 5) Binomial, 6) Chebyshev, and 7) Gaussian. These excitation patterns were selectively used in the research community to reduce side lobe levels, increase tapering, etc. In this report, we compared the frequency domain gain response at the boresight and time domain electric field response at 10 m radiated by the optimized Koshelev antenna array when fed by the excitation patterns.

(L)

We have tested the first 3D printed single element Koshelev antenna prototype. Frequency domain scattering parameters data was collected in the testing, which gives reflection coefficient, bandwidth, and gain metrics.

9.2.4 *Technical Results*

(K) Seven excitation patterns have been applied to the feeds of the optimized Koshelev antenna to understand the behavior of antenna array under these excitations. Fig. 9.2.1 shows the E-plane gain result (simulated at 900 MHz) compared between different excitation patterns. The uniform and Gaussian excitation patterns yielded the maximum peak gain of 11 dBi at boresight (θ = 0°). However, those two excitation patterns also yielded the maximum side lobe level. Alternatively, the Taylor, Binomial and Chebyshev excitation patterns yielded gain values close to 10 dBi at boresight. Moreover, these 3 excitation patterns yielded minimum side lobe levels without reduction in HPBW. The cosine and cosine-square excitation patterns yielded low peak gain value of 5 dBi at boresight with higher side lobe levels than other excitation patterns. Seven excitation patterns have been applied to the feeds of the optimized Koshelev antenna to understand the behavior of antenna array under these excitations. Fig. 9.2.1 shows the E-plane gain result (simulated at 900 MHz) compared between different excitation patterns. The uniform and Gaussian excitation patterns yielded the maximum peak gain of 11 dBi at boresight (θ = 0°). However, those two excitation patterns also yielded the maximum side lobe level. Alternatively, the Taylor, Binomial and Chebyshev excitation patterns yielded gain values close to 10 dBi at boresight. Moreover, these 3 excitation patterns yielded minimum side lobe levels without reduction in HPBW. The cosine and cosine-square

excitation patterns yielded low peak gain value of 5 dBi at boresight with higher side lobe levels than other excitation patterns.

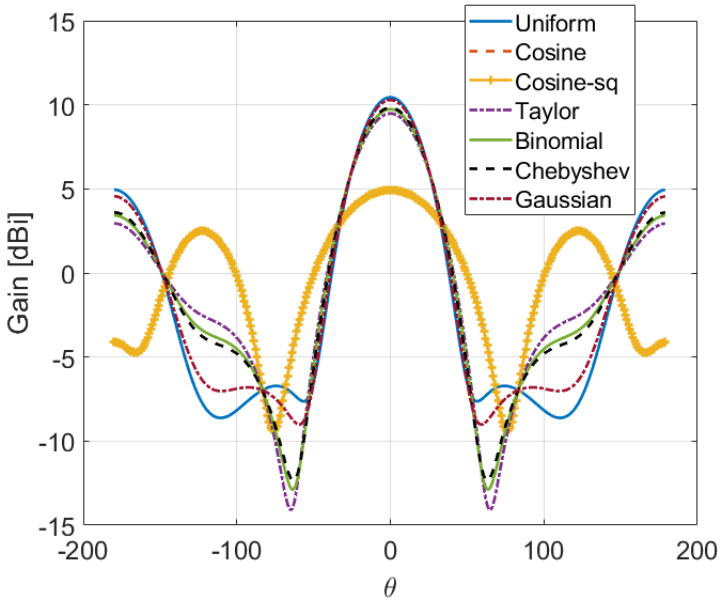
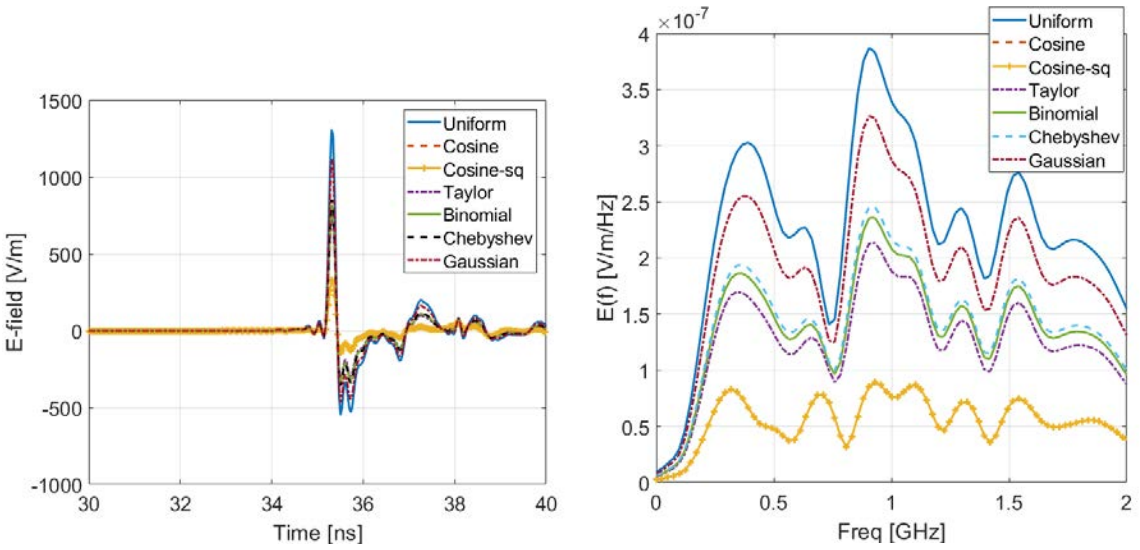


Figure 9.2.1. Boresight gain radiated by the optimized Koshelev antenna array under different excitation patterns.

(K) In addition to frequency domain gain result, the time-domain electric field response at 10 m distance from the aperture of the array is shown in the report. The input signal used for this study is the MI0731 waveform, which has been deemed as the optimum waveform for maximum rE/V in the previous report. Fig. 9.2.2(a) compares the E-field result at 10 m distance obtained by feeding seven excitation patterns mentioned earlier. The observations from time-domain E-field results follows a similar trend as the frequency domain gain at boresight. The uniform and Gaussian excitation patterns tend to yield maximum peak E-field, while the cosine and cosine-square excitation patterns yielded the minimum peak E-field. Fig. 9.2.2(b) shows the E-field spectrum comparison between all excitation patterns. It is evident from Fig. 9.2.2(b) that the maximum E-field spectrum is obtained from using an uniform excitation pattern followed by a Gaussian excitation pattern. The peak E-field, rE/V, and energy density metrics for the seven excitation patterns are shown in Table 9.2.1.



(a) (b)

Figure 9.2.2. Boresight gain radiated by the optimized Koshelev antenna array under different excitation patterns.

Table 9.2.1. Optimized Koshelev antenna array E-field response metrics at 10 m under different excitation patterns.

Excitation Pattern	Epeak [V/m]	rE/V	Ed [uJ/m2]
Uniform	1309.3	2.42	0.83
Cosine	326.27	0.6	0.05
Cosine-square	326.27	0.6	0.05
Taylor	743.46	1.37	0.26
Binomial	817.77	1.51	0.32
Chebyshev	849.92	1.57	0.34
Gaussian	1133.72	2.05	0.59

(L) The first 3D printed and metallized single element Koshelev antenna with integrated impedance transformer prototype has been tested for reflection coefficient (S11). The measured S11 is then compared against the simulated S11. Fig 9.2.3 shows this comparison. The measured and simulated does not overlap on top of each other, however, the measured S11 stays below -10 dB for most of the measured frequency

range. The main source of disagreement between simulated and measured data is more prominent in the high frequency i.e., above 2 GHz. We believe this disagreement originated from the impedance transformer which was believed to have some air gaps. We are currently working on improving the fabrication quality of embedded impedance transformer by 3D printing a thicker Koshelev antenna (3 mm).

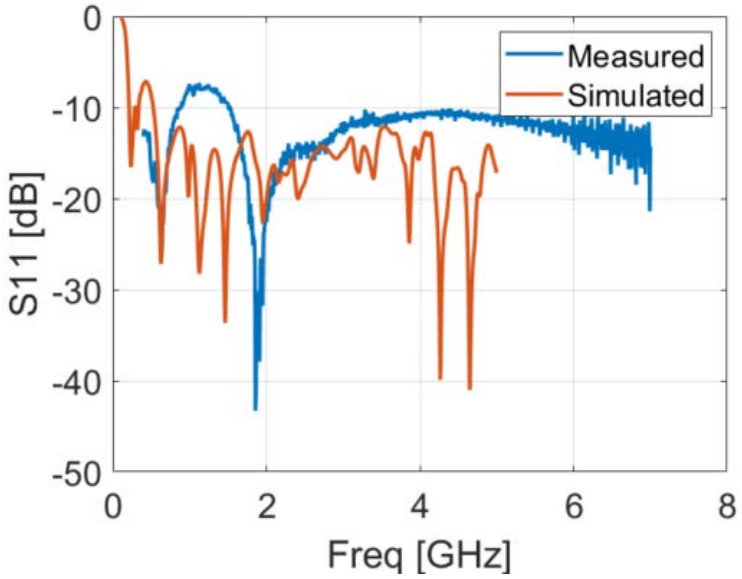


Figure 9.2.3. Simulated vs measured reflection coefficient (S11) of single-element Koshelev antenna.

9.2.5 *Summary of Significant Findings and Mission Impact*

(A) An extensive literature search on various UWB antenna elements has resulted in finding three promising options. The down-selected elements are the Koshelev, Shark, and Fractal antennas, which will be extensively studied using their individual design parameter space, which could result in physical aperture area reduction of the single antenna element. Later, the single antenna element will be converted into a planar array.

(B) Initial validation of the Koshelev antenna simulated using CST software agreed well with the antenna metrics published in the open literature [1]. A UWB bandwidth response (10:1 bandwidth) and rE/V > 1 has been observed from our initial simulations of the Koshelev antenna. This validation ensured that the Koshelev antenna can be subjected to further tradespace studies to understand its performance followed by optimizing the design according to OSPRES grant requirements.

(C) The initial tradespace study and analysis of the Koshelev antenna design yielded promising outputs to carry forward the investigation. A comparison of important antenna metrics between the Koshelev antenna in [1] and aperture reduced Koshelev antenna are shown in Table 5.2.1 of the APR 21 MSR.

(D) An in-house code has been developed to calculate important UWB time domain antenna metrics such as full-width half maximum (FWHM) and ringing. These metrics have been calculated using in-house MATLAB code using the excitation voltage and radiated electric field information obtained from CST simulations. FWHM and ringing antenna metrics help with assessing or characterizing an antenna's UWB response.

(E) The tradespace study of feed position provided a deeper understanding of how its position impacts the S11 value bandwidth. An optimum value for feed position i.e., $F = 1/20 < L < 1/10$ is recommended to achieve maximum bandwidth. The tradespace study of the antenna length (L) is straightforward. A longer antenna length will radiate better at lower frequencies. However, physical size restrictions/requirements must be kept in mind in determining the antenna length. Finally, a larger α value (>120°) is recommended to avoid unnecessary reflections from the electric monopole.

(F) From a thorough tradespace study, the aperture size of the Koshelev antenna (single element) is determined to be 90 mm × 100 mm in order to achieve desired antenna metrics performance proposed in the milestone. All metrics described in the milestone have been successfully achieved except the desired bandwidth (200 MHz on both sides) at 900 MHz center frequency. The bandwidth achieved is 900 ± 100 MHz.

(G) The physical aperture area of the Koshelev array antenna largely depends on the interelement spacing and the shape of the array. We were able to determine that the diamond topology is the optimum shape for the Koshelev array antenna. We were also able to obtain similar gain profile (peak gain and pattern) from making certain elements within the array passive (off state) when compared against regular active array (all elements in on state). From the non-symmetric interelement spacing values, we found that S_y has the least effect on the output; therefore a small spacing value can be chosen to reduce the physical aperture area of the Koshelev array.

(H) The literature search on the special EM techniques expanded our knowledge and opened the door to opportunities to apply some of those techniques to the antennas under study. EM techniques such as non-symmetric and non-square array topologies have been applied to the development and study of the Koshelev array antenna.

(I) The first impedance taper design under consideration has shown good S11 values (< -10 dB) over the frequency range of interest. In addition, we have shown that the shape of the pulse can be easily retained at the output of the taper with less than 5% amplitude losses.

(J) The Koshelev antenna array response from feeding a monopolar vs bipolar signal has demonstrated a clear winner: that is, a bipolar signal will radiate at least 10 times better than a monopolar signal. A comparison of the frequency spectrum of the radiated electric field from the optimized Koshelev antenna array between different monopolar pulse sources has identified the 'MI0731' pulse to be the optimum pulse.

(K) The uniform and Gaussian excitation patterns were determined to be the optimum excitation patterns. Selecting these excitation patterns would result in maximum electric field at boresight.

9.2.6 *References*

[1] Gubanov, V. P., et al. "Sources of high-power ultrawideband radiation pulses with a single antenna and a multielement array." *Instruments and Experimental Techniques* 48.3 (2005): 312-320.

9.3 Tradespace Analysis of Ultra-Wide-Band (UWB) Shark Antenna

(Kasey Norris and Kalyan Durbhakula)

1.2.1 Problem Statement, Approach, and Context

Primary Problem: Determine the extent to which the physical aperture area of an antenna array, composed of antenna elements, can be reduced, while maintaining performance in peak power density, bandwidth, and electronic beam steerability over the UHF range (0.4–1 GHz), compared with present-art high-power-microwave-capable antenna arrays.

Solution Space: An array of Shark antenna elements with an emphasis on inter-element and intra-element spacing effects is a good candidate for UWB HPM systems while having a reduced aperture area with respect to the current state-of-the-art. In the literature, the Shark antenna has already been shown to achieve a wide 20:1 impedance bandwidth, low dispersion, and a sectoral (also referred to as directional) radiation pattern.

Sub-Problem: The design parameter space of the Shark antenna has not been studied rigorously in the literature and therefore the effect of these parameters on the antenna metrics is not understood. In addition, the Shark antenna has been shown to be not very directive in the H-Plane. Preliminary studies have shown that aperture efficiencies at low frequencies are much better than at higher frequencies.

State-of-the-Art (SOTA): The balanced antipodal Vivaldi antenna (BAVA) is considered to be the SOTA antenna element due to its exceptional 20:1 impedance bandwidth ratio as well as the ability to handle tens-of-MW input power.

Deficiency in the SOTA: The BAVA design parameter space has been exhausted over the past couple of decades. The physical aperture area still remains very large and there is no viable path through tradespace study for further physical aperture area reduction.

Solution Proposed: Explore the array tradespace by generating different array topologies/lattices (hexagonal, octagon, square, elliptical) and with different intra and interelement spacing combinations.

Relevance to OSPRES Grant Objective: The Shark antenna dimensions were established to be frequency dependent and can be readily modulated to fit the spectrum characteristics of an ultra-fast rise time input pulse.

Risks, Payoffs and Challenges:

(i) The Shark antenna is comprised of flare-angle-dependent bicones that are truncated in the azimuthal angle. This still yields considerably higher half power beam width

(HPBW) than other antenna elements under investigation. The significant reduction of HPBW in the H-plane may be unattainable and can be considered a major risk.

(ii) Payoffs include the development of a library of antenna metrics data for various shapes and sizes of the bicones and reflector plates in the shark antenna.

(iii) Computational challenges remain present with respect to automation of design parameter space on our currently used supercomputer (LEWIS). Design challenges persist in obtaining lower operating frequencies while not increasing the height of the antenna and surpassing the 90 mm × 90 mm size requirement.

9.3.1 *Tasks and Milestones / Timeline / Status*

(A) Complete initial design, simulation, and validation of the Shark antenna / JAN21 / Complete.

(B) Validate Shark antenna design using the LEWIS supercomputer over a wider range of frequency results (up to 20 GHz) / FEB–MAR21 / Complete.

(C) Identify Shark antenna design parameters which contribute significantly to bandwidth, gain, and physical aperture area. Determine which parameters contribute most to performance improvement/size reduction/ FEB–MAR21 / Complete.

(D) Perform a tradespace study by simulating the Shark antenna with varying cases of flare angle, cone length, and distance to backplane. Gain a general understanding of how these parameters affect impedance bandwidth, rE/V, gain and HPBW / FEB–MAY21 / Complete.

- Milestone: produce a detailed summary of change in impedance bandwidth, rE/V, HPBW in H-plane and E-plane as a function of flare angle (α), cone height (h), and distance to backplane (d) / Complete.
- Milestone: Choose optimal Shark antenna design that has the lowest operating frequency within size requirements based on tradespace study / Complete.

(E) Using the optimal Shark antenna design in (D), simulate various array geometries including hexagonal, rectangular, and circular arrays. Determine which array geometries are optimal and analyze aperture fields and aperture efficiencies. Further study the effect of different time-domain waveforms in the far-field radiated by the optimized Shark antenna array / MAY–NOV2 / Ongoing.

- Milestone: Produce a report which states the effects of various array geometries for the Shark antenna. The optimal array geometry chosen should have the least interference between elements, therefore yielding higher impedance bandwidth and higher aperture efficiency. Overall, the optimal Shark array geometry should have at least 20% impedance bandwidth at 900 MHz center frequency for the centermost element with 130% array aperture efficiency, ± 60 degrees beam steering capability, and rE/V equal to or greater than 4. Identify a waveform that combines well with the optimized Shark antenna array in terms of peak electric field, rE/V, and energy density.

(F) Begin prototyping and validation of optimal Shark antenna single element. / JUN–OCT21 / Ongoing.

- Milestone: Have a finished Shark antenna prototype. Compare S11 and radiation pattern with simulated Shark antenna.

9.3.2 *Progress Made Since Last Report*

(F)

The single element Shark antenna shown in Fig. 9.3.1 has been tested for reflection coefficient (S11) in the last month.

Figure 9.3.1. 3D printed and metallized prototype of single element Shark antenna.

9.3.3 *Technical Results*

(F) The single element Shark antenna has been tested for S11 and found that the measured S11 has lower bandwidth than the simulated S11. Fig. .3.2 shows the measured S11 from 400 MHz to 7 GHz. The Shark antenna started to radiate at approximately from 2 GHz and onwards. At high frequencies (> 5 GHz), ripples can be noticed due to feed fabrication inaccuracies. To remind, the Shark antenna input impedance is 150 ohms therefore a coax transformer has been designed and incorporated into one of the two bicones. It has become difficult to fabricate such small feeds accurately and precisely with in-built impedance transformer.

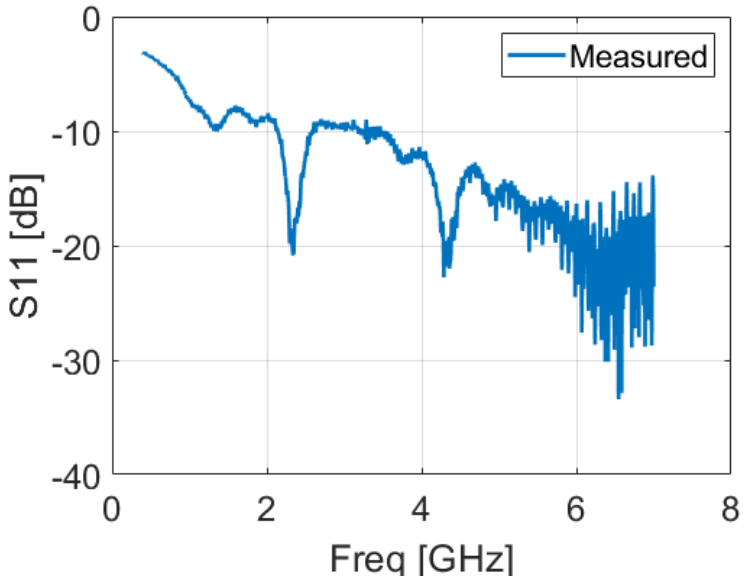


Figure 9.3.2. Radiated electric field at 10 meters distance from the antenna array aperture when fed with different monopolar pulse source signals/waveforms.

9.3.4 *Summary of Significant Findings and Mission Impact*

(A-B) The Shark antenna has been designed, simulated, and validated according to [1].

(C) The Shark antenna design parameters that have been found to contribute significantly to bandwidth performance, directivity, and gain are the cone height (*h*) and distance to backplane (*d*).

(D) The Shark antenna tradespace study has been completed and has provided insight into the Shark antenna design space. Increasing the cone height *h* yields better impedance bandwidth at low frequencies and is more directive in the *e* and *h* planes. However, increasing *h* results in a larger aperture area. To remain within 90 x 90 mm, the maximum *h* value is 45 mm; with this a lowest operating frequency of 815 MHz is achievable.

(E) The elliptical Shark antenna has the optimum metrics, which can be found in Table 6.3.1 in July 2021 MSR. The metrics from elliptical Shark antenna are closer to desired metrics provided in milestone 6.3.2 (E). The interelement spacing variable study has provided insight into the workings of Shark antenna array. The Shark antenna array is more sensitive to the interelement spacing variable in x-axis than in the y-axis. The elliptical topology has significantly smaller sidelobe level values and similar frequency-domain gain or transient gain values when compared against square and hexagonal topologies. If the input is a monopolar signal, a hexagonal or an elliptical topology is preferred. If the input is a bipolar signal, an elliptical topology is recommended for its decent transient gain value with significantly smaller sidelobe levels.

9.3.5 *References:*

[1] L. Desrumaux, A. Godard, M. Lalande, V. Bertrand, J. Andrieu and B. Jecko, "An Original Antenna for Transient High Power UWB Arrays: The Shark Antenna," in IEEE Transactions on Antennas and Propagation, vol. 58, no. 8, pp. 2515- 2522, Aug. 2010, doi: 10.1109/TAP.2010.2050418.

9.4 Machine Learning Inspired Tradespace Analysis of UWB Antenna Arrays

(Sai Indharapu and Kalyan Durbhakula)

9.4.1 *Problem Statement, Approach, and Context*

Primary Problem: Determine the extent to which the physical aperture area of an antenna array, composed of antenna elements, can be reduced while maintaining performance in peak power density, bandwidth, and electronic beam steerability over the UHF range (0.4–1 GHz), compared with present-art high-power-microwave-capable antenna arrays.

Solution Space: Fractal antennas possess exceptional fidelity factor values (>0.9), which describe how well the shape of the input pulse is retained at an observation point in the far-field. Their high degree of freedom provides an opportunity to develop systematically modified patch shapes, which in turn leads to improved bandwidth while retaining high fidelity factor values. Machine learning (ML) can be leveraged to predict the antenna array response for an arbitrary design parameter space upon sufficient training and validation.

Sub-Problem:

(i) Fractal antennas generate omni-directional radiation patterns in the H-plane over the desired frequency range.

(ii) ML can suffer from underfitting or overfitting the training model which in turn leads to deviations in the predicted output.

State-of-the-Art (SOTA): Conventional full-wave EM solvers such as method of moments (MoM), multi-level fast multipole method (MLFMM), finite element method (FEM), and finite difference time domain (FDTD) method are currently being used to study, analyze and assess the performance of UWB antennas.

Deficiency in the SOTA: UWB antenna optimization using conventional EM solvers utilizes significant computational time and memory resource.

Solution Proposed:

(i) Design, simulate, validate, and perform a tradespace study on the design parameter space of the selected fractal antenna element using commercially available electromagnetic (EM) wave solvers.

(ii) Train, validate, test and compare multiple ML models for quicker and accurate prediction of antenna array response for different physical aperture areas.

Relevance to OSPRES Grant Objective: The fractal antenna achieves an UWB response, a mandatory requirement of the OSPRES grant objective, in a small volume footprint and similar physical aperture area when compared against the SOTA BAVA, dual ridge horn antennas etc. Furthermore, the microstrip-design-based fractal antenna can efficiently handle electronic steering by integrating the feed network on the same board. This eliminates the need to build a separate feed network external to the fractal antenna using bulky coaxial cables.

Risks, Payoffs, and Challenges:

(i) A majority of the fractal antenna geometries yield an omni-directional pattern in the H-plane, which can be a risk. However, efforts are underway to mitigate this pattern without deteriorating bandwidth.

(ii) Payoffs include developing a library of antenna metrics data for various fractal shapes and sizes.

(iii) Design challenges and numerical calculations with respect to specific fractal shapes could arise after performing a certain number of iterations to further improve the bandwidth.

(iv) Fractal antennas were known to generate gain loss at random frequencies over their operating frequencies. Achieving gain stability over the desired frequency range can be a significant challenge.

9.4.2 *Tasks and Milestones / Timeline / Status*

(A) Perform tradespace analysis of the fractal element radius *b* over the desired frequency range (4 to 12 GHz) using the genetic algorithm (GA) optimization tool available in the commercial electromagnetic (EM) solver FEKO / FEB21 / Complete.

- Milestone: Provide a recommendation of an optimum value of *b* using OPTFEKO to minimize reflection coefficient or S11 (< –10 dB).

(B) Perform tradespace study on different fractal shapes by changing the number of fractal segments to understand the effect of this change on the impedance bandwidth / FEB21 / Complete.

- Milestone: Produce a detailed study of the antenna response such as S11, gain, and bandwidth by varying the number fractal segments.

(C) Apply the GA optimization tool on the fractal side length *b* over a wide frequency range (2 to 12 GHz with 201 discrete frequency points) and number of fractal segments using OPTFEKO on the LEWIS cluster / MAR21 / Complete.

- Milestone: Reduce physical aperture area by 10% of its present design, reported in the FEB MSR, and demonstrate minimal or no change in S11, gain, and fidelity factor values.

(D) Perform a parametric study and analysis of antenna response by varying hexagon radius, *a* / MAR–APR21 / Complete.

- Milestone: Recommend a value of *a* to reduce the physical aperture area and increase aperture efficiency (>50%) with no variation in other antenna metrics.

(E) Frequency scale fractal antenna design such that the center frequency of the resulting antenna equals 1.3 GHz / MAY21 / Complete.

- Milestone: Modify antenna design with a center frequency equal to 1.3 GHz and achieve similar results (3:1 bandwidth at fc = 1.3 GHz, 3 dBi gain and >130% aperture efficiency at 900 MHz) to antenna design at center frequency ~7 GHz.

(F) Design and simulate various array antenna geometries composed of optimized fractal antenna elements (obtained from (E)) to analyze the effect of overall array antenna geometry on the desired array antenna response metrics (i.e., gain vs. frequency, gain vs. elevation angle at constant phi, rE/V, half-power beamwidth and side-lobe level.) / MAY–JUL21 / Complete

- Milestone: Recommend a best possible structure with reduced aperture area and minimal loss in gain.

(G) Apply ML models available in Altair Hyperstudy (2021) on the fractal antenna to try and understand the possibilities and limitations of ML models for fast and efficient antenna metrics prediction and optimization. Expand the prediction capability to time-domain electric field using ML models implemented on Python programming tools. / MAY21–FEB22 / Ongoing.

- Milestone: Recommend most accurate and efficient ML model for a fractal antenna in time-domain and frequency domain.

(H) Apply ML models on the octagon fractal antenna array lattice to extend the prediction capabilities of ML models. / SEP21–JAN22 / Ongoing.

- Milestone: Recommend the best suitable ML model implemented/developed using Python programming language for array antenna metrics prediction.

9.4.3 *Progress Made Since Last Report*

(G) In the previous report, time-domain electric field prediction using kNN alogirthm has been presented and compared against traditional FEKO output. The comparison was done assuming Gaussian pulse as the input waveform. The results agreed well with a low RMSE value (< 1). We extended the prediction capability to other time-domain waveforms such as DSRD 4x2, MI0731, and NPG22, which are monopolar in nature.

(H) In the case of array response prediction, we pursued to predict reflection coefficient (S11) of non-symmetric individual elements in an array shape. In an octagon array shape, the S11 of a center element and any corner element are unique and the S11 of other element would either be equal to center or corner elements as shown in Fig. 9.4.1. Moreover, we also expanded the prediction to octagon array gain at boresight.

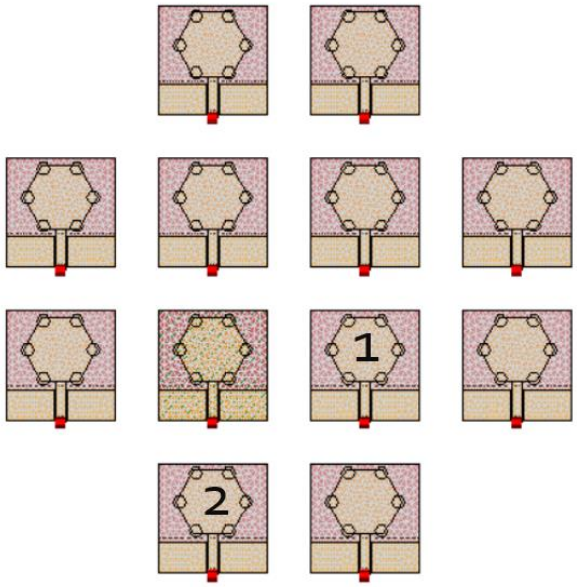
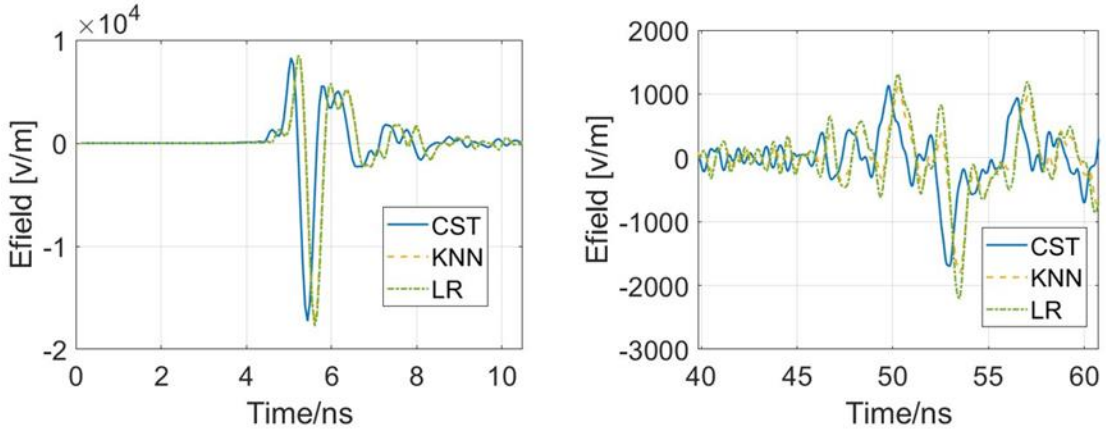
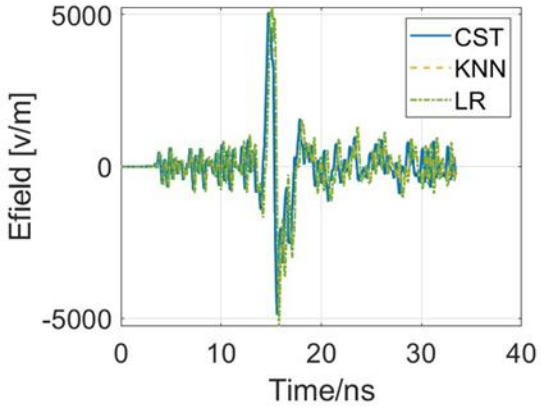


Figure 9.4.1. Center element is indicated ‘1’ and Corner element is indicated ‘2’.

9.4.4 *Technical Results*



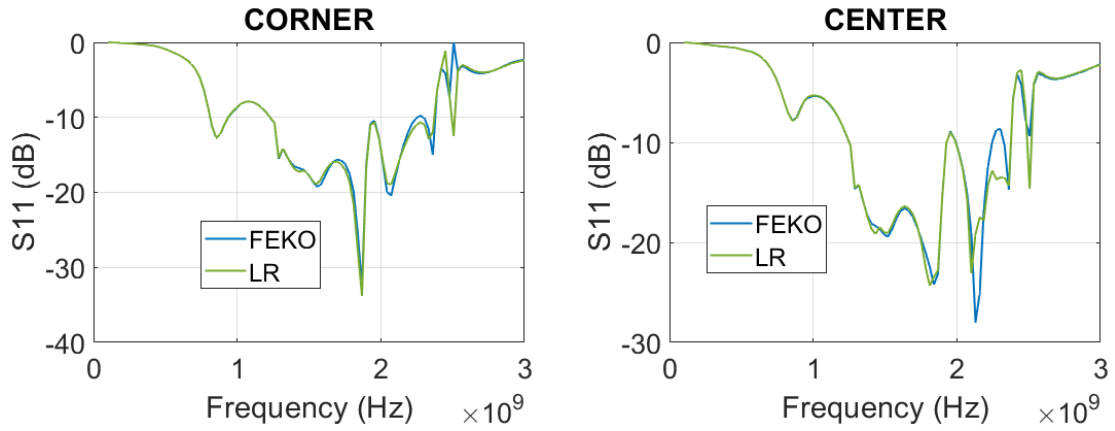
(a) (b)



(c)

Figure 9.4.2. Electric field prediction using kNN and LR ML models at 1 m distance from the aperture of the single-element fractal antenna for (a) DSRD 4x2 input waveform, (b) NPG22 input waveform, and (c) PPM0731 input waveform.

(H) The ML prediction of reflection coefficient (S11) for center and corner elements has been expanded using a new algorithm linear regression (LR), which is available on Python tool. Fig. 9.4.3 compares the traditional FEKO output against S11 predicted using kNN and LR ML models. As we can observe, the LR ML model agrees better with the FEKO output than the kNN. This can be seen for both center and corner elements. Table 9.4.1 compares the RMSE values obtained from the kNN and LR models in their prediction of S11 for center and corner elements. It is evident from Table 9.4.1 that LR ML model implemented on Python yields lower value than the kNN ML model for center and corner elements.



(a) (b)

Figure 9.4.3. Comparison of S11 predicted by kNN and LR ML models against FEKO for (a) Corner element, (b) Center element.

Table 9.4.1. RMSE values for center element and corner element prediction using kNN and LR ML models.

RMSE			
Center Element		Corner Element	
kNN	LR	kNN	LR
2.2340	1.6124	1.7352	1.3922

(H) Boresight gain is an important metric to consider when characterizing antenna's performance. Therefore, the models have been applied to predict gain at boresight for the optimized octagon antenna array. Fig. 9.4.4 compares the gain predicted using kNN and LR ML models against FEKO gain for the optimized octagon antenna array. Both ML models, kNN and LR, have shown decent agreement in the gain prediction over the frequencies of interest. The RMSE values obtained from kNN and LR gain prediction are 4.8379 and 4.1652, respectively. Although these values are lower than the S11 RMSE values, we believe this huge error is caused by the numerical error in the FEKO training data around 2.5 GHz. This error can also be seen in Fig. 9.4.4. One way to solve such kind of numerical errors is to employ extremely fine mesh to discretize the antenna geometry.

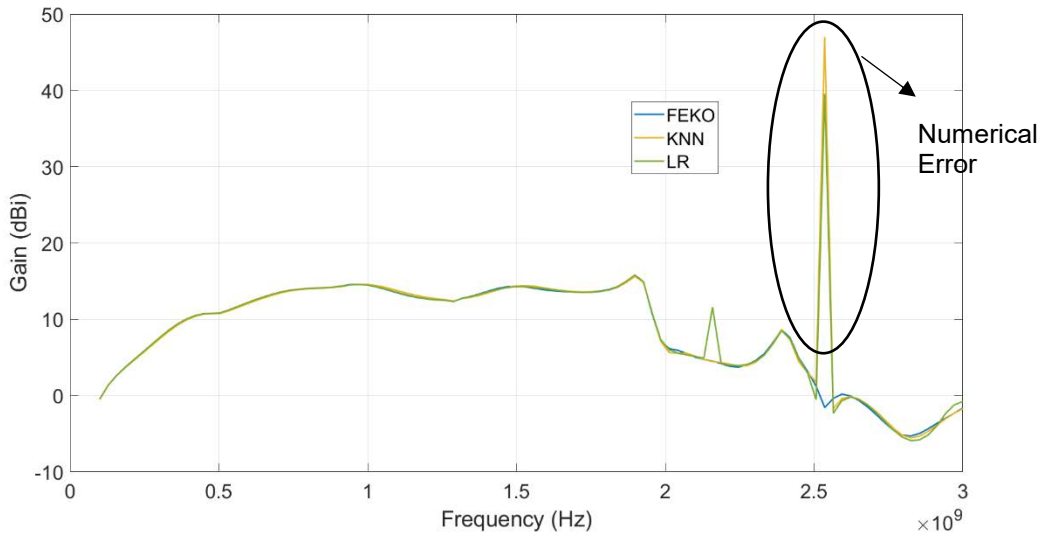


Figure 9.4.4. Gain prediction using kNN and LR ML models.

9.4.5 *Summary of Significant Findings and Mission Impact*

(A) The initial analysis of the simulation results with fractal radius *b* equal to 1.8 mm yielded multiple resonant frequencies with enhanced bandwidth. To further increase the bandwidth, OPTFEKO has been used as an optimization tool with fractal radius *b* as the optimization variable. The optimum value for *b* is found to be 1.66 mm. A comparison between reflection coefficient for initial *b* (= 1.8 mm) value and the

optimized *b* (= 1.66 mm) can be found in Figure. 6.4.6. The optimization is carried out over 51 discrete frequency points.

(B) The addition of fractal elements (*N*) to the simple hexagon improved antenna metrics such as S11. To further investigate and understand the fractal elements, the number of segments in the fractal geometry has been varied. The improvement in bandwidth is observed as the value of *N* is increased from 6 to 14.

(C) The initial optimum value of *b* over 51 discrete frequency points is reported as 1.66 mm in task (A). To further increase the accuracy of the optimization algorithm and to find a more precise value for *b*, optimization is further performed over wider frequency points (201 discrete points between 2 GHz to 12 GHz) which yielded the optimum value of b as 1.368 mm. The S11 response of antenna design with newly found *b* (i.e., 1.368 mm) hasn't produced any better bandwidth with respect to *b* (= 1.66 mm). Thus, *b* is set to be 1.66 mm for further research.

(D) The hexagonal patch radius *a* has a significant effect on the physical aperture area of the antenna. Therefore, Altair OPTFEKO has been utilized to find an optimum *a* value, which was found to be 8 mm over the range 7.2 to 9 mm. Antenna metrics such as S11, gain, and bandwidth have shown desired performance with the optimized *a* value.

(E) The initial antenna design has been modified to achieve a center frequency of ~1.3 GHz. The gain value at 900 MHz is 3.5 dBi and, with the modified antenna design, we were able to achieve an impedance bandwidth ratio of 3.3:1. The designed antenna has been fabricated and tested, and the S11 response of the fabricated antenna agrees well when compared against FEKO, CST.

(F) To summarize, four different fractal antenna array geometries (i.e., square, diamond, hexagon, and octagon) have been designed and simulated. Upon comparing antenna array metrics, octagonal fractal antenna array has yielded minimal sidelobe levels with a gain of 15.7 dBi at 900 MHz close to that of square geometry with 32.27% lower physical aperture area than that of square geometry. The octagonal fractal antenna array has been chosen as the optimum geometry with reduced aperture area and reduced side lobes while retaining the bandwidth and gain milestone metrics.

(G) Radial basis function (RBF) and least square regression (LSR) were down selected from the initial three ML models based upon their generalization capability for prediction of reflection coefficient (S11), gain, and electric field. Further analysis of increasing training data set size has shown no improvement in prediction accuracy. Trained ML models were tested for design variable values outside the training range. The resulting RMSE increased as the values drifted away from the mid-point of the training range. RBF performed well in the prediction of S11, while LSR performed slightly better for gain and electric field predictions. In addition, for time-domain electric field prediction, we recommend using k-nearest neighbors (kNN) ML algorithm for accurate prediction.

(H) Initial application of kNN ML model for the prediction of antenna array bandwidth response of center and corner element yielded positive results with a good agreement between traditional EM solver (FEKO) and trained kNN ML model. The new LR ML

model yielded improved RMSE values (over kNN) in its prediction of reflection coefficient and gain for the optimized octagon fractal antenna array.

9.4.6 *References*

[1] H. Fallahi and Z. Atlasbaf, "Study of a Class of UWB CPW-Fed Monopole Antenna With Fractal Elements," in IEEE Antennas and Wireless Propagation Letters, vol. 12, pp. 1484-1487, 2013, doi: 10.1109/LAWP.2013.2289868.

10 RF Coupling

10.1 Enclosure Effects on RF Coupling

(Mohamed Hamdalla and Ahmed Hassan)

10.1.1 *Problem Statement, Approach, and Context*

Primary Problem: UAVs are typically considered metallic/dielectric enclosures depending on their frame material. The shielding effectiveness of such enclosures might be compromised due to the slots and gaps on these enclosures, creating upset susceptibility to the enclosed electronics. The goal of this work is to quantify how the thresholds for upset susceptibility of enclosed wires and integrated circuits differ from those in free space.

Solution Space: Study enclosures with different shapes, material compositions, and slots to quantify their effect on RF coupling to the enclosed wires and electronics typically used in UAVs. The study will focus on the low-frequency range where the incident wavelength is comparable to the size of the enclosure or larger.

Sub-Problem: UAVs are manufactured with a wide variety of shapes and composites to accomplish an exponentially expanding list of missions. The configurations previously reported in the literature have simplistic assumptions regarding the shape and material composition of UAV enclosures that might overestimate or underestimate susceptibility.

State-of-the-Art (SOTA): Simple statistical analysis of specific enclosure configurations using either brute force simulations/measurements or pure statistical methods. Also, simplified UAV wire distributions are assumed.

Deficiency in the SOTA: Brute force simulations/measurements of the voltages and currents induced in wires and integrated circuits contained in enclosures are computationally or experimentally complex and have several limitations. The computations are complicated by the multiscale nature of the simulations, and the experiments are complicated by the cost of the equipment and the extensive time needed to measure every variation to cover all possible scenarios. Statistical methods, such as the Random Coupling Model (RCM) for example [1], are only accurate for high frequencies where the wavelength is much smaller than the size of the enclosure. Another main deficiency of the RCM is that it can't predict the exact induced voltages and currents for a specific well-characterized system but it only provides the statistical properties of these induced currents and voltages.

Solution Proposed: Apply Characteristic Mode Analysis (CMA) to identify the fundamental modes of the enclosure, current distribution, and the field pattern of each mode. This will allow us to predict the worst-case RF coupling scenarios without the need for lengthy simulations and/or expensive experimental measurements. The proposed approach can predict measurements at a fraction of the cost/time. Moreover, we propose to study RF coupling to realistic UAV wire distributions, experimentally reconstructed, when they are placed inside metallic/dielectric UAV enclosures.

Relevance to OSPRES Grant Objective: Provide general guidelines on how the environment, in this case, the enclosure, affects RF coupling and subsequent electromagnetic absorption to UAV wires and integrated circuits.

Risks, Payoffs, and Challenges: The modes depend mainly on the shape and material of the enclosure. Since UAVs have a wide variety of shapes and material compositions, a library of several UAVs needs to be studied before general quantitative conclusions can be drawn. Challenges can be mitigated by the use of the classification techniques of Machine Learning (ML). That is, different ML techniques will be evoked to detect hidden patterns on how the shape, material composition, and the shape/size location of slots correlate with the field enhancement inside the enclosure.

10.1.2 *Tasks and Milestones / Timeline / Status*

A. Complete the CMA implementation for studying the shielding effectiveness of metallic enclosures. Validate whether CMA can predict the worst-case shielding effectiveness of metallic enclosures as a function of their shapes. / JAN21 / Complete.

   A1. Prepare a manuscript for IEEE AWPL to document the progress done in A. / Ongoing.

B. Progressively build an accurate representation of the UAV wiring system with all of the integrated circuit (ICs) and electronics to test assist the predictions of (c) and the experimental measurement of the actual UAV. / JUL21 / Complete.

C. Address the 2021 UAV's semi-annual review recommendations to study arbitrarily shaped UAV wire distribution. / JUNE21 / Complete.

D. Define the main RF coupling pathways to UAVs, i.e. is RF coupling to the wires/traces the dominant pathway or is it the direct coupling to the electronics, and also quantify the sensitivity of these coupling pathways to load and wire variations. / December 21 / Ongoing.

10.1.3 *Technical Update*

Several prior studies have reported the use of radiating antennas in the payload of a UAV. These radiating antennas are typically used to characterize the radiation characteristics of receiving devices on the ground [1]-[5]. Fig. 10.1.1 shows an example of a UAV carrying an antenna from a study by Paonessa *et al.* [1]. So far, we have used the Equivalent Circuit Approach (ECA) to study RF coupling to the wiring system of the UAV when the source of excitation is a plane wave originating far from the UAV. However, the ECA is not limited to far-field excitation, and it can quantify coupling to UAV from nearby antennas in its payload.

To study RF coupling, we added a 0.16 m long dipole antenna at a separation s = 3.5 cm below the UAV wiring model as shown in Fig. 10.1.2a and calculated the equivalent circuit shown in Fig. 10.1.2b using FEKO. The dipole antenna is a narrow band antenna with a center frequency of ~ 0.87 GHz, as shown in Fig. 10.1.3. The antenna is excited by a constant input voltage of 0.794 V, corresponding to an input power of ~ 6 mW, at 501 different frequencies between 1 MHz and 1.5 GHz. Fig. 10.1.4 shows the open-circuit voltage induced at the Load Under Test (LUT) in the UAV. Even though the antenna is

only operational between 0.833 GHz to 0.914 GHz, significant V_{oc} is induced between 0.419 GHz to 1.5 GHz since the antenna is in the near-field of the UAV, which leads to strong coupling. Therefore, if the antenna is excited by a wideband pulse, input power outside the operation bandwidth of the antenna can couple to the UAV. We also calculated the input impedance, Zin, of the equivalent circuit at the LUT for different separation between the carried dipole antenna and the UAV, as shown in Fig. 10.1.4. The dipole-antenna does not affect the input impedance of the LUT at low frequencies, but it shows a growing effect for frequencies higher than 1 GHz, especially as s decreases i.e. as the dipole antenna moves closer to the UAV. Future reports will quantify coupling to the LUT and other UAV loads due to various antenna excitations and separations s.

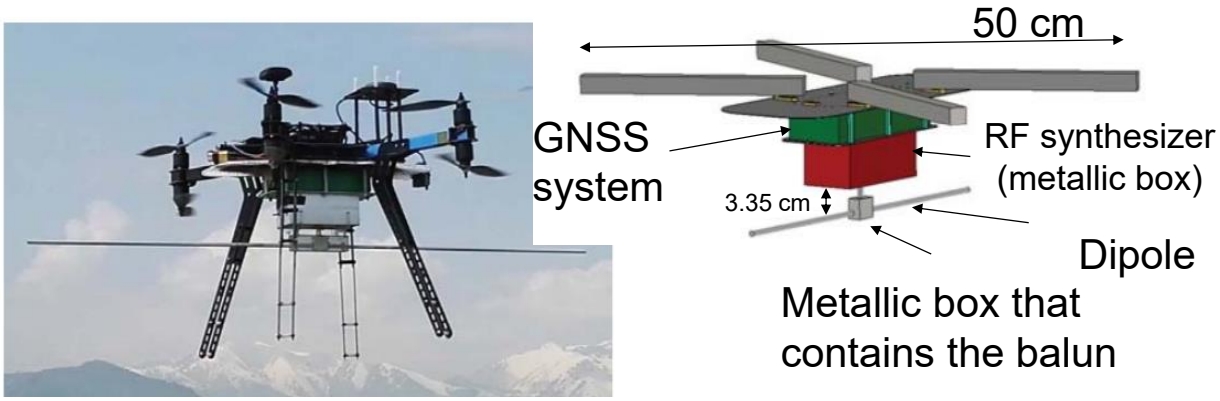


Fig. 10.1.1: Example of a previously reported UAV configuration showing a UAV carrying a dipole antenna [1].

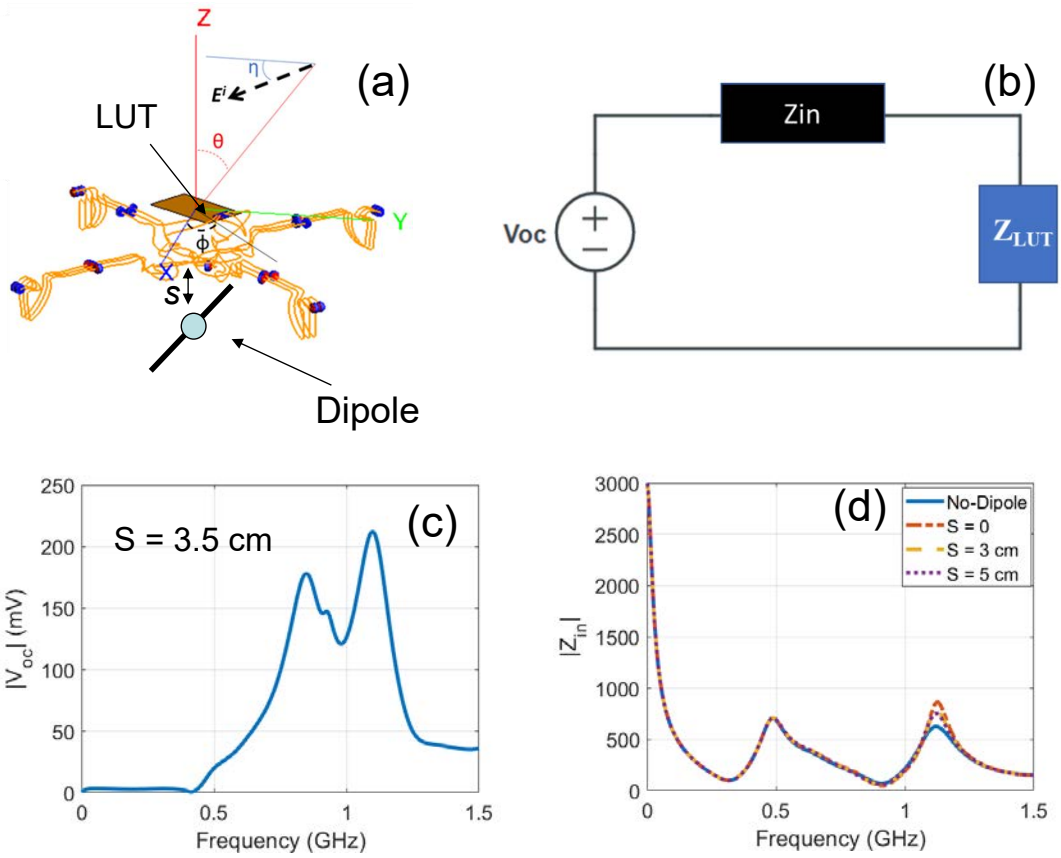


Fig. 10.1.2: (a) The UAV wire model with the dipole added and the Load Under Test (LUT) labelled (b) the equivalent circuit at the LUT, (c) the open circuit voltage at s = 3.5 cm and (d) the input impedance for different s values.

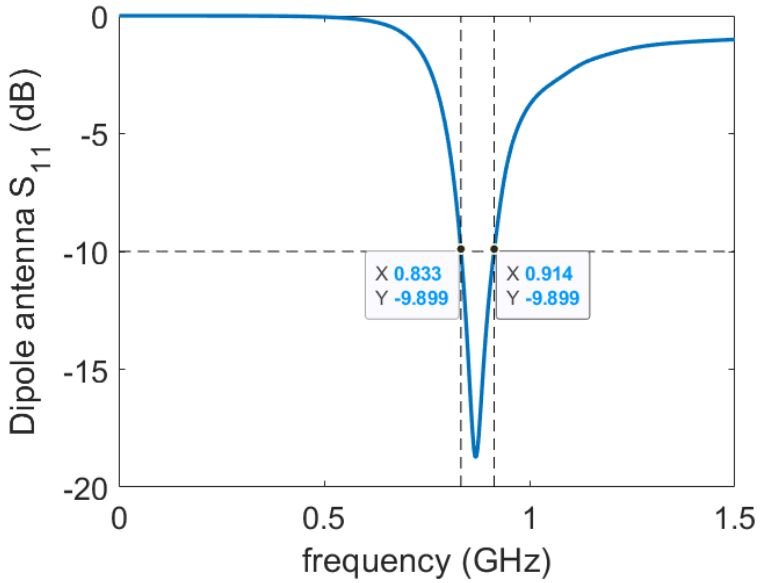


Fig. 10.1.3: Reflection form the dipole antenna showing a center frequency of 0.87 GHz and an operation bandwidth of 0.833 GHz to 0.914 GHz.

References:

[1] F. Paonessa, G. Virone, P. Bolli, G. Addamo, S. Matteoli and O. A. Peverini, "UAV-Based Antenna Measurements: Improvement of the Test Source Frequency Behavior," 2018 IEEE Conference on Antenna Measurements & Applications (CAMA), 2018, pp. 1-3, doi: 10.1109/CAMA.2018.8530506.

[2] G. Virone et al., "Antenna pattern measurements with a flying far-field source (Hexacopter)," 2014 IEEE Conference on Antenna Measurements & Applications (CAMA), 2014, pp. 1-2, doi: 10.1109/CAMA.2014.7003370.

[3] Pupillo, G., Naldi, G., Bianchi, G. et al. Medicina array demonstrator: calibration and radiation pattern characterization using a UAV-mounted radio-frequency source. Exp Astron 39, 405–421 (2015). https://doi.org/10.1007/s10686-015-9456-z

[4] G. Virone et al., "Antenna pattern measurement with UAVs: Modeling of the test source," 2016 10th European Conference on Antennas and Propagation (EuCAP), 2016, pp. 1-3, doi: 10.1109/EuCAP.2016.7481744.

[5] A. Y. Umeyama, J. L. Salazar-Cerreno and C. Fulton, "UAV-Based Antenna Measurements for Polarimetric Weather Radars: Probe Analysis," in IEEE Access, vol. 8, pp. 191862-191874, 2020, doi: 10.1109/ACCESS.2020.3027779.

10.1.4 *Summary of Significant Findings and Mission Impact*

A. A fast full-wave tool that facilitates studying the effect of a metallic enclosure on shielding effectiveness has been developed using CMA.

B. Developed an accurate model for the complete wiring system of an UAV, integrated the model with PECNEC, and validated the implementation with rigorous full-wave simulations.

C. Two Second series equivalent circuit branches/resonance is the best combination for the RLC circuit to accurately represent Zin of the system.

11 UAS Engagement Wargaming & Modeling and Simulation (M&S)

11.1 Fixed-Effector Wargaming Simulation Toolkit Development

(Nolan Petersen and Travis Fields)

11.1.1 *Problem Statement, Approach, and Context*

Primary Problem: Wargaming simulations enable rapid evaluation of different weapon systems and strategies. However, the lack of easy-to-use, high-fidelity software tools makes producing and studying different engagement scenarios (e.g., one friendly system versus five hostile agents) difficult and time-consuming.

Solution Space: We propose to develop a simulation environment using the Unity real-time development platform to offer an easy-to-use, medium-fidelity environment for the purpose of studying different blue vs. red engagement scenarios. Unity is a well-established game development software, with a strong community base for tutorials, training, and software assistance. This makes Unity an ideal solution for a medium-fidelity simulation environment to narrow down optimal fixed effector configurations, which could then be studied further in a higher fidelity environment.

State-of-the-Art (SOTA): Current software tools (e.g., AFSIM) for this purpose are tedious to adapt and/or modify for running different scenarios due to a lack of documentation and support.

Relevance to OSPRES Grant Objective: Wargaming simulations are relevant to the OSPRES Grant Objective because the ability to simulate and benchmark performance of different scenarios, such as different fixed-effector positions, types, and targeting strategies could provide insight into the ideal utilization of HPM-related systems.

Anticipated Outcome(s): The anticipated outcome of development of a wargaming simulation is a medium-fidelity user friendly wargaming simulation tool capable of simulating realistic engagement scenarios with the ability to easily manipulate the scenario and quickly obtain results.

Challenges: Capturing sufficient realism without significantly reducing performance.

Risks: The risk involved with wargaming simulations is the infinite number of scenarios and configurations, making generalizing difficult from within a simulation environment.

11.1.2 *Tasks and Milestones / Timeline / Status*

(A) Reproduction of results obtained from the previously used wargame software Modern Air Power by John Tiller Software, which is no longer in development, using the Unity environment / MAY21 – JUN21 / Completed.

(B) Implementation of radar uncertainty into simulation environment, enabling increased realism to better simulate current targeting capabilities / JUN21 – JUL21 / Completed.

(C) Trade-space study of microwave, tracking, and hostile agent performance to identify key limitations and low-risk, low-cost improvements, enabling increased weapon efficacy / JUL21 – MAR22 / In Progress.

(D) Optimization of current simulation framework to facilitate more quickly obtaining results / SEP21 – OCT21 / Completed.

(E) Implementation of more effector models such as kinetic weapons and radio jammers to better simulate a layered defense / OCT21 – FEB22 / In Progress.

(F) Implementation of electro-optical/infra-red and lidar sensor capabilities into simulation environment, enabling increased realism to better simulate current targeting capabilities / FEB22 – MAR22 / Upcoming.

11.1.3 *Progress Made Since Last Report*

(E) A high-level model for a close-in weapon system (CIWS) type kinetic effector was implemented into the C# library.

11.1.4 *Technical Results*

(E) The current kinetic effector model being used in the C# library was taken from a study on railgun development [1] in which they model a CIWS type of kinetic weapon and compare its performance to that of a proposed railgun to fill its place. In this study, they model the probabilistic nature of a kinetic weapon by using a 2d gaussian probability density function to calculate what they call the single shot hit probability (SSHP). Furthermore, it is assumed that the target is flying directly toward the CIWS boresight and that the projected cross-sectional area of the target is circular with a radius of s. The equation for finding the SSHP is shown in equation (1).

$$SSHP = \int_s \frac{r}{\sigma^2} exp\left(\frac{-r^2}{2\sigma^2}\right) dr \qquad (1)$$

Where σ^2 is the variance of the gaussian distribution and is a function of both the distance of the target as well as the flight time of the projectile. The equation for finding the variance σ^2 is shown in equation (2).

$$\sigma^2 = (R\sigma_{ball})^2 + \left(t_f \sigma_{atm}\right)^2 \qquad (2)$$

Where R is the distance of the target from the CIWS boresight, σ_{ball} is the standard deviation due to ballistic dispersion, t_f is the flight time of the projectile, and σ_{atm} is the standard deviation due to atmospheric dispersion. For values of σ_{ball} and σ_{atm}, they used values of 1 milliradian and 1 m/s, respectively. In short, the SSHP is effectively finding the probability that a projectile will be anywhere within the target's projected area by integrating a 2d gaussian distribution with a mean at the center of the target's cross section and a standard deviation of σ. Because a CIWS type kinetic effector typically shoots in bursts, the SSHP for each shot must then be accumulated and used to find the probability of no successful hits. Then, by taking the complement of the probability of no successful hits, the probability of at least one successful hit can be found (where one or more hits is assumed to be a kill). Once the probability of a hit is greater than or equal to 95%, the target is assumed to have been killed. This model was then implemented into the C# library and checked against data given in the original paper. The scenario used to produce the data is as follows: a target moving at 300 m/s is travelling towards the kinetic effector in a straight-line path and is engaged by the kinetic effector at different ranges

designated as the “open fire range”. Why each open fire range is chosen for each combination of parameters is not stated in the paper and was not deemed important as this was primarily to ensure that the version of the kinetic effector implemented in the C# library was correct, thus the open fire ranges have not been included in the data for simplicity. Furthermore, it should be noted that the authors of the study did not explicitly mention what cross-section radius they used to obtain these results. Due to this, because the targets being studies were anti-ship missiles, a google search was done to find that a typical radius of an anti-ship missile is 0.17 m, which was then used for the cross-section radius. The corresponding data this produced is shown in Figure 11.1.1.

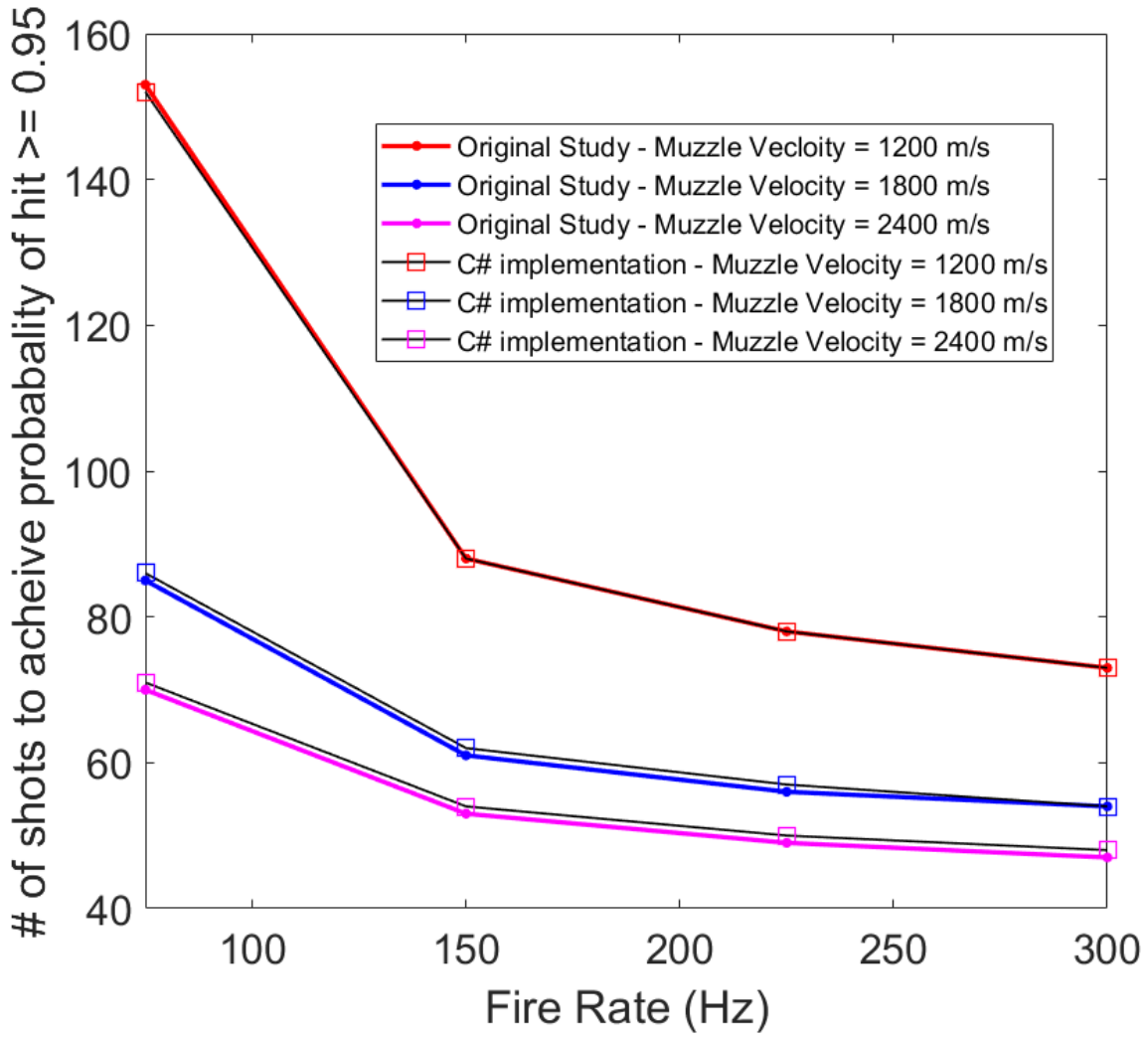


Figure 11.1.1. Comparison of data from the model implemented in the original study [1] and the C# implementation of that model.

From Figure 11.1.1., the C# implementation of the model is very closes to the original, typically using one more shot than the original to achieve a probability of a hit greater than or equal to 0.95. This discrepancy could be due to different step-sizes used in integrating

the SSHP, however, it is most likely due to different cross-section radii being used between studies.

While this treatment gives a good baseline for extremely simple cases where a UAV is flying directly towards the kinetic effector, it is lacking in that it cannot account for anything other than a straight-line path towards the effector and it also cannot account for a single burst hitting multiple UAVs because of the consideration of only one UAV's cross-section at a time. Due to this, work is currently being done to adapt this previous model to account for the aforementioned issues.

11.1.5 *Summary of Significant Finding and Mission Impact*

(A) Reproduction of previous results obtained from Modern Air Power by John Tiller Software was completed in Unity, which provided a framework to implement new features.

(B) Implementation of radar uncertainty into the Unity simulation environment was completed.

(C) A trade-space study of the effect of slew-rate on HPM effectors with and without radar uncertainty and off-boresight effects was performed. This study showed that beyond a threshold slew-rate, additional kills are not possible without decreasing firing delay. It also showed that the performance of energy weapons without off-boresight effects is susceptible to the effects of radar uncertainty, while energy weapons with off-boresight effects may mitigate the effects of radar uncertainty on performance.

A trade-space study around a specific type of high-powered microwave (HPM) effector modeled by the time to effect treatment was performed in both MATLAB and the C# simulation to both compare results and understand the behavior of the C# simulation. This provided insight into possible issues with the C# simulation which will be explored in the future.

The previous comparison between trade-space study results obtained using MATLAB and the C# simulation showed that the C# "float" data type used for storing object positions had an insufficient number of significant figures and was replaced with a more precise "double" data type for more accurate and robust results.

(D) Optimization of the simulation through development of a custom C# library was completed.

(E) A high-level model for a close-in weapon system (CIWS) type kinetic effector was implemented into the C# library.

11.1.6 *References*

[1] J. Gallant, E. Vanderbeke, F. Alouahabi and M. Schneider, "Design Considerations for an Electromagnetic Railgun to be Used Against Antiship Missiles," in IEEE Transactions on Plasma Science, vol. 41, no. 10, pp. 2800-2804, Oct. 2013, doi: 10.1109/TPS.2013.2278779.

12 Feedback

Comment	Response
12/17/2021 – Hoffman Great to see the DSRD advancements and topology studies. Have you got any good guidance from Andy or Michael for their diffusion studies?	**Caruso** Assume you mean Andy Koehler; not sure who Michael is. We haven't heard from either but will reach out to Andy.
12/17/2021 – Hoffman The laser developments and interactions with that community (Gov and Comm) is really great to see and at some point you should almost be reporting that to the laser community forums separate from anything on our work as there could be legitimate benefit.	**Shepard** We disseminated recent results to NRL Code 5600 fiber laser experts Jasbinder Sanghera and Craig Hoffman (with whom we have already met); they again expressed an interest in partnering on the optical power amplifier technology. We will keep you apprised of any collaborative work, comments, or separate funding from the HEL community.
01/05/2022 – anonymous via Hoffman *"Semiconductor Pulse Sharpeners. The p+–p–n profile DSRDs we are testing are structurally identical to SAS. However, the initiation of the impact ionization needed for a SAS at >2 kV/ns input pulse depends on the presence of certain types of defects states. Even in the absence of these defect states, DSRDs are expected to show SAS-like behavior at >5–10 kV/ns input pulse. We have begun testing DSRDs as sub-nanosecond pulse sharpeners using a custom-built test fixture and Megaimpulse PPM-0731 pulse generator (58 kV/ns output); however, no change has been observed in the output so far."* A DSRD is not structurally similar to a SAS device. DSRDs are 4-layer devices, whereas SASs are 3-layer devices, and their doping profiles are not at all consistent with one another. Further, mechanically speaking, a SAS operates exactly the opposite of a DSRD: A DSRD is a current breaker, a SAS is a current shaper (one is an opening switch, the other a closing switch). The theoretical prediction for the ramp rate required to initiate tunneling assisted impact ionization in Si is ~ 2 kV/ns. In practice, this is often demonstrated at ramp rates as low as .5 kV/ns, the dependence of which traces to the smoothness of the pn junction of the device. There is no basis upon which to press for ramp rates > 2 kV/ns in Si.	**Bhattarai** A drift-step recovery diode (DSRD) is a member of the semiconductor opening switch (SOS) family. The working principle (pump–sweep) of DSRDs and SOSs is the same, and many publications use these names interchangeably. Some early articles [1][2] that describe the DSRD action focus on 3 layer (p^+–n–n^+) devices, and there are many others who synonymously use SOS and DSRD for both 3 and 4 layer devices. A semiconductor avalanche sharpener/shaper (SAS) is a name given to different types of diodes that sharpen the pulse by exploiting fast-closing action due to impact ionization. Some refer to these heterostructures as delayed avalanche breakdown diodes or simply delayed breakdown diodes (DBD). SASs can also exist in 3-layer (p+–p–n or p^+–n–n^+) and 4-layer (p^+–p–n–n^+) structures. Thus, both DSRD and SAS can exist in both configurations. Regardless of nomenclature, the devices we refer to here as DSRDs are 3-layer devices (*p*+–*p*–*n*) that are physically identical to SASs. As the commenter points out, the doping profiles of DSRDs and SASs are different. Regarding their function, the commenter is correct in saying that the DSRD works exactly opposite to how a SAS does. But that is true only when the device is operated below the breakdown field. DSRD circuits are designed to maintain that condition. Beyond the breakdown field, there is no physical reason for these devices to not show the delayed impact ionization at high enough field and ramping rate. As we study DSRDs, it is not necessarily a bad idea to use the same diodes in SAS mode, which then allows us to optimize the doping profile for SAS action.

	We believe that determining the electric field and ramp rate at which impact ionization is initiated is a fundamental question. The onset of delayed impact ionization at 0.5–2 kV/ns in silicon diodes (SAS) is only in the presence of the "required defect states," which the Russian scientists call "process-induced (PI) defects," and their claim is that they are observed only in some Russia-made power diodes. In the absence of these defect states, there are not enough "seed" electrons to initiate impact ionization in the depletion region. We have not produced any SAS diodes nor proven that SAS diodes can be made without these PI defect states within the United States (to our knowledge). In the absence of such PI defects, there is still the possibility to ignite impact ionization, and according to some literature, that is achieved only if the ramping rate goes beyond 5–10 kV/ns. The references for these arguments are included in the main body of the report. References [1] I. V. Grekhov, A. F. Kardo-Sysoev, L. S. Kostina, and S. V. Shenderey, "High-power subnanosecond switch," *Electron. Lett.*, vol. 17, no. 12, pp. 422–423, 1981, doi: 10.1049/el:19810293. [2] S. Shinohara, H. Kobayashi, V. Hasegawa, and R. Saito, "High voltage charge-storage diodes and their new applications," *IEEE Int. Symp. Power Semicond. Devices ICs*, pp. 261–264, 1997, doi: 10.1109/ispsd.1997.601488.
01/05/2022 – anonymous via Hoffman *"Sub-Problem 1: TCAD and SPICE models of the DSRD are 40% accurate and must be improved. PSD models have not been developed.* *Sub-Problem 2: Inductive pulser designs are complicated by the DSRD (and PSD) parameter variability. Use TCAD and/or SPICE models to account for variability and improve pulser design."* I have no idea how "40%" is quantifiable. In general, the challenge resides in the limitation of SPICE, which is simply poor at modeling inductive circuits.	**Eifler** Various convergence problems can arise due even to simple diode models as well as inductors. Without more specific problem details, it is hard to determine whether modeling a particular inductive circuit accurately in SPICE is possible. Convergence issues (usually due to unrealistic models or hard sources) can often be solved, and more realistic models of inductors are often used. But inductive circuits can be modeled better in electromagnetic wave simulators than circuit simulators. To what extent SPICE vs EM wave propagation needs to be used to model the pulsers has not been resolved. I have not currently had any such issue in SPICE or TCAD simulations of failing to converge. I should say in larger pulser designs there have been some convergence issues that are not as easy to resolve in LTSPICE. We have removed the 40% reference. A lack of good MOSFET and driver models in TCAD have

	prevented improving accuracy further. The old inaccurate DSRD LTSPICE model is not based on sweeping pulser inputs such as trigger duration and observing the accuracy of the model and comparing to experiment which more fully characterizes the model accuracy. Further accuracy improvements are expected. More recent accuracy has been 10-50% accurate depending on what diode model was used or whether peak voltage and risetime were assessed.
01/05/2022 – anonymous via Hoffman *"Deficiency in the SOTA: A lack of accurate TCAD and SPICE models make design of DSRD and DSRD-based inductive pulser circuit topologies (with or without PSDs) difficult to the level of tens of MW of peak power while maintaining ns-order risetime (or sharpened 100 ps-order). In addition, DSRD (and PSD) fabrication variabilities further complicate pulser design."* Also not true. As I've mentioned to you previously, scaling to high power at sub-ns leading edge rise times is challenging owing to the lack of maturity of our pulse sharpening capabilities at higher voltage. This is a device limitation, not a modeling limitation.	**Eifler** I'm more on the device modeling simulation side than working experimentally in pulsed power. This comments suggests fundamental experimental limitations are known and then obviously modeling is not the limitation (so the response to the SOTA is more about experimental limits not modeling limits). Not clear what device is limiting what. We may not mean the diode is the limitation here, that's not been said. Clearly any design methodology relies on some theoretical assessment based on experimental data. This is my point. The comment doesn't assess modeling so much as experimental knowledge. In other words, we might design based on simulations but experimental testing will verify if any of the theory is correct. Somewhat chicken and egg problem here.
01/05/2022 – anonymous via Hoffman *"Primary Problem: DSRDs have not increased in performance due to deep diffusion manufacturing since the 60's. Their voltage-to-risetime, dV/dt remains on the order of 10^{12} V/s. To achieve the 10^{13} V/s (10 kV/ns) voltage-to-risetime required by an all-solid-state HPM pulse generator in support of the Naval afloat mission, improving DSRD manufacturing techniques is critical."* There are problems with this statement....	**Usenko** The comment is not specific. I would be glad to give my opinion if the commenter can describe the problems they see in more detail.
01/05/2022 – anonymous via Hoffman *"Sub-Problem 2 – Stacking of DSRD dies: The SOTA is based on soldering of diode dies into a stack, which limits the stack lifetime to below 10^{12} pulses. Also, the SOTA did not apply the methodology of stacking wafers first, then cutting into dies. Switching to wafer level stacking will decrease the number of stacking operations by more than 100x."*	**Usenko** I agree there are several different stacking techniques beyond soldering, and some are better than soldering. To be brief, I have only mentioned soldering here, which may have led to some misunderstanding. I would like to emphasize, however, that my main my point is that the SOTA is based on cutting wafers into dies first, then stacking dies, while we stack wafers first, then cut wafer stacks into already stacked dies. The

Also not true. We've made great advances in thermal compression bonding.	stacking of dies is very labor intensive, and we achieve much higher throughput by stacking on the wafer level.
01/05/2022 – anonymous via Hoffman *"State-of-the-Art (SOTA): In a recently published paper (2019),[1] the Russian St. Petersburg team at the Ioffe institute reported achieving a peak current density of 5 kA/cm^2 with a rise time of the output pulse front of ~2.3 ns, and a peak voltage across the load of 900 V (i.e., the peak switching power is 4.5×10^6 W/cm2). The St. Petersburg team utilized deep diffusion technology. A competing team at Ekaterinburg, Russia [2] reports similar pulse performance. Both teams use outdated deep diffusion technology. As one can see, there has not been any significant improvement in DSRD pulse performance since the pioneering work done in 1960 [3]"* Once again, this is just wrong.	**Usenko** This comment is not specific, so I can only guess at what the commenter means. I can assume they may be suggesting that there has been some improvement in DSRD pulse performance since 1960. I agree, and my wording here is oversimplifying (for the sake of brevity). I agree that there has been some improvement in pulse performance, however this has been limited as the fabrication technique has remained the same, relying on a diffusion-based process flow with minimal optimization. A 60-year history has proven that improvement in dV/dt was way below even an order of magnitude. I believe this justifies my claim "no significant improvement."
01/05/2022 – anonymous via Hoffman *"Deficiency in the SOTA: First, no DSRDs have been manufactured using epitaxy technology with doping profile optimization. Second, no DSRD processing method exists that integrates side passivation with silicon dioxide. Finally, an acceptable DSRD stacking process has yet to be developed."* Absolutely inaccurate. The Soreq nuclear research group out of Israel, in collaboration with the RAS, has been fabricating epitaxial grown DSRDs for years. All available information thus far suggests these device perform worse than long-diffusion devices.	**Usenko** Soreq did epitaxy with a flat doping profile, which does not fit for DSRD. It results in what Grekhov, Rukin, and others call "soft" diodes, whereas DSRDs should be "hard" diodes. A diffusion profile makes the diode "harder," but not optimally "hardest". We go further and have determined the "hardest" doping profile by simulation, subsequently copying that ideal profile into silicon via epitaxy. To do this, we had to upgrade our epitaxy tool with a doping gas flow controller. I believe that drawing the conclusion based on the Soreq result that: "diffusion is better than epitaxy for DSRD" is incorrect, and that the correct interpretation is rather that Soreq did not use epitaxy capabilities for DSRD properly, and therefore obtained diodes even worse than diffusion-based ones.

13 Program Management

13.1 Issues

i. Scope – No issues
ii. Budget – 12-month NCTE submitted/pending
iii. Schedule – No issues

13.2 Interactions with Others

Agency/Org	Performer	Project Name	Purpose of Research/ Collaboration

13.3 Major Procurement Actions

13.4 Travel

Destination	Purpose	Attendees	Estimated Costs

13.5 Pending or Upcoming Public Release Requests

14 Appendix A: Academic and IP Output

14.1 Students Graduated

Name	Degree	Currently
Al-Shaikhli, Waleed Azad, Wasekul	MS Spring 19 PhD Summer 21	Kansas City National Security Campus, Honeywell Applied Materials, Sunnyvale, CA
Berg, Jordan	MS Spring 21	MRI Global
Bissen, Bear	MS Spring 19	Kansas City National Security Campus, Honeywell
Floyd, Dennis	BS	Naval Air Warfare Center Weapons Division
Hanif, Abu	PhD Spring 21	UMKC/MIDE (Postdoc)
Harmon, Aaron	BS	Missouri University of Science & Technology
Harp, Joshua	MS	UMKC/MIDE (Senior Engineer)
Hauptman, Cash	BS Spring 18	University of Nebraska-Lincoln
Klappa, Paul	MS Spring 21	
Labrada, Dario	BS Spring 20	Honeywell Aerospace, Florida
Lancaster, John	MS Spring 17	Lawrence Livermore National Laboratory
Renzelman, Jeff	MS Spring 18	Kansas City National Security Campus, Honeywell
Roy, Sourov	PhD Spring21	
Wagner, Adam	MS Fall 20	Kansas City National Security Campus, Honeywell
Xia, Shengxuan	BS	Missouri University of Science & Technology

14.2 Journal Publications

14.2.1 *In Preparation*

[1] N. Gardner, K. C. Durbhakula, and A. N. Caruso, “UHF and L-Band Frequency Generation at MW Peak Power using Diode-based Nonlinear Transmission Lines as Pulse Forming Networks,” *Transactions on Plasma Science*, In Preparation, **2021**.

[2] N. Gardner, K. C. Durbhakula, and A. N. Caruso, “Electrically Tunable Diode-based Nonlinear Transmission Line,” *TBD*, In Preparation, **2021**.

[3] N. Gardner, A. N. Caruso, K. C. Durbhakula and P. Doynov, “Diode-Based Non-Linear Transmission Line Design Considerations,” *Journal of Applied Physics*, In Preparation, **2021**.

[4] B. Barman, D. Chatterjee, and A. N. Caruso, “Tradespace Analysis of Wideband, Electrically Small Microstrip Patch Antenna Elements for Phased Array Applications,” *IEEE Antennas and Propagation Magazine,* In preparation, **2021**.

[5] S. Xia, J. Hunter, A. Harmon, M. Hamdalla, A. Hassan, V. Khilkevich, D. Beetner, “Simulation Driven Statistical Analysis of the Electro-magnetic Coupling to Microstriplines,” *IEEE Transactions on Electromagnetic Compatibility*, In Preparation, **2020**.

[6] M. Hamdalla, V. Khilkevich, D. G. Beetner, A. N. Caruso, A. M. Hassan, “Characteristic Mode Analysis Justification of the Stochastic Electromagnetic Field

Coupling to Randomly Shaped Wires," *IEEE Transactions on Electromagnetic Compatibility*, In Preparation, **2020**.

14.2.2 *Submitted / Under Revision*

[7] B. Barman, K. C. Durbhakula, D. Chatterjee, and A. N. Caruso, "Comparison of Machine Learning Algorithms for Bandwidth Enhancement of a Coaxial Probe-fed Microstrip Patch Antenna," *Applied Computational Electromagnetics Society (ACES)*, Submitted, **2021**.

[8] B. K. Lau, M. Capek, and A. M. Hassan, "Characteristic Modes–Progress, Overview, and Future Perspectives," *IEEE Antennas and Propagation Magazine*, Submitted, **2021**.

[9] K. Alsultan, M. Z. M. Hamdalla, S. Dey, P. Rao, and A. M. Hassan, "Scalable and Fast Characteristic Mode Analysis Implementation Using a Hybrid CPU/GPU Platform," *ACES*, Submitted, **2021**.

[10] M. Z. M. Hamdalla, B. Bissen, J. Hunter, L. Yuanzhuo, V. Khilkevich, D. G. Beetner, A. N. Caruso, and A. M. Hassan, "Prediction of Experimental Electromagnetic Coupling to a UAV Model Using Characteristic Mode Analysis," *IEEE Access*, Submitted, **2021**.

[11] W. Azad, F. Khan, and A. N. Caruso, "A Scalable Multilevel-Modular 10 kV Silicon Carbide MOSFET Module Featuring Custom Isolated Gate Driver Circuit Combined with Coupling and Snubber Circuits," *IEEE Transactions on Power Electronics*, Submitted, **2021.**

[12] John Keerthi Paul Bhamidipati, Eliot R. Myers, Adam M. Conway, Lars F. Voss, and Anthony N. Caruso, "Figure of Merit Development for Linear-Mode Photoconductive Solid-State Switches," *IEEE Transactions on Electronic Devices*, Under Revision, **2020**.

14.2.3 *Published / In Press*

[13] M. Z. M. Hamdalla, B. Bissen, J. Hunter, Y. Liu, V. Khilkevich, D. G. Beetner, A. N. Caruso, and A. M. Hassan, "Prediction of Experimental Electromagnetic Coupling to a UAV Model Using Characteristic Mode Analysis," *IEEE Access*, In Press, **2021**.

[14] J. N. Berg, R. C. Allen, and S. Sobhansarbandi. "A Novel Method of Cooling a Semiconductor Device through a Jet Impingement Thermal Management System: CFD Modeling and Experimental Evaluation." *International Journal of Thermal Sciences*, 172, 107254, **Feb 2022** [doi].

[15] W. Azad, F. Khan, and A. N. Caruso, "A Medium Power, Self-Sustaining, Configurable RF Pulse Generation Circuit Using a Nonlinear Transmission Line and Power Amplifier in a Closed Loop Configuration, *IEEE Transactions on Plasma Science*, vol. 49, no. 7, pp. 2183–2194, **July 2021** [doi].

[16] S. Roy, W. Azad, S. Baidya and F. Khan, "A Comprehensive Review on Rectifiers, Linear Regulators and Switched-Mode Power Processing Techniques for Biomedical Sensors and Implants utilizing In-body Energy Harvesting and External

Power Delivery," *IEEE Transactions on Power Electronics*, vol. 36, no. 11, pp. 12721–12745, **Nov 2021** [doi].

[17] K. C. Durbhakula, D. Chatterjee, and A. M. Hassan, "An Efficient Algorithm for Locating TE and TM Poles for a Class of Multiscale Inhomogeneous Media Problems," *IEEE Journal on Multiscale and Multiphysics Computational Techniques*, vol. 4, no. 1, pp. 364–373, **2019** [doi].

14.3 Conference Publications

14.3.1 *Submitted / Accepted*

[1] S. R. Shepard and H. A. Thompson, "Self-focusing in Guided and Un-guided Media," submitted to the *2021 OSA Nonlinear Optics Topical Meeting, Virtual Event*, August 9-13, 2021.

14.3.2 *Presented*

[2] B. Barman, D. Chatterjee and A. N. Caruso, "Probe-location Optimization in a Wideband Microstrip Patch Antenna using Genetic Algorithm, Particle Swarm and Nelder-Mead Optimization Methods," *2021 International Applied Computational Electromagnetics Society Symposium (ACES)*, 2021, pp. 1-3 [doi].

[3] W. Azad, S. Roy, and F. Khan, "A Single Gate Driver-based Four-stage High-voltage SiC Switch Having Dynamic Voltage Balancing Capability," *2021 IEEE Applied Power Electronics Conference and Exposition* (APEC), Phoenix, AZ, USA, June 9-12, 2021.

[4] W. Azad, S. Roy, F. Khan and A. N. Caruso, "A Multilevel-Modular 10 kV Silicon Carbide MOSFET Module using Custom High-Voltage Isolated Gate Driver, Coupling, and Snubber Circuits," *2021 IEEE Kansas Power and Energy Conference* (KPEC), Manhattan, KS, USA, April 19-20, 2021 [doi].

[5] T. Layman, T. D. Fields, and O. A. Yakimenko, "Evaluation of Proportional Navigation for Multirotor Pursuit," AIAA SciTech Forum, Virtual Event, January 11-21, 2021 [doi].

[6] P. J. Klappa, and T. D. Fields, "Assessment of Fixed-Wing UAV System Identification Models during Actuator and Payload Drop Failures," AIAA Atmospheric Flight Mechanics Conference, Virtual Event, January 11-21, 2021 [doi].

[7] J. Hunter, S. Xia, A. Harmon, A. M. Hassan, V. Khilkevich, and D. Beetner, "Modeling and Statistical Characterization of Electromagnetic Coupling to Electronic Devices," *IEEE International Symposium on Antennas and Propagation and NSRM USNC-URSI National Radio Science Meeting*, Boulder, CO, January 4-9, 2021 [doi].

[8] B. Barman, K. C. Durbhakula, B. Bissen, D. Chatterjee, and A. N. Caruso, "Performance Optimization of a Microstrip Patch Antenna using Characteristic Mode and D/Q Analysis," *2020 XXXIIIrd General Assembly and Scientific Symposium of*

the International Union of Radio Science, Rome, Italy (online conference), Aug 29-Sept 5, 2020, pp. 1-4 [doi].

[9] J. Berg, and S. Sobhansarbandi. “CFD Modeling of Thermal Management Systems for a Silicon Semiconductor Switch.” *ASME 2020 Heat Transfer Summer Conference collocated with the ASME 2020 Fluids Engineering Division Summer Meeting and the ASME 2020 18th International Conference on Nanochannels, Microchannels, and Minichannels*, Virtual, July 13–15, 2020, American Society of Mechanical Engineers Digital Collection [doi].

[10] B. Barman, D. Chatterjee, and A. N. Caruso, “Performance Optimization of Electrically Small Microstrip Patch Antennas on Finite Ground Planes,” 2020 *IEEE International Symposium on Antennas and Propagation and North American Radio Science Meeting*, Montreal, Quebec, Canada, July 5-10, 2020, pp. 1–2 (online conference) [doi].

[11] M. Hamdalla, B. Bissen, A. N. Caruso, and A. M. Hassan, “Experimental Validations of Characteristic Mode Analysis Predictions Using GTEM Measurements,” *IEEE International Symposium on Antennas and Propagation and USNC-URSI Radio Science Meeting,* Montréal, Québec, Canada, July 5-10, 2020 [doi].

[12] K. Alsultan, P. Rao, A. N. Caruso, and A. M. Hassan, “Scalable Characteristic Mode Analysis: Requirements and Challenges (White Paper),” *Large Scale Networking (LSN) Workshop on Huge Data: A Computing, Networking and Distributed Systems Perspective Sponsored by NSF*, Chicago, IL, April 13-14, 2020.

[13] M. Hamdalla, A. N. Caruso, and A. M. Hassan, “Predicting Electromagnetic Interference to a Terminated Wire Using Characteristic Mode Analysis,” *Proceedings of the Annual Review of Progress in Applied Computational Electromagnetics (ACES)*, Monterey, CA, March 22-26, 2020. [doi]

[14] W. Azad, F. Khan, and A. Caruso, "Self-sustaining High-power RF Signal Generation Using LDMOS Based Power Amplifier and Nonlinear Transmission Line," *2020 IEEE Applied Power Electronics Conference and Exposition (APEC)*, New Orleans, LA, USA, March 15-19 2020, pp. 3567-3572 [doi].

[15] A. Hanif, W. Azad, and F. Khan, "Detection of Bond Wire Lift Off in IGBT Power Modules Using Ultrasound Resonators," *2020 IEEE Applied Power Electronics Conference and Exposition (APEC)*, New Orleans, LA, USA, March 15-19 2020, pp. 345-350 [doi].

[16] B. Barman, D. Chatterjee, and A. N. Caruso, “Some Investigations into Mutual Coupling Analysis for Trade Space Studies of Linear Arrays,” *2019 IEEE International Symposium on Phased Array Systems and Technology (PAST)*, Waltham, MA, October 2019, pp. 1-8 [doi].

[17] B. Barman, D. Chatterjee, and A. N. Caruso, “Characteristic Mode Analysis of a straight and an L-probe fed Microstrip Patch,” *2019 IEEE Indian Conference on Antennas and Propogation (InCAP)*, Ahmedabad, India, Dec 2019, pp. 1-3 [doi].

[18] M. Hamdalla, A. N. Caruso, and A. M. Hassan, "Characteristic Mode Analysis of the Effect of the UAV Frame Material on Coupling and Interference," *IEEE International*

Symposium on Antennas and Propagation and USNC-URSI Radio Science Meeting at Atlanta (2 pages), Georgia, USA, July 7-12, 2019 [doi].

[19] M. Hamdalla, J. Hunter, Y. Liu, V. Khilkevich, D. Beetner, A. Caruso, and A. M. Hassan, "Electromagnetic Interference of Unmanned Aerial Vehicles: A Characteristic Mode Analysis Approach," *IEEE International Symposium on Antennas and Propagation and USNC-URSI Radio Science Meeting at Atlanta (2 pages)*, Georgia, USA, July 7-12, 2019 [doi].

[20] K. C. Durbhakula, J. Lancaster, A. M. Hassan, D. Chatterjee, A. N. Caruso, J. D. Hunter, Y. Liu, D. Beetner, and V. Khilkevich, "Electromagnetic Coupling Analysis of Printed Circuit Board Traces using Characteristic Mode Analysis," *IEEE International Symposium on Antennas and Propagation and USNC-URSI Radio Science Meeting (2 pages)*, Atlanta, Georgia, USA, July 7-12 2019 [doi].

[21] K. C. Durbhakula, D. Chatterjee, and A. M. Hassan, "On the Location of Transverse Electric Surface Wave Poles for Electrically Thick Substrates," Proceedings of the *IEEE Antennas and Propagation International Symposium and National Radio Science Meeting*, Atlanta, Georgia, USA, July 7-12, 2019 [doi].

[22] W. Azad and F. Khan, "Sustaining High-power RF Signal Generation in a Positive Feedback Network," *2019 IEEE Pulsed Power and Plasma Science Conference (PPPS)*, Orlando, FL, USA, June 23-28 2019.

[23] K. Alsultan, P. Rao, A. N. Caruso, and A. M. Hassan, "Scalable characteristic mode analysis using big data techniques," *International Symposium on Electromagnetic Theory (EMTS 2019)*, San Diego, CA, USA, May 27-31, 2019.

[24] M. Hamdalla, W. Al-Shaikhli, J. Lancaster, J. D. Hunter, L. Yuanzhuo, V. Khilkevich, D. G. Beetner, A. N. Caruso, and A. M. Hassan, "Characteristic Mode Analysis of Electromagnetic Coupling to Wires with Realistic Shapes," *International Symposium on Electromagnetic Theory (EMTS 2019)*, San Diego, CA, USA, May 27-31, 2019.

[25] K. C. Durbhakula, D. Chatterjee, and A. M. Hassan, "Location of Surface Wave Poles in Sommerfeld Integrals: A Mittag-Leffler Expansion Approach," *Proceedings of the URSI-B International Symposium on Electromagnetic Theory*, URSI Commission, San Diego, USA, May 2019 [doi].

[26] K. C. Durbhakula, D. Chatterjee and A. M. Hassan, "Analytical Evaluation of Sommerfeld Integral Tails Present in Two-layered Media Green's Functions," *Proceedings of the Indian Conference on Antennas and Propagation* (InCAP), Hyderabad, India, December 2018 [doi].

[27] D. Beetner, V. Khilkevich, A. M. Hassan, J. Hunter, Y. Liu, and D. Floyd, "Characterization of the Electromagnetic Coupling to UAVs," *DE Systems Symposium*, September 24-27, 2018

[28] C. Hartshorn, K. Durbhakula, D. Welty, D. Chatterjee, J. Lancaster, A. M. Hassan, and A. N. Caruso, "Crosstalk and Coupling to Printed Circuit Board Metallic Traces with Arbitrary Shapes," *Proceedings of the AMEREM 2018 Conference*, Santa Barbra, CA, Aug 27-31, 2018.

[29] M. Hamdalla, J. Roacho-Valles, J. Hunter, D. Beetner, A. M. Hassan, and A. N. Caruso, "Electromagnetic Analysis of Unmanned Aerial Vehicles Using

Characteristic Mode Analysis," *Proceedings of the AMEREM 2018 Conference*, Santa Barbra, CA, Aug 27-31, 2018.

[30] C. Hartshorn, M. Hamdalla, J. Lancaster, A. M. Hassan, and A. N. Caruso, "Electromagnetic Vulnerability of Wires with Arbitrary Shape," *Proceedings of the AMEREM 2018 Conference*, Santa Barbra, CA, Aug 27-31, 2018.

[31] K. C. Durbhakula, D. Chatterjee, A. M. Hassan, and M. S. Kluskens, "Studies on Numerical Evaluation of Sommerfeld Integrals for Multilayer Topologies," *IEEE Antennas and Propagation International Symposium and National Radio Science Meeting*, Boston, Mass., USA, July 7-12, 2018.

[32] J. Lancaster, D. Chatterjee, and A. N. Caruso, "Some Investigations into the Dispersion Characteristics of Localized Bessel Beams," published in the *IEEE Antennas and Propagation International Symposium and National Radio Science Meeting*, Boston, Mass., USA, July 7-12, 2018 (1 page URSI Abstract).

[33] M. Hamdalla, A. M. Hassan, and A. N. Caruso "Characteristic Mode Analysis of Unmanned Aerial Vehicles with Realistic Shapes and Material Composition," *IEEE International Symposium on Antennas and Propagation and USNC-URSI Radio Science Meeting,* Boston, MA, July 8-13, 2018.

[34] W. Azad, S. Roy, A. S. Imtiaz, and F. Khan, "Microelectromechanical System (MEMS) Resonator: A New Element in Power Converter Circuits Featuring Reduced EMI," *2018 International Power Electronics Conference (IPEC-Niigata 2018-ECCE Asia)*, Niigata, May 20-24, 2018, pp. 2416-2420 [doi].

[35] J. Hunter, Y. Liu, D. Floyd, A. Hassan, V. Khilkevich, and D. Beetner, "Characterization of the Electromagnetic Coupling to UAVs," *Annual Directed Energy Science and Technology Symposium*, Feb 26-March 2, 2018.

14.4 Conference Presentations

14.4.1 *Submitted / Accepted*

[1] S. Bellinger, A. Caruso, A. Usenko, "Stacked Diodes for Pulsed Power Applications," GOMACTech-22, Miami, FL, March 21–24 2022 (submitted, oral).

[2] S. Bellinger, A. Caruso, A. Usenko, "New Paradigm on Making Semiconductor Opening Switches for Pulsed Power," 2021 23rd IEEE Pulsed Power Conference, Denver, CO, Dec. 12–16, 2021 (accepted, oral).

Directed Energy Professional Society, Directed Energy Systems Symposium, Washington DC, October 25-29 2021 (submitted):

[3] B. Barman, D. Chatterjee, A. Caruso, and K. Durbhakula, "Tradespace Analysis of a Phased Array of Microstrip Patch Electrically Small Antennas (ESAs)" (Poster)

[4] J. N. Berg, R. C. Allen, and S. Sobhansarbandi, "A Novel Method of Cooling a Semiconductor Device through a Jet Impingement Thermal Management System: CFD Modeling and Experimental Evaluation" (Poster)

[5] J. N. Berg, R. C. Allen, and S. Sobhansarbandi, “Heat Transfer Enhancement of a Jet Impingement Thermal Management System: A Comparison of Various Nanofluid Mixtures” (Poster)

[6] J. Bhamidipati, M. Paquette, R. Allen, and A. Caruso, “Photoconductive Semiconductor Switch Enabled Multi-Stage Optical Source Driver” (Poster)

[7] G. Bhattarai, J. Eifler, S. Roy, M. Hyde, J. Bhamidipati, A. Usenko, M. Pederson, M. Paquette, A. Caruso, S. Bellinger, L. Voss, and R. Allen, “All Solid-State High-Power Pulse Sharpeners” (Poster)

[8] S. Brasel, K. Norris, R. Allen, A. Caruso, and K. Durbhakula, “Efforts to Reduce Physical Aperture Area of Ultra-Wideband Arrays” (Poster)

[9] A Caruso, “ONR Short Pulse Research and Evaluation for c-sUAV: Supporting and Sub-Programs Overview” (Oral)

[10] J. Clark, R. C. Allen, and S. Sobhansarbandi, “Ultra-Compact Integrated Cooling System Development” (Poster)

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[12] N. Gardner, M. Paquette, and A. Caruso, “Diode-Based Nonlinear Transmission Lines Capable of GHz Frequency Generation at Single MW Peak Powers” (Poster)

[13] M. Hamdalla, A. Caruso, and A. Hassan, “The Shielding Effectiveness of UAV Frames to External RF Interference” (Poster)

[14] M. Hamdalla, A. Caruso, and A. Hassan, “A Predictive-Package for Electromagnetic Coupling to Nonlinear-Electronics using Equivalent-Circuits and Characteristic-Modes (PECNEC)” (Poster)

[15] M. Hyde, J. Eifler, S. Roy, G. Bhattarai, A. Usenko, M. Paquette, A. Caruso, S. Bellinger, L. Voss, and R. Allen, “Development of an Evaluation Network for Drift Step Recovered Diodes through and Augmented Design of Experiment” (Poster)

[16] S. Indharapu, A. Caruso, and K. Durbhakula, “Machine Learning Based Ultra-Wideband Antenna Array Optimization and Prediction” (Poster)

[17] F. Khan, W. Azad, and A. Caruso, “A Scalable Multilevel-Modular 10 kV Silicon Carbide MOSFET Architecture for Pulsed Power Applications” (Poser)

[18] D. F. Noor, J. Eifler, M. Hyde, G. Bhattarai, S. Roy, J. Bhamidipati, A. Usenko, M. Pederson, M. Paquette, A. Caruso, S. Bellinger, L. Voss, and R. Allen, “DSRD-IES Pulsed-Power Generator Topology Study Using Machine-Learning-Based Feature Selection Optimization and Predictive Learning” (Poster)

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[20] S. Shepard and A. Caruso, “Tubular Core Optical Power Amplifier” (Poster)

[21] H. Thompson, M. Paquette, and A. Caruso, “Minimizing On-State Resistance in GaN:X Photoconductive Semiconductor Switches (PCSSs) for Direct Modulation (Poster)

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[25] J. Hunter, S. Xia, A. Harmon, A. Hassan, V. Khilkevich, and D. Beetner, “Simulation-Driven Statistical Characterization of Electromagnetic Coupling to UAVS,” *Annual Directed Energy Science and Technology Symposium*, March 2020 (abstract appeared, but talk cancelled due to pandemic).

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[26] William Spaeth, Wideband Parallel Plate to Coaxial Cable Taper

[27] Stefan Wagner, Quickly Determining Minimum HPC Source Requirements Using Binary Search

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[28] Cash Hauptmann, Reduced Recovery Time in SiPCSS Photoconductive Switches

[29] Eliot Myers, Picosecond High Power Switching Technologies

[30] Heather Thompson, GaN Optimization for Use in Photoconductive Switch

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[28] B. Barman, D. Chatterjee, and A. N. Caruso, “Analytical Models for L-Probe fed Microstrip Antennas,” *Proceedings of the IEEE Antennas and Propagation International Symposium and National Radio Science Meeting*, Atlanta, Georgia, USA, July 7-12, 2019 (1 page URSI Abstract).

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[29] Ryan Butler, Mechanical Challenges of Modular Photoconductive Semiconductor Based HPM Sources

[30] Steve Young, Two-Dimensional Optoelectronic Pulsed Power Switches: Initial Effort

[31] Adam Wagner, Rapid Cost Effective RF Component Prototyping Using 3D Printers

[32] Heather Thompson, Cost to benefit analysis of GaN for Photoconductive Semiconductor Switches

[33] Colby Landwehr, Low Leakage Electroluminescence For Improving SiPCSS Hold Off

[34] James Kovarik, Some Investigations Into Applications Of Electrically Small Antennas As Phased Array Elements

[35] Spencer Fry, Maximizing SiPCSS Efficiency For HPM Sources

[36] Deb Chatterjee, Studies On Antenna Characterization And Propagation Of High Power Pulsed Electromagnetic Waves With Minimal Dispersion

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[37] Jeff Scully, ElectroLuminescence Studies of Silicon Based Photo-Switches

[38] Cash Hauptmann, Thermal Anlaysis of a PCSS through TCAD Simulation

[39] Nicholas Flippin, Fast Rise Time Switches: Drift Step Recovery Diode

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[3] Wasekul Azad, “Development of Pulsed Power Sources Using Self-Sustaining Nonlinear Transmission Lines and High-Voltage Solid-State Switches,” PhD Dissertation in Electrical Engineering, **2021** [mospace].

[4] Paul Klappa, “Implementation and Assessment of State Estimation Algorithms in Simulation and Real-World Applications,” MS Thesis in Mechanical Engineering, **2021** [mospace].

14.6 IP Disclosures Filed

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[7] Doynov, “Scalable Modular System for High-power Microwaves Generation,” 20UMK010, 19APR2020.

[8] Doynov, “Pulse Differential High-power Microwave Generation,” 19UMK007, 02JAN2019.

[9] Doynov, “Non-linear Network Topologies with Reutilized DC and Low-frequency Signal,” 19UMK008, 28DEC2018.

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14.7 Provisional Patents Filed

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[2] S. Bellinger, A. Caruso, A. Usenko, “Diode and Method of Making the Same” US Provisional Patent Application 63/216,550, filed June 30, 2021.

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14.8 Non-Provisional Patents Filed

None to date

15 Appendix B: A Scalable Multilevel-Modular 10 kV Silicon Carbide MOSFET Architecture for Pulsed Power Applications

(Faisal Khan)

15.1 Executive Summary

Within the scope of this project, the MIDE team has designed and developed multiple versions of a custom HV switch that can function as an inexpensive alternative to the commercial BEHLKE switches in terms of performance, cost and availability. To this end, the team has developed a modular series-connected SiC MOSFET architecture and fabricated an HV switch based on this topology powered by a custom isolated gate driver and precision voltage balancing in the 10-kV and 1-kV/ns class. The proposed voltage balancing method achieves <1.1% voltage mismatch under steady-state and switching transitions. Series connection of MOSFETs can mask the underlying limitation of voltage blocking capability of a single device and potentially attain ultra-high voltage blocking capability. Each module of the proposed HV switch consists of four series-connected 1.7 kV rated SiC MOSFETs, yielding a breakdown voltage of 6.8 kV, and driven by a single custom 10 kV rated isolated gate driver. The proposed HV switch consists of two identical modules, thereby rated for a theoretical voltage blocking limit of 13.6 kV. One gate driver per module, a limited number of passive components (e.g., coupling capacitors, resistors, etc.) per module lead to low-cost fabrication and simpler operation of this HV switch. The modularity of the proposed HV switch introduces a unique capability of scaling up the voltage rating by stacking modules to meet potential application requirements without a complete design overhaul. Simulation and experimental results demonstrate excellent voltage balancing among the individual MOSFETs of each module during switching transients and steady states. A maximum voltage imbalance of <80 V was recorded among the individual MOSFETs in the HV switch at a supply voltage of 6 kV and a switching frequency of 15 kHz during the first run. The switch has been eventually tested at 10 kV and 1 kHz switching frequency to test the voltage withstanding capability.

15.2 Objective

Primary Problem: Commercially available high-voltage solid-state switches made by BEHLKE are the best in SWaP-cooling, but are expensive, have long lead times (2–3 months), and are made outside of the US. For the Navy afloat mission to be successful, we need a sustainable supply of US-manufactured switches at a much lower cost.

Solution Space: Design and demonstrate modular high-voltage (~10 kV) and fast (repetition frequency = 100 kHz) solid-state switches using a combination of series- and parallel-connected commercially available inexpensive discrete MOSFETs and custom high-voltage (~10 kV) isolated gate drivers.

Sub-Problem: Voltage balancing among the series-connected MOSFETs, minimization of gate signal delays, cooling of the individual MOSFETs, balancing resistors, high-voltage isolation required for the power supplies, and the controlling pulse width modulated (PWM) signal as well as differential voltage feedback measurement across individual MOSFETs. A gate driver capable of providing sufficient galvanic isolation for

the power supply and gate-driver signal of the (high-side) driver IC is required to drive the HV switch. In addition, the high switching speed of the SiC MOSFETs in the HV switch module leads to high dV/dt, and introduces considerable common-mode (CM) current circulating the gate driver and control circuit, thereby posing a potential risk to the normal operation of the HV switch. A low coupling capacitance of the gate driver power supply can minimize this CM current. To this end, a custom gate driver with 10 kV isolation and low coupling capacitance (< 20 pF) is designed and developed to drive the modular HV switch.

Deficiency in the SOTA:

7. BEHLKE-made switches are expensive. For instance, a single HTS-151-30 switch costs around $5,000.
8. BEHLKE switches along with direct liquid cooling units occupy a considerable amount of space. For instance, an HTS-151-30 switch from BEHLKE has a footprint of approximately 225*85*75 mm without considering the liquid cooling system. Some key parameters of this switch are as follows.
    (a) Maximum operating voltage = 15 kV
    (b) Maximum continuous load current = 2.52 A (without cooling), 30 A (with liquid cooling)
    (c) Maximum turn-ON peak current = 300 A (pulse width = 200 μs, duty cycle <1%)
    (d) Turn-ON resistance = 1.3 Ω
9. Once the switching frequency is greater than 10 kHz, a liquid cooling system is required to operate the BEHLKE switch.
10. Without liquid cooling, the maximum continuous power dissipation (P_{cont}) of the BEHLKE switch is limited (e.g., for HTS-151-30, P_{cont} is 10 W without liquid cooling).
11. At a higher switching frequency (>20 kHz), the BEHLKE switch requires multiple ancillary DC power supplies, i.e., 5, 15, and 60 V.
12. The switches made by BEHLKE cannot be reconfigured to withstand a higher voltage exceeding their recommended rating. BEHLKE offers separate products to operate them at higher voltage/currents.

15.3 Technical Background

With the rapid advancement of wide-bandgap (WBG) semiconductor devices, applications of power electronics have increased manyfold. WBG material (e.g., SiC, GaN) based semiconductor devices (e.g., MOSFET, IGBT, etc.) undeniably edges the traditional Si-based semiconductor devices in some key performance metrics including but not limited to dielectric field strength, breakdown voltage, thermal reliability at high temperature, form factor [1]. Low conduction loss (due to low ON-resistance), low switching loss (due to low gate charge) of WBG devices enable higher switching speed, and lead to a diminished requirement of thermal management compared to Si devices,

thereby increasing the power density of an entire system reliant on semiconductor devices. The typical junction temperature of SiC-based devices is close to 200 °C which is approximately 50 °C higher than the typical junction temperature of Si-based devices [2]. This property coupled with excellent thermal conductivity allows the SiC devices to reliably operate at a higher temperature without introducing significant performance de-rating as opposed to the Si devices.

MOSFETs, in general, are inherently faster compared to other types of semiconductor devices (e.g., IGBT, thyristor, etc.). Therefore, WBG MOSFETs are predominantly chosen in high-voltage and high-speed power electronics applications, such as high-voltage pulse generator, electric vehicle powertrain, industrial motor drives, X-ray machines, pulsed power system, etc over other switch types. Lower switching loss and lower ON-resistance of the GaN MOSFETs notwithstanding, the maximum breakdown voltage (900 V) of the commercial-off-the-shelf (COTS) GaNFETs is lower than that of the COTS SiC MOSFET (3300 V) [3], [4]. Therefore, SiC MOSFETs are preferable in high-voltage and high-speed power electronics applications as an alternative to Si devices.

Recent advancement in SiC technology is mirrored in the gradually increasing blocking voltage capability of COTS SiC MOSFETs as evidenced by the new generation of commercially available SiC MOSFETs with a voltage breakdown rating of 3.3 kV. Testing of some of the high-voltage (10-15 kV rated) SiC modules has been demonstrated in select research laboratories. [5], [6]. However, commercialization of these modules seemingly not forthcoming due to excessive manufacturing cost and design complexities. Series connection of multiple low-cost COTS SiC MOSFETs or multilevel converter topologies is two intriguing approaches to attain higher voltage blocking capability. Notwithstanding the considerable advantages of the multilevel converter topologies in terms of low common-mode voltage, low dv/dt stress, and radiated electromagnetic interference to a lesser extent compared to the series-connected MOSFETs [7]–[9], features such as lesser cost, relatively simpler construction, higher efficiency related to the series-connected MOSFET tip the scale in favor of this approach.

Series connection of multiple low-cost COTS SiC MOSFETs is an intriguing cost-effective solution to the increasing demand for semiconductor devices with a high voltage blocking capability and high-speed compatibility. That being said, ensuring equal voltage stress across the MOSFETs in a series stack during the turn-OFF period (steady-state) and switching transients (dynamic state) is a major design challenge for researchers in this field.

Parameter variation of the switching devices, unsynchronized gate drive signals, non-optimized trace layout can lead to unequal voltage exposure across the series-connected MOSFETs in a stack. The unbalanced voltage distribution among the series-connected switches can subject to single or multiple switches to overvoltage stress beyond their rated values resulting in the failure of these switches. This event can subsequently lead to cascaded failures of all switches in a series stack, thereby leading to complete failure of the device which is catastrophic. To that end, mitigating the voltage imbalance issues pertaining to the series-connected switch is a major design consideration for the researchers working in this field.

Steady-state voltage balancing can be attained by paralleling balancing resistors across each switch connected in series [1], [10]–[23]. However, there is a tradeoff between the level of voltage imbalance at steady-state and losses due to leakage current [20]. As opposed to the relatively simpler design process of voltage balancing during the steady-state, a more sophisticated approach is required to address the dynamic voltage balancing issues. Researchers, working in this field, have proposed a number of approaches as of now to address this issue with a certain amount of success. The techniques proposed to ensure voltage balancing during switching transients can be classified into two major categories, namely- load-side techniques [24]–[27], and gate-side techniques [28]–[32].

The load-side technique is largely reliant on the utilization of passive snubbers, which are among the simplest forms of voltage balancing schemes. In this scheme, snubber capacitors coupled with snubber resistors (RC snubber) and/or diodes (RCD snubber), are connected in parallel with individual power switches. The capacitances of the snubber capacitors are required to be at least five to ten times the output capacitances of the semiconductor switches [24] to effectively control the dynamic voltage imbalance at the expense of the increased amount of snubber power loss and extended commutation time of the switches. In [25], a RCD snubber was introduced in the dynamic voltage balancing scheme for a series-connected HV switch made from two 1.7 kV rated MOSFETs. A RC snubber was used in [27] to minimize the dynamic voltage imbalance of a developmental series-stacked HV switch. To address the fundamental problem of high snubber losses associated with a snubber scheme, a strategy has been proposed in [26] that involves the partial discharge of snubber capacitors during a switching cycle leading to reduced reset current surge and reduced power loss. However, one onboard power supply per switch is required in this proposed scheme, thereby increasing the footprint, and cost of the HV switch.

The active gate control method can be a feasible solution for the dynamic voltage balancing problems among the semiconductor switches in a series stack. This method involves manipulating the dynamic of operation of the switches in their active region and capitalizing on the relationship between the levels of the gate drive signal and the switching transient of the devices. Active voltage clamping circuits proposed in [28], [33], and auxiliary circuits proposed in [29], [30] based on active gate control mechanism aim at controlling the dynamic voltage imbalance in a series stack of switches by feeding additional charges back to the gate terminal to marginally turn the switches ON at the onset of a voltage overshoot event. More sophisticated active gate control methods are demonstrated in [31], [32], [34], where feedback control is employed in the gate-drive loop to regulate the slew rate (dv/dt) of the devices connected in series with respect to carefully defined reference signals to control the voltage overshoot during switching transients. Another way to minimize voltage overshoot, thereby voltage imbalance in a series stack of switches caused by asynchronous gate signal delays during switching transients is to introduce controlled delays in the gate drive signals [12], [13]. The ingenuity of this approach lies in the fact that the switching speed of the HV switch remains the same while particular gate signals are slightly delayed by a precise amount to counteract the voltage overshoot pertaining to those switches. However, to ensure cycle-by-cycle control over the entire switch, feedback circuits and associated A/D conversion circuits are required

in these methods [12], [18], [35], [36]. A considerable amount of time delay may incur on top of the feedback circuitry-controlled gate signal delays due to the delay in sensing and prolonged response time of the A/D conversion circuits. This may curb the high-speed switching capability of SiC MOSFETs, thereby nullifying the advantages associated with WBG devices, and leading to excessive voltage imbalance during initial switching cycles that put the entire switch at risk of a cascaded failure. A modified gate delay control method using a delay line IC to increase the resolution of the delay control step to 150 ps has been reported in [18]. This method allows the SiC MOSFETs to retain their switching capability at the rated maximum operating frequency. However, this method does not account for the problem of voltage imbalance during the initial switching cycles encountered in similar aforementioned works. To solve this problem, a voltage balancing technique under steady-state and start-up conditions based on digital time delay circuit is proposed in [37]. This technique features the capability of updating the initial delay time to account for the voltage imbalance during the startup of the HV switch. However, parameter fluctuations of the switching devices due to process variation during the manufacturing process can lead to the variation of the initial delay time. In addition, the auxiliary circuits associated with generating the delays in gate signal compound the overall cost and complexity of the entire HV switch. In [38]–[40], authors introduced a new wrinkle to the dynamic voltage balancing schemes in the form of adaptive gate resistance for a specific period during the turn-ON or turn-OFF time of the switch. However, attaining the required amount of change in gate resistance with precision timing is of utmost importance to ensure optimal voltage balancing, which is relatively complex to accomplish, and costly to implement. In [14], a voltage balancing scheme incorporating a gate-balancing core is introduced to synchronize the gate drive signals for all the series-connected power devices. However, the magnetic core increases the footprint of the device, and the margin for error in core design is slim, thereby compromising its practical implementation feasibility. An active voltage control technique incorporating a current source at the gate control side of the low-side switch is proposed in [17]. This technique is capable of ensuring voltage balancing during switching transients for the low-side switch only.

Capacitive coupling-based series-connected switches employ a single gate driver to drive an entire switch stack aided by a few coupling components [1], [19]–[21], [41]. As opposed to the active gate control-based voltage balancing methods, the switches in a series stack in the capacitive coupling method do not require individual gate drives, resulting in a more compact footprint and reduced manufacturing/fabrication cost. In [1], the capacitive coupling method is used to control dynamic voltage balancing among series-connected MOSFETs. However, the design of the proposed HV switch is relevant for only two stages. A quasi-active gate control-based capacitive coupling method was proposed in [21] featuring a single gate driver. During the turn-OFF period, the gate-source voltage of the upper device of the series stack remains close to the threshold limit, thereby posing a risk of false turn-ON. Therefore, reliability and scalability issues plague this technique and compromise its implementation feasibility in practical applications. A two-stage GaN MOSFET-based HV switch featuring a capacitive coupling method is proposed in [41]. Unfortunately, the scalability of this method in terms of a higher number of stages requires experimental validation. In contrast with the passive snubber-based and active gate

control-based dynamic voltage balancing techniques, the capacitive coupling-based technique offers superior response speed, simpler circuit operation, and reduced fabrication cost. That being said, ensuring steady voltage balancing with higher number of stages and higher operating voltage remains an area of continuous improvement in HV switch design.

The unavailability of standard isolated gate drivers at high-voltage levels (>5.7 kV) is another major design challenge in experimentally validating the efficiency of the designs of HV switches (as high-side switches) at high (>5.7 kV) voltage levels. Standard COTS isolated gate driver ICs along with standard isolated power supplies for the gate driver ICs lack adequate ruggedness to handle high dv/dt stress typically associated with SiC MOSFETs. To that end, developing a custom gate driver equipped with adequate voltage isolation for the power supplies and the control signal for the gate driver IC is of equal importance as designing a HV switch.

In this report, a capacitive coupling-based modular series-connected HV SiC switch design with excellent voltage balancing has been documented. The proposed method takes advantage of the modular approach to offer scalability to cater to high-voltage applications without the need for a complete redesign and rebuild. The modularity requires the passive components (e.g., capacitors, diodes) in a module to be able to only withstand the voltage across that module instead of the entire HV switch, thereby reducing the voltage stress across those passive components. This eliminates the requirement of stacking many of those passive components in series leading to a compact footprint. A custom HV isolated gate driver with high (≈ 10 kV) galvanic isolation for the power supplies of the driver IC and optical fiber aided isolation for the control signal has been designed and developed to drive the modules of the proposed HV switch. Each module of the HV switch, therefore, consists of one custom isolated gate driver that drives four SiC MOSFETs connected in series coupled with coupling capacitors, diodes, and snubber circuits. The simulation and experimental results are in close agreements regarding voltage balancing among the series-connected 1.7 kV rated SiC MOSFETs in each module during both steady and dynamic states up to a DC supply voltage of 6 kV and a switching frequency up to 15 kHz.

15.4 Tasks, Milestones, and Status

1.4.1 Design a surface-mount MOSFET-based four-stage switch (6.8 kV rated) and control it using the in-house gate driver, then test its voltage-withstanding ability with a DC supply voltage up to 4–5 kV and evaluate the effectiveness of the thermal management at its current state / DEC 2020 / Completed.

1.4.2 Design and develop a modular HV switch (~10 kV rated) using the concept of the tested four-stage high-voltage switch module and an in-house modular gate driver to drive the modular switch /JAN–FEB 2021 / Completed.

1.4.3 Test the voltage withstanding ability of the modular HV switch with a DC supply voltage up to 10 kV and switching frequency up to 50 kHz using a resistive load (5–10 kΩ) and evaluate the effectiveness of the thermal management at its current state / FEB–SEP 2021 / Completed.

Details: *Achieving the necessary 10 kV breakdown voltage was a challenge in our previous version of the HV switch. Although the previous version was designed for 10 kV or higher, the gate driver circuit suffered from voltage breakdown on the PCB. We have identified the problem, and it was caused due to narrow spacing between two traces carrying a voltage gradient equal to the high-voltage (HV) supply. Since we experienced this failure, we have redesigned the PCB and used a new optical fiber TX-RX assembly to eliminate this problem.*

1.4.4 Test the isolation capability and evaluate the synchronization accuracy of the gate drive signal generated from the modular in-house gate driver / FEB–SEP 2021 / Completed.

Details: *A second test was conducted at a lower voltage using a different loading condition. The load was a series combination of a 200 kΩ resistor and a 9.6 kΩ resistor. Therefore, this combination worked as a voltage divider, and we measured the voltage across the 9.6kΩ resistor. The divider ratio was 21.833:1.*

1.4.5 Encapsulate the gate driver board with potting material with a high (~15–20 kV) breakdown voltage rating to prevent possible flashover/arcing in between the HV switch and this board / MAR–SEP 2021 / Ongoing.

Details: *The entire circuit assembly including the driver PCB was immersed in di-electric oil to prevent any unwanted arcing through air, although the final design will use some sort of potting materials for packaging ease. This technique not only resolves the arcing issue, but it also improves the thermal distribution of the system. A complete system has been tested at 10KV, and it successfully withstands this voltage. A repetition rate of 1 kHz is used during testing. The load impedance was 300 kΩ.*

1.4.6 Design and fabricate a compact power conditioner circuit based on a 12 kV rated SiC switch made by BEHLKE (HTS 121-15) / APR–MAY 2021 / Completed.

1.4.7 Test this modular HV switch coupled with a Si PCSS device up to a DC supply voltage of 5–6 kV and a switching frequency of 50 kHz / SEP 2021/Ongoing.

1.4.8 Design and develop a 20 kV rated modular (two modules, each with four MOSFETs) HV switch based on the design concept of the 10 kV rated modular switch using 3.3 kV rated SiC MOSFETs (new product made by GeneSiC Semi) / Ongoing.

1.4.9 Design and develop a 20 kV rated modular gate driver based on a WPT based planar transformer topology to ensure adequate galvanic isolation (~30–40 kV) for the power supplies of the gate driver / Ongoing.

15.5 Methods and Approach

15.5.1 *Architecture details*

The schematic of the proposed modular switch using series-connected SiC MOSFETs is shown in Fig. 1. Two identical modules comprise the HV switch, and each module consists of four series-connected MOSFETs. Aside from the SiC switches (S_i, i= 1, 2…..8), the circuit of the HV switch contains coupling capacitors, C_{ci} (i=2, 3, 4, 6, 7, 8), snubber capacitors, C_{si} (i=1, 2…8), zener diodes, Z_{ia} and Z_{ib} (i=1, 2….8), gate resistors,

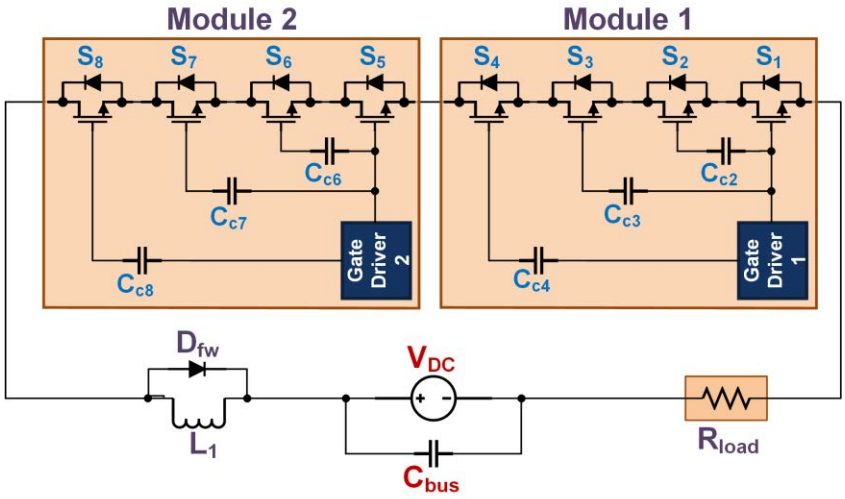


Fig. 1. Schematic of the proposed modular HV switch.

R_{gi} (i=1, 2….8), ferrite bead, FB_i (i=1, 2….8), balancing resistors, R_{si} (i=1, 2…..8), gate-loop diodes, D_{ci} (i=2, 3, 4, 6, 7, 8), inductor L_1 and a freewheeling diode, D_{fw}. A DC bus capacitor bank, C_{bus} is connected across the entire switch, and incorporated in the fabricated HV switch prototype to reduce parasitic inductance stemming from additional wire-board connections. Two custom HV gate drivers are connected across the gate-source terminals of the rightmost MOSFETs (S_1, S_5) in each module. These MOSFETs are coined as the master MOSFETs throughout the rest of the paper for the ease of narration. The rest of the MOSFETs are termed slave MOSFETs and are mentioned as such throughout the rest of the paper as well. A detailed schematic diagram of a single module is illustrated in Fig. 2.

15.5.2 *Key Parameter Selection*

A. Selection Criteria of Balancing Resistors

During the steady-state, the modular switch as a whole is subjected to the entire DC bus voltage. Two mechanisms primarily govern the degree of voltage imbalance among the series-connected MOSFETs in the series stack. Unequal leakage currents pertaining to the manufacturing process variations of the MOSFETs in the modular switch act as the salient instigator of the voltage imbalance during the steady-state. On top of that, probable voltage imbalance a mong the drain-source voltages of the series-connected MOSFETs at the end of the turn-OFF transition stage may carry over to the ensuing steady-state. Resistors can be connected in parallel to the drain-source terminals of the series-connected MOSFETs to minimize the aforementioned voltage imbalance issue associated with the steady-state. The selection of these resistors (R_{si}, i= 1, 2….8), termed as balancing resistors, is a trade-off between power dissipation and the level of voltage imbalance during the steady-state. The value of the balancing resistors required to ensure a steady-state voltage imbalance ratio below 10% can be determined from the following equation [1].

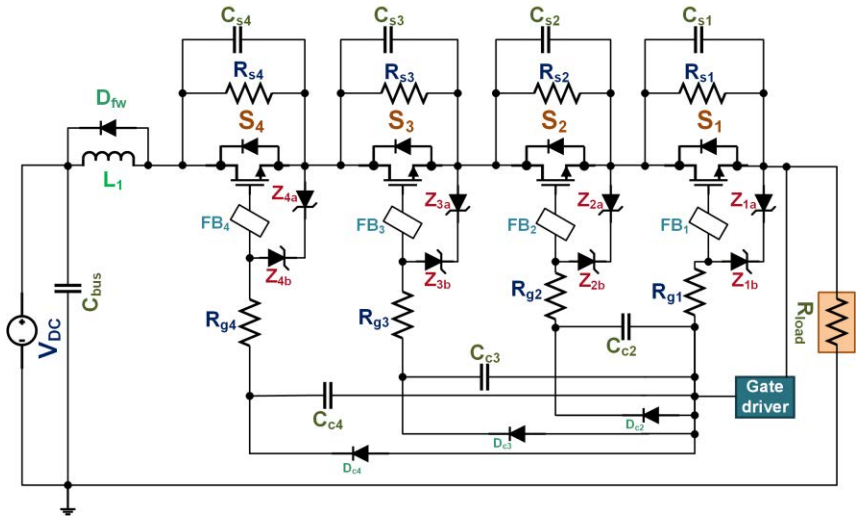


Fig. 2. Schematic of a single module of the HV switch.

$$R_{\mathrm{si}} < \frac{V_{\mathrm{DC}}}{10 I_{\mathrm{DSS(max)}}}, i = 1, 2 \ldots \ldots 8 \qquad (1)$$

Where I_{DSS} is the leakage current at V_{GS} = 0, and V_{DC} is the supply voltage. Lower R_s leads to a reduced level of voltage imbalance at the expense of higher static power dissipation. In practice, resistors are chosen to have values that are one magnitude less than the equivalent OFF-state resistance of the MOSFETs to direct the leakage current passing through them instead of the MOSFETs.

B. Selection Criteria of Coupling Capacitances

The influence of the coupling capacitors on the dynamics of the switching transient of the individual MOSFETs of the proposed modular switch is pronounced. The gate-source capacitances of the slave MOSFETs are charged and discharged by the discharging and charging of the coupling capacitors respectively. This implies that the amount of gate charge required to completely turn the slave MOSFETs ON and OFF are solely provided by these coupling capacitors. To that end, the stored charge in the coupling capacitors during the turn-OFF period should be greater than the total gate charges (Q_{gi}, i= 2, 3, 4, 6, 7, 8) of the slave MOSFETs.

In the proposed architecture, the coupling capacitor associated with the slave MOSFET located farthest from the master MOSFET in each module experiences the maximum voltage stress which does not exceed a level of $3V_{DC}/8$ thanks to the modularity of the proposed switch. The voltage level experienced by C_{c2}, C_{c6} is $V_{DC}/8$, and in the case of C_{c3}, C_{c7} it is $2V_{DC}/8$. The required capacitance values should satisfy the following equation.

$$C_{ci} > \frac{Q_{gi}}{(i-1) * V_{DC}/8}, i = 2, 3, 4 \qquad (2)$$

$$C_{cj} > \frac{Q_{gj}}{(j-5) * V_{DC}/8}, j = 6,7,8 \qquad (3)$$

The typical value of the gate charge (Q_g) of the used MOSFET is 13 nC under a DC bus voltage of 1.2 kV and a load current of 2 A. From equations (2) and (3), the minimum value required for the coupling capacitors at 6 kV can be determined as 5.7 pF, 8.7 pF, and 17.3 pF. The proposed modular switch includes coupling capacitors with values 7 pF, 10 pF, and 21 pF, thereby closely approximating the theoretical values.

C. Selection Criteria of Gate Resistors

SiC MOSFETs have superior switching speed compared to their Si counterparts, reaching a slew rate as high as 50V/ns [42]. However, the extremely high slew rate in addition to the package and circuit stray inductances can lead to voltage overshoot (*L*di/dt*) and subsequent ringing [43], [44]. A compactly designed PCB can contribute significantly to the reduction of stray inductance, thereby mitigating the aforementioned problem to a great extent. That said, minimum creepage and clearance requirements for safe high-voltage operation can inhibit the ability of the circuit designer to optimize the PCB footprint. An alternative solution can come in the form of sufficiently large gate resistors at the expense of increased loss. In our proposed design, we have incorporated 15 Ω gate resistors as a tradeoff between the level of gate ringing and additional loss.

D. Selection Criteria of Snubber Capacitors

Snubber capacitors (C_{si}, i= 1, 2…..8) connected across the drain-source terminals of the series-connected MOSFETs, minimizes the mismatch in slew rates (dV_{dsi}/dt, i= 1, 2,…..8) during switching transients. Unlike traditional snubber capacitors, small valued (in the range of picofarads) capacitors are connected across the drain-source terminals of individual MOSFETs. Snubber capacitors with large values prolong the turn-OFF transition of the individual MOSFETs, thereby increasing the switching loss. Conversely, the absence of snubber capacitors curtails the transition time during the turn-OFF period of the switch at the expense of too big of a mismatch between the slew rates of the individual MOSFETs that can potentially lead to voltage imbalance of excessive proportions. To that end, a tradeoff is required during the selection of the snubber capacitor values. In the fabricated HV switch prototype, 100 pF ceramic capacitors have been used as snubber capacitors.

E. Selection Criteria of Ferrite Bead

Mitigation of voltage overshoot, electromagnetic interference (EMI) associated with the ultrafast switching characteristic (i.e., high *di/dt*, high *dv/dt*) of the SiC devices is of paramount importance in any high-voltage application [44], [45]. Ferrite bead can assist gate resistors to further minimize the aforementioned issues related to ultrafast switching of the SiC devices [45]. Ferrite bead, in essence, mimics the performance of an RF choke, thereby incorporating high resistance (hundreds to thousands of ohms) in the gate loop at relatively high frequency (tens to hundreds of MHz). However, it barely impacts the circuit's operation at low frequency (tens to hundreds of kHz). Therefore, a carefully

selected ferrite bead that offers high impedance at the frequency of interest (ringing frequency) can drastically elevate the performance of the SiC switch. We have incorporated SMD ferrite beads with 2 kΩ resistance at 30 MHz in the gate loop circuits of the series-connected MOSFETs.

15.5.3 *Design Details of a Custom HV Isolated Gate Driver*

The modular 10 kV rated HV switch proposed by the authors in this report requires two isolated HV gate drivers, one for each module of the HV switch. The required isolation rating of each gate driver is at least 10 kV to ensure reliable operation of the HV switch. However, commercial-off-the-shelf (COTS) gate driver modules have isolation ratings as high as 5.7 kV [46], [47]. This rating implies that COTS gate driver modules are not equipped to drive a HV switch with a voltage rating greater than 5.7 kV. Prior studies on HV isolated gate drivers showcased designs based on some experimental switch modules (e.g., CPM3-10000-0350, XHV-9, XHV-7 developed by CREE) [48]–[51]. However, none of the gate driver designs has been realized as a commercial high-voltage isolated gate driver solution as of now. To this end, the authors have proposed and developed a working prototype of a modular (two modules) high-voltage (10 kV rated) isolated gate driver ensuring synchronization of the gate signals for the two modules of the proposed HV switch. Two levels of isolation are needed to be incorporated in the HV isolated gate driver design, namely, i) isolation of the control/PWM signal, and ii) isolation of the power supplies of the gate driver IC. Control signals (e.g., signals for pulse width modulation, overcurrent protection, temperature sensing, etc.) can be isolated by means of optocouplers [52], coreless transformers [53], classical transformers [54], optical fibers [55], etc. Optical fiber is the preferred choice in most cases to provide isolation for the control signals thanks to its superior immunity to noise coupled with high galvanic isolation capability.

Isolation required for the power supplies of the gate driver IC needs to satisfy two basic requirements- i) adequate high-voltage isolation, and ii) low coupling capacitance. The high voltage isolation barrier safeguards the primary side of the power supply from disruptive ground loops, potential dielectric breakdown casualties caused by high voltage surges, and protects human operators at the control side from deadly electric hazards [56]. Low coupling capacitance (C_{iso}) minimizes the coupling of common-mode current (i_{CM}) from the power side to the control side caused by high *dv/dt* during switching transients of SiC MOSFETs and ensure reliable operation of the gate driver. Equation (4) underscores the influence of the coupling capacitance (C_{iso}) of the gate driver and the slew rate (*dv/dt*) of the SiC MOSFET on the common-mode current.

$$i_{CM} = C_{iso} \frac{dv}{dt} \tag{4}$$

Air core or tape-insulated transformers [48], [50], [57]–[59] with discrete windings, or PCB windings [49], [60], inductive power transfer (IPT) coils [61]–[64], optical fibers [51] are the basis of some of the methods proposed in the literature to isolate the power supplies of the gate driver IC. However, a majority of these approaches (e.g., transformer, IPT,

etc.) lead to a large footprint whereas the optical fiber-based approach requires a bulky and expensive laser system, thereby compromising the feasibility of this approach.

A single module of the proposed 10 kV rated gate driver features three compact (≈ 1 sq. inch) 10 kV rated isolated DC-DC converters to provide galvanic isolation for the power supplies of the gate driver IC [65]. These converters, having a power rating of 6 W, can operate at an input voltage ranging from 24 V to 36 V, and capable of producing a regulated output. A 5.7 kV_{RMS} rated reinforced isolated gate driver IC with 2.5 A sourcing and 5 A sinking current capability, has been selected for the proposed gate driver module. The selected gate driver IC has a dedicated pin (V_{EE2}) for ease of application of bipolar supply that facilitates the supply of recommended negative voltage required to ensure reliable turn OFF of SiC MOSFET. An optical fiber link has been designed and developed using transmitters, receivers, and optical fiber that belong to the HFBR-0500Z series. The optical fiber link supports a data transmission rate of 5 MBd and can handle a breakdown voltage rating of 500 V/mm [66]. A DC supply voltage of 24 V powers the gate driver board. Three isolated DC-DC converters yield three voltage rails of +24 V, +5 V, and -5V respectively. The +5 V rail powers the input side of the gate driver IC as well as the receiver of the optical fiber link. A linear regulator (LM1086) scales down the +24 V rail to a regulated +20 V rail. The +20 V rail and the -5 V rails are connected to the output side of the gate driver IC to generate the recommended voltage levels (+20 V, -5 V) required for reliable switching of the SiC MOSFETs. Another linear regulator (LM1086) is

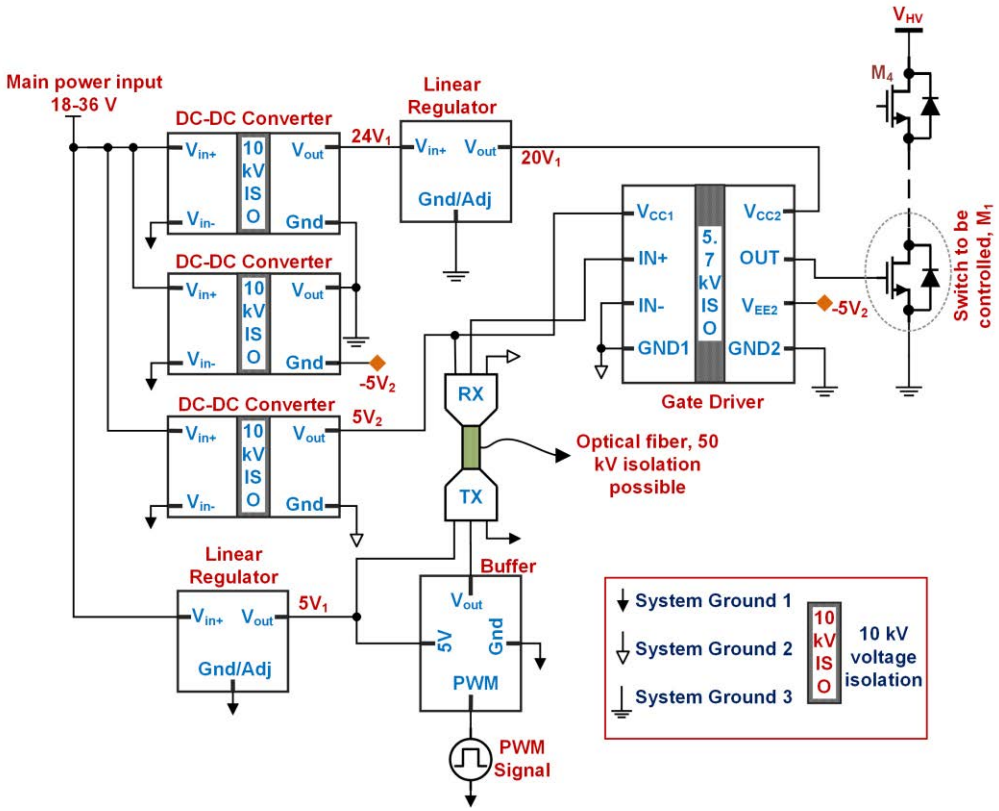


Fig. 3. Schematic of a single module of the proposed gate driver.

incorporated in the design to generate a steady +5 V rail from the primary DC supply that is used to power the transmitter of the optical fiber link. The entire setup is shown in Fig. 3.

The modular gate driver has six isolated DC-DC converters, three for each module as in the single module. However, both modules share the same input DC supply and a single buffer IC (SN75451) with dual outputs feeding identical PWM signals to two transmitters equally distanced from the buffer IC. The rest of the circuit designs of the two gate driver modules are quite identical, thereby eliminating the possibility of performance variation of the gate driver modules as much as possible. One of the major design concerns of a multi-output gate driver is ensuring synchronization of the gate drive signals. To that end, two gate driver ICs, one for each module, are placed equally apart from the receivers of two fiber-optic links in the PCB design. Board-to-board connectors are used to connect the modular gate driver board to the modular HV switch to reduce parasitic inductance in the gate drive loop as well as providing mechanical rigidity to the assembly of the HV gate driver and the HV switch. The traces from the output signals pins of the gate driver ICs to the board-to-board connectors are kept short and of equal length to ensure synchronization of the gate signals as well as further minimization of parasitic inductances

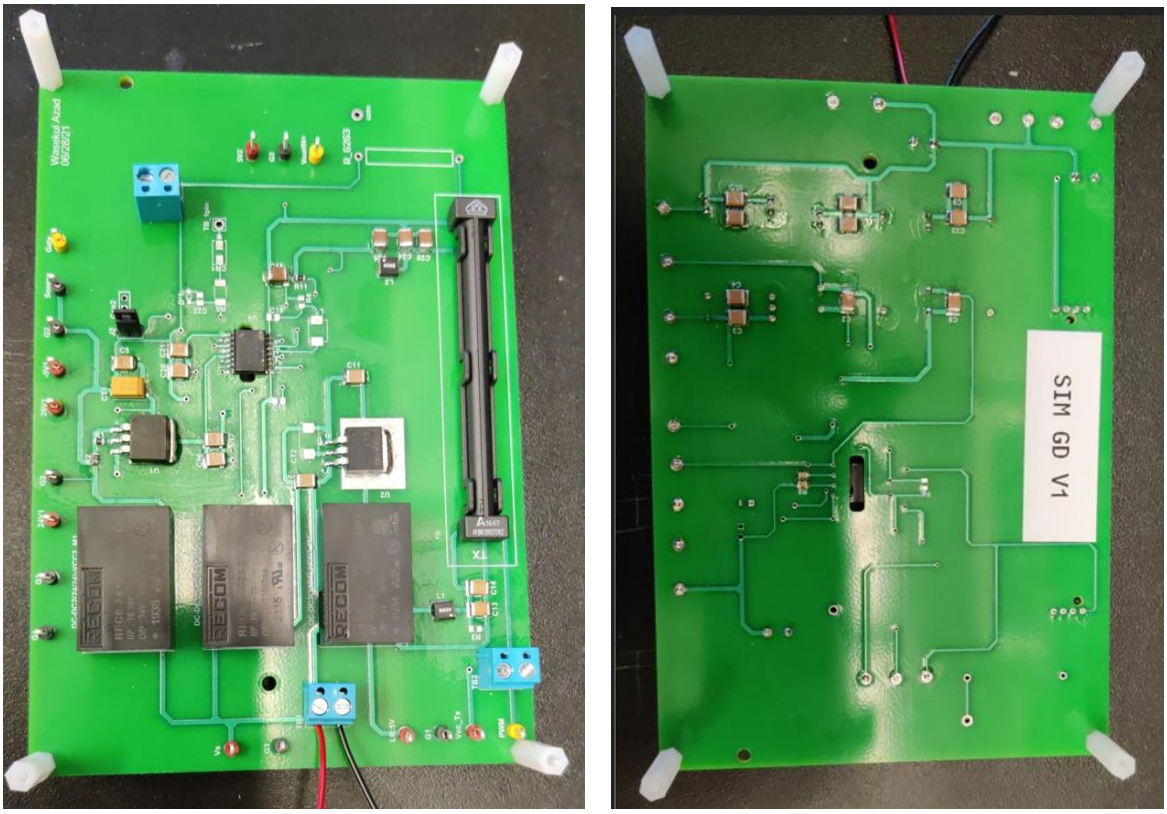


Fig. 4. Actual photograph of the modified gate driver circuit showing the integrated optical link (TX) on the left figure.

in the gate loop of the modules of the HV switch. The schematic of a single module of the modular HV gate driver and the fabricated modular HV gate driver board are shown in Fig. 4.

The new MOSFET board shown in Fig. 5 has two modules, and has the following +5V, -5V,24V,20V buses, and they all were tested stable and withing tolerance. Total Input current = 100mA. The signal integrity and rise/fall behavior of the new driver board have been shown in Figs. 10 and 11.

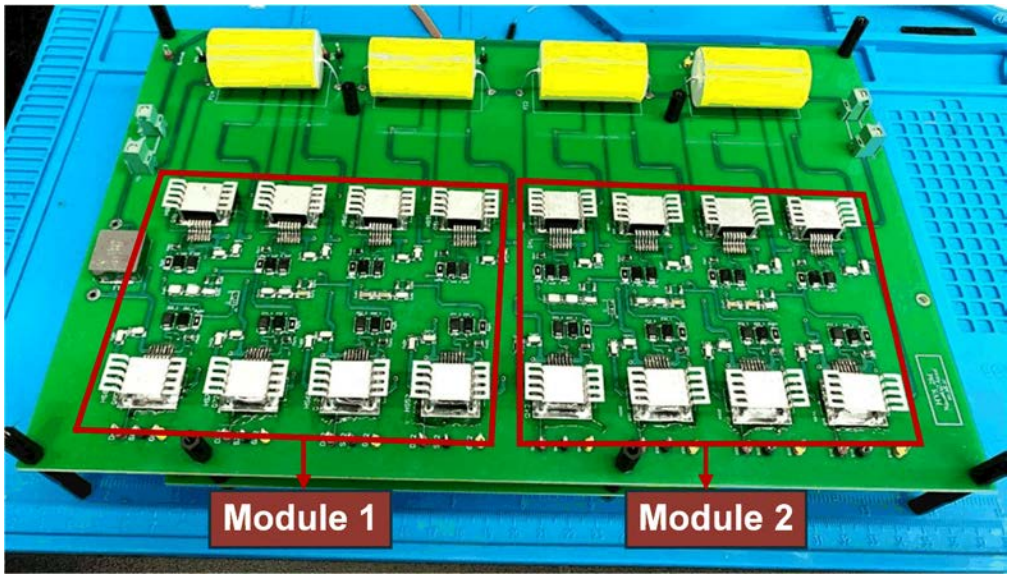


Fig. 5. Fabricated prototype of the proposed 10 kV modular switch.

15.6 Results and Discussion

Phase I: A 6.8 kV rated four-stage surface-mount MOSFET developed in-house was successfully tested up to a DC supply voltage of 4 kV and at a switching frequency up to 20 kHz with a 3.2 kΩ resistive load. The proposed voltage balancing method achieves <1.1% voltage mismatch under steady-state and switching transitions. The proposed modular HV switch coupled with the custom in-house HV isolated gate driver was tested using a DC supply voltage up to 6 kV and at a repetition frequency up to 15 kHz using the 9.6 kΩ resistive load. Experimental results show reliable turn-ON and turn-OFF characteristics of the entire HV switch under the specified operating condition. The voltages measured across the drain-source terminals of the MOSFETs in a single module are shown in Fig. 6 (VDC = 5 kV, $f$sw = 40 kHz, duty cycle = 50%). A maximum voltage imbalance close to 50 V was recorded among the drain-source voltages of the series-connected MOSFETs in a single module that experienced a DC voltage stress of 2.5 kV, thereby validating the effectiveness of the proposed voltage-balancing scheme. To test the entire switch at a higher voltage level, the voltage across the 9.6 kΩ load at a supply voltage of 6 kV and a repetition frequency of 10 kHz was measured and shown in Fig. 7. The measured voltages across the drain-source terminals of the series-connected MOSFETs from both of the modules are depicted in Fig. 8. In this configuration, each module experienced a maximum voltage stress close to 3 kV. A maximum voltage

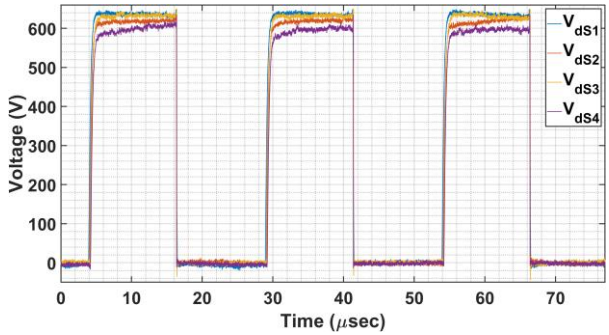


Fig. 6. Experimental drain-source voltages measured across the individual MOSFETs in a single module (V_{DC}= 5 kV).

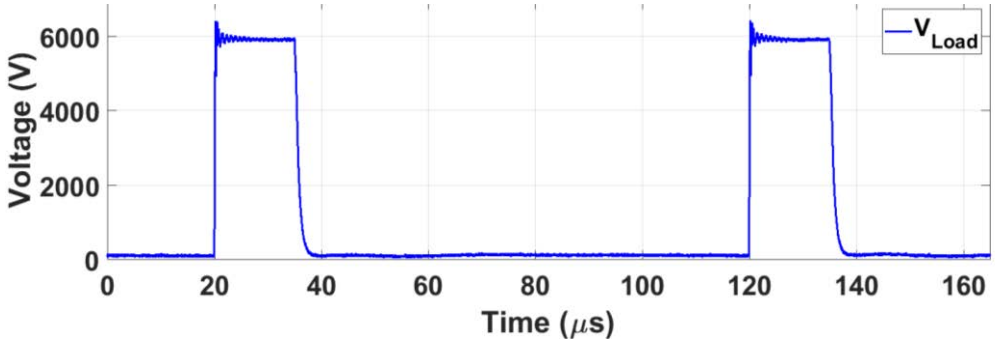


Fig. 7. Voltage measured across the 9.6 kΩ resistive load (V_{DC}= 6 kV) to test the 10 kV switch.

imbalance close to 80 V was recorded among the drain-source voltages, which is negligible compared to the breakdown voltage rating of an individual MOSFET. The experimental results are in close agreement with the simulation results regarding voltage balancing among the series-connected 1.7 kV rated SiC MOSFETs in each module during both steady and dynamic states up to a DC supply voltage of 6 kV and a switching frequency up to 15 kHz.

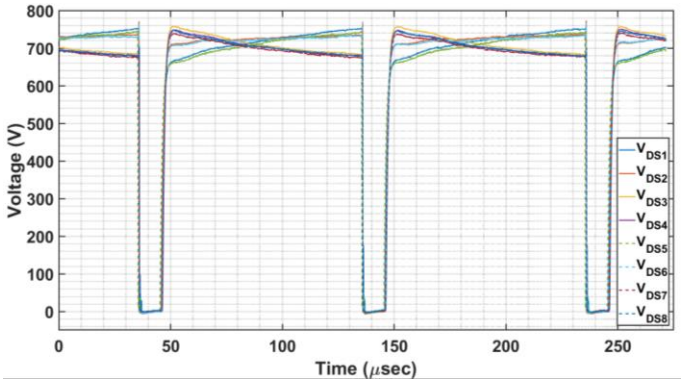
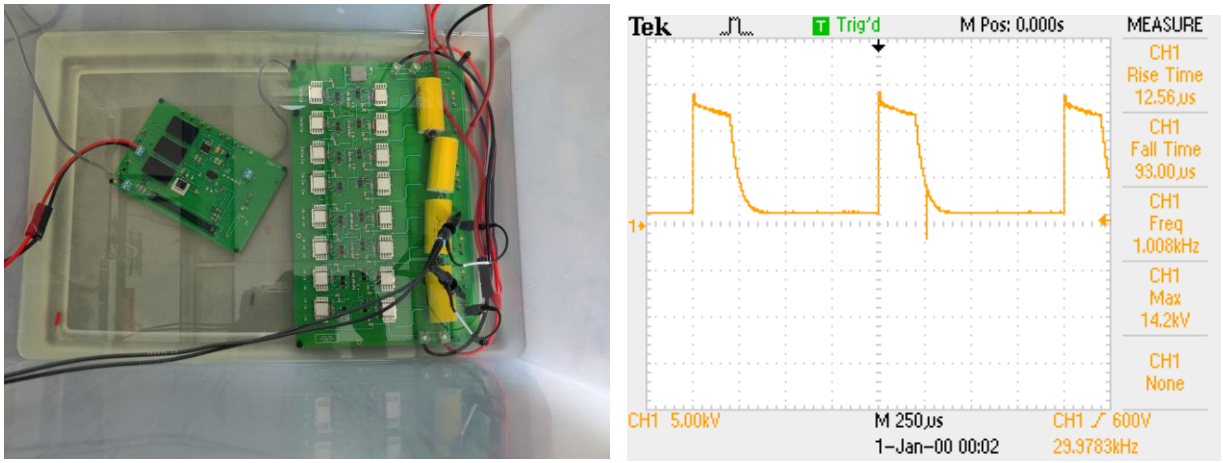


Fig. 8. Experimental drain-source voltages measured across the individual MOSFETs in the entire HV switch (V_{DC}= 5 kV).

The lowest rise time was measured as 41 ns associated with the slave MOSFETs (S_4, S_8) located farthest from the master MOSFET in each module. The highest rise time belonged to the master MOSFETs (S_1, S_5) in each module, and recorded as 52 ns. The rise time of the HV switch can be approximated by the highest rise time associated with the series-connected MOSFETs. That being said, the recorded rise time of the proposed modular HV switch is still considerably lower compared to the COTS switches with similar voltage ratings.

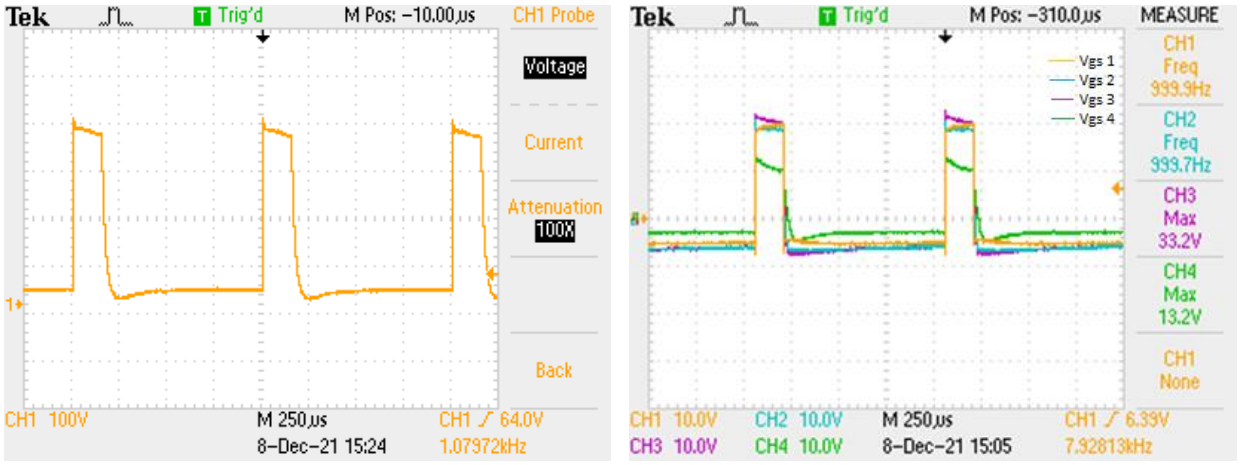
Phase II: A modular (two modules) 10 kV rated HV switch has been designed and a prototype has been developed using 1.7 kV rated SMD MOSFETs (C2M1000170J). An in-house 10 kV rated HV gate driver has been designed and incorporated with the HV switch to drive it (Fig. 9). A manuscript on the HV switch and the custom isolated gate driver has been submitted to IEEE Transaction on Power Electronics. An insulating naphthenic dielectric oil has been acquired that meets the ASTM D-3487 specification. With the use of this dielectric oil, altered component placement and new TX-RX optical module, the newly designed gate driver and MOSFET PCB can safely withstand 10KV. At present, the prototype runs at Fsw = 1 kHz, d = 15%, V_{DC} = 10KV, and R_{load} = 300 kΩ. We are yet to test the circuit at 50 kHz switching to complete milestone 1.4.3. We need to test the circuit at much higher load current (load impedance = 5–10 kΩ), and we plan to do so in January. Our present setup especially the HV power supply limits us to test the circuit at significantly smaller load current.

At 10 kV, the gate driver circuit operates flawlessly, and the gate-source signals have the necessary integrity to avoid malfunctions. Results are shown in Figs. 10 and 11.



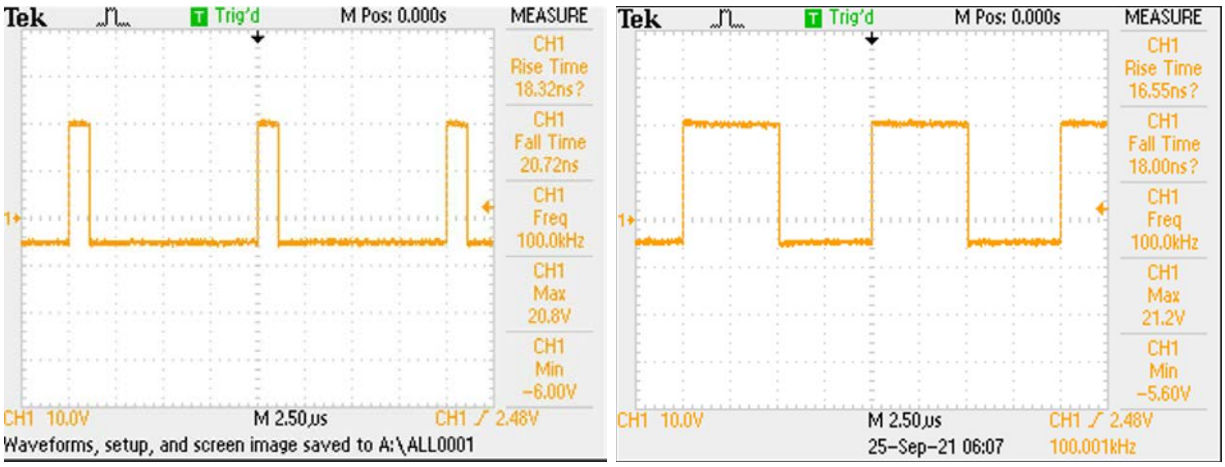
(a) (b)

Fig. 9. (a) The modified 10 kV switching module (right) and the gate driver board (left) are immersed in dielectric oil, (b) switching characteristics of the module using a voltage divider probe. The output voltage swing is 10 kV (5 kV/division).



(b) **(b)**

Fig. 10. (a) Voltage across the load, the voltage swing was 7.64 kV (b) Gate to source voltages of the four MOSFETs used in a module.



(a) (b)

Fig. 11. Modified gate driver output (a) at f = 100 kHz, D = 50%, no load, (b) at f = 100 kHz, D = 10%, no load.

The entire circuit assembly including the driver PCB was immersed in naphthenic dielectric oil to prevent any unwanted arcing through air, although the final design will use some sort of potting materials for packaging ease. The system has been tested up to 10 kV, and we are yet to test the oil's dielectric strength at 20 kV.

15.7 Summary and Recommendations

In this report, a 10 kV rated multilevel modular high-voltage switch architecture based on capacitive coupling technique and associated voltage balancing scheme have been presented, and the concept has been verified through simulation and experimental

results. The intricacies of the voltage balancing mechanism during switching transients and steady-state have been explained in a simplified manner. Criteria for critical parameter selection pertaining to the modular HV switch have been discussed with necessary details. The design of a custom high-voltage (10 kV rated) isolated gate driver to drive the modular HV switch has been outlined in this report as well. The modular HV switch coupled with the custom isolated gate driver has been tested at a supply voltage up to 10 kV and at a switching frequency up to 15 kHz in a high-side configuration with a resistive load. A maximum voltage imbalance <80 V has been recorded which is negligible compared to the breakdown voltage rating of a single MOSFET. In addition, the gate drive signals originated from the modular HV isolated gate driver exhibit little to no synchronization delay. Simulation and experimental results validate the modular approach of the proposed HV switch, thereby ushering in an intriguing way to scale up the voltage rating of an HV switch without requiring complete redesign and reconstruction.

15.8 Outputs

Graduating student: Dr. Wasekul Azad, July 2021

Conference papers:

(1) A. N. M. Azad, S. Roy, A. Caruso and F. H. Khan, “A Multilevel-Modular 10 kV Silicon Carbide MOSFET Module using Custom High-Voltage Isolated Gate Driver, Coupling, and Snubber Circuits,” 2021 IEEE Kansas Power and Energy Conference (KPEC)

(2) A. N. M. Azad, S. Roy and F. H. Khan, "A Single Gate Driver-Based Four-Stage High-Voltage SiC Switch Having Dynamic Voltage Balancing Capability," 2021 IEEE Applied Power Electronics Conference and Exposition (APEC).

Journal article:

A Custom High-Voltage Isolated Gate Driver Circuit Combined With Coupling, and Snubber Circuits for a Scalable Multilevel-Modular 10 kV Silicon Carbide MOSFET Module, submitted to IEEE Transactions on Power Electronics

Invention disclosure:

An invention disclosure with the title “A Multilevel-Modular 10 kV Silicon Carbide MOSFET Module Using Custom High-Voltage Isolated Gate Driver, Coupling, and Snubber Circuits” has been filed by UM Technology Commercialization to protect the technology.

15.9 References

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ONR HPM Program – Monthly Status Report (MSR) – January 2022

Anthony Caruso – Univ. Missouri – Kansas City

N00014-17-1-3016 [OSPRES Grant]

ONR Short Pulse Research, Evaluation and non-SWaP Demonstration for C-sUAS Study

15 FEBRUARY 2022

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OSPRES Grant Approach: A fail-fast philosophy is maintained, where if a technology or capability is deemed infeasible to be demonstrated or validated during the project period-of-performance, it shall be culled, results to date and basis of infeasibility documented, and the next major gap/deficiency area addressed by that part of the project sub-team. Students whose thesis depends on following through with a full answer during the life of the award will be given special dispensation to continue their work.

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1 Contents

2 Executive Summary

2.1 Progress, Significant Findings, and Impact

Fiber Laser and Optical Amplifiers. We improved the operating power limits of small diameter (100 micron) water-core optical power amplifiers by a factor of roughly 10—resulting in 1 GW power delivery in the core and amplification to 10 MW in the cladding—by replacing water in the core (of these simulations) with steam of a lower refractive index. This result was also enabled via a staged design in which we allow energy to be input into the core, as well as into the cladding (from a previous amplification stage). We discovered resonances in the simulated electric field distribution which could cause damage due to high peak-to-average power ratios. These normally are small but not always: for example, one observed enhancement factor of 2 over a 1 cm spot within a MW design would put us over the damage threshold rule-of-thumb of 1 MW/cm^2. We obtained a flat-top Gaussian output beam profile by increasing the core diameter to 120 microns.

On-State Resistance in GaN:X PCSS. More extensive research into sources of increased on-state resistance due to current collapse (from buffer trapping, gate instability, surface trapping, parasitic capacitance, etc.) has been done for electrically gated GaN-based devices, which will be used to identify sources of current collapse in GaN PCSS devices. Literature shows a reduction of on-state resistance of up to ~60% through the improvement of light use efficiency in GaAs PCSS by taking advantage of total internal reflection, using periodic grooves on the PCSS surface, along with altering duty cycle, providing a possible solution for improving optical efficiency in GaN:X PCSS without increasing incident laser energy.

DSRD Optimization Simulations. Experimental analysis of the DSRD inventory continues and is nearing completion along with the LTSPICE diode parameter fitting for simulation. A Tektronix 371A semiconductor analyzer is now in operation and being used for obtaining high voltage and current forward IV, reverse IV, and breakdown necessary for proper DSRD characterization experimentally and for SPICE parameter development. SmartSpice is operational and new diode models are being prepared for improved modeling and pulser simulation.

DSRD Processing and Manufacturing. A process for DSRD diode side surface passivation through the formation of a porous silicon layer has been improved, resulting in increased breakdown voltage of the diodes. After 5 experimental runs, a new process recipe has been developed. It allows us to grow much more uniform thickness passivation layers, thus improving the diode manufacturing yield from 40 to 60%.

DSRD Design of Experiments. A complete randomized block design (CRBD) experiment has been developed to directly compare testing performances of several types of DSRD diodes to pinpoint ideal diodes and pairs of diodes for pulser circuit applications. The CRBD is designed to evaluate the performances across different processing histories while reducing any unwanted effects that can influence the final result of each test. Tracking these unwanted effects is expected to lead to better diode selections for the pulser circuits, and to assist in making better recommendations for

future fabrication recipes. Previous repeatability studies have shown large variations in measured results, providing a possible explanation for inconsistencies between simulations and experimentally acquired data. Measured results of the CRBD will be evaluated once approximately 1/3 of the diodes have been tested to determine the validity of approach and if additional measurements are needed.

DSRD-Based Pulsed Power Source Optimization. Based on the simplified analytic theory we presented in the last reporting period, and considering the voltage and current ratings of the selected MOSFET, we optimized the circuit parameters for a 1×1 DSRD pulser containing four 7-stack LLNL diodes driven by a single MOSFET. The simulated output obtained from the pulser is 14 kV, which is limited by the expected breakdown voltage of 500 V for a single diode. Although the output voltage is less than the value reported before, the optimized output here is based on the true limitations on the circuit components which were not considered before. A new 1×1 DSRD pulser circuit board has been populated with the optimized circuit parameters and is being tested.

Continuous Wave Diode-NLTL Based Comb Generator. Continuous wave testing has been performed on high voltage lines up to 100 V to compare with the previously reported experimental measurements excited with a 700 MHz sinusoidal input. Pulse sharpening with rise time reduction from 370 ps to 200 ps has been observed along with frequency doubling at <10 $V_{p\text{-}p}$ excitation. However, ~65% power reflection has been noticed at the source due to impedance mismatch when excited with >50 $V_{p\text{-}p}$. The emphasis for the next reporting cycle will be on determining the root cause for the mismatch alongside demonstrating bipolar waveforms computationally.

Pulse-Compression-Based Signal Amplification. Magnetic pulse compression (MPC) is being evaluated for high frequency signal amplification. As part of the feasibility study and design efforts, magnetic core losses have been investigated. Core selection constraints have been determined based on core losses and high frequency MPC design considerations. A magnetic core with high permeability, sharp saturation characteristics, very small cross-sectional area, and very low saturation flux density is needed to maximize the operating frequency of MPC with sinusoidal input. The upper limit of the MPC operating frequency will also depend on the core cutoff frequency. In order to minimize core losses, which increase with frequency, duty cycle reduction or input signal DC shift can be utilized despite the tradeoffs.

Antennas. After achieving reasonable agreement between the measured and simulated results for narrowband, coaxial probe-fed, microstrip patch ESA elements in the UHF range (0.7–1 GHz), the design of wideband antennas, in the same frequency band, has been initiated. Preliminary results show ~26% improvement in bandwidth performance of the antenna when the standard SMA/N-type connectors are replaced by customized coaxial connectors of larger diameter.

The impedance transformer of the single element Koshelev antenna prototype has been re-fabricated to remove airgaps noticed in the previous prototype. The re-fabricated prototype yielded an improved (consistent –5 dB S11 values throughout the frequency range with no noise) S11 result at high frequencies, however the new S11 result was still not in agreement with the simulated S11 result. We are currently fabricating a sheet metal

version of the single element Koshelev antenna to create a benchmark for 3D printed versions to be compared.

On the machine learning (ML) effort, we have seen improved root mean square error (RMSE) values from KNN ML model over LR ML model for the prediction of time-domain electric field and antenna pattern. A RMSE value less than 1 is usually considered to be a good result in ML. The RMSE values are on the order of 10^{-4} and 10^{3} for KNN and LR ML models, respectively.

Reporting and Programmatic Updates. The Laser Diode Array Driver sub-project will be sunset and a summary report is provided in the Appendix. The frozen wave generator work, however, will be continued and broken out as a new sub-project in the next MSR. The Shark Antenna effort is also being sunset, with a summary provided in the Appendix. Reporting on the UAS Engagement Modeling and Simulation project has been moved to the PTERA Contract this month, and finally, reporting on the RF Coupling project will no longer be under the OSPRES Grant.

2.2 Completed, Ongoing, and Cancelled Sub-Efforts

	Start	End
2.2.1 *Ongoing Sub-Efforts*		
GaN:C Modeling and Optimization	OCT 2017	Present
Diode-Based Non-Linear Transmission Lines	FEB 2018	Present
Trade Space Analysis of Microstrip Patch Arrays	FEB 2019	Present
Enclosure Effects on RF Coupling	OCT2019	Present
Lasers and Optics	FEB 2020	Present
UWB Antenna Element Tradespace for Arrays	MAY 2020	Present
Si-PCSS Contact and Cooling Optimization	JAN 2021	Present
Drift-Step Recovery Diode Optimization	JAN 2021	Present
UAS Engagement M&S	MAR 2021	Present
DSRD-Based IES Pulse Generator Development	APR 2021	Present
Drift-Step Recovery Diode Manufacturing	MAY 2021	Present
IES Diode Characterization	MAY 2021	Present
Sub-Nanosecond Megawatt Pulse Shaper Alternatives	MAY 2021	Present
Ultra-Compact Integrated Cooling System Development	MAY 2021	Present
GaN-Based Power Amplifier RF Source	AUG 2021	Present
Reconfigurable RF Pulsed-Power Source	AUG 2021	Present
RF Driver Unit for GaN SD-MPM Power Amplifier	SEPT 2021	Present
Reconfigurable RF Antenna for SD-MPM Sources	SEPT 2021	Present
Continuous Wave Diode-NLTL Based Comb Generator	SEPT 2021	Present
2.2.2 *Completed Sub-Efforts*		
Adaptive Design-of-Experiments	OCT 2017	APR 2019
Non-perturbing UAV Diagnostics	OCT 2017	OCT 2018
Noise Injection as HPM Surrogate	OCT 2017	MAR 2019
SiC:N,V Properties (w/ LLNL)	APR 2018	MAR 2019
Helical Antennas and the Fidelity Factor	JUL 2018	SEPT 2019
Si-PCSS Top Contact Optimization	APR 2020	OCT 2020
Nanofluid Heat Transfer Fluid	NOV 2020	JUL 2021
HV Switch Pulsed Chargers	DEC 2018	DEC 2021
2.2.3 *Cancelled/Suspended Sub-Efforts*		
Ab Initio Informed TCAD	OCT 2017	OCT 2020
Positive Feedback Non-Linear Transmission Line	NOV 2017	DEC 2018
Minimally Dispersive Waves	FEB 2018	SEPT 2018
Multiferroic-Non-linear Transmission Line	NOV 2018	APR 2019
Avalanche-based PCSS	SEPT 2018	SEPT 2019
Gyromagnetic-NLTL	DEC 2017	NOV 2020
Multi-Stage BPFTL	APR 2020	JUL 2020
Heat Transfer by Jet Impingement	MAY 2018	FEB 2021
Si, SiC, and GaN Modeling and Optimization	NOV 2018	FEB 2021
Bistable Operation of GaN	FEB 2021	MAR 2021
IES Pulser Machine Learning Optimization	MAY 2021	AUG 2021
WBG-PCSS Enabled Laser Diode Array Driver	NOV 2020	JAN 2022

2.3 Running Total of Academic and IP Program Output

See Appendix for authors, titles and inventors (this list is continuously being updated)

Students Graduated	*5 BS, 8 MS, 3 PhD*
Journal Publications	*5 (6 submitted/under revision)*
Conference Publications	*33 (4 submitted/accepted)*
External Presentations/Briefings	*17 (23 submitted/accepted)*
Theses and Dissertations	*4*
IP Disclosures Filed	*10*
Provisional Patents Filed	*4*
Non-Provisional Patents Filed	*0*

3 Laser Development

3.1 Fiber Lasers and Optical Amplifiers

(Scott Shepard)

3.1.1 *Problem Statement, Approach, and Context*

Primary Problem: High-average-power 1064-nm picosecond lasers are too large (over 1100 cm^3/W) and too expensive (over \$1000/μJ per pulse) for PCSS (photoconductive semiconductor switch) embodiments of HPM-based defense systems. For example, a laser of this class might occupy a volume of 1 m x 30 cm x 30 cm = 90,000 cm^3 and provide an average power of 50 W (thus, 1800 cm^3/W). Costs in this class range from \$100K to \$300K to drive our Si-PCSS applications.

Solution Space: Optically pumped ytterbium-doped optical fiber amplifiers, fed by a low-power stable seed laser diode, can offer a cost-effective, low-weight, and small-volume solution (with respect to traditional fiber and traditional free-space laser designs). Moreover, our novel optical amplifier tubes, might operate at far higher power levels (over 1000 times greater), thus driving an entire array of PCSS with a single amplifier and thereby reducing the overall system costs and eliminating the optical pulse-to-pulse jitter constraints.

Sub-Problem (1): Optical pump power system costs account for over 50% of the budget for each laser (in this class, for normal/free-space, optical fiber, and tubular embodiments).

Sub-Problem (2): Fiber (as well as power tube) optical amplifier performance is degraded primarily by amplified spontaneous emission (ASE) noise, which limits the operating power point, and by nonlinearities, which distort the optical pulse shapes.

State-of-the-Art (SOTA): Free-space NdYAG lasers or Ytterbium-doped fiber amplifiers optimized for LIDAR, cutting, and other applications.

Deficiency in the SOTA: Optical pump power system costs (in either free-space or fiber lasers) are prohibitive for the PCSS applications until reduced by a factor of at least two.

Solution Proposed: Fiber lasers permit a pre-burst optical pumping technique (wherein we pump at a lower level over a longer time) which can reduce pumping costs by a factor of at least ten. To address the ASE and nonlinear impairments, we are pursuing the use of gain saturation and a staged design of different fiber diameters. We also apply these techniques to fiber amplifiers which incorporate our power amplifier tube in the final stage. The inclusion of our novel tubular-core power amplifier stage should permit a single laser to trigger an array of several PCSS (reducing system cost and mitigating timing jitter).

Relevance to OSPRES Grant Objective: The enhancement in SWaP-C^2 for the laser system enables PCSS systems for viable deployment via: a factor of 40 in pumping cost reduction of each laser; and a factor of *N* in system cost reductions as a single laser could drive *N* (at least 12) PCSS in an array, while also eliminating the optical jitter constraints.

Risks, Payoffs, and Challenges: Optically pumping outside the laser pulse burst time can enhance the ASE; pump costs could be reduced by 40, but ASE in the presence of dispersion and/or nonlinearities could enhance timing jitter thereby limiting steerability. The main challenge for power tube implementation is the entrance optics design.

3.1.2 *Tasks and Milestones / Timeline / Status*

(A) Devise a pre-burst optical pumping scheme by which we can reduce the costs of the laser by a factor of two or more and calculate the resulting increase in ASE. / FEB–JUL 2020 / Completed.

(B) Reduce the ASE via gain saturation. / Oct 2020 / Completed.

(C) Design saturable gain devices which avoid nonlinear damage. / Ongoing.

(D) Calculate and ensure that timing jitter remains less than +/-15 ps with a probability greater than 0.9. / Ongoing.

(E) Demonstrate a cost-reduced fiber laser. / Ongoing.

(E1) **March 2021** Finalize design. / Completed.
(E2) **April 2021** Assemble and test-check seed LD (laser diode)/driver. / Completed.
(E3) **April 2021** Measure power vs current transfer function of seed LD/driver. / Completed.
(E4) **May–July 2021** Measure ASE and jitter of 1064 nm seed LD/driver. / Completed.
(E5) **May–July 2021** Measure ASE and jitter of 1030 nm seed LD/driver. / Completed.
(E6) **June–July 2021** Assemble and test-check pump LDs/drivers. / Completed.
(E7) **June–July 2021** Measure power vs current transfer function of pump LDs/drivers. / Completed.
/ (E8) – (E14) Delayed due to vendor issues (see MAY MSR).
(E8) **September 2021** Splice power combiners to Yb doped preamp fiber. /Completed.
(E9) **September 2021** Connect seed and pumps to power combiners and test-check. / Completed.
(E10) **September–October 2021** Measure gain, ASE and jitter of 1064 nm preamp assembly (forward, backward and bidirectional pumping) as a function of pump power and duty cycle. / Partially complete.
(E11) **September–October 2021** Measure gain, ASE and jitter of 1030 nm preamp assembly (forward, backward and bidirectional pumping) as a function of pump power and duty cycle. / Partially complete.
(E12) **November 2021** Splice power amplifier and its power combiner to best preamp. / Ongoing (delay due to vendor error).
(E13) **November–December 2021** Measure gain, ASE and jitter of entire amp assembly. / Ongoing (delay due to vendor).
(E14) **December 2021** Analyze data and document. / Ongoing (delay due to vendor).

(F) Design a new type of higher power, tubular core fiber amplifier. / Ongoing.

(F1) Apply one high-power tubular amplifier to a system comprised of an array of several (say N) PCSS. For example: N=12 in a 3x4 array (or 4x4 array with corners omitted) N=16

in a 4x4 array, etc.; thereby eliminating jitter constraints and reducing laser system cost by more than a factor of 100 (independent of burst profile). / Ongoing.

3.1.3 *Progress Made Since Last Report*

(F) We continue to consider smaller diameter tubes (of 50 micron rather than 2.5 mm radius) since these would be flexible like fiber and fit the tooling of current manufacturing. Because the smaller tubes diminish the thermal benefits of a larger surface area, we consider the use of water (rather than air) in the core of the smaller diameter tubes. We improved the limit imposed by self-focusing from roughly 1/10 GW in the core and 1 MW in the cladding (of last month's MSR) to roughly 1 GW in the core and 10 MW in the cladding by allowing the water to turn into steam of a lower refractive index. This result was also enabled via a staged design in which we consider energy input to the core, as well as the cladding (from a previous amplification stage).

(F) To facilitate the optimizations (as used in the above) we added longitudinal "cut-lines" to the COMSOL simulations which yield plots of the electric field as a function of the longitudinal distance along the waveguide, in both the core and the cladding. These also revealed "hot spots" i.e., resonances which should be minimized to avoid damage from high peak-to-average field strength. Means of reducing these via anti-reflection techniques are underway and for now they add to the characterization of any particular design (as do the transverse cut-lines which characterize the output beam profile, a.k.a. beam quality).

(F1) In the HPM applications we want the output beam profile to be more uniform than Gaussian and found that we could do so by adjusting the tube parameters or by utilizing our "4-spot" entrance optics technique. The 4-spot design however resulted in sharper resonances than the staged design.

3.1.4 *Technical Results*

(F) We increased the power handling capabilities of smaller diameter power tubes, which are filled with water to compensate for the reduced thermal advantage with respect to our larger diameter air-filled designs. Water is a natural choice when designing for Si-PCSS since it has a transmission window near 900 nm where the responsivity of silicon has its peak. The index of refraction in the glass tube is $n = n_0 + \gamma I_0$ where γ characterizes the nonlinear response of the Kerr media to the optical intensity I_0, so the index of the glass is always larger than its linear component n_0, which is taken to be 1.448 at our wavelength of 1064nm. The index of refraction of room temperature water (near 1064nm) is 1.32 so the core mode is indeed confined by transverse reflections (rather than total internal reflection, TIR, since there is no critical angle for waves launched inside the media of lower index). The modes inside the higher index glass however are supported by TIR. In order to maintain these guidance conditions we chose to lower the index of the water (rather than increase it via additives) by allowing it to expand into steam. This also brings the situation closer to that of our successful air-core designs and we found good performance at a steam-core index of 1.22 as shown in Fig. 3.1.1 for the case of the input light illuminating the glass cladding only (i.e., no energy is input to the steam filled core). Therein we see a breakpoint at 3 MW (Pin.clad) yielding an output power in the cladding

(Pout.clad) of roughly the same amount (the straight line is a reference, which would result in the case of no nonlinearity, $\gamma = 0$).

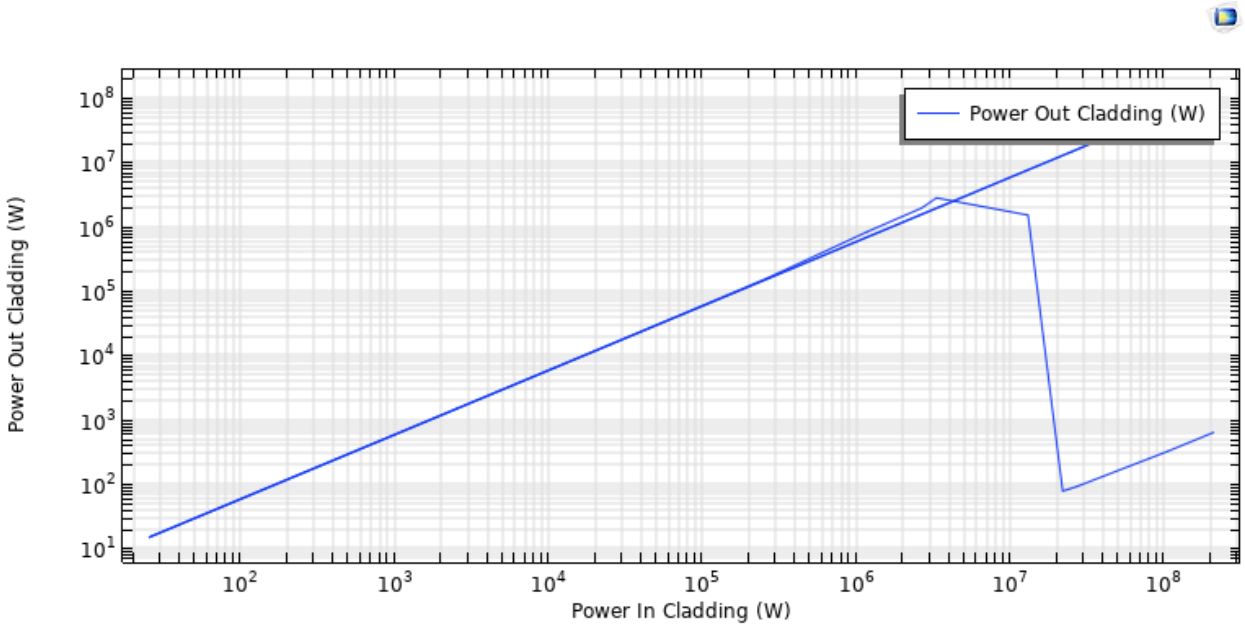

Fig. 3.1.1. Cladding output power vs operating point for illumination on cladding only.

The output power from the core of this amplifier (Pout.core) as a function of operating point (Pin.clad) is shown in Fig. 3.1.2; yielding a core output power of only 0.2 MW when operating at the above breakpoint power of 3 MW.

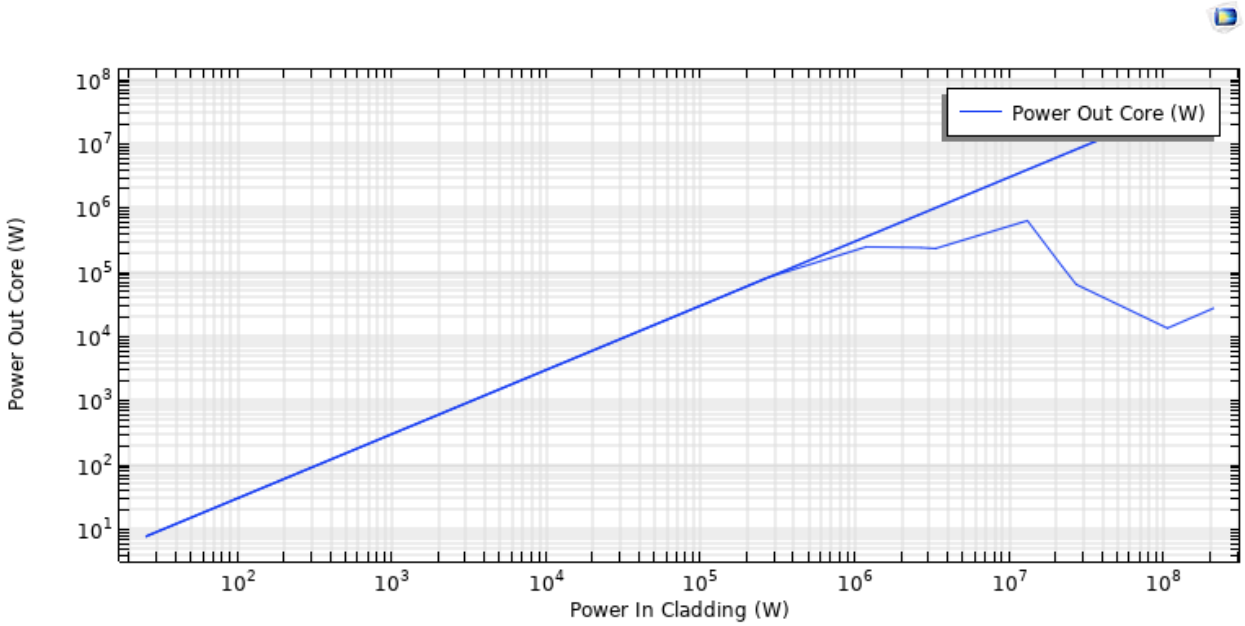

Fig. 3.1.2. Core output power vs operating point for illumination on cladding only.

If, however we allow for the input of energy into the core (as well as cladding) from a previous amplifying stage then the situation improves. Fig. 3.1.3 shows the cladding output power vs operating point curve for this case in which the breakpoint, now at roughly 10 MW, is about three times larger.

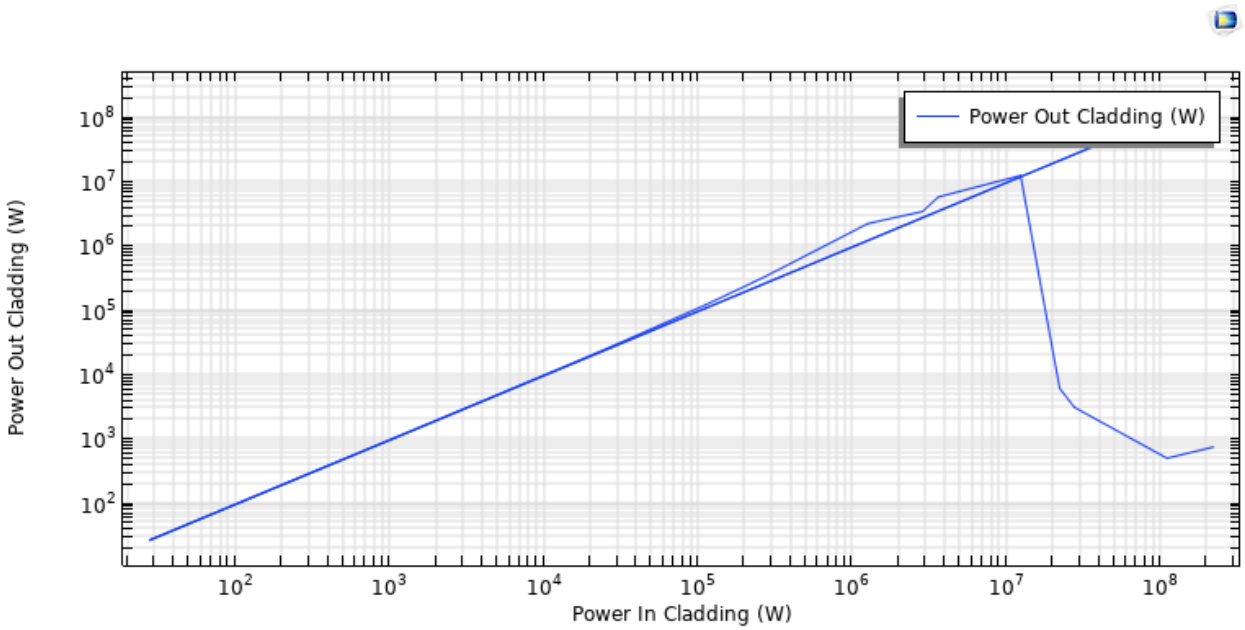

Fig. 3.1.3. Cladding output power vs operating point for illumination on both core and cladding.

Fig. 3.1.4 shows an even greater improvement in power handling capability. If we limited the operating point to the above breakpoint power of 10 MW it shows that we can deliver about 1 GW of power from the core. Indeed, any breakpoint effect here is barely observable – presumably because we still input energy into the core at the input, even when the energy coming from the cladding drops. Recall that the amplification and the nonlinearity take place within the cladding, hence operating very far above breakpoint would defeat our purpose (i.e., only power in the cladding gets amplified) but the ability to carry and accumulate high power in the core is useful. In this example (of a steam core index of 1.22, with core radius of 50 microns, and an input beam waist of 10 microns) the limitation imposed by the Kerr nonlinearity of the glass permits amplification up to 10 MW within its cladding, while also carrying 1 GW from that cladding and/or previous amplifier stages, within its core.

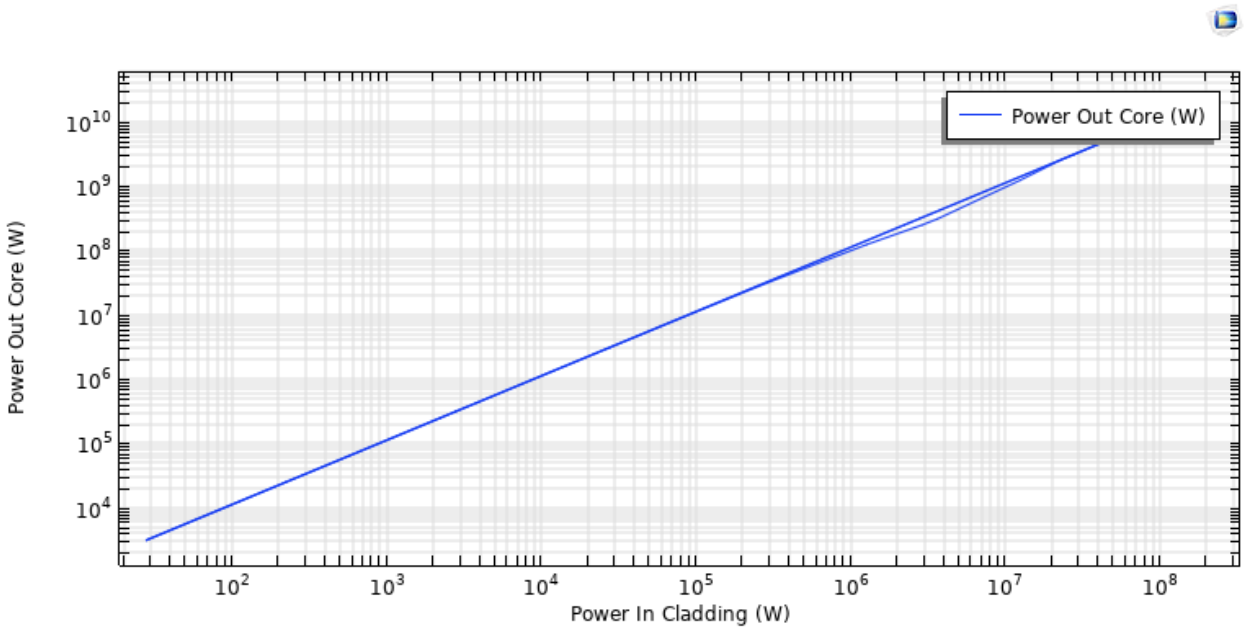

Fig. 3.1.4. Core output power vs operating point for illumination on both core and cladding.

(F) We added longitudinal "cut-lines" which yield plots of the electric field as a function of the longitudinal distance along the waveguide. These reveal instances of "hot spots" i.e., resonances which should be minimized to avoid damage from high peak-to-average field strength. In Fig. 3.1.5 we see an example (with a core radius of 60 microns) in which the resonances within the core are visible at distances of 3.3, and 6.6 (in units normalized by the linear gain parameter, g_0, so that 10 corresponds to a linear gain of 10). The units for the input intensity, I_0, are W/cm^2.

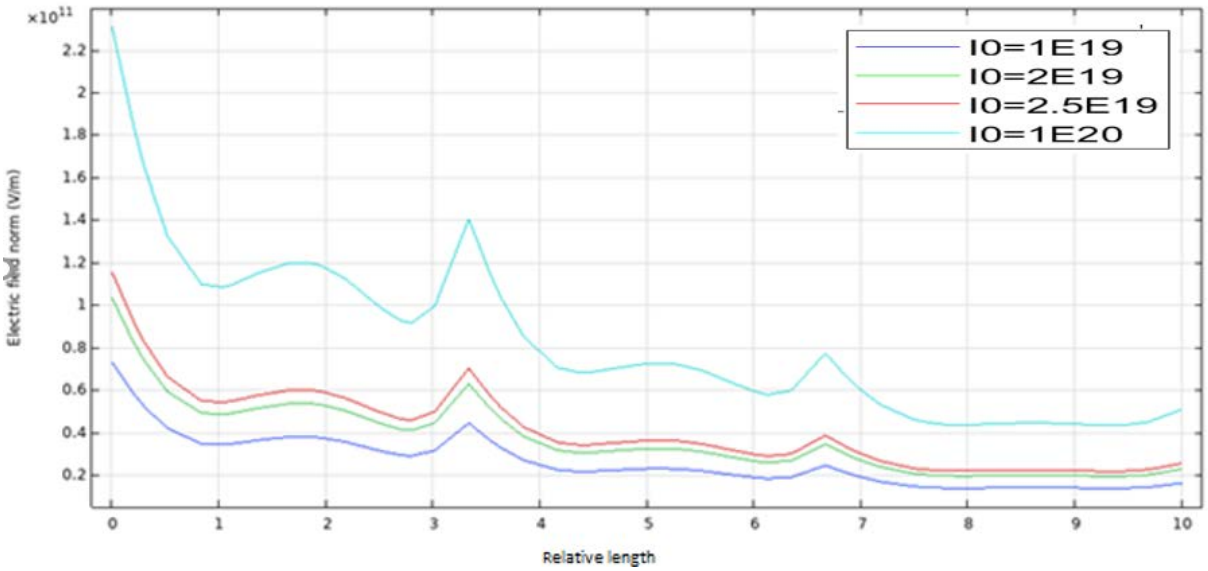

Fig. 3.1.5. Resonances within the core of a 60 micron core radius amplifier.

In Fig. 3.1.6 however, we see an example (with a core radius of 50 microns) in which the resonances within the cladding are barely visible and have moved to normalized distances of 2.5, 5, and 7.5. The source of these resonances is not yet well understood since they clearly are influenced by core radius, yet they manifest at locations which would identify them with a reflection from the amplifier's output.

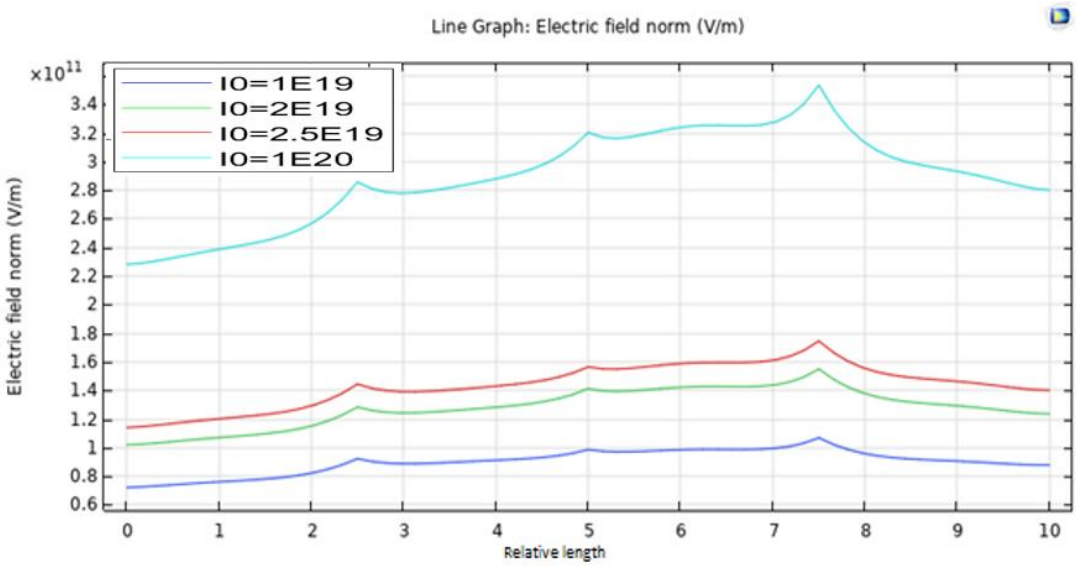

Fig. 3.1.6. Resonances within the core of a 50 micron core radius amplifier.

Means of reducing these via anti-reflection (AR) techniques are underway. The design of an AR coating at the output is complicated by its dependence on the angle at which the light exits (which is difficult to assess). Thus, multi-layer AR techniques might be required.

(F1) In the HPM applications we prefer the output beam profile to be more uniform than Gaussian. A Gaussian profile does not prohibit the HPM applications, but it would complicate the design of a passive power splitter (essentially a fiber bundle) because it would require a non-standard stacking of the power delivery fibers (with fewer fibers in the center) to achieve a more uniform split. Previously we found that we could achieve a more uniform output profile by operating slightly above breakpoint but such resulted in diminished output power. In January however we found an example of higher power resulting in a reasonably flat-topped Gaussian (for the case of a steam filled core, of index = 1.22 and radius = 60 microns) as shown in Fig. 3.1.7 (where the units for the input intensity, I_0, are W/cm^2).

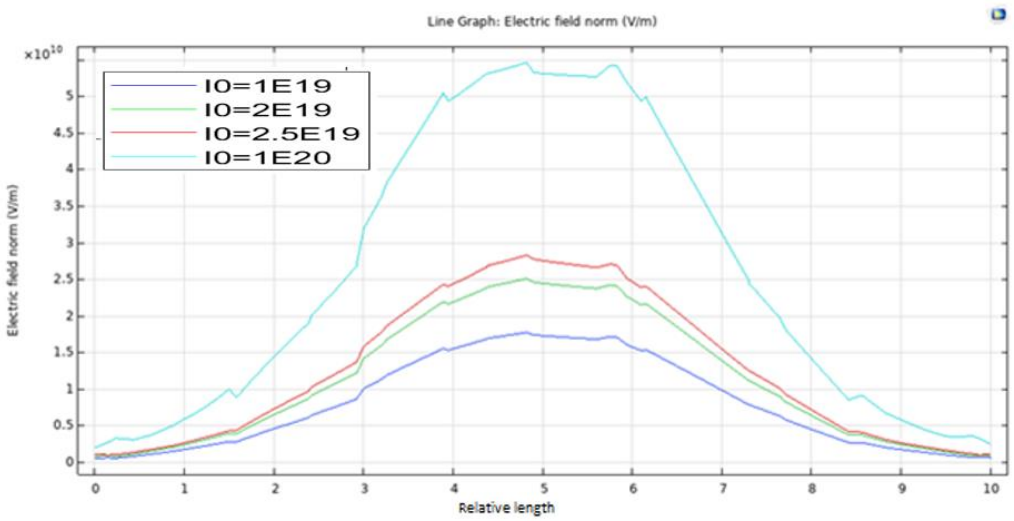

Fig. 3.1.7. Output beam profiles for a 60 micron core radius amplifier.

To this end we also considered utilizing our "4-spot" entrance optics technique. However, the 4-spot design resulted in sharper resonances than the staged design. Thus, its utility will hinge upon our development of an adequate AR technique.

3.1.5 *Summary of Significant Findings and Mission Impact*

(A) Our pre-burst optical pumping scheme simulations showed that we can drop the pump power costs by a factor of 40 with pre-burst ASE power levels below the heating level tolerance of 100 μW. UMKC invention disclosure filed 02JUN2020.

(B) For a proposed system gain of 8 million, a linear gain theory predicted the in-burst ASE would be over our heating level spec. by a factor of 3960, but by exploiting the nonlinearity of gain saturation we find that we can suppress the ASE by over 7000. UMKC invention disclosure filed 14SEP2020.

(C) Achieved initial practical device designs that exploit gain saturation, which remained below damage thresholds, via staged designs of different mode diameters NOV2020.

(D) Models of the impact of ASE on timing jitter in the presence of dispersion and/or nonlinearities were established JUL2020.

(E) The design of a proof-of-concept experiment demonstrating a cost-reduced optical pumping scheme was finalized MAR2021.

(F) We made (to our knowledge) the first observation of self-focusing effects that are not determined by beam power alone. We found instead that these can also be controlled via the geometric factors within a waveguide (such as fiber core diameter) MAY2021.

We additionally made (to our knowledge) the first observation that a mode exists in the air within a simple glass tube into which we can couple energy from the mode in

the glass. Thus, an amplifier (in the doped and pumped glass) can operate at higher powers JUNE2021.

We found conditions under which 0.25 GW of power can exist in the tube's air-core mode when its glass-cladding mode is at a power level near 0.5 GW JULY2021.

Advancements in the very high-power operating point (tens of GW) of our tubular optical amplifier (and the existence, size and spatial uniformity of its air-core mode) were shown to permit a single laser to trigger an array of several (up to 100) Si-PCSS – reducing the laser system cost and eliminating the optical timing jitter constraint. The symmetry breaking of the scattering from self-focusing in a curved waveguide was shown to enable such AUG2021.

3.1.6 *References*

[1] F. J. Zutavern, et al., "Photoconductive Semiconductor Switch (PCSS) Recovery," Distro A, ADA639129 (1989).

[2] J. S. Sullivan et al., "Wide Bandgap Extrinsic Photoconductive Switches," IEEE J. Plasma Sci., **36**, 5 (2008).

4 Photoconductive Switch Innovation

4.1 Characterizing and Optimizing On-State Resistance in GaN:X PCSS

(Heather Thompson)

4.1.1 *Problem Statement, Approach, and Context*

***Primary Problem*:** Traditionally, RF generation using photoconductive semiconductor switches (PCSS) relies on materials such as silicon (Si) or gallium arsenide (GaAs), due to their availability and low cost; however, as these applications begin to require higher operating frequencies, powers, and temperatures, with the same or reduced system form-factor, the theoretical operating limits of these materials are being reached.

***Solution Space*:** By exploiting the 3.4 eV bandgap, 1000 cm^2/Vs electron mobility, and thermal properties of GaN, it is possible to realize pulsed-power applications requiring up to a 5 MV/cm critical field, high-frequency operation, and ~400 °C operating temperature, respectively.

Sub-Problem: One of the most important problems in minimizing conduction losses, maximizing efficiency, and reducing thermal issues in compensated, semi-insulating GaN:X (i.e., GaN:X with X=C, Fe…) PCSS-based systems is achieving <1 Ω on-state resistance by optimizing the modifiable parameters of GaN:X at the material, device, and system levels, while still maintaining quick switch turn-off time and low turn-off losses.

***State-of-the-Art (SOTA*):** PCSS-based RF generation systems using Si, SiC, or GaAs can achieve MW-range output power, ones-of-gigawatts frequency content, and electrical efficiency of ~60% that require increased laser energies and device size to reach maximum efficiency and necessary operating power limits, respectively.

***Deficiency in the SOTA*:** Si-, SiC-, and GaAs-based PCSS require ones-of-mJ of incident laser energy to achieve <1 Ω on-state resistance, leading to increased incident laser requirements, increased heating in devices, and devices that are ones-of-cm^2 in area for the necessary peak power and operating temperatures.

***Solution Proposed*:** Use simulation and available experimental results, from the literature and collected results at UMKC, to optimize the variable parameters of GaN:X PCSS to achieve <1 Ω on-state resistance with increased electrical and optical efficiency while maintaining a quick switch turn-off time and low turn-off losses.

Risks, Payoffs, and Challenges:

***Challenges*:** The high cost of material leads to a limited number of devices available for experimental testing and analysis, requiring a majority of the optimization studies to be performed using simulation software (COMSOL and TCAD).

***Risks*:** Simulation results may differ from experimental results for certain PCSS parameters due to particular photogeneration and recombination parameters not being included in models along with non-ideal, real-world experiments requiring additions such as encapsulation material or other changes not fully addressed in simulation.

***Payoffs*:** By minimizing the conduction losses in GaN PCSS, a compact, tunable RF source can be realized with increased efficiency and SWAP-C^2 capabilities.

4.1.2 Tasks and Milestones / Timeline / Status

(A) Milestone – Determine material, device, and system parameters that affect on-state resistance and which of these can be best leveraged to reduce on-state losses and heating [*Estimated completion by DEC 21*].

1. Task – Literature study of photoelectric on-state resistance to understand how this parameter can be optimized to reduce conduction and on-state losses during PCSS operation *[ongoing].*
2. Task – Literature review of on-state resistance studies performed using GaN-based photoelectric devices to determine areas to further study *[ongoing].*
3. Task – Determine project milestones, tasks, and timeline for optimizing on-state resistance in GaN PCSS *[JAN 22]*.

(B) Milestone – Build model of GaN PCSS in TCAD and COMSOL to begin simulation studies *[ongoing].*

1. Task – Build simple, working GaN PCSS model that can be subsequently altered for more complex analysis of on-state resistance *[Complete]*.
2. Task – Compare simulation results with available experimental results to determine validity of models using COMSOL *[MARCH 22]*.
3. Task – Set up parametric sweep studies in COMSOL *[APRIL 22]*.
4. Task – Build a working GaN PCSS model in TCAD to determine which modeling software will provide accurate, efficient results *[FEB 22]*.
5. Task – Determine parameters that can be altered using TCAD and design studies using this program *[MARCH 22]*.

(C) Milestone – Determine device level characteristics that can be altered in simulation allowing for optimization of on-state resistance and efficiency of GaN:C PCSS and complete study on leveraging these parameters.

(D) Milestone – Determine circuit and incident photon source characteristics to be studied using simulation towards minimizing on-state resistance in GaN:C PCSS.

(E) Completion of manuscript on optimizing on-state resistance in GaN:C PCSS *[Ongoing]*

4.1.3 *Progress Made Since Last Report*

(A) Literature study of electronically gated GaN-based HEMPT and MOSFET devices shows deeper studies have been performed in minimizing on-state resistance in these devices by identifying and reducing the sources of current collapse and increased dynamic on-state resistance. Many of the same mechanisms of current collapse in electrically gated devices can be used as a starting point for identification of these sources in GaN-based PCSS devices.

Work has been done to increase the light use efficiency in GaAs PCSS devices by taking advantage of total reflection theory and altering the GaAs surface with periodic groves to increase optical efficiency of incident photons without needing to increase the necessary energy (number of photons).

(B) Simple, working model achieved in COMSOL to be altered for future parametric studies of optimizing on-state resistance in GaN:C.

Work began towards using Silvaco TCAD to simulate GaN:C PCSS material and device performance.

(C) Work on a manuscript focused on minimizing on-state resistance in GaN:C PCSS continued and will serve to direct needed simulation and experimental analysis throughout the project.

4.1.4 *Technical Results.*

(A) A large contributor to losses and decreased efficiency in GaN-based devices is dynamic on-state resistance in GaN-based HEMPT and MOSFET devices has been found to be increased due to current collapse in these devices with some reduced losses being achieved using clamping circuits thus some reduction of on-state resistance achieved through optimizing and altering the operating circuit [1].

The effects of light use efficiency, using total reflection theory, has been studied using GaAs PCSS devices, in which periodic grooves were formed on the GaAs surface and altered in size, spacing, and bevel angle towards achieving total internal reflection, allowing for increased optical efficiency of incident photons. This idea could be explored with GaN-based devices as well to increase optical efficiency without increasing the incident energy required from the photon source [2].

Work continued towards determining the tasks needed for on-state resistance optimization of GaN:C through literature review and manuscript work.

(B) Work began towards a working Silvaco TCAD GaN:C PCSS model as an alternative simulation program to use for optimizing on-state resistance and efficiency.

4.1.5 *Summary of Significant Findings and Mission Impact*

(A) A preliminary literature study of the on-state resistance of opto-electric devices began to find the parameters that affect the on-state resistance of GaN PCSS and similar devices of differing materials which will lead to the determination of what parameters can be manipulated to optimize on-state resistance in GaN PCSS, leading to a material option that provides increased efficiency and SWAP-C^2 capabilities of a PCSS-based RF generation system.

During literature review, it was found that publications in this area typically focus on vertical GaN-based PCSS devices, and this has led to the conclusion that assumptions used in evaluating vertical devices need to be studied to determine their validity in lateral devices.

Due to the minimal jitter operation and increased device lifespan, focus will be restricted to linear mode PCSS operation, which limits devices to lateral geometries.

Focus will also be placed on intrinsic carrier activation due to increased optical efficiency over extrinsic activation.

GaN and GaAs-based electrically gated devices have had more extensive work done towards minimizing and optimizing on-state resistance, including identifying common sources of loss and current collapse and utilizing clamping circuit altered to maximize efficiency.

Future work to consider for increasing optical efficiency in GaN PCSS, based off of GaAs PCSS work, using periodic groves formed in the top of the device to take advantage of total reflection theory to decrease on-state resistance without needing to increase energy of the photon source.

(B) A simple working GaN:C PCSS model was created using COMSOL which will be used towards parametric studies of optimization of on-state resistance.

Work began toward building a model of GaN:C PCSS using Silvaco TCAD as this software has been used for similar OSPRES research and offers additional capabilities to COMSOL.

(C) Work towards a manuscript based on optimizing on-state resistance in GaN:C PCSS has been started with the first version of the introduction written and currently being edited.

4.1.6 References

[1] T. Foulkes, T. Modeer, and R. C. N. Pilawa-Podgurski, “Developing a standardized method for measuring and quantifying dynamic on-state resistance via a survey of low voltage GaN HEMTs,” *Conf. Proc. - IEEE Appl. Power Electron. Conf. Expo. - APEC*, vol. 2018-March, pp. 2717–2724, 2018.

[2] L. Xiao, X. Hu, X. Chen, Y. Peng, X. Yang, and X. Xu, “Effect of periodic array on the on-state resistances of GaAs photoconductive semiconductor switch based on total reflection theory,” *AIP Adv.*, vol. 7, no. 6, pp. 1–7, 2017.

5 Drift-Step-Recovery-Diode-Based Source Alternatives

5.1 Drift-Step Recovery Diode and Pulse Shaping Device Optimization

(Jay Eifler)

5.1.1 *Problem Statement, Approach, and Context*

Primary Problem: Drift-step recovery diodes (DSRDs) and DSRD-based pulsed power systems are competitive with PCSS-based systems for HPM cUAS, with the benefit of not requiring a laser. Maximizing peak power while maintaining characteristic ns-order DSRD rise times requires optimization of the DSRD device design and pulser. Other considerations are for compactness, low-jitter, cooling required, and additional pulse-sharpening device within the pulse shaping head circuit. Additional goals for pulse repetition frequency are also to be satisfied for various applications.

Solution Space: By altering DSRD device parameters (geometry, doping, irradiation), optimize single-die and stack designs for peak power and risetime within various inductive pulser circuit topologies. Also optimize the pulse sharpening device (PSD) within the pulse shaping head circuit.

Sub-Problem 1: TCAD and SPICE models of the DSRD are inaccurate and must be improved. PSD models have not been developed.

Sub-Problem 2: Inductive pulser designs are complicated by the DSRD (and PSD) parameter variability. Use TCAD and/or SPICE models to account for variability and improve pulser design.

State-of-the-Art (SOTA): MW peak power and ns-order risetimes have been achieved in DSRD-based pulsed-power systems employing DSRD stacks for higher voltage holding and parallel lines of DSRD to increase current. PSD have sharpened DSRD pulses to 100 ps-order.

Deficiency in the SOTA: A lack of accurate TCAD and SPICE models make design of DSRD and DSRD-based inductive pulser circuit topologies (with or without PSDs) difficult to the level of tens of MW of peak power while maintaining ns-order risetime (or sharpened 100 ps-order). In addition, DSRD (and PSD) fabrication variabilities further complicate pulser design.

Solution Proposed: Develop further modeling capabilities in TCAD and SPICE for DSRD and DSRD-based inductive pulser circuit topologies to optimize DSRD and inductive pulser designs, especially for maximum peak power and minimum risetime, but also for low-jitter, reduced cooling, and compactness. Additionally, optimize pulser with PSD and pulse shaping head circuit.

Relevance to OSPRES Grant Objective: DSRD-based systems eliminate laser requirements necessary for PCSSs and are competitive in terms of thermal requirements and peak power. With sharpening, the DSRD-based systems can produce comparable risetimes. The SWaPC^2 cooling requirements of HPM cUAS systems can be solved with DSRD-based pulsed power systems, and low-jitter DSRD-based systems can be used for beam-steering in phased-arrays.

Risks, Payoffs, and Challenges: DSRD must be arrayed and staged to increase current since DSRD are limited in their ability to operate at high current densities. DSRD and PSD must also be stacked to operate at high voltages necessary for high peak power and maintain low risetimes. The stacking methods can damage dies and produce variable results in risetime and DSRD diffused doping profiles can be difficult to achieve and may require epitaxial methods. SPICE device models for DSRD are unavailable and must be developed, and questions remain about TCAD limitations for DSRD and PSD modeling.

5.1.2 Tasks and Milestones / Timeline / Status

(A) Milestone – Develop TCAD and SPICE models of the DSRD and MOSFET, respectively, that match experimental values of both the diode and circuit within 5% accuracy [*Estimated completion by AUG21*].

1. Task – Develop baseline DSRD model in TCAD [*completed JAN–APR21*];
2. Task – Develop SPICE model of DSRD within LTSPICE and SmartSpice, an automated model parameter fitting procedure, and LTSPICE and SmartSpice parameters for DSRD inventory [*Estimated completion AUG-NOV 2021 (continued effort as new DSRD arrive)*];
3. Task – Develop SPICE model of MOSFET within Silvaco [*JUL–SEP21*];
4. Task – Compare results of models developed in TCAD to the simulation values achieved using LTSPICE and experimentally (see Section 4.5) [*JUL–SEP21*];
5. Task – Incorporate parasitic capacitance, inductance, and resistance models for both single die and DSRD diode stacks (multiple dies in series) as well as for the DSRD-based pulser circuits [*discontinued after MAR–JUN21*];

(B) Milestone – Optimal characteristics of epitaxially-grown DSRD pinpointed from parametric study which produce the maximum waveform fidelity characteristics (e.g., maximum peak voltage, shortest risetime, highest dV/dt) [*Estimated completion by AUG21*].

1. Task – Determine carrier lifetime effect on risetime [*completed FEB–APR21*];
2. Task – Determine effect of including avalanche modeling on DSRD performance [*completed FEB–MAY21*];
3. Task – Determine effect of the width of outer edge contact on current density and breakdown in device [*discontinued after MAR–MAY21*];
4. Task – Model TCAD process in Silvaco Athena and Victory Process for DSRD diffused and epitaxial processes (and pulse sharpening devices) used for DSRD fabrication and DSRD device modeling [*discontinued after MAR–JUN21*];
5. Task – Determine optimal doping profile for Semiconductor Power Technologies (SPT) DSRD epitaxial designs [*completed MAY–JUL21*];
6. Task – Determine best doping profile from fabricated and optimal conceptual designs by comparing performance in the 2x2 DSRD pulser [***completed JUL21***];

7. Task – Complete DSRD performance study on epitaxial doping profile (n-side) variation manufactured by SPT in conjunction with LSRL [***completed JUL21***];
8. Task – Complete gain study for DSRD stack height and gain staging design [***completed JUL21***];
9. Task – Verify accuracy of TCAD simulations by comparing to experiment for DSRD-based pulser circuit topologies [*JUL–AUG21*];
10. Task – Perform first semiconductor opening switch (SOS) TCAD simulations for DSRD vs SOS mode of operation [SEP21];

(C) Milestone – Pulse sharpening devices developed within TCAD which improve the risetime and peak voltage of the IES pulse generator developed in Section 4.5 [***transitioned to Section 4.7 JUL21***].

1. Task – Develop preliminary pulse sharpening devices (PSD) models within TCAD [*discontinued after DEC20*];
2. Task – Develop standard PSD models within TCAD to reproduce results from published work [*discontinued APR–JUN20*];
3. Task – PSD simulated with DSRD 3-stack for more complete DSRD-based system modeling excluding only the primary switch model [*APR–JUN20*];
4. Task – Determine current carrying capacity of PSD and DSRD stacks [*discontinued MAR–JUN21*];

5.1.3 *Progress Made Since Last Report*

(A.2) SPICE Diode Model Parameter Development and Generation

Generation of LTSPICE Diode Parameters

Experimental standard diode testing data for the EG1600 diode batch was received from the testing team and LTSPICE standard diode model parameters were fit. Forward IV data used an increased 0.02 V voltage resolution (earlier 0.5 V resolution) and produced fits with the same error between experimental and LTSPICE forward IV curves as with the lower 0.5 V resolution but provides an improved forward IV curve and resulting fit. For forward IV, the IS and N parameters have distinct regions based mostly on stack size and trend in a fairly linear manner. Analysis of EG1600 parameters for CV and RRT are forthcoming.

Development of Series Resistance (RS) Diode Parameter

A Tektronic 371A semiconductor analyzer has been acquired and setup. Testing on COTS VMI High Voltage diode and inhouse custom DSRDs has begun. These measurements will provide higher voltage and current forward IV and an estimate of the series resistance (RS) of the diodes for use in SPICE simulation and experimental studies. The simplest method for extracting RS is used and serves as an estimate for RS adjustment in SPICE simulation. More rigorious RS extraction and forward IV fitting is forthcoming. Accurate measurement and fitting of RS will be required for accurate pulser SPICE simulations.

New Diode Models for SPICE Simulation and Diode Parameter Develepment

SmartSpice circuit simulation software and its diode models have been received. LTSPICE used the standard 'Berkeley' diode model which is also within SmartSpice. Smartspice also includes the Philips, HiSIM and industry-standard CMC diode models. All four Smartspice models allow adjustment of the reverse IV which has not been available in LTSPICE. The HiSIM and CMC diode models include recovery models which need to be tested for DSRD modeling and should also improve the capacitance modeling. In addition, SmartSpice may offer improved pulser simulation accuracy and convergence over LTSPICE.

5.1.4 *Technical Results*

(A.2) SPICE Diode Model Parameter Development and Generation

Generation of LTSPICE Diode Parameters

The EG1600 diode batch experimental data has been received from the DSRD diode characterization group and has begun processing and analysis (see Section 6.3) along with LTSPICE diode model parameter extraction. The fitted EG1600 forward IV model parameters (IS and N) are shown in Figure 5.1.1. Five different diode batches are shown colored and circled.

The Gen2.1 diodes have the highest N and IS, in fact most of the fittings produced about the same N since it was limited to a value of no more than 2, as is usual, but can be increased which would allow the IS parameter to decrease (the datapoints then should likely trend as with the other diode batches). The legacy 13-stack are more spread (in IS) since the devices have been tested and are older, but most of the datapoints (lighter blue) are for lowest N and IS (N is not usually decreased below 1 and is for ideal diode behavior and 2 is for recombination dominated diodes). The legacy 7-stack are also spread being older and used and have the largest spread of N and IS but most of the datapoints fall close to the other 7-stack diode batches. The EG1600 diode batch are more spread in the N and IS forward IV parameters compared to EG1500 (EG1600 has two diodes which have higher conductivity, that is, anomolous forward IV of the diode batch). EG1500 are the least spread in N and IS and fall within the other 7-stack diode regions. The N and IS parameters appear to trend together in a fairly, linear fashion and these parameters are fit together at the same time in general. Note RS is set to 0.01 Ω and IKF to 0.01 for all cases. Further results for CV and RRT are being fit.

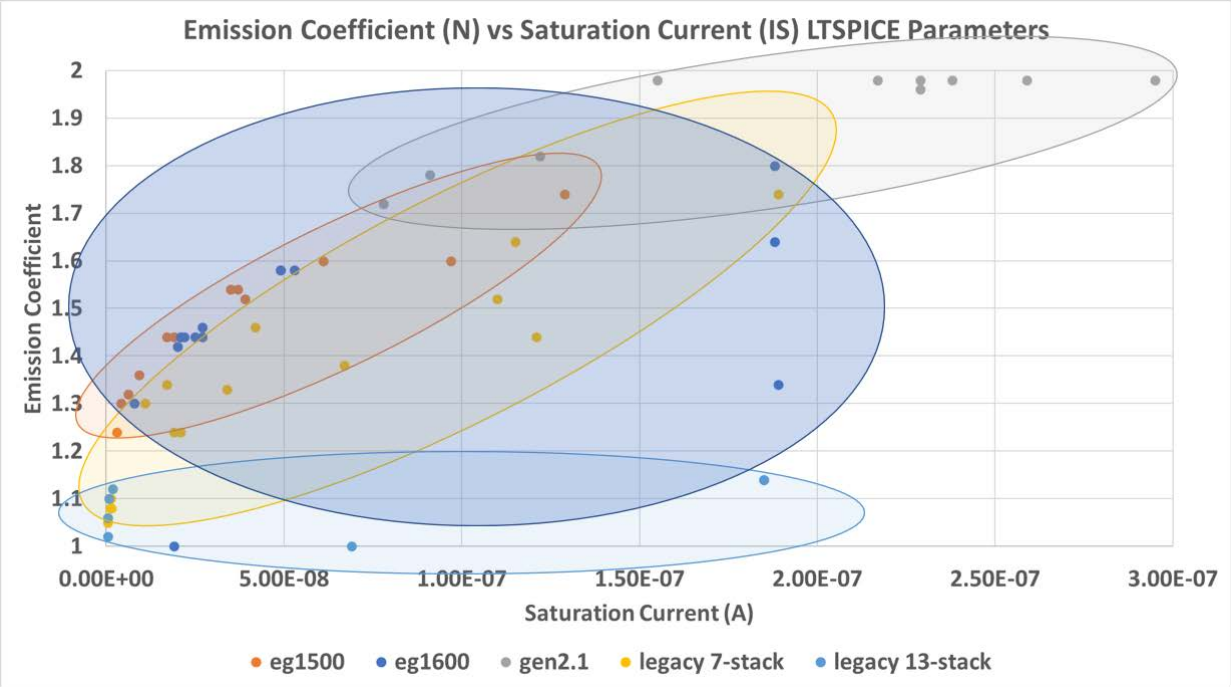

Figure 5.1.1. LTSPICE level 1 diode parameters of emission coefficient (N) vs saturation current (IS) for various diode batches circled.

Development of the Series Resistance Forward IV Diode Parameter

The forward IV experiments are used to parameterize the LTSPICE standard 'Berkeley' or Level 1 diode model (along with reverse CV and reverse recovery testing). However, the picoammeter used is current limited to 30 mA and is not capable of higher voltage and current testing associated with power diodes like the DSRDs.

A Tektronix 371A high power curve tracer (semiconductor analyzer) [10] has been acquired and setup and initial forward IV testing has begun. A VMI high-voltage diode (1N6517) [12] has been measured for its forward IV at higher voltage and current than possible in the picoammeter. Note, the picoammeter results are much more accurate in the low voltage and current region and are useful for low voltage and current characterization of the diode (likely not useful in the pulser simulations but useful in other applications). In Figure 5.1.2 a comparison of manufacturer datasheet forward IV and 371A measured forward IV is shown.

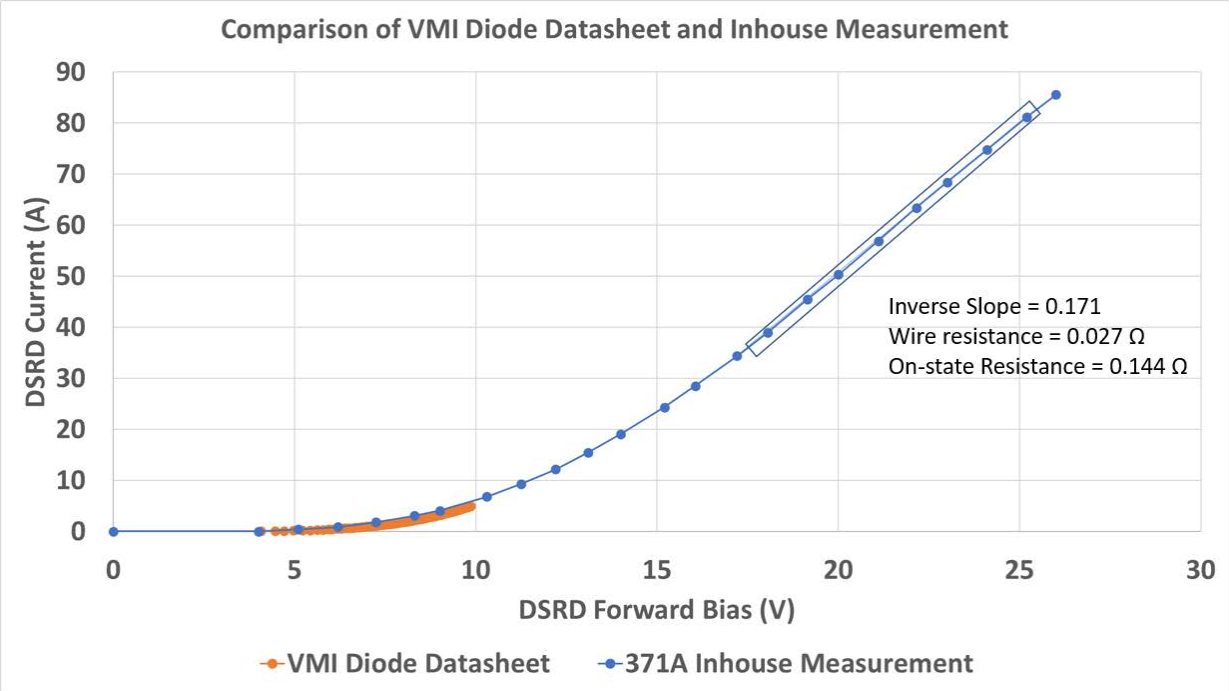

Figure 5.1.2. Experimental forward IV overlay of VMI High Voltage Diode (1N6517) Datasheet and Inhouse Tektronix 371A Measurement.

The measurements are slightly different since the datasheet is supposed to be an average of typical devices pulled from the process line, while the inhouse measurement is one device. Inhouse avergared measurements of several VMI diodes should produce a close match with the datasheet. As is typical, the inhouse measurement provides much more data. These measurements are at room temperature (25° C for datasheet and not yet measured for inhouse). Heat sinking has not yet been used on the devices and reverse IV and breakdown are still in the development stage. The inhouse measurement can be seen to become fairly linear suggestive of a series resistance.

The 371A extraction tools use the two point or inverse slope method of RS extraction (referred to more accurately as on-state resistance). In addition, the wire lead resistance was measured to be 0.027 Ω. From the inverse slope of the forward IV in its linear region, less the wire resistance, the on-state resistance is 0.144 Ω. Unfortunately, the datasheet does not provide an estimate of the on-state resistance to compare with. It would be useful to have a power diode for which the datasheet allows extraction of on-state resistance for comparison. Many methods exist for extracting and fitting the RS parameter and are under study (three-point methods, least-squares fitting, machine learning, etc.) [13-16]. The RS parameter in the LTSPICE simulation adjusts the peak load voltage and risetime within pulser simulations and must be accurately determined experimentally (forward IV) and fit correctly in the SPICE model. Currently we simply divide the measured on-state resistance by the stack height of the DSRD to obtain an estimate for RS for single diodes in the diode stack (RS and on-state resistance should not be the same number). Other methods are being explored for RS extraction, however,

in the end only the experimental and simulation forward IV need match using the correct RS (incorrect RS can lead to incorrect IS and N depending on the order of the fittin procedure).

Forward IV for DSRD EG1607 and EG1608 were obtained using the 371A semiconductor analyzer. In Figure 5.1.3, the EG1608 forward IV is shown with the two point on-state resistance extraction method illustrated. The measured on-state resistance was 0.097 Ω for this 7-stack DSRD. The single die RS parameter is then estimated at 0.014 Ω. The RS parameter is meant to include both contact and neutral region resistance within the device and can be used to include external wire resistance and high-level injection effects when not accounted for otherwise [17].

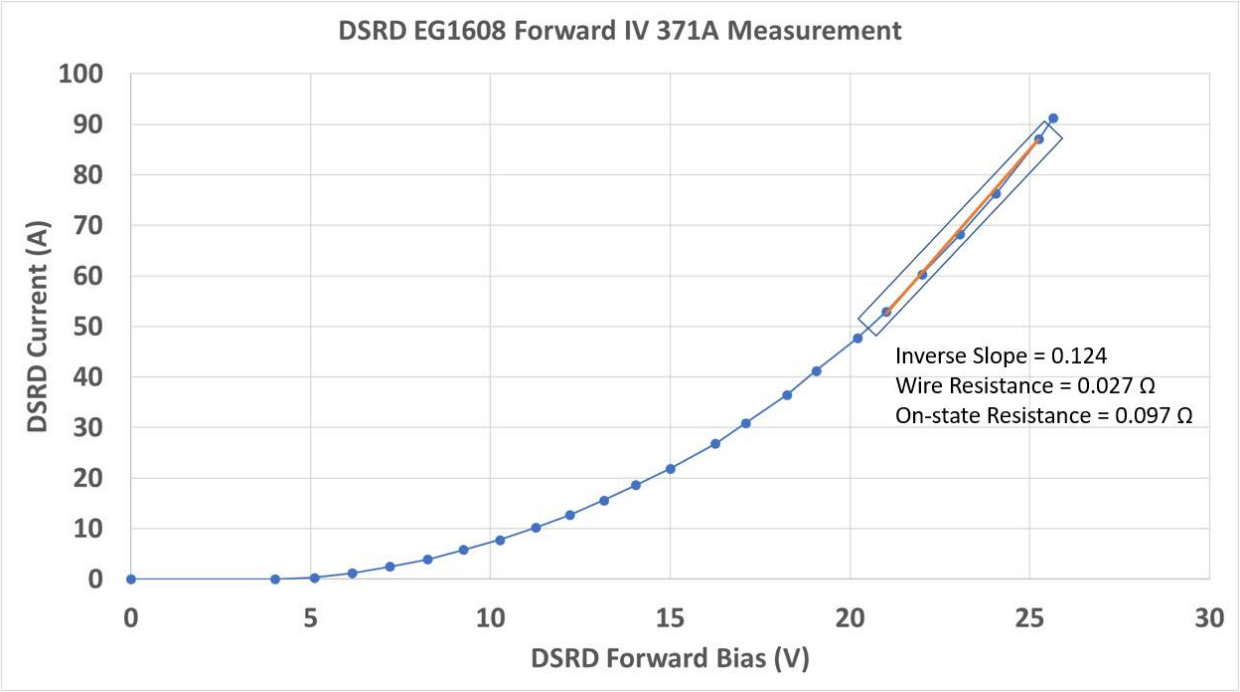

Figure 5.1.3. Experimental forward IV for DSRD EG1608 measured with the 371A semiconductor analyzer.

Further measurement studies and extraction procedures for forward IV parameters with RS are forthcoming. Once accurate RS measurements for inhouse DSRD are used within LTSPICE simulations, the accuracy of the pulser experiments and simulations can be assessed (new diode models with recovery modeling should improve the risetime and peak load voltage fitting).

From the datasheet of a Microsemi SiC MSC010SDA070K power diode [11], series resistance extracted (from the linear region of forward IV) was 0.05 Ω. For another DSRD manufacturer, a 1-stack DSRD had 0.08 Ω extracted series resistance from the forward IV. This kind of COTS power diode could be used to check the accuracy of the new 371A forward IV measurement since it has higher voltage and current measurement data (as opposed to the VMI high voltage diode).

New Diode Models for SPICE Simulation and Diode Parameter Develepment

SmartSpice [1] has been acquired and new diode models are now available. While LTSPICE [2] is a widely available free and fast circuit simulator, SmartSpice commercial simulator is highly accurate and has improved convergence. We have not yet tested the new diode models in DSRD-based pulser simulations and compared with earlier results using the LTSPICE standard 'Berkeley' diode model results.

The SmartSpice diode models include the same model available in LTSPICE, the standard level 1 extended 'Berkeley' model [2-4], but with reverse current parameter IKR that can be used to fit the reverse IV. There are three new SmartSpice diode models available: Philips, HiSIM and CMC diode [4]. All four models can be assessed in standard diode tests and pulser performance SPICE simulations, while the SmartSpice level 1 model can be compared to LTSPICE level 1 model results.

The Philips model includes physically based equations that allow modeling of detailed forward and reverse IV (and breakdown) not included in the standard level 1 model. How much this affects pulser performance and in what way has yet to be determined (higher reverse current results in higher switching losses and breakdown when it occurs can produce significant changes in circuit and device operation). The Philips model includes the same recovery and capacitance models as the standard level 1 model.

The HiSIM model does not include the same detailed modeling of forward and reverse IV but does include parameters for their adjustment similar to the standard level 1 model. The HiSIM model includes the lump-charge recovery model [5]. Initial testing has discovered the recovery and capacitance models do not appear to be working properly and is being discussed with the software vendor (Silvaco). Once the model is working properly, it may be that the HiSIM is adequate and computationally less expensive than other models for recovery (for example the CMC diode).

The CMC diode model [4,6,7] has been developed by the compact modeling committee as an industry standard diode model since so many diode models have existed and are in use. The model includes detailed forward and reverse IV modeling similar to the Philips diode model but taken from the juncap2 model [8,9]. The capacitance modeling has not been assessed well but initially appears to correctly operate. Also, an improved recovery model for diodes has been included in the CMC model. The CMC diode model is still under study as the information resources are scattered between documents and often poorly written.

SmartSpice contains Verilog-a modeling capabilities that should allow for the programming of custom diode models from TCAD DSRD studies and models in the the literature. The CMC diode model may be adequate to describe the DSRD within standard diode testing and pulser experiments, but a custom diode model or modifications to existing diode models may be required. One area of interest is a more detailed reverse capacitance model for accurately matching CV curves. The forward CV measurements and modeling are more problematic.

5.1.5 *Summary of Significant Findings and Mission Impact*

DSRD TCAD simulation started by replicating published TCAD DSRD results and then simulating devices similar with actual in-house DSRD. The variation of the sinewave pulse voltage input magnitude and period on DSRD charge storage were collected. Charge storage timing (when the diode empties charge stored from forward pulsing) of ~50% was achievable with sufficiently long voltage input period which is necessary for maximum reverse current cutoff.

DSRD stacks, as opposed to individual die DSRD, were simulated showing reduced risetime from single die to 5-stacked DSRDs consistent with published and earlier in-house data. Series resistance to model metal resistance between DSRD in stacks and doping variability in stacks was also modeled in TCAD showing metal resistance must be large to have an impact on peak voltage and risetime and that doping variations proportionally effect risetime.

(A.1) Accurate DSRD TCAD models have been developed that include both carrier-carrier scattering and Selberherr breakdown and are suitable for DSRD operation below the dynamic breakdown threshold. Peak voltage and risetime were limited by the breakdown model and more closely match experimental pulse data.

(A.2) A new DSRD LTSPICE model has been developed following the method used for developing a TCAD SPICE MOSFET model and by matching too experimental standard diode tests. The forward I-V and reverse C-V have been well matched using a 7-diode model for a 7-stack DSRD, as opposed to using only a 1-diode model for all DSRD stack heights. The reverse I-V and forward C-V are generally more problematic to fit to and proved to be so. More research and effort will be necessary to improve these matches and understand the impact on pulser simulation. The reverse recovery experiments have also been well matched (even for a single transit time over different reverse recovery testing voltages) and complete the matching of all the standard diode tests. New diodes are arriving and being tested and parameterized and tested in simulation and compared with experiment. Pulser performance has been difficult to assess due to the experimental data gathered thus far. The new DSRD LTSPICE model will also enable improvements in the TCAD SPICE MOSFET model. Overall, the new DSRD model represents a vast improvement over the previous model but has yet to include breakdown effects possible in the TCAD DSRD model and therefore breakdown limits of DSRD operation. A new automated fitting procedure now allows the model parameters to be more closely and quickly fit, has been used to fit various batches of different DSRD, and has used averaged curves (for improved measurement) when available. New Smartspice diode models have arrived and can provide for improved reverse IV, breakdown and recovery modeling, as well as, SmartSpice may improve the accuracy and convergence of pulser simulations. A 371A Tektronix semiconductor analyzer has been acquired and used to measure higher voltage and current forward IV (necessary for RS parameter development in SPICE models). Measurements for reverse IV and breakdown with the 371A are forthcoming.

(A.3) Work on TCAD SPICE MOSFET models has been done for the primary switch model (MOSFET) with conversion of the code to TCAD SPICE being partly completed to allow for modeling the complete DSRD-based pulser system (except driver). However, the conversion to TCAD of the MOSFET primary switch model, developed by CREE, to TCAD SPICE is complicated by having to develop custom behavioral models in TCAD SPICE which would be high-risk. Instead, a published model usable in TCAD SPICE was implemented and fit to the datasheet and then tested in a DSRD pulser simulation. The new MOSFET SPICE model usable in TCAD showed improvement in not having a first output pulse peak that was higher. This higher pulse had occurred in the TCAD MOSFET model (not SPICE model) and had not occurred in the voltage-controlled resistor MOSFET model (inaccurate model). Further refinement and testing of the new MOSFET SPICE model for use in TCAD has been more closely fit with the Cree LTSPICE model and compared to the Cree datasheet. The model can also be adapted to a new MOSFET in use within current DSRD pulsers. Further fitting can still be accomplished and matching both the Cree datasheet and LTSPICE model for gate charge and switching characteristics can be completed with more research into the test circuits used which are commonly not well explained in datasheets.

(A.4) LTSPICE, TCAD and experiment have been compared for the single bar pulser using a 7-stack DSRD, however there is some discrepancy for these experiments with earlier experiments (which the LTSPICE and TCAD simulations match better with) most likely due to the variability in DSRD and some to the new DSRD switch integration used for ease of switching out DSRD of various stack heights and combinations. As more experimental data is acquired for the pulsers the comparisons with simulation will yield more useful results. The 2x2 DSRD pulsers have been compared to TCAD simulation incorporating the latest TCAD SPICE MOSFET models showing some similarities in predicted peak voltage and risetime, but the most significant result is the matching of the experimental optimum trigger duration of 340 ns with TCAD results. LTSPICE simulations have been performed with the new DSRD LTSPICE models and show the standard diode model used can match experimental peak voltages and risetimes but only by adjusting mainly the CJO parameter. Without adjustment there is considerable error in simulated results. Better diode models exist that incorporate impact ionization effects and recovery time modeling the latter of which circumvents CJO adjustment. With further experiments and simulation refinement it is expected that the models will be predictive of experiment within the quality of the experimental data and models used. Some inconsistency between computers for LTSPICE, having to do most likely with convergence in the pulser simulations, is being studied for the 2x2 and 4x2 DSRD-based pulsers.

(B.1) DSRD risetime performance was collected from TCAD simulations for variable carrier lifetime. Changes in lifetime had no significant effect on risetime other than the output pulse starting earlier.

(B.2) DSRD peak voltage and risetime were simulated in TCAD to include avalanche modeling or not. TCAD avalanche models limited peak voltage and risetime at the

load over a range of voltage input magnitudes. A TCAD parameter study for DSRD stack height and DSRD area for several doping profiles with and without avalanche modeling was performed (Spring 2021 UMKC OSPRES Grant Review and Technical Exchange). The avalanche model and model parameters were also modified to account for dynamic breakdown rather than static and then compared to the no avalanche case and experimental data. From the improved avalanche modeling and TCAD parameter study, the optimal area of the DSRD can be obtained. However, for the 500 V voltage input magnitude used, the DSRD output were all in breakdown and are not predictive of non-breakdown behavior. Future studies for optimal area will include a range of voltage magnitudes to study DSRD performance and breakdown.

(B.4) TCAD process and device modeling for the development of process steps and their resultant doping profiles and device operation was begun. This modeling will enable a connection between the fabrication parameters and the device operation for DSRD (and PSD).

(B.5) Exponential doping profiles were shown (via TCAD) to outperform Gaussian and error function profiles slightly. Exponential profiles have an optimal minimum doping of 5×10^{13}–$1x10^{14}$ dopant atoms/cm^3, while Gaussian and error function profiles have an optimal minimum doping of 1×10^{13}-5×10^{13} dopant atoms/cm^3. Further exponential doping parameter studies were carried out in circuits A and B of Figure 4.2.1 (see JUN 2021 Grant Report) which included a broader doping parameter space for minimum doping, junction placement, basewidth and peak doping over a wider range of voltage input magnitudes (for breakdown limitations). The results are similar to before and show the optimally performing doping profile has a minimum doping of 5×10^{13}, no basewidth, junction placement of 95 µm, and peak doping of 1×10^{18} (p-side) and 1×10^{19} (n-side) dopant atoms/cm^3. A comparison was made for the optimal exponential doping profiles to optimal error function, LLNL and SPT DSRD designs within the 2x2 DSRD pulser system. The TCAD study showed the exponential doping profile performs the best overall when considering peak voltage, risetime, voltage riserate, maximum reverse current, FWHM pulsewidth, prepulse and gain. Epitaxy designs with realistic deviations from the ideal exponential profile from the SRP data were shown in TCAD to not significantly affect the performance.

(B.7) A more complete gain study for varying prime voltage input and stack height was completed. The results show a variety of considerations must be made for determining the better stack heights to use in DSRD pulsers. The design of the pulsers can be improved when considering the gain staging in multi-staged DSRD pulsers as caused by the DSRD stack heights used. The 7- and 13-stacks showed the best gain. However, the peak voltages were best for the 13-stack while the 26-stack required unrealistic MOSFET currents to achieve its maximal peak voltage (or gain). For gain per die within a DSRD stack, 1-stacks showed the best gain per single and showed that gain ‘efficiency’ drops with stack height. Still, higher 7- and 13-stacks had the highest gain. How best to use this new data for DSRD pulsers is under discussion.

(B.10) First semiconductor opening switch (SOS) TCAD simulations have been performed for demonstrating a hgiher current density mode of operation. Future SOS TCAD simulations can help delineate the difference in DSRD and SOS for current density snappy recovery according to doping profile and mode of device operation.

(C.1) Pulse sharpening has been verified for PSD devices for the standard design and another non-conventional design. The PSD was also modeled within a DSRD-based pulser circuit combining for the first time TCAD modeling of both DSRD and PSD together within the same circuit with only the primary switch model not included.

(E) DSRD pulser circuits for the single-bar (Circuit B of Figure 4.2.1) and 2x2 (circuit C of Figure 4.2.1) have been simulated within TCAD allowing the use of a TCAD DSRD model, whereas in SPICE no accurate DSRD SPICE model is available. Currently, the primary switch MOSFET is modeled in TCAD, as well, but SPICE models can also be developed for the SPICE within TCAD as and will allow for better use of computational resources within TCAD. The MOSFET model and pulse repetition are being studied in detail to more closely match experiment and TCAD.

5.2 Pioneering Drift-Step Recovery Diode Processing and Manufacturing

(Alex Usenko)

5.2.1 *Problem Statement, Approach, and Context*

Primary Problem: DSRDs have not increased in performance since the 1960's due to reliance on deep diffusion manufacturing. Their voltage-to-risetime, dV/dt, remains about 10^{12} V/s. To achieve the 10^{13} V/s (10 kV/ns) voltage-to-risetime required by an all-solid-state HPM pulse generator in support of the Naval afloat mission, improving DSRD manufacturing techniques is critical.

Solution Space: Leverage applicable concepts from the mainstream silicon chipmaking industry and apply new manufacturing methods to DSRD processing.

Sub-Problem 1 – Diode silicon surface termination/passivation: The SOTA uses diode termination by a vertical wall. This design results in low breakdown voltage as it is limited by surface breakdown. To increase the diode breakdown voltage to closer to that of the bulk silicon breakdown voltage value, the vertical side wall design must be avoided.

Sub-Problem 2 – Stacking of DSRD dies: The SOTA is based on soldering of diode dies into a stack, which limits the stack lifetime to below 10^{12} pulses. Also, the SOTA did not apply the methodology of stacking wafers first, then cutting into dies. Switching to wafer level stacking will decrease the number of stacking operations by more than 100x.

Sub-Problem 3 – Packaging of stacked dies: *The* SOTA uses bare stacked DSRDs. Mounting the bare stack into a press-pack type package will improve long-term stability, such that the stack will survive a much higher number of pulses before it burns out.

State-of-the-Art (SOTA): In a recently published paper (2019),[1] the Russian St. Petersburg team at the Ioffe institute reported achieving a peak current density of 5 kA/cm^2 with a rise time of the output pulse front of ~2.3 ns, and a peak voltage across the load of 900 V (i.e., the peak switching power is 4.5×10^6 W/cm^2). The St. Petersburg team utilized deep diffusion technology. A competing team at Ekaterinburg, Russia [2] reports similar pulse performance. Both teams use outdated deep diffusion technology. As one can see, there has not been any significant improvement in DSRD pulse performance since the pioneering work done in 1960 [3].

Deficiency in the SOTA: First, no DSRDs have been manufactured using epitaxy technology with doping profile optimization. Second, no DSRD processing method exists that integrates side passivation with silicon dioxide. Finally, an acceptable DSRD stacking process has yet to be developed.

Solution Proposed: Manufacture DSRDs within the continental United States using an epitaxial growth process leveraging the optimal characteristics (e.g., doping profile, carrier concentration) determined through the work performed in Section 6.1 and through working with industry partners at Semiconductor Power Technologies (SPT), Livermore Semiconductor Research Laboratories (LSRL) and Lawrence Livermore National Laboratory (LLNL – Voss Group).

Relevance to OSPRES Grant Objective: DSRD manufacturing technology is a major building block of short-pulse high-peak-power defense systems. Our new disruptive process flow for DSRDs enables not only manufacturing of DSRDs at scale, but within the continental United States (CONUS). In doing so we will redefine the SOTA by producing optimal DSRDs. Further, DSRDs will be used within best-in-class HPM pulse generators which become part of more advanced defense systems within the Navy arsenal.

Risks, Payoffs, and Challenges:

Risks: As the process of producing DSRDs using epitaxial growth with doping profile design is novel, uncharted territory, there is inherent risk to its success. Additionally, post-processing methods based on the discussions provided in the ***Sub-Problems*** section are not well-established.

Payoffs: Replacing traditional deep diffusion technology with a new process integration scheme would allow better DSRD pulse performance. Electrical breakdown voltage, reliability, and lifetime are expected to increase, and rise time on a load is expected to decrease.

5.2.2 Tasks and Milestones / Timeline / Status

(A) Milestone – Produce epitaxial DSRDs that contain optimal exponential doping profiles and carrier concentrations /estimated MAR22.

1. Task – Design of experiment on 25 wafers through negotiations with vendors / *MAY–JUL21* / Completed
2. Task – Perform DSRD stack epitaxy on 13 wafers at SVM Inc., and 25 wafers at LSRL / *JUN–AUG21* / Completed.

3. Develop process integration scheme that uses epitaxy instead of deep diffusion / *JUL–OCT21 /* Completed.
4. Compare traditional DSRD technology and suggested integration scheme. List disadvantages of traditional processes and define potential advantages of new processes / MAY–NOV21 / Completed.
5. Run Gen2 and Gen3 lots. Gen2 is on wafers with epi from SVM, Inc., Gen3 is on wafers with epi from LSRL. Gen2 uses the same BEOL as Gen1. Run BEOL of Gen3 – using our new patented processing scheme – Si_3N_4 masking, TMAH etch, oxidation, selective electroless metal deposition, wafer bonding, sawing into diode stacks / OCT–MAR22.
6. Submit Gen2 and Gen3 diode lots to UMKC team for pulsed performance measurements; collaborate with team on determining optimal doping profile through DoE (design of experiments) analysis by Minitab software / OCT21–MAR22.

(B) Milestone – Develop diode separation technique while keeping wafer integrity / Estimated completion FEB22.

1. Design lithography masks for short loop experiment, submit order to vendor. / MAR–APR21 / Completed.
2. Design short loop experiment for V-groove etching for diode separation. / MAR–APR21 / Completed.
3. Run short loop experiment for the diode separation by anisotropic etch; analyze results / MAY–OCT21 / Completed.
4. Based on results of previous short loop run, adjust equipment, and process recipes to achieve sufficient etch uniformity across the wafer. Run on updated equipment and recipe to prove etch uniformity. / Estimated JAN22.
5. Design lithography masks for epi DSRD run; submit order to vendor. / OCT21 / Completed.
6. Run Gen3 lot through V-groove etch step, transfer lot to next process step. / Estimated JAN22.

(C) Develop Ohmic contact deposition technique integrable with epitaxy, diode side termination/passivation, and wafer bonding steps / estimated AUG–JAN22.

1. Design short loop experiment to determine technical feasibility of selective electroless deposition of metal stack as a method of Ohmic contact forming in the DSRD process integration scheme. / OCT21 / Completed.
2. Determine vendor from which to order electroless deposition kits; obtain quotes, order, receive the kits. / OCT21 / Completed.
3. Run short loop experiment – nickel-copper-tin stack electroless deposition on a blanket wafer. Analyze results. / DEC21 / Completed.

4. Develop process recipe for the metal stack deposition to use in Gen3 DSRD lot manufacturing / estimated JAN22.
5. Run the selective metallization step on Gen3 lot; transfer the lot to next processing step. / Estimated FEB22.

(D) Develop wafer stack bonding technique integrable with the rest of Gen3 process flow / estimated SEP–FEB22.

1. Design short loop experiment for bonding 2 blanket wafers with Ni-Cu-Sn layers by solid–liquid interdiffusion. / SEP21 / Completed.
2. Run 2-wafers short loop experiment. Analyze results. / Estimated OCT–FEB22.
3. Test technical feasibility of multiple wafer bonding by bonding 10-wafer stack / estimated FEB22.
4. Upon proof of technical feasibility of 10-wafer stacking, develop process recipe to use for processing of Gen3 DSRD lot / estimated FEB22.
5. Run wafer bonding step on Gen3 lot, transfer the lot to next processing step. / Estimated MAR22.

(E) Develop wafer stack sawing technique into DSRD stacks, integrable with the rest of Gen3 process flow / estimated NOV–FEB22.

1. Design sawing process using Disco saw available at Semiconductor Power Technologies for cutting 10-wafer stack / estimated JAN22.
2. Run short loop cutting of blanket bonded 10-wafer stack. Analyze results. / Estimated FEB22.
3. Develop process recipe for Disco saw tool to use for Gen3 lot. / Estimated FEB22.
4. Run sawing step on Gen3 lot / estimated FEB22

(F) Develop diode side passivation process integrable with the rest of DSRD process flow.

1. Test compatibility of thermal oxidation for the diode side passivation with preceding anisotropic etch step / estimated FEB22.
2. Alternative diode side passivation process: design short loop experiment on room temperature oxidation by forming porous Si film and oxidizing the porous film / APR–OCT21 / Completed
3. Run part of Gen3 lot using the oxidized porous Si as diode side passivation / estimated FEB22.
4. Second alternative diode side passivation process: Design short loop experiment on room temperature oxide deposition from oversaturated fluorosilicic acid / estimated MAY–JAN22.

5. Run part of Gen3 lot using the oxidized porous Si as diode side passivation / estimated FEB22.
6. Choose the best from 3 methods of diode side surface passivation techniques / estimated FEB22.

(G) Develop a DSRD process based on out-diffusion (opposite to traditional in-diffusion process).

1. Process Gen4 lot based on process integration scheme described in our patent application filed in / estimated FEB22.

(H) Find vendor that manufactures press-pack parts, order the parts, and encapsulate the DSRD stacks into the press-packs / estimated FEB22.

5.2.3 *Progress Made Since Last Report*

(A5) Gen3 lot fabrication. Wafers are at lithography step. Attempt to replace lithography by mechanical sawing that removes part of mask failed. RIE tool needed for Si3N4 selective etch in our lab is still down. Therefore, the lot has been sent to outside vendor Noel Technologies for lithography and nitride etch in windows. The lot is expected to be back by the end of February.

(A5) Several more wafers from the 13-wafer Gen2 lot were fully processed. Non-stacked DSRDs were manufactured.

(F3) The process recipe for forming porous passivating layers has been significantly improved. The issue of thickness non-uniformity of the porous (stain) film has been resolved.

5.2.4 *Technical Results*

(F) **Diode side passivation development.** In the previous development run, described in last month's report, we observed the successful growth of a porous silicon film by processing in a 1000:1 mixture of concentrated hydrofluoric and nitric acids (Fig. 5.2.1). However, the porous film had a very motley colorful appearance, as shown in Fig. 5.2.2 where a control sample from a current run is imaged. The color variations across the wafer indicate heavy thickness non-uniformity of the film. The image also shows the major reason for non-uniformity: hydrogen bubbles. H_2 is a byproduct of the reaction, which forms bubbles. The bubbles remain stuck to the wafer surface, thus locally masking the surface. Therefore, the goal of the current run was to improve thickness uniformity—by modifying the etching recipe—to release the hydrogen bubbles from the surface quickly, so the bubbles do not achieve such a large size.

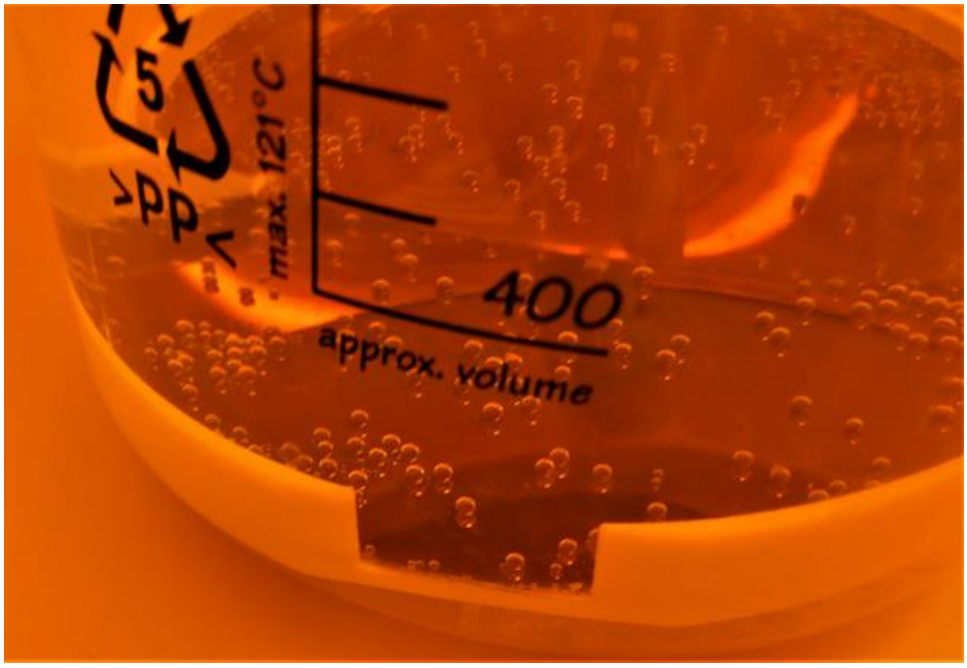

Figure 5.2.1. Control sample: wafer in beaker with 1000:1 HF/HNO_3 mixture. The hydrogen bubbles stuck to the wafer surface are clearly visible.

The average size of the hydrogen bubbles visible in Fig.5.2.1 is about 2 millimeters. This results in a drastically non-uniform porous Si film on the processed wafer, as evidenced by the assorted colors across the wafer.

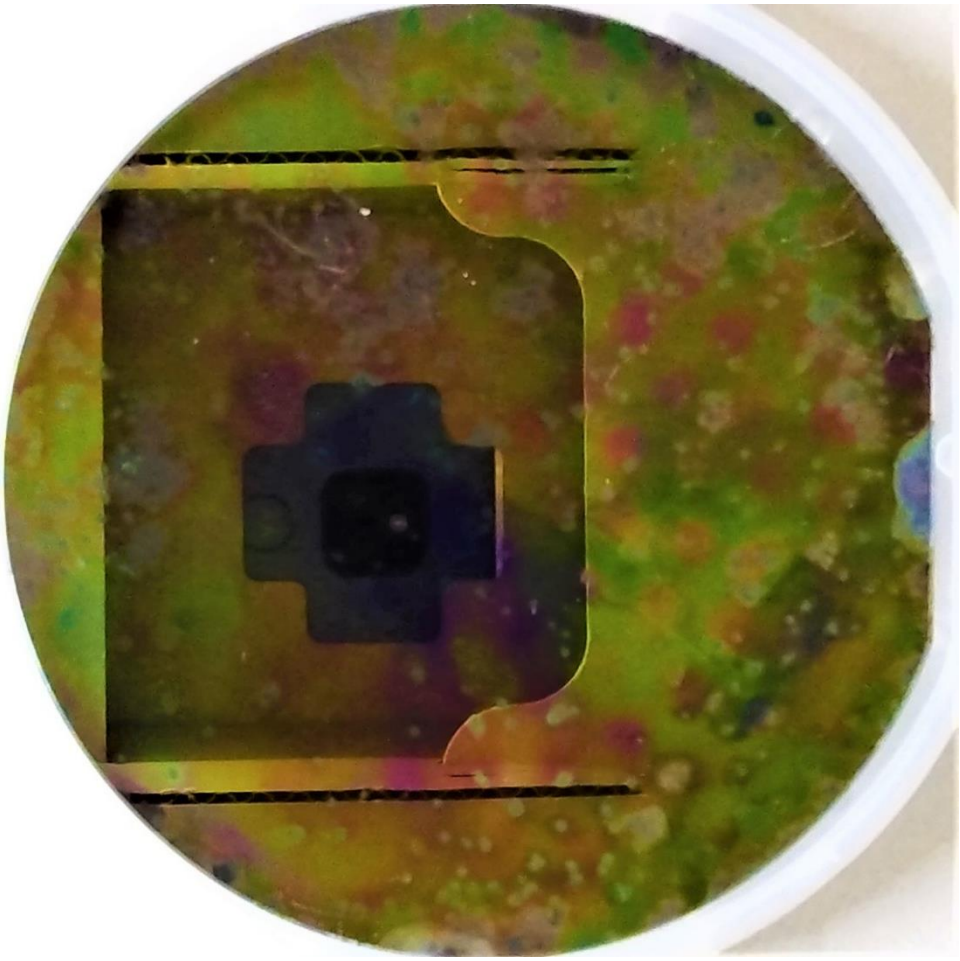

Figure 5.2.2. Appearance of porous Si film on control wafer processed in 1000:1 mixture $HF:HNO_3$.

The sticking force of the hydrogen bubbles to the surface is a capillary force between the Si and bubble surface. The capillary force is proportional to the surface tension of the liquid. In this water/HF/HNO_3 mixture, all components are polar molecules thus having high surface tension. To suppress sticking, we tried to add to the initial 1000:1 recipe either surfactant or low polar organic liquid. Triton-100 was used as the surfactant, and acetic acid was tried as an agent to lower surface tension.

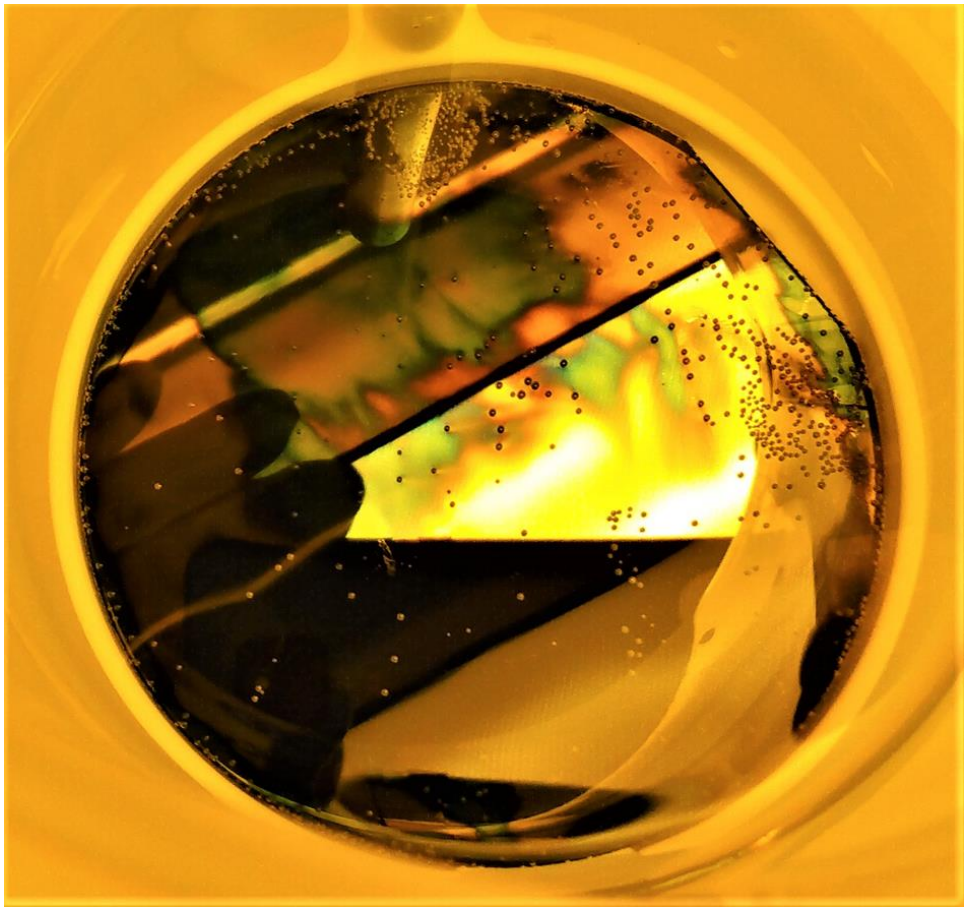

Figure 5.2.3. Hydrogen bubbles stuck to wafer surface in 1000:1 HF:HNO_3 recipe modified with a few drops of Triton-100.

As evident from Fig.5.2.3, the surfactant addition has limited the effect of bubble sticking. The average size of the bubbles is about 1 millimeter; thus, the bubbles get released faster than in the unmodified 1000:1 mixture, but it is not enough to obtain a final uniform porous Si film. The typical appearance of a wafer processed in the Triton-modified etchant is shown on Fig.5.2.4 and confirms significant non-uniformity.

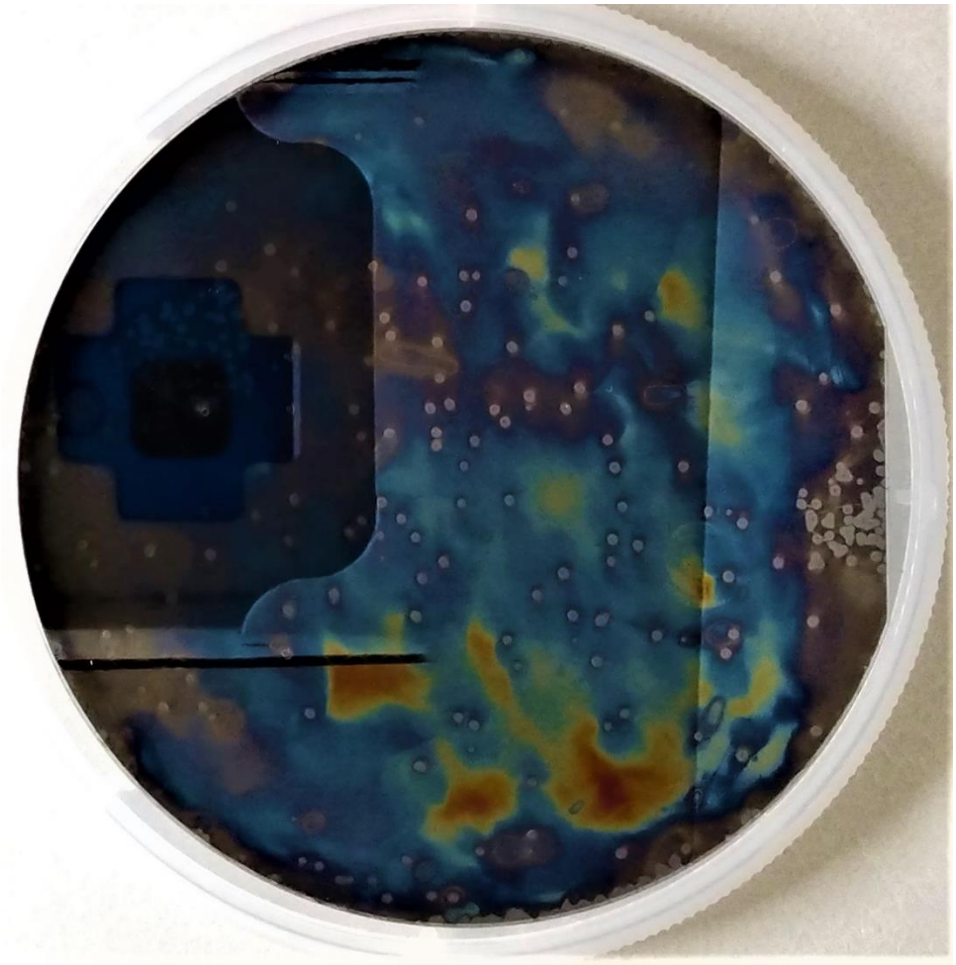

Figure 5.2.4. Stained wafer after processing in Triton modified etch.

For testing acetic acid on the etch uniformity, a HNA (HF/nitric/acetic) mixture 1000:1:1000 has been prepared. Glacial acetic was used. Fig.5.2.5 shows that during the etching no stuck bubbles are visible. The image does not catch what was observed by the naked eye: small chains of bubbles popping-up toward the liquid surface.

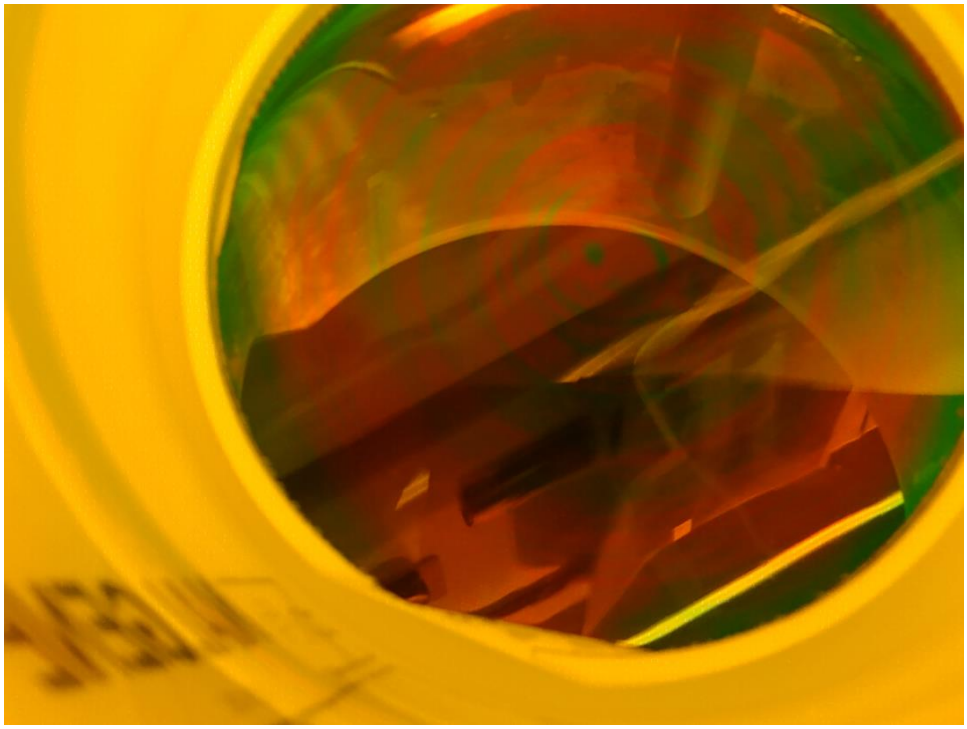

Figure 5.2.5. Wafer being etched in acetic acid modified recipe.

After the etching, rinsing, and drying of a wafer processed in the acetic modified recipe, a very uniform porous Si film has been obtained, as shown in Fig.5.2.6. Circles visible on the surface are due to non-uniformity of the wafer itself. The wafer is 100-mm size, so it was grown using the outdated version of the Czochralski process, without a magnetic field around the hot zone, and this results in fluctuations of crystallization rate, eventually visible as concentric circles on wafer surface.

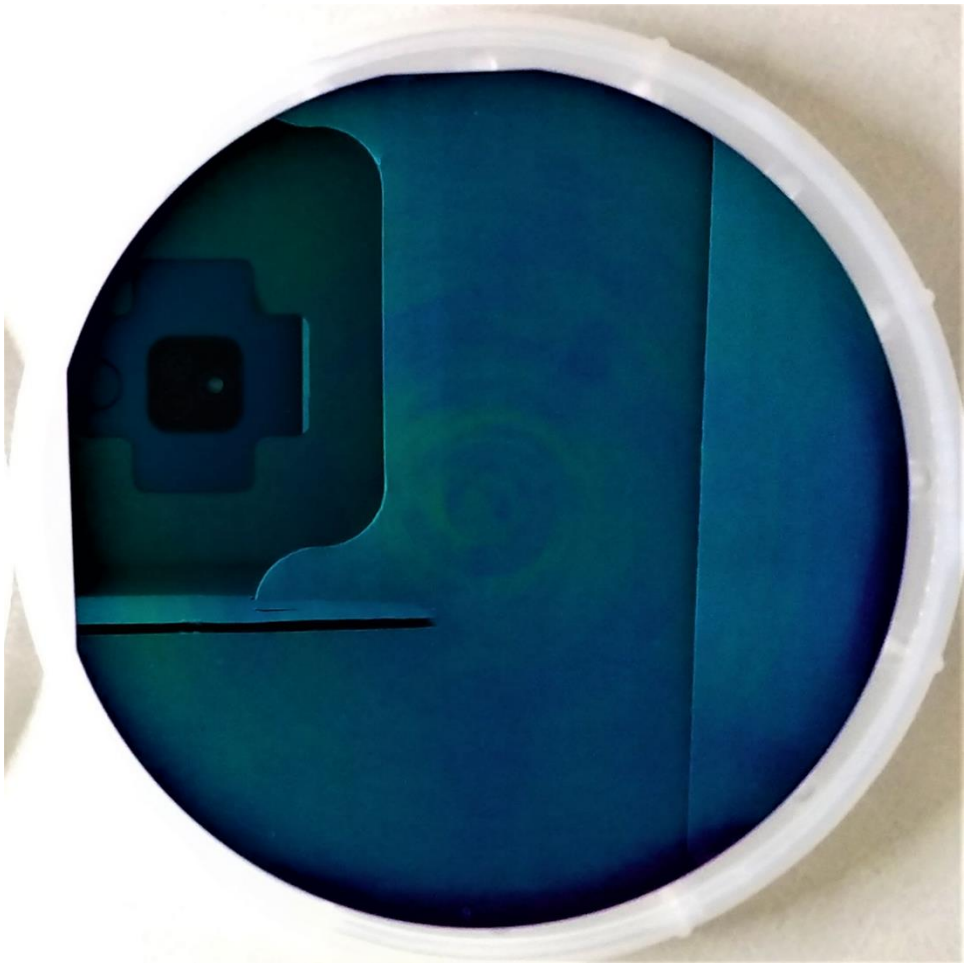

Figure 5.2.6. Typical appearance of stained Si after 1000:1:1000 HNA recipe.

Summarizing, we found a solution to create uniform thickness porous Si films. This method will be used in our DSRD manufacturing process to passivate side surfaces of diode dies. The process is performed at room temperature; therefore, it is easily integrable into the full diode process flow. The SEM image in Fig.5.2.7 confirms the uniform thickness of the stained (porous) Si layer through a cross sectional view, although the magnification is still not sufficient to see the porous layer morphology. This is one of next month's tasks: obtain a more detailed image of the Si porous structure obtained by etching in newly developed 1000:1:1000 HNA recipe. Notice that despite HNA (HF/nitric/acetic) being the most popular isotropic etch for silicon, using HNA for staining, i.e., in heavy oxidant-lean ratio, was described in the literature by only one research team in 2013 [4].

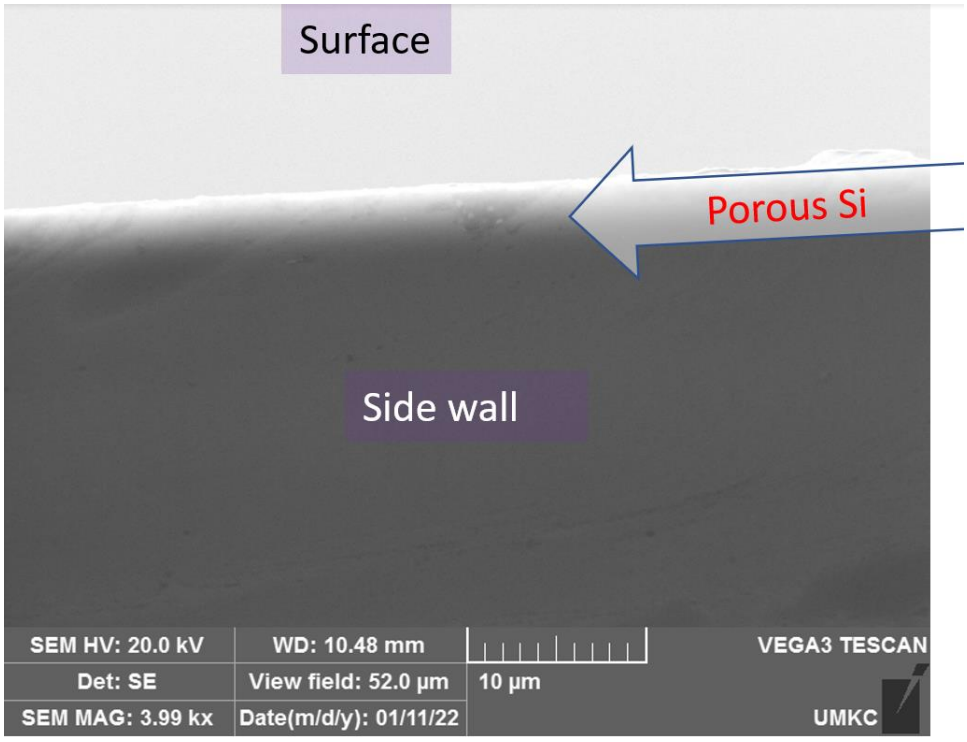

Figure 5.2.7. SEM image of heavily doped Si wafer after stain etch. 25 minutes in 1000:1:1000 HNA of <111> 720-880 Ohm-cm neutron transmutation doped n-type-phosphorus wafer. Courtesy S.Dhungana.

5.2.5 *Summary of Significant Findings and Mission Impact*

(A) Feedback from UMKC pulsed measurement team received - on Gen2 dies – see chapters 6.1 and 6.3 for details. The feedback has been thoroughly analyzed to improve the DSRD fabrication process. Several process adjustments have been implemented in processing of next Gen2 die lots. Die-to-die excessive variability is noticed. Process recipes and some equipment have been adjusted to achieve better uniformity and repeatability.

(B) Improving side termination of diodes. Upon analysis of etched v-grove shapes, decision made to purchase new labware including advanced wafer dippers. To prevent detrimental non-uniformity due to hydrogen bubbles sticking to wafer surface, several new process recipes have been developed. Next etch run will show whether sufficient uniformity achieved.

(C) Replacement of unreliable metal contact deposition technique (by electron beam sputtering in vacuum chamber). Technical feasibility run on direct electroless plating of the Palladium/Nickel stack was successful. Process recipe developed for next run, plate uniform stack of Pd/Ni/Cu/Sn.

The thickness and plating rate for the palladium and nickel in the electroless plating process have been determined from SEM cross section images of the samples.

(D) Diode side surface passivation by 2 new methods – stain etch, and SiOF deposition have been tried, and technical feasibility confirmed.

(F) A process recipe for side passivation of diodes using a stain etch has been developed. The thickness uniformity resulting from the stain etch technique has been drastically improved. Numerical recipes for the stain etch have been experimentally tested, and one recipe that totally suppresses hydrogen bubbles sticking to the Si surface was found. Using that recipe, very uniform thickness (porous Si) films were successfully grown on blanket silicon wafers with both low and high doping levels.

5.2.6 *References*

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5.3 Characterization of SOS Diode Performance through DOE Augmentation

(Megan Hyde)

5.3.1 *Problem Statement, Approach, and Context*

Primary Problem: Drift step recovery diodes (DSRDs) are planar diodes that are capable of nanosecond, high-frequency (10–10^3 kHz) pulses [1] with applications as opening switches in inductive energy storage (IES) pulse generation circuits. There is not a clear understanding of the effects DSRD parameters have on overall IES pulser performance. The purpose of this project is to tie the DSRD parameters to its tailored performance requirements.

Solution Space: Leveraging both design of experiment (DOE) and machine learning (ML) capabilities, we will develop a methodology of characterizing DSRDs in order to provide fabrication recommendations in the context of application targets.

***Sub-Problem 1*:** We do not yet understand how the diode parameters are tied to the diode performances.

Sub-Problem 2: There is no standardized method for correlating the diode key performance indicators (KPIs) to the IES pulser generator performance.

Sub-Problem 3: The number of possible inputs for the DOE is expected to be too large, so ML will need to be leveraged in order to guide decision-making processes.

State-of-the-Art (SOTA): Standard diode measurements include curve tracers for forward and reverse IV, impedance spectroscopy for forward and reverse CV, and

function generators or, for example, the Avtech pulser for reverse recovery with high voltage and/or high current when necessary. These measurements are used to generate commonly available datasheets for COTS diodes. These standard diode measurements can then be correlated to pulser performance using traditional data analytics.

Deficiency in the SOTA: The standard diode measurements and datasheets do not include pulser performance necessary to evaluate DSRDs. The datasets generated with doping profile assessment (for example spreading resistance profiling), standard diode measurements and pulser performance are too large and complex to leverage traditional data analytics and will benefit from machine learning techniques.

Solution Proposed: Develop a holistic evaluation network to characterize the KPIs of DSRDs. This network will include a DOE that will be a continuously evolving model as new KPIs are discovered between each of the stages within this section referred to as the "augmented DOE". Machine learning will be used as the primary decision-making tool for augmenting the DOE. Once the network is established, it will be used to outline the optimal parameters for stacks of DSRDs within an IES pulse generator.

Relevance to OSPRES Grant Objective: Bridging the gap between the theoretical and the physical performance of DSRDs enables closing the gap between a low fidelity TRL3 breadboard pulse generation system, and one which is at high fidelity TRL4 prototype level. At the TRL4 level, the DSRD-IES pulse generator system would be sufficient to replace the costly laser-based Si-PCSS HPM generator without compromise to scalability required to support the Naval afloat mission.

Risks, Payoffs, and Challenges:

Challenges: Traditional predictive analytics will be difficult to correlate with the augmented DOE due to the large volume of data. Machine learning is expected to assist with decision making processes for the DOE, but only if the proper KPIs have been established and good data has been used to train the machine learning model.

5.3.2 Tasks and Milestones / Timeline / Status

(A) Milestone – Establish preliminary DOE and standard operating procedure (SOP) for identifying KPIs of DSRDs [*estimated completion by DEC21*].

1. Task – Ascertain current KPIs used to optimize diodes simulated, manufactured, and utilized within the IES pulse generating circuit [completed AUG21];
2. Task – Construct preliminary DOE to acquire data on all KPIs based on Task 1 to produce an optimal output for the IES pulse generating circuit [AUG21–MAR22];
3. Task – Leverage existing Python scripts to process legacy DSRD KPI data [*completed SEP21*];
4. Task – Develop new and review existing SOPs for experimental testing apparatuses used to evaluate individual KPIs and measure their performance [*completed OCT21*];
5. Task – Identify gaps/deficiencies in legacy KPI data, evaluate existing theoretical relationships to bridge gap and minimize DOE if possible [*SEP–OCT21*];

6. Task – Using SOPs developed in Task 4, acquire experimental data from legacy DSRDs, refine SOP(s), and assess repeatability and reproducibility [*SEP21–FEB22*];
7. Task – Begin training machine learning model with legacy data to determine statistical correlations and significance of KPIs, and their interdependent relationships [*OCT21–MAR22*];

(B) Milestone – Evaluate DSRD performance by the developed SOPs and facilitated by the preliminary DOE [*on hold until Milestone A is completed*].

1. Task – Augment DOE to include previously unidentified yet relevant KPIs based on new findings [*Est. Spring22*];
2. Task – Acquire data on newly manufactured epitaxial DSRDs from Section 5.2 using refined SOPs from Milestone A [*Est. Spring22*];
3. Task – Correlate KPIs to TCAD simulation model, manufactured diode characteristics, and 'M×N' IES pulser's performance to aid in simulation model development, fabrication procedures, and circuit topology development [*Est. Spring22*];

(C) Milestone – SOS diode network evaluation [*on hold until Milestone B is completed*].

1. Task – Refine Python script to incorporate new correlations based on findings from Milestones A&B [*Est. Fall22*];
2. Task – Amend ML training model with data acquired on new DSRDs (as characterized by Sections 5.1–5.2) to investigate statistical correlation of diode performance [*Est. Summer22*];
3. Task – Work with TCAD simulation team to address discrepancies between the DSRD's performance obtained experimentally, and that achieved within simulations [*Est. Summer22*];
4. Task – Collaborate with DSRD manufacturing team to address discrepancies between the DSRD's characteristics evaluated experimentally, and that desired by manufacturing process [*Est. Summer22*];
5. Task – Investigate relationships between statistical significance of individual diode KPIs to the peak performance of the IES pulser with the pulse generator team. [*Est. Summer22*];
6. Task – Incorporate findings from Tasks 1–5 into ML model, pinpoint KPI correlations of interest, and provide recommendations to IES sub-teams accordingly [*Est. Summer22*];

(D) Milestone – SOS diode network evaluation [*on hold until Milestone C is completed*].

1. Task – Augment DOE network to streamline diode evaluation and identify checkpoints/gaps within simulation, manufacturing, and circuit development process to ensure optimal diodes are selected and utilized to produced robust high-fidelity IES pulse generator prototypes [*Est. Fall22*];

5.3.3 *Progress Made Since Last Report*

(A.2) A preliminary experimental design was constructed to include the following KPIs: zero junction bias capacitance, maximum forward voltage at 10 mA, and current at reverse 200 V. To begin, the current–voltage measurements are scheduled to be taken on a picoammeter, but progress is being made to provide comparison measurements on a Tektronix 371A Curve Tracer.

(A.6) Experimental data was acquired on all tests for all diodes except for the deep diffusion (DD7) 7 stack diodes that are awaiting reverse recovery testing (RRT). A completely randomized block design (CRBD) was developed, a testing schedule, and a complete list of diodes that have been compartmentalized into separate testing groups.

5.3.4 *Technical Results*

(A.2) The repeatability study performed on the Gen 2 diodes (Figure 5.3.1) provided some question with validating the results of each measurement (i.e., is the variability due to a damaged diode, inconsistent testing conditions). The main goal of this project is to determine a selection process for DSRD diodes that will produce the optimal pulser performance. Most of the circuit designs will involve pairs of diodes, so the variation in testing performance can hinder the diode selection process. The proposed solution is to determine the source of variability by using a completely randomized block design (CRBD) experiment.

A CRBD experiment was developed as a guide for selecting the best "type" of diode available for testing as well as the ideal selection of diodes for the IES pulse-generating circuits. Table 5.3.1 contains 6 types of DSRDs that have been selected for each of the 6 rounds of testing for the CRBD. For the experiment, one of each type of diode was selected for each "Round" or group to be tested. This maintains the "randomization" of the testing to protect against any unknown factors that will introduce variations in the test results [3]. As proof of concept, the Rounds 1 through 6 (out of a total of 16 Rounds) are currently being tested per the CRBD.

	Round 1	Round 2	Round 3
Deep Diffusion 7 Stack	D1	D319	D333
Deep Diffusion Untested	D630	D657	D801
Epitaxially Grown 1500	EG1562	EG1563	EG1564
Epitaxially Grown 1600	EG1601	EG1602	EG1603
Gen 2	1-1	1-2	1-3
Gen 2.2	1	2	3

	Round 4	Round 5	Round 6
Deep Diffusion 7 Stack	D366	D367	D380
Deep Diffusion Untested	D802	D803	D804
Epitaxially Grown 1500	EG1565	EG1566	EG1567
Epitaxially Grown 1600	EG1604	EG1605	EG1606
Gen 2	1-4	2-1	2-2
Gen 2.2	4	5	6

Table 5.3.1. This table is representative of 16 total rounds for the experimental design testing. Each round contains one of each type of diode (i.e., deep diffusion 7 stack, epitaxially grown diodes, gen 2 diodes).

The CRBD is different from the completely randomized design (CRD) in that it incorporates samples with different processing histories by "blocking" identified factors that are suspected in having an influence on the overall measurement. The effect's measurement is evaluated by the following model:

$$\underset{\text{Block 1}}{\begin{pmatrix} y_{11} \\ y_{21} \\ y_{31} \\ \vdots \\ y_{a1} \end{pmatrix}} \quad \underset{\text{Block 2}}{\begin{pmatrix} y_{12} \\ y_{22} \\ y_{32} \\ \vdots \\ y_{a2} \end{pmatrix}} \quad \underset{\text{Block b}}{\begin{pmatrix} y_{1b} \\ y_{2b} \\ y_{3b} \\ \vdots \\ y_{ab} \end{pmatrix}}$$

$$y_{ij} = \mu + \tau_i + \beta_j + \epsilon_{ij} \begin{cases} i = 1, 2, 3, \dots, a \\ j = 1, 2, 3, \dots, b \end{cases}$$

Where μ is the overall mean, τ_i is the effects of the ith treatment, β_j is the effects of the jth treatment, and ϵ_{ij} is a random error term [3]. Each "block" introduced in this experiment isolates the known influencing factors that we want to isolate from the result of each "a" diode per "b" unwanted influence.

For example, the "blocks", as introduced briefly in Figure 5.3.2, will be the Operator, Technique (forward IV, reverse IV, and CV), and Time in between measurements. Each operator will test a round of diodes (refer to Table 5.3.1) that will contain one of each diode type (each diode type is an "a" treatment from the above model) using each technique with a minimum of a 12-hour time period in between tests. The influencing factors such as the Operator, Technique, and Time ("b" treatments from the above model) will reflect the greatest influence on overall testing results.

(A.6) Preliminary results from the experimental data collected thus far showed inconsistencies in the results. These inconsistencies manifested themselves in the repeatability study performed on the Gen 2 diodes. These diodes underwent forward and reverse current–voltage and capacitance–voltage measurements a total of three times. The results of this repeatability study are shown in Figure 5.3.1. This study highlighted the need to identify and reduce the influence of "nuisance factors" that are probably affecting the experimental results.

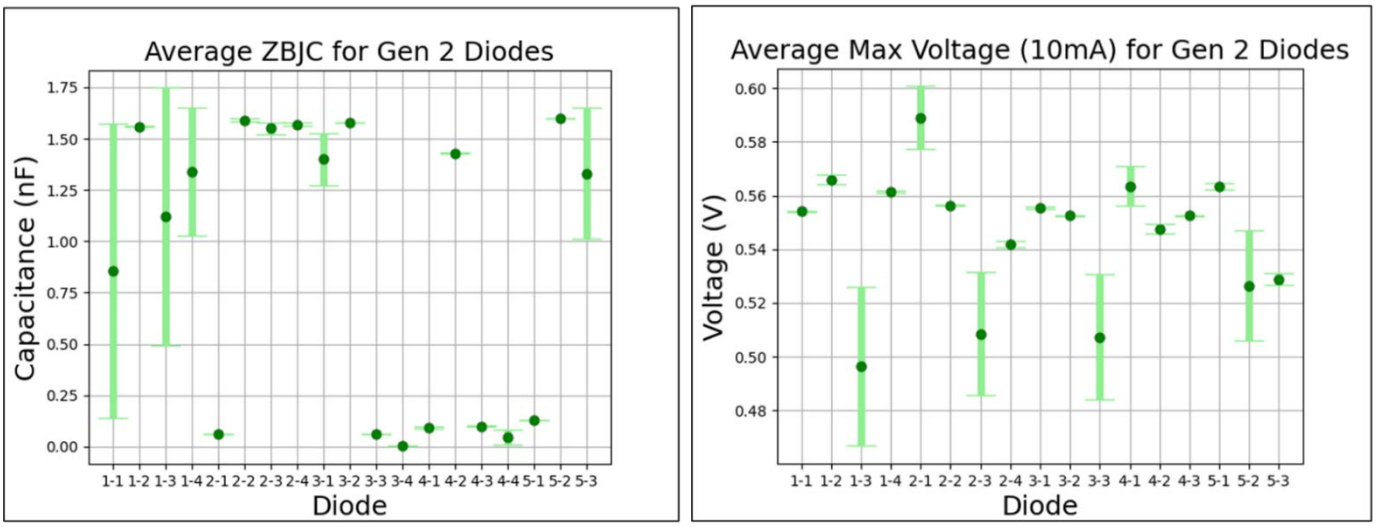

Figure 5.3.1. Results of the zero-junction bias capacitance and the maximum forward voltage at 10 mA for the repeatability study of the Gen 2 diodes. A Levene's Variability test was performed on the results for both tests, where the p-value validates the consistency of the testing performed (p = 0.8548 for the zero-junction bias capacitance and p = 0.8416 for maximum voltage measurements). Diodes 3-4 and 4-4 were not included in the maximum voltage graph because the devices failed to reach 10 mA.

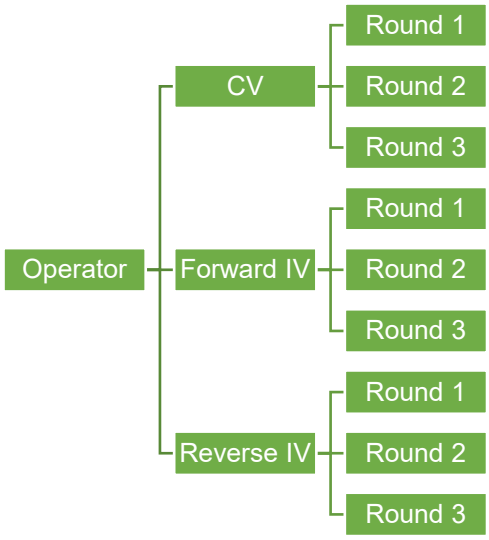

Figure 5.3.2. A simplified flow chart on how the diodes from Table 5.3.1 will be tested. Each round will be tested by 3 different operators using 3 different techniques (forward IV, reverse IV, and CV) with a minimum of 12-hour break in between each test. Note: only Rounds 1 through 3 were included in this chart for simplicity.

Possible nuisance factors that have been identified are operator, equipment/sample holders, and time in between data collection. These factors were used to outline a testing plan to mitigate future influence on measurement

results by “blocking” each factor. Figure 5.3.2 provides a basic outline of the testing expectation of each round of diode.

Development of a standardized procedure for reverse recovery testing (RRT) measurements for calculating minority carrier lifetimes are under investigation. Presently, the test is on hold due to limitations in pulse trigger lengths.. Due to this limitation, RRT measurements are currently not a part of the CRBD experiment. However, they have shown greater consistency in testing results than the DC measurements (refer to Figure 5.3.4) over a range of applied voltage parameters (Figure 5.3.3).

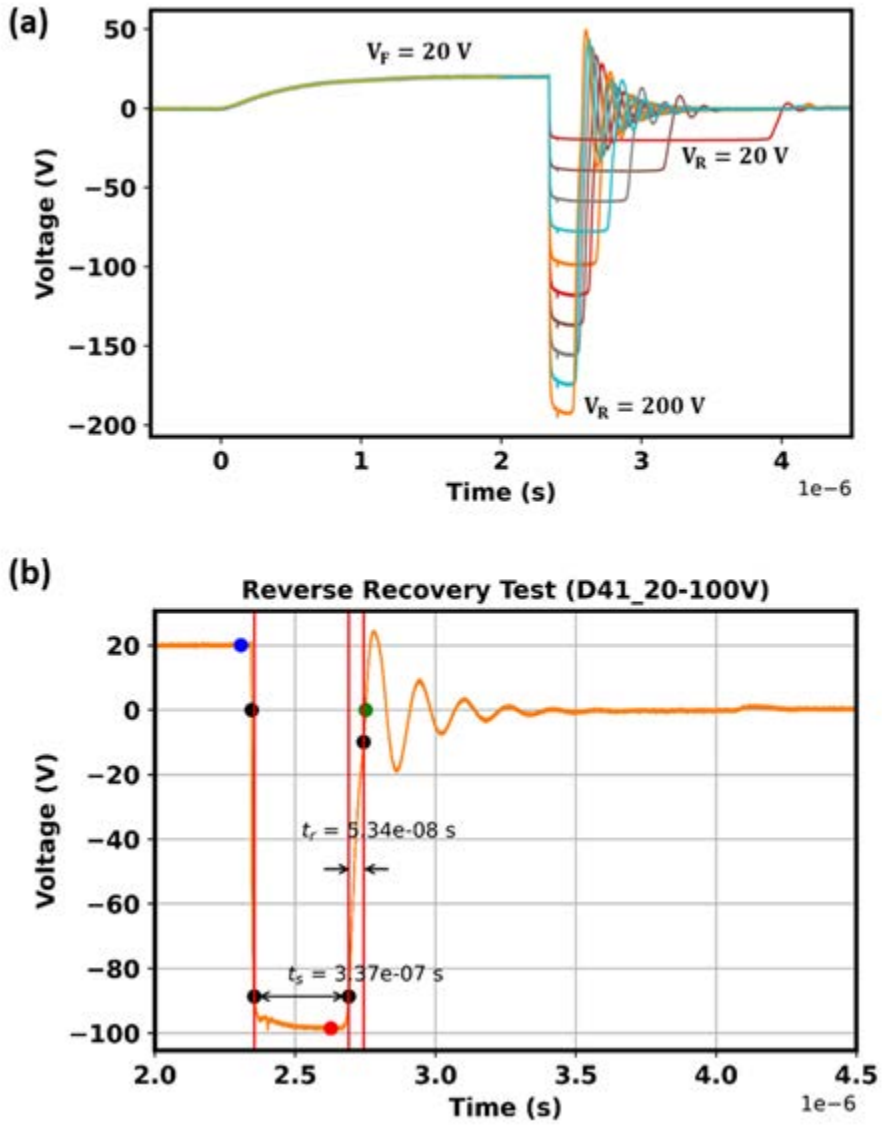

Figure 5.3.3 (a) A typical reverse recovery test data of a single-stack Gen 2 DSRD with forward voltage of 20 V and reverse voltage from 20 V to 200 V. Both forward and reverse voltage pulses were applied for 2 μs. (b) Reverse recovery test of Gen 2 diode 4-1 showing the charge storage time t_s and transition time t_r.

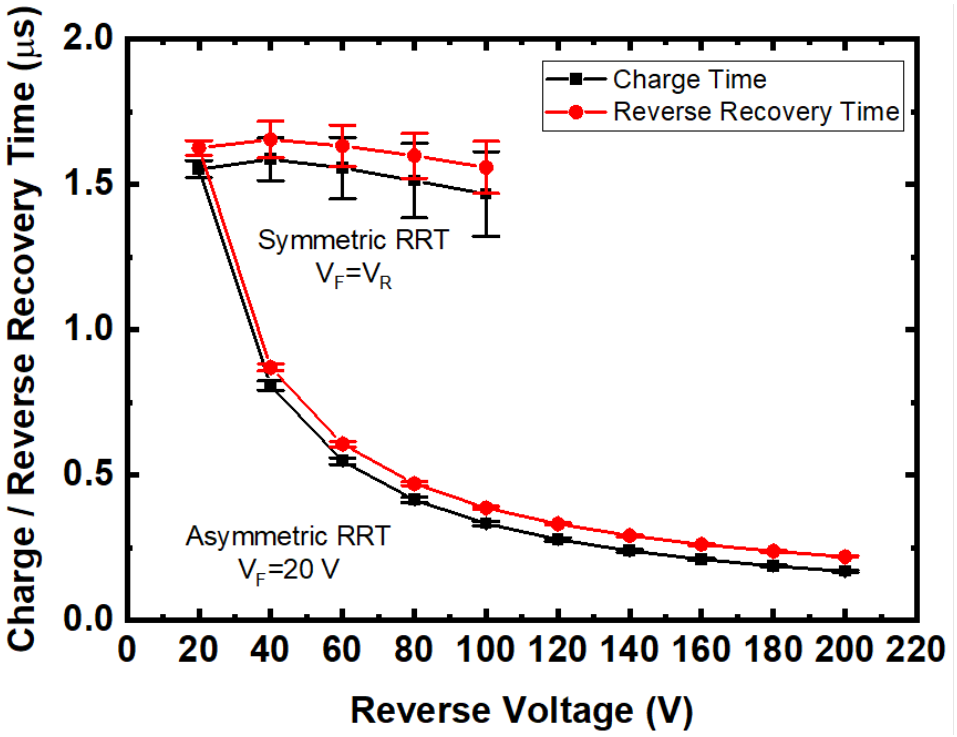

Figure 5.3.4. Charge storage and Reverse recovery time of single stack Gen-2 DSRD diodes as a function of reverse pulse voltage. The symmetric RRT is for test conditions where forward and reverse pulses were of equal amplitude, while asymmetric RRT is for increasing reverse voltage for 20 V forward pulse amplitude. Reverse recovery time is the sum of the charge storage time and the transition time (see Figure 5.3.3 (b)).

The minority carrier lifetime in the DSRDs were calculated using the Kingstone [5] equation given by:

$$\frac{1}{1 + I_R/I_F} = erf\left(\frac{t_s}{\tau_{eff}}\right)^{1/2}$$

where I_R, I_F, and τ_{eff} represent the reverse current, forward current, and the minority carrier lifetime, respectively. Since the carrier lifetime is expected to be independent of the reverse voltage applied, the observed linear relationship between them (refer to Figure 5.3.5) may indicate that the calculated parameter is not actually the carrier lifetime (a measurement depending on the diode thickness), but may instead represent the carrier transit time [5].

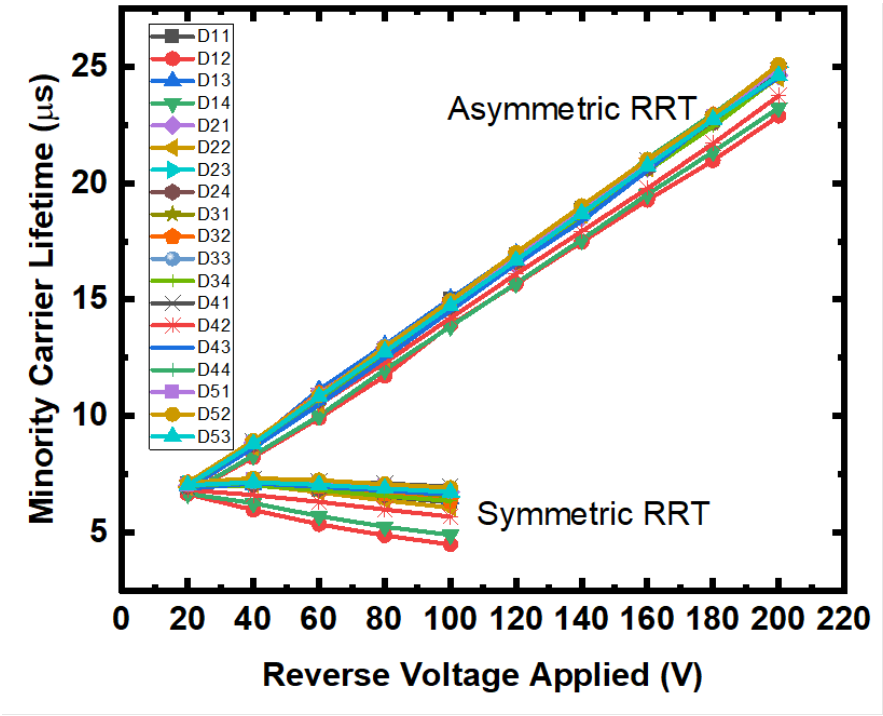

Figure 5.3.5. Minority carrier lifetime obtained for single-stack Gen 2 diodes as a function of applied reverse voltage.

5.3.5 *Summary of Significant Findings and Mission Impact*

(A.1) The KPIs established thus far are: current at -200 V, voltage at 10 mA (forward bias), zero junction bias capacitance, minority carrier lifetimes, and series resistance. Additional KPIs are expected for IES pulser circuits.

(A.2) A preliminary DOE is in process. Currently, 6 out of a total of 16 rounds of DSRD diodes are undergoing DC testing for characterization purposes. Once the 6 rounds have completed testing, statistical analysis will determine if the experimental design requires modification.

(A.3) Python scripts have been modified for calculating and exporting measurement results and plots into Excel file.

(A.4) SOPs for forward and reverse IV and CV have all been updated with a page for tracking changes made to the procedures.

A standardized testing procedure for RRT measurements is still in progress. Development of this test will lead to an increased understanding in minority carrier lifetime measurements and how they relate to the forward pumping time for pulsing.

(A.5) The IV measurements are performed by a picoammeter, which restricts the range of current that can be applied to each diode. A Tektronix curve tracer is under

investigation for data collection to provide test results for larger currents and voltages.

(A.6) Inconsistencies in the experimental results require a root cause analysis. A preliminary repeatability and reproducibility test was performed on all Gen 2 diodes. Each diode was tested three times on each test, but the results revealed large variations. A CRBD experiment will aid in eliminating some of the possible sources of variation.

5.3.6 *References*

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5.4 DSRD-Based Pulsed Power Source Systematic Topological Optimization

(Gyanendra Bhattarai & Roy Allen)

5.4.1 *Problem Statement, Approach, and Context*

Primary Problem: Inductive energy storage (IES) and release pulse generators that use drift-step recovery diodes (DSRDs), when able to achieve ones of gigawatts in ones of nanoseconds, are large, heavy, and require liquid-based cooling systems to dissipate the excess heat they generate during operation; therefore, rendering them impractical for Navy afloat missions.

Solution Space: Systematically develop a modular architecture of a pulser circuit using DSRDs by determining the optimal permutation of series and parallel combinations of the base pulser unit, and its component parameters, in order to maximize the peak voltage, peak power, and volumetric power density without sacrificing the desired nanosecond risetime of the pulses generated or requiring liquid-based cooling.

***Sub-Problem*:** DSRDs are not domestically available COTs components. The small-batch quantities that are manufactured have statistically significant variations in their performance parameters. In addition, SPICE models of these diodes are not accurate and do not account for their sample-to-sample parameter variability. The above-mentioned reasons may lead to an inaccurate simulation model of the pulser that may result in a difference between the simulation and experimental results.

State-of-the-Art (SOTA): DSRD-based pulsers (equivalent in size to the pulse generators developed for this effort, i.e., ~0.01-m^3, ~2-kg) can achieve 6-kV, 200-ps risetime, and <500 ps FWHM across a 50 Ω load.

Deficiency in the SOTA: DSRD-based air-cooled versions are limited to PRFs of < 15 kHz. Additionally, current studies on SOS-IES pulse generators attempt to present only the best-case circuit configurations, meaning a comprehensive study on optimizing the number and ratio of parallel branches and series-connected stages aiming to achieve maximum gain and efficiency (reducing thermal load) is missing in the SOTA.

Solution Proposed: Systematically determine topological SOS-IES circuit configurations and the necessary components therein that maximize voltage gain and efficiency and minimize the rise-time achieved by the pulser.

Relevance to OSPRES Grant Objective: IES pulse generators using DSRDs can remove the need for photo-triggered switches and their laser sub-systems. They are ideal for triggering sub-nanosecond rise-time sharpeners (SAS, D-NLTL, etc.), reducing overall cost, volume, and weight.

Risks, Payoffs, and Challenges:

Risks: Domestically manufactured (U.S.-based) DSRDs, which possess sub-optimal doping profiles, may lead to sub-optimal pulse generators with sub-optimal performance. The data gathered from these sub-optimal circuits would then be used to train the genetic/machine learning algorithms developed and the redesign of future topologies constructed; ultimately leading to spurious conclusions regarding ideal topological circuit

configurations with ‘N’ number of series-connected stages, each containing ‘M’ parallel branches.

Payoffs: Leveraging collaborative partnerships with U.S.-based manufacturers of DSRDs, the ability to refine and control the performance characteristics of the diodes themselves, along with the ability to simulate and manufacture the DSRD pulsers in-house, enables a holistic soup-to-nuts capability to optimize, produce, and evaluate these nanosecond pulse generators.

Challenges: Determining the superlative ratio of design/development (through numerical analysis) to the effort put towards experimental testing/evaluation of the DSRD pulser is challenging due to the novelty of the approach. The complexity of the theoretical model is extreme given the M×N number of DSRD base unit stages within the pulse forming network along with inaccurate DSRD spice model and large sample-to-sample variability.

5.4.2 Tasks and Milestones / Timeline / Status

(A) Milestone – Develop theory of DSRD pulse generator to facilitate optimization of 1×1 and M×N pulse generator [***Ongoing***].

(B) Milestone – Construct/demonstrate a DSRD-based 2×2 IES pulse generator prototype capable of producing $\geq$4 kV peak voltage, $\leq$1 ns risetime, $\leq$5 ns FWHM, $\geq$320 kW peak-power, $\geq$1 kHz PRF, $\geq$100 shots-per-burst, $\geq$5 number of bursts [***Completed JUL21***].

(C) Milestone – Construct/demonstrate a DSRD-based 1×1 IES pulse generator prototype capable of testing individual and combinations of diode stacks to acquire performance data [***Completed AUG21***].

(D) Milestone – Construct/demonstrate a DSRD-based 4×2 IES pulse generator prototype capable of producing $\geq$12 kV peak voltage, $\leq$1 ns risetime, $\leq$5 ns FWHM, $\geq$3 MW peak-power, $\geq$100 kHz PRF, $\geq$1,000 shots-per-burst, $\geq$500 number of bursts [*Ongoing, estimated completion by OCT21*].

1. Task – Develop revised layout in Altium and order PCB and components. [***Completed – SEP21***];
2. Task – Populate pulse generator and begin testing & evaluation phase [***Completed – NOV21***];

(E) Milestone – Develop waveform inverter which, when combined with the pulser from Milestone C, enables a balanced differential waveform output with >90% inverted signal fidelity. [***Completed – DEC21***].

(F) Milestone – Construct/demonstrate a M×N pulse generator prototype capable of producing $\geq$20 kV peak voltage, $\leq$1 ns risetime, $\leq$2 ns FWHM, $\geq$8 MW peak-power, $\geq$100 kHz PRF, and $\geq 2\sigma_{Vpeak}$, which operates in continuous-burst mode as a viable candidate for OSPRES Contract source alternative [*on hold until Milestones C & D are completed*].

5.4.3 *Progress Made Since Last Report*

(A) A circuit analysis for a single-bar (1×1) DSRD pulser was presented in the last reporting period. Based on the working theory, we have presented the optimization of a (1×1) DSRD pulser containing one 7-stack diode and four 7-stack diodes from LLNL.

(C) A new 1×1 DSRD-based pulse generator has been populated and is currently being tested and evaluated according to the theory presented in the previous reporting period.

5.4.4 *Technical Results*

5.4.4.1 Optimization of a Single-Bar 1×1 DSRD Pulser

With the DSRD pulser theory presented in the previous report, we have minimized the parameter space for the initial optimization of the DSRD pulser circuit shown in Figure 5.4.1. Specifically, we have the following independent parameters which can be optimized initially.

- Pumping time (t_{pump})
- Trigger length (T_{ON})
- Capacitance (C_1)
- Capacitance (C_s)

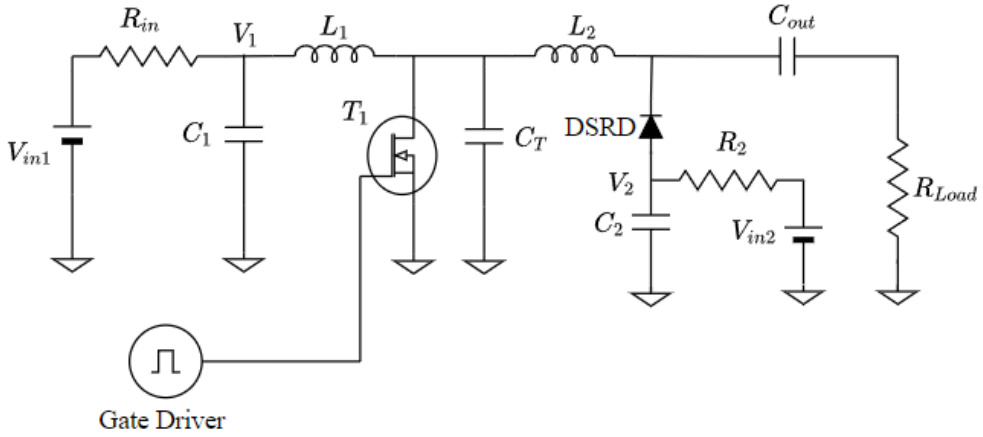


Figure 5.4.1. A schematic of a MOSFET-driven single-bar DSRD pulser circuit currently being used for study.

Now, with some circuit parameters set to previously optimized values, we present an optimization sequence for a 1x1 DSRD pulser using an updated spice diode model for a LLNL 7-stack diode. In this simulation and optimization process, an ON-Semi MOSFET NVH4L020N120SC1_4P has been used, which has a single 400 A pulse rating. Thus, the simulation circuit is limited to a total MOSFET current <400 A. Further, the maximum diode forward current is limited to 150 A for a pumping time less than 2 μs and the diode reverse breakdown voltage is set to infinite so that we find the most capable conditions which can drive multiple stacks of diodes with minimal adjustments.

(i) Optimization of pumping time (t_{pump})

For this optimization, we have used the following conditions. All remaining circuit parameters are chosen according to the theory presented.

- $V_{in1} = V_{in2} = 50$ V,
- $L_1 = L_2$
- $C_s = 15$ nF.
- Forward pumping time (t_{pump}) is varied between 100 ns to 1.5 μs in an interval of 100 ns
- MOSFET trigger length (T_{ON}) $= k \times t_{\mathrm{pump}}$; $k = 0.9$ to 1.6 in an interval of 0.1.

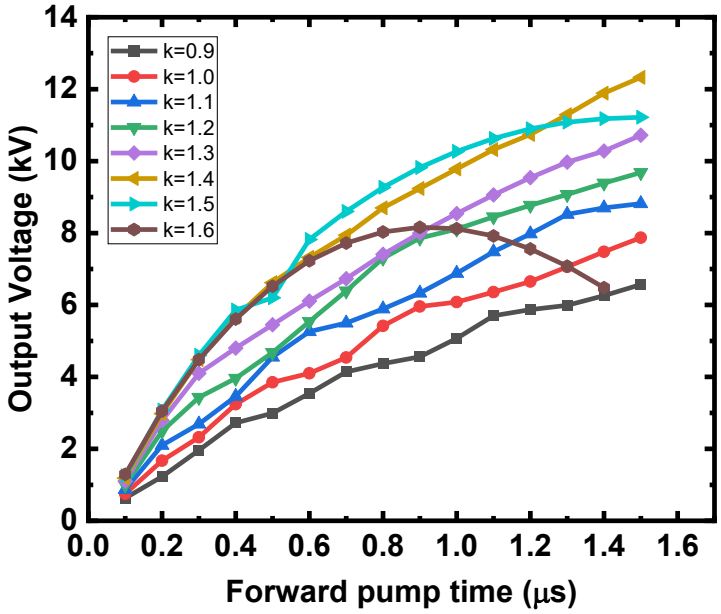


Figure 5.4.2. Variation of output voltage with changing forward pumping time.

Figure 5.4.2 shows the variation of the output pulse voltage as a function of forward pumping time for different trigger length. As expected, in the range of $t_{\mathrm{pump}} \leq T_{\mathrm{ON}} \leq 1.5\, t_{\mathrm{pump}}$, the output voltage increases with the pumping time. However, as the pumping time becomes much longer, the stored injected charge in the diode saturates due to continuous recombination which results in the saturation of the output voltage. Although we did not achieve a global maximum of the output voltage, it is not always possible to increase the pumping time indefinitely due to MOSFET current rating and limitation in PRF. Thus, here we use 1500 ns as an optimum pumping time. However, the pumping time can be significantly decreased for higher values of the prime voltages V_{in1} and V_{in2}. The result further verifies that the output voltage decreases when the trigger length becomes longer than 1.5 times the forward pumping time.

(ii) Optimization of C_{s}

For this optimization, all other circuit parameters are set at the optimized values of the optimization (i) and the capacitor C_s is varied between 5 nF and 40 nF in an interval of 5 nF.

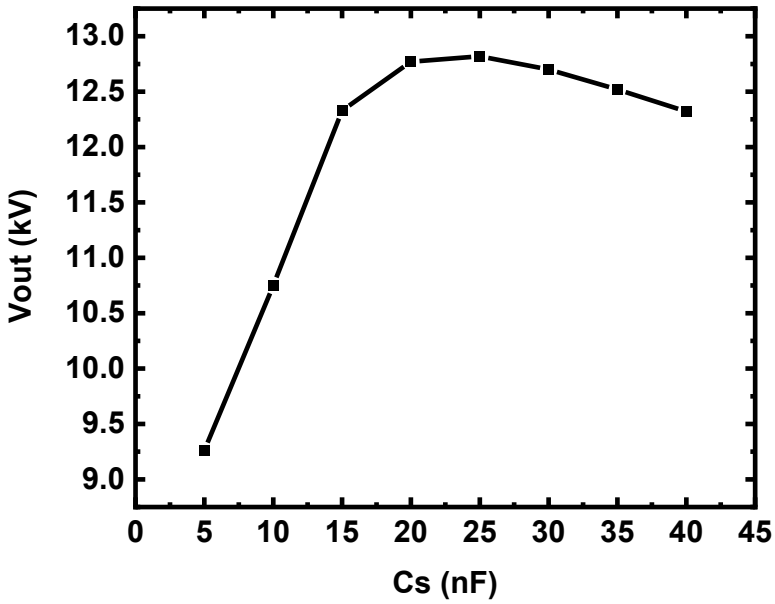


Figure 5.4.3. Variation of output voltage with varying value of C_s.

Figure 5.4.3 shows the variation of the output voltage as a function of C_s. Although the presented theory does not tell the effect of the shunt capacitance C_s due to mathematical complexity, we obtained that the output changes with its variation. For the circuit presented, we obtained maximum output for $C_s = 25$ nF.

(iii) Optimization of L_1

The initial choice of L_1 is made such that the current through it does not exceed the MOSFET current rating. Assuming equal initial rate of increase of currents I_1 and I_2, $L_1 = L_2$ gives $I_1 = \pi I_2$ at $t = t_{\text{pump}}$ (for a large capacitance C_1), at which the MOSFET can be turned off to induce a high reverse biasing voltage across the diode. The current through L_1 and MOSFET current as a function of time for $L_1 = L_2$ is shown in Figure 5.4.4.

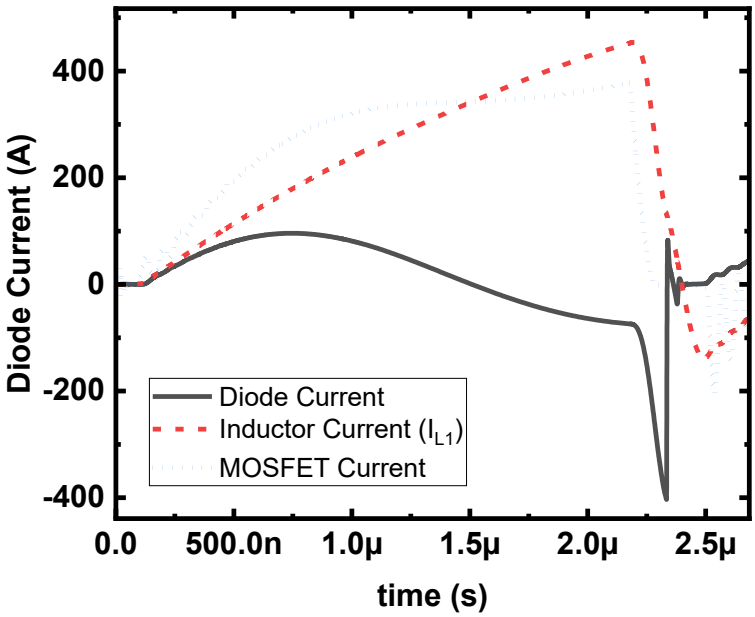


Figure 5.4.4. Circuit currents for $L_1 = L_2$. Other circuit parameters are set from the previous optimization.

We can see from the figure that the inductor current $I(L_1)$ exceeds the MOSFET rating (400 A). However, due to the reverse current through the diode after pumping time, the total MOSFET current remains below the rating.

Now for the optimization of L_1 we set $L_1 = m \times L_2$ with $m = 0.6$ to 2.0 in an interval of 0.2.

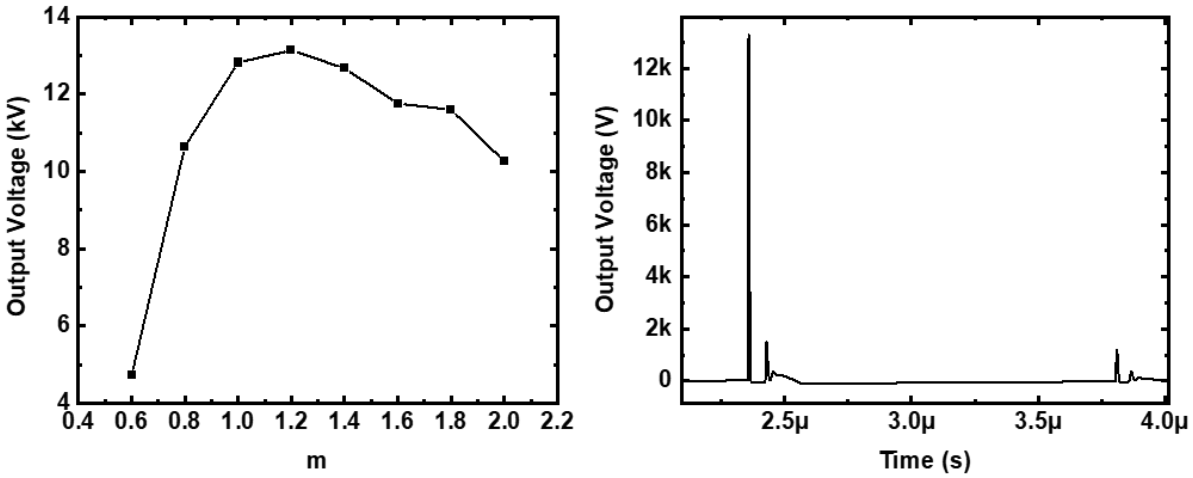


Figure 5.4.5. Variation of output voltage as a function of Inductance $L_1 = \mathrm{m}L_2$ and the output pulse for the optimized circuit parameters. The maximum output voltage is obtained for $L_1 = 1.2L_2$

Figure 5.4.5 shows the variation of output voltage with the variation of the inductance L_1 and the output voltage obtained for the optimized circuit. Although we obtained an output of ~13 kV with the optimized circuit with prime voltage of 50 V, the pumping time of 1500 ns is not practical due to MOSFET rating. Although the circuit parameters

are set to achieve the amplitude of forward pumping current to be 150A, the simulated current is lower than expected due to the non-negligible voltage drop across the MOSFET. This limitation on diode current can have an indirect effect on the optimum pumping time. Further, even with $V_{in1} = V_{in2} = 50$ V, we achieved ~13 kV of output voltage which can drive four 7-stack diodes with each diode having a reverse breakdown voltage of 500 V.

As we increase the number of diodes, the prime voltage sources V_{in1} and V_{in2} should be increased to provide necessary pumping current. Following the optimization procedure explained above, we obtained the following circuit parameters for a 1×1 DSRD pulser circuit (circuit as shown in Figure 5.4.1). The simulated output of the optimized circuit is shown in Figure 5.4.6.

$$V_{in1} = V_{in2} = 120 \text{ V}$$
$$R_{in} = 100 \text{ Ω}$$
$$L_1 = 265 \text{ nH}$$
$$C_1 = 45 \text{ μF}$$
$$L_2 = 330 \text{ nH}$$
$$C_2 = 250 \text{ nF}$$
$$C_s = 15 \text{ nF}$$
$$C_{\text{out}} = 15 \text{ nF}$$
$$R_2 = 1.2 \text{ kΩ}$$
$$T_{\text{ON}} = 1.1 \text{ μs}$$

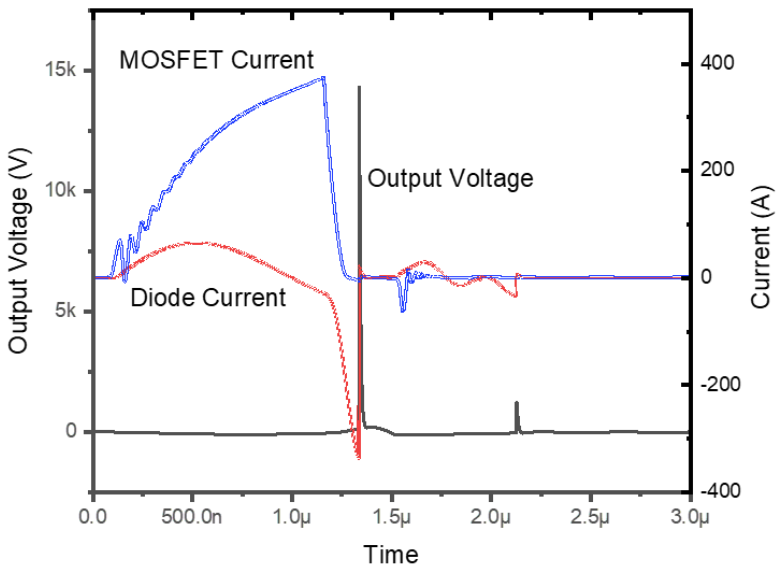


Figure 5.4.6. Simulated diode current, MOSFET current and output voltage of a 1×1 DSRD pulser containing four 7-stack diodes.

Figure 5.4.6 shows the simulated output voltage from an optimized 1×1 DSRD circuit using four 7-stack diodes. Although the circuit parameters could still be optimized for higher output voltage, a total of 28 diodes each with a breakdown voltage of 500 V will undergo device breakdown at higher voltages. So, the circuit parameters are optimized for an output voltage of 14kV. The figure further shows that the MOSFET current does not exceed the 400 A rating given by the manufacturer.

Although we have identified the optimized circuit parameters for a 1×1 DSRD pulser using LT-Spice simulation, it is important to remember that there are limitations in the DSRD modeling, which actually represents the true DSRD action. For example, LT-Spice diode models we have developed do not have the capability to model the carrier recombination within the diode which results into lower charge extraction for longer pumping time. Also, the diode models we are using are not capable to address the distribution of the charge carriers within the device during the current pumping time and the variation in the DSRD snap-off feature as a function of increasing pumping current. There could be issues with the true distribution of the charge carriers within the device The optimized parameters identified here are based on long carrier recombination lifetime so that the injected charge carriers remain free to be extracted for the entire trigger length and the device performance does not change as a function of pumping current. To address these complex issues, we will be implementing TCAD simulation tool in the future so as to obtain optimized circuit parameters based on the physics of DSRD.

5.4.5 *Summary of Significant Findings and Mission Impact*

(A) A systematic optimization of a 1×1 pulse generator based on the theory presented in the previous reporting period is presented. Based on the simulation, we optimized the circuit for a maximum output voltage of 14 kV using four 7-stack diodes.

(B) Successful construction and operation of a 2×2 DSRD-based IES pulse generator prototype has been completed, which meets or exceeds the required key performance metrics. Shown in Table 5.4.1 are the previous and current pulse generator performance specifications in comparison to a similar 2×2 pulser developed by Kesar et al. [1] using DSRDs, and to that of a commercial off-the-shelf (COTS) DSRD pulser of similar space and weight developed by Megaimpulse (i.e., PPM-0731), which also uses DSRDs with silicon avalanche shapers (SAS) [2]. Although the Megaimpulse pulser utilizes a SAS with a <500 ps risetime (a threshold we do not intend to go below due to Commerce Controlled List limitations), it is interesting to compare the results of linear voltage gain and peak power of this system, to that of one that utilizes a SAS. The current permutation of the 2×2 DSRD-IES pulser developed by MIDE under the ONR OSPRES Grant is able to achieve a higher peak voltage and shorter risetime than DSRD-based pulsers reported in the literature of comparable space and weight as well as those commercially available. The ability to generate a linear voltage gain of 40.8 to produce over a Megawatt of peak power into a 50 Ω load while achieving a peak voltage output standard deviation of 2σ when operating at a PRF of at least 100 kHz, brings this technology to the forefront of viable options to potentially support the Naval afloat mission.

Table 5.4.1. Comparison of DSRD-based IES Pulse Generator Performance.

KPM	Units	MIDE - V1 Previous	MIDE - V2 Current	Kesar *et al.* SOTA	MI-PPM0731 COTS
V_{supply}	V	225	180	300	160
T_{ON}	ns	100	340	?	200
V_{peak}	kV	5.59	**7.35**	5	6.3
Gain	V/V	24.8	**40.8**	16.7	39.4
$\tau_{rise,20\text{-}90\%}$	ns	1.2	1.142	1.96	0.12
dV/dτ	kV/ns	4.66	6.44	2.55	**52.50**
FWHM	ns	2	5.48	2.27	0.35
PW	ns	5	7	3.5	2.5
Z_{LOAD}	Ω	50	50	50	50
P_{peak}	MW	0.625	**1.080**	0.500	0.794
E_{pp}	mJ	0.125	0.154	0.143	0.318
PRF_{max}	kHz	100	100	100	15
Burst	shots	100	100	*N/A*	100
	%	100	100	*N/A*	100
SD_{Vpeak}	σ	> 2	**> 2**	*N/A*	*N/A*
	%	96.5	**97.8**	*N/A*	*N/A*

(C) Discrepancies exist in the obtained data for different series combinations and different samples of 7-stack DSRDs, which may be attributed to the inconsistencies in their manufacturing process. Future work in the coming months include carrying out further testing on the 1×1 DSRD-based pulse generator (base-unit) circuit using more combinations of series-connected as well as parallel-connected DSRD stacks.

5.4.6 *References*

[1] https://www.onsemi.com/pdf/datasheet/nvh4l020n120sc1-d.pdf

[2] https://cms.wolfspeed.com/app/uploads/2020/12/C2M0045170P.pdf

5.5 All-Solid-State Sub-ns MW Pulse Generators with Semiconductor Sharpeners

(Gyanendra Bhattarai)

5.5.1 *Problem Statement, Approach, and Context*

***Primary Problem*:** Broadband high-power microwave (HPM) systems need sub-nanosecond tens-of-MW pulses. Hydrogen spark gaps (HSG), traditionally used for such purposes, are severely limited by their low pulse repetition frequency (PRF ~1 kHz) and poor device lifetime (shot life ~1000 pulses), ill-suited to achieve the SWaP metrics

necessary for HPM pulse generators for the Navy afloat mission. Competitive solid-state solutions, such as inductive energy storage (IES) systems, utilizing a series stack of fast-opening diodes (drift-step recovery diodes (DSRD) and semiconductor opening switches (SOS)), have not been shown to break nanosecond barriers.

***Solution Space*:** Use viable pulse shaping/compression technologies based on semiconductor closing switches (e.g., delayed breakdown diodes (DBD), and fast ionization dynistors (FID)) to increase the peak power and shorten the rise time of the pulses produced by the DSRD-based pulse generator. Pulse sharpening/compression reduces the otherwise additional complexity of increased M×N stages within the pulser topology; a desired result towards achieving optimal SWaP metrics of the pulse generation system without sacrificing PRF, shot lifetime, and thermal management requirements. (*Please refer to the June 2021 MSR for full problem and solution space description).*

***Sub-Problem 1*:** Achieving an order of magnitude increase in peak power (1-to-10 MW) through compression/sharpening methods requires series and parallel stacks of semiconductor closing switches (SCS), ultimately resulting in increased pulse risetime. Determining the optimal combination of diode stacks to decrease pulse risetime and increase output power requires additional SPICE circuit simulations. However, device models for SCS are not commercially available and thus require maturing SCS device models based on experimental results and physics-based simulations, such as using packages such as T-CAD, which can be time consuming.

***Sub-Problem 2 (Fundamental Physics)*:** Sub-nanosecond high-power pulse sharpening using semiconductor devices is based on ultrafast delayed avalanche breakdown under steeply increasing reverse voltage applied, thereby initiating an impact ionization front. However, the phenomenon behind the origin of free carriers that trigger the impact ionization at higher-than-breakdown fields is not completely known. Further, it is not clear whether the switching (generation of electron–hole plasma) is uniform across the device area or is localized (filamentary). Such different mechanisms are believed to be dependent on device geometry and doping concentration, and are detrimental to the switching speed. A University of New Mexico study [1] has concluded that the operation of a silicon avalanche shaper (SAS) is inconsistent with the theory described by Russian scientists. More understanding of device operation from a fundamental physics perspective is necessary to enhance their performances.

***State-of-the-Art (SOTA)*:** Prototype sub-nanosecond solid-state pulsers based on semiconductor opening switches (SOS) and semiconductor sharpeners are shown to produce peak voltages (~500 kV), and peak power outputs (~5 GW). Solid-state power supplies providing peak power up to 800 MW are available to purchase from FID Technologies, Germany. *Please refer to Table 4.7.1 of the June MSR for list of devices and their performance metrics.*

***Deficiency in the SOTA*:** Prototype ~5 GW power supplies, such as SOS based S-500 system with semiconductor sharpeners, are large (>1 m^3). Commercially available moderate-power (~1 GW) all-solid-state pulsers utilizing semiconductor sharpeners have

long purchase lead time (~4 months). Their PRF capability is limited to ~1 kHz due to physical constraints in thermal management.

***Solution Proposed*:** Downselect viable pulse compression/shaping technologies which meet or exceed the performance parameters set forth in Section 6.3's Milestones A-D towards producing an all-solid-state, tens-of-megawatts, sub-nanosecond pulse generator with semiconductor sharpener without sacrificing PRF, shot lifetime, and thermal management requirements.

***Relevance to OSPRES Grant Objective*:** The alternative all-solid-state technologies discussed could individually, or in combination, provide the means to produce order(s) of magnitude greater peak power, without severe limitation to PRF, as SWaP-centric means to increase the capability and extent of protecting naval assets.

Risks, Payoffs, and Challenges:

***Risks*:** Semiconductor closing switches, such as DBD and FID are not available to purchase within the United States. Procuring devices from abroad could lead to significant delay in experiments and development of device fabrication technology. Undergoing time-intensive and complex simulations to then down-select one technology based on peak power output alone presents risk to other secondary or tertiary performance metrics such as PRF and pulse energy, which risks developing ill-suited technologies to support the float mission. Additionally, as new technology emerges via research, scope creep to numerically and experimentally evaluate new technologies may delay transitioning these technologies into viable systems.

***Payoffs*:** The SWaP tradeoff of generating a non-laser-based system with any number of these systems can yield a higher fidelity pulsed-power waveform output. Determining which technology is viable and feasible in terms of the key performance metrics should yield a more ultracompact form factor pulse generator with order(s) of magnitude greater power density without compromise to overall size and weight to the system.

***Challenges*:** Determining the true performance metrics of interest based on these highly different devices is challenging. Without a more robust and deep understanding of their operation, and how to utilize them within a pulse generator topology, in a swappable configuration or otherwise, requires additional time and consideration. Managing the tradeoff between the academic understanding of the technologies of interest presented in the foregoing table, and the transition to prototype effort/mentality, will require both a delicate balance and leveraging the pulsed-power team's combined effort.

5.5.2 Tasks and Milestones / Timeline / Status

(A) Milestone – Downselect viable pulse compression/shaping technology to be used in addition to currently utilized DSRD, which increases at least one of the key performance metrics by an order of magnitude without compromise to the overall volume of the system [*AUG21*].

1. Task – Finalize literature study of different technologies and topologies of SCS based pulse generators and compare SWaP tradeoff evaluation to PCSS- and DSRD/SOS-based pulse generators [*JUN–JUL21* / *Ongoing*].

2. Task – Determine commercially available technologies that could be used as pulse shaper/sharpening devices to improve pulse generator performance, and select appropriate devices for further experimental verification of their performance metrics [*JUN–AUG21* / *behind schedule*].

(B) Milestone – Model and experimentally verify the performance of the downselected technology as an additional component to the DSRDs utilized within a SOS-IES pulse generator. [*NOV21*].

1. Task – Develop T-CAD device model for the selected devices (DBD/DLD) based on available device information from the literature and perform device simulations for their performance under nanosecond input pulse conditions. *[In progress]*;
2. Task – Develop SPICE device model for the selected device based on T-CAD simulation. [*SEP–OCT21*];
3. Task – Design experimental circuit with one selected diode or dynistor and obtain theoretical performance metrics using standard electronic simulation tools such as LT-Spice using the device model developed in task 2. [*SEP–NOV21*];
4. Task – Experimentally verify whether the selected device topology can produce peak power and pulse risetime equivalent to or better than that of the SOTA. [*OCT–NOV21*].

(C) Milestone – Use Semiconductor Power Technologies (SPT) developed DSRDs and Voltage Multiplier Inc. developed Axial-lead Glass-body Diodes as alternatives to delayed breakdown diodes for pulse sharpening. [*Alternative to Milestone B, OCT–NOV21]*].

1. Task – Fabricate test fixtures for connecting DSRD and VMI diodes to DSRD–IES pulse generator, as described in **Section 6.4** or MegaImpulse PP10731 pulse generator. [*OCT–NOV21*];
2. Task – Test pulse sharpening using single, 2-stack, and 3-stack SPT DSRD and/or VMI diodes using the fixtures developed in Task 1. [*OCT–NOV21*]
3. Task – Prepare a performance matrix of DSRD and VMI diodes as pulse sharpeners as a function of variations in DSRD test parameters discussed in **Section 6.3**.

(D) Milestone – Model diode/dynistor topologies and fabrication process. [*on hold until Milestones A and B are completed*].

1. Task – Model silicon diode and dynistors, with optimized device cross section (size, geometry) based on theory and simulations to increase current and thermal dissipation. [*On hold*];
2. Task – Model/design fabrication process with optimum device topology and doping concentration. [*On hold*].

5.5.3 *Progress Made Since Last Report*

Focus this month was dedicated to advancing the effort described in Section 5.4.

5.5.4 *Summary of Significant Findings and Mission Impact*

(A) We have reviewed a number of literature reports on different approaches for pulse power generation and sub-nanosecond pulse sharpening, such as hydrogen spark-gap (HSG), solid-state pulse generators including SOS–IES based generator with semiconductor sharpener, diode-based non-linear transmission line, pulse generator based on Si and GaN photoconductive switches, and pulse generators with magnetic compression line. No single technology appears to meet or exceed the key performance metric requirements across the board. Where HSG lead in peak voltage and peak power, in comparison to the other technologies of interest, they lack in their ability to meet the required PRF, device lifetime, and SWaP-C metrics. All solid-state switching power supplies utilizing SOS and semiconductor sharpeners seem to be potentially viable technologies to compete against HSG with comparable or better SWaP-C metrics.

5.5.5 *References*

[1] E. Schamiloglu, C. B. Fleddermann, R. Focia, and J. Gaudet, “A STUDY OF ADVANCED SEMICONDUCTOR SWITCH PHYSICS AND TECHNOLOGY PHILLIPS LABORATORY Advanced Weapons and Survivability Directorate AIR FORCE MATERIEL COMMAND KIRTLAND AIR FORCE BASE, NM 87117-5776,” 1997.

6 Thermal Management

6.1 Ultra-Compact Integrated Cooling System Development

(Justin Clark, Roy Allen, and Sarvenaz Sobhansarbandi)

6.1.1 *Problem Statement, Approach, and Context*

Primary Problem: A thermal management system (TMS) is required for cooling semiconductor-based pulse-power devices, with the goal of maintaining the semiconductor device temperature below 80 °C. The proposed system must increase cooling densities, while decreasing pumping power requirements, in-line with the SWaP-C[2] objective.

Solution Space: To achieve such high cooling densities, an ultra-compact TMS (UC-TMS) directly integrated onto the semiconductor is proposed. Such a design is capable of creating turbulent flow in order to enhance the heat transfer rate. The proposed UC-TMS is restricted to 1 cm^2 surface area, therefore, the required pumping power should be kept to a minimum. An array of micro-sized jet nozzles will provide a turbulent flow onto a microchannel section directly on the semiconductor device. The UC-TMS design will reach turbulency at a faster rate while requiring less energy consumption.

Sub-Problem: The turbulency formed from the array of nozzles creates an extreme pressure loss from the large amount of jet nozzles (over 200) and a flow diameter of 100 microns. The pressure must be sustained to enable proper cooling and circulation processes.

State-of-the-Art (SOTA): Integrated chip cooling is being widely used to dramatically increase the operational power of high voltage silicon-based power devices. However, the current SOTA devices include individual parts which attach to a high-power device, causing less interaction between the semiconductor and coolant, degrading the heat removal rate.

Objective: The proposed UC-TMS design is based on refining in-chip jet-impingement geometry through leveraging theory and a parametric evaluation of nozzle geometry and flow channel arrangements. A Si-base unit will be prototyped to maneuver a higher capacity of heat removal. Moreover, to sustain the pressure, the application of different working fluids is suggested. Several types of coolant will be simulated to determine effects from fluid density and viscosity.

Anticipated Outcome(s): To create a UC-TMS with the ability to rapidly remove 1 kW/cm^2 of heat. A design capable of such high heat removal can be implemented on many applications such as high-power batteries.

Challenges: The manufacturing techniques of the semiconductor devices have not yet been adopted for integrated chip cooling systems. The proposed compact design is restricted due to low tolerance of the manufacturing process, as this process must be capable of layering the silicon TMS onto the semiconductor.

Risks: With a system so compact, the pressure drop could be a large issue regarding the objective heat dissipation rate. An extreme pressure drop would potentially cause the coolant to flow backwards, causing less fluid-to-solid interaction.

6.1.2 *Tasks and Milestones / Timeline / Status*

(A) Design a Si base 1 cm^2 UC-TMS, applying manufacturing tolerances, to achieve a heat dissipation rate of 1 kW/cm^2. The design must be able to be produced by manufacturing techniques such as etching and lithographic layering processes. To confirm the device can be manufactured as proposed, each section of the model will be layered step by step. / MAY21–AUG21 / Completed

(B) Using the optimal design, perform ANSYS simulations using either water or Si-C nanofluid. Other fluid types may be researched as pressure drop is a large factor / JUL21–DEC21 / In Progress

(C) Improve design parameters and sizing to have a lower pressure drop while having a high heat dissipation capability. Prove simulations from previous literature to show capable design configurations with acceptable pressure drop and steady temperature. / NOV21–JAN22 / In Progress

(D) With proper simulation results, manufacture a prototype to begin experimental testing and evaluation / JAN22–APR22 / Upcoming

6.1.3 *Progress Made Since Last Report*

A new student has been recruited and trained, and reporting will resume next month.

6.1.4 *Summary of Significant Findings and Mission Impact*

(A) From a literature review, similar designs were analyzed including a water-cooled, crossflow microchannel cooling system with various microchannel widths has been previously designed. The design achieved a simulated heat flux of 1.7 kW/cm^2 using 0.056 W of pumping power. Although this design is not the best fit when including the manufacturing constraints, the results using micro channel heat sinks are remarkable and design considerations are further analyzed. A similar design implemented the idea of having jets confined in their own individual spaces, experimentally reaching up to 900 W/ cm^2 with 0.83 W of pumping power. A third design analyzed two types of heat sinks with flat and oblique angled fins which were experimentally tested with a constant heat flux of 100 W/cm^2. The temperature difference was from 60 °C to 35 °C which proposed giving the design more power. The oblique angled fins caused 20 percent greater heat transfer than flat fins.

(B) To achieve a higher quality mesh around the nozzles and microchannels, the nozzles element size was initially set to 20 microns, or until the shape of the nozzles were more profound in a cylindrical shape. The surface which connects to the nozzles resulted with an element size of 15 microns and the nozzle sizing resulted in 13 microns. These values had to maintain an equivalent size to reduce the skewness and maintain mesh quality. Each surface with inadequate quality was selected and set to individual face sizing and is currently undergoing simulation.

To reduce the pressure loss while maintaining an effective turbulent flow produced by the jet nozzles, the microchannel fin designs did not effectively enhance the rate of heat transfer. The combination of micro channels and jet impingement caused too high of a pressure loss, causing the fluid to reverse its flow; therefore further enhancement of the UC-TMS will be based explicitly on jet impingement theory.

7 Pulse-Forming Networks

7.1 Diode-Based Nonlinear Transmission Lines

(Nicholas Gardner)

7.1.1 *Problem Statement, Approach, and Context*

Primary Problem: The size, weight, and cost of pulse forming/shaping networks (PFNs) need to be reduced and optimized for Navy afloat missions.

Solution Space: Develop a diode-based nonlinear transmission line (D-NLTL) as a pulse shaping network for the conversion of energy to the ultra-high frequency (UHF) band (0.3–3 GHz) at single MW peak power.

Sub-Problem: Metrics used for component selection are designed for D-NLTLs operating at sub 0.1 GHz frequencies. Using such metrics alone to design D-NLTLs capable of single GHz frequency generation introduces a trial by error nature to the design process wherein frequency/power generation predictions and measurements can differ by a few hundred MHz or the design potentially fails to operate at all.

State-of-the-Art (SOTA): D-NLTL prototypes have been shown to generate center frequencies of 0.2–0.5 GHz at kV amplitudes in a light-weight small-footprint circuit. Simulations of LE-NLTLs indicate achievable frequencies in the single GHz range.

Deficiency in the SOTA: Simulation/measurement agreement becomes increasingly sensitive to parameters and factors outside of inductive and capacitive element choice alone at frequencies above ~100 MHz. Disparities between measurement and simulation above contribute to a trial by error design process for D-NLTL networks.

Solution Proposed: Identify and characterize diode parameters affecting frequency generation in the context of a NLTL application via simulation and experiment, and identify limits/desired ranges required for UHF generation. Such parameters include, but are not limited to: diode frequency response, diode reverse bias hold-off voltage, diode small signal capacitance, diode chip/package parasitics, and diode relaxation time. The improved understanding of the explored parameters will be used to design and fabricate a D-NLTL capable of GHz center frequency generation at single MW peak powers.

Relevance to OSPRES Grant Objective: The SWaP-C^2 capabilities of D-NLTLs (shown in Figure 7.1.1) represent a potential solution to the size, weight, and cost optimization issue for PFNs on Navy afloat missions.

Figure 7.1.1. 20 cell D-NLTL of dimensions 1.1 x 23.45 cm constructed with commercial off the shelf components.

Risks, Payoffs, and Challenges: There exists a potential tradeoff between power and frequency generation. Devices such as ceramic capacitors may be used in a D-NLTL to generate high peak power due to their break down potentials in the 10s of kV, however,

such devices become highly resistive at 0.1–0.2 GHz frequencies. Diodes have been shown to be operational at frequencies upwards of 0.4 GHz, however, possess low hold-off potentials limiting peak output power. The payoff to overcoming these challenges is significant reductions in PFN size and cost.

7.1.2 *Tasks and Milestones / Timeline / Status*

(A) Milestone – Construct/demonstrate a prototype capable of UHF generation at low voltages (1–100 V excitation amplitude)

(A1) Break a low-voltage pulse into a sequence of solitons (SEP20)

(A2) Increase frequency generation past 200 MHz (NOV20)

(A3) Select diode candidate (junction capacitance <50 pF) and simulate expected results (Ongoing)

(A4) Design/fabricate/test line (Ongoing)

(A5) Write/Submit manuscript on D-NLTL design processes (Ongoing/In Revision)

(B) Milestone – Demonstrate tuning of waveform at low voltages using electrical or mechanical means (Completed with voltage biasing APR21)

(B1) Write/Submit manuscript on LV D-NLTL tuning circuit (Ongoing/In Revision)

(B2) Simulate a HV tunable D-NLTL topology using the K series epoxy diodes (**Completed DEC21**)

(B3) Design a PCB prototype HV Tunable D-NLTL

(B4) Demonstrate electrical tuning on a HV D-NLTL

(C) Milestone – Construct/demonstrate a prototype capable of frequency generation above 1 GHz at single MW peak powers (Completed MW peak power but not GHz center frequency – Ongoing)

(C1) Identify diode candidates with a hold-off voltage of several kV and a low signal junction capacitance under 100 pF (Completed JAN21)

(C2) Design/fabricate single diode prototypes (Completed JAN21)

(C3) Perform initial tests using half-barrel pulse source (Completed FEB21)

(C4) Refine simulation using measurements (Completed FEB21)

(C5) Test a prototype using two diodes in series (Completed FEB–MAR21)

(C6) Test lines using Mega Impulse source (Completed MAY21**)**

(C7) Test K50F D-NLTL using PCSS as a source (Completed JUN21)

(C8) Use simulations and tests to refine line for increased frequency generation (Completed JULY21)

(C9) Rebuild lines for negative polarity pulses (Completed JULY21)

(C10) Test lines using PCSS as a source with various cell inductances (Completed JULY**)**

(C11) Test lines using Marx Generator as a source (Completed AUG21)

(C12) Reconstruct PCSS strip line to produce a pulse similar to 5.1.2 (left) and retest (Ongoing AUG21)

(C13) Write/Submit manuscript on the GHz MW D-NLTL Prototype (Ongoing/In Revision)

(D) Milestone – Demonstrate power scalability using an array of D-NLTLs (On Hold – Prioritizing Milestone C)

(D1) Design a prototype capable of running two D-NLTLs simultaneously off of the same excitation pulse (Completed JUN21)

(D2) Demonstrate simultaneous operation of parallel D-NLTLs

(D3) Build a circuit capable of measuring the CV curve of low-voltage diodes and measure the CV curves of unused diodes and heavily used diodes (Completed JUN21)

(D4) Measure SMV1702 diode C(V) curve and compare against manufacturer specs

(D5) Measure C(V) curves for a sample of SMV1702 diodes for determination of degree of variability between diodes

7.1.3 *Progress Made Since Last Report*

All effort this month has been focused on preparing manuscripts for submission.

7.1.4 *Summary of Significant Findings and Mission Impact*

(A) After a failure of the high-voltage diode-based nonlinear transmission lines (D-NLTLs) to reproduce simulated results, work refocused on low-voltage D-NLTLs to determine the source of the discrepancy. In NOV2020 a center frequency of ~250 MHz was achieved using a D-NLTL design based on the diode model SMV1702.

(B) Following the success of the SMV1702 D-NLTL, a circuit was designed, capable of electrically tuning the center frequency utilizing DC biasing of the diodes. In FEB–APR2021 the circuit demonstrated a linear relationship between DC bias up to a limiting potential. Negative DC biases decreased center frequency while positive DC biases increased center frequency. A HV voltage tunable topology was simulated in the month of December indicating the center frequency can be altered by up to 50% of the unbiased center frequency with a voltage bias under 200 V.

(C) In JAN2021 two diode candidates (models K100F and K50F) were identified for a HV D-NLTL design. FEB2021 saw successful tests of both D-NLTLs with each sharpening the rise time of a pulse produced by a DSRD based source down from ~1 ns to ~600 ps. In AUG2021 the first major variation between the K50F and K100 F D-NLTLs was observed with the K50F line breaking the pulse into solitons while the K100F line primarily sharpened the rising edge of the pulse. In SEPT2021

comparisons between measured and simulated results for Marx+K50F measurements indicate further success in modeling inductor and diode parasitics to predict frequency generation.

(D) During MAY2021 a line topology capable of feeding two identical D-NLTLs with the same pulsed source at the same time was fabricated. Initial results were collected, and a prototype is currently being designed to test the ability to parallelize D-NLTLs.

7.2 Continuous Wave Diode-NLTL based Comb Generator

(Nicholas Gardner and John Bhamidipati)

7.2.1 *Problem Statement, Approach, and Context*

Primary Problem: When used as a pulse shaping network (PSN), diode-based nonlinear transmission lines (D-NLTLs) are promising solutions towards reducing the size, weight, and cost of RF and microwave sources on Navy afloat missions. However, D-NLTLs have a dynamic impedance, leading to signal/power reflection, standing wave generation, and return power losses at both the source–line and line–load interfaces, leading to difficulties in practical D-NLTL applications.

Sub-Problem: Design parameters for COTS high-frequency D-NLTL based comb generators capable of generating up to ~50 GHz output frequencies are limited to <1 Watt output powers, which is <0.1% of the power handling capability required for navy afloat missions. Using such metrics alone to design D-NLTLs capable of generating ~1–2 GHz frequency with capability to handle MW-order peak powers could potentially introduce design errors resulting in frequency/power prediction–measurement discrepancies on the order of a few hundred MHz.

Solution Space: Use a D-NLTL as a pulse shaping network (PSN) to convert continuous wave (CW) signals from low frequency–very high frequency (LF–VHF) bands (0.03 MHz–30 MHz) to the ultra-high frequency (UHF) band (0.3–3 GHz) at ones-of-MW peak power. Such an application will reduce impedance mismatch effects at the source–line interface by continuously oscillating D-NLTL impedance between the same two values. Use of MW D-NLTLs in the comb generator will push output frequency up to ranges required for Navy afloat missions.

State-of-the-Art (SOTA): Commercial-off-the-shelf (COTS) GaAs varactor diode-based monolithic microwave integrated circuit (MMIC) D-NLTL comb generators are capable of operating at input and output frequencies up to 600 MHz and 30 GHz, respectively. However, these comb generators are not capable of handling powers higher than 27 dBm (0.51 W). In-house pulsed D-NLTL prototypes have been shown to generate center frequencies of 0.2–0.5 GHz at kV amplitudes in a light-weight small-footprint circuit. Further D-NLTL network efficiency is hindered by a signal-dependent impedance characteristic to the network leaving reported efficiencies of RF content generation at 10% or less of incident pulse energy.

Objective 1: Design and demonstrate a high voltage D-NLTL based comb generator capable of L-Band Frequency generation and 0.1–5 MW power generation.

Objective 2: Increase D-NLTL network efficiency above the reported 10% threshold through use of CW sources suppressing impedance mismatch effects presented by the signal-dependent impedance characteristic to D-NLTLs.

Anticipated Outcome(s): A successful demonstration of improvements to impedance matching at the source–line interface using a CW signal measured as a reduction in signal amplitude loss between the source and D-NLTL.

Challenges: Nonlinear signal-dependent behavior provided by a reverse bias diode produces difficulties in predicting generated waveform behavior. Further D-NLTL performance is limited in both frequency and power generation by the availability and variety of COTS Schottky and epoxy diodes.

Risks: The reverse bias hold off potential (V_R) of a chosen diode limits the power generation capabilities of the system. If an excitation is used that exceeds V_R, diodes risk being damaged. Further reflections produced at the source–line interface caused by a signal dependent impedance can damage a CW source sensitive to such reflections.

7.2.2 *Tasks and Milestones / Timeline / Status*

(A) Demonstrate an ability of a CW excitation signal to reduce the source–line impedance mismatch effect on signal amplitude present in D-NLTLs when compared to a pulsed excitation signal, first through simulations and then by validating the results experimentally using low voltage (LV) and high voltage (HV) prototypes.

(A1) Show the potential to improve source–line impedance mismatch in simulation (Completed SEP21)

(A2) Experimentally demonstrate a low voltage (LV) prototype receiving a CW input (Completed SEP21)

(A3) Compare measured results with simulation behavior; comparison of results will be used to further refine D-NLTL simulation techniques (Ongoing)

(A4) Determine if there are improvements to system behavior if D-NLTL diodes are biased when receiving a CW input (Ongoing)

(A5) Demonstrate improvements to the source–line impedance mismatch in a LV prototype (Ongoing)

(A6) Demonstrate a HV prototype receiving a CW input (Completed NOV21)

(B) Demonstrate UHF – L-band (0.3–2 GHz frequency) generation with a CW D-NLTL.

(B1) Excitation of K100F and K50F D-NLTLs using a 700 MHz signal from the R&S amplifier (Completed NOV21)

(B2) Compare measurement with simulation to further refine simulation measurements. (**Ongoing**)

(B3) Simulate topologies capable of utilizing a bipolar pulse for CW applications. (**Ongoing**)

(C) Demonstrate UHF generation at single MW power levels with a CW D-NLTL.

7.2.3 *Progress Made Since Last Report*

(B2) Experimental measurements have been performed using the Rohde & Schwarz (R&S) amplifier on the D-NLTL lines based on the K100F and K50F epoxy diodes to verify the measurements from the November report. The results are discussed in section 7.2.4. Though very little agreement has been observed when compared with the simulated results, these measurements have provided much needed insight into the extent of source–line impedance mismatch existing in the HV lines.

7.2.4 *Technical Results*

(B2) D-NLTL lines based on the K50F and K100F epoxy diodes have been tested with a 7 $V_{p\text{-}p}$(+4V and -3 V), 700 MHz (10W) sinusoidal pulse from an R&S amplifier with a 7 $V_{p\text{-}p}$. The K50F line has demonstrated pulse sharpening as shown in Figure 7.2.1 while doubling the frequency as reported previously. Shockwave front generation is absent in this configuration due to the the C–V characteristics of the diodes. However, when excited at 70 $V_{p\text{-}p}$, i.e., with a 100 W 700 MHz sinusoid, both K50F and K100F lines have reflected ~70% of the input power back to the source due to impedance mismatch, leaving the line efficiency <7%. The expectation of the continuous AC averaging out the impedance mismatch to provide better source–load coupling has not been reached. Further simulation efforts for the HV line will focus on finding the source of the mismatch.

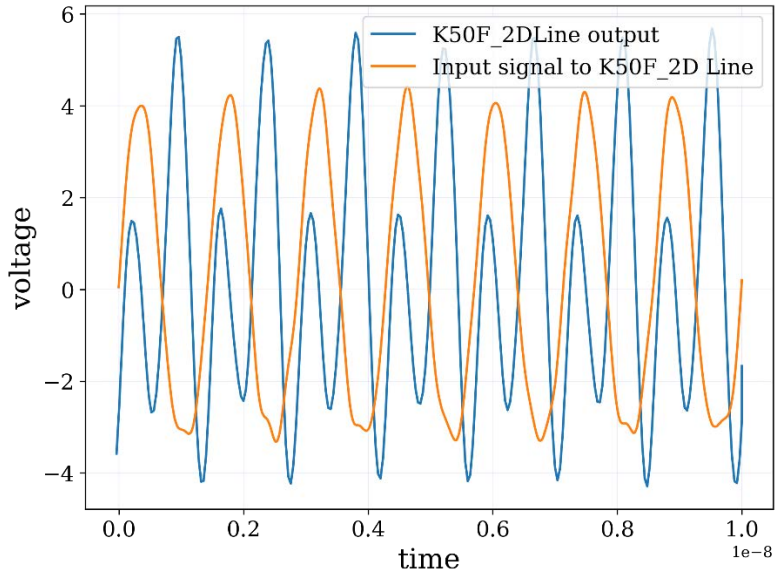


Figure 7.2.1. K50F measured results when excited with a 700 MHz 7 $V_{p\text{-}p}$ sine wave

7.2.5 *Summary of Significant Findings and Mission Impact*

(A) In the month of September, a LV prototype was given several continuous waveforms to observe initial behavior of a D-NLTL with a CW source. The LV D-NLTL demonstrated a capability to receive a CW based source. No effect on the source–line impedance mismatch was observed for the LV tests. During the month of November two high-voltage D-NLTLs based on epoxy diodes were tested using a sinusoidal waveform amplified by an R&S amplifier. Each D-NLTL demonstrated a

capability to function with a CW source, however little to no effect was observed on the source–line impedance mismatch.

(B) Two high voltage D-NLTLs based on epoxy diodes of models K50F and K100F were tested using a 700 MHz sinusoidal signal amplified by an R&S Amplifier. While pulse sharpening has been observed at low voltage (7 Vp-p) excitation in the K50F line alongside frequency doubling behavior (1.4 GHz output frequency) reported previously, , >65% power reflection has been observed in both the lines at 70 Vp-p excitation, resulting in <7% line efficiency.

7.3 Pulse-Compression-Based Signal Amplification

(Feyza Berber Halmen)

7.3.1 *Problem Statement, Approach, and Context*

Primary Problem: Solid-state amplifiers, such as gallium-nitride-based high electron mobility transistors (GaN HEMT), can be used as high power microwave (HPM) sources to achieve the SWAP-C2 performance metrics necessary to support the cUAV Naval afloat mission. However, even the best high-power GaN HEMTs are limited to 2–3 kW of peak power, much lower than the 0.1 to 3 MW pulsed power available from traditional HPM sources such as TWTs. Achieving a power density of 1 W/cm^2 at a distance of 10 m with a high gain (≥ 10-dBi) narrow-band antenna requires an input power increase of two to three orders of magnitude. Power combination methods to achieve an effective radiated power (ERP) at MW scale require 10s to 100s of GaN HEMTs, compromising the SWAP-C2 performance.

Solution Space: Pulse compression techniques are used to increase the peak power and lessen the pulse width in HPM applications. Adapting pulse compression at the GaN HEMT or any other SWAP-C2 compatible source output can achieve sufficient ERP with an optimal radiating element.

Sub-Problem**:** Pulse compression is generally used to generate a pulsed output with a high peak output power (P_{out_peak}) and a wideband frequency content from a DC input voltage. The main challenge lies in identifying a pulse compression technique that can be used to amplify a narrowband RF input signal. Some of the circuit elements for common pulse compression techniques, such as the saturable inductors used for energy storage in magnetic pulse compression (MPC), exhibit increasingly lossy behavior with high frequency. Another challenge will be to determine, if any, the operating frequency limits of the suitable pulse compression technique for high-frequency, high-power signals.

State-of-the-Art (SOTA): Large magnetic pulse compression (MPC) circuits (>1-m^3, >1000-lbs) have demonstrated peak output power up to a few GWs. Smaller versions (~0.125-m^3, 50-lbs to 100-lbs) can achieve 7.5 MW peak power [1].

Deficiency in the SOTA: Traditional MPC systems are large (few meters long), leverage huge transformers, and require liquid coolant such as transformer oil, which leads to undesirable system mass values of ≥1000 lbs. They are used for generating medium or high pulse power traditionally from DC or AC (50/60Hz) high voltage supplies. There is no known example of high-frequency signal amplification utilizing MPC.

Solution Proposed: Developing a pulse compression circuit that will act as a high-power signal amplifier with a gain of ≥10. Utilizing magnetic pulse compression, or any other suitable pulse compression method, for high power signal amplification with source fidelity.

Relevance to OSPRES Grant Objective: Pulse compression will enable a size and cost efficient solution to high power signal amplification that will lead to HPM source development with optimal SWaP-C2 parameters.

Risks, Payoffs, and Challenges:

Challenges: Modeling pulse compression circuits for high-frequency operation can present a challenge. Pulse compression circuits are generally evaluated in SPICE simulators with low frequency AC / transient simulations. SPICE is a lumped-element model simulator and cannot solve for the distributed-element model required at high frequencies where the wavelengths become comparable to the physical dimensions of the circuit. Some circuit components, such as the saturable inductor in the MPC, are not available in SPICE or many other simulators and need to be modeled using behavioral models and proprietary material data. Pulse compression circuit modeling, especially at high frequencies, needs to be investigated.

Risks: Pulse compression methods are usually lossy in nature and generate a considerable amount of heat; therefore, designing a proper cooling method must be carried out, which may inadvertently increase the volume (size and weight) of the overall design.

7.3.2 *Tasks and Milestones / Timeline / Status*

(A) Milestone – -Demonstrate 2–3 times increase in peak power and compression gain using magnetic pulse compression (MPC) [*estimated completion by MAR22*].

1. Subtask – Model saturable inductors in LTSpice or Matlab/Simulink in order to be able to develop MPC simulations / NOV21 / Ongoing.
2. Subtask – Design of MPC circuit with RF input and simulation in LTSpice or Matlab/Simulink to evaluate the resulting amplification and frequency content. / [On hold until the saturable inductor simulation model is realized].
3. Subtask – Model the high frequency behavior of MPC circuit / NOV21 / Ongoing.
4. Subtask – Build and test the MPC prototype using bench top power supply / OCT–*DEC21 / Ongoing*.

(B) Milestone – Increase the compression gain available from MPC.

(C) Milestone – Build and test SWAP-c2 compatible high-frequency MPC prototype with GaN source.

7.3.3 *Progress Made Since Last Report*

(A.3) High-frequency losses for magnetic cores have been compiled. Magnetic core selection criteria were established based on loss and MPC operation constraints.

7.3.4 *Technical Results*

(A.3) Magnetic core losses were investigated in order to determine the saturable inductor core characteristics suitable for high-frequency pulse compression. Magnetic core losses are classified in three groups: hysteresis, eddy current, and anomalous. Hysteresis loss is a common dissipative process in magnetic materials, analogous to 'friction' in rotating magnetic dipoles, and quantifies the energy lost in moving the operating point. The area inside the hysteresis loop gives the energy lost in the material in one cycle of the applied field:

$$W_H = A_e l_e \int H dB \tag{1}$$

where A_e and l_e are the effective magnetic area and length, respectively. Eddy current losses are due to voltage induced in the core finite resistance, caused by varying magnetic fields. Resulting power loss in one cycle is proportional to the eddy current loop area and inversely proportional to the core resistance:

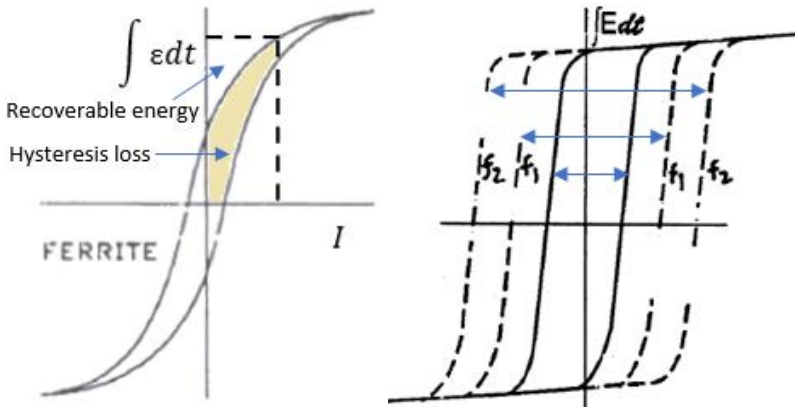
$$\boldsymbol{P_E} \propto \frac{\boldsymbol{A_{eddy\ current\ loop\ area}}}{\boldsymbol{R_C}} \tag{2}$$

In order to minimize eddy currents, core resistance should be very high, and the eddy current loop area should be minimized, which can be realized by core processing methods such as lamination. All the remaining losses caused by other mechanisms are called anomalous or residual losses.

Legg's equation for total loss provides an insight into the contribution of each loss [2]:

$$\frac{R_C}{\mu L} = aB_m f + cf + ef^2 \tag{3}$$

R_C, L, and μ are the core's effective ac resistance, inductance, and permeability, respectively. Hysteresis loss, shown in Figure 7.3.1 (a), is the first term of the Legg's equation and it increases with the maximum flux density, B_m, of the operation. Hysteresis and anomalous losses are proportional to operating frequency, whereas the eddy current loss increases with the square of frequency. The frequency dependence of losses results in the widening of core hysteresis loop with increasing frequency as depicted in Figure 7.3.1 (b). For pulse compression at high frequencies, losses will be the main limitation. They can be minimized by using a core with narrow initial hysteresis loop and a magnetic material composition optimized for eddy current reduction.



(a) (b)

Figure 7.3.1. (a) Hysteresis loss and (b) change of hysteresis loop with frequency [3].

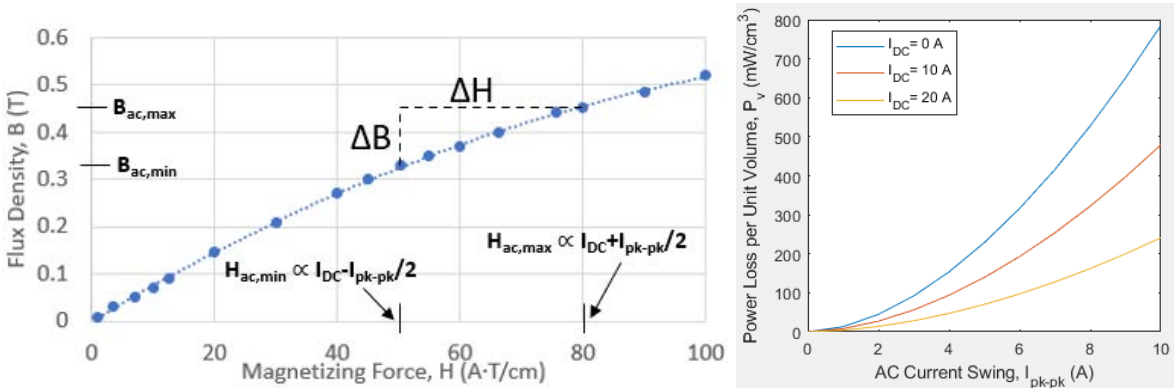
Legg's Equation is valid at low flux densities. A more accurate loss calculation for sinusoidal excitation at higher flux densities can be obtained through Steinmetz's Equation [4]:

$$P_v = k \cdot f^a \cdot {B_m}^b \tag{4}$$

P_v is the time average power loss per unit volume, B_m is the peak flux density calculated as half the flux swing, and a, b and k are the Steinmetz coefficients, normally provided by the manufacturer. Typically, 1<a<3 and 2<b<3 and the actual coefficient values depend on the magnetic core material. Flux swing is the most important design parameter to minimize the loss, especially with AC excitation. Flux density, B, is a function of magnetizing field, H, which in turn is a function of current, number of turns, N, and effective magnetic path length through Ampere's Law:

$$B = \mu H \quad \text{and} \quad H = \frac{N}{l_e} I \tag{5}$$

The current swing ($I_{DC} \pm I_{pk\text{-}pk}/2$) through an inductor results in a proportional flux swing, ΔB, and peak flux density, $B_m = \Delta B/2$, as illustrated in Figure 7.3.2 (a) (only positive B-H quadrant depicted). Resulting P_v for increasing AC current swing, $I_{pk\text{-}pk}$, is plotted in Figure 7.3.2 (b). Data from a Kool Mμ powder core with extremely narrow hysteresis loop and Steinmetz coefficients k=62.65, a=1.36 and b=1.781 is used for the figures [5]. For a pure AC current (I_{DC}=0A), the flux swing is between ± B_m and the power loss is at maximum. DC bias can be added to AC current to reduce the power loss as depicted in the same figure. Main reason for the decrease in power loss is the shift of operating point to a low permeability, i.e., reduced B-H slope, region. Neither including DC bias nor using a low permeability core seems to be a feasible option for the high frequency pulse compression circuit due to other design considerations.



(a) (b)

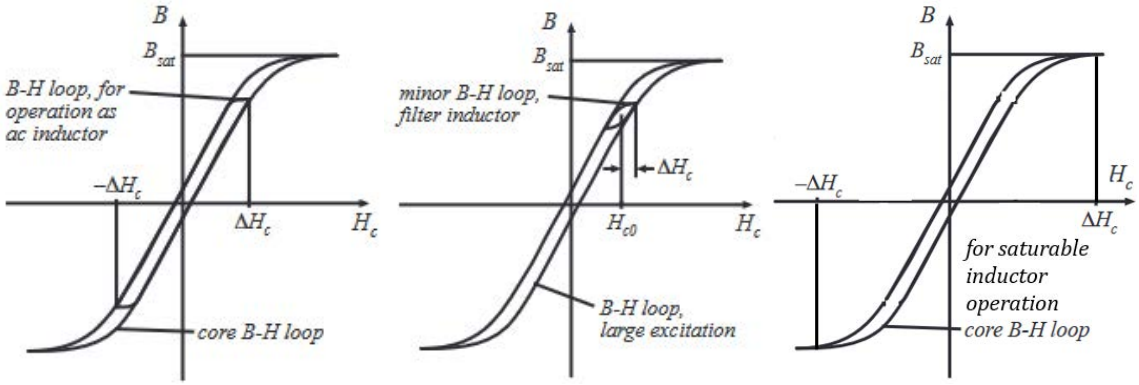
Figure 7.3.2. Change in (a) flux swing with AC current and (b) P_v with AC and DC current

Another method to reduce the losses, especially the eddy current losses, can be through the signal duty cycle. Eddy current losses can be modelled as a resistor, R_E, in parallel with the low-frequency inductance of the magnetic core [3]. Resulting loss can then be approximated from the voltage across this resistor as V_{rms}^2/R_E. Accordingly, loss for a pulse of peak voltage V_p and pulse duration t_p is:

$$Loss = \frac{V_P^2}{R_E}\frac{t_p}{T} \tag{6}$$

Eddy current losses increase with square of peak voltage and decrease with reduced pulse width for a given frequency. This concept could be exploited in the high frequency pulse compression, however, time integral of the applied voltage is an important design parameter and tradeoffs should be considered.

The idea behind magnetic pulse compression is to utilize the large impedance change in saturable inductors as their flux density moves between saturation and non-saturation regions in the B-H loop. Figures 7.3.3 (a), (b) and (c) show B-H loops for ac inductor, filter inductor and saturable inductor, respectively, in order to illustrate the difference between operating points and expected losses for different applications. With a regular ac inductor, the operating point moves between a positive and negative flux density avoiding the saturation regions. An inductor used for filtering is designed to have a small ac current ripple compared to the dc current to ensure it is operated within a minor B-H loop and the loss is minimized. For the saturable inductor with ac input, the operation is similar to that of the ac inductor but covers the whole B-H loop, and the losses are at maximum as $B_m=B_{sat}$ for Equation (4). A DC bias could be added to the saturable inductor input to reduce the losses as discussed previously. However, this would limit the operation to positive B-H loop (for positive DC) and result in the pulse compression circuit conducting only half cycle as there will be no saturation for the DC-shifted negative cycle of the AC signal. This could be considered if no other methods for loss reduction are available.



(a) (b) (c)

Figure 7.3.3. B-H loops for operation as (a) AC, (b) filter, and (c) saturable inductor

Change in flux density happens either by current flowing through the inductor magnetizing the core at a field intensity H, as given by (5), or through the voltage applied to the windings, as governed by Faraday's Law:

$$\varepsilon = -N\frac{d\phi}{dt} \quad \text{and} \quad \phi = B \cdot A_e \tag{7}$$

From (5) and (7), the condition for saturation with current or voltage input is obtained as follows:

$$L \cdot I > B_{sat} \cdot N \cdot A_e \tag{8}$$

$$V \cdot t > B_{sat} \cdot N \cdot A_e \tag{9}$$

These conditions need to be modified for periodic signals as they are derived for DC current and DC voltage pulse of duration t and peak V. For example, B_{sat} is multiplied by a factor of 4.4 ($2\pi/\sqrt{2}$) for a sinusoidal input voltage and 4 for a square wave input and t is replaced with signal period T. As the traditional series MPC uses voltage input to saturate the inductor, the rest of the analysis will focus on that.

Equation (9) determines the minimum operating V·T product for a given core of saturation flux density B_{sat} and magnetic cross-sectional area A_e with number of windings, N. In order to guarantee saturation at high frequency operation, where T is very small, BNA product needs to be minimized. Assuming N=1, the maximum B_{sat} allowable to ensure core saturation for a given sinusoidal input is plotted in Figure 7.3.4 for two different toroidal core cross-sectional areas. A one-inch outer diameter toroidal core (A_e=0.654cm^2), should have B_{sat} < 0.3 mT in order to be saturated by a 1GHz input of 100V, i.e., VT=10^{-7} Vs. For comparison, note that typical saturation flux densities reported for power ferrite, MPP, Iron Powder, and High Flux are 0.4T, 0.7T, 1T, and 1.5T, respectively [6]. More extensive research into minimum core cross-sectional areas and B_{sat} values need to be done; however, these values for commercially available magnetic cores will probably set the limit for MPC frequency.

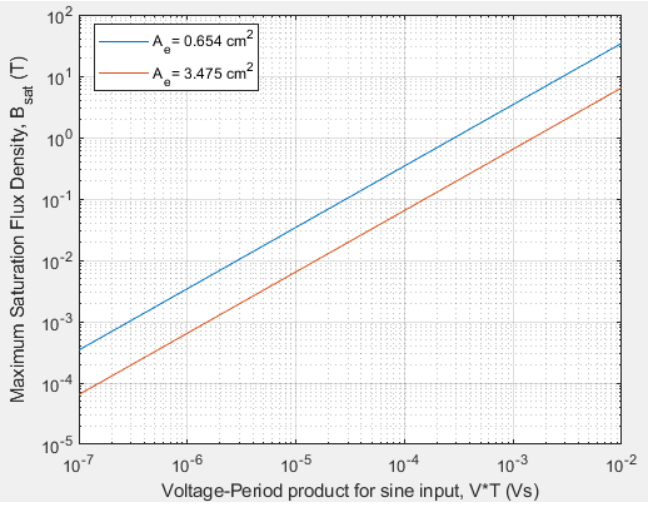
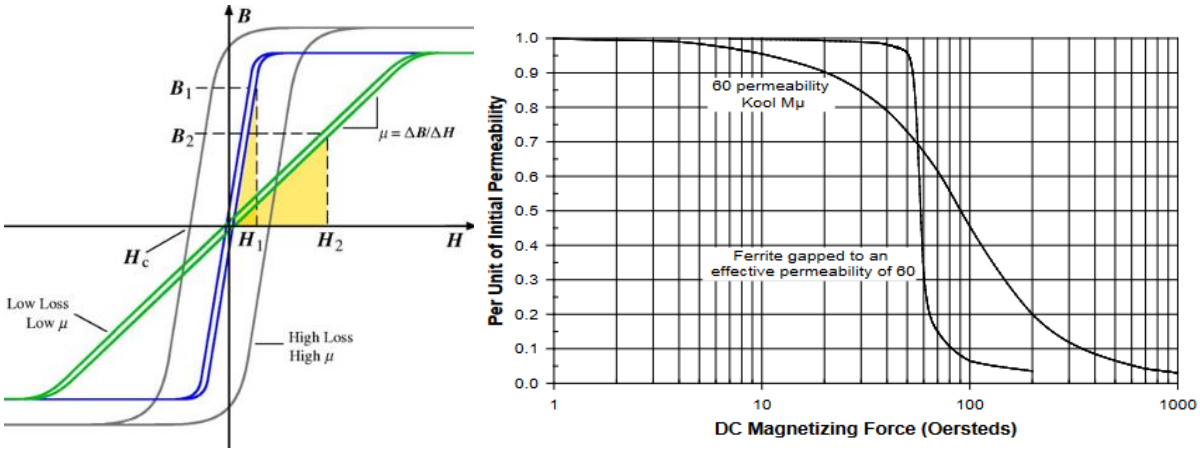


Figure 7.3.4. Maximum allowable saturation flux density for a given voltage-period product to ensure core saturation with sine input

Another consideration for the magnetic core is the saturation behavior. Ideal magnetic materials have a square B-H loop characteristics, like the blue loop in Figure 7.3.5(a), with high slope, hence permeability. Magnetic cores with “soft saturation” behavior (green loop), on the other hand, display a gradual change in B-H slope before saturation is reached. Kool Mμ powder core and Gapped Ferrite permeabilities depicted in 7.3.5 (b) correspond to “soft” and “sharp” saturation behavior, respectively. Permeability is constant up until saturation for Gapped Ferrite, whereas it changes constantly with H for the Kool Mμ core with soft saturation. The permeability change directly affects the impedances in the circuit as L∝ μ.



(a) (b)

Figure 7.3.5. (a) Sharp and soft saturation [7] and (b) corresponding change in μ [8]

For MPC to work properly, a very sharp change in permeability is required. Consider the 3-stage MPC circuit depicted in Figure 7.3.6. During time t_1, L1 and L2 present very high impedances, similar to an open switch, so that there is current flow only in the first stage.

During t_2, L2 preserves its high impedance while L1 is saturated and presents a low impedance path for the current flow. If L1 and L2 are designed with cores with soft saturation, their impedances will start decreasing as soon as the voltage at the node before the inductor starts increasing. This will result in current flowing through more than one stage at a given time. Rather than a sharp current in a limited time, there will be a gradually increasing current from the beginning of the operation. Pulse compression, will fail or have very limited gain, depending on the soft saturation characteristics and resulting pre-pulse currents. Therefore, a magnetic core with high permeability and sharp saturation is preferred for the MPC circuit for the inductors to minimize pre-pulse currents by presenting high impedance prior to saturation.

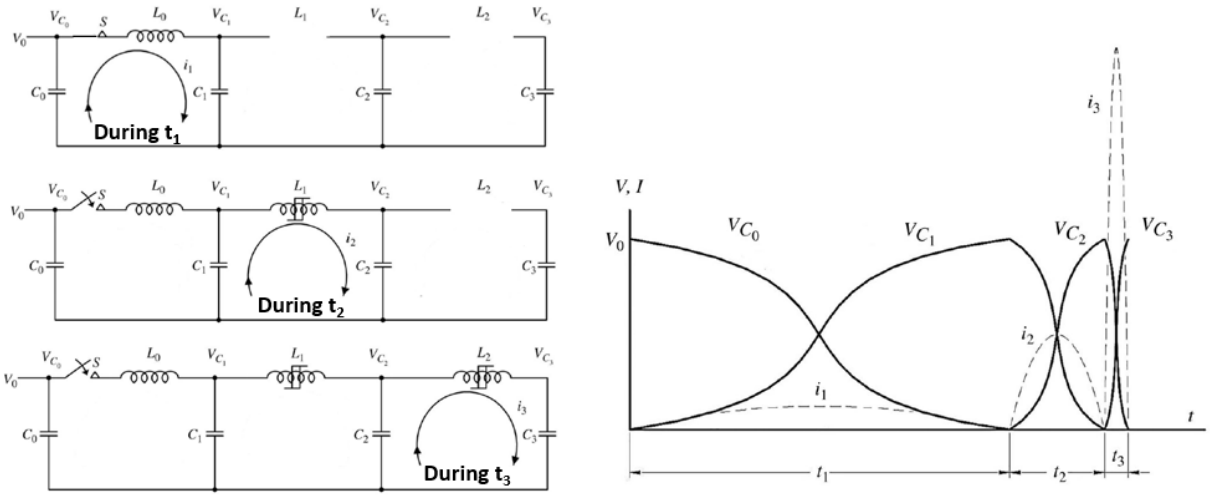


Figure 7.3.6. 3-stage MPC operation

Final and most important consideration for the core is the complex permeability behavior and the resulting cutoff frequency. B and H has a scalar relation defined with scalar permeability, μ, at low frequency. At high frequency, they interact with each other with some time lag. Defining δ as the phase delay of B from H:

$$H = H_0 e^{j\omega t} \quad \text{and} \quad B = B_0 e^{j(\omega t - \delta)} \implies \mu = \frac{B_0}{H_0} e^{-j\delta} \tag{10}$$

Complex permeability and loss tangent are then derived using Euler's formula:

$$\bar{\mu} = \frac{B_0}{H_0} cos\,\delta - j\frac{B_0}{H_0} sin\,\delta \implies \bar{\mu} = \mu' - j\mu'' \quad \text{and} \quad tan\,\delta = \frac{\mu''}{\mu'} \tag{11}$$

Loss tangent provides a measure of how much power is lost in the material. μ' is the inductance component, whereas μ" is the loss component which can be observed through the complex impedance:

$$\bar{Z} = j\omega\bar{\mu}L_0 = j\omega\mu' L_0 + \omega\mu'' L_0 \tag{12}$$

A typical magnetic core complex permeability is shown in Figure 7.3.7. At low frequencies $\bar{\mu} \approx \mu'$. At cutoff frequency, μ' starts dropping sharply, μ" reaches its peak, and the impedance becomes more resistive than inductive according to (12). Cutoff frequency is

reported to be inversely proportional to the initial permeability of the material according to Snoek's Law [10]. Complex permeability and cutoff frequency data need to be gathered to determine the frequency limits of different magnetic cores.

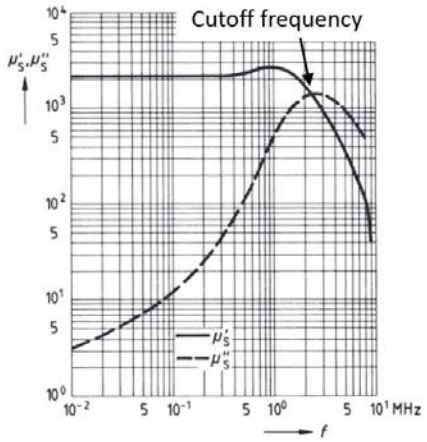


Figure 7.3.7. Typical magnetic core complex permeability [9]

7.3.5 *Summary of Significant Findings and Mission Impact*

(A) Magnetic core losses have been investigated. Core selection constraints were determined based on core losses and high frequency MPC design considerations. Possible changes to input signal in order to increase the operating frequency have also been identified. Significant findings are summarized below:

a. A core with high resistance, minimized eddy current loop area, and narrow hysteresis loop is needed to minimize core losses
b. A core with high permeability and very sharp saturation characteristics is preferred to minimize the pre-pulse currents and the MPC circuit losses.
c. The core cutoff frequency, at which the core becomes more resistive than inductive due to complex permeability, will determine the upper limit of the MPC operating frequency.
d. A core with a very small cross-sectional area and very low B_{sat} is needed to maximize the operating frequency as the core needs to be saturated with $VT>4.4B_{sat}NA_e$ for sinusoidal input MPC operation.
e. DC bias can be added to RF input to minimize the hysteresis losses and the VT product required for saturation. This will be the last resort as MPC output is limited to half cycle with this option.
f. Duty cycle reduction can also be used for loss minimization, but it would reduce the operating frequency as the time integral of input will be lower.

7.3.6 *References*

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8 Antenna Development

8.1 Tradespace Analysis of an Array of Electrically Small Antennas (ESAs)

(Bidisha Barman and Deb Chatterjee)

8.1.1 *Problem Statement, Approach, and Context*

Primary Problem: Determine the extent to which the physical aperture size of an antenna array, composed of patch elements, can be reduced, while maintaining performance in peak power density, bandwidth, and electronic beam steerability over the UHF range (0.4–1 GHz), compared with present-art high-power-microwave-capable antenna arrays.

Solution Space: An array of patch antenna elements whose feed, two-dimensional shape, and relative placement (i.e., intra-, and inter-element design) allow for the physical aperture size to be reduced by more than 20% compared with the present-art.

Sub-Problem: To overcome scan blindness (as the main beam is electronically steered), due to the excitation of surface waves (SW). (Note: scan blindness is a common phenomenon in electrically small microstrip patch antenna arrays).

State-of-the-Art (SOTA): Horn, reflector, Vivaldi, valentine, etc. are some of the commonly used ultra-wideband (UWB) antenna elements in a phased array for high-power microwave (HPM) transmissions.

Deficiency in SOTA: Large physical aperture size of the antennas.

Solution Proposed: Using electrically small antennas (ESAs) as array elements and optimizing their performance in terms of both near-field (bandwidth) and far-field (directivity) parameters, followed by arrangement of the ESAs in suitable lattice structures (preferably, hexagonal/triangular) to reduce the overall array aperture area. Using stochastic and machine learning (ML) algorithms to optimize antenna element and array performance.

Relevance to OSPRES Grant Objective: Provides design and optimization guidelines for UWB ESA elements, especially coaxial probe-fed microstrip patch antennas, and arrays for HPM applications.

8.1.2 *Tasks and Milestones / Timeline / Status*

(A) Develop an Array Pattern Tool in the context of lightweight calculations of large antenna arrays / JAN–MAY 2021 / Completed code.

(B) Investigate the effects of array aperture area reduction on different array parameters (such as gain, beamwidth, electronic beam steerability) and present a comparative study of antenna array parameters as a function of array aperture area / JAN–MAY 2021 / Completed investigations of arrays on infinite ground planes.

(C) Build minimum viable validation prototypes of single ESA elements on substrates that have good power handling capabilities for HPM transmissions at UHF range (such as polyethylene, FR-4, TMM-10i, TMM-6) / JAN 2021–MAR 2022 / Initiated designing of custom connectors for feeding ESAs in the UHF range.

(D) Optimization of ESA (single element) performance using ML based stochastic search algorithms / JUN 2021–MAR 2022 / Ongoing ML-based multi-objective-optimization (MOO) of ESA elements.

(E) Build minimum viable validation prototypes for arrays of ESA elements/ JUN 2021–MAY 2022/ Ongoing designing of 4×4 square and 10-hex array of ESAs.

(F) Optimization of array performance using ML algorithms / SEP 2021–MAY 2022 / Ongoing ML-based MOO of antenna array parameters.

8.1.3 *Progress Made Since Last Report*

(C) Build minimum viable validation prototypes of single ESA elements:

a. Tested the S_{11}-parameter of a newly manufactured coaxial-probe-fed, narrowband, microstrip patch antenna that is designed on a 3-D printed SLA substrate for operation at ~950 MHz.

b. Initiated the design of customized coaxial connectors to use as feeds for microstrip patch antennas in the UHF range (0.7–1 GHz).

(E) Build minimum viable validation prototypes for arrays of ESA elements:

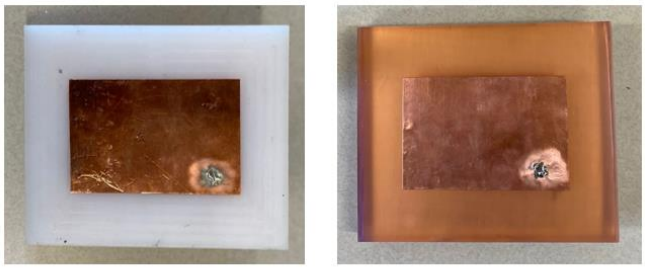
a. Initiated the design of two arrays (a 4×4 square and a 10-element hexagonal array) of ESA elements in the upper S-band (2.5–5 GHz).

8.1.4 *Technical Results*

(C) Build minimum viable validation prototypes of single ESA elements:

A narrowband, coaxial probe-fed, microstrip patch antenna that was manufactured on a 0.65-mm-thick, HDPE substrate was reported in last month's OSPRES-Grant MSR. The simulated and measured S_{11}-parameter and realized gains of the antenna were found to be in good agreement with each other.

To check if the prototype can be manufactured in-house in a more cost-effective and easier way, the antenna was 3-D printed on an SLA substrate (of same thickness), which has a dielectric constant close to that of HDPE. Fig. 8.1.1. shows the manufactured prototypes of the antenna on two different substrates. It can be observed from Fig. 8.1.2. that the S_{11}-parameter of the HDPE prototype has better agreement with the simulated data compared to the SLA-prototype. The shift in resonant frequency of the SLA patch antenna may be attributed to the slight change in the dielectric constant of the substrate.



(a) (b)

Figure 8.1.1. Manufactured prototypes of the narrowband, coaxial probe-fed, microstrip patch antenna, on 0.65-inch-thick, PEC-backed (a) HDPE and (b) 3-D printed SLA substrates.

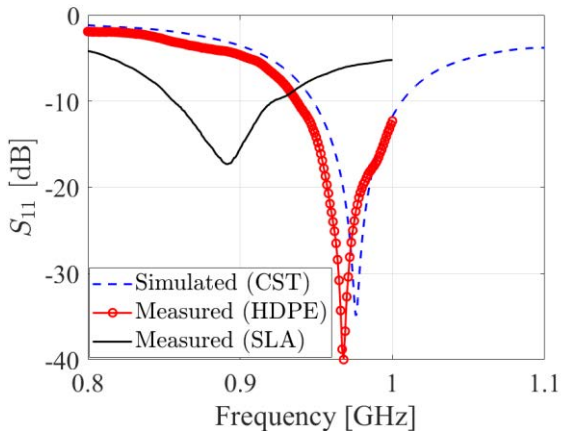


Figure 8.1.2. Comparison of the measured and simulated S_{11}-parameters of the narrowband, coaxial-probe-fed microstrip patch antenna elements.

The antenna designs, discussed so far, show narrowband behaviors. The bandwidth of these antennas can be enhanced by carefully selecting the location and dimension of the feed-probe. It was reported earlier (ONR-OSPRES-Grant MSR NOV 2021) that impedance bandwidth in excess of 30% can be achieved by placing the feed-probe along 2/3rd of the patch diagonal and with a probe radius $r_p \geq 0.005\lambda$ (with λ being the wavelength at the antenna's center frequency of operation. This implies that at the desired UHF range (0.6–1 GHz) the radius of the feed-probes must be $r_p \geq 2$ mm. However, the standard SMA or N-type connectors that are available commercially have $r_p = 0.635 - 0.65$ mm.

To meet the requirements of broadband coaxial probe-fed microstrip patch ESA element designs in the UHF range, the design of a custom coaxial connector (with $r_p \geq 0.005\lambda$) has been initiated. The custom connector consists of a thicker center conductor (which must be embedded in the dielectric substrate) that tapers to the standard SMA connector dimension as illustrated in Fig. 8.1.3. The tapering is necessary as the antenna must be connected to the ports of standard instruments (e.g., VNAs) for excitation and measurement. Fig. 8.1.4. shows the comparison between the simulated VSWRs of the antenna, with and without custom connector. The microstrip patch antenna design chosen

for the purpose is the same 0.65-mm-thick-HDPE based antenna reported in Fig. 8.1.1(a), with the standard SMA connector replaced by the custom connector. The preliminary results, in Fig. 8.1.4, shows that on using the custom connector, the 2:1 VSWR bandwidth is enhanced from 7% to 33%. The connector design will be further optimized to obtain a better VSWR performance before manufacturing.

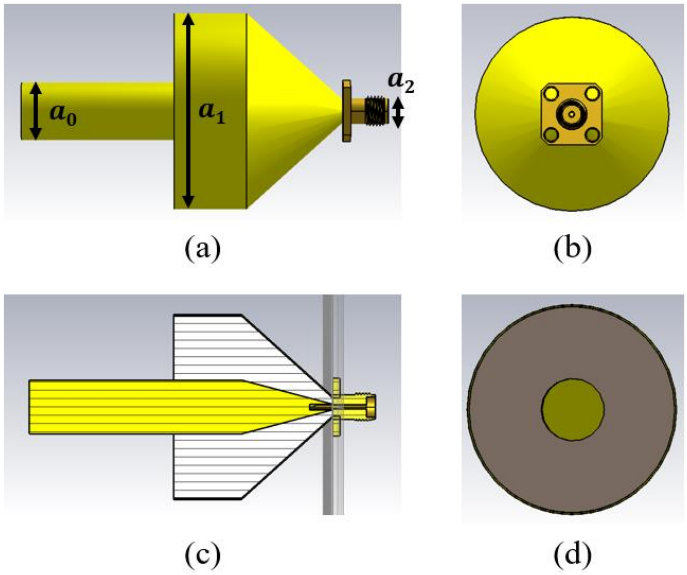


Figure 8.1.3. CAD model of the customized coaxial connector showing the (a) side, (b) back, (c) dissected and (d) front views.

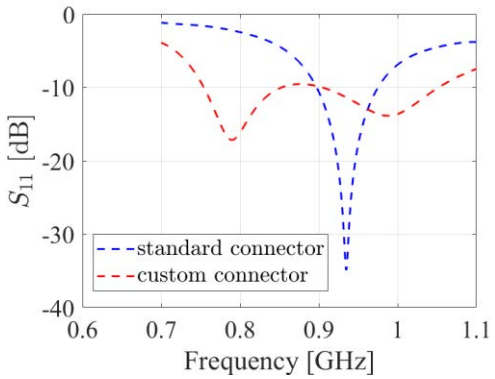


Figure 8.1.4. Simulated VSWR of the HDPE patch antenna with (a) standard SMA connector ($r_p = 0.65$) and (b) customized coaxial connector ($r_p = 6$). The dimensions of the custom connector (as denoted in Fig. 9.1.3) are $a_1 = 12, a_2 = 20, a_3 = 1.3$ (all dimensions are in mm).

8.1.5 *Summary of Significant Findings and Mission Impact*

(A) Developing Array Pattern Tool for large arrays calculations:

A MATLAB code has been developed for faster approximation of the radiation pattern of a linear/planar array of any size and composed of any type of antenna elements. The code requires the center element pattern of a small array (say, 3×3) composed of the same type of antenna elements, desired lattice arrangement, and total number of array elements, as user inputs. This work will be included in future publications.

(B) Investigate the effects of array aperture area reduction on different array parameters:

The effect of different array aperture area and lattice arrangements on the array parameters (such as array gain, beamwidth, electronic beam steerability, etc.) have been reported for arrays modeled on infinite ground planes (DEC 2020 ONR-OSPRES-Grant MSR). The results show that, with 30% reduction in the aperture area ($\approx 50\%$ reduction in # of elements), the gain drops by < 3.5 dBi without any scan blindness spotted as the main beam is steered from boresight to $\pm 60°$ in the $640-990$ MHz range.

The array parameters for large arrays ($\geq 15 \times 15$) on finite ground planes could not be computed using the commercial EM solvers (FEKO and CST) due to excessive memory and time consumption. This work will be resumed after developing a method to estimate array performances on finite ground planes, either through ML or conventional approaches.

(C) Build minimum viable validation prototypes of single ESA elements:

Investigated different bandwidth enhancement techniques applicable to single layer microstrip patch ESAs:

a. Method I: Bandwidth enhancement by strategically placing the coaxial probe along 2/3rd of the patch diagonal – This method is proposed and experimentally validated using prototypes manufactured on TMM-6 and TMM-10i substrates at $2.5-5$ GHz. Antennas have been modeled on various substrates (polyethylene, G10/FR-4, TMM-10i) at the UHF range ($0.6-1$ GHz) and are being considered for manufacturing.
b. Method II: Coaxial probe-fed U-slot loaded rectangular microstrip ESAs – A prototype is manufactured on a G10/FR-4 substrate ($0.9-1.3$ GHz) and tested.
c. Method III: L-probe-fed U-slot-loaded rectangular microstrip ESAs – An antenna has been modeled on a TMM-4 substrate that operates in the $0.52-1.17$ GHz range ($\approx 77\%$ 2:1 VSWR bandwidth). Due to the fabrication complexity of the L-probe proximity coupled feed, this antenna will not be manufactured.

(D) Optimization of ESA (single element) performance using regular and ML based stochastic search algorithms:

Investigated the bandwidth enhancement of the coaxial probe-fed microstrip patch antennas, using regular and ML based stochastic search algorithms (GA, PSO, and Simplex methods), by optimizing the feed-probe location and ground plane shape and size. Compared to regular search algorithms, ML algorithms are found to be less computationally intensive (in terms of time and memory consumption).

(E) Build minimum viable validation prototypes for arrays of ESA elements:

A wideband 3×3 array (2.5–5 GHz) and a narrowband 2×2 array (900 MHz) of coaxial probe-fed microstrip patch ESA elements, on 0.25-inch-thick TMM-10i substrates, have

been manufactured. The S11-parameters of the individual elements, in each array prototype, have been tested, with good agreement achieved between the simulated and the measured data. Modeling and characterization of a 4×4 square array, of wideband ESA elements in the UHF region, has been initiated for future prototyping.

(F) Optimization of array performance using ML algorithms:

(E) Initiated multi-objective optimization of a small 5×5 array by seeking the best array design parameters, including inter-element spacing, ground plane size, feed-probe locations, etc.

8.2 Tradespace Analysis of Ultra-Wide-Band (UWB) Koshelev Antenna

(Alex Dowell and Kalyan Durbhakula)

8.2.1 *Problem Statement, Approach, and Context*

Primary Problem: Determine the extent to which the physical aperture area of an antenna array, composed of antenna elements, can be reduced, while maintaining performance in peak power density, bandwidth, and electronic beam steerability over the UHF range (0.4–1 GHz), compared with present-art high-power-microwave-capable antenna arrays.

Solution Space: The Koshelev antenna has a unique design that is capable of generating an UWB response by effectively merging radiation characteristics from a transverse electromagnetic (TEM) horn antenna with exponentially tapered flares, an electric monopole, and magnetic dipoles over a wide frequency range [1]. This opens up an opportunity to investigate the design parameter space and understand parameter effects on impedance bandwidth, radiation pattern, electric field distribution, and other metrics via a tradespace study.

Sub-Problem:

(i) The integration of an impedance transformer to a single element Koshelev antenna to simulate and test the combined (transformer–antenna) performance is currently not feasible using commercial EM simulators.

(ii)The total surface currents on the Koshelev antenna over the desired frequency range arising from the present positioning of TEM exponential flares, an electric monopole, and magnetic dipoles is not yet clearly understood.

State-of-the-Art (SOTA): The balanced antipodal Vivaldi antenna (BAVA) is considered to be the SOTA antenna element due to its exceptional 20:1 impedance bandwidth ratio as well as the ability to handle tens-of-MW input power.

Deficiency in the SOTA: The BAVA design parameter space has been exhausted over the past couple of decades. The physical aperture area still remains very large and there is no viable path through tradespace study for further physical aperture area reduction.

Solution Proposed: Design, simulate, validate, and perform a tradespace study on the important design parameters of the Koshelev antenna array that effectively reduce its

physical aperture area while maintaining its UWB properties, in both the frequency and time domains. The Koshelev antenna has been shown in the literature to withstand higher voltage levels (over 200 kV peak voltage), thereby making it a viable antenna element for detailed tradespace study and analysis.

Relevance to OSPRES Grant Objective: From the literature, it was shown that the Koshelev antenna can handle high input voltages (and therefore high power with 50 Ω input impedance), which satisfies the specific OSPRES objective related to high input voltage/power. In addition, this work can yield a center-frequency-dependent, bandwidth-controlled, and electronically steerable Koshelev antenna design that can be quickly modified to the spectrum properties of the ultra-fast rise time input pulse.

Risks, Payoffs, Challenges:

(i) The electrical size of the Koshelev antenna is approximately λ/4 at its lowest operating frequency. Further reduction of electrical size to λ/10 could considerably reduce frequency dependent gain, thereby decreasing the power spectral density.

(ii) Payoffs include the development of a library of antenna metrics data for different shapes and sizes of the individual parts within the Koshelev antenna.

(iii) The large electrical size (>5λ) of the Koshelev antenna at its highest operating frequency poses huge computational challenges.

8.2.2 *Tasks and Milestones / Timeline / Status*

(A) Complete literature search to identify and list antenna elements that satisfy UWB properties and HPM requirements, and down-select accordingly / NOV–DEC20 / Complete.

(B) Complete initial design, simulation, and validation of Koshelev antenna [1] / JAN21 / Complete.

(C) Perform a preliminary parameter study to identify design parameters that considerably reduce the physical aperture area / FEB–MAR21 / Complete.

- Milestone: Using FEKO and/or CST electromagnetic (EM) simulators, reduce the physical aperture size of the Koshelev antenna to at least 95% of its original design and show minimal to no variation in the bandwidth, gain and increased aperture efficiency / Complete.

(D) Determine the full-width half-maximum (FWHM) and ringing metrics from the envelope of the time domain impulse response ($h_{rx/tx}(t, \phi, \theta)$) in receive or transmit mode / MAR–APR21 / Complete.

- Milestone: Produce a generalized code that calculates the impulse response envelope of the Koshelev antenna and plots the rate of change in FWHM and ringing values as a function of physical aperture size.

(E) Perform tradespace studies on design parameters such as feed position (*F*), length (*L*), and alpha (α). Obtain various antenna metrics data, compare, and analyze / MAR21/ Complete.

- Milestone: Identify Koshelev antenna design parameters that significantly alter the bandwidth, rE/V, peak gain over the desired bandwidth, and aperture efficiency.

(F) Reduce Koshelev antenna aperture size (H×W) to equal to or less than 90 mm × 90 mm, equal to that of the SOTA BAVA, for direct antenna metrics comparison / MAR–APR21 / Complete.

- Milestone: Provide a recommendation on the optimum design parameters and the resulting metrics, with comparison to SOTA BAVA. The optimized design parameters must yield 900 MHz ± 200 MHz bandwidth, rE/V greater than 1, peak gain around 3 dBi at 900 MHz, aperture efficiency equal to or greater than 130% at 900 MHz.

(G) Using the optimized model from (F), build various array simulation models/topologies to perform a tradespace study and report tradeoffs between array antenna metrics such as center element reflection coefficient (S11) value, gain vs theta at constant phi, physical aperture area, aperture efficiency, and rE/V / MAY–JULY21 / Complete.

- Milestone: Develop/showcase an optimized Koshelev array model that exceeds an aperture efficiency of 130% with a high rE/V.

(H) Perform literature search to investigate, understand, and determine the applicability of special electromagnetic (EM) techniques to the antennas under consideration. / JAN–APR21 / Complete.

(I) Explore impedance taper (microstrip based and coax based) designs that can interface well (both mechanically and electrically) to transition the signal from a coax cable to the input of the Koshelev antenna element / JULY21–AUG21 / Complete.

- Milestone: Recommend the optimum impedance taper design (with minimum reflections and maximum power transfer) with the optimum dimensions to successfully convert the high-voltage, short-rise time input signal from a coax cable to the feed of the Koshelev antenna array.

(J) Study response from optimized Koshelev antenna array when excited with different monopolar, differential, and bipolar pulse signals of significant interest / AUG21–NOV21 / Ongoing.

- Milestone: Provide a table comparing the Koshelev antenna array response metrics and narrow down the suitable pulse signals. Recommend (if any) changes to the downselected pulse signal(s) that can further improve the radiation efficiency, and/or transient gain.

(K) Investigate and analyze the response from the optimized Koshelev antenna array when excited by different excitation patterns /DEC 21/Complete.

- Milestone: Compare and recommend an appropriate excitation method to yield maximum boresight gain, maximum half-power beamwidth (HPWB), minimum side lobe levels, and maximum electric field, rE/V.

(L) Prototype single element Koshelev antenna and test for reflection coefficient, gain as a function of frequency, radiated electric field at 1-m, 2.5-m, 5-m and 10-m (if feasible) distances. / AUG21–MAR21 / Ongoing.

- Milestone: Report measured data and recommend any improvements to the fabrication/prototyping/testing methods.

8.2.3 *Progress Made Since Last Report*

(L) The initial 1mm thick PLA plastic frame of the Koshelev Antenna was 3D printed as a two-part assembly shown above. Copper foil was applied to all surfaces, except for parts of the transformer halves, using adhesive tape. The two halve were then connected to each other using adhesive backed copper foil for the exterior walls and epoxy for the joining the transformer halves. In the upright orientation shown below the antenna lacked the required structural integrity so RF transparent foam was cut and placed in the hallow cavities and in between the two sections. To finish the first iteration of the Koshelev antenna an N-type connector was attached to the transformer with nylon screws and solder. In Fig. 8.2.1(a), the N-type connector can be seen installed in the through type feed configuration, whereas in Fig. 8.2.1(b), the N-type connector was switched to edge feed configuration.

(a) (b)

Figure 8.2.1. (a) The initial iteration of single element Koshelev antenna and (b) Improved impedance transformer feed of single element Koshelev antenna.

8.2.4 *Technical Results*

(L) The initial S11 test of the Koshelev antenna showed that it was not picking up high frequencies that it should be picking up. It was determined that reflections were occurring due to air gaps in the epoxy and in the two transformer halves, since the two halves were not printed with 100% infill. From here the proposed solution was determined to be cutting out the existing the two transformer halves and replacing it with a single 100% infilled transformer. Once the transformer halves were removed the new transformer was epoxied to the existing frame and metalized with copper foil to produce the needed continuously conductive surfaces. To finalize the second iteration of the antenna a N-type

connector was soldered to the transformer horizontally relative to the antenna in an upright position.

(L) On closely observing the measured result in Fig. 8.2.2(a) and Fig. 8.2.2(b), we can notice that at high frequencies (> 2 GHz) the measured result in Fig. 8.2.2(b) has an expected pattern i.e., like that of simulated result. In Fig. 8.2.2(a), the S11 measured result displayed unusual flat response beyond 2 GHz. Therefore, the new S11 measured result is different and observes the pattern of S11 simulated result. However, the S11 amplitude in the case of measured result in Fig. 8.2.2(b) is still higher than that of simulate result, which stayed below -10 dB over the required frequencies. Our next goal is to further improve this design

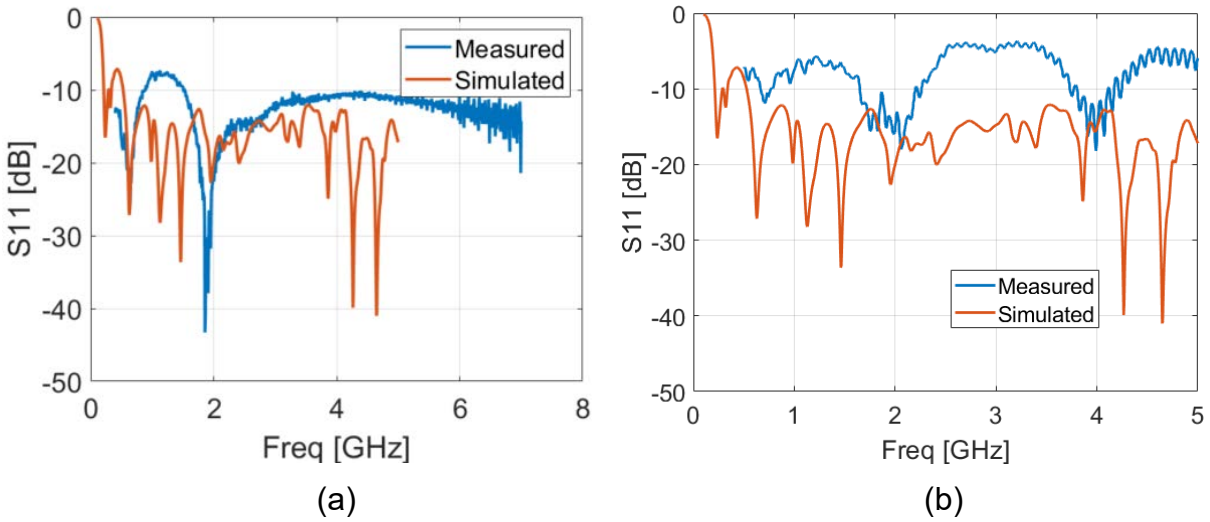


Figure 8.2.2. Simulated vs Measured reflection coefficient for (a) the initial iteration of single element Koshelev antenna, and (b) improved impedance transformer feed of single element Koshelev antenna.

8.2.5 *Summary of Significant Findings and Mission Impact*

(A) An extensive literature search on various UWB antenna elements has resulted in finding three promising options. The down-selected elements are the Koshelev, Shark, and Fractal antennas, which will be extensively studied using their individual design parameter space, which could result in physical aperture area reduction of the single antenna element. Later, the single antenna element will be converted into a planar array.

(B) Initial validation of the Koshelev antenna simulated using CST software agreed well with the antenna metrics published in the open literature [1]. A UWB bandwidth response (10:1 bandwidth) and rE/V > 1 has been observed from our initial simulations of the Koshelev antenna. This validation ensured that the Koshelev antenna can be subjected to further tradespace studies to understand its performance followed by optimizing the design according to OSPRES grant requirements.

(C) The initial tradespace study and analysis of the Koshelev antenna design yielded promising outputs to carry forward the investigation. A comparison of important antenna metrics between the Koshelev antenna in [1] and aperture reduced Koshelev antenna are shown in Table 5.2.1 of the APR 21 MSR.

(D) An in-house code has been developed to calculate important UWB time domain antenna metrics such as full-width half maximum (FWHM) and ringing. These metrics have been calculated using in-house MATLAB code using the excitation voltage and radiated electric field information obtained from CST simulations. FWHM and ringing antenna metrics help with assessing or characterizing an antenna's UWB response.

(E) The tradespace study of feed position provided a deeper understanding of how its position impacts the S11 value bandwidth. An optimum value for feed position i.e., $F = 1/20 < L < 1/10$ is recommended to achieve maximum bandwidth. The tradespace study of the antenna length (L) is straightforward. A longer antenna length will radiate better at lower frequencies. However, physical size restrictions/requirements must be kept in mind in determining the antenna length. Finally, a larger α value (>120°) is recommended to avoid unnecessary reflections from the electric monopole.

(F) From a thorough tradespace study, the aperture size of the Koshelev antenna (single element) is determined to be 90 mm × 100 mm in order to achieve desired antenna metrics performance proposed in the milestone. All metrics described in the milestone have been successfully achieved except the desired bandwidth (200 MHz on both sides) at 900 MHz center frequency. The bandwidth achieved is 900 ± 100 MHz.

(G) The physical aperture area of the Koshelev array antenna largely depends on the interelement spacing and the shape of the array. We were able to determine that the diamond topology is the optimum shape for the Koshelev array antenna. We were also able to obtain similar gain profile (peak gain and pattern) from making certain elements within the array passive (off state) when compared against regular active array (all elements in on state). From the non-symmetric interelement spacing values, we found that S_y has the least effect on the output; therefore a small spacing value can be chosen to reduce the physical aperture area of the Koshelev array.

(H) The literature search on the special EM techniques expanded our knowledge and opened the door to opportunities to apply some of those techniques to the antennas under study. EM techniques such as non-symmetric and non-square array topologies have been applied to the development and study of the Koshelev array antenna.

(I) The first impedance taper design under consideration has shown good S11 values (< -10 dB) over the frequency range of interest. In addition, we have shown that the shape of the pulse can be easily retained at the output of the taper with less than 5% amplitude losses.

(J) The Koshelev antenna array response from feeding a monopolar vs bipolar signal has demonstrated a clear winner: that is, a bipolar signal will radiate at least 10 times better than a monopolar signal. A comparison of the frequency spectrum of the radiated electric field from the optimized Koshelev antenna array between different monopolar pulse sources has identified the 'MI0731' pulse to be the optimum pulse.

(K) The uniform and Gaussian excitation patterns were determined to be the optimum excitation patterns. Selecting these excitation patterns would result in maximum electric field at boresight.

8.2.6 *References*

[1] Gubanov, V. P., et al. "Sources of high-power ultrawideband radiation pulses with a single antenna and a multielement array." *Instruments and Experimental Techniques* 48.3 (2005): 312-320.

8.3 Machine Learning Inspired Tradespace Analysis of UWB Antenna Arrays

(Sai Indharapu and Kalyan Durbhakula)

8.3.1 *Problem Statement, Approach, and Context*

Primary Problem: Determine the extent to which the physical aperture area of an antenna array, composed of antenna elements, can be reduced while maintaining performance in peak power density, bandwidth, and electronic beam steerability over the UHF range (0.4–1 GHz), compared with present-art high-power-microwave-capable antenna arrays.

Solution Space: Fractal antennas possess exceptional fidelity factor values (>0.9), which describe how well the shape of the input pulse is retained at an observation point in the far-field. Their high degree of freedom provides an opportunity to develop systematically modified patch shapes, which in turn leads to improved bandwidth while retaining high fidelity factor values. Machine learning (ML) can be leveraged to predict the antenna array response for an arbitrary design parameter space upon sufficient training and validation.

Sub-Problem:

(i) Fractal antennas generate omni-directional radiation patterns in the H-plane over the desired frequency range.

(ii) ML can suffer from underfitting or overfitting the training model which in turn leads to deviations in the predicted output.

State-of-the-Art (SOTA): Conventional full-wave EM solvers such as method of moments (MoM), multi-level fast multipole method (MLFMM), finite element method (FEM), and finite difference time domain (FDTD) method are currently being used to study, analyze and assess the performance of UWB antennas.

Deficiency in the SOTA: UWB antenna optimization using conventional EM solvers utilizes significant computational time and memory resource.

Solution Proposed:

(i) Design, simulate, validate, and perform a tradespace study on the design parameter space of the selected fractal antenna element using commercially available electromagnetic (EM) wave solvers.

(ii) Train, validate, test and compare multiple ML models for quicker and accurate prediction of antenna array response for different physical aperture areas.

Relevance to OSPRES Grant Objective: The fractal antenna achieves an UWB response, a mandatory requirement of the OSPRES grant objective, in a small volume footprint and similar physical aperture area when compared against the SOTA BAVA, dual ridge horn antennas etc. Furthermore, the microstrip-design-based fractal antenna can efficiently handle electronic steering by integrating the feed network on the same board. This eliminates the need to build a separate feed network external to the fractal antenna using bulky coaxial cables.

Risks, Payoffs, and Challenges:

(i) A majority of the fractal antenna geometries yield an omni-directional pattern in the H-plane, which can be a risk. However, efforts are underway to mitigate this pattern without deteriorating bandwidth.

(ii) Payoffs include developing a library of antenna metrics data for various fractal shapes and sizes.

(iii) Design challenges and numerical calculations with respect to specific fractal shapes could arise after performing a certain number of iterations to further improve the bandwidth.

(iv) Fractal antennas were known to generate gain loss at random frequencies over their operating frequencies. Achieving gain stability over the desired frequency range can be a significant challenge.

8.3.2 *Tasks and Milestones / Timeline / Status*

(A) Perform tradespace analysis of the fractal element radius *b* over the desired frequency range (4 to 12 GHz) using the genetic algorithm (GA) optimization tool available in the commercial electromagnetic (EM) solver FEKO / FEB21 / Complete.

- Milestone: Provide a recommendation of an optimum value of *b* using OPTFEKO to minimize reflection coefficient or S11 (< –10 dB).

(B) Perform tradespace study on different fractal shapes by changing the number of fractal segments to understand the effect of this change on the impedance bandwidth / FEB21 / Complete.

- Milestone: Produce a detailed study of the antenna response such as S11, gain, and bandwidth by varying the number fractal segments.

(C) Apply the GA optimization tool on the fractal side length *b* over a wide frequency range (2 to 12 GHz with 201 discrete frequency points) and number of fractal segments using OPTFEKO on the LEWIS cluster / MAR21 / Complete.

- Milestone: Reduce physical aperture area by 10% of its present design, reported in the FEB MSR, and demonstrate minimal or no change in S11, gain, and fidelity factor values.

(D) Perform a parametric study and analysis of antenna response by varying hexagon radius, *a* / MAR–APR21 / Complete.

- Milestone: Recommend a value of *a* to reduce the physical aperture area and increase aperture efficiency (>50%) with no variation in other antenna metrics.

(E) Frequency scale fractal antenna design such that the center frequency of the resulting antenna equals 1.3 GHz / MAY21 / Complete.

- Milestone: Modify antenna design with a center frequency equal to 1.3 GHz and achieve similar results (3:1 bandwidth at fc = 1.3 GHz, 3 dBi gain and >130% aperture efficiency at 900 MHz) to antenna design at center frequency ~7 GHz.

(F) Design and simulate various array antenna geometries composed of optimized fractal antenna elements (obtained from (E)) to analyze the effect of overall array antenna geometry on the desired array antenna response metrics (i.e., gain vs. frequency, gain vs. elevation angle at constant phi, rE/V, half-power beamwidth and side-lobe level.) / MAY–JUL21 / Complete

- Milestone: Recommend a best possible structure with reduced aperture area and minimal loss in gain.

(G) Apply ML models available in Altair Hyperstudy (2021) on the fractal antenna to try and understand the possibilities and limitations of ML models for fast and efficient antenna metrics prediction and optimization. Expand the prediction capability to time-domain electric field and antenna pattern using ML models (k-nearest neighbor and linear regression) available in scikit learn on Python programming tool “Anaconda”. / MAY21–FEB22 / Ongoing.

- Milestone: Recommend most accurate and efficient ML model for a fractal antenna in time-domain and frequency domain.

(H) Apply ML models on the octagon fractal antenna array lattice to extend the prediction capability beyond single element. / SEP21–JAN22 / Ongoing.

- Milestone: Recommend the best suitable ML model implemented/developed using Python programming language for array antenna metrics prediction.

8.3.3 *Progress Made Since Last Report*

(G) In the previous MSR, the time-domain electric field prediction from ML models was satisfactory for a Gaussian input pulse. However, the previous ML predictions results included certain time shift for all three input signals (i.e., “DSRD4x2”, “PPM0731”, and “NPG22”). We identified and fixed the time shift error in this MSR. From the initial analysis, it was observed that the training data generated using exported data from CST had non-uniform sampling. To resolve this issue a new approach is proposed to improve the accuracy of ML models.

(G) ML prediction of a single element fractal antenna is extended to gain as a function of theta and plotted as a polar plot. The test data used for validation of trained ML models is outside the training range. Both input training, input test data are shown in the table 8.3.1 and table 8.3.2.

Table 8.3.1 Input for training data

Design Parameter	Combination1	Combination2	Combination3	Combination4	Combination5
a (mm)	38.5	39.5	40.5	41.5	42.5
b (mm)	8	8.5	9	9.5	10
d (mm)	36	36.75	37.5	38.25	39
g (mm)	0.8	1	1.2	1.4	1.6

Table 8.3.2 Input for test data

Design Parameter	Combination1
a (mm)	37.5
b (mm)	7.5
d (mm)	36.25
g (mm)	0.6

(H) To validate and improve the accuracy of ML models prediction, we compared and analyzed the predicted S11 response against the simulated S11 response of all corner and center elements of Octagon antenna array. The S11 response of center and corner elements are separately plotted and compared against the ML prediction. The KNN model available in scikit learn is trained using 5 different antenna array designs and employed for ML prediction. Fig 8.3.1 illustrates the center and corner elements. In Fig 8.3.1, “1” indicates center elements and “2” indicates corner elements.

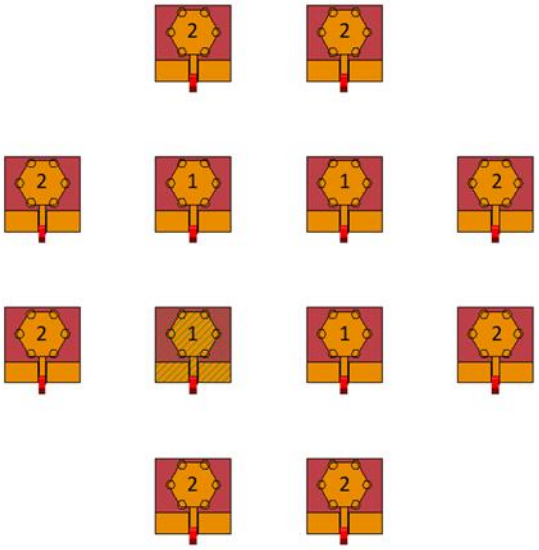


Figure 8.3.1. Center element is indicated '1' and Corner element is indicated '2'.

8.3.4 *Technical Results*

(G) The time shift in previously reported electric field plots is due to the non-uniform sampling, to resolve this the following steps are taken:

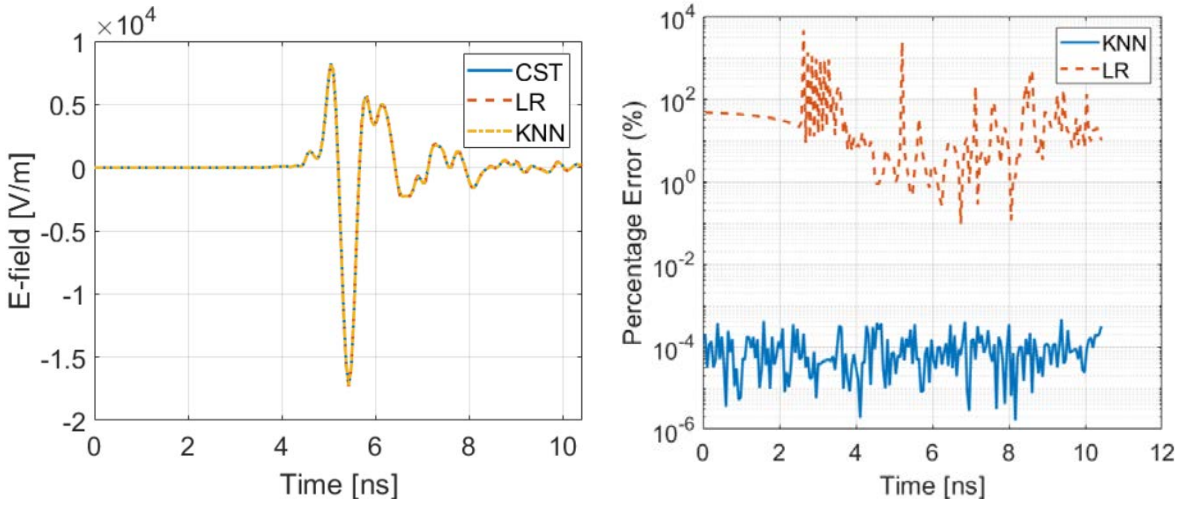
Step 1: Export the non-uniform E-filed data (set of 5) to Matlab.

Step 2: Use the time component of 1st set as reference and interpolate E-filed voltage components of other data.

Step 3: Generated data will have E-filed data at same sampling points (i.e, time intervals).

Step 4: Export the interpolated data to excel sheet for training ML model.

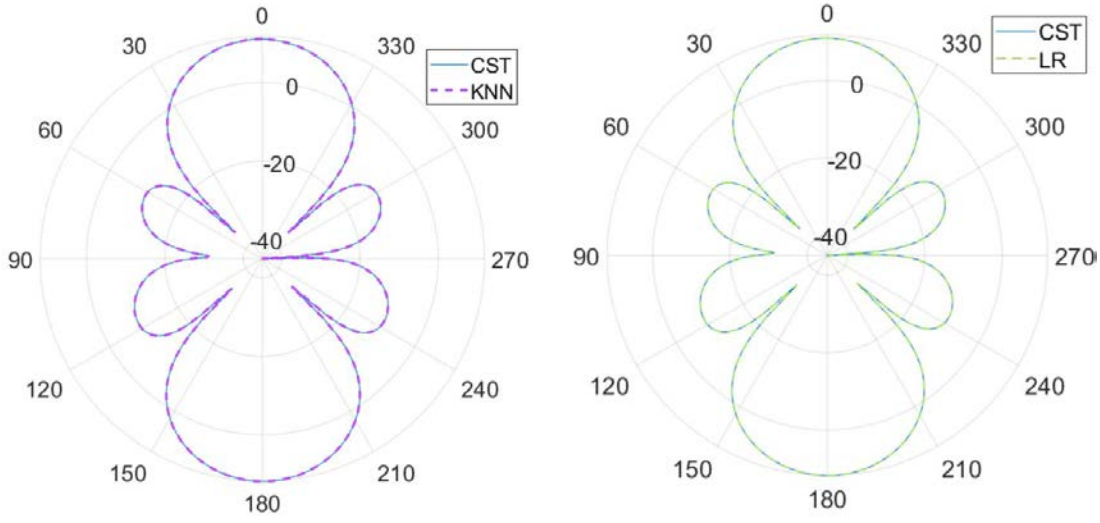
Fig 8.3.2(a) demonstrates the improvement in prediction accuracy. Both KNN and LR overlap with CST indicating better generalization than the previous report. To understand the true accuracy of the trained ML models, we have calculated the percentage error for KNN and LR ML models using CST response as the reference data. Fig 8.3.2(b) shows percentage error for KNN and LR ML models. Despite LR prediction showing good agreement with CST in Fig 8.3.2(a), the percentage error in Fig 8.3.2(b) for LR ML model resulted in high values. On the other hand, the percentage error in Fig 8.3.2(b) for KNN ML model is around 10^{-4}, which indicates a decent prediction.



(a) (b)

Figure 8.3.2. Electric field prediction using kNN and LR ML models at 1 m distance from the aperture of the single-element fractal antenna for DSRD 4x2 input waveform.

(G) We have further extended the ML prediction capability to antenna radiation pattern. In this study, the KNN and LR models were trained with gain data as a function of theta (θ). Five different antenna designs with design parameters as shown in Table 8.3.1 have been simulated to generate training data. Trained ML models are validated using tested data (outside the training data range) as shown in table 8.3.2. The generalization capability of both KNN and LR are satisfactory as they completely overlap with CST response. The results from KNN and LR ML models are compared against the response from CST in Fig 8.3.4(a) and Fig 8.3.4(b), respectively.



(a) (b)

Figure 8.3.4. Gain prediction using (a) kNN and (b) LR ML models compared against CST simulated response.

(H) In an octagonal fractal antenna array there are total 12 antenna elements, out of which 8 are corner elements and the remaining 4 are center elements. In this study, KNN model is trained with S11 response of a particular corner and center elements of 5 different antenna array designs. The predicted output response of ML model is plotted against all corner and center elements separately as shown in Fig 8.3.3. The overall agreement between ML prediction and CST simulated S11 response for corner elements is better than the center element.

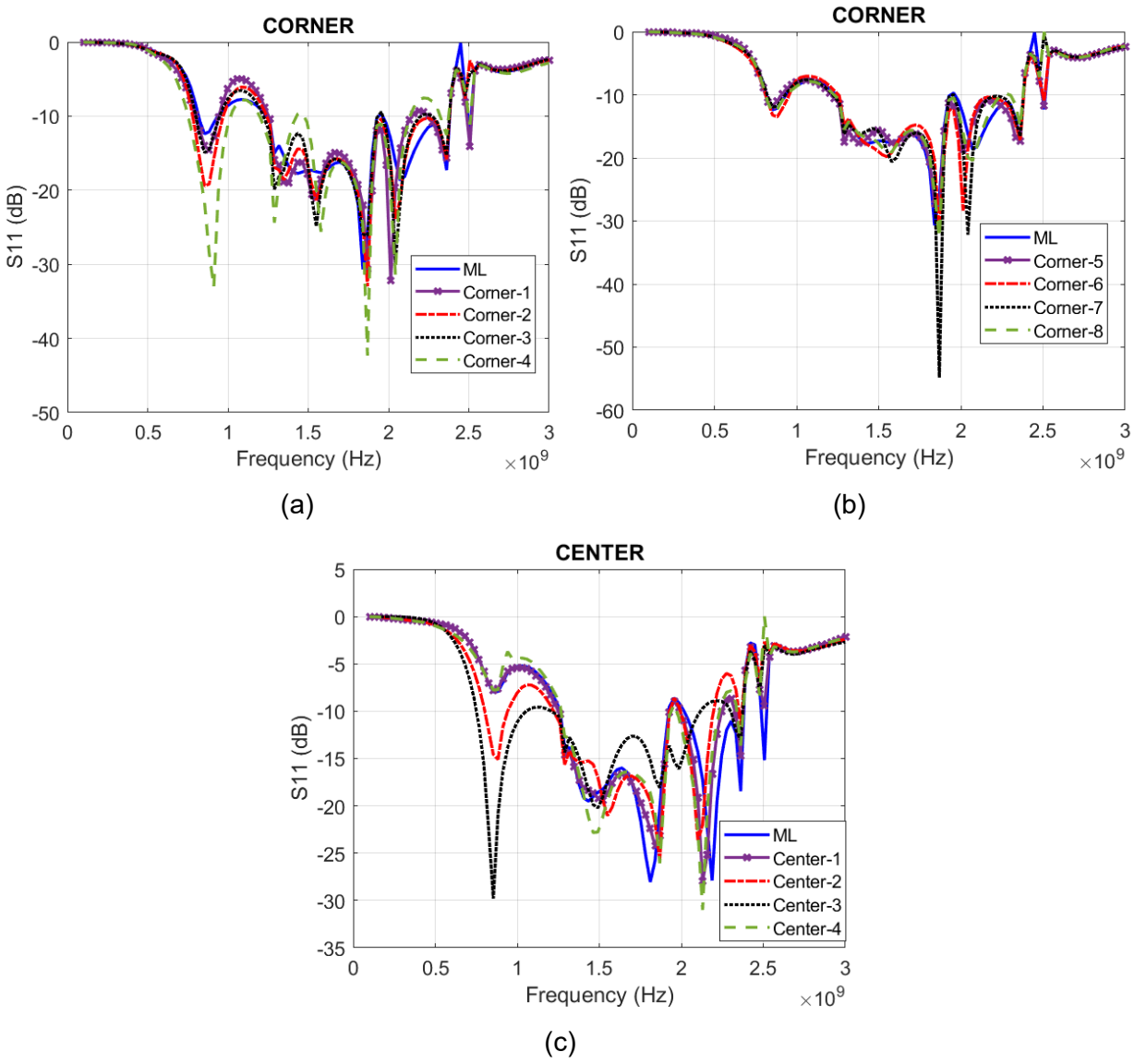


Figure 8.3.3. Comparison of S11 predicted by kNN against FEKO for (a), (b) Corner elements, (c) Center elements.

8.3.5 *Summary of Significant Findings and Mission Impact*

(A) The initial analysis of the simulation results with fractal radius *b* equal to 1.8 mm yielded multiple resonant frequencies with enhanced bandwidth. To further increase the bandwidth, OPTFEKO has been used as an optimization tool with fractal radius *b* as the optimization variable. The optimum value for *b* is found to be 1.66 mm. A comparison between reflection coefficient for initial *b* (= 1.8 mm) value and the optimized *b* (= 1.66 mm) can be found in Figure. 6.4.6. The optimization is carried out over 51 discrete frequency points.

(B) The addition of fractal elements (*N*) to the simple hexagon improved antenna metrics such as S11. To further investigate and understand the fractal elements, the number of segments in the fractal geometry has been varied. The improvement in bandwidth is observed as the value of *N* is increased from 6 to 14.

(C) The initial optimum value of *b* over 51 discrete frequency points is reported as 1.66 mm in task (A). To further increase the accuracy of the optimization algorithm and to find a more precise value for *b*, optimization is further performed over wider frequency points (201 discrete points between 2 GHz to 12 GHz) which yielded the optimum value of b as 1.368 mm. The S11 response of antenna design with newly found *b* (i.e., 1.368 mm) hasn't produced any better bandwidth with respect to *b* (= 1.66 mm). Thus, *b* is set to be 1.66 mm for further research.

(D) The hexagonal patch radius *a* has a significant effect on the physical aperture area of the antenna. Therefore, Altair OPTFEKO has been utilized to find an optimum *a* value, which was found to be 8 mm over the range 7.2 to 9 mm. Antenna metrics such as S11, gain, and bandwidth have shown desired performance with the optimized *a* value.

(E) The initial antenna design has been modified to achieve a center frequency of ~1.3 GHz. The gain value at 900 MHz is 3.5 dBi and, with the modified antenna design, we were able to achieve an impedance bandwidth ratio of 3.3:1. The designed antenna has been fabricated and tested, and the S11 response of the fabricated antenna agrees well when compared against FEKO, CST.

(F) To summarize, four different fractal antenna array geometries (i.e., square, diamond, hexagon, and octagon) have been designed and simulated. Upon comparing antenna array metrics, octagonal fractal antenna array has yielded minimal sidelobe levels with a gain of 15.7 dBi at 900 MHz close to that of square geometry with 32.27% lower physical aperture area than that of square geometry. The octagonal fractal antenna array has been chosen as the optimum geometry with reduced aperture area and reduced side lobes while retaining the bandwidth and gain milestone metrics.

(G) Radial basis function (RBF) and least square regression (LSR) were down selected from the initial three ML models based upon their generalization capability for prediction of reflection coefficient (S11), gain, and electric field. Further analysis of increasing training data set size has shown no improvement in prediction accuracy. Trained ML models were tested for design variable values outside the training range. The resulting RMSE increased as the values drifted away from the mid-point of the training range. RBF performed well in the prediction of S11, while LSR performed

slightly better for gain and electric field predictions. In addition, for time-domain electric field prediction, we recommend using k-nearest neighbors (kNN) ML algorithm for accurate prediction.

(H) Initial application of kNN ML model for the prediction of antenna array bandwidth response of center and corner element yielded positive results with a good agreement between traditional EM solver (FEKO) and trained kNN ML model. The new LR ML model yielded improved RMSE values (over kNN) in its prediction of reflection coefficient and gain for the optimized octagon fractal antenna array.

8.3.6 *References*

[1] H. Fallahi and Z. Atlasbaf, "Study of a Class of UWB CPW-Fed Monopole Antenna With Fractal Elements," in IEEE Antennas and Wireless Propagation Letters, vol. 12, pp. 1484-1487, 2013, doi: 10.1109/LAWP.2013.2289868.

9 Feedback

There is no feedback to report for the current reporting period.

10 Program Management

10.1 Issues

i. Scope – No issues
ii. Budget – 12-month NCTE submitted/pending
iii. Schedule – No issues

10.2 Interactions with Others

Agency/Org	Performer	Project Name	Purpose of Research/ Collaboration

10.3 Major Procurement Actions

10.4 Travel

Destination	Purpose	Attendees	Estimated Costs

10.5 Pending or Upcoming Public Release Requests

11 Appendix A: Academic and IP Output

11.1 Students Graduated

Name	Degree	Currently
Al-Shaikhli, Waleed Azad, Wasekul	MS Spring 19 PhD Summer 21	Kansas City National Security Campus, Honeywell Applied Materials, Sunnyvale, CA
Berg, Jordan	MS Spring 21	MRI Global
Bissen, Bear	MS Spring 19	Kansas City National Security Campus, Honeywell
Floyd, Dennis	BS	Naval Air Warfare Center Weapons Division
Hanif, Abu	PhD Spring 21	UMKC/MIDE (Postdoc)
Harmon, Aaron	BS	Missouri University of Science & Technology
Harp, Joshua	MS	UMKC/MIDE (Senior Engineer)
Hauptman, Cash	BS Spring 18	University of Nebraska-Lincoln
Klappa, Paul	MS Spring 21	
Labrada, Dario	BS Spring 20	Honeywell Aerospace, Florida
Lancaster, John	MS Spring 17	Lawrence Livermore National Laboratory
Renzelman, Jeff	MS Spring 18	Kansas City National Security Campus, Honeywell
Roy, Sourov	PhD Spring21	
Wagner, Adam	MS Fall 20	Kansas City National Security Campus, Honeywell
Xia, Shengxuan	BS	Missouri University of Science & Technology

11.2 Journal Publications

11.2.1 *In Preparation*

[1] N. Gardner, K. C. Durbhakula, and A. N. Caruso, “UHF and L-Band Frequency Generation at MW Peak Power using Diode-based Nonlinear Transmission Lines as Pulse Forming Networks,” *Transactions on Plasma Science*, In Preparation, **2021**.

[2] N. Gardner, K. C. Durbhakula, and A. N. Caruso, “Electrically Tunable Diode-based Nonlinear Transmission Line,” *TBD*, In Preparation, **2021**.

[3] N. Gardner, A. N. Caruso, K. C. Durbhakula and P. Doynov, “Diode-Based Non-Linear Transmission Line Design Considerations,” *Journal of Applied Physics*, In Preparation, **2021**.

[4] B. Barman, D. Chatterjee, and A. N. Caruso, “Tradespace Analysis of Wideband, Electrically Small Microstrip Patch Antenna Elements for Phased Array Applications,” *IEEE Antennas and Propagation Magazine,* In preparation, **2021**.

[5] S. Xia, J. Hunter, A. Harmon, M. Hamdalla, A. Hassan, V. Khilkevich, D. Beetner, “Simulation Driven Statistical Analysis of the Electro-magnetic Coupling to Microstriplines,” *IEEE Transactions on Electromagnetic Compatibility*, In Preparation, **2020**.

[6] M. Hamdalla, V. Khilkevich, D. G. Beetner, A. N. Caruso, A. M. Hassan, “Characteristic Mode Analysis Justification of the Stochastic Electromagnetic Field

Coupling to Randomly Shaped Wires," *IEEE Transactions on Electromagnetic Compatibility*, In Preparation, **2020**.

11.2.2 *Submitted / Under Revision*

[7] B. Barman, K. C. Durbhakula, D. Chatterjee, and A. N. Caruso, "Comparison of Machine Learning Algorithms for Bandwidth Enhancement of a Coaxial Probe-fed Microstrip Patch Antenna," *Applied Computational Electromagnetics Society (ACES)*, Submitted, **2021**.

[8] B. K. Lau, M. Capek, and A. M. Hassan, "Characteristic Modes–Progress, Overview, and Future Perspectives," *IEEE Antennas and Propagation Magazine*, Submitted, **2021**.

[9] K. Alsultan, M. Z. M. Hamdalla, S. Dey, P. Rao, and A. M. Hassan, "Scalable and Fast Characteristic Mode Analysis Implementation Using a Hybrid CPU/GPU Platform," *ACES*, Submitted, **2021**.

[10] M. Z. M. Hamdalla, B. Bissen, J. Hunter, L. Yuanzhuo, V. Khilkevich, D. G. Beetner, A. N. Caruso, and A. M. Hassan, "Prediction of Experimental Electromagnetic Coupling to a UAV Model Using Characteristic Mode Analysis," *IEEE Access*, Submitted, **2021**.

[11] W. Azad, F. Khan, and A. N. Caruso, "A Scalable Multilevel-Modular 10 kV Silicon Carbide MOSFET Module Featuring Custom Isolated Gate Driver Circuit Combined with Coupling and Snubber Circuits," *IEEE Transactions on Power Electronics*, Submitted, **2021.**

[12] John Keerthi Paul Bhamidipati, Eliot R. Myers, Adam M. Conway, Lars F. Voss, and Anthony N. Caruso, "Figure of Merit Development for Linear-Mode Photoconductive Solid-State Switches," *IEEE Transactions on Electronic Devices*, Under Revision, **2020**.

11.2.3 *Published / In Press*

[13] M. Z. M. Hamdalla, B. Bissen, J. Hunter, Y. Liu, V. Khilkevich, D. G. Beetner, A. N. Caruso, and A. M. Hassan, "Prediction of Experimental Electromagnetic Coupling to a UAV Model Using Characteristic Mode Analysis," *IEEE Access*, In Press, **2021**.

[14] J. N. Berg, R. C. Allen, and S. Sobhansarbandi. "A Novel Method of Cooling a Semiconductor Device through a Jet Impingement Thermal Management System: CFD Modeling and Experimental Evaluation." *International Journal of Thermal Sciences*, 172, 107254, **Feb 2022** [doi].

[15] W. Azad, F. Khan, and A. N. Caruso, "A Medium Power, Self-Sustaining, Configurable RF Pulse Generation Circuit Using a Nonlinear Transmission Line and Power Amplifier in a Closed Loop Configuration, *IEEE Transactions on Plasma Science*, vol. 49, no. 7, pp. 2183–2194, **July 2021** [doi].

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Power Delivery," *IEEE Transactions on Power Electronics*, vol. 36, no. 11, pp. 12721–12745, **Nov 2021** [doi].

[17] K. C. Durbhakula, D. Chatterjee, and A. M. Hassan, "An Efficient Algorithm for Locating TE and TM Poles for a Class of Multiscale Inhomogeneous Media Problems," *IEEE Journal on Multiscale and Multiphysics Computational Techniques*, vol. 4, no. 1, pp. 364–373, **2019** [doi].

11.3 Conference Publications

11.3.1 *Submitted / Accepted*

[1] S. R. Shepard and H. A. Thompson, "Self-focusing in Guided and Un-guided Media," submitted to the *2021 OSA Nonlinear Optics Topical Meeting, Virtual Event*, August 9-13, 2021.

11.3.2 *Presented*

[2] B. Barman, D. Chatterjee and A. N. Caruso, "Probe-location Optimization in a Wideband Microstrip Patch Antenna using Genetic Algorithm, Particle Swarm and Nelder-Mead Optimization Methods," *2021 International Applied Computational Electromagnetics Society Symposium (ACES)*, 2021, pp. 1-3 [doi].

[3] W. Azad, S. Roy, and F. Khan, "A Single Gate Driver-based Four-stage High-voltage SiC Switch Having Dynamic Voltage Balancing Capability," *2021 IEEE Applied Power Electronics Conference and Exposition* (APEC), Phoenix, AZ, USA, June 9-12, 2021.

[4] W. Azad, S. Roy, F. Khan and A. N. Caruso, "A Multilevel-Modular 10 kV Silicon Carbide MOSFET Module using Custom High-Voltage Isolated Gate Driver, Coupling, and Snubber Circuits," *2021 IEEE Kansas Power and Energy Conference* (KPEC), Manhattan, KS, USA, April 19-20, 2021 [doi].

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11.4 Conference Presentations

11.4.1 *Submitted / Accepted*

[1] S. Bellinger, A. Caruso, A. Usenko, "Stacked Diodes for Pulsed Power Applications," GOMACTech-22, Miami, FL, March 21–24 2022 (submitted, oral).

[2] S. Bellinger, A. Caruso, A. Usenko, "New Paradigm on Making Semiconductor Opening Switches for Pulsed Power," 2021 23rd IEEE Pulsed Power Conference, Denver, CO, Dec. 12–16, 2021 (accepted, oral).

Directed Energy Professional Society, Directed Energy Systems Symposium, Washington DC, October 25-29 2021 (submitted):

[3] B. Barman, D. Chatterjee, A. Caruso, and K. Durbhakula, "Tradespace Analysis of a Phased Array of Microstrip Patch Electrically Small Antennas (ESAs)" (Poster)

[4] J. N. Berg, R. C. Allen, and S. Sobhansarbandi, "A Novel Method of Cooling a Semiconductor Device through a Jet Impingement Thermal Management System: CFD Modeling and Experimental Evaluation" (Poster)

[5] J. N. Berg, R. C. Allen, and S. Sobhansarbandi, “Heat Transfer Enhancement of a Jet Impingement Thermal Management System: A Comparison of Various Nanofluid Mixtures” (Poster)

[6] J. Bhamidipati, M. Paquette, R. Allen, and A. Caruso, “Photoconductive Semiconductor Switch Enabled Multi-Stage Optical Source Driver” (Poster)

[7] G. Bhattarai, J. Eifler, S. Roy, M. Hyde, J. Bhamidipati, A. Usenko, M. Pederson, M. Paquette, A. Caruso, S. Bellinger, L. Voss, and R. Allen, “All Solid-State High-Power Pulse Sharpeners” (Poster)

[8] S. Brasel, K. Norris, R. Allen, A. Caruso, and K. Durbhakula, “Efforts to Reduce Physical Aperture Area of Ultra-Wideband Arrays” (Poster)

[9] A Caruso, “ONR Short Pulse Research and Evaluation for c-sUAV: Supporting and Sub-Programs Overview” (Oral)

[10] J. Clark, R. C. Allen, and S. Sobhansarbandi, “Ultra-Compact Integrated Cooling System Development” (Poster)

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[12] N. Gardner, M. Paquette, and A. Caruso, “Diode-Based Nonlinear Transmission Lines Capable of GHz Frequency Generation at Single MW Peak Powers” (Poster)

[13] M. Hamdalla, A. Caruso, and A. Hassan, “The Shielding Effectiveness of UAV Frames to External RF Interference” (Poster)

[14] M. Hamdalla, A. Caruso, and A. Hassan, “A Predictive-Package for Electromagnetic Coupling to Nonlinear-Electronics using Equivalent-Circuits and Characteristic-Modes (PECNEC)” (Poster)

[15] M. Hyde, J. Eifler, S. Roy, G. Bhattarai, A. Usenko, M. Paquette, A. Caruso, S. Bellinger, L. Voss, and R. Allen, “Development of an Evaluation Network for Drift Step Recovered Diodes through and Augmented Design of Experiment” (Poster)

[16] S. Indharapu, A. Caruso, and K. Durbhakula, “Machine Learning Based Ultra-Wideband Antenna Array Optimization and Prediction” (Poster)

[17] F. Khan, W. Azad, and A. Caruso, “A Scalable Multilevel-Modular 10 kV Silicon Carbide MOSFET Architecture for Pulsed Power Applications” (Poser)

[18] D. F. Noor, J. Eifler, M. Hyde, G. Bhattarai, S. Roy, J. Bhamidipati, A. Usenko, M. Pederson, M. Paquette, A. Caruso, S. Bellinger, L. Voss, and R. Allen, “DSRD-IES Pulsed-Power Generator Topology Study Using Machine-Learning-Based Feature Selection Optimization and Predictive Learning” (Poster)

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[20] S. Shepard and A. Caruso, “Tubular Core Optical Power Amplifier” (Poster)

[21] H. Thompson, M. Paquette, and A. Caruso, “Minimizing On-State Resistance in GaN:X Photoconductive Semiconductor Switches (PCSSs) for Direct Modulation (Poster)

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[26] William Spaeth, Wideband Parallel Plate to Coaxial Cable Taper

[27] Stefan Wagner, Quickly Determining Minimum HPC Source Requirements Using Binary Search

***

GOMAC 2019

[28] Cash Hauptmann, Reduced Recovery Time in SiPCSS Photoconductive Switches

[29] Eliot Myers, Picosecond High Power Switching Technologies

[30] Heather Thompson, GaN Optimization for Use in Photoconductive Switch

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[28] B. Barman, D. Chatterjee, and A. N. Caruso, “Analytical Models for L-Probe fed Microstrip Antennas,” *Proceedings of the IEEE Antennas and Propagation International Symposium and National Radio Science Meeting*, Atlanta, Georgia, USA, July 7-12, 2019 (1 page URSI Abstract).

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[29] Ryan Butler, Mechanical Challenges of Modular Photoconductive Semiconductor Based HPM Sources

[30] Steve Young, Two-Dimensional Optoelectronic Pulsed Power Switches: Initial Effort

[31] Adam Wagner, Rapid Cost Effective RF Component Prototyping Using 3D Printers

[32] Heather Thompson, Cost to benefit analysis of GaN for Photoconductive Semiconductor Switches

[33] Colby Landwehr, Low Leakage Electroluminescence For Improving SiPCSS Hold Off

[34] James Kovarik, Some Investigations Into Applications Of Electrically Small Antennas As Phased Array Elements

[35] Spencer Fry, Maximizing SiPCSS Efficiency For HPM Sources

[36] Deb Chatterjee, Studies On Antenna Characterization And Propagation Of High Power Pulsed Electromagnetic Waves With Minimal Dispersion

***

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[37] Jeff Scully, ElectroLuminescence Studies of Silicon Based Photo-Switches

[38] Cash Hauptmann, Thermal Anlaysis of a PCSS through TCAD Simulation

[39] Nicholas Flippin, Fast Rise Time Switches: Drift Step Recovery Diode

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DEPS Posters and Presentations 2017

[40] Noah Kramer, Recent Results of Silicon Based Photoconductive Solid State Switches for 500kHz Continuous Pulse Repetition Frequency

11.5 Theses and Dissertations

[1] Jordan N. Berg, “Development of a Jet Impingement Thermal Management System for a Semiconductor Device with the Implementation of Dielectric Nanofluids,” MS Thesis in Mechanical Engineering, University of Missouri-Kansas City, **2021** [mospace].

[2] James C. Kovarik, “Wideband High-Power Transmission Line Pulse Transformers,” MS Thesis in Electrical Engineering, **2021** [mospace].

[3] Wasekul Azad, “Development of Pulsed Power Sources Using Self-Sustaining Nonlinear Transmission Lines and High-Voltage Solid-State Switches,” PhD Dissertation in Electrical Engineering, **2021** [mospace].

[4] Paul Klappa, “Implementation and Assessment of State Estimation Algorithms in Simulation and Real-World Applications,” MS Thesis in Mechanical Engineering, **2021** [mospace].

11.6 IP Disclosures Filed

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[2] S. Bellinger, A. Caruso, A. Usenko, “Diode and Method of Making the Same,” 28JUNE2021.

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[4] Shepard, “A Low Noise Optical Amplifier,” 21UMK007, 14SEPT2020.

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11.8 Non-Provisional Patents Filed

None to date

12 Appendix B: WBG PCSS-Enabled Laser Diode Array Driver

(John Bhamidipati)

12.1 Executive Summary

A multi-stage wide bandgap (WBG) photoconductive semiconductor switch (PCSS) enabled laser diode array (LDA) driver was proposed in an effort to overcome the size, weight, and cost drawbacks of conventional laser systems used in high power microwave (HPM) systems. This involves an LDA enabled by an avalanche PCSS driven by a low power laser diode, which in turn drives the source driver for HPM generation, as shown in Figure 12.1. The primary goal of this effort is to retrofit a PCSS exhibiting persistent photoconductivity to function as a seed laser diode driven lock-on/avalanche switch [1] [2] to drive a high-power laser diode array (LDA) at ns–sub-µs transients.

An initial feasibility study was performed to determine the output pulse requirements of the enabling switch (PCSS) based on Jenoptik's actively cooled quasi continuous wave (QCW) vertical laser diode stack, which indicated the need for mΩ order on-state resistance, sub-ns risetimes and ~120 A output current. These pulse characteristics require lock-on conduction in the PCSS at <50 V bias, requiring a gain factor of ~$10^{2.6}$ when illuminated with ~1 µJ/pulse optical energy, raising a need for PCSSs made from direct bandgap materials like GaN and GaAs.

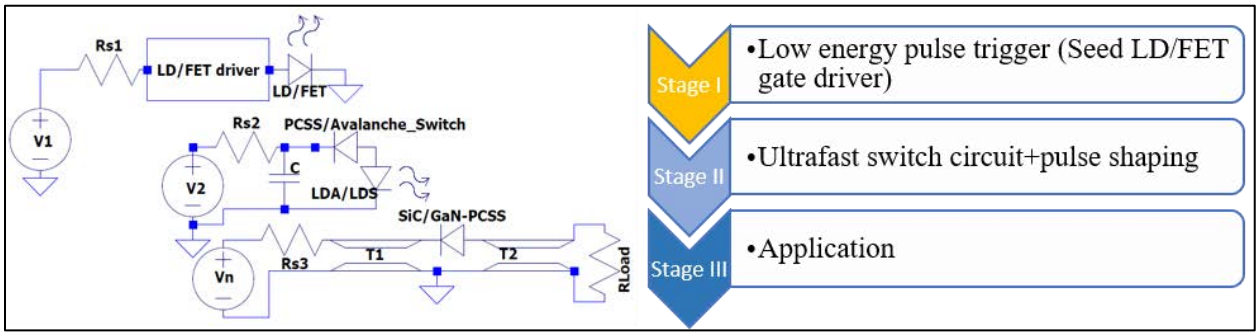

Figure 12.1. (a) Schematic of the proposed work and (b) flow diagram showing three implementation stages: (i) optical/electrical trigger, (ii) current gain and (iii) application.

Despite the published literature on GaN-PCSS lock-on conduction by Hirsch et al. [1] at Sandia National Lab (SNL), our in-house attempts to replicate the lock-on conduction using NRL fabricated lateral carbon doped GaN-PCSS were unsuccessful. The carbon doped PCSSs tested in-house may be structurally different compared with SNL-made GaN-PCSSs, leading to the discrepancy in results. To understand the material characteristics potentially contributing to lock-on conduction, carbon-doped GaN properties need to be studied computationally. [3] [4] Due to the unavailability of custom-made GaN-PCSSs, alternate PCSS technologies such as custom-made Si-PCSSs and Si optodiodes by voltage multipliers inc. (VMI), and electrically triggered switches like GaNFETs and avalanche transistors (ATs) with the capability to demonstrate avalanche conduction, have been evaluated to experimentally demonstrate the pulse characteristics

indicated by the feasibility study. Though the VMI optodiodes demonstrated ~400 ps rise times when illuminated with pulse energies between 20 µJ and 150 µJ/pulse, the on-state resistance was found to be on the order of 2.3–6.1 Ω, which is three orders of magnitude higher than the target metric. The Si-PCSS, along the same lines, failed to demonstrate the required on-state resistance when illuminated with pulse energies <100 µJ, rendering them inadequate for replacing GaN-PCSSs. The electrically triggered avalanche transistors rated for 60 A peak currents with 80 V hold-off are highly susceptible to device failure due to thermal runaway owing to their packaging and <150°C safe operating temperature. Furthermore, the requirement of 120 A by the LDA requires paralleling the ATs with capacitive coupling, increasing the chances of device failure.

To better understand the lock-on conduction in GaN-PCSS, a comprehensive study needs to be done to understand the effects of carbon/iron doping levels and distribution, crystal defect types, their energy levels, and concentration/densities on transient photocarrier generation, mobility, scattering, and recombination, requiring a dedicated personnel and computational resources with a slim chance of success. Due to the unavailability of GaN-PCSSs and lack of promising results in finding an alternative switch technology, keeping the program's immediate needs in mind, the LDA driver effort will not be pursued any further. However, a subset of this section constituting a solid-state switch enabled compact multifrequency generator referred to as a frozen wave generator will be pursued further and will be reported as a stand-alone section beginning FEB2022.

12.2 Objective

Demonstrate a modular multi-stage laser diode array (LDA) driver enabled by a seed-laser-diode-driven avalanche WBG-PCSS that is compact (~1.1 cu-ft), lightweight (~10–12 lbs.) and inexpensive (< $15,000) to be implemented as a potential alternative for the conventional optical trigger (laser) subsystem that enables PCSS-driven HPM-based defense systems and helps overcome the SOTA SWaP-C^2 limitations imposed by the laser's driver and auxiliary subsystems like amplifiers, optics and thermal management system (TMS).

12.3 Technical Background

High power microwave (HPM) generation primarily refers to the production of high peak power bursts of coherent narrow-to-ultrawideband electromagnetic waves spanning the frequency range of approximately 30 MHz to 100 GHz. [5][6] The technology used to generate such radiation is often based on pulsed power, [7] although more traditional modulator-based drivers are used as well, particularly at the higher frequencies where continuous wave (CW) operation can be supported for time scales of tens-of-minutes. The term high average-power microwaves implies a long pulse duration, high-repetition rate or continuous beam (referred to as "CW") sources, exemplified by vacuum tube based devices such as klystrons and magnetrons whereas high-peak power microwaves implies a short pulse duration, a low-repetition rate, or 'single shot' sources, exemplified by devices such as the magnetically insulated line oscillator (MILO), capable of pulse widths under 200 ns. [6][7]

Despite successful implementation of vacuum-tube-based sources in HPM generation, the application trade-space was limited due to the complexity in the construction of source drivers, their ~μs jitter, narrow bandwidth, and high failure rates. [8] Advancements in science and technology have enabled unceasing expansion in pulsed-power application trade space with applications like ground penetration radar, wide band communications, high energy linear colliders, power beaming, counter electronics,[8] and other significant civilian and military applications with a need for ultra-wide bandwidth and miniaturization alongside waveform tunability and enhanced reliability. [9] These requirements have rendered the conventional source drivers antiquated, prompting the need to seek alternatives in unconventional sources, including solid-state device technologies like electrically stimulated silicon-based drift step recovery diodes (DSRDs), switching diodes and avalanche transistors, and optically stimulated photoconductive semiconductor switch (PCSS) technologies made of Si and GaAs. [9][1] PCSSs are capable of providing electrical isolation and exhibiting sub-ns turn-on characteristics following the pulse characteristics of the incident optical pulse trigger, enabling operation at high pulse repetition rates (PRRs).

Thus far, implementation of linear and lock-on mode PCSS in pulsed power systems has been successfully demonstrated at multiple kilovolts through relatively mature narrow bandgap (NBG) semiconductors like Si and GaAs. [9][10] Wide bandgap (WBG) semiconductors like 4H-SiC and 3C-GaN, despite being relatively immature in terms of fabrication techniques, have demonstrated linear photoconductivity at ones-of-kilovolts. [9][11]

However, acute optical pulse energy requirements for linear mode PCSS actuation[12][13] have brought forth a need for high average power femtosecond–picosecond lasers with an additional need for ancillary driver control and cooling systems. Despite meeting the system needs, these high average power laser systems return a degraded SWaP-C[2] (size, weight, power, cost and cooling) index due to their cost and volume constraints with a majority of it being contributed by its driver and control subsystem. This limits the application trade space to systems with abundance in financial capital, real-estate, and payload capacity. Industrial state-of-the-art (SOTA) master oscillator power amplifier (MOPA) based 1064 nm picosecond lasers for PCSS-driven HPM-based defense systems are bulky (>5000 cm^3/W), heavy (~125 lbs.) and expensive (~$120,000) with an additional need for second and third harmonic generation optics to trigger WBG solids (GaN/SiC). For reference, a laser in this class would occupy a volume of ~10 cu-ft (2.83×10^5 cm^3) and provide an average power of 50 W, thus resulting in 5.67×10^3 cm^3/W.

12.4 Tasks, Milestones, and Status

(A) Perform initial feasibility study for the cascaded multi-stage optical amplifier design and determine functional requirements for the laser diodes (arrays) and source driver [DEC–JAN 2020 / completed].

  a) Determine the functional requirements of the enabling switch based on Jenoptik 1080 W QCW laser diode stack [JAN 2020 / completed]

(B) Complete initial stage experimental implementation of the PCSS-based driver and demonstrate positive current gain using GaN-PCSS, triggered with a 404 nm laser diode. [DEC 2021–JAN 2022 / incomplete].

   a) Demonstrate lock-on conduction at <50V bias in GaN-PCSS with switch gaps 50 –100 μm. [DEC 2022 / incomplete]

   b) Evaluate switch response when excited with 355 nm, 375 nm, and 404 nm laser diodes to understand the device performance when excited intrinsically and extrinsically. [JAN 2022 / incomplete]

(C) In addition to (B), investigate potential alternatives to GaN-PCSS in both PCSS and non-PCSS domains. [NOV–DEC 2021 / completed].

   a) Evaluate Si-PCSS, and Si optodiodes from voltage multipliers inc., to verify the lock-on conduction at <200 volts with <50μJ/pulse optical illumination.

   b) Evaluate avalanche transistors rated for 80 V to verify the peak output current and reliability when used at >100 kHz PRR.

(D) Define performance metrics for PCSS-based driver and complete numerical calculations for required output current at each stage and corresponding PCSS (GaN/GaAs) operating voltages in light of electric fields required for lock-on/avalanche mode, establish real-time implementation timeline, cost estimates, jitter limitation, and explore ways to protect LDA from PCSS ringing. [MAR 2021 / partially complete / revisit after completing (B)].

(E) Proof of concept testing of the two-stage PCSS-enabled driver system with a 50 Ω load at 1 kHz pulse repetition rate (PRR) [NOV–DEC 2021 / incomplete].

(F) Working prototype demonstration at ~MHz PRR with laser diode array/stack and ancillary optics based on HPM source driver needs including thermal management system (TMS). [JAN–FEB 2022 / suspended].

12.5 Methods and Approach

Initial efforts started as a survey of the existing laser technologies and laser drivers to establish the SOTA limitations in the current market. Based on the market research, a need for a compact optical source was established. The first priority of this effort was to demonstrate a low cost, compact and lightweight driver for the lasers and/or laser diode arrays.

To accomplish this, a multi-stage approach has been proposed, where the first stage includes a low power laser diode driven by a compact driver, exciting a PCSS in the second stage in lock-on/avalanche mode, as shown in Figure 12.1. The need for avalanche mode has been determined in the initial feasibility study. The avalanched PCSS enables an laser diode array (LDA), which in turn excites the source driver in the HPM generation system. The wavelength of LDA is determined based on the source driver material.

Two distinct approaches have been implemented for this work: (i) retrofit a PCSS exhibiting persistent photoconductivity [10] to function as a seed laser diode (SLD) driven

lock-on/avalanche switch [9] to drive a high-power laser diode array (LDA) at sub-μs–ns transients, and (ii) investigate the possibility of driving the LDA using electrically triggered switches like GaNFETs and avalanche transistors (ATs) with minimal jitter instead of PCSS to obtain similar results experimentally. [11]

The testing of GaN-PCSS to demonstrate lock-on conduction was performed in-house to replicate the published work of SNL using a capacitive circuit as shown in Figure 12.2

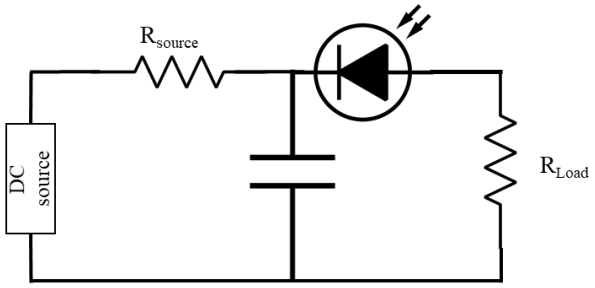

Figure 12.2. Operational circuit for GaN-PCSS testing

On the other hand, the experimental evaluation of alternative PCSS technologies like custom-made Si-PCSS and VMI Si-optodiodes has been performed on 4.4 Ω stripline with 2.5 ns charge and 5 ns discharge lengths, triggered with 70 ps FWHM optical pulse with energies between 20 and 200 μJ. The expectation is to potentially demonstrate avalanche switching with optical energies <20 μJ at <50 V bias.

The evaluation of electrically triggering switch technologies like avalanche transistors has been performed to replicate Marx generator operation to demonstrate high current outputs with multiple kHz repetition rates.

12.6 Results and Discussion

The state-of-the-art COTS laser driver specifications and limitations have been comprehensively studied, and working backwards from the LDA requirements, the target performance metrics of the enabling switch have been determined in terms of output current (>120-A), pulse repetition rate (>1-MHz), transient response (<200-ps risetime and <1-ns pulse width), and volume (<0.75 cu-ft). A preliminary feasibility study has signified the need for lock-on conduction mode with ~$10^{2.6}$ gain factor to drive at >1-MHz pulse repetition rate while limiting the amplification stages to 2. Inducing lock-on operation at low electric fields (~3–3.5 kV/cm) potentially reduces the risk of high jitter at ~MHz order pulse repetition rates (PRR) and negative currents due to ringing during recovery, which could otherwise damage the optical source (LDA). 72 mΩ on-state resistance (calculated) while operating PCSS in lock-on mode at low voltages (50-μm device at ~17.5 V bias) reduces the power dissipation (0.08 μJ/pulse), resulting in reduced cooling system requirements, retaining the expected SWaP-C^2 factor. This approach can potentially reduce the monetary costs to 10–12% of the conventional laser system, while achieving the expected goal of miniaturizing the optical subsystem by 90%.

To demonstrate the lock-on conduction mode in carbon-doped GaN-PCSS by replicating the published literature, [1] testing was performed in-house. Per the literature, the GaN-

PCSS is expected to switch in lock-on mode at electric fields ~3–3.5kV/cm. However, our in-house experimental results have shown a strictly linear response of GaN-PCSS up to 18 kV/cm electric fields when triggered using 355 nm and 404 nm wavelengths. The attempts to demonstrate lock-on mode have been unsuccessful with the devices on-hand.

To find an alternative to the GaN-PCSS, we evaluated PCSS technologies like custom-made Si-PCSSs and commercial-of-the-shelf Si optodiodes (SKU: OZ150SG) rated for 15-kV procured from Voltage Multipliers Inc. The testing has been performed on a 4.4-Ω microstrip to verify the device ability to demonstrate <200-ps t_{rise} and <75-mΩ R_{on} while pushing >100-A current when excited with a 70-ps FWHM laser pulse. An optical energy sweep test was performed, keeping the charge voltage and laser spaciotemporal profile the same. The results from the test are reported below in Table 12.1.

Table 12.1. Results from Si optodiode pulse testing performed at 200-V charge voltage with a 70-ps FWHM optical pulse illumination and varied optical pulse energies.

Pulse energy (μJ)	Charge/bias voltage (V)	Output voltage (V)	Rise time (ps)	Fall time (ns)	On-state resistance (Ω)
200	200	96	428	4.845	0.143
103	200	66	368.56	4.652	2.266
47	200	55	360.65	4.3	3.6
21	200	42	329.46	3.9	6.076

The best result in terms of on-state resistance (0.143-Ω) was observed at 200-μJ illumination while t_{rise} (329.4-ps) was observed when illuminated with 21-μJ optical energy. Nonetheless, the obtained results failed to satisfy the metrics (R_{on} = 0.072-Ω and t_{rise} < 200-ps) determined by the feasibility study, rendering the Si-PCSS and VMI optodiodes infeasible for implementation as an alternative to GaN-PCSS.

Alongside the photo switches, electrically triggered switches like avalanche transistors have been evaluated against the established performance metrics to work in Marx-generator-style avalanche circuit. Though the transistors are rated for 60 A peak currents with 80 V hold-off, the ATs are highly susceptible to device failure due to thermal runaway owing to their packaging and <150°C safe operating temperature and cannot be used even at a few kHz PRR. Furthermore, the requirement of 120 A by the LDA requires paralleling the ATs with capacitive coupling, increasing the chances of device failure.

12.7 Summary and Recommendations

PCSS and non-PCSS switch technologies capable of avalanche conduction have been evaluated against the pulse requirements for a LDA enabling switch. While GaN-PCSS with a direct bandgap has a potential to demonstrate lock-on/avalanche conduction, the

limited device availability and fabrication customization has restricted the extent of evaluation. A comprehensive computational study to understand the compensation effects of sub-bandgap states on the photoresponsivity of carbon-doped GaN is recommended to understand mid-gap optical excitation that would potentially contribute to lock-on conduction. Though avalanche transistors failed to meet the design requirements, there are potential candidates in electrically triggered switch technologies like drift step recovery diodes (DSRDs) and silicon avalanche shapers capable of meeting the pulse requirements. However, these bring forth a trade of in terms of jitter (>50 ns) and implementing these devices requires additional effort to compensate it.

12.8 Outputs

IP disclosures

J. Bhamidipati, E. R. Myers, and A. N. Caruso “Multi-Stage Photo-Stimulated WBG-PCSS Driven RF Pulse Generation System Implementing Miniature Optical Sources”, 21UMK009, 04NOV2020

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13 Appendix C: Tradespace Analysis of UWB Shark Antenna

(Sadie Brasel, Kasey Norris and Kalyan Durbhakula)

13.1 Executive Summary

The Shark antenna design had initially offered hope in achieving ultra-wideband (UWB) radiation with high transient gain values due to its unique truncated bi-cone shape. We believed that by carrying out a systematic study, we could uncover something fundamental that could help with enhancing the directional antenna pattern as well as a design that could handle tens of megawatts as input power. The objective was to propose an electrically small Shark antenna that can retain bandwidth as well as improve transient gain value over the state-of-the-art. Our approach has been to perform a systematic study by carefully investigating improvements and degradations on certain metrics at all frequencies of interest and for a given time-domain waveform. We have found two specific Shark antenna design parameters to heavily influence the bandwidth and gain to be the cone height (*h*) and distance to backplane (*d*). The study has yielded insights into the workings of the Shark antenna through parametrized and optimization studies, which have been helpful in the miniaturization of this antenna. However, the improvements (in terms of transient gain) were not significant enough. For this reason and to shift more of our efforts to the more promising Koshelev antenna, we have made a decision to sunset this study.

13.2 Objective

Primary Problem: Determine the extent to which the physical aperture area of an antenna array, composed of antenna elements, can be reduced, while maintaining performance in peak power density, bandwidth, and electronic beam steerability over the UHF range (0.4–1 GHz), compared with present-art high-power-microwave-capable antenna arrays.

Solution Space: An array of Shark antenna elements with an emphasis on inter-element and intra-element spacing effects is a good candidate for UWB HPM systems which maintain a reduced aperture area with respect to the current state-of-the-art. In the literature, the Shark antenna has already been shown to achieve a wide 20:1 impedance bandwidth, low dispersion, and a sectoral (also referred to as directional) radiation pattern.

Sub-Problem: The design parameter space of the Shark antenna has not been studied rigorously in the literature and therefore the effect of these parameters on the antenna metrics is not understood. In addition, the Shark antenna has been shown to be not very directive in the H-plane. Preliminary studies have shown that aperture efficiencies at low frequencies are much better than at higher frequencies.

State-of-the-Art (SOTA): The balanced antipodal Vivaldi antenna (BAVA) is considered to be the SOTA antenna element due to its exceptional 20:1 impedance bandwidth ratio as well as the ability to handle tens-of-MW input power.

Deficiency in the SOTA: The BAVA design parameter space has been exhausted over the past couple of decades. The physical aperture area still remains very large and there is no viable path through tradespace study for further physical aperture area reduction.

Solution Proposed: Explore the Shark antenna array tradespace by generating different array topologies/lattices (hexagonal, octagon, square, elliptical) with different intra- and interelement spacing combinations.

Relevance to OSPRES Grant Objective: The Shark antenna dimensions were established to be frequency dependent and can be readily modulated to fit the spectrum characteristics of an ultra-fast rise time input pulse.

13.3 Technical Background

The Shark antenna is a form of bi-cone antenna with a reflector connected to the top ends of the bi-cone. In addition, the bi-cones of the Shark antenna are truncated vertically (E-plane) and slightly tilted/inclined to make the antenna directional in the E-plane. Desrumaux et al [1] is the only known group working on the Shark antenna. The authors of [1] claim that the primary purpose in the development of this antenna is to demonstrate miniaturization, improve the front-to-back ratio, and have it be non-dispersive.. The authors performed simulation studies on multiple parameters of the Shark antenna. Fig. 13.1 shows the gradual transition of the Shark antenna design starting from a simple bi-cone antenna design.

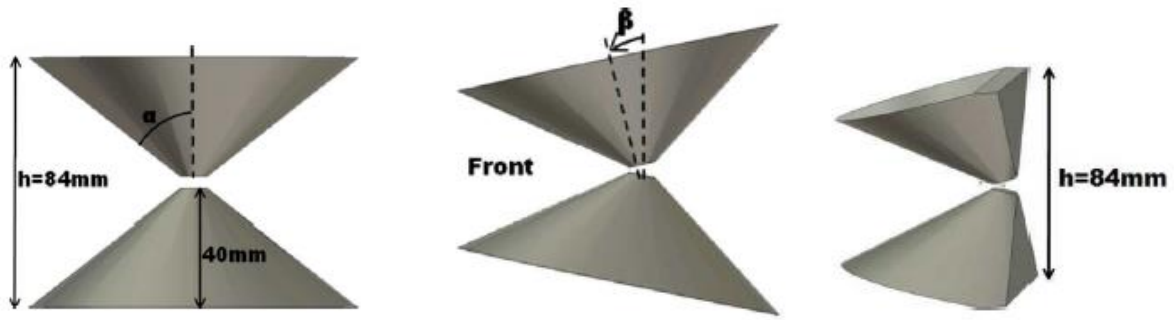
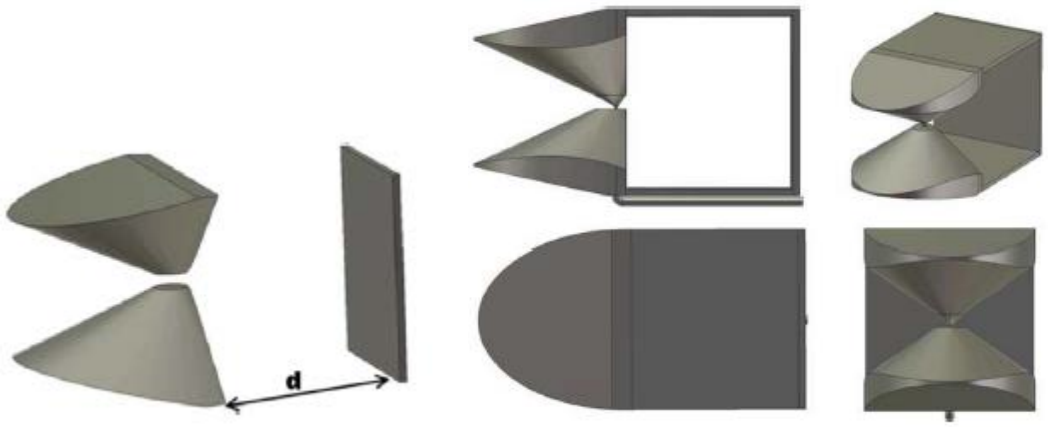


Figure 13.1. (a) Traditional bi-cone (b) Inclined bi-cone and (c) Truncated bi-cone.

As reported in [1], a big disadvantage with a bi-cone antenna is that its radiation pattern is omnidirectional in the H-plane. To make the antenna directional in one of the planes, the two cones have been inclined at a certain angle (β), which can be seen in Fig. 13.1(b). As seen in Fig. 13.1(c), the cones are truncated to improve the radiation in front of the antenna. To further assist in improving the radiation pattern in front of the antenna, a reflector plate has been added at the back of the antenna, which can be seen in Fig. 13.2(a). A complete design of the Shark antenna can be seen in Fig. 13.2(b).



(a) (b)

Figure 13.2. (a) Adding a reflector at the back. (b) Complete Shark antenna model.

This completes the design of the Shark antenna. It is reported in [1] that the width, height, and length of the Shark antenna are electrically small at the initial operating frequency/wavelength. This is one of the reasons to consider this antenna for further study by our group. The authors did not report any detailed parameter study in [1] to really understand their effect on the radiation. It was also reported that the Shark antenna array has a good front-to-back ratio, which is useful to have in transient UWB radiation. For these reasons, this antenna was pursued to improve our understanding of another transient UWB antenna as well push the state-of-the-art.

13.4 Tasks, Milestones, and Status

(A) Complete initial design, simulation, and validation of the Shark antenna / JAN21 / Complete.

(B) Validate Shark antenna design using the LEWIS supercomputer over a wider range of frequency results (up to 20 GHz) / FEB–MAR21 / Complete.

(C) Identify Shark antenna design parameters which contribute significantly to bandwidth, gain, and physical aperture area. Determine which parameters contribute most to performance improvement/size reduction/ FEB–MAR21 / Complete.

(D) Perform a tradespace study by simulating the Shark antenna with varying cases of flare angle, cone length, and distance to backplane. Gain a general understanding of how these parameters affect impedance bandwidth, rE/V, gain and HPBW / FEB–MAY21 / Complete.

- Milestone: produce a detailed summary of change in impedance bandwidth, rE/V, HPBW in H-plane and E-plane as a function of flare angle (α), cone height (h), and distance to backplane (d) / Complete.
- Milestone: Choose the optimal Shark antenna design that has the lowest operating frequency within size requirements based on tradespace study / Complete.

(E) Using the optimal Shark antenna design in (D), simulate various array geometries including hexagonal, rectangular, and circular arrays. Determine which array geometries are optimal and analyze aperture fields and aperture efficiencies. Further study the effect of different time-domain waveforms in the far-field radiated by the optimized Shark antenna array / MAY–NOV21 / Complete.

- Milestone: Produce a report which states the effects of various array geometries for the Shark antenna. The optimal array geometry chosen should have the least interference between elements, therefore yielding higher impedance bandwidth and higher aperture efficiency. Overall, the optimal Shark array geometry should have at least 20% impedance bandwidth at 900 MHz center frequency for the centermost element with 130% array aperture efficiency, ± 60 degrees beam steering capability, and rE/V equal to or greater than 4. Identify a waveform that combines well with the optimized Shark antenna array in terms of peak electric field, rE/V, and energy density.

(F) Begin prototyping and validation of optimal Shark antenna single element. / JUN–DEC21 / Complete.

- Milestone: Have a finished Shark antenna prototype. Compare S11 and radiation pattern with simulated Shark antenna.

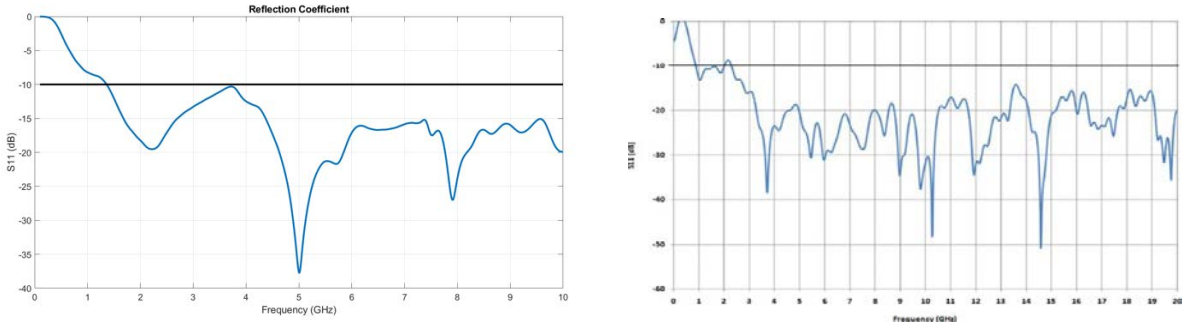
13.5 Methods and Approach

The methodology used in this study is relatively straightforward. The single element Shark antenna design has been initially parametrized to understand each design variable effect on the antenna performance. The parametrization has been carried out using the commercial electromagnetic (EM) wave solver CST microwave studio. Each design variable has been systematically varied and studied to understand its effect on antenna input impedance, antenna bandwidth, antenna pattern, peak gain, half-power beamwidth in E-plane and H-plane, transient gain, time domain electric field, and electric field frequency spectrum. After detailed investigation, an optimum single element Shark antenna of aperture area of 90 mm x 30 mm has been finalized and fabricated. Using simulations, the optimized single element Shark antenna has been converted into various array shapes with different interelement spacing values. A detailed time-domain study by feeding different pulses of interest has been carried out.

13.6 Results and Discussion

The study initially started with validating the Shark antenna design reported in [1]. In this section, we present some of the important antenna metrics (reflection coefficient, frequency domain gain, transient gain, E-plane beamwidth, H-plane beamwidth, and aperture efficiency) for both optimized single element Shark antenna and for an optimal array topology. Furthermore, we compared the above metrics for both single element and array designs in a table to be able to clearly see the tradeoffs between different design parameter values and for different array topologies. We have also included time-domain electric field responses especially for different array topologies. The frequency domain and time-domain studies clearly determined a particular array topology to be the optimum topology.

First, the reflection coefficient (S11) of the shark antenna has been shown to be matched to the reference input impedance (i.e., Z_{input} = 150 Ω) from ~1.5–10 GHz (Figure 13.3).



(a) **(b)**

Figure 13.3. Original Shark antenna S11 result (a) from CST simulation (b) from [1].

From Figure 13.4, we can notice that the Shark antenna cases with a large flare angle (α) value are not well matched to the reference impedance of 150 Ω. The α = 20° and α = 45° cases are matched to the reference impedance over a wide range. From Figure 13.4, we can notice that smaller α values perform better at low as well as high frequencies.

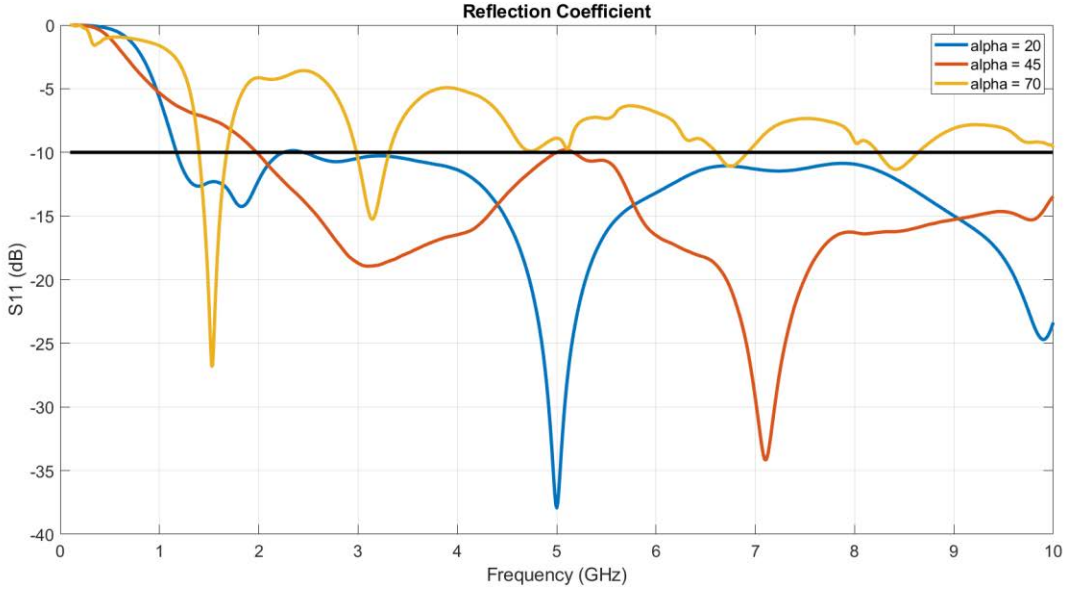
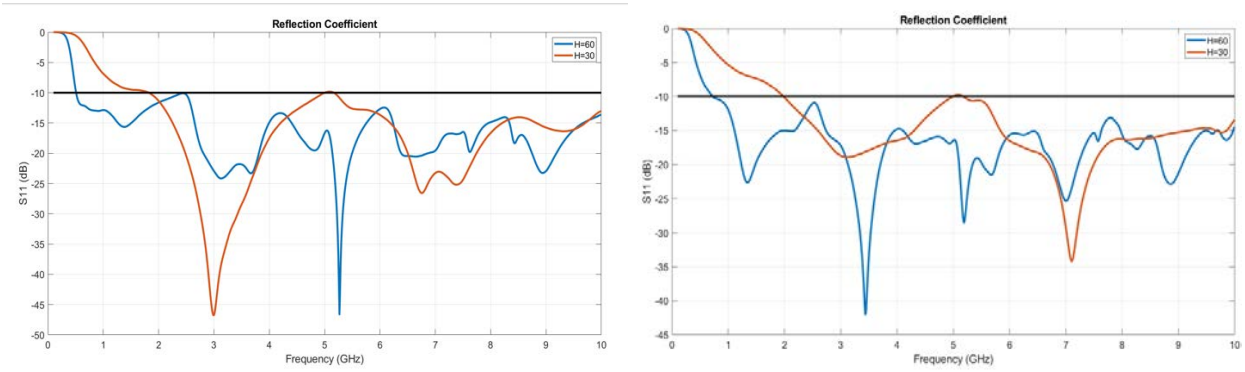


Figure 13.4. Reflection coefficient for *h* = 30 mm and *d* = 7 mm cases.



(a) (b)

Figure 13.5. Reflection coefficient: (a) α = 45° *d* = 45 mm (b) α = 45° *d* = 75 mm.

From Figure 13.5. the *h* = 60 mm case performs better than the *h* = 30 mm case for both values of *d*, as the reflection coefficient curve is below the –10dB line for a wider range of frequencies. Our preliminary study indicated that smaller alpha (α) values and larger *h* values resulted in improved S11 performance.

Table 13.1. Shark parametric study results.

H	d	Flare Angle	Frequency Dependent Dimensions (W,H,L) $\lambda = \frac{c}{5.5e9}$	Physical Aperture area $A_{phs} = W * H$	Bandwidth	Lowest Cutoff Frequency	Peak gain (5.5 GHz)	Directionality (5.5 GHz)		Aperture Efficiency (%) (5.5 GHz)
								E-plane	H-plane	
30 mm	75 mm	20°	$\frac{\lambda}{2.497}, \frac{\lambda}{0.8798}, \frac{\lambda}{0.59177}$	~0.001354 m^2	>10:1	1.168 GHz	3.534 dBi	48.7°	188.2°	61.79525764
		45°	$\frac{\lambda}{0.909}, \frac{\lambda}{0.8798}, \frac{\lambda}{0.492}$	~0.00372 m^2	>10:1	2 GHz	4.874 dBi	89.1°	97.8°	31.02057555
		70°	$\frac{\lambda}{0.3349}, \frac{\lambda}{0.8798}, \frac{\lambda}{0.337}$	~0.01022 m^2	Poor BW	1.39 GHz	5.573 dBi	49°	200°	12.91056991
60 mm	75 mm	20°	$\frac{\lambda}{1.249}, \frac{\lambda}{0.447}, \frac{\lambda}{0.5}$	~0.00533 m^2	>10:1	0.625 GHz	5.196 dBi	107.4°	69.4°	23.08071189
		45°	$\frac{\lambda}{0.455}, \frac{\lambda}{0.447}, \frac{\lambda}{0.373}$	~0.01464 m^2	>10:1	0.731 GHz	6.813 dBi	30°	54.4°	11.01804594
		70°	$\frac{\lambda}{0.165}, \frac{\lambda}{0.447}, \frac{\lambda}{0.220}$	~0.0402 m^2						
30 mm	45 mm	20°	$\frac{\lambda}{2.497}, \frac{\lambda}{0.8798}, \frac{\lambda}{0.59857}$	~0.001354 m^2	>10:1	1.219 GHz	3.959 dBi	39.8°	125.6°	69.22677561
		45°	$\frac{\lambda}{0.909}, \frac{\lambda}{0.8798}, \frac{\lambda}{0.492}$	~0.00372 m^2	>10:1	1.793 GHz	4.850 dBi	46.3°	228.5°	30.86782754
		70°	$\frac{\lambda}{0.331}, \frac{\lambda}{0.8798}, \frac{\lambda}{0.413}$	~0.01022 m^2	Poor BW	1.453 GHz	5.402 dBi	120.1°	73.9°	12.51442646
60 mm	45 mm	20°	$\frac{\lambda}{1.249}, \frac{\lambda}{0.447}, \frac{\lambda}{0.699}$	~0.00533 m^2	>10:1	0.644 GHz	4.653 dBi	82.8°	73.6°	20.66869754
		45°	$\frac{\lambda}{0.455}, \frac{\lambda}{0.447}, \frac{\lambda}{0.473}$	~0.01464 m^2	>10:1	0.512 GHz	8.425 dBi	37.1°	79.5°	13.62498708
		70°	$\frac{\lambda}{0.165}, \frac{\lambda}{0.447}, \frac{\lambda}{0.249}$	~0.0402 m^2						

Table 13.1 presents a comparison of physical aperture area, bandwidth, lowest cutoff/operating frequency (–10 dB), peak gain, E-plane beamwidth, H-plane beamwdith, and aperture efficiency at the center frequency. Table 13.1 shows that the Shark antenna with a larger physical area yields the maximum gain at the center frequency (5.5 GHz) and smallest aperture efficiency value. Therefore, the Shark antenna design with the most optimal aperture efficiency is the case with the smallest overall size, as highlighted in Table 13.1, and is considered for further studies. Taking the above design as the optimized single element Shark antenna design, we proceeded to investigate various array shapes.

A 3 x 3 Shark antenna array has been simulated. When creating the Shark antenna array, one can choose to connect the reflector plate of the individual elements or not. Both options have been explored as shown in Figure 13.6.

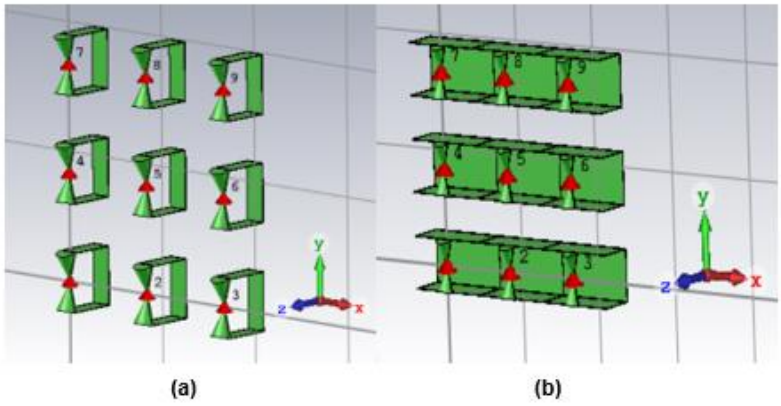


Figure 13.6. 3 x 3 Shark antenna array: (a) disconnected reflectors (b) connected reflectors.

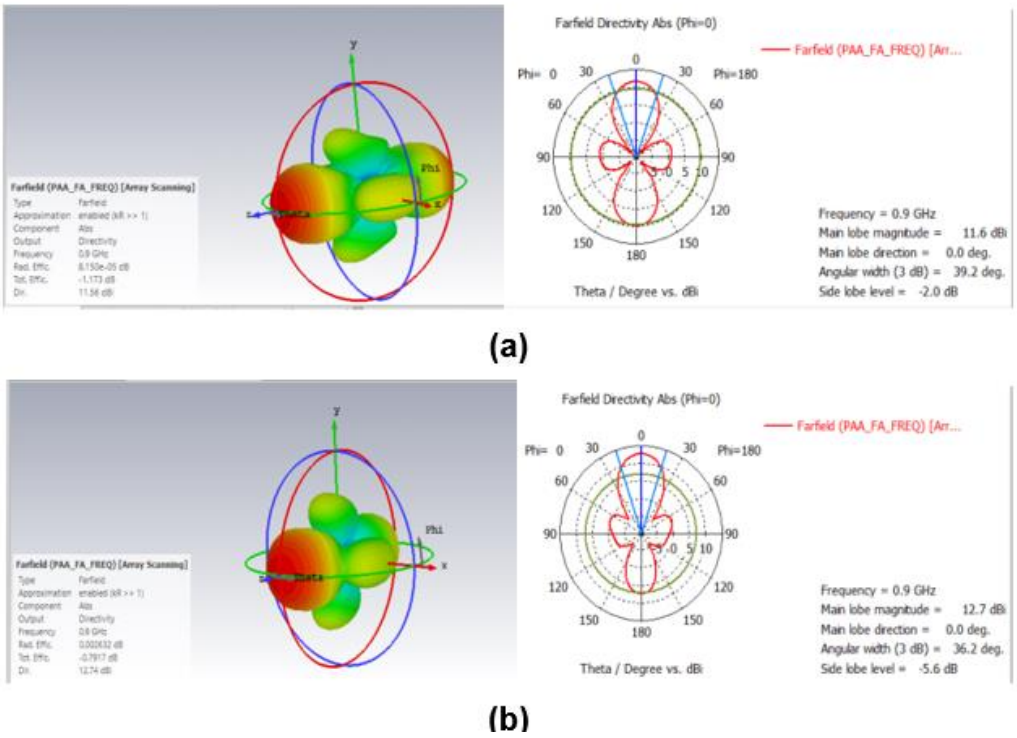


Figure 13.7. 900 MHz radiation pattern of square arrays for an (a) unconnected reflector (b) connected reflector.

From Fig. 13.7 it is evident that a connected reflector yields higher peak gain at 900 MHz than the unconnected reflectors. Therefore, we have chosen to use connected reflectors for the remainder of the Shark antenna array studies. Later, we compared the square Shark antenna array output response to that of hexagon and ellipse Shark antenna array output responses. The hexagon and ellipse shaped arrays had in total 8 elements. In comparison, the ellipse Shark antenna array turned out to be the optimum for its performance. This comparison has been shown in Table 13.2.

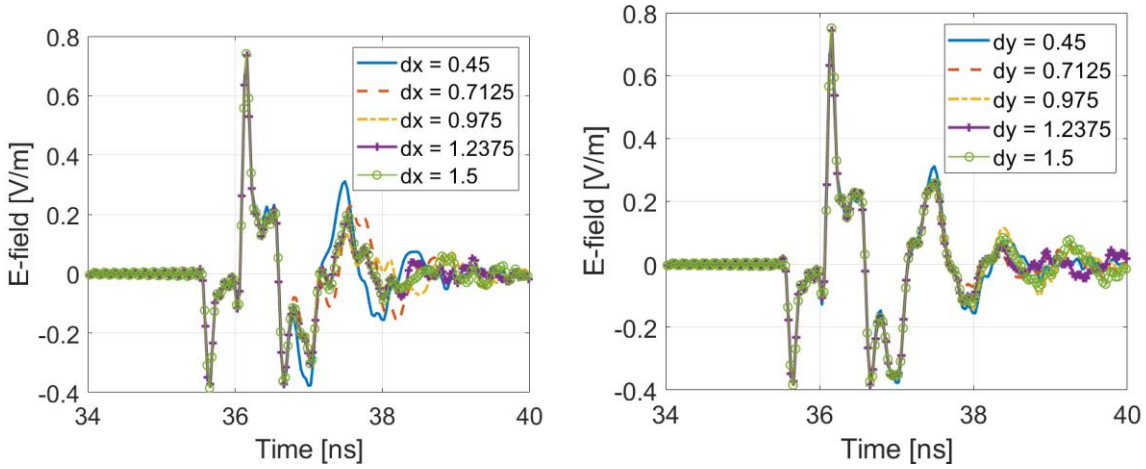
Table 13.2. Performance comparison of Shark array geometries.

Geometry	# of Elements	Max Gain (900MHz) (dBi)	Aperture Efficiency (%)	rE/V (1m)	rE/V (2m)	Beamwidth (°)	Sidelobes (dB)
square	9	12.719	53.13	8.91	9.25	36.2	-5.6
hexagon	8	11.728	52.38	7.98	8.21	32.4	-4.5
ellipse	8	12.408	52.3	7.86	8.13	40.4	-5.2

The efforts to fabricate the optimized single element Shark antenna were initiated to validate the simulation results. In parallel, we extended our study and analysis to feeding time-domain pulses of interest to the optimized elliptical Shark antenna array.

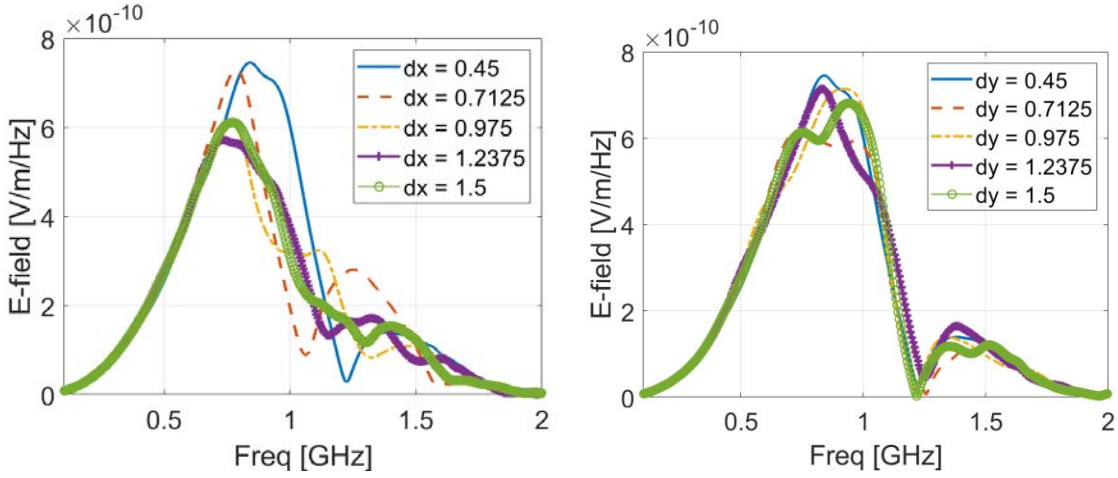
A normalized 900 MHz damped rectangular wave has been fed to the array elements to obtain the time domain radiated electric field at 10-meters distance from the aperture of the array antenna (Fig. 13.8). From comparing the frequency spectrum plots in Fig.

13.9(a) and Fig. 13.9(b), a significant difference can be noticed in Fig. 13.9(a), which shows that the radiated electric field is more sensitive to the interelement spacing variable in the x-axis (H-plane) than in the y-axis (E-plane). In Fig. 13.9(a), the 900 MHz peak frequency spectrum has been obtained for the interelement spacing value of d_x = 0.45.



(a) (b)

Figure 13.8. Simulated electric field at 10-meter distance from the aperture of the elliptical Shark antenna for different (a) interelement spacing values in the x-axis, and (b) interelement spacing values in the y-axis.



(a) (b)

Figure 13.9. Frequency spectrum of the simulated electric field at 10-meter distance from the aperture of the elliptical Shark antenna for different (a) interelement spacing values in the x-axis, and (b) interelement spacing values in the y-axis.

The optimized single element Shark antenna element was prototyped in August 2021. Fig. 13.10 shows two views of a 3D printed and metallized Shark antenna. The back plate is cut out from an aluminum sheet, whereas the cones were 3D printed and coated using nickel paint.

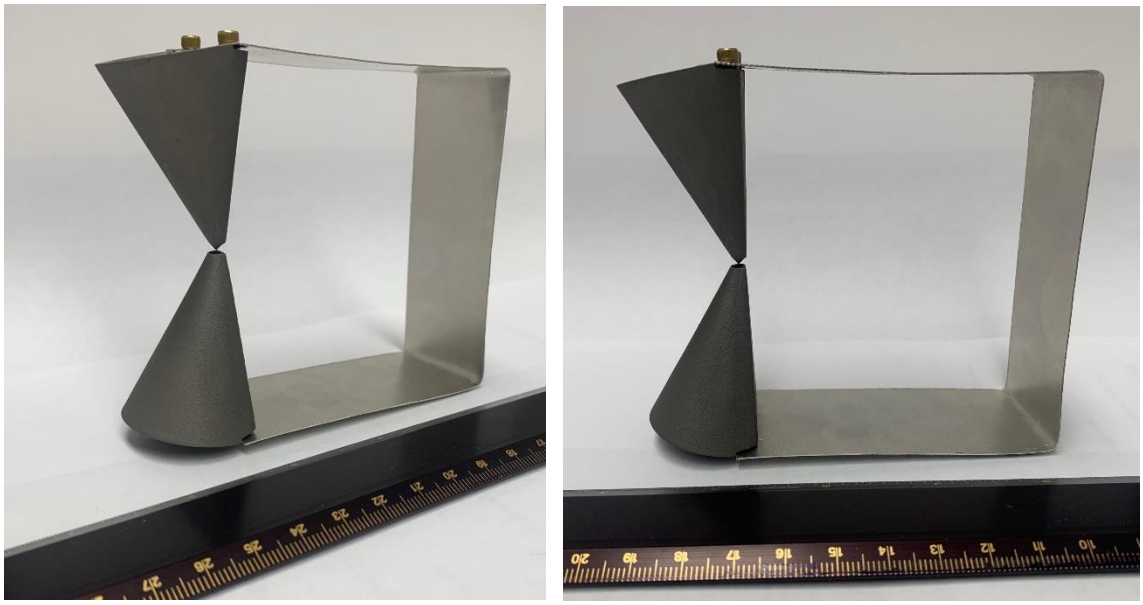


Figure 13.10. 3D printed and Metallized Single Element Shark antenna.

Later, we tried feeding other pulses of interest to the elliptical Shark antenna array as well as to the other array topologies to draw a comparison of time-domain electric field at 10 m distance. This comparison is shown in Fig. 13.11. It is evident that the square topology has the maximum peak E-field values followed by hexagonal and elliptical topologies. Similar observations were noted from feeding other pulses. This drew us to a preliminary conclusion that an unconventional Shark antenna array shape may not yield maximum peak E-field. One advantage noticed with unconventional array shapes is the decrease in side lobe level compared to square.

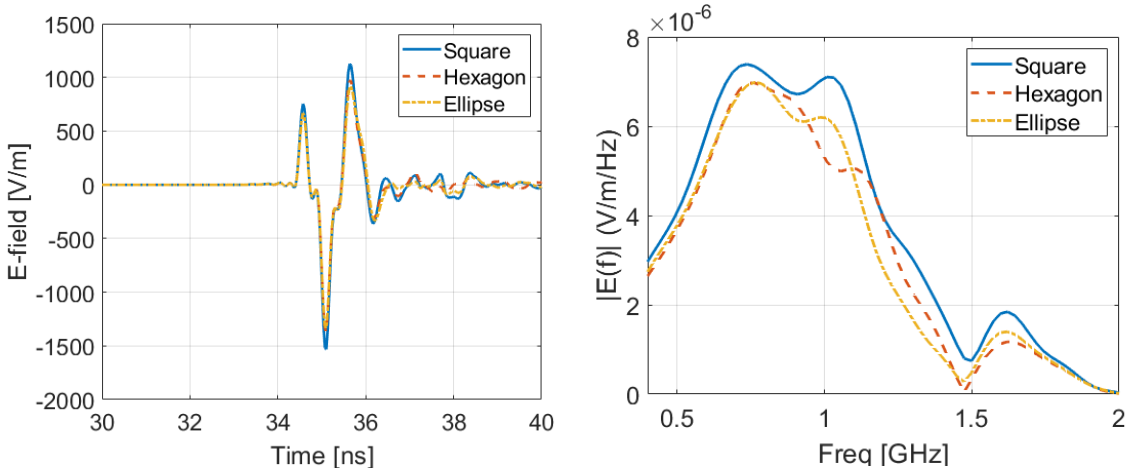


Figure 13.11. Radiated electric field at 10 m distance from three array topologies when excited by mega-impulse bipolar signal. (a) E-field in time domain and (b) frequency spectrum of E-field.

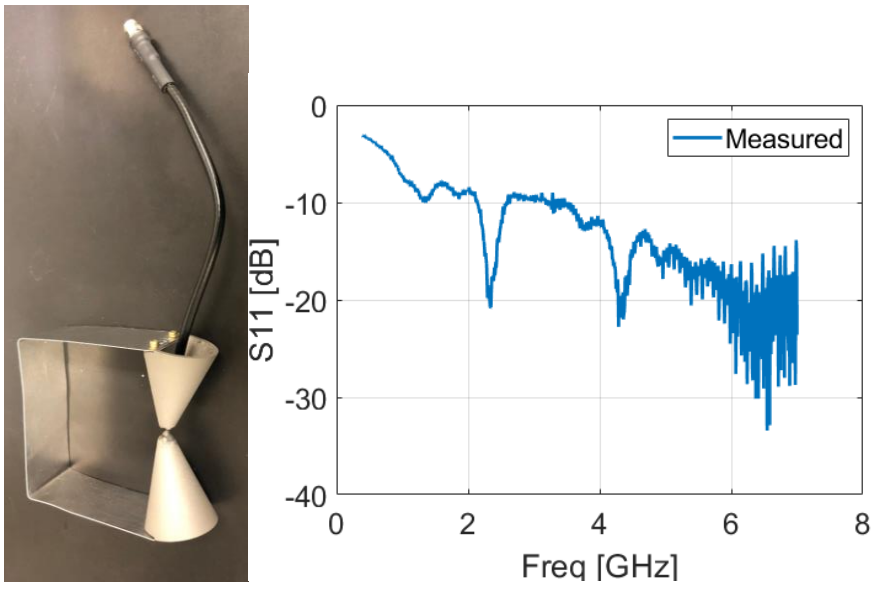
We have also simulated the elliptical Shark antenna array with different pulses and obtained their peak E-field at 10 m, transient gain, and energy density values. Table 13.3

shows these values for different pulses. The rE/V for an array is not satisfactory. This further led us to believe that this design may not be a right choice.

Table 13.3. Elliptical Shark antenna array response with different pulse source waveforms at 10 meters distance.

Pulse source	Epeak [kV/m]	rE/V	Ed [uJ/m2]
AT Marx	1.2	2.6	1.26
MI0731	1.3	2.5	2.33
DSRD 2x2	0.3	0.4	0.31
DSRD 4x2	0.78	0.4	2.25
NPG22	0.16	0.08	0.54
PPM2022	1.3	0.6	9.1

The assembled prototype of the optimized single element Shark antenna is shown in Fig. 13.12(a). The S11 result for the 3D printed and metallized single element Shark antenna is shown in Fig. 13.12(b) First the reflections are high before 2 GHz, which is unacceptable. Although the performance was satisfactory from 2 GHz to 4.5 GHz, the unusual noise at beyond 4.5 GHz might imply that it is difficult to achieve the required feed precision using the tools available at our disposal. This cemented our belief that it perhaps may be worth focusing our efforts on better antennas such as the Koshelev antenna and sunset the Shark antenna effort.



(a) (b)

Figure 13.12. Measured reflection coefficient of the optimized single element Shark antenna.

13.7 Summary and Recommendations

(A-B) The Shark antenna has been designed, simulated, and validated according to [1].

(C) The Shark antenna design parameters that have been found to contribute significantly to bandwidth performance, directivity, and gain are the cone height (*h*) and distance to backplane (*d*).

(D) The Shark antenna tradespace study has been completed and has provided insight into the Shark antenna design space. Increasing the cone height *h* yields better impedance bandwidth at low frequencies and is more directive in the E and H planes. However, increasing *h* results in a larger aperture area. To remain within 90 x 90 mm, the maximum *h* value is 45 mm; with this the lowest operating frequency of 815 MHz is achievable.

(E) The elliptical Shark antenna array topology yielded the optimum array metrics, which can be found in Table 13.2. The array metrics obtained from the elliptical Shark antenna array are closer to the desired metrics provided in milestone (E). The interelement spacing variable study has provided insight into the workings of a Shark antenna array. The Shark antenna array is more sensitive to the interelement spacing variable in the H-plane than in the E-plane. The elliptical topology has significantly smaller sidelobe level values and similar frequency-domain gain or transient gain values when compared against square and hexagonal topologies. If the input is a monopolar signal, a hexagonal or an elliptical topology is preferred. If the input is a bipolar signal, an elliptical topology is recommended for its decent transient gain value with significantly smaller sidelobe levels.

Recommendations: Overall, the Shark antenna is ideal for applications that can utilize a miniaturized version and slightly directive antenna version of a bi-cone antenna. The Shark antenna is also ideal for applications that do not require high transient gain values and require wider beamwidth in the H-plane. The two Shark antenna design parameters that stood out during this study to have the maximum effect were the cone height and distance to backplane. Employing a robust stochastic algorithm could further improve the transient gain value. In addition, more detailed study of the array topology is needed to study the interaction between individual Shark antenna elements.

13.8 References

[1] L. Desrumaux, A. Godard, M. Lalande, V. Bertrand, J. Andrieu and B. Jecko, "An Original Antenna for Transient High Power UWB Arrays: The Shark Antenna," in IEEE Transactions on Antennas and Propagation, vol. 58, no. 8, pp. 2515- 2522, Aug. 2010, doi: 10.1109/TAP.2010.2050418.

ONR HPM Program – Monthly Status Report (MSR) – February 2022

Anthony Caruso – Univ. Missouri – Kansas City

N00014-17-1-3016 [OSPRES Grant]

ONR Short Pulse Research, Evaluation and non-SWaP Demonstration for C-sUAS Study

15 MARCH 2022

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OSPRES Grant Objective: to execute high-risk, high-payoff efforts that mitigate, fill or rectify one or more grand-challenge or elementary gaps or deficiencies needed to achieve a modular, scalable and electronically steerable high-power microwave (HPM) based defense system for the counter unmanned aerial system (cUAS) mission. The OSPRES HPM system and sub-system development/evaluation efforts are focused on the short-pulse high-average-power space and includes the kill chain considerations including the target and its responsivity to radiofrequency stimuli.

OSPRES Metrics of Success: developed technologies and capabilities that are published in the peer review, protected as intellectual property, and/or, transitioned to the OSPRES Contract effort and beyond for integration with other DoD needs or dual-commercial-use, as enabling/integrable capability(ies).

OSPRES Grant Approach: A fail-fast philosophy is maintained, where if a technology or capability is deemed infeasible to be demonstrated or validated during the project period-of-performance, it shall be culled, results to date and basis of infeasibility documented, and the next major gap/deficiency area addressed by that part of the project sub-team. Students whose thesis depends on following through with a full answer during the life of the award will be given special dispensation to continue their work.

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1 Contents

2 Executive Summary

2.1 Progress, Significant Findings, and Impact

Fiber Laser and Optical Amplifiers. The tubular-core optical amplifiers that we are developing permit higher power levels of operation than standard optical fiber amplifiers. Hot spots, i.e., points of high peak-to-average ratio (PAR) of field strength, discovered in the tubular-core optical amplifier, could lead to damage and thereby restrict its operating power. We demonstrate that the locations of these hot spots are set by geometric factors (i.e., the *locations* are set via purely linear effects). The *size* of these PARs, however, are greatly enhanced by the fiber nonlinearity (from barely observable to factors of ten or more). Linear anti-reflective techniques are inapplicable, so we mitigate this nonlinear enhancement via the effects of gain saturation and obtained a reduction of the PAR of one such resonance from 12 down to 1.5.

On-State Resistance in GaN:X PCSS. A literature review revealed a ~100x increase in photocurrent—1.9 μA to 106 μA at a trigger fluence of 3.8 mW/cm^2—through the addition of a nanostructured array of fins, or grooves, in the gap length of lateral GaAs PCSS. This addition helps overcome on-state resistance minimization limitations due to the shallow photon absorption depth in GaAs at an incident wavelength of 532 nm and increases the effective device volume. A similar alteration will be studied in future simulations to determine the effectiveness of this approach in reducing on-state resistance in GaN:C PCSS.

DSRD Optimization Simulations. To achieve drift-step recovery diode (DSRD)-only peak load (50-Ω) voltage $\geq$40-kV with risetime <2-ns, circuit simulation (e.g., SPICE) models matching measured values to <5% are necessary to optimize DSRD-based pulsers. At a subsystem level the standard RC model yields error >>5% in the rise-, fall- and recovery-time/profile as a function of charging condition due primarily to the use of a standard/simple RC model; additional parasitics and non-linear elements must be included. We have attacked the underlying missing physics by adapting the CMC industry-standard diode model, which includes an improved recovery model (that can adjust cutoff or transition time to experiment) and detailed charge/discharge diode current. While our revised DSRD model has shown accuracy within 10%, the cases are limited and not consistent across input voltages (50-V to 200-V) and trigger durations (100-ns to 1000-ns). The CMC diode model will improve the revised DSRD model. The next improvement iteration will include physics into the Verilog-A code.

DSRD Processing and Manufacturing. We have improved a process step for diode sidewall termination. We had previously experimentally demonstrated the technical feasibility of our new, patented sidewall termination process. Instead of the traditional method of mechanically sawing a wafer into dies and etching away damage from the sawing process, we use anisotropic etching. Here, V-grooves are formed by the etch around each die. These diode termination sidewalls inherently have no cracks, thus no need for etching away damage. Additionally, the walls have a 57^o slope, thus increasing the breakdown voltage along the surface by 40% compared to vertical diode sidewalls in the traditional technology. A new anisotropic etching recipe was developed using a TMAH/DMSO mixture—used for Si V-groove etching for the first time—which shows

better uniformity, surface roughness, and edge rounding as compared to known anisotropic etch chemistries.

DSRD Design of Experiments. If proven to be intrinsic to the diode, variation in DSRD performances can manifest themselves as poor pulser circuit outputs, particularly when pairs of diodes are required to operate in harmony. A randomized complete block design (RCBD) experiment has been employed to reduce the effects of outside factors (e.g., operator or equipment bias) from influencing the diode test results. Initial findings of the RCBD show that the Gen2 DSRDs have the greatest variability in the capacitance–voltage measurements. To date, data collection has been completed on all of the first six rounds for the experimental design, but only the zero junction bias capacitance (ZJBC) measurements have been evaluated. Average Gen2 measurements range from 8.8E-10 to 1.1E-08F with standard deviations ranging from 2.4E-11 to 6.0E-09F. As a comparison to the least variable group of DSRDs, the Untested Deep Diffusion diodes have an average ZJBC measurements ranging from 6.6E-10 to 6.8E-10 with standard deviations ranging from 6.0E-12 to 1.7E-12F. Understanding the significance that diode variation has on the pulser circuit will lead to better diode selection decisions in the future.

DSRD-Based Pulsed Power Source Optimization*.* A pulsed output of 6.7 kV has been achieved with a DSRD pulser optimized for 28-stack diodes (four 7-stack diodes) with a prime source of 120 V, achieving a voltage gain of 55.8 (37% higher than the previous generation pulser). Testing of the pulser with higher prime source voltage has shown the potential to increase the output to 14–18 kV, limited by diode breakdown. Testing of individual 7-stack diodes and their combination has shown a significant variation in diode performance, resulting in large variations in output pulse voltage. In the coming reporting periods, we will design 21-stack and 28-stack pulsers utilizing higher current pumping schemes and selected diodes from the experiments performed so far.

Continuous Wave Diode-NLTL Based Comb Generator. Simulation and testing efforts on continuous wave D-NLTLs have been focused on minimizing the power reflected back to the source by varying the impedance(s) at source–line and line–load interfaces in an attempt to attain matched impedance. Despite the frequency doubling demonstrated by the D-NLTLs, the continually varying line impedance induced mismatch still shows ~60% power reflection back to the source, limiting the line efficiency to <7%. A dynamic impedance matching technique to mitigate the power reflection will be explored in the next reporting cycle.

Dynamically Tunable Multi-Frequency Solid-State Frozen Wave Generator. A redesigned tunable 12-segment lumped-element-based FWG was fabricated and tested up to 400 V to address the peak pulse reduction and pulse overlap issues reported in the earlier report. The change in the switch location and reduced footprint in the new design addressed the peak reduction problem partially, but the damaged tunable components were found to limit the performance in the unbalanced load configuration, leading to pulse overlap. This will be reviewed and addressed in the next reporting cycle.

Pulse-Compression-Based Signal Amplification. Different magnetic core materials were investigated to determine the most suitable candidate for high-frequency magnetic pulse compression (MPC), based on the core criteria reported in the Jan 2022 MSR. Commercially available magnetic cores are grouped as ‘soft’ iron, silicon steel,

amorphous, nanocrystalline, powder, and ferrites. NiZn ferrites were determined to be the best option for the high-frequency MPC application as they have the highest operating frequency of up to 300 MHz and lowest B_{sat} at ~0.2–0.4 T. The relative permeability of NiZn ferrites is low at 100 to 1000 but it is sufficient for this application. YIG-based toroid core development for high frequency MPC has been suggested by the Kostas Research Institute (KRI) at Northeastern University. Collaboration on high-frequency magnetic material development is being considered with KRI.

Antennas. A 4×4 square array (0.7–1.05 GHz), composed of coaxial probe-fed, microstrip patch, ESA elements, has been modeled and characterized. Reasonable rE/V values (≈1) were achieved when the array elements were subjected to various short monopolar pulses. The array model will be recharacterized upon integration with the customized feeding structures, which are currently being modeled and characterized. On achieving reasonable array performance from the end design, the model will be forwarded for building the final demonstrable prototype.

A second variant of the Koshelev antenna was 3D-printed, assembled, metallized, and measured for conductivity to develop a functioning and effective Koshelev antenna prototype. The prototype was initially metalilzed with nickel paint, which yielded a conductivity value of 600 S/m. Later, the same prototype was coated with a layer of silver paint, which yielded a conductivity value of 3000 S/m, improving the conductivity by 5x.

A tradespace study of antenna arrays using two specific machine learning (ML) models (k-nearest neighbors and least squares regression) was expanded to predict antenna power pattern as a function of elevation angle at the desired frequency. Between the two ML models, the k-nearest neighbors yielded a smaller root mean square error value (RMSE) of 2 (an ML model with an RMSE value of <1 is assumed to be a good ML predictive model).

2.2 Completed, Ongoing, and Cancelled Sub-Efforts

	Start	End
2.2.1 *Ongoing Sub-Efforts*		
GaN:C Modeling and Optimization	OCT 2017	Present
Diode-Based Non-Linear Transmission Lines	FEB 2018	Present
Trade Space Analysis of Microstrip Patch Arrays	FEB 2019	Present
Enclosure Effects on RF Coupling	OCT2019	Present
Lasers and Optics	FEB 2020	Present
UWB Antenna Element Tradespace for Arrays	MAY 2020	Present
Si-PCSS Contact and Cooling Optimization	JAN 2021	Present
Drift-Step Recovery Diode Optimization	JAN 2021	Present
UAS Engagement M&S	MAR 2021	Present
DSRD-Based IES Pulse Generator Development	APR 2021	Present
Drift-Step Recovery Diode Manufacturing	MAY 2021	Present
IES Diode Characterization	MAY 2021	Present
Sub-Nanosecond Megawatt Pulse Shaper Alternatives	MAY 2021	Present
Ultra-Compact Integrated Cooling System Development	MAY 2021	Present
GaN-Based Power Amplifier RF Source	AUG 2021	Present
Reconfigurable RF Pulsed-Power Source	AUG 2021	Present
RF Driver Unit for GaN SD-MPM Power Amplifier	SEPT 2021	Present
Reconfigurable RF Antenna for SD-MPM Sources	SEPT 2021	Present
Continuous Wave Diode-NLTL Based Comb Generator	SEPT 2021	Present
2.2.2 *Completed Sub-Efforts*		
Adaptive Design-of-Experiments	OCT 2017	APR 2019
Non-perturbing UAV Diagnostics	OCT 2017	OCT 2018
Noise Injection as HPM Surrogate	OCT 2017	MAR 2019
SiC:N,V Properties (w/ LLNL)	APR 2018	MAR 2019
Helical Antennas and the Fidelity Factor	JUL 2018	SEPT 2019
Si-PCSS Top Contact Optimization	APR 2020	OCT 2020
Nanofluid Heat Transfer Fluid	NOV 2020	JUL 2021
HV Switch Pulsed Chargers	DEC 2018	DEC 2021
2.2.3 *Cancelled/Suspended Sub-Efforts*		
Ab Initio Informed TCAD	OCT 2017	OCT 2020
Positive Feedback Non-Linear Transmission Line	NOV 2017	DEC 2018
Minimally Dispersive Waves	FEB 2018	SEPT 2018
Multiferroic-Non-linear Transmission Line	NOV 2018	APR 2019
Avalanche-based PCSS	SEPT 2018	SEPT 2019
Gyromagnetic-NLTL	DEC 2017	NOV 2020
Multi-Stage BPFTL	APR 2020	JUL 2020
Heat Transfer by Jet Impingement	MAY 2018	FEB 2021
Si, SiC, and GaN Modeling and Optimization	NOV 2018	FEB 2021
Bistable Operation of GaN	FEB 2021	MAR 2021
IES Pulser Machine Learning Optimization	MAY 2021	AUG 2021
WBG-PCSS Enabled Laser Diode Array Driver	NOV 2020	JAN 2022

2.3 Running Total of Academic and IP Program Output

See Appendix for authors, titles and inventors (this list is continuously being updated)

Students Graduated	*5 BS, 8 MS, 3 PhD*
Journal Publications	*5 (6 submitted/under revision)*
Conference Publications	*33 (4 submitted/accepted)*
External Presentations/Briefings	*17 (23 submitted/accepted)*
Theses and Dissertations	*4*
IP Disclosures Filed	*10*
Provisional Patents Filed	*4*
Non-Provisional Patents Filed	*0*

3 Laser Development

3.1 Fiber Lasers and Optical Amplifiers

(Scott Shepard)

3.1.1 *Problem Statement, Approach, and Context*

Primary Problem: High-average-power 1064-nm picosecond lasers are too large (over 1100 cm^3/W) and too expensive (over \$1000/μJ per pulse) for PCSS (photoconductive semiconductor switch) embodiments of HPM-based defense systems. For example, a laser of this class might occupy a volume of 1 m x 30 cm x 30 cm = 90,000 cm^3 and provide an average power of 50 W (thus, 1800 cm^3/W). Costs in this class range from \$100K to \$300K to drive our Si-PCSS applications.

Solution Space: Optically pumped ytterbium-doped optical fiber amplifiers, fed by a low-power stable seed laser diode, can offer a cost-effective, low-weight, and small-volume solution (with respect to traditional fiber and traditional free-space laser designs). Moreover, our novel optical amplifier tubes, might operate at far higher power levels (over 1000 times greater), thus driving an entire array of PCSS with a single amplifier and thereby reducing the overall system costs and eliminating the optical pulse-to-pulse jitter constraints.

Sub-Problem (1): Optical pump power system costs account for over 50% of the budget for each laser (in this class, for normal/free-space, optical fiber, and tubular embodiments).

Sub-Problem (2): Fiber (as well as power tube) optical amplifier performance is degraded primarily by amplified spontaneous emission (ASE) noise, which limits the operating power point, and by nonlinearities, which distort the optical pulse shapes.

State-of-the-Art (SOTA): Free-space NdYAG lasers or Ytterbium-doped fiber amplifiers optimized for LIDAR, cutting, and other applications.

Deficiency in the SOTA: Optical pump power system costs (in either free-space or fiber lasers) are prohibitive for the PCSS applications until reduced by a factor of at least two.

Solution Proposed: Fiber lasers permit a pre-burst optical pumping technique (wherein we pump at a lower level over a longer time) which can reduce pumping costs by a factor of at least ten. To address the ASE and nonlinear impairments, we are pursuing the use of gain saturation and a staged design of different fiber diameters. We also apply these techniques to fiber amplifiers which incorporate our power amplifier tube in the final stage. The inclusion of our novel tubular-core power amplifier stage should permit a single laser to trigger an array of several PCSS (reducing system cost and mitigating timing jitter).

Relevance to OSPRES Grant Objective: The enhancement in SWaP-C^2 for the laser system enables PCSS systems for viable deployment via: a factor of 40 in pumping cost reduction of each laser; and a factor of *N* in system cost reductions as a single laser could drive *N* (at least 12) PCSS in an array, while also eliminating the optical jitter constraints.

Risks, Payoffs, and Challenges: Optically pumping outside the laser pulse burst time can enhance the ASE; pump costs could be reduced by 40, but ASE in the presence of dispersion and/or nonlinearities could enhance timing jitter thereby limiting steerability. The main challenge for power tube implementation is the entrance optics design.

3.1.2 *Tasks and Milestones / Timeline / Status*

(A) Devise a pre-burst optical pumping scheme by which we can reduce the costs of the laser by a factor of two or more and calculate the resulting increase in ASE. / FEB–JUL 2020 / Completed.

(B) Reduce the ASE via gain saturation. / Oct 2020 / Completed.

(C) Design saturable gain devices which avoid nonlinear damage. / Ongoing.

(D) Calculate and ensure that timing jitter remains less than +/-15 ps with a probability greater than 0.9. / Ongoing.

(E) Demonstrate a cost-reduced fiber laser. / Ongoing.

(E1) **March 2021** Finalize design. / Completed.
(E2) **April 2021** Assemble and test-check seed LD (laser diode)/driver. / Completed.
(E3) **April 2021** Measure power vs current transfer function of seed LD/driver. / Completed.
(E4) **May–July 2021** Measure ASE and jitter of 1064 nm seed LD/driver. / Completed.
(E5) **May–July 2021** Measure ASE and jitter of 1030 nm seed LD/driver. / Completed.
(E6) **June–July 2021** Assemble and test-check pump LDs/drivers. / Completed.
(E7) **June–July 2021** Measure power vs current transfer function of pump LDs/drivers. / Completed.
/ (E8) – (E14) Delayed due to vendor issues (see MAY MSR).
(E8) **September 2021** Splice power combiners to Yb doped preamp fiber. /Completed.
(E9) **September 2021** Connect seed and pumps to power combiners and test-check. / Completed.
(E10) **September–October 2021** Measure gain, ASE and jitter of 1064 nm preamp assembly (forward, backward and bidirectional pumping) as a function of pump power and duty cycle. / Partially complete.
(E11) **September–October 2021** Measure gain, ASE and jitter of 1030 nm preamp assembly (forward, backward and bidirectional pumping) as a function of pump power and duty cycle. / Partially complete.
(E12) **November 2021** Splice power amplifier and its power combiner to best preamp. / Ongoing (delay due to vendor error).
(E13) **November–December 2021** Measure gain, ASE and jitter of entire amp assembly. / Ongoing (delay due to vendor).
(E14) **December 2021** Analyze data and document. / Ongoing (delay due to vendor).

(F) Design a new type of higher power, tubular core fiber amplifier. / Ongoing.

(F1) Apply one high-power tubular amplifier to a system comprised of an array of several (say N) PCSS. For example: N=12 in a 3x4 array (or 4x4 array with corners omitted) N=16

in a 4x4 array, etc.; thereby eliminating jitter constraints and reducing laser system cost by more than a factor of 100 (independent of burst profile). / Ongoing.

3.1.3 *Progress Made Since Last Report*

(F) (C) We again consider smaller diameter (100 micron) optical power amplifiers comprised of a glass tube with a steam filled core (of refractive index = 1.22), which led to a self-focusing imposed power handling limit of roughly 1 GW in the core and 10 MW in the cladding. These limits were achieved in a final stage (or section) of an amplifier which is driven by light input into the core (as well as into the amplifying cladding media). We now shift our attention towards the dynamics of the earlier stages (or sections) wherein the light is only input into the cladding; and we include the effects of gain saturation. Gain saturation (characterized by E_{sat}) is a nonlinear effect which stems from the depletion of pumped ions, to be distinguished from the "fiber nonlinearity" (characterized by γ) that stems from the fact that the index of refraction in glass, $n = n_0 + \gamma I_0$, depends on the optical intensity I_0. Gain saturation was utilized in task (B) to minimize ASE (amplified spontaneous emissions) whereas the fiber nonlinearity creates the self-focusing power limits, and we show in 3.1.4 that the combined effects enhance our understanding of the high-power amplifier dynamics.

(F) (C) The longitudinal "cut-lines" added to the COMSOL simulations (which plot the electric field as a function of the longitudinal distance along the waveguide) previously revealed "hot spots" i.e., resonances which should be minimized to avoid damage from high peak-to-average field strength. We show in 3.1.4 that these arise from the fiber nonlinearity rather than from a reflection at the amplifier's output. Thus, the resonances cannot be mitigated via anti-reflection techniques. We also show that, in the earlier stages of the amplifier, the resonances can be reduced via gain saturation (as E_{sat} can be adjusted via the concentration of the amplifying ions, whereas γ is set by the glass host).

3.1.4 *Technical Results*

(F) (C) In the earlier stages (or sections) of the power amplifier the light is only input into the amplifying glass cladding (and the hollow-core mode to which it is coupled will increase in intensity while it collects scattering from the cladding). We now include the effect of gain saturation, which stems from the depletion of pumped ions so that the gain is reduced from its unperturbed (linear) gain, g_0, to $g_0/(1 + (E/E_{sat})^2)$ where E is the electric field at that point in the waveguide and E_{sat} is a parameter which can be controlled via the ion concentration and the optical pump power. The nonlinear gain saturation is now incorporated into our simulations of the "fiber nonlinearity" (characterized by γ) which creates the self-focusing power limits. To debug the code and determine a reasonable parameter space for numerical convergence and reasonable computation times we first analyzed saturation in the simpler geometry of a rectangular slab waveguide. Fig. 3.1.1 shows the growth of the fundamental mode in which $g_0 = 2.5\ 10^{-6}$ [m^{-1}] results in an amplifier gain of 10 at a distance of 0.2 [m]. The output electric field strength of 2 10^6 [V/m] is small enough that gain saturation is barely perceptible since herein we used $E_{sat} = 10^7$ [V/m].

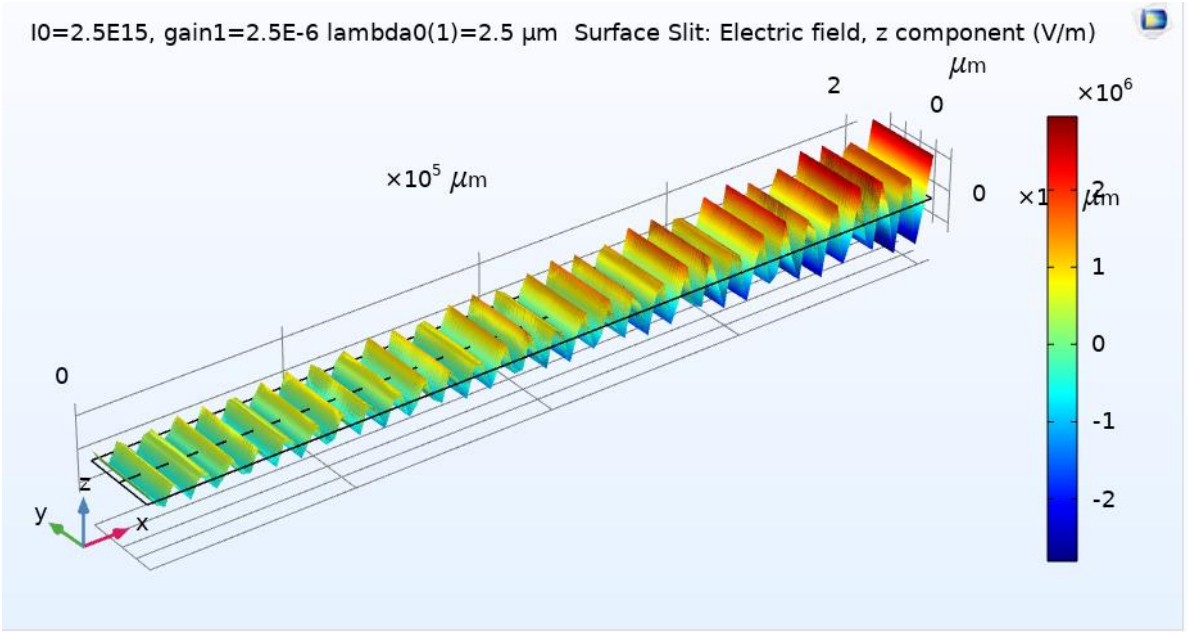

Fig. 3.1.1. Growth of the fundamental mode of a dielectric slab to the onset of saturation.

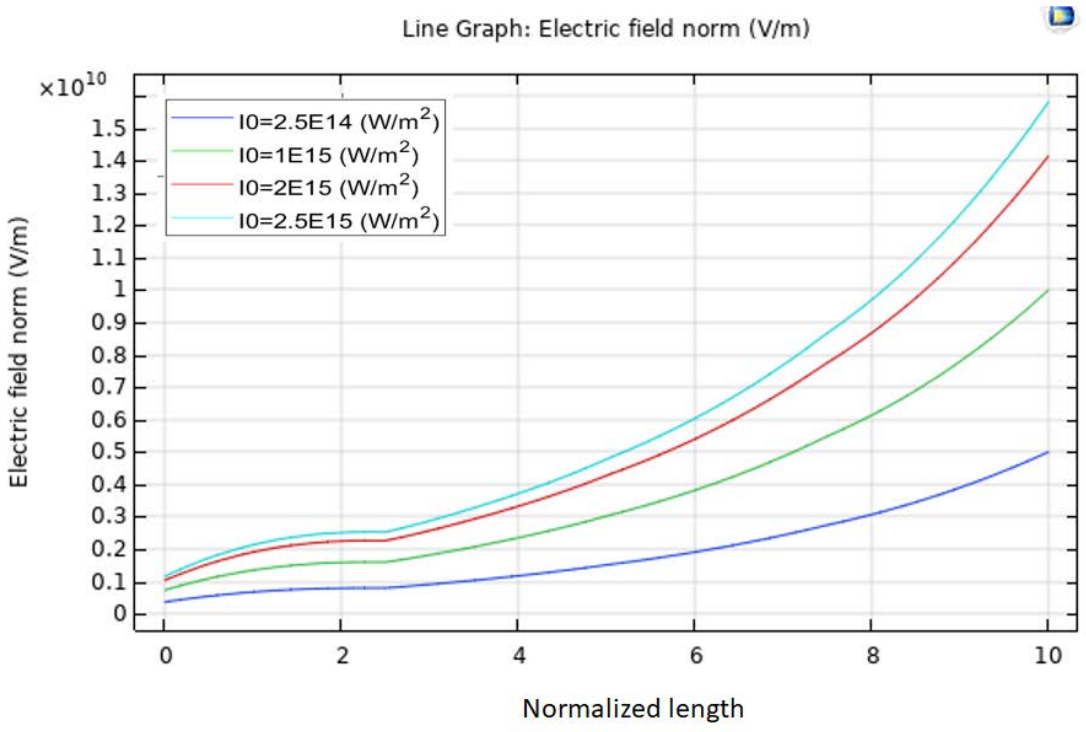

Fig. 3.1.2. Growth of the cladding-mode of the tubular-core amplifier in the absence of nonlinearities ($\gamma = 0$ and $E_{sat} = \infty$).

In the tubular-core amplifier results we normalize all waveguide longitudinal distances, z, such that z = 10 would correspond to an amplifier gain of 10 if the gain remained linear. In Fig. 3.1.2 and Fig. 3.1.3 both nonlinearities are absent ($\gamma = 0$ and $E_{sat} = \infty$). The growth of the mode in the amplifying cladding is seen in Fig. 3.1.2 to closely resemble an anticipated exponential curve, with the exception of a small "gain bump" near the input which must be due to (linear) electromagnetic effects.

The mode coupling provides the growth of the core mode (which has no gain media) in Fig. 3.1.3 and we notice that the linear aspects of the device are responsible for the slight onset of some resonance near z = 2.5 and z = 5, but the rest of the curves are surprisingly smooth. In both Fig. 3.1.2 and Fig. 3.1.3 we used what we refer to as low input intensities, $I_0 \leq 2.5\ 10^{15}$ [W/m], and at these intensities we observe no changes when we "turn on" the fiber nonlinearity (of $\gamma = 4\ 10^{10}$ [cm^2/W] as appropriate for most fiber glasses).

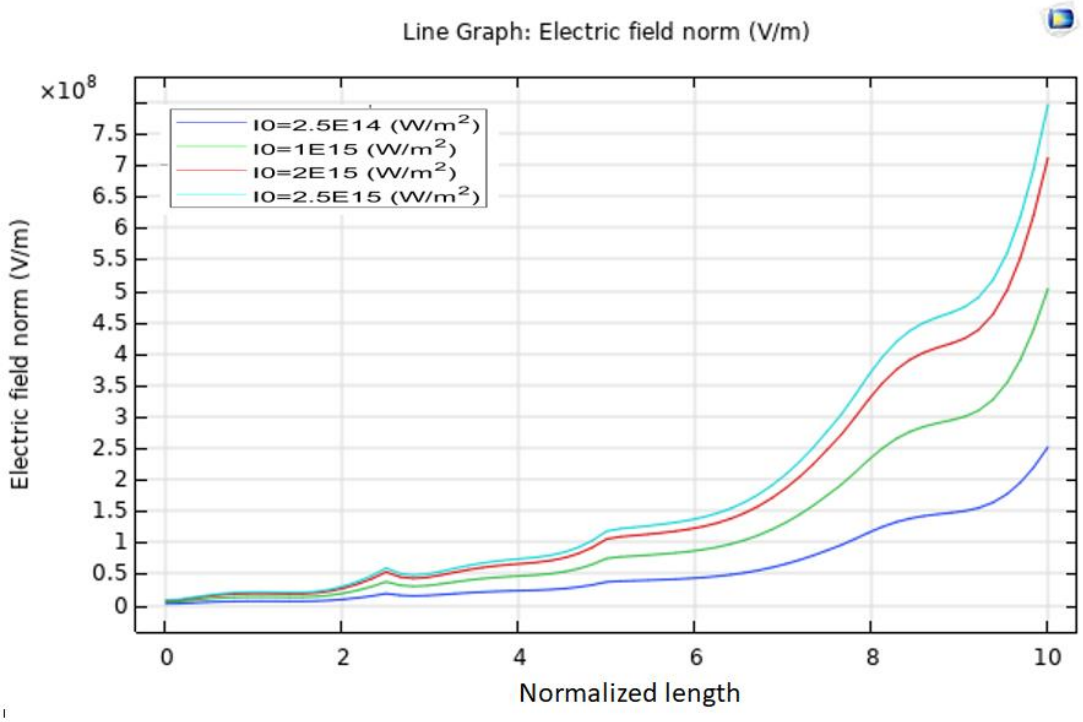

Fig. 3.1.3. Growth of the core-mode of the tubular-core amplifier in the absence of nonlinearities ($\gamma = 0$ and $E_{sat} = \infty$).

When we use higher intensities, such that $I_0 \geq 10^{19}$ [W/m] as in Fig. 3.1.4 and Fig. 3.1.5, the effect of the fiber nonlinearity (at $\gamma = 4\ 10^{10}$ [cm^2/W]) is quite dramatic. The cladding mode in Fig. 3.1.4, and the core mode in Fig. 3.1.5, both exhibit enhanced resonances. We note in particular the sharp resonance near z = 7.5 which was not even noticeable in the case of $\gamma = 0$. Thus, even if their locations are set by linear electromagnetics (possibly originating from reflections) the problem of high peak-to-average "hot spots" is clearly driven by the fiber nonlinearity.

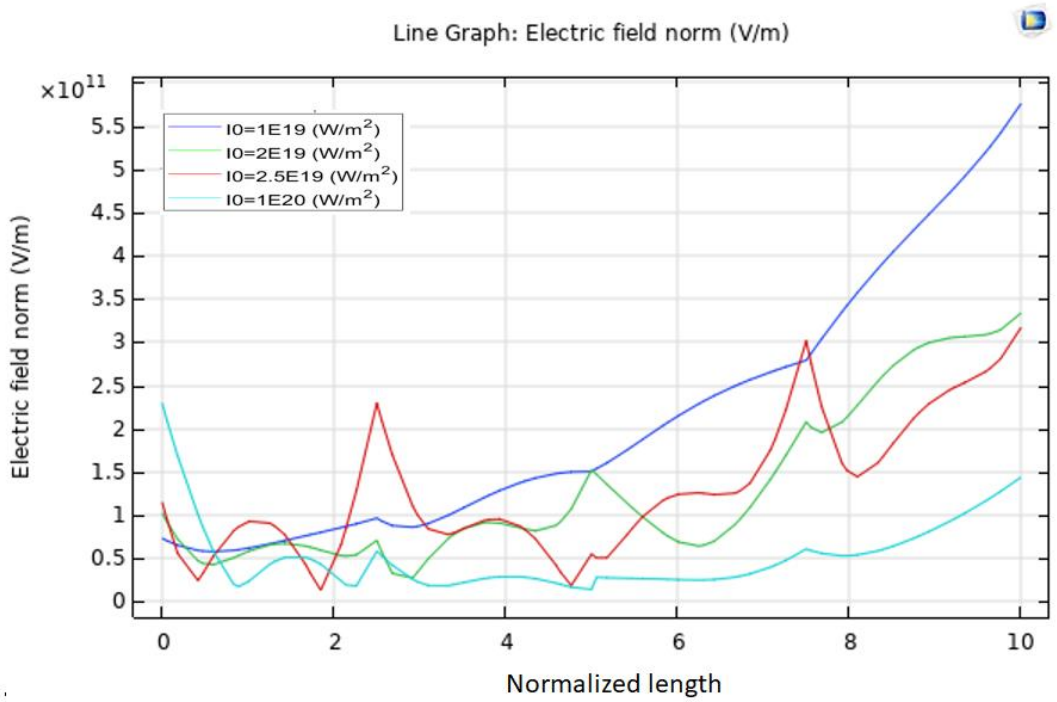

Fig. 3.1.4. Growth of the cladding-mode of the tubular-core amplifier in the presence of the fiber nonlinearity ($\gamma = 4\ 10^{10}$ [cm^2/W]).

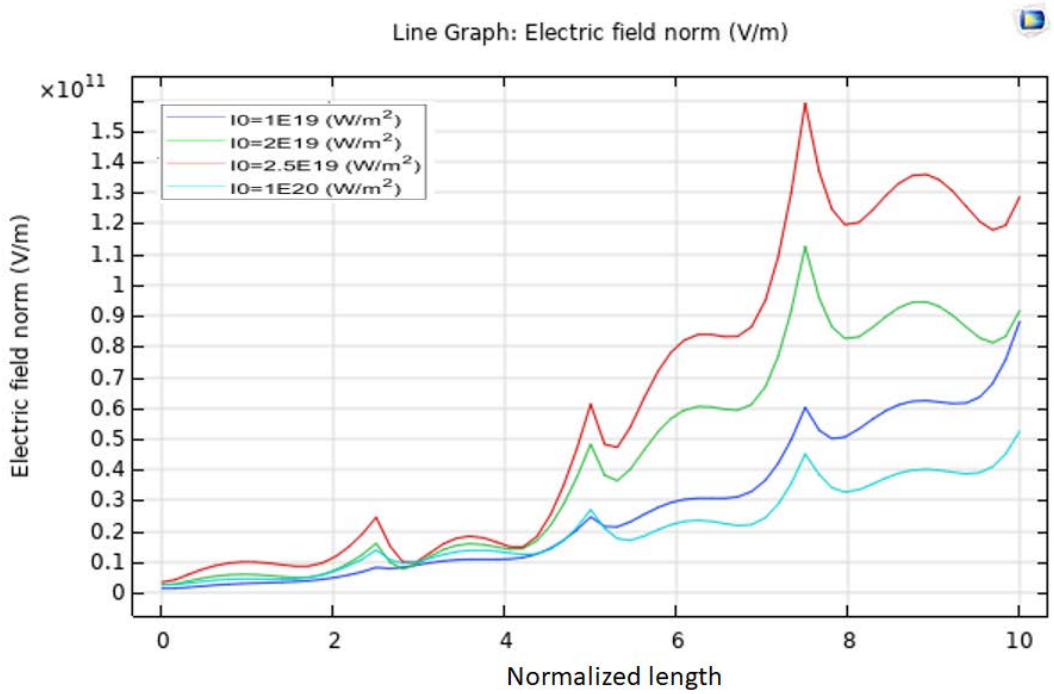

Fig. 3.1.5. Growth of the core-mode of the tubular-core amplifier in the presence of the fiber nonlinearity ($\gamma = 4\ 10^{10}$ [cm^2/W]).

(F) (C) Since the resonances cannot be eliminated via anti-reflection techniques, we pursued their reduction via gain saturation (recalling that E_{sat} can be adjusted by controlling the concentration of the amplifying ions, whereas γ is set by the glass host). We begin by considering the saturable amplifier in the absence of fiber nonlinearity (i.e., $\gamma = 0$) in Fig. 3.1.6 for lower intensities: $I_0 \leq 2.5\ 10^{15}$ [W/m]; and in Fig. 3.1.7 for higher intensities: $I_0 \geq 10^{19}$ [W/m]; where we used $E_{sat} = 10^9$ [V/m].

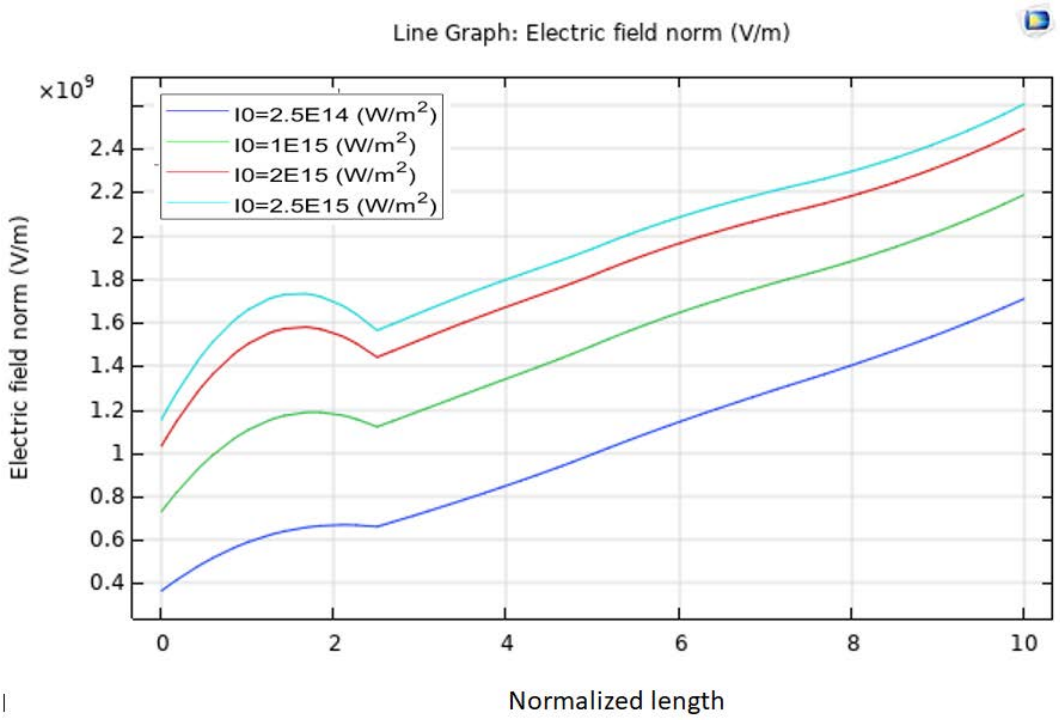

Fig. 3.1.6. Growth of the cladding-mode of the tubular-core amplifier for lower intensities: $I_0 \leq 2.5\ 10^{15}$ [W/m] (at $\gamma = 0, E_{sat} = 10^9$ [V/m]).

We note in Fig. 3.1.6, where the field strengths grow to be on the order of E_{sat}, that gain saturation results in a linear (rather than exponential) increase in z. These are favorable operating points since we can still increase the overall amplifier gain by making it longer. In contrast, for the cases shown in Fig. 3.1.7 where the field strengths are on the order of $100\ E_{sat}$, the gain saturation is so strong that it results in virtually no increased gain with increased amplifier length z (apart from the "gain bump" effect which persists for z < 1).

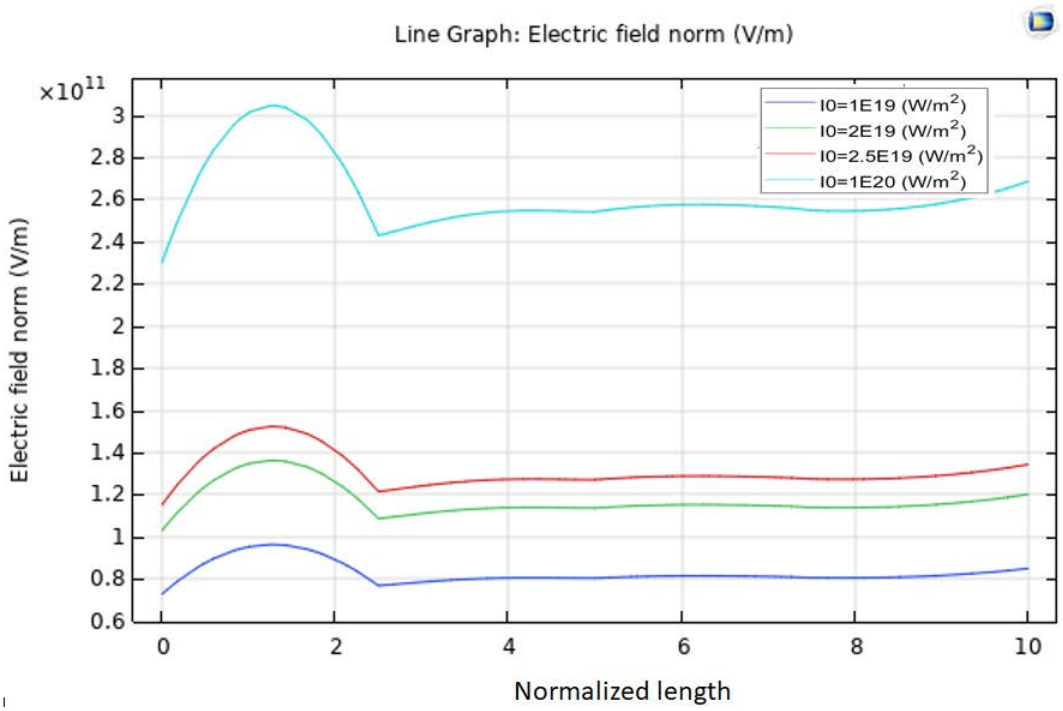

Fig. 3.1.7. Growth of the cladding-mode of the tubular-core amplifier for higher intensities: $I_0 \geq 10^{19}$ [W/m] (at $\gamma = 0, E_{sat} = 10^9$ [V/m]).

Numerical instabilities (not yet understood) often prevent convergence in the simulations when $E_{sat} > 10^9$ [V/m] so at this point we can only comment on what can be achieved in the earlier stages of the amplifier – where the lower intensities: $I_0 \leq 2.5\ 10^{15}$ [W/m] prevail (with $E_{sat} = 10^9$ [V/m]). Therein we found that we can diminish the peak-to-average ratio of a resonance, via gain saturation, from 12 down to 1.54 (an improvement factor of 7.8). Thus, we believe this technique merits further investigation.

3.1.5 *Summary of Significant Findings and Mission Impact*

(A) Our pre-burst optical pumping scheme simulations showed that we can drop the pump power costs by a factor of 40 with pre-burst ASE power levels below the heating level tolerance of 100 μW. UMKC invention disclosure filed 02JUN2020.

(B) For a proposed system gain of 8 million, a linear gain theory predicted the in-burst ASE would be over our heating level spec. by a factor of 3960, but by exploiting the nonlinearity of gain saturation we find that we can suppress the ASE by over 7000. UMKC invention disclosure filed 14SEP2020.

(C) Achieved initial practical device designs that exploit gain saturation, which remained below damage thresholds, via staged designs of different mode diameters NOV2020.

(D) Models of the impact of ASE on timing jitter in the presence of dispersion and/or nonlinearities were established JUL2020.

(E) The design of a proof-of-concept experiment demonstrating a cost-reduced optical pumping scheme was finalized MAR2021.

(F) We made (to our knowledge) the first observation of self-focusing effects that are not determined by beam power alone. We found instead that these can also be controlled via the geometric factors within a waveguide (such as fiber core diameter) MAY2021.

We additionally made (to our knowledge) the first observation that a mode exists in the air within a simple glass tube into which we can couple energy from the mode in the glass. Thus, an amplifier (in the doped and pumped glass) can operate at higher powers JUNE2021.

We found conditions under which 0.25 GW of power can exist in the tube's air-core mode when its glass-cladding mode is at a power level near 0.5 GW JULY2021.

Advancements in the very high-power operating point (tens of GW) of our tubular optical amplifier (and the existence, size and spatial uniformity of its air-core mode) were shown to permit a single laser to trigger an array of several (up to 100) Si-PCSS – reducing the laser system cost and eliminating the optical timing jitter constraint. The symmetry breaking of the scattering from self-focusing in a curved waveguide was shown to enable such AUG2021.

4 Photoconductive Switch Innovation

4.1 Characterizing and Optimizing On-State Resistance in GaN:X PCSS

(Heather Thompson)

4.1.1 *Problem Statement, Approach, and Context*

***Primary Problem*:** Traditionally, RF generation using photoconductive semiconductor switches (PCSS) relies on materials such as silicon (Si) or gallium arsenide (GaAs), due to their availability and low cost; however, as these applications begin to require higher operating frequencies, powers, and temperatures, with the same or reduced system form-factor, the theoretical operating limits of these materials are being reached.

***Solution Space*:** By exploiting the 3.4 eV bandgap, 1000 cm^2/Vs electron mobility, and thermal properties of GaN, it is possible to realize pulsed-power applications requiring up to a 5 MV/cm critical field, high-frequency operation, and ~400 °C operating temperature, respectively.

Sub-Problem: One of the most important problems in minimizing conduction losses, maximizing efficiency, and reducing thermal issues in compensated, semi-insulating GaN:X (i.e., GaN:X with X=C, Fe…) PCSS-based systems is achieving <1 Ω on-state resistance by optimizing the modifiable parameters of GaN:X at the material, device, and system levels, while still maintaining quick switch turn-off time and low turn-off losses.

***State-of-the-Art (SOTA*):** PCSS-based RF generation systems using Si, SiC, or GaAs can achieve MW-range output power, ones-of-gigawatts frequency content, and electrical efficiency of ~60% that require increased laser energies and device size to reach maximum efficiency and necessary operating power limits, respectively.

***Deficiency in the SOTA*:** Si-, SiC-, and GaAs-based PCSS require ones-of-mJ of incident laser energy to achieve <1 Ω on-state resistance, leading to increased incident laser requirements, increased heating in devices, and devices that are ones-of-cm^2 in area for the necessary peak power and operating temperatures.

***Solution Proposed*:** Use simulation and available experimental results, from the literature and collected results at UMKC, to optimize the variable parameters of GaN:X PCSS to achieve <1 Ω on-state resistance with increased electrical and optical efficiency while maintaining a quick switch turn-off time and low turn-off losses.

Risks, Payoffs, and Challenges:

***Challenges*:** The high cost of material leads to a limited number of devices available for experimental testing and analysis, requiring a majority of the optimization studies to be performed using simulation software (COMSOL and TCAD).

***Risks*:** Simulation results may differ from experimental results for certain PCSS parameters due to particular photogeneration and recombination parameters not being included in models along with non-ideal, real-world experiments requiring additions such as encapsulation material or other changes not fully addressed in simulation.

***Payoffs*:** By minimizing the conduction losses in GaN PCSS, a compact, tunable RF source can be realized with increased efficiency and SWAP-C^2 capabilities.

4.1.2 Tasks and Milestones / Timeline / Status

(A) Milestone – Determine material, device, and system parameters that affect on-state resistance and which of these can be best leveraged to reduce on-state losses and heating.

1. Task – Literature study of photoelectric on-state resistance to understand how this parameter can be optimized to reduce conduction and on-state losses during PCSS operation *[ongoing].*
2. Task – Literature review of on-state resistance studies performed using GaN-based photoelectric devices to determine areas to further study *[ongoing].*
3. Task – Determine project milestones, tasks, and timeline for optimizing on-state resistance in GaN PCSS *[ongoing]*.

(B) Milestone – Build model of GaN PCSS in TCAD and COMSOL to begin simulation studies *[ongoing].*

1. Task – Build simple, working GaN PCSS model that can be subsequently altered for more complex analysis of on-state resistance *[Complete]*.
2. Task – Compare simulation results with available experimental results to determine validity of models using COMSOL *[MARCH 22]*.
3. Task – Set up parametric sweep studies in COMSOL *[APRIL 22]*.
4. Task – Build a working GaN PCSS model in TCAD to determine which modeling software will provide accurate, efficient results *[MARCH 22]*.
5. Task – Determine parameters that can be altered using TCAD and design studies using this program *[MARCH 22]*.

(C) Milestone – Determine device level characteristics that can be altered in simulation allowing for optimization of on-state resistance and efficiency of GaN:C PCSS and complete study on leveraging these parameters.

(D) Milestone – Determine circuit and incident photon source characteristics to be studied using simulation towards minimizing on-state resistance in GaN:C PCSS.

(E) Completion of manuscript on optimizing on-state resistance in GaN:C PCSS *[Ongoing]*

4.1.3 *Progress Made Since Last Report*

(A) Our literature search focused on minimizing on-state resistance in GaAs PCSS devices found that this was limited by shallow absorption depth. To overcome this limitation, Liu et al [1] incorporated an array of “nano-fins” within the gap of the device to increase the effective absorption depth, thus increasing the active volume in the device. A similar approach will be used in future work towards minimizing on-state resistance in GaN:C PCSS without increasing incident laser energy.

(B) Work continued towards understanding how different device and material parameters affect on-state resistance through building a model for GaN:C PCSS in Silvaco TCAD, but error mitigation is still needed in the model and solution sections of the simulation before it is fully operational.

4.1.4 *Technical Results.*

(A) Literature shows significant work towards maximizing device efficiency through minimizing on-state resistance in GaAs PCSS devices, which is useful for finding ways of doing the same in GaN:C PCSS devices without increasing laser energy, which would increase the cost and size of the overall system. In Liu et. al. (2021)[1] it was found that minimizing on-state resistance in GaAs PCSS was limited due to the active device volume being restricted from the shallow absorption depth (~0.14 μm at 532 nm incident photon wavelength). By adding in a nanostructure wall array of "nano-fins" in the gap length of the device (Figure 4.1.1), or 3D grooves in the surface that are less than one half of the size of the incident photon wavelength to avoid scattering, photon absorption occurs on the top and side surfaces of these fins, essentially increasing the active area cross section and improving photocurrent while reducing trigger fluence (incident energy per area needed for device activation). Shown in Figure 4.1.2, photocurrent in linear mode operation was increased from 1.9 μA to 106 μA for a trigger fluence of 3.8 mW/cm^2 with the addition of these fins. This device geometry alteration could be replicated using simulation to determine the extent of on-state resistance minimization possibly achieved in GaN PCSS using a similar method.

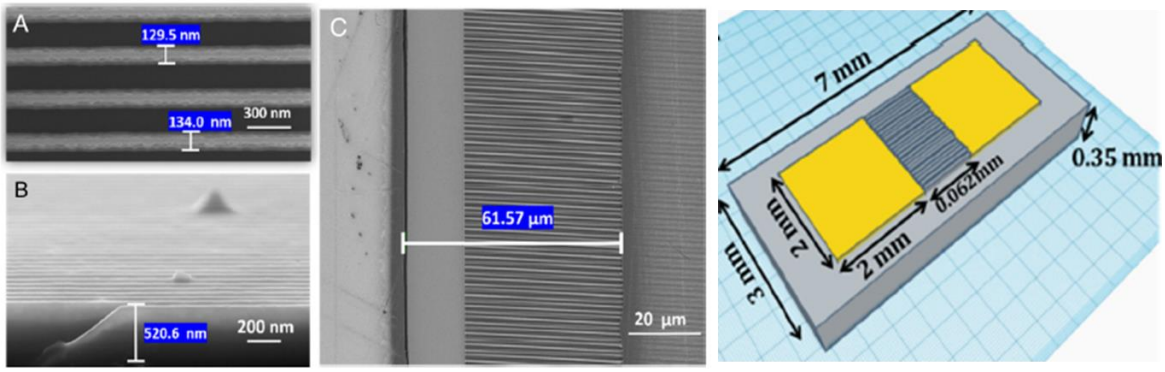

Figure 4.1.1: (Left) SEM images of nanostructure wall array on GaAs PCSS for increasing effective penetration depth and active volume to reduce on-state resistance with (A) being the top view, (B) the side view, and (C) a zoomed-out image of the nano-wall array. (Right) Illustration of GaAs PCSS device geometry with nanostructure wall array placement seen in the gap length of the device.[1]

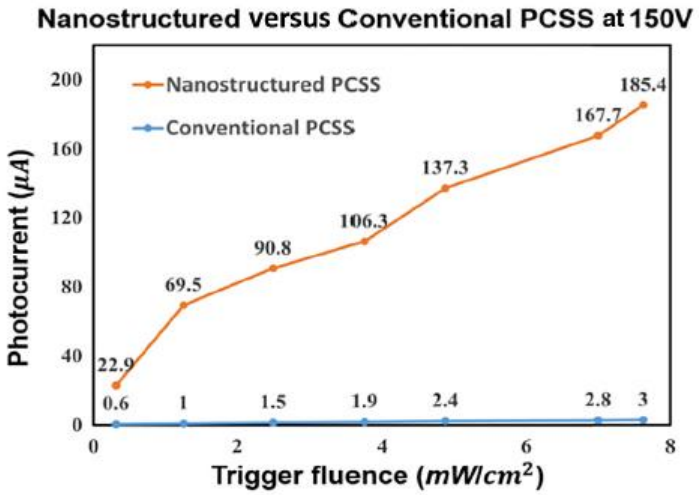

Figure 4.1.2: Photocurrent as a function of incident trigger fluence (energy per area) for a conventional and nanostructured GaAs PCSS showing the increase in photocurrent generated using the nanostructure addition to the devices [1].

(B) Towards using simulation to understand how different device and material parameters affect on-state resistance in GaN:C PCSS, work continued on building a model in Silvaco TCAD with the mesh and device geometry being built, but error mitigation is being done for the model and solution specification sections of the simulation.

4.1.5 *Summary of Significant Findings and Mission Impact*

(A) A preliminary literature study of the on-state resistance of opto-electric devices began to find the parameters that affect the on-state resistance of GaN PCSS and similar devices of differing materials which will lead to the determination of what parameters can be manipulated to optimize on-state resistance in GaN PCSS, leading to a material option that provides increased efficiency and SWAP-C[2] capabilities of a PCSS-based RF generation system.

During literature review, it was found that publications in this area typically focus on vertical GaN-based PCSS devices, and this has led to the conclusion that assumptions used in evaluating vertical devices need to be studied to determine their validity in lateral devices.

Due to the minimal jitter operation and increased device lifespan, focus will be restricted to linear mode PCSS operation, which limits devices to lateral geometries. Focus will also be placed on intrinsic carrier activation due to increased optical efficiency over extrinsic activation.

GaN and GaAs-based electrically gated devices have had more extensive work done towards minimizing and optimizing on-state resistance, including identifying common

sources of loss and current collapse and utilizing clamping circuit altered to maximize efficiency.

Future work to consider for increasing optical efficiency in GaN PCSS, based off of GaAs PCSS work, using periodic groves formed in the top of the device to take advantage of total reflection theory to decrease on-state resistance without needing to increase energy of the photon source.

Another alteration found in GaAs PCSS literature, was the addition of nanostructure wall array in the active area (gap length) of the device leading to an increased active volume in the device and overcoming on-state resistance minimization limitations due to shallow absorption depth of the photon source. By utilizing an array with fins >1/2 the incident laser wavelength, to prevent scattering, photocurrent was increased from 1.9 μA to 106 μA for a trigger fluence of 3.8 mW/cm^2. This device alteration can be replicated in simulation of GaN:C PCSS devices to determine the increase in efficiency that could be achieved through increasing the effective volume of the active device area.

(B) A simple working GaN:C PCSS model was created using COMSOL, which will be used towards parametric studies of optimization of on-state resistance.

Work also began toward building a model of GaN:C PCSS using Silvaco TCAD, as this software has been used for similar OSPRES research and offers additional capabilities to COMSOL.

The device geometry and meshing have been built in TCAD, and errors are being fixed in the model and solution specification sections of the simulation.

(C) Work towards a manuscript based on optimizing on-state resistance in GaN:C PCSS has been started with the first version of the introduction written and currently being edited.

4.1.6 References

[1] R. Liu, A. Shang, C.-J. Chen, Y. G. Lee, and S. Yin, “Nanostructure Enabled Lower On-State Resistance and Longer Lock-on Time GaAs Photoconductive Semiconductor Switches,” Opt. Letters, vol. 46, no. 4, pp. 825–828, 2021.

5 Drift-Step-Recovery-Diode-Based Source Alternatives

5.1 Drift-Step Recovery Diode and Pulse Shaping Device Optimization

(Jay Eifler)

5.1.1 *Problem Statement, Approach, and Context*

Primary Problem: Drift-step recovery diodes (DSRDs) and DSRD-based pulsed power systems are competitive with PCSS-based systems for HPM cUAS, with the benefit of not requiring a laser. Maximizing peak power while maintaining characteristic ns-order DSRD rise times requires optimization of the DSRD device design and pulser. Other considerations are for compactness, low-jitter, cooling required, and additional pulse-sharpening device within the pulse shaping head circuit. Additional goals for pulse repetition frequency are also to be satisfied for various applications.

Solution Space: By altering DSRD device parameters (geometry, doping, irradiation), optimize single-die and stack designs for peak power and risetime within various inductive pulser circuit topologies. Also optimize the pulse sharpening device (PSD) within the pulse shaping head circuit.

Sub-Problem 1: TCAD and SPICE models of the DSRD are inaccurate and must be improved. PSD models have not been developed.

Sub-Problem 2: Inductive pulser designs are complicated by the DSRD (and PSD) parameter variability. Use TCAD and/or SPICE models to account for variability and improve pulser design.

State-of-the-Art (SOTA): MW peak power and ns-order risetimes have been achieved in DSRD-based pulsed-power systems employing DSRD stacks for higher voltage holding and parallel lines of DSRD to increase current. PSD have sharpened DSRD pulses to 100 ps-order.

Deficiency in the SOTA: A lack of accurate TCAD and SPICE models make design of DSRD and DSRD-based inductive pulser circuit topologies (with or without PSDs) difficult to the level of tens of MW of peak power while maintaining ns-order risetime (or sharpened 100 ps-order). In addition, DSRD (and PSD) fabrication variabilities further complicate pulser design.

Solution Proposed: Develop further modeling capabilities in TCAD and SPICE for DSRD and DSRD-based inductive pulser circuit topologies to optimize DSRD and inductive pulser designs, especially for maximum peak power and minimum risetime, but also for low-jitter, reduced cooling, and compactness. Additionally, optimize pulser with PSD and pulse shaping head circuit.

Relevance to OSPRES Grant Objective: DSRD-based systems eliminate laser requirements necessary for PCSSs and are competitive in terms of thermal requirements and peak power. With sharpening, the DSRD-based systems can produce comparable risetimes. The SWaPC^2 cooling requirements of HPM cUAS systems can be solved with DSRD-based pulsed power systems, and low-jitter DSRD-based systems can be used for beam-steering in phased-arrays.

Risks, Payoffs, and Challenges: DSRD must be arrayed and staged to increase current since DSRD are limited in their ability to operate at high current densities. DSRD and PSD must also be stacked to operate at high voltages necessary for high peak power and maintain low risetimes. The stacking methods can damage dies and produce variable results in risetime and DSRD diffused doping profiles can be difficult to achieve and may require epitaxial methods. SPICE device models for DSRD are unavailable and must be developed, and questions remain about TCAD limitations for DSRD and PSD modeling.

5.1.2 Tasks and Milestones / Timeline / Status

(A) Milestone – Develop TCAD and SPICE models of the DSRD and MOSFET, respectively, that match experimental values of both the diode and circuit within 5% accuracy [*Estimated completion by AUG21*].

1. Task – Develop baseline DSRD model in TCAD [*completed JAN–APR21*];
2. Task – Develop SPICE model of DSRD within LTSPICE and SmartSpice, an automated model parameter fitting procedure, and LTSPICE and SmartSpice parameters for DSRD inventory [*Estimated completion AUG-NOV 2021 (continued effort as new DSRD arrive)*];
3. Task – Develop SPICE model of MOSFET within Silvaco [*JUL–SEP21*];
4. Task – Compare results of models developed in TCAD to the simulation values achieved using LTSPICE and experimentally (see Section 4.5) [*JUL–SEP21*];
5. Task – Incorporate parasitic capacitance, inductance, and resistance models for both single die and DSRD diode stacks (multiple dies in series) as well as for the DSRD-based pulser circuits [*discontinued after MAR–JUN21*];

(B) Milestone – Optimal characteristics of epitaxially-grown DSRD pinpointed from parametric study which produce the maximum waveform fidelity characteristics (e.g., maximum peak voltage, shortest risetime, highest dV/dt) [*Estimated completion by AUG21*].

1. Task – Determine carrier lifetime effect on risetime [*completed FEB–APR21*];
2. Task – Determine effect of including avalanche modeling on DSRD performance [*completed FEB–MAY21*];
3. Task – Determine effect of the width of outer edge contact on current density and breakdown in device [*discontinued after MAR–MAY21*];
4. Task – Model TCAD process in Silvaco Athena and Victory Process for DSRD diffused and epitaxial processes (and pulse sharpening devices) used for DSRD fabrication and DSRD device modeling [*discontinued after MAR–JUN21*];
5. Task – Determine optimal doping profile for Semiconductor Power Technologies (SPT) DSRD epitaxial designs [*completed MAY–JUL21*];
6. Task – Determine best doping profile from fabricated and optimal conceptual designs by comparing performance in the 2x2 DSRD pulser [***completed JUL21***];

7. Task – Complete DSRD performance study on epitaxial doping profile (n-side) variation manufactured by SPT in conjunction with LSRL [***completed JUL21***];
8. Task – Complete gain study for DSRD stack height and gain staging design [***completed JUL21***];
9. Task – Verify accuracy of TCAD simulations by comparing to experiment for DSRD-based pulser circuit topologies [*JUL–AUG21*];
10. Task – Perform first semiconductor opening switch (SOS) TCAD simulations for DSRD vs SOS mode of operation [SEP21];

(C) Milestone – Pulse sharpening devices developed within TCAD which improve the risetime and peak voltage of the IES pulse generator developed in Section 4.5 [***transitioned to Section 4.7 JUL21***].

1. Task – Develop preliminary pulse sharpening devices (PSD) models within TCAD [*discontinued after DEC20*];
2. Task – Develop standard PSD models within TCAD to reproduce results from published work [*discontinued APR–JUN20*];
3. Task – PSD simulated with DSRD 3-stack for more complete DSRD-based system modeling excluding only the primary switch model [*APR–JUN20*];
4. Task – Determine current carrying capacity of PSD and DSRD stacks [*discontinued MAR–JUN21*];

5.1.3 *Progress Made Since Last Report*

(A.2) SPICE Diode Model Parameter Development and Generation

Generation of LTSPICE Diode Parameters

Parameter extraction has been on hold awaiting more Gen2.2 diode testing and diode model assessment. Gen2.2 data has been received in part.

Development of Series Resistance (RS) Diode Parameter

371A semiconductor analyzer measurement data did not show a linear series resistance region at higher voltages and currents as seen in power diode and DSRD forward IV. Heating and distortion of the forward IV curve is suspected and thermo-couple and heat sink experiments are in planning. Once an accurate experimental series resistance is measured it can be included in SPICE model parameterizations.

New Diode Models for SPICE Simulation and Diode Parameter Development

Device modeling using behavioral, Verilog-A and built-in device models was undertaken in SmartSpice. The standard diode model was compared between LTSPICE and SmartSpice since there are differences. The main focus has been on using the recovery model within the CMC diode model which has been assessed only for the IV and CV correctly and recovery model testing is forthcoming. Diode behavioral modeling suffers from numerical problems and is typical used only for adding recovery models to the built-in diode models. Verilog-A modeling has begun and the industry standard CMC

(Compact Modeling Committee) diode Verilog-A model has been successfully used. Future DSRD models can now incorporate theoretical model equations directly into the Verilog-A code and SmartSpice simulations. Parameter extraction used two new techniques: python curve fitting and the SmartSpice optimizer. The python curve fitting is limited to model equations outside of circuit simulation but was otherwise successful. SmartSpice optimization should prove the best method but is still under study to reproduce consistently good fits as brute force or the python curve fits have been capable of.

5.1.4 *Technical Results*

(A.2) SPICE Diode Model Parameter Development and Generation

Generation of LTSPICE Diode Parameters

Parameter development was put on hold while Gen2.2 data collection and the new variability study are underway. New diode models are also being assessed for which parameter fitting is also necessary. Two new methods of parameter fitting were tested: python curve fitting and SmartSpice optimizer.

The python curve fitting tool was used to fit IS, N and IKF of the forward IV parameters and produced fits equally as good and very close to the brute force method. Including RS in the python curve fitting was not possible since multiple equations must be solved as is done in the circuit simulator. If RS could be included, the python curve fitting tool can be used to fit the forward IV in the standard diode model as accurately and more quickly than the brute force method and python fitting can then be used in subsequent CV curve fitting.

The SmartSpice optimizer was also used for curve fitting. Unfortunately, the optimizer was not successful yet in producing fits as good as the brute force method (and python optimizer for IS, N and IKF only). With study and practice, the optimizer should perform as well as the python curve fitting since the same method is used in both with SmartSpice but also employing circuit simulation. Ultimately, the optimizer will be necessary when a large number of parameters are to be fit and require circuit simulation.

In trying to replicate curve fitting for LTSPICE in SmartSpice a discrepancy between the standard diode models was found: the IKF results are different likely due to different modeling equations. LTSPICE has not documented the details of their diode model but appears to use the PSPICE IKF equation and HSPICE and SmartSpice use a different IKF modeling equation so the parameter fits are different. This highlights the careful checks and comparisons that must be done when using device models within SPICE.

Development of the Series Resistance Forward IV Diode Parameter

The forward IV from last report (Grant Report January 2022) for EG1608 was fitted for the forward IV parameters within the standard diode model. Fairly good fits were obtained by increasing IS and N to fit the curve in the higher voltage and current region. It is likely the present fits can be improved slightly but it will not be possible within the standard diode model to fit both the picoammeter low voltage/current data and the 371A higher voltage/current data. The inability to fit the curves could be due to temperature distortions

in the curve since the linear series resistance region does not occur (without the linear region RS cannot be approximately set to the measured series resistance). As well, other diode models and custom diode models could be employed to fit the curve including a tabulated diode model that goes directly from the experimental curves.

A thermocouple to measure the temperature of the diode and/or a heat sink are to be employed in measuring the forward IV on the 371A semiconductor analyzer. If the diodes are found to increase significantly enough in temperature the heat sink may allow the dissipation of enough heat to measure the correct constant-temperature forward IV. Once the temperature distortions are verified or disproven, data must be extracted from the 371A using an automated method for a large number of measurements to be taken (371A has antiquated memory system).

In Figure 5.1.1 is shown a forward IV fit in the standard diode model using four parameters: IS, N, IKF and RS. Fits for IS and N or adding either IKF or RS as a third parameter were also done and all resulted in about the same best fit. The picoammeter (gray) and 371A (blue) experimental result are shown in the figure. The (orange, IS=0.8) result fits all the available 371A data from 5.1 V to 26.65 V while the (yellow, IS=0.1) result only fits 371A data less than 15 V (since forward pumping voltage is generally below this value). The fit for 15 V and less (yellow) is closer to the picoammeter data (gray) but it was not possible to fit both the picoammeter and 371A data with any accuracy. Other models can be used to fit this data, if necessary, but the data may also be temperature distorted and explains why excellent fits are not obtainable.

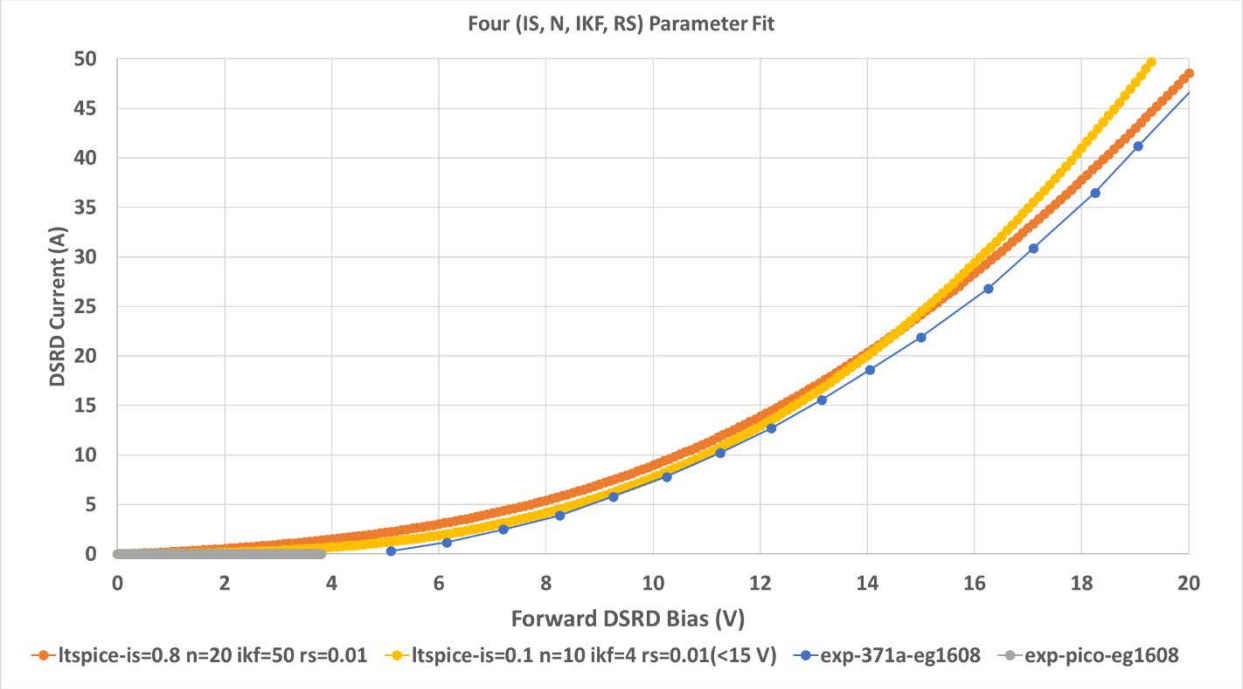

Figure 5.1.1. Fitted LTSPICE forward IV compared to experimental forward IV curves. The (orange, IS=0.8) result is fitted over all 371A data, while the (yellow, IS=0.1) result is only fit for 371A less than 15 V.

New Diode Models for SPICE Simulation and Diode Parameter Development

SmartSpice has not yet been evaluated for DSRD pulser performance. The standard diode model should be tested first between LTSPICE and Smartspice. Smartspice may be more accurate and have better convergence capabilities that could affect pulser simulations, especially for the 2x2 and 4x2 pulser designs since variations within LTSPICE were found likely to due with convergence issues.

The main focus in device modeling in this report has been in comparing the standard diode models and fitting between LTSPICE and SmartSpice to transfer simulations to SmartSpice with confidence. The other main focus has been in setting up the CMC diode model for simulation within SmartSpice since it has an improved recovery model.

The CMC diode model has been tested for IV and CV but has not yet been successful used for reverse recovery simulations. The forward IV has a parameter (VMAX but set by IMAX) in the CMC diode model to set when the forward IV goes from exponential to linear behavior. This method of controlling the exponential behavior of the diode did not allow for the 371A forward IV data to be fit as with the standard diode model (measured curve may be distorted). The forward CV equation is also different and may affect the recovery simulations. Testing on the CMC diode modeling in reverse recovery is forthcoming. Issues with the HiSIM have also prevented its use in reverse recovery testing and it also forthcoming (in communication with Silvaco).

In addition to built-in diode models in SmartSpice, behavioral and Verilog-A device models were tested. An equivalent circuit model was also tested within LTSPICE for the DSRD. The equivalent circuit model is best implemented in Verilog-A (not done yet) rather than a behavioral model. The model only served to implement a recovery model with voltage-controlled switches better handled within Verilog-A code models. The equivalent circuit model of Kyuregan will not capture DSRD operation as well as the newer diode models within SmartSpice that have recovery models (HiSim and CMC).

A purely behavioral diode model was tested with idea of using a tabulated diode that is directly fit to the experimental curves (with the addition of smoothing functions). However, the basic diode modeling equations failed in transient reverse recovery testing for the behavioral diode model but not in the built-in standard diode model using the same equations. This is due to the difficulty of modeling the diode due to its exponential nature. Smoothing functions and safe exponential evaluation are employed in the built-in diode models which are available in coded form within the Verilog-A CMC diode model and online resources. Implementing the basic diode equations directly in Verilog-A also failed in transient reverse recovering testing due to the lack of safe exponential evaluation preventing numerical over- and underflows. The basic diode equations were successful for IV and CV within the behavioral and Verilog-A forms. Published behavioral models use the built-in standard diode equation as part of a behavioral modeling of the recovery effects. A tabulated diode model can be made within Verilog-A but will still require smoothing and safe exponential evaluation for successful transient simulation for reverse recovery or otherwise.

The CMC diode model was obtained from the Si2 organization in Verilog-A which gives access to the coded form of the model details not available in the manuals. This code

was intended to be modified for model development by the semiconductor industry. The Verilog-A CMC diode model can be used directly to model the DSRD with its improved recovery model or modified in its diode equations to reflect theoretical, experimental and TCAD-based results on the DSRD operation and pulser performance.

The reading of the CMC diode manuals and code has begun and parameters have been adjusted not known (yet) to be available in the built-in model. The main goal is to assess the CMC diode model for its ability to model the recovery effects of the DSRD in reverse recovery and DSRD pulser tests.

5.1.5 *Summary of Significant Findings and Mission Impact*

DSRD TCAD simulation started by replicating published TCAD DSRD results and then simulating devices similar with actual in-house DSRD. The variation of the sinewave pulse voltage input magnitude and period on DSRD charge storage were collected. Charge storage timing (when the diode empties charge stored from forward pulsing) of ~50% was achievable with sufficiently long voltage input period which is necessary for maximum reverse current cutoff.

DSRD stacks, as opposed to individual die DSRD, were simulated showing reduced risetime from single die to 5-stacked DSRDs consistent with published and earlier in-house data. Series resistance to model metal resistance between DSRD in stacks and doping variability in stacks was also modeled in TCAD showing metal resistance must be large to have an impact on peak voltage and risetime and that doping variations proportionally effect risetime.

(A.1) Accurate DSRD TCAD models have been developed that include both carrier-carrier scattering and Selberherr breakdown and are suitable for DSRD operation below the dynamic breakdown threshold. Peak voltage and risetime were limited by the breakdown model and more closely match experimental pulse data.

(A.2) A new DSRD LTSPICE model has been developed following the method used for developing a TCAD SPICE MOSFET model and by matching too experimental standard diode tests. The forward I-V and reverse C-V have been well matched using a 7-diode model for a 7-stack DSRD, as opposed to using only a 1-diode model for all DSRD stack heights. The reverse I-V and forward C-V are generally more problematic to fit to and proved to be so. More research and effort will be necessary to improve these matches and understand the impact on pulser simulation. The reverse recovery experiments have also been well matched (even for a single transit time over different reverse recovery testing voltages) and complete the matching of all the standard diode tests. New diodes are arriving and being tested and parameterized and tested in simulation and compared with experiment. Pulser performance has been difficult to assess due to the experimental data gathered thus far. The new DSRD LTSPICE model will also enable improvements in the TCAD SPICE MOSFET model. Overall, the new DSRD model represents a vast improvement over the previous model but has yet to include breakdown effects possible in the TCAD DSRD model and therefore breakdown limits of DSRD operation. A new automated fitting procedure now allows the model parameters to be more closely and quickly fit, has been used to

fit various batches of different DSRD, and has used averaged curves (for improved measurement) when available. New SmartSpice diode models have arrived and can provide for improved reverse IV, breakdown and recovery modeling, as well as, SmartSpice may improve the accuracy and convergence of pulser simulations. A 371A Tektronix semiconductor analyzer has been acquired and used to measure higher voltage and current forward IV (necessary for RS parameter development in SPICE models). Measurements for reverse IV and breakdown with the 371A are forthcoming. Temperature distortions may exist in the 371A forward IV and are under study. Verilog-A device modeling capabilities are now being used that will allow the CMC diode model to be extended and modified for DSRD modeling by coding the correct modeling equations. The standard diode model has been compared between LTSPICE and SmartSpice and is different. The CMC diode model is nearing testing of its recovery modeling capabilities in reverse recovery and DSRD pulser simulations.

(A.3) Work on TCAD SPICE MOSFET models has been done for the primary switch model (MOSFET) with conversion of the code to TCAD SPICE being partly completed to allow for modeling the complete DSRD-based pulser system (except driver). However, the conversion to TCAD of the MOSFET primary switch model, developed by CREE, to TCAD SPICE is complicated by having to develop custom behavioral models in TCAD SPICE which would be high-risk. Instead, a published model usable in TCAD SPICE was implemented and fit to the datasheet and then tested in a DSRD pulser simulation. The new MOSFET SPICE model usable in TCAD showed improvement in not having a first output pulse peak that was higher. This higher pulse had occurred in the TCAD MOSFET model (not SPICE model) and had not occurred in the voltage-controlled resistor MOSFET model (inaccurate model). Further refinement and testing of the new MOSFET SPICE model for use in TCAD has been more closely fit with the Cree LTSPICE model and compared to the Cree datasheet. The model can also be adapted to a new MOSFET in use within current DSRD pulsers. Further fitting can still be accomplished and matching both the Cree datasheet and LTSPICE model for gate charge and switching characteristics can be completed with more research into the test circuits used which are commonly not well explained in datasheets.

(A.4) LTSPICE, TCAD and experiment have been compared for the single bar pulser using a 7-stack DSRD, however there is some discrepancy for these experiments with earlier experiments (which the LTSPICE and TCAD simulations match better with) most likely due to the variability in DSRD and some to the new DSRD switch integration used for ease of switching out DSRD of various stack heights and combinations. As more experimental data is acquired for the pulsers the comparisons with simulation will yield more useful results. The 2x2 DSRD pulsers have been compared to TCAD simulation incorporating the latest TCAD SPICE MOSFET models showing some similarities in predicted peak voltage and risetime, but the most significant result is the matching of the experimental optimum trigger duration of 340 ns with TCAD results. LTSPICE simulations have been performed with the new DSRD LTSPICE models and show the standard diode model used can match experimental peak voltages and risetimes but only by adjusting mainly

the CJO parameter. Without adjustment there is considerable error in simulated results. Better diode models exist that incorporate impact ionization effects and recovery time modeling the latter of which circumvents CJO adjustment. With further experiments and simulation refinement it is expected that the models will be predictive of experiment within the quality of the experimental data and models used. Some inconsistency between computers for LTSPICE, having to do most likely with convergence in the pulser simulations, is being studied for the 2x2 and 4x2 DSRD-based pulsers.

(B.1) DSRD risetime performance was collected from TCAD simulations for variable carrier lifetime. Changes in lifetime had no significant effect on risetime other than the output pulse starting earlier.

(B.2) DSRD peak voltage and risetime were simulated in TCAD to include avalanche modeling or not. TCAD avalanche models limited peak voltage and risetime at the load over a range of voltage input magnitudes. A TCAD parameter study for DSRD stack height and DSRD area for several doping profiles with and without avalanche modeling was performed (Spring 2021 UMKC OSPRES Grant Review and Technical Exchange). The avalanche model and model parameters were also modified to account for dynamic breakdown rather than static and then compared to the no avalanche case and experimental data. From the improved avalanche modeling and TCAD parameter study, the optimal area of the DSRD can be obtained. However, for the 500 V voltage input magnitude used, the DSRD output were all in breakdown and are not predictive of non-breakdown behavior. Future studies for optimal area will include a range of voltage magnitudes to study DSRD performance and breakdown.

(B.4) TCAD process and device modeling for the development of process steps and their resultant doping profiles and device operation was begun. This modeling will enable a connection between the fabrication parameters and the device operation for DSRD (and PSD).

(B.5) Exponential doping profiles were shown (via TCAD) to outperform Gaussian and error function profiles slightly. Exponential profiles have an optimal minimum doping of 5×10^{13}–$1\text{x}10^{14}$ dopant atoms/cm^3, while Gaussian and error function profiles have an optimal minimum doping of 1×10^{13}-5×10^{13} dopant atoms/cm^3. Further exponential doping parameter studies were carried out in circuits A and B of Figure 4.2.1 (see JUN 2021 Grant Report) which included a broader doping parameter space for minimum doping, junction placement, basewidth and peak doping over a wider range of voltage input magnitudes (for breakdown limitations). The results are similar to before and show the optimally performing doping profile has a minimum doping of 5×10^{13}, no basewidth, junction placement of 95 µm, and peak doping of 1×10^{18} (p-side) and 1×10^{19} (n-side) dopant atoms/cm^3. A comparison was made for the optimal exponential doping profiles to optimal error function, LLNL and SPT DSRD designs within the 2x2 DSRD pulser system. The TCAD study showed the exponential doping profile performs the best overall when considering peak voltage, risetime, voltage riserate, maximum reverse current, FWHM pulsewidth, prepulse and gain. Epitaxy designs with realistic deviations

from the ideal exponential profile from the SRP data were shown in TCAD to not significantly affect the performance.

(B.7) A more complete gain study for varying prime voltage input and stack height was completed. The results show a variety of considerations must be made for determining the better stack heights to use in DSRD pulsers. The design of the pulsers can be improved when considering the gain staging in multi-staged DSRD pulsers as caused by the DSRD stack heights used. The 7- and 13-stacks showed the best gain. However, the peak voltages were best for the 13-stack while the 26-stack required unrealistic MOSFET currents to achieve its maximal peak voltage (or gain). For gain per die within a DSRD stack, 1-stacks showed the best gain per single and showed that gain 'efficiency' drops with stack height. Still, higher 7- and 13-stacks had the highest gain. How best to use this new data for DSRD pulsers is under discussion.

(B.10) First semiconductor opening switch (SOS) TCAD simulations have been performed for demonstrating a hgiher current density mode of operation. Future SOS TCAD simulations can help delineate the difference in DSRD and SOS for current density snappy recovery according to doping profile and mode of device operation.

(C.1) Pulse sharpening has been verified for PSD devices for the standard design and another non-conventional design. The PSD was also modeled within a DSRD-based pulser circuit combining for the first time TCAD modeling of both DSRD and PSD together within the same circuit with only the primary switch model not included.

(E) DSRD pulser circuits for the single-bar (Circuit B of Figure 4.2.1) and 2x2 (circuit C of Figure 4.2.1) have been simulated within TCAD allowing the use of a TCAD DSRD model, whereas in SPICE no accurate DSRD SPICE model is available. Currently, the primary switch MOSFET is modeled in TCAD, as well, but SPICE models can also be developed for the SPICE within TCAD as and will allow for better use of computational resources within TCAD. The MOSFET model and pulse repetition are being studied in detail to more closely match experiment and TCAD.

5.2 Pioneering Drift-Step Recovery Diode Processing and Manufacturing

(Alex Usenko)

5.2.1 *Problem Statement, Approach, and Context*

Primary Problem: DSRDs have not increased in performance since the 1960's due to reliance on deep diffusion manufacturing. Their voltage-to-risetime, dV/dt, remains about 10^{12} V/s. To achieve the 10^{13} V/s (10 kV/ns) voltage-to-risetime required by an all-solid-state HPM pulse generator in support of the Naval afloat mission, improving DSRD manufacturing techniques is critical.

Solution Space: Leverage applicable concepts from the mainstream silicon chipmaking industry and apply new manufacturing methods to DSRD processing.

Sub-Problem 1 – Diode silicon surface termination/passivation: The SOTA uses diode termination by a vertical wall. This design results in low breakdown voltage as it is limited by surface breakdown. To increase the diode breakdown voltage to closer to that of the bulk silicon breakdown voltage value, the vertical side wall design must be avoided.

Sub-Problem 2 – Stacking of DSRD dies: The SOTA is based on soldering of diode dies into a stack, which limits the stack lifetime to below 10^{12} pulses. Also, the SOTA did not apply the methodology of stacking wafers first, then cutting into dies. Switching to wafer level stacking will decrease the number of stacking operations by more than 100x.

Sub-Problem 3 – Packaging of stacked dies: *The* SOTA uses bare stacked DSRDs. Mounting the bare stack into a press-pack type package will improve long-term stability, such that the stack will survive a much higher number of pulses before it burns out.

State-of-the-Art (SOTA): In a recently published paper (2019),[1] the Russian St. Petersburg team at the Ioffe institute reported achieving a peak current density of 5 kA/cm^2 with a rise time of the output pulse front of ~2.3 ns, and a peak voltage across the load of 900 V (i.e., the peak switching power is 4.5×10^6 W/cm^2). The St. Petersburg team utilized deep diffusion technology. A competing team at Ekaterinburg, Russia [2] reports similar pulse performance. Both teams use outdated deep diffusion technology. As one can see, there has not been any significant improvement in DSRD pulse performance since the pioneering work done in 1960 [3].

Deficiency in the SOTA: First, no DSRDs have been manufactured using epitaxy technology with doping profile optimization. Second, no DSRD processing method exists that integrates side passivation with silicon dioxide. Finally, an acceptable DSRD stacking process has yet to be developed.

Solution Proposed: Manufacture DSRDs within the continental United States using an epitaxial growth process leveraging the optimal characteristics (e.g., doping profile, carrier concentration) determined through the work performed by our simulation tteam (previous chapter of this report) and through working with industry partners at Semiconductor Power Technologies (SPT), Livermore Semiconductor Research Laboratories (LSRL) and Lawrence Livermore National Laboratory (LLNL – Voss Group).

Relevance to OSPRES Grant Objective: DSRD manufacturing technology is a major building block of short-pulse high-peak-power defense systems. Our new disruptive process flow for DSRDs enables not only manufacturing of DSRDs at scale, but within the continental United States (CONUS). In doing so we will redefine the SOTA by producing optimal DSRDs. Further, DSRDs will be used within best-in-class HPM pulse generators which become part of more advanced defense systems within the Navy arsenal.

Risks, Payoffs, and Challenges:

Risks: As the process of producing DSRDs using epitaxial growth with doping profile design is novel, uncharted territory, there is inherent risk to its success. Additionally, post-processing methods based on the discussions provided in the ***Sub-Problems*** section are not well-established.

Payoffs: Replacing traditional deep diffusion technology with a new process integration scheme would allow better DSRD pulse performance. Electrical breakdown voltage, reliability, and lifetime are expected to increase, and rise time on a load is expected to decrease.

5.2.2 Tasks and Milestones / Timeline / Status

(A) Milestone – Produce epitaxial DSRDs that contain optimal exponential doping profiles and carrier concentrations /estimated MAR*22*.

1. Task – Design of experiment on 25 wafers through negotiations with vendors / *MAY–JUL21* / Completed
2. Task – Perform DSRD stack epitaxy on 13 wafers at SVM Inc., and 25 wafers at LSRL / *JUN–AUG21* / Completed.
3. Develop process integration scheme that uses epitaxy instead of deep diffusion / *JUL–OCT21 /* Completed.
4. Compare traditional DSRD technology and suggested integration scheme. List disadvantages of traditional processes and define potential advantages of new processes / MAY–NOV21 / Completed.
5. Run Gen2 and Gen3 lots. Gen2 is on wafers with epi from SVM, Inc., Gen3 is on wafers with epi from LSRL. Gen2 uses the same BEOL as Gen1. Run BEOL of Gen3 – using our new patented processing scheme – Si_3N_4 masking, TMAH etch, oxidation, selective electroless metal deposition, wafer bonding, sawing into diode stacks / OCT–MAR22.
6. Submit Gen2 and Gen3 diode lots to UMKC team for pulsed performance measurements; collaborate with team on determining optimal doping profile through DoE (design of experiments) analysis by Minitab software / OCT21–MAR22.

(B) Milestone – Develop diode separation technique while keeping wafer integrity / Estimated completion FEB22.

1. Design lithography masks for short loop experiment, submit order to vendor. / MAR–APR21 / Completed.
2. Design short loop experiment for V-groove etching for diode separation. / MAR–APR21 / Completed.
3. Run short loop experiment for the diode separation by anisotropic etch; analyze results / MAY–OCT21 / Completed.
4. Based on results of previous short loop run, adjust equipment, and process recipes to achieve sufficient etch uniformity across the wafer. Run on updated equipment and recipe to prove etch uniformity. / Estimated JAN22.
5. Design lithography masks for epi DSRD run; submit order to vendor. / OCT21 / Completed.

6. Run Gen3 lot through V-groove etch step, transfer lot to next process step. / Estimated MAR22.

(C) Develop Ohmic contact deposition technique integrable with epitaxy, diode side termination/passivation, and wafer bonding steps / estimated AUG–JAN22.

1. Design short loop experiment to determine technical feasibility of selective electroless deposition of metal stack as a method of Ohmic contact forming in the DSRD process integration scheme. / OCT21 / Completed.
2. Determine vendor from which to order electroless deposition kits; obtain quotes, order, receive the kits. / OCT21 / Completed.
3. Run short loop experiment – nickel-copper-tin stack electroless deposition on a blanket wafer. Analyze results. / DEC21 / Completed.
4. Develop process recipe for the metal stack deposition to use in Gen3 DSRD lot manufacturing / estimated JAN22.
5. Run the selective metallization step on Gen3 lot; transfer the lot to next processing step. / Estimated FEB22.

(D) Develop wafer stack bonding technique integrable with the rest of Gen3 process flow / estimated SEP–FEB22.

1. Design short loop experiment for bonding 2 blanket wafers with Ni-Cu-Sn layers by solid–liquid interdiffusion. / SEP21 / Completed.
2. Run 2-wafers short loop experiment. Analyze results. / Estimated OCT–FEB22.
3. Test technical feasibility of multiple wafer bonding by bonding 10-wafer stack / estimated FEB22.
4. Upon proof of technical feasibility of 10-wafer stacking, develop process recipe to use for processing of Gen3 DSRD lot / estimated MAR22.
5. Run wafer bonding step on Gen3 lot, transfer the lot to next processing step. / Estimated MAR22.

(E) Develop wafer stack sawing technique into DSRD stacks, integrable with the rest of Gen3 process flow / estimated NOV–FEB22.

1. Design sawing process using Disco saw available at Semiconductor Power Technologies for cutting 10-wafer stack / estimated JAN22.
2. Run short loop cutting of blanket bonded 10-wafer stack. Analyze results. / Estimated FEB22.
3. Develop process recipe for Disco saw tool to use for Gen3 lot. / Estimated FEB22.
4. Run sawing step on Gen3 lot / estimated FEB22

(F) Develop diode side passivation process integrable with the rest of DSRD process flow.

1. Test compatibility of thermal oxidation for the diode side passivation with preceding anisotropic etch step / estimated FEB22.
2. Alternative diode side passivation process: design short loop experiment on room temperature oxidation by forming porous Si film and oxidizing the porous film / APR–OCT21 / Completed
3. Run part of Gen3 lot using the oxidized porous Si as diode side passivation / estimated FEB22.
4. Second alternative diode side passivation process: Design short loop experiment on room temperature oxide deposition from oversaturated fluorosilicic acid / estimated MAY–JAN22.
5. Run part of Gen3 lot using the oxidized porous Si as diode side passivation / estimated FEB22.
6. Choose the best from 3 methods of diode side surface passivation techniques / estimated FEB22.

(G) Develop a DSRD process based on out-diffusion (opposite to traditional in-diffusion process).

1. Process Gen4 lot based on process integration scheme described in our patent application filed in / estimated FEB22.

(H) Find vendor that manufactures press-pack parts, order the parts, and encapsulate the DSRD stacks into the press-packs / estimated FEB22.

5.2.3 *Progress Made Since Last Report*

(A5) Gen3 lot fabrication. We are waiting to receive wafers back from Noel Technologies after lithography and nitride etch in windows. Noel broke our lithography mask, thus incurring additional delays to reorder the mask. The lot is expected to be back by mid-March.

(A5) Gen2 lot fabrication. Gen2-1 and Gen2-2 sublots are at the static and pulse performance characterization step at UMKC. The last Gen2-3 sublot from the 13-wafer Gen2 lot is expected to finish processing by end of March. Non-stacked DSRDs were manufactured.

(B4) Process step development: die separation on wafers by anisotropic etch in TMAH (tetramethylammonium hydroxide) based bath. A previous technical feasibility run exhibited unacceptable non-uniformity of v-groove depth, width, and surface roughness. A new process recipe has been found that gives excellent uniformity. In the new recipe, DMSO (dimethyl sulfoxide) has been added to TMAH. Deep literature analysis confirmed that we are the first in the world to have used TMAH/DMSO for anisotropic etching.

5.2.4 *Technical Results*

(B) **Diode side termination development.** In previous months we have proven the technical feasibility of anisotropic etching of silicon for the purpose of defining individual

diode dies. First the wafer surface is thermally oxidized, then lithography is performed to open windows in the SiO_2 mask (Fig.5.2.1). Then the wafer is wet processed in a TMAH based etchant. After etching, the v-grooves are formed, and thus the surface area and side termination area of each die is defined (Fig.5.2.2). The active area of the diodes is in epitaxial layer. therefore if the bottom of the v-groove is deeper than the thickness of the epitaxial layer, the diodes are completely separated. The wafer is still not separated into pieces, thus further allows stacking of wafers, instead of stacking individual dies as in the traditional technology. There are many dies on the wafer, thus the number of stacking operations is much smaller compared to the traditional technology. This yields significant cost savings.

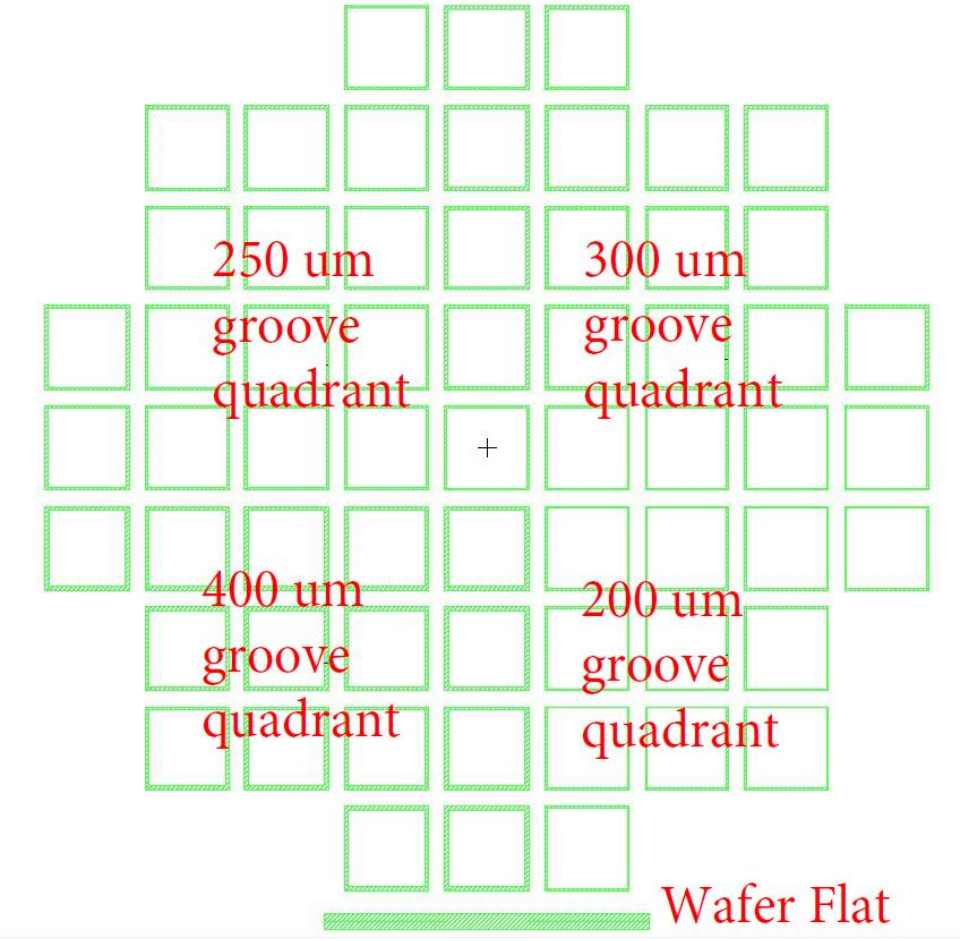

Figure 5.2.1. Mask design.

The anisotropic etch of silicon in alkaline solutions is based on different etch rates for different crystallographic orientations. The cross-sectional shape of each v-groove is determined by silicon wafer crystallographic orientation. For the TMAH etch case, the ratio of etching rates between <111> and <100> crystallographic planes is about 1:75. Resulting v-grooves etched on <100> silicon wafer are faceted by <111> planes thus giving about 57-degree slope sidewalls. As illustrated by Fig.5.2.2, the depth of the v-grove bottom point is determined by the width of the mask window. For example, in our

diodes with a 170-micron thick epitaxial layer, if we desire the v-grove bottom point to be at 200 microns, we must make mask windows 285 microns wide.

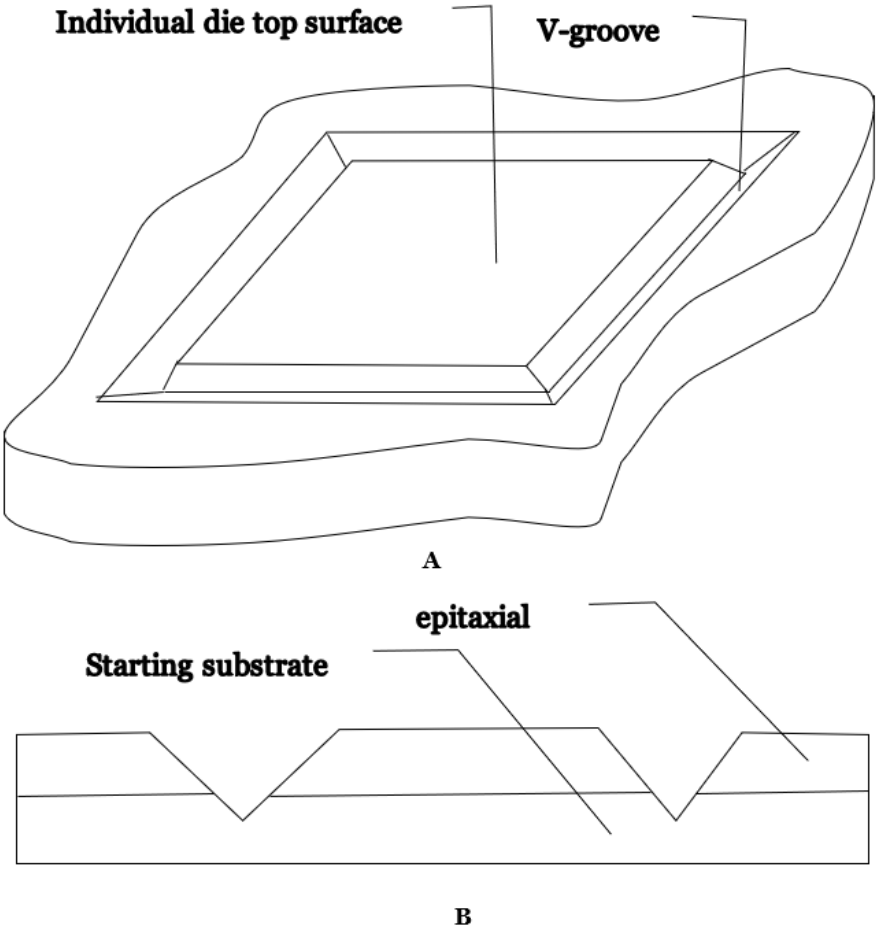

Figure 5.2.2. Illustration of how V-grooves define individual dies while keeping the wafer intact.

Either KOH (potassium hydroxide) or TMAH based etch solutions can be used for v-grove etch. KOH has about a 1:100 etch rate ratio between Si and SiO_2, while for TMAH the SiO_2 etch rate is negligible. That was one of the reasons to prefer TMAH over KOH – it allows for the use of SiO_2 as a mask. Another reason to choose TMAH over KOH is that they differ in etch rate ratios – between <110> and <100> planes, which eventually results in stronger corner rounding for TMAH (see Fig.5.2.3). Corner rounding is advantageous as it gives less electrical field concentration at the corners, thus eventually higher breakdown voltage of diodes.

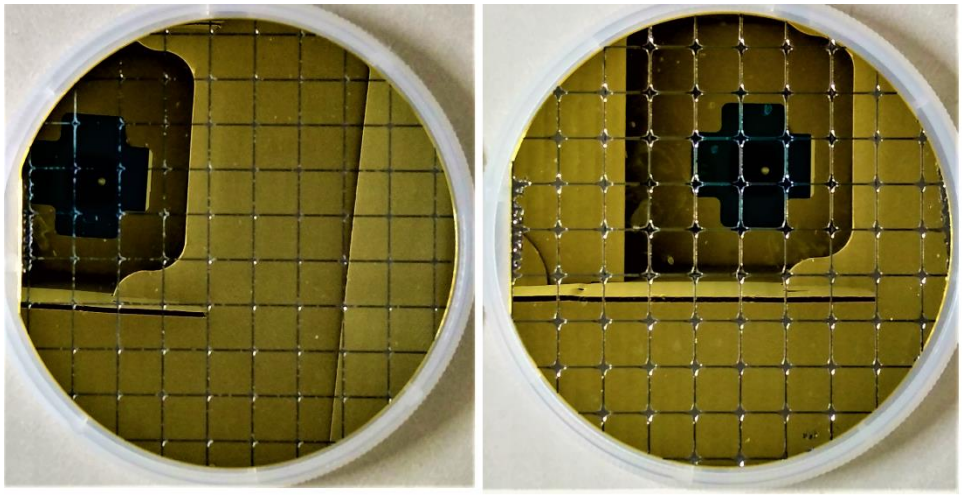

Figure 5.2.3. Comparison of edge rounding for KOH and TMAH etched wafers (left: KOH, right: TMAH).

Typical etch recipes for TMAH use 5% solution in water at 60–80 °C. At 80 °C the etch rate is 0.5 to 1 micron/minute, thus, to get 200-micron deep v-groove, 3.5 to 7 hours needed. 5% solution is often used as at this concentration the etch rate it the fastest. On the other hand, increasing the etch rate gives more reaction byproduct – hydrogen. Hydrogen forms bubbles that stick to wafer surface, act as local masks, and eventually cause etch non-uniformity and higher roughness of the etched wafer surface. Typical known solutions – to keep high etch rate, good uniformity, and low surface roughness – adding modifiers that help faster release of the hydrogen bubbles. IPA or Triton-100 are often added to the TMAH solution, speculating that lowering of liquid surface tension helps the bubble release. Our trial etching in both IPA and Triton-100 modified TMAH bathes shows some improvements, insignificant though. Therefore, we tried new modifiers, expecting to make significant improvements. One of trials used 1:1:1 mixture of standard 25% TMAH, DMSO, and water. So far, it has shown the best results for etch uniformity across the wafer, surface roughness and edge rounding. Fig.5.2.4, on left image the microscope has been focused on bottom of the v-groove. It shows that along the entire imaged length of the v-groove there is no under-etched (truncated) areas, v-groove is a clear triangle in cross section. Some features visible are due to contamination - insufficient cleaning after the etch. Fig.5.2.4 middle image is lower magnification of the same v-groove but focused on the wafer surface. V-groove bottom is out of focus and not visible. Punched lines on both sides of the groove are cantilevers of undercut SiO2 mask. It shows that width of the v-grove varies below 1% along its visible length. Fig.5.2.4, right image is the same low magnification image of the same v-groove, just in dark field mode and focused on the v-groove bottom. It confirms that the v-groove has near perfect triangle shape.

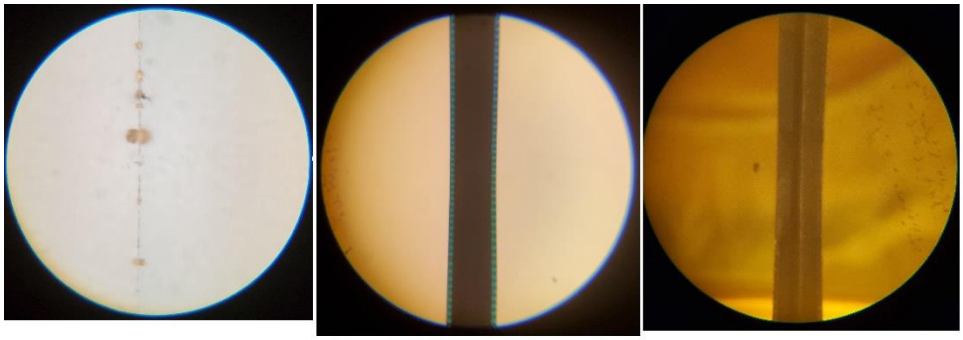

Figure 5.2.4. Optical microscopy of v-grove etched in 350-micron mask window using TMAH/DMSO etch recipe

Fig.5.2.5 shows a higher magnification optical image showing details of vertex rounding in our new TMAH/DMSO etchant. Neither non-modified TMAH, nor KOH etchants result in edge rounding. Again, punched lines are SiO2 undercut. SiO2 cantilever size is very uniform on the outer side of vertex but gets broken at various width at inner side of the vertex. Also visible is flat <100> surface area (white in color on image), not observed by etching with another recipes.

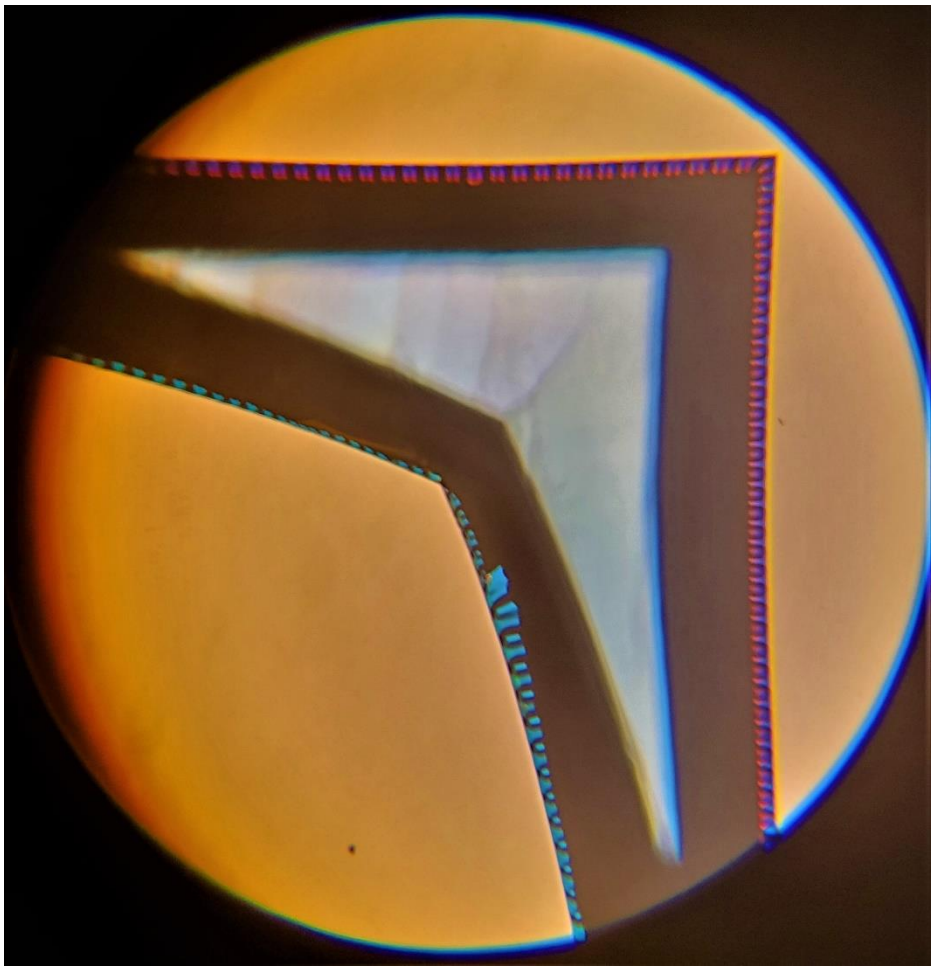

Figure 5.2.5. Optical microscopy image of vertex area showing edge rounding.

(D4) **Metallization step development**. Currently, our facility does not have equipment for electroless plating of metals on the top and back surface of our diodes. We have used in our previous DSRD generation – Gen1 and Gen2 - electron beam metal evaporation system to deposit metal film stacks and thus make Ohmic contacts to silicon dies. This technology is not efficient and costly. Therefore, efforts were directed to locate vendors that manufacture electroless plating tools, identify right tool, buy and install the tool in-house and eventually switch to electroless plating.

To guarantee that the tool will be able to make our desired metal stacks (Ni-Cu-Sn) we have arranged demo plating at application labs of the chosen tool vendors – Fibrotools, Stapleton, and Component Surfaces. First demo has been finished by Fibrotools. Fig.5.2.6 shows pictures of one of 3 wafers processed in the demo. As iit can be seen from the pictures, not an entire area of wafer is covered by the nickel film. Therefore, comprehensive measurements (electrical – Ohmic contact measurements, metal thickness and thickness uniformity, etc.) were not performed. Instead, a second demo has been arranged with Fibrotools. They expect to improve significantly plating quality after learning lessons from the first demo.

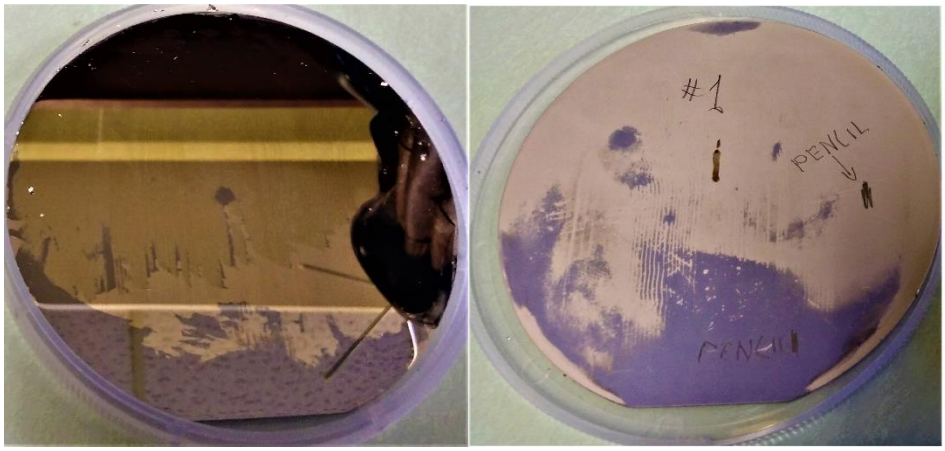

Figure 5.2.6. Front – left, and back – right of one Nickel plating demo wafers.

Only qualitative measurements of adhesion – by attempts to scratch the nickel film with a hard 6H pencil was performed. No scratch lines from pencil visible on front side of the wafer. On the back side of the wafer, the pencil leaves graphite lines – as expected – the back side of the wafer is not polished, but etched, thus have enough roughness for making a line by the pencil. Also, anneals at 250C, 450C, and 600C were performed. The scratch pencil test was repeated after each anneal step. Nickel on some samples flaked after the anneal. Though the anneal step is required – to convert nickel film into nickel silicide, thus improve both adhesion and electrical contact.

Another electroless plating manufacturer – Technics – refused to do a demo, as they have no application lab. They suggested we request demo from their former customers and shared the customer contacts with us. After several negotiations we got an offer from Hughes Research Lab that they donate the Technics tool to UMKC. Currently the tool is being crated for shipping and expected to be delivered by the end of March.

5.2.5 *Summary of Significant Findings and Mission Impact*

(A) Several process adjustments have been implemented in processing of next Gen2 die lots. Die-to-die excessive variability is noticed. Process recipes and some equipment have been adjusted to achieve better uniformity and repeatability.

(B) Improving side termination of diodes. To prevent detrimental non-uniformity due to hydrogen bubbles sticking to wafer surface, a new process recipe has been developed. TMAH/DMSO mixture showed excellent uniformity. Using this mixture for anisotropic silicon etch never described in literature, we found this first.

(C) Replacement of unreliable metal contact deposition technique (by electron beam sputtering in vacuum chamber). Technical feasibility run on direct electroless plating of the Palladium/Nickel stack was successful. Process recipe developed for next run, plate uniform stack of Pd/Ni/Cu/Sn. State of the art electroless plating tool being donated by Hughes Research Lab.

(D) A process recipe for side passivation of diodes using a stain etch has been developed. The thickness uniformity resulting from the stain etch technique has been drastically improved. New recipe that totally suppresses hydrogen bubbles sticking to the Si surface was found. Using that recipe, very uniform thickness (porous Si) films were successfully grown on blanket silicon wafers with both low and high doping levels.

5.2.6 *References*

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5.3 Characterization of SOS Diode Performance through DOE Augmentation

(Megan Hyde, Ethan Bozarth, & Joey Reeve-Barker)

5.3.1 *Problem Statement, Approach, and Context*

Primary Problem: Drift step recovery diodes (DSRDs) are planar diodes that are capable of nanosecond, high-frequency (10–10^3 kHz) pulses [1] with applications as opening switches in inductive energy storage (IES) pulse generation circuits. There is not a clear understanding of the effects DSRD parameters have on overall IES pulser performance. The purpose of this project is to tie the DSRD parameters to its tailored performance requirements.

Solution Space: Leveraging both design of experiment (DOE) and machine learning (ML) capabilities, we will develop a methodology of characterizing DSRDs in order to provide fabrication recommendations in the context of application targets.

***Sub-Problem 1*:** We do not yet understand how the diode parameters are tied to the diode performances.

Sub-Problem 2: There is no standardized method for correlating the diode key performance indicators (KPIs) to the IES pulser generator performance.

Sub-Problem 3: The number of possible inputs for the DOE is expected to be too large, so ML will need to be leveraged in order to guide decision-making processes.

State-of-the-Art (SOTA): Standard diode measurements include curve tracers for forward and reverse IV, impedance spectroscopy for forward and reverse CV, and function generators or, for example, the Avtech pulser for reverse recovery with high voltage and/or high current when necessary. These measurements are used to generate commonly available datasheets for COTS diodes. These standard diode measurements can then be correlated to pulser performance using traditional data analytics.

Deficiency in the SOTA: The standard diode measurements and datasheets do not include pulser performance necessary to evaluate DSRDs. The datasets generated with doping profile assessment (for example spreading resistance profiling), standard diode measurements and pulser performance are too large and complex to leverage traditional data analytics and will benefit from machine learning techniques.

Solution Proposed: Develop a holistic evaluation network to characterize the KPIs of DSRDs. This network will include a DOE that will be a continuously evolving model as new KPIs are discovered. Augmenting the DOE will ensure that the model will remain relevant throughout this study as more discoveries are made. Machine learning will be used as the primary decision-making tool for augmenting the DOE. Once the network is established, it will be used to outline the optimal parameters for stacks of DSRDs within an IES pulse generator.

Relevance to OSPRES Grant Objective: Bridging the gap between the theoretical and physical performance of DSRDs enables closing the gap between a low fidelity TRL3 breadboard pulse generation system, and one which is at high fidelity TRL4 prototype level. At the TRL4 level, the DSRD-IES pulse generator system would be sufficient to replace the costly laser-based Si-PCSS HPM generator without compromise to scalability required to support the Naval afloat mission.

Risks, Payoffs, and Challenges:

Challenges: Traditional predictive analytics will be difficult to correlate with the augmented DOE due to the large volume of data. Machine learning is expected to assist with decision making processes for the DOE, but only if the proper KPIs have been established and good data has been used to train the machine learning model.

5.3.2 Tasks and Milestones / Timeline / Status

(A) Milestone – Establish preliminary DOE and standard operating procedure (SOP) for identifying KPIs of DSRDs [*estimated completion by MAR22*].

1. Task – Ascertain current KPIs used to optimize diodes simulated, manufactured, and utilized within the IES pulse generating circuit [completed AUG21];

2. Task – Construct preliminary DOE to acquire data on all KPIs based on Task 1 [*completed FEB22*];
3. Task – Leverage existing Python scripts to process legacy DSRD KPI data [*completed SEP21*];
4. Task – Develop new and review existing SOPs for experimental testing apparatuses used to evaluate individual KPIs and measure their performance [*completed OCT21*];
5. Task – Identify gaps/deficiencies in legacy KPI data, evaluate existing theoretical relationships to bridge gap and minimize DOE if possible [*completed OCT21*];
6. Task – Using SOPs developed in Task 4, acquire experimental data from legacy DSRDs, refine SOP(s), and assess repeatability and reproducibility [*SEP21–MAR22*];

(B) Milestone – Evaluate DSRD performance by the developed SOPs and facilitated by the preliminary DOE [*estimated completion JUL22*].

1. Task – Acquire data on newly manufactured 2nd generation epitaxial DSRDs from Section 5.2 using refined SOPs from Milestone A [*completed JAN22*];
2. Task – Evaluate precision and power of DOE [*MAR22–JUL22*];
3. Task – Develop a test matrix to guide DSRD selection for the pulser circuit based on categorized test measurements of characterization tests *[MAR22—MAY22];*
4. Task – Correlate KPIs to TCAD simulation model, manufactured diode characteristics, and 'M×N' IES pulser performance to aid in simulation model development, fabrication procedures, and circuit topology development [[*MAR22—JUN22];*
5. Task – Begin training machine learning model with DSRD data to determine statistical correlations and significance of KPIs, and their interdependent relationships [*MAY22—JUL22*];
6. Task – Acquire data on newly manufactured 3rd generation epitaxial DSRDs from Section 5.2 using refined SOPs from Milestone A [*JUL22-SEP22*];

(C) Milestone – SOS diode network evaluation [*on hold until Milestone B is completed*].

1. Task – Refine Python script to incorporate new correlations based on findings from Milestones A&B [*Est. Summer22*];
2. Task – Amend ML training model with data acquired on new DSRDs (as characterized by Sections 5.1–5.2) to investigate statistical correlation of diode performance [*Est. Summer22*];
3. Task – Work with TCAD simulation team to address discrepancies between the DSRD performance obtained experimentally, and that achieved within simulations [*Est. Summer22*];

4. Task – Collaborate with DSRD manufacturing team to address discrepancies between the DSRD characteristics evaluated experimentally, and that desired by manufacturing process [*Est. Summer22*];
5. Task – Investigate relationships between statistical significance of individual diode KPIs to the peak performance of the IES pulser with the pulse generator team. [*Est. Summer22*];
6. Task – Incorporate findings from Tasks 1–5 into ML model, pinpoint KPI correlations of interest, and provide recommendations to IES sub-teams accordingly [*Est. Summer22*];

(D) Milestone – SOS diode network evaluation [*on hold until Milestone C is completed*].

1. Task – Augment DOE network to streamline diode evaluation and identify checkpoints/gaps within simulation, manufacturing, and circuit development process to ensure optimal diodes are selected and utilized to produce robust high-fidelity IES pulse generator prototypes [*Est. Fall22*].

5.3.3 *Progress Made Since Last Report*

(A.2) A preliminary experimental design was constructed to include the following KPIs: zero junction bias capacitance, maximum forward voltage at 10 mA, and current at reverse 200 V. To begin, the current–voltage measurements are scheduled to be acquired with a picoammeter, but progress is being made to provide comparison measurements on a Tektronix 371A Curve Tracer.

Table 5.3.1 contains a list of all the diodes selected for the preliminary experiment for the randomized complete block design (RCBD). All experiments have been completed except for Rounds 1, 2, and 3 by one out of the three analysts. Once these measurements have been completed, the repeatability of each test will be evaluated.

(A.6) Experimental data was acquired on all tests for all diodes except for the deep diffusion (DD7) 7 stack diodes that are awaiting reverse recovery testing (RRT). A completely randomized block design (RCBD) along with a diode testing schedule was established so that other projects (e.g., pulser testing) can anticipate diode availability for their testing requirements.

(B.3) The capacitance–voltage (CV) test measures the amount of charge stored in the diode as the amount of supplied voltage changes. The zero bias junction capacitance is a measurement of the amount of charge maintained in the diode when the outside supply is zero. This diode indicator can be tied to peak voltage and risetime, however, there is no quantified correlation between these values. This study intends to develop a testing matrix that will identify diodes with similar zero junction bias capacitance values and place them into categories based on their predicted performance in the pulser circuit. By classifying the diodes using the parameter values and connecting them with the values obtained from pulser testing, it should be possible to determine a correlation between the CV values and pulser

performance values. We will use this test matrix to optimize the implementation of diodes into the pulser circuit without the current levels of trial and error.

5.3.4 *Technical Results*

(A.6) Preliminary results from the experimental data collected thus far showed inconsistencies in the results. These inconsistencies manifested themselves in the repeatability study performed on the Gen 2 diodes. These diodes underwent forward and reverse current–voltage and capacitance–voltage measurements a total of three times. The results of this repeatability study are shown in Figure 5.3.1. This study highlighted the need to identify and reduce the influence of "nuisance factors" that are probably affecting the experimental results.

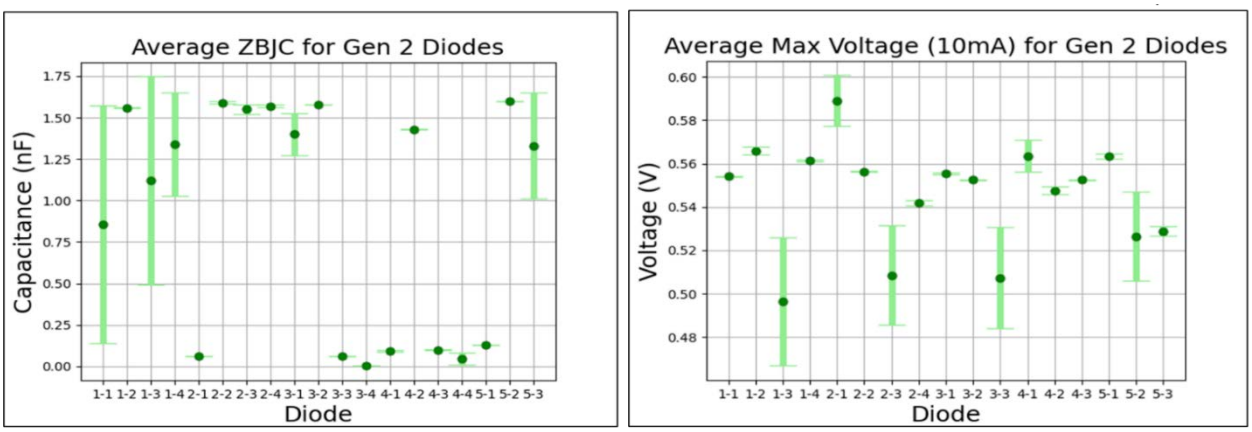

Figure 5.3.1. Results of the zero-junction bias capacitance and the maximum forward voltage at 10 mA for the repeatability study of the Gen 2 diodes. A Levene's Variability test was performed on the results for both tests, where the p-value validates the consistency of the testing performed (p = 0.85 for the zero-junction bias capacitance and p = 0.84 for maximum voltage measurements). Diodes 3-4 and 4-4 were not included in the maximum voltage graph because the devices failed to reach 10 mA.

	Round 1	Round 2	Round 3
Deep Diffusion 7 Stack	D1	D319	D333
Deep Diffusion Untested	630	657	801
Epitaxially Grown 1500	1562	1563	1564
Epitaxially Grown 1600	1601	1602	1603
Gen 2	1-1	1-2	1-3
Gen 2.2	1	2	3

	Round 4	Round 5	Round 6
Deep Diffusion 7 Stack	D366	D367	D380
Deep Diffusion Untested	802	803	804
Epitaxially Grown 1500	1565	1566	1567
Epitaxially Grown 1600	1604	1605	1606
Gen 2	1-4	2-1	2-2
Gen 2.2	4	5	6

Table 5.3.1. This table is representative of 16 total rounds for the experimental design testing. Each round contains one of each type of diode (i.e., deep diffusion 7 stack, epitaxially grown diodes, gen 2 diodes).

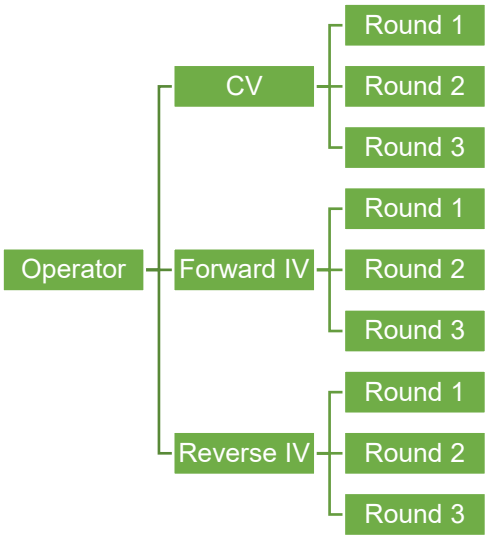

Figure 5.3.2. A simplified flow chart on how the diodes from Table 5.3.1 will be tested. Each round will be tested by 3 different operators using 3 different techniques (forward IV, reverse IV, and CV) with a minimum of 12-hour break in between each test. Note: only Rounds 1 through 3 were included in this chart for simplicity.

Possible nuisance factors that have been identified are operator, equipment/sample holders, and time in between data collection. These factors were used to outline a testing plan to mitigate future influence on measurement results by "blocking" each factor. Figure 5.3.2 provides a basic outline of the testing expectation of each round of diode.

The capacitance-voltage measurements for Rounds 1 through 6 in the DOE have been evaluated. The average of each diode was calculated along with their respective standard deviations. The Gen2 (single stack diodes) were multiplied by 7 in order to normalize the results to the other 7 stack diodes. As can be seen from Figure 5.3.3, the Gen2 diodes (both first and second Gen2 groups) have the greatest variability in measurement. Average Gen2 measurements range from 8.8E-10 to 1.1E-08F with standard deviations ranging from 2.4E-11 to 6.0E-09F. Further analysis will be required to determine if these measurements are an improvement to the previous repeatability study. Surprisingly, the untested deep diffusion showed the least deviation out of all the different groups of diodes with average zero junction capacitance measurements ranging from 6.6E-10 to 6.8E-10 with standard deviations ranging from 6.0E-12 to 1.7E-12F.

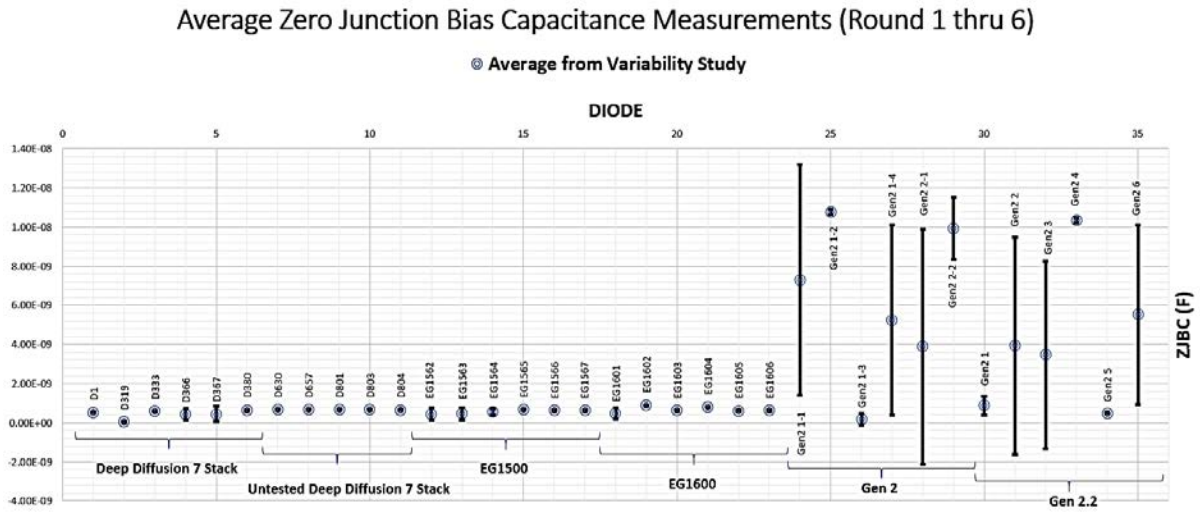

Figure 5.3.3 Each diode was measured once by three different analysts as part of the DOE variability study. Each measurement was averaged and is plotted with their respective standard deviations. Since the Gen2 diodes are all single stacks, each measurement was multiplied by 7 in order to normalize the data.

5.3.5 *Summary of Significant Findings and Mission Impact*

(A.1) The KPIs established thus far are: current at -200 V, voltage at 10 mA (forward bias), zero junction bias capacitance, minority carrier lifetimes, and series resistance. Additional KPIs are expected for IES pulser circuits.

(A.2) A preliminary DOE is in process. Currently, 6 out of a total of 16 rounds of DSRD diodes are undergoing DC testing for characterization purposes. Once the 6 rounds have completed testing, statistical analysis will determine if the experimental design requires modification.

(A.3) Python scripts have been modified for calculating and exporting measurement results and plots into Excel file.

(A.4) SOPs for forward and reverse IV and CV have all been updated with a page for tracking changes made to the procedures.

A standardized testing procedure for RRT measurements is still in progress. Development of this test will lead to an increased understanding in minority carrier lifetime measurements and how they relate to the forward pumping time for pulsing.

(A.5) The IV measurements are performed by a picoammeter, which restricts the range of current that can be applied to each diode. A Tektronix curve tracer is under investigation for data collection to provide test results for larger currents and voltages.

(A.6) Inconsistencies in the experimental results require a root cause analysis. A preliminary repeatability and reproducibility test was performed on all Gen 2

diodes. Each diode was tested three times on each test, but the results revealed large variations. A RCBD experiment will aid in eliminating some of the possible sources of variation.

(B.1) Measurements have been collected on all Gen2 diodes for forward and reverse current-voltage, capacitance-voltage, and reverse recovery time tests.

5.3.6 *References*

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5.4 DSRD-Based Pulsed Power Source Systematic Topological Optimization

(Gyanendra Bhattarai & Roy Allen)

5.4.1 *Problem Statement, Approach, and Context*

***Primary Problem*:** Inductive energy storage (IES) and release pulse generators that use drift-step recovery diodes (DSRDs), while able to achieve ones of gigawatts in ones of nanoseconds, are not topologically optimized to achieve high forward pumping current and voltage gain (peak pulse voltage/prime source voltage), making them require large and heavy high-voltage prime power supplies. They also require liquid-based cooling systems to dissipate the excess heat they generate during operation, further adding weight and rendering them impractical for Navy afloat missions.

***Solution Space*:** Systematically develop optimum circuit topology to maximize the voltage gain, and thus the peak voltage, peak power, and volumetric power density while minimizing the heat loss by increasing energy efficiency through circuit optimization without sacrificing the desired nanosecond risetime of the pulses generated.

***Sub-Problem*:** DSRDs are not domestically available COTs components. They are manufactured in small-batch quantities, and have statistically significant variations in their performance parameters. In addition, SPICE models of these diodes we have been developing may not be accurate. These issues may lead to an inaccurate simulation model of the pulser that may result in differences between simulated and experimental results.

***State-of-the-Art (SOTA)*:** Air-cooled DSRD-based pulsers (equivalent in size to the pulse generators developed for this effort, i.e., ~0.01-m^3, ~2-kg) can achieve 6-kV, 1–2 ns risetime, and <4 ns FWHM across a 50 Ω load.

***Deficiency in the SOTA*:** Small-volume air-cooled DSRD-based pulsers are limited to peak voltage and PRFs of <15 kHz. Additionally, current studies on SOS-IES pulse generators attempt to present only the best-case circuit configurations. There is a lack of comprehensive study of circuit topologies and optimization to achieve maximum gain and efficiency and reduce thermal load.

***Solution Proposed*:** Develop different DSRD circuit topologies implementing series and parallel combinations of DSRDs to minimize circuit components, such as inductors, capacitors, and switches. Systematically optimize the circuit configurations and necessary components through physics-based DSRD pulser circuit theory and SPICE simulation to maximize voltage gain and efficiency while minimizing the prime source voltage and thermal load.

Relevance to OSPRES Grant Objective: Air-cooled IES pulse generators using optimum DSRD stacking can remove the need for photo-triggered switches and their laser sub-systems. They are ideal for triggering sub-nanosecond rise-time sharpeners (SAS, D-NLTL, etc.), reducing overall cost, volume, and weight.

Risks, Payoffs, and Challenges:

***Risks*:** Domestically manufactured (U.S.-based) DSRDs, which possess sub-optimal doping profiles, may lead to sub-optimal pulse generators with sub-optimal performance.

The data gathered from these sub-optimal circuits would then be used to train the genetic/machine learning algorithms developed and the redesign of future topologies constructed; ultimately leading to spurious conclusions regarding ideal topological circuit configurations with 'N' number of series-connected stages, each containing 'M' parallel branches.

***Payoffs*:** Leveraging collaborative partnerships with U.S.-based manufacturers of DSRDs, the ability to refine and control the performance characteristics of the diodes themselves, along with the ability to simulate and manufacture the DSRD pulsers in-house, enables a holistic soup-to-nuts capability to optimize, produce, and evaluate these nanosecond pulse generators.

***Challenges*:** Determining the superlative ratio of design/development (through numerical analysis) to the effort put towards experimental testing/evaluation of the DSRD pulser is challenging due to the novelty of the approach. The complexity of the theoretical model is extreme given the M×N number of DSRD base unit stages within the pulse forming network along with inaccurate DSRD spice model and large sample-to-sample variability.

5.4.2 Tasks and Milestones / Timeline / Status

(A) Milestone – Develop theory of DSRD pulse generator to facilitate optimization of 1×1 pulse generator [***Completed – JAN22***]

(B) Milestone – Extend the theory developed in Milestone A to facilitate optimization of M×N pulse generator [***Ongoing***].

(C) Milestone – Construct/demonstrate a DSRD-based 1x1 pulse generator prototype based on theory developed in milestone (A) and obtain performance data for multiple combinations of diode stacks [***Ongoing***].

(D) Milestone – Construct/demonstrate a DSRD-based 2×2 IES pulse generator prototype capable of producing $\geq$4 kV peak voltage, $\leq$1 ns risetime, $\leq$5 ns FWHM, $\geq$320 kW peak-power, $\geq$1 kHz PRF, $\geq$100 shots-per-burst, $\geq$5 number of bursts [***Completed JUL21***].

(E) Milestone – Construct/demonstrate a DSRD-based 4×2 IES pulse generator prototype capable of producing $\geq$12 kV peak voltage, $\leq$1 ns risetime, $\leq$5 ns FWHM, $\geq$3 MW peak-power, $\geq$100 kHz PRF, $\geq$1,000 shots-per-burst, $\geq$500 number of bursts [*On hold*].

(F) Milestone – Develop waveform inverter which, when combined with the pulser from Milestone C, enables a balanced differential waveform output with >90% inverted signal fidelity. [***Completed – DEC21***].

(G) Milestone – Construct/demonstrate a M×N pulse generator prototype capable of producing $\geq$20 kV peak voltage, $\leq$1 ns risetime, $\leq$2 ns FWHM, $\geq$8 MW peak-power, $\geq$100 kHz PRF, and $\geq 2\sigma_{Vpeak}$, which operates in continuous-burst mode as a viable candidate for OSPRES Contract source alternative [*on hold until Milestones B, D, & E are completed*].

5.4.3 *Progress Made Since Last Report*

(A) Single-bar DSRD pulse generators optimized for four 7-stack diodes and two 7-stack diodes are simulated based on the theory presented in the MSR DEC2021.

(B) Two new 1×1 DSRD-based pulse generators optimized for four 7-stack diodes and two 7-stack diodes have been populated and are being tested for different combinations of diode stacks. A maximum peak output voltage of 6.7 kV is obtained with four 7-stack diodes for a trigger length of 700 ns using a prime supply voltage of 120 V. Increasing the prime source voltage to 170 V, the maximum peak output of 7.5 kV is obtained for a trigger length of 700 ns, suggesting the possibility of further enhancing the output with better MOSFETs.

5.4.4 *Technical Results*

5.4.4.1 Experimental Results from Single-Bar 1×1 DSRD Pulser

(C) The MOSFET-driven 1x1 DSRD pulser circuit board was populated with circuit elements optimized for a peak output voltage of 14 kV using a prime source of 120 V and a trigger length of 1.1 µs, as mentioned in MSR JAN2022. For higher pumping current, the previous MOSFET C2M0045170P was replaced by NVH4L020N120SC1. Though the new one needs more gate charge and has a lower breakdown voltage (1200 V vs 1700 V previously), it can handle a much higher pulsed current, 400 A vs 160 A previously. The peak output voltage was set at 14 kV assuming the breakdown voltage of 500 V per diode stack for a 28-stack diode and a maximum limiting MOSFET current of 400 A during forward pumping. The maximum output obtained from the pulser, however, was only 6.7 kV for a trigger length of 700 ns, as shown in Figure 5.4.1.

As the maximum peak voltage was not as expected from the simulation, we tried increasing the prime source voltage. Figure 5.4.2 shows the output obtained with a prime source of 150 and 170 V. As we can see from the figure, the output increased with the increasing prime voltage and attained 7.5 kV. However, the MOSFET driver and the MOSFET were blown out after experimenting with 170 V prime source. This confirmed that the optimized circuit elements were right under the limiting MOSFET current, but the smaller output obtained compared to the simulated value was due to the non-optimized SPICE diode models developed until now. The increasing output with the increasing prime voltage further suggests that the diodes can be pumped with higher current, which, however, requires better MOSFET and/or MOSFET paralleling.

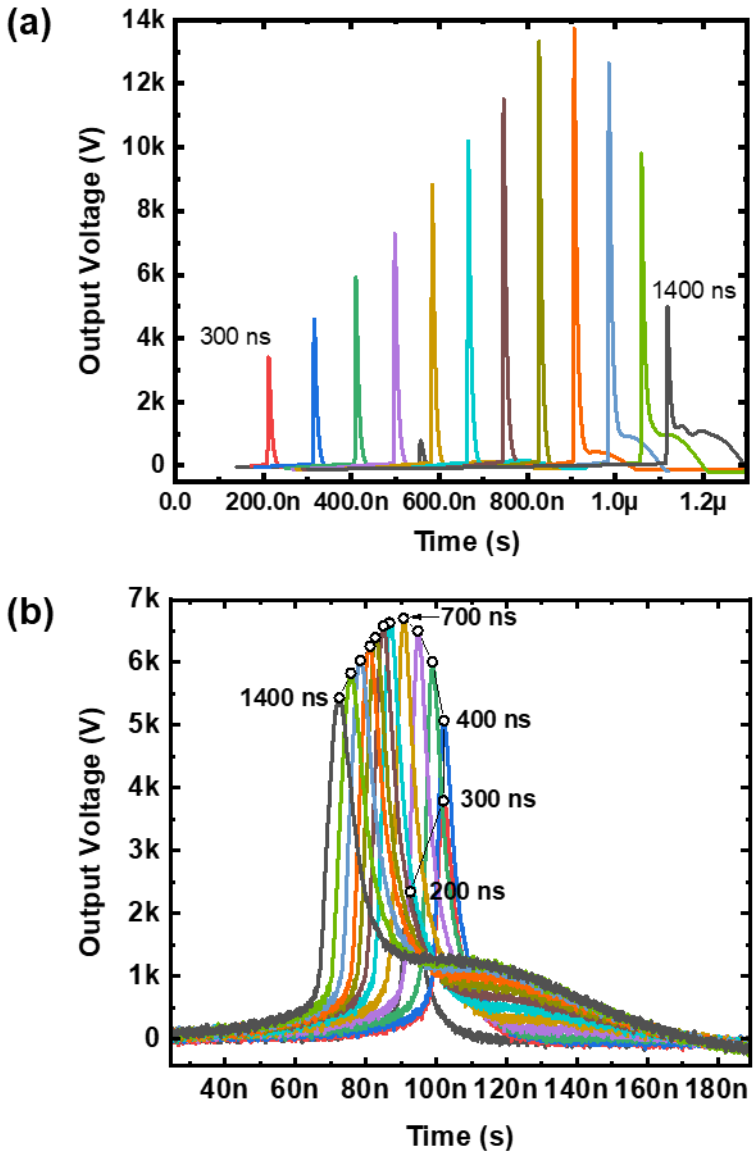


Figure 5.4.1. Simulated (a) and experimental (b) DSRD pulser output obtained with 28-stack diode (EG1571-1574) using optimized circuit elements for different trigger lengths.

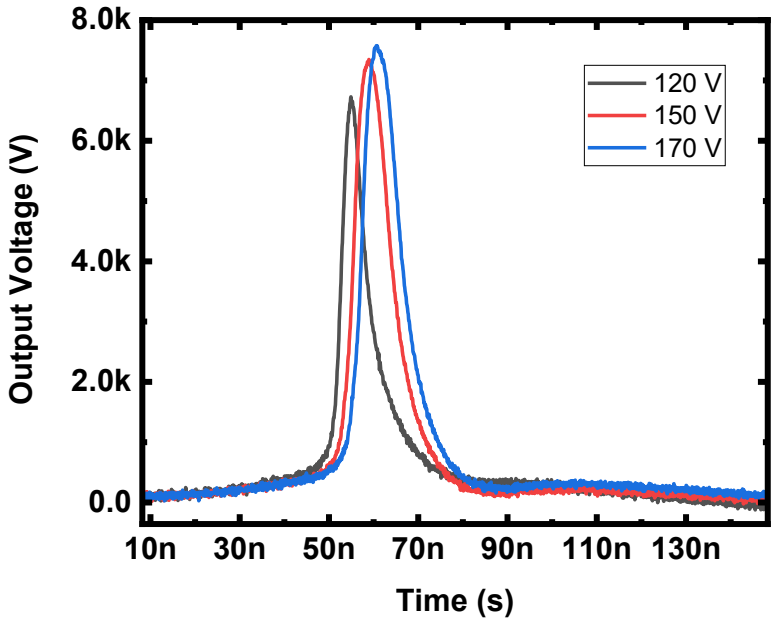


Figure 5.4.2. 1x1 28-stack (EG1571-1574) DSRD pulser output with optimized circuit elements and varying prime source voltages.

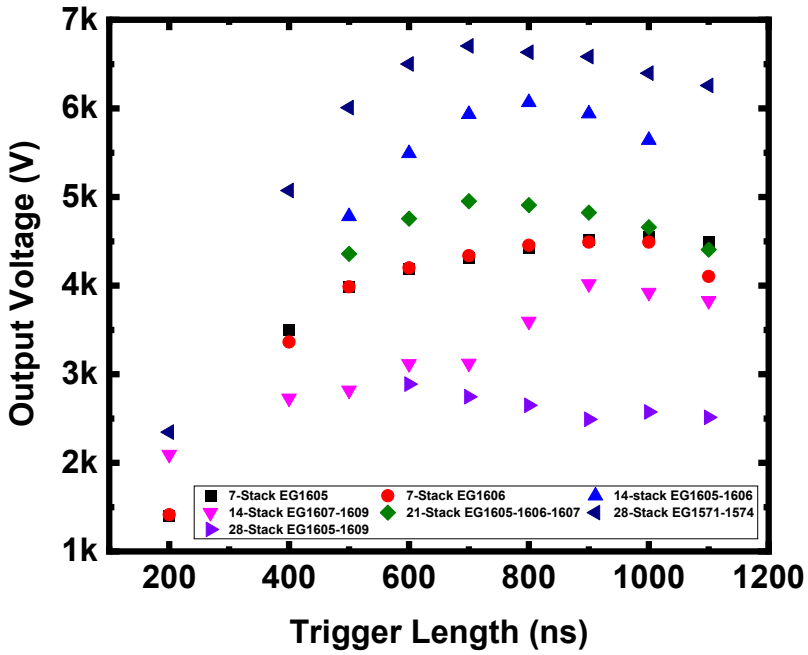


Figure 5.4.3. Variation of peak voltage with trigger length for different diode stacks obtained with DSRD pulser optimized for 28-stack diodes.

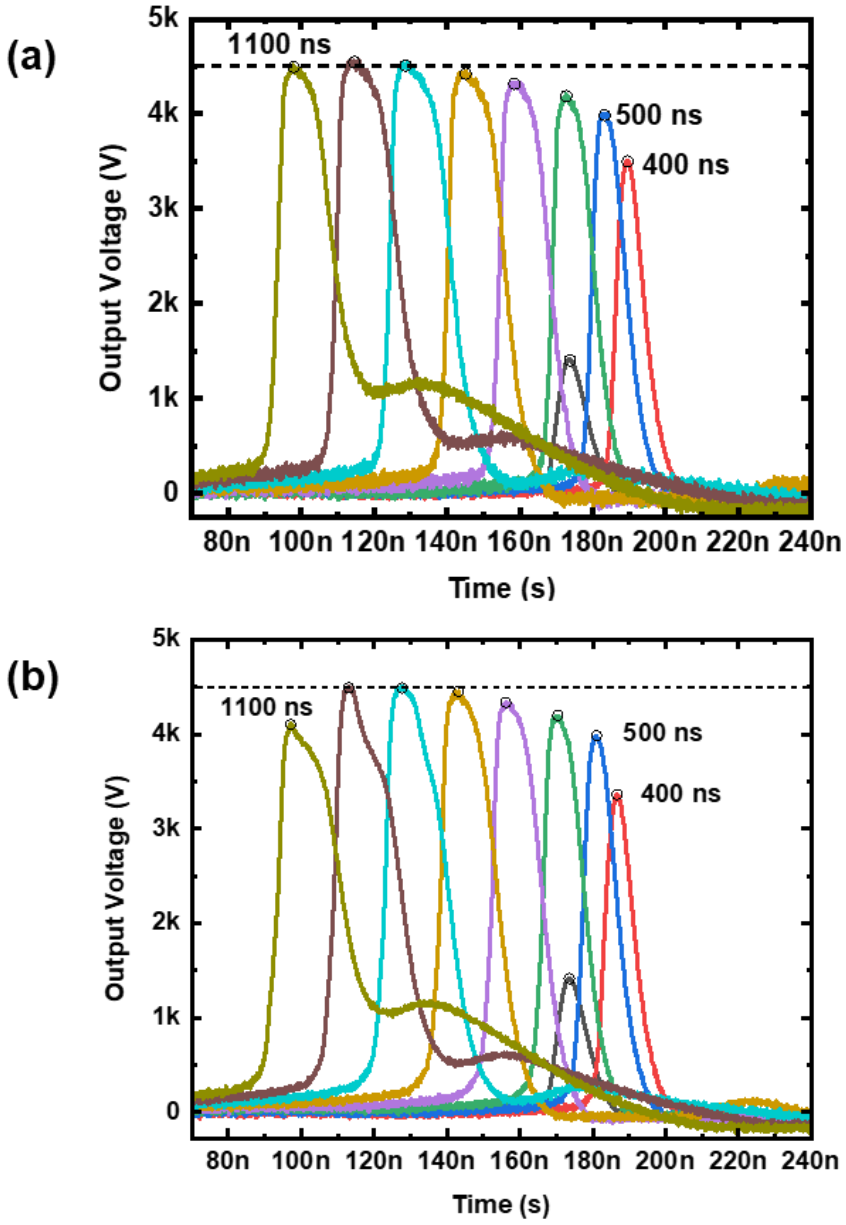


Figure 5.4.4. Output from 7-stack diodes (a) EG1605 and (b) EG1606 obtained from the pulser optimized for 28-stacks showing the output voltage limited to ~ 4.5 kV due to diode breakdown.

The 28-stack optimized circuit was further tested with 21-stack, 14-stack, and 7-stack diodes. Figure 5.4.3 shows the peak output voltage as a function of trigger length for different diode stack configurations from the EG1600 series. Although the 28-stack diode (EG1571-1574) had produced the maximum output of 6.7 kV for a trigger length of 700 ns, the 28-stack diode (EG1605-1608) performed the worst among all other configurations, suggesting a high variability in the diodes in the EG1500 and EG1600 series. The 7-stack diodes EG1605 and EG1606 produced peak output voltages up to 4.5 kV for a trigger length of 1 μs. However, we believe that their output was limited due to the diode breakdown as shown in Figure 5.4.4. This result suggests that the reverse breakdown voltage per diode stack in the EG1600 series could be ~ 650 V. Considering

the output from single stack diodes in the EG1500 series, the 14-stack diode (EG1605-1606) performed as expected producing a peak output of 6.1 kV for a trigger length of 800 ns. The 21-stack diode (EG1605-1607) produced a maximum peak voltage of 4.9 kV for a trigger length of 700 ns, which could be due to the decrease in pumping current while adding more diode stacks. However, the 21-stack diode (EG1607-1609) produced only a maximum peak output of 4 kV for a trigger length of 900 ns. This suggests that the 7-stack die EG1609 could be a bad diode. A further check is required to confirm the performance of the diode. Table 5.4.1 shows a summary of the DSRD pulser characteristics for different diode configurations using the circuit parameters optimized for 28-stack diodes.

Table 5.4.1. DSRD pulser performance metrics for different diode stack configurations obtained from DSRD pulser using circuit elements optimized for 28-stack diode.

Diode Configuration	Optimum Trigger length (ns)	Peak Voltage (kV)	Peak Power (kW)	Total Energy (mJ)	Rise Time (ns)	Fall Time (ns)	FWHM (ns)
28-stack Simulated	1100	13.7	3753.8	19.00	1.1	15.7	6.6
7-stack (EG1605)	1000	4.6	415.9	6.43	6.3	59.8	18.2
7-stack (EG1606)	1000	4.5	406.8	6.06	9.4	65.4	19.1
14-stack (EG1605-1606)	800	6.1	736.9	4.96	6.8	14.8	8.5
21-stack (EG1605-1607)	700	5.0	492.0	3.53	14.3	16.4	8.8
21-stack (EG1607-1609)	900	4.0	325.6	4.43	30.6	59.0	20.6
28-stack (EG1571-1574)	700	6.7	905.2	5.04	9.6	18.9	6.9
28-stack (EG1605-1608)	600	2.9	168.2	2.15	28.9	30.7	17.8

As the optimum trigger length of 700 ns obtained with the experiment did not match with the optimum trigger length of 1.1 µs from the SPICE simulation for a 28-stack configuration, and because the output was nearly 50% of the expected value, we repopulated the circuit board with elements optimized for an output of >13kV using 14-stack die with a trigger length of 700 ns. Here, we did not limit the output to 7 kV for 14-stack realizing that it would lower the output as seen from the 28-stack optimized circuit.

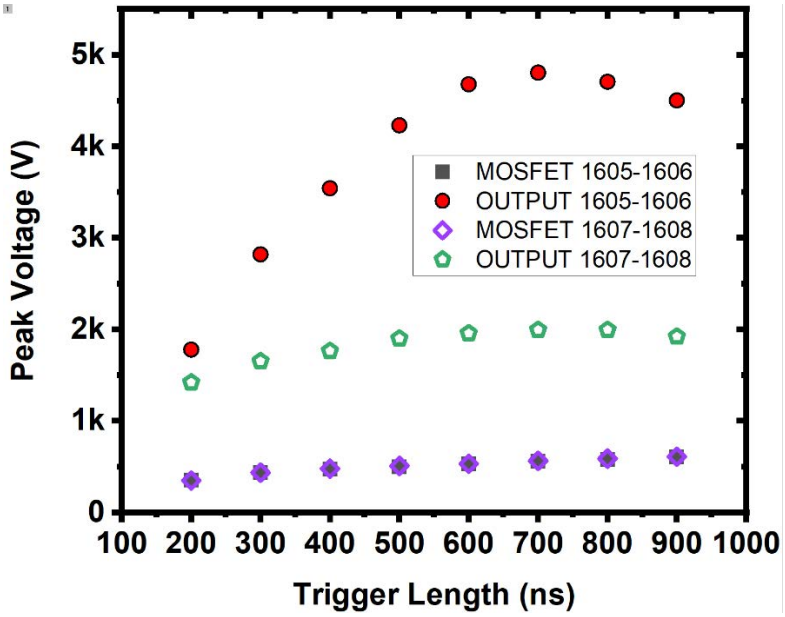


Figure 5.4.5. Output voltage and MOSFET voltage during charge extraction for two 14-stack diodes obtained from DSRD pulser optimized for 14-stack diodes.

The output obtained from 14-stack diode using circuit elements optimized for 14-stack diodes for different trigger lengths is shown in Figure 5.4.5. The figure shows that two 14-stack diode configurations performed significantly different under identical operating conditions, suggesting high variability among the diodes in the same series. It is important here to mention that the maximum peak voltage was obtained for the trigger length of 700 ns as expected from the simulation. In the figure, the MOSFET voltage during the charge extraction is also plotted to show that the circuit performed identically for both diode configurations.

5.4.5 *Summary of Significant Findings and Mission Impact*

(A) A systematic optimization of a 1×1 pulse generator based on the theory presented in the DEC2021 reporting period is presented. Based on the simulation, we optimized the circuit for a maximum output voltage of 14 kV using four 7-stack diodes.

(B) Two prototype pulse generators optimized for two 7-stack and four 7-stack diodes are successfully constructed using the optimization theory presented in the MSR JAN2022 report. Maximum peak outputs of 6.7 and 7.5 kV are obtained for a trigger length of 700 ns using a prime source voltage of 120 and 170 V, respectively, from the pulser optimized for four 7-stack diodes. This suggests that a high voltage gain can be achieved by implementing more powerful MOSFETs and/or MOSFET paralleling. Further, the reverse breakdown voltage of ~ 650 V per diode in the EG1600 series is estimated based on the DSRD pulser output using a single 7-stack diode.

(C) Successful construction and operation of a 2×2 DSRD-based IES pulse generator prototype has been completed, which meets or exceeds the required key performance metrics. Shown in Table 5.4.2 are the previous and current pulse

generator performance specifications in comparison to a similar 2×2 pulser developed by Kesar et al. [1] using DSRDs, and to that of a commercial off-the-shelf (COTS) DSRD pulser of similar space and weight developed by Megaimpulse (i.e., PPM-0731), which also uses DSRDs with silicon avalanche shapers (SAS) [2]. Although the Megaimpulse pulser utilizes a SAS with a <500 ps risetime (a threshold we do not intend to go below due to Commerce Controlled List limitations), it is interesting to compare the results of linear voltage gain and peak power of this system, to that of one that utilizes a SAS. The current permutation of the 2×2 DSRD-IES pulser developed by MIDE under the ONR OSPRES Grant is able to achieve a higher peak voltage and shorter risetime than DSRD-based pulsers reported in the literature of comparable space and weight as well as those commercially available. The ability to generate a linear voltage gain of 40.8 to produce over a Megawatt of peak power into a 50 Ω load while achieving a peak voltage output standard deviation of 2σ when operating at a PRF of at least 100 kHz, brings this technology to the forefront of viable options to potentially support the Naval afloat mission.

Table 5.4.2. Comparison of DSRD-based IES Pulse Generator Performance.

KPM	Units	MIDE - V1 Previous	MIDE - V2 Previous	MIDE – V3 Current	Kesar *et al.* SOTA	MI-PPM0731 COTS
V_{supply}	V	225	180	120	300	160
T_{ON}	ns	100	340	700	?	200
V_{peak}	kV	5.59	**7.35**	**6.7**	5	6.3
Gain	V/V	24.8	**40.8**	**55.8**	16.7	39.4
$\tau_{rise,20\text{-}90\%}$	ns	1.2	1.1	3.1	1.96	0.12
dV/dτ	kV/ns	4.66	6.44	2.16	2.55	**52.50**
FWHM	ns	2	5.48	6.90	2.27	0.35
PW	ns	5	7	7	3.5	2.5
Z_{LOAD}	Ω	50	50	50	50	50
P_{peak}	MW	0.625	**1.080**	**0.905**	0.500	0.794
E_{pp}	mJ	0.125	0.154		0.143	0.318
PRF_{max}	kHz	100	100		100	15
Burst	shots	100	100	*N/A*	*N/A*	100
	%	100	100	*N/A*	*N/A*	100
SD_{Vpeak}	σ	> 2	**> 2**	*N/A*	*N/A*	*N/A*
	%	96.5	**97.8**	*N/A*	*N/A*	*N/A*

(D) Discrepancies exist in the obtained pulser and device characterization data for different series combinations and different samples of 7-stack DSRDs, which may be attributed to the inconsistencies in their manufacturing process. Future work in the coming months include testing single 7-stack and two 7-stack diodes in pulser configurations with better MOSFETS or MOSFET paralleling to identify better diodes and increase the output voltage to >9 kV from the 1x1 pulser configuration. Future works also include the design and testing of 2×2 or higher configuration DSRD-based pulsers using more combinations of series-connected as well as parallel-connected DSRD stacks.

5.4.6 *References*

[1] https://www.onsemi.com/pdf/datasheet/nvh4l020n120sc1-d.pdf

[2] https://cms.wolfspeed.com/app/uploads/2020/12/C2M0045170P.pdf

5.5 All-Solid-State Sub-ns MW Pulse Generators with Semiconductor Sharpeners

(Gyanendra Bhattarai)

This sub-project is currently on hold as focus is directed toward Section 5.4. Please review the January 2022 MSR for the most recent project overview and status.

6 Thermal Management

6.1 Ultra-Compact Integrated Cooling System Development

(Justin Clark, Roy Allen, and Sarvenaz Sobhansarbandi)

6.1.1 *Problem Statement, Approach, and Context*

Primary Problem: A thermal management system (TMS) is required for cooling semiconductor-based pulse-power devices, with the goal of maintaining the semiconductor device temperature below 80 °C. The proposed system must increase cooling densities, while decreasing pumping power requirements, in-line with the SWaP-C[2] objective.

Solution Space: To achieve such high cooling densities, an ultra-compact TMS (UC-TMS) directly integrated onto the semiconductor is proposed. Such a design is capable of creating turbulent flow in order to enhance the heat transfer rate. The proposed UC-TMS is restricted to 1 cm^2 surface area, therefore, the required pumping power should be kept to a minimum. An array of micro-sized jet nozzles will provide a turbulent flow onto a microchannel section directly on the semiconductor device. The UC-TMS design will reach turbulency at a faster rate while requiring less energy consumption.

Sub-Problem: The turbulency formed from the array of nozzles creates an extreme pressure loss from the large amount of jet nozzles (over 200) and a flow diameter of 100 microns. The pressure must be sustained to enable proper cooling and circulation processes.

State-of-the-Art (SOTA): Integrated chip cooling is being widely used to dramatically increase the operational power of high voltage silicon-based power devices. However, the current SOTA devices include individual parts which attach to a high-power device, causing less interaction between the semiconductor and coolant, degrading the heat removal rate.

Objective: The proposed UC-TMS design is based on refining in-chip jet-impingement geometry through leveraging theory and a parametric evaluation of nozzle geometry and flow channel arrangements. A Si-base unit will be prototyped to maneuver a higher capacity of heat removal. Moreover, to sustain the pressure, the application of different working fluids is suggested. Several types of coolant will be simulated to determine effects from fluid density and viscosity.

Anticipated Outcome(s): To create a UC-TMS with the ability to rapidly remove 1 kW/cm^2 of heat. A design capable of such high heat removal can be implemented on many applications such as high-power batteries.

Challenges: The manufacturing techniques of the semiconductor devices have not yet been adopted for integrated chip cooling systems. The proposed compact design is restricted due to low tolerance of the manufacturing process, as this process must be capable of layering the silicon TMS onto the semiconductor.

Risks: With a system so compact, the pressure drop could be a large issue regarding the objective heat dissipation rate. An extreme pressure drop would potentially cause the coolant to flow backwards, causing less fluid-to-solid interaction.

6.1.2 *Tasks and Milestones / Timeline / Status*

(A) Design a Si base 1 cm^2 UC-TMS, applying manufacturing tolerances, to achieve a heat dissipation rate of 1 kW/cm^2. The design must be able to be produced by manufacturing techniques such as etching and lithographic layering processes. To confirm the device can be manufactured as proposed, each section of the model will be layered step by step. / MAY21–AUG21 / Completed

(B) Using the optimal design, perform ANSYS simulations using either water or Si-C nanofluid. Other fluid types may be researched as pressure drop is a large factor / JUL21–DEC21 / In Progress

(C) Improve design parameters and sizing to have a lower pressure drop while having a high heat dissipation capability. Prove simulations from previous literature to show capable design configurations with acceptable pressure drop and steady temperature. / NOV21–JAN22 / In Progress

(D) With proper simulation results, manufacture a prototype to begin experimental testing and evaluation / JAN22–APR22 / Upcoming

6.1.3 *Progress Made Since Last Report*

With the transition of roles in the development of the (TMS), training and review of previous data was completed to continue progress. The training consisted of becoming familiar with ANSYS Fluent and literature review from the previous researcher. The month of February was completely transitional, and no progress was made toward development of the (UC-TMS).

6.1.4 *Summary of Significant Findings and Mission Impact*

(A) From a literature review, similar designs were analyzed including a water-cooled, crossflow microchannel cooling system with various microchannel widths has been previously designed. The design achieved a simulated heat flux of 1.7 kW/cm^2 using 0.056 W of pumping power. Although this design is not the best fit when including the manufacturing constraints, the results using micro channel heat sinks are remarkable and design considerations are further analyzed. A similar design implemented the idea of having jets confined in their own individual spaces, experimentally reaching up to 900 W/cm^2 with 0.83 W of pumping power. A third design analyzed two types of heat sinks with flat and oblique angled fins which were experimentally tested with a constant heat flux of 100 W/cm^2. The temperature difference was from 60 °C to 35 °C which proposed giving the design more power. The oblique angled fins caused 20 percent greater heat transfer than flat fins.

(B) To achieve a higher quality mesh around the nozzles and microchannels, the nozzles element size was initially set to 20 microns, or until the shape of the nozzles were more profound in a cylindrical shape. The surface which connects to the

nozzles resulted with an element size of 15 microns and the nozzle sizing resulted in 13 microns. These values had to maintain an equivalent size to reduce the skewness and maintain mesh quality. Each surface with inadequate quality was selected and set to individual face sizing and is currently undergoing simulation.

To reduce the pressure loss while maintaining an effective turbulent flow produced by the jet nozzles, the microchannel fin designs did not effectively enhance the rate of heat transfer. The combination of micro channels and jet impingement caused too high of a pressure loss, causing the fluid to reverse its flow; therefore further enhancement of the UC-TMS will be based explicitly on jet impingement theory.

7 Pulse-Forming Networks

7.1 Diode-Based Nonlinear Transmission Lines

(Nicholas Gardner)

Attention on this sub-project is being entirely directed toward the preparation of manuscripts and an associated dissertation. A summary report will be provided in Summer 2022, and this will serve as a placeholder until this time. Please see the January 2022 MSR for the most recent summary and status.

7.2 Continuous Wave Diode-NLTL based Comb Generator

(Nicholas Gardner and John Bhamidipati)

7.2.1 *Problem Statement, Approach, and Context*

Primary Problem: When used as a pulse shaping network (PSN), diode-based nonlinear transmission lines (D-NLTLs) are promising solutions towards reducing the size, weight, and cost of RF and microwave sources on Navy afloat missions. However, D-NLTLs have a dynamic impedance, leading to signal/power reflection, standing wave generation, and return power losses at both the source–line and line–load interfaces, leading to difficulties in practical D-NLTL applications.

Sub-Problem: Design parameters for COTS high-frequency D-NLTL based comb generators capable of generating up to ~50 GHz output frequencies are limited to <1 Watt output powers, which is <0.1% of the power handling capability required for navy afloat missions. Using such metrics alone to design D-NLTLs capable of generating ~1–2 GHz frequency with capability to handle MW-order peak powers could potentially introduce design errors resulting in frequency/power prediction–measurement discrepancies on the order of a few hundred MHz.

Solution Space: Use a D-NLTL as a pulse shaping network (PSN) to convert continuous wave (CW) signals from low frequency–very high frequency (LF–VHF) bands (0.03 MHz–30 MHz) to the ultra-high frequency (UHF) band (0.3–3 GHz) at ones-of-MW peak power. Such an application will reduce impedance mismatch effects at the source–line interface by continuously oscillating D-NLTL impedance between the same two values. Use of MW D-NLTLs in the comb generator will push output frequency up to ranges required for Navy afloat missions.

State-of-the-Art (SOTA): Commercial-off-the-shelf (COTS) GaAs varactor diode-based monolithic microwave integrated circuit (MMIC) D-NLTL comb generators are capable of operating at input and output frequencies up to 600 MHz and 30 GHz, respectively. However, these comb generators are not capable of handling powers higher than 27 dBm (0.51 W). In-house pulsed D-NLTL prototypes have been shown to generate center frequencies of 0.2–0.5 GHz at kV amplitudes in a light-weight small-footprint circuit. Further D-NLTL network efficiency is hindered by a signal-dependent impedance characteristic to the network leaving reported efficiencies of RF content generation at 10% or less of incident pulse energy.

Objective 1: Design and demonstrate a high voltage D-NLTL based comb generator capable of L-Band Frequency generation and 0.1–5 MW power generation.

Objective 2: Increase D-NLTL network efficiency above the reported 10% threshold through use of CW sources suppressing impedance mismatch effects presented by the signal-dependent impedance characteristic to D-NLTLs.

Anticipated Outcome(s): A successful demonstration of improvements to impedance matching at the source–line interface using a CW signal measured as a reduction in signal amplitude loss between the source and D-NLTL.

Challenges: Nonlinear signal-dependent behavior provided by a reverse bias diode produces difficulties in predicting generated waveform behavior. Further D-NLTL performance is limited in both frequency and power generation by the availability and variety of COTS Schottky and epoxy diodes.

Risks: The reverse bias hold off potential (V_R) of a chosen diode limits the power generation capabilities of the system. If an excitation is used that exceeds V_R, diodes risk being damaged. Further reflections produced at the source–line interface caused by a signal dependent impedance can damage a CW source sensitive to such reflections.

7.2.2 *Tasks and Milestones / Timeline / Status*

(A) Demonstrate an ability of a CW excitation signal to reduce the source–line impedance mismatch effect on signal amplitude present in D-NLTLs when compared to a pulsed excitation signal, first through simulations and then by validating the results experimentally using low voltage (LV) and high voltage (HV) prototypes.

(A1) Show the potential to improve source–line impedance mismatch in simulation (Completed SEP21)

(A2) Experimentally demonstrate a low voltage (LV) prototype receiving a CW input (Completed SEP21)

(A3) Compare measured results with simulation behavior; comparison of results will be used to further refine D-NLTL simulation techniques (Ongoing)

(A4) Determine if there are improvements to system behavior if D-NLTL diodes are biased when receiving a CW input (Ongoing)

(A5) Demonstrate improvements to the source–line impedance mismatch in a LV prototype (Ongoing)

(A6) Demonstrate a HV prototype receiving a CW input (Completed NOV21)

(B) Demonstrate UHF – L-band (0.3–2 GHz frequency) generation with a CW D-NLTL.

(B1) Excitation of K100F and K50F D-NLTLs using a 700 MHz signal from the R&S amplifier (Completed NOV21)

(B2) Compare measurement with simulation to further refine simulation measurements. (**Ongoing**)

(B3) Simulate topologies capable of utilizing a bipolar pulse for CW applications. (**Ongoing**)

(C) Demonstrate UHF generation at single MW power levels with a CW D-NLTL.

7.2.3 *Progress Made Since Last Report*

(B2) Simulation study and experimental verification of K100F and K50F epoxy diode lines with 10–30 MHz (standard function generator) and 700 MHz (Rohde & Schwarz amplifier) CW sinusoidal inputs have been continued by varying the source and load resistance(s) to reduce the power reflection and improve the agreement between simulated and measured results. Thus far, the reflections have shown little improvement when constant source/load resistors were used.

7.2.4 *Technical Results*

(B2) D-NLTL lines based on the K50F and K100F epoxy diodes have been simulated and tested with 5 $V_{p\text{-}p}$10–30 MHz, and 80 $V_{p\text{-}p}$ 700 MHz CW sinusoidal excitation at varied source and load resistance(s) to minimize the 65% power reflection reported in the earlier cycle. The 25 MHz excitation resulted in shockwave generation with 3dB frequency >0.7 GHz with ~35% conversion efficiency. The 700 MHz excitation, however, has continued to show >60% power reflecting back to the R&S amplifier despite varying the resistances at source–line and line–load interfaces. Further simulation and experimental studied will be focused on developing a technique to match the continuously varying D-NLTL impedance with the load to minimize the reflected power.

7.2.5 *Summary of Significant Findings and Mission Impact*

(A) In the month of September, a LV prototype was given several continuous waveforms to observe initial behavior of a D-NLTL with a CW source. The LV D-NLTL demonstrated a capability to receive a CW based source. No effect on the source–line impedance mismatch was observed for the LV tests. During the month of November two high-voltage D-NLTLs based on epoxy diodes were tested using a sinusoidal waveform amplified by an R&S amplifier. Each D-NLTL demonstrated a capability to function with a CW source, however little to no effect was observed on the source–line impedance mismatch.

(B) Two high voltage D-NLTLs based on epoxy diodes of models K50F and K100F were tested using 25 MHz and 700 MHz sinusoidal sources. While formation of shockwave was noticed at 25 MHz excitation with ~35% conversion efficiency, pulse sharpening has been observed at low voltage (7 $V_{p\text{-}p}$) 700 MHz excitation in the K50F line alongside frequency doubling behavior (1.4 GHz output frequency) reported previously. However, the power reflection at ~70 $V_{p\text{-}p}$ remains >60% for both the lines at 70 $V_{p\text{-}p}$ excitation, resulting in <7% line efficiency. A technique to implement adaptive line–load impedance to minimize the power reflection needs to be developed.

7.3 Dynamically Tunable Multi-Frequency Solid-State Frozen Wave Generator

(John Bhamidipati)

7.3.1 Problem Statement, Approach, and Context

Primary Problem: Conventional RF generators such as vector inversion generators, relativistic magnetrons, etc. are limited by their frequency response (narrow bandwidth), form factor, and pulse conversion efficiency, limiting their application in Navy afloat missions.

Sub-Problem: Frozen wave generator, an alternative pulse generator capable of generating frequencies in the range of tens-of-MHz to sub-THz proposed by Forcier [1] and Best [2] is limited by the center frequency, form factor and the performance of the enabling switch.

Solution Space: Develop a single PCB-mount, all solid-state, mechanically/electronically tunable, multifrequency generator with dynamic tunability and chirp capability.

State-of-the-Art (SOTA): A photoconductive switch enabled FWG with adjustable frequency range between hundreds-of-MHz–2 GHz and pulse widths between 360 ps and 15 ns. [3]

Deficiency in the SOTA: Despite addressing the limitations of spark gaps used in the earlier FWG literature, the photoconductive switch-based FWGs suffer from laser systems whose size, weight, power, cost and cooling have not reached full maturity, and only the multi-switch embodiment has been demonstrated.

Risks: The proposed work implements a SiC-MOSFET based prototyping. MOSFETs are limited by their ns-order rise times, which could potentially limit the frequency response of the FWG. On the other hand, when the number of transmission line segments are increased, the MOSFET may not be able to switch all the segments simultaneously, resulting in distorted pulse wavefront. Furthermore, implementing lumped-element-based transmission lines can reduce the conversion efficiency.

7.3.2 Tasks and Milestones / Timeline / Status

1. Simulate a chirp-capable distribute-element transmission-line-based (DETL) 16-stage frozen wave generator (FWG) with balanced and unbalanced load configurations. [JUN-JUL 2021/complete]

(A) Demonstrate a SiC-MOSFET-powered FWG prototype on a custom-built PCB with Cree/Wolfspeed MOSFET, and 50 Ω coaxial cables and/or microstrip transmission lines capable of generating chirped pulse widths. [JUL–AUG 2021 / complete].

2. Simulate a lumped-element transmission line (LETL) based FWG with upto 12 segments to replicate results from the DETL-FWG simulations. [AUG-SEP 2021/complete]
3. Demonstrate a modular 4–8 stage SiC-MOSFET enabled FWG with lumped-element-based transmission lines with and without chirp capability. [SEP-OCT 2021/complete]

4. Design and test a 12-segment, MOSFET-enabled FWG prototype with dynamic pulse width tunability using lumped-element-based transmission lines [NOV–DEC 2021 / complete].
5. Perform root cause analysis to determine the causes for (i) pulse overlap demonstrated by the Gen1 LETL-FWG prototype under unbalanced load configuration, and (ii) consistent reduction in the peak voltage output of the pulse train output. [JAN-FEB 2022/in progress]

(B) Demonstrate motorized and/or electronically tunable DETL-FWG prototype with dynamic tunability capable of generating multiple center frequencies. [MAR-APR 2022]

7.3.3 Progress Made Since Last Report

(F) A Gen2 prototype of the 12-segment FWG with reduced footprint and updated MOSFET placement and has been designed, fabricated, and tested upto 400 V under balanced and unbalanced load configurations.

7.3.4 *Technical Results*

(F) To verify the hypothesis reported in the DEC2021 report for peak voltage reduction and pulse overlap issues in balanced and balanced load configurations, respectively, a 12-segment FWG with updated design has been implemented with modified switch position, optimized ground plane and reduced footprint (3″×12″ PCB), as shown in Figure 7.3.1. The updated design with new position of the enabling switch was expected to generate constant amplitude square pulses and minimize the pulse overlap of the reflected wavefront under unbalanced load configuration. However, it was not verified due to malfunctioning tunable elements. Another iteration of testing will be performed by replacing the components to verify the same.

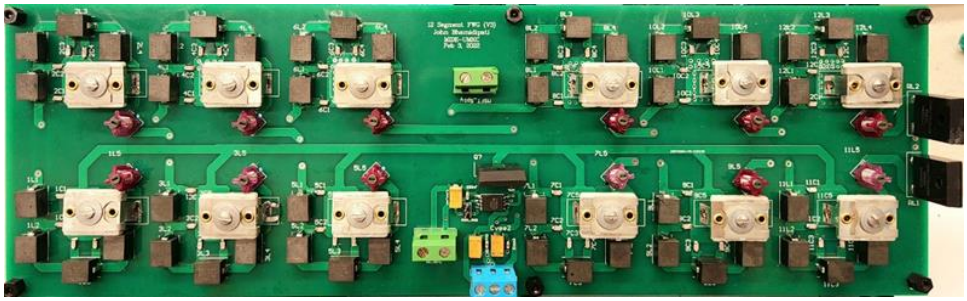


Figure 7.3.1. Gen2 12-segment dynamically tunable FWG prototype

7.3.5 *Summary of Significant Findings and Mission Impact*

(A) A 16-stage, chirp-capable, MOSFET-switched FWG was modeled and simulated in LTSpice with two load resistors, R_L and R_T, as shown in Figure 7.3.2. The model was designed for 125–500 MHz for illustration of the concept. Out of 16 transmission line segments in the simulation, 8 are used for generating the desired ON times, and the remaining 8 are required to introduce delays between the ON pulses (i.e., the second half of the pulse cluster is the mirror image of the first half).

The output voltage swings between +950 V and -950 V were noticed for charge voltages of $+V_0$=1.1 kV and $-V_0$= -1.1 kV with frequency content up to 4 GHz above 0 dB with highest magnitude obtained close to 500 MHz as shown in Figure 7.3.3.

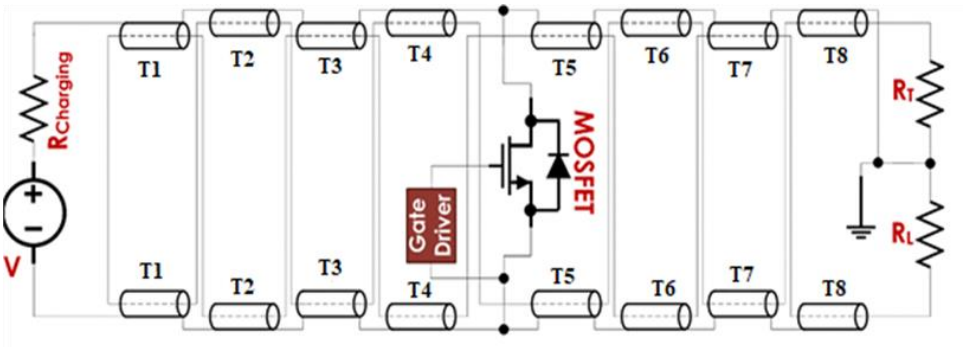


Figure 7.3.2. A sixteen-stage MOSFET-enabled modified FWG topology

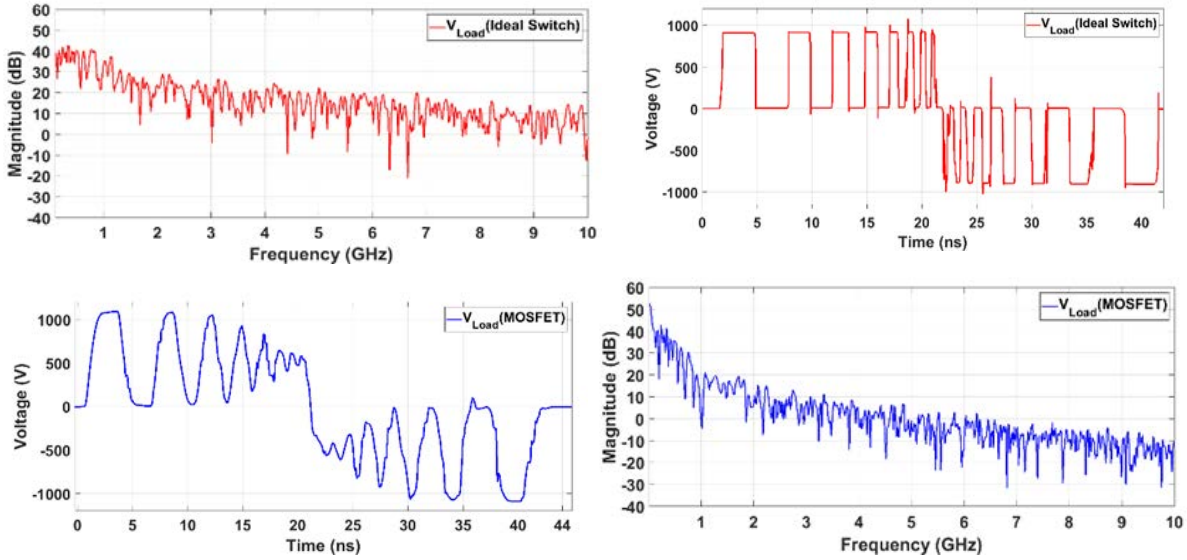


Figure 7.3.3. Simulation results showing the chirp generated from the sixteen-stage FWG circuit. **(a)** time domain output using an ideal switch, **(b)** frequency domain output using an ideal switch, **(c)** time domain output using a Si MOSFET, **(d)** frequency domain output using a Si MOSFET.

(B) A MOSFET-switched FWG prototype implementing coaxial transmission lines has been fabricated and tested with a goal to demonstrate a tunable pulse generator capable of demonstrating chirped pulse-. The primary operation of a FWG has been demonstrated with up to 8 transmission line segments under balanced and unbalanced load configurations. The experimental implementation results on pulse chirp were found to be in agreement with the simulation results. However, pulse overlap and deconstructive interference were observed in the 8-segment

configuration, which will be addressed using a different transmission line topology/configuration.

(C) 8- and 12-segment MOSFET-switched LETL-FWGs simulated in LTSpice XVII, with each LETL segment containing 8 LC cells, each with 81.25 nH-32.5 pF combination capable of generating 13.05 ns pulsewidth/delay showed +122 V and -150 V swing at 600 V charge voltages with a conversion efficiency of <50% when switched at 100 kHz PRR with 50% duty cycle. While the square-top, constant-amplitude, multi-cycle waveform has been demonstrated with 8-segment FWG, 12 segment version showed distortion in the waveform, potentially dude to the impedance line-load impedance mismatch. The simulation results are shown in Figure 7.3.4.

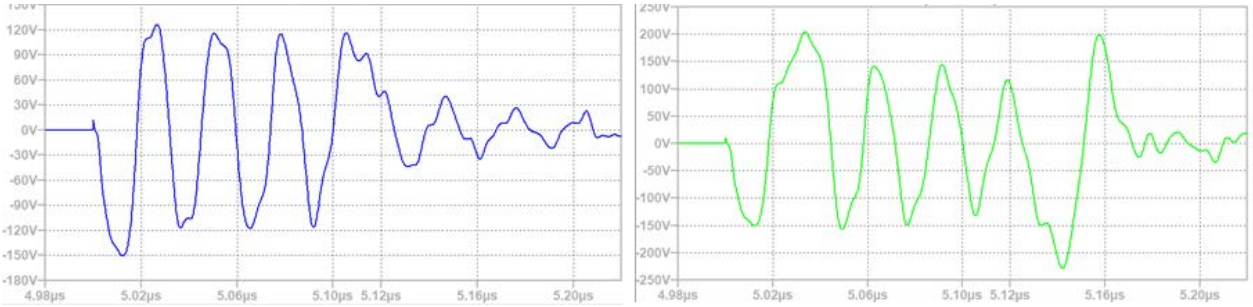


Figure 7.3.4. Load measurement of (a)an 8-segment LETL-FWG and (b) 12-segment LETL-FWG under balanced load at 600 V charge voltage.

In the 4-segment prototype, LC parameter combinations of 75nH-30pF and 110nH-43pF. Two transmission line segments were equipped with 6 cells of 75nH-30pF each and 6 cells of 110nH-43pF were used in the other two. These segments are capable of generating 9 ns and 12 ns, respectively. Figure 7.3.5 (a) shows the output pulse of the 4-segment FWG when load resistors $R_T = R_L$. Peak voltages of +75V and -100V have been observed in this prototype. However, when voltage was measured under an unbalanced load configuration, a lower voltage was seen alongside reflections and pulse overlap, as shown in Figure 7.3.5 (b). The lower voltage has been attributed to the power loss occurring at unmatched load resistor, and the pulse overlap due to the signal path optimization issues.

7.4 Pulse-Compression-Based Signal Amplification

(Feyza Berber Halmen)

7.4.1 *Problem Statement, Approach, and Context*

Primary Problem: Solid-state amplifiers, such as gallium-nitride-based high electron mobility transistors (GaN HEMT), can be used as high power microwave (HPM) sources to achieve the SWAP-C2 performance metrics necessary to support the cUAV Naval afloat mission. However, even the best high-power GaN HEMTs are limited to 2–3 kW of peak power, much lower than the 0.1 to 3 MW pulsed power available from traditional HPM sources such as travelling wave tubes (TWTs). Achieving a power density of 1 W/cm^2 at a distance of 10 m with a high gain (≥ 10 dBi) narrow-band antenna requires an input power increase of two to three orders of magnitude. Power combination methods to achieve an effective radiated power (ERP) at MW scale require 10 s to 100 s of GaN HEMTs, compromising the SWAP-C2 performance.

Solution Space: Pulse compression techniques are used to increase the peak power and lessen the pulse width in HPM applications. Adapting pulse compression at the GaN HEMT or any other SWAP-C2 compatible source output can achieve sufficient ERP with an optimal radiating element.

Sub-Problem**:** Pulse compression is generally used to generate a pulsed output with a high peak output power (P_{out_peak}) and a wideband frequency content from a DC input voltage. The main challenge lies in identifying a pulse compression technique that can be used to amplify a narrowband RF input signal. Some of the circuit elements for common pulse compression techniques, such as the saturable inductors used for energy storage in magnetic pulse compression (MPC), exhibit increasingly lossy behavior with high frequency. Another challenge will be to determine, if any, the operating frequency limits of the suitable pulse compression technique for high-frequency, high-power signals.

State-of-the-Art (SOTA): Large magnetic pulse compression (MPC) circuits (>1 m^3, >1000 lbs) have demonstrated peak output power up to a few GWs. Smaller versions (~0.125 m^3, 50 lbs to 100 lbs) can achieve 7.5 MW peak power [1].

Deficiency in the SOTA: Traditional MPC systems are large (few meters long), leverage huge transformers, and require liquid coolant such as transformer oil, which leads to undesirable system mass values of ≥1000 lbs. They are used for generating medium or high pulse power traditionally from DC or AC (50/60 Hz) high voltage supplies. There is no known example of high-frequency signal amplification utilizing MPC.

Solution Proposed: Developing a pulse compression circuit that will act as a high-power signal amplifier with a gain of ≥10. Utilizing magnetic pulse compression, or any other suitable pulse compression method, for high power signal amplification with source fidelity.

Relevance to OSPRES Grant Objective: Pulse compression will enable a size and cost efficient solution to high power signal amplification that will lead to HPM source development with optimal SWaP-C2 parameters.

Risks, Payoffs, and Challenges:

Challenges: Modeling pulse compression circuits for high-frequency operation can present a challenge. Pulse compression circuits are generally evaluated in SPICE simulators with low frequency AC / transient simulations. SPICE is a lumped-element model simulator and cannot solve for the distributed-element model required at high frequencies where the wavelengths become comparable to the physical dimensions of the circuit. Some circuit components, such as the saturable inductor in the MPC, are not available in SPICE or many other simulators and need to be modeled using behavioral models and proprietary material data. Pulse compression circuit modeling, especially at high frequencies, needs to be investigated.

Risks: Pulse compression methods are usually lossy in nature and generate a considerable amount of heat; therefore, designing a proper cooling method must be carried out, which may inadvertently increase the volume (size and weight) of the overall design.

7.4.2 *Tasks and Milestones / Timeline / Status*

(A) Milestone – -Demonstrate 2–3 times increase in peak power and compression gain using magnetic pulse compression (MPC) [*estimated completion by MAR22*].

1. Subtask – Model saturable inductors in LTSpice or Matlab/Simulink in order to be able to develop MPC simulations / NOV21 / Ongoing.
2. Subtask – Design of MPC circuit with RF input and simulation in LTSpice or Matlab/Simulink to evaluate the resulting amplification and frequency content. / [On hold until the saturable inductor simulation model is realized].
3. Subtask – Model the high frequency behavior of MPC circuit / NOV21 / Ongoing.
4. Subtask – Build and test the MPC prototype using bench top power supply / OCT–*DEC21 / Ongoing*.

(B) Milestone – Increase the compression gain available from MPC.

(C) Milestone – Build and test SWAP-c2 compatible high-frequency MPC prototype with GaN source.

7.4.3 *Progress Made Since Last Report*

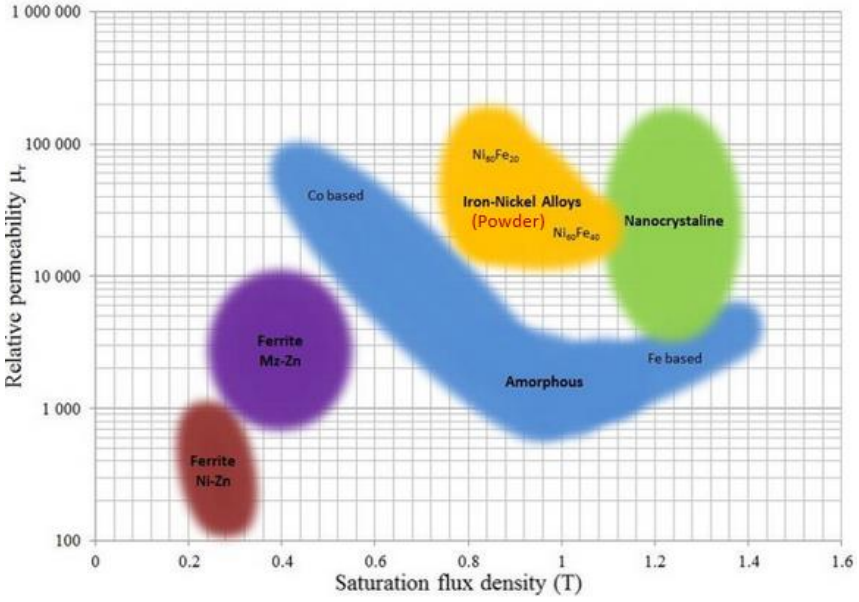
(A.3) Different magnetic core materials were investigated in order to determine the most suitable candidate for high frequency magnetic pulse compression. Collaboration on high frequency magnetic material development for MIDE MPC efforts was discussed with Kostas Research Institute (KRI) at Northeastern University.

7.4.4 *Technical Results*

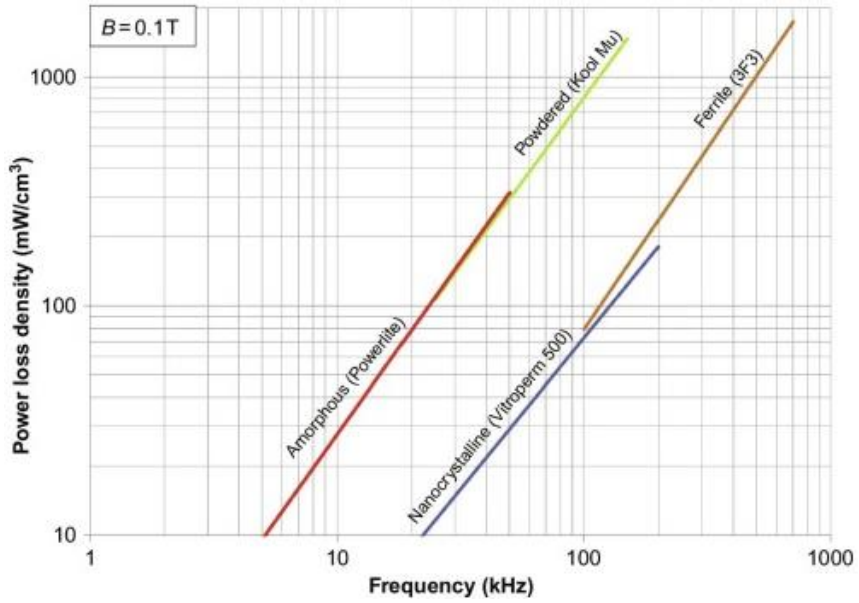
(A.3) Different magnetic core materials were investigated to determine the most suitable candidates for high-frequency pulse compression. As reported previously, such a core should have high resistance, narrow hysteresis loop, minimized eddy current area, and low saturation flux density (B_{sat}). High permeability (μ) and very sharp saturation characteristics are also preferred in order to minimize pre-pulse currents and resulting MPC gain loss.

Commercially available magnetic cores are grouped as 'soft' iron, silicon steel, amorphous, nanocrystalline, powder, and ferrites. 'Soft' iron cores are made of annealed iron that is easily magnetized and de-magnetized. They have high permeability and high saturation flux densities (B_{sat}) up to 2.16 T. Silicon steel is an alloy of iron and ~3% silicon, used in the form of stacked laminations, thin iron sheets coated with an insulating layer. Silicon is added to increase iron resistivity and laminations are used to reduce eddy current losses by limiting eddy current flow to narrow loops within lamination thickness of 0.3 to 0.7 mm. Amorphous cores, such as Metglas, are iron based alloys of cobalt, nickel, boron, silicon and manganese [2]. They are generally produced as thin ribbons or tapes, e.g., 12.5 μm thick, which are stacked like laminations to build a core. Such tape-wound cores have even less eddy current losses. Nanocrystalline materials are produced by annealing amorphous materials and have nanometer-sized grains. Powder cores consist of powdered metals or magnetic alloy powder with insulation coated grains or grains separated from each other by binder insulation. Therefore, resistivity is increased, and eddy currents are reduced. Such grain structures basically implement a distributed air gap which increases the power handling capability as the B-H curve slope is reduced, i.e., μ reduced. However, soft saturation behavior is observed, unlike the discrete air gaps cores. Powdered iron, carbonyl iron, hydrogen reduced iron and iron alloys with nickel, silicon etc. such as MPP, HighFlux(NiFe), KoolMμ are all powder cores. Ferrites are ceramic materials sintered out of iron oxides and combined with manganese zinc (MnZn) or nickel zinc (NiZn).

Important properties of amorphous, nanocrystalline, powder and ferrite cores, all of which are generally used for AC applications, are presented in Figure 7.4.1. Figure 7.4.1(a) depicts the permeability and saturation flux density of these materials. Nanocrystalline, and Fe-based amorphous cores generally have higher B_{sat} whereas ferrites have the lowest B_{sat} values. Silicon steel and soft iron, which are not included in the plot, have even higher B_{sat} values. In terms of low B required to saturate the core material at high frequency operation, ferrites seem to be the best option. Note that ferrites, especially NiZn ferrites, have the lowest permeability among these materials. High permeability is preferred in order to ensure that the unsaturated inductor presents a high impedance path and blocks any current flow to the next stage prior to saturation. However, one or two orders of magnitude difference between the unsaturated and saturated permeability should be sufficient to minimize the pre-pulse currents.



(a)



(b)

Figure 7.4.1. (a) Relative permeability and B_{sat} [2] and (b) Power loss density vs. frequency [3] for common magnetic core materials.

Figure 7.4.2(b) shows the power loss density versus frequency for some typical amorphous, nanocrystalline, powder and ferrite cores. The plot provides the general picture for the high frequency operation of the core materials. ‘Soft’ iron, not included in the plot, is not suitable for AC applications due to its high conductivity. Silicon steel, also not included, is generally used in 50-60 Hz power applications, and can operate up to 10

kHz with very thin steel laminations. Amorphous tape-wound cores, such as Metglas, are used in applications up to 100-200 kHz [4]. Nanocrystalline cores can operate at higher frequencies, e.g., up to a few MHz with Finemet [5]. Powder cores are various, and they are generally used from several hundred kHz to a few MHz. Carbonyl iron powder core, an outlier, is reported to work up to 200 MHz [6]. Typically, ferrite cores are preferred for high frequency MHz operation. As they are ceramic materials, they have very high resistivity and low AC core losses at high frequencies. MnZn ferrites are used in applications up to 1-2 MHz whereas NiZn can operate up to several hundred MHz [4]. Kemet Electronics Corporation advertises NiZn core operation up to about 300 MHz.

Data available from Kemet is presented in Figures 7.4.2 (a) and (b). Relative permeability for 1400L and 700L NiZn ferrites is less than 1000-2000 according to Figure 7.4.2 (a). Figure 7.4.2 (b) shows the impedance change with frequency for 700L NiZn core. The core frequency range is over 300 MHz with only one turn of winding, and it decreases with increasing number of turns, i.e., resonant frequency decreases due to increasing capacitance. These cores are intended for electromagnetic interference (EMI) applications and Kemet does not provide any additional information on its proprietary NiZn ferrite materials, such as the permeability, saturation flux density or B-H curves. More research is needed into commercially available high frequency NiZn cores.

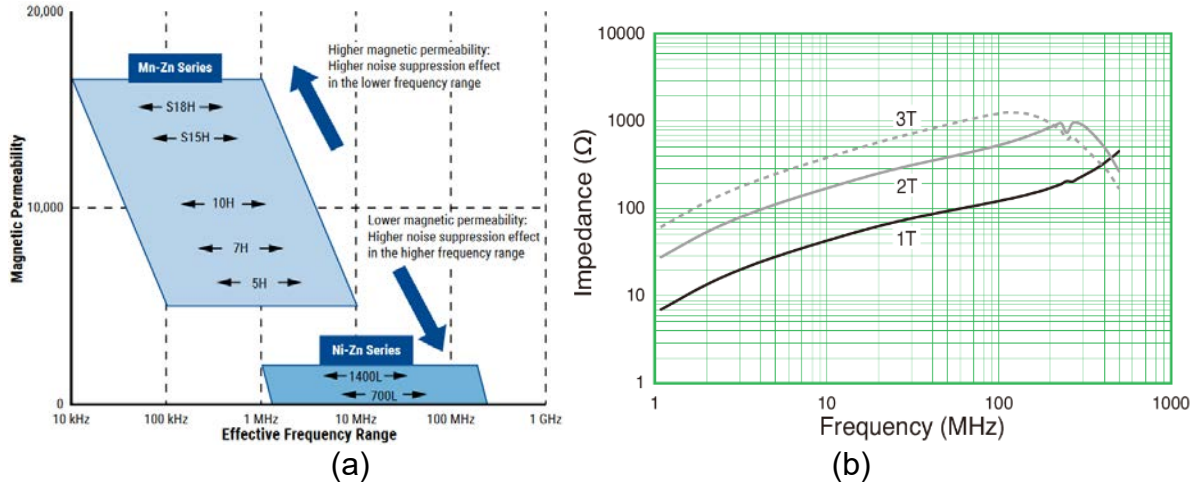


Figure 7.4.2. Kemet Electronics Corporation (a) NiZn cores magnetic permeability and effective frequency range and (b) 700L MnZn core impedance change with frequency [7]

Based on our current data, commercially available magnetic cores are limited to 300 MHz and this sets the upper frequency limit for the high frequency MPC circuit. Collaboration on high frequency magnetic material development is being considered with Kostas Research Institute (KRI) at Northeastern University. Different material options were discussed in a meeting with Vince Harris and Yunume Fitchorova of KRI. Other than NiZn, yttrium iron garnet (YIG) has been suggested for the high frequency MPC application due to its low dielectric and magnetic losses. With additives to YIG, magnetic core material with low B_{sat} at mT level, which is ideal for GHz range MPC, and relatively low permeability of ~50-150, tolerable for the MPC circuit, can be developed. KRI is also able to deliver

the magnetic core as toroid, which is not available for YIG materials. A statement of work is being drafted by KRI based on the discussions.

7.4.5 *Summary of Significant Findings and Mission Impact*

(A) Initially a basic 2-stage magnetic pulse compression circuit was built and tested with DC input to better understand the MPC principles and considerations such as inductor sizing, pre-pulse currents and inductor saturation. Next, saturable inductor modeling was realized in LTSpice with inductor flux expression and Chan model methods available. Prior to MPC system simulations, magnetic core losses were investigated and core selection constraints were determined based on the core losses and high frequency MPC design considerations. Next, different magnetic core materials were investigated to determine the most suitable candidate for high-frequency MPC. As reported previously, such a core should have high resistance, narrow hysteresis loop, minimized eddy current area, and low saturation flux density (B_{sat}). High permeability (μ) and very sharp saturation characteristics are also preferred in order to minimize pre-pulse currents and resulting MPC gain loss. Commercially available magnetic cores are grouped as 'soft' iron, silicon steel, amorphous, nanocrystalline, powder, and ferrites. NiZn ferrites are the best option for the high frequency MPC application as they have the highest operating frequency of up to 300 MHz. Relative permeability of NiZn ferrites changes between 100 to 1000, which is sufficient for this application. NiZn B_{sat} at ~0.2-0.4 T is among the lowest for commercial magnetic materials, which is beneficial for saturation at higher frequencies with low voltage-time products. Collaboration on high frequency magnetic material development is being considered with Kostas Research Institute (KRI) at Northeastern University. YIG-based toroid core development for high frequency MPC has been suggested by KRI.

7.4.6 *References*

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8 Antenna Development

8.1 Tradespace Analysis of an Array of Electrically Small Antennas (ESAs)

(Bidisha Barman and Deb Chatterjee)

8.1.1 *Problem Statement, Approach, and Context*

Primary Problem: Determine the extent to which the physical aperture size of an antenna array, composed of patch elements, can be reduced, while maintaining performance in peak power density, bandwidth, and electronic beam steerability over the UHF range (0.4–1 GHz), compared with present-art high-power-microwave-capable antenna arrays.

Solution Space: An array of patch antenna elements whose feed, two-dimensional shape, and relative placement (i.e., intra-, and inter-element design) allow for the physical aperture size to be reduced by more than 20% compared with the present-art.

Sub-Problem: To overcome scan blindness (as the main beam is electronically steered), due to the excitation of surface waves (SW). (Note: scan blindness is a common phenomenon in electrically small microstrip patch antenna arrays).

State-of-the-Art (SOTA): Horn, reflector, Vivaldi, valentine, etc. are some of the commonly used ultra-wideband (UWB) antenna elements in a phased array for high-power microwave (HPM) transmissions.

Deficiency in SOTA: Large physical aperture size of the antennas.

Solution Proposed: Using electrically small antennas (ESAs) as array elements and optimizing their performance in terms of both near-field (bandwidth) and far-field (directivity) parameters, followed by arrangement of the ESAs in suitable lattice structures (preferably, hexagonal/triangular) to reduce the overall array aperture area. Using stochastic and machine learning (ML) algorithms to optimize antenna element and array performance.

Relevance to OSPRES Grant Objective: Provides design and optimization guidelines for UWB ESA elements, especially coaxial probe-fed microstrip patch antennas, and arrays for HPM applications.

8.1.2 *Tasks and Milestones / Timeline / Status*

(A) Develop an Array Pattern Tool in the context of lightweight calculations of large antenna arrays / JAN–MAY 2021 / Completed code.

(B) Investigate the effects of array aperture area reduction on different array parameters (such as gain, beamwidth, electronic beam steerability) and present a comparative study of antenna array parameters as a function of array aperture area / JAN–MAY 2021 / Completed investigations of arrays on infinite ground planes.

(C) Build minimum viable validation prototypes of single ESA elements on substrates that have good power handling capabilities for HPM transmissions at UHF range (such as polyethylene, FR-4, TMM-10i, TMM-6) / JAN 2021–MAR 2022 / Ongoing designing of custom connectors for feeding ESAs in the UHF range.

(D) Optimization of ESA (single element) performance using ML based stochastic search algorithms / JUN 2021–MAR 2022 / Ongoing ML-based multi-objective-optimization (MOO) of ESA elements.

(E) Build minimum viable validation prototypes for arrays of ESA elements/ JUN 2021–MAY 2022/ Ongoing designing and characterization of a 4×4 square array of ESAs in the UHF range.

(F) Optimization of array performance using ML algorithms / SEP 2021–MAY 2022 / Ongoing ML-based MOO of antenna array parameters.

8.1.3 *Progress Made Since Last Report*

(E) Build minimum viable validation prototypes for arrays of ESA elements:

a. Designed and performed time-domain analysis of a 4×4 square array of ESA elements in the UHF range (0.7–1.05 GHz), subjected to different monopolar pulses.

8.1.4 *Technical Results*

(E) Build minimum viable validation prototypes for arrays of ESA elements:

A 4×4 square array composed of wideband, coaxial-probe-fed, microstrip patch, ESA elements, is modeled for operation in the UHF range (0.7–1.05 GHz) via CST Microwave Studio. The schematic of the array is shown in Fig. 8.1.1.

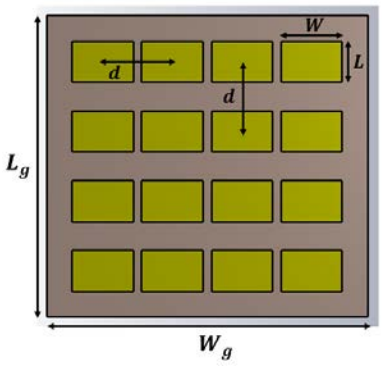


Figure 8.1.1. Front view of the 4×4 square array of wideband microstrip patch ESA elements in the UHF range (0.7–1.05 GHz) with $L_g = 59.17$, $W_g = 63.20$, $L = 8.05$, $W = 12.08$, $d = 13.70$ (all dimensions are in cm).

A maximum boresight gain of 16.86 dBi is achieved using the array model. The boresight gain of the array, as a function of frequency, and its radiation pattern at 900 MHz are plotted in Fig. 8.1.2.

To understand the effect of various input signals on the electric field, the array elements are subjected to different input pulses. For the study, three different monopolar pulses, as illustrated in Fig. 8.1.3, have been considered. The simulated time- and frequency-domain electric fields, at 2 m from the array, are obtained via CST, and are shown in Fig. 8.1.4 and Fig. 8.1.5 respectively.

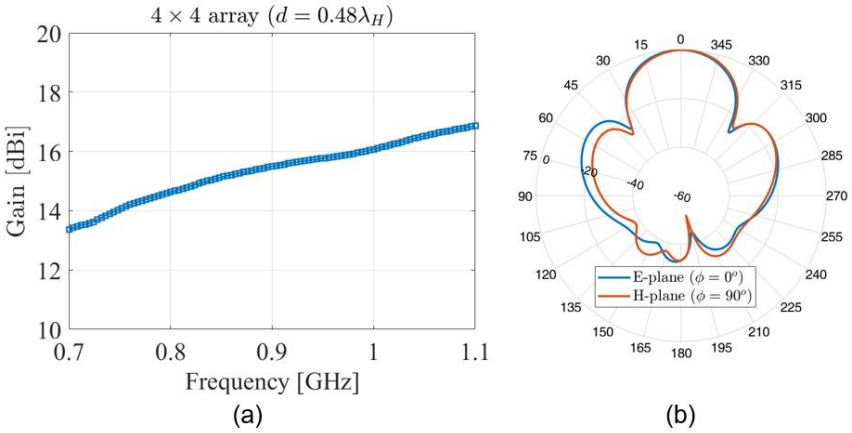


Figure 8.1.2. (a) Boresight gain of the 4×4 array as a function of frequency and (b) E- and H-plane radiation patterns of the array at 900 MHz.

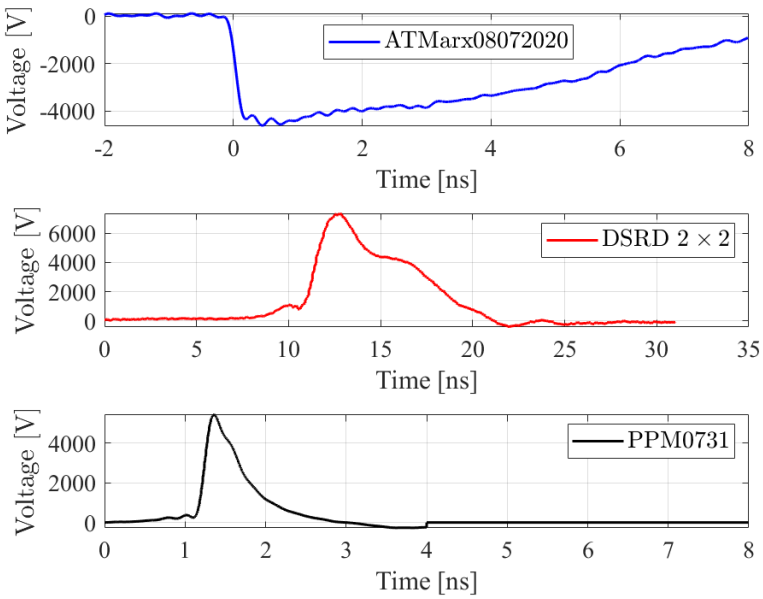


Figure 8.1.3. Input pulses used for the time-domain analysis of the 4×4 antenna array.

Table 8.1.1. Optimized microstrip patch antenna array E-field response at 2 m under different excitation patterns.

Excitation Pattern	E-peak [V/m]	rE/V
ATMarx08072020	3660.6385	1.587
DSRD 2 × 2	1098.3128	0.9974
PPM0731	5948.9347	2.199

The peak time-domain electric field and the corresponding rE/V values, in each case, are presented in Table 8.1.1. It can be observed that the PPM0731 pulse results in the best rE/V value and is most suitable for this ESA array.

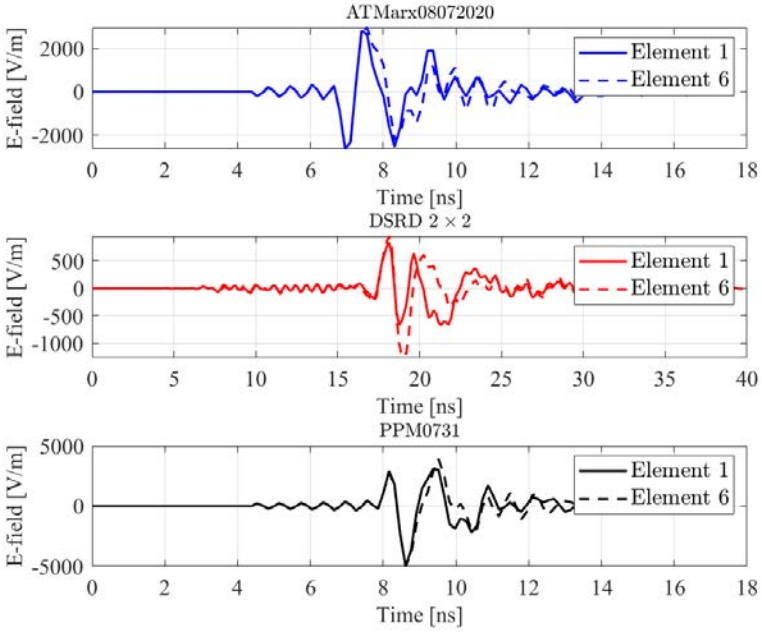


Figure 8.1.4. Time-domain electric field, at 2 m from the array, when elements 1 and 6 are excited by the monopolar pulses shown in Figure 8.1.3.

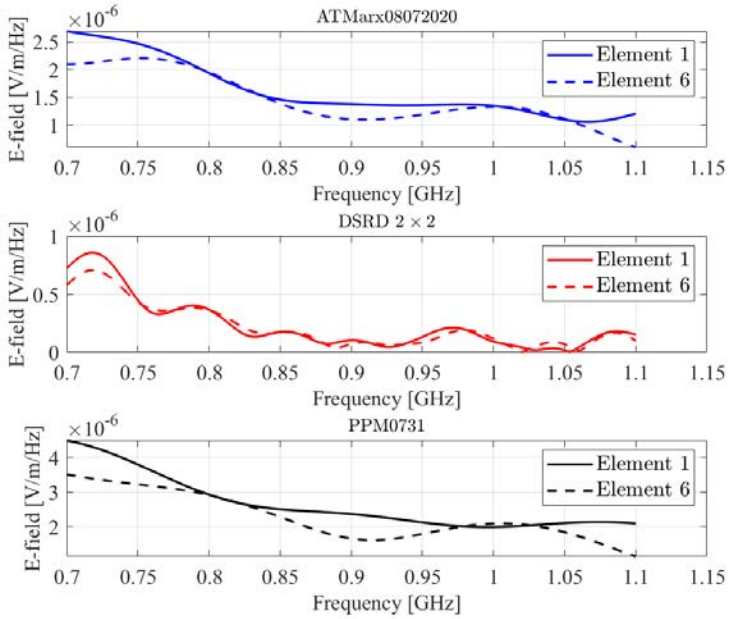


Figure 8.1.5. Frequency-domain electric field, at 2 m from the array, when elements 1 and 6 are excited by monopolar pulses shown in Figure 8.1.3.

8.1.5 *Summary of Significant Findings and Mission Impact*

(A) Developing Array Pattern Tool for large arrays calculations:

A MATLAB code has been developed for faster approximation of the radiation pattern of a linear/planar array of any size and composed of any type of antenna elements. The

code requires the center element pattern of a small array (say, 3×3) composed of the same type of antenna elements, desired lattice arrangement, and total number of array elements, as user inputs. This work will be included in future publications.

(B) Investigate the effects of array aperture area reduction on different array parameters:

The effect of different array aperture area and lattice arrangements on the array parameters (such as array gain, beamwidth, electronic beam steerability, etc.) have been reported for arrays modeled on infinite ground planes (DEC 2020 ONR-OSPRES-Grant MSR). The results show that, with 30% reduction in the aperture area ($\approx 50\%$ reduction in # of elements), the gain drops by < 3.5 dBi without any scan blindness spotted as the main beam is steered from boresight to $\pm 60°$ in the $640-990$ MHz range.

The array parameters for large arrays ($\geq 15 \times 15$) on finite ground planes could not be computed using the commercial EM solvers (FEKO and CST) due to excessive memory and time consumption. This work will be resumed after developing a method to estimate array performances on finite ground planes, either through ML or conventional approaches.

(C) Build minimum viable validation prototypes of single ESA elements:

Investigated different bandwidth enhancement techniques applicable to single layer microstrip patch ESAs:

a. Method I: Bandwidth enhancement by strategically placing the coaxial probe along 2/3rd of the patch diagonal – This method is proposed and experimentally validated using prototypes manufactured on TMM-6 and TMM-10i substrates at $2.5-5$ GHz. Antennas have been modeled on various substrates (polyethylene, G10/FR-4, TMM-10i) at the UHF range ($0.6-1$ GHz) and are being considered for manufacturing.
b. Method II: Coaxial probe-fed U-slot loaded rectangular microstrip ESAs – A prototype is manufactured on a G10/FR-4 substrate ($0.9-1.3$ GHz) and tested.
c. Method III: L-probe-fed U-slot-loaded rectangular microstrip ESAs – An antenna has been modeled on a TMM-4 substrate that operates in the $0.52-1.17$ GHz range ($\approx 77\%$ 2:1 VSWR bandwidth). Due to the fabrication complexity of the L-probe proximity coupled feed, this antenna will not be manufactured.

(D) Optimization of ESA (single element) performance using regular, and ML based stochastic search algorithms:

Investigated the bandwidth enhancement of the coaxial probe-fed microstrip patch antennas, using regular and ML based stochastic search algorithms (GA, PSO, and Simplex methods), by optimizing the feed-probe location and ground plane shape and size. Compared to regular search algorithms, ML algorithms are found to be less computationally intensive (in terms of time and memory consumption).

(E) Build minimum viable validation prototypes for arrays of ESA elements:

A wideband 3×3 array (2.5–5 GHz) and a narrowband 2×2 array (900 MHz) of coaxial probe-fed microstrip patch ESA elements, on 0.25-inch-thick TMM-10i substrates, have been manufactured. The S_{11}-parameters of the individual elements, in each array prototype, have been tested, with good agreement achieved between the simulated and

the measured data. Modeling and characterization of a 4×4 square array, of wideband ESA elements in the UHF region, has been initiated for future prototyping.

(F) Optimization of array performance using ML algorithms:

Completed optimization of inter-element spacings in a 4×4 square and a 10-element hexagonal array in the upper S-band (2.5-5 GHz) with the objective of array boresight gain enhancement. With this knowledge, multi-objective optimization of a 5×5 array, by seeking the best array design parameters, including inter-element spacing, ground plane size, feed-probe locations, etc., in the desired UHF range (0.6-1 GHz), has been initiated.

8.2 Tradespace Analysis of Ultra-Wide-Band (UWB) Koshelev Antenna

(Tyler Williams and Kalyan Durbhakula)

8.2.1 *Problem Statement, Approach, and Context*

Primary Problem: Determine the extent to which the physical aperture area of an antenna array, composed of antenna elements, can be reduced, while maintaining performance in peak power density, bandwidth, and electronic beam steerability over the UHF range (0.4–1 GHz), compared with present-art high-power-microwave-capable antenna arrays.

Solution Space: The Koshelev antenna has a unique design that is capable of generating an UWB response by effectively merging radiation characteristics from a transverse electromagnetic (TEM) horn antenna with exponentially tapered flares, an electric monopole, and magnetic dipoles over a wide frequency range [1]. This opens up an opportunity to investigate the design parameter space and understand parameter effects on impedance bandwidth, radiation pattern, electric field distribution, and other metrics via a tradespace study.

Sub-Problem:

(i) The integration of an impedance transformer to a single element Koshelev antenna to simulate and test the combined (transformer–antenna) performance is currently not feasible using commercial EM simulators.

(ii)The total surface currents on the Koshelev antenna over the desired frequency range arising from the present positioning of TEM exponential flares, an electric monopole, and magnetic dipoles is not yet clearly understood.

State-of-the-Art (SOTA): The balanced antipodal Vivaldi antenna (BAVA) is considered to be the SOTA antenna element due to its exceptional 20:1 impedance bandwidth ratio as well as the ability to handle tens-of-MW input power.

Deficiency in the SOTA: The BAVA design parameter space has been exhausted over the past couple of decades. The physical aperture area still remains very large and there is no viable path through tradespace study for further physical aperture area reduction.

Solution Proposed: Design, simulate, validate, and perform a tradespace study on the important design parameters of the Koshelev antenna array that effectively reduce its

physical aperture area while maintaining its UWB properties, in both the frequency and time domains. The Koshelev antenna has been shown in the literature to withstand higher voltage levels (over 200 kV peak voltage), thereby making it a viable antenna element for detailed tradespace study and analysis.

Relevance to OSPRES Grant Objective: From the literature, it was shown that the Koshelev antenna can handle high input voltages (and therefore high power with 50 Ω input impedance), which satisfies the specific OSPRES objective related to high input voltage/power. In addition, this work can yield a center-frequency-dependent, bandwidth-controlled, and electronically steerable Koshelev antenna design that can be quickly modified to the spectrum properties of the ultra-fast rise time input pulse.

Risks, Payoffs, Challenges:

(i) The electrical size of the Koshelev antenna is approximately λ/4 at its lowest operating frequency. Further reduction of electrical size to λ/10 could considerably reduce frequency dependent gain, thereby decreasing the power spectral density.

(ii) Payoffs include the development of a library of antenna metrics data for different shapes and sizes of the individual parts within the Koshelev antenna.

(iii) The large electrical size (>5λ) of the Koshelev antenna at its highest operating frequency poses huge computational challenges.

8.2.2 *Tasks and Milestones / Timeline / Status*

(A) Complete literature search to identify and list antenna elements that satisfy UWB properties and HPM requirements, and down-select accordingly / NOV–DEC20 / Complete.

(B) Complete initial design, simulation, and validation of Koshelev antenna [1] / JAN21 / Complete.

(C) Perform a preliminary parameter study to identify design parameters that considerably reduce the physical aperture area / FEB–MAR21 / Complete.

- Milestone: Using FEKO and/or CST electromagnetic (EM) simulators, reduce the physical aperture size of the Koshelev antenna to at least 95% of its original design and show minimal to no variation in the bandwidth, gain and increased aperture efficiency / Complete.

(D) Determine the full-width half-maximum (FWHM) and ringing metrics from the envelope of the time domain impulse response ($h_{rx/tx}(t, \phi, \theta)$) in receive or transmit mode / MAR–APR21 / Complete.

- Milestone: Produce a generalized code that calculates the impulse response envelope of the Koshelev antenna and plots the rate of change in FWHM and ringing values as a function of physical aperture size.

(E) Perform tradespace studies on design parameters such as feed position (*F*), length (*L*), and alpha (α). Obtain various antenna metrics data, compare, and analyze / MAR21/ Complete.

- Milestone: Identify Koshelev antenna design parameters that significantly alter the bandwidth, rE/V, peak gain over the desired bandwidth, and aperture efficiency.

(F) Reduce Koshelev antenna aperture size (H×W) to equal to or less than 90 mm × 90 mm, equal to that of the SOTA BAVA, for direct antenna metrics comparison / MAR–APR21 / Complete.

- Milestone: Provide a recommendation on the optimum design parameters and the resulting metrics, with comparison to SOTA BAVA. The optimized design parameters must yield 900 MHz ± 200 MHz bandwidth, rE/V greater than 1, peak gain around 3 dBi at 900 MHz, aperture efficiency equal to or greater than 130% at 900 MHz.

(G) Using the optimized model from (F), build various array simulation models/topologies to perform a tradespace study and report tradeoffs between array antenna metrics such as center element reflection coefficient (S11) value, gain vs theta at constant phi, physical aperture area, aperture efficiency, and rE/V / MAY–JULY21 / Complete.

- Milestone: Develop/showcase an optimized Koshelev array model that exceeds an aperture efficiency of 130% with a high rE/V.

(H) Perform literature search to investigate, understand, and determine the applicability of special electromagnetic (EM) techniques to the antennas under consideration. / JAN–APR21 / Complete.

(I) Explore impedance taper (microstrip based and coax based) designs that can interface well (both mechanically and electrically) to transition the signal from a coax cable to the input of the Koshelev antenna element / JULY21–AUG21 / Complete.

- Milestone: Recommend the optimum impedance taper design (with minimum reflections and maximum power transfer) with the optimum dimensions to successfully convert the high-voltage, short-rise time input signal from a coax cable to the feed of the Koshelev antenna array.

(J) Study response from optimized Koshelev antenna array when excited with different monopolar, differential, and bipolar pulse signals of significant interest / AUG21–NOV21 / Ongoing.

- Milestone: Provide a table comparing the Koshelev antenna array response metrics and narrow down the suitable pulse signals. Recommend (if any) changes to the downselected pulse signal(s) that can further improve the radiation efficiency, and/or transient gain.

(K) Investigate and analyze the response from the optimized Koshelev antenna array when excited by different excitation patterns / DEC 21 / Complete.

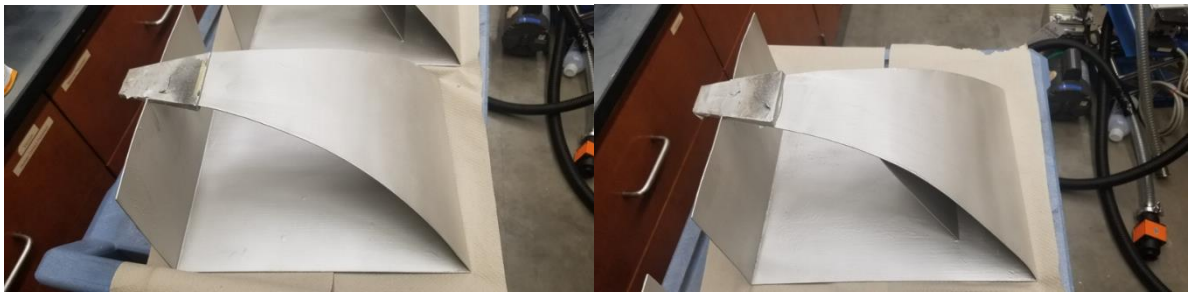
- Milestone: Compare and recommend an appropriate excitation method to yield maximum boresight gain, maximum half-power beamwidth (HPWB), minimum side lobe levels, and maximum electric field, rE/V.

(L) Prototype single element Koshelev antenna and test for reflection coefficient, gain as a function of frequency, radiated electric field at 1-m, 2.5-m, 5-m and 10-m (if feasible) distances. / AUG21–MAR21 / Ongoing.

- Milestone: Report measured data and recommend any improvements to the fabrication/prototyping/testing methods.

8.2.3 *Progress Made Since Last Report*

(L) In addition to the Cu foil variant, the optimized single element Koshelev antenna is 3D printed, smoothed with sanding and a filler primer, and metallized with nickel paint initially. Later, a layer of silver paint is applied to improve the conductivity values to achieve improved reflection values. Four-point linear resistivity measurements were carried out to determine the resistivity and conductivity values for both nickel paint followed by silver paint.



(a) (b)

Figure 8.2.1. Two halves of the silver painted Koshelev antenna ready for assembly. (a) Bottom half and (b) Top half.

8.2.4 *Technical Results*

(L) Four-point linear resistivity tests were run on samples with nickel and silver paints. Nickel was found to have a conductivity of ~601 S/m at a thickness of 60 μm and silver had a conductivity of 3577 S/m at a thickness of 50 μm. The 4-point van der Pauw method was used to verify the results for silver.

Table 8.2.1. Resistivity test results for a single coating of the silver and nickel paints.

Coatings	Thickness(μm)	Resistivity (Ω*m)	Conductivity (S/m)
Silver	50	2.79E-04	3.57794E+03
Nickel	60	1.66E-03	6.01095E+02

8.2.5 *Summary of Significant Findings and Mission Impact*

(A) An extensive literature search on various UWB antenna elements has resulted in finding three promising options. The down-selected elements are the Koshelev, Shark, and Fractal antennas, which will be extensively studied using their individual design parameter space, which could result in physical aperture area reduction of the

single antenna element. Later, the single antenna element will be converted into a planar array.

(B) Initial validation of the Koshelev antenna simulated using CST software agreed well with the antenna metrics published in the open literature [1]. A UWB bandwidth response (10:1 bandwidth) and rE/V > 1 has been observed from our initial simulations of the Koshelev antenna. This validation ensured that the Koshelev antenna can be subjected to further tradespace studies to understand its performance followed by optimizing the design according to OSPRES grant requirements.

(C) The initial tradespace study and analysis of the Koshelev antenna design yielded promising outputs to carry forward the investigation. A comparison of important antenna metrics between the Koshelev antenna in [1] and aperture reduced Koshelev antenna are shown in Table 5.2.1 of the APR 21 MSR.

(D) An in-house code has been developed to calculate important UWB time domain antenna metrics such as full-width half maximum (FWHM) and ringing. These metrics have been calculated using in-house MATLAB code using the excitation voltage and radiated electric field information obtained from CST simulations. FWHM and ringing antenna metrics help with assessing or characterizing an antenna's UWB response.

(E) The tradespace study of feed position provided a deeper understanding of how its position impacts the S11 value bandwidth. An optimum value for feed position i.e., $F = 1/20 < L < 1/10$ is recommended to achieve maximum bandwidth. The tradespace study of the antenna length (L) is straightforward. A longer antenna length will radiate better at lower frequencies. However, physical size restrictions/requirements must be kept in mind in determining the antenna length. Finally, a larger α value (>120°) is recommended to avoid unnecessary reflections from the electric monopole.

(F) From a thorough tradespace study, the aperture size of the Koshelev antenna (single element) is determined to be 90 mm × 100 mm in order to achieve desired antenna metrics performance proposed in the milestone. All metrics described in the milestone have been successfully achieved except the desired bandwidth (200 MHz on both sides) at 900 MHz center frequency. The bandwidth achieved is 900 ± 100 MHz.

(G) The physical aperture area of the Koshelev array antenna largely depends on the interelement spacing and the shape of the array. We were able to determine that the diamond topology is the optimum shape for the Koshelev array antenna. We were also able to obtain similar gain profile (peak gain and pattern) from making certain elements within the array passive (off state) when compared against regular active array (all elements in on state). From the non-symmetric interelement spacing values, we found that S_y has the least effect on the output; therefore a small spacing value can be chosen to reduce the physical aperture area of the Koshelev array.

(H) The literature search on the special EM techniques expanded our knowledge and opened the door to opportunities to apply some of those techniques to the antennas under study. EM techniques such as non-symmetric and non-square array topologies have been applied to the development and study of the Koshelev array antenna.

(I) The first impedance taper design under consideration has shown good S11 values (< -10 dB) over the frequency range of interest. In addition, we have shown that the shape of the pulse can be easily retained at the output of the taper with less than 5% amplitude losses.

(J) The Koshelev antenna array response from feeding a monopolar vs bipolar signal has demonstrated a clear winner: that is, a bipolar signal will radiate at least 10 times better than a monopolar signal. A comparison of the frequency spectrum of the radiated electric field from the optimized Koshelev antenna array between different monopolar pulse sources has identified the 'MI0731' pulse to be the optimum pulse.

(K) The uniform and Gaussian excitation patterns were determined to be the optimum excitation patterns. Selecting these excitation patterns would result in maximum electric field at boresight.

(L) Silver paint is shown to be the best conductive paint available for metallizing 3D printed antennas.

8.2.6 *References*

[1] Gubanov, V. P., et al. "Sources of high-power ultrawideband radiation pulses with a single antenna and a multielement array." *Instruments and Experimental Techniques* 48.3 (2005): 312-320.

8.3 Machine Learning Inspired Tradespace Analysis of UWB Antenna Arrays

(Sai Indharapu and Kalyan Durbhakula)

8.3.1 *Problem Statement, Approach, and Context*

Primary Problem: Determine the extent to which the physical aperture area of an antenna array, composed of antenna elements, can be reduced while maintaining performance in peak power density, bandwidth, and electronic beam steerability over the UHF range (0.4–1 GHz), compared with present-art high-power-microwave-capable antenna arrays.

Solution Space: Fractal antennas possess exceptional fidelity factor values (>0.9), which describe how well the shape of the input pulse is retained at an observation point in the far-field. Their high degree of freedom provides an opportunity to develop systematically modified patch shapes, which in turn leads to improved bandwidth while retaining high fidelity factor values. Machine learning (ML) can be leveraged to predict the antenna array response for an arbitrary design parameter space upon sufficient training and validation.

Sub-Problem:

(i) Fractal antennas generate omni-directional radiation patterns in the H-plane over the desired frequency range.

(ii) ML can suffer from underfitting or overfitting the training model which in turn leads to deviations in the predicted output.

State-of-the-Art (SOTA): Conventional full-wave EM solvers such as method of moments (MoM), multi-level fast multipole method (MLFMM), finite element method (FEM), and finite difference time domain (FDTD) method are currently being used to study, analyze and assess the performance of UWB antennas.

Deficiency in the SOTA: UWB antenna optimization using conventional EM solvers utilizes significant computational time and memory resource.

Solution Proposed:

(i) Design, simulate, validate, and perform a tradespace study on the design parameter space of the selected fractal antenna element using commercially available electromagnetic (EM) wave solvers.

(ii) Train, validate, test and compare multiple ML models for quicker and accurate prediction of antenna array response for different physical aperture areas.

Relevance to OSPRES Grant Objective: The fractal antenna achieves an UWB response, a mandatory requirement of the OSPRES grant objective, in a small volume footprint and similar physical aperture area when compared against the SOTA BAVA, dual ridge horn antennas etc. Furthermore, the microstrip-design-based fractal antenna can efficiently handle electronic steering by integrating the feed network on the same board. This eliminates the need to build a separate feed network external to the fractal antenna using bulky coaxial cables.

Risks, Payoffs, and Challenges:

(i) A majority of the fractal antenna geometries yield an omni-directional pattern in the H-plane, which can be a risk. However, efforts are underway to mitigate this pattern without deteriorating bandwidth.

(ii) Payoffs include developing a library of antenna metrics data for various fractal shapes and sizes.

(iii) Design challenges and numerical calculations with respect to specific fractal shapes could arise after performing a certain number of iterations to further improve the bandwidth.

(iv) Fractal antennas were known to generate gain loss at random frequencies over their operating frequencies. Achieving gain stability over the desired frequency range can be a significant challenge.

8.3.2 *Tasks and Milestones / Timeline / Status*

(A) Perform tradespace analysis of the fractal element radius *b* over the desired frequency range (4 to 12 GHz) using the genetic algorithm (GA) optimization tool available in the commercial electromagnetic (EM) solver FEKO / FEB21 / Complete.

- Milestone: Provide a recommendation of an optimum value of *b* using OPTFEKO to minimize reflection coefficient or S11 (< –10 dB).

(B) Perform tradespace study on different fractal shapes by changing the number of fractal segments to understand the effect of this change on the impedance bandwidth / FEB21 / Complete.

- Milestone: Produce a detailed study of the antenna response such as S11, gain, and bandwidth by varying the number fractal segments.

(C) Apply the GA optimization tool on the fractal side length *b* over a wide frequency range (2 to 12 GHz with 201 discrete frequency points) and number of fractal segments using OPTFEKO on the LEWIS cluster / MAR21 / Complete.

- Milestone: Reduce physical aperture area by 10% of its present design, reported in the FEB MSR, and demonstrate minimal or no change in S11, gain, and fidelity factor values.

(D) Perform a parametric study and analysis of antenna response by varying hexagon radius, *a* / MAR–APR21 / Complete.

- Milestone: Recommend a value of *a* to reduce the physical aperture area and increase aperture efficiency (>50%) with no variation in other antenna metrics.

(E) Frequency scale fractal antenna design such that the center frequency of the resulting antenna equals 1.3 GHz / MAY21 / Complete.

- Milestone: Modify antenna design with a center frequency equal to 1.3 GHz and achieve similar results (3:1 bandwidth at fc = 1.3 GHz, 3 dBi gain and >130% aperture efficiency at 900 MHz) to antenna design at center frequency ~7 GHz.

(F) Design and simulate various array antenna geometries composed of optimized fractal antenna elements (obtained from (E)) to analyze the effect of overall array antenna geometry on the desired array antenna response metrics (i.e., gain vs. frequency, gain vs. elevation angle at constant phi, rE/V, half-power beamwidth and side-lobe level.) / MAY–JUL21 / Complete

- Milestone: Recommend a best possible structure with reduced aperture area and minimal loss in gain.

(G) Apply ML models available in Altair Hyperstudy (2021) on the fractal antenna to try and understand the possibilities and limitations of ML models for fast and efficient antenna metrics prediction and optimization. Expand the prediction capability to time-domain electric field and antenna pattern using ML models (k-nearest neighbor and linear regression) available in scikit learn on Python programming tool “Anaconda”. / MAY21–FEB22 / Ongoing.

- Milestone: Recommend most accurate and efficient ML model for a fractal antenna in time-domain and frequency domain.

(H) Train and test the ML models on multiple fractal antenna array lattices and report tradespace study results using the trained ML models. / SEP21–FEB22 / Ongoing.

- Milestone: Recommend the best suitable ML model implemented/developed using Python programming language for array antenna metrics prediction and report tradeoffs.

(I) Develop a graphical user interface (GUI) that can perform tradespace studies on a fractal antenna array lattice and determine array metrics both in time-domain and frequency domain.

- Milestone: Propose a new and efficient method of performing tradespace studies on antenna arrays using ML models. / FEB22-JULY22 / Ongoing.

8.3.3 *Progress Made Since Last Report*

(H) In the previous report, the KNN ML model was successfully validated to predict the S11 response of center and corner elements. To further expand the scope of the KNN and LSR ML models, a new antenna array response metric (i.e., gain as a function of θ) is being tested. The KNN and LSR models available in the scikit-learn package of Python program are trained using 5 different antenna array design sets. Fig 8.3.1 illustrates the selected antenna array design.

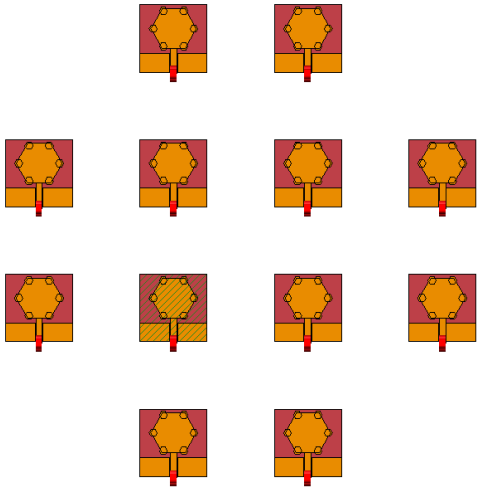


Figure 8.3.1. Octagonal shaped fractal antenna array.

(I) A new GUI is developed to enhance the usage of ML models for antenna design response prediction with a visual representation. Unlike the python scripts, GUI is generalized to extract the training data from *.out (FEKO output) of any kind of antenna irrespective of size of geometry, frequency range of interest, etc. Further, the extracted data will be stored in excel sheets that can be used as training data for ML models. Finally, GUI can be used to import the extracted training data and train the available ML models. Both KNN and LSR are added to the GUI.

8.3.4 *Technical Results*

(H) To generate the training data for five different sets, the interelement spacing (IE) between individual antenna elements has been varied. In total, 5 different antenna array designs with different IE values (i.e., 80mm, 90mm, 100mm, 110mm, 120mm) are simulated using CST studio. To validate the trained ML model, a new IE value (i.e, 125 mm) is considered. Fig. 8.3.2. demonstrates the radiation pattern comparison between the two ML models and against the radiation pattern obtained

from CST. From the plot it is evident that both KNN and LSR have good agreement with CST. The LSR prediction deviated from the CST result in the region where sidelobes are prominent, however, KNN showed better agreement with CST across the full θ-angle. From Table 8.3.1, the RMSE value of KNN is 2.4225, whereas the RMSE value for LSR is 4.3635. The KNN performs better with lower RMSE value compared to LSR.

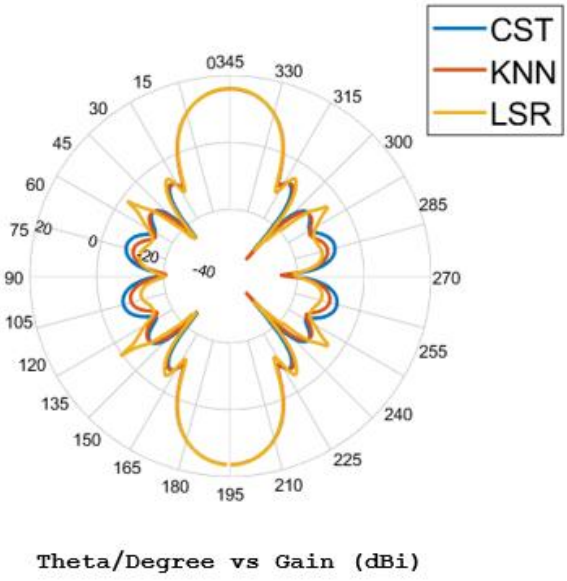


Figure 8.3.2. KNN and LSR prediction for gain as a function of theta

Table 8.3.1. RMSE comparison

ML model	RMSE value
KNN	2.4225
LSR	4.3635

(H) On the other hand, design simulation of a large antenna array is often time-consuming. To predict the radiation pattern of larger arrays using radiation pattern of smaller sub-arrays, active element pattern (AEP) or Subarray pattern method (SPM) can be employed [2]. The focus is to combine either of the above-mentioned approaches with machine learning models to develop a novel approach and reduce the time to prediction. In other words, this approach helps with performing faster tradespace studies of an antenna array provided the ML model is adequately trained and verified.

(I) Following are the steps involved in employing ML models to predict antenna design response using GUI.

Setup:

1. Import an Excel sheet with design variable and their values used to generate files in step 2
2. Import all the *.out files generated from FEKO to a single folder (training data).

3. Import *.out file into a separate folder (test data).

Model selection and training:

1. Select any a machine learning model from the drop-down button.
2. Train the model by passing the location of extracted training data.

Testing:

1. Predicted output will be stored into a excel sheet.

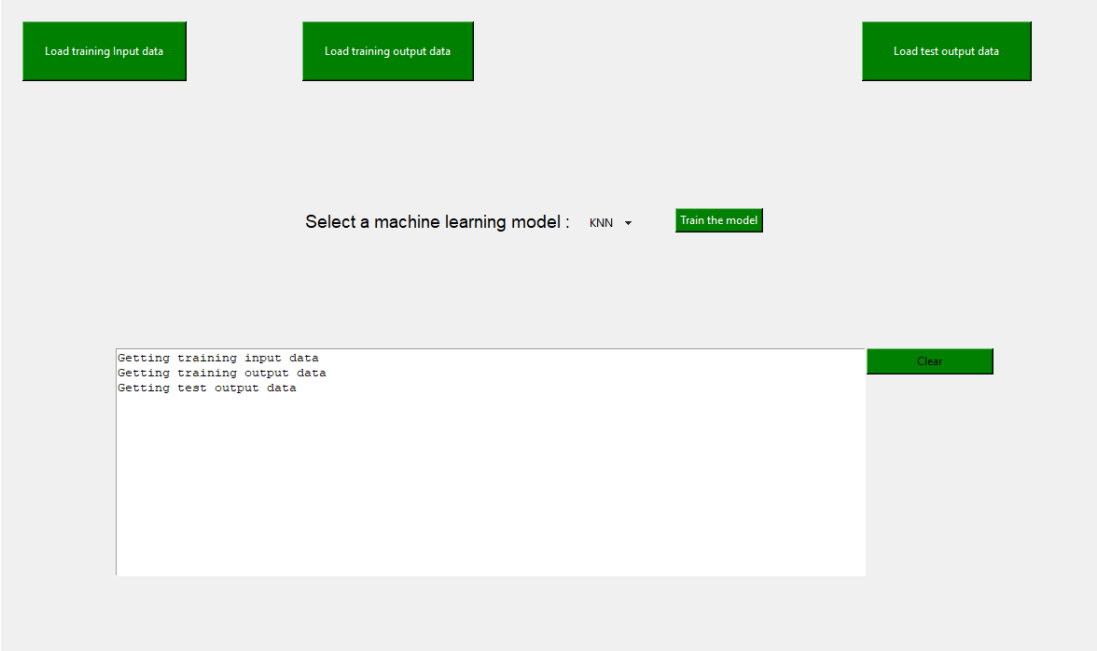


Figure 8.3.3. Snapshot of the GUI.

Successful implementation of the abovementioned steps will display a corresponding message in a white command window, which is shown in the bottom right of Fig. 8.3.3.

8.3.5 *Summary of Significant Findings and Mission Impact*

(A) The initial analysis of the simulation results with fractal radius *b* equal to 1.8 mm yielded multiple resonant frequencies with enhanced bandwidth. To further increase the bandwidth, OPTFEKO has been used as an optimization tool with fractal radius *b* as the optimization variable. The optimum value for *b* is found to be 1.66 mm. A comparison between reflection coefficient for initial *b* (= 1.8 mm) value and the optimized *b* (= 1.66 mm) can be found in Figure. 6.4.6. The optimization is carried out over 51 discrete frequency points.

(B) The addition of fractal elements (*N*) to the simple hexagon improved antenna metrics such as S11. To further investigate and understand the fractal elements, the number of segments in the fractal geometry has been varied. The improvement in bandwidth is observed as the value of *N* is increased from 6 to 14.

(C) The initial optimum value of *b* over 51 discrete frequency points is reported as 1.66 mm in task (A). To further increase the accuracy of the optimization algorithm and to find a more precise value for *b*, optimization is further performed over wider frequency points (201 discrete points between 2 GHz to 12 GHz) which yielded the optimum value of b as 1.368 mm. The S11 response of antenna design with newly found *b* (i.e., 1.368 mm) hasn't produced any better bandwidth with respect to *b* (= 1.66 mm). Thus, *b* is set to be 1.66 mm for further research.

(D) The hexagonal patch radius *a* has a significant effect on the physical aperture area of the antenna. Therefore, Altair OPTFEKO has been utilized to find an optimum *a* value, which was found to be 8 mm over the range 7.2 to 9 mm. Antenna metrics such as S11, gain, and bandwidth have shown desired performance with the optimized *a* value.

(E) The initial antenna design has been modified to achieve a center frequency of ~1.3 GHz. The gain value at 900 MHz is 3.5 dBi and, with the modified antenna design, we were able to achieve an impedance bandwidth ratio of 3.3:1. The designed antenna has been fabricated and tested, and the S11 response of the fabricated antenna agrees well when compared against FEKO, CST.

(F) To summarize, four different fractal antenna array geometries (i.e., square, diamond, hexagon, and octagon) have been designed and simulated. Upon comparing antenna array metrics, octagonal fractal antenna array has yielded minimal sidelobe levels with a gain of 15.7 dBi at 900 MHz close to that of square geometry with 32.27% lower physical aperture area than that of square geometry. The octagonal fractal antenna array has been chosen as the optimum geometry with reduced aperture area and reduced side lobes while retaining the bandwidth and gain milestone metrics.

(G) Radial basis function (RBF) and least square regression (LSR) were down selected from the initial three ML models based upon their generalization capability for prediction of reflection coefficient (S11), gain, and electric field. Further analysis of increasing training data set size has shown no improvement in prediction accuracy. Trained ML models were tested for design variable values outside the training range. The resulting RMSE increased as the values drifted away from the mid-point of the training range. RBF performed well in the prediction of S11, while LSR performed slightly better for gain and electric field predictions. In addition, for time-domain electric field prediction, we recommend using k-nearest neighbors (kNN) ML algorithm for accurate prediction.

(H) Initial application of kNN ML model for the prediction of antenna array bandwidth response of center and corner element yielded positive results with a good agreement between traditional EM solver (FEKO) and trained kNN ML model. The new LR ML model yielded improved RMSE values (over kNN) in its prediction of reflection coefficient and gain for the optimized octagon fractal antenna array. Furthermore, the KNN seemed efficient in the prediction of antenna pattern as a function of θ-angle.

8.3.6 *References*

[1] H. Fallahi and Z. Atlasbaf, "Study of a Class of UWB CPW-Fed Monopole Antenna With Fractal Elements," in IEEE Antennas and Wireless Propagation Letters, vol. 12, pp. 1484-1487, 2013, doi: 10.1109/LAWP.2013.2289868.

[2] S. Zhang, X. Wang and L. Chang, "Radiation Pattern of Large Planar Arrays Using Four Small Subarrays," in IEEE Antennas and Wireless Propagation Letters, vol. 14, pp. 1196-1199, 2015, doi: 10.1109/LAWP.2015.2397600.

9 Feedback

There is no feedback to report for the current reporting period.

10 Program Management

10.1 Issues

i. Scope – No issues
ii. Budget – 12-month NCTE submitted/pending
iii. Schedule – No issues

10.2 Interactions with Others

Agency/Org	Performer	Project Name	Purpose of Research/ Collaboration

10.3 Major Procurement Actions

10.4 Travel

Destination	Purpose	Attendees	Estimated Costs

10.5 Pending or Upcoming Public Release Requests

11 Appendix A: Academic and IP Output

11.1 Students Graduated

Name	Degree	Currently
Al-Shaikhli, Waleed Azad, Wasekul	MS Spring 19 PhD Summer 21	Kansas City National Security Campus, Honeywell Applied Materials, Sunnyvale, CA
Berg, Jordan	MS Spring 21	MRI Global
Bissen, Bear	MS Spring 19	Kansas City National Security Campus, Honeywell
Floyd, Dennis	BS	Naval Air Warfare Center Weapons Division
Hanif, Abu	PhD Spring 21	UMKC/MIDE (Postdoc)
Harmon, Aaron	BS	Missouri University of Science & Technology
Harp, Joshua	MS	UMKC/MIDE (Senior Engineer)
Hauptman, Cash	BS Spring 18	University of Nebraska-Lincoln
Klappa, Paul	MS Spring 21	
Labrada, Dario	BS Spring 20	Honeywell Aerospace, Florida
Lancaster, John	MS Spring 17	Lawrence Livermore National Laboratory
Renzelman, Jeff	MS Spring 18	Kansas City National Security Campus, Honeywell
Roy, Sourov	PhD Spring21	
Wagner, Adam	MS Fall 20	Kansas City National Security Campus, Honeywell
Xia, Shengxuan	BS	Missouri University of Science & Technology

11.2 Journal Publications

11.2.1 *In Preparation*

[1] N. Gardner, K. C. Durbhakula, and A. N. Caruso, “UHF and L-Band Frequency Generation at MW Peak Power using Diode-based Nonlinear Transmission Lines as Pulse Forming Networks,” *Transactions on Plasma Science*, In Preparation, **2021**.

[2] N. Gardner, K. C. Durbhakula, and A. N. Caruso, “Electrically Tunable Diode-based Nonlinear Transmission Line,” *TBD*, In Preparation, **2021**.

[3] N. Gardner, A. N. Caruso, K. C. Durbhakula and P. Doynov, “Diode-Based Non-Linear Transmission Line Design Considerations,” *Journal of Applied Physics*, In Preparation, **2021**.

[4] B. Barman, D. Chatterjee, K. C. Durbhakula, and A. N. Caruso, “Tradespace Analysis of Wideband, Electrically Small Microstrip Patch Antenna Elements for Phased Array Applications,” *IEEE Antennas and Propagation Magazine,* In preparation, **2021**.

[5] S. Xia, J. Hunter, A. Harmon, M. Hamdalla, A. Hassan, V. Khilkevich, D. Beetner, “Simulation Driven Statistical Analysis of the Electro-magnetic Coupling to Microstriplines,” *IEEE Transactions on Electromagnetic Compatibility*, In Preparation, **2020**.

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11.2.2 *Submitted / Under Revision*

[7] B. Barman, K. C. Durbhakula, D. Chatterjee, and A. N. Caruso, "Comparison of Machine Learning Algorithms for Bandwidth Enhancement of a Coaxial Probe-fed Microstrip Patch Antenna," *Applied Computational Electromagnetics Society (ACES)*, Submitted, **2021**.

[8] B. K. Lau, M. Capek, and A. M. Hassan, "Characteristic Modes–Progress, Overview, and Future Perspectives," *IEEE Antennas and Propagation Magazine*, Submitted, **2021**.

[9] K. Alsultan, M. Z. M. Hamdalla, S. Dey, P. Rao, and A. M. Hassan, "Scalable and Fast Characteristic Mode Analysis Implementation Using a Hybrid CPU/GPU Platform," *ACES*, Submitted, **2021**.

[10] M. Z. M. Hamdalla, B. Bissen, J. Hunter, L. Yuanzhuo, V. Khilkevich, D. G. Beetner, A. N. Caruso, and A. M. Hassan, "Prediction of Experimental Electromagnetic Coupling to a UAV Model Using Characteristic Mode Analysis," *IEEE Access*, Submitted, **2021**.

[11] W. Azad, F. Khan, and A. N. Caruso, "A Scalable Multilevel-Modular 10 kV Silicon Carbide MOSFET Module Featuring Custom Isolated Gate Driver Circuit Combined with Coupling and Snubber Circuits," *IEEE Transactions on Power Electronics*, Submitted, **2021.**

[12] John Keerthi Paul Bhamidipati, Eliot R. Myers, Adam M. Conway, Lars F. Voss, and Anthony N. Caruso, "Figure of Merit Development for Linear-Mode Photoconductive Solid-State Switches," *IEEE Transactions on Electronic Devices*, Under Revision, **2020**.

11.2.3 *Published / In Press*

[13] M. Z. M. Hamdalla, B. Bissen, J. Hunter, Y. Liu, V. Khilkevich, D. G. Beetner, A. N. Caruso, and A. M. Hassan, "Prediction of Experimental Electromagnetic Coupling to a UAV Model Using Characteristic Mode Analysis," *IEEE Access*, In Press, **2021**.

[14] J. N. Berg, R. C. Allen, and S. Sobhansarbandi. "A Novel Method of Cooling a Semiconductor Device through a Jet Impingement Thermal Management System: CFD Modeling and Experimental Evaluation." *International Journal of Thermal Sciences*, 172, 107254, **Feb 2022** [doi].

[15] W. Azad, F. Khan, and A. N. Caruso, "A Medium Power, Self-Sustaining, Configurable RF Pulse Generation Circuit Using a Nonlinear Transmission Line and Power Amplifier in a Closed Loop Configuration, *IEEE Transactions on Plasma Science*, vol. 49, no. 7, pp. 2183–2194, **July 2021** [doi].

[16] S. Roy, W. Azad, S. Baidya and F. Khan, “A Comprehensive Review on Rectifiers, Linear Regulators and Switched-Mode Power Processing Techniques for Biomedical Sensors and Implants utilizing In-body Energy Harvesting and External Power Delivery,” *IEEE Transactions on Power Electronics*, vol. 36, no. 11, pp. 12721–12745, **Nov 2021** [doi].

[17] K. C. Durbhakula, D. Chatterjee, and A. M. Hassan, “An Efficient Algorithm for Locating TE and TM Poles for a Class of Multiscale Inhomogeneous Media Problems,” *IEEE Journal on Multiscale and Multiphysics Computational Techniques*, vol. 4, no. 1, pp. 364–373, **2019** [doi].

11.3 Conference Publications

11.3.1 *Submitted / Accepted*

[1] B. Barman, D. Chatterjee, and A. N. Caruso, "On the Optimum Substrate Selection in Wideband Microstrip Patch Antenna Design," *2022 IEEE International Symposium on Antennas & Propagation & USNC-URSI Radio Science Meeting, Denver, Colorado, USA,* July 10-15, pp. 1-2. (Submitted)

[2] B. Barman, D. Chatterjee, and A. N. Caruso, "Time Domain Analysis of an UWB Electrically Small Microstrip Patch Antenna," *2022 IEEE International Symposium on Antennas & Propagation & USNC-URSI Radio Science Meeting, Denver, Colorado, USA,* July 10-15, pp. 1-2. (Submitted)

[3] S. R. Shepard and H. A. Thompson, “Self-focusing in Guided and Un-guided Media,” submitted to the *2021 OSA Nonlinear Optics Topical Meeting, Virtual Event*, August 9-13, 2021.

11.3.2 *Presented*

[4] B. Barman, D. Chatterjee and A. N. Caruso, "Probe-location Optimization in a Wideband Microstrip Patch Antenna using Genetic Algorithm, Particle Swarm and Nelder-Mead Optimization Methods," *2021 International Applied Computational Electromagnetics Society Symposium (ACES)*, 2021, pp. 1-3 [doi].

[5] W. Azad, S. Roy, and F. Khan, "A Single Gate Driver-based Four-stage High-voltage SiC Switch Having Dynamic Voltage Balancing Capability," *2021 IEEE Applied Power Electronics Conference and Exposition* (APEC), Phoenix, AZ, USA, June 9-12, 2021.

[6] W. Azad, S. Roy, F. Khan and A. N. Caruso, "A Multilevel-Modular 10 kV Silicon Carbide MOSFET Module using Custom High-Voltage Isolated Gate Driver, Coupling, and Snubber Circuits," *2021 IEEE Kansas Power and Energy Conference* (KPEC), Manhattan, KS, USA, April 19-20, 2021 [doi].

[7] T. Layman, T. D. Fields, and O. A. Yakimenko, “Evaluation of Proportional Navigation for Multirotor Pursuit,” AIAA SciTech Forum, Virtual Event, January 11-21, 2021 [doi].

[8] P. J. Klappa, and T. D. Fields, “Assessment of Fixed-Wing UAV System Identification Models during Actuator and Payload Drop Failures,” AIAA Atmospheric Flight Mechanics Conference, Virtual Event, January 11-21, 2021 [doi].

[9] J. Hunter, S. Xia, A. Harmon, A. M. Hassan, V. Khilkevich, and D. Beetner, “Modeling and Statistical Characterization of Electromagnetic Coupling to Electronic Devices,” *IEEE International Symposium on Antennas and Propagation and NSRM USNC-URSI National Radio Science Meeting*, Boulder, CO, January 4-9, 2021 [doi].

[10] B. Barman, K. C. Durbhakula, B. Bissen, D. Chatterjee, and A. N. Caruso, “Performance Optimization of a Microstrip Patch Antenna using Characteristic Mode and D/Q Analysis,” *2020 XXXIIIrd General Assembly and Scientific Symposium of the International Union of Radio Science*, Rome, Italy (online conference), Aug 29-Sept 5, 2020, pp. 1-4 [doi].

[11] J. Berg, and S. Sobhansarbandi. “CFD Modeling of Thermal Management Systems for a Silicon Semiconductor Switch.” *ASME 2020 Heat Transfer Summer Conference collocated with the ASME 2020 Fluids Engineering Division Summer Meeting and the ASME 2020 18th International Conference on Nanochannels, Microchannels, and Minichannels*, Virtual, July 13–15, 2020, American Society of Mechanical Engineers Digital Collection [doi].

[12] B. Barman, D. Chatterjee, and A. N. Caruso, “Performance Optimization of Electrically Small Microstrip Patch Antennas on Finite Ground Planes,” 2020 *IEEE International Symposium on Antennas and Propagation and North American Radio Science Meeting*, Montreal, Quebec, Canada, July 5-10, 2020, pp. 1–2 (online conference) [doi].

[13] M. Hamdalla, B. Bissen, A. N. Caruso, and A. M. Hassan, “Experimental Validations of Characteristic Mode Analysis Predictions Using GTEM Measurements,” *IEEE International Symposium on Antennas and Propagation and USNC-URSI Radio Science Meeting,* Montréal, Québec, Canada, July 5-10, 2020 [doi].

[14] K. Alsultan, P. Rao, A. N. Caruso, and A. M. Hassan, “Scalable Characteristic Mode Analysis: Requirements and Challenges (White Paper),” *Large Scale Networking (LSN) Workshop on Huge Data: A Computing, Networking and Distributed Systems Perspective Sponsored by NSF*, Chicago, IL, April 13-14, 2020.

[15] M. Hamdalla, A. N. Caruso, and A. M. Hassan, “Predicting Electromagnetic Interference to a Terminated Wire Using Characteristic Mode Analysis,” *Proceedings of the Annual Review of Progress in Applied Computational Electromagnetics (ACES)*, Monterey, CA, March 22-26, 2020. [doi]

[16] W. Azad, F. Khan, and A. Caruso, "Self-sustaining High-power RF Signal Generation Using LDMOS Based Power Amplifier and Nonlinear Transmission Line," *2020 IEEE Applied Power Electronics Conference and Exposition (APEC)*, New Orleans, LA, USA, March 15-19 2020, pp. 3567-3572 [doi].

[17] A. Hanif, W. Azad, and F. Khan, "Detection of Bond Wire Lift Off in IGBT Power Modules Using Ultrasound Resonators," *2020 IEEE Applied Power Electronics*

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[18] B. Barman, D. Chatterjee, and A. N. Caruso, “Some Investigations into Mutual Coupling Analysis for Trade Space Studies of Linear Arrays,” *2019 IEEE International Symposium on Phased Array Systems and Technology (PAST)*, Waltham, MA, October 2019, pp. 1-8 [doi].

[19] B. Barman, D. Chatterjee, and A. N. Caruso, “Characteristic Mode Analysis of a straight and an L-probe fed Microstrip Patch,” *2019 IEEE Indian Conference on Antennas and Propogation (InCAP)*, Ahmedabad, India, Dec 2019, pp. 1-3 [doi].

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[21] M. Hamdalla, J. Hunter, Y. Liu, V. Khilkevich, D. Beetner, A. Caruso, and A. M. Hassan, "Electromagnetic Interference of Unmanned Aerial Vehicles: A Characteristic Mode Analysis Approach," *IEEE International Symposium on Antennas and Propagation and USNC-URSI Radio Science Meeting at Atlanta (2 pages)*, Georgia, USA, July 7-12, 2019 [doi].

[22] K. C. Durbhakula, J. Lancaster, A. M. Hassan, D. Chatterjee, A. N. Caruso, J. D. Hunter, Y. Liu, D. Beetner, and V. Khilkevich, "Electromagnetic Coupling Analysis of Printed Circuit Board Traces using Characteristic Mode Analysis," *IEEE International Symposium on Antennas and Propagation and USNC-URSI Radio Science Meeting (2 pages)*, Atlanta, Georgia, USA, July 7-12 2019 [doi].

[23] K. C. Durbhakula, D. Chatterjee, and A. M. Hassan, “On the Location of Transverse Electric Surface Wave Poles for Electrically Thick Substrates,” Proceedings of the *IEEE Antennas and Propagation International Symposium and National Radio Science Meeting*, Atlanta, Georgia, USA, July 7-12, 2019 [doi].

[24] W. Azad and F. Khan, “Sustaining High-power RF Signal Generation in a Positive Feedback Network," *2019 IEEE Pulsed Power and Plasma Science Conference (PPPS)*, Orlando, FL, USA, June 23-28 2019.

[25] K. Alsultan, P. Rao, A. N. Caruso, and A. M. Hassan, “Scalable characteristic mode analysis using big data techniques,” *International Symposium on Electromagnetic Theory (EMTS 2019)*, San Diego, CA, USA, May 27-31, 2019.

[26] M. Hamdalla, W. Al-Shaikhli, J. Lancaster, J. D. Hunter, L. Yuanzhuo, V. Khilkevich, D. G. Beetner, A. N. Caruso, and A. M. Hassan, “Characteristic Mode Analysis of Electromagnetic Coupling to Wires with Realistic Shapes,” *International Symposium on Electromagnetic Theory (EMTS 2019)*, San Diego, CA, USA, May 27-31, 2019.

[27] K. C. Durbhakula, D. Chatterjee, and A. M. Hassan, “Location of Surface Wave Poles in Sommerfeld Integrals: A Mittag-Leffler Expansion Approach,” *Proceedings of the URSI-B International Symposium on Electromagnetic Theory*, URSI Commission, San Diego, USA, May 2019 [doi].

[28] K. C. Durbhakula, D. Chatterjee and A. M. Hassan, “Analytical Evaluation of Sommerfeld Integral Tails Present in Two-layered Media Green’s Functions,” *Proceedings of the Indian Conference on Antennas and Propagation* (InCAP), Hyderabad, India, December 2018 [doi].

[29] D. Beetner, V. Khilkevich, A. M. Hassan, J. Hunter, Y. Liu, and D. Floyd, *“*Characterization of the Electromagnetic Coupling to UAVs,*”* *DE Systems Symposium*, September 24-27, 2018

[30] C. Hartshorn, K. Durbhakula, D. Welty, D. Chatterjee, J. Lancaster, A. M. Hassan, and A. N. Caruso, “Crosstalk and Coupling to Printed Circuit Board Metallic Traces with Arbitrary Shapes,” *Proceedings of the AMEREM 2018 Conference*, Santa Barbra, CA, Aug 27-31, 2018.

[31] M. Hamdalla, J. Roacho-Valles, J. Hunter, D. Beetner, A. M. Hassan, and A. N. Caruso, “Electromagnetic Analysis of Unmanned Aerial Vehicles Using Characteristic Mode Analysis,” *Proceedings of the AMEREM 2018 Conference*, Santa Barbra, CA, Aug 27-31, 2018.

[32] C. Hartshorn, M. Hamdalla, J. Lancaster, A. M. Hassan, and A. N. Caruso, “Electromagnetic Vulnerability of Wires with Arbitrary Shape,” *Proceedings of the AMEREM 2018 Conference*, Santa Barbra, CA, Aug 27-31, 2018.

[33] K. C. Durbhakula, D. Chatterjee, A. M. Hassan, and M. S. Kluskens, “Studies on Numerical Evaluation of Sommerfeld Integrals for Multilayer Topologies,” *IEEE Antennas and Propagation International Symposium and National Radio Science Meeting*, Boston, Mass., USA, July 7-12, 2018.

[34] J. Lancaster, D. Chatterjee, and A. N. Caruso, “Some Investigations into the Dispersion Characteristics of Localized Bessel Beams,” published in the *IEEE Antennas and Propagation International Symposium and National Radio Science Meeting*, Boston, Mass., USA, July 7-12, 2018 (1 page URSI Abstract).

[35] M. Hamdalla, A. M. Hassan, and A. N. Caruso “Characteristic Mode Analysis of Unmanned Aerial Vehicles with Realistic Shapes and Material Composition,” *IEEE International Symposium on Antennas and Propagation and USNC-URSI Radio Science Meeting,* Boston, MA, July 8-13, 2018.

[36] W. Azad, S. Roy, A. S. Imtiaz, and F. Khan, "Microelectromechanical System (MEMS) Resonator: A New Element in Power Converter Circuits Featuring Reduced EMI," *2018 International Power Electronics Conference (IPEC-Niigata 2018-ECCE Asia)*, Niigata, May 20-24, 2018, pp. 2416-2420 [doi].

[37] J. Hunter, Y. Liu, D. Floyd, A. Hassan, V. Khilkevich, and D. Beetner, “Characterization of the Electromagnetic Coupling to UAVs,” *Annual Directed Energy Science and Technology Symposium*, Feb 26-March 2, 2018.

11.4 Conference Presentations

11.4.1 *Submitted / Accepted*

[1] S. Bellinger, A. Caruso, A. Usenko, “Stacked Diodes for Pulsed Power Applications,” GOMACTech-22, Miami, FL, March 21–24 2022 (submitted, oral).

[2] S. Bellinger, A. Caruso, A. Usenko, “New Paradigm on Making Semiconductor Opening Switches for Pulsed Power,” 2021 23rd IEEE Pulsed Power Conference, Denver, CO, Dec. 12–16, 2021 (accepted, oral).

Directed Energy Professional Society, Directed Energy Systems Symposium, Washington DC, October 25-29 2021 (submitted):

[3] B. Barman, D. Chatterjee, A. Caruso, and K. Durbhakula, “Tradespace Analysis of a Phased Array of Microstrip Patch Electrically Small Antennas (ESAs)” (Poster)

[4] J. N. Berg, R. C. Allen, and S. Sobhansarbandi, “A Novel Method of Cooling a Semiconductor Device through a Jet Impingement Thermal Management System: CFD Modeling and Experimental Evaluation” (Poster)

[5] J. N. Berg, R. C. Allen, and S. Sobhansarbandi, “Heat Transfer Enhancement of a Jet Impingement Thermal Management System: A Comparison of Various Nanofluid Mixtures” (Poster)

[6] J. Bhamidipati, M. Paquette, R. Allen, and A. Caruso, “Photoconductive Semiconductor Switch Enabled Multi-Stage Optical Source Driver” (Poster)

[7] G. Bhattarai, J. Eifler, S. Roy, M. Hyde, J. Bhamidipati, A. Usenko, M. Pederson, M. Paquette, A. Caruso, S. Bellinger, L. Voss, and R. Allen, “All Solid-State High-Power Pulse Sharpeners” (Poster)

[8] S. Brasel, K. Norris, R. Allen, A. Caruso, and K. Durbhakula, “Efforts to Reduce Physical Aperture Area of Ultra-Wideband Arrays” (Poster)

[9] A Caruso, “ONR Short Pulse Research and Evaluation for c-sUAV: Supporting and Sub-Programs Overview” (Oral)

[10] J. Clark, R. C. Allen, and S. Sobhansarbandi, “Ultra-Compact Integrated Cooling System Development” (Poster)

[11] J. Eifler, S. Roy, M. Hyde, G. Bhattarai, J. Bhamidipati, A. Usenko, M. Pederson, M. Paquette, A. Caruso, S. Bellinger, L. Voss, and R. Allen, “TCAD Optimization of Epitaxially Grown Drift-Step Recovery Diodes and Pulser Performance” (Poster)

[12] N. Gardner, M. Paquette, and A. Caruso, “Diode-Based Nonlinear Transmission Lines Capable of GHz Frequency Generation at Single MW Peak Powers” (Poster)

[13] M. Hamdalla, A. Caruso, and A. Hassan, “The Shielding Effectiveness of UAV Frames to External RF Interference” (Poster)

[14] M. Hamdalla, A. Caruso, and A. Hassan, “A Predictive-Package for Electromagnetic Coupling to Nonlinear-Electronics using Equivalent-Circuits and Characteristic-Modes (PECNEC)” (Poster)

[15] M. Hyde, J. Eifler, S. Roy, G. Bhattarai, A. Usenko, M. Paquette, A. Caruso, S. Bellinger, L. Voss, and R. Allen, “Development of an Evaluation Network for Drift Step Recovered Diodes through and Augmented Design of Experiment” (Poster)

[16] S. Indharapu, A. Caruso, and K. Durbhakula, “Machine Learning Based Ultra-Wideband Antenna Array Optimization and Prediction” (Poster)

[17] F. Khan, W. Azad, and A. Caruso, “A Scalable Multilevel-Modular 10 kV Silicon Carbide MOSFET Architecture for Pulsed Power Applications” (Poser)

[18] D. F. Noor, J. Eifler, M. Hyde, G. Bhattarai, S. Roy, J. Bhamidipati, A. Usenko, M. Pederson, M. Paquette, A. Caruso, S. Bellinger, L. Voss, and R. Allen, “DSRD-IES Pulsed-Power Generator Topology Study Using Machine-Learning-Based Feature Selection Optimization and Predictive Learning” (Poster)

[19] S. Roy, J. Eifler, M. Hyde, G. Bhattarai, D. Noor, J. Bhamidipati, A. Usenko, M. Pederson, M. Paquette, A. Caruso, S. Bellinger, L. Voss, and R. Allen, “Systematic Topological Optimization of DSRD-Based IES Pulse Generator” (Poster)

[20] S. Shepard and A. Caruso, “Tubular Core Optical Power Amplifier” (Poster)

[21] H. Thompson, M. Paquette, and A. Caruso, “Minimizing On-State Resistance in GaN:X Photoconductive Semiconductor Switches (PCSSs) for Direct Modulation (Poster)

[22] A. Usenko, J. Eifler, S. Roy, G. Bhattarai, M. Hyde, M. Paquette, A. Caruso, S. Bellinger, L. Voss, and R. Allen, “New Paradigm in Fabrication of Semiconductor Opening Switches for Pulsed Power” (Poster)

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[23] S. Bellinger, A. Caruso, A. Usenko, “Stacked Diodes for Pulsed Power Applications: New Process Integration Scheme,” 240th Electrochemical Society Meeting, Orlando, FL, Oct. 10–14, 2021 (submitted, oral).

11.4.2 *Presented*

[24] W. Azad, S. Roy, and F. Khan, “A Four-State Capacitively Coupled High-Voltage Switch Powered by a Single Gate Driver,” *47th IEEE Conference on Plasma Science*, Singapore, December 6-10, 2020 (oral).

[25] J. Hunter, S. Xia, A. Harmon, A. Hassan, V. Khilkevich, and D. Beetner, “Simulation-Driven Statistical Characterization of Electromagnetic Coupling to UAVS,” *Annual Directed Energy Science and Technology Symposium*, March 2020 (abstract appeared, but talk cancelled due to pandemic).

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DEPS Posters and Presentations 2020

[26] William Spaeth, Wideband Parallel Plate to Coaxial Cable Taper

[27] Stefan Wagner, Quickly Determining Minimum HPC Source Requirements Using Binary Search

***

GOMAC 2019

[28] Cash Hauptmann, Reduced Recovery Time in SiPCSS Photoconductive Switches

[29] Eliot Myers, Picosecond High Power Switching Technologies

[30] Heather Thompson, GaN Optimization for Use in Photoconductive Switch

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[28] B. Barman, D. Chatterjee, and A. N. Caruso, “Analytical Models for L-Probe fed Microstrip Antennas,” *Proceedings of the IEEE Antennas and Propagation International Symposium and National Radio Science Meeting*, Atlanta, Georgia, USA, July 7-12, 2019 (1 page URSI Abstract).

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Directed Energy Professional Society (DEPS) Annual Science and Technology Symposium, Destin, Florida, USA, April 2019:

[29] Ryan Butler, Mechanical Challenges of Modular Photoconductive Semiconductor Based HPM Sources

[30] Steve Young, Two-Dimensional Optoelectronic Pulsed Power Switches: Initial Effort

[31] Adam Wagner, Rapid Cost Effective RF Component Prototyping Using 3D Printers

[32] Heather Thompson, Cost to benefit analysis of GaN for Photoconductive Semiconductor Switches

[33] Colby Landwehr, Low Leakage Electroluminescence For Improving SiPCSS Hold Off

[34] James Kovarik, Some Investigations Into Applications Of Electrically Small Antennas As Phased Array Elements

[35] Spencer Fry, Maximizing SiPCSS Efficiency For HPM Sources

[36] Deb Chatterjee, Studies On Antenna Characterization And Propagation Of High Power Pulsed Electromagnetic Waves With Minimal Dispersion

***

DEPS Posters and Presentations 2018

[37] Jeff Scully, ElectroLuminescence Studies of Silicon Based Photo-Switches

[38] Cash Hauptmann, Thermal Anlaysis of a PCSS through TCAD Simulation

[39] Nicholas Flippin, Fast Rise Time Switches: Drift Step Recovery Diode

***

DEPS Posters and Presentations 2017

[40] Noah Kramer, Recent Results of Silicon Based Photoconductive Solid State Switches for 500kHz Continuous Pulse Repetition Frequency

11.5 Theses and Dissertations

[1] Jordan N. Berg, “Development of a Jet Impingement Thermal Management System for a Semiconductor Device with the Implementation of Dielectric Nanofluids,” MS Thesis in Mechanical Engineering, University of Missouri-Kansas City, **2021** [mospace].

[2] James C. Kovarik, “Wideband High-Power Transmission Line Pulse Transformers,” MS Thesis in Electrical Engineering, **2021** [mospace].

[3] Wasekul Azad, “Development of Pulsed Power Sources Using Self-Sustaining Nonlinear Transmission Lines and High-Voltage Solid-State Switches,” PhD Dissertation in Electrical Engineering, **2021** [mospace].

[4] Paul Klappa, “Implementation and Assessment of State Estimation Algorithms in Simulation and Real-World Applications,” MS Thesis in Mechanical Engineering, **2021** [mospace].

11.6 IP Disclosures Filed

[1] S. Bellinger, A. Caruso, A. Usenko, US Provisional Patent Application “Stacked Diode with Side Passivation and Method of Making the Same,” 12AUG2021.

[2] S. Bellinger, A. Caruso, A. Usenko, “Diode and Method of Making the Same,” 28JUNE2021.

[3] Bhamidipati, Myers, Caruso, “Multi-Stage Photo-Stimulated WBG-PCSS Driven RF Pulse Generation System Implementing Miniature Optical Sources,” 21UMK009, 04NOV2020.

[4] Shepard, “A Low Noise Optical Amplifier,” 21UMK007, 14SEPT2020.

[5] Shepard, “A Novel Optical Fiber Amplifier,” 20UMK012, 02JUN2020.

[6] Doynov, “High-power High Repetition Rate Microwaves Generation with Differentially Driven Antenna,” 20UMK011, 19APR2020.

[7] Doynov, “Scalable Modular System for High-power Microwaves Generation,” 20UMK010, 19APR2020.

[8] Doynov, “Pulse Differential High-power Microwave Generation,” 19UMK007, 02JAN2019.

[9] Doynov, “Non-linear Network Topologies with Reutilized DC and Low-frequency Signal,” 19UMK008, 28DEC2018.

[10] Doynov, Caruso, “Non-Linear Transmission Line Topologies for Improved Output,” 19UMK005, 28SEPT2018

11.7 Provisional Patents Filed

[1] S. Bellinger, A. Caruso, A. Usenko, US Provisional Patent Application “Stacked Diode with Side Passivation and Method of Making the Same,” filed 09/10/2021.

[2] S. Bellinger, A. Caruso, A. Usenko, “Diode and Method of Making the Same” US Provisional Patent Application 63/216,550, filed June 30, 2021.

[3] P. Doynov, A. Caruso, “High-Efficiency High-Power Microwave Generation using Multipass Non-Linear Network Topologies,” filed 26NOV2019.

[4] Plamen Doynov, James Prager, Tim Ziemba, Anthony N. Caruso, “Non-Linear Transmission Line Topologies for Improved Output”, USPTO Provisional Serial No. 62/737,185, filed 27SEPT2018.

11.8 Non-Provisional Patents Filed

None to date

ONR HPM Program – Monthly Status Report (MSR) – March 2022

Anthony Caruso – Univ. Missouri – Kansas City

N00014-17-1-3016 [OSPRES Grant]

ONR Short Pulse Research, Evaluation and non-SWaP Demonstration for C-sUAS Study

15 APRIL 2022

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1 Contents

2 Executive Summary

2.1 Progress, Significant Findings, and Impact

Fiber Laser and Optical Amplifiers. We extend our range of applications to include the use of our tubular-core optical power amplifier as a power combiner. Power combiners are of substantial DoD interest for the application of combining several lasers (typically fiber lasers) to achieve one higher power output beam. We approach this in a way that also covers our hopes of simplifying the entrance optics design (in our power amplifier application) by illuminating the glass tube with four Gaussian beam spots of various phases and polarizations. We discovered some new physics, which enable more beam profile options than a SOTA fiber power combiner. Specifically, we demonstrate one phase/polarization scheme that confines the output to the glass/cladding mode (for HMP applications) and another that maximizes the output coupling into the air/core mode (for HEL applications).

On-State Resistance in GaN:X PCSS. Towards minimizing on-state resistance in GaN photoconductive semiconductor switches (PCSS), the spot size/shape and energy density must be considered. A literature study of device performance using GaAs PCSS found that a smaller spot size, but larger energy density was better for reducing on-state resistance instead of a larger spot size covering more of the active area with the same average power but less energy density. A working model in Silvaco TCAD was made and initial results along with comparison to experimental results is expected next report.

DSRD Optimization Simulations. To achieve drift-step recovery diode (DSRD)-only peak load (50-Ω) voltage >40-kV with risetime <2-ns, circuit simulation (e.g., SPICE) models matching measured values to <5% are necessary to optimize DSRD-based pulsers. The CMC diode model has improved the DSRD modeling with a peak load voltage match with 0.4% error and a risetime match with 20% error, resulting in the closest match to 1x1 DSRD-based pulser performance with a realistic diode (DSRD) model. Future iterations will improve the fit for peak load voltage, risetime, pulsewidth, and voltage riserate and determine the ability of the CMC diode model to capture DSRD performance. The CMC diode Verilog-A code can also be modified to include more realistic DSRD-specific modeling.

DSRD Processing and Manufacturing. The Gen3 lot has reached the step of die singulation by anisotropic etching of v-grooves. The first wafer in the lot has been successfully processed in our unique etch composition of 1:1:1 TMAH:DMSO:water. In terms of process step development, the successful bonding into a stack was performed with solid–liquid interdiffusion technology.

DSRD Design of Experiments. The zero junction bias capacitance (ZJBC) results have been processed for the first six rounds of the experimental design. Their averaged measurements and coefficients of variance were used as a guide in diode selection across each group (12 diodes total) to begin correlation studies between the ZJBC measurements and the pulser performances. Additionally, the Gen2 diodes were compared to the results of the previous repeatability study; they showed an increase in

variation, the exact source of which cannot be concluded until after the remaining DC tests have also been evaluated.

DSRD-Based Pulsed Power Source Optimization. Towards increasing the output voltage of the air-cooled DSRD-based pulser to >10 kV, we have updated the circuit components and number of diodes based on experimental results from the previously reported pulser (FEB22 MSR Report), circuit theory, and simulation. Two new pulsers have been populated with the optimized components for three 7-stack and four 7-stack diodes, each capable of producing theoretical outputs of 13.5 and 18 kV respectively. We have successfully increased the diode current using two MOSFETs in parallel. Experimental observation of circuit voltages at different nodes indicates expected circuit operation and confirms the circuit simulation. However, the three 7-stack optimized circuit produced only 4.5 kV of output, which was nearly independent of applied prime voltage and trigger length. The produced lower output could be due to diode degradation or an inaccurate diode model.

Continuous Wave Diode-NLTL Based Comb Generator. Simulation and testing efforts on continuous wave D-NLTLs have been focused on attaining source–line impedance matching by using a resistor equivalent to the average line impedance. Low to no reflection was noticed at low frequency (10–30 MHz) excitation. However, when excited with an 80 V, 700 MHz CW signal, ~50% reflection was observed for the high voltage lines. A dynamic impedance matching technique to mitigate the power reflection is being explored to mitigate reflection at high frequencies.

Dynamically Tunable Multi-Frequency Solid-State Frozen Wave Generator (FWG). An updated Gen-2 12-segment FWG with modified switch position and optimized ground plane has been designed, fabricated, and tested up to 400 V to determine the root cause of the voltage drop measured in Gen-1 prototype testing. Upon testing, the rise-time of the MOSFET was considered to be the factor limiting the simultaneous switching of transmission line segments, leading to reduced peak voltages in the pulse train and <100 MHz output frequencies. A solid-state switch technology capable of sub-ns rise times would greatly benefit FWG implementation in generating sub-GHz frequencies.

Pulse-Compression-Based Signal Amplification. The two-stage magnetic pulse compression (MPC) circuit that was previously tested was simulated in LTSpice using the Chan model for Kemet NiZn cores. Simulation results match the expected output waveforms, indicating successful modeling of magnetic cores and MPC with LTSpice for DC input. Simulations provided invaluable insight into MPC operation, especially in terms of saturation and LC resonance timing. It was also observed from the simulations that the Kemet NiZn cores have a relatively slow change in inductance prior to saturation, increasing the pre-pulse currents and resulting in losses in voltage transfer. COTS NiZn cores with sharper saturation characteristics will be investigated for future prototype MPC circuits.

Antennas. A significant improvement in agreement between the simulated and experimental far-field antenna parameters was achieved upon re-testing the manufactured antenna element and array prototypes in an anechoic chamber at the University of Missouri-Columbia campus. A tapered coaxial connector that can be used to feed wideband (>30% impedance bandwidth) microstrip patch antennas, at the UHF

range, has been designed and will be forwarded for manufacturing. If reasonable performance is achieved from a single antenna element integrated with the tapered connector, the custom connectors will be employed as feeds to array elements for the final demonstrable prototype.

A second variant of the Koshelev antenna was 3D-printed, assembled, and metalized (with silver paint) to develop a functioning and low-cost Koshelev antenna prototype. The conductivity of the silver-painted Koshelev antenna has been measured and validated. In addition, we are currently fabricating a standalone prototype of the impedance transformer using polylactic acid (PLA) as dielectric material to ensure its functionality as intended before interfacing with the antenna. The PLA dielectric was chosen over stereolithography (SLA) for the former's rapid manufacturability, lower weight, lower material cost, and higher dielectric constant value.

In our effort to develop a novel Tradespace study tool using Python for single element and antenna array performance prediction and optimization using machine learning (ML) algorithms, we have improved the tool that can: (1) automatically import the training data; (2) train the ML algorithm of user-choice; (3) enter test data input of user-choice; and (4) display the desired single element antenna output metric. Using this tool in conjunction with multi-objective optimization algorithms would decrease the Tradespace study time by more than 80%. In addition, we are currently working on integrating the active element pattern (AEP) method into our tool that assists with estimating performance of electrically large antenna arrays while further reducing the time needed to see tradespace results.

2.2 Completed, Ongoing, and Cancelled Sub-Efforts

	Start	End
2.2.1 *Ongoing Sub-Efforts*		
GaN:C Modeling and Optimization	OCT 2017	Present
Diode-Based Non-Linear Transmission Lines	FEB 2018	Present
Trade Space Analysis of Microstrip Patch Arrays	FEB 2019	Present
Enclosure Effects on RF Coupling	OCT2019	Present
Lasers and Optics	FEB 2020	Present
UWB Antenna Element Tradespace for Arrays	MAY 2020	Present
Si-PCSS Contact and Cooling Optimization	JAN 2021	Present
Drift-Step Recovery Diode Optimization	JAN 2021	Present
UAS Engagement M&S	MAR 2021	Present
DSRD-Based IES Pulse Generator Development	APR 2021	Present
Drift-Step Recovery Diode Manufacturing	MAY 2021	Present
IES Diode Characterization	MAY 2021	Present
Sub-Nanosecond Megawatt Pulse Shaper Alternatives	MAY 2021	Present
Ultra-Compact Integrated Cooling System Development	MAY 2021	Present
GaN-Based Power Amplifier RF Source	AUG 2021	Present
Reconfigurable RF Pulsed-Power Source	AUG 2021	Present
RF Driver Unit for GaN SD-MPM Power Amplifier	SEPT 2021	Present
Reconfigurable RF Antenna for SD-MPM Sources	SEPT 2021	Present
Continuous Wave Diode-NLTL Based Comb Generator	SEPT 2021	Present
2.2.2 *Completed Sub-Efforts*		
Adaptive Design-of-Experiments	OCT 2017	APR 2019
Non-perturbing UAV Diagnostics	OCT 2017	OCT 2018
Noise Injection as HPM Surrogate	OCT 2017	MAR 2019
SiC:N,V Properties (w/ LLNL)	APR 2018	MAR 2019
Helical Antennas and the Fidelity Factor	JUL 2018	SEPT 2019
Si-PCSS Top Contact Optimization	APR 2020	OCT 2020
Nanofluid Heat Transfer Fluid	NOV 2020	JUL 2021
HV Switch Pulsed Chargers	DEC 2018	DEC 2021
2.2.3 *Cancelled/Suspended Sub-Efforts*		
Ab Initio Informed TCAD	OCT 2017	OCT 2020
Positive Feedback Non-Linear Transmission Line	NOV 2017	DEC 2018
Minimally Dispersive Waves	FEB 2018	SEPT 2018
Multiferroic-Non-linear Transmission Line	NOV 2018	APR 2019
Avalanche-based PCSS	SEPT 2018	SEPT 2019
Gyromagnetic-NLTL	DEC 2017	NOV 2020
Multi-Stage BPFTL	APR 2020	JUL 2020
Heat Transfer by Jet Impingement	MAY 2018	FEB 2021
Si, SiC, and GaN Modeling and Optimization	NOV 2018	FEB 2021
Bistable Operation of GaN	FEB 2021	MAR 2021
IES Pulser Machine Learning Optimization	MAY 2021	AUG 2021
WBG-PCSS Enabled Laser Diode Array Driver	NOV 2020	JAN 2022

2.3 Running Total of Academic and IP Program Output

See Appendix for authors, titles and inventors (this list is continuously being updated)

Students Graduated	*5 BS, 8 MS, 3 PhD*
Journal Publications	*5 (6 submitted/under revision)*
Conference Publications	*33 (4 submitted/accepted)*
External Presentations/Briefings	*17 (23 submitted/accepted)*
Theses and Dissertations	*4*
IP Disclosures Filed	*10*
Provisional Patents Filed	*4*
Non-Provisional Patents Filed	*0*

3 Laser Development

3.1 Fiber Lasers and Optical Amplifiers

(Scott Shepard)

3.1.1 *Problem Statement, Approach, and Context*

Primary Problem: High-average-power 1064-nm picosecond lasers are too large (over 1100 cm^3/W) and too expensive (over \$1000/μJ per pulse) for PCSS (photoconductive semiconductor switch) embodiments of HPM-based defense systems. For example, a laser of this class might occupy a volume of 1 m x 30 cm x 30 cm = 90,000 cm^3 and provide an average power of 50 W (thus, 1800 cm^3/W). Costs in this class range from \$100K to \$300K to drive our Si-PCSS applications.

Solution Space: Optically pumped ytterbium-doped optical fiber amplifiers, fed by a low-power stable seed laser diode, can offer a cost-effective, low-weight, and small-volume solution (with respect to traditional fiber and traditional free-space laser designs). Moreover, our novel optical amplifier tubes, might operate at far higher power levels (over 1000 times greater), thus driving an entire array of PCSS with a single amplifier and thereby reducing the overall system costs and eliminating the optical pulse-to-pulse jitter constraints.

Sub-Problem (1): Optical pump power system costs account for over 50% of the budget for each laser (in this class, for normal/free-space, optical fiber, and tubular embodiments).

Sub-Problem (2): Fiber (as well as power tube) optical amplifier performance is degraded primarily by amplified spontaneous emission (ASE) noise, which limits the operating power point, and by nonlinearities, which distort the optical pulse shapes.

State-of-the-Art (SOTA): Free-space NdYAG lasers or Ytterbium-doped fiber amplifiers optimized for LIDAR, cutting, and other applications.

Deficiency in the SOTA: Optical pump power system costs (in either free-space or fiber lasers) are prohibitive for the PCSS applications until reduced by a factor of at least two.

Solution Proposed: Fiber lasers permit a pre-burst optical pumping technique (wherein we pump at a lower level over a longer time) which can reduce pumping costs by a factor of at least ten. To address the ASE and nonlinear impairments, we are pursuing the use of gain saturation and a staged design of different fiber diameters. We also apply these techniques to fiber amplifiers which incorporate our power amplifier tube in the final stage. The inclusion of our novel tubular-core power amplifier stage should permit a single laser to trigger an array of several PCSS (reducing system cost and mitigating timing jitter).

Relevance to OSPRES Grant Objective: The enhancement in SWaP-C^2 for the laser system enables PCSS systems for viable deployment via: a factor of 40 in pumping cost reduction of each laser; and a factor of *N* in system cost reductions as a single laser could drive *N* (at least 12) PCSS in an array, while also eliminating the optical jitter constraints.

Risks, Payoffs, and Challenges: Optically pumping outside the laser pulse burst time can enhance the ASE; pump costs could be reduced by 40, but ASE in the presence of dispersion and/or nonlinearities could enhance timing jitter thereby limiting steerability. The main challenge for power tube implementation is the entrance optics design.

3.1.2 *Tasks and Milestones / Timeline / Status*

(A) Devise a pre-burst optical pumping scheme by which we can reduce the costs of the laser by a factor of two or more and calculate the resulting increase in ASE. / FEB–JUL 2020 / Completed.

(B) Reduce the ASE via gain saturation. / Oct 2020 / Completed.

(C) Design saturable gain devices which avoid nonlinear damage. / Ongoing.

(D) Calculate and ensure that timing jitter remains less than +/-15 ps with a probability greater than 0.9. / Ongoing.

(E) Demonstrate a cost-reduced fiber laser. / Ongoing.

(E1) **March 2021** Finalize design. / Completed.
(E2) **April 2021** Assemble and test-check seed LD (laser diode)/driver. / Completed.
(E3) **April 2021** Measure power vs current transfer function of seed LD/driver. / Completed.
(E4) **May–July 2021** Measure ASE and jitter of 1064 nm seed LD/driver. / Completed.
(E5) **May–July 2021** Measure ASE and jitter of 1030 nm seed LD/driver. / Completed.
(E6) **June–July 2021** Assemble and test-check pump LDs/drivers. / Completed.
(E7) **June–July 2021** Measure power vs current transfer function of pump LDs/drivers. / Completed.
/ (E8) – (E14) Delayed due to vendor issues (see MAY MSR).
(E8) **September 2021** Splice power combiners to Yb doped preamp fiber. /Completed.
(E9) **September 2021** Connect seed and pumps to power combiners and test-check. / Completed.
(E10) **September–October 2021** Measure gain, ASE and jitter of 1064 nm preamp assembly (forward, backward and bidirectional pumping) as a function of pump power and duty cycle. / Partially complete.
(E11) **September–October 2021** Measure gain, ASE and jitter of 1030 nm preamp assembly (forward, backward and bidirectional pumping) as a function of pump power and duty cycle. / Partially complete.
(E12) **November 2021** Splice power amplifier and its power combiner to best preamp. / Ongoing (delay due to vendor error).
(E13) **November–December 2021** Measure gain, ASE and jitter of entire amp assembly. / Ongoing (delay due to vendor).
(E14) **December 2021** Analyze data and document. / Ongoing (delay due to vendor).

(F) Design a new type of higher power, tubular core fiber amplifier. / Ongoing.

(F1) Apply one high-power tubular amplifier to a system comprised of an array of several (say N) PCSS. For example: N=12 in a 3x4 array (or 4x4 array with corners omitted) N=16

in a 4x4 array, etc.; thereby eliminating jitter constraints and reducing laser system cost by more than a factor of 100 (independent of burst profile). / Ongoing.

3.1.3 *Progress Made Since Last Report*

(F) We now extend our range of applications to include the use of our tubular-core optical power amplifier as a power combiner. Power combiners are of substantial DoD interest for the application of combining several lasers (typically fiber lasers) to achieve one higher power output beam. We approach this in a way that also covers our hopes of simplifying the entrance optics design, in our power amplifier application, via illuminating the glass tube with 4 spots. The 4 spots could come from 4 different lasers (in the combiner application) or from one laser, followed by three beam splitters to create 4 output beams (in the entrance optics application). We consider a variety of polarization and phase combinations and find examples of both: Gaussian-like; and more uniformly distributed, output beam profiles.

(F1) We constructed a model in COMSOL to simulate the passive optical power splitter for the application of driving several Si-PCSS from a single laser but ran into difficulties on importing the output of one COMSOL (the power amplifier) into the input of another (the splitter). We are in consultation with COMSOL support on how to resolve the issue.

3.1.4 *Technical Results*

(F) To address both the power combiner and entrance optics applications we consider illuminating the glass tube with 4 spots. Each spot is comprised of a Gaussian beam impinging on the glass wall/cladding of the tube and our performance metrics are the power and beam quality output from the tubes air-core, as illustrated in Fig. 3.1.1 (for the case of core radius, r = 5, tube thickness, t = 3, and radial polarization). All units are normalized with respect to the unperturbed (linear) gain, g_0, as discussed in the MSR of FEB2022, and the current study neglects gain saturation so the creation of the core mode in Fig. 3.1.1 is due solely to the “fiber nonlinearity” (characterized by γ) which creates the self-focusing power limits.

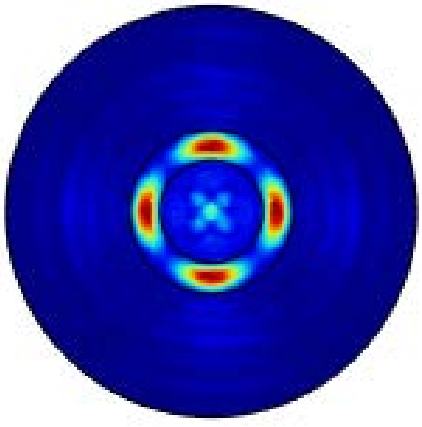


Fig. 3.1.1. Electric field distribution at the output of an optical power tube illuminated by 4 spots of radial polarization (for r = 5, t =3).

We consider four types of polarization and phase combinations: **radial** – in which the input field of each spot is polarized in the radial direction and in-phase (i.e., they all point inwards initially); **phi-phased** – in which each spot is vertically polarized but is phase-shifted according to the angle of the spot ($0, \pi/2, \pi, 3\pi/2$); **phi-polarized** – in which the polarization of each spot is in the direction of increasing angle (tracing out a circle, i.e., to the right on top, down on right, left on bottom, and up on left); and **in-phase** – in which case all spots are vertically polarized and in-phase. The results depend also on r and t, but typically we found that phi-polarized is best at confining the field into the glass cladding; while radial is best at coupling the field into the air core.

To quantify the metrics we examine the cutlines (one dimensional plots of the electric field) across the output of the tube, as exemplified in Fig. 3.1.2 (as well as consider the two dimensional distribution such as in Fig. 3.1.1). The following four figures compare the results of the four polarization/phasing schemes for the case of r = 2.5, t = 2; and then we will show likewise for the case of r = 5, t =3. In all these figures the input intensities range from 2.5×10^{14} [W/m^2] to 2.0×10^{20} [W/m^2]. In Fig. 3.1.2 we see that the radial polarization in this case creates a Gaussian at core center of amplitude roughly one-sixth that of the two sharply peaked fields in the cladding on both sides.

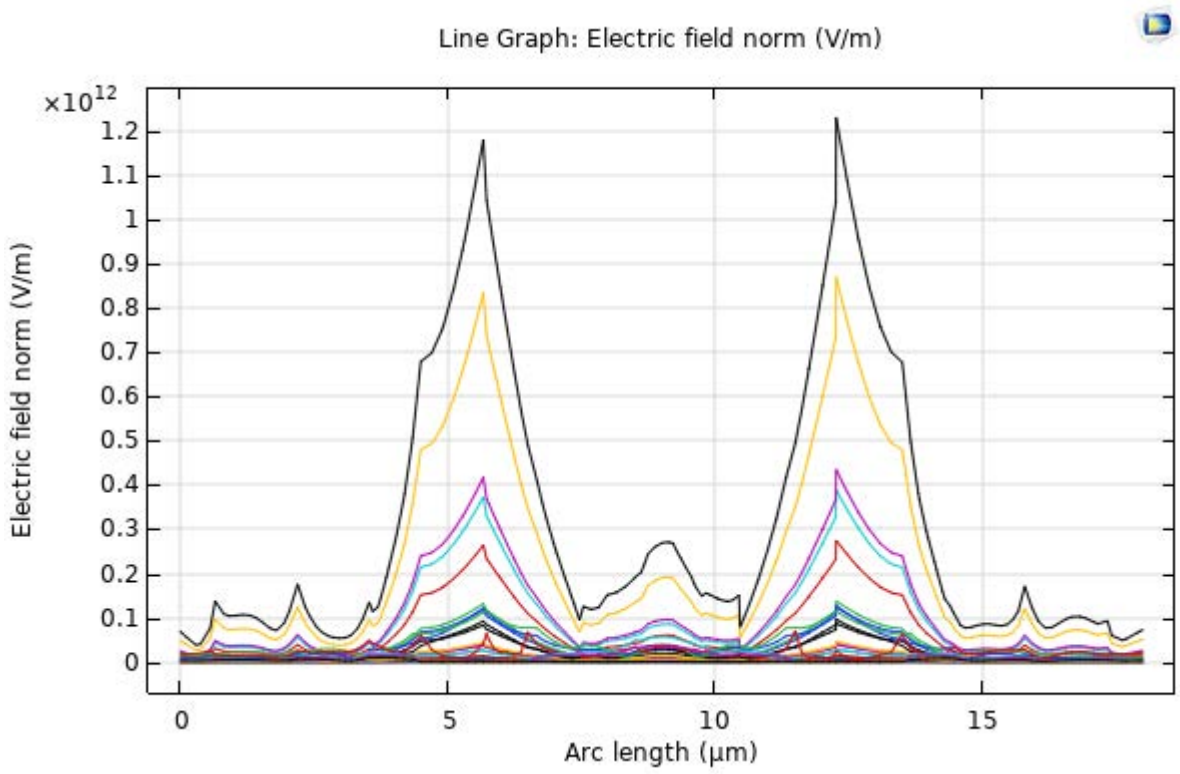


Fig. 3.1.2. Output field distribution for r = 2.5, t =2, with radial illumination.

In Fig. 3.1.3 we see that phi-polarized illumination creates essentially the opposite effect. There now is a null at core center and the previously sharply peaked fields of the cladding are now remarkably smooth. This type of polarization scheme should be advantageous for applications in which we wish the field to be primarily confined to the cladding.

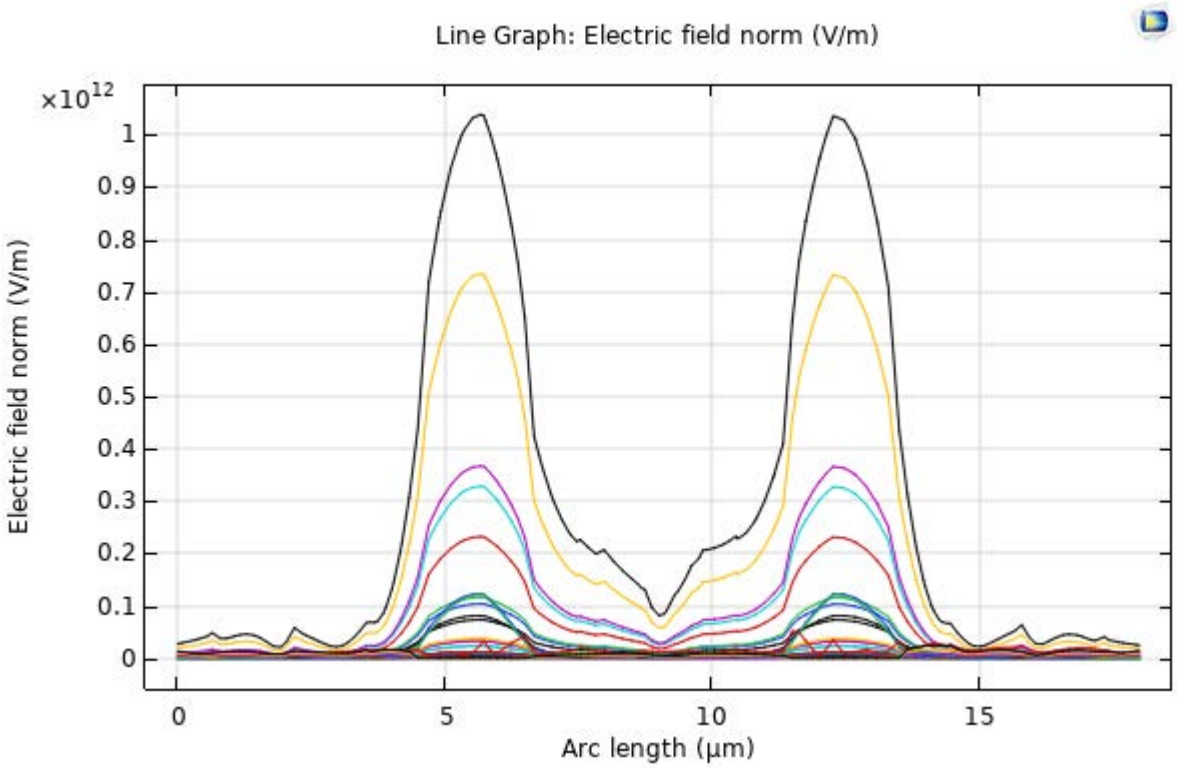


Fig. 3.1.3. Output field distribution for r = 2.5, t =2, with phi-polarized illumination.

For the case of phi-phased (and vertically polarized) illumination we see in Fig. 3.1.4 the return of the sharply peaked cladding fields and a roughly linear distribution (with a slight slant) across the core. In fact, sharply peaked cladding fields were observed in all the cases studied to date – excepting only for the case of phi-polarized illumination.

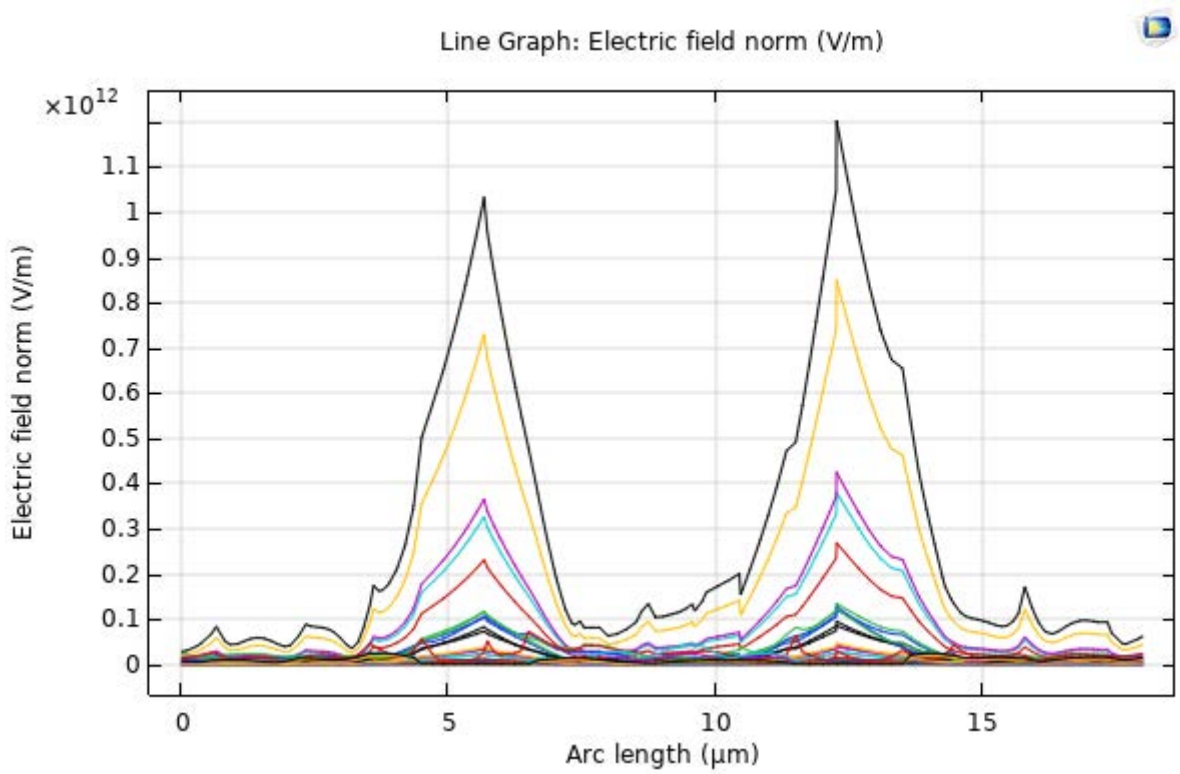


Fig. 3.1.4. Output field distribution for r = 2.5, t =2, with phi-phased illumination.

With the exception of the absence of a slant (on a roughly linear distribution in the core) the result obtained from in-phase illumination, as shown in Fig. 3.1.5., is similar to that obtained from phi-phase illumination. Such uniform, or flat, distributions can be useful.

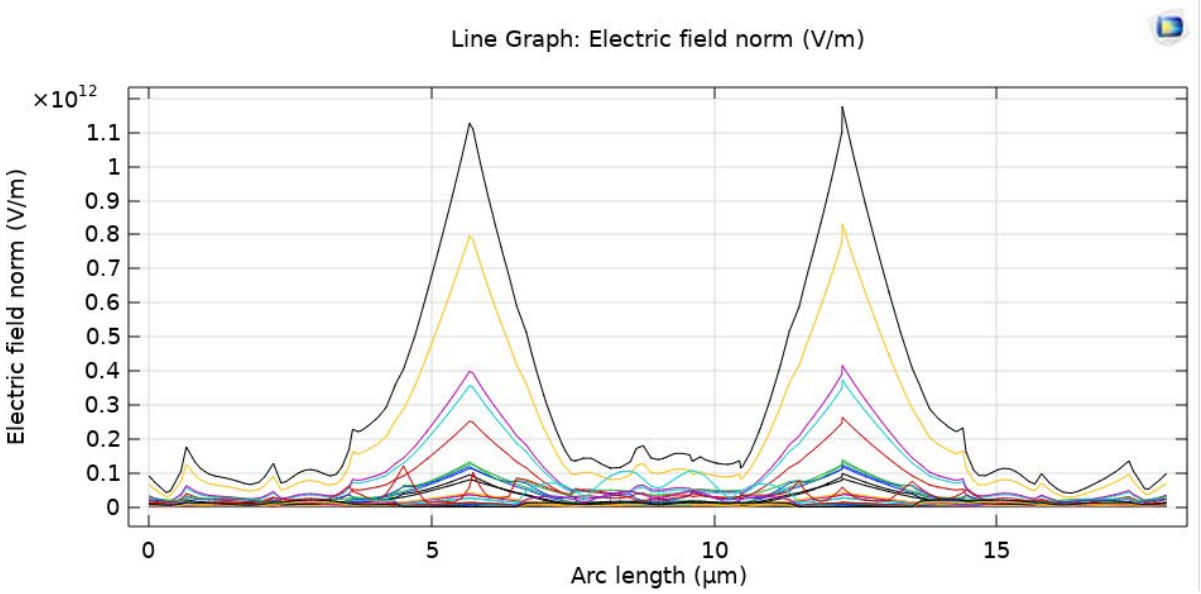


Fig. 3.1.5. Output field distribution for r = 2.5, t =2, with in-phase illumination.

The general aspects of the behaviors observed above carry over to the case of r =5, t =3 which is discussed in the following. In Fig. 3.1.6 however we see a dramatic increase in the amplitude of the core field (now at roughly the same amplitude as that of the cladding).

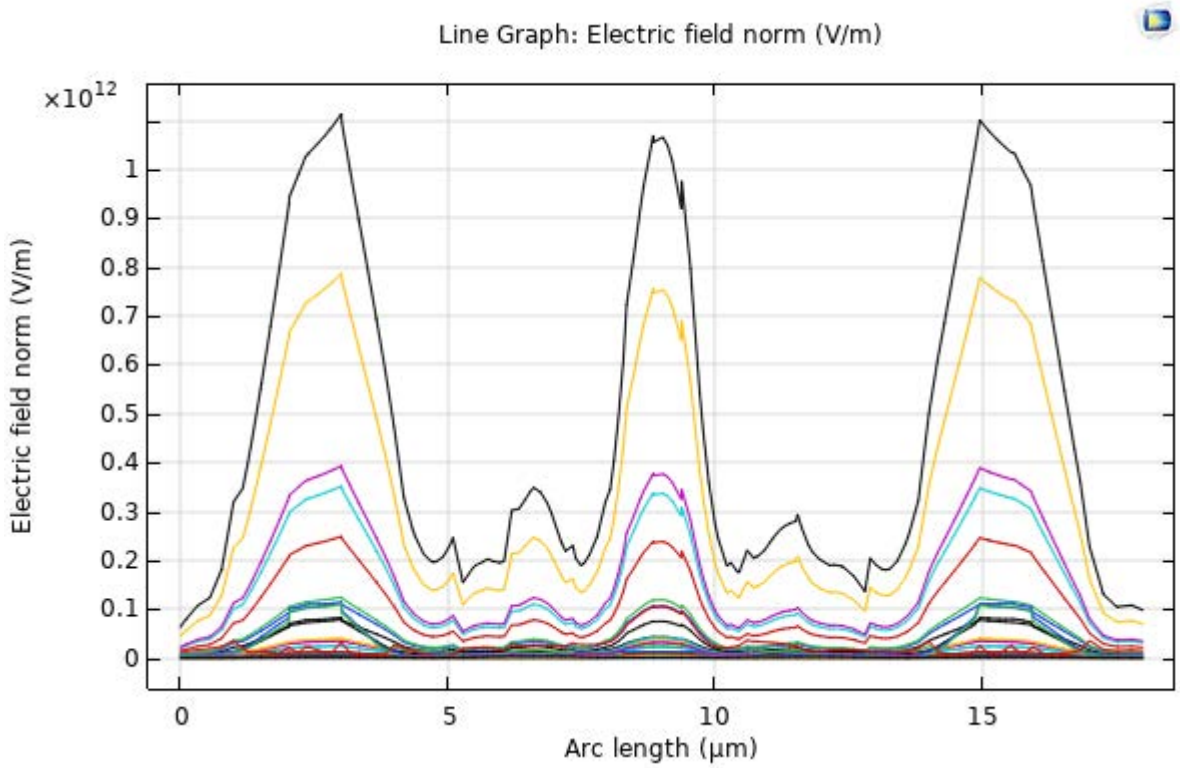


Fig. 3.1.6. Output field distribution for r = 5, t = 3, with radial illumination.

In Fig. 3.1.7 we see that phi-polarized illumination again creates essentially the opposite effect when compared to radial illumination. In this case we have an even deeper null at core center, as well as smooth peaks primarily confined within the cladding.

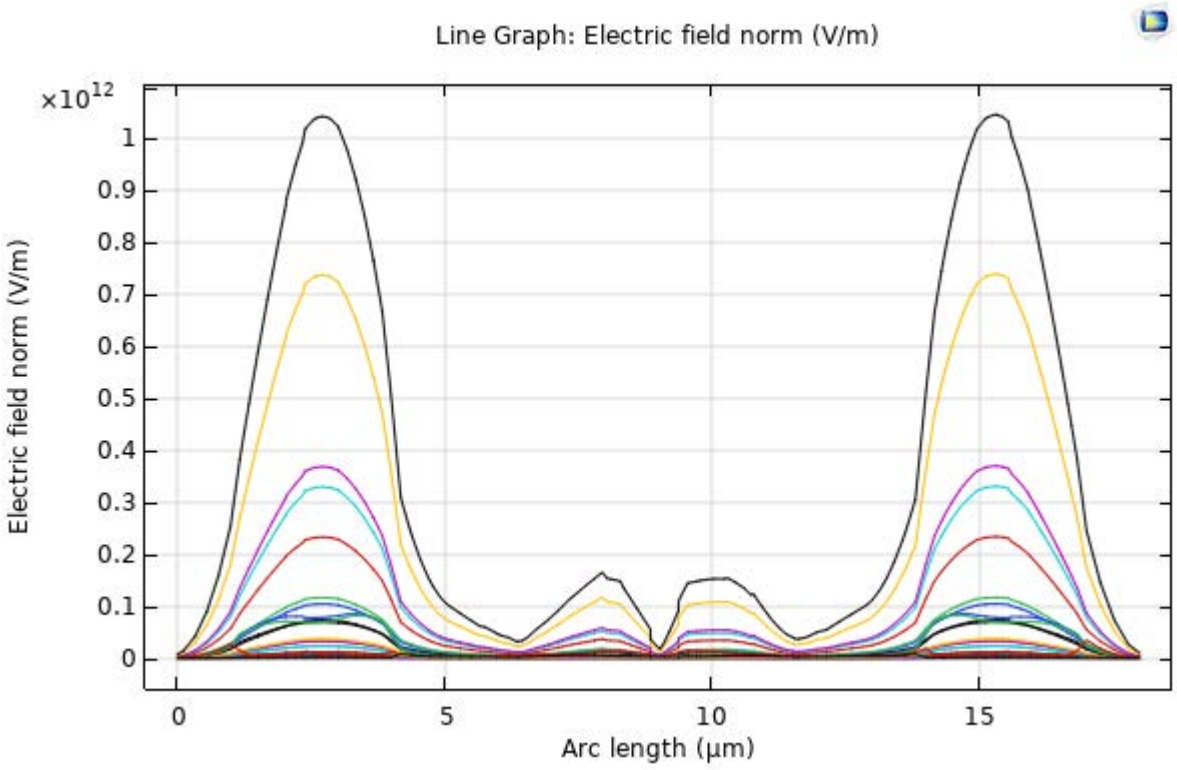


Fig. 3.1.7. Output field distribution for r = 5, t = 3, with phi-polarized illumination.

Again, the result obtained from phi-phase illumination has a slight slant on a roughly linear distribution across the core, as shown in Fig. 3.1.8. In this (r = 5, t = 3) case however, the core field is larger and is sitting on top of a slight pedestal.

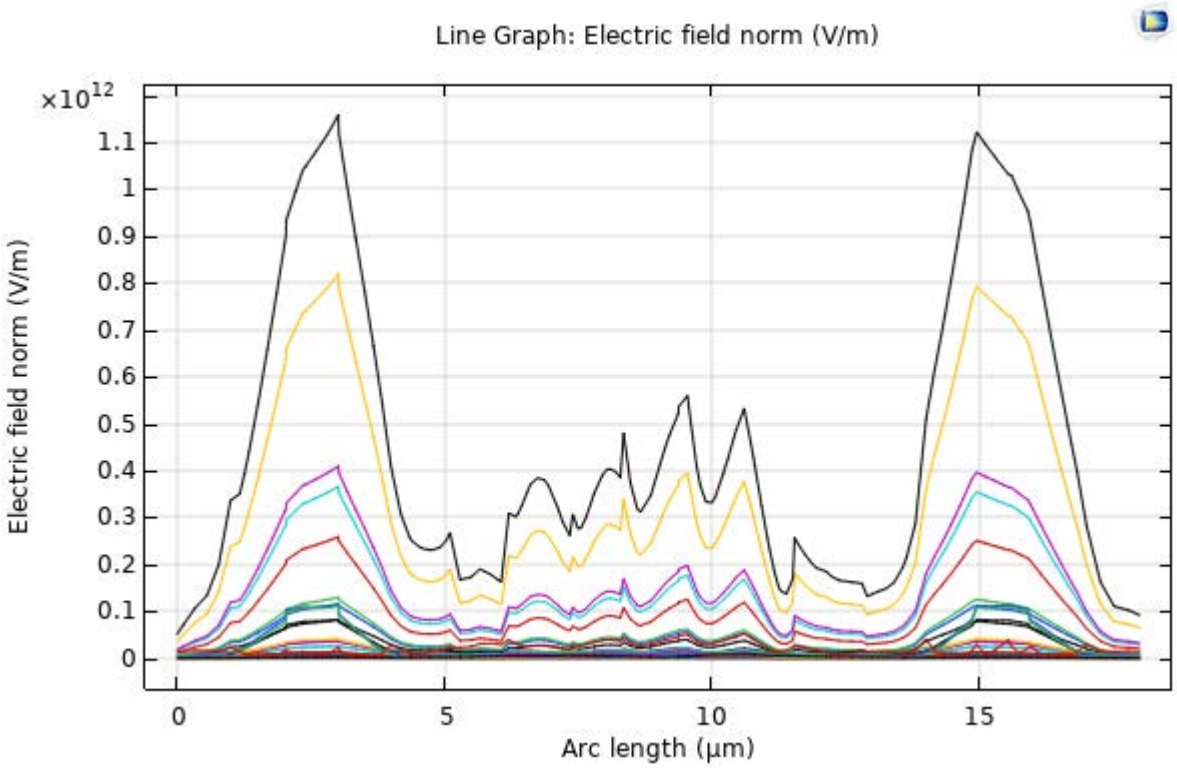


Fig. 3.1.8. Output field distribution for r = 5, t = 3, with phi-phased illumination.

In Fig. 3.1.9 we see that in-phase illumination results in a core distribution which is approaching that of a Gaussian (rather than a flat-top Gaussian) in this (r = 5, t = 3) case. For other r and t combinations we have seen flat-top Gaussian core distributions resulting from in-phase illumination.

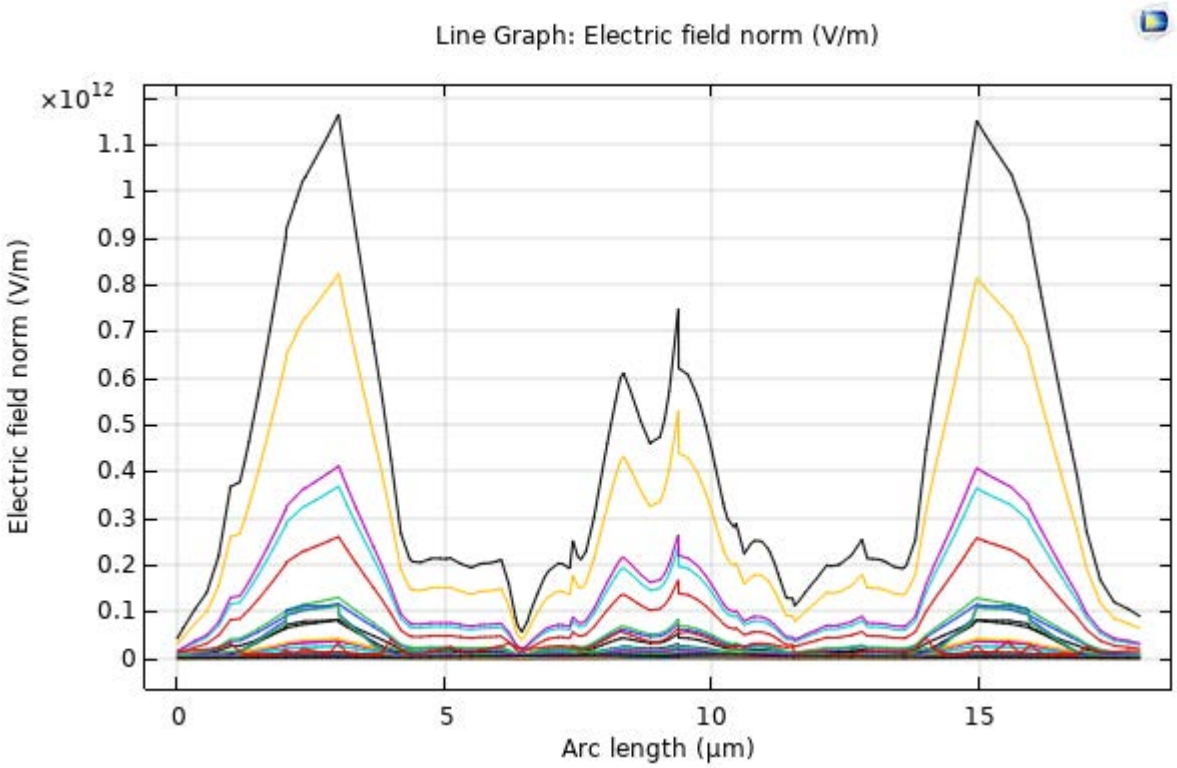


Fig. 3.1.9. Output field distribution for r = 5, t = 3, with in-phase illumination.

A plethora of combinations of polarization/phasing schemes with various r and t have been simulated. For applications which prefer high core power with Gaussian beam profile the radial polarization appears to be the most promising and we are continuing to optimize over grids of various r and t.

3.1.5 *Summary of Significant Findings and Mission Impact*

(A) Our pre-burst optical pumping scheme simulations showed that we can drop the pump power costs by a factor of 40 with pre-burst ASE power levels below the heating level tolerance of 100 μW. UMKC invention disclosure filed 02JUN2020.

(B) For a proposed system gain of 8 million, a linear gain theory predicted the in-burst ASE would be over our heating level spec. by a factor of 3960, but by exploiting the nonlinearity of gain saturation we find that we can suppress the ASE by over 7000. UMKC invention disclosure filed 14SEP2020.

(C) Achieved initial practical device designs that exploit gain saturation, which remained below damage thresholds, via staged designs of different mode diameters NOV2020.

(D) Models of the impact of ASE on timing jitter in the presence of dispersion and/or nonlinearities were established JUL2020.

(E) The design of a proof-of-concept experiment demonstrating a cost-reduced optical pumping scheme was finalized MAR2021.

(F) We made (to our knowledge) the first observation of self-focusing effects that are not determined by beam power alone. We found instead that these can also be controlled via the geometric factors within a waveguide (such as fiber core diameter) MAY2021.

We additionally made (to our knowledge) the first observation that a mode exists in the air within a simple glass tube into which we can couple energy from the mode in the glass. Thus, an amplifier (in the doped and pumped glass) can operate at higher powers JUNE2021.

We found conditions under which 0.25 GW of power can exist in the tube's air-core mode when its glass-cladding mode is at a power level near 0.5 GW JULY2021.

Advancements in the very high-power operating point (tens of GW) of our tubular optical amplifier (and the existence, size and spatial uniformity of its air-core mode) were shown to permit a single laser to trigger an array of several (up to 100) Si-PCSS – reducing the laser system cost and eliminating the optical timing jitter constraint. The symmetry breaking of the scattering from self-focusing in a curved waveguide was shown to enable such AUG2021.

4 Photoconductive Switch Innovation

4.1 Characterizing and Optimizing On-State Resistance in GaN:X PCSS

(Heather Thompson)

4.1.1 *Problem Statement, Approach, and Context*

***Primary Problem*:** Traditionally, RF generation using photoconductive semiconductor switches (PCSS) relies on materials such as silicon (Si) or gallium arsenide (GaAs), due to their availability and low cost; however, as these applications begin to require higher operating frequencies, powers, and temperatures, with the same or reduced system form-factor, the theoretical operating limits of these materials are being reached.

***Solution Space*:** By exploiting the 3.4 eV bandgap, 1000 cm^2/Vs electron mobility, and thermal properties of GaN, it is possible to realize pulsed-power applications requiring up to a 5 MV/cm critical field, high-frequency operation, and ~400 °C operating temperature, respectively.

Sub-Problem: One of the most important problems in minimizing conduction losses, maximizing efficiency, and reducing thermal issues in compensated, semi-insulating GaN:X (i.e., GaN:X with X=C, Fe…) PCSS-based systems is achieving <1 Ω on-state resistance by optimizing the modifiable parameters of GaN:X at the material, device, and system levels, while still maintaining quick switch turn-off time and low turn-off losses.

***State-of-the-Art (SOTA*):** PCSS-based RF generation systems using Si, SiC, or GaAs can achieve MW-range output power, ones-of-gigawatts frequency content, and electrical efficiency of ~60% that require increased laser energies and device size to reach maximum efficiency and necessary operating power limits, respectively.

***Deficiency in the SOTA*:** Si-, SiC-, and GaAs-based PCSS require ones-of-mJ of incident laser energy to achieve <1 Ω on-state resistance, leading to increased incident laser requirements, increased heating in devices, and devices that are ones-of-cm^2 in area for the necessary peak power and operating temperatures.

***Solution Proposed*:** Use simulation and available experimental results, from the literature and collected results at UMKC, to optimize the variable parameters of GaN:X PCSS to achieve <1 Ω on-state resistance with increased electrical and optical efficiency while maintaining a quick switch turn-off time and low turn-off losses.

Risks, Payoffs, and Challenges:

***Challenges*:** The high cost of material leads to a limited number of devices available for experimental testing and analysis, requiring a majority of the optimization studies to be performed using simulation software (COMSOL and TCAD).

***Risks*:** Simulation results may differ from experimental results for certain PCSS parameters due to particular photogeneration and recombination parameters not being included in models along with non-ideal, real-world experiments requiring additions such as encapsulation material or other changes not fully addressed in simulation.

***Payoffs*:** By minimizing the conduction losses in GaN PCSS, a compact, tunable RF source can be realized with increased efficiency and SWAP-C^2 capabilities.

4.1.2 Tasks and Milestones / Timeline / Status

(A) Milestone – Determine material, device, and system parameters that affect on-state resistance and which of these can be best leveraged to reduce on-state losses and heating.

1. Task – Literature study of photoelectric on-state resistance to understand how this parameter can be optimized to reduce conduction and on-state losses during PCSS operation *[ongoing].*
2. Task – Literature review of on-state resistance studies performed using GaN-based photoelectric devices to determine areas to further study *[ongoing].*
3. Task – Determine project milestones, tasks, and timeline for optimizing on-state resistance in GaN PCSS *[ongoing]*.

(B) Milestone – Build model of GaN PCSS in TCAD and COMSOL to begin simulation studies *[ongoing].*

1. Task – Build simple, working preliminary GaN PCSS model in COMSOL that can be subsequently altered for more complex analysis of on-state resistance *[Complete – JAN 22]*.
2. Task – Build a working preliminary GaN PCSS model in TCAD to determine which modeling software will provide accurate, efficient results for different parameters affecting on-state resistance *[Complete – MARCH 22]*.
3. Task – Determine parameters that can be altered using TCAD and design studies using this program *[Ongoing]*.
4. Task – Compare simulation results with available experimental results to determine validity of models using TCAD and/or COMSOL *[APRIL 22]*.
5. Task – Set up parametric sweep studies *[MAY 22]*.

(C) Milestone – Determine device level characteristics and relationship with material characteristics—relationship between device and material level characteristics—that can be altered in simulation allowing for optimization of on-state resistance and efficiency of GaN:C PCSS and complete study on leveraging these parameters.

(D) Milestone – Determine circuit and incident photon source characteristics to be studied using simulation towards minimizing on-state resistance in GaN:C PCSS.

(E) Milestone – Design simulation based on Liu, 2021 paper [1] using nano-structures on the surface of the device to overcome shallow absorption depth.

(F) Completion of manuscript on optimizing on-state resistance in GaN:C PCSS *[Ongoing]*

4.1.3 *Progress Made Since Last Report*

(A) A study of GaAs PCSS showed that using a smaller, focused incident laser with higher energy density results in lower on-state resistance than spreading out the same laser energy over a greater portion of the active area, leading to lower energy density. This shows adding additional optics to spread out the laser power over a greater portion of the active region may increase on-state resistance when the energy and pulse width are held constant to maintain a constant average power.

(B) A working GaN PCSS model has been constructed using Silvaco TCAD, and initial results will be compared to experimental results for validation in the next report.

4.1.4 *Technical Results.*

(A) An additional consideration towards minimizing on-state resistance without adding to incident laser energy, and costs, is the energy density and spot shape of the laser which is changed by keeping the laser energy and pulse width constant to maintain a steady average power. In Zhang 2015, the authors used GaAs PCSS devices with an incident energy of 1 μJ and pulse width of 300 ns to obtain an average laser power of 33.3 W for varying spot shapes and energy densities as shown in Figure 4.1.1. It was found that the more focused shape, with the highest energy density, achieved the lowest on-state resistance (Figure 4.1.2) [2]. This finding shows that using additional optics to spread out the incident laser spot size to the entire active area may increase the on-state resistance of the device compared to using a focused, smaller spot size.

Table 1. Performance details of laser pulses.

spot shape	Size(mm^2)	Energy density($uJ.mm^{-2}$)
scattered	16.24	0.06
Long-striped	9.975	0.1
focused	0.5027	1.99

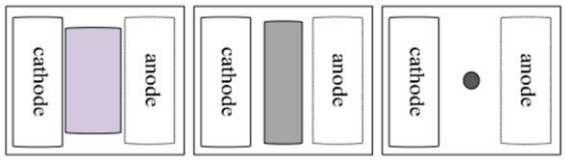


Figure 4.1.1: (left) Incident laser characteristics for incident laser power of 33.3 W with varying spot shapes and energy densities incident on the GaAs PCSS. (Right) Illustration of the various spot shapes used in the GaAs PCSS study.

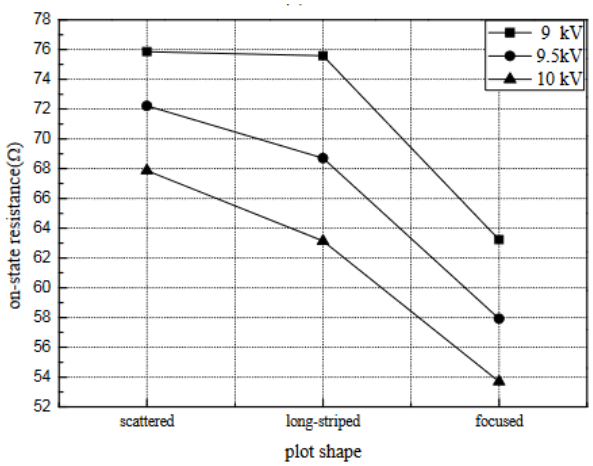


Figure 4.1.2: On-state resistance results from using different laser spot shapes and energy densities.

(B) Towards using simulation to understand how different device and material parameters affect on-state resistance in GaN:C PCSS, a working simulation has been constructed using Silvaco TCAD and initial simulation results and comparison of results to experimental data is expected in the next report.

4.1.5 *Summary of Significant Findings and Mission Impact*

(A) An ongoing literature review continues towards determining alterable parameters to optimize on-state resistance in GaN PCSS, leading to a material option that provides improved efficiency and SWAP-C2 capabilities for a PCSS-based RF generation system. Due to minimal jitter operation and increased device lifespan, focus will be on linear mode operation of GaN PCSS, limiting the geometry to lateral devices. Focus will also be on intrinsic carrier activation due to the increased optical efficiency offered over extrinsic activation.

Additionally, a possible way of improving optical efficiency without increasing incident laser energy (number of photons) is being considered from work towards minimizing on-state resistance and maximizing efficiency in GaAs PCSS devices. These devices include the addition of nanostructure wall array in the active area (gap length) of the device leading to an increased active volume in the device and overcoming on-state resistance minimization limitations due to shallow absorption depth of the photon source. By utilizing an array with fins >1/2 the incident laser wavelength, to prevent scattering, photocurrent was increased from 1.9 μA to 106 μA for a trigger

fluence of 3.8 mW/cm^2. This device alteration will be replicated in simulation of GaN:C PCSS devices to determine the increase in efficiency that could be achieved through increasing the effective volume of the active device area.

A working GaN PCSS model has been created using both COMSOL Multiphysics and Silvaco TCAD to allow for parametric studies towards minimizing on-state resistance in GaN PCSS without the need for manufacturing several iterations of devices.

(C) Work towards a manuscript based on optimizing on-state resistance in GaN:C PCSS has been started with the first version of the introduction written and currently being edited.

4.1.6 *References*

[1] R. Liu, A. Shang, C.-J. Chen, Y. G. Lee, and S. Yin, “Nanostructure Enabled Lower On-State Resistance and Longer Lock-on Time GaAs Photoconductive Semiconductor Switches,” Opt. Letters, vol. 46, no. 4, pp. 825–828, 2021.

[2] T. Zhang, K. Liu, S. Gao, and Y. Shi, “Characteristics of GaAs PCSS triggered by 1 μJ laser diode,” IEEE Trans. Dielectr. Electr. Insul., vol. 22, no. 4, pp. 1991–1996, 2015.

5 Drift-Step-Recovery-Diode-Based Source Alternatives

5.1 Drift-Step Recovery Diode and Pulse Shaping Device Optimization

(Jay Eifler)

5.1.1 *Problem Statement, Approach, and Context*

Primary Problem: Drift-step recovery diodes (DSRDs) and DSRD-based pulsed power systems are competitive with PCSS-based systems for HPM cUAS, with the benefit of not requiring a laser. Maximizing peak power while maintaining characteristic ns-order DSRD rise times requires optimization of the DSRD device design and pulser. Other considerations are for compactness, low-jitter, cooling required, and additional pulse-sharpening device within the pulse shaping head circuit. Additional goals for pulse repetition frequency are also to be satisfied for various applications.

Solution Space: By altering DSRD device parameters (geometry, doping, irradiation), optimize single-die and stack designs for peak power and risetime within various inductive pulser circuit topologies. Also optimize the pulse sharpening device (PSD) within the pulse shaping head circuit.

Sub-Problem 1: TCAD and SPICE models of the DSRD are inaccurate and must be improved. PSD models have not been developed.

Sub-Problem 2: Inductive pulser designs are complicated by the DSRD (and PSD) parameter variability. Use TCAD and/or SPICE models to account for variability and improve pulser design.

State-of-the-Art (SOTA): MW peak power and ns-order risetimes have been achieved in DSRD-based pulsed-power systems employing DSRD stacks for higher voltage holding and parallel lines of DSRD to increase current. PSD have sharpened DSRD pulses to 100 ps-order.

Deficiency in the SOTA: A lack of accurate TCAD and SPICE models make design of DSRD and DSRD-based inductive pulser circuit topologies (with or without PSDs) difficult to the level of tens of MW of peak power while maintaining ns-order risetime (or sharpened 100 ps-order). In addition, DSRD (and PSD) fabrication variabilities further complicate pulser design.

Solution Proposed: Develop further modeling capabilities in TCAD and SPICE for DSRD and DSRD-based inductive pulser circuit topologies to optimize DSRD and inductive pulser designs, especially for maximum peak power and minimum risetime, but also for low-jitter, reduced cooling, and compactness. Additionally, optimize pulser with PSD and pulse shaping head circuit.

Relevance to OSPRES Grant Objective: DSRD-based systems eliminate laser requirements necessary for PCSSs and are competitive in terms of thermal requirements and peak power. With sharpening, the DSRD-based systems can produce comparable risetimes. The SWaPC^2 cooling requirements of HPM cUAS systems can be solved with DSRD-based pulsed power systems, and low-jitter DSRD-based systems can be used for beam-steering in phased-arrays.

Risks, Payoffs, and Challenges: DSRD must be arrayed and staged to increase current since DSRD are limited in their ability to operate at high current densities. DSRD and PSD must also be stacked to operate at high voltages necessary for high peak power and maintain low risetimes. The stacking methods can damage dies and produce variable results in risetime and DSRD diffused doping profiles can be difficult to achieve and may require epitaxial methods. SPICE device models for DSRD are unavailable and must be developed, and questions remain about TCAD limitations for DSRD and PSD modeling.

5.1.2 Tasks and Milestones / Timeline / Status

(A) Milestone – Develop DSRD SPICE model within SmartSpice using the CMC diode model (built-in and Verilog-A).

1. Task – Develop accurate forward IV, reverse CV and reverse recovery testing (RRT) modeling in CMC diode model using either built-in (faster) or Verilog-A (customizable) models; On-going [APR-JUN 2022];

2. Task – Develop reverse IV and forward CV modeling and parameters in SmartSpice CMC diode models (built-in and/or Verilog-A); Preliminary exploration [MAY-JUL 2022];

3. Task – Develop 1x1 DSRD-based pulser recovery parameters within CMC diode model of SmartSpice (built-in or Verilog-A) and compare to RRT parameters; On-going [APR-JUL 2022];

(B) Milestone – Complete LTSPICE parameterization of the standard diode model for DSRD inventory.

1. Task – Finish Gen2.2 DSRD LTSPICE parameter extraction; On-going as received [APR-MAY 2022];

(C) Milestone – Develop automated fitting procedures for developed LTSPICE and/or SmartSpice DSRD models.

1. Task – Improve speed/accuracy/size of brute force fitting methods for LTSPICE and SmartSpice diode models; On-going [APR-JUN 2022];

2. Task – Improve python-based fitting methods for diode models used in LTSPICE and/or SmartSpice; On-going [APR-JUN 2022];

3. Task – Improve use of SmartSpice Optimizer for parameter fitting of diode models; On-going [APR-JUN 2022];

4. Task – Develop automated fitting procedures for Verilog-A diode models (CMC or custom); Preliminary exploration [APR-AUG 2022];

(D) Milestone – Convert manufacturer PSPICE and PSPICE/LTSPICE unencrypted device models into SmartSpice format for use in DSRD-based pulser simulation.

1. Task – Convert unencrypted PSPICE/LTSPICE Cree MOSFET model into SmartSpice format; On-going [APR-JUN 2022];

2. Task – Convert unencrypted Texas Instruments Gate Driver model from PSPICE into SmartSpice format; On-going [APR-JUN 2022];

(E) Milestone – Develop DSRD parameters for new 371A semiconductor analyzer measurement data (forward IV and reverse IV).

1. Task – Develop standard diode LTSPICE 371A semiconductor analyzer measurement data parameters; On-going [APR-JUN 2022];

2. Task – Develop SmartSpice CMC (Verilog-A) 371A semiconductor analyzer measurement data parameters; On-going [APR-JUN 2022];

(F) Milestone – Determine performance of doping profiles within TCAD

1. Task – Determine TCAD performance of SOS, dynistor and thyristor doping profiles; Doping profiles not yet received; [?-? 2022];

2. Task – Determine TCAD performance of square root DSRD doping profiles; Not yet begun [? 2022];

3. Task – Determine TCAD performance of Gen3 manufacturer doping profiles; Not yet begun [? 2022];

4. Task – Determine recovery behavior of DSRD doping profiles within TCAD for development of custom Verilog-A CMC-based DSRD models; Not yet begun [?-? 2022];

5. Task – Determine effect of doping and defects on DSRD forward IV performance; Not yet begun [?-? 2022].

5.1.3 *Progress Made Since Last Report*

(A.1) Develop CMC Diode Forward IV and Reverse CV parameters

DSRD EG1562 has been fit for forward IV and zero-bias junction capacitance within the CMC diode model of SmartSpice for use in DSRD-based pulser simulations.

(A.3) Develop 1x1 DSRD-based pulser recovery parameters for the CMC diode model

Initial recovery parameters have been determined for the CMC diode model in SmartSpice for EG1562 in the 1x1 DSRD-based pulser. To accomplish the recovery parameter fit, the CMC diode model within SmartSpice was fit to an inhouse DSRD for forward IV and zero-bias junction capacitance and then a large recovery parameter study was performed to determine the best parameters for 1x1 pulser performance. The peak load voltage was well matched and the risetime was fairly close resulting in the best fit to date (previous 10% match used an adjusted CJO within the standard diode model that is

not realistic) obtained for a DSRD within the 1x1 pulser. The experimental peak load voltage was 3296 V (simulation was 3281 V) and 10/90 risetime was 5.76 ns (simulation was 4.61ns). The peak load voltage percent error was 0.4% and 10/90 risetime was 20%. Details of the pre- and post-pulse shape were not correct likely due to the forward IV being only for low voltage and current. Further studies are being completed to match the peak load voltage, risetime, pulsewidth and voltage riserate of the output pulse, as well as, the matching pre- and post-pulse shape.

(B.1) LTSPICE Standard Diode Model Parameter Development for DSRD Inventory

LTSPICE parameters have been extracted for the Gen2.2 DSRD from the first 6 rounds of the variability study (see Section 5.3).

(D.1-2) Convert manufacturer MOSFET and Gate Driver models into SmartSpice format

The unencrypted Cree MOSFET model (PSPICE/LTSPICE model) and the unencrypted Texas Instruments Gate Driver model (PSPICE model) have been converted into SmartSpice. These converted models were then tested in SmartSpice simulations of the 1x1 DSRD-based pulser and compared successfully to their performance in LTSPICE.

(E.1-2) Develop forward IV parameters for 371A semiconductor measurement data

Published data [1] on power diode forward IV has shown similar forward IV curves as obtained from the 371A semiconductor analyzer for EG1608. Although thermo-couple measurements and a heat sink have not been integrated, forward IV should now be collected using the 371A.

5.1.4 *Technical Results*

(A.1) Develop CMC Diode Forward IV and Reverse CV parameters

DSRD EG1562 was fit in the CMC diode model for forward IV (from the picoammeter data) resulting in a reasonably close match. The fit was obtained through a parameter sweep of IS (IDSATRBOT in CMC diode model) and N (in part NFABOT in CMC diode model) using the brute force method. Additional parameters NJH (high-injection emission coefficient) and NJDV (transition slope of emission coefficient) were adjusted manually in conjunction with the parameter sweep to obtain the fit. The reverse IV was not adjusted but appeared reasonable and was not fit to the reverse IV experimental data (this has not been performed for any of the previous model fits). The reverse CV was only adjusted to match the zero-bias junction capacitance leaving the grading coefficient at the default 0.5 (PBOT in CMC diode model). With these two curves fits the CMC diode was reasonably well parameterized for studies of matching pulser performance by adjusting the recovery parameters. In Figure 5.1.1 is shown the forward IV fit within SmartSpice using the CMC diode model and compared to the experimental data from the picoammeter. The fit had

average absolute deviation error of 1.51×10^{-4} which is close to but not below the 1×10^{-4} error established from practice (the resulting fit is close but not very close visually).

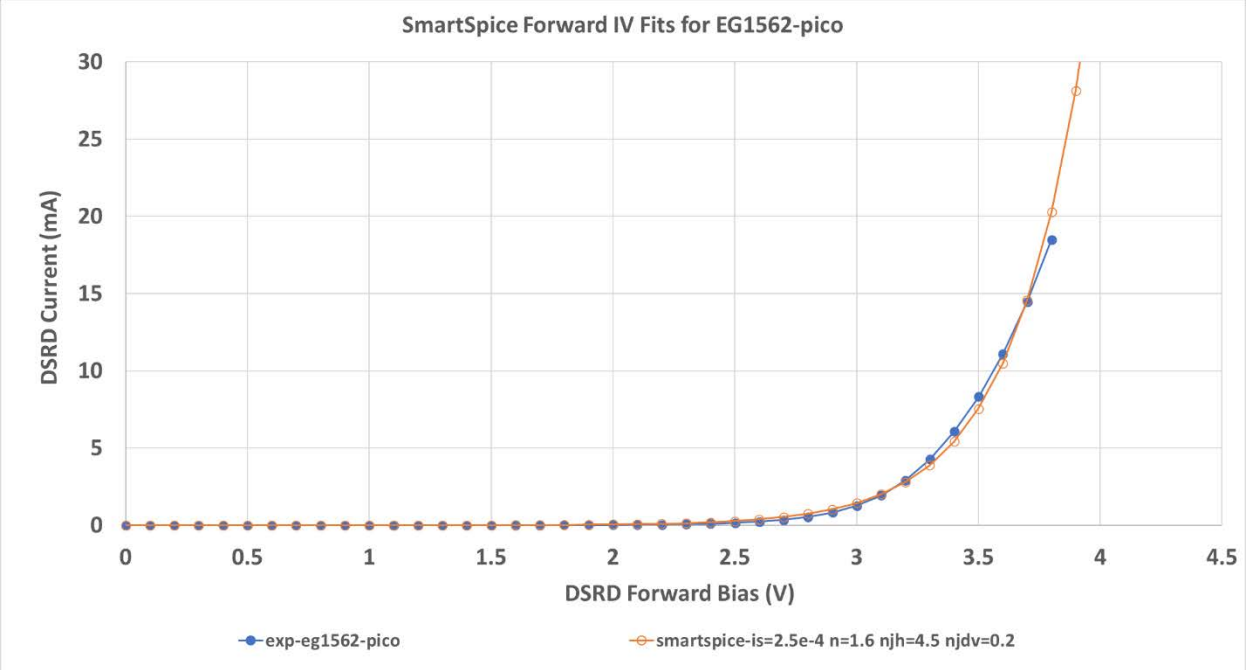


Figure 5.1.1. Forward IV fit for EG1562 within SmartSpice using the CMC diode model.

New fits of the diode stock can be performed for the CMC diode model within SmartSpice but are awaiting the receiving and analysis of higher voltage and current forward IV using the 371A semiconductor analyzer. Fits to the picoammeter data will be performed after the brute force fitting method is better understood for the CMC diode model.

(A.3) Develop 1x1 DSRD-based pulser recovery parameters for the CMC diode model

The CMC diode model within SmartSpice has been fit for 1x1 pulser performance using DSRD EG1562. The DSRD EG1562 was fit within the CMC diode model using picoammeter data (for the forward IV) which does not capture the higher voltage and current operation of the diode. First manual guesses of the recovery parameters achieved a reasonably close fit in pulser performance in terms of the peak load voltage and risetime. Next a large parameter study was performed (9600 simulations) adjusting four of the six recovery parameters. The fit obtained is compared to experiment in Figure 5.1.2. The six recovery parameters are: INJ1 (recovery charge carrier density, should be close to 1 for physically correct model), INJ2 (high-injection recovery charge carrier density), NQS (carrier delay time), DEPNQS (depletion delay time), WI (width of intrinsic region), and TAU (carrier lifetime).

In a separate smaller study varying one recovery parameter at a time, the effect of a parameter variation with other all other parameters fixed was examined. From this study INJ2 was not observed to produce an effect on pulser performance and so was excluded

from the larger recovery parameter study. INJ1 was observed to scale the peak load voltage as it is adjusted well above 1 (up to 1000 in our model), but this is not physically correct within the PIN diode model of the CMC diode model. However, adjusting INJ1 parameter was necessary to fit the data for DSRD within the pulser. Further studies are forthcoming to better understand the CMC diode recovery model. NQS and DEPNQS were also set to the same value to reduce the number of parameters to four for the brute force fitting method.

The SmartSpice post-pulse hump in Figure 5.1.2 was present in all output pulses and is likely caused by the forward IV and reverse CV fitting used. An improved fit of the forward and reverse CV and a higher current and voltage forward IV should produce better pre- and post-pulse shape matching (and likely improved pulsewidth fitting). The EG1562 experimental peak load voltage was 3296 V (3281 V for simulation) and 10/90 risetime was 5.76 ns (4.61 ns for simulation). The percent error for the peak load voltage is 0.4 % and for the 10/90 risetime 20%. In improved future fits the peak load voltage, 10/90 risetime, FWHM pulsewidth and 10/90 voltage riserate will be matched closely along with similar pre- and post-pulse shape. The study will culminate in an understanding of the limits of the CMC diode model to capture DSRD pulser performance. Using the Verilog-A CMC diode code the model can be modified for DSRD operation.

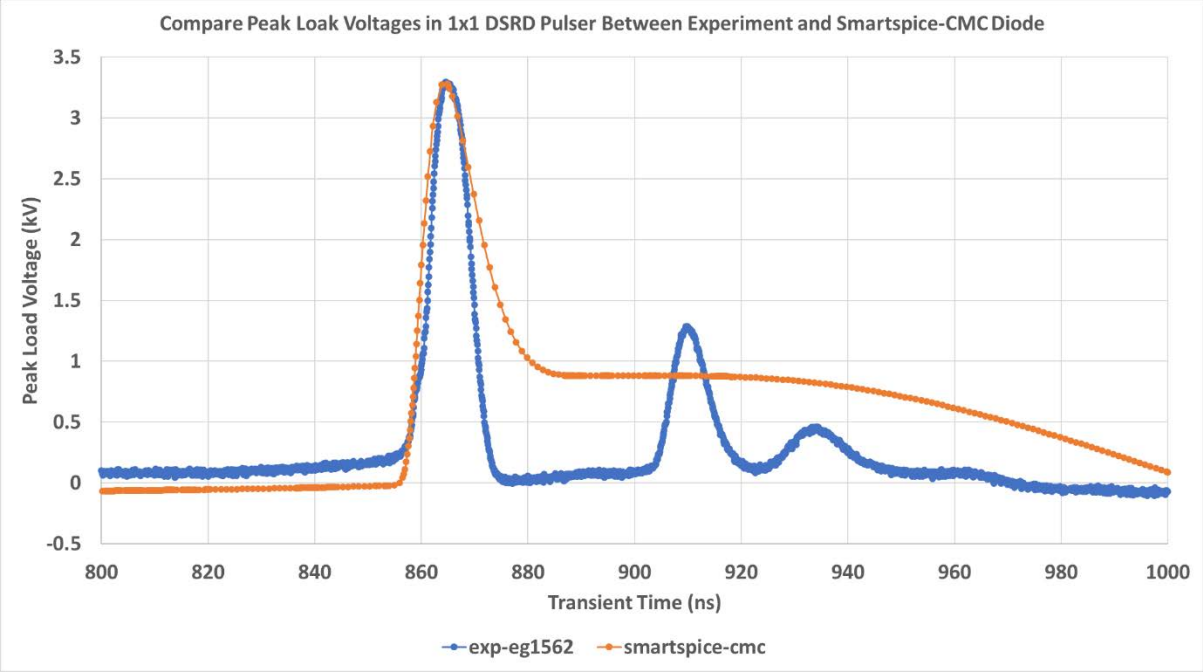


Figure 5.1.2. Comparison of experimental output pulse in the 1x1 DSRD-based pulser using the fitted CMC diode model within SmartSpice. This is the first reasonably close match of both peak load voltage and risetime within a realistic model.

(D.1-2) Convert manufacturer MOSFET and Gate Driver models into SmartSpice format

The Cree MOSFET and gate driver models used in LTSPICE do not work within SmartSpice. There are no available SmartSpice device models for manufacturer devices

(likely costly to purchase manufacturer models from Silvaco). Therefore, LTSPICE and PSPICE models must be converted into the SmartSpice code syntax and parameter definitions.

The MOSFET model was relatively easy to convert with a minimum of changes, in part due to earlier familiarity when developing a MOSFET model for use in TCAD. The MOSFET model was not subsequently tested for its standard curves and compared to either the LTSPICE model or the datasheet (LTSPICE model does not closely match datasheet). It should be noted that the behavioral model developed by Cree for their SiC Power MOSFET (C2M0045170P) was originally for PSPICE (usually the case) and was converted into LTSPICE (could be some issues). Other MOSFETs (or gate drivers) used in the pulser that have encrypted models for LTSPICE cannot be converted into SmartSpice.

The single channel isolated gate driver (Texas Instruments UCC5390-Q1) used to drive the SiC MOSFET is a PSPICE model. The use of the model in LTSPICE has been observed within online discussions but not confirmed by us with the manufacturers. In the process of converting the driver model from PSPICE to SmartSpice it was observed that a voltage-controlled switch in the model was incorrect for use in LTSPICE. Therefore, the PSPICE model must still be converted into LTSPICE to perform correctly. The model appears to have operated correctly in LTSPICE but if certain pin conditions are met the driver model as is will fail in LTSPICE. Diagnostics on the driver model have not been performed yet in LTSPICE or SmartSpice. However, the PSPICE model was successfully converted into SmartSpice (with the voltage-controlled switch fixed) and successfully used in SmartSpice for the 1x1 DSRD-based pulser (and compared to results within LTSPICE). Other manufacturer gate drivers may not have an unencrypted SPICE model that can be converted into SmartSpice. In this case, simpler gate driver models can be used (in practice this has been a voltage-controlled switch producing a trapezoidal input pulse of the correct pulsewidth and rise and fall times).

(E.1-2) Develop forward IV parameters for 371A semiconductor measurement data

Published data [1] on power diode forward IV has shown the previous DSRD 371A forward IV measurements may well be correct. Therefore, 371A data will be collected without a thermo-couple measurement or heat sink to assess the 371A forward IV data better, with thermo-couple measurements and heat sink forthcoming in future studies. In [1] the power diode forward IV appears to be a result of gradual N-side doping (to soften the hard recovery, uniform axial lifetime killing can also be used) and/or P-side local lifetime killing (to reduce P-emitter efficiency to make the forward voltage drop less susceptible to temperature variation). TCAD studies can be done to confirm these effects in power diodes or DSRD on the forward IV (we cannot perform thermal studies on stacked DSRD in TCAD).

5.1.5 *Summary of Significant Findings and Mission Impact*

(A) Development of DSRD Model Within SmartSpice CMC Diode Model

The SmartSpice circuit simulation software has been received in JAN 2022 and in FEB 2022 the Verilog-A CMC diode code was retrievable from the Si2 organization website. Development immediately began of the CMC diode model for DSRD modeling by producing forward IV, reverse CV and reverse recovery testing simulations and fitting to example DSRD in the inventory. Recovery parameter fitting within the 1x1 DSRD-based pulser has also begun. The capability of the CMC diode model for modeling DSRD can now be assessed. Any deficiencies in the CMC-DSRD model can be improved using the programmable Verilog-A code of the CMC diode model to include DSRD specific modeling equations based on theory, TCAD simulation, experiment and the literature.

(B) LTSPICE Standard Diode Model Parameter Development for DSRD Inventory

DSRD in the inventory of received diodes (legacy, EG and Gen2) have been fit for LTSPICE standard diode model parameters (for forward IV, reverse CV and reverse recovery testing) for use in LTSPICE DSRD-based pulser simulations and to provide another metric for the characterization of the DSRDs in comparison to pulser performance. Some details of the very low voltage and current forward IV have not been fit but the fitting is still very close when visually inspected in non-log format. Reverse IV have not been fit in the standard diode model since it cannot capture the behavior and breakdown has not yet been measured, only estimated. Forward CV measurement are problematic and not fit mostly since the forward CV parameters in the standard diode model are used for recovery modeling. Various methods exist in LTSPICE to improve fitting but are either inadequate (Vp or carrier viscosity) or non-realistic (adjustment of reverse CV parameters) but have produced fits within 10% error for DSRD-based pulser performance. Gen2.2 has not yet completed standard diode testing measurements but are being fit as received.

(C) Develop Automated Fitting Procedures for LTSPICE and SmartSpice

The current best method of fitting is using a brute force method of running LTSPICE or SmartSpice simulations sweeping over the desired parameter space. The brute force method can produce the most accurate fits but requires long simulation times and cannot be used to explore large parameter spaces easily (which is why more physically-based models using only measurable parameters is derisable). There is ultimately a limit to how quickly and accurately one can develop parameter sets. Another method is to program in the model equations into Python and use their curve fitting tools, however this method cannot incorporate circuit simulation and will therefore be less effective in producing accurate fits but is much faster in simulation time (can depend on how much parameter adjustments affect DSRD-based pulser performance on which method to use). The other fitting method is to use the built-in optimizer within SmartSpice, but the optimizer has not yet produced as good of fits consistently as the brute force method and will take some experience in using well.

(D) Conversion to SmartSpice of Manufacturer Device Models

Unfortunately, manufacturer device models are not openly available in SmartSpice only PSPICE and to some extent LTSPICE (usually converted from PSPICE). Therefore, the available PSPICE and PSPICE/LTSPICE models must be converted to the SmartSpice format, otherwise keeping the model the same. Note that encrypted models cannot be converted into SmartSpice, such models either have to be developed from scratch and either the datasheet or additional experimental tests used (or purchased from Silvaco for SmartSpice if available).

The unencrypted Cree MOSFET model has been converted into SmartSpice and tested within 1x1 DSRD-based pulser simulations and compared to LTSPICE simulations successfully. The unencrypted Texas Instruments gate driver model has also been converted into SmartSpice successfully. One issue with the driver model is it is intended for PSPICE but used often in online discussion in LTSPICE. However, close examination of the model shows that the model cannot perform correctly in all pin conditions in LTSPICE due to incorrect parameter types used in a voltage-controlled switch within the driver model. The voltage-controlled switch has been correctly implemented in the SmartSpice conversion and can be fixed for the LTSPICE version (Texas Instruments has not responded to inquires). Neither the MOSFET or gate driver models have been extensively diagnostically tested and compared to the datasheets which are often somewhat different to the free provided models (only so accurate).

(E) IV Parameter Development for 371A Semiconductor Analyzer Measurement Data

A 371A semiconductor analyzer has been acquired and setup for forward IV testing with the potential for higher voltage/current reverse IV testing and breakdown. Initially concerns arose about the shape of the forward IV and whether temperature distortion was occurring at the higher voltages and current available with the 371A compared to the picoammeter. However, published power diode forward IV have been discovered showing similar forward IV at room temperature. 371A testing will proceed by testing more DSRD and subsequently using thermocouples and/or heat sinks. 371A higher voltage/current forward IV testing is necessary to characterize the DSRD in the diode models to perform correctly in the DSRD-based pulser simulations. How accurate the forward IV must be, has not been determined, as well as, to what extent individual diodes can be reliably distinguished in modeling.

(F) TCAD-Based Doping Profile Performance Evaluation

Many DSRD TCAD simulation studies have been performed assessing the doping profiles used for the DSRD manufactured by SPT and in stock (this summary includes work from the past six months). The TCAD modeling has been temporarily on hold as effort is focused toward developing an accurate SPICE DSRD model due to the unavailability of manufacturer device models for MOSFETs and gate drivers within TCAD. A MOSFET model was developed for the Cree MOSFET for use within TCAD but still had some differences when used in pulser simulations, so the development of the DSRD SPICE model was prioritized so that manufacturer models (for MOSFETs and drivers) could be used.

Doping profiles are forthcoming for various SOS, dynistor and thyristor devices and TCAD will be used to assess their performance. Some interest has been expressed in assessing square-root doping profiles for DSRD. Gen3 doping profiles from the manufacturer have yet to be assessed within TCAD for performance differences with the requested doping profiles. As well, the recovery models within the CMC diode model are themselves based on PIN diode TCAD simulations and TCAD can perform DSRD doping profile specific simulations to determine model equations and parameters. Additionally, the forward IV behavior of our DSRD can be modeled as seen in the 371A semiconductor analyzer mesaurements. TCAD modeling will continue to be of use in device modeling since it is the only way to assess doping profiles.

5.1.6 *References*

[1] Chandra Bose, JV Subhaus, I. Imrie, H. Ostmann, and P. Ingram. “SONIC-A New Generation of Fast Recovery Diodes [D].” IXYS Semiconductor (2011).

5.2 Pioneering Drift-Step Recovery Diode Processing and Manufacturing

(Alex Usenko)

5.2.1 *Problem Statement, Approach, and Context*

Primary Problem: DSRDs have not increased in performance since the 1960’s due to reliance on deep diffusion manufacturing. Their voltage-to-risetime, dV/dt, remains about 10^{12} V/s. To achieve the 10^{13} V/s (10 kV/ns) voltage-to-risetime required by an all-solid-state HPM pulse generator in support of the Naval afloat mission, improving DSRD manufacturing techniques is critical.

Solution Space: Leverage applicable concepts from the mainstream silicon chipmaking industry and apply new manufacturing methods to DSRD processing.

Sub-Problem 1 – Diode silicon surface termination/passivation: The SOTA uses diode termination by a vertical wall. This design results in low breakdown voltage as it is limited by surface breakdown. To increase the diode breakdown voltage to closer to that of the bulk silicon breakdown voltage value, the vertical side wall design must be avoided.

Sub-Problem 2 – Stacking of DSRD dies: The SOTA is based on soldering of diode dies into a stack, which limits the stack lifetime to below 10^{12} pulses. Also, the SOTA did not apply the methodology of stacking wafers first, then cutting into dies. Switching to wafer level stacking will decrease the number of stacking operations by more than 100x.

Sub-Problem 3 – Packaging of stacked dies: *The* SOTA uses bare stacked DSRDs. Mounting the bare stack into a press-pack type package will improve long-term stability, such that the stack will survive a much higher number of pulses before it burns out.

State-of-the-Art (SOTA): In a recently published paper (2019),[1] the Russian St. Petersburg team at the Ioffe institute reported achieving a peak current density of 5 kA/cm^2 with a rise time of the output pulse front of ~2.3 ns, and a peak voltage across the load of 900 V (i.e., the peak switching power is 4.5×10^6 W/cm^2). The St. Petersburg team utilized deep diffusion technology. A competing team at Ekaterinburg, Russia [2] reports

similar pulse performance. Both teams use outdated deep diffusion technology. As one can see, there has not been any significant improvement in DSRD pulse performance since the pioneering work done in 1960 [3].

Deficiency in the SOTA: First, no DSRDs have been manufactured using epitaxy technology with doping profile optimization. Second, no DSRD processing method exists that integrates side passivation with silicon dioxide. Finally, an acceptable DSRD stacking process has yet to be developed.

Solution Proposed: Manufacture DSRDs within the continental United States using an epitaxial growth process leveraging the optimal characteristics (e.g., doping profile, carrier concentration) determined through the work performed by our simulation team (previous chapter of this report) and through working with industry partners at Semiconductor Power Technologies (SPT), Livermore Semiconductor Research Laboratories (LSRL) and Lawrence Livermore National Laboratory (LLNL – Voss Group).

Relevance to OSPRES Grant Objective: DSRD manufacturing technology is a major building block of short-pulse high-peak-power defense systems. Our new disruptive process flow for DSRDs enables not only manufacturing of DSRDs at scale, but within the continental United States (CONUS). In doing so we will redefine the SOTA by producing optimal DSRDs. Further, DSRDs will be used within best-in-class HPM pulse generators which become part of more advanced defense systems within the Navy arsenal.

Risks, Payoffs, and Challenges:

Risks: As the process of producing DSRDs using epitaxial growth with doping profile design is novel, uncharted territory, there is inherent risk to its success. Additionally, post-processing methods based on the discussions provided in the ***Sub-Problems*** section are not well-established.

Payoffs: Replacing traditional deep diffusion technology with a new process integration scheme would allow better DSRD pulse performance. Electrical breakdown voltage, reliability, and lifetime are expected to increase, and rise time on a load is expected to decrease.

5.2.2 Tasks and Milestones / Timeline / Status

(A) Milestone – Produce epitaxial DSRDs that contain optimal exponential doping profiles and carrier concentrations /estimated JUN22.

1. Task – Design of experiment on 25 wafers through negotiations with vendors / *MAY–JUL21* / Completed
2. Task – Perform DSRD stack epitaxy on 13 wafers at SVM Inc., and 25 wafers at LSRL / *JUN–AUG21* / Completed.
3. Develop process integration scheme that uses epitaxy instead of deep diffusion / *JUL–OCT21 /* Completed.

4. Compare traditional DSRD technology and suggested integration scheme. List disadvantages of traditional processes and define potential advantages of new processes / MAY–NOV21 / Completed.
5. Run Gen2 and Gen3 lots. Gen2 is on wafers with epi from SVM, Inc., Gen3 is on wafers with epi from LSRL. Gen2 uses the same BEOL as Gen1. Run BEOL of Gen3 – using our new patented processing scheme – TMAH etch, oxidation, selective electroless metal deposition, wafer bonding, sawing into diode stacks / OCT21–MAY22.
6. Submit Gen2 and Gen3 diode lots to UMKC team for pulsed performance measurements; collaborate with team on determining optimal doping profile through DoE (design of experiments) analysis by Minitab software / OCT21–MAY22.

(B) Milestone – Develop diode separation technique while keeping wafer integrity / Estimated completion FEB22.

1. Design lithography masks for short loop experiment, submit order to vendor. / MAR–APR21 / Completed.
2. Design short loop experiment for V-groove etching for diode separation. / MAR–APR21 / Completed.
3. Run short loop experiment for the diode separation by anisotropic etch; analyze results / MAY–OCT21 / Completed.
4. Based on results of previous short loop run, adjust equipment, and process recipes to achieve sufficient etch uniformity across the wafer. Run on updated equipment and recipe to prove etch uniformity. / Completed.
5. Design lithography masks for epi DSRD run; submit order to vendor. / OCT21 / Completed.
6. Run Gen3 lot through V-groove etch step, transfer lot to next process step. / Estimated MAY22.

(C) Develop Ohmic contact deposition technique integrable with epitaxy, diode side termination/passivation, and wafer bonding steps / estimated AUG21 - MAY22.

1. Design short loop experiment to determine technical feasibility of selective electroless deposition of metal stack as a method of Ohmic contact forming in the DSRD process integration scheme. / OCT21 / Completed.
2. Determine vendor from which to order electroless deposition kits; obtain quotes, order, receive the kits. / OCT21 / Completed.
3. Run short loop experiment – nickel-copper-tin stack electroless deposition on a blanket wafer. Analyze results. / DEC21 / Completed.
4. Develop process recipe for the metal stack deposition to use in Gen3 DSRD lot manufacturing / estimated JAN22.
5. Run the selective metallization step on Gen3 lot; transfer the lot to next processing step. / Estimated FEB22.

(D) Develop wafer stack bonding technique integrable with the rest of Gen3 process flow / estimated SEP–FEB22.
    1. Design short loop experiment for bonding 2 diode dies with Ni-Cu-Sn layers by solid–liquid interdiffusion. / SEP21 / Completed.
    2. Run 2 dies short loop experiment. Analyze results. / MAR22 / Completed.
    3. Test technical feasibility of multiple wafer bonding by bonding 10-wafer stack / estimated APR22.
    4. Upon proof of technical feasibility of 10-wafer stacking, develop process recipe to use for processing of Gen3 DSRD lot / estimated MAY22.
    5. Run wafer bonding step on Gen3 lot, transfer the lot to next processing step. / Estimated MAY22.

(E) Develop wafer stack sawing technique into DSRD stacks, integrable with the rest of Gen3 process flow / estimated NOV21–MAY22.
    1. Design sawing process using Disco saw available at Semiconductor Power Technologies for cutting 10-wafer stack / estimated JAN22.
    2. Run short loop cutting of blanket bonded 10-wafer stack. Analyze results. / Estimated FEB22.
    3. Develop process recipe for Disco saw tool to use for Gen3 lot. / Estimated MAY22.
    4. Run sawing step on Gen3 lot / estimated MAY22

(F) Develop diode side passivation process integrable with the rest of DSRD process flow.
    1. Test compatibility of thermal oxidation for the diode side passivation with preceding anisotropic etch step / estimated FEB22.
    2. Alternative diode side passivation process: design short loop experiment on room temperature oxidation by forming porous Si film and oxidizing the porous film / APR–OCT21 / Completed
    3. Run part of Gen3 lot using the oxidized porous Si as diode side passivation / estimated FEB22.
    4. Second alternative diode side passivation process: Design short loop experiment on room temperature oxide deposition from oversaturated fluorosilicic acid / estimated MAY–JAN22.
    5. Run part of Gen3 lot using the oxidized porous Si as diode side passivation / estimated FEB22.
    6. Choose the best from 3 methods of diode side surface passivation techniques / estimated FEB22.

(G) Develop a DSRD process based on out-diffusion (opposite to traditional in-diffusion process).
    1. Process Gen4 lot based on process integration scheme described in our patent application filed in / estimated MAY22.

(H) Find vendor that manufactures press-pack parts, order the parts, and encapsulate the DSRD stacks into the press-packs / estimated MAY22.

5.2.3 *Progress Made Since Last Report*

(A5) Gen3 lot fabrication. 23 wafers were received back from vendor Noel Technologies after lithography and nitride etch in windows. We have started processing the next step – singulation of individual dies while keeping wafer integrity – by anisotropic etching through windows; we use TMAH based recipe. Visual inspection of the first processed wafer showed many etch through pits in the Si_3N_3 mask. This means that the quality of the Si_3N_4 layer is unacceptably low. The Si_3N_4 layer was deposited by vendor Nova Electronic Materials, LLC, Flower Mound, TX. Unfortunately, we now must strip the bad nitride layer, deposit again, and do lithography, thus more delays.

(A5) Gen2 lot fabrication. Gen2-1 and Gen2-2 sublots are at the static and pulse performance characterization step at UMKC. The last Gen2-3 sublot from the 13-wafer Gen2 lot finished in the form of single dies, and is now waiting for stacking operation. A new die bonding process called SLID will be used for bonding, replacing traditional soldering.

(B4) Process step development: die separation on wafers by anisotropic etch in TMAH (tetramethylammonium hydroxide) based bath. Last month we found a new TMAH/DMSO (dimethyl sulfoxide) mixture etch chemistry which shows much better etch uniformity compared to all known TMAH/IPA or TMAH/surfactant chemistries. This month we determined etch rates for various TMAH/DMSO mixtures and chose a final production recipe. The first Gen3 wafer has been successfully processed at the die singulation step.

(D2) Process step development: stacking. Single diode dies have been successfully bonded using SLID (solid-liquid interdiffusion) technology.

(G1) Out-diffusion version of DSRD process. Sample p++ and n++ wafers were processed in-house in our diffusion furnace. Profiles of dopants after out-diffusion measured by SRP. Conclusion drawn why forming gas N+H shown lower out-diffusion than calculated. A new run in Argon+Hydrogen ambient planned.

5.2.4 *Technical Results*

(B) **Gen3 lot fabrication.** Late March the lot arrived from Noel vendor - for the next - anisotropic etch step in-house. Upon finishing the v-groove etch on the first wafer in the lot, the wafer has been visually inspected. The inspection shows a big count of pits etched through the silicon nitride mask, Fig.5.2.1 Conclusion is, unfortunately we must redo the mask/litho/etch processing steps on the rest 22 wafers. Processing of one – already TMAH etched wafer will continue and will give us the first finished Gen3 dies.

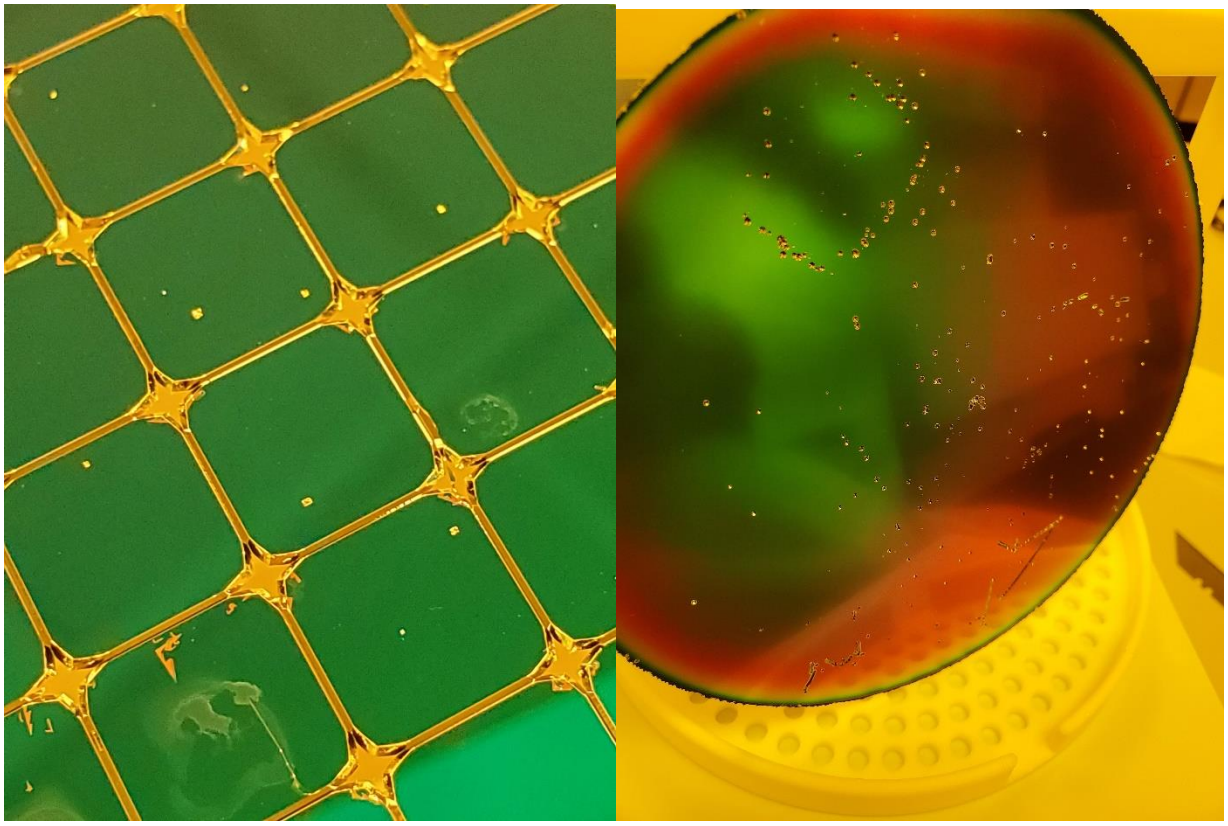


Figure 5.2.1. Etch pits on part of wafer front side – left, etch pit on wafer back side-right.

Except the etch pits failure – due to wrong choice of silicon nitride deposition vendor, the etch recipe we have developed on dummy wafers is now experimentally proven on the production wafers. The unique TMAH/DMSO (tetramethylammonium hydroxide/dimethyl sulfoxide) etching chemistry has shown expected results: our TMAH:DMSO:water 1:1:1 mixture at 80C recipe have been used for 20 hours etch of the first Gen3 wafer and gave full v-groove triangles on entire wafer. Fig.5.2.2 show examples of optical microscopy images focused either on wafer surface or on the deepest point of the v-groove. The full v-groove can be seen.

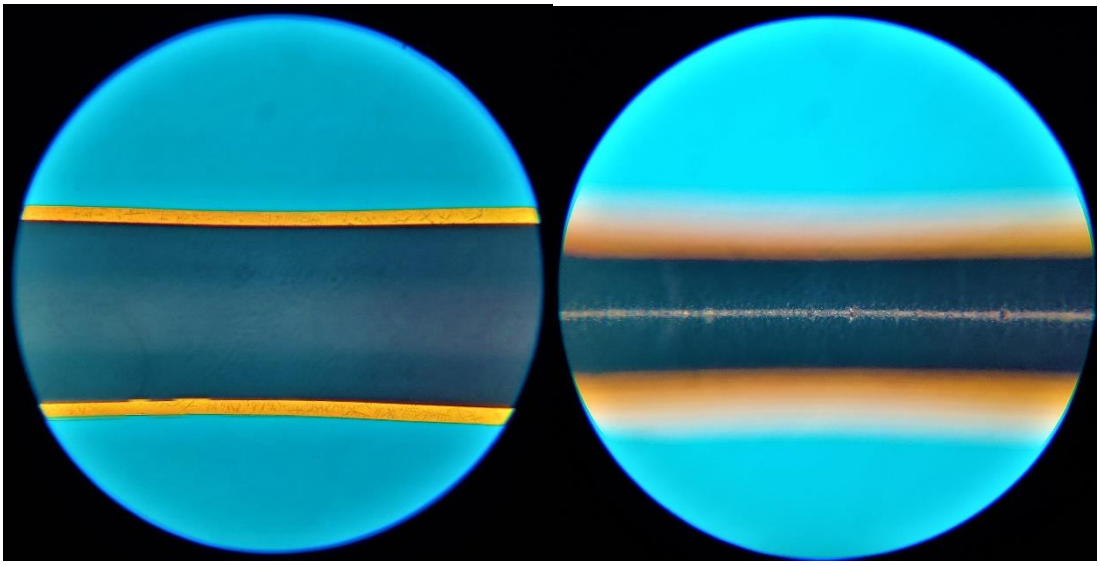


Figure 5.2.2. Optical microscopy images of the same area after the v-groove etch - left image is focused on wafer surface and shows under etch width (yellow) compared to the total 350-micron window width, right image is focused on bottom of the v-groove; it shows a straight narrow line that means complete v-groove etch, no truncated pyramid.

(B4) **Anisotropic etch step development.** Last month we tried for the first time in the world – adding DMSO to a standard TMAH etch recipe, and found it has advantage over all known chemistries - in the etch uniformity (as it suppresses hydrogen bubble sticking to the wafer surfaces). Now we have measured the etch rate of various TMAH/DMSO recipes. All etch experiments were on the same <100> heavy boron doped ~ about $1E^{19}$ cm^{-3} wafers. We have found that the control sample - TMAH:water 1:2 etch rate is about 0.5 micron/minute, equal to all data reported in literature for 80C, 9% TMAH etch. The etch rate has been calculated by weighing the wafers before and after the etch. Etching in TMAH:DMSO 1:2 resulted in 0.07 micron/minute etch rate – too low. Etching in TMAH:DMSO:water 1:1:1 resulted in 0.25 micron/minute etch rate and chosen as production recipe. Visually, both TMAH:DMSO recipes show no bubbling. Also, wafer surface appearance after the etch was very different for control and DMSO modified recipes: control one has matte appearance (means high roughness) while our recipes resulted in mirror like appearance – means low roughness. The wafers have been submitted to AFM measurement – to quantify the roughness improvement.

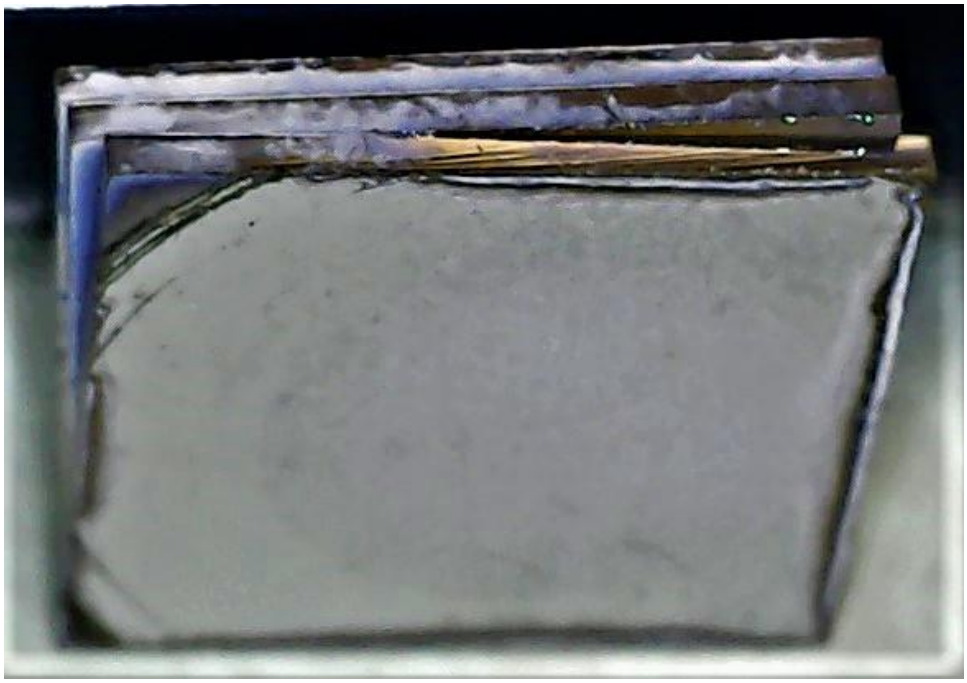
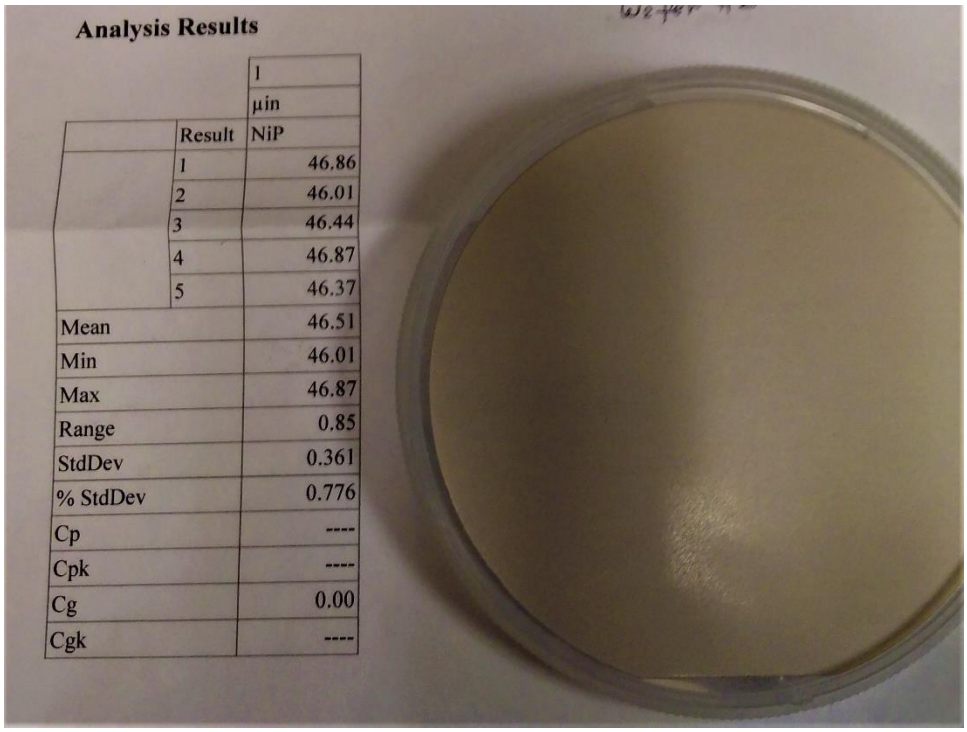


Figure 5.2.3. 3 individual 1x1 cm diode dies stacked by bonding with SLID technology.

(D2) **Stacking**. Our integration scheme calls for stacking on wafer level. This month we ran a short loop experiment – bonding individual diode dies into the stack. Upon developing the process recipe on die level, we will switch to bonding on wafer level. As we do not yet have electroless plating recipe developed, the metal stack Cr/Ni/Cu/Sn was deposited in-house by electron beam evaporation of each metal in a vacuum chamber. The metal coated dies were bonded using SLID – Solid-Liquid-InterDiffusion technique - reference [4]. The SLID has advantages compared to the traditional stacking by soldering – no metal squeezed-out and thus no parasitic electrical shorts along diode stack periphery, and much less voids in the metal layer. The process consists of placing dies to form a stack, applying pressure that pushes the dies together, placing the assembly into an oven with an inert atmosphere, and heating above tin melting point 232C. Upon the tin melting, tin dissolves copper and forms CuSn intermetallic compound. The melting point of the compound is above 500C, thus it immediately becomes a solid phase. The process continues until all available tin is consumed. SLID needs just a micron-thick metal layer - much thinner compared to soldering, therefore advantages in squeeze-out and voids.

An example of 3 stacked together dies is shown on Fig.5.2.3. The first runs were unsuccessful. Analysis shows that dies do not bond as there is a thin tin oxide layer on top of the tin. 2 methods are known to overcome this issue: either use flux or increase pressure. We have used the pressure approach: designed a fixture that keeps the die stack together, then during heating in the oven, thermal expansion causes enough pressure increase. Tin is ductile, and oxide film is thin, thus the oxide is broken allowing tin-to-tin contact, thus eventual success of the bonding. Currently the bonded samples

are under SEM analysis – to determine whether it contains voids, what is thickness of metal stack, whether all tin reacted, and what CuSn intermetallic phases are formed.



Analysis Results

		1
		µin
	Result	NiP
	1	46.86
	2	46.01
	3	46.44
	4	46.87
	5	46.37
Mean		46.51
Min		46.01
Max		46.87
Range		0.85
StdDev		0.361
% StdDev		0.776
Cp		----
Cpk		----
Cg		0.00
Cgk		----

Figure 5.2.4. Appearance of one of demo wafers

(D4) **Metallization step development**. Our DSRD integration scheme for metallization step calls for Ni-Cu-Sn metal stack. It starts from Ni electroless plating. We consider both options – either in-house or use vendors for the plating service. We have arranged demo plating at 3 different vendors. This month we got Ni plated demo wafers from one of the vendors – Component Surfaces. This is a service company specializing in contract electroless plating of customer's parts. We sent them 5 blanket heavy Boron doped wafers, they tried various plating recipes, several of them failed until they found a working recipe. Fig.5.2.4 shows one of wafers plated by Component Surfaces. The Nickel layer looks very uniform, its thickness variation is less than 1% across the wafer. The uniformity is much better compared to demo earlier done by Fibrotool vendor, and better than wafers we plated in-house using Palladium-then-Nickel recipe. Currently we are testing the quality of the Ohmic contact between Ni and Si, and Ni-Si adhesion. It also includes an annealing step – converting the Ni layer into silicide – to stabilize electrical and adhesion properties. If the tests pass, we will request a quote from Component Surfaces for the contract Ni plating.

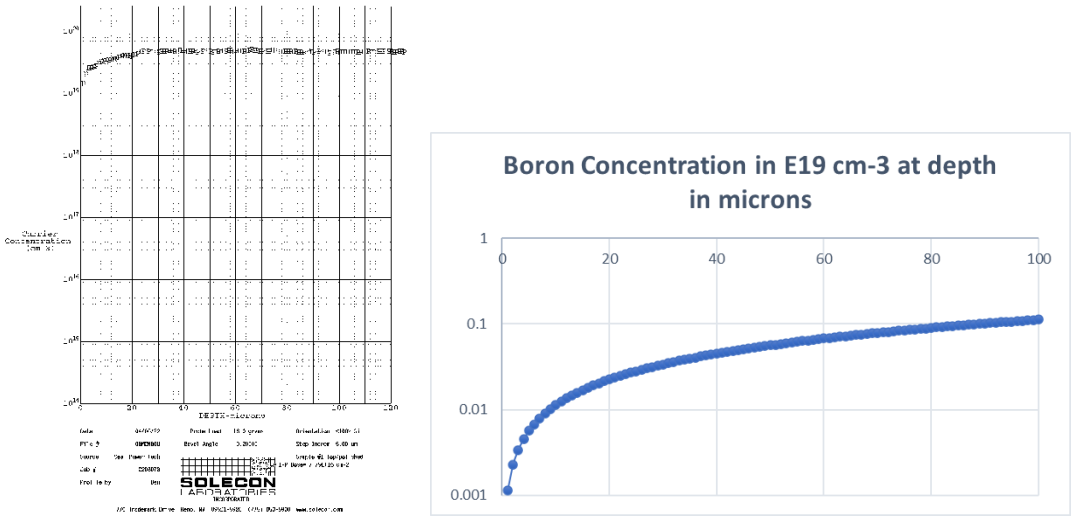


Figure 5.2.5. Measured – left and calculated – right - Boron profile upon 1300C/50hr anneal

(G1) Out-diffusion based DSRD process. The out-diffusion DSRD manufacturing is described in our patent application. After steep increase in epitaxy prices from all epi vendors, this process might be viable. We performed the trial run using an in-house furnace. Intel paper [5] on the boron out-diffusion describes anneal in pure hydrogen. Due to safety precautions, we have adjusted the recipe by 2.5% hydrogen in nitrogen (forming gas). As measurement shows, adding nitrogen significantly reduces out-diffusion. Analysis of literature confirmed that nitrogen reacts at 1300C with silicon, a thin nitride film forms - that prevents diffusion [6]. Now we will re-run the out-diffusion, adjusting to Argon/Hydrogen ambient.

5.2.5 *Summary of Significant Findings and Mission Impact*

(A) Several process adjustments have been implemented in processing of next Gen2 die lots. Die-to-die excessive variability is noticed. Process recipes and some equipment have been adjusted to achieve better uniformity and repeatability.

(B) Improving side termination of diodes. To prevent detrimental non-uniformity due to hydrogen bubbles sticking to wafer surface, a new process recipe has been developed. TMAH/DMSO mixture showed excellent uniformity. Using this mixture for anisotropic silicon etch never described in literature, we found this first.

(C) Replacement of unreliable metal contact deposition technique (by electron beam sputtering in vacuum chamber). Technical feasibility run on direct electroless plating of the Palladium/Nickel stack was successful. Process recipe developed for next run, plate uniform stack of Pd/Ni/Cu/Sn. State of the art electroless plating tool being donated by Hughes Research Lab.

(D) A process recipe for side passivation of diodes using a stain etch has been developed. The thickness uniformity resulting from the stain etch technique has been drastically improved. A new recipe that totally suppresses hydrogen bubbles sticking to the Si surface was found. Using that recipe, very uniform thickness (porous Si) films were successfully grown on blanket silicon wafers with both low and high doping levels.

5.2.6 *References*

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5.3 Characterization of SOS Diode Performance through DOE Augmentation

(Ethan Bozarth & Megan Hyde)

5.3.1 *Problem Statement, Approach, and Context*

Primary Problem: Drift step recovery diodes (DSRDs) are planar diodes that are capable of nanosecond, high-frequency (10–10^3 kHz) pulses [1] with applications as opening switches in inductive energy storage (IES) pulse generation circuits. There is not a clear understanding of the effects DSRD parameters have on overall IES pulser performance. The purpose of this project is to tie the DSRD parameters to its tailored performance requirements.

Solution Space: Leveraging both design of experiment (DOE) and machine learning (ML) capabilities, we will develop a methodology of characterizing and optimizing DSRDs in order to provide fabrication recommendations in the context of application targets.

***Sub-Problem 1*:** We do not yet understand how diode parameters are tied to diode performance.

Sub-Problem 2: There is no standardized method for correlating the diode key performance indicators (KPIs) to the IES pulser generator performance.

Sub-Problem 3: The number of possible inputs for the DOE is expected to be too large, so ML will need to be leveraged in order to guide decision-making processes.

State-of-the-Art (SOTA): Standard diode measurements include curve tracers for forward and reverse IV, impedance spectroscopy for forward and reverse CV, and function generators or, for example, the Avtech pulser for reverse recovery with high voltage and/or high current when necessary. These measurements are used to generate commonly available datasheets for COTS diodes. These standard diode measurements can then be correlated to pulser performance using traditional data analytics.

Deficiency in the SOTA: The standard diode measurements and datasheets do not include pulser performance necessary to evaluate DSRDs. The datasets generated with

doping profile assessment (for example spreading resistance profiling), standard diode measurements and pulser performance are too large and complex to leverage traditional data analytics and will benefit from machine learning techniques.

Solution Proposed: Develop a holistic evaluation network to characterize the KPIs of DSRDs. This network will include a DOE that will be a continuously evolving model as new KPIs are discovered. Augmenting the DOE will ensure that the model will remain relevant throughout this study as more discoveries are made. Machine learning will be used as the primary decision-making tool for augmenting the DOE. Once the network is established, it will be used to outline the optimal parameters for stacks of DSRDs within an IES pulse generator.

Relevance to OSPRES Grant Objective: Bridging the gap between the theoretical and physical performance of DSRDs enables closing the gap between a low fidelity TRL3 breadboard pulse generation system, and one which is at high fidelity TRL4 prototype level. At the TRL4 level, the DSRD-IES pulse generator system would be sufficient to replace the costly laser-based Si-PCSS HPM generator without compromise to scalability required to support the Naval afloat mission.

Risks, Payoffs, and Challenges:

Challenges: Traditional predictive analytics will be difficult to correlate with the augmented DOE due to the large volume of data. Machine learning is expected to assist with decision making processes for the DOE, but only if the proper KPIs have been established and good data have been used to train the machine learning model.

5.3.2 Tasks and Milestones / Timeline / Status

(A) Milestone – Establish preliminary DOE and standard operating procedure (SOP) for identifying KPIs of DSRDs [*estimated completion by MAR22*].

1. Task – Ascertain current KPIs used to optimize diodes simulated, manufactured, and utilized within the IES pulse generating circuit [completed AUG21];
2. Task – Construct preliminary DOE to acquire data on all KPIs based on Task 1 [*completed FEB22*];
3. Task – Leverage existing Python scripts to process legacy DSRD KPI data [*completed SEP21*];
4. Task – Develop new and review existing SOPs for experimental testing apparatuses used to evaluate individual KPIs and measure their performance [*completed OCT21*];
5. Task – Identify gaps/deficiencies in legacy KPI data, evaluate existing theoretical relationships to bridge gap and minimize DOE if possible [*completed OCT21*];
6. Task – Using SOPs developed in Task 4, acquire experimental data from legacy DSRDs, refine SOP(s), and assess repeatability and reproducibility [*SEP21–MAR22*];

(B) Milestone – Evaluate DSRD performance using the developed SOPs and facilitated by the preliminary DOE [*estimated completion JUL22*].

1. Task – Acquire data on newly manufactured 2nd generation epitaxial DSRDs from Section 5.2 using refined SOPs from Milestone A [*completed JAN22*];
2. Task – Evaluate the precision and power of the DOE [*MAR22–JUL22*];
3. Task – Develop a DSRD selection guide for the pulser circuit based on the static DC test measurements *[MAR22—MAY22];*
4. Task – Correlate the static DC test measurements to the performances of the IES pulser circuits and to fabrication procedures [*MAR22—JUN22];*
5. Task – Begin training machine learning model with DSRD data to determine correlations between static DC and pulser testing results [*MAY22—JUL22*];
6. Task – Acquire data on newly manufactured 3rd generation epitaxial DSRDs from Section 5.2 using refined SOPs from Milestone A [*JUL22-SEP22*];

(C) Milestone –DSRD diode network evaluation [*on hold until Milestone B is completed*].

1. Task – Refine Python script to incorporate new correlations based on findings from Milestones A&B [*Est. Summer22*];
2. Task – Amend ML training model with data acquired on new DSRDs (as characterized by Sections 5.1–5.2) to investigate statistical correlation of diode performance [*Est. Summer22*];
3. Task – Work with TCAD simulation team to address discrepancies between the DSRD performance obtained experimentally, and that achieved within simulations [*Est. Summer22*];
4. Task – Collaborate with DSRD manufacturing team to address discrepancies between the DSRD characteristics evaluated experimentally, and that desired by manufacturing process [*Est. Summer22*];
5. Task – Investigate relationships between statistical significance of individual diode KPIs to the peak performance of the IES pulser with the pulse generator team. [*Est. Summer22*];
6. Task – Incorporate findings from Tasks 1–5 into ML model, pinpoint KPI correlations of interest, and provide recommendations to IES sub-teams accordingly [*Est. Summer22*];

(D) Milestone – DSRD diode network evaluation [*on hold until Milestone C is completed*].

1. Task – Augment DOE network to streamline diode evaluation and identify checkpoints/gaps within simulation, manufacturing, and circuit development process to ensure optimal diodes are selected and utilized to produce robust high-fidelity IES pulse generator prototypes [*Est. Fall22*].

5.3.3 *Progress Made Since Last Report*

(A.6) The measurement results of the first six rounds (refer to Table 5.3.1) were processed for all three static DC tests, forward and reverse current-voltage and capacitance-voltage, that were tested by all three operators. The first static test

evaluated was the capacitance voltage test. Each diode was tested three different times by three different operators (e.g., 9 tests per diode).

	Round 1	Round 2	Round 3
Deep Diffusion 7 Stack	D1	D319	D333
Deep Diffusion Untested	630	657	801
Epitaxially Grown 1500	1562	1563	1564
Epitaxially Grown 1600	1601	1602	1603
Gen 2	1-1	1-2	1-3
Gen 2.2	1	2	3

	Round 4	Round 5	Round 6
Deep Diffusion 7 Stack	D366	D367	D380
Deep Diffusion Untested	~~802~~	803	804
Epitaxially Grown 1500	1565	1566	1567
Epitaxially Grown 1600	1604	1605	1606
Gen 2	1-4	2-1	2-2
Gen 2.2	4	5	6

Table 5.3.1. This table is representative of 16 total rounds for the experimental design testing. Each round contains one of each type of diode (i.e., deep diffusion 7 stack, epitaxially grown diodes, gen 2 diodes). Each number corresponds to the sample number of each DSRD. The diode crossed out in red was not a part of this study.

(B.3) To build a diode selection guide to direct the pulser operator in diode selection, we will need to correlate the static DC tests to the pulser performance (refer to Table 5.3.2). Two diodes from each diode group were selected as candidates for the pulser circuit tests.

Diode Group Type	Diode Name	Zero Junction Bias Capacitance (nF)
Deep Diffusion 7 Stack	D1	0.54
	D366	0.42
Untested Deep Diffusion 7 Stack	D657	0.68
	D804	0.66
EG1500	EG1562	0.45
	EG1565	0.67
EG1600	EG1602	0.91
	EG1603	0.64
Gen2	1-2	0.22
	2-1	0.08
Gen2.2	1	0.02
	4	0.21

Table 5.3.2. The diodes in the table have been selected as candidates for pulser test performances to begin correlating circuit testing with capacitance-voltage measurements.

5.3.4 *Technical Results*

(A.6) The conclusions drawn from the previous repeatability study performed on the Gen2 diodes were that there were large deviations in the measurements that could be caused by several “nuisance factors”. Possible nuisance factors that have been

identified are operator, equipment/sample holders, and charge build-up in diodes from previous testing. A randomized complete block design experiment was developed to reduce, or eliminate, the effects of these nuisance factors.

The average measured zero junction bias capacitance is plotted in Figure 5.3.1 with their respective standard deviations. A handful of diodes stand-out due to their large deviations, as can be easily seen by the error bars plotted for each point. Three of the epitaxially grown diodes (EG1562, EG1563, and EG1601) have unexpectedly large deviations, which may be the result of being the preferred pulser circuit test diodes. The group of Untested Diodes was found to have the smallest deviations as well as having coefficient of variance of less than 1% across all tests. The coefficient of variance is a ratio of standard deviation to the mean, often expressed as a percentage, and is a convenient way to calculate the relative impact of the deviation on a measurement. Table 5.3.3 contains the information that was plotted in Figure 5.3.1 along with the coefficient of variance of each respective diode.

The capacitance-voltage measurements from the previous repeatability study were compared to the measurements of this study. In Figure 5.3.2, the averaged test results of each study can be compared against each other, with the plotted values displayed in Table 5.3.4. As can be seen from Table 5.3.4, the coefficient of variance increased from the previous repeatability study. This measurement difference is most likely due to the change in the conditions of the diode tests. The previous study involved one analyst measuring taking each diode test after, presumably, different number of previous tests. Once the other two current-voltage tests have been evaluated, a more complete comparison can be made about the Gen2 diodes results.

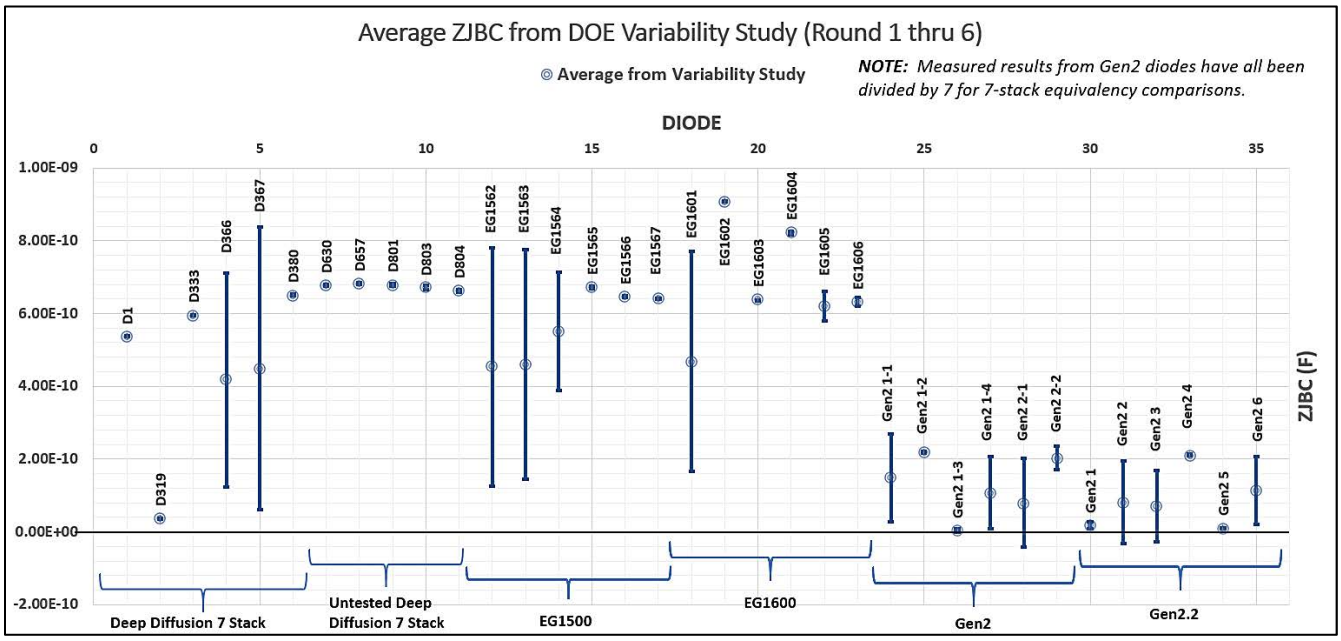

Figure 5.3.1 Each diode was measured once by three different analysts as part of the DOE variability study. Each measurement was averaged across all three analysts. NOTE:

Correction from previous month includes properly normalized Gen2 measurements for 7-stack die equivalency.

Diode Name	Average (nF)	Std. Dev (nF)	Coeff. Of Variance
D1	0.54	0.00	0.18%
D319	0.04	0.00	2.94%
D333	0.60	0.00	0.07%
D366	0.42	0.29	70.28%
D367	0.45	0.39	86.21%
D380	0.65	0.00	0.40%
D630	0.68	0.00	0.38%
D657	0.68	0.00	0.26%
D801	0.68	0.00	0.59%
D803	0.67	0.01	0.90%
D804	0.66	0.00	0.49%
EG1562	0.45	0.33	72.08%
EG1563	0.46	0.32	68.79%
EG1564	0.55	0.16	29.63%
EG1565	0.67	0.00	0.55%
EG1566	0.65	0.00	0.23%
EG1567	0.64	0.00	0.31%

Diode Name	Average (nF)	Std. Dev (nF)	Coeff. Of Variance
EG1601	0.47	0.30	64.66%
EG1602	0.91	0.00	0.18%
EG1603	0.64	0.00	0.02%
EG1604	0.82	0.00	0.52%
EG1605	0.62	0.04	6.53%
EG1606	0.63	0.01	2.00%
Gen2 1-1	0.15	0.12	80.95%
Gen2 1-2	0.22	0.00	1.21%
Gen2 1-3	0.00	0.01	161.16%
Gen2 1-4	0.11	0.10	92.88%
Gen2 2-1	0.08	0.12	153.99%
Gen2 2-2	0.20	0.03	16.15%
Gen2 1	0.02	0.01	53.20%
Gen2 2	0.08	0.11	141.07%
Gen2 3	0.07	0.10	138.01%
Gen2 4	0.21	0.00	1.35%
Gen2 5	0.01	0.00	5.04%
Gen2 6	0.11	0.09	82.83%

Table 5.3.3 Each diode in the table above corresponds to the plotted average measurement in Figure 5.3.1. Standard deviations in the pF range are listed in the table as 0.00. The coefficient of variance is the ratio of standard deviation to the mean, expressed as a percentage ($c_v = \frac{\sigma}{\mu} \times 100\%$).

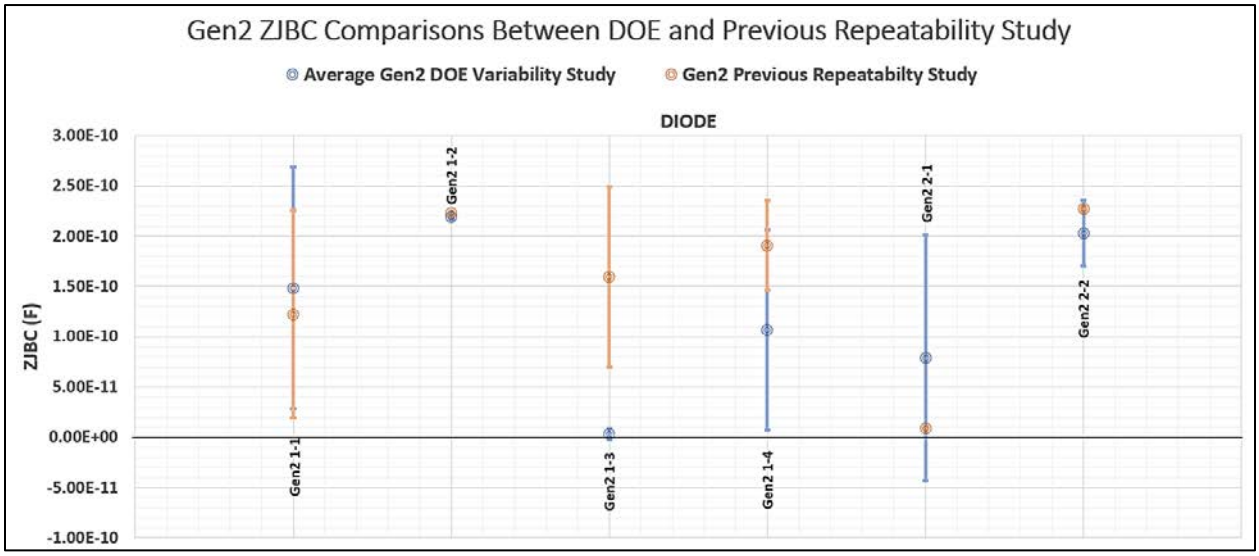

Figure 5.3.2 Each diode can be compared against the results of the previous repeatability study. One possible theory on the differences in results may be due to charge build-up in the previous test, or the introduction of three operators instead of just one. Each diode's result was normalized for 7-stack equivalency comparisons (to the other diode groups) by dividing by 7.

Gen2 Data from Previous Repeatability Study				Gen2 Data from DOE Variability Study			
Diode Name	Average (nF)	Std Dev (nF)	Coeff of Variance	Diode Name	Average (nF)	Std Dev (nF)	Coeff of Variance
Gen2 1-1	0.12	0.10	84.09%	Gen2 1-1	0.15	0.12	80.95%
Gen2 1-2	0.22	0.00	0.00%	Gen2 1-2	0.22	0.00	1.21%
Gen2 1-3	0.16	0.09	56.08%	Gen2 1-3	0.00	0.01	161.16%
Gen2 1-4	0.19	0.04	23.16%	Gen2 1-4	0.11	0.10	92.88%
Gen2 2-1	0.01	0.00	0.42%	Gen2 2-1	0.08	0.12	153.99%
Gen2 2-2	0.23	0.00	0.72%	Gen2 2-2	0.20	0.03	16.15%

Table 5.3.3 Each diode in the table above corresponds to the plotted average measurement in Figure 5.3.4. Standard deviations in the pF range are listed in the table as 0.00. The coefficient of variance is the ratio of standard deviation to the mean, expressed as a percentage ($c_v = \frac{\sigma}{\mu} \times 100\%$).

5.3.5 *Summary of Significant Findings and Mission Impact*

(A.1) The KPIs established thus far are: current at -200 V, voltage at 10 mA (forward bias), zero junction bias capacitance, minority carrier lifetimes, and series resistance. Additional KPIs are expected for IES pulser circuits.

(A.2) A preliminary DOE has been developed. The first 6 out of 16 rounds are currently being processed per (B.2).

(A.3) Python scripts have been modified for calculating and exporting measurement results and plots into Excel file.

(A.4) SOPs for forward and reverse IV and CV have all been updated with a page for tracking changes made to the procedures.

(A.5) One of the identified deficiencies of the DC static tests involves the picoammeter. We are unable to measure breakdown voltages of the diodes due to the limited range. A Tektronix curve tracer is a possible solution measuring larger currents and voltages.

(A.6) Inconsistencies in the experimental results require a root cause analysis. A preliminary repeatability and reproducibility test was performed on all Gen 2 diodes. Each diode was tested three times on each test, but the results revealed large variations. A RCBD experiment will aid in eliminating some of the possible sources of variation.

(B.1) Measurements have been collected on all Gen2 diodes for forward and reverse current-voltage, capacitance-voltage, and reverse recovery time tests.

(B.2) Twelve diodes have been selected as test diodes based on the measured results of the zero junction bias capacitance results so that we can begin correlating pulser performances to DC diode tests.

5.3.6 *References*

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5.4 DSRD-Based Pulsed Power Source Systematic Topological Optimization

(Islam Sarwar & Gyanendra Bhattarai)

5.4.1 *Problem Statement, Approach, and Context*

***Primary Problem*:** Inductive energy storage (IES) and release pulse generators that use drift-step recovery diodes (DSRDs) can be used as the fundamental units of all-solid-state high-power microwave (HPM) systems. The output from DSRD-based pulsers is then fed into sub-nanosecond pulse sharpeners to achieve ultra-short high-voltage pulses. While DSRD-based pulsers can theoretically achieve the targeted 1's of GW in 1's of ns, their circuits are not topologically optimized to achieve high voltage gain (peak pulse voltage/prime source voltage), making them require large and heavy high-voltage (multiple kV) prime power supplies to achieve the required 100's of kV pulses. They also necessitate liquid-based cooling systems to dissipate the excess heat they generate during operation, further adding weight and rendering them impractical for Navy afloat missions.

***Solution Space*:** Systematically develop optimum circuit topology to maximize the voltage gain, and thus the peak voltage, peak power, and volumetric power density. Minimize the heat loss to be able to air cool by increasing energy efficiency through optimization of circuit elements without sacrificing the desired nanosecond risetime of the pulses generated. Air-cooled IES pulse generators using optimum DSRD stacking can remove the need for photo-triggered switches and their laser sub-systems. They are ideal for triggering sub-nanosecond rise-time sharpeners (SAS, D-NLTL, etc.), reducing overall cost, volume, and weight.

***Sub-Problem*:** DSRDs are not domestically available COTs components, but rather manufactured in small-batch quantities, with statistically significant variations in their performance parameters. In addition, our current SPICE models of these diodes may not be accurate due to unknown device parameters such as carrier distribution, carrier lifetime and the limiting current that we can pump without affecting the diode recovery property (see section 5.1 and 5.3) during high-voltage transients. These issues may lead to an inaccurate simulation model of the pulser and discrepancies between simulated and experimental results.

***State-of-the-Art (SOTA)*:** Air-cooled DSRD-based pulsers (equivalent in size to the pulse generators developed for this effort, i.e., ~0.01-m^3, ~2-kg) can achieve <20 kV, 1–2 ns

risetime, and <4 ns FWHM across a 50 Ω load with a PRF of <15 kHz in burst mode. Available literature on IES pulse generators only describe a few circuit configurations, and there is a lack of comprehensive investigation of circuit topologies and optimization to achieve maximum gain and efficiency and reduce thermal load. Additionally, these pulsers are expensive and are not available within the United States.

***Solution Proposed*:** Develop different DSRD circuit topologies implementing series and parallel combinations of DSRDs (to increase reverse breakdown voltage and diode current, respectively) to minimize circuit components, such as inductors, capacitors, and switches. Systematically identify the best circuit topology and optimize the circuit components through physics-based DSRD pulser circuit theory and SPICE simulation to maximize voltage gain and efficiency while minimizing the prime source voltage and thermal load.

Risks, Payoffs, and Challenges:

***Risks*:** All-solid-state DSRD-based IES pulsers require many other electronic components. Most importantly, the current pumping capability of available MOSFETs/electronic switches is limited, which may make maximizing the output voltage impossible even though the DSRDs are capable of higher current and output voltages.

***Payoffs*:** Being able to simulate and fabricate DSRD-based pulsers using physics-based pulser theory, partnered with US-based DSRD manufacturers, will enable a comprehensive domestic ability to optimize, produce, and evaluate these nanosecond pulsers.

***Challenges*:** Domestically manufactured (U.S.-based) DSRDs, which possess sub-optimal doping profiles, may lead to sub-optimal pulse generators. Accurate spice modeling of the diodes could be affected by expected wide variability in the diode characteristics or unavailability of advanced device characterization techniques. Determining the superlative ratio of design/development (through numerical analysis) to the effort put towards experimental testing/evaluation of the DSRD pulser is challenging due to the novelty of the approach. Extending the theory of single (1×1) pulse generator to cascaded (M×N) generator to increase the output will be very complex and may require long time and powerful computing power.

5.4.2 Tasks and Milestones / Timeline / Status

(A) Milestone – Develop theory of DSRD pulse generator to facilitate optimization of 1×1 pulse generator [***Completed JAN22***]

(B) Milestone – Extend the theory developed in Milestone A to facilitate optimization of M×N pulse generator [**JAN–MAY22** / ***Ongoing***].

(C) Milestone – Construct/demonstrate a DSRD-based 1x1 pulse generator prototype based on theory developed in milestone (A) and obtain performance data for multiple combinations of diode stacks [**JAN–MAY22 / *Ongoing***].

(D) Milestone – Construct/demonstrate a DSRD-based 2×2 IES pulse generator prototype capable of producing ≥4 kV peak voltage, ≤1 ns risetime, ≤5 ns FWHM,

≥320 kW peak-power, ≥1 kHz PRF, ≥100 shots-per-burst, ≥5 number of bursts [***Completed JUL21***].

(E) Milestone – Construct/demonstrate a DSRD-based 4×2 IES pulse generator prototype capable of producing ≥12 kV peak voltage, ≤1 ns risetime, ≤5 ns FWHM, ≥3 MW peak-power, ≥100 kHz PRF, ≥1,000 shots-per-burst, ≥500 number of bursts [*On hold*].

(F) Milestone – Develop waveform inverter which, when combined with the pulser from Milestone C, enables a balanced differential waveform output with >90% inverted signal fidelity. [***Completed DEC21***].

(G) Milestone – Construct/demonstrate a M×N pulse generator prototype capable of producing ≥20 kV peak voltage, ≤1 ns risetime, ≤2 ns FWHM, ≥8 MW peak-power, ≥100 kHz PRF, and $\geq 2\sigma_{Vpeak}$, which operates in continuous-burst mode as a viable candidate for OSPRES Contract source alternative [*on hold until Milestones B, D, & E are completed*].

5.4.3 *Progress Made Since Last Report*

(A) Single-bar DSRD pulse generators optimized for three 7-stack diodes and four 7-stack diodes were simulated based on the theory presented in the DEC2021 MSR.

(B) Two new 1×1 DSRD-based pulse generators optimized for three 7-stack diodes and four 7-stack diodes have been populated and are being tested for different combinations of diode stacks, this time including the voltage drop across the diodes during forward pumping in calculating diode current. Although we obtained higher voltage pulses during FEB22 reporting period, only a maximum peak output voltage of 4.5 kV is obtained with four 7-stack diodes for a trigger length of 700 ns using a prime supply voltage of 120–200 V. Increasing the prime source voltage upto 200 V did not significantly increase the output.

5.4.4 *Technical Results*

5.4.4.1 Experimental Results from Single-Bar 1×1 DSRD Pulser

(B) In the previous report (FEB 2022 MSR), we had presented the second gen DSRD pulser optimized for 28-stack diodes. The pulser was expected to produce 14 kV assuming a diode breakdown voltage of 500V per diode. However, the maximum output obtained from the pulser was 6.7 kV—nearly half of the expected output—for a trigger length of 700 ns. Although an inaccurate SPICE model for the diode could be responsible for the lower output, a limited forward pumping current through the diode due to MOSFET current limitation could be a major factor. Although the limiting MOSFET current is 400A, nearly 75% of the current flows through the circuit L1-C1 and only ∼100A of current was possible to pump through the diode. Another issue with the MOSFETs was their frequent burning, the reason of which was not identified clearly, but could be due to their operation very close to their maximum current limit.

Towards achieving the goal of producing a 10 kV pulse, we sought to increase the current pumping capability of the circuit. Thus, a new pulser was designed to include two

MOSFETs in parallel so that ~200 A of current could be forward pumped through the diodes. This version of the pulser was designed to use 21-stack diodes which would theoretically produce 13.5 kV pulse assuming a reverse diode breakdown voltage of ~650 V per diode, as explained in FEB 2022 MSR Report.

Although the circuit was expected to produce ≥10 kV and was expected to be operational for prime voltage up to 200 V due to increased current limit of two parallel MOSFETs, it only produced ~4.5 kV from the circuit, as shown in Figure 5.4.1. Interestingly, the output did not change significantly by changing the prime voltage and the trigger length, which was not expected based on the theory, and we have not found what caused this decreased output yet.

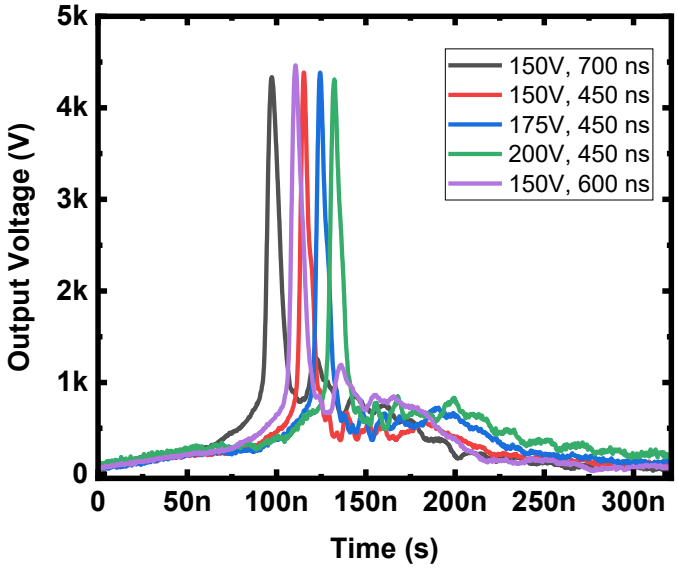

Figure 5.4.1. Output pulse from DSRD pulser optimized for 21-stack diodes for different prime voltage and trigger lengths.

One possible factor that could change the output significantly is whether the forward pumping current through the diode was as expected from the theory. Although we do not have a capability to measure the diode current (~200 A) directly without affecting the circuit performance at present, it is possible to measure the MOSFET voltage from which the total current through it could be estimated. Figure 5.4.2 shows the MOSFET voltage measured during the forward pumping for the prime voltage of 120 V.

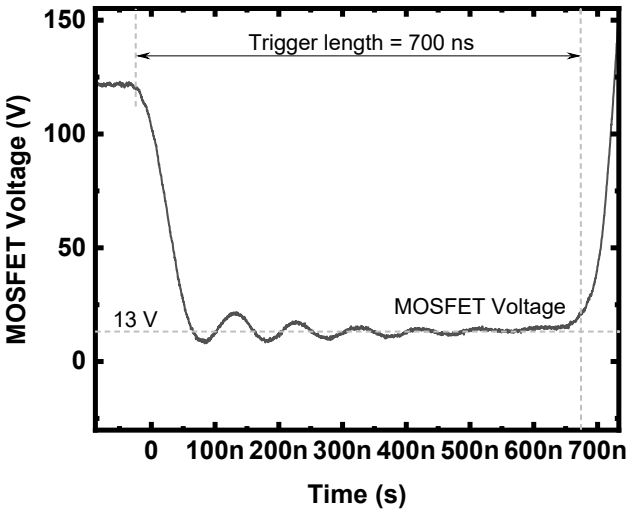

Figure 5.4.2. Voltage across MOSFET during the trigger length.

We can see from Figure 5.4.2 that the MOSFET voltage remained at ~13 V during the MOSFET ON time suggesting an estimated current of ~450 A per MOSFET, which is slightly higher than the MOSFET rating. Thus, it can be expected that the diode current was close to the theoretically expected value and the circuit was operating as expected.

Another factor that could reduce the output voltage is the MOSFET voltage right after the MOSFET is turned off. Figure 5.4.3 shows the MOSFET voltage and output voltage while using the prime voltage of 150 V and trigger length of 700 ns. As we can see that the MOSFET voltage reached ~800V while the MOSFET was turned off which can effectively reverse bias the diode to extract the injected charge. Thus, other than the output voltage, the circuit was performing as expected. However, we observed high voltage oscillations exceeding 1.2 kV across the MOSFET after the output pulse is generated. We think the frequent burning of the MOSFETs is due to this high voltage oscillations across the MOSFET and should be reduced for safe circuit operation.

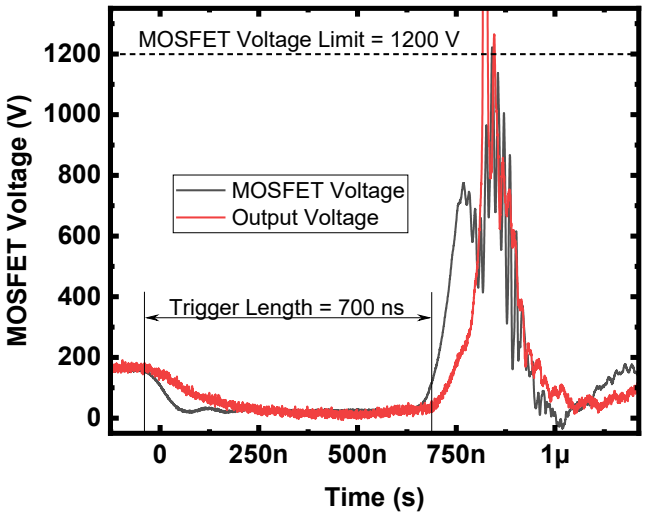

Figure 5.4.3. MOSFET voltage and Output signal for trigger length of 700 ns and prime voltage of 150 V.

Apart from the oscillations in the output, we also observed oscillations in the gate driver output. While observing the gate signal when both prime voltage sources were disconnected, we observed a much slower rise-time and fall-time compared to the trigger signal, as shown in figure 5.4.4. When the prime voltage sources were connected large oscillations were observed after the turn-off of the gate driver (after output pulse is generated) which could initiate a false trigger and damage the driver IC.

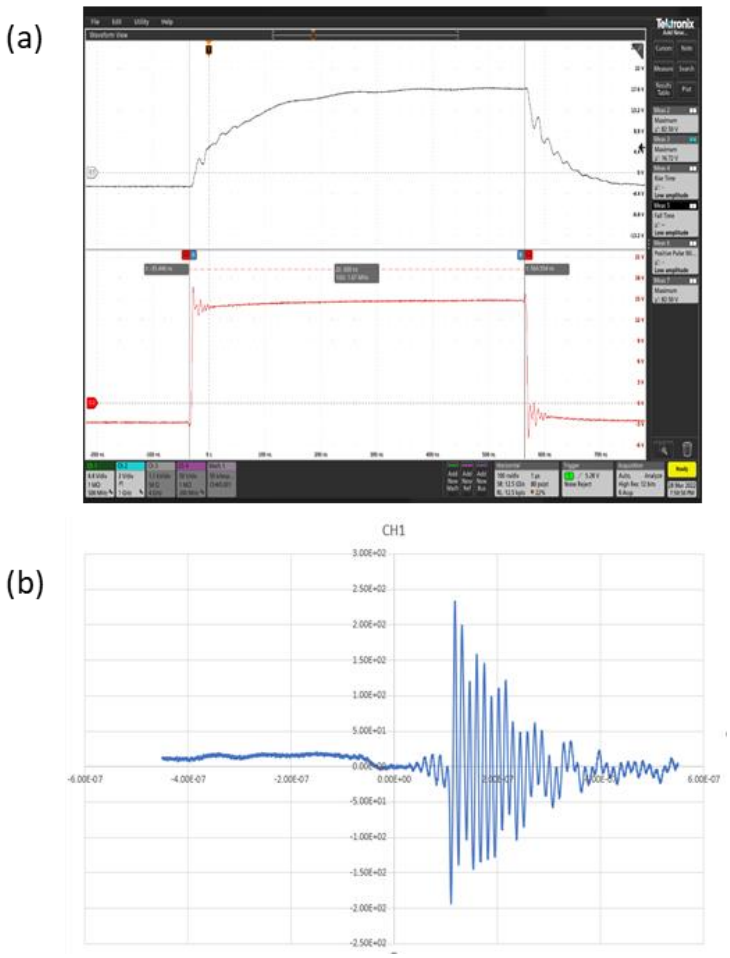

Figure 5.4.4. (a) Gate driver output with Prime sources disconnected and (b) with prime sources connected showing the voltage oscillations after the MOSFET is turned off.

To solve the issues discussed above, we recalculated the gate resistor value to sink and source more current during switching transients. A new gate driver module from CREE is retrofitted on the board to evaluate the performance. The current version of the prototype board is populated with 1.25 Ohms gate resistor, which initially was fitted with 2 Ohms, and can drive a parallel set of MOSFETs satisfactorily. The pulser board is now re-populated with newly optimized parameters for 28-stack diodes so that the MOSFET voltage pulse remains below 1000 V before and after the output pulse is generated. However, we have not yet tested the pulser.

5.4.5 *Summary of Significant Findings and Mission Impact*

(A) A systematic optimization of a 1×1 pulse generator based on the theory covered in the DEC2021 MSR reporting period was presented. Based on the simulation, we optimized the circuit for a maximum output voltage of 18 kV using four 7-stack diodes.

(B) Using the 28-stack pulser, maximum peak outputs of 6.7 and 7.5 kV are obtained for a trigger length of 700 ns using a prime source voltage of 120 and 170 V. This suggests that a high voltage gain can be achieved by implementing more powerful MOSFETs and/or MOSFET paralleling. Further, the reverse breakdown voltage of ~650 V per diode in the EG1600 series is estimated based on the DSRD pulser output using a single 7-stack diode. Measurement of circuit voltages at different nodes confirms the circuit performance matching the SPICE simulation. Obtained lower output voltages indicates requirement of more accurate DSRD SPICE Model which takes account of carrier distribution and recombination during high voltage transients.

Table 5.4.2. Comparison of DSRD-based IES Pulse Generator Performance.

KPM	**Units**	**MIDE - V1** Previous	**MIDE - V2** Previous	**MIDE – V3** Current	**Kesar *et al.*** SOTA	**MI-PPM0731** COTS
V_{supply}	V	225	180	120	300	160
T_{ON}	ns	100	340	700	?	200
V_{peak}	kV	5.59	**7.35**	**6.7**	5	6.3
Gain	V/V	24.8	**40.8**	**55.8**	16.7	39.4
$\tau_{rise,20\text{-}90\%}$	ns	1.2	1.1	3.1	1.96	0.12
dV/dτ	kV/ns	4.66	6.44	2.16	2.55	**52.50**
FWHM	ns	2	5.48	6.90	2.27	0.35
PW	ns	5	7	7	3.5	2.5
Z_{LOAD}	Ω	50	50	50	50	50
P_{peak}	MW	0.625	**1.080**	**0.905**	0.500	0.794
E_{pp}	mJ	0.125	0.154		0.143	0.318
PRF_{max}	kHz	100	100		100	15
Burst	shots	100	100	*N/A*	*N/A*	100
	%	100	100	*N/A*	*N/A*	100
SD_{Vpeak}	σ	> 2	**> 2**	*N/A*	*N/A*	*N/A*
	%	96.5	**97.8**	*N/A*	*N/A*	*N/A*

(C) Successful construction and operation of a 2×2 DSRD-based IES pulse generator prototype has been completed, which meets or exceeds the required key performance metrics. Shown in Table 5.4.2 are the previous and current pulse generator performance specifications in comparison to a similar 2×2 pulser

developed by Kesar et al. [1] using DSRDs, and to that of a commercial off-the-shelf (COTS) DSRD pulser of similar space and weight developed by Megaimpulse (i.e., PPM-0731), which also uses DSRDs with silicon avalanche shapers (SAS) [2]. Although the Megaimpulse pulser utilizes a SAS with a <500 ps risetime (a threshold we do not intend to go below due to Commerce Controlled List limitations), it is interesting to compare the results of linear voltage gain and peak power of this system, to that of one that utilizes a SAS. The current permutation of the 2×2 DSRD-IES pulser developed by MIDE under the ONR OSPRES Grant is able to achieve a higher peak voltage and shorter risetime than DSRD-based pulsers reported in the literature of comparable space and weight as well as those commercially available. The ability to generate a linear voltage gain of 40.8 to produce over a Megawatt of peak power into a 50 Ω load while achieving a peak voltage output standard deviation of 2σ when operating at a PRF of at least 100 kHz, brings this technology to the forefront of viable options to potentially support the Naval afloat mission.

(D) Discrepancies exist in the obtained pulser and device characterization data for different series combinations and different samples of 7-stack DSRDs, which may be attributed to the inconsistencies in their manufacturing process. Future work in the coming months include testing single 7-stack and two 7-stack diodes in pulser configurations with better MOSFETS or MOSFET paralleling to identify better diodes and increase the output voltage to >9 kV from the 1x1 pulser configuration. Future works also include the design and testing of 2×2 or higher configuration DSRD-based pulsers using more combinations of series-connected as well as parallel-connected DSRD stacks.

5.4.6 *References*

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[2] https://cms.wolfspeed.com/app/uploads/2020/12/C2M0045170P.pdf

5.5 All-Solid-State Sub-ns MW Pulse Generators with Semiconductor Sharpeners

(Gyanendra Bhattarai)

This sub-project is currently on hold as focus is directed toward Section 5.4. Please review the January 2022 MSR for the most recent project overview and status.

6 Thermal Management

6.1 Ultra-Compact Integrated Cooling System Development

(Samual, Roy Allen, and Sarvenaz Sobhansarbandi)

6.1.1 *Problem Statement, Approach, and Context*

Primary Problem: A thermal management system (TMS) is required for cooling semiconductor-based pulse-power devices, with the goal of maintaining the semiconductor device temperature below 80 °C. The proposed system must increase cooling densities, while decreasing pumping power requirements, in-line with the SWaP-C[2] objective.

Solution Space: To achieve such high cooling densities, an ultra-compact TMS (UC-TMS) directly integrated onto the semiconductor is proposed. Such a design is capable of creating turbulent flow in order to enhance the heat transfer rate. The proposed UC-TMS is restricted to 1 cm^2 surface area, therefore, the required pumping power should be kept to a minimum. An array of micro-sized jet nozzles will provide a turbulent flow onto a microchannel section directly on the semiconductor device. The UC-TMS design will reach turbulency at a faster rate while requiring less energy consumption.

Sub-Problem: The turbulency formed from the array of nozzles creates an extreme pressure loss from the large amount of jet nozzles (over 200) and a flow diameter of 100 microns. The pressure must be sustained to enable proper cooling and circulation processes.

State-of-the-Art (SOTA): Integrated chip cooling is being widely used to dramatically increase the operational power of high voltage silicon-based power devices. However, the current SOTA devices include individual parts which attach to a high-power device, causing less interaction between the semiconductor and coolant, degrading the heat removal rate.

Objective: The proposed UC-TMS design is based on refining in-chip jet-impingement geometry through leveraging theory and a parametric evaluation of nozzle geometry and flow channel arrangements. A Si-base unit will be prototyped to maneuver a higher capacity of heat removal. Moreover, to sustain the pressure, the application of different working fluids is suggested. Several types of coolant will be simulated to determine effects from fluid density and viscosity.

Anticipated Outcome(s): To create a UC-TMS with the ability to rapidly remove 1 kW/cm^2 of heat. A design capable of such high heat removal can be implemented on many applications such as high-power batteries.

Challenges: The manufacturing techniques of the semiconductor devices have not yet been adopted for integrated chip cooling systems. The proposed compact design is restricted due to low tolerance of the manufacturing process, as this process must be capable of layering the silicon TMS onto the semiconductor.

Risks: With a system so compact, the pressure drop could be a large issue regarding the objective heat dissipation rate. An extreme pressure drop would potentially cause the coolant to flow backwards, causing less fluid-to-solid interaction.

6.1.2 *Tasks and Milestones / Timeline / Status*

(A) Design a Si base 1 cm^2 UC-TMS, applying manufacturing tolerances, to achieve a heat dissipation rate of 1 kW/cm^2. The design must be able to be produced by manufacturing techniques such as etching and lithographic layering processes. To confirm the device can be manufactured as proposed, each section of the model will be layered step by step. / MAR22–MAY22 / In Progress

(B) Using the optimal design, perform ANSYS simulations using either water or Si-C nanofluid. Other fluid types may be researched as pressure drop is a large factor / MAY22–JULY22 / Upcoming

(C) Improve design parameters and sizing to have a lower pressure drop while having a high heat dissipation capability. Prove simulations from previous literature to show capable design configurations with acceptable pressure drop and steady temperature. / AUG22– OCT22 / Upcoming

(D) With proper simulation results, manufacture a prototype to begin experimental testing and evaluation / NOV22–APR23 / Upcoming

6.1.3 *Progress Made Since Last Report*

Reviewing literature that pertains to Integrated Chip Cooling, a design and simulation report was found. Using this report to recreate the technology and simulate it to give a proof of concept to the future geometry's in ANSYS simulation. A model of this design has been created with SolidWorks and will be simulated within the next report.

6.1.4 *Summary of Significant Findings and Mission Impact*

From a literature review, a design was found to have a low pressure drop while being able to extract 1.7 kilowatts per square centimeter only using 0.57 watts of pumping power. This was achieved with a monolithically integrated manifold microchannel (mMMC) with 2, 4 and 10 inlet and outlet manifold channels and identical 20 × 125 μm microchannels, referred to as the 2×-, 4×- and 10×-manifold chips. The 10×-manifold chip was able to achieve an average change in temperature of 50 K at 100 Watts of power.

(A) After looking over past work the main issue being had was the significant pressure loss from the geometries. This problem seems to be solved with the geometries provided by the 10x manifold chip. The pressure readings from the literature and the ANSYS results need to be compared. This will give a better understanding of why there is not as high of pressure losses with the literature geometries compared to previous designs.

7 Pulse-Forming Networks

7.1 Diode-Based Nonlinear Transmission Lines

(Nicholas Gardner)

Attention on this sub-project is being entirely directed toward the preparation of manuscripts and an associated dissertation. A summary report will be provided in Summer 2022, and this will serve as a placeholder until this time. Please see the January 2022 MSR for the most recent summary and status.

7.2 Continuous Wave Diode-NLTL based Comb Generator

(Nicholas Gardner and John Bhamidipati)

7.2.1 *Problem Statement, Approach, and Context*

Primary Problem: When used as a pulse shaping network (PSN), diode-based nonlinear transmission lines (D-NLTLs) are promising solutions towards reducing the size, weight, and cost of RF and microwave sources on Navy afloat missions. However, in pulsed-mode, the impedance of D-NLTLs changes significantly, leading to signal/power reflection, standing wave generation, and return power losses at both the source–line and line–load interfaces, leading to difficulties in practical D-NLTL applications.

Solution Space: Use a D-NLTL to work as comb generator (capable of producing multiple harmonics of the input signal) by converting continuous wave (CW) signals from low frequency–very high frequency (LF–VHF) bands (0.03 MHz–30 MHz) to the ultra-high frequency (UHF) band (0.3–3 GHz) at ones-of-MW peak power. Such an application with reduced dependence on transient changes will decrease impedance mismatch effects at the source–line and line–load interfaces by continuously oscillating D-NLTL peak impedance between the same two values. Use of MW D-NLTLs in the comb generator will push output frequency up to ranges required for Navy afloat missions.

Sub-Problem: Design parameters for COTS high-frequency D-NLTL based comb generators capable of generating up to ~50 GHz output frequencies are limited to <1 Watt output powers, which is <0.1% of the power handling capability required for navy afloat missions. Using the metrics associated with low power comb generators alone to design D-NLTLs capable of generating ~1–2 GHz frequency with capability to handle MW-order peak powers could potentially introduce design errors resulting in frequency/power prediction–measurement discrepancies on the order of a few hundred MHz.

State-of-the-Art (SOTA): Commercial-off-the-shelf (COTS) GaAs varactor diode-based monolithic microwave integrated circuit (MMIC) D-NLTL comb generators are capable of operating at input and output frequencies up to 600 MHz and 30 GHz, respectively. However, these comb generators are not capable of handling powers higher than 27 dBm (0.51 W). In-house pulsed D-NLTL prototypes have been shown to generate center frequencies of 0.2–0.5 GHz at kV amplitudes (~0.5–0.7 MW peak power) in a light-weight small-footprint circuit. Further D-NLTL network efficiency is hindered by a signal-dependent impedance characteristic to the network leaving reported efficiencies of RF content generation at 10% or less of incident pulse energy.

Objective 1: Design and demonstrate a high voltage D-NLTL based comb generator capable of L-Band Frequency generation and 0.1–5 MW power generation.

Objective 2: Increase D-NLTL network efficiency above the reported 10% threshold through use of CW sources suppressing impedance mismatch effects presented by the signal-dependent impedance characteristic of D-NLTLs.

Anticipated Outcome(s): A successful demonstration of improvements to impedance matching at the source–line interface using a CW signal measured as a reduction in signal amplitude loss between the source and D-NLTL.

Challenges: Nonlinear signal-dependent behavior provided by a reverse bias diode produces difficulties in predicting generated waveform behavior. Further D-NLTL performance is limited in both frequency and power generation by the availability and variety of COTS Schottky and epoxy diodes.

Risks: The reverse bias hold off potential (V_R) of a chosen diode limits the power generation capabilities of the system. If an excitation is used that exceeds V_R, diodes risk being damaged. Further reflections produced at the source–line interface caused by a signal dependent impedance can damage a CW source sensitive to such reflections.

7.2.2 *Tasks and Milestones / Timeline / Status*

(A) Demonstrate an ability of a CW excitation signal to reduce the source–line impedance mismatch effect on signal amplitude present in D-NLTLs when compared to a pulsed mode operation, first through simulations and then by validating the results experimentally using low voltage (LV) and high voltage (HV) prototypes.

(A1) Show the potential to improve source–line impedance mismatch in simulation (Completed SEP21)

(A2) Experimentally demonstrate a low voltage (LV) prototype receiving a CW input (Completed SEP21)

(A3) Compare measured results with simulation behavior; comparison of results will be used to further refine D-NLTL simulation techniques (Ongoing)

(A4) Determine if there are improvements to system behavior if D-NLTL diodes are biased when receiving a CW input (Ongoing)

(A5) Demonstrate improvements to the source–line impedance mismatch in a LV prototype (Ongoing)

(A6) Demonstrate a HV prototype receiving a CW input (Completed NOV21)

(B) Demonstrate UHF – L-band (0.3–2 GHz frequency) generation with a CW D-NLTL.

(B1) Excitation of K100F and K50F D-NLTLs using a 700 MHz signal from the R&S amplifier (Completed NOV21)

(B2) Compare measurement with simulation to further refine simulation measurements (**Ongoing**)

(B3) Simulate topologies capable of utilizing a bipolar pulse for CW applications (**Ongoing**)

(C) Demonstrate UHF generation at single MW power levels with a CW D-NLTL.

7.2.3 *Progress Made Since Last Report*

(B2) Simulation and experimental studies have been performed on D-NLTLs at two different excitation frequencies: (i) 10–30 MHz at <10 V, and (ii) 700 MHz at ~80 V bias, with focus on source–line impedance matching at 'cell 0' to minimize reflected power. To match the impedance at cell 0 in epoxy diode-based D-NLTLs, a resistor equivalent to the average line impedance has been used. No significant reflections were observed for case (i), but a significant reflection was still seen at ~700 MHz excitation frequency.

7.2.4 *Technical Results*

(B2) Impedance matching at the source–line interface (cell 0) has been focused on for this reporting cycle. D-NLTL lines based on the K50F and K100F epoxy diodes have been simulated and tested with 5 $V_{p\text{-}p}$ at 10–30 MHz, and 80 $V_{p\text{-}p}$ at 700 MHz CW sinusoidal excitation. At the source–line interface, a linear resistor equivalent to the average impedance of the line has been used. At low frequency excitation (~25 MHz), shockwave generation with low-to-no reflection was observed with >0.7 GHz 3dB frequency. However, when tested at 700 MHz excitation with an R&S amplifier, >50% power reflection was noticed. Impedance matching at cell 0 needs to be studied individually for the high frequency excitation. Further simulation and experimental studies will be focused on matching the cell 0 impedance with that of cell 1, average impedance of cell 0 and cell 1 with that of cell 2, and so on in multiple iterations.

7.2.5 *Summary of Significant Findings and Mission Impact*

(A) In the month of September 2021, a LV prototype was given several continuous waveforms to observe initial behavior of a D-NLTL with a CW source. The LV D-NLTL demonstrated a capability to receive a CW based source. No effect on the source–line impedance mismatch was observed for the LV tests. During the month of November 2021, two high-voltage D-NLTLs based on epoxy diodes were tested using a sinusoidal waveform amplified by an R&S amplifier. Each D-NLTL demonstrated a capability to function with a CW source, however little to no effect was observed on the source–line impedance mismatch.

(B) Two high voltage D-NLTLs based on epoxy diodes of models K50F and K100F were tested using 25 MHz and 700 MHz sinusoidal sources. While shockwave formation was noticed at 25 MHz excitation with ~35% conversion efficiency, pulse sharpening has been observed at low voltage (7 $V_{p\text{-}p}$) 700 MHz excitation in the K50F line alongside the frequency doubling behavior (1.4 GHz output frequency) reported previously. However, the power reflection at ~70 $V_{p\text{-}p}$ remains >60% for both the lines at 70 $V_{p\text{-}p}$ excitation, resulting in <7% line efficiency. A technique to implement adaptive line–load impedance to minimize the power reflection needs to be developed.

7.3 Dynamically Tunable Multi-Frequency Solid-State Frozen Wave Generator

(John Bhamidipati)

7.3.1 Problem Statement, Approach, and Context

Primary Problem: Conventional RF generators such as vector inversion generators, relativistic magnetrons, etc. are limited by their frequency response (narrow bandwidth), form factor, and pulse conversion efficiency, limiting their application in Navy afloat missions.

Solution Space: Develop a single PCB-mount, all-solid-state multifrequency generator with chirp capability and dynamic (electronic/mechanical) tunability. A sub-class of microwave pulsers called frozen wave generators (FWGs) capable of DC-to-RF pulse conversion provide a potential solution in terms of form factor, frequency tunability and power conversion efficiency.

Sub-Problem: A frozen wave generator, an alternative pulse generator capable of generating frequencies in the range of tens-of-MHz to sub-THz proposed by Forcier [1] and Best [2] is limited by the center frequency, form factor, and the performance of the enabling switch.

State-of-the-Art (SOTA): A photoconductive-switch-enabled FWG with adjustable frequency range between hundreds-of-MHz–2 GHz and pulse widths between 360 ps and 15 ns.

Deficiency in the SOTA: Despite addressing the limitations of spark gaps used in the earlier FWG literature, the photoconductive-switch-based FWGs suffer from limitations of the laser systems whose size (>5 cu-ft), weight (>120 lbs.), cost (>$120,000), and cooling have not reached full maturity. Furthermore, they require multiple enabling switches, increasing the switching and synchronization complexity. A single MOSFET-enabled FWG implementation requires an inexpensive (<$500) electronic pulse trigger generator with < 1cu-ft volume.

Risks: The proposed work implements a SiC-MOSFET based prototyping. MOSFETs are limited by their ns-order rise times, which could potentially limit the frequency response of the FWG. On the other hand, when the number of transmission line segments is increased, the MOSFET may not be able to switch all the segments simultaneously, resulting in distorted pulse wavefront. Furthermore, implementing lumped-element-based transmission lines can reduce the conversion efficiency.

7.3.2 Tasks and Milestones / Timeline / Status

1. Simulate a chirp-capable distributed-element transmission-line-based (DETL) 16-stage frozen wave generator (FWG) with balanced and unbalanced load configurations. [JUN–JUL 2021 / complete]
2. Demonstrate a SiC-MOSFET-powered FWG prototype on a custom-built PCB with Cree/Wolfspeed MOSFET, and 50 Ω coaxial cables and/or microstrip transmission lines capable of generating chirped pulse widths. [JUL–AUG 2021 / complete].

3. Simulate a lumped-element transmission line (LETL) based FWG with up to 12 segments to replicate results from the DETL-FWG simulations. [AUG–SEP 2021 / complete]
4. Demonstrate a modular 4–8 stage SiC-MOSFET enabled FWG with lumped-element-based transmission lines with and without chirp capability. [SEP–OCT 2021 / complete]
5. Design and test a 12-segment, MOSFET-enabled FWG prototype with dynamic pulse width tunability using lumped-element-based transmission lines [NOV–DEC 2021 / complete].
6. Perform root cause analysis to determine the causes for (i) pulse overlap demonstrated by the Gen1 LETL-FWG prototype under unbalanced load configuration, and (ii) consistent reduction in the peak voltage output of the pulse train output. [JAN–FEB 2022 / in progress]
7. Demonstrate motorized and/or electronically tunable DETL-FWG prototype with dynamic tunability capable of generating multiple center frequencies. [MAR–APR 2022]

7.3.3 Progress Made Since Last Report

(F) A modified 12-segment FWG (Gen-2) with reduced footprint and updated MOSFET placement was tested upto 400 V under balanced and unbalanced load configurations to determine the root cause for the peak voltage drop seen in the Gen-1 prototype as reported in the previous cycle.

7.3.4 *Technical Results*

(F) A Gen-2 FWG prototype with modified switch (MOSFET) position, optimized ground plane, and reduced PCB footprint has been tested to determine the root cause for peak voltage drop. Despite the modified design, a consistent voltage drop and pulse overlap have been noticed under balanced (R_L=R_T) and unbalanced (R_L>>R_T) load configurations, respectively, when tested at 400 V bias. The inability of the MOSFET to simultaneously switch all TL segments was determined to be the reason for these phenomena. The MOSFET was rated for 10.5 ns rise-time, limiting its ability to perform ultrafast switching, subsequently limiting >100 MHz frequency generation.

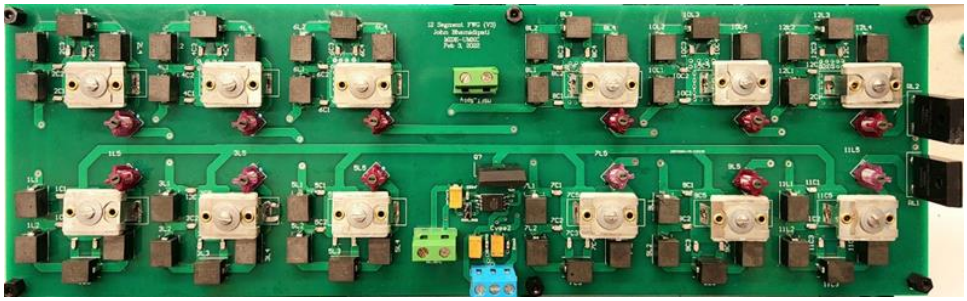


Figure 7.3.1. Gen-2 12-segment dynamically tunable FWG prototype

7.3.5 *Summary of Significant Findings and Mission Impact*

(A) A 16-stage, chirp-capable FWG with was modeled in LTSpice for concept illustration. The TL segments were selected to demonstrate 125–500 MHz output frequencies. Out of 16 transmission line segments in the simulation, 8 are used for generating the desired ON times, and the remaining 8 are required to introduce delays between the ON pulses. At 1.1 kV DC excitation, ~90% conversion efficiency was demonstrated by the model with frequency content upto 4 GHz above 0 dB, and highest magnitude close to 500 MHz.

(B) A MOSFET-switched FWG prototype implementing coaxial TLs has been fabricated and tested with a goal to demonstrate a tunable pulse generator capable of demonstrating chirped pulses. The primary operation of a FWG has been demonstrated with up to 8 TL segments under balanced and unbalanced load configurations. The experimental implementation results on pulse chirp agreed with the simulation results. However, pulse overlap, and deconstructive interference were observed in the 8-segment configuration, which were addressed in the LETL-based FWG prototypes.

(C) Lumped-element-based ladder networks were implemented as an alternative to overcome the limitations of coaxial lines in terms of size and weight. This also provides an advantage of integrating the TLs into the PCB, minimizing the distance between the switch (MOSFET) and charged lines. An 8-segment LETL-FWG was simulated in LTSpice. The components of the LETL were selected to generate ~13.05 ns pulsewidth/delay. When switched at 100 kHz PRR, upto 60 MHz frequencies were generated. with a ~50% conversion efficiency. While the balanced load configuration load response was in-line with the theoretical expectation, pulse train overlap was noticed under unbalanced load configuration, limiting the frequency response. Additional study is required to understand the TL line arrangement required for unbalanced load operation.

(D) In the 4-segment prototype, two TL segments were equipped with 6 cells of 75nH-30pF each, the remaining were equipped with 6 cells of 110nH-43pF, capable of generating 9 ns and 12 ns, respectively. Frequencies upto 50 MHz have been measured across the load. However, when measured under an unbalanced load configuration, a lower voltage was seen alongside reflections and pulse overlap. The lower voltage has been attributed to the power loss occurring at unmatched load resistor, and the pulse overlap due to the unoptimized signal reflection path.

(E) A 12-segment FWG with dynamic tunability was designed with LC ladder networks on a 4.1″ ×14.1″ PCB. Pulse width tunability has been demonstrated by mechanically tuning the L and C parameters. Resulting in a frequency response of 10 – 60 MHz. However, a consistent reduction in peak voltage across the pulse train has been noticed as the pulse train progresses, as shown in Figure 7.3.2. This phenomenon could have been potentially caused either due to (i) the inability of the MOSFET to switch all 6 pairs of transmission lines simultaneously, or (ii) the distance to the transmission line segments from the MOSFET being long, causing a

delay in switching. If (i) is validated, creates the need for a faster switch/technology alternative to facilitate simul-switching.

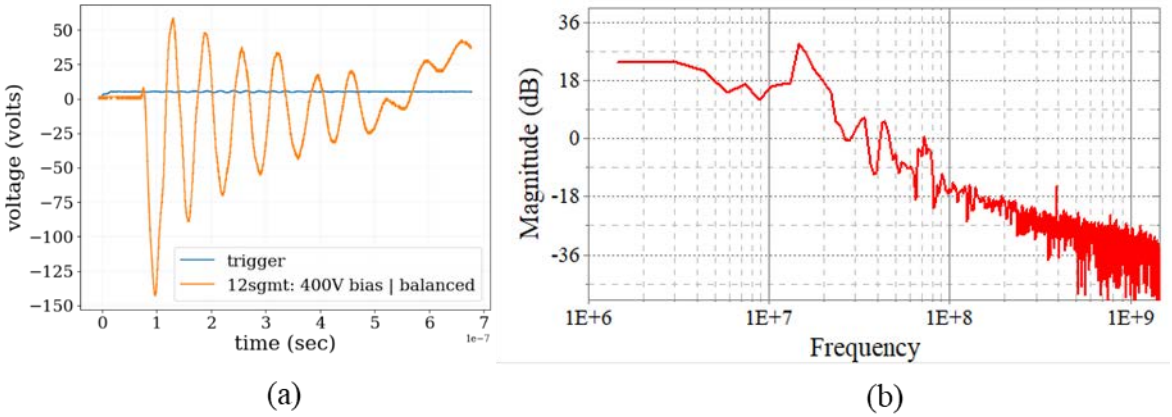


Figure 7.3.2. (a) Load characteristics of a 12-segment fixed pulse width LETLs with 4x 300nH-120pF LC ladder cells in each segment, capable of generating 24 ns pulse width,**(b)** frequency domain representation of (a)

(F) The consistent drop in the peak voltage reported in (E) was measured in Gen 2 prototype despite revising the 12-segment FWG design with modified switch position, optimized ground plane and reduced PCB footprint. The MOSFET with 10.5ns t_{rise} and ~60 ns t_{fall} has been determined to be the bottleneck of the FWG performance, inhibiting simultaneous switching of TL segments. >10.5 ns t_{rise} requires long pulse widths (>11 ns), limiting the frequency to <100 MHz. A solid-state PCSS-like switch capable of low jitter and sub-ns rise-time with compact form factor can greatly benefit all-solid-state implementation of the FWG.

7.4 Pulse-Compression-Based Signal Amplification

(Feyza Berber Halmen)

7.4.1 *Problem Statement, Approach, and Context*

Primary Problem: Solid-state amplifiers, such as gallium-nitride-based high electron mobility transistors (GaN HEMT), can be used as high power microwave (HPM) sources to achieve the SWAP-C2 performance metrics necessary to support the cUAV Naval afloat mission. However, even the best high-power GaN HEMTs are limited to 2–3 kW of peak power, much lower than the 0.1 to 3 MW pulsed power available from traditional HPM sources such as travelling wave tubes (TWTs). Achieving a power density of 1 W/cm^2 at a distance of 10 m with a high gain (≥ 10 dBi) narrow-band antenna requires an input power increase of two to three orders of magnitude. Power combination methods to achieve an effective radiated power (ERP) at MW scale require 10 s to 100 s of GaN HEMTs, compromising the SWAP-C2 performance.

Solution Space: Pulse compression techniques are used to increase the peak power and lessen the pulse width in HPM applications. Adapting pulse compression at the GaN

HEMT or any other SWAP-C2 compatible source output can achieve sufficient ERP with an optimal radiating element.

***Sub-Problem*:** Pulse compression is generally used to generate a pulsed output with a high peak output power (P_{out_peak}) and a wideband frequency content from a DC input voltage. The main challenge lies in identifying a pulse compression technique that can be used to amplify a narrowband RF input signal. Some of the circuit elements for common pulse compression techniques, such as the saturable inductors used for energy storage in magnetic pulse compression (MPC), exhibit increasingly lossy behavior with high frequency. Another challenge will be to determine, if any, the operating frequency limits of the suitable pulse compression technique for high-frequency, high-power signals.

State-of-the-Art (SOTA): Large magnetic pulse compression (MPC) circuits (>1 m^3, >1000 lbs) have demonstrated peak output power up to a few GWs. Smaller versions (~0.125 m^3, 50 lbs to 100 lbs) can achieve 7.5 MW peak power [1].

Deficiency in the SOTA: Traditional MPC systems are large (few meters long), leverage huge transformers, and require liquid coolant such as transformer oil, which leads to undesirable system mass values of ≥1000 lbs. They are used for generating medium or high pulse power traditionally from DC or AC (50/60 Hz) high voltage supplies. There is no known example of high-frequency signal amplification utilizing MPC.

Solution Proposed: Developing a pulse compression circuit that will act as a high-power signal amplifier with a gain of ≥10. Utilizing magnetic pulse compression, or any other suitable pulse compression method, for high power signal amplification with source fidelity.

Relevance to OSPRES Grant Objective: Pulse compression will enable a size and cost efficient solution to high power signal amplification that will lead to HPM source development with optimal SWaP-C2 parameters.

Risks, Payoffs, and Challenges:

Challenges: Modeling pulse compression circuits for high-frequency operation can present a challenge. Pulse compression circuits are generally evaluated in SPICE simulators with low frequency AC / transient simulations. SPICE is a lumped-element model simulator and cannot solve for the distributed-element model required at high frequencies where the wavelengths become comparable to the physical dimensions of the circuit. Some circuit components, such as the saturable inductor in the MPC, are not available in SPICE or many other simulators and need to be modeled using behavioral models and proprietary material data. Pulse compression circuit modeling, especially at high frequencies, needs to be investigated.

Risks: Pulse compression methods are usually lossy in nature and generate a considerable amount of heat; therefore, designing a proper cooling method must be carried out, which may inadvertently increase the volume (size and weight) of the overall design.

7.4.2 *Tasks and Milestones / Timeline / Status*

(A) Milestone – Demonstrate 2–3 times increase in peak power and compression gain using magnetic pulse compression (MPC) [*estimated completion by MAY22*].

1. Subtask – Model saturable inductors in LTSpice or Matlab/Simulink in order to be able to develop MPC simulations / NOV21 / **Complete**.
2. Subtask – Design of MPC circuit with RF input and simulation in LTSpice or Matlab/Simulink to evaluate the resulting amplification and frequency content. / **MAY22**
3. Subtask – Model the high frequency behavior of MPC circuit / NOV21 / Ongoing.
4. Subtask – Build and test the MPC prototype using bench top power supply / OCT–**MAY22** */ Ongoing*.

(B) Milestone – Increase the compression gain available from MPC.

(C) Milestone – Build and test SWAP-c2 compatible high-frequency MPC prototype with GaN source.

7.4.3 *Progress Made Since Last Report*

(A.3) Kemet toroid cores, that were used in initial MPC testing, were simulated in LTSpice to model their permeability change with applied volts·second. Using the modeled cores, a 2 stage MPC circuit was simulated and the details of MPC operation were investigated.

7.4.4 *Technical Results*

(A.3) LTSpice simulations, which were paused due to magnetic core loss and COTS magnetic core material research, were resumed. Previously, only the ability to simulate saturable inductors in LTSpice was investigated. Saturable inductors can be modeled with tanh or arctan flux behavior, but the Chan model [2] provides a more accurate B-H behavior as explained before.

Kemet toroid cores, that were used in the initial MPC testing, are simulated with the Chan model using the data provided by Kemet. B-H curve and toroid data provided by Kemet, as well as the calculated magnetic area and length are tabulated in Table 7.4.1 and were used for the Chan model. Magnetic length, l_e, and cross-sectional area, A_e, of the toroid are calculated from its outer and inner diameter, OD and ID, and height as:

$$A_e = h(OD - ID)/2 \tag{1}$$

$$l_e = \frac{\pi(OD - ID)}{ln(OD/ID)} \tag{2}$$

Table 7.4.1. Kemet NiZn material 700L toroid properties

B_{sat}(mT)	B_r(mT)	H_c(A/m)	OD(mm)	ID(mm)	h(mm)	A_e (mm^2)	l_e(mm)
350	150	40	61	33.2	25	347.5	143.6

B-H curve of a magnetic material can be related to the electrical characteristics of the inductor through a few conversions as shown in Figure 7.4.1. As observed in the figure, resulting time integral of voltage vs current graph resembles the B-H curve and depicts the saturation behavior with applied volts·second.

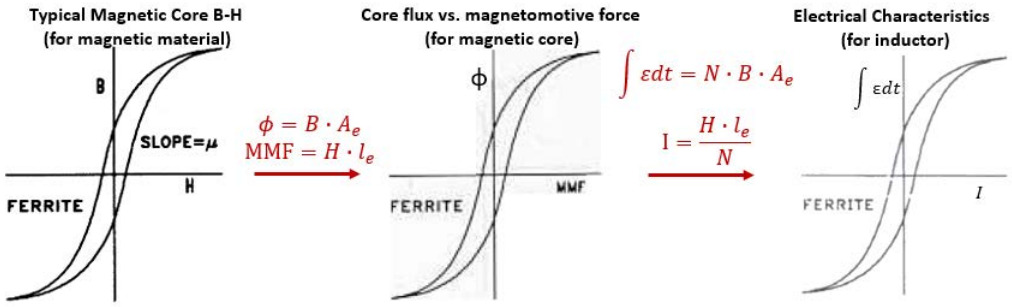
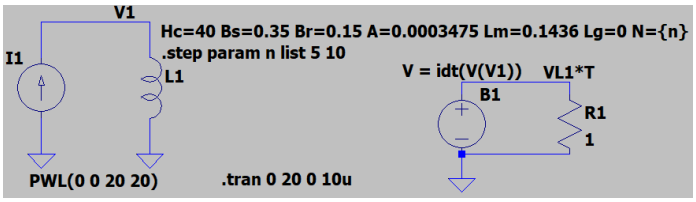


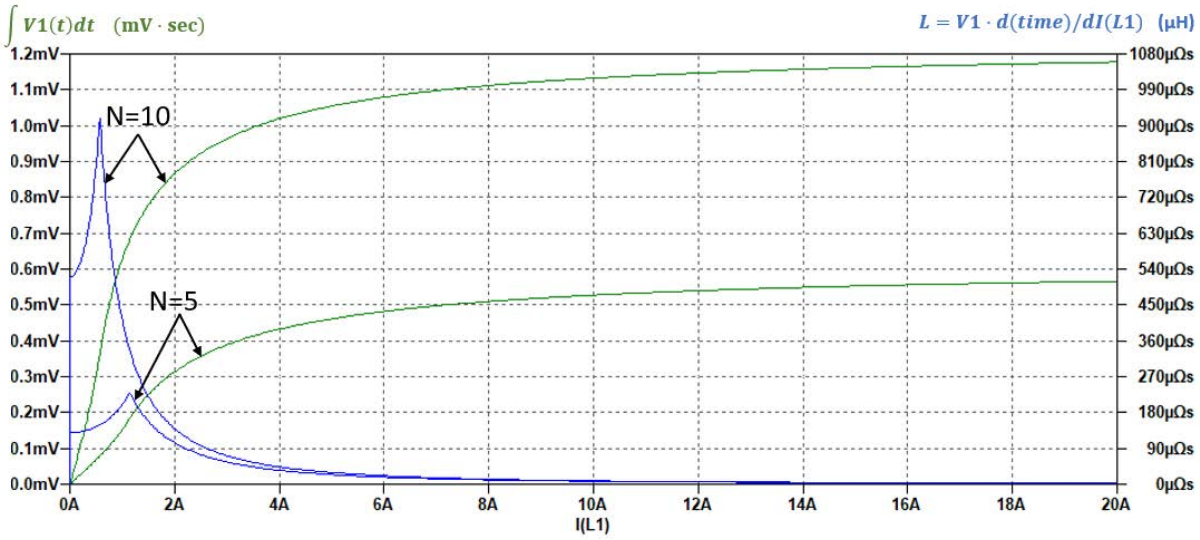
Figure 7.4.1. Conversion of magnetic material B-H curve to magnetic core flux vs. MMF curve and inductor time integral of voltage vs. current curve.

For volts·second vs. current plots for the magnetic core, behavioral voltage source needs to be used in LTSpice to calculate the time integral of the inductor voltage. Figure 7.4.2(a) shows the Chan model of the Kemet inductor as well as the circuit for voltage integration. A current ramp of 20A is applied within 20 seconds in the transient simulation in order to ensure saturation. The inductor is simulated with number of turns, N, of 10 and 5 to model the behavior of saturable inductors in stage 1 and 2 of the MPC circuit. Time integral of inductor voltage and the inductance vs. current are plotted in Figure 7.4.2(b) in green (left axis) and blue (right axis), respectively. Plot shows that inductor with N=10 saturates with time integral of inductor voltage approaching 1.2 mV·s and N=5 saturates approaching 0.6 mV·s. Same volts·second products are calculated from the saturation equation $V \cdot T > N \cdot B_{sat} \cdot A_e$ and the inductor with N=10 requires twice as much VT according to the equation. Higher N for the same magnetic core also results in lower current for saturation:

$$L \cdot I > B_{sat} \cdot N \cdot A_e \quad \rightarrow \quad N \cdot I > B_{sat} \cdot l_e / \mu \tag{3}$$



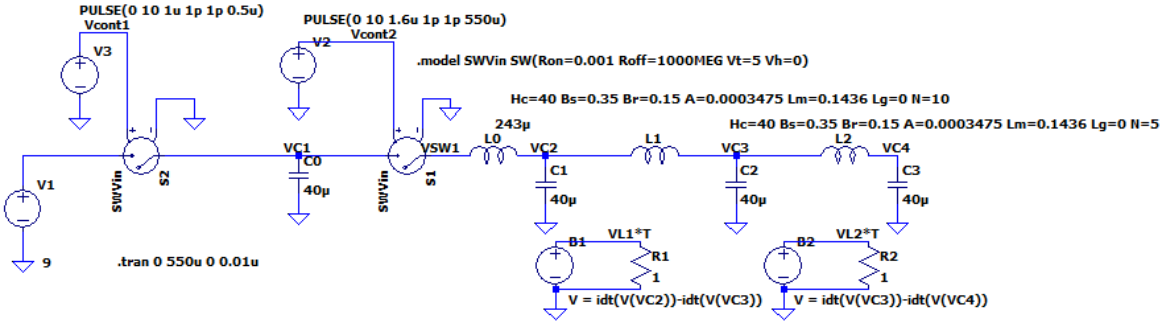
(a)



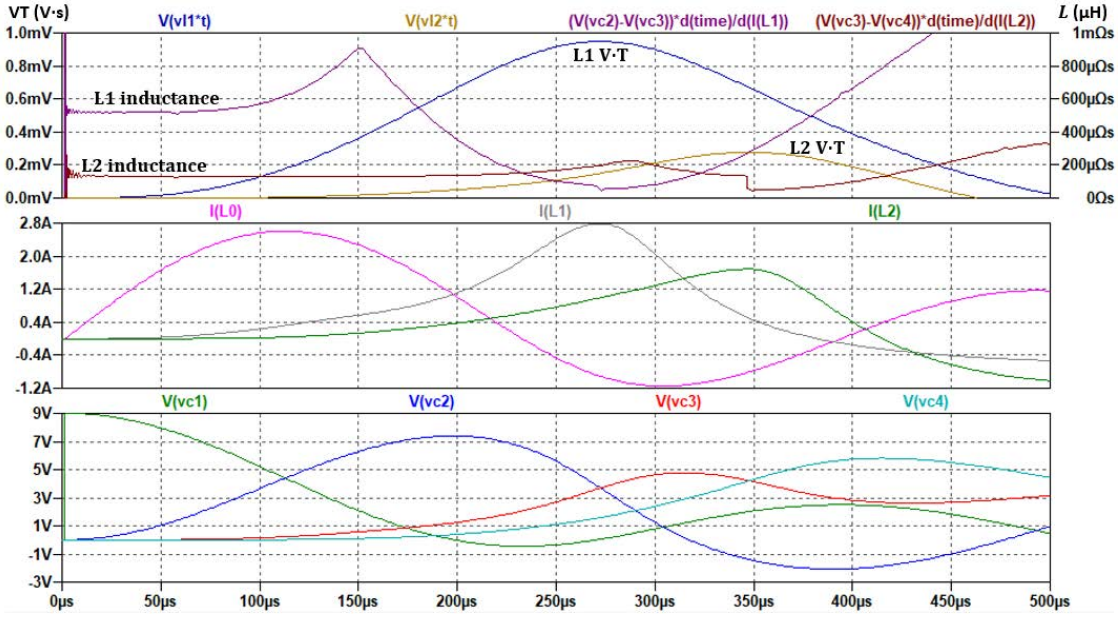
(b)

Figure 7.4.2. (a) LTSpice simulation circuit for saturable inductor with Chan model using Kemet NiZn toroid core, (b) Volts·second product and inductance vs. current for saturable inductors with N=5 and 10.

Inductance value is calculated as $L=V_L \cdot dt/dI_L$ from inductor voltage and current. Note that the inductance changes with applied current and voltage even before saturation, implying constant slope change in the B-H curves - either due to the material property or due to inaccuracy in the Chan model. Initial inductance values are 520 µH and 130 µH for N=10 and N=5, respectively, with a perfect ratio of 4 between the two, as expected from $L_1/L_2=N_1^2/N_2^2$. As current increases, the ratio between the two inductances drops for a given current value. This is because the inductors are at different operating points of the B-H curve as $I \propto H/N$. Relative permeability calculated from initial inductance values of 510 and 130 µH is 1709 whereas the initial relative permeability reported by Kemet for NiZn is 780. In general, the initial permeability provided by suppliers is obtained from the slope of initial magnetization and is different from the permeability obtained from the B-H loops at different field strengths. LTSpice notes that initial magnetization curve and minor B-H loops are obtained from the major loop parameters according to the Chan model [2]. The difference in calculated and supplier provided initial permeability values suggest a possible inaccuracy in the simulated B-H loops.



(a)



(b)

Figure 7.4.3. (a) LTSpice simulation circuit for 2-stage MPC previously tested in the lab, (b) simulated capacitor voltages, inductor currents and VT and L for saturable inductors.

Next, 2-stage MPC circuit that was previously tested in lab is simulated using the Chan model as depicted in Figure 7.4.3(a). Simulated capacitor voltages, inductor currents as well as the inductances and volts·second products of the saturable inductors L1 and L2 are given in Figure 7.4.3(b). The figure shows that the saturable inductors are not fully saturated during the circuit operation, with their inductance values reaching only below 100 µH. Current is compressed but not amplified in this circuit. Inductance saturation is crucial for MPC power amplification; however, it needs to be in sync with LC resonant energy transfer for the proper circuit operation. The circuit equation for MPC input stage can be written from KVL as:

$$\frac{1}{C_0}\int i_1(t)dt + L_0\frac{di_1(t)}{dt} + \frac{1}{C_1}\int i_1(t)dt = 0 \qquad (4)$$

From the initial conditions $i_1(t) = 0$ and $L_0 \frac{di_1(t)}{dt} = V_0$, the solutions for $i_1(t)$ and $v_{C1}(t)$ are:

$$i_1(t) = \frac{V_0}{L_0 \omega_0} \sin \omega_0 t \tag{5}$$

$$v_{C1}(t) = \frac{V_0}{C_1 L_0 \omega_0^2} (1 - \cos \omega_0 t) \tag{6}$$

where ω_0 is defined as:

$$\omega_0 = \sqrt{\frac{1}{L_0 C_{01}}} = \sqrt{\frac{1}{L_0}\left(\frac{1}{C_0} + \frac{1}{C_1}\right)} = \sqrt{\frac{C_0 + C_1}{L_0 C_0 C_1}} \tag{7}$$

Equations (5) and (6) show that maximum current occurs at $t = \pi/2\sqrt{L_0 C_{01}}$ (from $\sin \omega_0 t = 1$) and maximum voltage occurs at $t = \pi\sqrt{L_0 C_{01}}$ (from $1 - \cos \omega_0 t = 2$). From equation (5), it can also be shown that maximum current is obtained for C_1=C_2=C as:

$$I_{1,max} = V_0 \sqrt{C/(2L_0)} \tag{8}$$

For equal capacitors, the maximum voltage is equal to V_0. Same equations are used for the next stage, under the assumption that its inductance is much smaller than that of the first stage during its operation. This is ensured by the use of a saturable inductor which is designed to saturate at the time $t = \pi\sqrt{L_0 C_{01}}$ when C_1 is charged to its maximum value. Saturable inductor presents high inductance, hence isolation, between the stages until it saturates. Its lower inductance during saturation ensures the input capacitor discharge through the saturable inductor.

Simulation results from Figure 7.4.3 show that the resonant energy transfer in the input stage from capacitor C_0 to C_1 is complete around 200 µs when the VT product for saturable inductor L_1 has not yet reached the saturation value of ~1.2 mVs. Capacitor C1 discharges through L1 which still has a high inductance value that results in a larger time constant for the first MPC stage. In order to fix the MPC operation by ensuring inductor saturation, either the time constant for resonant transfer or the input voltage needs to be increased. Figure 7.4.4 shows the simulation results for the same MPC circuit with 27 V input voltage instead of 9 V. With higher input voltage, both saturable inductors are fully saturated. Even though the saturation for the 1st MPC stage occurs before the resonant energy transfer is complete in the input stage, instantaneous input power is increased from 0.1 kW to about 1.7 kW at the output.

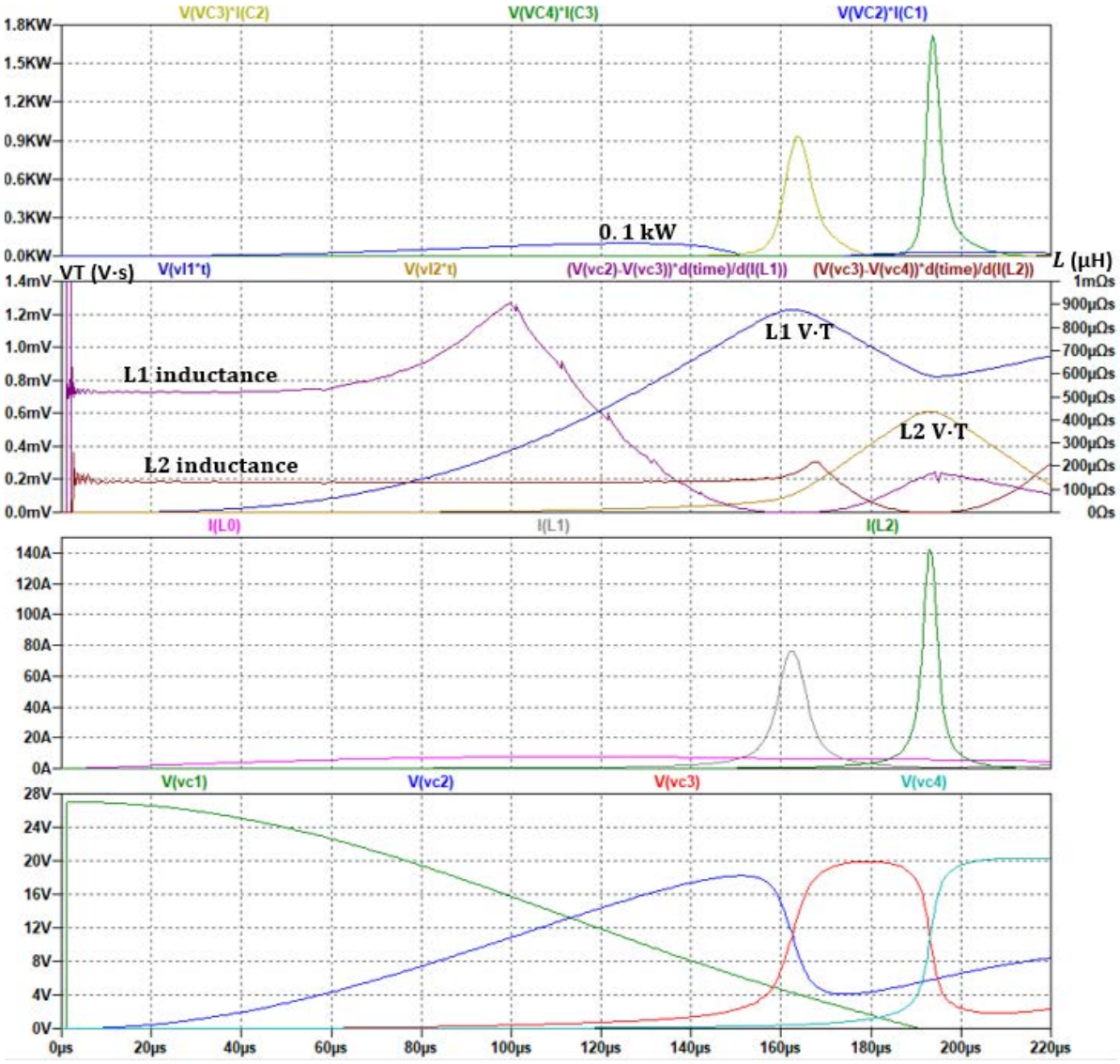


Figure 7.4.4. Capacitor voltages, inductor currents, VT and L for saturable inductors, and instantaneous power for the circuit of Figure 7.4.3(a) with V1=27 V.

Another method to fix the MPC operation would be to increase the time constant $t = \pi\sqrt{L_0 C/2}$ for the resonant energy transfer. Equation (8) shows that, increasing the inductance value will decrease the maximum output current of the MPC stage. Therefore, capacitor value should be increased for higher time constants. Figure 7.4.5 shows the simulation results for C = 200 µF for the same circuit. Again, the input stage resonance transfer is not complete prior to L1 saturation. In order to optimize the resonance time constant, while keeping the inductor saturation VT, input stage inductance can be reduced. This will increase the current through L0 and will result in higher flux, preserving the VT despite the shorter time to saturation. Simulation results for C = 200 µF and L0 = 90 µH with 9 V input voltage are given in Figure 7.4.6. The capacitor voltage plot shows

that the first capacitor is fully discharged right before the second capacitor starts discharging, implying perfect alignment of saturation and resonance for the input stage.

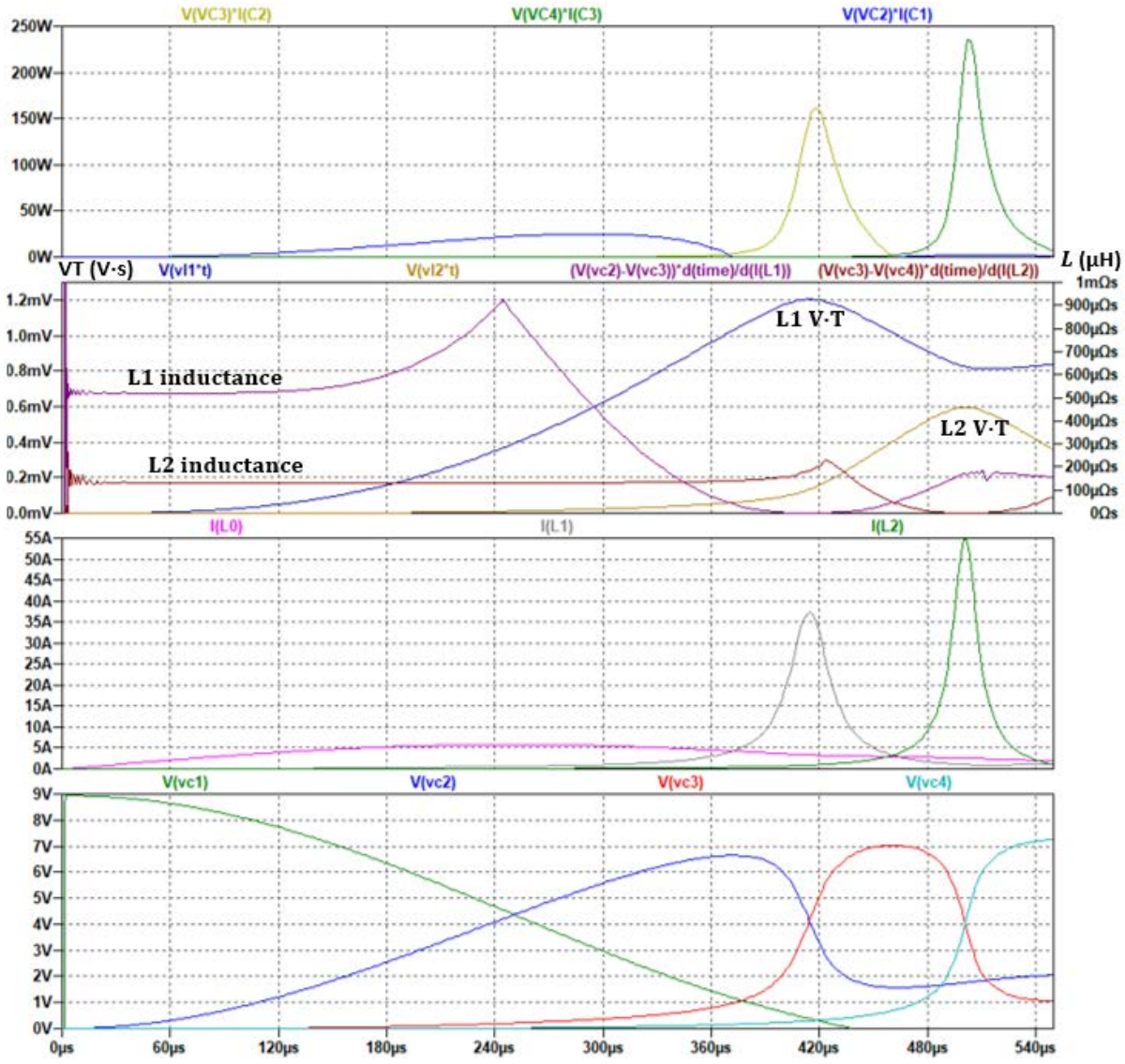


Figure 7.4.5. Capacitor voltages, inductor currents, VT and L for saturable inductors, and instantaneous power for the circuit of Figure 7.4.3(a) with C=200 µF.

Another important point to note is the slow change of inductance for the Kemet NiZn core prior to saturation. This leads to pre-pulse currents and is suspected to be the reason for the capacitors not to be fully charged to the applied input voltage. This can be observed in the capacitor voltage plot of Figure 7.4.6, where VC2 only reaches 8.1 V instead of 9 V that is discharged from the input capacitor. The remaining voltage of 0.9 V is at the next capacitor as observed from VC3. A sharper saturation behavior is optimum for the MPC operation in order to avoid voltage loss and a subsequent drop in compression efficiency. The MPC circuit design will be optimized based on the simulation findings.

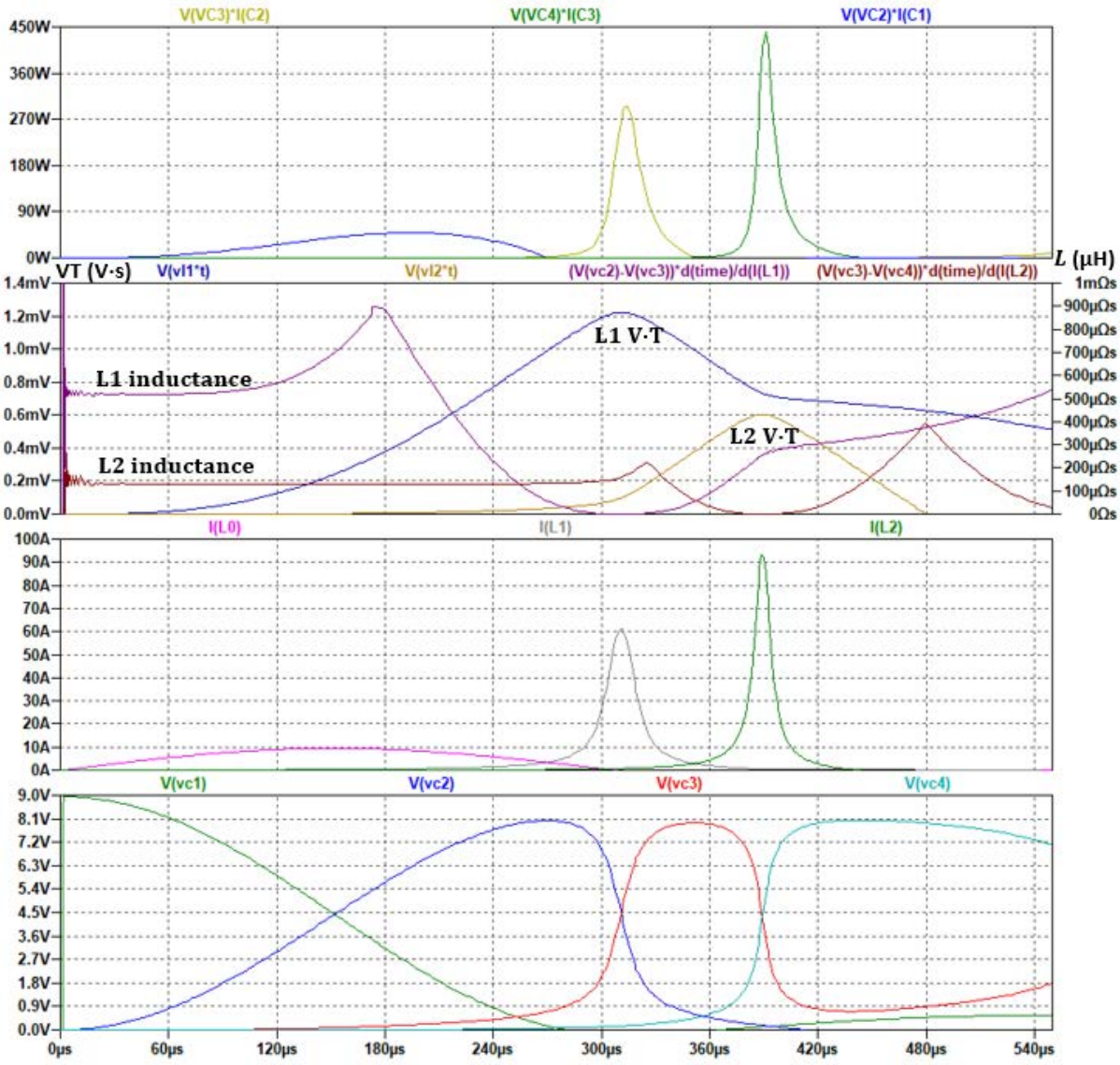


Figure 7.4.6. Capacitor voltages, inductor currents, VT and L for saturable inductors, and instantaneous power for the circuit of Figure 7.4.3(a) with C=200 µF and L0=90 µH.

7.4.5 *Summary of Significant Findings and Mission Impact*

(A) Initially a basic 2-stage magnetic pulse compression circuit was built and tested with DC input to better understand the MPC principles and considerations such as inductor sizing, pre-pulse currents and inductor saturation. Next, saturable inductor modeling was realized in LTSpice with inductor flux expression and Chan model methods available. Prior to MPC system simulations, magnetic core losses were investigated and core selection constraints were determined based on the core losses and high frequency MPC design considerations. Next, different magnetic core

materials were investigated to determine the most suitable candidate for high-frequency MPC. As reported previously, such a core should have high resistance, narrow hysteresis loop, minimized eddy current area, and low saturation flux density (B_{sat}). High permeability (μ) and very sharp saturation characteristics are also preferred in order to minimize pre-pulse currents and resulting MPC gain loss. NiZn ferrites are the best option among the commercially available magnetic cores for the high frequency MPC application as they have the highest operating frequency, low B_{sat}, and sufficiently high μ. After investigating suitable magnetic cores and their properties, LTSpice simulations of the previously tested 2 stage MPC circuit were resumed using the Chan model for Kemet NiZn cores. Simulations suggest that synchronizing the resonant energy transfer with inductor saturation is crucial for MPC operation. If inductor saturation is not achieved at the end of resonant energy transfer, time compression and, therefore, current amplification is compromised. The time integral of the applied voltage must be increased to ensure timely saturation. This can be achieved by increasing the input voltage or the time constant of MPC stages through a higher capacitor value. Increasing the inductance of a stage, to increase the time constant, is not recommended as this results in a reduced output current. It is also observed that the Kemet NiZn cores have a relatively slow change in inductance prior to saturation, increasing the prepulse currents and resulting in losses in voltage transfer. Simulations provide an important guideline for MPC optimization.

7.4.6 *References*

[1] D. Zhang, Y. Zhou, J. Wang and P. Yan, "A compact, high repetition-rate, nanosecond pulse generator based on magnetic pulse compression system," in IEEE Transactions on Dielectrics and Electrical Insulation, vol. 18, no. 4, pp. 1151-1157, August 2011, doi: 10.1109/TDEI.2011.5976109.

[2] J J. H. Chan, A. Vladimirescu, X.-C. Gao, P. Liebmann and J. Valainis, "Nonlinear transformer model for circuit simulation," in *IEEE Transactions on Computer-Aided Design,* vol. 10, no. 4, pp. 476-482, 1991

8 Antenna Development

8.1 Tradespace Analysis of an Array of Electrically Small Antennas (ESAs)

(Bidisha Barman and Deb Chatterjee)

8.1.1 *Problem Statement, Approach, and Context*

Primary Problem: Determine the extent to which the physical aperture size of an antenna array, composed of patch elements, can be reduced, while maintaining performance in peak power density, bandwidth, and electronic beam steerability over the UHF range (0.4–1 GHz), compared with present-art high-power-microwave-capable antenna arrays.

Solution Space: An array of patch antenna elements whose feed, two-dimensional shape, and relative placement (i.e., intra-, and inter-element design) allow for the physical aperture size to be reduced by more than 20% compared with the present-art.

Sub-Problem: To overcome scan blindness (as the main beam is electronically steered), due to the excitation of surface waves (SW). (Note: scan blindness is a common phenomenon in electrically small microstrip patch antenna arrays).

State-of-the-Art (SOTA): Horn, reflector, Vivaldi, valentine, etc. are some of the commonly used ultra-wideband (UWB) antenna elements in a phased array for high-power microwave (HPM) transmissions.

Deficiency in SOTA: Large physical aperture size of the antennas.

Solution Proposed: Using electrically small antennas (ESAs) as array elements and optimizing their performance in terms of both near-field (bandwidth) and far-field (directivity) parameters, followed by arrangement of the ESAs in suitable lattice structures (preferably, hexagonal/triangular) to reduce the overall array aperture area. Using stochastic and machine learning (ML) algorithms to optimize antenna element and array performance.

Relevance to OSPRES Grant Objective: Provides design and optimization guidelines for UWB ESA elements, especially coaxial probe-fed microstrip patch antennas, and arrays for HPM applications.

8.1.2 *Tasks and Milestones / Timeline / Status*

(A) Develop an Array Pattern Tool in the context of lightweight calculations of large antenna arrays / JAN–MAY 2021 / Completed code.

(B) Investigate the effects of array aperture area reduction on different array parameters (such as gain, beamwidth, electronic beam steerability) and present a comparative study of antenna array parameters as a function of array aperture area / JAN–MAY 2021 / Completed investigations of arrays on infinite ground planes.

(C) Build minimum viable validation prototypes of single ESA elements on substrates that have good power handling capabilities for HPM transmissions at UHF range (such as polyethylene, FR-4, TMM-10i, TMM-6) / JAN 2021–MAR 2022 / Completed custom connector modeling to feed UWB ESA elements in the UHF range.

(D) Optimization of ESA (single element) performance using ML based stochastic search algorithms / JUN 2021–APR 2022 / Ongoing ML-based multi-objective-optimization (MOO) of ESA elements.

(E) Build minimum viable validation prototypes for arrays of ESA elements/ JUN 2021–MAY 2022 / Ongoing characterization of a 4×4 square array of ESA elements fed by the custom tapered coaxial connectors.

(F) Optimization of array performance using ML algorithms / SEP 2021–MAY 2022 / Ongoing ML-based MOO of antenna array parameters.

8.1.3 *Progress Made Since Last Report*

(C) Build minimum viable validation prototypes of single ESA elements:

a. The S_{11}-parameters and realized gain of the previously manufactured microstrip patch ESA prototypes were tested in the anechoic chamber at Mizzou - University of Missouri (MU) campus.

b. A significant improvement in agreement between the simulated and the new experimental realized gain data has been achieved due to the reduction of multipath reflections from surrounding metal objects within the chamber.

c. Completed modeling of a custom connector that can be used to feed an UWB, coaxial-probe-fed, microstrip patch, ESA element in the UHF region (0.6-1 GHz).

(E) Build minimum viable validation prototypes for arrays of ESA elements:

a. Tested S_{11}-parameters and realized gain of the manufactured array prototypes at the anechoic testing facility at the MU campus.

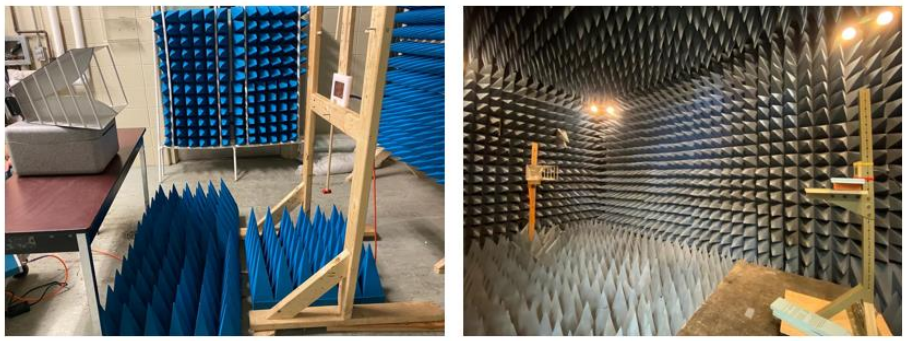
b. Initiated characterization of a 4×4 array, composed of microstrip patch antennas that are fed by the custom coaxial connectors, for operation in the required UHF region (0.6-1 GHz).

8.1.4 *Technical Results*

(C) Build minimum viable validation prototypes of single ESA elements:

Antenna Testing

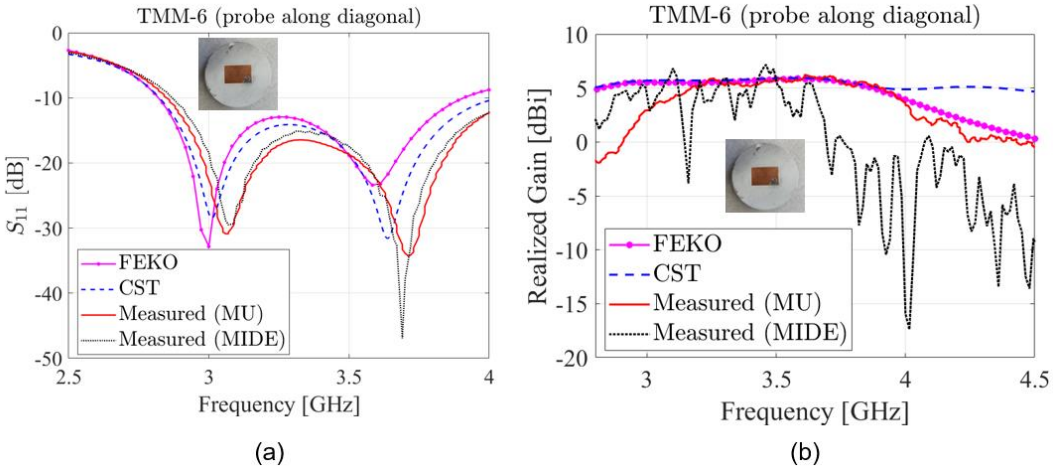
It has been reported earlier that the far-field antenna parameters, such as realized gain, directivity, and radiation patterns, tested in the absence of an anechoic chamber are negatively impacted because of multipath reflections from the nearby metal objects. To reduce the effect of undesirable reflections, the manufactured ESA prototypes were tested for the first time in an anechoic chamber at Mizzou – University of Missouri campus. A comparison of the testing environment in MIDE and at the MU campus is shown in Fig. 8.1.1.



(a) (b)

Figure 8.1.1. Antenna test setup in: (a) MIDE and (b) anechoic chamber at Mizzou - University of Missouri (MU) campus.

The single ESA elements that were tested included two coaxial-probe-fed, wideband, microstrip patches designed on circular-shaped, PEC-backed, TMM-6 and TMM-10i substrates (2.5-5 GHz), and a narrowband, microstrip patch antenna on a rectangular-shaped, PEC-backed, HDPE substrate (0.8-1 GHz). The comparison between experimental and simulated data for these antenna elements are shown in Fig. 8.1.2 through Fig. 8.1.4. In all three cases, the measured S_{11}-parameters are shown to agree well with the simulation results. Figs. 8.1.2(b) and 8.1.3(b) show that the measured realized gain data from MIDE (in the absence of an anechoic chamber) departed appreciably from the simulated data. However, a significant improvement in agreement has been achieved between the simulated and the new experimental data, from the MU testing facility, due to the reduction of unwanted reflections from surrounding metal objects.



(a) (b)

Figure 8.1.2. (a) S_{11} and (b) realized gain of a wideband microstrip ESA on a 6.35 mm TMM-6 board at the higher S-band.

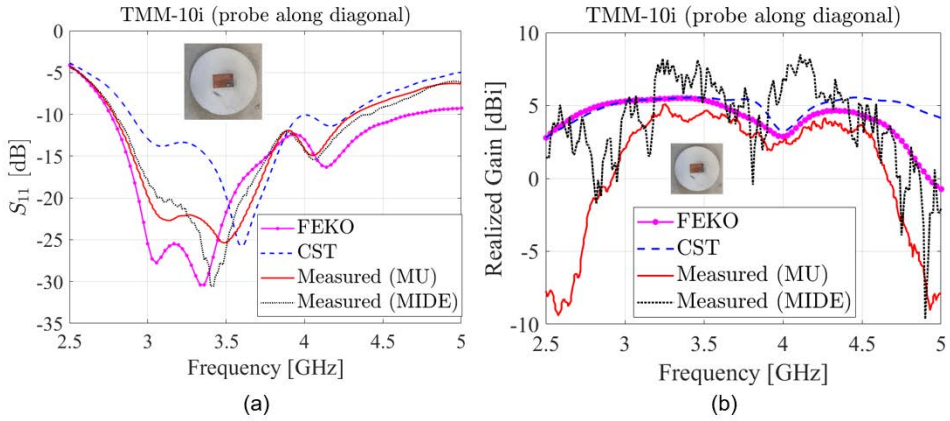


Figure 8.1.3. (a) S_{11} and (b) realized gain of a wideband microstrip ESA on a 6.35 mm TMM-10i board at the higher S-band.

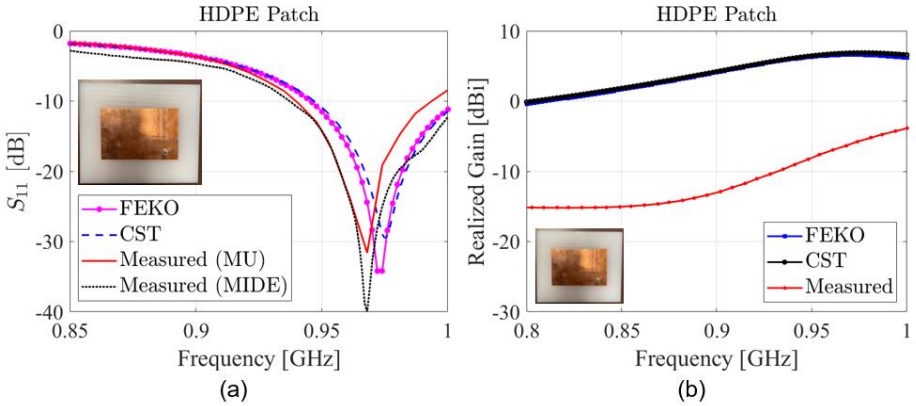


Figure 8.1.4. (a) S_{11} and (b) realized gain of a narrowband microstrip patch antenna on a 0.65-inch polyethylene board at the required UHF range.

For the narrowband antenna designed on an HDPE panel, a huge discrepancy ($\sim$15 dBi) between the measured and simulated realized gain has been observed, as illustrated in Fig. 8.1.4(b). One reason for this disagreement could be the difference between the actual material properties and the properties that were assumed for simulating the model. The exact material properties of the HDPE panel used for the prototype was unknown, and hence, the model was simulated considering the dielectric constant of HDPE, $\varepsilon_r = 2.2$, and dissipation factor, $\tan\delta = 0.0009$.

Characterization of the wideband antenna element with tapered coaxial connector:

As reported earlier in ONR-OSPRES-Grant MSR NOV 2021 and JAN 2022, to achieve $> 30\%$ impedance bandwidth from a coaxial-probe-fed microstrip patch antenna, the feed-probe should have a radius $r_p \geq 0.005\lambda$ (λ is the wavelength at the center frequency of operation) and must be placed strategically along the patch diagonal. At the desired UHF range (0.6–1 GHz) the radius of the feed-probes must be $r_p \gg 2$ mm. However, the commercially available SMA or N-type connectors have $r_p \approx 0.65$ mm. Therefore, to meet the requirements of broadband, coaxial probe-fed, microstrip patch, ESA element designs in the UHF range, a custom coaxial connector (with $r_p \gg 0.005\lambda$) has been modeled. The

schematic of the custom coaxial connector is shown in Fig. 8.1.5(a). It consists of two dissimilar coaxial lines with different dimensions and characteristic impedances (Z_1 and Z_3). The center conductor of the thicker section is used to excite the microstrip patch and has a radius, $r_{i1} = 6$ mm. The center conductor of the thinner section has the dimension of a commercially available SMA connector, viz. $r_{i3} = 0.65$ mm. An intermediate tapered section is used to match the characteristic impedances of these two coaxial sections. The tapering is necessary as the antenna must be connected to the ports of standard instruments (e.g., VNAs and/or signal generators).

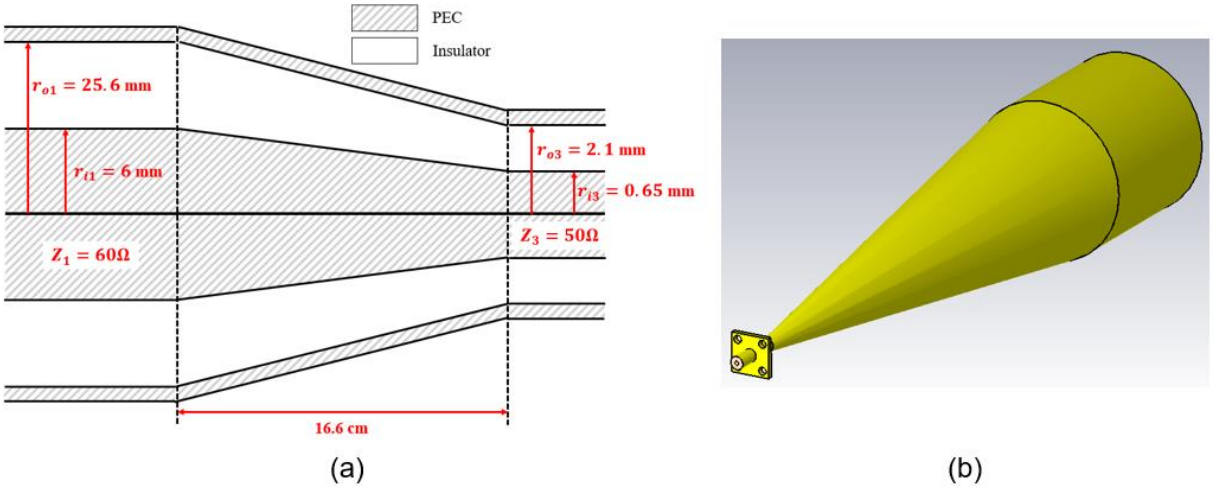
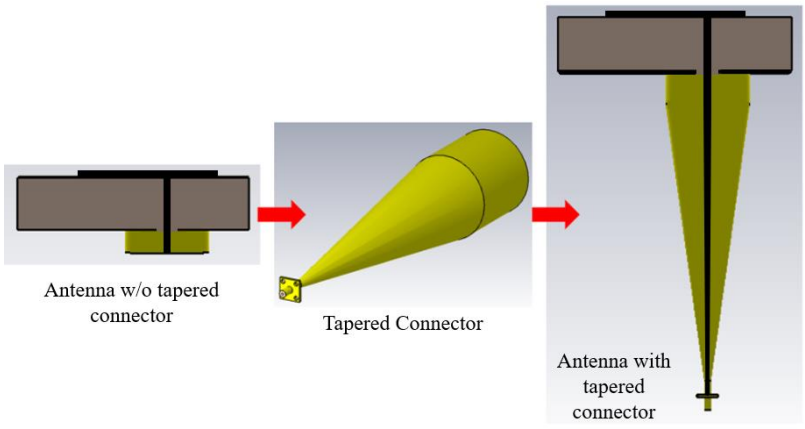


Figure 8.1.5. (a) Schematic and (b) CAD model of the tapered connector.

A wideband, coaxial-probe-fed, microstrip patch antenna that was modeled on a 1.25-inch thick, PEC-backed, polyethylene substrate, for operation at the UHF range (0.7-1.1 GHz) is integrated with the tapered connector, as shown in Fig. 8.1.6(a). The S_{11}-parameter and realized gain of the antenna with and without the custom connector are shown in Fig. 8.1.6(b). The -10 dB bandwidth of the antenna with and without the tapered connector are 30.19% and 36.13%, respectively, with a maximum realized gain of $\sim$7 dBi in both cases.



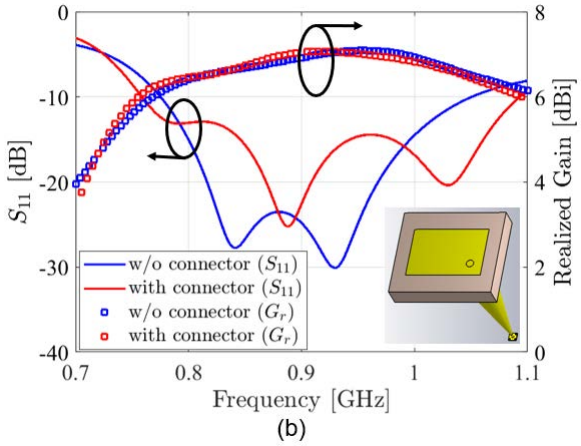


Figure 8.1.6. (a) Side view of the antenna element integrated with the tapered coaxial connector. (b) Simulated S_{11} and realized gain of the antenna.

Time-domain analysis: To understand the effect of various input signals on the electric field, the wideband antenna element, integrated with the tapered connector, was subjected to different input pulses. For the study, three different monopolar pulses, as illustrated in Fig. 8.1.7, were considered. The simulated time- and frequency-domain electric fields, at 1- and 5-m from the element, were obtained via CST Microwave Studio, and are shown in Fig. 8.1.8 and Fig. 8.1.9, respectively.

The peak time-domain electric field and the corresponding rE/V values, at 1- and 5-m from the antenna element, are enlisted in Table 8.1.1. The PPM0731 and ATMarx pulses are shown to have good rE/V values (> 1) and are suitable for transmission through the wideband antenna element.

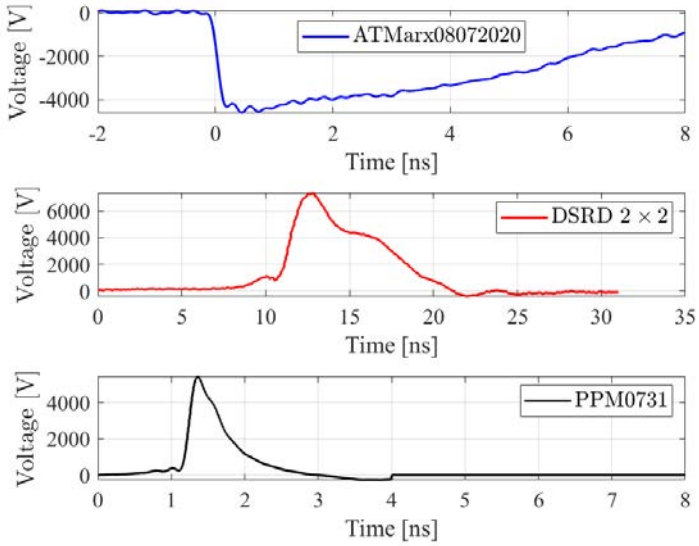


Figure 8.1.7. Input pulses used for the time-domain analysis of the wideband antenna element modeled on a PEC-backed, 1.25-inch thick, polyethylene ($\varepsilon_r = 2.3, \tan\delta = 0.0009$) board.

Table 8.1.1. Optimized microstrip patch antenna array E-field response under different excitation patterns.

Excitation Pattern	E-peak at 1 m [V/m]	rE/V at 1 m	E-peak at 5 m [V/m]	rE/V at 5 m
ATMarx08072020	9376.20	2.03	2015.15	2.18
DSRD 2×2	2355.34	0.32	465.95	0.32
PPM0731	12644.28	2.34	2458.16	2.27

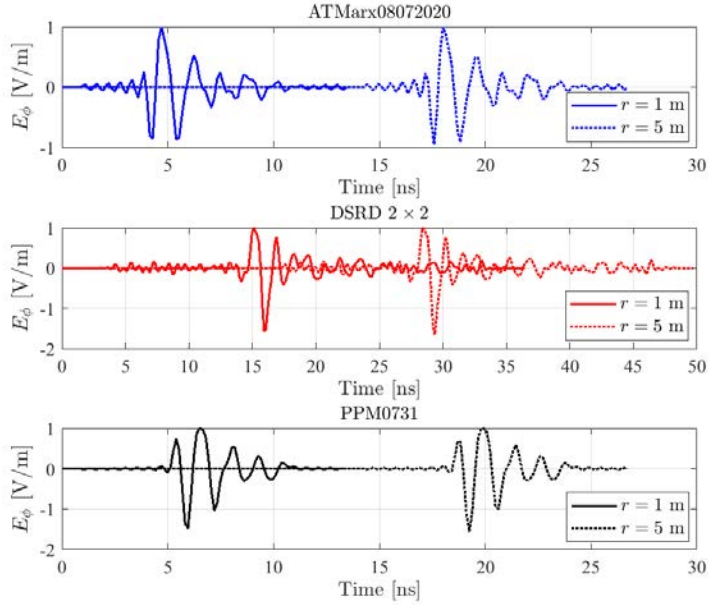


Figure 8.1.8. Phi (ϕ) component of the time-domain electric field when the antenna element is subjected to three different monopolar input pulses (shown in Fig. 8.1.7).

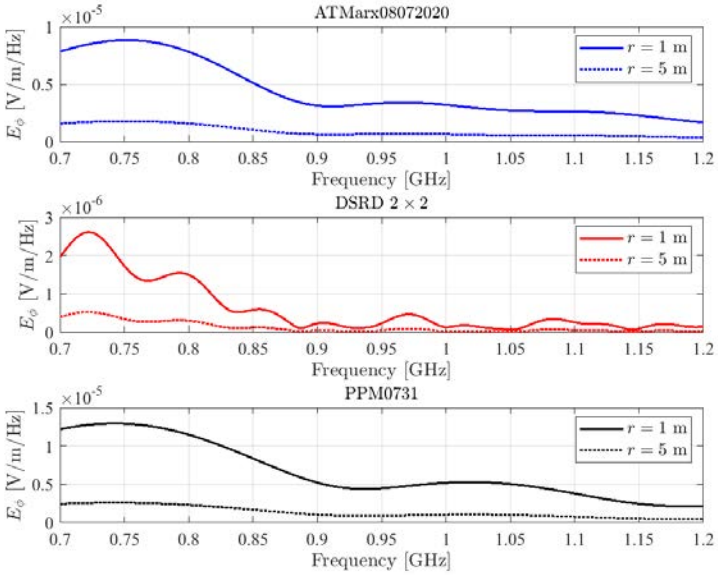


Figure 8.1.9. Phi (ϕ) component of the frequency-domain electric field when the antenna element is subjected to three different monopolar input pulses (shown in Fig. 8.1.7).

(E) Build minimum viable validation prototypes for arrays of ESA elements:

The realized gain and S_{11}-parameters of the embedded elements of two antenna arrays (a 3×3 and a 2×2 square array), which were manufactured earlier, were tested at the MU anechoic chamber. To test the embedded element parameters, the required antenna element was excited while rest of the array elements were terminated in 50-ohm loads. This process was repeated for all the array elements. For brevity, the embedded element parameters of the center-most element in the 3×3 array and element (1,2) of the 2×2 array are reported here. Figs. 8.1.10 and 8.1.11 show that in both arrays, the measured data has better agreement with CST simulated data compared to that of FEKO. This agreement is primarily due to the difference in CAD modeling of feed-probes in CST and FEKO. While FEKO uses a straight-line geometry to model a feed-probe, a very accurate CAD model is used in CST

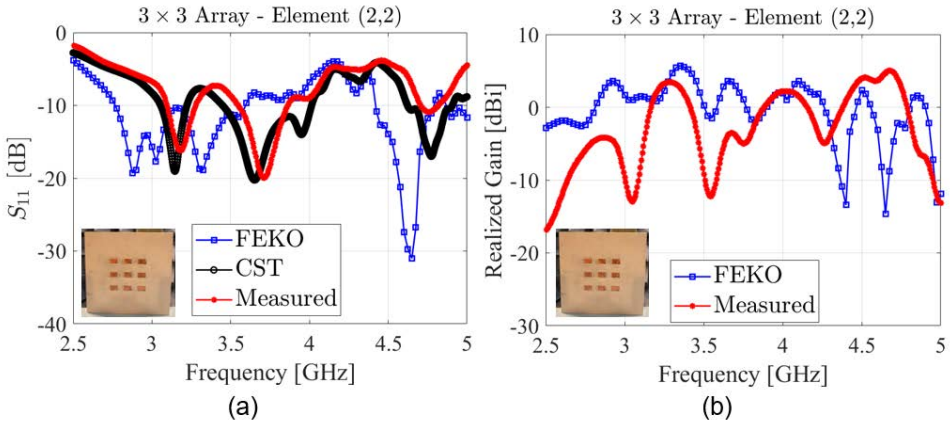


Figure 8.1.10. (a) S_{11} and (b) realized gain of the center-most element of a 3×3 array composed of UWB microstrip patch ESA elements on a 6.35 mm thick TMM-10i substrate. All other elements were terminated in matched loads.

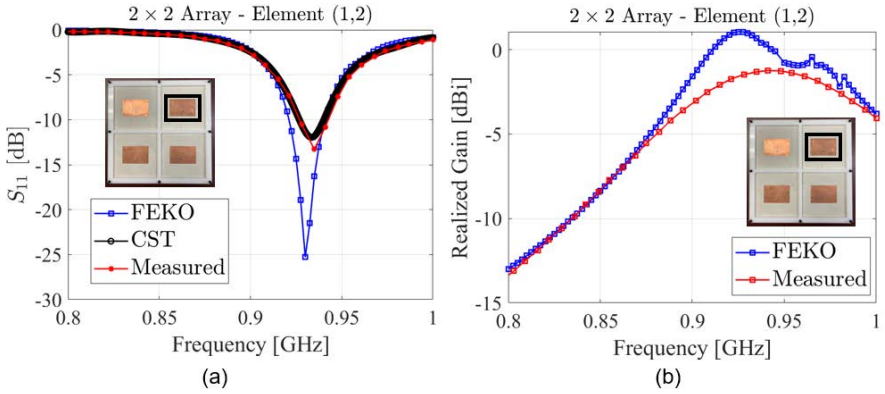


Figure 8.1.11. (a) S_{11} and (b) realized gain of element (1,2) of a 2×2 array composed of narrowband microstrip patch ESA elements on a 6.35 mm thick TMM-10i substrate at the UHF range (0.8-1 GHz).

Having obtained reasonable agreement between the simulated and experimental data, for the wideband 3×3 array (2.5-5 GHz) and the narrowband 2×2 array (0.8-1 GHz), the next target is to design and manufacture the final demonstrable 4×4 array prototype, composed of wideband antenna elements, in the desired UHF region (0.6-1 GHz). For this, the wideband antenna elements in the array must be integrated with the tapered coaxial connectors that is reported in section 8.1.4(C). Characterization of the 4×4 array has been initiated, via CST simulations, and the results will be reported in Apr 2022 MSR.

8.1.5 *Summary of Significant Findings and Mission Impact*

(A) Developing Array Pattern Tool for large arrays calculations:

A MATLAB code has been developed for faster approximation of the radiation pattern of a linear/planar array of any size and composed of any type of antenna elements. The code requires the center element pattern of a small array (say, 3×3) composed of the same type of antenna elements, desired lattice arrangement, and total number of array elements, as user inputs. This work will be included in future publications.

(B) Investigate the effects of array aperture area reduction on different array parameters:

The effect of different array aperture area and lattice arrangements on the array parameters (such as array gain, beamwidth, electronic beam steerability, etc.) have been reported for arrays modeled on infinite ground planes (DEC 2020 ONR-OSPRES-Grant MSR). The results show that, with 30% reduction in the aperture area ($\approx 50\%$ reduction in # of elements), the gain drops by < 3.5 dBi without any scan blindness spotted as the main beam is steered from boresight to $\pm 60°$ in the $640-990$ MHz range.

The array parameters for large arrays ($\geq 15 \times 15$) on finite ground planes could not be computed using the commercial EM solvers (FEKO and CST) due to excessive memory and time consumption. This work will be resumed after developing a method to estimate array performances on finite ground planes, either through ML or conventional approaches.

(C) Build minimum viable validation prototypes of single ESA elements:

Investigated different bandwidth enhancement techniques applicable to single layer microstrip patch ESAs:

a. Method I: Bandwidth enhancement by strategically placing the coaxial probe along 2/3rd of the patch diagonal – This method is proposed and experimentally validated using prototypes manufactured on TMM-6 and TMM-10i substrates at $2.5-5$ GHz. Antennas have been modeled on various substrates (polyethylene, G10/FR-4, TMM-10i) at the UHF range ($0.6-1$ GHz) and are being considered for manufacturing.
b. Method II: Coaxial probe-fed U-slot loaded rectangular microstrip ESAs – A prototype is manufactured on a G10/FR-4 substrate ($0.9-1.3$ GHz) and tested.
c. Method III: L-probe-fed U-slot-loaded rectangular microstrip ESAs – An antenna has been modeled on a TMM-4 substrate that operates in the $0.52-1.17$ GHz range ($\approx 77\%$ 2:1 VSWR bandwidth). Due to the fabrication complexity of the L-probe proximity coupled feed, this antenna will not be manufactured.

(D) Optimization of ESA (single element) performance using regular, and ML based stochastic search algorithms:

Investigated the bandwidth enhancement of the coaxial probe-fed microstrip patch antennas, using regular and ML based stochastic search algorithms (GA, PSO, and Simplex methods), by optimizing the feed-probe location and ground plane shape and size. Compared to regular search algorithms, ML algorithms are found to be less computationally intensive (in terms of time and memory consumption).

(E) Build minimum viable validation prototypes for arrays of ESA elements:

A wideband 3×3 array (2.5–5 GHz) and a narrowband 2×2 array (900 MHz) of coaxial probe-fed microstrip patch ESA elements, on 0.25-inch-thick TMM-10i substrates, have been manufactured. The S_{11}-parameters of the individual elements, in each array prototype, have been tested, with good agreement achieved between the simulated and the measured data. Modeling and characterization of a 4×4 square array, of wideband ESA elements in the UHF region, has been initiated for future prototyping.

(F) Optimization of array performance using ML algorithms:

Completed optimization of inter-element spacings in a 4×4 square and a 10-element hexagonal array in the upper S-band (2.5-5 GHz) with the objective of array boresight gain enhancement. With this knowledge, multi-objective optimization of a 5×5 array, by seeking the best array design parameters, including inter-element spacing, ground plane size, feed-probe locations, etc., in the desired UHF range (0.6-1 GHz), has been initiated.

8.2 Tradespace Analysis of Ultra-Wide-Band (UWB) Koshelev Antenna

(Tyler Williams and Kalyan Durbhakula)

8.2.1 *Problem Statement, Approach, and Context*

Primary Problem: Determine the extent to which the physical aperture area of an antenna array, composed of antenna elements, can be reduced, while maintaining performance in peak power density, bandwidth, and electronic beam steerability over the UHF range (0.4–1 GHz), compared with present-art high-power-microwave-capable antenna arrays.

Solution Space: The Koshelev antenna has a unique design that is capable of generating an UWB response by effectively merging radiation characteristics from a transverse electromagnetic (TEM) horn antenna with exponentially tapered flares, an electric monopole, and magnetic dipoles over a wide frequency range [1]. This opens up an opportunity to investigate the design parameter space and understand parameter effects on impedance bandwidth, radiation pattern, electric field distribution, and other metrics via a tradespace study.

Sub-Problem:

(i) The integration of an impedance transformer to a single element Koshelev antenna to simulate and test the combined (transformer–antenna) performance is currently not feasible using commercial EM simulators.

(ii)The total surface currents on the Koshelev antenna over the desired frequency range arising from the present positioning of TEM exponential flares, an electric monopole, and magnetic dipoles is not yet clearly understood.

State-of-the-Art (SOTA): The balanced antipodal Vivaldi antenna (BAVA) is considered to be the SOTA antenna element due to its exceptional 20:1 impedance bandwidth ratio as well as the ability to handle tens-of-MW input power.

Deficiency in the SOTA: The BAVA design parameter space has been exhausted over the past couple of decades. The physical aperture area still remains very large and there is no viable path through tradespace study for further physical aperture area reduction.

Solution Proposed: Design, simulate, validate, and perform a tradespace study on the important design parameters of the Koshelev antenna array that effectively reduce its physical aperture area while maintaining its UWB properties, in both the frequency and time domains. The Koshelev antenna has been shown in the literature to withstand higher voltage levels (over 200 kV peak voltage), thereby making it a viable antenna element for detailed tradespace study and analysis.

Relevance to OSPRES Grant Objective: From the literature, it was shown that the Koshelev antenna can handle high input voltages (and therefore high power with 50 Ω input impedance), which satisfies the specific OSPRES objective related to high input voltage/power. In addition, this work can yield a center-frequency-dependent, bandwidth-controlled, and electronically steerable Koshelev antenna design that can be quickly modified to the spectrum properties of the ultra-fast rise time input pulse.

Risks, Payoffs, Challenges:

(i) The electrical size of the Koshelev antenna is approximately λ/4 at its lowest operating frequency. Further reduction of electrical size to λ/10 could considerably reduce frequency dependent gain, thereby decreasing the power spectral density.

(ii) Payoffs include the development of a library of antenna metrics data for different shapes and sizes of the individual parts within the Koshelev antenna.

(iii) The large electrical size (>5λ) of the Koshelev antenna at its highest operating frequency poses huge computational challenges.

8.2.2 *Tasks and Milestones / Timeline / Status*

(A) Complete literature search to identify and list antenna elements that satisfy UWB properties and HPM requirements, and down-select accordingly / NOV–DEC20 / Complete.

(B) Complete initial design, simulation, and validation of Koshelev antenna [1] / JAN21 / Complete.

(C) Perform a preliminary parameter study to identify design parameters that considerably reduce the physical aperture area / FEB–MAR21 / Complete.

- Milestone: Using FEKO and/or CST electromagnetic (EM) simulators, reduce the physical aperture size of the Koshelev antenna to at least 95% of its original design and show minimal to no variation in the bandwidth, gain and increased aperture efficiency / Complete.

(D) Determine the full-width half-maximum (FWHM) and ringing metrics from the envelope of the time domain impulse response ($h_{rx/tx}(t, \phi, \theta)$) in receive or transmit mode / MAR–APR21 / Complete.

- Milestone: Produce a generalized code that calculates the impulse response envelope of the Koshelev antenna and plots the rate of change in FWHM and ringing values as a function of physical aperture size.

(E) Perform tradespace studies on design parameters such as feed position (*F*), length (*L*), and alpha (α). Obtain various antenna metrics data, compare, and analyze / MAR21/ Complete.

- Milestone: Identify Koshelev antenna design parameters that significantly alter the bandwidth, rE/V, peak gain over the desired bandwidth, and aperture efficiency.

(F) Reduce Koshelev antenna aperture size (H×W) to equal to or less than 90 mm × 90 mm, equal to that of the SOTA BAVA, for direct antenna metrics comparison / MAR–APR21 / Complete.

- Milestone: Provide a recommendation on the optimum design parameters and the resulting metrics, with comparison to SOTA BAVA. The optimized design parameters must yield 900 MHz ± 200 MHz bandwidth, rE/V greater than 1, peak gain around 3 dBi at 900 MHz, aperture efficiency equal to or greater than 130% at 900 MHz.

(G) Using the optimized model from (F), build various array simulation models/topologies to perform a tradespace study and report tradeoffs between array antenna metrics such as center element reflection coefficient (S11) value, gain vs theta at constant phi, physical aperture area, aperture efficiency, and rE/V / MAY–JULY21 / Complete.

- Milestone: Develop/showcase an optimized Koshelev array model that exceeds an aperture efficiency of 130% with a high rE/V.

(H) Perform literature search to investigate, understand, and determine the applicability of special electromagnetic (EM) techniques to the antennas under consideration. / JAN–APR21 / Complete.

(I) Explore impedance taper (microstrip based and coax based) designs that can interface well (both mechanically and electrically) to transition the signal from a coax cable to the input of the Koshelev antenna element / JULY21–AUG21 / Complete.

- Milestone: Recommend the optimum impedance taper design (with minimum reflections and maximum power transfer) with the optimum dimensions to successfully convert the high-voltage, short-rise time input signal from a coax cable to the feed of the Koshelev antenna array.

(J) Study response from optimized Koshelev antenna array when excited with different monopolar, differential, and bipolar pulse signals of significant interest / AUG21–NOV21 / Ongoing.

- Milestone: Provide a table comparing the Koshelev antenna array response metrics and narrow down the suitable pulse signals. Recommend (if any) changes to the downselected pulse signal(s) that can further improve the radiation efficiency, and/or transient gain.

(K) Investigate and analyze the response from the optimized Koshelev antenna array when excited by different excitation patterns / DEC 21 / Complete.

- Milestone: Compare and recommend an appropriate excitation method to yield maximum boresight gain, maximum half-power beamwidth (HPWB), minimum side lobe levels, and maximum electric field, rE/V.

(L) Prototype single element Koshelev antenna and test for reflection coefficient, gain as a function of frequency, radiated electric field at 1-m, 2.5-m, 5-m and 10-m (if feasible) distances. / AUG21–MAR22 / Ongoing.

- Milestone: Report measured data and recommend any improvements to the fabrication/prototyping/testing methods.

8.2.3 *Progress Made Since Last Report*

(L) During the sanding process for the Koshelev antenna prototype, the connection between the curve and the impedance transformer was broken. Since then, it has been reattached using an adhesive. A second set of tests using a digital multimeter was carried out to measure the sheet resistance of the Koshelev antenna and verify its conductivity.

8.2.4 *Technical Results*

(L) The conductivity of the silver paint on the Koshelev antenna was determined using two methods: a two-point digital multimeter (DMM) measurement and a 4-point probe method. For the DMM measurement, probes were placed ~3 mm apart to obtain the sheet resistance in Ω/square, which was multiplied by the thickness of the coat of paint to obtain resistivity. Table 8.2.1 shows the conductivity comparison between the two methods. The 4-point probe method has yielded slightly higher conductivity value than the DMM method. The repaired piece of the impedance transformer is shown in Fig. 8.2.1. The interface (highlighted) between the impedance transformer and the exponential flare of the Koshelev antenna has presented a manufacturing challenge in terms of structural rigidity.

Table 8.2.1. Comparison between the DMM and 4-point probe method to verify the conductivity of the silver paint directly on the Koshelev antenna.

Test Method	thickness (m)	Sheet Resistance (Ω/square)	Resistivity (Ω*m)	Conductivity (S/m)
DMM Sheet Resistance	0.00005	6.7	3.35E-04	2.985E+03
4-Point Probe	0.00005	N/A	2.79E-04	3.578E+03

Figure 8.2.1 Repaired Koshelev transformer connection.

8.2.5 *Summary of Significant Findings and Mission Impact*

(A) An extensive literature search on various UWB antenna elements has resulted in finding three promising options. The down-selected elements are the Koshelev, Shark, and Fractal antennas, which will be extensively studied using their individual design parameter space, which could result in physical aperture area reduction of the single antenna element. Later, the single antenna element will be converted into a planar array.

(B) Initial validation of the Koshelev antenna simulated using CST software agreed well with the antenna metrics published in the open literature [1]. A UWB bandwidth response (10:1 bandwidth) and rE/V > 1 has been observed from our initial simulations of the Koshelev antenna. This validation ensured that the Koshelev antenna can be subjected to further tradespace studies to understand its performance followed by optimizing the design according to OSPRES grant requirements.

(C) The initial tradespace study and analysis of the Koshelev antenna design yielded promising outputs to carry forward the investigation. A comparison of important antenna metrics between the Koshelev antenna in [1] and aperture reduced Koshelev antenna are shown in Table 5.2.1 of the APR 21 MSR.

(D) An in-house code has been developed to calculate important UWB time domain antenna metrics such as full-width half maximum (FWHM) and ringing. These metrics have been calculated using in-house MATLAB code using the excitation voltage and radiated electric field information obtained from CST simulations. FWHM and ringing antenna metrics help with assessing or characterizing an antenna's UWB response.

(E) The tradespace study of feed position provided a deeper understanding of how its position impacts the S11 value bandwidth. An optimum value for feed position i.e., $F = 1/20 < L < 1/10$ is recommended to achieve maximum bandwidth. The tradespace study of the antenna length (L) is straightforward. A longer antenna length will radiate better at lower frequencies. However, physical size restrictions/requirements must be kept in mind in determining the antenna length. Finally, a larger α value (>120°) is recommended to avoid unnecessary reflections from the electric monopole.

(F) From a thorough tradespace study, the aperture size of the Koshelev antenna (single element) is determined to be 90 mm × 100 mm in order to achieve desired antenna metrics performance proposed in the milestone. All metrics described in the milestone have been successfully achieved except the desired bandwidth (200 MHz on both sides) at 900 MHz center frequency. The bandwidth achieved is 900 ± 100 MHz.

(G) The physical aperture area of the Koshelev array antenna largely depends on the interelement spacing and the shape of the array. We were able to determine that the diamond topology is the optimum shape for the Koshelev array antenna. We were also able to obtain similar gain profile (peak gain and pattern) from making certain elements within the array passive (off state) when compared against regular active array (all elements in on state). From the non-symmetric interelement spacing values, we found that S_y has the least effect on the output; therefore a small spacing value can be chosen to reduce the physical aperture area of the Koshelev array.

(H) The literature search on the special EM techniques expanded our knowledge and opened the door to opportunities to apply some of those techniques to the antennas under study. EM techniques such as non-symmetric and non-square array topologies have been applied to the development and study of the Koshelev array antenna.

(I) The first impedance taper design under consideration has shown good S11 values (< -10 dB) over the frequency range of interest. In addition, we have shown that the shape of the pulse can be easily retained at the output of the taper with less than 5% amplitude losses.

(J) The Koshelev antenna array response from feeding a monopolar vs bipolar signal has demonstrated a clear winner: that is, a bipolar signal will radiate at least 10 times better than a monopolar signal. A comparison of the frequency spectrum of the radiated electric field from the optimized Koshelev antenna array between different monopolar pulse sources has identified the 'MI0731' pulse to be the optimum pulse.

(K) The uniform and Gaussian excitation patterns were determined to be the optimum excitation patterns. Selecting these excitation patterns would result in maximum electric field at boresight.

(L) Silver paint is shown to be the best conductive paint available for metallizing 3D printed antennas.

8.2.6 *References*

[1] Gubanov, V. P., et al. "Sources of high-power ultrawideband radiation pulses with a single antenna and a multielement array." *Instruments and Experimental Techniques* 48.3 (2005): 312-320.

8.3 Machine Learning Inspired Tradespace Analysis of UWB Antenna Arrays

(Sai Indharapu and Kalyan Durbhakula)

8.3.1 *Problem Statement, Approach, and Context*

Primary Problem: Determine the extent to which the physical aperture area of an antenna array, composed of antenna elements, can be reduced while maintaining performance in peak power density, bandwidth, and electronic beam steerability over the UHF range (0.4–1 GHz), compared with present-art high-power-microwave-capable antenna arrays.

Solution Space: Fractal antennas possess exceptional fidelity factor values (>0.9), which describe how well the shape of the input pulse is retained at an observation point in the far-field. Their high degree of freedom provides an opportunity to develop systematically modified patch shapes, which in turn leads to improved bandwidth while retaining high fidelity factor values. Machine learning (ML) can be leveraged to predict the antenna array response for an arbitrary design parameter space upon sufficient training and validation.

Sub-Problem:

(i) Fractal antennas generate omni-directional radiation patterns in the H-plane over the desired frequency range.

(ii) ML can suffer from underfitting or overfitting the training model which in turn leads to deviations in the predicted output.

State-of-the-Art (SOTA): Conventional full-wave EM solvers such as method of moments (MoM), multi-level fast multipole method (MLFMM), finite element method (FEM), and finite difference time domain (FDTD) method are currently being used to study, analyze and assess the performance of UWB antennas.

Deficiency in the SOTA: UWB antenna optimization using conventional EM solvers utilizes significant computational time and memory resource.

Solution Proposed:

(i) Design, simulate, validate, and perform a tradespace study on the design parameter space of the selected fractal antenna element using commercially available electromagnetic (EM) wave solvers.

(ii) Train, validate, test and compare multiple ML models for quicker and accurate prediction of antenna array response for different physical aperture areas.

Relevance to OSPRES Grant Objective: The fractal antenna achieves an UWB response, a mandatory requirement of the OSPRES grant objective, in a small volume footprint and similar physical aperture area when compared against the SOTA BAVA, dual ridge horn antennas etc. Furthermore, the microstrip-design-based fractal antenna can efficiently handle electronic steering by integrating the feed network on the same board. This eliminates the need to build a separate feed network external to the fractal antenna using bulky coaxial cables.

Risks, Payoffs, and Challenges:

(i) A majority of the fractal antenna geometries yield an omni-directional pattern in the H-plane, which can be a risk. However, efforts are underway to mitigate this pattern without deteriorating bandwidth.

(ii) Payoffs include developing a library of antenna metrics data for various fractal shapes and sizes.

(iii) Design challenges and numerical calculations with respect to specific fractal shapes could arise after performing a certain number of iterations to further improve the bandwidth.

(iv) Fractal antennas were known to generate gain loss at random frequencies over their operating frequencies. Achieving gain stability over the desired frequency range can be a significant challenge.

8.3.2 *Tasks and Milestones / Timeline / Status*

(A) Perform tradespace analysis of the fractal element radius *b* over the desired frequency range (4 to 12 GHz) using the genetic algorithm (GA) optimization tool available in the commercial electromagnetic (EM) solver FEKO / FEB21 / Complete.

- Milestone: Provide a recommendation of an optimum value of *b* using OPTFEKO to minimize reflection coefficient or S11 (< –10 dB).

(B) Perform tradespace study on different fractal shapes by changing the number of fractal segments to understand the effect of this change on the impedance bandwidth / FEB21 / Complete.

- Milestone: Produce a detailed study of the antenna response such as S11, gain, and bandwidth by varying the number fractal segments.

(C) Apply the GA optimization tool on the fractal side length *b* over a wide frequency range (2 to 12 GHz with 201 discrete frequency points) and number of fractal segments using OPTFEKO on the LEWIS cluster / MAR21 / Complete.

- Milestone: Reduce physical aperture area by 10% of its present design, reported in the FEB MSR, and demonstrate minimal or no change in S11, gain, and fidelity factor values.

(D) Perform a parametric study and analysis of antenna response by varying hexagon radius, *a* / MAR–APR21 / Complete.

- Milestone: Recommend a value of *a* to reduce the physical aperture area and increase aperture efficiency (>50%) with no variation in other antenna metrics.

(E) Frequency scale fractal antenna design such that the center frequency of the resulting antenna equals 1.3 GHz / MAY21 / Complete.

- Milestone: Modify antenna design with a center frequency equal to 1.3 GHz and achieve similar results (3:1 bandwidth at fc = 1.3 GHz, 3 dBi gain and >130% aperture efficiency at 900 MHz) to antenna design at center frequency ~7 GHz.

(F) Design and simulate various array antenna geometries composed of optimized fractal antenna elements (obtained from (E)) to analyze the effect of overall array antenna geometry on the desired array antenna response metrics (i.e., gain vs. frequency, gain vs. elevation angle at constant phi, rE/V, half-power beamwidth and side-lobe level.) / MAY–JUL21 / Complete

- Milestone: Recommend a best possible structure with reduced aperture area and minimal loss in gain.

(G) Apply ML models available in Altair Hyperstudy (2021) on the fractal antenna to try and understand the possibilities and limitations of ML models for fast and efficient antenna metrics prediction and optimization. Expand the prediction capability to time-domain electric field and antenna pattern using ML models (k-nearest neighbor and linear regression) available in scikit learn on Python programming tool “Anaconda”. / MAY21–FEB22 / Complete.

- Milestone: Recommend most accurate and efficient ML model for a fractal antenna in time-domain and frequency domain.

(H) Apply ML models on the octagon fractal antenna array lattice to extend the prediction capability beyond single element. / SEP21–MAY22 / Ongoing.

- Milestone: Recommend the best suitable ML model implemented/developed using Python programming language for array antenna metrics prediction.

(I) Develop a graphical user interface (GUI) to ease the process of employing ML models to predict the antenna output response.

- Milestone: Incorporate the developed automated data extraction scripts, ML scripts to the GUI to enable user to predict antenna response with shorter time. / FEB22-JULY22 / Ongoing

8.3.3 *Progress Made Since Last Report*

(H) A new study is being carried out to further reduce the computational time required to calculate antenna array metrics. As described in the previous MSR, the radiation

pattern of larger arrays using the radiation pattern of smaller sub-arrays the active element pattern (AEP) method is being investigated.

(I)The GUI is updated with the ability to take the user input in real-time and predict the antenna output response. In the case of the fractal antenna, four input design parameters were added with user entry fields to the GUI validation window. To make the process of ML validation easy and to enhance the GUI, the predicted output can be visualized in the GUI itself. The block diagram in Fig. 8.3.1 illustrates the steps involved in employing ML models for antenna response prediction using an in-house build GUI. The new validation window is illustrated in Fig. 8.3.1

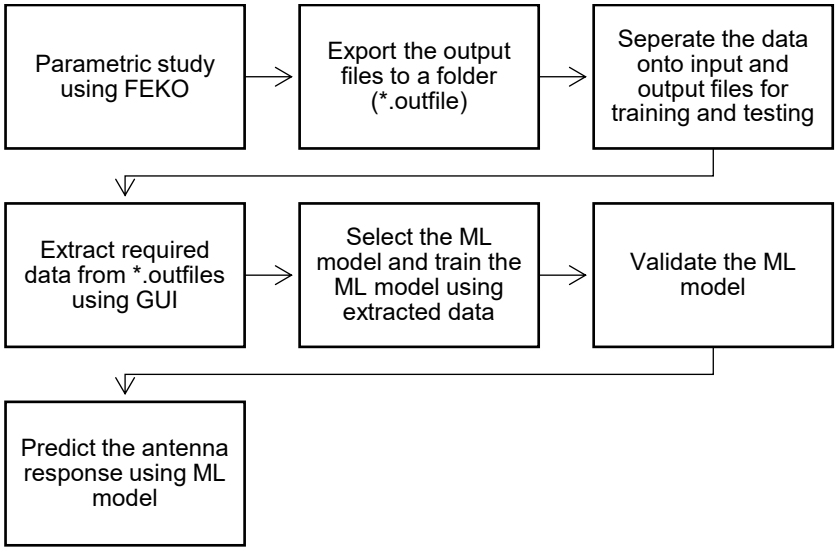


Figure 8.3.1. Block diagram showing steps involved in employing ML models for antenna output predictions.

8.3.4 *Technical Results*

(H) From the literature [2], the AEPs of the interior elements of a larger planar array can be assumed to be identical and approximated by the central element of a square array. Further, this method has the ability to reduce the time for output response calculation but the interelement spacing between the elements of an antenna array needs to be very large. Fig. 8.3.2 demonstrates the procedure involved in the AEPs method. A larger array (6x7 elements) can be constructed using a smaller array (5x5).

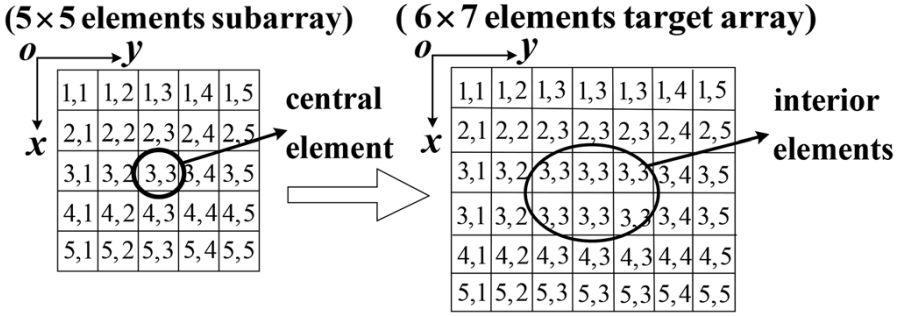


Fig. 8.3.2. Subarray of 5x5 elements is used to construct a 6x7 element array.

Following are the limitations involved in the AEP method:

1. In the case of the AEP method, the mutual coupling between elements is ignored and forced to be zero only when inter-element spacing is larger than 2 x d_x and 2 x d_y (d_x and d_y are the distance between elements in x and y directions) which results in the formation of an uniform array.
2. To achieve accuracy the smaller array size is increased.
3. Only applicable for square antenna geometry.

(I) The following steps are followed to use GUI for extracting training data for antenna output response prediction:

1. Start the process by loading the training input data using “Load inpud data” button.
2. In the next step, select the flder contating the *.outfiles using “Load training output data” button.
3. Finally, Load the test output data using “Load test output data” button.

Futher, steps below are followed for training and validating the trained ML model:

4. Select the ML model from the drop down list and train the model using “Train the model” button.
5. “Validate” button is used to open the validation window.

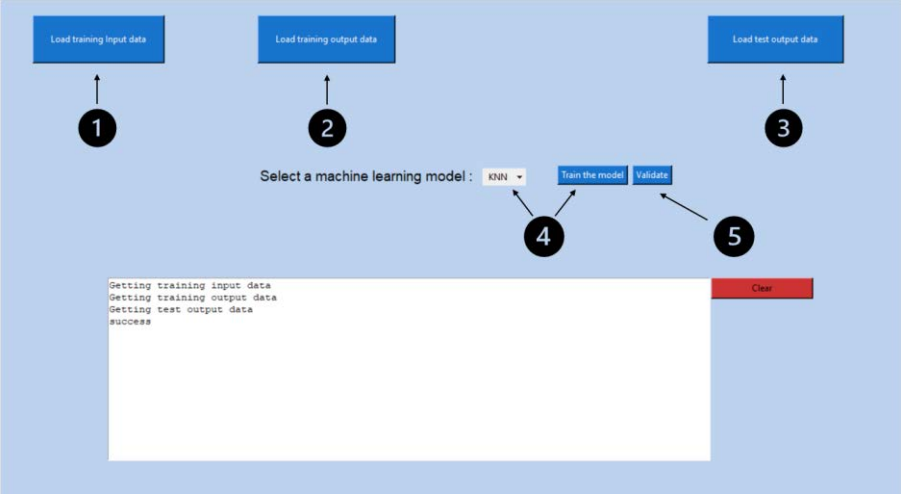


Fig. 8.3.3 Snapshot of the setup window in the GUI.

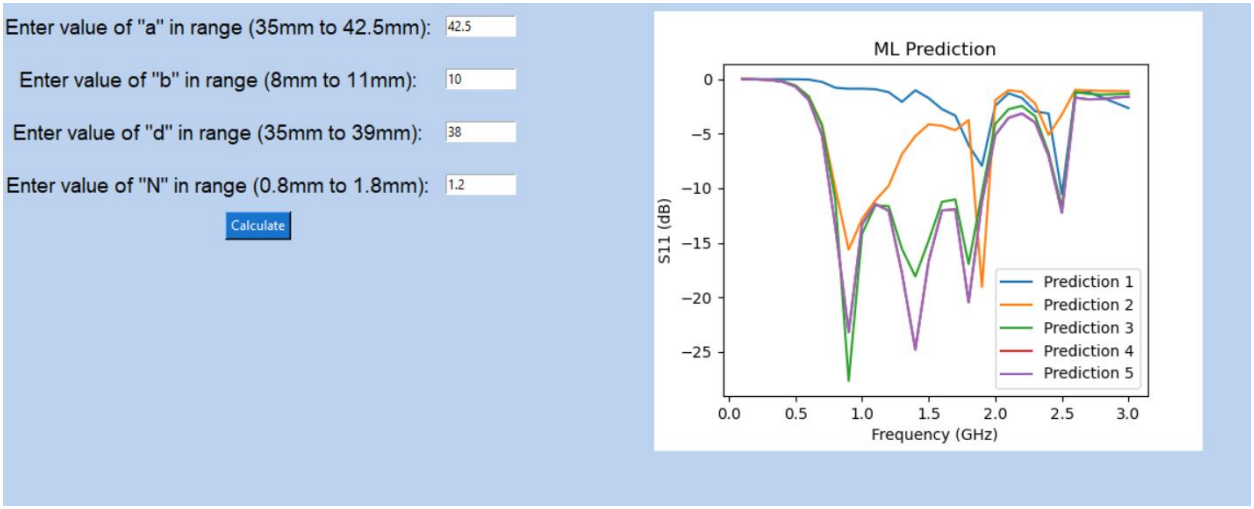
Following the steps shown in Fig. 8.3.3, the KNN model is trained and validated. With the entry fields added to the validation window, new values are entered for each of the design variables within the range of interest. Upon clicking the calculate button the selected ML model in the backend will predict the antenna response for the user input and the plot is added to the window. The complete process of prediction and plotting is done within few seconds of time.

The developed GUI is used to employ the KNN algorithm to predict S11 and Gain consecutively. Five different combinations of ‘a’ and ‘b’ as shown in the Table 8.3.1 are used as input for testing.

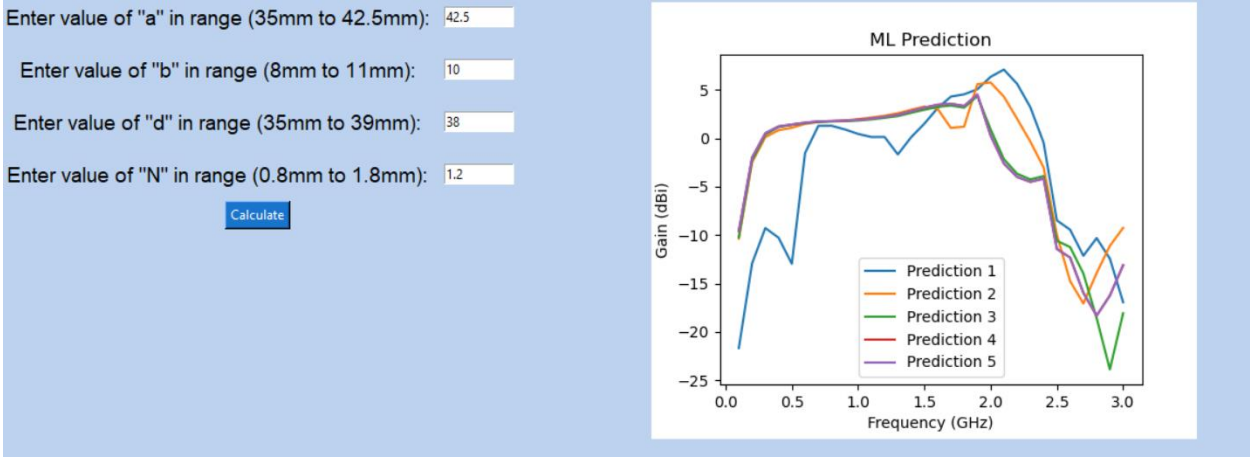
Table 8.3.1: Input parameters and their values

Data set	'a'	'b'	'd'	'N'
Prediction-1	36	8.5	38	1.2
Prediction-2	39	9	38	1.2
Prediction-3	38	9.2	38	1.2
Prediction-4	40.5	9.7	38	1.2
Prediction-5	42.5	10	38	1.2

Test inputs shown in Table 8.3.1 are entered to predict S11 and Gain. The predicted response for each user input is plotted in a single plot as shown in Fig. 8.3.4. The complete process of training data extraction, ML model training and parametric analysis is carried out using the GUI. Following the same process, a parametric study of any antenna model can be carried out.



(a)



(b)

Fig. 8.3.4 (a) S11 and (b) Gain response prediction using the GUI.

The bandwidth and gain comparison values of each ML prediction are shown in Table 8.3.2. Any input values for the selected input can be passed using the entry fields to study the output response of an antenna. Irrespective of antenna response from the ML model this example demonstrates the viability of using the GUI for faster antenna tradespace analysis

Table 8.3.2: Antenna metrics

Data set	Bandwidth Ratio	Bandwidth	Gain (dBi) at 1.55 GHz
Prediction 1	*N/A* F_l = 0 GHz, F_h = 0 GHz	N/A	3.10
Prediction 2	*1.8:1* F_l = 0.7 GHz, F_h = 1.3 GHz	600 MHz	3.03
Prediction 3	*2.57:1* F_l = 0.7 GHz, F_h = 1.8 GHz	1100 MHz	3.23
Prediction 4	*2.79:1* F_l = 0.68 GHz, F_h = 1.9 GHz	1220 MHz	3.45
Prediction 5	*2.79:1* F_l = 0.68 GHz, F_h = 1.9 GHz	1220 MHz	3.45

A result that can help identify the optimal set of design parameters is shown in Fig. 8.3.5. Fig. 8.3.5 shows the bandwidth and gain (at the center frequency) predicted by the KNN model for five different test data sets. The target is to create an antenna design that achieves UWB response with the highest gain possible. In Fig. 8.3.5, the prediction from the KNN model determines P-4 or P-5 test data sets as optimal solutions. In this case, two objectives (S11 < -10 dB and gain as high as possible) have been used. We are currently adding new antenna metrics, an option to predict array response, and a feature to include optimization.

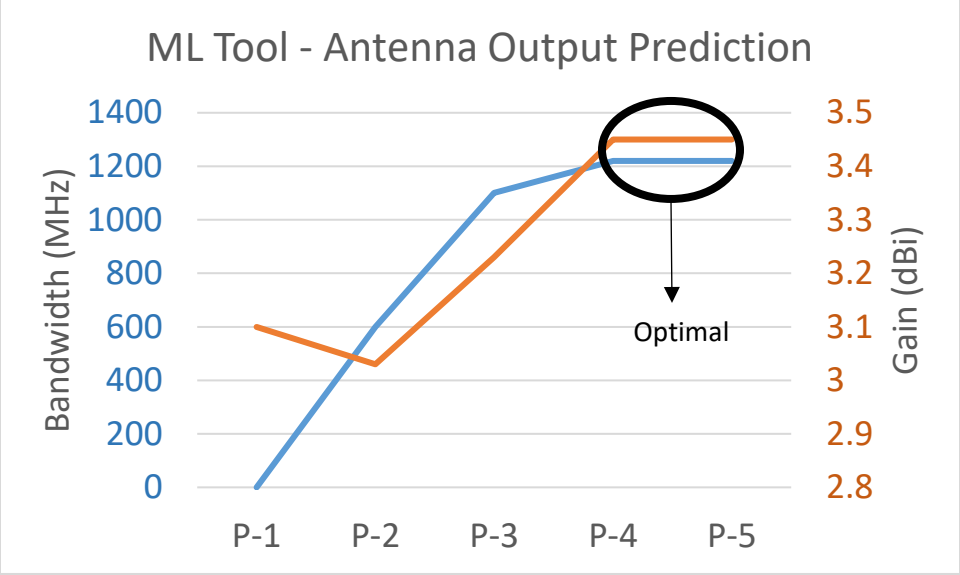


Fig. 8.3.5. The bandwidth and gain (at center frequency) predicted by the KNN model for five different test data sets.

8.3.5 *Summary of Significant Findings and Mission Impact*

(A) The initial analysis of the simulation results with fractal radius *b* equal to 1.8 mm yielded multiple resonant frequencies with enhanced bandwidth. To further increase the bandwidth, OPTFEKO has been used as an optimization tool with fractal radius *b* as the optimization variable. The optimum value for *b* is found to be 1.66 mm. A comparison between reflection coefficient for initial *b* (= 1.8 mm) value and the optimized *b* (= 1.66 mm) can be found in Figure. 6.4.6. The optimization is carried out over 51 discrete frequency points.

(B) The addition of fractal elements (*N*) to the simple hexagon improved antenna metrics such as S11. To further investigate and understand the fractal elements, the number of segments in the fractal geometry has been varied. The improvement in bandwidth is observed as the value of *N* is increased from 6 to 14.

(C) The initial optimum value of *b* over 51 discrete frequency points is reported as 1.66 mm in task (A). To further increase the accuracy of the optimization algorithm and to find a more precise value for *b*, optimization is further performed over wider frequency points (201 discrete points between 2 GHz to 12 GHz) which yielded the optimum value of b as 1.368 mm. The S11 response of antenna design with newly found *b*

(i.e., 1.368 mm) hasn't produced any better bandwidth with respect to *b* (= 1.66 mm). Thus, *b* is set to be 1.66 mm for further research.

(D) The hexagonal patch radius *a* has a significant effect on the physical aperture area of the antenna. Therefore, Altair OPTFEKO has been utilized to find an optimum *a* value, which was found to be 8 mm over the range 7.2 to 9 mm. Antenna metrics such as S11, gain, and bandwidth have shown desired performance with the optimized *a* value.

(E) The initial antenna design has been modified to achieve a center frequency of ~1.3 GHz. The gain value at 900 MHz is 3.5 dBi and, with the modified antenna design, we were able to achieve an impedance bandwidth ratio of 3.3:1. The designed antenna has been fabricated and tested, and the S11 response of the fabricated antenna agrees well when compared against FEKO, CST.

(F) To summarize, four different fractal antenna array geometries (i.e., square, diamond, hexagon, and octagon) have been designed and simulated. Upon comparing antenna array metrics, octagonal fractal antenna array has yielded minimal sidelobe levels with a gain of 15.7 dBi at 900 MHz close to that of square geometry with 32.27% lower physical aperture area than that of square geometry. The octagonal fractal antenna array has been chosen as the optimum geometry with reduced aperture area and reduced side lobes while retaining the bandwidth and gain milestone metrics.

(G) Radial basis function (RBF) and least square regression (LSR) were down selected from the initial three ML models based upon their generalization capability for prediction of reflection coefficient (S11), gain, and electric field. Further analysis of increasing training data set size has shown no improvement in prediction accuracy. Trained ML models were tested for design variable values outside the training range. The resulting RMSE increased as the values drifted away from the mid-point of the training range. RBF performed well in the prediction of S11, while LSR performed slightly better for gain and electric field predictions. In addition, for time-domain electric field prediction, we recommend using k-nearest neighbors (kNN) ML algorithm for accurate prediction.

(H) Initial application of kNN ML model for the prediction of antenna array bandwidth response of center and corner element yielded positive results with a good agreement between traditional EM solver (FEKO) and trained kNN ML model. The new LR ML model yielded improved RMSE values (over kNN) in its prediction of reflection coefficient and gain for the optimized octagon fractal antenna array.

(I) A GUI is currently under development, which accepts training data for an antenna (single-element or array) of user choice and can predict output response (S11 and gain) for a range of test data within a few seconds. The GUI can significantly help users with carrying out the Tradespace study in a short time. Therefore, users can build/prototype the desired antenna design quickly.

8.3.6 *References*

[1] H. Fallahi and Z. Atlasbaf, "Study of a Class of UWB CPW-Fed Monopole Antenna With Fractal Elements," in IEEE Antennas and Wireless Propagation Letters, vol. 12, pp. 1484-1487, 2013, doi: 10.1109/LAWP.2013.2289868.

[2] S. Zhang, X. Wang and L. Chang, "Radiation Pattern of Large Planar Arrays Using Four Small Subarrays," in IEEE Antennas and Wireless Propagation Letters, vol. 14, pp. 1196-1199, 2015, doi: 10.1109/LAWP.2015.2397600.

9 Feedback

There is no feedback to report for the current reporting period.

10 Program Management

10.1 Issues

i. Scope – No issues
ii. Budget – 12-month NCTE submitted/pending
iii. Schedule – No issues

10.2 Interactions with Others

Agency/Org	Performer	Project Name	Purpose of Research/ Collaboration

10.3 Major Procurement Actions

10.4 Travel

Destination	Purpose	Attendees	Estimated Costs

10.5 Pending or Upcoming Public Release Requests

11 Appendix A: Academic and IP Output

11.1 Students Graduated

Name	Degree	Currently
Al-Shaikhli, Waleed Azad, Wasekul	MS Spring 19 PhD Summer 21	Kansas City National Security Campus, Honeywell Applied Materials, Sunnyvale, CA
Berg, Jordan	MS Spring 21	MRI Global
Bissen, Bear	MS Spring 19	Kansas City National Security Campus, Honeywell
Floyd, Dennis	BS	Naval Air Warfare Center Weapons Division
Hanif, Abu	PhD Spring 21	UMKC/MIDE (Postdoc)
Harmon, Aaron	BS	Missouri University of Science & Technology
Harp, Joshua	MS	UMKC/MIDE (Senior Engineer)
Hauptman, Cash	BS Spring 18	University of Nebraska-Lincoln
Klappa, Paul	MS Spring 21	
Labrada, Dario	BS Spring 20	Honeywell Aerospace, Florida
Lancaster, John	MS Spring 17	Lawrence Livermore National Laboratory
Renzelman, Jeff	MS Spring 18	Kansas City National Security Campus, Honeywell
Roy, Sourov	PhD Spring21	
Wagner, Adam	MS Fall 20	Kansas City National Security Campus, Honeywell
Xia, Shengxuan	BS	Missouri University of Science & Technology

11.2 Journal Publications

11.2.1 *In Preparation*

[1] N. Gardner, K. C. Durbhakula, and A. N. Caruso, “UHF and L-Band Frequency Generation at MW Peak Power using Diode-based Nonlinear Transmission Lines as Pulse Forming Networks,” *Transactions on Plasma Science*, In Preparation, **2021**.

[2] N. Gardner, K. C. Durbhakula, and A. N. Caruso, “Electrically Tunable Diode-based Nonlinear Transmission Line,” *TBD*, In Preparation, **2021**.

[3] N. Gardner, A. N. Caruso, K. C. Durbhakula and P. Doynov, “Diode-Based Non-Linear Transmission Line Design Considerations,” *Journal of Applied Physics*, In Preparation, **2021**.

[4] B. Barman, D. Chatterjee, K. C. Durbhakula, and A. N. Caruso, “Tradespace Analysis of Wideband, Electrically Small Microstrip Patch Antenna Elements for Phased Array Applications,” *IEEE Antennas and Propagation Magazine,* In preparation, **2021**.

[5] S. Xia, J. Hunter, A. Harmon, M. Hamdalla, A. Hassan, V. Khilkevich, D. Beetner, “Simulation Driven Statistical Analysis of the Electro-magnetic Coupling to Microstriplines,” *IEEE Transactions on Electromagnetic Compatibility*, In Preparation, **2020**.

[6] M. Hamdalla, V. Khilkevich, D. G. Beetner, A. N. Caruso, A. M. Hassan, "Characteristic Mode Analysis Justification of the Stochastic Electromagnetic Field Coupling to Randomly Shaped Wires," *IEEE Transactions on Electromagnetic Compatibility*, In Preparation, **2020**.

11.2.2 *Submitted / Under Revision*

[7] B. Barman, K. C. Durbhakula, D. Chatterjee, and A. N. Caruso, "Comparison of Machine Learning Algorithms for Bandwidth Enhancement of a Coaxial Probe-fed Microstrip Patch Antenna," *Applied Computational Electromagnetics Society (ACES)*, Submitted, **2021**.

[8] B. K. Lau, M. Capek, and A. M. Hassan, "Characteristic Modes–Progress, Overview, and Future Perspectives," *IEEE Antennas and Propagation Magazine*, Submitted, **2021**.

[9] K. Alsultan, M. Z. M. Hamdalla, S. Dey, P. Rao, and A. M. Hassan, "Scalable and Fast Characteristic Mode Analysis Implementation Using a Hybrid CPU/GPU Platform," *ACES*, Submitted, **2021**.

[10] M. Z. M. Hamdalla, B. Bissen, J. Hunter, L. Yuanzhuo, V. Khilkevich, D. G. Beetner, A. N. Caruso, and A. M. Hassan, "Prediction of Experimental Electromagnetic Coupling to a UAV Model Using Characteristic Mode Analysis," *IEEE Access*, Submitted, **2021**.

[11] W. Azad, F. Khan, and A. N. Caruso, "A Scalable Multilevel-Modular 10 kV Silicon Carbide MOSFET Module Featuring Custom Isolated Gate Driver Circuit Combined with Coupling and Snubber Circuits," *IEEE Transactions on Power Electronics*, Submitted, **2021.**

[12] John Keerthi Paul Bhamidipati, Eliot R. Myers, Adam M. Conway, Lars F. Voss, and Anthony N. Caruso, "Figure of Merit Development for Linear-Mode Photoconductive Solid-State Switches," *IEEE Transactions on Electronic Devices*, Under Revision, **2020**.

11.2.3 *Published / In Press*

[13] M. Z. M. Hamdalla, B. Bissen, J. Hunter, Y. Liu, V. Khilkevich, D. G. Beetner, A. N. Caruso, and A. M. Hassan, "Prediction of Experimental Electromagnetic Coupling to a UAV Model Using Characteristic Mode Analysis," *IEEE Access*, In Press, **2021**.

[14] J. N. Berg, R. C. Allen, and S. Sobhansarbandi. "A Novel Method of Cooling a Semiconductor Device through a Jet Impingement Thermal Management System: CFD Modeling and Experimental Evaluation." *International Journal of Thermal Sciences*, 172, 107254, **Feb 2022** [doi].

[15] W. Azad, F. Khan, and A. N. Caruso, "A Medium Power, Self-Sustaining, Configurable RF Pulse Generation Circuit Using a Nonlinear Transmission Line and Power Amplifier in a Closed Loop Configuration, *IEEE Transactions on Plasma Science*, vol. 49, no. 7, pp. 2183–2194, **July 2021** [doi].

[16] S. Roy, W. Azad, S. Baidya and F. Khan, “A Comprehensive Review on Rectifiers, Linear Regulators and Switched-Mode Power Processing Techniques for Biomedical Sensors and Implants utilizing In-body Energy Harvesting and External Power Delivery,” *IEEE Transactions on Power Electronics*, vol. 36, no. 11, pp. 12721–12745, **Nov 2021** [doi].

[17] K. C. Durbhakula, D. Chatterjee, and A. M. Hassan, “An Efficient Algorithm for Locating TE and TM Poles for a Class of Multiscale Inhomogeneous Media Problems,” *IEEE Journal on Multiscale and Multiphysics Computational Techniques*, vol. 4, no. 1, pp. 364–373, **2019** [doi].

11.3 Conference Publications

11.3.1 *Submitted / Accepted*

[1] B. Barman, D. Chatterjee, and A. N. Caruso, "On the Optimum Substrate Selection in Wideband Microstrip Patch Antenna Design," *2022 IEEE International Symposium on Antennas & Propagation & USNC-URSI Radio Science Meeting, Denver, Colorado, USA,* July 10-15, pp. 1-2. (Submitted)

[2] B. Barman, D. Chatterjee, and A. N. Caruso, "Time Domain Analysis of an UWB Electrically Small Microstrip Patch Antenna," *2022 IEEE International Symposium on Antennas & Propagation & USNC-URSI Radio Science Meeting, Denver, Colorado, USA,* July 10-15, pp. 1-2. (Submitted)

[3] S. R. Shepard and H. A. Thompson, “Self-focusing in Guided and Un-guided Media,” submitted to the *2021 OSA Nonlinear Optics Topical Meeting, Virtual Event*, August 9-13, 2021.

11.3.2 *Presented*

[4] B. Barman, D. Chatterjee and A. N. Caruso, "Probe-location Optimization in a Wideband Microstrip Patch Antenna using Genetic Algorithm, Particle Swarm and Nelder-Mead Optimization Methods," *2021 International Applied Computational Electromagnetics Society Symposium (ACES)*, 2021, pp. 1-3 [doi].

[5] W. Azad, S. Roy, and F. Khan, "A Single Gate Driver-based Four-stage High-voltage SiC Switch Having Dynamic Voltage Balancing Capability," *2021 IEEE Applied Power Electronics Conference and Exposition* (APEC), Phoenix, AZ, USA, June 9-12, 2021.

[6] W. Azad, S. Roy, F. Khan and A. N. Caruso, "A Multilevel-Modular 10 kV Silicon Carbide MOSFET Module using Custom High-Voltage Isolated Gate Driver, Coupling, and Snubber Circuits," *2021 IEEE Kansas Power and Energy Conference* (KPEC), Manhattan, KS, USA, April 19-20, 2021 [doi].

[7] T. Layman, T. D. Fields, and O. A. Yakimenko, “Evaluation of Proportional Navigation for Multirotor Pursuit,” AIAA SciTech Forum, Virtual Event, January 11-21, 2021 [doi].

[8] P. J. Klappa, and T. D. Fields, “Assessment of Fixed-Wing UAV System Identification Models during Actuator and Payload Drop Failures,” AIAA Atmospheric Flight Mechanics Conference, Virtual Event, January 11-21, 2021 [doi].

[9] J. Hunter, S. Xia, A. Harmon, A. M. Hassan, V. Khilkevich, and D. Beetner, “Modeling and Statistical Characterization of Electromagnetic Coupling to Electronic Devices,” *IEEE International Symposium on Antennas and Propagation and NSRM USNC-URSI National Radio Science Meeting*, Boulder, CO, January 4-9, 2021 [doi].

[10] B. Barman, K. C. Durbhakula, B. Bissen, D. Chatterjee, and A. N. Caruso, “Performance Optimization of a Microstrip Patch Antenna using Characteristic Mode and D/Q Analysis,” *2020 XXXIIIrd General Assembly and Scientific Symposium of the International Union of Radio Science*, Rome, Italy (online conference), Aug 29-Sept 5, 2020, pp. 1-4 [doi].

[11] J. Berg, and S. Sobhansarbandi. “CFD Modeling of Thermal Management Systems for a Silicon Semiconductor Switch.” *ASME 2020 Heat Transfer Summer Conference collocated with the ASME 2020 Fluids Engineering Division Summer Meeting and the ASME 2020 18th International Conference on Nanochannels, Microchannels, and Minichannels*, Virtual, July 13–15, 2020, American Society of Mechanical Engineers Digital Collection [doi].

[12] B. Barman, D. Chatterjee, and A. N. Caruso, “Performance Optimization of Electrically Small Microstrip Patch Antennas on Finite Ground Planes,” 2020 *IEEE International Symposium on Antennas and Propagation and North American Radio Science Meeting*, Montreal, Quebec, Canada, July 5-10, 2020, pp. 1–2 (online conference) [doi].

[13] M. Hamdalla, B. Bissen, A. N. Caruso, and A. M. Hassan, “Experimental Validations of Characteristic Mode Analysis Predictions Using GTEM Measurements,” *IEEE International Symposium on Antennas and Propagation and USNC-URSI Radio Science Meeting,* Montréal, Québec, Canada, July 5-10, 2020 [doi].

[14] K. Alsultan, P. Rao, A. N. Caruso, and A. M. Hassan, “Scalable Characteristic Mode Analysis: Requirements and Challenges (White Paper),” *Large Scale Networking (LSN) Workshop on Huge Data: A Computing, Networking and Distributed Systems Perspective Sponsored by NSF*, Chicago, IL, April 13-14, 2020.

[15] M. Hamdalla, A. N. Caruso, and A. M. Hassan, “Predicting Electromagnetic Interference to a Terminated Wire Using Characteristic Mode Analysis,” *Proceedings of the Annual Review of Progress in Applied Computational Electromagnetics (ACES)*, Monterey, CA, March 22-26, 2020. [doi]

[16] W. Azad, F. Khan, and A. Caruso, "Self-sustaining High-power RF Signal Generation Using LDMOS Based Power Amplifier and Nonlinear Transmission Line," *2020 IEEE Applied Power Electronics Conference and Exposition (APEC)*, New Orleans, LA, USA, March 15-19 2020, pp. 3567-3572 [doi].

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Conference and Exposition (APEC), New Orleans, LA, USA, March 15-19 2020, pp. 345-350 [doi].

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[20] M. Hamdalla, A. N. Caruso, and A. M. Hassan, "Characteristic Mode Analysis of the Effect of the UAV Frame Material on Coupling and Interference," *IEEE International Symposium on Antennas and Propagation and USNC-URSI Radio Science Meeting at Atlanta (2 pages)*, Georgia, USA, July 7-12, 2019 [doi].

[21] M. Hamdalla, J. Hunter, Y. Liu, V. Khilkevich, D. Beetner, A. Caruso, and A. M. Hassan, "Electromagnetic Interference of Unmanned Aerial Vehicles: A Characteristic Mode Analysis Approach," *IEEE International Symposium on Antennas and Propagation and USNC-URSI Radio Science Meeting at Atlanta (2 pages)*, Georgia, USA, July 7-12, 2019 [doi].

[22] K. C. Durbhakula, J. Lancaster, A. M. Hassan, D. Chatterjee, A. N. Caruso, J. D. Hunter, Y. Liu, D. Beetner, and V. Khilkevich, "Electromagnetic Coupling Analysis of Printed Circuit Board Traces using Characteristic Mode Analysis," *IEEE International Symposium on Antennas and Propagation and USNC-URSI Radio Science Meeting (2 pages)*, Atlanta, Georgia, USA, July 7-12 2019 [doi].

[23] K. C. Durbhakula, D. Chatterjee, and A. M. Hassan, “On the Location of Transverse Electric Surface Wave Poles for Electrically Thick Substrates,” Proceedings of the *IEEE Antennas and Propagation International Symposium and National Radio Science Meeting*, Atlanta, Georgia, USA, July 7-12, 2019 [doi].

[24] W. Azad and F. Khan, “Sustaining High-power RF Signal Generation in a Positive Feedback Network," *2019 IEEE Pulsed Power and Plasma Science Conference (PPPS)*, Orlando, FL, USA, June 23-28 2019.

[25] K. Alsultan, P. Rao, A. N. Caruso, and A. M. Hassan, “Scalable characteristic mode analysis using big data techniques,” *International Symposium on Electromagnetic Theory (EMTS 2019)*, San Diego, CA, USA, May 27-31, 2019.

[26] M. Hamdalla, W. Al-Shaikhli, J. Lancaster, J. D. Hunter, L. Yuanzhuo, V. Khilkevich, D. G. Beetner, A. N. Caruso, and A. M. Hassan, “Characteristic Mode Analysis of Electromagnetic Coupling to Wires with Realistic Shapes,” *International Symposium on Electromagnetic Theory (EMTS 2019)*, San Diego, CA, USA, May 27-31, 2019.

[27] K. C. Durbhakula, D. Chatterjee, and A. M. Hassan, “Location of Surface Wave Poles in Sommerfeld Integrals: A Mittag-Leffler Expansion Approach,” *Proceedings of the URSI-B International Symposium on Electromagnetic Theory*, URSI Commission, San Diego, USA, May 2019 [doi].

[28] K. C. Durbhakula, D. Chatterjee and A. M. Hassan, “Analytical Evaluation of Sommerfeld Integral Tails Present in Two-layered Media Green’s Functions,” *Proceedings of the Indian Conference on Antennas and Propagation* (InCAP), Hyderabad, India, December 2018 [doi].

[29] D. Beetner, V. Khilkevich, A. M. Hassan, J. Hunter, Y. Liu, and D. Floyd, *“*Characterization of the Electromagnetic Coupling to UAVs,*”* *DE Systems Symposium*, September 24-27, 2018

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[31] M. Hamdalla, J. Roacho-Valles, J. Hunter, D. Beetner, A. M. Hassan, and A. N. Caruso, “Electromagnetic Analysis of Unmanned Aerial Vehicles Using Characteristic Mode Analysis,” *Proceedings of the AMEREM 2018 Conference*, Santa Barbra, CA, Aug 27-31, 2018.

[32] C. Hartshorn, M. Hamdalla, J. Lancaster, A. M. Hassan, and A. N. Caruso, “Electromagnetic Vulnerability of Wires with Arbitrary Shape,” *Proceedings of the AMEREM 2018 Conference*, Santa Barbra, CA, Aug 27-31, 2018.

[33] K. C. Durbhakula, D. Chatterjee, A. M. Hassan, and M. S. Kluskens, “Studies on Numerical Evaluation of Sommerfeld Integrals for Multilayer Topologies,” *IEEE Antennas and Propagation International Symposium and National Radio Science Meeting*, Boston, Mass., USA, July 7-12, 2018.

[34] J. Lancaster, D. Chatterjee, and A. N. Caruso, “Some Investigations into the Dispersion Characteristics of Localized Bessel Beams,” published in the *IEEE Antennas and Propagation International Symposium and National Radio Science Meeting*, Boston, Mass., USA, July 7-12, 2018 (1 page URSI Abstract).

[35] M. Hamdalla, A. M. Hassan, and A. N. Caruso “Characteristic Mode Analysis of Unmanned Aerial Vehicles with Realistic Shapes and Material Composition,” *IEEE International Symposium on Antennas and Propagation and USNC-URSI Radio Science Meeting,* Boston, MA, July 8-13, 2018.

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[37] J. Hunter, Y. Liu, D. Floyd, A. Hassan, V. Khilkevich, and D. Beetner, “Characterization of the Electromagnetic Coupling to UAVs,” *Annual Directed Energy Science and Technology Symposium*, Feb 26-March 2, 2018.

11.4 Conference Presentations

11.4.1 *Submitted / Accepted*

[1] S. Bellinger, A. Caruso, A. Usenko, “Stacked Diodes for Pulsed Power Applications,” GOMACTech-22, Miami, FL, March 21–24 2022 (submitted, oral).

[2] S. Bellinger, A. Caruso, A. Usenko, “New Paradigm on Making Semiconductor Opening Switches for Pulsed Power,” 2021 23rd IEEE Pulsed Power Conference, Denver, CO, Dec. 12–16, 2021 (accepted, oral).

Directed Energy Professional Society, Directed Energy Systems Symposium, Washington DC, October 25-29 2021 (submitted):

[3] B. Barman, D. Chatterjee, A. Caruso, and K. Durbhakula, “Tradespace Analysis of a Phased Array of Microstrip Patch Electrically Small Antennas (ESAs)” (Poster)

[4] J. N. Berg, R. C. Allen, and S. Sobhansarbandi, “A Novel Method of Cooling a Semiconductor Device through a Jet Impingement Thermal Management System: CFD Modeling and Experimental Evaluation” (Poster)

[5] J. N. Berg, R. C. Allen, and S. Sobhansarbandi, “Heat Transfer Enhancement of a Jet Impingement Thermal Management System: A Comparison of Various Nanofluid Mixtures” (Poster)

[6] J. Bhamidipati, M. Paquette, R. Allen, and A. Caruso, “Photoconductive Semiconductor Switch Enabled Multi-Stage Optical Source Driver” (Poster)

[7] G. Bhattarai, J. Eifler, S. Roy, M. Hyde, J. Bhamidipati, A. Usenko, M. Pederson, M. Paquette, A. Caruso, S. Bellinger, L. Voss, and R. Allen, “All Solid-State High-Power Pulse Sharpeners” (Poster)

[8] S. Brasel, K. Norris, R. Allen, A. Caruso, and K. Durbhakula, “Efforts to Reduce Physical Aperture Area of Ultra-Wideband Arrays” (Poster)

[9] A Caruso, “ONR Short Pulse Research and Evaluation for c-sUAV: Supporting and Sub-Programs Overview” (Oral)

[10] J. Clark, R. C. Allen, and S. Sobhansarbandi, “Ultra-Compact Integrated Cooling System Development” (Poster)

[11] J. Eifler, S. Roy, M. Hyde, G. Bhattarai, J. Bhamidipati, A. Usenko, M. Pederson, M. Paquette, A. Caruso, S. Bellinger, L. Voss, and R. Allen, “TCAD Optimization of Epitaxially Grown Drift-Step Recovery Diodes and Pulser Performance” (Poster)

[12] N. Gardner, M. Paquette, and A. Caruso, “Diode-Based Nonlinear Transmission Lines Capable of GHz Frequency Generation at Single MW Peak Powers” (Poster)

[13] M. Hamdalla, A. Caruso, and A. Hassan, “The Shielding Effectiveness of UAV Frames to External RF Interference” (Poster)

[14] M. Hamdalla, A. Caruso, and A. Hassan, “A Predictive-Package for Electromagnetic Coupling to Nonlinear-Electronics using Equivalent-Circuits and Characteristic-Modes (PECNEC)” (Poster)

[15] M. Hyde, J. Eifler, S. Roy, G. Bhattarai, A. Usenko, M. Paquette, A. Caruso, S. Bellinger, L. Voss, and R. Allen, “Development of an Evaluation Network for Drift Step Recovered Diodes through and Augmented Design of Experiment” (Poster)

[16] S. Indharapu, A. Caruso, and K. Durbhakula, “Machine Learning Based Ultra-Wideband Antenna Array Optimization and Prediction” (Poster)

[17] F. Khan, W. Azad, and A. Caruso, “A Scalable Multilevel-Modular 10 kV Silicon Carbide MOSFET Architecture for Pulsed Power Applications” (Poser)

[18] D. F. Noor, J. Eifler, M. Hyde, G. Bhattarai, S. Roy, J. Bhamidipati, A. Usenko, M. Pederson, M. Paquette, A. Caruso, S. Bellinger, L. Voss, and R. Allen, “DSRD-IES Pulsed-Power Generator Topology Study Using Machine-Learning-Based Feature Selection Optimization and Predictive Learning” (Poster)

[19] S. Roy, J. Eifler, M. Hyde, G. Bhattarai, D. Noor, J. Bhamidipati, A. Usenko, M. Pederson, M. Paquette, A. Caruso, S. Bellinger, L. Voss, and R. Allen, “Systematic Topological Optimization of DSRD-Based IES Pulse Generator” (Poster)

[20] S. Shepard and A. Caruso, “Tubular Core Optical Power Amplifier” (Poster)

[21] H. Thompson, M. Paquette, and A. Caruso, “Minimizing On-State Resistance in GaN:X Photoconductive Semiconductor Switches (PCSSs) for Direct Modulation (Poster)

[22] A. Usenko, J. Eifler, S. Roy, G. Bhattarai, M. Hyde, M. Paquette, A. Caruso, S. Bellinger, L. Voss, and R. Allen, “New Paradigm in Fabrication of Semiconductor Opening Switches for Pulsed Power” (Poster)

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[23] S. Bellinger, A. Caruso, A. Usenko, “Stacked Diodes for Pulsed Power Applications: New Process Integration Scheme,” 240th Electrochemical Society Meeting, Orlando, FL, Oct. 10–14, 2021 (submitted, oral).

11.4.2 *Presented*

[24] W. Azad, S. Roy, and F. Khan, “A Four-State Capacitively Coupled High-Voltage Switch Powered by a Single Gate Driver,” *47th IEEE Conference on Plasma Science*, Singapore, December 6-10, 2020 (oral).

[25] J. Hunter, S. Xia, A. Harmon, A. Hassan, V. Khilkevich, and D. Beetner, “Simulation-Driven Statistical Characterization of Electromagnetic Coupling to UAVS,” *Annual Directed Energy Science and Technology Symposium*, March 2020 (abstract appeared, but talk cancelled due to pandemic).

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DEPS Posters and Presentations 2020

[26] William Spaeth, Wideband Parallel Plate to Coaxial Cable Taper

[27] Stefan Wagner, Quickly Determining Minimum HPC Source Requirements Using Binary Search

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GOMAC 2019

[28] Cash Hauptmann, Reduced Recovery Time in SiPCSS Photoconductive Switches

[29] Eliot Myers, Picosecond High Power Switching Technologies

[30] Heather Thompson, GaN Optimization for Use in Photoconductive Switch

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[28] B. Barman, D. Chatterjee, and A. N. Caruso, “Analytical Models for L-Probe fed Microstrip Antennas,” *Proceedings of the IEEE Antennas and Propagation International Symposium and National Radio Science Meeting*, Atlanta, Georgia, USA, July 7-12, 2019 (1 page URSI Abstract).

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Directed Energy Professional Society (DEPS) Annual Science and Technology Symposium, Destin, Florida, USA, April 2019:

[29] Ryan Butler, Mechanical Challenges of Modular Photoconductive Semiconductor Based HPM Sources

[30] Steve Young, Two-Dimensional Optoelectronic Pulsed Power Switches: Initial Effort

[31] Adam Wagner, Rapid Cost Effective RF Component Prototyping Using 3D Printers

[32] Heather Thompson, Cost to benefit analysis of GaN for Photoconductive Semiconductor Switches

[33] Colby Landwehr, Low Leakage Electroluminescence For Improving SiPCSS Hold Off

[34] James Kovarik, Some Investigations Into Applications Of Electrically Small Antennas As Phased Array Elements

[35] Spencer Fry, Maximizing SiPCSS Efficiency For HPM Sources

[36] Deb Chatterjee, Studies On Antenna Characterization And Propagation Of High Power Pulsed Electromagnetic Waves With Minimal Dispersion

***

DEPS Posters and Presentations 2018

[37] Jeff Scully, ElectroLuminescence Studies of Silicon Based Photo-Switches

[38] Cash Hauptmann, Thermal Anlaysis of a PCSS through TCAD Simulation

[39] Nicholas Flippin, Fast Rise Time Switches: Drift Step Recovery Diode

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DEPS Posters and Presentations 2017

[40] Noah Kramer, Recent Results of Silicon Based Photoconductive Solid State Switches for 500kHz Continuous Pulse Repetition Frequency

11.5 Theses and Dissertations

[1] Jordan N. Berg, “Development of a Jet Impingement Thermal Management System for a Semiconductor Device with the Implementation of Dielectric Nanofluids,” MS Thesis in Mechanical Engineering, University of Missouri-Kansas City, **2021** [mospace].

[2] James C. Kovarik, “Wideband High-Power Transmission Line Pulse Transformers,” MS Thesis in Electrical Engineering, **2021** [mospace].

[3] Wasekul Azad, “Development of Pulsed Power Sources Using Self-Sustaining Nonlinear Transmission Lines and High-Voltage Solid-State Switches,” PhD Dissertation in Electrical Engineering, **2021** [mospace].

[4] Paul Klappa, “Implementation and Assessment of State Estimation Algorithms in Simulation and Real-World Applications,” MS Thesis in Mechanical Engineering, **2021** [mospace].

11.6 IP Disclosures Filed

[1] S. Bellinger, A. Caruso, A. Usenko, US Provisional Patent Application “Stacked Diode with Side Passivation and Method of Making the Same,” 12AUG2021.

[2] S. Bellinger, A. Caruso, A. Usenko, “Diode and Method of Making the Same,” 28JUNE2021.

[3] Bhamidipati, Myers, Caruso, “Multi-Stage Photo-Stimulated WBG-PCSS Driven RF Pulse Generation System Implementing Miniature Optical Sources,” 21UMK009, 04NOV2020.

[4] Shepard, “A Low Noise Optical Amplifier,” 21UMK007, 14SEPT2020.

[5] Shepard, “A Novel Optical Fiber Amplifier,” 20UMK012, 02JUN2020.

[6] Doynov, “High-power High Repetition Rate Microwaves Generation with Differentially Driven Antenna,” 20UMK011, 19APR2020.

[7] Doynov, “Scalable Modular System for High-power Microwaves Generation,” 20UMK010, 19APR2020.

[8] Doynov, “Pulse Differential High-power Microwave Generation,” 19UMK007, 02JAN2019.

[9] Doynov, “Non-linear Network Topologies with Reutilized DC and Low-frequency Signal,” 19UMK008, 28DEC2018.

[10] Doynov, Caruso, “Non-Linear Transmission Line Topologies for Improved Output,” 19UMK005, 28SEPT2018

11.7 Provisional Patents Filed

[1] S. Bellinger, A. Caruso, A. Usenko, US Provisional Patent Application “Stacked Diode with Side Passivation and Method of Making the Same,” filed 09/10/2021.

[2] S. Bellinger, A. Caruso, A. Usenko, “Diode and Method of Making the Same” US Provisional Patent Application 63/216,550, filed June 30, 2021.

[3] P. Doynov, A. Caruso, “High-Efficiency High-Power Microwave Generation using Multipass Non-Linear Network Topologies,” filed 26NOV2019.

[4] Plamen Doynov, James Prager, Tim Ziemba, Anthony N. Caruso, “Non-Linear Transmission Line Topologies for Improved Output”, USPTO Provisional Serial No. 62/737,185, filed 27SEPT2018.

11.8 Non-Provisional Patents Filed

None to date

ONR HPM Program – Monthly Status Report (MSR) – April 2022

Anthony Caruso – Univ. Missouri – Kansas City

N00014-17-1-3016 [OSPRES Grant]

ONR Short Pulse Research, Evaluation and non-SWaP Demonstration for C-sUAS Study

15 MAY 2022

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OSPRES Grant Approach: A fail-fast philosophy is maintained, where if a technology or capability is deemed infeasible to be demonstrated or validated during the project period-of-performance, it shall be culled, results to date and basis of infeasibility documented, and the next major gap/deficiency area addressed by that part of the project sub-team. Students whose thesis depends on following through with a full answer during the life of the award will be given special dispensation to continue their work.

OSPRES Grant Security: All efforts should be fundamental and publicly releasable in nature when taken individually. This report has been reviewed for operational security, compilation, proprietary and pre-decisional information concerns.

1 Contents

2 Executive Summary

2.1 Progress, Significant Findings, and Impact

Fiber Laser and Optical Amplifiers. We continued to extend our range of applications to the use of our tubular-core optical power amplifier technology as power combiners (which are of substantial DoD interest). We created two COMSOL models of a beam shaping, optical power combiner: one using a cladding of 6 tubes coupling into a 7^{th} (inner) tube, the other using a cladding of 6 tubes coupling into only the hollow core of the entire waveguide. In both the 7-tube and 6-tube designs we have initiated a plan for optimizing power transfer and beam quality. The 7-tube model will also permit the analysis of power splitting the single tube amplifier output for HPM applications. For the HEL applications we obtained our best-yet Gaussian beam profile via the discovery of new hollow-core dynamics (an intensity dependent resonance). Experimental work on the fiber amplifier prototype revealed that we must shorten the fiber length, and the tools to properly do so have been obtained.

On-State Resistance in GaN:X Photoconductive Semiconductor Switches (PCSSs). All of the literature review information compiled to date has been summarized, and will serve as a guide for simulation and study direction. Our near-term focus will be directed towards completion of a manuscript, before moving forward with acquiring TCAD and COMSOL results.

DSRD Optimization Simulations. For drift-step-recovery diode (DSRD) based pulser systems, achieving >10-kV power module peak load voltage while maintaining low risetimes (via voltage riserates experimentally seen at ~6×10^{11} V/s for single 7-stacks) is crucial for increasing peak power capabilities of large systems (~1 GW). Circuit simulations (SPICE software) are used to optimize capacitive and inductive components within the power modules of the DSRD-based pulser designs for peak load voltage but rely on accurate SPICE DSRD models. To improve upon the DSRD CMC SmartSpice diode model already developed for DSRD-based pulser simulations, a sectioned forward IV fitting has been developed in the Verilog-A code to very closely match the non-standard experimental forward IV seen for EG series DSRD. With improved fitting of the forward IV (and reverse CV) within the CMC diode model, DSRD-based power module pulser simulations of recovery properties can match experimental peak load voltage, voltage riserates, risetimes, and pulsewidths over a variety of pulser prime voltages and trigger durations and for different DSRD devices. Progress in collecting the experimental lower and higher voltage and current forward IV are being made and account for clamping pressure and improved measurement accuracy using 2- vs 4-point probe methods and sourcing current vs voltage for different low, medium and high measurement ranges. The CMC diode model can then fit the improved experimental forward IV dependent on clamp pressure and determine to what extent the experimental forward IV must be modeled to capture experimental pulser performance within the recovery parameter fitting.

DSRD Processing and Manufacturing. A process window for the anisotropic etch of v-grooves has been experimentally evaluated. It was found that the process window is wide enough to guarantee near 100% yield at this process step during DSRD manufacturing. In the development of the DSRD stacking step, solid–liquid interdiffusion (SLID) bonded

dies were analyzed with scanning electron microscopy (SEM). The SEM cross section shows high-quality bonding with much lower size and density of voids as compared to traditional stacking techniques such as eutectic bonding or soldering. The thickness of the SLID bonding metal layer is about an order of magnitude lower compared to that of traditional bonding techniques. Lower thickness will result in higher reliability of the final DSRDs.

DSRD Design of Experiments. The evaluation of the forward current–voltage measurements showed poor measurement outcomes as a result of the picoammeter sample fixture. These poor outcomes are believed to be due to the inconsistent pressure applied to each diode during the current–voltage test, as it was found that a diode under test would show measurement fluctuations as the pressure across the diode changed. A press pack fixture from the pulser circuit can be used to apply consistent pressure across the diode and can be hooked up, not only to the picoammeter, but also to the 371A curve tracer. Current–voltage measurements of the diodes using the press pack fixture are in progress, and measurement improvement will be evaluated.

DSRD-Based Pulsed Power Source Optimization. We have extended the DSRD pulser simulations to the SPT Gen-2 diodes and have optimized the pulsers containing 7-, 14, 21-, and 28-stack diodes. In the simulation, we also included circuit limitations such as diode breakdown voltage, limiting MOSFET current, and MOSFET voltage required to keep the circuit safe. We have shown that the output voltage obtained from the experiments can be significantly lower than the simulated output if the diode series resistance is larger than the resistance used in the LT-Spice model, and this could possibly be due to the method we have used to extract the diode series resistance.

Thermal Management. Based on the results from the previous jet impingement thermal management system (JI-TMS) design and further literature review, it was concluded that the JI-TMS performance shows promise for further investigation with adjustments to the geometry as well as the use of alternative heat transfer fluids to overcome the shortcomings of pressure losses and to increase heat removal. Moreover, two other types of TMS are proposed for performance comparison alongside the JI-TMS: a monolithically integrated manifold microchannel chip and an ultra-compact TMS to be directly integrated into the semiconductor. Moving forward, all three designs will be modeled with SOLIDWORKS and the performance of said designs will be investigated under the same boundary conditions by using ANSYS Fluent to provide a baseline for narrowing down TMS design considerations.

Continuous Wave Diode-NLTL Based Comb Generator. Frequency harmonics up to 0.3 GHz were realized using a K50F epoxy diode-based nonlinear transmission line (D-NLTL) with 3.3 nH series inductance at excitation frequencies <70 MHz. A decrease in the number of generated frequency bands was noticed with an increase in excitation frequency, eventually pushing the D-NLTL to pulse sharpening (frequency doubling) mode. Upon studying the center frequency (f_c) and peak voltage (V_{peak}) as a function of source and load impedances, a NLTL configuration with 10 Ω source impedance and 50 Ω load impedance demonstrated higher f_c and V_{peak}, while a NLTL configuration with 50 Ω impedances at source and load demonstrated the lowest. With the test equipment

equipped with 50 Ω connectors, the possibility of implementing a 10 Ω impedance transformer capable of interfacing the NLTL will be investigated in the next report cycle.

Dynamically Tunable Multi-Frequency Solid-State Frozen Wave Generator (FWG). The Gen-2 12-segment FWG with updated tunable components was retested to verify the limitations such as peak voltage reduction, pulse overlap, and frequency generation (reported in the previous report cycle). Based on the results, a manuscript was submitted to the international journal of electronics and communications, which is currently under review. A comprehensive summary report of the findings and potential future scope will be included in the next report cycle.

Pulse-Compression-Based Signal Amplification. The effects of core remanence and coercivity on core saturation behavior and on the magnetic pulse compression (MPC) circuit leakage currents and reflections were investigated through LTSpice simulations. The MPC input stage was modified to work efficiently in an MPC circuit with bipolar input while minimizing reflections. Leakage currents and reflections are important design considerations for the high frequency MPC circuit as they will limit the input pulse window during continuous MPC operation. A prototype B–H curve tracer circuit was built for core characterization in order to ensure accurate modeling of magnetic cores for simulations and design.

Antennas. A wideband, microstrip patch, electrically small antenna (ESA) element, fed by a customized tapered coaxial connector, was designed for operation in the UHF range (0.7–1.1 GHz) and was forwarded for fabrication. If reasonable performance is achieved from the single antenna element, they will be arrayed to form the final demonstrable prototype.

A standalone prototype of the impedance transformer was fabricated and tested to identify the source of reflections in the original 3D printed & Cu-foil-plated variant of the Koshelev antenna prototype. The frequency-domain measured S-parameters of the standalone mirrored stereolithography (SLA)-based balanced impedance transformer maintained good reflection coefficient values (< –10 dB) throughout the frequency spectrum. Moreover, the time-domain simulated output voltage validates the proposed transformer design by retaining over 99% of the peak power and the pulse shape. However, the transformer–antenna combined simulation resulted in increased feed reflections. The performance reduction noticed in the S-parameters and frequency spectrum of the electric field is significant between 1 and 2 GHz. A 17% peak field reduction is observed from the combined simulation (transformer–antenna) when compared to the standalone Koshelev antenna simulation.

The machine-learning-based antenna response prediction tool has been improved to generate hundreds to thousands of tradespace study data points within seconds to make faster design decisions. The graphical user interface (GUI) includes more features such as (1) a selection of different antenna response metrics and (2) an option to input a custom number of samples over a pre-determined design parameter range.

2.2 Completed, Ongoing, and Cancelled Sub-Efforts

	Start	End
2.2.1 *Ongoing Sub-Efforts*		
GaN:C Modeling and Optimization	OCT 2017	Present
Diode-Based Non-Linear Transmission Lines	FEB 2018	Present
Trade Space Analysis of Microstrip Patch Arrays	FEB 2019	Present
Lasers and Optics	FEB 2020	Present
UWB Antenna Element Tradespace for Arrays	MAY 2020	Present
Si-PCSS Contact and Cooling Optimization	JAN 2021	Present
Drift-Step Recovery Diode Optimization Simulations	JAN 2021	Present
DSRD-Based IES Pulse Generator Development	APR 2021	Present
Drift-Step Recovery Diode Manufacturing	MAY 2021	Present
DSRD Characterization through Design of Experiments	MAY 2021	Present
Sub-Nanosecond Megawatt Pulse Shaper Alternatives	MAY 2021	Present
Ultra-Compact Integrated Cooling System Development	MAY 2021	Present
Continuous Wave Diode-NLTL Based Comb Generator	SEPT 2021	Present
Pulse-Compression-Based Signal Amplification	DEC 2021	Present
2.2.2 *Completed/Transferred Sub-Efforts*		
Adaptive Design-of-Experiments	OCT 2017	APR 2019
Non-perturbing UAV Diagnostics	OCT 2017	OCT 2018
Noise Injection as HPM Surrogate	OCT 2017	MAR 2019
SiC:N,V Properties (w/ LLNL)	APR 2018	MAR 2019
Helical Antennas and the Fidelity Factor	JUL 2018	SEPT 2019
Si-PCSS Top Contact Optimization	APR 2020	OCT 2020
Nanofluid Heat Transfer Fluid	NOV 2020	JUL 2021
HV Switch Pulsed Chargers	DEC 2018	DEC 2021
Enclosure Effects on RF Coupling	OCT2019	DEC 2021
UAS Engagement M&S	MAR 2021	DEC 2021
GaN-Based Power Amplifier RF Source	AUG 2021	DEC 2021
2.2.3 *Cancelled/Suspended Sub-Efforts*		
Ab Initio Informed TCAD	OCT 2017	OCT 2020
Positive Feedback Non-Linear Transmission Line	NOV 2017	DEC 2018
Minimally Dispersive Waves	FEB 2018	SEPT 2018
Multiferroic-Non-linear Transmission Line	NOV 2018	APR 2019
Avalanche-based PCSS	SEPT 2018	SEPT 2019
Gyromagnetic-NLTL	DEC 2017	NOV 2020
Multi-Stage BPFTL	APR 2020	JUL 2020
Heat Transfer by Jet Impingement	MAY 2018	FEB 2021
Si, SiC, and GaN Modeling and Optimization	NOV 2018	FEB 2021
Bistable Operation of GaN	FEB 2021	MAR 2021
WBG-PCSS Enabled Laser Diode Array Driver	NOV 2020	JAN 2022

2.3 Running Total of Academic and IP Program Output

See Appendix for authors, titles and inventors (this list is continuously being updated)

Students Graduated	*6 BS, 9 MS, 4 PhD*
Journal Publications	*6 (6 submitted/under revision)*
Conference Publications	*35 (3 submitted/accepted)*
External Presentations/Briefings	*40*
Theses and Dissertations	*4*
IP Disclosures Filed	*10*
Provisional Patents Filed	*4*
Non-Provisional Patents Filed	*0*

3 Laser Development

3.1 Fiber Lasers and Optical Amplifiers

(Scott Shepard)

3.1.1 *Problem Statement, Approach, and Context*

Primary Problem: High-average-power 1064-nm picosecond lasers are too large (over 1100 cm^3/W) and too expensive (over \$1000/μJ per pulse) for PCSS (photoconductive semiconductor switch) embodiments of HPM-based defense systems. For example, a laser of this class might occupy a volume of 1 m x 30 cm x 30 cm = 90,000 cm^3 and provide an average power of 50 W (thus, 1800 cm^3/W). Costs in this class range from \$100K to \$300K to drive our Si-PCSS applications.

Solution Space: Optically pumped ytterbium-doped optical fiber amplifiers, fed by a low-power stable seed laser diode, can offer a cost-effective, low-weight, and small-volume solution (with respect to traditional fiber and traditional free-space laser designs). Moreover, our novel optical amplifier tubes, might operate at far higher power levels (over 1000 times greater), thus driving an entire array of PCSS with a single amplifier and thereby reducing the overall system costs and eliminating the optical pulse-to-pulse jitter constraints.

Sub-Problem (1): Optical pump power system costs account for over 50% of the budget for each laser (in this class, for normal/free-space, optical fiber, and tubular embodiments).

Sub-Problem (2): Fiber (as well as power tube) optical amplifier performance is degraded primarily by amplified spontaneous emission (ASE) noise, which limits the operating power point, and by nonlinearities, which distort the optical pulse shapes.

State-of-the-Art (SOTA): Free-space NdYAG lasers or Ytterbium-doped fiber amplifiers optimized for LIDAR, cutting, and other applications.

Deficiency in the SOTA: Optical pump power system costs (in either free-space or fiber lasers) are prohibitive for the PCSS applications until reduced by a factor of at least two.

Solution Proposed: Fiber lasers permit a pre-burst optical pumping technique (wherein we pump at a lower level over a longer time) which can reduce pumping costs by a factor of at least ten. To address the ASE and nonlinear impairments, we are pursuing the use of gain saturation and a staged design of different fiber diameters. We also apply these techniques to fiber amplifiers which incorporate our power amplifier tube in the final stage. The inclusion of our novel tubular-core power amplifier stage should permit a single laser to trigger an array of several PCSS (reducing system cost and mitigating timing jitter).

Relevance to OSPRES Grant Objective: The enhancement in SWaP-C^2 for the laser system enables PCSS systems for viable deployment via: a factor of 40 in pumping cost reduction of each laser; and a factor of *N* in system cost reductions as a single laser could drive *N* (at least 12) PCSS in an array, while also eliminating the optical jitter constraints.

Risks, Payoffs, and Challenges: Optically pumping outside the laser pulse burst time can enhance the ASE; pump costs could be reduced by 40, but ASE in the presence of dispersion and/or nonlinearities could enhance timing jitter thereby limiting steerability. The main challenge for power tube implementation is the entrance optics design.

3.1.2 *Tasks and Milestones / Timeline / Status*

(A) Devise a pre-burst optical pumping scheme by which we can reduce the costs of the laser by a factor of two or more and calculate the resulting increase in ASE. / FEB–JUL 2020 / Completed.

(B) Reduce the ASE via gain saturation. / Oct 2020 / Completed.

(C) Design saturable gain devices which avoid nonlinear damage. / Ongoing.

(D) Calculate and ensure that timing jitter remains less than +/-15 ps with a probability greater than 0.9. / Ongoing.

(E) Demonstrate a cost-reduced fiber laser. / August 2022.

(E1) March 2021 Finalize design. / Completed.
(E2) April 2021 Assemble and test-check seed LD (laser diode)/driver. / Completed.
(E3) April 2021 Measure power vs current transfer function of seed LD/driver. / Completed.
(E4) May–July 2021 Measure ASE and jitter of 1064 nm seed LD/driver. / Completed.
(E5) May–July 2021 Measure ASE and jitter of 1030 nm seed LD/driver. / Completed.
(E6) June–July 2021 Assemble and test-check pump LDs/drivers. / Completed.
(E7) June–July 2021 Measure power vs current transfer function of pump LDs/drivers. / Completed.
(E8) July–September 2021 Splice power combiners to Yb doped preamp fiber. /Completed.
(E9) July–September 2021 Connect seed and pumps to power combiners and test-check. / Completed.
(E10) September–October 2021 Measure gain, ASE and jitter of 1064 nm preamp assembly (forward, backward and bidirectional pumping) as a function of pump power and duty cycle. / Partially completed before task eliminated.
(E11) September–October 2021 Measure gain, ASE and jitter of 1030 nm preamp assembly (forward, backward and bidirectional pumping) as a function of pump power and duty cycle. / Partially completed before task eliminated.
(E12) November 2021 Splice power amplifier and its power combiner to best preamp. / Partially completed before task eliminated.
(E13) May–August 2022 Measure gain, ASE and jitter of entire amp assembly. / Ongoing.
(E14) May–August 2022 Analyze data and document. / Ongoing.

(F) Design a new type of higher power, tubular core fiber amplifier. / August 2022.

(F1) Apply one high-power tubular amplifier to a system comprised of an array of several (say N) PCSS. For example: N=12 in a 3x4 array (or 4x4 array with corners omitted) N=16

in a 4x4 array, etc.; thereby eliminating jitter constraints and reducing laser system cost by more than a factor of 100 (independent of burst profile). / August 2022.

(F2) Design a high power, multiple tube optical amplifier and determine if it permits advantages for power handling or beam profile. / August 2022 / Initiated.

(G1) Design a beam shaping, optical power combiner using a cladding of 6 tubes. / June 2022 / Initiated.

(G1.1) Develop COMSOL models. / April 2022 / Completed.

(G1.2) Discover and optimize the length at which the cladding modes couple maximal power into the core mode (of the entire waveguide). / June 2022 / Ongoing.

(G2) Design a beam shaping, optical power combiner using a cladding of 6 tubes surrounding one inner tube. / July 2022 / Initiated.

(G2.1) Develop COMSOL models. / April 2022 / Completed.

(G2.2) Discover and optimize the length at which the cladding modes couple maximal power into the inner tube. / July 2022 / Ongoing.

(G3) Develop spectral combiners based on multiple-tube waveguides and compare to existing PCF (photonic crystal fiber) technologies. / August 2022 / Initiated.

3.1.3 *Progress Made Since Last Report*

(E13) Experimental work on the fiber amplifier prototype revealed that we must shorten the fiber length. Recall that miscommunication between our vendors resulted in an 8 [m] length of dual-core Yb doped fiber was fused to the output of our power combiner (instead of our directive to use 2 [m] for a pre-amp; and save the remaining 6 [m] for a power amp). We decided to circumvent this by cutting the doped fiber to progressively shorter lengths but encountered (supply chain) delivery delays on an order of the tools to properly do the cutting. Recently we experimentally confirmed that our pump laser diode power cannot be detected after the anticipated 40 dB loss at a length of 8 [m] so we have no choice other than to shorten the length. The tools to properly do so have recently been obtained, so our experimental effort can now continue.

(F) Recall that last month we considered a variety of polarization and phase combinations for the input to our optical power tube, and found that we could produce Gaussian-like; or more uniformly distributed, output beam profiles (for the HEL and HPM applications respectively). We now report on our best-yet Gaussian beam profile and how it was enabled via the discovery of a new hollow-core intensity dependent resonance.

(F1) For the HPM application of uniformly illuminating a passive power splitter to drive an array of PCSS from a single laser, we resolved last month’s difficulties on importing the output of one COMSOL (e.g., a power amplifier) into the input of another (e.g., a splitter). This required a surprisingly large amount of time in consultation with COMSOL support and others on how to resolve the issue, so we have yet had time to utilize it fully. But we found better cases of uniform-like distributions, to be quantified via the new tool.

(G1.1) (G2.1) We constructed COMSOL models for a 6-tube design and a 7-tube design of a beam shaping, optical power combiner. In contrast to the SOTA power combiners

which utilize a tapering of many waveguides into one, our approach is to use mode-coupling. Thus, their manufacturing would avoid the costly step of creating a taper. We also expect that the absence of a taper will increase their power handling capability.

3.1.4 *Technical Results*

(F) To address both the power combiner and entrance optics applications we again consider illuminating the glass tube with 4 spots. Each spot is comprised of a Gaussian beam impinging on the glass wall/cladding of the tube (of radius r, and thickness t in units normalized with respect to the linear gain, g_0, as discussed in the MSR of FEB2022). For applications which prefer high core power with Gaussian beam profile, the radial polarization appeared to be the most promising so we continued to optimize over grids of various r and t, as shown in table 3.1.1, which enumerates the peak core electric field output in [V/m] with the largest two values in blue at (r=5, t=1) and (r=5, t=3).

r\t	**1**	**2**	**3**
2.5	0.8E+12	0.3E+12	0.6E+12
5	1.4E+12	0.2E+12	1.1E+12
7	0.7E+12	0.2E+12	0.6E+12

Table 3.1.1. Grid of peak core electric field output [V/m] for various r and t values.

For the case of (r=5, t=3) the electric field distribution at the output is shown in Fig. 3.1.1, which reveals a peak amplitude of the core field at roughly the same amplitude as that of the cladding (on the two sides of this cutline across the output). The range of intensities will be discussed after we compare to the (r=5, t=1) case, which is shown in Fig. 3.1.2 to have diminished amplitudes in two cladding peaks on each side of the core.

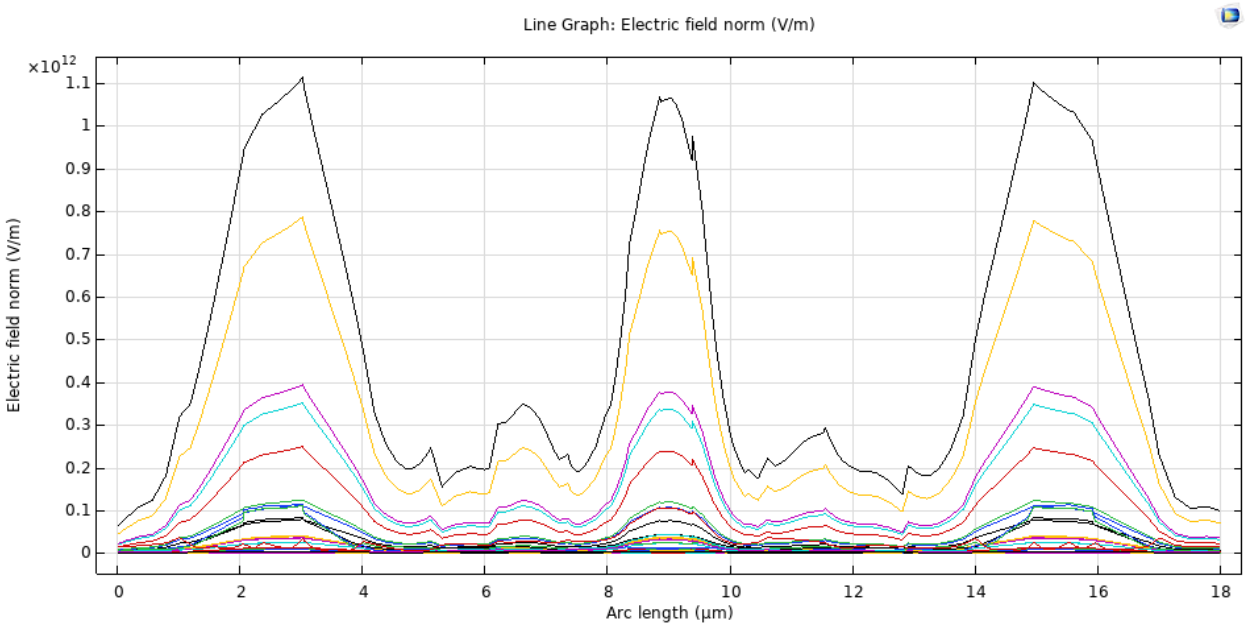

Fig. 3.1.1. Electric field distribution at the output of an optical power tube illuminated by 4 spots of radial polarization (for r=5, t=3).

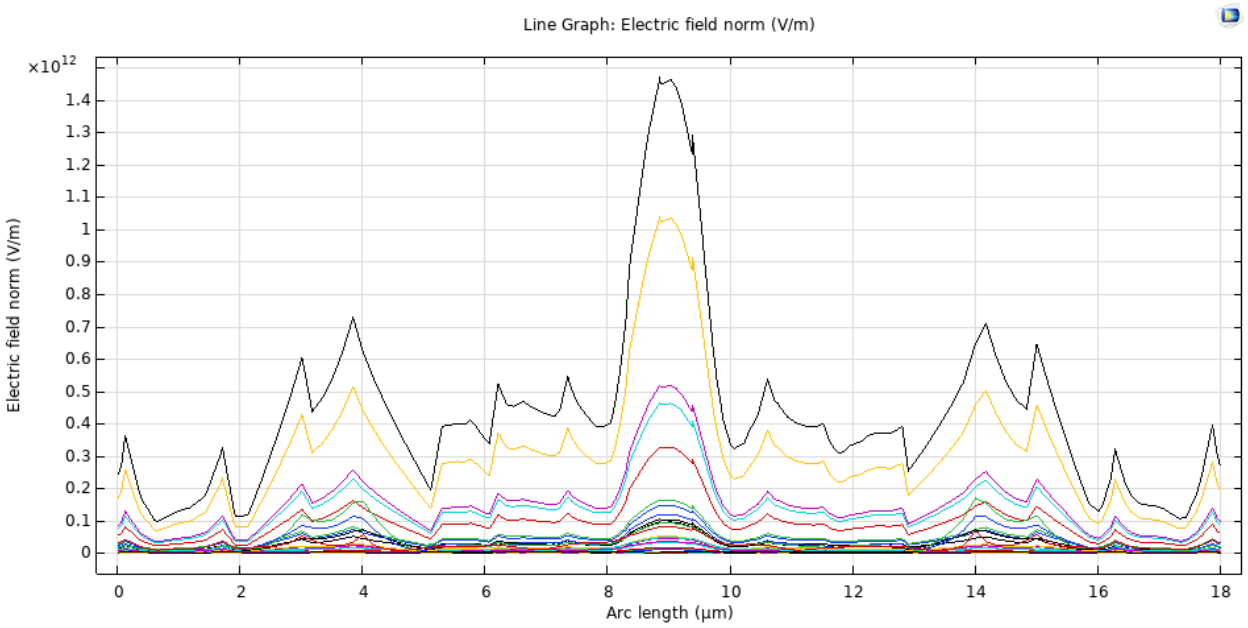

Fig. 3.1.2. Electric field distribution at the output of an optical power tube illuminated by 4 spots of radial polarization (for r=5, t=1).

Smaller values of thickness t do often diminish the cladding output but they would also decrease the nonlinear thresholds for stimulated Brillouin and stimulated Raman scattering, so alternatives are preferable. One could simply block the cladding output with

an aperture (in applications where a single Gaussian profile from the core is desired) but that would constitute wasting energy. Also, Table 3.1.2 shows continued improvement at smaller t, but below t = 0.9 the peak core value is reduced.

r\t	**0.7**	**0.8**	**0.9**
4.9	1.4E+12	1.5E+12	1.52E+12
5	1.4E+12	1.52E+12	1.6E+12
5.1	1.45E+12	1.42E+12	1.5E+12

Table 3.1.2. Grid of peak core electric field output [V/m] for various r and t values.

Fortunately, we have discovered an alternative means of diminishing the cladding output (without resorting to small t). This also provides a means of optimization which includes beam quality (whereas searching grids of peak field strength does not). Returning to the case of (r=5, t=3) we consider the power transfer curves of Pin.clad to Pout.clad in Fig. 3.1.3 and Pin.clad to Pout.core in Fig. 3.1.4.

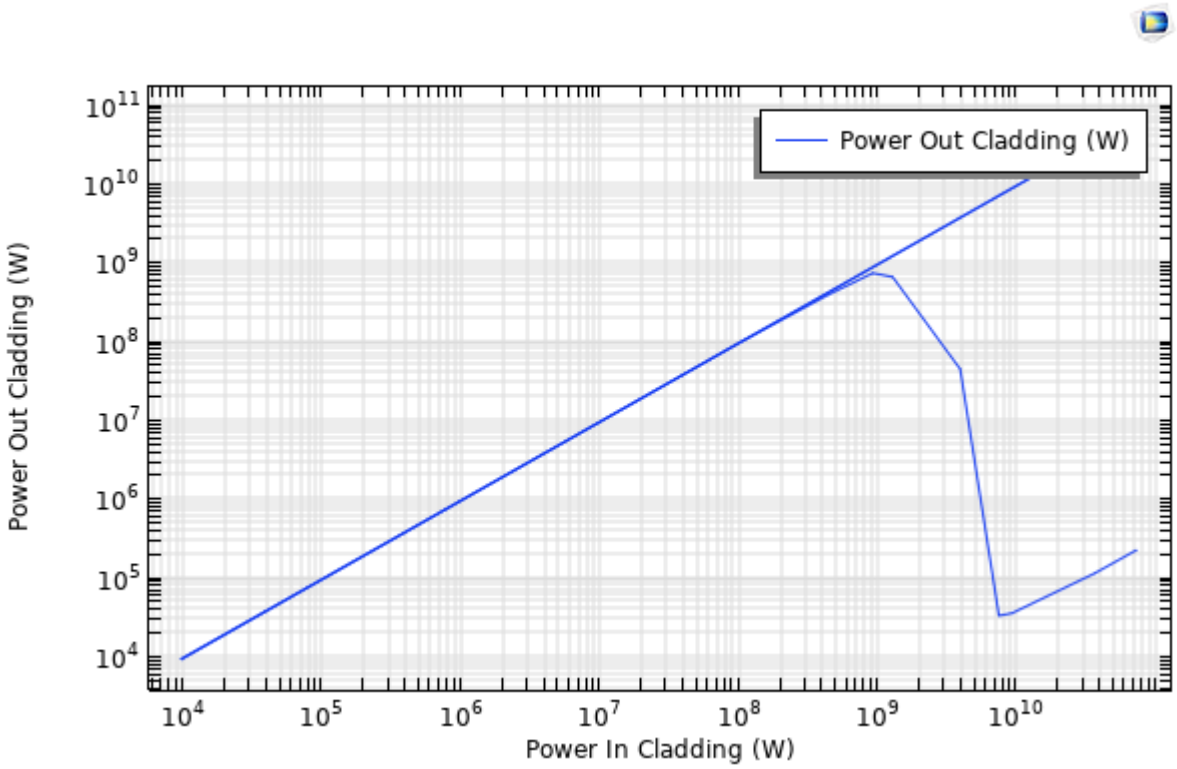

Fig. 3.1.3. Power transfer curve into the cladding output (for r=5, t=3). Straight line represents no nonlinearity ($\gamma = 0$).

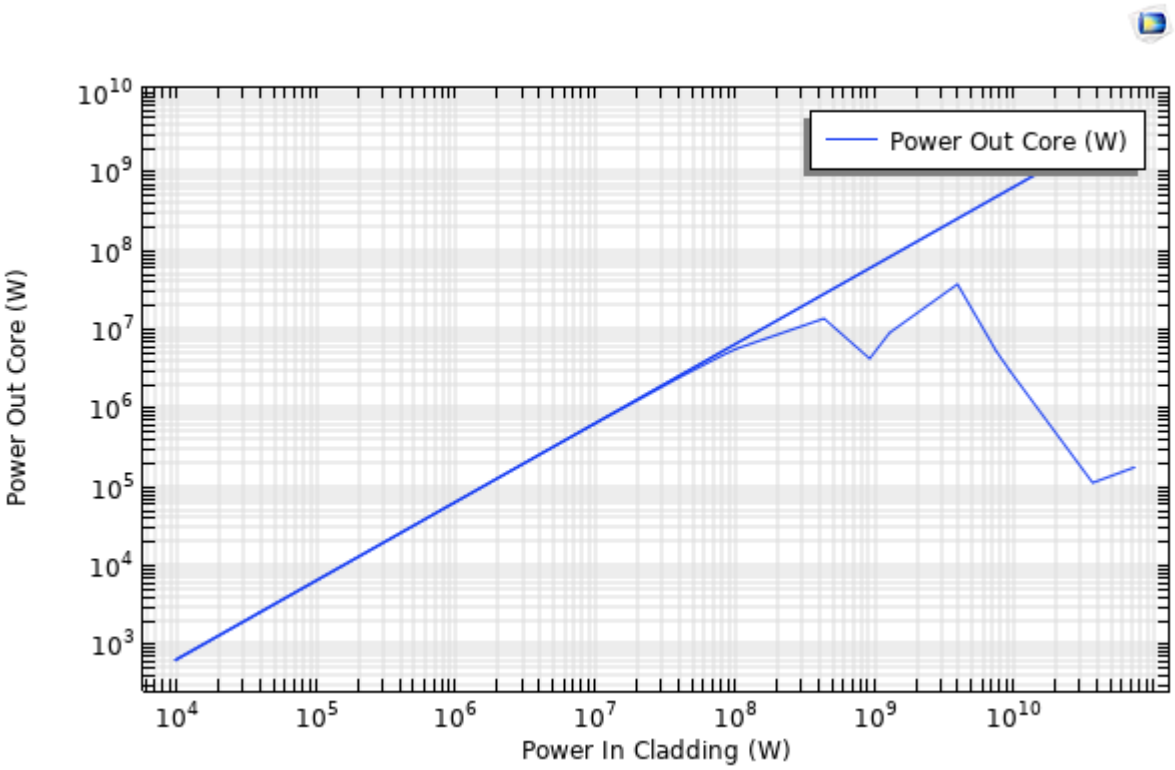

Fig. 3.1.4. Power transfer curve into the core output (for r=5, t=3).
Straight line represents no nonlinearity ($\gamma = 0$).

In Fig. 3.1.3 we observe the familiar breakpoint phenomena near an operating point of Pin.clad ~ 1 GW (for which the power output from the cladding is a little less than 1 GW). In most applications there would be no reason to operate above this breakpoint level since the output power from the cladding (and typically also the core) would rapidly diminish. In Fig. 3.1.4 however, we observe a new phenomena which can happen in the core for this 4 spot, radial polarized illumination. An intensity dependent resonance, at an operating point of 4 GW, surprisingly increases the core output power (and simultaneously diminishes the cladding output, of course since that is above the 1 GW breakpoint).

The operating point of 4 GW corresponds to an input intensity of I_0 = 2 E20 [W/m^2] which yields the best-yet single-Gaussian output beam profile shown in the light blue curve of Fig. 3.1.5. The three lower input intensities of the run are at 1 E20 [W/m^2], 2 E19 [W/m^2], and 1 E19 [W/m^2], for which the cladding output clearly dominates that of the core.

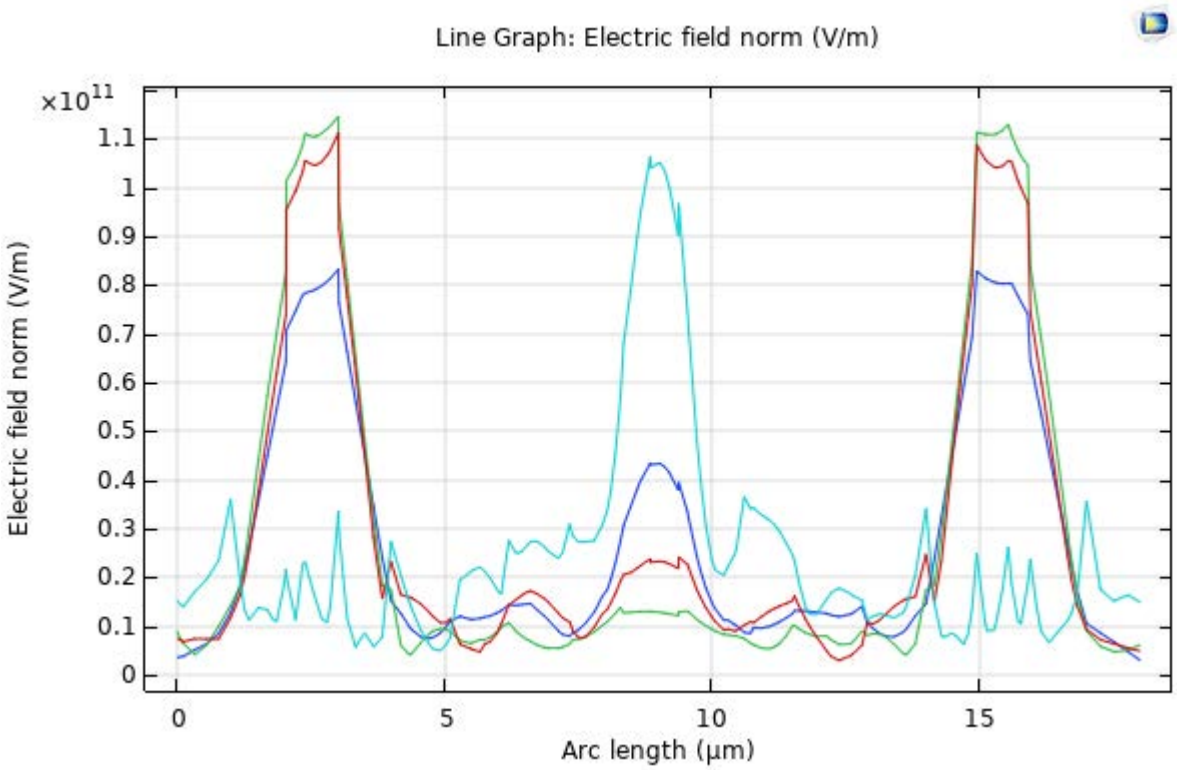

Fig. 3.1.5. Electric field distribution at the output of an optical power tube exhibiting an intensity dependent core resonance (for r=5, t=3).

(F1) For the HPM application of driving an array of PCSS elements via a single laser, split by passive power delivery fibers/tubes, we desire a more uniform output beam profile. For these we prefer the “in-phase polarization” (all 4 spots are z-polarized and driven in-phase). The in-phase example of Fig. 3.1.6 can be contrast to the radial polarized result in Fig. 3.1.2 of the same dimensions. In Fig. 3.1.7 we show an example in which there is more uniformity across the core.

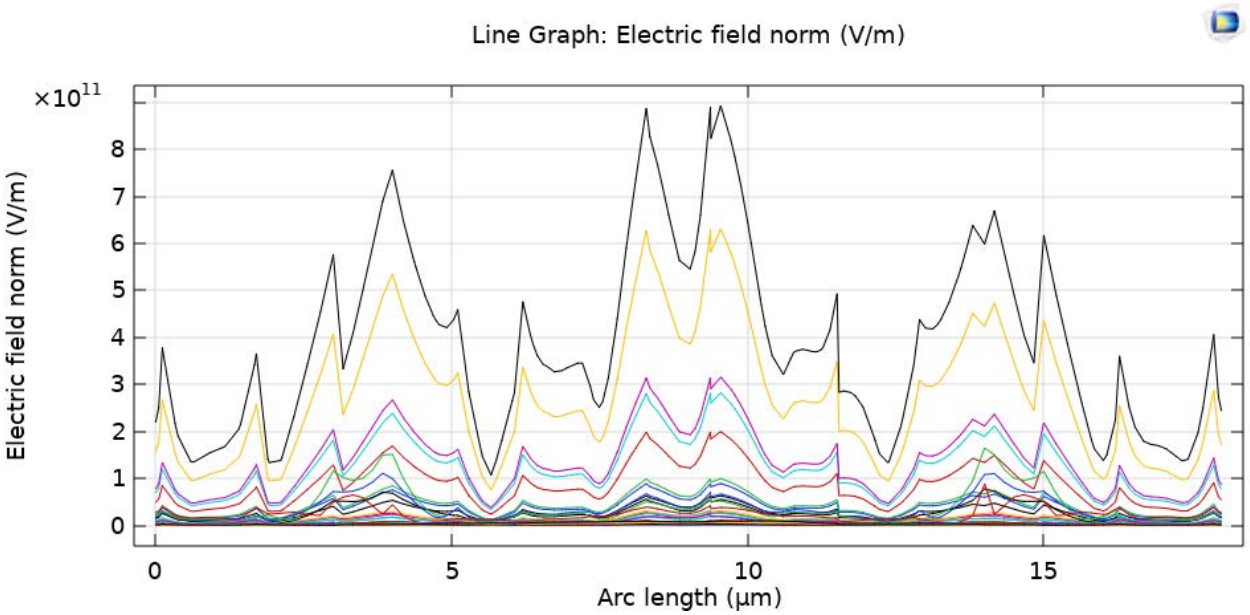

Fig. 3.1.6. Electric field distribution at the output of an optical power tube illuminated by 4 spots of in-phase polarization (for r=5, t=1).

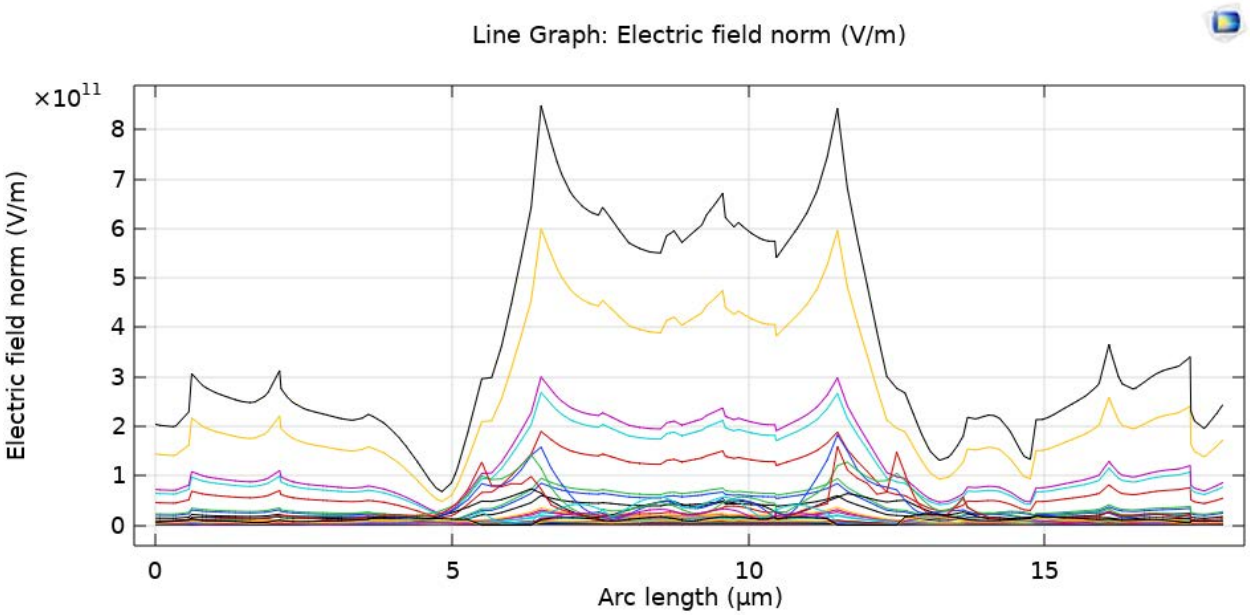

Fig. 3.1.7. Electric field distribution at the output of an optical power tube illuminated by 4 spots of in-phase polarization (for r=2.5, t=1).

To quantify the uniformity of such cases we will export the output-plane field data of the power tube COMSOLs and import them as the input to a different COMSOL which models the passive splitter. Rather than a 37 legged splitter we will begin with 7 legs since this will also simplify our initiation of the study of beam shaping power combiners.

(G1) (G2) for our 6-tube and 7-tube power combiners we have built models with either: 6 tubes surrounding an empty core, as shown in Fig. 3.1.8; or 6 tubes surrounding a 7th (inner) tube.

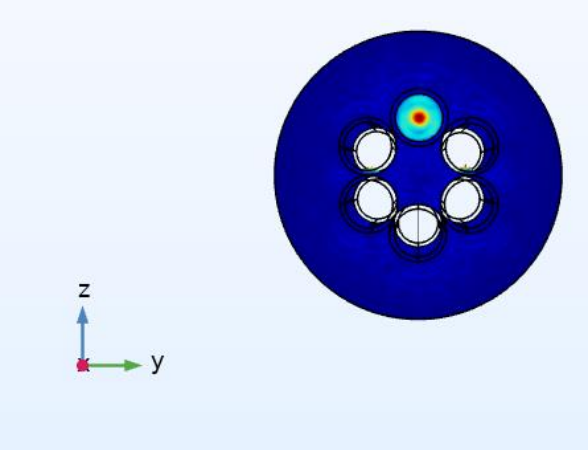

Fig. 3.1.8. End view of a 6-tube beam shaping power combiner.

Our approach to power combining is to utilize mode-coupling between the tubes (rather than the standard technique of using a taper). Evidence of such mode-coupling can be seen in Fig. 3.1.9, where we see the input to a single tube couple into all 6 and then couple back again into a single tube at the output. In the actual application all tubes will be illuminated at the input-plane; but it is important that we first understand some of the nonlinear dynamics before pursuing an assessment of the impacts of the technology.

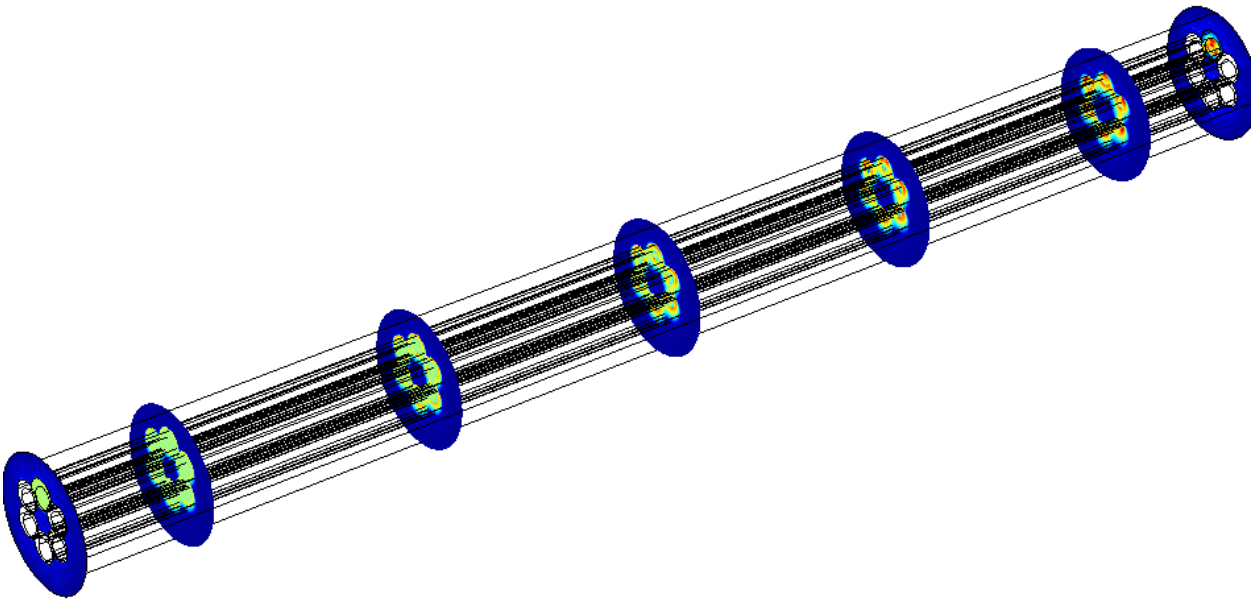

Fig. 3.1.9. Evidence of mode-coupling in a 6-tube beam shaping power combiner.

3.1.5 *Summary of Significant Findings and Mission Impact*

(A) Our pre-burst optical pumping scheme simulations showed that we can drop the pump power costs by a factor of 40 with pre-burst ASE power levels below the heating level tolerance of 100 μW. UMKC invention disclosure filed 02JUN2020.

(B) For a proposed system gain of 8 million, a linear gain theory predicted the in-burst ASE would be over our heating level spec. by a factor of 3960, but by exploiting the nonlinearity of gain saturation we find that we can suppress the ASE by over 7000. UMKC invention disclosure filed 14SEP2020.

(C) Achieved initial practical device designs that exploit gain saturation, which remained below damage thresholds, via staged designs of different mode diameters NOV2020.

(D) Models of the impact of ASE on timing jitter in the presence of dispersion and/or nonlinearities were established JUL2020.

(E) The design of a proof-of-concept experiment demonstrating a cost-reduced optical pumping scheme was finalized MAR2021.

(F) We made (to our knowledge) the first observation of self-focusing effects that are not determined by beam power alone. We found instead that these can also be controlled via the geometric factors within a waveguide (such as fiber core diameter) MAY2021.

We additionally made (to our knowledge) the first observation that a mode exists in the air within a simple glass tube into which we can couple energy from the mode in the glass. Thus, an amplifier (in the doped and pumped glass) can operate at higher powers JUNE2021.

We found conditions under which 0.25 GW of power can exist in the tube's air-core mode when its glass-cladding mode is at a power level near 0.5 GW JULY2021.

Advancements in the very high-power operating point (tens of GW) of our tubular optical amplifier (and the existence, size and spatial uniformity of its air-core mode) were shown to permit a single laser to trigger an array of several (up to 100) Si-PCSS – reducing the laser system cost and eliminating the optical timing jitter constraint. The symmetry breaking of the scattering from self-focusing in a curved waveguide was shown to enable such AUG2021.

4 Photoconductive Switch Innovation

4.1 Characterizing and Optimizing On-State Resistance in GaN:X PCSS

(Heather Thompson)

4.1.1 *Problem Statement, Approach, and Context*

***Primary Problem*:** Traditionally, RF generation using photoconductive semiconductor switches (PCSS) relies on materials such as silicon (Si) or gallium arsenide (GaAs), due to their availability and low cost; however, as these applications begin to require higher operating frequencies, powers, and temperatures, with the same or reduced system form-factor, the theoretical operating limits of these materials are being reached.

***Solution Space*:** By exploiting the 3.4 eV bandgap, 1000 cm^2/Vs electron mobility, and thermal properties of GaN, it is possible to realize pulsed-power applications requiring up to a 5 MV/cm critical field, high-frequency operation, and ~400 °C operating temperature, respectively.

Sub-Problem: One of the most important problems in minimizing conduction losses, maximizing efficiency, and reducing thermal issues in compensated, semi-insulating GaN:X (i.e., GaN:X with X=C, Fe…) PCSS-based systems is achieving <1 Ω on-state resistance by optimizing the modifiable parameters of GaN:X at the material, device, and system levels, while still maintaining quick switch turn-off time and low turn-off losses.

***State-of-the-Art (SOTA*):** PCSS-based RF generation systems using Si, SiC, or GaAs can achieve MW-range output power, ones-of-gigawatts frequency content, and electrical efficiency of ~60% that require increased laser energies and device size to reach maximum efficiency and necessary operating power limits, respectively.

***Deficiency in the SOTA*:** Si-, SiC-, and GaAs-based PCSS require ones-of-mJ of incident laser energy to achieve <1 Ω on-state resistance, leading to increased incident laser requirements, increased heating in devices, and devices that are ones-of-cm^2 in area for the necessary peak power and operating temperatures.

***Solution Proposed*:** Use simulation and available experimental results, from the literature and collected results at UMKC, to optimize the variable parameters of GaN:X PCSS to achieve <1 Ω on-state resistance with increased electrical and optical efficiency while maintaining a quick switch turn-off time and low turn-off losses.

Risks, Payoffs, and Challenges:

***Challenges*:** The high cost of material leads to a limited number of devices available for experimental testing and analysis, requiring a majority of the optimization studies to be performed using simulation software (COMSOL and TCAD).

***Risks*:** Simulation results may differ from experimental results for certain PCSS parameters due to particular photogeneration and recombination parameters not being included in models along with non-ideal, real-world experiments requiring additions such as encapsulation material or other changes not fully addressed in simulation.

***Payoffs*:** By minimizing the conduction losses in GaN PCSS, a compact, tunable RF source can be realized with increased efficiency and SWAP-C^2 capabilities.

4.1.2 Tasks and Milestones / Timeline / Status

(A) Milestone – Determine material, device, and system parameters that affect on-state resistance and which of these can be best leveraged to reduce on-state losses and heating.

1. Task – Literature study of photoelectric on-state resistance to understand how this parameter can be optimized to reduce conduction and on-state losses during PCSS operation *[ongoing].*
2. Task – Literature review of on-state resistance studies performed using GaN-based photoelectric devices to determine areas to further study *[ongoing].*
3. Task – Determine project milestones, tasks, and timeline for optimizing on-state resistance in GaN PCSS *[ongoing]*.

(B) Milestone – Build model of GaN PCSS in TCAD and COMSOL to begin simulation studies *[ongoing].*

1. Task – Build simple, working preliminary GaN PCSS model in COMSOL that can be subsequently altered for more complex analysis of on-state resistance *[Complete – JAN 22]*.
2. Task – Build a working preliminary GaN PCSS model in TCAD to determine which modeling software will provide accurate, efficient results for different parameters affecting on-state resistance *[Complete – MARCH 22]*.
3. Task – Determine parameters that can be altered using TCAD and design studies using this program *[Ongoing]*.
4. Task – Compare simulation results with available experimental results to determine validity of models using TCAD and/or COMSOL *[APRIL 22]*.
5. Task – Set up parametric sweep studies *[MAY 22]*.

(C) Milestone – Determine device level characteristics and relationship with material characteristics—relationship between device and material level characteristics—that can be altered in simulation allowing for optimization of on-state resistance and efficiency of GaN:C PCSS and complete study on leveraging these parameters.

(D) Milestone – Determine circuit and incident photon source characteristics to be studied using simulation towards minimizing on-state resistance in GaN:C PCSS.

(E) Milestone – Design simulation based on Liu, 2021 paper using nano-structures on the surface of the device to overcome shallow absorption depth.

(F) Completion of manuscript on optimizing on-state resistance in GaN:C PCSS *[Ongoing]*

4.1.3 *Progress Made Since Last Report*

(A) Information gathered thus far in literature review has been compiled and summarized below to guide initial simulation and study direction.

(B) A working GaN PCSS model has been constructed using Silvaco TCAD, but will be put on the back burner as focus shifts to completion of a manuscript.

4.1.4 *Technical Results*

On-state resistance is a major contributor to losses and decreased efficiency in GaN-based PCSSs, and this can be mitigated by optimizing certain material, device, and system level parameters towards minimizing on-state resistance. By defining the parameters affecting on-state resistance, how they are correlated to one another, and which are easily manipulated, GaN-based PCSS devices can be used to reduce the size and cost of RF generation systems along with provide systems with increased power, frequency, and temperature capabilities.

By first identifying the operating modes and photogeneration methods to be used, this will reduce the number of possible parameters considered for optimization. Two modes of operation are possible for GaN PCSS: linear (one carrier generated per absorbed photon) and non-linear (impact ionization utilized generating multiple carriers per absorbed photon). While a non-linear mode could offer reduced laser energy needs and increased responsivity, linear operation is preferred due to decreased jitter and increased device lifespan and will be the focus of this work [1]. Photogeneration methods available for GaN PCSS are intrinsic—relying on incident photons at or above the bandgap energy to move electrons to the conduction band—and extrinsic—exploiting mid-gap impurities and defects that can be activated using below bandgap photon energy—but intrinsic operation offers lower on-state resistance due to higher quantum and optical efficiency. However, due to the shallow absorption depth in intrinsic operation, we will restrict the study to lateral devices [2].

Many material characteristics are determined by the inherent material properties and cannot be manipulated, so we will limit this study to those which can be changed during the manufacturing process. The first material alteration we will look at is the carbon doping concentration in GaN, which can be altered during the growth process by varying the growth temperature, pressure, and ratio of precursors but the concentration must stay within a certain range to maintain semi-insulating material properties instead of n- or p-type properties [3]. The second material characteristic that will be considered is substrate type and quality. Typically, Si or GaAs are used due to their low cost, but by using SiC or GaN, defects due to dislocations and strains from lattice and thermal mismatch between substrate and GaN, can be reduced as these defects lead to device failure.

Device level parameters to be studied will encompass device contact type and geometry as these can greatly affect the responsivity and power handling capabilities of these devices by changing the amount of the device surface covered by contact material and the gap length between contacts, respectively. Additional device changes will include the addition of a nanostructure wall array of “nano-fins” based on work done by Liu et al. (2021) using GaAs PCSSs. This work sought to overcome limited active device volume

restricting the minimization of on-state resistance due to shallow absorption depth of incident photons (~0.14 μm at 532 nm incident photon wavelength for GaAs). By adding in a nanostructure wall array of "nano-fins" in the gap length of the device (Figure 4.1.1), or 3D grooves in the surface that are less than one half of the size of the incident photon wavelength to avoid scattering, photon absorption occurs on the top and side surfaces of these fins, essentially increasing the active area cross section and improving photocurrent while reducing trigger fluence (incident energy per area needed for device activation). Shown in Figure 4.1.2, photocurrent in linear mode operation was increased from 1.9 μA to 106 μA for a trigger fluence of 3.8 mW/cm^2 with the addition of these fins [4].

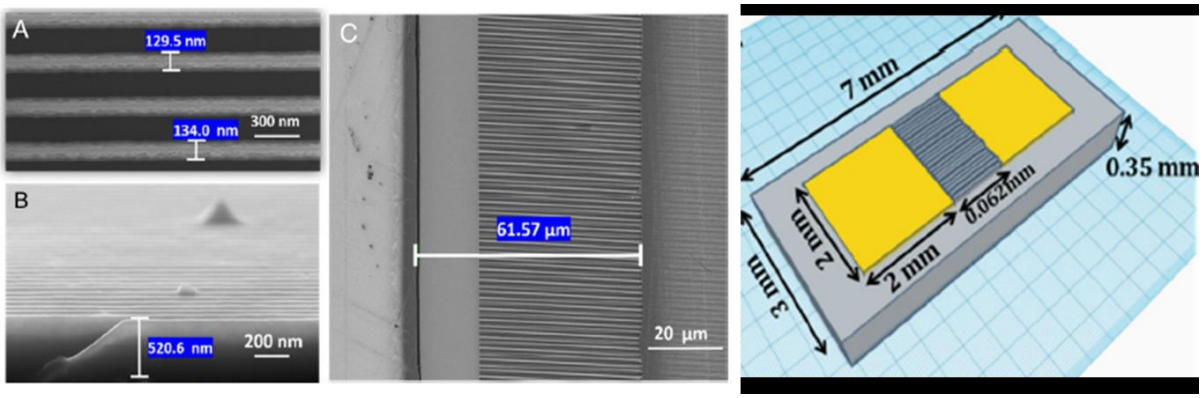

Figure 4.1.1: (Left) SEM images of nanostructure wall array on GaAs PCSS for increasing effective penetration depth and active volume to reduce on-state resistance with (A) being the top view, (B) the side view, and (C) a zoomed-out image of the nano-wall array. (Right) Illustration of GaAs PCSS device geometry with nanostructure wall array placement seen in the gap length of the device [4].

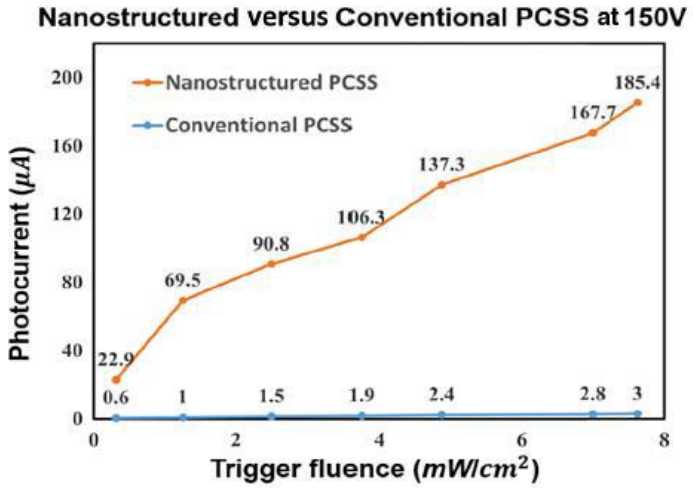

Figure 4.1.2: Photocurrent as a function of incident trigger fluence (energy per area) for a conventional and nanostructured GaAs PCSS showing the increase in photocurrent generated using the nanostructure addition to the devices [4].

System level parameters studied will include the operating circuit and incident photon source, which add additional cost and size to the overall system depending on the source

used. For the laser, the wavelength, energy (number of photons), operating frequency, and pulse width will be considered as these all affect efficiency and on-state resistance. An additional consideration towards minimizing on-state resistance without adding to incident laser energy, and costs, is the energy density and spot shape of the laser which is changed by keeping the laser energy and pulse width constant to maintain a steady average power. In the study mentioned in Zhang (2015) GaAs PCSS devices were used with an incident energy of 1 μJ and pulse width of 300 ns to obtain an average laser power of 33.3 W for varying spot shapes and energy densities as shown in Figure 4.1.3. It was found that the more focused shape, with the highest energy density, achieved the lowest on-state resistance (Figure 4.1.4) [5]. This finding shows that using additional optics to spread out the incident laser spot size to the entire active area may increase the on-state resistance of the device compared to using a focused, smaller spot size.

Table 1. Performance details of laser pulses.

spot shape	Size(mm^2)	Energy density($uJ.mm^{-2}$)
scattered	16.24	0.06
Long-striped	9.975	0.1
focused	0.5027	1.99

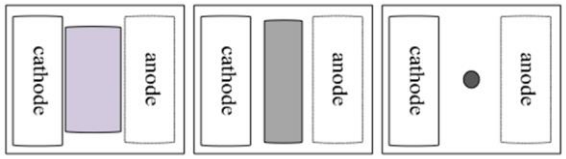

Figure 4.1.3: (left) Incident laser characteristics for incident laser power of 33.3 W with varying spot shapes and energy densities incident on the GaAs PCSS. (Right) Illustration of the various spot shapes used in the GaAs PCSS study.

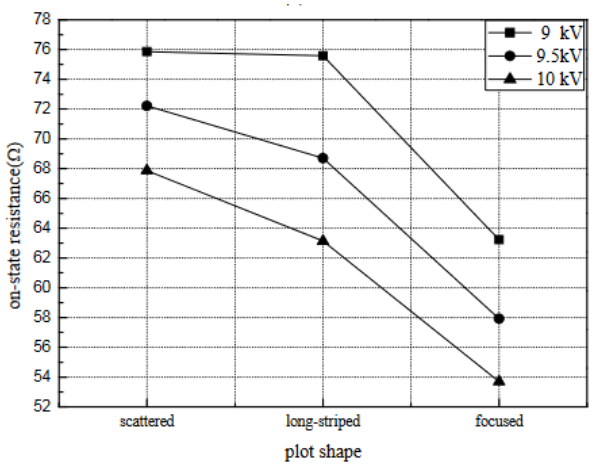

Figure 4.1.4: On-state resistance results from using different laser spot shapes and energy densities.

4.1.5 *Summary of Significant Findings and Mission Impact*

(A) Literature review continues towards determining changeable parameters to optimize on-state resistance in GaN PCSS, leading to a material option that provides improved efficiency and SWAP-C2 capabilities for a PCSS-based RF generation system.

Constraints:

- Linear mode due to minimal jitter operation and increased device lifetime.

- Intrinsic activation because of increased optical efficiency over extrinsic activation.
- Limited to lateral devices resulting from intrinsic mode constraint.

Changeable Parameters:

- Material and growth characteristics: doping concentration, substrate type and quality
- Device geometry: gap length, device area, interdigitated vs traditional linear, etc.
- Laser characteristics: incident wavelength, incident power (number of photons), energy density, and spot shape/size.
- Nano-structure topology: increasing active volume in the device to overcome on-state resistance minimization limitations due to shallow absorption depth of the photon source through utilizing an array of fins <1/2 the incident wavelength, to prevent scattering. This allows for improving optical efficiency without increasing the incident laser energy (number of photons) thus preventing increased laser costs and size. A similar study using GaAs PCSS devices showed an increase in photocurrent from 1.9 μA to 106 μA for a trigger fluence of 3.8 mW/cm^2 [1].

(C) A working GaN PCSS model has been created using both COMSOL Multiphysics and Silvaco TCAD to allow for parametric studies towards minimizing on-state resistance in GaN PCSS without the need for manufacturing several iterations of devices.

(D) Work towards a manuscript based on optimizing on-state resistance in GaN:C PCSS has been started with the first version of the introduction written and currently being edited.

4.1.6 *References*

[1] J. S. Sullivan and J. R. Stanley, “Wide bandgap extrinsic photoconductive switches,” *PPPS-2007 - Pulsed Power Plasma Sci. 2007*, vol. 2, pp. 1040–1043, 2007.

[2] A. D. Koehler *et al.*, “High Voltage GaN Lateral Photoconductive Semiconductor Switches,” *ECS J. Solid State Sci. Technol.*, vol. 6, no. 11, pp. S3099–S3102, 2017.

[3] G. B. Stringfellow, *Organometallic Vapor-Phase Epitaxy: Theory and Practice*. San Diego, CA: Academic Press, 1999.

[4] R. Liu, A. Shang, C.-J. Chen, Y. G. Lee, and S. Yin, “Nanostructure Enabled Lower On-State Resistance and Longer Lock-on Time GaAs Photoconductive Semiconductor Switches,” Opt. Letters, vol. 46, no. 4, pp. 825–828, 2021.

[5] Zhang, K. Liu, S. Gao, and Y. Shi, “Characteristics of GaAs PCSS triggered by 1 μJ laser diode,” IEEE Trans. Dielectr. Electr. Insul., vol. 22, no. 4, pp. 1991–1996, 2015.

5 Drift-Step-Recovery-Diode-Based Source Alternatives

5.1 Drift-Step Recovery Diode and Pulse Shaping Device Optimization

(Jay Eifler)

5.1.1 *Problem Statement, Approach, and Context*

Primary Problem: Drift-step recovery diodes (DSRDs) and DSRD-based pulsed power systems are competitive with PCSS-based systems for HPM cUAS, with the benefit of not requiring a laser. Maximizing peak power while maintaining characteristic ns-order DSRD rise times requires optimization of the DSRD device design and pulser. Other considerations are for compactness, low-jitter, cooling required, and additional pulse-sharpening device within the pulse shaping head circuit. Additional goals for pulse repetition frequency are also to be satisfied for various applications.

Solution Space: By altering DSRD device parameters (geometry, doping, irradiation), optimize single-die and stack designs for peak power and risetime within various inductive pulser circuit topologies. Also optimize the pulse sharpening device (PSD) within the pulse shaping head circuit.

Sub-Problem 1: TCAD and SPICE models of the DSRD are inaccurate and must be improved. PSD models have not been developed.

Sub-Problem 2: Inductive pulser designs are complicated by the DSRD (and PSD) parameter variability. Use TCAD and/or SPICE models to account for variability and improve pulser design.

State-of-the-Art (SOTA): MW peak power and ns-order risetimes have been achieved in DSRD-based pulsed-power systems employing DSRD stacks for higher voltage holding and parallel lines of DSRD to increase current. PSD have sharpened DSRD pulses to 100 ps-order.

Deficiency in the SOTA: A lack of accurate TCAD and SPICE models make design of DSRD and DSRD-based inductive pulser circuit topologies (with or without PSDs) difficult to the level of tens of MW of peak power while maintaining ns-order risetime (or sharpened 100 ps-order). In addition, DSRD (and PSD) fabrication variabilities further complicate pulser design.

Solution Proposed: Develop further modeling capabilities in TCAD and SPICE for DSRD and DSRD-based inductive pulser circuit topologies to optimize DSRD and inductive pulser designs, especially for maximum peak power and minimum risetime, but also for low-jitter, reduced cooling, and compactness. Additionally, optimize pulser with PSD and pulse shaping head circuit.

Relevance to OSPRES Grant Objective: DSRD-based systems eliminate laser requirements necessary for PCSSs and are competitive in terms of thermal requirements and peak power. With sharpening, the DSRD-based systems can produce comparable risetimes. The SWaPC^2 cooling requirements of HPM cUAS systems can be solved with DSRD-based pulsed power systems, and low-jitter DSRD-based systems can be used for beam-steering in phased-arrays.

Risks, Payoffs, and Challenges: DSRD must be arrayed and staged to increase current since DSRD are limited in their ability to operate at high current densities. DSRD and PSD must also be stacked to operate at high voltages necessary for high peak power and maintain low risetimes. The stacking methods can damage dies and produce variable results in risetime and DSRD diffused doping profiles can be difficult to achieve and may require epitaxial methods. SPICE device models for DSRD are unavailable and must be developed, and questions remain about TCAD limitations for DSRD and PSD modeling.

5.1.2 Tasks and Milestones / Timeline / Status

(A) Milestone – Develop DSRD SPICE model within SmartSpice using the CMC diode model (built-in and Verilog-A).

1. Task – Develop accurate forward IV, reverse CV and reverse recovery testing (RRT) modeling in CMC diode model using either built-in (faster) or Verilog-A (customizable) models; On-going [APR-JUN 2022];

2. Task – Develop reverse IV and forward CV modeling and parameters in SmartSpice CMC diode models (built-in and/or Verilog-A); Preliminary exploration [MAY-JUL 2022];

3. Task – Develop 1x1 DSRD-based pulser recovery parameters within CMC diode model of SmartSpice (built-in or Verilog-A) and compare to RRT parameters; On-going [APR-JUL 2022];

(B) Milestone – Complete LTSPICE parameterization of the standard diode model for DSRD inventory.

1. Task – Finish Gen2.2 DSRD LTSPICE parameter extraction; On-going as received [APR-MAY 2022];

(C) Milestone – Develop automated fitting procedures for developed LTSPICE and/or SmartSpice DSRD models.

1. Task – Improve speed/accuracy/size of brute force fitting methods for LTSPICE and SmartSpice diode models; On-going [APR-JUN 2022];

2. Task – Improve python-based fitting methods for diode models used in LTSPICE and/or SmartSpice; On-going [APR-JUN 2022];

3. Task – Improve use of SmartSpice Optimizer for parameter fitting of diode models; On-going [APR-JUN 2022];

4. Task – Develop automated fitting procedures for Verilog-A diode models (CMC or custom); Preliminary exploration [APR-AUG 2022];

(D) Milestone – Convert manufacturer PSPICE and PSPICE/LTSPICE unencrypted device models into SmartSpice format for use in DSRD-based pulser simulation.

1. Task – Convert unencrypted PSPICE/LTSPICE Cree MOSFET model into SmartSpice format; On-going [APR-JUN 2022];

2. Task – Convert unencrypted Texas Instruments Gate Driver model from PSPICE into SmartSpice format; On-going [APR-JUN 2022];

(E) Milestone – Develop DSRD parameters for new 371A semiconductor analyzer measurement data (forward IV and reverse IV).

1. Task – Develop standard diode LTSPICE 371A semiconductor analyzer measurement data parameters; On-going [APR-JUN 2022];

2. Task – Develop SmartSpice CMC (Verilog-A) 371A semiconductor analyzer measurement data parameters; On-going [APR-JUN 2022];

(F) Milestone – Determine performance of doping profiles within TCAD

1. Task – Determine TCAD performance of SOS, dynistor and thyristor doping profiles; Doping profiles not yet received; [?-? 2022];

2. Task – Determine TCAD performance of square root DSRD doping profiles; Not yet begun [? 2022];

3. Task – Determine TCAD performance of Gen3 manufacturer doping profiles; Not yet begun [? 2022];

4. Task – Determine recovery behavior of DSRD doping profiles within TCAD for development of custom Verilog-A CMC-based DSRD models; Not yet begun [?-? 2022];

5. Task – Determine effect of doping and defects on DSRD forward IV performance; Not yet begun [?-? 2022].

5.1.3 *Progress Made Since Last Report*

(A.1) Develop CMC Diode Forward IV and Reverse CV parameters

Automated methods for fitting forward IV and reverse CV for the CMC Verilog-A diode have been completed and applied with some success. The Verilog-A code for the CMC diode model has been successfully modified to allow different parameters for different voltage ranges of a forward IV which in turn allows experimental forward IV to be fit more accurately.

(B.1) LTSPICE Standard Diode Model Parameter Development for DSRD Inventory

Parameter extraction has been completed for Gen2.2 for the diodes that had good, multiple measurements.

(E.1-2) Develop forward IV parameters for 371A semiconductor measurement data

New 371 forward IV measurement data has been collected. The CMC Verilog-A code has been modified for more accurate fitting of the DSRD 371 forward IV and parameters are under extraction.

5.1.4 *Technical Results*

(A.1) Develop CMC Diode Forward IV and Reverse CV parameters

Previous fits for forward IV and reverse CV were done manually in some cases and used automated methods for the built-in CMC diode model. Automated methods for fitting forward IV and reverse CV in both the built-in and Verilog-A code versions has been

completed. The reverse CV were not fit too well with the new automated methods and more of the parameter space will be explored. Effort was shifted toward fitting the forward IV in the Verilog-A model and for the picoammeter and 371 measurement data to improve the pulser simulations within SmartSpice using the CMC diode model.

The difficulty is 371 measurement data for the 7-stack DSRD cannot be fit well with the diode equations in either the standard diode model or the CMC diode model. Tabulated diode models are one solution to fitting an experimental forward IV that is non-standard. The approach taken has been to modify the CMC diode Verilog-A code directly and allow for different parameters values for different ranges of voltage. The code has been modified successfully to generate forward IV using multiple parameter sets with testing in the pulser awaiting a more complete forward IV fit.

The fit that was accomplished included the picoammeter data (for EG1562) and the first data point of the 371 data (for EG1608) as shown in Figure 5.1.1. Fitting both the picoammeter data with any of the 371 data is the most difficult part of the experimental forward IV fitting. It may be much easier to fit the Gen2 1-stack data which preliminarily shows a linear RS region like the more standard higher voltage/current forward IV of a power diode. More higher voltage/current 371 data is still being collected on Gen2 and can serve as data to fit (as well as the EG DSRD). Also, the 371 data was never fit over its full range to high accuracy in the standard diode models within LTspice of SmartSpice. The modified CMC diode Verilog-A code also allows fitting of the 371 data over its full range by using different sets of parameters to fit the curve at different voltage ranges. These fits are still in progress in part due to a computational slowdown caused by a slow license verifying network. The EG1608 371 data has been fit throughout in sections that overlap for C-3 continuity concerns and must still be sequentially fit again for the final forward IV simulations, afterwhich reverse CV and testing in pulser simulations can be completed.

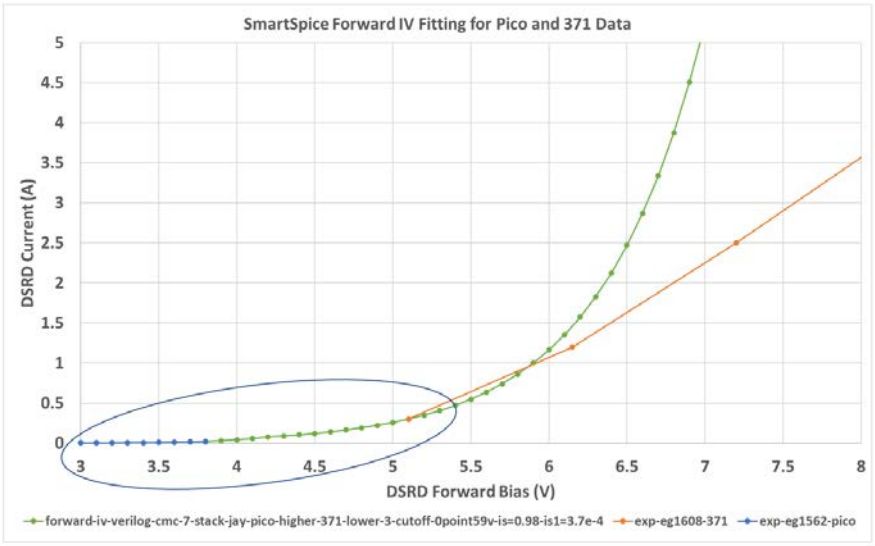

Figure 5.1.1. CMC Verilog-A diode fit to both picoammeter and 371 forward IV measurement data. This fit paves way for complete forward IV fitting.

(B.1) LTSPICE Standard Diode Model Parameter Development for DSRD Inventory

Experimental test data has been received for Gen2.2. Only two diodes had complete sets of good multiple measurements. A new fixture for forward IV has been made and testing shows that the pressure placed on the DSRD by the replaceable screw-in DSRD holder effects the forward IV and its serial resistance. The Gen2.2 DSRD forward IV clearly have a series resistance effect caused by the procedures used with older taped fixture. In Figure 5.1.2 can be seen the LTspice fitted forward IV compared to experiment for Gen2.2. The reverse CV and transit time have also been fit for Gen2.2 that had good multiple measurements (Gen2.2-d2 and Gen2.2-d6).

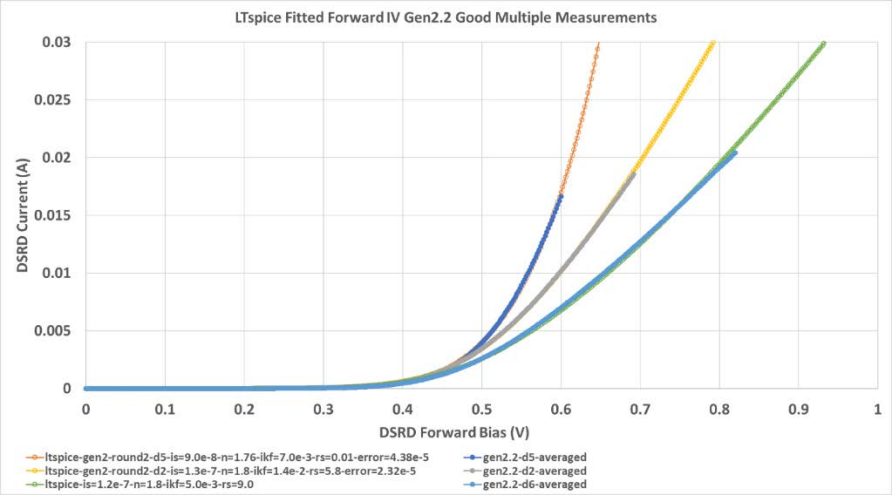

Figure 5.1.2. Fitted forward IV for Gen2.2 in LTspice.

5.1.5 *Summary of Significant Findings and Mission Impact*

(A) Development of DSRD Model Within SmartSpice CMC Diode Model

The SmartSpice circuit simulation software has been received in JAN 2022 and in FEB 2022 the Verilog-A CMC diode code was retrievable from the Si2 organization website. Development immediately began of the CMC diode model for DSRD modeling by producing forward IV, reverse CV and reverse recovery testing simulations and fitting to example DSRD in the inventory. Recovery parameter fitting within the 1x1 DSRD-based pulser has also begun. The capability of the CMC diode model for modeling DSRD can now be assessed. Any deficiencies in the CMC-DSRD model can be improved using the programmable Verilog-A code of the CMC diode model to include DSRD specific modeling equations based on theory, TCAD simulation, experiment and the literature. The Verilog-A code has been modified to allow different fitting parameters for different sections of the curve so that real, experimental forward IV can be accurately fit. Improved forward IV fitting in the Verilog-A CMC diode model will allow for improved pulser simulation.

(B) LTSPICE Standard Diode Model Parameter Development for DSRD Inventory

DSRD in the inventory of received diodes (legacy, EG and Gen2) have been fit for LTSPICE standard diode model parameters (for forward IV, reverse CV and reverse recovery testing) for use in LTSPICE DSRD-based pulser simulations and to provide another metric for the characterization of the DSRDs in comparison to pulser performance. Some details of the very low voltage and current forward IV have not been fit but the fitting is still very close when visually inspected in non-log format. Reverse IV have not been fit in the standard diode model since it cannot capture the behavior and breakdown has not yet been measured, only estimated. Forward CV measurement are problematic and not fit mostly since the forward CV parameters in the standard diode model are used for recovery modeling. Various methods exist in LTSPICE to improve recovery parameter fitting but are either inadequate (Vp or carrier viscosity) or non-realistic (adjustment of reverse CV parameters) but have produced fits within 10% error for DSRD-based pulser performance. Gen2.2 experimental data has been received fitted within LTspice but there is high, variable series resistance in the Gen2.2 measurements that are being addressed with a new fixture and testing.

(C) Develop Automated Fitting Procedures for LTSPICE and SmartSpice

The current best method of fitting is using a brute force method of running LTSPICE or SmartSpice simulations sweeping over the desired parameter space. The brute force method can produce the most accurate fits but requires long simulation times and cannot be used to explore large parameter spaces easily (which is why more physically-based models using only measurable parameters is derisable). There is ultimately a limit to how quickly and accurately one can develop parameter sets. Another method is to program in the model equations into Python and use their curve fitting tools, however this method cannot incorporate circuit simulation and will therefore be less effective in producing accurate fits but is much faster in simulation time (can depend on how much parameter adjustments affect DSRD-based pulser performance on which method to use). The other fitting method is to use the built-in optimizer within SmartSpice, but the optimizer has not yet produced as good of fits consistently as the brute force method and will take some experience in using well.

(D) Conversion to SmartSpice of Manufacturer Device Models

Unfortunately, manufacturer device models are not openly available in SmartSpice only PSPICE and to some extent LTSPICE (usually converted from PSPICE). Therefore, the available PSPICE and PSPICE/LTSPICE models must be converted to the SmartSpice format, otherwise keeping the model the same. Note that encrypted models cannot be converted into SmartSpice, such models either have to be developed from scratch and either the datasheet or additional experimental tests used (or purchased from Silvaco for SmartSpice if available).

The unencrypted Cree MOSFET model has been converted into SmartSpice and tested within 1x1 DSRD-based pulser simulations and compared to LTSPICE simulations successfully. The unencrypted Texas Instruments gate driver model has also been converted into SmartSpice successfully. One issue with the driver model is it is intended for PSPICE but used often in online discussion in LTSPICE. However, close examination of the model shows that the model cannot perform correctly in all pin conditions in LTSPICE due to incorrect parameter types used in a voltage-controlled switch within the

driver model. The voltage-controlled switch has been correctly implemented in the SmartSpice conversion and can be fixed for the LTSPICE version (Texas Instruments has not responded to inquires). Neither the MOSFET or gate driver models have been extensively diagnostically tested and compared to the datasheets which are often somewhat different to the free provided models (only so accurate).

(E) IV Parameter Development for 371A Semiconductor Analyzer Measurement Data

A 371A semiconductor analyzer has been acquired and setup for forward IV testing with the potential for higher voltage/current reverse IV testing and breakdown. Initially concerns arose about the shape of the forward IV and whether temperature distortion was occurring at the higher voltages and current available with the 371A compared to the picoammeter. However, published power diode forward IV have been discovered showing similar forward IV at room temperature. 371A testing will proceed by testing more DSRD and subsequently using thermocouples and/or heat sinks. 371A higher voltage/current forward IV testing is necessary to characterize the DSRD in the diode models to perform correctly in the DSRD-based pulser simulations. How accurate the forward IV must be, has not been determined, as well as, to what extent individual diodes can be reliably distinguished in modeling. A new method for fitting forward IV has been implemented in the CMC Verilog-A diode modeling code that will allow for more accurate fitting of the 371 data for its full range.

(F) TCAD-Based Doping Profile Performance Evaluation

Many DSRD TCAD simulation studies have been performed assessing the doping profiles used for the DSRD manufactured by SPT and in stock (this summary includes work from the past six months). The TCAD modeling has been temporarily on hold as effort is focused toward developing an accurate SPICE DSRD model due to the unavailability of manufacturer device models for MOSFETs and gate drivers within TCAD. A MOSFET model was developed for the Cree MOSFET for use within TCAD but still had some differences when used in pulser simulations, so the development of the DSRD SPICE model was prioritized so that manufacturer models (for MOSFETs and drivers) could be used.

Doping profiles are forthcoming for various SOS, dynistor and thyristor devices and TCAD will be used to assess their performance. Some interest has been expressed in assessing square-root doping profiles for DSRD. Gen3 doping profiles from the manufacturer have yet to be assessed within TCAD for performance differences with the requested doping profiles. As well, the recovery models within the CMC diode model are themselves based on PIN diode TCAD simulations and TCAD can perform DSRD doping profile specific simulations to determine model equations and parameters. Additionally, the forward IV behavior of our DSRD can be modeled as seen in the 371A semiconductor analyzer mesaurements. TCAD modeling will continue to be of use in device modeling since it is the only way to assess doping profiles.

5.1.6 *References*

[1] Chandra Bose, JV Subhaus, I. Imrie, H. Ostmann, and P. Ingram. “SONIC-A New Generation of Fast Recovery Diodes [D].” IXYS Semiconductor (2011).

5.2 Pioneering Drift-Step Recovery Diode Processing and Manufacturing

(Alex Usenko)

5.2.1 *Problem Statement, Approach, and Context*

Primary Problem: DSRDs have not increased in performance since the 1960's due to reliance on deep diffusion manufacturing. Their voltage-to-risetime, dV/dt, remains about 10^{12} V/s. To achieve the 10^{13} V/s (10 kV/ns) voltage-to-risetime required by an all-solid-state HPM pulse generator in support of the Naval afloat mission, improving DSRD manufacturing techniques is critical.

Solution Space: Leverage applicable concepts from the mainstream silicon chipmaking industry and apply new manufacturing methods to DSRD processing.

Sub-Problem 1 – Diode silicon surface termination/passivation: The SOTA uses diode termination by a vertical wall. This design results in low breakdown voltage as it is limited by surface breakdown. To increase the diode breakdown voltage to closer to that of the bulk silicon breakdown voltage value, the vertical side wall design must be avoided.

Sub-Problem 2 – Stacking of DSRD dies: The SOTA is based on soldering of diode dies into a stack, which limits the stack lifetime to below 10^{12} pulses. Also, the SOTA did not apply the methodology of stacking wafers first, then cutting into dies. Switching to wafer level stacking will decrease the number of stacking operations by more than 100x.

Sub-Problem 3 – Packaging of stacked dies: *The* SOTA uses bare stacked DSRDs. Mounting the bare stack into a press-pack type package will improve long-term stability, such that the stack will survive a much higher number of pulses before it burns out.

State-of-the-Art (SOTA): In a recently published paper (2019),[1] the Russian St. Petersburg team at the Ioffe institute reported achieving a peak current density of 5 kA/cm^2 with a rise time of the output pulse front of ~2.3 ns, and a peak voltage across the load of 900 V (i.e., the peak switching power is 4.5×10^6 W/cm^2). The St. Petersburg team utilized deep diffusion technology. A competing team at Ekaterinburg, Russia [2] reports similar pulse performance. Both teams use outdated deep diffusion technology. As one can see, there has not been any significant improvement in DSRD pulse performance since the pioneering work done in 1960 [3].

Deficiency in the SOTA: First, no DSRDs have been manufactured using epitaxy technology with doping profile optimization. Second, no DSRD processing method exists that integrates side passivation with silicon dioxide. Finally, an acceptable DSRD stacking process has yet to be developed.

Solution Proposed: Manufacture DSRDs within the continental United States using an epitaxial growth process leveraging the optimal characteristics (e.g., doping profile, carrier concentration) determined through the work performed by our simulation team (previous chapter of this report) and through working with industry partners at Semiconductor Power Technologies (SPT), Livermore Semiconductor Research Laboratories (LSRL) and Lawrence Livermore National Laboratory (LLNL – Voss Group).

Relevance to OSPRES Grant Objective: DSRD manufacturing technology is a major building block of short-pulse high-peak-power defense systems. Our new disruptive process flow for DSRDs enables not only manufacturing of DSRDs at scale, but within the continental United States (CONUS). In doing so we will redefine the SOTA by producing optimal DSRDs. Further, DSRDs will be used within best-in-class HPM pulse generators which become part of more advanced defense systems within the Navy arsenal.

Risks, Payoffs, and Challenges:

Risks: As the process of producing DSRDs using epitaxial growth with doping profile design is novel, uncharted territory, there is inherent risk to its success. Additionally, post-processing methods based on the discussions provided in the ***Sub-Problems*** section are not well-established.

Payoffs: Replacing traditional deep diffusion technology with a new process integration scheme would allow better DSRD pulse performance. Electrical breakdown voltage, reliability, and lifetime are expected to increase, and rise time on a load is expected to decrease.

5.2.2 Tasks and Milestones / Timeline / Status

(A) Milestone – Produce epitaxial DSRDs that contain optimal exponential doping profiles and carrier concentrations /estimated JUN*22*.

1. Task – Design of experiment on 25 wafers through negotiations with vendors / *MAY–JUL21* / Completed
2. Task – Perform DSRD stack epitaxy on 13 wafers at SVM Inc., and 25 wafers at LSRL / *JUN–AUG21* / Completed.
3. Develop process integration scheme that uses epitaxy instead of deep diffusion / *JUL–OCT21 /* Completed.
4. Compare traditional DSRD technology and suggested integration scheme. List disadvantages of traditional processes and define potential advantages of new processes / MAY–NOV21 / Completed.
5. Run Gen2 and Gen3 lots. Gen2 is on wafers with epi from SVM, Inc., Gen3 is on wafers with epi from LSRL. Gen2 uses the same BEOL as Gen1. Run BEOL of Gen3 – using our new patented processing scheme – TMAH etch, oxidation, selective electroless metal deposition, wafer bonding, sawing into diode stacks / OCT21–MAY22.
6. Submit Gen2 and Gen3 diode lots to UMKC team for pulsed performance measurements; collaborate with team on determining optimal doping profile through DoE (design of experiments) analysis by Minitab software / OCT21–MAY22.

(B) Milestone – Develop diode separation technique while keeping wafer integrity / Estimated completion FEB22.

1. Design lithography masks for short loop experiment, submit order to vendor. / MAR–APR21 / Completed.
2. Design short loop experiment for V-groove etching for diode separation. / MAR–APR21 / Completed.
3. Run short loop experiment for the diode separation by anisotropic etch; analyze results / MAY–OCT21 / Completed.
4. Based on results of previous short loop run, adjust equipment, and process recipes to achieve sufficient etch uniformity across the wafer. Run on updated equipment and recipe to prove etch uniformity. / Completed.
5. Design lithography masks for epi DSRD run; submit order to vendor. / OCT21 / Completed.
6. Run Gen3 lot through V-groove etch step, transfer lot to next process step. / Estimated MAY22.

(C) Develop Ohmic contact deposition technique integrable with epitaxy, diode side termination/passivation, and wafer bonding steps / estimated AUG21 - MAY22.

1. Design short loop experiment to determine technical feasibility of selective electroless deposition of metal stack as a method of Ohmic contact forming in the DSRD process integration scheme. / OCT21 / Completed.
2. Determine vendor from which to order electroless deposition kits; obtain quotes, order, receive the kits. / OCT21 / Completed.
3. Run short loop experiment – nickel-copper-tin stack electroless deposition on a blanket wafer. Analyze results. / DEC21 / Completed.
4. Develop process recipe for the metal stack deposition to use in Gen3 DSRD lot manufacturing / estimated JAN22.
5. Run the selective metallization step on Gen3 lot; transfer the lot to next processing step. / Estimated FEB22.

(D) Develop wafer stack bonding technique integrable with the rest of Gen3 process flow / estimated SEP–FEB22.

1. Design short loop experiment for bonding 2 diode dies with Ni-Cu-Sn layers by solid–liquid interdiffusion. / SEP21 / Completed.
2. Run 2 dies short loop experiment. Analyze results. / MAR22 / Completed.
3. Test technical feasibility of multiple wafer bonding by bonding 10-wafer stack / estimated APR22.
4. Upon proof of technical feasibility of 10-wafer stacking, develop process recipe to use for processing of Gen3 DSRD lot / estimated MAY22.
5. Run wafer bonding step on Gen3 lot, transfer the lot to next processing step. / Estimated MAY22.

(E) Develop wafer stack sawing technique into DSRD stacks, integrable with the rest of Gen3 process flow / estimated NOV21–MAY22.

1. Design sawing process using Disco saw available at Semiconductor Power Technologies for cutting 10-wafer stack / estimated JAN22.
2. Run short loop cutting of blanket bonded 10-wafer stack. Analyze results. / Estimated FEB22.
3. Develop process recipe for Disco saw tool to use for Gen3 lot. / Estimated MAY22.
4. Run sawing step on Gen3 lot / estimated MAY22

(F) Develop diode side passivation process integrable with the rest of DSRD process flow.

1. Test compatibility of thermal oxidation for the diode side passivation with preceding anisotropic etch step / estimated FEB22.
2. Alternative diode side passivation process: design short loop experiment on room temperature oxidation by forming porous Si film and oxidizing the porous film / APR–OCT21 / Completed
3. Run part of Gen3 lot using the oxidized porous Si as diode side passivation / estimated FEB22.
4. Second alternative diode side passivation process: Design short loop experiment on room temperature oxide deposition from oversaturated fluorosilicic acid / estimated MAY–JAN22.
5. Run part of Gen3 lot using the oxidized porous Si as diode side passivation / estimated FEB22.
6. Choose the best from 3 methods of diode side surface passivation techniques / estimated FEB22.

(G) Develop a DSRD process based on out-diffusion (opposite to traditional in-diffusion process).

1. Process Gen4 lot based on process integration scheme described in our patent application filed in / estimated MAY22.

(H) Find vendor that manufactures press-pack parts, order the parts, and encapsulate the DSRD stacks into the press-packs / estimated MAY22.

5.2.3 *Progress Made Since Last Report*

(A5) Gen3 lot fabrication. Re-processing of 22 wafers left in the Gen3 lot has been arranged with Noel Technology, and a quote obtained. A new inspection tool has been added to the cleanroom facility at Kansas State University, Manhattan, KS: a bright light inspection tool. All 22 wafers left in the Gen3 lot have been analyzed with the new tool, and the number of pinholes in the defective nitride layer have been

counted; the best wafer has 10 pinholes, the worst one 200 (more than 1 per die, so expected yield 0% from this wafer—definitely needs rework).

(A5) Gen2 lot fabrication. The disco saw tool is now fully repaired and up; the remaining wafers are being singulated into dies. A new die bonding process called solid–liquid interdiffusion (SLID) continues to be developed, to replace traditional soldering/eutectic bonding.

(B4) Process step development: die separation on wafers by anisotropic etch in TMAH (tetramethylammonium hydroxide) based bath. Last month we found a new TMAH/DMSO (dimethyl sulfoxide) mixture etch chemistry which shows much better etch uniformity compared to all known TMAH/IPA or TMAH/surfactant chemistries. This month we determined the process window for our production recipe — 1:1:1 TMAH/DMSO/water mixture. The recipe was found to have a wide process window, thus high production yield is expected.

(D2) Process step development: stacking. Single diode dies have been successfully bonded using SLID (solid-liquid interdiffusion) technology. The bonded assembly was analyzed by SEM and found to have much thinner metal layer thickness compared to known eutectic or soldering processes.

(G1) Out-diffusion version of DSRD process. Sample p++ and n++ wafers were processed in-house in our diffusion furnace. The doping profiles after out-diffusion were measured by SRP. An argon + hydrogen anneal still shows lower than calculated diffusion. An exact copy of Intel's 1999 run (pure hydrogen) is planned.

5.2.4 *Technical Results*

(B) **Gen3 lot fabrication.** We have obtained a quote from Noel Technology and arranged stripping of defective silicon nitride layer, depositing new nitride, and lithography over the nitride. To ensure quality of processing, recipes of inspection steps at Noel have been audited and found to be sufficient. The cycle at Noel is expected to be completed in one month.

(B4) **Anisotropic etch step development**. Previous month we have developed new recipe for v-groove anisotropic etch. The new recipe allowed complete suppression of hydrogen bubble sticking to wafer surface, thus shown much better etch uniformity across the wafer and much lower roughness of the silicon surface after the etch. This month we carried out a short loop run to experimentally prove that our new etch recipe has a wide process window – so we can reliably get the desired triangular shape v-grooves even if process time and bath temperature has some variations.

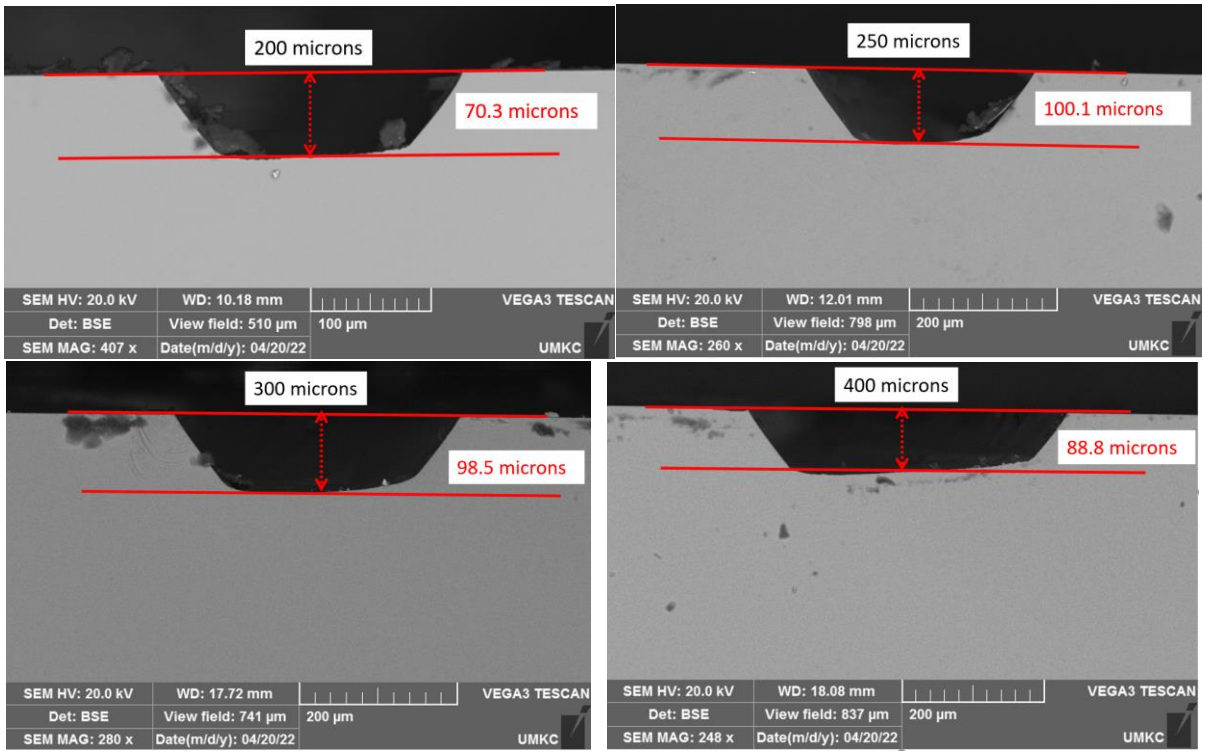

Figure 5.2.1. V-groove shapes after etching in a standard TMAH etch recipe – 1:2 25% TMAH mixture with deionized wafer, bath temperature 80C, 16 hours etch time. Courtesy Shailesh Dhungana.

Fig.5.2.1 and Fig.5.2.2 give a comparison of the v-groove shapes after a standard TMAH etch recipe and after our new modified recipe. In both cases the wafers were covered with 200 nm thermal oxide mask, and windows in masks were formed by lithography and etching in diluted HF. The lithography mask is designed to have different window widths – 200, 250, 300, and 400 microns. Thus, if all 4 different width v-grooves can be obtained with the same recipe, it means that the process has wide window and, consequently, will have a high manufacturing yield.

Indeed, Fig. 5.2.1 shows an incomplete v-groove etch – truncated shape and more than 30% variation in the groove depth – from 70 to 100 micron, thus using the well-known recipe will not result in a robust high yield process.

Oppositely, v-groove shape after etching in our new modified recipe - Fig. 5.2.2 – shows near perfect triangle shaped v-grooves for all 4 groove sizes. This means, that even not precisely controlled processing – with 50% variation in etch time, or with ±10^{o}C variation in bath temperature (temperature change by 10^{o}C results in 2X change in etch rate) still will result in 100% yield at v-groove etch step.

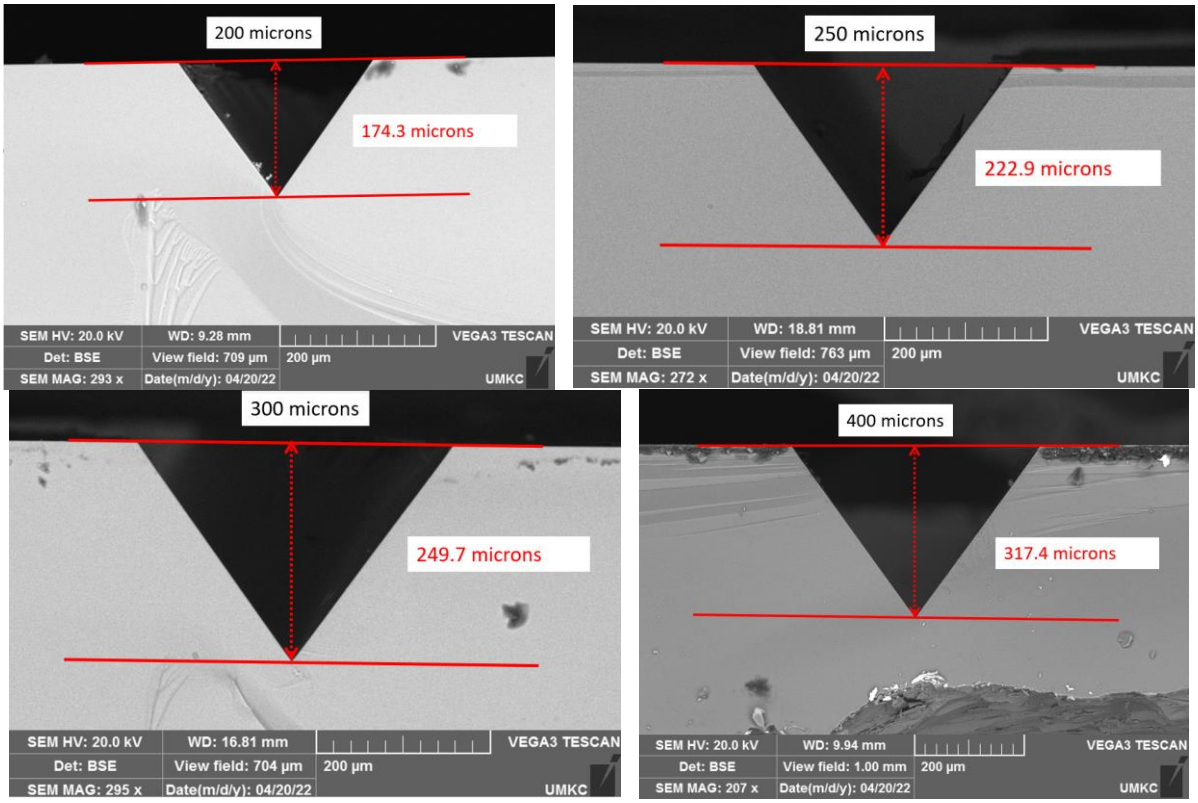

Figure 5.2.2. V-groove shapes after etching in a modified etch recipe – 1:1:1 25% TMAH mixture with DMSO (dimethyl sulfoxide) and deionized wafer, bath temperature 80C, 16 hours etch time. Courtesy Shailesh Dhungana.

(D2) **Die stacking development**. This month we have analyzed samples that are bonded with SLID (solid-liquid interdiffusion bonding) technology [4]. The SLID is expected to give much thinner metal layers between the bonded silicon dies as compared to bonding techniques traditionally used for DSRD stacking – like soldering or eutectic bonding. The thinner metal layers further expected to lower mechanical stresses in the bonded sandwiches upon thermal cycling. Even further, the low stresses results in less cracking in metal or in silicon, thus better DSRD reliability and longer service time. Other advantages stemming from the thinner metal layers are less number and smaller size voids, and lower probability of electrical shorts by metal squeezed out from a space between silicon dies. By using the SLID, about an order of magnitude thinner metal layers are expected – micron-size thicknesses, while soldering or eutectic gives tens of microns metal layer thickness.

The following metal stacks were deposited onto top and bottom Si die surfaces. On the top die side, 500 Ångström of Aluminum, then 1000 Å of Titanium, then 10 kÅ of Copper, then 5 kÅ of Tin have been deposited. On the bottom die side Ti(1000Å)/Cu(10kÅ)/Sn(5kÅ) stack have been deposited. All depositions were performed in a vacuum chamber using electron beam evaporation of metals. The metals needed for the SLID are Copper and Tin only. On the top – polished silicon wafer side - Al and Ti were added below the Cu/Sn just ensure strong adhesion and good Ohmic contact. Al makes good adhesion to polished Si surface, and Ti makes Copper well adhered. On

back die side, surface is etched, not polished, thus it has enough roughness to directly adhere Ti; therefore, the Al layer skipped.

The dies with the metal stacks were attempted to stack by SLID-bond Tin-to-Tin. In a first attempt, 1x1 cm dies were put into an oven and pressed together with 1kG weight. Due to the SLID process, the die assembly must be heated above Tin melting temperature 232°C. Target oven temperature was put on 250°C. Upon the Tin melting, the Tin start dissolving Copper due to a solid-liquid interdiffusion phenomena. It creates several CuSn intermetallic compounds - from Cu_3Sn to Cu_6Sn_5 – all having melting temperature above 500°C. Therefore, there no significant thickness of liquid metal at any point of the SLID process (advantage over eutectic or soldering). The SLID continues until all Tin consumed – therefore deposited Cu thickness have been chosen twice thicker than Sn.

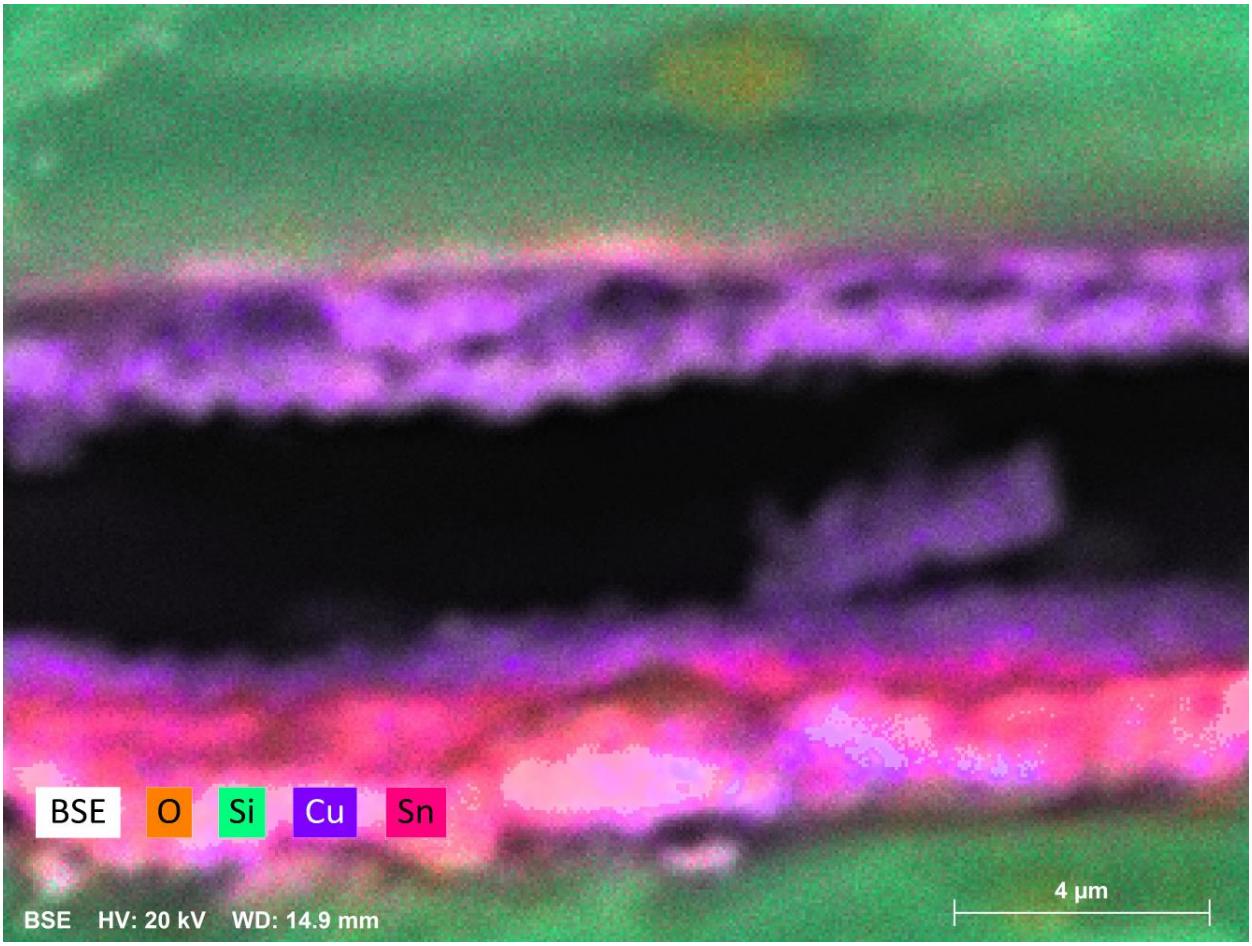

Figure 5.2.3. SEM cross section of bonding area between two silicon dies, bonded by SLID process – unsuccessful attempt. Courtesy Shailesh Dhungana.

Fig.5.2.3 is a SEM cross section of the bonded die assembly. The total thickness of a layer between the silicon dies (green on the pic) is roughly 10 microns, which is significantly thicker than expected 50 nm Al + 100 nm Ti + 1000 nm Cu + 500 nm Sn + 500 nm Sn + 1000 nm Cu + 100 nm Ti = 3.25 microns. Also, a black gap is visible between

the SEM-recognize-colored elements. We suppose the black band is a bonding void, so the SLID bonding failed here.

Before the second SLID bonding attempt, we have analyzed some potential causes of the failure, and ways to achieve successful bonding. The main suspect is that the Tin surface get oxidized in air, and the oxide film prevents the liquid interdiffusion Cu-Sn. To resolve the issue, literature suggests either using a flux (here – formic acid fume) or increase bonding pressure – so the ductile Tin will break the thin oxide. We use the second approach: use a c-clamp. Upon heating in the oven, the c-clamp develops additional pressure on the die pair being bonded.

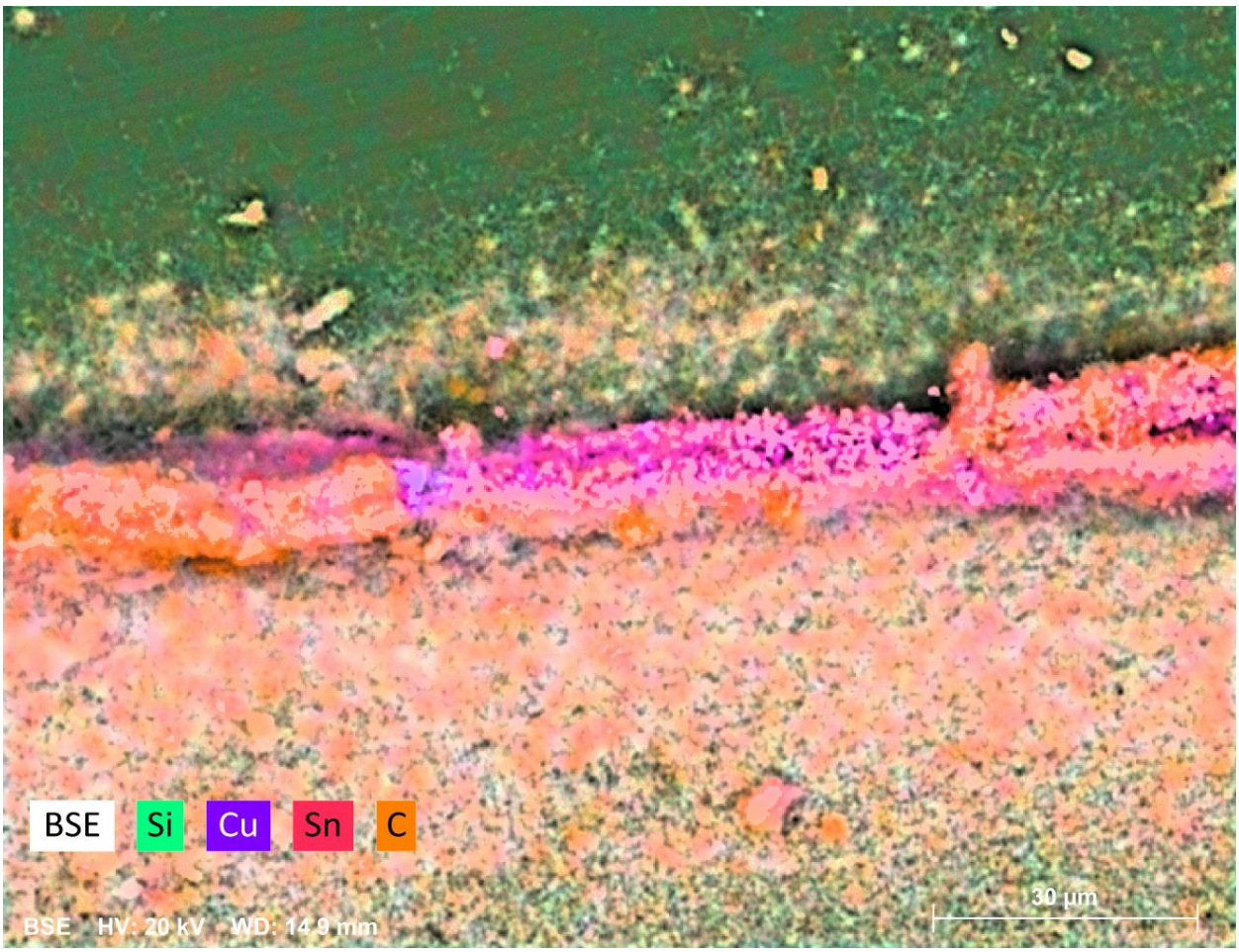

Figure 5.2.4. SEM cross section of bonding area between two silicon dies, bonded by SLID process – successful attempt. Courtesy Shailesh Dhungana.

Fig. 5.2.4 shows the similar cross section as the previous Fig. 5.2.3 but using the c-clamp. As one can see, the black gap disappeared meaning successful bonding. There are also visible some quite thick yellow colored (carbon) areas, quite asymmetric – mostly in the bottom silicon die side. We do not understand this well yet: if it is just contamination, it will likely be symmetric. But the Copper and Tin colored area have total thickness about 4 microns, which fits well to estimated total thickness of the metals deposited – 3.25

microns. That is the major result confirming technical feasibility and advantages of using SLID technology to replace eutectic bonding and soldering for the DSRD stacking.

5.2.5 *Summary of Significant Findings and Mission Impact*

(A) Several process adjustments have been implemented in processing of next Gen2 die lots. Die-to-die excessive variability is noticed. Process recipes and some equipment have been adjusted to achieve better uniformity and repeatability.

(B) Improving side termination of diodes. To prevent detrimental non-uniformity due to hydrogen bubbles sticking to wafer surface, a new process recipe has been developed. TMAH/DMSO mixture showed excellent uniformity. Using this mixture for anisotropic silicon etch never described in literature, we found this first.

(C) Replacement of unreliable metal contact deposition technique (by electron beam sputtering in vacuum chamber). Technical feasibility run on direct electroless plating of the Palladium/Nickel stack was successful. Process recipe developed for next run, plate uniform stack of Pd/Ni/Cu/Sn. State of the art electroless plating tool being donated by Hughes Research Lab.

(D) A process recipe for side passivation of diodes using a stain etch has been developed. The thickness uniformity resulting from the stain etch technique has been drastically improved. A new recipe that totally suppresses hydrogen bubbles sticking to the Si surface was found. Using that recipe, very uniform thickness (porous Si) films were successfully grown on blanket silicon wafers with both low and high doping levels.

5.2.6 *References*

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5.3 Characterization of SOS Diode Performance through DOE Augmentation

(Ethan Bozarth, Joseph Reeve-Barker, & Megan Hyde)

5.3.1 *Problem Statement, Approach, and Context*

Primary Problem: Drift step recovery diodes (DSRDs) are planar diodes that are capable of nanosecond, high-frequency (10–10^3 kHz) pulses [1] with applications as opening switches in inductive energy storage (IES) pulse generation circuits. There is not a clear understanding of the effects DSRD parameters have on overall IES pulser performance. The purpose of this project is to tie the DSRD parameters to its tailored performance requirements.

Solution Space: Leveraging both design of experiment (DOE) and machine learning (ML) capabilities, we will develop a methodology of characterizing and optimizing DSRDs in order to provide fabrication recommendations in the context of application targets.

Sub-Problem 1**:** We do not yet understand how diode parameters are tied to diode performance.

Sub-Problem 2: There is no standardized method for correlating the diode key performance indicators (KPIs) to the IES pulser generator performance.

Sub-Problem 3: The number of possible inputs for the DOE is expected to be too large, so ML will need to be leveraged in order to guide decision-making processes.

State-of-the-Art (SOTA): Standard diode measurements include curve tracers for forward and reverse IV, impedance spectroscopy for forward and reverse CV, and function generators or, for example, the Avtech pulser for reverse recovery with high voltage and/or high current when necessary. These measurements are used to generate commonly available datasheets for COTS diodes. These standard diode measurements can then be correlated to pulser performance using traditional data analytics.

Deficiency in the SOTA: The standard diode measurements and datasheets do not include pulser performance necessary to evaluate DSRDs. The datasets generated with doping profile assessment (for example spreading resistance profiling), standard diode measurements and pulser performance are too large and complex to leverage traditional data analytics and will benefit from machine learning techniques.

Solution Proposed: Develop a holistic evaluation network to characterize the KPIs of DSRDs. This network will include a DOE that will be a continuously evolving model as new KPIs are discovered. Augmenting the DOE will ensure that the model will remain relevant throughout this study as more discoveries are made. Machine learning will be used as the primary decision-making tool for augmenting the DOE. Once the network is established, it will be used to outline the optimal parameters for stacks of DSRDs within an IES pulse generator.

Relevance to OSPRES Grant Objective: Bridging the gap between the theoretical and physical performance of DSRDs enables closing the gap between a low fidelity TRL3 breadboard pulse generation system, and one which is at a high fidelity TRL4 prototype level. At the TRL4 level, the DSRD-IES pulse generator system would be sufficient to replace the costly laser-based Si-PCSS HPM generator without compromise to scalability required to support the Naval afloat mission.

Risks, Payoffs, and Challenges:

Challenges: Traditional predictive analytics will be difficult to correlate with the augmented DOE due to the large volume of data. Machine learning is expected to assist with decision making processes for the DOE, but only if the proper KPIs have been established and good data have been used to train the machine learning model.

5.3.2 Tasks and Milestones / Timeline / Status

(A) Milestone – Establish preliminary DOE and standard operating procedure (SOP) for identifying KPIs of DSRDs [*estimated completion by MAR22*].

1. Task – Ascertain current KPIs used to optimize diodes simulated, manufactured, and utilized within the IES pulse generating circuit [completed AUG21];
2. Task – Construct preliminary DOE to acquire data on all KPIs based on Task 1 [*completed FEB22*];
3. Task – Leverage existing Python scripts to process legacy DSRD KPI data [*completed SEP21*];
4. Task – Develop new and review existing SOPs for experimental testing apparatuses used to evaluate individual KPIs and measure their performance [*completed OCT21*];
5. Task – Identify gaps/deficiencies in legacy KPI data, evaluate existing theoretical relationships to bridge gap and minimize DOE if possible [*completed OCT21*];
6. Task – Using SOPs developed in Task 4, acquire experimental data from legacy DSRDs, refine SOP(s), and assess repeatability and reproducibility [*In progress*: *SEP21–MAR22*];

(B) Milestone – Evaluate DSRD performance using the developed SOPs and facilitated by the preliminary DOE [*estimated completion JUL22*].

1. Task – Acquire data on newly manufactured 2nd generation epitaxial DSRDs from Section 5.2 using refined SOPs from Milestone A [*completed JAN22*];
2. Task – Evaluate the precision and power of the DOE [*In progress*: *MAR22–JUL22:*];
3. Task – Develop a DSRD selection guide for the pulser circuit based on the static DC test measurements *[In progress: MAR22–MAY22];*
4. Task – Correlate the static DC test measurements to the performances of the IES pulser circuits and to fabrication procedures [*MAR22–JUN22];*
5. Task – Begin training machine learning model with DSRD data to determine correlations between static DC and pulser testing results [*MAY22–JUL22*];
6. Task – Acquire data on newly manufactured 3rd generation epitaxial DSRDs from Section 5.2 using refined SOPs from Milestone A [*JUL22–SEP22*];

(C) Milestone –DSRD diode network evaluation [*on hold until Milestone B is completed*].

1. Task – Refine Python script to incorporate new correlations based on findings from Milestones A&B [*Est. Summer22*];
2. Task – Amend ML training model with data acquired on new DSRDs (as characterized by Sections 5.1–5.2) to investigate statistical correlation of diode performance [*Est. Summer22*];
3. Task – Work with TCAD simulation team to address discrepancies between the DSRD performance obtained experimentally, and that achieved within simulations [*Est. Summer22*];

4. Task – Collaborate with DSRD manufacturing team to address discrepancies between the DSRD characteristics evaluated experimentally, and that desired by manufacturing process [*Est. Summer22*];
5. Task – Investigate relationships between statistical significance of individual diode KPIs to the peak performance of the IES pulser with the pulse generator team. [*Est. Summer22*];
6. Task – Incorporate findings from Tasks 1–5 into ML model, pinpoint KPI correlations of interest, and provide recommendations to IES sub-teams accordingly [*Est. Summer22*];

(D) Milestone – DSRD diode network evaluation [*on hold until Milestone C is completed*].

1. Task – Augment DOE network to streamline diode evaluation and identify checkpoints/gaps within simulation, manufacturing, and circuit development process to ensure optimal diodes are selected and utilized to produce robust high-fidelity IES pulse generator prototypes [*Est. Fall22*].

5.3.3 *Progress Made Since Last Report*

(A.6) The measurement results of the first six rounds (Table 5.3.1) were processed for all three static DC tests (forward and reverse current-voltage and capacitance-voltage) by three operators. Each diode was tested three different times by three different operators (e.g., 9 tests per diode). The forward current-voltage measurements were evaluated for repeatability, and showed large variations due to the sample fixture (refer to Table 5.3.2 in the Technical Results section. A new press pack fixture was proposed as a viable solution to the measurement variation.

	Round 1	Round 2	Round 3
Deep Diffusion 7 Stack	D1	D319	D333
Deep Diffusion Untested	630	657	801
Epitaxially Grown 1500	1562	1563	1564
Epitaxially Grown 1600	1601	1602	1603
Gen 2	1-1	1-2	1-3
Gen 2.2	1	2	3

	Round 4	Round 5	Round 6
Deep Diffusion 7 Stack	D366	D367	D380
Deep Diffusion Untested	~~802~~	803	804
Epitaxially Grown 1500	1565	1566	1567
Epitaxially Grown 1600	1604	1605	1606
Gen 2	1-4	2-1	2-2
Gen 2.2	4	5	6

Table 5.3.1. This table is representative of 16 total rounds for the experimental design testing. Each round contains one of each type of diode (i.e., deep diffusion 7 stack, epitaxially grown diodes, gen 2 diodes). Each number corresponds to the sample number of each DSRD. The diode crossed out in red was not a part of this study.

The press pack (refer to Figure 5.3.1) can apply equal and consistent pressure across the diode, reducing the variations in current-voltage measurements and is an interchangeable test fixture for both the 371A curve tracer and the picoammeter.

This ensures our ability to measure each diode as consistently as possible as we attempt to correlate the current-voltage readings from both pieces of equipment.

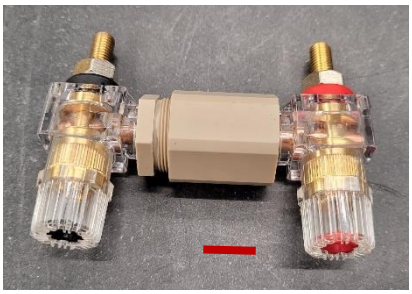

Figure 5.3.1P Press pack fixture that was used to collect current-voltage measurements from both the 371A curve tracer and from the Keithley picoammeter. This fixture applies consistent pressure across the diode and is expected to significantly reduce the variation found within the current-voltage measurements.

In addition to constructing a new diode testing fixture, a SOP for the 371A curve tracer has been developed. Unfortunately, the data collection process is tedious since it has a bubble memory, an obsolete non-volatile computer memory technology, requiring the user to toggle along each data point while writing the numbers down by hand. A group of different types of diodes is currently being tested and evaluated using this procedure.

5.3.4 *Technical Results*

(A.6) Initial results of the Randomized Complete Block Design of the forward current-voltage measurements showed significant measurement deviations. As seen in Table 5.3.2, each red arrow indicates at least one failed measurement of the three taken for each diode. The Gen2 group had 5 out of 12 diodes produce only one usable voltage reading. These measurement results are due to the sample fixture used in this study since it was unable to apply consistent pressure. The Gen2 diodes were difficult to measure since they are approximately a third of the height of the 7-stack diode. A press pack fixture from the pulser team was presented as a viable alternative (Figure 5.3.1) to our current fixture. Studies evaluating the measurement improvement of the fixture are currently in progress.

Diode Name	Average (V)	Std Dev (V)	Coeff of Variance	Diode Name	Average (V)	Std Dev (V)	Coeff of Variance
D1	3.39	0.01	0.30%	EG1601	3.64	0.02	0.49%
D319	3.32	0.01	0.45%	EG1602	2.47	0.01	0.34%
D333	3.48	0.02	0.52%	EG1603	3.48	0.02	0.48%
D366	3.31	0.01	0.15%	EG1604	2.72	0.02	0.60%
D367	2.93	0.01	0.20%	EG1605	3.53	0.02	0.55%
D380	3.05	0.01	0.20%	EG1606	3.55	0.02	0.46%
D630	3.56	0.02	0.49%	Gen2 1-1	4.05	N/A	N/A
D657	3.52	0.02	0.61%	Gen2 1-2	4.35	0.21	4.72%
D801	3.70	0.02	0.61%	Gen2 1-3	4.01	N/A	N/A
D803	3.81	0.11	2.75%	Gen2 1-4	4.13	0.14	3.29%
D804	3.88	0.03	0.67%	Gen2 2-1	4.14	0.03	0.71%
EG1562	3.60	0.02	0.42%	Gen2 2-2	4.35	0.48	11.03%
EG1563	3.50	0.02	0.51%	Gen2 2	4.13	N/A	N/A
EG1564	3.45	0.02	0.49%	Gen2 3	3.88	N/A	N/A
EG1565	3.51	0.03	0.79%	Gen2 4	3.97	N/A	N/A
EG1566	3.49	0.02	0.61%	Gen2 5	3.94	0.05	1.38%
EG1567	3.47	0.02	0.63%	Gen2 6	4.58	0.04	0.90%

Table 5.3.2 Each diode in the table above with a red arrow means that at least one of the three measurements failed to provide a voltage reading at 10 mA. The coefficient of variance is the ratio of standard deviation to the mean, expressed as a percentage ($c_v = \frac{\sigma}{\mu} \times 100\%$). NOTE: each Gen2 diode measurement has been normalized for 7-stack die equivalency.

The findings of these current-voltage measurements are noteworthy since the test fixture was not currently known to produce such large variations in measurement. This source of variation was quick and simple to correct and will lead to more accurate measurements in the future that can be correlated to pulser circuit data.

5.3.5 *Summary of Significant Findings and Mission Impact*

(A.1) Several KPIs have been identified that tie the experimental diode test results to SPICE model simulation parameters. The first KPI is the forward current-voltage (the voltage reading at 10 mA) that is linked to the following SPICE parameters: saturation current, ohmic resistance, emission coefficient, and the forward knee voltage. From the impedance analyzer, the capacitance-voltage measurement is tied to the zero bias junction capacitance and the bottom junction grading coefficient. Both the forward voltage-current and the capacitance-voltage KPIs can be further tied to the SPICE simulation circuit peak voltage performance. The reverse current-voltage (current at -200 V) is linked to the breakdown voltage SPICE parameter. The reverse recovery time measurements, such as the charge storage time and the transition time, are tied to the transit time SPICE parameter and to the full width at half maximum of the pulse signal. Several of these KPIs are not yet associated with specific circuit performances but will require further analysis as outlined in B.4.

(A.2) A preliminary DOE has been developed. The first 6 out of 16 rounds are currently being processed per (A.6).

(A.6) It was found that the test fixture for the picoammeter was causing large variations in the current-voltage measurements due to inconsistent pressure application to the diode. The variation was significantly larger on the Gen2 diodes since they are approximately one-third the height of the 7-stack diodes. A new press pack fixture has been modified for use on the picoammeter and is expected to drastically decrease the variation in results.

(B.1) In A.6, it was discovered that the test fixture was the cause of significant variation within the test results, particularly with the Gen2 diodes. Several diodes are scheduled for repeat measurements to determine if all diodes need to be re-tested, which would affect the "completed" status of this milestone.

5.3.6 *References*

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5.4 DSRD-Based Pulsed Power Source Systematic Topological Optimization

(Islam Sarwar & Gyanendra Bhattarai)

5.4.1 *Problem Statement, Approach, and Context*

***Primary Problem*:** Inductive energy storage (IES) and release pulse generators that use drift-step recovery diodes (DSRDs) can be used as the fundamental units of all-solid-state high-power microwave (HPM) systems. The output from DSRD-based pulsers can then be fed into sub-nanosecond pulse sharpeners to achieve ultra-short high-voltage pulses. While DSRD-based pulsers can theoretically achieve the targeted 1's of GW in 1's of ns, their circuits are not topologically optimized to achieve high voltage gain (peak pulse voltage/prime source voltage), thus requiring large and heavy high-voltage (multiple kV) prime power supplies to achieve the required 100's of kV pulses. They also necessitate liquid-based cooling systems to dissipate the excess heat they generate during operation, further adding weight and rendering them impractical for Navy afloat missions.

***Solution Space*:** Systematically develop optimum circuit topology to maximize the voltage gain, and thus the peak voltage, peak power, and volumetric power density of DSRD-based HPM systems. Minimize the heat loss to be able to air cool by increasing

energy efficiency through optimization of circuit elements without sacrificing the desired nanosecond risetime of the pulses generated. Air-cooled IES pulse generators using optimum DSRD stacking can remove the need for photo-triggered switches and their laser sub-systems. They are ideal for triggering sub-nanosecond rise-time sharpeners (SAS, D-NLTL, etc.), reducing overall cost, volume, and weight.

***Sub-Problem*:** DSRDs are not domestically available COTs components, but rather manufactured in small-batch quantities, with statistically significant variations in their performance parameters. In addition, our current SPICE models of these diodes may not be accurate due to unknown device parameters such as carrier distribution, carrier lifetime and the limiting current that we can pump without affecting the diode recovery property (see section 5.1 and 5.3) during high-voltage transients. These issues may lead to an inaccurate simulation model of the pulser and discrepancies between simulated and experimental results.

***State-of-the-Art (SOTA)*:** Air-cooled DSRD-based pulsers (equivalent in size to the pulse generators developed for this effort, i.e., ~0.01-m^3, ~2-kg) can achieve <20 kV, 1–2 ns risetime, and <4 ns FWHM across a 50 Ω load with a PRF of <15 kHz in burst mode. Available literature on IES pulse generators only describe a few circuit configurations, and there is a lack of comprehensive investigation of circuit topologies and optimization to achieve maximum gain and efficiency and reduce thermal load. Additionally, these pulsers are expensive and are not available within the United States.

***Solution Proposed*:** Develop different DSRD circuit topologies implementing series and parallel combinations of DSRDs (to increase reverse breakdown voltage and diode current, respectively) to minimize circuit components, such as inductors, capacitors, and switches. Systematically identify the best circuit topology and optimize the circuit components through physics-based DSRD pulser circuit theory and SPICE simulation to maximize voltage gain and efficiency while minimizing the prime source voltage and thermal load.

Risks, Payoffs, and Challenges:

***Risks*:** All-solid-state DSRD-based IES pulsers require many other electronic components. Most importantly, the current pumping capability of available MOSFETs/electronic switches is limited, which may make maximizing the output voltage impossible even though the DSRDs are capable of higher current and output voltages.

***Payoffs*:** Being able to simulate and fabricate DSRD-based pulsers using physics-based pulser theory, partnered with US-based DSRD manufacturers, will enable a comprehensive domestic ability to optimize, produce, and evaluate these nanosecond pulsers.

***Challenges*:** Domestically manufactured (U.S.-based) DSRDs, which possess sub-optimal doping profiles, may lead to sub-optimal pulse generators. Accurate spice modeling of the diodes could be affected by expected wide variability in the diode characteristics or unavailability of advanced device characterization techniques. Determining the superlative ratio of design/development (through numerical analysis) to the effort put towards experimental testing/evaluation of the DSRD pulser is challenging due to the novelty of the approach. Extending the theory of single (1×1) pulse generator

to cascaded (M×N) generator to increase the output will be very complex and may require significant time and computing power.

5.4.2 Tasks and Milestones / Timeline / Status

(A) Milestone – Develop theory of DSRD pulse generator to facilitate optimization of 1×1 pulse generator [***Completed JAN22***]

(B) Milestone – Extend the theory developed in Milestone A to facilitate optimization of M×N pulse generator [**JAN–MAY22** / ***Ongoing***].

(C) Milestone – Construct/demonstrate a DSRD-based 1x1 pulse generator prototype based on theory developed in milestone (A) and obtain performance data for multiple combinations of diode stacks [**JAN–MAY22 / *Ongoing***].

(D) Milestone – Construct/demonstrate a DSRD-based 2×2 IES pulse generator prototype capable of producing ≥4 kV peak voltage, ≤1 ns risetime, ≤5 ns FWHM, ≥320 kW peak-power, ≥1 kHz PRF, ≥100 shots-per-burst, ≥5 number of bursts [***Completed JUL21***].

(E) Milestone – Construct/demonstrate a DSRD-based 4×2 IES pulse generator prototype capable of producing ≥12 kV peak voltage, ≤1 ns risetime, ≤5 ns FWHM, ≥3 MW peak-power, ≥100 kHz PRF, ≥1,000 shots-per-burst, ≥500 number of bursts [*On hold*].

(F) Milestone – Develop waveform inverter which, when combined with the pulser from Milestone C, enables a balanced differential waveform output with >90% inverted signal fidelity. [***Completed DEC21***].

(G) Milestone – Construct/demonstrate a M×N pulse generator prototype capable of producing ≥20 kV peak voltage, ≤1 ns risetime, ≤2 ns FWHM, ≥8 MW peak-power, ≥100 kHz PRF, and $\geq 2\sigma_{Vpeak}$, which operates in continuous-burst mode as a viable candidate for OSPRES Contract source alternative [*on hold until Milestones B, D, & E are completed*].

5.4.3 *Progress Made Since Last Report*

(B) Single-bar DSRD pulse generators optimized for 7-, 14-, 21-, and 28-stack LLNL and SPT Gen-2 diodes are simulated and compared for their theoretical output. Based on the previous experimental results and the simulated output, we hypothesize that the inaccurate diode series resistance could be a factor in lowering the output voltage.

(C) A modular driver circuit for optimized MOSFET operation is designed and simulated which is capable of driving four parallel MOSFETs to increase forward pumping current through the diodes.

5.4.4 *Technical Results*

5.4.4.1 Optimization Simulations for Different Diode Stacks Considering Circuit Limitations and Effect of Diode Series Resistance.

(B) In the previous reports, the DSRD pulsers were designed and simulated using diodes obtained from LLNL. In this reporting period, we have optimized the pulser circuits using the SPT Gen-2 diodes. Figure 5.4.1 shows a simplified schematic of the 1×1 DSRD pulser circuit, and the working principle and optimization sequence of the pulser has already been presented in the DEC 2021 MSR. However, the optimization sequence we presented did not consider circuit limitations such as diode break-down voltage, diode series resistance, maximum MOSFET current, OFF-state MOSFET voltage, and the prime source voltage. Here we revisit the optimization sequence considering these circuit limitations.

For the circuit elements optimizations, there are some conditions that we need to set up before starting the optimization simulation sequence, which are described below.

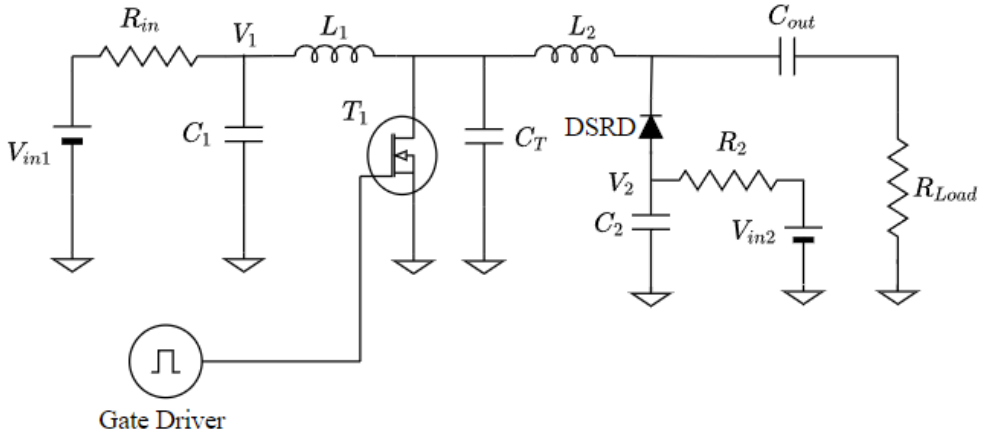


Figure 5.4.1. A simplified circuit schematic of DSRD pulser.

i. Output Voltage (V_{out}): The maximum output voltage of a DSRD pulser is no more than the total reverse breakdown voltage of all diodes connected in series.
ii. Prime Power Voltage (Vin1 and Vin2): Our aim in the project is to obtain the maximum output using a minimum prime source voltage. Thus, we start with a minimum possible prime source voltage.
iii. Total Injected Charge (Q_{inj}): We know from the working theory of the DSRD pulser that the output voltage depends on the maximum diode reverse current (depends on the total injected charge) and the DSRD snap-off time. For optimum circuit operation, we need to obtain maximum possible output with minimum possible injected charge. Thus, we start the circuit optimization with the minimum charge injected.

After considering these important conditions, other circuit parameters are optimized by simulating the circuit using the following circuit parameters.

i. Forward Pumping Time (t_{pump}): The total injected charge during forward pumping time is given as

$$Q_{\text{inj}} = \frac{2I_{20}t_{\text{pump}}}{\pi}$$

Where I_{20} is the amplitude of the forward diode current. Because I_{20} is limited due to the limitations in prime source voltage, diode resistance, and MOSFET current limit, the LT-spice simulation is performed for different values of pumping time to get maximum output without crossing the circuit limitations.

ii. Circuit Elements L_2 and C_2: As the forward pumping current/charge is obtained from L_2C_2 oscillations, the parameters are selected as

$$L_2 = 2\frac{(V_{\text{in2}} - V_{\text{MOSFET}} - V_{\text{diode}})t_{\text{pump}}^2}{\pi^2 Q_{\text{inj}}}$$

And

$$C_2 = \frac{Q_{\text{inj}}}{2(V_{\text{in2}} - V_{\text{MOSFET}} - V_{\text{diode}})}$$

where V_{MOSFET} and V_{diode} are the MOSFET turn ON voltage and the built-in voltage of the diode, respectively.

iii. Trigger Length (T_{ON}): The trigger length is related to the pumping time by the following relation:

$$T_{ON} = mt_{\text{pump}}: \qquad 1.0 < m < 1.5$$

So, the simulation is performed for increasing value of the parameter m.

iv. Circuit Elements L_1 and C_1: The circuit elements L_1 and C_1 are chosen such that the time period of oscillation $2\pi\sqrt{L_1C_1}$ is very large compared to the trigger length (T_{ON}). Specifically,

$$L_1C_1 \geq 4T_{\text{ON}}^2$$

However, because L_1 determines the current I_{L1}, to keep it below a limiting value determined by the MOSFET current and voltage, we set $L_1 = kL_2$ where we simulate the circuit for a wide range of k, and C_1 is set according to equation above.

v. Shunt Capacitance (C_T): In our simplified working theory, the capacitor C_T does not come into play. However, it provides a path of current flow when the MOSFET suddenly turns OFF. Thus, the optimum value of C_T is obtained by simulating the circuit for different values of C_T which gives the maximum output voltage.

Table 5.4.1 summarizes the values of optimum circuit elements and the output voltages for different diode stacks of LLNL and SPT Gen-2 diodes. The optimum circuit parameters are obtained for the minimum possible charge injected at minimum possible prime source voltages to obtain the target output voltages.

Table 5.4.1. Optimized circuit parameters for DSRD pulsers with different diode stack lengths.

Circuit Parameters	EG series diodes				SPT Gen-2 Diodes			
	7-stack	14-stack	21-stack	28-stack	7-stack	14-stack	21-stack	28-stack
$V_{in1} = V_{in2}$ (V)	50	80	100	120	50	60	80	110
Injected Charge (μC)	3.5	8	12	20	2.2	5	10	16
Pumping Time (ns)	250	300	325	350	125	250	300	325
Trigger length (s)	275	375	390	440	125	315	375	405
$I_{20}\ (A)$	26	43	55	75	30	34	48	63
C_T (nF)	9	9	8	10	4	4	6	6
L_2 (nH)	116	130	128	108	45	95	95	105
C_2 (nF)	55	70	83	115	35	70	95	105
L_1(nH)	35	58	64	70	30	60	55	70
Output Voltage (kV)	3.5	7	10.5	14	3.5	7	10.5	14
Max MOSFET Voltage (V)	500	800	950	1030	313	640	787	995
Max MOSFET Current (A)	170	215	260	316	104	140	232	274
Voltage Gain	70	87.5	105	117	70	117	131	127
$\frac{V_{\text{out}}}{Q_{\text{inj}}}\left(\frac{\text{GV}}{\text{C}}\right)$	1.00	0.88	0.88	0.70	1.59	1.40	1.05	0.88

The optimized parameters presented here are based on the diode models we have developed based on the experimental diode characterization. However, based on the experimental results of the previous pulsers tested, we always faced difficulties in achieving pulse voltage output comparable to simulated values. One of the important diode parameters that could lead to reduced output is the diode series resistance. The diode series resistance causes the forward pumping current to damp over time (damped harmonic oscillator). If the diode ON-state series resistance as seen by the circuit during the forward pumping is significantly higher than the values we obtained from the steady-state DC measurement, the output voltage decreases significantly. Figure 5.4.2 shows the output pulse voltage for different values of series resistance of the diode.

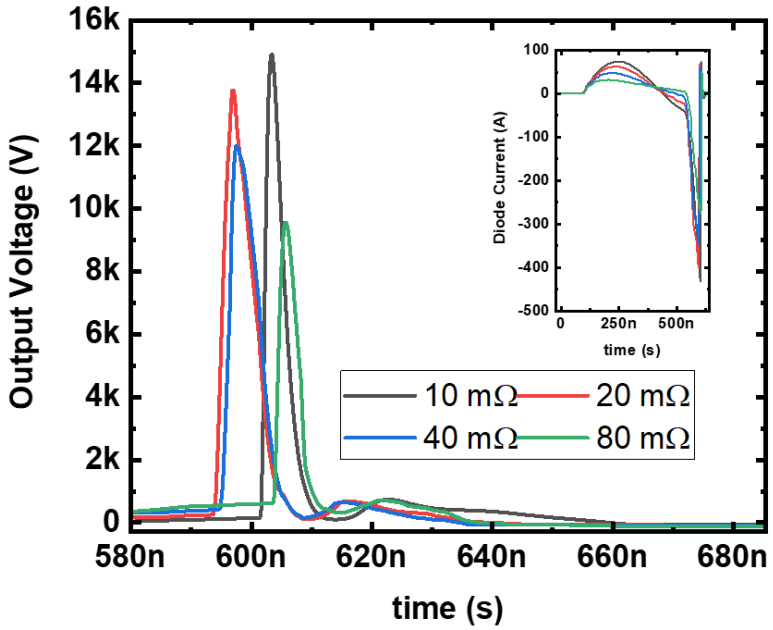


Figure 5.4.2. Simulated output voltages of a 28-stack pulser for different values of diode series resistance. Figure in the inset shows the diode forward pumping current for different diode series resistance. We can see that the pumping current no longer oscillates for 80 mΩ of series resistance per diode stack.

We can see from the figure that the pulsed output voltage decreases with increasing series resistance for a circuit with identical operating conditions. The decreased pumping current with increasing diode series resistance can be seen from the figure in the inset. For a certain value of diode series resistance, the forward pumping circuit no longer oscillates due to over damping. Thus, to keep the circuit oscillating, we need a specific condition given as

$$R_{\text{diode}} \leq 2\sqrt{\frac{L_2}{C_2}}$$

where R_{diode} is the total ON-state diode series resistance.

From the above observations, we make a hypothesis that the lowered output voltages obtained from our previous pulsers could be due to the inaccurate series resistance obtained from the diode characterizations. This could be due to the fact that we did not achieve a reasonable straight line in the IV measurement to extract the series resistance of the 7-stack LLNL diode within a current range of 90 A while the maximum theoretical forward current we pump through the circuit in the pulser is 75 A. Thus the diode forward resistance as seen by the pulser circuit could be significantly higher than the series resistance obtained from the IV measurement.

(B) The existing gate driver circuit was designed to drive a single MOSFET which has a maximum transient current limit of 400 A. However, the driver circuit was not sufficient to drive the MOSFET even with 1 Ω of gate resistance. Further, the lower value of gate resistance caused the driver circuit to burn out frequently when high frequency ringings

propagated to the driver IC. For the DSRD pulsers optimized to produce >10 kV output, the required MOSFET current is much higher than 400 A, requiring multiple MOSFETs to be connected in parallel, further adding more stress on the driver IC. To solve these problems of frequent MOSFET and driver circuit burns, we have designed a modular MOSFET driver circuit with a totem-pole BJT pair, as shown in Figure 5.4.3.

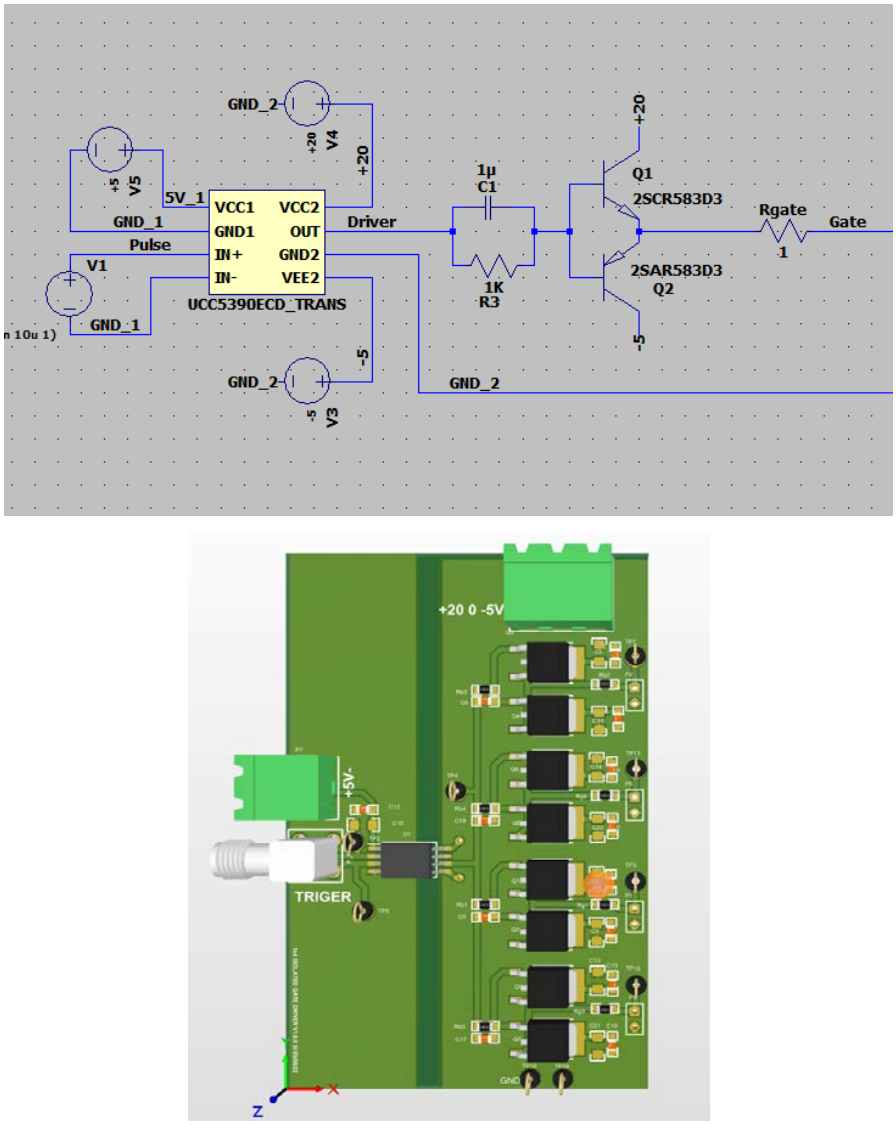


Figure 5.4.3. A modular gate driver circuit schematic (top) and the designed PCB layout of the circuit (bottom).

The new gate driver circuit, which contains a current buffer containing the totem pole BJT pair with each transistor rated for 7 A continuous current, is now sufficient to drive four parallel MOSFETs providing a total MOSFET current of 1600 A. The totem pole network also reduces the stress on the gate drive IC. To make the MOSFET transients short, a capacitor is placed in parallel with the base resistor (R3 in Figure 5.4.3 (top)) which provides a low impedance path for turn ON and turn OFF transients of the MOSFETs.

The modular design further helps replacing the driver circuit without affecting other circuit components.

5.4.5 *Summary of Significant Findings and Mission Impact*

(A) A systematic optimization of a 1×1 pulse generator based on the theory covered in the DEC2021 MSR reporting period was presented. In this reporting period, we have presented an optimization sequence considering the circuit limitations. Based on the previous measurements and simulations, we hypothesized that the lowered output voltage obtained from the previous pulsers could be due to higher diode ON-state series resistance than the value considered for simulation.

(B) Using the 28-stack pulser, maximum peak outputs of 6.7 and 7.5 kV are obtained for a trigger length of 700 ns using a prime source voltage of 120 and 170 V. This suggests that a high voltage gain can be achieved by implementing more powerful MOSFETs and/or MOSFET paralleling. Further, the reverse breakdown voltage of ~650 V per diode in the EG1600 series is estimated based on the DSRD pulser output using a single 7-stack diode. Measurement of circuit voltages at different nodes confirms the circuit performance matching the SPICE simulation. Obtained lower output voltages indicates requirement of more accurate DSRD SPICE Model which takes account of forward diode series resistance, carrier distribution and recombination during high voltage transients.

Table 5.4.2. Comparison of DSRD-based IES Pulse Generator Performance.

KPM	Units	MIDE - V1 Previous	MIDE - V2 Previous	MIDE – V3 Current	Kesar *et al.* SOTA	MI-PPM0731 COTS
V_{supply}	V	225	180	120	300	160
T_{ON}	ns	100	340	700	?	200
V_{peak}	kV	5.59	**7.35**	**6.7**	5	6.3
Gain	V/V	24.8	**40.8**	**55.8**	16.7	39.4
$\tau_{rise,20\text{-}90\%}$	ns	1.2	1.1	3.1	1.96	0.12
dV/dτ	kV/ns	4.66	6.44	2.16	2.55	**52.50**
FWHM	ns	2	5.48	6.90	2.27	0.35
PW	ns	5	7	7	3.5	2.5
Z_{LOAD}	Ω	50	50	50	50	50
P_{peak}	MW	0.625	**1.080**	**0.905**	0.500	0.794
E_{pp}	mJ	0.125	0.154		0.143	0.318
PRF_{max}	kHz	100	100		100	15
Burst	shots	100	100	*N/A*	*N/A*	100
	%	100	100	*N/A*	*N/A*	100
SD_{Vpeak}	σ	> 2	**> 2**	*N/A*	*N/A*	*N/A*
	%	96.5	**97.8**	*N/A*	*N/A*	*N/A*

(C) Successful construction and operation of a 2×2 DSRD-based IES pulse generator prototype has been completed, which meets or exceeds the required key performance metrics. Shown in Table 5.4.2 are the previous and current pulse generator performance specifications in comparison to a similar 2×2 pulser developed by Kesar et al. [1] using DSRDs, and to that of a commercial off-the-shelf (COTS) DSRD pulser of similar space and weight developed by Megaimpulse (i.e., PPM-0731), which also uses DSRDs with silicon avalanche shapers (SAS) [2]. Although the Megaimpulse pulser utilizes a SAS with a <500 ps risetime (a threshold we do not intend to go below due to Commerce Controlled List limitations), it is interesting to compare the results of linear voltage gain and peak power of this system, to that of one that utilizes a SAS. The current permutation of the 2×2 DSRD-IES pulser developed by MIDE under the ONR OSPRES Grant is able to achieve a higher peak voltage and shorter risetime than DSRD-based pulsers reported in the literature of comparable space and weight as well as those commercially available. The ability to generate a linear voltage gain of 40.8 to produce over a Megawatt of peak power into a 50 Ω load while achieving a peak voltage output standard deviation of 2σ when operating at a PRF of at least 100 kHz, brings this technology to the forefront of viable options to potentially support the Naval afloat mission.

(D) Discrepancies exist in the obtained pulser and device characterization data for different series combinations and different samples of 7-stack DSRDs, which may be attributed to the inconsistencies in their manufacturing process. Future work in the coming months include testing multiple stack diodes in pulser configurations with MOSFET paralleling using modular gate driver circuit to identify better diodes and increase the output voltage to >9 kV from the 1x1 pulser configuration. Future work also includes the design and testing of 2×2 or higher configuration DSRD-based pulsers using more combinations of series-connected as well as parallel-connected DSRD stacks.

5.4.6 *References*

[1] https://www.onsemi.com/pdf/datasheet/nvh4l020n120sc1-d.pdf

[2] https://cms.wolfspeed.com/app/uploads/2020/12/C2M0045170P.pdf

5.5 All-Solid-State Sub-ns MW Pulse Generators with Semiconductor Sharpeners

(Gyanendra Bhattarai)

This sub-project is currently on hold as focus is directed toward Section 5.4. Please review the January 2022 MSR for the most recent project overview and status.

6 Thermal Management

6.1 Ultra-Compact Integrated Cooling System Development

(Sam Sisk, Roy Allen, and Sarvenaz Sobhansarbandi)

6.1.1 *Problem Statement, Approach, and Context*

Primary Problem: A thermal management system (TMS) is required for cooling semiconductor-based pulse-power devices, with the goal of maintaining the semiconductor device temperature below 80 °C. The proposed system must increase cooling densities, while decreasing pumping power requirements, in-line with the SWaP-C^2 objective.

Solution Space: To achieve such high cooling densities, an ultra-compact TMS (UC-TMS) to be directly integrated into the semiconductor, a monolithically integrated manifold microchannel chip (mMMC) TMS, and an updated jet impingement TMS (JI-TMS) are proposed herein. The UC-TMS and JI-TMS are expected to achieve turbulent flow with said designs in order to enhance the heat transfer rate. The mMMC-TMS is expected to have low pressure losses while still transferring sufficient heat. The updated JI-TMS is expected to decrease pressure losses while improving or staying consistent with previous versions. The proposed TMS's are restricted to 1 cm^2 surface area, therefore, the required pumping power should be kept to a minimum. An array of micro-sized jet nozzles will provide a turbulent flow onto a microchannel section directly on the semiconductor device. The UC-TMS design will reach turbulency at a faster rate while requiring less energy consumption.

Sub-Problem: The turbulency formed from the array of nozzles creates an extreme pressure loss from the large amount of jet nozzles (over 200) and a flow diameter of 100 microns. The pressure must be sustained to enable proper cooling and circulation processes.

State-of-the-Art (SOTA): Integrated chip cooling is being widely used to dramatically increase the operational power of high voltage silicon-based power devices. However, the current SOTA devices include individual parts that attach to a high-power device, causing less interaction between the semiconductor and coolant, degrading the heat removal rate.

Objective: The proposed UC-TMS and updated JI-TMS design are based on refining in-chip jet-impingement geometry through leveraging theory and a parametric evaluation of nozzle geometry, flow channel arrangements, and outlet to inlet area ratios. The mMMC TMS performance will be compared with the corresponding results available in the literature and with the results from the other two designs. A Si-base unit will be prototyped to maneuver a higher capacity of heat removal. Moreover, to sustain the pressure, the application of different working fluids is suggested. Several types of coolant will be simulated to determine effects from fluid density and viscosity.

Anticipated Outcome(s): To create a TMS with the ability to rapidly remove 1 kW/cm^2 of heat. A design capable of such high heat removal can be implemented on many applications such as high-power batteries.

Challenges: The manufacturing techniques of the semiconductor devices have not yet been adopted for integrated chip cooling systems. The proposed compact design is restricted due to low tolerance of the manufacturing process, as this process must be capable of layering the silicon TMS onto the semiconductor.

Risks: With a system so compact, the pressure drop could be a large issue regarding the objective heat dissipation rate. An extreme pressure drop would potentially cause the coolant to flow backwards, causing less fluid-to-solid interaction.

6.1.2 *Tasks and Milestones / Timeline / Status*

(A) Design a Si base 1 cm^2 UC-TMS, JI-TMS and mMMC-TMS, applying manufacturing tolerances, to achieve a heat dissipation rate of 1 kW/cm^2. The design must be able to be produced by manufacturing techniques such as etching and lithographic layering processes. To confirm the device can be manufactured as proposed, each section of the model will be layered step by step. / MAR22–MAY22 / In Progress

(B) Using the optimal design, perform ANSYS simulations using de-ionized water or Si-C nanofluid. Other fluid types may be researched as pressure drop is a large factor / MAY22–JULY22 / Upcoming

(C) Improve design parameters and sizing to have a lower pressure drop while having a high heat dissipation capability. Prove simulations from previous literature to show capable design configurations with acceptable pressure drop and steady temperature. / AUG22–OCT22 / Upcoming

(D) With proper simulation results, manufacture a prototype to begin experimental testing and evaluation / NOV22–APR23 / Upcoming

6.1.3 *Progress Made Since Last Report*

After further literature review and based on the achieved results on the previous JI-TMS design, three designs have been chosen to move forward with varying alterations to each one. The three designs are UC-TMS, increased outlet JI-TMS and mMMC-TMS. The selected type of heat transfer fluid (HTF) is de-ionized water, due to its promising heat removal capability. De-ionized water is a viable candidate to reduce corrosion within the cooling system, and has the capability to remove heat from the system at low pumping power [1].

6.1.4 *Summary of Significant Findings and Mission Impact*

A preliminary literature review shows that the mMMC-TMS was found to have a low pressure drop while being able to extract 1.7 kilowatts per square centimeter only by using 0.57 watts of pumping power [1]. This was achieved with the mMMC with 2, 4 and 10 inlet and outlet manifold channels and identical 20 × 125 μm microchannels, referred to as the 2×-, 4×- and 10×-manifold chips. The 10×-manifold chip was able to achieve an average change in temperature of 50 K at 100 Watts of power.

(A) After looking over past work on JI-TMS, one significant deficiency of the system was the pressure loss from the geometries. This solution proposed herein with the design of 10x manifold chip, may resolve the pressure loss issue. In order to better validate the effectiveness of such design, a cross-validation of simulation modeling and the results reported in the literature [1] will be performed.

(B) The said three designs, are currently being designed in SOLIDWORKS to be imported to the ANSYS Fluent for performance comparison. All three design will be investigated under the same boundary conditions. As it can be seen in Figures 6.1-6.3, the JI-TMS will have its outlet area increased to reduce the pressure drops, the UC-TMS will have varying angled impingement nozzles in different arrangements, and the mMMC-TMS design will have multiple manifold arrangements at different lengths and narrowing.

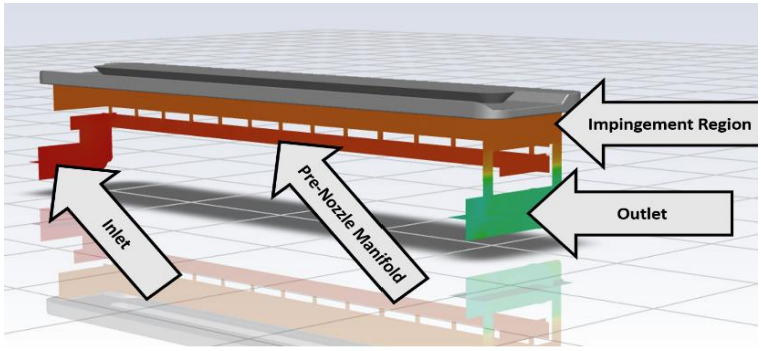


Figure 6.1. JI-TMS

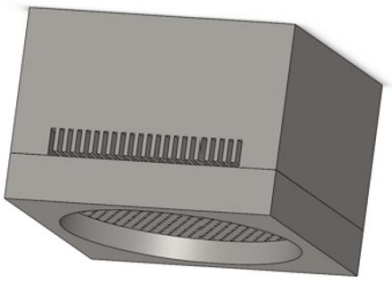


Figure 6.2. UC-TMS

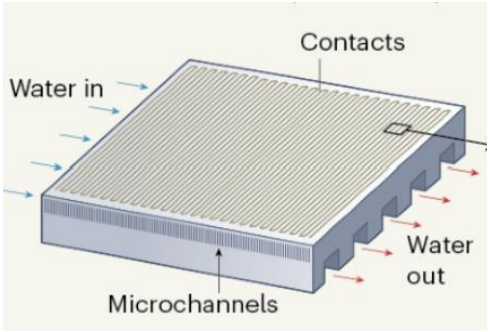


Figure 6.3. mMMC-TMS

6.1.5 *References*

[1] van Erp, R., Soleimanzadeh, R., Nela, L. et al. Co-designing electronics with microfluidics for more sustainable cooling. Nature 585, 211–216 (2020). https://doi.org/10.1038/s41586-020-2666-1

7 Pulse-Forming Networks

7.1 Diode-Based Nonlinear Transmission Lines

(Nicholas Gardner)

Attention on this sub-project is being entirely directed toward the preparation of manuscripts and an associated dissertation. A summary report will be provided in Summer 2022, and this will serve as a placeholder until this time. Please see the January 2022 MSR for the most recent summary and status.

The following paper has been accepted for publication:

N. Gardner, K. C. Durbhakula and A. N. Caruso, “Design Considerations for Diode-Based Nonlinear Transmission Lines,” *AIP Advances*, 12, 055012, **2022** [doi].

7.2 Continuous Wave Diode-NLTL based Comb Generator

(Nicholas Gardner and John Bhamidipati)

7.2.1 *Problem Statement, Approach, and Context*

Primary Problem: When used as a pulse shaping network (PSN), diode-based nonlinear transmission lines (D-NLTLs) are promising solutions towards reducing the size, weight, and cost of RF and microwave sources on Navy afloat missions. However, in pulsed-mode, the impedance of D-NLTLs changes significantly, leading to signal/power reflection, standing wave generation, and return power losses at both the source–line and line–load interfaces, leading to difficulties in practical D-NLTL applications.

Solution Space: Use a D-NLTL to work as comb generator (capable of producing multiple harmonics of the input signal) by converting continuous wave (CW) signals from low frequency–very high frequency (LF–VHF) bands (0.03 MHz–30 MHz) to the ultra-high frequency (UHF) band (0.3–3 GHz) at ones-of-MW peak power. Such an application with reduced dependence on transient changes will decrease impedance mismatch effects at the source–line and line–load interfaces by continuously oscillating D-NLTL peak impedance between the same two values. Use of MW D-NLTLs in the comb generator will push output frequency up to ranges required for Navy afloat missions.

Sub-Problem: Design parameters for COTS high-frequency D-NLTL based comb generators capable of generating up to ~50 GHz output frequencies are limited to <1 Watt output powers, which is <0.1% of the power handling capability required for navy afloat missions. Using the metrics associated with low power comb generators alone to design D-NLTLs capable of generating ~1–2 GHz frequency with capability to handle MW-order peak powers could potentially introduce design errors resulting in frequency/power prediction–measurement discrepancies on the order of a few hundred MHz.

State-of-the-Art (SOTA): Commercial-off-the-shelf (COTS) GaAs varactor diode-based monolithic microwave integrated circuit (MMIC) D-NLTL comb generators are capable of operating at input and output frequencies up to 600 MHz and 30 GHz, respectively. However, these comb generators are not capable of handling powers higher than 27 dBm

(0.51 W). In-house pulsed D-NLTL prototypes have been shown to generate center frequencies of 0.2–0.5 GHz at kV amplitudes (~0.5–0.7 MW peak power) in a light-weight small-footprint circuit. Further D-NLTL network efficiency is hindered by a signal-dependent impedance characteristic to the network leaving reported efficiencies of RF content generation at 10% or less of incident pulse energy.

Objective 1: Design and demonstrate a high voltage D-NLTL based comb generator capable of L-Band Frequency generation and 0.1–5 MW power generation.

Objective 2: Increase D-NLTL network efficiency above the reported 10% threshold through use of CW sources suppressing impedance mismatch effects presented by the signal-dependent impedance characteristic of D-NLTLs.

Anticipated Outcome(s): A successful demonstration of improvements to impedance matching at the source–line interface using a CW signal measured as a reduction in signal amplitude loss between the source and D-NLTL.

Challenges: Nonlinear signal-dependent behavior provided by a reverse bias diode produces difficulties in predicting generated waveform behavior. Further D-NLTL performance is limited in both frequency and power generation by the availability and variety of COTS Schottky and epoxy diodes.

Risks: The reverse bias hold off potential (V_R) of a chosen diode limits the power generation capabilities of the system. If an excitation is used that exceeds V_R, diodes risk being damaged. Further reflections produced at the source–line interface caused by a signal dependent impedance can damage a CW source sensitive to such reflections.

7.2.2 *Tasks and Milestones / Timeline / Status*

(A) Demonstrate an ability of a CW excitation signal to reduce the source–line impedance mismatch effect on signal amplitude present in D-NLTLs when compared to a pulsed mode operation, first through simulations and then by validating the results experimentally using low voltage (LV) and high voltage (HV) prototypes.

(A1) Show the potential to improve source–line impedance mismatch in simulation (Completed SEP21)

(A2) Experimentally demonstrate a low voltage (LV) prototype receiving a CW input (Completed SEP21)

(A3) Compare measured results with simulation behavior; comparison of results will be used to further refine D-NLTL simulation techniques (Ongoing)

(A4) Determine if there are improvements to system behavior if D-NLTL diodes are biased when receiving a CW input (Ongoing)

(A5) Demonstrate improvements to the source–line impedance mismatch in a LV prototype (Ongoing)

(A6) Demonstrate a HV prototype receiving a CW input (Completed NOV21)

(B) Demonstrate UHF – L-band (0.3–2 GHz frequency) generation with a CW D-NLTL.

(B1) Excitation of K100F and K50F D-NLTLs using a 700 MHz signal from the R&S amplifier (Completed NOV21)

(B2) Demonstrate frequency comb generation in K50F D-NLTL using continuous wave VHF excitation (Completed APR22)

(B3) Perform simulation- and experimental studies to measure center frequencies and peak voltage output as a function of source–line and line–load impedances (Completed APR22)

(B3) Simulate topologies capable of utilizing a bipolar pulse for CW applications (**Ongoing**)

(C) Demonstrate UHF generation at single MW power levels with a CW D-NLTL.

7.2.3 *Progress Made Since Last Report*

(B2) To demonstrate frequency comb generation, a D-NLTL prototype with a K50F diode was tested with 3.3 nH and 6.6 nH series inductances upto 200 W input power at excitation frequencies 20–100 MHz. Upto 0.35 GHz frequencies were noticed as shown in Figure 7.3.1.

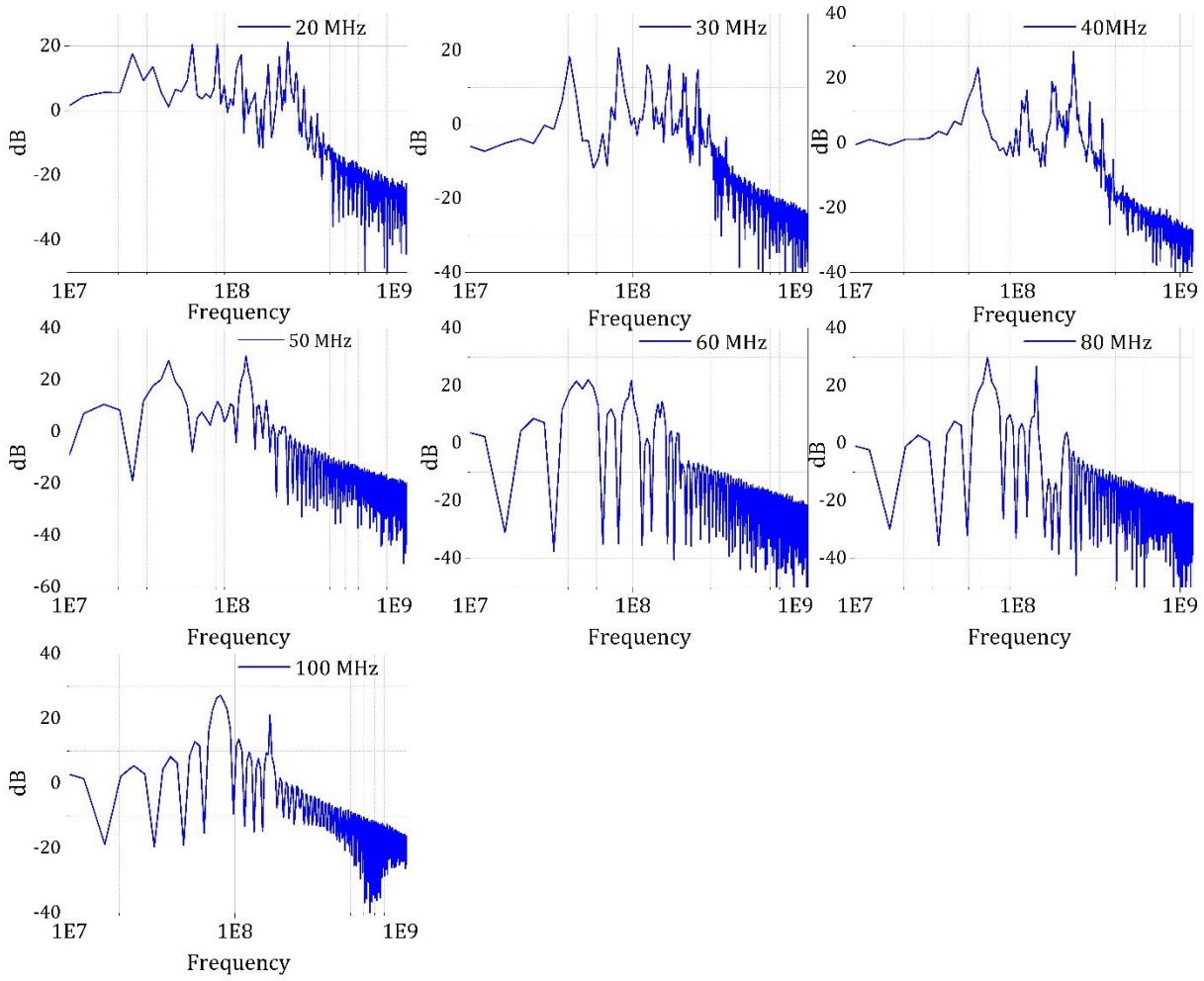


Figure 7.2.1. K50F D-NLTL output frequencies as a function of input excitation frequencies.

(B3) To investigate the possibility of impedance mismatch mitigation, K50F D-NLTL was simulated with two K50F diodes connected back-to-back and center frequency (f_c) and peak voltage parameters were studied as a function of source–line and line–load impedance.

7.2.4 *Technical Results*

(B2) Upon testing K50F D-NLTL with 3.3 nH and 6.6 nH series inductances using ENI 3200L RF amplifier with sinusoidal excitation frequencies upto 100 MHz, frequency harmonics upto 0.3 GHz were realized. However, with an increase in the excitation frequency, a decrease in the number of generated frequency bands was noticed, eventually shifting the D-NLTL operation from soliton generation mode to pulse sharpening mode. A destructive interference due to impedance mismatch-induced reflections could be a potential contributing factor contributing alongside diode CV curve limitations. While the testing was performed at 200 W input powers, <50 W of output powers were noticed. A deformed sinusoidal wave with crossover distortion was noticed when measured at ‘cell 0’ due to reflections between source–line and line–load interface.

(B3) A K50F D-NLTL implementing two back-to-back connected diodes was simulated in LTSpice to study the center frequency (f_c) and peak voltage (V_{peak}) output as a function of source–line and line–load impedances by varying each of them between 10 Ω and 50 Ω. Highest V_{peak} and f_c were noticed with 10Ω source impedance and 50 Ω load impedance, while the lowest V_{peak} and f_c were noticed when 50 Ω impedances are used at source and load as shown in Figure 7.2.2. The prototypes under test are equipped with 50 Ω n-type connectors, resulting in low V_{peak} and f_c.

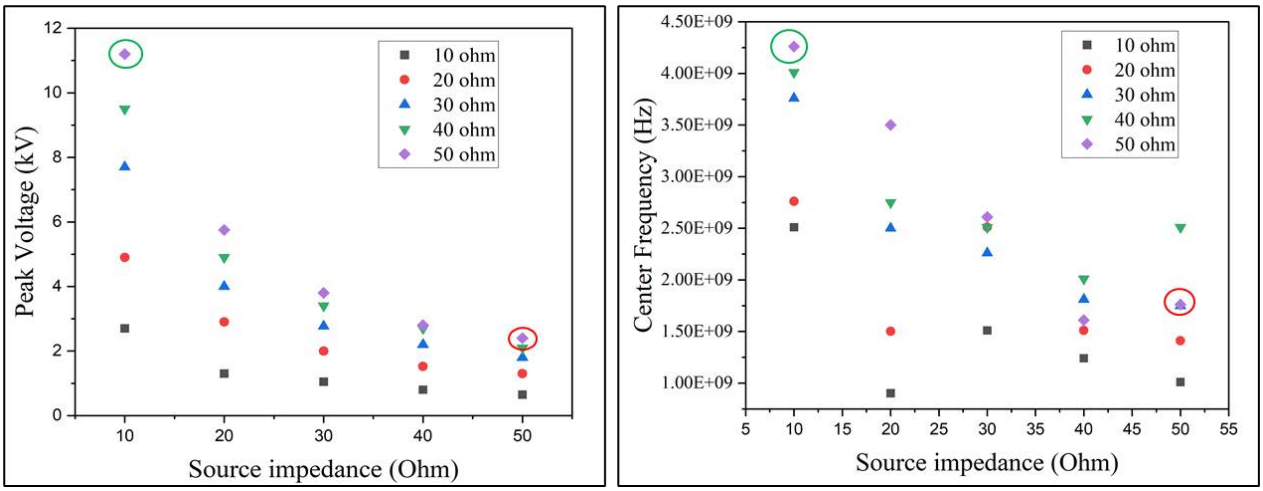


Figure 7.2.2. (a) Peak voltage and (b) center frequency of a D-NLTL as a function of varied source and load impedances

7.2.5 *Summary of Significant Findings and Mission Impact*

(A) In the month of September 2021, a LV prototype was given several continuous waveforms to observe initial behavior of a D-NLTL with a CW source. The LV D-NLTL demonstrated a capability to receive a CW based source. No effect on the source–line impedance mismatch was observed for the LV tests. During the month of November 2021, two high-voltage D-NLTLs based on epoxy diodes were tested using a sinusoidal waveform amplified by an R&S amplifier. Each D-NLTL demonstrated a capability to function with a CW source, however little to no effect was observed on the source–line impedance mismatch.

(B) High voltage D-NLTL based on epoxy diodes of model K50F equipped with 50 Ωn-type connectors on source and load ends was tested with sinusoidal excitation with frequencies 20 MHz–100 MHz. Test was performed using 'ENI 3200 L' RF amplifier with upto 200 W input power. Output frequencies upto 0.3 GHz were generated with < 100 MHz excitation. While soliton generation was noticed below 100 MHz excitation with ~25% conversion efficiency, a shift in NLTL operation from soliton generation to pulse sharpening (frequency doubling) was noticed. However, a decrease in number of frequency bands was noticed with an increase in excitation frequency. When V_{peak} and f_c were studied computationally as a function of source and load impedances, a highest V_{peak} and f_c were noticed when a combination of 10 Ω and 50 Ω were used at source and load, respectively, while the lowest was noticed with 50 Ω at both the

ends. Designing a 50 Ω to 10 Ω impedance transformer to interface the n-type connectors with the NLTL could potentially reduce the impedance mismatch at the load.

7.3 Dynamically Tunable Multi-Frequency Solid-State Frozen Wave Generator

(John Bhamidipati)

7.3.1 Problem Statement, Approach, and Context

Primary Problem: Conventional RF generators such as vector inversion generators, relativistic magnetrons, etc. are limited by their frequency response (narrow bandwidth), form factor, and pulse conversion efficiency, limiting their application in Navy afloat missions.

Solution Space: Develop a single PCB-mount, all-solid-state multifrequency generator with chirp capability and dynamic (electronic/mechanical) tunability. A sub-class of microwave pulsers called frozen wave generators (FWGs) capable of DC-to-RF pulse conversion provide a potential solution in terms of form factor, frequency tunability and power conversion efficiency.

Sub-Problem: A frozen wave generator, an alternative pulse generator capable of generating frequencies in the range of tens-of-MHz to sub-THz proposed by Forcier [1] and Best [2] is limited by the center frequency, form factor, and the performance of the enabling switch.

State-of-the-Art (SOTA): A photoconductive-switch-enabled FWG with adjustable frequency range between hundreds-of-MHz–2 GHz and pulse widths between 360 ps and 15 ns.

Deficiency in the SOTA: Despite addressing the limitations of spark gaps used in the earlier FWG literature, the photoconductive-switch-based FWGs suffer from limitations of the laser systems whose size (>5 cu-ft), weight (>120 lbs.), cost (>$120,000), and cooling have not reached full maturity. Furthermore, they require multiple enabling switches, increasing the switching and synchronization complexity. A single MOSFET-enabled FWG implementation requires an inexpensive (<$500) electronic pulse trigger generator with < 1cu-ft volume.

Risks: The proposed work implements a SiC-MOSFET based prototyping. MOSFETs are limited by their ns-order rise times, which could potentially limit the frequency response of the FWG. On the other hand, when the number of transmission line segments is increased, the MOSFET may not be able to switch all the segments simultaneously, resulting in distorted pulse wavefront. Furthermore, implementing lumped-element-based transmission lines can reduce the conversion efficiency.

7.3.2 Tasks and Milestones / Timeline / Status

1. Simulate a chirp-capable distributed-element transmission-line-based (DETL) 16-stage frozen wave generator (FWG) with balanced and unbalanced load configurations. [JUN–JUL 2021 / complete]
2. Demonstrate a SiC-MOSFET-powered FWG prototype on a custom-built PCB with Cree/Wolfspeed MOSFET, and 50 Ω coaxial cables and/or microstrip transmission lines capable of generating chirped pulse widths. [JUL–AUG 2021 / complete].
3. Simulate a lumped-element transmission line (LETL) based FWG with up to 12 segments to replicate results from the DETL-FWG simulations. [AUG–SEP 2021 / complete]
4. Demonstrate a modular 4–8 stage SiC-MOSFET enabled FWG with lumped-element-based transmission lines with and without chirp capability. [SEP–OCT 2021 / complete]
5. Design and test a 12-segment, MOSFET-enabled FWG prototype with dynamic pulse width tunability using lumped-element-based transmission lines [NOV–DEC 2021 / complete].
6. Perform root cause analysis to determine the causes for (i) pulse overlap demonstrated by the Gen1 LETL-FWG prototype under unbalanced load configuration, and (ii) consistent reduction in the peak voltage output of the pulse train output. [JAN–FEB 2022 / in progress]
7. Demonstrate motorized and/or electronically tunable DETL-FWG prototype with dynamic tunability capable of generating multiple center frequencies. [MAR–APR 2022]

7.3.3 Progress Made Since Last Report

(F) The Gen-2 12-segment FWG prototype was retested with replaced tunable components to verify the results and root cause analysis presented in the previous report cycles. A manuscript based on dynamically-tunable FWG was submitted to the international journal of electronics and communications and is currently in review. A summary report of findings and potential future scope of the FWG will be included in the next report cycle.

7.3.4 *Technical Results*

(F) The damaged tunable components on Gen-2 12-segment FWG prototype due to overvoltage were replaced and retested upto 400V. Upon retest, the previously reported limitations such as voltage drop, pulse overlap, and frequency generation were verified and a need for higher voltage rated tunable capacitors and sub-ns rise-time capable enabling switch have been identified through root cause analysis.

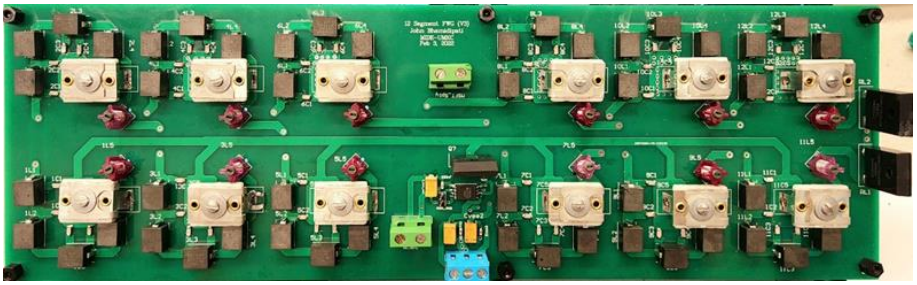


Figure 7.3.1. Gen-2 12-segment dynamically tunable FWG prototype

7.3.5 *Summary of Significant Findings and Mission Impact*

(A) A 16-stage, chirp-capable FWG with was modeled in LTSpice for concept illustration. The TL segments were selected to demonstrate 125–500 MHz output frequencies. Out of 16 transmission line segments in the simulation, 8 are used for generating the desired ON times, and the remaining 8 are required to introduce delays between the ON pulses. At 1.1 kV DC excitation, ~90% conversion efficiency was demonstrated by the model with frequency content upto 4 GHz above 0 dB, and highest magnitude close to 500 MHz.

(B) A MOSFET-switched FWG prototype implementing coaxial TLs has been fabricated and tested with a goal to demonstrate a tunable pulse generator capable of demonstrating chirped pulses. The primary operation of a FWG has been demonstrated with up to 8 TL segments under balanced and unbalanced load configurations. The experimental implementation results on pulse chirp agreed with the simulation results. However, pulse overlap, and deconstructive interference were observed in the 8-segment configuration, which were addressed in the LETL-based FWG prototypes.

(C) Lumped-element-based ladder networks were implemented as an alternative to overcome the limitations of coaxial lines in terms of size and weight. This also provides an advantage of integrating the TLs into the PCB, minimizing the distance between the switch (MOSFET) and charged lines. An 8-segment LETL-FWG was simulated in LTSpice. The components of the LETL were selected to generate ~13.05 ns pulsewidth/delay. When switched at 100 kHz PRR, upto 60 MHz frequencies were generated. with a ~50% conversion efficiency. While the balanced load configuration load response was in-line with the theoretical expectation, pulse train overlap was noticed under unbalanced load configuration, limiting the frequency response. Additional study is required to understand the TL line arrangement required for unbalanced load operation.

(D) In the 4-segment prototype, two TL segments were equipped with 6 cells of 75nH-30pF each, the remaining were equipped with 6 cells of 110nH-43pF, capable of generating 9 ns and 12 ns, respectively. Frequencies upto 50 MHz have been measured across the load. However, when measured under an unbalanced load configuration, a lower voltage was seen alongside reflections and pulse overlap. The lower voltage has been attributed to the power loss occurring at unmatched load resistor, and the pulse overlap due to the unoptimized signal reflection path.

(E) A 12-segment FWG with dynamic tunability was designed with LC ladder networks on a 4.1″ ×14.1″ PCB. Pulse width tunability has been demonstrated by mechanically tuning the L and C parameters. Resulting in a frequency response of 10 – 60 MHz. However, a consistent reduction in peak voltage across the pulse train has been noticed as the pulse train progresses, as shown in Figure 7.3.2. This phenomenon could have been potentially caused either due to (i) the inability of the MOSFET to switch all 6 pairs of transmission lines simultaneously, or (ii) the distance to the transmission line segments from the MOSFET being long, causing a delay in switching. If (i) is validated, creates the need for a faster switch/technology alternative to facilitate simul-switching.

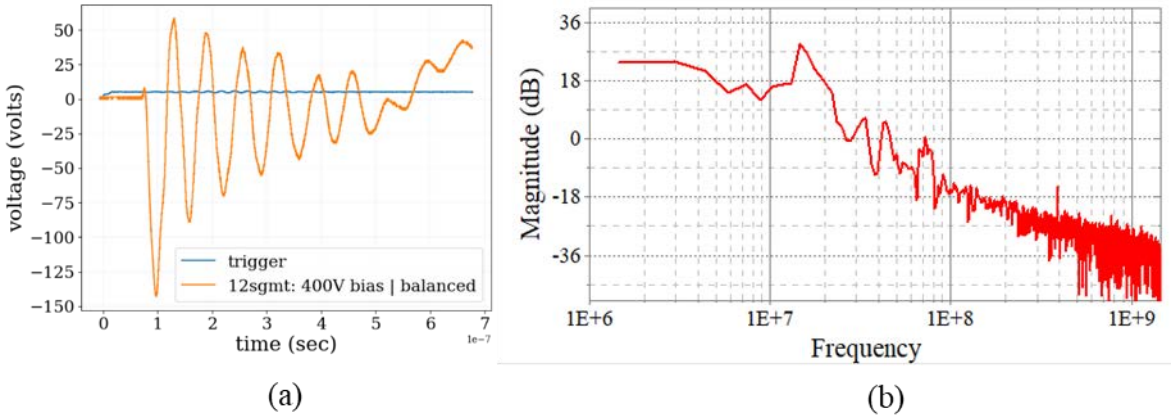


Figure 7.3.2. (a) Load characteristics of a 12-segment fixed pulse width LETLs with 4x 300nH-120pF LC ladder cells in each segment, capable of generating 24 ns pulse width,**(b)** frequency domain representation of (a)

(F) The consistent drop in the peak voltage reported in (E) was measured in Gen 2 prototype despite revising the 12-segment FWG design with modified switch position, optimized ground plane and reduced PCB footprint. The MOSFET with 10.5ns t_{rise} and ~60 ns t_{fall} has been determined to be the bottleneck of the FWG performance, inhibiting simultaneous switching of TL segments. >10.5 ns t_{rise} requires long pulse widths (>11 ns), limiting the frequency to <100 MHz. A solid-state PCSS-like switch capable of low jitter and sub-ns rise-time with compact form factor can greatly benefit all-solid-state implementation of the FWG.

7.4 Pulse-Compression-Based Signal Amplification

(Feyza Berber Halmen)

7.4.1 *Problem Statement, Approach, and Context*

Primary Problem: Solid-state amplifiers, such as gallium-nitride-based high electron mobility transistors (GaN HEMT), can be used as high power microwave (HPM) sources to achieve the SWAP-C2 performance metrics necessary to support the cUAV Naval afloat mission. However, even the best high-power GaN HEMTs are limited to 2–3 kW of peak power, much lower than the 0.1 to 3 MW pulsed power available from traditional

HPM sources such as travelling wave tubes (TWTs). Achieving a power density of 1 W/cm^2 at a distance of 10 m with a high gain (≥ 10 dBi) narrow-band antenna requires an input power increase of two to three orders of magnitude. Power combination methods to achieve an effective radiated power (ERP) at MW scale require 10 s to 100 s of GaN HEMTs, compromising the SWAP-C2 performance.

Solution Space: Pulse compression techniques are used to increase the peak power and lessen the pulse width in HPM applications. Adapting pulse compression at the GaN HEMT or any other SWAP-C2 compatible source output can achieve sufficient ERP with an optimal radiating element.

***Sub-Problem*:** Pulse compression is generally used to generate a pulsed output with a high peak output power (P_{out_peak}) and a wideband frequency content from a DC input voltage. The main challenge lies in identifying a pulse compression technique that can be used to amplify a narrowband RF input signal. Some of the circuit elements for common pulse compression techniques, such as the saturable inductors used for energy storage in magnetic pulse compression (MPC), exhibit increasingly lossy behavior with high frequency. Another challenge will be to determine, if any, the operating frequency limits of the suitable pulse compression technique for high-frequency, high-power signals.

State-of-the-Art (SOTA): Large magnetic pulse compression (MPC) circuits (>1 m^3, >1000 lbs) have demonstrated peak output power up to a few GWs. Smaller versions (~0.125 m^3, 50 lbs to 100 lbs) can achieve 7.5 MW peak power [1].

Deficiency in the SOTA: Traditional MPC systems are large (few meters long), leverage huge transformers, and require liquid coolant such as transformer oil, which leads to undesirable system mass values of ≥1000 lbs. They are used for generating medium or high pulse power traditionally from DC or AC (50/60 Hz) high voltage supplies. There is no known example of high-frequency signal amplification utilizing MPC.

Solution Proposed: Developing a pulse compression circuit that will act as a high-power signal amplifier with a gain of ≥10. Utilizing magnetic pulse compression, or any other suitable pulse compression method, for high power signal amplification with source fidelity.

Relevance to OSPRES Grant Objective: Pulse compression will enable a size and cost efficient solution to high power signal amplification that will lead to HPM source development with optimal SWaP-C2 parameters.

Risks, Payoffs, and Challenges:

Challenges: Modeling pulse compression circuits for high-frequency operation can present a challenge. Pulse compression circuits are generally evaluated in SPICE simulators with low frequency AC / transient simulations. SPICE is a lumped-element model simulator and cannot solve for the distributed-element model required at high frequencies where the wavelengths become comparable to the physical dimensions of the circuit. Some circuit components, such as the saturable inductor in the MPC, are not available in SPICE or many other simulators and need to be modeled using behavioral models and proprietary material data. Pulse compression circuit modeling, especially at high frequencies, needs to be investigated.

Risks: Pulse compression methods are usually lossy in nature and generate a considerable amount of heat; therefore, designing a proper cooling method must be carried out, which may inadvertently increase the volume (size and weight) of the overall design.

7.4.2 *Tasks and Milestones / Timeline / Status*

(A) Milestone – Demonstrate 2–3 times increase in peak power and compression gain using magnetic pulse compression (MPC) [*estimated completion by MAY22*].

1. Subtask – Model saturable inductors in LTSpice or Matlab/Simulink in order to be able to develop MPC simulations / NOV21 / Complete.
2. Subtask – Design MPC circuit with RF input and simulation in LTSpice or Matlab/Simulink to evaluate the resulting amplification and frequency content. / JUNE22.
3. Subtask – Model the high frequency behavior of MPC circuit / NOV21 / Ongoing.
4. Subtask – Build and test the MPC prototype using bench top power supply / OCT21–AUG22 */ Ongoing*.

(B) Milestone – Increase the compression gain available from MPC.

(C) Milestone – Build and test SWAP-c2 compatible high-frequency MPC prototype with GaN source.

7.4.3 *Progress Made Since Last Report*

(A.3) Effects of core remanence and coercivity on core saturation behavior and on MPC circuit leakage currents and reflections were investigated through LTSpice simulations. Conditions for the input stage to minimize reflections were determined and the input stage was modified to work efficiently in an MPC circuit with bipolar input. A prototype B–H curve tracer circuit was built for core characterization.

7.4.4 *Technical Results*

(A.3) LTSpice simulations of the MPC circuit were continued in order to evaluate the leakage currents and reflections observed in the circuit. Both leakage currents and reflections need to be minimized in order for the continuous operation of the MPC circuit with sinusoidal input so that the instantaneous output power amplification can be realized at the given frequency.

The effect of core remanence and coercivity on the saturation behavior and inductance change is investigated for the Kemet core previously used in the simulations. Figure 7.4.1 shows the change in inductance and saturation VT product with the input current, i.e. H, for varying B_r and H_c values. The figure shows that decreasing B_r and increasing H_c values slow down the saturation behavior and the resulting change in inductance. The ideal core should have low H_c and high B_r for a given B_{sat} to reduce the leakage currents. Leakage currents not only cause the saturable inductors to behave like leaky switches but also alter their on/off times which need to be precise for efficient MPC design.

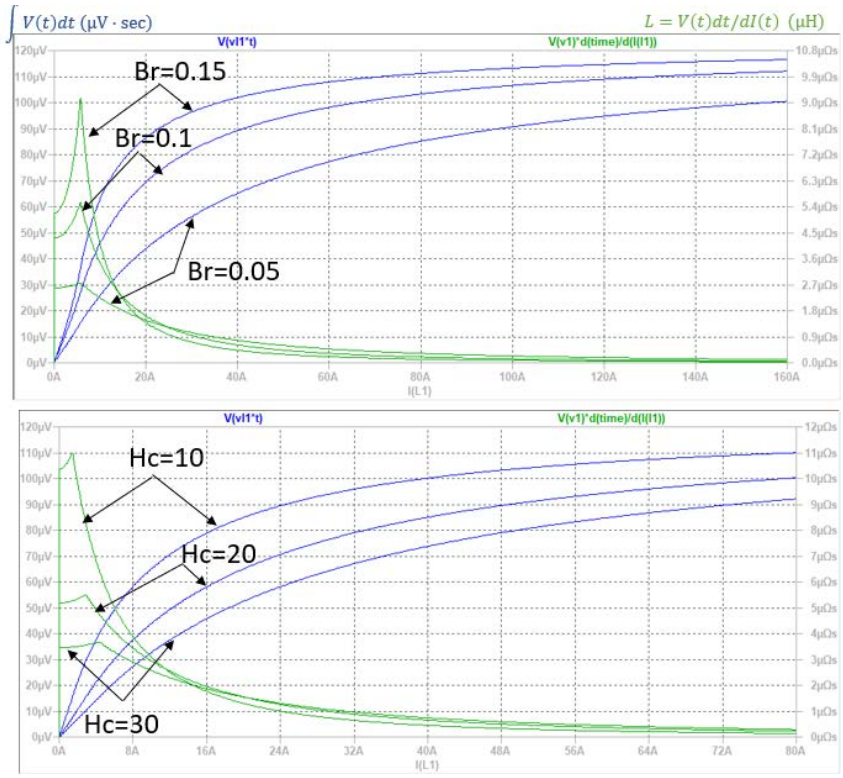


Figure 7.4.1. Change in inductance and saturation VT product with input current for varying magnetic core remanence, B_r, and coercivity, H_c.

In order to minimize the core non-idealities and resulting leakage currents in the initial high frequency MPC design, the original core model is modified to have a much lower H_c of 1 A/m, instead of 40 A/m. The resulting inductance and saturation VT product for input current of 0 to 30 A are depicted in Figure 7.4.2 for N = 1, 4, 10 and 16. The plots clearly show that the core with H_c = 1 A/m almost saturates for less than 3 A input current whereas the actual core of H_c = 40 A/m, used in previous simulations, shows much slower saturation almost up to 30 A. The approximate saturation VT product extracted from these simulations and the calculated saturated inductance are tabulated in Table 7.4.1 for the Kemet core. Note that coercivity is not included in any core or MPC design equations but it does have a huge effect on the design as the B-H curve shape determines the time to saturation.

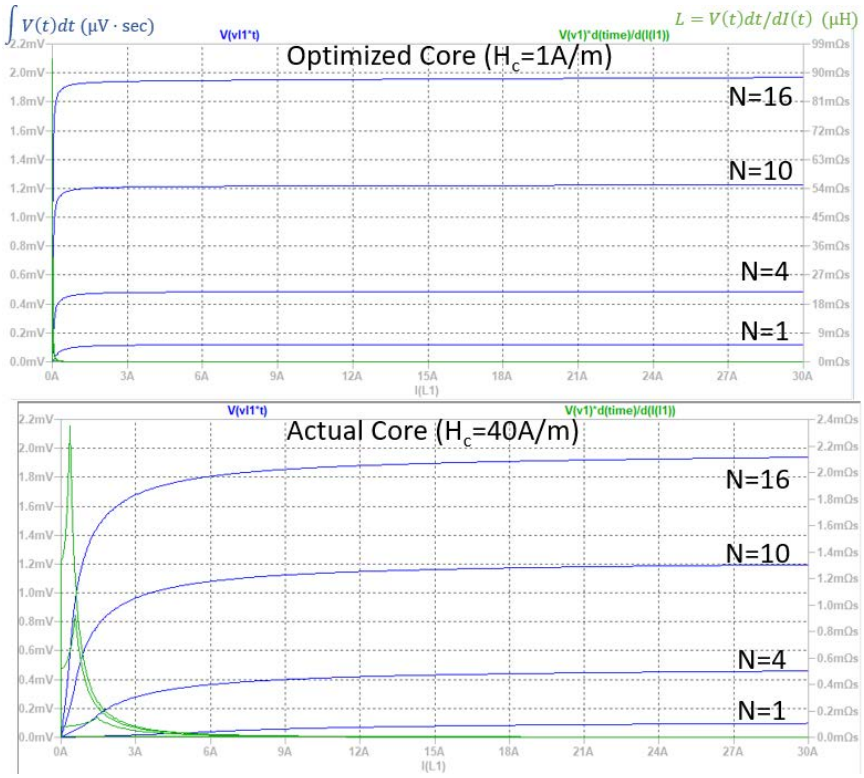
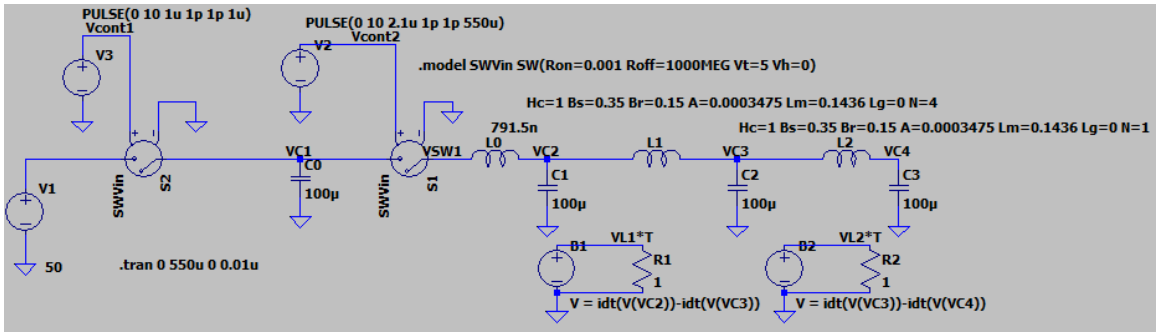


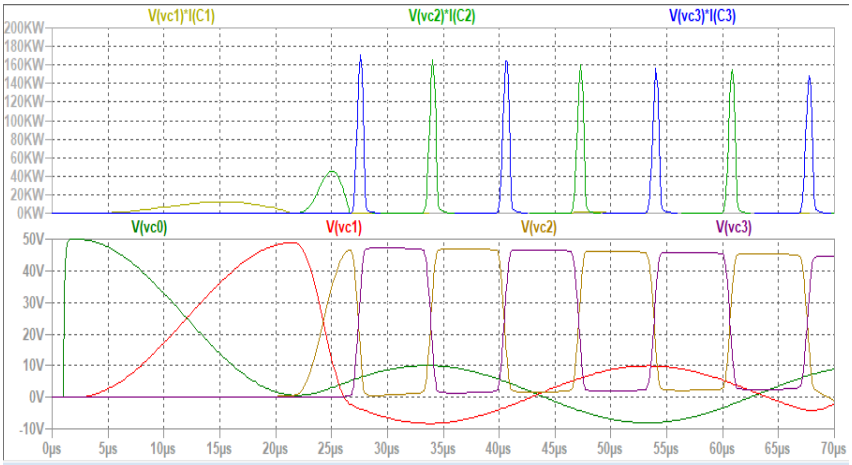
Figure 7.4.2. Change in inductance and saturation VT product with input current for Kemet core with H_c =1 A/m (optimized) and 40 A/m (actual).

Table 7.4.1. Saturation VT product and inductance for the Kemet NiZn material 700L toroid

N	1	4	10	16
L_{sat} (nH)	3.04	48.66	304.16	778.65
VT (V·s)	121μ	488μ	1.223m	1.97m



(a)



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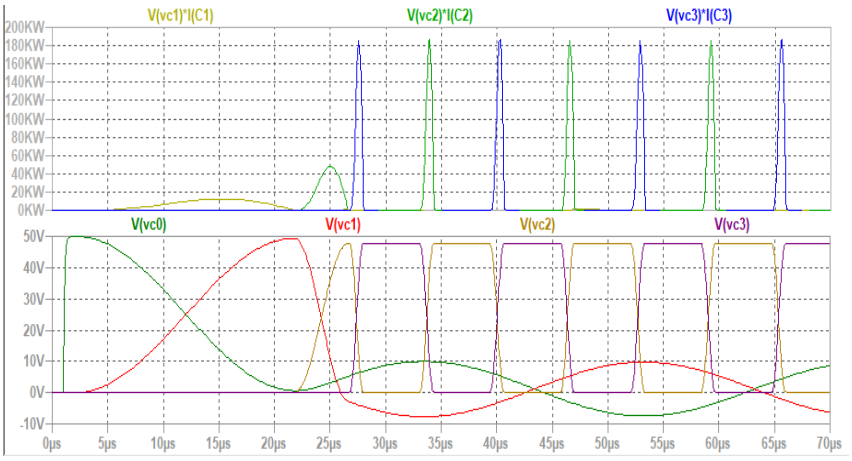


(c)

Figure 7.4.3. Simulated LTSpice MPC circuit (a) and simulated voltage and power values at each capacitor node for magnetic core H_c = 40 A/m (b) and H_c = 1 A/m (c).

The effect of magnetic core coercivity can be observed in Figure 7.4.3. The simulated circuit is shown in 7.4.3(a). Simulation results show the voltage and power at each capacitor node. 7.4.3(b) depicts the results for H_c = 40 A/m and 7.4.3(c) for H_c = 1 A/m.

For this MPC circuit, ideally, the voltage at C0 and C1 should stay at 0 V after these two capacitors discharge. As there is no load at the output, once C3 fully charges, it should start discharging through L2, which is now saturated in reverse direction. C2 and C3 should charge each other indefinitely through L2 unless there is a leakage current. Comparing the voltage and power values for C2 and C3 in Figure 7.4.3(a) and (b), it is observed that high coercivity, hence, slow change in inductance with saturation, results in those capacitors not fully charging or discharging. This leads to loss in output power with time due to decrease in node voltages and inductor currents.

Another reason for the reflections is the input stage of the MPC, which is generally depicted to include a switch and a non-saturable inductor. Unless the switch is unidirectional, this results in a current flow back into the input capacitor, which eventually alters the node voltages and saturation condition of the magnetic switches. The non-zero voltages on C0 and C1 after the initial discharge, observed in Figure 7.4.3, is due to the bidirectional switch S1 before the non-saturable inductor L0. Figure 7.4.4 shows the simulation results for H_c = 1 A/m with the switch S1 turned off right after C0 fully discharges in order to imitate the unidirectional switch behavior. Results indicate no reflections as voltages at C0 and C1 go to zero after initial discharge and voltages at C2 and C3 oscillate between the input voltage value and 0V. Efficiency is maximized for the MPC circuit with unidirectional switch at the input stage and magnetic cores with low coercivity value.

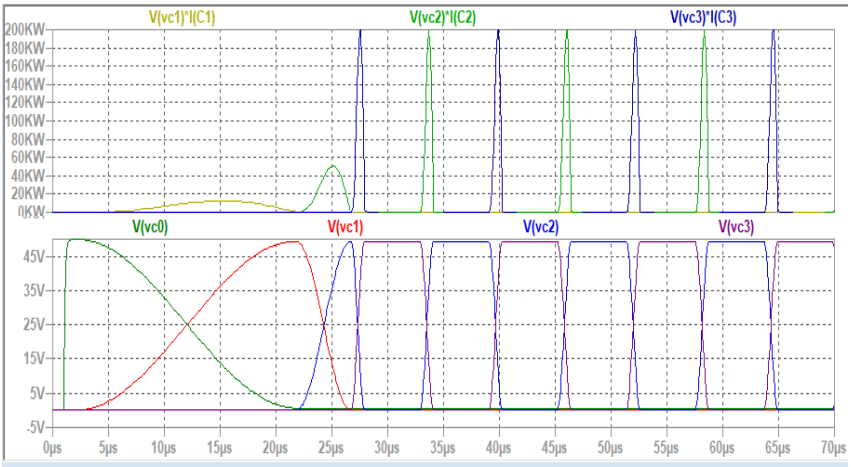


Figure 7.4.4. Simulated voltage and power values at each capacitor node for magnetic core H_c = 1 A/m with 'unidirectional' switch S1

For the high frequency MPC circuit, bipolar input signal is considered for automatic resetting of the magnetic cores at each half cycle. This will avoid synchronization and pulse repetition frequency issues that might arise from separate core reset circuitry. However, in this case a unipolar switch cannot be used at the input stage as it would block the negative half cycle. Instead, the initial stage should be designed with a saturable inductor, which will act like a bidirectional switch which only conducts in saturation. Figure 7.4.5 shows the simulation results for L0 replaced with a saturable inductor. The circuit is simulated for a long time period to show the eventual result of leakage currents, even when they are very small. Figure shows the ideal MPC operation up till about 110 µs,

when C2 charges C1 instead of C3. This is due to residual voltages slowly increasing and resulting in a lower impedance path through L1. As L0 is still a high impedance node, C1 charges C2 and the circuit goes back to normal operation. After a few cycles of this behavior, finally L0 becomes low impedance and C0 is charged at 360 µs. After C0 discharges, circuit operation reverts back to beginning, with a very slow decrease in maximum capacitor voltage due to small leakage currents.

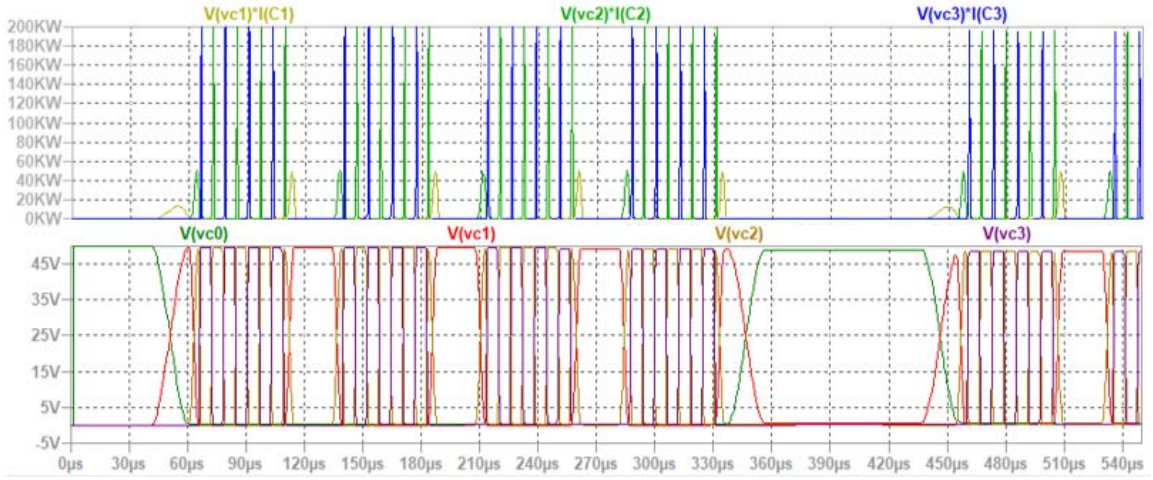


Figure 7.4.5. MPC circuit voltage and power values at each capacitor node simulated with saturable inductor L0 and H_c = 1 A/m.

The results in 7.4.5 show how the leakage currents affect the circuit in time, even when they are very small. This will be a very important consideration while designing the high frequency MPC in order to ensure continuous operation for the required pulse window. Methods for mitigating this effect will be further investigated. High remanence helps reduce the leakage currents, but it might be affecting the untimely switching of the saturable inductors. Effects of remanence on MPC circuit operation will also be investigated.

(A.4) B-H curve tracer is needed to determine the actual magnetic core B-H curves, which do not always match with the manufacturer data as observed with the Kemet 700L NiZn toroidal core. Accurate µ, B_{sat}, B_r and H_c values are needed to properly design the MPC prototype and estimate the possible non-idealities.

The B-H curve tracer circuit schematic is depicted in Figure 7.4.6. It uses a variac and a 5:1 step-transformer to apply up to 24 V to the core under test from a 120 V AC input. The core is setup as a transformer and the series resistor at the input provides the current to the transformer primary with N_1 windings that produces the magnetic field H:

$$N_1 \cdot I = \int H dl_e \;\rightarrow\; H \approx \frac{N_1}{l_e} I \qquad (1)$$

Voltage across the resistor is displayed as the horizontal x-axis on the oscilloscope and is used to calculate H from equation (1). R_1 = 1 Ω is used in the prototype circuit depicted

in Figure 7.4.7(a) to directly read the current from the oscilloscope x-axis. For cores with low B_{sat} values, such as ferrites, the core saturates at small input current levels, limiting the x-axis resolution. Variac can be adjusted to reduce the input voltage and, hence, the input current but this is not sufficient for low B_{sat} values. Increasing the input resistor value also helps decrease the applied current and increase the response time of the core. A switchable series resistor R_2 of 20 Ω, as depicted in Figure 7.4.6 will be added to the prototype circuit in order to keep similar resolution for high and low B_{sat} cores.

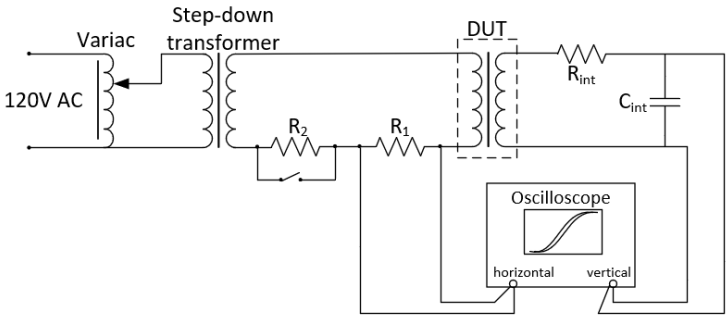


Figure 7.4.6. B-H curve tracer circuit with adjustable input current.

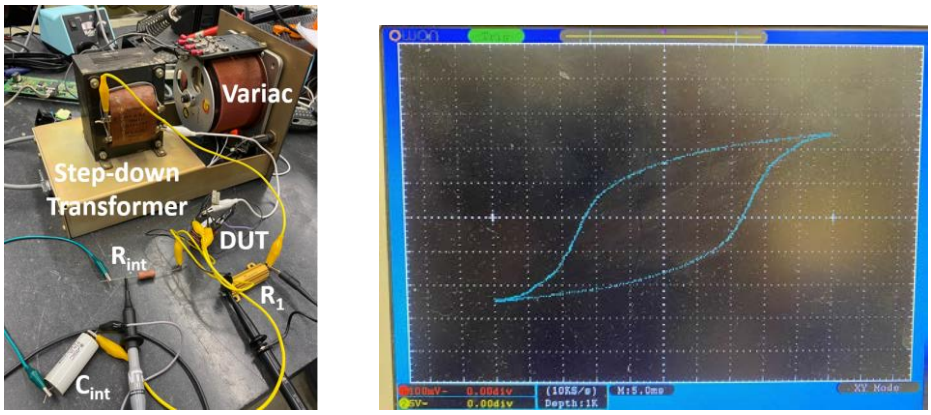
The voltage output of the DUT secondary with N_2 windings is proportional to the flux change in the core:

$$\frac{d\phi}{dt} = \frac{dB \cdot A_e}{dt} = -\frac{\varepsilon}{N_2} \quad \rightarrow \quad B = \frac{\int \varepsilon dt}{N_2 \cdot A_e} \tag{2}$$

With an RC integrator at the transformer output, the voltage across the capacitor is:

$$V_{out} = \frac{1}{R_{int} \cdot C_{int}} \int V_{in} dt \tag{3}$$

Integrator output voltage is displayed as the oscilloscope vertical y-axis. B can be obtained from the y-axis data via equations (2) and (3). Note that the secondary of the DUT should be terminated by high enough impedance so that its current is negligible, and it does not alter the H-field established by the input current. R_{int} = 22 kΩ and C_{int} = 1 μF are used in the initial prototype depicted in Figure 7.4.7(a). The B-H measurement result for a sample magnetic core is depicted in Figure 7.4.7(b). The core measurement displays saturation behavior and B-H hysteresis as expected. The accuracy of the B-H curve tracer circuit still needs to be verified with known magnetic cores. A simple code to produce B-H curves from the oscilloscope x-y data will be prepared next. Also, the prototype circuit will be modified to isolate the high voltage section with variac and step-down transformer in an enclosure and to add a switchable input resistor R_2 to adjust the input current level.



(a) (b)

Figure 7.4.7. (a) Prototype B-H curve tracer and (b) sample magnetic core measurement

7.4.5 *Summary of Significant Findings and Mission Impact*

(A) Initially a basic 2-stage magnetic pulse compression circuit was built and tested with DC input to better understand the MPC principles and considerations such as inductor sizing, pre-pulse currents and inductor saturation. Next, saturable inductor modeling was realized in LTSpice with inductor flux expression and Chan model [2]. Prior to MPC system simulations, magnetic core losses were investigated, and core selection constraints were determined based on the core losses and high frequency MPC design considerations. Next, different magnetic core materials were investigated to determine the most suitable candidate for high-frequency MPC. As reported previously, such a core should have high resistance, narrow hysteresis loop, minimized eddy current area, and low saturation flux density (B_{sat}). High permeability (μ) and very sharp saturation characteristics are also preferred in order to minimize pre-pulse currents and resulting MPC gain loss. NiZn ferrites are the best option among the commercially available magnetic cores for the high frequency MPC application as they have the highest operating frequency, low B_{sat}, and sufficiently high μ. After investigating suitable magnetic cores and their properties, LTSpice simulations of the previously tested 2 stage MPC circuit were resumed using the Chan model for Kemet NiZn cores. Simulations suggest that synchronizing the resonant energy transfer with inductor saturation is crucial for MPC operation. If inductor saturation is not achieved at the end of resonant energy transfer, time compression and, therefore, current amplification is compromised. Input voltage or capacitor values can be adjusted for synchronization; increase in inductance should be avoided as it results in a reduced output current. Effects of core remanence and coercivity on saturation behavior were simulated to optimize the leakage currents and reflections in the MPC circuit. High remanence and low coercivity result in sharp saturation behavior and minimize the losses. Simulations also show the importance of having a unidirectional switch at the input stage of the MPC when a non-saturable inductor is used to improve the efficiency. For a bipolar input signal, which is beneficial for core resetting, the input stage should be replaced with a saturable inductor, which will switch on only when it is saturated in either direction. Leakages

and reflections are important considerations for the high frequency MPC operation as they will determine the overall pulse duration. A prototype B-H curve tracer has also been built in order to characterize the magnetic cores that will be used in the MPC circuit. This will ensure that the core models used in simulations match the actual core behavior.

7.4.6 *References*

[1] D. Zhang, Y. Zhou, J. Wang and P. Yan, "A compact, high repetition-rate, nanosecond pulse generator based on magnetic pulse compression system," in IEEE Transactions on Dielectrics and Electrical Insulation, vol. 18, no. 4, pp. 1151-1157, August 2011, doi: 10.1109/TDEI.2011.5976109.

[2] J J. H. Chan, A. Vladimirescu, X.-C. Gao, P. Liebmann and J. Valainis, "Nonlinear transformer model for circuit simulation," in *IEEE Transactions on Computer-Aided Design,* vol. 10, no. 4, pp. 476-482, 1991

8 Antenna Development

8.1 Tradespace Analysis of an Array of Electrically Small Antennas (ESAs)

(Bidisha Barman and Deb Chatterjee)

8.1.1 *Problem Statement, Approach, and Context*

Primary Problem: Determine the extent to which the physical aperture size of an antenna array, composed of patch elements, can be reduced, while maintaining performance in peak power density, bandwidth, and electronic beam steerability over the UHF range (0.4–1 GHz), compared with present-art high-power-microwave-capable antenna arrays.

Solution Space: An array of patch antenna elements whose feed, two-dimensional shape, and relative placement (i.e., intra-, and inter-element design) allow for the physical aperture size to be reduced by more than 20% compared with the present-art.

Sub-Problem: To overcome scan blindness (as the main beam is electronically steered), due to the excitation of surface waves (SW). (Note: scan blindness is a common phenomenon in electrically small microstrip patch antenna arrays).

State-of-the-Art (SOTA): Horn, reflector, Vivaldi, valentine, etc. are some of the commonly used ultra-wideband (UWB) antenna elements in a phased array for high-power microwave (HPM) transmissions.

Deficiency in SOTA: Large physical aperture size of the antennas.

Solution Proposed: Using electrically small antennas (ESAs) as array elements and optimizing their performance in terms of both near-field (bandwidth) and far-field (directivity) parameters, followed by arrangement of the ESAs in suitable lattice structures (preferably, hexagonal/triangular) to reduce the overall array aperture area. Using stochastic and machine learning (ML) algorithms to optimize antenna element and array performance.

Relevance to OSPRES Grant Objective: Provides design and optimization guidelines for UWB ESA elements, especially coaxial probe-fed microstrip patch antennas, and arrays for HPM applications.

8.1.2 *Tasks and Milestones / Timeline / Status*

(A) Develop an Array Pattern Tool in the context of lightweight calculations of large antenna arrays / JAN–MAY 2021 / Completed code.

(B) Investigate the effects of array aperture area reduction on different array parameters (such as gain, beamwidth, electronic beam steerability) and present a comparative study of antenna array parameters as a function of array aperture area / JAN–MAY 2021 / Completed investigations of arrays on infinite ground planes.

(C) Build minimum viable validation prototypes of single ESA elements on substrates that have good power handling capabilities for HPM transmissions at UHF range (such as polyethylene, FR-4, TMM-10i, TMM-6) / JAN 2021–MAR 2022 / Custom connector design forwarded for manufacturing.

(D) Optimization of ESA (single element) performance using ML based stochastic search algorithms / JUN 2021–APR 2022 / Completed single objective optimization of ESA elements.

(E) Build minimum viable validation prototypes for arrays of ESA elements / JUN 2021–MAY 2022 / Ongoing characterization of a 4×4 square array of ESA elements fed by the custom tapered coaxial connectors.

(F) Optimization of array performance using ML algorithms / SEP 2021–MAY 2022 / Completed single objective optimization of antenna arrays on infinite ground planes.

8.1.3 *Progress Made Since Last Report*

(B) Investigate the effects of array aperture area reduction:

a. Based on the aperture area reduction study conducted earlier, a manuscript has been prepared for submission in the 2022 IEEE International Symposium on Phased Array Systems and Technology.

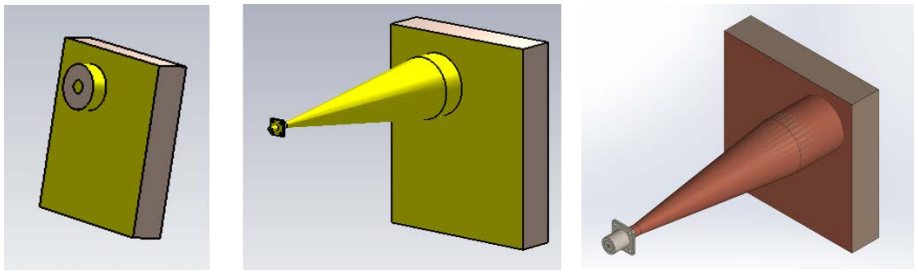
(C) Build minimum viable validation prototypes of single ESA elements:

a. Completed modeling of a wideband, microstrip patch, ESA element, fed by a customized tapered coaxial connector, in the UHF range (0.7–1.1 GHz).

b. The design has been forwarded for manufacturing.

8.1.4 *Technical Results*

(C) Build minimum viable validation prototypes of single ESA elements:



(a) (b) (c)

Figure 8.1.1. Microstrip patch antenna, modeled on a polyethylene substrate and fed by: (a) an ideal connector on $5.5" \times 6.5"$ ground, (b) a tapered connector on $5.5" \times 6.5"$ ground, and (c) a tapered connector on $6" \times 6"$ ground.

Wideband antenna element with tapered coaxial connector:

The detailed design of a wideband, microstrip patch antenna, fed by a customized tapered connector, for operation in the UHF range (0.7–1.1 GHz) was provided in ONR-OSPRES-Grant MSR APR 2022. The initial design was modeled on a $5.5" \times 6.5"$, PEC-backed, polyethylene substrate. However, the commercially available polyethylene panels are $6" \times 6"$ in dimension. Hence, the antenna was remodeled on a $6" \times 6"$, PEC-backed,

polyethylene substrate and characterized in terms of S_{11}-parameter and realized gain. Fig. 8.1.1 shows the three stages of antenna modeling. The corresponding antenna performances are shown in Fig. 8.1.2.

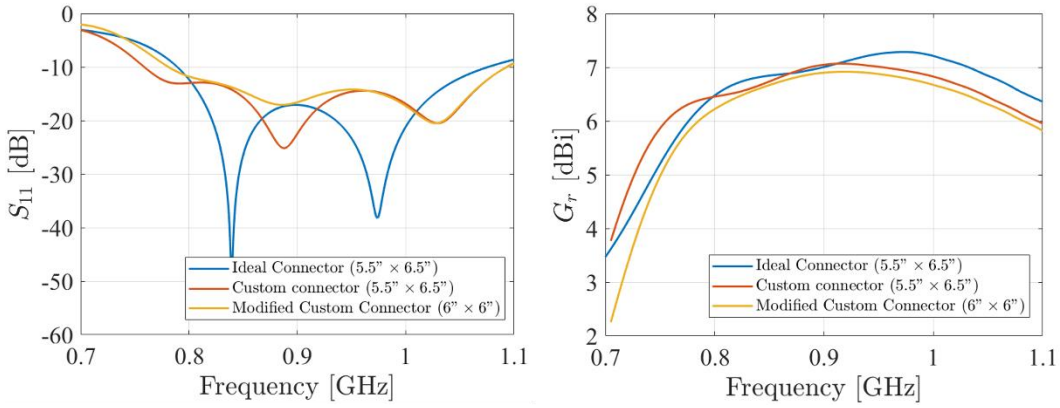


Figure 8.1.2. (a) S_{11} and (b) realized gain of the antenna for the three design iterations considered in Fig. 8.1.1.

Table 8.1.1. Bandwidth and maximum realized gain of the antennas with and without custom connectors.

Iteration #	Description	BW	Max. Gain (dBi)
1	Antenna with ideal connector, 5.5" × 6.5" ground	30.75%	7.28
2	Antenna with tapered connector, 5.5" × 6.5" ground	36.13%	7.06
3	Antenna with tapered connector, 6" × 6" ground	33.25%	6.98

Fig. 8.1.2. shows that although the S_{11}-parameter of the antenna deteriorates with the augmentation of the tapered connector, the overall –10 dB bandwidth increases, with 0.3 dBi loss in peak realized gain. With the available substrate panel dimension, 33.35% of impedance bandwidth could be achieved with 6.98 dBi of maximum realized gain. The antenna element design of Fig. 8.1.1(c) has been finalized for manufacturing and forwarded to the workshop for prototyping.

8.1.5 *Summary of Significant Findings and Mission Impact*

(A) Developing Array Pattern Tool for large arrays calculations:

A MATLAB code has been developed for faster approximation of the radiation pattern of a linear/planar array of any size and composed of any type of antenna elements. The code requires the center element pattern of a small array (say, 3×3) composed of the same type of antenna elements, desired lattice arrangement, and total number of array elements, as user inputs. This work will be included in future publications.

(B) Investigate the effects of array aperture area reduction on different array parameters:

The effects of different aperture shape and lattice arrangements on array gain and beam steerability have been studied for arrays modeled on infinitely large, PEC-backed, substrates. Investigations show that a transformation from square-grid-rectangular-aperture to triangular-grid-hexagonal-aperture leads to $\approx 30\%$ reduction in aperture area ($\approx 50\%$ reduction in number of array elements) with a tradeoff of ≈ 1.5 dBi (in 2.5–5 GHz) and ≈ 3.5 dBi (640–990 MHz range) gain reduction. The aperture area reduction, however, comes at the cost of limited beam steerability to $\pm 45°$ from boresight, compared to the $\pm 60°$ scanning capabilities achieved from the square-grid-rectangular-aperture arrays, at all frequency ranges.

(C) Build minimum viable validation prototypes of single ESA elements:

Developed a design technique for electrically small microstrip patch antenna that provides $\geq 30\%$ impedance bandwidth by strategic placement of the feed-probe along the patch diagonal, at operating frequencies in the UHF (MHz) to microwave (GHz) frequencies. The method avoids any sophisticated prototyping and is a transformative approach in the design of electrically small microstrip antennas for ultrawideband wireless applications. The design approach was validated via prototypes manufactured on TMM-6 and TMM-10i substrates, in the 2.5–5 GHz range. Manufacturing of similar antenna prototypes, for operation in the required UHF range (0.6–1 GHz), is currently underway.

(D) Optimization of ESA (single element) performance using regular, and ML based stochastic search algorithms:

Optimization of feed-probe location and ground plane shape and size in a microstrip patch antenna, with the objective of bandwidth enhancement, using ML based stochastic search algorithms (GA, PSO, and Simplex methods), was performed. ML algorithms were found to be ≈ 2 times faster and ≈ 0.3 times less memory intensive compared to regular search algorithms, while maintaining same degree of accuracy.

It is concluded that, although these automated ML algorithms do not provide insight into the underlying physics of the problems and require human intervention at every stage for better decision making, they can still be considered as potential tools for faster optimization of antenna performance, especially for multi-objective optimization of complex structures, which are computationally intensive using conventional EM solvers.

(E) Build minimum viable validation prototypes for arrays of ESA elements:

A 3×3 array of wideband antenna elements (2.5–5 GHz) and a 2×2 array of narrowband elements (900 MHz), on TMM-10i substrates were manufactured and tested. Having achieved reasonably good agreement between simulated and measured S_{11} and gain responses from individual array elements, it was decided to implement the design method for building the final demonstrable prototypes. Currently, a 4×4 square-grid-rectangular-aperture and a 10-element triangular-grid-hexagonal-aperture array, of wideband, microstrip, ESA elements, in the UHF range (0.6-1 GHz), are being characterized for prototyping.

(F) Optimization of array performance using ML algorithms:

Completed inter-element spacing optimization in a 4×4 square-grid array, on an infinitely large, PEC-backed, dielectric substrate, using ML based genetic algorithm, in the 2.5–5 GHz range, with the objective of array boresight gain enhancement. Multi-objective optimization (simultaneous enhancement in boresight gain and impedance bandwidth) of a 4×4 square-grid array on a finite, PEC-backed, substrate, by seeking the best array design parameters, including inter-element spacing, ground plane size, and feed-probe locations, in the desired UHF range (0.6–1 GHz), is pursued presently.

8.2 Tradespace Analysis of Ultra-Wide-Band (UWB) Koshelev Antenna

(Alex Dowell and Kalyan Durbhakula)

8.2.1 *Problem Statement, Approach, and Context*

Primary Problem: Determine the extent to which the physical aperture area of an antenna array, composed of antenna elements, can be reduced, while maintaining performance in peak power density, bandwidth, and electronic beam steerability over the UHF range (0.4–1 GHz), compared with present-art high-power-microwave-capable antenna arrays.

Solution Space: The Koshelev antenna has a unique design that is capable of generating an UWB response by effectively merging radiation characteristics from a transverse electromagnetic (TEM) horn antenna with exponentially tapered flares, an electric monopole, and magnetic dipoles over a wide frequency range [1]. This opens up an opportunity to investigate the design parameter space and understand parameter effects on impedance bandwidth, radiation pattern, electric field distribution, and other metrics via a tradespace study.

Sub-Problem:

(i) The integration of an impedance transformer to a single element Koshelev antenna to simulate and test the combined (transformer–antenna) performance is currently not feasible using commercial EM simulators.

(ii)The total surface currents on the Koshelev antenna over the desired frequency range arising from the present positioning of TEM exponential flares, an electric monopole, and magnetic dipoles is not yet clearly understood.

State-of-the-Art (SOTA): The balanced antipodal Vivaldi antenna (BAVA) is considered to be the SOTA antenna element due to its exceptional 20:1 impedance bandwidth ratio as well as the ability to handle tens-of-MW input power.

Deficiency in the SOTA: The BAVA design parameter space has been exhausted over the past couple of decades. The physical aperture area still remains very large and there is no viable path through tradespace study for further physical aperture area reduction.

Solution Proposed: Design, simulate, validate, and perform a tradespace study on the important design parameters of the Koshelev antenna array that effectively reduce its physical aperture area while maintaining its UWB properties, in both the frequency and time domains. The Koshelev antenna has been shown in the literature to withstand higher

voltage levels (over 200 kV peak voltage), thereby making it a viable antenna element for detailed tradespace study and analysis.

Relevance to OSPRES Grant Objective: From the literature, it was shown that the Koshelev antenna can handle high input voltages (and therefore high power with 50 Ω input impedance), which satisfies the specific OSPRES objective related to high input voltage/power. In addition, this work can yield a center-frequency-dependent, bandwidth-controlled, and electronically steerable Koshelev antenna design that can be quickly modified to the spectrum properties of the ultra-fast rise time input pulse.

Risks, Payoffs, Challenges:

(i) The electrical size of the Koshelev antenna is approximately λ/4 at its lowest operating frequency. Further reduction of electrical size to λ/10 could considerably reduce frequency dependent gain, thereby decreasing the power spectral density.

(ii) Payoffs include the development of a library of antenna metrics data for different shapes and sizes of the individual parts within the Koshelev antenna.

(iii) The large electrical size (>5λ) of the Koshelev antenna at its highest operating frequency poses huge computational challenges.

8.2.2 *Tasks and Milestones / Timeline / Status*

(A) Complete literature search to identify and list antenna elements that satisfy UWB properties and HPM requirements, and down-select accordingly / NOV–DEC20 / Complete.

(B) Complete initial design, simulation, and validation of Koshelev antenna [1] / JAN21 / Complete.

(C) Perform a preliminary parameter study to identify design parameters that considerably reduce the physical aperture area / FEB–MAR21 / Complete.

- Milestone: Using FEKO and/or CST electromagnetic (EM) simulators, reduce the physical aperture size of the Koshelev antenna to at least 95% of its original design and show minimal to no variation in the bandwidth, gain and increased aperture efficiency / Complete.

(D) Determine the full-width half-maximum (FWHM) and ringing metrics from the envelope of the time domain impulse response ($h_{rx/tx}(t, \phi, \theta)$) in receive or transmit mode / MAR–APR21 / Complete.

- Milestone: Produce a generalized code that calculates the impulse response envelope of the Koshelev antenna and plots the rate of change in FWHM and ringing values as a function of physical aperture size.

(E) Perform tradespace studies on design parameters such as feed position (*F*), length (*L*), and alpha (α). Obtain various antenna metrics data, compare, and analyze / MAR21/ Complete.

- Milestone: Identify Koshelev antenna design parameters that significantly alter the bandwidth, rE/V, peak gain over the desired bandwidth, and aperture efficiency.

(F) Reduce Koshelev antenna aperture size (H×W) to equal to or less than 90 mm × 90 mm, equal to that of the SOTA BAVA, for direct antenna metrics comparison / MAR–APR21 / Complete.

- Milestone: Provide a recommendation on the optimum design parameters and the resulting metrics, with comparison to SOTA BAVA. The optimized design parameters must yield 900 MHz ± 200 MHz bandwidth, rE/V greater than 1, peak gain around 3 dBi at 900 MHz, aperture efficiency equal to or greater than 130% at 900 MHz.

(G) Using the optimized model from (F), build various array simulation models/topologies to perform a tradespace study and report tradeoffs between array antenna metrics such as center element reflection coefficient (S11) value, gain vs theta at constant phi, physical aperture area, aperture efficiency, and rE/V / MAY–JULY21 / Complete.

- Milestone: Develop/showcase an optimized Koshelev array model that exceeds an aperture efficiency of 130% with a high rE/V.

(H) Perform literature search to investigate, understand, and determine the applicability of special electromagnetic (EM) techniques to the antennas under consideration. / JAN–APR21 / Complete.

(I) Explore impedance taper (microstrip based and coax based) designs that can interface well (both mechanically and electrically) to transition the signal from a coax cable to the input of the Koshelev antenna element / JULY21–AUG21 / Complete.

- Milestone: Recommend the optimum impedance taper design (with minimum reflections and maximum power transfer) with the optimum dimensions to successfully convert the high-voltage, short-rise time input signal from a coax cable to the feed of the Koshelev antenna array.

(J) Study response from optimized Koshelev antenna array when excited with different monopolar, differential, and bipolar pulse signals of significant interest / AUG21–NOV21 / Ongoing.

- Milestone: Provide a table comparing the Koshelev antenna array response metrics and narrow down the suitable pulse signals. Recommend (if any) changes to the downselected pulse signal(s) that can further improve the radiation efficiency, and/or transient gain.

(K) Investigate and analyze the response from the optimized Koshelev antenna array when excited by different excitation patterns / DEC 21 / Complete.

- Milestone: Compare and recommend an appropriate excitation method to yield maximum boresight gain, maximum half-power beamwidth (HPWB), minimum side lobe levels, and maximum electric field, rE/V.

(L) Prototype single element Koshelev antenna and test for reflection coefficient, gain as a function of frequency, radiated electric field at 1-m, 2.5-m, 5-m and 10-m (if feasible) distances. / AUG21–SEP22 / Ongoing.

> (L1) Fabricate Cu-foil and paint (silver or copper) variants of 3D-printed balanced Koshelev antenna with integrated impedance transformer.

  - Milestone: Demonstrate a 3D printed Koshelev antenna prototype that is cost-effective and lightweight. / AUG21–NOV21 / Complete.

  (L2) Perform scattering parameter measurements of Cu-foil and paint variants of 3D-printed prototypes to identify any design and fabrication issues/challenges.

  - Milestone: Report fabrication & assembly challenges, test outcomes and identify the source of mistmatch (if any) to alleviate reflections. Verify against simulations to validate mismatches. / DEC21–APR22 / Ongoing.

  (L3) Downselect to one variant of the 3D printed Koshelev antenna prototype and measure frequency domain gain and time-domain electric field at multiple distances.

  - Milestone: Experimentally demonstrate a 3D-printed Koshelev antenna with a performance similar to the standard sheet metal variant of the Koshelev antenna. / MAY22–SEP22.

- Milestone: Report performance of 3D printed Koshelev antenna, compare against the performance of balanced antipodal Vivaldi antenna (BAVA), and recommend any overall improvements to the fabrication/prototyping/testing methods.

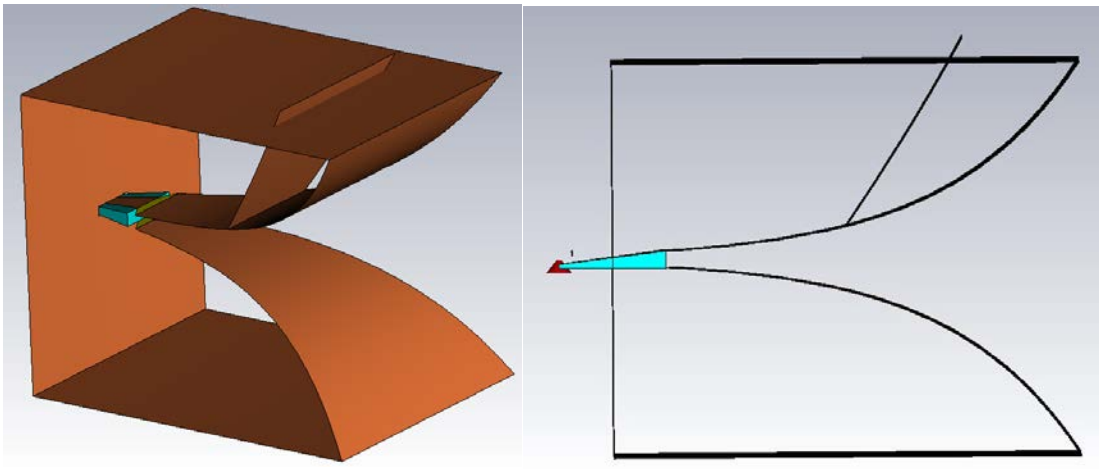
8.2.3 *Progress Made Since Last Report*

(L2) A standalone stereolithography (SLA) based impedance transformer was fabricated and tested for S-parameters to understand its RF performance. Moreover, the impedance transformer was integrated with the Koshelev antenna in the CST studio suite to simulate for combined RF performance and was compared against the standalone Koshelev antenna simulations.

8.2.4 *Technical Results*

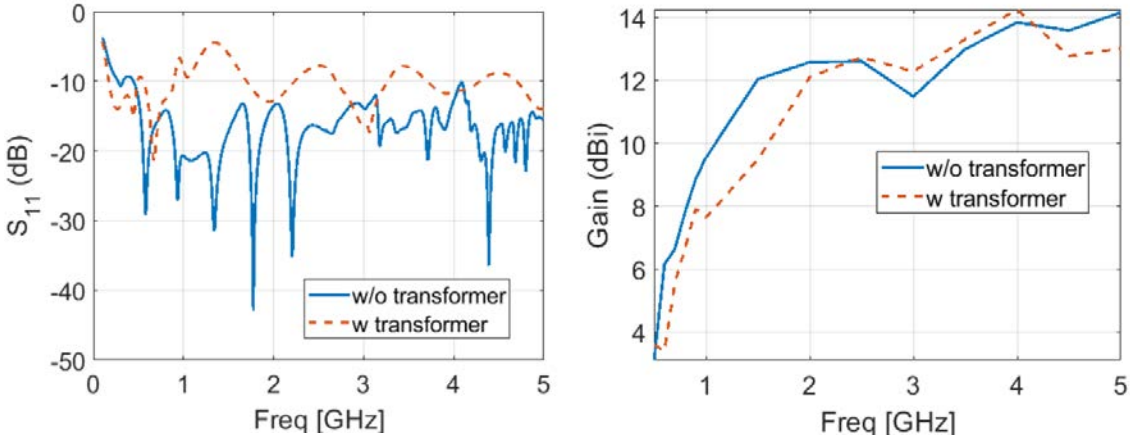
(L2) Over the past month, simultaneous efforts were carried out to understand the reasons for poor performance of the first 3D printed & Cu-foil plated Koshelev antenna prototype integrated with the impedance transformer. The transformer was included to introduce a balanced Koshelev antenna over the unbalanced Koshelev antenna for the former's wide-bandwidth response. However, the balanced Koshelev antenna also needs an impedance transformer. A linear impedance transformer was designed using SLA and poly lactic acid (PLA) as the dielectric substrate.

In the first effort, the PLA based impedance transformer was integrated with the Koshelev antenna in CST Studio Suite. A small copper piece was added to connect the output of the impedance transformer to the input of the Koshelev antenna. Fig. 8.2.1 shows two different views of the simulated design. The reflection coefficient (S_{11}) and the gain simulated with and without the impedance transformer is shown in Fig. 8.2.2 (a), and Fig. 8.2.2(b), respectively. The S_{11} comparison indicates the case with the transformer (dashed red) suffers from degraded performance as expected due to field discontinuity at the transformer–antenna interface. Conversely, the gain values did not differ by a lot.



(a) (b)

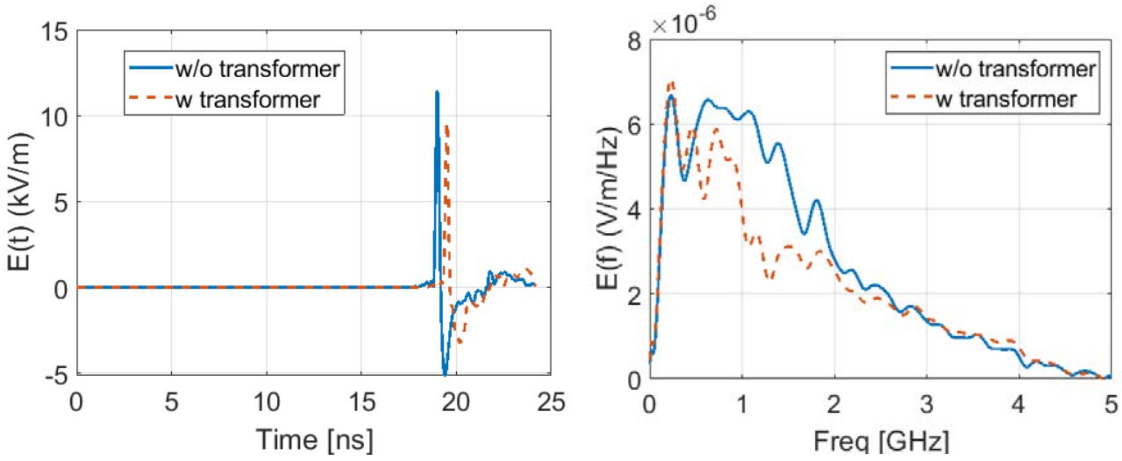
Fig. 8.2.1. Impedance transformer integrated with the Koshelev antenna in CST Studio Suite. (a) Isometric view, and (b) side view.



(a) (b)

Fig. 8.2.2. (a) S_{11} vs frequency and (b) gain vs frequency performance comparison of the Koshelev antenna with and without transformer.

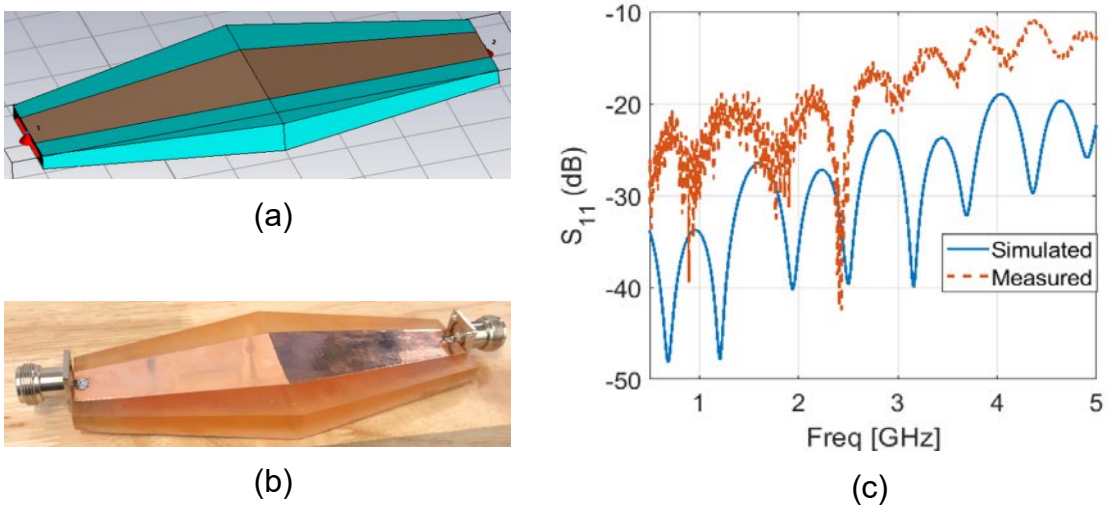
In addition, the electric field response at 5 m distance from the aperture of the antenna is simulated for and is shown in Fig. 8.2.3 (a). The input signal utilized to generate the time-domain electric field response is the megaimpulse waveform with 160 ps rise time and a peak voltage of 5.4 kV. We can notice that the peak field value dropped from 11.5 kV/m to 9.5 kV/m after adding the impedance transformer, showing a 17% reduction. Fig. 8.2.3(b) compares the frequency spectrum of the electric field for both cases. While the electric field response from both cases agreed with each other up to 1 GHz, the difference increases significantly between 1 and 2 GHz.



(a) (b)

Fig. 8.2.3. Comparison of (a) time-domain electric field and (b) frequency spectrum at 5 m distance.

In parallel, an effort to experimentally validate the performance of the impedance transformer was carried out. Fig. 8.2.4 (a), and Fig. 8.2.4 (b) show the CAD model and the fabricated prototype of back-to-back (mirrored) SLA-based impedance transformer. Fig. 8.2.4 (c) compares the S_{11} between the measured and simulated results. The difference in amplitude can be attributed to the material loss factor (loss tangent), which was not considered in the simulation.



(a) (b) (c)

Fig. 8.2.4. Comparison of measured and simulated S_{11} performance of SLA based impedance transformer (a) CAD model, (b) prototype, and (c) S_{11} vs frequency comparison.

The measured data also shifted to the left when compared against simulation data. This phenomenon usually occurs when the total length of the transformer is longer than desired. Overall, the RF performance of the standalone SLA based impedance transformer is satisfactory.

8.2.5 *Summary of Significant Findings and Mission Impact*

(A) An extensive literature search on various UWB antenna elements has resulted in finding three promising options. The down-selected elements are the Koshelev, Shark, and Fractal antennas, which will be extensively studied using their individual design parameter space, which could result in physical aperture area reduction of the single antenna element. Later, the single antenna element will be converted into a planar array.

(B) Initial validation of the Koshelev antenna simulated using CST software agreed well with the antenna metrics published in the open literature [1]. A UWB bandwidth response (10:1 bandwidth) and rE/V > 1 has been observed from our initial simulations of the Koshelev antenna. This validation ensured that the Koshelev antenna can be subjected to further tradespace studies to understand its performance followed by optimizing the design according to OSPRES grant requirements.

(C) The initial tradespace study and analysis of the Koshelev antenna design yielded promising outputs to carry forward the investigation. A comparison of important antenna metrics between the Koshelev antenna in [1] and aperture reduced Koshelev antenna are shown in Table 5.2.1 of the APR 21 MSR.

(D) An in-house code has been developed to calculate important UWB time domain antenna metrics such as full-width half maximum (FWHM) and ringing. These metrics have been calculated using in-house MATLAB code using the excitation voltage and radiated electric field information obtained from CST simulations. FWHM and ringing antenna metrics help with assessing or characterizing an antenna's UWB response.

(E) The tradespace study of feed position provided a deeper understanding of how its position impacts the S11 value bandwidth. An optimum value for feed position i.e., $F = 1/20 < L < 1/10$ is recommended to achieve maximum bandwidth. The tradespace study of the antenna length (L) is straightforward. A longer antenna length will radiate better at lower frequencies. However, physical size restrictions/requirements must be kept in mind in determining the antenna length. Finally, a larger α value (>120°) is recommended to avoid unnecessary reflections from the electric monopole.

(F) From a thorough tradespace study, the aperture size of the Koshelev antenna (single element) is determined to be 90 mm × 100 mm in order to achieve desired antenna metrics performance proposed in the milestone. All metrics described in the milestone have been successfully achieved except the desired bandwidth (200 MHz on both sides) at 900 MHz center frequency. The bandwidth achieved is 900 ± 100 MHz.

(G) The physical aperture area of the Koshelev array antenna largely depends on the interelement spacing and the shape of the array. We were able to determine that the diamond topology is the optimum shape for the Koshelev array antenna. We were also able to obtain similar gain profile (peak gain and pattern) from making certain elements within the array passive (off state) when compared against regular active array (all elements in on state). From the non-symmetric interelement spacing values, we found that S_y has the least effect on the output; therefore a small spacing value can be chosen to reduce the physical aperture area of the Koshelev array.

(H) The literature search on the special EM techniques expanded our knowledge and opened the door to opportunities to apply some of those techniques to the antennas under study. EM techniques such as non-symmetric and non-square array topologies have been applied to the development and study of the Koshelev array antenna.

(I) The first impedance taper design under consideration has shown good S11 values (< –10 dB) over the frequency range of interest. In addition, we have shown that the shape of the pulse can be easily retained at the output of the taper with less than 5% amplitude losses.

(J) The Koshelev antenna array response from feeding a monopolar vs bipolar signal has demonstrated a clear winner: that is, a bipolar signal will radiate at least 10 times better than a monopolar signal. A comparison of the frequency spectrum of the radiated electric field from the optimized Koshelev antenna array between different monopolar pulse sources has identified the 'MI0731' pulse to be the optimum pulse.

(K) The optimized Koshelev antenna array was studied for the electric field response under different array excitation patterns. The study determined that the uniform and Gaussian excitation patterns were the optimum excitation patterns. Selecting the uniform or Gaussian excitation pattern would yield the maximum electric field at the boresight for an arbitrary input signal.

(L) Two variants (Cu-foil plated and silver painted) of the 3D-printed Koshelev antenna have been fabricated to demonstrate a working antenna prototype. The measured S_{11} result of the Cu-foil plated variant showed poor performance due to issues at the transformer–antenna interface. To identify the root cause of the above issue, we have fabricated and tested a standalone impedance transformer component, which displayed good measurement values. On the other hand, the combined simulation of transformer–antenna design yielded slightly degraded S_{11} when compared to the standalone Koshelev antenna design due to field discontinuity at the interface.

8.2.6 *References*

[1] Gubanov, V. P., et al. "Sources of high-power ultrawideband radiation pulses with a single antenna and a multielement array." *Instruments and Experimental Techniques* 48.3 (2005): 312-320.

8.3 Machine Learning Inspired Tradespace Analysis of UWB Antenna Arrays

(Sai Indharapu and Kalyan Durbhakula)

8.3.1 *Problem Statement, Approach, and Context*

Primary Problem: Determine the extent to which the physical aperture area of an antenna array, composed of antenna elements, can be reduced while maintaining performance in peak power density, bandwidth, and electronic beam steerability over the UHF range (0.4–1 GHz), compared with present-art high-power-microwave-capable antenna arrays.

Solution Space: Fractal antennas possess exceptional fidelity factor values (>0.9), which describe how well the shape of the input pulse is retained at an observation point in the far-field. Their high degree of freedom provides an opportunity to develop systematically modified patch shapes, which in turn leads to improved bandwidth while retaining high fidelity factor values. Machine learning (ML) can be leveraged to predict the antenna array response for an arbitrary design parameter space upon sufficient training and validation.

Sub-Problem:

(i) Fractal antennas generate omni-directional radiation patterns in the H-plane over the desired frequency range.

(ii) ML can suffer from underfitting or overfitting the training model which in turn leads to deviations in the predicted output.

State-of-the-Art (SOTA): Conventional full-wave EM solvers such as method of moments (MoM), multi-level fast multipole method (MLFMM), finite element method (FEM), and finite difference time domain (FDTD) method are currently being used to study, analyze and assess the performance of UWB antennas.

Deficiency in the SOTA: UWB antenna optimization using conventional EM solvers utilizes significant computational time and memory resource.

Solution Proposed:

(i) Design, simulate, validate, and perform a tradespace study on the design parameter space of the selected fractal antenna element using commercially available electromagnetic (EM) wave solvers.

(ii) Train, validate, test and compare multiple ML models for quicker and accurate prediction of antenna array response for different physical aperture areas.

Relevance to OSPRES Grant Objective: The fractal antenna achieves an UWB response, a mandatory requirement of the OSPRES grant objective, in a small volume footprint and similar physical aperture area when compared against the SOTA BAVA, dual ridge horn antennas etc. Furthermore, the microstrip-design-based fractal antenna can efficiently handle electronic steering by integrating the feed network on the same board. This eliminates the need to build a separate feed network external to the fractal antenna using bulky coaxial cables.

Risks, Payoffs, and Challenges:

(i) A majority of the fractal antenna geometries yield an omni-directional pattern in the H-plane, which can be a risk. However, efforts are underway to mitigate this pattern without deteriorating bandwidth.

(ii) Payoffs include developing a library of antenna metrics data for various fractal shapes and sizes.

(iii) Design challenges and numerical calculations with respect to specific fractal shapes could arise after performing a certain number of iterations to further improve the bandwidth.

(iv) Fractal antennas were known to generate gain loss at random frequencies over their operating frequencies. Achieving gain stability over the desired frequency range can be a significant challenge.

8.3.2 *Tasks and Milestones / Timeline / Status*

(A) Perform tradespace analysis of the fractal element radius *b* over the desired frequency range (4 to 12 GHz) using the genetic algorithm (GA) optimization tool available in the commercial electromagnetic (EM) solver FEKO / FEB21 / Complete.

- Milestone: Provide a recommendation of an optimum value of *b* using OPTFEKO to minimize reflection coefficient or S_{11} (< –10 dB).

(B) Perform tradespace study on different fractal shapes by changing the number of fractal segments to understand the effect of this change on the impedance bandwidth / FEB21 / Complete.

- Milestone: Produce a detailed study of the antenna response such as S_{11}, gain, and bandwidth by varying the number of fractal segments.

(C) Apply the GA optimization tool on the fractal side length *b* over a wide frequency range (2 to 12 GHz with 201 discrete frequency points) and number of fractal segments using OPTFEKO on the LEWIS cluster / MAR21 / Complete.

- Milestone: Reduce physical aperture area by 10% of its present design, reported in the FEB MSR, and demonstrate minimal or no change in S_{11}, gain, and fidelity factor values.

(D) Perform a parametric study and analysis of antenna response by varying hexagon radius, *a* / MAR–APR21 / Complete.

- Milestone: Recommend a value of *a* to reduce the physical aperture area and increase aperture efficiency (>50%) with no variation in other antenna metrics.

(E) Frequency scale fractal antenna design such that the center frequency of the resulting antenna equals 1.3 GHz / MAY21 / Complete.

- Milestone: Modify antenna design with a center frequency equal to 1.3 GHz and achieve similar results (3:1 bandwidth at fc = 1.3 GHz, 3 dBi gain and >130% aperture efficiency at 900 MHz) to antenna design at center frequency ~7 GHz.

(F) Design and simulate various array antenna geometries composed of optimized fractal antenna elements (obtained from (E)) to analyze the effect of overall array antenna geometry on the desired array antenna response metrics (i.e., gain vs. frequency, gain vs. elevation angle at constant phi, rE/V, half-power beamwidth and side-lobe level.) / MAY–JUL21 / Complete

- Milestone: Recommend a best possible structure with reduced aperture area and minimal loss in gain.

(G) Apply ML models available in Altair Hyperstudy (2021) on the fractal antenna to try and understand the possibilities and limitations of ML models for fast and efficient antenna metrics prediction and optimization. Expand the prediction capability to time-

domain electric field and antenna pattern using ML models (k-nearest neighbor and linear regression) available in scikit learn on Python programming tool “Anaconda”. / MAY21–FEB22 / Complete.

- Milestone: Recommend most accurate and efficient ML model for a fractal antenna in time-domain and frequency domain.

(H) Apply ML models on the octagon fractal antenna array lattice to extend the prediction capability beyond single element / SEP21–MAY22 / Complete.

- Milestone: Recommend the best suitable ML model implemented/developed using Python programming language for array antenna metrics prediction.

(I) Develop a graphical user interface (GUI) to ease the process of employing ML models to predict the antenna output response/ FEB22–SEP22 / Ongoing.

- Milestone: Incorporate the developed automated data extraction scripts, ML scripts to the GUI to enable user to predict antenna response with shorter time.

8.3.3 *Progress Made Since Last Report*

(I) From the previous version of the GUI, the user was able to give real-time input and visualize the antenna output response. To ease the process of tradespace study, the GUI is updated with the ability to carry out parametric sweep analysis. New widgets are added to the validation window as shown in Fig 8.3.1.

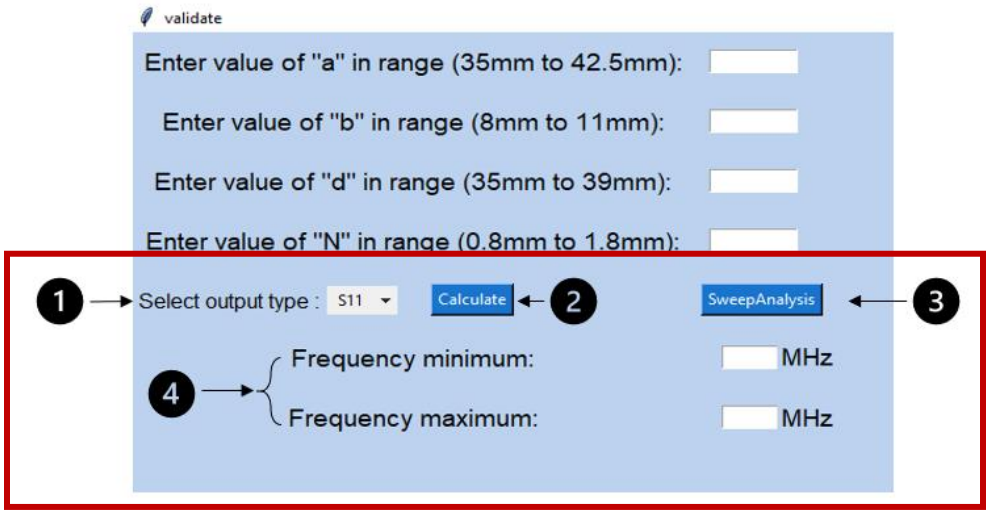


Fig. 8.3.1. Snapshot of updated validation window.

Following are the descriptions for the widgets shown above:

1. The “Select output type” list is used to specify within the GUI the output response type used in the training data.
2. The “Calculate” button is used to predict the output response for the user input.
3. The “SweepAnalysis” button is used to open the parametric sweep window ().
4. “Frequency minimum” & “Frequency maximum” entry fields are used to specify the frequency range of the selected antenna.

The parametric sweep button opens a new window as shown in Fig 8.3.2. The “Parametric Sweep Analysis” window enables the user to specify the input ranges (start & end) of the design parameters and the sampling rate. Further, a drop-down list is added on top of the window to select the sampling type (“Linearly Spaced Values”, “Random values”).

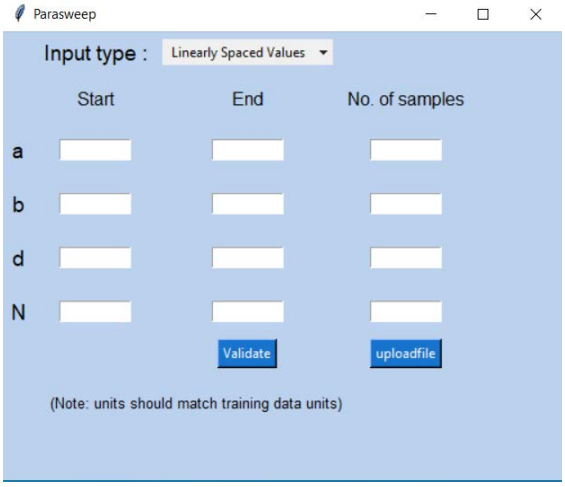


Fig. 8.3.2. Snapshot of the parametric sweep analysis window.

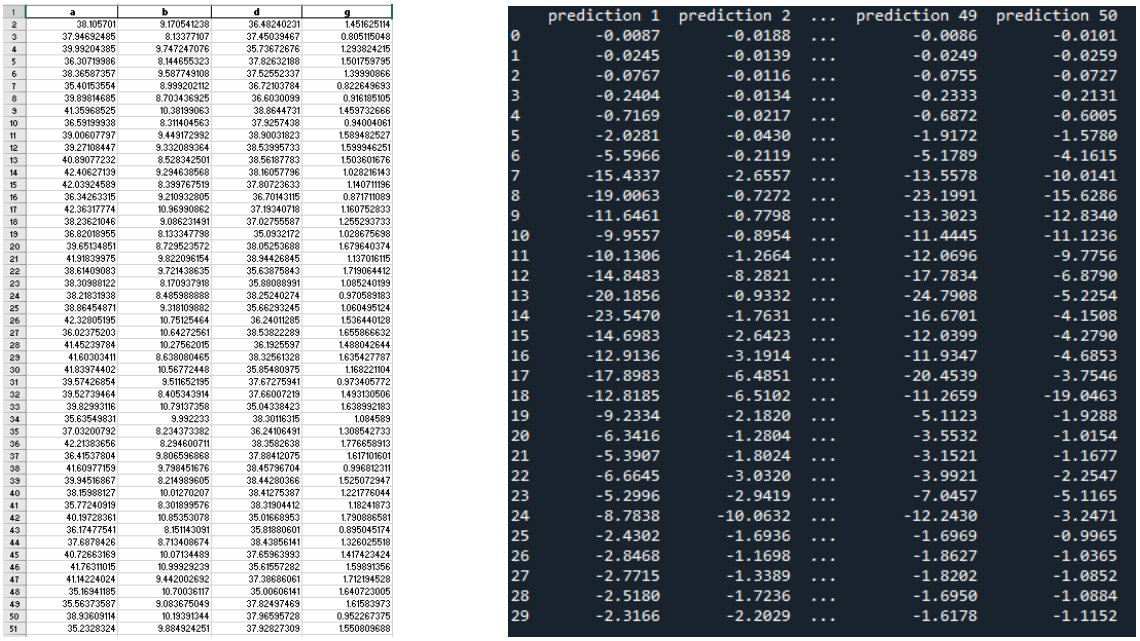
8.3.4 *Technical Results*

(I) To test the updated GUI, a parametric study of S_{11} and Gain is carried out. Following the steps mentioned in the previous MSR, the KNN model is trained using 10 samples of input (design parameters) and output (S_{11} or gain) of a fractal antenna (from the previous MSR).

Below are the steps that should be followed for the parametric study of S_{11}:

1. Specify ‘Frequency minimum’ and ‘Frequency maximum’ using the entry fields in the validation window.
2. Specify the range of interest of each design parameter using the ‘Start’ and ‘End’ entry fields.
3. Specify the number of samples (‘n’) you want to generate between the specified start and end values of design parameters using the ‘No. of samples’ entry fields.
4. Using the drop-down list on the top of the ‘parasweep’ window select the input type.

Upon following the above steps, an excel file containing ‘n=50’ input combinations of design parameters generated is shown in Fig. 8.3.3 (a). In the next step, the GUI will automatically use the generated input combinations in the excel sheet to predict the S_{11} response as illustrated in Fig. 8.3.3 (b).



	a	b	d	g
2	38.105701	9.170541238	36.48240231	1.451625114
3	37.94692485	8.13377107	37.45039467	0.805115048
4	39.99204385	9.747247076	35.73672676	1.293824215
5	36.30719986	8.144655323	37.82632188	1.501759795
6	38.36587357	9.587749108	37.52552337	1.39990866
7	35.40153554	8.999202112	36.72103784	0.822649693
8	39.89814685	8.703436925	36.6030099	0.916185105
9	41.35968525	10.38199063	38.8644731	1.459732666
10	36.59199338	8.311404563	37.3257438	0.94004061
11	39.00607797	9.449172992	38.90031823	1.589482527
12	39.27108447	9.332089364	38.53995733	1.599946251
13	40.89077232	8.528342501	38.56187783	1.503601676
14	42.40627139	9.294638568	38.16057796	1.028216143
15	42.03924589	8.399767519	37.80723633	1.140711196
16	36.34263315	9.210932805	36.70143115	0.871711089
17	42.36317774	10.96990862	37.19340718	1.160752833
18	38.23621046	9.086231491	37.02755587	1.255293733
19	36.82018955	8.133347798	35.0932172	1.028675698
20	39.65134851	8.729523572	38.05253688	1.679640374
21	41.91839975	9.822096154	38.94426945	1.137016115
22	38.61409083	9.721438635	35.63875843	1.719064412
23	38.30988122	8.170937918	35.88088991	1.085240199
24	38.21831938	8.485988888	38.25240274	0.970569183
25	38.86454871	9.318109882	35.66293245	1.060495124
26	42.32805195	10.75125464	36.24011285	1.536440128
27	36.02375200	10.64272561	38.53822289	1.655986632
28	41.45239784	10.27562015	36.1925597	1.489042644
29	41.60303411	8.638080465	38.32561328	1.635427787
30	41.83974402	10.56772448	35.85480975	1.168221104
31	39.57426854	9.511652195	37.67275941	0.973405772
32	39.52739464	8.405343914	37.66007219	1.493130506
33	39.82993116	10.79137358	35.04338423	1.638392183
34	35.63549831	9.992233	38.30116315	1.084589
35	37.03200792	8.234373382	36.24106491	1.309542733
36	42.21383656	8.294600711	38.3582638	1.776658913
37	36.41537804	9.806596868	37.88412075	1.617101601
38	41.60977159	9.798451676	38.45796704	0.996812311
39	39.94516867	8.214989605	38.44280366	1.525072947
40	38.15988127	10.01270207	38.41275387	1.221776044
41	35.77240919	8.301899576	38.31904412	1.18241873
42	40.19728361	10.85353078	35.01668953	1.790886581
43	36.17477541	8.15143091	35.81880601	0.895045174
44	37.6878426	8.713408674	38.43856141	1.326025518
45	40.72663169	10.07124489	37.65963393	1.417423424
46	41.76311015	10.99929239	35.61557282	1.59891356
47	41.14224024	9.442002692	37.38686061	1.712194528
48	35.16941185	10.70036117	35.00606141	1.640723005
49	35.56373587	9.083675049	37.82497469	1.61583973
50	38.93609114	10.19391344	37.96595728	0.952267375
51	35.2328324	9.884924251	37.92827309	1.550809688

(a)

	prediction 1	prediction 2	...	prediction 49	prediction 50
0	-0.0087	-0.0188	...	-0.0086	-0.0101
1	-0.0245	-0.0139	...	-0.0249	-0.0259
2	-0.0767	-0.0116	...	-0.0755	-0.0727
3	-0.2404	-0.0134	...	-0.2333	-0.2131
4	-0.7169	-0.0217	...	-0.6872	-0.6005
5	-2.0281	-0.0430	...	-1.9172	-1.5780
6	-5.5966	-0.2119	...	-5.1789	-4.1615
7	-15.4337	-2.6557	...	-13.5578	-10.0141
8	-19.0063	-0.7272	...	-23.1991	-15.6286
9	-11.6461	-0.7798	...	-13.3023	-12.8340
10	-9.9557	-0.8954	...	-11.4445	-11.1236
11	-10.1306	-1.2664	...	-12.0696	-9.7756
12	-14.8483	-8.2821	...	-17.7834	-6.8790
13	-20.1856	-0.9332	...	-24.7908	-5.2254
14	-23.5470	-1.7631	...	-16.6701	-4.1508
15	-14.6983	-2.6423	...	-12.0399	-4.2790
16	-12.9136	-3.1914	...	-11.9347	-4.6853
17	-17.8983	-6.4851	...	-20.4539	-3.7546
18	-12.8185	-6.5102	...	-11.2659	-19.0463
19	-9.2334	-2.1820	...	-5.1123	-1.9288
20	-6.3416	-1.2804	...	-3.5532	-1.0154
21	-5.3907	-1.8024	...	-3.1521	-1.1677
22	-6.6645	-3.0320	...	-3.9921	-2.2547
23	-5.2996	-2.9419	...	-7.0457	-5.1165
24	-8.7838	-10.0632	...	-12.2430	-3.2471
25	-2.4302	-1.6936	...	-1.6969	-0.9965
26	-2.8468	-1.1698	...	-1.8627	-1.0365
27	-2.7715	-1.3389	...	-1.8202	-1.0852
28	-2.5180	-1.7236	...	-1.6950	-1.0884
29	-2.3166	-2.2029	...	-1.6178	-1.1152

(b)

Fig. 8.3.3. (a) Snapshot of input excel sheet generated using GUI, (b) S_{11} prediction for generated input.

Finally, the maximum bandwidth is calculated from the predicted output of every input combination. A 2D plot with input number (1-n) on the x-axis and bandwidth on the y-axis is added to the validation window. A text field is added below the plot to display the maximum bandwidth observed and the corresponding input as shown in the Fig. 8.3.4.

Similarly, below are steps that should be followed for parametric study of Gain:

1. Specify ‘Frequency minimum’ and ‘Frequency maximum’ using the entry fields in the validation window.
2. Specify the range of interest of each design parameter using the ‘Start’ and ‘End’ entry fields.
3. Specify the number of samples (‘n’) you want to generate between the specified start and end values of design parameters using the ‘No. of samples’ entry fields.
4. Using the drop-down list on the top of the ‘parasweep’ window select the input type.

The process of generating the input file is similar to the S_{11} analysis. Following the above steps, a new input excel file containing ‘n = 50’ input combinations of design parameters is generated for the gain analysis using the GUI as shown in Fig. 8.3.5 (a). Further, the GUI will automatically use the generated input excel file to predict the gain response as illustrated in Fig. 8.3.5 (b). The developed GUI can predict and analyze any number of input samples (‘n’) within no time.

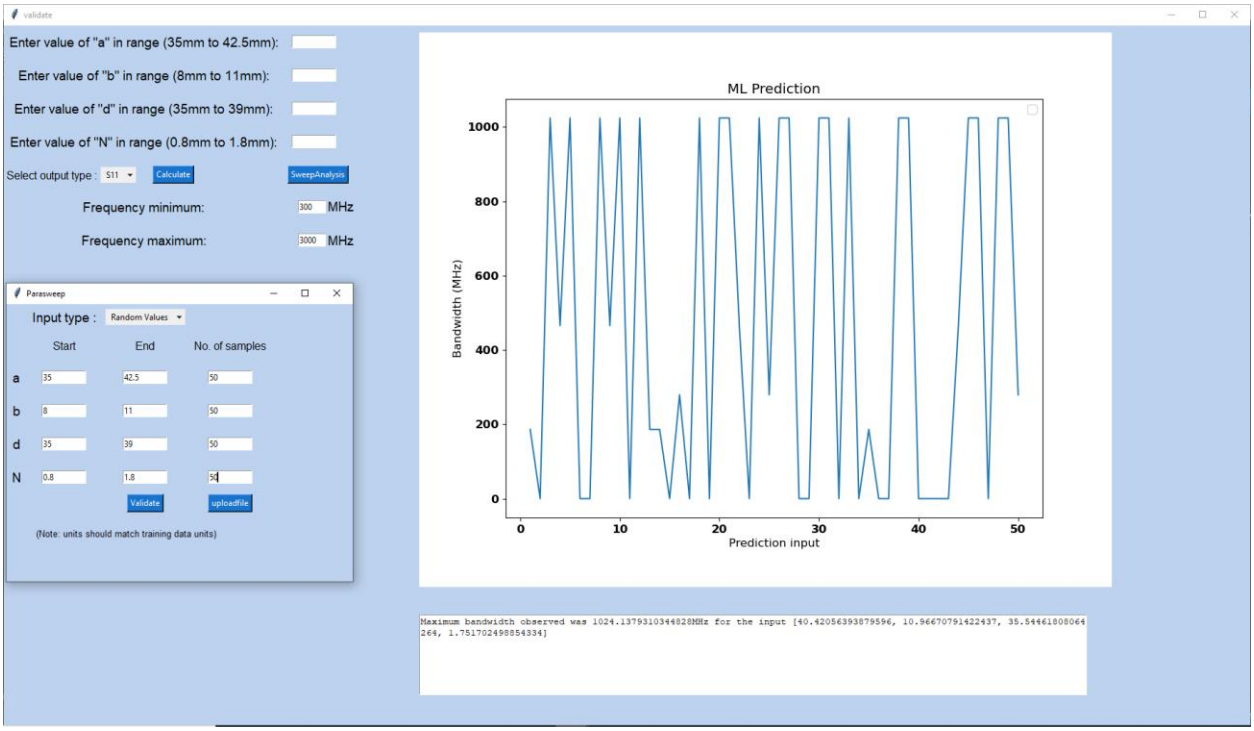


Fig. 8.3.4. Snapshot of validation window with final 2D plot and the text field.

	a	b	d	g
2	38.105701	9.170541238	36.48240231	1.451625114
3	37.94692485	8.13377107	37.45039467	0.805115048
4	39.99204385	9.747247076	35.73672676	1.293824215
5	36.30719986	8.144655323	37.82632188	1.501759795
6	38.36587357	9.587749108	37.52552337	1.39990866
7	35.40853554	8.999202112	36.72103784	0.822649693
8	39.89814685	8.703436925	36.6030099	0.916185105
9	41.35968525	10.38199063	38.8644731	1.459732666
10	36.59199938	8.311404563	37.9257438	0.94004061
11	39.00607797	9.449172992	38.90031823	1.589482527
12	39.27108447	9.332089364	38.53995733	1.599946251
13	40.89077232	8.528342501	38.56187783	1.503601676
14	42.40627139	9.294638568	38.16057796	1.028216143
15	42.03924589	8.399767519	37.80723633	1.140711196
16	36.34263315	9.210932805	36.70143115	0.871711089
17	42.36317774	10.96990862	37.19340718	1.160752833
18	38.23621046	9.086231491	37.02755587	1.255293733
19	36.82018955	8.133347798	35.0932172	1.028675698
20	39.65134851	8.729523572	38.05253688	1.679640374
21	41.91839975	9.822096154	38.94426845	1.137016115
22	38.61409083	9.721438635	35.63875843	1.719064412
23	38.30988122	8.170937918	35.88088391	1.086240199
24	38.21831938	8.485988888	38.25240274	0.970589183
25	38.86454871	9.318109882	35.66293245	1.060495124
26	42.32805195	10.75125464	36.24011285	1.536440128
27	36.02375203	10.64272561	38.53822289	1.655866632
28	41.45239784	10.27562015	36.1925597	1.488042644
29	41.60303411	8.638080465	38.32561328	1.635427787
30	41.83974402	10.56772448	35.85480975	1.16822104
31	39.57426854	9.51165219	37.67275941	0.973405772
32	39.52739464	8.405343914	37.66007219	1.493100506
33	39.82393116	10.79137358	35.04338423	1.638992183
34	35.63549831	9.992233	38.30116315	1.084589
35	37.03200792	8.234373382	36.24106491	1.308542733
36	42.21383656	8.294600711	38.3582638	1.776658913
37	36.41537804	9.806596868	37.88412075	1.617101601
38	41.60977159	9.798451676	38.45796704	0.996812311
39	39.94516867	8.214989605	38.44280366	1.525072947
40	38.15988127	10.01270207	38.41275387	1.221776044
41	35.77240919	8.301899576	38.31904412	1.18241873
42	40.19728361	10.85353078	35.01668953	1.790886581
43	36.17477541	8.151143091	35.81880601	0.895045174
44	37.6878426	8.713408674	38.43856141	1.326025518
45	40.72663169	10.07134489	37.65963993	1.417423424
46	41.76311015	10.99929239	35.61557282	1.59891356
47	41.14224024	9.442002692	37.38686061	1.712194528
48	35.16941185	10.70036117	35.00606141	1.640723005
49	35.56372587	9.083675049	37.82497469	1.61583973
50	38.9360114	10.19391344	37.96595728	0.952267375
51	35.2328324	9.884924251	37.92827309	1.550809688

(a)

	prediction 1	prediction 2	...	prediction 49	prediction 50
0	-10.0436	-10.0436	...	-10.2411	-9.4640
1	-2.3082	-2.3082	...	-2.2968	-1.8182
2	0.3193	0.3193	...	0.3687	0.5302
3	1.0808	1.0808	...	1.1482	1.1839
4	1.3292	1.3292	...	1.3746	1.3865
5	1.5745	1.5745	...	1.5477	1.6075
6	1.7102	1.7102	...	1.6788	1.7388
7	1.7494	1.7494	...	1.7271	1.7802
8	1.7984	1.7984	...	1.7549	1.8238
9	1.8965	1.8965	...	1.8167	1.9044
10	2.0623	2.0623	...	1.9375	2.0479
11	2.2933	2.2933	...	2.0979	2.2341
12	2.5962	2.5962	...	2.2826	2.4659
13	2.9497	2.9497	...	2.6142	2.8442
14	3.2466	3.2466	...	2.9318	3.2182
15	3.2726	3.2726	...	3.2348	3.5532
16	2.4390	2.4390	...	3.3711	3.7173
17	-0.1745	-0.1745	...	3.1460	3.6342
18	5.3496	5.3496	...	4.3556	4.7326
19	4.8332	4.8332	...	0.9101	-0.7472
20	2.5185	2.5185	...	-2.1573	-3.5701
21	0.3924	0.3924	...	-3.6758	-4.8063
22	-1.4768	-1.4768	...	-4.2578	-5.0758
23	-3.3024	-3.3024	...	-3.9155	-4.5548
24	-10.0345	-10.0345	...	-10.5979	-11.5076
25	-12.2958	-12.2958	...	-11.2490	-13.8058
26	-15.3074	-15.3074	...	-13.9813	-16.8822
27	-15.1319	-15.1319	...	-18.5755	-18.0369
28	-12.5306	-12.5306	...	-23.8826	-15.4067
29	-10.2157	-10.2157	...	-18.0834	-12.4625

(b)

Fig. 8.3.5. (a) Snapshot of input excel sheet generated using GUI, (b) Gain prediction for generated input.

Finally, A 2D plot with input number (1–n) on the x-axis and gain at a center frequency on the y-axis is added to the validation window. A text field is added below the plot to display the peak observed and the corresponding input as shown in Fig. 8.3.6.

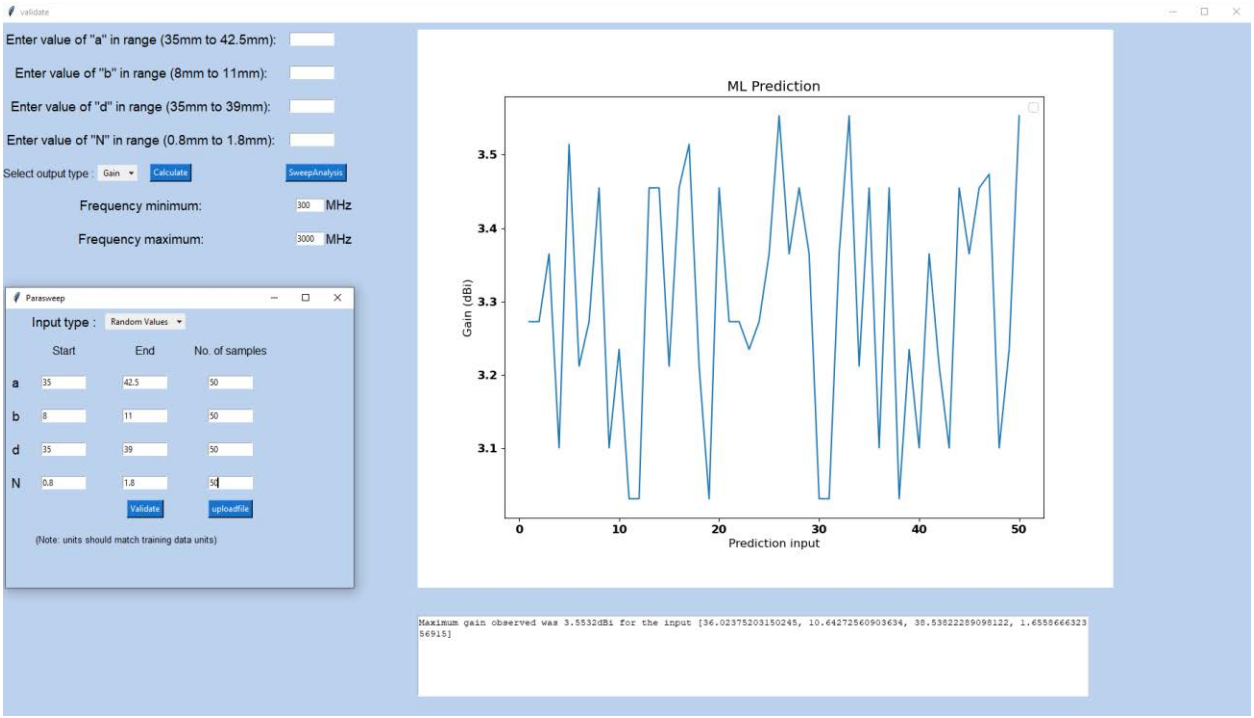


Fig. 8.3.6. Snapshot of validation window with final 2D plot and the text field.

8.3.5 *Summary of Significant Findings and Mission Impact*

(A) We carried out an effort to identify the dominant fractal antenna design parameter and its corresponding value using parameter study and FEKO optimization tool. It was found that the side length 'b' of the fractal elements play a significant effect on the antenna bandwidth. The initial analysis of the simulation results with fractal radius *b* equal to 1.8 mm yielded multiple resonant frequencies with enhanced bandwidth. To further increase the bandwidth, OPTFEKO was used as an optimization tool with fractal radius *b* as the optimization variable. Finally, the optimum value for *b* is found to be 1.66 mm which minimizes the S_{11} (-10 dB).

(B) The addition of fractal elements (*N*) to the simple hexagon improved antenna metrics such as reflection coefficient (S_{11}). To further investigate and understand the fractal elements, the number of segments (sides of the fractal element) in the fractal geometry were varied within the range of 6 to 14. By varying the number of segments in the fractal element, the resultant S_{11} response has positive impact at higher frequencies and negative impact at lower frequencies. Therefore, the number of segments of the fractal element were chosen to be 6 as it has better balance of S_{11} values both at lower and higher frequencies.

(C) The initial optimum value of *b* over 51 discrete frequency points is reported as 1.66 mm in task (A). To further increase the accuracy of the optimization algorithm and to

find a more precise value for *b*, optimization is further performed over a wider frequency range (201 discrete points between 2 GHz to 12 GHz) which yielded an optimum value of *b* as 1.37 mm. The S_{11} response of the antenna design with this newly obtained *b* parameter (i.e., 1.37 mm) has not produced any better bandwidth compared to *b* = 1.66 mm. Thus, *b* is set to be 1.66 mm for further research.

(D) The hexagonal patch radius *a* has a significant effect on the physical aperture area of the antenna. Therefore, Altair OPTFEKO has been utilized to find an optimum *a* value, which was determined to be 8 mm over the range 7.2 to 9 mm. Antenna metrics such as S_{11}, gain, and bandwidth have shown desired performance with the optimized *a* value.

(E) The initial antenna design has been modified to achieve a center frequency of ~1.3 GHz. The gain value at 900 MHz is 3.5 dBi and, with the modified antenna design, we were able to achieve an impedance bandwidth ratio of 3.3:1. The designed antenna has been fabricated and tested, and the S_{11} response of the fabricated antenna agrees well when compared against FEKO, CST.

(F) Four different fractal antenna array geometries (i.e., square, diamond, hexagon, and octagon) have been designed and simulated. Upon comparing antenna array metrics, the octagonal fractal antenna array has yielded minimal sidelobe levels with a gain of 15.7 dBi at 900 MHz, close to that of the square geometry but with with 32.27% lower physical aperture area. The octagonal fractal antenna array has been chosen as the optimum geometry with reduced aperture area and reduced side lobes while retaining the bandwidth and gain milestone metrics.

(G) The ML models available (radial basis function (RBF), least square regression (LSR) and, hyper kriging (HK)) in Altair Hyperstudy were employed to predict the output response of a fractal antenna. From the above mentioned ML models RBF and LSR were down selected from the initial three ML models based upon their generalization capability for prediction of reflection coefficient (S_{11}), gain, and electric field. Further analysis of increasing training data set size has shown no improvement in prediction accuracy of antenna output response. Trained ML models were tested for design variable values outside the training range. The resulting RMSE increased as the values drifted away from the mid-point of the training range. RBF performed well in the prediction of S_{11}, while LSR performed slightly better for gain and electric field predictions. In addition, for time-domain electric field prediction, we recommend using k-nearest neighbors (kNN) ML algorithm for accurate prediction.

(H) The initial application of the kNN ML model for the prediction of antenna array bandwidth response of center and corner element yielded positive results with a good agreement between traditional EM solver (FEKO) and trained kNN ML model. The new LR ML model yielded improved RMSE values (over kNN) in its prediction of reflection coefficient (27.82% less RMSE for center element and 19.76% less RMSE for corner element). On the other hand, the RMSE values for gain (as function of theta) prediction using LR ML model has 55.51% increase over kNN prediction. Finally, kNN provides better generalization to predict reflection coefficient, whereas LR provides better generalization to predict frequency domain gain in the case of a fractal antenna array. Further, the application of the AEP method for antenna array

has many limitations and is applicable only for square antenna geometry. As a result, the study and application of the AEP method was put on hold.

(l) A GUI is currently under development, which accepts training data for an antenna (single-element or array) of user choice and can predict output response (S_{11} and gain) for a range of test data within a few seconds. The GUI can significantly help users with carrying out the tradespace study in a short time. Therefore, users can build/prototype the desired antenna design quickly.

8.3.6 *References*

[1] H. Fallahi and Z. Atlasbaf, "Study of a Class of UWB CPW-Fed Monopole Antenna With Fractal Elements," in IEEE Antennas and Wireless Propagation Letters, vol. 12, pp. 1484-1487, 2013, doi: 10.1109/LAWP.2013.2289868.

[2] S. Zhang, X. Wang and L. Chang, "Radiation Pattern of Large Planar Arrays Using Four Small Subarrays," in IEEE Antennas and Wireless Propagation Letters, vol. 14, pp. 1196-1199, 2015, doi: 10.1109/LAWP.2015.2397600.

9 Feedback

There is no feedback to report for the current reporting period.

10 Program Management

10.1 Issues

i. Scope – No issues
ii. Budget – 12-month NCTE submitted/pending
iii. Schedule – No issues

10.2 Interactions with Others

Agency/Org	Performer	Project Name	Purpose of Research/ Collaboration

10.3 Major Procurement Actions

10.4 Travel

Destination	Purpose	Attendees	Estimated Costs

10.5 Pending or Upcoming Public Release Requests

11 Appendix A: Academic and IP Output

11.1 Students Graduated

Name	Degree	Currently
Al-Shaikhli, Waleed Azad, Wasekul	MS Spring 19 PhD Summer 21	Kansas City National Security Campus, Honeywell Applied Materials, Sunnyvale, CA
Berg, Jordan	MS Spring 21	MRI Global
Bhamidipati, John	PhD Spring 22	MIDE
Bissen, Bear	MS Spring 19	Kansas City National Security Campus, Honeywell
Brasel, Sadie	BS Spring 21	
Floyd, Dennis	BS	Naval Air Warfare Center Weapons Division
Hanif, Abu	PhD Spring 21	
Harmon, Aaron	BS	Missouri University of Science & Technology
Harp, Joshua	MS	
Hauptman, Cash	BS Spring 18	University of Nebraska-Lincoln
Klappa, Paul	MS Spring 21	
Kovarik, James	MS 21	
Labrada, Dario	BS Spring 20	Honeywell Aerospace, Florida
Lancaster, John	MS Spring 17	Lawrence Livermore National Laboratory
Renzelman, Jeff	MS Spring 18	Kansas City National Security Campus, Honeywell
Roy, Sourov	PhD Spring 21	
Wagner, Adam	MS Fall 20	Kansas City National Security Campus, Honeywell
Xia, Shengxuan	BS	Missouri University of Science & Technology

11.2 Journal Publications

11.2.1 *In Preparation*

[1] J. K. P Bhamidipati, G. Bhattarai, A. N. Caruso, “Effect of Proton Irradiation Induced Localized Defect/Trap Clusters on Silicon Photoconductive Semiconductor Switch (Si-PCSS) Recovery Time and Leakage currents,” *Solid-State Electronics,* In Preparation, **2022**.

[2] N. Gardner, K. C. Durbhakula, and A. N. Caruso, “UHF and L-Band Frequency Generation at MW Peak Power using Diode-based Nonlinear Transmission Lines as Pulse Forming Networks,” *Transactions on Plasma Science*, In Preparation, **2022**.

[3] N. Gardner, K. C. Durbhakula, and A. N. Caruso, “Electrically Tunable Diode-based Nonlinear Transmission Line,” *TBD*, In Preparation, **2022**.

[4] B. Barman, D. Chatterjee, K. C. Durbhakula, and A. N. Caruso, “Tradespace Analysis of Wideband, Electrically Small Microstrip Patch Antenna Elements for Phased Array Applications,” *IEEE Antennas and Propagation Magazine,* In preparation, **2021**.

[5] S. Xia, J. Hunter, A. Harmon, M. Hamdalla, A. Hassan, V. Khilkevich, D. Beetner, "Simulation Driven Statistical Analysis of the Electro-magnetic Coupling to Microstriplines," *IEEE Transactions on Electromagnetic Compatibility*, In Preparation, **2020**.

[6] M. Hamdalla, V. Khilkevich, D. G. Beetner, A. N. Caruso, A. M. Hassan, "Characteristic Mode Analysis Justification of the Stochastic Electromagnetic Field Coupling to Randomly Shaped Wires," *IEEE Transactions on Electromagnetic Compatibility*, In Preparation, **2020**.

11.2.2 *Submitted / Under Revision*

[7] J. K. P. Bhamidipati, E. R. Myers, A. M. Conway, L. F. Voss, M. M. Paquette, and A. N. Caruso, "Figure of Merit Development for Linear-Mode Photoconductive Solid-State Switches," *IEEE Journal of the Electron Devices Society*, Submitted May 1 **2022**, Manuscript ID#JEDS-2022-05-0136-R.

[8] J. K. P. Bhamidipati, K. C. Durbhakula, and A. N. Caruso, "A Dynamically Tunable Discrete-Element Transmission Line Pulse Generator," *International Journal of Electronics and Communications*, Submitted March 6 **2022**, Manuscript ID#AEUE-S-22-01270.

[9] B. Barman, K. C. Durbhakula, D. Chatterjee, and A. N. Caruso, "Comparison of Machine Learning Algorithms for Bandwidth Enhancement of a Coaxial Probe-fed Microstrip Patch Antenna," *Applied Computational Electromagnetics Society (ACES)*, Submitted, **2021**.

[10] B. K. Lau, M. Capek, and A. M. Hassan, "Characteristic Modes–Progress, Overview, and Future Perspectives," *IEEE Antennas and Propagation Magazine*, Submitted, **2021**.

[11] K. Alsultan, M. Z. M. Hamdalla, S. Dey, P. Rao, and A. M. Hassan, "Scalable and Fast Characteristic Mode Analysis Implementation Using a Hybrid CPU/GPU Platform," *ACES*, Submitted, **2021**.

[12] W. Azad, F. Khan, and A. N. Caruso, "A Scalable Multilevel-Modular 10 kV Silicon Carbide MOSFET Module Featuring Custom Isolated Gate Driver Circuit Combined with Coupling and Snubber Circuits," *IEEE Transactions on Power Electronics*, Submitted, **2021.**

11.2.3 *Published / In Press*

[13] N. Gardner, K. C. Durbhakula and A. N. Caruso, "Design Considerations for Diode-Based Nonlinear Transmission Lines," *AIP Advances*, 12, 055012, **2022** [doi].

[14] J. N. Berg, R. C. Allen, and S. Sobhansarbandi. "A Novel Method of Cooling a Semiconductor Device through a Jet Impingement Thermal Management System: CFD Modeling and Experimental Evaluation." *International Journal of Thermal Sciences*, 172, 107254, **Feb 2022** [doi].

[15] M. Z. M. Hamdalla, B. Bissen, J. Hunter, Y. Liu, V. Khilkevich, D. G. Beetner, A. N. Caruso, and A. M. Hassan, "Characteristic Mode Analysis Prediction and Guidance

of Electromagnetic Coupling Measurements to a UAV Model," *IEEE Access*, 10, 914–925, **Dec 2021** [doi].

[16] W. Azad, F. Khan, and A. N. Caruso, "A Medium Power, Self-Sustaining, Configurable RF Pulse Generation Circuit Using a Nonlinear Transmission Line and Power Amplifier in a Closed Loop Configuration, *IEEE Transactions on Plasma Science*, vol. 49, no. 7, pp. 2183–2194, **July 2021** [doi].

[17] S. Roy, W. Azad, S. Baidya and F. Khan, "A Comprehensive Review on Rectifiers, Linear Regulators and Switched-Mode Power Processing Techniques for Biomedical Sensors and Implants utilizing In-body Energy Harvesting and External Power Delivery," *IEEE Transactions on Power Electronics*, vol. 36, no. 11, pp. 12721–12745, **Nov 2021** [doi].

[18] K. C. Durbhakula, D. Chatterjee, and A. M. Hassan, "An Efficient Algorithm for Locating TE and TM Poles for a Class of Multiscale Inhomogeneous Media Problems," *IEEE Journal on Multiscale and Multiphysics Computational Techniques*, vol. 4, no. 1, pp. 364–373, **2019** [doi].

11.3 Conference Publications

11.3.1 *Submitted / Accepted*

[1] B. Barman, D. Chatterjee, and A. N. Caruso, "Characterization of Planar Phased Arrays of Electrically Small UWB Microstrip Patch Antennas," *2022 IEEE International Symposium on Phased Array and Technology,* Waltham, Massachusetts, USA, Oct. 11-14, 2022, pp. 1-8. (Submitted).

[2] B. Barman, D. Chatterjee, and A. N. Caruso, "On the Optimum Substrate Selection in Wideband Microstrip Patch Antenna Design," *2022 IEEE International Symposium on Antennas & Propagation & USNC-URSI Radio Science Meeting*, Denver, Colorado, USA, July 10-15, 2022, pp. 1-2. (Accepted)

[3] B. Barman, D. Chatterjee, and A. N. Caruso, "Time Domain Analysis of an UWB Electrically Small Microstrip Patch Antenna," *2022 IEEE International Symposium on Antennas & Propagation & USNC-URSI Radio Science Meeting*, Denver, Colorado, USA, July 10-15, 2022, pp. 1-2. (Accepted)

11.3.2 *Presented*

[4] S. R. Shepard and H. A. Thompson, "Self-focusing in Guided and Un-guided Media," submitted to the *2021 OSA Nonlinear Optics Topical Meeting, Virtual Event*, August 9-13, 2021.

[5] B. Barman, D. Chatterjee and A. N. Caruso, "Probe-location Optimization in a Wideband Microstrip Patch Antenna using Genetic Algorithm, Particle Swarm and Nelder-Mead Optimization Methods," *2021 International Applied Computational Electromagnetics Society Symposium (ACES)*, 2021, pp. 1-3 [doi].

[6] W. Azad, S. Roy, and F. Khan, "A Single Gate Driver-based Four-stage High-voltage SiC Switch Having Dynamic Voltage Balancing Capability," *2021 IEEE Applied Power Electronics Conference and Exposition* (APEC), Phoenix, AZ, USA, June 9-12, 2021.

[7] W. Azad, S. Roy, F. Khan and A. N. Caruso, "A Multilevel-Modular 10 kV Silicon Carbide MOSFET Module using Custom High-Voltage Isolated Gate Driver, Coupling, and Snubber Circuits," *2021 IEEE Kansas Power and Energy Conference* (KPEC), Manhattan, KS, USA, April 19-20, 2021 [doi].

[8] T. Layman, T. D. Fields, and O. A. Yakimenko, "Evaluation of Proportional Navigation for Multirotor Pursuit," AIAA SciTech Forum, Virtual Event, January 11-21, 2021 [doi].

[9] P. J. Klappa, and T. D. Fields, "Assessment of Fixed-Wing UAV System Identification Models during Actuator and Payload Drop Failures," AIAA Atmospheric Flight Mechanics Conference, Virtual Event, January 11-21, 2021 [doi].

[10] J. Hunter, S. Xia, A. Harmon, A. M. Hassan, V. Khilkevich, and D. Beetner, "Modeling and Statistical Characterization of Electromagnetic Coupling to Electronic Devices," *IEEE International Symposium on Antennas and Propagation and NSRM USNC-URSI National Radio Science Meeting*, Boulder, CO, January 4-9, 2021 [doi].

[11] B. Barman, K. C. Durbhakula, B. Bissen, D. Chatterjee, and A. N. Caruso, "Performance Optimization of a Microstrip Patch Antenna using Characteristic Mode and D/Q Analysis," *2020 XXXIIIrd General Assembly and Scientific Symposium of the International Union of Radio Science*, Rome, Italy (online conference), Aug 29-Sept 5, 2020, pp. 1-4 [doi].

[12] J. Berg, and S. Sobhansarbandi. "CFD Modeling of Thermal Management Systems for a Silicon Semiconductor Switch." *ASME 2020 Heat Transfer Summer Conference collocated with the ASME 2020 Fluids Engineering Division Summer Meeting and the ASME 2020 18th International Conference on Nanochannels, Microchannels, and Minichannels*, Virtual, July 13–15, 2020, American Society of Mechanical Engineers Digital Collection [doi].

[13] B. Barman, D. Chatterjee, and A. N. Caruso, "Performance Optimization of Electrically Small Microstrip Patch Antennas on Finite Ground Planes," 2020 *IEEE International Symposium on Antennas and Propagation and North American Radio Science Meeting*, Montreal, Quebec, Canada, July 5-10, 2020, pp. 1–2 (online conference) [doi].

[14] M. Hamdalla, B. Bissen, A. N. Caruso, and A. M. Hassan, "Experimental Validations of Characteristic Mode Analysis Predictions Using GTEM Measurements," *IEEE International Symposium on Antennas and Propagation and USNC-URSI Radio Science Meeting,* Montréal, Québec, Canada, July 5-10, 2020 [doi].

[15] K. Alsultan, P. Rao, A. N. Caruso, and A. M. Hassan, "Scalable Characteristic Mode Analysis: Requirements and Challenges (White Paper)," *Large Scale Networking*

(LSN) Workshop on Huge Data: A Computing, Networking and Distributed Systems Perspective Sponsored by NSF, Chicago, IL, April 13-14, 2020.

[16] M. Hamdalla, A. N. Caruso, and A. M. Hassan, “Predicting Electromagnetic Interference to a Terminated Wire Using Characteristic Mode Analysis,” *Proceedings of the Annual Review of Progress in Applied Computational Electromagnetics (ACES)*, Monterey, CA, March 22-26, 2020. [doi]

[17] W. Azad, F. Khan, and A. Caruso, "Self-sustaining High-power RF Signal Generation Using LDMOS Based Power Amplifier and Nonlinear Transmission Line," *2020 IEEE Applied Power Electronics Conference and Exposition (APEC)*, New Orleans, LA, USA, March 15-19 2020, pp. 3567-3572 [doi].

[18] A. Hanif, W. Azad, and F. Khan, "Detection of Bond Wire Lift Off in IGBT Power Modules Using Ultrasound Resonators," *2020 IEEE Applied Power Electronics Conference and Exposition (APEC)*, New Orleans, LA, USA, March 15-19 2020, pp. 345-350 [doi].

[19] B. Barman, D. Chatterjee, and A. N. Caruso, “Some Investigations into Mutual Coupling Analysis for Trade Space Studies of Linear Arrays,” *2019 IEEE International Symposium on Phased Array Systems and Technology (PAST)*, Waltham, MA, October 2019, pp. 1-8 [doi].

[20] B. Barman, D. Chatterjee, and A. N. Caruso, “Characteristic Mode Analysis of a straight and an L-probe fed Microstrip Patch,” *2019 IEEE Indian Conference on Antennas and Propogation (InCAP)*, Ahmedabad, India, Dec 2019, pp. 1-3 [doi].

[21] M. Hamdalla, A. N. Caruso, and A. M. Hassan, "Characteristic Mode Analysis of the Effect of the UAV Frame Material on Coupling and Interference," *IEEE International Symposium on Antennas and Propagation and USNC-URSI Radio Science Meeting at Atlanta (2 pages)*, Georgia, USA, July 7-12, 2019 [doi].

[22] M. Hamdalla, J. Hunter, Y. Liu, V. Khilkevich, D. Beetner, A. Caruso, and A. M. Hassan, "Electromagnetic Interference of Unmanned Aerial Vehicles: A Characteristic Mode Analysis Approach," *IEEE International Symposium on Antennas and Propagation and USNC-URSI Radio Science Meeting at Atlanta (2 pages)*, Georgia, USA, July 7-12, 2019 [doi].

[23] K. C. Durbhakula, J. Lancaster, A. M. Hassan, D. Chatterjee, A. N. Caruso, J. D. Hunter, Y. Liu, D. Beetner, and V. Khilkevich, "Electromagnetic Coupling Analysis of Printed Circuit Board Traces using Characteristic Mode Analysis," *IEEE International Symposium on Antennas and Propagation and USNC-URSI Radio Science Meeting (2 pages)*, Atlanta, Georgia, USA, July 7-12 2019 [doi].

[24] K. C. Durbhakula, D. Chatterjee, and A. M. Hassan, “On the Location of Transverse Electric Surface Wave Poles for Electrically Thick Substrates,” Proceedings of the *IEEE Antennas and Propagation International Symposium and National Radio Science Meeting*, Atlanta, Georgia, USA, July 7-12, 2019 [doi].

[25] W. Azad and F. Khan, “Sustaining High-power RF Signal Generation in a Positive Feedback Network," *2019 IEEE Pulsed Power and Plasma Science Conference (PPPS)*, Orlando, FL, USA, June 23-28 2019.

[26] K. Alsultan, P. Rao, A. N. Caruso, and A. M. Hassan, “Scalable characteristic mode analysis using big data techniques,” *International Symposium on Electromagnetic Theory (EMTS 2019)*, San Diego, CA, USA, May 27-31, 2019.

[27] M. Hamdalla, W. Al-Shaikhli, J. Lancaster, J. D. Hunter, L. Yuanzhuo, V. Khilkevich, D. G. Beetner, A. N. Caruso, and A. M. Hassan, “Characteristic Mode Analysis of Electromagnetic Coupling to Wires with Realistic Shapes,” *International Symposium on Electromagnetic Theory (EMTS 2019)*, San Diego, CA, USA, May 27-31, 2019.

[28] K. C. Durbhakula, D. Chatterjee, and A. M. Hassan, “Location of Surface Wave Poles in Sommerfeld Integrals: A Mittag-Leffler Expansion Approach,” *Proceedings of the URSI-B International Symposium on Electromagnetic Theory*, URSI Commission, San Diego, USA, May 2019 [doi].

[29] K. C. Durbhakula, D. Chatterjee and A. M. Hassan, “Analytical Evaluation of Sommerfeld Integral Tails Present in Two-layered Media Green’s Functions,” *Proceedings of the Indian Conference on Antennas and Propagation* (InCAP), Hyderabad, India, December 2018 [doi].

[30] D. Beetner, V. Khilkevich, A. M. Hassan, J. Hunter, Y. Liu, and D. Floyd, *“*Characterization of the Electromagnetic Coupling to UAVs,*”* *DE Systems Symposium*, September 24-27, 2018

[31] C. Hartshorn, K. Durbhakula, D. Welty, D. Chatterjee, J. Lancaster, A. M. Hassan, and A. N. Caruso, “Crosstalk and Coupling to Printed Circuit Board Metallic Traces with Arbitrary Shapes,” *Proceedings of the AMEREM 2018 Conference*, Santa Barbra, CA, Aug 27-31, 2018.

[32] M. Hamdalla, J. Roacho-Valles, J. Hunter, D. Beetner, A. M. Hassan, and A. N. Caruso, “Electromagnetic Analysis of Unmanned Aerial Vehicles Using Characteristic Mode Analysis,” *Proceedings of the AMEREM 2018 Conference*, Santa Barbra, CA, Aug 27-31, 2018.

[33] C. Hartshorn, M. Hamdalla, J. Lancaster, A. M. Hassan, and A. N. Caruso, “Electromagnetic Vulnerability of Wires with Arbitrary Shape,” *Proceedings of the AMEREM 2018 Conference*, Santa Barbra, CA, Aug 27-31, 2018.

[34] K. C. Durbhakula, D. Chatterjee, A. M. Hassan, and M. S. Kluskens, “Studies on Numerical Evaluation of Sommerfeld Integrals for Multilayer Topologies,” *IEEE Antennas and Propagation International Symposium and National Radio Science Meeting*, Boston, Mass., USA, July 7-12, 2018.

[35] J. Lancaster, D. Chatterjee, and A. N. Caruso, “Some Investigations into the Dispersion Characteristics of Localized Bessel Beams,” published in the *IEEE Antennas and Propagation International Symposium and National Radio Science Meeting*, Boston, Mass., USA, July 7-12, 2018 (1 page URSI Abstract).

[36] M. Hamdalla, A. M. Hassan, and A. N. Caruso “Characteristic Mode Analysis of Unmanned Aerial Vehicles with Realistic Shapes and Material Composition,” *IEEE International Symposium on Antennas and Propagation and USNC-URSI Radio Science Meeting,* Boston, MA, July 8-13, 2018.

[37] W. Azad, S. Roy, A. S. Imtiaz, and F. Khan, "Microelectromechanical System (MEMS) Resonator: A New Element in Power Converter Circuits Featuring Reduced

EMI," *2018 International Power Electronics Conference (IPEC-Niigata 2018-ECCE Asia)*, Niigata, May 20-24, 2018, pp. 2416-2420 [doi].

[38] J. Hunter, Y. Liu, D. Floyd, A. Hassan, V. Khilkevich, and D. Beetner, "Characterization of the Electromagnetic Coupling to UAVs," *Annual Directed Energy Science and Technology Symposium*, Feb 26-March 2, 2018.

11.4 Conference Presentations

11.4.1 *Submitted / Accepted*

[1] S. Bellinger, A. Caruso, A. Usenko, "Stacked Diodes for Pulsed Power Applications," GOMACTech-22, Miami, FL, March 21–24 2022 (submitted, oral).

[2] S. Bellinger, A. Caruso, A. Usenko, "New Paradigm on Making Semiconductor Opening Switches for Pulsed Power," 2021 23rd IEEE Pulsed Power Conference, Denver, CO, Dec. 12–16, 2021 (accepted, oral).

Directed Energy Professional Society, Directed Energy Systems Symposium, Washington DC, October 25-29 2021 (submitted):

[3] B. Barman, D. Chatterjee, A. Caruso, and K. Durbhakula, "Tradespace Analysis of a Phased Array of Microstrip Patch Electrically Small Antennas (ESAs)" (Poster)

[4] J. N. Berg, R. C. Allen, and S. Sobhansarbandi, "A Novel Method of Cooling a Semiconductor Device through a Jet Impingement Thermal Management System: CFD Modeling and Experimental Evaluation" (Poster)

[5] J. N. Berg, R. C. Allen, and S. Sobhansarbandi, "Heat Transfer Enhancement of a Jet Impingement Thermal Management System: A Comparison of Various Nanofluid Mixtures" (Poster)

[6] J. Bhamidipati, M. Paquette, R. Allen, and A. Caruso, "Photoconductive Semiconductor Switch Enabled Multi-Stage Optical Source Driver" (Poster)

[7] G. Bhattarai, J. Eifler, S. Roy, M. Hyde, J. Bhamidipati, A. Usenko, M. Pederson, M. Paquette, A. Caruso, S. Bellinger, L. Voss, and R. Allen, "All Solid-State High-Power Pulse Sharpeners" (Poster)

[8] S. Brasel, K. Norris, R. Allen, A. Caruso, and K. Durbhakula, "Efforts to Reduce Physical Aperture Area of Ultra-Wideband Arrays" (Poster)

[9] A Caruso, "ONR Short Pulse Research and Evaluation for c-sUAV: Supporting and Sub-Programs Overview" (Oral)

[10] J. Clark, R. C. Allen, and S. Sobhansarbandi, "Ultra-Compact Integrated Cooling System Development" (Poster)

[11] J. Eifler, S. Roy, M. Hyde, G. Bhattarai, J. Bhamidipati, A. Usenko, M. Pederson, M. Paquette, A. Caruso, S. Bellinger, L. Voss, and R. Allen, "TCAD Optimization of Epitaxially Grown Drift-Step Recovery Diodes and Pulser Performance" (Poster)

[12] N. Gardner, M. Paquette, and A. Caruso, "Diode-Based Nonlinear Transmission Lines Capable of GHz Frequency Generation at Single MW Peak Powers" (Poster)

[13] M. Hamdalla, A. Caruso, and A. Hassan, “The Shielding Effectiveness of UAV Frames to External RF Interference” (Poster)

[14] M. Hamdalla, A. Caruso, and A. Hassan, “A Predictive-Package for Electromagnetic Coupling to Nonlinear-Electronics using Equivalent-Circuits and Characteristic-Modes (PECNEC)” (Poster)

[15] M. Hyde, J. Eifler, S. Roy, G. Bhattarai, A. Usenko, M. Paquette, A. Caruso, S. Bellinger, L. Voss, and R. Allen, “Development of an Evaluation Network for Drift Step Recovered Diodes through and Augmented Design of Experiment” (Poster)

[16] S. Indharapu, A. Caruso, and K. Durbhakula, “Machine Learning Based Ultra-Wideband Antenna Array Optimization and Prediction” (Poster)

[17] F. Khan, W. Azad, and A. Caruso, “A Scalable Multilevel-Modular 10 kV Silicon Carbide MOSFET Architecture for Pulsed Power Applications” (Poser)

[18] D. F. Noor, J. Eifler, M. Hyde, G. Bhattarai, S. Roy, J. Bhamidipati, A. Usenko, M. Pederson, M. Paquette, A. Caruso, S. Bellinger, L. Voss, and R. Allen, “DSRD-IES Pulsed-Power Generator Topology Study Using Machine-Learning-Based Feature Selection Optimization and Predictive Learning” (Poster)

[19] S. Roy, J. Eifler, M. Hyde, G. Bhattarai, D. Noor, J. Bhamidipati, A. Usenko, M. Pederson, M. Paquette, A. Caruso, S. Bellinger, L. Voss, and R. Allen, “Systematic Topological Optimization of DSRD-Based IES Pulse Generator” (Poster)

[20] S. Shepard and A. Caruso, “Tubular Core Optical Power Amplifier” (Poster)

[21] H. Thompson, M. Paquette, and A. Caruso, “Minimizing On-State Resistance in GaN:X Photoconductive Semiconductor Switches (PCSSs) for Direct Modulation (Poster)

[22] A. Usenko, J. Eifler, S. Roy, G. Bhattarai, M. Hyde, M. Paquette, A. Caruso, S. Bellinger, L. Voss, and R. Allen, “New Paradigm in Fabrication of Semiconductor Opening Switches for Pulsed Power” (Poster)

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[23] S. Bellinger, A. Caruso, A. Usenko, “Stacked Diodes for Pulsed Power Applications: New Process Integration Scheme,” 240th Electrochemical Society Meeting, Orlando, FL, Oct. 10–14, 2021 (submitted, oral).

11.4.2 *Presented*

[24] W. Azad, S. Roy, and F. Khan, “A Four-State Capacitively Coupled High-Voltage Switch Powered by a Single Gate Driver,” *47th IEEE Conference on Plasma Science*, Singapore, December 6-10, 2020 (oral).

[25] J. Hunter, S. Xia, A. Harmon, A. Hassan, V. Khilkevich, and D. Beetner, “Simulation-Driven Statistical Characterization of Electromagnetic Coupling to UAVS,” *Annual Directed Energy Science and Technology Symposium*, March 2020 (abstract appeared, but talk cancelled due to pandemic).

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DEPS Posters and Presentations 2020

[26] William Spaeth, Wideband Parallel Plate to Coaxial Cable Taper

[27] Stefan Wagner, Quickly Determining Minimum HPC Source Requirements Using Binary Search

***

GOMAC 2019

[28] Cash Hauptmann, Reduced Recovery Time in SiPCSS Photoconductive Switches

[29] Eliot Myers, Picosecond High Power Switching Technologies

[30] Heather Thompson, GaN Optimization for Use in Photoconductive Switch

***

[28] B. Barman, D. Chatterjee, and A. N. Caruso, “Analytical Models for L-Probe fed Microstrip Antennas,” *Proceedings of the IEEE Antennas and Propagation International Symposium and National Radio Science Meeting*, Atlanta, Georgia, USA, July 7-12, 2019 (1 page URSI Abstract).

***

Directed Energy Professional Society (DEPS) Annual Science and Technology Symposium, Destin, Florida, USA, April 2019:

[29] Ryan Butler, Mechanical Challenges of Modular Photoconductive Semiconductor Based HPM Sources

[30] Steve Young, Two-Dimensional Optoelectronic Pulsed Power Switches: Initial Effort

[31] Adam Wagner, Rapid Cost Effective RF Component Prototyping Using 3D Printers

[32] Heather Thompson, Cost to benefit analysis of GaN for Photoconductive Semiconductor Switches

[33] Colby Landwehr, Low Leakage Electroluminescence For Improving SiPCSS Hold Off

[34] James Kovarik, Some Investigations Into Applications Of Electrically Small Antennas As Phased Array Elements

[35] Spencer Fry, Maximizing SiPCSS Efficiency For HPM Sources

[36] Deb Chatterjee, Studies On Antenna Characterization And Propagation Of High Power Pulsed Electromagnetic Waves With Minimal Dispersion

***

DEPS Posters and Presentations 2018

[37] Jeff Scully, ElectroLuminescence Studies of Silicon Based Photo-Switches

[38] Cash Hauptmann, Thermal Anlaysis of a PCSS through TCAD Simulation

[39] Nicholas Flippin, Fast Rise Time Switches: Drift Step Recovery Diode

***

DEPS Posters and Presentations 2017

[40] Noah Kramer, Recent Results of Silicon Based Photoconductive Solid State Switches for 500kHz Continuous Pulse Repetition Frequency

11.5 Theses and Dissertations

[1] Jordan N. Berg, “Development of a Jet Impingement Thermal Management System for a Semiconductor Device with the Implementation of Dielectric Nanofluids,” MS Thesis in Mechanical Engineering, University of Missouri-Kansas City, **2021** [mospace].

[2] James C. Kovarik, “Wideband High-Power Transmission Line Pulse Transformers,” MS Thesis in Electrical Engineering, **2021** [mospace].

[3] Wasekul Azad, “Development of Pulsed Power Sources Using Self-Sustaining Nonlinear Transmission Lines and High-Voltage Solid-State Switches,” PhD Dissertation in Electrical Engineering, **2021** [mospace].

[4] Paul Klappa, “Implementation and Assessment of State Estimation Algorithms in Simulation and Real-World Applications,” MS Thesis in Mechanical Engineering, **2021** [mospace].

11.6 IP Disclosures Filed

[1] S. Bellinger, A. Caruso, A. Usenko, US Provisional Patent Application “Stacked Diode with Side Passivation and Method of Making the Same,” 12AUG2021.

[2] S. Bellinger, A. Caruso, A. Usenko, “Diode and Method of Making the Same,” 28JUNE2021.

[3] Bhamidipati, Myers, Caruso, “Multi-Stage Photo-Stimulated WBG-PCSS Driven RF Pulse Generation System Implementing Miniature Optical Sources,” 21UMK009, 04NOV2020.

[4] Shepard, “A Low Noise Optical Amplifier,” 21UMK007, 14SEPT2020.

[5] Shepard, “A Novel Optical Fiber Amplifier,” 20UMK012, 02JUN2020.

[6] Doynov, “High-power High Repetition Rate Microwaves Generation with Differentially Driven Antenna,” 20UMK011, 19APR2020.

[7] Doynov, “Scalable Modular System for High-power Microwaves Generation,” 20UMK010, 19APR2020.

[8] Doynov, “Pulse Differential High-power Microwave Generation,” 19UMK007, 02JAN2019.

[9] Doynov, “Non-linear Network Topologies with Reutilized DC and Low-frequency Signal,” 19UMK008, 28DEC2018.

[10] Doynov, Caruso, “Non-Linear Transmission Line Topologies for Improved Output,” 19UMK005, 28SEPT2018

11.7 Provisional Patents Filed

[1] S. Bellinger, A. Caruso, A. Usenko, US Provisional Patent Application “Stacked Diode with Side Passivation and Method of Making the Same,” filed 09/10/2021.

[2] S. Bellinger, A. Caruso, A. Usenko, “Diode and Method of Making the Same” US Provisional Patent Application 63/216,550, filed June 30, 2021.

[3] P. Doynov, A. Caruso, “High-Efficiency High-Power Microwave Generation using Multipass Non-Linear Network Topologies,” filed 26NOV2019.

[4] Plamen Doynov, James Prager, Tim Ziemba, Anthony N. Caruso, “Non-Linear Transmission Line Topologies for Improved Output”, USPTO Provisional Serial No. 62/737,185, filed 27SEPT2018.

11.8 Non-Provisional Patents Filed

None to date

ONR HPM Program – Monthly Status Report (MSR) – May 2022

Anthony Caruso – Univ. Missouri – Kansas City

N00014-17-1-3016 [OSPRES Grant]

ONR Short Pulse Research, Evaluation and non-SWaP Demonstration for C-sUAS Study

15 JUNE 2022

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OSPRES Grant Objective: to execute high-risk, high-payoff efforts that mitigate, fill or rectify one or more grand-challenge or elementary gaps or deficiencies needed to achieve a modular, scalable and electronically steerable high-power microwave (HPM) based defense system for the counter unmanned aerial system (cUAS) mission. The OSPRES HPM system and sub-system development/evaluation efforts are focused on the short-pulse high-average-power space and includes the kill chain considerations including the target and its responsivity to radiofrequency stimuli.

OSPRES Metrics of Success: developed technologies and capabilities that are published in the peer review, protected as intellectual property, and/or, transitioned to the OSPRES Contract effort and beyond for integration with other DoD needs or dual-commercial-use, as enabling/integrable capability(ies).

OSPRES Grant Approach: A fail-fast philosophy is maintained, where if a technology or capability is deemed infeasible to be demonstrated or validated during the project period-of-performance, it shall be culled, results to date and basis of infeasibility documented, and the next major gap/deficiency area addressed by that part of the project sub-team. Students whose thesis depends on following through with a full answer during the life of the award will be given special dispensation to continue their work.

OSPRES Grant Security: All efforts should be fundamental and publicly releasable in nature when taken individually. This report has been reviewed for operational security, compilation, proprietary and pre-decisional information concerns.

1 Contents

2 Executive Summary

2.1 Progress, Significant Findings, and Impact

Fiber Laser and Optical Amplifiers. We cleaved the length of our dual-core Yb doped fiber down to the proper length of 2 [m] for our pre-amp design. The cleave must have left a sufficiently flat surface at the break in the fiber since no reflections were seen in the output pulse shape. We did however notice some gain fluctuations—traced down to a pump laser diode instability. We intend to solve this problem via the use of alternate pump input ports at the power combiner.

We developed an optical transmission design tool and applied it to our power combiner and passive power delivery design tasks. We show that the mechanical flexibility of fiber (in contrast to a rigid tube) comes with a high price in bandwidth and loss, e.g., if we wanted to guarantee over 90% transmission, then a commercially available photonic crystal fiber cannot exceed about 2 [m] in length and the spectral bandwidth is limited to roughly 80 nm—a far cry below the 300 nm of bandwidth that a water-filled tube could provide at that same length.

In our multiple tube combiner and amplifier designs we find that the tube-to-tube mode coupling is predominantly driven by the nonlinear effect of self-focusing (within the glass walls). This nonlinear mode coupling is enhanced by an order of magnitude when we reduce the thickness of the glass walls from 2 microns to a wall thickness of 0.5 micron.

DSRD Optimization Simulations. For drift-step-recovery diode (DSRD) based pulser systems, achieving >10 kV power module peak load voltage while maintaining low risetimes (via voltage riserates experimentally seen at ~6 $\times 10^{11}$ V/s for single 7-stacks) is crucial for increasing peak power capabilities of large systems (~1 GW). Circuit simulations (SPICE software) are used to optimize capacitive and inductive components within the power modules of the DSRD-based pulser designs for peak load voltage but rely on accurate SPICE DSRD models. To improve upon the DSRD CMC SmartSpice diode model already developed for DSRD-based pulser simulations, a sectioned forward IV fitting has been developed in the Verilog-A code to very closely match the non-standard experimental forward IV seen for EG series DSRD, with forward IV and pulser simulations next to test the convergence of the sectionally fitted forward IV.

DSRD Processing and Manufacturing. Both Gen2 and Gen3 wafer lots continue with processing. The Gen2 samples have been processed at the wafer level, cut into single dies, and are currently at the saw damage etching step. Our attempt to use parylene as a mask for the etching failed, and we are currently trying various mask materials to complete this process step. If not successful, we will switch from HNA (hydrofluoric/nitric/acetic) wet etch chemistry to XeF_2 gas etch, as this does not require masking of metal-coated front and back wafer surfaces. With regard to process step development, we have measured wafer surface roughness after the anisotropic wet etch. The AFM data shows that our new etch recipe – TMAH (tetramethylammonium hydroxide) with added DMSO (dimethyl sulfoxide) results in surface polishing, while standard TMAH results in surface roughening. This demonstrates the advantage of our etch recipe over the standard one.

DSRD Design of Experiments. Diode forward IV testing was modified with regard to test fixture used, cabling, and measurement techniques. Breakdown testing in the Tektronik 371 semiconductor analyzer has been performed, showing ~40% of diodes hold at least 500 V (at 1 mA) per diode in stack. Impedance analysis has also shown the CV fixture to have high series resistance, and the forward IV test fixture will be evaluated in the impedance analyzer to help determine a more accurate DSRD series resistance. Forward IV measurements have become more consistent and have lower added series resistance, but the secondary factors still do not allow for a single accurate forward IV measurement to be taken. Variability in CV measurements will also be evaluated. Accurate diode testing data improves SPICE device modeling and allows for analysis of the design of experiments for relationships between doping profile, device manufacture, standard diode testing (IV, CV, RRT), and DSRD pulser performance.

DSRD-Based Pulsed Power Source Optimization. We have started developing the theory for a multi-stage DSRD pulser to increase the output voltage to ≥ 20 kV by stacking 1x1 pulsers in series. The design principle of such stacking is that the output pulse of the first stage is applied to reverse bias the second stage pulser, increasing the reverse pumping current and decreasing the DSRD snap-OFF time significantly, which ultimately results in very high voltage pulses. Preliminary circuit analysis shows, however, that such a stacked pulser could still be limited in performance due to the current and voltage limitations in the state-of-the-art MOSFETs currently available.

Dynamically Tunable Multi-Frequency Solid-State Frozen Wave Generator (FWG). A final summary report has been provided for this project in the Appendix.

Pulse-Compression-Based Signal Amplification. We have determined that a magnetic switch, which is the fundamental component of the magnetic pulse compression circuit, cannot be realized at frequencies higher than 300 MHz due to material limitations. A statement of work (SoW) has been drafted with KRI in order to develop high-frequency saturable inductor materials over 500 MHz. A B-H curve tracer circuit has been completed with the high voltage section isolated in an enclosure. Measurements and analysis are ongoing to verify accurate circuit operation.

Antennas. Manufacturing of a small, wideband (0.7–1.1 GHz), microstrip patch antenna, fed by a tapered coaxial connector, is ongoing. The prototyping went through a series of challenges, most of which have been addressed, and is expected to be completed in a week. A successful testing of the antenna parameters will be followed by manufacturing of the 4×4 array for final demonstration.

A new dielectric graded impedance transformer has been designed and simulated to replace the traditional impedance transformer to alleviate the reflections (> –10 dB) seen at the input port of the Koshelev antenna. The new transformer design yielded improved S_{11} and S_{21} values when compared to the previous design, especially in the frequencies above 3 GHz and up to 5 GHz. The new transformer overcomes the field discontinuity problem at the transformer–antenna interface and satisfies impedance matching and field matching at the interface.

The machine learning (ML) tool for tradespace study of antenna arrays has been upgraded to provide the users with the option to define antenna design parameters required for training the ML algorithm, prediction, and tradespace analysis. The ML tool has also been tested on a different antenna design (rectangular horn antenna with dielectric loading) from the fractal antenna and was asked to predict reflection coefficient and gain metrics for a new set of design parameter values different from the training data. The tool was able to predict the S_{11} and gain response of the rectangular horn antenna with dielectric loading with RMSE values less than 2.

2.2 Completed, Ongoing, and Cancelled Sub-Efforts

2.2.1 *Ongoing Sub-Efforts*

	Start	End
GaN:C Modeling and Optimization	OCT 2017	Present
Diode-Based Non-Linear Transmission Lines	FEB 2018	Present
Trade Space Analysis of Microstrip Patch Arrays	FEB 2019	Present
Lasers and Optics	FEB 2020	Present
UWB Antenna Element Tradespace for Arrays	MAY 2020	Present
Si-PCSS Contact and Cooling Optimization	JAN 2021	Present
Drift-Step Recovery Diode Optimization Simulations	JAN 2021	Present
DSRD-Based IES Pulse Generator Development	APR 2021	Present
Drift-Step Recovery Diode Manufacturing	MAY 2021	Present
DSRD Characterization through Design of Experiments	MAY 2021	Present
Sub-Nanosecond Megawatt Pulse Shaper Alternatives	MAY 2021	Present
Ultra-Compact Integrated Cooling System Development	MAY 2021	Present
Continuous Wave Diode-NLTL Based Comb Generator	SEPT 2021	Present
Pulse-Compression-Based Signal Amplification	DEC 2021	Present

2.2.2 *Completed/Transferred Sub-Efforts*

Adaptive Design-of-Experiments	OCT 2017	APR 2019
Non-perturbing UAV Diagnostics	OCT 2017	OCT 2018
Noise Injection as HPM Surrogate	OCT 2017	MAR 2019
SiC:N,V Properties (w/ LLNL)	APR 2018	MAR 2019
Helical Antennas and the Fidelity Factor	JUL 2018	SEPT 2019
Si-PCSS Top Contact Optimization	APR 2020	OCT 2020
Nanofluid Heat Transfer Fluid	NOV 2020	JUL 2021
HV Switch Pulsed Chargers	DEC 2018	DEC 2021
Enclosure Effects on RF Coupling	OCT2019	DEC 2021
UAS Engagement M&S	MAR 2021	DEC 2021
GaN-Based Power Amplifier RF Source	AUG 2021	DEC 2021

2.2.3 *Cancelled/Suspended Sub-Efforts*

Ab Initio Informed TCAD	OCT 2017	OCT 2020
Positive Feedback Non-Linear Transmission Line	NOV 2017	DEC 2018
Minimally Dispersive Waves	FEB 2018	SEPT 2018
Multiferroic-Non-linear Transmission Line	NOV 2018	APR 2019
Avalanche-based PCSS	SEPT 2018	SEPT 2019
Gyromagnetic-NLTL	DEC 2017	NOV 2020
Multi-Stage BPFTL	APR 2020	JUL 2020
Heat Transfer by Jet Impingement	MAY 2018	FEB 2021
Si, SiC, and GaN Modeling and Optimization	NOV 2018	FEB 2021
Bistable Operation of GaN	FEB 2021	MAR 2021
WBG-PCSS Enabled Laser Diode Array Driver	NOV 2020	JAN 2022

2.3 Running Total of Academic and IP Program Output

See Appendix for authors, titles and inventors (this list is continuously being updated)

Students Graduated	*6 BS, 9 MS, 4 PhD*
Journal Publications	*6 (6 submitted/under revision)*
Conference Publications	*35 (3 submitted/accepted)*
External Presentations/Briefings	*40*
Theses and Dissertations	*5*
IP Disclosures Filed	*10*
Provisional Patents Filed	*4*
Non-Provisional Patents Filed	*0*

3 Laser Development

3.1 Fiber Lasers and Optical Amplifiers

(Scott Shepard)

3.1.1 *Problem Statement, Approach, and Context*

Primary Problem: High-average-power 1064-nm picosecond lasers are too large (over 1100 cm^3/W) and too expensive (over \$1000/μJ per pulse) for PCSS (photoconductive semiconductor switch) embodiments of HPM-based defense systems. For example, a laser of this class might occupy a volume of 1 m x 30 cm x 30 cm = 90,000 cm^3 and provide an average power of 50 W (thus, 1800 cm^3/W). Costs in this class range from \$100K to \$300K to drive our Si-PCSS applications.

Solution Space: Optically pumped ytterbium-doped optical fiber amplifiers, fed by a low-power stable seed laser diode, can offer a cost-effective, low-weight, and small-volume solution (with respect to traditional fiber and traditional free-space laser designs). Moreover, our novel optical amplifier tubes, might operate at far higher power levels (over 1000 times greater), thus driving an entire array of PCSS with a single amplifier and thereby reducing the overall system costs and eliminating the optical pulse-to-pulse jitter constraints.

Sub-Problem (1): Optical pump power system costs account for over 50% of the budget for each laser (in this class, for normal/free-space, optical fiber, and tubular embodiments).

Sub-Problem (2): Fiber (as well as power tube) optical amplifier performance is degraded primarily by amplified spontaneous emission (ASE) noise, which limits the operating power point, and by nonlinearities, which distort the optical pulse shapes.

State-of-the-Art (SOTA): Free-space NdYAG lasers or Ytterbium-doped fiber amplifiers optimized for LIDAR, cutting, and other applications.

Deficiency in the SOTA: Optical pump power system costs (in either free-space or fiber lasers) are prohibitive for the PCSS applications until reduced by a factor of at least two.

Solution Proposed: Fiber lasers permit a pre-burst optical pumping technique (wherein we pump at a lower level over a longer time) which can reduce pumping costs by a factor of at least ten. To address the ASE and nonlinear impairments, we are pursuing the use of gain saturation and a staged design of different fiber diameters. We also apply these techniques to fiber amplifiers which incorporate our power amplifier tube in the final stage. The inclusion of our novel tubular-core power amplifier stage should permit a single laser to trigger an array of several PCSS (reducing system cost and mitigating timing jitter).

Relevance to OSPRES Grant Objective: The enhancement in SWaP-C^2 for the laser system enables PCSS systems for viable deployment via: a factor of 40 in pumping cost reduction of each laser; and a factor of *N* in system cost reductions as a single laser could drive *N* (at least 12) PCSS in an array, while also eliminating the optical jitter constraints.

Risks, Payoffs, and Challenges: Optically pumping outside the laser pulse burst time can enhance the ASE; pump costs could be reduced by 40, but ASE in the presence of dispersion and/or nonlinearities could enhance timing jitter thereby limiting steerability. The main challenge for power tube implementation is the entrance optics design.

3.1.2 *Tasks and Milestones / Timeline / Status*

(A) Devise a pre-burst optical pumping scheme by which we can reduce the costs of the laser by a factor of two or more and calculate the resulting increase in ASE. / FEB–JUL 2020 / Completed.

(B) Reduce the ASE via gain saturation. / Oct 2020 / Completed.

(C) Design saturable gain devices which avoid nonlinear damage. / Ongoing.

(D) Calculate and ensure that timing jitter remains less than +/-15 ps with a probability greater than 0.9. / Ongoing.

(E) Demonstrate a cost-reduced fiber laser: the level of success to be quantified via the amount of ASE growth per duration of a pre-burst pumping interval. Growth of 100 uw over 6 ms (the limit in theory) would be considered outstanding. / August 2022.

(E1) March 2021 Finalize design. / Completed.
(E2) April 2021 Assemble and test-check seed LD (laser diode)/driver. / Completed.
(E3) April 2021 Measure power vs current transfer function of seed LD/driver. / Completed.
(E4) May–July 2021 Measure ASE and jitter of 1064 nm seed LD/driver. / Completed.
(E5) May–July 2021 Measure ASE and jitter of 1030 nm seed LD/driver. / Completed.
(E6) June–July 2021 Assemble and test-check pump LDs/drivers. / Completed.
(E7) June–July 2021 Measure power vs current transfer function of pump LDs/drivers. / Completed.
(E8) July–September 2021 Splice power combiners to Yb doped preamp fiber. /Completed.
(E9) July–September 2021 Connect seed and pumps to power combiners and test-check. / Completed.
(E10) September–October 2021 Measure gain, ASE and jitter of 1064 nm preamp assembly (forward, backward and bidirectional pumping) as a function of pump power and duty cycle. / Partially completed before task eliminated.
(E11) September–October 2021 Measure gain, ASE and jitter of 1030 nm preamp assembly (forward, backward and bidirectional pumping) as a function of pump power and duty cycle. / Partially completed before task eliminated.
(E12) November 2021 Splice power amplifier and its power combiner to best preamp. / Partially completed before task eliminated.
(E13) May–August 2022 Measure gain, ASE and jitter of entire amp assembly. / Ongoing.
(E14) May–August 2022 Analyze data and document. / Ongoing.

(F) Design a new type of higher power, tubular core fiber amplifier. / May–August 2022.

(F1) Apply one high-power tubular amplifier to a system comprised of an array of several (say N) PCSS. For example: N=12 in a 3x4 array (or 4x4 array with corners omitted) N=16 in a 4x4 array, etc.; thereby eliminating jitter constraints and reducing laser system cost by more than a factor of 100 (independent of burst profile). / August 2022.

(F2) Design a high power, multiple tube optical amplifier and determine if it permits advantages for power handling or beam profile. / August 2022 / Initiated.

(G1) Design a beam shaping, optical power combiner using a cladding of 6 tubes. / June 2022 / Initiated.

(G1.1) Develop COMSOL models. / April 2022 / Completed.

(G1.2) Discover and optimize the length at which the cladding modes couple maximal power into the core mode (of the entire waveguide). / June 2022 / Ongoing.

(G2) Design a beam shaping, optical power combiner using a cladding of 6 tubes surrounding one inner tube. / July 2022 / Initiated.

(G2.1) Develop COMSOL models. / April 2022 / Completed.

(G2.2) Discover and optimize the length at which the cladding modes couple maximal power into the inner tube. / July 2022 / Ongoing.

(G3) Develop spectral combiners based on multiple-tube waveguides and compare to existing PCF (photonic crystal fiber) technologies. / August 2022 / Partially completed.

3.1.3 *Progress Made Since Last Report*

(E13) We reduced the length of our dual-core Yb doped fiber (which is fused to the output of our power combiner) to the proper length of 2 [m] for our pre-amp design. The cleave led to a decent signal pulse shape at the output, so it must have left a sufficiently flat surface at the break in the fiber (otherwise reflections would distort the pulse shape). We did however notice some gain fluctuations and identified that these stem from a pump laser diode instability. We intend to solve this problem via the use of alternate pump input ports at the power combiner; and/or via the use of an alternate pump laser current driver.

(F1) (G3) The spectral filtering properties of waveguides, needed for both the spectral power combiner task and the task of designing passive power delivery fibers, depend on the length of such waveguides which for our purposes range from 1 to 10 meters. For commercial fiber the data sheets typically provide the loss (in dB/km) vs wavelength. In cases where we only know the refractive index of the material (e.g., our water filled glass tubes) another step is involved, as described in 3.1.4.

We find that water filled tubes provide a far greater spectral bandwidth than commercial fiber (e.g., telecom. grade SPF-28; or photonic crystal fiber, PCF) at any of these lengths. If the mechanical flexibility of fiber is desired for the power delivery task, then PCF (designed for 850 nm) has far less loss than SPF-28. Quantified comparison is in 3.1.4.

(G1) (G2) We refined our COMSOL models for a 6-tube design and a 7-tube design of an optical power combiner, so that we can readily vary the thickness of the walls of the tubes. We find that our tube-to-tube mode coupling is predominantly driven by the nonlinear effect of self-focusing (within the glass walls). This nonlinear mode coupling is enhanced by reducing the thickness of the glass walls (which also enhances the amount of linear mode coupling, to a lesser extent).

3.1.4 *Technical Results*

(E13) We reduced the length of our dual-core Yb doped fiber (which is fused to the output of our power combiner) to the proper length of 2 [m] for our pre-amp design. The cleave led to a decent signal pulse shape at the output, as shown on the left in Fig. 3.1.1, so the cleave must have left a sufficiently flat surface at the break in the fiber (otherwise reflections would distort the pulse shape). The pulses on the right in Fig. 3.1.1, however, indicate some gain fluctuations since these were captured in a scope trace just a few seconds later. The traces varied between examples of this type on the time scale of a few seconds. It was identified that these gain fluctuations stem from a pump laser diode instability (which was seen to vary on the same time scale). We intend to solve this problem via the use of alternate pump input ports at the power combiner and/or via the use of an alternate pump laser current driver (as well as simply ensuring thermal equilibrium by allowing the entire system to maintain a single operating point for an hour or more).

Fig. 3.1.1. Sample of scope traces demonstrating good pulse shape on the left and gain fluctuations on the right.

(F1) (G3) The spectral filtering properties of waveguides, needed for both the spectral power combiner task and the task of designing passive power delivery fibers, depend on the length of such waveguides, which for our purposes range from 1 to 10 meters. For commercial fiber the data sheets typically provide the loss (in dB/km) vs wavelength. In cases where we only know the refractive index of the material (e.g., our water filled glass tubes) another step is involved. Wave propagation follows e^{jkz}, where $k = 2\pi/\lambda$ is the wavevector component in the direction of propagation, z; so the imaginary part of the refractive index gives rise to attenuation: $e^{jkz} = e^{-\alpha z} = 10^{-\alpha_{dB} z/10}$. Since $\lambda = \lambda_0/n_i$ we

obtain the conversion formula: $\alpha_{dB} = 10\,[\log_{10}(e)]\,n_i(2\,\pi)/\lambda_0$, where λ_0 is the free-space wavelength.

Water has a good transmission window near 920nm, where the responsivity of silicon peaks. This is fortuitous since silicon is a popular PCSS material and because it makes a good choice when targeting semiconductors in Directed Energy attacks. Thus, water is a natural material to investigate for both our HPM (passive power delivery) and HEL (power combiner) applications. Water is highly absorptive in the IR, with a dramatic four orders of magnitude increase in n_i when we increase the wavelength from 920nm to 1125nm. Since our conversion formula shows that the absorption coefficient *in dB* is linear in n_i we compress the scale further by plotting $\log_e(\alpha_{dB})$ in Fig. 3.1.2 (instead of α_{dB}) as a function of wavelength.

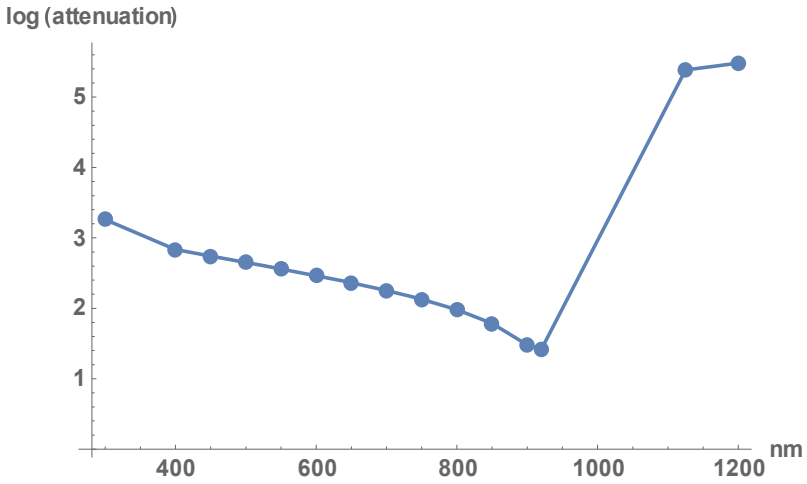

Fig. 3.1.2. Logarithm of the attenuation coefficient, α_{dB} in [dB/km] for water, versus λ_0.

For our purposes this information is more usefully conveyed in Fig. 3.1.3 where the y-axis is the waveguide length, *z*, in [m] and the contour plot shows the optical transmission for contour height of 90% at red to orange, down in steps of 10%, to the contour height of 10% at blue to purple. Such plots are useful design tools. For example, if we wanted to guarantee over 90% transmission in a 2 [m] power combiner we would limit the spectral range be within roughly 650 to 950 nm. This also illustrates how waveguide can function as a filter of a shape which evolves with the distance of the guide.

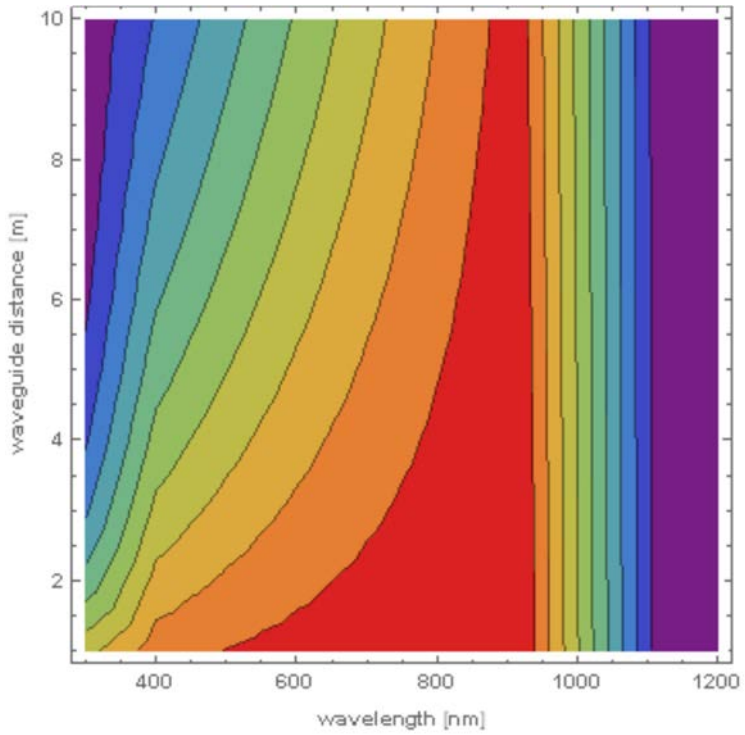

Fig. 3.1.3. Contour plot of transmission in water, as a function of distance down the waveguide and λ_0 (with red above 90% and purple below 10%, in steps of 10%).

In contrast to the extremely broadband low-loss transmission window in water-filled glass tubes we find that mechanically flexible fiber is relatively narrowband. One commercially available PCF, designed for minimal loss at 850nm, has an attenuation profile presented in Fig. 3.1.4 (where again we compress the scale by plotting $\log_e(\alpha_{dB})$ instead of α_{dB}).

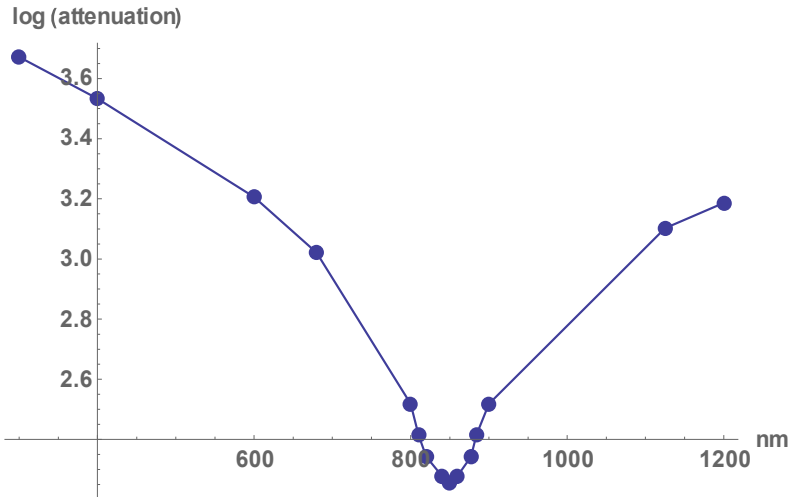

Fig. 3.1.4. Logarithm of the attenuation coefficient, α_{dB} in [dB/km] for a PCF, versus λ_0.

The corresponding contour plot in Fig. 3.1.5 shows the optical transmission for contour height of 90% at red to orange, down in steps of 10%, to the contour height of 10% at blue to purple. We find that the mechanical flexibility of fiber (in contrast to a rigid tube) comes with a high price in bandwidth and loss, e.g., if we wanted to guarantee over 90% transmission then the PCF cannot exceed about 2 [m] in length and the spectral bandwidth is limited to roughly 80nm – a far cry below the 300nm of bandwidth that a water-filled tube could provide at that same length.

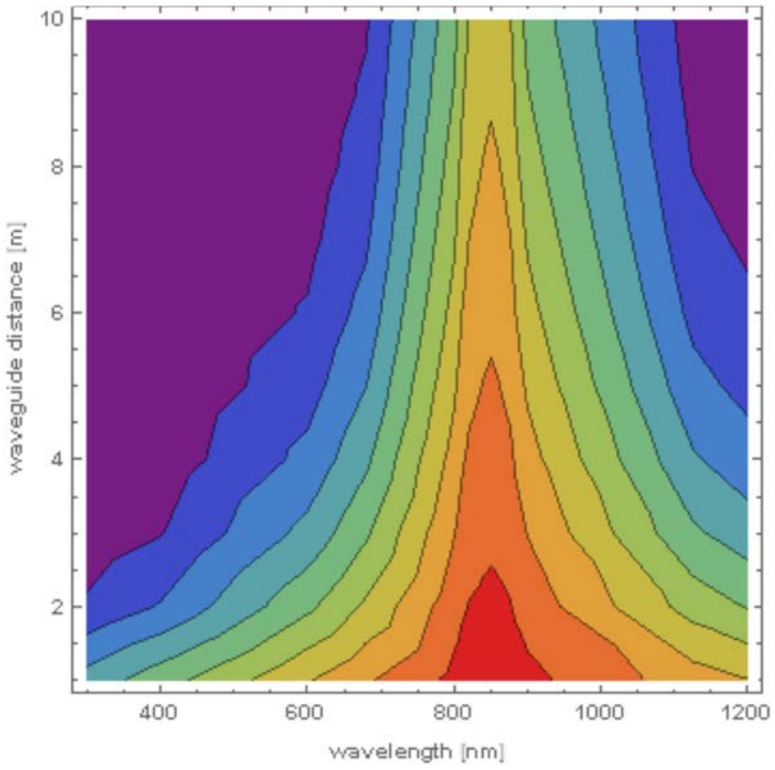

Fig. 3.1.5. Contour plot of transmission in a PCF, as a function of distance down the waveguide and λ_0 (with red above 90% and purple below 10%, in steps of 10%).

(G1) (G2) We refined our COMSOL models for a 6-tube design and a 7-tube design of an optical power combiner, so that we can readily vary the thickness of the walls of the tubes (without affecting the inner diameter of the tubes, or the fact that their walls are in contact with each other. We asses the mode coupling between tubes herein by launching a uniform electric field over the air-core and glass-cladding of the top tube (labeled port 5) and examine how much power is transferred into the air-core of an adjacent tube (labeled port 7). At a wavelength of 1 micron and a wall thickness, t = 2 microns, Fig. 3.1.6 presents the resulting power transfer curve, where the straight line represents the linear ($\gamma = 0$) response. We note that at an input power of 1GW the linear power transfer would be 2kW but the nonlinear response increases this to 50kW. At very high power the nonlinearity reduces the mode coupling and at very low power the nonlinear response follows the linear curve.

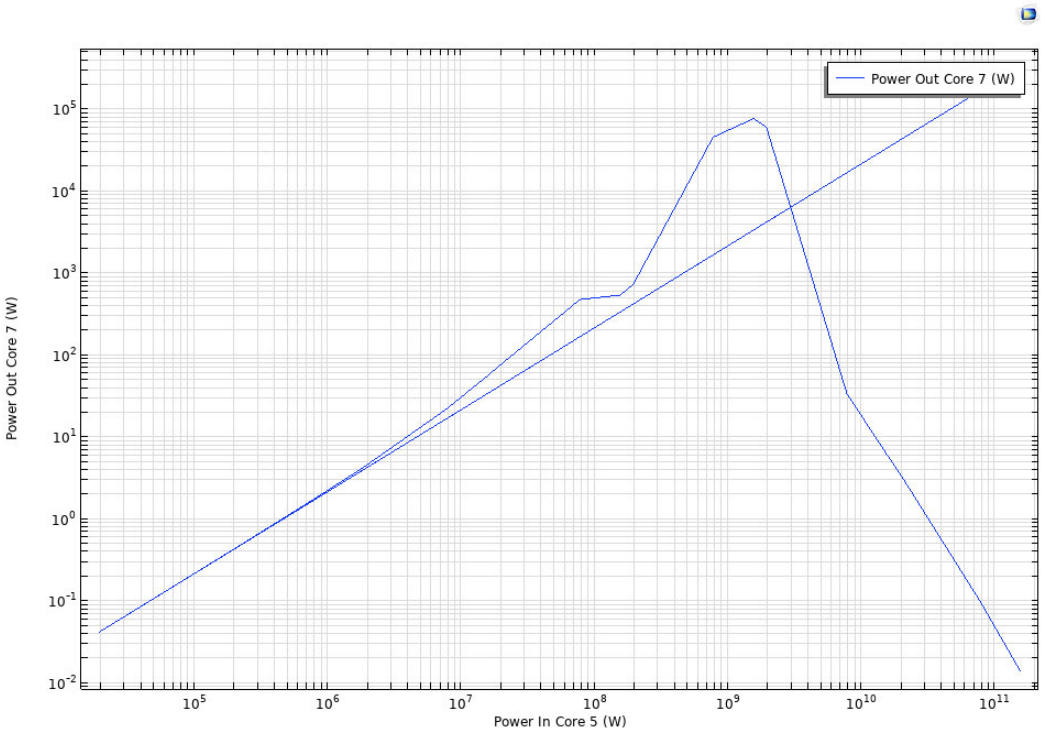

Fig. 3.1.6. Power transfer curves of one tube (port 5) into an adjacent tube (port 7) for a glass wall thickness, t = 2 microns (at λ_0= 1 micron).

Thus, the tube-to-tube mode coupling is predominantly driven by the nonlinear effect of self-focusing (within the glass walls). This nonlinear mode coupling is enhanced by reducing the thickness of the glass walls as exemplified in Fig. 3.1.7 in which (again at a wavelength of 1 micron) we reduce the wall thickness to t = 0.5 microns. This results in a maximal power transfer closer to 1MW for a broader range of input powers (the amount of linear mode coupling is also enhanced, to a lesser extent).

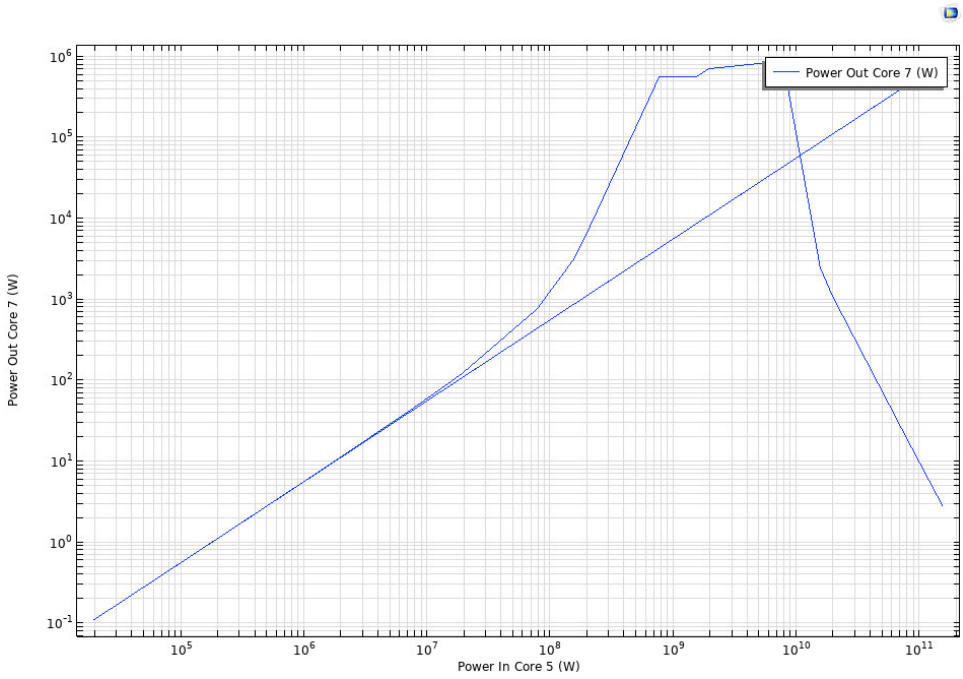

Fig. 3.1.7. Power transfer curves of one tube (port 5) into an adjacent tube (port 7) for a glass wall thickness, t = 0.5 microns (at λ_0= 1 micron).

We also explore the frequency dependence of the mode coupling and find that it exhibits resonances at various wavelengths, λ_0, in the nonlinear case (although the linear power transfer was seen to increase monotonically with λ_0). Fig. 3.1.8 summarizes our findings for an input power of 2GW with t = 2 microns; and at t = 0.5 microns a similar dependence was found, as shown in Fig. 3.1.9.

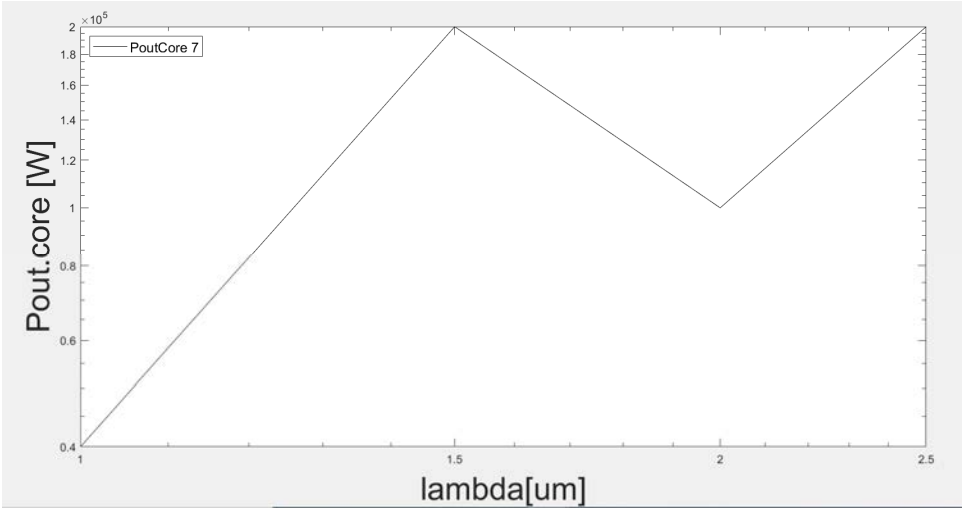

Fig. 3.1.8. Spectral dependence of the nonlinear power transfer of one tube into an adjacent tube for a glass wall thickness, t = 2 microns (at an input power = 2GW).

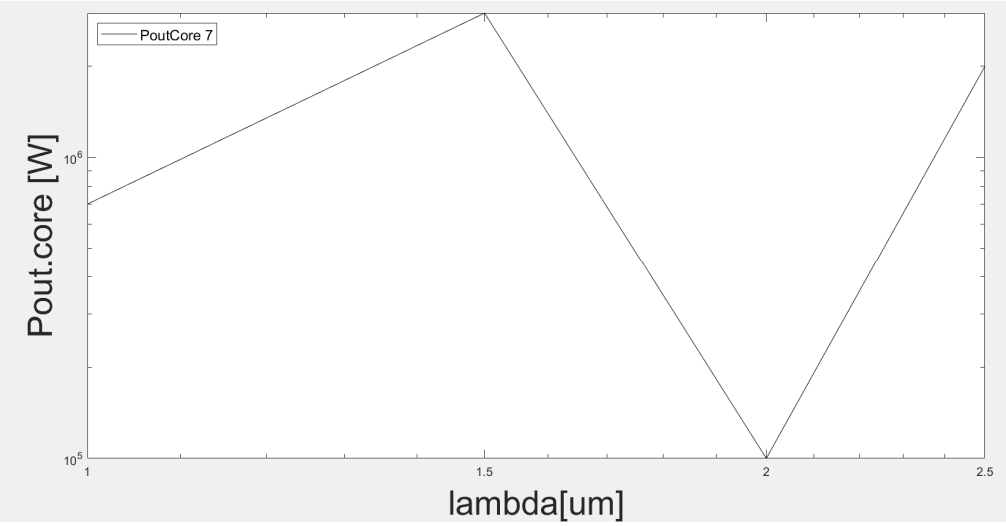

Fig. 3.1.9. Spectral dependence of the nonlinear power transfer of one tube into an adjacent tube for a glass wall thickness, t = 0.5 microns (at an input power = 2GW).

3.1.5 *Summary of Significant Findings and Mission Impact*

(A) Our pre-burst optical pumping scheme simulations showed that we can drop the pump power costs by a factor of 40 with pre-burst ASE power levels below the heating level tolerance of 100 μW. UMKC invention disclosure filed 02JUN2020.

(B) For a proposed system gain of 8 million, a linear gain theory predicted the in-burst ASE would be over our heating level spec. by a factor of 3960, but by exploiting the nonlinearity of gain saturation we find that we can suppress the ASE by over 7000. UMKC invention disclosure filed 14SEP2020.

(C) Achieved initial practical device designs that exploit gain saturation, which remained below damage thresholds, via staged designs of different mode diameters NOV2020.

(D) Models of the impact of ASE on timing jitter in the presence of dispersion and/or nonlinearities were established JUL2020.

(E) The design of a proof-of-concept experiment demonstrating a cost-reduced optical pumping scheme was finalized MAR2021.

(F) We made (to our knowledge) the first observation of self-focusing effects that are not determined by beam power alone. We found instead that these can also be controlled via the geometric factors within a waveguide (such as fiber core diameter) MAY2021.

We additionally made (to our knowledge) the first observation that a mode exists in the air within a simple glass tube into which we can couple energy from the mode in the glass. Thus, an amplifier (in the doped and pumped glass) can operate at higher powers JUNE2021.

We found conditions under which 0.25 GW of power can exist in the tube’s air-core mode when its glass-cladding mode is at a power level near 0.5 GW JULY2021.

Advancements in the very high-power operating point (tens of GW) of our tubular optical amplifier (and the existence, size and spatial uniformity of its air-core mode) were shown to permit a single laser to trigger an array of several (up to 100) Si-PCSS – reducing the laser system cost and eliminating the optical timing jitter constraint. The symmetry breaking of the scattering from self-focusing in a curved waveguide was shown to enable such AUG2021.

4 Photoconductive Switch Innovation

4.1 Characterizing and Optimizing On-State Resistance in GaN:X PCSS

(Heather Thompson)

4.1.1 *Problem Statement, Approach, and Context*

***Primary Problem*:** Traditionally, RF generation using photoconductive semiconductor switches (PCSS) relies on materials such as silicon (Si) or gallium arsenide (GaAs), due to their availability and low cost; however, as these applications begin to require higher operating frequencies, powers, and temperatures, with the same or reduced system form-factor, the theoretical operating limits of these materials are being reached.

***Solution Space*:** By exploiting the 3.4 eV bandgap, 1000 cm^2/Vs electron mobility, and thermal properties of GaN, it is possible to realize pulsed-power applications requiring up to a 5 MV/cm critical field, high-frequency operation, and ~400 °C operating temperature, respectively.

Sub-Problem: One of the most important problems in minimizing conduction losses, maximizing efficiency, and reducing thermal issues in compensated, semi-insulating GaN:X (i.e., GaN:X with X=C, Fe…) PCSS-based systems is achieving <1 Ω on-state resistance by optimizing the modifiable parameters of GaN:X at the material, device, and system levels, while still maintaining quick switch turn-off time and low turn-off losses.

***State-of-the-Art (SOTA*):** PCSS-based RF generation systems using Si, SiC, or GaAs can achieve MW-range output power, ones-of-gigawatts frequency content, and electrical efficiency of ~60% that require increased laser energies and device size to reach maximum efficiency and necessary operating power limits, respectively.

***Deficiency in the SOTA*:** Si-, SiC-, and GaAs-based PCSS require ones-of-mJ of incident laser energy to achieve <1 Ω on-state resistance, leading to increased incident laser requirements, increased heating in devices, and devices that are ones-of-cm^2 in area for the necessary peak power and operating temperatures.

***Solution Proposed*:** Use simulation and available experimental results, from the literature and collected results at UMKC, to optimize the variable parameters of GaN:X PCSS to achieve <1 Ω on-state resistance with increased electrical and optical efficiency while maintaining a quick switch turn-off time and low turn-off losses.

Risks, Payoffs, and Challenges:

***Challenges*:** The high cost of material leads to a limited number of devices available for experimental testing and analysis, requiring a majority of the optimization studies to be performed using simulation software (COMSOL and TCAD).

***Risks*:** Simulation results may differ from experimental results for certain PCSS parameters due to particular photogeneration and recombination parameters not being included in models along with non-ideal, real-world experiments requiring additions such as encapsulation material or other changes not fully addressed in simulation.

***Payoffs*:** By minimizing the conduction losses in GaN PCSS, a compact, tunable RF source can be realized with increased efficiency and SWAP-C^2 capabilities.

4.1.2 Tasks and Milestones / Timeline / Status

(A) Milestone – Determine material, device, and system parameters that affect on-state resistance and which of these can be best leveraged to reduce on-state losses and heating.

1. Task – Literature study of photoelectric on-state resistance to understand how this parameter can be optimized to reduce conduction and on-state losses during PCSS operation *[ongoing].*
2. Task – Literature review of on-state resistance studies performed using GaN-based photoelectric devices to determine areas to further study *[ongoing].*
3. Task – Determine project milestones, tasks, and timeline for optimizing on-state resistance in GaN PCSS *[ongoing]*.

(B) Milestone – Build model of GaN PCSS in TCAD and COMSOL to begin simulation studies *[ongoing].*

1. Task – Build simple, working preliminary GaN PCSS model in COMSOL that can be subsequently altered for more complex analysis of on-state resistance *[Complete – JAN 22]*.
2. Task – Build a working preliminary GaN PCSS model in TCAD to determine which modeling software will provide accurate, efficient results for different parameters affecting on-state resistance *[Complete – MARCH 22]*.
3. Task – Determine parameters that can be altered using TCAD and design studies using this program *[Ongoing]*.
4. Task – Compare simulation results with available experimental results to determine validity of models using TCAD and/or COMSOL *[APRIL 22]*.
5. Task – Set up parametric sweep studies *[MAY 22]*.

(C) Milestone – Determine device level characteristics and relationship with material characteristics—relationship between device and material level characteristics—that can be altered in simulation allowing for optimization of on-state resistance and efficiency of GaN:C PCSS and complete study on leveraging these parameters.

(D) Milestone – Determine circuit and incident photon source characteristics to be studied using simulation towards minimizing on-state resistance in GaN:C PCSS.

(E) Milestone – Design simulation based on Liu, 2021 paper using nano-structures on the surface of the device to overcome shallow absorption depth.

(F) Completion of manuscript on optimizing on-state resistance in GaN:C PCSS *[Ongoing]*

4.1.3 *Progress Made Since Last Report*

(F) Work is currently focused on manuscript preparation. See the April 2022 MSR for the most up-to-date summary of this project.

4.1.4 *Summary of Significant Findings and Mission Impact*

(A) Literature review continues towards determining changeable parameters to optimize on-state resistance in GaN PCSS, leading to a material option that provides improved efficiency and SWAP-C2 capabilities for a PCSS-based RF generation system.

Constraints:

- Linear mode due to minimal jitter operation and increased device lifetime.
- Intrinsic activation because of increased optical efficiency over extrinsic activation.
- Limited to lateral devices resulting from intrinsic mode constraint.

Changeable Parameters:

- Material and growth characteristics: doping concentration, substrate type and quality
- Device geometry: gap length, device area, interdigitated vs traditional linear, etc.
- Laser characteristics: incident wavelength, incident power (number of photons), energy density, and spot shape/size.
- Nano-structure topology: increasing active volume in the device to overcome on-state resistance minimization limitations due to shallow absorption depth of the photon source through utilizing an array of fins <1/2 the incident wavelength, to prevent scattering. This allows for improving optical efficiency without increasing the incident laser energy (number of photons) thus preventing increased laser costs and size. A similar study using GaAs PCSS devices showed an increase in photocurrent from 1.9 μA to 106 μA for a trigger fluence of 3.8 mW/cm^2 [1].

(C) A working GaN PCSS model has been created using both COMSOL Multiphysics and Silvaco TCAD to allow for parametric studies towards minimizing on-state resistance in GaN PCSS without the need for manufacturing several iterations of devices.

(F) Work towards a manuscript based on optimizing on-state resistance in GaN:C PCSS has been started with the first version of the introduction written and currently being edited.

4.1.5 *References*

[1] J. S. Sullivan and J. R. Stanley, “Wide bandgap extrinsic photoconductive switches,” *PPPS-2007 - Pulsed Power Plasma Sci. 2007*, vol. 2, pp. 1040–1043, 2007.

[2] A. D. Koehler *et al.*, “High Voltage GaN Lateral Photoconductive Semiconductor Switches,” *ECS J. Solid State Sci. Technol.*, vol. 6, no. 11, pp. S3099–S3102, 2017.

[3] G. B. Stringfellow, *Organometallic Vapor-Phase Epitaxy: Theory and Practice*. San Diego, CA: Academic Press, 1999.

[4] R. Liu, A. Shang, C.-J. Chen, Y. G. Lee, and S. Yin, “Nanostructure Enabled Lower On-State Resistance and Longer Lock-on Time GaAs Photoconductive Semiconductor Switches,” Opt. Letters, vol. 46, no. 4, pp. 825–828, 2021.

[5] Zhang, K. Liu, S. Gao, and Y. Shi, “Characteristics of GaAs PCSS triggered by 1 μJ laser diode,” IEEE Trans. Dielectr. Electr. Insul., vol. 22, no. 4, pp. 1991–1996, 2015.

5 Drift-Step-Recovery-Diode-Based Source Alternatives

5.1 Drift-Step Recovery Diode and Pulse Shaping Device Optimization

(Jay Eifler)

5.1.1 *Problem Statement, Approach, and Context*

Primary Problem: Drift-step recovery diodes (DSRDs) and DSRD-based pulsed power systems are competitive with PCSS-based systems for HPM cUAS, with the benefit of not requiring a laser. Maximizing peak power while maintaining characteristic ns-order DSRD rise times requires optimization of the DSRD device design and pulser. Other considerations are for compactness, low-jitter, cooling required, and additional pulse-sharpening device within the pulse shaping head circuit. Additional goals for pulse repetition frequency are also to be satisfied for various applications.

Solution Space: By altering DSRD device parameters (geometry, doping, irradiation), optimize single-die and stack designs for peak power and risetime within various inductive pulser circuit topologies. Also optimize the pulse sharpening device (PSD) within the pulse shaping head circuit.

Sub-Problem 1: TCAD and SPICE models of the DSRD are inaccurate and must be improved. PSD models have not been developed.

Sub-Problem 2: Inductive pulser designs are complicated by the DSRD (and PSD) parameter variability. Use TCAD and/or SPICE models to account for variability and improve pulser design.

State-of-the-Art (SOTA): MW peak power and ns-order risetimes have been achieved in DSRD-based pulsed-power systems employing DSRD stacks for higher voltage holding and parallel lines of DSRD to increase current. PSD have sharpened DSRD pulses to 100 ps-order.

Deficiency in the SOTA: A lack of accurate TCAD and SPICE models make design of DSRD and DSRD-based inductive pulser circuit topologies (with or without PSDs) difficult to the level of tens of MW of peak power while maintaining ns-order risetime (or sharpened 100 ps-order). In addition, DSRD (and PSD) fabrication variabilities further complicate pulser design.

Solution Proposed: Develop further modeling capabilities in TCAD and SPICE for DSRD and DSRD-based inductive pulser circuit topologies to optimize DSRD and inductive pulser designs, especially for maximum peak power and minimum risetime, but also for low-jitter, reduced cooling, and compactness. Additionally, optimize pulser with PSD and pulse shaping head circuit.

Relevance to OSPRES Grant Objective: DSRD-based systems eliminate laser requirements necessary for PCSSs and are competitive in terms of thermal requirements and peak power. With sharpening, the DSRD-based systems can produce comparable risetimes. The SWaPC^2 cooling requirements of HPM cUAS systems can be solved with DSRD-based pulsed power systems, and low-jitter DSRD-based systems can be used for beam-steering in phased-arrays.

Risks, Payoffs, and Challenges: DSRD must be arrayed and staged to increase current since DSRD are limited in their ability to operate at high current densities. DSRD and PSD must also be stacked to operate at high voltages necessary for high peak power and maintain low risetimes. The stacking methods can damage dies and produce variable results in risetime and DSRD diffused doping profiles can be difficult to achieve and may require epitaxial methods. SPICE device models for DSRD are unavailable and must be developed, and questions remain about TCAD limitations for DSRD and PSD modeling.

5.1.2 Tasks and Milestones / Timeline / Status

(A) Milestone – Develop DSRD SPICE model within SmartSpice using the CMC diode model (built-in and Verilog-A).

1. Task – Develop accurate forward IV, reverse CV and reverse recovery testing (RRT) modeling in CMC diode model using either built-in (faster) or Verilog-A (customizable) models; On-going [APR-JUN 2022];

2. Task – Develop reverse IV and forward CV modeling and parameters in SmartSpice CMC diode models (built-in and/or Verilog-A); Preliminary exploration [MAY-JUL 2022];

3. Task – Develop 1x1 DSRD-based pulser recovery parameters within CMC diode model of SmartSpice (built-in or Verilog-A) and compare to RRT parameters; On-going [APR-JUL 2022];

(B) Milestone – Complete LTSPICE parameterization of the standard diode model for DSRD inventory.

1. Task – Finish Gen2.2 DSRD LTSPICE parameter extraction; On-going as received [APR-MAY 2022];

(C) Milestone – Develop automated fitting procedures for developed LTSPICE and/or SmartSpice DSRD models.

1. Task – Improve speed/accuracy/size of brute force fitting methods for LTSPICE and SmartSpice diode models; On-going [APR-JUN 2022];

2. Task – Improve python-based fitting methods for diode models used in LTSPICE and/or SmartSpice; On-going [APR-JUN 2022];

3. Task – Improve use of SmartSpice Optimizer for parameter fitting of diode models; On-going [APR-JUN 2022];

4. Task – Develop automated fitting procedures for Verilog-A diode models (CMC or custom); Preliminary exploration [APR-AUG 2022];

(D) Milestone – Convert manufacturer PSPICE and PSPICE/LTSPICE unencrypted device models into SmartSpice format for use in DSRD-based pulser simulation.

1. Task – Convert unencrypted PSPICE/LTSPICE Cree MOSFET model into SmartSpice format; On-going [APR-JUN 2022];

2. Task – Convert unencrypted Texas Instruments Gate Driver model from PSPICE into SmartSpice format; On-going [APR-JUN 2022];

(E) Milestone – Develop DSRD parameters for new 371A semiconductor analyzer measurement data (forward IV and reverse IV).

1. Task – Develop standard diode LTSPICE 371A semiconductor analyzer measurement data parameters; On-going [APR-JUN 2022];

2. Task – Develop SmartSpice CMC (Verilog-A) 371A semiconductor analyzer measurement data parameters; On-going [APR-JUN 2022];

(F) Milestone – Determine performance of doping profiles within TCAD

1. Task – Determine TCAD performance of SOS, dynistor and thyristor doping profiles; Doping profiles not yet received; [?-? 2022];

2. Task – Determine TCAD performance of square root DSRD doping profiles; Not yet begun [? 2022];

3. Task – Determine TCAD performance of Gen3 manufacturer doping profiles; Not yet begun [? 2022];

4. Task – Determine recovery behavior of DSRD doping profiles within TCAD for development of custom Verilog-A CMC-based DSRD models; Not yet begun [?-? 2022];

5. Task – Determine effect of doping and defects on DSRD forward IV performance; Not yet begun [?-? 2022].

5.1.3 *Progress Made Since Last Report*

(E.1-2) Develop forward IV parameters for 371A semiconductor measurement data

A sectional or tabulated-like diode model was implemented in SmartSpice CMC Verilog-A code for DSRD forward IV. The model visually had a continuous appearance and will next be tested for convergence in forward IV and then pulser simulations. Other options exist if the sectional model fails to converge adequately. TCAD results have verified the forward IV from the spreading resistance profile (SRP) of the Gen2 doping profile, but TCAD results for the EG-series DSRD did not replicate the experimental forward IV due to a lack of knowledge of the EG-DSRD doping profile and manufacture.

5.1.4 *Technical Results*

(E.1-2) Develop forward IV parameters for 371 semiconductor measurement data

Previously, forward IV fitting had been accomplished for the whole curves of either Keithley 2400/6485-picoammeter or Tektronik 371 data that cover different voltage and current ranges of the DSRD. The lower part of the 371 data could not be fit well nor could both the picoammeter and 371 be fit for a complete fit of the whole set of experimental forward IV data. Effort has shifted from device modeling to improving the quality of the experimental forward IV data with device modeling as parallel effort. The device modeling effort is focusing on accurately fitting both the picoammeter and 371 forward IV data within the SmartSpice CMC Verilog-A diode model for DSRD pulser simulation.

The 371 and 6485 picoammeter data were both separately fit using a sectional method (or for a limited range of voltage and current with different parameters for each voltage section of the forward IV). One issue with a sectional method is the allowable discontinuity at joins between fitted sections. Figure 5.1.1 shows the results of sectional forward IV fitting (and the continuities via colored voltage regions) for picoammeter data of EG1562. Figure 5.1.2 shows a sectional forward IV fitting of 371 data for EG1608.

The region of missing data between the picoammeter and 371 (or 2450 and 371) must be filled in and this has been accomplished in April 2022 Grant Report. However, the lowest part of the 371 data is likely inaccurate and is the only part of the data not fit well. This means the region of missing data is larger and must be fit between the data endpoints. Next the forward IV must be sequentially refit in forward IV simulations as small errors exist in the production of the forward IV fit within the Verilog-A code. New higher resolution 371 experimental data also been taken and may improve the fitting. Also, more complete forward IV from both the Keithley 2450 Sourcemeter and the Tektronik 371 semiconductor analyzer can also improve fitting.

The Gen2 DSRD have a different shaped forward IV that can be fit easily in both LTspice and SmartSpice. The EG DSRD have been the focus of forward IV fitting since stacked EG are available and have been tested in the DSRD pulser to which the pulser simulations can be verified. The main concern with the sectional fitting is whether it will first converge in forward IV simulation and next in transient pulser simulation. If this method of fitting fails due to the small discontinuities that exist in the sectional forward IV three other methods can be used to develop a forward IV.

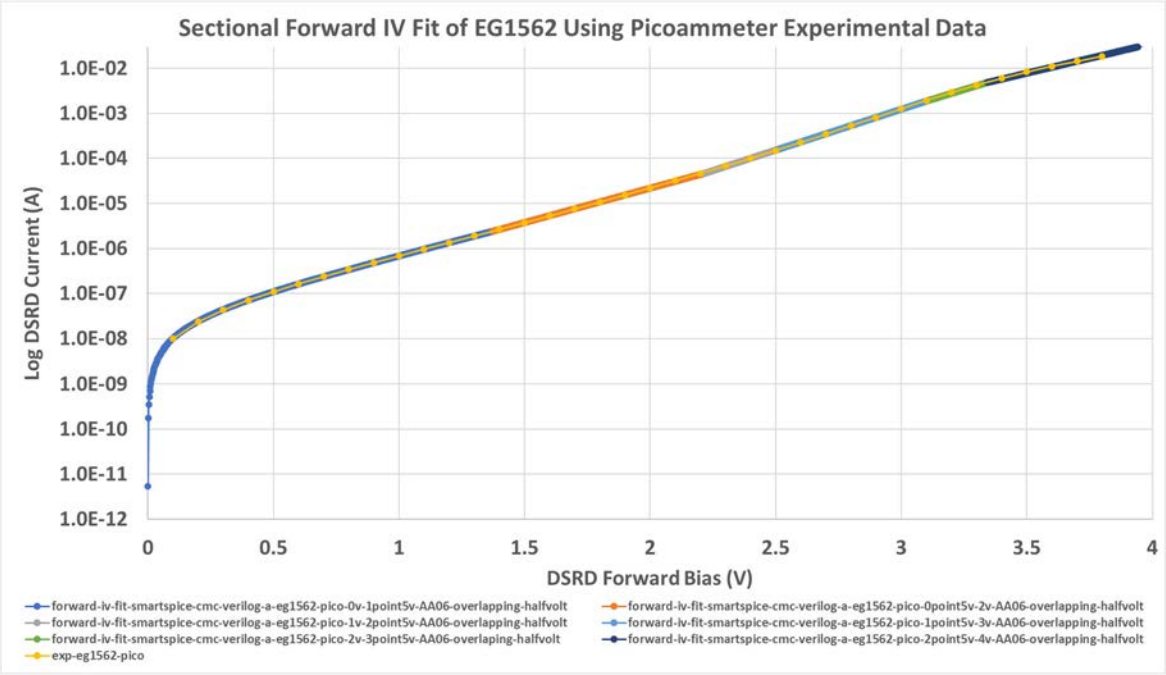

Figure 5.1.1. Sectional Fit of EG1562 Keithley 6485 Picoammeter forward IV showing continuity at joined regions.

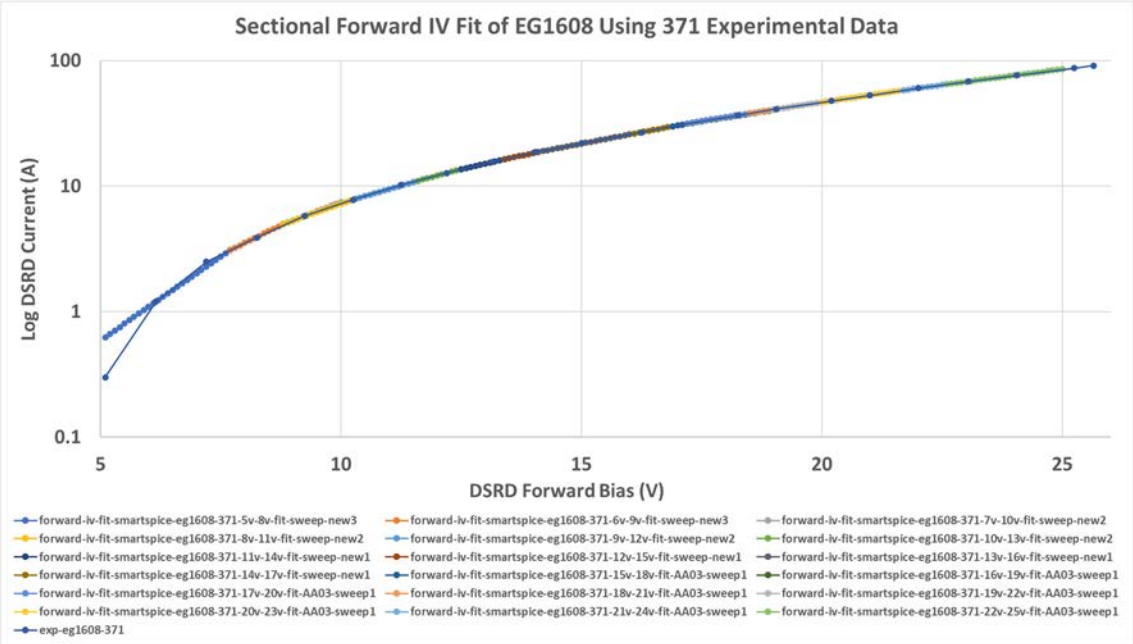

Figure 5.1.2. Sectional Fit of EG1608 Tektronik 371 forward IV showing continuity at joined regions. The lowest voltage section is not fit as well and is suspect experimental data.

The first alternative fitting method is to fit 6485 picoammeter and 371 data separately as full curves over the entire range with one set of parameters as usual (has already been accomplished) and then fit the two curves together smoothly since there are only two places that must be smoothly joined (since there is a missing data gap). This joining has been successfully done in part. One issue is the lower part of the 371 could not be fit previously and is very likely inaccurate so must be excluded as missing data. Also, the picoammeter data is to be replaced and/or supplemented with Keithley 2450 sourcemeter forward IV which goes to a higher level of current testing (1 A).

The second method is to use only the 2450 and/or 6485 picoammeter data and fit only RS (the inverse slope of the linear region of the curve) from the 371 data. This method has been used before and does not closely match the forward IV but reflects some of its properties (only method available for LTspice).

The third method is the highest risk and involves manually changing the Verilog-A code to incorporate smoothing functions to allow use of the forward IV data points directly (or in part) to implement a tabulated DSRD forward IV model (DC component of current in the diode model). The sectional fit was done first since it would be easier to implement and lower risk.

Having an accurate forward IV modeled is key to accurately representing the DSRD behavior in circuit simulation. The Gen2 DSRD should be easily matched to the simulated and experimental forward IV but have not been experimentally tested in the DSRD pulser. The EG-series DSRD forward IV are difficult to match. TCAD simulations of the Gen2

DSRD doping profile have shown a close match of the TCAD forward IV and the experimental forward IV as can be seen in Figure 5.1.3. Attempts were made to match the EG-series DSRD forward IV by altering the doping profile but were not successful. A combination of doping profile gradient, defects and metals used for contacts could be responsible for the EG-series DSRD forward IV (this same EG style forward IV has been seen in the literature for power diodes).

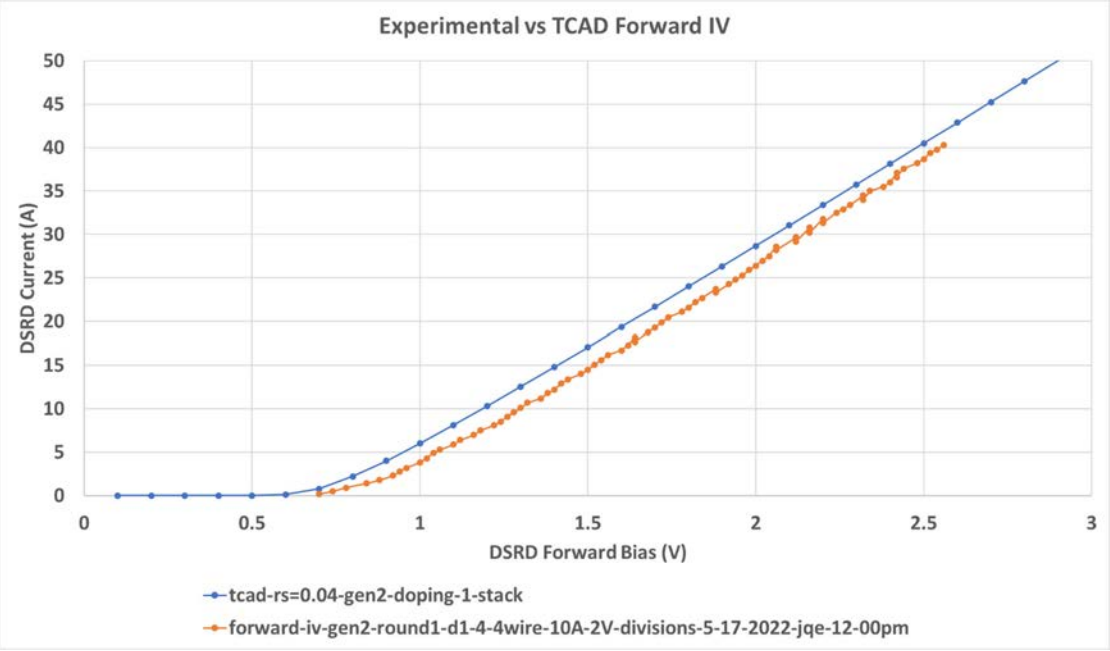

Figure 5.1.3. Forward IV comparison between TCAD (blue) and Experiment (Orange).

In conclusion, the parameters for a sectional fit have been determined for both the picoammeter and 371 data of and EG DSRD. Next these parameters are incorporated and adjusted slightly for a SmartSpice CMC Verilog-A diode model forward IV simulation. With successful convergence and matching of the experimental forward IV, the pulser simulations can be more readily matched to experiment. A 371 survey of EG and Gen2 diodes is underway from which averaged forward IV (of device and measurement variability denoted by min and max) can be developed and a determination of RS for use with the LTspice models. With improved low resistance, high current measurements using a 4-wire technique in the 2450 Keithley sourcemeter, a complete experimental (some missing data) forward IV can be measured and fit for SmartSpice DSRD pulser simulations using the CMC diode recovery model.

5.1.5 *Summary of Significant Findings and Mission Impact*

(A) Development of DSRD Model Within SmartSpice CMC Diode Model

The SmartSpice circuit simulation software has been received in JAN 2022 and in FEB 2022 the Verilog-A CMC diode code was retrievable from the Si2 organization website.

Development immediately began of the CMC diode model for DSRD modeling by producing forward IV, reverse CV and reverse recovery testing simulations and fitting to example DSRD in the inventory. Recovery parameter fitting within the 1x1 DSRD-based pulser has also begun. The capability of the CMC diode model for modeling DSRD can now be assessed. Any deficiencies in the CMC-DSRD model can be improved using the programmable Verilog-A code of the CMC diode model to include DSRD specific modeling equations based on theory, TCAD simulation, experiment and the literature. The Verilog-A code has been modified to allow different fitting parameters for different sections of the curve so that real, experimental forward IV can be accurately fit. Improved forward IV fitting in the Verilog-A CMC diode model will allow for improved pulser simulation.

(B) LTSPICE Standard Diode Model Parameter Development for DSRD Inventory

DSRD in the inventory of received diodes (legacy, EG and Gen2) have been fit for LTSPICE standard diode model parameters (for forward IV, reverse CV and reverse recovery testing) for use in LTSPICE DSRD-based pulser simulations and to provide another metric for the characterization of the DSRDs in comparison to pulser performance. Some details of the very low voltage and current forward IV have not been fit but the fitting is still very close when visually inspected in non-log format. Reverse IV have not been fit in the standard diode model since it cannot capture the behavior and breakdown has not yet been measured, only estimated. Forward CV measurement are problematic and not fit mostly since the forward CV parameters in the standard diode model are used for recovery modeling. Various methods exist in LTSPICE to improve recovery parameter fitting but are either inadequate (Vp or carrier viscosity) or non-realistic (adjustment of reverse CV parameters) but have produced fits within 10% error for DSRD-based pulser performance. Gen2.2 experimental data has been received fitted within LTspice but there is high, variable series resistance in the Gen2.2 measurements that are being addressed with a new fixture and testing.

(C) Develop Automated Fitting Procedures for LTSPICE and SmartSpice

The current best method of fitting is using a brute force method of running LTSPICE or SmartSpice simulations sweeping over the desired parameter space. The brute force method can produce the most accurate fits but requires long simulation times and cannot be used to explore large parameter spaces easily (which is why more physically-based models using only measurable parameters is derisable). There is ultimately a limit to how quickly and accurately one can develop parameter sets. Another method is to program in the model equations into Python and use their curve fitting tools, however this method cannot incorporate circuit simulation and will therefore be less effective in producing accurate fits but is much faster in simulation time (can depend on how much parameter adjustments affect DSRD-based pulser performance on which method to use). The other fitting method is to use the built-in optimizer within SmartSpice, but the optimizer has not yet produced as good of fits consistently as the brute force method and will take some experience in using well.

(D) Conversion to SmartSpice of Manufacturer Device Models

Unfortunately, manufacturer device models are not openly available in SmartSpice only PSPICE and to some extent LTSPICE (usually converted from PSPICE). Therefore, the available PSPICE and PSPICE/LTSPICE models must be converted to the SmartSpice format, otherwise keeping the model the same. Note that encrypted models cannot be converted into SmartSpice, such models either have to be developed from scratch and either the datasheet or additional experimental tests used (or purchased from Silvaco for SmartSpice if available).

The unencrypted Cree MOSFET model has been converted into SmartSpice and tested within 1x1 DSRD-based pulser simulations and compared to LTSPICE simulations successfully. The unencrypted Texas Instruments gate driver model has also been converted into SmartSpice successfully. One issue with the driver model is it is intended for PSPICE but used often in online discussion in LTSPICE. However, close examination of the model shows that the model cannot perform correctly in all pin conditions in LTSPICE due to incorrect parameter types used in a voltage-controlled switch within the driver model. The voltage-controlled switch has been correctly implemented in the SmartSpice conversion and can be fixed for the LTSPICE version (Texas Instruments has not responded to inquires). Neither the MOSFET or gate driver models have been extensively diagnostically tested and compared to the datasheets which are often somewhat different to the free provided models (only so accurate).

(E) IV Parameter Development for 371A Semiconductor Analyzer Measurement Data

A 371A semiconductor analyzer has been acquired and setup for forward IV testing with the potential for higher voltage/current reverse IV testing and breakdown. Initially concerns arose about the shape of the forward IV and whether temperature distortion was occurring at the higher voltages and current available with the 371A compared to the picoammeter. However, published power diode forward IV have been discovered showing similar forward IV at room temperature. 371A testing will proceed by testing more DSRD and subsequently using thermocouples and/or heat sinks. 371A higher voltage/current forward IV testing is necessary to characterize the DSRD in the diode models to perform correctly in the DSRD-based pulser simulations. How accurate the forward IV must be, has not been determined, as well as, to what extent individual diodes can be reliably distinguished in modeling. A new method for fitting forward IV has been implemented in the CMC Verilog-A diode modeling code that will allow for more accurate fitting of the 371 data for its full range. More rigorous forward IV testing has been implemented incorpating a number of modifications to the forward IV test fixture, cabling and testing methods (2- vs 4-wire) yielding forward IV with definite error bars. Breakdown testing has also been performed for Gen2 and EG DSRD showing 40% yield for higher breakdown devices needed for DSRD stacking and DSRD pulser testing.

(F) TCAD-Based Doping Profile Performance Evaluation

Many DSRD TCAD simulation studies have been performed assessing the doping profiles used for the DSRD manufactured by SPT and in stock (this summary includes work from the past six months). The TCAD modeling has been temporarily on hold as effort is focused toward developing an accurate SPICE DSRD model due to the unavailability of manufacturer device models for MOSFETs and gate drivers within TCAD. A MOSFET model was developed for the Cree MOSFET for use within TCAD but still had some

differences when used in pulser simulations, so the development of the DSRD SPICE model was prioritized so that manufacturer models (for MOSFETs and drivers) could be used.

Doping profiles are forthcoming for various SOS, dynistor and thyristor devices and TCAD will be used to assess their performance. Some interest has been expressed in assessing square-root doping profiles for DSRD. Gen3 doping profiles from the manufacturer have yet to be assessed within TCAD for performance differences with the requested doping profiles. As well, the recovery models within the CMC diode model are themselves based on PIN diode TCAD simulations and TCAD can perform DSRD doping profile specific simulations to determine model equations and parameters. Additionally, the forward IV behavior of our DSRD can be modeled as seen in the 371A semiconductor analyzer mesaurements. TCAD modeling will continue to be of use in device modeling since it is the only way to assess doping profiles.

5.1.6 *References*

[1] Chandra Bose, JV Subhaus, I. Imrie, H. Ostmann, and P. Ingram. “SONIC-A New Generation of Fast Recovery Diodes [D].” IXYS Semiconductor (2011).

5.2 Pioneering Drift-Step Recovery Diode Processing and Manufacturing

(Alex Usenko)

5.2.1 *Problem Statement, Approach, and Context*

Primary Problem: DSRDs have not increased in performance since the 1960’s due to reliance on deep diffusion manufacturing. Their voltage-to-risetime, dV/dt, remains about 10^{12} V/s. To achieve the 10^{13} V/s (10 kV/ns) voltage-to-risetime required by an all-solid-state HPM pulse generator in support of the Naval afloat mission, improving DSRD manufacturing techniques is critical.

Solution Space: Leverage applicable concepts from the mainstream silicon chipmaking industry and apply new manufacturing methods to DSRD processing.

Sub-Problem 1 – Diode silicon surface termination/passivation: The SOTA uses diode termination by a vertical wall. This design results in low breakdown voltage as it is limited by surface breakdown. To increase the diode breakdown voltage to closer to that of the bulk silicon breakdown voltage value, the vertical side wall design must be avoided.

Sub-Problem 2 – Stacking of DSRD dies: The SOTA is based on eutectic soldering of diode dies into a stack, which limits the stack lifetime to below 10^{12} pulses. Also, the SOTA did not apply the methodology of stacking wafers first, then cutting into dies. Switching to wafer level stacking will decrease the number of stacking operations by more than 100x.

Sub-Problem 3 – Packaging of stacked dies: *The* SOTA uses bare stacked DSRDs. Mounting the bare stack into a press-pack, stud or power module type package will improve long-term stability, such that the stack will survive a much higher number of pulses before it burns out.

State-of-the-Art (SOTA): In a recently published paper (June 2022),[1] the Russian St. Petersburg team at the Ioffe institute reported ~500 V/ns voltage rise rate on a load. A competing team at Ekaterinburg, Russia [2] reports slightly better pulse performance – but for SOS (SOS is similar to DSRD) combined with an avalanche shaper. Both teams use outdated deep diffusion technology. As one can see, there has not been any significant improvement in DSRD pulse performance since the pioneering work done in 1960 [3].

Deficiency in the SOTA: First, no DSRDs have been manufactured using epitaxy technology with doping profile optimization. Second, no DSRD processing method exists that integrates side passivation with silicon dioxide. Finally, an acceptable DSRD stacking process has yet to be developed.

Solution Proposed: Manufacture DSRDs within the continental United States using an epitaxial growth process leveraging the optimal characteristics (e.g., doping profile, carrier concentration) determined through the work performed by our simulation team (previous chapter of this report) and through working with industry partners at Semiconductor Power Technologies (SPT), Livermore Semiconductor Research Laboratories (LSRL) and Lawrence Livermore National Laboratory (LLNL – Voss Group).

Relevance to OSPRES Grant Objective: DSRD manufacturing technology is a major building block of short-pulse high-peak-power defense systems. Our new disruptive process flow for DSRDs enables not only manufacturing of DSRDs at scale, but within the continental United States (CONUS). In doing so we will redefine the SOTA by producing optimal DSRDs. Further, DSRDs will be used within best-in-class HPM pulse generators which become part of more advanced defense systems within the Navy arsenal.

Risks, Payoffs, and Challenges:

Risks: As the process of producing DSRDs using epitaxial growth with doping profile design is novel, uncharted territory, there is inherent risk to its success. Additionally, post-processing methods based on the discussions provided in the ***Sub-Problems*** section are not well-established.

Payoffs: Replacing traditional deep diffusion technology with a new process integration scheme would allow better DSRD pulse performance. Electrical breakdown voltage, reliability, and lifetime are expected to increase, and rise time on a load is expected to decrease.

5.2.2 Tasks and Milestones / Timeline / Status

(A) Milestone – Produce epitaxial DSRDs that contain optimal exponential doping profiles and carrier concentrations /estimated JUN*22*.

1. Task – Design of experiment on 25 wafers through negotiations with vendors / *MAY–JUL21* / Completed
2. Task – Perform DSRD stack epitaxy on 13 wafers at SVM Inc., and 25 wafers at LSRL / *JUN–AUG21* / Completed.

3. Develop process integration scheme that uses epitaxy instead of deep diffusion / *JUL–OCT21* / Completed.
4. Compare traditional DSRD technology and suggested integration scheme. List disadvantages of traditional processes and define potential advantages of new processes / MAY–NOV21 / Completed.
5. Run Gen2 and Gen3 lots. Gen2 is on wafers with epi from SVM, Inc., Gen3 is on wafers with epi from LSRL. Gen2 uses the same BEOL as Gen1. Run BEOL of Gen3 – using our new patented processing scheme – TMAH etch, oxidation, selective electroless metal deposition, wafer bonding, sawing into diode stacks / OCT21–MAY22.
6. Submit Gen2 and Gen3 diode lots to UMKC team for pulsed performance measurements; collaborate with team on determining optimal doping profile through DoE (design of experiments) analysis by Minitab software / OCT21–MAY22.

(B) Milestone – Develop diode separation technique while keeping wafer integrity / Estimated completion FEB22.

1. Design lithography masks for short loop experiment, submit order to vendor. / MAR–APR21 / Completed.
2. Design short loop experiment for V-groove etching for diode separation. / MAR–APR21 / Completed.
3. Run short loop experiment for the diode separation by anisotropic etch; analyze results / MAY–OCT21 / Completed.
4. Based on results of previous short loop run, adjust equipment, and process recipes to achieve sufficient etch uniformity across the wafer. Run on updated equipment and recipe to prove etch uniformity. / Completed.
5. Design lithography masks for epi DSRD run; submit order to vendor. / OCT21 / Completed.
6. Run Gen3 lot through V-groove etch step, transfer lot to next process step. / Estimated MAY22.

(C) Develop Ohmic contact deposition technique integrable with epitaxy, diode side termination/passivation, and wafer bonding steps / estimated AUG21 - MAY22.

1. Design short loop experiment to determine technical feasibility of selective electroless deposition of metal stack as a method of Ohmic contact forming in the DSRD process integration scheme. / OCT21 / Completed.
2. Determine vendor from which to order electroless deposition kits; obtain quotes, order, receive the kits. / OCT21 / Completed.
3. Run short loop experiment – nickel-copper-tin stack electroless deposition on a blanket wafer. Analyze results. / DEC21 / Completed.

4. Develop process recipe for the metal stack deposition to use in Gen3 DSRD lot manufacturing / estimated JAN22.
5. Run the selective metallization step on Gen3 lot; transfer the lot to next processing step. / Estimated FEB22.

(D) Develop wafer stack bonding technique integrable with the rest of Gen3 process flow / estimated SEP–FEB22.

1. Design short loop experiment for bonding 2 diode dies with Ni-Cu-Sn layers by solid–liquid interdiffusion. / SEP21 / Completed.
2. Run 2 dies short loop experiment. Analyze results. / MAR22 / Completed.
3. Test technical feasibility of multiple wafer bonding by bonding 10-wafer stack / estimated APR22.
4. Upon proof of technical feasibility of 10-wafer stacking, develop process recipe to use for processing of Gen3 DSRD lot / estimated MAY22.
5. Run wafer bonding step on Gen3 lot, transfer the lot to next processing step. / Estimated MAY22.

(E) Develop wafer stack sawing technique into DSRD stacks, integrable with the rest of Gen3 process flow / estimated NOV21–MAY22.

1. Design sawing process using Disco saw available at Semiconductor Power Technologies for cutting 10-wafer stack / estimated JAN22.
2. Run short loop cutting of blanket bonded 10-wafer stack. Analyze results. / Estimated FEB22.
3. Develop process recipe for Disco saw tool to use for Gen3 lot. / Estimated MAY22.
4. Run sawing step on Gen3 lot / estimated MAY22

(F) Develop diode side passivation process integrable with the rest of DSRD process flow.

1. Test compatibility of thermal oxidation for the diode side passivation with preceding anisotropic etch step / estimated FEB22.
2. Alternative diode side passivation process: design short loop experiment on room temperature oxidation by forming porous Si film and oxidizing the porous film / APR–OCT21 / Completed
3. Run part of Gen3 lot using the oxidized porous Si as diode side passivation / estimated FEB22.
4. Second alternative diode side passivation process: Design short loop experiment on room temperature oxide deposition from oversaturated fluorosilicic acid / estimated MAY–JAN22.
5. Run part of Gen3 lot using the oxidized porous Si as diode side passivation / estimated FEB22.

6. Choose the best from 3 methods of diode side surface passivation techniques / estimated FEB22.

(G) Develop a DSRD process based on out-diffusion (opposite to traditional in-diffusion process).

1. Process Gen4 lot based on process integration scheme described in our patent application filed in / estimated MAY22.

(H) Find vendor that manufactures press-pack parts, order the parts, and encapsulate the DSRD stacks into the press-packs / estimated MAY22.

5.2.3 *Progress Made Since Last Report*

(A5) Gen3 lot fabrication. Upon inspection results, the lot is divided into 3 sub-lots, each sub-lot continues in process flow.

(A5) Gen2 lot fabrication. Parylene fails to perform as a mask for HNA etching; currently we are looking for an alternative mask material.

(B4) Process step development: die separation on wafers by anisotropic etch in TMAH (tetramethylammonium hydroxide) based bath. We have compared surface roughness by AFM – after a standard etching recipe and after our new TMAH/DMSO (dimethyl sulfoxide) mixture etch chemistry. The new recipe has shown 2 orders of magnitude improvement in roughness.

5.2.4 *Technical Results*

(B) **Gen3 lot fabrication.** Upon the bright light inspection, wafers with the high defect count (13 wafers) have been sent back to Noel Technologies - for stripping of the defective silicon nitride layer, depositing new nitride, and lithography over the nitride. Wafers with a defect count below 40 (9 wafers) will continue processing without the rework. One wafer that past the v-groove etch already - is now at the oxidation step. Fig.5.2.1. illustrates the current state of the wafer #23 in the Gen3 processing. A planned oxidation recipe is 75 minutes, wet, at 800^{o}C. It will result in the 50 nm thick SiO_2 layer – the film that is thick enough for the efficient diode side passivation, and thin enough to prevent a positive charge accumulation in the oxide. Also, the thermal budget is low enough to exclude an undesirable diffusion of the dopants in the epitaxial layers. After that step, we will continue the process flow on this wafer – nitride strip, selective Nickel electroless deposition, and conversion of the deposited Nickel into a nickel silicide. At that point we will be able to do all the static electrical testing of the finished single (non-stacked yet) Gen3 diodes on the #23 wafer.

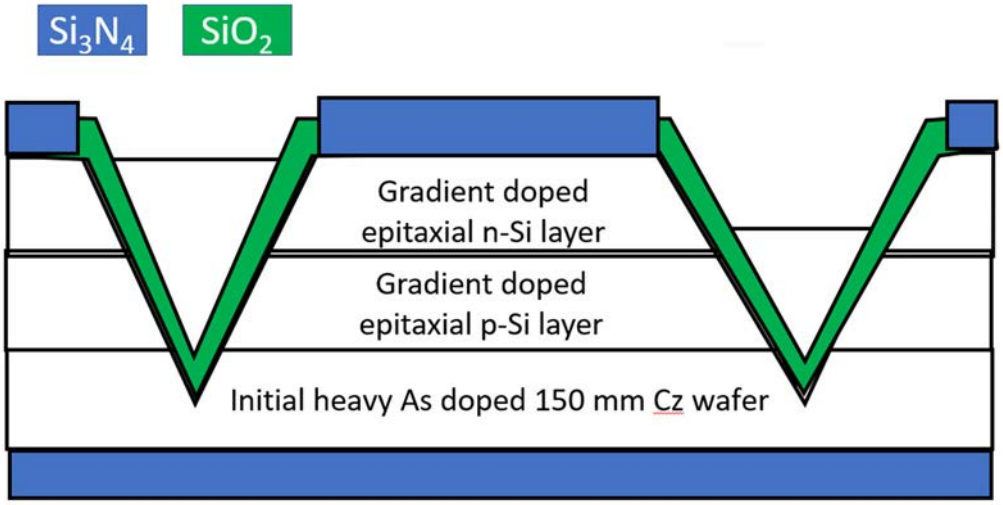

Figure 5.2.1. Simplified cross section of a die on wafer at current process stage.

(B4) **Anisotropic etch step development**. Previously, we have developed a new recipe for the v-groove anisotropic etch. This month we have performed AFM roughness measurements – to compare roughness after the standard TMAH etch recipe, and after our new recipe. The measurements were performed by NanoSurf, Inc. at their application lab in Boston, MA. The Nanosurf is a manufacturer of the AFM tools that are capable to do both - roughness and SSRM (Scanning Spreading Resistance Microscopy) measurements. The SSRM gives the same doping profile data as the traditional SRP (Spreading Resistance Profiling). In this DSRD manufacturing project, we need a quick turnaround roughness measurement – as we have a wafer bonding step in our process flow, as well as quick turnaround doping profile measurements. This Nanosurf $75K tool serves both, therefore we ordered roughness and doping profile demo measurements – considering an option to purchase the tool.

Fig.5.2.2. shows 90-micron scan maps on a bare 100 mm silicon wafer bought from Addison Engineering wafer reseller. These wafers were used for the TMAH etch recipe development, and all the rest of the AFM images are form the same wafer box.

Fig.5.2.3. is a photo of the label on the wafer box. It illustrates all the major issues while using the small wafers (smaller than 200 or 300 mm size):
1. Resellers replace the original wafer manufacturer label with their own label, thus a lot of information about the wafer is lost. In this example, reseller indicates only the very basic wafer properties – size, grade, orientation, dopant, resistivity, thickness.
2. Only the major wafer manufacturers (Shin Etsu, Sumco, MEMC, Siltronic) are capable to manufacture high quality Si wafers. Since 2002 they make 200- and 300-mm sized wafers only. Therefore, there are only 2 options while purchasing the small (100 mm here) wafers – either wafers made 20-50 years ago, or Chinese manufactured wafers (i.e., made on 50+ years old equipment). Quality of both is about the same.
3. Our diodes are completely in the epitaxially grown film on the surface of the purchased silicon wafers. It is grown on the state-of-the-art equipment; therefore, quality of initial wafers does not matter, provided we have prepared the wafer surfaces right for the

epitaxy. Though, in the short loop experiments, we use as-purchased Si wafers: so, we must adjust the results.

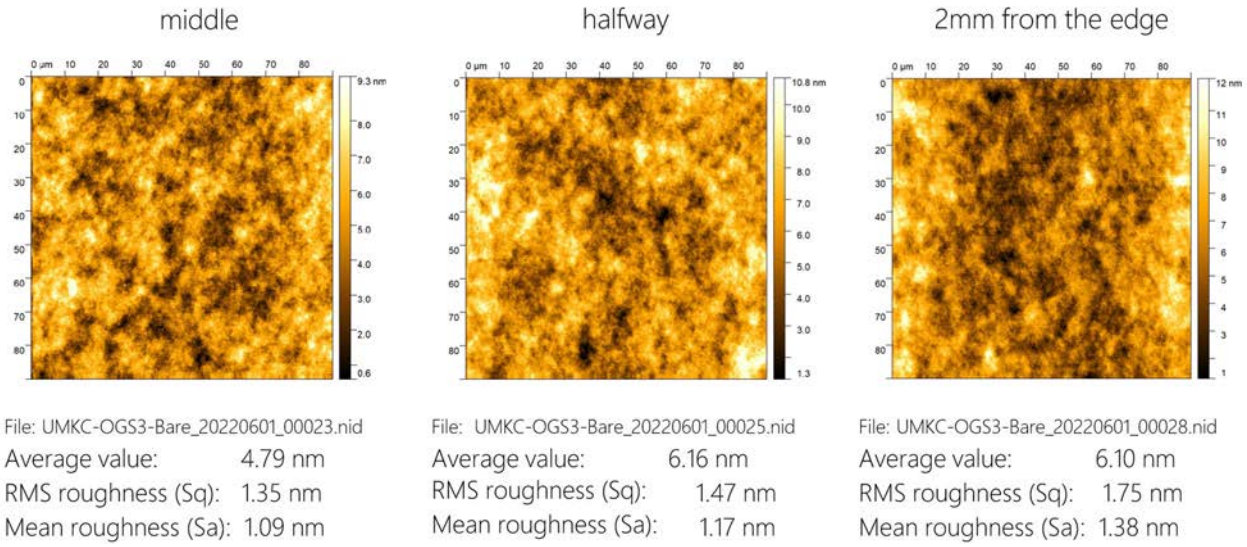

Figure 5.2.2. Wafer roughness of a control wafer (starting wafer, no processing). Courtesy NanoSurf, Inc.

Figure 5.2.3. Typical label on a wafer box – purchased from wafer re-sellers.

Thus, not a big surprise, Fig.5.2.2 shows above 1 nm rms roughness. While roughness requirement for the wafer bonding is <0.5 nm rms (i.e., these wafers will have a big number of voids – if bonded). However, we still have a number for the comparison. The AFM scans made on a FlexAFM tool show all the expected features – roughness on the

left image – at wafer center – is lowest, and it slightly increases toward the wafer edge – at 25 mm from edge (middle image), and at 2mm from the wafer edge (right image).

Fig.5.2.4 shows the AFM scans after etching in the TMAH:DMSO:water 1:1:1 mixture at 80C recipe, for 20 hours (our final recipe). Notice, about a half of the wafer thickness have been etched away (the wafer weight before the etch is about 9 Grams, and after it is about 5 Grams). Surprisingly, the wafer surface roughness is about the same as before the etching. While it is still a modified acoustic etch. The standard acoustic etch in KOH – usually used to treat back side of wafers - always results in a surface covered with the square truncated pyramids. So, we found that our TMAH/DMSO recipe is rather a polishing etch. Also, comparing Fig.5.2.2 and Fig.5.2.4 images on small scale (1.5 nm scans – right side images on both) – shows about 3X lowering of the roughness value. Thus, we experimentally proven here that our new recipe is a polishing etch. We did not expect that, but this is still a very important result – on fundamental material science side.

Fig.5.2.5 comparison shows the drastic advantage of the recipe we have developed over the standard TMAH anisotropic etch recipe. Well, this comparison is for <100> surfaces, as we run here a short loop experiment to just determine the etch rate using various recipes. Means this does not relate to roughness of <111> facet surface after the v-groove etch. Still this result has a fundamental value for, say, MEMS industry.

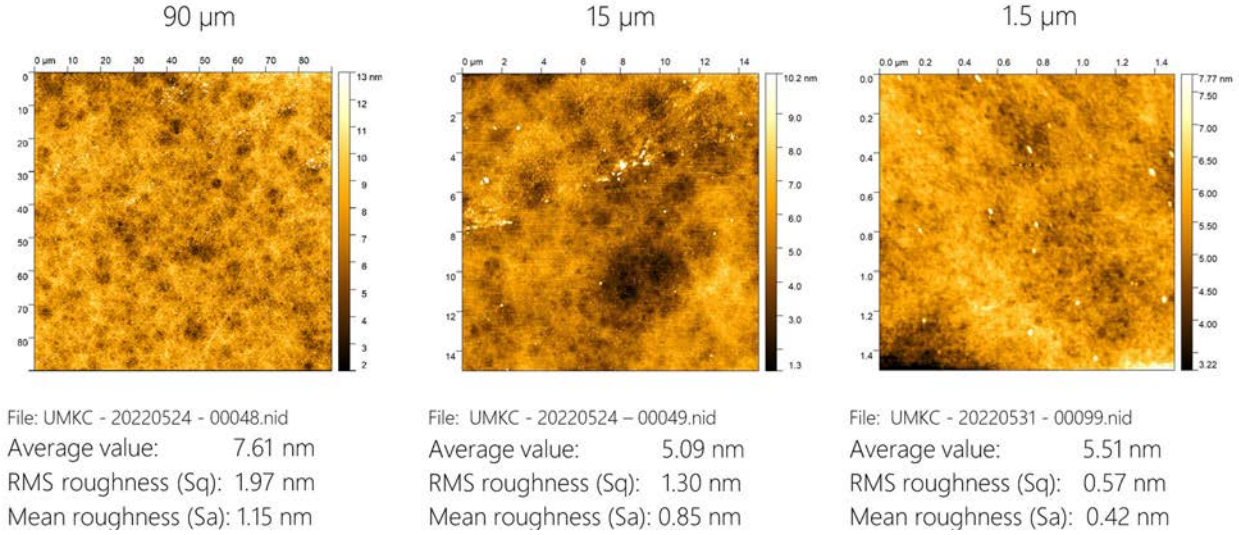

Figure 5.2.4. AFM scans on a wafer after TMAH etch in our new developed recipe – TMAH:DMSO:water 1:1:1. Courtesy NanoSurf, Inc.

As one can see on the Fig.5.2.5, the standard TMAH etch recipe (5% TMAH in water) shows 271 nm roughness – more than 2 orders of magnitude higher roughness as compared to our DMSO-modified recipes. The right image on the Fig.5.2.5 is the most informative. It shows the pyramids – on the locations were hydrogen bubbles stack to the wafer surface. The bigger the pyramids are – the longer time the individual bubble was sticking to the surface and masking the etch.

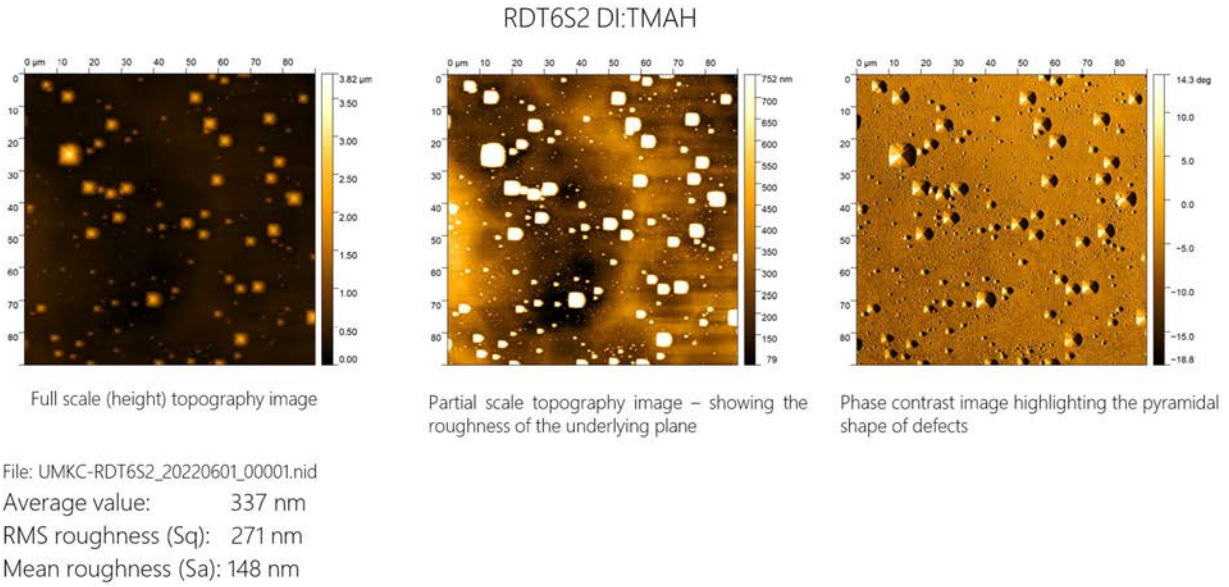

Figure 5.2.5. AFM scans on a wafer after a standard TMAH etch recipe. Courtesy NanoSurf.

Fig.5.2.6 compares wafer roughness for a standard TMAH etch (middle image) and 2 modified recipes: 1:1:1 TMAH:DMSO:water (left image) and 1:1 TMAH:DMSO. It shows that both DMSO modified recipes results in roughness that is either equal or better than the roughness of the initial wafer and are drastically different from the roughness after the standard TMAH etch – which increases the roughness from about 1 nm to more than 100 nm. Conclusion is – adding DMSO to TMAH etch allows completely suppress hydrogen bubble sticking to the wafer surface and thus obtain very smooth wafer surface.

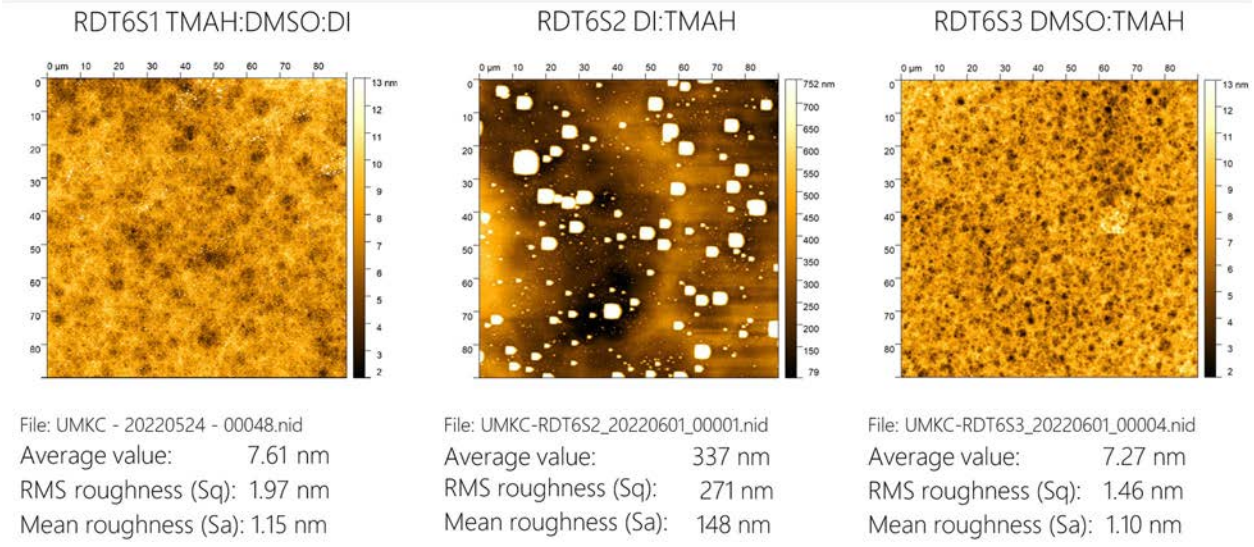

Figure 5.2.6. 90-micron AFM scans on a wafers after 3 different etch recipes. Courtesy NanoSurf, Inc.

5.2.5 *Summary of Significant Findings and Mission Impact*

(A) Several process adjustments have been implemented in processing of next Gen2 die lots. Die-to-die excessive variability is noticed. Process recipes and some equipment have been adjusted to achieve better uniformity and repeatability.

(B) Improving side termination of diodes. To prevent detrimental non-uniformity due to hydrogen bubbles sticking to wafer surface, a new process recipe has been developed. TMAH/DMSO mixture showed excellent uniformity. Using this mixture for anisotropic silicon etch never described in literature, we found this first.

(C) Replacement of unreliable metal contact deposition technique (by electron beam sputtering in vacuum chamber). Technical feasibility run on direct electroless plating of the Palladium/Nickel stack was successful. Process recipe developed for next run, plate uniform stack of Pd/Ni/Cu/Sn. State of the art electroless plating tool being donated by Hughes Research Lab.

(D) A process recipe for side passivation of diodes using a stain etch has been developed. The thickness uniformity resulting from the stain etch technique has been drastically improved. A new recipe that totally suppresses hydrogen bubbles sticking to the Si surface was found. Using that recipe, very uniform thickness (porous Si) films were successfully grown on blanket silicon wafers with both low and high doping levels.

5.2.6 *References*

[1] Lyublinsky, A. G., A. F. Kardo-Sysoev, M. N. Cherenev, and M. I. Vexler. "Influence of DSRD Operation Cycle on the Output Pulse Parameters." *IEEE transactions on power electronics*, vol. 37, no. 6, June 2022, 6271-6274.

[2] Rukin, S. N. "Pulsed power technology based on semiconductor opening switches: A review."*Review of Scientific Instruments* 91, no. 1 (2020): 011501.

[3] Boff, A., J. Moll, and R. Shen. "A new high-speed effect in solid-state diodes." in *1960 IEEE International Solid-State Circuits Conference. Digest of Technical Papers*, vol. 3, pp. 50-51. IEEE, 1960.

5.3 Characterization of SOS Diode Performance through DOE Augmentation

(Joseph Reeve-Barker, Jay Eifler & Megan Hyde)

5.3.1 *Problem Statement, Approach, and Context*

Primary Problem: Drift step recovery diodes (DSRDs) are planar diodes that are capable of nanosecond, high-frequency (10–10^3 kHz) pulses [1] with applications as opening switches in inductive energy storage (IES) pulse generation circuits. There is not a clear understanding of the effects DSRD parameters have on overall IES pulser performance. The purpose of this project is to tie the DSRD parameters to its tailored performance requirements.

Solution Space: Leveraging both design of experiment (DOE) and machine learning (ML) capabilities, we will develop a methodology of characterizing and optimizing DSRDs in order to provide fabrication recommendations in the context of application targets.

***Sub-Problem 1*:** We do not yet understand how diode parameters are tied to diode performance.

Sub-Problem 2: There is no standardized method for correlating the diode key performance indicators (KPIs) to the IES pulser generator performance.

Sub-Problem 3: The number of possible inputs for the DOE is expected to be too large, so ML will need to be leveraged in order to guide decision-making processes.

State-of-the-Art (SOTA): Standard diode measurements include curve tracers for forward and reverse IV, impedance spectroscopy for forward and reverse CV, and function generators or, for example, the Avtech pulser for reverse recovery with high voltage and/or high current when necessary. These measurements are used to generate commonly available datasheets for COTS diodes. These standard diode measurements can then be correlated to pulser performance using traditional data analytics.

Deficiency in the SOTA: The standard diode measurements and datasheets do not include pulser performance necessary to evaluate DSRDs. The datasets generated with doping profile assessment (for example spreading resistance profiling), standard diode measurements and pulser performance are too large and complex to leverage traditional data analytics and will benefit from machine learning techniques.

Solution Proposed: Develop a holistic evaluation network for DSRD characterization. This network will include a DOE that will be a continuously evolving model as diode parameters are correlated to pulser performances. Augmenting the DOE will ensure that the model will remain relevant throughout this study as more discoveries are made. Machine learning will be used as the primary decision-making tool for augmenting the DOE. Once the network is established, it will be used to outline the optimal parameters for stacks of DSRDs within an IES pulse generator.

Relevance to OSPRES Grant Objective: Bridging the gap between the theoretical and physical performance of DSRDs enables closing the gap between a low fidelity TRL3 breadboard pulse generation system, and one which is at a high fidelity TRL4 prototype level. At the TRL4 level, the DSRD-IES pulse generator system would be sufficient to replace the costly laser-based Si-PCSS HPM generator without compromise to scalability required to support the Naval afloat mission.

Risks, Payoffs, and Challenges:

Challenges: Traditional predictive analytics will be difficult to correlate with the augmented DOE due to the large volume of data. Machine learning is expected to assist with decision making processes for the DOE, but only if ideal diode characteristics have been established and good data have been used to train the machine learning model.

5.3.2 Tasks and Milestones / Timeline / Status

(A) Milestone – Establish preliminary DOE and standard operating procedure (SOP) for identifying KPIs of DSRDs [*estimated completion by MAR22*].

1. Task – Ascertain current KPIs used to optimize diodes simulated, manufactured, and utilized within the IES pulse generating circuit [completed AUG21];

2. Task – Construct preliminary DOE to acquire data on all KPIs based on Task 1 [*completed FEB22*];
3. Task – Leverage existing Python scripts to process legacy DSRD KPI data [*completed SEP21*];
4. Task – Develop new and review existing SOPs for experimental testing apparatuses used to evaluate individual KPIs and measure their performance [*completed OCT21*];
5. Task – Identify gaps/deficiencies in legacy KPI data, evaluate existing theoretical relationships to bridge gap and minimize DOE if possible [*completed OCT21*];
6. Task – Using SOPs developed in Task 4, acquire experimental data from legacy DSRDs, refine SOP(s), and assess repeatability and reproducibility [*In progress*: *SEP21–MAR22*];

(B) Milestone – Evaluate DSRD performance using the developed SOPs and facilitated by the preliminary DOE [*estimated completion JUL22*].

1. Task – Acquire data on newly manufactured 2nd generation epitaxial DSRDs from Section 5.2 using refined SOPs from Milestone A [*completed JAN22*];
2. Task – Evaluate the precision and power of the DOE [*In progress*: *MAR22–JUL22:*];
3. Task – Develop a DSRD selection guide for the pulser circuit based on the static DC test measurements *[In progress: MAR22–MAY22];*
4. Task – Correlate the static DC test measurements to the performances of the IES pulser circuits and to fabrication procedures [*MAR22–JUN22];*
5. Task – Begin training machine learning model with DSRD data to determine correlations between static DC and pulser testing results [*MAY22–JUL22*];
6. Task – Acquire data on newly manufactured 3rd generation epitaxial DSRDs from Section 5.2 using refined SOPs from Milestone A [*JUL22–SEP22*];

(C) Milestone –DSRD diode network evaluation [*on hold until Milestone B is completed*].

1. Task – Refine Python script to incorporate new correlations based on findings from Milestones A&B [*Est. Summer22*];
2. Task – Amend ML training model with data acquired on new DSRDs (as characterized by Sections 5.1–5.2) to investigate statistical correlation of diode performance [*Est. Summer22*];
3. Task – Work with TCAD simulation team to address discrepancies between the DSRD performance obtained experimentally, and that achieved within simulations [*Est. Summer22*];
4. Task – Collaborate with DSRD manufacturing team to address discrepancies between the DSRD characteristics evaluated experimentally, and that desired by manufacturing process [*Est. Summer22*];

5. Task – Investigate relationships between statistical significance of individual diode KPIs to the peak performance of the IES pulser with the pulse generator team. [*Est. Summer22*];
6. Task – Incorporate findings from Tasks 1–5 into ML model, pinpoint KPI correlations of interest, and provide recommendations to IES sub-teams accordingly [*Est. Summer22*];

(D) Milestone – DSRD diode network evaluation [*on hold until Milestone C is completed*].

1. Task – Augment DOE network to streamline diode evaluation and identify checkpoints/gaps within simulation, manufacturing, and circuit development process to ensure optimal diodes are selected and utilized to produce robust high-fidelity IES pulse generator prototypes [*Est. Fall22*].

5.3.3 *Progress Made Since Last Report*

(A.6) DSRD Standard Diode Testing

Rigorous Forward IV Testing and Breakdown Testing

Rigorous forward IV testing has been implemented to improve series resistance effects seen when using a taped in fixture. Series resistance effects have been controlled with a bolt in the DSRD clamp, and new measurement techniques (4-wire) have been incorporated to reduce series resistance effects. Forward IV measurements in the Tektronik 371 semiconductor analyzer are now better understood for their accuracy and repeatability. Breakdown testing in the 371 was performed showing 40% of diodes achieved higher breakdown voltage, which is important for selecting diodes to stack and test in the pulser for achieving maximum peak voltage.

Series Resistance from CV Testing

The results of the RX plots have shown that the impedance analyzer sample fixture has a very high series resistance (in the range of 10’s of ohms). A new sample fixture will be assembled within the next two weeks that is expected to show a significant reduction in contact resistances due to the application of a controllable contact force using a calibrated torque wrench.

5.3.4 *Technical Results*

(A.6) DSRD Standard Diode Testing

Rigorous Forward IV Testing and Breakdown Testing

The picoammeter setup (Keithley 6485 picoammeter and 2400 sourcemeter) has been used primarily for forward IV testing of DSRD and incorporated tape to hold the DSRD into electrical contact. However, for 1-stack Gen2 diodes especially the taped fixture was prone to high series resistance in the procedure. For this reason, a screw bolt to clamp the DSRD into the fixture was used instead (Figure 5.3.1). Additionally, new measuring instruments were employed: a Keithley 2450 sourcemeter and Tektronik 371 high power semiconductor analyzer. The 2450 can source and measure current and voltage, do 2- and 4-wire measurements, and can source up to 1 A of current which goes beyond the

20 mA measurement limit for the Keithley 6485 picoammeter. To reduce the effects of series resistance a 4-wire method is used to measure forward IV and the inverse slope of the linear region (series resistance or RS) and is a high-current, low resistance measurement with 1 mΩ accuracy.

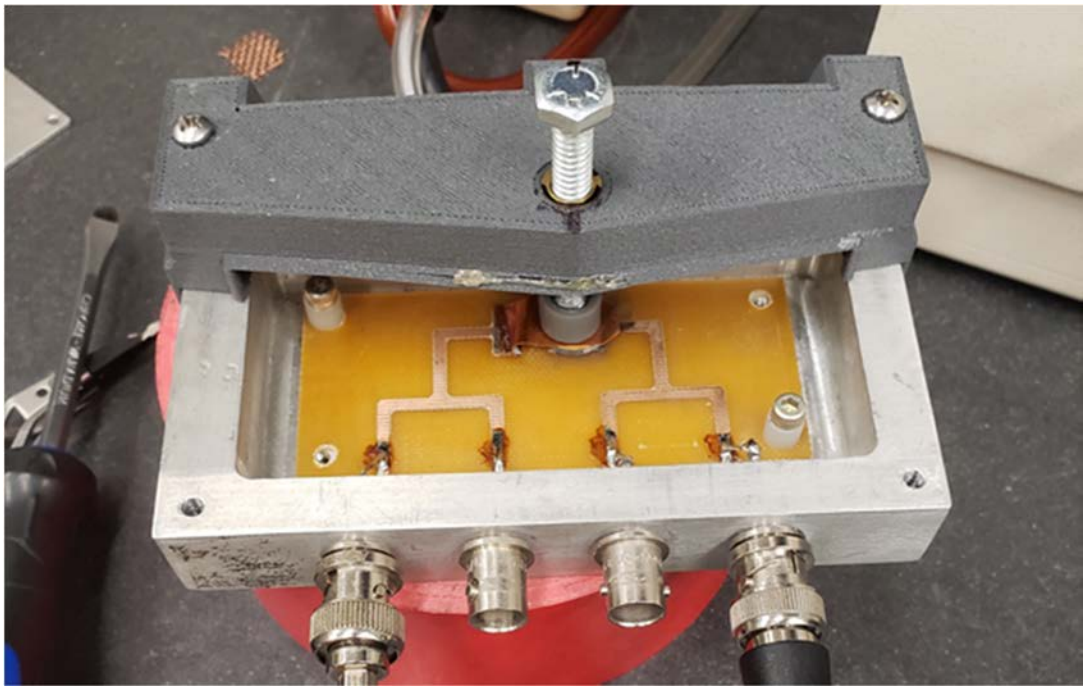

Figure 5.3.1. DSRD forward IV test fixture with screw bolt for DSRD clamping.

Modifications were done to the fixture to allow for higher torquing of the main screw bolt used for clamping the DSRD. The PCB was initially supported by standoffs but had no copper ground plane and was placed directly onto the bottom metal piece of the fixture to prevent warping of the PCB under the force of the clamping bolt. In Figure 5.3.2 is shown the results of a torque vs RS study for Gen2.1-d1-4. Some anomalies exist in the data likely due to the testing procedure used but the result shows generally that RS decreases with increased torque applied to the bolt with some leveling off of the effect. From the figure, 5 in*lb-force of applied torque is sufficient to lower the series resistance and has been employed for a future survey of the devices for RS using the 371. Higher torque was attempted (>10 in*lb), but this popped the heat insert screw sleeve for the main bolt, and the setup has been redesigned for higher torques by placing the insert from the bottom rather than the top. Future RS vs torque studies can determine if an optimal clamping torque exists. Our interest in pressed electrical contacts is with ease of device testing while maintaining low series resistance and repeatability.

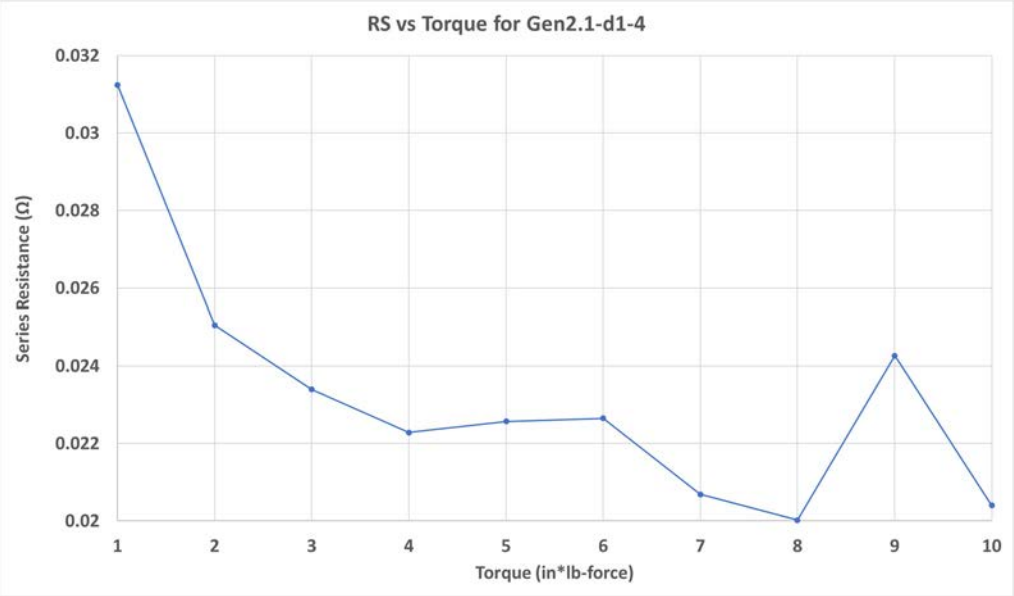

Figure 5.3.2. Series resistance vs torque in the 371 forward IV measurements of gen2.1-d1-4 devices.

Various modifications have been done to the forward IV fixture in testing. As mentioned, the clamping method was changed from tape to bolt. The endcap for the bolt used both a smaller more malleable endcap and a larger, harder material. Longer and shorter bolts were used based on whether the PCB is placed on standoffs or not. Cabling used to connect the fixture to test equipment was changed from BNC to alligator clipping with new shorter cabling on order. The PCB had to be replaced due to failure in breakdown testing. The top 3D-material printed piece of the fixture had to be replaced due to the inset hole warping from repeated attempts to repair the dislodged main bolt. The top copper foil contacting the DSRD was replaced with a thicker foil to prevent the rotating bolt head from shifting the DSRD. The testing methods were changed from 2- to 4-wire methods to reduce series resistance in the measurement. Also, two c-clamps have been used on either side of the main bolt to prevent the 3D-printed top piece from bowing significantly, which affects the measured screw position of the bolt and the DSRD clamping pressure. All these changes led to tracking their effect on new results and old results begin drawn into question as to their accuracy (for example the forward IV picoammeter results that had larger measurement variability were due to the series resistance added due to the procedure used to tape the DSRD into the fixture).

A series of ten measurements were done to determine the measurement variability or accuracy in repeated measurement. The measurements themselves were not initially performed for this purpose but to track how the forward IV changes due to the fixture setup. However, the results are still representative of the spread seen in a series of different forward IV measurements in the 371 of a DSRD. In Figure 5.3.3 is shown the averaged forward IV and the standard deviation from the ten measurements (the ten individual measurements are not shown). The standard deviation increases as the current and voltage level increase suggesting greater inaccuracy with increasing

current/voltage level. However in the figure inset, the coefficient of variance (standard deviation divided by mean) shows a sharp increase below 5 volts or approximately 1 A (1 A is the accuracy of the 371 measurement) which suggests the measurements are not accurate below 1 A and 5 V (consistent with not being fittable in SPICE). The STD is 2.5 A at maximum voltage and current. Not shown but forward IV for Gen2 appeared to undergo forward breakdown at sufficient voltage and current.

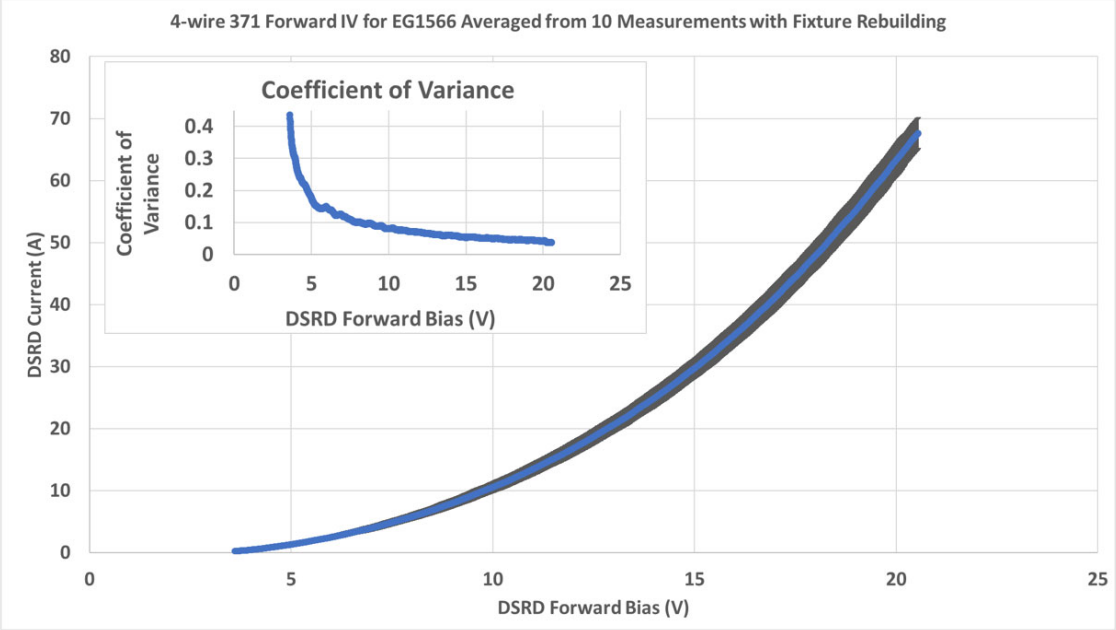

Figure 5.3.3. Averaged forward IV 371 measurement of EG1566 with standard deviation for error bars and coefficient of variance vs voltage in inset.

The 371 semiconductor analyzer allows for reverse breakdown testing using rectified sine-squared sinewaves which reduces heating. The 371 can test reverse bias up to 3100 V. Both Gen2 and EG-series DSRD were tested for breakdown. There are both theoretical and practicing definitions of the breakdown voltage. The breakdown voltage is the voltage for which a small increase in voltage produces a large significant exponential increase in current. However, in practice this definition is hard to implement and a breakdown current is usually defined based on the application. Previous pass-fail breakdown tests have used 1 mA breakdown current limit to avoid overheating and to have an easy definition to collect data from. In Figure 5.3.4 are shown the compiled breakdown voltage results for EG-series DSRD. 21 diodes were tested and 8 are close to 3000 V breakdown with 5 testing up to 3100 V with low current which may have higher breakdown limits than can be tested in the 371 (but pass as high voltage holding diodes). Ultimately pulser testing is the application by which the breakdown current can be set. The breakdown effects of pulse peaking and impatt-style oscillations can be observed in pulser testing to occur at certain peak voltages for particular diodes and can then be used to select a breakdown current in static breakdown tests that give the correct breakdown voltage seen in pulser tests. This is essentially comparing the breakdown results in static and DSRD pulser breakdown tests to determine the static breakdown tests predictability

for pulser performance. Breakdown data will also be analyzed in terms of rapid increase of current. Gen2 breakdown results showed a similar distribution to EG-series but for the Gen2 1-stack the breakdown voltages were as high as 600 V with a 1 mA definition for the breakdown current.

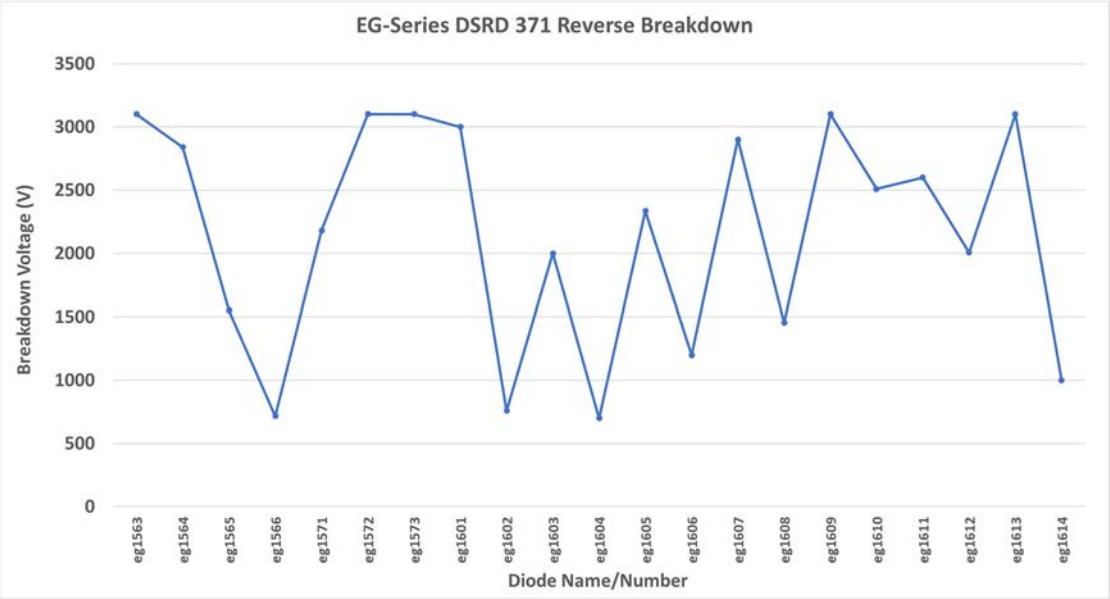

Figure 5.3.4. Compiled breakdown voltages of EG-series DSRD tested in 371 using the 1 mA breakdown current definition.

Series Resistance from CV Testing

Variation due to sample fixture continues to impact current-voltage measurements, thus hindering the (equivalent) series resistance measurement of the DSRDs. Several alternatives are under investigation for repeatability and measurement accuracy. One option that is under review is the use of an impedance analyzer (as opposed to an ammeter) to calculate the series resistance through a resistance-reactance measurement.

Resistance is analogous to friction against current and is present in all conductors. An AC signal that goes through a resistor will produce an in-phase shift with the current. Reactance, in comparison, is like inertia and works towards maintaining the state of the current. An AC signal that goes through a reactance (e.g., capacitor, inductor) produces a voltage drop 90º out of phase with the current. A resistance-reactance (RX) Nyquist plot can be used to better understand the equivalent series resistances of the DSRDs, which is currently the limiting factor for the pulser circuit performance.

As seen in Figure 5.3.6, an equivalent circuit of a DSRD contains both a capacitor and a resistor. A typical RX plot should appear as a semi-circle (see Figure 5.3.5). The equivalent circuit is not yet an ideal fit to the RX plot, but a new fixture may reduce the contact resistances that are not properly accounted for in the fit. This is an active area of

investigation and will be used as a comparison technique to the 371 curve tracing technique for measuring series resistances.

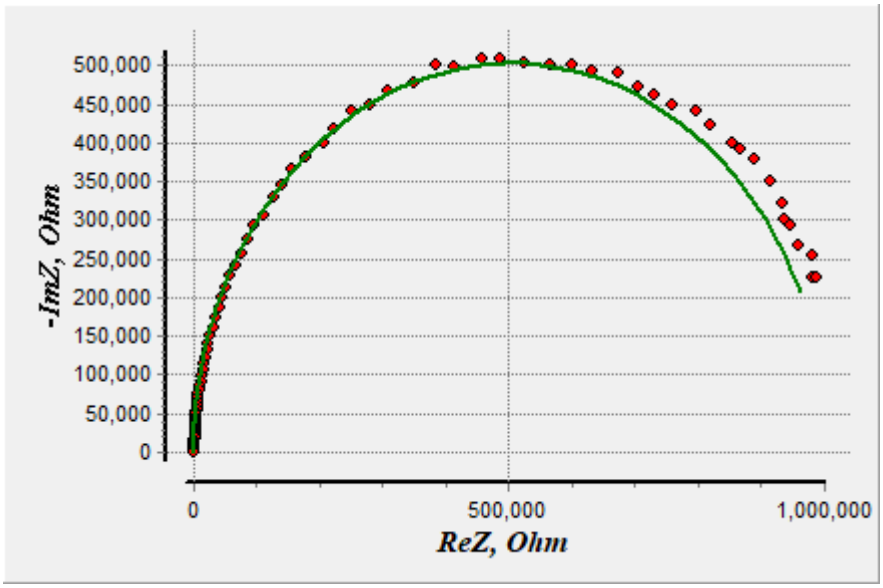

Figure 5.3.5. Resistance-Reactance (RX) plot of EG1605 diode at 0.5 V (red data points) with equivalent circuit of a DSRD fit (green line).

Figure 5.3.6. Equivalent circuit of DSRD as plotted in Figure 5.3.5.

An SOP for the 371 curve tracer has been developed. Unfortunately, the data collection process is tedious since it has a bubble memory, an obsolete non-volatile computer memory technology, requiring the user to toggle along each data point while writing the numbers down by hand. A group of different types of diodes is currently being tested and evaluated using this procedure.

5.3.5 *Summary of Significant Findings and Mission Impact*

(A.1) Several KPIs have been identified that tie the experimental diode test results to SPICE model simulation parameters. The first KPI is the forward current-voltage (the voltage reading at 10 mA) that is linked to the following SPICE parameters: saturation current, ohmic resistance, emission coefficient, and the forward knee voltage. From the impedance analyzer, the capacitance-voltage measurement is tied to the zero bias junction capacitance and the bottom junction grading coefficient. Both the forward voltage-current and the capacitance-voltage KPIs can be further tied to the SPICE simulation circuit peak voltage performance. The

reverse current-voltage (current at -200 V) is linked to the breakdown voltage SPICE parameter. The reverse recovery time measurements, such as the charge storage time and the transition time, are tied to the transit time SPICE parameter and to the full width at half maximum of the pulse signal. Several of these KPIs are not yet associated with specific circuit performances but will require further analysis as outlined in B.4.

(A.2) A preliminary DOE has been developed. The first 6 out of 16 rounds are currently being processed per (A.6).

(A.6) It was found that the test fixture for the picoammeter was causing large variations in the current-voltage measurements due to inconsistent pressure application to the diode. The variation was significantly larger on the Gen2 diodes since they are approximately one-third the height of the 7-stack diodes. A new 3D printed fixture with the ability to apply consistent pressure is expected to drastically reduce the contact resistances and variability that have been introduced to the measurements. New forward IV measurements have produced an averaged measurement with standard deviation error bars. Breakdown testing has shown ~40% of diodes hold at least 500 V per diode in stack. CV testing for series resistance has shown high series resistance associated with the CV test fixture and CV testing in the forward IV fixture may show lower series resistance.

(B.1) In A.6, it was discovered that the test fixture was the cause of significant variation within the test results, particularly with the Gen2 diodes. Several diodes are scheduled for repeat measurements to determine if all diodes need to be re-tested, which would affect the “completed” status of this milestone.

5.3.6 *References*

[1] Benda, H., & Spenke, E. (1967). Reverse recovery processes in silicon power rectifiers. Proceedings of the IEEE, 55(8), 1331-1354.

[2] Kozlov, V. A., Smirnova, I. A., Moryakova, S. A., & Kardo-Sysoev, A. F. (2002, June). New generation of drift step recovery diodes (DSRD) for subnanosecond switching and high repetition rate operation. In Conference Record of the Twenty-Fifth International Power Modulator Symposium, 2002 and 2002 High-Voltage Workshop. (pp. 441-444). IEEE.

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[5] Foll, H. (n.d.). *Reverse Recovery Time of Junction Diodes*. Retrieved from Semiconductors:https://www.tf.unikiel.de/matwis/amat/semi_en/kap_8/advanced/t8_1_1.html

5.4 DSRD-Based Pulsed Power Source Systematic Topological Optimization

(Islam Sarwar & Gyanendra Bhattarai)

5.4.1 *Problem Statement, Approach, and Context*

***Primary Problem*:** Inductive energy storage (IES) and release pulse generators that use drift-step recovery diodes (DSRDs) can be used as the fundamental units of all-solid-state high-power microwave (HPM) systems. The output from DSRD-based pulsers can then be fed into sub-nanosecond pulse sharpeners to achieve ultra-short high-voltage pulses. While DSRD-based pulsers can theoretically achieve the targeted 1's of GW in 1's of ns, their circuits are not topologically optimized to achieve high voltage gain (peak pulse voltage/prime source voltage), thus requiring large and heavy high-voltage (multiple kV) prime power supplies to achieve the required 100's of kV pulses. They also necessitate liquid-based cooling systems to dissipate the excess heat they generate during operation, further adding weight and rendering them impractical for Navy afloat missions.

***Solution Space*:** Systematically develop optimum circuit topology to maximize the voltage gain, and thus the peak voltage, peak power, and volumetric power density of DSRD-based HPM systems. Minimize the heat loss to be able to air cool by increasing energy efficiency through optimization of circuit elements without sacrificing the desired nanosecond risetime of the pulses generated. Air-cooled IES pulse generators using optimum DSRD stacking can remove the need for photo-triggered switches and their laser sub-systems. They are ideal for triggering sub-nanosecond rise-time sharpeners (SAS, D-NLTL, etc.), reducing overall cost, volume, and weight.

***Sub-Problem*:** DSRDs are not domestically available COTs components, but rather manufactured in small-batch quantities, with statistically significant variations in their performance parameters. In addition, our current SPICE models of these diodes may not be accurate due to unknown device parameters such as carrier distribution, carrier lifetime and the limiting current that we can pump without affecting the diode recovery property (see section 5.1 and 5.3) during high-voltage transients. These issues may lead to an inaccurate simulation model of the pulser and discrepancies between simulated and experimental results.

***State-of-the-Art (SOTA)*:** Air-cooled DSRD-based pulsers (equivalent in size to the pulse generators developed for this effort, i.e., ~0.01-m^3, ~2-kg) can achieve <20 kV, 1–2 ns risetime, and <4 ns FWHM across a 50 Ω load with a PRF of <15 kHz in burst mode. Available literature on IES pulse generators only describes a few circuit configurations, and there is a lack of comprehensive investigation of circuit topologies and optimization to achieve maximum gain and efficiency and reduce thermal load. Additionally, these pulsers are expensive and are not available within the United States.

***Solution Proposed*:** Develop different DSRD circuit topologies implementing series and parallel combinations of DSRDs (to increase reverse breakdown voltage and diode current, respectively) to minimize circuit components, such as inductors, capacitors, and switches. Systematically identify the best circuit topology and optimize the circuit components through physics-based DSRD pulser circuit theory and SPICE simulation to

maximize voltage gain and efficiency while minimizing the prime source voltage and thermal load.

Risks, Payoffs, and Challenges:

***Risks*:** All-solid-state DSRD-based IES pulsers require many other electronic components. Most importantly, the current pumping capability of available MOSFETs/electronic switches is limited, which may make maximizing the output voltage impossible even though the DSRDs are capable of higher current and output voltages.

***Payoffs*:** Being able to simulate and fabricate DSRD-based pulsers using physics-based pulser theory, partnered with US-based DSRD manufacturers, will enable a comprehensive domestic ability to optimize, produce, and evaluate these nanosecond pulsers.

***Challenges*:** Domestically manufactured (U.S.-based) DSRDs, which possess sub-optimal doping profiles, may lead to sub-optimal pulse generators. Accurate spice modeling of the diodes could be affected by expected wide variability in the diode characteristics or unavailability of advanced device characterization techniques. Determining the superlative ratio of design/development (through numerical analysis) to the effort put towards experimental testing/evaluation of the DSRD pulser is challenging due to the novelty of the approach. Extending the theory of single (1×1) pulse generator to cascaded (M×N) generator to increase the output will be very complex and may require significant time and computing power.

5.4.2 Tasks and Milestones / Timeline / Status

(A) Milestone – Develop theory of DSRD pulse generator to facilitate optimization of 1×1 pulse generator [***Completed JAN22***]

(B) Milestone – Extend the theory developed in Milestone A to facilitate optimization of M×N pulse generator [**JAN–MAY22** / ***Ongoing***].

(C) Milestone – Construct/demonstrate a DSRD-based 1x1 pulse generator prototype based on theory developed in milestone (A) and obtain performance data for multiple combinations of diode stacks [**JAN–JUN22 / *Ongoing***].

(D) Milestone – Construct/demonstrate a DSRD-based 4×2 IES pulse generator prototype capable of producing $\geq$12 kV peak voltage, $\leq$1 ns risetime, $\leq$5 ns FWHM, $\geq$3 MW peak-power, $\geq$100 kHz PRF, $\geq$1,000 shots-per-burst, $\geq$500 number of bursts [*On hold*].

(E) Milestone – Develop waveform inverter which, when combined with the pulser from Milestone C, enables a balanced differential waveform output with >90% inverted signal fidelity. [***Completed DEC21***].

(F) Milestone – Construct/demonstrate a M×N pulse generator prototype capable of producing $\geq$20 kV peak voltage, $\leq$1 ns risetime, $\leq$2 ns FWHM, $\geq$8 MW peak-power, $\geq$100 kHz PRF, and $\geq 2\sigma_{Vpeak}$, which operates in continuous-burst mode as a viable candidate for OSPRES Contract source alternative [*on hold until Milestones B, D, & E are completed*].

5.4.3 *Progress Made Since Last Report*

(B) Theory development of a 1×2 DSRD pulser is underway. The complete status of the theory development will be presented in the next reporting period.

(C) A modular driver circuit for optimized MOSFET operation is designed and simulated which is capable of driving four parallel MOSFETs to increase forward pumping current through the diodes. The new driver circuit with TOTEM pole configuration needs specific bipolar junction transistors which have been ordered from the United Kingdom due to their unavailability in the US.

5.4.4 *Technical Results*

(B) 1×2 DSRD pulser theory development

The idea of stacking and cascading pulsers is to use the output pulse obtained from the first pulser (first stage) to reverse bias the second stage. The requirement of stacking comes from the limitations in the MOSFET short-circuit current and open-circuit voltage. If the MOSFET (or any other fast opening switch) did not have a current or voltage limitation, a very high output voltage pulse could be achieved with a single stage pulser. In the stacking scheme, the first stage DSRD pulser can be connected to the second stage using either an AC or DC coupling via an impedance transfer network. In the case of an AC coupling, the second stage needs a separate MOSFET for the forward pumping cycle as shown in Figure 5.4.1. Instead, if DC coupling is used, the MOSFET of the first stage needs to provide the forward pumping current to the second stage, bringing the original issue of MOSFET current limitation.

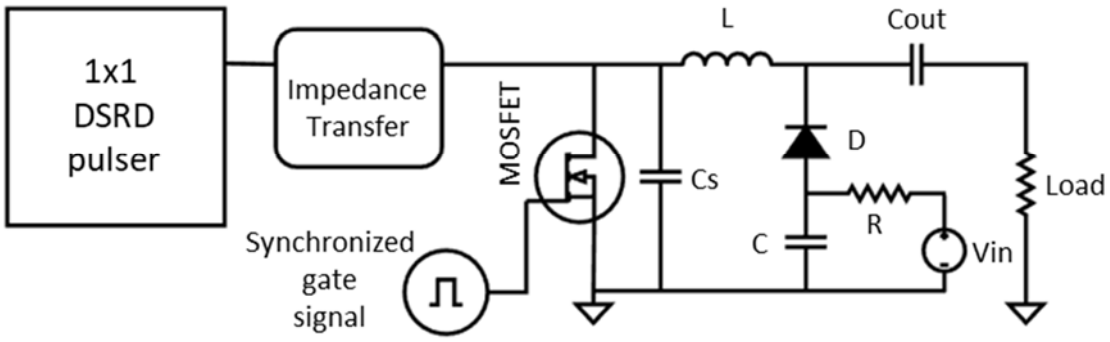


Figure 5.4.1. 1×2 stacked DSRD pulser using AC coupling between first and second stages.

Working Principle: Before the first stage of the DSRD pulser produces the output voltage pulse, the MOSFET gets a gate signal at an appropriate time, which enables the capacitor C to discharge through the diode D and inductor L, setting up a forward pumping current. Just before the first stage DSRD pulser produces a high voltage pulse, the MOSFET is turned off. Once the first stage produces the output voltage pulse, it is transferred to the

second stage and reverse biases the diode through the inductor L and sets up a large reverse current through the diode. After a certain time, the diode snaps OFF (reverse recovery) causing a sharp decrease in the diode current which induces a very high voltage pulse ($V_{out} = L\,(dI/dt)$ across the load.

Outstanding Questions:

a. The first complication comes from the voltage limitation of the MOSFET itself. We have demonstrated 1×1 DSRD pulsers producing up to ~8 kV pulses in which the MOSFET voltage has been measured up to 1.2 kV. This measured voltage is already the open circuit voltage limit for the MOSFET we have been using. As the output voltage of the first stage DSRD pulser is an order of magnitude higher, the second stage MOSFET eventually burns out due to the higher voltage. Thus, the stacking becomes unsuccessful.
b. The first stage DSRD pulsers are optimized for a 50 Ω load. When the first stage is connected to the second stage, the load is removed, and an impedance transfer network is added in between. However, the requirements of the impedance transfer network are stringent due to the very high voltage pulse with risetime of a couple of ns (~1 GHz frequency), which may not be entirely possible. One possibility in this case is to connect the first stage to the second stage via a capacitor only while optimizing the second stage to have an input impedance equal to 50 Ω. This requires a specific set of circuit elements (for example Cs, L, and C in Figure 5.4.1) which may not match with the values required for the expected output from the second stage. However, even with this approach, a separate MOSFET is required for second stage which then brings the problem discussed above in (a).

With these outstanding questions, it is not yet clear whether the stacking of pulsers produces very high voltage pulses compared to that of the 1×1 pulser. We have started doing simulations of the stacked pulsers with different options discussed above. A detailed explanation and the status of pulser stacking will be presented in coming reports.

5.4.5 *Summary of Significant Findings and Mission Impact*

(A) A systematic optimization of a 1×1 pulse generator based on the theory covered in the DEC2021 MSR reporting period was presented. In this reporting period, we have presented an optimization sequence considering the circuit limitations. Based on the previous measurements and simulations, we hypothesized that the lowered output voltage obtained from the previous pulsers could be due to higher diode ON-state series resistance than the value considered for simulation. A proposed working principle for a two-stage DSRD pulser has been described, however, with certain outstanding questions that may inform the efficacy of multi-stage DSRD pulsers.

(B) Using the 28-stack pulser, maximum peak outputs of 6.7 and 7.5 kV are obtained for a trigger length of 700 ns using a prime source voltage of 120 and 170 V. This suggests that a high voltage gain can be achieved by implementing more powerful MOSFETs and/or MOSFET paralleling. Further, the reverse breakdown voltage of ~650 V per diode in the EG1600 series is estimated based on the DSRD pulser output using a single 7-stack diode. Measurement of circuit voltages at different nodes confirms the circuit performance matching the SPICE simulation. Obtained

lower output voltages indicates requirement of more accurate DSRD SPICE Model which takes account of forward diode series resistance, carrier distribution and recombination during high voltage transients.

Table 5.4.2. Comparison of DSRD-based IES Pulse Generator Performance.

KPM	Units	MIDE - V1 Previous	MIDE - V2 Previous	MIDE – V3 Current	Kesar *et al.* SOTA	MI-PPM0731 COTS
V_{supply}	V	225	180	120	300	160
T_{ON}	ns	100	340	700	?	200
V_{peak}	kV	5.59	**7.35**	**6.7**	5	6.3
Gain	V/V	24.8	**40.8**	**55.8**	16.7	39.4
$\tau_{rise,20\text{-}90\%}$	ns	1.2	1.1	3.1	1.96	0.12
dV/dτ	kV/ns	4.66	6.44	2.16	2.55	**52.50**
FWHM	ns	2	5.48	6.90	2.27	0.35
PW	ns	5	7	7	3.5	2.5
Z_{LOAD}	Ω	50	50	50	50	50
P_{peak}	MW	0.625	**1.080**	**0.905**	0.500	0.794
E_{pp}	mJ	0.125	0.154		0.143	0.318
PRF_{max}	kHz	100	100		100	15
Burst	shots	100	100	*N/A*	*N/A*	100
	%	100	100	*N/A*	*N/A*	100
SD_{Vpeak}	σ	> 2	**> 2**	*N/A*	*N/A*	*N/A*
	%	96.5	**97.8**	*N/A*	*N/A*	*N/A*

(C) Successful construction and operation of a 2×2 DSRD-based IES pulse generator prototype has been completed, which meets or exceeds the required key performance metrics. Shown in Table 5.4.2 are the previous and current pulse generator performance specifications in comparison to a similar 2×2 pulser developed by Kesar et al. [1] using DSRDs, and to that of a commercial off-the-shelf (COTS) DSRD pulser of similar space and weight developed by Megaimpulse (i.e., PPM-0731), which also uses DSRDs with silicon avalanche shapers (SAS) [2]. Although the Megaimpulse pulser utilizes a SAS with a <500 ps risetime (a threshold we do not intend to go below due to Commerce Controlled List limitations), it is interesting to compare the results of linear voltage gain and peak power of this system, to that of one that utilizes a SAS. The current permutation of the 2×2 DSRD-IES pulser developed by MIDE under the ONR OSPRES Grant is able to achieve a higher peak voltage and shorter risetime than DSRD-based pulsers reported in the literature of comparable space and weight as well as those commercially available. The ability to generate a linear voltage gain of 40.8 to produce over a Megawatt of peak power into a 50 Ω load while achieving a peak voltage output standard deviation

of 2σ when operating at a PRF of at least 100 kHz, brings this technology to the forefront of viable options to potentially support the Naval afloat mission.

(D) Discrepancies exist in the obtained pulser and device characterization data for different series combinations and different samples of 7-stack DSRDs, which may be attributed to the inconsistencies in their manufacturing process. Future work in the coming months include testing multiple stack diodes in pulser configurations with MOSFET paralleling using modular gate driver circuit to identify better diodes and increase the output voltage to >9 kV from the 1x1 pulser configuration. Future work also includes the design and testing of 2×2 or higher configuration DSRD-based pulsers using more combinations of series-connected as well as parallel-connected DSRD stacks.

5.4.6 *References*

[1] https://www.onsemi.com/pdf/datasheet/nvh4l020n120sc1-d.pdf

[2] https://cms.wolfspeed.com/app/uploads/2020/12/C2M0045170P.pdf

5.5 All-Solid-State Sub-ns MW Pulse Generators with Semiconductor Sharpeners

(Gyanendra Bhattarai)

This sub-project is currently on hold as focus is directed toward Section 5.4. Please review the January 2022 MSR for the most recent project overview and status.

6 Thermal Management

6.1 Ultra-Compact Integrated Cooling System Development

(Sam Sisk, Roy Allen, and Sarvenaz Sobhansarbandi)

6.1.1 *Problem Statement, Approach, and Context*

Primary Problem: A thermal management system (TMS) is required for cooling semiconductor-based pulse-power devices, using anywhere from 50 to 200 W, with the goal of maintaining the semiconductor device temperature below 80 °C to avoid chip damage. The proposed system must increase cooling densities at a rate of at least 1 kW/cm^2, the current state of the art, while decreasing pumping power requirements, in-line with the SWaP-C^2 objective. This device also needs to be small enough to be used anywhere from server warehouses to drones, thus 1 cm^2 is targeted, with scaling up remaining a possibility.

Solution Space: To achieve such high cooling densities, we propose three potential solutions: an ultra-compact TMS (UC-TMS) to be directly integrated into the semiconductor, a monolithically integrated manifold microchannel chip (mMMC) TMS, and an updated jet impingement TMS (JI-TMS). The UC-TMS and JI-TMS are expected to achieve enhanced heat transfer rates due to the turbulent flow from the array of nozzles. The mMMC-TMS is expected to have low pressure losses while still transferring sufficient heat. The JI-TMS and UC-TMS are expected to have lower pressure losses if the outlet cross-sectional surface area for transfer fluid is equivalent to the inlet cross sectional area. The proposed TMS's are restricted to 1 cm^2 surface area, therefore, the required pumping power should be kept to a minimum. An array of micro-sized jet nozzles will provide a turbulent flow onto a microchannel section directly on the semiconductor device.

Sub-Problem: The turbulency formed from the array of nozzles creates an extreme pressure loss from the large amount of jet nozzles (over 200) and a flow diameter of 100 microns. The pressure must be sustained to enable proper cooling and circulation processes.

State-of-the-Art (SOTA): Integrated chip cooling is being widely used to dramatically increase the operational power of high-voltage silicon-based power devices. However, the current SOTA devices include surface to surface contact points that rely on cohesive connections. These connections increase the amount of material through which heat must transfer to the coolant, thus limiting the heat removal rate.

Objective: To design, simulate, and compare three different TMSs (ultra-compact, monolithically integrated manifold microchannel chip, and jet impingement) under the same operating conditions, and optimize through an iterative process. The proposed UC-TMS and JI-TMS design are based on refining in-chip jet-impingement geometry through leveraging theory and a parametric evaluation of nozzle geometry, flow channel arrangements, and outlet to inlet area ratios. The mMMC TMS performance will be compared with the corresponding results available in the literature and with the results from the other two designs.

Challenges: The manufacturing techniques needed for integrated chip cooling systems have not been entirely adopted. The proposed compact designs are restricted due to the low tolerances needed for the geometries of the nozzles and heating plate; the manufacturing process must be capable of layering the silicon TMS onto the semiconductor.

Risks: With a system so compact, the pressure drop could be a large issue regarding the objective heat dissipation rate. An extreme pressure drop would potentially cause the coolant to flow backwards, causing less fluid-to-solid interaction.

6.1.2 *Tasks and Milestones / Timeline / Status*

(A) Design a Si base 1 cm^2 UC-TMS, JI-TMS, and mMMC-TMS to achieve a heat dissipation rate of 1 kW/cm^2. The device will also need to be designed in a way where it can be manufactured as proposed. / MAR22–MAY22 / In Progress

(B) Using the computational fluid dynamics (CFD) ANSYS software, simulate the results for the UC-TMS, JI-TMS, and mMMC-TMS all operating under the same conditions. Compare the results and make improvements to the designs to meet the target metrics. This process will continue until an optimal design is chosen to move further with. / MAY22-JUN22 / In Progress

(C) Using the optimal design, perform ANSYS simulations using de-ionized water or Si-C nanofluid as the coolant and see how fluid type changes the effectiveness of the TMS. Other fluid types may be researched as pressure drop is a large factor. / June22–JULY22 / Upcoming

- Prove simulations from previous literature to show capable design configurations with acceptable pressure drop and steady temperature.

(D) With all problems addressed with simulation results and having a single design able to be manufactured, manufacture a prototype to begin experimental testing and evaluation / AUG22– OCT22 / Upcoming

6.1.3 *Progress Made Since Last Report*

(A) The focus for this month has been mainly on the two impinging jets designs. The mMMC-TMS design is still being considered but will be focused on in the coming weeks.

6.1.4 *Technical Results*

(A) Fundamental simulations took place for different variations of jet impingement designs. The different variations in these designs were nozzle diameter, nozzle shaft length, distance from the nozzle to the heated plate, distance for an array of nozzles from each other, and outlet area for heated fluid. These can be visualized from an illustration from Incropera in Figure 6.1.1. [1].

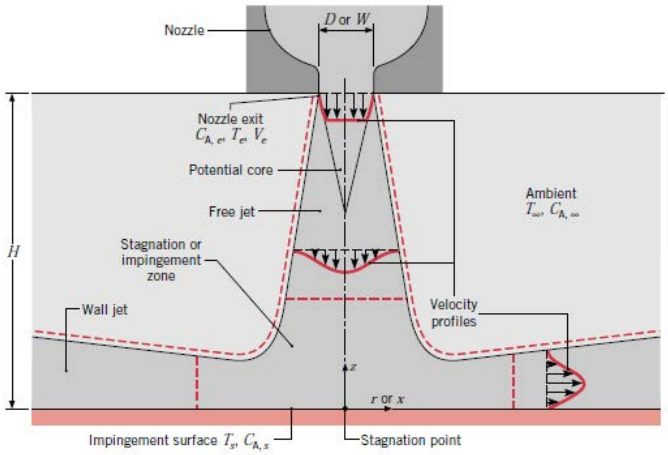


Fig 6.1.1. Middle cross section of impinging jet.

(B) The varied jet impingement designs are currently still being simulated using ANSYS and results are yet to be compared.

6.1.5 *Summary of Significant Findings and Mission Impact*

(A) We are in the process of refining our jet impingement system design based on literature review and preliminary simulations.

6.1.6 *References*

[1] Incropera, Frank P. Fundamentals of Heat and Mass Transfer. 7th ed. John Wiley, 2011.

7 Pulse-Forming Networks

7.1 Diode-Based Nonlinear Transmission Lines

(Nicholas Gardner)

Attention on this sub-project is being entirely directed toward the preparation of manuscripts and an associated dissertation. A summary report will be provided in Summer 2022, and this will serve as a placeholder until this time. Please see the January 2022 MSR for the most recent summary and status and the Outputs section for papers in preparation or published.

7.2 Continuous Wave Diode-NLTL based Comb Generator

(Nicholas Gardner and John Bhamidipati)

7.2.1 *Problem Statement, Approach, and Context*

Primary Problem: When used as a pulse shaping network (PSN), diode-based nonlinear transmission lines (D-NLTLs) are promising solutions towards reducing the size, weight, and cost of RF and microwave sources on Navy afloat missions. However, in pulsed-mode, the impedance of D-NLTLs changes significantly, leading to signal/power reflection, standing wave generation, and return power losses at both the source–line and line–load interfaces, leading to difficulties in practical D-NLTL applications.

Solution Space: Use a D-NLTL to work as comb generator (capable of producing multiple harmonics of the input signal) by converting continuous wave (CW) signals from low frequency–very high frequency (LF–VHF) bands (0.03 MHz–30 MHz) to the ultra-high frequency (UHF) band (0.3–3 GHz) at ones-of-MW peak power. Such an application with reduced dependence on transient changes will decrease impedance mismatch effects at the source–line and line–load interfaces by continuously oscillating D-NLTL peak impedance between the same two values. Use of MW D-NLTLs in the comb generator will push output frequency up to ranges required for Navy afloat missions.

Sub-Problem: Design parameters for COTS high-frequency D-NLTL based comb generators capable of generating up to ~50 GHz output frequencies are limited to <1 Watt output powers, which is <0.1% of the power handling capability required for navy afloat missions. Using the metrics associated with low power comb generators alone to design D-NLTLs capable of generating ~1–2 GHz frequency with capability to handle MW-order peak powers could potentially introduce design errors resulting in frequency/power prediction–measurement discrepancies on the order of a few hundred MHz.

State-of-the-Art (SOTA): Commercial-off-the-shelf (COTS) GaAs varactor diode-based monolithic microwave integrated circuit (MMIC) D-NLTL comb generators are capable of operating at input and output frequencies up to 600 MHz and 30 GHz, respectively. However, these comb generators are not capable of handling powers higher than 27 dBm (0.51 W). In-house pulsed D-NLTL prototypes have been shown to generate center frequencies of 0.2–0.5 GHz at kV amplitudes (~0.5–0.7 MW peak power) in a light-weight small-footprint circuit. Further D-NLTL network efficiency is hindered by a signal-

dependent impedance characteristic to the network leaving reported efficiencies of RF content generation at 10% or less of incident pulse energy.

Objective 1: Design and demonstrate a high voltage D-NLTL based comb generator capable of L-Band Frequency generation and 0.1–5 MW power generation.

Objective 2: Increase D-NLTL network efficiency above the reported 10% threshold through use of CW sources suppressing impedance mismatch effects presented by the signal-dependent impedance characteristic of D-NLTLs.

Anticipated Outcome(s): A successful demonstration of improvements to impedance matching at the source–line interface using a CW signal measured as a reduction in signal amplitude loss between the source and D-NLTL.

Challenges: Nonlinear signal-dependent behavior provided by a reverse bias diode produces difficulties in predicting generated waveform behavior. Further D-NLTL performance is limited in both frequency and power generation by the availability and variety of COTS Schottky and epoxy diodes.

Risks: The reverse bias hold off potential (V_R) of a chosen diode limits the power generation capabilities of the system. If an excitation is used that exceeds V_R, diodes risk being damaged. Further reflections produced at the source–line interface caused by a signal dependent impedance can damage a CW source sensitive to such reflections.

7.2.2 *Tasks and Milestones / Timeline / Status*

(A) Demonstrate an ability of a CW excitation signal to reduce the source–line impedance mismatch effect on signal amplitude present in D-NLTLs when compared to a pulsed mode operation, first through simulations and then by validating the results experimentally using low voltage (LV) and high voltage (HV) prototypes.

(A1) Show the potential to improve source–line impedance mismatch in simulation (Completed SEP21)

(A2) Experimentally demonstrate a low voltage (LV) prototype receiving a CW input (Completed SEP21)

(A3) Compare measured results with simulation behavior; comparison of results will be used to further refine D-NLTL simulation techniques (Ongoing)

(A4) Determine if there are improvements to system behavior if D-NLTL diodes are biased when receiving a CW input (Ongoing)

(A5) Demonstrate improvements to the source–line impedance mismatch in a LV prototype (Ongoing)

(A6) Demonstrate a HV prototype receiving a CW input (Completed NOV21)

(B) Demonstrate UHF – L-band (0.3–2 GHz frequency) generation with a CW D-NLTL.

(B1) Excitation of K100F and K50F D-NLTLs using a 700 MHz signal from the R&S amplifier (Completed NOV21)

(B2) Demonstrate frequency comb generation in K50F D-NLTL using continuous wave VHF excitation (Completed APR22)

(B3) Perform simulation- and experimental studies to measure center frequencies and peak voltage output as a function of source–line and line–load impedances (Completed APR22)

(B3) Simulate topologies capable of utilizing a bipolar pulse for CW applications (**Ongoing**)

(C) Demonstrate UHF generation at single MW power levels with a CW D-NLTL.

7.2.3 *Progress Made Since Last Report*

Work on this sub-project was put on hold for this month to focus on 7.3 and other reporting/dissemination efforts.

7.2.4 *Summary of Significant Findings and Mission Impact*

(A) In the month of September 2021, a LV prototype was given several continuous waveforms to observe initial behavior of a D-NLTL with a CW source. The LV D-NLTL demonstrated a capability to receive a CW based source. No effect on the source–line impedance mismatch was observed for the LV tests. During the month of November 2021, two high-voltage D-NLTLs based on epoxy diodes were tested using a sinusoidal waveform amplified by an R&S amplifier. Each D-NLTL demonstrated a capability to function with a CW source, however little to no effect was observed on the source–line impedance mismatch.

(B) High voltage D-NLTL based on epoxy diodes of model K50F equipped with 50 Ωn-type connectors on source and load ends was tested with sinusoidal excitation with frequencies 20 MHz–100 MHz. Test was performed using ‘ENI 3200 L’ RF amplifier with upto 200 W input power. Output frequencies upto 0.3 GHz were generated with < 100 MHz excitation. While soliton generation was noticed below 100 MHz excitation with ~25% conversion efficiency, a shift in NLTL operation from soliton generation to pulse sharpening (frequency doubling) was noticed. However, a decrease in number of frequency bands was noticed with an increase in excitation frequency. When V_{peak} and f_c were studied computationally as a function of source and load impedances, a highest V_{peak} and f_c were noticed when a combination of 10 Ω and 50 Ω were used at source and load, respectively, while the lowest was noticed with 50 Ω at both the ends. Designing a 50 Ω to 10 Ω impedance transformer to interface the n-type connectors with the NLTL could potentially reduce the impedance mismatch at the load.

7.3 Dynamically Tunable Multi-Frequency Solid-State Frozen Wave Generator

(John Bhamidipati)

Please see the Appendix for a summary report of this sub-project.

7.4 Pulse-Compression-Based Signal Amplification

(Feyza Berber Halmen)

7.4.1 *Problem Statement, Approach, and Context*

Primary Problem: Solid-state amplifiers, such as gallium-nitride-based high electron mobility transistors (GaN HEMT), can be used as high power microwave (HPM) sources to achieve the SWAP-C2 performance metrics necessary to support the cUAV Naval afloat mission. However, even the best high-power GaN HEMTs are limited to 2–3 kW of peak power, much lower than the 0.1 to 3 MW pulsed power available from traditional HPM sources such as travelling wave tubes (TWTs). Achieving a power density of 1 W/cm^2 at a distance of 10 m with a high gain (≥ 10 dBi) narrow-band antenna requires an input power increase of two to three orders of magnitude. Power combination methods to achieve an effective radiated power (ERP) at MW scale require 10 s to 100 s of GaN HEMTs, compromising the SWAP-C2 performance.

Solution Space: Pulse compression techniques are used to increase the peak power and lessen the pulse width in HPM applications. Adapting pulse compression at the GaN HEMT or any other SWAP-C2 compatible source output can achieve sufficient ERP with an optimal radiating element.

***Sub-Problem*:** Pulse compression is generally used to generate a pulsed output with a high peak output power (P_{out_peak}) and a wideband frequency content from a DC input voltage. The main challenge lies in identifying a pulse compression technique that can be used to amplify a narrowband RF input signal. Some of the circuit elements for common pulse compression techniques, such as the saturable inductors used for energy storage in magnetic pulse compression (MPC), exhibit increasingly lossy behavior with high frequency. Another challenge will be to determine, if any, the operating frequency limits of the suitable pulse compression technique for high-frequency, high-power signals.

State-of-the-Art (SOTA): Large magnetic pulse compression (MPC) circuits (>1 m^3, >1000 lbs) have demonstrated peak output power up to a few GWs. Smaller versions (~0.125 m^3, 50 lbs to 100 lbs) can achieve 7.5 MW peak power [1].

Deficiency in the SOTA: Traditional MPC systems are large (few meters long), leverage huge transformers, and require liquid coolant such as transformer oil, which leads to undesirable system mass values of ≥1000 lbs. They are used for generating medium or high pulse power traditionally from DC or AC (50/60 Hz) high voltage supplies. There is no known example of high-frequency signal amplification utilizing MPC.

Solution Proposed: Developing a pulse compression circuit that will act as a high-power signal amplifier with a gain of ≥10. Utilizing magnetic pulse compression, or any other

suitable pulse compression method, for high power signal amplification with source fidelity.

Relevance to OSPRES Grant Objective: Pulse compression will enable a size and cost efficient solution to high power signal amplification that will lead to HPM source development with optimal SWaP-C2 parameters.

Risks, Payoffs, and Challenges:

Challenges: Modeling pulse compression circuits for high-frequency operation can present a challenge. Pulse compression circuits are generally evaluated in SPICE simulators with low frequency AC / transient simulations. SPICE is a lumped-element model simulator and cannot solve for the distributed-element model required at high frequencies where the wavelengths become comparable to the physical dimensions of the circuit. Some circuit components, such as the saturable inductor in the MPC, are not available in SPICE or many other simulators and need to be modeled using behavioral models and proprietary material data. Pulse compression circuit modeling, especially at high frequencies, needs to be investigated.

Risks: Pulse compression methods are usually lossy in nature and generate a considerable amount of heat; therefore, designing a proper cooling method must be carried out, which may inadvertently increase the volume (size and weight) of the overall design.

7.4.2 *Tasks and Milestones / Timeline / Status*

(A) Milestone – Demonstrate 2–3 times increase in peak power and compression gain using magnetic pulse compression (MPC) [*estimated completion by MAY22*].

1. Subtask – Model saturable inductors in LTSpice or Matlab/Simulink in order to be able to develop MPC simulations / NOV21 / Complete.
2. Subtask – Design MPC circuit with RF input and simulation in LTSpice or Matlab/Simulink to evaluate the resulting amplification and frequency content. / JUNE22.
3. Subtask – Model the high frequency behavior of MPC circuit / NOV21 / Ongoing.
4. Subtask – Build and test the MPC prototype using bench top power supply / OCT21–AUG22 / *Ongoing*.

(B) Milestone – Increase the compression gain available from MPC.

(C) Milestone – Build and test SWAP-c2 compatible high-frequency MPC prototype with GaN source.

7.4.3 *Progress Made Since Last Report*

(A.3) The magnetic switch, which is the fundamental component of the magnetic pulse compression circuit, cannot be realized at frequencies higher than 300 MHz due to material limitations. A statement of work (SoW) has been drafted with KRI in order to develop high-frequency saturable inductor materials.

(A.4) The B-H curve tracer circuit was completed with the high voltage section isolated in an enclosure. Tests were conducted with available cores to verify accurate circuit operation.

7.4.4 *Technical Results*

(A.3) Magnetic pulse compression utilizes magnetic switches in order to compress the current and as a result provide compression gain. The basic mechanism enabling the inductor to act as a magnetic switch is the large change in relative permeability (μ_r) when the inductor core is saturated. Magnetic materials have high relative permeability, which drops to ~1 when they are saturated, resulting in a high or low impedance path depending on the saturation condition. The permeability of magnetic materials decreases with frequency, in accordance with Snoek's law. NiZn has the highest cutoff frequency among the magnetic core materials. However, the best commercially available NiZn core has a cutoff frequency of less than 350 MHz and μ_r of only 7.5 [2], which is not high enough to be employed as a 'low-loss switch'. MIDE has been collaborating with KRI in determining the available options for saturable magnetic materials at high frequencies. YIG and NiZn ferrite composite have been suggested as the most suitable materials for the high-frequency magnetic switch operation by KRI. A SoW has been drafted to address the design and fabrication of such a magnetic composite with cutoff frequency of over 500 MHz and relative permeability of 25. Target magnetic and dielectric loss tangents and dielectric constant, which will affect the compression gain of the MPC, have also been included in the SoW. A low saturation flux density, required for saturation at high frequencies for the given input voltage levels, will also be targeted in the new material development. A low-frequency prototype for continuous-wave input will be fabricated at MIDE as proof of concept before finalizing the SoW on high-frequency saturable magnetic materials.

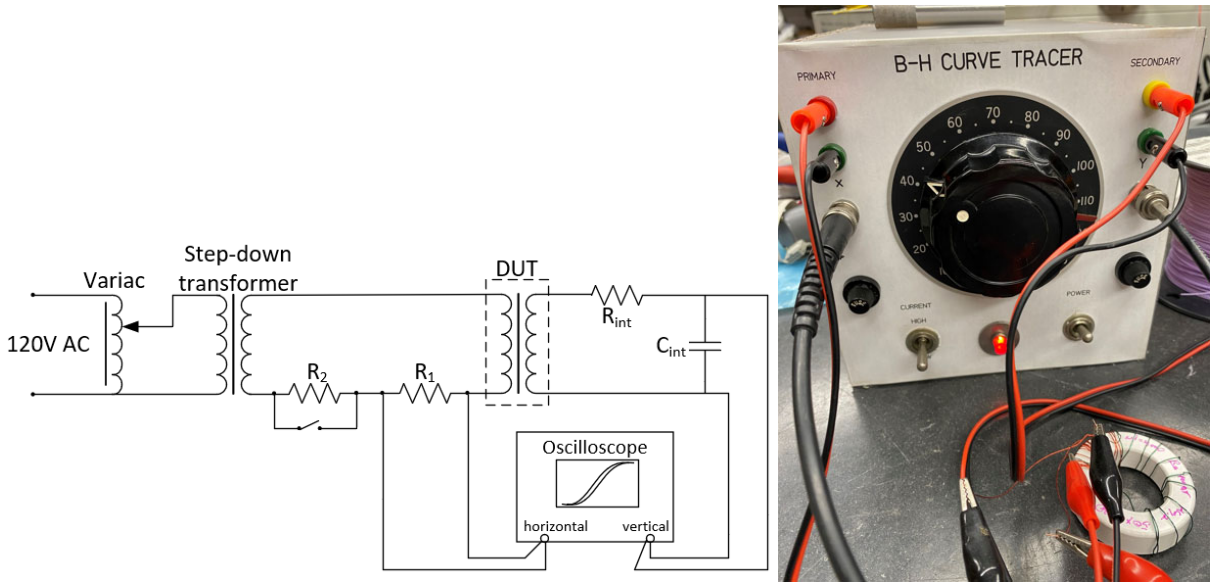
(A.4) The B-H curve tracer prototype circuit that was built last month was modified to isolate the high-voltage section with the variac and the step-down transformer in an enclosure, as depicted in Figure 7.4.1(b). A switchable input resistor R_2 of 20 Ω was added to the circuit to adjust the input current level to 'low' or 'high' for cores with different B_{sat} values. The circuit schematic is given in Figure 7.4.1 (a). In order to ensure that the DUT secondary is terminated by high enough impedance so that its current is negligible, and it does not alter the H-field established by the input current, R_{int} was replaced with a 200 kΩ resistor instead of 22 kΩ.

Next, the accuracy of the B-H curve tracer circuit was tested with available magnetic cores at MIDE. Magnetic field and flux density can be extracted from scope x-axis (current) and y-axis (voltage) data as explained in the previous MSR:

$$H \approx \frac{N_1}{l_e} I \tag{1}$$

$$B = \frac{R_{int} \cdot C_{int}}{N_2 \cdot A_e} V_{out} \tag{2}$$

B and H values calculated from the measurements were then compared with the datasheet values for verification.



(a) (b)

Figure 7.4.1. B-H curve tracer (a) schematic and (b) prototype

The measured and calculated B_{sat} and H_c values are tabulated in Table 7.4.1 for Kemet 700L [3], TDK H5C2 [4,5], and Metglas 2605S3A [6]. Two measurements are taken from the Kemet 700L magnetic core with different number of turns to check the consistency and measurement accuracy. B-H curve tracer operation could not be verified with these measurements. Measurements and analysis are ongoing to determine if the problem is with the B-H curve tracer circuit or the tested samples.

Table 7.4.1. Kemet NiZn material 700L toroid properties

							B_{sat} (mT)		H_c (A/m)	
Core	A_e (mm^2)	l_e(mm)	N1	N2	I (A)	V_{out} (mV)	Measured	Datasheet	Measured	Datasheet
700L	347.5	143.6	10	9	0.6	2	127.9	350	41.78	40
			10	20	0.5	5	143.9		34.82	
H5C2	129.5	125.7	12	24	0.05	5	321.7	400	4.77	7.2
2605S3A	213.75	260.8	10	10	0.2	5	468	1410	7.67	<8

7.4.5 *Summary of Significant Findings and Mission Impact*

(A) Initially a basic 2-stage magnetic pulse compression circuit was built and tested with DC input to better understand the MPC principles and considerations such as inductor sizing, pre-pulse currents and inductor saturation. Next, saturable inductor

modeling was realized in LTSpice with inductor flux expression and Chan model [2]. Prior to MPC system simulations, magnetic core losses were investigated, and core selection constraints were determined based on the core losses and high-frequency MPC design considerations. Next, different magnetic core materials were investigated to determine the most suitable candidate for high-frequency MPC. As reported previously, such a core should have high resistance, narrow hysteresis loop, minimized eddy current area, and low saturation flux density (B_{sat}). High permeability (μ) and very sharp saturation characteristics are also preferred in order to minimize pre-pulse currents and resulting MPC gain loss. NiZn ferrites are the best option among the commercially available magnetic cores for the high-frequency MPC application as they have the highest operating frequency, low B_{sat}, and sufficiently high μ. After investigating suitable magnetic cores and their properties, LTSpice simulations of the previously tested 2 stage MPC circuit were resumed using the Chan model for Kemet NiZn cores. The inductor for the input stage was replaced with a magnetic switch based on the simulation results. The effects of core coercivity and remanence on MPC operation, which is not included in the design equations, were simulated, and high remanence and low coercivity were found to result in the lowest leakage currents due to sharper saturation behavior. A prototype B-H curve tracer was also built in order to characterize the magnetic cores that will be used in the MPC circuit. The prototype is now complete with the high voltage section isolated in an enclosure. Measurement of known cores with the B-H curve tracer and analysis of the results are ongoing in order to verify the accuracy of the prototype. A SoW has been drafted with KRI for the design and fabrication of a NiZn-YIG magnetic composite with cutoff frequency of over 500 MHz and relative permeability of 25. Commercial magnetic cores offer the highest cutoff frequency of 350 MHz with relative permeability of only 7.5. New magnetic material development is needed to realize a magnetic switch at higher frequencies. A prototype MPC circuit with continuous-wave input at low frequencies will be fabricated for proof of concept before finalizing the KRI SoW.

7.4.6 *References*

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8 Antenna Development

8.1 Tradespace Analysis of an Array of Electrically Small Antennas (ESAs)

(Bidisha Barman and Deb Chatterjee)

8.1.1 *Problem Statement, Approach, and Context*

Primary Problem: Determine the extent to which the physical aperture size of an antenna array, composed of patch elements, can be reduced, while maintaining performance in peak power density, bandwidth, and electronic beam steerability over the UHF range (0.4–1 GHz), compared with present-art high-power-microwave-capable antenna arrays.

Solution Space: An array of patch antenna elements whose feed, two-dimensional shape, and relative placement (i.e., intra-, and inter-element design) allow for the physical aperture size to be reduced by more than 20% compared with the present-art.

Sub-Problem: To overcome scan blindness (as the main beam is electronically steered), due to the excitation of surface waves (SW). (Note: scan blindness is a common phenomenon in electrically small microstrip patch antenna arrays).

State-of-the-Art (SOTA): Horn, reflector, Vivaldi, valentine, etc. are some of the commonly used ultra-wideband (UWB) antenna elements in a phased array for high-power microwave (HPM) transmissions.

Deficiency in SOTA: Large physical aperture size of the antennas.

Solution Proposed: Using electrically small antennas (ESAs) as array elements and optimizing their performance in terms of both near-field (bandwidth) and far-field (directivity) parameters, followed by arrangement of the ESAs in suitable lattice structures (preferably, hexagonal/triangular) to reduce the overall array aperture area. Using stochastic and machine learning (ML) algorithms to optimize antenna element and array performance.

Relevance to OSPRES Grant Objective: Provides design and optimization guidelines for UWB ESA elements, especially coaxial probe-fed microstrip patch antennas, and arrays for HPM applications.

8.1.2 *Tasks and Milestones / Timeline / Status*

(A) Develop an Array Pattern Tool in the context of lightweight calculations of large antenna arrays / JAN–MAY 2021 / Completed MATLAB code.

(B) Investigate the effects of array aperture area reduction on different array parameters (such as gain, beamwidth, electronic beam steerability) and present a comparative study of antenna array parameters as a function of array aperture area / JAN–MAY 2021 / Completed.

(C) Build minimum viable validation prototypes of single ESA elements on substrates that have good power handling capabilities for HPM transmissions at UHF range (such as polyethylene, FR-4, TMM-10i, TMM-6) / JAN 2021–JUN 2022 / Ongoing manufacturing of a tapered coaxial connector fed wideband microstrip element.

(D) Optimization of ESA (single element) performance using ML based stochastic search algorithms / JUN 2021–FEB 2022 / Completed single objective optimization of ESA elements.

(E) Build minimum viable validation prototypes for arrays of ESA elements / JUN 2021–SEP 2022 / Prototyping of a 4×4 array to be initiated after the successful completion of (C).

(F) Optimization of array performance using ML algorithms / SEP 2021–FEB 2022 / Completed single objective optimization of antenna arrays on infinite ground planes.

8.1.3 *Progress Made Since Last Report*

(C) Build minimum viable validation prototypes of single ESA elements:

a. Prototyping of the tapered, coaxial, connector fed wideband, microstrip patch antenna, for operation in the 0.7–1.1 GHz range, is still underway.

b. Most of the challenges encountered while manufacturing the novel prototype have been addressed.

8.1.4 *Technical Results*

(C) Build minimum viable validation prototypes of single ESA elements:

The wideband (0.7–1.1 GHz), microstrip patch antenna element, fed by a tapered coaxial connector (as shown in Fig. 8.1.1(a)), is currently being manufactured. Prototyping of this relatively new design took longer than the expected lead time of 2 weeks, due to several challenges encountered during the process. Some of the challenges include but are not limited to: (a) difficulties to CNC lathe the inner conductor of the tapered coax, (b) limitation in the printing capacity of the SLA printer, and (c) electromagnetic discontinuities at the junctions of different attachments, etc.

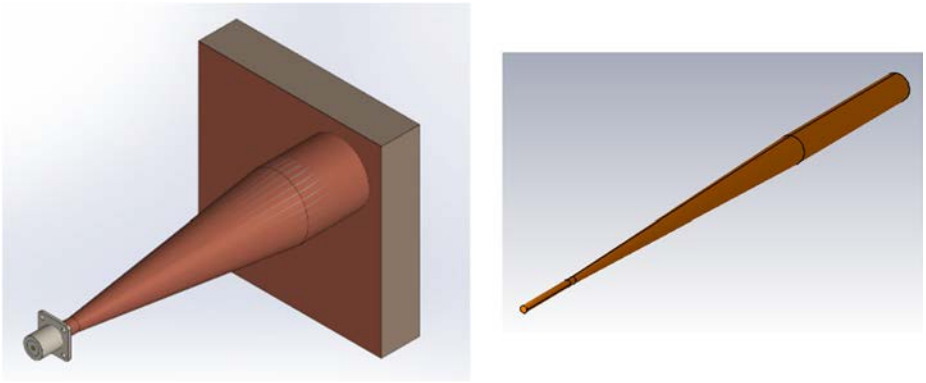


Figure 8.1.1. CST simulation model of the (a) wideband, microstrip patch antenna, fed by the tapered coaxial connector, on a PEC-backed, square shaped ($6" \times 6"$), polyethylene substrate, and (b) inner conductor of the tapered coaxial connector.

The methods used to manufacture the prototype and tackle the challenges are detailed below:

1. The inner conductor, of the tapered coaxial connector, being a solid, tapered, metallic cylinder (Fig. 8.1.1(b)), was difficult to lathe accurately using the CNC lathe machine. Therefore, it was SLA printed and coated entirely with silver paint, while maintaining the skin depth.

2. To maintain continuum in the structure, initially it was decided to 3D print the dielectric substrate and the insulating layer of the tapered connector as a single block. However, due to limited capacity of the SLA printer, only the tapered section could be printed at once, while the dielectric substrate was cut out of a polyethylene panel. Both polyethylene and SLA have similar dielectric constants ($\varepsilon_r \approx 2.3$), and hence, are expected to retain the antenna properties.

3. The inner conductor was fitted in the hollow insulating (SLA) layer of the connector. The narrower end of the conductor was attached to a commercial N-type connector.

4. The entire tapered connector was then attached to the polyethylene substrate panel with UV cured PMMA glue/cement. This attachment was tricky as the glue refused to stick to the polyethylene block.

5. The final stage is metallization of the entire tapered section (forming the outer conductor of a coax), back of the polyethylene panel (that works as the ground plane), and the radiating patch. Silver paint has been used to metallize the tapered connector, as using copper tape may result in uneven surfaces. However, for the ground plane and patch, copper plates have been used.

Fig. 8.1.2. shows the latest prototype, before and after metallization. The prototype is expected to be ready for testing within a week, and the test results will be furnished in the next MSR.

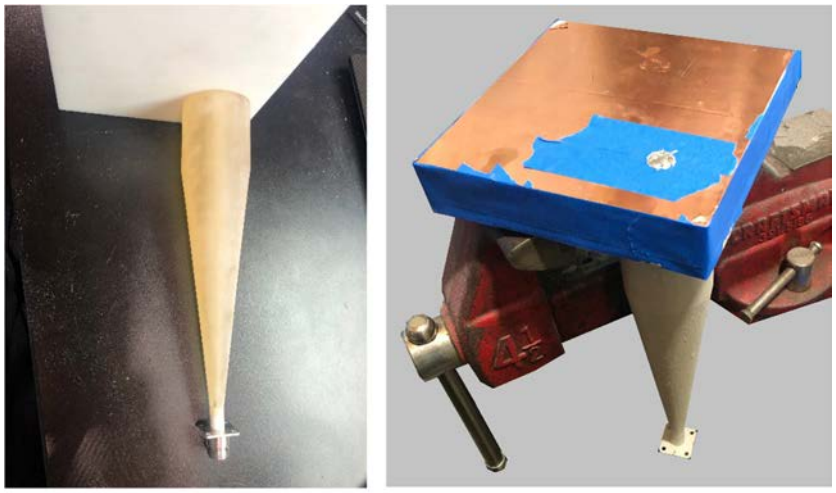


Figure 8.1.2. The tapered coaxial connector integrated with the polyethylene substrate (a) before and (b) after metallization. The patch is yet to be cut out.

8.1.5 *Summary of Significant Findings and Mission Impact*

(A) Developing Array Pattern Tool for large arrays calculations:

A MATLAB code has been developed for faster radiation pattern approximation of a linear/planar array of any size and composed of any type of antenna elements. The code requires the center element pattern of a small array (say, 3×3) composed of the same type of antenna elements, desired lattice arrangement, and total number of array elements, as user inputs. The usage of this code will be included in future publications.

(B) Investigate the effects of array aperture area reduction on different array parameters:

The effects of different aperture shape and lattice arrangements on array gain and beam steerability have been studied for arrays modeled on PEC-backed substrates. Investigations show that a transformation from square-grid-rectangular-aperture to triangular-grid-hexagonal-aperture leads to $\approx 30\%$ reduction in aperture area ($\approx 50\%$ reduction in number of array elements) with a tradeoff of ≈ 1.5 dBi (in 2.5–5 GHz) and ≈ 3.5 dBi (640–990 MHz range) gain reduction. The aperture area reduction, however, comes at the cost of limited beam steerability to $\pm 45°$ from boresight, compared to the $\pm 60°$ scanning capabilities achieved from the square-grid-rectangular-aperture arrays, at all frequency ranges.

(C) Build minimum viable validation prototypes of single ESA elements:

Developed a design technique for electrically small microstrip patch antenna that provides $\geq 30\%$ impedance bandwidth by strategic placement of the feed-probe along the patch diagonal, at operating frequencies in the UHF (MHz) to microwave (GHz) frequencies. The method avoids any sophisticated prototyping and is a transformative approach in the design of electrically small microstrip antennas for ultrawideband wireless applications. The design approach was validated via prototypes manufactured on TMM-6 and TMM-10i substrates, in the 2.5–5 GHz range. Manufacturing of a prototype, for operation in the required UHF range (0.6–1 GHz), is currently underway.

(D) Optimization of ESA (single element) performance using regular, and ML based stochastic search algorithms:

Optimization of feed-probe location, ground plane shape and size in a microstrip patch antenna, with the objective of bandwidth enhancement, using ML based stochastic search algorithms (GA, PSO, and Simplex methods), was performed. ML algorithms were found to be ≈ 2 times faster and ≈ 0.3 times less memory intensive compared to regular search algorithms, while maintaining same degree of accuracy.

It is concluded that, although these automated ML algorithms do not provide insight into the underlying physics of the problems and require human intervention at every stage for better decision making, they can still be considered as potential tools for faster optimization of antenna performance, especially for multi-objective optimization of complex structures, which are computationally intensive using conventional EM solvers.

(E) Build minimum viable validation prototypes for arrays of ESA elements:

A 3×3 array of wideband elements (2.5–5 GHz) and a 2×2 array of narrowband elements (900 MHz), on TMM-10i substrates, were manufactured and tested. Having

achieved reasonably good agreement between simulated and measured S_{11} and gain responses from individual array elements, it was decided to implement the design method for building the final demonstrable prototypes. Currently, a 4×4 square-grid-rectangular-aperture and a 10-element triangular-grid-hexagonal-aperture array of wideband, microstrip, ESA elements, in the UHF range (0.6-1 GHz), are being characterized for prototyping.

(F) Optimization of array performance using ML algorithms:

Completed inter-element spacing optimization in a 4×4 square-grid array, on an infinitely large, PEC-backed, dielectric substrate, using ML based genetic algorithm, in the 2.5–5 GHz range, with the objective of array boresight gain enhancement. Multi-objective optimization (simultaneous enhancement in boresight gain and impedance bandwidth) of a 4×4 square-grid array on a finite, PEC-backed, substrate, by seeking the best array design parameters, including inter-element spacing, ground plane size, and feed-probe locations, in the desired UHF range (0.6–1 GHz), is pursued presently.

8.2 Tradespace Analysis of Ultra-Wide-Band (UWB) Koshelev Antenna

(Alex Dowell and Kalyan Durbhakula)

8.2.1 *Problem Statement, Approach, and Context*

Primary Problem: Determine the extent to which the physical aperture area of an antenna array, composed of antenna elements, can be reduced, while maintaining performance in peak power density, bandwidth, and electronic beam steerability over the UHF range (0.4–1 GHz), compared with present-art high-power-microwave-capable antenna arrays.

Solution Space: The Koshelev antenna has a unique design that is capable of generating an UWB response by effectively merging radiation characteristics from a transverse electromagnetic (TEM) horn antenna with exponentially tapered flares, an electric monopole, and magnetic dipoles over a wide frequency range [1]. This opens up an opportunity to investigate the design parameter space and understand parameter effects on impedance bandwidth, radiation pattern, electric field distribution, and other metrics via a tradespace study.

Sub-Problem:

(i) The integration of an impedance transformer to a single element Koshelev antenna to simulate and test the combined (transformer–antenna) performance is currently not feasible using commercial EM simulators.

(ii)The total surface currents on the Koshelev antenna over the desired frequency range arising from the present positioning of TEM exponential flares, an electric monopole, and magnetic dipoles is not yet clearly understood.

State-of-the-Art (SOTA): The balanced antipodal Vivaldi antenna (BAVA) is considered to be the SOTA antenna element due to its exceptional 20:1 impedance bandwidth ratio as well as the ability to handle tens-of-MW input power.

Deficiency in the SOTA: The BAVA design parameter space has been exhausted over the past couple of decades. The physical aperture area still remains very large and there is no viable path through tradespace study for further physical aperture area reduction.

Solution Proposed: Design, simulate, validate, and perform a tradespace study on the important design parameters of the Koshelev antenna array that effectively reduce its physical aperture area while maintaining its UWB properties, in both the frequency and time domains. The Koshelev antenna has been shown in the literature to withstand higher voltage levels (over 200 kV peak voltage), thereby making it a viable antenna element for detailed tradespace study and analysis.

Relevance to OSPRES Grant Objective: From the literature, it was shown that the Koshelev antenna can handle high input voltages (and therefore high power with 50 Ω input impedance), which satisfies the specific OSPRES objective related to high input voltage/power. In addition, this work can yield a center-frequency-dependent, bandwidth-controlled, and electronically steerable Koshelev antenna design that can be quickly modified to the spectrum properties of the ultra-fast rise time input pulse.

Risks, Payoffs, Challenges:

(i) The electrical size of the Koshelev antenna is approximately λ/4 at its lowest operating frequency. Further reduction of electrical size to λ/10 could considerably reduce frequency dependent gain, thereby decreasing the power spectral density.

(ii) Payoffs include the development of a library of antenna metrics data for different shapes and sizes of the individual parts within the Koshelev antenna.

(iii) The large electrical size (>5λ) of the Koshelev antenna at its highest operating frequency poses huge computational challenges.

8.2.2 *Tasks and Milestones / Timeline / Status*

(A) Complete literature search to identify and list antenna elements that satisfy UWB properties and HPM requirements, and down-select accordingly / NOV–DEC20 / Complete.

(B) Complete initial design, simulation, and validation of Koshelev antenna [1] / JAN21 / Complete.

(C) Perform a preliminary parameter study to identify design parameters that considerably reduce the physical aperture area / FEB–MAR21 / Complete.

- Milestone: Using FEKO and/or CST electromagnetic (EM) simulators, reduce the physical aperture size of the Koshelev antenna to at least 95% of its original design and show minimal to no variation in the bandwidth, gain and increased aperture efficiency / Complete.

(D) Determine the full-width half-maximum (FWHM) and ringing metrics from the envelope of the time domain impulse response ($h_{rx/tx}(t, \phi, \theta)$) in receive or transmit mode / MAR–APR21 / Complete.

- Milestone: Produce a generalized code that calculates the impulse response envelope of the Koshelev antenna and plots the rate of change in FWHM and ringing values as a function of physical aperture size.

(E) Perform tradespace studies on design parameters such as feed position (*F*), length (*L*), and alpha (α). Obtain various antenna metrics data, compare, and analyze / MAR21/ Complete.

- Milestone: Identify Koshelev antenna design parameters that significantly alter the bandwidth, rE/V, peak gain over the desired bandwidth, and aperture efficiency.

(F) Reduce Koshelev antenna aperture size (H×W) to equal to or less than 90 mm × 90 mm, equal to that of the SOTA BAVA, for direct antenna metrics comparison / MAR–APR21 / Complete.

- Milestone: Provide a recommendation on the optimum design parameters and the resulting metrics, with comparison to SOTA BAVA. The optimized design parameters must yield 900 MHz ± 200 MHz bandwidth, rE/V greater than 1, peak gain around 3 dBi at 900 MHz, aperture efficiency equal to or greater than 130% at 900 MHz.

(G) Using the optimized model from (F), build various array simulation models/topologies to perform a tradespace study and report tradeoffs between array antenna metrics such as center element reflection coefficient (S11) value, gain vs theta at constant phi, physical aperture area, aperture efficiency, and rE/V / MAY–JULY21 / Complete.

- Milestone: Develop/showcase an optimized Koshelev array model that exceeds an aperture efficiency of 130% with a high rE/V.

(H) Perform literature search to investigate, understand, and determine the applicability of special electromagnetic (EM) techniques to the antennas under consideration. / JAN–APR21 / Complete.

(I) Explore impedance taper (microstrip based and coax based) designs that can interface well (both mechanically and electrically) to transition the signal from a coax cable to the input of the Koshelev antenna element / JULY21–AUG21 / Complete.

- Milestone: Recommend the optimum impedance taper design (with minimum reflections and maximum power transfer) with the optimum dimensions to successfully convert the high-voltage, short-rise time input signal from a coax cable to the feed of the Koshelev antenna array.

(J) Study response from optimized Koshelev antenna array when excited with different monopolar, differential, and bipolar pulse signals of significant interest / AUG21–NOV21 / Ongoing.

- Milestone: Provide a table comparing the Koshelev antenna array response metrics and narrow down the suitable pulse signals. Recommend (if any) changes to the downselected pulse signal(s) that can further improve the radiation efficiency, and/or transient gain.

(K) Investigate and analyze the response from the optimized Koshelev antenna array when excited by different excitation patterns / DEC 21 / Complete.

- Milestone: Compare and recommend an appropriate excitation method to yield maximum boresight gain, maximum half-power beamwidth (HPWB), minimum side lobe levels, and maximum electric field, rE/V.

(L) Prototype single element Koshelev antenna and test for reflection coefficient, gain as a function of frequency, radiated electric field at 1-m, 2.5-m, 5-m and 10-m (if feasible) distances. / AUG21–SEP22 / Ongoing.

(L1) Fabricate Cu-foil and paint (silver or copper) variants of 3D-printed balanced Koshelev antenna with integrated impedance transformer.

- Milestone: Demonstrate a 3D printed Koshelev antenna prototype that is cost-effective and lightweight. / AUG21–NOV21 / Complete.

(L2) Perform scattering parameter measurements of Cu-foil and paint variants of 3D-printed prototypes to identify any design and fabrication issues/challenges.

- Milestone: Report fabrication & assembly challenges, test outcomes and identify the source of mistmatch (if any) to alleviate reflections. Verify against simulations to validate mismatches. / DEC21–APR22 / Ongoing.

(L3) Downselect to one variant of the 3D printed Koshelev antenna prototype and measure frequency domain gain and time-domain electric field at multiple distances.

- Milestone: Experimentally demonstrate a 3D-printed Koshelev antenna with a performance similar to the standard sheet metal variant of the Koshelev antenna. / MAY22–SEP22.

- Milestone: Report performance of 3D printed Koshelev antenna, compare against the performance of balanced antipodal Vivaldi antenna (BAVA), and recommend any overall improvements to the fabrication/prototyping/testing methods.

8.2.3 *Progress Made Since Last Report*

(L2) In the previous report, the S_{11} from the Koshelev antenna with impedance transformer showed degraded performance. Research was then conducted to try to minimize the losses due to reflections at the transformer–antenna interface. After a possible solution was identified, simulations were run on computer aided design (CAD) models to identify radiofrequency (RF) performance and to determine viability.

8.2.4 *Technical Results*

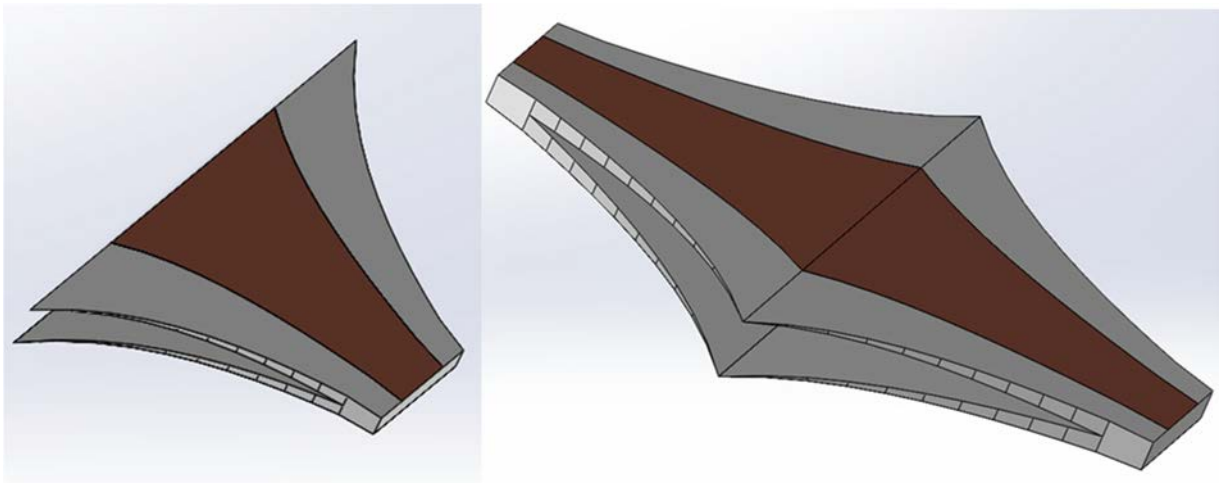
(L2) A new method of decreasing the relative permittivity of a fused deposition modeling (FDM) 3D printed polymer by decreasing the infill percentage has been reported [2]. In this paper, an equation is provided that is hypothesized to increase the performance of the current 3D printed Koshelev transformer. In theory, an impedance transformer that has a relative permittivity that matches the free space permittivity at the transformer-antenna interface and has a tapered dielectric that linearly increases the permittivity until it reaches the N-type feed, would minimize losses due to reflections.

$$v = \frac{\varepsilon_{reff} - 1}{\varepsilon_{ro} - 1} \quad (1)$$

Ɛ_reff	Volume %	Ɛ_0_PLA	Length From N Type Feed (mm)	Dielectric Height Cross Section Outer (mm)	Dielectric Width Cross Section Outer (mm)	Dielectric Height Cross Section Inner (mm)	Dielectric Width Cross Section Inner (constant)(mm)	Trace Height Cross Section Outer (mm)	Trace Width Cross Section Outer (mm)
3.11000	100%	3.11	10.0	7.87	38.95	7.87	38.95	7.87	19.47
2.89900	90%	3.11	17.0	8.48	48.82	7.63	48.82	8.48	22.02
2.68800	80%	3.11	24.0	9.1	58.687	7.28	58.68	9.1	24.84
2.47700	70%	3.11	31.0	9.71	68.55	6.79	68.55	9.71	27.97
2.26600	60%	3.11	38.0	10.32	78.41	6.19	78.41	10.32	31.49
2.05500	50%	3.11	45.0	10.93	88.27	5.46	88.27	10.93	35.47
1.84400	40%	3.11	52.0	11.55	98.14	4.62	98.14	11.55	40.04
1.63300	30%	3.11	59.0	12.16	108	3.64	108	12.16	45.35
1.42200	20%	3.11	66.0	12.77	117.87	2.55	117.87	12.77	51.64
1.21100	10%	3.11	73.0	13.38	127.73	1.33	127.73	13.38	59.26
1.00000	0%	3.11	80.0	14	137.6	0	137.6	14	68.8
			L step size						
			7.000						

Fig. 8.2.1. Effective relative permittivity and its corresponding design variable values utilized to design new impedance transformer model.

Using equation (1), where v is the volume percentage, ε_{reff} is the permittivity of material at that volume percentage, and ε_{ro} is the solid body permittivity of material, in addition to a RF micro strip calculator, a spreadsheet shown in Fig 8.2.1 was created to provide governing dimensions for a poly lactic acid (PLA) Koshelev partial dielectric impedance transformer. In the spreadsheet shown in Fig 8.2.1, each row represents dimensions and characteristics at cross sections every 7 mm starting from 10 mm from the N-type feed. A symmetric wedge was removed from the transformer. Therefore, between the top and ground plane 100% PLA is used for the first 10 mm then linearly tapering to 0% PLA at 80 mm where it interfaces with the antenna. Using the equation above every 7 mm a new permittivity was calculated. The height of the transformer runs from 7 mm at the N-type feed to 14 mm where it interfaces with the antenna. Starting at 10 mm from the N-type feed inputs of permittivity, constant impedance (50 ohm), and percentage of the transformer's height was used to calculate the width of the trace at each cross section.



(a) (b)

Fig. 8.2.2. SolidWorks CAD models of (a) LA based partial dielectric impedance transformer and (b) Mirrored PLA based partial dielectric impedance transformer.

After generating models, simulations in CST studio suite were ran on the PLA based partial dielectric impedance transformer and the mirrored PLA based partial dielectric impedance transformer to collect S-parameters. Then the S-parameters were compared to the original and the mirrored original versions.

Figs. 8.2.3 to 8.2.6 compare the S-parameters (S_{11}, and S_{21}) between original and newer versions of impedance transformer. To reiterate, the original transformer was designed using constant relative permittivity throughout the length of the transformer whereas the newer version is shown in Fig. 8.2.2, which varies the relative permittivity from one end to the other linearly. The S-parameters for the original version are obtained using FEKO and the S-parameters for the newer version are obtained using CST. Figs. 8.2.3 and 8.2.4 compare the S_{11} and S_{21} for the standalone transformer model as shown in Fig. 8.2.2(a), whereas Figs. 8.2.5 and 8.2.6 compare the S_{11} and S_{21} for the mirrored transformer model as shown in Fig. 8.2.2(b). In most of the results shown in Figs. 8.2.3 to 8.2.6, the partial dielectric impedance transformer outperforms the traditional/original impedance transformer i.e., by yielding lower S_{11} values and higher S_{21} values over the frequency range.

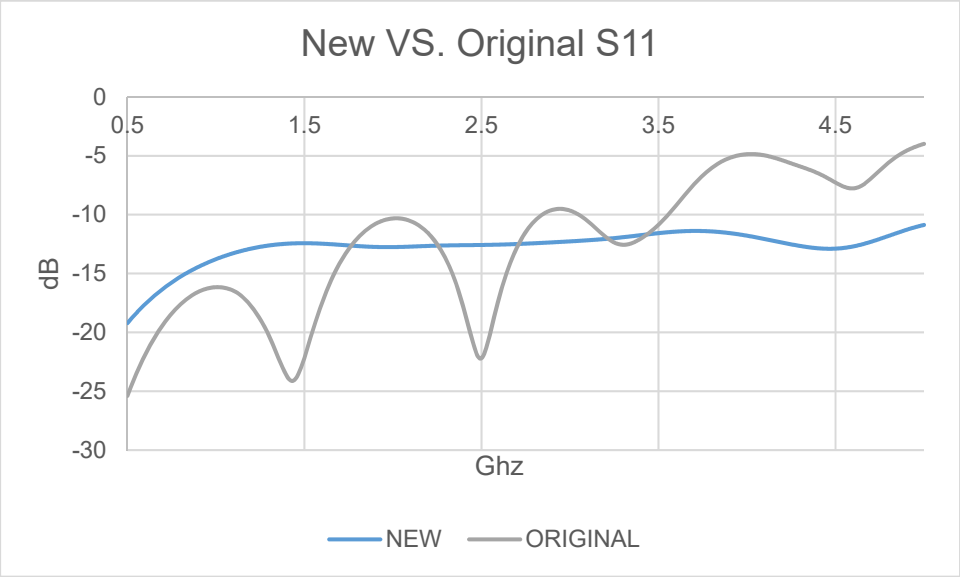


Fig. 8.2.3. S11 of the PLA Koshelev partial dielectric impedance transformer collected from CST compared to S11 of the original PLA Koshelev partial transformer.

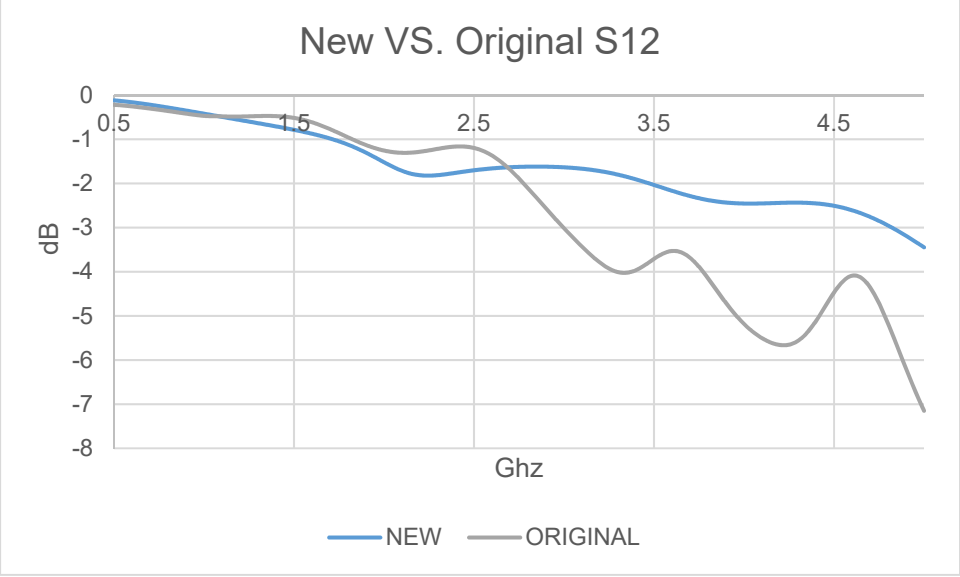


Fig. 8.2.4. S12 of the PLA Koshelev partial dielectric impedance transformer collected from CST compared to S12 of the original PLA Koshelev partial transformer.

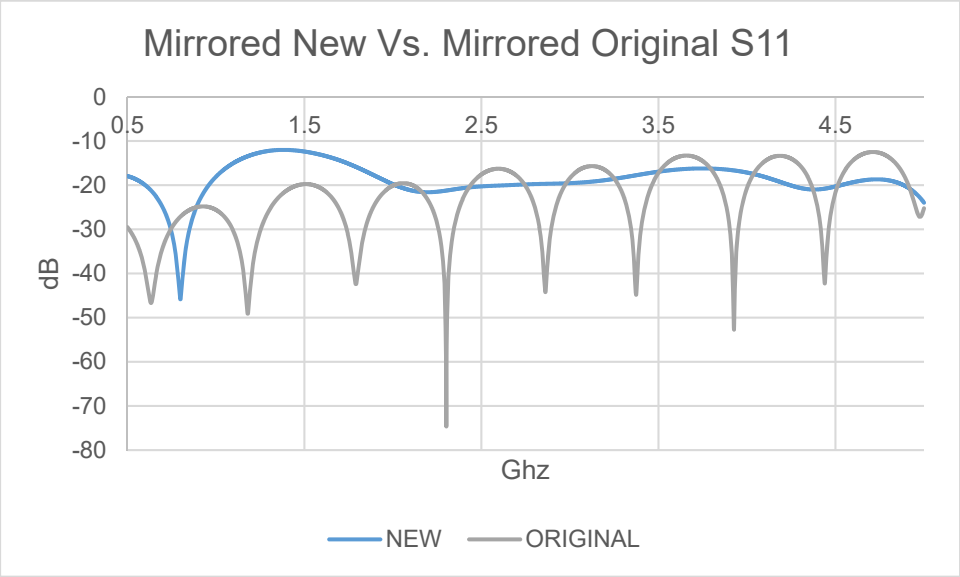


Fig. 8.2.5. S11 of the mirrored PLA Koshelev partial dielectric impedance transformer collected from CST compared to S11 of the mirrored original PLA Koshelev partial transformer.

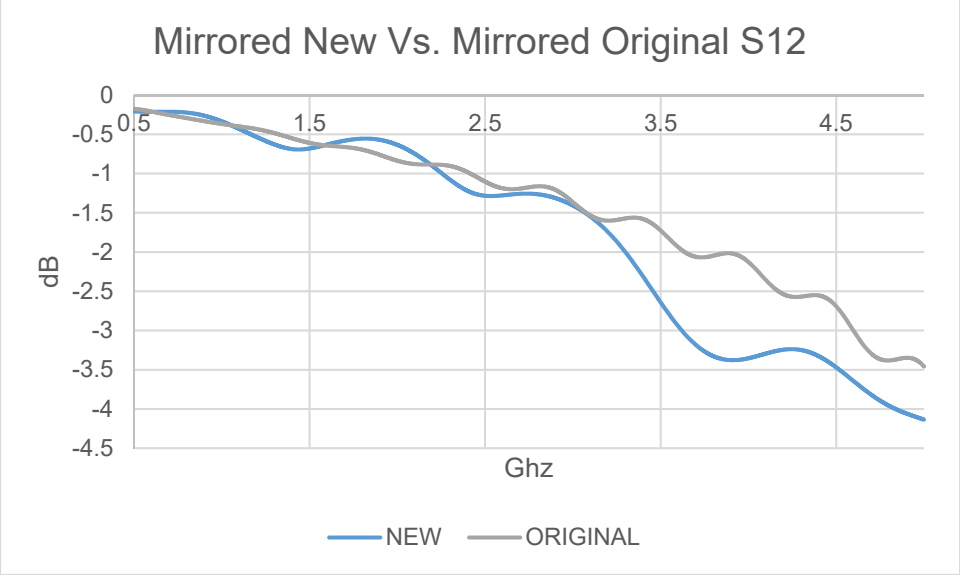


Fig. 8.2.6. S11 of the mirrored PLA Koshelev partial dielectric impedance transformer collected from CST compared to S11 of the mirrored original PLA Koshelev partial transformer.

8.2.5 *Summary of Significant Findings and Mission Impact*

(A) An extensive literature search on various UWB antenna elements has resulted in finding three promising options. The down-selected elements are the Koshelev, Shark, and Fractal antennas, which will be extensively studied using their individual design parameter space, which could result in physical aperture area reduction of the

single antenna element. Later, the single antenna element will be converted into a planar array.

(B) Initial validation of the Koshelev antenna simulated using CST software agreed well with the antenna metrics published in the open literature [1]. A UWB bandwidth response (10:1 bandwidth) and rE/V > 1 has been observed from our initial simulations of the Koshelev antenna. This validation ensured that the Koshelev antenna can be subjected to further tradespace studies to understand its performance followed by optimizing the design according to OSPRES grant requirements.

(C) The initial tradespace study and analysis of the Koshelev antenna design yielded promising outputs to carry forward the investigation. A comparison of important antenna metrics between the Koshelev antenna in [1] and aperture reduced Koshelev antenna are shown in Table 5.2.1 of the APR 21 MSR.

(D) An in-house code has been developed to calculate important UWB time domain antenna metrics such as full-width half maximum (FWHM) and ringing. These metrics have been calculated using in-house MATLAB code using the excitation voltage and radiated electric field information obtained from CST simulations. FWHM and ringing antenna metrics help with assessing or characterizing an antenna's UWB response.

(E) The tradespace study of feed position provided a deeper understanding of how its position impacts the S11 value bandwidth. An optimum value for feed position i.e., $F = 1/20 < L < 1/10$ is recommended to achieve maximum bandwidth. The tradespace study of the antenna length (L) is straightforward. A longer antenna length will radiate better at lower frequencies. However, physical size restrictions/requirements must be kept in mind in determining the antenna length. Finally, a larger α value (>120°) is recommended to avoid unnecessary reflections from the electric monopole.

(F) From a thorough tradespace study, the aperture size of the Koshelev antenna (single element) is determined to be 90 mm × 100 mm in order to achieve desired antenna metrics performance proposed in the milestone. All metrics described in the milestone have been successfully achieved except the desired bandwidth (200 MHz on both sides) at 900 MHz center frequency. The bandwidth achieved is 900 ± 100 MHz.

(G) The physical aperture area of the Koshelev array antenna largely depends on the interelement spacing and the shape of the array. We were able to determine that the diamond topology is the optimum shape for the Koshelev array antenna. We were also able to obtain similar gain profile (peak gain and pattern) from making certain elements within the array passive (off state) when compared against regular active array (all elements in on state). From the non-symmetric interelement spacing values, we found that S_y has the least effect on the output; therefore a small spacing value can be chosen to reduce the physical aperture area of the Koshelev array.

(H) The literature search on the special EM techniques expanded our knowledge and opened the door to opportunities to apply some of those techniques to the antennas under study. EM techniques such as non-symmetric and non-square array topologies have been applied to the development and study of the Koshelev array antenna.

(I) The first impedance taper design under consideration has shown good S11 values (< –10 dB) over the frequency range of interest. In addition, we have shown that the shape of the pulse can be easily retained at the output of the taper with less than 5% amplitude losses.

(J) The Koshelev antenna array response from feeding a monopolar vs bipolar signal has demonstrated a clear winner: that is, a bipolar signal will radiate at least 10 times better than a monopolar signal. A comparison of the frequency spectrum of the radiated electric field from the optimized Koshelev antenna array between different monopolar pulse sources has identified the 'MI0731' pulse to be the optimum pulse.

(K) The optimized Koshelev antenna array was studied for the electric field response under different array excitation patterns. The study determined that the uniform and Gaussian excitation patterns were the optimum excitation patterns. Selecting the uniform or Gaussian excitation pattern would yield the maximum electric field at the boresight for an arbitrary input signal.

(L) Two variants (Cu-foil plated and silver painted) of the 3D-printed Koshelev antenna have been fabricated to demonstrate a working antenna prototype. The measured S_{11} result of the Cu-foil plated variant showed poor performance due to issues at the transformer–antenna interface. To identify the root cause of the above issue, we have fabricated and tested a standalone impedance transformer component, which displayed good measurement values. On the other hand, the combined simulation of transformer–antenna design yielded slightly degraded S_{11} when compared to the standalone Koshelev antenna design due to field discontinuity at the interface. The newer version of impedance transformer, i.e., the partial dielectric impedance transformer, displayed improved S_{11} and S_{21} values when compared to the original impedance transformer. These results introduce a new method of designing impedance transformers with minimum insertion loss over wider operating frequencies.

8.2.6 *References*

[1] Gubanov, V. P., et al. "Sources of high-power ultrawideband radiation pulses with a single antenna and a multielement array." *Instruments and Experimental Techniques* 48.3 (2005): 312-320.

[2] S. Zhang, Y. Vardaxoglou, W. Whittow and R. Mittra, "3D-printed graded index lens for RF applications," 2016 International Symposium on Antennas and Propagation (ISAP), 2016, pp. 90-91.

8.3 Machine Learning Inspired Tradespace Analysis of UWB Antenna Arrays

(Sai Indharapu and Kalyan Durbhakula)

8.3.1 *Problem Statement, Approach, and Context*

Primary Problem: Determine the extent to which the physical aperture area of an antenna array, composed of antenna elements, can be reduced while maintaining performance in peak power density, bandwidth, and electronic beam steerability over the

UHF range (0.4–1 GHz), compared with present-art high-power-microwave-capable antenna arrays.

Solution Space: Fractal antennas possess exceptional fidelity factor values (>0.9), which describe how well the shape of the input pulse is retained at an observation point in the far-field. Their high degree of freedom provides an opportunity to develop systematically modified patch shapes, which in turn leads to improved bandwidth while retaining high fidelity factor values. Machine learning (ML) can be leveraged to predict the antenna array response for an arbitrary design parameter space upon sufficient training and validation.

Sub-Problem:

(i) Fractal antennas generate omni-directional radiation patterns in the H-plane over the desired frequency range.

(ii) ML can suffer from underfitting or overfitting the training model which in turn leads to deviations in the predicted output.

State-of-the-Art (SOTA): Conventional full-wave EM solvers such as method of moments (MoM), multi-level fast multipole method (MLFMM), finite element method (FEM), and finite difference time domain (FDTD) method are currently being used to study, analyze and assess the performance of UWB antennas.

Deficiency in the SOTA: UWB antenna optimization using conventional EM solvers utilizes significant computational time and memory resource.

Solution Proposed:

(i) Design, simulate, validate, and perform a tradespace study on the design parameter space of the selected fractal antenna element using commercially available electromagnetic (EM) wave solvers.

(ii) Train, validate, test and compare multiple ML models for quicker and accurate prediction of antenna array response for different physical aperture areas.

Relevance to OSPRES Grant Objective: The fractal antenna achieves an UWB response, a mandatory requirement of the OSPRES grant objective, in a small volume footprint and similar physical aperture area when compared against the SOTA BAVA, dual ridge horn antennas etc. Furthermore, the microstrip-design-based fractal antenna can efficiently handle electronic steering by integrating the feed network on the same board. This eliminates the need to build a separate feed network external to the fractal antenna using bulky coaxial cables.

Risks, Payoffs, and Challenges:

(i) A majority of the fractal antenna geometries yield an omni-directional pattern in the H-plane, which can be a risk. However, efforts are underway to mitigate this pattern without deteriorating bandwidth.

(ii) Payoffs include developing a library of antenna metrics data for various fractal shapes and sizes.

(iii) Design challenges and numerical calculations with respect to specific fractal shapes could arise after performing a certain number of iterations to further improve the bandwidth.

(iv) Fractal antennas were known to generate gain loss at random frequencies over their operating frequencies. Achieving gain stability over the desired frequency range can be a significant challenge.

8.3.2 *Tasks and Milestones / Timeline / Status*

(A) Perform tradespace analysis of the fractal element radius *b* over the desired frequency range (4 to 12 GHz) using the genetic algorithm (GA) optimization tool available in the commercial electromagnetic (EM) solver FEKO / FEB21 / Complete.

- Milestone: Provide a recommendation of an optimum value of *b* using OPTFEKO to minimize reflection coefficient or S_{11} (< –10 dB).

(B) Perform tradespace study on different fractal shapes by changing the number of fractal segments to understand the effect of this change on the impedance bandwidth / FEB21 / Complete.

- Milestone: Produce a detailed study of the antenna response such as S_{11}, gain, and bandwidth by varying the number of fractal segments.

(C) Apply the GA optimization tool on the fractal side length *b* over a wide frequency range (2 to 12 GHz with 201 discrete frequency points) and number of fractal segments using OPTFEKO on the LEWIS cluster / MAR21 / Complete.

- Milestone: Reduce physical aperture area by 10% of its present design, reported in the FEB MSR, and demonstrate minimal or no change in S_{11}, gain, and fidelity factor values.

(D) Perform a parametric study and analysis of antenna response by varying hexagon radius, *a* / MAR–APR21 / Complete.

- Milestone: Recommend a value of *a* to reduce the physical aperture area and increase aperture efficiency (>50%) with no variation in other antenna metrics.

(E) Frequency scale fractal antenna design such that the center frequency of the resulting antenna equals 1.3 GHz / MAY21 / Complete.

- Milestone: Modify antenna design with a center frequency equal to 1.3 GHz and achieve similar results (3:1 bandwidth at fc = 1.3 GHz, 3 dBi gain and >130% aperture efficiency at 900 MHz) to antenna design at center frequency ~7 GHz.

(F) Design and simulate various array antenna geometries composed of optimized fractal antenna elements (obtained from (E)) to analyze the effect of overall array antenna geometry on the desired array antenna response metrics (i.e., gain vs. frequency, gain vs. elevation angle at constant phi, rE/V, half-power beamwidth and side-lobe level.) / MAY–JUL21 / Complete

- Milestone: Recommend a best possible structure with reduced aperture area and minimal loss in gain.

(G) Apply ML models available in Altair Hyperstudy (2021) on the fractal antenna to try and understand the possibilities and limitations of ML models for fast and efficient antenna metrics prediction and optimization. Expand the prediction capability to time-domain electric field and antenna pattern using ML models (k-nearest neighbor and linear regression) available in scikit learn on Python programming tool “Anaconda”. / MAY21–FEB22 / Complete.

- Milestone: Recommend most accurate and efficient ML model for a fractal antenna in time-domain and frequency domain.

(H) Apply ML models on the octagon fractal antenna array lattice to extend the prediction capability beyond single element / SEP21–MAY22 / Complete.

- Milestone: Recommend the best suitable ML model implemented/developed using Python programming language for array antenna metrics prediction.

(I) Develop a graphical user interface (GUI) to ease the process of employing ML models to predict the antenna output response/ FEB22–SEP22 / Ongoing.

- Milestone: Incorporate the developed automated data extraction scripts, ML scripts to the GUI to enable user to predict antenna response with shorter time.

8.3.3 *Progress Made Since Last Report*

(I) Development and testing of the GUI.

The earlier version of the graphical user interface (GUI) was developed to carry out tradespace study on a selected group of design variables of the fractal antenna (i.e., the design variables added to the validation window cannot be adjusted or renamed). Over the past month, the GUI has been updated to allow users to add antenna design of choice, the capability to add desired number of design variables, and assign design variable names.

- A rectangular horn antenna design with dielectric loading is selected to test the development made and to understand the ease of employing machine learning (ML) algorithms. The horn antenna design illustrated in Fig. 8.3.1 has many adjustable parameters. A test is carried out to predict the value of ε_r of dielectric loading for which the horn antenna design yields maximum impedance bandwidth, and maximum gain consecutively.

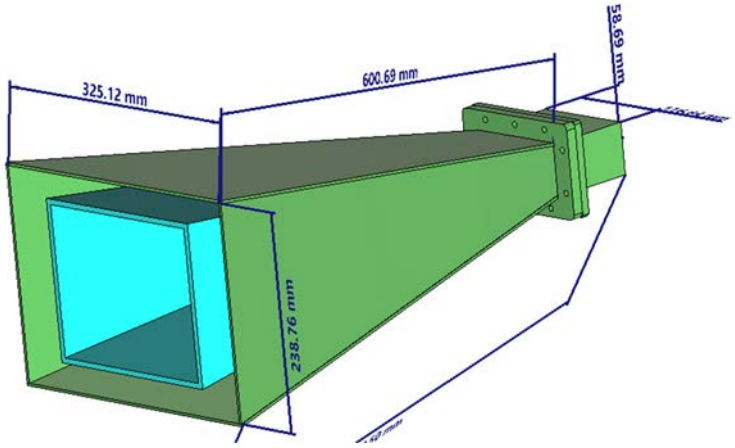


Fig 8.3.1. A rectangular horn antenna with dielectric loading (blue region).

8.3.4 *Technical Results*

(I) Development and testing of the GUI.

- The focus and development of the GUI is to ease the process of employing ML algorithms for the users. To achieve that, the GUI has been generalized and can be used for parametric study of any given antenna irrespective of frequency range of interest, type of the antenna design, etc. Irrespective of the antenna design, the steps involved in extracting the training data and training the ML model remains the same.

Below are the steps that should be followed to assign the Labels for the input fields:

1. Upon clicking the “validate” button a small window pops up with an entry field requesting the user to enter number of inputs, which will be utilized to train the ML model, which is shown in Fig. 8.3.2.
2. After specifying the number of inputs and clicking the “Next” button the GUI will now open a new window with entry fields requesting user to assign the design variables for each of the input as shown in Fig. 8.3.3.

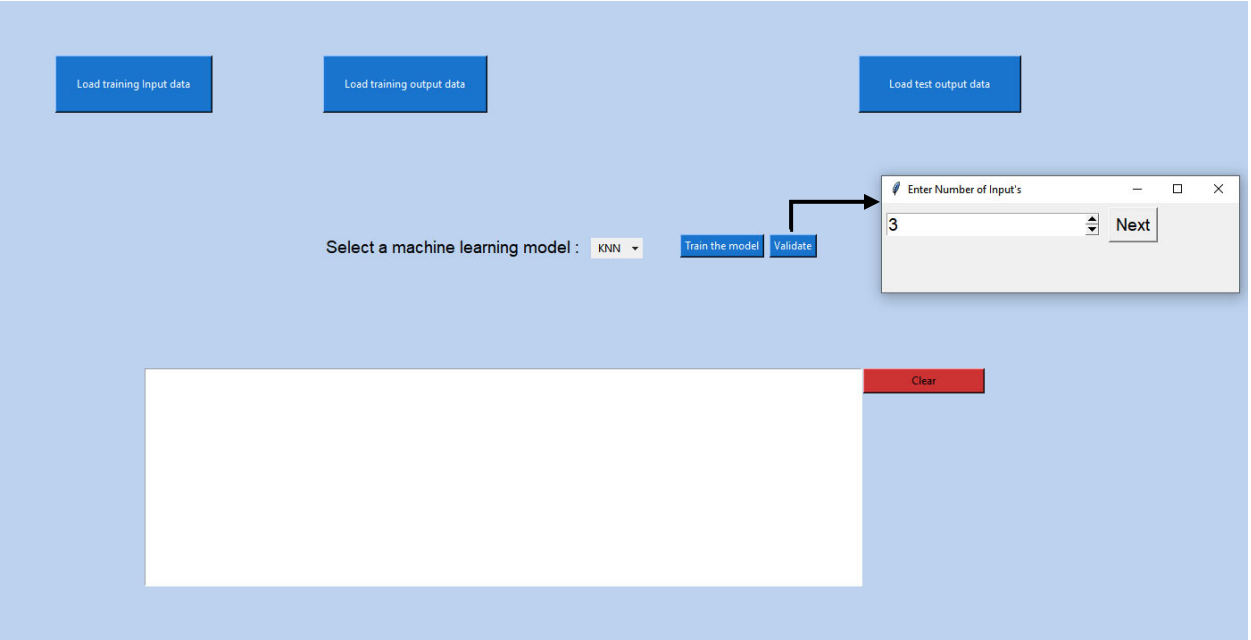
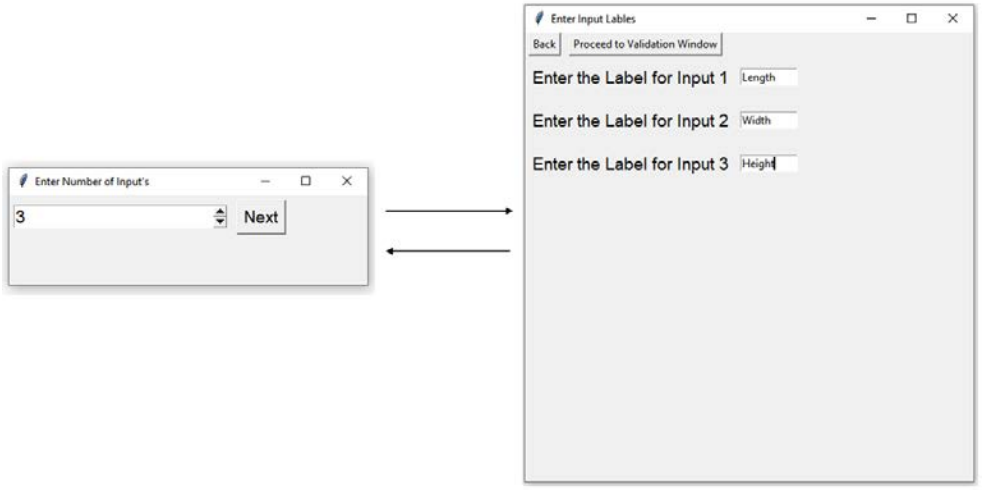


Fig. 8.3.2. Snapshot of the GUI with the pop up box to enter number of design variables.

3. The user can move in between entering the number of Input window and entering the labels by using the “Next” button and the “Back” button.



(a) (b)

Fig. 8.3.4. Snapshot of (a) “Enter Number of Input’s” window, (b) “Enter Input Labels" window.

4. Finally, after specifying the labels for the inputs, the “Proceed to validation window” button can be used to open validation window for further analysis.

- To validate the new version of the GUI and to test the ability of the GUI in carrying out parametric sweep analysis on other antenna designs, a Horn antenna design is used. The selected design is simulated using CST to generate training data, a

single design parameter (ε_r) is changed between 1 and 20 and the corresponding S_{11} and gain response are recorded to be used in training and testing the ML.

S_{11} prediction using the GUI:

Upon generating 20 samples of input and output using CST, the ML model included in the GUI has been trained using 15 samples and the remaining 5 are saved to be used while testing. From Fig. 8.3.5, it is evident that the new version of the GUI can adjust the label of the input according to the user input (i.e., the new user input Label of ε_r in Fig 8.3.5) and predict the output for the given antenna.

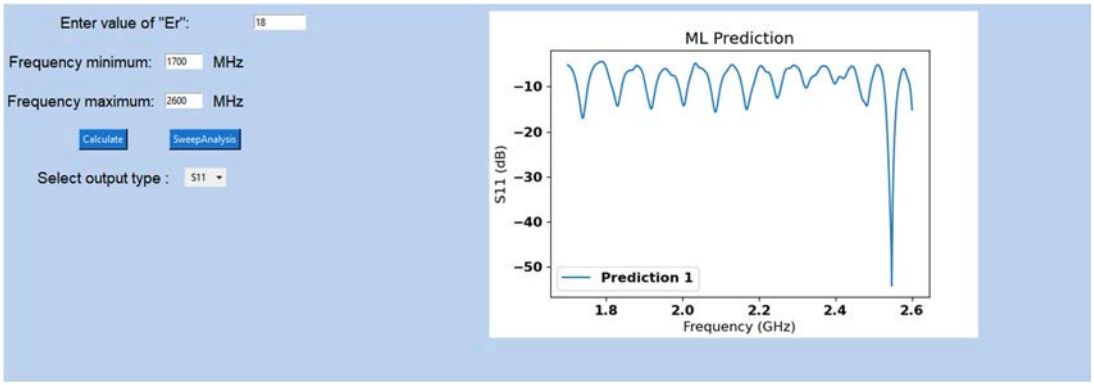


Fig. 8.3.5. Snapshot of validation window of the GUI (S_{11} prediction).

To validate the GUI prediction for the test input (i.e., ε_r = 18), the GUI response is compared against the CST response for the same input as shown in the Fig. 8.3.6.

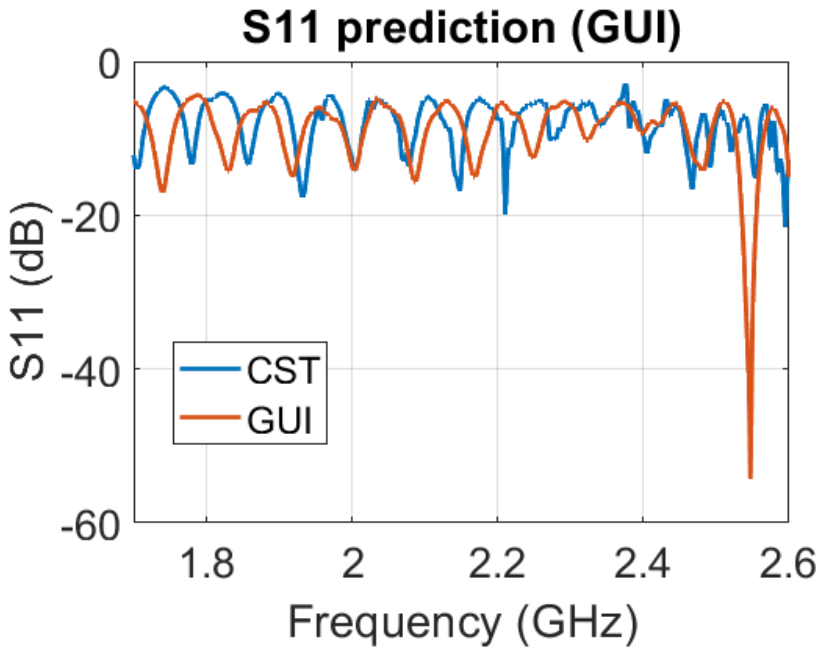


Fig. 8.3.5. Comparison of S11 response from CST with GUI prediction.

Gain prediction using the GUI:

The approach used in "S_{11} prediction using GUI" has been followed for validating the GUI for gain prediction. The training data includes 20 samples of input (ε_r) and corresponding output (gain) are generated using CST for training the ML model in the GUI. Fig. 8.3.6 illustrates the gain prediction of the GUI for a user specified input (i.e., $\varepsilon_r = 17$).

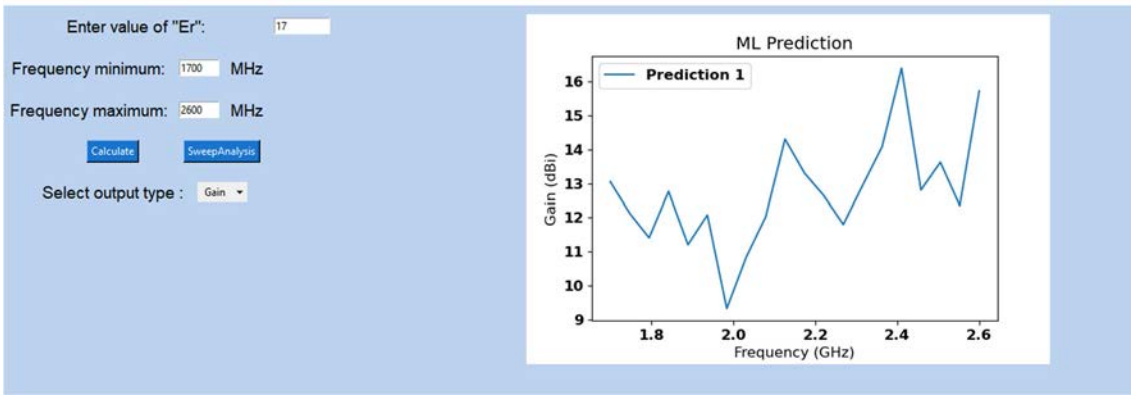


Fig. 8.3.6. Snapshot of validation window of the GUI (Gain prediction).

To validate the gain prediction from the GUI the predicted output is compared against the CST response as shown in the Fig. 8.3.7.

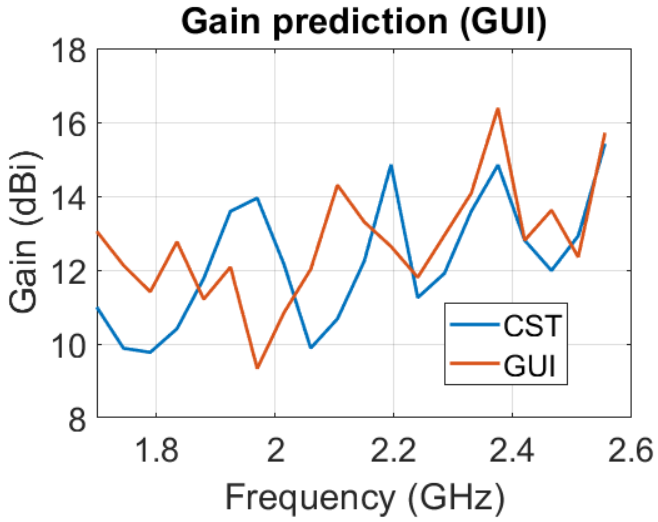


Fig. 8.3.7. Comparison of gain response from CST with GUI prediction.

Finally, from the above test GUI can be used for any given antenna design. The RMSE values for S_{11} and gain prediction are 5.7468 and 1.9211 respectively. The high RMSE value seen from the prediction of S_{11} can be decreased further by increasing the number of samples in the training data.

8.3.5 *Summary of Significant Findings and Mission Impact*

(A) We carried out an effort to identify the dominant fractal antenna design parameter and its corresponding value using parameter study and FEKO optimization tool. It was found that the side length 'b' of the fractal elements play a significant effect on the antenna bandwidth. The initial analysis of the simulation results with fractal radius *b* equal to 1.8 mm yielded multiple resonant frequencies with enhanced bandwidth. To further increase the bandwidth, OPTFEKO was used as an optimization tool with fractal radius *b* as the optimization variable. Finally, the optimum value for *b* is found to be 1.66 mm which minimizes the S_{11} (-10 dB).

(B) The addition of fractal elements (*N*) to the simple hexagon improved antenna metrics such as reflection coefficient (S_{11}). To further investigate and understand the fractal elements, the number of segments (sides of the fractal element) in the fractal geometry were varied within the range of 6 to 14. By varying the number of segments in the fractal element, the resultant S_{11} response has positive impact at higher frequencies and negative impact at lower frequencies. Therefore, the number of segments of the fractal element were chosen to be 6 as it has better balance of S_{11} values both at lower and higher frequencies.

(C) The initial optimum value of *b* over 51 discrete frequency points is reported as 1.66 mm in task (A). To further increase the accuracy of the optimization algorithm and to find a more precise value for *b*, optimization is further performed over a wider frequency range (201 discrete points between 2 GHz to 12 GHz) which yielded an optimum value of *b* as 1.37 mm. The S_{11} response of the antenna design with this newly obtained *b* parameter (i.e., 1.37 mm) has not produced any better bandwidth compared to *b* = 1.66 mm. Thus, *b* is set to be 1.66 mm for further research.

(D) The hexagonal patch radius *a* has a significant effect on the physical aperture area of the antenna. Therefore, Altair OPTFEKO has been utilized to find an optimum *a* value, which was determined to be 8 mm over the range 7.2 to 9 mm. Antenna metrics such as S_{11}, gain, and bandwidth have shown desired performance with the optimized *a* value.

(E) The initial antenna design has been modified to achieve a center frequency of ~1.3 GHz. The gain value at 900 MHz is 3.5 dBi and, with the modified antenna design, we were able to achieve an impedance bandwidth ratio of 3.3:1. The designed antenna has been fabricated and tested, and the S_{11} response of the fabricated antenna agrees well when compared against FEKO, CST.

(F) Four different fractal antenna array geometries (i.e., square, diamond, hexagon, and octagon) have been designed and simulated. Upon comparing antenna array metrics, the octagonal fractal antenna array has yielded minimal sidelobe levels with a gain of 15.7 dBi at 900 MHz, close to that of the square geometry but with with 32.27% lower physical aperture area. The octagonal fractal antenna array has been chosen as the optimum geometry with reduced aperture area and reduced side lobes while retaining the bandwidth and gain milestone metrics.

(G) The ML models available (radial basis function (RBF), least square regression (LSR) and, hyper kriging (HK)) in Altair Hyperstudy were employed to predict the output

response of a fractal antenna. From the above-mentioned ML models RBF and LSR were down selected from the initial three ML models based upon their generalization capability for prediction of fractal antenna output response. The test RMSE increased as the values drifted away from the mid-point of the training range. RBF performed well in the prediction of S_{11}, while LSR performed slightly better for gain and electric field predictions. In addition, for time-domain electric field prediction, we recommend using k-nearest neighbors (kNN) ML algorithm for accurate prediction.

(H) The initial application of the kNN ML model for the prediction of antenna array bandwidth response of center and corner element yielded positive results with a good agreement between traditional EM solver (FEKO) and trained kNN ML model. The new LR ML model yielded improved RMSE values (over kNN) in its prediction of reflection coefficient (27.82% less RMSE for center element and 19.76% less RMSE for corner element). On the other hand, the RMSE values for gain (as function of theta) prediction using LR ML model has 55.51% increase over kNN prediction. Finally, kNN provides better generalization to predict reflection coefficient, whereas LR provides better generalization to predict frequency domain gain in the case of a fractal antenna array. On the other hand, the application of the AEP method for antenna array was put on hold due to its limitations.

(I) A GUI is developed, which accepts training data for an antenna (single-element or array) of user choice and can predict output response (S_{11} and gain) for a range of test data within a few seconds. Further, the GUI is updated to perform parametric sweep analysis for S_{11} and gain response of a fractal antenna design. Finally, the current version of the GUI can be used to perform tradespace analysis, parametric sweep analysis of any given antenna design using ML model.

8.3.6 *References*

[1] H. Fallahi and Z. Atlasbaf, "Study of a Class of UWB CPW-Fed Monopole Antenna With Fractal Elements," in IEEE Antennas and Wireless Propagation Letters, vol. 12, pp. 1484-1487, 2013, doi: 10.1109/LAWP.2013.2289868.

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9 Feedback

There is no feedback to report for the current reporting period.

10 Program Management

10.1 Issues

i. Scope – No issues
ii. Budget – 12-month NCTE submitted/pending
iii. Schedule – No issues

10.2 Interactions with Others

Agency/Org	Performer	Project Name	Purpose of Research/ Collaboration

10.3 Major Procurement Actions

10.4 Travel

Destination	Purpose	Attendees	Estimated Costs

10.5 Pending or Upcoming Public Release Requests

11 Appendix A: Academic and IP Output

11.1 Students Graduated

Name	Degree	Currently
Al-Shaikhli, Waleed	MS Spring 19	Kansas City National Security Campus, Honeywell
Azad, Wasekul	PhD Summer 21	Applied Materials, Sunnyvale, CA
Berg, Jordan	MS Spring 21	MRI Global
Bhamidipati, John	PhD Spring 22	MIDE
Bissen, Bear	MS Spring 19	Capella Space, San Francisco, CA
Brasel, Sadie	BS Spring 21	
Floyd, Dennis	BS	Naval Air Warfare Center Weapons Division
Hanif, Abu	PhD Spring 21	
Harmon, Aaron	BS	Missouri University of Science & Technology
Harp, Joshua	MS	
Hauptman, Cash	BS Spring 18	University of Nebraska-Lincoln
Klappa, Paul	MS Spring 21	
Kovarik, James	MS 21	
Labrada, Dario	BS Spring 20	Honeywell Aerospace, Florida
Lancaster, John	MS Spring 17	Lawrence Livermore National Laboratory, CA
Renzelman, Jeff	MS Spring 18	Kansas City National Security Campus, Honeywell
Roy, Sourov	PhD Spring 21	BTCPower, Orange County, CA
Wagner, Adam	MS Fall 20	Los Alamos National Laboratory, New Mexico
Xia, Shengxuan	BS	Missouri University of Science & Technology

11.2 Journal Publications

11.2.1 *In Preparation*

[1] S. S. Indharapu, A. N. Caruso, K. C. Durbhakula, “Machine Learning Assisted Antenna Design Optimization of UWB Fractal Antenna,” TBD, In Preparation, **2022**.

[2] J. K. P Bhamidipati, G. Bhattarai, A. N. Caruso, “Effect of Proton Irradiation Induced Localized Defect/Trap Clusters on Silicon Photoconductive Semiconductor Switch (Si-PCSS) Recovery Time and Leakage currents,” *Solid-State Electronics,* In Preparation, **2022**.

[3] N. Gardner, K. C. Durbhakula, and A. N. Caruso, “UHF and L-Band Frequency Generation at MW Peak Power using Diode-based Nonlinear Transmission Lines as Pulse Forming Networks,” *Transactions on Plasma Science*, In Preparation, **2022**.

[4] N. Gardner, K. C. Durbhakula, and A. N. Caruso, “Electrically Tunable Diode-based Nonlinear Transmission Line,” *TBD*, In Preparation, **2022**.

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[7] M. Hamdalla, V. Khilkevich, D. G. Beetner, A. N. Caruso, A. M. Hassan, "Characteristic Mode Analysis Justification of the Stochastic Electromagnetic Field Coupling to Randomly Shaped Wires," *IEEE Transactions on Electromagnetic Compatibility*, In Preparation, **2020**.

11.2.2 *Submitted / Under Revision*

[8] J. K. P. Bhamidipati, E. R. Myers, A. M. Conway, L. F. Voss, M. M. Paquette, and A. N. Caruso, "Figure of Merit Development for Linear-Mode Photoconductive Solid-State Switches," *IEEE Journal of the Electron Devices Society*, Submitted May 1 **2022**, Manuscript ID#JEDS-2022-05-0136-R.

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[11] B. K. Lau, M. Capek, and A. M. Hassan, "Characteristic Modes–Progress, Overview, and Future Perspectives," *IEEE Antennas and Propagation Magazine*, Submitted, **2021**.

[12] K. Alsultan, M. Z. M. Hamdalla, S. Dey, P. Rao, and A. M. Hassan, "Scalable and Fast Characteristic Mode Analysis Implementation Using a Hybrid CPU/GPU Platform," *ACES*, Submitted, **2021**.

[13] W. Azad, F. Khan, and A. N. Caruso, "A Scalable Multilevel-Modular 10 kV Silicon Carbide MOSFET Module Featuring Custom Isolated Gate Driver Circuit Combined with Coupling and Snubber Circuits," *IEEE Transactions on Power Electronics*, Submitted, **2021.**

11.2.3 *Published / In Press*

[14] N. Gardner, K. C. Durbhakula, and A. N. Caruso, "Design Considerations for Diode-Based Nonlinear Transmission Lines," *AIP Advances*, 12, 055012, **May 2022** [doi].

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11.3 Conference Publications

11.3.1 *Submitted / Accepted*

[1] B. Barman, D. Chatterjee, and A. N. Caruso, "Characterization of Planar Phased Arrays of Electrically Small UWB Microstrip Patch Antennas," *2022 IEEE International Symposium on Phased Array and Technology,* Waltham, Massachusetts, USA, Oct. 11-14, 2022, pp. 1-8. (Submitted).

[2] B. Barman, D. Chatterjee, and A. N. Caruso, "On the Optimum Substrate Selection in Wideband Microstrip Patch Antenna Design," *2022 IEEE International Symposium on Antennas & Propagation & USNC-URSI Radio Science Meeting*, Denver, Colorado, USA, July 10-15, 2022, pp. 1-2. (Accepted)

[3] B. Barman, D. Chatterjee, and A. N. Caruso, "Time Domain Analysis of an UWB Electrically Small Microstrip Patch Antenna," *2022 IEEE International Symposium on Antennas & Propagation & USNC-URSI Radio Science Meeting*, Denver, Colorado, USA, July 10-15, 2022, pp. 1-2. (Accepted)

11.3.2 *Presented*

[4] S. R. Shepard and H. A. Thompson, “Self-focusing in Guided and Un-guided Media,” submitted to the *2021 OSA Nonlinear Optics Topical Meeting, Virtual Event*, August 9-13, 2021.

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11.4 Conference Presentations

11.4.1 *Submitted / Accepted*

[1] S. Bellinger, A. Caruso, A. Usenko, "Stacked Diodes for Pulsed Power Applications," GOMACTech-22, Miami, FL, March 21–24 2022 (submitted, oral).

[2] S. Bellinger, A. Caruso, A. Usenko, "New Paradigm on Making Semiconductor Opening Switches for Pulsed Power," 2021 23rd IEEE Pulsed Power Conference, Denver, CO, Dec. 12–16, 2021 (accepted, oral).

Directed Energy Professional Society, Directed Energy Systems Symposium, Washington DC, October 25-29 2021 (submitted):

[3] B. Barman, D. Chatterjee, A. Caruso, and K. Durbhakula, "Tradespace Analysis of a Phased Array of Microstrip Patch Electrically Small Antennas (ESAs)" (Poster)

[4] J. N. Berg, R. C. Allen, and S. Sobhansarbandi, "A Novel Method of Cooling a Semiconductor Device through a Jet Impingement Thermal Management System: CFD Modeling and Experimental Evaluation" (Poster)

[5] J. N. Berg, R. C. Allen, and S. Sobhansarbandi, "Heat Transfer Enhancement of a Jet Impingement Thermal Management System: A Comparison of Various Nanofluid Mixtures" (Poster)

[6] J. Bhamidipati, M. Paquette, R. Allen, and A. Caruso, "Photoconductive Semiconductor Switch Enabled Multi-Stage Optical Source Driver" (Poster)

[7] G. Bhattarai, J. Eifler, S. Roy, M. Hyde, J. Bhamidipati, A. Usenko, M. Pederson, M. Paquette, A. Caruso, S. Bellinger, L. Voss, and R. Allen, "All Solid-State High-Power Pulse Sharpeners" (Poster)

[8] S. Brasel, K. Norris, R. Allen, A. Caruso, and K. Durbhakula, "Efforts to Reduce Physical Aperture Area of Ultra-Wideband Arrays" (Poster)

[9] A Caruso, "ONR Short Pulse Research and Evaluation for c-sUAV: Supporting and Sub-Programs Overview" (Oral)

[10] J. Clark, R. C. Allen, and S. Sobhansarbandi, "Ultra-Compact Integrated Cooling System Development" (Poster)

[11] J. Eifler, S. Roy, M. Hyde, G. Bhattarai, J. Bhamidipati, A. Usenko, M. Pederson, M. Paquette, A. Caruso, S. Bellinger, L. Voss, and R. Allen, "TCAD Optimization of Epitaxially Grown Drift-Step Recovery Diodes and Pulser Performance" (Poster)

[12] N. Gardner, M. Paquette, and A. Caruso, "Diode-Based Nonlinear Transmission Lines Capable of GHz Frequency Generation at Single MW Peak Powers" (Poster)

[13] M. Hamdalla, A. Caruso, and A. Hassan, “The Shielding Effectiveness of UAV Frames to External RF Interference” (Poster)

[14] M. Hamdalla, A. Caruso, and A. Hassan, “A Predictive-Package for Electromagnetic Coupling to Nonlinear-Electronics using Equivalent-Circuits and Characteristic-Modes (PECNEC)” (Poster)

[15] M. Hyde, J. Eifler, S. Roy, G. Bhattarai, A. Usenko, M. Paquette, A. Caruso, S. Bellinger, L. Voss, and R. Allen, “Development of an Evaluation Network for Drift Step Recovered Diodes through and Augmented Design of Experiment” (Poster)

[16] S. Indharapu, A. Caruso, and K. Durbhakula, “Machine Learning Based Ultra-Wideband Antenna Array Optimization and Prediction” (Poster)

[17] F. Khan, W. Azad, and A. Caruso, “A Scalable Multilevel-Modular 10 kV Silicon Carbide MOSFET Architecture for Pulsed Power Applications” (Poster)

[18] D. F. Noor, J. Eifler, M. Hyde, G. Bhattarai, S. Roy, J. Bhamidipati, A. Usenko, M. Pederson, M. Paquette, A. Caruso, S. Bellinger, L. Voss, and R. Allen, “DSRD-IES Pulsed-Power Generator Topology Study Using Machine-Learning-Based Feature Selection Optimization and Predictive Learning” (Poster)

[19] S. Roy, J. Eifler, M. Hyde, G. Bhattarai, D. Noor, J. Bhamidipati, A. Usenko, M. Pederson, M. Paquette, A. Caruso, S. Bellinger, L. Voss, and R. Allen, “Systematic Topological Optimization of DSRD-Based IES Pulse Generator” (Poster)

[20] S. Shepard and A. Caruso, “Tubular Core Optical Power Amplifier” (Poster)

[21] H. Thompson, M. Paquette, and A. Caruso, “Minimizing On-State Resistance in GaN:X Photoconductive Semiconductor Switches (PCSSs) for Direct Modulation (Poster)

[22] A. Usenko, J. Eifler, S. Roy, G. Bhattarai, M. Hyde, M. Paquette, A. Caruso, S. Bellinger, L. Voss, and R. Allen, “New Paradigm in Fabrication of Semiconductor Opening Switches for Pulsed Power” (Poster)

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[23] S. Bellinger, A. Caruso, A. Usenko, “Stacked Diodes for Pulsed Power Applications: New Process Integration Scheme,” 240th Electrochemical Society Meeting, Orlando, FL, Oct. 10–14, 2021 (submitted, oral).

11.4.2 *Presented*

[24] W. Azad, S. Roy, and F. Khan, “A Four-State Capacitively Coupled High-Voltage Switch Powered by a Single Gate Driver,” *47th IEEE Conference on Plasma Science*, Singapore, December 6-10, 2020 (oral).

[25] J. Hunter, S. Xia, A. Harmon, A. Hassan, V. Khilkevich, and D. Beetner, “Simulation-Driven Statistical Characterization of Electromagnetic Coupling to UAVS,” *Annual Directed Energy Science and Technology Symposium*, March 2020 (abstract appeared, but talk cancelled due to pandemic).

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[26] William Spaeth, Wideband Parallel Plate to Coaxial Cable Taper

[27] Stefan Wagner, Quickly Determining Minimum HPC Source Requirements Using Binary Search

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GOMAC 2019

[28] Cash Hauptmann, Reduced Recovery Time in SiPCSS Photoconductive Switches

[29] Eliot Myers, Picosecond High Power Switching Technologies

[30] Heather Thompson, GaN Optimization for Use in Photoconductive Switch

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[28] B. Barman, D. Chatterjee, and A. N. Caruso, “Analytical Models for L-Probe fed Microstrip Antennas,” *Proceedings of the IEEE Antennas and Propagation International Symposium and National Radio Science Meeting*, Atlanta, Georgia, USA, July 7-12, 2019 (1 page URSI Abstract).

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Directed Energy Professional Society (DEPS) Annual Science and Technology Symposium, Destin, Florida, USA, April 2019:

[29] Ryan Butler, Mechanical Challenges of Modular Photoconductive Semiconductor Based HPM Sources

[30] Steve Young, Two-Dimensional Optoelectronic Pulsed Power Switches: Initial Effort

[31] Adam Wagner, Rapid Cost Effective RF Component Prototyping Using 3D Printers

[32] Heather Thompson, Cost to benefit analysis of GaN for Photoconductive Semiconductor Switches

[33] Colby Landwehr, Low Leakage Electroluminescence For Improving SiPCSS Hold Off

[34] James Kovarik, Some Investigations Into Applications Of Electrically Small Antennas As Phased Array Elements

[35] Spencer Fry, Maximizing SiPCSS Efficiency For HPM Sources

[36] Deb Chatterjee, Studies On Antenna Characterization And Propagation Of High Power Pulsed Electromagnetic Waves With Minimal Dispersion

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DEPS Posters and Presentations 2018

[37] Jeff Scully, ElectroLuminescence Studies of Silicon Based Photo-Switches

[38] Cash Hauptmann, Thermal Anlaysis of a PCSS through TCAD Simulation

[39] Nicholas Flippin, Fast Rise Time Switches: Drift Step Recovery Diode

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[40] Noah Kramer, Recent Results of Silicon Based Photoconductive Solid State Switches for 500kHz Continuous Pulse Repetition Frequency

11.5 Theses and Dissertations

[1] John Keerthi Paul Bhamidipati, “Pulse Generation, Shaping, and Optimization Solutions for Solid-State-Switch-Enabled High-Power Microwave Generation Systems” PhD Dissertation in Physics and Electrical Engineering, University of Missouri-Kansas City, **2022**.

[2] Jordan N. Berg, “Development of a Jet Impingement Thermal Management System for a Semiconductor Device with the Implementation of Dielectric Nanofluids,” MS Thesis in Mechanical Engineering, University of Missouri-Kansas City, **2021** [mospace].

[3] James C. Kovarik, “Wideband High-Power Transmission Line Pulse Transformers,” MS Thesis in Electrical Engineering, **2021** [mospace].

[4] Wasekul Azad, “Development of Pulsed Power Sources Using Self-Sustaining Nonlinear Transmission Lines and High-Voltage Solid-State Switches,” PhD Dissertation in Electrical Engineering, **2021** [mospace].

[5] Paul Klappa, “Implementation and Assessment of State Estimation Algorithms in Simulation and Real-World Applications,” MS Thesis in Mechanical Engineering, **2021** [mospace].

11.6 IP Disclosures Filed

[1] S. Bellinger, A. Caruso, A. Usenko, US Provisional Patent Application “Stacked Diode with Side Passivation and Method of Making the Same,” 12AUG2021.

[2] S. Bellinger, A. Caruso, A. Usenko, “Diode and Method of Making the Same,” 28JUNE2021.

[3] Bhamidipati, Myers, Caruso, “Multi-Stage Photo-Stimulated WBG-PCSS Driven RF Pulse Generation System Implementing Miniature Optical Sources,” 21UMK009, 04NOV2020.

[4] Shepard, “A Low Noise Optical Amplifier,” 21UMK007, 14SEPT2020.

[5] Shepard, “A Novel Optical Fiber Amplifier,” 20UMK012, 02JUN2020.

[6] Doynov, “High-power High Repetition Rate Microwaves Generation with Differentially Driven Antenna,” 20UMK011, 19APR2020.

[7] Doynov, “Scalable Modular System for High-power Microwaves Generation,” 20UMK010, 19APR2020.

[8] Doynov, “Pulse Differential High-power Microwave Generation,” 19UMK007, 02JAN2019.

[9] Doynov, “Non-linear Network Topologies with Reutilized DC and Low-frequency Signal,” 19UMK008, 28DEC2018.

[10] Doynov, Caruso, “Non-Linear Transmission Line Topologies for Improved Output,” 19UMK005, 28SEPT2018

11.7 Provisional Patents Filed

[1] S. Bellinger, A. Caruso, A. Usenko, US Provisional Patent Application “Stacked Diode with Side Passivation and Method of Making the Same,” filed 09/10/2021.

[2] S. Bellinger, A. Caruso, A. Usenko, “Diode and Method of Making the Same” US Provisional Patent Application 63/216,550, filed June 30, 2021.

[3] P. Doynov, A. Caruso, “High-Efficiency High-Power Microwave Generation using Multipass Non-Linear Network Topologies,” filed 26NOV2019.

[4] Plamen Doynov, James Prager, Tim Ziemba, Anthony N. Caruso, “Non-Linear Transmission Line Topologies for Improved Output”, USPTO Provisional Serial No. 62/737,185, filed 27SEPT2018.

11.8 Non-Provisional Patents Filed

None to date

12 Appendix B: Dynamically Tunable Multi-Frequency Solid-State Frozen Wave Generator

(John Bhamidipati)

12.1 Executive Summary

An all-solid-state compact multifrequency generator with chirp-capability and dynamic tunability was proposed as an attempt to overcome the limitations of the conventional RF pulsers in terms of form factor, frequency response, waveform tunability, and power conversion efficiency. Historically, frozen wave generators (FWGs), a sub-class of RF pulsers, were studied to address the aforementioned limitations, but their experimental realization implementing sparkgaps and coax-based distributed element transmission lines (DETLs) limited the system weight, reliability, form factor, and frequency tunability. The primary goal of the effort was to replicate the literature-standard coax-based FWG with varied coaxial cable lengths to demonstrate chirped pulse widths and extend the work by replacing the DETL system with lumped-element-based TLs (LETLs) to achieve SWaP optimization. SiC MOSFET-switched FWG prototypes for DETL- and LETL-based FWGs were implemented, where the lumped-element parameters such as inductance and capacitance for LETLs were adapted from the literature-standard DETLs with a velocity factor of 0.66.

Upon demonstrating the LETL-based FWG, the chirp- and dynamic-tuning-capability of an all-solid-state FWG was realized on a 7.5-cm × 30-cm × 3-cm printed circuit board via a 12-segment LETL embodiment. Dynamically tunable pulse trains with 15–24 ns pulse widths (40–80 MHz) were demonstrated with >35% pulse conversion efficiency with $<2\times10^{-4}$ m^3 volume, yielding >80% reduction in volume compared with vacuum-relativistic pulsers, and 60% reduction in weight compared with coax-based FWG system.

However, the transient characteristics of the enabling switch (MOSFET) in terms of t_{rise} and t_{fall} were noticed to be the limiting factors to attain flat-top pulse trains. Furthermore, a need for >11 ns pulse width/delay to be compatible with rated t_{rise} of the MOSFET capped the frequency response of the pulser at <100 MHz. A solid-state switch analogous to photoconductive solid-state switches (PCSSs) capable of sub-ns t_{rise} with low jitter and compact trigger mechanism would greatly benefit the solid-state LETL topology of the FWG.

12.2 Objective

Demonstrate a compact single PCB-mount, all-solid-state multifrequency generator capable of DC-to-RF pulse conversion with chirp capability and dynamic (electronic/mechanical) frequency tunability, and 30% or more power conversion efficiency, yielding >75% reduction in form factor compared with conventional microwave pulsers.

12.3 Technical Background

A pulse generator or a pulser is either an electronic circuit or a piece of electronic test equipment capable of generating rectangular pulses. Sources capable of generating RF

pulses from DC energy find applications in the pulsed power domain for microwave and millimeter-wave pulse generation, plasma physics, radar, time domain metrology, etc. Historically, equipment like vector inversion generators (VIG), quarter wave transmission-line-based oscillators, and lumped-element L-C oscillators have been typically implemented for generating frequencies <500 MHz [2]. The frequency of oscillation for such devices is inversely proportional to the square root of the product of the capacitance (C), and the inductance (L) (frequency $\propto \frac{1}{\sqrt{LC}}$) . For frequencies >500 MHz, the capacitance and inductance required for discrete LC oscillators are so small that stray effects tend to dominate and limit the attainable frequency. In the microwave region of the spectrum, devices like vircators, backward wave oscillators, relativistic magnetrons, etc. are used [2]. While VIGs configured as oscillators and lumped-element NLTLs are capable of generating pulses with center frequencies of 500 MHz and 1.2 GHz, respectively, they are limited by <12% efficiency. These pulsers are typically large, making them infeasible to deploy in compact and portable payload spaces. In general, the wave packet generated by these techniques consists of a decaying sinusoid of a few cycles with only one or two of the cycles having high peak power.

A frozen wave generator (FWG) is an alternative technique investigated for years by researchers such as Forcier *et al*.,[1] Gripshover *et al*.,[3] Best *et al*.,[2] Holzman *et al*.,[7] and Weibel *et al.,* [8] to overcome drawbacks in conventional microwave pulse generators by exploiting the ability of this device to generate a square-top, constant-amplitude, multi-cycle waveform of user-defined pulse width, covering tens-of-MHz to sub-THz center frequency range with scalability to MW-order powers in the RF domain.

A classical FWG consists of a linear, multi-switch ensemble of TL segments with alternate segments charged to opposite polarity, constituting a single cycle, as shown in Figure 12.1. Multiple pairs of segments, each with an enabling switch, are connected in series to generate a stream of RF pulses with a fixed center frequency and a narrow bandwidth. Simultaneous closure of all the switches converts the spatially stored electrostatic charge distribution to dynamic “traveling” waves moving through the line segments in opposite directions toward the load. The length of each TL segment is one-half of the wavelength of the desired radiation. In this arrangement, energy from a power supply is statically stored in alternately charged sections of the transmission lines with constant characteristic impedance Z_0 and requires ‘(n–1)’ switches for ‘*n’* segments of TLs to produce ‘n/2’ cycles of RF pulses.

For years, multi-switch embodiments of FWGs have been implemented using coax-based TLs, alternately connected to two equal valued DC power supplies (one positive and one negative) to enable bipolar pulse generation as shown in Figure 12.1. The primary drawbacks of the initial FWG embodiment are (i) the need for a separate switch between each pair of segments and (ii) their fixed center frequency. With multiple switching elements regulating the transmission line charge–discharge cycles, a few significant challenges associated with the synchronization need to be addressed to efficiently generate low-jitter RF pulses. These include synchronization of sub-nanosecond switching, external trigger, and sub-nanosecond switch impedance collapse (requires comprehensive characterization of individual switches to match the parameters exactly).

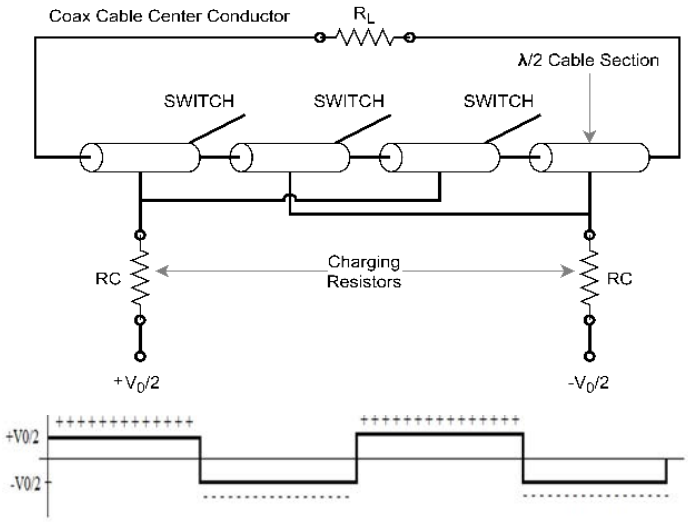

Figure 12.1. Circuit configuration of a two-cycle FWG (transmission line is replaced by a coaxial cable)

To elude this complexity, Forcier implemented a single-switch-enabled folded FWG topology where alternate coaxial transmission lines charged by a positive power supply are connected to one end of the switch, and the other set of alternate transmission lines charged by a negative power supply are connected to the other end of the switch. However, the center conductor of the coaxial transmission lines remains continuous throughout all the line segments as shown in Figure 12.2. This folded topology implemented by Best et al. and Forcier et al. offers an additional advantage of reduced switching loss that affects the first half cycle of the output pulse. Despite successful implementation of the folded topology, the use of coaxial cables limited the ability to tune center frequencies dynamically. Furthermore, Best and Forcier implemented modified stab switches and spark gaps, respectively, which were suboptimal due to their switching speeds, jitter, and device lifetime.

Typically, 50 Ω coaxial cables are used to facilitate impedance matching with the load, which is usually a radiating antenna. These cables have a velocity factor (v_f) of 0.66, capable of generating pulse widths of 5.05 ns for every meter of the coaxial cable used. Though this approach reduced the synchronization complexities, the coaxial cables with fixed lengths result in fixed pulse widths, making it infeasible to tune the frequency bands.

However, if the pairs of transmission line segments are varied in length discretely for *n*-segments, at sufficiently high *n*, a chirped output pulse train with smoothly varying $\lambda/2$ in the time domain and a moderately smooth frequency space can be realized. Forcier et al. have demonstrated this technique using coaxial cables, but the number of pulses realized experimentally was limited to 3 [1], [5]. Furthermore, if the transmission lines are made to be remotely tunable, the center frequency and the bandwidth of the system can be dynamically tuned. FWGs capable of chirped pulse widths and dynamic tunability can potentially broaden the application space of the FWG, making it a one-size-fits-all solution for pulser needs without the use of a vacuum-electron source.

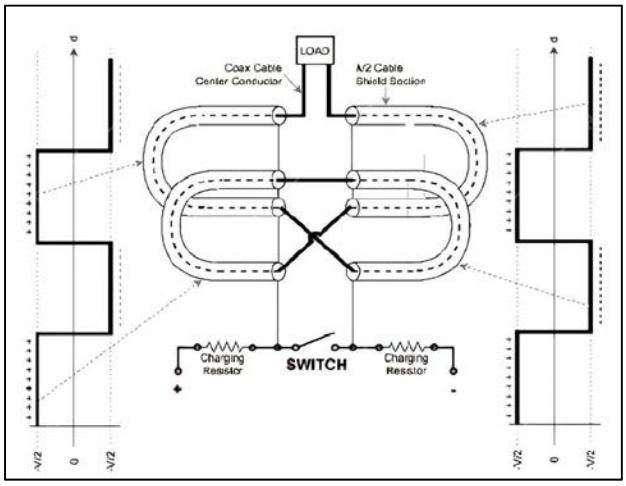

Figure 12.2. Basic architecture of a folded frozen wave generator

12.4 Tasks, Milestones, and Status

A. Simulate a chirp-capable distributed-element transmission-line-based (DETL) 16-stage frozen wave generator (FWG) with balanced and unbalanced load configurations. [JUN–JUL 2021 / complete]

B. Demonstrate a SiC-MOSFET-powered FWG prototype on a custom-built PCB with Cree/Wolfspeed MOSFET, and 50 Ω coaxial cables and/or microstrip transmission lines capable of generating chirped pulse widths. [JUL–AUG 2021 / complete].

C. Simulate a lumped-element transmission line (LETL) based FWG with up to 12 segments to replicate results from the DETL-FWG simulations. [AUG–SEP 2021 / complete]

D. Demonstrate a modular 4–8 stage SiC-MOSFET enabled FWG with lumped-element-based transmission lines with and without chirp capability. [SEP–OCT 2021 / complete]

E. Design and test a 12-segment, MOSFET-enabled FWG prototype with dynamic pulse width tunability using lumped-element-based transmission lines [NOV–DEC 2021 / complete].

F. Perform root cause analysis to determine the causes for (i) pulse overlap demonstrated by the Gen1 LETL-FWG prototype under unbalanced load configuration, and (ii) consistent reduction in the peak voltage output of the pulse train output. [JAN–FEB 2022 / complete]

G. Demonstrate motorized and/or electronically tunable DETL-FWG prototype with dynamic tunability capable of generating multiple center frequencies. [MAR–APR 2022 / suspended]

12.5 Methods and Approach

The DETL and LETL based FWG topologies were implemented computationally and experimentally under balanced and unbalanced load configurations. The literature-

standard folded coaxial topology (DETL) reported by Forcier and Best [1–2, 4–5] was realized with Cree/Wolfspeed SiC MOSFET(C2M1000170D) to establish the baseline measurements for the FWG and to calculate inductance and capacitance of the DETLs as a function of coax length. These parameters were used in the lumped-element TLs (LETLs) to mimic the behavior of the DETL-FWG characteristics with a reduced form factor. The design was modified for a 12-segment LETL-FWG to optimize the pulse widths/delays and enable dynamic tunability by including a tunable L-C pair in each LETL. The design specifics are discussed below.

A. Distributed Element Transmission Line based FWG (DETL-FWG):

A 16-stage, chirp-capable, MOSFET-switched FWG shown in Figure 12.3 was modeled in LTSpice with two load resistors, R_L and R_T. In simulations, TL segments capable of pulse widths between 0.5–3 ns were used to demonstrate chirp capability from 0.3–2 GHz. FWG performance is studied with two load configurations: (i) balanced (R_L=R_T), and (ii) unbalanced (R_L>> R_T), respectively. Given that the path of traveling waves in (i) and (ii) were distinct, crossover distortion was avoided by implementing a horizontal symmetry of TL segments for the balanced load configuration as shown in Figure 12.3(a), and a diagonal symmetry for unbalanced load as shown in Figure 12.3(b). TL segment arrangement can be distinguished by the naming convention.

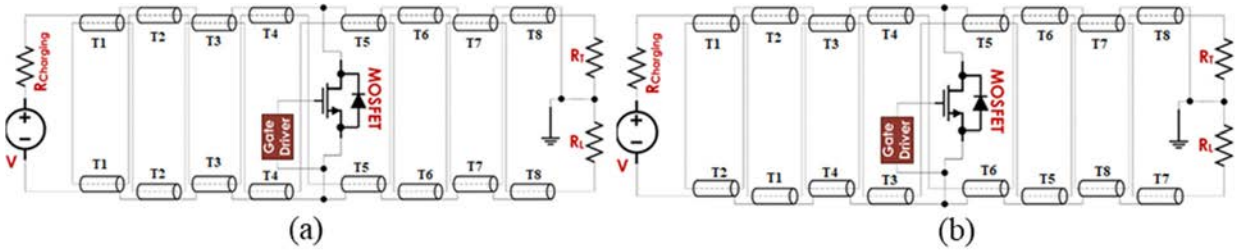

Figure 12.3. (a) A 16-stage symmetric FWG (R_T=R_L), and (b) an asymmetric FWG (R_T<< R_L), with programmable delay and ON-time.

Experimentally, the DETL-FWG topology was realized through a MOSFET-switched prototype implemented using 50 Ω coax-based TL segments with a 0.66 velocity factor. The MOSFET was rated for 10.5 ns rise-time (t_{rise}), 60 ns fall-time (t_{fall}), 1.7 kV drain-source voltage, and 1 Ω drain-source on-state resistance (R_{DS}(on)); driven by a Texas Instruments UCC5390Q1 gate driver. The implemented coaxial cable demonstrates 5.05 ns t_{pulse}/t_{delay} per meter. Figure 12.4 shows an 8-segment DETL-FWG prototype implementing four coaxial pairs of lengths 5-, 4-, 3- and 1-meters, inducing propagation delays of 25 ns, 20 ns, 15 ns, and 5 ns, respectively.

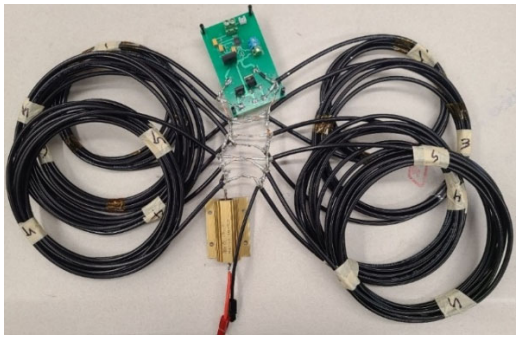

Figure 12.4. An 8-segment coax-based chirp-capable SiC-MOSFET-driven FWG.

B. Lumped-Element Transmission Line based FWG (LETL-FWG)

The DETL topologies yield length-dependent, non-tunable pulse widths that subsequently limit the application trade space of the FWGs. In addition, high-power, high-frequency DETLs are bulky and heavy with limited flexibility to minimize the form factor. To address said limitations, LETL-based FWG was designed using lumped-elements, where t_{pulse} and t_{delay} depend on the L and C parameters instead. Each TL segment was equipped with an ensemble of fixed LC cells and one tunable LC cell. Similar to DETL-FWG design, it employs a SiC-MOSFET and a UCC5390Q1 driver. The L and C parameters for each cell were precisely selected to maintain a 50 Ω characteristic impedance in each LETL segment. With L-C combination of 75 nH-30 pF generating 1.5 ns t_{pulse}/t_{delay}, their multiples were selected for LETL cells. The t_{pulse} of each segment can be tuned individually by varying the L and C parameters in the tunable cell(s), which subsequently tunes the center frequency (f_c).

12.6 Results and Discussion

A chirp-capable coax-based design was implemented with 4-, and 8-segment TL topologies under balanced and unbalanced load configurations.

A four-segment FWG topology implemented with two coax cables of 4 m each, and the other two of 5 m each demonstrated ~20 and ~25 ns pulse widths, respectively, under balanced and unbalanced load configurations with chirp based on the lengths of the coaxial cables. A center frequency of ~20 MHz was noticed in the unbalanced load configuration for the unipolar pulse train generation with voltage swings between +160 and –220 V, while in the balanced load with bipolar pulse train generation, it was noticed to be ~ 75 MHz with voltage swings between –170 and +170 V as shown in Figure 12.5. Furthermore, when the number of TL segments is increased to eight with coax pairs of lengths 5, 4, 3 and 1 m, a significantly lower peak voltage swing was observed alongside ringing towards the tail with frequencies chirping between 15 and 70 MHz were noticed.

With an increase in number of transmission line segments, an increase in pulse overlap and pulse deformation due to deconstructive interference was noticed under unbalanced load conditions, and the load measurements start to deviate from the expected waveform when the number of segments is >8. Significant ringing was observed when 8 and more TL segments were used under balanced load conditions, caused due to the impedance mismatch between the transmission line ensemble and the load.

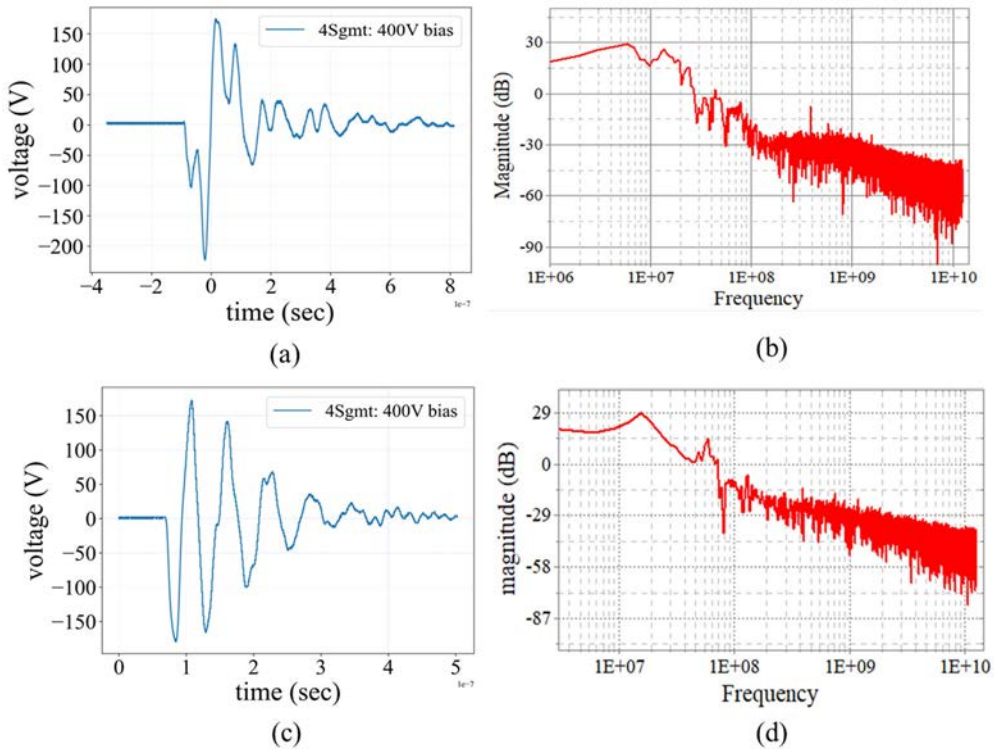

Figure 12.5. (a) 4-segment FWG load characteristics under unbalanced load, (b) frequency domain representation of (a), (c) 4-segment FWG load characteristics under balanced load, and (d) frequency domain representation of (a)

Extending the literature-standard work, LETL-FWG prototypes were experimentally verified for eight-, and twelve-segment configurations under balanced and unbalanced loads using folded FWG topology with one power supply and switched using a Cree/Wolfspeed C2M1000170D SiC-MOSFET. The LC parameters were selected such that the characteristic impedance of the line is maintained at 50 Ω, while waveform tunability was introduced in the 12-segment FWG prototype by including a mechanically-tunable inductor capacitor pair (highlighted in red) in each transmission line segment as shown in Figure 12.6

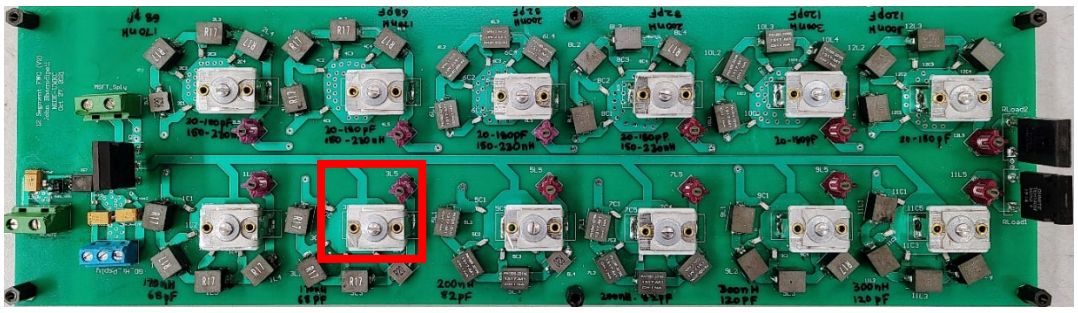

Figure 12.6. Twelve-segment dynamically-tunable LETL-FWG prototype switched using Cree/Wolfspeed C2M1000170D MOSFET, driven using a Texas Instruments UCC5390Q driver.

In the 8-segment FWG, 4 segments were loaded with 4 cells of 270 nH – 102 pF each and the other 4 were loaded with 4 cells of 150 nH – 62 pF, capable of generating 21 ns and 12 ns pulse width/delay, respectively. When tested at 400 V under unbalanced configuration, issues with pulse overlap were noticed. Though the pulse train in one polarity represented the expected waveform from the simulations, the reflected waveform failed to demonstrate similar properties. A significant pulse-train overlap has been noticed in the unbalanced load configuration. Despite demonstrating the center frequencies >70 MHz, the unbalanced load configuration demonstrated pulse overlap due to the non-aligned charge–discharge cycles of the LETLs, limiting the frequency content of the FWG.

A twelve-segment Gen-I non-chirp-capable prototype (shown in Figure 12.6), when tested at 400 V bias under balanced load configuration with 4 cells of 300 nH – 120 pF in each segment has shown a consistent temporal waveform in-line with the simulation results. However, a consistent drop in the peak voltages has been observed under balanced load as shown in Figure 12.7. With an increase in the number of TL segments, the inability of the MOSFET to perform simultaneous switching of all the transmission lines has been elevated, leading to decreased charge time due to delayed opening and prolonged high-charge state due to delayed closing. The placement MOSFET at one end of the FWG was speculated to be the root cause, leading to switching delays.

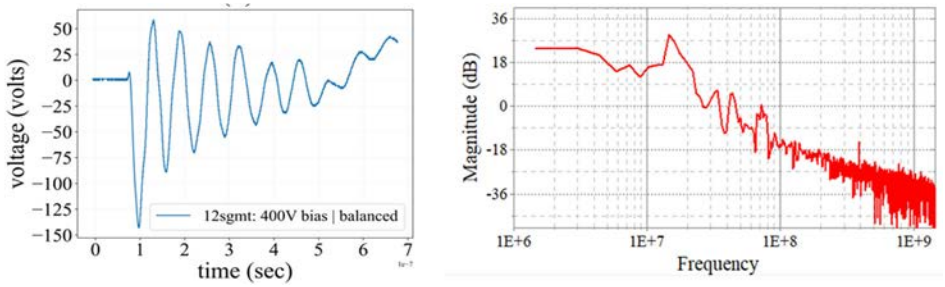

Figure 12.7. (left) Load characteristics of a 12-segment fixed pulse width LETLs with 4× 300nH-120pF LC ladder cells in each segment, capable of generating 24 ns pulse width,(right) frequency domain representation

To confirm this speculation, a Gen II 12-segment FWG was designed with modified MOSFET placement as shown in Figure 12.8 to minimize switching delays. The characteristic impedance of the LC ladder networks was set to 50 Ω and the fixed LC components were selected to generate pulse widths between ~13 and ~24 ns, and additional tunable LC components in each segment add 2 – 5 ns. Anticipated pulse width(s) were measured under balanced (50 Ω and 50 Ω) load configuration as shown in Figure 12.9.

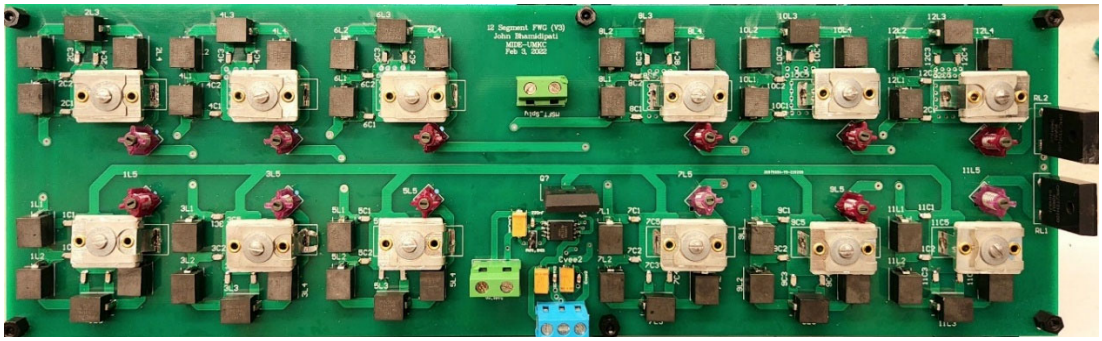

Figure 12.8. Gen 2 prototype with modified MOSFET and gate driver layout.

Nevertheless, the Gen II prototype with updated MOSFET (results shown in Figure 12.9) did not show a significant improvement in peak voltage trends of the output wave packet. The rise-time of the MOSFET being ~10.5 ns is determined to be too slow to perform simul-switching of the transmission lines, raising a need for a switch with sub-ns rise-time and ns-order fall-time.

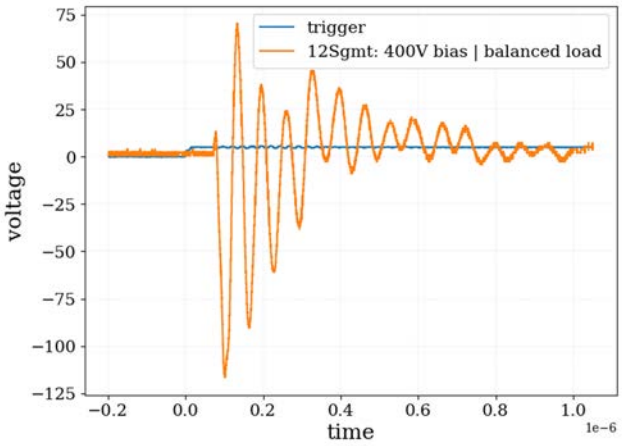

Figure 12.9. 12-segment balanced load FWG output when the lines are charged to 400 V. Each transmission line segment has been loaded with 4x 300nH-120pF LC ladder cells, capable of generating 24 ns pulse width.

Switches such as PCSSs and drift step recovery diodes (DSRDs) with sub-ns pulse characteristics can be potentially implemented to address this limitation if a compact, lightweight trigger mechanism is developed. Furthermore, remote tunability can be made possible by including an MCU/ECU controlled tunable L-C pair in each TL segment.

12.7 Summary and Recommendations

The chirp- and dynamic-tuning-capability of an all-solid-state FWG was realized on a 7.5-cm × 30-cm × 3-cm printed circuit board via a 12-segment LETL embodiment. Dynamically-tunable pulse trains with 15–24 ns pulse widths (40–80 MHz) were realized with >35% pulse conversion efficiency at $<2\times10^{-4}$ m^3 volume, yielding >80% reduction in volume compared with vacuum-relativistic pulsers. Replacing the DETLs in literature-standard coax-based topology with lumped elements enabled tunability, enhanced

robustness, and yielded >60% reduction in size and weight. Transient characteristics of the enabling switch (MOSFET) in terms of t_{rise} and t_{fall} were noticed to be the limiting factors to attain flat-top pulse trains. Furthermore, a need for >11 ns pulse width/delay to be compatible with rated t_{rise} of the MOSFET capped the frequency response of the pulser at <100 MHz. A solid-state switch analogous to PCSS capable of sub-ns t_{rise} with low jitter and compact trigger mechanism would greatly benefit the solid-state LETL topology of the FWG.

12.8 Outputs

12.8.1 *Journal Publications*

J. K. P. Bhamidipati, K. C. Durbhakula, and A. N. Caruso, "A Dynamically Tunable Discrete-Element Transmission Line Pulse Generator," *International Journal of Electronics and Communications*, Submitted March 6 **2022**, Manuscript ID#AEUE-S-22-01270.

12.8.2 *Dissertation*

John Keerthi Paul Bhamidipati, "Pulse Generation, Shaping, and Optimization Solutions for Solid-State-Switch-Enabled High-Power Microwave Generation Systems" PhD Dissertation in Physics and Electrical Engineering, University of Missouri-Kansas City, **2022**.

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ONR HPM Program – Monthly Status Report (MSR) – June 2022

Anthony Caruso – Univ. Missouri – Kansas City

N00014-17-1-3016 [OSPRES Grant]

ONR Short Pulse Research, Evaluation and non-SWaP Demonstration for C-sUAS Study

15 JULY 2022

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OSPRES Grant Goal: address and transition technologies and capabilities that enable the OSPRES Grant Objective using the OSPRES Grant Approach, while educating the next generation of pulsed power and defense minded, stewards and innovators.

OSPRES Grant Objective: to execute high-risk, high-payoff efforts that mitigate, fill or rectify one or more grand-challenge or elementary gaps or deficiencies needed to achieve a modular, scalable and electronically steerable high-power microwave (HPM) based defense system for the counter unmanned aerial system (cUAS) mission. The OSPRES HPM system and sub-system development/evaluation efforts are focused on the short-pulse high-average-power space and includes the kill chain considerations including the target and its responsivity to radiofrequency stimuli.

OSPRES Metrics of Success: developed technologies and capabilities that are published in the peer review, protected as intellectual property, and/or, transitioned to the OSPRES Contract effort and beyond for integration with other DoD needs or dual-commercial-use, as enabling/integrable capability(ies).

OSPRES Grant Approach: A fail-fast philosophy is maintained, where if a technology or capability is deemed infeasible to be demonstrated or validated during the project period-of-performance, it shall be culled, results to date and basis of infeasibility documented, and the next major gap/deficiency area addressed by that part of the project sub-team. Students whose thesis depends on following through with a full answer during the life of the award will be given special dispensation to continue their work.

OSPRES Grant Security: All efforts should be fundamental and publicly releasable in nature when taken individually. This report has been reviewed for operational security, compilation, proprietary and pre-decisional information concerns.

1 Contents

2 Executive Summary

2.1 Progress, Significant Findings, and Impact

Fiber Laser and Optical Amplifiers. Our beam shaping, optical power combiner designs are a spin-off of our tubular optical power amplifier innovations. They utilize “photonic crystal” effects, which have led to less dispersion in optical fiber, as well as increased gain and steerability in patch antennas. We broaden their narrow-band resonances in order to open the door to a means of extending reconfigurable patch antenna techniques to dual ridged horn antennas at RF (simply by lining more tubes of glass inside the wall of an outer tube). By extending the length of the waveguides in our simulations we have revealed new physics, including the surprising creation of high intensity surface waves at the air/glass interfaces. These surface waves have a dramatic impact on the output beam profile (by creating strikingly narrow spikes or pencil beams, which could be exploited in directed energy systems due to their highly localized nature. These are special waves which “hug” the material interface (rather than reflect from it) as do so-called “creeping waves” which have been observed previously, but such require conductivity. To our knowledge, this is the first prediction that something similar can happen at a non-conducting dielectric interface. The Kerr nonlinearity of glass (at optical frequencies) enhances the creation of surface waves (by a factor of up to 6) but it is not essential. Thus, such effects must be readily transferrable to RF radiators as well because they exist even in the case of no Kerr nonlinearity. Metallic tubes could generate creeping waves at RF but surface waves from glass would improve the SWaP.

DSRD Optimization Simulations. Accurately fit drift-step-recovery diode (DSRD) testing data is necessary for the accurate DSRD models used for the design and optimization of DSRD-based pulser modules for achieving maximum possible peak power (2 MW per module) while maintaining low risetimes (~2 ns at 4 kV peak voltage). New Keithley 2450 forward IV data has been successfully fit within the LTspice standard diode model that extends the current up to 1 A. The SmartSpice Compact Modeling Committee (CMC) Verilog-A diode model code has been successfully modified to implement a sectional forward IV model that fits the non-standard forward IV of EG DSRD. The new sectional forward IV data was used within a SmartSpice Verilog-A 1x1 DSRD-based pulser simulation, producing the correct pulse shape and pre- and post-pulse effects. New fitting of recovery parameters to the new sectional forward IV will produce very closely matched pulse characteristics.

DSRD Processing and Manufacturing. A step of the DSRD die side passivation process using a stain etch has been further developed. FIB-SEM images of the porous film cross sections have been obtained and show an average pore diameter of about 100 nm and average silicon wall thickness between neighboring pores of about 30 nm. The total depth of the porous silicon layer exceeds 5 microns.

DSRD Design of Experiments. Breakdown testing and series resistance are two significant factors in selecting manufactured DSRDs for peak pulser performance. Toward obtaining accurate and useful DSRD electrical characterization data, forward IV curves have been and are being collected using both Keithley 2450 and Tektronik 371 instruments for the Gen2 and EG DSRDs. After testing and optimizing fixture, cabling,

and DSRD clamping, a new forward IV procedure has been developed, and the 2450 and 371 forward IV measurements align well to combine into a complete forward IV data set spanning the ranges of voltage and current of interest in DSRD-based pulsers. Series resistance has been found to vary over its range by a factor of two, which affects pulser peak voltage also by a factor of two.

DSRD-Based Pulsed Power Source Optimization. As continuation of the modular pulser design, a schematic and working principle of a 2×1 pulser design (two independent 1×1 pulsers stacked in parallel) has been presented, which can produce ~20 kV of output pulse, however, with the expense of 4 times the total number of diodes. Unlike in a series stacked pulser, this design does not require more powerful (high current, high open voltage) MOSFETs. A newly designed and populated 1×1 pulser utilizing three seven stack diodes produced 6.2 kV of output. The inaccuracy in the measurements of diode series resistance, inductance of custom-built inductor, and DSRD SPICE modelling are believed to be the factors that are limiting the experimental output to reach the theoretically expected result. Greater efforts in inductor modelling, fabrication, and measurements, as well as diode resistance measurements have been applied using impedance spectroscopy. A custom-built inductance measurement fixture has been designed that minimizes the stray inductance and capacitance.

Pulse-Compression-Based Signal Amplification. Time reversal pulse compression (TR PC) methods were investigated as an alternative PC-based signal amplification method. TR PC shows a few dBs of gain in the time domain but loss in the frequency domain. One-bit time reversal (OBTR) PC, which increases the time domain gain to ≥ 20 dB, shows ~3x gain in the frequency domain at some frequencies but completely distorts the output signal. The impulse response record time significantly affects the compression gain and limits the pulse repetition frequency. The compression gain also drops significantly for narrowband signals. Time-reversal-based pulse compression methods were found to be incompatible with GaN source, especially due to their limited pulse repetition frequency and low compression gain for narrowband signals.

Antennas. A tapered, coaxial-connector-fed, small, wideband, microstrip patch antenna for operation in the UHF (0.7–1.2 GHz) region was manufactured and tested. Preliminary test results showed reasonable agreement with the simulated data despite manufacturing defects and electromagnetic discontinuities in the prototype. This is a transformative step showing the proposed wideband, electrically small, microstrip patch antenna design technique is applicable at operating frequencies in the UHF (MHz) to microwave (GHz) frequency ranges. An updated version of the prototype is currently being modeled for manufacturing and is expected to mitigate the fabrication errors. A successful testing of the modified design will be followed by the manufacturing of the final demonstrable array prototype.

A new gradient refractive index (GRIN) style impedance transformer has been designed, integrated into the Koshelev antenna, and optimized for the best reflection coefficient (S_{11}) and gain performances. The results from the integrated and optimized Koshelev–transformer design agreed closely with the standalone Koshelev antenna design over the frequency spectrum of interest (0.5 to 2 GHz). The new integrated simulation effort

(antenna + transformer) unfolds a new pathway to perform electromagnetic (EM) wave simulations without introducing additional power loss.

The in-house machine learning (ML)-based graphical user interface (GUI) has been subjected to additional tests by employing the tool on a new horn antenna design conjugated with a GRIN lens. The ML tool was able to accurately predict the frequency domain gain performance of the new antenna design with a root mean square error value of 0.42. The predictive capabilities of the tool have now been tested on at least two different antenna designs validating the robustness of the in-house ML tool. The tool helps predict antenna performance metrics in a shorter time than traditional EM solvers.

2.2 Completed, Ongoing, and Cancelled Sub-Efforts

	Start	End
2.2.1 *Ongoing Sub-Efforts*		
GaN:C Modeling and Optimization	OCT 2017	Present
Diode-Based Non-Linear Transmission Lines	FEB 2018	Present
Trade Space Analysis of Microstrip Patch Arrays	FEB 2019	Present
Lasers and Optics	FEB 2020	Present
UWB Antenna Element Tradespace for Arrays	MAY 2020	Present
Si-PCSS Contact and Cooling Optimization	JAN 2021	Present
Drift-Step Recovery Diode Optimization Simulations	JAN 2021	Present
DSRD-Based IES Pulse Generator Development	APR 2021	Present
Drift-Step Recovery Diode Manufacturing	MAY 2021	Present
DSRD Characterization through Design of Experiments	MAY 2021	Present
Sub-Nanosecond Megawatt Pulse Shaper Alternatives	MAY 2021	Present
Ultra-Compact Integrated Cooling System Development	MAY 2021	Present
Continuous Wave Diode-NLTL Based Comb Generator	SEPT 2021	Present
Pulse-Compression-Based Signal Amplification	DEC 2021	Present
2.2.2 *Completed/Transferred Sub-Efforts*		
Adaptive Design-of-Experiments	OCT 2017	APR 2019
Non-perturbing UAV Diagnostics	OCT 2017	OCT 2018
Noise Injection as HPM Surrogate	OCT 2017	MAR 2019
SiC:N,V Properties (w/ LLNL)	APR 2018	MAR 2019
Helical Antennas and the Fidelity Factor	JUL 2018	SEPT 2019
Si-PCSS Top Contact Optimization	APR 2020	OCT 2020
Nanofluid Heat Transfer Fluid	NOV 2020	JUL 2021
HV Switch Pulsed Chargers	DEC 2018	DEC 2021
Enclosure Effects on RF Coupling	OCT2019	DEC 2021
UAS Engagement M&S	MAR 2021	DEC 2021
GaN-Based Power Amplifier RF Source	AUG 2021	DEC 2021
2.2.3 *Cancelled/Suspended Sub-Efforts*		
Ab Initio Informed TCAD	OCT 2017	OCT 2020
Positive Feedback Non-Linear Transmission Line	NOV 2017	DEC 2018
Minimally Dispersive Waves	FEB 2018	SEPT 2018
Multiferroic-Non-linear Transmission Line	NOV 2018	APR 2019
Avalanche-based PCSS	SEPT 2018	SEPT 2019
Gyromagnetic-NLTL	DEC 2017	NOV 2020
Multi-Stage BPFTL	APR 2020	JUL 2020
Heat Transfer by Jet Impingement	MAY 2018	FEB 2021
Si, SiC, and GaN Modeling and Optimization	NOV 2018	FEB 2021
Bistable Operation of GaN	FEB 2021	MAR 2021
WBG-PCSS Enabled Laser Diode Array Driver	NOV 2020	JAN 2022

2.3 Running Total of Academic and IP Program Output

See Appendix for authors, titles and inventors (this list is continuously being updated)

Students Graduated	*6 BS, 9 MS, 4 PhD*
Journal Publications	*6 (6 submitted/under revision)*
Conference Publications	*35 (3 submitted/accepted)*
External Presentations/Briefings	*40*
Theses and Dissertations	*5*
IP Disclosures Filed	*10*
Provisional Patents Filed	*4*
Non-Provisional Patents Filed	*0*

3 Laser Development

3.1 Fiber Lasers and Optical Amplifiers

(Scott Shepard)

3.1.1 *Problem Statement, Approach, and Context*

Primary Problem: High-average-power 1064-nm picosecond lasers are too large (over 1100 cm^3/W) and too expensive (over \$1000/μJ per pulse) for PCSS (photoconductive semiconductor switch) embodiments of HPM-based defense systems. For example, a laser of this class might occupy a volume of 1 m x 30 cm x 30 cm = 90,000 cm^3 and provide an average power of 50 W (thus, 1800 cm^3/W). Costs in this class range from \$100K to \$300K to drive our Si-PCSS applications.

Solution Space: Optically pumped ytterbium-doped optical fiber amplifiers, fed by a low-power stable seed laser diode, can offer a cost-effective, low-weight, and small-volume solution (with respect to traditional fiber and traditional free-space laser designs). Moreover, our novel optical amplifier tubes, might operate at far higher power levels (over 1000 times greater), thus driving an entire array of PCSS with a single amplifier and thereby reducing the overall system costs and eliminating the optical pulse-to-pulse jitter constraints.

Sub-Problem (1): Optical pump power system costs account for over 50% of the budget for each laser (in this class, for normal/free-space, optical fiber, and tubular embodiments).

Sub-Problem (2): Fiber (as well as power tube) optical amplifier performance is degraded primarily by amplified spontaneous emission (ASE) noise, which limits the operating power point, and by nonlinearities, which distort the optical pulse shapes.

State-of-the-Art (SOTA): Free-space NdYAG lasers or Ytterbium-doped fiber amplifiers optimized for LIDAR, cutting, and other applications.

Deficiency in the SOTA: Optical pump power system costs (in either free-space or fiber lasers) are prohibitive for the PCSS applications until reduced by a factor of at least two.

Solution Proposed: Fiber lasers permit a pre-burst optical pumping technique (wherein we pump at a lower level over a longer time) which can reduce pumping costs by a factor of at least ten. To address the ASE and nonlinear impairments, we are pursuing the use of gain saturation and a staged design of different fiber diameters. We also apply these techniques to fiber amplifiers which incorporate our power amplifier tube in the final stage. The inclusion of our novel tubular-core power amplifier stage should permit a single laser to trigger an array of several PCSS (reducing system cost and mitigating timing jitter).

Relevance to OSPRES Grant Objective: The enhancement in SWaP-C^2 for the laser system enables PCSS systems for viable deployment via: a factor of 40 in pumping cost reduction of each laser; and a factor of *N* in system cost reductions as a single laser could drive *N* (at least 12) PCSS in an array, while also eliminating the optical jitter constraints.

Risks, Payoffs, and Challenges: Optically pumping outside the laser pulse burst time can enhance the ASE; pump costs could be reduced by 40, but ASE in the presence of dispersion and/or nonlinearities could enhance timing jitter thereby limiting steerability. The main challenge for power tube implementation is the entrance optics design.

3.1.2 *Tasks and Milestones / Timeline / Status*

(A) Devise a pre-burst optical pumping scheme by which we can reduce the costs of the laser by a factor of two or more and calculate the resulting increase in ASE. / FEB–JUL 2020 / Completed.

(B) Reduce the ASE via gain saturation. / Oct 2020 / Completed.

(C) Design saturable gain devices which avoid nonlinear damage. / Ongoing.

(D) Calculate and ensure that timing jitter remains less than +/-15 ps with a probability greater than 0.9. / Ongoing.

(E) Demonstrate a cost-reduced fiber laser: the level of success to be quantified via the amount of ASE growth per duration of a pre-burst pumping interval. Growth of 100 uw over 6 ms (the limit in theory) would be considered outstanding. / August 2022.

(E1) March 2021 Finalize design. / Completed.
(E2) April 2021 Assemble and test-check seed LD (laser diode)/driver. / Completed.
(E3) April 2021 Measure power vs current transfer function of seed LD/driver. / Completed.
(E4) May–July 2021 Measure ASE and jitter of 1064 nm seed LD/driver. / Completed.
(E5) May–July 2021 Measure ASE and jitter of 1030 nm seed LD/driver. / Completed.
(E6) June–July 2021 Assemble and test-check pump LDs/drivers. / Completed.
(E7) June–July 2021 Measure power vs current transfer function of pump LDs/drivers. / Completed.
(E8) July–September 2021 Splice power combiners to Yb doped preamp fiber. /Completed.
(E9) July–September 2021 Connect seed and pumps to power combiners and test-check. / Completed.
(E10) September–October 2021 Measure gain, ASE and jitter of 1064 nm preamp assembly (forward, backward and bidirectional pumping) as a function of pump power and duty cycle. / Partially completed before task eliminated.
(E11) September–October 2021 Measure gain, ASE and jitter of 1030 nm preamp assembly (forward, backward and bidirectional pumping) as a function of pump power and duty cycle. / Partially completed before task eliminated.
(E12) November 2021 Splice power amplifier and its power combiner to best preamp. / Partially completed before task eliminated.
(E13) May–August 2022 Measure gain, ASE and jitter of entire amp assembly. / Ongoing.
(E14) May–August 2022 Analyze data and document. / Ongoing.

(F) Design a new type of higher power, tubular core fiber amplifier. / May–August 2022.

(F1) Apply one high-power tubular amplifier to a system comprised of an array of several (say N) PCSS. For example: N=12 in a 3x4 array (or 4x4 array with corners omitted) N=16 in a 4x4 array, etc.; thereby eliminating jitter constraints and reducing laser system cost by more than a factor of 100 (independent of burst profile). / August 2022.

(F2) Design a high power, multiple tube optical amplifier and determine if it permits advantages for power handling or beam profile. / August 2022 / Initiated.

(G1) Design a beam shaping, optical power combiner using a cladding of 6 tubes. / June 2022 / Initiated.

(G1.1) Develop COMSOL models. / April 2022 / Completed.

(G1.2) Discover and optimize the length at which the cladding modes couple maximal power into the core mode (of the entire waveguide). / June 2022 / Partially completed.

(G2) Design a beam shaping, optical power combiner using a cladding of 6 tubes surrounding one inner tube. / July 2022 / Initiated.

(G2.1) Develop COMSOL models. / April 2022 / Completed.

(G2.2) Discover and optimize the length at which the cladding modes couple maximal power into the inner tube. / July 2022 / Partially completed.

(G3) Develop spectral combiners based on multiple-tube waveguides and compare to existing PCF (photonic crystal fiber) technologies. / August 2022 / Partially completed.

3.1.3 *Progress Made Since Last Report*

(G1.2) (G2.2) Our beam shaping, optical power combiner designs are a spin-off of our tubular optical power amplifier innovations. They utilize “photonic crystal” effects which have led to less dispersion in optical fiber; and increased gain and steerability in patch antennas. Our optical power combiner research, on capillary-sized tubes [hundreds of microns], also opens the door to a means of extending reconfigurable patch antenna techniques to dual ridged horn antennas via larger sized tubes [tens of centimeters] at RF.

Fig. 3.1.1 shows our “6-tube” design, with a cladding of 6 tubes, on the left; and a “7-tube” design, with a cladding of 6 tubes surrounding one inner/7^{th} tube, on the right. Photonic crystal effects are known to have narrow-band resonances and fiber resembling the 6-tube design (called negative curvature fiber) have led to broader-band performance. They also tend to suppress the higher-order modes, which leads to better beam quality. In our optical power combiner applications we study the mode coupling among beams launched into the various tubes and how these combine to form a single output beam. By extending the length of the waveguides we have revealed new physics (detailed in 3.1.4) including the surprising creation of high intensity surface waves at the air/glass interfaces. These surface waves have a dramatic impact on the output beam profile which could be exploited in Directed Energy systems due to their highly localized nature.

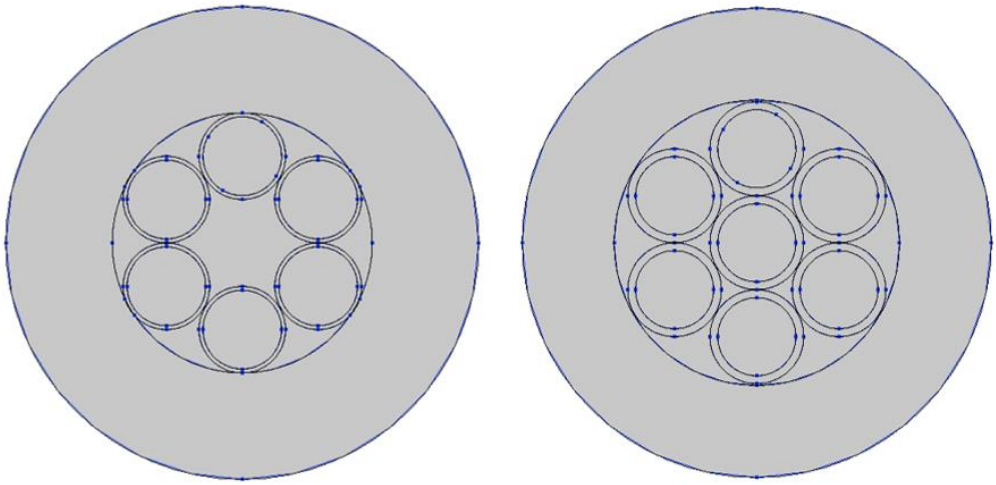

Fig. 3.1.1. 6-tube (left) and 7-tube (right) power combiner geometries.

3.1.4 *Technical Results*

(G1.2) (G2.2) We optimize the combiners over ranges of: tube radius; tube wall thickness; optical input intensity; and wavelength. In the following we consider illumination via one Gaussian beam launched into either the top (inner) tube or the center of the overall guide. The tubes (referred to herein as “cladding”) are BK7 glass of nonlinear refractive index as per all of our previous self-focusing studies and all other regions (referred to herein as “core”) are air.

We first consider illumination from the core of the top tube. Fig. 3.1.2 shows the evolution of the electric field in the center of that top core as a function of the waveguide distance (where “arc length” is in normalized units described in previous MSRs). The different curves correspond to different wavelengths from 1 to 2.5 microns and we notice these are roughly independent of that wavelength. We observe the decrease of field strength due to the energy coupling into the other modes and note the abrupt behavior at a normalized distance of x = 20 – which we will identify in the following.

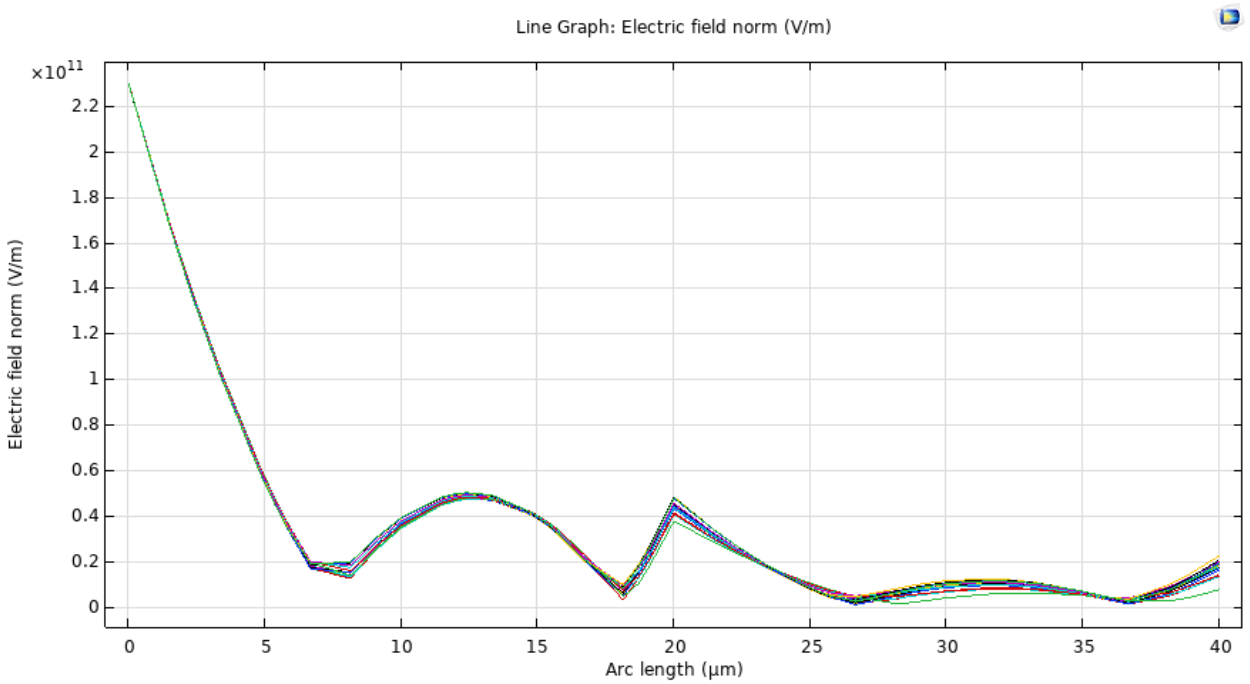

Fig. 3.1.2. Electric field in the top core vs normalized distance down the waveguide.

The field coupled into the core of an adjacent tube, as shown in Fig. 3.1.3, exhibits wavelength dependence due to the coupling between the two glass claddings (as one might anticipate). We again observe an abrupt discontinuity of field slope at a distance of x = 20. This is suggestive of the creation of surface charge, but we will soon show that something far more unusual is beginning to occur. Note in passing that our previous studies only went out to a distance of x = 10. By going further we had to endure an increase in computation time but our patience is rewarded as we reveal new physics.

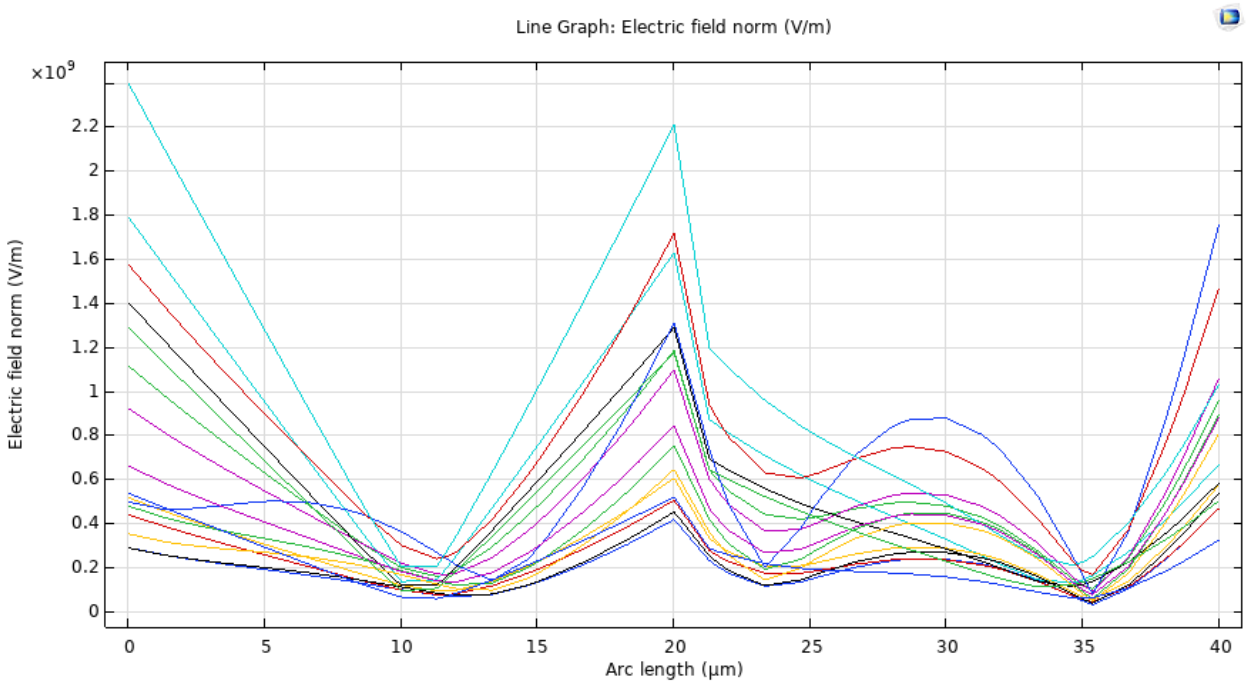

Fig. 3.1.3. Electric field in an adjacent core vs normalized distance down the waveguide.

The field coupled into the central core of the entire waveguide is shown in Fig. 3.1.4 from which we see that we will have to go even further in x to accomplish the task of finding the maximal power transfer point. Although the central core field strength at the output is of respectable size, we launched such a high intensity beam that the output from that tube is still two orders of magnitude larger (hence this central spot in the output plane of a standard COMSOL 2D plot would not be noticed, so these cutline plots are essential to this analysis). We also note the onset of periodicity in the discontinuity of field slope.

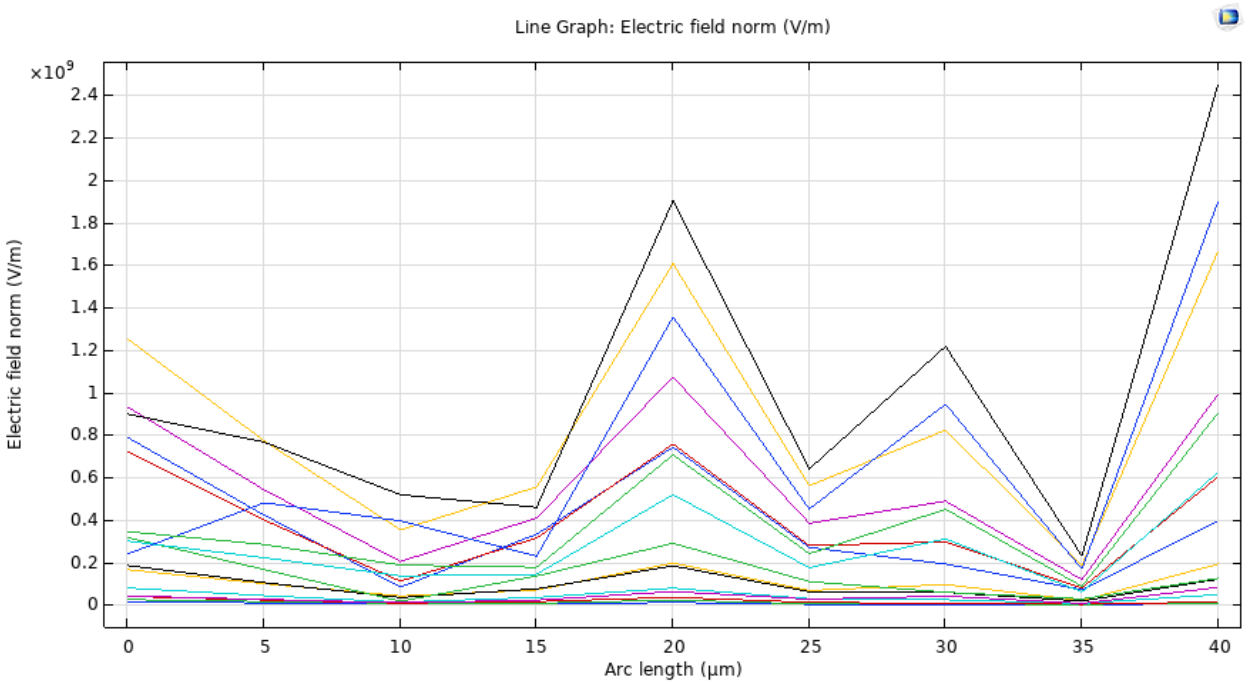

Fig. 3.1.4. Electric field in the central core vs normalized distance down the waveguide.

The field evolution in the outermost cladding (outermost glass tube) is shown in Fig. 3.1.5. This reveals something even more unusual – the field itself is almost discontinuous near x = 20. This almost instantaneous drop in energy within the glass must mean that energy is going somewhere else, so we examine the transverse (rather than longitudinal) field distribution at x = 20 in Fig. 3.1.6.

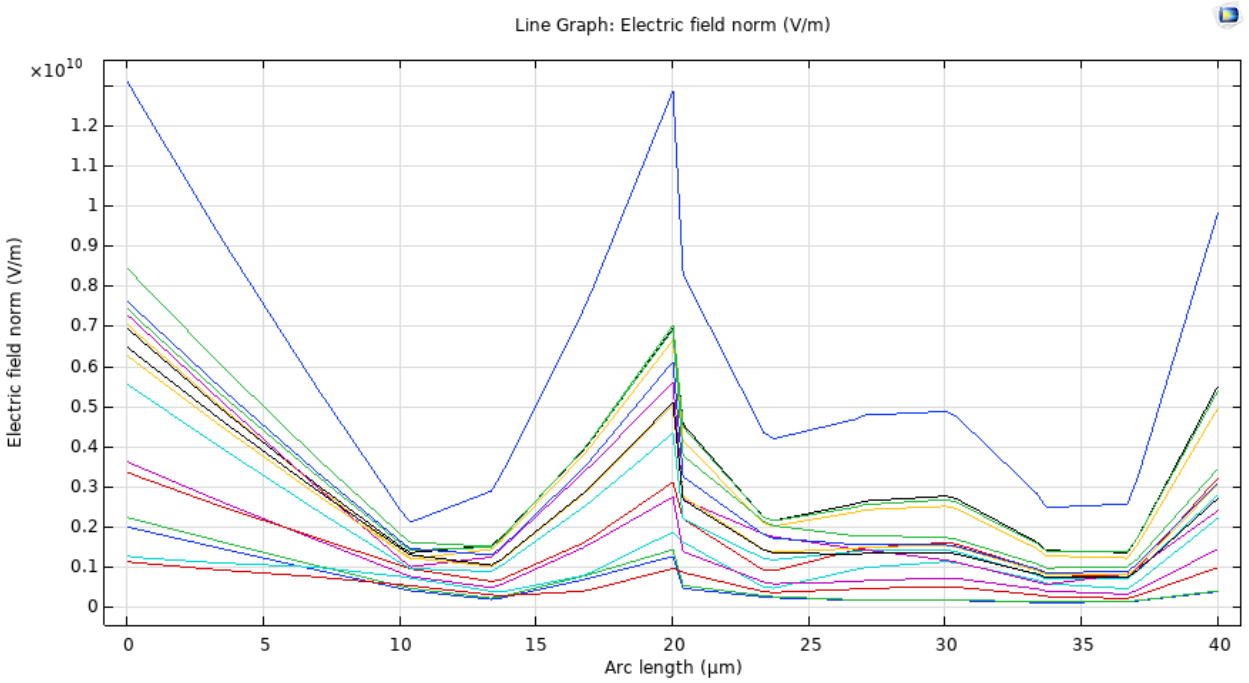

Fig. 3.1.5. Electric field in the central core vs normalized distance down the waveguide.

In Fig. 3.1.6 the x-axis is now the cross-sectional height (i.e., the z-axis of Fig. 3.1.1) so we see the Gaussian towards the right corresponding to the dominant field coming out of the top tube (where it was launched). The strikingly narrow “spikes” on each side of the Gaussian correspond to being exactly at the air/glass interfaces of that tube! Thus, these are “surface waves” which suddenly originate at that distance down the waveguide. These are special waves which “hug” the material interface (rather than reflecting from it). So-called “creeping waves” have been observed, but such require conductivity (personal communication: MIT professor Jin Au Kong). To our knowledge this is the first prediction that something similar can happen at a non-conducting dielectric interface.

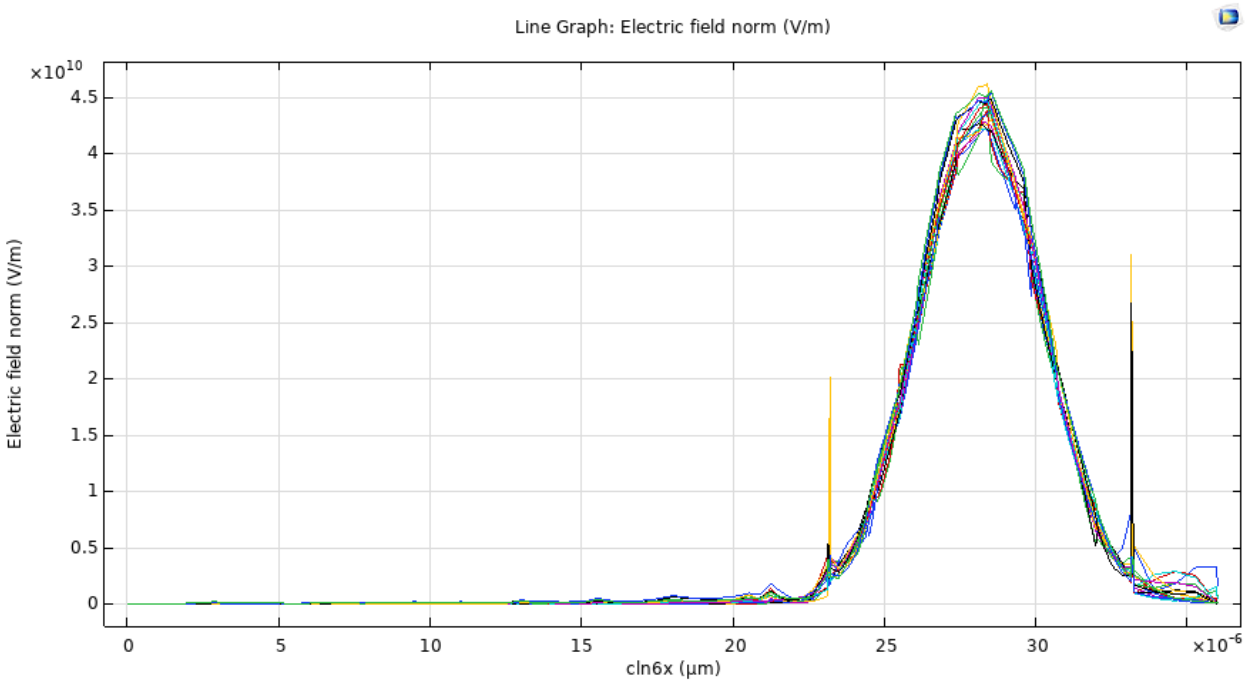

Fig. 3.1.6. Electric field vs normalized transverse distance across the waveguide (at a normalized waveguide length of 20).

Our simulations show that they do not require the Kerr nonlinearity of the glass, but they are greatly enhanced by it (by a factor of up to 6 seen to date). They continue to grow (at the expense of energy in the core) as we increase the waveguide length (from 20 [au] in Fig. 3.1.6 to 40 [au] in Fig. 3.1.7). In Fig. 3.1.7 we observe that the surface wave field can exceed that of the Gaussian core. Moreover, their extremely small “spot size” generates an extremely high intensity. These surface waves have a dramatic impact on the output beam profile which could be exploited in Directed Energy systems due to their highly localized nature. Such effects must be readily transferrable to RF radiators as well because they exist even in the case of no Kerr nonlinearity. Metallic tubes could generate creeping waves at RF but these surface waves from glass would improve the SWAP.

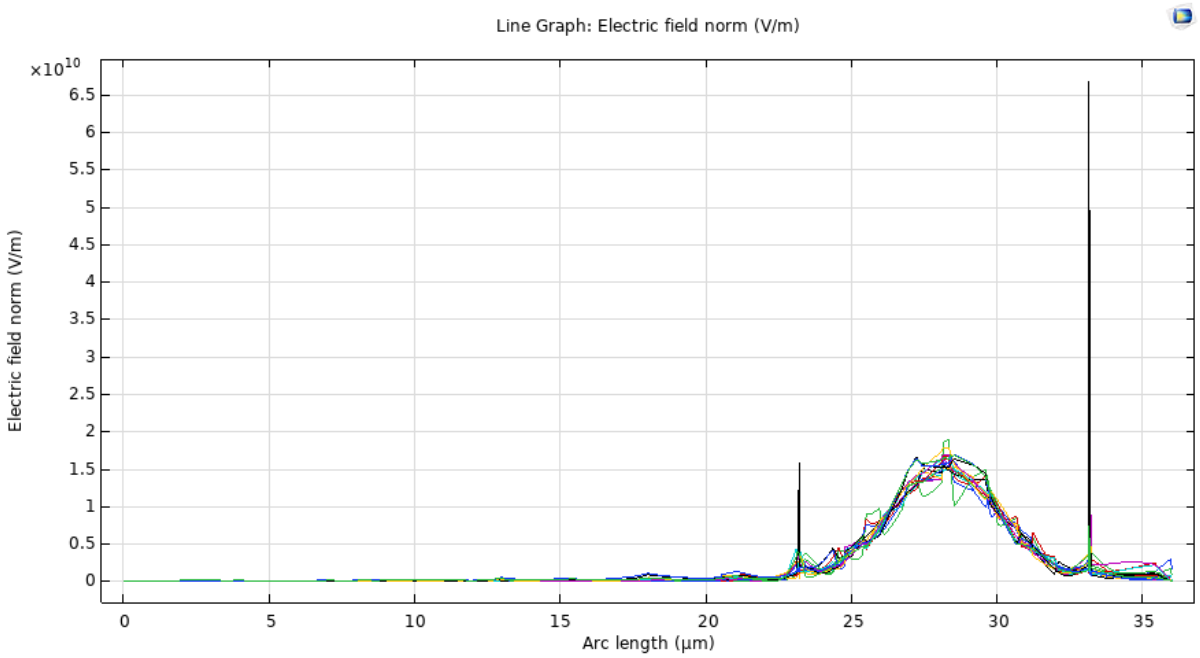

Fig. 3.1.7. Electric field vs normalized transverse distance across the waveguide (at a normalized waveguide length of 40).

We demonstrate in Fig. 3.1.8 that an output almost exclusively comprised of surface waves is achievable. In Fig. 3.1.8 this was created by illuminating the center of our 7-tube design. Noticeably, no output Gaussian beam is discernable as virtually all of the energy has gone into the surface waves which have created these “pencil beams.”

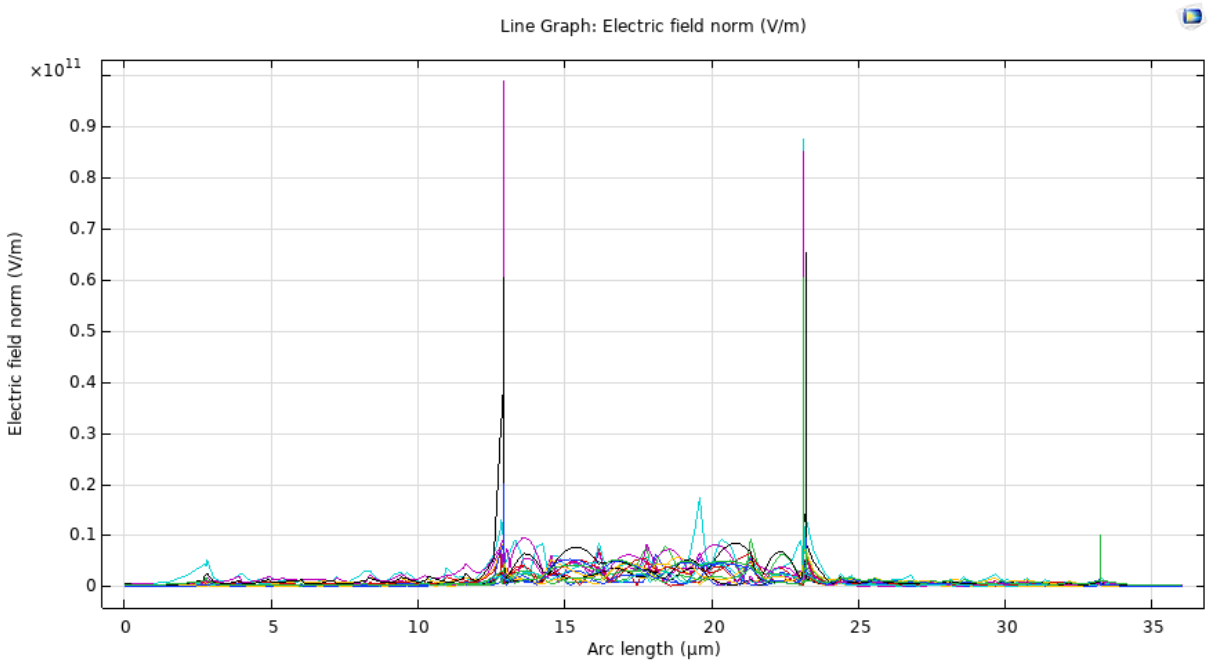

Fig. 3.1.8. Electric field vs normalized transverse distance across a 7-tube output.

3.1.5 *Summary of Significant Findings and Mission Impact*

(A) Our pre-burst optical pumping scheme simulations showed that we can drop the pump power costs by a factor of 40 with pre-burst ASE power levels below the heating level tolerance of 100 μW. UMKC invention disclosure filed 02JUN2020.

(B) For a proposed system gain of 8 million, a linear gain theory predicted the in-burst ASE would be over our heating level spec. by a factor of 3960, but by exploiting the nonlinearity of gain saturation we find that we can suppress the ASE by over 7000. UMKC invention disclosure filed 14SEP2020.

(C) Achieved initial practical device designs that exploit gain saturation, which remained below damage thresholds, via staged designs of different mode diameters NOV2020.

(D) Models of the impact of ASE on timing jitter in the presence of dispersion and/or nonlinearities were established JUL2020.

(E) The design of a proof-of-concept experiment demonstrating a cost-reduced optical pumping scheme was finalized MAR2021.

(F) We made (to our knowledge) the first observation of self-focusing effects that are not determined by beam power alone. We found instead that these can also be controlled via the geometric factors within a waveguide (such as fiber core diameter) MAY2021.

We additionally made (to our knowledge) the first observation that a mode exists in the air within a simple glass tube into which we can couple energy from the mode in the glass. Thus, an amplifier (in the doped and pumped glass) can operate at higher powers JUNE2021.

We found conditions under which 0.25 GW of power can exist in the tube's air-core mode when its glass-cladding mode is at a power level near 0.5 GW JULY2021.

Advancements in the very high-power operating point (tens of GW) of our tubular optical amplifier (and the existence, size and spatial uniformity of its air-core mode) were shown to permit a single laser to trigger an array of several (up to 100) Si-PCSS – reducing the laser system cost and eliminating the optical timing jitter constraint. The symmetry breaking of the scattering from self-focusing in a curved waveguide was shown to enable such AUG2021.

4 Photoconductive Switch Innovation

4.1 Characterizing and Optimizing On-State Resistance in GaN:X PCSS

(Heather Thompson)

Work is currently focused on manuscript preparation. Please see the April 2022 MSR for the most up-to-date summary of this project.

5 Drift-Step-Recovery-Diode-Based Source Alternatives

5.1 Drift-Step Recovery Diode and Pulse Shaping Device Optimization

(Jay Eifler)

5.1.1 *Problem Statement, Approach, and Context*

Primary Problem: Drift-step recovery diodes (DSRDs) and DSRD-based pulsed power systems are competitive with PCSS-based systems for HPM cUAS, with the benefit of not requiring a laser. Maximizing peak power while maintaining characteristic ns-order DSRD rise times requires optimization of the DSRD device design and pulser. Other considerations are for compactness, low-jitter, cooling required, and additional pulse-sharpening device within the pulse shaping head circuit. Additional goals for pulse repetition frequency are also to be satisfied for various applications.

Solution Space: By altering DSRD device parameters (geometry, doping, irradiation), optimize single-die and stack designs for peak power and risetime within various inductive pulser circuit topologies. Also optimize the pulse sharpening device (PSD) within the pulse shaping head circuit.

Sub-Problem 1: TCAD and SPICE models of the DSRD are inaccurate and must be improved. PSD models have not been developed.

Sub-Problem 2: Inductive pulser designs are complicated by the DSRD (and PSD) parameter variability. Use TCAD and/or SPICE models to account for variability and improve pulser design.

State-of-the-Art (SOTA): MW peak power and ns-order risetimes have been achieved in DSRD-based pulsed-power systems employing DSRD stacks for higher voltage holding and parallel lines of DSRD to increase current. PSD have sharpened DSRD pulses to 100 ps-order.

Deficiency in the SOTA: A lack of accurate TCAD and SPICE models make design of DSRD and DSRD-based inductive pulser circuit topologies (with or without PSDs) difficult to the level of tens of MW of peak power while maintaining ns-order risetime (or sharpened 100 ps-order). In addition, DSRD (and PSD) fabrication variabilities further complicate pulser design.

Solution Proposed: Develop further modeling capabilities in TCAD and SPICE for DSRD and DSRD-based inductive pulser circuit topologies to optimize DSRD and inductive pulser designs, especially for maximum peak power and minimum risetime, but also for low-jitter, reduced cooling, and compactness. Additionally, optimize pulser with PSD and pulse shaping head circuit.

Relevance to OSPRES Grant Objective: DSRD-based systems eliminate laser requirements necessary for PCSSs and are competitive in terms of thermal requirements and peak power. With sharpening, the DSRD-based systems can produce comparable risetimes. The SWaPC^2 cooling requirements of HPM cUAS systems can be solved with DSRD-based pulsed power systems, and low-jitter DSRD-based systems can be used for beam-steering in phased-arrays.

Risks, Payoffs, and Challenges: DSRD must be arrayed and staged to increase current since DSRD are limited in their ability to operate at high current densities. DSRD and PSD must also be stacked to operate at high voltages necessary for high peak power and maintain low risetimes. The stacking methods can damage dies and produce variable results in risetime and DSRD diffused doping profiles can be difficult to achieve and may require epitaxial methods. SPICE device models for DSRD are unavailable and must be developed, and questions remain about TCAD limitations for DSRD and PSD modeling.

5.1.2 Tasks and Milestones / Timeline / Status

(A) Milestone – Develop DSRD SPICE model within SmartSpice using the CMC diode model (built-in and Verilog-A).

1. Task – Develop accurate forward IV, reverse CV and reverse recovery testing (RRT) modeling in CMC diode model using either built-in (faster) or Verilog-A (customizable) models; On-going [APR-JUN 2022];

2. Task – Develop reverse IV and forward CV modeling and parameters in SmartSpice CMC diode models (built-in and/or Verilog-A); Preliminary exploration [MAY-JUL 2022];

3. Task – Develop 1x1 DSRD-based pulser recovery parameters within CMC diode model of SmartSpice (built-in or Verilog-A) and compare to RRT parameters; On-going [APR-JUL 2022];

(B) Milestone – Complete LTSPICE parameterization of the standard diode model for DSRD inventory.

1. Task – Finish Gen2.2 DSRD LTSPICE parameter extraction; On-going as received [APR-MAY 2022];

(C) Milestone – Develop automated fitting procedures for developed LTSPICE and/or SmartSpice DSRD models.

1. Task – Improve speed/accuracy/size of brute force fitting methods for LTSPICE and SmartSpice diode models; On-going [APR-JUN 2022];

2. Task – Improve python-based fitting methods for diode models used in LTSPICE and/or SmartSpice; On-going [APR-JUN 2022];

3. Task – Improve use of SmartSpice Optimizer for parameter fitting of diode models; On-going [APR-JUN 2022];

4. Task – Develop automated fitting procedures for Verilog-A diode models (CMC or custom); Preliminary exploration [APR-AUG 2022];

(D) Milestone – Convert manufacturer PSPICE and PSPICE/LTSPICE unencrypted device models into SmartSpice format for use in DSRD-based pulser simulation.

1. Task – Convert unencrypted PSPICE/LTSPICE Cree MOSFET model into SmartSpice format; On-going [APR-JUN 2022];

2. Task – Convert unencrypted Texas Instruments Gate Driver model from PSPICE into SmartSpice format; On-going [APR-JUN 2022];

(E) Milestone – Develop DSRD parameters for 2450 and new 371 semiconductor analyzer measurement data (forward IV and reverse IV).

1. Task – Develop standard diode LTSPICE 371A semiconductor analyzer measurement data parameters; On-going [APR-JUN 2022];

2. Task – Develop SmartSpice CMC (Verilog-A) 371A semiconductor analyzer measurement data parameters; On-going [APR-JUN 2022];

(F) Milestone – Determine performance of doping profiles within TCAD

1. Task – Determine TCAD performance of SOS, dynistor and thyristor doping profiles; Doping profiles not yet received; [?-? 2022];

2. Task – Determine TCAD performance of square root DSRD doping profiles; Not yet begun [? 2022];

3. Task – Determine TCAD performance of Gen3 manufacturer doping profiles; Not yet begun [? 2022];

4. Task – Determine recovery behavior of DSRD doping profiles within TCAD for development of custom Verilog-A CMC-based DSRD models; Not yet begun [?-? 2022];

5. Task – Determine effect of doping and defects on DSRD forward IV performance; Not yet begun [?-? 2022].

5.1.3 *Progress Made Since Last Report*

(E.1-2) Develop forward IV parameters for 2450/371 semiconductor measurement data

DSRD EG1605 experimental forward IV data was received from Keithley 2450 measurements and successfully fit in the LTspice standard diode model. The fit to both the Keithley 2450 and Tektronik 371 forward IV was poor in LTspice as expected for the EG series.

Earlier 2450/371 experimental forward IV data for EG1608 was fit within the SmartSpice CMC Verilog-A diode model using a custom segmented or sectional fitting method (akin to the tabulated diode model). The EG DSRD have a non-standard forward IV (due to doping, defects, contacts) that cannot be fit in LTspice. The CMC fitted forward IV was then successfully used to simulate pulse output at 50 Ω load in the 1x1 DSRD-based pulser and showed the correct pulse shape (the recovery parameters will have to be re-fit for a pulse match).

5.1.4 *Technical Results*

(E.1-2) Develop forward IV parameters for 2450/371 semiconductor measurement data

LTspice

New experimental forward IV from the Keithley 2450 for EG DSRD have been taken and received and extend the forward IV data up to 1 A of current from the earlier picoammeter measurments. For EG1605 the data was fit within the LTspice standard diode model sweeping IS, N, IKF and RS forward diode parameters. Experimental Tektronik high

power 371 semiconductor analyzer was also taken and an attempted fit in LTspice was also done alongside the 2450 data as shown in Figure 5.1.1. The inset shows the fit to the 2450 data alone and the fit can be improved since the 4-parameter sweep was at lower resolution (10x10x10x10=10,000 simulations). Once the correct functional shape can be made, the closeness of fit has generally not been a problem (but is only as good as the experimental data). A fit to the 371 data was also attempted within LTspice but the functional shape of the curve cannot be fit, and the fit is of limited accuracy and application in simulation.

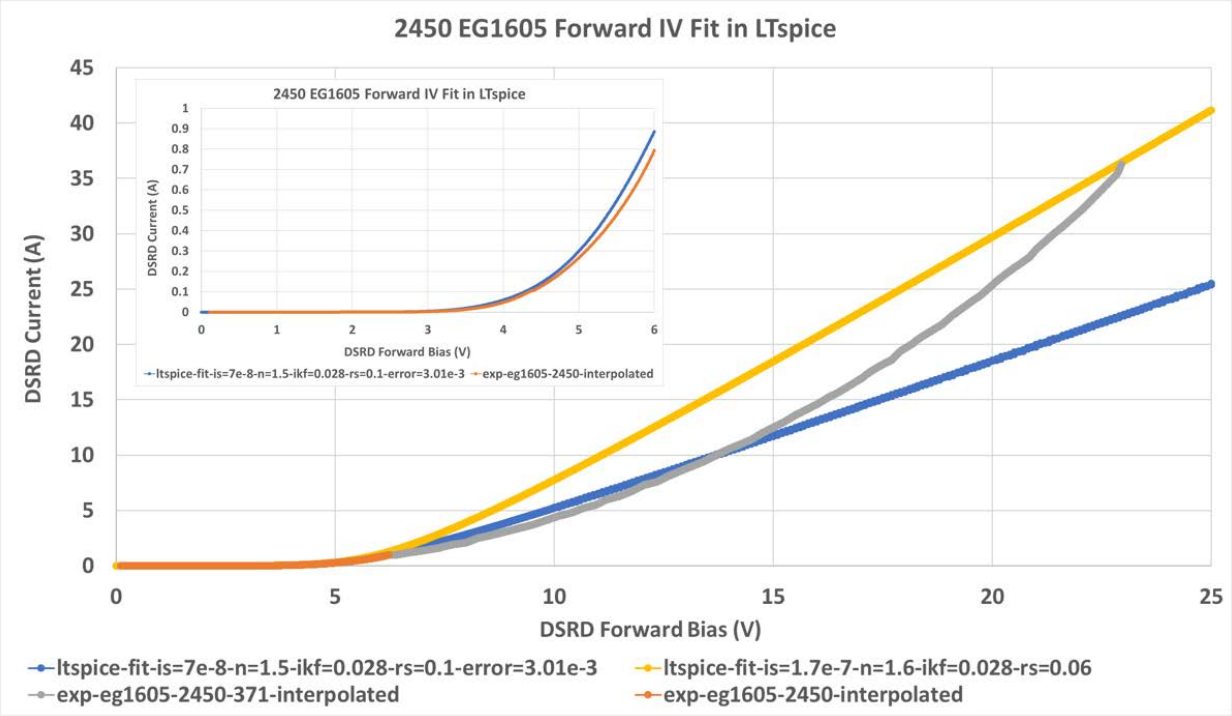

Figure 5.1.1. LTspice forward IV fits to Keithley 2450 and Tektronik 371 experimental data. Inset shows the fit to the Keithley 2450 forward IV data.

SmartSpice

SmartSpice contains the Compact Modeling Committee (CMC) industry-standard diode model, and the Verilog-A code has also been obtained. The CMC diode model has a recovery model which the standard diode model (within LTspice or SmartSpice) does not have. The Verilog-A code can be modified to tailor forward IV fits or alter the recovery model (LTspice does not have Verilog-A capabilities in the free version).

The EG DSRD forward IV is a non-standard forward IV that cannot be fit with the conventional diode equations available in the standard diode model and is likely due to manufacturing details involving the doping, defects and contacts to improve the hardness/softness of recovery. A segmented or sectional forward IV model was coded into the CMC Verilog-A diode model within SmartSpice and is akin to a tabulated diode model that goes directly from the data. In the sectional model developed here the CMC diode equations (exponential) are used for as many data points as can fit very closely

and different sets of parameters (IDSATRBOT, NFABOT within the CMC diode model) are developed for different sections (voltage range) of the forward IV curve (see May 2022 OSPRES Grant Report). These parameters are then coded into the Verilog-A model for the different voltage ranges allowing a very close fit to both the Keithley 2450 and Tektronik 371 experimental forward IV data as shown in Figure 5.1.2. The experimental data shown is the first 371 data collected and was matched with a similar diode measured in the Keithley 6485 picoammeter. Newer, more accurate forward IV is being experimentally measured with the Keithley 2450 and Tektronik 371 that will now be accurately fit in the CMC Verilog-A DSRD model. This is the first accurate fit to 371 data and the first accurate fit to both picoammeter and 371 data. It should be mentioned that 5 out of 8 DSRD had 2450/371 curves that aligned or agreed in the data overlap region (measurement data least accurate near ends of measurement range, that is, no real data overlap).

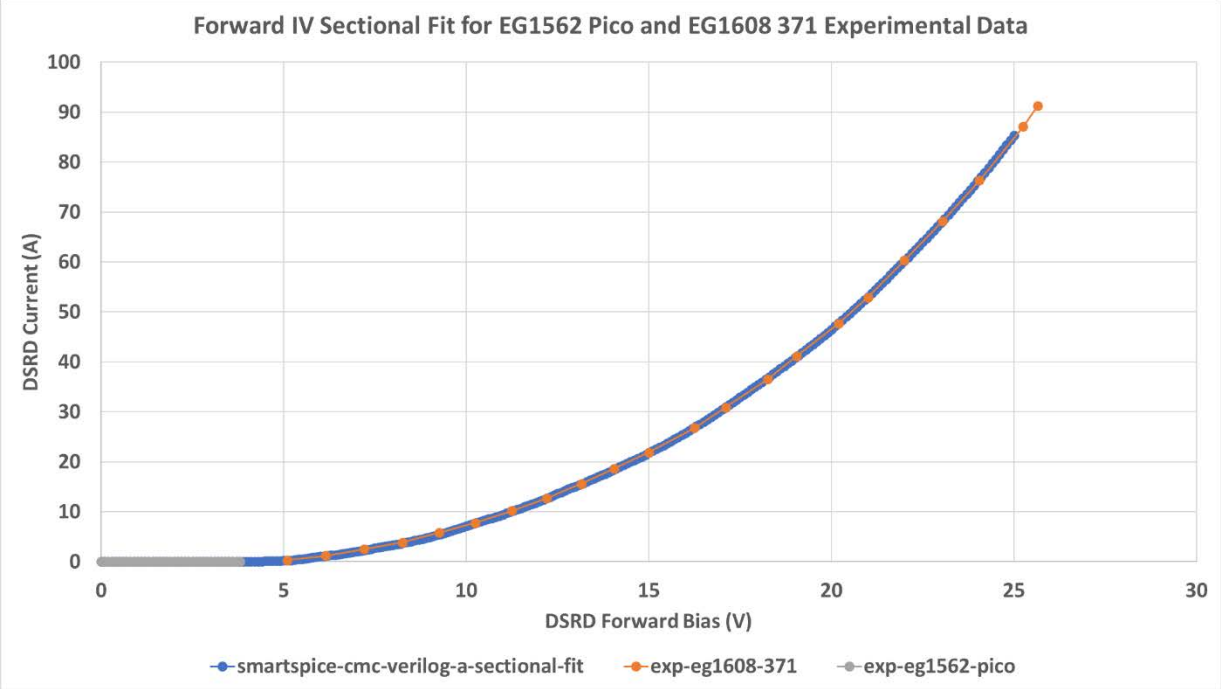

Figure 5.1.2. SmartSpice CMC Verilog-A forward IV very close fit to both Keithley 2450 and Tektronik 371 experimental data.

Next the forward IV parameters fit to the picoammeter and 371 data were used within a 1x1 DSRD-based pulser simulation within SmartSpice using the CMC Verilog-A diode model. Previously the reverse CV data had been fit somewhat accurately and was re-used along with the recovery parameter fits performed to an earlier poor fit to the forward IV data (now replaced with a good fit). The output pulse at the 50 Ω load is shown in Figure 5.1.3. The peak voltage (8382 V) is much higher than the ~3300 V experimental data but the recovery parameters are set to the older, inaccurate forward IV fit. However, the pulse shape and pre- and post-pulse characteristics match experiment and will continue to match as the recovery parameters are refit to obtain very close matches to

peak voltage, risetime, pulsewidth and voltage riserate. In Figure 5.1.3, the 10/90 risetime was 5.19 ns which more closely matches experiment for the 8382 V peak voltage (that is similar voltage riserates).

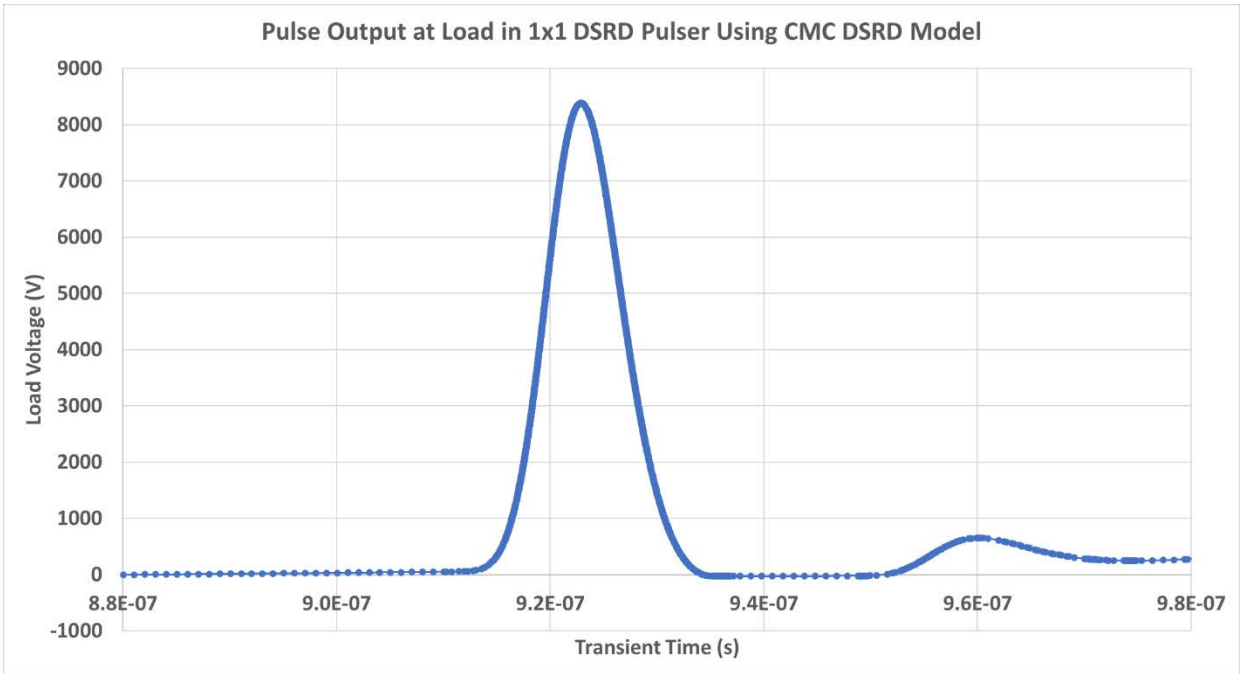

Figure 5.1.3. Output pulse at load within 1x1 DSRD-based pulser simulation within SmartSpice using the CMC Verilog-A diode model with sectionally-fit forward IV.

Next the forward IV will be improved by using newer, improved forward IV data and refining any discontinuities in the fit within the missing data gap (between the 2450 and 371). The reverse CV will be more closely fit than has been done within the CMC diode model. The forward CV and reverse IV can be compared to LTspice fits and experiment (no specific fit likely needed). Finally, the recovery parameters can be refit to the new IV and CV fits to match a single pulse very closely. The next step after the pulse fit is to observe the variation in recovery parameters over a range of input supply voltages and trigger durations and then to either set a fixed set of recovery parameters or allow them to vary with the circuit conditions used (somewhat like the sectionally fit forward IV if necessary). Further refinements to the recovery model can be made incorporating model equations from the literature directly into the Verilog-A code. Ultimately, tests of the predictive capability of the DSRD model within circuit design simulations will be performed along with variations in the DSRD parameters and circuit component values for inductors, capacitors, and resistors used.

5.1.5 *Summary of Significant Findings and Mission Impact*

(A) Development of DSRD Model Within SmartSpice CMC Diode Model

The SmartSpice circuit simulation software has been received in JAN 2022 and in FEB 2022 the Verilog-A CMC diode code was retrievable from the Si2 organization website.

Development immediately began of the CMC diode model for DSRD modeling by producing forward IV, reverse CV and reverse recovery testing simulations and fitting to example DSRD in the inventory. Recovery parameter fitting within the 1x1 DSRD-based pulser has also begun. The capability of the CMC diode model for modeling DSRD can now be assessed. Any deficiencies in the CMC-DSRD model can be improved using the programmable Verilog-A code of the CMC diode model to include DSRD specific modeling equations based on theory, TCAD simulation, experiment and the literature. The Verilog-A code has been modified to allow different fitting parameters for different sections of the curve so that real, experimental forward IV can be accurately fit. Improved forward IV fitting in the Verilog-A CMC diode model will allow for improved pulser simulation.

(B) LTSPICE Standard Diode Model Parameter Development for DSRD Inventory

DSRD in the inventory of received diodes (legacy, EG and Gen2) have been fit for LTSPICE standard diode model parameters (for forward IV, reverse CV and reverse recovery testing) for use in LTSPICE DSRD-based pulser simulations and to provide another metric for the characterization of the DSRDs in comparison to pulser performance. Some details of the very low voltage and current forward IV have not been fit but the fitting is still very close when visually inspected in non-log format. Reverse IV have not been fit in the standard diode model since it cannot capture the behavior and breakdown has not yet been measured, only estimated. Forward CV measurement are problematic and not fit mostly since the forward CV parameters in the standard diode model are used for recovery modeling. Various methods exist in LTSPICE to improve recovery parameter fitting but are either inadequate (Vp or carrier viscosity) or non-realistic (adjustment of reverse CV parameters) but have produced fits within 10% error for DSRD-based pulser performance. Gen2.2 experimental data has been received fitted within LTspice but there is high, variable series resistance in the Gen2.2 measurements that are being addressed with a new fixture and testing.

(C) Develop Automated Fitting Procedures for LTSPICE and SmartSpice

The current best method of fitting is using a brute force method of running LTSPICE or SmartSpice simulations sweeping over the desired parameter space. The brute force method can produce the most accurate fits but requires long simulation times and cannot be used to explore large parameter spaces easily (which is why more physically-based models using only measurable parameters is derisable). There is ultimately a limit to how quickly and accurately one can develop parameter sets. Another method is to program in the model equations into Python and use their curve fitting tools, however this method cannot incorporate circuit simulation and will therefore be less effective in producing accurate fits but is much faster in simulation time (can depend on how much parameter adjustments affect DSRD-based pulser performance on which method to use). The other fitting method is to use the built-in optimizer within SmartSpice, but the optimizer has not yet produced as good of fits consistently as the brute force method and will take some experience in using well.

(D) Conversion to SmartSpice of Manufacturer Device Models

Unfortunately, manufacturer device models are not openly available in SmartSpice only PSPICE and to some extent LTSPICE (usually converted from PSPICE). Therefore, the available PSPICE and PSPICE/LTSPICE models must be converted to the SmartSpice format, otherwise keeping the model the same. Note that encrypted models cannot be converted into SmartSpice, such models either have to be developed from scratch and either the datasheet or additional experimental tests used (or purchased from Silvaco for SmartSpice if available).

The unencrypted Cree MOSFET model has been converted into SmartSpice and tested within 1x1 DSRD-based pulser simulations and compared to LTSPICE simulations successfully. The unencrypted Texas Instruments gate driver model has also been converted into SmartSpice successfully. One issue with the driver model is it is intended for PSPICE but used often in online discussion in LTSPICE. However, close examination of the model shows that the model cannot perform correctly in all pin conditions in LTSPICE due to incorrect parameter types used in a voltage-controlled switch within the driver model. The voltage-controlled switch has been correctly implemented in the SmartSpice conversion and can be fixed for the LTSPICE version (Texas Instruments has not responded to inquires). Neither the MOSFET or gate driver models have been extensively diagnostically tested and compared to the datasheets which are often somewhat different to the free provided models (only so accurate).

(E) IV Parameter Development for 371A Semiconductor Analyzer Measurement Data

A 371 semiconductor analyzer has been acquired and setup for forward IV testing with the potential for higher voltage/current reverse IV testing and breakdown. Initially concerns arose about the shape of the forward IV and whether temperature distortion was occurring at the higher voltages and current available with the 371 compared to the 6485 Keithley picoammeter. However, published power diode forward IV have been discovered showing similar forward IV at room temperature. 371 testing will proceed by testing more DSRD and subsequently using thermocouples and/or heat sinks. 371 higher voltage/current forward IV testing is necessary to characterize the DSRD in the diode models to perform correctly in the DSRD-based pulser simulations. How accurate the forward IV must be, has not been determined, as well as, to what extent individual diodes can be reliably distinguished in modeling. A new method for fitting forward IV has been implemented in the CMC Verilog-A diode modeling code that will allow for more accurate fitting of the 371 data for its full range. More rigorous forward IV testing has been implemented incorporating a number of modifications to the forward IV test fixture, cabling and testing methods (2- vs 4-wire) yielding forward IV with definite error bars. Also, lower current and voltage forward IV data are now taken with the Keithley 2450 sourcemeter which has a higher current limit (1 A) than the picoammeter (20 mA). Data collection of the DSRD inventory for forward IV using both the 2450 and 371 has begun and the curves align well for most DSRD. Breakdown testing has also been performed for Gen2 and EG DSRD showing 40% yield for higher breakdown devices needed for DSRD stacking and DSRD pulser testing.

(F) TCAD-Based Doping Profile Performance Evaluation

Many DSRD TCAD simulation studies have been performed assessing the doping profiles used for the DSRD manufactured by SPT and in stock (this summary includes work from

the past six months). The TCAD modeling has been temporarily on hold as effort is focused toward developing an accurate SPICE DSRD model due to the unavailability of manufacturer device models for MOSFETs and gate drivers within TCAD. A MOSFET model was developed for the Cree MOSFET for use within TCAD but still had some differences when used in pulser simulations, so the development of the DSRD SPICE model was prioritized so that manufacturer models (for MOSFETs and drivers) could be used.

Doping profiles are forthcoming for various SOS, dynistor and thyristor devices and TCAD will be used to assess their performance. Some interest has been expressed in assessing square-root doping profiles for DSRD. Gen3 doping profiles from the manufacturer have yet to be assessed within TCAD for performance differences with the requested doping profiles. As well, the recovery models within the CMC diode model are themselves based on PIN diode TCAD simulations and TCAD can perform DSRD doping profile specific simulations to determine model equations and parameters. Additionally, the forward IV behavior of our DSRD can be modeled as seen in the 371A semiconductor analyzer mesaurements. TCAD modeling will continue to be of use in device modeling since it is the only way to assess doping profiles.

5.1.6 *References*

[1] Chandra Bose, JV Subhaus, I. Imrie, H. Ostmann, and P. Ingram. “SONIC-A New Generation of Fast Recovery Diodes [D].” IXYS Semiconductor (2011).

5.2 Pioneering Drift-Step Recovery Diode Processing and Manufacturing

(Alex Usenko)

Detailed reporting for this section is on hold. A summary report of work completed under OSPRES Grant will be provided in a future MSR, and more streamlined reporting may be provided as appropriate. Please see the May 2022 MSR for the most recent progress update.

5.3 Characterization of SOS Diode Performance through DOE Augmentation

(Joseph Reeve-Barker, Jay Eifler & Megan Hyde)

5.3.1 *Problem Statement, Approach, and Context*

Primary Problem: Drift step recovery diodes (DSRDs) are planar diodes that are capable of nanosecond, high-frequency (10–10^3 kHz) pulses [1] with applications as opening switches in inductive energy storage (IES) pulse generation circuits. There is not a clear understanding of the effects DSRD parameters have on overall IES pulser performance. The purpose of this project is to tie the DSRD parameters to its tailored performance requirements.

Solution Space: Leveraging both design of experiment (DOE) and machine learning (ML) capabilities, we will develop a methodology of characterizing and optimizing DSRDs in order to provide fabrication recommendations in the context of application targets.

***Sub-Problem 1*:** We do not yet understand how diode parameters are tied to diode performance.

Sub-Problem 2: There is no standardized method for correlating the diode key performance indicators (KPIs) to the IES pulser generator performance.

Sub-Problem 3: The number of possible inputs for the DOE is expected to be too large, so ML will need to be leveraged in order to guide decision-making processes.

State-of-the-Art (SOTA): Standard diode measurements include curve tracers for forward and reverse IV, impedance spectroscopy for forward and reverse CV, and function generators or, for example, the Avtech pulser for reverse recovery with high voltage and/or high current when necessary. These measurements are used to generate commonly available datasheets for COTS diodes. These standard diode measurements can then be correlated to pulser performance using traditional data analytics.

Deficiency in the SOTA: The standard diode measurements and datasheets do not include pulser performance necessary to evaluate DSRDs. The datasets generated with doping profile assessment (for example spreading resistance profiling), standard diode measurements and pulser performance are too large and complex to leverage traditional data analytics and will benefit from machine learning techniques.

Solution Proposed: Develop a holistic evaluation network for DSRD characterization. This network will include a DOE that will be a continuously evolving model as diode parameters are correlated to pulser performances. Augmenting the DOE will ensure that the model will remain relevant throughout this study as more discoveries are made. Machine learning will be used as the primary decision-making tool for augmenting the DOE. Once the network is established, it will be used to outline the optimal parameters for stacks of DSRDs within an IES pulse generator.

Relevance to OSPRES Grant Objective: Bridging the gap between the theoretical and physical performance of DSRDs enables closing the gap between a low fidelity TRL3 breadboard pulse generation system, and one which is at a high fidelity TRL4 prototype level. At the TRL4 level, the DSRD-IES pulse generator system would be sufficient to replace the costly laser-based Si-PCSS HPM generator without compromise to scalability required to support the Naval afloat mission.

Risks, Payoffs, and Challenges:

Challenges: Traditional predictive analytics will be difficult to correlate with the augmented DOE due to the large volume of data. Machine learning is expected to assist with decision making processes for the DOE, but only if ideal diode characteristics have been established and good data have been used to train the machine learning model.

5.3.2 Tasks and Milestones / Timeline / Status

(A) Milestone – Establish preliminary DOE and standard operating procedure (SOP) for identifying KPIs of DSRDs [*estimated completion by MAR22*].

1. Task – Ascertain current KPIs used to optimize diodes simulated, manufactured, and utilized within the IES pulse generating circuit [completed AUG21];
2. Task – Construct preliminary DOE to acquire data on all KPIs based on Task 1 [*completed FEB22*];
3. Task – Leverage existing Python scripts to process legacy DSRD KPI data [*completed SEP21*];
4. Task – Develop new and review existing SOPs for experimental testing apparatuses used to evaluate individual KPIs and measure their performance [*completed OCT21*];
5. Task – Identify gaps/deficiencies in legacy KPI data, evaluate existing theoretical relationships to bridge gap and minimize DOE if possible [*completed OCT21*];
6. Task – Using SOPs developed in Task 4, acquire experimental data from legacy DSRDs, refine SOP(s), and assess repeatability and reproducibility [*In progress*: *SEP21–MAR22*];

(B) Milestone – Evaluate DSRD performance using the developed SOPs and facilitated by the preliminary DOE [*estimated completion JUL22*].

1. Task – Acquire data on newly manufactured 2nd generation epitaxial DSRDs from Section 5.2 using refined SOPs from Milestone A [*completed JAN22*];
2. Task – Evaluate the precision and power of the DOE [*In progress*: *MAR22–JUL22:*];
3. Task – Develop a DSRD selection guide for the pulser circuit based on the static DC test measurements *[In progress: MAR22–MAY22];*
4. Task – Correlate the static DC test measurements to the performances of the IES pulser circuits and to fabrication procedures [*MAR22–JUN22];*
5. Task – Begin training machine learning model with DSRD data to determine correlations between static DC and pulser testing results [*MAY22–JUL22*];
6. Task – Acquire data on newly manufactured 3rd generation epitaxial DSRDs from Section 5.2 using refined SOPs from Milestone A [*JUL22–SEP22*];

(C) Milestone –DSRD diode network evaluation [*on hold until Milestone B is completed*].

1. Task – Refine Python script to incorporate new correlations based on findings from Milestones A&B [*Est. Summer22*];
2. Task – Amend ML training model with data acquired on new DSRDs (as characterized by Sections 5.1–5.2) to investigate statistical correlation of diode performance [*Est. Summer22*];
3. Task – Work with TCAD simulation team to address discrepancies between the DSRD performance obtained experimentally, and that achieved within simulations [*Est. Summer22*];

4. Task – Collaborate with DSRD manufacturing team to address discrepancies between the DSRD characteristics evaluated experimentally, and that desired by manufacturing process [*Est. Summer22*];
5. Task – Investigate relationships between statistical significance of individual diode KPIs to the peak performance of the IES pulser with the pulse generator team. [*Est. Summer22*];
6. Task – Incorporate findings from Tasks 1–5 into ML model, pinpoint KPI correlations of interest, and provide recommendations to IES sub-teams accordingly [*Est. Summer22*];

(D) Milestone – DSRD diode network evaluation [*on hold until Milestone C is completed*].

1. Task – Augment DOE network to streamline diode evaluation and identify checkpoints/gaps within simulation, manufacturing, and circuit development process to ensure optimal diodes are selected and utilized to produce robust high-fidelity IES pulse generator prototypes [*Est. Fall22*].

5.3.3 *Progress Made Since Last Report*

(A.6) DSRD Standard Diode Testing

Rigorous Forward IV Testing and Breakdown Testing

EG and Gen2 forward IV testing has begun with three gen2.1 and eight EG DSRD completed for forward IV. The new forward IV consist of two measurements: one on the Keithley 2450 and the other on the high power Tektronik 371 which are combined to produce a complete forward IV over the voltage range of interest in DSRD-based pulsers. Breakdown testing awaits the design and build of a new breakdown test fixture.

5.3.4 *Technical Results*

(A.6) DSRD Standard Diode Testing

Rigorous Forward IV Testing and Breakdown Testing

Forward IV were collected using both the Keithley 2450 sourcemeter and the Tektronik 371 semiconductor analyzer to provide experimental data covering the range of voltages needed for characterizing the DSRD pulser design and simulation (also for correlating standard diode tests to pulser performance). All forward IV measurements were done as 4-wire measurements to avoid series resistance effects for cabling and fixturing.

For the 2450 to avoid overheating, seven segments of data are collected with 100 data points per section (sections: 0-1 µA, 1-10 µA, 10-100 µA, 100 µA-1 mA, 1-10 mA, 10-100 mA, 100 mA-1 A). The source delay was set to auto-delay rather than 0.5 seconds since the longer constant source delay produced overheating at higher currents. For the 371, the forward iv measurements use a 240 µs pulse to avoid overheating and measurements were collected over the full voltage and current range possible.

Three gen2.1 and eight EG DSRD have been measured for forward IV. In Figure 5.3.1 are shown the three Gen2.1 forward IV which were taken with cables having banana and alligator clips on either end. In Figure 5.3.2 are shown the eight EG1600 forward IV

taken with banana cables and using a BNC-banana adapter. In Figure 5.3.3 the forward IV measurement setup incorporating the 2450 and 371 (using banana cables and BNC-banana adapters) is shown with c-clamps reinforcing the top 3D-printed mounting piece holding the pressurizing bolt.

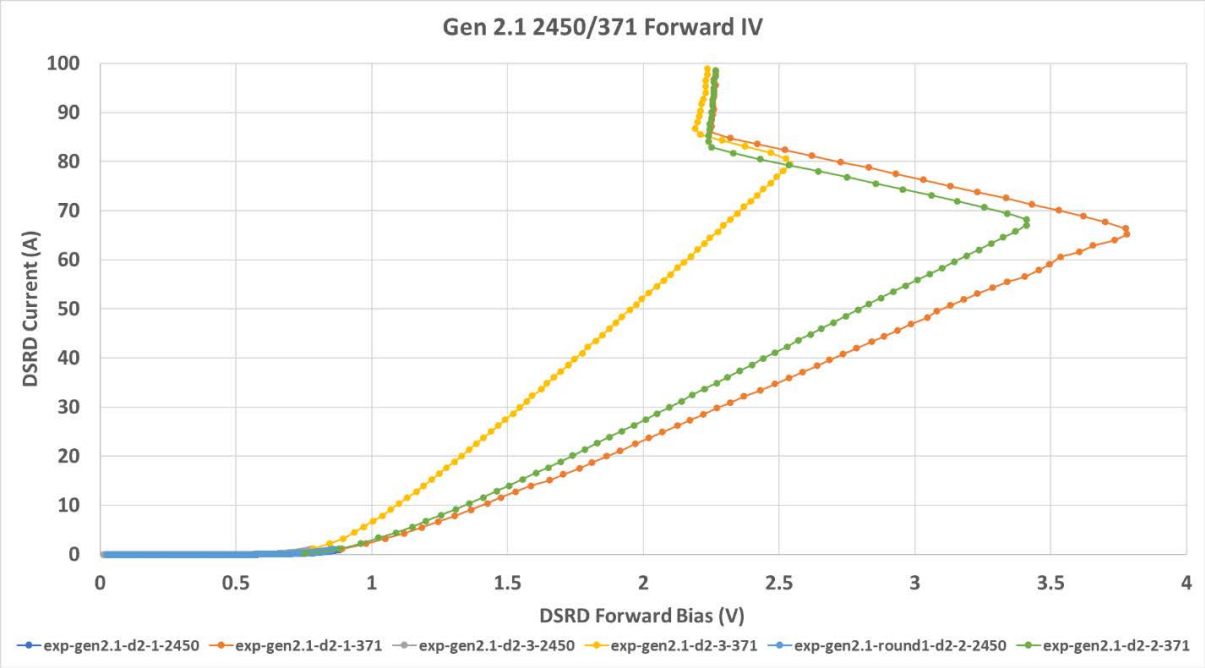

Figure 5.3.1. Gen2.1 forward IV using Keithley 2450 and Tektronik 371. Apparent snapback is instrument limitation due to use of alligator clipping.

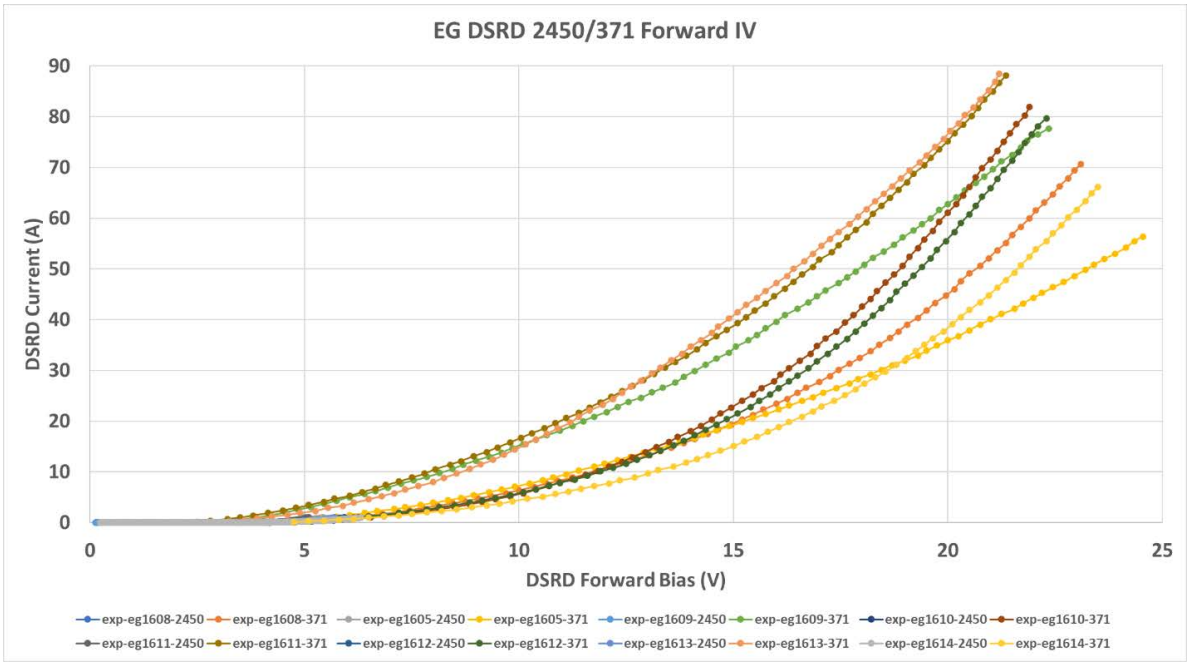

Figure 5.3.2. EG1600 forward IV using Keithley 2450 and Tektronik 371.

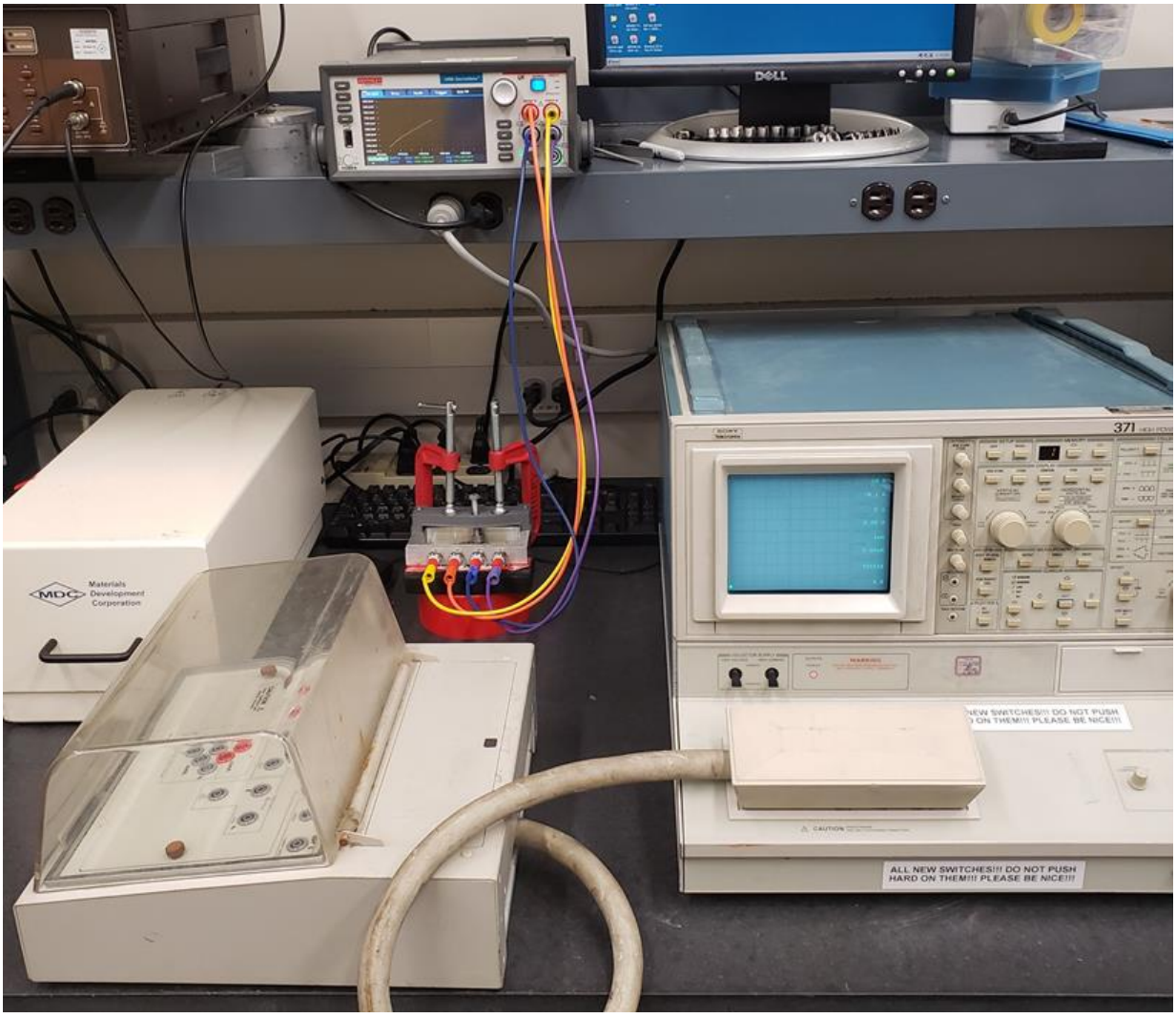

Figure 5.3.3. 4-wire Keithley 2450 and Tektronik 371 forward IV measurement setup. Forward IV fixture uses reinforcing c-clamps and banana-banana cables with BNC-banana adapters.

Accurate, consistent forward IV are necessary for parameterizing diode models to the experimental data. The Gen2.1 forward IV clearly show a linear region indicative of reaching minimum on-state resistance which is very close to the series resistance of the device and its electrical contacts (series resistance is largely due to the contact resistances). For the EG1600 measurements the linear region is not so clear but is taken from the higher voltage and current data of the curve, so series resistance estimated from this method for the EG diodes is over-estimated. In Table 5.3.1 the series resistance calculated using the two-point method (straight line method) are shown for the earlier measurements.

diode	RS			diode	RS
eg1610	0.089			gen2.1-d2-3	0.020
eg1612	0.095			gen2.1-d2-2	0.036
eg1611	0.108			gen2.1-d2-1	0.042
eg1608	0.112			average	0.032
eg1614	0.117				
eg1613	0.117				
eg1609	0.154				
eg1605	0.210				
average	0.125				
ratio average	3.860				

Table 5.3.1. Two-point method calculated series resistance (RS) for EG and Gen2 DSRD.

The average series resistance (RS parameter in diode models) for Gen2 and EG DSRD is shown along with their ratio. The range of RS is about a factor of 2 in both the Gen2 and EG DSRD, while the ratio of the average RS is about 4 where we might expect 7 due to comparing 1-stack Gen2 and 7-stack EG here. While Gen2 and EG use different cabling, measurements have shown RS is affected little by the cabling change. Series resistance is important for assessing pulser performance. DSRD that have twice the RS will have half the peak voltage output. Along with breakdown testing, series resistance measurements from forward IV in part determine the peak voltage pulser performance (snappiest of recovery also necessary to determine pulser performance, maximum DSRD current, DSRD charge storage time). The differences in series resistance can be related to the contacting method or pressure on the DSRD but also the metallization on the DSRD and other manufacturing factors.

5.3.5 *Summary of Significant Findings and Mission Impact*

(A.1) Several KPIs have been identified that tie the experimental diode test results to SPICE model simulation parameters. The first KPI is the forward current-voltage (the voltage reading at 10 mA) that is linked to the following SPICE parameters: saturation current, ohmic resistance, emission coefficient, and the forward knee voltage. From the impedance analyzer, the capacitance-voltage measurement is tied to the zero bias junction capacitance and the bottom junction grading coefficient. Both the forward voltage-current and the capacitance-voltage KPIs can be further tied to the SPICE simulation circuit peak voltage performance. The reverse current-voltage (current at -200 V) is linked to the breakdown voltage SPICE parameter. The reverse recovery time measurements, such as the charge storage time and the transition time, are tied to the transit time SPICE parameter and to the full width at half maximum of the pulse signal. Several of these KPIs are not yet associated with specific circuit performances but will require further analysis as outlined in B.4.

(A.2) A preliminary DOE has been developed. The first 6 out of 16 rounds are currently being processed per (A.6).

(A.6) It was found that the test fixture for the picoammeter was causing large variations in the current-voltage measurements due to inconsistent pressure application to

the diode. The variation was significantly larger on the Gen2 diodes since they are approximately one-third the height of the 7-stack diodes. A new 3D printed fixture with the ability to apply consistent pressure is expected to drastically reduce the contact resistances and variability that have been introduced to the measurements. New forward IV measurements have produced an averaged measurement with standard deviation error bars. Breakdown testing has shown ~40% of diodes hold at least 500 V per diode in stack. CV testing for series resistance has shown high series resistance associated with the CV test fixture and CV testing in the forward IV fixture may show lower series resistance. Forward IV from the Keithley 2450 and Tektronik 371 have been combined to produce measurements over a larger range of current and voltage necessary to model the DSRD in DSRD-based pulsers. The DSRD inventory is currently being tested for forward IV using both the 2450 and 371.

(B.1) In A.6, it was discovered that the test fixture was the cause of significant variation within the test results, particularly with the Gen2 diodes. Several diodes are scheduled for repeat measurements to determine if all diodes need to be re-tested, which would affect the “completed” status of this milestone.

5.3.6 *References*

[1] Benda, H., & Spenke, E. (1967). Reverse recovery processes in silicon power rectifiers. Proceedings of the IEEE, 55(8), 1331-1354.

[2] Kozlov, V. A., Smirnova, I. A., Moryakova, S. A., & Kardo-Sysoev, A. F. (2002, June). New generation of drift step recovery diodes (DSRD) for subnanosecond switching and high repetition rate operation. In Conference Record of the Twenty-Fifth International Power Modulator Symposium, 2002 and 2002 High-Voltage Workshop. (pp. 441-444). IEEE.

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[4] Sharabani, Y., Rosenwaks, Y., & Eger, D. (2015). Mechanism of Fast Current Interruption in p− π− n Diodes for Nanosecond Opening Switches in High-Voltage-Pulse Applications. Physical Review Applied, 4(1), 014015.

[5] Foll, H. (n.d.). *Reverse Recovery Time of Junction Diodes*. Retrieved from Semiconductors:https://www.tf.unikiel.de/matwis/amat/semi_en/kap_8/advanced/t8_1_1.html

5.4 DSRD-Based Pulsed Power Source Systematic Topological Optimization

(Islam Sarwar & Gyanendra Bhattarai)

5.4.1 *Problem Statement, Approach, and Context*

***Primary Problem*:** Inductive energy storage (IES) and release pulse generators that use drift-step recovery diodes (DSRDs) can be used as the fundamental units of all-solid-state high-power microwave (HPM) systems. The output from DSRD-based pulsers can then be fed into sub-nanosecond pulse sharpeners to achieve ultra-short high-voltage pulses. While DSRD-based pulsers can theoretically achieve the targeted 1's of GW in 1's of ns, their circuits are not topologically optimized to achieve high voltage gain (peak pulse voltage/prime source voltage), thus requiring large and heavy high-voltage (multiple kV) prime power supplies to achieve the required 100's of kV pulses. They also necessitate liquid-based cooling systems to dissipate the excess heat they generate during operation, further adding weight and rendering them impractical for Navy afloat missions.

***Solution Space*:** Systematically develop optimum circuit topology to maximize the voltage gain, and thus the peak voltage, peak power, and volumetric power density of DSRD-based HPM systems. Minimize the heat loss to be able to air cool by increasing energy efficiency through optimization of circuit elements without sacrificing the desired nanosecond risetime of the pulses generated. Air-cooled IES pulse generators using optimum DSRD stacking can remove the need for photo-triggered switches and their laser sub-systems. They are ideal for triggering sub-nanosecond rise-time sharpeners (SAS, D-NLTL, etc.), reducing overall cost, volume, and weight.

***Sub-Problem*:** DSRDs are not domestically available COTs components, but rather manufactured in small-batch quantities, with statistically significant variations in their performance parameters. In addition, our current SPICE models of these diodes may not be accurate due to unknown device parameters such as carrier distribution, carrier lifetime and the limiting current that we can pump without affecting the diode recovery property (see section 5.1 and 5.3) during high-voltage transients. These issues may lead to an inaccurate simulation model of the pulser and discrepancies between simulated and experimental results.

***State-of-the-Art (SOTA)*:** Air-cooled DSRD-based pulsers (equivalent in size to the pulse generators developed for this effort, i.e., ~0.01-m^3, ~2-kg) can achieve <20 kV, 1–2 ns risetime, and <4 ns FWHM across a 50 Ω load with a PRF of <15 kHz in burst mode. Available literature on IES pulse generators only describes a few circuit configurations, and there is a lack of comprehensive investigation of circuit topologies and optimization to achieve maximum gain and efficiency and reduce thermal load. Additionally, these pulsers are expensive and are not available within the United States.

***Solution Proposed*:** Develop different DSRD circuit topologies implementing series and parallel combinations of DSRDs (to increase reverse breakdown voltage and diode current, respectively) to minimize circuit components, such as inductors, capacitors, and switches. Systematically identify the best circuit topology and optimize the circuit components through physics-based DSRD pulser circuit theory and SPICE simulation to

maximize voltage gain and efficiency while minimizing the prime source voltage and thermal load.

Risks, Payoffs, and Challenges:

***Risks*:** All-solid-state DSRD-based IES pulsers require many other electronic components. Most importantly, the current pumping capability of available MOSFETs/electronic switches is limited, which may make maximizing the output voltage impossible even though the DSRDs are capable of higher current and output voltages.

***Payoffs*:** Being able to simulate and fabricate DSRD-based pulsers using physics-based pulser theory, partnered with US-based DSRD manufacturers, will enable a comprehensive domestic ability to optimize, produce, and evaluate these nanosecond pulsers.

***Challenges*:** Domestically manufactured (U.S.-based) DSRDs, which possess sub-optimal doping profiles, may lead to sub-optimal pulse generators. Accurate spice modeling of the diodes could be affected by expected wide variability in the diode characteristics or unavailability of advanced device characterization techniques. Determining the superlative ratio of design/development (through numerical analysis) to the effort put towards experimental testing/evaluation of the DSRD pulser is challenging due to the novelty of the approach. Extending the theory of single (1×1) pulse generator to cascaded (M×N) generator to increase the output will be very complex and may require significant time and computing power.

5.4.2 Tasks and Milestones / Timeline / Status

(A) Milestone – Develop theory of DSRD pulse generator to facilitate optimization of 1×1 pulse generator [***Completed JAN22***]

(B) Milestone – Extend the theory developed in Milestone A to facilitate optimization of M×N pulse generator [**JAN–MAY22** / ***Ongoing***].

(C) Milestone – Construct/demonstrate a DSRD-based 1x1 pulse generator prototype based on theory developed in milestone (A) and obtain performance data for multiple combinations of diode stacks [**JAN–JUN22 / *Ongoing***].

(D) Milestone – Construct/demonstrate a DSRD-based 4×2 IES pulse generator prototype capable of producing $\geq$12 kV peak voltage, $\leq$1 ns risetime, $\leq$5 ns FWHM, $\geq$3 MW peak-power, $\geq$100 kHz PRF, $\geq$1,000 shots-per-burst, $\geq$500 number of bursts [*On hold*].

(E) Milestone – Develop waveform inverter which, when combined with the pulser from Milestone C, enables a balanced differential waveform output with >90% inverted signal fidelity. [***Completed DEC21***].

(F) Milestone – Construct/demonstrate a M×N pulse generator prototype capable of producing $\geq$20 kV peak voltage, $\leq$1 ns risetime, $\leq$2 ns FWHM, $\geq$8 MW peak-power, $\geq$100 kHz PRF, and $\geq 2\sigma_{Vpeak}$, which operates in continuous-burst mode as a viable candidate for OSPRES Contract source alternative [*on hold until Milestones B, D, & E are completed*].

5.4.3 *Progress Made Since Last Report*

(B) Theory development of a 1×2 DSRD pulser is underway. The complete status of the theory development will be presented in the next reporting period.

(C) A modular driver circuit for optimized MOSFET operation is designed and simulated which is capable of driving four parallel MOSFETs to increase forward pumping current through the diodes. The new driver circuit with TOTEM pole configuration needs specific bipolar junction transistors which have been ordered from the United Kingdom due to their unavailability in the US.

5.4.4 *Technical Results*

(B) Parallel Stacking of DSRD pulser: 2×1 Pulser Theory

In the previous reporting period (MSR May 2022), we presented the theory of series cascading of individual 1×1 pulsers to increase the overall voltage output, similar to two stage amplifiers. The idea of stacking and cascading pulsers is to use the output pulse obtained from the first pulser (first stage) to reverse bias the second stage. Along with the circuit working principle, we also outlined some circuit limitations such as maximum MOSFET voltage, maximum MOSFET current, and problem in high-frequency and high-voltage impedance transfer. In this report, we present a scheme of stacking individual 1×1 pulsers in parallel configuration so that the total output is increased without exceeding the circuit limitations explained above.

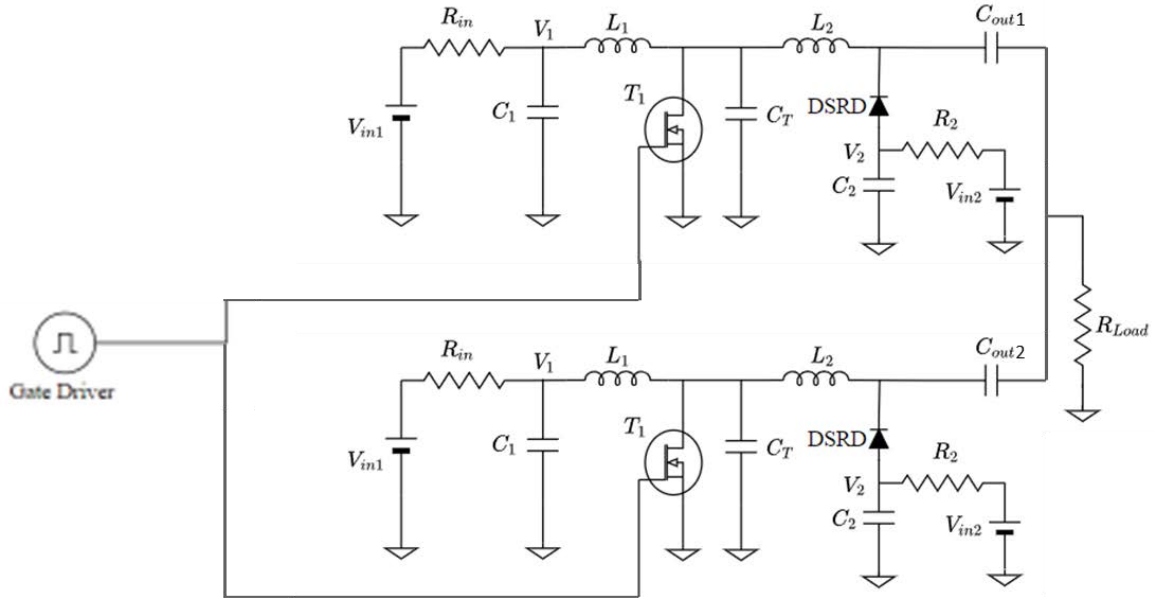


Figure 5.4.1. A 2×1 DSRD pulser—a parallel stacking of two individual 1×1 pulsers. The output of two pulsers are coupled to the load capacitively via the output capacitors C_{out1} and C_{out2}.

Figure 5.4.1 shows a parallel stacking of two 1×1 pulser. The two pulsers are connected to a single load R_L through two coupling capacitors C_{out1} and C_{out2}. The low frequency

operation of two individual pulsers, before the final output is obtained, are not significantly affected by the capacitive coupling. At the time when the two pulsers generate output pulse of very short risetime (high-frequency operation), the capacitive coupling between the two pulsers decreases the overall output impedance below 50 Ω. In an ideal case, when the output impedance remains 50 Ω, the total output from the stacked pulser will be double of the individual pulser's output. However, due to the lowered output impedance, the output in real case is lower than double of the individual pulser's output.

Design and Optimization Considerations

a. Number of Diodes: As the parallel stacking of 1×1 pulsers increases the output voltage, the number of diodes in each 1×1 pulser should be increased so that the total breakdown voltage of the diodes in series becomes equal or greater than the expected output voltage from the combined pulser. For example, we have reported a theoretical design and simulation of a 1×1 pulser producing 10 kV output using 21 diode stacks in the previous MSR report (MSR APR 2022). To produce an output of 20 kV by stacking such two pulsers in parallel, both pulsers should have 42 diode stacks in series to support the required output. This increases the number of diodes by 4 times to produce double the output of a 1×1 pulser. Thus, in an ideal case, to increase the output voltage by a factor n, the total number of diodes in the stacked pulser increases by a factor of n^2.
b. Optimization: As the number of diodes in an individual 1×1 pulser increases, the total series resistance of the diodes also increases, which requires a complete re-optimization of the individual pulsers so that a final parallel stacking can be achieved.
c. Pulser Synchronization: To produce a combined output voltage, the individual pulsers should be perfectly in sync so that the energy stored on the inductors of the individual pulsers are released simultaneously to the load, increasing the load current, and thus the output voltage.

With these considerations, we have optimized a 2×1 stacked DSRD pulser within the working limit of the gate driver and MOSFETs. The circuit parameters and output voltage are summarized below.

$$
\begin{aligned}
V_{in1} &= 110\ \text{V} \\
V_{in2} &= 110\ \text{V} \\
L_1 &= 38\ \text{nH} \\
L_2 &= 94\ \text{nH} \\
C_1 &= 200\ \mu\text{F} \\
C_2 &= 195\ \text{nF} \\
\text{Trigger Length} &= 470\ \text{ns} \\
\text{Number of Diodes in one branch} &= 42 \\
\text{Total number of Diodes} &= 84 \\
\text{Individual Output} &= 15.5\ \text{kV} \\
\text{Stacked Output} &= 23.0\ \text{kV}
\end{aligned}
$$

(C) 1×1 DSRD Pulser Fabrication and Testing:

A pulser circuit board consisting of a re-designed MOSFET driver to drive four MOSFETs in parallel and capable of producing 10 kV output pulses has been populated (Figure 5.4.2). Along with the increased target output voltage, the circuit components have been updated to increase the pulse repetition rate of up to 100 kHz.

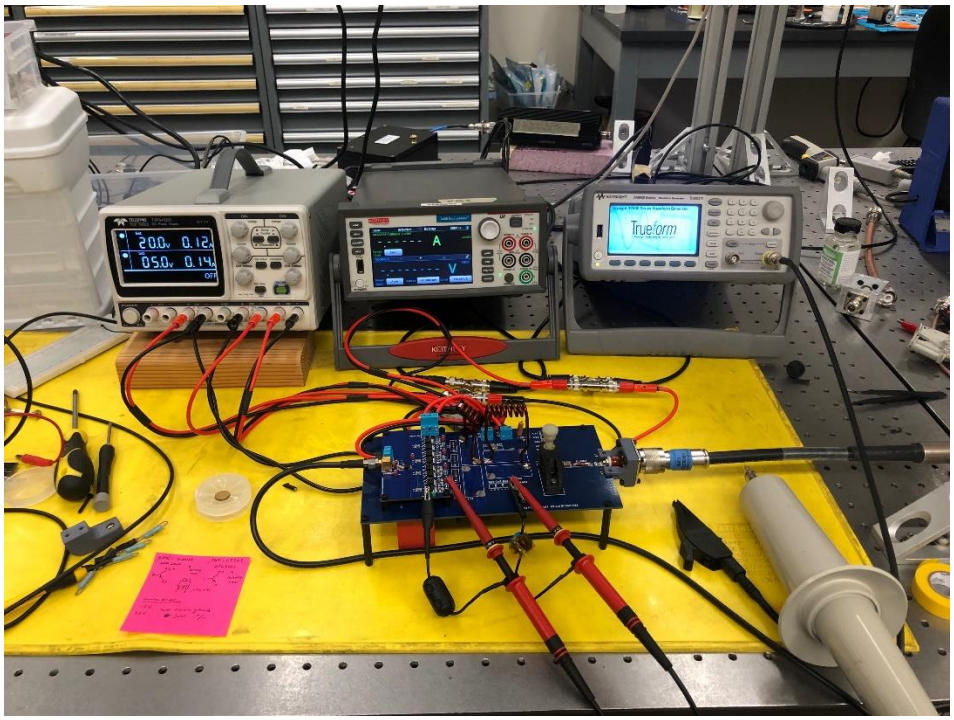


Figure 5.4.2. Experimental setup of 1×1 DSRD pulser designed to produce 10 kV output pulse.

Among the circuit components, we have been fabricating the inductors using thick copper wires because of the amplitude of current expected to flow through them. However, as the wire thickness increases, obtaining the theoretical inductance of such inductors becomes increasingly difficult. The accurate measurement of such custom-built inductors also becomes difficult due to their self-capacitances and series resistances. To accurately characterize the inductors, a significant effort has been given to impedance measurement and the analysis of data using impedance spectroscopy. As the impedance measurement can be significantly affected by stray inductance and capacitance of measurement fixture, and the effect of magnetic materials and ground plane around the inductor, we have designed a custom-built fixture (as shown in Figure 5.4.3) made of non-metallic and non-magnetic fixture body to accommodate a wide range of inductor sizes while minimizing the stray inductance and capacitances.

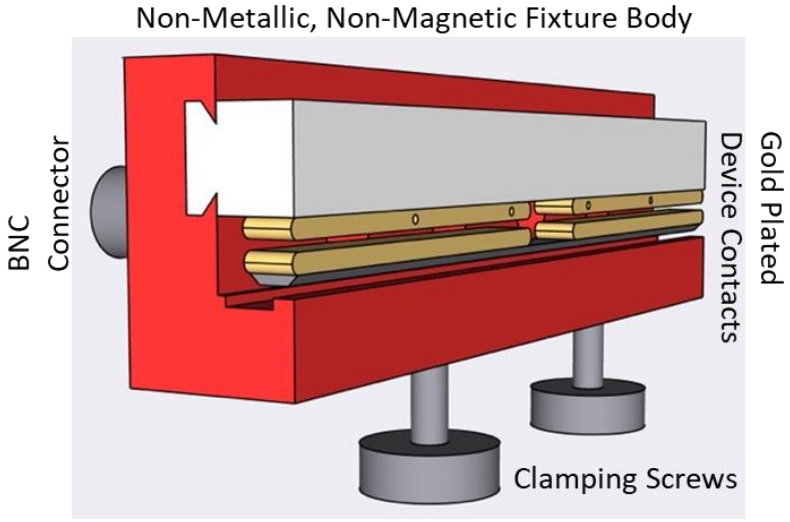


Figure 5.4.3. Newly designed Inductance measurement fixture made of non-metallic, non-magnetic fixture body.

As our effort for accurate inductance measurement is ongoing, we have tested the performance of the newly fabricated pulser with inductors $L_1 = 63\ \mathrm{nH}$ and $L_2 = 125\ \mathrm{nH}$. The inductances are measured with HIOKI IM 3536 LCR meter, however, their complete characterization has not been possible due to fixture issues. Thus, we expect these values to have moderate to significant variations.

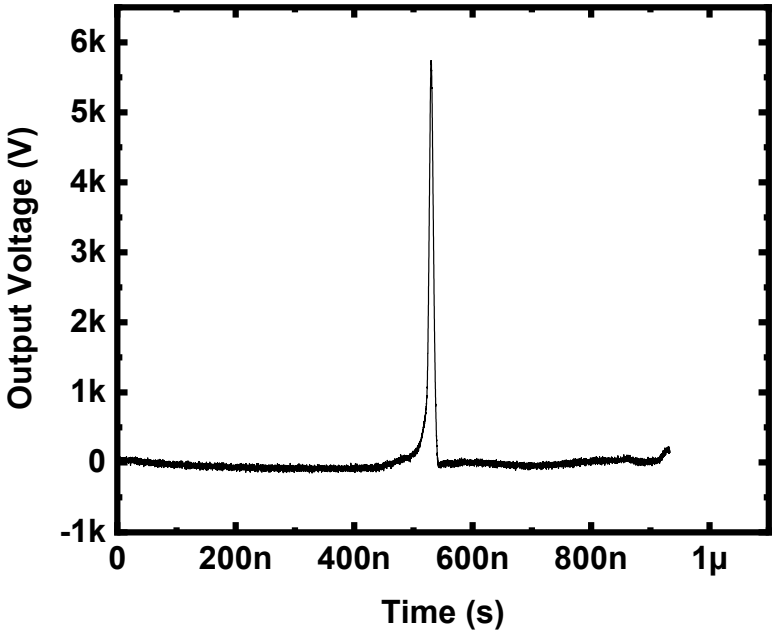


Figure 5.4.4. Output voltage pulse from a 1×1 DSRD pulser using EG1571, EG1572, and EG1573 7-stack diodes designed to produce 10 kV output.

Figure 5.4.4. shows the output pulse voltage from the newly built DSRD pulser using three 7-stack diodes (EG1571, EG1572, and EG1573). Although the output is still lower than the expected value, we believe that the output can be significantly improved once the problem in manufacturing and characterizing the inductors gets solved.

5.4.5 *Summary of Significant Findings and Mission Impact*

(B) A systematic optimization of a 1×1 pulse generator based on the theory covered in the DEC2021 MSR reporting period was presented. In this reporting period, we have presented an optimization sequence considering the circuit limitations. Based on the previous measurements and simulations, we hypothesized that the lowered output voltage obtained from the previous pulsers could be due to higher diode ON-state series resistance than the value considered for simulation. A proposed working principle for a two-stage DSRD pulser has been described in the MAY2022 MSR reporting period, however, with certain outstanding questions that may inform the efficacy of multi-stage DSRD pulsers. A new approach for stacking multiple 1×1 pulsers in parallel to increase the output voltage while keeping the MOSFET current and voltage within safe operating limit has been proposed.

(C) Using the 28-stack pulser, maximum peak outputs of 6.7 and 7.5 kV are obtained for a trigger length of 700 ns using a prime source voltage of 120 and 170 V. A newly designed and fabricated pulser with four MOSFETs in parallel achieved an output of 6.2 kV using three 7-stack diodes, an improvement compared to the previous version in the context of total number of diodes. The lower-than-expected output (10 kV) is believed to be due to inaccurate values of custom-built inductors and inaccurate diode series resistance. Based on the DSRD pulser output using a single 7-stack diode, the reverse breakdown voltage of the EG1600 series diodes is estimated to be ~650 V. Measurement of circuit voltages at different nodes confirms the circuit performance matching the SPICE simulation. Obtained lower output voltages indicates requirement of more accurate DSRD SPICE Model which takes account of forward diode series resistance, carrier distribution and recombination during high voltage transients.

(D)

Table 5.4.2. Comparison of DSRD-based IES Pulse Generator Performance.

KPM	Units	MIDE - V1 Previous	MIDE - V2 Previous	MIDE – V3 Current	Kesar *et al.* SOTA	MI-PPM0731 COTS
V_{supply}	V	225	180	120	300	160
T_{ON}	ns	100	340	700	?	200
V_{peak}	kV	5.59	**7.35**	**6.7**	5	6.3
Gain	V/V	24.8	**40.8**	**55.8**	16.7	39.4
$\tau_{rise,20\text{-}90\%}$	ns	1.2	1.1	3.1	1.96	0.12
dV/dτ	kV/ns	4.66	6.44	2.16	2.55	**52.50**
FWHM	ns	2	5.48	6.90	2.27	0.35
PW	ns	5	7	7	3.5	2.5
Z_{LOAD}	Ω	50	50	50	50	50
P_{peak}	MW	0.625	**1.080**	**0.905**	0.500	0.794
E_{pp}	mJ	0.125	0.154		0.143	0.318
PRF_{max}	kHz	100	100		100	15
Burst	shots	100	100	*N/A*	*N/A*	100
	%	100	100	*N/A*	*N/A*	100
SD_{Vpeak}	σ	> 2	**> 2**	*N/A*	*N/A*	*N/A*
	%	96.5	**97.8**	*N/A*	*N/A*	*N/A*

(E) Successful construction and operation of a 2×2 DSRD-based IES pulse generator prototype has been completed, which meets or exceeds the required key performance metrics. Shown in Table 5.4.2 are the previous and current pulse generator performance specifications in comparison to a similar 2×2 pulser developed by Kesar et al. [1] using DSRDs, and to that of a commercial off-the-shelf (COTS) DSRD pulser of similar space and weight developed by Megaimpulse (i.e., PPM-0731), which also uses DSRDs with silicon avalanche shapers (SAS) [2]. Although the Megaimpulse pulser utilizes a SAS with a <500 ps risetime (a threshold we do not intend to go below due to Commerce Controlled List limitations), it is interesting to compare the results of linear voltage gain and peak power of this system, to that of one that utilizes a SAS. The current permutation of the 2×2 DSRD-IES pulser developed by MIDE under the ONR OSPRES Grant is able to achieve a higher peak voltage and shorter risetime than DSRD-based pulsers reported in the literature of comparable space and weight as well as those commercially available. The ability to generate a linear voltage gain of 40.8 to produce over a Megawatt of peak power into a 50 Ω load while achieving a peak voltage output standard deviation of 2σ when operating at a PRF of at least 100 kHz, brings this technology to the forefront of viable options to potentially support the Naval afloat mission.

(F) Discrepancies exist in the obtained pulser and device characterization data for different series combinations and different samples of 7-stack DSRDs, which may be attributed to the inconsistencies in their manufacturing process. Future work in the coming months include testing multiple stack diodes in pulser configurations with MOSFET paralleling using modular gate driver circuit to identify better diodes and increase the output voltage to >9 kV from the 1x1 pulser configuration. Future work also includes the design and testing of 2×2 or higher configuration DSRD-based pulsers using more combinations of series-connected as well as parallel-connected DSRD stacks.

5.4.6 *References*

[1] https://www.onsemi.com/pdf/datasheet/nvh4l020n120sc1-d.pdf

[2] https://cms.wolfspeed.com/app/uploads/2020/12/C2M0045170P.pdf

5.5 All-Solid-State Sub-ns MW Pulse Generators with Semiconductor Sharpeners

(Gyanendra Bhattarai)

This sub-project is currently on hold as focus is directed toward Section 5.4. Please review the January 2022 MSR for the most recent project overview and status.

6 Thermal Management

6.1 Ultra-Compact Integrated Cooling System Development

(Sam Sisk, Roy Allen, and Sarvenaz Sobhansarbandi)

6.1.1 *Problem Statement, Approach, and Context*

Primary Problem: A thermal management system (TMS) is required for cooling semiconductor-based pulse-power devices, using anywhere from 50 to 200 W, with the goal of maintaining the semiconductor device temperature below 80 °C to avoid chip damage. The proposed system must increase cooling densities at a rate of at least 1 kW/cm^2, the current state of the art, while decreasing pumping power requirements, in-line with the SWaP-C^2 objective. This device also needs to be small enough to be used anywhere from server warehouses to drones, thus 1 cm^2 is targeted, with scaling up remaining a possibility.

Solution Space: To achieve such high cooling densities, we propose three potential solutions: an ultra-compact TMS (UC-TMS) to be directly integrated into the semiconductor, a monolithically integrated manifold microchannel chip (mMMC) TMS, and an updated jet impingement TMS (JI-TMS). The UC-TMS and JI-TMS are expected to achieve enhanced heat transfer rates due to the turbulent flow from the array of nozzles. The mMMC-TMS is expected to have low pressure losses while still transferring sufficient heat. The JI-TMS and UC-TMS are expected to have lower pressure losses if the outlet cross-sectional surface area for the transfer fluid is equivalent to the inlet cross sectional area. As the proposed TMS dimensions are restricted to 1 cm^2 surface area, the required pumping power should be kept to a minimum. An array of micro-sized jet nozzles will provide a turbulent flow onto a microchannel section directly on the semiconductor device.

Sub-Problem: The turbulency formed from the array of nozzles creates an extreme pressure loss from the large amount of jet nozzles (over 200) and a flow diameter of 100 microns. The pressure must be sustained to enable proper cooling and circulation processes.

State-of-the-Art (SOTA): Integrated chip cooling is being widely used to dramatically increase the operational power of high-voltage silicon-based power devices. However, the current SOTA devices include surface to surface contact points that rely on cohesive connections. These connections increase the amount of material through which heat must transfer to the coolant, thus limiting the heat removal rate.

Objective: To design, simulate, and compare three different TMSs (ultra-compact, monolithically integrated manifold microchannel chip, and jet impingement) under the same operating conditions, and optimize through an iterative process. The proposed UC-TMS and JI-TMS design are based on refining in-chip jet-impingement geometry through leveraging theory and a parametric evaluation of nozzle geometry, flow channel arrangements, and outlet to inlet area ratios. The mMMC TMS performance will be compared with the corresponding results available in the literature and with the results from the other two designs.

Challenges: The manufacturing techniques needed for integrated chip cooling systems have not been entirely adopted. The proposed compact designs are restricted due to the low tolerances needed for the geometries of the nozzles and heating plate; the manufacturing process must be capable of layering the silicon TMS onto the semiconductor.

Risks: With a system so compact, the pressure drop could be a large issue regarding the objective heat dissipation rate. An extreme pressure drop would potentially cause the coolant to flow backwards, causing less fluid-to-solid interaction.

6.1.2 *Tasks and Milestones / Timeline / Status*

(A) Design a Si base 1 cm^2 UC-TMS, JI-TMS, and mMMC-TMS to achieve a heat dissipation rate of 1 kW/cm^2. The device will also need to be designed in a way where it can be manufactured as proposed. / MAR22–MAY22 / In Progress

(B) Using the computational fluid dynamics (CFD) ANSYS software, simulate the results for the UC-TMS, JI-TMS, and mMMC-TMS all operating under the same conditions. Compare the results and make improvements to the designs to meet the target metrics. This process will continue until an optimal design is chosen to move forward with. / MAY22–JUN22 / In Progress

(C) Using the optimal design, perform ANSYS simulations using de-ionized water or Si-C nanofluid as the coolant and see how fluid type changes the effectiveness of the TMS. Other fluid types may be researched as pressure drop is a large factor. / June22–JULY22 / Upcoming

- Prove simulations from previous literature to show capable design configurations with acceptable pressure drop and steady temperature.

(D) With all problems addressed with simulation results and having a single design able to be manufactured, manufacture a prototype to begin experimental testing and evaluation / AUG22– OCT22 / Upcoming

6.1.3 *Progress Made Since Last Report*

(A) A design was created for a JI-TMS, this design met all geometric criteria set. The design consists of over 400 nozzles each of diameter 1 mm. The nozzles are spaced 2.5 mm in a triagonal pattern to increase the total number that can be fit into the 1 cm^2 area. These decisions on geometry were calculated from equations found within Incorpra; the equations for geometrics specifications of the array of jets seem to mostly rely on the diameter of the nozzles.

The features that were most integral to heat removal performance were the heat transfer coefficient ($\bar{h}$), a dimensionless ratio of the diameter to array spacing diameter (Ar), illustrated in Figure 6.1.1., and another dimensionless ratio of nozzle height from heated surface to nozzle diameter (H/D), illustrated in Figure 6.1.2.

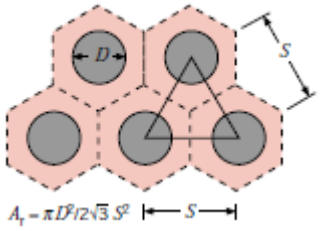


Figure 6.1.1. Diagram for Ar Relation.

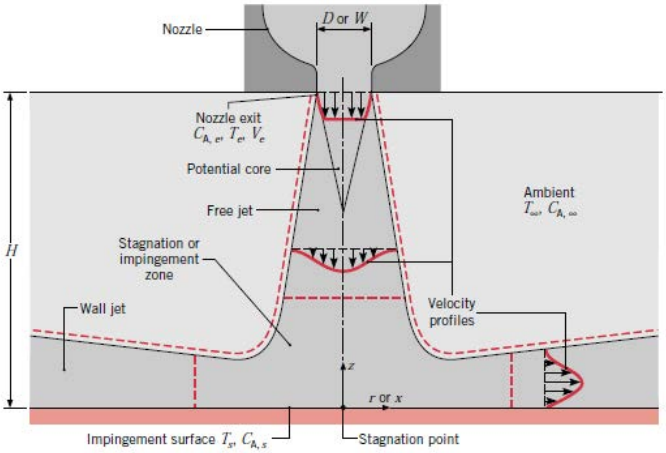


Figure 6.1.2. Middle cross section of impinging jet.

(B) Given that a JI-TMS design was found, simulations were conducted using ANSYS Fluents CFD software. The JI-TMS design was split into two sections called the entry stage and exit stage. This was done too save on computation time as the design has over 14 million elements to calculate on.

6.1.4 *Technical Results*

(A) The JI-TMS design was achieved using equations found in the Incropera book, as provided below. The geometric governing equations were all input into an excel spreadsheet. This spreadsheet made it much easier to tweak the nozzle diameters and the incoming fluid velocity.

$$\overline{Nu} = .5K\left(A_r\frac{H}{D}\right)G\left(A_r\frac{H}{D}\right)\mathrm{Re}^{2/3}Pr^{.42} \tag{1}$$

$$K = \left[1+\left(\frac{\frac{H}{D}}{\frac{0.6}{Ar^{.5}}}\right)^6\right]^{-0.05} \tag{2}$$

$$G = 2Ar^{.5}\frac{1-2.2Ar^{.5}}{1+0.2\left(\frac{H}{D}-6\right)Ar^{.5}} \tag{3}$$

$$Ar = \frac{\pi D^2}{2\sqrt{3}S^2} \tag{4}$$

$$Re = \frac{VD}{\nu} \tag{5}$$

$$\overline{Nu} = \frac{\bar{h}D}{k} \rightarrow \bar{h} = \frac{\overline{Nu} * k}{D} \tag{6}$$

$$q = \bar{h}A(\Delta T) \tag{7}$$

$$2000 \leq Re \leq 100{,}000$$

$$2 \leq H/D \leq 12$$

$$.004 \leq Ar \leq .04$$

One of the most important goals of the design is to be able to dissipate the heat of incoming power of 200 W; knowing this paired with knowing the max surface area and max change in temperature, a min value for $\bar{h}$ can be found using eq (7) which is 33333.33 $\frac{W}{m^2K}$. The other main geometric feature that determined the greatest heat removal performance have values of 0.04 for Ar and 2 for H/D for all cases. These values are used as constants in the spreadsheet below.

D (m)	S	H (m)	Re	K	G	Nu	h
0.001	0.0025	0.01	10000	0.574416	0.094678	10.93056	6536.474
0.00095	0.004522339	0.0019	9500	0.995801	0.266667	51.57695	32466.34
0.0009	0.004284321	0.0018	9000	0.995801	0.266667	49.75098	33056.76
0.00085	0.004046303	0.0017	8500	0.995801	0.266667	47.89085	33692.62
0.0008	0.003808286	0.0016	8000	0.995801	0.266667	45.99387	34380.42
0.00075	0.003570268	0.0015	7500	0.995801	0.266667	44.05692	35128.05
0.0007	0.00333225	0.0014	7000	0.995801	0.266667	42.07641	35945.27
0.00065	0.003094232	0.0013	6500	0.995801	0.266667	40.04813	36844.28
0.0006	0.002856214	0.0012	6000	0.995801	0.266667	37.9671	37840.55
0.00055	0.002618196	0.0011	5500	0.995801	0.266667	35.82738	38954.14
0.0005	0.002380178	0.001	5000	0.995801	0.266667	33.62172	40211.58
0.00045	0.002142161	0.0009	4500	0.995801	0.266667	31.34115	41648.91
0.0004	0.001904143	0.0008	4000	0.995801	0.266667	28.97432	43316.61
0.00035	0.001666125	0.0007	3500	0.995801	0.266667	26.50648	45288.21
0.0003	0.001428107	0.0006	3000	0.995801	0.266667	23.91778	47676.1
0.00025	0.001190089	0.0005	2500	0.995801	0.266667	21.18036	50663.42
0.0002	0.000952071	0.0004	2000	0.995801	0.266667	18.25268	54575.51
0.00015	0.000714054	0.0003	1500	0.995801	0.266667	15.06725	60068.12
1E-04	0.000476036	0.0002	1000	0.995801	0.266667	11.49847	68760.84
5E-05	0.000238018	1E-04	500	0.995801	0.266667	7.243581	86633.22

Figure 6.1.3. Spreadsheet with varying nozzle diameters.

(B) The decided geometry of a 1 mm diameter was created using Solidworks, as shown in Figure 6.1.4. The file was then converted into a format that can be simulated with ANSYS FLUENT. The model used was Epsilon-k as the system is turbulent due to the Re greater than 2000 and the Energy Model as there was energy transfer within the system. As stated previously the simulation had to take place in two separate simulation stages.

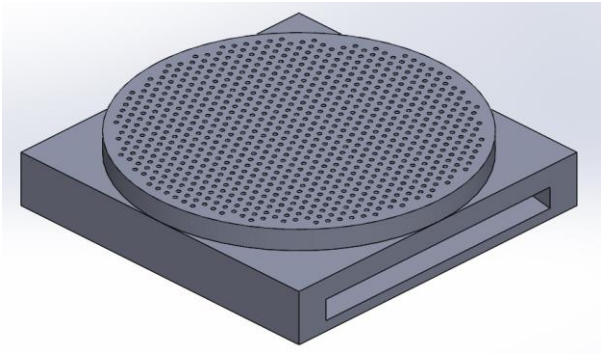


Figure 6.1.4. Solidworks geometry.

- The entry stage was primarily simulated to find the average velocity at the end of the nozzles. Once this velocity was known the exit stage simulation took place and using the energy model the heated plate was given an operating condition heat flux of 2000 kW/m^2. The following figures show the pressure and velocity contours.

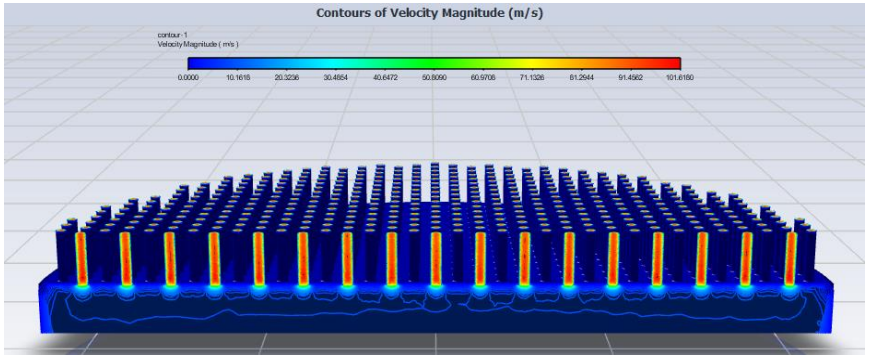


Figure 6.1.5. Contour plot of velocity at entry stage.

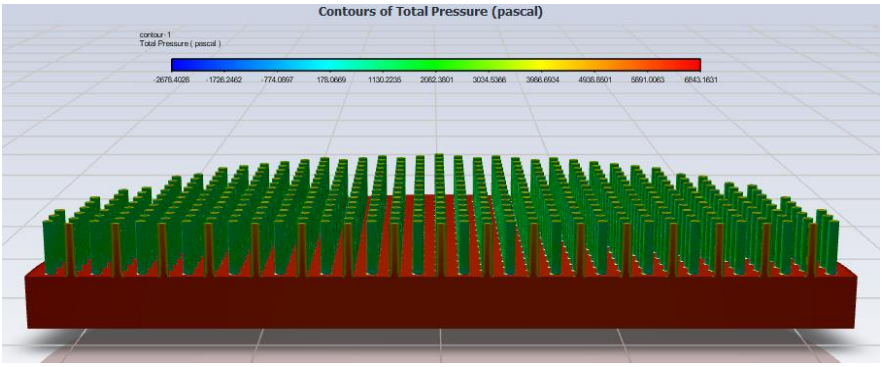


Figure 6.1.6. Contour plot of pressure at entry stage.

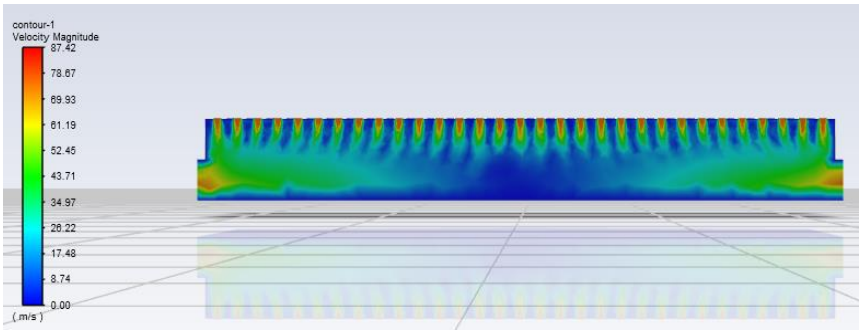


Figure 6.1.7. Contour plot of velocity at exit stage.

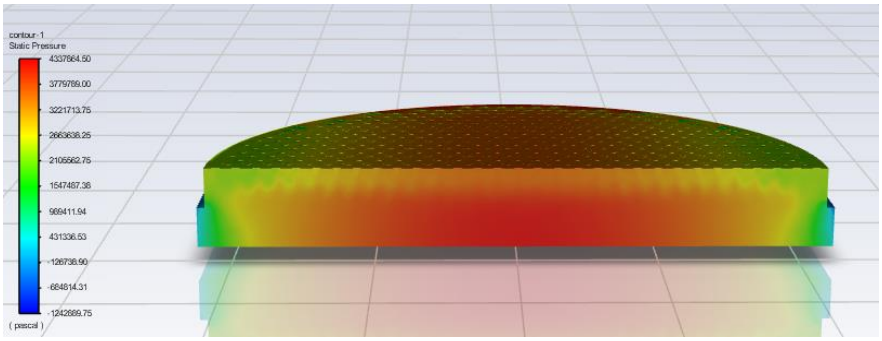


Figure 6.1.8. Contour plot of pressure at exit stage.

6.1.5 *Summary of Significant Findings and Mission Impact*

(A) After many iterations of various geometries, we narrowed down the features most integral to the performance of a JI-TMS. In the following months, improved geometries will be designed and compared for further simulations.

(B) The simulations done for the first trial of a JI-TMS geometry showed heat removal from the source, keeping the system below the 80 degree Celsius limit while also not having huge losses in outlet pressure. The deficiency with the result is that the incoming velocity might not be achievable in the real world, so future designs will need to factor in a realistic flow rate.

6.1.6 *References*

[1] Incropera, Frank P. Fundamentals of Heat and Mass Transfer. 7th ed. John Wiley, 2011.

7 Pulse-Forming Networks

7.1 Diode-Based Nonlinear Transmission Lines

(Nicholas Gardner)

Attention on this sub-project is being entirely directed toward the preparation of manuscripts and an associated dissertation. A summary report will be provided in Summer 2022, and this will serve as a placeholder until this time. Please see the January 2022 MSR for the most recent summary and status and the Outputs section for papers in preparation or published.

7.2 Continuous Wave Diode-NLTL based Comb Generator

(Nicholas Gardner and John Bhamidipati)

Work on this sub-project is currently on hold to focus on reporting and other sub-projects. Please see the May 2022 MSR for the most recent summary.

7.3 Pulse-Compression-Based Signal Amplification

(Feyza Berber Halmen)

7.3.1 *Problem Statement, Approach, and Context*

Primary Problem: Solid-state amplifiers, such as gallium-nitride-based high electron mobility transistors (GaN HEMT), can be used as high power microwave (HPM) sources to achieve the SWAP-C2 performance metrics necessary to support the cUAV Naval afloat mission. However, even the best high-power GaN HEMTs are limited to 2–3 kW of peak power, much lower than the 0.1 to 3 MW pulsed power available from traditional HPM sources such as travelling wave tubes (TWTs). Achieving a power density of 1 W/cm^2 at a distance of 10 m with a high gain (≥ 10 dBi) narrow-band antenna requires an input power increase of two to three orders of magnitude. Power combination methods to achieve an effective radiated power (ERP) at MW scale require 10 s to 100 s of GaN HEMTs, compromising the SWAP-C2 performance.

Solution Space: Pulse compression techniques are used to increase the peak power and lessen the pulse width in HPM applications. Adapting pulse compression at the GaN HEMT or any other SWAP-C2 compatible source output can achieve sufficient ERP with an optimal radiating element.

***Sub-Problem*:** Pulse compression is generally used to generate a pulsed output with a high peak output power (P_{out_peak}) and a wideband frequency content from a DC input voltage. The main challenge lies in identifying a pulse compression technique that can be used to amplify a narrowband RF input signal. Some of the circuit elements for common pulse compression techniques, such as the saturable inductors used for energy storage in magnetic pulse compression (MPC), exhibit increasingly lossy behavior with high frequency. Another challenge will be to determine, if any exist, the operating frequency limits of the suitable pulse compression technique for high-frequency, high-power signals.

State-of-the-Art (SOTA): Large magnetic pulse compression (MPC) circuits (>1 m^3, >1000 lbs) have demonstrated peak output power up to a few GWs. Smaller versions (~0.125 m^3, 50 lbs to 100 lbs) can achieve 7.5 MW peak power [1].

Deficiency in the SOTA: Traditional MPC systems are large (few meters long), leverage huge transformers, and require liquid coolant such as transformer oil, which leads to undesirable system mass values of ≥1000 lbs. They are used for generating medium or high pulse power traditionally from DC or AC (50/60 Hz) high voltage supplies. There is no known example of high-frequency signal amplification utilizing MPC.

Solution Proposed: Developing a pulse compression circuit that will act as a high-power signal amplifier with a gain of ≥10. Utilizing magnetic pulse compression, or any other suitable pulse compression method, for high power signal amplification with source fidelity.

Relevance to OSPRES Grant Objective: Pulse compression will enable a size and cost efficient solution to high power signal amplification that will lead to HPM source development with optimal SWaP-C2 parameters.

Risks, Payoffs, and Challenges:

Challenges: Modeling pulse compression circuits for high-frequency operation can present a challenge. Pulse compression circuits are generally evaluated in SPICE simulators with low frequency AC / transient simulations. SPICE is a lumped-element model simulator and cannot solve for the distributed-element model required at high frequencies where the wavelengths become comparable to the physical dimensions of the circuit. Some circuit components, such as the saturable inductor in the MPC, are not available in SPICE or many other simulators and need to be modeled using behavioral models and proprietary material data. Pulse compression circuit modeling, especially at high frequencies, needs to be investigated.

Risks: Pulse compression methods are usually lossy in nature and generate a considerable amount of heat; therefore, designing a proper cooling method must be carried out, which may inadvertently increase the volume (size and weight) of the overall design.

7.3.2 *Tasks and Milestones / Timeline / Status*

(A) Milestone – Demonstrate 2–3 times increase in peak power and compression gain using magnetic pulse compression (MPC) [*estimated completion by MAY22*].

1. Subtask – Model saturable inductors in LTSpice or Matlab/Simulink in order to be able to develop MPC simulations / NOV21 / Complete.
2. Subtask – Design MPC circuit with RF input and simulation in LTSpice or Matlab/Simulink to evaluate the resulting amplification and frequency content. / JUNE22 / *Ongoing*.
3. Subtask – Model the high frequency behavior of MPC circuit / NOV21 / Ongoing.
4. Subtask – Build and test the MPC prototype using bench top power supply / OCT21–AUG22 */ Ongoing*.

(B) Milestone – Investigate pulse compression methods other than MPC for feasibility *Ongoing*

1. Subtask – Study time reversal pulse compression to assess its compatibility with GaN-based source. JUNE22 / Complete.

(C) Milestone – Increase the compression gain available from PC.

(D) Milestone – Build and test SWAP-C2 compatible high-frequency PC prototype with GaN source.

7.3.3 *Progress Made Since Last Report*

(B.1) Time-reversal pulse compression (TR PC) has been evaluated for signal amplification. The TR output signal in the time and frequency domains and the conditions for TR PC gain have been investigated to determine the feasibility for increasing the GaN amplifier output power.

7.3.4 *Technical Results*

(B.1) Another pulse compression method, time-reversal, is investigated for GaN amplifier output power amplification. The time-reversal pulse compression method utilizes a resonant cavity and signal processing to generate a high-peak ultrashort pulse from an impulse. Figure 7.3.1(a) shows the architecture for the time reversal pulse compression system [2]. An ultrashort pulse is applied to a reverberant cavity, and the recorded impulse response (IR) is time reversed and re-applied to the same cavity. A reconstructed pulse, with higher peak power, is obtained at the output of the cavity. The output y(t) of the cavity after time-reversed impulse response (TR-IR) is the convolution of the impulse response h(t) and time-reversed impulse response h(T–t):

$$y(t) = h(t) * h(T - t) \tag{1}$$

T is the impulse response record time, and the reconstructed output pulse is formed at t=T, indicating a time delay determined by the response measurement duration. In the frequency domain, the output is given by [3]:

$$Y(\omega) = H(\omega)H(\omega) = |H(\omega)|e^{-j\Theta\omega}|H^*(\omega)|e^{j\Theta\omega} = |H(\omega)|^2 \tag{2}$$

Equation (2) indicates that signal fidelity is preserved, and phase errors caused by the dispersive cavity environment are corrected by the TR-PC process.

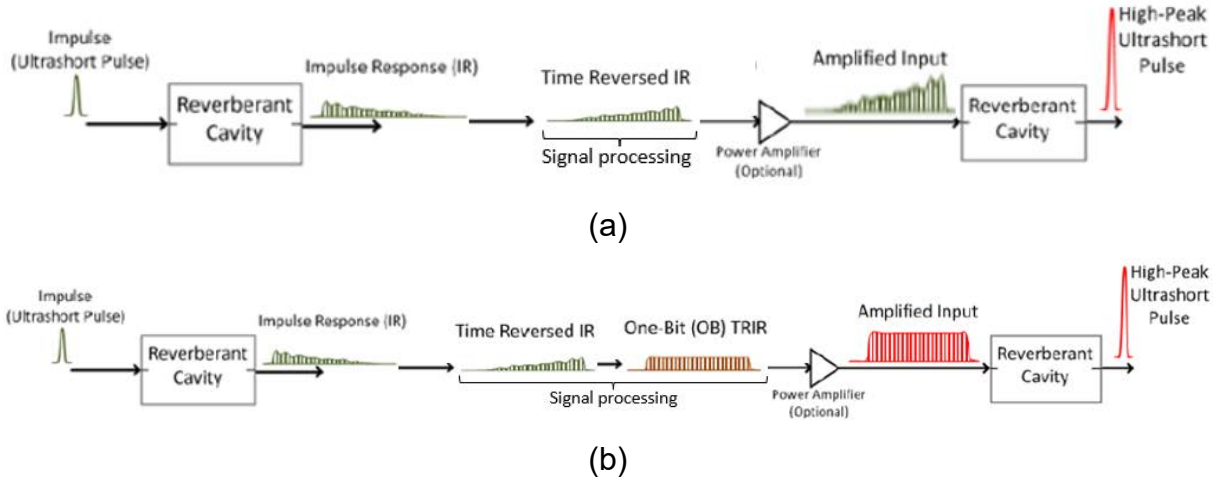


Figure 7.3.1. Architecture of (a) time reversal pulse compression and (b) one-bit time reversal pulse compression systems (adapted from [2]).

The compression gain of the reverberant cavity is defined as the ratio of cavity output signal peak magnitude to time reversed cavity input signal peak magnitude. The gain is calculated from the time-domain signal values in volts and then converted to decibels. Only a few dBs of compression gain is available from TR PC. In order to increase the gain, the process is modified to one-bit time-reversal pulse compression (OBTR PC), depicted in Figure 7.3.1(b) [2,3]. OBTR PC applies the signum function to the TR IR prior to cavity input, effectively increasing the energy per time of the TR signal. The compression gain is increased to over 20 dB with OBTR PC. However, time sidelobes are created with the OBTR, indicating compromised signal fidelity.

Figure 7.3.2 shows the input and output waveforms for the TR PC implementation from [2]. The original impulse input of 0.25 V is passed through the cavity to obtain the impulse response given in Figure 7.3.2(a). Figure 7.3.2(b) shows the reconstructed impulse after time reversal and re-transmission through the cavity. If the original impulse is considered as the input to the system, there is significant gain observed in the time-domain. Corresponding frequency domain plots $H(\omega)$ and $Y(\omega)$ are given in Figures (c) and (d), respectively. Frequency responses are normalized to an input impulse with magnitude of 1. The plots indicate that more than half of the input impulse is lost in the 2–9 GHz frequency band after the impulse is transmitted through the cavity. More loss is observed in the reconstructed signal after the TR IR is retransmitted through the cavity. Loss in frequency domain is expected as the resonant cavity is a passive, dispersive circuit component. Comparing Figures 7.3.2 (c) and (d) shows that signal fidelity is quite well-preserved through the TR IR process.

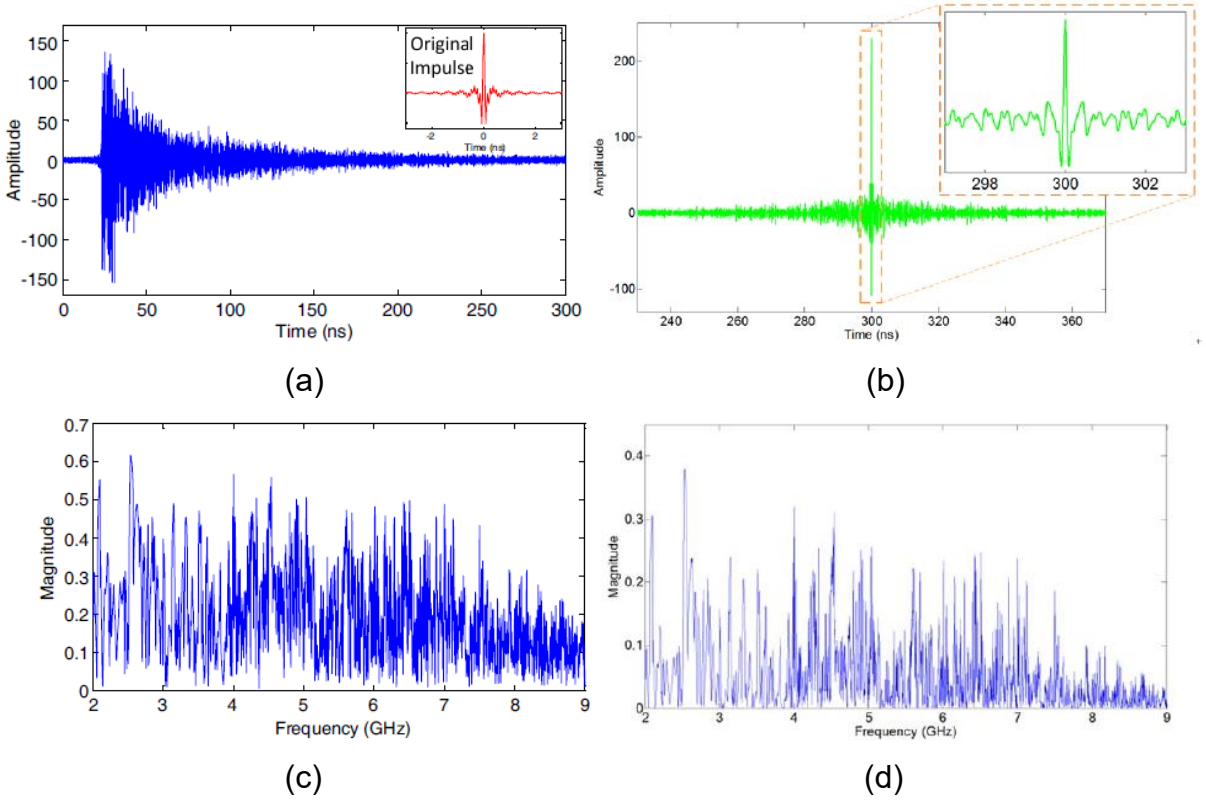
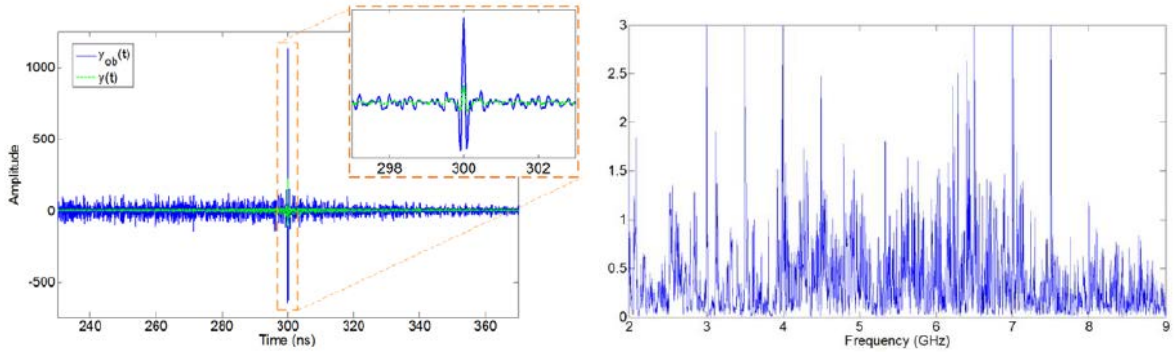


Figure 7.3.2. TR-PC input and output waveforms in time and frequency domains: (a) h(t) and original input impulse, (b) y(t), (c) H(ω), and (d) Y(ω) [2]

Figure 7.3.3 (a) and (b) show the time and frequency domain outputs after OBTR is applied to the same PC system. Figure 7.3.3 (a) depicts a significant increase in time-domain gain with OBTR. Gain, compared to the input impulse of 1, is also observed in the frequency domain for some frequencies according to Figure 7.3.3 (b). However, substantial alteration of the frequency content with OBTR process is noted after comparing Figures 7.3.3 (b) with 7.3.2 (c) and (d).



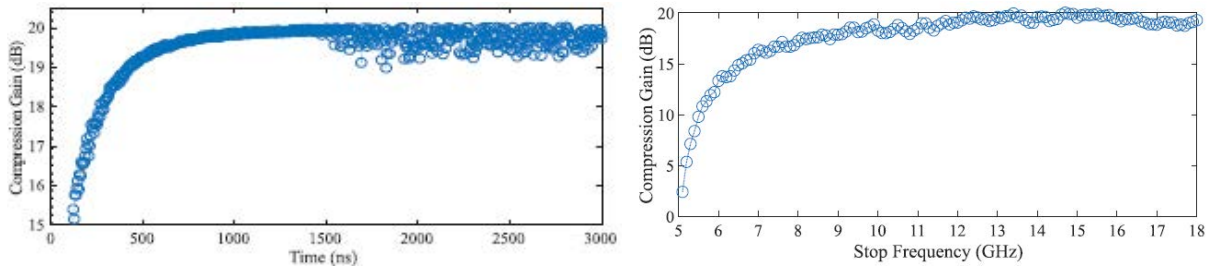
(a) (b)

Figure 7.3.3. (a) OBTR PC vs. TR PC outputs in time domain and (b) OBTR PC output in frequency domain [2]

According to the results presented in [2], TR PC preserves signal fidelity in the frequency domain but suffers from loss, and OBTR PC shows some gain in frequency domain but suffers from non-linearity. Loss is expected from such a PC system as the resonant cavity is a passive and dispersive circuit element. The TR process alone corrects the phase errors as explained in [2] and [3], resulting in signal fidelity. The OBTR process adds gain to TR PC due to digitization; however, digitization also introduces phase errors, which translate into additional frequency components. If used at the output of a GaN source, TR PC will attenuate the GaN output but somehow observe its linearity whereas OBTR PC will provide a gain of 3x at some frequencies but will completely distort the output signal.

Another consideration with OBTR or TR PC methods is the effect of impulse response record time on system gain. Figure 7.3.4 (a) shows that an impulse response record length of 1000 ns or more is required to obtain 20 dB gain for an input impulse with 5–18 GHz bandwidth (BW) [3]. Decreasing the impulse response measurement duration lowers the gain, with 15 dB achieved for IR record time of 10 ns. This effectively limits the achievable pulse repetition frequency (PRF) for a given TR PC system. For this system with IR record length of ≥1000 ns, PRF is limited to 1 MHz.

Another experiment with the same OBTR PC system, depicted in Figure 7.3.4 (b), indicates extremely low compression gain for narrowband signals with TR PC. For this experiment, an IR record length of 1000 ns is used and the input impulse bandwidth is varied by keeping the start frequency at 5 GHz and increasing the stop frequency. For the stop frequency of 5.1 GHz, i.e., BW = 0.1 GHz, a compression gain of only 2–3 dB is obtained. The results indicate that TR PC is not suitable for narrowband signals, such as in the case of GaN source output.



(a) (b)

Figure 7.3.4. Effect of IR record time on OBTR PC process: (a) compression gain vs. IR record time for a 5–16 GHz signal and (b) compression gain vs. input bandwidth, with start frequency = 5 GHz and stop frequency varying between 5.1 and 18 GHz for 1 μs IR record time [3]

7.3.5 *Summary of Significant Findings and Mission Impact*

(A) Initially a basic 2-stage magnetic pulse compression circuit was built and tested with DC input to better understand the MPC principles and considerations such as inductor sizing, pre-pulse currents and inductor saturation. Next, saturable inductor modeling was realized in LTSpice with inductor flux expression and Chan model [2]. Prior to MPC system simulations, magnetic core losses were investigated, and core selection constraints were determined based on the core losses and high-frequency MPC design considerations. Next, different magnetic core materials were investigated to determine the most suitable candidate for high-frequency MPC. As reported previously, such a core should have high resistance, narrow hysteresis loop, minimized eddy current area, and low saturation flux density (B_{sat}). High permeability (μ) and very sharp saturation characteristics are also preferred in order to minimize pre-pulse currents and resulting MPC gain loss. NiZn ferrites are the best option among the commercially available magnetic cores for the high-frequency MPC application as they have the highest operating frequency, low B_{sat}, and sufficiently high μ. After investigating suitable magnetic cores and their properties, LTSpice simulations of the previously tested 2 stage MPC circuit were resumed using the Chan model for Kemet NiZn cores. The inductor for the input stage was replaced with a magnetic switch based on the simulation results. The effects of core coercivity and remanence on MPC operation, which is not included in the design equations, were simulated, and high remanence and low coercivity were found to result in the lowest leakage currents due to sharper saturation behavior. A prototype B-H curve tracer was also built in order to characterize the magnetic cores that will be used in the MPC circuit. The prototype is now complete with the high voltage section isolated in an enclosure. Measurement of known cores with the B-H curve tracer and analysis of the results are ongoing in order to verify the accuracy of the prototype. A SoW has been drafted with KRI for the design and fabrication of a NiZn-YIG magnetic composite with cutoff frequency of over 500 MHz and relative permeability of 25. Commercial magnetic cores offer the highest cutoff frequency of 350 MHz with

relative permeability of only 7.5. New magnetic material development is needed to realize a magnetic switch at higher frequencies. A prototype MPC circuit with continuous-wave input at low frequencies will be fabricated for proof of concept before finalizing the KRI SoW.

(B) Time reversal pulse compression (TR PC) is investigated as an alternative PC-based signal amplification method. TR PC shows a few dBs of gain in the time domain but loss in the frequency domain as its main component, the resonant cavity, is a passive and lossy circuit element. One-bit time reversal (OBTR) PC, which increases the time domain gain to ≥20 dB, shows ~3x gain in the frequency domain at some frequencies but completely distorts the output signal due to the digitization process. The impulse response record time significantly affects the compression gain and limits the pulse repetition frequency. The compression gain also drops significantly for narrowband signals. Time reversal based pulse compression methods are therefore found to be incompatible with a GaN source, especially due to their limited PRF and low compression gain for narrowband signals.

7.3.6 *References*

[1] D. Zhang, Y. Zhou, J. Wang and P. Yan, "A compact, high repetition-rate, nanosecond pulse generator based on magnetic pulse compression system," in IEEE Transactions on Dielectrics and Electrical Insulation, vol. 18, no. 4, pp. 1151-1157, August 2011, doi: 10.1109/TDEI.2011.5976109.

[2] S.K. Hong, E. Lathrop, V.M. Mendez, and J. Kim, “Ultrashort microwave pulse generation by passive pulse compression in a compact reverberant cavity”, in Progress in Electromagnetics Research, vol. 153, pp. 113-121, 2015

[3] Z.B. Drikas, B.D. Addissie, V.M. Mendez, and S. Raman, “A compact, high-gain, high-power, ultrawideband microwave pulse compressor using time reversal techniques”, in IEEE Transactions on Microwave Theory and Techniques, vol. 68, no. 8, August 2020.

8 Antenna Development

8.1 Tradespace Analysis of an Array of Electrically Small Antennas (ESAs)

(Bidisha Barman and Deb Chatterjee)

8.1.1 *Problem Statement, Approach, and Context*

Primary Problem: Determine the extent to which the physical aperture size of an antenna array, composed of patch elements, can be reduced, while maintaining performance in peak power density, bandwidth, and electronic beam steerability over the UHF range (0.4–1 GHz), compared with present-art high-power-microwave-capable antenna arrays.

Solution Space: An array of patch antenna elements whose feed, two-dimensional shape, and relative placement (i.e., intra-, and inter-element design) allow for the physical aperture size to be reduced by more than 20% compared with the present-art.

Sub-Problem: To overcome scan blindness (as the main beam is electronically steered), due to the excitation of surface waves (SW). (Note: scan blindness is a common phenomenon in electrically small microstrip patch antenna arrays).

State-of-the-Art (SOTA): Horn, reflector, Vivaldi, valentine, etc. are some of the commonly used ultra-wideband (UWB) antenna elements in a phased array for high-power microwave (HPM) transmissions.

Deficiency in SOTA: Large physical aperture size of the antennas.

Solution Proposed: Using electrically small antennas (ESAs) as array elements and optimizing their performance in terms of both near-field (bandwidth) and far-field (directivity) parameters, followed by arrangement of the ESAs in suitable lattice structures (preferably, hexagonal/triangular) to reduce the overall array aperture area. Using stochastic and machine learning (ML) algorithms to optimize antenna element and array performance.

Relevance to OSPRES Grant Objective: Provides design and optimization guidelines for UWB ESA elements, especially coaxial probe-fed microstrip patch antennas, and arrays for HPM applications.

8.1.2 *Tasks and Milestones / Timeline / Status*

(A) Develop an Array Pattern Tool in the context of lightweight calculations of large antenna arrays / JAN–MAY 2021 / Completed MATLAB code.

(B) Investigate the effects of array aperture area reduction on different array parameters (such as gain, beamwidth, electronic beam steerability) and present a comparative study of antenna array parameters as a function of array aperture area / JAN–MAY 2021 / Completed.

(C) Build minimum viable validation prototypes of single ESA elements on substrates that have good power handling capabilities for HPM transmissions at UHF range (such as polyethylene, FR-4, TMM-10i, TMM-6) / JAN 2021–JUN 2022 / Completed

manufacturing of the tapered coaxial-connector fed, UWB, microstrip antenna element (0.7-1.2 GHz).

(D) Optimization of ESA (single element) performance using ML based stochastic search algorithms / JUN 2021–FEB 2022 / Completed single objective optimization of ESA elements.

(E) Build minimum viable validation prototypes for arrays of ESA elements / JUN 2021–SEP 2022 / Initiated modeling of the final demonstrable 4×4 array prototype and the associated feed-network.

(F) Optimization of array performance using ML algorithms / SEP 2021–FEB 2022 / Completed single objective optimization of antenna arrays on infinite ground planes.

8.1.3 *Progress Made Since Last Report*

(C) Build minimum viable validation prototypes of single ESA elements:

a. Completed prototyping of the tapered, coaxial-connector-fed wideband, microstrip patch antenna, for operation in the 0.7–1.2 GHz range.

b. S_{11}-parameter of the antenna has been tested.

c. Measured data comports with the simulated result, even in the presence of significant EM discontinuities within the structure.

8.1.4 *Technical Results*

(C) Build minimum viable validation prototypes of single ESA elements:

Manufacturing of the tapered, coaxial-connector-fed, wideband (0.7–1.2 GHz), microstrip patch antenna element has been completed. Prototyping of this relatively new design took longer than the expected lead time of 2 weeks due to several challenges encountered during the process. Some of the challenges include but are not limited to: (a) difficulties to CNC lathe the inner conductor of the tapered coax and (b) limitation in the printing capacity of the SLA printer, etc.

Fig. 8.1.1 and 8.1.2 show the simulated design and the manufactured prototype, respectively. The S_{11}-parameter of the antenna is measured using a Keysight FieldFox VNA. The measurement setup and a comparison between the simulated and measured S_{11}-parameters are shown in Fig. 8.1.3. It must be noted here that due to the limited capacity of the SLA printer, the substrate and tapered connector sections could not be printed as a single block. They were manufactured in parts and connected using UV-cured PMMA glue/cement leading to electromagnetic discontinuities. Further discontinuities were introduced on press-fitting an N-type connector to the narrower end of the taper. Even with these discontinuities, the simulated and measured data showed reasonably good agreement (as illustrated in Fig. 8.1.3(b)). Hence, we have shown the proposed wideband, small, microstrip patch antenna element design technique is applicable at operating frequencies in the UHF (MHz) to microwave (GHz) range.

As a next step, it has been decided to manufacture a second iteration of the prototype. In this iteration, a newly acquired, larger, SLA printer will be employed to print the substrate

and the tapered connector as a single block. This is expected to *eliminate* the discontinuities between the substrate panel and the connector encountered in the first iteration. In addition, reduced lead time is expected.

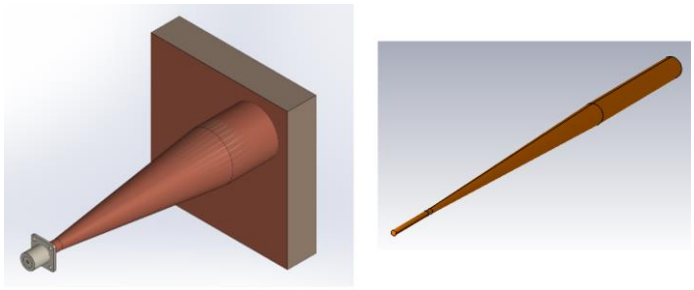


Figure 8.1.1. CST simulation model of the (a) wideband, microstrip patch antenna, fed by the tapered coaxial connector, on a PEC-backed, square shaped ($6" \times 6"$), polyethylene substrate, and (b) inner conductor of the tapered coaxial connector.

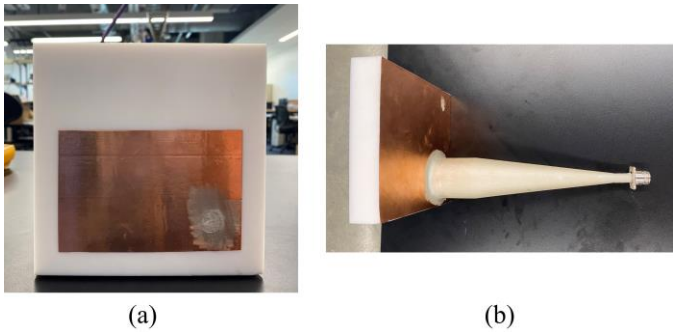


Figure 8.1.2. (a) Front and (b) side view of the microstrip patch antenna, fed by a tapered coaxial connector, for operation in the UHF (0.7–1.2 GHz) range.

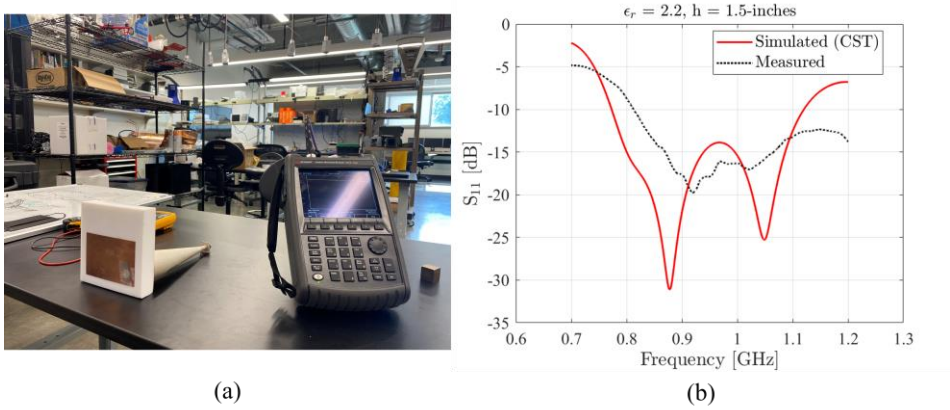


Figure 8.1.3. (a) Measurement setup. (b) Comparison between the measured and simulated S_{11}-parameter of the prototype.

8.1.5 *Summary of Significant Findings and Mission Impact*

(A) Developing Array Pattern Tool for large arrays calculations:

A MATLAB code has been developed for faster radiation pattern approximation of a linear/planar array of any size and composed of any type of antenna elements. The code requires the center element pattern of a small array (say, 3×3) composed of the same type of antenna elements, desired lattice arrangement, and total number of array elements, as user inputs. The usage of this code will be included in future publications.

(B) Investigate the effects of array aperture area reduction on different array parameters:

The effects of different aperture shape and lattice arrangements on array gain and beam steerability have been studied for arrays modeled on PEC-backed substrates. Investigations show that a transformation from square-grid-rectangular-aperture to triangular-grid-hexagonal-aperture leads to $\approx 30\%$ reduction in aperture area ($\approx 50\%$ reduction in number of array elements) with a tradeoff of ≈ 1.5 dBi (in 2.5–5 GHz) and ≈ 3.5 dBi (640–990 MHz range) gain reduction. The aperture area reduction, however, comes at the cost of limited beam steerability to $\pm 45°$ from boresight, compared to the $\pm 60°$ scanning capabilities achieved from the square-grid-rectangular-aperture arrays, at all frequency ranges.

(C) Build minimum viable validation prototypes of single ESA elements:

Developed a design technique for electrically small microstrip patch antenna that provides $\geq 30\%$ impedance bandwidth by strategic placement of the feed-probe along the patch diagonal, at operating frequencies in the UHF (MHz) to microwave (GHz) frequencies. The method avoids any sophisticated prototyping and is a transformative approach in the design of electrically small microstrip antennas for ultrawideband wireless applications. The design approach was validated via prototypes manufactured on TMM-6 and TMM-10i substrates, in the 2.5–5 GHz range. In addition, a prototype has been built for operation in the UHF range (0.7–1.2 GHz). Despite a few manufacturing defects, the preliminary test results showed reasonable agreement with the simulated values. An updated version of the prototype is currently being manufactured for improved performance.

(D) Optimization of ESA (single element) performance using regular, and ML based stochastic search algorithms:

Optimization of feed-probe location, ground plane shape and size in a microstrip patch antenna, with the objective of bandwidth enhancement, using ML based stochastic search algorithms (GA, PSO, and Simplex methods), was performed. ML algorithms were found to be ≈ 2 times faster and ≈ 0.3 times less memory intensive compared to regular search algorithms, while maintaining same degree of accuracy.

It is concluded that, although these automated ML algorithms do not provide insight into the underlying physics of the problems and require human intervention at every stage for better decision making, they can still be considered as potential tools for faster optimization of antenna performance, especially for multi-objective optimization of complex structures, which are computationally intensive using conventional EM solvers.

(E) Build minimum viable validation prototypes for arrays of ESA elements:

A 3×3 array of wideband elements (2.5–5 GHz) and a 2×2 array of narrowband elements (900 MHz), on TMM-10i substrates, were manufactured and tested. Having achieved reasonably good agreement between simulated and measured S_{11} and gain responses from individual array elements, it was decided to implement the design method for building the final demonstrable prototypes. Currently, a 4×4 square-grid-rectangular-aperture and a 10-element triangular-grid-hexagonal-aperture array of wideband, microstrip, ESA elements, in the UHF range (0.6-1 GHz), are being characterized for prototyping.

(F) Optimization of array performance using ML algorithms:

Completed inter-element spacing optimization in a 4×4 square-grid array, on an infinitely large, PEC-backed, dielectric substrate, using ML based genetic algorithm, in the 2.5–5 GHz range, with the objective of array boresight gain enhancement. Multi-objective optimization (simultaneous enhancement in boresight gain and impedance bandwidth) of a 4×4 square-grid array on a finite, PEC-backed, substrate, by seeking the best array design parameters, including inter-element spacing, ground plane size, and feed-probe locations, in the desired UHF range (0.6–1 GHz), is pursued presently.

8.2 Tradespace Analysis of Ultra-Wide-Band (UWB) Koshelev Antenna

(Alex Dowell and Kalyan Durbhakula)

8.2.1 *Problem Statement, Approach, and Context*

Primary Problem: Determine the extent to which the physical aperture area of an antenna array, composed of antenna elements, can be reduced, while maintaining performance in peak power density, bandwidth, and electronic beam steerability over the UHF range (0.4–1 GHz), compared with present-art high-power-microwave-capable antenna arrays.

Solution Space: The Koshelev antenna has a unique design that is capable of generating an UWB response by effectively merging radiation characteristics from a transverse electromagnetic (TEM) horn antenna with exponentially tapered flares, an electric monopole, and magnetic dipoles over a wide frequency range [1]. This opens up an opportunity to investigate the design parameter space and understand parameter effects on impedance bandwidth, radiation pattern, electric field distribution, and other metrics via a tradespace study.

Sub-Problem:

(i) The integration of an impedance transformer to a single element Koshelev antenna to simulate and test the combined (transformer–antenna) performance is currently not feasible using commercial EM simulators.

(ii)The total surface currents on the Koshelev antenna over the desired frequency range arising from the present positioning of TEM exponential flares, an electric monopole, and magnetic dipoles is not yet clearly understood.

State-of-the-Art (SOTA): The balanced antipodal Vivaldi antenna (BAVA) is considered to be the SOTA antenna element due to its exceptional 20:1 impedance bandwidth ratio as well as the ability to handle tens-of-MW input power.

Deficiency in the SOTA: The BAVA design parameter space has been exhausted over the past couple of decades. The physical aperture area still remains very large and there is no viable path through tradespace study for further physical aperture area reduction.

Solution Proposed: Design, simulate, validate, and perform a tradespace study on the important design parameters of the Koshelev antenna array that effectively reduce its physical aperture area while maintaining its UWB properties, in both the frequency and time domains. The Koshelev antenna has been shown in the literature to withstand higher voltage levels (over 200 kV peak voltage), thereby making it a viable antenna element for detailed tradespace study and analysis.

Relevance to OSPRES Grant Objective: From the literature, it was shown that the Koshelev antenna can handle high input voltages (and therefore high power with 50 Ω input impedance), which satisfies the specific OSPRES objective related to high input voltage/power. In addition, this work can yield a center-frequency-dependent, bandwidth-controlled, and electronically steerable Koshelev antenna design that can be quickly modified to the spectrum properties of the ultra-fast rise time input pulse.

Risks, Payoffs, Challenges:

(i) The electrical size of the Koshelev antenna is approximately λ/4 at its lowest operating frequency. Further reduction of electrical size to λ/10 could considerably reduce frequency dependent gain, thereby decreasing the power spectral density.

(ii) Payoffs include the development of a library of antenna metrics data for different shapes and sizes of the individual parts within the Koshelev antenna.

(iii) The large electrical size (>5λ) of the Koshelev antenna at its highest operating frequency poses huge computational challenges.

8.2.2 *Tasks and Milestones / Timeline / Status*

(A) Complete literature search to identify and list antenna elements that satisfy UWB properties and HPM requirements, and down-select accordingly / NOV–DEC20 / Complete.

(B) Complete initial design, simulation, and validation of Koshelev antenna [1] / JAN21 / Complete.

(C) Perform a preliminary parameter study to identify design parameters that considerably reduce the physical aperture area / FEB–MAR21 / Complete.

- Milestone: Using FEKO and/or CST electromagnetic (EM) simulators, reduce the physical aperture size of the Koshelev antenna to at least 95% of its original design and show minimal to no variation in the bandwidth, gain and increased aperture efficiency / Complete.

(D) Determine the full-width half-maximum (FWHM) and ringing metrics from the envelope of the time domain impulse response ($h_{rx/tx}(t, \phi, \theta)$) in receive or transmit mode / MAR–APR21 / Complete.

- Milestone: Produce a generalized code that calculates the impulse response envelope of the Koshelev antenna and plots the rate of change in FWHM and ringing values as a function of physical aperture size.

(E) Perform tradespace studies on design parameters such as feed position (*F*), length (*L*), and alpha (α). Obtain various antenna metrics data, compare, and analyze / MAR21/ Complete.

- Milestone: Identify Koshelev antenna design parameters that significantly alter the bandwidth, rE/V, peak gain over the desired bandwidth, and aperture efficiency.

(F) Reduce Koshelev antenna aperture size (H×W) to equal to or less than 90 mm × 90 mm, equal to that of the SOTA BAVA, for direct antenna metrics comparison / MAR–APR21 / Complete.

- Milestone: Provide a recommendation on the optimum design parameters and the resulting metrics, with comparison to SOTA BAVA. The optimized design parameters must yield 900 MHz ± 200 MHz bandwidth, rE/V greater than 1, peak gain around 3 dBi at 900 MHz, aperture efficiency equal to or greater than 130% at 900 MHz.

(G) Using the optimized model from (F), build various array simulation models/topologies to perform a tradespace study and report tradeoffs between array antenna metrics such as center element reflection coefficient (S11) value, gain vs theta at constant phi, physical aperture area, aperture efficiency, and rE/V / MAY–JULY21 / Complete.

- Milestone: Develop/showcase an optimized Koshelev array model that exceeds an aperture efficiency of 130% with a high rE/V.

(H) Perform literature search to investigate, understand, and determine the applicability of special electromagnetic (EM) techniques to the antennas under consideration. / JAN–APR21 / Complete.

(I) Explore impedance taper (microstrip based and coax based) designs that can interface well (both mechanically and electrically) to transition the signal from a coax cable to the input of the Koshelev antenna element / JULY21–AUG21 / Complete.

- Milestone: Recommend the optimum impedance taper design (with minimum reflections and maximum power transfer) with the optimum dimensions to successfully convert the high-voltage, short-rise time input signal from a coax cable to the feed of the Koshelev antenna array.

(J) Study response from optimized Koshelev antenna array when excited with different monopolar, differential, and bipolar pulse signals of significant interest / AUG21–NOV21 / Ongoing.

- Milestone: Provide a table comparing the Koshelev antenna array response metrics and narrow down the suitable pulse signals. Recommend (if any) changes to the

downselected pulse signal(s) that can further improve the radiation efficiency, and/or transient gain.

(K) Investigate and analyze the response from the optimized Koshelev antenna array when excited by different excitation patterns / DEC 21 / Complete.

- Milestone: Compare and recommend an appropriate excitation method to yield maximum boresight gain, maximum half-power beamwidth (HPWB), minimum side lobe levels, and maximum electric field, rE/V.

(L) Prototype single element Koshelev antenna and test for reflection coefficient, gain as a function of frequency, radiated electric field at 1-m, 2.5-m, 5-m and 10-m (if feasible) distances. / AUG21–SEP22 / Ongoing.

(L1) Fabricate Cu-foil and paint (silver or copper) variants of 3D-printed balanced Koshelev antenna with integrated impedance transformer.

- Milestone: Demonstrate a 3D printed Koshelev antenna prototype that is cost-effective and lightweight. / AUG21–NOV21 / Complete.

(L2) Perform scattering parameter measurements of Cu-foil and paint variants of 3D-printed prototypes to identify any design and fabrication issues/challenges.

- Milestone: Report fabrication & assembly challenges, test outcomes and identify the source of mismatch (if any) to alleviate reflections. Verify against simulations to validate mismatches. / DEC21–APR22 / Ongoing.

(L3) Downselect to one variant of the 3D printed Koshelev antenna prototype and measure frequency domain gain and time-domain electric field at multiple distances.

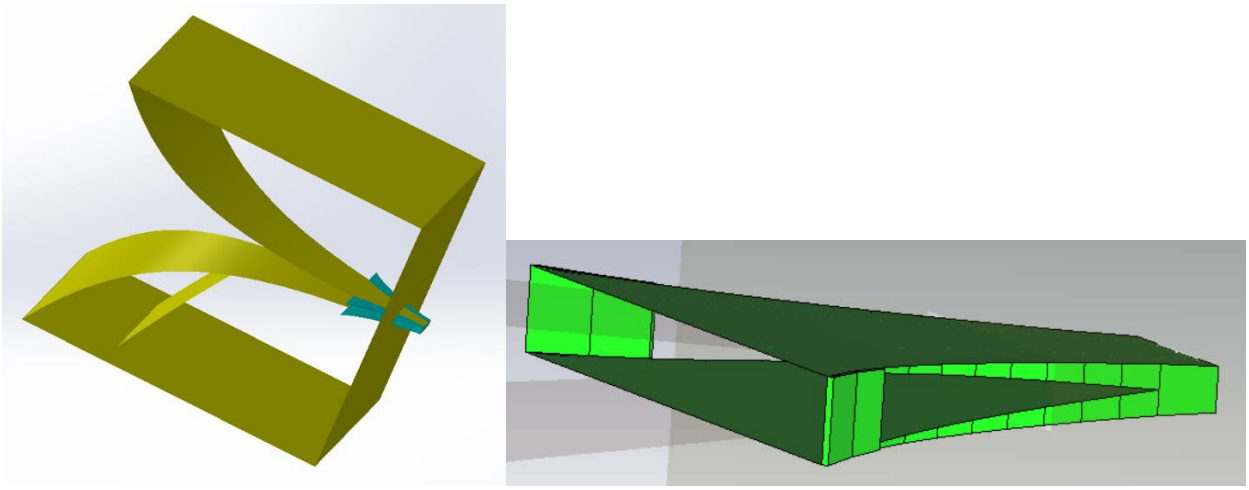
- Milestone: Experimentally demonstrate a 3D-printed Koshelev antenna with a performance comparable to the standard sheet metal variant of the Koshelev antenna. / MAY22–SEP22.

- Milestone: Report performance of 3D printed Koshelev antenna, compare against the performance of balanced antipodal Vivaldi antenna (BAVA), and recommend any overall improvements to the fabrication/prototyping/testing methods.

8.2.3 *Progress Made Since Last Report*

(L2) In the previous report, a gradient dielectric impedance transformer and a mirrored version were modeled and simulated to identify radiofrequency (RF) performance. After analyzing the S_{11} parameter, it was determined that the new transformer computer aided design (CAD) model should be simulated with the Koshelev antenna CAD model to determine viability before prototyping.

8.2.4 *Technical Results*



(a) (b)

Fig. 8.2.1. CAD models of (a) a gradient dielectric impedance transformer integrated with a CAD model of a Koshelev antenna (b) a gradient dielectric impedance transformer with structural support

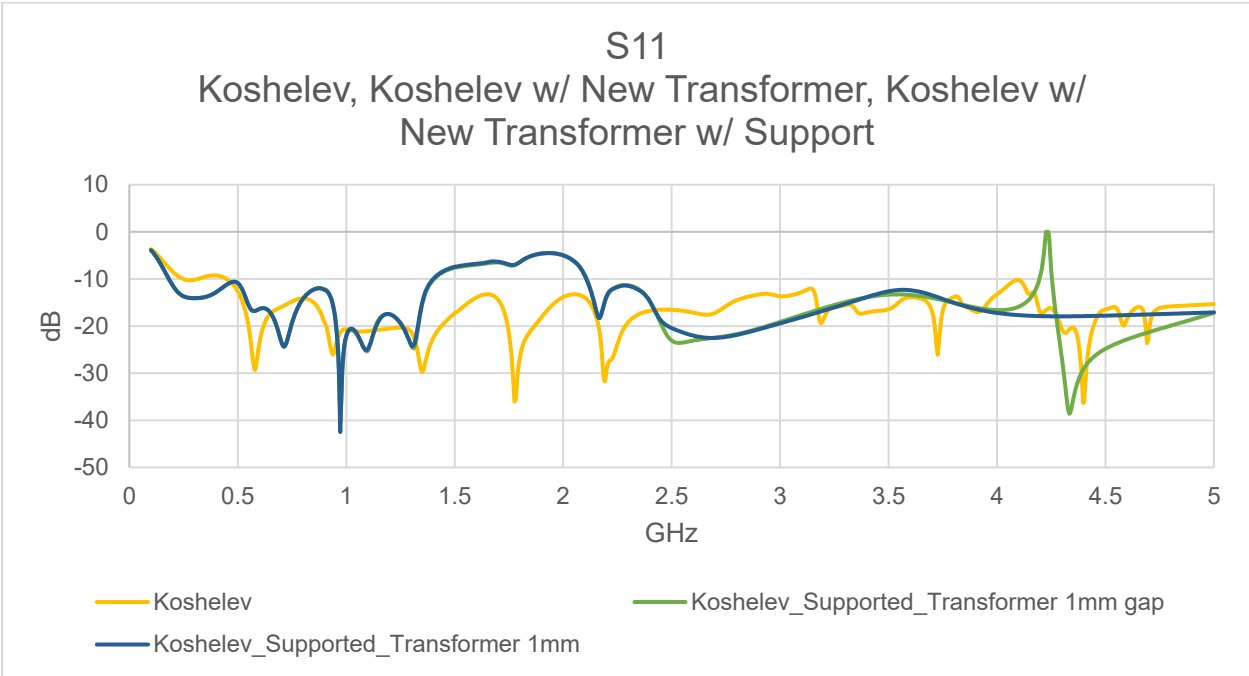
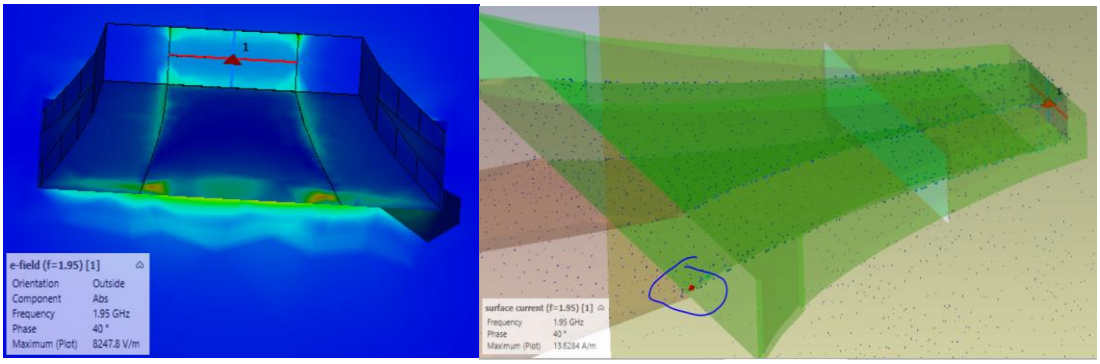


Fig. 8.2.2. Comparing S_{11} of a Koshelev antenna integrated with a PLA Koshelev gradient dielectric impedance transformer with and without structural support collected from CST Studio Suite and comparing it to the S_{11} of the standalone Koshelev antenna

(L2) After modeling the new graded transformer with and without support and integrating it with the Koshelev antenna, shown in Fig. 8.2.1(a) and Fig. 8.2.1(b), S_{11} results from CST Studio Suite were compared to the standalone Koshelev antenna. Fig. 8.2.2. shows a degraded performance for Koshelev-transformer models with and without support

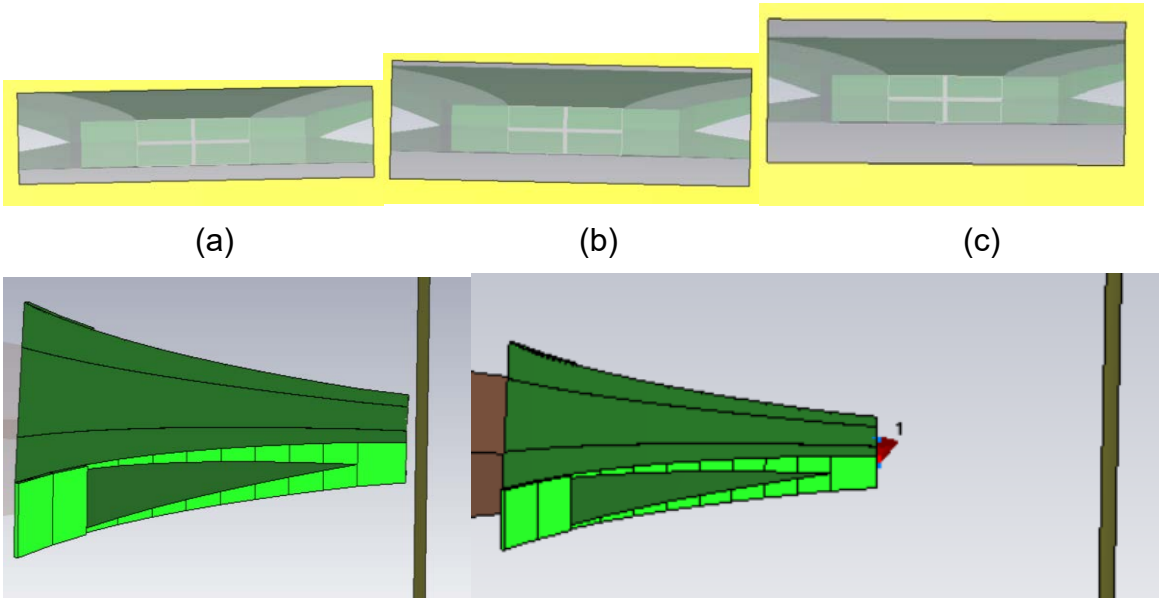
between 1 and 2.5 GHz. Although the added structural support did negatively effect performance, the only degradation is at 4.2 GHz. Since this is outside the frequency range of interest, this is not of concern.



(a) (b)

Fig. 8.2.3. (a) E-field and (b) surface current plots of the initial Koshelev-Transformer configuration collected from CST Studio Suite, where the transformer and the Koshelev backplate meet.

The Koshelev-Transformer simulation was then rerun with the added monitors of E-field and surface currents, shown above in Fig. 8.2.3 (a) and Fig. 8.2.3 (b), for the poor performing range between 1 GHz and 2.5 GHz. The surface current plot shows a small concentration where the transformer traces connect to the antenna, but no concerning reflections were seen. After analyzing the E-field plots, coupling between the transformer and the Koshelev backplate was identified.



(a) (b) (c)

(d) (e)

Fig. 8.2.3. The geometric changes of the Koshelev-Transformer configuration for an optimization case study. The geometric changes consist of: (a) 3 mm gap height, (b) 5 mm gap

height, (c) 7 mm gap height, (d) translating the Koshelev backplate 3 mm behind the transformer, (e) translating the Koshelev backplate 50 mm behind the transformer

From here a case study was conducted where geometric changes, shown in Fig. 8.2.3 (a) – (e), were varied and simulated to reduce the coupling between the transformer and the Koshelev backplate and improve performance.

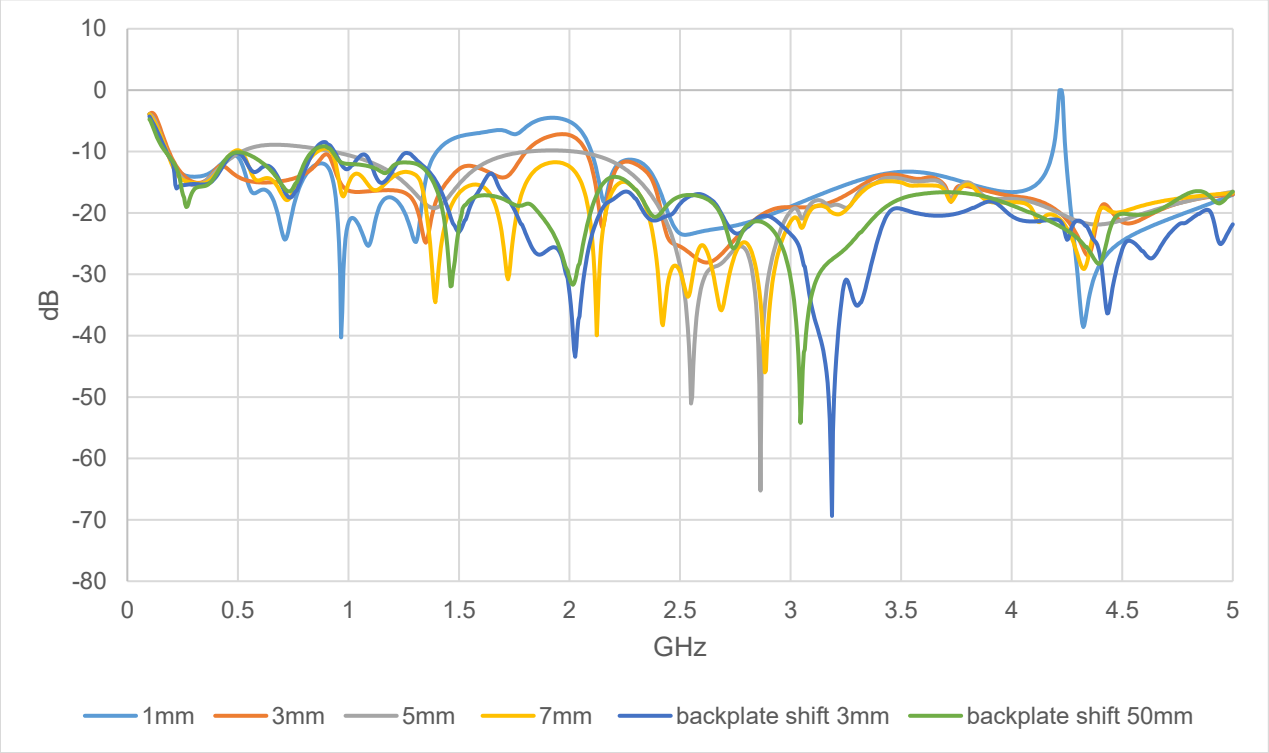


Fig. 8.2.4. Comparing S_{11} of a Koshelev antenna integrated with a PLA Koshelev gradient dielectric impedance transformer with structural support for each geometric variation collected from CST Studio Suite

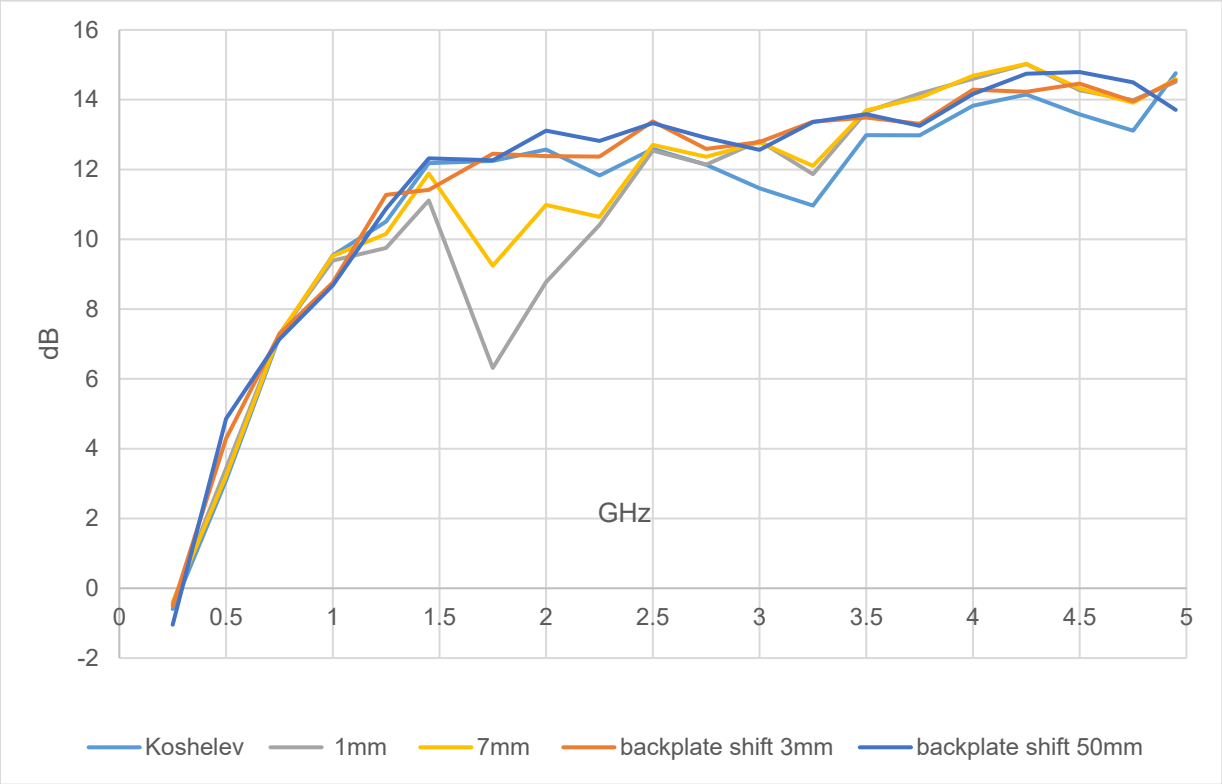


Fig. 8.2.5. Comparing max gains of a Koshelev antenna integrated with a PLA Koshelev gradient dielectric impedance transformer with structural support for each geometric variation collected from CST Studio Suite

Fig. 8.2.4. and Fig 8.2.5 show that increasing the gap sizes produced increased performance between 1 GHz and 2.5 GHz. The 7 mm gap variation performed the best of the gap variations. In Fig. 8.2.4. and Fig 8.2.5 the backplate shift variations also showed an increase in performance but also would increase the antenna's overall footprint.

8.2.5 *Summary of Significant Findings and Mission Impact*

(A) An extensive literature search on various UWB antenna elements has resulted in finding three promising options. The down-selected elements are the Koshelev, Shark, and Fractal antennas, which will be extensively studied using their individual design parameter space, which could result in physical aperture area reduction of the single antenna element. Later, the single antenna element will be converted into a planar array.

(B) Initial validation of the Koshelev antenna simulated using CST software agreed well with the antenna metrics published in the open literature [1]. A UWB bandwidth response (10:1 bandwidth) and rE/V > 1 has been observed from our initial simulations of the Koshelev antenna. This validation ensured that the Koshelev antenna can be subjected to further tradespace studies to understand its performance followed by optimizing the design according to OSPRES grant requirements.

(C) The initial tradespace study and analysis of the Koshelev antenna design yielded promising outputs to carry forward the investigation. A comparison of important antenna metrics between the Koshelev antenna in [1] and aperture reduced Koshelev antenna are shown in Table 5.2.1 of the APR 21 MSR.

(D) An in-house code has been developed to calculate important UWB time domain antenna metrics such as full-width half maximum (FWHM) and ringing. These metrics have been calculated using in-house MATLAB code using the excitation voltage and radiated electric field information obtained from CST simulations. FWHM and ringing antenna metrics help with assessing or characterizing an antenna's UWB response.

(E) The tradespace study of feed position provided a deeper understanding of how its position impacts the S11 value bandwidth. An optimum value for feed position i.e., $F = 1/20 < L < 1/10$ is recommended to achieve maximum bandwidth. The tradespace study of the antenna length (L) is straightforward. A longer antenna length will radiate better at lower frequencies. However, physical size restrictions/requirements must be kept in mind in determining the antenna length. Finally, a larger α value (>120°) is recommended to avoid unnecessary reflections from the electric monopole.

(F) From a thorough tradespace study, the aperture size of the Koshelev antenna (single element) is determined to be 90 mm × 100 mm in order to achieve desired antenna metrics performance proposed in the milestone. All metrics described in the milestone have been successfully achieved except the desired bandwidth (200 MHz on both sides) at 900 MHz center frequency. The bandwidth achieved is 900 ± 100 MHz.

(G) The physical aperture area of the Koshelev array antenna largely depends on the interelement spacing and the shape of the array. We were able to determine that the diamond topology is the optimum shape for the Koshelev array antenna. We were also able to obtain similar gain profile (peak gain and pattern) from making certain elements within the array passive (off state) when compared against regular active array (all elements in on state). From the non-symmetric interelement spacing values, we found that S_y has the least effect on the output; therefore a small spacing value can be chosen to reduce the physical aperture area of the Koshelev array.

(H) The literature search on the special EM techniques expanded our knowledge and opened the door to opportunities to apply some of those techniques to the antennas under study. EM techniques such as non-symmetric and non-square array topologies have been applied to the development and study of the Koshelev array antenna.

(I) The first impedance taper design under consideration has shown good S11 values (< –10 dB) over the frequency range of interest. In addition, we have shown that the shape of the pulse can be easily retained at the output of the taper with less than 5% amplitude losses.

(J) The Koshelev antenna array response from feeding a monopolar vs bipolar signal has demonstrated a clear winner: that is, a bipolar signal will radiate at least 10 times better than a monopolar signal. A comparison of the frequency spectrum of the radiated electric field from the optimized Koshelev antenna array between different monopolar pulse sources has identified the 'MI0731' pulse to be the optimum pulse.

(K) The optimized Koshelev antenna array was studied for the electric field response under different array excitation patterns. The study determined that the uniform and Gaussian excitation patterns were the optimum excitation patterns. Selecting the uniform or Gaussian excitation pattern would yield the maximum electric field at the boresight for an arbitrary input signal.

(L) Two variants (Cu-foil plated and silver painted) of the 3D-printed Koshelev antenna have been fabricated to demonstrate a working antenna prototype. The measured S_{11} result of the Cu-foil plated variant showed poor performance due to issues at the transformer–antenna interface. The traditional transformer contributed to field discontinuity at the interface. To alleviate this issue, we have designed and simulated a gradient dielectric transformer, which showed improved performance over traditional transformer. A slot was made on the backplate to facilitate the new transformer which introduced new coupling issues. The size of the slot was studied and optimized to obtain satisfactory results compared to original no transformer Koshelev antenna results.

8.2.6 *References*

[1] Gubanov, V. P., et al. "Sources of high-power ultrawideband radiation pulses with a single antenna and a multielement array." *Instruments and Experimental Techniques* 48.3 (2005): 312-320.

[2] S. Zhang, Y. Vardaxoglou, W. Whittow and R. Mittra, "3D-printed graded index lens for RF applications," 2016 International Symposium on Antennas and Propagation (ISAP), 2016, pp. 90-91.

8.3 Machine Learning Inspired Tradespace Analysis of UWB Antenna Arrays

(Sai Indharapu and Kalyan Durbhakula)

8.3.1 *Problem Statement, Approach, and Context*

Primary Problem: Determine the extent to which the physical aperture area of an antenna array, composed of antenna elements, can be reduced while maintaining performance in peak power density, bandwidth, and electronic beam steerability over the UHF range (0.4–1 GHz), compared with present-art high-power-microwave-capable antenna arrays.

Solution Space: Fractal antennas possess exceptional fidelity factor values (>0.9), which describe how well the shape of the input pulse is retained at an observation point in the far-field. Their high degree of freedom provides an opportunity to develop systematically modified patch shapes, which in turn leads to improved bandwidth while retaining high fidelity factor values. Machine learning (ML) can be leveraged to predict the antenna array response for an arbitrary design parameter space upon sufficient training and validation.

Sub-Problem:

(i) Fractal antennas generate omni-directional radiation patterns in the H-plane over the desired frequency range.

(ii) ML can suffer from underfitting or overfitting the training model which in turn leads to deviations in the predicted output.

State-of-the-Art (SOTA): Conventional full-wave EM solvers such as method of moments (MoM), multi-level fast multipole method (MLFMM), finite element method (FEM), and finite difference time domain (FDTD) method are currently being used to study, analyze and assess the performance of UWB antennas.

Deficiency in the SOTA: UWB antenna optimization using conventional EM solvers utilizes significant computational time and memory resource.

Solution Proposed:

(i) Design, simulate, validate, and perform a tradespace study on the design parameter space of the selected fractal antenna element using commercially available electromagnetic (EM) wave solvers.

(ii) Train, validate, test and compare multiple ML models for quicker and accurate prediction of antenna array response for different physical aperture areas.

Relevance to OSPRES Grant Objective: The fractal antenna achieves an UWB response, a mandatory requirement of the OSPRES grant objective, in a small volume footprint and similar physical aperture area when compared against the SOTA BAVA, dual ridge horn antennas etc. Furthermore, the microstrip-design-based fractal antenna can efficiently handle electronic steering by integrating the feed network on the same board. This eliminates the need to build a separate feed network external to the fractal antenna using bulky coaxial cables.

Risks, Payoffs, and Challenges:

(i) A majority of the fractal antenna geometries yield an omni-directional pattern in the H-plane, which can be a risk. However, efforts are underway to mitigate this pattern without deteriorating bandwidth.

(ii) Payoffs include developing a library of antenna metrics data for various fractal shapes and sizes.

(iii) Design challenges and numerical calculations with respect to specific fractal shapes could arise after performing a certain number of iterations to further improve the bandwidth.

(iv) Fractal antennas were known to generate gain loss at random frequencies over their operating frequencies. Achieving gain stability over the desired frequency range can be a significant challenge.

8.3.2 *Tasks and Milestones / Timeline / Status*

(A) Perform tradespace analysis of the fractal element radius *b* over the desired frequency range (4 to 12 GHz) using the genetic algorithm (GA) optimization tool available in the commercial electromagnetic (EM) solver FEKO / FEB21 / Complete.

- Milestone: Provide a recommendation of an optimum value of *b* using OPTFEKO to minimize reflection coefficient or S_{11} (< –10 dB).

(B) Perform tradespace study on different fractal shapes by changing the number of fractal segments to understand the effect of this change on the impedance bandwidth / FEB21 / Complete.

- Milestone: Produce a detailed study of the antenna response such as S_{11}, gain, and bandwidth by varying the number of fractal segments.

(C) Apply the GA optimization tool on the fractal side length *b* over a wide frequency range (2 to 12 GHz with 201 discrete frequency points) and number of fractal segments using OPTFEKO on the LEWIS cluster / MAR21 / Complete.

- Milestone: Reduce physical aperture area by 10% of its present design, reported in the FEB MSR, and demonstrate minimal or no change in S_{11}, gain, and fidelity factor values.

(D) Perform a parametric study and analysis of antenna response by varying hexagon radius, *a* / MAR–APR21 / Complete.

- Milestone: Recommend a value of *a* to reduce the physical aperture area and increase aperture efficiency (>50%) with no variation in other antenna metrics.

(E) Frequency scale fractal antenna design such that the center frequency of the resulting antenna equals 1.3 GHz / MAY21 / Complete.

- Milestone: Modify antenna design with a center frequency equal to 1.3 GHz and achieve similar results (3:1 bandwidth at fc = 1.3 GHz, 3 dBi gain and >130% aperture efficiency at 900 MHz) to antenna design at center frequency ~7 GHz.

(F) Design and simulate various array antenna geometries composed of optimized fractal antenna elements (obtained from (E)) to analyze the effect of overall array antenna geometry on the desired array antenna response metrics (i.e., gain vs. frequency, gain vs. elevation angle at constant phi, rE/V, half-power beamwidth and side-lobe level.) / MAY–JUL21 / Complete

- Milestone: Recommend a best possible structure with reduced aperture area and minimal loss in gain.

(G) Apply ML models available in Altair Hyperstudy (2021) on the fractal antenna to try and understand the possibilities and limitations of ML models for fast and efficient antenna metrics prediction and optimization. Expand the prediction capability to time-domain electric field and antenna pattern using ML models (k-nearest neighbor and linear regression) available in scikit learn on Python programming tool “Anaconda”. / MAY21–FEB22 / Complete.

- Milestone: Recommend most accurate and efficient ML model for a fractal antenna in time-domain and frequency domain.

(H) Apply ML models on the octagon fractal antenna array lattice to extend the prediction capability beyond single element / SEP21–MAY22 / Complete.

- Milestone: Recommend the best suitable ML model implemented/developed using Python programming language for array antenna metrics prediction.

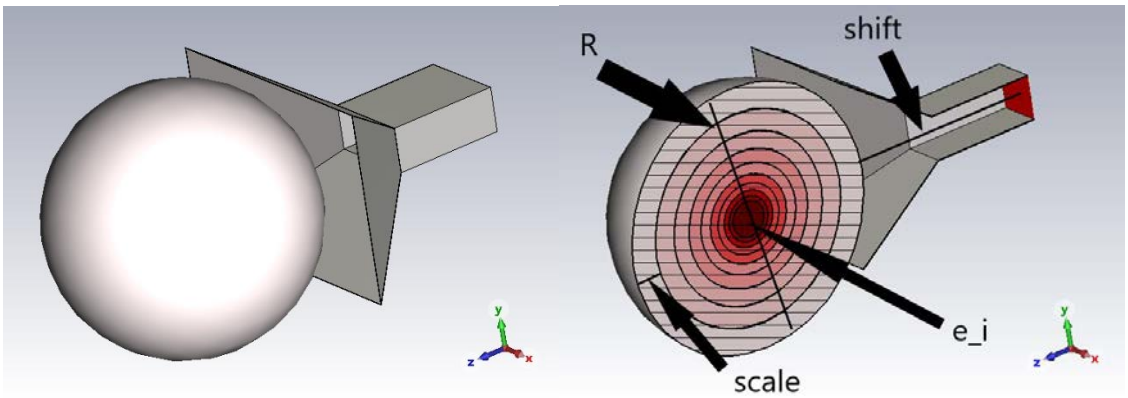
(I) Develop, validate, and demonstrate a graphical user interface (GUI) to automate the process of employing ML models to predict the antenna output response/ FEB22–SEP22 / Ongoing.

- Milestone: Incorporate the developed automated data extraction scripts, ML scripts to the GUI to enable user to predict antenna response with shorter time.

8.3.3 *Progress Made Since Last Report*

(I) Development and testing of the GUI.

- The GUI scripts are converted from *.py to *.exe file which makes the GUI a standalone application. The *.exe file generated using the *.py files can be used to open the GUI by any user on any device without any preinstalled python or scikit-learn packages.
- A traditional horn antenna with spherical gradient index refractive (GRIN) lens has been selected to test the ability of the GUI to predict the antenna response. The selected antenna design is illustrated in Fig. 8.3.1, which has multiple adjustable design variables, but only 4 design variables were selected for the analysis (i.e., shift, e_i, scale, R). The four design variables are shown in Fig. 8.3.1. In the training phase, the k-nearest neighbor (kNN) model is used to correlate the gain response to different combinations of input design variables. Once the model is trained, it is used to predict the gain response of the RF lens design for the test data.



(a) (b)

Fig 8.3.1. A traditional horn antenna with spherical gradient index refractive (GRIN) lens: (a) full model (b) cross section.

8.3.4 *Technical Results*

(I) Testing of the GUI.

<u>Gain prediction using the GUI (Test-2):</u>

The kNN model is trained using a training data set size of 31. The training data is generated using CST and consists of design variables (input) and the

corresponding gain values (output). The trained model is then used to predict the gain response for a new combination of design variables using a validation window in the GUI. The predicted output is plotted and displayed on the validation window as shown in Fig. 8.3.2.

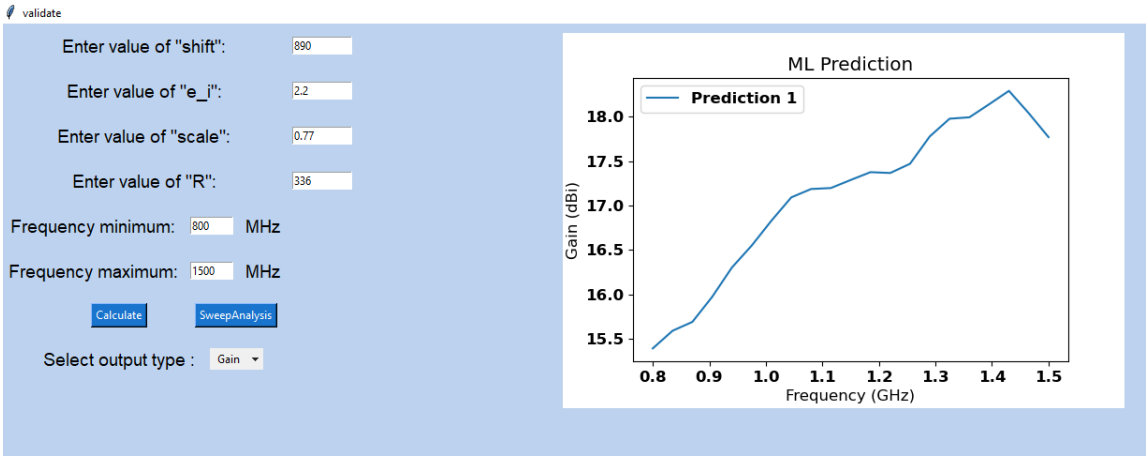


Fig. 8.3.2. Snapshot of validation window of the GUI (Gain prediction).

To validate the gain prediction from the GUI, the predicted output is compared against the CST response as shown in Fig. 8.3.3.

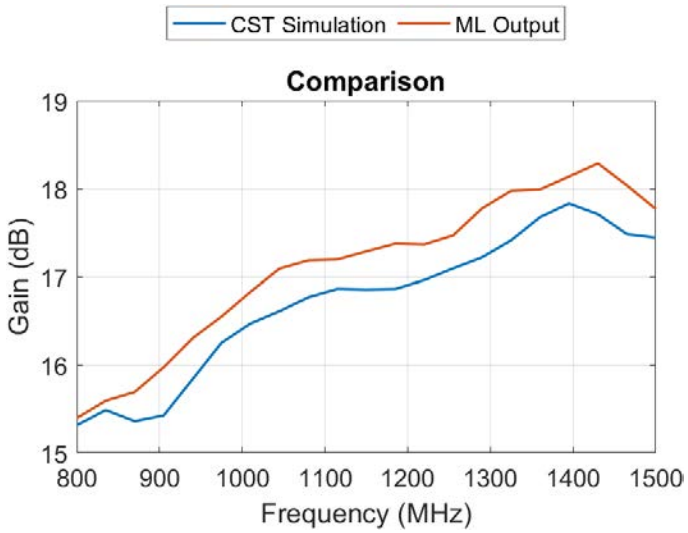


Fig. 8.3.3. Comparison of gain response from CST with GUI prediction.

From the comparison of gain response between CST and ML, the overall agreement is satisfactory. Further, to measure the error value between ML predictions using the GUI and the CST, the RMSE is calculated. The resultant root mean square error (RMSE) value is 0.42, which is acceptable as the value is lower than 1 and close to zero.

Finally, from the feedback received by users and from the overall evaluation of the GUI, below are points considered as updates/improvements that can be seen in the next version of the GUI.

Updates for the next version of the GUI:

2. X-axis and Y-axis gridlines on the plots (a checkbox to on/off the gridlines).
3. An option to export the predicted data from the GUI.
4. A real-time status monitor window that provides detailed information on the steps executed.(the messages include the details of steps completed).
5. Enabling the user to calculate the error of user's choice (drop-down button to select the desired error calculation method).
6. Enabling the user to plot the predicted response against the actual output within the validation window.
7. A "Readme" file that gives a quick introduction to the user about the available ML models on the GUI.

Apart from the updates mentioned in the points above, an additional "Auto-Design" feature will be added to the validation window. This step will provide the user with the flexibility to automate the process of generating training data, training the ML algorithm, and validating the trained model. With this feature, the user is no longer required to extract training data from the *.outfile or upload training data as excel sheets to the GUI. The "Auto-Design" feature will only require the antenna design file (*.cfx) as the input.

8.3.5 *Summary of Significant Findings and Mission Impact*

(A) We carried out an effort to identify the dominant fractal antenna design parameter and its corresponding value using parameter study and FEKO optimization tool. It was found that the side length '*b*' of the fractal elements play a significant effect on the antenna bandwidth. The initial analysis of the simulation results with fractal radius *b* equal to 1.8 mm yielded multiple resonant frequencies with enhanced bandwidth. To further increase the bandwidth, OPTFEKO was used as an optimization tool with fractal radius *b* as the optimization variable. Finally, the optimum value for *b* is found to be 1.66 mm which minimizes the S_{11} (-10 dB).

(B) The addition of fractal elements (*N*) to the simple hexagon improved antenna metrics such as reflection coefficient (S_{11}). To further investigate and understand the fractal elements, the number of segments (sides of the fractal element) in the fractal geometry were varied within the range of 6 to 14. By varying the number of segments in the fractal element, the resultant S_{11} response has positive impact at higher frequencies and negative impact at lower frequencies. Therefore, the number of segments of the fractal element were chosen to be 6 as it has better balance of S_{11} values both at lower and higher frequencies.

(C) The initial optimum value of *b* over 51 discrete frequency points is reported as 1.66 mm in task (A). To further increase the accuracy of the optimization algorithm and to find a more precise value for *b*, optimization is further performed over a wider

frequency range (201 discrete points between 2 GHz to 12 GHz) which yielded an optimum value of *b* as 1.37 mm. The S_{11} response of the antenna design with this newly obtained *b* parameter (i.e., 1.37 mm) has not produced any better bandwidth compared to *b* = 1.66 mm. Thus, *b* is set to be 1.66 mm for further research.

(D) The hexagonal patch radius *a* has a significant effect on the physical aperture area of the antenna. Therefore, Altair OPTFEKO has been utilized to find an optimum *a* value, which was determined to be 8 mm over the range 7.2 to 9 mm. Antenna metrics such as S_{11}, gain, and bandwidth have shown desired performance with the optimized *a* value.

(E) The initial antenna design has been modified to achieve a center frequency of ~1.3 GHz. The gain value at 900 MHz is 3.5 dBi and, with the modified antenna design, we were able to achieve an impedance bandwidth ratio of 3.3:1. The designed antenna has been fabricated and tested, and the S_{11} response of the fabricated antenna agrees well when compared against FEKO, CST.

(F) Four different fractal antenna array geometries (i.e., square, diamond, hexagon, and octagon) have been designed and simulated. Upon comparing antenna array metrics, the octagonal fractal antenna array has yielded minimal sidelobe levels with a gain of 15.7 dBi at 900 MHz, close to that of the square geometry but with 32.27% lower physical aperture area. The octagonal fractal antenna array has been chosen as the optimum geometry with reduced aperture area and reduced side lobes while retaining the bandwidth and gain milestone metrics.

(G) The ML models available (radial basis function (RBF), least square regression (LSR) and, hyper kriging (HK)) in Altair Hyperstudy were employed to predict the output response of a fractal antenna. RBF and LSR were down selected from the initial three ML models based upon their generalization capability for prediction of fractal antenna output response. The test RMSE increased as the values drifted away from the mid-point of the training range. RBF performed well in the prediction of S_{11}, while LSR performed slightly better for gain and electric field predictions. In addition, for time-domain electric field prediction, we recommend using k-nearest neighbors (kNN) ML algorithm for accurate prediction.

(H) The initial application of the kNN ML model for the prediction of antenna array bandwidth response of center and corner element yielded positive results with good agreement between traditional EM solver (FEKO) and trained kNN ML model. The new LR ML model yielded improved RMSE values (over kNN) in its prediction of reflection coefficient (27.82% less RMSE for center element and 19.76% less RMSE for corner element). On the other hand, the RMSE values for gain (as function of theta) prediction using LR ML model has 55.51% increase over kNN prediction. Finally, kNN provides better generalization to predict reflection coefficient, whereas LR provides better generalization to predict frequency domain gain in the case of a fractal antenna array. On the other hand, the application of the AEP method for antenna array was put on hold due to its limitations.

(I) A GUI was developed, which accepts training data for an antenna (single-element or array) of user choice and can predict output response (S_{11} and gain) for a range of

test data within a few seconds. The GUI has been configured to perform parametric sweep analysis for S_{11} and gain response of a fractal antenna design. Finally, the current version of the GUI has been tested by users with two different antenna designs (i.e., a corrugated conical horn antenna and a traditional horn antenna with GRIN lens). The feedback/suggestions from the users have been recorded to update the GUI.

8.3.6 *References*

[1] H. Fallahi and Z. Atlasbaf, "Study of a Class of UWB CPW-Fed Monopole Antenna With Fractal Elements," in IEEE Antennas and Wireless Propagation Letters, vol. 12, pp. 1484-1487, 2013, doi: 10.1109/LAWP.2013.2289868.

[2] S. Zhang, X. Wang and L. Chang, "Radiation Pattern of Large Planar Arrays Using Four Small Subarrays," in IEEE Antennas and Wireless Propagation Letters, vol. 14, pp. 1196-1199, 2015, doi: 10.1109/LAWP.2015.2397600.

9 Feedback

There is no feedback to report for the current reporting period.

10 Program Management

10.1 Issues

i. Scope – No issues
ii. Budget – 12-month NCTE submitted/pending
iii. Schedule – No issues

10.2 Interactions with Others

Agency/Org	Performer	Project Name	Purpose of Research/ Collaboration

10.3 Major Procurement Actions

10.4 Travel

Destination	Purpose	Attendees	Estimated Costs

10.5 Pending or Upcoming Public Release Requests

11 Appendix A: Academic and IP Output

11.1 Students Graduated

Name	Degree	Currently
Al-Shaikhli, Waleed	MS Spring 19	Kansas City National Security Campus, Honeywell
Azad, Wasekul	PhD Summer 21	Applied Materials, Sunnyvale, CA
Berg, Jordan	MS Spring 21	MRI Global
Bhamidipati, John	PhD Spring 22	MIDE
Bissen, Bear	MS Spring 19	Capella Space, San Francisco, CA
Brasel, Sadie	BS Spring 21	
Floyd, Dennis	BS	Naval Air Warfare Center Weapons Division
Hanif, Abu	PhD Spring 21	
Harmon, Aaron	BS	Missouri University of Science & Technology
Harp, Joshua	MS	
Hauptman, Cash	BS Spring 18	University of Nebraska-Lincoln
Klappa, Paul	MS Spring 21	
Kovarik, James	MS 21	
Labrada, Dario	BS Spring 20	Honeywell Aerospace, Florida
Lancaster, John	MS Spring 17	Lawrence Livermore National Laboratory, CA
Renzelman, Jeff	MS Spring 18	Kansas City National Security Campus, Honeywell
Roy, Sourov	PhD Spring 21	BTCPower, Orange County, CA
Wagner, Adam	MS Fall 20	Los Alamos National Laboratory, New Mexico
Xia, Shengxuan	BS	Missouri University of Science & Technology

11.2 Journal Publications

11.2.1 *In Preparation*

[1] S. S. Indharapu, A. N. Caruso, K. C. Durbhakula, “Machine Learning Assisted Antenna Design Optimization of UWB Fractal Antenna,” TBD, In Preparation, **2022**.

[2] J. K. P Bhamidipati, G. Bhattarai, A. N. Caruso, “Effect of Proton Irradiation Induced Localized Defect/Trap Clusters on Silicon Photoconductive Semiconductor Switch (Si-PCSS) Recovery Time and Leakage currents,” *Solid-State Electronics,* In Preparation, **2022**.

[3] N. Gardner, K. C. Durbhakula, and A. N. Caruso, “UHF and L-Band Frequency Generation at MW Peak Power using Diode-based Nonlinear Transmission Lines as Pulse Forming Networks,” *Transactions on Plasma Science*, In Preparation, **2022**.

[4] N. Gardner, K. C. Durbhakula, and A. N. Caruso, “Electrically Tunable Diode-based Nonlinear Transmission Line,” *TBD*, In Preparation, **2022**.

[5] B. Barman, D. Chatterjee, K. C. Durbhakula, and A. N. Caruso, “Tradespace Analysis of Wideband, Electrically Small Microstrip Patch Antenna Elements for

Phased Array Applications," *IEEE Antennas and Propagation Magazine,* In preparation, **2022**.

[6] S. Xia, J. Hunter, A. Harmon, M. Hamdalla, A. Hassan, V. Khilkevich, D. Beetner, "Simulation Driven Statistical Analysis of the Electro-magnetic Coupling to Microstriplines," *IEEE Transactions on Electromagnetic Compatibility*, In Preparation, **2020**.

[7] M. Hamdalla, V. Khilkevich, D. G. Beetner, A. N. Caruso, A. M. Hassan, "Characteristic Mode Analysis Justification of the Stochastic Electromagnetic Field Coupling to Randomly Shaped Wires," *IEEE Transactions on Electromagnetic Compatibility*, In Preparation, **2020**.

11.2.2 *Submitted / Under Revision*

[8] J. K. P. Bhamidipati, E. R. Myers, A. M. Conway, L. F. Voss, M. M. Paquette, and A. N. Caruso, "Figure of Merit Development for Linear-Mode Photoconductive Solid-State Switches," *IEEE Journal of the Electron Devices Society*, Submitted May 1 **2022**, Manuscript ID#JEDS-2022-05-0136-R.

[9] J. K. P. Bhamidipati, K. C. Durbhakula, and A. N. Caruso, "A Dynamically Tunable Discrete-Element Transmission Line Pulse Generator," *International Journal of Electronics and Communications*, Submitted March 6 **2022**, Manuscript ID#AEUE-S-22-01270.

[10] B. Barman, K. C. Durbhakula, D. Chatterjee, and A. N. Caruso, "Comparison of Machine Learning Algorithms for Bandwidth Enhancement of a Coaxial Probe-fed Microstrip Patch Antenna," *Applied Computational Electromagnetics Society (ACES)*, Under Revision (Accepted with Major Revisions), **2022**.

[11] B. K. Lau, M. Capek, and A. M. Hassan, "Characteristic Modes–Progress, Overview, and Future Perspectives," *IEEE Antennas and Propagation Magazine*, Submitted, **2021**.

[12] K. Alsultan, M. Z. M. Hamdalla, S. Dey, P. Rao, and A. M. Hassan, "Scalable and Fast Characteristic Mode Analysis Implementation Using a Hybrid CPU/GPU Platform," *ACES*, Submitted, **2021**.

[13] W. Azad, F. Khan, and A. N. Caruso, "A Scalable Multilevel-Modular 10 kV Silicon Carbide MOSFET Module Featuring Custom Isolated Gate Driver Circuit Combined with Coupling and Snubber Circuits," *IEEE Transactions on Power Electronics*, Submitted, **2021.**

11.2.3 *Published / In Press*

[14] N. Gardner, K. C. Durbhakula, and A. N. Caruso, "Design Considerations for Diode-Based Nonlinear Transmission Lines," *AIP Advances*, 12, 055012, **May 2022** [doi].

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[17] W. Azad, F. Khan, and A. N. Caruso, “A Medium Power, Self-Sustaining, Configurable RF Pulse Generation Circuit Using a Nonlinear Transmission Line and Power Amplifier in a Closed Loop Configuration, *IEEE Transactions on Plasma Science*, vol. 49, no. 7, pp. 2183–2194, **July 2021** [doi].

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[19] K. C. Durbhakula, D. Chatterjee, and A. M. Hassan, “An Efficient Algorithm for Locating TE and TM Poles for a Class of Multiscale Inhomogeneous Media Problems,” *IEEE Journal on Multiscale and Multiphysics Computational Techniques*, vol. 4, no. 1, pp. 364–373, **Dec 2019** [doi].

11.3 Conference Publications

11.3.1 *Submitted / Accepted*

[1] B. Barman, D. Chatterjee, and A. N. Caruso, "Characterization of Planar Phased Arrays of Electrically Small UWB Microstrip Patch Antennas," *2022 IEEE International Symposium on Phased Array and Technology,* Waltham, Massachusetts, USA, Oct. 11-14, 2022, pp. 1-8. (Submitted).

[2] B. Barman, D. Chatterjee, and A. N. Caruso, "On the Optimum Substrate Selection in Wideband Microstrip Patch Antenna Design," *2022 IEEE International Symposium on Antennas & Propagation & USNC-URSI Radio Science Meeting*, Denver, Colorado, USA, July 10-15, 2022, pp. 1-2. (Accepted)

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11.4 Conference Presentations

11.4.1 *Submitted / Accepted*

[1] S. Bellinger, A. Caruso, A. Usenko, "Stacked Diodes for Pulsed Power Applications," GOMACTech-22, Miami, FL, March 21–24 2022 (submitted, oral).

[2] S. Bellinger, A. Caruso, A. Usenko, "New Paradigm on Making Semiconductor Opening Switches for Pulsed Power," 2021 23rd IEEE Pulsed Power Conference, Denver, CO, Dec. 12–16, 2021 (accepted, oral).

Directed Energy Professional Society, Directed Energy Systems Symposium, Washington DC, October 25-29 2021 (submitted):

[3] B. Barman, D. Chatterjee, A. Caruso, and K. Durbhakula, "Tradespace Analysis of a Phased Array of Microstrip Patch Electrically Small Antennas (ESAs)" (Poster)

[4] J. N. Berg, R. C. Allen, and S. Sobhansarbandi, "A Novel Method of Cooling a Semiconductor Device through a Jet Impingement Thermal Management System: CFD Modeling and Experimental Evaluation" (Poster)

[5] J. N. Berg, R. C. Allen, and S. Sobhansarbandi, "Heat Transfer Enhancement of a Jet Impingement Thermal Management System: A Comparison of Various Nanofluid Mixtures" (Poster)

[6] J. Bhamidipati, M. Paquette, R. Allen, and A. Caruso, "Photoconductive Semiconductor Switch Enabled Multi-Stage Optical Source Driver" (Poster)

[7] G. Bhattarai, J. Eifler, S. Roy, M. Hyde, J. Bhamidipati, A. Usenko, M. Pederson, M. Paquette, A. Caruso, S. Bellinger, L. Voss, and R. Allen, "All Solid-State High-Power Pulse Sharpeners" (Poster)

[8] S. Brasel, K. Norris, R. Allen, A. Caruso, and K. Durbhakula, "Efforts to Reduce Physical Aperture Area of Ultra-Wideband Arrays" (Poster)

[9] A Caruso, "ONR Short Pulse Research and Evaluation for c-sUAV: Supporting and Sub-Programs Overview" (Oral)

[10] J. Clark, R. C. Allen, and S. Sobhansarbandi, "Ultra-Compact Integrated Cooling System Development" (Poster)

[11] J. Eifler, S. Roy, M. Hyde, G. Bhattarai, J. Bhamidipati, A. Usenko, M. Pederson, M. Paquette, A. Caruso, S. Bellinger, L. Voss, and R. Allen, "TCAD Optimization of Epitaxially Grown Drift-Step Recovery Diodes and Pulser Performance" (Poster)

[12] N. Gardner, M. Paquette, and A. Caruso, "Diode-Based Nonlinear Transmission Lines Capable of GHz Frequency Generation at Single MW Peak Powers" (Poster)

[13] M. Hamdalla, A. Caruso, and A. Hassan, “The Shielding Effectiveness of UAV Frames to External RF Interference” (Poster)

[14] M. Hamdalla, A. Caruso, and A. Hassan, “A Predictive-Package for Electromagnetic Coupling to Nonlinear-Electronics using Equivalent-Circuits and Characteristic-Modes (PECNEC)” (Poster)

[15] M. Hyde, J. Eifler, S. Roy, G. Bhattarai, A. Usenko, M. Paquette, A. Caruso, S. Bellinger, L. Voss, and R. Allen, “Development of an Evaluation Network for Drift Step Recovered Diodes through and Augmented Design of Experiment” (Poster)

[16] S. Indharapu, A. Caruso, and K. Durbhakula, “Machine Learning Based Ultra-Wideband Antenna Array Optimization and Prediction” (Poster)

[17] F. Khan, W. Azad, and A. Caruso, “A Scalable Multilevel-Modular 10 kV Silicon Carbide MOSFET Architecture for Pulsed Power Applications” (Poster)

[18] D. F. Noor, J. Eifler, M. Hyde, G. Bhattarai, S. Roy, J. Bhamidipati, A. Usenko, M. Pederson, M. Paquette, A. Caruso, S. Bellinger, L. Voss, and R. Allen, “DSRD-IES Pulsed-Power Generator Topology Study Using Machine-Learning-Based Feature Selection Optimization and Predictive Learning” (Poster)

[19] S. Roy, J. Eifler, M. Hyde, G. Bhattarai, D. Noor, J. Bhamidipati, A. Usenko, M. Pederson, M. Paquette, A. Caruso, S. Bellinger, L. Voss, and R. Allen, “Systematic Topological Optimization of DSRD-Based IES Pulse Generator” (Poster)

[20] S. Shepard and A. Caruso, “Tubular Core Optical Power Amplifier” (Poster)

[21] H. Thompson, M. Paquette, and A. Caruso, “Minimizing On-State Resistance in GaN:X Photoconductive Semiconductor Switches (PCSSs) for Direct Modulation (Poster)

[22] A. Usenko, J. Eifler, S. Roy, G. Bhattarai, M. Hyde, M. Paquette, A. Caruso, S. Bellinger, L. Voss, and R. Allen, “New Paradigm in Fabrication of Semiconductor Opening Switches for Pulsed Power” (Poster)

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[23] S. Bellinger, A. Caruso, A. Usenko, “Stacked Diodes for Pulsed Power Applications: New Process Integration Scheme,” 240th Electrochemical Society Meeting, Orlando, FL, Oct. 10–14, 2021 (submitted, oral).

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[24] W. Azad, S. Roy, and F. Khan, “A Four-State Capacitively Coupled High-Voltage Switch Powered by a Single Gate Driver,” *47th IEEE Conference on Plasma Science*, Singapore, December 6-10, 2020 (oral).

[25] J. Hunter, S. Xia, A. Harmon, A. Hassan, V. Khilkevich, and D. Beetner, “Simulation-Driven Statistical Characterization of Electromagnetic Coupling to UAVS,” *Annual Directed Energy Science and Technology Symposium*, March 2020 (abstract appeared, but talk cancelled due to pandemic).

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[26] William Spaeth, Wideband Parallel Plate to Coaxial Cable Taper

[27] Stefan Wagner, Quickly Determining Minimum HPC Source Requirements Using Binary Search

***

GOMAC 2019

[28] Cash Hauptmann, Reduced Recovery Time in SiPCSS Photoconductive Switches

[29] Eliot Myers, Picosecond High Power Switching Technologies

[30] Heather Thompson, GaN Optimization for Use in Photoconductive Switch

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[28] B. Barman, D. Chatterjee, and A. N. Caruso, “Analytical Models for L-Probe fed Microstrip Antennas,” *Proceedings of the IEEE Antennas and Propagation International Symposium and National Radio Science Meeting*, Atlanta, Georgia, USA, July 7-12, 2019 (1 page URSI Abstract).

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Directed Energy Professional Society (DEPS) Annual Science and Technology Symposium, Destin, Florida, USA, April 2019:

[29] Ryan Butler, Mechanical Challenges of Modular Photoconductive Semiconductor Based HPM Sources

[30] Steve Young, Two-Dimensional Optoelectronic Pulsed Power Switches: Initial Effort

[31] Adam Wagner, Rapid Cost Effective RF Component Prototyping Using 3D Printers

[32] Heather Thompson, Cost to benefit analysis of GaN for Photoconductive Semiconductor Switches

[33] Colby Landwehr, Low Leakage Electroluminescence For Improving SiPCSS Hold Off

[34] James Kovarik, Some Investigations Into Applications Of Electrically Small Antennas As Phased Array Elements

[35] Spencer Fry, Maximizing SiPCSS Efficiency For HPM Sources

[36] Deb Chatterjee, Studies On Antenna Characterization And Propagation Of High Power Pulsed Electromagnetic Waves With Minimal Dispersion

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DEPS Posters and Presentations 2018

[37] Jeff Scully, ElectroLuminescence Studies of Silicon Based Photo-Switches

[38] Cash Hauptmann, Thermal Anlaysis of a PCSS through TCAD Simulation

[39] Nicholas Flippin, Fast Rise Time Switches: Drift Step Recovery Diode

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DEPS Posters and Presentations 2017

[40] Noah Kramer, Recent Results of Silicon Based Photoconductive Solid State Switches for 500kHz Continuous Pulse Repetition Frequency

11.5 Theses and Dissertations

[1] John Keerthi Paul Bhamidipati, “Pulse Generation, Shaping, and Optimization Solutions for Solid-State-Switch-Enabled High-Power Microwave Generation Systems” PhD Dissertation in Physics and Electrical Engineering, University of Missouri-Kansas City, **2022**.

[2] Jordan N. Berg, “Development of a Jet Impingement Thermal Management System for a Semiconductor Device with the Implementation of Dielectric Nanofluids,” MS Thesis in Mechanical Engineering, University of Missouri-Kansas City, **2021** [mospace].

[3] James C. Kovarik, “Wideband High-Power Transmission Line Pulse Transformers,” MS Thesis in Electrical Engineering, **2021** [mospace].

[4] Wasekul Azad, “Development of Pulsed Power Sources Using Self-Sustaining Nonlinear Transmission Lines and High-Voltage Solid-State Switches,” PhD Dissertation in Electrical Engineering, **2021** [mospace].

[5] Paul Klappa, “Implementation and Assessment of State Estimation Algorithms in Simulation and Real-World Applications,” MS Thesis in Mechanical Engineering, **2021** [mospace].

11.6 IP Disclosures Filed

[1] S. Bellinger, A. Caruso, A. Usenko, US Provisional Patent Application “Stacked Diode with Side Passivation and Method of Making the Same,” 12AUG2021.

[2] S. Bellinger, A. Caruso, A. Usenko, “Diode and Method of Making the Same,” 28JUNE2021.

[3] Bhamidipati, Myers, Caruso, “Multi-Stage Photo-Stimulated WBG-PCSS Driven RF Pulse Generation System Implementing Miniature Optical Sources,” 21UMK009, 04NOV2020.

[4] Shepard, “A Low Noise Optical Amplifier,” 21UMK007, 14SEPT2020.

[5] Shepard, “A Novel Optical Fiber Amplifier,” 20UMK012, 02JUN2020.

[6] Doynov, “High-power High Repetition Rate Microwaves Generation with Differentially Driven Antenna,” 20UMK011, 19APR2020.

[7] Doynov, “Scalable Modular System for High-power Microwaves Generation,” 20UMK010, 19APR2020.

[8] Doynov, “Pulse Differential High-power Microwave Generation,” 19UMK007, 02JAN2019.

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11.7 Provisional Patents Filed

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[4] Plamen Doynov, James Prager, Tim Ziemba, Anthony N. Caruso, “Non-Linear Transmission Line Topologies for Improved Output”, USPTO Provisional Serial No. 62/737,185, filed 27SEPT2018.

11.8 Non-Provisional Patents Filed

None to date

ONR HPM Program – Monthly Status Report (MSR) – July 2022

Anthony Caruso – Univ. Missouri – Kansas City

N00014-17-1-3016 [OSPRES Grant]

ONR Short Pulse Research, Evaluation and non-SWaP Demonstration for C-sUAS Study

15 AUG 2022

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1 Contents

2 Executive Summary

2.1 Progress, Significant Findings, and Impact

Fiber Laser and Optical Amplifiers. Continuing with the design of a beam shaping, optical power combiner, we determined the length for maximal coupling of cladding modes into the central core mode and find it to be 20 Rayleigh lengths (for both the 6-tube and 7-tube power combiner designs). Beyond that length, surface waves (on the air/glass interfaces) arise at the expense of the core mode energy. Leveraging this technology into RF antenna design, we find similar behavior when we line the walls of a rectangular waveguide feed to a dual ridge horn antenna with glass tubes. An overly simplified model helps to visualize how the *transverse* resonance effects of the tubes affect the overall waveguide. Therein we can think of each tube as a Fabry–Perot resonator (for the transverse direction of propagation). When off-resonance, the mode strongly reflects from the tube, which in effect shortens the distance between the copper walls. It is only when we are on-resonance that the mode will penetrate the tubes all the way to the copper walls and sense the original copper waveguide dimensions. It is important to note that this is a *transverse* resonance effect – the use of a *longitudinal* resonator would confine energy to be on the antenna; ours only confines the beam shape to be centered or not (with nothing impeding the longitudinal direction of propagation).

DSRD Optimization Simulations. The latest drift-step recovery diode (DSRD) pulser design and MOSFETs have been successfully converted from LTspice format to SmartSpice, and we have successfully simulated DSRD pulser output with the sectionally fit EG forward IV. Fitting of the forward IV, reverse CV, and recovery parameters of the DSRD tested in the pulser to match pulses for peak voltage, risetime, and pulsewidth is in progress for the CMC DSRD model. Next is assessing the recovery model over prime voltages, trigger durations and DSRD used to develop the CMC DSRD model for predictive simulation and determining the relationship between DSRD and circuit parameters for optimal DSRD pulser design and performance.

DSRD Design of Experiments. Forward IV measurements for the Gen2 and EG DSRD inventory have been completed using both the Keithley 2450 and Tektronik 371, and electrical breakdown measurements using the 371. The analysis of the forward IV and breakdown data allowed selection of the best performing DSRD for the DSRD pulser and ultimately the achievement of experimental 9 kV load voltage (see below).

DSRD-Based Pulsed Power Source Optimization. The effort towards developing the DSRD-based pulser and its extension towards a M×N stack continues. Multiple air core inductors required for the pulser circuit were designed, fabricated, and characterized. Using a newly designed and fabricated MOSFET driver circuit, we have achieved a maximum pulsed output voltage of 9.2 kV with a 20–90% risetime of 5 ns from a pulser designed to produce 10 kV.

Pulse-Compression-Based Signal Amplification. A prototype magnetic pulse compression (MPC) circuit with continuous-wave input at low frequencies will be fabricated as proof of concept before finalizing the KRI SoW on high-frequency magnetic material development. Commercially available magnetic cores were investigated for their

suitability for the MPC prototype operating at kHz to MHz frequency range. Only three magnetic materials are commercially available with a cutoff frequency of 200 MHz and higher. Considering the need for high permeability, sharp saturation, and low coercivity for high compression gain as well as the toroids readily available for purchase, Material 68 from Fair-Rite was selected for the prototype. The prototype design will proceed with the downselected toroids. MPC simulations were continued to observe the effects of resistive loading. Optimal energy transfer can be obtained with impedance matching at the output stage. MPC design equations that affect the load resistance value were derived. Some voltage and current artifacts due to non-ideal switch behavior were observed with resistive loading, and as this behavior can be detrimental to continuous wave MPC operation, different loading schemes will be investigated.

Antennas. The boresight gain of the recently manufactured, tapered, coaxial-connector-fed, small, wideband microstrip patch antenna element, for operation in the UHF (0.7–1.2 GHz) region, was tested in an anechoic chamber. The test results showed reasonable agreement, especially at the higher frequency end, with the simulated data, despite manufacturing defects and electromagnetic discontinuities in the prototype. Manufacturing of an improved version of the prototype is underway and is expected to mitigate the fabrication errors. A successful testing of the improved prototype will be followed by manufacturing of the final demonstrable 4×4 array, which is currently being characterized.

The Koshelev antenna combined with the integrated gradient dielectric transformer design has been structurally modified to 3D print and metalize an improved antenna prototype. Before printing, the new design models were tested using electromagnetic (EM) wave solvers for radiofrequency antenna response. In comparison with the ideal Koshelev antenna, the RF performance of the new model did not deteriorate in terms of reflection coefficient and frequency domain gain. The structurally robust Koshelev antenna design has demonstrated the ability to develop a new 3D-print-based antenna prototype without affecting the RF performance.

The in-house graphical user interface (GUI) that uses machine learning (ML) algorithms to predict RF antenna responses has been upgraded to include antenna pattern plot prediction and new options to perform better data analysis. The root mean square error (RMSE) value obtained for the antenna pattern prediction is less than 1, indicating a good predictive behavior by the ML algorithm in a few seconds. The tool has been updated to train using a higher number of data samples to increase the prediction accuracy and reduce the error value between actual and predicted antenna responses. Overall, the tool can perform a tradespace study of a single element antenna design using ML algorithms within a few seconds (excluding training) while retaining antenna response accuracy (RMSE < 1).

2.2 Completed, Ongoing, and Cancelled Sub-Efforts

	Start	End
2.2.1 *Ongoing Sub-Efforts*		
GaN:C Modeling and Optimization	OCT 2017	Present
Diode-Based Non-Linear Transmission Lines	FEB 2018	Present
Trade Space Analysis of Microstrip Patch Arrays	FEB 2019	Present
Lasers and Optics	FEB 2020	Present
UWB Antenna Element Tradespace for Arrays	MAY 2020	Present
Si-PCSS Contact and Cooling Optimization	JAN 2021	Present
Drift-Step Recovery Diode Optimization Simulations	JAN 2021	Present
DSRD-Based IES Pulse Generator Development	APR 2021	Present
Drift-Step Recovery Diode Manufacturing	MAY 2021	Present
DSRD Characterization through Design of Experiments	MAY 2021	Present
Sub-Nanosecond Megawatt Pulse Shaper Alternatives	MAY 2021	Present
Ultra-Compact Integrated Cooling System Development	MAY 2021	Present
Continuous Wave Diode-NLTL Based Comb Generator	SEPT 2021	Present
Pulse-Compression-Based Signal Amplification	DEC 2021	Present
2.2.2 *Completed/Transferred Sub-Efforts*		
Adaptive Design-of-Experiments	OCT 2017	APR 2019
Non-perturbing UAV Diagnostics	OCT 2017	OCT 2018
Noise Injection as HPM Surrogate	OCT 2017	MAR 2019
SiC:N,V Properties (w/ LLNL)	APR 2018	MAR 2019
Helical Antennas and the Fidelity Factor	JUL 2018	SEPT 2019
Si-PCSS Top Contact Optimization	APR 2020	OCT 2020
Nanofluid Heat Transfer Fluid	NOV 2020	JUL 2021
HV Switch Pulsed Chargers	DEC 2018	DEC 2021
Enclosure Effects on RF Coupling	OCT2019	DEC 2021
UAS Engagement M&S	MAR 2021	DEC 2021
GaN-Based Power Amplifier RF Source	AUG 2021	DEC 2021
2.2.3 *Cancelled/Suspended Sub-Efforts*		
Ab Initio Informed TCAD	OCT 2017	OCT 2020
Positive Feedback Non-Linear Transmission Line	NOV 2017	DEC 2018
Minimally Dispersive Waves	FEB 2018	SEPT 2018
Multiferroic-Non-linear Transmission Line	NOV 2018	APR 2019
Avalanche-based PCSS	SEPT 2018	SEPT 2019
Gyromagnetic-NLTL	DEC 2017	NOV 2020
Multi-Stage BPFTL	APR 2020	JUL 2020
Heat Transfer by Jet Impingement	MAY 2018	FEB 2021
Si, SiC, and GaN Modeling and Optimization	NOV 2018	FEB 2021
Bistable Operation of GaN	FEB 2021	MAR 2021
WBG-PCSS Enabled Laser Diode Array Driver	NOV 2020	JAN 2022

2.3 Running Total of Academic and IP Program Output

See Appendix for authors, titles and inventors (this list is continuously being updated)

Students Graduated	*6 BS, 9 MS, 4 PhD*
Journal Publications	*6 (6 submitted/under revision)*
Conference Publications	*35 (3 submitted/accepted)*
External Presentations/Briefings	*40*
Theses and Dissertations	*5*
IP Disclosures Filed	*10*
Provisional Patents Filed	*4*
Non-Provisional Patents Filed	*0*

3 Laser Development

3.1 Fiber Lasers and Optical Amplifiers

(Scott Shepard)

3.1.1 *Problem Statement, Approach, and Context*

Primary Problem: High-average-power 1064-nm picosecond lasers are too large (over 1100 cm^3/W) and too expensive (over \$1000/μJ per pulse) for PCSS (photoconductive semiconductor switch) embodiments of HPM-based defense systems. For example, a laser of this class might occupy a volume of 1 m x 30 cm x 30 cm = 90,000 cm^3 and provide an average power of 50 W (thus, 1800 cm^3/W). Costs in this class range from \$100K to \$300K to drive our Si-PCSS applications.

Solution Space: Optically pumped ytterbium-doped optical fiber amplifiers, fed by a low-power stable seed laser diode, can offer a cost-effective, low-weight, and small-volume solution (with respect to traditional fiber and traditional free-space laser designs). Moreover, our novel optical amplifier tubes, might operate at far higher power levels (over 1000 times greater), thus driving an entire array of PCSS with a single amplifier and thereby reducing the overall system costs and eliminating the optical pulse-to-pulse jitter constraints.

Sub-Problem (1): Optical pump power system costs account for over 50% of the budget for each laser (in this class, for normal/free-space, optical fiber, and tubular embodiments).

Sub-Problem (2): Fiber (as well as power tube) optical amplifier performance is degraded primarily by amplified spontaneous emission (ASE) noise, which limits the operating power point, and by nonlinearities, which distort the optical pulse shapes.

State-of-the-Art (SOTA): Free-space NdYAG lasers or Ytterbium-doped fiber amplifiers optimized for LIDAR, cutting, and other applications.

Deficiency in the SOTA: Optical pump power system costs (in either free-space or fiber lasers) are prohibitive for the PCSS applications until reduced by a factor of at least two.

Solution Proposed: Fiber lasers permit a pre-burst optical pumping technique (wherein we pump at a lower level over a longer time) which can reduce pumping costs by a factor of at least ten. To address the ASE and nonlinear impairments, we are pursuing the use of gain saturation and a staged design of different fiber diameters. We also apply these techniques to fiber amplifiers which incorporate our power amplifier tube in the final stage. The inclusion of our novel tubular-core power amplifier stage should permit a single laser to trigger an array of several PCSS (reducing system cost and mitigating timing jitter).

Relevance to OSPRES Grant Objective: The enhancement in SWaP-C^2 for the laser system enables PCSS systems for viable deployment via: a factor of 40 in pumping cost reduction of each laser; and a factor of *N* in system cost reductions as a single laser could drive *N* (at least 12) PCSS in an array, while also eliminating the optical jitter constraints.

Risks, Payoffs, and Challenges: Optically pumping outside the laser pulse burst time can enhance the ASE; pump costs could be reduced by 40, but ASE in the presence of dispersion and/or nonlinearities could enhance timing jitter thereby limiting steerability. The main challenge for power tube implementation is the entrance optics design.

3.1.2 *Tasks and Milestones / Timeline / Status*

(A) Devise a pre-burst optical pumping scheme by which we can reduce the costs of the laser by a factor of two or more and calculate the resulting increase in ASE. / FEB–JUL 2020 / Completed.

(B) Reduce the ASE via gain saturation. / Oct 2020 / Completed.

(C) Design saturable gain devices which avoid nonlinear damage. / Ongoing.

(D) Calculate and ensure that timing jitter remains less than +/-15 ps with a probability greater than 0.9. / Ongoing.

(E) Demonstrate a cost-reduced fiber laser: the level of success to be quantified via the amount of ASE growth per duration of a pre-burst pumping interval. Growth of 100 uw over 6 ms (the limit in theory) would be considered outstanding. / August 2022.

(E1) March 2021 Finalize design. / Completed.
(E2) April 2021 Assemble and test-check seed LD (laser diode)/driver. / Completed.
(E3) April 2021 Measure power vs current transfer function of seed LD/driver. / Completed.
(E4) May–July 2021 Measure ASE and jitter of 1064 nm seed LD/driver. / Completed.
(E5) May–July 2021 Measure ASE and jitter of 1030 nm seed LD/driver. / Completed.
(E6) June–July 2021 Assemble and test-check pump LDs/drivers. / Completed.
(E7) June–July 2021 Measure power vs current transfer function of pump LDs/drivers. / Completed.
(E8) July–September 2021 Splice power combiners to Yb doped preamp fiber. /Completed.
(E9) July–September 2021 Connect seed and pumps to power combiners and test-check. / Completed.
(E10) September–October 2021 Measure gain, ASE and jitter of 1064 nm preamp assembly (forward, backward and bidirectional pumping) as a function of pump power and duty cycle. / Partially completed before task eliminated.
(E11) September–October 2021 Measure gain, ASE and jitter of 1030 nm preamp assembly (forward, backward and bidirectional pumping) as a function of pump power and duty cycle. / Partially completed before task eliminated.
(E12) November 2021 Splice power amplifier and its power combiner to best preamp. / Partially completed before task eliminated.
(E13) May–August 2022 Measure gain, ASE and jitter of entire amp assembly. / Ongoing.
(E14) May–August 2022 Analyze data and document. / Ongoing.

(F) Design a new type of higher power, tubular core fiber amplifier. / May–August 2022.

(F1) Apply one high-power tubular amplifier to a system comprised of an array of several (say N) PCSS. For example: N=12 in a 3x4 array (or 4x4 array with corners omitted) N=16 in a 4x4 array, etc.; thereby eliminating jitter constraints and reducing laser system cost by more than a factor of 100 (independent of burst profile). / August 2022.

(F2) Design a high power, multiple tube optical amplifier and determine if it permits advantages for power handling or beam profile. / August 2022 / Initiated.

(G1) Design a beam shaping, optical power combiner using a cladding of 6 tubes. / June 2022 / Completed.

(G1.1) Develop COMSOL models. / April 2022 / Completed.

(G1.2) Discover and optimize the length at which the cladding modes couple maximal power into the core mode (of the entire waveguide). / June 2022 / Completed.

(G2) Design a beam shaping, optical power combiner using a cladding of 6 tubes surrounding one inner tube. / July 2022 / Completed.

(G2.1) Develop COMSOL models. / April 2022 / Completed.

(G2.2) Discover and optimize the length at which the cladding modes couple maximal power into the inner tube. / July 2022 / Completed.

(G3) Develop spectral combiners based on multiple-tube waveguides and compare to existing PCF (photonic crystal fiber) technologies. / August 2022 / Completed.

3.1.3 *Progress Made Since Last Report*

(G1.2) (G2.2) Our beam shaping, optical power combiner designs are a spin-off of our tubular optical power amplifier innovations. The research at optical frequencies, on capillary-sized tubes [hundreds of microns], has also opened the door to a means of extending such techniques to patch and horn antennas via larger sized tubes [ones of centimeters] at RF frequencies (e.g., 600 MHz – 6 GHz). At optical frequencies we have completed the tasks (G1.2) (G2.2) of determining the length for maximal coupling of cladding modes into the central core mode and find it to be 20 Rayleigh lengths for both the 6-tube and 7-tube designs. After that length we found that surface waves (on the air/glass interfaces) arise at the expense of the core mode energy. Leveraging this technology into RF we find similar behavior where these surface waves could be used as pencil beams, as detailed in 3.1.4. We also created a simple model for the estimation of the reconfigurable bandwidths and center frequencies enabled by such structures.

(G3) The partially-completed task of designing spectral power combiners is now complete since we find no photonic crystal fiber that can surpass the 300 nm spectral width (at > 90% power transmission) of a water-filled glass tube (at a waveguide length of 2 meters).

3.1.4 *Technical Results*

(G1.2) (G2.2) Our 6-tube and 7-tube power combiners utilized a circular glass outer tube as shown in Fig. 3.1.1. In both cases the power transfer from a glass-cladding mode into a hollow air-core mode will increase with waveguide length until a distance at which

surface waves arise. These are special waves which “hug” the air/glass interface (rather than reflect from it).

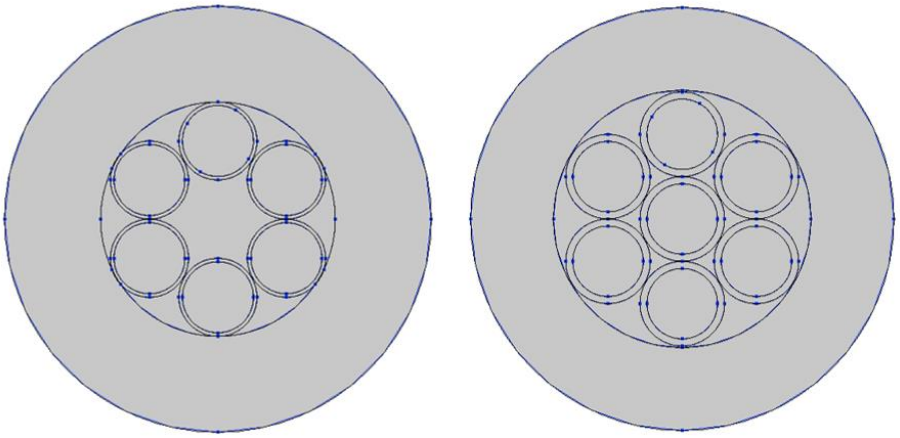

Fig. 3.1.1. 6-tube (left) and 7-tube (right) power combiner geometries.

The onset (and later dominance) of the surface waves depends on the waveguide length with respect to the Rayleigh length, $z_R = \pi\omega_0^2/\lambda$, where ω_0 is the beam-waist (i.e., the 1/e radius) and λ the wavelength in the media of refractive index *n*. We have observed that the onset of surface waves occurs abruptly at a waveguide length of 20 z_R as in the left figure of Fig. 3.1.2, wherein we launched a Gaussian beam in the center of the rightmost tube at the input.

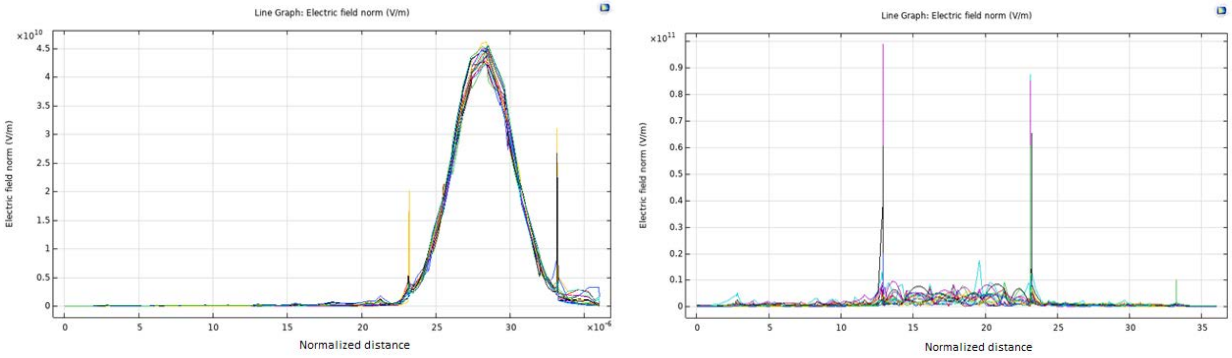

Fig. 3.1.2. Electric field vs normalized transverse distance across the waveguide (at a waveguide length of 20 z_R on the left; and a waveguide length of 40 z_R on the right).

The left figure of Fig. 3.1.2 clearly shows the remnant of that Gaussian beam profile as well as strikingly narrow “spikes” on each side of the Gaussian, which are confirmed (via accounting for energy changes elsewhere in the guide) to be surface waves which suddenly originate at that distance down the waveguide. At shorter distances they are essentially unobservable. The colors in the figure correspond to different frequencies and

the resonant conditions are controllable via the index *n* and the tube dimensions. At longer distances the surface waves continue to grow in field strength (at the expense of the energy in the Gaussian mode). At a waveguide length of 40 z_R, as in the right figure of Fig. 3.1.2 wherein we launched a Gaussian beam in the center of the entire guide, we find no output Gaussian beam is discernable as virtually all of the energy has gone into the surface waves which have created these “pencil beams.” These can be turned on or off by exploiting their frequency dependance; or controlling the refractive index; or mechanically telescoping the length of the waveguide.

The lengths required are compatible with dual ridge horn antenna dimensions and the glass tubes can line the walls of its rectangular waveguide feed and/or the ridge itself. For example, with a rectangular feed of width = 20.9 cm and height = 15.5 cm we can readily fit a lining of tubes resembling (or made from) fluorescent light bulbs and so have ω_0= 1 cm. At 1 GHz, in air, we find z_R = 0.1047 cm so 20 z_R, or even 40 z_R, readily fits within its feed length of 9.296 cm (and/or along its ridge length of 39.37 cm). At lower frequencies z_R decreases so accommodating the length needed for surface wave induced pencil beams becomes even easier.

Glass tubes lining the copper walls of a rectangular waveguide are depicted in Fig.3.1.3. A simplified model for visualizing how the *transverse* resonance effects of the tubes affect the overall waveguide is to think of each tube as a Fabry-Perot resonator influencing the transverse direction of propagation. This model is too simplified for resonance prediction since it neglects the wave nature of the diffracting beams scattering off of curved reflectors within a 2D rectangular structure – but it provides a visualization of the underlying physics. When off-resonance the mode strongly reflects from the tube, which in effect shortens the distance between the copper walls. It is only when we are on-resonance that the mode will penetrate the tubes all the way to the copper walls and sense the original copper waveguide dimensions. It is important to note that this is a *transverse* resonance effect – the use of a *longitudinal* resonator would confine energy to be on the antenna; ours only confines the beam shape to be centered or not (with nothing impeding the longitudinal direction of propagation).

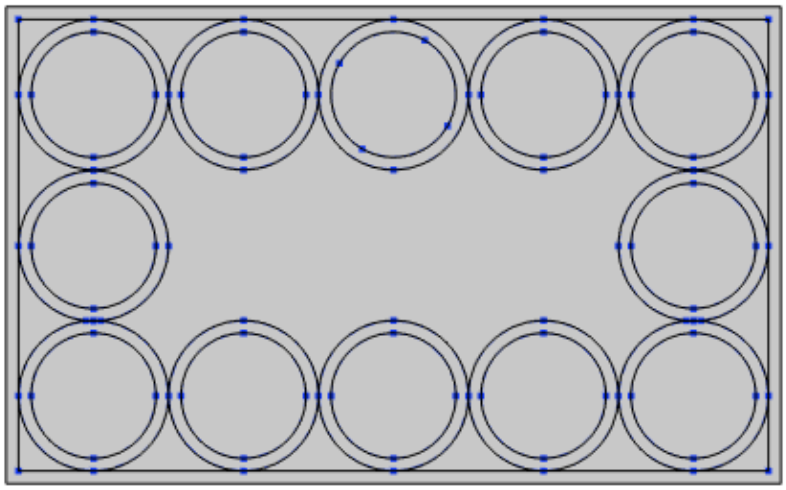

Fig. 3.1.3. Glass tubes lining the copper walls of a rectangular waveguide.

Preliminary results indicate a wide variety of mode patterns can be achieved. In addition to standard beam profiles we have observed some unusual ones, such as in Fig. 3.1.4 where we see how sharp features at the air/glass and glass/copper interfaces at one distance, *z,* (on the left) can evolve into an antisymmetric mode with surface waves at 2*z* (on the right).

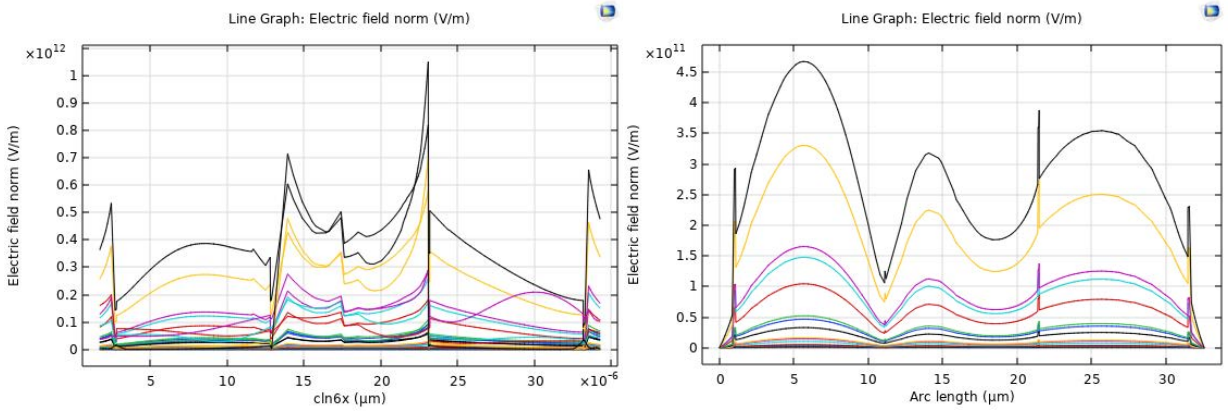

Fig.3.1.4. Sharp features at the air/glass and glass/copper interfaces (on the left) evolve into an antisymmetric mode with surface waves (on the right).

Another unusual mode pattern is exhibited in Fig. 3.1.5, where again we observe sharp features at the air/glass interface, but also a strong drop in field strength in the middle of the waveguide (between the glass tubes). We expect to alter this nulling in the middle into a constructive interference via an asymmetric variation on this case. The rapid oscillations within the tubes are also unusual and all of these features are strongly dependent on the dielectric constant (i.e., refractive index) of the material inside the tubes. For our patch antenna designs the “tubes” are shortened in length to “holes” and in both cases we expect to achieve reconfigurability by controlling the *transverse* resonance effects (rather than via, for example, a longitudinal phase shift).

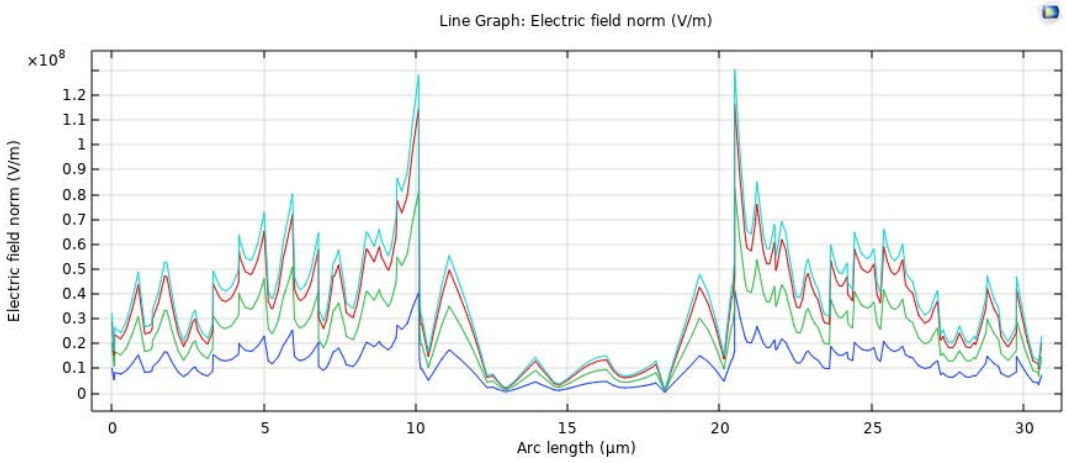

Fig.3.1.5. Sharp features at the air/glass interface and field nulling near the beam center.

3.1.5 *Summary of Significant Findings and Mission Impact*

(A) Our pre-burst optical pumping scheme simulations showed that we can drop the pump power costs by a factor of 40 with pre-burst ASE power levels below the heating level tolerance of 100 μW. UMKC invention disclosure filed 02JUN2020.

(B) For a proposed system gain of 8 million, a linear gain theory predicted the in-burst ASE would be over our heating level spec. by a factor of 3960, but by exploiting the nonlinearity of gain saturation we find that we can suppress the ASE by over 7000. UMKC invention disclosure filed 14SEP2020.

(C) Achieved initial practical device designs that exploit gain saturation, which remained below damage thresholds, via staged designs of different mode diameters NOV2020.

(D) Models of the impact of ASE on timing jitter in the presence of dispersion and/or nonlinearities were established JUL2020.

(E) The design of a proof-of-concept experiment demonstrating a cost-reduced optical pumping scheme was finalized MAR2021.

(F) We made (to our knowledge) the first observation of self-focusing effects that are not determined by beam power alone. We found instead that these can also be controlled via the geometric factors within a waveguide (such as fiber core diameter) MAY2021.

We additionally made (to our knowledge) the first observation that a mode exists in the air within a simple glass tube into which we can couple energy from the mode in the glass. Thus, an amplifier (in the doped and pumped glass) can operate at higher powers JUNE2021.

We found conditions under which 0.25 GW of power can exist in the tube's air-core mode when its glass-cladding mode is at a power level near 0.5 GW JULY2021.

Advancements in the very high-power operating point (tens of GW) of our tubular optical amplifier (and the existence, size and spatial uniformity of its air-core mode) were shown to permit a single laser to trigger an array of several (up to 100) Si-PCSS – reducing the laser system cost and eliminating the optical timing jitter constraint. The symmetry breaking of the scattering from self-focusing in a curved waveguide was shown to enable such AUG2021.

4 Photoconductive Switch Innovation

4.1 Characterizing and Optimizing On-State Resistance in GaN:X PCSS

(Heather Thompson)

Work is currently focused on manuscript preparation. Please see the April 2022 MSR for the most up-to-date summary of this project.

5 Drift-Step-Recovery-Diode-Based Source Alternatives

5.1 Drift-Step Recovery Diode and Pulse Shaping Device Optimization

(Jay Eifler)

5.1.1 *Problem Statement, Approach, and Context*

Primary Problem: Drift-step recovery diodes (DSRDs) and DSRD-based pulsed power systems are competitive with PCSS-based systems for HPM cUAS, with the benefit of not requiring a laser. Maximizing peak power while maintaining characteristic ns-order DSRD rise times requires optimization of the DSRD device design and pulser. Other considerations are for compactness, low-jitter, cooling required, and additional pulse-sharpening device within the pulse shaping head circuit. Additional goals for pulse repetition frequency are also to be satisfied for various applications.

Solution Space: By altering DSRD device parameters (geometry, doping, irradiation), optimize single-die and stack designs for peak power and risetime within various inductive pulser circuit topologies. Also optimize the pulse sharpening device (PSD) within the pulse shaping head circuit.

Sub-Problem 1: TCAD and SPICE models of the DSRD are inaccurate and must be improved. PSD models have not been developed.

Sub-Problem 2: Inductive pulser designs are complicated by the DSRD (and PSD) parameter variability. Use TCAD and/or SPICE models to account for variability and improve pulser design.

State-of-the-Art (SOTA): MW peak power and ns-order risetimes have been achieved in DSRD-based pulsed-power systems employing DSRD stacks for higher voltage holding and parallel lines of DSRD to increase current. PSD have sharpened DSRD pulses to 100 ps-order.

Deficiency in the SOTA: A lack of accurate TCAD and SPICE models make design of DSRD and DSRD-based inductive pulser circuit topologies (with or without PSDs) difficult to the level of tens of MW of peak power while maintaining ns-order risetime (or sharpened 100 ps-order). In addition, DSRD (and PSD) fabrication variabilities further complicate pulser design.

Solution Proposed: Develop further modeling capabilities in TCAD and SPICE for DSRD and DSRD-based inductive pulser circuit topologies to optimize DSRD and inductive pulser designs, especially for maximum peak power and minimum risetime, but also for low-jitter, reduced cooling, and compactness. Additionally, optimize pulser with PSD and pulse shaping head circuit.

Relevance to OSPRES Grant Objective: DSRD-based systems eliminate laser requirements necessary for PCSSs and are competitive in terms of thermal requirements and peak power. With sharpening, the DSRD-based systems can produce comparable risetimes. The SWaPC^2 cooling requirements of HPM cUAS systems can be solved with DSRD-based pulsed power systems, and low-jitter DSRD-based systems can be used for beam-steering in phased-arrays.

Risks, Payoffs, and Challenges: DSRD must be arrayed and staged to increase current since DSRD are limited in their ability to operate at high current densities. DSRD and PSD must also be stacked to operate at high voltages necessary for high peak power and maintain low risetimes. The stacking methods can damage dies and produce variable results in risetime and DSRD diffused doping profiles can be difficult to achieve and may require epitaxial methods. SPICE device models for DSRD are unavailable and must be developed, and questions remain about TCAD limitations for DSRD and PSD modeling.

5.1.2 Tasks and Milestones / Timeline / Status

(A) Milestone – Develop DSRD SPICE model within SmartSpice using the CMC diode model (built-in and Verilog-A).

1. Task – Develop accurate forward IV, reverse CV and reverse recovery testing (RRT) modeling in CMC diode model using either built-in (faster) or Verilog-A (customizable) models; On-going [APR-JUN 2022];

2. Task – Develop reverse IV and forward CV modeling and parameters in SmartSpice CMC diode models (built-in and/or Verilog-A); Preliminary exploration [MAY-JUL 2022];

3. Task – Develop 1x1 DSRD-based pulser recovery parameters within CMC diode model of SmartSpice (built-in or Verilog-A) and compare to RRT parameters; On-going [APR-JUL 2022];

(B) Milestone – Complete LTSPICE parameterization of the standard diode model for DSRD inventory.

1. Task – Finish Gen2.2 DSRD LTSPICE parameter extraction; On-going as received [APR-MAY 2022];

(C) Milestone – Develop automated fitting procedures for developed LTSPICE and/or SmartSpice DSRD models.

1. Task – Improve speed/accuracy/size of brute force fitting methods for LTSPICE and SmartSpice diode models; On-going [APR-JUN 2022];

2. Task – Improve python-based fitting methods for diode models used in LTSPICE and/or SmartSpice; On-going [APR-JUN 2022];

3. Task – Improve use of SmartSpice Optimizer for parameter fitting of diode models; On-going [APR-JUN 2022];

4. Task – Develop automated fitting procedures for Verilog-A diode models (CMC or custom); Preliminary exploration [APR-AUG 2022];

(D) Milestone – Convert manufacturer PSPICE and PSPICE/LTSPICE unencrypted device models into SmartSpice format for use in DSRD-based pulser simulation.

1. Task – Convert unencrypted PSPICE/LTSPICE Cree MOSFET model into SmartSpice format; On-going [APR-JUN 2022];

2. Task – Convert unencrypted Texas Instruments Gate Driver model from PSPICE into SmartSpice format; On-going [APR-JUN 2022];

(E) Milestone – Develop DSRD parameters for 2450 and new 371 semiconductor analyzer measurement data (forward IV and reverse IV).

1. Task – Develop standard diode LTSPICE 371A semiconductor analyzer measurement data parameters; On-going [APR-JUN 2022];

2. Task – Develop SmartSpice CMC (Verilog-A) 371A semiconductor analyzer measurement data parameters; On-going [APR-JUN 2022];

(F) Milestone – Determine performance of doping profiles within TCAD

1. Task – Determine TCAD performance of SOS, dynistor and thyristor doping profiles; Doping profiles not yet received; [?-? 2022];

2. Task – Determine TCAD performance of square root DSRD doping profiles; Not yet begun [? 2022];

3. Task – Determine TCAD performance of Gen3 manufacturer doping profiles; Not yet begun [? 2022];

4. Task – Determine recovery behavior of DSRD doping profiles within TCAD for development of custom Verilog-A CMC-based DSRD models; Not yet begun [?-? 2022];

5. Task – Determine effect of doping and defects on DSRD forward IV performance; Not yet begun [?-? 2022].

5.1.3 *Progress Made Since Last Report*

(D) Revised DSRD pulser circuit and United MOSFET model conversion into SmartSpice

A revised LTspice DSRD pulser circuit including a new United MOSFET model has been converted into SmartSpice. The new pulser circuit incorporated the sectionally fit forward IV data for the EG DSRD and produced improved pulser circuit output in terms of pulse shape and pre- and post-pulse features. The CMC DSRD model is in progress of refitting to the new forward IV data, needs some improvement to reverse CV fitting, and fitting recovery parameters to match new pulser data.

5.1.4 *Technical Results*

(D) Revised DSRD pulser circuit and United MOSFET model conversion into SmartSpice

The new DSRD pulser circuit (developed in Section 5.4) has been converted into SmartSpice format. A number of aspects of the circuit code had to be carefully converted (schematic to code version in LTspice, removal of braces, conversion of model syntax) and a few new elements (BJTs and multiple driving MOSFETS) had to be added. The main issue was conversion of the new United MOSFET model (UF3SC120009K4S) into SmartSpice (SmartSpice has no provided manufacturer models). The MOSFET model is actually a JFET in series with a MOSFET. Many aspects of the pulser circuit and model were examined and ultimately the tolerance of node voltages had to be reset from the default to a value which speeds convergence but does not force it (from 50 µV to 1 mV) for the pulser circuit to perform correctly in SmartSpice. Sometimes MOSFET models

can have convergence problems especially with models like this that are both preliminary and contain unusual features, such as the included JFET.

A couple of issues were discovered in the manufacturer provided model of the United MOSFET. The model is a PSPICE model which can work in LTspice. One issue was LTspice uses 1 mΩ of default series resistance on all inductors and this causes the PSPICE model in LTspice to not match the datasheet. Removing the default 1 mΩ inductor series resistance allows both the LTspice and SmartSpice converted United MOSFET models to match the datasheet. The only curve that did not match well for LTspice or SmartSpice United MOSFET models to the datasheet was the low voltage transfer capacitance (Crss). Figures of the United MOSFET curves compared between the datasheet and LTspice and SmartSpice models are not shown. The second issue did not immediately cause problems which was the inclusion of a JFET parameter in PSPICE that does not exist in LTspice and has the same name as an undocumented LTspice feature for area factor (did not appear to cause problems in the LTspice model and the parameter exists in the SmartSpice JFET model). The two issues were fixed in both the LTspice and SmartSpice models.

The new DSRD pulser circuit and converted United MOSFET model were simulated and resulted in reasonable pulser output as shown in Figure 5.1.1. The forward IV fit used must be refit for the DSRD used in experimental pulser tests and the new forward IV data collected for those DSRD, the reverse CV fit can be improved, and the recovery parameters must be refit to the new experimental pulse data. Even without refitting the pulser simulation produced reasonable output and details of circuit operation (DSRD and MOSFET currents).

Another issue that had to be corrected was for fitting CV in the SmartSpice model within the Verilog-A format/code. A discontinuity existed in the SmartSpice reverse CV fitting due to the CMC breakdown model. Rather than turning off the breakdown model, breakdown had to be set to the newly measured experimental breakdown data and this resulted in reverse CV without discontinuity for the SmartSpice CMC DSRD model.

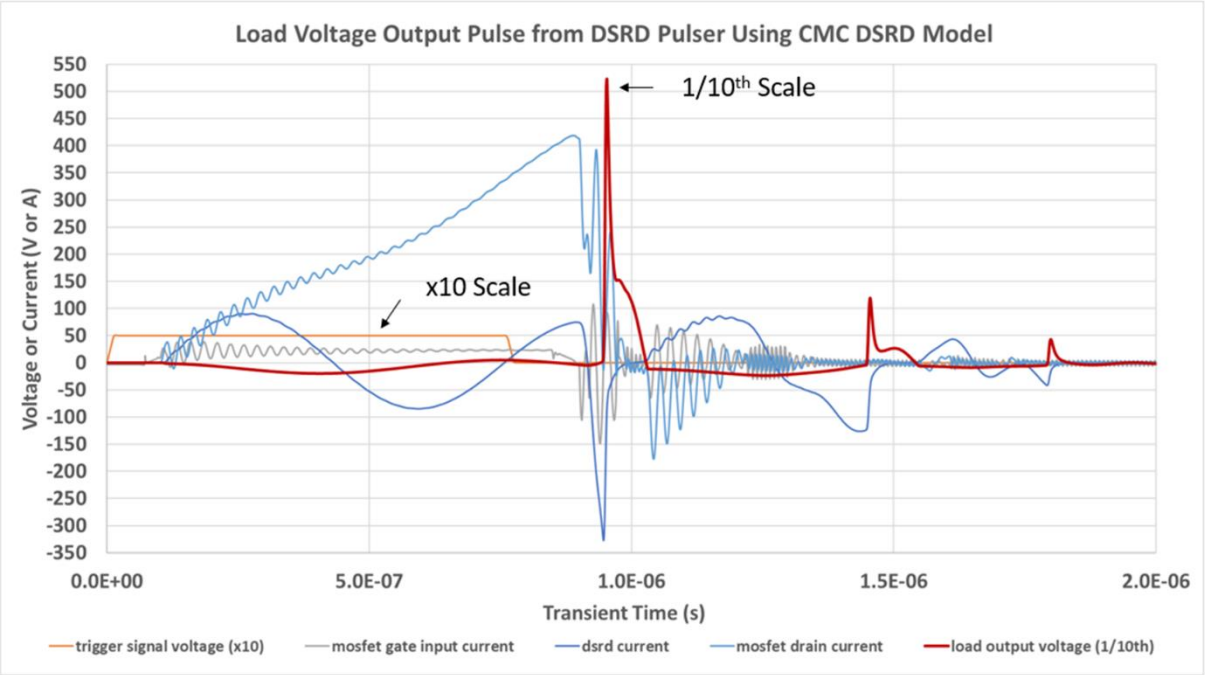

Figure 5.1.1. SmartSpice simulation using the CMC DSRD model within the latest pulser circuit designs showing the voltage output pulse at load (red, 1/10th scale) and other voltages and currents within the circuit for the DSRD and MOSFET.

With the improved fitting of IV/CV/recovery parameters the model can be verified and set to match individual pulse outputs. In Figure 5.1.2 is shown an outline for the progress of the CMC DSRD model from its current state to being used for predictive modeling and determination of the how DSRD parameters interact with the circuit components and devices used necessary for improving DSRD pulser designs.

Steps in DSRD Modeling

- Fit iv, cv, and experimental pulse data with the CMC DSRD model
- Analyze parameter fits to experimental pulse data for how or if CMC recovery parameters vary
- Change recovery model (could be simple fix or more involved literature study) to fit over range of prime voltages and trigger durations for (at least one) particular diode(s), initial CMC DSRD model developed
- Optimize components for particular diode fit and test in experiments (verify predictive capability of CMC DSRD model), refine model as necessary
- Understand through simulation how component values (and mosfet) vary for dsrd and its pulser performance→test experimentally by optimizing performance of a pulser (essentially for the interaction of dsrd with circuit components and devices within the design of circuit)
- Likely improve standard diode tests (iv, cv, rrt) and start pulse measurements in tandem with the above steps

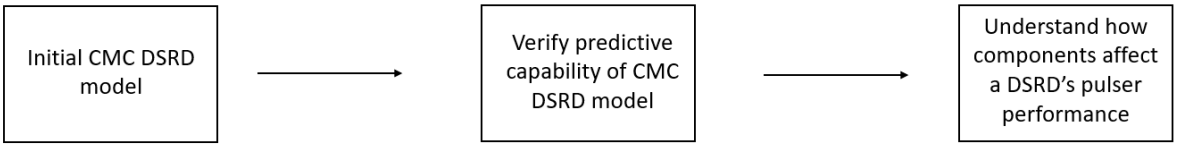

Figure 5.1.2. Roadmap for CMC DSRD model from current fitting in progress to use for predictive simulation and determining the interaction between DSRD, circuit and pulser performance.

5.1.5 *Summary of Significant Findings and Mission Impact*

(A) Development of DSRD Model Within SmartSpice CMC Diode Model

The SmartSpice circuit simulation software has been received in JAN 2022 and in FEB 2022 the Verilog-A CMC diode code was retrievable from the Si2 organization website. Development immediately began of the CMC diode model for DSRD modeling by producing forward IV, reverse CV and reverse recovery testing simulations and fitting to example DSRD in the inventory. Recovery parameter fitting within the 1x1 DSRD-based pulser has also begun. The capability of the CMC diode model for modeling DSRD can now be assessed. Any deficiencies in the CMC-DSRD model can be improved using the programmable Verilog-A code of the CMC diode model to include DSRD specific modeling equations based on theory, TCAD simulation, experiment and the literature. The Verilog-A code has been modified to allow different fitting parameters for different sections of the curve so that real, experimental forward IV can be accurately fit. Improved forward IV fitting in the Verilog-A CMC diode model will allow for improved pulser simulation.

(B) LTSPICE Standard Diode Model Parameter Development for DSRD Inventory

DSRD in the inventory of received diodes (legacy, EG and Gen2) have been fit for LTSPICE standard diode model parameters (for forward IV, reverse CV and reverse recovery testing) for use in LTSPICE DSRD-based pulser simulations and to provide another metric for the characterization of the DSRDs in comparison to pulser performance. Some details of the very low voltage and current forward IV have not been

fit but the fitting is still very close when visually inspected in non-log format. Reverse IV have not been fit in the standard diode model since it cannot capture the behavior and breakdown has not yet been measured, only estimated. Forward CV measurement are problematic and not fit mostly since the forward CV parameters in the standard diode model are used for recovery modeling. Various methods exist in LTSPICE to improve recovery parameter fitting but are either inadequate (Vp or carrier viscosity) or non-realistic (adjustment of reverse CV parameters) but have produced fits within 10% error for DSRD-based pulser performance. Gen2.2 experimental data has been received fitted within LTspice but there is high, variable series resistance in the Gen2.2 measurements that are being addressed with a new fixture and testing.

(C) Develop Automated Fitting Procedures for LTSPICE and SmartSpice

The current best method of fitting is using a brute force method of running LTSPICE or SmartSpice simulations sweeping over the desired parameter space. The brute force method can produce the most accurate fits but requires long simulation times and cannot be used to explore large parameter spaces easily (which is why more physically-based models using only measurable parameters is derisable). There is ultimately a limit to how quickly and accurately one can develop parameter sets. Another method is to program in the model equations into Python and use their curve fitting tools, however this method cannot incorporate circuit simulation and will therefore be less effective in producing accurate fits but is much faster in simulation time (can depend on how much parameter adjustments affect DSRD-based pulser performance on which method to use). The other fitting method is to use the built-in optimizer within SmartSpice, but the optimizer has not yet produced as good of fits consistently as the brute force method and will take some experience in using well.

(D) Conversion to SmartSpice of Manufacturer Device Models

Unfortunately, manufacturer device models are not openly available in SmartSpice only PSPICE and to some extent LTSPICE (usually converted from PSPICE). Therefore, the available PSPICE and PSPICE/LTSPICE models must be converted to the SmartSpice format, otherwise keeping the model the same. Note that encrypted models cannot be converted into SmartSpice, such models either have to be developed from scratch and either the datasheet or additional experimental tests used (or purchased from Silvaco for SmartSpice if available).

The unencrypted Cree MOSFET model has been converted into SmartSpice and tested within 1x1 DSRD-based pulser simulations and compared to LTSPICE simulations successfully. The unencrypted Texas Instruments gate driver model has also been converted into SmartSpice successfully. One issue with the driver model is it is intended for PSPICE but used often in online discussion in LTSPICE. However, close examination of the model shows that the model cannot perform correctly in all pin conditions in LTSPICE due to incorrect parameter types used in a voltage-controlled switch within the driver model. The voltage-controlled switch has been correctly implemented in the SmartSpice conversion and can be fixed for the LTSPICE version (Texas Instruments has not responded to inquires). Neither the MOSFET or gate driver models have been extensively diagnostically tested and compared to the datasheets which are often somewhat different to the free provided models (only so accurate).

The United MOSFET model (UF3SC120009K4S) had to be converted from PSPICE format to SmartSpice format. A couple model issues for the use of the model in LTspice were corrected, one which caused the model to not match the datasheet. The conversion to SmartSpice was successful and allowed simulation of the latest DSRD pulser circuit design with new MOSFETs using the CMC DSRD model to be performed successfully.

(E) IV Parameter Development for 371A Semiconductor Analyzer Measurement Data

A 371 semiconductor analyzer has been acquired and setup for forward IV testing with the potential for higher voltage/current reverse IV testing and breakdown. Initially concerns arose about the shape of the forward IV and whether temperature distortion was occurring at the higher voltages and current available with the 371 compared to the 6485 Keithley picoammeter. However, published power diode forward IV have been discovered showing similar forward IV at room temperature. 371 testing will proceed by testing more DSRD and subsequently using thermocouples and/or heat sinks. 371 higher voltage/current forward IV testing is necessary to characterize the DSRD in the diode models to perform correctly in the DSRD-based pulser simulations. How accurate the forward IV must be, has not been determined, as well as, to what extent individual diodes can be reliably distinguished in modeling. A new method for fitting forward IV has been implemented in the CMC Verilog-A diode modeling code that will allow for more accurate fitting of the 371 data for its full range. More rigorous forward IV testing has been implemented incorporating a number of modifications to the forward IV test fixture, cabling and testing methods (2- vs 4-wire) yielding forward IV with definite error bars. Also, lower current and voltage forward IV data are now taken with the Keithley 2450 sourcemeter which has a higher current limit (1 A) than the picoammeter (20 mA). Data collection of the DSRD inventory for forward IV using both the 2450 and 371 has begun and the curves align well for most DSRD. Breakdown testing has also been performed for Gen2 and EG DSRD showing 40% yield for higher breakdown devices needed for DSRD stacking and DSRD pulser testing.

(F) TCAD-Based Doping Profile Performance Evaluation

Many DSRD TCAD simulation studies have been performed assessing the doping profiles used for the DSRD manufactured by SPT and in stock (this summary includes work from the past six months). The TCAD modeling has been temporarily on hold as effort is focused toward developing an accurate SPICE DSRD model due to the unavailability of manufacturer device models for MOSFETs and gate drivers within TCAD. A MOSFET model was developed for the Cree MOSFET for use within TCAD but still had some differences when used in pulser simulations, so the development of the DSRD SPICE model was prioritized so that manufacturer models (for MOSFETs and drivers) could be used.

Doping profiles are forthcoming for various SOS, dynistor and thyristor devices and TCAD will be used to assess their performance. Some interest has been expressed in assessing square-root doping profiles for DSRD. Gen3 doping profiles from the manufacturer have yet to be assessed within TCAD for performance differences with the requested doping profiles. As well, the recovery models within the CMC diode model are themselves based on PIN diode TCAD simulations and TCAD can perform DSRD doping profile specific simulations to determine model equations and parameters. Additionally, the forward IV

behavior of our DSRD can be modeled as seen in the 371A semiconductor analyzer mesaurements. TCAD modeling will continue to be of use in device modeling since it is the only way to assess doping profiles.

5.2 Pioneering Drift-Step Recovery Diode Processing and Manufacturing

(Alex Usenko)

Detailed reporting for this section is on hold. A summary report of work completed under OSPRES Grant will be provided in a future MSR, and more streamlined reporting may be provided as appropriate. Please see the May 2022 MSR for the most recent progress update.

5.3 Characterization of SOS Diode Performance through DOE Augmentation

(Joseph Reeve-Barker, Jay Eifler & Megan Hyde)

5.3.1 *Problem Statement, Approach, and Context*

Primary Problem: Drift step recovery diodes (DSRDs) are planar diodes that are capable of nanosecond, high-frequency (10–10^3 kHz) pulses [1] with applications as opening switches in inductive energy storage (IES) pulse generation circuits. There is not a clear understanding of the effects DSRD parameters have on overall IES pulser performance. The purpose of this project is to tie the DSRD parameters to its tailored performance requirements.

Solution Space: Leveraging both design of experiment (DOE) and machine learning (ML) capabilities, we will develop a methodology of characterizing and optimizing DSRDs in order to provide fabrication recommendations in the context of application targets.

***Sub-Problem 1*:** We do not yet understand how diode parameters are tied to diode performance.

Sub-Problem 2: There is no standardized method for correlating the diode key performance indicators (KPIs) to the IES pulser generator performance.

Sub-Problem 3: The number of possible inputs for the DOE is expected to be too large, so ML will need to be leveraged in order to guide decision-making processes.

State-of-the-Art (SOTA): Standard diode measurements include curve tracers for forward and reverse IV, impedance spectroscopy for forward and reverse CV, and function generators or, for example, the Avtech pulser for reverse recovery with high voltage and/or high current when necessary. These measurements are used to generate commonly available datasheets for COTS diodes. These standard diode measurements can then be correlated to pulser performance using traditional data analytics.

Deficiency in the SOTA: The standard diode measurements and datasheets do not include pulser performance necessary to evaluate DSRDs. The datasets generated with doping profile assessment (for example spreading resistance profiling), standard diode

measurements and pulser performance are too large and complex to leverage traditional data analytics and will benefit from machine learning techniques.

Solution Proposed: Develop a holistic evaluation network for DSRD characterization. This network will include a DOE that will be a continuously evolving model as diode parameters are correlated to pulser performances. Augmenting the DOE will ensure that the model will remain relevant throughout this study as more discoveries are made. Machine learning will be used as the primary decision-making tool for augmenting the DOE. Once the network is established, it will be used to outline the optimal parameters for stacks of DSRDs within an IES pulse generator.

Relevance to OSPRES Grant Objective: Bridging the gap between the theoretical and physical performance of DSRDs enables closing the gap between a low fidelity TRL3 breadboard pulse generation system, and one which is at a high fidelity TRL4 prototype level. At the TRL4 level, the DSRD-IES pulse generator system would be sufficient to replace the costly laser-based Si-PCSS HPM generator without compromise to scalability required to support the Naval afloat mission.

Risks, Payoffs, and Challenges:

Challenges: Traditional predictive analytics will be difficult to correlate with the augmented DOE due to the large volume of data. Machine learning is expected to assist with decision making processes for the DOE, but only if ideal diode characteristics have been established and good data have been used to train the machine learning model.

5.3.2 Tasks and Milestones / Timeline / Status

(A) Milestone – Establish preliminary DOE and standard operating procedure (SOP) for identifying KPIs of DSRDs [*estimated completion by MAR22*].

1. Task – Ascertain current KPIs used to optimize diodes simulated, manufactured, and utilized within the IES pulse generating circuit [completed AUG21];
2. Task – Construct preliminary DOE to acquire data on all KPIs based on Task 1 [*completed FEB22*];
3. Task – Leverage existing Python scripts to process legacy DSRD KPI data [*completed SEP21*];
4. Task – Develop new and review existing SOPs for experimental testing apparatuses used to evaluate individual KPIs and measure their performance [*completed OCT21*];
5. Task – Identify gaps/deficiencies in legacy KPI data, evaluate existing theoretical relationships to bridge gap and minimize DOE if possible [*completed OCT21*];
6. Task – Using SOPs developed in Task 4, acquire experimental data from legacy DSRDs, refine SOP(s), and assess repeatability and reproducibility [*In progress*: *SEP21–MAR22*];

(B) Milestone – Evaluate DSRD performance using the developed SOPs and facilitated by the preliminary DOE [*estimated completion JUL22*].

1. Task – Acquire data on newly manufactured 2nd generation epitaxial DSRDs from Section 5.2 using refined SOPs from Milestone A [*completed JAN22*];
2. Task – Evaluate the precision and power of the DOE [*In progress*: *MAR22–JUL22:*];
3. Task – Develop a DSRD selection guide for the pulser circuit based on the static DC test measurements *[In progress: MAR22–MAY22];*
4. Task – Correlate the static DC test measurements to the performances of the IES pulser circuits and to fabrication procedures [*MAR22–JUN22];*
5. Task – Begin training machine learning model with DSRD data to determine correlations between static DC and pulser testing results [*MAY22–JUL22*];
6. Task – Acquire data on newly manufactured 3rd generation epitaxial DSRDs from Section 5.2 using refined SOPs from Milestone A [*JUL22–SEP22*];

(C) Milestone –DSRD diode network evaluation [*on hold until Milestone B is completed*].

1. Task – Refine Python script to incorporate new correlations based on findings from Milestones A&B [*Est. Summer22*];
2. Task – Amend ML training model with data acquired on new DSRDs (as characterized by Sections 5.1–5.2) to investigate statistical correlation of diode performance [*Est. Summer22*];
3. Task – Work with TCAD simulation team to address discrepancies between the DSRD performance obtained experimentally, and that achieved within simulations [*Est. Summer22*];
4. Task – Collaborate with DSRD manufacturing team to address discrepancies between the DSRD characteristics evaluated experimentally, and that desired by manufacturing process [*Est. Summer22*];
5. Task – Investigate relationships between statistical significance of individual diode KPIs to the peak performance of the IES pulser with the pulse generator team. [*Est. Summer22*];
6. Task – Incorporate findings from Tasks 1–5 into ML model, pinpoint KPI correlations of interest, and provide recommendations to IES sub-teams accordingly [*Est. Summer22*];

(D) Milestone – DSRD diode network evaluation [*on hold until Milestone C is completed*].

1. Task – Augment DOE network to streamline diode evaluation and identify checkpoints/gaps within simulation, manufacturing, and circuit development process to ensure optimal diodes are selected and utilized to produce robust high-fidelity IES pulse generator prototypes [*Est. Fall22*].

5.3.3 *Progress Made Since Last Report*

(A.6) DSRD Standard Diode Testing

Rigorous Forward IV Testing and Breakdown Testing

Forward IV testing, including Keithley 2450 and Tektronik 371 measurements, has been completed for EG and Gen2 DSRD. In addition, Gen2.2 DSRD have been tested for breakdown. The breakdown, series resistance, and forward voltage drop (at 50 A for power diodes) have been analyzed for the best performing DSRD. Using this data, DSRD were selected that allowed for peak voltage of 9 kV to be achieved in the latest DSRD pulser (see Section 5.4).

5.3.4 *Technical Results*

(A.6) DSRD Standard Diode Testing

Rigorous Forward IV Testing and Breakdown Testing

Forward IV experimental data were collected for EG and Gen2 DSRD using both the Keithley 2450 Sourcemeter and the Tektronik 371 semiconductor analyzer. Two measurement systems were used to cover the full range of voltages and currents necessary to characterize the DSRD operation within the DSRD pulser for both correlation of experimental data and SPICE model parameter development. The data analysis of forward IV and breakdown data allowed for the selection of the best performing DSRD within the DSRD pulser and the achievement of 9 kV load output.

In Figure 5.3.1 are shown the forward IV for EG DSRD with both the 2450 and 371 data shown (the 2450 data is difficult to see). For EG the overlap of data between the 2450 and 371 aligned or matched ~60% of the time (not shown). For this reason, there are some different approaches to fitting this data in the SPICE models. One approach is to exclude the overlapping data region and measurement low and high end ranges as less accurate to be fit to. The other approach is to fit directly to both datasets and this will automatically smooth the data between the 2450 and 371 measurements (the second approach is currently being used). Both the EG1500 (open circles) and EG1600 (closed circles) are included in the figure and are distributed similarly with the EG1600 having a few higher series resistance cases than the EG1500 data.

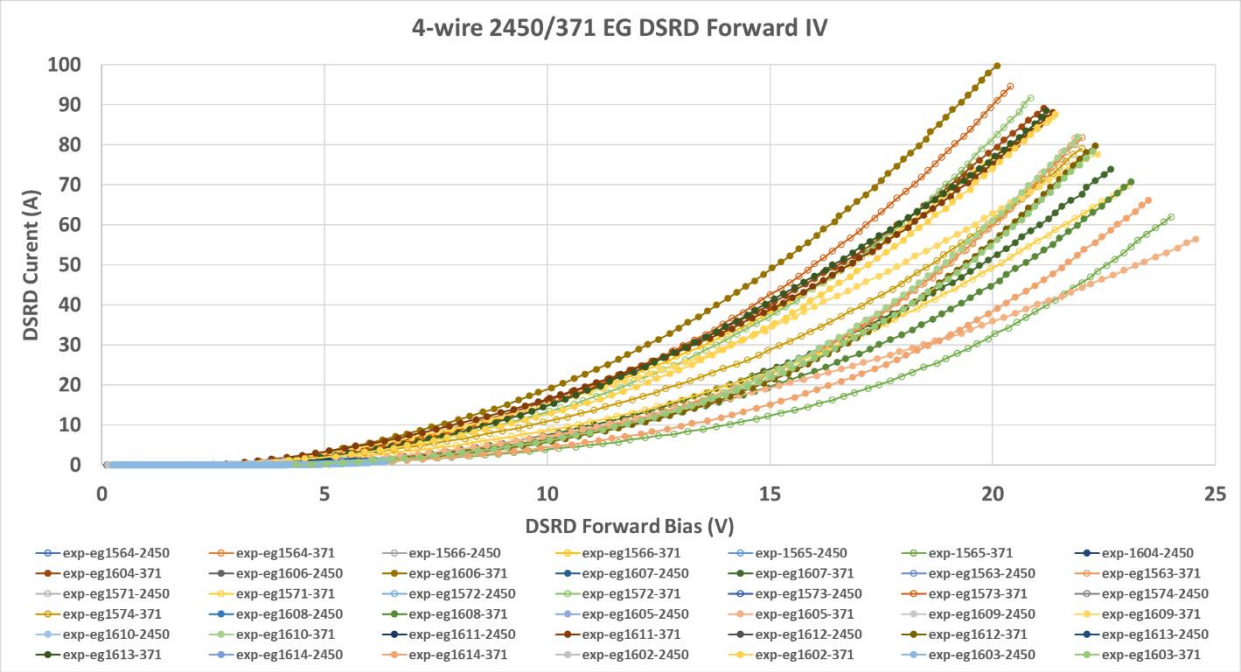

Figure 5.3.1. EG DSRD Keithley 2450 and 371 Tektronik forward IV curves.

In Figure 5.3.2 are shown the forward IV data for Gen2 DSRD with both the 2450 and 371 data shown. The Gen2 DSRD data have a different forward IV shape than the EG series DSRD data. The Gen2 forward IV data are of the conventional power diode shape, whereas the sub-threshold region of the EG DSRD shows higher current and there is a lack of a clear linear region for the EG DSRD. The Gen2 DSRD have a clear linear region where the resistance of the diode is not changing and can represent the minimum on-state resistance which is approximately the added series resistance of the DSRD into the forward IV fixture (primarily a combination of pressed contacts and metal-silicon contact resistance). Where the EG DSRD required a sectional fit, the Gen2 can be fit with a regular diode model of the DC current.

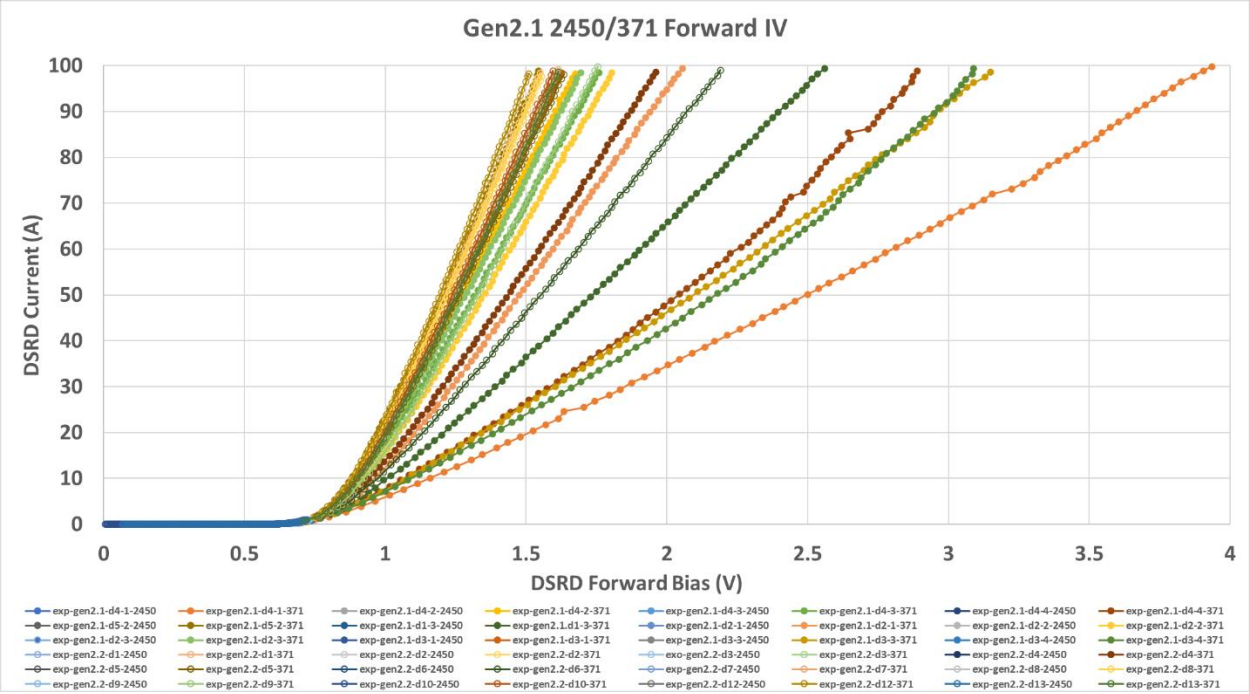

Figure 5.3.2. Gen2 DSRD Keithley 2450 and 371 Tektronik forward IV curves.

The Gen2.1 DSRD (closed circles) and Gen2.2 DSRD (open circles) are both shown with the Gen2.1 showing some higher series resistance cases, otherwise the distribution of forward IV being similar. It should be noted that the measured forward IV data are single measurements. A repeated measurement of forward IV in the 371 has been done earlier (May 2022 OSPRES grant report) showing the measurement error (standard deviation) associated with replacing the DSRD into the fixture (as with actual measurement data of different DSRD) is about ±2 A. The error associated with a single measurement should double this standard deviation implying some DSRD forward IV are distinguishable and others not.

The analysis of the forward IV data was completed for series resistance (RS) and forward voltage drop at 50 A (conventional for power diodes, should be normalized with device area for comparing devices of different areas and voltage normalized for DSRD of different stack heights). Included in the analysis are the breakdown data, which are critical in selecting DSRD for peak voltage performance along with the forward IV RS and drop.

In Figure 5.3.3 is shown the RS/drop product vs breakdown voltage. The RS/drop product is used to assess the effect of the forward IV parameters (RS and drop) on a single axis and breakdown on a single axis (RS/drop product not necessary for Gen2 since there is a large linear region). The best performing diodes are sectioned off and labeled and were selected to achieve the experimental 9 kV peak voltage in the DSRD pulser along with worst performers to contrast the effect. A more in-depth analysis correlating standard diode measurement and pulse data is forthcoming.

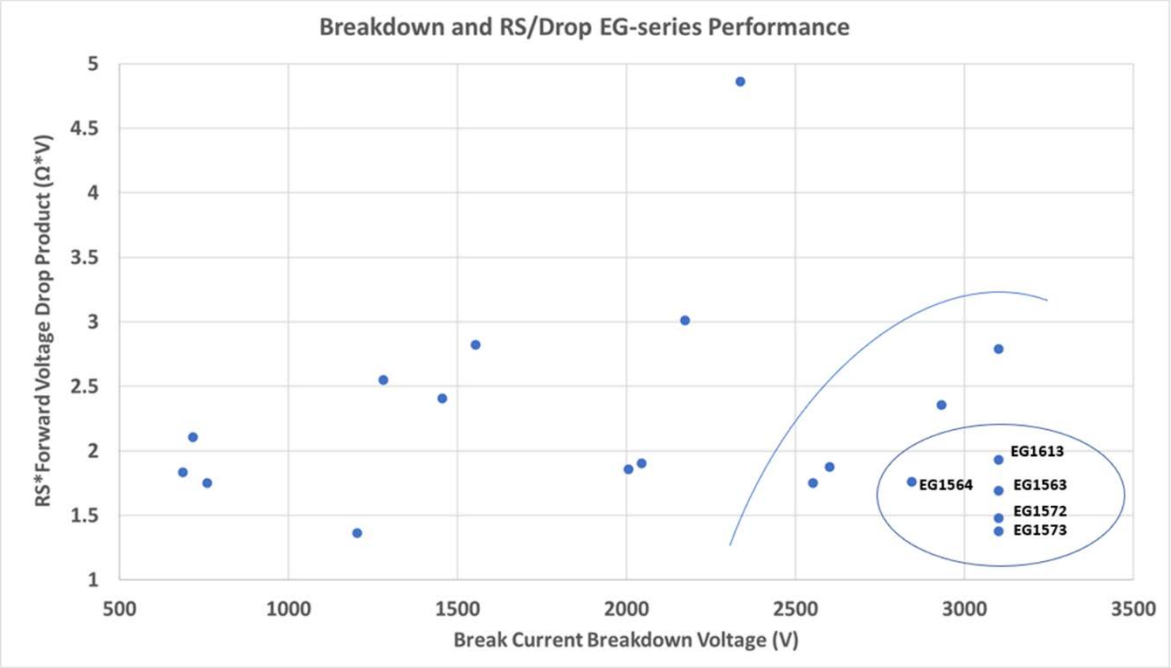

Figure 5.3.3. RS/drop product vs breakdown voltage for EG DSRD with best performers sectioned off and labeled.

The Gen2 DSRD were also analyzed for best performers (SPT 21-stack Gen2 DSRD are to be delivered within a month) although no pulser data has been collected since the pulsers are not designed for 1-stack DSRD and press-stacked Gen2 have high series resistance. In Figure 5.3.4 is shown the RS vs breakdown analysis. Only RS was used for Gen2 since the curves go linear at sufficiently high current and voltage. The RS vs breakdown analysis can be used for selecting best performers of Gen2 in DSRD pulsers. The 21-stack Gen2 likely cannot be tested for RS, drop or breakdown due to the high voltage requirements, so DSRD characterization for pulser performance should be done before stacking.

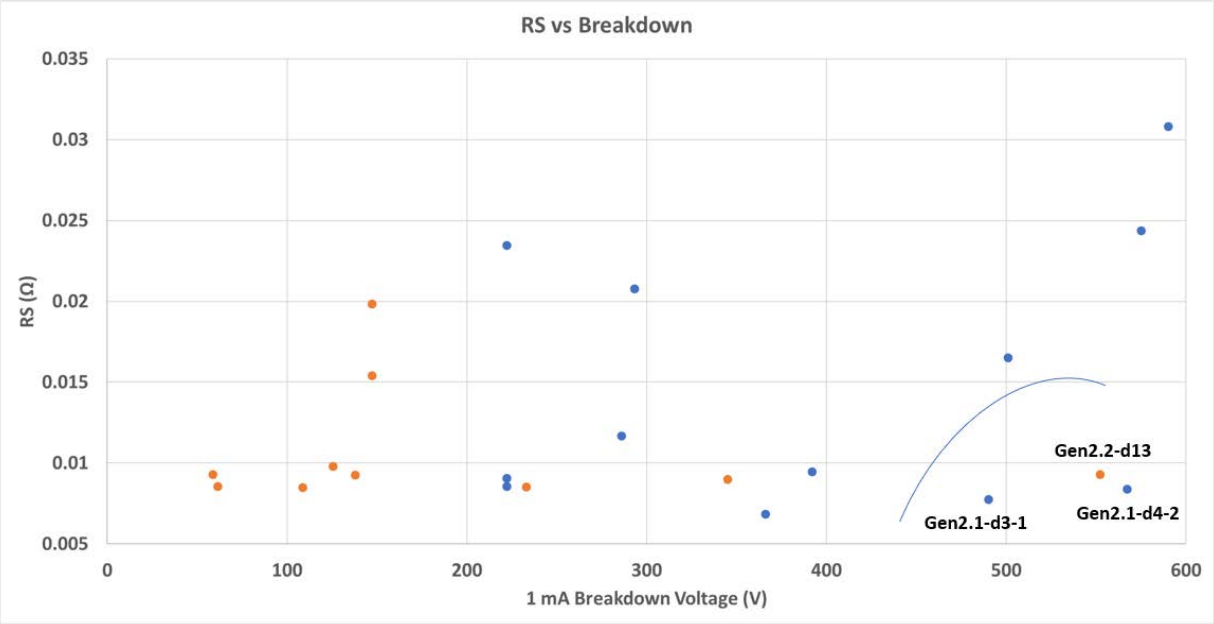

Figure 5.3.4. RS vs breakdown voltage for Gen2 DSRD with best performers sectioned off and labeled.

A more in-depth measurement and analysis of the breakdown is likely required to assess breakdown using another method than the 1 mA breakdown current convention (should be dependent on diode area). The method chosen is to determine significant current increase for small voltage steps (rather than a conventional hi-pot test to 1 mA), but the experimental data must be more carefully collected. Preliminary analysis using the current increase method shows similar results but different breakdown voltages and currents. Ultimately, breakdown must be studied in the pulser and correlated to static breakdown tests.

5.3.5 *Summary of Significant Findings and Mission Impact*

(A.1) Several KPIs have been identified that tie the experimental diode test results to SPICE model simulation parameters. The first KPI is the forward current-voltage (the voltage reading at 10 mA) that is linked to the following SPICE parameters: saturation current, ohmic resistance, emission coefficient, and the forward knee voltage. From the impedance analyzer, the capacitance-voltage measurement is tied to the zero bias junction capacitance and the bottom junction grading coefficient. Both the forward voltage-current and the capacitance-voltage KPIs can be further tied to the SPICE simulation circuit peak voltage performance. The reverse current-voltage (current at -200 V) is linked to the breakdown voltage SPICE parameter. The reverse recovery time measurements, such as the charge storage time and the transition time, are tied to the transit time SPICE parameter and to the full width at half maximum of the pulse signal. Several of these KPIs are not yet associated with specific circuit performances but will require further analysis as outlined in B.4.

(A.2) A preliminary DOE has been developed. The first 6 out of 16 rounds are currently being processed per (A.6).

(A.6) It was found that the test fixture for the picoammeter was causing large variations in the current-voltage measurements due to inconsistent pressure application to the diode. The variation was significantly larger on the Gen2 diodes since they are approximately one-third the height of the 7-stack diodes. A new 3D printed fixture with the ability to apply consistent pressure is expected to drastically reduce the contact resistances and variability that have been introduced to the measurements. New forward IV measurements have produced an averaged measurement with standard deviation error bars. Breakdown testing has shown ~40% of diodes hold at least 500 V per diode in stack. CV testing for series resistance has shown high series resistance associated with the CV test fixture and CV testing in the forward IV fixture may show lower series resistance. Forward IV from the Keithley 2450 and Tektronik 371 have been combined to produce measurements over a larger range of current and voltage necessary to model the DSRD in DSRD-based pulsers. The DSRD EG and Gen2 inventory has been tested for forward IV using both the 2450 and 371 along with breakdown testing in the 371. The data has been successfully used to pick best performing DSRD for the DSRD pulser with experimental 9 kV peak voltage resulting.

(B.1) In A.6, it was discovered that the test fixture was the cause of significant variation within the test results, particularly with the Gen2 diodes. Several diodes are scheduled for repeat measurements to determine if all diodes need to be re-tested, which would affect the “completed” status of this milestone.

5.4 DSRD-Based Pulsed Power Source Systematic Topological Optimization

(Shailesh Dhungana & Gyanendra Bhattarai)

5.4.1 *Problem Statement, Approach, and Context*

***Primary Problem*:** Inductive energy storage (IES) and release pulse generators that use drift-step recovery diodes (DSRDs) can be used as the fundamental units of all-solid-state high-power microwave (HPM) systems. The output from DSRD-based pulsers can then be fed into sub-nanosecond pulse sharpeners to achieve ultra-short high-voltage pulses. While DSRD-based pulsers can theoretically achieve the targeted 1's of GW in 1's of ns, their circuits are not topologically optimized to achieve high voltage gain (peak pulse voltage/prime source voltage), thus requiring large and heavy high-voltage (multiple kV) prime power supplies to achieve the required 100's of kV pulses. They also necessitate liquid-based cooling systems to dissipate the excess heat they generate during operation, further adding weight and rendering them impractical for Navy afloat missions.

***Solution Space*:** Systematically develop optimum circuit topology to maximize the voltage gain, and thus the peak voltage, peak power, and volumetric power density of DSRD-based HPM systems. Minimize the heat loss to be able to air cool by increasing energy efficiency through optimization of circuit elements without sacrificing the desired nanosecond risetime of the pulses generated. Air-cooled IES pulse generators using optimum DSRD stacking can remove the need for photo-triggered switches and their laser sub-systems. They are ideal for triggering sub-nanosecond rise-time sharpeners (SAS, D-NLTL, etc.), reducing overall cost, volume, and weight.

***Sub-Problem*:** DSRDs are not domestically available COTs components, but rather manufactured in small-batch quantities, with statistically significant variations in their performance parameters. In addition, our current SPICE models of these diodes may not be accurate due to unknown device parameters such as carrier distribution, carrier lifetime and the limiting current that we can pump without affecting the diode recovery property (see section 5.1 and 5.3) during high-voltage transients. These issues may lead to an inaccurate simulation model of the pulser and discrepancies between simulated and experimental results.

***State-of-the-Art (SOTA)*:** Air-cooled DSRD-based pulsers (equivalent in size to the pulse generators developed for this effort, i.e., ~0.01-m^3, ~2-kg) can achieve <20 kV, 1–2 ns risetime, and <4 ns FWHM across a 50 Ω load with a PRF of <15 kHz in burst mode. Available literature on IES pulse generators only describes a few circuit configurations, and there is a lack of comprehensive investigation of circuit topologies and optimization to achieve maximum gain and efficiency and reduce thermal load. Additionally, these pulsers are expensive and are not available within the United States.

***Solution Proposed*:** Develop different DSRD circuit topologies implementing series and parallel combinations of DSRDs (to increase reverse breakdown voltage and diode current, respectively) to minimize circuit components, such as inductors, capacitors, and switches. Systematically identify the best circuit topology and optimize the circuit components through physics-based DSRD pulser circuit theory and SPICE simulation to

maximize voltage gain and efficiency while minimizing the prime source voltage and thermal load.

Risks, Payoffs, and Challenges:

***Risks*:** All-solid-state DSRD-based IES pulsers require many other electronic components. Most importantly, the current pumping capability of available MOSFETs/electronic switches is limited, which may make maximizing the output voltage impossible even though the DSRDs are capable of higher current and output voltages.

***Payoffs*:** Being able to simulate and fabricate DSRD-based pulsers using physics-based pulser theory, partnered with US-based DSRD manufacturers, will enable a comprehensive domestic ability to optimize, produce, and evaluate these nanosecond pulsers.

***Challenges*:** Domestically manufactured (U.S.-based) DSRDs, which possess sub-optimal doping profiles, may lead to sub-optimal pulse generators. Accurate spice modeling of the diodes could be affected by expected wide variability in the diode characteristics or unavailability of advanced device characterization techniques. Determining the superlative ratio of design/development (through numerical analysis) to the effort put towards experimental testing/evaluation of the DSRD pulser is challenging due to the novelty of the approach. Extending the theory of single (1×1) pulse generator to cascaded (M×N) generator to increase the output will be very complex and may require significant time and computing power.

5.4.2 Tasks and Milestones / Timeline / Status

(A) Milestone – Develop theory of DSRD pulse generator to facilitate optimization of 1×1 pulse generator [***Completed JAN22***]

(B) Milestone – Extend the theory developed in Milestone A to facilitate optimization of M×N pulse generator [**JAN–MAY22** / ***Ongoing***].

(C) Milestone – Construct/demonstrate a DSRD-based 1x1 pulse generator prototype based on theory developed in milestone (A) and obtain performance data for multiple combinations of diode stacks [**JAN–JUN22 / *Ongoing***].

(D) Milestone – Construct/demonstrate a DSRD-based 4×2 IES pulse generator prototype capable of producing $\geq$12 kV peak voltage, $\leq$1 ns risetime, $\leq$5 ns FWHM, $\geq$3 MW peak-power, $\geq$100 kHz PRF, $\geq$1,000 shots-per-burst, $\geq$500 number of bursts [*On hold*].

(E) Milestone – Develop waveform inverter which, when combined with the pulser from Milestone C, enables a balanced differential waveform output with >90% inverted signal fidelity. [***Completed DEC21***].

(F) Milestone – Construct/demonstrate a M×N pulse generator prototype capable of producing $\geq$20 kV peak voltage, $\leq$1 ns risetime, $\leq$2 ns FWHM, $\geq$8 MW peak-power, $\geq$100 kHz PRF, and $\geq 2\sigma_{Vpeak}$, which operates in continuous-burst mode as a viable candidate for OSPRES Contract source alternative [*on hold until Milestones B, D, & E are completed*].

5.4.3 *Progress Made Since Last Report*

(B) We have been developing the theory of a 1×2 DSRD pulser and generalizing it to an M×N pulser.

(C) A modular driver circuit for optimized MOSFET operation, that was designed during the June reporting period and needed a specific bipolar junction transistor from the United Kingdom, has been populated and tested, and is capable of driving four parallel MOSFETs to increase forward pumping current through the diodes. A 1×1 DSRD pulser utilizing the modular driver circuit has been populated and tested. An output voltage of 9.2 kV with a risetime of 5 ns has been achieved with a prime voltage of 170 V and a trigger length of 750 ns.

5.4.4 *Technical Results*

(C) 1×1 DSRD Pulser Fabrication and Testing

i. Inductor Fabrication and Characterization

The performance of a solenoid air-core inductor is affected immensely by parasitics such as self-capacitance and winding resistance [1]–[7]. The non-ideal behavior of such inductors can be analyzed using a simple model, referred to as the lumped-parameter model, shown in Figure 5.4.1. In the lumped-parameter model, an inductor has the following parasitics: (1) the total inductance L_s, which is the sum of the inductances of the core and the windings of the inductor, (2) the series resistance R_s, which is the resistance of the wire that makes up the solenoid, and (3) the self-capacitance C_p, which is the series combination of the capacitances between the adjacent turns [1], [6]–[8]. From a practical standpoint, the parasitics act as if the resistance is in series with the inductance while the capacitor is in parallel with the series combination of the two; hence the subscripts "*s*" and "*p*" used to represent this behavior.

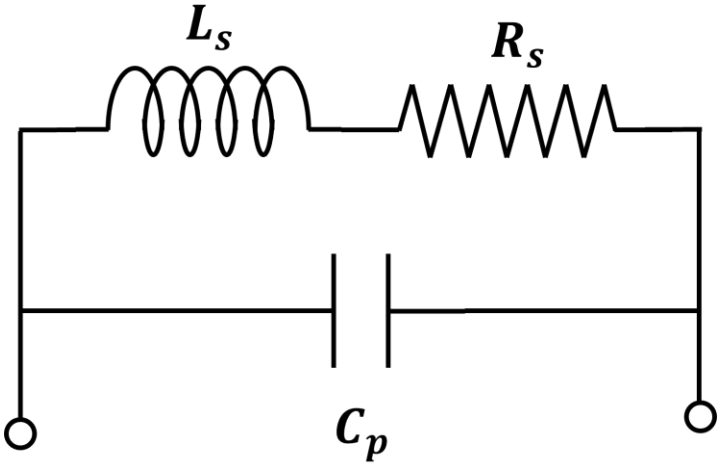

Figure 5.4.1. Lumped-parameter inductor model.

Design/Construction of Inductors

We used Coil64 [9], an open-source application, to obtain the number of turns required to construct an inductor of a desired inductance using a wire of known diameter. The application also estimates the resistance, self-capacitance, reactance, and self-resonant frequency of the solenoid. Based on the results of these calculations, we fabricated some inductors with copper wires insulated with polyamide.

Characterization of Inductors

The inductors were characterized using an Agilent 4294A Impedance Analyzer. A custom-built test fixture was used as shown in Figure 5.4.2. Preliminary measurements show that there is a slight discrepancy between the desired and the measured inductance values. There could be three reasons behind this discrepancy: (1) the limitation of the Coil64 application, (2) the errors introduced due to noise while measuring low impedances, (3) the errors introduced in the measurement during fixture compensation (can be significant for custom-built test fixtures and especially measuring low inductances; ≤50 μH). It has been well-established in the literature that the inductance of a solenoid is a function of the operating frequency. Similarly, the resistance and self-capacitance also depend on the operating frequency [4], [10]–[14]. However, the Coil64 program does not consider this and gives the same value of inductance regardless of the operating frequency. Consequently, we can expect to obtain lower values of inductance than the calculated value.

In order to better characterize the inductors, we are working on ways to obtain better results for both the calculated as well as the measured inductance. For calculated inductance, we are working on a Python program that calculates the inductance as a function of frequency for a given inductor. The program will use various equations and approximation found in the literature [6]–[8], [12]–[16]. Simultaneously, we are also in the process of refining the experimental set-up, which involves measuring a standard inductor and comparing the data with that provided by the manufacturer and upgrading the fixture accordingly until a good agreement is reached between the two values. Once we verify that our set-up is working properly, we will measure the inductors that we have built. The values will be cross-checked with the calculated values.

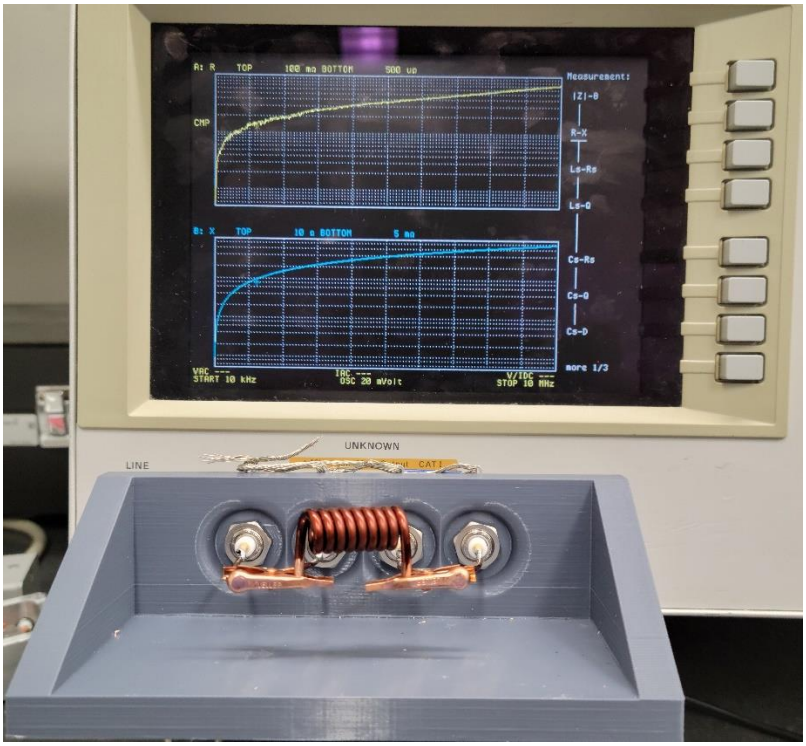

Figure 5.4.2. Experimental set-up to characterize inductor using a custom-built fixture and an Agilent 4294A Impedance Analyzer.

ii. Pulser Fabrication and Testing

A pulser circuit board consisting of a re-designed MOSFET driver to drive four MOSFETs in parallel and capable of producing 10 kV output pulses has been populated (Figure 5.4.3). Along with the increased target output voltage, the circuit components have been updated to increase the pulse repetition rate of up to 100 kHz. The pulser circuit has been designed using three 7-stack DSRDs for a trigger length of 500 ns and prime source of 120 V. However, we were able to achieve the highest output voltage of 9.2 kV with a 10–90% risetime of 9 ns (20–90% risetime of 5 ns) for a prime source of 140 V and a trigger length of 750 ns.

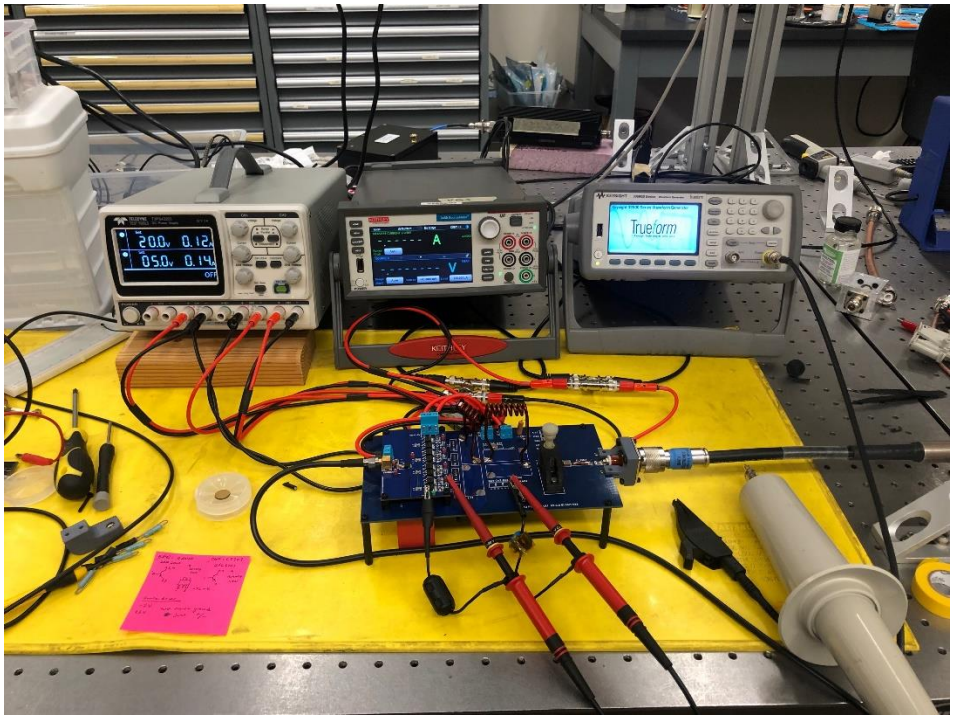

Figure 5.4.3. Experimental setup of 1×1 DSRD pulser designed to produce 10 kV output pulse.

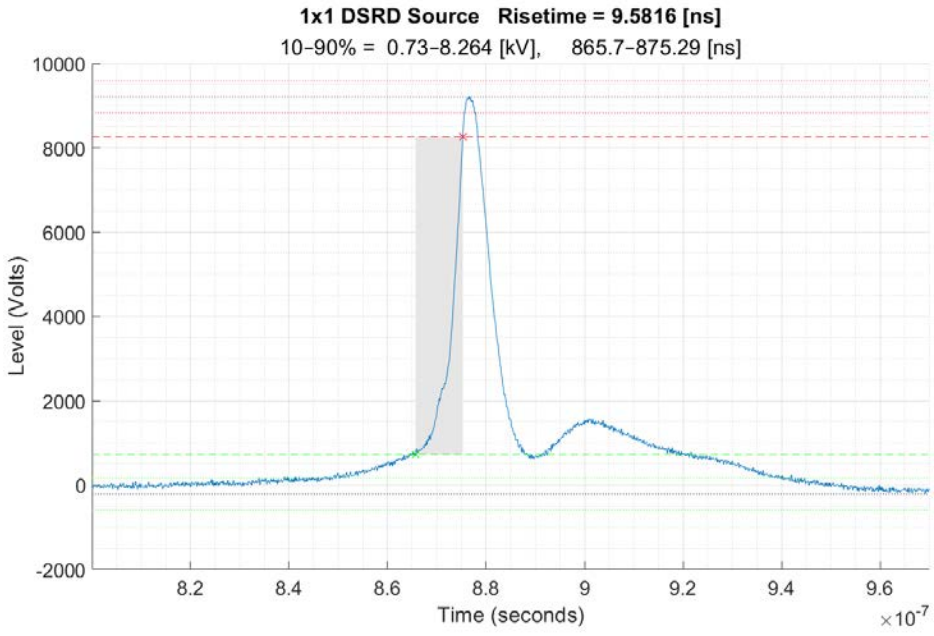

Figure 5.4.4. Output voltage pulse from a 1×1 DSRD pulser using EG1571, EG1572, and EG1573 7-stack diodes designed to produce 10 kV output.

Figure 5.4.4. shows the output pulse voltage from the newly built DSRD pulser using three 7-stack diodes (EG1571, EG1572, and EG1573). The output obtained is the highest peak voltage obtained with a single 1×1 DSRD pulser fabricated in this study and is very close to the target output. However, there is still a discrepancy between the simulated and experimental trigger length, which might be because of the inaccurate on-state resistance of the diodes measured as higher on-state resistance can significantly increase the forward pumping time due to critical damping of the LCR circuit.

5.4.5 *Summary of Significant Findings and Mission Impact*

(B) A systematic optimization of a 1×1 pulse generator based on the theory covered in the DEC2021 MSR reporting period was presented. In this reporting period, we have presented an optimization sequence considering the circuit limitations. Based on the previous measurements and simulations, we hypothesized that the lowered output voltage obtained from the previous pulsers could be due to higher diode ON-state series resistance than the value considered for simulation. A proposed working principle for a two-stage DSRD pulser has been described in the MAY2022 MSR reporting period, however, with certain outstanding questions that may inform the efficacy of multi-stage DSRD pulsers. A new approach for stacking multiple 1×1 pulsers in parallel to increase the output voltage while keeping the MOSFET current and voltage within safe operating limit has been proposed.

(C) Using the 28-stack pulser, maximum peak outputs of 6.7 and 7.5 kV are obtained for a trigger length of 700 ns using a prime source voltage of 120 and 170 V. A newly designed and fabricated pulser with four MOSFETs in parallel achieved an output of 9.2 kV using three 7-stack diodes for a prime source voltage of 140 V and a trigger length of 750 ns. The lower-than-expected output (10 kV) is believed to be due to inaccurate values of custom-built inductors and inaccurate diode on-state resistance. Based on the DSRD pulser output using a single 7-stack diode, the reverse breakdown voltage of the EG1600 series diodes is estimated to be ~650 V. Measurement of circuit voltages at different nodes confirms the circuit performance matching the SPICE simulation. Obtained lower output voltages indicates requirement of more accurate DSRD SPICE Model which takes account of forward diode series resistance, carrier distribution and recombination during high voltage transients.

(D)

Table 5.4.2. Comparison of DSRD-based IES Pulse Generator Performance.

KPM	Units	MIDE - V1	MIDE - V2	MIDE – V3	MIDE – V4	Kesar *et al.*	MI-PPM0731
		Previous	Previous	Previous	Current	SOTA	COTS
V_{supply}	V	225	180	120	140	300	160
T_{ON}	ns	100	340	700	750	?	200
V_{peak}	kV	5.59	**7.35**	**6.7**	**9.2**	5	6.3
Gain	V/V	24.8	**40.8**	**55.8**	**65.7**	16.7	39.4
$\tau_{rise,20\text{-}90\%}$	ns	1.2	1.1	3.1	5.0	1.96	0.12
dV/dτ	kV/ns	4.66	6.44	2.16	-	2.55	**52.50**
FWHM	ns	2	5.48	6.90	7.8	2.27	0.35
PW	ns	5	7	7	-	3.5	2.5
Z_{LOAD}	Ω	50	50	50	50	50	50
P_{peak}	MW	0.625	**1.080**	**0.905**	**1.692**	0.500	0.794
E_{pp}	mJ	0.125	0.154			0.143	0.318
PRF_{max}	kHz	100	100		100	100	15
Burst	shots	100	100	*N/A*	*N/A*	*N/A*	100
	%	100	100	*N/A*	*N/A*	*N/A*	100
SD_{Vpeak}	σ	> 2	**> 2**	*N/A*	*N/A*	*N/A*	*N/A*
	%	96.5	**97.8**	*N/A*	*N/A*	*N/A*	*N/A*

(E) Successful construction and operation of a 2×2 DSRD-based IES pulse generator prototype has been completed, which meets or exceeds the required key performance metrics. Shown in Table 5.4.2 are the previous and current pulse generator performance specifications in comparison to a similar 2×2 pulser developed by Kesar et al. [1] using DSRDs, and to that of a commercial off-the-shelf (COTS) DSRD pulser of similar space and weight developed by Megaimpulse (i.e., PPM-0731), which also uses DSRDs with silicon avalanche shapers (SAS) [2]. Although the Megaimpulse pulser utilizes a SAS with a <500 ps risetime (a threshold we do not intend to go below due to Commerce Controlled List limitations), it is interesting to compare the results of linear voltage gain and peak power of this system, to that of one that utilizes a SAS. The current permutation of the 2×2 DSRD-IES pulser developed by MIDE under the ONR OSPRES Grant is able to achieve a higher peak voltage and shorter risetime than DSRD-based pulsers reported in the literature of comparable space and weight as well as those commercially available. The ability to generate a linear voltage gain of 65.7 to produce over a Megawatt of peak power into a 50 Ω load while achieving a peak voltage output standard deviation

of 2σ when operating at a PRF of at least 100 kHz, brings this technology to the forefront of viable options to potentially support the Naval afloat mission.

(F) Discrepancies exist in the obtained pulser and device characterization data for different series combinations and different samples of 7-stack DSRDs, which may be attributed to the inconsistencies in their manufacturing process. Future work includes the design and testing of 2×2 or higher configuration DSRD-based pulsers using more combinations of series-connected as well as parallel-connected DSRD stacks.

5.4.6 *References*

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5.5 All-Solid-State Sub-ns MW Pulse Generators with Semiconductor Sharpeners

(Gyanendra Bhattarai)

This sub-project is currently on hold as focus is directed toward Section 5.4. Please review the January 2022 MSR for the most recent project overview and status.

6 Thermal Management

6.1 Ultra-Compact Integrated Cooling System Development

(Sam Sisk, Roy Allen, and Sarvenaz Sobhansarbandi)

6.1.1 *Problem Statement, Approach, and Context*

Primary Problem: A thermal management system (TMS) is required for cooling semiconductor-based pulse-power devices, using anywhere from 50 to 200 W, with the goal of maintaining the semiconductor device temperature below 80 °C to avoid chip damage. The proposed system must increase cooling densities at a rate of at least 1 kW/cm^2, the current state of the art, while decreasing pumping power requirements, in-line with the SWaP-C^2 objective. This device also needs to be small enough to be used anywhere from server warehouses to drones, thus a dimension of 1 cm^2 is initially targeted, with scaling up remaining a future possibility.

Solution Space: To achieve such high cooling densities, we propose three potential solutions: an ultra-compact TMS (UC-TMS) to be directly integrated into the semiconductor, a monolithically integrated manifold microchannel chip (mMMC) TMS, and an updated jet impingement TMS (JI-TMS). The UC-TMS and JI-TMS are expected to achieve enhanced heat transfer rates due to the turbulent flow from the array of nozzles. The mMMC-TMS is expected to have low pressure losses while still transferring sufficient heat. The JI-TMS and UC-TMS are expected to have lower pressure losses if the outlet cross-sectional surface area for the transfer fluid is equivalent to the inlet cross sectional area. As the proposed TMS dimensions are restricted to 1 cm^2 surface area, the required pumping power should be kept to a minimum. An array of micro-sized jet nozzles will provide a turbulent flow onto a microchannel section directly on the semiconductor device.

Sub-Problem: The turbulency formed from the array of nozzles creates an extreme pressure loss from the large amount of jet nozzles (over 200) and a flow diameter of 100 microns. The pressure must be sustained to enable proper cooling and circulation processes.

State-of-the-Art (SOTA): Integrated chip cooling is being widely used to dramatically increase the operational power of high-voltage silicon-based power devices. However, the current SOTA devices include surface to surface contact points that rely on cohesive connections. These connections increase the amount of material through which heat must transfer to the coolant, thus limiting the heat removal rate.

Objective: To design, simulate, and compare three different TMSs (ultra-compact, monolithically integrated manifold microchannel chip, and jet impingement) under the same operating conditions, and optimize through an iterative process. The proposed UC-TMS and JI-TMS design are based on refining in-chip jet-impingement geometry through leveraging theory and a parametric evaluation of nozzle geometry, flow channel arrangements, and outlet to inlet area ratios. The mMMC TMS performance will be compared with the corresponding results available in the literature and with the results from the other two designs.

Challenges: The manufacturing techniques needed for integrated chip cooling systems have not been entirely adopted. The proposed compact designs are restricted due to the low tolerances needed for the geometries of the nozzles and heating plate; the manufacturing process must be capable of layering the silicon TMS onto the semiconductor.

Risks: With a system so compact, the pressure drop could be a large issue regarding the objective heat dissipation rate. An extreme pressure drop would potentially cause the coolant to flow backwards, causing less fluid-to-solid interaction.

6.1.2 *Tasks and Milestones / Timeline / Status*

(A) Design a Si base 1 cm^2 UC-TMS, JI-TMS, and mMMC-TMS to achieve a heat dissipation rate of 1 kW/cm^2. The devices will need to be designed with consideration of manufacturing capabilities. / MAR22–MAY22 / In Progress

(B) Using the computational fluid dynamics (CFD) ANSYS software, simulate the results for the UC-TMS, JI-TMS, and mMMC-TMS all operating under the same conditions. Compare the results and iterate on the designs to meet the target metrics, such that an optimal design may be chosen to move forward with. / MAY22–JUN22 / In Progress

(C) Using the optimal design, perform ANSYS simulations using de-ionized water or Si-C nanofluid as the coolant and see how fluid type changes the effectiveness of the TMS. Other fluid types may be researched as pressure drop is a large factor. / June22–JULY22 / Upcoming

- Prove simulations from previous literature to show capable design configurations with acceptable pressure drop and steady temperature.

(D) With all problems addressed with simulation results and having a single design able to be manufactured, manufacture a prototype to begin experimental testing and evaluation / AUG22–OCT22 / Upcoming

6.1.3 *Progress Made Since Last Report*

(A) Taking what was learned from last month's design and making sure the heat transfer coefficient needed is at least the same from what is derived from the equations using dimensions from the design, the properties of de-ionized water, and addressing the 1 kW/m. This new design is significantly more compact as well which allows for better placement on the processor.

(B) Given that a JI-TMS design was found, simulations were conducted using ANSYS Fluent's CFD software. The JI-TMS design was split into two sections called the entry stage and exit stage. This was done to save on computation time as the design has over 14 million elements. Simulations on this version were able to be done in one stage. These simulations were done at 7 different inlet velocities, and measured the semiconductor wall temperature, outlet pressure, and outlet velocities.

(C) Simulations using ANSYS Fluent were validated to real world experiments to show that the model is acceptable in predicting the energy and fluid physics. This validation will lead to a redesign of the TMS for future prototyping.

6.1.4 *Technical Results*

(A) The second version of the JI-TMS design was achieved using equations found in Incropera, as provided belowm, and mainly focusing on matching the required heat transfer coefficient. The geometric governing equations were all input into an excel spreadsheet. This spreadsheet made it much easier to tweak the nozzle diameters and the incoming fluid velocity.

$$\overline{Nu} = .5K\left(A_r \frac{H}{D}\right) G\left(A_r \frac{H}{D}\right) \mathrm{Re}^{2/3} Pr^{.42} \quad (1)$$

$$K = \left[1 + \left(\frac{\frac{H}{D}}{\frac{0.6}{Ar^{.5}}}\right)^6\right]^{-0.05} \quad (2)$$

$$G = 2Ar^{.5} \frac{1-2.2Ar^{.5}}{1+0.2\left(\frac{H}{D}-6\right)Ar^{.5}} \quad (3)$$

$$Ar = \frac{\pi D^2}{2\sqrt{3}S^2} \quad (4)$$

$$Re = \frac{VD}{\nu} \quad (5)$$

$$\overline{Nu} = \frac{\bar{h}D}{k} \rightarrow \bar{h} = \frac{\overline{Nu} * k}{D} \quad (6)$$

$$q = \bar{h}A(\Delta T) \quad (7)$$

$$2000 \leq Re \leq 100{,}000$$
$$2 \leq H/D \leq 12$$
$$.004 \leq Ar \leq .04$$

(B) The decided geometry of a 0.088 mm diameter was created using Solidworks, as shown in Figure 6.1.1. The file was then converted into a format that can be simulated with ANSYS FLUENT. The model used was Epsilon-k as the system is turbulent due to the Re greater than 2000 and the Energy Model as there was energy transfer within the system. An initial simulation was done at a velocity of 20 m/s shown in Figures 6.1.2-.4, this was done to show that it was a successful trial in removing the heat from the semiconductor.

The 7 simulations were then done at various inlet velocities to better visualize the relationship with semiconductor wall, outlet velocities, and outlet pressure.

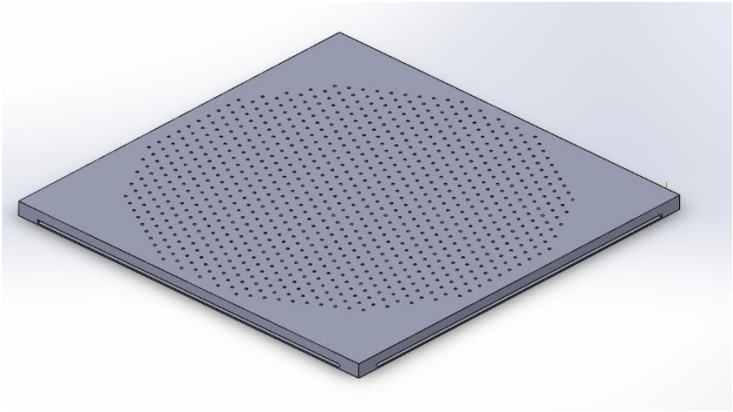

Figure 6.1.1. Solidworks geometry.

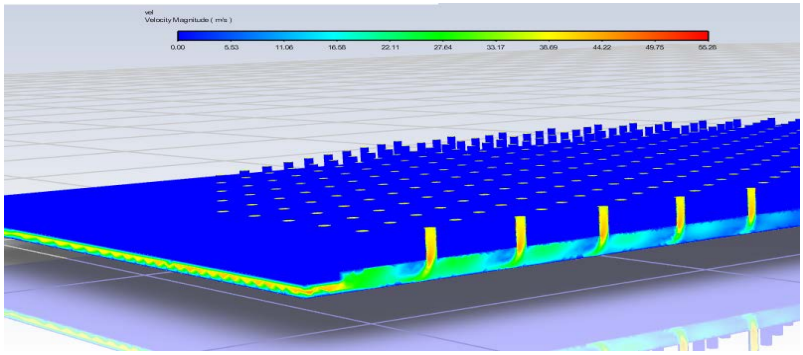

Figure 6.1.2. Contour plot of velocity.

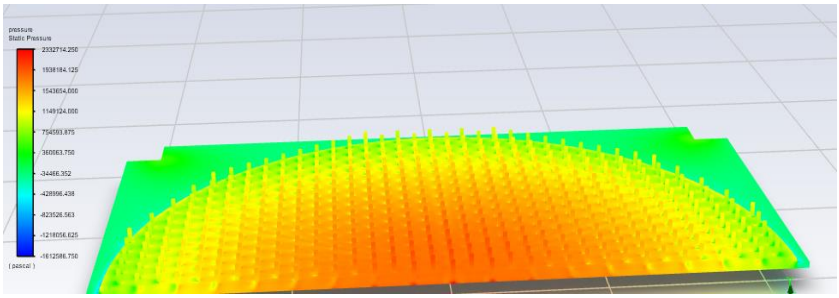

Figure 6.1.3. Contour plot of pressure.

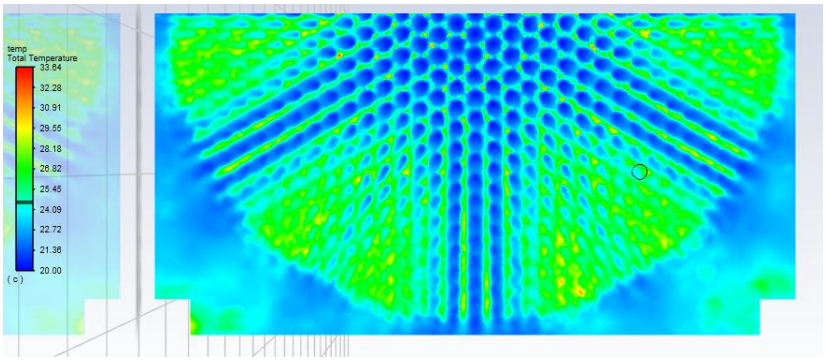

Figure 6.1.4. Contour plot of semiconductor temperature.

1kW/cm^2	Semiconductor Wall			Outlets			Outlets		
Vel (m/s)	Min Temp	Max Temp	Avg Temp	Pressure Min	Pressure Max	Pressure Avg	Min Vel	Max vel	Avg Vel
10	19.97	71.997	34.16701	-96205.11	235512.6	52261.31	0	15.65179	10.14164
15	19.98431	50.80291	30.28365	-183850.2	487552.6	117840.7	0	22.11517	15.24262
20	19.98861	48.14755	27.81217	-323868.9	828917	209796.4	0	29.31488	20.3478
25	19.9913	42.32336	26.24605	-497941	1258708	328133	0	36.64879	25.45503
30	19.99322	37.20333	25.21831	-712091.9	1776461	473002.4	0	43.80521	30.56848
35	19.99459	34.640617	24.48916	-937216.6	2382329	644381.3	0	50.9682	35.68513
40	19.9956	32.46942	23.94143	-1204792	3074510	842181.7	0	58.23039	40.80144

Table 6.1.1. Numerical results showing relationship with inlet velocity.

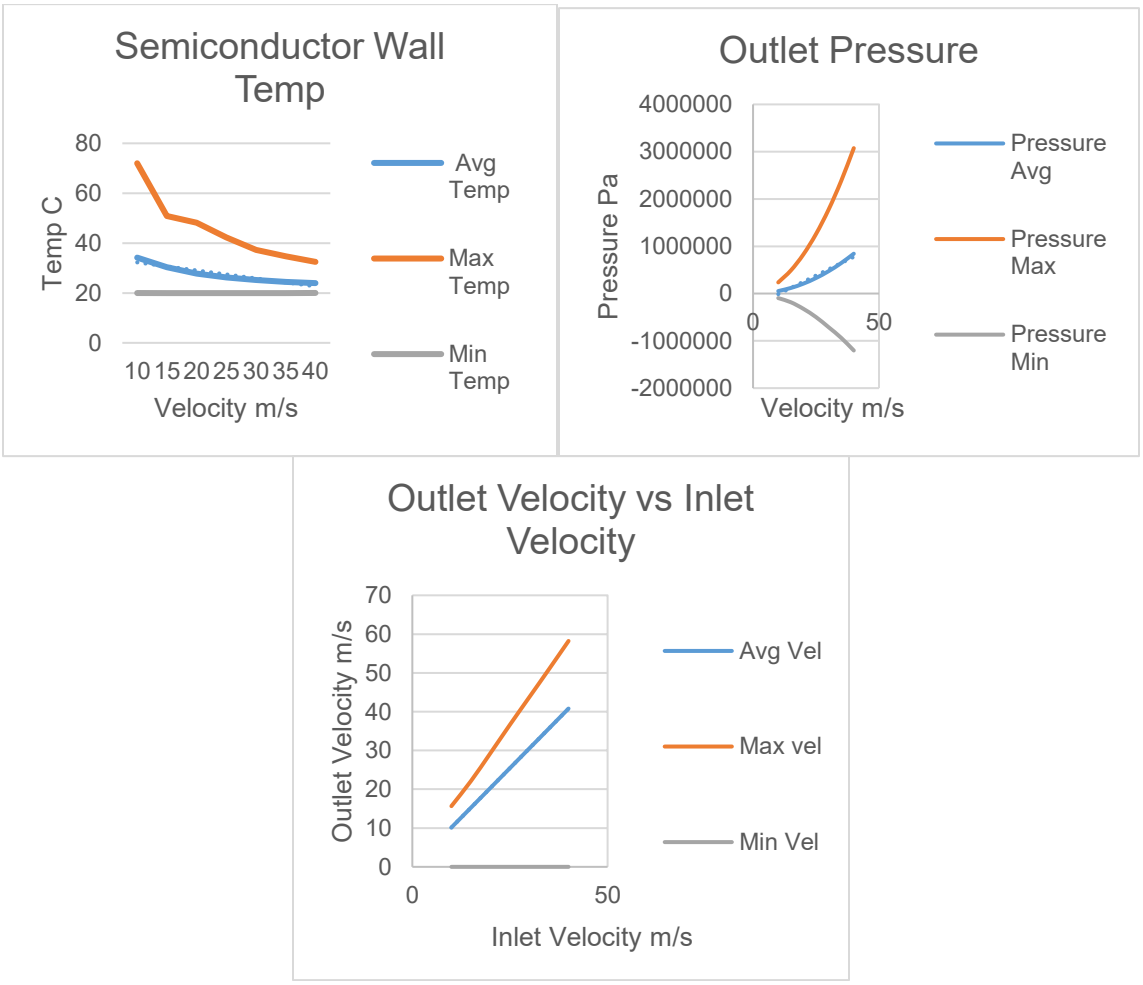

Figure 6.1.5. Graphical representation of Table 6.1.1.

(C) To validate the finding made by the numerical model used in ANSYS fluent, we compared our results to the literature [2]. In this work they created a Impinging jet geometry of 22 300 μm diameter impinging jets called Jet Impingement Surface Cooling (JISC); the nozzles were spaced evenly 4550 μm from each other in 2 rows (Figure 6.1.6).

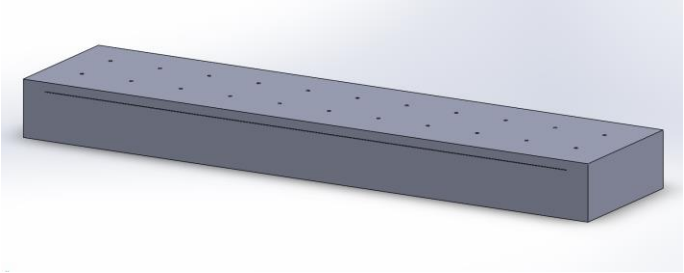

Figure 6.1.6. JISC Geometry.

To validate our experimental set up all geometrical and starting conditions were used exactly as stated in the previous work; the only thing that was changed were the simulations set up. The comparison that was most insightful to assess whether the setup was correct is the change in temperature of the case.

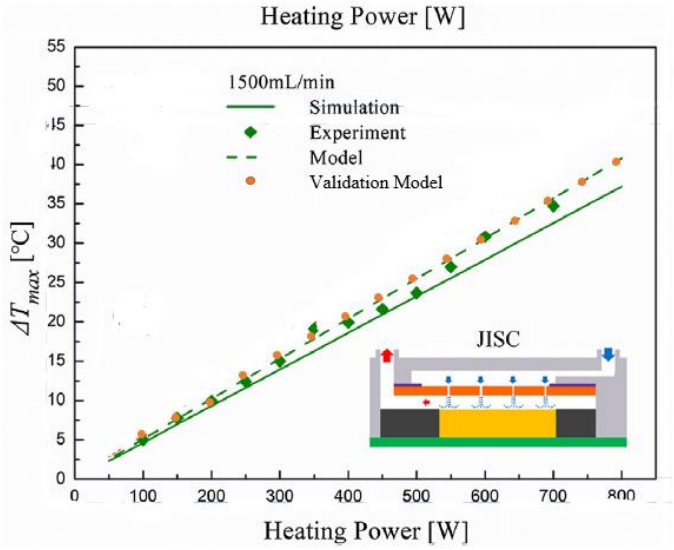

Figure 6.1.7. Comparison with validation model graph from Wu.[2]

Watt Power	Experimental	Validation Model	% Difference
100	4.944674965	5.51819	11.59863972
150	7.7593361	7.59586	2.106831016
200	9.889349931	9.6106	2.818688112
250	12.39972337	13.05826	5.310897713
300	15.06224066	15.5177	3.023848485
350	19.17012448	17.9765	6.226482684
400	19.93084371	20.43567	2.532889729
450	21.604426	22.89481	5.97277612
500	23.65836791	25.35147	7.156461912
550	27.08	27.80685	2.684084195
600	30.08160443	30.26361	0.60503945

Table 6.1.2. Comparison with validation model table from Wu.[2]

6.1.5 *Summary of Significant Findings and Mission Impact*

(A) A geometry was made to meet all geometrical and calculated cooling demands. This geometry is a huge improvement in all key aspects previously stated. This will impact future designs as a process for creating a JI TMS was partially developed. Moving further there may be a few tweaks such as adding fins to further increase turbulence which will improve cooling performance.

(B) The simulations done for the second trial of a JI-TMS geometry showed improved heat removal from the semiconductor. Also achieving low increase in temperature keeping the system below the 80-degree Celsius limit while also decreasing outlet pressure loss.

(C) The validation was a success, proving that not only the simulations model works but achieving a average 5% difference to real world scenarios. Further validation will take place in future entries.

6.1.6 *References*

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[2] Wu, Ruikang, et al. “Thermal Modeling and Comparative Analysis of Jet Impingement Liquid Cooling for High Power Electronics.” International Journal of Heat and Mass Transfer, vol. 137, no. Complete, July 2019, pp. 42–51, doi:10.1016/j.ijheatmasstransfer.2019.03.112.

7 Pulse-Forming Networks

7.1 Diode-Based Nonlinear Transmission Lines

(Nicholas Gardner)

Attention on this sub-project is being entirely directed toward the preparation of manuscripts and an associated dissertation. A summary report will be provided in Summer 2022, and this will serve as a placeholder until this time. Please see the January 2022 MSR for the most recent summary and status and the Outputs section for papers in preparation or published.

7.2 Continuous Wave Diode-NLTL based Comb Generator

(Nicholas Gardner and John Bhamidipati)

Work on this sub-project is currently on hold to focus on reporting and other sub-projects. Please see the May 2022 MSR for the most recent summary.

7.3 Pulse-Compression-Based Signal Amplification

(Feyza Berber Halmen)

7.3.1 *Problem Statement, Approach, and Context*

Primary Problem: Solid-state amplifiers, such as gallium-nitride-based high electron mobility transistors (GaN HEMTs), can be used as high power microwave (HPM) sources to achieve the SWAP-C2 performance metrics necessary to support the cUAV Naval afloat mission. However, even the best high-power GaN HEMTs are limited to 2–3 kW of peak power, much lower than the 0.1 to 3 MW pulsed power available from traditional HPM sources such as travelling wave tubes (TWTs). Achieving a power density of 1 W/cm^2 at a distance of 10 m with a high gain (≥ 10 dBi) narrow-band antenna requires an input power increase of two to three orders of magnitude. Power combination methods to achieve an effective radiated power (ERP) at MW scale require 10 s to 100 s of GaN HEMTs, compromising the SWAP-C2 performance.

Solution Space: Pulse compression techniques are used to increase the peak power and lessen the pulse width in HPM applications. Adapting pulse compression at the GaN HEMT or any other SWAP-C2 compatible source output can achieve sufficient ERP with an optimal radiating element.

***Sub-Problem*:** Pulse compression is generally used to generate a pulsed output with a high peak output power (P_{out_peak}) and a wideband frequency content from a DC input voltage. The main challenge lies in identifying a pulse compression technique that can be used to amplify a narrowband RF input signal. Some of the circuit elements for common pulse compression techniques, such as the saturable inductors used for energy storage in magnetic pulse compression (MPC), exhibit increasingly lossy behavior with high frequency. Another challenge will be to determine, if any exist, the operating frequency limits of the suitable pulse compression technique for high-frequency, high-power signals.

State-of-the-Art (SOTA): Large magnetic pulse compression (MPC) circuits (>1 m^3, >1000 lbs) have demonstrated peak output power up to a few GWs. Smaller versions (~0.125 m^3, 50 lbs to 100 lbs) can achieve 7.5 MW peak power [1].

Deficiency in the SOTA: Traditional MPC systems are large (few meters long), leverage huge transformers, and require liquid coolant such as transformer oil, which leads to undesirable system mass values of ≥1000 lbs. They are used for generating medium or high pulse power traditionally from DC or AC (50/60 Hz) high voltage supplies. There is no known example of high-frequency signal amplification utilizing MPC.

Solution Proposed: Developing a pulse compression circuit that will act as a high-power signal amplifier with a gain of ≥10. Utilizing magnetic pulse compression, or any other suitable pulse compression method, for high power signal amplification with source fidelity.

Relevance to OSPRES Grant Objective: Pulse compression will enable a size and cost efficient solution to high power signal amplification that will lead to HPM source development with optimal SWaP-C2 parameters.

Risks, Payoffs, and Challenges:

Challenges: Modeling pulse compression circuits for high-frequency operation can present a challenge. Pulse compression circuits are generally evaluated in SPICE simulators with low-frequency AC / transient simulations. SPICE is a lumped-element model simulator and cannot solve for the distributed-element model required at high frequencies where the wavelengths become comparable to the physical dimensions of the circuit. Some circuit components, such as the saturable inductor in the MPC, are not available in SPICE or many other simulators and need to be modeled using behavioral models and proprietary material data. Pulse compression circuit modeling, especially at high frequencies, needs to be investigated.

Risks: Pulse compression methods are usually lossy in nature and generate a considerable amount of heat; therefore, designing a proper cooling method must be carried out, which may inadvertently increase the volume (size and weight) of the overall design.

7.3.2 *Tasks and Milestones / Timeline / Status*

(A) Milestone – Demonstrate 2–3 times increase in peak power and compression gain using magnetic pulse compression (MPC) [*estimated completion by SEP22*].

1. Subtask – Model saturable inductors in LTSpice or Matlab/Simulink in order to be able to develop MPC simulations / NOV21 / Complete.
2. Subtask – Investigate the operation, design, and pitfalls of MPC circuits / NOV21 / *Ongoing*.
3. Subtask – Design MPC circuit with RF input and simulation in LTSpice or Matlab/Simulink to evaluate the resulting amplification and frequency content. / JUNE22 / *Ongoing*.
4. Subtask – Model the high frequency behavior of MPC circuit / DEC21 / *Ongoing*.

5. Subtask – Build and test the MPC prototype using bench top power supply / OCT21 / *Ongoing*.

(B) Milestone – Investigate pulse compression methods other than MPC for feasibility *Ongoing*

1. Subtask – Study time reversal pulse compression to assess its compatibility with GaN-based source. JUNE22 / Complete.

(C) Milestone – Increase the compression gain available from PC.

(D) Milestone – Build and test SWAP-C2 compatible high-frequency PC prototype with GaN source.

7.3.3 *Progress Made Since Last Report*

(A.2) LTSpice simulations are continued to observe the effect of resistive load on the MPC circuit.

(A.4) Commercially available magnetic cores were investigated for their suitability for a continuous wave input MPC prototype operating at kHz to MHz frequency range.

7.3.4 *Technical Results*

(A.2) LTSpice simulations were used to observe the effect of resistive load on the MPC circuit. Figure 7.3.1 shows the MPC circuit schematic with the resistive load replacing the last capacitor of the 2nd stage. For optimum power transfer, the load impedance should match the pulse forming network impedance, which is a function of the last stage capacitance C_2 and saturated inductance of saturable inductor L_2:

$$R_L = Z_0 = \sqrt{\frac{L_{2,sat}}{C_2}} \tag{1}$$

For a matched load, the voltage and current at the load becomes:

$$V_L = V_0 \cdot \frac{R_L}{R_L + Z_0} = 0.5V_0 \tag{2}$$

$$I_L = \frac{V_0}{R_L + Z_0} \tag{3}$$

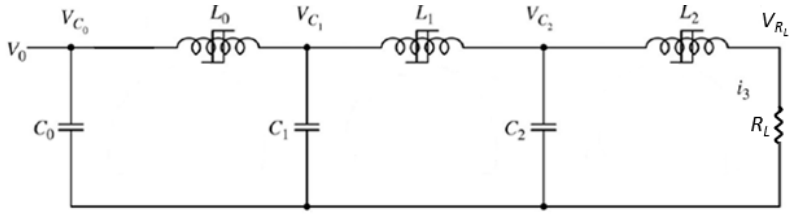


Figure 7.3.1. Circuit schematic for 2-stage MPC circuit with resistive load.

Note that the instantaneous power at the load becomes a function of input voltage and the characteristic impedance of the last stage:

$$P_L = I_L \cdot V_L = \frac{V_0^2}{4Z_0} \tag{4}$$

The effect of the load is simulated using the previously designed MPC circuit reported in the April 2022 MSR. The LTSpice circuit schematic used in the simulations is given in Figure 7.3.2. Note that the 100 µF capacitor at the output is replaced with a load resistor of 5.5 mΩ. The saturated inductance of the last saturable inductor is only 3.04 nH, drastically reducing the load resistance required for impedance matching.

The R_L value can be increased by increasing $L_{2,sat}$ or reducing the capacitance according to Equation (1). Increasing the last stage inductance can be done through changing the geometry of the toroid, i.e., increasing its cross-sectional area or decreasing its electrical length, or by increasing the number of turns, N, for the inductor. The latter would result in impractical N values for the initial MPC stages as the compression gain is equal to N_n/N_{n+1} for inductors with same core material and size. Reducing the capacitance will result in the need to increase the input voltage for accurate MPC operation. Considering the circuit in Figure 7.3.1 with $C_0=C_1=C_2=C$, the time to charge C_1 to its maximum value is given by:

$$t_{C1} = \pi\sqrt{L_{0,sat}C/2} \ = \frac{\pi}{\omega_0} \tag{5}$$

For proper MPC operation, the next stage inductor L1 should saturate at time t_{c1}. The total voltage applied to inductor L_1 at $t=\pi/\omega_0$ is:

$$\langle V_{c1}\rangle t_{C1} = \int_0^{\frac{\pi}{\omega_0}} \frac{V_0}{2}(1-\cos(\omega_0 t)) = \frac{V_0}{2}\frac{\pi}{\omega_0} = \frac{V_0}{2}\pi\sqrt{L_{0,sat}C/2} \tag{6}$$

The saturation condition for L_1 is:

$$\langle V_{c1}\rangle t_{C1} = B_{sat,1} \cdot N_1 \cdot A_{e,1} \tag{7}$$

Substituting (6) into (7):

$$\frac{V_0}{2}\pi\sqrt{L_{0,sat}C/2} = B_{sat,1} \cdot N_1 \cdot A_{e,1} \quad \Rightarrow V_0\sqrt{L_{0,sat}C} = \frac{2\sqrt{2}}{\pi} B_{sat,1} \cdot N_1 \cdot A_{e,1} \tag{8}$$

Given that inductor values are determined by the desired compression gain, and

$$L = \frac{\mu N^2 A_e}{l_e}, \tag{9}$$

(8) becomes:

$$V_0^2 C = \frac{8}{\pi^2}\frac{N_1^2}{N_0^2}\frac{B_{sat,1}^2 \cdot A_{e,1}^2 \cdot l_{e,0}}{\mu_{sat,0} \cdot A_{e,0}} \tag{10}$$

For the same inductor core material and size, (10) reduces to:

$$V_0^2 C = \frac{8}{\pi^2}\frac{N_1^2}{N_0^2}\frac{B_{sat}^2 \cdot A_e \cdot l_e}{\mu_{sat}} = \frac{8}{\pi^2}\frac{N_1^2}{N_0^2}\frac{B_{sat}^2 \cdot V_e}{\mu_{sat}} \tag{11}$$

Equation (11) must be satisfied for proper operation of the MPC circuit, meaning the input voltage – capacitance relation is determined by the core volume and saturation flux

density as well as the MPC compression gain, N_0/N_1. Reducing the C value to increase the load resistance will require an increase in the input voltage for a given MPC circuit. Note that, for a continuous wave input, time to saturation/resonance period given by (5) should also coincide with the input signal period, resulting in further constraints on the values of C and L and the resulting load resistor.

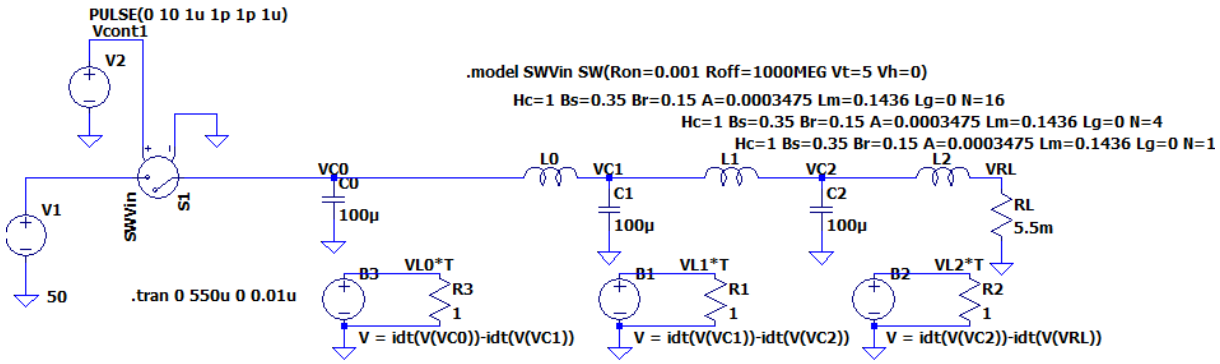
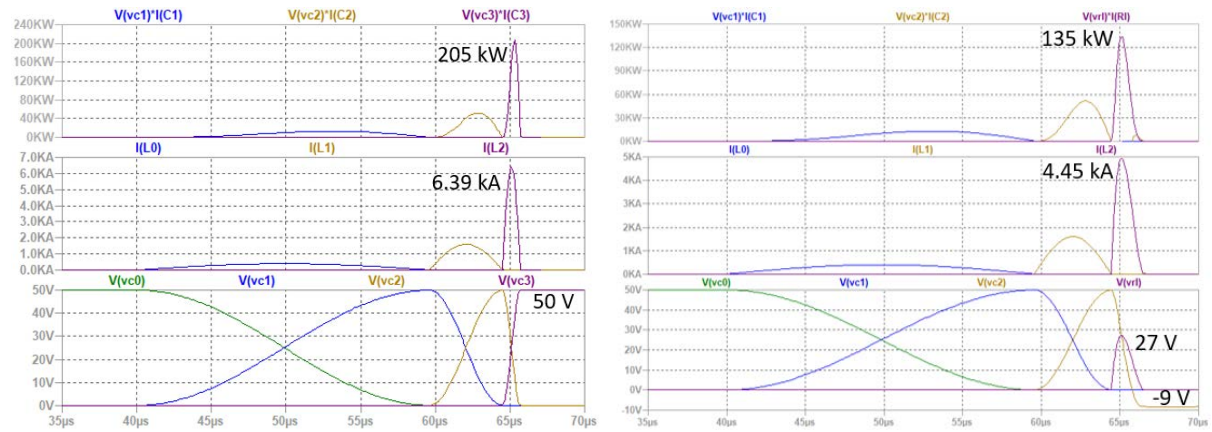


Figure 7.3.2. LTSpice schematic for 2-stage MPC circuit with resistive load simulations.

Simulation results with capacitive and resistive loading at the last stage are depicted in Figure 7.3.3 (a) and (b), respectively. The output voltage and current values are reduced, as given by Equations (2) and (3). Output power is lower with resistive loading compared to the capacitive loading, as the resonant energy transfer is the most efficient method. The negative voltage and resulting power on C2 after energy transfer seems to be a common artifact [2] and can be detrimental in CW operation of the MPC circuit.



(a) (b)

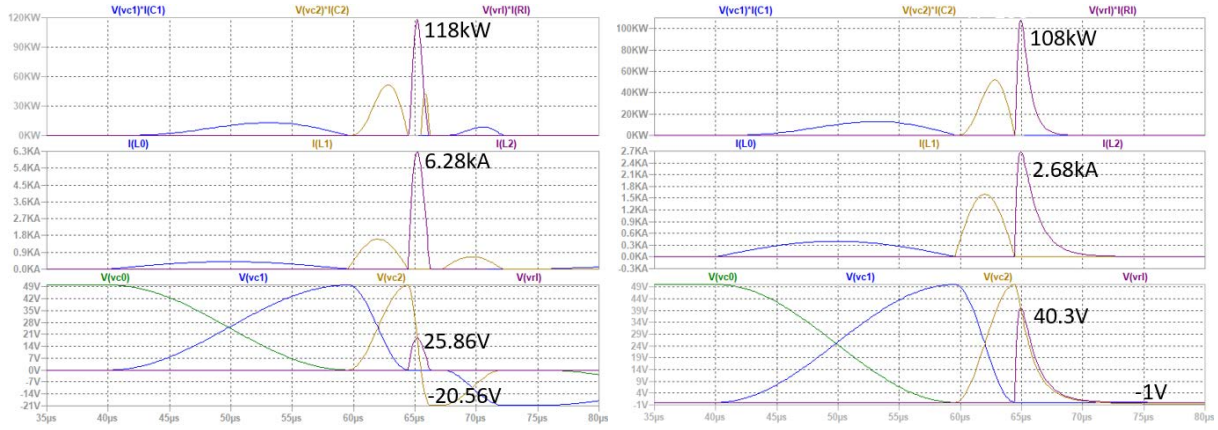
Figure 7.3.3. MPC output voltage, current, and power for (a) capacitive loading (C_L = 100 µF) and (b) resistive loading ($R_L = Z_0$ = 5.5 mΩ).

To observe the effect of different load resistances, the same simulations are repeated in Figure 7.3.4 (a) and (b) for $R_L<Z_0$ and $R_L>Z_0$, respectively. The negative voltage and the resulting power on previous stage capacitors after energy is transferred to the load is more evident for $R_L<Z_0$. The reason is again the non-ideal switch behavior of the saturable

inductors and leakage currents. For $R_L > Z_0$, the artifacts are minimized but the compression gain is much lower. Optimum energy transfer is obtained for impedance matching as expected. Note that the resistive load current and voltage waveforms have shorter rise and longer decay times with increasing load resistance. The current on the resistive load is given by [3]:

$$i_{R_L}(t) = \frac{V_0}{\gamma \cdot L_{2,sat}} e^{-\frac{1}{2}\left|\frac{R_L}{L_{2,sat}} - \gamma\right| t}[1 - e^{-\gamma t}] \quad \text{where} \quad \gamma = \sqrt{\left(\frac{R_L}{L_{2,sat}}\right)^2 - \frac{4}{L_{2,sat} C_2}} \qquad (12)$$

The last term of (12) determines the rise time and the decaying exponential determines the fall time of the pulse on the resistive load. The value of R_L alters the output voltage waveform drastically, as indicated by Equation (12). Different loading schemes need to be investigated the CW input MPC. Pulse forming lines or pulse forming networks are generally utilized as the last stage of MPC in order to obtain rectangular pulses at the output [2-4].



(a) (b)

Figure 7.3.4. MPC output voltage, current, and power for (a) R_L = 3 mΩ and (b) R_L = 15 mΩ.

(A.4) A prototype MPC circuit with continuous wave input at kHz to MHz frequencies will be fabricated as proof of concept. Commercially available magnetic cores were investigated for the MPC prototype. Previous study of the magnetic core materials indicates that the NiZn ferrite is the best material for high-frequency MPC design. The highest frequency NiZn ferrites that are commercially available are M5 from National Magnetics [5], Material 68 from Fair-Rite [6], and 4E2 from Ferroxcube [7,8]. Plots of complex permeability as a function of frequency and B-H curves are presented in Figure 7.3.5 for these magnetic materials. Material properties for all three are summarized in Table 7.3.1.

The cutoff frequency given in Table 7.3.1 is determined as the frequency at which the real permeability, μ', is no lower than the initial real permeability and is at least two times the imaginary permeability, μ''. For all three NiZn materials, μ'' starts increasing rapidly after 100MHz, indicating a large increase in magnetic core loss. M5 offers the lowest μ'' and best loss performance at high frequencies. Frequency-permeability trade-off, dictated by

the Snoek's law, can be observed in Table 7.3.1. with the initial permeability decreasing as the operating frequency increases. M5 has the lowest initial permeability of 7.5 which will result in a low on/off impedance ratio and increase the leakage currents as previously explained.

Table 7.3.1. Material properties for M5, Material 68, and 4E2 NiZn ferrites.

NiZn ferrite	f_c (MHz)	μ_i	B_{sat} (mT)	B_r (mT)	H_c (A/m)
M5	400	7.5±20%	175	125	1830
Material 68	300	16	270	100	557
4E2	200	25±20%	250	195	500

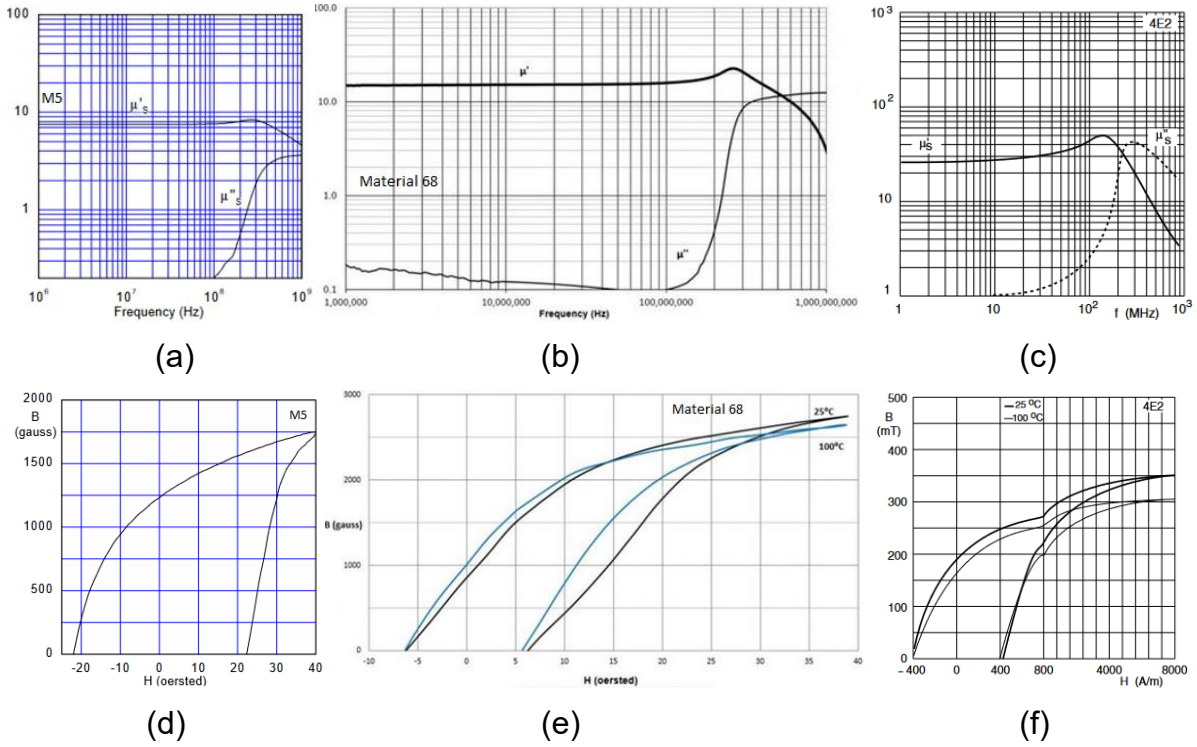


Figure 7.3.5. Complex permeability vs. frequency and B-H curve plots for M5, Material 68, and 4E2.

Core saturation flux density, B_{sat}, is important as it determines the input voltage – period product, VT, required for saturable inductor operation. High-frequency operation reduces the VT value drastically, making it impossible to saturate the inductors. Referring to maximum allowable saturation flux density for a given VT plot from January 2022 MSR, VT of around 10^{-4} V·s is needed to saturate these commercial NiZn cores of $B_{sat} \approx 10^{-1}$ T. This means an input voltage of at least 100 V would be needed at 1 MHz for the accurate operation of the MPC circuit built with these cores. Lower input voltage would be needed for lower frequency operation. Exact VT value depends on the magnetic core

area; however, given the initial calculations with available NiZn B_{sat} values, a prototype MPC will be designed for less than 1 MHz operating frequency.

Even though the B_{sat} for 4E2 is given as 250 mT in the datasheets, its B-H curve given in Figure 7.3.5 (f) shows that the material is not fully saturated at 250 mT but rather undergoes a decrease in its permeability due to the decrease in B-H curve slope. It is not possible to model this B-H curve simulator with LTSpice, but such a change would result in increased leakage currents and lower compression gain in the prototype. Therefore, 4E2 will not be considered for the prototype design.

Core remanence, B_r, and coercivity, H_c, are not included in any MPC design equations but they affect the saturation behavior as described in the April 2022 MSR. Low H_c and high B_r were shown to minimize the leakage currents in MPC, improving the compression gain. Material 68 has much lower H_c compared to M5, which would result in much lower leakage currents as well as hysteresis losses.

Given the cutoff frequency, initial permeability, B-H curve, and commercial availability considerations, Fair-Rite Material 68 toroids will be used for the prototype design. Only toroids of magnetic length 29.5, 78, and 158 mm are readily available for purchase with this material, resulting in additional design constraints.

7.3.5 *Summary of Significant Findings and Mission Impact*

(A) Initially a basic 2-stage magnetic pulse compression (MPC) circuit was built and tested with DC input to better understand the MPC principles and considerations such as inductor sizing, pre-pulse currents, and inductor saturation. Next, saturable inductor modeling was realized in LTSpice with inductor flux expression and the Chan model [2]. Prior to MPC system simulations, magnetic core losses were investigated, and core selection constraints were determined based on the core losses and high-frequency MPC design considerations. Next, different magnetic core materials were investigated to determine the most suitable candidate for high-frequency MPC. As reported previously, such a core should have high resistance, narrow hysteresis loop, minimized eddy current area, and low saturation flux density (B_{sat}). High permeability (μ) and very sharp saturation characteristics are also preferred in order to minimize pre-pulse currents and resulting MPC gain loss. NiZn ferrites are the best option among the commercially available magnetic cores for the high-frequency MPC application as they have the highest operating frequency, low B_{sat}, and sufficiently high μ. After investigating suitable magnetic cores and their properties, LTSpice simulations of the previously tested 2-stage MPC circuit were resumed using the Chan model for Kemet NiZn cores. The inductor for the input stage was replaced with a magnetic switch based on the simulation results. The effects of core coercivity and remanence on MPC operation, which is not included in the design equations, were simulated, and high remanence and low coercivity were found to result in the lowest leakage currents due to sharper saturation behavior. A prototype B-H curve tracer was also built in order to characterize the magnetic cores that will be used in the MPC circuit. The prototype is now complete with the high voltage section isolated in an enclosure. Measurement of known cores with the B-H curve tracer and analysis of the results are ongoing in order to verify the accuracy of the prototype. A SoW has

been drafted with KRI for the design and fabrication of a NiZn-YIG magnetic composite with cutoff frequency of over 500 MHz and relative permeability of 25. Commercial magnetic cores offer the highest cutoff frequency of 350 MHz with relative permeability of only 7.5. New magnetic material development is needed to realize a magnetic switch at higher frequencies. A prototype MPC circuit with continuous-wave input at low frequencies will be fabricated as proof of concept before finalizing the KRI SoW. Commercially available magnetic cores were investigated for their suitability for the MPC prototype operating at kHz to MHz frequency range. Only three magnetic materials are commercially available with a cutoff frequency of 200 MHz and higher. Considering the need for high permeability, sharp saturation, and low coercivity for high compression gain as well as the toroids readily available for purchase, Material 68 from Fair-Rite was selected for the prototype. Prototype design will proceed with the downselected toroids. MPC simulations were continued to observe the effects of resistive loading. Optimal energy transferred is obtained for load resistance matched with output stage impedance, which results in very small, e.g., mΩ range, load resistors. MPC circuit elements and input voltage could be sized to maximize the load resistance, and related design equations were derived. Some voltage and current artifacts due to non-ideal switch behavior were observed with resistive loading. As this behavior can be detrimental to CW MPC operation, different loading schemes will be investigated.

(B) Time reversal pulse compression (TR PC) is investigated as an alternative PC-based signal amplification method. TR PC shows a few dBs of gain in the time domain but loss in the frequency domain as its main component, the resonant cavity, is a passive and lossy circuit element. One-bit time reversal (OBTR) PC, which increases the time domain gain to ≥20 dB, shows ~3x gain in the frequency domain at some frequencies but completely distorts the output signal due to the digitization process. The impulse response record time significantly affects the compression gain and limits the pulse repetition frequency. The compression gain also drops significantly for narrowband signals. Time-reversal-based pulse compression methods are therefore found to be incompatible with a GaN source, especially due to their limited PRF and low compression gain for narrowband signals.

7.3.6 *References*

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8 Antenna Development

8.1 Tradespace Analysis of an Array of Electrically Small Antennas (ESAs)

(Bidisha Barman and Deb Chatterjee)

8.1.1 *Problem Statement, Approach, and Context*

Primary Problem: Determine the extent to which the physical aperture size of an antenna array, composed of patch elements, can be reduced, while maintaining performance in peak power density, bandwidth, and electronic beam steerability over the UHF range (0.4–1 GHz), compared with present-art high-power-microwave-capable antenna arrays.

Solution Space: An array of patch antenna elements whose feed, two-dimensional shape, and relative placement (i.e., intra-, and inter-element design) allow for the physical aperture size to be reduced by more than 20% compared with the present-art.

Sub-Problem: To overcome scan blindness (as the main beam is electronically steered), due to the excitation of surface waves (SW). (Note: scan blindness is a common phenomenon in electrically small microstrip patch antenna arrays).

State-of-the-Art (SOTA): Horn, reflector, Vivaldi, valentine, etc. are some of the commonly used ultra-wideband (UWB) antenna elements in a phased array for high-power microwave (HPM) transmissions.

Deficiency in SOTA: Large physical aperture size of the antennas.

Solution Proposed: Using electrically small antennas (ESAs) as array elements and optimizing their performance in terms of both near-field (bandwidth) and far-field (directivity) parameters, followed by arrangement of the ESAs in suitable lattice structures (preferably, hexagonal/triangular) to reduce the overall array aperture area. Using stochastic and machine learning (ML) algorithms to optimize antenna element and array performance.

Relevance to OSPRES Grant Objective: Provides design and optimization guidelines for UWB ESA elements, especially coaxial probe-fed microstrip patch antennas, and arrays for HPM applications.

8.1.2 *Tasks and Milestones / Timeline / Status*

(A) Develop an Array Pattern Tool in the context of lightweight calculations of large antenna arrays / JAN–MAY 2021 / Completed MATLAB code.

(B) Investigate the effects of array aperture area reduction on different array parameters (such as gain, beamwidth, electronic beam steerability) and present a comparative study of antenna array parameters as a function of array aperture area / JAN–MAY 2021 / Completed.

(C) Build minimum viable validation prototypes of single ESA elements on substrates that have good power handling capabilities for HPM transmissions at UHF range (such as polyethylene, FR-4, TMM-10i, TMM-6) / JAN 2021–JUN 2022 / Manufactured and tested a tapered coaxial-connector-fed, wideband, rectangular, microstrip patch

antenna element (0.7–1.2 GHz); initiated prototyping an improved version of the same design.

(D) Optimization of ESA (single element) performance using ML based stochastic search algorithms / JUN 2021–FEB 2022 / Completed single objective optimization of ESA elements.

(E) Build minimum viable validation prototypes for arrays of ESA elements / JUN 2021–SEP 2022 / Initiated modeling of the final demonstrable 4×4 array prototype and the associated feed-network.

(F) Optimization of array performance using ML algorithms / SEP 2021–FEB 2022 / Completed single objective optimization of antenna arrays on infinite ground planes.

8.1.3 *Progress Made Since Last Report*

(C) Build minimum viable validation prototypes of single ESA elements:

a. S_{11}-parameter and realized gain of the tapered-coaxial-connector fed microstrip patch antenna were tested.

b. Measured data comports with the simulated result, even in the presence of significant EM discontinuities within the structure.

c. Initiated prototyping of an improved version (v2) of the same antenna element with the objective of reducing discontinuities and improved antenna performances.

(E) Build minimum viable validation prototypes for arrays of ESA elements:

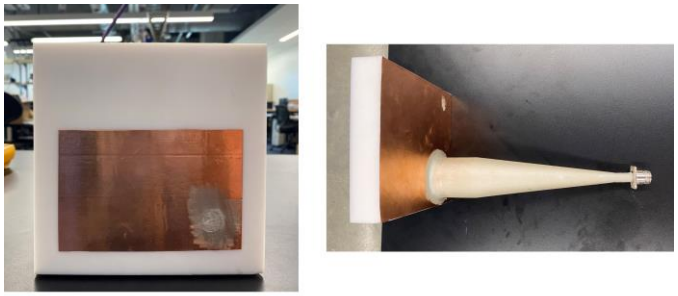
a. A 4×4 array of the tapered coaxial-connector-fed microstrip patch antennas was modeled and characterized via CST microwave studio.

8.1.4 *Technical Results*

(C) Build minimum viable validation prototypes of single ESA elements:

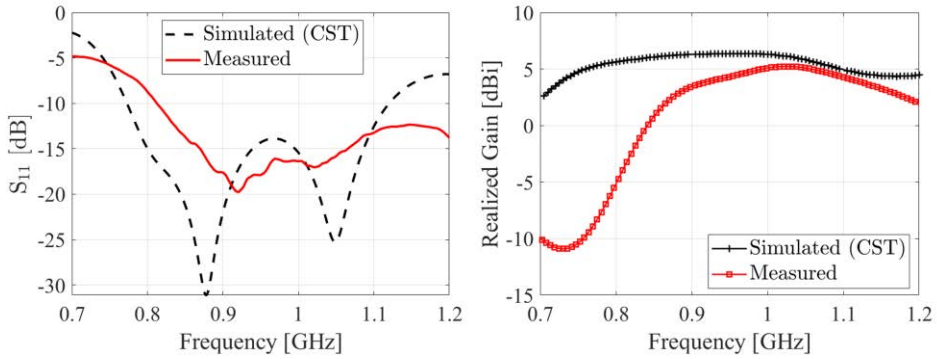
The recently manufactured prototype of the tapered, coaxial-connector-fed, wideband (0.7–1.2 GHz) microstrip patch antenna element, on SLA substrate, was tested in the anechoic chamber at the Lawrence campus of the University of Kansas. Fig. 8.1.1 shows the manufactured prototype of the antenna. Comparison between the simulated and measured S_{11}-parameters and realized gain of the antenna is shown in Fig. 8.1.2.

As mentioned in the ONR-OSPRES-Grant-JUN2022 report, due to the limited capacity of the SLA printer, the substrate and tapered connector sections of the prototype could not be printed as a single block. They were manufactured in parts and connected using UV-cured PMMA glue/cement, leading to electromagnetic discontinuities. Further discontinuities were introduced on press-fitting an N-type connector to the narrower end of the taper. However, even with these discontinuities, the simulated and measured data showed reasonably good agreement (as illustrated in Fig. 8.1.2).



(a) (b)

Figure 8.1.1. (a) Front and (b) side view of the microstrip patch antenna, fed by a tapered coaxial connector, for operation in the UHF (0.7–1.2 GHz) range.



(a) (b)

Figure 8.1.2. Measured and simulated (a) S_{11}-parameter and (b) realized gain of the prototype.

It was decided to manufacture an improved version of the same prototype. In this second iteration, a newly acquired, larger, SLA printer is being used to print the substrate and the tapered connector as a single block, which is expected to *eliminate* the discontinuities between the substrate panel and the connector encountered in the first iteration. The manufacturing of the improved prototype has been initiated with an expected lead time of 1 week.

(E) Build minimum viable validation prototypes for arrays of ESA elements:

A 4×4 array has been modeled with the tapered-coaxial-connector fed, microstrip patch antennas as the array elements. The aperture area of the antenna array (including the PEC-backed substrate) is ≈ 0.31 m^2 with a maximum boresight gain of 17.4 dBi at 1.085 GHz. The boresight gain of the antenna array, as a function of frequency, has been computed using CST microwave studio and is shown in Fig. 8.1.3.

The time-domain performance of the array, subjected to various input short pulses and its beam steerability are currently being investigated and will be reported in the next MSR.

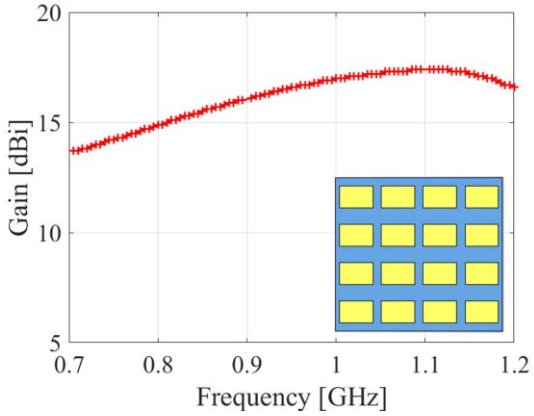


Figure 8.1.3. Boresight gain of the 4x4 array composed of the tapered, coaxial-connector-fed microstrip patch antennas on SLA substrate.

Table 8.1.1. Performance summary of the 4x4 antenna array.

Volume $(\mathrm{L} \times \mathrm{W} \times \mathrm{H})$ (m^3)	Operating Freq. (GHz)	Max. Gain (dBi)	Input Peak Power P_{in} (MW)	Power Density $S(\theta,\phi) = \frac{1}{4\pi}\frac{P_{in}}{R^2}G^R(\theta,\phi)$ at 100 m $(\mathrm{W/cm}^2)$
$\approx 0.61 \times 0.5 \times 0.032$	0.7-1.2	17.4	10	0.44

8.1.5 *Summary of Significant Findings and Mission Impact*

(A) Developing Array Pattern Tool for large arrays calculations:

A MATLAB code has been developed for faster radiation pattern approximation of a linear/planar array of any size and composed of any type of antenna elements. The code requires the center element pattern of a small array (say, 3×3) composed of the same type of antenna elements, desired lattice arrangement, and total number of array elements, as user inputs. The usage of this code will be included in future publications.

(B) Investigate the effects of array aperture area reduction on different array parameters:

The effects of different aperture shape and lattice arrangements on array gain and beam steerability have been studied for arrays modeled on PEC-backed substrates. Investigations show that a transformation from square-grid-rectangular-aperture to triangular-grid-hexagonal-aperture leads to $\approx 30\%$ reduction in aperture area ($\approx 50\%$ reduction in number of array elements) with a tradeoff of ≈ 1.5 dBi (in 2.5–5 GHz) and ≈ 3.5 dBi (640–990 MHz range) gain reduction. The aperture area reduction, however, comes at the cost of limited beam steerability to $\pm 45°$ from boresight, compared to the $\pm 60°$ scanning capabilities achieved from the square-grid-rectangular-aperture arrays, at all frequency ranges.

(C) Build minimum viable validation prototypes of single ESA elements:

Developed a design technique for electrically small microstrip patch antenna that provides $\geq 30\%$ impedance bandwidth by strategic placement of the feed-probe along the patch diagonal, at operating frequencies in the UHF (MHz) to microwave (GHz) frequencies. The method avoids any sophisticated prototyping and is a transformative approach in the design of electrically small microstrip antennas for ultrawideband wireless applications. The design approach was validated via prototypes manufactured on TMM-6 and TMM-10i substrates, in the 2.5–5 GHz range. In addition, a prototype has been built for operation in the UHF range (0.7–1.2 GHz). Despite a few manufacturing defects, the preliminary test results showed reasonable agreement with the simulated values. An updated version of the prototype is currently being manufactured for improved performance.

(D) Optimization of ESA (single element) performance using regular, and ML based stochastic search algorithms:

Optimization of feed-probe location, ground plane shape and size in a microstrip patch antenna, with the objective of bandwidth enhancement, using ML based stochastic search algorithms (GA, PSO, and Simplex methods), was performed. ML algorithms were found to be ≈ 2 times faster and ≈ 0.3 times less memory intensive compared to regular search algorithms, while maintaining the same degree of accuracy.

It is concluded that, although these automated ML algorithms do not provide insight into the underlying physics of the problems and require human intervention at every stage for better decision making, they can still be considered as potential tools for faster optimization of antenna performance, especially for multi-objective optimization of complex structures, which is computationally intensive using conventional EM solvers.

(E) Build minimum viable validation prototypes for arrays of ESA elements:

A 3×3 array of wideband elements (2.5–5 GHz) and a 2×2 array of narrowband elements (900 MHz), on TMM-10i substrates, were manufactured and tested. Having achieved reasonably good agreement between simulated and measured S_{11} and gain responses from individual array elements, it was decided to implement the design method for building the final demonstrable prototypes. Currently, a 4×4 square-grid-rectangular-aperture and a 10-element triangular-grid-hexagonal-aperture array of wideband, microstrip ESA elements, in the UHF range (0.6–1 GHz), are being characterized for prototyping.

(F) Optimization of array performance using ML algorithms:

Completed inter-element spacing optimization in a 4×4 square-grid array, on an infinitely large, PEC-backed dielectric substrate, using a ML-based genetic algorithm, in the 2.5–5 GHz range, with the objective of array boresight gain enhancement. Multi-objective optimization (simultaneous enhancement in boresight gain and impedance bandwidth) of a 4×4 square-grid array on a finite, PEC-backed substrate, by seeking the best array design parameters, including inter-element spacing, ground plane size, and feed-probe locations, in the desired UHF range (0.6–1 GHz), is pursued presently.

8.2 Tradespace Analysis of Ultra-Wide-Band (UWB) Koshelev Antenna

(Alex Dowell and Kalyan Durbhakula)

8.2.1 *Problem Statement, Approach, and Context*

Primary Problem: Determine the extent to which the physical aperture area of an antenna array, composed of antenna elements, can be reduced, while maintaining performance in peak power density, bandwidth, and electronic beam steerability over the UHF range (0.4–1 GHz), compared with present-art high-power-microwave-capable antenna arrays.

Solution Space: The Koshelev antenna has a unique design that is capable of generating an UWB response by effectively merging radiation characteristics from a transverse electromagnetic (TEM) horn antenna with exponentially tapered flares, an electric monopole, and magnetic dipoles over a wide frequency range [1]. This opens up an opportunity to investigate the design parameter space and understand parameter effects on impedance bandwidth, radiation pattern, electric field distribution, and other metrics via a tradespace study.

Sub-Problem:

(i) The integration of an impedance transformer to a single element Koshelev antenna to simulate and test the combined (transformer–antenna) performance is currently not feasible using commercial EM simulators.

(ii)The total surface currents on the Koshelev antenna over the desired frequency range arising from the present positioning of TEM exponential flares, an electric monopole, and magnetic dipoles is not yet clearly understood.

State-of-the-Art (SOTA): The balanced antipodal Vivaldi antenna (BAVA) is considered to be the SOTA antenna element due to its exceptional 20:1 impedance bandwidth ratio as well as the ability to handle tens-of-MW input power.

***Deficiency in the SOTA*:** The BAVA design parameter space has been exhausted over the past couple of decades. The physical aperture area still remains very large and there is no viable path through tradespace study for further physical aperture area reduction.

Solution Proposed: Design, simulate, validate, and perform a tradespace study on the important design parameters of the Koshelev antenna array that effectively reduce its physical aperture area while maintaining its UWB properties, in both the frequency and time domains. The Koshelev antenna has been shown in the literature to withstand higher voltage levels (over 200 kV peak voltage), thereby making it a viable antenna element for detailed tradespace study and analysis.

Relevance to OSPRES Grant Objective: From the literature, it was shown that the Koshelev antenna can handle high input voltages (and therefore high power with 50 Ω input impedance), which satisfies the specific OSPRES objective related to high input voltage/power. In addition, this work can yield a center-frequency-dependent, bandwidth-controlled, and electronically steerable Koshelev antenna design that can be quickly modified to the spectrum properties of the ultra-fast rise time input pulse.

Risks, Payoffs, Challenges:

(i) The electrical size of the Koshelev antenna is approximately λ/4 at its lowest operating frequency. Further reduction of electrical size to λ/10 could considerably reduce frequency dependent gain, thereby decreasing the power spectral density.

(ii) Payoffs include the development of a library of antenna metrics data for different shapes and sizes of the individual parts within the Koshelev antenna.

(iii) The large electrical size (>5λ) of the Koshelev antenna at its highest operating frequency poses huge computational challenges.

8.2.2 *Tasks and Milestones / Timeline / Status*

(A) Complete literature search to identify and list antenna elements that satisfy UWB properties and HPM requirements, and down-select accordingly / NOV–DEC20 / Complete.

(B) Complete initial design, simulation, and validation of Koshelev antenna [1] / JAN21 / Complete.

(C) Perform a preliminary parameter study to identify design parameters that considerably reduce the physical aperture area / FEB–MAR21 / Complete.

- Milestone: Using FEKO and/or CST electromagnetic (EM) simulators, reduce the physical aperture size of the Koshelev antenna to at least 95% of its original design and show minimal to no variation in the bandwidth, gain and increased aperture efficiency / Complete.

(D) Determine the full-width half-maximum (FWHM) and ringing metrics from the envelope of the time domain impulse response ($h_{rx/tx}(t, \phi, \theta)$) in receive or transmit mode / MAR–APR21 / Complete.

- Milestone: Produce a generalized code that calculates the impulse response envelope of the Koshelev antenna and plots the rate of change in FWHM and ringing values as a function of physical aperture size.

(E) Perform tradespace studies on design parameters such as feed position (*F*), length (*L*), and alpha (α). Obtain various antenna metrics data, compare, and analyze / MAR21/ Complete.

- Milestone: Identify Koshelev antenna design parameters that significantly alter the bandwidth, rE/V, peak gain over the desired bandwidth, and aperture efficiency.

(F) Reduce Koshelev antenna aperture size (H×W) to equal to or less than 90 mm × 90 mm, equal to that of the SOTA BAVA, for direct antenna metrics comparison / MAR–APR21 / Complete.

- Milestone: Provide a recommendation on the optimum design parameters and the resulting metrics, with comparison to SOTA BAVA. The optimized design parameters must yield 900 MHz ± 200 MHz bandwidth, rE/V greater than 1, peak gain around 3 dBi at 900 MHz, aperture efficiency equal to or greater than 130% at 900 MHz.

(G) Using the optimized model from (F), build various array simulation models/topologies to perform a tradespace study and report tradeoffs between array antenna metrics such as center element reflection coefficient (S11) value, gain vs theta at constant phi, physical aperture area, aperture efficiency, and rE/V / MAY–JULY21 / Complete.

- Milestone: Develop/showcase an optimized Koshelev array model that exceeds an aperture efficiency of 130% with a high rE/V.

(H) Perform literature search to investigate, understand, and determine the applicability of special electromagnetic (EM) techniques to the antennas under consideration. / JAN–APR21 / Complete.

(I) Explore impedance taper (microstrip based and coax based) designs that can interface well (both mechanically and electrically) to transition the signal from a coax cable to the input of the Koshelev antenna element / JULY21–AUG21 / Complete.

- Milestone: Recommend the optimum impedance taper design (with minimum reflections and maximum power transfer) with the optimum dimensions to successfully convert the high-voltage, short-rise time input signal from a coax cable to the feed of the Koshelev antenna array.

(J) Study response from optimized Koshelev antenna array when excited with different monopolar, differential, and bipolar pulse signals of significant interest / AUG21–NOV21 / Ongoing.

- Milestone: Provide a table comparing the Koshelev antenna array response metrics and narrow down the suitable pulse signals. Recommend (if any) changes to the downselected pulse signal(s) that can further improve the radiation efficiency, and/or transient gain.

(K) Investigate and analyze the response from the optimized Koshelev antenna array when excited by different excitation patterns / DEC 21 / Complete.

- Milestone: Compare and recommend an appropriate excitation method to yield maximum boresight gain, maximum half-power beamwidth (HPWB), minimum side lobe levels, and maximum electric field, rE/V.

(L) Prototype single element Koshelev antenna and test for reflection coefficient, gain as a function of frequency, radiated electric field at 1-m, 2.5-m, 5-m and 10-m (if feasible) distances. / AUG21–SEP22 / Ongoing.

(L1) Fabricate Cu-foil and paint (silver or copper) variants of 3D-printed balanced Koshelev antenna with integrated impedance transformer.

- Milestone: Demonstrate a 3D printed Koshelev antenna prototype that is cost-effective and lightweight. / AUG21–NOV21 / Complete.

(L2) Perform scattering parameter measurements of Cu-foil and paint variants of 3D-printed prototypes to identify any design and fabrication issues/challenges.

- Milestone: Report fabrication & assembly challenges, test outcomes and identify the source of mismatch (if any) to alleviate reflections. Verify against simulations to validate mismatches. / DEC21–APR22 / Ongoing.

(L3) Downselect to one variant of the 3D printed Koshelev antenna prototype and measure frequency domain gain and time-domain electric field at multiple distances.

- Milestone: Experimentally demonstrate a 3D-printed Koshelev antenna with a performance comparable to the standard sheet metal variant of the Koshelev antenna. / MAY22–SEP22.

- Milestone: Report performance of 3D printed Koshelev antenna, compare against the performance of balanced antipodal Vivaldi antenna (BAVA), and recommend any overall improvements to the fabrication/prototyping/testing methods.

8.2.3 *Progress Made Since Last Report*

(L2) In the previous report, a partial dielectric impedance transformer integrated with a Koshelev antenna with varying backplate geometries was simulated. Analysis of the simulated S_{11} and gain plots revealed a viable antenna–transformer combination. Before moving forward with prototyping, structural and fabrication concerns needed to be addressed. After adding structural support and making some modifications to account for 3D printing limitations, the computer aided design (CAD) models were simulated to determine radiofrequency (RF) performance.

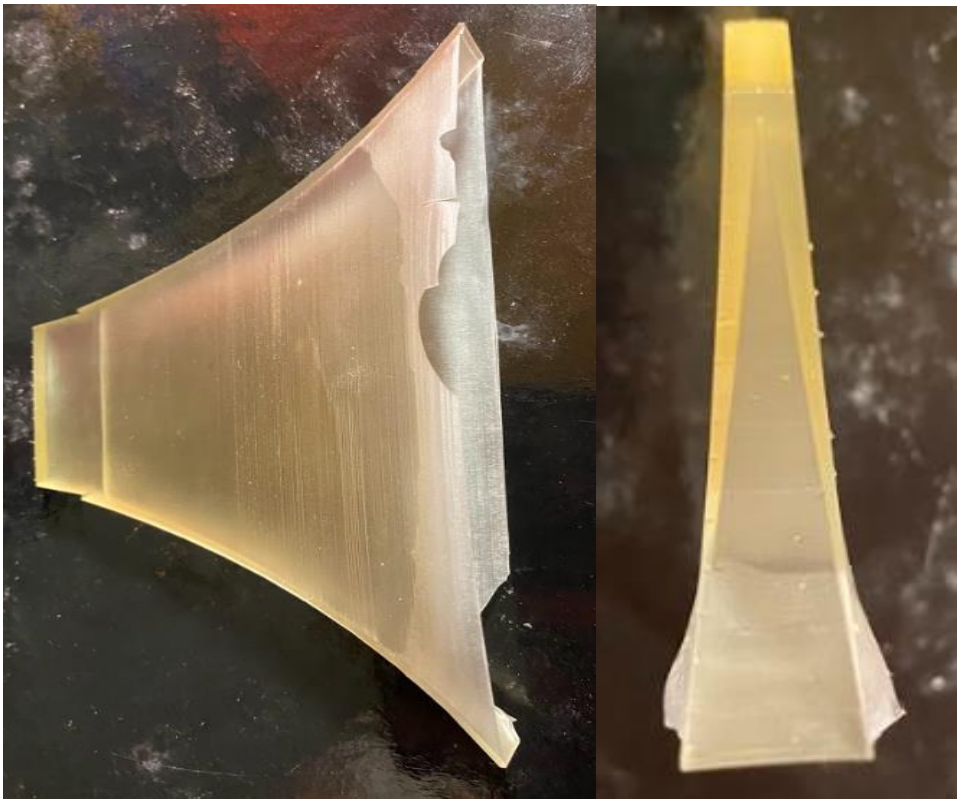
8.2.4 *Technical Results*

$$vol\ \% = \frac{\varepsilon_{reff}-1}{\varepsilon_{ro}-1} \quad (1)$$

It was discovered that the initial polylactic acid (PLA) partial dielectric impedance transformer would not print on a fused deposition modeling (FDM) printer due to the fact that the PLA transformer's smallest feature is smaller than the printer nozzle width of 0.4 mm. The transformer was then redesigned using the permittivity of an ultraviolet (UV) curable resin to see if a stereolithography (SLA) printer would be able to print the transformer. Using Equation (1), where v is the volume percentage, ε_{ref} is the permittivity of the material at that volume percentage, and ε_{ro} is the solid body permittivity of the material, as well as a RF microstrip calculator, a spreadsheet (Table 8.2.1) was created to provide governing dimensions for a resin Koshelev partial dielectric impedance transformer. In the spreadsheet, each row represents dimensions and characteristics at cross sections every 7 mm starting from 10 mm from the N-type feed. A symmetric wedge was removed from the transformer. Therefore, between the top and ground plane, 100% UV curable resin is used for the first 10 mm then linearly tapering to 0% UV curable resin at 80 mm where it interfaces with the antenna. Using the equation above, every 7 mm a new permittivity was calculated. The height of the transformer runs from 7 mm at the N-type feed to 14 mm where it interfaces with the antenna. Starting at 10 mm from the N-type feed inputs of permittivity, constant impedance (50 ohm), and percentage of the transformers height was used to calculate the width of the trace at each cross section.

Table 8.2.1. Effective relative permittivity and its corresponding design variable values utilized to design a SLA impedance transformer model.

ε_ref	Vol %	ε_0 SLA	Length From N Type Feed (mm)	Dielectric Height Cross Section Outer (mm)	Dielectric Width Cross Section Outer (mm)	Dielectric Height Cross Section Inner (mm)	Dielectric Width Cross Section Inner (constant) (mm)	Trace Height Cross Section Outer (mm)	Trace Width Cross Section Outer (mm)
2.60	100%	2.6	10.0	7.77	43.36	7.77	43.36	7.77	21.68
2.44	90%	2.6	17.0	8.31	48.32	7.48	48.32	8.31	24.16
2.28	80%	2.6	24.0	8.85	53.74	7.08	53.74	8.85	26.87
2.12	70%	2.6	31.0	9.39	59.7	6.57	59.7	9.39	29.85
1.96	60%	2.6	38.0	9.92	66.28	5.95	66.28	9.92	33.14
1.80	50%	2.6	45.0	10.46	73.6	5.23	73.6	10.46	36.8
1.64	40%	2.6	52.0	11.00	81.84	4.40	81.84	11.00	40.92
1.48	30%	2.6	59.0	11.54	91.16	3.46	91.16	11.54	45.58
1.32	20%	2.6	66.0	12.08	101.88	2.42	101.88	12.08	50.94
1.16	10%	2.6	73.0	12.62	114.4	1.26	114.4	12.62	57.2
1.00	0%	2.6	80.0	13.15	129.28	0.00	129.28	13.15	64.64



(a) (b)

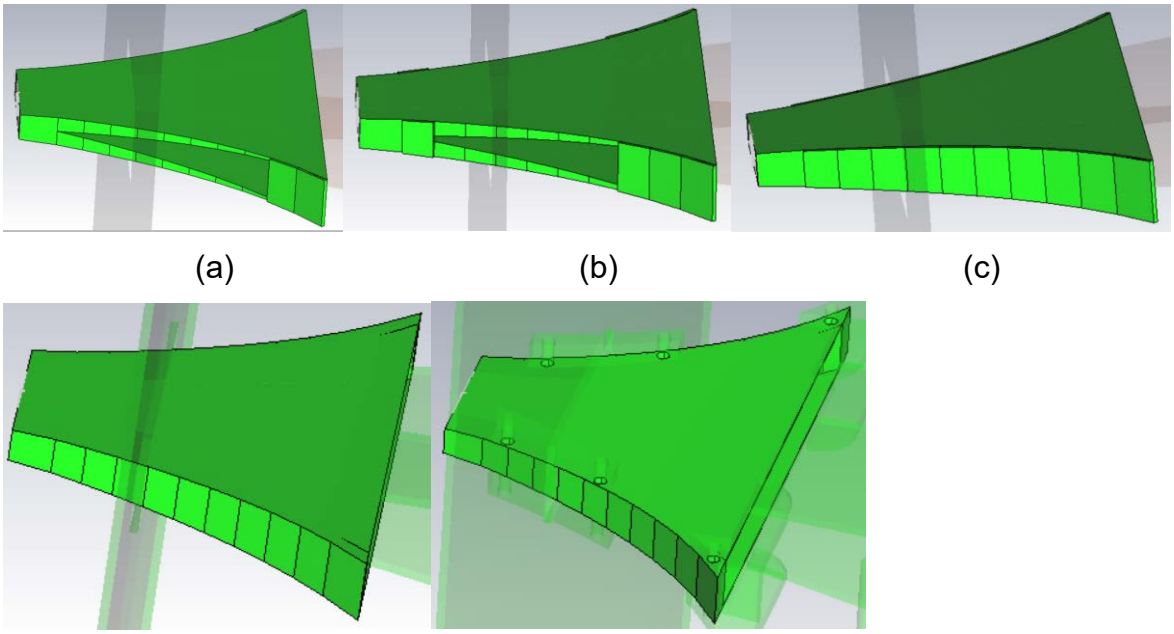
Fig. 8.2.1. (a) Top and (b) side views of a resin partial dielectric impedance transformer printed using a SLA 3D printer.

Fig 8.2.1. (a) and (b) shows that when the transformer walls became thinner than 0.5 mm, the resin began to warp. To further combat this issue, a 0.25 mm printer nozzle was installed on the FDM printer.

(a) (b)

Fig. 8.2.2. (a) Top and (b) edge view(s) of a PLA partial dielectric impedance transformer printed using a FDM printer with a 0.25 mm nozzle.

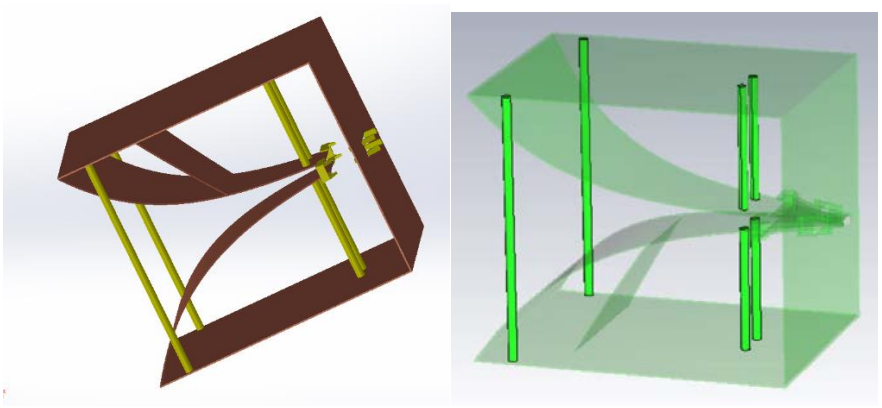
Fig 8.2.2. (a) and (b) show that a smaller 0.25 mm nozzle would not print the section of tapered wall that was thinner than 0.25 mm. To resolve this issue all future iterations of the transformer have the thinnest wall of the tapered sections at least 0.25 mm thick.



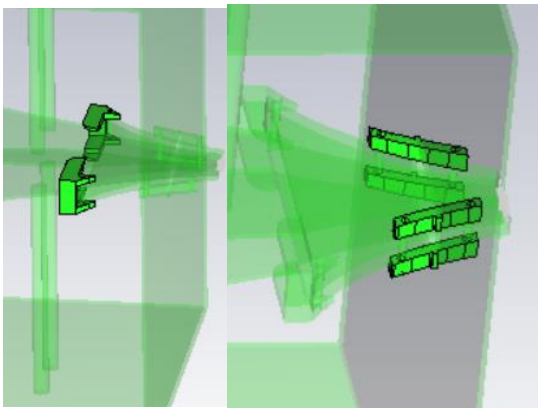
(a) (b) (c)

(d) (e)

Fig. 8.2.3. The geometric changes of the transformer iterations for a structural support case study. The geometric changes consist of: (a) v1 is the initial PLA transformer with minimal 1 mm thick side support, (b) v2 is the second PLA iteration with slightly more 1 mm thick side support, (c) v3 is the third PLA iteration with complete 1 mm thick side wall support, (d) v4 is the first resin transformer with complete 5 mm thick side wall support, (e) v5 is the fourth PLA iteration with complete 5 mm thick side wall support and holes for mounting.



(a) (b)



(c) (d)

Fig. 8.2.4. (a) Koshelev antenna with supporting pillars and transformer mounting brackets, (b) supporting pillars, (c) transformer front mounting brackets, (d) transformer rear mounting brackets.

In Fig. 8.2.3. and in Fig. 8.2.4. are various geometric changes to the Koshelev antenna and transformer respectively to provide adequate support.

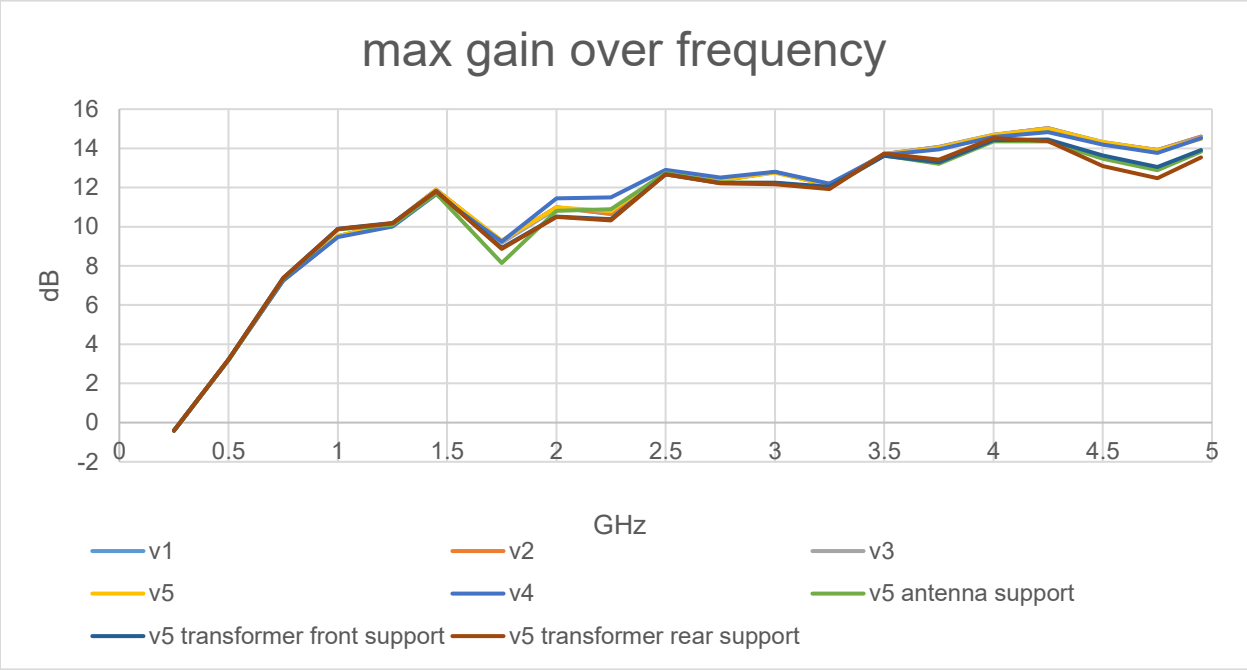


Fig. 8.2.5. Comparing max gains of a Koshelev antenna integrated with a partial dielectric impedance transformer with increasing structural support for each geometric variation collected from CST Studio Suite.

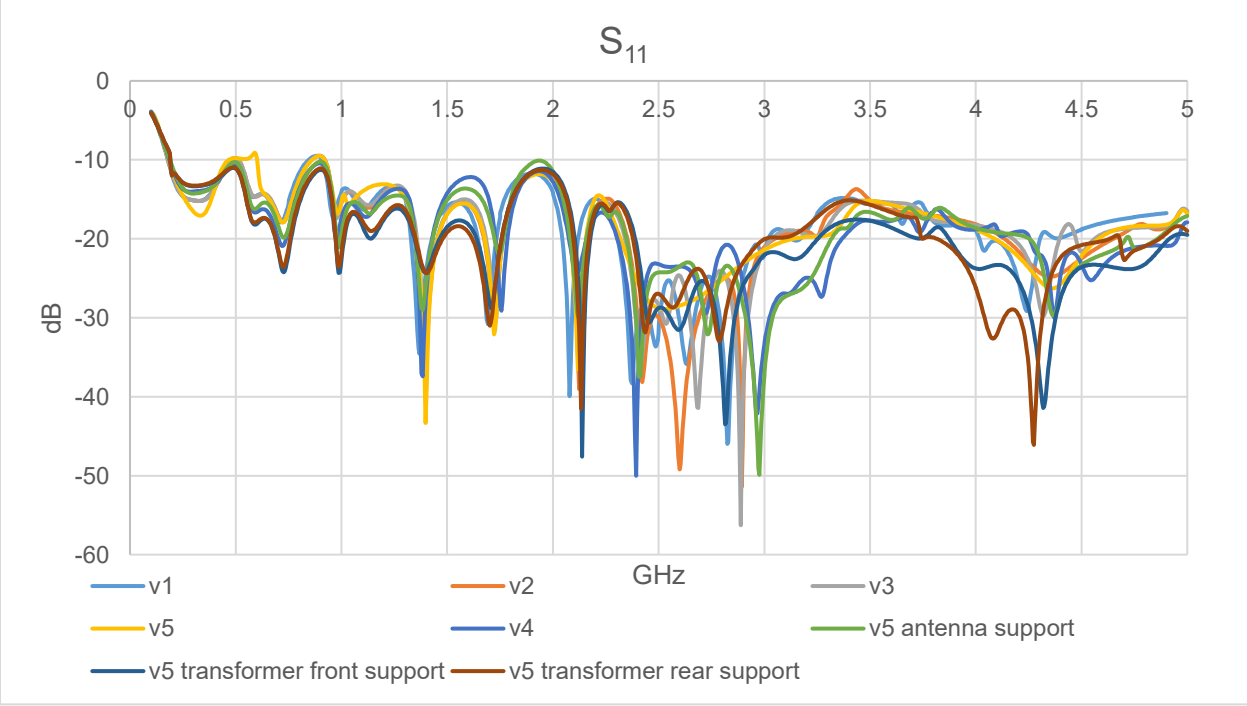


Fig. 8.2.6. Comparing the S_{11} of a Koshelev antenna integrated with a partial dielectric impedance transformer with increasing structural support for each geometric variation collected from CST Studio Suite.

Fig. 8.2.6. and Fig 8.2.7 show that adequate support can be added to the Koshelev antenna and the partial dielectric impedance transformer to produce minimal to no performance degradation.

8.2.5 *Summary of Significant Findings and Mission Impact*

(A) An extensive literature search on various UWB antenna elements has resulted in finding three promising options. The down-selected elements are the Koshelev, Shark, and Fractal antennas, which will be extensively studied using their individual design parameter space, which could result in physical aperture area reduction of the single antenna element. Later, the single antenna element will be converted into a planar array.

(B) Initial validation of the Koshelev antenna simulated using CST software agreed well with the antenna metrics published in the open literature [1]. A UWB bandwidth response (10:1 bandwidth) and rE/V > 1 has been observed from our initial simulations of the Koshelev antenna. This validation ensured that the Koshelev antenna can be subjected to further tradespace studies to understand its performance, followed by optimizing the design according to OSPRES grant requirements.

(C) The initial tradespace study and analysis of the Koshelev antenna design yielded promising outputs to carry forward the investigation. A comparison of important antenna metrics between the Koshelev antenna in [1] and aperture reduced Koshelev antenna are shown in Table 5.2.1 of the APR 21 MSR.

(D) An in-house code has been developed to calculate important UWB time domain antenna metrics such as full-width half maximum (FWHM) and ringing. These metrics have been calculated using in-house MATLAB code using the excitation voltage and radiated electric field information obtained from CST simulations. FWHM and ringing antenna metrics help with assessing or characterizing an antenna's UWB response.

(E) The tradespace study of feed position provided a deeper understanding of how its position impacts the S_{11} value bandwidth. An optimum value for feed position i.e., $F = 1/20 < L < 1/10$ is recommended to achieve maximum bandwidth. The tradespace study of the antenna length (L) is straightforward. A longer antenna length will radiate better at lower frequencies. However, physical size restrictions/requirements must be kept in mind in determining the antenna length. Finally, a larger α value (>120°) is recommended to avoid unnecessary reflections from the electric monopole.

(F) From a thorough tradespace study, the aperture size of the Koshelev antenna (single element) is determined to be 90 mm × 100 mm in order to achieve desired antenna metrics performance proposed in the milestone. All metrics described in the milestone have been successfully achieved except the desired bandwidth (200 MHz on both sides) at 900 MHz center frequency. The bandwidth achieved is 900 ± 100 MHz.

(G) The physical aperture area of the Koshelev array antenna largely depends on the interelement spacing and the shape of the array. We were able to determine that the diamond topology is the optimum shape for the Koshelev array antenna. We were also able to obtain similar gain profile (peak gain and pattern) from making certain

elements within the array passive (off state) when compared against regular active array (all elements in on state). From the non-symmetric interelement spacing values, we found that S_y has the least effect on the output; therefore a small spacing value can be chosen to reduce the physical aperture area of the Koshelev array.

(H) The literature search on the special EM techniques expanded our knowledge and opened the door to opportunities to apply some of those techniques to the antennas under study. EM techniques such as non-symmetric and non-square array topologies have been applied to the development and study of the Koshelev array antenna.

(I) The first impedance taper design under consideration has shown good S11 values (< –10 dB) over the frequency range of interest. In addition, we have shown that the shape of the pulse can be easily retained at the output of the taper with less than 5% amplitude losses.

(J) The Koshelev antenna array response from feeding a monopolar vs bipolar signal has demonstrated a clear winner: that is, a bipolar signal will radiate at least 10 times better than a monopolar signal. A comparison of the frequency spectrum of the radiated electric field from the optimized Koshelev antenna array between different monopolar pulse sources has identified the 'MI0731' pulse to be the optimum pulse.

(K) The optimized Koshelev antenna array was studied for the electric field response under different array excitation patterns. The study determined that the uniform and Gaussian excitation patterns were the optimum excitation patterns. Selecting the uniform or Gaussian excitation pattern would yield the maximum electric field at the boresight for an arbitrary input signal.

(L) Two variants (Cu-foil plated and silver painted) of the 3D-printed Koshelev antenna have been fabricated to demonstrate a working antenna prototype. The measured S_{11} result of the Cu-foil plated variant showed poor performance due to issues at the transformer–antenna interface. The traditional transformer contributed to field discontinuity at the interface. To alleviate this issue, we have designed and simulated a gradient dielectric transformer, which showed improved performance over the traditional transformer. A slot was made on the backplate to facilitate the new transformer, which introduced new coupling issues. The size of the slot was studied and optimized to obtain satisfactory results compared to the original no transformer Koshelev antenna results.

8.2.6 *References*

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8.3 Machine Learning Inspired Tradespace Analysis of UWB Antenna Arrays

(Sai Indharapu and Kalyan Durbhakula)

8.3.1 *Problem Statement, Approach, and Context*

Primary Problem: Determine the extent to which the physical aperture area of an antenna array, composed of antenna elements, can be reduced while maintaining performance in peak power density, bandwidth, and electronic beam steerability over the UHF range (0.4–1 GHz), compared with present-art high-power-microwave-capable antenna arrays.

Solution Space: Fractal antennas possess exceptional fidelity factor values (>0.9), which describe how well the shape of the input pulse is retained at an observation point in the far-field. Their high degree of freedom provides an opportunity to develop systematically modified patch shapes, which in turn leads to improved bandwidth while retaining high fidelity factor values. Machine learning (ML) can be leveraged to predict the antenna array response for an arbitrary design parameter space upon sufficient training and validation.

Sub-Problem:

(i) Fractal antennas generate omni-directional radiation patterns in the H-plane over the desired frequency range.

(ii) ML can suffer from underfitting or overfitting the training model which in turn leads to deviations in the predicted output.

State-of-the-Art (SOTA): Conventional full-wave EM solvers such as method of moments (MoM), multi-level fast multipole method (MLFMM), finite element method (FEM), and finite difference time domain (FDTD) method are currently being used to study, analyze and assess the performance of UWB antennas.

Deficiency in the SOTA: UWB antenna optimization using conventional EM solvers utilizes significant computational time and memory resource.

Solution Proposed:

(i) Design, simulate, validate, and perform a tradespace study on the design parameter space of the selected fractal antenna element using commercially available electromagnetic (EM) wave solvers.

(ii) Train, validate, test, and compare multiple ML models for quicker and accurate prediction of antenna array response for different physical aperture areas.

Relevance to OSPRES Grant Objective: The fractal antenna achieves an UWB response, a mandatory requirement of the OSPRES grant objective, in a small volume footprint and similar physical aperture area when compared against the SOTA BAVA, dual ridge horn antennas etc. Furthermore, the microstrip-design-based fractal antenna can efficiently handle electronic steering by integrating the feed network on the same board. This eliminates the need to build a separate feed network external to the fractal antenna using bulky coaxial cables.

Risks, Payoffs, and Challenges:

(i) A majority of the fractal antenna geometries yield an omni-directional pattern in the H-plane, which can be a risk. However, efforts are underway to mitigate this pattern without deteriorating bandwidth.

(ii) Payoffs include developing a library of antenna metrics data for various fractal shapes and sizes.

(iii) Design challenges and numerical calculations with respect to specific fractal shapes could arise after performing a certain number of iterations to further improve the bandwidth.

(iv) Fractal antennas were known to generate gain loss at random frequencies over their operating frequencies. Achieving gain stability over the desired frequency range can be a significant challenge.

8.3.2 *Tasks and Milestones / Timeline / Status*

(A) Perform tradespace analysis of the fractal element radius *b* over the desired frequency range (4 to 12 GHz) using the genetic algorithm (GA) optimization tool available in the commercial electromagnetic (EM) solver FEKO / FEB21 / Complete.

- Milestone: Provide a recommendation of an optimum value of *b* using OPTFEKO to minimize reflection coefficient or S_{11} (< –10 dB).

(B) Perform tradespace study on different fractal shapes by changing the number of fractal segments to understand the effect of this change on the impedance bandwidth / FEB21 / Complete.

- Milestone: Produce a detailed study of the antenna response such as S_{11}, gain, and bandwidth by varying the number of fractal segments.

(C) Apply the GA optimization tool on the fractal side length *b* over a wide frequency range (2 to 12 GHz with 201 discrete frequency points) and number of fractal segments using OPTFEKO on the LEWIS cluster / MAR21 / Complete.

- Milestone: Reduce physical aperture area by 10% of its present design, reported in the FEB MSR, and demonstrate minimal or no change in S_{11}, gain, and fidelity factor values.

(D) Perform a parametric study and analysis of antenna response by varying hexagon radius, *a* / MAR–APR21 / Complete.

- Milestone: Recommend a value of *a* to reduce the physical aperture area and increase aperture efficiency (>50%) with no variation in other antenna metrics.

(E) Frequency scale fractal antenna design such that the center frequency of the resulting antenna equals 1.3 GHz / MAY21 / Complete.

- Milestone: Modify antenna design with a center frequency equal to 1.3 GHz and achieve similar results (3:1 bandwidth at fc = 1.3 GHz, 3 dBi gain and >130% aperture efficiency at 900 MHz) to antenna design at center frequency ~7 GHz.

(F) Design and simulate various array antenna geometries composed of optimized fractal antenna elements (obtained from (E)) to analyze the effect of overall array antenna

geometry on the desired array antenna response metrics (i.e., gain vs. frequency, gain vs. elevation angle at constant phi, rE/V, half-power beamwidth and side-lobe level.) / MAY–JUL21 / Complete

- Milestone: Recommend a best possible structure with reduced aperture area and minimal loss in gain.

(G) Apply ML models available in Altair Hyperstudy (2021) on the fractal antenna to try and understand the possibilities and limitations of ML models for fast and efficient antenna metrics prediction and optimization. Expand the prediction capability to time-domain electric field and antenna pattern using ML models (k-nearest neighbor and linear regression) available in scikit learn on Python programming tool “Anaconda”. / MAY21–FEB22 / Complete.

- Milestone: Recommend most accurate and efficient ML model for a fractal antenna in time-domain and frequency domain.

(H) Apply ML models on the octagon fractal antenna array lattice to extend the prediction capability beyond single element / SEP21–MAY22 / Complete.

- Milestone: Recommend the best suitable ML model implemented/developed using Python programming language for array antenna metrics prediction.

(I) Develop, validate, and demonstrate a graphical user interface (GUI) to automate the process of employing ML models to predict the antenna output response/ FEB22–SEP22 / Ongoing.

- Milestone: Incorporate the developed automated data extraction scripts, ML scripts to the GUI to enable user to predict antenna response 100x faster than full wave solvers.

8.3.3 *Progress Made Since Last Report*

(I) Latest updates of the GUI.

- The ML GUI for tradespace analysis has been updated following the feedback received by multiple in-house users. In addition to gridlines, users can export the antenna response data directly to a local computer as an excel file. Further, a menu bar is added to the validation window to allow users to compare the predicted antenna response against the actual antenna response calculated using full-wave solvers. The comparison plot will be displayed in a new window. Also, the comparison is illustrated in an interactive plot, which helps the user to understand trends and uncover the patterns faster than in a conventional plot. Finally, two error calculation methods were added to the GUI to calculate the predicted output's error instantly.

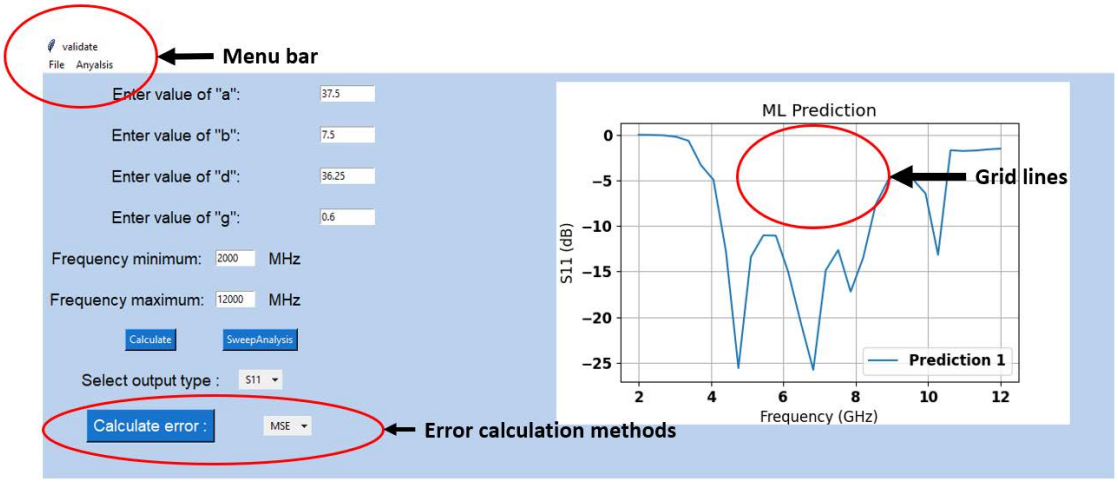


Fig 8.3.1. A snapshot of the GUI validation window.

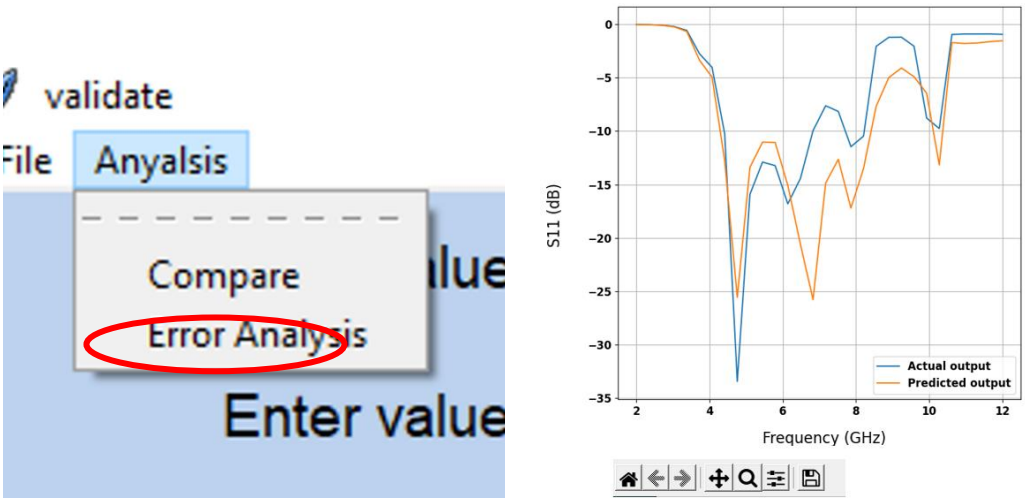
Users can export the predicted antenna response data and plot the comparison plot using the menu bar added to the validation window.

8.3.4 *Technical Results*

(I) Latest updates of the GUI.

Comparison plot:

The addition of an option to compare the EM solver's antenna response to the predicted output will help in evaluating the performance of the selected ML model. This step of comparing data will help the user to analyze the accuracy of the chosen machine learning (ML) model.



(a) (b)

Fig 8.3.2. Snapshot of: (a) compare option on the menu bar, and (b) plot comparing actual and predicted data.

The GUI will request the user to upload the antenna response or test data before plotting the graph. Later, a new window, as illustrated in Fig 8.3.2, will display the corresponding plot.

Error calculation:

After uploading the test data either in the step of data comparison or while directly using error calculation methods, the user can calculate the error. After calculation, the error will be displayed in the message box within the validation window, as illustrated in fig 8.3.3 (b).

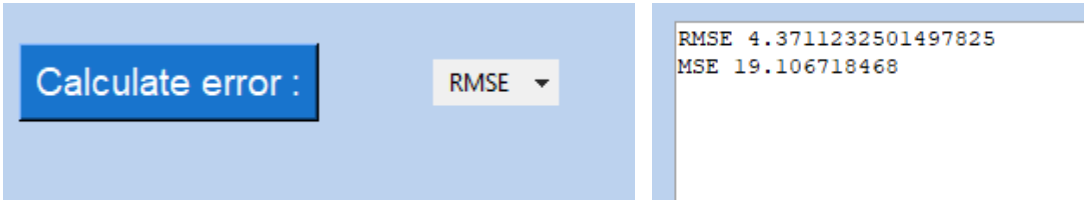


Fig 8.3.3. Snapshot of (a) error calculation icon (b) message box with error values.

Both root mean squared error (RMSE) and mean squared error (MSE) methods can be selected from the dropdown menu to calculate the error. This step will allow the user to measure the error and record the performance of the ML model while altering the training data size or the number of input variables of the ML model.

Data extraction and the Grid lines:

From the feedback received by users, exporting the predicted data was considered to allow users to conduct further analysis. An option to export predicted data is cascaded to the file menu. The GUI allows users to save the data into an excel format in the desired location. Finally, grid lines are also added to the plots.

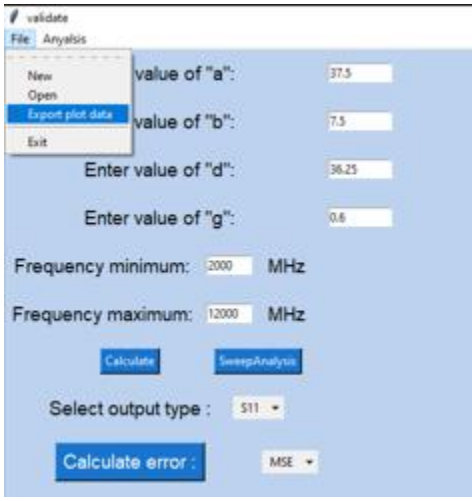
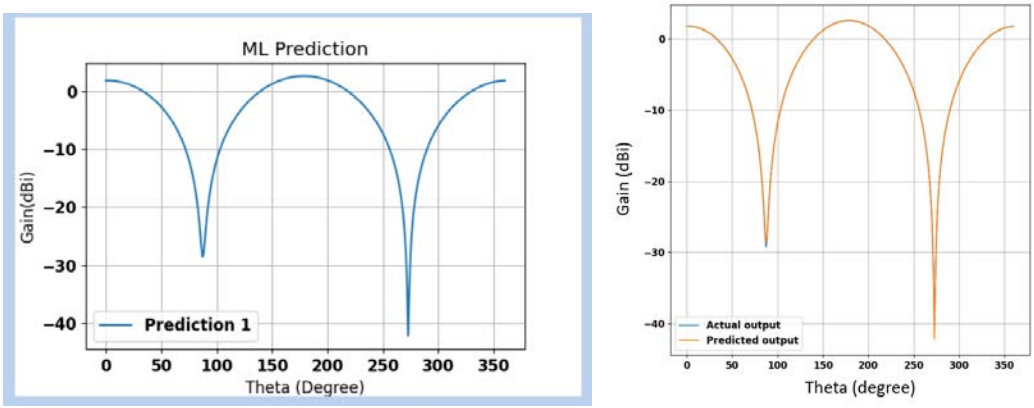


Fig 8.3.4. Data extraction option in validation window.

Gain prediction using the GUI:

The GUI is used to employ the k-Nearest Neighbor (kNN) algorithm to predict the gain(ɵ) response of a fractal antenna. First, a training data set the size of four, including four input design parameters (*a,b,d, and g*), is used to train the model. Following the training, the selected kNN algorithm is tested with a new combination of input design parameters. Fig 8.3.5 (a) illustrates the ML prediction for the test input. Apart from testing the GUI for gain prediction, this step has successfully evaluated the abovementioned updates. Furthermore, the GUI reported the RMSE value of 0.113, indicating an excellent generalization capability of the ML model.



(a) (b)

Fig 8.3.5. (a) Gain as a function of theta prediction for a fractal antenna at 900 MHz, (b) plot comparing actual antenna response and predicted antenna response.

The predicted response and the actual antenna response overlap each other throughout the x-axis (theta) as shown in fig 8.3.5 (b).

8.3.5 *Summary of Significant Findings and Mission Impact*

(A) We carried out an effort to identify the dominant fractal antenna design parameter and its corresponding value using parameter study and FEKO optimization tool. It was found that the side length '*b*' of the fractal elements plays a significant effect on the antenna bandwidth. The initial analysis of the simulation results with fractal radius *b* equal to 1.8 mm yielded multiple resonant frequencies with enhanced bandwidth. To further increase the bandwidth, OPTFEKO was used as an optimization tool with fractal radius *b* as the optimization variable. Finally, the optimum value for *b* is found to be 1.66 mm which minimizes the S_{11} (-10 dB).

(B) The addition of fractal elements (*N*) to the simple hexagon improved antenna metrics such as reflection coefficient (S_{11}). To further investigate and understand the fractal elements, the number of segments (sides of the fractal element) in the fractal geometry were varied within the range of 6 to 14. By varying the number of segments in the fractal element, the resultant S_{11} response has positive impact at higher frequencies and negative impact at lower frequencies. Therefore, the number of

segments of the fractal element were chosen to be 6 as it has better balance of S_{11} values both at lower and higher frequencies.

(C) The initial optimum value of *b* over 51 discrete frequency points is reported as 1.66 mm in task (A). To further increase the accuracy of the optimization algorithm and to find a more precise value for *b*, optimization is further performed over a wider frequency range (201 discrete points between 2 GHz to 12 GHz) which yielded an optimum value of *b* as 1.37 mm. The S_{11} response of the antenna design with this newly obtained *b* parameter (i.e., 1.37 mm) has not produced any better bandwidth compared to *b* = 1.66 mm. Thus, *b* is set to be 1.66 mm for further research.

(D) The hexagonal patch radius *a* has a significant effect on the physical aperture area of the antenna. Therefore, Altair OPTFEKO has been utilized to find an optimum *a* value, which was determined to be 8 mm over the range 7.2 to 9 mm. Antenna metrics such as S_{11}, gain, and bandwidth have shown desired performance with the optimized *a* value.

(E) The initial antenna design has been modified to achieve a center frequency of ~1.3 GHz. The gain value at 900 MHz is 3.5 dBi and, with the modified antenna design, we were able to achieve an impedance bandwidth ratio of 3.3:1. The designed antenna has been fabricated and tested, and the S_{11} response of the fabricated antenna agrees well when compared against FEKO, CST.

(F) Four different fractal antenna array geometries (i.e., square, diamond, hexagon, and octagon) have been designed and simulated. Upon comparing antenna array metrics, the octagonal fractal antenna array has yielded minimal sidelobe levels with a gain of 15.7 dBi at 900 MHz, close to that of the square geometry but with 32.27% lower physical aperture area. The octagonal fractal antenna array has been chosen as the optimum geometry with reduced aperture area and reduced side lobes while retaining the bandwidth and gain milestone metrics.

(G) The ML models available (radial basis function (RBF), least square regression (LSR) and, hyper kriging (HK)) in Altair Hyperstudy were employed to predict the output response of a fractal antenna. RBF and LSR were down selected from the initial three ML models based upon their generalization capability for prediction of fractal antenna output response. The test RMSE increased as the values drifted away from the mid-point of the training range. RBF performed well in the prediction of S_{11}, while LSR performed slightly better for gain and electric field predictions. In addition, for time-domain electric field prediction, we recommend using k-nearest neighbors (kNN) ML algorithm for accurate prediction.

(H) The initial application of the kNN ML model for the prediction of antenna array bandwidth response of center and corner element yielded positive results with good agreement between traditional EM solver (FEKO) and trained kNN ML model. The new LR ML model yielded improved RMSE values (over kNN) in its prediction of reflection coefficient (27.82% less RMSE for center element and 19.76% less RMSE for corner element). On the other hand, the RMSE values for gain (as function of theta) prediction using LR ML model has 55.51% increase over kNN prediction. Finally, kNN provides better generalization to predict reflection coefficient, whereas

LR provides better generalization to predict frequency domain gain in the case of a fractal antenna array. On the other hand, the application of the AEP method for antenna array was put on hold due to its limitations.

(I) A GUI was developed, which accepts training data for an antenna (single-element or array) of user choice and can predict output response (S_{11} and gain) for a range of test data within a few seconds. The GUI has been configured to perform parametric sweep analysis for S_{11} and gain response of a fractal antenna design. Finally, the current version of the GUI has been tested by users with two different antenna designs (i.e., a corrugated conical horn antenna and a traditional horn antenna with GRIN lens). Finally, the GUI is updated to a new version from the feedback/suggestions from the users.

8.3.6 *References*

[1] H. Fallahi and Z. Atlasbaf, "Study of a Class of UWB CPW-Fed Monopole Antenna With Fractal Elements," in IEEE Antennas and Wireless Propagation Letters, vol. 12, pp. 1484-1487, 2013, doi: 10.1109/LAWP.2013.2289868.

[2] S. Zhang, X. Wang and L. Chang, "Radiation Pattern of Large Planar Arrays Using Four Small Subarrays," in IEEE Antennas and Wireless Propagation Letters, vol. 14, pp. 1196-1199, 2015, doi: 10.1109/LAWP.2015.2397600.

9 Feedback

There is no feedback to report for the current reporting period.

10 Program Management

10.1 Issues

i. Scope – No issues
ii. Budget – 12-month NCTE submitted/pending
iii. Schedule – No issues

10.2 Interactions with Others

Agency/Org	Performer	Project Name	Purpose of Research/ Collaboration

10.3 Major Procurement Actions

10.4 Travel

Destination	Purpose	Attendees	Estimated Costs

10.5 Pending or Upcoming Public Release Requests

11 Appendix A: Academic and IP Output

11.1 Students Graduated

Name	Degree	Currently
Al-Shaikhli, Waleed	MS Spring 19	Kansas City National Security Campus, Honeywell
Azad, Wasekul	PhD Summer 21	Applied Materials, Sunnyvale, CA
Berg, Jordan	MS Spring 21	MRI Global
Bhamidipati, John	PhD Spring 22	MIDE
Bissen, Bear	MS Spring 19	Capella Space, San Francisco, CA
Brasel, Sadie	BS Spring 21	
Floyd, Dennis	BS	Naval Air Warfare Center Weapons Division
Hanif, Abu	PhD Spring 21	
Harmon, Aaron	BS	Missouri University of Science & Technology
Harp, Joshua	MS	
Hauptman, Cash	BS Spring 18	University of Nebraska-Lincoln
Klappa, Paul	MS Spring 21	
Kovarik, James	MS 21	
Labrada, Dario	BS Spring 20	Honeywell Aerospace, Florida
Lancaster, John	MS Spring 17	Lawrence Livermore National Laboratory, CA
Renzelman, Jeff	MS Spring 18	Kansas City National Security Campus, Honeywell
Roy, Sourov	PhD Spring 21	BTCPower, Orange County, CA
Wagner, Adam	MS Fall 20	Los Alamos National Laboratory, New Mexico
Xia, Shengxuan	BS	Missouri University of Science & Technology

11.2 Journal Publications

11.2.1 *In Preparation*

[1] S. S. Indharapu, A. N. Caruso, K. C. Durbhakula, “Machine Learning Assisted Antenna Design Optimization of UWB Fractal Antenna,” TBD, In Preparation, **2022**.

[2] J. K. P Bhamidipati, G. Bhattarai, A. N. Caruso, “Effect of Proton Irradiation Induced Localized Defect/Trap Clusters on Silicon Photoconductive Semiconductor Switch (Si-PCSS) Recovery Time and Leakage currents,” *Solid-State Electronics,* In Preparation, **2022**.

[3] N. Gardner, K. C. Durbhakula, and A. N. Caruso, “UHF and L-Band Frequency Generation at MW Peak Power using Diode-based Nonlinear Transmission Lines as Pulse Forming Networks,” *Transactions on Plasma Science*, In Preparation, **2022**.

[4] N. Gardner, K. C. Durbhakula, and A. N. Caruso, “Electrically Tunable Diode-based Nonlinear Transmission Line,” *TBD*, In Preparation, **2022**.

[5] B. Barman, D. Chatterjee, K. C. Durbhakula, and A. N. Caruso, “Tradespace Analysis of Wideband, Electrically Small Microstrip Patch Antenna Elements for

Phased Array Applications," *IEEE Antennas and Propagation Magazine,* In preparation, **2022**.

[6] S. Xia, J. Hunter, A. Harmon, M. Hamdalla, A. Hassan, V. Khilkevich, D. Beetner, "Simulation Driven Statistical Analysis of the Electro-magnetic Coupling to Microstriplines," *IEEE Transactions on Electromagnetic Compatibility*, In Preparation, **2020**.

[7] M. Hamdalla, V. Khilkevich, D. G. Beetner, A. N. Caruso, A. M. Hassan, "Characteristic Mode Analysis Justification of the Stochastic Electromagnetic Field Coupling to Randomly Shaped Wires," *IEEE Transactions on Electromagnetic Compatibility*, In Preparation, **2020**.

11.2.2 *Submitted / Under Revision*

[8] J. K. P. Bhamidipati, E. R. Myers, A. M. Conway, L. F. Voss, M. M. Paquette, and A. N. Caruso, "Figure of Merit Development for Linear-Mode Photoconductive Solid-State Switches," *IEEE Journal of the Electron Devices Society*, Submitted May 1 **2022**, Manuscript ID#JEDS-2022-05-0136-R.

[9] J. K. P. Bhamidipati, K. C. Durbhakula, and A. N. Caruso, "A Dynamically Tunable Discrete-Element Transmission Line Pulse Generator," *International Journal of Electronics and Communications*, Submitted March 6 **2022**, Manuscript ID#AEUE-S-22-01270.

[10] B. Barman, K. C. Durbhakula, D. Chatterjee, and A. N. Caruso, "Comparison of Machine Learning Algorithms for Bandwidth Enhancement of a Coaxial Probe-fed Microstrip Patch Antenna," *Applied Computational Electromagnetics Society (ACES)*, Under Revision (Accepted with Major Revisions), **2022**.

[11] B. K. Lau, M. Capek, and A. M. Hassan, "Characteristic Modes–Progress, Overview, and Future Perspectives," *IEEE Antennas and Propagation Magazine*, Submitted, **2021**.

[12] K. Alsultan, M. Z. M. Hamdalla, S. Dey, P. Rao, and A. M. Hassan, "Scalable and Fast Characteristic Mode Analysis Implementation Using a Hybrid CPU/GPU Platform," *ACES*, Submitted, **2021**.

[13] W. Azad, F. Khan, and A. N. Caruso, "A Scalable Multilevel-Modular 10 kV Silicon Carbide MOSFET Module Featuring Custom Isolated Gate Driver Circuit Combined with Coupling and Snubber Circuits," *IEEE Transactions on Power Electronics*, Submitted, **2021.**

11.2.3 *Published / In Press*

[14] N. Gardner, K. C. Durbhakula, and A. N. Caruso, "Design Considerations for Diode-Based Nonlinear Transmission Lines," *AIP Advances*, 12, 055012, **May 2022** [doi].

[15] J. N. Berg, R. C. Allen, and S. Sobhansarbandi, "A Novel Method of Cooling a Semiconductor Device through a Jet Impingement Thermal Management System: CFD Modeling and Experimental Evaluation," *International Journal of Thermal Sciences*, 172, 107254, **Feb 2022** [doi].

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11.3 Conference Publications

11.3.1 *Submitted / Accepted*

[1] B. Barman, D. Chatterjee, and A. N. Caruso, "Characterization of Planar Phased Arrays of Electrically Small UWB Microstrip Patch Antennas," *2022 IEEE International Symposium on Phased Array and Technology,* Waltham, Massachusetts, USA, Oct. 11-14, 2022, pp. 1-8. (Submitted).

[2] B. Barman, D. Chatterjee, and A. N. Caruso, "On the Optimum Substrate Selection in Wideband Microstrip Patch Antenna Design," *2022 IEEE International Symposium on Antennas & Propagation & USNC-URSI Radio Science Meeting*, Denver, Colorado, USA, July 10-15, 2022, pp. 1-2. (Accepted)

[3] B. Barman, D. Chatterjee, and A. N. Caruso, "Time Domain Analysis of an UWB Electrically Small Microstrip Patch Antenna," *2022 IEEE International Symposium on Antennas & Propagation & USNC-URSI Radio Science Meeting*, Denver, Colorado, USA, July 10-15, 2022, pp. 1-2. (Accepted)

11.3.2 *Presented*

[4] S. R. Shepard and H. A. Thompson, “Self-focusing in Guided and Un-guided Media,” submitted to the *2021 OSA Nonlinear Optics Topical Meeting, Virtual Event*, August 9-13, 2021.

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11.4 Conference Presentations

11.4.1 *Submitted / Accepted*

[1] S. Bellinger, A. Caruso, A. Usenko, "Stacked Diodes for Pulsed Power Applications," GOMACTech-22, Miami, FL, March 21–24 2022 (submitted, oral).

[2] S. Bellinger, A. Caruso, A. Usenko, "New Paradigm on Making Semiconductor Opening Switches for Pulsed Power," 2021 23rd IEEE Pulsed Power Conference, Denver, CO, Dec. 12–16, 2021 (accepted, oral).

Directed Energy Professional Society, Directed Energy Systems Symposium, Washington DC, October 25-29 2021 (submitted):

[3] B. Barman, D. Chatterjee, A. Caruso, and K. Durbhakula, "Tradespace Analysis of a Phased Array of Microstrip Patch Electrically Small Antennas (ESAs)" (Poster)

[4] J. N. Berg, R. C. Allen, and S. Sobhansarbandi, "A Novel Method of Cooling a Semiconductor Device through a Jet Impingement Thermal Management System: CFD Modeling and Experimental Evaluation" (Poster)

[5] J. N. Berg, R. C. Allen, and S. Sobhansarbandi, "Heat Transfer Enhancement of a Jet Impingement Thermal Management System: A Comparison of Various Nanofluid Mixtures" (Poster)

[6] J. Bhamidipati, M. Paquette, R. Allen, and A. Caruso, "Photoconductive Semiconductor Switch Enabled Multi-Stage Optical Source Driver" (Poster)

[7] G. Bhattarai, J. Eifler, S. Roy, M. Hyde, J. Bhamidipati, A. Usenko, M. Pederson, M. Paquette, A. Caruso, S. Bellinger, L. Voss, and R. Allen, "All Solid-State High-Power Pulse Sharpeners" (Poster)

[8] S. Brasel, K. Norris, R. Allen, A. Caruso, and K. Durbhakula, "Efforts to Reduce Physical Aperture Area of Ultra-Wideband Arrays" (Poster)

[9] A Caruso, "ONR Short Pulse Research and Evaluation for c-sUAV: Supporting and Sub-Programs Overview" (Oral)

[10] J. Clark, R. C. Allen, and S. Sobhansarbandi, "Ultra-Compact Integrated Cooling System Development" (Poster)

[11] J. Eifler, S. Roy, M. Hyde, G. Bhattarai, J. Bhamidipati, A. Usenko, M. Pederson, M. Paquette, A. Caruso, S. Bellinger, L. Voss, and R. Allen, "TCAD Optimization of Epitaxially Grown Drift-Step Recovery Diodes and Pulser Performance" (Poster)

[12] N. Gardner, M. Paquette, and A. Caruso, "Diode-Based Nonlinear Transmission Lines Capable of GHz Frequency Generation at Single MW Peak Powers" (Poster)

[13] M. Hamdalla, A. Caruso, and A. Hassan, “The Shielding Effectiveness of UAV Frames to External RF Interference” (Poster)

[14] M. Hamdalla, A. Caruso, and A. Hassan, “A Predictive-Package for Electromagnetic Coupling to Nonlinear-Electronics using Equivalent-Circuits and Characteristic-Modes (PECNEC)” (Poster)

[15] M. Hyde, J. Eifler, S. Roy, G. Bhattarai, A. Usenko, M. Paquette, A. Caruso, S. Bellinger, L. Voss, and R. Allen, “Development of an Evaluation Network for Drift Step Recovered Diodes through and Augmented Design of Experiment” (Poster)

[16] S. Indharapu, A. Caruso, and K. Durbhakula, “Machine Learning Based Ultra-Wideband Antenna Array Optimization and Prediction” (Poster)

[17] F. Khan, W. Azad, and A. Caruso, “A Scalable Multilevel-Modular 10 kV Silicon Carbide MOSFET Architecture for Pulsed Power Applications” (Poster)

[18] D. F. Noor, J. Eifler, M. Hyde, G. Bhattarai, S. Roy, J. Bhamidipati, A. Usenko, M. Pederson, M. Paquette, A. Caruso, S. Bellinger, L. Voss, and R. Allen, “DSRD-IES Pulsed-Power Generator Topology Study Using Machine-Learning-Based Feature Selection Optimization and Predictive Learning” (Poster)

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[20] S. Shepard and A. Caruso, “Tubular Core Optical Power Amplifier” (Poster)

[21] H. Thompson, M. Paquette, and A. Caruso, “Minimizing On-State Resistance in GaN:X Photoconductive Semiconductor Switches (PCSSs) for Direct Modulation (Poster)

[22] A. Usenko, J. Eifler, S. Roy, G. Bhattarai, M. Hyde, M. Paquette, A. Caruso, S. Bellinger, L. Voss, and R. Allen, “New Paradigm in Fabrication of Semiconductor Opening Switches for Pulsed Power” (Poster)

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[23] S. Bellinger, A. Caruso, A. Usenko, “Stacked Diodes for Pulsed Power Applications: New Process Integration Scheme,” 240th Electrochemical Society Meeting, Orlando, FL, Oct. 10–14, 2021 (submitted, oral).

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[24] W. Azad, S. Roy, and F. Khan, “A Four-State Capacitively Coupled High-Voltage Switch Powered by a Single Gate Driver,” *47th IEEE Conference on Plasma Science*, Singapore, December 6-10, 2020 (oral).

[25] J. Hunter, S. Xia, A. Harmon, A. Hassan, V. Khilkevich, and D. Beetner, “Simulation-Driven Statistical Characterization of Electromagnetic Coupling to UAVS,” *Annual Directed Energy Science and Technology Symposium*, March 2020 (abstract appeared, but talk cancelled due to pandemic).

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DEPS Posters and Presentations 2020

[26] William Spaeth, Wideband Parallel Plate to Coaxial Cable Taper

[27] Stefan Wagner, Quickly Determining Minimum HPC Source Requirements Using Binary Search

***

GOMAC 2019

[28] Cash Hauptmann, Reduced Recovery Time in SiPCSS Photoconductive Switches

[29] Eliot Myers, Picosecond High Power Switching Technologies

[30] Heather Thompson, GaN Optimization for Use in Photoconductive Switch

***

[28] B. Barman, D. Chatterjee, and A. N. Caruso, “Analytical Models for L-Probe fed Microstrip Antennas,” *Proceedings of the IEEE Antennas and Propagation International Symposium and National Radio Science Meeting*, Atlanta, Georgia, USA, July 7-12, 2019 (1 page URSI Abstract).

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Directed Energy Professional Society (DEPS) Annual Science and Technology Symposium, Destin, Florida, USA, April 2019:

[29] Ryan Butler, Mechanical Challenges of Modular Photoconductive Semiconductor Based HPM Sources

[30] Steve Young, Two-Dimensional Optoelectronic Pulsed Power Switches: Initial Effort

[31] Adam Wagner, Rapid Cost Effective RF Component Prototyping Using 3D Printers

[32] Heather Thompson, Cost to benefit analysis of GaN for Photoconductive Semiconductor Switches

[33] Colby Landwehr, Low Leakage Electroluminescence For Improving SiPCSS Hold Off

[34] James Kovarik, Some Investigations Into Applications Of Electrically Small Antennas As Phased Array Elements

[35] Spencer Fry, Maximizing SiPCSS Efficiency For HPM Sources

[36] Deb Chatterjee, Studies On Antenna Characterization And Propagation Of High Power Pulsed Electromagnetic Waves With Minimal Dispersion

***

DEPS Posters and Presentations 2018

[37] Jeff Scully, ElectroLuminescence Studies of Silicon Based Photo-Switches

[38] Cash Hauptmann, Thermal Anlaysis of a PCSS through TCAD Simulation

[39] Nicholas Flippin, Fast Rise Time Switches: Drift Step Recovery Diode

***

DEPS Posters and Presentations 2017

[40] Noah Kramer, Recent Results of Silicon Based Photoconductive Solid State Switches for 500kHz Continuous Pulse Repetition Frequency

11.5 Theses and Dissertations

[1] John Keerthi Paul Bhamidipati, “Pulse Generation, Shaping, and Optimization Solutions for Solid-State-Switch-Enabled High-Power Microwave Generation Systems” PhD Dissertation in Physics and Electrical Engineering, University of Missouri-Kansas City, **2022**.

[2] Jordan N. Berg, “Development of a Jet Impingement Thermal Management System for a Semiconductor Device with the Implementation of Dielectric Nanofluids,” MS Thesis in Mechanical Engineering, University of Missouri-Kansas City, **2021** [mospace].

[3] James C. Kovarik, “Wideband High-Power Transmission Line Pulse Transformers,” MS Thesis in Electrical Engineering, **2021** [mospace].

[4] Wasekul Azad, “Development of Pulsed Power Sources Using Self-Sustaining Nonlinear Transmission Lines and High-Voltage Solid-State Switches,” PhD Dissertation in Electrical Engineering, **2021** [mospace].

[5] Paul Klappa, “Implementation and Assessment of State Estimation Algorithms in Simulation and Real-World Applications,” MS Thesis in Mechanical Engineering, **2021** [mospace].

11.6 IP Disclosures Filed

[1] S. Bellinger, A. Caruso, A. Usenko, US Provisional Patent Application “Stacked Diode with Side Passivation and Method of Making the Same,” 12AUG2021.

[2] S. Bellinger, A. Caruso, A. Usenko, “Diode and Method of Making the Same,” 28JUNE2021.

[3] Bhamidipati, Myers, Caruso, “Multi-Stage Photo-Stimulated WBG-PCSS Driven RF Pulse Generation System Implementing Miniature Optical Sources,” 21UMK009, 04NOV2020.

[4] Shepard, “A Low Noise Optical Amplifier,” 21UMK007, 14SEPT2020.

[5] Shepard, “A Novel Optical Fiber Amplifier,” 20UMK012, 02JUN2020.

[6] Doynov, “High-power High Repetition Rate Microwaves Generation with Differentially Driven Antenna,” 20UMK011, 19APR2020.

[7] Doynov, “Scalable Modular System for High-power Microwaves Generation,” 20UMK010, 19APR2020.

[8] Doynov, “Pulse Differential High-power Microwave Generation,” 19UMK007, 02JAN2019.

[9] Doynov, “Non-linear Network Topologies with Reutilized DC and Low-frequency Signal,” 19UMK008, 28DEC2018.

[10] Doynov, Caruso, “Non-Linear Transmission Line Topologies for Improved Output,” 19UMK005, 28SEPT2018

11.7 Provisional Patents Filed

[1] S. Bellinger, A. Caruso, A. Usenko, US Provisional Patent Application “Stacked Diode with Side Passivation and Method of Making the Same,” filed 09/10/2021.

[2] S. Bellinger, A. Caruso, A. Usenko, “Diode and Method of Making the Same” US Provisional Patent Application 63/216,550, filed June 30, 2021.

[3] P. Doynov, A. Caruso, “High-Efficiency High-Power Microwave Generation using Multipass Non-Linear Network Topologies,” filed 26NOV2019.

[4] Plamen Doynov, James Prager, Tim Ziemba, Anthony N. Caruso, “Non-Linear Transmission Line Topologies for Improved Output”, USPTO Provisional Serial No. 62/737,185, filed 27SEPT2018.

11.8 Non-Provisional Patents Filed

None to date

ONR HPM Program – Monthly Status Report (MSR) – August 2022

Anthony Caruso – Univ. Missouri – Kansas City

N00014-17-1-3016 [OSPRES Grant]

Period of Performance – 30SEPT2017–29SEPT2022

ONR Short Pulse Research, Evaluation and non-SWaP Demonstration for C-sUAS Study

15 SEPT 2022

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OSPRES Grant Security: All efforts should be fundamental and publicly releasable in nature when taken individually. This report has been reviewed for operational security, compilation, proprietary and pre-decisional information concerns.

1 Contents

2 Executive Summary

2.1 Progress, Significant Findings, and Impact

Fiber Laser and Optical Amplifiers. We explored various ways of analyzing the impact of tubular resonators on RF horn antennas (as well as modeling optical power amplifier tubes enclosed in a metallic sheath). The most productive model is found to be that based on reflection coefficients and wave impedances. By transforming the wave impedance of the outer wall through the materials in the tube, we can predict the main influences on the overall mode. For the case of an air-load (relevant for a tube not touching the metallic wall) we find that the in-band resonances (at multiples of 1.875 GHz, arising from the radius of the tube) can be dramatically influenced by the out-of-band resonances (starting at 50 GHz, arising from the wall thickness of the tube). In the case of a copper-load (for a tube touching the metallic wall), however, the out-of-band resonances have no impact. Having an analytic model provides a valuable design tool since the parameter space is too large for optimization via simulation alone.

DSRD Optimization Simulations. A preliminary silicon avalanche shaper (SAS) SPICE model has been developed, which adds voltage collapse to the standard diode model within the CMC diode model of SmartSpice by altering the Verilog-A code. LTspice DSRD parameter fitting for the DSRD inventory based on improved forward IV measurements is being completed.

DSRD Design of Experiments. IV measurements were completed for the outstanding EG and Gen2 DSRDs, along with a VMI diode and new Gen2.3 DSRD received from SPT. Analysis of the measurements showed that the Gen2 DSRD were generally more conductive than the EG DSRD. When compared to all Gen2 DSRD, Gen2.3 DSRD were found to have lower on-state resistance and voltage drop and more consistent CV due to improved gold-plating of the devices. Analysis of the characterization and pulser data showed on-state resistance and voltage drop have been more critical determiners in pulser performance than breakdown.

DSRD-Based Pulsed Power Source Optimization. We have been working on testing a 1×1 DSRD-based pulser with different sets of 7-stack diodes to achieve 10 kV peak voltage. However, the maximum output voltage obtained to date is 9.2 kV as reported in the July 2022 MSR. The discrepancy between simulated and experimental output could be linked to inaccurate measurement of inductance of the custom-built inductors. We have tested and characterized several COTS inductors using impedance spectroscopy and found that the error in measurement of nH-range inductance is more than 50%. To reduce the error in the inductance measurement, a custom-designed inductance measurement fixture is under construction.

Pulse-Compression-Based Signal Amplification. LTSpice simulations were continued with the magnetic pulse compression (MPC) circuit modified for continuous-wave (CW) input. Initial simulations show x10 power amplification and provide proof of concept. More theoretical and experimental work is needed for the optimization and realization of MPC power amplification with CW input at high frequencies. Time-reversal-based pulse compression (TR PC) methods were re-evaluated as an alternative signal amplification

method through in-depth discussions with our collaborator. Initial discussions indicate that gain, both in the time and frequency domains, can be achieved when short pulses or CW waveforms pulsed with very narrow pulse widths are used as the source for the one-bit (OB) TR PC system. More in-depth study is needed to determine if OBTR-PC could provide signal amplification for a pulsed GaN source.

Antennas. Manufacturing of an improved version of a tapered, coaxial-connector-fed, single, microstrip, patch antenna element is underway and is expected to mitigate the fabrication errors encountered in the first iteration of the prototype. A successful testing of the improved prototype will be followed by manufacturing of the final demonstrable 4×4 array.

The proposed partial dielectric transformer integrated to Koshelev antenna (single element) has been successfully prototyped, and the agreement between measured and simulated reflection coefficient (S_{11}) is more than satisfactory over the range 300 MHz to 5 GHz. The proposed antenna design exceeds the state-of-the-art Koshelev antenna design by achieving a wider bandwidth ratio (16:1) and higher boresight gain (≈4 dBi) at 900 MHz. This prototype demonstrates our capability to achieve wider bandwidth and higher antenna gain without increasing physical aperture area, which can radiate short rise time pulses with high efficiency (>90%).

The in-house machine learning (ML)-based graphical user interface (GUI) has been updated to demonstrate the optimum design parameter values for the fractal array antenna. The optimum design parameter values for the fractal array antenna were automatically identified by the GUI that effectively yield maximum possible gain at the center frequency with the minimum physical array aperture area. This effort directly correlates with one of the OSPRES-G requirements, i.e., to perform tradespace study, determine and develop an optimum antenna array shape that yields maximum gain with the lowest possible aperture area. The in-house GUI tool has demonstrated this requirement without spending significant time in optimizing the antenna design unlike conventional electromagnetic (EM) wave simulators.

Summary Reports. We include two sub-project summary reports, Direct RF Modulation using GaN:C and Tradespace Analysis of Ultra-Wide-Band Antenna Elements in Appendices B and C, respectively.

2.2 Completed, Ongoing, and Cancelled Sub-Efforts

	Start	End
2.2.1 *Ongoing Sub-Efforts*		
GaN:C Modeling and Optimization	OCT 2017	Present
Diode-Based Non-Linear Transmission Lines	FEB 2018	Present
Trade Space Analysis of Microstrip Patch Arrays	FEB 2019	Present
Lasers and Optics	FEB 2020	Present
UWB Antenna Element Tradespace for Arrays	MAY 2020	Present
Si-PCSS Contact and Cooling Optimization	JAN 2021	Present
Drift-Step Recovery Diode Optimization Simulations	JAN 2021	Present
DSRD-Based IES Pulse Generator Development	APR 2021	Present
Drift-Step Recovery Diode Manufacturing	MAY 2021	Present
DSRD Characterization through Design of Experiments	MAY 2021	Present
Sub-Nanosecond Megawatt Pulse Shaper Alternatives	MAY 2021	Present
Ultra-Compact Integrated Cooling System Development	MAY 2021	Present
Continuous Wave Diode-NLTL Based Comb Generator	SEPT 2021	Present
Pulse-Compression-Based Signal Amplification	DEC 2021	Present
2.2.2 *Completed/Transferred Sub-Efforts*		
Adaptive Design-of-Experiments	OCT 2017	APR 2019
Non-perturbing UAV Diagnostics	OCT 2017	OCT 2018
Noise Injection as HPM Surrogate	OCT 2017	MAR 2019
SiC:N,V Properties (w/ LLNL)	APR 2018	MAR 2019
Helical Antennas and the Fidelity Factor	JUL 2018	SEPT 2019
Si-PCSS Top Contact Optimization	APR 2020	OCT 2020
Nanofluid Heat Transfer Fluid	NOV 2020	JUL 2021
HV Switch Pulsed Chargers	DEC 2018	DEC 2021
Enclosure Effects on RF Coupling	OCT2019	DEC 2021
UAS Engagement M&S	MAR 2021	DEC 2021
GaN-Based Power Amplifier RF Source	AUG 2021	DEC 2021
2.2.3 *Cancelled/Suspended Sub-Efforts*		
Ab Initio Informed TCAD	OCT 2017	OCT 2020
Positive Feedback Non-Linear Transmission Line	NOV 2017	DEC 2018
Minimally Dispersive Waves	FEB 2018	SEPT 2018
Multiferroic-Non-linear Transmission Line	NOV 2018	APR 2019
Avalanche-based PCSS	SEPT 2018	SEPT 2019
Gyromagnetic-NLTL	DEC 2017	NOV 2020
Multi-Stage BPFTL	APR 2020	JUL 2020
Heat Transfer by Jet Impingement	MAY 2018	FEB 2021
Si, SiC, and GaN Modeling and Optimization	NOV 2018	FEB 2021
Bistable Operation of GaN	FEB 2021	MAR 2021
WBG-PCSS Enabled Laser Diode Array Driver	NOV 2020	JAN 2022

2.3 Running Total of Academic and IP Program Output

See Appendix for authors, titles and inventors (this list is continuously being updated)

Students Graduated	*6 BS, 9 MS, 4 PhD*
Journal Publications	*6 (6 submitted/under revision)*
Conference Publications	*35 (3 submitted/accepted)*
External Presentations/Briefings	*40*
Theses and Dissertations	*5*
IP Disclosures Filed	*10*
Provisional Patents Filed	*4*
Non-Provisional Patents Filed	*0*

3 Laser Development

3.1 Fiber Lasers and Optical Amplifiers

(Scott Shepard)

3.1.1 *Problem Statement, Approach, and Context*

Primary Problem: High-average-power 1064-nm picosecond lasers are too large (over 1100 cm^3/W) and too expensive (over \$1000/μJ per pulse) for PCSS (photoconductive semiconductor switch) embodiments of HPM-based defense systems. For example, a laser of this class might occupy a volume of 1 m x 30 cm x 30 cm = 90,000 cm^3 and provide an average power of 50 W (thus, 1800 cm^3/W). Costs in this class range from \$100K to \$300K to drive our Si-PCSS applications.

Solution Space: Optically pumped ytterbium-doped optical fiber amplifiers, fed by a low-power stable seed laser diode, can offer a cost-effective, low-weight, and small-volume solution (with respect to traditional fiber and traditional free-space laser designs). Moreover, our novel optical amplifier tubes, might operate at far higher power levels (over 1000 times greater), thus driving an entire array of PCSS with a single amplifier and thereby reducing the overall system costs and eliminating the optical pulse-to-pulse jitter constraints.

Sub-Problem (1): Optical pump power system costs account for over 50% of the budget for each laser (in this class, for normal/free-space, optical fiber, and tubular embodiments).

Sub-Problem (2): Fiber (as well as power tube) optical amplifier performance is degraded primarily by amplified spontaneous emission (ASE) noise, which limits the operating power point, and by nonlinearities, which distort the optical pulse shapes.

State-of-the-Art (SOTA): Free-space NdYAG lasers or Ytterbium-doped fiber amplifiers optimized for LIDAR, cutting, and other applications.

Deficiency in the SOTA: Optical pump power system costs (in either free-space or fiber lasers) are prohibitive for the PCSS applications until reduced by a factor of at least two.

Solution Proposed: Fiber lasers permit a pre-burst optical pumping technique (wherein we pump at a lower level over a longer time) which can reduce pumping costs by a factor of at least ten. To address the ASE and nonlinear impairments, we are pursuing the use of gain saturation and a staged design of different fiber diameters. We also apply these techniques to fiber amplifiers which incorporate our power amplifier tube in the final stage. The inclusion of our novel tubular-core power amplifier stage should permit a single laser to trigger an array of several PCSS (reducing system cost and mitigating timing jitter).

Relevance to OSPRES Grant Objective: The enhancement in SWaP-C^2 for the laser system enables PCSS systems for viable deployment via: a factor of 40 in pumping cost reduction of each laser; and a factor of *N* in system cost reductions as a single laser could drive *N* (at least 12) PCSS in an array, while also eliminating the optical jitter constraints.

Risks, Payoffs, and Challenges: Optically pumping outside the laser pulse burst time can enhance the ASE; pump costs could be reduced by 40, but ASE in the presence of dispersion and/or nonlinearities could enhance timing jitter thereby limiting steerability. The main challenge for power tube implementation is the entrance optics design.

3.1.2 *Tasks and Milestones / Timeline / Status*

(A) Devise a pre-burst optical pumping scheme by which we can reduce the costs of the laser by a factor of two or more and calculate the resulting increase in ASE. / FEB–JUL 2020 / Completed.

(B) Reduce the ASE via gain saturation. / Oct 2020 / Completed.

(C) Design saturable gain devices which avoid nonlinear damage. / Ongoing.

(D) Calculate and ensure that timing jitter remains less than +/-15 ps with a probability greater than 0.9. / Ongoing.

(E) Demonstrate a cost-reduced fiber laser: the level of success to be quantified via the amount of ASE growth per duration of a pre-burst pumping interval. Growth of 100 uw over 6 ms (the limit in theory) would be considered outstanding. / August 2022.

(E1) March 2021 Finalize design. / Completed.
(E2) April 2021 Assemble and test-check seed LD (laser diode)/driver. / Completed.
(E3) April 2021 Measure power vs current transfer function of seed LD/driver. / Completed.
(E4) May–July 2021 Measure ASE and jitter of 1064 nm seed LD/driver. / Completed.
(E5) May–July 2021 Measure ASE and jitter of 1030 nm seed LD/driver. / Completed.
(E6) June–July 2021 Assemble and test-check pump LDs/drivers. / Completed.
(E7) June–July 2021 Measure power vs current transfer function of pump LDs/drivers. / Completed.
(E8) July–September 2021 Splice power combiners to Yb doped preamp fiber. /Completed.
(E9) July–September 2021 Connect seed and pumps to power combiners and test-check. / Completed.
(E10) September–October 2021 Measure gain, ASE and jitter of 1064 nm preamp assembly (forward, backward and bidirectional pumping) as a function of pump power and duty cycle. / Partially completed before task eliminated.
(E11) September–October 2021 Measure gain, ASE and jitter of 1030 nm preamp assembly (forward, backward and bidirectional pumping) as a function of pump power and duty cycle. / Partially completed before task eliminated.
(E12) November 2021 Splice power amplifier and its power combiner to best preamp. / Partially completed before task eliminated.
(E13) May–August 2022 Measure gain, ASE and jitter of entire amp assembly. / Ongoing.
(E14) May–August 2022 Analyze data and document. / Ongoing.

(F) Design a new type of higher power, tubular core fiber amplifier. / May–August 2022.

(F1) Apply one high-power tubular amplifier to a system comprised of an array of several (say N) PCSS. For example: N=12 in a 3x4 array (or 4x4 array with corners omitted) N=16 in a 4x4 array, etc.; thereby eliminating jitter constraints and reducing laser system cost by more than a factor of 100 (independent of burst profile). / August 2022.

(F2) Design a high power, multiple tube optical amplifier and determine if it permits advantages for power handling or beam profile. / August 2022 / Initiated.

(G1) Design a beam shaping, optical power combiner using a cladding of 6 tubes. / June 2022 / Completed.

(G1.1) Develop COMSOL models. / April 2022 / Completed.

(G1.2) Discover and optimize the length at which the cladding modes couple maximal power into the core mode (of the entire waveguide). / June 2022 / Completed.

(G2) Design a beam shaping, optical power combiner using a cladding of 6 tubes surrounding one inner tube. / July 2022 / Completed.

(G2.1) Develop COMSOL models. / April 2022 / Completed.

(G2.2) Discover and optimize the length at which the cladding modes couple maximal power into the inner tube. / July 2022 / Completed.

(G3) Develop spectral combiners based on multiple-tube waveguides and compare to existing PCF (photonic crystal fiber) technologies. / August 2022 / Completed.

3.1.3 *Progress Made Since Last Report*

(F2) Our high-power multiple tube power amplifiers are similar to our power combiners in the sense that the research at optical frequencies, on capillary-sized tubes [hundreds of microns] can run in parallel with the pursuit of a means of extending such techniques to horn antennas (and their feed waveguides) via larger sized tubes [ones of centimeters] at RF frequencies (e.g., 600 MHz – 6 GHz). At RF or optical we mode-couple multiple tubes (passive at RF, active at optical) within an overall metallic sheath (a.k.a. outer waveguide wall). We examined a simple model in which the tubes function as Fabry-Perot resonators which permit (or inhibit) field penetration to the outer wall when conditions are on (or off) resonance. A more complicated model only yields closed-form approximations in limiting cases and the most productive model is found to be that based on reflection coefficients and wave impedances. By transforming the wave impedance of the outer wall through the materials in the tube we can predict the main influences on the overall mode structure (finer details still requiring simulation due to the curved surfaces). Having an analytic model provides a valuable design tool since the parameter space is too large for optimization via simulation alone.

3.1.4 *Technical Results*

(F2) Glass tubes lining the copper walls of a rectangular waveguide are depicted in Fig.3.1.1. Such a geometry would hold if: 1) we are using the *transverse* resonance effects of the passive (non-amplifying) tubes to affect the overall waveguide mode pattern at RF; or 2) if the glass tubes are Yb-doped optical amplifiers within a metallic sheath. In either case a simple model of the tubes as a Fabry-Perot resonator is limited because it

neglects the wave nature of the diffracting beams scattering off of curved reflectors within a 2D rectangular structure. Moreover, the basic concept of a transfer function (as in circuit theory or optics) is of limited use because we have waves going in both directions (equivalent to having a source at the output port as well as the input port). Another way of seeing the problem is to note that modeling the tube as a layer of glass, then air, then glass (like a Fabry-Perot) is limited because it would ignore the wave impedance of what follows the second layer of glass. In the case of our real tube this could be metal (where they touch) or more air (where the glass tube isn't touching the metal wall). To understand the reflective properties of the glass tubes we therefore begin by modeling them as 3 sections of different transmission lines terminated in a load of either: close to a short circuit (metal) or close to an open circuit (air).

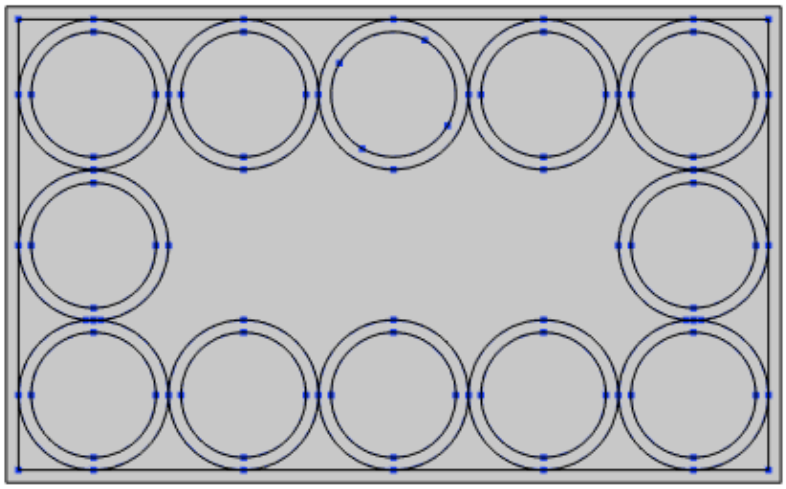

Fig. 3.1.1. Glass tubes lining the copper walls of a rectangular waveguide.

In the case of a short circuit load (appropriate for copper at RF frequencies) we can take the reflection coefficient at the outer wall as $\Gamma_w \sim -1$, which we transform back through a glass wall of thickness d to $\Gamma(-\mathrm{d}) = \Gamma_w e^{-jkd}$ but $2\pi d \ll \lambda$ because d is 1/10 cm, so this is still ~ -1. Thus $Z_g(-d) \sim 0$ becomes the load for the next section of waveguide which is of length = 2 r_c (where r_c is the inner radius of the glass tube) and characteristic impedance $Z_{0n} = 377/n$ [ohms] and n is the index of the material inside the tube (1 in air). Because r_c is 1 cm we do get observable, i.e., in-band, resonances at 3.25 (m) GHz, where m = 1, 3, 5… correspond to infinite Z (open circuit) and m = 2, 4, 6… correspond to Z = 0 (short circuit) cases. The resonances associated with the distance d however begin at 50 GHz (assuming an index of 1.5 for glass) and indeed the transformation of Z through another glass wall (of thickness d) only diminishes "infinite" to "large" impedance resonances of $j\,\lambda/(2\,\pi d)$ and "zero" to "small" impedance resonances of $-j(2\,\pi d)/\lambda$. Thus, the impedance presented by our glass tube in contact with a copper wall is dominated by the resonances associated with the radius of the tube, as shown in Fig.3.1.2 (for a frequency range of 0 to 20 GHz).

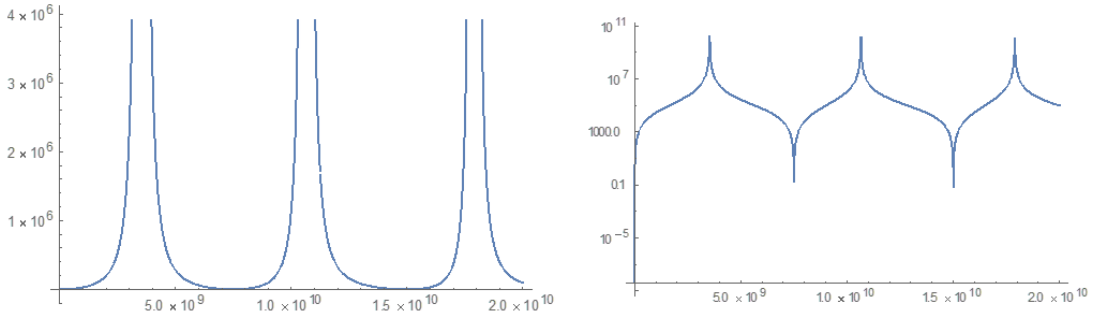

Fig. 3.1.2. Wave impedance presented by an air-filled glass tube with a copper load for a frequency range of 0 to 20 GHz (linear scale on left, logarithmic scale on right).

In the case of closer to an open circuit load (appropriate for a glass-to-air interface) we find the reflection coefficient at the load is $\Gamma_w = -.2$ (for glass of index = 1.5) which we transform back through a glass wall of thickness d to $\Gamma(-\mathrm{d}) = \Gamma_w e^{-jkd}$ and again $Z_g(-d)$ becomes the load for the next section of waveguide, which is of length = 2 r_c and characteristic impedance $Z_{0n} = 377/n$ [ohms]. The final transformation, through another layer of glass of thickness d, yields Z. As shown in Fig. 3.1.3 (on the left for 0 to 20 GHz) we do still get observable, i.e., in-band, resonances near 3.25 (m) GHz, where m = 1, 3, 5… correspond to largest Z; and m = 2, 4, 6… correspond to smallest Z, but the strength of these resonances is greatly diminished and is not constant. The resonances associated with the distance d, which begin at 50 GHz have created an envelope which modifies the r_c resonances, as we clearly see on the right of Fig. 3.1.3 which extends our range out to 200 GHz. The influence of the d resonances was not observable in the perfect conductor loaded case, but in the air loaded case they are clearly of great significance.

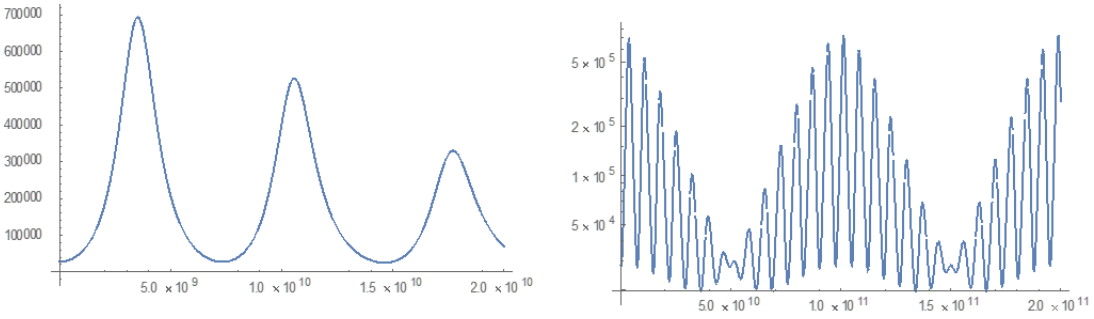

Fig. 3.1.2. Wave impedance presented by an air-filled glass tube with an air load (for a frequency range of 0 to 20 GHz on left; and 0 to 200 GHz on right).

We now alter the index of the material inside the glass tube to n = 2. In the case of the copper load (which functions like a perfect electric conductor, i.e., a short circuit, at these frequencies) this only red-shifts the r_c-based resonant frequencies by a factor of 2, per $f_m = (m\,c)/(8\,n\,r_c)$, where c is the speed of light in a vacuum. In the case of the air load we again find that the d-based resonant frequencies have a dramatic impact (despite the fact that they begin at 50 GHz, which is "out of band" with respect to frequencies from say 1.875 GHz – the lowest f_m for n = 2; up to say around 20 GHz).

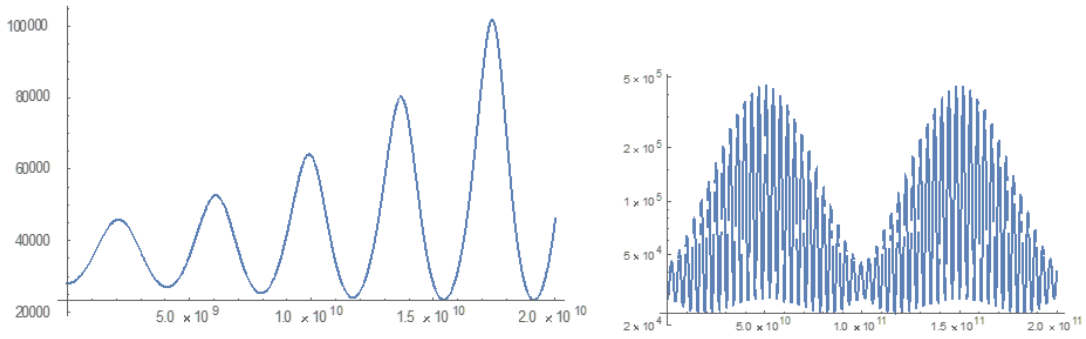

Fig. 3.1.3. Wave impedance presented by an n = 2 material-filled glass tube with an air load (for a frequency range of 0 to 20 GHz on left; and 0 to 200 GHz on right).

Indeed, Fig. 3.1.3 shows that the envelope which *diminished* the in-band resonances with increasing frequency at n = 1, now *increases* the in-band resonances with increasing frequency at n = 2. Control of the index n therefore enables reconfigurability in the bandwidth and center frequency location of transverse resonance enhanced devices such as horn antennas at ones of GHz (and power amplifiers at optical frequencies where we scale all dimensions and wavelengths from centimeters to microns). The wave impedance analytic model provides a valuable design tool since the parameter space is too large for optimization via simulation alone.

3.1.5 *Summary of Significant Findings and Mission Impact*

(A) Our pre-burst optical pumping scheme simulations showed that we can drop the pump power costs by a factor of 40 with pre-burst ASE power levels below the heating level tolerance of 100 μW. UMKC invention disclosure filed 02JUN2020.

(B) For a proposed system gain of 8 million, a linear gain theory predicted the in-burst ASE would be over our heating level spec. by a factor of 3960, but by exploiting the nonlinearity of gain saturation we find that we can suppress the ASE by over 7000. UMKC invention disclosure filed 14SEP2020.

(C) Achieved initial practical device designs that exploit gain saturation, which remained below damage thresholds, via staged designs of different mode diameters NOV2020.

(D) Models of the impact of ASE on timing jitter in the presence of dispersion and/or nonlinearities were established JUL2020.

(E) The design of a proof-of-concept experiment demonstrating a cost-reduced optical pumping scheme was finalized MAR2021.

(F) We made (to our knowledge) the first observation of self-focusing effects that are not determined by beam power alone. We found instead that these can also be controlled via the geometric factors within a waveguide (such as fiber core diameter) MAY2021.

We additionally made (to our knowledge) the first observation that a mode exists in the air within a simple glass tube into which we can couple energy from the mode in

the glass. Thus, an amplifier (in the doped and pumped glass) can operate at higher powers JUNE2021.

We found conditions under which 0.25 GW of power can exist in the tube's air-core mode when its glass-cladding mode is at a power level near 0.5 GW JULY2021.

Advancements in the very high-power operating point (tens of GW) of our tubular optical amplifier (and the existence, size and spatial uniformity of its air-core mode) were shown to permit a single laser to trigger an array of several (up to 100) Si-PCSS – reducing the laser system cost and eliminating the optical timing jitter constraint. The symmetry breaking of the scattering from self-focusing in a curved waveguide was shown to enable such AUG2021.

Complicated entrance optics for the tubular amplifiers greatly simplified by passively splitting (via e.g., a beam splitter such as a microscope slide) a single source into a finite number of "spots" (e.g., 1 or 2 or 4) to illuminate the wall of the tube. We found that with 4 spots of radial polarization we can still achieve GW core and 10 GW cladding power levels SEP2021.

We showed that one device can cover both DoD applications of HMP and HEL by simply changing the operating power point to adjust the output beam profile from almost uniform to almost Gaussian (respectively). UMKC signed NDAs with NKT. Meetings were held with NRL NOV2021.

Smaller core (~ 50 micron) tubular amplifiers enable mechanical flexibility (like a fiber) at diminished thermal capability, so we incorporated water-filled (rather than air-filled) designs capable of 1/10 GW core at 1 MW cladding power levels. We calculated SWaPC improvement examples for the use of a single optical power tube to drive an array of PCSS (relative to a normal free-space implementation of the laser system) finding a cost reduction factor (for a 100 element array) of 83 at reduction in size by a factor of 290. For a 12 element array these improvement factors are 21 and 35 DEC2021.

The use of lower index steam (instead of liquid water) and a staged design, in which the core of each stage also receives an input, increased the power levels by a factor of 10: to 1 GW in the core and 10 MW in the cladding (of these 50 micron core fibers) JAN2022.

(C) Hot spots, i.e., points of high peak-to-average ratio (PAR) of field strength, were discovered. These could lead to damage and thus they restrict the amplifier's operating power. We demonstrate that the locations of these hot spots are set by geometric factors (i.e., the *locations* are set via purely linear effects). The *size* of these PARs however are greatly enhanced by the fiber nonlinearity (from barely observable to factors of ten or more). Linear anti-reflective techniques are inapplicable, so we mitigated this nonlinear enhancement via the effects of gain saturation and obtained a reduction of the PAR by a factor of 10 FEB2022.

(G) Power combiners are important components in high-power fiber laser systems and to that application we leverage our power tube technology; again using a 4 spot input (now with each spot coming from a different laser). We simulated four categories of

input polarization and phasing combinations; and found that the “radial” case (each spot in phase with radial directed polarization) maximizes power transfer into the core. The “phi polarized” case (in which the polarization of each spot is in the direction of increasing angle – tracing out a circle, i.e., to the right on top, down on right, left on bottom, and up on left); minimized power transfer into the core, while confining it primarily inside the cladding MAR2022.

Combiners comprised of 6 or 7 tubes lining the walls of an outer tube resulted in our best-yet Gaussian beam profiles (M2 < 1.13) by exploiting a new type of hollow-core resonance which ensues at operating power just beyond the breakpoint (and thus comes at a cost of a 3 dB reduction of cladding power) APR2022.

Spectral power combiners require broadband transmission windows. We developed an optical transmission design tool/graphic and applied it to our power combiner and passive power delivery design tasks. We show that the mechanical flexibility of fiber (in contrast to a rigid tube) comes with a high price in bandwidth and loss, e.g., if we wanted to guarantee over 90% transmission then a commercially available photonic crystal fiber cannot exceed about 2 [m] in length and the spectral bandwidth is limited to roughly 80 nm – a far cry below the 300 nm of bandwidth that a water-filled tube could provide at that same length MAY2022.

By extending the length of the waveguides in our simulations we have revealed new physics, including the surprising creation of high intensity surface waves at the air/glass interfaces. These strikingly narrow spikes or pencil beams could be exploited in Directed Energy systems due to their highly localized nature. These are special waves which “hug” the material interface (rather than reflect from it) as do so-called “creeping waves” which have been observed previously, but such require conductivity. To our knowledge this is the first prediction that something similar can happen at a non-conducting dielectric interface. Such effects must be readily transferrable to RF radiators as well because they exist even in the case of the absence of a Kerr nonlinearity. Metallic tubes could generate creeping waves at RF but surface waves from glass would improve the SWaP JUN2022.

We show that surface waves can be generated at RF by lining the walls of a copper rectangular waveguide with glass tubes and that the lengths required are compatible with the dimensions of a rectangular feed to a dual-ridge horn antenna. Such photonic crystal effects have enhanced the gain of patch antennas and we have opened the door to applying these transverse resonances to higher power antennas JUL2022.

We simultaneously analyze the impact of tubular resonators on RF horn antennas; while we also model optical power amplifier tubes enclosed in a metallic sheath. By transforming the wave impedance of the outer wall through the materials in the tube we characterize their impact on the overall mode. For an air-load (tube not touching metal) we find that the in-band resonances (at multiples of 1.875 GHz, arising from the radius of the tube) can be dramatically influenced by the out-of-band resonances (starting at 50 GHz, arising from the wall thickness of the tube). For a copper-load (tube touching the metallic wall) however, the out-of-band resonances have no impact. Having an analytic model provides a valuable design tool since the parameter space is too large for optimization via simulation alone AUG2022.

4 Photoconductive Switch Innovation

4.1 Characterizing and Optimizing On-State Resistance in GaN:X PCSS

(Heather Thompson)

Work is currently focused on manuscript preparation. Please see the April 2022 MSR for the most up-to-date summary of this project.

5 Drift-Step-Recovery-Diode-Based Source Alternatives

5.1 Drift-Step Recovery Diode and Pulse Shaping Device Optimization

(Jay Eifler)

5.1.1 *Problem Statement, Approach, and Context*

Primary Problem: Drift-step recovery diodes (DSRDs) and DSRD-based pulsed power systems are competitive with PCSS-based systems for HPM cUAS, with the benefit of not requiring a laser. Maximizing peak power while maintaining characteristic ns-order DSRD rise times requires optimization of the DSRD device design and pulser. Other considerations are for compactness, low-jitter, cooling required, and additional pulse-sharpening device within the pulse shaping head circuit. Additional goals for pulse repetition frequency are also to be satisfied for various applications.

Solution Space: By altering DSRD device parameters (geometry, doping, irradiation), optimize single-die and stack designs for peak power and risetime within various inductive pulser circuit topologies. Also optimize the pulse sharpening device (PSD) within the pulse shaping head circuit.

Sub-Problem 1: TCAD and SPICE models of the DSRD are inaccurate and must be improved. PSD models have not been developed.

Sub-Problem 2: Inductive pulser designs are complicated by the DSRD (and PSD) parameter variability. Use TCAD and/or SPICE models to account for variability and improve pulser design.

State-of-the-Art (SOTA): MW peak power and ns-order risetimes have been achieved in DSRD-based pulsed-power systems employing DSRD stacks for higher voltage holding and parallel lines of DSRD to increase current. PSD have sharpened DSRD pulses to 100 ps-order.

Deficiency in the SOTA: A lack of accurate TCAD and SPICE models make design of DSRD and DSRD-based inductive pulser circuit topologies (with or without PSDs) difficult to the level of tens of MW of peak power while maintaining ns-order risetime (or sharpened 100 ps-order). In addition, DSRD (and PSD) fabrication variabilities further complicate pulser design.

Solution Proposed: Develop further modeling capabilities in TCAD and SPICE for DSRD and DSRD-based inductive pulser circuit topologies to optimize DSRD and inductive pulser designs, especially for maximum peak power and minimum risetime, but also for low-jitter, reduced cooling, and compactness. Additionally, optimize pulser with PSD and pulse shaping head circuit.

Relevance to OSPRES Grant Objective: DSRD-based systems eliminate laser requirements necessary for PCSSs and are competitive in terms of thermal requirements and peak power. With sharpening, the DSRD-based systems can produce comparable risetimes. The SWaPC^2 cooling requirements of HPM cUAS systems can be solved with DSRD-based pulsed power systems, and low-jitter DSRD-based systems can be used for beam-steering in phased-arrays.

Risks, Payoffs, and Challenges: DSRD must be arrayed and staged to increase current since DSRD are limited in their ability to operate at high current densities. DSRD and PSD must also be stacked to operate at high voltages necessary for high peak power and maintain low risetimes. The stacking methods can damage dies and produce variable results in risetime and DSRD diffused doping profiles can be difficult to achieve and may require epitaxial methods. SPICE device models for DSRD are unavailable and must be developed, and questions remain about TCAD limitations for DSRD and PSD modeling.

5.1.2 Tasks and Milestones / Timeline / Status

(A) Milestone – Develop DSRD SPICE model within SmartSpice using the CMC diode model (built-in and Verilog-A).

1. Task – Develop accurate forward IV, reverse CV and reverse recovery testing (RRT) modeling in CMC diode model using either built-in (faster) or Verilog-A (customizable) models; On-going [APR-JUN 2022];

2. Task – Develop reverse IV and forward CV modeling and parameters in SmartSpice CMC diode models (built-in and/or Verilog-A); Preliminary exploration [MAY-JUL 2022];

3. Task – Develop 1x1 DSRD-based pulser recovery parameters within CMC diode model of SmartSpice (built-in or Verilog-A) and compare to RRT parameters; On-going [APR-JUL 2022];

(B) Milestone – Complete LTSPICE parameterization of the standard diode model for DSRD inventory.

1. Task – Finish Gen2.2 DSRD LTSPICE parameter extraction; On-going as received [APR-MAY 2022];

(C) Milestone – Develop automated fitting procedures for developed LTSPICE and/or SmartSpice DSRD models.

1. Task – Improve speed/accuracy/size of brute force fitting methods for LTSPICE and SmartSpice diode models; On-going [APR-JUN 2022];

2. Task – Improve python-based fitting methods for diode models used in LTSPICE and/or SmartSpice; On-going [APR-JUN 2022];

3. Task – Improve use of SmartSpice Optimizer for parameter fitting of diode models; On-going [APR-JUN 2022];

4. Task – Develop automated fitting procedures for Verilog-A diode models (CMC or custom); Preliminary exploration [APR-AUG 2022];

(D) Milestone – Convert manufacturer PSPICE and PSPICE/LTSPICE unencrypted device models into SmartSpice format for use in DSRD-based pulser simulation.

1. Task – Convert unencrypted PSPICE/LTSPICE Cree MOSFET model into SmartSpice format; On-going [APR-JUN 2022];

2. Task – Convert unencrypted Texas Instruments Gate Driver model from PSPICE into SmartSpice format; On-going [APR-JUN 2022];

(E) Milestone – Develop DSRD parameters for 2450 and new 371 semiconductor analyzer measurement data (forward IV and reverse IV).

1. Task – Develop standard diode LTSPICE 371A semiconductor analyzer measurement data parameters; On-going [APR-JUN 2022];

2. Task – Develop SmartSpice CMC (Verilog-A) 371A semiconductor analyzer measurement data parameters; On-going [APR-JUN 2022];

(F) Milestone – Determine performance of doping profiles within TCAD

1. Task – Determine TCAD performance of SOS, dynistor and thyristor doping profiles; Doping profiles not yet received; [?-? 2022];

2. Task – Determine TCAD performance of square root DSRD doping profiles; Not yet begun [? 2022];

3. Task – Determine TCAD performance of Gen3 manufacturer doping profiles; Not yet begun [? 2022];

4. Task – Determine recovery behavior of DSRD doping profiles within TCAD for development of custom Verilog-A CMC-based DSRD models; Not yet begun [?-? 2022];

5. Task – Determine effect of doping and defects on DSRD forward IV performance; Not yet begun [?-? 2022].

5.1.3 *Progress Made Since Last Report*

(A) Develop Silicon Avalanche Shaper (SAS) SPICE model

A quasi-SAS SPICE model, based on the SmartSpice CMC diode model, has been developed as a diode model but allowing voltage collapse of the diode after breakdown and is a preliminary demonstration of voltage collapse as it occurs in SAS.

(E) LTspice Parameter Fitting for 2450/371 Forward IV

The LTspice standard diode model parameters are being fit for the DSRD inventory for the new 2450/371 forward IV data. With the refitting of the forward IV data, the other parameters for CV and RRT must also be refit.

5.1.4 *Technical Results*

(A) Develop Silicon Avalanche Shaper (SAS) SPICE model

For SPICE modeling and design optimization of the DSRD pulser systems, a silicon avalanche shaper (SAS) SPICE model is needed but no such model is available. Some preliminary work has been performed on SAS models with TCAD following [1]. A SmartSpice quasi-SAS model has been developed to compare to these published results. The SmartSpice CMC diode Verilog-A model code has been modified simply to allow a voltage collapse of the diode after breakdown. This voltage collapse is not a feature of the breakdown models available in the standard diode models (or as modified for Zener

diodes). Some issues with coding prevented using the breakdown voltage as the condition for voltage collapse (will be implemented in future models), so simulation time was used in the Verilog-A code as an easy way to provide a condition for voltage collapse. The voltage collapse is accomplished by setting the breakdown voltage (set with CMC diode parameter VBR) to a low value after the higher static breakdown voltage has been achieved. In Figure 5.1.1 is shown the input voltage, voltage across the SAS, and voltage at the 50 Ω load (the SAS and load resistor are in series with the input voltage pulse source).

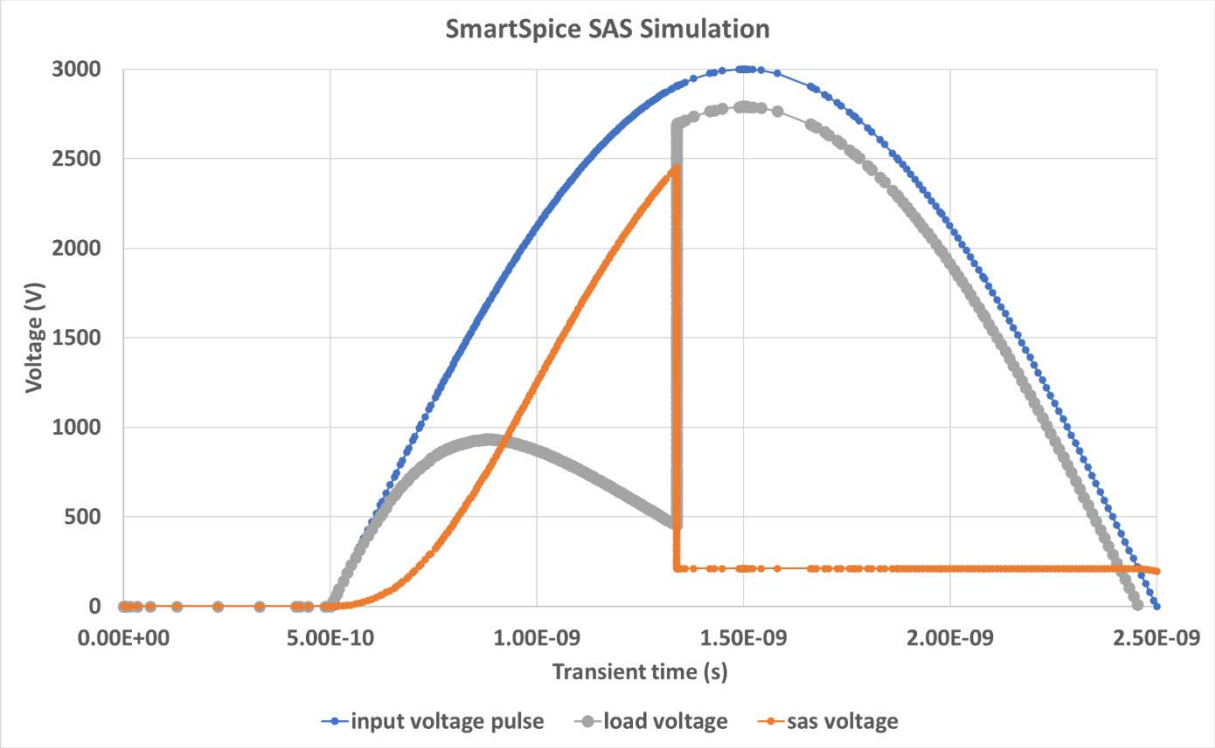

Figure 5.1.1. Quasi-SAS SPICE model shows voltage collapse across the SAS (orange) and the concomitant voltage rise at the load.

The voltage input is a 2.5 ns halfwave sinusoidal oscillation with a voltage peak of 3000 V representative of a DSRD input into a SAS with sufficiently voltage riserate. At 1.33 ns the voltage collapse is triggered in the Verilog-A code by resetting the breakdown voltage and the voltage across the SAS is seen to collapse (orange). The load voltage rises with the SAS voltage collapse (grey). To produce these results the static breakdown curves were matched between the LTspice standard diode model and SmartSpice CMC diode model by adjusting the slope after breakdown (adjusted FREV parameter from 1e3 to 2e10). As well, the zero-bias junction capacitance (CJO) was adjusted to match the SAS riserate seen in the published TCAD SAS example. The initial breakdown voltage (VBR) is also set to produce breakdown at 2450 V as in the published example. The voltage collapse breakdown sets VBR to 30 V.

This SAS SPICE model is preliminary and only produces a voltage collapse as seen in SAS devices but not included in the standard or CMC diode models (or for Zener diode models). A large amount of effort remains to capture the known SAS behaviors. For example, the riserate at the load has not been set to any realistic values or what it would depend on in the model (this riserate is the sharpening capability of the SAS). Future work will incorporate known, published SAS properties beyond voltage collapse to give a more realistic SAS SPICE model.

(E) LTspice Parameter Fitting for 2450/371 Forward IV

New data from forward IV measurement is being fit in the LTspice standard diode model. With refitting the forward IV to the Keithley 2450 Sourcemeter and Tektronik 371 semiconductor analyzer data, CV and reverse recovery testing (RRT) will also need to be refit. The EG-series diodes have been fit in LTspice for the 2450/371 data and the parameters completed thus far are shown in Table 5.1.1. The CV parameters are still in the process of fitting and must follow the forward IV fit within the standard diode model. RRT will also need to be refit (not shown) but ultimately the DSRD pulser simulations determine if adjustments to the transit time (TT) are necessary beyond the RRT fitting. The fits to the 2450/371 data for the EG-series are inherently not very close (not shown) since the shape of the EG-series curve cannot be captured in the standard diode model (a sectional model within the CMC diode model has been developed to fit this shape of forward IV).

The Gen2 DSRD are also being fit to the new 2450/371 data. While the shape of this forward IV can be captured in the standard diode model or the CMC diode model (without a sectional model), there have been some difficulties in getting a very close fit. But very close fits have been achieved and the fitting process is in progress.

The EG and Gen2 DSRD will first be fit for forward IV (near completion) and then the CV will be fit (partially complete) and then RRT (not necessary for pulser sims as transit time is reset to pulser results). As seen in Table 5.1.1 the DSRD were fit for forward IV and CV that were more recently tested in the pulser (as 3x7 stacking of 7-stack DSRD to achieve 10 kV peak voltage at the load). Using the RRT as previously fit (ranges from 4e-6 to 1.6e-5) and choosing 1e-5 transit time for all 7-stacks, the DSRD pulser simulations were not seen to match experiment well. Surprisingly, the 140 V and 750 ns trigger duration for the maximum peak voltage at load seen (8.8 kV) matched very well. But at other trigger durations and prime voltages the results differed. By adding series resistance representative of the 3x7 press-stacking, the pulser simulations in LTspice showed some similarity over with experiment in that the peak voltage was seen to rise only with increasing trigger duration (as well as the DSRD current in forward bias was seen to be more damped). While the underlying model has been improved, deficiencies in the recovery model and actual series resistance cause the LTspce model to differ from experiment.

Diode	IS	N	IKF	RS	Error-2450	Error-371	CJO (pF)	M	Error-Cap
eg1563	1.70E-07	1.60	0.037	0.04	3.72E-03	6.08	4503.40	0.36	5.06E-12
eg1564	1.50E-07	1.60	0.037	0.04	5.08E-03	6.32	4464.44		
eg1565	1.30E-07	1.60	0.037	0.09	5.64E-03	6.53			
eg1566	3.00E-10	1.10	0.031	0.03	3.46E-03	3.86			
eg1567	1.10E-07	1.60	0.028	0.03	3.83E-03	5.01			
eg1568	3.00E-10	1.10	0.019	0.02	6.52E-03	4.40			
eg1569	9.00E-08	1.60	0.037	0.10	4.15E-03	7.93			
eg1570	1.90E-07	1.70	0.037	0.05	3.51E-03	6.92			
eg1571	5.00E-09	1.30	0.040	0.04	1.58E-03	3.86	4494.08	0.36	5.15E-12
eg1572	5.00E-09	1.30	0.031	0.03	2.04E-03	4.65	4488.95	0.35	7.46E-12
eg1573	3.00E-10	1.10	0.016	0.03	2.28E-03	5.34	4459.72	0.32	4.62E-12
eg1574	5.00E-09	1.30	0.025	0.04	2.30E-03	4.52			
eg1602	9.00E-08	1.10	0.034	0.04	3.57E-03	6.57			
eg1603	1.90E-07	1.70	0.028	0.08	5.72E-03	11.71			
eg1604	3.00E-09	1.00	0.013	0.03	3.74E-03	4.41	5718.52	0.45	1.37E-11
eg1605	3.00E-09	1.20	0.019	0.05	1.74E-03	3.04	4515.52	0.38	8.08E-12
eg1606	1.00E-10	1.00	0.007	0.02	5.94E-03	6.15	4358.83	0.43	7.36E-12
eg1607	5.00E-08	1.50	0.037	0.04	3.14E-03	4.43			
eg1608	1.50E-07	1.60	0.040	0.04	3.19E-03	4.98			
eg1609	1.00E-10	1.00	0.013	0.03	6.80E-03	3.58	4513.26	0.34	2.08E-12
eg1610	1.90E-07	1.70	0.028	0.06	6.18E-03	9.96			
eg1611	1.00E-10	1.00	0.013	0.03	4.31E-03	3.45			
eg1612	1.10E-07	1.60	0.037	0.05	3.62E-03	7.20			
eg1613	5.00E-08	1.50	0.028	0.03	3.45E-03	5.31	4499.23	0.40	8.34E-12
eg1614	1.50E-07	1.60	0.022	0.10	4.14E-03	9.03			

Table 5.1.1. LTspice forward IV and reverse CV standard diode fitted parameters.

5.1.5 *Summary of Significant Findings and Mission Impact*

(A) Development of DSRD Model Within SmartSpice CMC Diode Model

The SmartSpice circuit simulation software has been received in JAN 2022 and in FEB 2022 the Verilog-A CMC diode code was retrievable from the Si2 organization website. Development immediately began of the CMC diode model for DSRD modeling by producing forward IV, reverse CV and reverse recovery testing simulations and fitting to example DSRD in the inventory. Recovery parameter fitting within the 1x1 DSRD-based pulser has also begun. The capability of the CMC diode model for modeling DSRD can now be assessed. Any deficiencies in the CMC-DSRD model can be improved using the programmable Verilog-A code of the CMC diode model to include DSRD specific modeling equations based on theory, TCAD simulation, experiment and the literature. The Verilog-A code has been modified to allow different fitting parameters for different sections of the curve so that real, experimental forward IV can be accurately fit. Improved forward IV fitting in the Verilog-A CMC diode model will allow for improved pulser simulation. A new SmartSpice CMC Verilog-A diode model has been developed for modeling silicon avalanche shapers (SAS) that adds voltage collapse to the diode model.

(B) LTSPICE Standard Diode Model Parameter Development for DSRD Inventory

DSRD in the inventory of received diodes (legacy, EG and Gen2) have been fit for LTSPICE standard diode model parameters (for forward IV, reverse CV and reverse recovery testing) for use in LTSPICE DSRD-based pulser simulations and to provide another metric for the characterization of the DSRDs in comparison to pulser performance. Some details of the very low voltage and current forward IV have not been fit but the fitting is still very close when visually inspected in non-log format. Reverse IV have not been fit in the standard diode model since it cannot capture the behavior and breakdown has not yet been measured, only estimated. Forward CV measurement are problematic and not fit mostly since the forward CV parameters in the standard diode model are used for recovery modeling. Various methods exist in LTSPICE to improve recovery parameter fitting but are either inadequate (Vp or carrier viscosity) or non-realistic (adjustment of reverse CV parameters) but have produced fits within 10% error for DSRD-based pulser performance. Gen2.2 experimental data has been received fitted within LTspice but there is high, variable series resistance in the Gen2.2 measurements that are being addressed with a new fixture and testing.

(C) Develop Automated Fitting Procedures for LTSPICE and SmartSpice

The current best method of fitting is using a brute force method of running LTSPICE or SmartSpice simulations sweeping over the desired parameter space. The brute force method can produce the most accurate fits but requires long simulation times and cannot be used to explore large parameter spaces easily (which is why more physically-based models using only measurable parameters is derisable). There is ultimately a limit to how quickly and accurately one can develop parameter sets. Another method is to program in the model equations into Python and use their curve fitting tools, however this method cannot incorporate circuit simulation and will therefore be less effective in producing accurate fits but is much faster in simulation time (can depend on how much parameter adjustments affect DSRD-based pulser performance on which method to use). The other fitting method is to use the built-in optimizer within SmartSpice, but the optimizer has not yet produced as good of fits consistently as the brute force method and will take some experience in using well.

(D) Conversion to SmartSpice of Manufacturer Device Models

Unfortunately, manufacturer device models are not openly available in SmartSpice only PSPICE and to some extent LTSPICE (usually converted from PSPICE). Therefore, the available PSPICE and PSPICE/LTSPICE models must be converted to the SmartSpice format, otherwise keeping the model the same. Note that encrypted models cannot be converted into SmartSpice, such models either have to be developed from scratch and either the datasheet or additional experimental tests used (or purchased from Silvaco for SmartSpice if available).

The unencrypted Cree MOSFET model has been converted into SmartSpice and tested within 1x1 DSRD-based pulser simulations and compared to LTSPICE simulations successfully. The unencrypted Texas Instruments gate driver model has also been converted into SmartSpice successfully. One issue with the driver model is it is intended for PSPICE but used often in online discussion in LTSPICE. However, close examination

of the model shows that the model cannot perform correctly in all pin conditions in LTSPICE due to incorrect parameter types used in a voltage-controlled switch within the driver model. The voltage-controlled switch has been correctly implemented in the SmartSpice conversion and can be fixed for the LTSPICE version (Texas Instruments has not responded to inquires). Neither the MOSFET or gate driver models have been extensively diagnostically tested and compared to the datasheets which are often somewhat different to the free provided models (only so accurate).

The United MOSFET model (UF3SC120009K4S) had to be converted from PSPICE format to SmartSpice format. A couple model issues for the use of the model in LTspice were corrected, one which caused the model to not match the datasheet. The conversion to SmartSpice was successful and allowed simulation of the latest DSRD pulser circuit design with new MOSFETs using the CMC DSRD model to be performed successfully.

(E) IV Parameter Development for 371A Semiconductor Analyzer Measurement Data

A 371 semiconductor analyzer has been acquired and setup for forward IV testing with the potential for higher voltage/current reverse IV testing and breakdown. Initially concerns arose about the shape of the forward IV and whether temperature distortion was occurring at the higher voltages and current available with the 371 compared to the 6485 Keithley picoammeter. However, published power diode forward IV have been discovered showing similar forward IV at room temperature. 371 testing will proceed by testing more DSRD and subsequently using thermocouples and/or heat sinks. 371 higher voltage/current forward IV testing is necessary to characterize the DSRD in the diode models to perform correctly in the DSRD-based pulser simulations. How accurate the forward IV must be, has not been determined, as well as, to what extent individual diodes can be reliably distinguished in modeling. A new method for fitting forward IV has been implemented in the CMC Verilog-A diode modeling code that will allow for more accurate fitting of the 371 data for its full range. More rigorous forward IV testing has been implemented incorporating a number of modifications to the forward IV test fixture, cabling and testing methods (2- vs 4-wire) yielding forward IV with definite error bars. Also, lower current and voltage forward IV data are now taken with the Keithley 2450 sourcemeter which has a higher current limit (1 A) than the picoammeter (20 mA). Data collection of the DSRD inventory for forward IV using both the 2450 and 371 has begun and the curves align well for most DSRD. Breakdown testing has also been performed for Gen2 and EG DSRD showing 40% yield for higher breakdown devices needed for DSRD stacking and DSRD pulser testing. The DSRD inventory is being refit within LTspice for diode parameters based on the new 2450/371 forward IV.

(F) TCAD-Based Doping Profile Performance Evaluation

Many DSRD TCAD simulation studies have been performed assessing the doping profiles used for the DSRD manufactured by SPT and in stock (this summary includes work from the past six months). The TCAD modeling has been temporarily on hold as effort is focused toward developing an accurate SPICE DSRD model due to the unavailability of manufacturer device models for MOSFETs and gate drivers within TCAD. A MOSFET model was developed for the Cree MOSFET for use within TCAD but still had some differences when used in pulser simulations, so the development of the DSRD SPICE

model was prioritized so that manufacturer models (for MOSFETs and drivers) could be used.

Doping profiles are forthcoming for various SOS, dynistor and thyristor devices and TCAD will be used to assess their performance. Some interest has been expressed in assessing square-root doping profiles for DSRD. Gen3 doping profiles from the manufacturer have yet to be assessed within TCAD for performance differences with the requested doping profiles. As well, the recovery models within the CMC diode model are themselves based on PIN diode TCAD simulations and TCAD can perform DSRD doping profile specific simulations to determine model equations and parameters. Additionally, the forward IV behavior of our DSRD can be modeled as seen in the 371A semiconductor analyzer mesaurements. TCAD modeling will continue to be of use in device modeling since it is the only way to assess doping profiles.

5.1.6 *References*

[1] Kesar, Amit S., Arie Raizman, Gil Atar, Shoval Zoran, Svetlana Gleizer, Yakov Krasik, and Doron Cohen-Elias. "A fast avalanche Si diode with a 517 μ m low-doped region." *Applied Physics Letters* 117, no. 1 (2020): 013501.

5.2 Pioneering Drift-Step Recovery Diode Processing and Manufacturing

(Alex Usenko)

Detailed reporting for this section is on hold. A summary report of work completed under OSPRES Grant will be provided in a future MSR, and more streamlined reporting may be provided as appropriate. Please see the May 2022 MSR for the most recent progress update.

5.3 Characterization of SOS Diode Performance through DOE Augmentation

(Joseph Reeve-Barker, Jay Eifler & Megan Hyde)

5.3.1 *Problem Statement, Approach, and Context*

Primary Problem: Drift step recovery diodes (DSRDs) are planar diodes that are capable of nanosecond, high-frequency (10–10^3 kHz) pulses [1] with applications as opening switches in inductive energy storage (IES) pulse generation circuits. There is not a clear understanding of the effects DSRD parameters have on overall IES pulser performance. The purpose of this project is to tie the DSRD parameters to its tailored performance requirements.

Solution Space: Leveraging both design of experiment (DOE) and machine learning (ML) capabilities, we will develop a methodology of characterizing and optimizing DSRDs in order to provide fabrication recommendations in the context of application targets.

***Sub-Problem 1*:** We do not yet understand how diode parameters are tied to diode performance.

Sub-Problem 2: There is no standardized method for correlating the diode key performance indicators (KPIs) to the IES pulser generator performance.

Sub-Problem 3: The number of possible inputs for the DOE is expected to be too large, so ML will need to be leveraged in order to guide decision-making processes.

State-of-the-Art (SOTA): Standard diode measurements include curve tracers for forward and reverse IV, impedance spectroscopy for forward and reverse CV, and function generators or, for example, the Avtech pulser for reverse recovery with high voltage and/or high current when necessary. These measurements are used to generate commonly available datasheets for COTS diodes. These standard diode measurements can then be correlated to pulser performance using traditional data analytics.

Deficiency in the SOTA: The standard diode measurements and datasheets do not include pulser performance necessary to evaluate DSRDs. The datasets generated with doping profile assessment (for example spreading resistance profiling), standard diode measurements and pulser performance are too large and complex to leverage traditional data analytics and will benefit from machine learning techniques.

Solution Proposed: Develop a holistic evaluation network for DSRD characterization. This network will include a DOE that will be a continuously evolving model as diode parameters are correlated to pulser performances. Augmenting the DOE will ensure that the model will remain relevant throughout this study as more discoveries are made. Machine learning will be used as the primary decision-making tool for augmenting the DOE. Once the network is established, it will be used to outline the optimal parameters for stacks of DSRDs within an IES pulse generator.

Relevance to OSPRES Grant Objective: Bridging the gap between the theoretical and physical performance of DSRDs enables closing the gap between a low fidelity TRL3 breadboard pulse generation system, and one which is at a high fidelity TRL4 prototype level. At the TRL4 level, the DSRD-IES pulse generator system would be sufficient to replace the costly laser-based Si-PCSS HPM generator without compromise to scalability required to support the Naval afloat mission.

Risks, Payoffs, and Challenges:

Challenges: Traditional predictive analytics will be difficult to correlate with the augmented DOE due to the large volume of data. Machine learning is expected to assist with decision making processes for the DOE, but only if ideal diode characteristics have been established and good data have been used to train the machine learning model.

5.3.2 Tasks and Milestones / Timeline / Status

(A) Milestone – Establish preliminary DOE and standard operating procedure (SOP) for identifying KPIs of DSRDs [*estimated completion by MAR22*].

1. Task – Ascertain current KPIs used to optimize diodes simulated, manufactured, and utilized within the IES pulse generating circuit [completed AUG21];
2. Task – Construct preliminary DOE to acquire data on all KPIs based on Task 1 [*completed FEB22*];

3. Task – Leverage existing Python scripts to process legacy DSRD KPI data [*completed SEP21*];
4. Task – Develop new and review existing SOPs for experimental testing apparatuses used to evaluate individual KPIs and measure their performance [*completed OCT21*];
5. Task – Identify gaps/deficiencies in legacy KPI data, evaluate existing theoretical relationships to bridge gap and minimize DOE if possible [*completed OCT21*];
6. Task – Using SOPs developed in Task 4, acquire experimental data from legacy DSRDs, refine SOP(s), and assess repeatability and reproducibility [*In progress*: *SEP21–MAR22*];

(B) Milestone – Evaluate DSRD performance using the developed SOPs and facilitated by the preliminary DOE [*estimated completion JUL22*].

1. Task – Acquire data on newly manufactured 2nd generation epitaxial DSRDs from Section 5.2 using refined SOPs from Milestone A [*completed JAN22*];
2. Task – Evaluate the precision and power of the DOE [*In progress*: *MAR22–JUL22:*];
3. Task – Develop a DSRD selection guide for the pulser circuit based on the static DC test measurements *[In progress: MAR22–MAY22];*
4. Task – Correlate the static DC test measurements to the performances of the IES pulser circuits and to fabrication procedures [*MAR22–JUN22];*
5. Task – Begin training machine learning model with DSRD data to determine correlations between static DC and pulser testing results [*MAY22–JUL22*];
6. Task – Acquire data on newly manufactured 3rd generation epitaxial DSRDs from Section 5.2 using refined SOPs from Milestone A [*JUL22–SEP22*];

(C) Milestone –DSRD diode network evaluation [*on hold until Milestone B is completed*].

1. Task – Refine Python script to incorporate new correlations based on findings from Milestones A&B [*Est. Summer22*];
2. Task – Amend ML training model with data acquired on new DSRDs (as characterized by Sections 5.1–5.2) to investigate statistical correlation of diode performance [*Est. Summer22*];
3. Task – Work with TCAD simulation team to address discrepancies between the DSRD performance obtained experimentally, and that achieved within simulations [*Est. Summer22*];
4. Task – Collaborate with DSRD manufacturing team to address discrepancies between the DSRD characteristics evaluated experimentally, and that desired by manufacturing process [*Est. Summer22*];
5. Task – Investigate relationships between statistical significance of individual diode KPIs to the peak performance of the IES pulser with the pulse generator team. [*Est. Summer22*];

6. Task – Incorporate findings from Tasks 1–5 into ML model, pinpoint KPI correlations of interest, and provide recommendations to IES sub-teams accordingly [*Est. Summer22*];

(D) Milestone – DSRD diode network evaluation [*on hold until Milestone C is completed*].

1. Task – Augment DOE network to streamline diode evaluation and identify checkpoints/gaps within simulation, manufacturing, and circuit development process to ensure optimal diodes are selected and utilized to produce robust high-fidelity IES pulse generator prototypes [*Est. Fall22*].

5.3.3 *Progress Made Since Last Report*

(A.6) DSRD Standard Diode Testing

Outstanding EG-series and Gen2 DSRD were measured for 2450/371 forward IV. A VMI diode was also characterized for 2450/371 forward IV, picoammeter reverse IV and 4294A CV. Three new Gen2.3 DSRD were received from SPT and were characterized for forward IV, reverse IV, breakdown and CV. The new Gen2.3 DSRD had improved consistency in CV measurement and lower RS/drop due to improved gold-plating of devices. The Gen2 DSRD were seen in analysis to be more conductive than EG-series when normalized for stack height and area. Analysis of the pulser data with the DSRD characterization testing data showed breakdown was less a factor than RS and forward voltage drop in predicting peak power performance in the pulser of the DSRD.

5.3.4 *Technical Results*

(A.6) DSRD Standard Diode Testing

Misplaced EG-series (EG1567, EG1568, EG1569, EG1570) and Gen2 (X-1, X-2, X-3) were measured for their 2450/371 forward IV. In Figure 5.3.1 is shown the normalized curves (with respect to area and stack height) for Gen2 and EG DSRD. Also in the figure, are shown the new forward IV for the missing EG DSRD. One can also see the Gen2 DSRD are generally more conductive (and lower RS and forward drop) than EG DSRD. The EG-series DSRD curves were normalized to the Gen2 curves by dividing the voltage by the stack height and the current by the device area to produce J-V curves. EG DSRD CV were consistent with earlier measurements with only a few differences likely due to damage to the devices from characterization and pulse testing. Further analysis was performed on the experimental DSRD pulser data and DSRD characterization data and preliminarily show breakdown was not the factor in producing differences in pulser performance (peak voltage) of the DSRD pulse tested. The RS and forward voltage drop correlated with the increase in peak power across various trigger durations and prime voltage when the pulser data is taken into account. Several lower RS/drop DSRD exist in our inventory and could produce higher peak voltages, as well, low RS/drop and low breakdown DSRD should exhibit breakdown effects more readily.

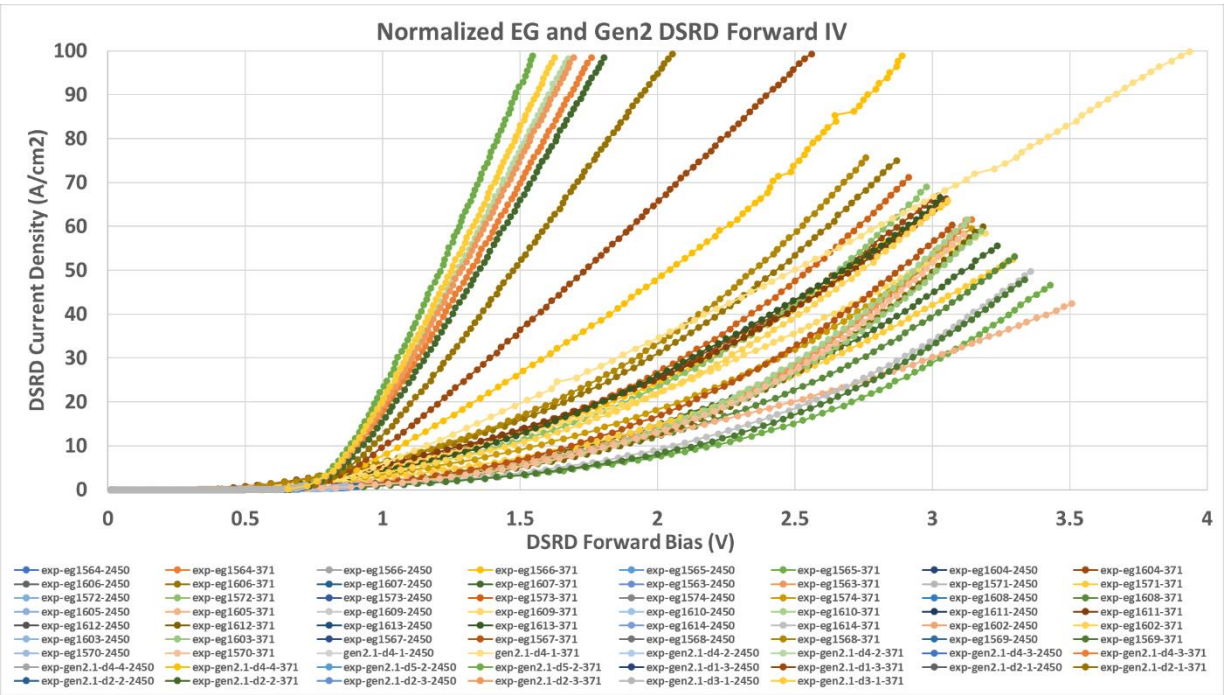

Figure 5.3.1. Normalized forward IV (JV curve) for EG and Gen2 DSRD for comparison. Gen2 DSRD are generally more conductive than the EG DSRD.

New Gen2 DSRD were received from SPT. Three DSRD with much thicker gold-plating than earlier Gen2 were tested for 2450/371 forward IV, pico reverse IV, 371 reverse breakdown, and 4294A CV. In Figure 5.3.2 is shown the Gen2 forward IV (including X-1, X-2, X-3 that were missing) with the new Gen2.3 DSRD as solid triangles and other DSRD as thin lines. The Gen2.3 DSRD can be seen to be highly conductive compared to most of the Gen2 DSRD. This is likely due to the thicker gold-plating (earlier Gen2 DSRD had very little gold). In addition, the CV testing for Gen2.3 DSRD were consistent whereas before with poor gold-plating the CV were inconsistent. It may also be the observed measurement variability for Gen2 371 forward IV has lowered due to the thicker gold-plating. The 371 reverse breakdown showed low breakdown consistent with hi-pot testing performed at SPT. Picoammeter reverse IV (on such low breakdown devices) also yielded consistent low breakdown. The causes and correction of low breakdown are being investigated and corrected in the manufacturing process.

A VMI diode was also characterized for 2450/371 forward IV, reverse IV and CV. Overall, the results were fairly consistent with the datasheet but show differences due to the particular diode used and the measurement setups (data not shown). This indicates that the datasheet may not always provide accurate data especially for SPICE model parameterization (manufacturers recommend testing your own devices for more accurate data). For example, the 2450/371 measured forward IV is more conductive for in-house than datasheet measurement, but we use a 4-wire technique. Earlier 2-wire techniques were much closer to the datasheet but obviously include fixturing resistance. Datasheets may therefore only provide a rough estimation of the performance of actual devices. It

should also be noted manufacturer provided SPICE models only partly match their own datasheets.

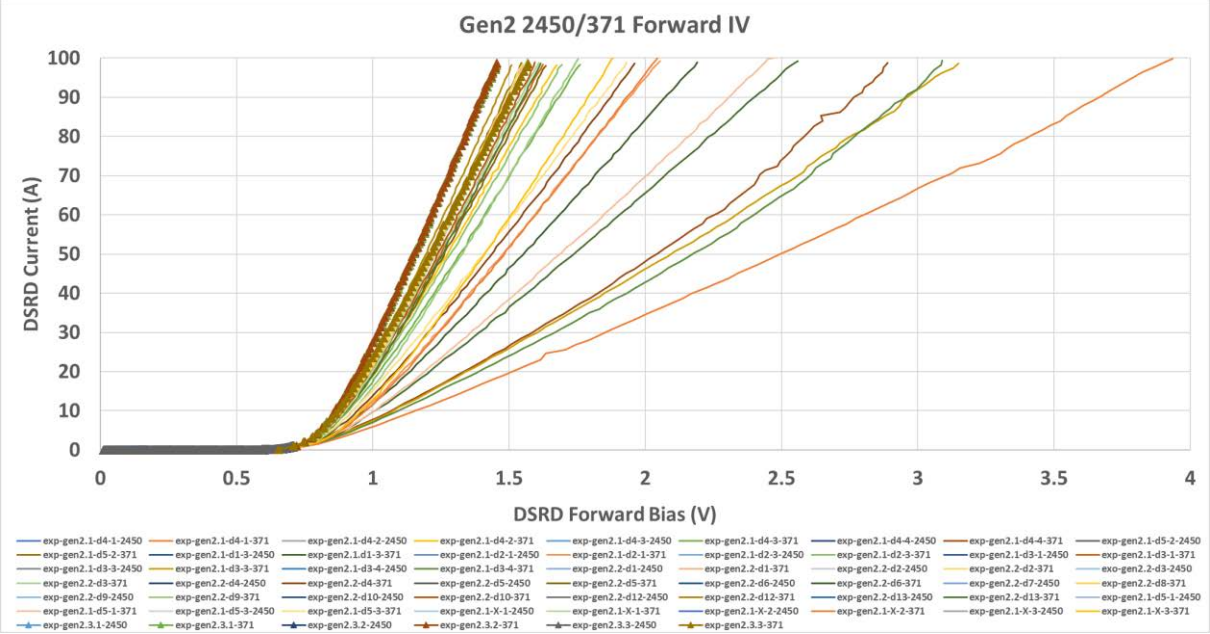

Figure 5.3.2. Gen2 forward IV including X-1, X-2, X-3 DSRD and Gen2.3 (solid triangles). The Gen2.3 diodes are highly conductive.

New equipment for IV and CV testing is being reviewed and demoed from Keithley to improve the accuracy and measurement capabilities.

5.3.5 *Summary of Significant Findings and Mission Impact*

(A.1) Several KPIs have been identified that tie the experimental diode test results to SPICE model simulation parameters. The first KPI is the forward current-voltage (the voltage reading at 10 mA) that is linked to the following SPICE parameters: saturation current, ohmic resistance, emission coefficient, and the forward knee voltage. From the impedance analyzer, the capacitance-voltage measurement is tied to the zero bias junction capacitance and the bottom junction grading coefficient. Both the forward voltage-current and the capacitance-voltage KPIs can be further tied to the SPICE simulation circuit peak voltage performance. The reverse current-voltage (current at -200 V) is linked to the breakdown voltage SPICE parameter. The reverse recovery time measurements, such as the charge storage time and the transition time, are tied to the transit time SPICE parameter and to the full width at half maximum of the pulse signal. Several of these KPIs are not yet associated with specific circuit performances but will require further analysis as outlined in B.4.

(A.2) A preliminary DOE has been developed. The first 6 out of 16 rounds are currently being processed per (A.6).

(A.6) It was found that the test fixture for the picoammeter was causing large variations in the current-voltage measurements due to inconsistent pressure application to the diode. The variation was significantly larger on the Gen2 diodes since they are approximately one-third the height of the 7-stack diodes. A new 3D printed fixture with the ability to apply consistent pressure is expected to drastically reduce the contact resistances and variability that have been introduced to the measurements. New forward IV measurements have produced an averaged measurement with standard deviation error bars. Breakdown testing has shown ~40% of diodes hold at least 500 V per diode in stack. CV testing for series resistance has shown high series resistance associated with the CV test fixture and CV testing in the forward IV fixture may show lower series resistance. Forward IV from the Keithley 2450 and Tektronik 371 have been combined to produce measurements over a larger range of current and voltage necessary to model the DSRD in DSRD-based pulsers. The DSRD EG and Gen2 inventory has been tested for forward IV using both the 2450 and 371 along with breakdown testing in the 371. The data has been successfully used to pick best performing DSRD for the DSRD pulser with experimental 9 kV peak voltage resulting New Gen2.3 DSRD have been tested and show improved RS/drop and more consistent CV measurement due to improved gold-plating. Analysis of pulser data with diode characterization shows RS/drop were important factors determining peak voltage in pulser performance as compared to breakdown.

(B.1) In A.6, it was discovered that the test fixture was the cause of significant variation within the test results, particularly with the Gen2 diodes. Several diodes are scheduled for repeat measurements to determine if all diodes need to be re-tested, which would affect the “completed” status of this milestone.

5.4 DSRD-Based Pulsed Power Source Systematic Topological Optimization

(Shailesh Dhungana & Gyanendra Bhattarai)

5.4.1 *Problem Statement, Approach, and Context*

***Primary Problem*:** Inductive energy storage (IES) and release pulse generators that use drift-step recovery diodes (DSRDs) can be used as the fundamental units of all-solid-state high-power microwave (HPM) systems. The output from DSRD-based pulsers can then be fed into sub-nanosecond pulse sharpeners to achieve ultra-short high-voltage pulses. While DSRD-based pulsers can theoretically achieve the targeted 1's of GW in 1's of ns, their circuits are not topologically optimized to achieve high voltage gain (peak pulse voltage/prime source voltage), thus requiring large and heavy high-voltage (multiple kV) prime power supplies to achieve the required 100's of kV pulses. They also necessitate liquid-based cooling systems to dissipate the excess heat they generate during operation, further adding weight and rendering them impractical for Navy afloat missions.

***Solution Space*:** Systematically develop optimum circuit topology to maximize the voltage gain, and thus the peak voltage, peak power, and volumetric power density of DSRD-based HPM systems. Minimize the heat loss to be able to air cool by increasing energy efficiency through optimization of circuit elements without sacrificing the desired nanosecond risetime of the pulses generated. Air-cooled IES pulse generators using optimum DSRD stacking can remove the need for photo-triggered switches and their laser sub-systems. They are ideal for triggering sub-nanosecond rise-time sharpeners (SAS, D-NLTL, etc.), reducing overall cost, volume, and weight.

***Sub-Problem*:** DSRDs are not domestically available COTs components, but rather manufactured in small-batch quantities, with statistically significant variations in their performance parameters. In addition, our current SPICE models of these diodes may not be accurate due to unknown device parameters such as carrier distribution, carrier lifetime and the limiting current that we can pump without affecting the diode recovery property (see section 5.1 and 5.3) during high-voltage transients. These issues may lead to an inaccurate simulation model of the pulser and discrepancies between simulated and experimental results.

***State-of-the-Art (SOTA)*:** Air-cooled DSRD-based pulsers (equivalent in size to the pulse generators developed for this effort, i.e., ~0.01-m^3, ~2-kg) can achieve <20 kV, 1–2 ns risetime, and <4 ns FWHM across a 50 Ω load with a PRF of <15 kHz in burst mode. Available literature on IES pulse generators only describes a few circuit configurations, and there is a lack of comprehensive investigation of circuit topologies and optimization to achieve maximum gain and efficiency and reduce thermal load. Additionally, these pulsers are expensive and are not available within the United States.

***Solution Proposed*:** Develop different DSRD circuit topologies implementing series and parallel combinations of DSRDs (to increase reverse breakdown voltage and diode current, respectively) to minimize circuit components, such as inductors, capacitors, and switches. Systematically identify the best circuit topology and optimize the circuit components through physics-based DSRD pulser circuit theory and SPICE simulation to

maximize voltage gain and efficiency while minimizing the prime source voltage and thermal load.

Risks, Payoffs, and Challenges:

***Risks*:** All-solid-state DSRD-based IES pulsers require many other electronic components. Most importantly, the current pumping capability of available MOSFETs/electronic switches is limited, which may make maximizing the output voltage impossible even though the DSRDs are capable of higher current and output voltages.

***Payoffs*:** Being able to simulate and fabricate DSRD-based pulsers using physics-based pulser theory, partnered with US-based DSRD manufacturers, will enable a comprehensive domestic ability to optimize, produce, and evaluate these nanosecond pulsers.

***Challenges*:** Domestically manufactured (U.S.-based) DSRDs, which possess sub-optimal doping profiles, may lead to sub-optimal pulse generators. Accurate spice modeling of the diodes could be affected by expected wide variability in the diode characteristics or unavailability of advanced device characterization techniques. Determining the superlative ratio of design/development (through numerical analysis) to the effort put towards experimental testing/evaluation of the DSRD pulser is challenging due to the novelty of the approach. Extending the theory of single (1×1) pulse generator to cascaded (M×N) generator to increase the output will be very complex and may require significant time and computing power.

5.4.2 Tasks and Milestones / Timeline / Status

(A) Milestone – Develop theory of DSRD pulse generator to facilitate optimization of 1×1 pulse generator [***Completed JAN22***]

(B) Milestone – Extend the theory developed in Milestone A to facilitate optimization of M×N pulse generator [**JAN–MAY22** / ***Ongoing***].

(C) Milestone – Construct/demonstrate a DSRD-based 1x1 pulse generator prototype based on theory developed in milestone (A) and obtain performance data for multiple combinations of diode stacks [**JAN–JUN22 / *Ongoing***].

(D) Milestone – Construct/demonstrate a DSRD-based 4×2 IES pulse generator prototype capable of producing $\geq$12 kV peak voltage, $\leq$1 ns risetime, $\leq$5 ns FWHM, $\geq$3 MW peak-power, $\geq$100 kHz PRF, $\geq$1,000 shots-per-burst, $\geq$500 number of bursts [*On hold*].

(E) Milestone – Develop waveform inverter which, when combined with the pulser from Milestone C, enables a balanced differential waveform output with >90% inverted signal fidelity. [***Completed DEC21***].

(F) Milestone – Construct/demonstrate a M×N pulse generator prototype capable of producing $\geq$20 kV peak voltage, $\leq$1 ns risetime, $\leq$2 ns FWHM, $\geq$8 MW peak-power, $\geq$100 kHz PRF, and $\geq 2\sigma_{Vpeak}$, which operates in continuous-burst mode as a viable candidate for OSPRES Contract source alternative [*on hold until Milestones B, D, & E are completed*].

5.4.3 *Progress Made Since Last Report*

(B) We have been developing the theory of a 2×1 DSRD pulser and generalizing it to an M×1 pulser. Simulation of 2×1 pulser shows that parallel stacking increases the output voltage without reaching the MOSFET voltage limitation.

(C) Several standard inductors have been measured and characterized using impedance spectroscopy. Inductors with inductance in the nH range (typically required for pulser fabrication) have the greatest error in measurement due to incorrect fixture compensation. A new inductor measurement fixture is under construction.

5.4.4 *Technical Results*

(C) 1×1 DSRD Pulser Fabrication and Testing

a) Unreliable results of impedance measurements

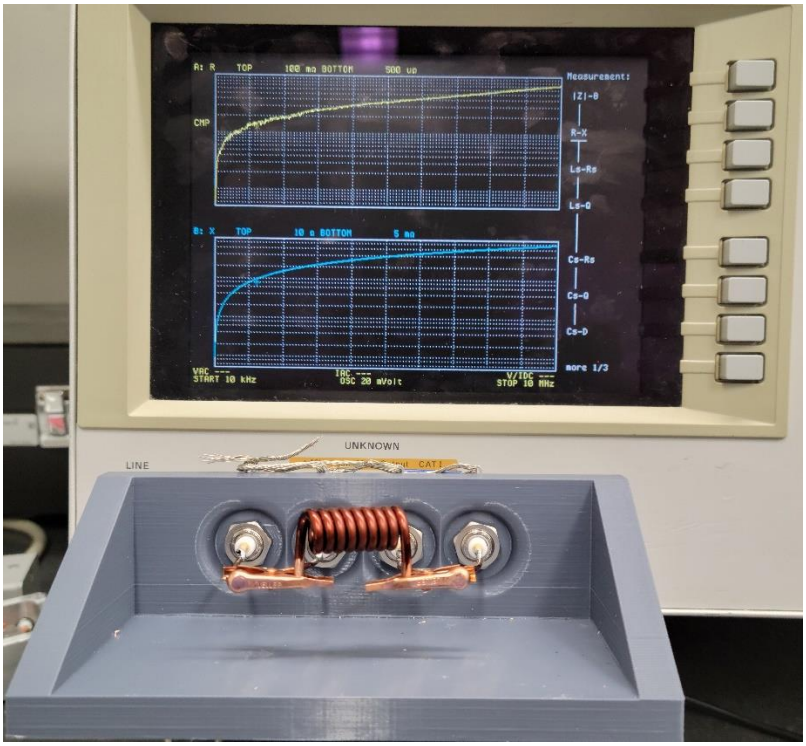

Figure 5.4.1. Experimental set-up to characterize an inductor using a custom-built fixture and an Agilent 4294A Impedance Analyzer.

The Agilent 4294A impedance analyzer was used to measure the inductance of commercially available inductors to test the accuracy/reliability of the equipment and fixture (Figure 5.4.1). It was found that the measured values agreed with the rated inductance values for inductance >1 μH. However, for inductance values <1 μH, the measured inductance values were much lower than the rated values. **Error! Reference source not found.** shows the rated and measured inductance values of some commercial inductors.

Table 5.4.1. Values of rated and measured inductance of commercial inductors.

Rated inductance	Measured inductance
1 mH	0.98 mH
4.7 μH	4.66 μH
68 nH	29.2 nH
66 nH	35.9 nH

As seen from **Error! Reference source not found.**.4.1, the lower inductance values have ~50% error, which we believe is due to parasitics of the fixture and connectors. Like the commercial inductors, the measured inductance of our custom-built inductors differed significantly from their expected values (obtained from Coil64 desktop application). For example, the inductor with an expected inductance of 136 nH was measured as 84.1 nH. Similarly, the inductor with an expected inductance of 158 nH was measured as 96.1 nH. To solve this problem of mismatch between the expected and measured value, we are in the process of building a “better” fixture (Figure 5.4.2), as described in the July 2022 MSR.

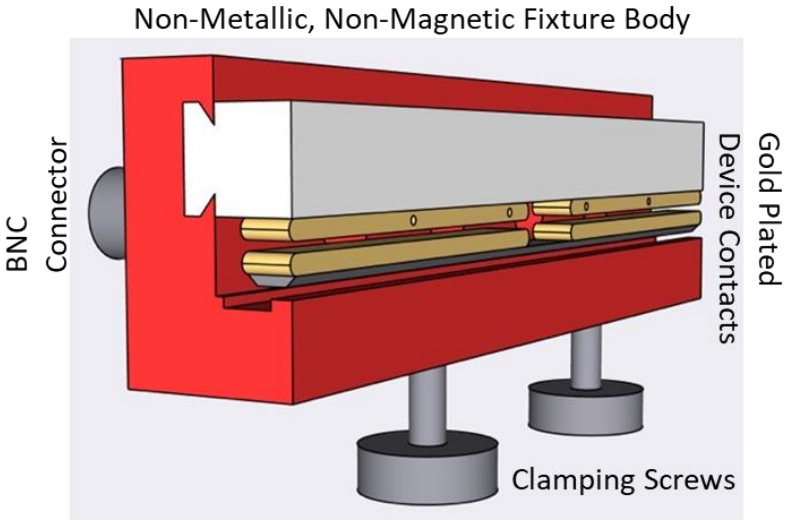

Figure 5.4.2. Inductor measurement fixture designed to have low parasitic capacitance and inductance.

(b) Calculation of inductance and resistance as a function of working frequency

A Python program was written to calculate the inductance and resistance of the inductors as a function of working frequency. The program accepts the diameter of the wire, the length, diameter of the cross-section, number of turns, and the pitch of the solenoid as input parameters and calculates the inductance and resistance of the solenoid. Example plots of the calculated impedance and inductance corresponding to a custom-built inductor are shown in Figure 5.4.1. The input parameters are as follows: length of the solenoid = 1.96 cm, diameter of the cross-section of the solenoid = 0.537 cm, diameter

of the wire = 2.56 mm, number of turns = 6.5. The inductor value of this particular inductor obtained from the Coil64 application was 136 nH.

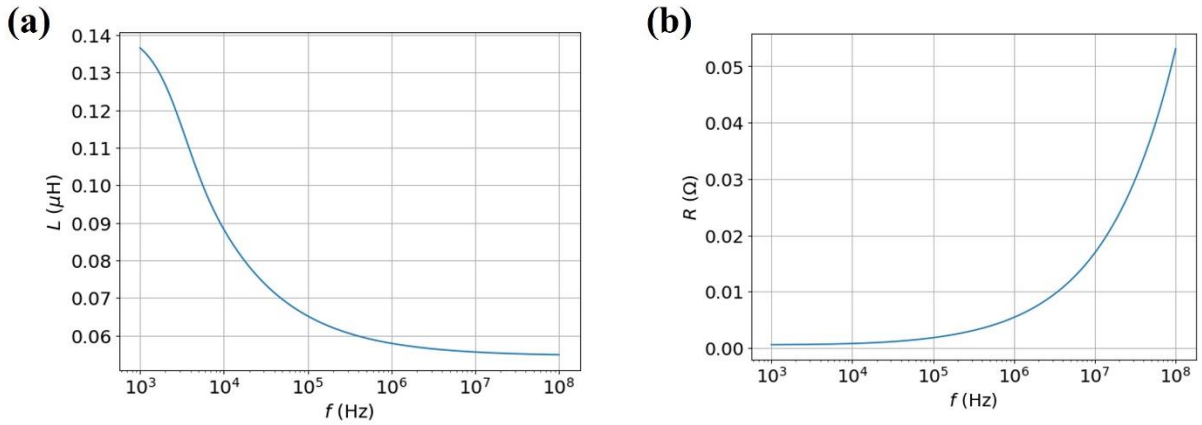

Figure 5.4.3. (a) Calculated inductance as a function of frequency. (b) Calculated resistance as a function of frequency.

5.4.5 *Summary of Significant Findings and Mission Impact*

(B) A systematic optimization of a 1×1 pulse generator based on the theory covered in the DEC2021 MSR reporting period was presented. In this reporting period, we have presented an optimization sequence considering the circuit limitations. Based on the previous measurements and simulations, we hypothesized that the lowered output voltage obtained from the previous pulsers could be due to higher diode ON-state series resistance than the value considered for simulation. A proposed working principle for a two-stage DSRD pulser has been described in the MAY2022 MSR reporting period, however, with certain outstanding questions that may inform the efficacy of multi-stage DSRD pulsers. A new approach for stacking multiple 1×1 pulsers in parallel to increase the output voltage while keeping the MOSFET current and voltage within safe operating limit has been proposed.

(C) Using the 28-stack pulser, maximum peak outputs of 6.7 and 7.5 kV are obtained for a trigger length of 700 ns using a prime source voltage of 120 and 170 V. A newly designed and fabricated pulser with four MOSFETs in parallel achieved an output of 9.2 kV using three 7-stack diodes for a prime source voltage of 140 V and a trigger length of 750 ns. The lower-than-expected output (10 kV) is believed to be due to inaccurate values of custom-built inductors and inaccurate diode on-state resistance. Based on the DSRD pulser output using a single 7-stack diode, the reverse breakdown voltage of the EG1600 series diodes is estimated to be ~650 V. Measurement of circuit voltages at different nodes confirms the circuit performance matching the SPICE simulation. Obtained lower output voltages indicates requirement of more accurate DSRD SPICE Model which takes account of forward

diode series resistance, carrier distribution and recombination during high voltage transients.

(D)

Table 5.4.2. Comparison of DSRD-based IES Pulse Generator Performance.

KPM	Units	MIDE - V1	MIDE - V2	MIDE – V3	MIDE – V4	Kesar *et al.*	MI-PPM0731
		Previous	Previous	Previous	Current	SOTA	COTS
V_{supply}	V	225	180	120	140	300	160
T_{ON}	ns	100	340	700	750	?	200
V_{peak}	kV	5.59	**7.35**	**6.7**	**9.2**	5	6.3
Gain	V/V	24.8	**40.8**	**55.8**	**65.7**	16.7	39.4
$\tau_{rise,20\text{-}90\%}$	ns	1.2	1.1	3.1	5.0	1.96	0.12
dV/dτ	kV/ns	4.66	6.44	2.16	-	2.55	**52.50**
FWHM	ns	2	5.48	6.90	7.8	2.27	0.35
PW	ns	5	7	7	-	3.5	2.5
Z_{LOAD}	Ω	50	50	50	50	50	50
P_{peak}	MW	0.625	**1.080**	**0.905**	**1.692**	0.500	0.794
E_{pp}	mJ	0.125	0.154			0.143	0.318
PRF_{max}	kHz	100	100		100	100	15
Burst	shots	100	100	*N/A*	*N/A*	*N/A*	100
	%	100	100	*N/A*	*N/A*	*N/A*	100
SD_{Vpeak}	σ	> 2	**> 2**	*N/A*	*N/A*	*N/A*	*N/A*
	%	96.5	**97.8**	*N/A*	*N/A*	*N/A*	*N/A*

(E) Successful construction and operation of a 2×2 DSRD-based IES pulse generator prototype has been completed, which meets or exceeds the required key performance metrics. Shown in Table 5.4.2 are the previous and current pulse generator performance specifications in comparison to a similar 2×2 pulser developed by Kesar et al. [1] using DSRDs, and to that of a commercial off-the-shelf (COTS) DSRD pulser of similar space and weight developed by Megaimpulse (i.e., PPM-0731), which also uses DSRDs with silicon avalanche shapers (SAS) [2]. Although the Megaimpulse pulser utilizes a SAS with a <500 ps risetime (a threshold we do not intend to go below due to Commerce Controlled List limitations), it is interesting to compare the results of linear voltage gain and peak power of this system, to that of one that utilizes a SAS. The current permutation of the 2×2 DSRD-IES pulser developed by MIDE under the ONR OSPRES Grant is able to achieve a higher peak voltage and shorter risetime than DSRD-based pulsers reported in the literature of comparable space and weight as well as those commercially available. The ability to generate a linear voltage gain of 65.7 to produce over a Megawatt of

peak power into a 50 Ω load while achieving a peak voltage output standard deviation of 2σ when operating at a PRF of at least 100 kHz, brings this technology to the forefront of viable options to potentially support the Naval afloat mission.

(F) Discrepancies exist in the obtained pulser and device characterization data for different series combinations and different samples of 7-stack DSRDs, which may be attributed to the inconsistencies in their manufacturing process. Future work includes the design and testing of 2×2 or higher configuration DSRD-based pulsers using more combinations of series-connected as well as parallel-connected DSRD stacks.

5.4.6 *References*

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5.5 All-Solid-State Sub-ns MW Pulse Generators with Semiconductor Sharpeners

(Gyanendra Bhattarai)

This sub-project is currently on hold as focus is directed toward Section 5.4. Please review the January 2022 MSR for the most recent project overview and status.

6 Thermal Management

6.1 Ultra-Compact Integrated Cooling System Development

(Sam Sisk, Roy Allen, and Sarvenaz Sobhansarbandi)

6.1.1 *Problem Statement, Approach, and Context*

Primary Problem: A thermal management system (TMS) is required for cooling semiconductor-based pulse-power devices, using anywhere from 50 to 200 W, with the goal of maintaining the semiconductor device temperature below 80 °C to avoid chip damage. The proposed system must increase cooling densities at a rate of at least 1 kW/cm^2, the current state of the art, while decreasing pumping power requirements, in-line with the SWaP-C^2 objective. This device also needs to be small enough to be used anywhere from server warehouses to drones, thus 1 cm^2 is targeted, with scaling up remaining a possibility.

Solution Space: To achieve such high cooling densities, we propose an updated jet impingement TMS (JI-TMS) design. The JI-TMS is expected to achieve an enhanced heat transfer rate due to the turbulent flow from an array of nozzles. The JI-TMS is also expected to have some pressure losses due to the fluid flow path. As the proposed TMS dimensions are restricted to 1 cm^2 surface area, the required pumping power should be kept to a minimum.

Sub-Problem: The turbulency formed from the array of nozzles on the targeted surface creates an extreme pressure loss, which is mainly from the large amount of jet nozzles impinging fluid streams interfering with other fluid streams. The pressure must be sustained to enable proper cooling and circulation processes.

State-of-the-Art (SOTA): Integrated chip cooling is being widely used to dramatically increase the operational power of high-voltage silicon-based power devices. However, the current SOTA devices include surface-to-surface contact points that rely on cohesive connections. These connections increase the amount of material through which heat must transfer to the coolant, thus limiting the heat removal rate.

Objective: To design, simulate, compare through validation with other JI-TMS designs under the same operating conditions, and optimize through an iterative process. The proposed JI-TMS design is based on refining in-chip jet-impingement geometry through leveraging theory of fluid flow and a parametric evaluation of nozzle geometry, flow channel arrangements, and outlet to inlet area ratios. The JI-TMS performance will be compared with the corresponding results available in the literature and with the results from the JI-TMS designs.

Challenges: The manufacturing techniques such as layering needed for a JI-TMS integrated onto a chip are expensive, so other manufacturing techniques should also be explored such as CNC milling. As the proposed compact designs are restricted due to the low tolerances needed for the geometries of the nozzles and heating plate, the manufacturing process must be capable of having a cohesive bond of the TMS and targeted cooling (semiconductor).

Risks: With a system so compact, the pressure drop could be a large issue in the objective to the targeted heat dissipation rate. An extreme pressure drop would potentially cause the coolant to flow backwards, causing less fluid-to-solid interaction.

6.1.2 *Tasks and Milestones / Timeline / Status*

(A) Design a 1 cm^2 Si base JI-TMS to achieve a heat dissipation rate of 1 kW/cm^2. The device will also need to be designed in a way where it can be manufactured as proposed. / MAR22–MAY22 / In Progress

(B) Using the computational fluid dynamics (CFD) ANSYS software, simulate how de-ionized water will react to the applied heat flux and geometry. The operating conditions will remain the same for all geometry design iterations to ensure simulation continuity and useful comparison. / MAY22–JUN22 / In Progress

   a. Compare the results from previous design iterations and make improvements to the designs to meet the target metrics.

   b. This process of looping through (A) and (B) will continue until a design addresses all main and sub problems as well as challenges stated previously; once accomplished that design will be chosen for the next stage of the project.

(C) Using the selected design, perform ANSYS simulations using Si-C nanofluid or other high conductivity fluids as the coolant and see how fluid type changes the effectiveness of the TMS in terms of heat extracted and pressure losses. / June22–JULY22 / Upcoming

   - Prove simulations to be comparable to a real world process. This will be done by validation with other JI-TMS experimental and simulated data from the literature.

(D) After selection and validations of simulated results of the JI-TMS design, manufacture a prototype to begin experimental testing and evaluation./ AUG22–OCT22 / Upcoming

6.1.3 *Progress Made Since Last Report*

(A) Taking what was learned from the previous designs, it was found that deriving the geometric dimensions from the equations found to dictate heat removal behavior was most beneficial. This change in finding a geometry ensures the heat removal rate is high enough to keep the targeted surface under the 80 °C thermal limit.

(B)

(C) Simulations were done at boundary conditions as previously. Due to the simulations being validated and knowing the desired turbulency needed, the velocity as well stayed constant.

6.1.4 *Technical Results*

(A) The third version of the JI-TMS design was achieved using equations from Incropera, as provided below and mainly focusing on matching the required heat transfer coefficient.

Using equations (6) and (7) to calculate the required $\bar{h}$ in order to get $\overline{Nu}$. Knowing the required $\overline{Nu}$ allows for the use of equations (1) to then derive the geometric dimensions. The geometry was tweaked to meet manufacturing tolerances of 0.025 mm.

$$\overline{Nu} = .5K\left(A_r\frac{H}{D}\right)G\left(A_r\frac{H}{D}\right)\mathrm{Re}^{2/3}Pr^{.42} \quad (1)$$

$$K = \left[1+\left(\frac{\frac{H}{D}}{\frac{0.6}{Ar^{.5}}}\right)^6\right]^{-0.05} \quad (2)$$

$$G = 2Ar^{.5}\frac{1-2.2Ar^{.5}}{1+0.2\left(\frac{H}{D}-6\right)Ar^{.5}} \quad (3)$$

$$Ar = \frac{\pi D^2}{2\sqrt{3}S^2} \quad (4)$$

$$Re = \frac{VD}{\nu} \quad (5)$$

$$\overline{Nu} = \frac{\bar{h}D}{k} \rightarrow \bar{h} = \frac{\overline{Nu}*k}{D} \quad (6)$$

$$q = \bar{h}A(\Delta T) \quad (7)$$

$$2000 \leq Re \leq 100{,}000$$

$$2 \leq H/D \leq 12$$

$$.004 \leq Ar \leq .04$$

$$\boxed{\begin{array}{c} 2000 \leq Re \leq 100{,}000 \\ 2 \leq H/D \leq 12 \\ .004 \leq Ar \leq .04 \end{array}}$$

The 0.3 mm diameter nozzles, spaced at the appropriate distance found with Ar, was modeled using SolidWorks where the resulting CAD model isometric cross-section is shown in Figure 6.1.1. The file was then converted into a format that can be simulated with ANSYS FLUENT. The CFD solver's model employed was the Epsilon-k model due to the fluid's turbulent nature as satisfied when Re greater than 2000 and the Energy Model as there was energy transfer within the system. An initial simulation was done at a velocity of 40 m/s shown in Figures 6.1.2-.3, this was done to show that it was a successful trial in limiting the semiconductor contact surface temperature below 80 °C at the desired 1 kW/cm^2 heat flux from the semiconductor.

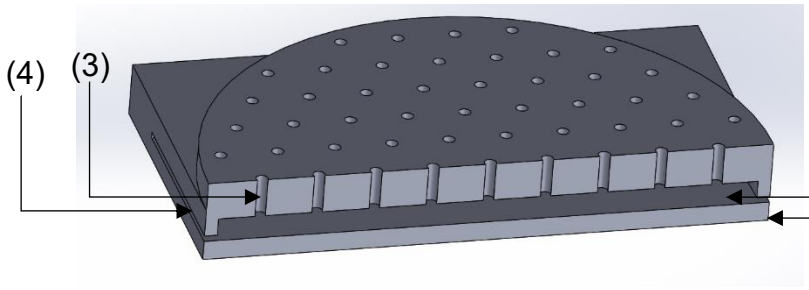

Figure 6.1.1. SolidWorks geometry isometric cross section. (1) Semiconductor contact. (2) Jet impingement contact. (3) Nozzles x81. (4) Fluid outlet x4.

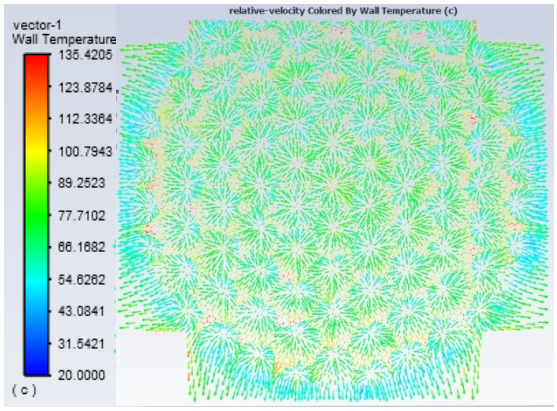

Figure 6.1.2. Top view of jet impingement contact displaying contour plot of velocity vector colored by temperature.

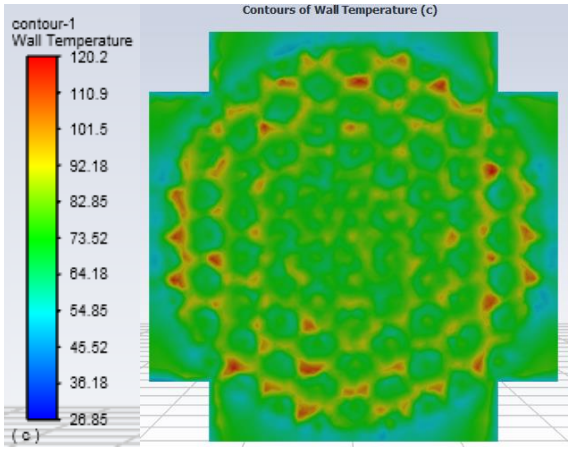

Figure 6.1.3. Top view of jet impingement contact displaying contour plot of temperature.

Semiconductor Wall			Outlets			Outlets		
Min Temp	Max Temp	Avg Temp	Pressure Min	Pressure Max	Pressure Avg	Min Vel	Max Vel	Avg Vel
26.85	120.1851	74.8786	-482362.7	2096615	828882.9	0	46.65291	40.15266

Table 6.1.1. Table of results for 6.1.1 geometry.

6.1.5 *Summary of Significant Findings and Mission Impact*

(A) A new JI-TMS geometry was made to meet all geometrical and calculated cooling demands for the 1 kW/cm^2 heat flux. This geometry shows there will be a decrease in cooling capacity due to the number of nozzles dropping from 200 to 80. This change was made to account for manufacturing tolerances. Moving further there may be a few tweaks such as adding fins to further increase turbulence, which will improve cooling performance.

(B) The simulations done for the second trial of a JI-TMS geometry showed that there was heat removal from the semiconductor and as the jet contact average temperature was 74 °C. The pressure losses from nozzle inlet to outlet was over all low but was not a main focus for this trial of simulations. Going further there will be a focus on minimizing pressure losses.

6.1.6 *References*

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7 Pulse-Forming Networks

7.1 Diode-Based Nonlinear Transmission Lines

(Nicholas Gardner)

Attention on this sub-project is being entirely directed toward the preparation of manuscripts and an associated dissertation. A summary report will be provided in Summer 2022, and this will serve as a placeholder until this time. Please see the January 2022 MSR for the most recent summary and status and the Outputs section for papers in preparation or published.

7.2 Continuous Wave Diode-NLTL based Comb Generator

(Nicholas Gardner and John Bhamidipati)

Work on this sub-project is currently on hold to focus on reporting and other sub-projects. Please see the May 2022 MSR for the most recent summary.

7.3 Pulse-Compression-Based Signal Amplification

(Feyza Berber Halmen)

7.3.1 *Problem Statement, Approach, and Context*

Primary Problem: Solid-state amplifiers, such as gallium-nitride-based high electron mobility transistors (GaN HEMTs), can be used as high power microwave (HPM) sources to achieve the SWAP-C2 performance metrics necessary to support the cUAV Naval afloat mission. However, even the best high-power GaN HEMTs are limited to 2–3 kW of peak power, much lower than the 0.1 to 3 MW pulsed power available from traditional HPM sources such as travelling wave tubes (TWTs). Achieving a power density of 1 W/cm^2 at a distance of 10 m with a high gain (≥ 10 dBi) narrow-band antenna requires an input power increase of two to three orders of magnitude. Power combination methods to achieve an effective radiated power (ERP) at MW scale require 10 s to 100 s of GaN HEMTs, compromising the SWAP-C2 performance.

Solution Space: Pulse compression techniques are used to increase the peak power and lessen the pulse width in HPM applications. Adapting pulse compression at the GaN HEMT or any other SWAP-C2 compatible source output can achieve sufficient ERP with an optimal radiating element.

***Sub-Problem*:** Pulse compression is generally used to generate a pulsed output with a high peak output power (P_{out_peak}) and a wideband frequency content from a DC input voltage. The main challenge lies in identifying a pulse compression technique that can be used to amplify a narrowband RF input signal. Some of the circuit elements for common pulse compression techniques, such as the saturable inductors used for energy storage in magnetic pulse compression (MPC), exhibit increasingly lossy behavior with high frequency. Another challenge will be to determine, if any exist, the operating frequency limits of the suitable pulse compression technique for high-frequency, high-power signals.

State-of-the-Art (SOTA): Large magnetic pulse compression (MPC) circuits (>1 m^3, >1000 lbs) have demonstrated peak output power up to a few GWs. Smaller versions (~0.125 m^3, 50 lbs to 100 lbs) can achieve 7.5 MW peak power [1].

Deficiency in the SOTA: Traditional MPC systems are large (few meters long), leverage huge transformers, and require liquid coolant such as transformer oil, which leads to undesirable system mass values of ≥1000 lbs. They are used for generating medium or high pulse power traditionally from DC or AC (50/60 Hz) high voltage supplies. There is no known example of high-frequency signal amplification utilizing MPC.

Solution Proposed: Developing a pulse compression circuit that will act as a high-power signal amplifier with a gain of ≥10. Utilizing magnetic pulse compression, or any other suitable pulse compression method, for high power signal amplification with source fidelity.

Relevance to OSPRES Grant Objective: Pulse compression will enable a size and cost efficient solution to high power signal amplification that will lead to HPM source development with optimal SWaP-C2 parameters.

Risks, Payoffs, and Challenges:

Challenges: Modeling pulse compression circuits for high-frequency operation can present a challenge. Pulse compression circuits are generally evaluated in SPICE simulators with low-frequency AC / transient simulations. SPICE is a lumped-element model simulator and cannot solve for the distributed-element model required at high frequencies where the wavelengths become comparable to the physical dimensions of the circuit. Some circuit components, such as the saturable inductor in the MPC, are not available in SPICE or many other simulators and need to be modeled using behavioral models and proprietary material data. Pulse compression circuit modeling, especially at high frequencies, needs to be investigated.

Risks: Pulse compression methods are usually lossy in nature and generate a considerable amount of heat; therefore, designing a proper cooling method must be carried out, which may inadvertently increase the volume (size and weight) of the overall design.

7.3.2 *Tasks and Milestones / Timeline / Status*

(A) Milestone – Demonstrate 2–3 times increase in peak power and compression gain using magnetic pulse compression (MPC) [*estimated completion by SEP22*].

1. Subtask – Model saturable inductors in LTSpice or Matlab/Simulink in order to be able to develop MPC simulations / NOV21 / Complete.
2. Subtask – Investigate the operation, design, and pitfalls of MPC circuits / NOV21 / *Ongoing*.
3. Subtask – Design MPC circuit with RF input and simulation in LTSpice or Matlab/Simulink to evaluate the resulting amplification and frequency content. / JUNE22 / *Ongoing*.
4. Subtask – Model the high frequency behavior of MPC circuit / DEC21 / *Ongoing*.

5. Subtask – Build and test the MPC prototype using bench top power supply / OCT21 / *Ongoing*.

(B) Milestone – Investigate pulse compression methods other than MPC for feasibility *Ongoing*

1. Subtask – Study time reversal pulse compression to assess its compatibility with GaN-based source. JUNE22 / Ongoing.

(C) Milestone – Increase the compression gain available from PC.

(D) Milestone – Build and test SWAP-C2 compatible high-frequency PC prototype with GaN source.

7.3.3 *Progress Made Since Last Report*

(A.2) LTSpice simulations were continued with modified magnetic pulse compression (MPC) for continuous-wave input to observe the achievable power amplification.

(B.1) One-bit time reversal pulse compression (OBTR-PC) was re-evaluated through discussions with our collaborator in terms of gain in frequency-domain and gain with pulsed continuous-wave input.

7.3.4 *Technical Results*

(A.2) MPC design equations and procedure were modified for the MPC circuit with sinusoidal input, given in Figure 7.3.1. For the sinusoidal input, the input capacitor is redundant and, therefore, removed from the MPC circuit depicted.

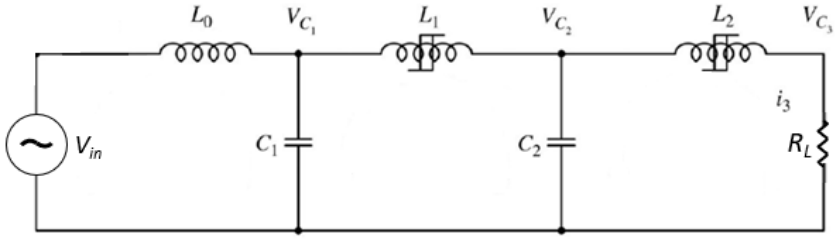


Figure 7.3.1. Circuit schematic for 2-stage MPC circuit with sinusoidal input.

The saturable inductor at the input stage of the MPC proved to be challenging to balance in this initial design cycle and was replaced with a regular inductor with a non-magnetic core. With the L1 in a non-saturated state, i.e., high impedance, the input circuit transfer function is:

$$\frac{V_{C_1}}{V_{in}} = \frac{1}{1 + s^2 L_0 C_1} = \frac{1}{1 - \frac{\omega^2}{\omega_0^2}}\,, \tag{1}$$

where the resonance frequency of ω0 is defined as:

$$\omega_0 = \frac{1}{\sqrt{L_0 C_1}}\,. \tag{2}$$

The other two stages still follow the general MPC design equations included in the previous MSRs.

The initial design is based on the previous 2-stage MPC circuit described in the April and July 2022 MSRs. The input inductor value, L_0, was chosen to provide a compression gain of four between the input stage and the first stage. The input sinewave frequency is equal to the resonance frequency calculated by equation (2). The schematic for the circuit simulated in LTSpice is given in Figure 7.3.2 and the simulation results are included in Figure 7.3.3 (a) and (b).

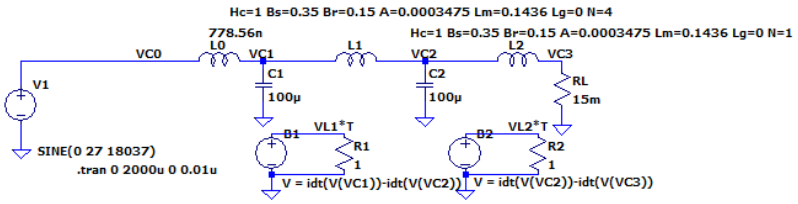
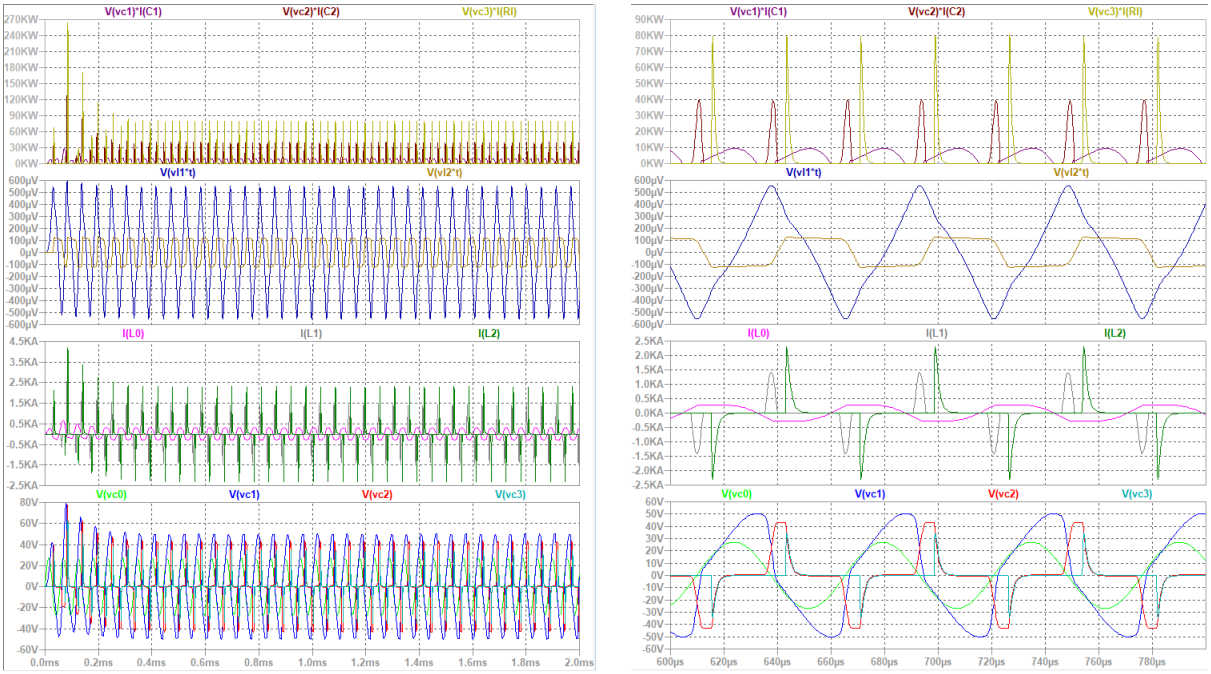


Figure 7.3.2. Circuit schematic for 2-stage MPC circuit with sinusoidal input.



(a) (b)

Figure 7.3.3. (a) 2-stage MPC circuit waveforms for sinewave input and (b) waveform details

Figure 7.3.3 (a) shows that the MPC circuit output settles to expected operation within a few input signal cycles. The operation is quite different than that of the traditional MPC circuit. Unlike traditional MPC, the inductors are saturated in both directions, i.e., positive and negative saturation flux. The time integral of the applied voltage that results in inductor saturation is shown as waveforms V(vl1*t) and V(vl2*t) for inductors L1 and L2, respectively. This results in positive voltage on the capacitors/load and current flow

through the inductors towards the output in the positive sinusoidal cycle and negative capacitor/load voltage and current flow in the opposite direction in the negative cycle. In this design, L1 and L2 do not saturate as soon as their input capacitor node reaches its maximum value, which is evident from the time delay between the current pulses from consecutive stages. This could be optimized in future design cycles. Compression gain of 4 is obtained between the input and 1st stages as designed. The compression gain between the 1st and 2nd stage is reduced to 2 due to resistive loading at the output, as explained in the July 2022 MSR. The input and output voltage, current and power waveforms for this 2-stage MPC circuit with sinusoidal input are given in Figure 7.3.4. The input and output power levels are around 7 kW and 80 kW, respectively, suggesting over 10x increase in power.

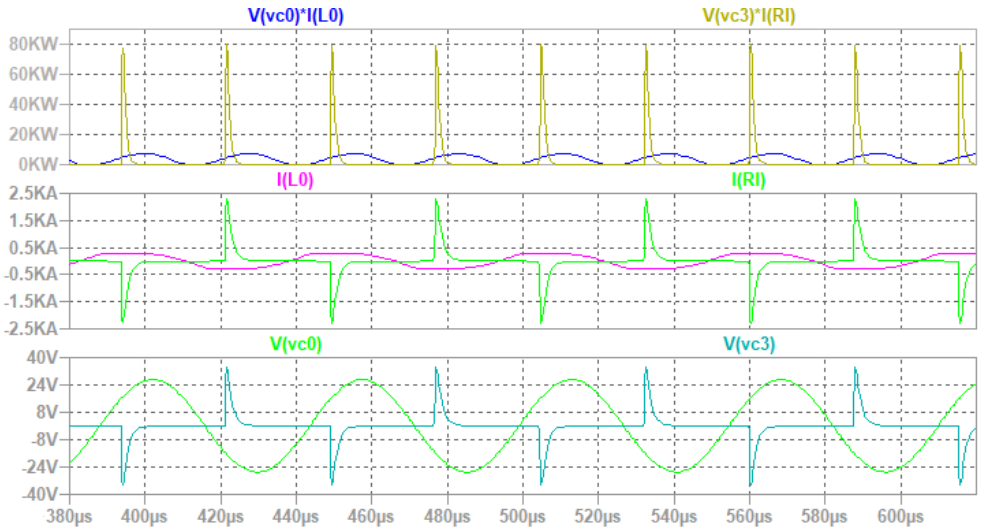


Figure 7.3.4. Input and output voltage, current and power waveforms for 2-stage MPC circuit for sinewave input

The LTSpice simulations show the initial proof of concept for sinusoidal signal power amplification with MPC. More detailed study and experimental work is needed to determine the feasibility of the MPC for this task. Note that the simulations take into account the magnetic core characteristics, which is not included in MPC design equations. However, inductor parasitic components such as core resistivity and winding capacitance are not included in the initial simulations. Also, the circuit is very sensitive to resistive loading and other loading schemes need to be investigated for reliable circuit operation. MPC operating frequency will also be limited by the operating frequency of magnetic cores and requires materials research to extend the operation over 300 MHz.

(B.1) More detailed study of time reversal pulse compression (TR PC) was conducted through in-depth discussions with the collaborator on this topic. The system block diagrams for both TR PC and one-bit time reversal (OBTR) PC are given in Figure 7.3.5 (a) and (b), respectively. For TR-PC, gain is typically defined as the ratio of maximum power level of the reconstructed signal at point C to that of the time reversed (TR) or one-

bit time reversed (OBTR) PC signal at point B. As mentioned in the June 2022 MSR, even though gain is observed in the time domain signal, there is loss in the frequency domain. However, this study is investigating the feasibility of TR PC based methods for signal amplification and the definition of gain should be modified to fit the intended application. When the TR PC based system is used as an amplification block, the impulse input to the system will be replaced with a 'source' and the gain should be defined as the ratio of power levels between points C and A. When the gain is defined as the ratio between the system output and input, a mean gain of more than 20 dB is observed in the frequency domain with an impulse input.

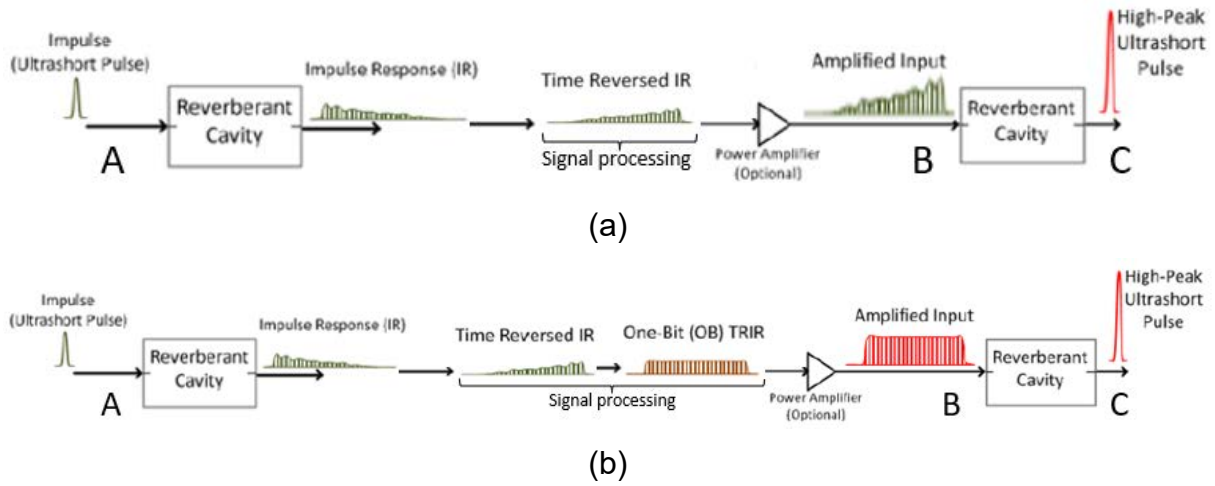


Figure 7.3.5. Architecture of (a) time reversal pulse compression and (b) one-bit time reversal pulse compression systems (adapted from [2]).

If the input to the system is replaced with a source, the gain, C/B, depends on the source type. For sources with narrow pulse width, such as the DSRD, high gain is expected. The gain drops with increasing pulse width. However, significant gain can be obtained for a CW amplifier operated in pulsed mode with narrow pulse widths. Frequency domain gain between input-output, C/A, still needs to be determined to verify the feasibility of OBTR-PC as a "signal amplifier". Details will not be discussed in this MSR due to the nature of the collaboration. OBTR-PC application as a means for signal amplification for solid-state amplifiers could be evaluated as a separate project.

7.3.5 *Summary of Significant Findings and Mission Impact*

(A) Initially a basic 2-stage magnetic pulse compression (MPC) circuit was built and tested with DC input to better understand the MPC principles and considerations such as inductor sizing, pre-pulse currents, and inductor saturation. Next, saturable inductor modeling was realized in LTSpice with inductor flux expression and the Chan model [2]. Prior to MPC system simulations, magnetic core losses were investigated, and core selection constraints were determined based on the core losses and high-frequency MPC design considerations. Next, different magnetic core materials were investigated to determine the most suitable candidate for high-frequency MPC. As reported previously, such a core should have high resistance, narrow hysteresis loop,

minimized eddy current area, and low saturation flux density (B_{sat}). High permeability (μ) and very sharp saturation characteristics are also preferred in order to minimize pre-pulse currents and resulting MPC gain loss. NiZn ferrites are the best option among the commercially available magnetic cores for the high-frequency MPC application as they have the highest operating frequency, low B_{sat}, and sufficiently high μ. After investigating suitable magnetic cores and their properties, LTSpice simulations of the previously tested 2-stage MPC circuit were resumed using the Chan model for Kemet NiZn cores. The inductor for the input stage was replaced with a magnetic switch based on the simulation results. The effects of core coercivity and remanence on MPC operation, which is not included in the design equations, were simulated, and high remanence and low coercivity were found to result in the lowest leakage currents due to sharper saturation behavior. A prototype B-H curve tracer was also built in order to characterize the magnetic cores that will be used in the MPC circuit. The prototype is now complete with the high voltage section isolated in an enclosure. Measurement of known cores with the B-H curve tracer and analysis of the results are ongoing in order to verify the accuracy of the prototype. A SoW has been drafted with KRI for the design and fabrication of a NiZn-YIG magnetic composite with cutoff frequency of over 500 MHz and relative permeability of 25. Commercial magnetic cores offer the highest cutoff frequency of 350 MHz with relative permeability of only 7.5. New magnetic material development is needed to realize a magnetic switch at higher frequencies. A prototype MPC circuit with continuous-wave input at low frequencies will be fabricated as proof of concept before finalizing the KRI SoW. Commercially available magnetic cores were investigated for their suitability for the MPC prototype operating at kHz to MHz frequency range. Only three magnetic materials are commercially available with a cutoff frequency of 200 MHz and higher. Considering the need for high permeability, sharp saturation, and low coercivity for high compression gain as well as the toroids readily available for purchase, Material 68 from Fair-Rite was selected for the prototype. Prototype design will proceed with the downselected toroids. MPC simulations were continued to observe the effects of resistive loading. Optimal energy transferred is obtained for load resistance matched with output stage impedance, which results in very small, e.g., mΩ range, load resistors. MPC circuit elements and input voltage could be sized to maximize the load resistance, and related design equations were derived. Some voltage and current artifacts due to non-ideal switch behavior were observed with resistive loading. After determining the optimal load resistance for the designed MPC circuit, it was modified to operate with sinusoidal input. Initial simulations show stable operation after a few cycles of settling behavior. 10x power amplification is obtained with the design, providing proof of concept for sinusoidal signal power amplification with MPC. More theoretical and experimental work is needed for realization of MPC power amplification with CW input at high frequencies..

(B) Time reversal pulse compression (TR PC) was investigated as an alternative PC-based signal amplification method. TR PC shows a few dBs of gain in the time domain but loss in the frequency domain as its main component, the resonant cavity, is a passive and lossy circuit element. One-bit time reversal (OBTR) PC, which increases the time domain gain to ≥20 dB, shows ~3x gain in the frequency domain at some

frequencies but completely distorts the output signal due to the digitization process. The impulse response record time significantly affects the compression gain and limits the pulse repetition frequency. The compression gain also drops significantly for narrowband signals. Time-reversal-based pulse compression methods were therefore found to be incompatible with a GaN source, especially due to their limited PRF and low compression gain for narrowband signals. OBTR PC is re-evaluated as an alternative PC-based signal amplification method through discussions with our collaborator. Significant time domain gain is observed with one-bit (OB) TR PC when a continuous-wave (CW) source is pulsed with very narrow pulse widths. The frequency domain waveforms have not yet been investigated for this case. However, more than 20 dB gain is observed in the frequency domain if the gain is re-defined as the ratio between the input impulse and the output reconstructed pulse for the evaluation of OBTR-PC as a “signal amplifier”. More in-depth study is needed to determine if OBTR-PC could provide signal amplification for a pulsed GaN source.

7.3.6 *References*

[1] D. Zhang, Y. Zhou, J. Wang and P. Yan, "A compact, high repetition-rate, nanosecond pulse generator based on magnetic pulse compression system," in IEEE Transactions on Dielectrics and Electrical Insulation, vol. 18, no. 4, pp. 1151-1157, August 2011, doi: 10.1109/TDEI.2011.5976109.

[2] S.K. Hong, E. Lathrop, V.M. Mendez, and J. Kim, “Ultrashort microwave pulse generation by passive pulse compression in a compact reverberant cavity”, in Progress in Electromagnetics Research, vol. 153, pp. 113-121, 2015

8 Antenna Development

8.1 Tradespace Analysis of an Array of Electrically Small Antennas (ESAs)

(Bidisha Barman and Deb Chatterjee)

8.1.1 *Problem Statement, Approach, and Context*

Primary Problem: Determine the extent to which the physical aperture size of an antenna array, composed of patch elements, can be reduced, while maintaining performance in peak power density, bandwidth, and electronic beam steerability over the UHF range (0.4–1 GHz), compared with present-art high-power-microwave-capable antenna arrays.

Solution Space: An array of patch antenna elements whose feed, two-dimensional shape, and relative placement (i.e., intra-, and inter-element design) allow for the physical aperture size to be reduced by more than 20% compared with the present-art.

Sub-Problem: To overcome scan blindness (as the main beam is electronically steered), due to the excitation of surface waves (SW). (Note: scan blindness is a common phenomenon in electrically small microstrip patch antenna arrays).

State-of-the-Art (SOTA): Horn, reflector, Vivaldi, valentine, etc. are some of the commonly used ultra-wideband (UWB) antenna elements in a phased array for high-power microwave (HPM) transmissions.

Deficiency in SOTA: Large physical aperture size of the antennas.

Solution Proposed: Using electrically small antennas (ESAs) as array elements and optimizing their performance in terms of both near-field (bandwidth) and far-field (directivity) parameters, followed by arrangement of the ESAs in suitable lattice structures (preferably, hexagonal/triangular) to reduce the overall array aperture area. Using stochastic and machine learning (ML) algorithms to optimize antenna element and array performance.

Relevance to OSPRES Grant Objective: Provides design and optimization guidelines for UWB ESA elements, especially coaxial probe-fed microstrip patch antennas, and arrays for HPM applications.

8.1.2 *Tasks and Milestones / Timeline / Status*

(A) Develop an Array Pattern Tool in the context of lightweight calculations of large antenna arrays / JAN–MAY 2021 / Completed MATLAB code.

(B) Investigate the effects of array aperture area reduction on different array parameters (such as gain, beamwidth, electronic beam steerability) and present a comparative study of antenna array parameters as a function of array aperture area / JAN–MAY 2021 / Completed.

(C) Build minimum viable validation prototypes of single ESA elements on substrates that have good power handling capabilities for HPM transmissions at UHF range (such as polyethylene, FR-4, TMM-10i, TMM-6) / JAN 2021–JUN 2022 / Ongoing

manufacturing of the updated version of a tapered, coaxial-connector-fed, wideband, rectangular, microstrip patch antenna element (0.7–1.2 GHz).

(D) Optimization of ESA (single element) performance using ML based stochastic search algorithms / JUN 2021–FEB 2022 / Completed single objective optimization of ESA elements.

(E) Build minimum viable validation prototypes for arrays of ESA elements / JUN 2021–SEP 2022 / Completed modeling of the final demonstrable 4×4 array prototype.

(F) Optimization of array performance using ML algorithms / SEP 2021–FEB 2022 / Completed single objective optimization of antenna arrays on infinite ground planes.

8.1.3 *Progress Made Since Last Report*

(C) Build minimum viable validation prototypes of single ESA elements:

a. Ongoing prototyping of an improved version (v2) of the tapered, coaxial-connector-fed, microstrip patch antenna element, for operation in the desired UHF range (0.7–1.2 GHz).

b. Completed 3D printing of the substrate and the insulating section of the tapered, coaxial connector.

c. Metallization of the prototype to be initiated.

8.1.4 *Technical Results*

(C) Build minimum viable validation prototypes of single ESA elements:

As mentioned in the JUN2022 and JUL2022 ONR-OSPRES-Grant reports, the tapered, coaxial-connector-fed, microstrip patch antenna, which was manufactured for operation in the UHF range (0.7–1.2 GHz), had several structural discontinuities. These structural discontinuities originated due to the limited capacity of the SLA printer which restricted printing of the substrate and the tapered connector sections as a single block. This eventually led to EM discontinuities which negatively impacted the antenna's responses, in terms of S_{11}-parameters and realized gain.

To alleviate these discontinuities and help improve the antenna's performance, it was decided to manufacture an improved version of the same prototype. For the second version, a larger SLA printer has been employed to print the substrate and the tapered connector as a single block. In addition to this, an SLA frame, to provide external support to the prototype, has also been modeled. The CAD model of the prototype, with the supporting frame, is shown in Fig. 8.1.1(a).

The manufacturing of the second prototype was initiated in August 2022 with an expected lead time of 1 week. However, due to technical glitches in the 3D printer, the printing failed 3 times and hence took more time than expected. The latest, 3D-printed (4^{th} iteration), tapered, coaxial-connector-fed, substrate block (as a single unit) is shown in Fig. 8.1.1(b). The inner conductor of the tapered-coaxial-connector is being manufactured currently and will be attached to the SLA block for final prototyping. This will be followed by metallization

of the completed structure. A comparison between the experimental and the simulated S_{11} and realized gain data will be provided in the next report.

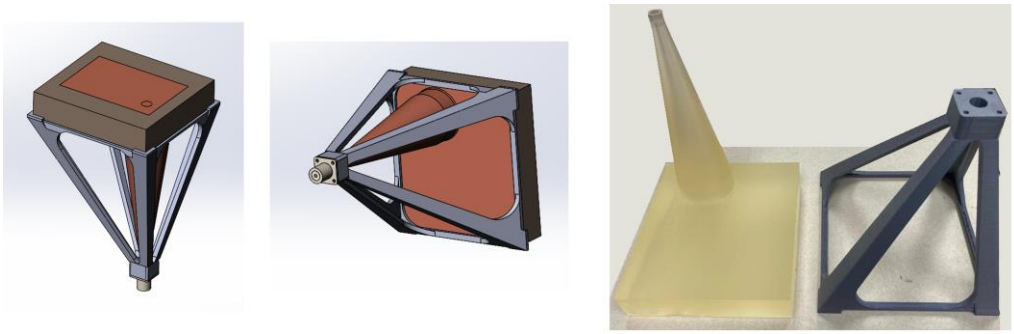


Figure 8.1.1. (a) CAD model and (b) manufactured (incomplete) prototype of an improved version of the tapered-coaxial-connector fed microstrip patch antenna, with an additional supporting frame.

8.1.5 *Summary of Significant Findings and Mission Impact*

(A) Developing Array Pattern Tool for large arrays calculations:

A MATLAB code has been developed for faster radiation pattern approximation of a linear/planar array of any size and composed of any type of antenna elements. The code requires the center element pattern of a small array (say, 3×3) composed of the same type of antenna elements, desired lattice arrangement, and total number of array elements, as user inputs. The usage of this code will be included in future publications.

(B) Investigate the effects of array aperture area reduction on different array parameters:

The effects of different aperture shape and lattice arrangements on array gain and beam steerability have been studied for arrays modeled on PEC-backed substrates. Investigations show that a transformation from square-grid-rectangular-aperture to triangular-grid-hexagonal-aperture leads to $\approx 30\%$ reduction in aperture area ($\approx 50\%$ reduction in number of array elements) with a tradeoff of ≈ 1.5 dBi (in 2.5–5 GHz) and ≈ 3.5 dBi (640–990 MHz range) gain reduction. The aperture area reduction, however, comes at the cost of limited beam steerability to $\pm 45°$ from boresight, compared to the $\pm 60°$ scanning capabilities achieved from the square-grid-rectangular-aperture arrays, at all frequency ranges.

(C) Build minimum viable validation prototypes of single ESA elements:

Developed a design technique for electrically small microstrip patch antenna that provides $\geq 30\%$ impedance bandwidth by strategic placement of the feed-probe along the patch diagonal, at operating frequencies in the UHF (MHz) to microwave (GHz) frequencies. The method avoids any sophisticated prototyping and is a transformative approach in the design of electrically small microstrip antennas for ultrawideband wireless applications.

The design approach was validated via prototypes manufactured on TMM-6 and TMM-10i substrates, in the 2.5–5 GHz range. In addition, a prototype has been built for operation in the UHF range (0.7–1.2 GHz). Despite a few manufacturing defects, the preliminary test results showed reasonable agreement with the simulated values. An updated version of the prototype is currently being manufactured for improved performance.

(D) Optimization of ESA (single element) performance using regular, and ML based stochastic search algorithms:

Optimization of feed-probe location, ground plane shape and size in a microstrip patch antenna, with the objective of bandwidth enhancement, using ML based stochastic search algorithms (GA, PSO, and Simplex methods), was performed. ML algorithms were found to be ≈ 2 times faster and ≈ 0.3 times less memory intensive compared to regular search algorithms, while maintaining the same degree of accuracy.

It is concluded that, although these automated ML algorithms do not provide insight into the underlying physics of the problems and require human intervention at every stage for better decision making, they can still be considered as potential tools for faster optimization of antenna performance, especially for multi-objective optimization of complex structures, which is computationally intensive using conventional EM solvers.

(E) Build minimum viable validation prototypes for arrays of ESA elements:

A 3×3 array of wideband elements (2.5–5 GHz) and a 2×2 array of narrowband elements (900 MHz), on TMM-10i substrates, were manufactured and tested. Having achieved reasonably good agreement between simulated and measured S_{11} and gain responses from individual array elements, it was decided to implement the design method for building the final demonstrable prototypes. Currently, a 4×4 square-grid-rectangular-aperture and a 10-element triangular-grid-hexagonal-aperture array of wideband, microstrip ESA elements, in the UHF range (0.6–1 GHz), are being characterized for prototyping.

(F) Optimization of array performance using ML algorithms:

Completed inter-element spacing optimization in a 4×4 square-grid array, on an infinitely large, PEC-backed dielectric substrate, using a ML-based genetic algorithm, in the 2.5–5 GHz range, with the objective of array boresight gain enhancement. Multi-objective optimization (simultaneous enhancement in boresight gain and impedance bandwidth) of a 4×4 square-grid array on a finite, PEC-backed substrate, by seeking the best array design parameters, including inter-element spacing, ground plane size, and feed-probe locations, in the desired UHF range (0.6–1 GHz), is pursued presently.

8.2 Tradespace Analysis of Ultra-Wide-Band (UWB) Koshelev Antenna

(Alex Dowell and Kalyan Durbhakula)

8.2.1 *Problem Statement, Approach, and Context*

Primary Problem: Determine the extent to which the physical aperture area of an antenna array, composed of antenna elements, can be reduced, while maintaining performance in peak power density, bandwidth, and electronic beam steerability over the UHF range (0.4–1 GHz), compared with present-art high-power-microwave-capable antenna arrays.

Solution Space: The Koshelev antenna has a unique design that is capable of generating an UWB response by effectively merging radiation characteristics from a transverse electromagnetic (TEM) horn antenna with exponentially tapered flares, an electric monopole, and magnetic dipoles over a wide frequency range [1]. This opens up an opportunity to investigate the design parameter space and understand parameter effects on impedance bandwidth, radiation pattern, electric field distribution, and other metrics via a tradespace study.

Sub-Problem:

(i) The integration of an impedance transformer to a single element Koshelev antenna to simulate and test the combined (transformer–antenna) performance is currently not feasible using commercial EM simulators.

(ii)The total surface currents on the Koshelev antenna over the desired frequency range arising from the present positioning of TEM exponential flares, an electric monopole, and magnetic dipoles is not yet clearly understood.

State-of-the-Art (SOTA): The balanced antipodal Vivaldi antenna (BAVA) is considered to be the SOTA antenna element due to its exceptional 20:1 impedance bandwidth ratio as well as the ability to handle tens-of-MW input power.

***Deficiency in the SOTA*:** The BAVA design parameter space has been exhausted over the past couple of decades. The physical aperture area still remains very large and there is no viable path through tradespace study for further physical aperture area reduction.

Solution Proposed: Design, simulate, validate, and perform a tradespace study on the important design parameters of the Koshelev antenna array that effectively reduce its physical aperture area while maintaining its UWB properties, in both the frequency and time domains. The Koshelev antenna has been shown in the literature to withstand higher voltage levels (over 200 kV peak voltage), thereby making it a viable antenna element for detailed tradespace study and analysis.

Relevance to OSPRES Grant Objective: From the literature, it was shown that the Koshelev antenna can handle high input voltages (and therefore high power with 50 Ω input impedance), which satisfies the specific OSPRES objective related to high input voltage/power. In addition, this work can yield a center-frequency-dependent, bandwidth-controlled, and electronically steerable Koshelev antenna design that can be quickly modified to the spectrum properties of the ultra-fast rise time input pulse.

Risks, Payoffs, Challenges:

(i) The electrical size of the Koshelev antenna is approximately λ/4 at its lowest operating frequency. Further reduction of electrical size to λ/10 could considerably reduce frequency dependent gain, thereby decreasing the power spectral density.

(ii) Payoffs include the development of a library of antenna metrics data for different shapes and sizes of the individual parts within the Koshelev antenna.

(iii) The large electrical size (>5λ) of the Koshelev antenna at its highest operating frequency poses huge computational challenges.

8.2.2 *Tasks and Milestones / Timeline / Status*

(A) Complete literature search to identify and list antenna elements that satisfy UWB properties and HPM requirements, and down-select accordingly / NOV–DEC20 / Complete.

(B) Complete initial design, simulation, and validation of Koshelev antenna [1] / JAN21 / Complete.

(C) Perform a preliminary parameter study to identify design parameters that considerably reduce the physical aperture area / FEB–MAR21 / Complete.

- Milestone: Using FEKO and/or CST electromagnetic (EM) simulators, reduce the physical aperture size of the Koshelev antenna to at least 95% of its original design and show minimal to no variation in the bandwidth, gain and increased aperture efficiency / Complete.

(D) Determine the full-width half-maximum (FWHM) and ringing metrics from the envelope of the time domain impulse response ($h_{rx/tx}(t, \phi, \theta)$) in receive or transmit mode / MAR–APR21 / Complete.

- Milestone: Produce a generalized code that calculates the impulse response envelope of the Koshelev antenna and plots the rate of change in FWHM and ringing values as a function of physical aperture size.

(E) Perform tradespace studies on design parameters such as feed position (*F*), length (*L*), and alpha (α). Obtain various antenna metrics data, compare, and analyze / MAR21/ Complete.

- Milestone: Identify Koshelev antenna design parameters that significantly alter the bandwidth, rE/V, peak gain over the desired bandwidth, and aperture efficiency.

(F) Reduce Koshelev antenna aperture size (H×W) to equal to or less than 90 mm × 90 mm, equal to that of the SOTA BAVA, for direct antenna metrics comparison / MAR–APR21 / Complete.

- Milestone: Provide a recommendation on the optimum design parameters and the resulting metrics, with comparison to SOTA BAVA. The optimized design parameters must yield 900 MHz ± 200 MHz bandwidth, rE/V greater than 1, peak gain around 3 dBi at 900 MHz, aperture efficiency equal to or greater than 130% at 900 MHz.

(G) Using the optimized model from (F), build various array simulation models/topologies to perform a tradespace study and report tradeoffs between array antenna metrics such as center element reflection coefficient (S11) value, gain vs theta at constant phi, physical aperture area, aperture efficiency, and rE/V / MAY–JULY21 / Complete.

- Milestone: Develop/showcase an optimized Koshelev array model that exceeds an aperture efficiency of 130% with a high rE/V.

(H) Perform literature search to investigate, understand, and determine the applicability of special electromagnetic (EM) techniques to the antennas under consideration. / JAN–APR21 / Complete.

(I) Explore impedance taper (microstrip based and coax based) designs that can interface well (both mechanically and electrically) to transition the signal from a coax cable to the input of the Koshelev antenna element / JULY21–AUG21 / Complete.

- Milestone: Recommend the optimum impedance taper design (with minimum reflections and maximum power transfer) with the optimum dimensions to successfully convert the high-voltage, short-rise time input signal from a coax cable to the feed of the Koshelev antenna array.

(J) Study response from optimized Koshelev antenna array when excited with different monopolar, differential, and bipolar pulse signals of significant interest / AUG21–NOV21 / Ongoing.

- Milestone: Provide a table comparing the Koshelev antenna array response metrics and narrow down the suitable pulse signals. Recommend (if any) changes to the downselected pulse signal(s) that can further improve the radiation efficiency, and/or transient gain.

(K) Investigate and analyze the response from the optimized Koshelev antenna array when excited by different excitation patterns / DEC 21 / Complete.

- Milestone: Compare and recommend an appropriate excitation method to yield maximum boresight gain, maximum half-power beamwidth (HPWB), minimum side lobe levels, and maximum electric field, rE/V.

(L) Prototype single element Koshelev antenna and test for reflection coefficient, gain as a function of frequency, radiated electric field at 1-m, 2.5-m, 5-m and 10-m (if feasible) distances. / AUG21–SEP22 / Ongoing.

    (L1) Fabricate Cu-foil and paint (silver or copper) variants of 3D-printed balanced Koshelev antenna with integrated impedance transformer.

    - Milestone: Demonstrate a 3D printed Koshelev antenna prototype that is cost-effective and lightweight. / AUG21–NOV21 / Complete.

    (L2) Perform scattering parameter measurements of Cu-foil and paint variants of 3D-printed prototypes to identify any design and fabrication issues/challenges.

    - Milestone: Report fabrication & assembly challenges, test outcomes and identify the source of mismatch (if any) to alleviate reflections. Verify against simulations to validate mismatches. / DEC21–APR22 / Complete .

(L3) Downselect to one variant of the 3D printed Koshelev antenna prototype and measure frequency domain gain and time-domain electric field at multiple distances.

- Milestone: Experimentally demonstrate a 3D-printed Koshelev antenna with a performance comparable to the standard sheet metal variant of the Koshelev antenna. / MAY22–SEP22/ Partially Complete.

- Milestone: Report performance of 3D printed Koshelev antenna, compare against the performance of balanced antipodal Vivaldi antenna (BAVA), and recommend any overall improvements to the fabrication/prototyping/testing methods.

8.2.3 *Progress Made Since Last Report*

(L2) In the previous report, several versions of a partial dielectric impedance transformer integrated with a Koshelev antenna computer aided design (CAD) model were simulated to identify a structurally sound transformer with minimal radio frequency (RF) performance degradation. After reviewing S_{11} and boresight gain from 100 MHz – 5 GHz plots, it was determined that the partial dielectric impedance transformer integrated with a Koshelev antenna meets the desired performance requirements and should be prototyped. Before fabrication could begin, a structural support case study was conducted to identify where adequate structural support could be added to the partial dielectric impedance transformer integrated with a Koshelev antenna CAD model with minimal RF performance degradation. After adequate support structure for the Koshelev antenna and the partial dielectric impedance transformer was validated from CST Studio Suite the prototype was built and tested.

8.2.4 *Technical Results*

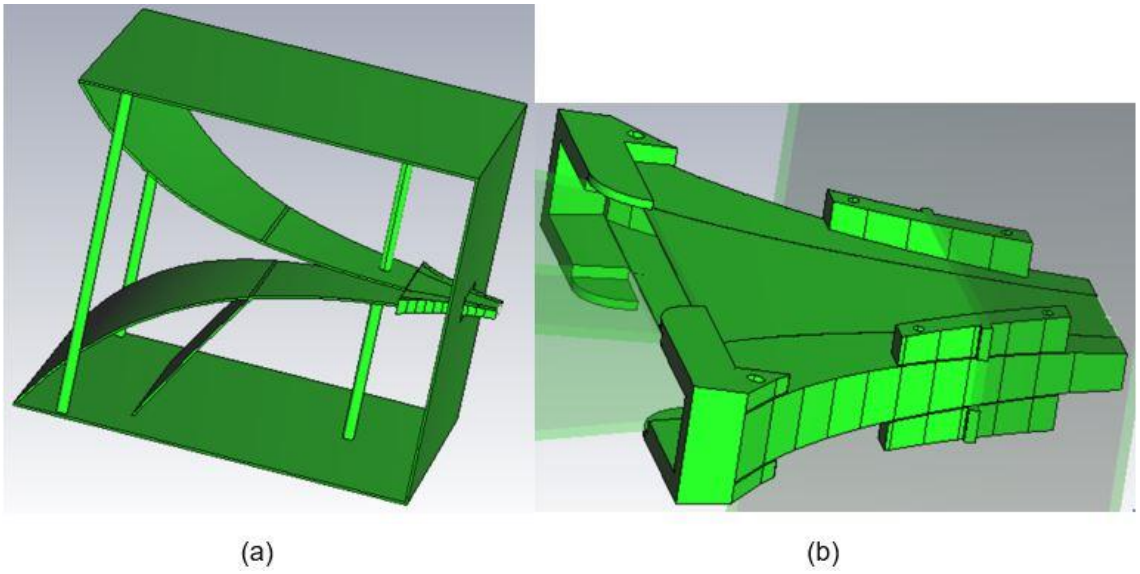


Fig. 8.2.1. CAD models of (a) a partial dielectric impedance transformer integrated with a Koshelev antenna and antenna structural support (b) a partial dielectric impedance transformer with front and rear structural support.

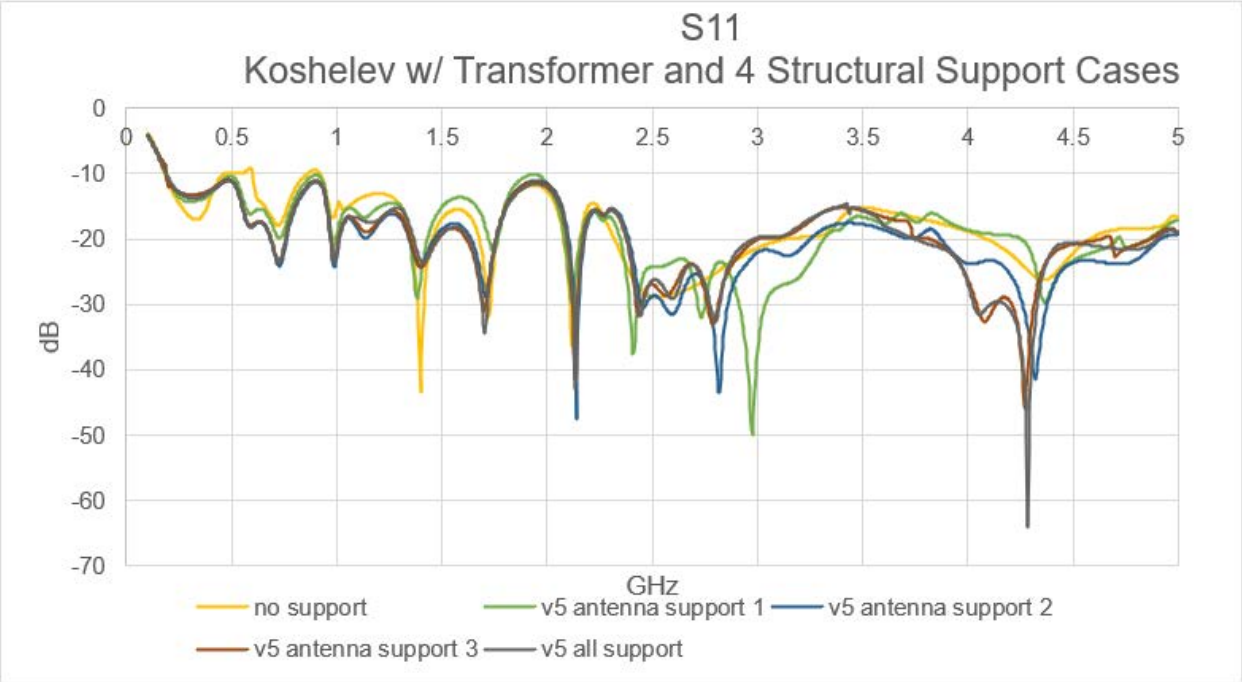


Fig. 8.2.2. Comparing $S11$ of a Koshelev antenna integrated with a PLA partial dielectric impedance transformer with 4 structural support cases collected from CST Studio Suite and comparing it to the $S11$ of the standalone Koshelev antenna integrated with a PLA partial dielectric impedance transformer.

(L2) A structural support study was conducted where Koshelev antenna support pillars, shown in Fig. 8.2.1 (a), and poly-lactic acid (PLA) partial dielectric impedance transformer mounts, shown in Fig. 8.2.1 (b), were varied in size, shape, and location. The S_{11} results shown above in Fig. 8.2.2 show minimal variance from 100 MHz to 2.5 GHz. The largest variance occurred at approximately 3 GHz and 4.25 GHz. All cases were able to stay below –10 dB.

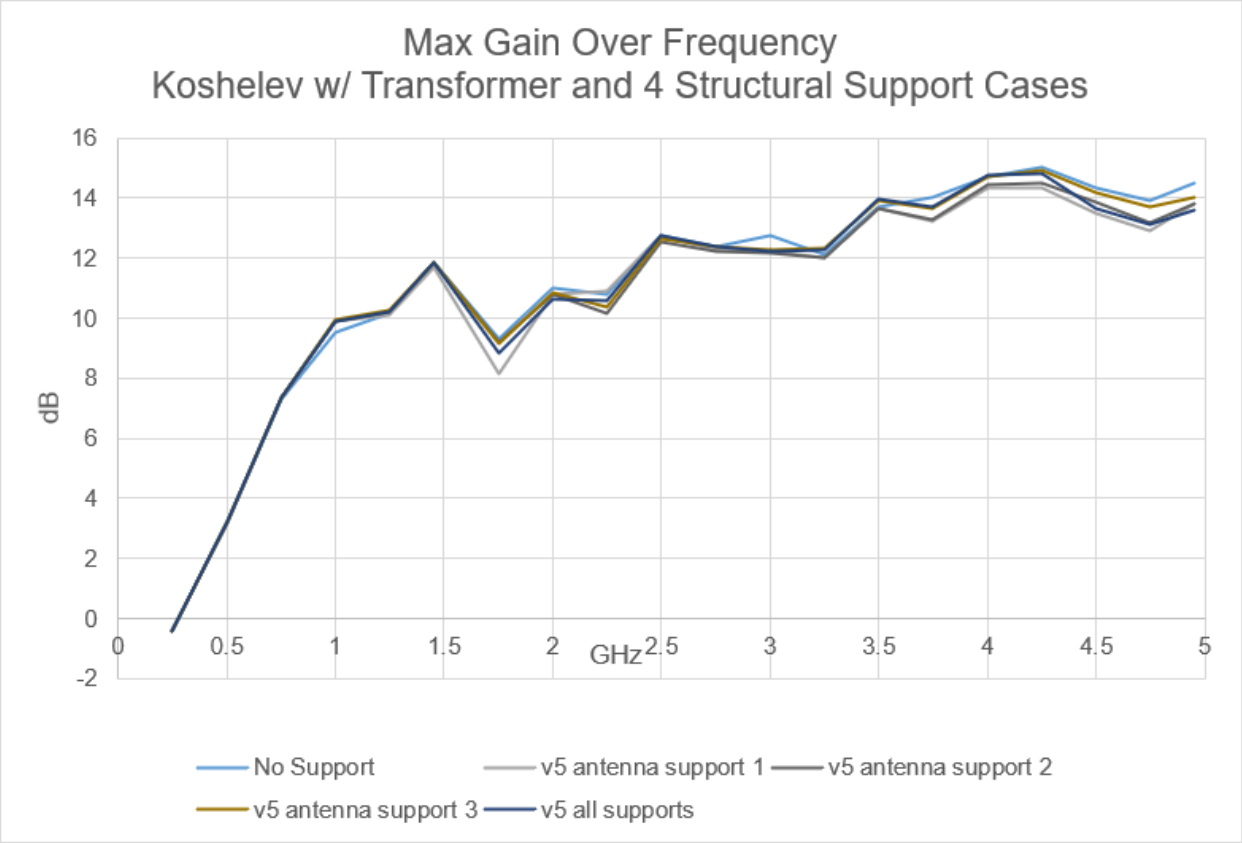


Fig 8.2.3. Comparing max gains of a Koshelev antenna integrated with a PLA Koshelev partial dielectric impedance transformer with 4 structural support cases collected from CST Studio Suite and comparing it to the $S11$ of the standalone Koshelev antenna integrated with a PLA Koshelev partial dielectric impedance transformer.

Shown in Fig. 8.2.3, the antenna structural support pillars proved to have the largest degrading effect. With the support pillars, losses begin at 3.5 GHz. By decreasing the diameter of the outside pillars and reducing the total number of pillars from 6 to 4, an improvement of 1 to 2 dB was achieved from 3.5 GHz to 5 GHz.

(a) (b)

Fig 8.2.4. (a) Side and (b) rear view of Koshelev antenna integrated with a PLA partial dielectric impedance transformer with structural support and a N-type connector prototype.

The 2.5 mm thick frame of the Koshelev Antenna, a partial dielectric impedance transformer, and structural support was 3D printed out of PLA. Copper foil was applied to all surfaces, except for part of the transformer and the structural support, using adhesive tape. Then the transformer mounts where then bolted to the PLA partial dielectric impedance transformer using nylon nuts and bolts. Then the transformer support pillars, and the transformer mounts were epoxied to the Koshelev antenna, shown in Fig. 8.2.4 (a). The last step in the fabrication process was to solder on a N-type connector horizontally to the top and bottom traces, shown in Fig. 8.2.4 (b).

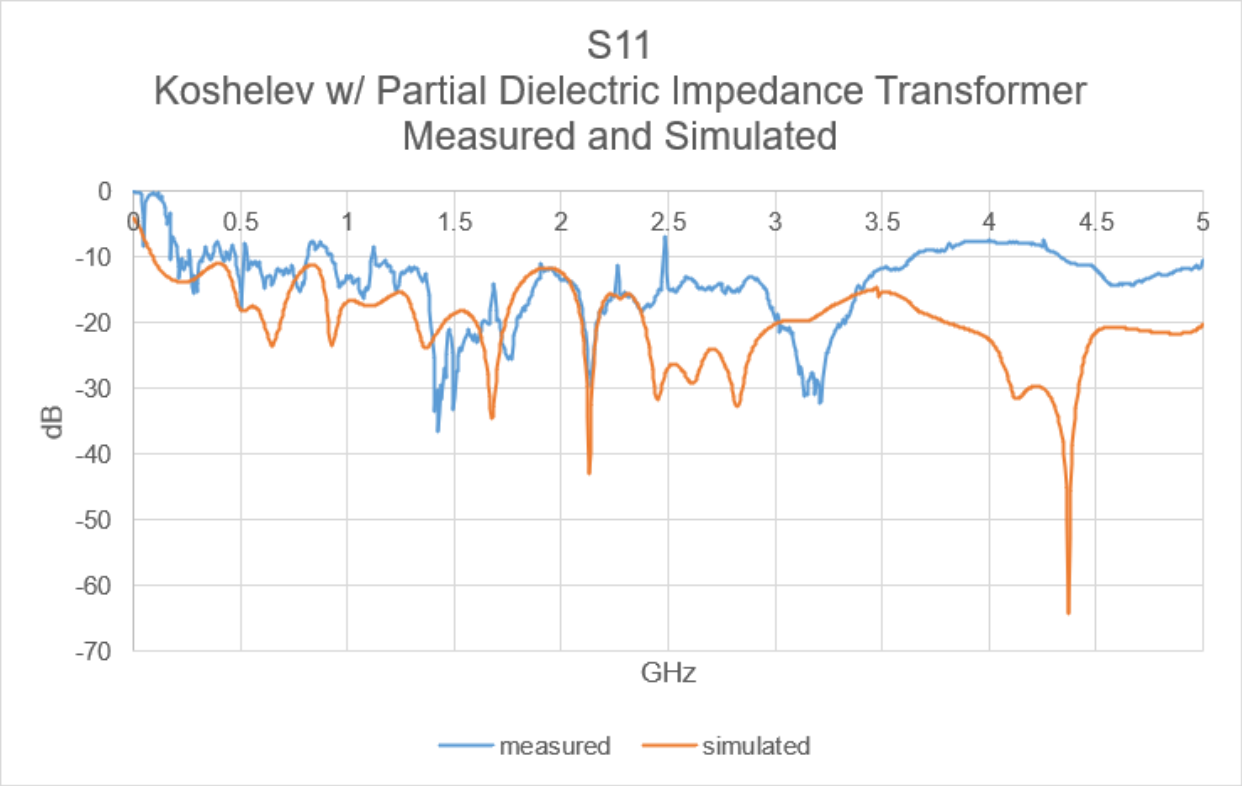


Fig 8.2.5. Comparing S_{11} of a simulated Koshelev antenna integrated with a PLA partial dielectric impedance transformer with structural support collected from CST Studio Suite and a measured Koshelev antenna integrated with a PLA partial dielectric impedance transformer with structural support prototype.

After fabrication, the Koshelev antenna integrated with a PLA partial dielectric impedance transformer with structural support prototype was tested and compared to the simulated S_{11} results, shown in Fig. 8.2.5. The simulated and measured result in Fig. 8.2.5 shows a good agreement over the entire frequency range from 300 MHz to 5 GHz. Some losses can be noticed from the measured result (between 3.5 GHz and 4.5 GHz) because of the fabrication imperfections that could arise in the 3D printing, assembly, and/or in the metallization stages of the prototype. Despite these imperfections, similar trends can be noticed from both results over a wide frequency range (0.3 to 5 GHz) as shown in Fig. 8.2.5. The measured S_{11} result validates our proposed partial dielectric transformer integrated Koshelev antenna design. The next step would be to 3D print a Koshelev antenna with similar aperture area to that of SOTA BAVA and provide 1-to-1 metrics comparison.

8.2.5 *Summary of Significant Findings and Mission Impact*

(A) An extensive literature search on various UWB antenna elements has resulted in finding three promising options. The down-selected elements are the Koshelev, Shark, and Fractal antennas, which will be extensively studied using their individual design parameter space, which could result in physical aperture area reduction of the

single antenna element. Later, the single antenna element will be converted into a planar array.

(B) Initial validation of the Koshelev antenna simulated using CST software agreed well with the antenna metrics published in the open literature [1]. A UWB bandwidth response (10:1 bandwidth) and rE/V > 1 has been observed from our initial simulations of the Koshelev antenna. This validation ensured that the Koshelev antenna can be subjected to further tradespace studies to understand its performance, followed by optimizing the design according to OSPRES grant requirements.

(C) The initial tradespace study and analysis of the Koshelev antenna design yielded promising outputs to carry forward the investigation. A comparison of important antenna metrics between the Koshelev antenna in [1] and aperture reduced Koshelev antenna are shown in Table 5.2.1 of the APR 21 MSR.

(D) An in-house code has been developed to calculate important UWB time domain antenna metrics such as full-width half maximum (FWHM) and ringing. These metrics have been calculated using in-house MATLAB code using the excitation voltage and radiated electric field information obtained from CST simulations. FWHM and ringing antenna metrics help with assessing or characterizing an antenna's UWB response.

(E) The tradespace study of feed position provided a deeper understanding of how its position impacts the S_{11} value bandwidth. An optimum value for feed position i.e., $F = 1/20 < L < 1/10$ is recommended to achieve maximum bandwidth. The tradespace study of the antenna length (L) is straightforward. A longer antenna length will radiate better at lower frequencies. However, physical size restrictions/requirements must be kept in mind in determining the antenna length. Finally, a larger α value (>120°) is recommended to avoid unnecessary reflections from the electric monopole.

(F) From a thorough tradespace study, the aperture size of the Koshelev antenna (single element) is determined to be 90 mm × 100 mm in order to achieve desired antenna metrics performance proposed in the milestone. All metrics described in the milestone have been successfully achieved except the desired bandwidth (200 MHz on both sides) at 900 MHz center frequency. The bandwidth achieved is 900 ± 100 MHz.

(G) The physical aperture area of the Koshelev array antenna largely depends on the interelement spacing and the shape of the array. We were able to determine that the diamond topology is the optimum shape for the Koshelev array antenna. We were also able to obtain similar gain profile (peak gain and pattern) from making certain elements within the array passive (off state) when compared against regular active array (all elements in on state). From the non-symmetric interelement spacing values, we found that S_y has the least effect on the output; therefore a small spacing value can be chosen to reduce the physical aperture area of the Koshelev array.

(H) The literature search on the special EM techniques expanded our knowledge and opened the door to opportunities to apply some of those techniques to the antennas under study. EM techniques such as non-symmetric and non-square array topologies have been applied to the development and study of the Koshelev array antenna.

(I) The first impedance taper design under consideration has shown good S11 values (< –10 dB) over the frequency range of interest. In addition, we have shown that the shape of the pulse can be easily retained at the output of the taper with less than 5% amplitude losses.

(J) The Koshelev antenna array response from feeding a monopolar vs bipolar signal has demonstrated a clear winner: that is, a bipolar signal will radiate at least 10 times better than a monopolar signal. A comparison of the frequency spectrum of the radiated electric field from the optimized Koshelev antenna array between different monopolar pulse sources has identified the 'MI0731' pulse to be the optimum pulse.

(K) The optimized Koshelev antenna array was studied for the electric field response under different array excitation patterns. The study determined that the uniform and Gaussian excitation patterns were the optimum excitation patterns. Selecting the uniform or Gaussian excitation pattern would yield the maximum electric field at the boresight for an arbitrary input signal.

(L) Two variants (Cu-foil plated and silver painted) of the 3D-printed Koshelev antenna have been fabricated to demonstrate a working antenna prototype. The Cu-foil plated 3D printed Koshelev antenna prototype with partial dielectric transformer has shown to yield better RF performance over the silver painted one. A publishable agreement was noticed between the S_{11} results from the Cu-foil plated Koshelev antenna prototype and simulation model. A 1-to1 comparison between the proposed Koshelev antenna and the SOTA BAVA can be drawn provided the aperture area of both antenna elements have similar aperture area. The Koshelev antenna prototype produced in this effort was to demonstrate proof-of-concept, which was done successfully. Next, we plan to 3-D print and metalize a Koshelev antenna with aperture area equivalent to BAVA and draw a fair comparison.

8.2.6 *References*

[1] Gubanov, V. P., et al. "Sources of high-power ultrawideband radiation pulses with a single antenna and a multielement array." *Instruments and Experimental Techniques* 48.3 (2005): 312-320.

[2] S. Zhang, Y. Vardaxoglou, W. Whittow and R. Mittra, "3D-printed graded index lens for RF applications," 2016 International Symposium on Antennas and Propagation (ISAP), 2016, pp. 90-91.

8.3 Machine Learning Inspired Tradespace Analysis of UWB Antenna Arrays

(Sai Indharapu and Kalyan Durbhakula)

8.3.1 *Problem Statement, Approach, and Context*

Primary Problem: Determine the extent to which the physical aperture area of an antenna array, composed of antenna elements, can be reduced while maintaining performance in peak power density, bandwidth, and electronic beam steerability over the UHF range (0.4–1 GHz), compared with present-art high-power-microwave-capable antenna arrays.

Solution Space: Fractal antennas possess exceptional fidelity factor values (>0.9), which describe how well the shape of the input pulse is retained at an observation point in the far-field. Their high degree of freedom provides an opportunity to develop systematically modified patch shapes, which in turn leads to improved bandwidth while retaining high fidelity factor values. Machine learning (ML) can be leveraged to predict the antenna array response for an arbitrary design parameter space upon sufficient training and validation.

Sub-Problem:

(i) Fractal antennas generate omni-directional radiation patterns in the H-plane over the desired frequency range.

(ii) ML can suffer from underfitting or overfitting the training model which in turn leads to deviations in the predicted output.

State-of-the-Art (SOTA): Conventional full-wave EM solvers such as method of moments (MoM), multi-level fast multipole method (MLFMM), finite element method (FEM), and finite difference time domain (FDTD) method are currently being used to study, analyze and assess the performance of UWB antennas.

Deficiency in the SOTA: UWB antenna optimization using conventional EM solvers utilizes significant computational time and memory resource.

Solution Proposed:

(i) Design, simulate, validate, and perform a tradespace study on the design parameter space of the selected fractal antenna element using commercially available electromagnetic (EM) wave solvers.

(ii) Train, validate, test, and compare multiple ML models for quicker and accurate prediction of antenna array response for different physical aperture areas.

Relevance to OSPRES Grant Objective: The fractal antenna achieves an UWB response, a mandatory requirement of the OSPRES grant objective, in a small volume footprint and similar physical aperture area when compared against the SOTA BAVA, dual ridge horn antennas etc. Furthermore, the microstrip-design-based fractal antenna can efficiently handle electronic steering by integrating the feed network on the same board. This eliminates the need to build a separate feed network external to the fractal antenna using bulky coaxial cables.

Risks, Payoffs, and Challenges:

(i) A majority of the fractal antenna geometries yield an omni-directional pattern in the H-plane, which can be a risk. However, efforts are underway to mitigate this pattern without deteriorating bandwidth.

(ii) Payoffs include developing a library of antenna metrics data for various fractal shapes and sizes.

(iii) Design challenges and numerical calculations with respect to specific fractal shapes could arise after performing a certain number of iterations to further improve the bandwidth.

(iv) Fractal antennas were known to generate gain loss at random frequencies over their operating frequencies. Achieving gain stability over the desired frequency range can be a significant challenge.

8.3.2 *Tasks and Milestones / Timeline / Status*

(A) Perform tradespace analysis of the fractal element radius *b* over the desired frequency range (4 to 12 GHz) using the genetic algorithm (GA) optimization tool available in the commercial electromagnetic (EM) solver FEKO / FEB21 / Complete.

- Milestone: Provide a recommendation of an optimum value of *b* using OPTFEKO to minimize reflection coefficient (S_{11}) (< –10 dB).

(B) Perform tradespace study on different fractal shapes by changing the number of fractal segments to understand the effect of this change on the impedance bandwidth / FEB21 / Complete.

- Milestone: Produce a detailed study of the antenna response such as S_{11}, gain, and bandwidth by varying the number of fractal segments.

(C) Apply the GA optimization tool on the fractal side length *b* over a wide frequency range (2 to 12 GHz with 201 discrete frequency points) and number of fractal segments using OPTFEKO on the LEWIS cluster / MAR21 / Complete.

- Milestone: Reduce physical aperture area by 10% of its present design, reported in the FEB MSR, and demonstrate minimal or no change in S_{11}, gain, and fidelity factor values.

(D) Perform a parametric study and analysis of antenna response by varying hexagon radius, *a* / MAR–APR21 / Complete.

- Milestone: Recommend a value of *a* to reduce the physical aperture area and increase aperture efficiency (>50%) with no variation in other antenna metrics.

(E) Frequency scale fractal antenna design such that the center frequency of the resulting antenna equals 1.3 GHz / MAY21 / Complete.

- Milestone: Modify antenna design with a center frequency equal to 1.3 GHz and achieve similar results (3:1 bandwidth at fc = 1.3 GHz, 3 dBi gain and >130% aperture efficiency at 900 MHz) to antenna design at center frequency ~7 GHz.

(F) Design and simulate various array antenna geometries composed of optimized fractal antenna elements (obtained from (E)) to analyze the effect of overall array antenna geometry on the desired array antenna response metrics (i.e., gain vs. frequency, gain vs. elevation angle at constant phi, rE/V, half-power beamwidth and side-lobe level.) / MAY–JUL21 / Complete

- Milestone: Recommend a best possible structure with reduced aperture area and minimal loss in gain.

(G) Apply ML models available in Altair Hyperstudy (2021) on the fractal antenna to try and understand the possibilities and limitations of ML models for fast and efficient antenna metrics prediction and optimization. Expand the prediction capability to time-

domain electric field and antenna pattern using ML models (k-nearest neighbor and linear regression) available in scikit learn on Python programming tool “Anaconda”. / MAY21–FEB22 / Complete.

- Milestone: Recommend most accurate and efficient ML model for a fractal antenna in time-domain and frequency domain.

(H) Apply ML models on the octagon fractal antenna array lattice to extend the prediction capability beyond single element / SEP21–MAY22 / Complete.

- Milestone: Recommend the best suitable ML model implemented/developed using Python programming language for array antenna metrics prediction.

(I) Develop, validate, and demonstrate a graphical user interface (GUI) to automate the process of employing ML models to predict the antenna output response/ FEB22–SEP22 / Complete.

- Milestone: Incorporate the developed automated data extraction scripts, ML scripts to the GUI to enable user to predict antenna response 100x faster than full wave solvers.

8.3.3 *Progress Made Since Last Report*

(I) Antenna array response prediction and latest updates of the GUI.

- Initially, a python script was developed to generate training data input combinations. Upon generating a total of 50 input combinations of design parameters, an EM simulator (CST) was used to calculate the antenna array output response for the generated input combination. Later, input combinations and the corresponding output response were stored in excel sheets to train machine learning (ML) models. Finally, the in-house developed GUI was used to train, validate, and test the antenna array response metrics.
- With the new “Antenna Array Analysis” option added to the GUI, users can now calculate aperture area and aperture efficiency (given gain value) for single input or a sweep analysis. This option will allow users to learn and uncover the relation between the physical aperture area and other antenna response metrics. The GUI allows the user to select from a standard antenna array shape or a custom shape, as shown in Fig. 8.3.1. Each option requires input from the user (side length of the antenna array shape or an equation to calculate the physical aperture area).

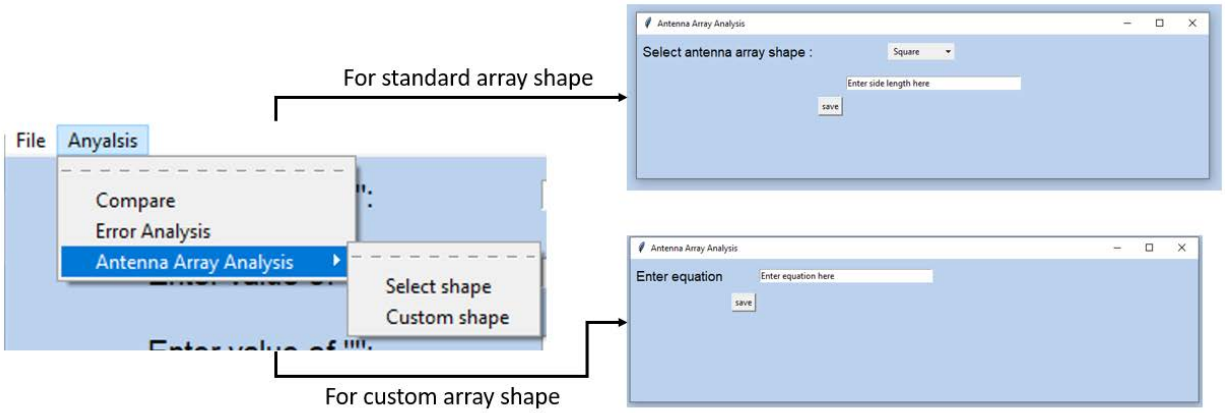


Fig 8.3.1. A block diagram illustrating the workflow of “Antenna Array Analysis”.

8.3.4 *Technical Results*

(I) *Antenna Array prediction:* With the help of a python script, fifty combinations of input design parameters were generated and used as an input file for parametric sweep analysis on CST. Following the calculation of antenna response for the fifty combinations on CST, S_{11} and gain responses for all fifty combinations were exported and processed. The final data version was stored in Excel to further train ML models. For S_{11} and gain response prediction of a fractal antenna array, a training data size of 40 was used with six input parameters such as hexagonal patch side length ‘a ’, fractal side length ‘b’, the distance between patch center and fractal center ‘d’, distance between top ground plane and the transmission line ‘gap’, Inter element spacing between antenna elements in an array ‘IEx’ (in x-axis) and ‘IEy’ (in the y-axis). Unlike the training data size used for gain, five samples of input/output were used for radiation pattern prediction due to limited training data.

The k-nearest neighbor (kNN) ML model available in the GUI was employed to predict the S_{11} response of a fractal antenna array. The above mentioned setup was used to train the ML model with the S_{11} response of the center elements in the output. The number of nearest neighbors suitable for fractal antenna array prediction was found by manual grid search technique.

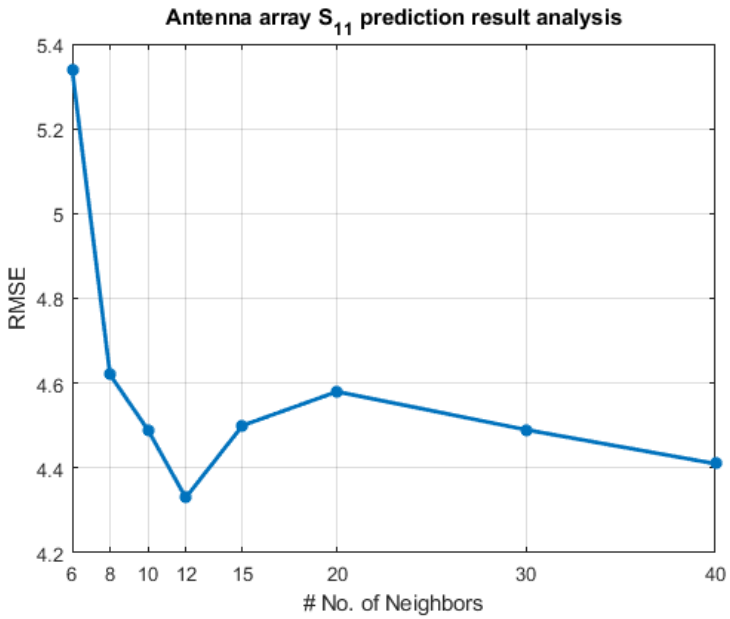


Fig 8.3.2. RMSE vs 'k' nearest neighbors plot.

From Fig 8.3.2. the RMSE value is the least for the kNN model with 12 neighbors. Thus, the model was updated with *k* as 12. From Fig 8.3.3 (a), the GUI has successfully predicted the S_{11} response of a fractal antenna array. The RMSE value reported for this model is 4.33.

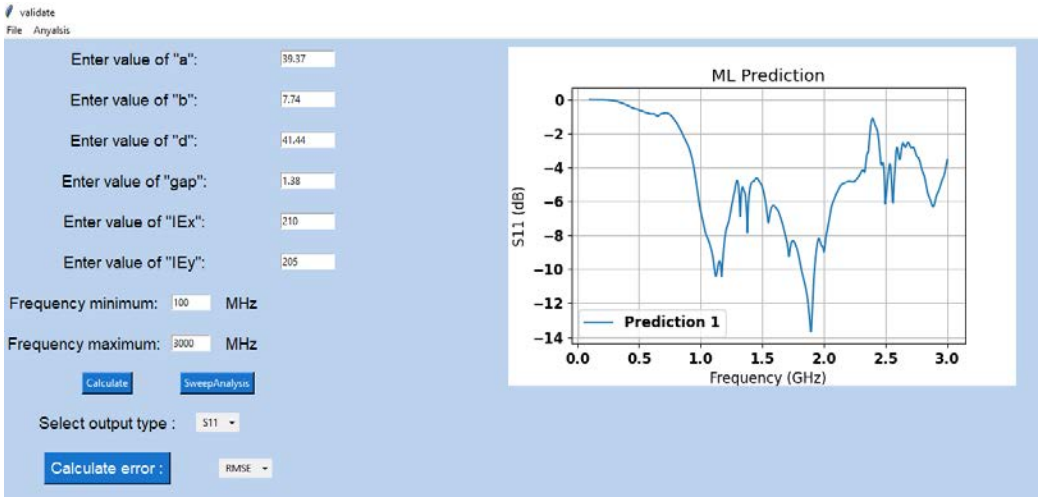


Fig 8.3.3. (a) Snapshot of validation window illustrating the S_{11} prediction.

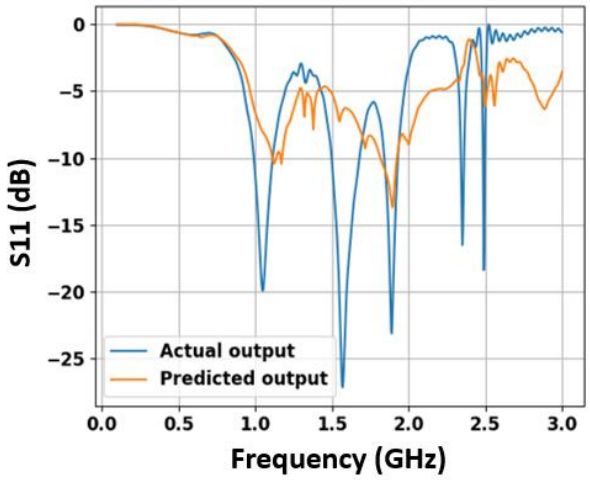


Fig 8.3.3. (b) Comparison of actual S_{11} output (CST response) with predicted S_{11} output (ML response)

Like S_{11} prediction, due to the availability of data (50 samples), the '*k*' value or the number of nearest neighbors was found by manual grid search. From Fig 8.3.4 (a) illustrating the relation between '*k*' and RMSE, the RMSE value for a kNN model with six neighbors is least compared to any other value of '*k*'.

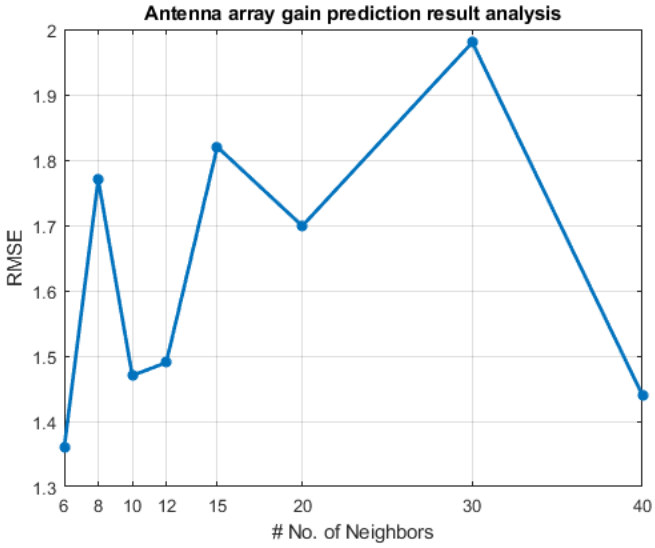


Fig 8.3.4. RMSE vs 'k' nearest Neighbors plot.

Further, the kNN model with six neighbors was used to predict gain response for a fractal antenna array. The ML model in the GUI has successfully predicted the gain output response and displayed it on the validation window as shown in Fig. 8.3.4.(a) The RMSE value reported for this prediction is 1.36.

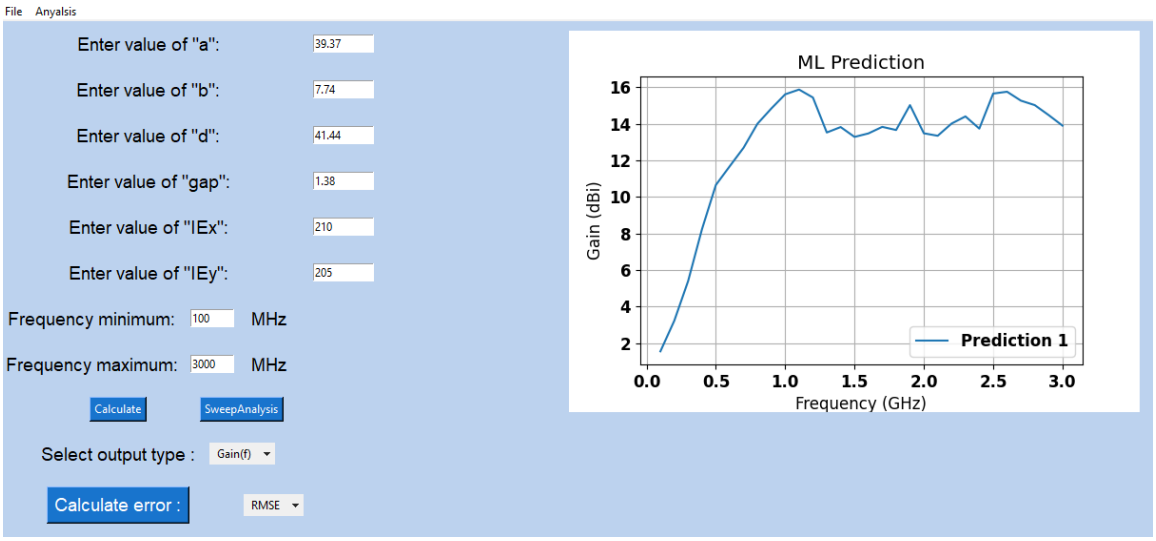


Fig 8.3.4. (a) Snapshot of validation window illustrating the gain prediction.

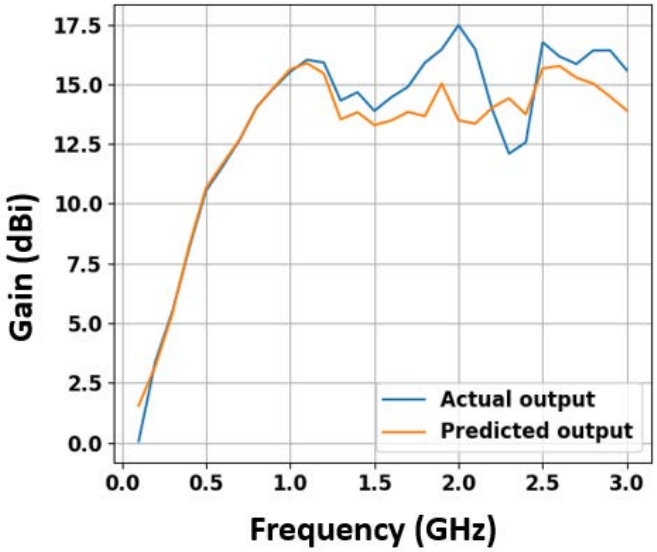


Fig 8.3.4. (b) Comparison of actual gain output (CST response) with predicted gain output (ML response)

Unlike S_{11} and gain predictions, sweep analysis feature on CST cannot be used to produce results for multiple combination with a single simulation. Due to this limitation, the data generated for radiation pattern was limited to 5 samples and the search for optimum values of '*k*' in kNN could not be carried out. Thus, '*k*' as one is set for this study. The dataset sample size of five is used to train the kNN model available in the GUI. Fig 8.3.5 (a) illustrates the predicted response of the ML model.

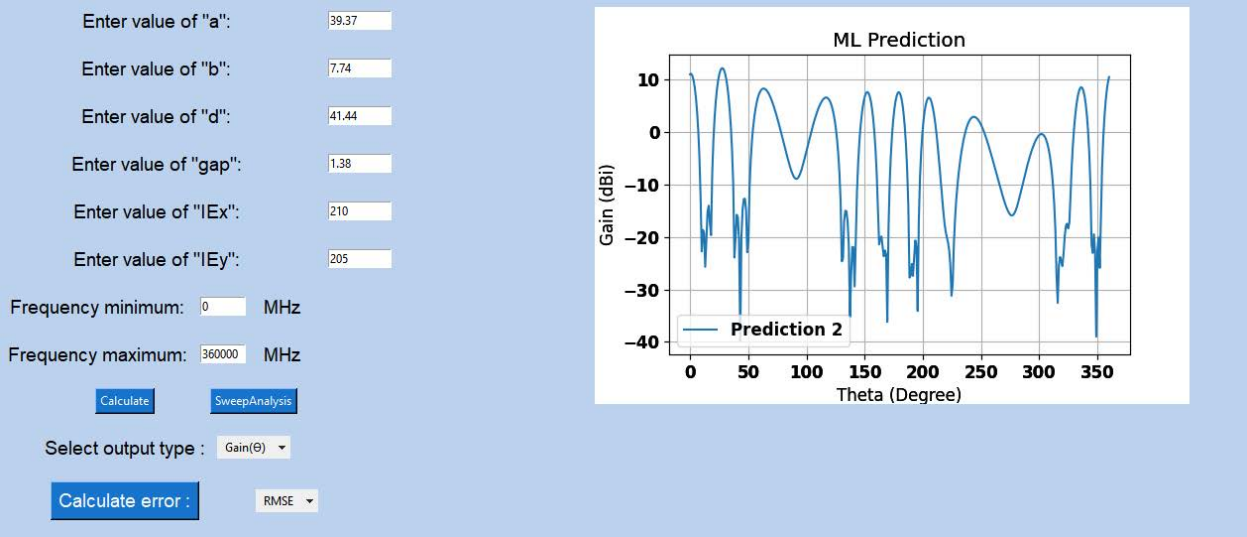


Fig 8.3.5. (a) Snapshot of validation window illustrating the radiation pattern prediction.

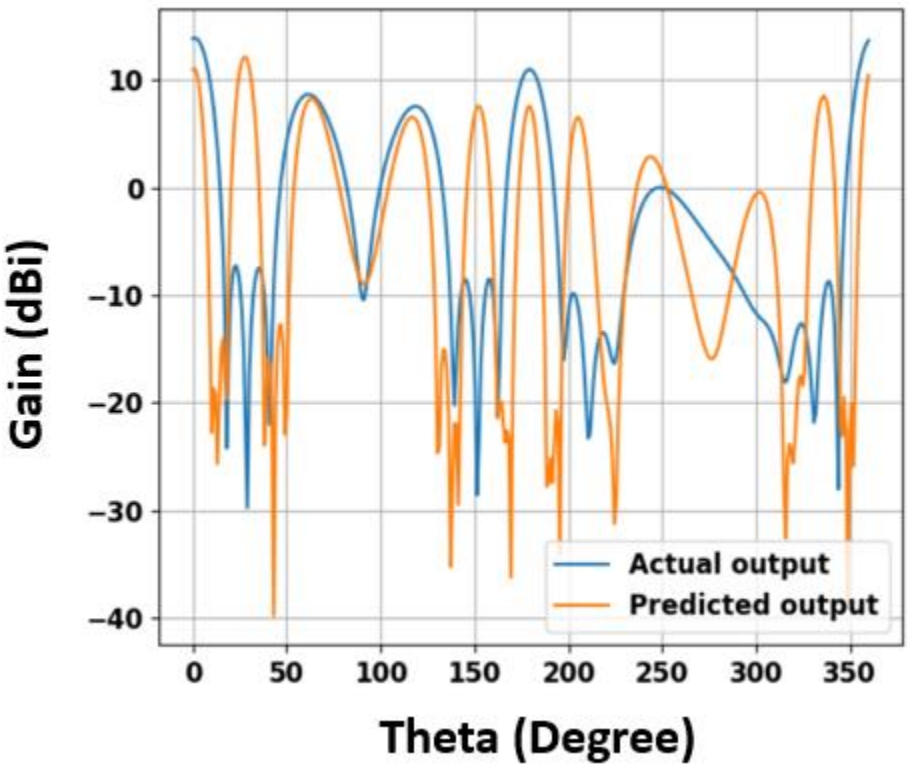
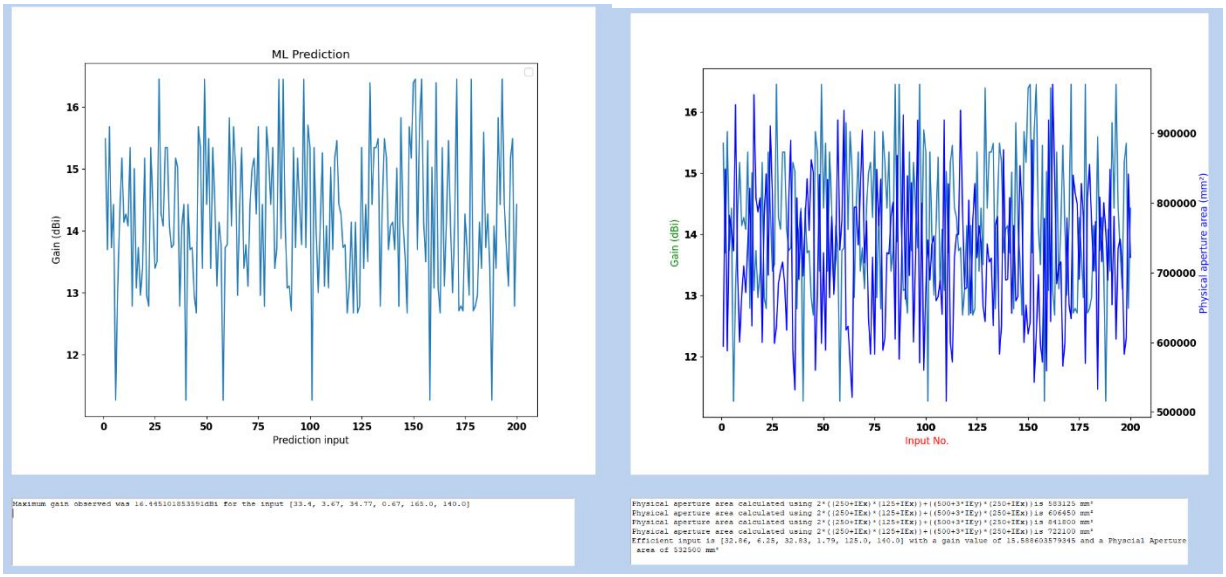


Fig 8.3.5. (b) Comparison of actual radiation pattern output (CST response) with predicted radiation pattern output (ML response).

The RMSE value recorded for this prediction is 13.11. This poor generalization of the ML model can be improved by increasing the training data size and updating the '*k*' neighbors for the kNN model.

To enhance the usage of ML prediction, the GUI was updated with a new feature that helps the user to predict gain and calculate the corresponding physical aperture area. The new feature can be used for single input predictions and sweep analysis. As shown in Fig 8.3.1, the user must select either from the standard antenna array shape or manually enter the equation to calculate the physical aperture area of any antenna array shape. Upon saving the shape of the user's choice, the GUI will now be able to calculate and display the physical aperture area.



(a) (b)

(c)

Fig 8.3.6. Snapshot of validation window illustrating the results obtained from (a)Sweep analysis (b) antenna array analysis, (c) Message box displaying optimal antenna design parameter values.

Unlike the conventional sweep analysis, this feature also calculates the efficiency and displays input for which antenna has maximum gain and minimum physical aperture area. A sweep analysis is carried out to validate the abovementioned updates and calculate gain, as shown in Fig. 8.3.6 (a). Further, the ‘Antenna Array Analysis’ option was used from the menu bar to calculate the physical aperture area and the efficient input from the sweep. The results are displayed in the message box in Fig 8.3.6 (b). With the help of a trained ML model, this feature can calculate gain, physical aperture area, and efficient input for any given input within no time. Also, it will boost the efforts to effectively reduce the physical aperture area of any given antenna array. Table 8.3.1 showcases the computational difference between conventional approach and the ML approach using the GUI.

Table 8.3.1. Comparison of computation time for conventional approach and ML approach using the GUI.

	Conventional approach	ML approach using the GUI
Antenna response calculations	Using FEM, MoM solvers	Using trained ML models (kNN, Linear regression)
Computational time (Fractal antenna element)	~34 mins	<1 sec*
Computational time (Fractal antenna array)	~90 mins	<1 sec*
Design optimization	Requires high performance computer for faster response calculation	Can be carried out on a local a computer.

*Does not include simulation time utilized to generate the training data.

8.3.5 *Summary of Significant Findings and Mission Impact*

(A) We carried out an effort to identify the dominant fractal antenna design parameter and its corresponding value using parameter study and FEKO optimization tool. It was found that the side length '*b*' of the fractal elements plays a significant effect on the antenna bandwidth. The initial analysis of the simulation results with fractal radius *b* equal to 1.8 mm yielded multiple resonant frequencies with enhanced bandwidth. To further increase the bandwidth, OPTFEKO was used as an optimization tool with fractal radius *b* as the optimization variable. Finally, the optimum value for *b* was found to be 1.66 mm which minimizes the S_{11} (-10 dB).

(B) The addition of fractal elements (*N*) to the simple hexagon improved antenna metrics such as reflection coefficient (S_{11}). To further investigate and understand the fractal elements, the number of segments (sides of the fractal element) in the fractal geometry were varied within the range of 6 to 14. By varying the number of segments in the fractal element, the resultant S_{11} response had positive impact at higher frequencies and negative impact at lower frequencies. Therefore, the number of segments of the fractal element were chosen to be 6 as it has better balance of S_{11} values both at lower and higher frequencies.

(C) The initial optimum value of *b* over 51 discrete frequency points is reported as 1.66 mm in task (A). To further increase the accuracy of the optimization algorithm and to find a more precise value for *b*, optimization is further performed over a wider frequency range (201 discrete points between 2 GHz to 12 GHz) which yielded an optimum value of *b* as 1.37 mm. The S_{11} response of the antenna design with this

newly obtained *b* parameter (i.e., 1.37 mm) has not produced any better bandwidth compared to *b* = 1.66 mm. Thus, *b* is set to be 1.66 mm for further research.

(D) The hexagonal patch radius *a* has a significant effect on the physical aperture area of the antenna. Therefore, Altair OPTFEKO has been utilized to find an optimum *a* value, which was determined to be 8 mm over the range 7.2 to 9 mm. Antenna metrics such as S_{11}, gain, and bandwidth have shown desired performance with the optimized *a* value.

(E) The initial antenna design has been modified to achieve a center frequency of ~1.3 GHz. The gain value at 900 MHz is 3.5 dBi and, with the modified antenna design, we were able to achieve an impedance bandwidth ratio of 3.3:1. The designed antenna has been fabricated and tested, and the S_{11} response of the fabricated antenna agrees well when compared against FEKO, CST.

(F) Four different fractal antenna array geometries (i.e., square, diamond, hexagon, and octagon) have been designed and simulated. Upon comparing antenna array metrics, the octagonal fractal antenna array has yielded minimal sidelobe levels with a gain of 15.7 dBi at 900 MHz, close to that of the square geometry but with 32.27% lower physical aperture area. The octagonal fractal antenna array has been chosen as the optimum geometry with reduced aperture area and reduced side lobes while retaining the bandwidth and gain milestone metrics.

(G) The ML models available (radial basis function (RBF), least square regression (LSR) and, hyper kriging (HK)) in Altair Hyperstudy were employed to predict the output response of a fractal antenna. RBF and LSR were down selected from the initial three ML models based upon their generalization capability for prediction of fractal antenna output response. The test RMSE increased as the values drifted away from the mid-point of the training range. RBF performed well in the prediction of S_{11}, while LSR performed slightly better for gain and electric field predictions. In addition, for time-domain electric field prediction, we recommend using kNN ML algorithm for accurate prediction.

(H) The initial application of the kNN ML model for the prediction of antenna array bandwidth response of center and corner element yielded positive results with good agreement between traditional EM solver (FEKO) and trained kNN ML model. The new LR ML model yielded improved RMSE values (over kNN) in its prediction of reflection coefficient (27.82% less RMSE for center element and 19.76% less RMSE for corner element). On the other hand, the RMSE values for gain (as function of theta) prediction using LR ML model has 55.51% increase over kNN prediction. Finally, kNN provides better generalization to predict reflection coefficient, whereas LR provides better generalization to predict frequency domain gain in the case of a fractal antenna array. On the other hand, the application of the AEP method for antenna array was put on hold due to its limitations.

(I) A GUI was developed to handle antenna response prediction of an antenna element and an antenna array geometry. The GUI requires training data for an antenna (single-element or array) of user choice and predicts desired antenna output response (S_{11}, antenna gain, radiation pattern) for a range of test data within a few

seconds. The GUI has been configured to perform parametric sweep analysis for S_{11} and gain response outputs for the fractal antenna design. Based on feedback/suggestions received from the other in-house researchers, key features such as data comparison plot, error calculation, data exporting, and antenna array analysis were added to the GUI. Finally, the antenna array analysis option was able to display the most efficient input combination for which the antenna array has less physical aperture area and high gain.

8.3.6 *References*

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9 Feedback

There is no feedback to report for the current reporting period.

10 Program Management

10.1 Issues

i. Scope – No issues
ii. Budget – 12-month NCTE submitted/pending
iii. Schedule – No issues

10.2 Interactions with Others

Agency/Org	Performer	Project Name	Purpose of Research/ Collaboration

10.3 Major Procurement Actions

10.4 Travel

Destination	Purpose	Attendees	Estimated Costs

10.5 Pending or Upcoming Public Release Requests

11 Appendix A: Academic and IP Output

11.1 Students Graduated

Name	Degree	Currently
Al-Shaikhli, Waleed	MS Spring 19	Kansas City National Security Campus, Honeywell
Azad, Wasekul	PhD Summer 21	Applied Materials, Sunnyvale, CA
Berg, Jordan	MS Spring 21	MRI Global
Bhamidipati, John	PhD Spring 22	MIDE
Bissen, Bear	MS Spring 19	Capella Space, San Francisco, CA
Brasel, Sadie	BS Spring 21	
Floyd, Dennis	BS	Naval Air Warfare Center Weapons Division
Hanif, Abu	PhD Spring 21	
Harmon, Aaron	BS	Missouri University of Science & Technology
Harp, Joshua	MS	
Hauptman, Cash	BS Spring 18	University of Nebraska-Lincoln
Klappa, Paul	MS Spring 21	
Kovarik, James	MS 21	
Labrada, Dario	BS Spring 20	Honeywell Aerospace, Florida
Lancaster, John	MS Spring 17	Lawrence Livermore National Laboratory, CA
Renzelman, Jeff	MS Spring 18	Kansas City National Security Campus, Honeywell
Roy, Sourov	PhD Spring 21	BTCPower, Orange County, CA
Wagner, Adam	MS Fall 20	Los Alamos National Laboratory, New Mexico
Xia, Shengxuan	BS	Missouri University of Science & Technology

11.2 Journal Publications

11.2.1 *In Preparation*

[1] S. S. Indharapu, A. N. Caruso, K. C. Durbhakula, “Machine Learning Assisted Antenna Design Optimization of UWB Fractal Antenna,” TBD, In Preparation, **2022**.

[2] J. K. P Bhamidipati, G. Bhattarai, A. N. Caruso, “Effect of Proton Irradiation Induced Localized Defect/Trap Clusters on Silicon Photoconductive Semiconductor Switch (Si-PCSS) Recovery Time and Leakage currents,” *Solid-State Electronics,* In Preparation, **2022**.

[3] N. Gardner, K. C. Durbhakula, and A. N. Caruso, “UHF and L-Band Frequency Generation at MW Peak Power using Diode-based Nonlinear Transmission Lines as Pulse Forming Networks,” *Transactions on Plasma Science*, In Preparation, **2022**.

[4] N. Gardner, K. C. Durbhakula, and A. N. Caruso, “Electrically Tunable Diode-based Nonlinear Transmission Line,” *TBD*, In Preparation, **2022**.

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Phased Array Applications," *IEEE Antennas and Propagation Magazine,* In preparation, **2022**.

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11.2.2 *Submitted / Under Revision*

[8] J. K. P. Bhamidipati, E. R. Myers, A. M. Conway, L. F. Voss, M. M. Paquette, and A. N. Caruso, "Figure of Merit Development for Linear-Mode Photoconductive Solid-State Switches," *IEEE Journal of the Electron Devices Society*, Submitted May 1 **2022**, Manuscript ID#JEDS-2022-05-0136-R.

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[12] K. Alsultan, M. Z. M. Hamdalla, S. Dey, P. Rao, and A. M. Hassan, "Scalable and Fast Characteristic Mode Analysis Implementation Using a Hybrid CPU/GPU Platform," *ACES*, Submitted, **2021**.

[13] W. Azad, F. Khan, and A. N. Caruso, "A Scalable Multilevel-Modular 10 kV Silicon Carbide MOSFET Module Featuring Custom Isolated Gate Driver Circuit Combined with Coupling and Snubber Circuits," *IEEE Transactions on Power Electronics*, Submitted, **2021.**

11.2.3 *Published / In Press*

[14] N. Gardner, K. C. Durbhakula, and A. N. Caruso, "Design Considerations for Diode-Based Nonlinear Transmission Lines," *AIP Advances*, 12, 055012, **May 2022** [doi].

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11.3 Conference Publications

11.3.1 *Submitted / Accepted*

[1] B. Barman, D. Chatterjee, and A. N. Caruso, "Characterization of Planar Phased Arrays of Electrically Small UWB Microstrip Patch Antennas," *2022 IEEE International Symposium on Phased Array and Technology,* Waltham, Massachusetts, USA, Oct. 11-14, 2022, pp. 1-8. (Submitted).

[2] B. Barman, D. Chatterjee, and A. N. Caruso, "On the Optimum Substrate Selection in Wideband Microstrip Patch Antenna Design," *2022 IEEE International Symposium on Antennas & Propagation & USNC-URSI Radio Science Meeting*, Denver, Colorado, USA, July 10-15, 2022, pp. 1-2. (Accepted)

[3] B. Barman, D. Chatterjee, and A. N. Caruso, "Time Domain Analysis of an UWB Electrically Small Microstrip Patch Antenna," *2022 IEEE International Symposium on Antennas & Propagation & USNC-URSI Radio Science Meeting*, Denver, Colorado, USA, July 10-15, 2022, pp. 1-2. (Accepted)

11.3.2 *Presented*

[4] S. R. Shepard and H. A. Thompson, “Self-focusing in Guided and Un-guided Media,” submitted to the *2021 OSA Nonlinear Optics Topical Meeting, Virtual Event*, August 9-13, 2021.

[5] B. Barman, D. Chatterjee and A. N. Caruso, "Probe-location Optimization in a Wideband Microstrip Patch Antenna using Genetic Algorithm, Particle Swarm and Nelder-Mead Optimization Methods," *2021 International Applied Computational Electromagnetics Society Symposium (ACES)*, 2021, pp. 1-3 [doi].

[6] W. Azad, S. Roy, and F. Khan, "A Single Gate Driver-based Four-stage High-voltage SiC Switch Having Dynamic Voltage Balancing Capability," *2021 IEEE Applied Power Electronics Conference and Exposition* (APEC), Phoenix, AZ, USA, June 9-12, 2021.

[7] W. Azad, S. Roy, F. Khan and A. N. Caruso, "A Multilevel-Modular 10 kV Silicon Carbide MOSFET Module using Custom High-Voltage Isolated Gate Driver, Coupling, and Snubber Circuits," *2021 IEEE Kansas Power and Energy Conference* (KPEC), Manhattan, KS, USA, April 19-20, 2021 [doi].

[8] T. Layman, T. D. Fields, and O. A. Yakimenko, "Evaluation of Proportional Navigation for Multirotor Pursuit," AIAA SciTech Forum, Virtual Event, January 11-21, 2021 [doi].

[9] P. J. Klappa, and T. D. Fields, "Assessment of Fixed-Wing UAV System Identification Models during Actuator and Payload Drop Failures," AIAA Atmospheric Flight Mechanics Conference, Virtual Event, January 11-21, 2021 [doi].

[10] J. Hunter, S. Xia, A. Harmon, A. M. Hassan, V. Khilkevich, and D. Beetner, "Modeling and Statistical Characterization of Electromagnetic Coupling to Electronic Devices," *IEEE International Symposium on Antennas and Propagation and NSRM USNC-URSI National Radio Science Meeting*, Boulder, CO, January 4-9, 2021 [doi].

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11.4 Conference Presentations

11.4.1 *Submitted / Accepted*

[1] S. Bellinger, A. Caruso, A. Usenko, "Stacked Diodes for Pulsed Power Applications," GOMACTech-22, Miami, FL, March 21–24 2022 (submitted, oral).

[2] S. Bellinger, A. Caruso, A. Usenko, "New Paradigm on Making Semiconductor Opening Switches for Pulsed Power," 2021 23rd IEEE Pulsed Power Conference, Denver, CO, Dec. 12–16, 2021 (accepted, oral).

Directed Energy Professional Society, Directed Energy Systems Symposium, Washington DC, October 25-29 2021 (submitted):

[3] B. Barman, D. Chatterjee, A. Caruso, and K. Durbhakula, "Tradespace Analysis of a Phased Array of Microstrip Patch Electrically Small Antennas (ESAs)" (Poster)

[4] J. N. Berg, R. C. Allen, and S. Sobhansarbandi, "A Novel Method of Cooling a Semiconductor Device through a Jet Impingement Thermal Management System: CFD Modeling and Experimental Evaluation" (Poster)

[5] J. N. Berg, R. C. Allen, and S. Sobhansarbandi, "Heat Transfer Enhancement of a Jet Impingement Thermal Management System: A Comparison of Various Nanofluid Mixtures" (Poster)

[6] J. Bhamidipati, M. Paquette, R. Allen, and A. Caruso, "Photoconductive Semiconductor Switch Enabled Multi-Stage Optical Source Driver" (Poster)

[7] G. Bhattarai, J. Eifler, S. Roy, M. Hyde, J. Bhamidipati, A. Usenko, M. Pederson, M. Paquette, A. Caruso, S. Bellinger, L. Voss, and R. Allen, "All Solid-State High-Power Pulse Sharpeners" (Poster)

[8] S. Brasel, K. Norris, R. Allen, A. Caruso, and K. Durbhakula, "Efforts to Reduce Physical Aperture Area of Ultra-Wideband Arrays" (Poster)

[9] A Caruso, "ONR Short Pulse Research and Evaluation for c-sUAV: Supporting and Sub-Programs Overview" (Oral)

[10] J. Clark, R. C. Allen, and S. Sobhansarbandi, "Ultra-Compact Integrated Cooling System Development" (Poster)

[11] J. Eifler, S. Roy, M. Hyde, G. Bhattarai, J. Bhamidipati, A. Usenko, M. Pederson, M. Paquette, A. Caruso, S. Bellinger, L. Voss, and R. Allen, "TCAD Optimization of Epitaxially Grown Drift-Step Recovery Diodes and Pulser Performance" (Poster)

[12] N. Gardner, M. Paquette, and A. Caruso, "Diode-Based Nonlinear Transmission Lines Capable of GHz Frequency Generation at Single MW Peak Powers" (Poster)

[13] M. Hamdalla, A. Caruso, and A. Hassan, “The Shielding Effectiveness of UAV Frames to External RF Interference” (Poster)

[14] M. Hamdalla, A. Caruso, and A. Hassan, “A Predictive-Package for Electromagnetic Coupling to Nonlinear-Electronics using Equivalent-Circuits and Characteristic-Modes (PECNEC)” (Poster)

[15] M. Hyde, J. Eifler, S. Roy, G. Bhattarai, A. Usenko, M. Paquette, A. Caruso, S. Bellinger, L. Voss, and R. Allen, “Development of an Evaluation Network for Drift Step Recovered Diodes through and Augmented Design of Experiment” (Poster)

[16] S. Indharapu, A. Caruso, and K. Durbhakula, “Machine Learning Based Ultra-Wideband Antenna Array Optimization and Prediction” (Poster)

[17] F. Khan, W. Azad, and A. Caruso, “A Scalable Multilevel-Modular 10 kV Silicon Carbide MOSFET Architecture for Pulsed Power Applications” (Poster)

[18] D. F. Noor, J. Eifler, M. Hyde, G. Bhattarai, S. Roy, J. Bhamidipati, A. Usenko, M. Pederson, M. Paquette, A. Caruso, S. Bellinger, L. Voss, and R. Allen, “DSRD-IES Pulsed-Power Generator Topology Study Using Machine-Learning-Based Feature Selection Optimization and Predictive Learning” (Poster)

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[20] S. Shepard and A. Caruso, “Tubular Core Optical Power Amplifier” (Poster)

[21] H. Thompson, M. Paquette, and A. Caruso, “Minimizing On-State Resistance in GaN:X Photoconductive Semiconductor Switches (PCSSs) for Direct Modulation (Poster)

[22] A. Usenko, J. Eifler, S. Roy, G. Bhattarai, M. Hyde, M. Paquette, A. Caruso, S. Bellinger, L. Voss, and R. Allen, “New Paradigm in Fabrication of Semiconductor Opening Switches for Pulsed Power” (Poster)

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[27] Stefan Wagner, Quickly Determining Minimum HPC Source Requirements Using Binary Search

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[28] Cash Hauptmann, Reduced Recovery Time in SiPCSS Photoconductive Switches

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[30] Steve Young, Two-Dimensional Optoelectronic Pulsed Power Switches: Initial Effort

[31] Adam Wagner, Rapid Cost Effective RF Component Prototyping Using 3D Printers

[32] Heather Thompson, Cost to benefit analysis of GaN for Photoconductive Semiconductor Switches

[33] Colby Landwehr, Low Leakage Electroluminescence For Improving SiPCSS Hold Off

[34] James Kovarik, Some Investigations Into Applications Of Electrically Small Antennas As Phased Array Elements

[35] Spencer Fry, Maximizing SiPCSS Efficiency For HPM Sources

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11.6 IP Disclosures Filed

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11.7 Provisional Patents Filed

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11.8 Non-Provisional Patents Filed

None to date

12 Appendix B: Direct RF Modulation Using GaN:C

(Heather Thompson)

12.1 Executive Summary

Silicon (Si) is commonly used in RF pulse generation systems utilizing photoconductive semi-conductor switches (PCSS) due to its technological maturity, availability, and low cost; however, as applications require more extreme operating ranges, it becomes necessary to consider other materials. Gallium nitride (GaN) is a wide-bandgap semiconductor (~3.4 eV) with material characteristics allowing for higher operating voltage, frequency, and temperature. The fast recombination of GaN also allows for direct modulation of the output pulse by altering the photon source characteristics (i.e., pulse-width, rise-time, etc.), which also eliminates the need for pulse forming transmission lines that can be ones-of-feet long and allows for PCSS operation using a small PCB. Towards proving proof-of-concept, two different PCB were set up to allow for unipolar and bipolar modulation and optical delay system setup to provide various time delays between pulses. Unipolar modulation was successfully demonstrated at >2 kV, with higher voltages being unobtainable due to surface flashover between the PCSS contacts. Bipolar modulation was achieved at low voltages by adding a second PCSS, operating with negative bias, showing proof-of-concept for direct RF modulation using GaN:C PCSS. Further testing using a picosecond laser with quicker rise-time and 70 ps pulse-width was not achievable as the resulting usable laser energy, after conversion to 355 nm, did not allow for a low enough on-state resistance in GaN PCSS. Work was subsequently stopped as focus shifted to other OSPRES projects.

12.2 Objective

Primary Problem: Need for a more compact, cost-effective RF pulse generation system for Navy afloat missions on smaller vessels and vehicles.

Solution Space: Improve efficiency and reduce necessary material, size, and thermal requirements by utilizing gallium nitride (GaN) in photoconductive semiconductor switches (PCSS) through exploitation of its material properties, which can theoretically allow for higher operating voltages, frequencies, and temperatures, while also eliminating the need for pulse-shaping transmission lines through direct RF modulation using the laser/photon source driving the PCSS.

Sub-Problem: Lack of maturity in compensated gallium nitride semiconductor (i.e., GaN:X with X=C,Fe) PCSS manufacturing, development, and optimization.

State-of-the-art (SOTA):

Silicon-based technologies:

(1) Theoretical breakdown of 0.3 MW/cm limiting operating voltage leading to larger devices—contributing to increased overall system size—to reach >10 kV operating voltage.

(2) For minimizing on-state resistance and maximizing efficiency, ~100 μJ optical pulses per 4 MW of peak power, increasing the size of laser necessary for device triggering.

(3) Ones-of-μs recovery time, limits quick device turn on and high pulse-repetition rate operation and leads to increased device heating and increased cooling requirements.

(4) Operating temperature of <160 °C leading to increased cooling requirements.

Solution Proposed:

Replacing Si with GaN:C:

(1) Theoretical breakdown of 3 MV/cm allowing for higher operating voltage per device area allowing for smaller devices at similar operating parameters as Si.

(2) Fast recombination time allows for output pulse modulation determined by the incident laser characteristics (rise-time, pulse width, etc.), allowing for direct RF modulation eliminating the need for bulky pulse-forming transmission lines (~3 ft long).

(3) Incident optical energy of ~20 μJ needed for peak power operation at >3 MW, reducing the size of laser.

(4) Theoretical operating temperature of ~500°C (limited by circuit components and materials) reducing system cooling needs and allowing for operation in harsh environments.

Relevance to OSPRES Grant Objective: Reduction in size and cost for cooling system, removal of a pulse-shaping system, and decrease in material cost, leading to enhanced SWaP-C^2 capability with greater modularity and scalability.

Risks, Payoffs, and Challenges: Due to manufacturing limitations, GaN PCSS devices tend to be limited to lateral geometries (both contacts on the top side of the device), limiting operating voltage due to current crowding and surface flashover. The recovery time (ones-to-tens-of-ns) may lead to device heating and increased DC content when generating RF content with a period on the same order as the recovery time.

12.3 Technical Background

RF generation using PCSS devices is commonly done with silicon (Si) due to its technological maturity and low material cost, but its narrow bandgap and material characteristics cause deficiencies in performance that can be overcome by using a wide-bandgap material such as gallium nitride (GaN). The bandgap (~3.4 eV) of GaN, along with its higher electric field breakdown, faster saturation electron velocity, and drift-velocity (Figure 12.1.1), allow for operation at higher operating voltages, frequencies, and temperatures, leading to an overall system with a reduced form factor and increased SWAP-C^2 capabilities [1].

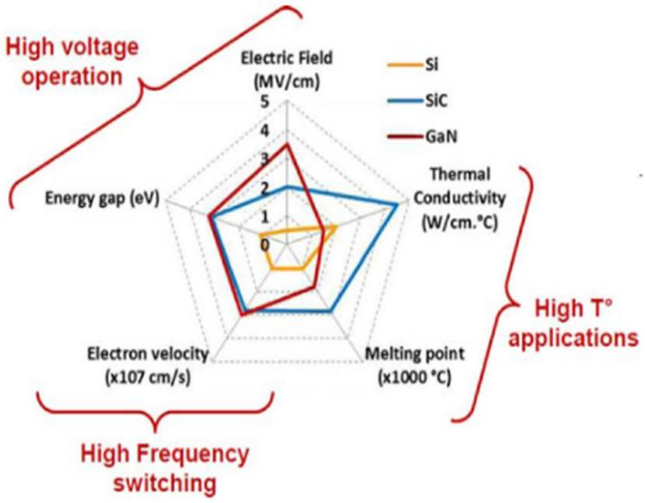

Figure 12.1.1. Comparison of Si, SiC, and GaN material properties [1].

The fast recombination in GaN allows for output pulse—thus frequency content—determination based on the characteristics of the incident light source (Figure 12.1.2). Utilizing the quick recombination time allows for GaN:C-based PCSS to be used as a frequency agile RF source by altering the incident laser rise-time, pulse-width, pulse repetition rate, and delay time towards eliminating the bulky pulse-forming transmission lines required in Si-based PCSS systems.

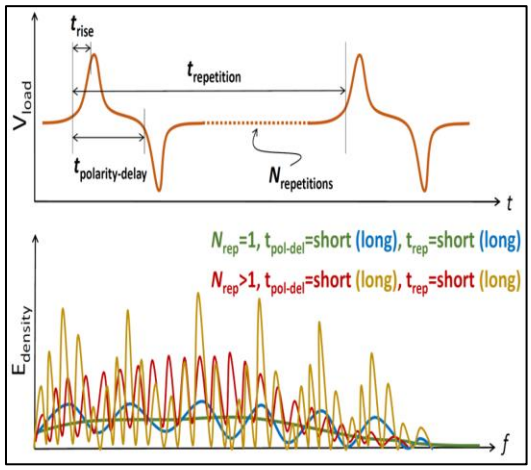

Figure 12.1.2. Diagram demonstrating possible ways of direct RF modulation of GaN:C.

Gallium arsenide (GaAs) is another commonly used narrow-bandgap material that is readily available, but unlike Si, has a direct bandgap and faster recombination time, allowing for laser characteristics to again dictate the output pulse achieved using PCSS. Direct RF modulation has been demonstrated using GaAs PCSSs by Stoudt et al [2], and they were able to show that a frequency agile RF source was possible, as shown in Figure 12.1.3, at ones-of-GHz operation. This work served as the inspiration for using GaN as a frequency agile RF source through direct modulation.

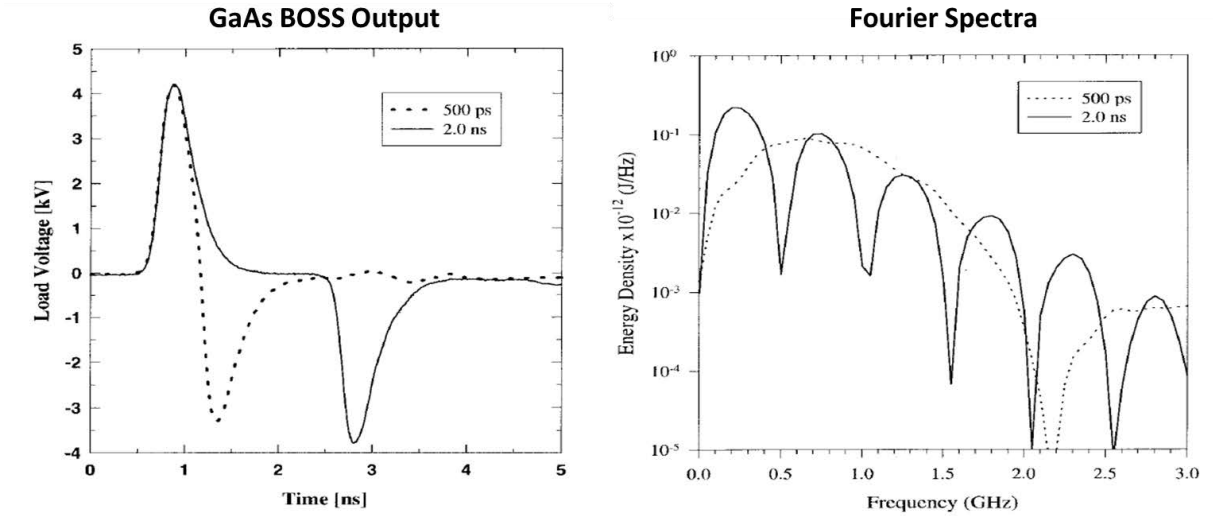

Figure 12.1.3. (Left) Plot of GaAs BOSS output utilizing bipolar modulation output for direct RF modulation. (Right) The Fourier spectra resulting from the GaAs PCSS output.

12.4 Tasks, Milestones, and Status

(A) **Dec 2020** Demonstrate GaN:C PCSS high-voltage operation (ones-of-kV to start) using pulse charger obtained from the HV switch development team. [Complete]

(B) **Jan 2021** Demonstrate RF unipolar modulation in the 1–2 GHz regime and up to 2 kV operating voltage with current PCB setup and the automated optical delay system. [Complete – up to >1 kV]

(C) **March 2021** Demonstrate RF bipolar modulation using two GaN:C devices, along with a positive and negative power source, based on the pulse-switch-out-generator-based circuit and setup with the automated optical delay system. [Complete – at low voltage only]

(D) **April 2021** Move test setup and show higher center frequency content and repetition frequency of unipolar and bipolar modulation using the neoLASE (70 ps) laser versus the wedge (~1.5 ns) laser. [Complete – neoLASE had insufficient laser energy after converting to 355 nm to allow for minimal on-state resistance in GaN PCSS]

(E) **May 2021** Complete study of recovery for differing gap lengths, incident energies, and operating voltages and find solutions to reduce the recovery time. [Incomplete as efforts were focused on other OSPRES projects.]

12.5 Methods and Approach

Due to the wide bandgap of GaN, incident UVA light is necessary for device activation, and therefore converting the existing IR source to UV using second- and triple-harmonic generation (SHG/THG) is necessary (Figure 12.1.4). To manipulate the output, a free-space optical delay is set up to be adjustable, enabling the control of timing between pulses for manipulation of RF frequency output and allowing for frequency agility.

Towards maintaining a small form-factor, a PCB is used to connect two PCSSs to a positive and negative power source and pulse charger, allowing for bipolar modulation (Figure 12.1.5). The outputs are then measured using an oscilloscope and plotted using Origin.

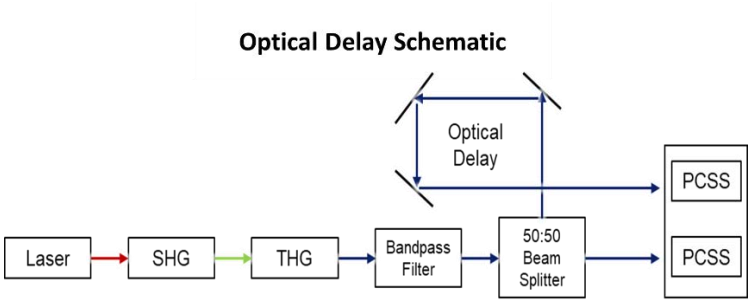

Figure 12.1.4. Optical delay schematic for bipolar RF modulation using GaN:C PCSS.

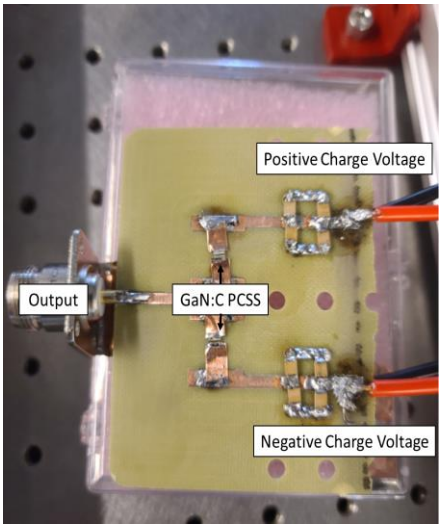

Figure 12.1.5. PCB layout for bipolar direct modulation using GaN:C PCSS.

12.6 Results and Discussion

Unipolar modulation using one GaN:C PCSS with free-space optical delay was demonstrated at <2 kV using a wedge laser (~1 ns rise-time). It is expected that adding a second GaN:C PCSS, operating using negative bias, and adjusting the timing between the two pulses, will result in a decrease of non-radiating DC content and allow for frequencies in the hundreds of MHz to ones of GHz to be achievable. The attained unipolar output is shown on the top left in Figure 12.1.6, with the expected bipolar output and bipolar FFT output shown in the same figure, with resulting frequencies in the hundreds-of-MHz range. Results at higher voltages were not achieved due to flashover occurring across the contacts of the GaN PCSSs even when using encapsulating material, Sylgard 184, as air bubbles in the Sylgard, after vacuum curing, allowed for arcing between the contacts.

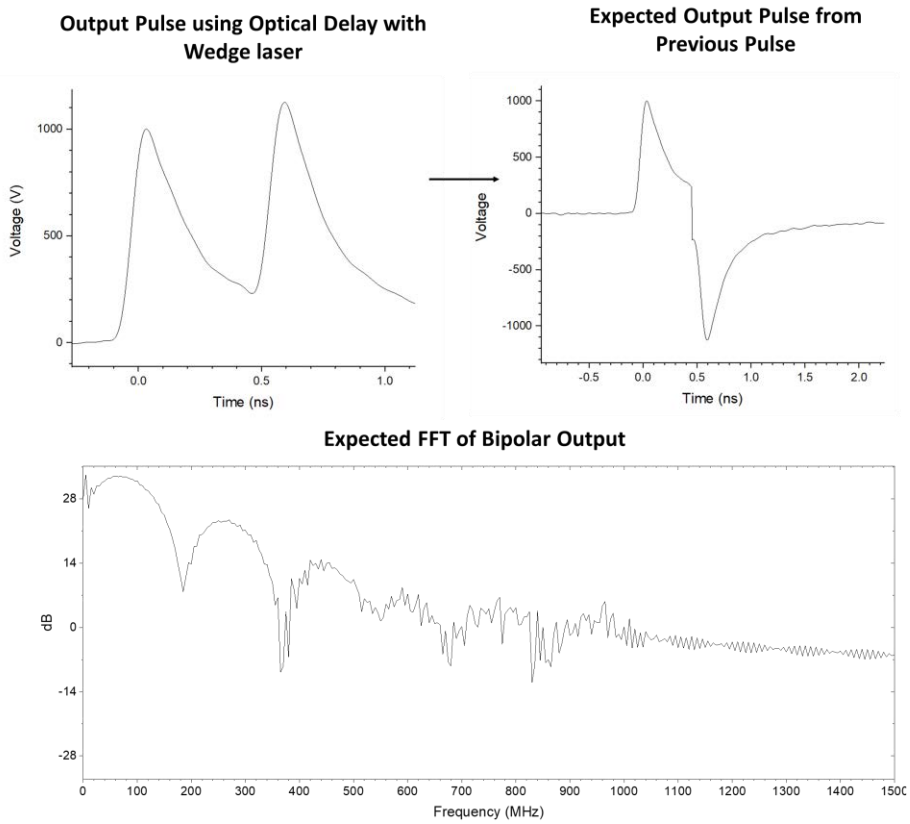

Figure 12.1.6. (Top Right) Unipolar modulation output using GaN:C PCSS. (Top Left) Expected bipolar output using GaN:C PCSS, determined from unipolar modulation results. (Bottom) Expected Fourier spectra of bipolar output using GaN:C PCSS for direct RF modulation.

Bipolar output was achieved at low voltage (~10 V) as a proof-of-concept for the PCB/direct modulation using two GaN devices. To achieve higher voltages and power, a different power supply is required. The resulting bipolar pulse is shown in Figure 12.1.7.

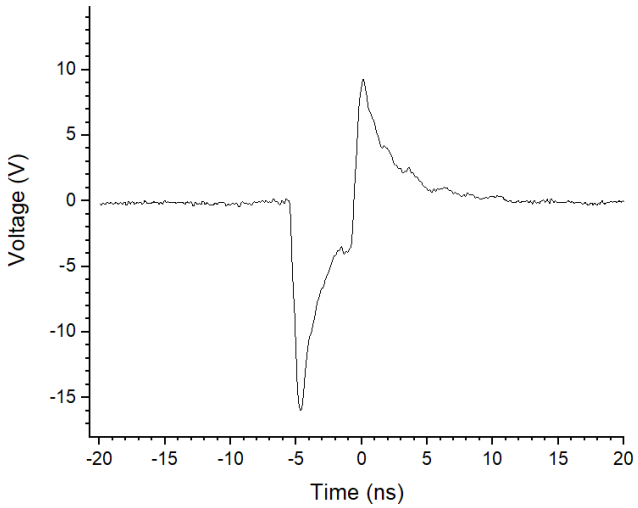

Figure 12.1.7. Bipolar output using GaN:C PCSS at low voltage for proof-of-concept towards direct bipolar RF generation.

To allow for higher frequency content, bipolar modulation using the neoLASE laser (70 ps vs ~1 ns pulse-width) was planned because of this photon source offering a quicker rise time. The optical delay and SHG/THG setups were moved to work with this laser and conversion to 355 nm was successful; however, only ~6 μJ of energy was left after conversion, which then needed to be split approximately in half for the free-space optical delay. Because of this small usable energy, there was not enough laser power to reach low enough on-state resistance to demonstrate outputs using quicker rise-time and pulse-width. To overcome this challenge, a different laser with similar rise-time and pulse-width but higher laser energy would need to be sourced. Further testing ceased as efforts were put towards other OSPRES projects.

12.7 Summary and Recommendations

GaN is a promising material for RF generation systems offering higher operating voltage, power, and temperature while maintaining or reducing the system form-factor over Si. The fast recombination time of GaN also allows for direct output modulation using the incident photon source activating the PCSS, negating the need for bulky pulse-forming transmission lines and allowing for device operation using a small PCB. Unipolar operation was demonstrated at >2 kV, with higher voltage results not being obtained due to flashover between the contacts. Bipolar modulation was shown at 10 V as a proof-of-concept, but higher voltage operation not demonstrated due to lack of needed power supply allowing for higher negative bias operation. Further results using the neoLASE, which offers a quicker rise-time and pulse-width, for higher output frequency output was not achieved as there was insufficient usable energy once this laser was converted to 355 nm using SHG/THG, thus low enough on-state resistance was not achieved in GaN PCSS using this laser. Further work was stopped due to efforts being placed towards other OSPRES projects. Future success using GaN:C PCSS would benefit from a comprehensive study of minimizing on-state resistance to allow for devices with wider

gap lengths and/or device type (lateral vs. vertical) towards eliminating arcing between contacts at >2 kV operation. Studies should include allowing operation using a higher incident wavelength (405 or 532 nm) and less incident energy (number of incident photons) to reduce incident photon source cost and size.

12.8 References

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[2] Stoudt, D. C., Richardson, M. A., & Peterkin, F. E. (1997). Bistable optically controlled semiconductor switches in a frequency-agile RF source. IEEE Transactions on Plasma Science, 25(2), 131–137. https://doi.org/10.1109/27.602483

13 Appendix C: Tradespace Analysis of UWB Antenna Elements

(Kalyan Durbhakula)

13.1 Executive Summary

In this tradespace analysis, we have assembled, compared, and analyzed multiple ultra-wide-band (UWB) single-element antennas using the information available in the literature to downselect at least 5 UWB antenna elements. A detailed comparison has revealed five specific UWB antenna elements that could potentially exceed the performance of the state-of-the-art (SOTA) balanced antipodal Vivaldi antenna (BAVA) upon careful study and optimization. The five antenna elements are then compared against the SOTA BAVA for reflection coefficient (S_{11}) bandwidth (≤10 dB), peak gain at the center frequency, directionality, full-width half-maximum, ringing, electronic beam steerability, high-power handling capability, and aperture efficiency. The comparison led to further downselection of antenna elements to: the Koshelev antenna, the Shark antenna, and the Fractal antenna. The Koshelev antenna packs multiple resonances over a wide frequency range in a smaller volumetric size, enabling UWB characteristics. The Shark antenna (a variant of the Bicone antenna) offers directionality without sacrificing bandwidth or gain. The Fractal antenna has a broader scope for shape optimization and bandwidth enhancement in a smaller aperture area. Future efforts will demonstrate improvements with respect to three downselected antenna elements using parametric sweep and/or metrics-based optimization.

13.2 Objective

Primary Problem: Determine the extent to which the physical aperture size of an antenna array, composed of patch elements, can be reduced, while maintaining performance in peak power density, bandwidth, and electronic beam steerability over the UHF range (0.4–1 GHz), compared with the present art high power microwave capable antenna arrays.

Solution Space: Through a survey, three new antenna elements (Fractal, Shark, and Koshelev) were identified. The downselected antenna elements can be further analyzed using tradespace study (via parametric sweep) to compare and demonstrate improvements in metrics such as bandwidth, antenna gain, and transient gain while maintaining the smallest aperture area possible.

State-of-the-Art (SOTA)/Deficiency in SOTA: The balanced antipodal Vivaldi antenna (BAVA) is the SOTA antenna element due to its exceptional 20:1 impedance bandwidth ratio as well as the ability to handle tens-of-MW input power. The BAVA design parameter space has been exhausted over the past couple of decades. The physical aperture area remains very large and there is no viable path through tradespace study for further physical aperture area reduction.

13.3 Technical Background

We expand on the methodology and technical reasoning employed towards the downselection of specific UWB antenna elements (or single elements) [1-21]. The tradespace analysis began with a thorough literature search on the existing wide range of antenna elements that possess the key UWB performance metrics. In this effort, a list of key metrics has been put together that helps with comparing downselected antenna elements and therefore make important design decisions for further tradespace studies.

Fig. 13.3.1 shows a total of 29 different antenna and size, weight and power (SWaP) metrics (or research parameters) that are available for comparing selected UWB antenna elements. Some of these metrics (scattering parameters, radiated electric field, bandwidth, realized gain, etc.) are readily available directly from measurement/simulation, while others (fidelity factor, impulse response, energy density, envelope, etc.) require post-processing. It is practically difficult to compare antenna elements for all these metrics; therefore, we have downselected to the most important ones. The downselected metrics are frequency-dependent dimensions (size expressed in terms of wavelength at the center frequency), bandwidth (in hertz), peak gain (dBi), directionality (Omni vs directional) in both planes (E-plane & H-plane), ringing, electronic beam steering, aperture efficiency, and effective radiated power. In the time-domain response of antennas, other metrics such as transient gain (rE/V), and radiated electric field are also deemed to be important and were considered for some comparisons.

Research Parameter/Metric Context Description:

1. **Physical aperture area**
2. **Effective aperture area**
3. **Aperture efficiency**
4. **Center frequency**
5. **Bandwidth**
6. **Realized gain**
7. **Directionality**
8. **E-plane, H-plane patterns**
9. **Half-power beamwidth**
10. **Side lobe levels**
11. **Electronic Beam Steering**
12. **Mutual coupling**
13. **Peak/Avg. power**
14. **Pulse shape (Mono./Diff./Bipolar)**
15. **Radiated E-field**
16. **Waveform dispersion**
17. **rE/V**
18. **Pulse width**
19. **Rise time**
20. **Fidelity factor**
21. **Envelope**
22. **Pulse repetition frequency**
21. **Impulse response/Transfer function**
22. **Full width half maximum (FWHM)**
23. **Effective radiated power (ERP)**
24. **Polarization**
25. **Energy density**
26. **Energy pattern**
27. **Ringing**
28. **Breakdown voltage**
29. **Profile, Cost, Manufacture difficulty**

Figure 13.3.1. A list of different antenna metrics (single element and array) under a time-domain excitation.

The design requirements have been defined to assist with the design optimization.

- Wide frequency band (500 MHz or more) or cover the short pulse frequency spectrum.
- Withstand input waveforms with high peak-to-peak input voltages (>10 MW) and high pulse repetition frequencies (10’s to 100’s of kHz).
- Possess directionality in the E-plane and the H-plane.

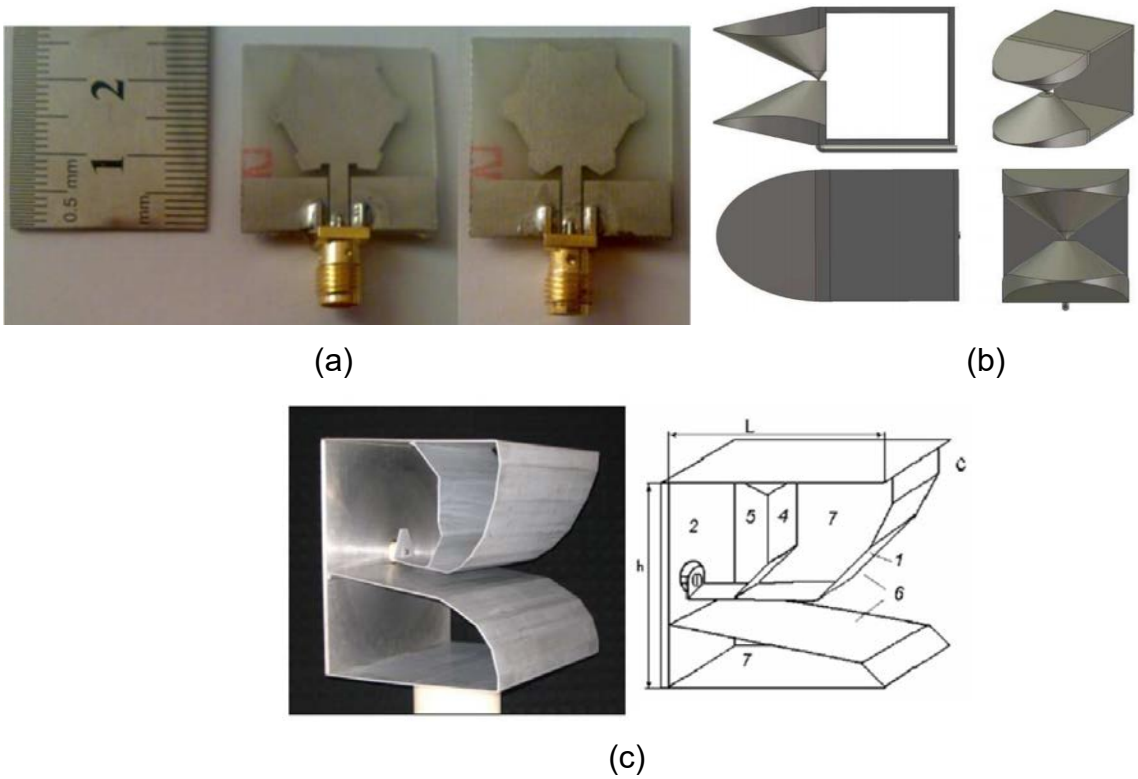
Based on the taxonomies defined above, a select list of single-element antennas has been identified for UWB HPM applications. The list consists of:

1. Shark antenna (high aperture efficiency)
2. TEM horn (Flare, Exponential, K) and double ridge guide horn
3. Log-periodic dipole (dispersive, low power handling capability)
4. Spiral antenna (small aperture area, circular polarization)
5. Helical antenna (difficult to steer and circular polarization)
6. Full and half Impulse radiating antenna, lens IRA
7. Centered and offset reflectors
8. Fractal antennas (good fidelity factor)
9. Bowtie antenna (omnidirectional in H-plane)
10. Monocone antenna (omnidirectional in H-plane)
11. Koshelev antenna (withstand > 460 kV peak to peak)
12. Leaky-wave antenna (high directivity, difficult to steer)
13. Valentine antenna

Table 13.3.1. Antenna Element Survey for Reduced Aperture Area UWB Arrays.

Antenna element type	Dimensions (single element)	Bandwidth	Peak gain (dBi)	Directionality		FWHM	Ringing	Aperture efficiency
				E-plane	H-plane			
BAVA (SOTA)	-	> 25:1	8	Dir.	Dir.	Low (≈ 135 ps)	Low (≈ 150 ps)	> 90%
Spiral antenna	D = λ/π	10:1	7.5	Dir.	Dir.	Around 200 ps	Around 250 ps	40% to 50%
Shark antenna	λ/3.52 × λ/3.36 × λ/1.91	10:1	7–8	Dir.	Dir.	Lower than vivaldi	Unknown	Unknown
Koshelev antenna	-	6:1	6–8	Dir.	Dir.	Unknown	Unknown	85% (energy efficiency)
Fractal antenna	-	4:1	4–6	Dir.	Dir./Omni	Assuming low (100 to 200 ps) due to good fidelity factor reported in literature	Assuming low due to good fidelity factor	> 90%
Leak wave antenna	0.83λ (length, 1D)	≈ 2:1 or less	7–8	Dir.	Dir.	Higher than Vivaldi	Higher than Vivaldi	50% to 60%

The pros (green text) and cons (red text) provided an initial understanding of radiating properties. The antennas with pros have been downselected and compared against the SOTA BAVA using the downselected key performance metrics. Table 13.3.1 presents a comprehensive comparison of the downselected antenna elements and the BAVA. The comparison is drawn from the designs reported in the literature. Although they do not exceed the performance of the BAVA, the downselected antennas have not yet been rigorously optimized for our metrics of interest (bandwidth, low ringing/fidelity, aperture efficiency, etc.). The comparison presents how each of the downselected antenna elements perform when compared against the SOTA BAVA and identifies metrics requiring improvement through design optimization and tradespace study. Out of five initially identified antenna elements, the spiral antenna and the leaky-wave antenna were removed from contention. The spiral antenna is omni-directional, whereas the leaky-wave antenna has limited scope for bandwidth enhancement and possesses minimum (<30° steerability). The Koshelev, Shark, and Fractal antennas have been selected as the final candidates for shape optimization and tradespace study. Fig. 13.3.2 shows computer-aided design (or fabricated) models of the three downselected antennas.



(a) (b)

(c)

Figure 13.3.2. (a) Fractal antenna (b) Shark antenna and (c) Koshelev antenna.

13.4 Summary and Recommendations

The tradespace analysis revealed three new UWB antenna elements that meet the OSPRES grant objective in terms of power handling and compactness while meeting the desired bandwidth (>500 MHz) and high transient gain (>1). The three elements will need to be further studied and optimized for a one-to-one comparison against the SOTA.

The Koshelev, Shark, and Fractal antennas offer the potential for bandwidth enhancement in a smaller aperture area than the SOTA leading to high aperture efficiency. Some challenges remain in the field of manufacturability such as obtaining smooth hexagon edges in the Fractal antenna (for better high-frequency performance) and fabricating tapered coax (50 ohms to 150 ohms) in the Shark antenna.

13.5 References

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ONR HPM Program – Monthly Status Report (MSR) – September 2022

Anthony Caruso – Univ. Missouri – Kansas City

N00014-17-1-3016 [OSPRES Grant]

Period of Performance – 30SEPT2017–29SEPT2022

ONR Short Pulse Research, Evaluation and non-SWaP Demonstration for C-sUAS Study

15 OCT 2022

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OSPRES Grant Security: All efforts should be fundamental and publicly releasable in nature when taken individually. This report has been reviewed for operational security, compilation, proprietary and pre-decisional information concerns.

1 Contents

2 Executive Summary

2.1 Progress, Significant Findings, and Impact

Fiber Laser and Optical Amplifiers. Some of our research on high-power multiple tube power amplifiers [of micron scale dimension] is also applicable to RF resonators, e.g., in considering the influence of an anti-reflective coating we simultaneously analyze those of a quarter-wave transformer on matching other structures to resonant loads. We transfer our resonance findings and techniques into RF (specifically reconfigurable antenna design) and further their development within the context of how photonic crystals (an array of air holes) can enhance the performance of patch antennas [with structures on the scale of millimeters]. These foundations for further study have already shown that we can dramatically move a minimal reflection coefficient (S11) from 4.7 GHz to 900 MHz by changing the index of refraction from 1 to 3 within the material inside the holes.

DSRD Optimization: Measurements and Simulations. The DSRD inventory has been fit for LTspice parameters within the standard diode model for IV, CV, and reverse recovery testing (RRT). These parameters are closely fit to accurate experimental diode characterization measurements and are necessary for the LTspice simulations to design and optimize DSRD-based pulsers. With these parameters and simulations the performance of DSRD pulsers for peak voltage can be maximized more successfully.

DSRD-Based Pulsed Power Source Optimization. Update

Pulse-Compression-Based Signal Amplification. Several design constraints related to energy transfer and inductor saturation were investigated for accurate evaluation of high frequency magnetic pulse compression (MPC) viability. Both magnetic cross-sectional area and path length need to be minimized in order to ensure maximum energy transfer and inductor saturation. High frequency MPC magnetic material needs B_{sat} < 10 mT to achieve saturation when interfaced with a solid-state amplifier operating at 1 GHz. Even though lower frequency load resistor for optimal energy transfer is limited to mΩ range, 50 Ω loading can easily be achieved at 1 GHz.

Antennas. We completed the manufacturing of the improved version of a tapered, coaxial-connector-fed, single microstrip patch antenna element for operation in the UHF region (0.7–1.3 GHz). Around 58% (0.712–1.299 GHz) of measured impedance bandwidth is achieved from the single antenna element, which is significantly higher compared to conventional, microstrip patch antenna designs that have $\sim 8-10\%$ of bandwidth. Due to prior technical failures, the prototyping of the final 4×4 array model could not be initiated on time. However, the acquired knowledge can be utilized in the future to rapidly manufacture multiple high-performance and cost-effective prototypes. The full array performance will be demonstrated using simulation results at the NOV2022 ONR OSPRES-G Program Review Meeting.

The Koshelev antenna with partial dielectric transformer prototype has been measured for gain, and demonstrated a convergence with the simulated gain data from 350 MHz to 1.8 GHz. Beyond 1.8 GHz, experimental and simulated responses diverged due to non-ideal measurement conditions. The 3-D printed antenna prototype by the UMKC team is functional as expected and demonstrates our ability to design, optimize, and prototype an

ultrawideband antenna that yields fundamental improvements impactful to the mission. The simulation comparison between the proposed Koshelev antenna and the state-of-the-art balanced antipodal Vivaldi antenna resulted in the Koshelev antenna performing better than the BAVA in terms of transient gain and aperture area while not quite showing an advantage in the steerability. In the case of an array, the high-transient gain from the Koshelev antenna over the BAVA implies that the proposed antenna would be an ideal choice for a ground-based HPM system.

A machine learning (ML)-based predictive tool has been developed using MATLAB that can estimate and display antenna metrics (bandwidth, radiation pattern, electric field in time-domain etc.) with a root mean square error (RMSE) < 2 while using $1/100^{th}$ the computational time of conventional methods (Method of Moments or Finite Integration Technique). The in-house tool is also capable of calculating optimum design variables with the help of the genetic algorithm. This tool can eventually be utilized to predict and optimize an antenna element or array of choice with high-accuracy and low-latency.

Outputs. The outputs section has been substantially updated in preparation for the final report.

2.2 Completed, Ongoing, and Cancelled Sub-Efforts

	Start	End
2.2.1 *Ongoing Sub-Efforts*		
GaN:C Modeling and Optimization	OCT 2017	Present
Diode-Based Non-Linear Transmission Lines	FEB 2018	Present
Trade Space Analysis of Microstrip Patch Arrays	FEB 2019	Present
Lasers and Optics	FEB 2020	Present
UWB Antenna Element Tradespace for Arrays	MAY 2020	Present
Si-PCSS Contact and Cooling Optimization	JAN 2021	Present
Drift-Step Recovery Diode Optimization Simulations	JAN 2021	Present
DSRD-Based IES Pulse Generator Development	APR 2021	Present
Drift-Step Recovery Diode Manufacturing	MAY 2021	Present
DSRD Characterization through Design of Experiments	MAY 2021	Present
Sub-Nanosecond Megawatt Pulse Shaper Alternatives	MAY 2021	Present
Ultra-Compact Integrated Cooling System Development	MAY 2021	Present
Continuous Wave Diode-NLTL Based Comb Generator	SEPT 2021	Present
Pulse-Compression-Based Signal Amplification	DEC 2021	Present
2.2.2 *Completed/Transferred Sub-Efforts*		
Adaptive Design-of-Experiments	OCT 2017	APR 2019
Non-perturbing UAV Diagnostics	OCT 2017	OCT 2018
Noise Injection as HPM Surrogate	OCT 2017	MAR 2019
SiC:N,V Properties (w/ LLNL)	APR 2018	MAR 2019
Helical Antennas and the Fidelity Factor	JUL 2018	SEPT 2019
Si-PCSS Top Contact Optimization	APR 2020	OCT 2020
Nanofluid Heat Transfer Fluid	NOV 2020	JUL 2021
HV Switch Pulsed Chargers	DEC 2018	DEC 2021
Enclosure Effects on RF Coupling	OCT2019	DEC 2021
UAS Engagement M&S	MAR 2021	DEC 2021
GaN-Based Power Amplifier RF Source	AUG 2021	DEC 2021
2.2.3 *Cancelled/Suspended Sub-Efforts*		
Ab Initio Informed TCAD	OCT 2017	OCT 2020
Positive Feedback Non-Linear Transmission Line	NOV 2017	DEC 2018
Minimally Dispersive Waves	FEB 2018	SEPT 2018
Multiferroic-Non-linear Transmission Line	NOV 2018	APR 2019
Avalanche-based PCSS	SEPT 2018	SEPT 2019
Gyromagnetic-NLTL	DEC 2017	NOV 2020
Multi-Stage BPFTL	APR 2020	JUL 2020
Heat Transfer by Jet Impingement	MAY 2018	FEB 2021
Si, SiC, and GaN Modeling and Optimization	NOV 2018	FEB 2021
Bistable Operation of GaN	FEB 2021	MAR 2021
WBG-PCSS Enabled Laser Diode Array Driver	NOV 2020	JAN 2022

2.3 Running Total of Academic and IP Program Output

See Appendix for authors, titles and inventors (this list is continuously being updated)

Students Graduated	*15 BS, 12 MS, 7 PhD*
Journal Publications	*13 published (5 submitted/under revision)*
Conference Publications	*45 (1 submitted/accepted)*
External Presentations/Briefings	*53 (2 submitted/accepted)*
Theses and Dissertations	*10*
IP Disclosures Filed	*12*
Provisional Patents Filed	*4*
Non-Provisional Patents Filed	*2*
Allowed/Issued Patents	*1*

3 Laser Development

3.1 Fiber Lasers and Optical Amplifiers

(Scott Shepard)

3.1.1 *Problem Statement, Approach, and Context*

Primary Problem: High-average-power 1064-nm picosecond lasers are too large (over 1100 cm^3/W) and too expensive (over \$1000/μJ per pulse) for PCSS (photoconductive semiconductor switch) embodiments of HPM-based defense systems. For example, a laser of this class might occupy a volume of 1 m x 30 cm x 30 cm = 90,000 cm^3 and provide an average power of 50 W (thus, 1800 cm^3/W). Costs in this class range from \$100K to \$300K to drive our Si-PCSS applications.

Solution Space: Optically pumped ytterbium-doped optical fiber amplifiers, fed by a low-power stable seed laser diode, can offer a cost-effective, low-weight, and small-volume solution (with respect to traditional fiber and traditional free-space laser designs). Moreover, our novel optical amplifier tubes, might operate at far higher power levels (over 1000 times greater), thus driving an entire array of PCSS with a single amplifier and thereby reducing the overall system costs and eliminating the optical pulse-to-pulse jitter constraints.

Sub-Problem (1): Optical pump power system costs account for over 50% of the budget for each laser (in this class, for normal/free-space, optical fiber, and tubular embodiments).

Sub-Problem (2): Fiber (as well as power tube) optical amplifier performance is degraded primarily by amplified spontaneous emission (ASE) noise, which limits the operating power point, and by nonlinearities, which distort the optical pulse shapes.

State-of-the-Art (SOTA): Free-space NdYAG lasers or Ytterbium-doped fiber amplifiers optimized for LIDAR, cutting, and other applications.

Deficiency in the SOTA: Optical pump power system costs (in either free-space or fiber lasers) are prohibitive for the PCSS applications until reduced by a factor of at least two.

Solution Proposed: Fiber lasers permit a pre-burst optical pumping technique (wherein we pump at a lower level over a longer time) which can reduce pumping costs by a factor of at least ten. To address the ASE and nonlinear impairments, we are pursuing the use of gain saturation and a staged design of different fiber diameters. We also apply these techniques to fiber amplifiers which incorporate our power amplifier tube in the final stage. The inclusion of our novel tubular-core power amplifier stage should permit a single laser to trigger an array of several PCSS (reducing system cost and mitigating timing jitter).

Relevance to OSPRES Grant Objective: The enhancement in SWaP-C^2 for the laser system enables PCSS systems for viable deployment via: a factor of 40 in pumping cost reduction of each laser; and a factor of *N* in system cost reductions as a single laser could drive *N* (at least 12) PCSS in an array, while also eliminating the optical jitter constraints.

Risks, Payoffs, and Challenges: Optically pumping outside the laser pulse burst time can enhance the ASE; pump costs could be reduced by 40, but ASE in the presence of dispersion and/or nonlinearities could enhance timing jitter thereby limiting steerability. The main challenge for power tube implementation is the entrance optics design.

3.1.2 *Tasks and Milestones / Timeline / Status*

(A) Devise a pre-burst optical pumping scheme by which we can reduce the costs of the laser by a factor of two or more and calculate the resulting increase in ASE. / FEB–JUL 2020 / Completed.

(B) Reduce the ASE via gain saturation. / Oct 2020 / Completed.

(C) Design saturable gain devices which avoid nonlinear damage. / Completed.

(D) Calculate and ensure that timing jitter remains less than +/-15 ps with a probability greater than 0.9. / Completed.

(E) Demonstrate a cost-reduced fiber laser: the level of success to be quantified via the amount of ASE growth per duration of a pre-burst pumping interval. Growth of 100 uw over 6 ms (the limit in theory) would be considered outstanding. / August 2022.

(E1) March 2021 Finalize design. / Completed.
(E2) April 2021 Assemble and test-check seed LD (laser diode)/driver. / Completed.
(E3) April 2021 Measure power vs current transfer function of seed LD/driver. / Completed.
(E4) May–July 2021 Measure ASE and jitter of 1064 nm seed LD/driver. / Completed.
(E5) May–July 2021 Measure ASE and jitter of 1030 nm seed LD/driver. / Completed.
(E6) June–July 2021 Assemble and test-check pump LDs/drivers. / Completed.
(E7) June–July 2021 Measure power vs current transfer function of pump LDs/drivers. / Completed.
(E8) July–September 2021 Splice power combiners to Yb doped preamp fiber. /Completed.
(E9) July–September 2021 Connect seed and pumps to power combiners and test-check. / Completed.
(E10) September–October 2021 Measure gain, ASE and jitter of 1064 nm preamp assembly (forward, backward and bidirectional pumping) as a function of pump power and duty cycle. / Partially completed before task eliminated.
(E11) September–October 2021 Measure gain, ASE and jitter of 1030 nm preamp assembly (forward, backward and bidirectional pumping) as a function of pump power and duty cycle. / Partially completed before task eliminated.
(E12) November 2021 Splice power amplifier and its power combiner to best preamp. / Partially completed before task eliminated.
(E13) May–August 2022 Measure gain, ASE and jitter of entire amp assembly. / Sunset.
(E14) May–August 2022 Analyze data and document. / Sunset.

(F) Design a new type of higher power, tubular core fiber amplifier. / May–August 2022. / Completed.

(F1) Apply one high-power tubular amplifier to a system comprised of an array of several (say N) PCSS. For example: N=12 in a 3x4 array (or 4x4 array with corners omitted) N=16 in a 4x4 array, etc.; thereby eliminating jitter constraints and reducing laser system cost by more than a factor of 100 (independent of burst profile). / August 2022. / Completed.

(F2) Design a high power, multiple tube optical amplifier and determine if it permits advantages for power handling or beam profile. / August 2022 / Completed.

(G1) Design a beam shaping, optical power combiner using a cladding of 6 tubes. / June 2022 / Completed.

(G1.1) Develop COMSOL models. / April 2022 / Completed.

(G1.2) Discover and optimize the length at which the cladding modes couple maximal power into the core mode (of the entire waveguide). / June 2022 / Completed.

(G2) Design a beam shaping, optical power combiner using a cladding of 6 tubes surrounding one inner tube. / July 2022 / Completed.

(G2.1) Develop COMSOL models. / April 2022 / Completed.

(G2.2) Discover and optimize the length at which the cladding modes couple maximal power into the inner tube. / July 2022 / Completed.

(G3) Develop spectral combiners based on multiple-tube waveguides and compare to existing PCF (photonic crystal fiber) technologies. / August 2022 / Completed.

3.1.3 *Progress Made Since Last Report*

(E13) (E14) These two final tasks on the experiment had to be sunset because someone broke the dual clad Yb doped fiber amplifier (despite signs of “do not touch” and “expensive fragile fiber” other lab users clearly had moved things around). To repair the break we would need to purchase a fiber splicer (at 50K$) or hire a vendor to do the splice (at 3K$ plus a few months time).

(F2) Our research on high-power multiple tube power amplifiers of capillary-sized tubes [hundreds of microns] has run in parallel with the pursuit of a means of extending such techniques to horn antennas (and their feed waveguides) via larger sized tubes [ones of centimeters] at RF frequencies (e.g., 600 MHz – 6 GHz). We transfer our resonance findings and techniques into RF (specifically reconfigurable antenna design) and further their development within the context of how photonic crystals (an array of air holes) can enhance the performance of patch antennas [with structures on the scale of millimeters].

3.1.4 *Technical Results*

We model the antenna as a series R, L, C resonant circuit, so that the power dissipated in R will represent the power radiated by the antenna, by setting R equal to the radiation resistance. We consider a patch antenna for which we have R = 250 ohms, L = 1.326 nH, and C = 2.195 pF which is therefore resonant at 2.95 GHz. Note that a parallel R, L, C circuit would be inappropriate because we want larger R to represent increased loss – which diminishes the Q (i.e., increases the bandwidth) of the resonator: $Q = \omega_0 \tau,$ where the decay time constant is $\tau = L/R$ and the resonant frequency is $\omega_0 = 1/(2\,\pi\,\sqrt{LC})$.

The impedance on resonance is R, i.e., the antenna load becomes purely resistive so to match it to a 50-ohm source we can use a quarter-wave transformer (QWT). A QWT is a transmission-line (optically a layer) of length $d = \lambda/4$ and wave impedance of $Z_Q = \sqrt{Z_s Z_l}$ (where *s* and *l* refer to source and load so Z_Q is simply $\sqrt{50\ 250}$ = 111.8 ohms; and λ is the wavelength within that media so d = 7.545 mm). The match is perfect when on the LC resonance, which would result in a reflection coefficient, S11, of zero (thus, an infinite return-loss $RL \equiv 10\ Log_{10}(S_{11})$) at that resonant frequency of 2.95 GHz. To model a finite RL we detune the resonance of the QWT to 2 GHz by setting d = 11.1289 mm instead; and obtain the curves in Fig.3.1.1 for S11 and RL vs frequency. Note in passing, some define return-loss as -RL, others simply refer to the absolute value.

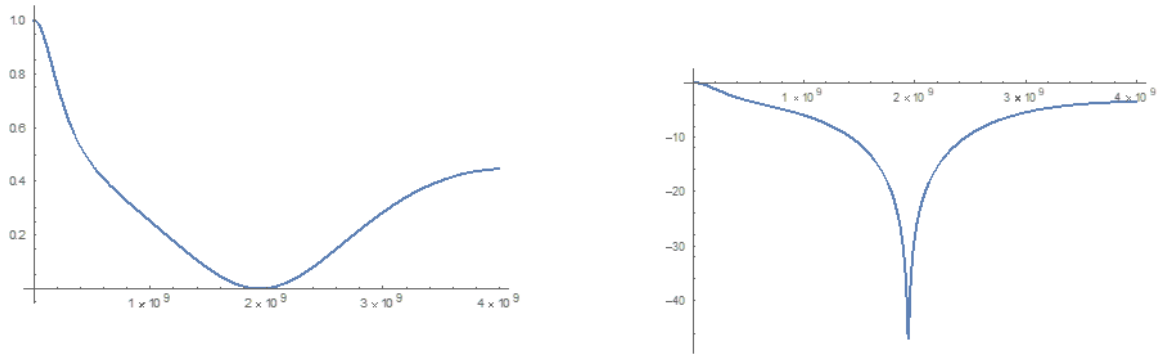


Fig. 3.1.1. Reflection coefficient (linear scale on left) and return-loss (log scale on right) of a patch antenna preceded by a QWT detuned to 2 GHz, as seen by a 50-ohm source.

We notice that the resonant frequency of the QWT dominates the system resulting in a RL of over 40 dB sharply peaked at 2 GHz. In Fig. 3.1.2 we show the same S11 over longer frequency ranges and observe how the initial (lower frequency) depth of the .4444 swing between envelopes (set because that is the reflection coefficient for 50 ohms connecting to 250 ohms) gets diminished at higher frequencies. This is because at higher frequencies the inductive reactance will dominate the antenna impedance, thus enforcing S11 → 1 (to which the QWT can only put "dents" in it).

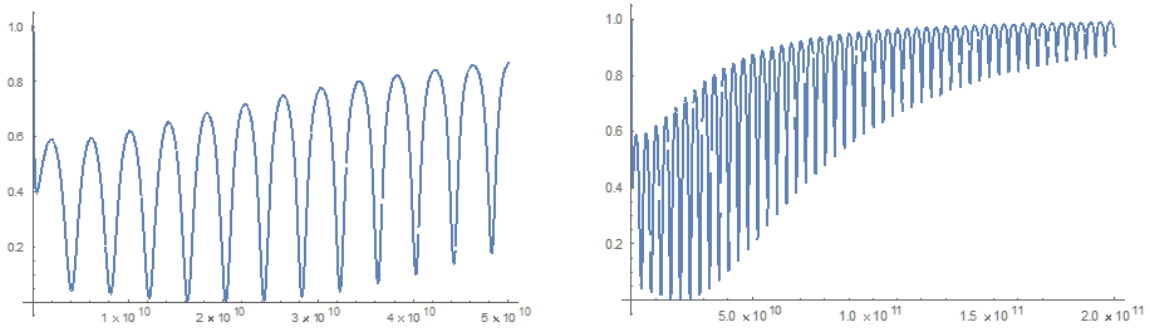


Fig. 3.1.2. Reflection coefficient of a patch antenna preceded by a QWT detuned to 2 GHz, as seen by a 50-ohm source, on a frequency range of 50 GHz (on left) and 200 GHz (on right).

To this antenna/QWT system we now add a section of transmission line of length = 2 R1 = 2mm and of impedance = 376.734 ohms (representing an air-hole of radius R1, drilled in a patch) followed by a section of transmission line of length D2 = 4mm and of relative dielectric constant, $\epsilon_r = 4.4$. A series of such transmission line pairs will later be taken as a one-dimensional approximation to a two-dimensional (photonic crystal) array of air holes (separated by a distance of D2) within a patch antenna. The relatively high resonance frequencies associated with the relatively small dimensions, 2 R1 and D2, are 37.5 GHz and 35.7548 GHz respectively – and hence out-of-band with respect to those near 2 or 3 GHz. But we borrow from knowledge recently gained (as in the MSR of AUG2022) on how out-of-band resonances can affect in-band resonances, in hopes of controlling lower frequency resonances without having to incorporate larger dimensions.

Fig.3.1.3 shows how the envelopes of Fig. 3.1.2 have been dramatically modified by the addition of only a single pair of such transmission lines. The previously monotonically increasing envelopes have been diminished and enhanced at a beat frequency of roughly 80 GHz.

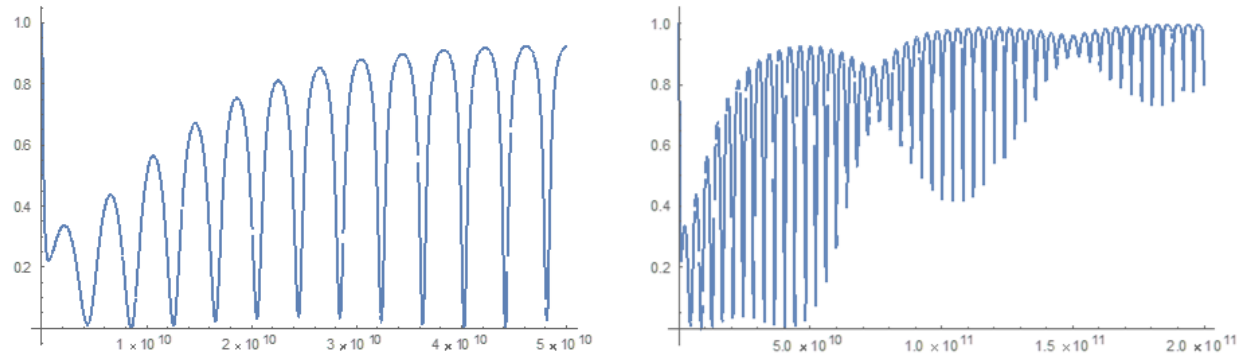


Fig. 3.1.3. Reflection coefficient of a patch antenna preceded by a QWT and a hole of index n=1, on a frequency range of 50 GHz (on left) and 200 GHz (on right).

Fig.3.1.4 shows the effect of replacing air in the patch hole with a material of refractive index n = 3. The rate at which the envelopes are diminished and enhanced has been reduced to a beat frequency of roughly 20 GHz.

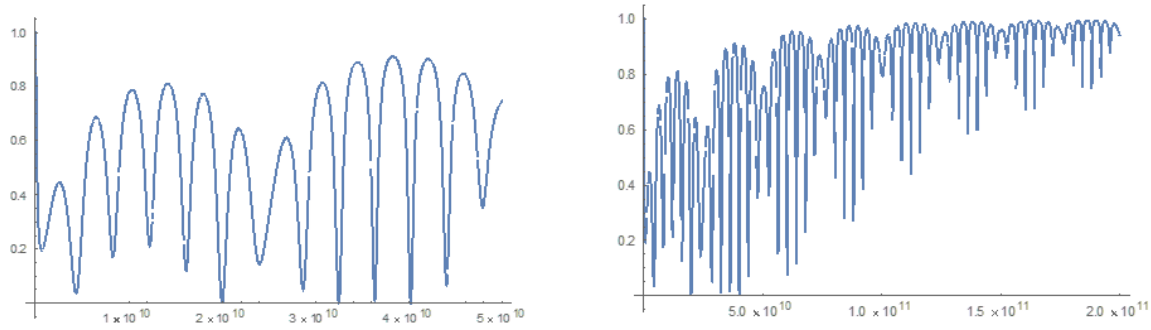


Fig. 3.1.4. Reflection coefficient of a patch antenna preceded by a QWT and a hole of index n=3, on a frequency range of 50 GHz (on left) and 200 GHz (on right).

To bring the out-of-band resonances to lower frequencies and thereby increase their influence at frequencies near 1 to 6 GHz, we can increase the R1 and D2 dimensions. We increase these by a factor of two in Fig. 3.1.5 which shows the difference in RL for an n=1 hole vs an n=3 hole. We observe that dramatically different in-band performance can be achieved.

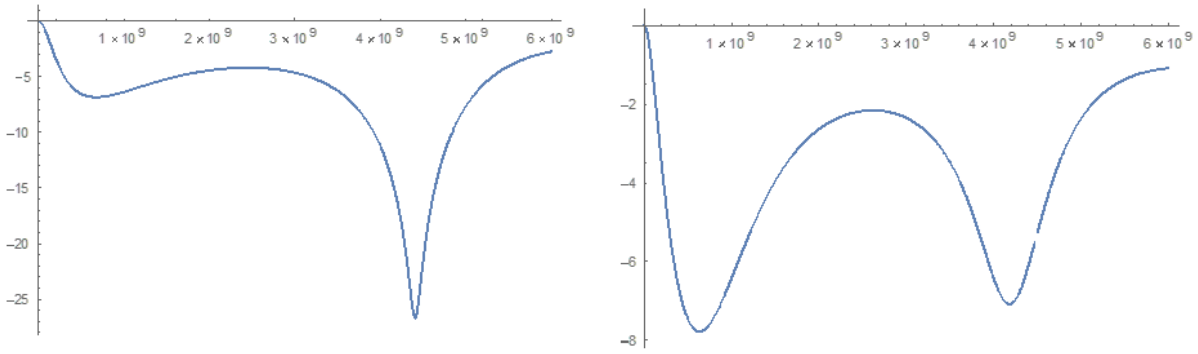


Fig. 3.1.5. RL on a frequency range of 6 GHz of a patch antenna preceded by a QWT and a hole of index n=1 (on left) and n=3 (on right).

3.1.5 *Summary of Significant Findings and Mission Impact*

(A) Our pre-burst optical pumping scheme simulations showed that we can drop the pump power costs by a factor of 40 with pre-burst ASE power levels below the heating level tolerance of 100 μW. UMKC invention disclosure filed 02JUN2020.

(B) For a proposed system gain of 8 million, a linear gain theory predicted the in-burst ASE would be over our heating level spec. by a factor of 3960, but by exploiting the nonlinearity of gain saturation we find that we can suppress the ASE by over 7000. UMKC invention disclosure filed 14SEP2020.

(C) Achieved initial practical device designs that exploit gain saturation, which remained below damage thresholds, via staged designs of different mode diameters NOV2020.

Hot spots, i.e., points of high peak-to-average ratio (PAR) of field strength, were discovered. These could lead to damage and thus they restrict the amplifier's operating power. We demonstrate that the locations of these hot spots are set by geometric factors (i.e., the *locations* are set via purely linear effects). The *size* of these PARs however are greatly enhanced by the fiber nonlinearity (from barely observable to factors of ten or more). Linear anti-reflective techniques are inapplicable, so we mitigated this nonlinear enhancement via the effects of gain saturation and obtained a reduction of the PAR by a factor of 10 FEB2022.

(D) Models of the impact of ASE on timing jitter in the presence of dispersion and/or nonlinearities were established JUL2020.

(E) The design of a proof-of-concept experiment demonstrating a cost-reduced optical pumping scheme was finalized MAR2021.

(F) We made (to our knowledge) the first observation of self-focusing effects that are not determined by beam power alone. We found instead that these can also be controlled via the geometric factors within a waveguide (such as fiber core diameter) MAY2021.

We additionally made (to our knowledge) the first observation that a mode exists in the air within a simple glass tube into which we can couple energy from the mode in the glass. Thus, an amplifier (in the doped and pumped glass) can operate at higher powers JUNE2021.

We found conditions under which 0.25 GW of power can exist in the tube's air-core mode when its glass-cladding mode is at a power level near 0.5 GW JULY2021.

Advancements in the very high-power operating point (tens of GW) of our tubular optical amplifier (and the existence, size and spatial uniformity of its air-core mode) were shown to permit a single laser to trigger an array of several (up to 100) Si-PCSS – reducing the laser system cost and eliminating the optical timing jitter constraint. The symmetry breaking of the scattering from self-focusing in a curved waveguide was shown to enable such AUG2021.

Complicated entrance optics for the tubular amplifiers greatly simplified by passively splitting (via e.g., a beam splitter such as a microscope slide) a single source into a finite number of "spots" (e.g., 1 or 2 or 4) to illuminate the wall of the tube. We found that with 4 spots of radial polarization we can still achieve GW core and 10 GW cladding power levels SEP2021.

We showed that one device can cover both DoD applications of HMP and HEL by simply changing the operating power point to adjust the output beam profile from almost uniform to almost Gaussian (respectively). UMKC signed NDAs with NKT. Meetings were held with NRL NOV2021.

Smaller core (~ 50 micron) tubular amplifiers enable mechanical flexibility (like a fiber) at diminished thermal capability, so we incorporated water-filled (rather than air-filled) designs capable of 1/10 GW core at 1 MW cladding power levels. We calculated SWaPC improvement examples for the use of a single optical power tube to drive an array of PCSS (relative to a normal free-space implementation of the laser system) finding a cost reduction factor (for a 100 element array) of 83 at reduction in size by a factor of 290. For a 12 element array these improvement factors are 21 and 35 DEC2021.

The use of lower index steam (instead of liquid water) and a staged design, in which the core of each stage also receives an input, increased the power levels by a factor of 10: to 1 GW in the core and 10 MW in the cladding (of these 50 micron core fibers) JAN2022.

(G) Power combiners are important components in high-power fiber laser systems and to that application we leverage our power tube technology; again using a 4 spot input (now with each spot coming from a different laser). We simulated four categories of input polarization and phasing combinations; and found that the "radial" case (each

spot in phase with radial directed polarization) maximizes power transfer into the core. The “phi polarized” case (in which the polarization of each spot is in the direction of increasing angle – tracing out a circle, i.e., to the right on top, down on right, left on bottom, and up on left); minimized power transfer into the core, while confining it primarily inside the cladding MAR2022.

Combiners comprised of 6 or 7 tubes lining the walls of an outer tube resulted in our best-yet Gaussian beam profiles (M2 < 1.13) by exploiting a new type of hollow-core resonance which ensues at operating power just beyond the breakpoint (and thus comes at a cost of a 3 dB reduction of cladding power) APR2022.

Spectral power combiners require broadband transmission windows. We developed an optical transmission design tool/graphic and applied it to our power combiner and passive power delivery design tasks. We show that the mechanical flexibility of fiber (in contrast to a rigid tube) comes with a high price in bandwidth and loss, e.g., if we wanted to guarantee over 90% transmission then a commercially available photonic crystal fiber cannot exceed about 2 [m] in length and the spectral bandwidth is limited to roughly 80 nm – a far cry below the 300 nm of bandwidth that a water-filled tube could provide at that same length MAY2022.

By extending the length of the waveguides in our simulations we have revealed new physics, including the surprising creation of high intensity surface waves at the air/glass interfaces. These strikingly narrow spikes or pencil beams could be exploited in Directed Energy systems due to their highly localized nature. These are special waves which “hug” the material interface (rather than reflect from it) as do so-called “creeping waves” which have been observed previously, but such require conductivity. To our knowledge this is the first prediction that something similar can happen at a non-conducting dielectric interface. Such effects must be readily transferrable to RF radiators as well because they exist even in the case of the absence of a Kerr nonlinearity. Metallic tubes could generate creeping waves at RF but surface waves from glass would improve the SWaP JUN2022.

We show that surface waves can be generated at RF by lining the walls of a copper rectangular waveguide with glass tubes and that the lengths required are compatible with the dimensions of a rectangular feed to a dual-ridge horn antenna. Such photonic crystal effects have enhanced the gain of patch antennas and we have opened the door to applying these transverse resonances to higher power antennas JUL2022.

We simultaneously analyze the impact of tubular resonators on RF horn antennas; while we also model optical power amplifier tubes enclosed in a metallic sheath. By transforming the wave impedance of the outer wall through the materials in the tube we characterize their impact on the overall mode. For an air-load (tube not touching metal) we find that the in-band resonances (at multiples of 1.875 GHz, arising from the radius of the tube) can be dramatically influenced by the out-of-band resonances (starting at 50 GHz, arising from the wall thickness of the tube). For a copper-load (tube touching the metallic wall) however, the out-of-band resonances have no impact. Having an analytic model provides a valuable design tool since the parameter space is too large for optimization via simulation alone AUG2022.

4 Photoconductive Switch Innovation

4.1 Characterizing and Optimizing On-State Resistance in GaN:X PCSS

(Heather Thompson)

A final summary report for this project was provided in the August 2022 MSR.

5 Drift-Step-Recovery-Diode-Based Source Alternatives

5.1 Drift-Step Recovery Diode and Pulse Shaping Device Optimization

(Jay Eifler)

5.1.1 *Problem Statement, Approach, and Context*

Primary Problem: Drift-step recovery diodes (DSRDs) and DSRD-based pulsed power systems are competitive with PCSS-based systems for HPM cUAS, with the benefit of not requiring a laser. Maximizing peak power while maintaining characteristic ns-order DSRD rise times requires optimization of the DSRD device design and pulser. Other considerations are for compactness, low-jitter, cooling required, and additional pulse-sharpening device within the pulse shaping head circuit. Additional goals for pulse repetition frequency are also to be satisfied for various applications.

Solution Space: By altering DSRD device parameters (geometry, doping, irradiation), optimize single-die and stack designs for peak power and risetime within various inductive pulser circuit topologies. Also optimize the pulse sharpening device (PSD) within the pulse shaping head circuit.

Sub-Problem 1: TCAD and SPICE models of the DSRD are inaccurate and must be improved. PSD models have not been developed.

Sub-Problem 2: Inductive pulser designs are complicated by the DSRD (and PSD) parameter variability. Use TCAD and/or SPICE models to account for variability and improve pulser design.

State-of-the-Art (SOTA): MW peak power and ns-order risetimes have been achieved in DSRD-based pulsed-power systems employing DSRD stacks for higher voltage holding and parallel lines of DSRD to increase current. PSD have sharpened DSRD pulses to 100 ps-order.

Deficiency in the SOTA: A lack of accurate TCAD and SPICE models make design of DSRD and DSRD-based inductive pulser circuit topologies (with or without PSDs) difficult to the level of tens of MW of peak power while maintaining ns-order risetime (or sharpened 100 ps-order). In addition, DSRD (and PSD) fabrication variabilities further complicate pulser design.

Solution Proposed: Develop further modeling capabilities in TCAD and SPICE for DSRD and DSRD-based inductive pulser circuit topologies to optimize DSRD and inductive pulser designs, especially for maximum peak power and minimum risetime, but also for low-jitter, reduced cooling, and compactness. Additionally, optimize pulser with PSD and pulse shaping head circuit.

Relevance to OSPRES Grant Objective: DSRD-based systems eliminate laser requirements necessary for PCSSs and are competitive in terms of thermal requirements and peak power. With sharpening, the DSRD-based systems can produce comparable risetimes. The SWaPC^2 cooling requirements of HPM cUAS systems can be solved with DSRD-based pulsed power systems, and low-jitter DSRD-based systems can be used for beam-steering in phased-arrays.

Risks, Payoffs, and Challenges: DSRD must be arrayed and staged to increase current since DSRD are limited in their ability to operate at high current densities. DSRD and PSD must also be stacked to operate at high voltages necessary for high peak power and maintain low risetimes. The stacking methods can damage dies and produce variable results in risetime and DSRD diffused doping profiles can be difficult to achieve and may require epitaxial methods. SPICE device models for DSRD are unavailable and must be developed, and questions remain about TCAD limitations for DSRD and PSD modeling.

5.1.2 Tasks and Milestones / Timeline / Status

(A) Milestone – Develop DSRD SPICE model within SmartSpice using the CMC diode model (built-in and Verilog-A) based on 6485 forward IV data.

1. Task – Develop accurate forward IV, reverse CV and reverse recovery testing (RRT) modeling in CMC diode model using either built-in (faster) or Verilog-A (customizable) models; Completed [APR-JUN 2022];

2. Task – Develop reverse IV and forward CV modeling and parameters in SmartSpice CMC diode models (built-in and/or Verilog-A); Discontinued [MAY-JUL 2022];

3. Task – Develop 1x1 DSRD-based pulser recovery parameters within CMC diode model of SmartSpice (built-in or Verilog-A) and compare to RRT parameters; Transitioning [APR-JUL 2022];

(B) Milestone – Complete LTSPICE parameterization of the standard diode model for DSRD inventory.

1. Task – Finish Gen2.2 DSRD LTSPICE parameter extraction; Completed [APR-MAY 2022];

(C) Milestone – Develop automated fitting procedures for developed LTSPICE and/or SmartSpice DSRD models.

1. Task – Improve speed/accuracy/size of brute force fitting methods for LTSPICE and SmartSpice diode models; Completed [APR-JUN 2022];

2. Task – Improve python-based fitting methods for diode models used in LTSPICE and/or SmartSpice; Discontinued [APR-JUN 2022];

3. Task – Improve use of SmartSpice Optimizer for parameter fitting of diode models; Discontinued [APR-JUN 2022];

4. Task – Develop automated fitting procedures for Verilog-A diode models (CMC or custom); Completed [APR-AUG 2022];

(D) Milestone – Convert manufacturer PSPICE and PSPICE/LTSPICE unencrypted device models into SmartSpice format for use in DSRD-based pulser simulation.

1. Task – Convert unencrypted PSPICE/LTSPICE Cree MOSFET model into SmartSpice format; Completed [APR-JUN 2022];

2. Task – Convert unencrypted Texas Instruments Gate Driver model from PSPICE into SmartSpice format; Completed [APR-JUN 2022];

(E) Milestone – Develop DSRD parameters for 2450 and new 371 semiconductor analyzer measurement data (forward IV and reverse IV).

1. Task – Develop standard diode LTSPICE 371A semiconductor analyzer measurement data parameters; Completed [APR-JUN 2022];

2. Task – Develop SmartSpice CMC (Verilog-A) 371A semiconductor analyzer measurement data parameters; Transitioning [APR-JUN 2022];

(F) Milestone – Determine performance of doping profiles within TCAD

1. Task – Determine TCAD performance of SOS, dynistor and thyristor doping profiles; Discontinued; [?-? 2022];

2. Task – Determine TCAD performance of square root DSRD doping profiles; Discontinued [JUN 2022];

3. Task – Determine TCAD performance of Gen3 manufacturer doping profiles; Discontinued [JUL 2022];

4. Task – Determine recovery behavior of DSRD doping profiles within TCAD for development of custom Verilog-A CMC-based DSRD models; Transitioning [JUL-OCT 2022];

5. Task – Determine effect of doping and defects on DSRD forward IV performance; Discontinued [AUG-OCT 2022].

5.1.3 *Progress Made Since Last Report*

(E) LTspice Parameter Fitting for 2450/371 Forward IV

The LTspice standard diode model parameters have been fit for the DSRD inventory based on the combined 2450/371 forward IV data. The fitting includes forward IV, reverse CV and reverse recovery testing (RRT). The parameter data has been passed along to the DSRD pulser design team (see Section 5.4).

5.1.4 *Technical Results*

(E) LTspice Parameter Fitting for 2450/371 Forward IV, CV and RRT

The design and optimization of the DSRD-based pulser module relies on accurate experimental characterization measurements (Section 5.3) and device model parameters based on the measurements. LTspice has been used for pulser design and optimization (Section 5.4) and uses the standard Berkeley diode model available in LTspice and almost all circuit simulators, therefore DSRD parameters have been developed and fit for LTspice. Eight tables (Tables 5.1.1-8) are included here which are nearly complete (completed tables will be included in the OSPRES final report) for both the key performance indicators (KPI) derived from the experimental characterization measurements (included here as, opposed to Section 5.3, for convenience of viewing

both sets of tables) and LTspice parameters for the standard diode model (as opposed to SmartSpice CMC diode model).

Table 5.1.1. EG1500 DSRD characterization measurement key performance indicators.

Diode	Forward Voltage Drop at 50 A (V)	On-State Resistance (Ω)	Breakdown Voltage (V)	Reverse Current At 200 V (µA)	Zero-Bias Junction Capacitance (pF)	Reverse Capacitance At 35 V (pF)	Maximum Forward Capacitance (pF)	Maximum Forward Capacitance Voltage (V)
*EG1562					650.07	380.62	15610.83	3.43
EG1563	18.95	0.089	3100	0.86	643.34	311.43	12468.72	3.65
EG1564	19.00	0.093	2843	1.04	637.78	323.50	53549.35	5.00
EG1565	22.60	0.125	1553	0.48	635.92	337.35	4640.91	2.98
EG1566	16.78	0.126	716	1.32	645.94	333.54	9686.39	3.43
EG1567	18.33	0.106		0.76	638.49	361.70	2682.24	2.98
EG1568	14.73	0.082		0.51	640.72	322.91	9769.77	3.43
EG1569	21.78	0.117		0.94	647.95	356.07	3986.10	2.98
EG1570	19.17	0.096		4.25	668.21	319.63	3883.47	3.20
EG1571	20.10	0.150	2172	1.01	642.01	309.29	10778.68	3.20
EG1572	16.75	0.088	3100	0.78	641.28	314.96	39529.54	4.10
EG1573	15.38	0.090	3100	1.73	637.10	334.63	11199.25	3.43
EG1574	18.58	0.109		0.53	641.20	311.04	34970.94	4.10

*broken

Table 5.1.2. EG1500 DSRD LTspice standard diode model parameters.

Diode	IS (A)	N	IKF (A)	RS (Ω)	Error-2450 (A)	Error-371 (A)	CJO (pF)	M	Error-Cap (F)	Transit Time (s)	Error-RRT (s)
*EG1562											
EG1563	1.7E-07	1.6	0.037	0.04	3.72E-03	6.08	4503.40	0.36	5.06E-12	3.90E-06	3.10E-07
EG1564	1.5E-07	1.6	0.037	0.04	5.08E-03	6.32	4464.44	0.34	5.30E-12	6.90E-06	3.37E-07
EG1565	1.3E-07	1.6	0.037	0.09	5.64E-03	6.53	4451.41	0.30	5.02E-12	5.60E-06	1.19E-07
EG1566	3.0E-10	1.1	0.031	0.03	3.46E-03	3.86	4521.57	0.31	6.01E-12	6.80E-06	1.12E-07
EG1567	1.1E-07	1.6	0.028	0.03	3.83E-03	5.01	4469.43	0.28	7.71E-12	7.20E-06	1.41E-07
EG1568	3.0E-10	1.1	0.019	0.02	6.52E-03	4.40	4485.05	0.34	9.60E-12	5.80E-06	8.77E-08
EG1569	9.0E-08	1.6	0.037	0.10	4.15E-03	7.93	4535.68	0.28	8.35E-12	5.90E-06	8.80E-08
EG1570	1.9E-07	1.7	0.037	0.05	3.51E-03	6.92	4677.48	0.37	8.35E-12	5.60E-06	7.56E-08
EG1571	5.0E-09	1.3	0.040	0.04	1.58E-03	3.86	4494.08	0.36	5.15E-12	8.60E-06	9.28E-08
EG1572	5.0E-09	1.3	0.031	0.03	2.04E-03	4.65	4488.95	0.35	7.46E-12	7.30E-06	1.39E-07
EG1573	3.0E-10	1.1	0.016	0.03	2.28E-03	5.34	4459.72	0.32	4.62E-12	6.40E-06	7.75E-08
EG1574	5.0E-09	1.3	0.025	0.04	2.30E-03	4.52	4488.41	0.36	4.43E-12	8.30E-06	1.73E-07

*broken

Table 5.1.3. EG1600 DSRD characterization measurement key performance indicators.

Diode	Forward Voltage Drop at 50 A (V)	On-State Resistance (Ω)	Breakdown Voltage (V)	Reverse Current At 200 V (μA)	Zero-Bias Junction Capacitance (pF)	Reverse Capacitance at 35 V (pF)	Maximum Forward Capacitance (pF)	Maximum Forward Capacitance Voltage (V)
*EG1601			2900	0.83	644.93	309.41	5807.58	3.20
EG1602	0.10	17.45	759	4.96	908.25	409.12	5114.83	2.08
EG1603	0.10	19.43	2043	7.43	637.51	273.21	5772.84	3.20
EG1604	0.11	16.55	687	16.31	816.93	337.08	4573.45	3.20
EG1605	0.21	23.20	2335	1.46	645.07	300.25	5927.26	3.20
EG1606	0.09	15.15	1202	3.38	622.69	266.80	4906.40	2.98
EG1607	0.12	19.72	2930	0.54	645.68	279.60	5670.35	3.20
EG1608	0.12	20.60	1454	2.26	644.12	284.38	5197.58	3.20
EG1609	0.16	17.93	3100	0.76	644.75	323.90	5648.64	3.20
EG1610	0.09	18.87	2551	3.23	640.05	332.37	5660.95	3.20
EG1611	0.11	16.78	2600	1.31	635.25	286.64	4974.92	3.20
EG1612	0.10	19.35	2005	4.51	622.33	265.68	5837.07	3.20
EG1613	0.12	16.40	3100	0.78	642.75	292.28	5649.65	2.98
EG1614	0.12	21.60	1280	8.45	660.93	338.35	5844.48	3.43

*broken

Table 5.1.4. EG1600 DSRD LTspice standard diode model parameters.

Diode	IS (A)	N	IKF (A)	RS (Ω)	Error-2450 (A)	Error-371 (A)	CJO (pF)	M	Error-Cap (F)	Transit Time (s)	Error-RRT (s)
*EG1601											
EG1602	9.0E-08	1.1	0.034	0.04	3.57E-03	6.57	6357.74	0.41	2.00E-11	3.40E-06	5.34E-07
EG1603	1.9E-07	1.7	0.028	0.08	5.72E-03	11.71	4462.55	0.43	7.97E-12	6.50E-06	2.23E-07
EG1604	3.0E-09	1.0	0.013	0.03	3.74E-03	4.41	5718.52	0.45	1.37E-11	5.20E-06	3.34E-07
EG1605	3.0E-09	1.2	0.019	0.05	1.74E-03	3.04	4515.52	0.38	8.08E-12	6.70E-06	2.49E-07
EG1606	1.0E-10	1.0	0.007	0.02	5.94E-03	6.15	4358.83	0.43	7.36E-12	6.30E-06	2.73E-07
EG1607	5.0E-08	1.5	0.037	0.04	3.14E-03	4.43	4519.76	0.42	7.10E-12	9.00E-06	2.33E-07
EG1608	1.5E-07	1.6	0.040	0.04	3.19E-03	4.98	4508.81	0.41	8.77E-12	4.20E-06	3.81E-07
EG1609	1.0E-10	1.0	0.013	0.03	6.80E-03	3.58	4513.26	0.34	2.08E-12	6.80E-06	2.13E-07
EG1610	1.9E-07	1.7	0.028	0.06	6.18E-03	9.96	4480.35	0.32	4.16E-12	3.90E-06	4.01E-07
EG1611	1.0E-10	1.0	0.013	0.03	4.31E-03	3.45	4446.75	0.40	8.98E-12	4.60E-06	3.16E-07
EG1612	1.1E-07	1.6	0.037	0.05	3.62E-03	7.20	4356.32	0.43	7.45E-12	3.60E-06	4.24E-07
EG1613	5.0E-08	1.5	0.028	0.03	3.45E-03	5.31	4499.23	0.40	8.34E-12	5.40E-06	5.09E-07
EG1614	1.5E-07	1.6	0.022	0.10	4.14E-03	9.03	4626.53	0.33	5.86E-12	3.60E-06	4.87E-07

*broken

Table 5.1.5. Gen2.1 DSRD characterization measurement key performance indicators.

Diode	Forward Voltage Drop At 50 A (V)	On-State Resistance (Ω)	Breakdown Voltage (V)	Average Reverse Current At 200 V (μA)	Zero-Bias Junction Capacitance (pF)	Reverse Capacitance At 10 V (pF)	Maximum Forward Capacitance (pF)	Maximum Forward Capacitance Voltage (V)
*gen2.1-d1-1			222	151.65	1254.79	551.82	1509.39	0.2
*gen2.1-d1-2				544.43	1603.10	574.41	11455.49	0.4
gen2.1-d1-3	1.77	0.017	501	180.57	1473.05	560.70	2816.24	0.3
*gen2.1-d1-4			290	433.97	1363.13	555.61	2457.19	0.3
gen2.1-d2-1	1.48	0.012	286	251.13				
gen2.1-d2-2	1.35	0.009	392	13.31	1639.92	573.38	6733.56	0.4
gen2.1-d2-3	1.29	0.009	222	18.84	1599.31	567.65	13442.30	0.4
*gen2.1-d2-4			410	6.44	1613.30	560.98	13952.90	0.4
gen2.1-d3-1	1.25	0.008	490	63.00	1426.36	561.56	5311.02	0.4
*gen2.1-d3-2			406	31.07	1615.77	573.13	12790.80	0.4
gen2.1-d3-3	2.10	0.023	222	818.87				
gen2.1-d3-4	2.17	0.024	575	4.69				
gen2.1-d4-1	2.50	0.031	590	6.00				
gen2.1-d4-2	1.27	0.008	567	294.45	1470.40	564.62	2707.21	0.3
gen2.1-d4-3	1.32	0.009	222	620.19				
gen2.1-d4-4	2.04	0.021	293	2000.75				
gen2.1-d5-1	1.69	0.015	210	3324.74				
gen2.1-d5-2	1.21	0.007	366	44.00	1646.70	570.99	7296.07	0.4
gen2.1-d5-3	1.41	0.011	440		1554.31	569.14	4502.31	0.3
gen2.1-x-1	1.23	0.007	585					
gen2.1-x-2	1.48	0.011	190					
gen2.1-x-3	1.41	0.009	571					

*broken

Table 5.1.6. Gen2.1 DSRD LTspice standard diode model parameters.

Diode	IS (A)	N	IKF (A)	RS (Ω)	Error-2450 (A)	Error-371 (A)	CJO (pF)	M	Error-Cap (F)	Transit Time (s)	Error-RRT (s)
*gen2.1-d1-1											
*gen2.1-d1-2											
gen2.1-d1-3	3.0E-11	1.0	0.019	0.0160	7.35E-03	0.176	1441.59	0.38	3.76E-11	8.90E-06	3.57E-07
*gen2.1-d1-4											
gen2.1-d2-1	1.0E-12	0.9	0.022	0.0113	2.90E-03	0.579					
gen2.1-d2-2	7.0E-13	0.9	0.040	0.0088	3.45E-03	0.298	1596.27	0.42	4.60E-11	9.50E-06	5.62E-07
gen2.1-d2-3	1.0E-13	0.8	0.010	0.0082	3.78E-03	0.754	1555.45	0.41	4.53E-11	9.60E-06	3.80E-07
*gen2.1-d2-4											
gen2.1-d3-1	1.0E-13	0.8	0.010	0.0074	2.82E-03	0.590	1397.90	0.37	3.54E-11	9.50E-06	4.04E-07
*gen2.1-d3-2											
gen2.1-d3-3	1.0E-12	0.9	0.034	0.0235	5.58E-03	0.962					
gen2.1-d3-4	1.0E-12	0.9	0.031	0.0244	4.89E-03	2.138					
gen2.1-d4-1	1.0E-12	0.9	0.034	0.0310	5.53E-03	0.980					
gen2.1-d4-2	1.0E-13	0.8	0.010	0.0078	4.18E-03	0.517	1448.14	0.38	3.98E-11	7.80E-06	6.42E-07
gen2.1-d4-3	1.0E-13	0.8	0.010	0.0087	3.12E-03	0.626					
gen2.1-d4-4	1.0E-12	0.9	0.037	0.0208	4.43E-03	2.478					
gen2.1-d5-1	1.0E-12	0.9	0.025	0.0151	1.99E-03	0.925					
gen2.1-d5-2	1.0E-13	0.8	0.010	0.0066	3.96E-03	0.490	1603.55	0.42	4.60E-11	1.09E-05	3.12E-07
gen2.1-d5-3	1.0E-13	0.8	0.010	0.0103	3.26E-03	0.987	1513.54	0.40	4.36E-11	9.60E-06	3.13E-07
gen2.1-x-1	1.0E-12	0.9	0.037	0.0065	5.05E-03	0.670					
gen2.1-x-2	7.0E-13	0.9	0.025	0.0111	1.70E-03	0.759					
gen2.1-x-3	1.0E-11	1.0	0.040	0.0093	4.60E-03	0.723					

*broken

Table 5.1.7. Gen2.2 DSRD characterization measurement key performance indicators.

Diode	Forward Voltage Drop At 50 A (V)	On-State Resistance (Ω)	Breakdown Voltage (V)	Reverse Current At 200 V (μA)	Zero-Bias Junction Capacitance (pF)	Reverse Capacitance At 10 V (pF)	Maximum Forward Capacitance (pF)	Maximum Forward Capacitance Voltage (V)
gen2.2-d1	1.21	0.008	108.50	20348.44	1425.50	542.54	4434.20	0.34
gen2.2-d2	1.21	0.009	61.25	4293.42	1348.92	550.84	2116.79	0.29
gen2.2-d3	1.24	0.009	137.75	0.00	1431.42	527.27	4123.29	0.34
gen2.2-d4	1.44	0.015	147.00	1462.64	1478.53	556.70	4505.37	0.34
gen2.2-d5	1.26	0.010	125.50	17473.26	70.46	70.43	70.47	0.50
gen2.2-d6	1.52	0.020	147.00	0.00	1448.09	552.66	3946.40	0.29
gen2.2-d7	1.24	0.009	58.50	0.00	1404.60	554.25	2765.78	0.29
gen2.2-d8	1.22	0.009	233.00	0.00	104.03	96.38	108.51	0.50
gen2.2-d9	1.33	0.011	347.00	84.16	1446.94	555.83	3469.84	0.29
gen2.2-d10	1.24	0.009	345.00	0.00	1314.32	548.68	1829.67	0.24
*gen2.2-d11				4.88	120.84	120.58	120.85	0.45
gen2.2-d12	1.20	0.008	395.00	126.71	1485.72	558.86	8211.75	0.34
gen2.2-d13	1.26	0.009	552.00	5.28	81.73	81.68	81.74	0.45
*gen2.2-d14				15.85	1044.36	533.65	1088.24	0.19

*missing

Table 5.1.8. Gen2.2 DSRD LTspice standard diode model parameters.

Diode	IS (A)	N	IKF (A)	RS (Ω)	Error-2450 (A)	Error-371 (A)	CJO (pF)	M	Error-Cap (F)	Transit Time (s)	Error-RRT (s)
gen2.2-d1	1.0E-13	0.8	0.010	0.0068	2.94E-03	1.0447	1425.50	0.39	4.07E-11	8.9E-06	3.32E-07
gen2.2-d2	1.0E-13	0.8	0.010	0.0066	2.66E-03	0.6931	1348.92	0.36	3.32E-11	9.4E-06	2.92E-07
gen2.2-d3	1.0E-13	0.8	0.013	0.0073	2.42E-03	0.9060	1431.42	0.41	4.12E-11		
gen2.2-d4	1.0E-13	0.8	0.007	0.0109	5.17E-03	0.9180	1478.53	0.40	4.24E-11		
gen2.2-d5	1.0E-13	0.8	0.010	0.0078	3.02E-03	1.3739					
gen2.2-d6	1.0E-12	0.9	0.037	0.0128	3.85E-03	0.6231	1448.09	0.39	4.12E-11		
gen2.2-d7	1.0E-13	0.8	0.010	0.0073	2.54E-03	0.7490	1404.60	0.38	3.75E-11		
gen2.2-d8	1.0E-12	0.9	0.040	0.0065	5.12E-03	0.4674					
gen2.2-d9	7.0E-13	0.9	0.040	0.0084	3.61E-03	0.9218	1446.94	0.39	4.02E-11		
gen2.2-d10	1.0E-13	0.8	0.007	0.0070	6.25E-03	0.6198	1314.43				
*gen2.2-d11											
gen2.2-d12							1485.72				
gen2.2-d13											
*gen2.2-d14											

*missing

Now the data in the tables will be explained to gather together in one place this understanding. The forward voltage drop at 50 A is a metric used to assess the conductivity of the DSRD (along with the on-state resistance) used for power diodes at rated current usually 50 A. The on-state resistance can be measured when a power diode, such as the DSRD, goes nearly linear in the forward IV (indicative of a constant resistance). So, these two metrics then are extracted from the forward IV curves. The conductivity (or conversely the resistivity) of the DSRD will limit the peak voltage that can be obtained and effects the pulse risetime, falltime and consequently pulsewidth and voltage riserate but if not the major determiner of these effects (the snap-off or transition

time is the major determiner). The on-state resistance is synonymous with the standard diode parameter RS which is a series resistance in the equivalent circuit of the model. The on-state resistance should represent the near minimum on-state resistance and effects the peak voltage, risetime, etc. just as in experiment.

Several standard diode parameters are fit to the forward IV curves. These are saturation current (IS), ideality factor or emission coefficient (N), high-level injection knee current (IKF) and the series resistance (RS). Together they allow a close fit to the forward IV but are not always sufficient to fit very closely (as the the EG-series) due to sub-level injection.

The breakdown voltage is the static breakdown (as opposed to breakdown effects in the pulser), as is typically used, and is assessed at 1 mA of reverse current. The measurement was performed in the Tektronik 371 which uses a sine squared rectified source to reduce heating effects (in some cases when breakdown is below 200 V this measurement has also been confirmed using reverse IV testing in the Keithley 6485 pcioammeter at 1 mA reverse current and is a DC test). The static breakdown voltage test is used to estimate the peak voltage that can be obtained in the DSRD pulser and must be based ultimately on experience and measurement of breakdown effects in the pulser. The breakdown voltage is a standard diode parameter (BV) and limits the peak voltage in circuit simulation.

The reverse current at 200 V is a KPI and is derived from the reverse IV obtained using the Keithley 6485 picoammeter. The reverse current is used to assess the quality of a diode (such as the DSRD) and is related to the heat generated in reverse-biasing (also depends on the thermal environment). The reverse IV KPI is not used in the standard diode model but can be included in other diode models but with an increased difficulty of fitting the forward IV due to the number of parameters to fit together.

The zero-bias junction capacitance (ZBJC) is a KPI derived from the CV curves and is indicative of the overall capacitance level of the curve as a single metric. The capacitance is often referred to as being lower for faster switching in diodes but mostly relates to how fast or slow the capacitance of the diode can be charged or discharged, while the snap-off time is the important characteristic of the DSRD fast circuit breaking effect. The ZBJC is similar to the standard diode CJO parameter and can usually be substituted directly for it (also depends on the forward IV and the transit time).

The reverse capacitance (at 35 V or 10 V) is a KPI that is a better measure of the capacitance at higher voltages than the ZBJC. Sometimes the ZBJC serves to differentiate CV curves at higher voltages but curves can cross and therefore the ZBJC is not necessarily indicative of the capacitance at higher (or high) voltages and the effects on switching speed at high voltage. The reverse capacitance at higher voltage is not directly used to fit the standard diode model to the CV data but can be thought of as related to the M parameter (grading coefficient) within the common textbook CV equation used in the standard model.

The maximum forward capacitance is a KPI derived from the forward biased part of the CV curve or forward CV and occurs at the maximum forward capacitance voltage which is then another KPI. It is desirable to not operate at voltages with the higher capacitance of the maximum forward capacitance. Due to the unreliability of forward CV

measurements (that is when the phase begins to deviate from the 90° lag of a capacitor significantly) it has not been used but has been gathered for later assessment and improved measurements. The experimental forward CV has had higher measurement variability likely indicative of the unreliable measurement as the conductance of the DSRD increases at higher forward bias. The forward CV can be fit in the standard diode model but this is co-opted for the recovery model as is the standard engineering practice.

The reverse recovery testing (RRT) data has not been included in the KPI tables. A number of RRT were performed (up to 14 separate measurements) at various forward and reverse bias and pulse durations. The RRT provide measurements of the recovery time which decomposes into the charge storage time and the transition time (snap-off time). However, the AVTECH pulser used can only accurately measure the charge storage time (as well as cannot forward and reverse pump the DSRD at the high voltages of the pulser). The standard diode model itself only accurately models the charge storage time of the DSRD as well with little control over the snap-off or transition time. Again, the transit time (TT) of the forward CV model, within the standard diode model, is co-opted from modeling forward CV for modeling the recovery behavior of the DSRD with RRT and the pulser simulations. The TT then is fit as a single metric capable of accurately modeling the several RRTs measured and provides an experimental basis for setting the TT parameter for use in matching experimental pulser data to the SPICE simulations. The TT may have to be adjusted to match the peak voltage of the pulser experiments over its range of prime voltages and trigger durations used in testing, while the risetime is not captured well within the standard diode model due to the forward CV TT being used to model the charge storage effects (the SmartSpice CMC Verilog-A industry-standard diode model is being used to capture risetime as it includes a diode recovery model).

Also included in the parameter tables are the fitting errors for forward IV, reverse CV and RRT. The forward IV and reverse CV errors are the average absolute deviation. The RRT error is the total time difference in charge storage time between experimental and simulated curves (note different numbers of RRT have sometimes been used due to the data collected but this is not included here due to the amount of data). The fits of the curves are estimated visually as well and through experience the error values of good fits can be obtained.

The stack height or number of diodes in series of the DSRD differ with the EG-series having 7 diodes pressed together for increased voltage hold-off while the Gen2 are single diodes with no stacking. As well, the area of the EG-series is 1.33cm^2 and the Gen2 1 cm^2. The stack height must be normalized for voltage and the area normalized for current to make comparisons which is not shown here.

Some DSRD are marked as broken or lost and have not had all measurements performed and therefore parameter fitting performed. In some cases, the breakdown voltage has not been assessed due to the breakdown fixture having to be replaced properly yet for higher voltages. Also, some CV are not present due to the quality of the metallization of the contacts giving high CV measurement variability.

With the KPI, DSRD diodes have been previously successfully selected for improved peak voltage in the DSRD pulsers. With the model parameters, DSRD pulsers have been successfully designed for improved peak voltage. With this new complete set of KPI and

model parameters design and performance can be improved for the DSRD pulsers for higher peak voltages.

5.1.5 *Summary of Significant Findings and Mission Impact*

(A) Development of DSRD Model Within SmartSpice CMC Diode Model

The SmartSpice circuit simulation software was received in JAN 2022 and in FEB 2022 the Verilog-A CMC diode code was retrievable from the Si2 organization website. Development immediately began of the CMC diode model for DSRD modeling by producing forward IV, reverse CV and reverse recovery testing simulations and fitting to example DSRD in the inventory. Recovery parameter fitting within the 1x1 DSRD-based pulser was also begun. The capability of the CMC diode model for modeling DSRD can now be assessed. Any deficiencies in the CMC-DSRD model can be improved using the programmable Verilog-A code of the CMC diode model to include DSRD specific modeling equations based on theory, TCAD simulation, experiment and the literature. The Verilog-A code has been modified to allow different fitting parameters for different sections of the curve so that real, experimental, non-standard forward IV can be accurately fit. Improved forward IV fitting in the Verilog-A CMC diode model will allow for improved pulser simulation. A new SmartSpice CMC Verilog-A diode model has been developed for modeling silicon avalanche shapers (SAS) that adds voltage collapse to the diode model.

(B) LTSPICE Standard Diode Model Parameter Development for DSRD Inventory

DSRD in the inventory of received diodes (legacy, EG and Gen2) have been fit for LTSPICE standard diode model parameters (for forward IV, reverse CV and reverse recovery testing) for use in LTSPICE DSRD-based pulser simulations and to provide another metric for the characterization of the DSRDs in comparison to pulser performance. Some details of the very low voltage and current forward IV have not been fit but the fitting is still very close when visually inspected in non-log format. Reverse IV have not been fit in the standard diode model since it cannot capture the behavior. Breakdown has been measured and included within the standard diode model. Forward CV measurement are problematic and not fit mostly since the forward CV parameters in the standard diode model are used for recovery modeling. Various methods exist in LTSPICE to improve recovery parameter fitting but are either inadequate (Vp or carrier viscosity) or non-realistic (adjustment of reverse CV parameters) but have produced fits within 10% error for DSRD-based pulser performance.

(C) Develop Automated Fitting Procedures for LTSPICE and SmartSpice

The current best method of fitting is using a brute force method of running LTSPICE or SmartSpice simulations sweeping over the desired parameter space. The brute force method can produce the most accurate fits but requires long simulation times and cannot be used to explore large parameter spaces easily (which is why more physically-based models using only measurable parameters are desirable). There is ultimately a limit to how quickly and accurately one can develop parameter sets. Another method is to program in the model equations into Python and use their curve fitting tools, however this method cannot incorporate circuit simulation and will therefore be less effective in

producing accurate fits but is much faster in simulation time (can depend on how much parameter adjustments affect DSRD-based pulser performance on which method to use). The other fitting method is to use the built-in optimizer within SmartSpice, but the optimizer has not produced as good of fits consistently as the brute force method and will take some experience in using well.

(D) Conversion to SmartSpice of Manufacturer Device Models

Unfortunately, manufacturer device models are not openly available in SmartSpice only PSPICE and to some extent LTSPICE (usually converted from PSPICE). Therefore, the available PSPICE and PSPICE/LTSPICE models must be converted to the SmartSpice format, otherwise keeping the model the same. Note that encrypted models cannot be converted into SmartSpice, such models either have to be developed from scratch and either the datasheet or additional experimental tests used (or purchased from Silvaco for SmartSpice if available).

The unencrypted Cree MOSFET model has been converted into SmartSpice and tested within 1x1 DSRD-based pulser simulations and compared to LTSPICE simulations successfully. The unencrypted Texas Instruments gate driver model has also been converted into SmartSpice successfully. One issue with the driver model is it is intended for PSPICE but used often LTspice as reported in online discussions. However, close examination of the model shows that the model cannot perform correctly in all pin conditions in LTSPICE due to incorrect parameter types used in a voltage-controlled switch within the driver model. The voltage-controlled switch has been correctly implemented in the SmartSpice conversion and can be fixed for the LTSPICE version (Texas Instruments has not responded to inquires). Neither the MOSFET or gate driver models have been extensively diagnostically tested and compared to the datasheets which are often somewhat different from the free provided models (only so accurate).

The United MOSFET model (UF3SC120009K4S) had to be converted from PSPICE format to SmartSpice format. A couple model issues for the use of the model in LTspice were corrected, one which caused the model to not match the datasheet. The conversion to SmartSpice was successful and allowed simulation of the latest DSRD pulser circuit design with new MOSFETs using the CMC DSRD model to be performed successfully.

(E) IV Parameter Development for 371A Semiconductor Analyzer Measurement Data

A Tektronik 371 semiconductor analyzer has been acquired and setup for forward IV testing with the potential for higher voltage/current reverse IV testing and breakdown. Initially concerns arose about the shape of the EG-series forward IV and whether temperature distortion was occurring at the higher voltages and current available with the 371 compared to the 6485 Keithley picoammeter. However, published power diode forward IV have been discovered showing similar forward IV at room temperature.. 371 higher voltage/current forward IV testing is necessary to characterize the DSRD in the diode models to perform correctly in the DSRD-based pulser simulations. How accurate the forward IV must be, has not been determined, as well as, to what extent individual diodes can be reliably distinguished in modeling. A new method for fitting forward IV has been implemented in the CMC Verilog-A diode modeling code that will allow for more accurate fitting of the 371 data for its full range. More rigorous forward IV testing has

been implemented incorporating a number of modifications to the forward IV test fixture, cabling and testing methods (2- vs 4-wire) yielding forward IV with definite error bars. Also, lower current and voltage forward IV data are now taken with the Keithley 2450 sourcemeter which has a higher current limit (1 A) than the picoammeter (20 mA). Data collection of the DSRD inventory for forward IV using both the 2450 and 371 has been finished and the curves align well for most DSRD. Breakdown testing has also been performed for Gen2 and EG DSRD showing 40% yield for higher breakdown devices needed for DSRD stacking and DSRD pulser testing. The DSRD inventory has beenrefit within LTspice for diode parameters based on the new 2450/371 forward IV.

(F) TCAD-Based Doping Profile Performance Evaluation

Many DSRD TCAD simulation studies have been performed assessing the doping profiles used for the DSRD manufactured by SPT and in stock. The TCAD modeling has been on hold as effort is focused toward developing an accurate SPICE DSRD model due to the unavailability of manufacturer device models for MOSFETs and gate drivers within TCAD. A MOSFET model was developed for the Cree MOSFET for use within TCAD but still had some differences when used in pulser simulations, so the development of the DSRD SPICE model was prioritized so that manufacturer models (for MOSFETs and gate drivers) could be used.

Doping profiles are forthcoming for various SOS, dynistor and thyristor devices and TCAD will be used to assess their performance. Some interest has been expressed in assessing square-root doping profiles for DSRD. Gen3 doping profiles from the manufacturer have yet to be assessed within TCAD for performance differences with the requested doping profiles. As well, the recovery models within the CMC diode model are themselves based on PIN diode TCAD simulations and TCAD can perform DSRD doping profile specific simulations to determine model equations and parameters. Additionally, the forward IV behavior of our DSRD can be modeled as seen in the 371A semiconductor analyzer measurements. TCAD modeling will continue to be of use in device modeling since it is the only way to assess doping profiles when needed.

5.2 Pioneering Drift-Step Recovery Diode Processing and Manufacturing

(Alex Usenko)

Detailed reporting for this section has been transferred. A summary report of work for this sub-project completed under OSPRES Grant will be provided in the final report. Please see the May 2022 MSR for the most recent progress update.

5.3 Characterization of SOS Diode Performance through DOE Augmentation

(Joseph Reeve-Barker, Jay Eifler & Megan Hyde)

Reporting for this section can be found in Section 5.1 for this month. Please see the August 2022 MSR for the most recent update to this sub-project report.

5.4 DSRD-Based Pulsed Power Source Systematic Topological Optimization

(Shailesh Dhungana & Gyanendra Bhattarai)

5.4.1 *Problem Statement, Approach, and Context*

***Primary Problem*:** Inductive energy storage (IES) and release pulse generators that use drift-step recovery diodes (DSRDs) can be used as the fundamental units of all-solid-state high-power microwave (HPM) systems. The output from DSRD-based pulsers can then be fed into sub-nanosecond pulse sharpeners to achieve ultra-short high-voltage pulses. While DSRD-based pulsers can theoretically achieve the targeted 1's of GW in 1's of ns, their circuits are not topologically optimized to achieve high voltage gain (peak pulse voltage/prime source voltage), thus requiring large and heavy high-voltage (multiple kV) prime power supplies to achieve the required 100's of kV pulses. They also necessitate liquid-based cooling systems to dissipate the excess heat they generate during operation, further adding weight and rendering them impractical for Navy afloat missions.

***Solution Space*:** Systematically develop optimum circuit topology to maximize the voltage gain, and thus the peak voltage, peak power, and volumetric power density of DSRD-based HPM systems. Minimize the heat loss to be able to air cool by increasing energy efficiency through optimization of circuit elements without sacrificing the desired nanosecond risetime of the pulses generated. Air-cooled IES pulse generators using optimum DSRD stacking can remove the need for photo-triggered switches and their laser sub-systems. They are ideal for triggering sub-nanosecond rise-time sharpeners (SAS, D-NLTL, etc.), reducing overall cost, volume, and weight.

***Sub-Problem*:** DSRDs are not domestically available COTs components, but rather manufactured in small-batch quantities, with statistically significant variations in their performance parameters. In addition, our current SPICE models of these diodes may not be accurate due to unknown device parameters such as carrier distribution, carrier lifetime and the limiting current that we can pump without affecting the diode recovery property (see section 5.1 and 5.3) during high-voltage transients. These issues may lead to an inaccurate simulation model of the pulser and discrepancies between simulated and experimental results.

***State-of-the-Art (SOTA)*:** Air-cooled DSRD-based pulsers (equivalent in size to the pulse generators developed for this effort, i.e., ~0.01-m^3, ~2-kg) can achieve <20 kV, 1–2 ns risetime, and <4 ns FWHM across a 50 Ω load with a PRF of <15 kHz in burst mode. Available literature on IES pulse generators only describes a few circuit configurations, and there is a lack of comprehensive investigation of circuit topologies and optimization to achieve maximum gain and efficiency and reduce thermal load. Additionally, these pulsers are expensive and are not available within the United States.

***Solution Proposed*:** Develop different DSRD circuit topologies implementing series and parallel combinations of DSRDs (to increase reverse breakdown voltage and diode current, respectively) to minimize circuit components, such as inductors, capacitors, and switches. Systematically identify the best circuit topology and optimize the circuit components through physics-based DSRD pulser circuit theory and SPICE simulation to

maximize voltage gain and efficiency while minimizing the prime source voltage and thermal load.

Risks, Payoffs, and Challenges:

***Risks*:** All-solid-state DSRD-based IES pulsers require many other electronic components. Most importantly, the current pumping capability of available MOSFETs/electronic switches is limited, which may make maximizing the output voltage impossible even though the DSRDs are capable of higher current and output voltages.

***Payoffs*:** Being able to simulate and fabricate DSRD-based pulsers using physics-based pulser theory, partnered with US-based DSRD manufacturers, will enable a comprehensive domestic ability to optimize, produce, and evaluate these nanosecond pulsers.

***Challenges*:** Domestically manufactured (U.S.-based) DSRDs, which possess sub-optimal doping profiles, may lead to sub-optimal pulse generators. Accurate spice modeling of the diodes could be affected by expected wide variability in the diode characteristics or unavailability of advanced device characterization techniques. Determining the superlative ratio of design/development (through numerical analysis) to the effort put towards experimental testing/evaluation of the DSRD pulser is challenging due to the novelty of the approach. Extending the theory of single (1×1) pulse generator to cascaded (M×N) generator to increase the output will be very complex and may require significant time and computing power.

5.4.2 Tasks and Milestones / Timeline / Status

(A) Milestone – Develop theory of DSRD pulse generator to facilitate optimization of 1×1 pulse generator [***Completed JAN22***]

(B) Milestone – Extend the theory developed in Milestone A to facilitate optimization of M×N pulse generator [***Transitioned to PTERA-G***].

(C) Milestone – Construct/demonstrate a DSRD-based 1x1 pulse generator prototype based on theory developed in milestone (A) and obtain performance data for multiple combinations of diode stacks [***Transitioned to PTERA-G***].

(D) Milestone – Construct/demonstrate a DSRD-based 4×2 IES pulse generator prototype capable of producing $\geq$12 kV peak voltage, $\leq$1 ns risetime, $\leq$5 ns FWHM, $\geq$3 MW peak-power, $\geq$100 kHz PRF, $\geq$1,000 shots-per-burst, $\geq$500 number of bursts [***Transitioned to PTERA-G***].

(E) Milestone – Develop waveform inverter which, when combined with the pulser from Milestone C, enables a balanced differential waveform output with >90% inverted signal fidelity. [***Completed DEC21***].

(F) Milestone – Construct/demonstrate a M×N pulse generator prototype capable of producing $\geq$20 kV peak voltage, $\leq$1 ns risetime, $\leq$2 ns FWHM, $\geq$8 MW peak-power, $\geq$100 kHz PRF, and $\geq 2\sigma_{Vpeak}$, which operates in continuous-burst mode as a viable candidate for OSPRES Contract source alternative [***Transitioned to PTERA-G***].

5.4.3 *Progress Made Since Last Report*

This project has been transitioned to the PTERA grant. We will be reporting further progress in the PTERA monthly status reports. Work completed under OSPRES Grant will be summarized in the final report.

5.4.4 *Summary of Significant Findings and Mission Impact*

(A) A physics-based circuit working principle for DSRD-based pulser circuit is presented in the DEC 2021 reporting period. A systematic optimization of a 1×1 pulse generator based on the theory we have developed is presented.

(B) A proposed working principle for a two-stage DSRD pulser has been described in the MAY2022 MSR reporting period, however, with certain outstanding questions that may impact the efficacy of multi-stage DSRD pulsers. A new approach for stacking multiple 1×1 pulsers in parallel to increase the output voltage while keeping the MOSFET current and voltage within safe operating limit has been proposed. The extension of the circuit theory will be covered in the PTERA MSR.

(C) Using the 28-stack pulser, maximum peak outputs of 6.7 and 7.5 kV are obtained for a trigger length of 700 ns using a prime source voltage of 120 and 170 V. A pulser fabricated with four MOSFETs in parallel achieved an output of 9.2 kV using three 7-stack diodes for a prime source voltage of 140 V and a trigger length of 750 ns. Based on the DSRD pulser output using a single 7-stack diode, the reverse breakdown voltage of the EG1600 series diodes is estimated to be ~650 V. Measurement of circuit voltages at different nodes confirms the circuit performance matching the SPICE simulation.

(D) Transitioned to PTERA-G.

(E) Transitioned to PTERA-G.

(F) Transitioned to PTERA-G.

5.5 All-Solid-State Sub-ns MW Pulse Generators with Semiconductor Sharpeners

(Gyanendra Bhattarai)

This sub-project is currently on hold as focus is directed toward Section 5.4. Please review the January 2022 MSR for the most recent project overview and status.

6 Thermal Management

6.1 Ultra-Compact Integrated Cooling System Development

(Sam Sisk, Roy Allen, and Sarvenaz Sobhansarbandi)

6.1.1 *Problem Statement, Approach, and Context*

Primary Problem: A thermal management system (TMS) is required for cooling semiconductor-based pulse-power devices with the goal of maintaining the device temperature below 80 °C to avoid chip malfunction. In-line with the SWaP-C^2 objectives, the proposed TMS must be capable of providing 1 kW/cm^2 cooling rate to account for the amount of applied heat flux to the surface of the chip. Moreover, certain limitations should be considered for the pumping power. The TMS should be designed to be small enough to be used anywhere from data centers to drones, thus 1 cm^2 is targeted, with the capability of scaling up the dimensions.

Solution Space: To achieve such high cooling densities, we propose a modified jet impingement TMS (JI-TMS) design based on the preliminary results achieved by the group in earlier stages of this project. The JI-TMS is expected to achieve an enhanced heat transfer rate due to the creation of turbulent flow by a unique nozzle array design. The JI-TMS is also expected to have some pressure losses due to the fluid flow path. As the proposed TMS dimensions are restricted to 1 cm^2 surface area, the required pumping power should be kept to a minimum.

Sub-Problem: The turbulency formed from the array of nozzles on the targeted surface creates an extreme pressure loss, which is mainly from the large amount of jet nozzles impinging fluid streams interfering with other fluid streams. The pressure must be sustained to enable proper cooling and circulation processes.

State-of-the-Art (SOTA): Integrated chip cooling is being widely used to dramatically increase the operational power of high-voltage silicon-based power devices. However, the current SOTA devices include surface-to-surface contact points that rely on cohesive connections. These connections increase the amount of material through which heat must be transferred to the coolant, thus limiting the heat removal rate.

Objective: To design, simulate and investigate the performance comparison of the proposed JI-TMS with the SOTA TMS designs under the same operating conditions, and optimize the design through an iterative process. The proposed JI-TMS design is based on refining in-chip jet-impingement geometry through leveraging theory of fluid flow and a parametric evaluation of nozzle geometry, flow channel arrangements, and outlet-to inlet area ratio.

Challenges: The manufacturing techniques such as layering needed for a JI-TMS integrated onto a chip are expensive, so other manufacturing techniques should also be explored such as CNC milling. As the proposed compact design is restricted, due to the low tolerances needed for the geometries of the nozzles and heating plate, the manufacturing process must be capable of having a cohesive bond of the TMS and target surface (chip).

Risks: With a system so compact, the pressure drop could be a large issue. An extreme pressure drop would potentially cause the coolant to flow backwards, causing less fluid-to-solid interaction.

6.1.2 *Tasks and Milestones / Timeline / Status*

(A) Design a 1 cm^2 Si base JI-TMS to achieve a heat dissipation rate of 1 kW/cm^2. The device will also need to be designed in a way where it can be manufactured as proposed. / MAR22–MAY22 / Completed

(B) Using the computational fluid dynamics (CFD) modeling, simulate how de-ionized water will affect the cooling rate. The operating conditions will remain the same for all geometry design iterations to ensure simulation continuity and useful comparison. / MAY22–JUN22 / Completed

   a. Compare the results with the previous design iterations and make improvements to meet the target metrics.

   b. The process of looping through (A) and (B) will continue until a design addresses all main and sub-problems as well as challenges stated previously; once accomplished the selected design will be used for further investigation in the next stage of the project.

(C) Using the selected design, perform ANSYS simulations using nanofluid or other fluids with high thermal conductivity as the coolant, and evaluate how fluid type changes the effectiveness of the TMS in terms of heat extracted and pressure losses. / JUN22–SEP22 / Completed

   - Perform feasibility analysis of the simulation results to be comparable to a real-world process. This will be done by validation with other JI-TMS experimental and simulated data in the literature.

6.1.3 *Progress Made Since Last Report*

(C) Simulations are validated through other JI-TMS designs in the literature. The coolant alternatives are examined at this stage.

6.1.4 *Technical Results*

(C) The achieved results from de-ionized water simulation showed an average surface temperature of 74 °C, which is below the target temperature threshold. By utilizing pure silicone fluid, with thermal conductivity of $0.0454\frac{W}{m\,K}$, the average surface temperature of 36.73 °C was achieved which shows enhancement compared with the de-ionized water.

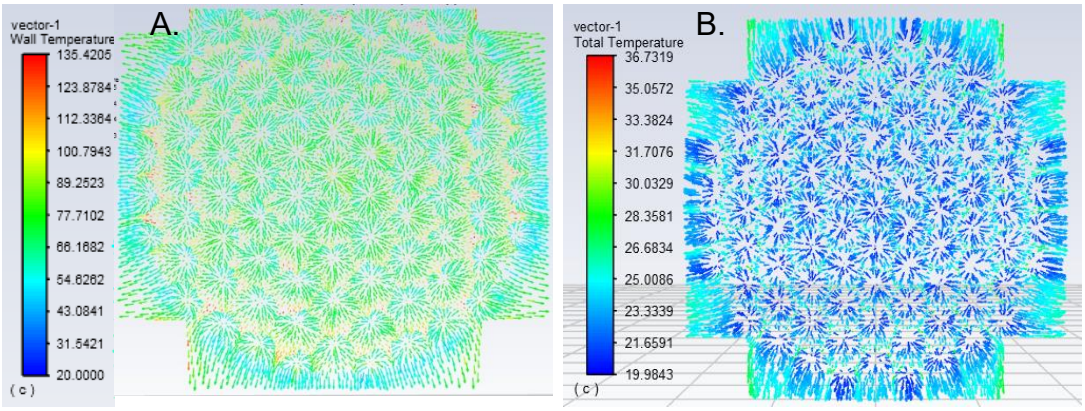


Figure 6.1.2. Top view of JI contact displaying contour plot of velocity vector colored by temperature. (A) Fluid is water, (B) fluid is pure Si fluid.

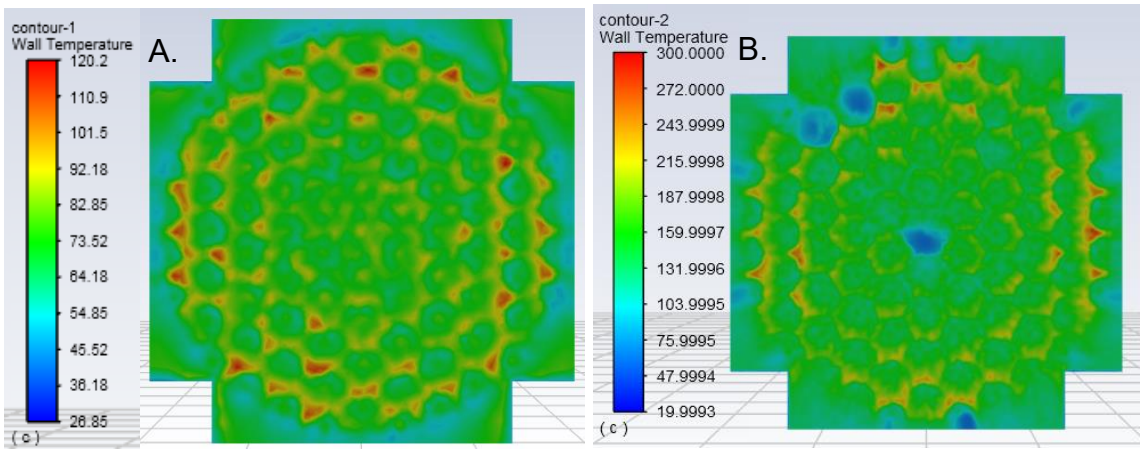


Figure 6.1.3. Top view of JI contact displaying contour plot of temperature. (A) Fluid is water, (B) fluid is pure Si fluid.

6.1.5 *Summary of Significant Findings and Mission Impact*

(C) It was found that silicon fluid exhibits an increased performance in removing heat at the heated surface, but due the heat removal is limited due to viscosity being so high and the geometry being to small. However, the pressure changes need to be further investigated once the design needs to be prototyped and experimentally investigated.

6.1.6 *References*

[1] Wu, Ruikang, et al. “Thermal Modeling and Comparative Analysis of Jet Impingement Liquid Cooling for High Power Electronics.” International Journal of Heat and Mass Transfer, vol. 137, no. Complete, July 2019, pp. 42–51, doi:10.1016/j.ijheatmasstransfer.2019.03.112.

7 Pulse-Forming Networks

7.1 Diode-Based Nonlinear Transmission Lines

(Nicholas Gardner)

A summary report for this sub-project will be provided in the final report. Please see the January 2022 MSR for the most recent summary and status and the Outputs section for papers in preparation or published.

7.2 Continuous Wave Diode-NLTL based Comb Generator

(Nicholas Gardner and John Bhamidipati)

A summary report for this sub-project will be provided in the final report. Please see the May 2022 MSR for the most recent summary.

7.3 Pulse-Compression-Based Signal Amplification

(Feyza Berber Halmen)

7.3.1 *Problem Statement, Approach, and Context*

Primary Problem: Solid-state amplifiers, such as gallium-nitride-based high electron mobility transistors (GaN HEMTs), can be used as high power microwave (HPM) sources to achieve the SWAP-C2 performance metrics necessary to support the cUAV Naval afloat mission. However, even the best high-power GaN HEMTs are limited to 2–3 kW of peak power, much lower than the 0.1 to 3 MW pulsed power available from traditional HPM sources such as travelling wave tubes (TWTs). Achieving a power density of 1 W/cm^2 at a distance of 10 m with a high gain (≥ 10 dBi) narrow-band antenna requires an input power increase of two to three orders of magnitude. Power combination methods to achieve an effective radiated power (ERP) at MW scale require 10's to 100's of GaN HEMTs, compromising the SWAP-C2 performance.

Solution Space: Pulse compression techniques are used to increase the peak power and lessen the pulse width in HPM applications. Adapting pulse compression at the GaN HEMT or any other SWAP-C2 compatible source output can achieve sufficient ERP with an optimal radiating element.

***Sub-Problem*:** Pulse compression is generally used to generate a pulsed output with a high peak output power (P_{out_peak}) and a wideband frequency content from a DC input voltage. The main challenge lies in identifying a pulse compression technique that can be used to amplify a narrowband RF input signal. Some of the circuit elements for common pulse compression techniques, such as the saturable inductors used for energy storage in magnetic pulse compression (MPC), exhibit increasingly lossy behavior with high frequency. Another challenge will be to determine, if any exist, the operating frequency limits of suitable pulse compression techniques for high-frequency, high-power signals.

State-of-the-Art (SOTA): Large magnetic pulse compression (MPC) circuits (>1 m^3, >1000 lbs) have demonstrated peak output power up to a few GWs. Smaller versions (~0.125 m^3, 50 lbs to 100 lbs) can achieve 7.5 MW peak power [1].

Deficiency in the SOTA: Traditional MPC systems are large (few meters long), leverage huge transformers, and require liquid coolant such as transformer oil, which leads to undesirable system mass values of ≥1000 lbs. They are used for generating medium or high pulse power traditionally from DC or AC (50/60 Hz) high voltage supplies. There is no known example of high-frequency signal amplification utilizing MPC.

Solution Proposed: Developing a pulse compression circuit that will act as a high-power signal amplifier with a gain of ≥10. Utilizing magnetic pulse compression, or any other suitable pulse compression method, for high power signal amplification with source fidelity.

Relevance to OSPRES Grant Objective: Pulse compression will enable a size and cost efficient solution to high power signal amplification that will lead to HPM source development with optimal SWaP-C2 parameters.

Risks, Payoffs, and Challenges:

Challenges: Modeling pulse compression circuits for high-frequency operation can present a challenge. Pulse compression circuits are generally evaluated in SPICE simulators with low-frequency AC / transient simulations. SPICE is a lumped-element model simulator and cannot solve for the distributed-element model required at high frequencies where the wavelengths become comparable to the physical dimensions of the circuit. Some circuit components, such as the saturable inductor in the MPC, are not available in SPICE or many other simulators and need to be modeled using behavioral models and proprietary material data. Pulse compression circuit modeling, especially at high frequencies, needs to be investigated.

Risks: Pulse compression methods are usually lossy in nature and generate a considerable amount of heat; therefore, designing a proper cooling method must be carried out, which may inadvertently increase the volume (size and weight) of the overall design.

7.3.2 *Tasks and Milestones / Timeline / Status*

(A) Milestone – Demonstrate 2–3 times increase in peak power and compression gain using magnetic pulse compression (MPC) [*complete*].

1. Subtask – Model saturable inductors in LTSpice or Matlab/Simulink in order to be able to develop MPC simulations / NOV21 / Complete.
2. Subtask – Investigate the operation, design, and pitfalls of MPC circuits / / *complete*.
3. Subtask – Design MPC circuit with RF input and simulation in LTSpice or Matlab/Simulink to evaluate the resulting amplification and frequency content. / *complete*.
4. Subtask – Model the high frequency behavior of MPC circuit / DEC21 / *complete*.
5. Subtask – Build and test the MPC prototype using bench top power supply / OCT21 */ suspended*.

(B) Milestone – Investigate pulse compression methods other than MPC for feasibility *partially complete*

1. Subtask – Study time reversal pulse compression to assess its compatibility with GaN-based source. partially complete.

(C) Milestone – Increase the compression gain available from PC. suspended

(D) Milestone – Build and test SWAP-C2 compatible high-frequency PC prototype with GaN source. suspended

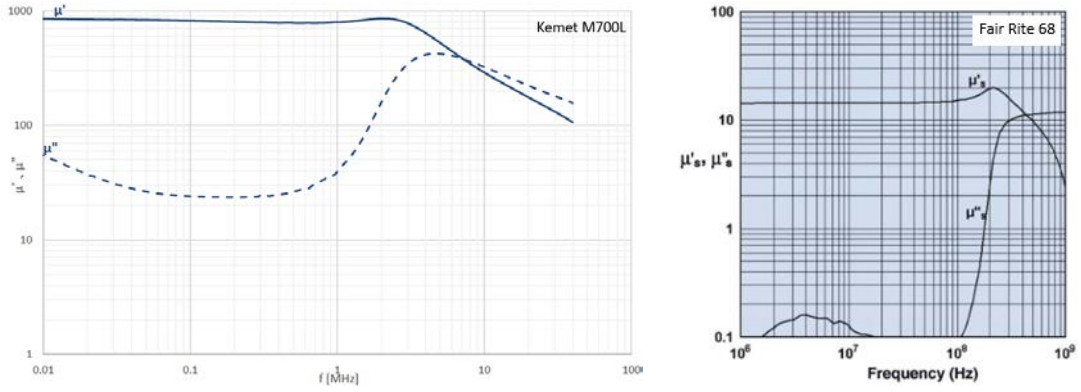
7.3.3 *Progress Made Since Last Report*

(A.2) In order for accurate evaluation of high frequency MPC viability, several design constraints to ensure efficient energy transfer and saturation were detailed..

7.3.4 *Technical Results*

(A.2) For the final OSPRES MSR, design considerations for sinusoidal input, high frequency MPC circuit were investigated. Constraints on magnetic core materials, circuit component sizing, loading and input signal characteristics are detailed for an accurate evaluation of MPC viability.

A Kemet M700L magnetic core has been used for the MPC circuits reported in the previous MSRs. Even though the Kemet M700L is advertised to operate up to several hundred MHz for noise and electromagnetic interference (EMI) applications [2], they can only be used up to several MHz for MPC applications. The complex permeability of the M700L, shown in Figure 7.3.1(a), indicates that the material becomes more resistive than inductive over 1 MHz [3], making it too lossy for energy transfer in an MPC circuit. Fair Rite Material 68 is the optimal commercially available magnetic core as explained in the July22 MSR. Material 68 can be used at slightly over 100 MHz [4] for MPC as suggested by its complex permeability in Figure 7.3.1(b). Fair Rite 68 toroids are considered as the magnetic core material in the discussions below.



(a) (b)

Figure 7.3.1. Complex permeability for (a) Kemet M700L [3] and (b) Fair Rite Material 68 [4].

For an MPC circuit, the total compression gain is determined by the ratio of resonant times of each stage. With equal capacitors and the same magnetic cores used in each stage for efficient energy transfer [5], the compression gain for a 2-stage MPC reduces to:

$$G_{MPC} = \frac{t_0}{t_1} \cdot \frac{t_1}{t_2} = \sqrt{\frac{L_{0,sat}}{L_{1,sat}}} \cdot \sqrt{\frac{L_{0,sat}}{L_{2,sat}}} = \frac{N_0}{N_1} \cdot \frac{N_1}{N_2} = \frac{N_0}{N_2}. \quad (1)$$

The ratio of turns for the input and output stage inductors determines the compression gain for the MPC. The maximum number of turns, and therefore the compression gain, is limited by the magnetic core toroid dimensions and the parasitic winding capacitance.

Note that the maximum energy transfer in each stage is given by [5]:

$$E_T = \int_0^{T/2} I(t)V(t)dt = \left(\frac{V_0 T}{2\pi}\right)^2 \cdot \frac{1}{L_{sat}}, \quad (2)$$

where Vo is the maximum node voltage on the capacitor and T is the resonant time. According to equation (2), total inductance during saturation should be minimized for maximum energy transfer. This condition results in the last stage of compression using N=1 or 2 for the saturable inductor design. The saturated inductance for a toroid is:

$$L_{sat} = \frac{\mu_0 \mu_{sat} N^2 A_e}{l_e} \approx \frac{\mu_0 N^2 A_e}{l_e}, \quad (3)$$

where A_e and l_e are the magnetic material cross-sectional area and the magnetic field path length, respectively. A_e is determined by the saturation condition, given the input voltage, saturation time, and saturation flux density. As relative permeability is approximately unity for a saturated inductor and N is limited to 1 or 2 for low inductance design, the only flexible design parameter is the magnetic path length, which is approximately equal to the winding width for a saturated inductor. Setting the winding width equal to the core length, i.e., using the entire core for conductor windings, provides the lowest saturated inductance.

For the MPC with sine input, the saturable inductors are saturated in both directions, eliminating the need for a reset circuit for the cores. This means that in the input signal amplitude and frequency should provide enough flux to saturate the inductor for $\Delta B = 2B_{sat}$. For saturation occurring at half signal period, the time voltage product, VT, required is:

$$\int_0^{\frac{\pi}{\omega}} V_0 \sin \omega t \, dt = 2B_{sat} \cdot N \cdot A_e \quad \Rightarrow \quad V_0 \cdot T = \ 2\pi \cdot B_{sat} \cdot N \cdot A_e \quad (4)$$

The dimensions for commercially available Fair Rite Material 68 toroids are tabulated in Table 7.3.1. The saturated inductance ($\mu_{r,sat} \approx 1$) and VT required for saturation (B_{sat}=270 mT) is also included for a 2-stage MPC input and output inductors. Assuming a gain of 4 at each stage, the input and output inductors have N=16 and N=1, respectively. Table 7.3.1 also includes the input voltage that would be required to saturate the input inductor

at 100 MHz input. At 100MHz, the input signal amplitude needs to be 35-430 kV for a design with these cores due to the extremely short time available for saturation.

Table 7.3.1. Available Fair Rite 68 toroid dimensions and corresponding L_{sat}, VT and V_{in}.

Area	Length	$L_{sat,2}$ (for N=1)	VT_2 (for N=1)	$L_{sat,0}$ (for N=16)	VT_0 (for N=16)	V_{in} (at f=100MHz)
12.9 mm^2	29.5 mm	0.55 nH	21.88 μVs	140.8 nH	0.35 mVs	35 kV
78 mm^2	89 mm	1.1 nH	132.2 μVs	256 nH	2.1 mVs	210 kV
158 mm^2	145 mm	1.37 nH	268.0 μVs	350.7 nH	4.3 mVs	430 kV

Toroids with cross-sectional area of ~1 mm^2 exist for other ferrites [6]; however, toroid dimensions required to fit in the conductor windings need to be considered. Even if such small toroids can be used in the design, the input amplitude requirement is only relaxed by an order of 10. Using a regular inductor for the input stage would also relax the input voltage requirements as a lower N value can be used for the saturable inductor in the 1st MPC stage. Note that high frequency NiZn Ferrites have the lowest B_{sat} of several hundred mT among the commercially available magnetic materials. Any new high frequency material development effort for MPC, such as the one proposed by KRI, should also aim decreasing magnetic material B_{sat}. Figure 7.3.2 shows V_{in} required for saturation vs. frequency for B_{sat} values between 1 - 270 mT. V_{in} values are calculated for A_e=12.9 mm^2 and N=4. B_{sat} needs to be lower than 10 mT for V_{in} requirement to be reduced to several hundred volts, a more realistic value for solid-state amplifier output voltages.

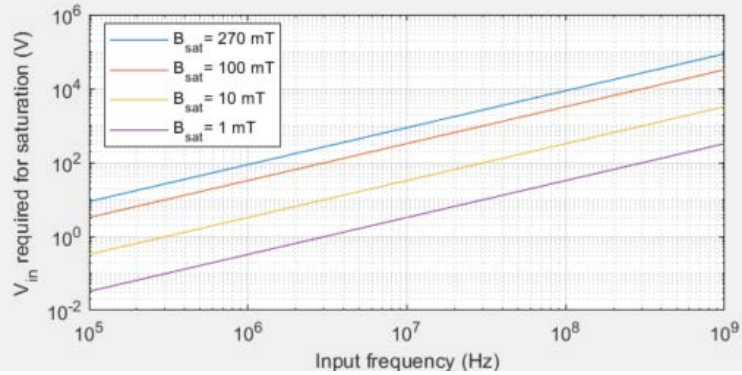


Figure 7.3.2. V_{in} required for inductor saturation at different input frequencies for various magnetic core saturation flux densities (A_e = 12.9 mm^2 and N=4).

Another consideration for the MPC design is the load resistor selection and its effects on other design parameters. The optimum load resistance for MPC, as explained in July 2022 MSR, is:

$$R_L = Z_0 = \sqrt{\frac{L_{2,sat}}{C}} \tag{5}$$

and the input frequency for the sinusoidal input MPC is given by:

$$\omega_0 = \frac{1}{\sqrt{L_0 C}} \, . \tag{6}$$

Given equal capacitors are used for efficient energy transfer and the inductors are related through Equation (1), R_L can be expressed in terms of input frequency, compression gain and $L_{2,sat}$ as:

$$R_L = 2\pi \cdot f \cdot G_{MPC} \cdot L_{2,sat} \tag{7}$$

Equation (7) needs to be considered if the resistive load is to be optimized, i.e., 50 Ω for ease of integration. For R_L=50 Ω with a 100MHz input frequency MPC design using the saturable inductors given in Table 7.3.1, an MPC gain of 58 to 145 is required for $L_{2,sat}$ = 1.37 nH and 0.55 nH, respectively. Reasonable compression gain values limit R_L to mΩ range for lower frequency design but 50 Ω is easily achievable at high frequencies. For example, optimum load resistance is 55 Ω for an MPC with last stage saturated inductance of 0.55 nH and compression gain of 16 at 1 GHz.

7.3.5 *Summary of Significant Findings and Mission Impact*

(A) Initially a basic 2-stage magnetic pulse compression (MPC) circuit was built and tested with DC input to better understand the MPC principles and considerations such as inductor sizing, pre-pulse currents, and inductor saturation. Next, saturable inductor modeling was realized in LTSpice with inductor flux expression and the Chan model [2]. Prior to MPC system simulations, magnetic core losses were investigated, and core selection constraints were determined based on the core losses and high-frequency MPC design considerations. Next, different magnetic core materials were investigated to determine the most suitable candidate for high-frequency MPC. As reported in Jan 2022 MSR, such a core should have high resistance, a narrow hysteresis loop, minimized eddy current area, and low saturation flux density (B_{sat}). High permeability (μ) and very sharp saturation characteristics are also preferred in order to minimize pre-pulse currents and resulting MPC gain loss. NiZn ferrites are the best option among the commercially available magnetic cores for the high-frequency MPC application as they have the highest operating frequency, low B_{sat}, and sufficiently high μ. After investigating suitable magnetic cores and their properties, LTSpice simulations of the previously tested 2-stage MPC circuit were resumed using the Chan model for Kemet NiZn cores. The effects of core coercivity and remanence on MPC operation, which is not included in the design equations, were simulated, and high remanence and low coercivity were found to result in the lowest leakage currents due to sharper saturation behavior. MPC simulations were continued to observe the effects of resistive loading. The optimal energy transfer is obtained for load resistance matched with output stage impedance, which results in very small, e.g., mΩ range, load resistors. MPC circuit elements and input voltage could be sized to maximize the load resistance, and related design equations were derived. Some voltage and current artifacts due to non-ideal switch behavior were

observed with resistive loading. After determining the optimal load resistance for the designed MPC circuit, it was modified to operate with sinusoidal input. Initial simulations show stable operation after a few cycles of settling behavior. 10x power amplification is obtained with the design, providing proof of concept for sinusoidal signal power amplification with MPC. In order to accurately evaluate the viability of sine input MPC, some constraints on core material and circuit component sizing were detailed. The last stage saturated inductor is minimized for max energy transfer in each stage. Core cross-sectional area is determined based on the saturation condition, but the core magnetic path length can be maximized to reduce inductance. For saturation at high frequencies, even the minimum core cross-sectional area results in input voltage requirement in the order of kV. Optimum material for high frequency MPC needs B_{sat} < 10 mT so that it can be saturated with a solid-state amplifier output. Load resistor values for optimum energy transfer are in the order of mΩ for lower frequency design but 50 Ω loading is easily achievable for 1 GHz operation. Commercially available magnetic cores were investigated for their suitability for the MPC prototype operating at MHz to GHz frequency range. Material 68 from Fair-Rite is the best commercially available option, offering the highest cutoff frequency of 350 MHz with relative permeability of only 7.5.New magnetic material development is needed to realize a magnetic switch at higher frequencies. A SoW was drafted with KRI for the design and fabrication of a NiZn- magnetic nanoparticle composite with cutoff frequency of over 500 MHz and relative permeability of 25. MPC viability and the MIDE-KRI material development proposal will be evaluated during the annual review in Nov 2022. MPC project will either be shelved or will continue with more theoretical and experimental work, as well as material development, depending on the viability discussions.

(B) Time reversal pulse compression (TR PC) was investigated as an alternative PC-based signal amplification method. TR PC shows a few dBs of gain in the time domain but loss in the frequency domain as its main component, the resonant cavity, is a passive and lossy circuit element. One-bit time reversal (OBTR) PC, which increases the time domain gain to ≥20 dB, shows ~3x gain in the frequency domain at some frequencies but completely distorts the output signal due to the digitization process. The impulse response record time significantly affects the compression gain and limits the pulse repetition frequency. The compression gain also drops significantly for narrowband signals. Time-reversal-based pulse compression methods were therefore found to be incompatible with a GaN source, especially due to their limited PRF and low compression gain for narrowband signals. OBTR PC is re-evaluated as an alternative PC-based signal amplification method through discussions with our collaborator. Significant time domain gain is observed with one-bit (OB) TR PC when a continuous-wave (CW) source is pulsed with very narrow pulse widths. The frequency domain waveforms have not yet been investigated for this case. However, more than 20 dB gain is observed in the frequency domain if the gain is re-defined as the ratio between the input impulse and the output reconstructed pulse for the evaluation of OBTR-PC as a “signal amplifier”. More in-depth study is needed to determine if OBTR-PC could provide signal amplification for a pulsed GaN source.

7.3.6 *References*

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[3] Kemet Electronics Corporation, "M700L Material Specification", 4/5/2022, obtained via private communication, accessed: 4/6/2022

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8 Antenna Development

8.1 Tradespace Analysis of an Array of Electrically Small Antennas (ESAs)

(Bidisha Barman and Deb Chatterjee)

8.1.1 *Problem Statement, Approach, and Context*

Primary Problem: Determine the extent to which the physical aperture size of an antenna array, composed of patch elements, can be reduced, while maintaining performance in peak power density, bandwidth, and electronic beam steerability over the UHF range (0.4–1 GHz), compared with present-art high-power-microwave-capable antenna arrays.

Solution Space: An array of patch antenna elements whose feed, two-dimensional shape, and relative placement (i.e., intra-, and inter-element design) allow for the physical aperture size to be reduced by more than 20% compared with the present-art.

Sub-Problem: To overcome scan blindness (as the main beam is electronically steered), due to the excitation of surface waves (SW). (Note: scan blindness is a common phenomenon in electrically small microstrip patch antenna arrays).

State-of-the-Art (SOTA): Horn, reflector, Vivaldi, valentine, etc. are some of the commonly used ultra-wideband (UWB) antenna elements in a phased array for high-power microwave (HPM) transmissions.

Deficiency in SOTA: Large physical aperture size of the antennas.

Solution Proposed: Using electrically small antennas (ESAs) as array elements and optimizing their performance in terms of both near-field (bandwidth) and far-field (directivity) parameters, followed by arrangement of the ESAs in suitable lattice structures (preferably, hexagonal/triangular) to reduce the overall array aperture area. Using stochastic and machine learning (ML) algorithms to optimize antenna element and array performance.

Relevance to OSPRES Grant Objective: Provides design and optimization guidelines for UWB ESA elements, especially coaxial probe-fed microstrip patch antennas, and arrays for HPM applications.

8.1.2 *Tasks and Milestones / Timeline / Status*

(A) Develop an Array Pattern Tool in the context of lightweight calculations of large antenna arrays / JAN–MAY 2021 / Completed MATLAB code.

(B) Investigate the effects of array aperture area reduction on different array parameters (such as gain, beamwidth, electronic beam steerability) and present a comparative study of antenna array parameters as a function of array aperture area / JAN–MAY 2021 / Completed.

(C) Build minimum viable validation prototypes of single ESA elements on substrates that have good power handling capabilities for HPM transmissions at UHF range (such as polyethylene, FR-4, TMM-10i, TMM-6) / JAN 2021–SEP 2022 / Completed

manufacturing and S_{11} parameter testing of the updated SLA patch with tapered, coaxial, feed.

(D) Optimization of ESA (single element) performance using ML based stochastic search algorithms / JUN 2021–FEB 2022 / Completed single objective optimization of ESA elements.

(E) Build minimum viable validation prototypes for arrays of ESA elements / JUN 2021–SEP 2022 / Completed modeling and characterization of a 15×15 array for simulation-based demonstration.

(F) Optimization of array performance using ML algorithms / SEP 2021–FEB 2022 / Completed single objective optimization of antenna arrays on infinite ground planes.

8.1.3 *Progress Made Since Last Report*

(C) Build minimum viable validation prototypes of single ESA elements:

a. Completed prototyping of an improved version (v2) of the tapered, coaxial-connector-fed, microstrip patch antenna element, for operation in the desired UHF range (0.7–1.2 GHz).

b. Measurement of S_{11}-parameter of the antenna showed $\sim 58\%$ of impedance bandwidth.

c. Antenna gain to be measured and reported during the NOV2022 ONR OSPRES-G Review Meet.

8.1.4 *Technical Results*

(C) Build minimum viable validation prototypes of single ESA elements:

Manufacturing of an improved version of the tapered, coaxial-connector-fed, microstrip patch antenna, for operation in the UHF range (0.7–1.2 GHz), has been completed. Many structural discontinuities that were encountered in the first version of the prototype have been eliminated in this updated version.

To alleviate the discontinuities and help improve the antenna's S_{11} and gain performances, the 3D SLA printer was employed to print the substrate and the tapered connector as a single block. For metallization of the patch and ground planes, silver paint has been used, which helped reduce metallic discontinuities. The CAD model and final manufactured prototypes are shown in Fig. 8.1.1.

The S_{11} parameter of the prototype-v2 was tested using Keysight's FieldFox Microwave Analyzer. The testing setup and a comparison of the simulated and measured S_{11} parameters of the antenna are shown in Fig. 8.1.2. Reduction in electromagnetic discontinuities in the improved version of the prototype (v2) can be easily observed through the improvement in S_{11} response of the prototypes (see Fig. 8.1.2b).

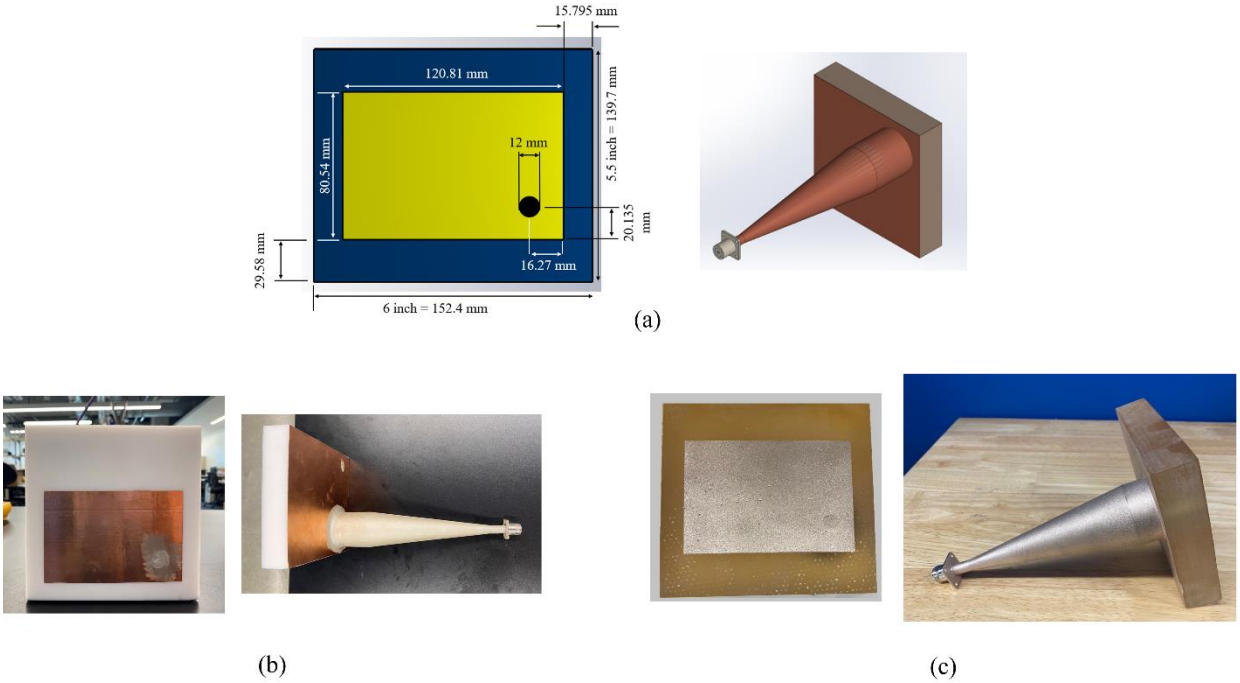

Figure 8.1.1. Front and side views of the improved SLA patch antenna with tapered, coaxial, feed: (a) CAD model, (b) manufactured prototype – v1, and (c) manufactured prototype – v2 (improved).

The measured impedance bandwidth of the prototype-v2 is ~58% (0.7126–1.299 GHz), which is a 12% improvement compared to the simulated data (~36%). This result is extremely significant since such a wide bandwidth, from a simple microstrip patch antenna design, has never been reported in the literature before.

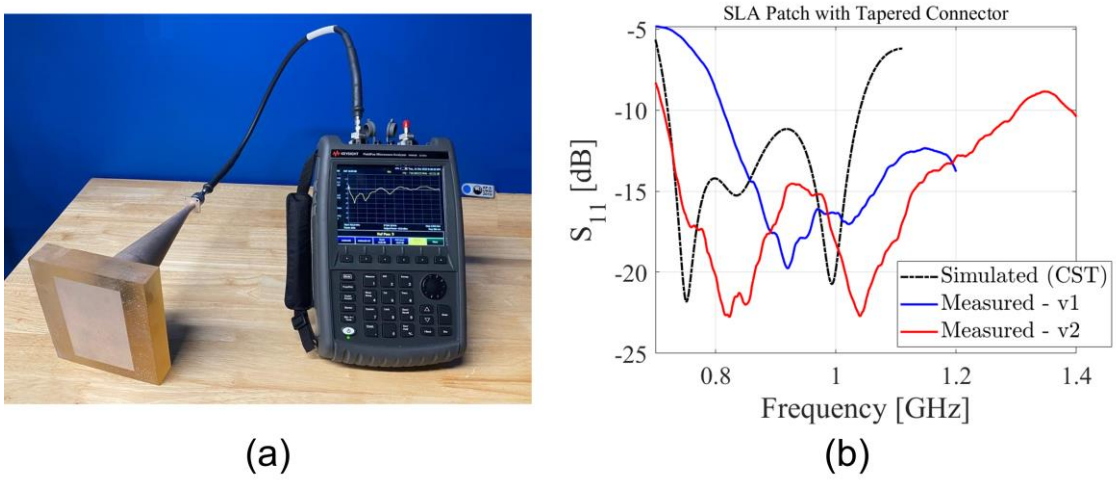

Figure 8.1.2. (a) S_{11} measurement setup using Keysight's Fieldfox VNA. (b) Simulated and measured S_{11}-parameter of the antenna.

Table 8.1.1. Comparison of the simulated and measured S_{11}-parameter data.

	Frequency Range ($S_{11} < -10$ dB)	%BW
Simulated	0.7208–1.039 GHz	36.2
Measured (v1)	Upper frequency limit unknown	-
Measured (v2)	0.7126–1.299 GHz	58.3

8.1.5 *Summary of Significant Findings and Mission Impact*

(A) Developing Array Pattern Tool for large arrays calculations:

A MATLAB code has been developed for faster radiation pattern approximation of a linear/planar array of any size and composed of any type of antenna elements. The code requires the center element pattern of a small array (say, 3×3) composed of the same type of antenna elements, desired lattice arrangement, and total number of array elements, as user inputs. The usage of this code will be included in future publications.

(B) Investigate the effects of array aperture area reduction on different array parameters:

The effects of different aperture shape and lattice arrangements on array gain and beam steerability have been studied for arrays modeled on PEC-backed substrates. Investigations show that a transformation from square-grid-rectangular-aperture to triangular-grid-hexagonal-aperture leads to $\approx 30\%$ reduction in aperture area ($\approx 50\%$ reduction in number of array elements) with a tradeoff of ≈ 1.5 dBi (in 2.5–5 GHz) and ≈ 3.5 dBi (640–990 MHz range) gain reduction. The aperture area reduction, however, comes at the cost of limited beam steerability to $\pm 45°$ from boresight, compared to the $\pm 60°$ scanning capabilities achieved from the square-grid-rectangular-aperture arrays, at all frequency ranges.

(C) Build minimum viable validation prototypes of single ESA elements:

Developed a design technique for electrically small microstrip patch antenna that provides $\geq 30\%$ impedance bandwidth by strategic placement of the feed-probe along the patch diagonal, at operating frequencies in the UHF (MHz) to microwave (GHz) frequencies. The method avoids any sophisticated prototyping and is a transformative approach in the design of electrically small microstrip antennas for ultrawideband wireless applications. The design approach was validated at the 2.5-5 GHz range, using prototypes manufactured on TMM-6 and TMM-10i substrates, and at the UHF range (0.7-1.3 GHz), using a prototype built on 3-D printed SLA substrate.

(D) Optimization of ESA (single element) performance using regular, and ML based stochastic search algorithms:

Optimization of feed-probe location, ground plane shape and size in a microstrip patch antenna, with the objective of bandwidth enhancement, using ML based stochastic search algorithms (GA, PSO, and Simplex methods), was performed. ML algorithms were found to be ≈ 2 times faster and ≈ 0.3 times less memory intensive compared to regular search algorithms, while maintaining the same degree of accuracy.

It is concluded that, although these automated ML algorithms do not provide insight into the underlying physics of the problems and require human intervention at every stage for better decision making, they can still be considered as potential tools for faster optimization of antenna performance, especially for multi-objective optimization of complex structures, which is computationally intensive using conventional EM solvers.

(E) Build minimum viable validation prototypes for arrays of ESA elements:

A 3×3 array of wideband antenna elements (2.5–5 GHz) and a 2×2 array of narrowband antenna elements (900 MHz), on TMM-10i substrates, were manufactured and tested. In both the cases, reasonably good agreement were achieved between simulated and measured S_{11} and gain responses of the individual array elements, thereby providing a proof-of-concept of the array design approach.

(F) Optimization of array performance using ML algorithms:

Completed inter-element spacing optimization in a 4×4 square-grid array, on an infinitely large, PEC-backed dielectric substrate, using a ML-based genetic algorithm (GA), in the 2.5–5 GHz range, with the objective of array boresight gain enhancement. ML-based GA was found to be ≈ 0.5 times faster than a regular GA based optimization, However, the generation of data samples that were used for training the ML algorithm is very time consuming, rendering the optimization approach largely inconsequential in this application paradigm.

8.2 Tradespace Analysis of Ultra-Wide-Band (UWB) Koshelev Antenna

(Alex Dowell and Kalyan Durbhakula)

8.2.1 *Problem Statement, Approach, and Context*

Primary Problem: Determine the extent to which the physical aperture area of an antenna array, composed of antenna elements, can be reduced, while maintaining performance in peak power density, bandwidth, and electronic beam steerability over the UHF range (0.4–1 GHz), compared with present-art high-power-microwave-capable antenna arrays.

Solution Space: The Koshelev antenna has a unique design that is capable of generating an UWB response by effectively merging radiation characteristics from a transverse electromagnetic (TEM) horn antenna with exponentially tapered flares, an electric monopole, and magnetic dipoles over a wide frequency range [1]. This opens up an opportunity to investigate the design parameter space and understand parameter effects on impedance bandwidth, radiation pattern, electric field distribution, and other metrics via a tradespace study.

Sub-Problem:

(i) The integration of an impedance transformer to a single element Koshelev antenna to simulate and test the combined (transformer–antenna) performance is currently not feasible using commercial EM simulators.

(ii)The total surface currents on the Koshelev antenna over the desired frequency range arising from the present positioning of TEM exponential flares, an electric monopole, and magnetic dipoles is not yet clearly understood.

State-of-the-Art (SOTA): The balanced antipodal Vivaldi antenna (BAVA) is considered to be the SOTA antenna element due to its exceptional 20:1 impedance bandwidth ratio as well as the ability to handle tens-of-MW input power.

***Deficiency in the SOTA*:** The BAVA design parameter space has been exhausted over the past couple of decades. The physical aperture area still remains very large and there is no viable path through tradespace study for further physical aperture area reduction.

Solution Proposed: Design, simulate, validate, and perform a tradespace study on the important design parameters of the Koshelev antenna array that effectively reduce its physical aperture area while maintaining its UWB properties, in both the frequency and time domains. The Koshelev antenna has been shown in the literature to withstand higher voltage levels (over 200 kV peak voltage), thereby making it a viable antenna element for detailed tradespace study and analysis.

Relevance to OSPRES Grant Objective: From the literature, it was shown that the Koshelev antenna can handle high input voltages (and therefore high power with 50 Ω input impedance), which satisfies the specific OSPRES objective related to high input voltage/power. In addition, this work can yield a center-frequency-dependent, bandwidth-controlled, and electronically steerable Koshelev antenna design that can be quickly modified to the spectrum properties of the ultra-fast rise time input pulse.

Risks, Payoffs, Challenges:

(i) The electrical size of the Koshelev antenna is approximately λ/4 at its lowest operating frequency. Further reduction of electrical size to λ/10 could considerably reduce frequency dependent gain, thereby decreasing the power spectral density.

(ii) Payoffs include the development of a library of antenna metrics data for different shapes and sizes of the individual parts within the Koshelev antenna.

(iii) The large electrical size (>5λ) of the Koshelev antenna at its highest operating frequency poses huge computational challenges.

8.2.2 *Tasks and Milestones / Timeline / Status*

(A) Complete literature search to identify and list antenna elements that satisfy UWB properties and HPM requirements, and down-select accordingly / NOV–DEC20 / Complete.

(B) Complete initial design, simulation, and validation of Koshelev antenna [1] / JAN21 / Complete.

(C) Perform a preliminary parameter study to identify design parameters that considerably reduce the physical aperture area / FEB–MAR21 / Complete.

- Milestone: Using FEKO and/or CST electromagnetic (EM) simulators, reduce the physical aperture size of the Koshelev antenna to at least 95% of its original design and show minimal to no variation in the bandwidth, gain and increased aperture efficiency / Complete.

(D) Determine the full-width half-maximum (FWHM) and ringing metrics from the envelope of the time domain impulse response ($h_{rx/tx}(t, \phi, \theta)$) in receive or transmit mode / MAR–APR21 / Complete.

- Milestone: Produce a generalized code that calculates the impulse response envelope of the Koshelev antenna and plots the rate of change in FWHM and ringing values as a function of physical aperture size.

(E) Perform tradespace studies on design parameters such as feed position (*F*), length (*L*), and alpha (α). Obtain various antenna metrics data, compare, and analyze / MAR21/ Complete.

- Milestone: Identify Koshelev antenna design parameters that significantly alter the bandwidth, rE/V, peak gain over the desired bandwidth, and aperture efficiency.

(F) Reduce Koshelev antenna aperture size (H×W) to equal to or less than 90 mm × 90 mm, equal to that of the SOTA BAVA, for direct antenna metrics comparison / MAR–APR21 / Complete.

- Milestone: Provide a recommendation on the optimum design parameters and the resulting metrics, with comparison to SOTA BAVA. The optimized design parameters must yield 900 MHz ± 200 MHz bandwidth, rE/V greater than 1, peak gain around 3 dBi at 900 MHz, aperture efficiency equal to or greater than 130% at 900 MHz.

(G) Using the optimized model from (F), build various array simulation models/topologies to perform a tradespace study and report tradeoffs between array antenna metrics such as center element reflection coefficient (S11) value, gain vs theta at constant phi, physical aperture area, aperture efficiency, and rE/V / MAY–JULY21 / Complete.

- Milestone: Develop/showcase an optimized Koshelev array model that exceeds an aperture efficiency of 130% with a high rE/V.

(H) Perform literature search to investigate, understand, and determine the applicability of special electromagnetic (EM) techniques to the antennas under consideration. / JAN–APR21 / Complete.

(I) Explore impedance taper (microstrip based and coax based) designs that can interface well (both mechanically and electrically) to transition the signal from a coax cable to the input of the Koshelev antenna element / JULY21–AUG21 / Complete.

- Milestone: Recommend the optimum impedance taper design (with minimum reflections and maximum power transfer) with the optimum dimensions to successfully convert the high-voltage, short-rise time input signal from a coax cable to the feed of the Koshelev antenna array.

(J) Study response from optimized Koshelev antenna array when excited with different monopolar, differential, and bipolar pulse signals of significant interest / AUG21–NOV21 / Complete.

- Milestone: Provide a table comparing the Koshelev antenna array response metrics and narrow down the suitable pulse signals. Recommend (if any) changes to the downselected pulse signal(s) that can further improve the radiation efficiency, and/or transient gain.

(K) Investigate and analyze the response from the optimized Koshelev antenna array when excited by different excitation patterns / DEC 21 / Complete.

- Milestone: Compare and recommend an appropriate excitation method to yield maximum boresight gain, maximum half-power beamwidth (HPWB), minimum side lobe levels, and maximum electric field, rE/V.

(L) Prototype single element Koshelev antenna and test for reflection coefficient, gain as a function of frequency, radiated electric field at 1-m, 2.5-m, 5-m and 10-m (if feasible) distances. / AUG21–SEP22 / Partially Complete.

(L1) Fabricate Cu-foil and paint (silver or copper) variants of 3D-printed balanced Koshelev antenna with integrated impedance transformer.

- Milestone: Demonstrate a 3-D printed Koshelev antenna prototype that is cost-effective and lightweight. / AUG21–NOV21 / Complete.

(L2) Perform scattering parameter measurements of Cu-foil and paint variants of 3D-printed prototypes to identify any design and fabrication issues/challenges.

- Milestone: Report fabrication & assembly challenges, test outcomes and identify the source of mismatch (if any) to alleviate reflections. Verify against simulations to validate mismatches. / DEC21–APR22 / Complete.

(L3) Downselect to one variant of the 3-D printed Koshelev antenna prototype and measure frequency domain gain and time-domain electric field at multiple distances.

- Milestone: Experimentally demonstrate a 3D-printed Koshelev antenna with a performance comparable to the standard sheet metal variant of the Koshelev antenna. / MAY22–SEP22/ Complete.

- Milestone: Report performance of 3D printed Koshelev antenna, compare against the performance of balanced antipodal Vivaldi antenna (BAVA), and recommend any overall improvements to the fabrication/prototyping/testing methods.

8.2.3 *Progress Made Since Last Report*

(L3) In the previous month, the 3-D printed Koshelev antenna with a partial dielectric transformer was subjected to free-space gain testing at one of UMKC's testing facilities. Furthermore, we were able to draw a comparison via simulations between the proposed Koshelev antenna model and the SOTA BAVA to satisfy one of the milestones..

8.2.4 *Technical Results*

(L3) The first functional Koshelev antenna with partial dielectric transformer prototype developed in-house at UMKC has been subjected to free-space gain measurements over the frequency range 400 MHz to 6.2 GHz. The transmitting and receiving antenna (MVG SH400) are separated by 4 meters. Fig. 8.2.1 compares the measured and simulated gain results. The four unusual peaks and random oscillations in the measured data in Fig. 8.2.1 can be attributed to undesired reflections from the walls and other metallic objects nearby. The measured gain result demonstrated good agreement with the simulated gain result up until 1.8 GHz. However, beyond 1.8 GHz, the measured data saturated around 10 dBi because the far field condition was not met in the free space beyond 1.8 GHz at a separation distance of 4 meters.

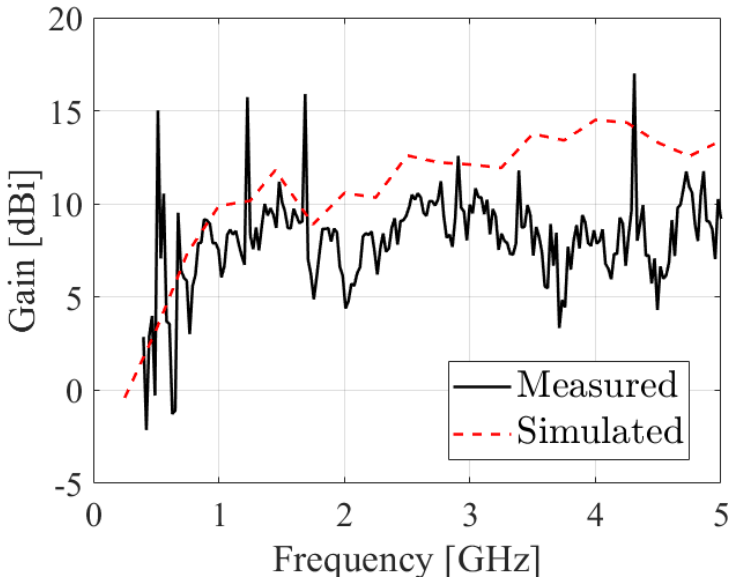

Fig. 8.2.1. Comparison of measured and simulated gain of the Koshelev antenna with partial dielectric transformer.

Table 8.2.1. An EM simulation comparison of metrics of interest between the Koshelev antenna and SOTA BAVA.

		Single Element		4x4 Array	
		BAVA	Koshelev Antenna	BAVA	Koshelev Antenna
Aperture size (H×W) - **cm²**		**12 × 12**	**9.1 × 10**	**63.7 x 63.7**	**55 × 58**
Physical Aperture area (m^2)		**0.0144**	**0.0091**	**0.4058**	**0.3190**
Operating frequency range (fc±BW in MHz)		**900 ± 200**	**900 ± 180**	**950 ± 50**	**900 ± 100**
Peak gain at 900 MHz [dBi]		**3.7**	**4.5**	**14.7**	**15**
Transient Gain (rE/V)		**0.4**	**1.2**	**6.5**	**9.67**
Half-Power (-3 dB) Beamwidth	E-plane	**115°**	**83°**	**26.2°**	**30°**
Aperture Percentage at 900 MHz		**143%**	**243%**	**63%**	**87%**

In addition, we have drawn a comparison between the Koshelev antenna and the SOTA BAVA using some of the important antenna metrics obtained via simulations. Table 8.2.1 demonstrates this comparison between the two antennas for the single element and the 4x4 array configurations. In the case of single element comparison, the proposed Koshelev antenna dominates the SOTA BAVA in all except bandwidth, and steerability (narrow half-power beamwidth value implies narrow steering-angle). The single element Koshelev antenna is significantly smaller in aperture size than the SOTA BAVA while yielding higher transient gain value. In the case of an array, the proposed Koshelev antenna array performs better than the SOTA BAVA in all of the metrics listed.

8.2.5 *Summary of Significant Findings and Mission Impact*

(A) An extensive literature search on various UWB antenna elements has resulted in finding three promising options. The down-selected elements are the Koshelev, Shark, and Fractal antennas, which will be extensively studied using their individual design parameter space, which could result in physical aperture area reduction of the single antenna element. Later, the single antenna element will be converted into a planar array.

(B) Initial validation of the Koshelev antenna simulated using CST software agreed well with the antenna metrics published in the open literature [1]. A UWB bandwidth response (10:1 bandwidth) and rE/V > 1 has been observed from our initial simulations of the Koshelev antenna. This validation ensured that the Koshelev antenna can be subjected to further tradespace studies to understand its performance, followed by optimizing the design according to OSPRES grant requirements.

(C) The initial tradespace study and analysis of the Koshelev antenna design yielded promising outputs to carry forward the investigation. A comparison of important antenna metrics between the Koshelev antenna in [1] and aperture reduced Koshelev antenna are shown in Table 5.2.1 of the APR 21 MSR.

(D) An in-house code has been developed to calculate important UWB time domain antenna metrics such as full-width half maximum (FWHM) and ringing. These metrics have been calculated using in-house MATLAB code using the excitation voltage and radiated electric field information obtained from CST simulations. FWHM and ringing antenna metrics help with assessing or characterizing an antenna's UWB response.

(E) The tradespace study of feed position provided a deeper understanding of how its position impacts the S_{11} value bandwidth. An optimum value for feed position i.e., $F = 1/20 < L < 1/10$ is recommended to achieve maximum bandwidth. The tradespace study of the antenna length (L) is straightforward. A longer antenna length will radiate better at lower frequencies. However, physical size restrictions/requirements must be kept in mind in determining the antenna length. Finally, a larger α value (>120°) is recommended to avoid unnecessary reflections from the electric monopole.

(F) From a thorough tradespace study, the aperture size of the Koshelev antenna (single element) is determined to be 90 mm x 100 mm to achieve desired antenna metrics performance proposed in the milestone. All metrics described in the milestone have

been successfully achieved via simulations except the desired bandwidth (200 MHz on both sides) at 900 MHz center frequency. The bandwidth achieved via simulations is 900 ± 100 MHz.

(G) The physical aperture area of the Koshelev array antenna largely depends on the interelement spacing and the shape of the array. We were able to determine that the diamond topology is the optimum shape and were able to obtain similar gain profile (peak gain and radiation pattern) from turning off certain elements in the array as an active array (all elements in on state). The interelement spacing study revealed that S_y has the least effect on the output; therefore, a smaller spacing value can be chosen to reduce the physical aperture area of the Koshelev array.

(H) A literature search on special EM techniques expanded our knowledge and opened the door to opportunities to apply some of those techniques to the antennas under study. EM techniques such as non-symmetric and non-square array topologies have been applied to the development and study of the Koshelev array antenna.

(I) The first impedance taper design under consideration has shown good S_{11} values (< –10 dB) over the frequency range of interest. In addition, we have shown that the shape of the pulse can be easily retained at the output of the taper with less than 5% amplitude losses.

(J) The Koshelev antenna array response from feeding a monopolar vs bipolar signal has demonstrated that the bipolar signal fed to antenna will radiate at least 10 times better than a monopolar signal. A comparison of the frequency spectrum of the radiated electric field from the optimized Koshelev antenna array between different monopolar pulse sources has identified the ‘MI0731’ pulse to be the optimum pulse.

(K) The optimized Koshelev antenna array was studied for the electric field response under different array excitation patterns. The study determined that the uniform and Gaussian excitation patterns were the optimum excitation patterns. Selecting the uniform or Gaussian excitation pattern would yield the maximum electric field at the boresight for an arbitrary input signal.

(L) The Cu-foil plated 3D printed Koshelev antenna prototype with partial dielectric transformer has shown to yield better RF performance over the silver painted prototype. The reflection coefficient and the measured gain values from the Cu-foil plated prototype agreed with the simulated values at least up to 2 GHz yielding an impedance bandwidth of 1.7 GHz with a measured gain of 8 dBi at 900 MHz. Using simulations, we demonstrated that the proposed Koshelev antenna (as single element and as an array) performs exceedingly well than the SOTA BAVA with few exceptions as listed in Table 8.2.1.

8.2.6 *References*

[1] Gubanov, V. P., et al. "Sources of high-power ultrawideband radiation pulses with a single antenna and a multielement array." *Instruments and Experimental Techniques* 48.3 (2005): 312-320.

[2] S. Zhang, Y. Vardaxoglou, W. Whittow and R. Mittra, "3D-printed graded index lens for RF applications," 2016 International Symposium on Antennas and Propagation (ISAP), 2016, pp. 90-91.

8.3 Machine Learning Inspired Tradespace Analysis of UWB Antenna Arrays

(Sai Indharapu and Kalyan Durbhakula)

8.3.1 *Problem Statement, Approach, and Context*

Primary Problem: Determine the extent to which the physical aperture area of an antenna array, composed of antenna elements, can be reduced while maintaining performance in peak power density, bandwidth, and electronic beam steerability over the UHF range (0.4–1 GHz), compared with present-art high-power-microwave-capable antenna arrays.

Solution Space: Fractal antennas possess exceptional fidelity factor values (>0.9), which describe how well the shape of the input pulse is retained at an observation point in the far-field. Their high degree of freedom provides an opportunity to develop systematically modified patch shapes, which in turn leads to improved bandwidth while retaining high fidelity factor values. Machine learning (ML) can be leveraged to predict the antenna array response for an arbitrary design parameter space upon sufficient training and validation.

Sub-Problem:

(i) Fractal antennas generate omni-directional radiation patterns in the H-plane over the desired frequency range.

(ii) ML can suffer from underfitting or overfitting the training model which in turn leads to deviations in the predicted output.

State-of-the-Art (SOTA): Conventional full-wave EM solvers such as method of moments (MoM), multi-level fast multipole method (MLFMM), finite element method (FEM), and finite difference time domain (FDTD) method are currently being used to study, analyze and assess the performance of UWB antennas.

Deficiency in the SOTA: UWB antenna optimization using conventional EM solvers utilizes significant computational time and memory resource.

Solution Proposed:

(i) Design, simulate, validate, and perform a tradespace study on the design parameter space of the selected fractal antenna element using commercially available electromagnetic (EM) wave solvers.

(ii) Train, validate, test, and compare multiple ML models for quicker and accurate prediction of antenna array response for different physical aperture areas.

Relevance to OSPRES Grant Objective: The fractal antenna achieves an UWB response, a mandatory requirement of the OSPRES grant objective, in a small volume footprint and similar physical aperture area when compared against the SOTA BAVA, dual ridge horn antennas etc. Furthermore, the microstrip-design-based fractal antenna can efficiently handle electronic steering by integrating the feed network on the same board. This eliminates the need to build a separate feed network external to the fractal antenna using bulky coaxial cables.

Risks, Payoffs, and Challenges:

(i) A majority of the fractal antenna geometries yield an omni-directional pattern in the H-plane, which can be a risk. However, efforts are underway to mitigate this pattern without deteriorating bandwidth.

(ii) Payoffs include developing a library of antenna metrics data for various fractal shapes and sizes.

(iii) Design challenges and numerical calculations with respect to specific fractal shapes could arise after performing a certain number of iterations to further improve the bandwidth.

(iv) Fractal antennas were known to generate gain loss at random frequencies over their operating frequencies. Achieving gain stability over the desired frequency range can be a significant challenge.

8.3.2 *Tasks and Milestones / Timeline / Status*

(A) Perform tradespace analysis of the fractal element radius *b* over the desired frequency range (4 to 12 GHz) using the genetic algorithm (GA) optimization tool available in the commercial electromagnetic (EM) solver FEKO / FEB21 / Complete.

- Milestone: Provide a recommendation of an optimum value of *b* using OPTFEKO to minimize reflection coefficient (S_{11}) (< –10 dB).

(B) Perform tradespace study on different fractal shapes by changing the number of fractal segments to understand the effect of this change on the impedance bandwidth / FEB21 / Complete.

- Milestone: Produce a detailed study of the antenna response such as S_{11}, gain, and bandwidth by varying the number of fractal segments.

(C) Apply the GA optimization tool on the fractal side length *b* over a wide frequency range (2 to 12 GHz with 201 discrete frequency points) and number of fractal segments using OPTFEKO on the LEWIS cluster / MAR21 / Complete.

- Milestone: Reduce physical aperture area by 10% of its present design, reported in the FEB MSR, and demonstrate minimal or no change in S_{11}, gain, and fidelity factor values.

(D) Perform a parametric study and analysis of antenna response by varying hexagon radius, *a* / MAR–APR21 / Complete.

- Milestone: Recommend a value of *a* to reduce the physical aperture area and increase aperture efficiency (>50%) with no variation in other antenna metrics.

(E) Frequency scale fractal antenna design such that the center frequency of the resulting antenna equals 1.3 GHz / MAY21 / Complete.

- Milestone: Modify antenna design with a center frequency equal to 1.3 GHz and achieve similar results (3:1 bandwidth at fc = 1.3 GHz, 3 dBi gain and >130% aperture efficiency at 900 MHz) to antenna design at center frequency ~7 GHz.

(F) Design and simulate various array antenna geometries composed of optimized fractal antenna elements (obtained from (E)) to analyze the effect of overall array antenna

geometry on the desired array antenna response metrics (i.e., gain vs. frequency, gain vs. elevation angle at constant phi, rE/V, half-power beamwidth and side-lobe level.) / MAY–JUL21 / Complete

- Milestone: Recommend a best possible structure with reduced aperture area and minimal loss in gain.

(G) Apply ML models available in Altair Hyperstudy (2021) on the fractal antenna to try and understand the possibilities and limitations of ML models for fast and efficient antenna metrics prediction and optimization. Expand the prediction capability to time-domain electric field and antenna pattern using ML models (k-nearest neighbor and linear regression) available in scikit learn on Python programming tool “Anaconda”. / MAY21–FEB22 / Complete.

- Milestone: Recommend most accurate and efficient ML model for a fractal antenna in time-domain and frequency domain.

(H) Apply ML models on the octagon fractal antenna array lattice to extend the prediction capability beyond single element / SEP21–MAY22 / Complete.

- Milestone: Recommend the best suitable ML model implemented/developed using Python programming language for array antenna metrics prediction.

(I) Develop, validate, and demonstrate a graphical user interface (GUI) to automate the process of employing ML models to predict the antenna output response/ FEB22–SEP22 / Complete.

- Milestone: Incorporate the developed automated data extraction scripts, ML scripts to the GUI to enable user to predict antenna response 100x faster than full wave solvers.

8.3.3 *Progress Made Since Last Report*

(I) In the last MSR, we demonstrated the ML-based GUI’s ability to successfully predict antenna array metrics such as reflection coefficient (S_{11}), gain vs frequency, and radiation pattern. To complete the efforts mentioned in (I), the kNN model available in the GUI was trained to predict the electric(E)-field response. A total of 18 different training data samples were generated from the antenna array design using CST Studio Suite. Each training data sample has an input (i.e., antenna array design variables) and an output (corresponding E-field response).

8.3.4 *Technical Results*

(I) For S_{11} and gain response prediction of a fractal antenna array, a training data size of 18 was used with six input parameters: “hexagonal patch side length *a*”, “fractal side length *b*”, “distance between patch center and fractal center *d*”, “distance between top ground plane and the transmission line *gap*”, "inter element spacing between antenna elements in an array *IEx* (in x-axis) and ‘*IEy*’ (in the y-axis)”. Following the training, the trained kNN model was used to predict E-field response for an unseen test input. The change in value of *k* had negative impact on the predictions and the RMSE. So, the number of neighbors *k* was set to 1. Finally, the predicted output is illustrated in Fig 8.3.1.

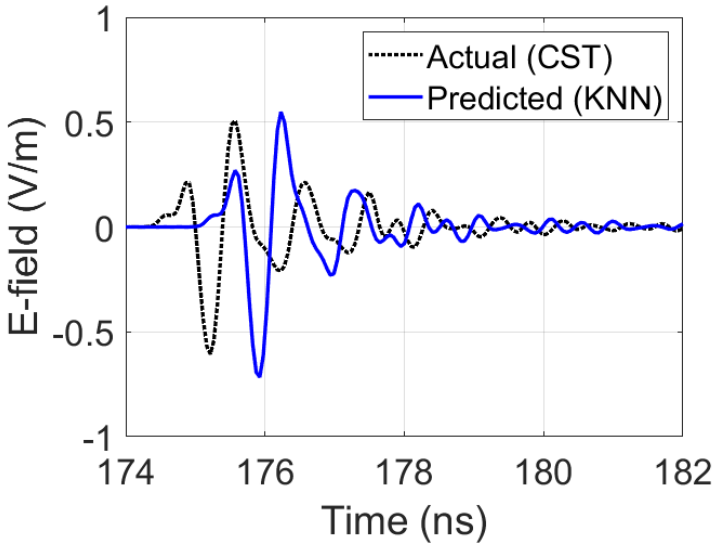

Fig 8.3.1. Comparison of predicted and actual E-field response of an antenna array.

From Fig 8.3.1, the predicted response from the kNN model looks shifted along the axis towards the right. The shift in the response from the predicted model is due to inconsistency in the E-field sampling interval for each output calculation. However, this can be fixed by data pre-processing. That is, interpolating E-field with respect to time for each combination in training with a fixed sampling rate. Further, the kNN predicted output is moved (13 ns) towards the negative x-axis and compared with the actual E-field response in Fig 8.3.2.

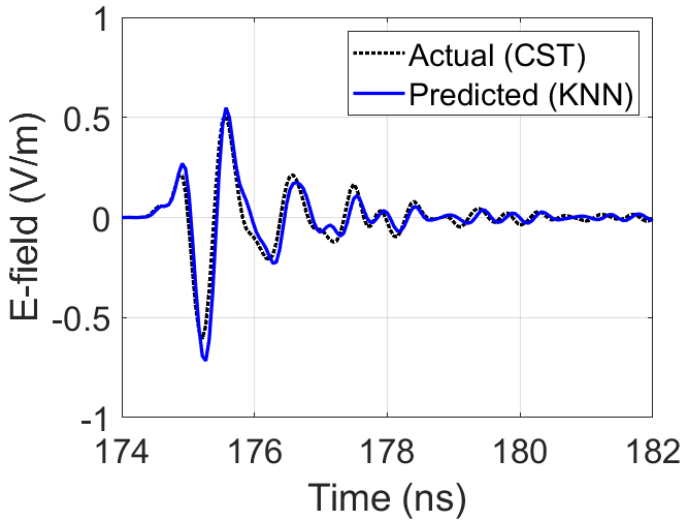

Fig 8.3.2. Comparison of time-shifted kNN prediction with actual E-field response of an antenna array.

With this effort, the GUI was validated for S_{11}, gain, radiation pattern, and electric field response predictions for a single element and an array with more than 100x faster response calculation than conventional EM solvers.

Table 8.3.1. Comparison of various computational resources and RMSE for conventional and GUI-based ML approaches.

	Conventional approach	GUI-based ML approach
Antenna response calculations	Using frequency domain solver in CST studio suite	Using trained kNN model
Computational time (fractal antenna array)	~90 min	<1 sec*
RMSE	0	0.043

*Does not include time utilized to generate training data.

8.3.5 *Summary of Significant Findings and Mission Impact*

(A) We carried out an effort to identify the dominant fractal antenna design parameter and its corresponding value using parameter study and FEKO optimization tool. It was found that the side length '*b*' of the fractal elements plays a significant role in determining the antenna bandwidth. The initial analysis of the simulation results with fractal radius *b* equal to 1.8 mm yielded multiple resonant frequencies with enhanced bandwidth. To further increase the bandwidth, OPTFEKO was used as an optimization tool with fractal radius *b* as the optimization variable. Finally, the optimum value for *b* that minimizes the S_{11} (-10 dB) was found to be 1.66 mm.

(B) The addition of fractal elements (*N*) to the simple hexagon improved antenna metrics such as reflection coefficient (S_{11}). To further investigate and understand the fractal elements, the number of segments (sides of the fractal element) in the fractal geometry were varied within the range of 6 to 14. The resultant S_{11} response had positive impact (improving bandwidth) at higher frequencies and negative impact (decreasing bandwidth) at lower frequencies. Therefore, the number of segments of the fractal element was chosen to be 6 as it has better balance of S_{11} values both at lower and higher frequencies.

(C) The initial optimum value of *b* over 51 discrete frequency points was reported as 1.66 mm in task (A). To further increase the accuracy of the optimization algorithm and to find a more precise value for *b*, optimization was further performed over a wider frequency values (201 discrete points between 2 and 12 GHz), which yielded an optimum value of *b* as 1.37 mm. The S_{11} response of the antenna design with this newly obtained *b* parameter (i.e., 1.37 mm) did not produced any better bandwidth compared to *b* = 1.66 mm. Thus, *b* was set to be 1.66 mm for further research.

(D) The hexagonal patch radius *a* has a significant effect on the physical aperture area of the antenna. Therefore, Altair OPTFEKO has been utilized to find an optimum *a* value, which was determined to be 8.0 mm over the range 7.2 to 9.0 mm. Antenna metrics such as S_{11}, gain, and bandwidth have shown desired performance with the optimized *a* value.

(E) The initial antenna design has been modified from a center frequency $(f_c) = 7\ GHz$ to achieve a center frequency $(f_c) = 1.3\ GHz$. The gain value at 900 MHz is 3.5 dBi and, with the modified antenna design, we were able to achieve an impedance bandwidth ratio of 3.3:1. The designed antenna has been fabricated and tested, and the S_{11} response of the fabricated antenna agrees well when compared against FEKO, CST.

(F) Four different fractal antenna array geometries (i.e., square, diamond, hexagon, and octagon) have been designed and simulated. Upon comparing antenna array metrics, the octagonal fractal antenna array has yielded minimal sidelobe levels with a gain of 15.7 dBi at 900 MHz, close to that of the square geometry but with 32.2% lower physical aperture area. The octagonal fractal antenna array has been chosen as the optimum geometry with reduced aperture area and reduced side lobes while retaining the bandwidth and gain milestone metrics.

(G) The ML models available in Altair Hyperstudy (radial basis function (RBF), least square regression (LSR), and hyper kriging (HK)) were employed and evaluated to predict the output response of a fractal antenna. RBF and LSR were down selected from the initial three ML models based upon the aforementioned evaluation. RBF performed well in the prediction of S_{11}, while LSR performed slightly better for gain and electric field predictions. In addition, for time-domain electric field prediction, we recommend usingthe kNN ML algorithm for accurate prediction.

(H) The initial application of the kNN ML model for the prediction of antenna array bandwidth response of center and corner element yielded positive results. The new LR ML model yielded improved RMSE values (over kNN) in its prediction of reflection coefficient (27.8% less RMSE for center element and 19.7% less RMSE for corner element). On the other hand, the RMSE values for gain (as function of theta) prediction using LR ML model has 55.5% increase over kNN prediction. Finally, kNN provides better generalization to predict reflection coefficient, whereas LR provides better generalization to predict frequency domain gain in the case of a fractal antenna array. On the other hand, the application of the antenna element pattern (AEP) method for antenna array was put on hold due to its limitations.

(I) A GUI was developed to handle antenna response prediction of an antenna element and an antenna array geometry. The GUI requires training data for an antenna (single-element or array) of user choice and predicts the desired antenna output response (S_{11}, antenna gain, radiation pattern, electric field) for a range of test data within a few seconds. The GUI has been configured to perform parametric sweep analysis for S_{11} and gain, electric field, radiation pattern response outputs for the fractal antenna design. Based on feedback/suggestions received from other in-house researchers, key features such as data comparison plot, error calculation, data exporting, and antenna array analysis were added to the GUI. Furthermore, the antenna array analysis option was able to display the most efficient input combination

for which the antenna array has less physical aperture area and high gain. Finally, the RMSE values for the predict outputs (i.e., S_{11} and gain, electric field, radiation pattern) of an antenna array were close to 0 and the computational time was reduced from 90 mins to less than 1 sec for a single simulation.

8.3.6 *References*

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9 Feedback

There is no feedback to report for the current reporting period.

10 Program Management

10.1 Issues

i. Scope – No issues
ii. Budget – 12-month NCTE submitted/pending
iii. Schedule – No issues

10.2 Interactions with Others

Agency/Org	Performer	Project Name	Purpose of Research/ Collaboration

10.3 Major Procurement Actions

10.4 Travel

Destination	Purpose	Attendees	Estimated Costs

10.5 Pending or Upcoming Public Release Requests

11 Appendix A: Academic and IP Output

11.1 Students Graduated

Name	Degree	Last Known
Al-Shaikhli, Waleed	MS Spring 20	Genuen, KS; Cognitive Copper, KS
Alsultan, Khulud	PhD Spring 21	King Saud University, Saudi Arabia
Azad, Wasekul	PhD Summer 21	Applied Materials, Sunnyvale, CA
Berg, Jordan	MS Spring 21	MRI Global, MO
Bhamidipati, John	PhD Spring 22	Intel, NM
Bissen, Bear	MS Spring 19	Capella Space, San Francisco, CA
Bozarth, Ethan	BS 21	
Brasel, Sadie	BS Spring 21	Graduate Student, Rice University, TX
Clark, Justin	BS 22	MRI Global, MO
Dowell, Alexander	BS Spring 22	Graduate Student, UMKC
Fazekas, Max	MS Summer 21	
Floyd, Dennis	BS	Naval Air Warfare Center Weapons Division
Fry, Spencer	BS Spring 2021	Garmin, KS
Hamdalla, Mohamed	PhD Fall 21	MIDE, MO
Hanif, Abu	PhD Spring 21	Intel Corporation, OR
Harmon, Aaron	BS 18	PhD Student, Missouri Univ. of Science & Tech.
Harp, Joshua	MS 19	Small Business
Hauptman, Cash	BS Spring 18	University of Nebraska-Lincoln
Herrington Shawn	PhD Summer 21	Honeywell Aerospace, NM
Karnes, Simeon	BS Spring 21	Graduate Student, UMKC
Klappa, Paul	MS Spring 21	Sierra Nevada Corporation, NV
Kovarik, James	MS Spring 21	
Kramer, Noah	MS Spring 19	MIDE, MO
Labrada, Dario	BS Spring 20	Honeywell Aerospace, FL
Lancaster, John	MS Spring 17	Lawrence Livermore National Laboratory, CA
Landwehr, Colby	BS Fall 21	Burns & McDonnell
Reed, Demetri	BS Spring 22	Evergy, MO
Renzelman, Jeff	MS Spring 18	Sensata Technologies, MA
Roy, Sourov	PhD Spring 21	BTCPower, Orange County, CA
Smith, Cody	BS 20, MS 21	Winchester Ammunition, MO
Thompson, Heather	MS 20	University of Missouri-Kansas City, MO
Wagner, Adam	MS Fall 20	Los Alamos National Laboratory, NM
Utt, Anthony	BS	
Xia, Shengxuan	BS	PhD Student, Missouri Univ. of Science & Tech.

11.2 Journal Publications

11.2.1 *In Preparation*

[1] G. Bhattarai et al., "Optimizing Multi-Stacked Nanosecond DSRD-Based Pulser: Theory, Simulation, and Experiment," *IEEE Transactions in Power Electronics*, **2022**.

[2] M. Hamdalla, V. Khilkevich, D. G. Beetner, A. N. Caruso, A. M. Hassan, "Characteristic Mode Analysis Justification of the Stochastic Electromagnetic Field Coupling to Randomly Shaped Wires," *IEEE Transactions on Electromagnetic Compatibility*, In Preparation, **2022**.

[3] S. S. Indharapu, A. N. Caruso, K. C. Durbhakula, "Machine Learning Assisted Antenna Design Optimization of UWB Fractal Antenna," TBD, In Preparation, **2022**.

[4] J. K. P Bhamidipati, G. Bhattarai, A. N. Caruso, "Effect of Proton Irradiation Induced Localized Defect/Trap Clusters on Silicon Photoconductive Semiconductor Switch (Si-PCSS) Recovery Time and Leakage currents," *Solid-State Electronics,* In Preparation, **2022**.

[5] N. Gardner, K. C. Durbhakula, and A. N. Caruso, "UHF and L-Band Frequency Generation at MW Peak Power using Diode-based Nonlinear Transmission Lines as Pulse Forming Networks," *Transactions on Plasma Science*, In Preparation, **2022**.

[6] N. Gardner, K. C. Durbhakula, and A. N. Caruso, "Electrically Tunable Diode-based Nonlinear Transmission Line," *TBD*, In Preparation, **2022**.

[7] B. Barman, D. Chatterjee, and A. N. Caruso, "Design and Analysis of a Class of Wideband, Electrically Small, Microstrip Patch Antenna Elements for Phased Array Applications," *IEEE Antennas and Propagation Magazine,* In preparation, **2022**.

11.2.2 *Submitted / Under Revision*

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[9] E. W. Gasta, E. D. Krulewich, M. A. Mardikes, N. S. Petersen, A. H. Stark, T. D. Fields, and R. B. Hoffman, "Surface and Airborne HPM Effector Capabilities Realized by Computational Wargaming," *Journal of Defense Research and Engineering*, Submitted May 27, **2022**.

[10] J. K. P. Bhamidipati, E. R. Myers, A. M. Conway, L. F. Voss, M. M. Paquette, and A. N. Caruso, "Figure of Merit Development for Linear-Mode Photoconductive Solid-State Switches," *IEEE Journal of the Electron Devices Society*, Submitted May 1 **2022**, Manuscript ID#JEDS-2022-05-0136-R.

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Electronics and Communications, Submitted March 6 **2022**, Manuscript ID#AEUE-S-22-01270.

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11.2.3 *Published / In Press*

[13] M. Z. M. Hamdalla, A. N. Caruso, and A. M. Hassan, "Electromagnetic Compatibility Analysis of Quadcopter UAVs Using the Equivalent Circuit Approach," *IEEE Open Journal of Antennas and Propagation*, vol. 3, pp. 1090-1101, **Sept 2022** [doi].

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11.3 Conference Publications

11.3.1 *Submitted / Accepted*

[1] S. Bellinger, A. Caruso, and A. Usenko, “Stacked Diodes for Pulsed Power Applications: New Process Integration Scheme,” *GOMACTech*, San Diego, CA, March 20-23, **2023**.

11.3.2 *Presented*

[2] A. Usenko, A Caruso, S. Bellinger, S. Dhungana, and R. Allen, “Adopting Processes from Mainstream Silicon Technology to Discrete Power Devices Technology,” *2nd Annual Workshop on Solid State Devices and Applications for Directed Energy at GE Research*, Niskayuna, NY, October 26-28 **2022**.

[3] A. Usenko, S. Dhungana, A. N. Caruso and S. L. Bellinger, “Electroless Nickel Plating for Ohmic Contacts to Silicon Power Devices,” *Abstracts of 242nd Electrochemical Society Meeting*, Atlanta, GA, October 9-13, **2022**.

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[7] S. S. Indharapu, A. N. Caruso, and K. C. Durbhakula, "Supervised Machine Learning Model for Accurate Output Prediction of Various Antenna Designs," *2022 IEEE International Symposium on Antennas and Propagation and USNC-URSI Radio Science Meeting (AP-S/URSI)*, Denver, Colorado, USA, July 10-15, **2022**, pp. 495-496 [doi].

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[11] B. Bissen, T. Ory, M. Z. M. Hamdalla, A. M. Hassan, A. N. Caruso, *"*An Automated Experiment for Parametric Investigation of Voltage Stacking Behavior*," IEEE International Symposium on Antennas and Propagation and USNC-URSI Radio Science Meeting*, Singapore, December 4-10, **2021**, pp. 605-606 [doi].

[12] M. Z. M. Hamdalla, A. N. Caruso, A. M. Hassan *"*Predicting RF Coupling to a UAV Wiring System Using the Equivalent Circuit Approach*," IEEE International Symposium on Antennas and Propagation and USNC-URSI Radio Science Meeting*, Singapore, December 4-10, **2021**, pp. 1091-1092 [doi].

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[45] M. Hamdalla, A. M. Hassan, and A. N. Caruso "Characteristic Mode Analysis of Unmanned Aerial Vehicles with Realistic Shapes and Material Composition," *IEEE International Symposium on Antennas and Propagation and USNC-URSI Radio Science Meeting,* Boston, MA, July 8-13, **2018**.

[46] W. Azad, S. Roy, A. S. Imtiaz, and F. Khan, "Microelectromechanical System (MEMS) Resonator: A New Element in Power Converter Circuits Featuring Reduced EMI," *2018 International Power Electronics Conference (IPEC-Niigata 2018-ECCE Asia)*, Niigata, May 20-24, **2018**, pp. 2416-2420 [doi].

11.4 Conference Presentations

11.4.1 *Submitted / Accepted*

[1] S. Bellinger, A. Caruso, and A. Usenko, "Stacked Diodes for Pulsed Power Applications: New Process Integration Scheme" *GOMACTech* 2023, San Diego, CA, USA, March 20-23 **2023** (*submitted*).

[2] A. Usenko, A. Caruso, S. Bellinger, S. Dhungana, R. Allen, "Adopting Processes from Mainstream Silicon Technology to Discrete Power Devices Technology" *2nd Annual Workshop on Solid State Devices and Applications for Directed Energy at GE Research*, Niskayuna, NY, October 26-28 **2022** (*submitted*).

11.4.2 *Presented*

[3] S. Sisk and S. Sobhansarbandi, "In-Chip Cooling Technology within Semiconductor Switches," *UMKC SUROP Symposium*, Kansas City, MO, Sept **2022** (poster).

[4] S. Bellinger, A. Caruso, A. Usenko, "New Paradigm on Making Semiconductor Opening Switches for Pulsed Power," *2021 23rd IEEE Pulsed Power Conference*, Denver, CO, Dec. 12–16, **2021** (oral, virtual).

Directed Energy Professional Society, Directed Energy Systems Symposium, Washington DC, October 25-29 **2021**:

[5] B. Barman, D. Chatterjee, A. Caruso, and K. Durbhakula, "Tradespace Analysis of a Phased Array of Microstrip Patch Electrically Small Antennas (ESAs)" (Poster)

[6] J. N. Berg, R. C. Allen, and S. Sobhansarbandi, "A Novel Method of Cooling a Semiconductor Device through a Jet Impingement Thermal Management System: CFD Modeling and Experimental Evaluation" (Poster)

[7] J. N. Berg, R. C. Allen, and S. Sobhansarbandi, "Heat Transfer Enhancement of a Jet Impingement Thermal Management System: A Comparison of Various Nanofluid Mixtures" (Poster)

[8] J. Bhamidipati, M. Paquette, R. Allen, and A. Caruso, "Photoconductive Semiconductor Switch Enabled Multi-Stage Optical Source Driver" (Poster)

[9] G. Bhattarai, J. Eifler, S. Roy, M. Hyde, J. Bhamidipati, A. Usenko, M. Pederson, M. Paquette, A. Caruso, S. Bellinger, L. Voss, and R. Allen, "All Solid-State High-Power Pulse Sharpeners" (Poster)

[10] S. Brasel, K. Norris, R. Allen, A. Caruso, and K. Durbhakula, "Efforts to Reduce Physical Aperture Area of Ultra-Wideband Arrays" (Poster)

[11] A Caruso, "ONR Short Pulse Research and Evaluation for c-sUAV: Supporting and Sub-Programs Overview" (Oral)

[12] J. Clark, R. C. Allen, and S. Sobhansarbandi, "Ultra-Compact Integrated Cooling System Development" (Poster)

[13] J. Eifler, S. Roy, M. Hyde, G. Bhattarai, J. Bhamidipati, A. Usenko, M. Pederson, M. Paquette, A. Caruso, S. Bellinger, L. Voss, and R. Allen, “TCAD Optimization of Epitaxially Grown Drift-Step Recovery Diodes and Pulser Performance” (Poster)

[14] N. Gardner, M. Paquette, and A. Caruso, “Diode-Based Nonlinear Transmission Lines Capable of GHz Frequency Generation at Single MW Peak Powers” (Poster)

[15] M. Hamdalla, A. Caruso, and A. Hassan, “The Shielding Effectiveness of UAV Frames to External RF Interference” (Poster)

[16] M. Hamdalla, A. Caruso, and A. Hassan, “A Predictive-Package for Electromagnetic Coupling to Nonlinear-Electronics using Equivalent-Circuits and Characteristic-Modes (PECNEC)” (Poster)

[17] M. Hyde, J. Eifler, S. Roy, G. Bhattarai, A. Usenko, M. Paquette, A. Caruso, S. Bellinger, L. Voss, and R. Allen, “Development of an Evaluation Network for Drift Step Recovered Diodes through and Augmented Design of Experiment” (Poster)

[18] S. Indharapu, A. Caruso, and K. Durbhakula, “Machine Learning Based Ultra-Wideband Antenna Array Optimization and Prediction” (Poster)

[19] F. Khan, W. Azad, and A. Caruso, “A Scalable Multilevel-Modular 10 kV Silicon Carbide MOSFET Architecture for Pulsed Power Applications” (Poster)

[20] D. F. Noor, J. Eifler, M. Hyde, G. Bhattarai, S. Roy, J. Bhamidipati, A. Usenko, M. Pederson, M. Paquette, A. Caruso, S. Bellinger, L. Voss, and R. Allen, “DSRD-IES Pulsed-Power Generator Topology Study Using Machine-Learning-Based Feature Selection Optimization and Predictive Learning” (Poster)

[21] S. Roy, J. Eifler, M. Hyde, G. Bhattarai, D. Noor, J. Bhamidipati, A. Usenko, M. Pederson, M. Paquette, A. Caruso, S. Bellinger, L. Voss, and R. Allen, “Systematic Topological Optimization of DSRD-Based IES Pulse Generator” (Poster)

[22] S. Shepard and A. Caruso, “Tubular Core Optical Power Amplifier” (Poster)

[23] H. Thompson, M. Paquette, and A. Caruso, “Minimizing On-State Resistance in GaN:X Photoconductive Semiconductor Switches (PCSSs) for Direct Modulation” (Poster)

[24] A. Usenko, J. Eifler, S. Roy, G. Bhattarai, M. Hyde, M. Paquette, A. Caruso, S. Bellinger, L. Voss, and R. Allen, “New Paradigm in Fabrication of Semiconductor Opening Switches for Pulsed Power” (Poster)

[25] J. Harp, A. Caruso, T. Fields, R. Allen, M. Paquette, A. Hassan, J. Currie, N. Kramer, T. Ory, B. Bissen, K. Durbhakula, “Short Pulse Research and Evaluation for sUAS (OSPRES): Program Update”

[26] J. Harp, A. Caruso, T. Fields, R. Allen, J. Currie, N. Kramer, B. Bissen, R. Butler, S. Karnes, S. Herrington, C. Smith, D. Reed, P. Klappa, P. Meyerhoffer, Z. Drikas, M. McQuage, C. Hoshor, B. Grady, J. Lancaster, “OSPRES cUAS Effects Summary”

[27] J. Harp, N. Kramer, T. Ory, and A. Caruso, “Coaxial Ringdown Oscillator (CRO)”

[28] M. S. Richman, N. Petersen, J. Harp, A. Norris, and T. D. Fields, "Fixed HPM Effector Capabilities Realized Through Computational Wargaming"

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[29] S. Bellinger, A. Caruso, A. Usenko, "Stacked Diodes for Pulsed Power Applications: New Process Integration Scheme," *240th Electrochemical Society Meeting*, Orlando, FL, Oct. 10–14, **2021** (oral).

[30] J. Clark and S. Sobhansarbandi, "Ultra-Compact Integrated Product Cooling Technology," *UMKC SUROP Symposium*, Kansas City, MO, Sept **2021** (poster).

[31] S. R. Shepard and H. A. Thompson, "Self-focusing in Guided and Un-guided Media," submitted to the *2021 OSA Nonlinear Optics Topical Meeting, Virtual Event*, August 9-13, **2021** (oral).

[32] W. Azad, S. Roy, and F. Khan, "A Four-State Capacitively Coupled High-Voltage Switch Powered by a Single Gate Driver," *47th IEEE Conference on Plasma Science*, Singapore, December 6-10, **2020** (oral).

[33] J. Hunter, S. Xia, A. Harmon, A. Hassan, V. Khilkevich, and D. Beetner, "Simulation-Driven Statistical Characterization of Electromagnetic Coupling to UAVS," *Annual Directed Energy Science and Technology Symposium*, March **2020** (abstract appeared, but talk cancelled due to pandemic).

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Directed Energy Professional Society, Annual Directed Energy Science and Technology Symposium, West Point, NY, March 9-13 **2020**:

[34] W. Spaeth, J. Kovarik, R. Allen, S. Fry, B. Bissen, E. Myers, and A. Caruso, "Wideband Parallel Plate to Coaxial Cable Taper"

[35] S. C. Wagner, J. E. Currie, E. R. Myers, and A. N. Caruso, "Quickly Determining Minimum HPC Source Requirements Using Binary Search"

[36] D. Labrada, N. Flippin, and A. N. Caruso, "Rapid Prototyping Nanosecond Pulse Drivers Based on Drift Step Recovery Diode"

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Government Microcircuit Applications & Critical Technology Conference (GOMAC Tech), Albuquerque, NM, March 25-28 **2019**:

[37] C. Hauptmann, J. Bhamidipati, E. R. Myers, S. Bellinger, and A. N. Caruso, "Reduced Recovery Time in SiPCSS Photoconductive Switches"

[38] E. Myers, J. Bhamidipati, C. Hauptmann, S. Bellinger, A. Conway, and A. N. Caruso, "Picosecond High Power Switching Technologies"

[39] H. Thompson, N. Kramer, E. R. Myers, J. Crow, A. Khoeler, and A. N. Caruso, "GaN Optimization for Use in Photoconductive Switch"

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[28] B. Barman, D. Chatterjee, and A. N. Caruso, “Analytical Models for L-Probe fed Microstrip Antennas,” *Proceedings of the IEEE Antennas and Propagation International Symposium and National Radio Science Meeting*, Atlanta, Georgia, USA, July 7-12, **2019** (1 page URSI Abstract).

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Directed Energy Professional Society (DEPS) Annual Directed Energy Science and Technology Symposium, Destin, Florida, USA, April 8-12 **2019**:

[29] R. Butler, A. Gantt, and E. R. Myers, “Mechanical Challenges of Modular Photoconductive Semiconductor Based HPM Sources”

[30] S. Young, M. Richman, J. Bhamidipati, S. Fry, J. Crow, E. Myers, and A. Caruso, “Two-Dimensional Optoelectronic Pulsed Power Switches: Initial Effort”

[31] A. Wagner, J. Lancaster, E. Myers, and A. Caruso, “Rapid Cost Effective RF Component Prototyping Using 3D Printers”

[32] H. A. Thompson, N. J. Kramer, A. Utt, J. Crow, E. R. Myers, A. D. Koehler, and A. N. Caruso, “Cost-to-benefit analysis of GaN for Photoconductive Semiconductor Switches (PCSS)”

[33] C. D. Landwehr, S. Fry, J. Scully, S. Bellinger, E. R. Myers, and A. N. Caruso, “Low Leakage Electroluminescence For Improving SiPCSS Hold Off”

[34] J. Kovarik, B. Barman, D. Chatterjee, and A. N. Caruso, “Some Investigations Into Applications Of Electrically Small Antennas As Phased Array Elements”

[35] S. R. Fry, E. R. Myers, S. L. Bellinger, and A. N. Caruso, “Maximizing SiPCSS Efficiency For HPM Sources”

[36] D. Chatterjee, B. Barman, J. Kovarik, and A. N. Caruso, “Studies On Antenna Characterization And Propagation Of High Power Pulsed Electromagnetic Waves With Minimal Spatial Dispersion”

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Directed Energy Professional Society (DEPS) Annual Science and Technology Symposium, Oxnard, CA, Feb 26-March 2, **2018**:

[37] J. Scully, N. J. Kramer, P. Doynov, N. M. Flippin, E. Cash, S. Kovaleski, E. R. Myers, and A. N. Caruso, “Photo- and Electro-Luminescence Studies of Silicon-Based Photo-Switches”

[38] C. Hauptmann, E. R. Myers, A. N. Caruso, J. B. Newhook, J. Verzella, S. L. Bellinger, and P. G. Doynov, “Thermal Analysis of a PCSS through TCAD Simulation”

[39] N. Flippin, E. R. Myers, and A. N. Caruso, “Fast Rise Time Switches: Drift Step Recovery Diode”

[40] J. Hunter, Y. Liu, D. Floyd, A. Hassan, V. Khilkevich, and D. Beetner, “Characterization of the Electromagnetic Coupling to UAVs”

[41] E. R. Myers, N. J. Kramer, P. Doynov, N. Flippin, J. Scully, E. Cash, S. Kovaleski, J. Beaudin, S. Bellinger, and A. N. Caruso, “High Power and Electronically Steerable Compact Phased Arrays: Design Considerations”

[42] N. Kramer, A. Koehler, T. Anderson, K. Hobart, F. Kub, S. Bellinger, B. Montag, J. Mcgeehan, Y. Morel, P. Doynov, C. Hauptmann, E. Myers, and A. Caruso, “Carbon Compensated Gallium Nitride for PCSS Applications”

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Directed Energy Professional Society (DEPS) Annual Science and Technology Symposium, Huntsville, AL, February 13-17 **2017**:

[43] N. Kramer, S. Bellinger, B. W. Montag, J. E. McGeehan, Y. C. Morel, and A. N. Caruso, “Recent Results of Silicon Based Photoconductive Solid State Switches for 500kHz Continuous Pulse Repetition Frequency.”

11.5 Theses and Dissertations

[1] John Keerthi Paul Bhamidipati, “Pulse Generation, Shaping, and Optimization Solutions for Solid-State-Switch-Enabled High-Power Microwave Generation Systems” PhD Dissertation in Physics and Electrical Engineering, UMKC, **2022**.

[2] Mohamed Hamdalla, “RF Coupling to Realistic Wire Systems in Complex Environments,” PhD Dissertation in Electrical Engineering, UMKC, **2021**.

[3] Khulud AlSultan, “Scalable Acceleration of The Characteristic Mode Analysis Computational Toolbox Using Big Data Techniques,” PhD Dissertation in Computer Science and Electrical Engineering, UMKC, **2021** [mospace].

[4] Jordan N. Berg, “Development of a Jet Impingement Thermal Management System for a Semiconductor Device with the Implementation of Dielectric Nanofluids,” MS Thesis in Mechanical Engineering, University of Missouri-Kansas City, **2021** [mospace].

[5] James C. Kovarik, “Wideband High-Power Transmission Line Pulse Transformers,” MS Thesis in Electrical Engineering, UMKC, **2021** [mospace].

[6] Wasekul Azad, “Development of Pulsed Power Sources Using Self-Sustaining Nonlinear Transmission Lines and High-Voltage Solid-State Switches,” PhD Dissertation in Electrical Engineering, UMKC, **2021** [mospace].

[7] Paul Klappa, “Implementation and Assessment of State Estimation Algorithms in Simulation and Real-World Applications,” MS Thesis in Mechanical Engineering, UMKC, **2021** [mospace].

[8] Shawn Herrington, “Toward a Framework for Systematically Categorizing Future UAS Threat Space,” PhD Dissertation in Electrical and Computer Engineering, UMKC, **2021** [mospace].

[9] Waleed Al-Shaikhli, “Numerical Analysis of Helical And Log-Periodic Antennas For Short Pulse Applications,” MS Thesis in Electrical Engineering, UMKC, **2020** [mospace].

[10] Joshua Harp, “Development of an Adaptive Electromagnetic Interference Testing Method,” MS Thesis in Mechanical Engineering, UMKC, **2019** [mospace].

11.6 IP Disclosures Filed

[1] D. Beetner, V. Khilkevich, A. Hassan, S. Xia, J. Hunter, A. Harmon, “Rapid Prediction of Electromagnetic Coupling to Electronic Circuits and Harnesses,” 2022.

[2] S. Bellinger, A. Caruso, A. Usenko, US Provisional Patent Application “Stacked Diode with Side Passivation and Method of Making the Same,” 12AUG2021.

[3] S. Bellinger, A. Caruso, A. Usenko, “Diode and Method of Making the Same,” 28JUNE2021.

[4] Bhamidipati, Myers, Caruso, “Multi-Stage Photo-Stimulated WBG-PCSS Driven RF Pulse Generation System Implementing Miniature Optical Sources,” 21UMK009, 04NOV2020.

[5] Shepard, “A Low Noise Optical Amplifier,” 21UMK007, 14SEPT2020.

[6] Eifler, “Photoconductive Contact Pattern for Enhanced Charge Collection,” 08JUL2020.

[7] Shepard, “A Novel Optical Fiber Amplifier,” 20UMK012, 02JUN2020.

[8] Doynov, “High-power High Repetition Rate Microwaves Generation with Differentially Driven Antenna,” 20UMK011, 19APR2020.

[9] Doynov, “Scalable Modular System for High-power Microwaves Generation,” 20UMK010, 19APR2020.

[10] Doynov, “Pulse Differential High-power Microwave Generation,” 19UMK007, 02JAN2019.

[11] Doynov, “Non-linear Network Topologies with Reutilized DC and Low-frequency Signal,” 19UMK008, 28DEC2018.

[12] Doynov, Caruso, “Non-Linear Transmission Line Topologies for Improved Output,” 19UMK005, 28SEPT2018

11.7 Provisional Patents Filed

[1] S. Bellinger, A. Caruso, A. Usenko, US Provisional Patent Application “Stacked Diode with Side Passivation and Method of Making the Same,” filed 09/10/2021.

[2] S. Bellinger, A. Caruso, A. Usenko, “Diode and Method of Making the Same” US Provisional Patent Application 63/216,550, filed 06/30/2021.

[3] P. Doynov, A. Caruso, “High-Efficiency High-Power Microwave Generation using Multipass Non-Linear Network Topologies,” filed 11/26/2019.

[4] Plamen Doynov, James Prager, Tim Ziemba, Anthony N. Caruso, “Non-Linear Transmission Line Topologies for Improved Output”, USPTO Provisional Serial No. 62/737,185, filed 09/272018.

11.8 Non-Provisional Patents Filed

[1] S. Bellinger, A. Caruso, A. Usenko, “Stacked Diode with Side Passivation and Method of Making the Same,” US Patent Application 17/946,022, filed 09/15/2022.

[2] S. Bellinger, A. Caruso, A. Usenko, “Diode and Method of Making the Same” US Patent Application 17/855,735, filed 06/30/2022.

11.9 Allowed/Issued Patents

[1] P. Doynov, A. Caruso, “Multi-Pass Nonlinear Network for Microwave Generation” US Patent Application 17/455,026, filed 11/16/2021 (Allowed 10/13/2022).