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PERFORMANCE ANALYSIS OF A MICROCOMPUTER-BASED SINGLE-LOOP
DIGITAL CONTROL SYSTEM



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Data Acquisition Group
Technology Branch

April 1986

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The subject of this thesis is the design, development, and analysis of a 16-bit micro-processor based digital control system. The purpose of the study is threefold:

1. To show that a hybrid computer system, consisting of 16-bit single board microcomputer and an analog computer, can be used effectively for digital control studies.
2. To evaluate the frequency response of the hybrid system.
3. To identify and evaluate the error contributors which can effect the performance of digital control systems.

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TABLE OF CONTENTS

	Page
1.0 INTRODUCTION	1
2.0 DESIGN OF THE DIGITAL CONTROL SYSTEM	3
2.1 Selection of the Microcomputer and Analog Computer.	3
2.2 Digital Control System Configuration.	3
2.3 Derivation of the Control Algorithms.	7
2.4 Implementation of the Control Equation on the Micro- computer.	7
2.5 Simulation of Plant Parameters on the Analog Computer	11
2.6 Interface Between the Microcomputer and Analog Computer	13
3.0 CONTROL LOOP PERFORMANCE ANALYSIS.	16
3.1 Response to a Step Input.	16
3.2 Response to Sinusoidal Inputs	19
3.3 Frequency Response and Phase Angle Measurements	19
3.4 Improved A/D Conversion	22
3.5 Step Responses of a Tustin Based Controller	22
3.6 Comparison Between the Tustin-Based and Rattan-Based Controllers	25
4.0 ERROR CONTRIBUTORS	28
4.1 Analog Computer	28
4.2 D/A Biasing	28
4.3 A/D and D/A Quantization.	29
4.4 Word Length	29

TABLE OF CONTENTS (CONTINUED)

	Page
4.5 Computation Delay	30
4.6 Truncation and Round Off.	34
5.0 PLANT SIMULATION ON TEXAS INSTRUMENTS (TI) TMS32010 DIGITAL SIGNAL PROCESSING CHIP	36
5.1 Rationale	36
5.2 Plant Digitization.	37
5.3 Control Loop Configuration.	37
5.4 Implementation of the Plant on the Texas Instruments TMS 32010 EVM Microcomputer	39
5.5 Step Response of the TMS32010 Plant	39
5.6 State Space Representation of the Plant	43
6.0 CONCLUSIONS.	48
 APPENDICES	
A1 Program Listing: 8-bit A/D; 8-bit D/A	50
A2 Program Listing: 8-bit A/D; 12-bit D/A.	52
A3 Program Listing: 12-bit A/D; 12-bit D/A	54
A4 Program Listing: Computational Delay.	56
A5 Program Listing: Round Off Routine.	58
A6 Program Listing: TMS32010 Digitized Plant	60
B1 Circuit Diagram: Interface Circuit 8-bit A/D; 8-bit D/A	62
B2 Circuit Diagram: Interface Circuit 8-bit A/D; 12-bit D/A.	63
B3 Circuit Layout and Diagram: Interface Circuit 12-bit A/D; 12-bit D/A	65
C1 Wiring Diagram: Analog Computer Patch for Uncompensated Plant.	70

TABLE OF CONTENTS (CONTINUED)

	Page
REFERENCES.	71

LIST OF FIGURES

Figure	Page
1. Block diagram of a sampled-data control loop.	4
2. Block diagram of a digital control loop with $H(s)=1$	5
3. Block diagram of a digital control loop used for this study .	6
4. Flow chart of the software package for the digital controller.	10
5. Analog computer patching configuration.	12
6. Interface circuitry for interconnecting the MEX68KECB and the analog computer	14
7. Experimental unit step response of the uncompensated plant with unity feedback.	17
8. Unit step responses with an 8-bit A/D converter and two different D/A converters	18
9. Experimental sinusoidal response of the digital control system	20
10. Frequency response demonstrating improvement of results with 12-bit D/A converter	21
11. Unit step responses demonstrating improvement of results with 12-bit A/D converter	23
12. Comparison between unit step responses of Rattan- and Tustin-based controllers with 8-bit A/D converter	26
13. Comparison between unit step responses of Rattan- and Tustin-based controllers with 12-bit A/D converter.	27
14. Computation delay results for Rattan-based controller	31
15. Computation delay results for Tustin-based ($T=0.04$ sec) controller	32
16. Computation delay results for Tustin-based ($T=0.15$ sec) controller	33
17. Unit step response. Truncation versus round off.	35

LIST OF FIGURES (CONTINUED)

Figure	Page
18. Block diagram of a MC68000/TMS32010 digital control loop. . .	38
19. Flow chart of the TMS32010 software package for the digitized plant.	40
20. Unit step response of TMS32010 Plant at $T=0.15$ sec.	42
21. State space representation of the plant	44
22. Alternative state space representation of the plant	45

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1.0 INTRODUCTION

Interest in digital control has expanded rapidly as a result of low cost 16-bit microprocessors and associated support devices being introduced. Digital control is an attractive alternative when considering a control strategy. Therefore, it is important that the capabilities and shortcomings of microprocessor based controllers be fully understood before they are put into service.

It is well known to designers of control systems that major difficulties are found in mechanization of the control algorithm. Mechanization means the selection of digital equipment, such as the Analog-to-Digital (A/D) and Digital-to-Analog (D/A) converters and the word length of the computer; the actual programming of the algorithm; and analysis of various error sources and the effects each has on the dynamics of the controller.

The digital control configuration, used for this study, consists of: a digital controller, implemented on a Motorola MC68000 based microcomputer board; in series with an analog plant, simulated on an analog computer.

The steps needed to meet the stated objectives are:

1. Selection of the digital processing components.
2. Generation of the software package which implements the control algorithm on the microcomputer system.
3. Simulation of the analog plant on an analog computer, and interconnection of the microcomputer and analog computer.

4. Evaluation of the performance of the control loop for several configurations.

5. Identification of items which cause degradation in the performance of the control loop.

6. Demonstration of a totally digital control loop configuration where the plant is digitized and simulated on a high speed microcomputer.

The results of this study will demonstrate the effectiveness of using a microprocessor based system for digital control.

2.0 DESIGN OF THE DIGITAL CONTROL SYSTEM

2.1 SELECTION OF THE MICROCOMPUTER AND ANALOG COMPUTER

The resources for performing digital control studies should be readily available and moderate in cost. The equipment used for this study was available for use at Wright State University. The Comdyna GP-6 and Electronics Associates, Inc., (EAI) TR-20 were the analog computers used throughout the digital control study effort. The processor chosen for the digital controller was the Motorola MC68000 16-bit microprocessor. This chip is representative of the many 16-bit microprocessors on the market, but it has several attributes which made it more suitable for the control study. The Motorola MEX68KECB Educational Circuit Board, a low cost MC68000 based microcomputer board, was used as the digital controller. This computer board was purchased for this project and several other digital control studies which will follow.

2.2 DIGITAL CONTROL SYSTEM CONFIGURATION

A single-loop sampled data control configuration is shown in Figure 1. The primary components of the loop are: $D_c(z)$, the digital controller which receives and transmits control data at sampling instant T ; $G_{ho}(s)$, a zero order hold device; $G(s)$, the plant or device which is to be controlled; and $H(s)$, the feedback element which takes the output of the plant to a summing junction where the difference between the set point and plant output, or the amount of error remaining to be corrected, is fed back to the controller input.

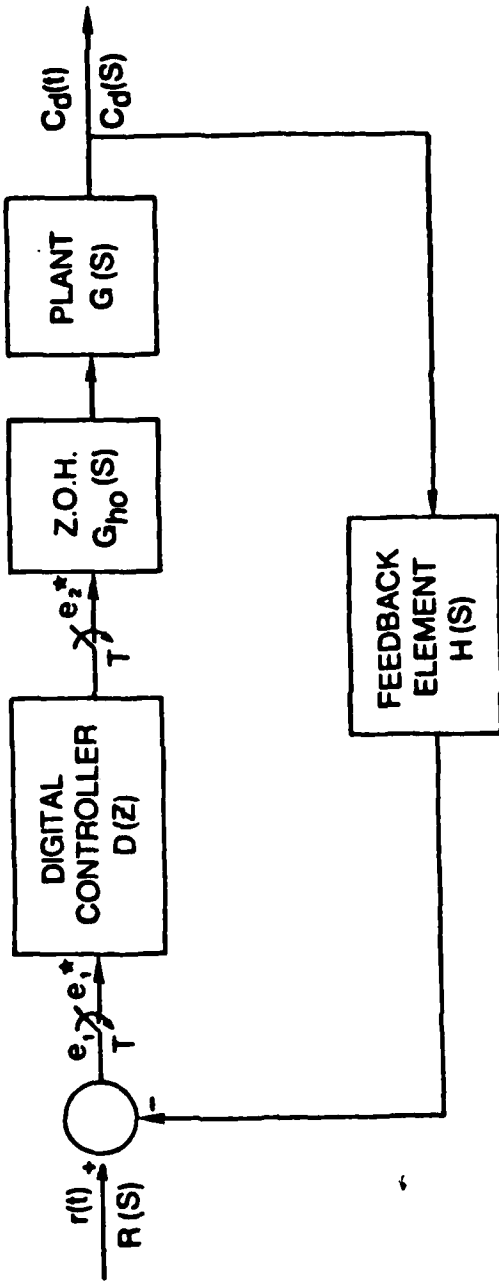


Figure 1. Block diagram of a sampled data control loop

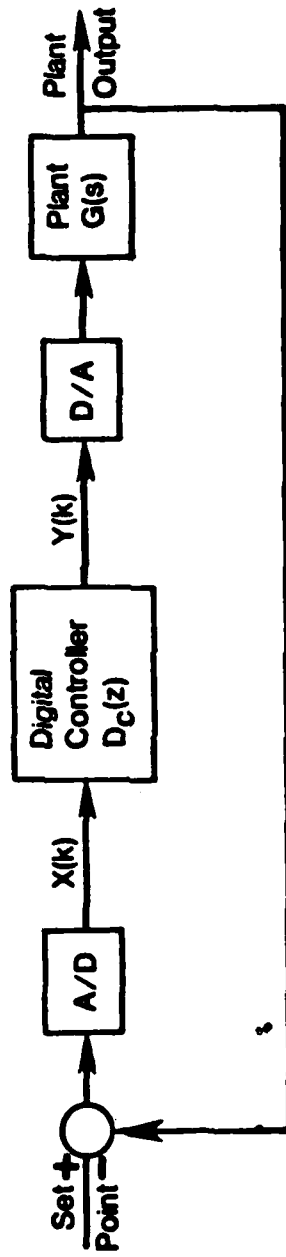


Figure 2. Block diagram of a digital control loop with $H(s)=1$

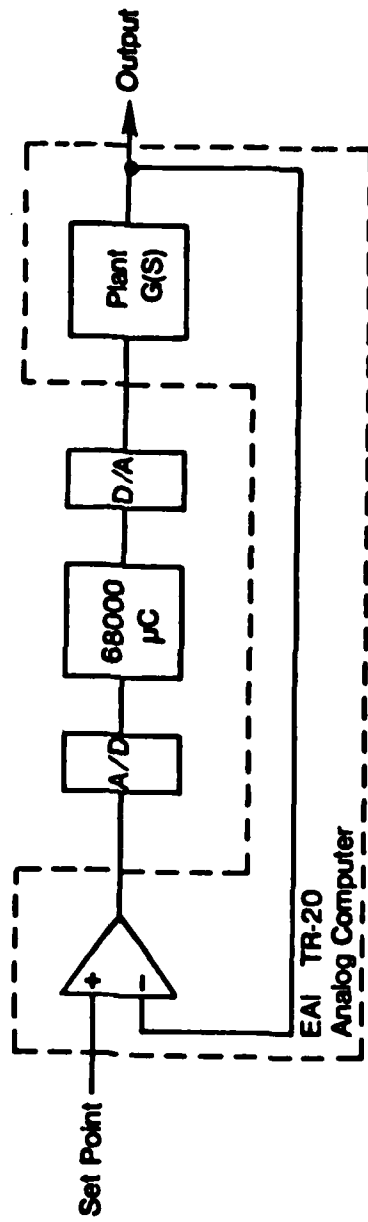


Figure 3. Block diagram of a digital control loop used for this study

The digital control loop used for this control study is similar to the configuration of Figure 1, except that the feedback element, $H(s)$, was set equal to one. Figure 2 shows this configuration. Figure 3 is a block diagram representation of the control system as implemented.

The plant $G(s)$, the unity feedback element $H(s)$, and the summing junction were implemented on an analog computer. The digital controller was implemented on the Motorola MEX68KECB computer board. The signal conversion devices, the A/D and D/A converters, were part of an interface board which was developed for this project.

The system characteristics are the following:

$$G(s) = \frac{6000}{s(s^2 + 40s + 300)} \quad (1)$$

$$H(s) = 1 \quad (2)$$

2.3 DERIVATION OF THE CONTROL ALGORITHM

The pulse-transfer function of the first order digital controller, used with the control loop, was obtained using the computer aided frequency matching method of Rattan [1]. The equation for $T=0.15$ seconds is given by:

$$D_c(z) = 0.154 \frac{z - 0.523}{z - 0.425} \quad (3)$$

This control equation will be the reference control algorithm to which other algorithms (under evaluation) will be compared.

2.4 IMPLEMENTATION OF THE CONTROL EQUATION ON THE MICROCOMPUTER

The digital control equation $D_c(z)$ must be implemented on a micro-computer. One method that is readily adaptable to computer application

and the method chosen for this study is the representation of $D_c(z)$ as a difference equation. Equation (3) can be written as:

$$\frac{Y(z)}{X(z)} = \frac{0.154z - 0.081}{z - 0.425} \quad (4)$$

Cross-multiplying equation (4), multiplying this result by z^{-1} , and solving for $Y(z)$, we get:

$$Y(z) = 0.425z^{-1}Y(z) + 0.154X(z) - 0.081z^{-1}x(z) \quad (5)$$

Taking the inverse z-transform of equation (5) yields:

$$Y(K) = 0.425*Y(K-1) + 0.154*X(K) - 0.081*X(K-1) \quad (6)$$

To implement the first-order difference equation given in equation (6) on a microprocessor, the coefficients have to be scaled to a convenient base for ease of numerical calculation. Since the word length of the MC68000 is essentially 16 bits, and none of the coefficients in the difference equation are greater than one, $32767(2^{15})$ was chosen as the base for all coefficients to maximize word length utilization (1 sign bit/15 magnitude bits). The resulting scaled integer coefficients were then converted to hexadecimal, and the resulting equation (7) is given by:

$$Y(K) = 3666*Y(K-1) + 13B6*X(K) - 0A5E*X(K-1) \quad (7)$$

where the coefficients for equation (7) were obtained by:

$$3666_{16} = 0.425*32767 \quad (8)$$

$$13B6_{16} = 0.154*32767 \quad (9)$$

$$0A5E_{16} = 0.081*32767 \quad (10)$$

Now that a control equation is in a form that can be implemented on the microprocessor, a software package must be written to instruct the microprocessor to execute a sequence of steps in order to achieve the desired output. The software package developed for the digital controller consists of four sections:

1. Initialization section
2. Interrupt servicing and data input section
3. Algorithm section
4. Data output section

The initialization section establishes the appropriate configuration for the microprocessor and its support chips. Some of the operations performed are: programming the peripheral interface adapters (PIAs), initializing the programmable interrupt timer (PI/T), and setting initial conditions for the control equation. The last operation of the initialization section is to enable interrupts, enter the halt mode, and wait for an interrupt to occur.

The interrupt service and data input section, which begin at each sampling instant by acknowledging the interrupt, resets the interrupt device and reads the data value, $X(K)$, to be processed.

The algorithm section calculates $Y(K)$ based on the control equation programmed on the microprocessor, outputs the results to the D/A for use by the plant, and stores appropriate values of $Y(K-1)$ and $X(K-1)$ for the next enumeration. The last operation performed is again enabling interrupts, forcing the processor to enter the wait mode until the next sampling instant. The flow chart of the software package is shown in Figure 4.

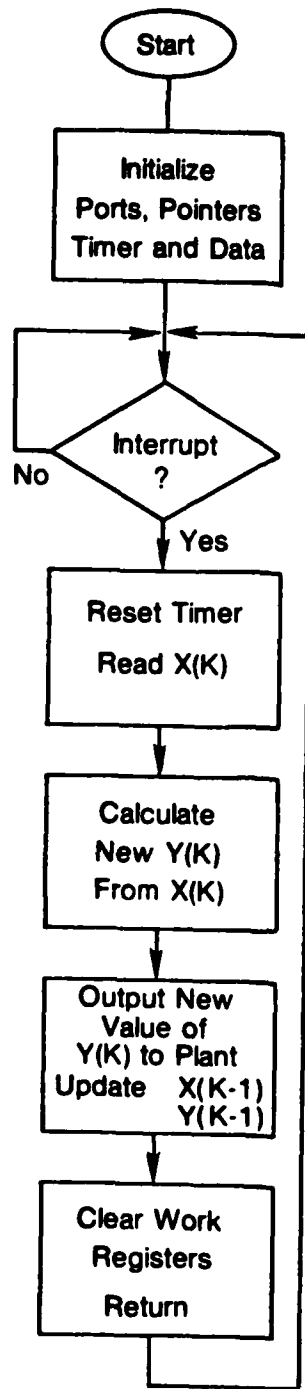


Figure 4: Flow chart of the software package for the digital controller

2.5 SIMULATION OF PLANT PARAMETERS ON THE ANALOG COMPUTER

The analog computer provides a convenient method for implementing the summing junction, the unity feedback element, and the plant characteristics. It contains a variety of active and passive components which can be externally configured through a patchboard to simulate the desired transfer function. The transfer function of the plant can be converted into an analog computer program as follows:

$$G(s) = \frac{C(s)}{Y(s)} = \frac{6000}{s^3 + 40s^2 + 300s} \quad (11)$$

Cross multiplying equation (11), we get:

$$s^3 C(s) + 40s^2 C(s) + 300s C(s) = 6000Y(s) \quad (12)$$

Inverse Laplace-transform of equation (12) yields:

$$\frac{d^3 C(t)}{dt^3} + 40 \frac{d^2 C(t)}{dt^2} + 300 \frac{dC(t)}{dt} = 6000Y(t) \quad (13)$$

In order to assure that the rate of change of $C(t)$ is consistent with the dynamic properties of the analog computer and X-Y plotter, equation (13) needs to be "time scaled" before it can be implemented on the analog computer. A time scaling of 50 resulted in the following equation:

$$s^3 C(s) = -0.8s^2 C(s) - 0.12s C(s) + 0.048Y(s) \quad (14)$$

This Laplace-transform representation of $C(s)$ can now be patched on the analog computer using the configuration shown in Figure 5.

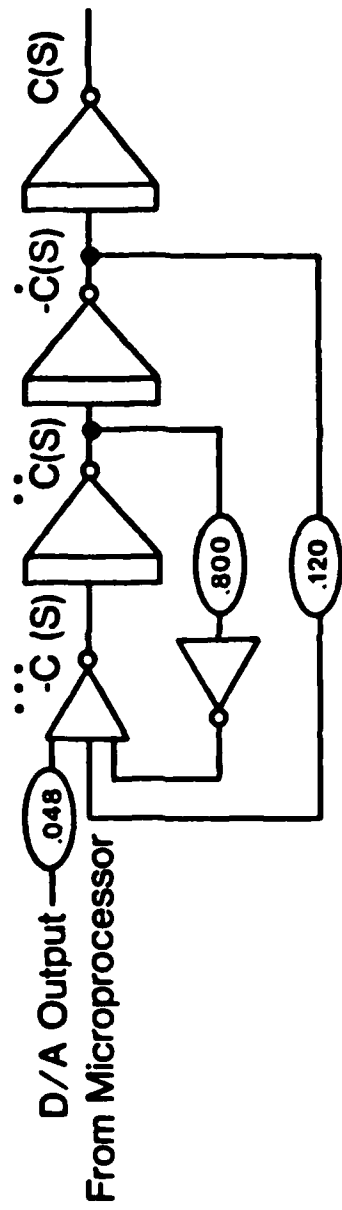


Figure 5. Analog computer patching configuration

2.6 INTERFACE BETWEEN THE MICROCOMPUTER AND ANALOG COMPUTER

Interface circuitry, which would permit interconnection of the microcomputer board and the analog computer, was developed for this study. This circuitry consisted of: the A/D and D/A converters and associated circuitry; two Peripheral Interface Adapters (PIA), one programmed as an input port (PIA1) and one programmed as an output port (PIA2); and devices used for chip enable circuits. Figure 6 shows a block diagram representation of the interface circuit. Interconnection between the interface circuit and the microcomputer was accomplished with 50 pin ribbon connectors and two specially made patchcords for connection to the analog computer. The interface circuit was easily modifiable for different A/D and D/A configurations. Let us take a closer look at each of the blocks of Figure 6. A substantial amount of time went into the design of the interface circuitry so a little more detailed description is called for at this time.

Motorola MC6821 Peripheral Interface Adapters (PIA) were used as the bus interface devices since the MC68000 contained control lines which would permit easy interconnection and operation. When a memory location above 030000 Hex was accessed on the MEX68KECB, the MC68000 microprocessor would enter the synchronous mode of operation. The Valid Memory Address (VMA*), an active-low signal was used as on chip enable signal for each PIA. Once a PIA was selected, a negative-going edge of the Enable (E) signal would cause the transfer of data. Three address lines (A1, A2 and A3) were used to select the proper PIA and the peripheral register. Each PIA needed to be initialized before it could be used to transfer data. Writing the proper data to the Control Registers and Data Direction Registers would set up each bit of the selected port

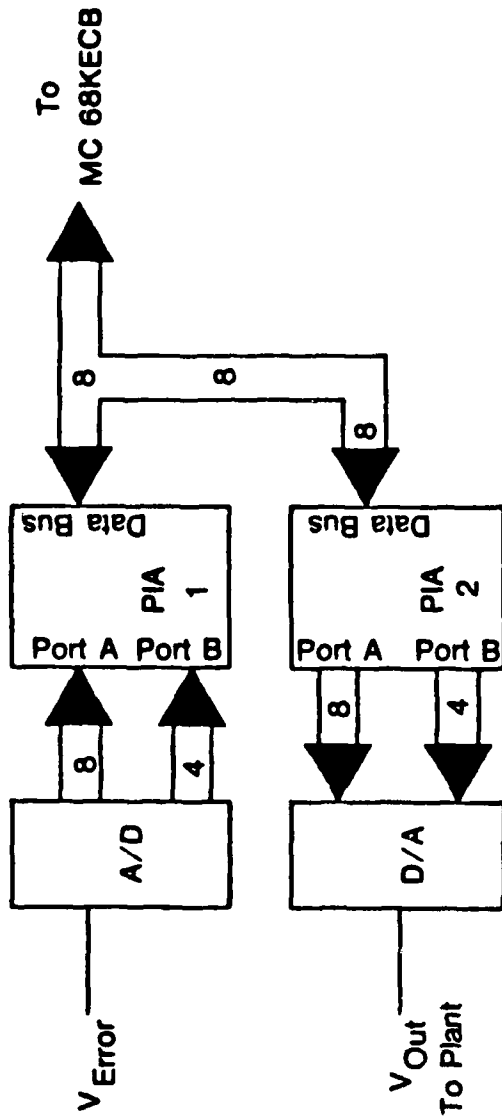


Figure 6. Interface circuitry for interconnecting the MEX68KECB and the analog computer

as an input or output. Bits PA0 through PA7 were programmed as input lines on PIA1. Bits PB4 through PB7 were also used when a 12-bit A/D converter was to be connected into the circuit. PB0 of PIA1 was used to provide a start convert signal to the 12-bit A/D converter. PIA2 was programmed in a similar manner as PIA1 except the peripheral ports were used as output lines. The Read/Write (R/W*) would determine the direction of the data transfer. When the R/W* line was a high logic level, data was transferred from the A/D converter, to a CPU register. When this line was a low logic level, data was transferred from a CPU register to the D/A converter.

The 8-bit devices used for the first hardware configuration were National Semiconductor ADC0800 8-bit successive approximation A/D converter; the D/A converter was the 8-bit DAC0808. The 12-bit D/A converter selected for the second configuration was the National Semiconductor DAC1218. The 8-bit A/D converter of the two previous arrangements was replaced with an Analog Devices AD572 12-bit successive approximation A/D converter. These conversion devices were selected for use since they were representative of current technology and readily available for use in the laboratory.

3.0 CONTROL LOOP PERFORMANCE ANALYSIS

3.1 RESPONSE TO A STEP INPUT

There were three signal conversion configurations used for this control study. The first configuration was an 8-bit A/D converter and an 8-bit D/A converter arrangement. The second configuration was similar to the first except that the 8-bit D/A converter was replaced with a 12-bit D/A converter. The final arrangement consisted of a 12-bit A/D converter and a 12-bit D/A converter. As will be shown later, the third arrangement provided the best performance, consequently, a permanent interface card was wire-wrapped.

The first step response to be measured was that of the uncompensated plant. Figure 7 shows the response obtained when the uncompensated plant was subject to a unit step input. Notice that the step response demonstrates the classical overshoot and oscillations associated with an underdamped system. Also notice that the steady-state value of the plant output is not 1 volt, but slightly less. This fact will be discussed further in Section 4.1.

The unit step responses of Figure 8 are for the compensated plant for the first- and second-signal conversion configurations. The overshoot is reduced significantly, as would be expected with a compensated plant. The steady-state oscillations observed will be discussed more thoroughly in Section 4.3.

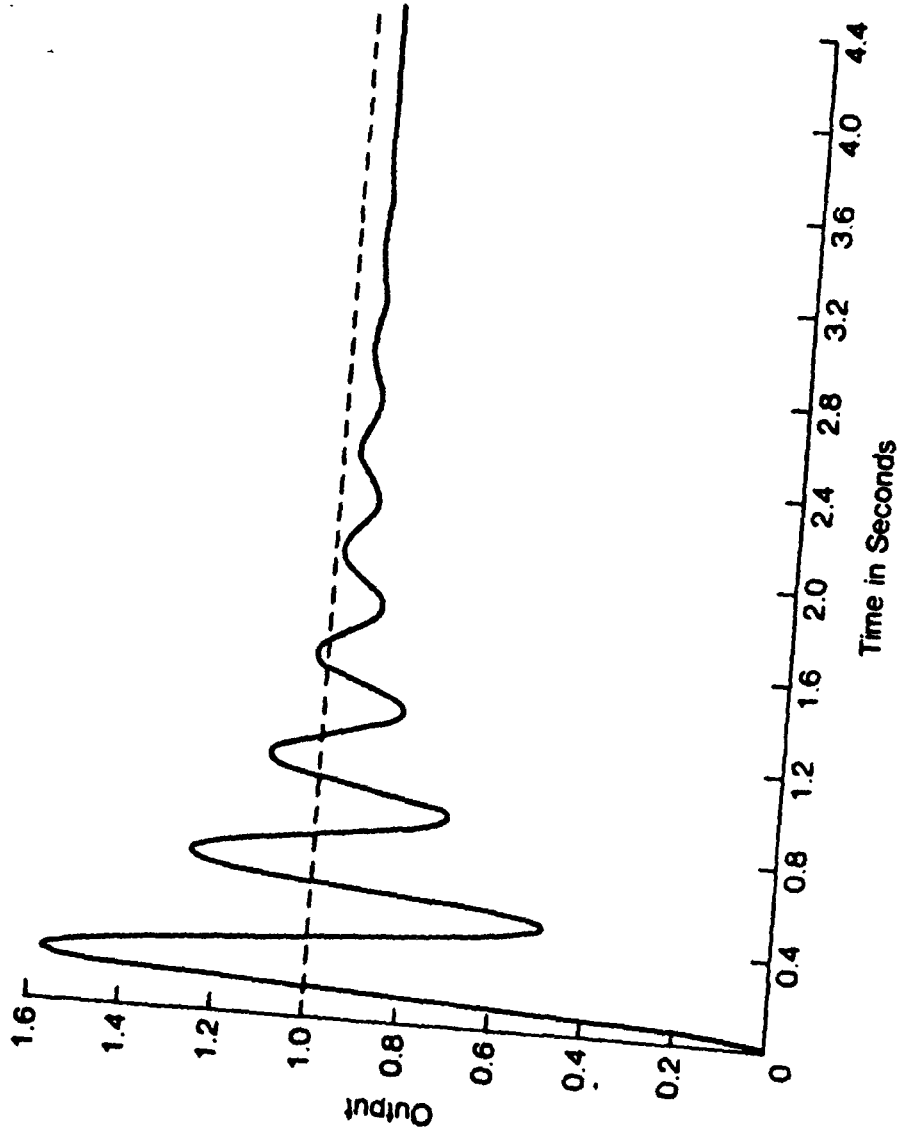


Figure 7. Experimental unit step response of the uncompensated plant with unity feedback

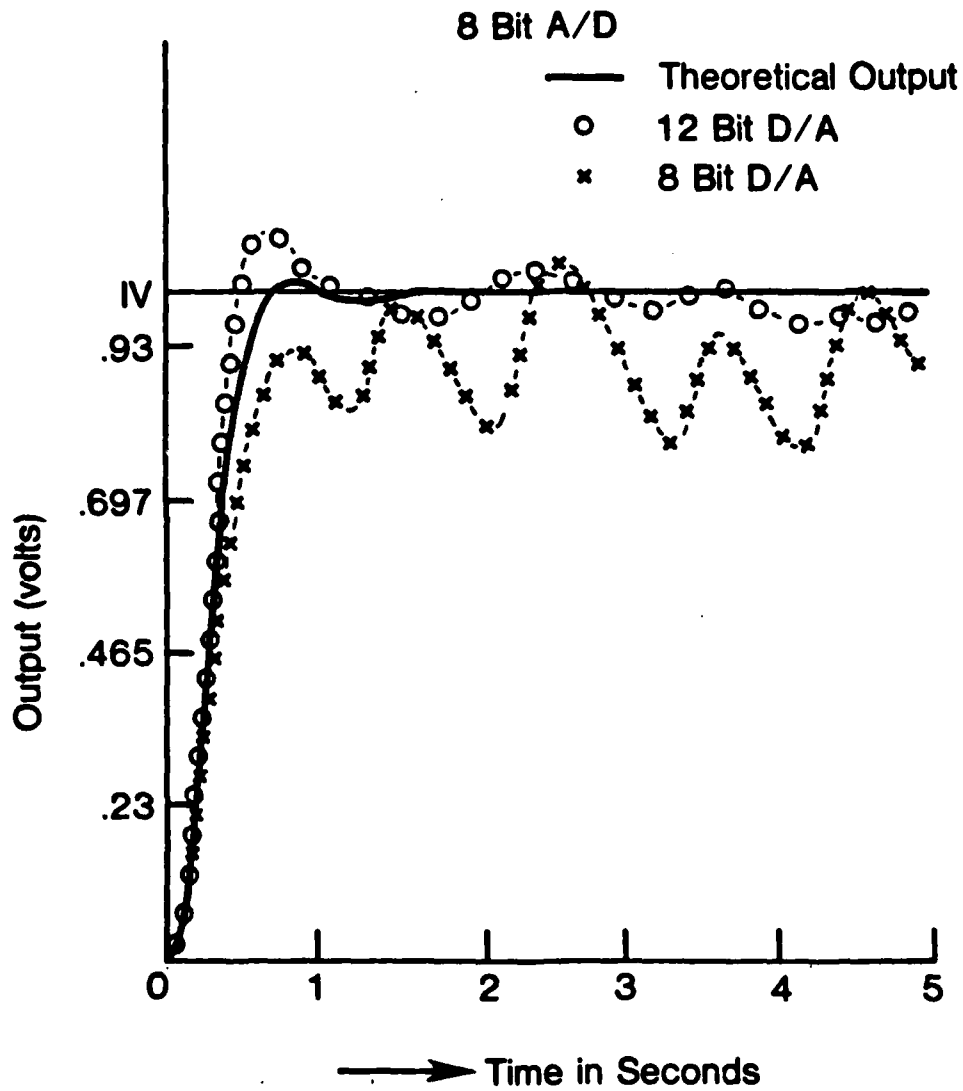


Figure 8. Unit step responses with 8-bit A/D converter and two different D/A converters

3.2 RESPONSE TO SINUSOIDAL INPUTS

One of the goals of the study effort was to experimentally evaluate the control loop response to sinusoidal inputs. This would provide a means of determining the frequency response of the digital control system. Sinusoidal inputs of frequency between 0 and $\omega_s/2$ were applied to the set point input of the control loop. Due to the amount of time scaling involved for the plant simulation, the frequency range needed for the sine waves was lower than that obtainable with waveform generators available in the laboratory. It was then necessary to use a second analog computer which generated the desired sine wave. The Laplace transform of the sine function is given by:

$$F(s) = \frac{\omega}{s^2 + \omega^2} \quad (15)$$

The analog computer was configured for equation (15) and different values for ω were programmed to yield the proper input frequency. Figure 9 shows the results obtained for one of the input frequencies. Results for both 8-bit D/A and 12-bit D/A converters are shown on the same plot, along with the input frequency. Notice the magnitude attenuation and phase shift associated with each response. The magnitude attenuation is greater with the 8-bit D/A converter than with the 12-bit D/A converter. Comparison of the phase shifts for each D/A configuration shows little difference between them.

3.3 FREQUENCY RESPONSE AND PHASE ANGLE MEASUREMENTS

The results obtained for frequency response and phase angle measurements are shown in Figure 10. Data for both D/A converter configurations are plotted together with the theoretical responses. The theoretical responses for magnitude and phase angle were obtained using

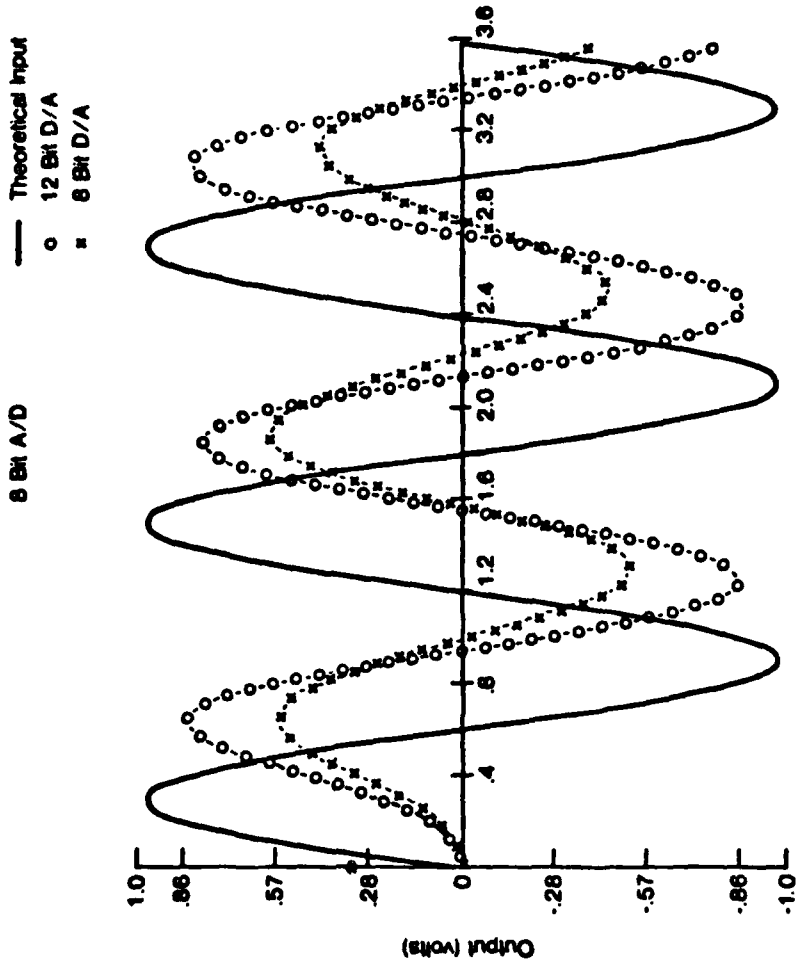


Figure 9. Experimental sinusoidal response of the digital control system

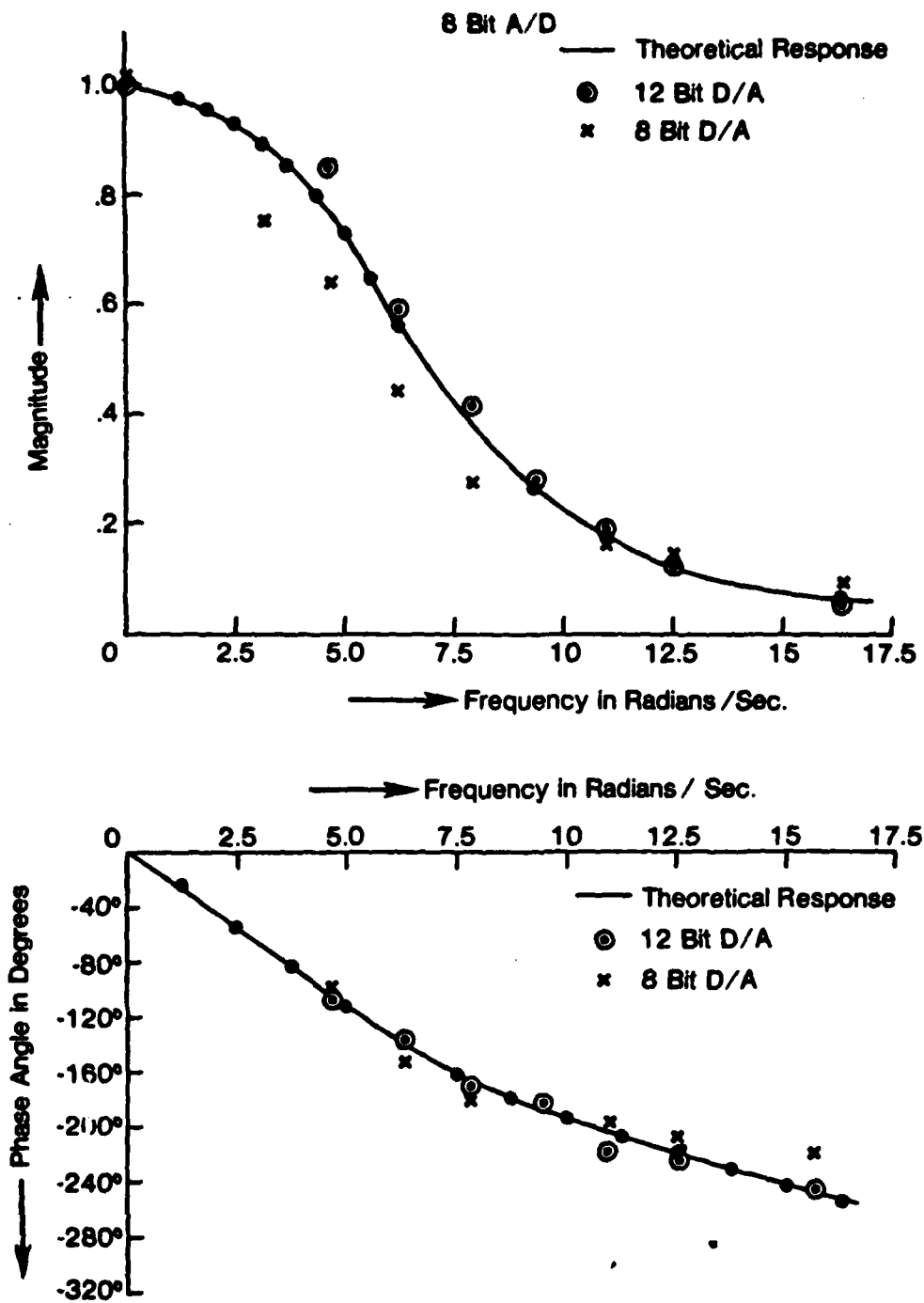


Figure 10. Frequency response demonstrating improvement of results with 12-bit D/A converter

the interactive control analysis program TOTAL. The theoretical data curves provide a reference to which the experimental results can be compared. The magnitude plot shows that the frequency response with the 12-bit D/A converter follows the theoretical frequency response more closely than with the 8-bit D/A converter. Results from the phase angle plot demonstrate that little differences exist between the phase plots for the 8-bit D/A and 12-bit D/A converters, except at the highest frequencies where the 8-bit D/A converter exhibited more deviation from the theoretical phase angle curve.

3.4 IMPROVED A/D CONVERSION

All of the performance analysis of the control loop thus far has been with an 8-bit A/D converter. There was an improvement in control system accuracy when the 8-bit D/A converter was replaced with the 12-bit D/A device. The 8-bit A/D converter will be replaced with a 12-bit A/D converter, resulting in the third control system configuration, that is, 12-bit A/D and 12-bit D/A converters. The remaining performance tests were based on this configuration. Figure 11 contains step responses, one where the loop uses an 8-bit A/D converter and one where the loop uses a 12-bit A/D converter. The step response associated with the 12-bit A/D device exhibits slightly less steady-state oscillation than with the 8-bit A/D converter. The improvement in control loop performance (obtained with improved A/D conversion) is not as pronounced as the improvement demonstrated with improved D/A conversion.

3.5 STEP RESPONSES OF A TUSTIN BASED CONTROLLER

Control loop performance was demonstrated with several different hardware configurations, but all of them with the Rattan-based control

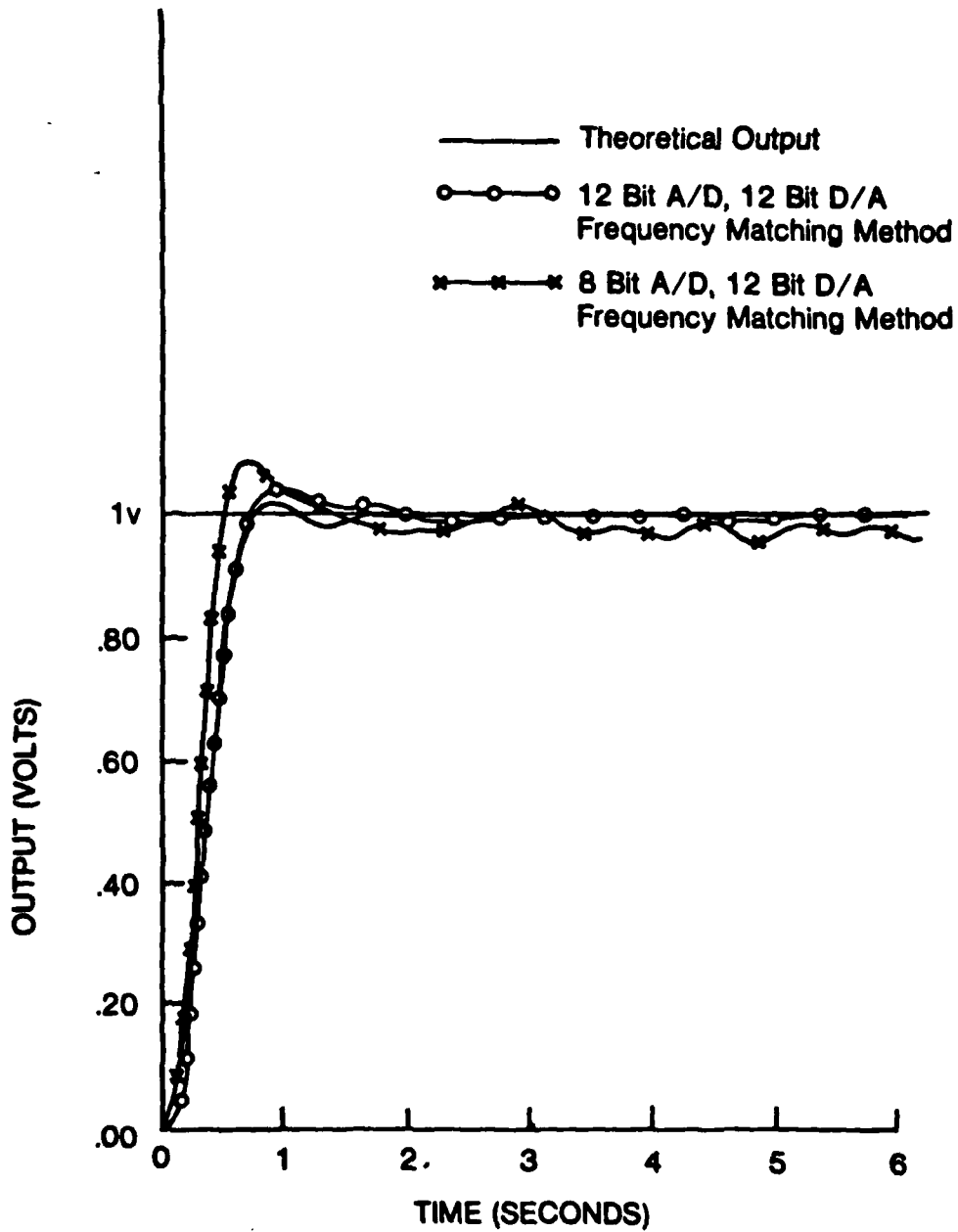


Figure 11. Unit step responses demonstrating improvement of results with 12-bit A/D converter

algorithm. The Tustin transformation or bilinear transformation [4] as it is commonly known, provides another means of obtaining a discrete system from the continuous system. The continuous controller on which the Rattan algorithm was based is given by:

$$G(s) = 0.322 \frac{(s+1.914)}{(s+0.616)} \quad (16)$$

Substituting:

$$s = \frac{2}{T} \frac{z - 1}{z + 1} \quad (17)$$

into equation (16) and using the appropriate value for the sampling period (T), the result obtained is a digitized controller of the same order. The Tustin-based controllers for T=0.15 seconds and T=0.04 seconds are given by equations (18) and (19), respectively as:

$$D(z) = 0.352 \frac{(z - 0.749)}{(z - 0.912)} \quad (18)$$

$$D(z) = 0.330 \frac{(z - 0.926)}{(z - 0.976)} \quad (19)$$

The Tustin controller equations can be rearranged and the coefficients converted to hexadecimal, as previously demonstrated with the Rattan controller, to obtain the control algorithms:

$$Y(K) = 74B2Y(K-1) + 2D04X(K) - 21B7X(K-1) \quad (20)$$

$$Y(K) = 7CE3Y(K-1) + 2A40X(K) - 2721X(K-1) \quad (21)$$

for T=0.15 seconds and T=0.04 seconds, respectively. The Tustin control algorithms were implemented on the digital controller by changing the memory locations, which contained the associated coefficients.

3.6 COMPARISON BETWEEN THE TUSTIN BASED AND RATTAN BASED CONTROLLERS

The step responses of Figures 12 and 13 demonstrate the significant response variations between the Rattan and Tustin control algorithms. The lessons learned from this indicate that for a given hardware configuration, variations in the control algorithm can have a significant effect on the overall performance of the control loop. The Tustin control algorithms seem to be more sensitive to the size of the signal conversion device than the Rattan algorithm. It is best to use the largest bit sized conversion device possible when implementing a Tustin based controller to insure proper control loop operation.

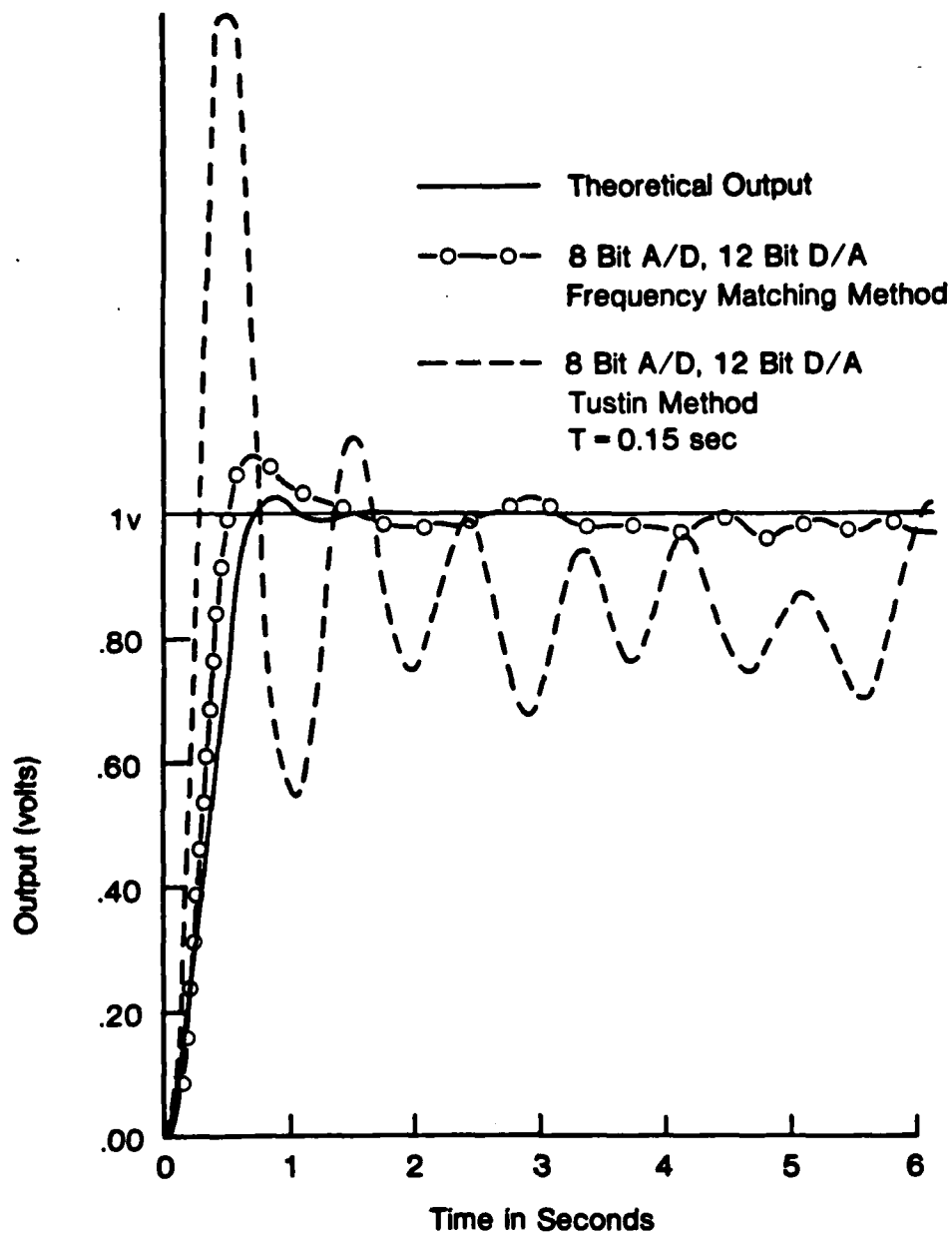


Figure 12. Comparison between unit step responses of Rattan- and Tustin-based controllers with 8-bit A/D converter

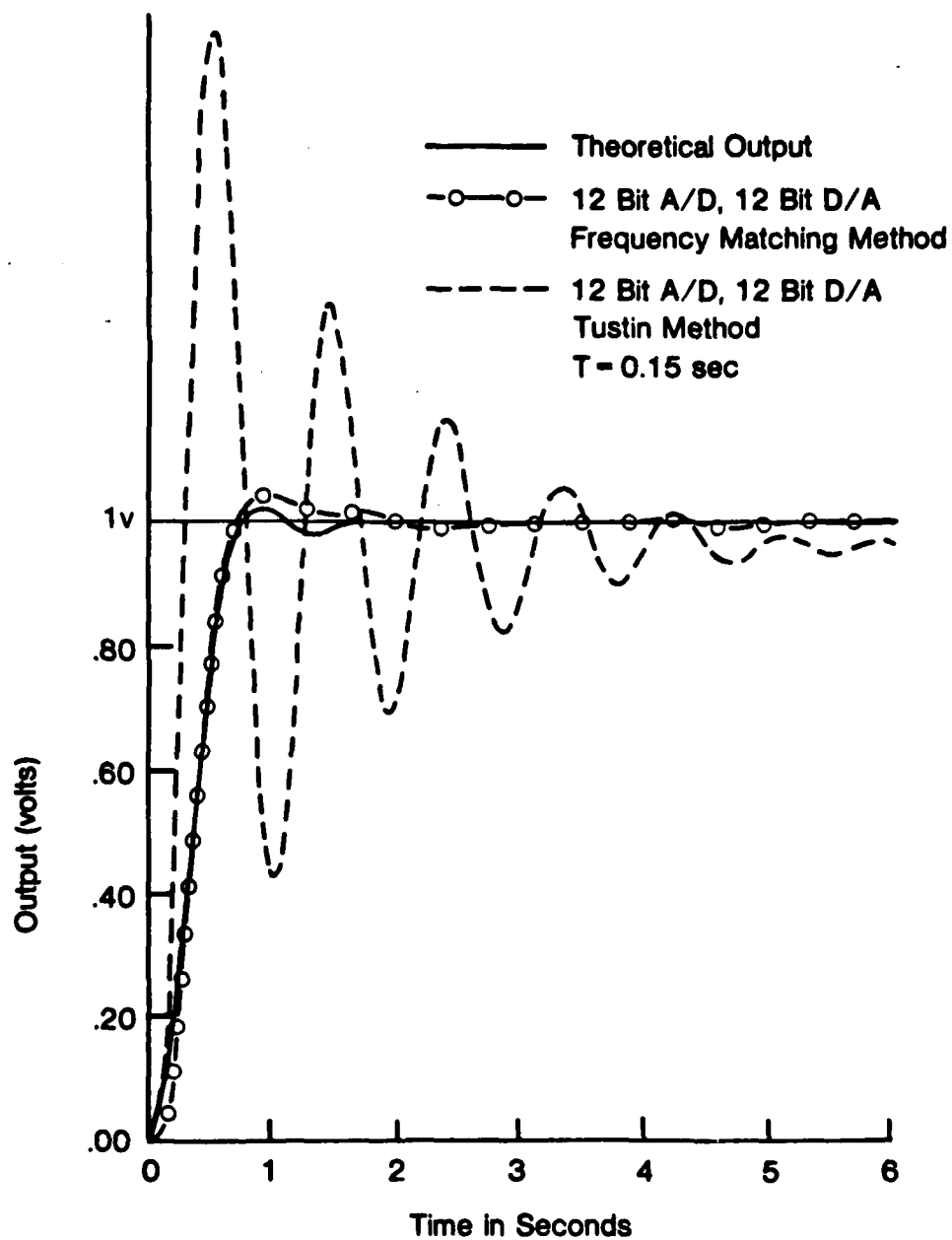


Figure 13. Comparison between unit step responses of Rattan- and Tustin-based controllers with 12-bit A/D converter

4.0 ERROR CONTRIBUTORS

4.1 ANALOG COMPUTER

The transfer function of equation (1) is of type 1, which means that the theoretical steady-state error is equal to zero. However, the plant, as implemented on the analog computer, was found to have an error of +50 millivolts (mV) when configured with unity feedback and a set point of 1 volt, (v), hence, it was necessary to establish a D/A bias at "digital zero," which resulted in a +50 mV output from the controller. This D/A bias would, in effect, compensate for the analog computer error.

4.2 D/A BIASING

The use of a +50 mV D/A bias is in itself an induced error, since it is desirable to have "digital zero" to the D/A represent a true value of zero volt. Two problems closely related to the D/A biasing error are over/under D/A biasing and D/A bit size. If the bias was set to some value other than +50 mV, excessive steady-state oscillations would occur. Care was taken to insure the setting of the proper D/A bias prior to any data collection. Proper setting of the required D/A bias was difficult at best with the 8-bit D/A converter, but became less of a problem when the 12-bit D/A converter was used. Establishment of the proper D/A bias insured that the overall plant response would be correct.

4.3 A/D AND D/A QUANTIZATION

An 8-bit converting device has 256 discrete values, whereas, a 12-bit converting device has 4096 discrete values associated with it. For a reference voltage range of 10 V ($\pm 5V$), the resolution for an 8-bit and a 12-bit converters are 39 mV and 2.44 mV, respectively. Due to D/A quantization, the plant output oscillated between the D/A output levels, which drove it positive or negative. As the D/A size was increased, the number of quantization levels also increased, which resulted in smaller increments between the output levels, therefore, less steady-state oscillation. Similarly, an increase in A/D bit size increased the digital accuracy and reduced the input quantization approximation error.

A comparison of the D/A output quantization effects can be seen in the unit step plots of Figure 8. The reduction in oscillation of the 12-bit configuration is very evident. The step response plots of Figure 11 demonstrate that further improvement in plant response was observed with a 12-bit A/D converter, although this improvement is not as significant as seen with the D/A converter change.

4.4 WORD LENGTH

Another source of system error is the finite word length of the computer. As seen previously, the size of the signal conversion components has a significant effect on the performance of the control loop. The coefficients of the control algorithm are scaled values based upon a binary fixed-point numerical representation. As the internal precision of the word length of the computer goes up, so does the resolution of the coefficients. This increased precision propagates throughout the calculations so that the upper word of the final computed value is a more accurate representation than what would have been

obtained using lower precision numerical representation. It is the upper word of the final value which is sent to the D/A converter. The 16-bit word length of the MC68000 found to be more than sufficient for producing acceptable accuracy.

4.5 COMPUTATION DELAY

The control algorithm takes a finite amount of time to produce an output based upon a given input. This delay is the amount of time it takes to calculate the control output at a given sampling instant from an error input taken simultaneously. The effects of computation delay on control loop performance may or may not be significant. If the ratio of computation delay to sample rate is small, then computation delay should not be a problem. As this ratio becomes larger, the effects of computation delay on loop performance should become apparent. To experimentally determine computation delay, it was necessary to place a delay routine in the control algorithm. The length of the delay was controlled by a specific value, placed in a register, which was decremented until it was zero. Computation delay values of $1/4T$ and $1/2T$ were used. Figures 14 and 15 show results obtained for the Rattan based and Tustin-based ($T=0.04$ sec.) controllers. The plots for computation delays of $1/2T$ show that during transient periods, the plant will tend to overshoot more when compared to the plots with computation delay of $1/4T$. A comparison of computation delays of $1/16T$ and $1/8T$ for the Tustin-based ($T=0.15$ sec.) is given in Figure 16. The effects of smaller computation delays are more noticeable with this longer sampling period than with the $T=0.04$ sec. controller. This is an indication that the plant is sensitive to a fixed amount of computation delay since $1/16T$ of the $T=0.15$ sec. controller is approximately equal to $1/4T$ of

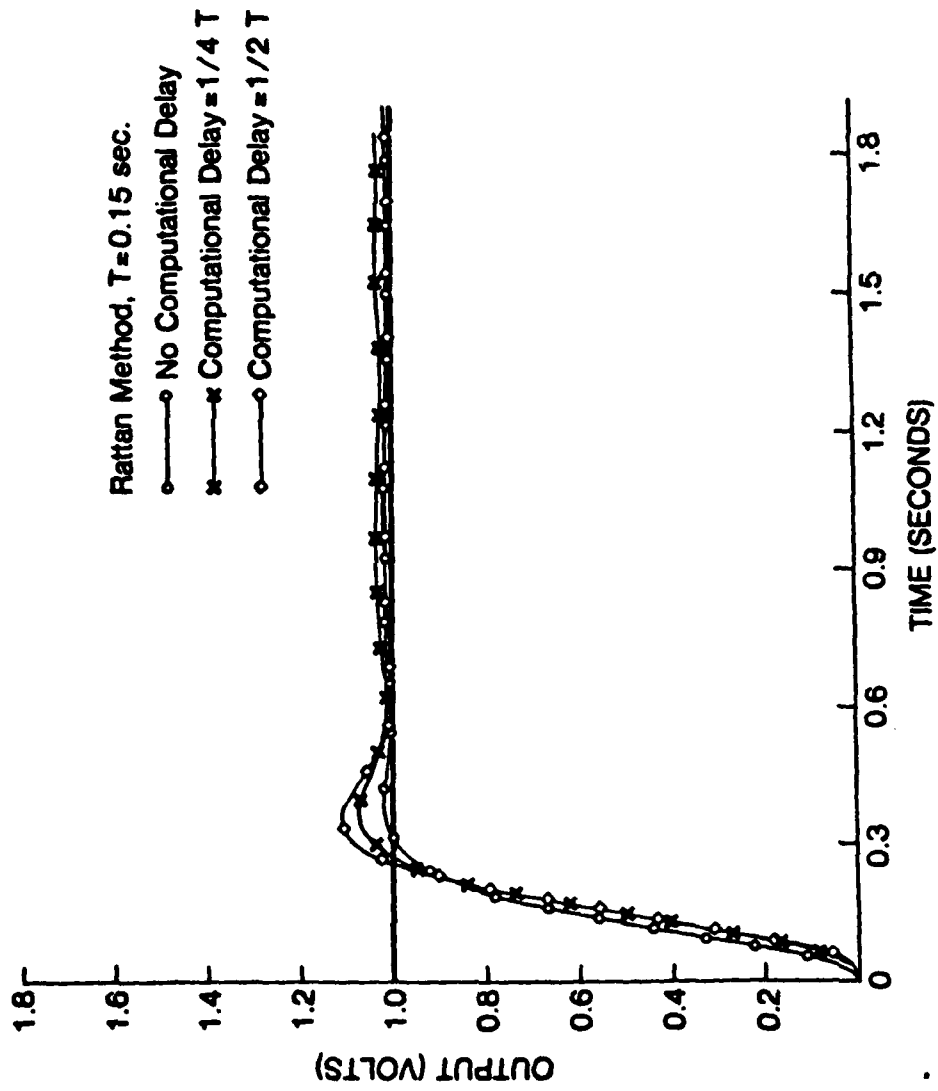


Figure 14. Computation delay results for Rattan-based controller

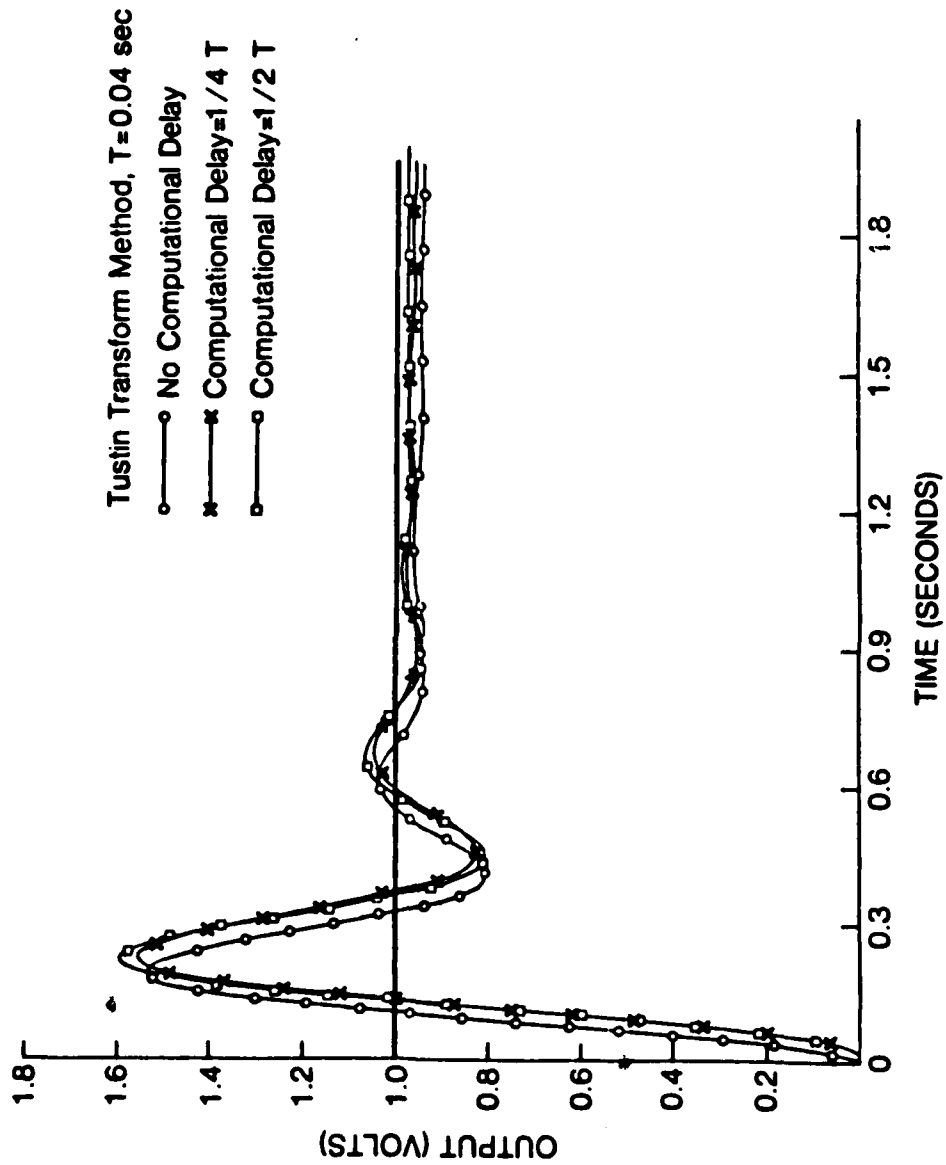


Figure 15. Computation delay results for Tustin-based ($T=0.04$ sec) controller

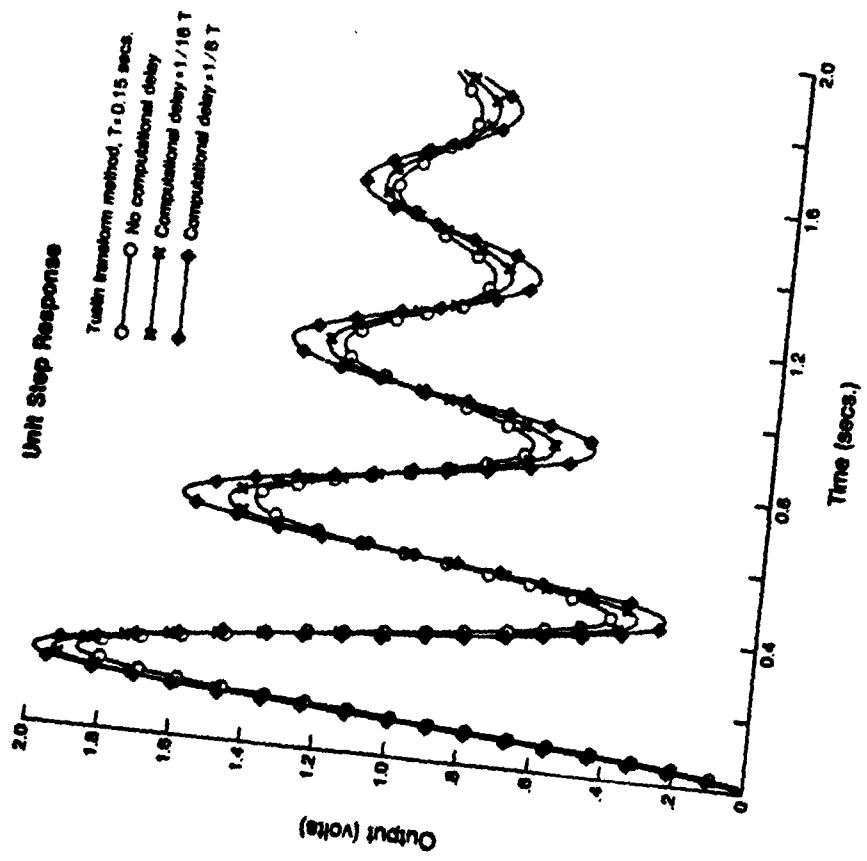


Figure 16. Computation delay results for Tustin-based ($T=0.15$ sec) controller

the $T=0.04$ sec. controller. As the plant approaches steady-state, the effects of computation delay diminish. For the control configurations of this study, it appeared that computation delay did not effect the control loop significantly; however, this may not be true for other types of reference inputs.

4.6 TRUNCATION AND ROUND OFF

Truncation is the process of ignoring all bits less than the least significant bit, whereas, round off is the process of selecting a number which is closest to the unrounded quantity. For example, the decimal number 1.96 will be truncated to a value of 1.9 and rounded to 2.0 for two significant digits of accuracy. The procedures of truncation and round off for binary numbers are the same. All of the control algorithms so far have used truncation of the final output result. The final result obtained was either a 24-bit or a 28-bit result, depending on the size of the A/D converter used. The most significant 8- or 12-bits for the final value were passed to the D/A converter, depending on the size of the D/A device. The remainder of the lower significant bits did not contribute to the magnitude of the final output value. A rounding routine was written for the 12-bit A/D, 12-bit D/A control configuration to include the effects on these lowest bits in the final value. Figure 17 shows unit step responses of the plant; one with rounding, one without. For the configuration used in this control study, rounding did not provide significant improvement in loop performance as anticipated. However, the step response of the control algorithm with rounding did seem to have a steady-state value slightly closer to the value of 1 volt.

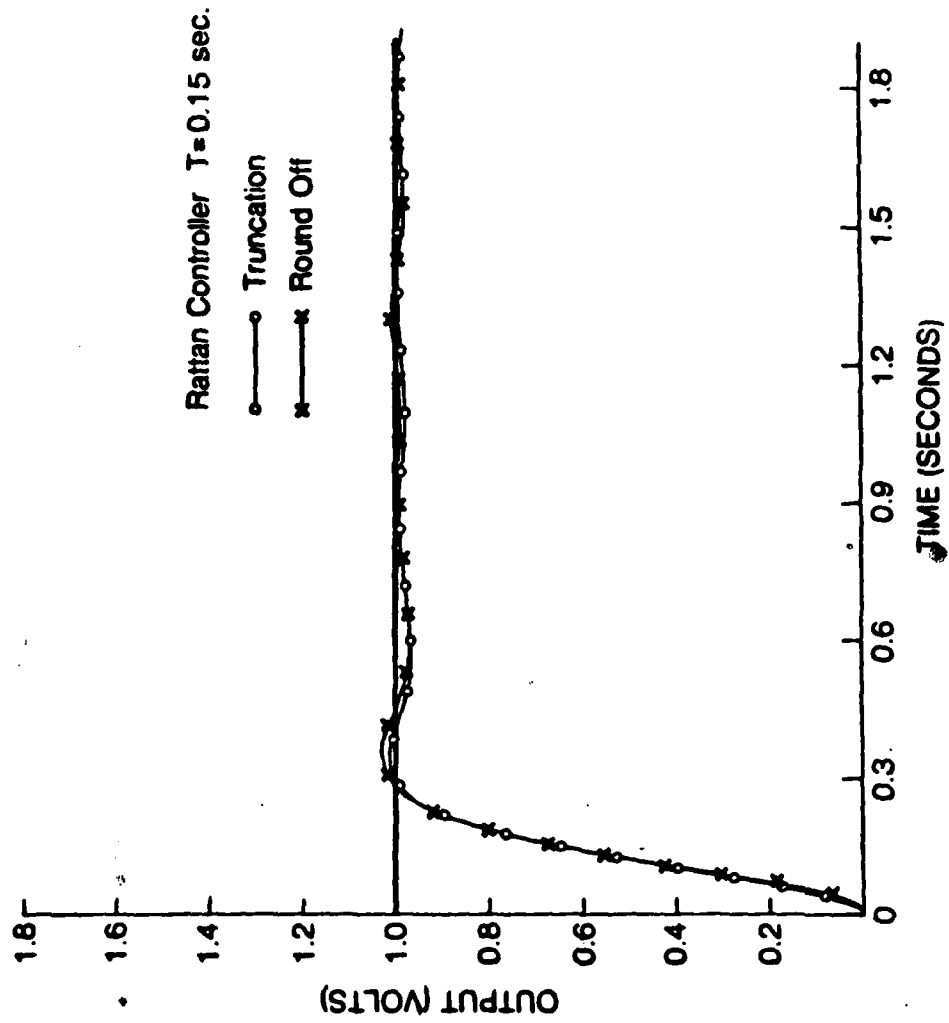


Figure 17. Unit step response. Truncation versus roundoff

5.0 PLANT SIMULATION ON THE TEXAS INSTRUMENTS (TI) TMS32010 DIGITAL SIGNAL PROCESSING (DSP) CHIP

5.1 RATIONALE

The plant for the control study thus far has been simulated on an analog computer, which has a time scale factor of 50. This time scaling equates to a sampling period of 7.5 seconds. There could be several advantages in replacing the analog computer with a digital computer such as; more flexibility, elimination of offset error and elimination of time scaling. The sampling period of the control loop would then be 0.15 seconds instead of 7.5 seconds. The requirement is that the plant must be able to be simulated on a computer, which would permit proper operation of the control loop at the desired sampling rate. One approach is to digitize the plant using the Tustin transform with a sampling period of 0.015 seconds and implement the resulting digital transfer function on a high speed digital signal processing computer. The computer considered for plant implementation was the Texas Instruments (TI) TMS32010 Evaluation Module (EVM) and the TI TMS32010 Analog Interface Board (AIB). The EVM board is an evaluation microcomputer board based upon the TI TMS32010 digital signal processor chip. The AIB is a support board which provides the necessary 12-bit signal conversion so that the EVM board can be used for signal processing applications. The combination of these boards would provide everything needed for "real-time" digital simulation of the plant.

5.2 PLANT DIGITIZATION

The transfer function of the plant must be digitized before it can be implemented on the TMS32010 EVM. The Tustin transformation, equation (17) must be substituted into equation (1). Keeping T unspecified so that a general equation can be derived and simplifying the resulting expression will give a digitized transfer function of:

$$G(z) = \frac{6000T^3[z^3+3z^2+3z+1]}{8[z^3-3z^2+3z-1]+160T[z^3-z^2-z+1]+600T^2[z^3+z^2-z-1]} \quad (22)$$

If T is set equal to 0.015 seconds, equation (22), when simplified becomes

$$G(z) = \frac{Y(z)}{X(z)} = \frac{0.02025z^3+0.06075z^2+0.06075z+0.02025}{10.535z^3-26.265z^2+21.465z-5.735} \quad (23)$$

Equation (23) will be implemented in software on the TMS32010 EVM board.

5.3 CONTROL LOOP CONFIGURATION

The control loop configuration (using the TMS32010 EVM) is essentially the same as that of Figure 1, except that now there is a digital plant instead of analog plant. Figure 18 is a block diagram of the control loop configuration needed for this portion of the control study. There are two major differences between the control loop of Figure 1 and the control loop of Figure 18; the summing junction is a difference amplifier located on the digital controller interface card and the plant transfer function, which is implemented on the TMS32010 EVM/A1B combination, is a sampled data system operating one-tenth of the controller sample rate.

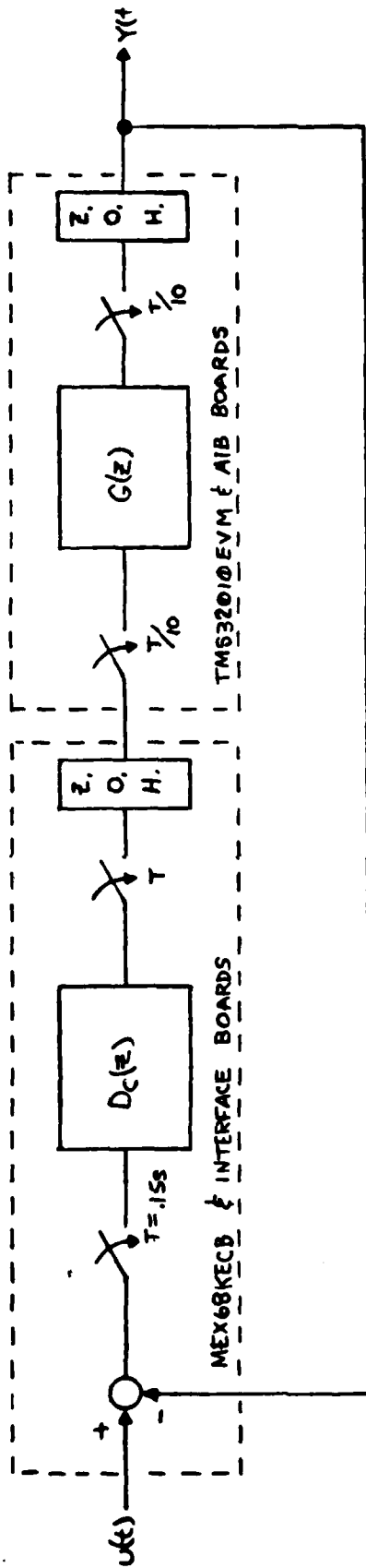


Figure 18. Block diagram of a MC68000/TMS 32010 digital control loop

5.4 IMPLEMENTATION OF THE PLANT ON THE TEXAS INSTRUMENTS TMS32010 EVM MICROCOMPUTER

Equation (23) must be converted to a difference equation so that the plant transfer function can be implemented directly on the EVM. Solving equation (23) for $Y(z)$ yields the following:

$$Y(z) = 2.493z^{-1}Y(z) - 2.037z^{-2}Y(z) + 0.544z^{-3}Y(z) + 0.00192X(z) \\ + 0.00577z^{-1}X(z) + 0.00577z^{-2}X(z) + 0.00192z^{-3}X(z) \quad (24)$$

Notice that the first two coefficients are larger than one, which means that scaling must be employed to obtain functional values for the coefficients. The smallest number that is equal to 2^n and larger than all of the coefficients is 4. Dividing all coefficients of equation (24) is effectively a normalization process. Taking the inverse Z-transform and converting the coefficients to their representative hexadecimal values which results in the following:

$$\frac{Y(K)}{4} = 4FCE * Y(K-1) + BED1 * Y(K-2) + 1168 * Y(K-3) + 0010 * X(K) + 002F * X(K-1) \\ + 002F * X(K-2) + 0010 * X(K-3) \quad (25)$$

Equation (25) can now be programmed directly into TMS32010 assembly language, employing the same techniques as used when the digital control equation was implemented in software. Figure 19 is a flow chart for implementation of the digitized plant transfer function on the TMS32010 EVM/A1B system.

5.5 STEP RESPONSE OF THE TMS32010 PLANT

The unit step response of the uncompensated digital plant at $T=0.015$ sec. was not obtainable for some unknown reason, so a search into the possible problems was conducted. The software was checked for

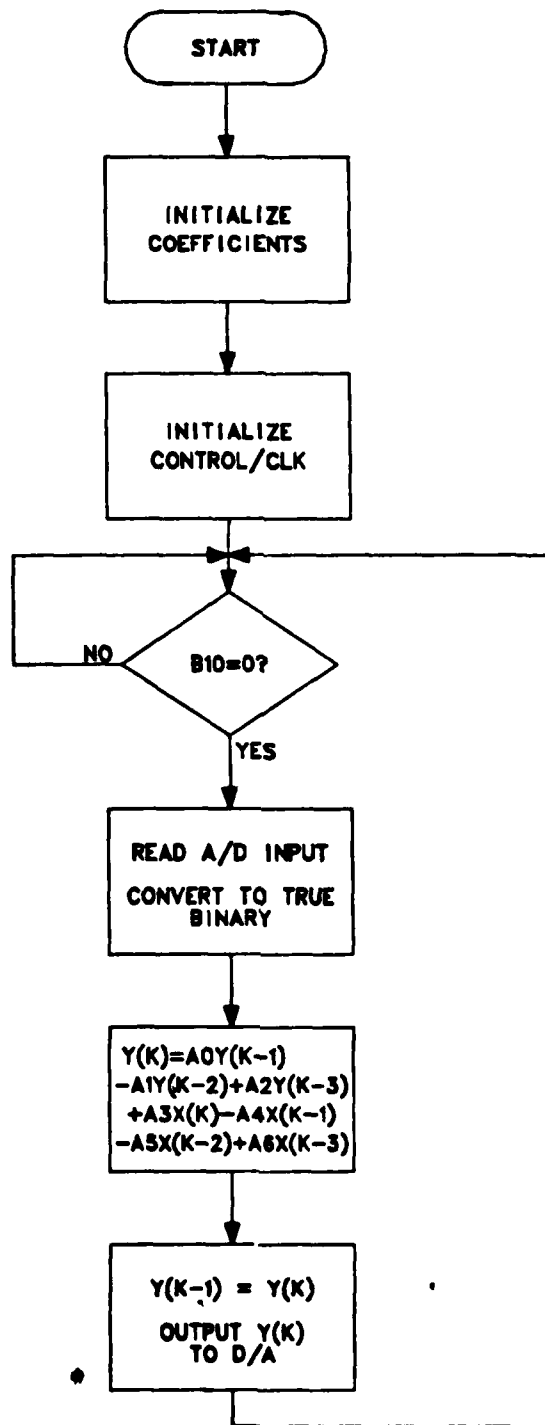


Figure 19. Flow chart of the TMS 32010 package for the digitized plant

any logic or programming errors. corrections were made, but the control loop still did not function properly. Once the program had been thoroughly checked, the next step was to try a slower sampling rate, in this case $T=0.15$ sec. The unit step response of Figure 20 is that of the uncompensated digital plant in closed loop form with the slower sampling rate. The unit step response had proven that the program was indeed working, since there is little difference between this program and the program for the digitized plant operating at $T=0.015$ sec. Furthermore, the plant is undersampled at $T=0.015$ sec., an indication that a higher sampling rate is definitely needed for proper plant representation. The major difference between the two plant programs is in the coefficients of the difference equation. Closer inspection of equation (24) shows that the ratio between the largest coefficient and the smallest coefficient is approximately 1300 to 1. This large of a coefficient span was not represented accurately with the fixed point binary numbering scheme. The use of coefficient normalization apparently added to the problem. By comparison, the closed loop representation of the $T=0.15$ sec. plant required no coefficient normalization and the span of the coefficients was smaller.

The problem just discussed becomes worse as the sampling rate of a system is increased. Direct implementation of a difference equation is not feasible particularly when higher sampling rates are used. An alternative method of implementation that produces more manageable fixed point coefficients is needed. One method which may work is to represent the plant as a set of discrete state equations.

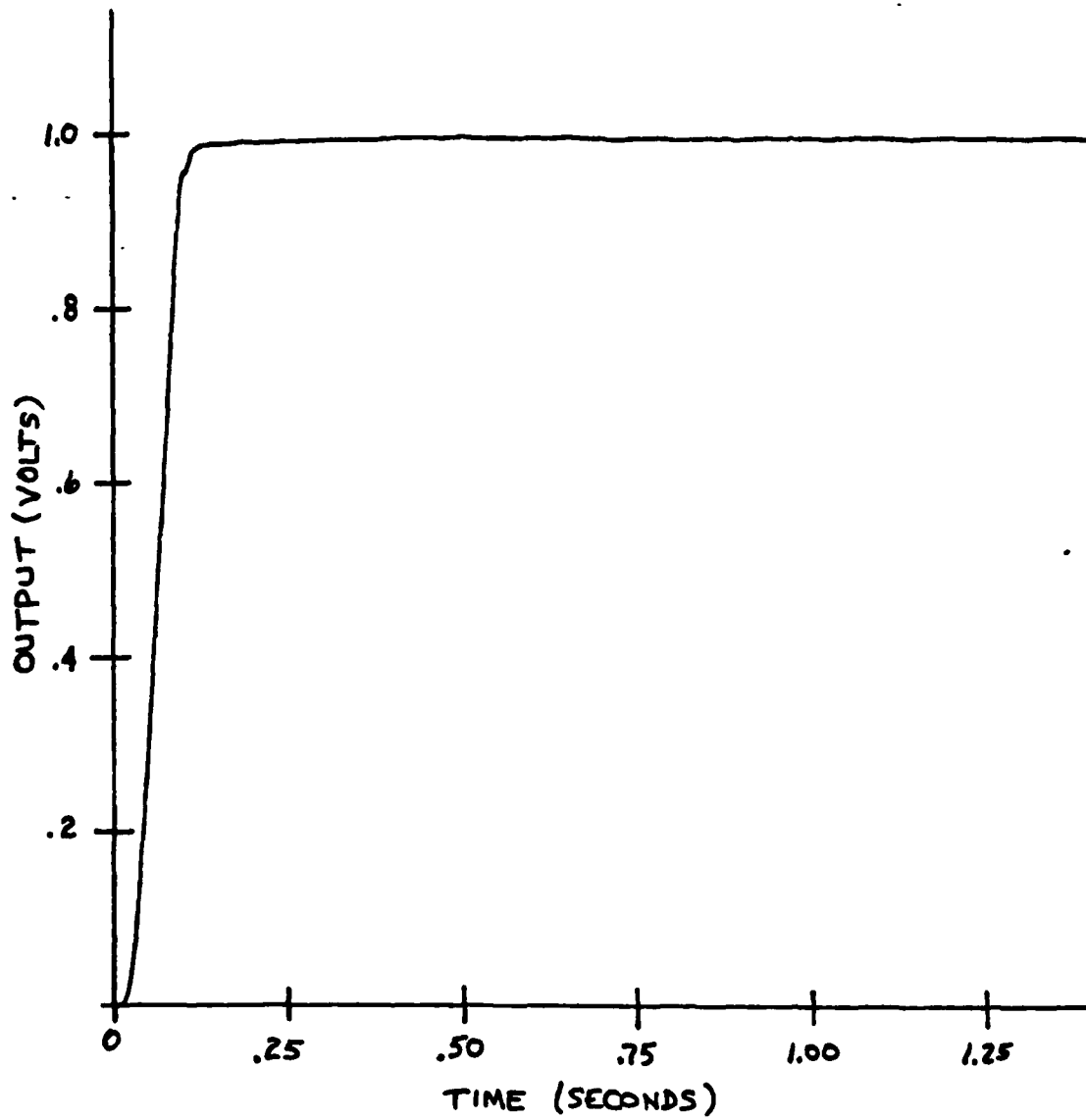


Figure 20. Unit step response of TMS 32010 plant at $T=0.15$ sec.

5.6 STATE SPACE REPRESENTATION OF THE PLANT

The characteristics of the plant can be represented in standard state space form as:

$$\dot{x} = Ax + Bu \quad (26)$$

$$y = C^T x \quad (27)$$

where

$$A = \begin{bmatrix} 0 & 1 & 0 \\ 0 & 0 & 1 \\ 0 & -300 & -40 \end{bmatrix} \quad (28)$$

$$B = \begin{bmatrix} 0 \\ 0 \\ 6000 \end{bmatrix} \quad (29)$$

$$C^T = [1 \ 0 \ 0] \quad (30)$$

The block diagram of this system is shown in Figure 21. An equivalent system can be derived by changing the B and C^T matrices slightly. The resulting matrices are:

$$B = \begin{bmatrix} 0 \\ 0 \\ 100 \end{bmatrix} \quad (31)$$

$$C^T = [60 \ 0 \ 0] \quad (32)$$

The block diagram of the alternative state space form is shown in Figure 22. The discrete state transition equations are given by:

$$X(K + 1) = \phi X(K) + \theta u(K) \quad (33)$$

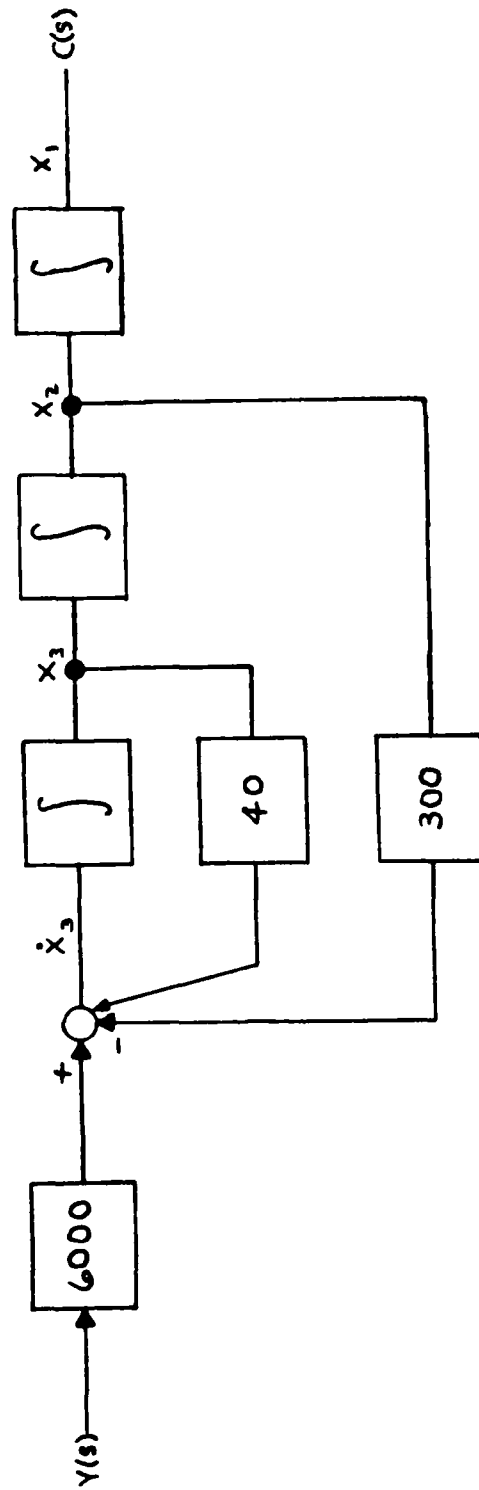


Figure 21. State space representation of the plant

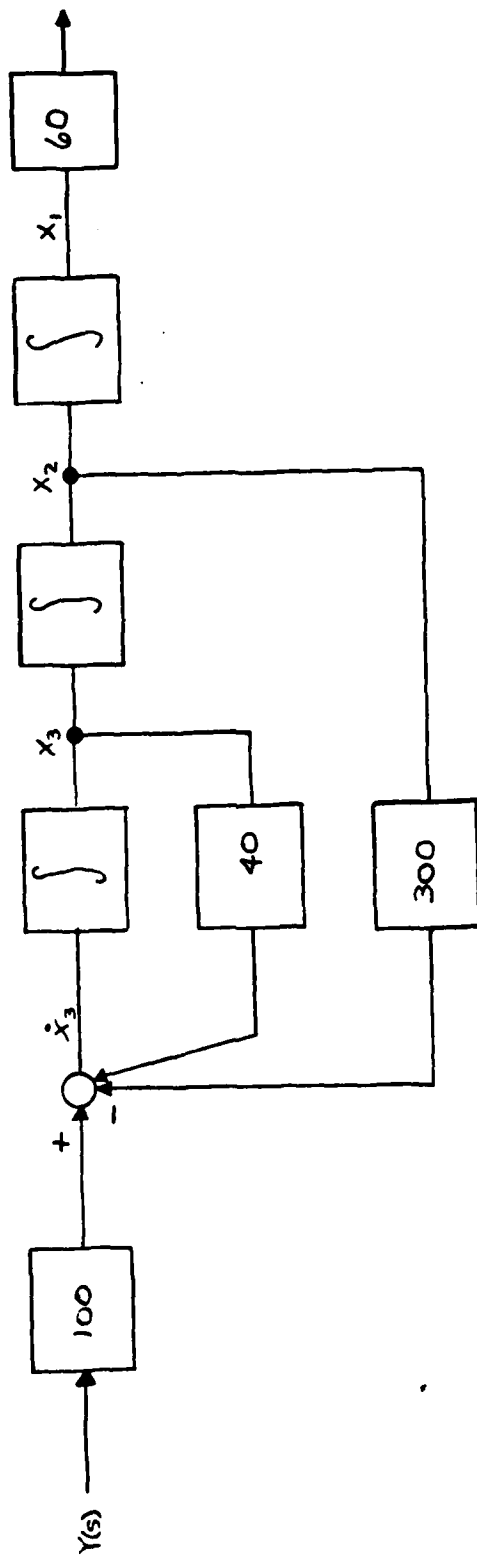


Figure 22. Alternate state space representation of the plant

$$C(K) = DX(K) \quad (34)$$

where

$$\phi = \mathcal{L}^{-1}(SI - A)^{-1} \quad (35)$$

$$\theta = \int_0^T \phi(T - \tau) B d\tau \quad (36)$$

The alternative state space representation can be implemented in the following manner. Portions of Figure 22 can be converted directly into discrete state space form. Forming a system including only the first two integrators will give:

$$A = \begin{bmatrix} 0 & 1 \\ -300 & -40 \end{bmatrix} \quad (37)$$

$$B = \begin{bmatrix} 0 \\ 100 \end{bmatrix} \quad (38)$$

Solving equation (35) and equation (36) yields:

$$\phi = \begin{bmatrix} 0.972 & 0.011 \\ -3.346 & 0.526 \end{bmatrix} \quad (39)$$

$$\theta = \begin{bmatrix} 0.009 \\ 1.115 \end{bmatrix} \quad (40)$$

The discrete state equations of this system become:

$$\begin{bmatrix} X_1(K+1) \\ X_2(K+1) \end{bmatrix} = \begin{bmatrix} 0.972 & 0.011 \\ -3.346 & 0.526 \end{bmatrix} \begin{bmatrix} X_1(K) \\ X_2(K) \end{bmatrix} + \begin{bmatrix} 0.009 \\ 1.115 \end{bmatrix} U(K) \quad (41)$$

The remaining portion of the system to be implemented is:

$$y = \frac{6\theta}{s} X_1 \quad (42)$$

Substituting equation (17) into equation (42) and using value of $T=0.015$ sec. will give:

$$y = 0.45 X_1(K) + 0.45 X_1(K-1) + y(K-1) \quad (43)$$

Equation (41) and equation (43) totally describe the system characteristics and can be implemented in software without the coefficient problems which were previously discussed. Verification of the discrete state space technique is left as an exercise for future control studies.

6.0 CONCLUSIONS

The major objective of this control study was to demonstrate the effectiveness of using 16-bit microprocessors for digital control applications. Emphasis was placed on control implementation techniques and error identification rather than control algorithm analysis. Control loop performance was measured for several hardware configurations and several control algorithm variations.

Sources of error which effect the performance of the control loop were identified. Methods were suggested which would reduce the error effects. Quantization error was the most troublesome error encountered. The use of larger bit-sized converters reduced quantization error significantly. Computation delay was shown to introduce a slight amount of error in the control loop during transients as the amount of delay increased. Computation delay did not seem to effect the steady-state behavior of the control loop. To insure proper performance, the microprocessor must be able to execute the control algorithm well within the sampling period so that the effects of the computation delay will be minimized.

The stated objectives of the control study were met. Digital control using microprocessors is practical when considering a control strategy. The increased execution speed of the DSP chips will undoubtedly make these devices even more suitable for more complex

digital control applications. It is recommended that additional control studies be performed which would exploit the full capabilities of the newer DSP chips.

APPENDIX A1

TUTOR	1.1 > MD 1000 DA;D1 (0 BIT A/D ; 0 BIT D/A) 5/1/83	
001000	46FC2000	MOVE.W #8192,SR
001004	4280	CLR.L D0
001006	7204	MOVEQ.L #4,D1
001008	207C00030000	MOVE.L #196608,A0
00100E	30C0	MOVE.W D0,(A0)+
001010	30C1	MOVE.W D1,(A0)+
001012	30C0	MOVE.W D0,(A0)+
001014	30C1	MOVE.W D1,(A0)+
001016	4440	NOT.W D0
001018	30C0	MOVE.W D0,(A0)+
00101A	30C1	MOVE.W D1,(A0)+
00101C	30C0	MOVE.W D0,(A0)+
00101E	30C1	MOVE.W D1,(A0)+
001020	13FC000000030009	MOVE.B #128,000030009
001028	203C000E4E1C	MOVE.L #937500,D0
00102E	207C00010025	MOVE.L #65573,A0
001034	01C00000	MOVEP.L D0,0000(A0)
001038	13FC000000010035	MOVE.B #0,000010035
001040	4280	CLR.L D0
001042	4281	CLR.L D1
001044	4282	CLR.L D2
001046	4283	CLR.L D3
001048	327C2000	MOVE.W #8192,A1
00104C	347C2002	MOVE.W #8194,A2
001050	367C2004	MOVE.W #8196,A3
001054	387C2010	MOVE.W #8208,A4
001058	3A7C2020	MOVE.W #8224,A5
00105C	328C3666	MOVE.W #13926,(A1)
001060	348C13B6	MOVE.W #5046,(A2)
001064	368C0A5E	MOVE.W #2654,(A3)
001068	4254	CLR.W (A4)
00106A	4255	CLR.W (A5)
00106C	13FC004000010023	MOVE.B #64,000010023
001074	21FC000010000100	MOVE.L #4232,000000100
00107C	13FC00A100010021	MOVE.B #161,000010021
001084	4E71	NOP
001086	40FC	BRA.S 0001084
001088	13FC000100010035	MOVE.B #1,000010035
001090	143900030001	MOVE.B 000030001,D2
001094	143900030001	MOVE.B 000030001,D2
00109C	0A020080	EOB.B #128,D2
0010A0	4402	NEG.B D2
0010A2	4882	EXT.W D2
0010A4	4286	CLR.L D6
0010A6	3215	MOVE.W (A5),D1
0010AB	3614	MOVE.W (A4),D3
0010AA	3882	MOVE.W D2,(A4)
0010AC	C3D1	MULS.W (A1),D1
0010AE	2C01	MOVE.L D1,D6
0010B0	C5D2	MULS.W (A2),D2
0010B2	DC82	ADD.L D2,D6
0010B4	C7D3	MULS.W (A3),D3
0010B6	9C83	SUB.L D3,D6
0010B8	E386	ASL.L #1,D6
0010BA	2A86	MOVE.L D6,(A5)
0010BC	4B14	BMI.S 00010D4
0010BE	00C40017	BSET #23,D6
0010C2	4846	SWAP.W D6
0010C4	13C400030009	MOVE.B D6,000030009
0010CA	4280	CLR.L D0
0010CC	4281	CLR.L D1
0010CE	4282	CLR.L D2
0010D0	4283	CLR.L D3

APPENDIX A2 (CONTINUED)

0010D2 4E73
0010D4 00060017
0010D8 00E8

RTE
BCLR #23,D6
BRA.S 00010C2

TUTOR 1.1 >

APPENDIX A2

TUTOR 1.1 > MD 1000 11E;D1 (8 BIT A/D , 12 BIT D/A) 5/1/83		
001000	46FC2000	MOVE.W #8192,SR
001004	4280	CLR.L D0
001006	7204	MOVEQ.L #4,D1
001008	13C000030003	MOVE.B D0,000030003
00100E	13C000030007	MOVE.B D0,000030007
001014	13C00003000B	MOVE.B D0,00003000B
00101A	13C00003000F	MOVE.B D0,00003000F
001020	13C000030001	MOVE.B D0,000030001
001026	13C100030003	MOVE.B D1,000030003
00102C	13C000030005	MOVE.B D0,000030005
001032	13C100030007	MOVE.B D1,000030007
001038	4600	NOT.B D0
00103A	13C000030009	MOVE.B D0,000030009
001040	13C10003000B	MOVE.B D1,00003000B
001046	13C00003000D	MOVE.B D0,00003000D
00104C	13C10003000F	MOVE.B D1,00003000F
001052	13FC00000003000D	MOVE.B #120,00003000D
00105A	13FC000000030009	MOVE.B #0,000030009
001062	203C000E4E1C	MOVE.L #937500,D0
001068	207C00010025	MOVE.L #65573,A0
00106E	01C00000	MOVEP.L D0,00000(A0)
001072	13FC000000010035	MOVE.B #0,000010035
00107A	4200	CLR.L D0
00107C	4281	CLR.L D1
00107E	4202	CLR.L D2
001080	4283	CLR.L D3
001082	327C2000	MOVE.W #8192,A1
001086	347C2002	MOVE.W #8194,A2
00108A	367C2004	MOVE.W #8196,A3
00108E	307C2010	MOVE.W #8200,A4
001092	3A7C2020	MOVE.W #8224,A5
001096	32BC3666	MOVE.W #13926,(A1)
00109A	34BC13B6	MOVE.W #5046,(A2)
00109E	36BC0A5E	MOVE.W #2654,(A3)
0010A2	4254	CLR.W (A4)
0010A4	4255	CLR.W (A5)
0010A6	13FC004000010023	MOVE.B #64,000010023
0010AE	21FC000010C20100	MOVE.L #4290,000000100
0010B6	13FC00A100010021	MOVE.B #161,000010021
0010BE	4E71	NOP
0010C0	60FC	BRA.S #0010BE
0010C2	13FC000100010035	MOVE.B #1,000010035
0010CA	143900030001	MOVE.B #000030001,D2
0010D0	143900030001	MOVE.B #000030001,D2
0010D6	0A020000	EOR.B #120,D2
0010DA	4402	NEG.B D2
0010DC	4002	EXT.W D2
0010DE	4206	CLR.L D6
0010E0	3215	MOVE.W (A5),D1
0010E2	3614	MOVE.W (A4),D3
0010E4	3002	MOVE.W D2,(A4)
0010E6	C3D1	MULS.W (A1),D1
0010E8	2C01	MOVE.L D1,D6
0010EA	C5D2	MULS.W (A2),D2
0010EC	DC02	ADD.L D2,D6
0010EE	C7D3	MULS.W (A3),D3
0010F0	9C83	SUB.L D3,D6
0010F2	E306	ASL.L #1,D6
0010F4	2A86	MOVE.L D6,(A5)
0010F6	4B20	BMI.S #001110
0010F8	00C60017	BSET #23,D6
0010FC	E906	ASL.L #4,D6
0010FE	4046	SWAP.W D6

APPENDIX A2 (CONTINUED)

001100	13C600030009	MOVE.B	D6,000030009
001106	E006	ASR.L	#4,D6
001108	13C60003000D	MOVE.B	D6,00003000D
00110E	4280	CLR.L	D0
001110	4281	CLR.L	D1
001112	4282	CLR.L	D2
001114	4283	CLR.L	D3
001116	4E73	RTE	
001118	00060017	BCLR	#23,D6
00111C	60DE	BRA.S	00010FC

TUTOR 1.1 >

APPENDIX A3

```

TUTOR 1.1 > MD 1000 144;DI ( 12 BIT A/D ; 12 BIT D/A ) 5/1/83
001000 46FC2000 MOVE.W #8192,6R
001004 4200 CLR.L D0
001006 7204 MOVEQ.L #4,D1
001008 740F MOVEQ.L #15,D2
00100A 13C000030003 MOVE.B D0,000030003
001010 13C000030007 MOVE.B D0,000030007
001016 13C00003000B MOVE.B D0,00003000B
00101C 13C00003000F MOVE.B D0,00003000F
001022 13C000030001 MOVE.B D0,000030001
001028 13C100030003 MOVE.B D1,000030003
00102E 13C200030005 MOVE.B D2,000030005
001034 13C100030007 MOVE.B D1,000030007
00103A 4600 NOT.B D0
00103C 13C000030009 MOVE.B D0,000030009
001042 13C10003000B MOVE.B D1,00003000B
001048 13C00003000D MOVE.B D0,00003000D
00104E 13C10003000F MOVE.B D1,00003000F
001054 13FC00000003000D MOVE.B #128,00003000D
00105C 13FC000000030009 MOVE.B #0,000030009
001064 203C000E4E1C MOVE.L #937500,D0
00106A 207C00010025 MOVE.L #65573,A0
001070 01C00000 MOVEP.L D0,00000(A0)
001074 13FC000000010035 MOVE.B #0,000010035
00107C 4200 CLR.L D0
00107E 4201 CLR.L D1
001080 4202 CLR.L D2
001082 4203 CLR.L D3
001084 4207 CLR.L D7
001086 327C2000 MOVE.W #8192,A1
00108A 347C2002 MOVE.W #8194,A2
00108E 367C2004 MOVE.W #8196,A3
001092 307C2010 MOVE.W #8200,A4
001096 3A7C2020 MOVE.W #8224,A5
00109A 32BC3666 MOVE.W #13926,(A1)
00109E 34BC13B6 MOVE.W #5046,(A2)
0010A2 36BC0A5E MOVE.W #2654,(A3)
0010A6 4254 CLR.W (A4)
0010A8 4255 CLR.W (A5)
0010AA 13FC004000010023 MOVE.B #64,000010023
0010B2 21FC000010C60100 MOVE.L #4294,000000100
0010BA 13FC00A100010021 MOVE.B #161,000010021
0010C2 4E71 NOP
0010C4 60FC BRA.S 00010C2
0010C6 13FC000100010035 MOVE.B #1,000010035
0010CE 13FC000F00030005 MOVE.B #15,000030005
0010D6 13FC000000030005 MOVE.B #0,000030005
0010DE 7E06 MOVEQ.L #6,D7
0010E0 5307 SUBQ.L #1,D7
0010E2 64FC BNE.S 00010E0
0010E4 143900030005 MOVE.B 000030005,D2
0010EA 143900030005 MOVE.B 000030005,D2
0010F0 0A020000 EOR.B #128,D2
0010F4 4002 EXT.W D2
0010F6 E942 ASL.W #4,D2
0010F8 143900030001 MOVE.B 000030001,D2
0010FE 143900030001 MOVE.B 000030001,D2
001104 4206 CLR.L D6
001106 3215 MOVE.W (A5),D1
001108 3614 MOVE.W (A4),D3
00110A 3002 MOVE.W D2,(A4)
00110C C3D1 MULS.W (A1),D1
00110E 2C01 MOVE.L D1,D6

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APPENDIX A3 (CONTINUED)

001110	C9D2	MULS.W	(A2),D2
001112	DC82	ADD.L	D2,D6
001114	C7D3	MULS.W	(A3),D3
001116	9C83	SUB.L	D3,D6
001118	E386	ASL.L	#1,D6
00111A	2A86	MOVE.L	D6,(A5)
00111C	6B1E	IMI.S	00113C
00111E	08C6001B	BSET	#27,D6
001122	4846	SWAP.W	D6
001124	13C600030009	MOVE.B	D6,000030009
00112A	E886	ASR.L	#4,D6
00112C	13C60003000D	MOVE.B	D6,00003000D
001132	4280	CLR.L	D0
001134	4281	CLR.L	D1
001136	4282	CLR.L	D2
001138	4283	CLR.L	D3
00113A	4287	CLR.L	D7
00113C	4E73	RTE	
00113E	0806001B	BCLR	#27,D6
001142	60E8	BRA.S	001124

APPENDIX A4

		MD 1000 14E,DI (COMPUTATIONAL DELAY-7/2/64)
001000	46FC2000	MOVE.W #B192,SR
001004	4200	CLR.L D0
001006	7204	MOVEQ.L #4,D1
001008	740F	MOVEQ.L #15,D2
00100A	13C000030003	MOVE.B D0,\$00030003
001010	13C000030007	MOVE.B D0,\$00030007
001016	13C00003000B	MOVE.B D0,\$0003000B
00101C	13C00003000F	MOVE.B D0,\$0003000F
001022	13C000030001	MOVE.B D0,\$00030001
001028	13C100030003	MOVE.B D1,\$00030003
00102E	13C200030005	MOVE.B D2,\$00030005
001034	13C100030007	MOVE.B D1,\$00030007
00103A	4600	NOT.B D0
00103C	13C000030009	MOVE.B D0,\$00030009
001042	13C10003000B	MOVE.B D1,\$0003000B
001048	13C00003000D	MOVE.B D0,\$0003000D
00104E	13C10003000F	MOVE.B D1,\$0003000F
001054	13FC00000003000D	MOVE.B #120,\$0003000D
00105C	13FC000000030009	MOVE.B #0,\$00030009
001064	203C000E4E1C	MOVE.L #937500,D0
00106A	207C00010025	MOVE.L #65573,A0
001070	01C00000	MOVEP.L D0,\$0000(A0)
001074	13FC000000010035	MOVE.B #0,\$00010035
00107C	4200	CLR.L D0
00107E	4201	CLR.L D1
001080	4202	CLR.L D2
001082	4203	CLR.L D3
001084	4207	CLR.L D7
001086	327C2000	MOVE.W #B192,A1
00108A	347C2002	MOVE.W #B194,A2
00108E	367C2004	MOVE.W #B196,A3
001092	387C2010	MOVE.W #B200,A4
001096	3A7C2020	MOVE.W #B224,A5
00109A	32BC3664	MOVE.W #13926,(A1)
00109E	34BC13B6	MOVE.W #5046,(A2)
0010A2	36BC0A5E	MOVE.W #2654,(A3)
0010A6	4254	CLR.W (A4)
0010A8	4255	CLR.W (A5)
0010AA	13FC004000010023	MOVE.B #64,\$00010023
0010B2	21FC000010C60100	MOVE.L #4294,\$00000100
0010BA	13FC000A100010021	MOVE.B #161,\$00010021
0010C2	4E71	NOP
0010C4	60FC	BRA.S \$0010C2
0010C6	13FC000100010035	MOVE.B #1,\$00010035
0010CE	13FC000F00030005	MOVE.B #15,\$00030005
0010D6	13FC000000030005	MOVE.B #0,\$00030005
0010DE	7E06	MOVEQ.L #6,D7
0010E0	5387	SUBQ.L #1,D7
0010E2	66FC	BNE.S \$0010E0
0010E4	143900030005	MOVE.B \$00030005,D2
0010EA	143900030005	MOVE.B \$00030005,D2
0010F0	0A020000	EOR.B #120,D2
0010F4	4802	EXT.W D2
0010F6	E942	ASL.W #4,D2
0010F8	143900030001	MOVE.B \$00030001,D2
0010FE	143900030001	MOVE.B \$00030001,D2
001104	4206	CLR.L D6
001106	3215	MOVE.W (A5),D1
001108	3614	MOVE.W (A4),D3
00110A	38B2	MOVE.W D2,(A4)
00110C	C3D1	MULS.W (A1),D1
00110E	2C01	MOVE.L D1,D6
001110	C5D2	MULS.W (A2),D2
001112	DC02	ADD.L D2,D6

APPENDIX A4 (CONTINUED)

001114	C7D3	MULS.W	(A3),D3
001116	9C83	SUB.L	D3,D6
001118	E386	ASL.L	#1,D6
00111A	2A86	MOVE.L	D6,(A5)
00111C	6B2A	BMI.S	*001148
00111E	08C6001B	BSET	#27,D6
001122	2E3C000D3464	MOVE.L	#865380,D7
001128	5387	SUBQ.L	#1,D7
00112A	66FC	BNE.S	*001128
00112C	4846	SWAP.W	D6
00112E	13C600030009	MOVE.B	D6,*00030009
001134	E886	ASR.L	#4,D6
001136	13C60003000D	MOVE.B	D6,*0003000D
00113C	4280	CLR.L	D8
00113E	4281	CLR.L	D1
001140	4282	CLR.L	D2
001142	4283	CLR.L	D3
001144	4287	CLR.L	D7
001146	4E73	RTE	
001148	0886001B	BCLR	#27,D6
00114C	60DE	BRA.S	*00112C

TUTOR 1.1 >

APPENDIX A5

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TUTOR 1.1 > MD 1000 170;D1 (ROUNDOFF-7/6/84;M;JG)
001000 46FC2000 MOVE.W #8192,SR
001004 4280 CLR.L D0
001006 7204 MOVEQ.L #4,D1
001008 740F MOVEQ.L #15,D2
00100A 13C000030003 MOVE.B D0,$00030003
001010 13C000030007 MOVE.B D0,$00030007
001016 13C00003000B MOVE.B D0,$0003000B
00101C 13C00003000F MOVE.B D0,$0003000F
001022 13C000030001 MOVE.B D0,$00030001
001028 13C100030003 MOVE.B D1,$00030003
00102E 13C200030005 MOVE.B D2,$00030005
001034 13C100030007 MOVE.B D1,$00030007
00103A 4400 NOT.B D0
00103C 13C000030009 MOVE.B D0,$00030009
001042 13C10003000B MOVE.B D1,$0003000B
001048 13C00003000D MOVE.B D0,$0003000D
00104E 13C10003000F MOVE.B D1,$0003000F
001054 13FC00000003000D MOVE.B #120,$0003000D
00105C 13FC000000030009 MOVE.B #0,$00030009
001064 203C000E4E1C MOVE.L #937500,D0
00106A 207C00010025 MOVE.L #65573,A0
001070 01C00000 MOVEP.L D0,$0000(A0)
001074 13FC000000010035 MOVE.B #0,$00010035
00107C 4280 CLR.L D0
00107E 4281 CLR.L D1
001080 4282 CLR.L D2
001082 4283 CLR.L D3
001084 4287 CLR.L D7
001086 327C2000 MOVE.W #8192,A1
00108A 347C2002 MOVE.W #8194,A2
00108E 367C2004 MOVE.W #8196,A3
001092 387C2010 MOVE.W #8208,A4
001096 3A7C2020 MOVE.W #8224,A5
00109A 32BC3644 MOVE.W #13926,(A1)
00109E 34BC13B6 MOVE.W #5046,(A2)
0010A2 36BC0A5E MOVE.W #2654,(A3)
0010A6 4254 CLR.W (A4)
0010AB 4255 CLR.W (A5)
0010AA 13FC004000010023 MOVE.B #64,$00010023
0010B2 21FC000010C60100 MOVE.L #4294,$00000100
0010BA 13FC00A100010021 MOVE.B #161,$00010021
0010C2 4E71 NOP
0010C4 60FC BRA.S $0010C2
0010C6 13FC000100010035 MOVE.B #1,$00010035
0010CE 13FC000F00030005 MOVE.B #15,$00030005
0010D6 13FC000000030005 MOVE.B #0,$00030005
0010DE 7E06 MOVEQ.L #6,D7
0010E0 5307 SUBQ.L #1,D7
0010E2 66FC BNE.S $0010E0
0010E4 143900030005 MOVE.B $00030005,D2
0010EA 143900030005 MOVE.B $00030005,D2
0010F0 0A020000 EOR.B #120,D2
0010F4 40B2 EXT.W D2
0010F6 E942 ASL.W #4,D2
0010F8 143900030001 MOVE.B $00030001,D2
0010FE 1439A0030001 MOVE.B $00030001,D2
001104 4206 CLR.L D6
001106 3215 MOVE.W (A5),D1
001108 3614 MOVE.W (A4),D3
00110A 30B2 MOVE.W D2,(A4)
00110C C3D1 MULS.W (A1),D1
00110E 2C01 MOVE.L D1,D6
001110 C5D2 MULS.W (A2),D2
001112 DC82 ADD.L D2,D6

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APPENDIX A5 (CONTINUED)

001114	C7D3	MULS.W	(A3),D3
001116	9C83	SUB.L	D3,D6
001118	E386	ASL.L	#1,D6
00111A	2A86	MOVE.L	D6,(A5)
00111C	6B2A	BMI.S	*001148
00111E	0806000F	BTST	#15,D6
001122	673C	BEQ.S	*001160
001124	5255	ADDQ.W	#1,(A5)
001126	4846	SWAP.W	D6
001128	5246	ADDQ.W	#1,D6
00112A	08C6000B	BSET	#11,D6
00112E	13C600030009	MOVE.B	D6,*00030009
001134	E886	ASR.L	#4,D6
001136	13C60003000D	MOVE.B	D6,*0003000D
00113C	4280	CLR.L	D0
00113E	4281	CLR.L	D1
001140	4282	CLR.L	D2
001142	4283	CLR.L	D3
001144	4287	CLR.L	D7
001146	4E73	RTE	
001148	0806000F	BTST	#15,D6
00114C	661A	BNE.S	*001168
00114E	0C470000	CMP.W	#0,D7
001152	6714	BEQ.S	*001160
001154	5355	SUBQ.W	#1,(A5)
001156	4846	SWAP.W	D6
001158	5346	SUBQ.W	#1,D6
00115A	0886000B	BCLR	#11,D6
00115E	60CE	BRA.S	*00112E
001160	08C6001B	BSET	#27,D6
001164	4846	SWAP.W	D6
001166	60C6	BRA.S	*00112E
001168	0886001B	BCLR	#27,D6
00116C	4846	SWAP.W	D6
00116E	608E	BRA.S	*00112E

TUTOR 1.1 >

APPENDIX A6

** TMS320 EVM ASSEMBLER **

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>
00010 000 * THIS PROGRAM IMPLEMENTS THE UNIT STEP RESPONSE OF
00020 000 * THE CLOSED-LOOP, UNCOMPENSATED PLANT. THE PLANT
00030 000 * IS DIGITIZED USING THE TUSTIN TRANSFORM WITH T=.15 SEC.
00040 000 * PROGRAM WRITTEN BY: MICHAEL J. GAUDER 11/12/84
00050 000 * ADRG 3 START PROGRAM AT ADDR 0003
00060 003 *
00070 003 * SYSTEM EQUATES AND DATA ASSIGNMENTS
00080 003 *
00090 003 0000 ZERO DATA >0000 ZERO
00100 004 0001 ONE DATA >0001 ONE
00110 005 0004 FOUR DATA >0004 FOUR
00120 006 0008 EIGHT DATA >0008 SAMPLE DELAY/CONT. CONVERSION
00130 007 0005 SAMRT DATA >0005 SAMPLE PERIOD 0.010 SEC APPR.
00140 008 7FF0 MASK1 DATA >7FF0 MASK FOR INPUT DATA
00150 009 B000 MASK2 DATA >B000 MASK FOR OUTPUT DATA
00160 00A PA0 EQU 0 PORT ADDR FOR A/D CONTROL PORT
00170 00A PA1 EQU 1 PORT ADDR FOR SAMPLE RATE PORT
00180 00A PA2 EQU 2 PORT ADDR FOR A/D AND D/A
00190 00A *
00200 00A * COEFFICIENTS FOR DIFFERENCE EQUATION
00210 00A *
00220 00A CCEE A0 DATA >CCEE FP VALUE FOR NORMALIZED A0
00230 00B A3F9 A1 DATA >A3F9 FP VALUE FOR NORMALIZED A1
00240 00C D3B7 A2 DATA >D3B7 FP VALUE FOR NORMALIZED A2
00250 00D 2746 A3A6 DATA >2746 FP VALUE FOR NORMALIZED A3&A6
00260 00E 7645 A4A5 DATA >7645 FP VALUE FOR NORMALIZED A4&A5
00270 00F *
00280 00F * VARIABLE STORAGE
00290 00F *
00300 00F ** Y VALUES **
00310 00F TEMP BSS 1 TEMP Y(K) LOC.
00320 010 Y1 BSS 1 Y(K-1)
00330 011 Y2 BSS 1 Y(K-2)
00340 012 Y3 BSS 1 Y(K-3)
00350 013 ** X VALUES **
00360 013 X0 BSS 1 X(K)
00370 014 X1 BSS 1 X(K-1)
00380 015 X2 BSS 1 X(K-2)
00390 016 X3 BSS 1 X(K-3)
00400 017 *
00410 017 * INITIALIZE THE VARIABLE STORAGE TO ZERO
00420 017 *
00430 017 4E00 LDPK 0 LOAD DATA POINTER WITH 0
00440 018 7007 LARK 0,7 LOAD AUX. REG 0 WITH COUNT
00450 019 7E03 LACK ZERO LOAD STARTING VARIABLE ADDR
00460 01A 6703 TBLR ZERO INIT D.M.
00470 01B 710F LARK 1,TEMP START OF DATA STORAGE
00480 01C 6881 CVB LARP 1 AUX. REG. POINTER SET TO 1
00490 01D 67A0 TBLR *+,0 CLEAR MEM. LOC./INC. ADDR/ARP=0
00500 01E F400 BANZ CVB CONT. UNTIL ARO = 0
00510 020 *
00520 020 * INITIALIZE DATA MEMORY WITH CONTROL VALUES
00530 020 *
00540 020 7E04 LACK ONE LOAD ACC WITH ADDR OF ONE
00550 021 6704 TBLR ONE STORE PH INTO DM
00560 022 7009 LARK 0,9 LOAD AUX. REG 0 WITH COUNT
00570 023 7105 LARK 1,FOUR AUX. HAS STARTING D.M. ADDR
00580 024 7E05 LACK FOUR ACC HAS START ADDR FOR INIT
00590 025 6881 CDI LARP 1 AUX. REG. POINTER = 1
00600 026 67A0 TBLR *+,0 MOVE PH TO DM/INC DM POINTER

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APPENDIX A6 (CONTINUED)

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00610 027 0004          ADD  ONE          INC PH POINTER
00620 02B F400          BANZ CDI          CONT. UNTIL DONE
029 0025
00630 02A              *
00640 02A              * ANALOG BOARD INITIALIZATION
00650 02A              *
00660 02A 700F          LARK 0,>000F      LOAD ARO WITH COUNT FOR SAMPLE
00670 02B 4907          OUT  SAMRT,PA1    SET UP SAMPLE CLOCK
00680 02C 4806          OUT  MODE,PA0     SET UP MODE; START CLOCK
00690 02D              *
00700 02D              * WAIT FOR DATA TO BE CONVERTED
00710 02D              *
00720 02D F600          WAIT  BIOZ CNTDWN    START COUNTDOWN WHEN BIO = 0
02E FFFF
00730 02F F900          B      WAIT        WAIT UNTIL BIO = 0 BEFORE CONT.
030 002D
00740 031 6B80          CNTDWN LARP 0      LOAD AR POINTER WITH ZERO
00750 032 F400          BANZ WAIT        IF ARO NE ZERO,GO BACK TO WAIT
033 002D
00760 034 700F          LARK 0,>000F      RESET COUNTDOWN REGISTER
00770 035              *
00780 035              * READ DATA AND CONVERT TO TRUE BINARY
00790 035              *
00800 035 7F89          CALC  ZAC          CLEAR ACCUMULATOR
00810 036 4213          IN   X0,PA2       INPUT DATA FROM A/D
00820 037 2013          LAC  X0           LOAD ACC FROM X(K)
00830 038 7B0B          XOR  MASK1        COMPLEMENT SIGN BIT
00840 039 5013          SACL X0           STORE TRUE BIN AT X(K)
00850 03A 7F89          ZAC              CLEAR ACC.
00860 03B              *
00870 03B              * CALCULATE DIFFERENCE EQUATION
00880 03B              *
00890 03B 6A12          LT   Y3           Y(K-3) IN T REG
00900 03C 6D0C          MPY  A2           A2*Y(K-3)
00910 03D 6B11          LTD  Y2           Y(K-3)=Y(K-2)+ACC SUM
00920 03E 6D0B          MPY  A1           A1*Y(K-2)
00930 03F 6B10          LTD  Y1           Y(K-2)=Y(K-1)+ACC SUM
00940 040 6D0A          MPY  A0           A0*Y(K-1)
00950 041 6C16          LTA  X3           ACC SUM+X(K-3) IN T REG
00960 042 6D0D          MPY  A3A6        A6*X(K-3)
00970 043 6B15          LTD  X2           X(K-3)=X(K-2)+ACC SUM
00980 044 6D0E          MPY  A4A5        A5*X(K-2)
00990 045 6B14          LTD  X1           X(K-2)=X(K-1)+ACC SUM
01000 046 6D0E          MPY  A4A5        A4*X(K-1)
01010 047 6B13          LTD  X0           X(K-1)=X(K)+ACC SUM
01020 04B 6D0D          MPY  A3A6        A3*X(K)
01030 049 7FBF          APAC             ACC NOW HAS Y(K)
01040 04A 590F          SACH TEMP,1     TEMP=Y(K)
01050 04B 200F          LAC  TEMP        LOAD ACC WITH TEMP
01060 04C 5010          SACL Y1         STORE RESULT IN Y(K-1)
01070 04D 7B09          XOR  MASK2       COMPLEMENT SIGN BIT
01080 04E 500F          SACL TEMP       SAVE VALUE IN TEMP
01090 04F 4A0F          OUT  TEMP,PA2   DATA OUT TO D/A
01100 050 F900          B      WAIT      GO AND GET NEXT SAMPLE
051 002D
01110 052              END

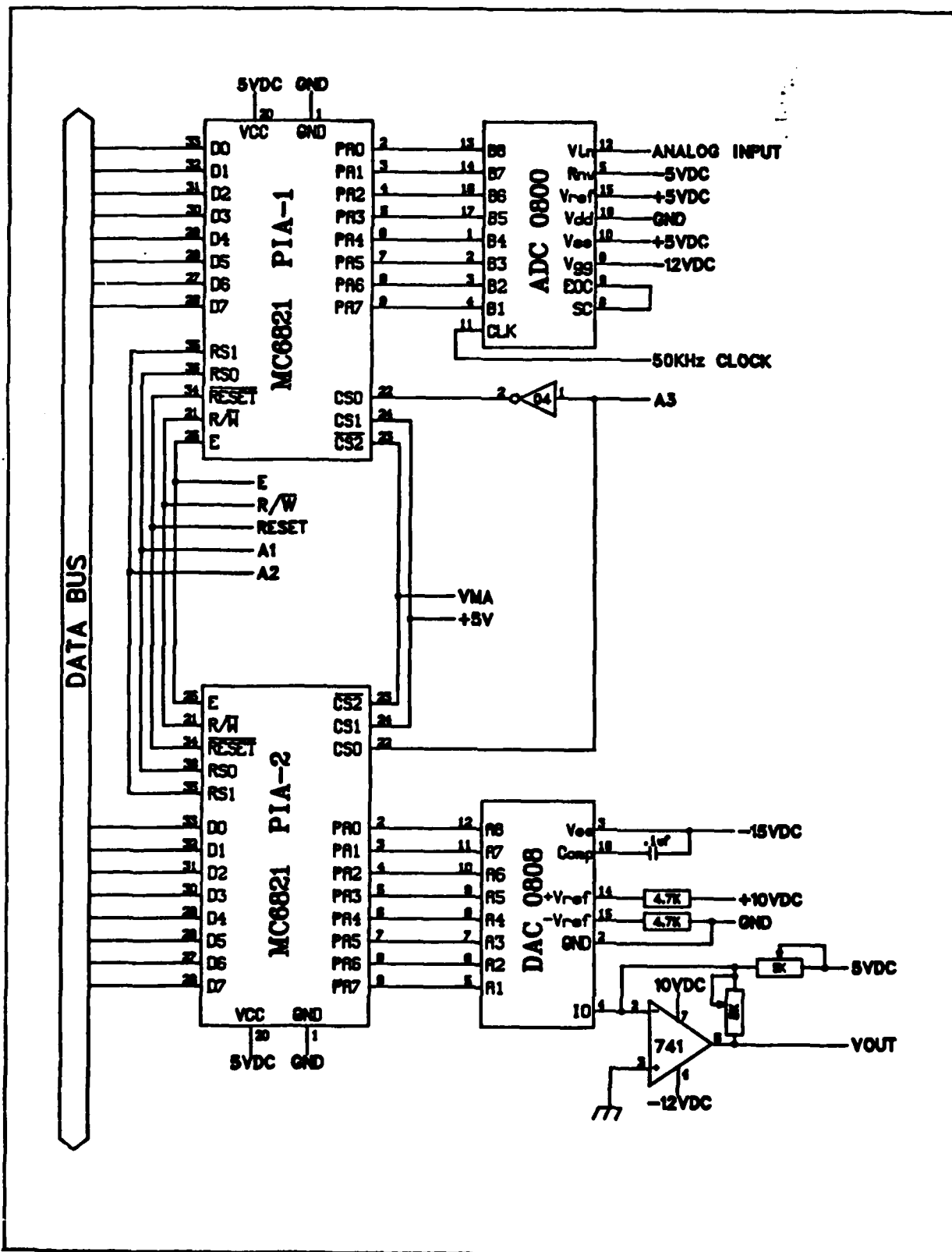
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NUMBER OF ERRORS 00000

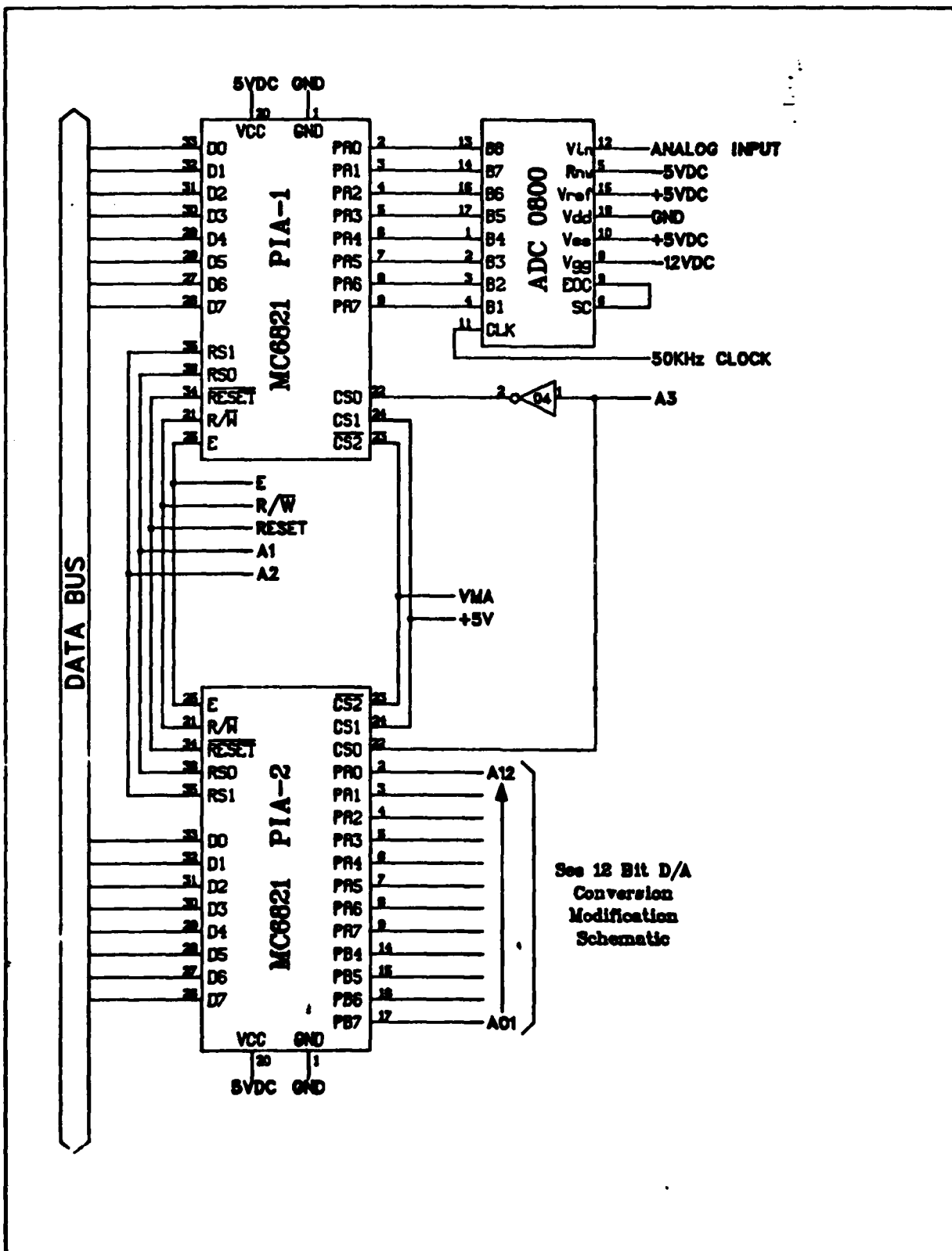
NUMBER OF WARNINGS 00000

ASSEMBLY COMPLETE

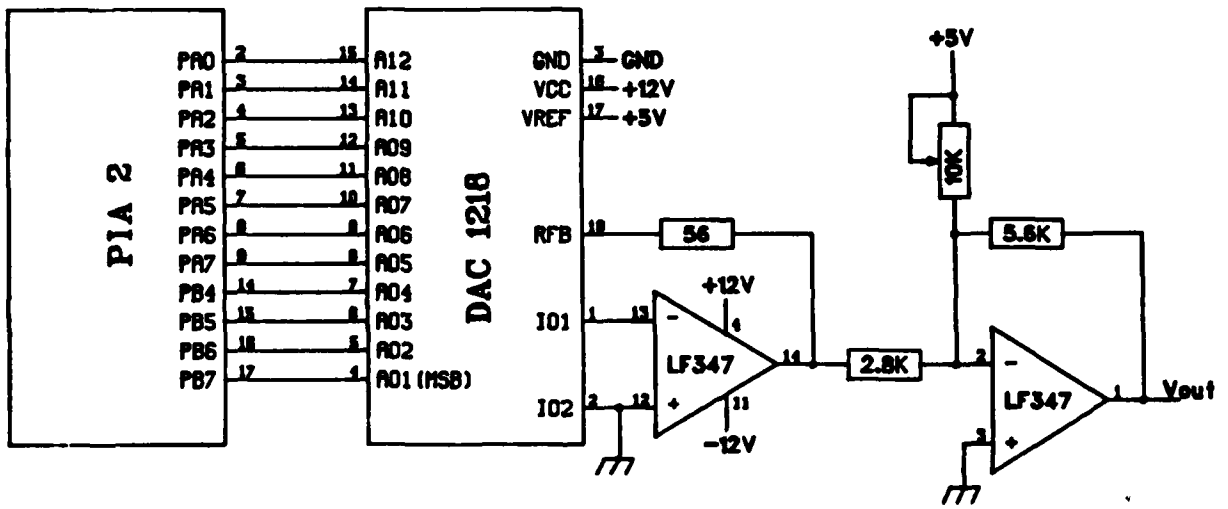
APPENDIX B1



APPENDIX B2

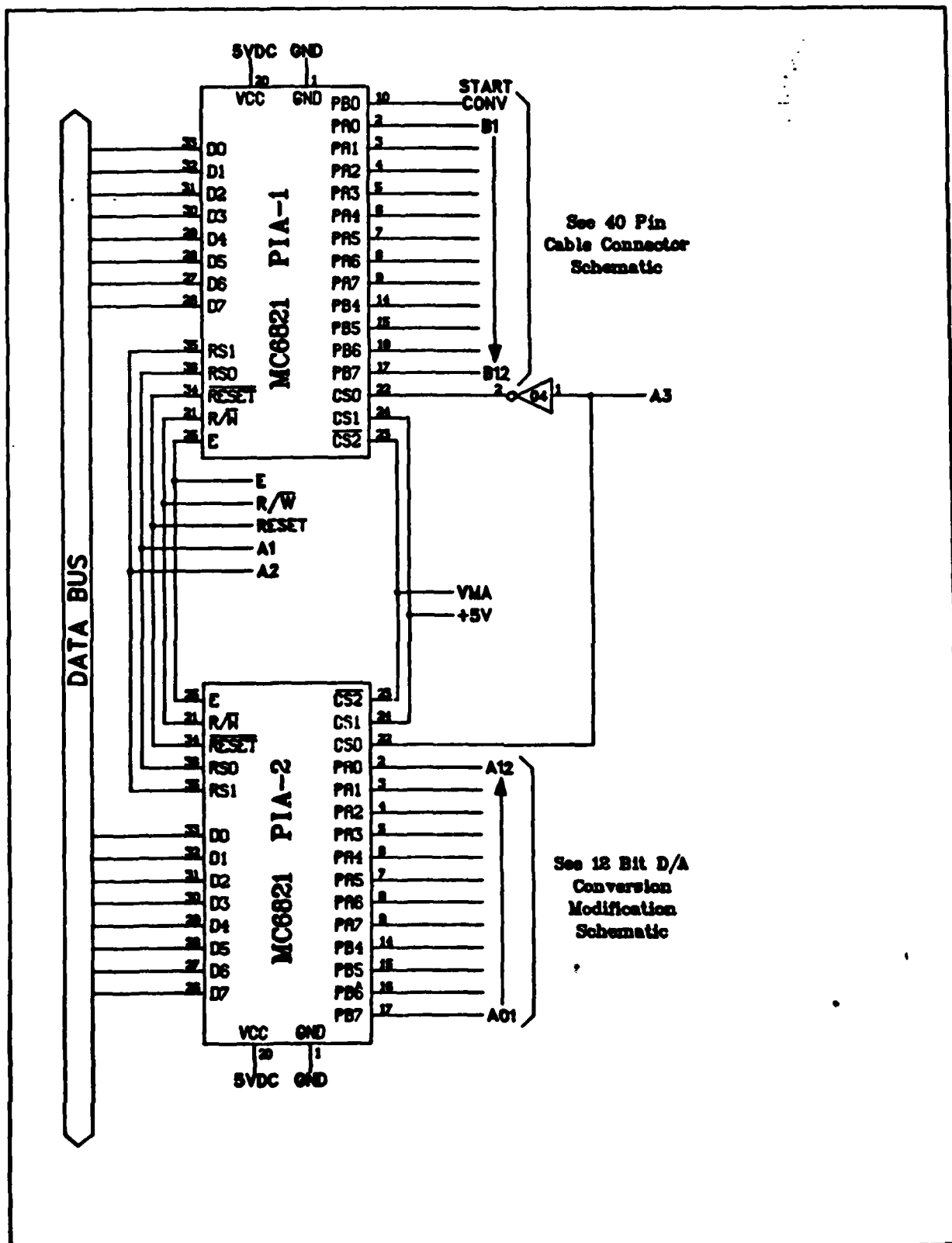


APPENDIX B2 (CONTINUED)

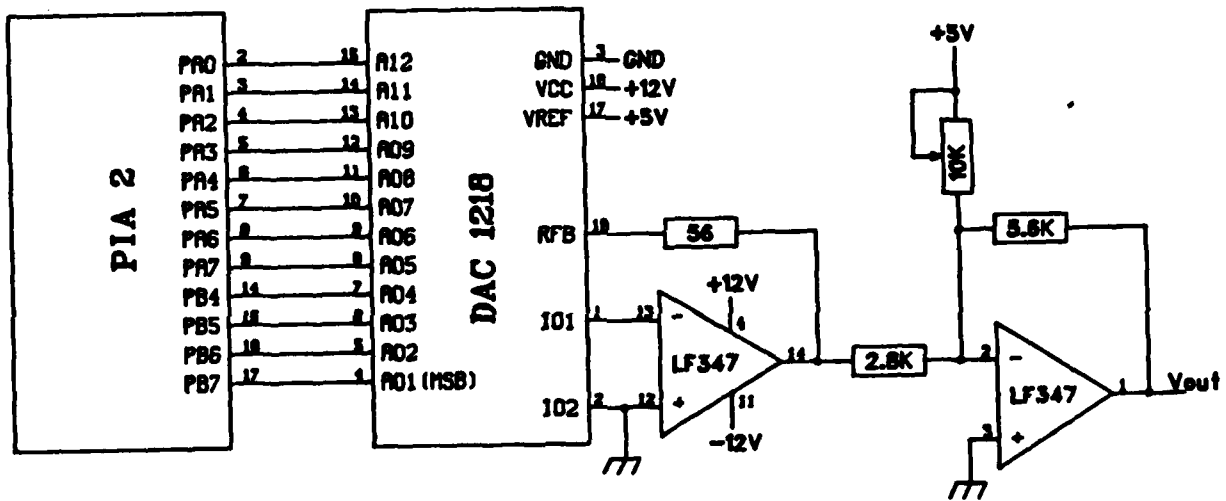


MODIFICATION TO CONTROLLER
FOR 12 BIT D/A CONVERTER

APPENDIX B3

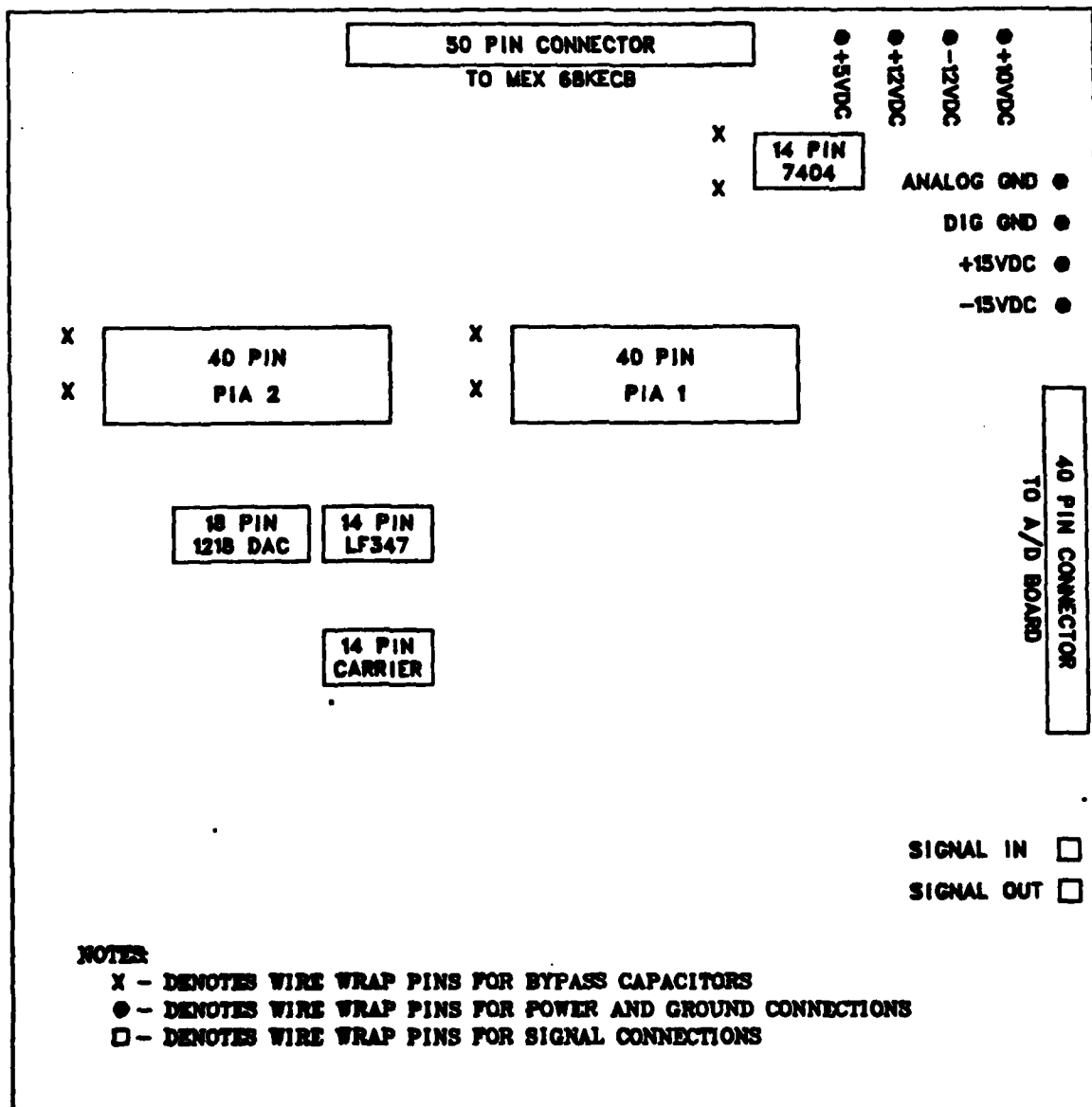


APPENDIX B3 (CONTINUED)



MODIFICATION TO CONTROLLER
FOR 12 BIT, D/A CONVERTER

APPENDIX B3 (CONTINUED)



APPENDIX B3 (CONTINUED)

40 PIN RIBBON CONNECTOR
ON WIRE WRAP INTERFACE BOARD
TO A/D MOTHERBOARD

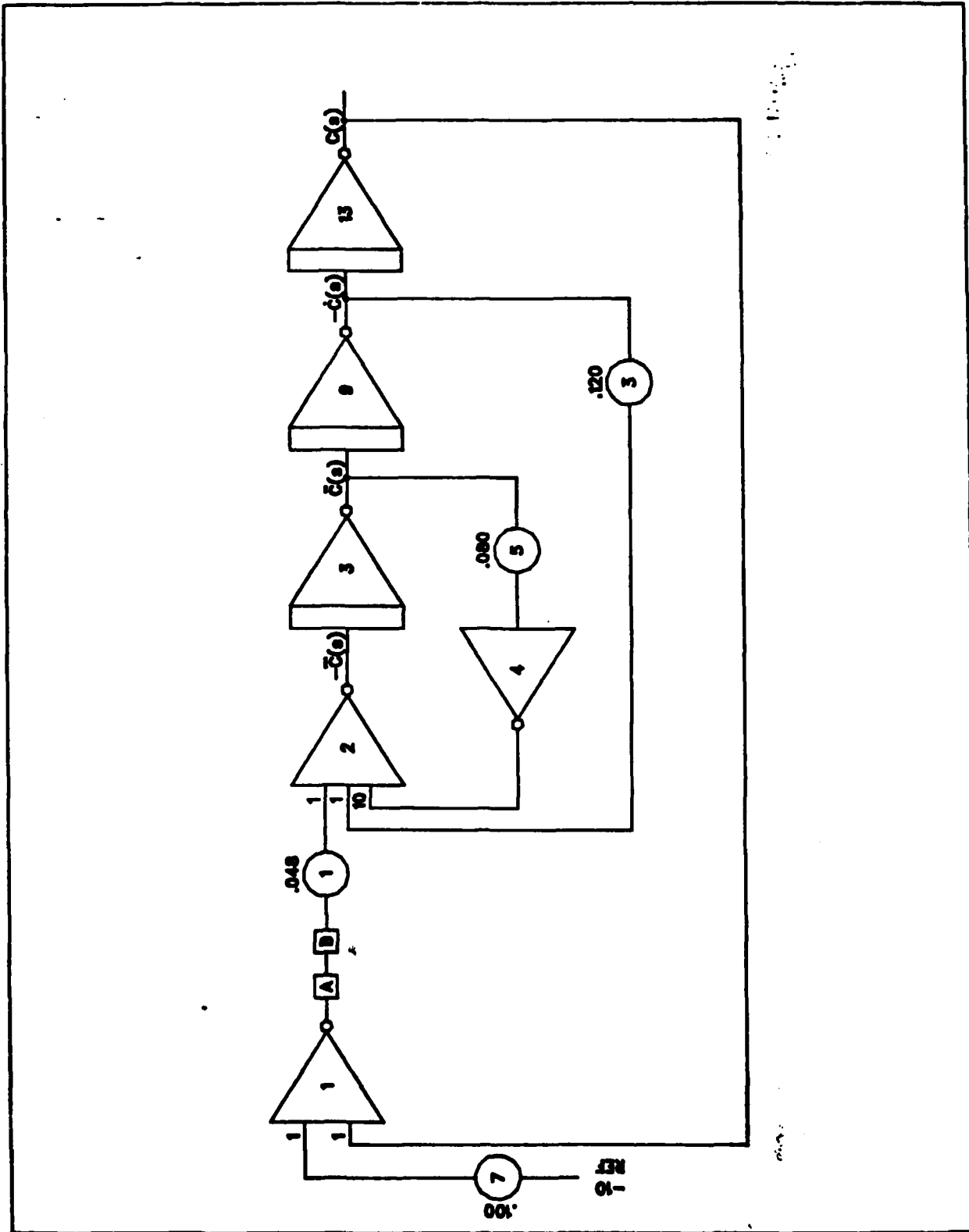
GROUND	1	2	B12 (LSB)
+15VDC	3	4	B11
-15VDC	5	6	B10
+10VDC	7	8	B09
ANALOG IN	9	10	B08
	11	12	B07
START CONV	13	14	B06
	15	16	B05
	17	18	B04
	19	20	B03
	21	22	B02
	23	24	B01 (MSB)
	25	26	
	27	28	
	29	30	
	31	32	
	33	34	
	35	36	
	37	38	
	39	40	

50 PIN RIBBON CONNECTOR ON WIRE WRAP INTERFACE BOARD TO MEX68KECB CPU BOARD

D04	1	2	D03
D05	3	4	D02
D06	5	6	4 MHz CLOCK
D07	7	8	D14
D08	9	10	D15
D09	11	12	RESET \bar{M}
D10	13	14	DD1
D11	15	16	E
D12	17	18	PS \bar{M}
D13	19	20	UDS \bar{M}
D00	21	22	LDS \bar{M}
A15	23	24	R/W \bar{M}
A14	25	26	A13
A12	27	28	FC2
A11	29	30	FC1
A10	31	32	FC0
A09	33	34	AD1
A08	35	36	AD2
A06	37	38	AD3
A07	39	40	AD4
A05	41	42	DTACK \bar{M}
8 MHz CLOCK	43	44	6800 IRD \bar{M}
1 MHz CLOCK	45	46	VPA \bar{M}
	47	48	
	49	50	PROTO BD GND

\bar{M} - ACTIVE LOW

APPENDIX C1



REFERENCES

1. Rattan, K. S.: "Computer-Aided Design of Sampled-Data Control Systems via Complex-Curve Fitting," Dissertation, University of Kentucky, 1975.
2. Hartke, P. V.: "Hardware Implementation and Error Analysis of a Digital Control Loop," Master's Thesis, Wright State University, 1981.
3. Kuo, B. C.: Digital Control Systems, Holt, Rinehart and Winston, Inc., New York, 1980.
4. Katz, P.: Digital Control Using Microprocessors, Prentice-Hall International, New Jersey, 1981.
5. James, M. L.; Smith G. M.; Wolford, J. C.: Analog Computer Simulation of Engineering Systems, Intext Educational Publishers, Scranton, 1971.
6. MC68000 16-Bit Microcompressor User's Manual, 2nd Ed., Motorola Semiconductor Products, Inc., 1980.
7. MC68000 Educational Computer Board User's Manual, 2nd Ed., Motorola Semiconductor Products, Inc., 1982.
8. TMS32010 User's Guide, Texas Instruments, Inc., 1983.
9. TMS32010 Assembly Language Programmer's Guide, Texas Instruments, Inc., 1983.
10. TMS32010 Evaluation Module, Texas Instruments, Inc., 1983.
11. TMS32010 Analog Interface Board, Texas Instruments, Inc., 1983.
12. Gauder, M. J.; Rattan, K. S.; Sarwal, A.: "Microcompressor Based System for Evaluating Frequency Response of a Digital Control System," Paper, National Aerospace Electronics Conference (NAECON), 1983.

END

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