⑨ *Final rept.*

NAVAL RESEARCH LABORATORY
4555 Overlook Avenue, S.W.
Washington, D.C. 20375

FINAL REPORT
Contract Number N00173-76-C-0132
⑮

⑥ **PIN DIODE TRADE-OFF STUDY FOR BROADBAND HIGH POWER FAST SWITCHING SPEED MICROWAVE SWITCHES**

⑩ BY
John Moran
Project Engineer

T.W. Carr
Manager
ECM Control Devices

⑫ 109 p.

⑪ January 1979

D D C
RECEIVED
JUN 7 1979
E

Microwave Associates
A M/ACOM COMPANY
Burlington, M

79 05 30

229 400

TABLE OF CONTENTS

i   79 05 30 223

LIST OF TABLES

LIST OF FIGURES

LIST OF FIGURES (cont.)

PHASE I

DIODE STUDY PROGRAM

Background

The contract was for the investigation of fundamental PIN diode switching speed and RF power handling trade-offs. The program was conducted in two phases. The first phase was to determine the characteristics of PIN diodes. This characterization was conducted experimentally with I-region thickness as the prime variable. Each diode type was evaluated in terms of its inherent power handling capabilities and switching characteristics. The equivalent circuit parameters for each diode type were also compiled to determine the frequency response of proposed switch designs. The second phase of the program was to develop a series of broadband switches which would incorporate the design information generated from the initial effort, and compare the results.

Diodes ranging from 2 microns to 100 microns thickness I-region were utilized. Their static characteristics were determined and samples of each were designed into single chip all-shunt SPST switch circuits. These were then subjected to various switching speed and high power RF tests at three frequencies in the microwave spectrum.

The results from the diode study led to the generation of specifications for five switches. These units were constructed, tested and delivered with summary data included in this document. This portion of the investigation put into practical application the test results from Phase I.

Investigation - Static Diode Data

The final selection of diodes to be utilized for this study was determined somewhat by current engineering practice. The range was open, but thickness extremes were chosen to include the thinnest PIN (2 microns) and one which was thick enough (100 microns) to exceed the capabilities of available test equipment. Available diodes of comparable physical and electrical paramters dictated the following selection

1	2 micron I-layer	
2	8 micron I-layer	
3	18 micron I-layer	
4	30 micron I-layer	(1 mil)
5	50 micron I-layer	(2 mil)
6	100 micron I-layer	(4 mil)

Static measurements were run on forty diodes of each type to determine consistency and to ascertain the design parameters for RF use. Table I summarizes this data.

In reference to Table 1, the voltage breakdown (V_B) range signifies the minimum and maximum values for the forty piece sample. The distribution was quite uniform, with approximately 80% falling in the middle 50% of the range and the remainder being spread on both sides of the major portion. Thus, a selection process could reduce the V_B variation by 50% with only a 20% parts shrinkage. This parameter is an indication of power/speed performance. A thin diode has a small intrinsic volume and cannot store much charge (low V_B). This results in rapid recombination, and faster switching speeds. However, the small volume also results in lower power handling capabilities since the higher current density causes the junction to heat more rapidly when the diode is in the forward conducting state. In the reverse bias state, the voltage breakdown level can also be exceeded by lower RF voltages compared to that of a thicker diode. This fact is the crux of this investigation where several diodes of varying thicknesses were selected to determine exactly what speed and power trade-offs can be established. In contrast to the previous discussion for thin diodes, thick diodes exhibit large breakdowns with voltage, resulting in larger power handling, but are slower in speed.

Diode capacitance determines the upper frequency limit for broadband PIN diode switches. The diode capacitance can be utilized in two ways. In the first case, the diode shunts the transmission line and series inductance is added to optimize an equivalent low pass filter. The filter cutoff is inversely proportional to the diode capacitance. The second circuit type uses the diode in series with the transmission

line. In this case, the diode capacitance acts as a series blocking
element and dependent on the absolute blocking or isolation required,
the high frequency cutoff is inversely proportional to diode capaci-
tance. To maximize the power handling capability of any PIN diode,
it is important to mount the diode to a heat sink surface. As shunt
mounted PIN diodes are soldered directly to the massive ground plane,
excellent cooling is achieved. This is not possible for series mounted
diodes as both terminals of the diode have to be attached to the center
conductor making significant heat sinking unlikely. For this reason,
a high power requirement dictates the necessity of a shunt diode design.

Diode TYPE NUMBER	M/A SLICE REFERENCE	THICKNESS (MICRONS)	VOLTAGE BREAKDOWN (VOLTS)	CAPACITANCE (pf)			FORWARD RESISTANCE (Ohms)-8 GHz		LIFETIME 10mA/10V (n Sec)
				10V	20V	50V	10mA	50mA	
1	L-35A	2	26-34	.13-.15	N/A	N/A.	1.2-1.4	1.2-1.4	10-20
2	X-507E	8	150-180	.09-.10	.09-.10	.09-.10	1.5-1.7	1.4-1.5	110-130
3	RL-31	18	280-350	.09-.11	.09-.11	.09-.11	1.3-1.5	1.2-1.4	300-350
4	X-184C	30	400-500	.16-.18	.16-.18	.16-.18	0.9-1.2	0.6-0.9	750-900
5	SG-137	50	700-850	.18-.21	.16-.20	.15-.18	1.3-1.5	1.0-1.2	1600-1800
6	SG-263	100	1300-1500	.28-.33	.22-.26	.19-.23	1.9-2.0	1.2-1.3	2700-3100

TABLE 1 DIODE STATIC DATA

Consistency is also important for capacitance. Type 1 through Type 4 diodes are excellent for this parameter. Varying the voltage over a 5:1 range results in no significant change in capacitance. Type 5 showed a moderate change, and Type 6 showed a large variation. However, diodes of that thickness would not be employed at low bias voltages. As such, they are well within a useful range for normal usage at 30 to 50 volts reverse bias.

Forward resistance (R_S) is a major factor in RF high power burnout. The I^2R heating causes the diode junction to burn out due to excessive junction temperature in the order of 150°C or greater. The current is a combination of bias current and current from the incident RF signal. Under CW conditions, this current is easily calculated, but pulsed conditions must take into account the cooling intervals between pulses. If the RF pulse is very long, for example, greater than 100 micro-seconds, the diode will be heated to its maximum regardless of the cooling period between pulses. To assure proper evaluation of all diodes in this study, a pulse width of 1.0 microseconds was chosen. This is a commonly used value and is much less than the thermal time constant of all diodes under consideration. The R_S was measured at two bias current levels, 10mA and 50mA. This trade-off yields the following benefits and detriments. At lower current levels, the stored charge is lower and the diode can be switched faster. The major detriment is the higher R_S associated with the lower current. This results in higher power dissipation within the junction due to the increased I^2R losses for a given current. It can be seen that this adds a third dimension to the speed/power trade-off and will be discussed in detail under the section on dynamic measurements for these diodes.

Lifetime (the time it takes for minority carriers to recombine) is proportional to the speed that can be achieved with a diode. Because

the tests were actually run on these chips, the lifetime was recorded for reference only. Actually, switching speed is strongly dependent on driver waveforms, which must be optimized for fastest possible switching speed.

Several other points should be discussed for clarity. The actual diode thickness is not easily controlled. Processing, doping, and environmental changes all contribute to slight variations in the final value. Therefore, the thickness as recorded should not be taken as absolute, but as close approximations for comparision purposes. All diodes were passivated. Types 1 through 4 were Silicon-dioxide passivated, and Types 5 and 6 were hard-glass passivated. Both are acceptable in military environments. Finally, the slice number is an M/A internal control number which gives a unique identity to every processing run for PIN diodes.

Investigation - Dynamic Diode Data

As discussed in the previous section, the various diode thicknesses result in different stored charge and a wide range of switching speed capabilities. To exploit the switching capabilities, an injected waveform must be produced. This waveform is of the opposite polarity of the stored charge when removing it, and is of the same polarity when inducing carriers.

Figure 1 presents a typical pulse as produced by a driver to create the desired switching action in a PIN diode. In effect, the TTL driver circuit stores internal charge which is several times that to be removed from the PIN diode. At the reception of a gated signal, the transistors change state, and the stored charge is impressed on the diode. With reference to Figure 1, the speed with which the signal reaches its maximum value (Ip) is the risetime. The duration of the spiking pulse is the pulse width. This curve represents the amount of energy avail-
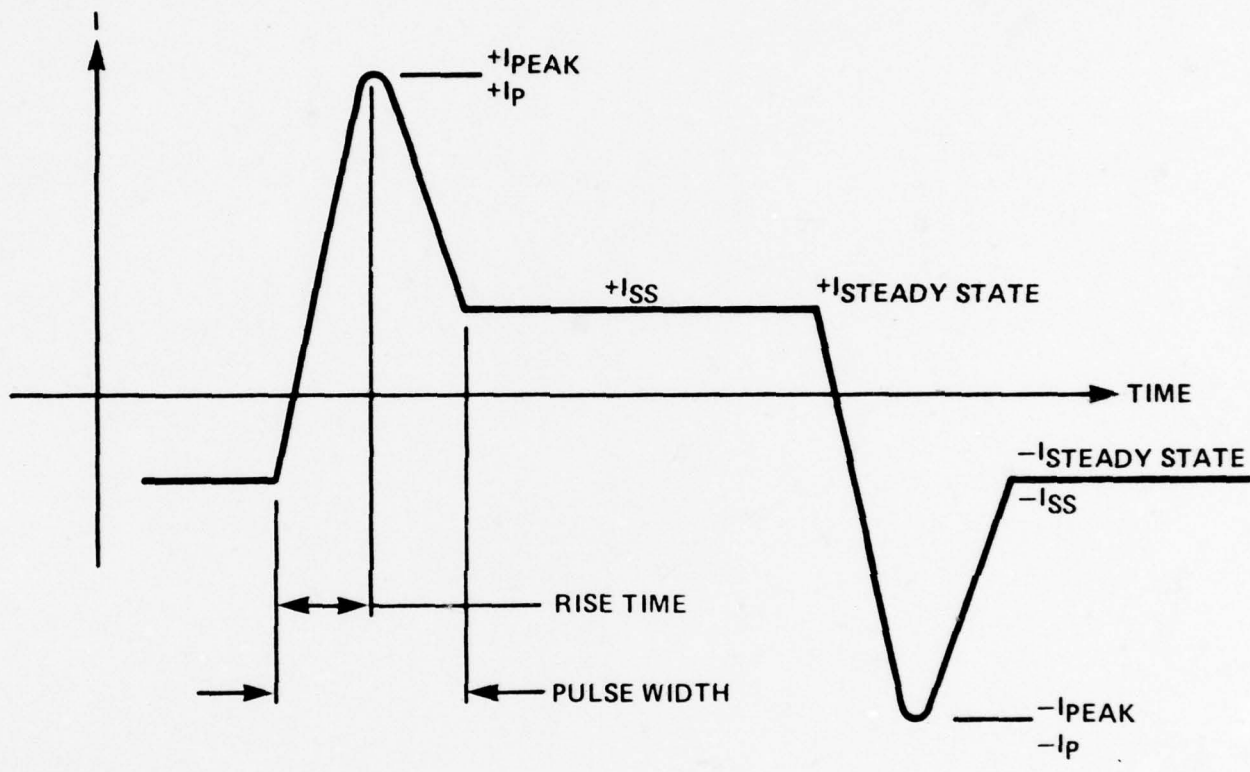
FIGURE 1. TYPICAL DRIVER OUTPUT PULSE

D-16942

able to remove the stored charge in the PIN diode. When the charge is removed, the driver supplied the specified steady-state bias (Iss) until the gated signal at the driver input is reversed. At this time, the diode is forces into the opposite state by spiking in the reverse polarity

An important consideration encountered when designing a driver is to produce adequate spiking for thick diodes. Transistors with 50 to 100 volt breakdowns must be utilized. They provide the necessary gain and current capability to remove large charge, but unfortunately, the response time is slower. Conversely, the drivers with faster response times cannot provide adequate pulse outputs to clear the charge from thick diodes, but will be much faster for thin diodes. Microwave Associates produced two drivers for this study. Type A was optimized for speed with a 2 micron diode. Type B was designed to switch the 4 mil diode. Figures 2 and 3 show schematic diagrams for these driver circuits. In the data summary, the crossover in speed is very apparent, whereby the slower but more powerful driver becomes beneficial for switching the thicker I-region diodes.

All switching speed data was taken at room temperature on a single chip SPST switch for each diode type. The mounting structures were identical, and the data was taken by the same technician on the same test set. The results are presented in Table 2. It can be seen that Driver A exhibits less delay time for diodes Type 1 through 3. However, the injection of carriers (risetime) is accomplished more quickly with Driver B for Type 3 only. As the diode thickness increases to Type 4, the high voltage driver can create faster rise and fall times, and less delay. Clearly, the tradeoff is at 20-25 microns. Continuing to Types 5 and 6, the output pulse from Driver B is clearly superior to that of Driver A.

Referring to Table 2, four parameters are recorded in each test. The RF risetime and RF falltime are the 10%-90% times for the detected RF pulse. The total rise speed and total full speed also includes the driver delay from the 50% point of the initial command. The actual driver delay is the difference between the total rise (fall) speed and the RF risetime (falltime).

- 8 -
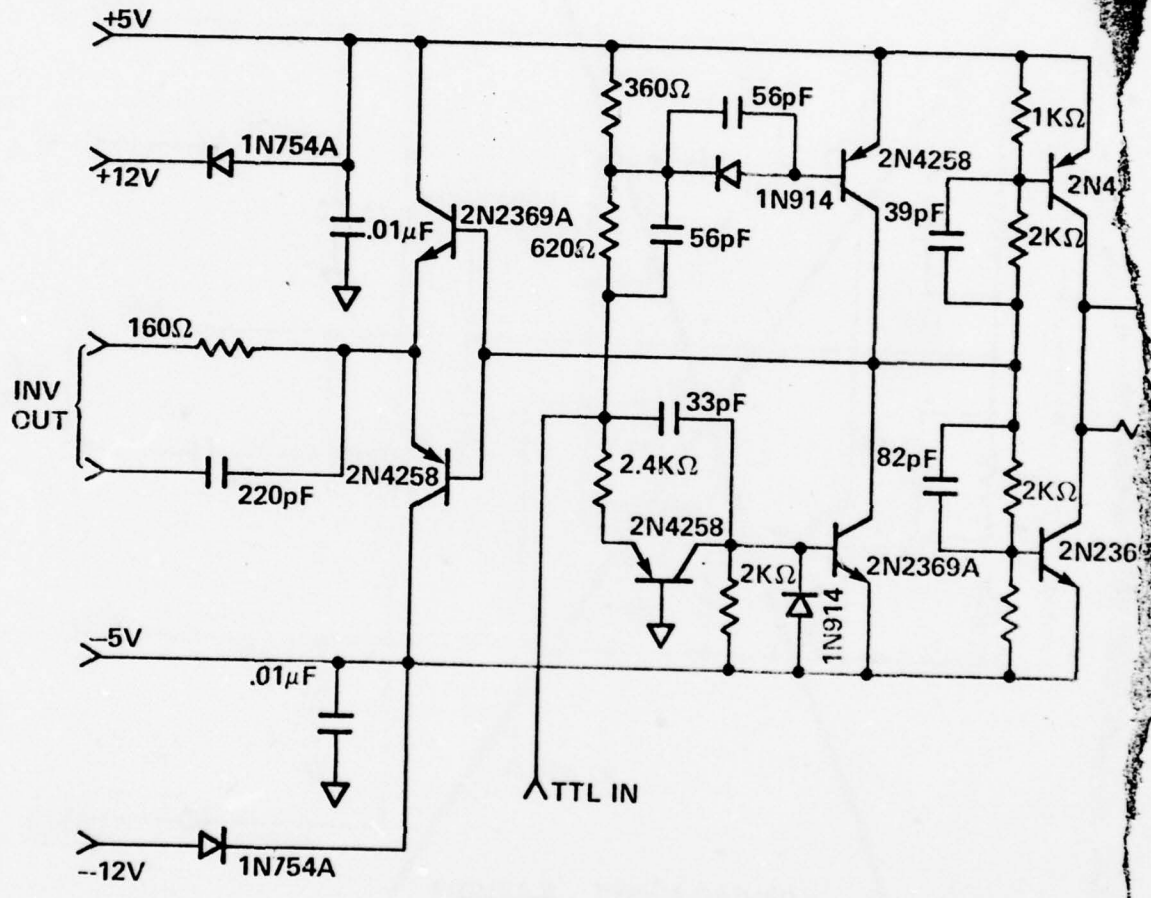
FIGURE 2. TYPE A DRIVER
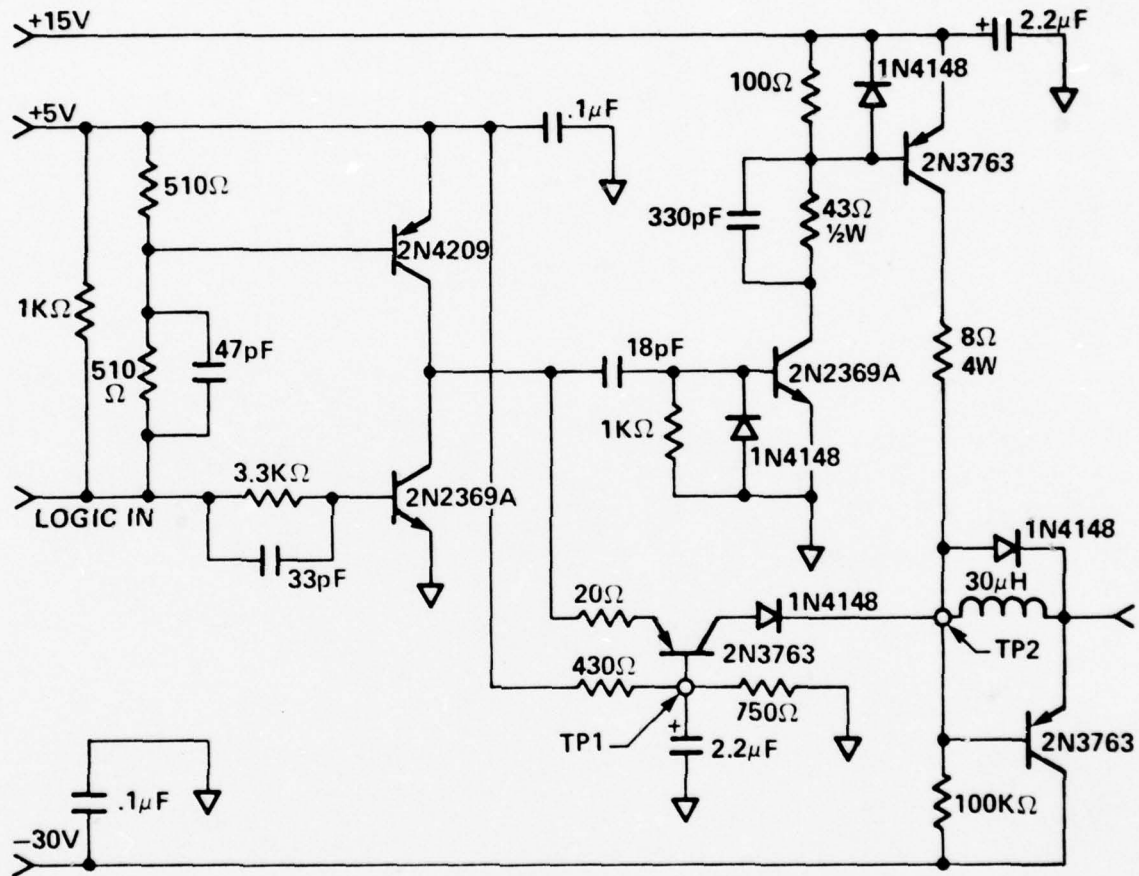
FIGURE 3.   TYPE B DRIVER

D-16944

-10-

DIODE TYPE Number	DRIVER TYPE A				DRIVER TYPE B			
	RISETIME	TOTAL RISE SPEED	FALLTIME	TOTAL FALL SPEED	RISETIME	TOTAL RISE SPEED	FALLTIME	TOTAL FALL SPEED
1	2-3	6-9	2-3	6-9	N/A	N/A	N/A	N/A
2	3-6	10-17	3-6	10-17	5-9	8-10	15-20	40-45
3	8-10	25-29	8-10	25-29	6-7	22-35	20-22	60-75
4	23-28	300-320	45-50	330-350	10-11	120-160	25-28	160-200
5	80-100	760-835	105-125	800-875	24-37	275-470	40-55	325-520
6	500-800	3000-4000	600-900	3500-4300	140-200	1100-2100	180-260	1200-2200

*All speeds in Nanoseconds

TABLE 2 SWITCHING SPEED DATA

It should be noted that there are other distinct differences between the two test drivers. These are noted below:

Driver A

Bias supplies	+5V and -5V
Rep Rate	10 MHz
Output Voltage	4.3V (+ and -)

Driver B

Bias Supplies	+5V, +15V, and -35V
Rep Rate	500 KHz
Output Voltage	+14.3V and -34.3V

Additionally, the difference in complexity results in a cost increase of approximately 3:1 for the Type B driver.

Investigation - High Power RF Tests

With the information available on switching speed, the other investigative parameter, RF power was included. To gain maximum frequency coverage, and use the available facilities, the frequencies of 1 GHz, 9 GHz and 18 GHz were selected as test frequencies. At each frequency, the following tests were conducted:

1. Burn-out power (peak and average) at -5V reverse bias.
2. Burn-out power (peak and average) at -30V reverse bias.
3. Burn-out power (peak and average) at +10mA forward bias.
4. Burn-out power (peak and average) at +50mA forward bias
5. Conductivity modulation (dB compression) at -5V reverse bias
6. Conductivity modulation (dB compression) at -30V reverse bias

The burn-out and compression data were taken for CW and pulse conditions. In some cases power was not available and under no conditions did the power exceed an incident level of 10kW, because of connector/equipment/circuit stress versus diode stress which was the program intent. As shown in the following data, there is considerable difference between burn-out levels on the same diode depending on whether the diode is forward biased or reverse biased. From a thermal burn-out viewpoint, the line impedance of the switching structure could always be adjusted to equalize the dissipated power in the two states. This impedance change would band limit the device and since the program was dedicated to broad band devices, all testing was done in 50 ohm systems.

The curves of Figures 4, 5, 6, 7, 8 and 9 were generated to depict comparison data of peak power performance for the various thicknesses of diode I-regions as frequency is varied. It must be considered that
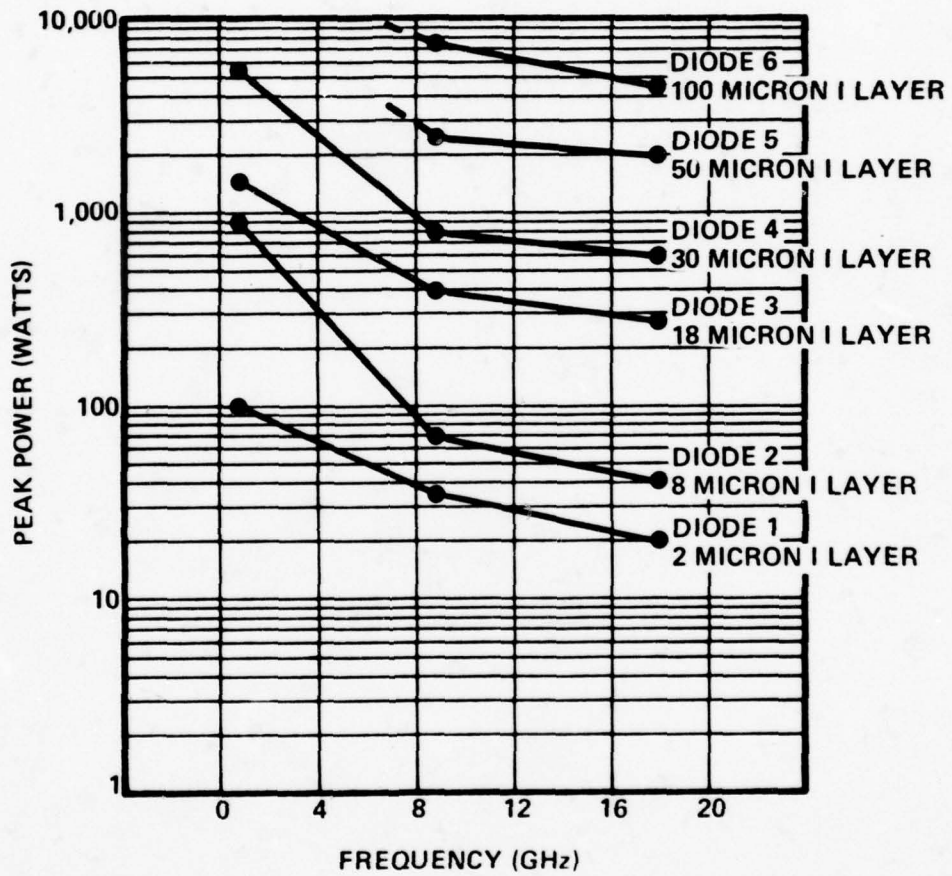
FIGURE 4. PEAK BURNOUT AT --5V BIAS

D-16945
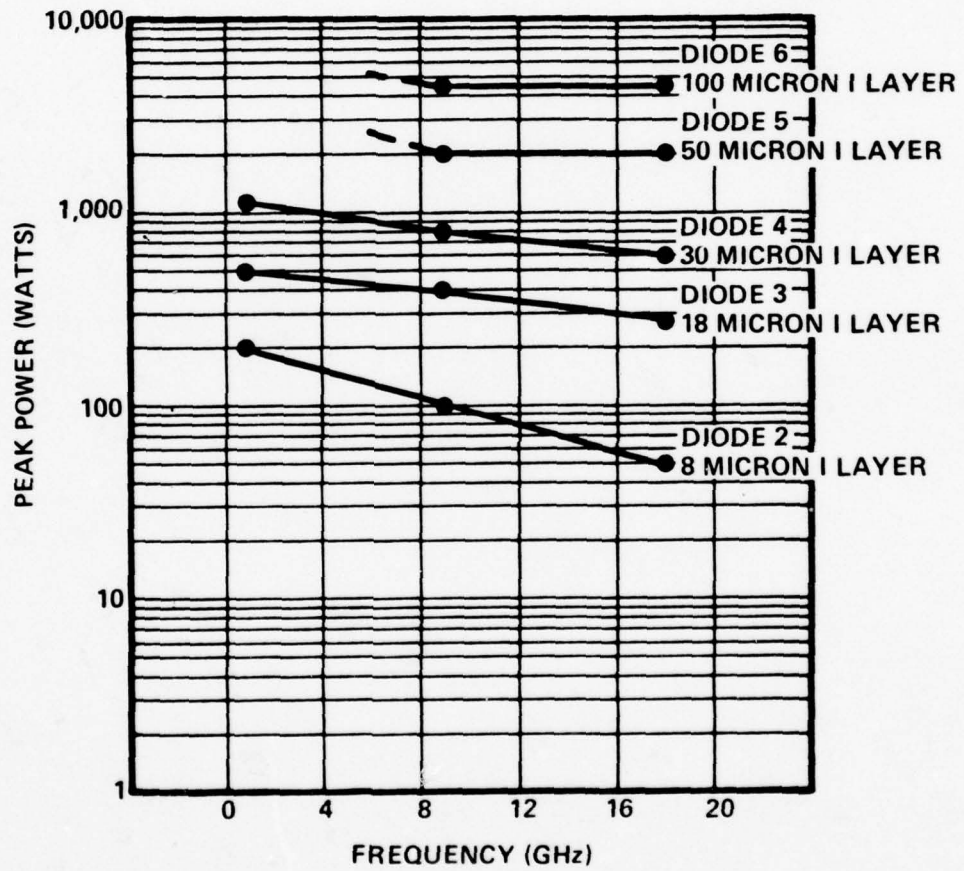
FIGURE 5. PEAK BURNOUT AT −30V BIAS

D-16946
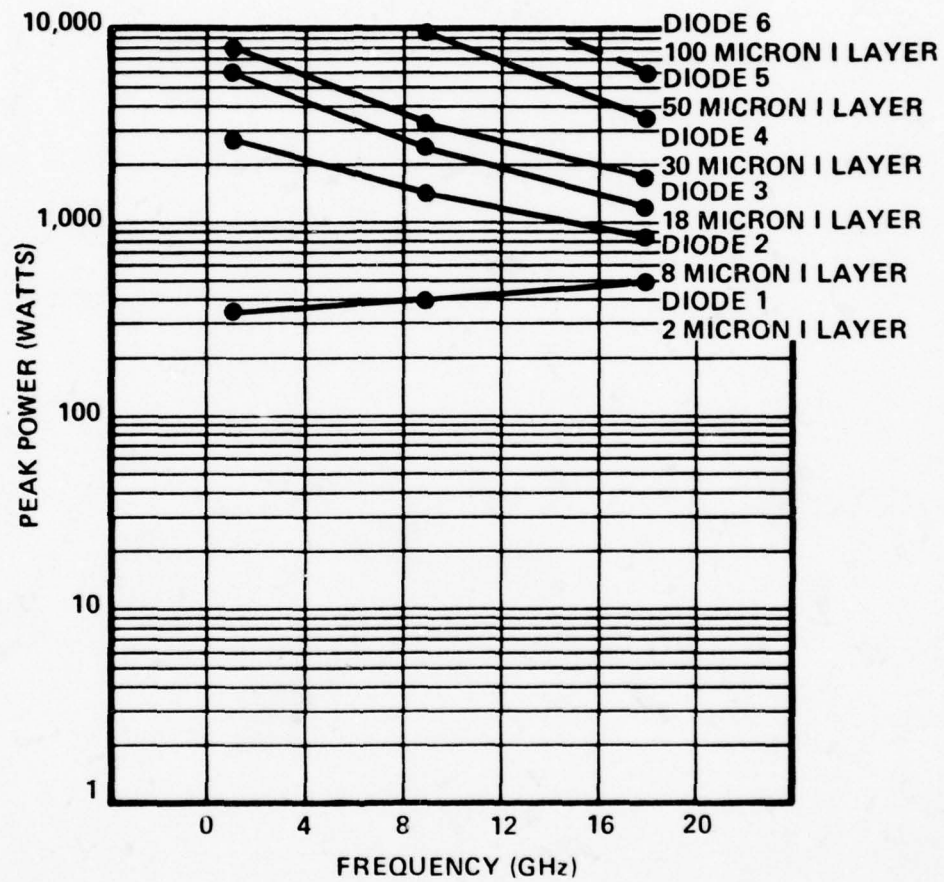
FIGURE 6. PEAK BURNOUT AT +10mA BIAS

D-16947
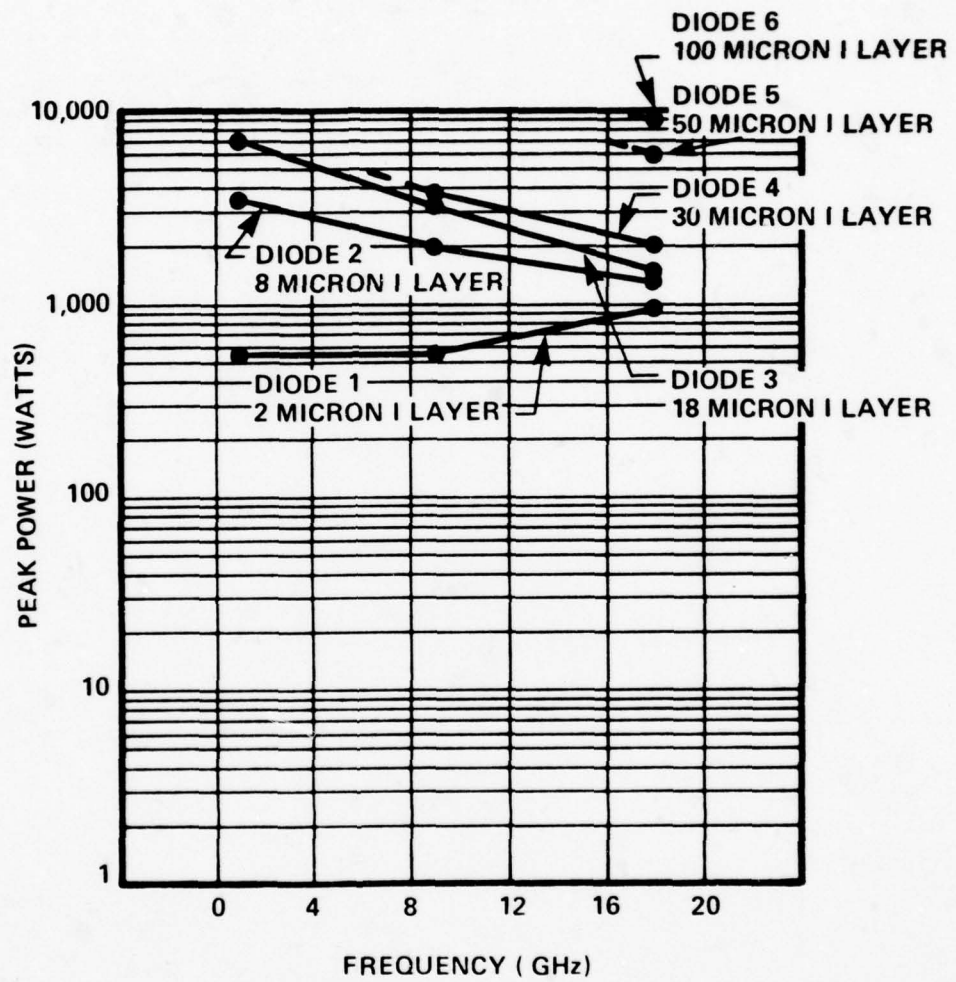
FIGURE 7. PEAK BURNOUT AT +50mA BIAS

D-16948
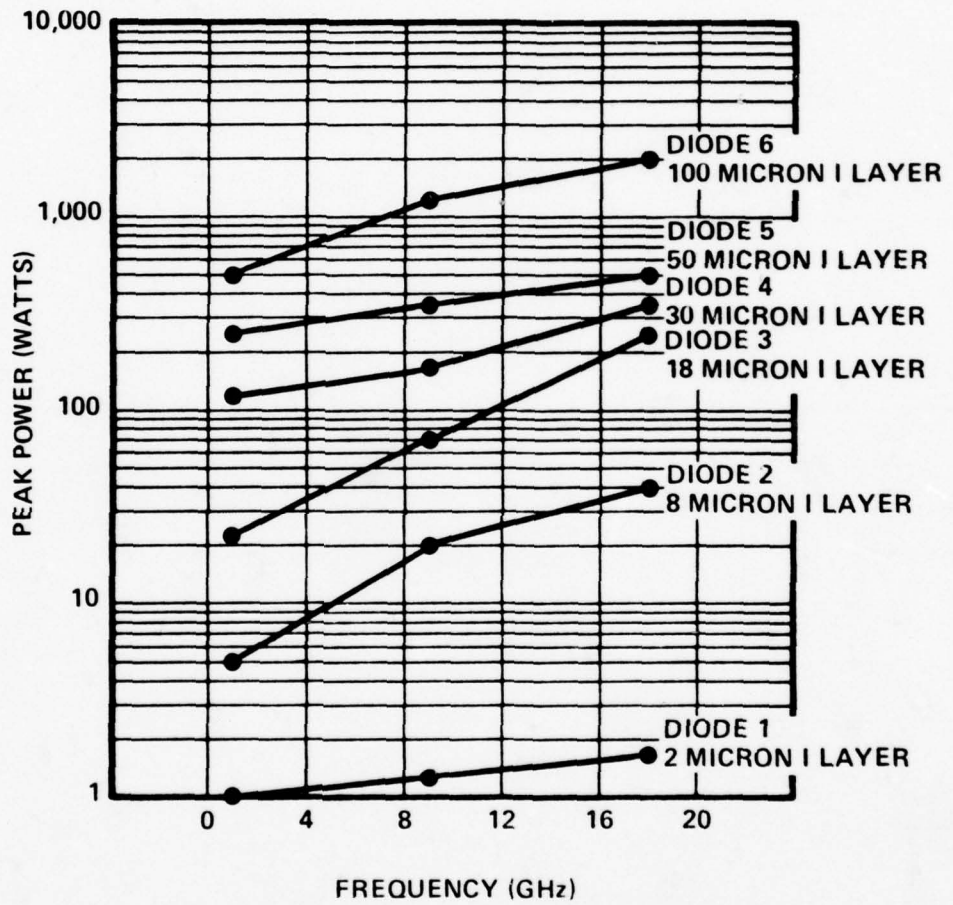
FIGURE 8. PEAK COMPRESSION AT −5V BIAS

D-16949
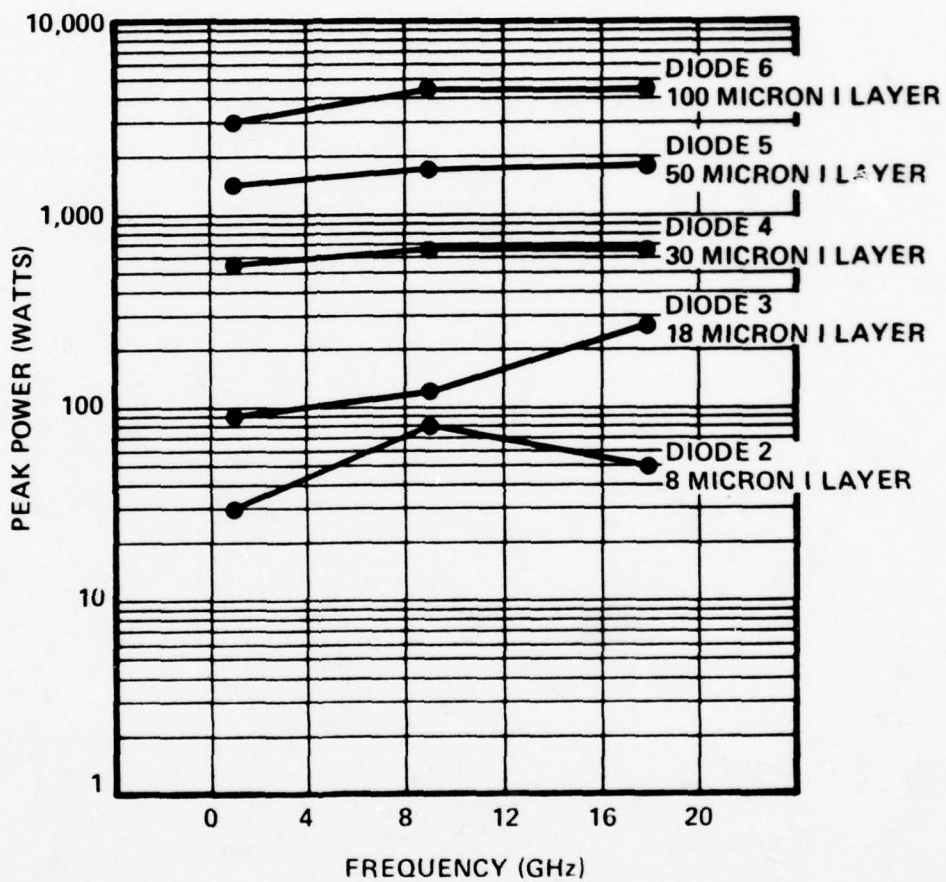
FIGURE 9. PEAK COMPRESSION AT −30V BIAS

D-16950

each burn-out meant a completely new switch circuit was assembled to allow resumption of the tests. Therefore, subtle differences in mechanical tolerances, moderate variances in diode junction characteristics and test equipment accuracy all contributed to the introduction of some undertermined deviation from completely reproducible performances. However, any major discrepancy resulted in retests to ascertain proper data points. The curves of Figures 4 thru 9 present this data.

Figure 4 clearly shows the increased power handling capacity of the thicker diodes. The trade off for selecting higher power levels is the necessarily slower speed associated with the larger junction. Increased frequency creates higher power densities within the junction resulting in burn-out at lower levels. In all respects, this data conformed to expected trends, but yielded actual values under a controlled investigation versus intermittent measurements on various programs. It should be noted that the data at 10KW peak was arrived at by extrapolation of the curve to approximate the typical slope of the curve family (dashed curves).

When reverse bias is increased, the power burn-out may increase, or stay the same for a particular diode. Because the increased DC voltage will be given a larger portion of the total maximum tolerated voltage (DC voltage plus RF voltage) before burn-out, it is normal to assume the threshold will be crossed at a lower peak power. However, the increased voltage also reduces the base-spreading resistance (determines reverse bias Q of the diode), and the resultant is lower power consumed and higher burn-out capabilities at lower frequencies. Sometimes one of these effects will outweigh the other; sometimes they balance for no change. Figure 5 provides -30V bias data to indicate the

subtleties of this reaction. Comparison to Figure 4 shows little effect in general at high frequencies and enhanced power handling at lower frequencies.

As noted previously in this document, increased forward bias current results in lower Rs and a corresponding reduction in junction heating due to the incident RF power. Therefore, the power capability improves. Figures 6 and 7 present the trade-off for 10 mA and 50 mA. In all cases, the 50mA resulted in enhanced power handling for a particular diode, to coincide with the measured Rs values of Table 1. However, as noted in the section on switching speed, a 50 mA bias produces five times the stored charge of 10 mA, and the speed degrades in the process.

Compression point is the power level at which the DC bias is overcome by RF voltages, and the insertion loss increases from conductivity modulation. Normal measurement standards employ the 1.0dB point as the reference level, but a more conservative value of 0.5dB was utilized for the evaluations in this investigation. Obviously, a bias level of 30 volts cannot be overcome as quickly as 5 volts as RF power is increased. Comparision of Figures 8 and 9 show the improved compression point response very clearly as bias is increased to 30 volts. However, the inevitable presence of a trade-off is not avoided. To produce the larger reverse voltages, higher breakdown transistors must be utilized in the driver circuits. The resultant is a reduction in speed as the higher voltage transistors have longer delay times.

Compression point data improves with increasing frequency. This can best be understood by considering a complete period of the RF waveform at low and high frequencies. The opposing RF voltage is impressed across the diode nine times longer at 1 GHz than at 9 GHz and eighteen

-20-

times longer than at 18 GHz. Thus, even though the peak voltages are identical, the RF waveform allows a greater opportunity for diode conduction at lower frequencies during any given period. This can be related to the response time for the diode junction itself; both Figures 8 and 9 indicate this as the longer lifetime diodes have improved compression point performance at any test frequency.

Because of the thermal time constant associated with PIN diode junctions, the burn-out level must be carefully defined for peak levels. For instance, the peak power levels to which diodes were subjected during this investigation were always at one microsecond pulse width and 0.1% duty cycle. This assured destruction from avalanche voltage effects versus excess heating effects caused by absorbed power. For CW investigations, the heating effect is the general mode of destruction. Figures 10, 11, 12 and 13 present data for burn-out under application of CW signals.

CW power equipment was restricted to 100 watts. Therefore, the curves of Figures 10 through 13 are not entirely complete, but sufficient data is available to allow significant design aid.

Increased negative bias always improves burn-out for CW applications. The reduced base spreading resistance simply results in lower heating and, thus, better survival characteristics. This effect can be noted by comparison of Figures 10 and 11. Similarly, the increased bias of +50mA versus +10mA results in better power handling capabilities. This is due to lower Rs and, consequently, lower I^2R losses (heating). Figures 12 and 13 depict this effect. To restate the trade-offs associated with increased bias, the speed will be affected either because of slower transistors (to accommodate increased reverse bias) or larger stored charge in the PIN diode junction (due to increased forward bias).
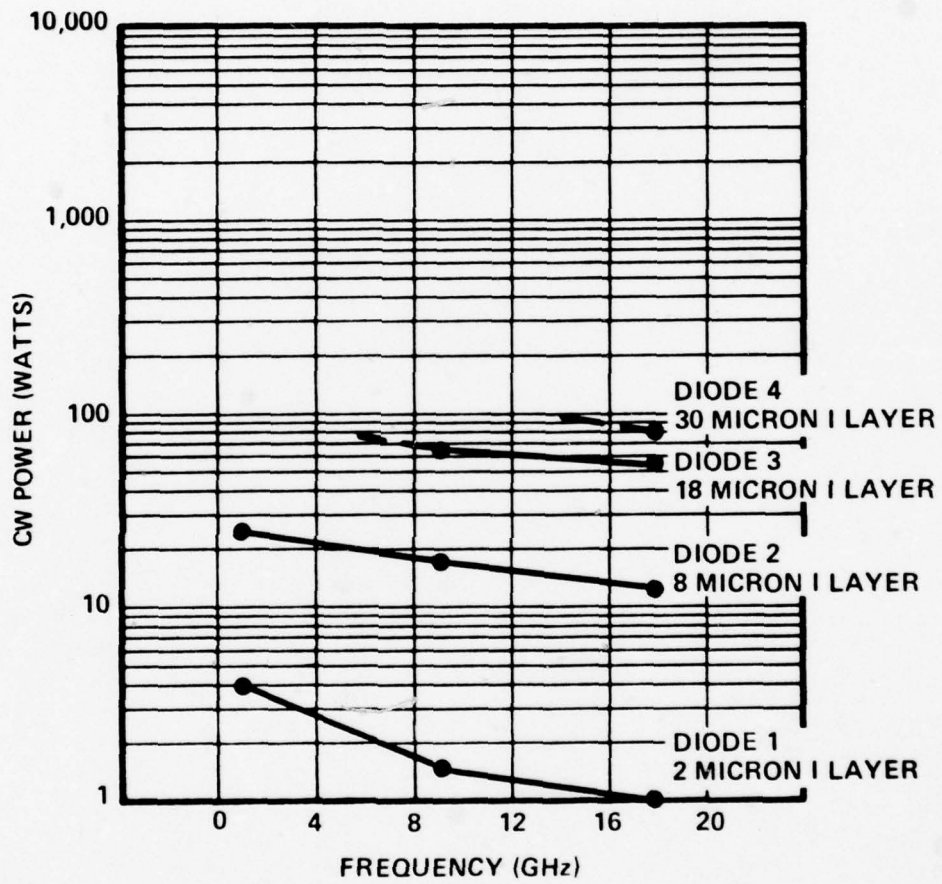
FIGURE 10. CW BURNOUT AT −5V BIAS

10,000

1,000

CW POWER (WATTS)

DIODE 4
30 MICRON I LAYER

100

DIODE 3
18 MICRON I LAYER

DIODE 2
8 MICRON I LAYER

10

DIODE 1
2 MICRON I LAYER

1

0   4   8   12   16   20

FREQUENCY (GHz)
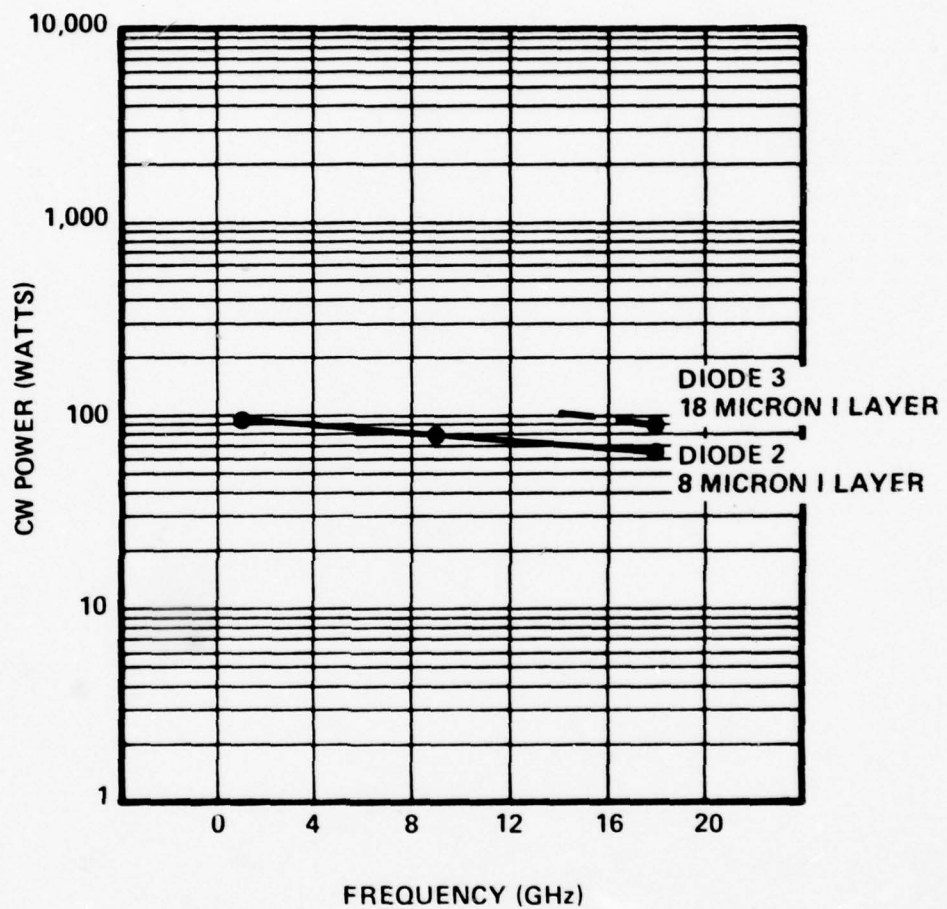
D-16951

FIGURE 11. CW BURNOUT AT −30V BIAS

D-16952
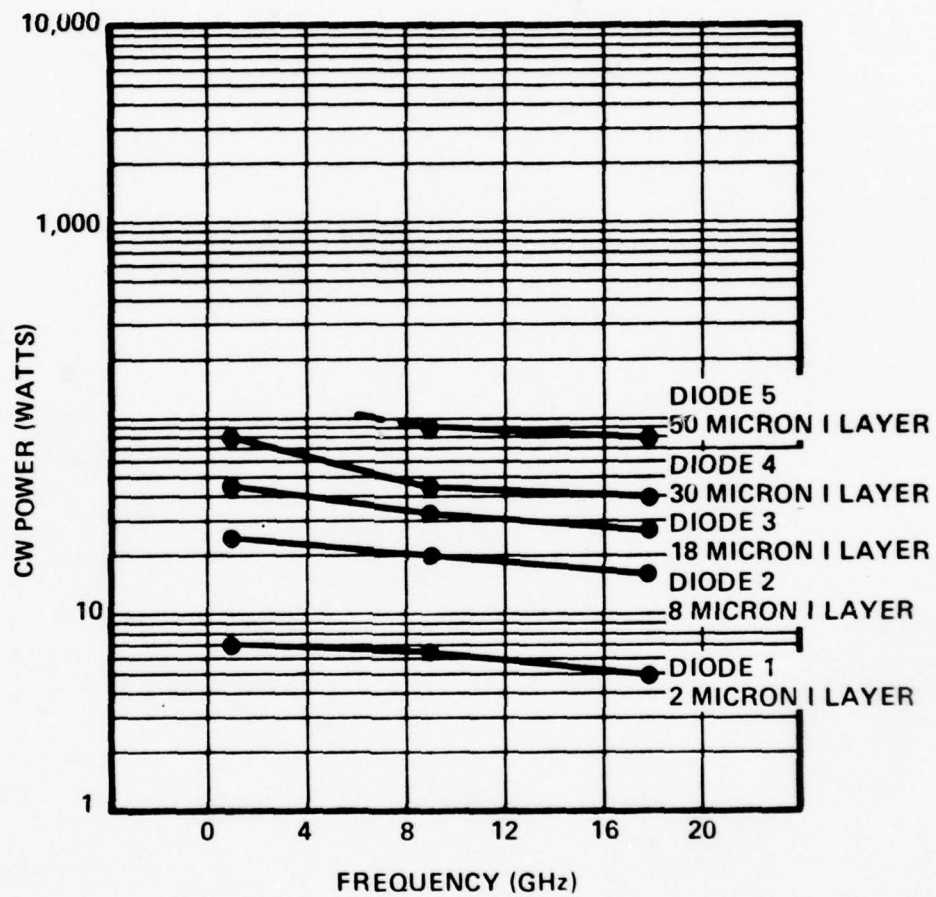
FIGURE 12. CW BURNOUT AT +10mA BIAS

D-16953
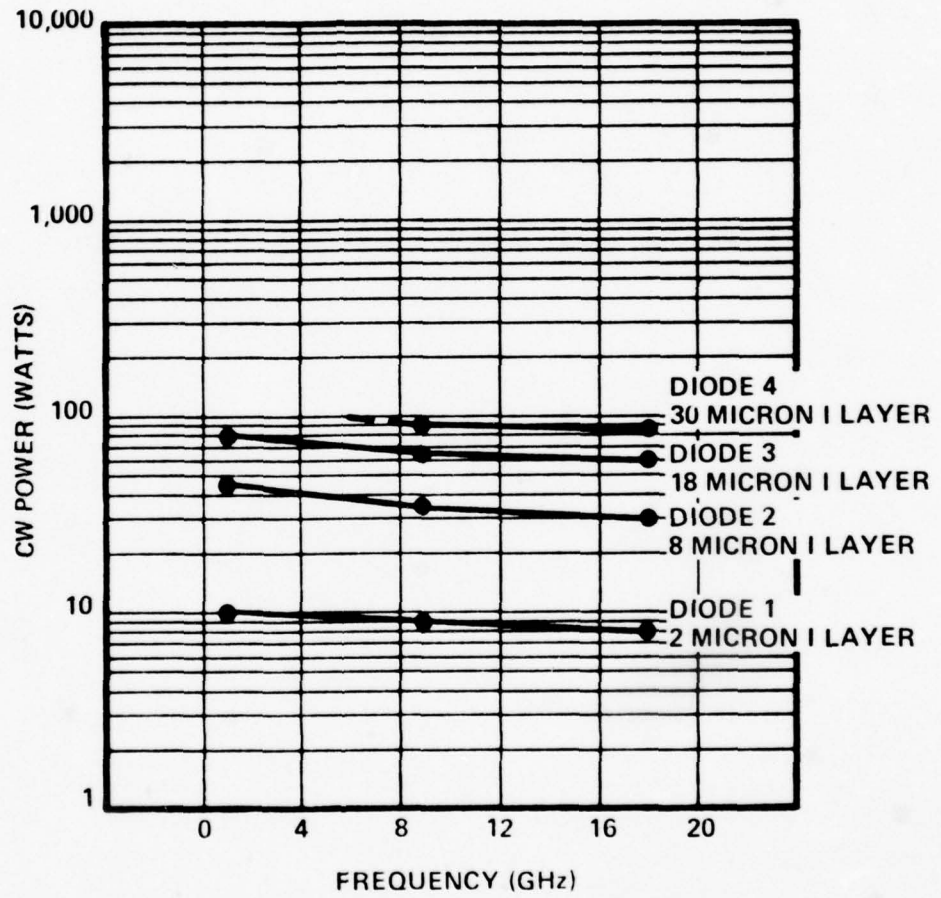
FIGURE 13. CW BURNOUT AT +50mA BIAS

D-16954

INVESTIGATION - SPECIAL DIODES

Off center mesa and multi-dot diodes

During this program, the concept of off center mesas and multi-dot diodes was investigated. The rationale for an off-center mesa is to minimize bond wire lengths when using the diode in the series configuration on a multi-throw switch. The shorter bond wires minimizes undesirable series inductance. The multi-dot diode also minimizes bond wire inductance and in addition, it permits construction of a multi-throw junction using only a single chip. The single chip is smaller and hopefully each diode on the chip is matched very closely to the others. In this study, four diodes were etched on a chip about twenty (20) mils square. This is sometimes called a "Quad Chip". The Quad Chip can also be constructed so that each diode is different, i.e., the capacitance can increase from diode to diode on the same chip (with an attendant decrease in series resistance). This device is useful for making a multi-throw switch where each arm is optimized for its own unique bandwidth requirement.

Table 3 presents data for the initial feasibility run for multi-dot diodes. It provided enough optimism for generation of new etching masks to attempt closer control. The variation in breakdown voltage (Table 3) would guarantee a wide variation in switching speed. This prompted the aforementioned second run. All other aspects of this first run were very encouraging; chips 1, 3, 6, 7, 8 and 10 could have been utilized and would probably produce acceptable results for switching speed. However, chips 6 and 10 would have to be eliminated for low bias capacitance (0.05 pf). Lifetimes were 80-140 nanoseconds.

Table 4 depicts the status data for the second run of "identical capacitance" multi-dot diodes. Breakdown voltage showed a slightly wider range than would be desired, but all other parameters are exceptionally good. Chips 1, 7, 8, 9, and 10 are almost perfect. The yield of 40 for 40 mesas is well above normal expectations.

Table 5 presents the data taken for the "varying" capacitance multi-dot diode. Increasing dot diameter corresponds to higher capacitance as

TABLE 3

PRELIMINARY MULTI-DOT DATA

CHIP #	V_B	CAP @ 0.7 V	CAP @ 10.0 V
# 1	120	.04	.03
	120	.03	.02
	100	.03	.02
	80	.04	.03
# 2	140	.04	.03
	80	.03	.02
	80	.04	.03
	80	.03	.02
# 3	140	.03	.03
	140	.03	.02
	140	.03	.03
	160	.04	.03
# 4	120	.04	.03
	60	.03	.02
	Short	.04	.03
	120	.05	.05
# 5	Short	.04	.03
	120	.03	.02
	80	.05	.04
	95	.04	.03
# 6	80	.04	.03
	110	.04	.03
	80	.03	.02
	100	.05	.03
# 7	125	.03	.02
	130	.03	.02
	110	.04	.03
	100	.03	.03
# 8	95	.04	.03
	95	.04	.03
	105	.03	.02
	115	.03	.03
# 9	135	.03	.02
	80	.03	.02
	Short	.03	.03
	110	.04	.03

TABLE 3 (CONT)

PRELIMINARY MULTI-DOT DATA

CHIP #	V_B	CAP @ 0.7 V	CAP @ 10.0 V
#10	100	.05	.03
	110	.03	.02
	130	.03	.02
	105	.03	.03

TABLE 4

MULTI-DOT "IDENTICAL CAPACITANCE" DATA

CHIP #	DOT SIZE	V_B	C 0.7V	C 10.0V	LIFETIME
# 1	.0010	45	0.83	0.02	90
	.0012	45	0.03	0.02	95
	.0010	40	0.03	0.02	110
	.0011	45	0.03	0.02	95
# 2	.0013	82	0.04	0.03	110
	.0015	100	0.04	0.04	90
	.0018	68	0.03	0.03	110
	.0014	65	0.04	0.03	95
# 3	.0011	60	0.04	0.04	120
	.0013	80	0.04	0.04	125
	.0013	80	0.04	0.03	110
	.0015	80	0.05	0.04	95
# 4	.0013	62	0.05	0.04	110
	.0012	60	0.05	0.04	110
	.0011	60	0.05	0.04	105
	.0012	40	0.05	0.04	110
# 5	.0013	42	0.05	0.04	115
	.0011	22	0.05	0.04	90
	.0014	40	0.05	0.04	85
	.0012	20	0.05	0.04	95
# 6	.0013	58	0.05	0.04	95
	.0013	40	0.05	0.04	110
	.0014	100	0.05	0.04	120
	.0012	60	0.05	0.04	120
# 7	.0011	40	0.03	0.02	95
	.0013	40	0.03	0.02	90
	.0012	40	0.03	0.02	80
	.0012	40	0.03	0.02	80
# 8	.0010	40	0.03	0.02	95
	.0014	40	0.03	0.02	105
	.0014	40	0.03	0.02	105
	.0015	40	0.03	0.02	90
# 9	.0014	20	0.04	0.02	85
	.0011	50	0.04	0.03	110
	.0011	100	0.04	0.02	90
	.0012	40	0.03	0.02	90

TABLE 4 (CONT)

MULTI-DOT "IDENTICAL CAPACITANCE" DATA

CHIP #	DOT SIZE	V_B	C 0.7V	C 10.0V	LIFETIME
#10	.0015	80	0.03	0.02	90
	.0014	100	0.03	0.02	90
	.0015	100	0.03	0.02	105
	.0010	80	0.03	0.02	95

TABLE 4 (CONT)

TABLE 5

MULTI-DOT - VARYING CAPACITANCE DATA

CHIP #	DOT SIZE	V_B	C 0.7V	C 10.0V	LIFETIME
# 1	.0015 TYP	40	.11	.02	80
	.0020 TYP	-	.11	.04	95
	.0025 TYP	-	.13	.06	95
	.0028 TYP	50	.14	.09	105
# 2	-	42	.04	.02	105
	-	80	.05	.03	115
	-	80	.05	.04	125
	-	80	.07	.05	120
# 3	-	10	.04	.03	90
	-	100	.05	.03	90
	-	20	.06	.04	100
	-	100	.06	.04	100
# 4	-	40	.04	.03	-
	-	40	.05	.04	105
	-	80	.06	.04	100
	-	90	.07	.06	100
# 5	-	60	.05	.02	80
	-	20	.02	.02	90
	-	78	.06	.02	90
	-	90	.04	.03	105

noted. Although this device was not utilized in this program, the data is added for reference. This type of diode would be useful in multi-throw switches where each arm is optimized over a different frequency band.

The uniform capacitance multi-dot diode was utilized in Phase II of the program. Our initial estimate of its value was a lower anticipated phase variation due to the shorter bond wires. However, as discussed in more detail later, the processing difficulties encountered with this diode compromised the results somewhat.

The Plated Heat Sink Diode

Another Diode Type was also investigated on this program. This was the so called "Plated Heat Sink Diode". This diode is unique in that it is built on a copper plated heat sink, and it offers significantly lower thermal and electrical resistance. Additionally, the etching process is more complete and results in lower capacitance. Preliminary RF test data shows that the RC product for this type of diode is approximately 20-25% better than conventionally fabricated PIN diodes.

When mounted in a typical SPST switch circuit, this diode resulted in .2 - .3dB lower insertion loss and 3-6dB higher isolation at 18 GHz than a comparable PIN diode (i.e. an 8 micron I-layer diode). Initial high power tests show that this diode is capable of handling at least 15% more power (in the worst case operating condition of CW power and forward bias) than a comparable PIN of conventional design (i.e. 8 micron). Tests were run at 25 watts CW at 16 GHz and an applied bias of 10mA without burnout. This diode is comparable to an eight (8) micron diode (type 2 on the basis of switching speed. As shown in Fig. 12, this diode has a burnout level of 20 watts. Thus for a diode with comparable RF and switchi performance, the plated heat sink diode offers at least a 15-20% increase

in power handling capability. ' The improved performance is a consequence of the reduced electrical and thermal resistance.

CONCLUSION (PHASE I)

A broad range of pin diodes suitable for microwave switching applications was selected for proper characterization. The selection ranged in six steps from very thin I-layer types with fast switching characteristics (less than 10 nanoseconds). to very thick I-layer types with relatively slower switching characteristics (on the order of a few microseconds).

The RF power handling capability in 50 ohm systems of each diode was determined for each of the applicable operating modes, and at a variety of bias conditions in each mode.

The switching speeds for each diode type were determined with two types of driver circuits.

The tables and graphs present this data and show the trade offs between RF power handling and switching speeds, for a broad range of PIN diodes suitable for wide band microwave switching circuits.

PHASE II

SWITCH PROGRAM

INTRODUCTION

In order to corroborate the findings of the diode study phase of the program, the second phase of the program addressed application of the data to meet specific design criteria. Five different switches were built and tested. The specifications and some additional design goals are outlined in Figure 14. The principle trade-off for each design centers around the power handling/switching speed problem. After discussing the general circuit design approach and certain uniformly applied concepts, each switch will be discussed in detail.

FUNDAMENTAL DESIGN CONCEPTS

Diode Control Devices have been in use for a number of years. Early designs used packaged diodes and matching circuits. This type of circuit suffered degraded performance at microwave frequencies. In order to circumvent the parasitic problems inherent in this approach, special diode packages were designed and integrated into coaxial or stripline packages. This approach worked well up to approximately 8 or 12 GHz. The current state-of-the-art eliminates most of the parasitics associated with the diode package and packaging constraints by using the diodes in chip form and utilizing "microstrip" as the transmission line to connect the various circuit elements. As a result, diode switching devices and packages can be made to 18 GHz and higher.

-34-

Switch Specification ( )'s Denote Design Goals

Type	-1 Transfer	-2 SPDT	-3 SP4T Note F:	-4 SPDT Note G:	-5 SPDT
Frequency Range (GHz)	12-18 (7-18)	12-18 (7-18)	F_L-F_H	F_L-F_H	12-18 (7-18) Note C
Peak Power (W)	5	5	5	2	500 (1000)
Average Power (W)	5	5	5	2	25 (50)
Load VSWR	NA	NA	2:1 max. Note D:	2:1 max. Note D:	2:1 max. Note D:
Loss (dB)	3.8 max. (3.5 max.)	2.7 max. (2.5 max.) Note A:	3.5 max.	2.9 max.	2.4 max. (2.0 max.)
Isolation (dB)	50 min.	40-50 min.	35 min.	60 min.	35 min. (40 min.)
Input VSWR Switch "ON"	1.8:1 (1.6:1)	1.7:1 (1.6:1)	1.9:1 (1.8:1)	2.0:1	1.7:1 (1.6:1)
Input VSWR Switch "OFF"	NA	1.7:1 (1.6:1)	NA	NA	NA Note E:

FIGURE 14 - SWITCH
SPECIFICATIONS

Switch Specification · ( )'s Denote Design Goals

Type	-1 Transfer	-2 SPDT	-3 SP4T	-4 SPDT	-5 SPDT
Amplitude Tracking (dB)	± 0.2 Note B: (± 0.1)	± 0.2 (± 0.1)	± 0.2 -0.4 (± 0.1)	± 0.4 (± 0.1)	± 0.2 (± 0.1)
Phase Tracking (°)	(± 1)	(± 1)	NA	NA	(± 1)
RF Transition Speed (ns)	(2) -3	3 (2)	3-4 (2-3)	8 (5)	60 (40)
Total Speed RF + Driver (ns)*	10-12	15 (10)	(12)	20 (15)	90 (50)'
Driver Control	T^2L, 1 bit	T^2L, 2 bit	T^2L, 2 bit	T^2L, 2 bit	T^2L, 2 bit
Video Leakage(V)	NA	NA	(0.05 max. to 1 GHz)	(2 max.)	NA
Operating Ambient Temp. Range (°C)	0-70	0-70	0-70 Will employ multi-dot series diode chip.	-54 to +110 Driver Voltage: ± 12V	0-70

Logic 0 = "ON"
Logic 1 = "OFF"

*Not applicable for fixed clock speed.

FIGURE 14 (CONT)

-36-

Table 1 Switch Specification ( )'s Denote Design Goals

Comments:

Note A: **-2 SPDT Isolation**
Isolation to be determined for 1, 2, and 3 shunt diodes each. Isolated ports to look matched.

Note B: **-1 Transfer Amplitude Tracking (dB)**

A1 - A2 and B1 - B2 only.
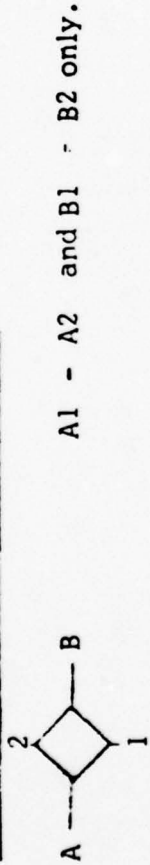
Note C: **-5 SPDT, Peak Power (W)**
RF pulsewidth = 1 μs peak power "Hot Switching" required.

Note D: **-3 SP4T, -4 SPDT, -5 SPDT Load VSWR**
Measurements of switching under power into 2:1 VSWR Load only (switch survival) at band edges. Other parameters measured into matched loads.

Note E: **-5 SPDT Input VSWR Switch "OFF"**
A design goal of matched outputs with low reflective power(less than 100 mW).

Note F: **-3 SP4T Frequency Range (GHz)**
$F_H = F_H$ of contract listed in Note G. $F_L = F_L$ of contract listed in Note G -800 MHz.

Note G: **-4 SPDT Frequency Range (GHz)**
Frequency range of N00173-76-C-0313

FIGURE 14 (CONT)

DIODE CIRCUITS

Diode Control Devices can utilize either series or shunt mounted diodes. Each approach has it's domain. In general, series designs are preferred at low frequencies and in broadband multi-throw applications, shunt designs are preferred at high frequencies, and for narrow band multi-throw switches. The diodes can also be configured in series and shunt to produce very broadband designs; however, they are slower and can handle less power, due to the inherent limitations imposed by the series-shunt configuration.

In general, the shunt mounted diode is preferred for high power switching because of the low thermal resistance attained by attaching the diode chip directly to a large heat sink. Series designs for high power applications are possible also, but the thermal resistance of the diode when mounted to a coax center conductor is much higher than the same diode mounted in shunt.

The series-shunt configuration is commonly used for low power applications. For high power devices, this circuit has two limitations. The first is the thermal problem discussed above. The second is that the bias voltage applied to either diode is limited to .7 - .8 volts. This limitation reduces the power handling by reducing the reverse bias on the diodes. The reduced bias voltage also increases the switching speed for a given diode since it results in a slower removal of carriers.

Approaches have been proposed to resolve the difficulties associated with series and series-shunt designs. For instance,

-38-

the series diode could be mounted on a beryllia chip (improving the thermal resistance), however, the capacitance of the beryllia chip degrades RF performance. The bias limitations could be resolved by adding an additional bias coil and blocking capacitor between the series and shunt diode and providing a separate independent driver for each diode. This approach, in addition to the cost of an additional driver, also compromises RF performance due to the additional bias circuit which must be designed into the circuit at the junction.

The detailed tradeoffs involved in choosing a particular diode configuration are inextricably involved with the particular set of specifications for a given device, and the final choice of circuitry must be based on the specific requirements.

SHUNT DIODE CIRCUITS

Figure 15 shows the equivalent circuits and practical realization of a shunt diode switch. To mount the diode, a gap is cut into the microstrip, the diode inserted and connected with a bond wire. The gap width and bond wire inductance are adjusted so that the LC combination is that required for a low ripple (.01 to .1 dB) Tschebyshev Filter (low pass) with a cutoff above the maximum operating frequency. For practical microwave devices, diode junction capacitances of .10 pF to .30 pF are required. Since the $R_S C_J$ product of microwave PIN diodes is approximately constant, and R_S of .5 ohms to 2 ohms can be achieved in the forward bias state. With this type of diode, a switching ratio of about 20 dB per diode can be achieved.

PICTORIAL
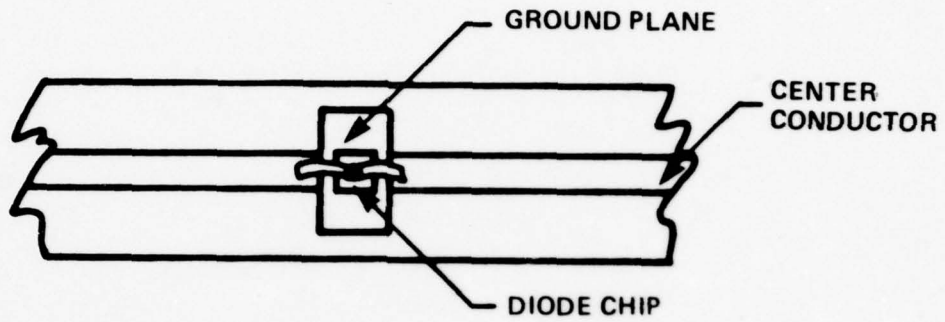
EQUIVALENT CIRCUITS

REVERSE BIAS (LOW LOSS)   FORWARD BIAS (HIGH LOSS)
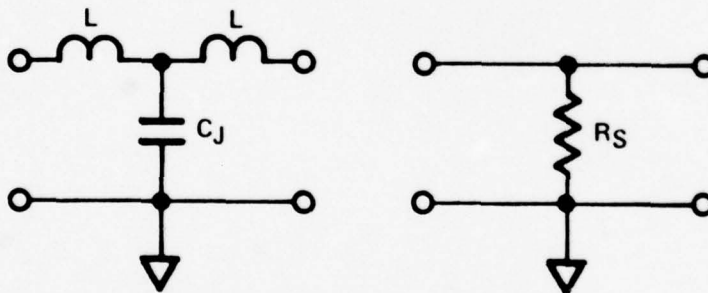
C_J — DIODE JUNCTION CAPACITANCE
R_S — DIODE SERIES RESISTANCE
L — BOND WIRE INDUCTANCE

FIGURE 15. SHUNT DIODE CIRCUITS

D-16955

-40-

The model is valid for "small signal" conditions. For
PIN diodes, this means that the incident RF power is not high
enough to cause conductivity modulation to exist. This con-
dition can be met by limiting the power level or if higher
power levels are required, by increasing the reverse bias on
the diode. The diode breakdown voltage (V_B) is the upper
limit in this process. That means that the sum of the peak
RF voltage and the bias voltage cannot exceed V_B.

Shunt diode matching characteristics were investigated
for a number of idealized models. These computer generated
curves show the VSWR behavior for shunt mounted PIN diode
models in a 50 ohm circuit. Figure 16 shows the VSWR of a
2 diode circuit using 0.1 pF uncompensated diodes which are
quarter-wavelength spaced at 16 GHz. Figure 17 is a three
diode model with quarter-wavelength spaced diodes for three
conditions; 1) 0.1 pF diodes, 2) 0.2 pF diodes, and 3) two
0.1 pF diodes and one 0.2 pF diode. The effects of inductive
compensation are shown in Figure 18 for case of single shunt
diodes of 0.10, 0.14, and 0.16 pF capacitance. Figure 19
clearly shows the ultimate limitation of junction capacitance
as a single 0.2 pF diode is modeled for a number of compensating
inductances. Figure 20 compares the matching characteristics
of a single 0.2 pF compensated diode to a two 0.2 pF diode
model using both optimal inductive compensation and quarter-
wavelength spacing.
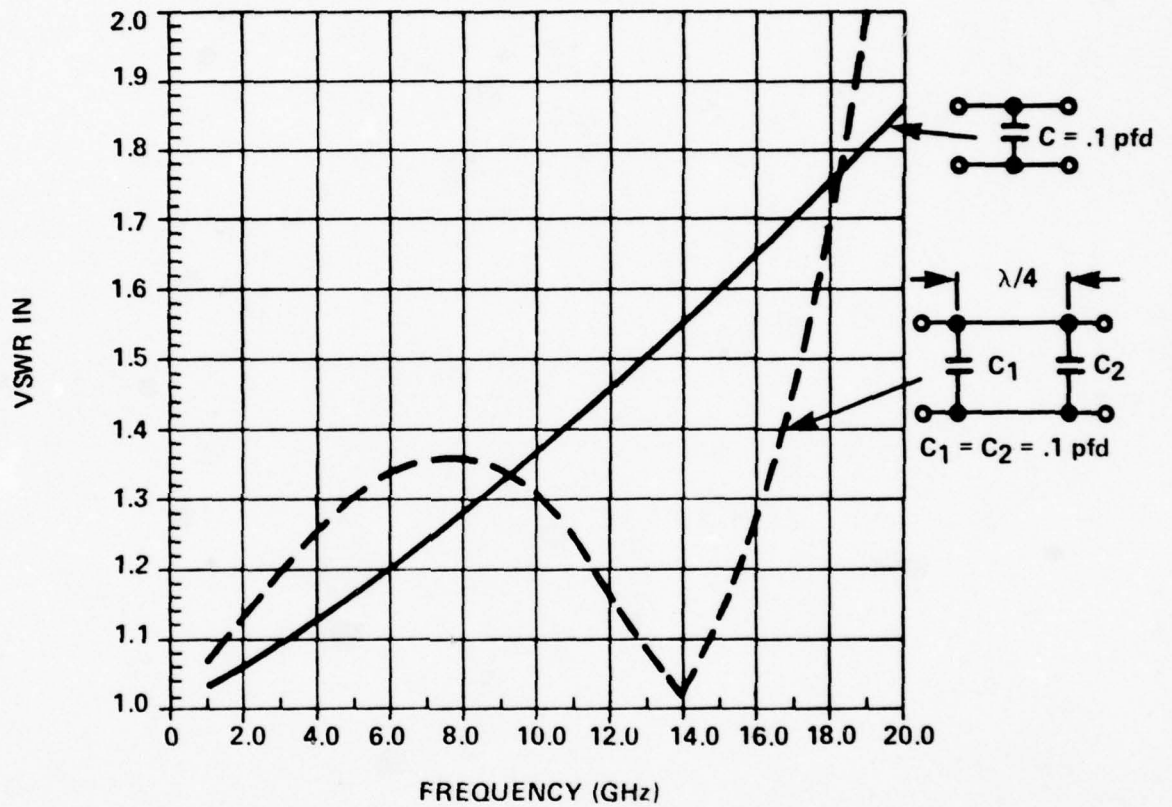
FIGURE 16. ONE DIODE C = .1 pfd AND TWO SPACED λ/4 @ 10 GHz

D-16979

-42-
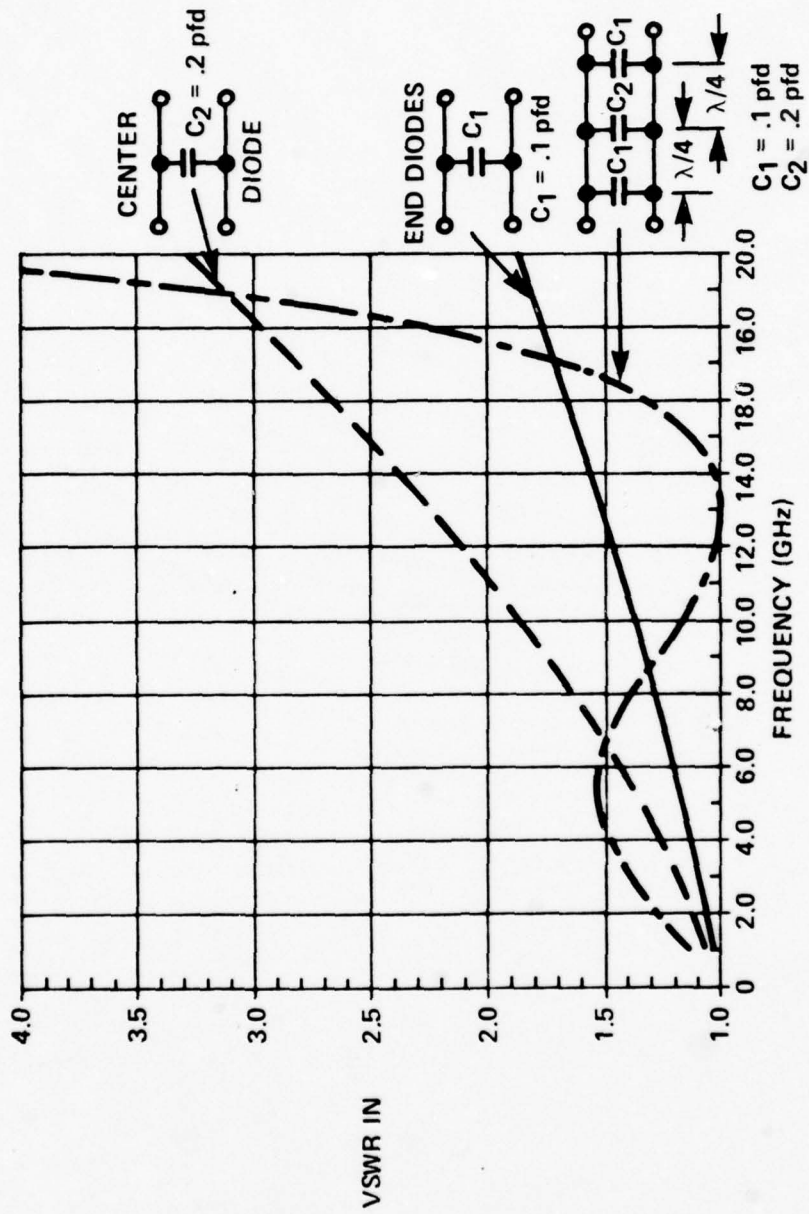
FIGURE 17. THREE DIODE MODEL λ/4 SPACED AT 16 GHz

D-16978
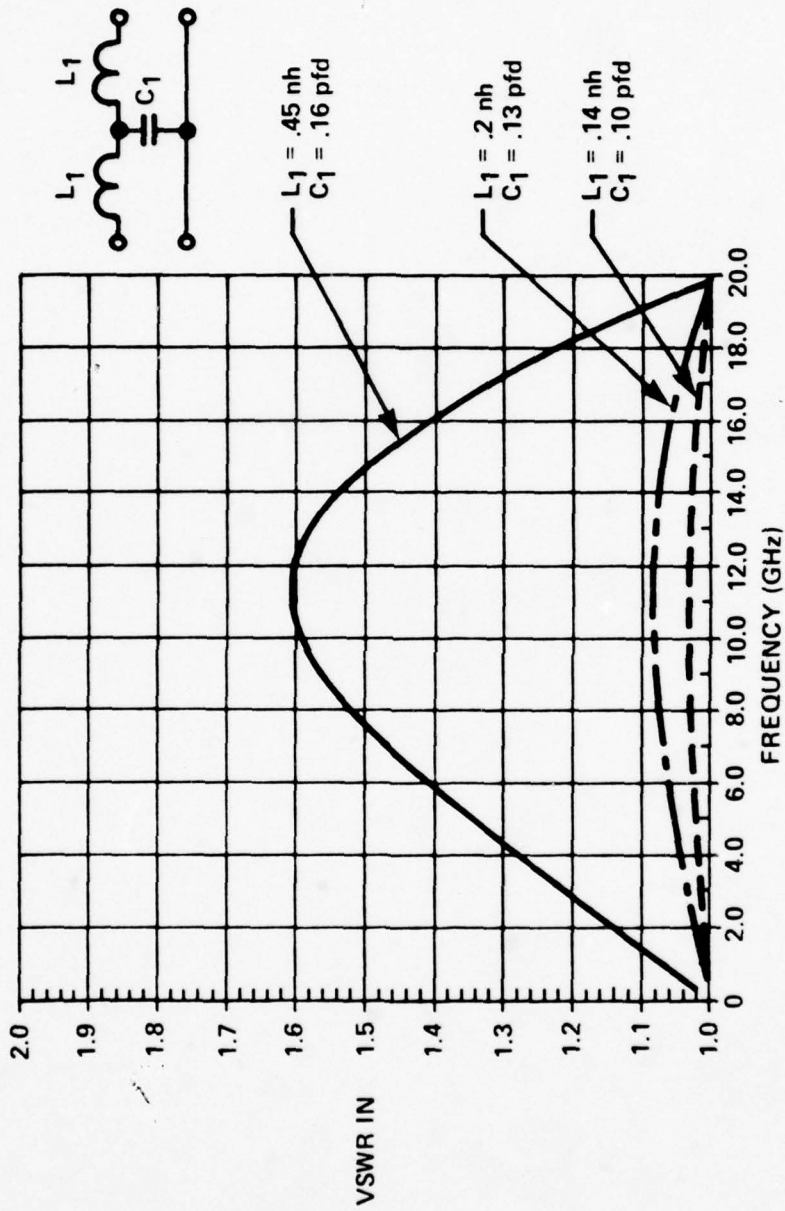
FIGURE 18. SHUNT DIODE COMPENSATION @ 19.5 GHz

$L_1 = .45$ nh
$C_1 = .16$ pfd

$L_1 = .2$ nh
$C_1 = .13$ pfd

$L_1 = .14$ nh
$C_1 = .10$ pfd

VSWR IN

FREQUENCY (GHz)
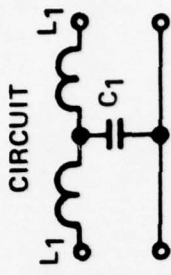
D-16976

CIRCUIT

$L_1 = .56$ nh
$C_1 = .3$ pfd ①

$L_1 = .385$ nh
$C_1 = .25$ pfd ②

$L_1 = .28$ nh
$C_1 = .2$ pfd ③
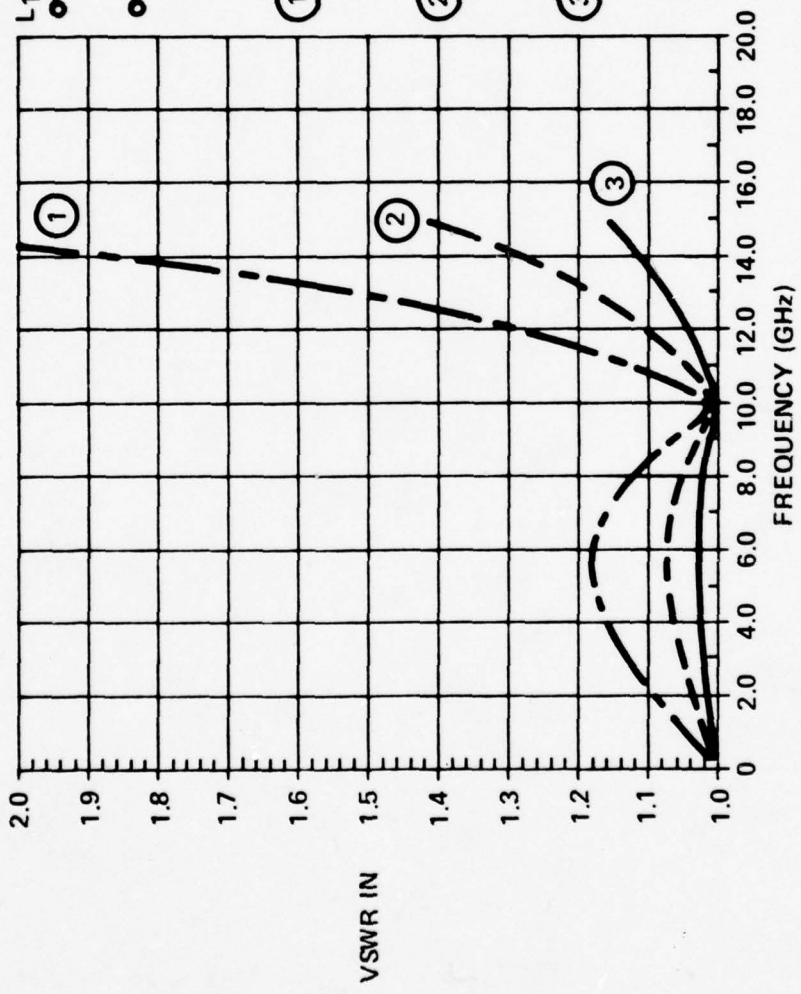
FIGURE 19. SHUNT DIODE COMPENSATION

VSWR IN

FREQUENCY (GHz)

D-16977

-45-
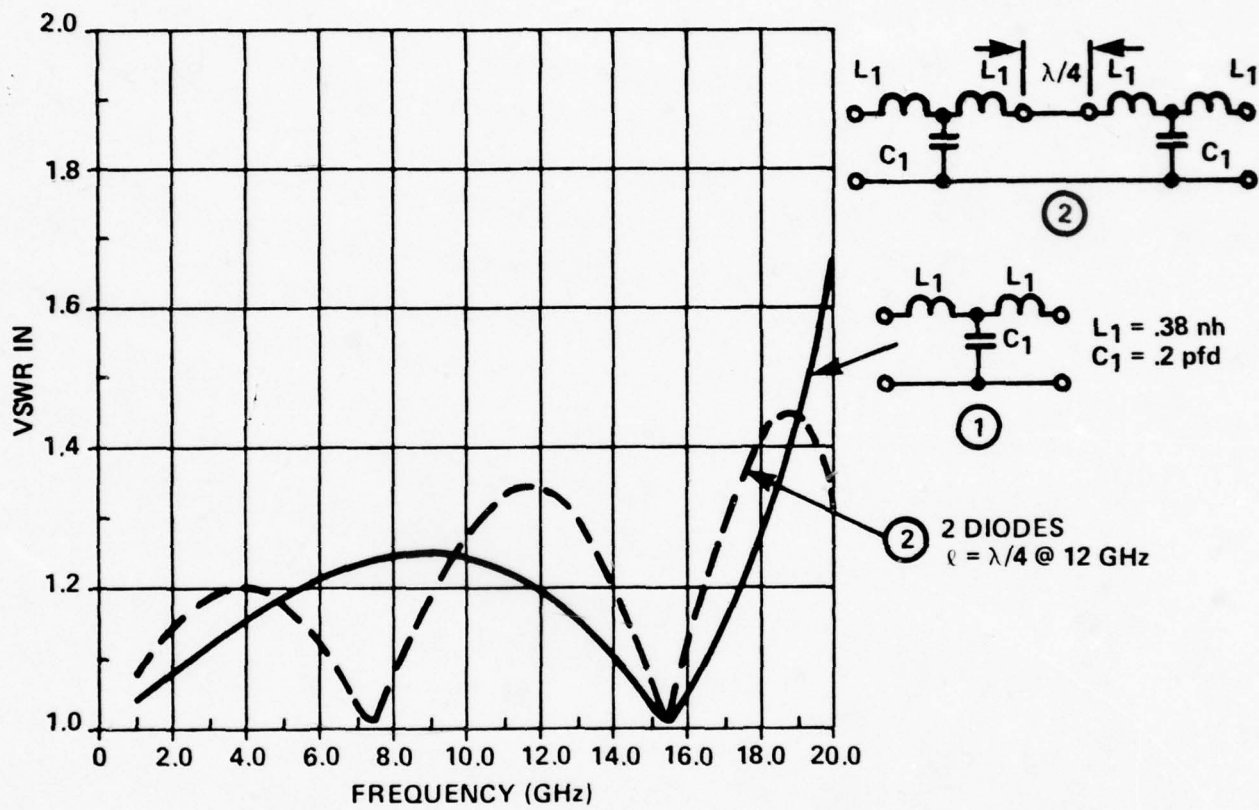
FIGURE 20. TWO COMPENSATED DIODES

D-16981

SERIES DIODE CIRCUITS

Figure 21 shows the equivalent circuits and practical realization of a series diode switch. In the reverse bias state, the junction capacitance blocks the signal. Isolation is frequency dependent decreasing at approximately 6dB per octave. In the forward bias condition, the signal is attenuated slightly by the series resistance of the diode.

Figure 22 shows a multi-throw junction utilizing series diodes. In this case, one diode is forward biased and the balance reverse biased. Performance of this circuit is similar to the circuit of Figure 21 except for an additional loss caused by leakage through the reverse biased diodes. The loss increases with frequency and number of throws. The design requirements for series diodes dictates lower capacitance at the expense of series resistance. Good series diodes have junction capacitances of .02 pF to .05 pF and series resistance of 2 ohms to 6 ohms. The applicability of these models is again limited to "small signal" conditions.

MISCELLANEOUS CIRCUITRY

A few additional circuits are also required to make diode switching circuits. The most commonly used of these is shown in Figure 23 and Figure 24. Figure 23 shows a DC block circuit. This circuit prevents diode biasing voltages from entering the center conductor outside of the switch. Figure 24 shows a bias circuit commonly used to apply DC bias to the diodes, while not interrupting the RF signal path. Both of these circuits are used extensively in the five switch designs.

PICTORIAL

BOND WIRE

CENTER
CONDUCTOR

DIODE CHIP

EQUIVALENT CIRCUITS

REVERSE BIAS (HIGH LOSS)   FORWARD BIAS (LOW LOSS)
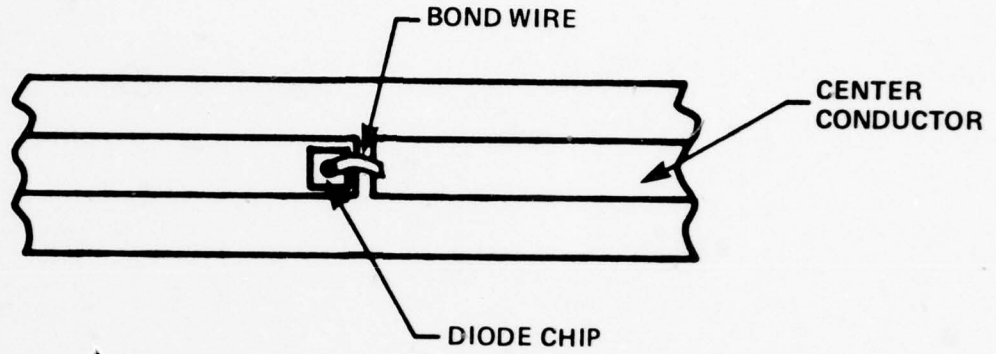
C_J R_S
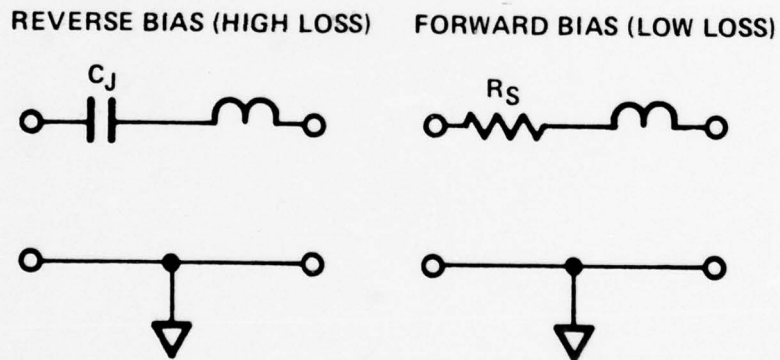
FIGURE 21. SERIES DIODE CIRCUITS

D-16956

-48-

PICTORIAL

EQUIVALENT CIRCUIT

HIGH LOSS
PATH

C_J

R_S

LOW LOSS
PATH
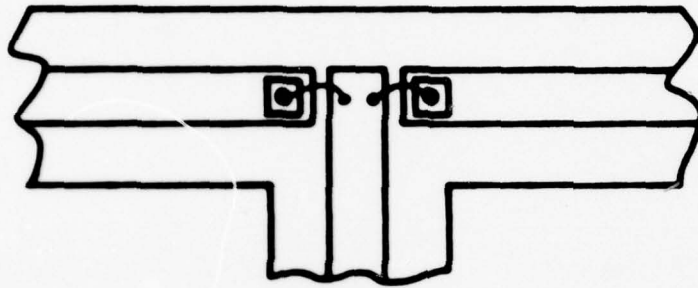
INPUT
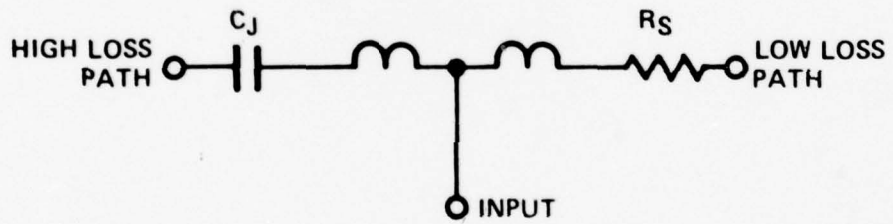
FIGURE 22. SERIES CIRCUIT

D-16957

PICTORIAL

CHIP CAPACITOR

CENTER
CONDUCTOR

MULTIPLE BOND WIRES
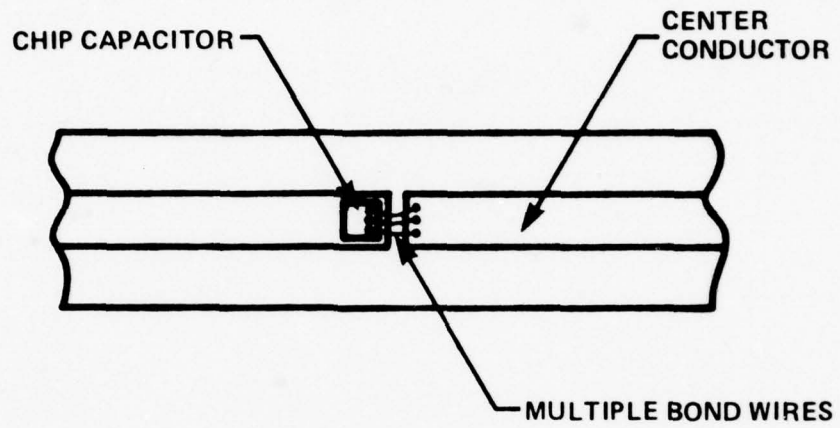
EQUIVALENT CIRCUIT
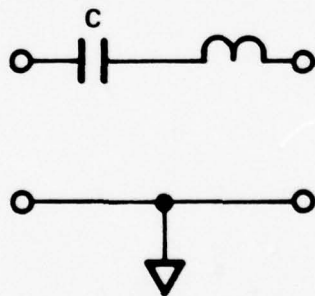
FIGURE 23. DC BLOCK CIRCUIT

D-16958

PICTORIAL

CENTER
CONDUCTOR

SMALL AIR
WOUND COIL

CHIP
CAPACITOR

BIAS INPUT
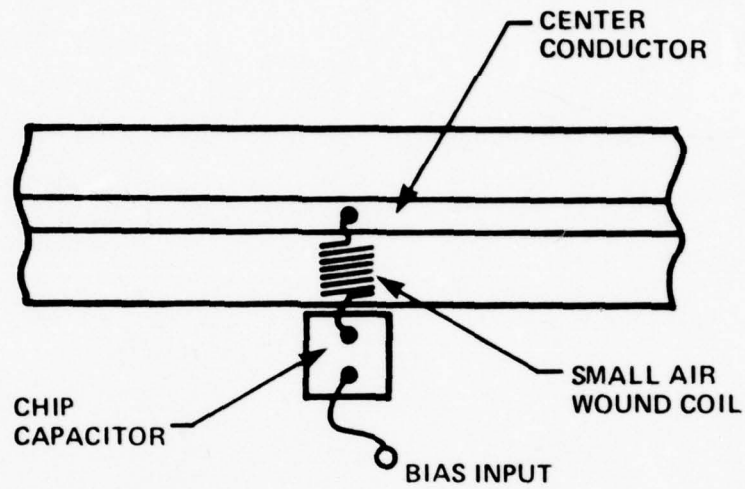
EQUIVALENT CIRCUIT
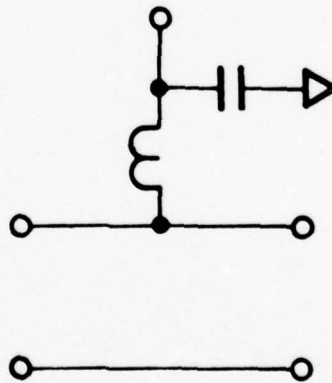
FIGURE 24. BIAS CIRCUIT

D-16959

THE ALL SHUNT SP2T

All of the switches except the SP4T utilize the shunt
SP2T circuit. An equivalent circuit for this design is shown
in Figure 25. In this circuit, one diode is forward biased and
the other reverse biased. The quarter-wave section transforms
the low impedance of the forward biased diode to a high impedance
at the junction. The transmission path then exhibits the band-
pass as shown in Figure 25. The quarter-wave sections are made
40 ohms to increase the width of the bandpass. The choice of
the all shunt design for high power, fast switching designs is
based on two considerations. First, the diodes can be soldered
directly to the case allowing heat to be efficiently removed
from the diodes and second, the full reverse voltage from the
driver can be applied to the diode which improves the switching
speed.

SHUNT DIODE "T" CIRCUIT SWITCH

Figure 25 shows simplified T junction with shunt diodes.
The shorting diode producing a quarter-wave short stub at the
T junction. This stub is broadbanded by making all 3 lines
40 ohm for a 50 ohm input impedance. A computer generated
curve of this broadbanding of the "T" junction is shown in
Figure 26.[1] The four curves were generated with all three lines
changed from 50 to 45, 40, and 35 ohms. In an actual circuit,
the two arms of the "T" are made slightly shorter ($\sim.22 \wedge$ long)
when the inductance of the shunt diodes is used to compensate
for the capacitance of the diode as a passing circuit.

---

[1] (Ref) "Computer Analysis of Microwave Integrated Switches",
H. Stinehelfer, IEEE Int'l Microwave Symposium, 1967.

CIRCUIT

QUARTER WAVE SECTIONS
3 PLACES

40Ω SECTIONS

OUTPUT

OUTPUT

SHUNT DIODE

INPUT
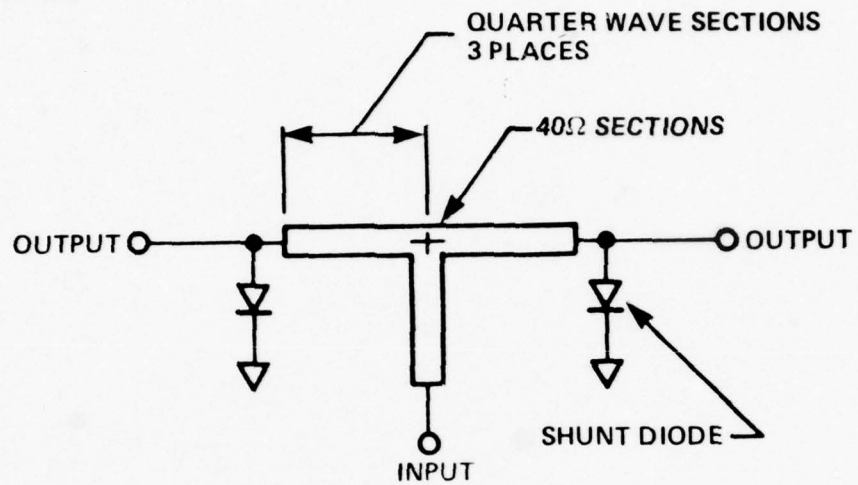
BANDPASS CHARACTERISTIC

VSWR

1.2:1 MAX.
OVER
OCTAVE
BAND

F_1 F_O F_2
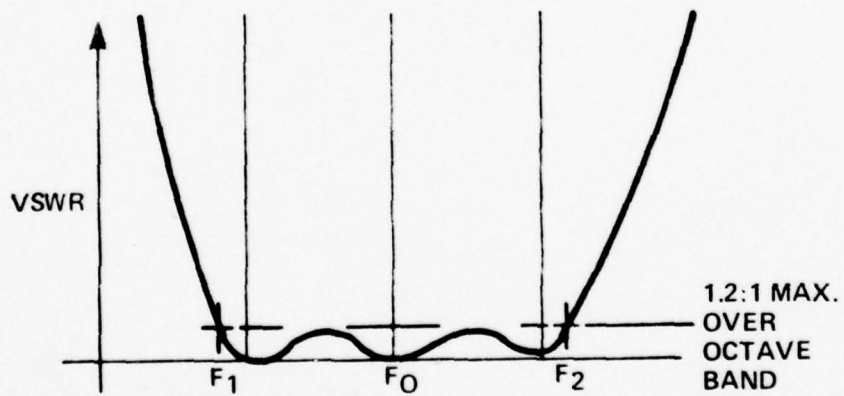
FIGURE 25. ALL SHUNT SP2T CIRCUIT   D-16968

-53-
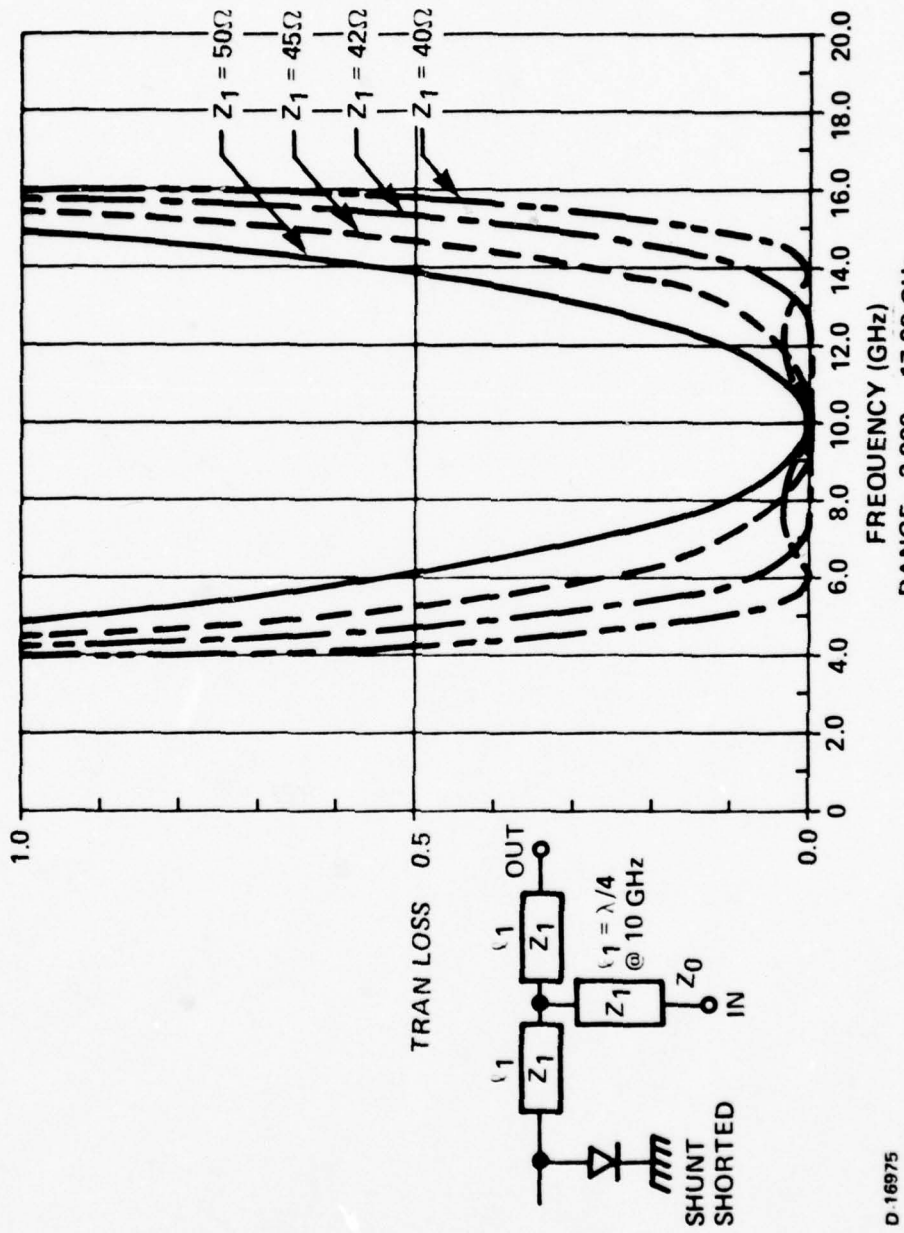
FIGURE 26 OPTIMUM T JUNCTION IMPEDANCE FOR SP2T SWITCH

D-16975

INDIVIDUAL SWITCH DISCUSSION

I. TRANSFER SWITCH

Figure 27 shows a diagram of the transfer switch. The basic design consists of four back to back SP2T switches. The internal arrangement is depicted in Figure 28. Essential design features include physical symmetry. This is essential to maintain amplitude and phase balance through each signal path. Two diodes are used in each signal path to achieve the 50 dB isolation.

All of the switches, except the high power SP2T, use a diode similar to the type 2 diode used in the Phase I study program, and a driver of the type A design (this choice based on the speed/power specifications).

Referring to the Transfer Switch data in Appendix I, nearly all of the specifications were met. The insertion loss and VSWR far exceed expectations.

The major difficulty on this design was achieving phase balance of +/- 1 to +/- 2 degrees. Two problem areas were encountered. The first is a mechanical problem of cutting and centering the circuit with nearly perfect symmetry. In the frequency range of interest and with the dielectric material chosen, one degree of phase error is created with only .001 to .002 inches of asymmetry. Better tolerance control could be achieved with other dielectric materials, but they would not be suitable due to either excessive loss or high dielectric constant. A second factor is measurement accuracy. The test data was taken on a computer controlled network analyzer which
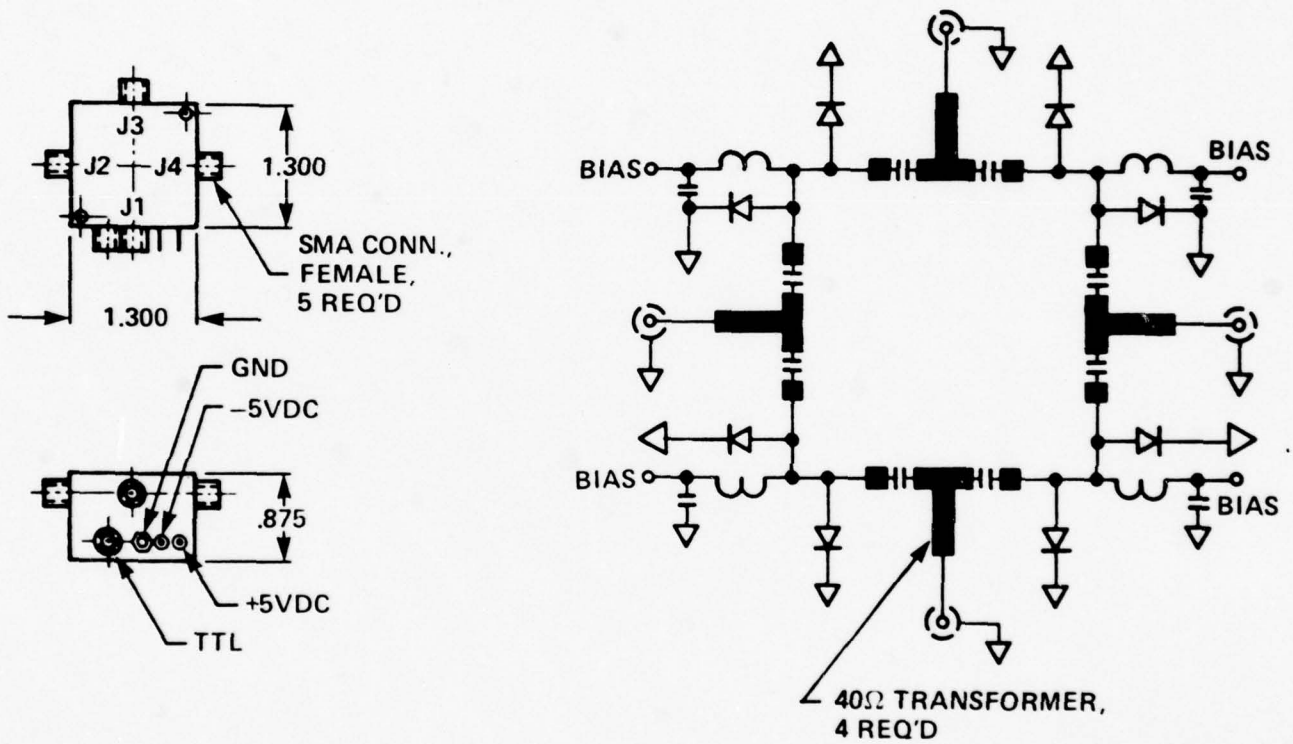
FIGURE 27. TRANSFER SWITCH (-1)

D-16973
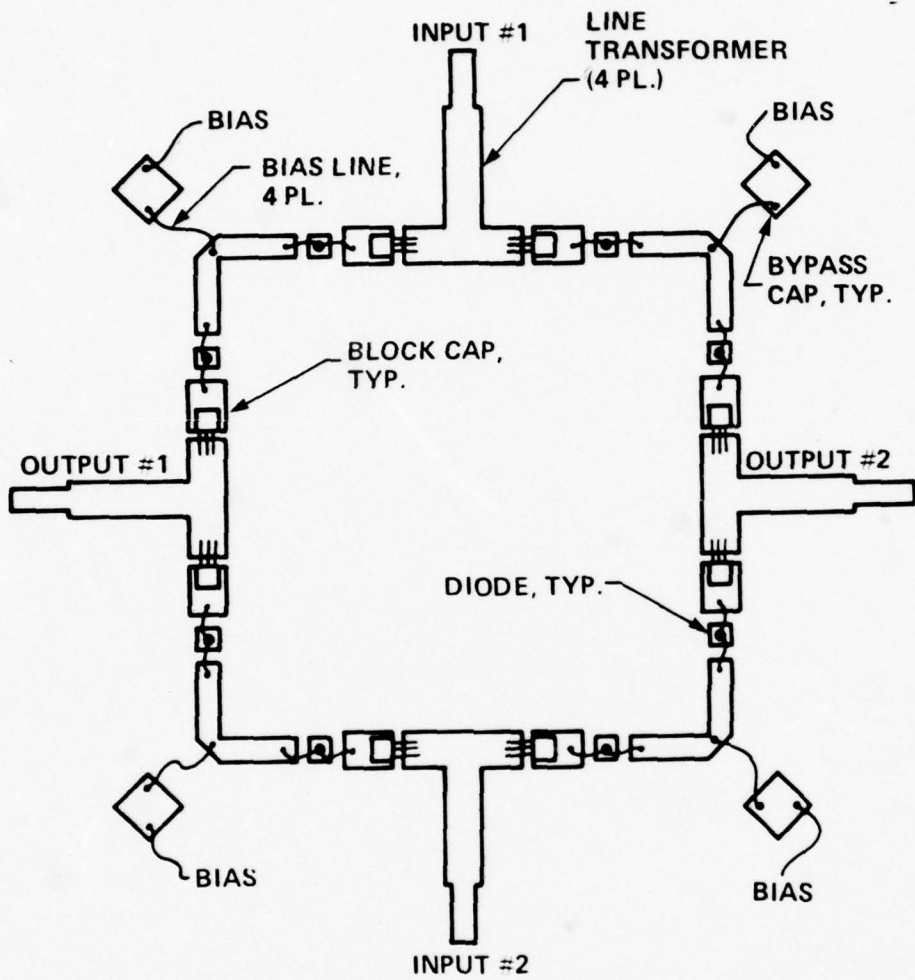
FIGURE 28. TRANSFER (-1) RF ASSEMBLY

D-16974

corrects for detectable system errors in the calibration process. Despite the automatic corrections, the uncertainty is specified as +/- 1°. The final test results for the phase and amplitude unbalance are summarized below:

Phase Variations:

J1 Input	2.1°	(12 - 18 GHz)
	2.5°	(7 - 18 GHz)
J3 Input	4.3°	(12 - 18 GHz)
	4.4°	(7 - 18 GHz)

Amplitude Variations:

J1 Input	.17 dB	(12 - 18 GHz)
	.22 dB	(7 - 18 GHz)
J3 Input	.21 dB	(12 - 18 GHz)
	.33 dB	(7 - 18 GHz)

The complete data is shown in the Appendix.

As with all switches (except SP2T, High Power), the switch was operated at 5 watts CW (into a 2:1 termination) under both the on and off conditions. Based on available data, it would be expected that the diode used in this switch could handle considerably more power than 5 watts. No tests were conducted at higher levels to preclude switch burn-out.

II. SP2T

The internal design details of the high power SP2T (Item 5) design is shown in Figure 29. Again, the all shunt design is used and the output ports are terminated in internal 50 ohm resistors to provide constant VSWR matching. The requirements that the output ports be matched under all conditions preclude making this switch with one, two, and three diodes. This is due to the fact that each of the SP2T switches depends on

-58-

TO DRIVER
BYPASS CAP,
4 PL.

TO DRIVER

BIAS LINE
(.005 WIRE)

TO DRIVER

TO DRIVER

DIODE, TYP.
(10 MIL
STRAPS)

OUTPUT
#2

INPUT

OUTPUT
#1

50Ω INTERNAL
TERMINATION,
2 PL

λ/4 TRANSFORMER, 3 PL.

DC BLOCK
CAP., TYP.
(10 MIL
STRAPS)
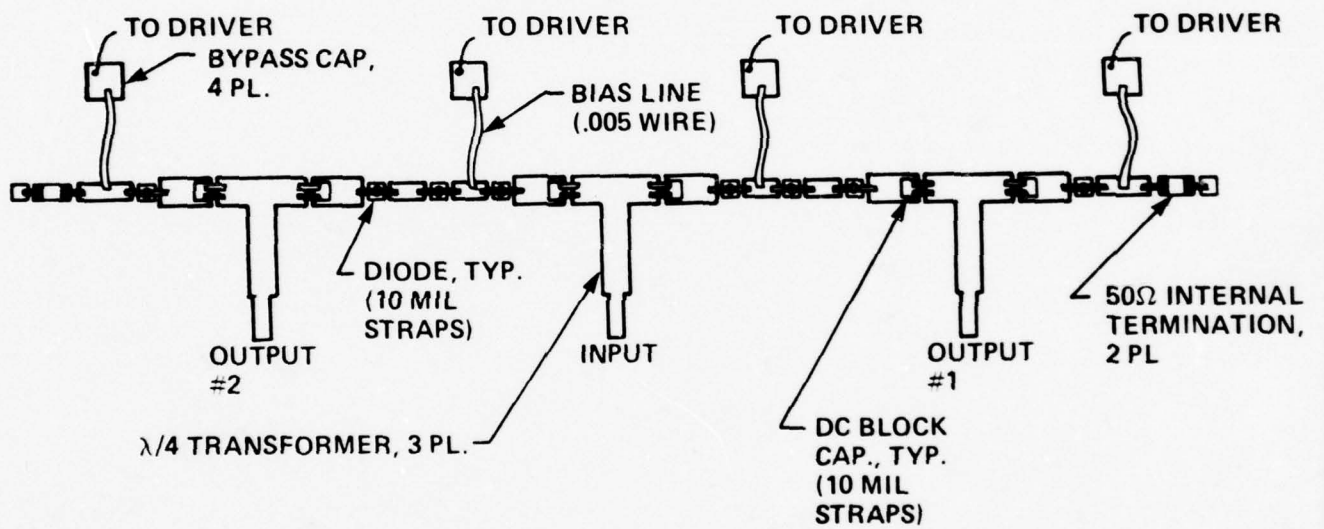
FIGURE 29. SP2T (5) RF ASSEMBLY

D-16966

BIAS   BIAS   BIAS   BIAS

OUT   IN   OUT

GND

TTL FOR J2

+5VDC

+15VDC

−35VDC

TTL FOR J1

SMA CONN.,
FEMALE
5 REQ'D

2.000

2.000

J2

J3

J1

.750
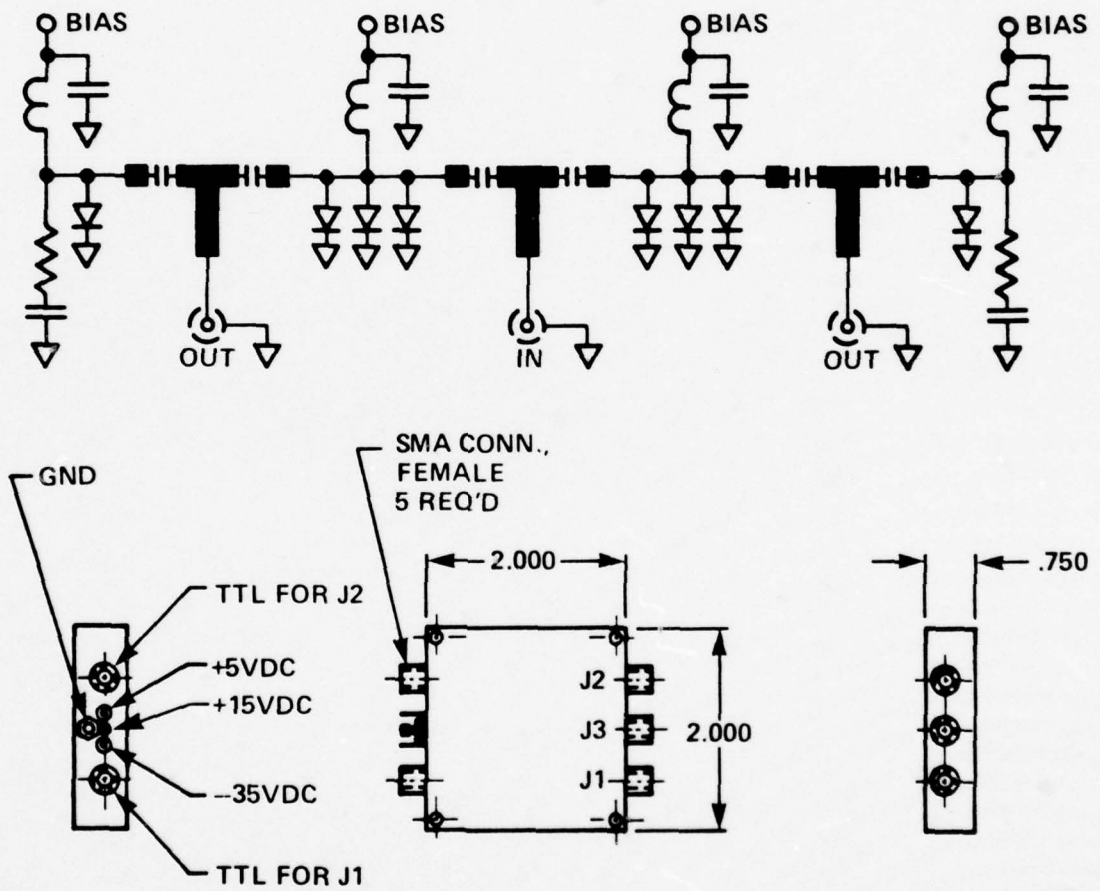
FIGURE 30. SP2T-5

D-16972

-60-

diode location. With one half inch connector spacing, at least three diodes per arm are required to maintain proper circuit performance. For this reason, the switch performance exhibited higher loss and VSWR than originally anticipated. The isolation on the other hand is much better than required. Without the requirement that the output ports be matched in the off condition, the loss and VSWR could be improved significantly. The configuration for this switch is shown in Figure 30.

The phase tolerance on this device also deviated significantly from the requirement. The phase difference between the two switch paths varied from 4.9 to 8.5 degrees in the 12 to 18 GHz band. The variations are introduced by the same mechanisms discussed on the transfer switch. Amplitude balance meets the +/- .2 dB spec over most of the 12 - 18 GHz band. The complete data is presented in the Appendix.

III. SP4T

Due to the bandwidth requirements, the SP4T utilizes the series/shunt design outlined earlier. In particular, the Quad diode was utilized at the junction. This diode consists of 4 PIN junctions etched onto a single .020 x .020 inch section of silicon. The advantages of this approach are simplicity and reduced junction size resulting in lower parasitic inductance. The physical configuration of the SP4T is shown in Figure 31.

The performance of the switch did not meet all of the design expectations. This was attributed to two principle problem areas. One is lack of uniformity from diode to diode on the

-61-

1.500 DIA.

3.000

3.000

+5VDC

SMA CONN.,
FEMALE,
72° SPACING,
5 REQ'D

.500

1.500

-5VDC

'X' INPUT (SMC)

'Y' INPUT (SMC)

GND

J2
(REPEAT J1 CKT)

J3
(REPEAT J1 CKT)

BIAS

OUTPUT
(J1)

J4
REPEAT
J1 CKT)

QUAD CHIP

HIGH PASS
FILTER
(TYP.)

INPUT
(J5)
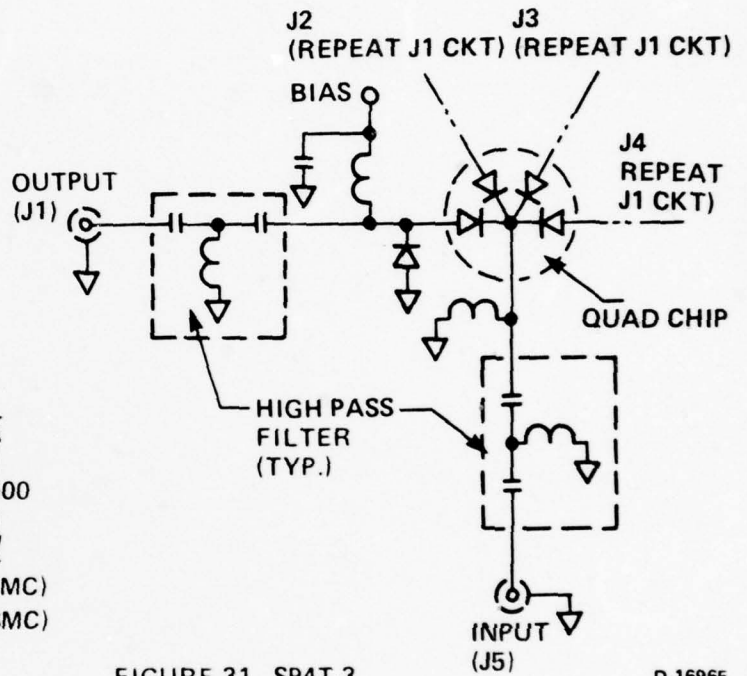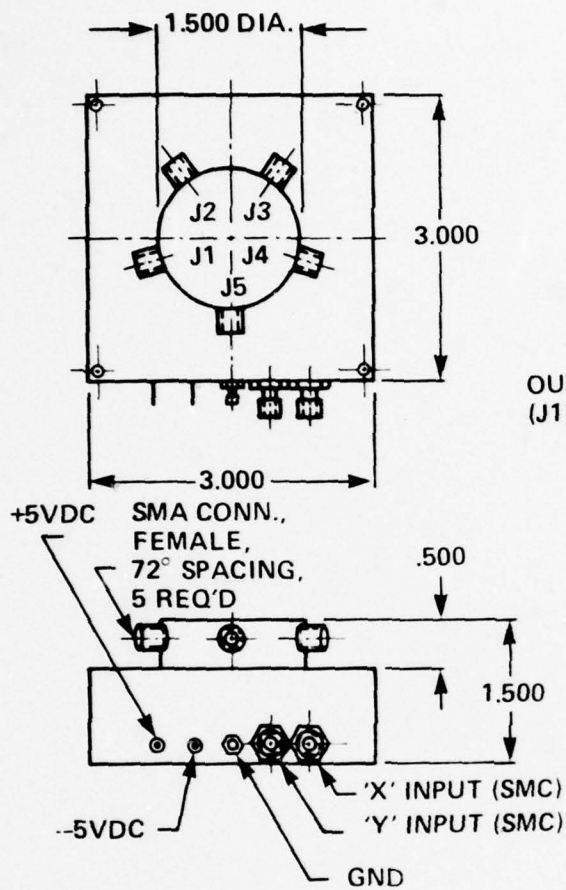
FIGURE 31. SP4T-3

D-16965

Quad chip. This variation in the C_J and R_S of the diodes results in considerable amplitude unbalance from channel to channel. Several Quad chip diodes were tried, but the variation was consistent. Solution to the program appears to be a processing problem and further study would be required to determine the value of this approach. A second problem with the Quad chip is the small size which although good from a theoretical point of view, is difficult from an assembly standpoint. To connect the diode into the circuit requires four successive thermocompression bonds onto a single chip. Consistent difficulty was encountered in getting good bonds on all four contacts. The yields were lower than normal and the time of assembly increased dramatically for the Quad diode switch. Figure 32 shows a detail of the Quad junction and a conventional junction. Notice especially the difference involved in bonding the series diodes.

Despite these difficulties, the concept does show significant merit. It is felt that the diode to diode uniformity can be improved to a consistent level. The assembly difficulties would be reduced by slightly increasing the size of the chip to approximately .030 x .030 inches, and utilizing a substrate with a harder composition than the Duroid used in these switches.

The initial data is shown in the Appendix. The unit had been returned to Microwave Associates to be reworked to improve performance. The results are included in a supplement to this report. The intricacy of this design approach precluded significant improvement in the available time frame of this program.

-63-

QUAD JUNCTION ← .020 SQUARE

INPUT ARM
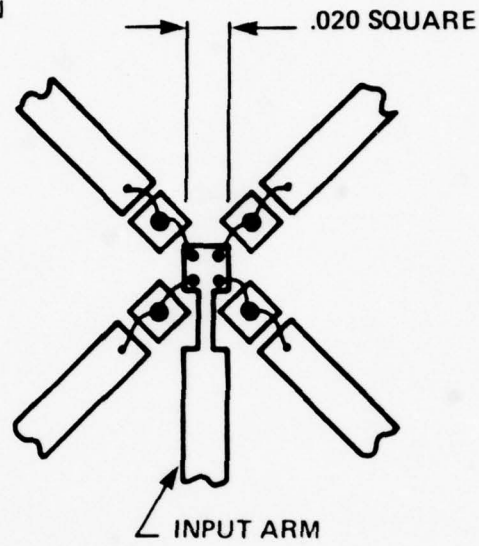
CONVENTIONAL JUNCTION (TO SAME SCALE)

INPUT ARM
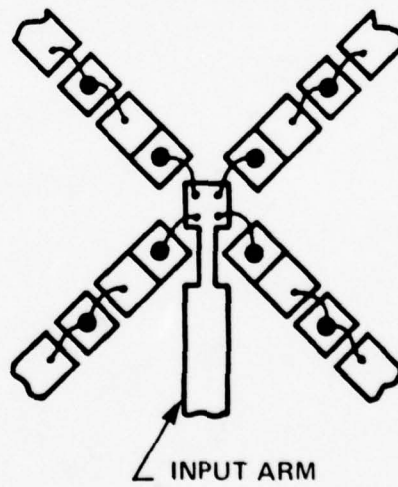
FIGURE 32. SP4T CIRCUIT DETAILS

As shown in the data in Appendix I, the prime problem was with insertion loss which runs to slightly over 5 dB. It was hoped to reduce this to about 4.0 - 4.5 dB on this unit. On the plus side, our testing shows that the switch can handle as much as 8 watts CW. This would still allow the specified output level to be maintained despite higher switch loss. (The final data is shown at the end of the Appendix.)

IV. SP2T

Figures 33 and 34 show the construction details of this switch. Most of the requirements of this switch were less stringent than the others. Performance was generally good. VSWR exceeded the specification at a few points in the band, due primarily to the additional filter circuit in the switch which was required to suppress video components to under 2V. Actually, video levels into a 50 ohm load were approximately 50 millivolts.

As shown in Appendix I, the performance of this switch was good. Loss was a full .5 dB better than specification. Switching speed was also considerably faster than required. Of some interest here is a comparison of the amplitude tracking. Over the full band, the maximum deviations were +.36 and -.22 dB (spec was +/- .4 dB). Over most of the band, the deviation was only +/- .2 dB or better. The principle reason for this is the physical simplicity of the circuit and small overall size. In any future developments, it would be prudent to emphasize these factors in the circuit layout.

TTL FOR J1
TTL FOR J2
-12VDC
.500
GND
+12VDC

1.500
2.000
J1 J2
J3
SMA CONN.,
FEMALE,
5 REQ'D.

OUTPUT
(J2)

HIGH
PASS
FILTER

BIAS

40Ω TRANSFORMER

INPUT
(J3)

BIAS

HIGH
PASS
FILTER

OUTPUT
(J1)

FIGURE 33. SP2T-4

D-16961

-66-

TO DRIVER

BYPASS C.A.P., 2 PL.

BIAS LINE, 2 PL.

OUTPUT #2

TO DRIVER

OUTPUT #1

DIODE
TYP.

BLOCK CAP.,
2 REQ'D

HIGH PASS FILTER
2 PL. (AS SHOWN)

LINE
TRANSFORMER
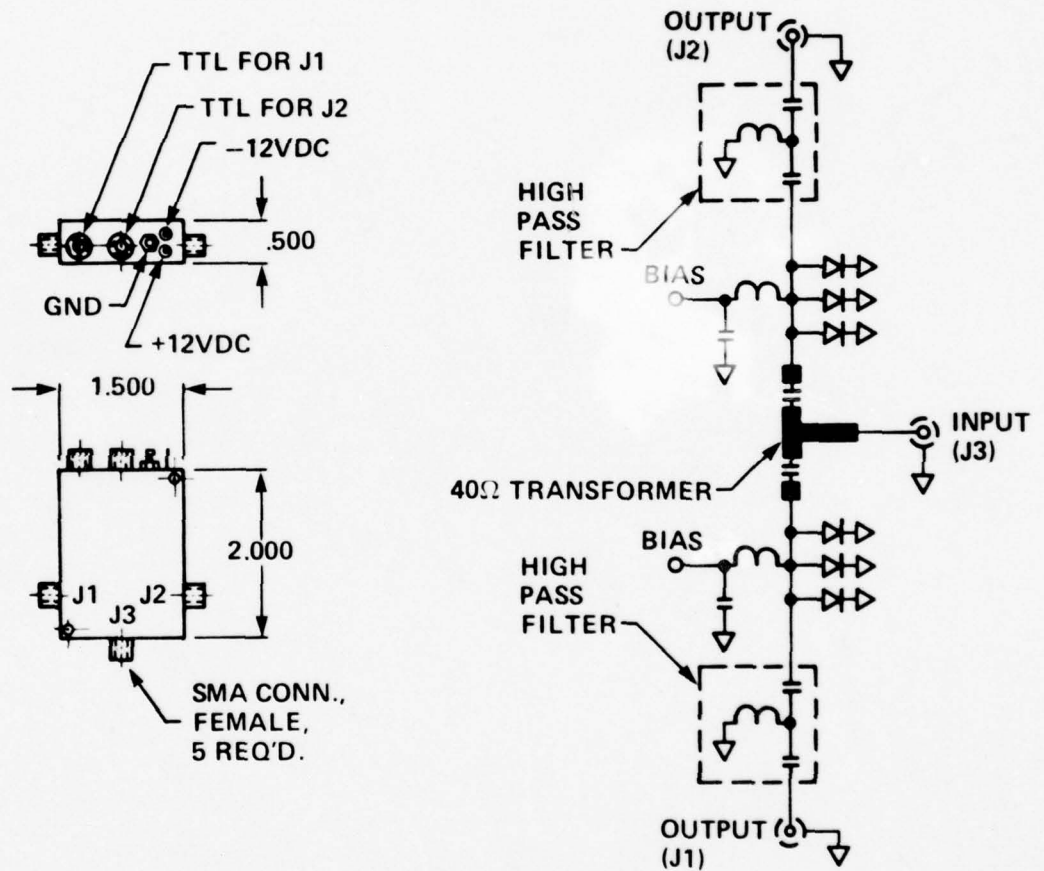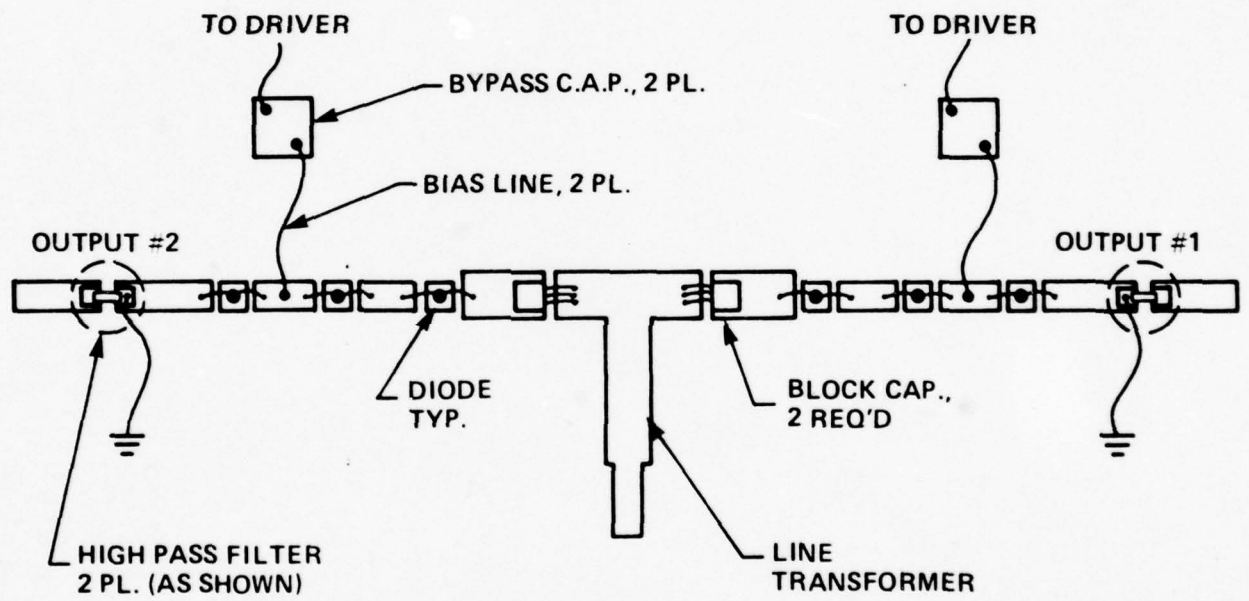
FIGURE 34. SP2T (-4) RF ASSEMBLY

D-16962

-67-

V. SP2T, HIGH POWER

The basic design of this switch follows closely the design
of the -2 SP2T (See Figure 35 and 36). To handle the higher
power levels, three component selections are altered. First,
the diode is considerably thicker, a diode of the type 4 design
was selected (approximately 30 microns I layer) with bias levels
of +60 mA and -35V. Second, the driver is a high power type
similar to the type -B driver of the diode study. Finally,
the circuit components are increased to size. This includes
DC blocks, bias lines, and diode straps as shown in Figure 5.

Due to the higher capacitance of the 30 micron diode, the
insertion loss ran about 0.5 dB higher than the spec. Other
steady state parameters were close to spec. The switching
speed and high power testing showed better than expected per-
formance. All switching time data exceeded even the design
goals of the program.

The results of the high power/hot switching tests is
shown in Figure 37. Figures 38 and 39 show the test set and
the resultant oscilloscope displays for this test. The device
functioned to 600W peak/30W average power. With a thicker
diode, this could be increased somewhat at some degradation
in switching speed.

Figure 37 shows a timing diagram which defines the relation-
ship of the RF response to the TTL control. The response is
broken into two components. First, the "RF transition time"
which is the time required for the RF power level to change from

BIAS   BIAS   BIAS   BIAS

50Ω   50Ω

OUT   IN   OUT

GND

SMA CONN.,
FEMALE,
5 REQ'D.

TTL FOR J2

+5VDC

←——— 2.000 ———→   .500 →||←

J2

J3   2.000

−5VDC

J1

TTL FOR J1

FIGURE 35. SP2T-2

D-16963

−69−

TO DRIVER
BYPASS CAP, 4 PL.
BIAS LINE, 4 PL.
TO DRIVER
TO DRIVER
TO DRIVER

DIODE, TYP.
OUTPUT #2
INPUT
DC BLOCK CAP., TYP.
OUTPUT #1
50Ω INTERNAL TERMINATION, 2 PL.
λ/4 TRANSFORMER, 3 PL.
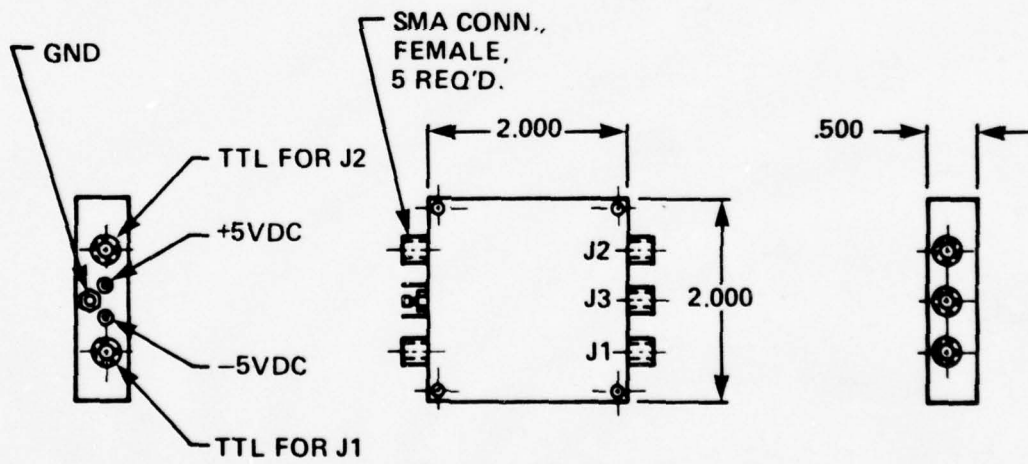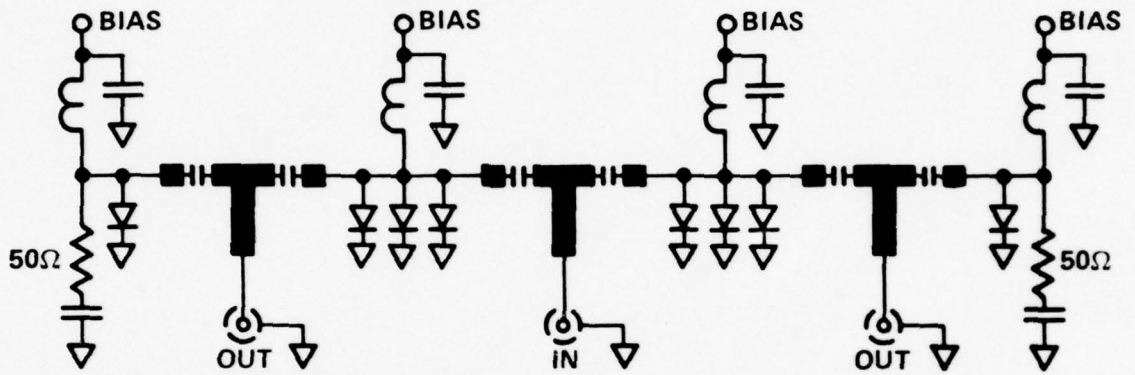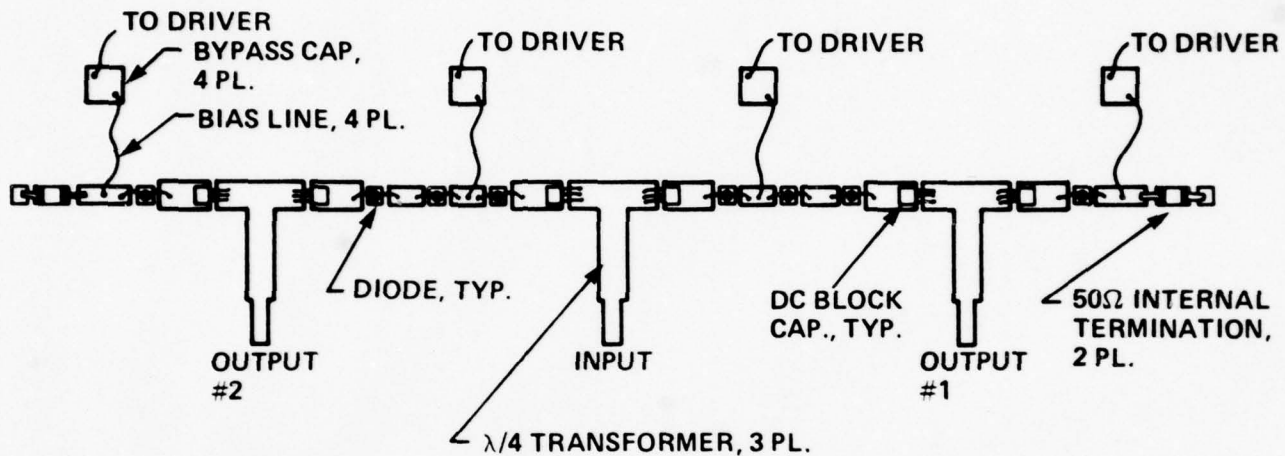
FIGURE 36. SP2T (-2) RF ASSEMBLY

D-16964

-70-
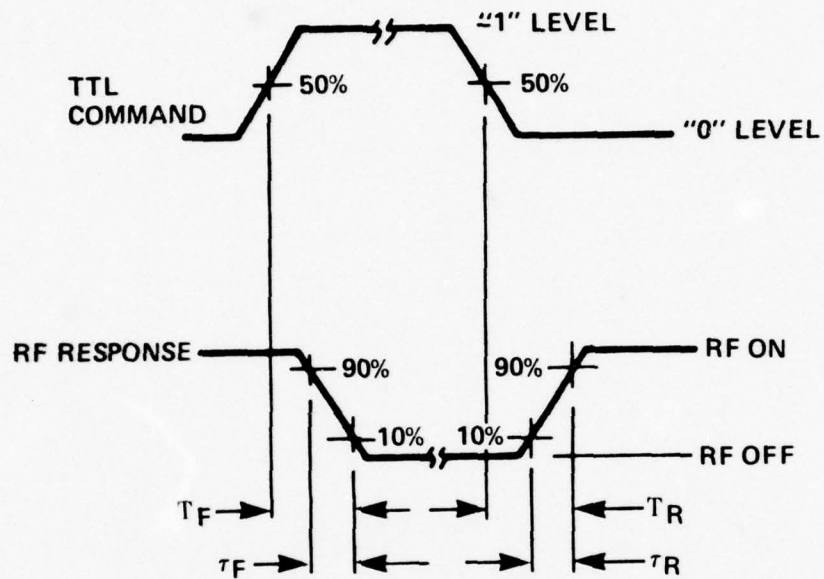
TEST RESULTS

RF TRANSITION TIME   ON   25 - 30 ns
                                 OFF 15 - 20 ns
TOTAL SWITCH TIME   ON   45 - 50 ns
                                 OFF 75 - 80 ns

FIGURE 37. TIMING DIAGRAM — SP2T (#5)

D-16970

-71-

16 GHz SOURCE

MODULATOR

AMPLIFIER

50Ω TERM

J1

J3

J2

SP2T (#5)

TTL CONTROL

PAD

DETECTOR

SYNC

PULSE GEN

OUTPUT (INCL DELAY)

CH1

CH2

SYNC

SCOPE
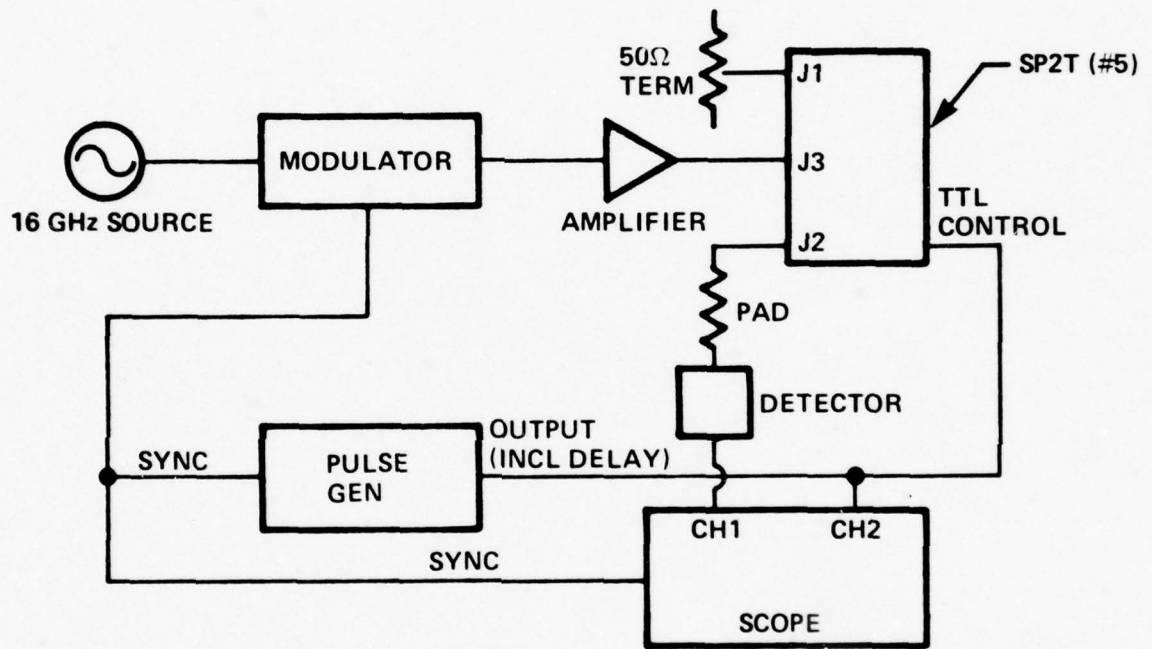
NOTE: PULSE GENERATOR OUTPUT IS DELAYED TO SWITCH THE SP2T DURING THE RF PULSE ON INTERVAL (SEE FIGURE 33).

FIGURE 38. HOT SWITCHING TEST SET

D-16969
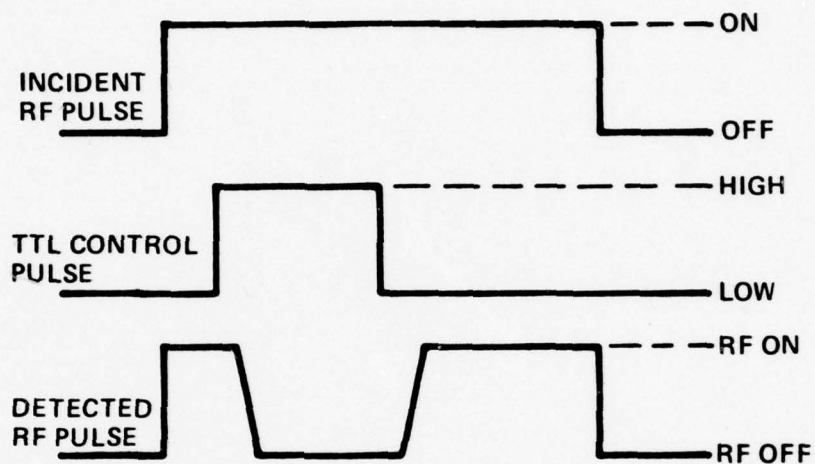
TEST CONDITIONS:

INCIDENT RF PULSE 1μs WIDE @ 50 KHz PRF
TTL CONTROL PULSE .5μs WIDE @ 50 KHz DELAYED APPROXIMATELY 100 ns WITH
RESPECT TO THE RF PULSE.

THE INCIDENT LEVEL WAS INCREASED IN 100 WATT STEPS TO 500 WATTS AND LEFT
OPERATING FOR ½ HOUR.
DELAY AND TRANSITION TIMES REMAINED STABLE.
THE POWER LEVEL WAS THEN INCREASED TO 600 WATTS FOR 15 MINUTES. THE UNIT
FAILED GOING TO 700 WATTS. THE MODE OF FAILURE WAS A SHORT CIRCUITED DIODE.

FIGURE 39. TIMING DIAGRAM — HOT SWITCHING

D-16971

10% to 90% of the static level. The second is the "total switching time" which is referenced to the 50% level on the TTL input; this includes the effects of driver delay. As shown in the tabulation, all switching times were considerably less than the original design specifications.

The critical tests on this device was the "hot switching test". Figure 38 shows the test kit arranged to perform this test. The low level signal generator output is first modulated with a pulse generator synchronization pulse to produce an RF pulse 1 μsec long which is duplicated at a 50 KHz rate. This pulse is then amplified and applied to the switch. The amplifier output level can then be set to the required peak and average power levels of the specification.

The pulse generator output is delayed with respect to the incident RF pulse and the duration adjusted to approximately 500 nanoseconds. This in effect, turns the switch off and on during the RF pulse-on intervals. The test began with an incident level of 100 watts peak/5 watts average, and was increased in 100 watt peak steps (the average remained at 5% of the peak). The switch was allowed to remain in each state for 30 minutes. The switch functioned properly up to the 500 watt peak level per the specification. As agreed upon, the power level was increased. The switch worked at 600 watts peak power successfully. Failure occurred instantaneously when the power was increased to 700 watts. The mode of failure was a short circuit diode caused by peak burn-out. The timing diagram for this test is shown in

Figure 39. Comparing this to the data generated in Phase I, we see excellent correlation. Figure 5 shows a peak burn-out of 600 watts peak for this diode type.

As indicated earlier, line impedance could be adjusted to equalize the theoretical burn-out levels for a given set of operating conditions. For instance, CW burn-out in the "on" and "off" switch states could be equalized with such a change. However, the bandwidths would be decreased. In some cases, the desired line impedance would be impractically low or high.

CONCLUSIONS

Tables 6 through 10 present a comparison of specification
and actual performance for the significant parameters for the
five switches built under this program. The final column in
each tabulation evaluates that parameter according to the
following format:

- indicates nominal conformance with the specification
  and includes minor variances

+ indicates performance significantly better than
  specified

X indicates out-of-spec condition

* indicates performance better than the design goal
  (design goals were eliminated from the listing
  for clarity)

Because power handling and switching speed were the prime
program goals, these parameters were emphasized. In this
respect, all of the switches performed well. With the exception
of the SP4T switch, all devices also performed well statically.
The SP4T switch utilized a new concept of execution. Despite
the problems of this approach, it merits still stand clear,
and should not be discarded without further study.

ITEM 1 - TRANSFER SWITCH

(Actual vs Specification)

PARAMETER	SPECIFICATION	ACTUAL	RESULTS
Frequency (GHz)	12-18	12-18	-
Peak Power (watts)	5	5	-
Average Power (watts)	5	5	-
* Loss (dB)	3.8	2.3	+
Isol (dB)	50	52	-
* VSWR	1.8	1.4	+
Tracking (dB)	$\pm$ .2	$\pm$ .2	+
Transition speed (ns)	3	2	-
Total Speed (ns)	12	10	-
Phase Tracking	$\pm 1°$	$\simeq +/- 5°$	X

NOTES:

* = exceeds design goal
- = nominally meets spec
+ = significantly exceeds spec
X = fails to meet spec

TABLE 6

-77-

ITEM 2 - SP2T SWITCH

(Actual vs Specification)

PARAMETER	SPECIFICATION	ACTUAL	RESULTS
Frequency (GHz)	12-18	12-18	-
Peak Power (watts)	5	5	-
Average Power (watts)	5	5	-
Loss (dB)	2.7	2.8	-
Isol (dB)	40-50	70	+
VSWR (IN)	1.7	1.83	-
VSWR (OUT)	1.7	1.73	-
Tracking (dB)	$\pm$ .2	$\pm$ .4	X
Transition speed (ns)	3	2	-
Total speed (ns)	15	8	+
*Phase	$\pm$ 1°	$\approx 4 - 6°$	X

*includes test set error

NOTES:

* = exceeds design goal
- = nominally meets spec
+ = significantly exceeds spec
X = fails to meet spec

TABLE ___7___

ITEM 3 - SP4T SWITCH

(Actual vs Specification)

PARAMETER	SPECIFICATION	ACTUAL	RESULTS
Frequency (GHz)	$F_L - F_H$	$F_L - F_H$	-
Peak Power (watts)	5	8	+
Average Power (watts)	5	8	+
Loss (dB)	3.5	5	X
Isol (dB)	35	30	X
VSWR	2.0	2.2	-
Tracking (dB)	$\pm$ .4	> 1	X
Transition Time (ns)	4	5	-
Total Speed (ns)	12	15	-
Video (mV)	50	40-50	-

NOTES:

* = exceeds design goal
- = nominally meets spec
+ = significantly exceeds spec
X = fails to meet spec

TABLE   3

-79-

ITEM 4 - SP2T SWITCH

(Actual vs Specification)

PARAMETER	SPECIFICATION	ACTUAL	RESULTS
Frequency (GHz)	F_L-F_H	F_L-F_H	-
Peak Power(watts)	2	5	+
Average Power(watts)	2	5	+
Loss (dB)	2.9	2.4	+
Isol(dB)	60	62	-
VSWR	2.0	2.1	-
Tracking (dB)	$\pm$ .4	$\pm$ .3	+
Transition time(ns)	8	4	-
Total speed (ns)	20	14	-
Video (volts)	2	.05	+

NOTES:

* = exceeds design goal
- = nominally meets spec
+ = significantly exceeds spec
X = fails to meet spec

TABLE   9

ITEM 5 - SP2T SWITCH - HIGH POWER

(Actual vs Specification)

PARAMETER	SPECIFICATION	ACTUAL	RESULTS
Frequency (GHz)	12-18	12-18	-
Peak Power (watts)	500	600	+
Average Power (watts)	25	30	+
Loss (dB)	2.4	3.1	X
Isol (dB)	35	55	+
VSWR	1.7	1.8	-
Tracking (dB)	$\pm$ .2	$\pm$ .4	X
* Transition time (ns)	60	30	+
Total Speed (ns)	90	80	+
Phase	$\pm$ 1°	-6.7°	X

NOTES:

* = exceeds design goal
- = nominally meets spec
+ = significantly exceeds spec
X = fails to meet spec

TABLE   10

-81-

- APPENDIX I

SWITCH DATA

TRANSFER SWITCH DATA (#1)

MPM-238

P542R ATP# 1P-2 AUGUST,24TH,1978 DAY= 236 TIME= 17: 1: 55
6219
MPS-23H
P/N 271058

FRFO J1-J2 VSWR	J1-J2 LOSS-DB	J1-J2 PHASE	J1-J2 ISOL-DB	J1-J4 VSWR	J1-J4 LOSS-DB	J1-J4 PHASE	J1-J4 ISOL-DB
FL 2.19	2.71	-49.9	54.51	2.15	2.81	-58.4	56.56
2.06	2.39	-142.8	55.56	2.08	2.57	-143.6	59.83
2.06	2.31	123.3	57.15	2.19	2.47	-123.4	59.45
2.46	2.66	33.7	57.97	2.67	2.68	34.2	59.86
2.15	2.22	-54.8	58.35	2.37	2.43	-53.7	59.28
2.07	2.28	-146.1	59.11	2.27	2.39	-144.8	59.56
1.88	2.12	-126.4	59.02	2.47	2.32	-128.6	58.11
1.34	1.72	35.8	60.54	1.44	1.84	38.3	58.76
1.34	1.76	-54.8	61.59	1.34	1.79	-52.6	61.63
1.14	1.76	-145.1	62.14	1.08	1.77	-142.8	61.32
1.39	1.89	-126.0	62.36	1.34	1.83	128.1	62.46
1.33	1.86	36.3	61.89	1.29	1.79	38.4	62.96
1.48	2.05	-52.9	63.48	1.40	1.94	-58.9	63.08
1.29	1.92	-141.4	66.26	1.21	1.81	-139.6	58.93
1.26	1.97	-128.8	71.15	1.14	1.83	138.5	74.22
1.38	2.09	-39.7	70.55	1.18	1.92	41.1	72.18
1.25	2.01	-49.4	63.98	1.14	1.89	-48.6	65.28
1.39	2.19	-139.6	60.92	1.30	2.08	-138.5	61.64
1.32	2.13	130.8	58.80	1.26	2.06	131.7	58.71
1.36	2.28	39.8	57.64	1.32	2.24	41.0	57.25
1.33	2.27	-50.1	56.00	1.38	2.29	-48.9	55.55
1.12	2.28	-142.2	54.79	1.23	2.24	-146.3	53.82
FH 1.13	2.42	125.2	53.79	1.22	2.44	127.2	52.67
MIN 1.12	1.72	-146.1	53.79	1.08	1.77	-144.8	52.07
MAX 2.46	2.71	130.8	71.15	2.67	2.88	131.7	74.22
DELTA 1.34	.98	276.9	17.36	1.59	1.11	276.6	21.55

REF PLANE EXT(CM): INPUT= .000 TRAN= .000

R542R ATP# 1R-2 AUGUST,24TH,1978 DAY= 236 TIME= 17: 2: 4
6219
MPS-23R
B/N 271058

FREQ   D-LOSS   D-PHASE
       LOSS-DB PHASE

FL

LOSS-DB	PHASE
-.10	.5
-.18	.2
-.16	-.1
-.22	-.5
-.21	-1.1
-.19	-1.3
-.20	-1.7
-.12	-2.5
-.02	-2.2
-.01	-2.3
-.06	-2.1
-.07	-2.1
-.12	-2.0
-.11	-1.9
-.15	-1.6
-.17	-1.4
-.13	-1.4
-.12	-1.0
-.06	-.9
-.04	-1.2
-.02	-1.3
-.05	-1.9
-.02	-2.0

FH

MIN	-.22	-2.5
MAX	.17	.5
DELTA	.39	3.0

REF PLANE EXT(CM): INPUT= .000 TRAN= .000

8542R ATP# 10-2 AUGUST,24TH,1978 DAY= 236 TIME= 17: A: 32
6219
MPS-238
B/N 271058

FREQ	J3-J2 VSWR	J3-J2 LOSS-DB	J3-J2 PHASE	J3-J2 ISOL-DB	J3-J4 VSWR	J3-J4 LOSS-DB	J3-J4 PHASE	J3-J4 ISOL-DB
F_L	2.05	2.95	-43.7	54.51	1.94	2.62	-48.2	56.24
	1.86	2.56	-137.8	57.03	1.87	2.38	-140.9	55.74
	1.87	2.39	127.8	57.05	1.95	2.25	-125.3	57.65
	2.25	2.69	36.8	57.16	2.40	2.66	35.3	58.13
	2.02	2.34	-52.3	57.02	2.17	2.29	-52.9	58.76
	1.98	2.36	-143.8	59.19	2.09	2.29	-143.8	59.52
	1.85	2.33	-128.6	60.06	1.96	2.28	-129.0	60.38
	1.33	1.92	38.7	60.99	1.38	1.84	39.0	60.69
	1.31	1.95	-52.1	61.63	1.29	1.81	-50.8	61.54
	1.15	1.87	-142.5	61.13	1.07	1.82	-146.9	62.42
	1.45	1.98	128.3	62.53	1.37	1.96	-136.3	63.43
	1.41	1.99	38.5	63.12	1.35	1.82	41.6	63.83
	1.56	2.12	-50.6	63.81	1.49	2.66	-47.9	56.32
	1.33	2.06	-139.4	66.27	1.26	1.85	-136.3	71.82
	1.35	2.10	131.1	66.81	1.29	1.90	-133.8	72.12
	1.32	2.18	42.3	66.14	1.27	2.00	45.6	67.67
	1.16	2.07	-46.9	62.43	1.12	1.91	-44.6	63.84
	1.22	2.19	-136.9	59.70	1.15	2.05	-134.2	68.29
	1.18	2.16	133.3	57.38	1.15	2.05	-136.2	58.61
	1.23	2.31	42.4	55.95	1.25	2.25	45.4	57.44
	1.23	2.38	-47.7	54.67	1.33	2.29	-44.1	56.03
	1.05	2.38	-139.3	53.08	1.14	2.28	-135.6	54.26
F_H	1.12	2.58	129.1	52.18	1.07	2.43	-133.0	52.69
MIN	1.05	1.87	-143.8	52.18	1.07	1.81	-143.8	52.69
MAX	2.25	2.95	133.3	66.81	2.40	2.66	136.2	72.12
DELTA	1.20	1.08	277.1	14.78	1.33	.85	286.0	19.43

REF PLANE EXT(CM): INPUT= .000 TRAN= .000

-86-

6219
MPS-238
B/N 271058

FREQ	D-LOSS LOSS-DB	D-PHASE PHASE
FL	.33	4.4
	.18	3.1
	.14	2.5
	.03	1.5
	.05	.6
	.07	.0
	.05	-.4
	.08	-.9
	.09	-1.2
	.05	-1.6
	.08	-2.0
	.08	-2.4
	.12	-2.6
	.15	-3.0
	.21	-2.7
	.18	-2.7
	.16	-3.0
	.15	-2.7
	.11	-2.9
	.06	-3.1
	.02	-3.6
	.18	-4.3
FH	.14	-3.9
MIN	.02	-4.3
MAX	.33	4.4
DELTA	.31	8.7

REF PLANE EXT(CM): INPUT= .000 TRAN= .000

SP2T SWITCH DATA (#2)

MPM-239

8540R ATPN 19-2 AUGUST,24TH,1978 DAY= 236 TIME= 18: 12: 36
6219
PPS-239
S/N 0001

FREQ	J3-J1 VSWR	J3-J1 LOSS-DB	J3-J1 PHASE	J3-J1 ISOL-DB	J3-J2 VSWR	J3-J2 LOSS-DB	J3-J2 PHASE	J3-J2 ISOL-DB
F_L	1.19	1.56	-164.2	82.03	1.27	1.72	-157.3	81.68
	1.25	1.49	-213.5	88.40	1.34	1.54	-207.1	85.92
	1.49	1.65	-251.6	86.05	1.35	1.60	-256.3	91.76
	1.31	1.54	-308.9	85.07	1.27	1.59	-304.2	85.33
	1.41	1.62	-356.3	86.01	1.06	1.55	-351.7	86.50
	1.32	1.68	-403.5	86.51	1.26	1.76	-399.6	88.37
	1.70	1.97	-449.2	88.07	1.66	2.05	-444.8	86.58
	1.66	2.05	-493.8	86.26	1.74	2.17	-489.9	86.24
	2.01	2.45	-538.8	83.14	2.23	2.71	-534.2	84.86
	1.91	2.33	-581.7	84.58	2.15	2.54	-576.2	85.23
	1.66	2.18	-626.3	90.44	1.03	2.35	-620.1	88.82
	1.18	1.88	-671.4	92.15	1.39	1.86	-665.1	85.48
	1.06	1.81	-718.2	87.52	1.29	1.82	-712.1	89.76
	1.16	1.88	-764.1	89.35	1.20	1.86	-758.0	102.06
	1.14	1.92	-809.8	91.15	1.18	1.95	-803.5	91.23
	1.13	1.96	-856.2	78.55	1.14	1.94	-849.8	89.03
	1.18	2.00	-902.1	82.03	1.19	1.96	-895.4	82.69
	1.35	2.14	-949.0	85.40	1.11	1.96	-941.6	85.41
	1.37	2.23	-994.5	79.53	1.13	2.08	-987.9	79.06
	1.44	2.40	-1042.4	84.62	1.23	2.22	-1035.3	78.05
	1.44	2.45	-1086.8	80.96	1.22	2.22	-1082.0	75.62
	1.26	2.43	-1136.9	79.87	1.17	2.34	-1130.2	77.73
F_H	1.39	2.71	-1185.3	74.14	1.09	2.44	-1179.4	76.20
MIN	1.06	1.49	-1185.3	74.14	1.06	1.54	-1179.4	75.62
MAX	2.01	2.71	-164.2	91.15	2.23	2.71	-157.3	102.06
DELTA	.94	1.22	1021.1	17.02	1.17	1.17	1022.1	26.44

-89-
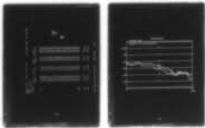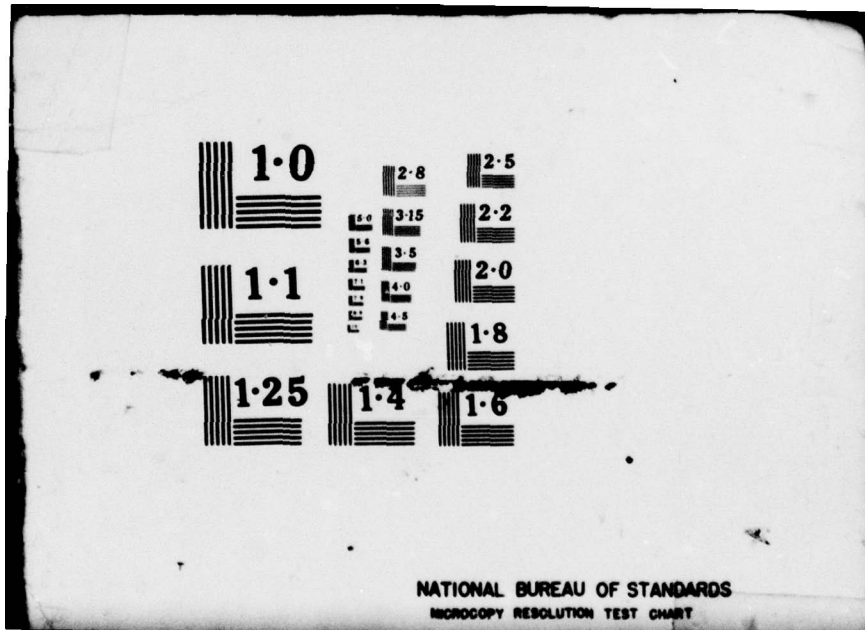
NATIONAL BUREAU OF STANDARDS
MICROCOPY RESOLUTION TEST CHART

8542R ATP# 19-2 AUGUST,24TH,1978 DAY= 236 TIME= 18: 19: 44
6219
PPS-239
S/N 0001

FRFQ	1/2 REF LOSS-DB	1/2 REF PHASE
F_L	.16	6.9
	.06	6.4
	-.05	5.3
	-.05	4.8
	-.07	4.6
	-.08	3.9
	-.08	4.5
	.13	3.9
	.27	4.6
	.21	5.5
	.17	6.2
	-.02	6.3
	-.01	6.1
	-.02	6.1
	-.03	6.3
	-.01	6.5
	-.03	6.7
	-.18	7.4
	-.15	6.6
	-.18	7.1
	-.25	6.0
	-.09	6.6
F_H	-.27	5.9
MIN	-.27	3.9
MAX	.27	7.4
DELTA	.53	3.5

REF PLANE EXT(CM): INPUT= .000 TRAN= .000

-90-

SP4T SWITCH DATA (#3)

MPM-240

07/ 28/ 1977   DAY= 209   TIME= 15: 13: 31

MPH=240

FREQ	J5-J3 VSWR	J5-J3 LOSS-DB ISOL	J5-J3 ISOL	J5-J3 D-LOSS	J5-J4 VSWR	J5-J4 LOSS-DB ISOL	J5-J4 ISOL	J5-J4 D-LOSS
F_L	1.38	2.96	60.02	.34	1.48	2.02	60.02	.19
	1.38	2.43	58.64	.58	1.38	2.12	57.08	.46
	1.39	2.28	56.33	.44	1.43	2.16	55.77	.27
	1.42	2.35	57.08	.46	1.39	2.17	54.03	.24
	1.55	2.45	53.96	.57	1.40	2.38	51.97	.27
	1.34	2.75	58.72	.87	1.20	2.67	56.59	.39
	1.25	2.87	62.36	.81	1.20	2.92	60.98	.58
	1.25	2.66	56.71	.37	1.43	2.66	58.73	.37
	1.17	2.77	55.35	.28	1.42	2.74	54.73	.44
	1.16	2.68	52.67	.58	1.38	2.81	51.56	.34
	1.14	2.96	52.25	.56	1.16	2.89	49.92	.39
	1.23	2.93	52.38	.45	1.16	2.76	49.38	.33
	1.04	2.98	49.25	.36	1.17	3.05	46.85	.33
	1.19	3.54	31.65	.37	1.36	3.73	31.90	.48
	1.56	3.45	40.23	.45	1.78	3.43	40.14	.74
	1.66	3.68	52.33	.55	2.11	3.75	55.96	.62
	1.88	3.50	44.19	.68	2.19	3.53	46.88	.71
	1.76	3.91	34.95	1.14	2.11	3.77	37.14	1.67
	1.48	3.96	53.78	.95	1.69	4.29	53.84	1.27
	1.44	3.92	49.23	.39	1.66	4.15	47.14	.61
	1.17	4.48	49.59	-.22	1.33	4.93	47.52	.88
	1.12	4.56	51.65	-.12	1.19	4.98	49.96	-.11
F_H	1.51	4.57	52.67	-1.33	1.98	5.19	51.83	-.99
MIN	1.04	2.96	31.65	-1.33	1.16	2.02	31.90	-.99
MAX	1.88	4.57	62.36	1.14	2.19	5.19	60.98	1.27
DELTA	.84	2.51	30.71	2.47	1.09	3.17	29.03	2.25

RF TRANSITION TIME   5 ns
TOTAL SPEED   15 ns

-92-

FREQ	J5-J1 VSWR	J5-J1 LOSS-DB	J5-J1 ISOL	J5-J1 D-LOSS	J5-J2 VSWR	J5-J2 LOSS-DB	J5-J2 ISOL	J5-J2 D-LOSS
F_L	1.48	1.82	61.61	.11	1.56	2.39	48.68	.08
	1.39	8.09	58.55	-.02	1.52	2.51	48.88	.02
	1.41	1.91	56.99	.88	1.51	2.47	39.44	.68
	1.31	1.92	55.83	.85	1.48	2.53	39.67	.07
	1.39	2.05	54.64	.88	1.51	2.66	42.28	.85
	1.21	2.43	56.32	.85	1.34	2.87	48.82	.82
	1.16	2.27	60.48	-.83	1.25	3.81	47.23	.65
	1.24	2.26	60.84	-.88	1.38	3.96	48.87	.71
	1.21	2.39	56.25	.84	1.35	3.99	37.26	.83
	1.19	2.44	52.89	-.88	1.27	3.22	35.48	.75
	1.07	2.45	58.25	-.82	1.16	3.48	34.53	.88
	1.28	2.59	49.96	.83	1.17	3.36	34.73	.98
	1.83	3.07	49.12	-.98	1.37	3.92	36.28	.81
	1.24	2.97	58.82	-.82	1.76	4.06	48.79	.81
	1.62	3.07	53.35	.45	2.11	4.26	44.59	1.19
	1.98	3.22	56.28	.32	2.10	4.17	39.33	1.38
	1.93	3.12	54.39	.38	1.88	4.13	34.44	1.28
	1.64	3.13	56.65	.34	1.46	4.34	32.68	1.35
	1.33	3.45	49.84	.84	1.37	4.64	32.26	1.37
	1.55	3.33	48.97		1.19	5.07	32.81	1.34
	1.27	4.33	47.72	-.88	1.18	5.12	33.61	1.84
	1.68	4.08	48.96		1.67	5.28	37.18	1.86
F_H	1.54	4.38	51.28	-.81			39.62	1.88
MIN	1.03	1.82	47.72	-.06	1.16	2.39	32.21	.02
MAX	1.93	4.33	61.61	.45	2.11	5.28	48.88	1.37
DELTA	.90	2.51	13.89	.53	1.01	2.88	16.61	.76

NRL-3

SP2T SWITCH DATA (#4)

MPM-241

85425 05/01/1977   DAY= 121   TIME= 17: 39: 43
3503-390
MPX=641

FREQ	IN-J1 VSWR	IN-J1 LOSS-DB	IN-J2 VSWR	IN-J2 LOSS-DB	IN-1/2 LOSS-DB
F$_L$	1.76	1.78	1.81	2.15	.36
	1.83	1.91	2.04	2.16	.26
	1.91	1.61	2.09	1.84	.23
	1.58	1.29	1.69	1.32	.12
	1.35	1.31	1.38	1.39	.08
	1.13	1.24	1.27	1.39	.16
	1.21	1.32	1.33	1.41	.09
	1.40	1.47	1.41	1.60	.13
	1.48	1.51	1.48	1.72	.21
	1.40	1.51	1.55	1.71	.20
	1.30	1.78	1.55	1.96	.26
	1.23	1.72	1.48	1.92	.24
	1.32	1.67	1.59	1.84	.17
	1.59	1.72	1.84	1.88	.16
	2.00*	2.04	2.05	2.19	.15
	2.33*	1.95	2.05	2.03	.08
	2.19	1.72	1.79	1.74	.03
	1.65	1.68	1.45	1.68	.06
	1.44	1.99	1.34	1.77	-.22
	1.77	1.71	1.55	1.72	.01
	1.97	2.24	1.78	2.33	.09
	1.75	2.45	1.76	2.39	-.05
F$_H$	1.51	1.86	1.53	1.92	.16
MIN	1.13	1.20	1.27	1.32	-.22
MAX	2.33	2.45	2.09	2.39	.36

REF PLANE EXT(CM): INPUT= .005   TRAN= .005

*MEASURED AS 2.10 ON BENCH TEST

NRL-4

RF TRANSITION TIME   < 4 ns
SWITCHING SPEED   < 14 ns

84628 25/ 01/ 1977   DAYS 121   TIME= 17: 45: 31

3503-090

MPY=731

NRL-4

FREQ   TN-J1   TN-J2
        ISOI -DB TSOL-DB

F_L
        69.01   66.04
        67.97   64.04
        74.97   74.23
        69.94   65.89
        75.09   65.43
        75.38   71.35
        77.51   67.40
        68.73   71.41
        66.36   53.84
        65.14   64.28
        58.68   70.13
        71.34   75.46
        69.36   70.72
        65.27   66.95
        66.66   67.27
        67.21   63.97
        66.34   65.69
        63.17   55.66*
        53.12   82.76
        74.07   76.41
        66.53   76.46
        68.21   67.11
        68.86   68.05

F_H

MIN   53.12   55.06

MAY   77.41   82.76

REF FLANE FXTENT= TEDITS   .394 TRANS   .000

-96-

SP2T SWITCH DATA (#5)

MPM-242

```
8542B  05/06/1077   DAYS 126        TIME:  22: 48: 43
3563-356
MPM-242
S/N 271571
```

FREQ	IN-J1 VSWR	IN-J1 LOSS-DB	IN-J1 PHASE	IN-J1 ISOL-DB	IN-J2 VSWR	IN-J2 LOSS-DB	IN-J2 PHASE	IN-J2 ISOL-DB
FL	1.75	3.55	60.9	56.86	1.72	2.82	58.5	55.99
	1.68	2.65	28.2	57.43	1.59	2.37	24.8	66.14
	1.50	2.21	-5.3	50.41	1.37	2.18	-9.3	62.25
	1.24	2.10	-39.6	50.04	1.12	2.27	-42.3	57.76
	1.08	2.19	-70.5	61.71	1.14	2.21	-72.7	68.35
	1.54	2.36	-101.3	55.29	1.39	2.25	-102.0	61.77
	1.62	2.27	-132.1	73.43	1.68	2.08	-133.6	64.97
	1.78	2.65	-162.5	68.90	1.85	2.27	-165.2	64.60
	1.85	2.68	162.8	67.09	1.86	2.26	165.8	69.74
	1.80	2.51	140.4	67.07	1.81	2.37	135.6	67.54
	1.81	2.64	111.8	69.17	1.72	2.35	186.6	68.82
	1.64	2.47	82.5	60.41	1.63	2.43	76.5	67.83
	1.60	2.05	51.5	56.41	1.63	2.42	44.8	67.79
	1.49	2.58	21.5	66.15	1.55	3.13	16.3	66.38
	1.53	2.74	-9.1	55.29	1.61	3.22	-19.8	69.81
	1.41	2.35	-33.3	50.07	1.88	3.02	-38.2	68.46
	1.73	2.08	-62.6	62.47	2.00	2.59	-66.0	66.39
	1.39	2.47	-94.6	68.15	1.98	2.27	-94.9	65.96
	1.05	2.54	-127.2	67.46	1.68	2.47	-131.5	68.99
	1.33	2.69	-157.0	68.05	1.15	2.73	-162.3	68.78
	1.63	2.59	172.7	66.04	1.19	2.71	158.4	67.34
	1.63	2.74	141.1	64.46	1.57	2.71	136.1	67.73
FH			107.4	65.62	1.62	2.72	103.3	68.35
MIN	1.08	2.04	-162.5	55.29	1.12	2.08	-165.2	55.99
MAX	1.88	3.09	172.7	73.48	2.00	3.13	168.4	69.74

REF PLANE EXTEND: INPUT   .000 TRANS .000

FOR SWITCHING TIMES SEE TEXT

MPM-242
NRL-5

B542P 05/06/1077   DAYS 126   TIME= 22: 48: 51

3503-000
MPF=2.2?
S/N 271?7?
FREQ TN=?0/J2 TN=11/J3
REF LOSS REF PH03

F_L   -.20   -2.3
           -.28   -3.?
           -.11   -4.0
           -.08   -2.8
           -.02   -1.9
           -.16   -1.6
           -.23   -1.5
           -.41   -2.7
           -.37   -4.5
           -.31   -4.7
           -.21   -5.1
           -.17   -5.5
           -.05   -6.7
           -.19   -5.6
           -.21   -5.8
           -.28   -5.0
           -.24   -4.?
           -.10   -4.3
           -.1?   -4.8
           -.19   -4.4
           -.02   -4.2
           -.1?   -5.1
           -.02   -4.1

F_H

MIN   -.41   -6.7

MAX   .28   -1.5

REF PLANE EXTERN)? INPUTS .41? TRANS .???

SUPPLEMENTARY DATA SP4T (#3)

MPM-240

85423 ATP# 11-2 12/ 12/ 1977   DAY= 283 TIME= 17: 12: 32
6505
SPDT SWITCH
S/N 0001

FREQ	J5-J1 VSWR	J5-J1 LOSS-DB	J5-J1 ISOL-DB	J5-J2 VSWR	J5-J2 LOSS-DB	J5-J2 ISOL-DB	J5-J3 VSWR	J5-J3 LOSS-DB
F_L	2.38	2.62	58.40	1.53	2.17	59.55	1.39	2.07
	2.54	2.69	58.21	1.77	2.37	59.16	1.56	2.38
	2.55	2.69	58.09	1.61	2.46	59.57	1.47	2.33
	1.26	2.33	56.54	1.59	2.46	58.35	1.67	2.43
	1.82	2.34	55.35	1.51	2.58	57.83	1.66	2.54
	1.22	2.44	55.71	1.36	2.69	57.72	1.50	2.65
	1.25	2.51	55.13	1.22	3.06	57.56	1.36	2.86
	1.13	2.34	55.68	1.26	2.75	57.55	1.20	2.73
	1.24	2.43	53.93	1.27	2.78	56.60	1.23	2.85
	1.25	2.56	53.68	1.23	2.96	56.65	1.66	2.99
	1.21	2.74	52.24	1.18	3.19	56.29	1.68	3.06
	1.31	2.80	51.14	1.25	3.24	56.37	1.61	3.04
	1.33	2.88	52.38	1.44	3.53	56.47	1.18	3.36
	1.67	3.36	51.94	1.95	4.09	58.81	1.55	3.70
	1.64	3.25	51.22	2.54	4.63	54.58	1.76	3.89
	2.32	3.54	51.45	2.62	4.61	57.83	2.39	3.96
	2.70	3.64	52.35	2.49	3.84	57.58	2.42	3.86
	2.57	3.56	52.75	2.41	3.91	57.41	2.07	4.00
	2.17	3.54	52.35	1.74	3.87	56.42	1.90	4.04
	1.75	3.75	52.45	1.74	4.06	56.23	1.72	4.19
	1.52	4.36	52.63	1.71	4.57	55.41	1.69	4.51
	1.15	4.49	48.55	1.16	5.14	53.71	1.89	4.82
F_H	1.32	4.68	47.44	1.34	4.63	52.01	1.26	4.58
MIN	1.09	2.34	47.44	1.16	2.17	52.01	1.81	2.07
MAX	2.70	4.49	58.44	2.62	5.14	59.58	2.42	4.82

REF PLANE EXT(CM): INPUT=   .000 TRANS=   .000

FREQ	J5-J5 ISUL-DB	J5-J4 VSWR	J5-J4 LOSS-DB	J5-J4 ISUL-DB
FL	59.52	1.63	2.21	58.52
	59.25	1.66	2.41	54.26
	59.08	1.55	2.44	53.56
	57.65	1.49	2.43	56.65
	56.73	1.44	2.53	55.52
	56.21	1.23	2.65	55.59
	55.62	1.23	2.91	54.94
	56.13	1.23	2.73	55.35
	55.44	1.31	2.76	54.32
	55.53	1.29	3.06	54.77
	54.96	1.21	3.17	53.94
	55.05	1.24	3.20	53.41
	54.91	1.16	3.43	55.62
	57.49	1.61	3.98	58.26
	56.55	2.14	4.23	58.24
	55.23	2.74	4.23	55.93
	53.82	2.49	4.65	55.28
	53.05	2.56	4.63	53.46
	52.84	2.23	4.47	51.96
	51.79	1.91	4.31	50.69
	49.87	1.64	5.12	49.53
	48.33	1.24	5.36	49.48
FH	44.67	1.52	5.19	51.21
MIN	46.33	1.21	2.21	49.48
MAX	59.52	2.89	5.36	58.56

REF PLANE EXT(CM): INPUT= .960 TRANS= .000

-102-

SP4T SWITCH #5

MPM 240 - LOSS

J5 INPUT, J1, 2, 3, 4 ARE OUTPUTS

D-16960