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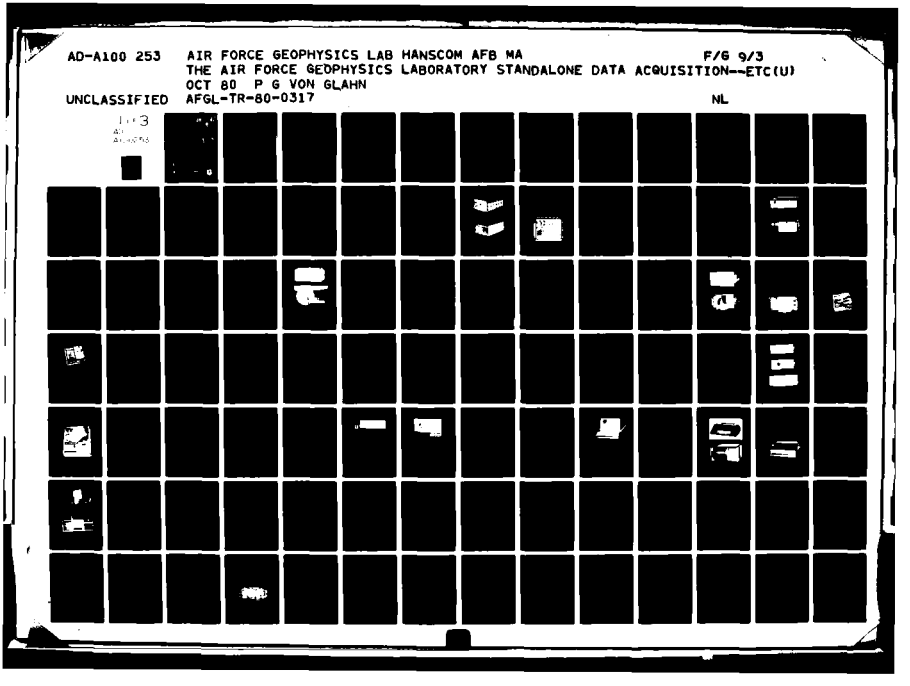

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The Air Force Geophysics Laboratory Standalone Data Acquisition System: A Functional Description

PETER G. VON GLAHN, Capt, USAF

9 October 1980

TERRESTRIAL SCIENCES DIVISION PROJECT 7600
AIR FORCE GEOPHYSICS LABORATORY
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AIR FORCE SYSTEMS COMMAND, USAF

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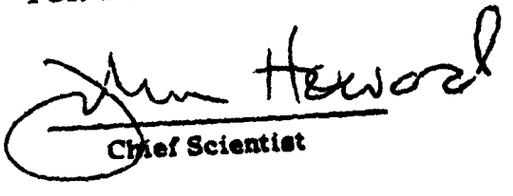

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The Standalone Data Acquisition System (SDAS) is a portable digital data recording system for geophysical field data collection. This report describes the SDAS, giving special emphasis to the SDAS signal conditioning subsystem, which uses custom-designed active filter modules for signal filtering and amplifications. Detailed descriptions of the active filters, including design equations and software, are provided. This subsystem, together with software for its configuration and performance verification, provides an improved

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20. Abstract (Continued)

capability for analog signal conditioning. This report also provides a functional description of the SDAS. It documents the system hardware and such software as is needed for system configuration and checkout. Each subsystem in the SDAS is described via functional descriptions and such diagrams and schematics as are necessary to understand subsystem functioning. Detailed schematics, parts lists, software listings, and subsystem specifications are covered in appendices. References are included.

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The Air Force Geophysics Laboratory Standalone Data Acquisition System: A Functional Description

1. INTRODUCTION

1.1 Report Overview

This report gives a functional description of the Air Force Geophysics Laboratory Standalone Data Acquisition System (SDAS). It documents the system hardware and such software as is needed for system configuration and checkout. This document does not cover either the sensors used with the SDAS or the software used for system operation or data reduction.

The SDAS, as described in the report, represents a refinement of the system described in Syverson, et al (1978).[1] The system has been completely repackaged. All digital interfaces have been redesigned. Furthermore, an entirely new signal conditioning subsystem has been designed and incorporated into the SDAS. This conditioner, together with software for its configuration and performance verification, provides an improved capability for analog signal amplification and filtering.

(Report received for publication 9 October 1980)

1. Syverson, C.R., Blaney, J.I., Hartnett, E.B., and Molineux, C.E. (1978) Geokinetic Environment Studies, AFGL-TR-78-0124, Final Report, Boston College

1.2 Report Organization

Chapter 2 of this report provides an overview of the SDAS subsystems and their interrelationships. Subsequent chapters cover each of the subsystems in detail. These chapters include subsystem descriptions, principles of operation, and such diagrams and schematics as are necessary for the understanding of subsystem functioning. Detailed schematics and specifications are treated in the appendices. Additional references are given so that an interested reader may obtain further information on areas of interest.

2. SYSTEM OVERVIEW

2.1 Purpose of System

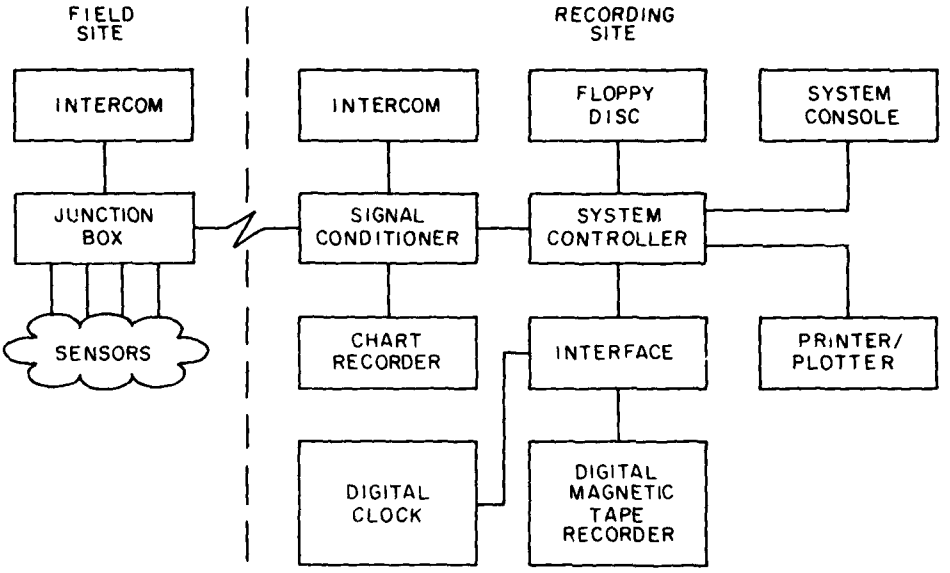
The Standalone Data Acquisition System is a portable digital data recording system for geophysical field data collection. The system accepts analog electrical signals from sensors, conditions the signals, converts them to a digital form, and records the digital information on magnetic tape. While still in the field, the SDAS can be used to do initial analysis of the recorded data.

2.2 System Organization

The SDAS consists of two groups of components; one group is located adjacent to the sensor array and the other is located in a trailer or recording site. The group near the sensor array (see Figure 1) consists of a junction box and an intercom headset. The junction box serves as a connection point for the sensor signal lines. It also includes a power supply for preamplifiers mounted in or adjacent to the sensors. The intercom headset connected to the box provides an easy means of field coordination during equipment setup and maintenance.

A 19-pair shielded cable connects the junction box to the subsystem group located at the recording site. Of the 19, 17 pairs are used for sensor channels. One cable pair is used for sending a calibration signal from the signal conditioner to the junction box for sensor calibration. The 19th pair is used for the intercom channel. Several thousand feet of this cable can be used, depending on the signal levels put out by the sensors or their preamplifiers.

Located at the recording site are the rest of the SDAS subsystems shown in Figure 1. The signal conditioning subsystem provides amplification and analog conditioning (filtering, including anti-alias) of the signals. After conditioning, the analog signals pass to the system controller and an analog strip chart recorder. The recorder provides a continuous record of input signals for real time monitoring and for aiding in later data analysis.



1. SDAS Block Diagram

The controller consists of a small digital computer running under programs stored on the floppy disk memory. An analog-to-digital (A/D) converter, controlled by the computer and located within the controller subsystem, converts the analog signals to digital words. These digital words are then routed to the interface subsystem by the computer.

The interface subsystem contains digital circuitry to interconnect a digital magnetic tape recorder with the computer for recording the digitized data. Also connected to circuitry in the interface subsystem is a digital clock to provide time and date information to the computer. This time and date information is added into the digital data stream by the computer prior to recording on the tape recorder.

A system console connected to the control box provides a means for operator communication with the computer. Graphics output (plots) or listings (printouts) can be either displayed on the console or printed on a printer/plotter connected to the computer.

Customized fiberglass shipping cases are used for transporting the SDAS. The system console and printer/plotter each fit into a foam-padded shipping case. The other SDAS components (except the junction box) fit into shock-mounted equipment racks housed in three fiberglass instrument enclosures. Space has been provided in the racks to transport test equipment (such as an oscilloscope or digital multimeter) for use setup and maintenance of the SDAS.

Although the SDAS is designed for easy transportation, some constraints exist on where it can be used. First, the junction box must be provided with 110 Vac 60 Hz power if any of the sensors used

Table 1 System Specifications

Number of Analog Channels: 16
Power Requirements:
Junction Box: 110 Vac, 0.2 A
Rest of System: 110 Vac, 14.5 A
Operating Temperatures:
Junction Box: -20 to +75 deg C
Rest of System: +15 to +32 deg C *
Electronic:
Signal conditioner circuit board input noise:
12.5 μV (P-P) (dc-200 Hz) **
Signal conditioner circuit board harmonic distortion:
< 0.5% (12 Hz input)
Shipping Weight (Including Cases):
Rack 1 (controller, interface, floppy):
220 lb (99.8 kg)
Rack 2 (recorder, signal conditioner):
171 lb (77.6 kg)
Rack 3 (instrumentation and chart recorder):
221 lb (100.2 kg)
Peripherals:
System console: 106 lb (48.1 kg)
Printer/plotter: 93 lb (42.2 kg)
Shipping Sizes (Including Cases):
Rack 1 (controller, interface, floppy):
36.4 in. H, 24 in. W, 28.5 in. D
(92.5 x 61.0 x 72.4 cm)
Rack 2 (recorder, signal conditioner):
31 in. H, 24 in. W, 29.75 in. D
(78.7 x 61.0 x 72.4 cm)
Rack 3 (instrumentation and chart recorder):
31 in. H, 24 in. W, 29.75 in. D
(78.7 x 61.0 x 72.4 cm)
Peripherals:
System console:
16.5 in. H, 25.5 in. W, 25.5 in. D
(41.9 x 64.8 x 64.6 cm)
Printer/plotter:
12.5 in. H, 28 in. W, 28 in. D
(31.8 x 71.1 x 71.1 cm)

* Limited by floppy disk temperature specifications.

** Input noise rises to approximately 1 mV (P-P) during printing or plotting on the system printer/plotter. Probable cause is a ground loop through the serial interface for the printer/plotter.

require power from its power supply. Second, the box must be located within a few thousand feet of the recording site with the desired signal to noise ratio and cable availability dictating the exact maximum distance. Third, the recording site must provide some degree of climate control (most of the subsystems there use commercial equipment), as well as 110 Vac 60 Hz power for all subsystems.

2.3 System Specifications

Overall system specifications are contained in Table 1. Detailed subsystem specifications are covered in the chapter devoted to each.

3. JUNCTION BOX SUBSYSTEM

3.1 Chapter Overview

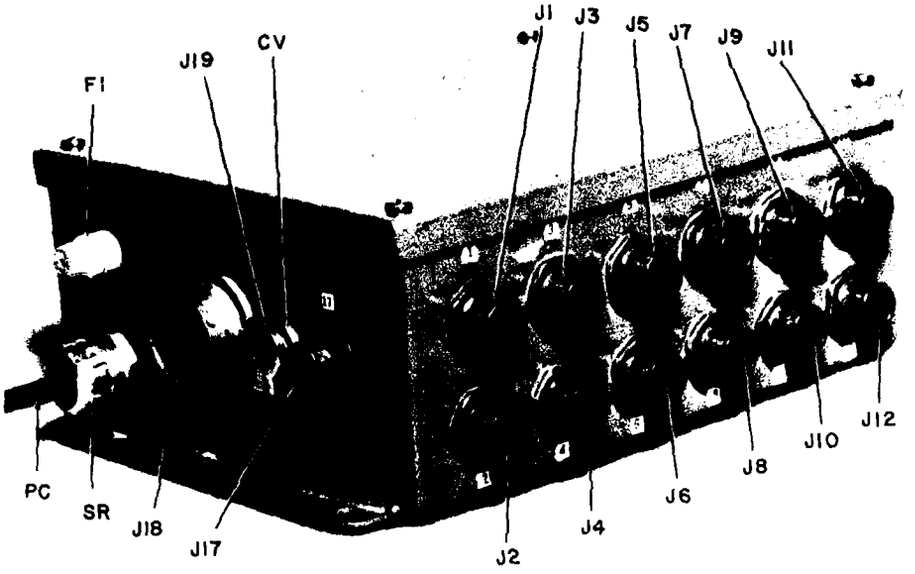
This chapter covers the SDAS junction box. It contains a functional, physical, and electrical description of the box. Also included are parts lists and power and signal wiring diagrams.

3.2 Junction Box Functional Description

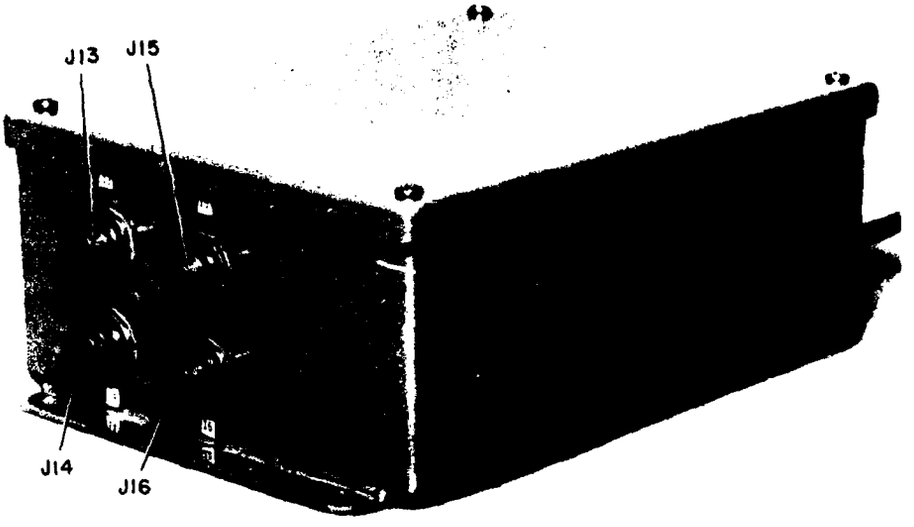
The junction box provides a connection point between the individual sensors and a 19-pair shielded cable connected to the signal conditioning subsystem. Mounted on the box are 17 input connectors, each connected to one pair of conductors in the cable. Another cable pair is used for a calibration signal which is received from the signal conditioning subsystem and routed in parallel to all input connectors. The 19th cable pair connects to a separate jack on the box for use with an intercom headphone. A power supply in the box is connected to all 17 input connectors to provide dc power for the sensors or sensor preamplifiers. The power supply runs on 110 Vac supplied through a separate power cord.

3.3 Junction Box Physical Description

The SDAS junction box (Figures 2 and 3) measures 8 in. (20.3 cm) wide by 10 in. (25.4 cm) deep by 4 in. (10.2 cm) high. It has a removable cover secured by four corner-mounted screws. Mounted on its sides are the connectors for attaching cables from the sensors (labeled J1-J17 in Figures 2 and 3); a connector for the 19-pair cable that connects the box to the signal conditioning subsystem (J18); and a jack for the intercommunications system (J19) protected by a weather-tight dust cover (CV). Also on the side of the box is a water-tight strain relief (SR) for the power cord (PC) supplying 110 Vac, 60 Hz for the internal power supply. A fuse for this power (F1) is also included.



2. Junction Box External View, Showing Side Containing J1 to J12



3. Junction Box External View, Showing Side Containing J13 to J16

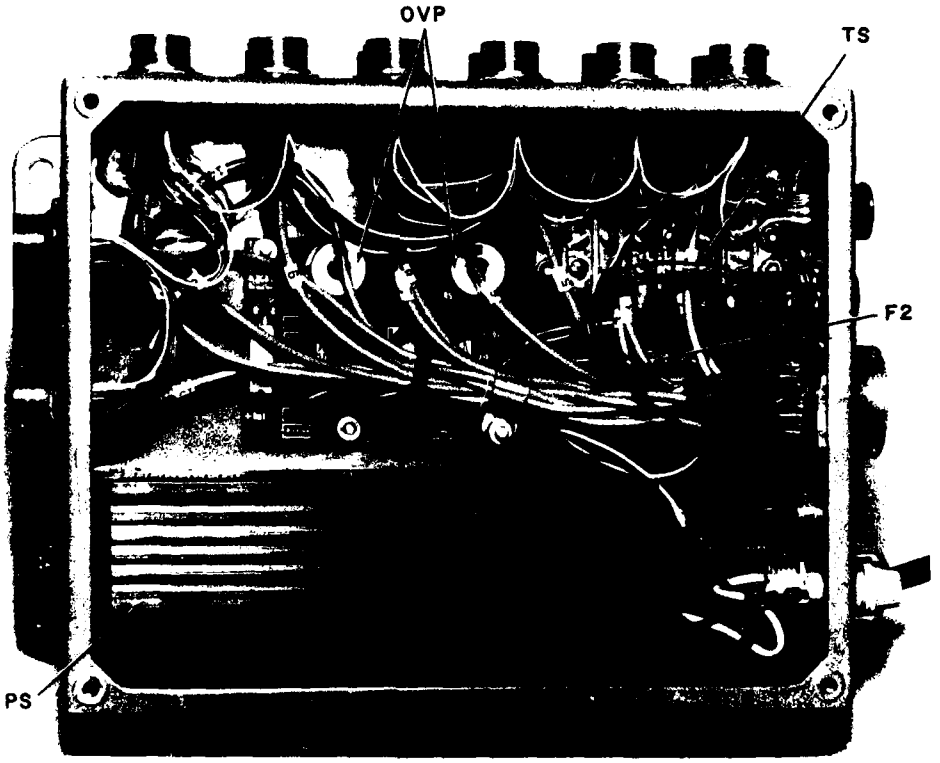
Mounted on the inside bottom of the box (see Figure 4) are a terminal strip (TS), the sensor power supply (PS), two overvoltage protection devices (OVP), and two fuses (F2) for the power supply output. (Note: Two weldnuts mounted on the inside bottom of the box near J1-J12 were ground off during box assembly to allow clearance for the connectors.)

Table 2 gives a parts list for the box.

3.4 Junction Box Wiring Diagrams

Figure 5 gives the power distribution wiring diagram for the junction box. The power supply is adjusted for a +12 Vdc output with the OVP trip point set to approximately 13 Vdc. (OVP trip point adjustment procedures are in Appendix A.) Specifications for the power supply and overvoltage protectors are given in Table 2.

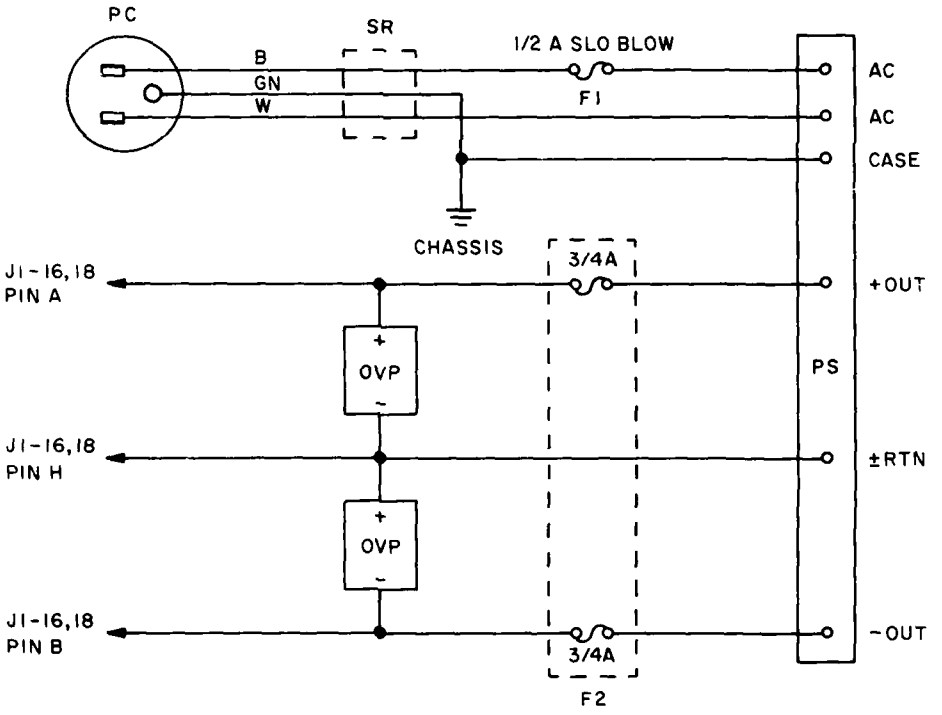
Junction box signal routing information is contained in Appendix A.



4. Junction Box Internal View

Table 2 Junction Box Parts List

Part	Noun	Mfgr Part No.	Manufacturer
	Box	A-1008SCEP	Hoffman Engineering Co.
J1-17	Connector	PT07A-12-10S	Bendix
J18	Connector	PT07-24-61S	Bendix
J19	Jack	12B	Switchcraft
CV	Dust cover	512	Switchcraft
Sr	Strain relief	2520	Thomas and Betts
PC	Power cord	17513	Belden
F1	Fuse holder	342006	Littlefuse
PS	Power supply	115	RO Associates
OVP	Overvolt protector	OVP-2	Standard Power, Inc
F2	Fuse holder	357002	Littlefuse
TS	Terminal strip	603-6	Kulka



5. Junction Box Power Distribution Schematic

Table 3 Junction Box Power System Specifications

Power Supply:	
Output Voltage:	± 12 to ± 15 Vdc, adjustable
Output Ripple:	2 mV P-P
Output Regulation:	± 1 mV (± 10 % Line)
	3 mV (no load to full load)
Output Current:	0.75 A
Size:	3.5 x 7.9 x 1.7 in.
	(8.9 x 20.1 x 4.3 cm)
Operating Temperature:	-20 to +75 deg C
Overvoltage Protector:	
Trip Range (Adjustable):	5.35 to 32 Vdc
Current Capacity:	16 A (continuous)
	240 A (instantaneous)
Size:	1.7 x 2.8 x 0.7 in.
	(4.3 x 7.1 x 1.8 cm)

4. SIGNAL CONDITIONING SUBSYSTEM

4.1 Chapter Overview

This chapter covers the signal conditioning subsystem. It begins with a functional description of the subsystem. Following this is a description of the physical components of the unit, including theory of operation and circuit diagrams. The final part of the section deals with software that has been developed to configure the subsystem and to determine its actual operational characteristics.

4.2 Signal Conditioner Functional Description

The signal conditioning subsystem amplifies and filters analog signals prior to their digitization and recording. The subsystem consists of a rack of 16 single-channel conditioners, each of which is on a separate printed circuit board. Each board can be configured to provide a variety of types of signal conditioning including lowpass, highpass, bandpass, and anti-aliasing filters. Three parallel isolated outputs are provided on each board. One is routed to each of the output connectors, while the third is routed to a special board slot as described below. Each board has an overrange indicator to provide a visual signal if the output voltage exceeds the linear input range of the digitizer. Also included on each board is dc voltage adjustment to correct for dc bias in the signals being processed. Several test points are included on the board to allow monitoring of the signals at various stages in the conditioning process.

Mounted on the back of the signal conditioning card rack are a power supply and the input/output connectors. The power supply

provides dc power for the active circuits on the boards. The 19-pair cable from the junction box is connected to the input connector, while cables to the analog strip chart recorder and the system controller are connected to the output connectors. A jack for the intercom headphones is also mounted on the rear of the card rack.

In addition to the 16 signal conditioning cards, two special purpose card slots have been included in the card rack. One is designed for calibration of both the signal conditioning cards and the sensor array. The other slot allows the combination of the outputs of the 16 conditioner cards for custom signal processing (such as the summation of several channels).

4.3 Signal Conditioner Physical Description

4.3.1 SIGNAL CONDITIONER CHASSIS

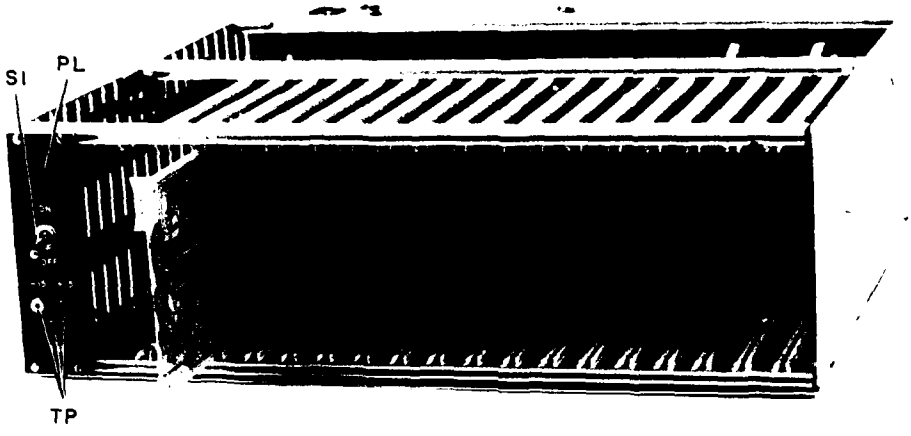
4.3.1.1 Chassis Hardware Description

Sixteen printed circuit boards mounted in a card rack make up the signal conditioning subsystem (Figures 6 and 7). The basic card rack is built from components made by the Vector Electronic Co. The card rack takes up 5.25 in. (13.3 cm) of space in a standard 19 in. (48.3 cm) equipment rack and measures 18.5 in. (47.0 cm) deep, power supply included. A 1/8 in. (0.3 cm) thick aluminum back panel has been added to the Vector rack. Top and bottom dust covers of 1/16 in. (0.2 cm) aluminum have also been added as has a front panel (the top cover has been removed in Figures 6 and 7 for clarity).

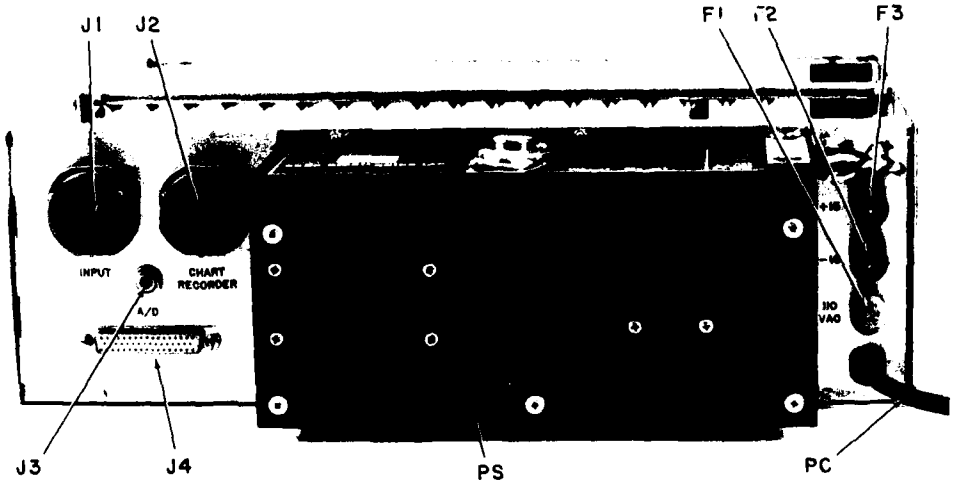
Mounted on the front panel are the conditioner power switch (S1) and pilot light (PL) as are three test points (TP) for monitoring the power supply output. The power supply (PS) itself is bolted to the back panel. Also on the back panel are the input connector (J1) for the cable from the junction box, an output connector (J2) for the cable to the analog chart recorder, and an output connector (J4) for the cable to the control subsystem. A phone jack (J3) on the back panel has been provided for connection of an intercom system to the junction box. A power cord (PC) provides 110 Vac 60 Hz power for the power supply, which is protected by a fuse (F1). The power supply outputs are also fused (F2 and F3). Table 4 gives a parts list for the signal conditioner subsystem.

4.3.1.2 Chassis Wiring Description

Figure 8 contains the power wiring schematic for the signal conditioner card rack. Eighteen-gage wire is used for the +12 Vdc and power common lines to reduce voltage drop problems. These lines are connected to bus wires on the card sockets that distribute the power to all cards. The supply wires are conected to the busses near the center of the card cage to equalize bus voltage drops as much as possible. Also connected to the bus at the same location are two 250 μF 50 V electrolytic capacitors (C1 and C2) and the lines from the remote voltage sense terminals on the power supply.



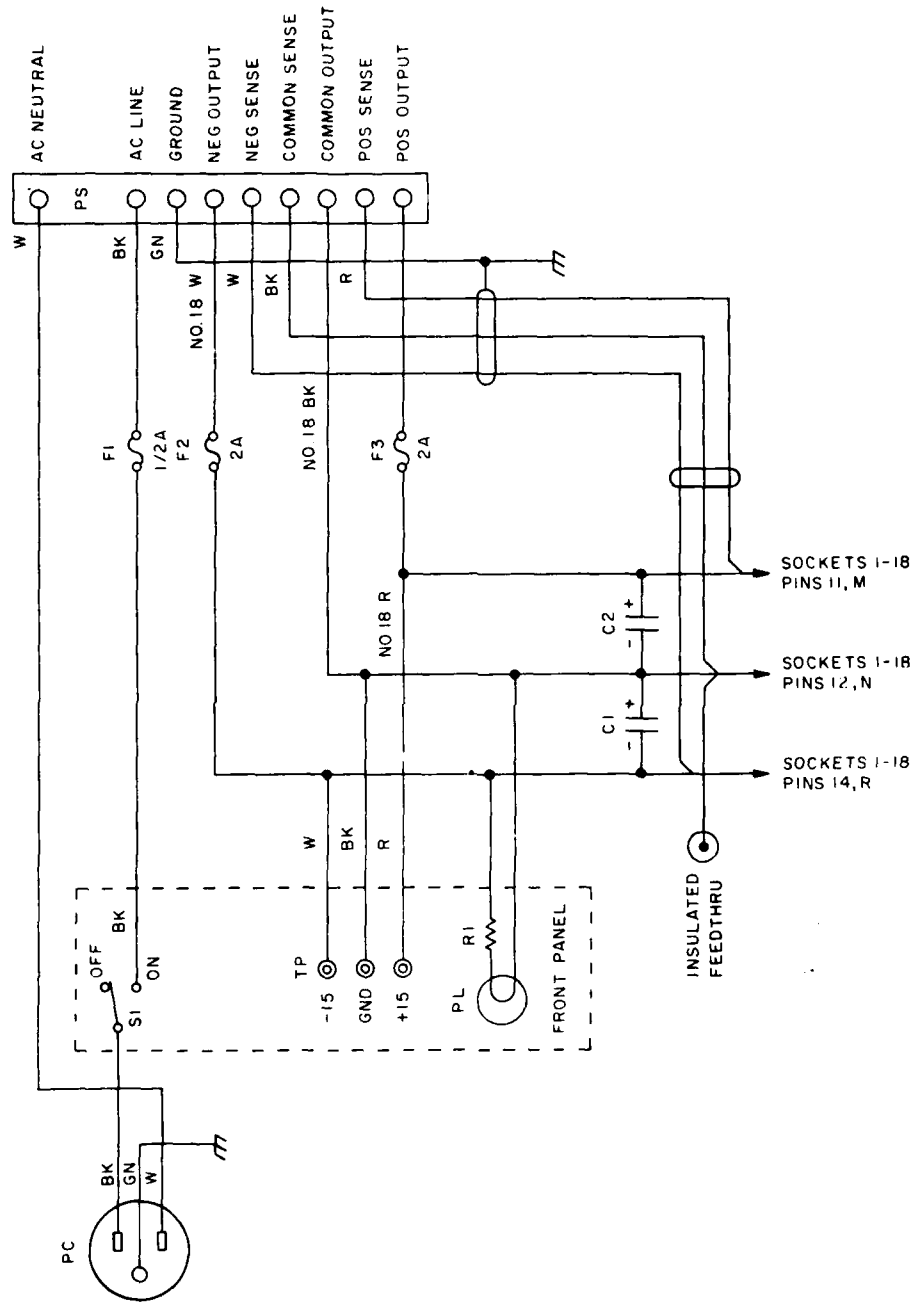
6. Signal Conditioner Chassis Front View



7. Signal Conditioner Chassis Rear View

Table 4 Signal Conditioner Chassis Parts List

Part	Noun	Mfgr Part No.	Manufacturer
S1	Power switch	7580K7	Cutler-Hammer
PL	Lamp holder	MCM-175T	Alco
	Pilot lamp	330	Chicago Miniature Lamp
TP	Test point	1506-101/102/103	H. H. Smith
PS	Power supply	OEM15D2.4-1-2	ACDC Electronics
J1	Connector	PT07-24-61S	Bendix
J2	Connector	PT07-24-61P	Bendix
J3	Jack	C-12B	Switchcraft
J4	Connector	DD50S	Cannon
PC	Power cord	17513	Belden
F1-F3	Fuse holder	342014	Littlefuse
	Card rack, consisting of the following parts:		
	Side walls (2)	SW-52-P-156	Vector Electronics Co.
	T-struts (8)	TS-169-P	Vector Electronics Co.
	T-strut mounting brackets (8 reqd - come in pkg of 6)	BR16-A	Vector Electronics Co.
	Card guides (3 pkg of 12)	BR20-10-HP	Vector Electronics Co.
	Nuts, T-strut (2 pkg of 24)	NT4-7PA	Vector Electronics Co.
	Hex-head T-strut screws (1 pkg)	SC4-26	Vector Electronics Co.
	Hex-head T-strut screws (1 pkg of 24)	SC24-28	Vector Electronics Co.
	T-strut screw inserts (2 pkg of 24)	NT6-3	Vector Electronics Co.
	Edgecard receptacle (18)	R644	Vector Electronics Co.



8. Signal Conditioner Distribution Chassis Power Schematic

The power supply common is not tied to the chassis ground. Rather, it is connected to an isolated stud on the back panel of the rack. This stud, in turn, can be tied to a separate ground point to isolate the signal ground from digital or 60 Hz ground noise (stud not shown in Figure 7).

A voltage dropping resistor (R1 - 15Ω , 1/2 W) has been added to the pilot lamp circuit. It provides a drop of about 1 V so the 14 V pilot lamp can be connected to the 15 V power supply lines.

Specifications for the signal conditioner power supply are given in Table 5.

Figure 9 gives a simplified signal wiring diagram for the signal conditioner subsystem (detailed pin assignments and signal routing information is in Appendix B). The signal conditioner card rack has slots for 18 cards. Slots 1 through 16 are used for signal conditioning cards. Input signals for these slots come from the input connector on the back panel; output signals go to the two back panel output connectors and to slot 17.

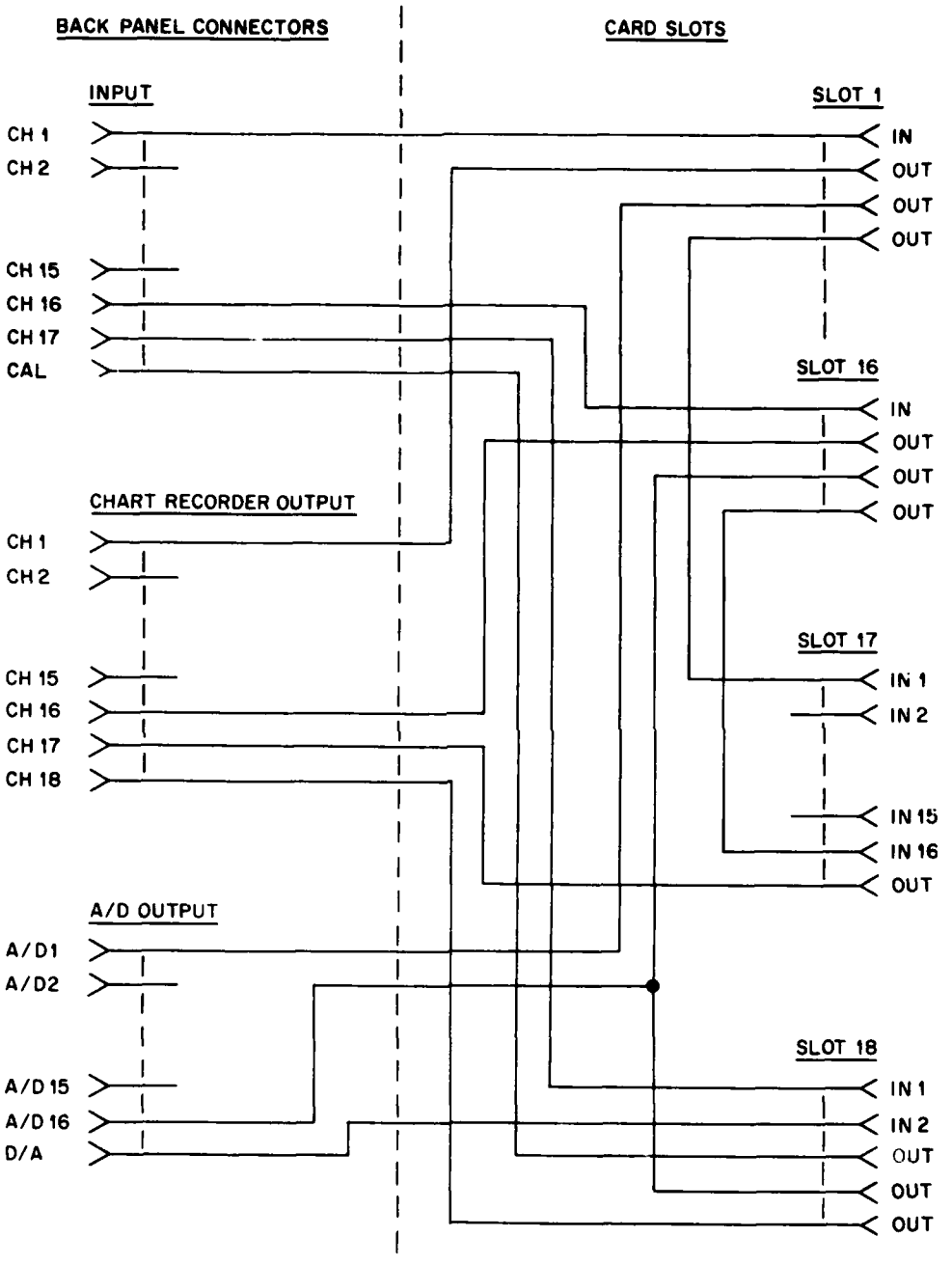
Card rack slot 17 is set up for an analog signal combination circuit card for combining the outputs from the 16 conditioning cards. The output from this slot is connected to channel 17 chart recorder output.

Card rack slot 18 is designed for three purposes - conditioning card checkout, calibration, and spare channel signal conditioning.

The output of the digital-to-analog (D/A) converter in the system controller is routed through the A/D output connector to the slot 18 input pins. Further, the slot 18 output pins are connected in parallel to the slot 16 output pins. Thus, a conditioning card to be checked out can be plugged into slot 18, the slot 16 card removed, and a signal generated using the system controller D/A converter. The output of the card can be measured using the channel 16 A/D input to verify correct card performance.

Table 5 Signal Conditioner Power Supply Specifications

Output Voltage:	± 15 Vdc (± 0.5 V adj range)
Output Ripple:	20 mV P-P, max
Output Regulation:	± 20 mV (± 10% line)
	± 20 mV (no load to full load)
Output Stability:	10 mV / 8 hr, typ (after warmup)
	(Pos to neg relative 5 mV)
Output Tempco:	0.02% / deg C, max
Output Current:	2.4 A, max
Overvoltage Protection:	Built-in
Size:	10.0 x 3.2 x 4.9 in.
	(254.0 x 81.0 x 125.5 cm)
Operating Temperature:	0 to +71 deg C



9. . gnal Conditioner Chassis Simplified Signal Distribution Schematic

For sensor calibration, circuitry can be inserted into slot 18 to generate a calibrating signal which is routed to the calibration signal pair going to the junction box. Alternatively, the D/A converter in the system controller can be used to generate a calibration signal. This signal could be buffered on a card inserted into slot 18 and sent to the sensors via the junction box.

The spare channel signal pair (channel 17) from the junction box is also routed to a different pair of input pins in slot 18. A custom conditioning card inserted in slot 18 could be used to condition this signal for recording by on A/D channel 16 (note that slot 16 must be vacant if this is done to prevent signal conflict).

Outputs for any of the three envisioned uses for slot 18 can be displayed on channel 18 of the chart recorder, as shown in Figure 9.

4.3.2 SIGNAL CONDITIONER CIRCUIT BOARD DESCRIPTION

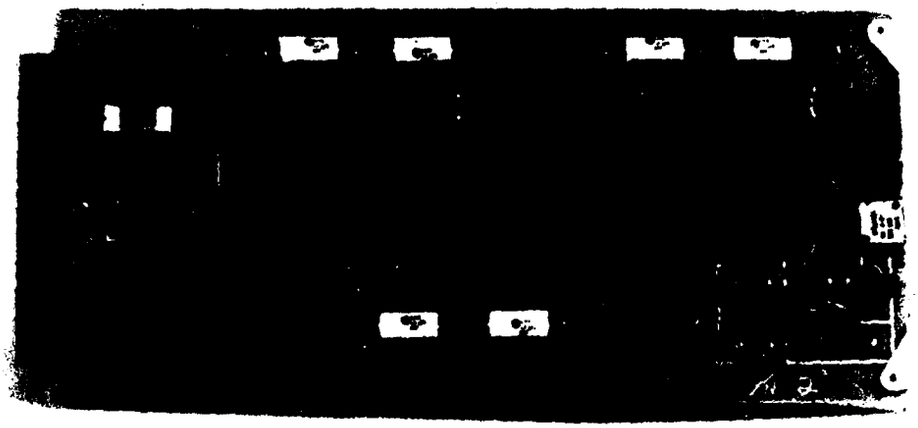
4.3.2.1 Circuit Board Physical Description

Each signal conditioning card consists of a 4.5 x 10 in. (11.4 x 25.4 cm) fiberglass printed circuit board as shown in Figure 10. Permanently mounted on the board are the amplifiers and certain components used to form the filter and gain sections. The exact configuration of the filters is determined by carrier-mounted components (see Figure 11) that plug into the four vacant integrated circuit sockets visible on the card. (The following sections discuss the functions of these components and give information on two computer programs for selecting and checking their values.) A set of test points has been included for monitoring the signal at various points in the filter chain. Mounted near the test points are a trimpot for adjusting circuit dc offset and a light emitting diode (LED) for indicating overrange signals. Appendix C contains the detailed circuit board schematics and parts lists.

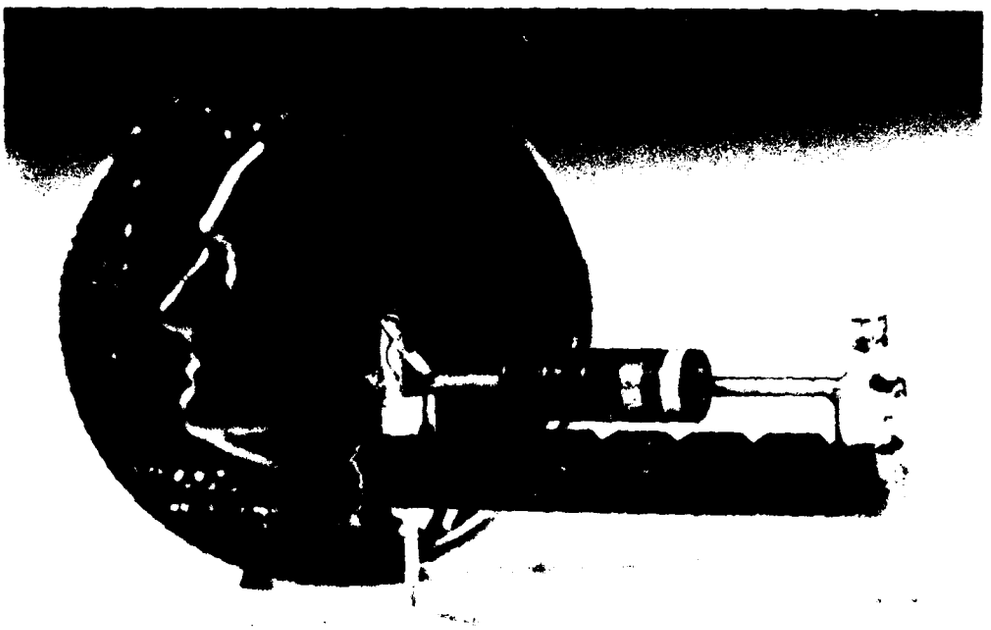
4.3.2.2 Signal Conditioner Circuit Description

Figure 12 gives a block diagram of the signal conditioning circuit board. Each card consists of five conditioning stages, output buffers, and an overrange indicator. Detailed circuit diagrams and circuit descriptions are contained in Appendix C.

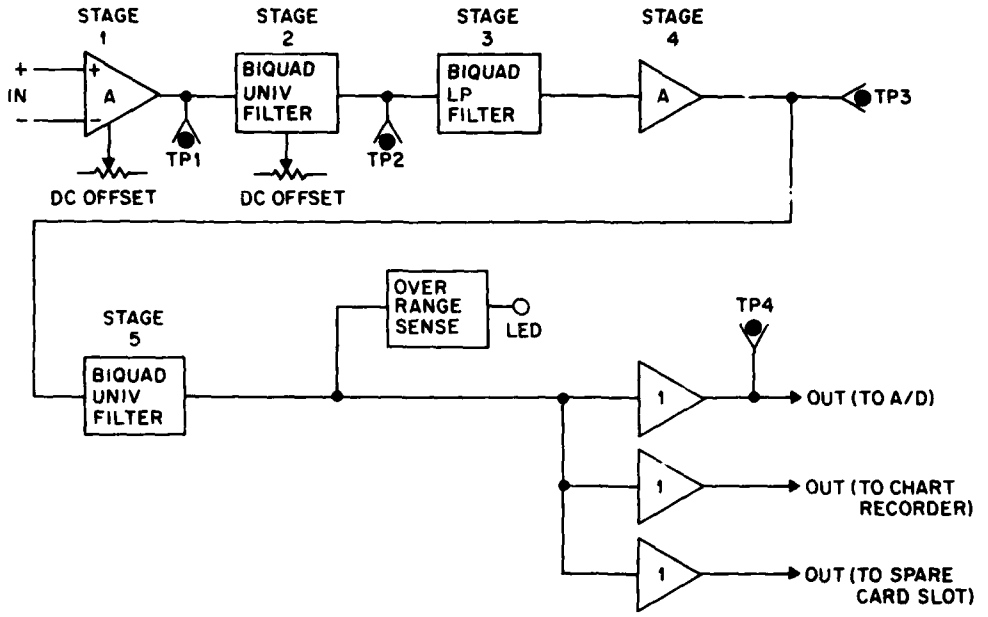
Stage 1 consists of a variable gain instrumentation amplifier. The amplifier features a differential input with high common mode signal rejection to minimize the effects of noise picked up by the cable from the junction box. It functions as an input buffer, isolating the following stages from interaction with the input signals. It also provides signal gain as set by two resistors, R101 and R102, located near the amplifier on the circuit card. A dc offset adjusting trimpot is located near the amplifier for nulling out any input offset voltages. The high frequency response of the amplifier is limited by a resistor/capacitor network. The network inserts a pole at approximately 677 Hz.



10. Signal Conditioner Circuit Board



11. Signal Conditioner Circuit Board
Component Carrier



12. Signal Conditioner Circuit Block Diagram

Stages 2, 3, and 5 are similar. Each consists of amplifiers and certain fixed components needed to form biquadratic (biquad) universal active filters. Each filter stage can provide a second order lowpass, bandpass, highpass, allpass, or band reject filter. In addition, each stage can provide amplification of the signal. (Appendix D presents a detailed discussion of the theory and design equations for the biquad active filter.) Stages 2 and 3 differ slightly from stage 5. Stage 2 has an additional dc offset voltage adjustment via a trimpot located on the outside edge of the card. This adjustment allows the user to correct for dc drift or offset of signals amplified by the card. Stage 3 is set up as a lowpass filter only. It can handle lower frequencies than the other two stages through the addition of extra capacitors (using solder pads included for that purpose). All parameters for these filters (filter type, gain, frequency response, damping coefficient) are set by carrier-mounted resistors plugged into the board. Section 4.4 of this report covers software developed to assist in the selection of these resistors.

Stage 4 is an amplification stage. Its gain is set by two plug-in resistors. Also, by the addition of a capacitor in parallel with one of the resistors, the stage can provide a single lowpass pole.

Three independently buffered outputs are provided on the board. They appear on the board's edge connector and are single ended. They supply signals to the A/D converter (in the controller chassis), to the chart recorder, and to a spare card slot in the card rack.

A visual overrange indication has been built into each board. The indicator uses a buffered comparator to monitor the boards output and turn on the LED when the output exceeds approximately +10 or -10 Vdc. This level corresponds to the maximum input signal level of the A/D converter. Thus, the user is given a visual indication of possible A/D signal clipping.

Four test points have been incorporated into the board. These appear, together with system ground, on a multiple test point module on the edge of the board. They give the outputs of stages 1, 2, 4, and 5, with the stage 5 output paralleling the signal recorded by the A/D. At these points, a technician can measure dc offset and observe the signal waveform using a voltmeter or an oscilloscope.

CAUTION:

The stage 1 test point should be monitored using a 10X oscilloscope probe only. Lower impedance probes cause the stage 1 amplifier to oscillate.

Table 6 summarizes the features of each conditioning stage; Table 7 gives specifications for the signal conditioning board.

Table 6 Signal Conditioner Card
Feature Summary

Stage	Features
1	Variable gain, differential input, instrumentation amplifier Dc - 677 Hz frequency response Input offset null adjustment Output fed to card edge test point
2	General purpose (Gain, LP, HP, BP, BR, AP) biquad filter Dc offset adjustment (via pot. at card edge) Output fed to card edge test point
3	Lowpass biquad filter Lower gain capability than stages 2 and 5 Additional filter capacitors easily added
4	Amplification only Can add capacitor for one lowpass pole Output fed to card edge test point
5	General purpose (Gain, LP, HP, BP, BR, AP) biquad filter
Output	Three individually buffered outputs (one fed to card edge test point) LED overrange indicator

Table 7 Signal Conditioner Card Specifications

Input Impedance:	3000 MOhms / 1.8 pF
Input CMRR:	100 dB, min
Input Noise:	12.5 uV (P-P) (dc-200 Hz) *
Max Input Voltage (Above GND) For Rated Performance:	± 10 Vdc
Max Input Voltage Without Damage:	30 Vdc (differential) ± 30 Vdc (each input to ground)
Output Saturation Level:	± 15 Vdc
Harmonic Distortion:	< 0.5% (12 Hz input)
Output Impedance:	75 Ohm

* Rises to 1.0 mV (P-P) during printer/plotter operation.

4.4 Signal Conditioner Software Description

4.4.1 SOFTWARE OVERVIEW

Two computer programs have been developed for the design and analysis of a circuit conditioning card. The design program (FILTER) accepts desired filter parameters from the user and calculates the components required to build the filters. The program prints out a complete table of component values and filter parameters for the card.

The analysis program (FCHECK) is a derivative of FILTER. FCHECK is designed to accept component values and calculate the stage by stage filter parameters. It is intended for use after a signal conditioning card is built up to determine the filter's parameters from the values of the actual components used. A table of component values and filter parameters can be printed out as a record of the filter configuration for use in documenting data acquisition configurations and determining system responses.

Both programs include a provision for storing the filter parameters in disk files for use by other programs.

To aid the user in the operation of the programs, two sample circuit card configurations have been selected as typical of those used. Appendix E contains design sheets, annotated system console listings, and component table printouts documenting the design and analysis of these sample configurations.

The following sections give more detailed information on these two programs.

4.4.2 DESIGN SOFTWARE

This section describes a computer program developed to aid in building up a signal conditioning card. The program, called FILTER, was written in FORTRAN and runs on the system computer (see Chapter 5). It can be used to design any or all stages of the signal

conditioning card. Prior to running FILTER, the exact conditioning card configuration (gain distribution, filter types, filter frequencies, filter damping coefficients) must be selected. Figure 13 gives a conditioner card design worksheet to aid in configuration design documentation. The program accepts this configuration information and calculates the resistor/capacitor values needed to build the filters.

The program also can use user-entered component values to calculate filter parameters. Thus, the user can substitute available component values for those calculated by the program and check the effect on the filter parameters of these values. The process of entering component values can be repeated until a satisfactory set of filter parameters is achieved for that stage. Once satisfactory component values are arrived at for all stages on the board, the user can redesign a stage to correct errors or change filter types. Finally, a table of component and filter parameter values can be printed on the line printer to aid in building up the conditioning cards.

Complete annotated listings of the program are contained in Appendix F for those desiring further insight into its workings.

4.4.3 ANALYSIS SOFTWARE

This section describes a computer program used to document the stage-by-stage filter parameters of a signal conditioning card. The program, called FCHECK, was written in FORTRAN and runs on the system computer (see Chapter 5). The program accepts component values and calculates the filter parameters for all stages (or any one stage) on the conditioning card. In case of error, the values can be reentered and the calculations repeated. Once all parameters have been calculated, the program allows the user to repeat the process of entering component values for any given stage to correct errors or change filter type for that stage. Finally, a table of component values and filter parameters can be printed on the line printer for archival purposes.

Complete annotated listings of the program are contained in Appendix G of this report for those desiring further insight into its workings.

DATE: _____ CHANNEL NO: _____

TOTAL RESPONSE DESIRED:

STAGE 1: GAIN ONLY

STAGE GAIN: _____(V/V)
POLE FREQUENCY: _____(HZ)

STAGE 2: FILTER TYPE: GAIN LP BP HP BR

ADDED CAPACITOR VALUE: _____(UFD)
STAGE GAIN: _____(V/V)
ZERO FREQUENCY: _____(HZ) ZERO DAMPING COEFF: _____
POLE FREQUENCY: _____(HZ) POLE DAMPING COEFF: _____

STAGE 3: LOW PASS FILTER ONLY

ADDED CAPACITOR VALUE: _____(UFD)
STAGE GAIN: _____(V/V)
POLE FREQUENCY: _____(HZ) POLE DAMPING COEFF: _____

STAGE 4: FILTER TYPE: GAIN GAIN AND LP

STAGE GAIN: _____(V/V)
POLE FREQUENCY: _____(HZ)

STAGE 5: FILTER TYPE: GAIN LP BP HP BR

ADDED CAPACITOR VALUE: _____(UFD)
STAGE GAIN: _____(V/V)
ZERO FREQUENCY: _____(HZ) ZERO DAMPING COEFF: _____
POLE FREQUENCY: _____(HZ) POLE DAMPING COEFF: _____

13. Signal Conditioner Circuit Board
Design Worksheet

5. SYSTEM CONTROLLER SUBSYSTEM

5.1 Chapter Overview

This chapter addresses the system controller. Included is an overview of the subsystem functions and detailed descriptions of its components. Separate subsections will cover the controller chassis and wiring, the system control computer, and the analog to digital (A/D) converter. Digital Equipment Co.[2] (1979) offers detailed information on the system computer as well as an overview of the system software.

5.2 System Controller Functional Description

The system contoller is the heart of the SDAS. It contains the digital computer that controls the recording of data and analyzes prerecorded data. The computer also runs programs to design the signal conditioning cards, as documented in Chapter 4 of this report. Further, the power supplies in the unit provide dc power to the interface subsystem.

5.3 System Controller Chassis Description

5.3.1 CHASSIS PHYSICAL DESCRIPTION

A custom-built aluminum chassis houses the system controller. Figures 14 through 16 give external views of the chassis. (Component labels are referred to below.)

The chassis is designed to fit into a standard 19 in. (48.26 cm) equipment rack. Its front panel, on which is glued an engraved blue plastic dress plate, is made from Ø.125 in. (Ø.32 cm) aluminum. The panel measures 1Ø.48 x 19 in. (26.6 x 48.3 cm) and includes two slots on each side for screws to fasten the chassis to the equipment rack. A 8.5 x 11.5 in. (21.6 x 29.2 cm) door is cut into the front panel to allow access to the computer cards as shown in Figure 14. Figure 15 shows the front view with the door opened, illustrating the locations of the cards. The white ribbon cables visible in this figure connect the inputs and outputs of the computer cards to J3 through J17 on the chassis rear panel.

The chassis box itself is made from aluminum and measures 19 in. (48.3 cm) deep, 1Ø in. (25.4 cm) high, and 17 in. (43.2 cm) wide. It has a removable top panel to allow access to the internal components. A Ø.125 in. (Ø.3 cm) rear panel contains engraved labels

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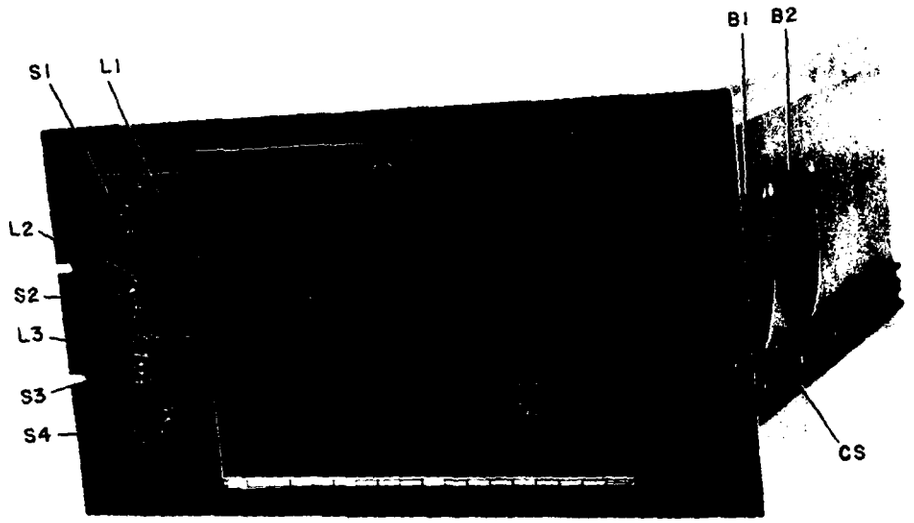
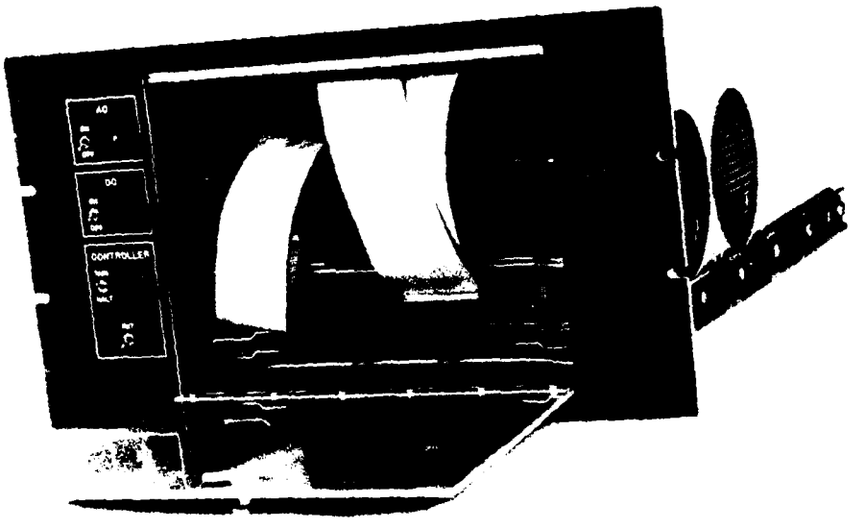
2. Microcomputer Processor Handbook, (1979) Digital Equipment Co., Maynard, MA



14. System Controller Chassis Front View



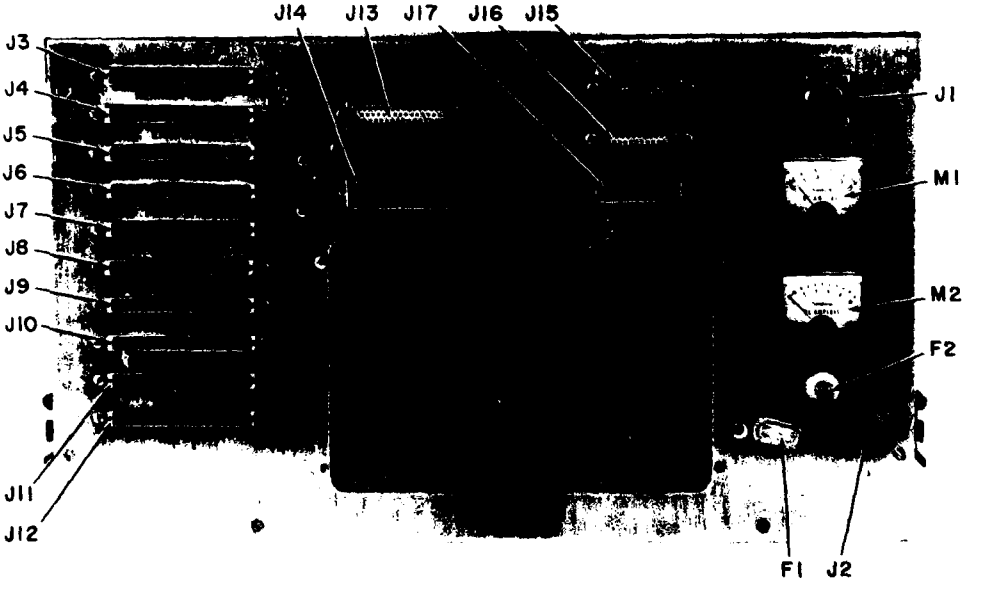
15. System Controller Chassis Front View
(Front Panel Open)

for the components mounted on it. In the middle of the panel is a grill for exhausting ventilation air.

Mounted on the front panel are several switches and pilot lights. Switch S1 controls the ac power to the controller. The nearby indicator light (L1) gives a visual indication when the ac power is on. A second switch (S2) controls the dc power supplies' outputs; pilot light L2 lights up when the dc power is on. The other two switches control the status of the system computer. The *RUN/HALT* switch (S3) enables or disables the computer RUN mode. When the computer is running, pilot lamp L3 is on. Momentary contact switch S4 initializes (restarts) the computer.

The chassis is mounted in an equipment rack using two chassis slides (CS), one on each side of the box. Two ventilation fans (B1 and B2) are mounted on the side of the chassis to provide ventilation air; they are active whenever ac power in the chassis is on.

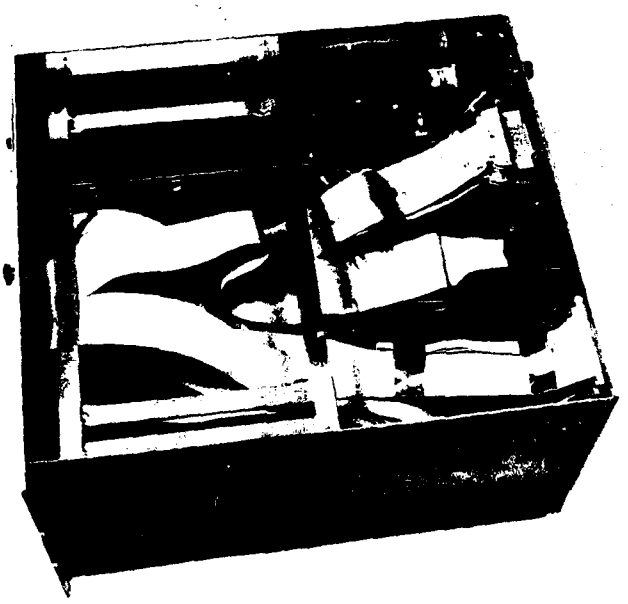
On the rear panel (see Figure 16) are mounted the input, output, and power connectors as well as fuses and dc ammeters. J3 through J6 provide the parallel digital connections between the interface subsystem and the parallel input/output cards mounted in the computer card rack. Connectors J7 through J11 are spare input/output connectors; they are connected to ribbon cables that run to the front of the computer card rack but which are not currently connected to any input/output cards. J12 is used for connecting the floppy disk subsystem to the floppy disk controller card in the computer card rack. J13 is used for routing analog signals between the signal



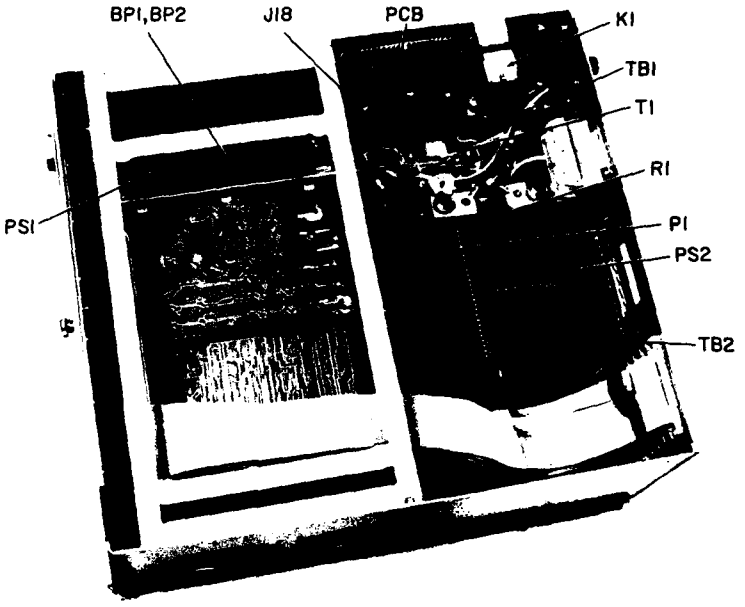
16. System Controller Chassis Rear View

conditioning subsystem and the A/D converter module in the computer card rack. (J14 is a spare analog signal connector slot for future expansion.) Serial digital communications are provided through J15 and J16. These are used for communications between the computer and the system console and printer. A spare serial connector (J17) is provided for future system expansion; it is currently not connected to any computer card. Five Vdc power is supplied to the interface subsystem through J1, while 110 Vac is supplied to the controller through J2. A power cord (PC), not shown, connects J2 to ac power. Two fuses (F1 and F2) provide protection for the entire controller and for the power control card, respectively. Finally, two dc ammeters (M1 and M2) monitor the current supplied by the controller 5 V and 12 V power supplies.

The inside of the system controller chassis is rather closely packed as illustrated by Figures 17 and 18. Figure 17 shows an inside view of the chassis with the ribbon cables linking J3-J17 to the computer cards in place to illustrate their routing. Figure 18 gives the same view with the cables removed or relocated in order to illustrate component location.



17. System Controller Chassis Interior View



18. System Controller Chassis Interior View (Ribbon Cables Removed)

Card racks (BP1 and BP2) for the system control computer dominate the interior of the chassis. Two power supplies, PS1 and PS2, provide 12 and 5 Vdc power, respectively, for the system computer and interface circuitry. Mounted on top of PS2 is a ammeter shunt (R1) for the 5 V ammeter. On the bottom of the chassis is mounted a power transformer (T1) which supplies low voltage ac to the power control board (PCB). This board is connected to the chassis wiring harness through edge connector J18. A ribbon cable runs from this connector to a plug (P1), which is plugged into the lower computer card cage (BP2) to provide power status signals to the computer. On the side panel of the chassis near the control board are mounted the 110 Vac control relay (K1) and an ac distribution terminal strip (TB1). Finally, a terminal strip (TB2) is mounted on the rear panel near J6 for connecting two signals from this connector to J18.

Table 8 gives the parts list for the subsystem.

Table 8 System Controller Chassis Parts List

Part	Noun	Mfgr Part No.	Manufacturer
S1	Switch, SPST	7580K7	Cutler-Hammer
L1	Lamp holder	508-7538-504	Dialco
	Neon lamp cartridge	507-4537-56K	Dialco
S2,S3	Switch, SPDT	MTA-106D	Alcoswitch
L2,L3	Lamp holder	MCM-175T	Alco
	Pilot lamp	328	Chicago Miniature Lamp
S4	Switch, SPDT	MTA-106F	Alcoswitch
CS	Chassis slide (Pr)	C-300-S-20	Zero Corp.
B1,B2	Fan	WR2H1	Rotron
J1	Connector	PT07A-12-3S	Bendix
J2	Connector	PT07A-12-3P	Bendix
J3-J12	Connector	3331-0000	3M
J13,J14	Connector	DD-50S	Cannon
J15-J17	Connector	DB-25S	Cannon
J18	Socket, PC	R644	Vector
F1	Fuse holder	344-125A	Littlefuse
F2	Fuse holder	342-858A	Littlefuse
M1	Ammeter, 25 A	02437	Simpson
M2	Ammeter, 10 A	02435	Simpson
BP1,BP2	Card rack	H9270	Digital Equipment Co.
PS1	Power supply, 12 V	LJS-10-12-OV	Lambda
PS2	Power supply, 5 V	LJS-12-5-OV	Lambda
R1	Ammeter shunt	6707	Simpson
T1	Transformer, 12.6 V	P-8358	Stancor
P1	Plug	3473-3	3M
K1	Relay	W388ACQX-9	Magnecraft
TB1	Terminal strip	603-4	Kulka
TB2	Terminal strip	LTS-202	SPC Technology
C1-C4	Capacitor, 2.5 μF, 25 Vdc, tantalum	196D225X9025HA1	Sprague
D1	Diode, 1 A, 50 V	1N4001	Motorola
PC	Power cord (with Bendix PT06SE-12-3S connector)	17513	Belden

5.3.2 CHASSIS WIRING DESCRIPTION

Figure 19 gives the power and control signal wiring diagram for the system controller chassis. Wire sizes are annotated on the figure where they are important (to reduce voltage drop). All 110 Vac power lines are twisted as shown and are routed well away from all dc and signal lines.

Pin 18 on J18 is not connected to anything on the power control board. Rather, it serves as a junction point between the ribbon cable connected to P1 and the twisted pair connected to TB2.

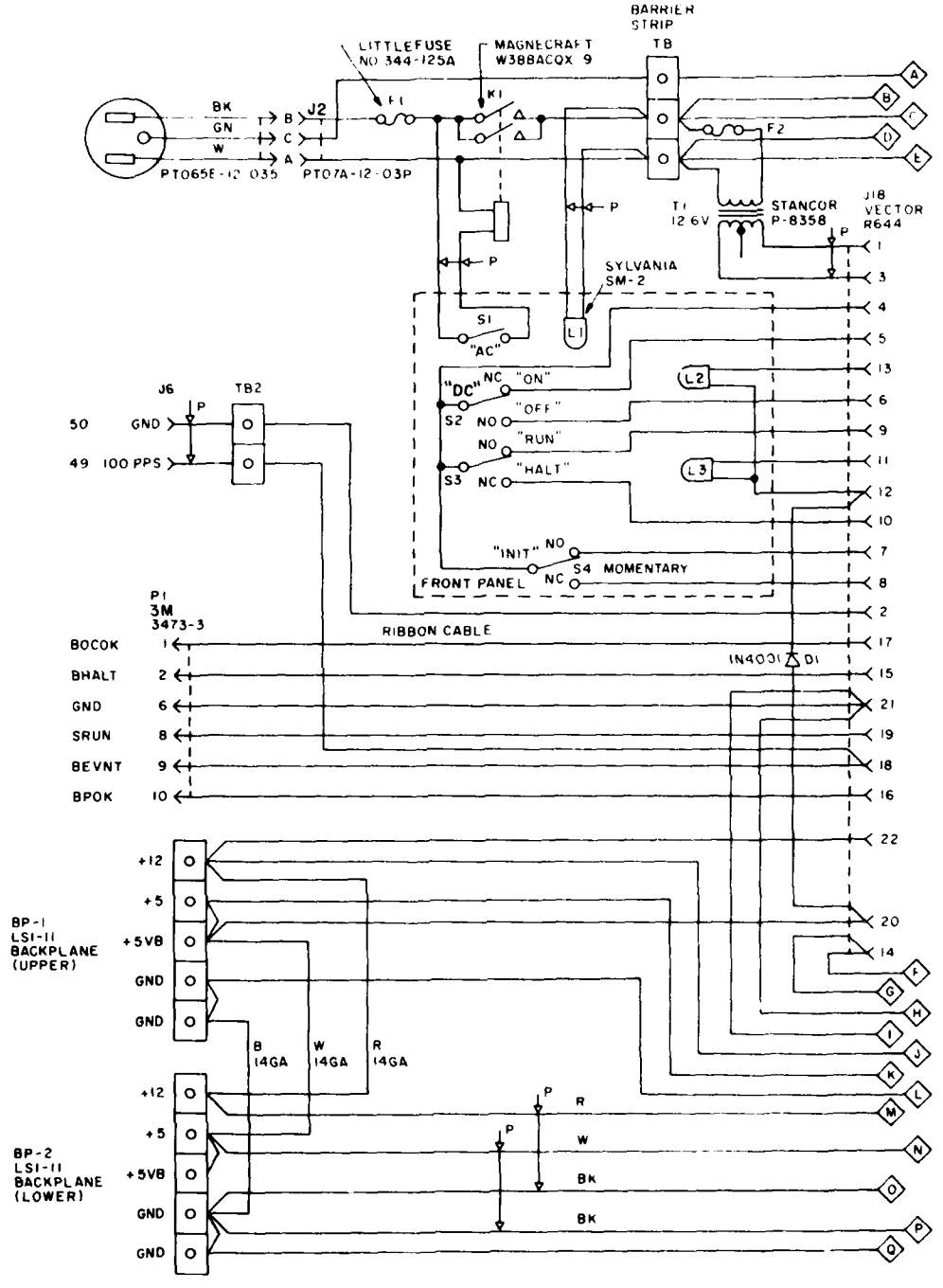
Specifications for the controller power supplies are given in Table 9.

Appendix H contains the signal wiring lists for the system controller subsystem. Also included in the appendix are the connection instructions for serial interfaces, such as terminals and printers. Appendix I contains a jumper list for interconnecting the two computer backplanes.

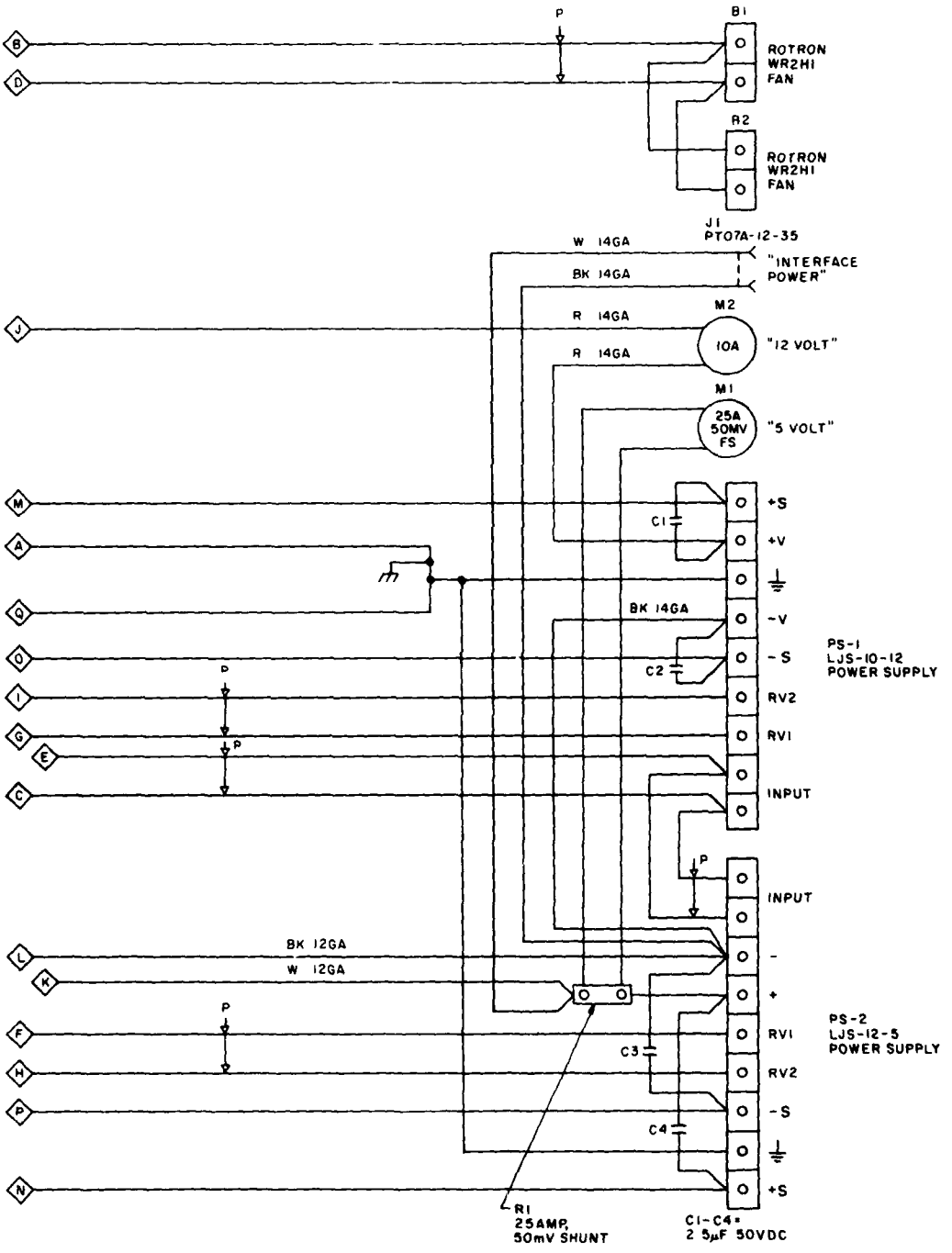
5.3.3 POWER CONTROL CIRCUIT DESCRIPTION

The power control circuit board is mounted inside the system controller chassis. It provides power control and status information to the controller power supplies and the controller computer. A block diagram of the board is given in Figure 20.

As shown on the block diagram, the board has its own ac input power supply for running the onboard logic and power supplies. The ac input is also fed into an ac sensing circuit as are the leads from the dc ON/OFF front panel switch. This circuit detects the presence of ac power and the status of the dc ON/OFF switch. It provides the control signals for controlling dc power supplies. A dc sense circuit senses the presence of both power supplies' outputs. When both dc voltages are at operating level, the circuit turns on the dc on pilot lamp. It also informs a delay circuit of the power status. This circuit provides the properly-timed power status signals to the system computer for both power up and power down conditions. Also on the board are a buffer for the RUN/HALT front panel switch and a retriggerable oneshot multivibrator. This latter circuit senses the SRUN pulse train from the computer (which indicates that the computer is the RUN rather than HALT mode), and turns on the RUN front panel lamp. Detailed circuit descriptions and board parts lists are contained in Appendix J of this report.



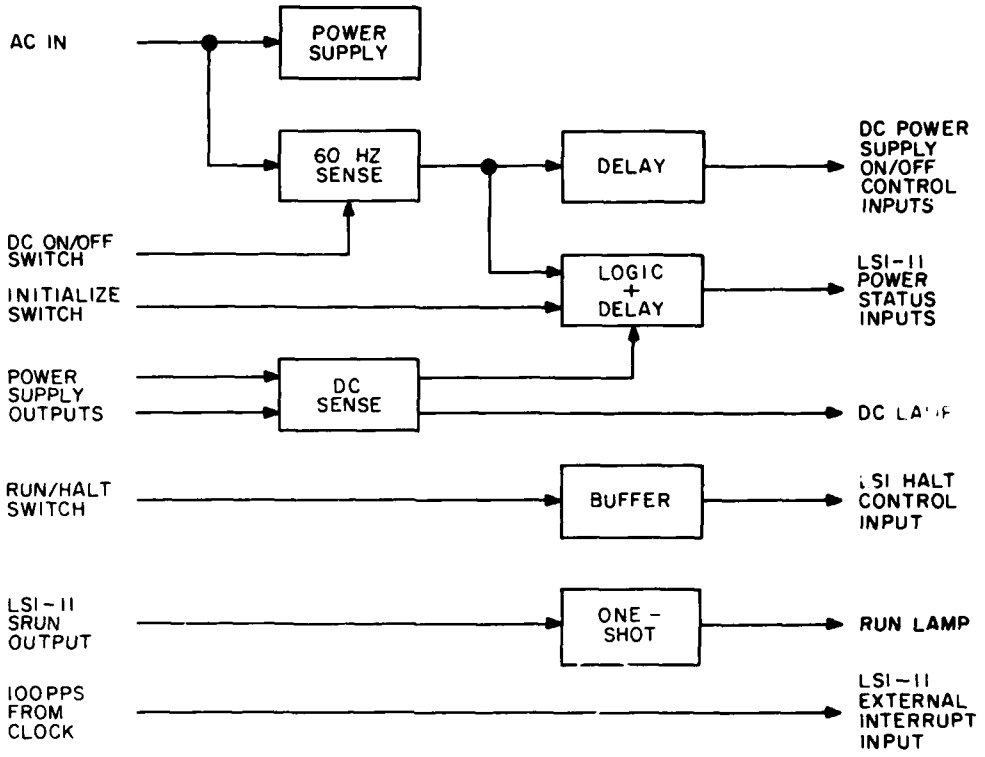
19. System Controller Chassis Power Distribution Schematic



19. System Controller Chassis Power Distribution Schematic (Cont.)

Table 9 System Controller Power Supply Specifications

5 Volt Supply:	
Output Voltage:	5 Vdc (± 0.25 V adj range)
Output Ripple:	50 mV P-P, max
Output Regulation:	± 20 mV (± 10% line, no load to full load)
Output Tempco:	0.03% / deg C, max
Output Current:	30 A at 50 deg C, ambient 24 A at 60 deg C, ambient 16.5 A at 71 deg C, ambient
Overvoltage Protection:	Built-in, 6.4-6.8 Vdc trip
Current Limiting:	Built-in
Size:	6.2 x 4.7 x 10.2 in. (15.8 x 12.0 x 26.0 cm)
Operating Temperature:	0 to +71 deg C
12 Volt Supply.	
Output Voltage:	12 Vdc (± 0.60 V adj range)
Output Ripple:	100 mV P-P, max
Output Regulation:	± 48 mV (± 10% line, no load to full load)
Output Tempco:	0.03% / deg C, max
Output Current:	4.2 A at 50 deg C, ambient 3.4 A at 60 deg C, ambient 2.3 A at 71 deg C, ambient
Overvoltage Protection:	Built-in, 13.3-14.1 Vdc trip
Current Limiting:	Built-in
Size:	2.1 x 4.7 x 10.2 in. (5.2 x 12.0 x 26.0 cm)
Operating Temperature:	0 to +71 deg C



20. System Controller Power Control Board Block Diagram

5.4 System Controller Computer Description

5.4.1 GENERAL DESCRIPTION

Acting as the controller for all digital data acquisition and analysis functions, the system computer can be considered the heart of SDAS. It consists of a DEC LSI-11 microcomputer, a number of interface cards, and program storage memory. The computer is housed in a card rack in the controller chassis and can be accessed through the front panel door of the chassis. The rack itself consists of card guides and a backplane/socket array into which the computer cards are plugged. The computer communicates with the outside world through interface cards . These are connected to the chassis back panel by multiple-conductor ribbon cables as discussed in the previous section. These cables and the computer cards are visible in Figure 15.

The following sections give an overview of the system computer components. More detailed information on the components can be found in the publication by Digital Equipment Co. [3](1980). Appendix I to this report contains a description (including jumper installations on the modules and a system memory map) of a minimum SDAS computer configuration.

5.4.2 CARD CAGE AND BACKPLANE DESCRIPTION

All LSI-11 system circuit boards are housed in two DEC H9270 backplane/card cage assemblies. These are mounted in a custom-built aluminum rack in the controller chassis. Room has been left in the rack for a third backplane assembly should future expansion require it.

The two backplane assemblies are jumpered together using wire wrap techniques. (Appendix I gives the pins jumpered.)

DEC's LSI-11 computer and support circuitry are mounted on printed circuit boards of two sizes: dual- and quad-height modules (the quad-height boards are twice the size of the dual-height boards). These backplanes provide enough room for the LSI-11 processor and up to 7 quad-height or 14 dual-height modules. The backplane provides all signal and power interconnections between the modules.

5.4.3 COMPUTER MODULE DESCRIPTION

A DEC LSI-11 microcomputer is used as the computer module in the SDAS. It is a single-board microcomputer version of DEC's PDP-11 minicomputer. It has the same internal architecture and instruction set as the PDP-11. Like the PDP-11, it is a 16-bit word length computer with multiple general-purpose internal registers. The LSI-11 modules used in the SDAS include the KEV-11 option, which provides additional fixed point as well as floating point arithmetic instructions.

The LSI-11 is housed on a quad-height circuit card bearing DEC module number M7264. Also on the card are 4K words of random access memory (RAM).

5.4.4 MEMORY MODULE DESCRIPTION

Additional memory beyond that provided on the LSI-11 card is required for running system and applications software. Three types of memory cards are used with the SDAS, depending on availability and system requirements: 4K, 16K, and 32K word capacities.

The 4K word memory used in this sytem is a DEC MSV-11B dynamic MOS RAM. Location of the 4K word block in memory is determined by onboard jumpers. The module is dual-height and bears an M7944 module number.

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3. Microcomputer Interfaces Handbook, (1980) Digital Equipment Co., Maynard, MA

A larger 16K word RAM capabilty is provided by the DEC MSV11-CD dynamic MOS RAM module. Like the 4K module, this unit's position in address space is determined by jumpers. The module is quad-height and has an M7955-YD identification number.

A full 32K words of RAM (the maximum that the LSI-11 can address) can be provided on a single dual-height module by using a Monolithic Systems Corp. MSC4601 LSI-11-compatible memory module.

5.4.5 INTERFACE MODULE DESCRIPTION

Two types of digital interface modules (serial and parallel) are used in the SDAS. The serial interfaces are used to communicate with the system console and printer through the use of full duplex serial bit streams. The parallel interfaces are used to control, write to, and read from the system tape recorder and clocks. Signals for these later units are of a multiline, parallel nature.

DEC DLV-11 serial interface cards (module number M7940) are used in the SDAS. They communicate with asynchronous serial devices using either a 20 mA current loop or a RS232 interface. The cards can provide jumper-selectable data rates of between 50 and 9600 baud with user-selectable character formats. Each dual-height DLV-11 card can support one full-duplex serial link. Signals to and from the external device are routed through a ribbon cable socket on the module. (Note: The DLV-11 used for the printer/plotter interface is modified, as described in Appendix I, to reduce the software overhead needed to support the unit.)

For parallel interfaces, the SDAS uses DEC's DRV-11 parallel line units (module M7941). They provide 16 input, 16 output, and 4 control lines between the module and the device connected to it. All lines are TTL level and appear on two ribbon cable sockets on the board. The module is dual height.

5.4.6 MISCELLANEOUS MODULE DESCRIPTION

Two other module types are used with the SDAS computer - a bus terminator and floppy disk interface. The bus terminator (DEC REV11-A, module M9400-YA) provides several support functions for the LSI-11 system. It includes bus termination resistor networks to provide proper bus voltage and impedance levels. Also on the module is a bootstrap ROM to provide the routines for initial program loading using paper tape, floppy disk, or hard disk program storage media. The module also provides the proper signals for refreshing the system dynamic memories. The bus terminator is a dual-height card and must be inserted as the last card in the card cage.

A DEC RXV-11 floppy disk interface module is also used in the system. This module (number M7946) provides control functions for the RX01 floppy disk subsystem.

5.5 System Controller A/D Converter Description

Due to its importance in the data acquisition process, the A/D converter module will be discussed in greater detail than the other computer modules. A model 600-LSI-11 Data Acquisition and Control System, made by ADAC Corporation of Woburn, MA, is used in the SDAS. The module is built on a quad-height circuit board. Included on the board are input signal multiplexers, the A/D converter, provisions for two D/A converters, and LSI-11 bus interface circuitry.

Input signal multiplexers are provided for up to 16 single-ended or 8 differential analog signals. Expansion to a maximum of 64/32 single ended/differential signals is possible with the addition of additional components to the board. (Single-ended implies that only one of the two input signal leads is switched; the other is tied to ground. Differential implies that both leads are switched, each being connected to one side of a differential input amplifier.) Further, the board can be configured for either true single ended operation or for a pseudo-differential mode. In the latter, the signal common is not connected to signal ground but rather to the low input side of the A/D differential input amplifier. Input signals and grounds are brought onto the board through a ribbon cable socket on the board edge.

After multiplexing, the analog signals are captured by a sample and hold amplifier. The amplifier is used to reduce the effective time that the A/D is connected to a given signal from approximately 15 usec to 20 nsec.

The module uses a 12-bit successive approximation A/D converter to digitize the signals held by the sample and hold. A/D converter range can be selected by jumpers on the module.

Also on the module is one 12-bit D/A converter (solder pads for a second are included, but not components). The input to the converter comes from a user-loaded register on the card. D/A output voltage range is programmed by oncard jumpers. The D/A output signal (and a separate D/A signal return) runs to the ribbon cable socket on the board edge.

Also included on the board is the digital circuitry to connect the multiplexer and converters to the LSI-11 bus. Four registers are provided for the software interface. Two registers contain input words for the D/A converters: one contains the A/D output word, and one contains status/control bits. These latter bits give the status of the module and allow control of the multiplexing and conversion processes.

Table 10 contains key subsystem specifications.

As typically used in the SDAS, the A/D module is set up for -10 to +10 Vdc, pseudo-differential input and -10 to +10 Vdc output. Appendix I details the jumpers required for this configuration.

Table 10 A/D Module Specifications

A/D:	
Input Voltage Range:	-10 to +10 Vdc, 0 to +10 Vdc -5 to +5 Vdc, 0 to +5 Vdc
Digital Code:	Binary (unipolar ranges) 2's complement binary (bipolar ranges)
Max Input Voltage (Proper OPN):	-10.24 to +10.24 Vdc
Max Input Voltage (No Damage):	-15 to +15 Vdc
Sample Time / Channel:	33.4 μsec
Sample and Hold Aperture:	20 nsec
Resolution:	12 bits
Relative Accuracy:	±0.025% of full scale reading (FSR)
Tempco of Linearity:	< 3 ppm FSR / deg C
Tempco of Range:	< 30 ppm FSR / deg C
Tempco of Offset:	0.001% FSR / deg C
Crosstalk:	-80 dB at 1 kHz
Common Mode Rejection:	70 dB (dc to 1 kHz)
Sample and Hold Feedthrough:	-80 dB at 1 kHz
Maximum Error, -FS to +FS Between Channels:	1 LSB
Operating Temperature:	0 to +55 deg C
D/A:	
Output Voltage Range:	-10 to +10 Vdc, 0 to +10 Vdc, -5 to +5 Vdc, 0 to +5 Vdc
Digital Code:	Binary (unipolar ranges) 2's complement binary (bipolar ranges)
Settling Time (to 1/2 LSB):	5 sec, typ; 10 sec, max
Slew Rate:	10 V / μsec
Max Output Current:	5 mA
Max Load Capacitance for Rated Settling Time:	1000 pF
Resolution:	12 bits
Relative Accuracy:	±0.012% FSR
Max Output Drift (at 0 V):	20 ppm FSR / deg C
Max Output Drift (FSR):	40 ppm FSR / deg C
Operating Temperature:	0 to +55 deg C

6. INTERFACE SUBSYSTEM

6.1 Chapter Overview

This chapter covers the interface subsystem, the system digital clock, and the system digital tape recorder. It includes an overview of the subsystems and their interrelationships. Separate sections then cover the interface chassis and its wiring, the system clock and its interface, and the system digital tape recorder and its interface. Detailed support information is included as required in each section.

6.2 Interface Subsystem Functional Description

The interface subsystem houses interface circuits to interconnect the computer's parallel pc ts with the system clock and digital tape recorder. Power for a subsystem is provided by the power supply in the controller chassis.

Mounted in the interface chassis is the system clock. The clock provides the calendar date and time for data identification as well as timing pulses to initiate data sampling. These signals are routed through the interface electronics to the computer.

The system digital tape recorder provides bulk storage on magnetic tape of data acquired by the SDAS. It also can play back prerecorded data tapes for analysis. Input and output signals to/from the recorder are routed through the interface electronics to/from the computer.

6.3 Interface Chassis Description

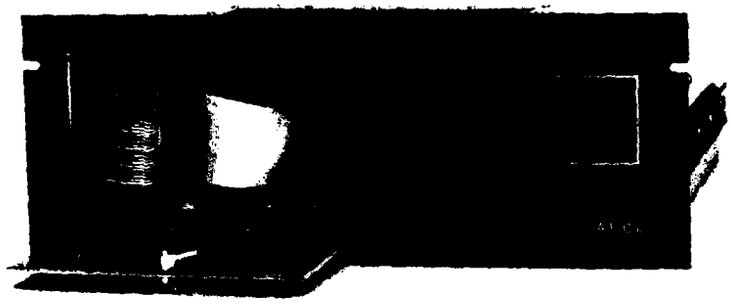
6.3.1 PHYSICAL DESCRIPTION

A custom-built aluminum chassis houses the interface hardware. Figures 21 through 23 give external views of the chassis. Component labels will be referred to below.

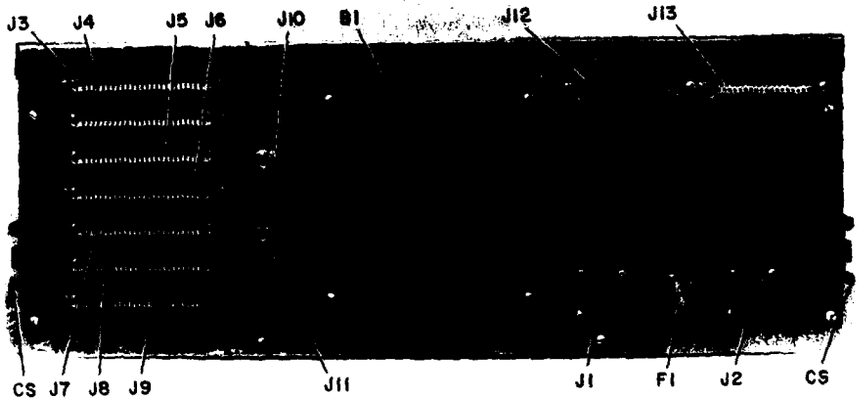
The chassis is designed to fit into a standard 19 in. (48.3 cm) equipment rack. Its front panel is covered with a blue plastic dress panel and is made from 0.125 in. (0.32 cm) aluminum. It measures 6.96 x 19 in. (17.7 x 48.3 cm) and includes a slot in each side for fastening the chassis to an equipment rack. Also mounted on the panel is the system clock. A 5 x 8.25 in. (12.7 x 21 cm) bottom-hinged door is cut into the panel to allow access to the interface cards as shown in Figure 21. In Figure 22, the door is open, showing the cards. The ribbon cables connected to the card edges connect the interface cards to the system clock and the system tape recorder.

The chassis sides, top, and bottom are made from aluminum and measure 19 in. (48.3 cm) deep, 6.5 in. (16.5 cm) high, and 17 in. (43.2 cm) wide. The chassis has a removable top panel to allow access

21. Interface Chassis Front View



22. Interface Chassis Front View
(Front Panel Open)



23. Interface Chassis Rear View

to the wiring and card cage. A Ø.125 in. (Ø.32 cm) rear panel is screwed to the sides and bottom. It contains cutouts for a ventilation fan and for assorted power and signal connectors. Engraved labels are provided on the panel for ease of system interconnection.

The chassis is mounted in the equipment rack on two chassis slides (CS), one on each side of the unit. A ventilation fan (B1) mounted on the rear air provides ventilation for the components inside; a grill in the chassis top allows the air to exhaust. All input, output, and power connectors are mounted on the rear panel. Ac power for the fan and clock is supplied through J1. A power cord (PC), not shown, connects the ac power to J1. A fuse (F1) provides protection for this power. Five Vdc power is supplied to the interface cards through J2. Sockets J3 through J9 connect the interface cards to the parallel interfaces in the controller subsystem. Two BNC connectors (J10 and J11) provide an external connection point for access to the clock master oscillator for special applications. For normal SDAS operation, a BNC to BNC jumper is installed between the two connectors. Finally, J12 and J13 connect the interface cards to the system tape recorder.

An inside view of the chassis (Figure 24) shows the routing of the signal cables between the card cage (CC), back panel, and system clock. The card cage is made up of commercial card guides and edge connectors mounted between two custom-made aluminum plates. The system clock is inserted through the front panel and is supported by an aluminum bracket.

A parts list for the subsystem is given in Table 11.

6.3.2 CHASSIS WIRING

Interface chassis wiring is shown in Figure 25. Power and ground lines are bussed between the edge connectors using 14-gauge buswire. Wirewrap jumpers are used between the two tape recorder interface card connectors. Although the card cage has slots for six circuit boards, only four circuit board edge connectors are currently installed (three active and one spare).

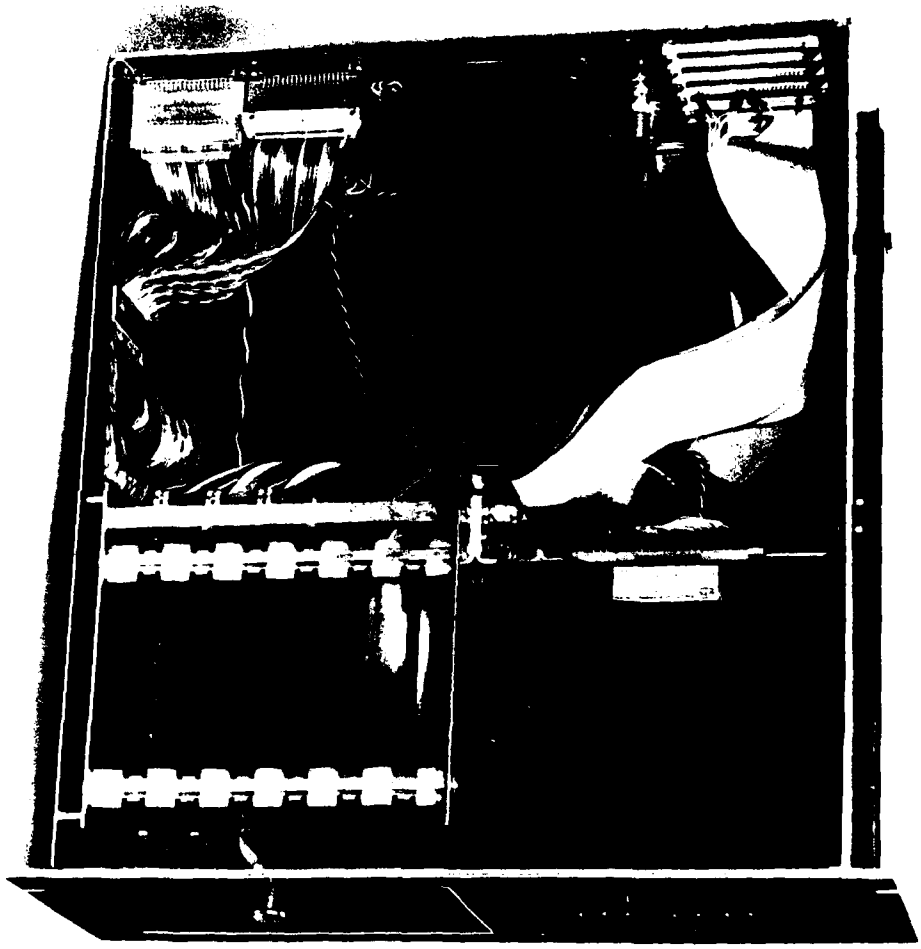
Connections between the card edge connectors and sockets J6-J9 on the back panel are made using 50-conductor ribbon cable. (Sockets J3-J6 are spares and are plugged with ribbon cable connectors to keep out foreign objects.) The back panel end of the cable is terminated with a 3M type 3331 socket; the other end terminates with a type 3307-0000 socket. The 3307 socket plugs directly onto the card cage edge connector pins 1-50. A keying header (3M type 3404) on the connector pins insures proper alignment.

Connections to the oncard sockets are also made using ribbon cables. A 50-conductor cable connects the clock interface to the clock. Forty-conductor twisted pair cables are used to connect the tape recorder interface cards to J12 and J13 on the back panel.

Details on all ribbon cables used in the chassis are contained in Appendices K and L.

Single conductor coax cable connects the clock interface edge

connector with J10 and J11. The edge connector end is stripped and soldered to the edge connector pins, while the other end is terminated with a BNC male connector.



24. Interface Chassis Interior View

Table 11 Interface Chassis Parts List

Part	Noun	Mfgr Part No.	Manufacturer
CS	Chassis slide (2)	C-300-S-20	Zero Corp.
B1	Fan	WR2H1	Rotron
F1	Fuse holder	344-125A	Littlefuse
J1	Connector	PT07A-12-3P	Bendix
J2	Connector	PT07A-12-3S	Bendix
J3-J9	Connector	3331-0000	3M
J10-J11	Connector, BNC	3846	Pomona Electronics
J12	Connector	DD-37P	Cannon
J13	Connector	DD-37S	Cannon
PC	Power cord (with Bendix PT06SE-12-3S connector)	17513	Belden
CC	Card cage parts:		
	Mounting bar (2)	802	Scanbe
	Connector bar (1)	26480-1	Scanbe
	Card guide (12)	T-309-60	Scanbe
	Spacer (20)	T-101-700	Scanbe
	Spacer (8)	T-910	Scanbe
	Edge connector (6)	50-72C-30	Cinch

Note: Card cage bars must be cut to 8 in. length.

6.4 System Clock and Clock Interface

6.4.1 CLOCK DESCRIPTION

The system clock serves two main functions: providing date/time information for recording on the data tapes, and providing the master timing source for data acquisition.

An Electronic Research Company (ERC) model 2446 digital calendar clock (see Figure 26) is used as the SDAS master clock. (Note: ERC no longer makes calendar clocks.) The clock is powered from the 110 Vac power line and uses an internal crystal time base. It provides TTL-level calendar day and time (24 hr period) information in binary coded decimal (BCD) format to the interface. Also sent to the interface are a 1 pps and a 100 pps TTL signal. Both provide interrupt signals to the computer. The 1 pps interrupt can be isabled under user control (see below), while the 100 pps interrupt always enabled. This later rate can be used by system software for data acquisition control.

On the clock's front panel are the user controls. A SET/RUN switch controls the state of the clock. When the switch is in the SET position, day and time (hours and minutes) values can be set into the clock using the pushbutton switches below the time display. When the switch is moved to RUN, the clock starts counting off time, automatically advancing the day count at 0:00:00 hours. A switch to the left of the day display provides for leap years (366 days).

Two printed circuit edge connectors on the back of the clock provide power, control, and data signal connections. (See Appendix K for connector pin identifications.)

The clock has been modified to allow external signal synchronization. The oscillator divider chain is broken at the 1000 pps level and the 1000 pps signal routed to a spare pin on the edge connector. The next divider stage input is also brought to another spare pin on the connector. These signals are buffered and routed to the chassis back panel. (See Appendix K for a detailed description of this modification. Several external signal synchronization procedures are also discussed in Appendix K.)

Table 12 lists clock specifications.

6.4.2 CLOCK INTERFACE DESCRIPTION

A block diagram of the system clock interface is given in Figure 27. (See Appendix K for detailed schematic diagrams and parts list.) The interface consists of a multichannel two-to-one line multiplexer to connect the 30 BCD date/time signals from the clock to the 16 parallel input lines of the LSI-11 parallel interface. Two resetable flipflops on the card buffer the one pps interrupt signal; they are cleared by control signals from the LSI-11 parallel interface card. Finally, a number of buffers are included on the card to isolate the assorted control and pulse train signals that pass between the clock and the system computer.

Appendix K discusses software considerations for reading and controlling the interface. Also included is a short interface checkout program.

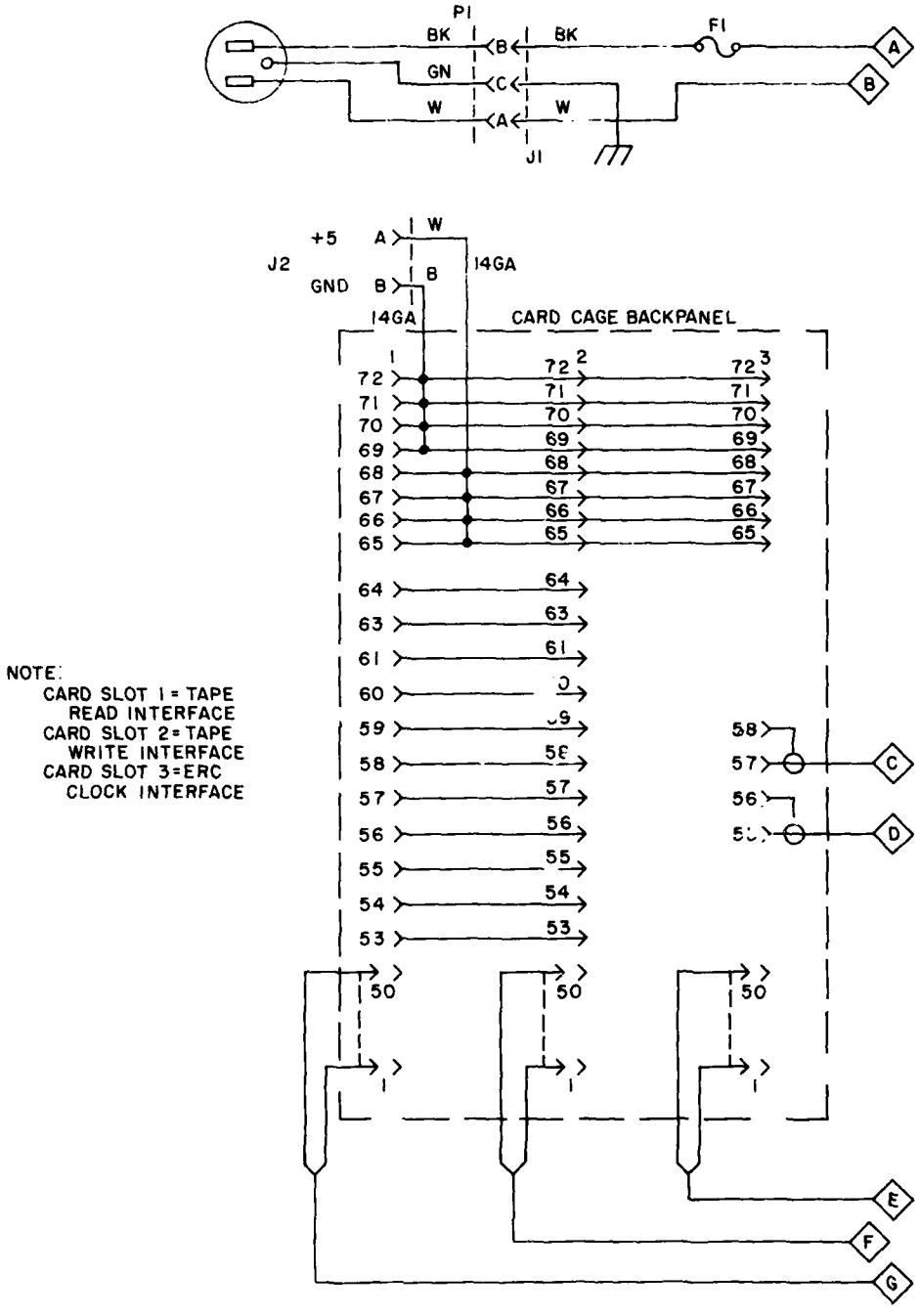
6.5 Digital Tape Recorder and Interface

6.5.1 RECORDER DESCRIPTION

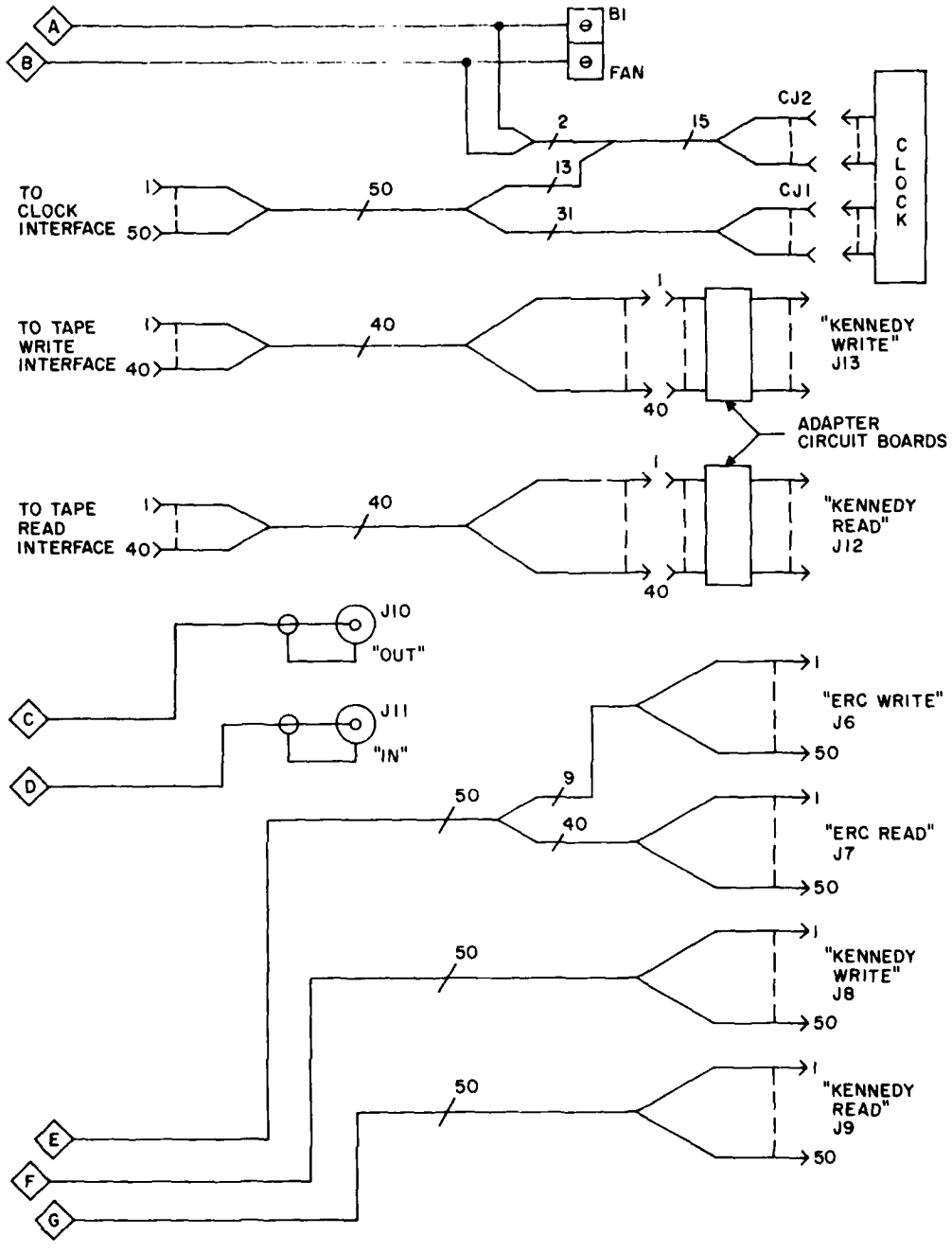
The system digital tape recorder provides the primary means of data storage in the SDAS. It also can be used to play back previously-recorded data tapes for analysis. Further, it provides a backup means of program entry in case of floppy disk failure.

A Kennedy Corp. (Altadena, CA) model 9832 buffered digital tape transport is used as the SDAS digital recorder as shown in Figure 28. It records IBM-compatible (NRZI) tapes in either a 7-track or a 9-track format. (The 9-track format, with 8 data bits and 1 parity bit, is used in the SDAS installation.) Half-inch (1.3 cm) digital magnetic tape is used on 8.5 in. (21.6 cm) reels (1200 ft [366 m] length, nominal); recording density is 800 bpi.

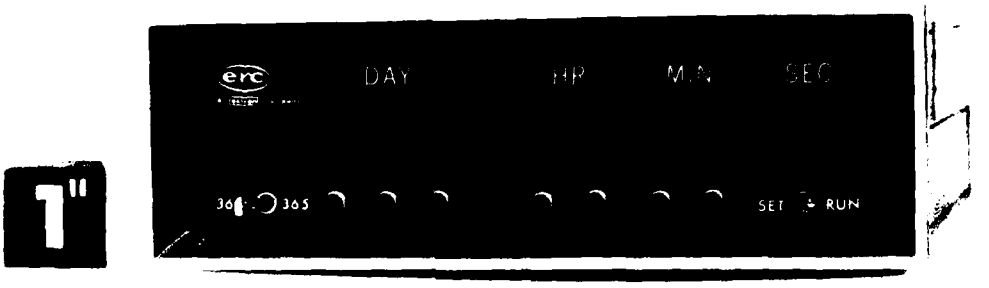
The built-in formatter in the recorder handles many of the functions normally performed by the user. The formatter consists of two 1024-character buffer memories and appropriate control, error check, and interface circuitry. (Character size is 6 or 8 bits for 7- or 9-track operation, respectively.) The received data is loaded into



25. Interface Chassis Schematic



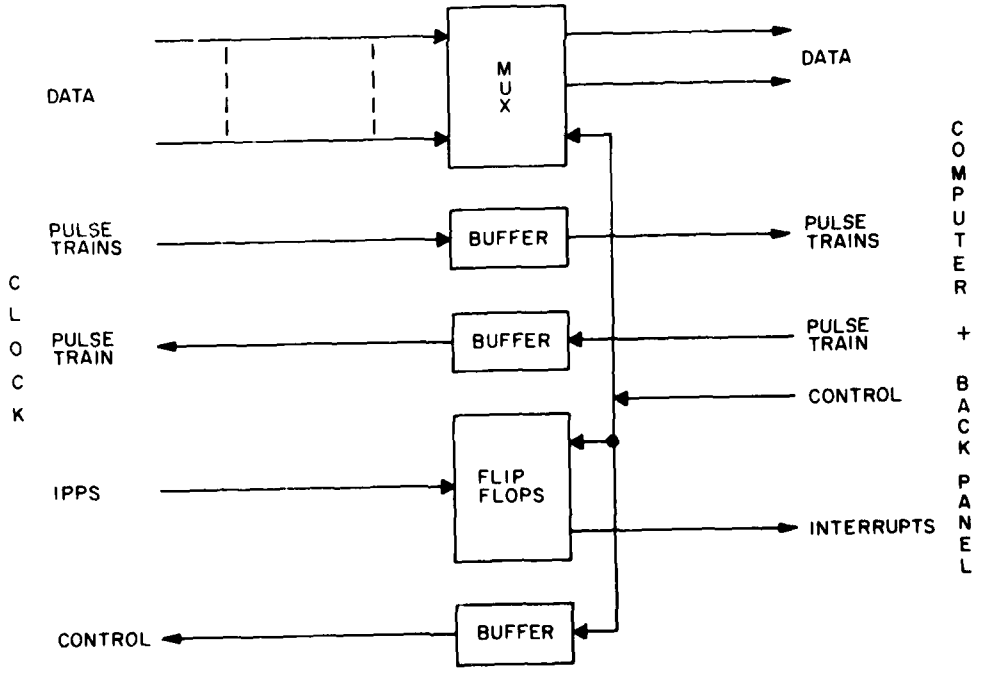
25. Interface Chassis Schematic (Cont.)



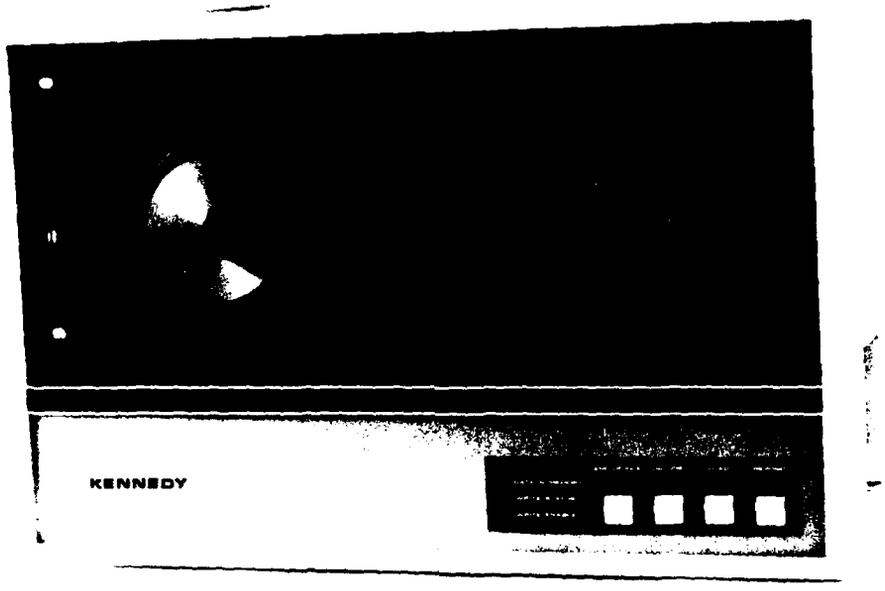
26. System Clock Front View

Table 12 System Clock Specifications

Time Base:	Crystal oscillator
Worst Case Accuracy (Constant Temp):	± 5 ppm
Oscillator Tempco:	± 20 ppm / deg C
Oscillator Frequency:	1.00 MHz
Operating Temperature:	0 to +50 deg C



27. System Clock Interface Simplified Block Diagram



28. Tape Recorder Front View

a memory which, when full, is swapped with the second memory. While the second is being filled with data, the first is being recorded on tape as a 1024-character record. When the second buffer is full, it is swapped with the first and the process of loading and dumping to tape continues; should the second memory fill before the first is finished dumping to tape, a busy signal is sent to the user until a memory is free for loading. The formatter includes built-in read after write capablity to perform error checks of the recorded data. Should an error be detected, the unit automatically backspaces the tape and rerecords the data. The entire load/write process can support an average asynchronous data rate of 13,617 characters per second (maximum burst data rate is 250,000 characters per second).

For reading data, the formatter initially loads a 1024-character record of data into both buffer memories. The first buffer is then made available for asynchronous user readout. When it is empty, the second buffer is made available for user access while the first is being filled from the tape. The data is available as an 8-bit parallel word. As in read, automatic error checking and rereading is built into the formatter. In the read mode, the transport can support an average read rate of 13,617 characters per second.

Other functions are also performed by the formatter. A command allows the user to dump a partially filled memory to tape. Another command writes an end of file to the tape, while further commands control read/write status, initiate a rewind of the tape, and reinitialize the formatter.

Weighing 50 lb (23 kg), the recorder is designed to mount in a standard 19 in. (48.3 cm) equipment rack occupying 12.25 in. (31.1 cm) of rack space. The unit is 16.68 in. (42.4 cm) deep and requires a 110 Vac power source. It is rated for operation over a +2 to +50° C temperature range.

6.5.2 TAPE RECORDER MODIFICATION DESCRIPTION

Operational problems (due to crosstalk between write data lines and write command lines) resulted in a redesign of the tape recorder write adapter card. This card plugs into the rear of the recorder and connects the recorder's internal data and control signals to the outside world. The new card has differential line receivers to match the differential line drivers on the interface card. To provide power for the new card, one additional wire had to be added to the write adapter socket.

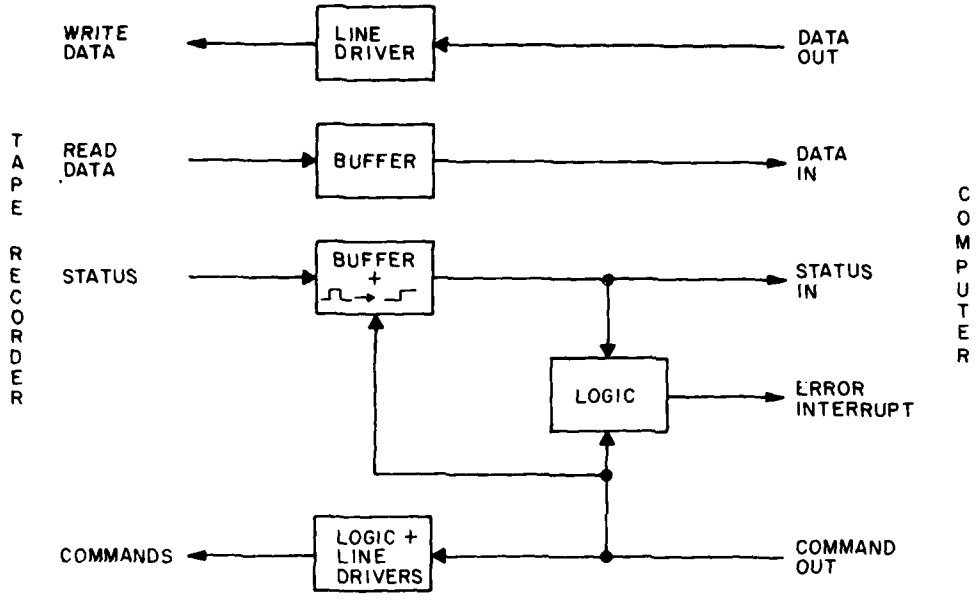
These modifications are transparent to the SDAS user. Full details of both the new card and the recorder modification procedures are contained in Appendix L.

6.5.3 TAPE RECORDER INTERFACE DESCRIPTION

Two printed circuit boards in the interface chassis provide the interface electronics between the tape recorder and the DRV-11 parallel line interface module in the computer. The interface functions are divided between the two boards. An overall view of these functions is given in Figure 29.

The interface provides the buffering and differential line drivers for write data and buffering for read data. Recorder status information is buffered on the cards and, for certain signals, converted from a pulse to a level before being sent to the DRV-11 module. These status signals, together with certain command signals, are combined through digital logic to produce an error signal for interrupting the SDAS computer in case of recorder problems. The cards also include logic for forming and buffering the commands issued to the recorder to control its operations.

Complete circuit descriptions and parts lists for these interface cards are included in Appendix L. Also listed there are software considerations for interface operation and a short computer program for checking out the tape recorder and its interface.



29. Tape Recorder Interface Simplified Block Diagram

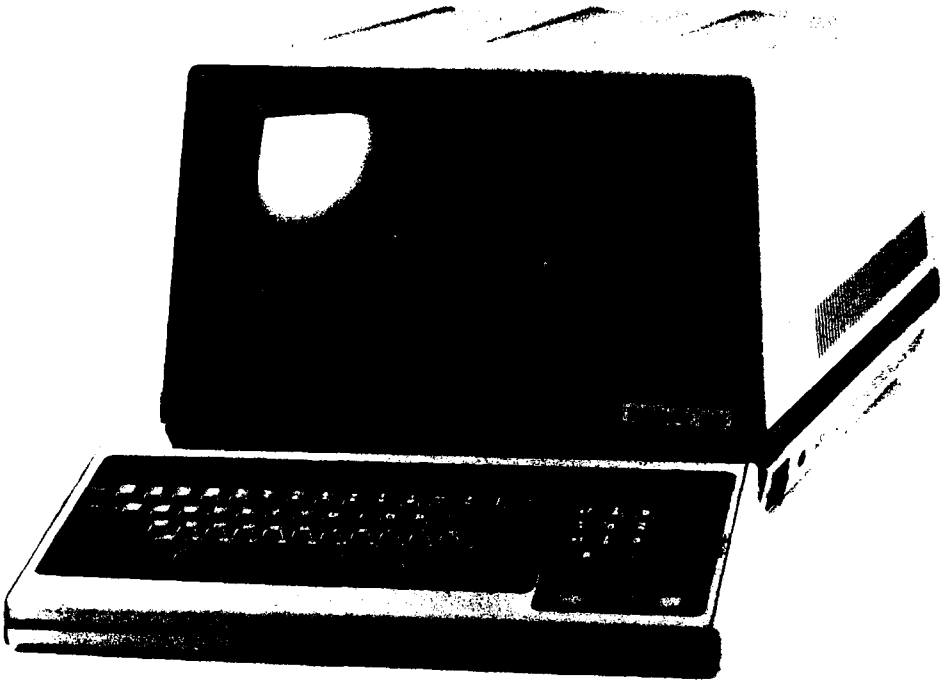
7. SYSTEM PERIPHERALS

7.1 Chapter Overview

This chapter describes the peripheral hardware needed for SDAS operation. This hardware includes the system console, printer/plotter, chart recorder, floppy disk memory, intercom system, and system shipping cases. A brief description of each of these items, together with appropriate specifications, follows. More details can be found in the equipment users manuals.

7.2 System Console Description

A Tektronix Model 4025 computer display terminal (see Figure 30) is used as the SDAS computer system console. The terminal has the capability of displaying both alphanumeric and graphic data using a raster scan display format. It can display 34 lines of 80 characters of ASCII alphanumeric data stored in a built-in 16K-byte buffer memory. Up to 2048 cells of graphics data can also be displayed in the user-defined graphics area (each cell is a 14x8 dot matrix). The terminal allows offline editing of text prior to transmission to the



30. System Console Front View

system computer. Most keys on the console keyboard can be redefined by keyboard-entered commands as can the communications interface configuration. The terminal communicates with the system computer over an RS232 serial line with data rates up to 9600 baud in a full or half duplex mode.

The detachable terminal keyboard has an 8 ft (2.44 m) cable connecting it to the display; this allows considerable leeway in terminal installation. The display measures 12.5 x 17.5 x 21.3 in. (31.7 x 44.5 x 54 cm), while the keyboard measures 3 x 18 x 9.3 in. (7.6 x 45.7 x 23.5 cm). Rated at an operating temperature range of +10 to +40° C., the terminal can be stored at -60 to +50° C. It weighs 60 lb (27.2 kg).

7.3 Printer/Plotter Description

A Bedford Computer Systems, Inc. System 75 data terminal is used as the SDAS printer/plotter (Figure 31). The System 75 is built around the Hytype II printer mechanism made by Diablo System, Inc. Under built-in microprocessor control, the System 75 can print 45 characters per second. Microprocessor routines optimize printhead motion (by combining strings of motion commands) to yield a higher effective character throughput. As a plotter, the System 75 has a

resolution of 120 horizontal and 48 vertical steps per inch. Bicolored ribbons allow both red and black printing/plotting, thus enhancing output readability.

The Bedford System 75 accepts either single sheet or continuous-sheet paper up to 14 in. (35.6 cm) in width. It will also accept standard sprocket-feed 14.9 x 11 in. (37.9 x 27.9 cm) fan-fold computer paper. It can produce plots or listings up to 13.2 in. (33.6 cm) wide with a length limited by the paper available.

The System 75 communicates with the SDAS computer over a serial full- or half-duplex RS232 data link at either 300 or 1200 baud. An internal 128-character buffer is included in the unit reduces system computer overhead requirements (see Appendix I, section I-4, for a description of a modification to the computer serial interface card to take full advantage of this buffer). ASCII character strings from the SDAS computer can be used to change a number of terminal parameters, including tab stops, ribbon color, margins, form size, and line spacing. Measuring 8.3 x 23.3 x 21 in. (21 x 59 x 53.3 cm), the System 75 weighs 48 lb (21.8 kg) and is rated for an operational temperature range of +7 to +35° C. It requires 110 Vac power for operation.

7.4 Chart Recorder Description

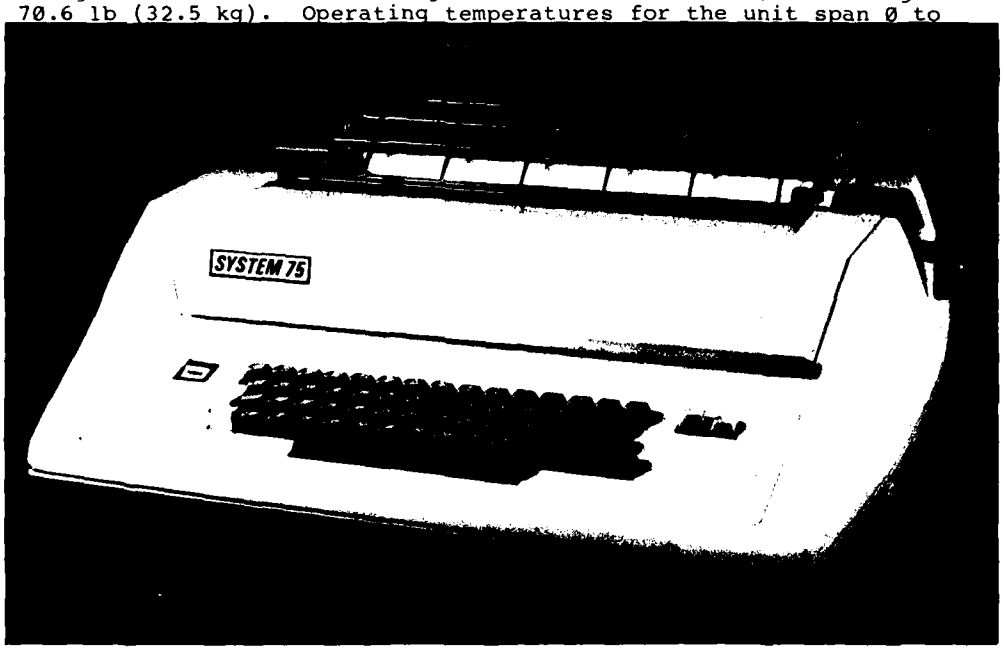
The model 1858 Visicorder (manufactured by the Honeywell Test Instrument Division, Denver, CO) oscillographic recorder is used as the SDAS chart recorder. The Visicorder is an 18-channel optical chart recorder with a dc to 5 KHz frequency response (see Figure 32). It uses ultraviolet light generated by a cathode ray tube to expose photosensitized direct print paper. Exposure to room lighting devlopes the paper and yields the finished recording. Chart speeds from 0.1 to 120 in./sec are selected by front panel controls on the recorder. Time and grid lines recorded on the chart assist in reading the resulting record. Further, an external timeline input allows time mark generation by an external clock (such as the SDAS 1 pps clock output). Also written on the chart are channel identification numbers as aids to keeping track of the 18 channels.

Eighteen individual channel preamplifiers (Honeywell Model 1883A) are used to amplify the incoming signals. Front panel gain and trace positioning controls on the preamps allow formatting of the channels for ease of reading and optimum sensitivity. Each preamp also has calibration controls to allow accurate amplitude calibration. Due to the high sensitivity of the preamps, a padding network has to be added to allow 18 channels of 20 V p-p (the output range of the signal conditioning subsystem) to readily fit on the chart. Details on the pad are contained in Appendix M.

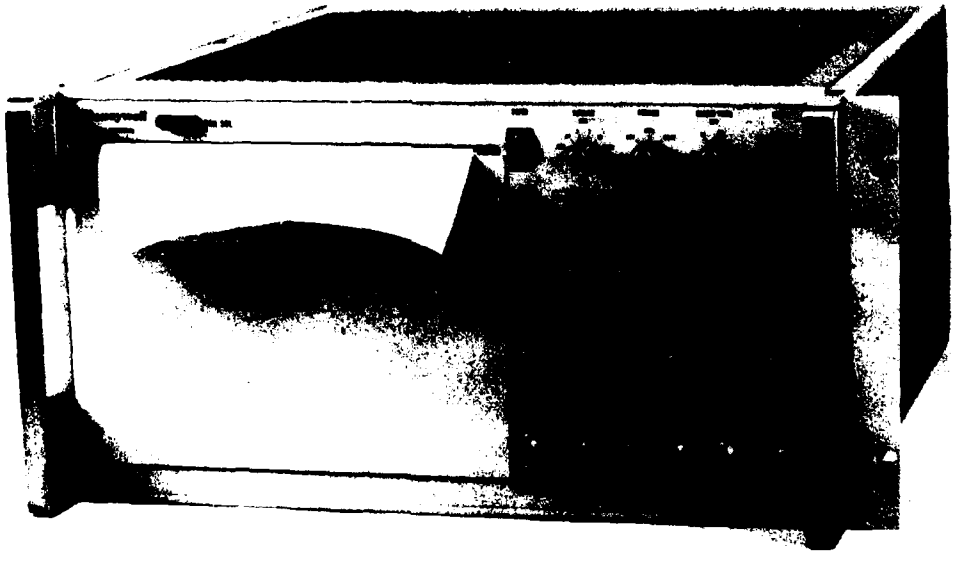
The Visicorder preamp can accept signals from either the front-mounted BNC or rear-mounted input connectors. Which input is connected is determined by jumpers mounted within the preamp. Appendix M gives further information on these jumpers.

The Visicorder can be mounted in a standard 19 in. (48.2 cm) equipment rack. It occupies 8.8 in. (22.2 cm) of rack space and is 19 in. (48.2 cm) deep. Front panel controls and carrying handles

bring the total instrument depth to 21 in. (53.3 cm). It weighs 70.6 lb (32.5 kg). Operating temperatures for the unit span 0 to



31. Printer/Plotter Front View



32. Chart Recorder Front View

7.5 Floppy Disk System Description

A DEC RX01 dual floppy disk system is used with the SDAS (see Figure 33). The RX01 is a single-sided, single density disk drive that uses 8 in. soft sectored floppy disks. The disk is organized as 77 tracks with 26 sectors per track. Each sector has a capacity of 128 bytes. The RX01 has a formatted capacity of 256K bytes per drive. Average access time for a read or write operation is 483 msec. The drives connect to the LSI-11 computer through a 40-conductor ribbon cable connected to a RXV11 interface card. A built-in power supply is included for powering the drives and drive electronics.

The RX01 mounts in a standard 19 in. (48.2 cm) equipment rack, occupying 10.8 in. (27.3 cm) of rack space. It requires 20 in. (50.8 cm) of rack depth and has a total depth of 21.5 in. (54.6 cm). The dual drive assembly weighs 60 lb (27.2 kg). Operating temperatures for the assembly are +15 to +32° C.

7.6 Intercom System Description

A sound-powered headset system is used for communications between persons near the junction box and the signal conditioning system. David Clark model 5030 headsets are used, with the cables terminated in Switchcraft type 480 plugs.

33. Floppy Disk System Front View

7.7 Shipping Case Description

Customized fiberglass shipping cases are used to provide in-transit protection for the major components of the SDAS. They were built by Environmental Container Systems (ECS) of Grants Pass, Oregon. The cases are made of pressure-laminated fiberglass with aluminum extrusion fittings. They are waterproof. Each is equipped with a manual pressure relief valve to allow equalization of internal air pressure prior to opening. Cam-action catches hold the removable covers onto the case bodies, while heavy-duty hand grips allow easy carrying. These cases take two forms: transit cases and instrumentation enclosures.

Figure 34 shows typical transit cases. These cases are used to ship the system console and the printer/plotter. Custom-contoured foam cushions in the cases provide shock control for the items shipped.

ECS instrumentation enclosures are designed for housing and shipping rack-mounted equipment. Each case has removable front and rear covers to allow access to the equipment rack. The rack itself is mounted on elastomeric shock mounts to provide shock and vibration attenuation. It accepts standard 19 in. (46.3 cm) rack modules. Figure 35 shows the SDAS enclosures.

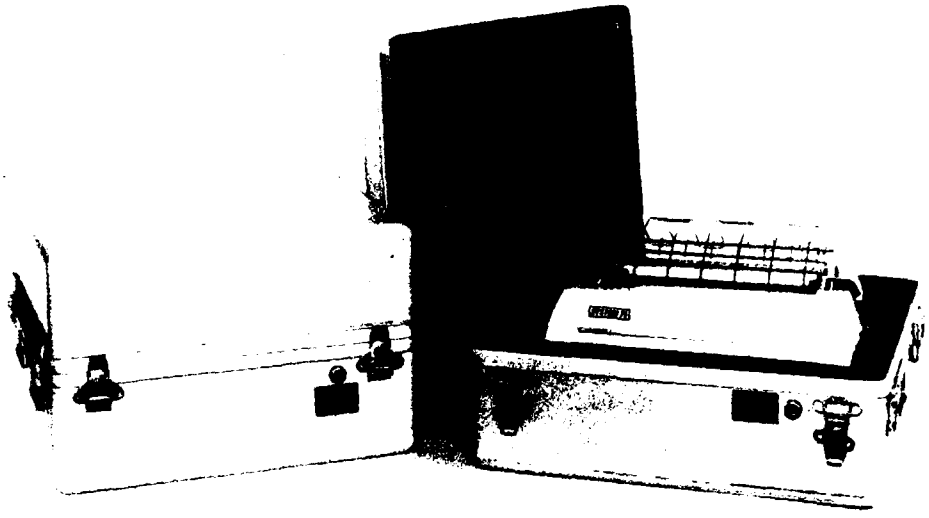
Two sizes of instrument enclosures house the SDAS. One provides 29.8 in. (75.6 cm) of rack space. In it are mounted, top to bottom, the RXØ1 floppy disk, the interface chassis, and the system controller chassis as shown in Figure 35. These subsystems are mounted on equipment slides attached to the enclosure rack. The other rack provides 24.5 in. (62.2 cm) of rack space; it houses the digital tape recorder, signal conditioning subsystem, and a 3.5 in. (8.9 cm) high drawer unit. The drawer unit contains the resistors used to configure the signal conditioning cards.

Another 24.5 in. (62.2 cm) equipment enclosure housing test equipment is used in conjunction with the SDAS. Included in it are the Visicorder described above, a rack-mounted storage oscilloscope (Tektronix model 466 in Tektronix type Ø35-Ø131-ØØ rack adapter), a rack-mounted digital multimeter (Data Precision model 35ØØ), and a 3.5 in. (8.9 cm) high drawer unit for test leads and probes.

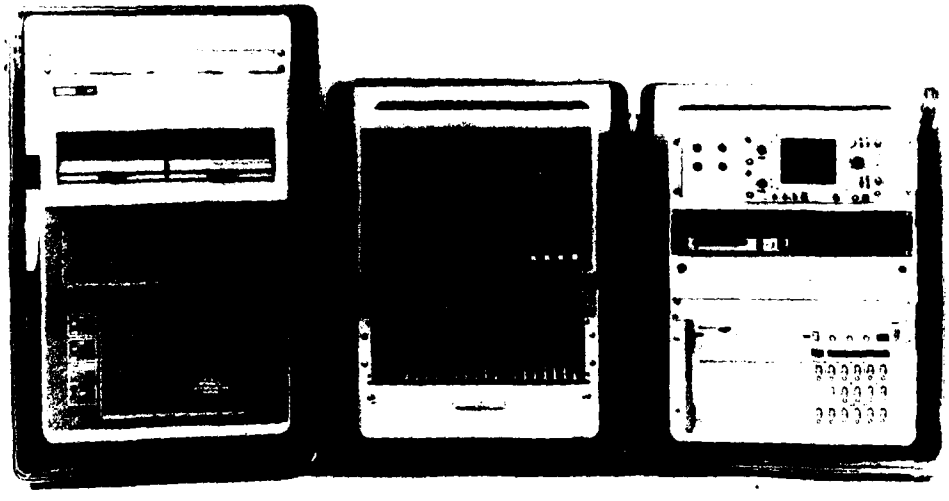
8. SUBSYSTEM INTERCONNECTION DESCRIPTION

The previous six chapters have described the various components of the Standalone Data Acquisition System. In order for the system to function, these components must be interconnected as described in the following paragraphs.

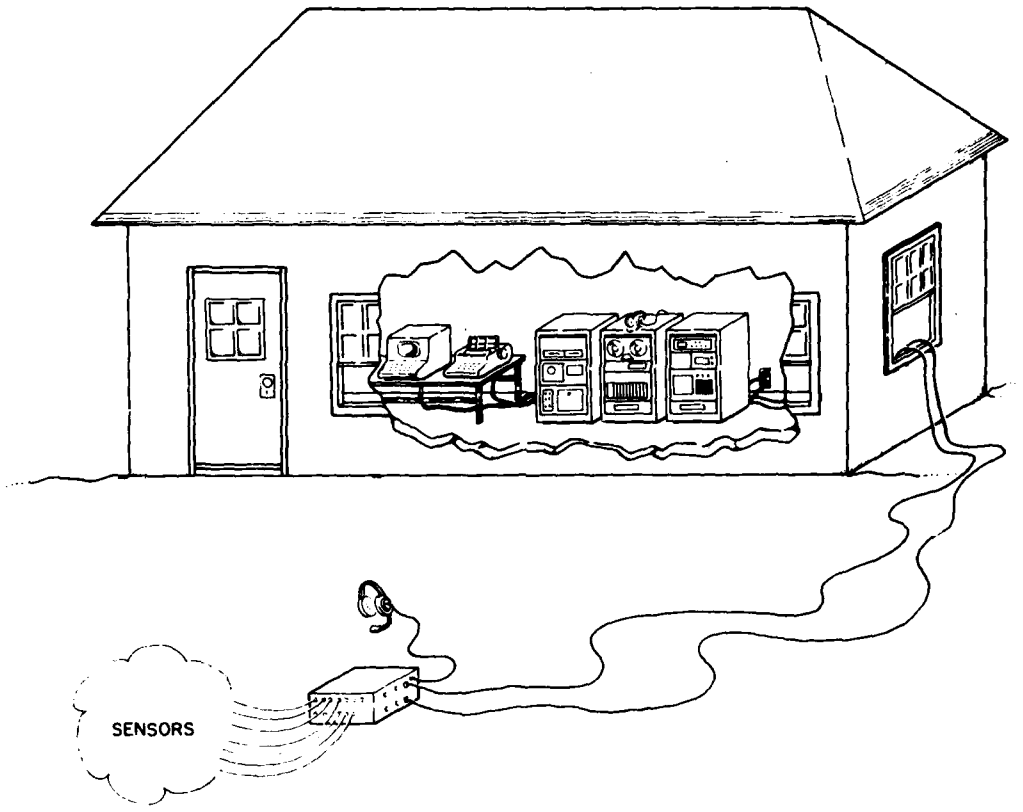
A typical field installation of the SDAS is illustrated in Figure 36. In such an installation, the sensor array and junction box are located remotely from the equipment racks. These later items, together with the system console, printer/plotter, and instrumentation rack (if used), would be located in a climate-controlled area. Sufficient power must be available in this area to run the system.



34. Transit Cases



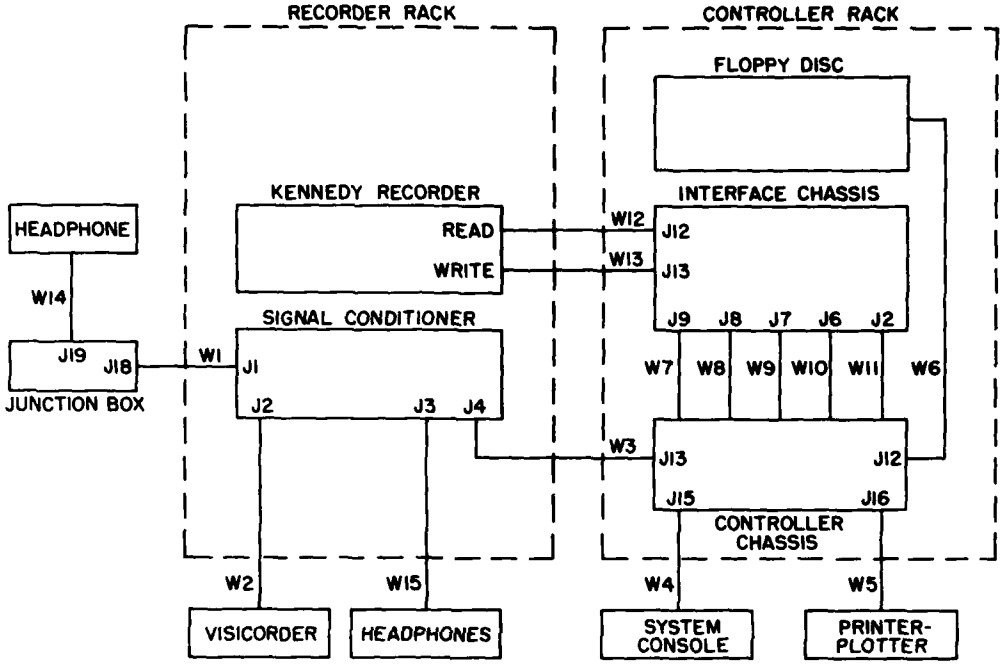
35. Instrumentation Enclosures



36. SDAS Field Installation

Further, tables of some sort are required to support the console and printer/plotter.

Sensors (such as seismometers with preamplifiers or pressure sensors) are connected to J1-J16 of the junction box, as is the intercommunications headphone. A signal and a power cable run from the junction box to the SDAS signal conditioning subsystem and the nearest power line, respectively. A block diagram of the SDAS equipment racks, showing interconnections, is given in Figure 37. Details of the interconnection cables, including location of connector pin identification, is given in Table 13.



37. SDAS Equipment Interconnection Diagram

Table 13 SDAS Interconnection Cable Details

Cable			Connector		Signal
ID	Length	Type	Type	Pin ID Locn	ID
W1	1000 ft	Belden 8769	Bendix PT06SE-24-61P(SR)	A-2, B-1	Analog - sensor outputs
W2	6 ft	Belden 8451 (x18)	Bendix PT06SE-24-61S(SR) & Amphennol 165-33 (Honeywell P/N 16773755-001)	B-2	Analog - conditioned signals
W3	5 ft	Note 1	Cannon DD50P	B-3, H-4	Analog - conditioned signals
W4	10 ft	Note 2	Cannon DB25P	H-3	SD* - console
W5	10 ft	Note 2	Cannon DB25P	H-3	SD - printer/plotter
W6	7 ft	3M #3365/40	3M #3417	Ref 3	PD** - floppy disk
W7	22 in.	3M #3365/50	3M #3425	H-1, L-4	PD - tape read
W8	24 in.	3M #3365/50	3M #3425	H-2, L-7	PD - tape write
W9	26 in.	3M #3365/50	3M #3425	H-1, K-3	PD - clock read
W10	28 in.	3M #3365/50	3M #3425	H-2, K-3	PD - clock write
W11	24 in.	Note 3	Bendix PT06SE-12-3P	Fig. 19, Fig. 25	5 Vdc power
W12	5 ft	Spectra-Strip 455-248-40	Cannon DD-37S	L-5	PD - read data
W13	5 ft	Spectra-Strip 455-248-40	Cannon DD-37P	L-8	PD - write data
W14	3 ft	Note 2	Switchcraft 267	A-2	Audio
W15	3 ft	Note 2	Switchcraft 267	B-1	Audio

* "SD" = serial digital.
** "PD" = parallel digital.

Notes:
1. Custom-made cable (20 - #26 AWG stranded wire with shield).
2. Comes with equipment.
3. Custom-made cable (2 - #14 AWG stranded).

References

1. Syverson, C.R.; Blaney, J.I.; Hartnett, E.B.; Molineux, C.E. (1978) Geokinetic Environment Studies, AFGL-TR-78-0124, Final Report, Boston College

2. Microcomputer Processor Handbook (1979), Digital Equipment Co., Maynard, MA

3. Microcomputer Interfaces Handbook (1980), Digital Equipment Co., Maynard, MA

4. Tow, J. (1969a) Design formulas for active RC filters using operational-amplifier Biquad, Electronic Letters, 5 (No. 15):339-341

5. Tow, J. (1969b) A step-by-step active filter design, IEEE Spectrum, 6 (Dec 69):64-68

6. Thomas, L.C. (1971a) The biquad: part I - some practical design considerations, IEEE Transactions on Circuit Theory, CT-18 (No. 3):350-357

7. Thomas, L.C. (1971b) The biquad: part II - a multipurpose active filtering system, IEEE Transactions on Circuit Theory, CT-18 (No. 3):358-361

8. Daniels, R.W. (1974) Approximation Methods for Electronic Filter Design, McGraw Hill, New York, Chapter 14

Appendix A

Junction Box Details

A.1 JUNCTION BOX CONNECTOR WIRING

Tables A-1 and A-2 give the connector pin identification and signal routing for junction box connectors J1-J19. Belden 8451 two-conductor shielded cable is used for all signal lines. The red conductor is used for the + signal, while the black is used for the - signal.

A.2 JUNCTION BOX OVERVOLTAGE PROTECTOR ADJUSTMENT PROCEDURES

The overvoltage protection (OVP) devices in the junction box are designed to short out the power supply output if that output voltage exceeds a preset value. The following steps should be followed to adjust the OVP threshold.

1. Unplug power cord. Disconnect all input and output cables.
2. Remove the two dc power fuses.
3. Jumper across one fuse holder (the power supply overcurrent protection circuits prevent damage when the OVP fires and shorts out the output.)
4. Connect voltmeter from jumpered fuse to power common.
5. Turn potentiometer on OVP connected to jumpered fuse fully counterclockwise.
6. Plug in junction box power cord.
7. Adjust power supply output voltage, as measured by the voltmeter, to the desired OVP trip voltage. (Adjustment potentiometer is near the terminal strip on power supply.)

8. Turn the OVP potentiometer clockwise until OVP trips (measured voltage drops to approximately zero).
9. Unplug power supply.
10. Move jumper and voltmeter to other fuse slot.
11. Repeat steps 5 through 9 for the second OVP.
12. Remove jumper. Connect voltmeter between one power supply output and the power supply common.
13. Plug in power cord.
14. Adjust power supply output for desired operational voltage.
15. Unplug power cord.
16. Replace both fuses.
17. Plug in power cord. Measure each power supply output to power common with voltmeter to verify that neither OVP is tripped.
18. Dab locking compound (or nail polish) on the two OVP potentiometers to insure that the setting is retained.

Table A-1 Junction Box Input Connector (J1-J17) Pin Identification

J1-J17 Connector: Bendix PT07A-12-10S Mating Connector: Bendix PT06SE-12-10P(SR)			
J1-J17		Destination:	
Pin	Signal	Connector	Pin
A	+ 12 Vdc	(Power Supply)	
B	- 12 Vdc	(Power Supply)	
C	Power shield	NC	
D	Signal +	J17	-
E	Signal -	J17	-
F	Signal shield	J17	-
G	Calibration	J17	AA
H	Power common/ calibration return	J17 (and Power Supply)	BB
K	Calibration shield	NC	

Table A-2 Junction Box Output Connector (J18) Pin Identification

J18 Connector: Bendix PT07A-24-61S Mating Connector: Bendix PT06SE-24-61P(SR)			
J18		Destination	
Pin	Signal	Connector	Pin
A	Channel 1 signal +	J1	A
B	Channel 1 signal -	J1	B
c	Channel 1 shield	J1	C
C	Channel 2 signal +	J2	A
D	Channel 2 signal -	J2	B

Table A-2 Junction Box Output Connector (J18)
Pin Identification (contd)

d	Channel 2 shield	J2	C
E	Channel 3 signal +	J3	A
e	Channel 3 signal -	J3	B
f	Channel 3 shield	J3	C
F	Channel 4 signal +	J4	A
G	Channel 4 signal -	J4	B
g	Channel 4 shield	J4	C
H	Channel 5 signal +	J5	A
J	Channel 5 signal -	J5	B
h	Channel 5 shield	J5	C
K	Channel 6 signal +	J6	A
i	Channel 6 signal -	J6	B
j	Channel 6 shield	J6	C
L	Channel 7 signal +	J7	A
M	Channel 7 signal -	J7	B
N	Channel 7 shield	J7	C
P	Channel 8 signal +	J8	A
m	Channel 8 signal -	J8	B
n	Channel 8 shield	J8	C
R	Channel 9 signal +	J9	A
S	Channel 9 signal -	J9	B
p	Channel 9 shield	J9	C
T	Channel 10 signal +	J10	A
U	Channel 10 signal -	J10	B
q	Channel 10 shield	J10	C
V	Channel 11 signal +	J11	A
r	Channel 11 signal -	J11	B
s	Channel 11 shield	J11	C
W	Channel 12 signal +	J12	A
X	Channel 12 signal -	J12	B
t	Channel 12 shield	J12	C
Y	Channel 13 signal +	J13	A
Z	Channel 13 signal -	J13	B
u	Channel 13 shield	J13	C
a	Channel 14 signal +	J14	A
b	Channel 14 signal -	J14	B
v	Channel 14 shield	J14	C
w	Channel 15 signal +	J15	A
x	Channel 15 signal -	J15	B
JJ	Channel 15 shield	J15	C
y	Channel 16 signal +	J16	A
z	Channel 16 signal -	J16	B
KK	Channel 16 shield	J16	C
AA	Calibration +	J1-J17	G
BB	Calibration -, Power common	J1-J17 (+Power supply)	H
CC	Calibration shield	(Case)	
DD	Spare channel signal +	J17	A
EE	Spare channel signal -	J17	B
MM	Spare channel shield	J17	C
FF	Intercom signal +	J19	Tip
GG	Intercom signal -	J19	Ring
NN	Intercom shield	(Case)	

Appendix B

Signal Conditioner Chassis Wiring

Tables B-1 through B-6 give the pin identifications and signal routing for the signal conditioner chassis input and output connectors (J1-J4) and all card sockets. Belden 8451 two-conductor shielded cable is used for all signal lines except between sockets 1-16 and socket 17, where twisted pair is used.

Table B-1 Signal Conditioner Input Connector (J1)
Pin Identification

J1 Connector: Bendix PT07A-24-61S Mating Connector: Bendix PT06SE-24-61P(SR)			
J1		Destination	
Pin	Signal	Socket	Pin
A	Channel 1 signal +	1	7
B	Channel 1 signal -	1	9
c	Channel 1 shield	1	-
C	Channel 2 signal +	2	7
D	Channel 2 signal -	2	9
d	Channel 2 shield	2	-
E	Channel 3 signal +	3	7
e	Channel 3 signal -	3	9
f	Channel 3 shield	3	-
F	Channel 4 signal +	4	7
G	Channel 4 signal -	4	9
g	Channel 4 shield	4	-
H	Channel 5 signal +	5	7
J	Channel 5 signal -	5	9

Table B-1 Signal Conditioner Input Connector (J1)
Pin Identification (contd)

h	Channel 5 shield	5	-
K	Channel 6 signal +	6	7
i	Channel 6 signal -	6	9
j	Channel 6 shield	6	-
L	Channel 7 signal +	7	7
M	Channel 7 signal -	7	9
N	Channel 7 shield	7	-
P	Channel 8 signal +	8	7
m	Channel 8 signal -	8	9
n	Channel 8 shield	8	-
R	Channel 9 signal +	9	7
S	Channel 9 signal -	9	9
p	Channel 9 shield	9	-
T	Channel 10 signal +	10	7
U	Channel 10 signal -	10	9
q	Channel 10 shield	10	-
V	Channel 11 signal +	11	7
r	Channel 11 signal -	11	9
s	Channel 11 shield	11	-
W	Channel 12 signal +	12	7
X	Channel 12 signal -	12	9
t	Channel 12 shield	12	-
Y	Channel 13 signal +	13	7
Z	Channel 13 signal -	13	9
u	Channel 13 shield	13	-
a	Channel 14 signal +	14	7
b	Channel 14 signal -	14	9
v	Channel 14 shield	14	-
w	Channel 15 signal +	15	7
x	Channel 15 signal -	15	9
JJ	Channel 15 shield	15	-
y	Channel 16 signal +	16	7
z	Channel 16 signal -	16	9
KK	Channel 16 shield	16	-
AA	Calibration output +	18	1
BB	Calibration output -	18	A
CC	Calibration shield	18	-
DD	Spare channel signal +	18	2
EE	Spare channel signal -	18	B
MM	Spare channel shield	18	-
FF	Intercom signal +	J3	Tip
GG	Intercom signal -	J3	Ring
NN	Intercom shield	J3	Sleeve

Table B-2 Signal Conditioner Chart Recorder Output (J3) Pin Identification

J3 Connector: Bendix PTØ7A-24-61P
Mating Connector: Bendix PTØ6SE-24-61S(SR)

J3		Destination	
Pin	Signal	Socket	Pin
A	Channel 1 output +	1	19
B	Channel 1 output -	1	X
c	Channel 1 shield	1	X
C	Channel 2 output +	2	19
D	Channel 2 output -	2	X
d	Channel 2 shield	2	X
E	Channel 3 output +	3	19
e	Channel 3 output -	3	X
f	Channel 3 shield	3	X
F	Channel 4 output +	4	19
G	Channel 4 output -	4	X
g	Channel 4 shield	4	X
H	Channel 5 output +	5	19
J	Channel 5 output -	5	X
h	Channel 5 shield	5	X
K	Channel 6 output +	6	19
i	Channel 6 output -	6	X
j	Channel 6 shield	6	X
L	Channel 7 output +	7	19
M	Channel 7 output -	7	X
N	Channel 7 shield	7	X
P	Channel 8 output +	8	19
m	Channel 8 output -	8	X
n	Channel 8 shield	8	X
R	Channel 9 output +	9	19
S	Channel 9 output -	9	X
p	Channel 9 shield	9	X
T	Channel 1Ø output +	1Ø	19
U	Channel 1Ø output -	1Ø	X
q	Channel 1Ø shield	1Ø	X
V	Channel 11 output +	11	19
r	Channel 11 output -	11	X
s	Channel 11 shield	11	X
W	Channel 12 output +	12	19
X	Channel 12 output -	12	X
t	Channel 12 shield	12	X
Y	Channel 13 output +	13	19
Z	Channel 13 output -	13	X
u	Channel 13 shield	13	X
a	Channel 14 output +	14	19
b	Channel 14 output -	14	X
v	Channel 14 shield	14	X
w	Channel 15 output +	15	19
x	Channel 15 output -	15	X
JJ	Channel 15 shield	15	X
y	Channel 16 output +	16	19
z	Channel 16 output -	16	X
KK	Channel 16 shield	16	X
AA	Summation Card output +	19	19
BB	Summation Card output -	19	X
CC	Summ. Card out shield	19	X
DD	Calib. Card output +	18	19
EE	Calib. Card output -	18	X
MM	Calib. Card out shield	18	X

Table B-3 Signal Conditioner A/D Output Connector (J4) Pin Identification

J4 Connector: Cannon DD50S
Mating Connector: Cannon DD50P

J4		Destination	
Pin	Signal	Socket	Pin
16	Channel 1 output +	1	21
15	Channel 2 output +	2	21
14	Channel 3 output +	3	21
13	Channel 4 output +	4	21
12	Channel 5 output +	5	21
11	Channel 6 output +	6	21
10	Channel 7 output +	7	21
9	Channel 8 output +	8	21
33	Channel 9 output +	9	21
32	Channel 10 output +	10	21
31	Channel 11 output +	11	21
30	Channel 12 output +	12	21
29	Channel 13 output +	13	21
28	Channel 14 output +	14	21
27	Channel 15 output +	15	21
26	Channel 16 output +	16, 18	21
50	Output common -	1-16	Z
46	D/A signal +	18	7
45	D/A signal -	18	9
48	Signal return	(Pin 50 of J4 through 1 MΩ resistor)	
49	Power return	(Pin 42 of J4)	
42	Shield	(Pin 49 of J4)	

Note: Twisted pair used for D/A signals in cable going from J4 to A/D.

Table B-4 Conditioner Card Socket (Sockets 1-16) Pin Identification

Sockets 1-16		
Pin	Signal	Destination
7	Input +	J1
9	Input -	J1
11	+15 Vdc	(Power supply)
M	+15 Vdc	(Power supply)
12	Power Common	(Power supply)
N	Power Common	(Power supply)
14	-15 Vdc	(Power supply)
R	-15 Vdc	(Power supply)
17	Output +	S17 (Summation card)
V	Output -	S17 (Summation card)
19	Output +	J2 (Chart recorder)
X	Output -	J2 (Chart recorder)
	Output shield	J2 (Chart recorder)
21	Output +	J4 (A/D)
Z	Output -	J4 (A/D)
	Output shield	

Table B-5 Summation Card Socket (Socket 17)
Pin Identification

Socket 17		Destination	
Pin	Signal	Socket/Conn Pin	
1	Channel 1 output +	S1	17
A	Channel 1 output -	S1	V
2	Channel 2 output +	S2	17
B	Channel 2 output -	S2	V
3	Channel 3 output +	S3	17
C	Channel 3 output -	S3	V
4	Channel 4 output +	S4	17
D	Channel 4 output -	S4	V
5	Channel 5 output +	S5	17
E	Channel 5 output -	S5	V
6	Channel 6 output +	S6	17
F	Channel 6 output -	S6	V
8	Channel 7 output +	S7	17
H	Channel 7 output -	S7	V
K	Channel 8 output +	S8	17
J	Channel 8 output -	S8	V
10	Channel 9 output +	S9	17
L	Channel 9 output -	S9	V
11	+15 Vdc	(Power supply)	
M	+15 Vdc	(Power supply)	
12	Power common	(Power supply)	
N	Power common	(Power supply)	
14	-15 Vdc	(Power supply)	
R	-15 Vdc	(Power supply)	
15	Channel 10 output +	S10	17
S	Channel 10 output -	S10	V
16	Channel 11 output +	S11	17
T	Channel 11 output -	S11	V
17	Channel 12 output +	S12	17
U	Channel 12 output -	S12	V
18	Channel 13 output +	S13	17
V	Channel 13 output -	S13	V
19	Output +	J2	AA
X	Output -	J2	BB
	Output shield	J2	CC
20	Channel 14 output +	S14	17
W	Channel 14 output -	S14	V
21	Channel 15 output +	S15	17
Y	Channel 15 output -	S15	V
22	Channel 16 output +	S16	17
Z	Channel 16 output -	S16	V

Table B-6 Calibration Card Socket (Socket 18)
Pin Identification

Socket 18		Destination	
Pin	Signal	Connector	Pin
1	Calibration +	J1	AA
A	Calibration -	J1	BB
2	Spare channel signal +	J1	DD
B	Spare channel signal -	J1	EE
7	D/A signal +	J2	46
9	D/A signal -	J2	45
11	+15 Vdc	(Power supply)	
M	+15 Vdc	(Power supply)	
12	Power common	(Power supply)	
N	Power common	(Power supply)	
14	-15 Vdc	(Power supply)	
R	-15 Vdc	(Power supply)	
19	Output +	J2	DD
X	Output -	J2	EE
	Output shield	J2	MM
21	Output + (A/D Ch 16+)	J4	26
Z	Output - (A/D Ch 16-)	J4	50
	Output shield		

Appendix C

Signal Conditioner Circuit Board Details

Figure C-1 contains the schematic diagram of the signal conditioner circuit card.

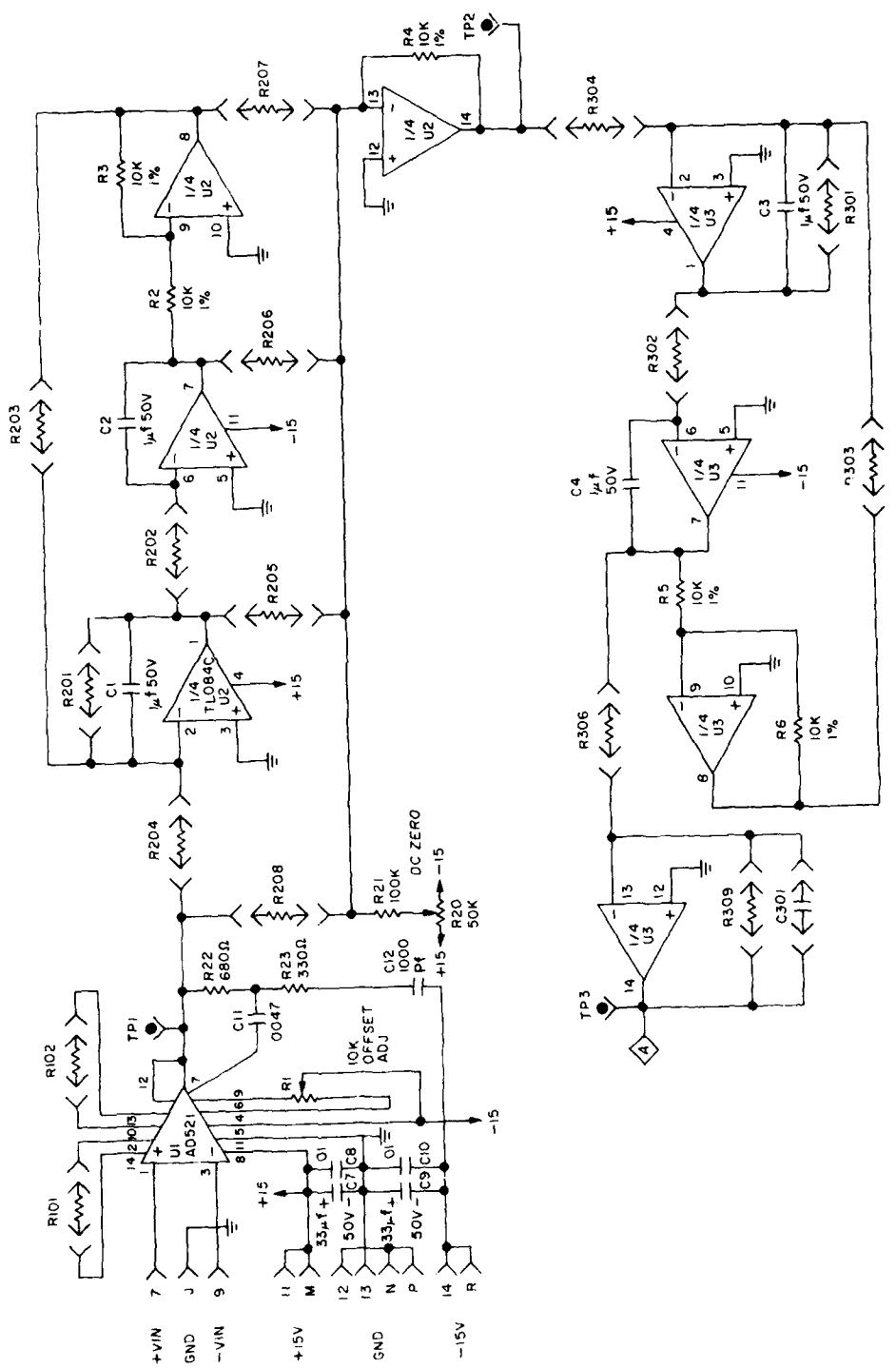
Amplifier U1; together with R1, R22, R23, C11, and C12; makes up stage 1 of the conditioning card. Stage gain is set by the values of R101 and R102 which plug into socket XR1 (see Figure C-2). C11, C12, R22, and R23 make up a compensation network to prevent high-frequency oscillation. R1 allows for nulling of the stage dc input offset voltage.

Stage 2, a universal biquad filter, is made up of U2 and associated components. R2, R3, R4, R20, R21, C1, and C2 are soldered to the board. R20 and 21 allow dc offset adjustment for the entire card. The dc value set by the wiper on R20 is added to the filter output and amplified by the rest of the card. R201-R208 are mounted on component carriers and plug into socket XR2.

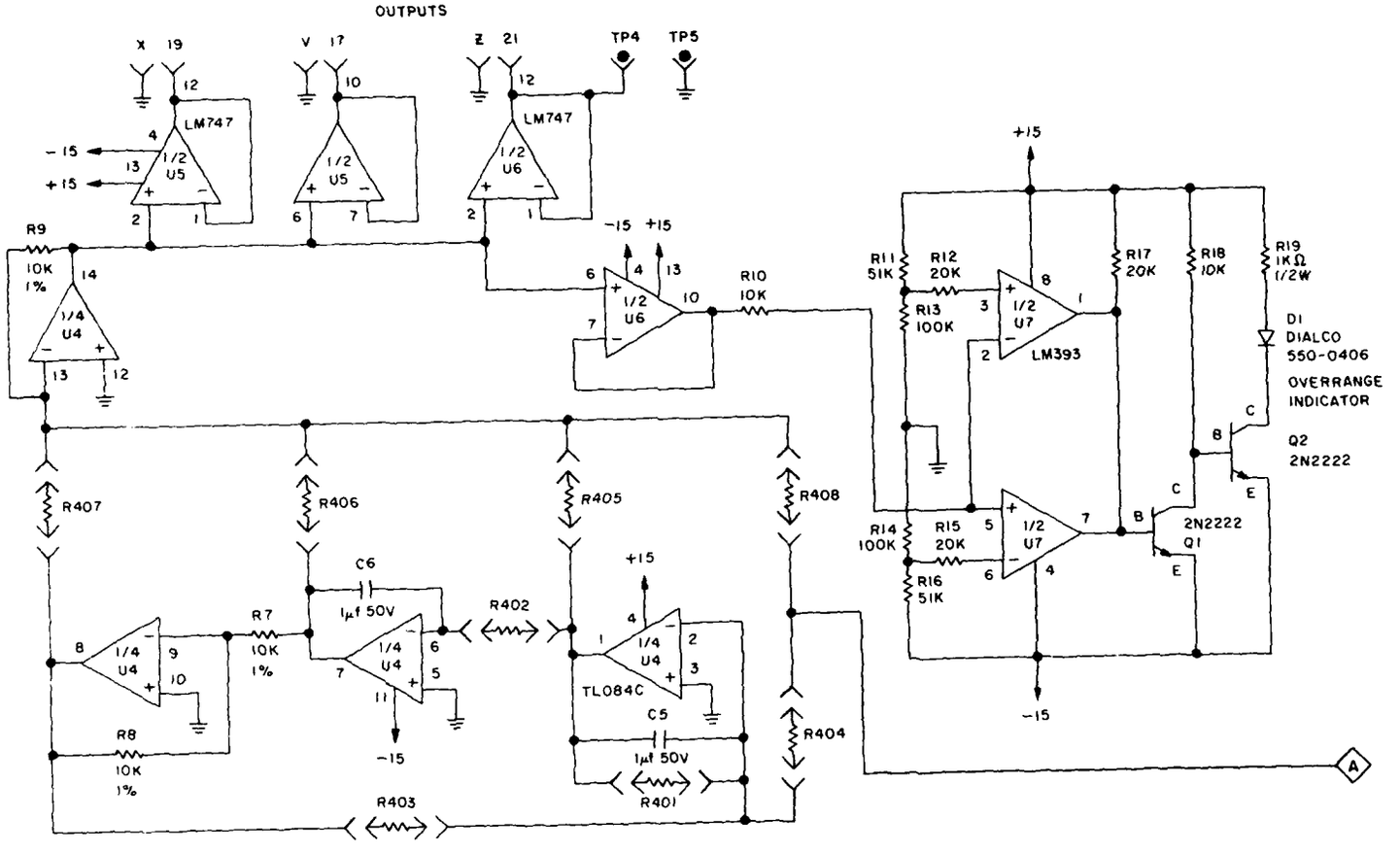
Three of the four sections of U3 make up stage 3, a biquad lowpass filter. R5, R6, C3, and C4 are soldered to the circuit board. Extra solder pads have been provided in parallel with C3 and C4 to allow addition of capacitors to lower the frequency range of the stage. R301-R304 are mounted on component carriers and plug into socket XR3.

The fourth section of operational amplifier U3 is used to form stage 4 of the signal conditioning card chain. Its characteristics are set by R306, R309, and C301, which plug into socket XR3.

The four sections of U4 are used to make up stage 5, a universal biquad filter. R7-R9, C5, and C6 are soldered to the board. R401-R408 plug into socket XF4.



C-1. Signal Conditioner Circuit Board Schematic

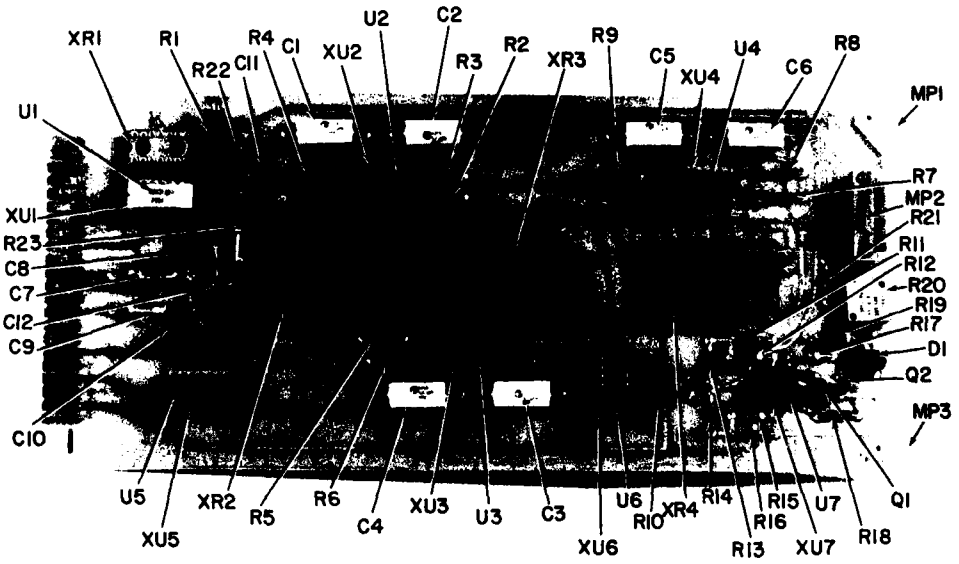


C-1. Signal Conditioner Circuit Board Schematic (Cont.)

Unity-gain buffers for the board outputs are provided by U5 and U6. Half of U6 is used to buffer the input to the overrange sensing circuit.

Dual comparator U7 and associated components make up the overrange sensing circuit. U7 is set up as a window comparator with a range of approximately +10 to -10 Vdc set by R11-R16. When the input voltage is outside the window, Q1 and Q2 turn on the overrange indicator D1.

Figure C-2 gives the location of all parts permanently attached to the circuit card. Table C-1 contains a complete parts list of these fixed parts. Part identifiers refer to the annotations on Figure C-2.



C-2. Signal Conditioner Circuit Board Component Locations

Table C-1 Signal Conditioner Card Parts List

Part	Noun	Mfgr Part No.	Manufacturer
XU1-XU6, XR1	Low profile DIP IC socket, 14 pin	514-AG10D	Augat
XU7	Low profile DIP IC socket, 8 pin	508-AG10D	Augat
XR2-XR4	Low profile DIP IC socket, 32 pin	532-AG10D	Augat
MP1, MP3	Card ejector	CP-06PC	Waldom
MP2	Test Point Connector	500SR5	Dale
R1	Trimpot, 10K Ω, 1 W, 10%, wirewound	3057P	Bourns
R2-R10	Resistor, 10K Ω, 1/4 W, 1%, cermet film	CCH	Allen-Bradley
R11, R16	Resistor, 51K Ω, 1/4 W, 2%, metal film	C4	Corning
R12, R15, R17	Resistor, 20K Ω, 1/4 W, 2%, metal film	C4	Corning
R13, R14	Resistor, 100K Ω, 1/4 W, 2%, metal film	C4	Corning
R18	Resistor, 10K Ω, 1/4 W, 2%, metal film	C4	Corning
R19	Resistor, 1K Ω, 1/2 W, 2%, metal film	C5	Corning
R20	Trimpot, 50K Ω, 1/2 W, 10%, cermet film	66PR50KWK	Beckman
R21	Resistor, 100K Ω, 1/4 W, 1%, cermet film	CCH	Allen-Bradley
R22	Resistor, 680 Ω, 1/4 W, 2%, metal film	C4	Corning
R23	Resistor, 330 Ω, 1/4 W, 2%, metal film	C4	Corning
C1-C6	Capacitor, 1 μF, 50 V, 5%, polycarbonate	625B-1-A-105-J	Electrocube
C7, C9	Capacitor, 33 μF, 50 V, tantalum	336M050P1B	Mallory
C8, C10	Capacitor, 0.01 μF, 200 V	CKR06	AVX
C11	Capacitor, 0.0047 μF, 100 V, 10%, polyester	601PE	TRW
C12	Capacitor, 1000 pF, 500 V, 2%, mica	CM06F102G03	Arco
Q1, Q2	Transistor	2N2222	TI
D1	Indicator, LED, red	550-0406	Dialco
U1	Instrumentation amplifier	AD521K	Analog Devices
U2-U4	Operational amplifier, quad, Bi-FET	TL084CN	TI
U5, U6	Operational amplifier, dual	LM747EN	Nat'l Semic.
U7	Comparator, dual	LM393AN	Nat'l Semic.

Appendix D

Biquadratic Filter Theory

D.1 GENERAL BIQUADRATIC FILTER THEORY

D.1.1 BACKGROUND

Biquadratic (biquad) active filters are an outgrowth of using an analog computer to model system transfer functions. Tow (1969a)[4] reported on the circuit used here. His circuit uses resistors, capacitors, and differential input operational amplifiers in a configuration that could provide any second order transfer function.

Tow (1969b)[5] and Thomas (1971a and 1971b)[6,7] further analyzed the circuit. They reported that the circuit possessed low sensitivities to both the active and passive components (that is, any changes in the gain of the amplifiers or the values of the passive components

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4. Tow, J. (1969a) Design formulas for active RC filters using operational-amplifier biquad, Electronic Letters, 5 (No. 15):339-341

5. Tow, J. (1969b) A step-by-step active filter design, IEEE Spectrum, 6 (Dec 69):64-68

6. Thomas, L.C. (1971a) The biquad: part I - some practical design considerations, IEEE Transactions on Circuit Theory, CT-18 (No. 3):350-357

7. Thomas, L.C. (1971b) The biquad: part II - a multipurpose active filtering system, IEEE Transactions on Circuit Theory, CT-18 (No. 3):358-361

are not magnified by the circuit). Further, they reported that the circuit was unconditionally stable (wouldn't oscillate), had a low output impedance, and a high purely resistive input impedance.

The work reported in this section is an extension of that reported in Tow (1969b). In that paper, the basic design and analysis equations for the biquad were presented. These have been reworked to break out the specific parameter terms so that the transfer function can be derived more readily.

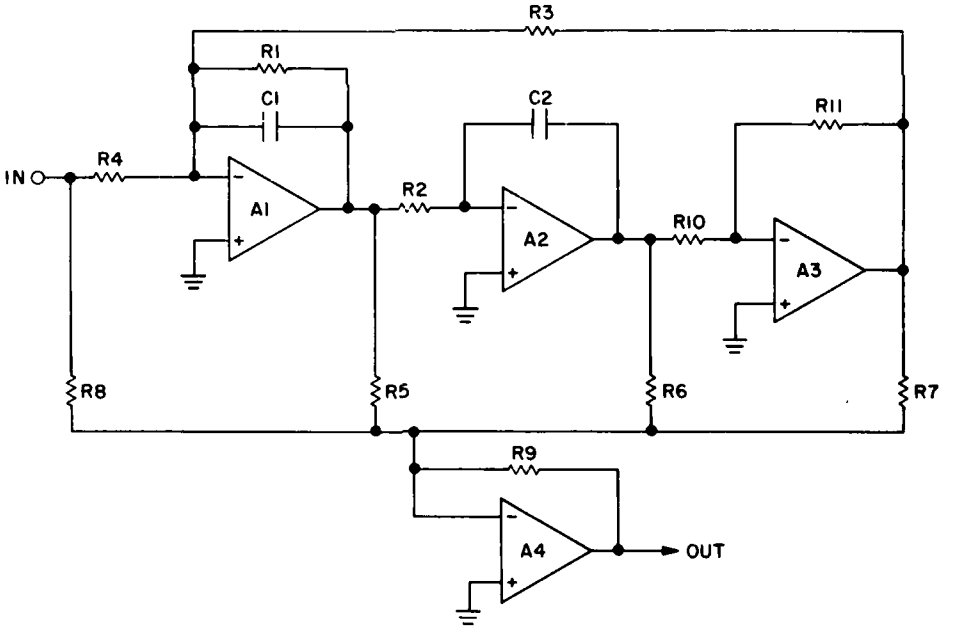
D.1.2 GENERAL BIQUAD CIRCUIT DESCRIPTION

Figure D-1 gives the general schematic of a biquadratic active filter section. The transfer function for this circuit can be given by

$$H(S) = \frac{V_{out}(S)}{V_{in}(S)} = \frac{mS^2 + cS + d}{S^2 + aS + b} \qquad (1)$$

where

S is complex frequency. ($S = \sigma + j\omega$, where σ = logarithmic rate of growth/decline in nepers/sec and ω is angular frequency in radians/sec.)



D-1. General Biquadratic Filter Schematic

The values of the coefficients (m,a,b,c,ω) in Eq. [1] determine the frequency response of the filter represented by this equation. These coefficients, in turn, are determined by the values of the passive components (R1-R11, C1, C2) used in the circuit. By appropriate selection of these components, a number of different second-order active filters (lowpass, bandpass, highpass, allpass, or band reject) can be constructed from the general circuit. Further, if the values of these components are known, the circuit transfer function can be derived directly. Thus, for the use of a biquadratic active filter, two sets of equations (synthesis and analysis) are required for each type of filter (lowpass, etc.). The following sections give these design equations.

Since the signal conditioning cards are designed for low frequency use (under 500 Hz), several simplifying assumptions have been made in deriving these equations. First, ideal operational amplifiers have been assumed. Second, no parasitic reactances have been considered, since these most often affect RF circuits. Third, the effects of amplifier frequency response limitations are ignored.

D.2 BIQUAD LOWPASS FILTER DESIGN EQUATIONS

The general second order lowpass filter equation is

$$H(s) = \frac{m}{S^2 + (\xi p)(\omega p)S + \omega p^2} \qquad (2)$$

where

ωp is the cutoff or pole frequency (in radians/sec)

ξp is the damping coefficient.

D.2.1 LOWPASS SYNTHESIS EQUATIONS

Given a desired filter gain at frequencies well below cutoff (Adc) in volts/volt, a desired ωp, and a desired ξp as illustrated in Figure D-2, the following equations apply. (Resistor values are in ohms, capacitor values in farads, k1 is a scaling constant [typically = 1].) (R5, R7, and R8 are not used.)

$$R1 = \frac{1}{2(\xi p)(\omega p)(C1)} \qquad (3)$$

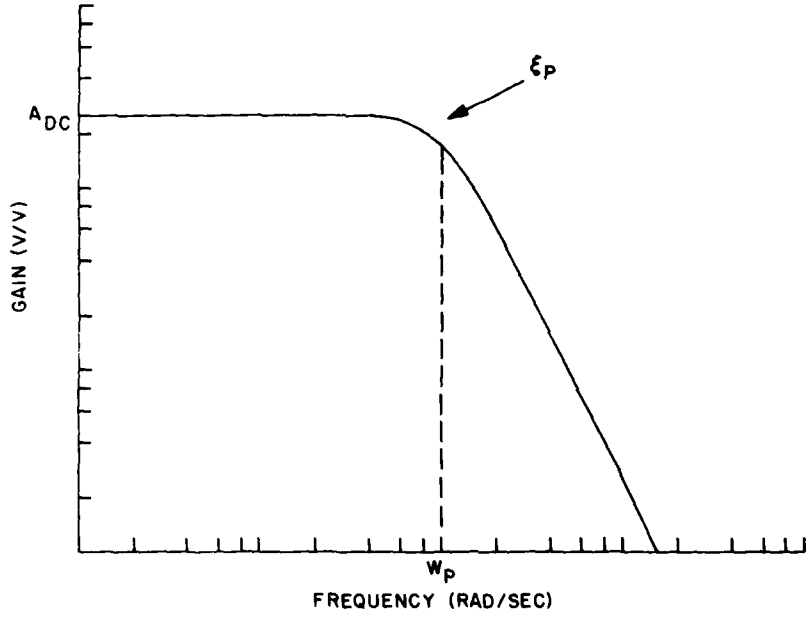
$$R2 = \frac{k1}{(\omega p)(C2)} \tag{4}$$

$$R3 = \frac{1}{(k1)(\omega p)(C1)} \tag{5}$$

$$R4 = \frac{1}{(k1)(\omega p)(C1)(\sqrt{Adc})} \tag{6}$$

$$R6 = \frac{R9}{\sqrt{Adc}} \tag{7}$$

$$R10 = R11 \tag{8}$$



D-2. Biquadratic Lowpass Filter Frequency Response

D.2.2 LOWPASS ANALYSIS EQUATIONS

Given the values of R's and C's actually used in the lowpass filter design, the following equations give the gain at frequencies well below cutoff (Adc), the actual ωp, and the actual ξp. (Resistor values are given in ohms, capacitor values in farads.)

$$\text{Adc (V/V)} = \frac{-(R3)(R9)(R10)}{(R4)(R6)(R11)} \tag{9}$$

$$\omega p \text{ (rad/sec)} = \sqrt{\frac{R11}{(R2)(R3)(R10)(C1)(C2)}} \tag{10}$$

$$\xi p = \frac{1}{2(R1)} \sqrt{\frac{(R2)(R3)(R10)(C2)}{(C1)(R11)}} \tag{11}$$

D.3 BIQUAD BANDPASS FILTER DESIGN EQUATIONS

The general second order bandpass equation, as can be implemented in a single biquad section, is

$$H(S) = \frac{mS}{S^2 + (\xi p)(\omega p)S + \omega p^2} \tag{12}$$

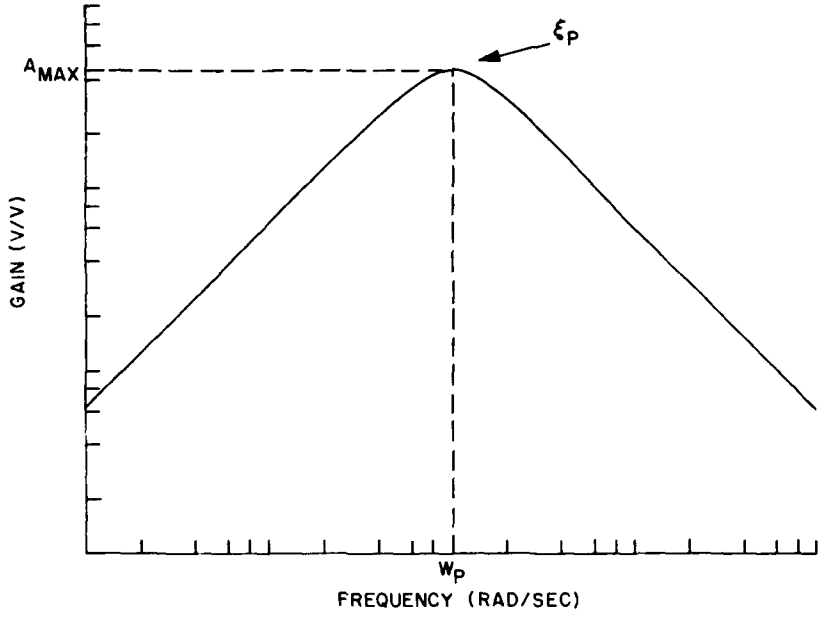
where

ωp is the center frequency of the bandpass (in radians/sec)

ξp is the damping coefficient.

D.3.1 BANDPASS SYNTHESIS EQUATIONS

Given a desired filter gain at center frequency (Amax) in volts/volt, a desired ωp, a desired ξp (see Figure D-3), Eqs. [3], [4], [5], and [8], in addition to the following equations, apply. (Resistor values are in ohms, capacitor values in farads.) (R6, R7, and R8 are not used.)



D-3. Biquadratic Bandpass Filter Frequency Response

$$R4 = \frac{1}{2(\omega p)(\xi p + 1)(C1)\sqrt{Amax}} \tag{13}$$

$$R5 = \frac{R9}{\sqrt{Amax}} \tag{14}$$

D.3.2 BANDPASS ANALYSIS EQUATIONS

Given the values of R's and C's actually used in the bandpass filter design, Eqs. [10] and [11], in addition to the following equations, give the gain at the actual ωp (Amax), the actual ωp, and the actual ξp. (Resistor values are in ohms, capacitor values in farads.) Note: Should filter requirements be defined in terms of selectivity (Q) or bandwidth (BW), $\xi p = 1/Q = BW/\omega p$.

$$RT = (R2)(R3)(R10)(R11)(C1)(C2) \tag{15}$$

$$\text{Amax (V/V)} = \frac{(R1)(R9)}{(R4)(R5)} \quad \frac{\sqrt{RT}}{2(R1)(R11)(C1) + \sqrt{RT}} \tag{16}$$

D.4 BIQUAD HIGHPASS FILTER DESIGN EQUATIONS

The general second order highpass filter design equation is

$$H(S) = \frac{-mS^2}{S^2 + (\xi p)(\omega p)S + \omega p^2} \tag{17}$$

where

ωp is the cutoff frequency (in radians/sec)

ξp is the damping coefficient.

D.4.1 HIGHPASS SYNTHESIS EQUATIONS

Given a desired filter gain at frequencies much above cutoff (Ah) in volts/volt, a desired ωp, and a desired ξp (see Figure D-4), Eqs. [3], [4], [5], and [8], in addition to the following design equations, apply. (Resistor values are in ohms, capacitor values in farads, k1 and k2 are scaling constants [typically = 1].) (R6 is not used.)

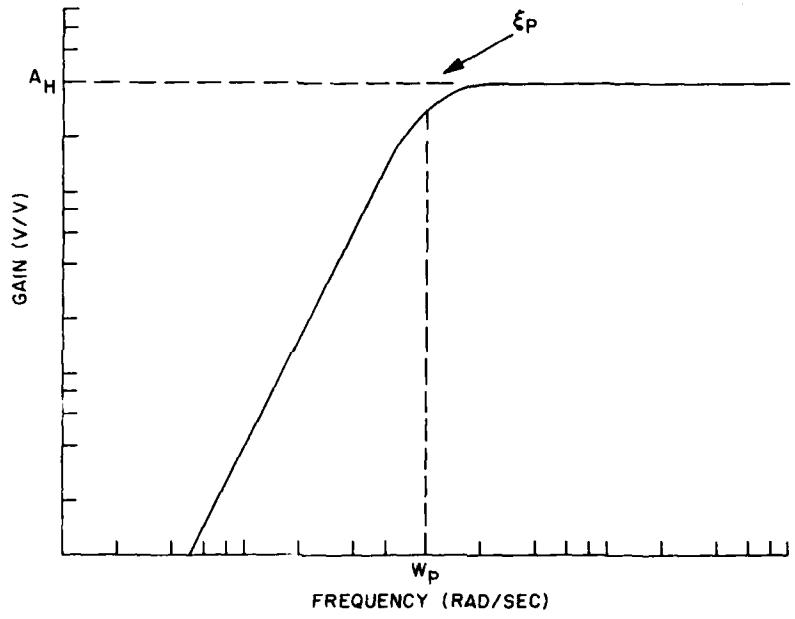
$$R4 = \frac{1}{2(k2)(Ah)(\xi p)(\omega p)(C1)} \tag{18}$$

$$R5 = R9 \tag{19}$$

$$R7 = \frac{2(k2)(\xi p)(R9)}{k1} \tag{20}$$

$$R8 = \frac{R10}{Ah} \qquad (21)$$

Note: Low frequency performance degradation can result if actual resistor values are not carefully chosen. See the following section for a discussion of these effects.



D-4. Biquadratic Highpass Filter Frequency Response

D.4.2 HIGHPASS ANALYSIS EQUATIONS

Although Eq. [17] models an ideal highpass filter, an actual filter constructed using a biquad active filter stage may not have an ideal frequency response. Such a response comes from values of components which differ slightly from the ideal values given in the above equations. Thus, the actual highpass filter is modeled by

$$H(S) = \frac{-m\left(S^2 + (\xi z)(\omega z)S + \omega z^2\right)}{S^2 + (\xi p)(\omega p)S + \omega p^2} \qquad (22)$$

where

ξp and ωp are defined as in Eq. [17]

ωz is the zero frequency (in radians/sec)

ξz is the zero damping coefficient.

It should be noted that, for actual component values close to those derived in Section D.4.1, ωz and ξz are close to zero. Also, Eq. [22] assumes an ideal high frequency response for the filter (i.e. gain of m at ω of infinity). The actual filter response is limited to several MHz by the high frequency response of the amplifiers as well as by parasitic capacitances and inductances. However, these effects occur at frequencies orders of magnitude higher than those for which the SDAS filters are designed and hence are ignored here.

The presence of these ωz and ξz terms shows up as a degradation in the low frequency rejection of the filter. This degradation can be minimized by adjustment of certain resistor values as described below.

Given the actual values of R's (in ohms) and C's (in farads) used in a circuit, Eqs. [10] and [11], in addition to the following equations, derive values for the above parameters as well as for the actual filter gain at frequencies much above ωp (Ah).

$$Ah\ (V/V) = \frac{-R9}{R8} \qquad (23)$$

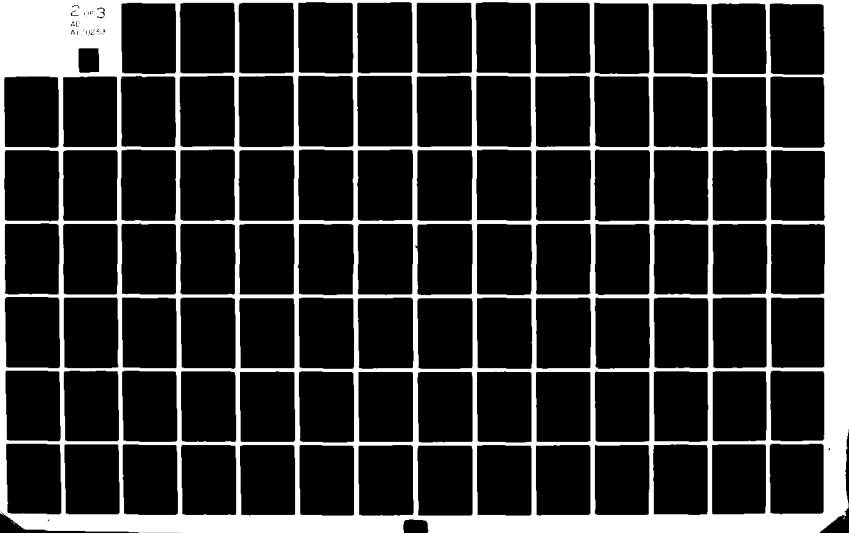
$$\omega z\ (rad/sec) = \omega p \sqrt{1 - \frac{(R3)(R8)}{(R4)(R7)}} \qquad (24)$$

$$\xi z = \frac{1}{2(\omega z)(R1)(C1)} \left(1 - \frac{(R1)(R8)}{(R4)(R5)}\right) \qquad (25)$$

As can be seen from the above, changes in R7 affect the value of ωz only while changes in R5 effect ξz only; therefore, these resistors can be changed to vary ωz and ξz and thus "tune" a filter's low frequency rejection.

Several effects can show up in the filter's response, depending on the value of these resistors. Specifically, in Eq. [24], if (due

AD-A100 253 AIR FORCE GEOPHYSICS LAB HANSCOM AFB MA F/G 9/3
THE AIR FORCE GEOPHYSICS LABORATORY STANDALONE DATA ACQUISITION--ETC(U)
OCT 80 P G VON GLAHN
UNCLASSIFIED AFGL-TR-80-0317 NL



to the resistors used) the product (R3)(R8) is greater than (R4)(R7), a negative value exists under the square root. Although this negative value implies an imaginary ωz, its presence shows up in actual circuit operation as a real degradation in low frequency rejection of the filter. Further, in Eq. [24], note that as the product (R3)(R8) approaches (R4)(R7), ωz approaches zero and, consequently, the filter's response approaches that of an ideal highpass filter. Therefore, the value used for R7 should be selected to insure that (R3)(R8) is equal to or slightly greater than (R4)(R7) to insure optimum low frequency rejection.

Another effect shows up in Eq. [25]. In this equation, a value of the product (R1)(R8) greater than the product (R4)(R5) will result in a negative value of ξz. This, in turn, can be observed as a change in low frequency phase response. This change can be reduced or eliminated by careful selection of R5. Thus, to insure optimum low frequency rejection, the values of R5 and R7 used in actual filters should be carefully selected to avoid the possible degradation modes discussed above.

D.5 BIQUAD ALLPASS FILTER DESIGN EQUATIONS

The allpass filter, or delay equalizer, can be described by

$$H(S) = \frac{-\left(S^2 - 2(\omega o/B)S + \omega o^2\right)}{S^2 + 2(\omega o/B)S + \omega o^2} \qquad (26)$$

where

ωo is the critical frequency (in radians/sec)

B is the stiffness ratio.

The ideal allpass filter passes all frequencies with unchanged amplitude but with a frequency-dependent delay. (See Daniels[8] for a good discussion of the allpass filter characteristics. This section uses his notation for the stiffness ratio.)

D.5.1 ALLPASS SYNTHESIS EQUATIONS

Given a desired ωo and B, Eq. [8], in addition to the following design equations, apply for the allpass filter. (Resistor values are in ohms, capacitor values in farads, k1 and k2 are scaling constants [typically = 1].) (R6 and R7 are not used.)

---

8. Daniels, R.W. (1974) Approximation Methods for Electronic Filter Design, McGraw Hill, New York, Chapter 14

$$R1 = \frac{B}{2(\omega o)(C1)} \tag{27}$$

$$R2 = \frac{k1}{(\omega o)(C2)} \tag{28}$$

$$R3 = \frac{1}{(k1)(\omega o)(C1)} \tag{29}$$

$$R4 = \frac{B}{4(k2)(\omega o)(C1)} \tag{30}$$

$$R5 = (k2)(R9) \tag{31}$$

$$R8 = R9 \tag{32}$$

D.5.2 ALLPASS ANALYSIS EQUATIONS

Although Eq. [26] models an ideal allpass filter, an actual filter constructed using a biquad active filter stage may not have an ideal frequency response. Such a non-ideal response comes from using components which differ slightly from the ideal values given in the above equations. Thus, the actual allpass filter is modeled by

$$H(s) = -\frac{\left(S^2 - 2(\omega o/B1)S + \omega o^2\right)}{S^2 + 2(\omega o/B2)S + \omega o^2} \tag{33}$$

where

ωo is the critical frequency (in radians/sec)

B1 and B2 are the numerator and denominator stiffness ratios, respectively.

Given the actual values of R's (in ohms) and C's (in farads) used in constructing the filter, the following equations give the actual values for these parameters.

$$\omega o \text{ (rad/sec)} = \sqrt{\frac{R11}{(R2)(R3)(R10)(C1)(C2)}} \tag{34}$$

$$B2 = 2(R1)\sqrt{\frac{(R11)(C1)}{(R2)(R3)(R10)(C2)}} \tag{35}$$

$$B1 = (B2)\frac{(R4)(R5)}{(R4)(R5) - (R1)(R9)} \tag{36}$$

Note that in Eq. [36], the values of R1, R4, R5, and R9 determine the deviation of the actual from the ideal performance of the filter.

D.6 BIQUAD BAND REJECT FILTER DESIGN EQUATIONS

A band reject filter, as implemented using a biquad filter section, can be modeled by

$$H(S) = \frac{-m\left(S^2 + \omega z^2\right)}{S^2 + 2(\xi p)(\omega p)S + \omega p^2} \tag{37}$$

where

ωz is the zero frequency (in radians/sec)

ωp is the pole frequency (in radians/sec)

ξp is the pole damping coefficient.

The response of this filter is characterized by a notch or gain minimum at ωz and a peak or gain maximum at ωp. Two design cases arise with this filter type: those in which ωp is greater than ωz (case I) and those where ωp is less than ωz (case II).

At first glance, both cases would appear equally usable for a given band reject application. However, this may not be the case. The band reject frequency response is characterized by a minimum gain at

the zero frequency and higher gains on either side. These gains are not identical, however (see Figures D-5 and D-6). The gains at frequencies much above ωz (Ahi) are related to those much below (Alo) by

$$Alo = Ahi \left(\frac{\omega z}{\omega p}\right)^2 \tag{38}$$

where both gains are in volts/volt and ωz and ωp are defined as above. Therefore, if a greater low frequency gain were required, ωz would be specified as higher than ωp (case II).

As ωz approaches ωp, Eq. [38] implies that the two gains become equal. However, as the two approach each other, the value of one of the resistors in the filter grows. (In the limit, where ωz equals ωp, the resistor's value is infinity and the frequency response curve changes to that of an allpass filter.) Thus, the growth of the resistor value puts a limit on the closeness of ωz to ωp.

Another difference between the cases relates to the shape of the frequency response curve in the vicinity of ωz. Only the shape of the curve closest to ωp can be effected by changing filter parameters (specifically ξp). The other limb of the curve is fixed by the requirement of having ξz equal to zero. Therefore, if a specific response is required on one side of ωz, it can be achieved by selection of ωp to be on that side of ωz.

Finally, another difference between the cases arises from the relationship between filter frequency and component size. Since resistor/capacitor size is inversely proportional to frequency, smaller valued components will result if ωp is specified as higher than ωz.

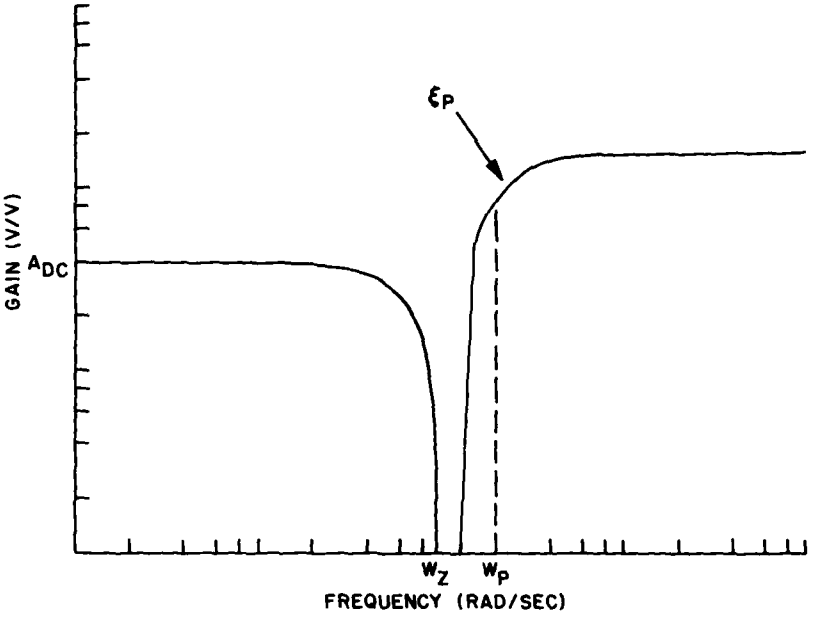
Design and analysis equations for both these two cases are given in the following sections.

D.6.1 CASE I BAND REJECT FILTER

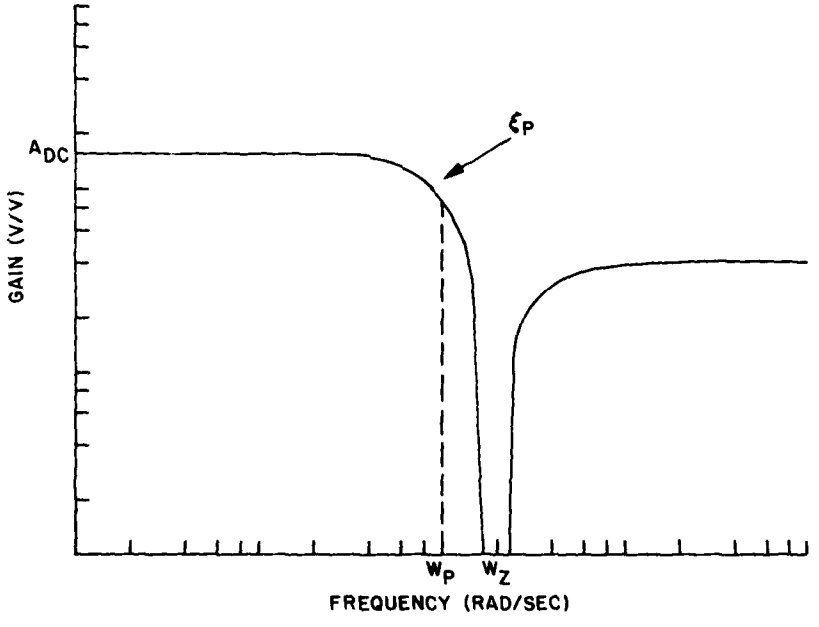
D.6.1.1 Case I Band Reject Synthesis Equations

Given desired values for ωz, ωp, ξp, and the desired filter gain at frequencies much below cutoff (Adc) in volts/volt (see Figure D-5),Eqs. [3], [4], [5], [8], and [31], in addition to the following design equations, apply. (Resistors values are given in ohms, capacitors in farads, k1 and k2 are scaling constants [typically = 1.]) (R6 is not used.)

$$R4 = \frac{\omega z^2}{2(k2)(\omega p^3)(\xi p)(C1)(Adc)} \tag{39}$$



D-5. Biquadratic Case I Band Reject Filter Frequency Response



D-6. Biquadratic Case II Band Reject Filter Frequency Response

$$R7 = \frac{2(k2)(\omega p^2)(\xi p)(R9)}{(k1)(\omega z^2)\left|\frac{\omega p^2}{\omega z^2} - 1\right|} \quad (40)$$

$$R8 = \frac{(\omega z^2)(R10)}{(\omega p^2)(Adc)} \quad (41)$$

Note: Severe performance degradation can result if actual resistor values used are not carefully chosen. See the following section for a discussion of the selection criteria.

D.6.1.2 Case I Band Reject Analysis Equations

Although Eq. [37] models an ideal band rejection filter, an actual filter constructed using a biquad active filter stage may have a frequency response that differs from the ideal. Such a response comes from from using resistor values that differ from those derived in the above equations. Thus, actual filter response is modeled by Eq. [22]. The presence of a nonzero ξz term in Eq. [22] results in a degradation of the filter's frequency rejection at the zero frequency. Given actual values of R's (in ohms) and C's (in farads), Eqs. [10], [11], [24], and [25], in addition to the following equations, give actual values for the above parameters as well as for Adc and for the maximum gain at ωp (Amax):

$$Adc\ (volts/volts) = \frac{-R9}{R8}\left(1 - \frac{(R3)(R8)}{(R4)(R7)}\right) \quad (42)$$

$$RT = \sqrt{\frac{(R2)(R3)(R10)(C2)}{(R1^2)(R11)(C1)}} \quad (43)$$

$$Amax\ (volts/volt) = \frac{-R9}{R8}\left(\frac{2 - \left(\frac{(R3)(R8)}{(R4)(R7)}\right) + \left(1 - \frac{(R1)(R8)}{(R4)(R5)}\right) RT}{2 + RT}\right) \quad (44)$$

As can be seen from the above equations, changes in R7 affect the value of ωz and Amax only, while changes in R5 effect ξz and Amax only; therefore, these resistor values can be changed to "tune" the filter's response. Several effects can show up in the filter's response, depending on the value of these resistors. Specifically, in Eq. [24], if the product (R3)(R8) is greater than (R4)(R7), a negative value exists under the square root. This shows up in circuit performace as a complete elimination of the gain minimum or notch at ωz. Therefore, the value used for R7 should be selected to insure

that (R3)(R8) is greater than (R4)(R7) to insure proper frequency rejection.

Another effect shows up in Eq. [25]. In this equation, a value of the product (R1)(R8) greater than the product (R4)(R5) will result in a negative value of ξz. This, in turn, can be observed in the filter's response as a phase change in the vicinity of ωz. This change can be reduced or eliminated by careful selection of R5. Thus, to insure proper frequency rejection and phase, the values of R5 and R7 used in actual filters should be carefully selected to avoid the possible degradation modes discussed above.

D.6.2 CASE II BAND REJECT FILTER

D.6.2.1 Case II Band Reject Synthesis Equations

Given desired values for ωz, ωp, ξp, and the desired filter gain at frequencies much below cutoff (Adc) in volts/volt (see Figure D-6), Eqs. [3], [4], [5], [8], [31], [39], and [41], in addition to the following design equation, apply. (Resistors values are given in ohms, capacitors in farads, k1 and k2 are scaling constants [typically = 1.])

$$R6 = \frac{2(k2)(\omega p^2)(\xi p)(R9)}{(k1)(\omega z^2)\left|\frac{\omega p^2}{\omega z^2} - 1\right|} \tag{45}$$

Note: Filter performance changes can result if actual resistor values used are not carefully chosen. See the following section for a discussion of the selection criteria.

D.6.2.2 Case II Band Reject Analysis Equations

Although Eq. [37] models an ideal band rejection filter, an actual filter constructed using a biquad active filter stage may have a frequency response that differs from the ideal. This comes from using resistor values in the actual filter that differ from those derived in the above equations. Thus, actual filter response is modeled by Eq. [22]. The presence of a nonzero ξz term in Eq. [22] results in a degradation of the filter's frequency rejection at the zero frequency. Given actual values of R's (in ohms) and C's (in farads), Eqs. [10], [11], [25], and [43], in addition to the following equations, give actual values for the above parameters as well as for Adc and for the maximum gain at ωp (Amax):

$$\text{Adc (volts/volt)} = \frac{-R9}{R8}\left(1 + \frac{(R3)(R8)(R10)}{(R4)(R6)(R11)}\right) \tag{46}$$

$$\text{Amax (volts/volt)} = \frac{-R9}{R8}\left(\frac{2+\left(\frac{(R3)(R8)(R10)}{(R4)(R6)(R11)}\right)+\left(1-\frac{(R1)(R8)}{(R4)(R5)}\right)RT}{2+RT}\right) \tag{47}$$

$$\omega z\ (\text{rad/sec}) = \sqrt{\omega p^2\left(1+\frac{(R3)(R8)(R10)}{(R4)(R6)(R11)}\right)} \tag{48}$$

As can be seen from the above, a change in R5 effects ξz and Amax only; therefore, this resistor value can be changed to "tune" the filter's response. This effect shows up in Eq. [25]. In this equation, a value of the product (R1)(R8) greater than the product (R4)(R5) will result in a negative value of ξz. This, in turn, can be observed in the filter's response as a phase change in the vicinity of ωz. This change can be reduced or eliminated by careful selection of R5. Thus, to insure proper frequency rejection and phase, the values of R5 used in actual filters should be carefully selected.

Appendix E

Sample Signal Conditioning Circuit Card Designs

E.1 APPENDIX OVERVIEW

This appendix documents two sample signal conditioning card design sessions using programs FILTER and FCHECK. It is intended to aid users of these programs in understanding their operation. The sample conditioning card configurations selected are typical of those used in actual data acquisition environments. No attempt has been made to demonstrate every card configuration option. Further, the filter parameter distribution among the stages are not necessarily the optimum to achieve the desired overall performance.

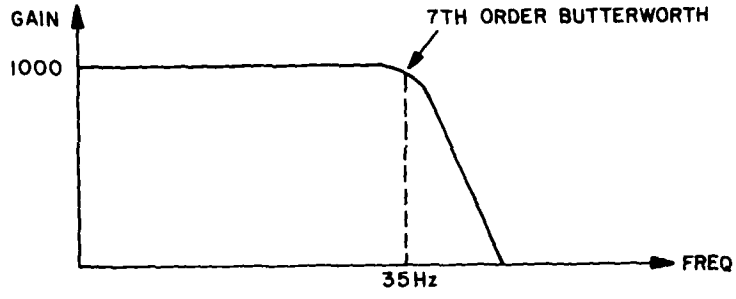
The following sections document these sample configurations. Each contains a signal conditioning card design sheet documenting the desired overall and stage responses. An annotated system console listing follows to document the running of FILTER. The resulting SDAS signal conditioning card resistor value and filter parameters table is also included to document the final board configuration. Next, the component values listed are changed slightly to simulate measured resistor and capacitor values as would be encountered in a actual circuit board. Program FCHECK is run next to determine the actual filter parameters resulting from using the "measured" component values. The annotated console listings and component/parameter table resulting are included to round out the section.

E.2 EXAMPLE 1

This example results in the design of a simple multistage lowpass filter conditioning card with a dc gain of 1000. Figure E-1 contains the signal conditioning card design sheet documenting the desired

DATE: _____ CHANNEL NO: _____

TOTAL RESPONSE DESIRED:



STAGE 1: GAIN ONLY

STAGE GAIN: 10.0 (V/V)
POLE FREQUENCY: 670.0 (HZ)

STAGE 2: FILTER TYPE: GAIN (LP) BP HP BR

ADDED CAPACITOR VALUE: — (UFD)
STAGE GAIN: 5.0 (V/V)
ZERO FREQUENCY: — (HZ) ZERO DAMPING COEFF: —
POLE FREQUENCY: 35.0 (HZ) POLE DAMPING COEFF: 0.900969

STAGE 3: LOW PASS FILTER ONLY

ADDED CAPACITOR VALUE: — (UFD)
STAGE GAIN: 1.0 (V/V)
POLE FREQUENCY: 35.0 (HZ) POLE DAMPING COEFF: 0.623490

STAGE 4: FILTER TYPE: GAIN (GAIN AND LP)

STAGE GAIN: 10.0 (V/V)
POLE FREQUENCY: 35.0 (HZ)

STAGE 5: FILTER TYPE: GAIN (LP) BP HP BR

ADDED CAPACITOR VALUE: — (UFD)
STAGE GAIN: 2.0 (V/V)
ZERO FREQUENCY: — (HZ) ZERO DAMPING COEFF: —
POLE FREQUENCY: 35.0 (HZ) POLE DAMPING COEFF: 0.222521

E-1. Example 1 Signal Conditioning Circuit Board Design Worksheet

total response and stage type assignments. Note that more gain is assigned to stages 1 and 3; this results in a smaller spread of resistor values in the active filters in the other stages. The pole damping coefficients were selected to provide a seventh-order Butterworth rolloff at a cutoff frequency of 35 Hz.

Program FILTER is next run to calculate the required component values. Table E-1 contains the system console transactions necessary to design this circuit card. Several mistakes have been intentionally added to illustrate error recovery procedures. Prompts and responses issued by the program are underlined. Table E-2 gives the SDAS signal conditioning card resistor value and filter parameters printout resulting from the session given in Table E-1.

In a real situation, the signal conditioning card would next be constructed and used to acquire data. The resistors and capacitors plugged in to the circuit would be measured and their values recorded for later use in program FCHECK. To simulate this, the values determined in the above listings are changed at random by less than 5%. These values are entered into program FCHECK in Table E-3, together with a few intentional errors, again to show error recovery. Table E-4 contains the parameter printout resulting from the session.

E.3 EXAMPLE 2

This example results in the design of a notch and lowpass filter card with a dc gain of 1000. Figure E-2 contains the signal conditioning card design sheet documenting the desired total response and stage type assignments. Note that more gain is assigned to stages 1 and 3; this results in a smaller spread of resistor values in the active filters in the other stages. Also, note that an additional 1.0 μF capacitor has been paralleled with the existing capacitor in stage 5. The pole damping coefficients used result in a fourth-order Butterworth response for the lower limb of the notch and a third-order Butterworth response for the anti-aliasing filter at 35 Hz. Also note that the total response diagram indicates a lower gain above 1 Hz. This lower gain reflects the high frequency gain reduction discussed in Appendix D, section D-6 and not necessarily a desired response.

Program FILTER is next run to calculate the required component values. Table E-5 contains the system console transactions necessary to design this circuit card. Several mistakes have been intentionally added to illustrate error recovery procedures. Prompts and responses issued by the program are underlined. Table E-6 gives the SDAS signal conditioning card resistor value and filter parameters printout resulting from the session given in Table E-5.

In a real situation, the signal conditioning card would next be constructed and used to acquire data. The resistors and capacitors plugged in to the circuit would be measured and their values recorded for later use in program FCHECK. To simulate this, the values determined in the above listings are changed at random by less than 5 percent. These values are entered into program FCHECK in Table E-7, together with a few intentional errors, again to show error recovery. Table E-8 contains the parameter printout resulting from the session.

Table E-1 Example 1 - FILTER System Console Transactions

```
.RUN FILTER                                          <- Program loaded and executed.

SDAS SIGNAL CONDITIONING CARD DESIGN PROGRAM

 STAGE TO BE DESIGNED (0=ENTIRE BOARD) = ? 0         <- If nonzero stage number entered,
                                                        only that stage is designed.
STAGE 1:
DC GAIN (V/V) = ? 10.

R102 (K OHMS) = ? 100.

R101 =   10.00     KOHMS

 CHECK ACTUAL COMPONENTS (Y/N) ? N                   <- See next stage for effect of replying Y.

POLE FREQ (HZ) = ? 670.                              <- N response not required. If Y response
                                                        not desired, <cr> alone has same effect
STAGE 2:                                                as entering N<cr>.
FILTER TYPE (NONE=0, LP=1, HP=2, BP=3, BR=4)= ? 1

SECOND ORDER LOW PASS FILTER
ADDITIONAL CAPACITORS ADDED (Y/N) ? N

DC GAIN (V/V) = ? 5.

POLE FREQ (HZ), DAMPING COEFF = ? 35.,.900969

R201 =   2.52     KOHMS
R202 =   4.55     KOHMS
R203 =   4.55     KOHMS
R204 =   2.03     KOHMS
R206 =   4.47     KOHMS

RX01 INFLUENCES DAMPING, RX04 / RX06 GAIN
     NOTE: STAGE INVERTS SIGNAL
```

Table E-1 Example 1 FILTER System Console Transactions (contd)

```
CHECK ACTUAL COMPONENTS (Y/N) ? Y

R201    (KOHMS) = ? 2.55

R202    (KOHMS) = ? 4.53

R203    (KOHMS) = ? 4.53

R204    (KOHMS) = ? 2.

R206    (KOHMS) = ? 4.42

ADDITIONAL CAPACITORS ADDED (Y/N)?N

GAIN =    5.124      (V/V)      14.2      (DB)
POLE FREQ (HZ) =    35.1     , DAMPING COEF =  0.888
REPEAT CHECK (Y/N)?N <-- Y response returns to prompt for first resistor value.
STAGE 3:
GAIN CAPABILITY 1/2 OTHER STAGES
SECOND ORDER LOW PASS FILTER
ADDITIONAL CAPACITORS ADDED (Y/N) ? N

DC GAIN (V/V) = ? 1.

POLE FREQ (HZ), DAMPING COEFF = ? 35.,.623490

R301 =    3.65      KOHMS
R302 =    4.55      KOHMS
R303 =    4.55      KOHMS
R304 =    4.55      KOHMS

RX01 INFLUENCES DAMPING, RX04 / RX06 GAIN
     NOTE: STAGE INVERTS SIGNAL

CHECK ACTUAL COMPONENTS (Y/N) ? Y

R301    (KOHMS) = ? 3.65

R302    (KOHMS) = ? 4.53
```

Table E-1 Example 1 FILTER System Console Transactions (contd)

```
R303    (KOHMS) = ? 4.53

R304    (KOHMS) = ? 4.53

ADDITIONAL CAPACITORS ADDED (Y/N)?N

GAIN =    1.000      (V/V)     0.000      (DB)
POLE FREQ (HZ) =    35.1     , DAMPING COEF =   0.621
REPEAT CHECK (Y/N)?N

FOURTH STAGE:
GAIN AND/OR SINGLE LP POLE ONLY
DC GAIN (V/V) = ? 10.

R309 (KOHMS) = ? 10.

R306 =    1.000     KOHMS

 NOTE: STAGE INVERTS SIGNAL

 FILTER FREQ (GAIN ONLY = 0.) (HZ) = ? 350.

C301 (UFD) =  0.45473E-01

 CHECK ACTUAL COMPONENTS (Y/N) ? N

STAGE 5:
FILTER TYPE (NONE=0, LP=1, HP=2, BP=3, BR=4)= ? 2

SECOND ORDER HIGH PASS FILTER
ADDITIONAL CAPACITORS ADDED (Y/N)?N

HI FREQ GAIN (V/V) = ? 2.

POLE FREQ (HZ), DAMPING COEFF = ? 35.,.2

R401 =    11.4      KOHMS
R402 =    4.55      KOHMS
R403 =    4.55      KOHMS
```

Error. Value of 35. should have been entered. Stage redesigned below.

Error. Wrong filter type number. Values must be entered when requested. Stage redesigned below.

Table E-1 Example 1 FILTER System Console Transactions (contd)

```
R404 =    5.68      KOHMS
R405 =    10.0      KOHMS
R407 =    4.00      KOHMS
R408 =    5.00      KOHMS

RX01 / RX05 INFLUENCE DAMPING; RX07 ZERO FREQ; RX08 GAIN
****** FOR PROPER LOW FREQ ATTEN, RX04*RX07 = RX03*RX08
       AND RX01*RX08 > RX04*RX05 ******

     NOTE: STAGE INVERTS SIGNAL

CHECK ACTUAL COMPONENTS  (Y/N) ? N

 ANY CHANGES (Y/N) ? Y

STAGE TO BE CHANGED (1-5) = ? 4

FOURTH STAGE:
GAIN AND/OR SINGLE LP POLE ONLY
DC GAIN (V/V) = ? 10.

R309 (KOHMS) = ? 100.

R306 =    10.00      KOHMS

 NOTE: STAGE INVERTS SIGNAL

 FILTER FREQ (GAIN ONLY = 0.) (HZ) = ? 35.

C301 (UFD) =  0.45473E-01

 CHECK ACTUAL COMPONENTS (Y/N) ? Y

R306 (KOHMS) = ? 10.

R309 (KOHMS) = ? 100.

C301 (UFD) = ? .047
```

Y response redesigns one stage without changing other stages.

Stage 4 redesigned due to error above.

Table E-1 Example 1 *FILTER* System Console Transactions (contd)

```
DC GAIN =   10.00      (V/V)    [  20.0      (DB)]

 NOTE: STAGE INVERTS SIGNAL
POLE FREQ =   33.86      HZ

CHECK AGAIN (Y/N) ? N

 ANY CHANGES (Y/N) ? Y <------------------------------------------
                                                                  |
STAGE TO BE CHANGED (1-5) = ? 5 <---- Stage 5 redesigned due to error above.

STAGE 5:
FILTER TYPE (NONE=0, LP=1, HP=2, BP=3, BR=4)= ? 1

SECOND ORDER LOW PASS FILTER
ADDITIONAL CAPACITORS ADDED (Y/N) ? N

DC GAIN (V/V) = ? 2.

POLE FREQ (HZ), DAMPING COEFF = ? 35.,.222521

R401 =    10.2      KOHMS
R402 =    4.55      KOHMS
R403 =    4.55      KOHMS
R404 =    3.22      KOHMS
R406 =    7.07      KOHMS

RX01 INFLUENCES DAMPING, RX04 / RX06 GAIN
     NOTE: STAGE INVERTS SIGNAL

CHECK ACTUAL COMPONENTS (Y/N) ? Y

R401    (KOHMS) = ? 10.2

R402    (KOHMS) = ? 4.53

R403    (KOHMS) = ? 4.53
```

Table E-1 Example 1 FILTER System Console Transactions (contd)

```
R404    (KOHMS) = ? 3.24

R406    (KOHMS) = ? 7.15

ADDITIONAL CAPACITORS ADDED (Y/N)?N

GAIN =    1.955      (V/V)      5.82      (DB)
POLE FREQ (HZ) =    35.1     , DAMPING COEF =   0.222
REPEAT CHECK (Y/N)?N


 ANY CHANGES (Y/N) ? N

RESISTOR AND PARAMETER PRINTOUT (Y/N) ? Y

PRINTOUT ID (<40 CHAR)?EXAMPLE 1

STORE PARAMETERS ON DISK (Y/N) ? N

RESTART PROGRAM (Y/N) ? N

STOP --
```

Title for printout.

Y response results in parameter storage on disk. See Table E-3 for example of usage.

Y response returns to beginning of program.

Table E-2 Example 1 - Filter Value and Parameter Table

```
     SDAS SIGNAL CONDITIONING CARD RESISTOR VALUES AND FILTER PARAMETERS
29-FEB-80                EXAMPLE 1

STAGE 1:                          -- GAIN --
      R101 =    10.00      KOHMS
      R102 =    100.0      KOHMS

               DC GAIN =    10.00      (V/V)   [  20.0      (DBV)]
               SINGLE POLE FREQ =    670.0      HZ

STAGE 2:                          -- LOW PASS --
      R201 =    2.550      KOHMS
      R202 =    4.530      KOHMS
      R203 =    4.530      KOHMS
      R204 =    2.000      KOHMS
      R206 =    4.420      KOHMS
           RX01 CHANGES DAMPING; RX04 / RX06 GAIN

               DC GAIN =   -5.124      (V/V)    [  14.2      (DBV)]
               DOUBLE POLE FREQ =    35.13      HZ; DAMPING COEFF =   0.888

STAGE 3:                          -- LOW PASS --
      R301 =    3.650      KOHMS
      R302 =    4.530      KOHMS
      R303 =    4.530      KOHMS
      R304 =    4.530      KOHMS
           RX01 CHANGES DAMPING; RX04 / RX06 GAIN

               DC GAIN =    1.000      (V/V)    [ 0.000      (DBV)]
               DOUBLE POLE FREQ =    35.13      HZ; DAMPING COEFF =   0.621

STAGE 4:                          -- LOW PASS --
      R306 =    10.00      KOHMS
      R309 =    100.0      KOHMS
      C301 =  0.4700E-01 UFD

               DC GAIN =   -10.00      (V/V)   [  20.0      (DBV)]
               POLE FREQ =    33.86      HZ

STAGE 5:                          -- LOW PASS --
      R401 =    10.20      KOHMS
      R402 =    4.530      KOHMS
      R403 =    4.530      KOHMS
      R404 =    3.240      KOHMS
      R406 =    7.150      KOHMS
           RX01 CHANGES DAMPING; RX04 / RX06 GAIN

               DC GAIN =   -1.955      (V/V)    [  5.82      (DBV)]
               DOUBLE POLE FREQ =    35.13      HZ; DAMPING COEFF =   0.222

TOTAL FILTER GAIN =  -1002.      (V/V)    60.0      (DBV)
    (CAUTION: TOTAL GAIN IS SIMPLE PRODUCT. CHECK FILTER TYPE
    TO DETERMINE ACTUAL COMPOSITE GAIN.)
FILTER INVERTS SIGNAL
```

Table E-3 Example 1 - FCHECK System Console Transactions

```
.RUN FCHECK

SDAS SIGNAL CONDITIONING CARD ANALYSIS PROGRAM

 STAGE TO BE ENTERED (0=ENTIRE BOARD)?0

STAGE 1:
R101 (KOHMS) = ? 10.43

R102 (KOHMS) = ? 99.76

DC GAIN =   9.565     (V/V)    [  19.6     (DBV)]
POLE FREQ (HZ) = ? 670.


ENTER AGAIN (Y/N) ? N

STAGE 2:
FILTER TYPE (NONE=0, LP=1, HP=2, BP=3, BR=4)?1

SECOND ORDER LOW PASS FILTER
R201    (KOHMS) = ? 2.54

R202    (KOHMS) = ? 4.56

R203    (KOHMS) = ? 4.34

R204    (KOHMS) = ? 1.98

R206    (KOHMS) = ? 4.43

DC GAIN =   4.948     (V/V)    [  13.9     (DB)]
     NOTE: STAGE INVERTS SIGNAL
POLE FREQ (HZ) =   35.8     , DAMPING COEF =  0.876
MORE CHECKS (Y/N) ? N

STAGE 3:
SECOND ORDER LOW PASS FILTER
R301    (KOHMS) = ? 3.65
```

Table E-3 Example 1 FCHECK System Console Transactions (contd)

```
R302    (KOHMS) = ? 4.55

R303    (KOHMS) = ? 4.56

R304    (KOHMS) = ? 4.49

ADDITIONAL CAPACITORS ADDED (Y/N)?N

DC GAIN =    1.016      (V/V)    [ 0.134      (DB)]
     NOTE: STAGE INVERTS SIGNAL
POLE FREQ (HZ) =    34.9     , DAMPING COEF =  0.624
MORE CHECKS (Y/N) ? N

FOURTH STAGE:
R306 (KOHMS) = ? 9.89

R309 (KOHMS) = ? 98.94

C301 (UFD) (=0. IF NOT USED) = ? .05

DC GAIN =    10.00      (V/V)    [  20.0      (DBV)]
    NOTE: STAGE INVERTS SIGNAL
POLE FREQ =    32.17      HZ

ENTER AGAIN (Y/N) ? N

STAGE 5:
FILTER TYPE (NONE=0, LP=1, HP=2, BP=3, BR=4)?1

SECOND ORDER LOW PASS FILTER
R401    (KOHMS) = ? 10.3

R402    (KOHMS) = ? 4.55

R403    (KOHMS) = ? 4.39

R404    (KOHMS) = ? 3.33

R406    (KOHMS) = ? 7.24
```

Table E-3 Example 1 FCHECK System Console Transactions (contd)

```
DC GAIN =   1.821      (V/V)    [  5.21      (DB)]
     NOTE: STAGE INVERTS SIGNAL
POLE FREQ (HZ) =   35.6     , DAMPING COEF =  0.217
MORE CHECKS (Y/N) ? N


ANY CHANGES (Y/N) ? N

RESISTOR AND PARAMETER PRINTOUT (Y/N) ?Y

PRINTOUT ID (<40 CHAR)?EXAMPLE 1

STORE PARAMETERS ON DISK (Y/N) ? Y

DISK FILE NAME (FORM:DXN:XXXXX.YYY) ? DX1:DUMMY.DAT

CHANNEL NUMBER (1-16) = ? 1

STORE PARAMETERS ON DISK (Y/N) ? N

RERUN PROGRAM (Y/N) ? N

STOP --
```

Parameters stored in disk file.

Disk file previously created (see Appendix G, Section G.15).

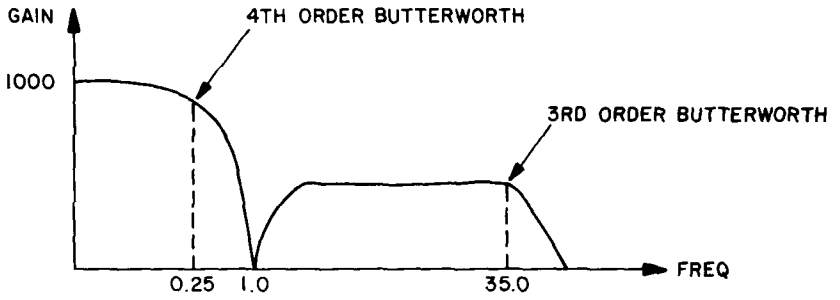
Y response results in request for disk file name and channel number. Allows same information to be put in several disk file channels.

Table E-4 Example 1 - FCHECK Value and Parameter Table

```
     SDAS SIGNAL CONDITIONING CARD RESISTOR VALUES AND FILTER PARAMETERS
29-FEB-80                    ACTUAL COMPONENT VALUES
                          EXAMPLE 1

STAGE 1:                          -- GAIN --
      R101 =    10.43      KOHMS
      R102 =    99.76      KOHMS

               DC GAIN =    9.565      (V/V)    [  19.6      (DBV)]
               POLE FREQ =    670.0      HZ

STAGE 2:                          -- LOW PASS --
      R201 =    2.540      KOHMS
      R202 =    4.560      KOHMS
      R203 =    4.340      KOHMS
      R204 =    1.980      KOHMS
      R206 =    1.430      KOHMS

               DC GAIN =   -4.948      (V/V)    [  13.9      (DBV)]
               DOUBLE POLE FREQ =    35.78      HZ; DAMPING COEFF =   0.876

STAGE 3:                          -- LOW PASS --
      R301 =    3.650      KOHMS
      R302 =    4.550      KOHMS
      R303 =    4.560      KOHMS
      R304 =    4.490      KOHMS

               DC GAIN =    1.016      (V/V)    [ 0.134      (DBV)]
               DOUBLE POLE FREQ =    34.94      HZ; DAMPING COEFF =   0.624

STAGE 4:                          -- LOW PASS --
      R306 =    9.890      KOHMS
      R309 =    98.94      KOHMS
      C301 =  0.5000E-01 UFD

               DC GAIN =   -10.00      (V/V)    [  20.0      (DBV)]
               POLE FREQ =    32.17      HZ

STAGE 5:                          -- LOW PASS --
      R401 =    10.30      KOHMS
      R402 =    4.550      KOHMS
      R403 =    4.390      KOHMS
      R404 =    3.330      KOHMS
      R406 =    7.240      KOHMS

               DC GAIN =   -1.821      (V/V)    [  5.21      (DBV)]
               DOUBLE POLE FREQ =    35.61      HZ; DAMPING COEFF =   0.217

TOTAL FILTER GAIN =   -875.5      (V/V)    58.8      (DBV)
    (CAUTION: TOTAL GAIN IS SIMPLE PRODUCT. CHECK FILTER TYPE
    TO DETERMINE ACTUAL COMPOSITE GAIN.)
FILTER INVERTS SIGNAL

RESULTS STORED IN FILE DX1:DUMMY.DAT  CHANNEL  1
```

DATE: _____ CHANNEL NO: _____

TOTAL RESPONSE DESIRED:



STAGE 1: GAIN ONLY

STAGE GAIN: 10.0 (V/V)
POLE FREQUENCY: 670.0 (HZ)

STAGE 2: FILTER TYPE: GAIN LP BP HP (BR)

ADDED CAPACITOR VALUE: — (UFD)
STAGE GAIN: 5.0 (V/V)
ZERO FREQUENCY: 1.0 (HZ) ZERO DAMPING COEFF: —
POLE FREQUENCY: 0.25 (HZ) POLE DAMPING COEFF: 0.92388

STAGE 3: LOW PASS FILTER ONLY

ADDED CAPACITOR VALUE: — (UFD)
STAGE GAIN: 1 (V/V)
POLE FREQUENCY: 35.0 (HZ) POLE DAMPING COEFF: 0.500

STAGE 4: FILTER TYPE: GAIN (GAIN AND LP)

STAGE GAIN: 10.0 (V/V)
POLE FREQUENCY: 35.0 (HZ)

STAGE 5: FILTER TYPE: GAIN LP BP HP (BR)

ADDED CAPACITOR VALUE: 1.0 (UFD)
STAGE GAIN: 2.0 (V/V)
ZERO FREQUENCY: 1.0 (HZ) ZERO DAMPING COEFF: —
POLE FREQUENCY: 0.25 (HZ) POLE DAMPING COEFF: 0.38268

E-2. Example 2 Signal Conditioning Circuit Board Design Worksheet

Table E-5 Example 2 - FILTER System Console Transactions

```
.RUN FILTER

SDAS SIGNAL CONDITIONING CARD DESIGN PROGRAM

 STAGE TO BE DESIGNED (0=ENTIRE BOARD) = ? 0

STAGE 1:
DC GAIN (V/V) = ? 10.

R102 (K OHMS) = ? 100.

R101 =    10.00      KOHMS

 CHECK ACTUAL COMPONENTS (Y/N) ? N

POLE FREQ (HZ) = ? 670.

STAGE 2:
FILTER TYPE (NONE=0, LP=1, HP=2, BP=3, BR=4)= ? 4

SECOND ORDER BAND REJECT FILTER
ADDITIONAL CAPACITORS ADDED (Y/N)?N

DC GAIN (V/V) = ? 5.

ZERO FREQ (HZ) = ? 1.

POLE FREQ (HZ), DAMPING COEFF = ? .25,.92388

R201 =    345.      KOHMS
R202 =    637.      KOHMS
R203 =    637.      KOHMS
R204 =  0.110E+04   KOHMS
R205 =    10.0      KOHMS
R206 =    1.23      KOHMS
R208 =    32.0      KOHMS

RX01 INFLUENCES DAMPING; RX08 GAIN
****** FOR BEST FREQ REJECTION, RX01*RX08 SHOULD EQUAL RX04*RX05 ******
NOTE: STAGE INVERTS SIGNAL

CHECK ACTUAL COMPONENTS  (Y/N)?Y

R201    (KOHMS) = ? 348.

R202    (KOHMS) = ? 634.

R203    (KOHMS) = ? 634.

R204    (KOHMS) = ? 1100.

R205    (KOHMS) = ? 10.

R206    (KOHMS) = ? 1.24

R208    (KOHMS) = ? 31.6
```

Table E-5 Example 2 FILTER System Console Transactions (contd)

```
ADDITIONAL CAPACITORS ADDED (Y/N)?N

DC GAIN =   4.965      (V/V)      13.9      (DB)
ZERO FREQ (HZ) =  0.9943      ZERO DAMPING COEF =  0.669E-04
POLE FREQ (HZ) =  0.2510      POLE DAMPING COEF =  0.911

MORE CHECKS (Y/N) ? N

STAGE 3:
GAIN CAPABILITY 1/2 OTHER STAGES
SECOND ORDER LOW PASS FILTER
ADDITIONAL CAPACITORS ADDED (Y/N) ? N

DC GAIN (V/V) = ? 1.

POLE FREQ (HZ), DAMPING COEFF = ? 35.,.5

R301 =   4.55      KOHMS
R302 =   4.55      KOHMS
R303 =   4.55      KOHMS
R304 =   4.55      KOHMS

RX01 INFLUENCES DAMPING, RX04 / RX06 GAIN
     NOTE: STAGE INVERTS SIGNAL

CHECK ACTUAL COMPONENTS (Y/N) ? Y

R301    (KOHMS) = ? 4.53

R302    (KOHMS) = ? 4.53

R303    (KOHMS) = ? 4.53

R304    (KOHMS) = ? 4.53

ADDITIONAL CAPACITORS ADDED (Y/N)?N

GAIN =   1.000      (V/V)     0.000      (DB)
POLE FREQ (HZ) =   35.1     , DAMPING COEF =  0.500
REPEAT CHECK (Y/N)?N

FOURTH STAGE:
GAIN AND/OR SINGLE LP POLE ONLY
DC GAIN (V/V) = ? 10.

R309 (KOHMS) = ? 100.

R306 =   10.00      KOHMS

 NOTE: STAGE INVERTS SIGNAL

 FILTER FREQ (GAIN ONLY = 0.) (HZ) = ? 35.

C301 (UFD) =  0.45473E-01

 CHECK ACTUAL COMPONENTS (Y/N) ? Y
```

Table E-5 Example 2 FILTER System Console Transactions (contd)

```
R306 (KOHMS) = ? 10.

R309 (KOHMS) = ? 12.  <-- Error. Wrong value for R309 entered.

C301 (UFD) = ? .4

DC GAIN =   1.200     (V/V)    [  1.58     (DB)]

 NOTE: STAGE INVERTS SIGNAL
POLE FREQ =   33.16     HZ

CHECK AGAIN (Y/N) ? Y  <-- Component values entered again.

R306 (KOHMS) = ? 10.

R309 (KOHMS) = ? 100.

C301 (UFD) = ? .047

DC GAIN =   10.00     (V/V)    [  20.0     (DB)]

 NOTE: STAGE INVERTS SIGNAL
POLE FREQ =   33.86     HZ

CHECK AGAIN (Y/N) ? N

STAGE 5:
FILTER TYPE (NONE=0, LP=1, HP=2, BP=3, BR=4)= ? 4

SECOND ORDER BAND REJECT FILTER
ADDITIONAL CAPACITORS ADDED (Y/N)?Y

CAPACITOR VALUE (BOTH ASSUMED EQUAL) - (UFD)?1.

DC GAIN (V/V) = ? 2.

ZERO FREQ (HZ) = ? 1.

POLE FREQ (HZ), DAMPING COEFF = ? .25,.38268

R401 =   416.      KOHMS
R402 =   318.      KOHMS
R403 =   318.      KOHMS
R404 =  0.333E+04 KOHMS
R405 =   10.0      KOHMS
R406 =  0.510      KOHMS
R408 =   80.0      KOHMS

RX01 INFLUENCES DAMPING; RX08 GAIN
****** FOR BEST FREQ REJECTION, RX01*RX08 SHOULD EQUAL RX04*RX05 ******
NOTE: STAGE INVERTS SIGNAL

CHECK ACTUAL COMPONENTS  (Y/N)?Y

R401   (KOHMS) = ? 412.
```

Table E-5 Example 2 FILTER System Console Transactions (contd)

```
R402    (KOHMS) = ? 316.

R403    (KOHMS) = ? 316.

R404    (KOHMS) = ? 3320.

R405    (KOHMS) = ? 10.

R406    (KOHMS) = ? .511

R408    (KOHMS) = ? 80.6

ADDITIONAL CAPACITORS ADDED (Y/N)?Y

CAPACITOR VALUE (BOTH ASSUMED EQUAL) - (UFD)?1.

DC GAIN =   1.987      (V/V)      5.96      (DB)
ZERO FREQ (HZ) =   1.008      ZERO DAMPING COEF = -0.208E-04
POLE FREQ (HZ) =  0.2518      POLE DAMPING COEF =  0.383

MORE CHECKS (Y/N) ? N


 ANY CHANGES (Y/N) ? N

RESISTOR AND PARAMETER PRINTOUT (Y/N) ? Y

PRINTOUT ID (<40 CHAR)?EXAMPLE 2

STORE PARAMETERS ON DISK (Y/N) ? Y

DISK FILE NAME (FORM:DXN:XXXXX.YYY) ? DX1:DUMMY.DAT

CHANNEL NUMBER (1-16) = ? 1

STORE PARAMETERS ON DISK (Y/N) ? N

RESTART PROGRAM (Y/N) ? N

STOP --
```

Table E-6 Example 2 - FILTER Value and Parameter Table

```
     SDAS SIGNAL CONDITIONING CARD RESISTOR VALUES AND FILTER PARAMETERS
29-FEB-80                EXAMPLE 2

STAGE 1:                      -- GAIN --
      R101 =   10.00      KOHMS
      R102 =   100.0      KOHMS

              DC GAIN =   10.00      (V/V)   [  20.0      (DBV)]
              SINGLE POLE FREQ =   670.0      HZ
```

Table E-6 Example 2 FILTER Value and Parameter Table (contd)

```
STAGE 2:                        -- BAND REJECT --
      R201 =    348.0      KOHMS
      R202 =    634.0      KOHMS
      R203 =    634.0      KOHMS
      R204 =    1100.      KOHMS
      R205 =    10.00      KOHMS
      R206 =    1.240      KOHMS
      R208 =    31.60      KOHMS
           RX01 CHANGES DAMPING; RX08 GAIN
             ****** FOR BEST FREQ REJECTION, RX01*RX08  = RX04*RX05 ******

              DC GAIN =  -4.965      (V/V)    [  13.9      (DBV)]
              DOUBLE POLE FREQ =  0.2510      HZ; DAMPING COEFF =  0.911
              DOUBLE ZERO FREQ =  0.9943      HZ; DAMPING COEFF =  0.669E-04

STAGE 3:                        -- LOW PASS --
      R301 =    4.530      KOHMS
      R302 =    4.530      KOHMS
      R303 =    4.530      KOHMS
      R304 =    4.530      KOHMS
           RX01 CHANGES DAMPING; RX04 / RX06 GAIN

              DC GAIN =    1.000      (V/V)    [ 0.000      (DBV)]
              DOUBLE POLE FREQ =    35.13      HZ; DAMPING COEFF =  0.500

STAGE 4:                        -- LOW PASS --
      R306 =    10.00      KOHMS
      R309 =    100.0      KOHMS
      C301 =  0.4700E-01 UFD

              DC GAIN =  -10.00      (V/V)  [  20.0      (DBV)]
              POLE FREQ =    33.86      HZ

STAGE 5:                        -- BAND REJECT --
      R401 =    412.0      KOHMS
      R402 =    316.0      KOHMS
      R403 =    316.0      KOHMS
      R404 =    3320.      KOHMS
      R405 =    10.00      KOHMS
      R406 =  0.5110      KOHMS
      R408 =    80.60      KOHMS
           RX01 CHANGES DAMPING; RX08 GAIN
             ****** FOR BEST FREQ REJECTION, RX01*RX08  = RX04*RX05 ******

              DC GAIN =  -1.987      (V/V)    [  5.96      (DBV)]
              DOUBLE POLE FREQ =  0.2518      HZ; DAMPING COEFF =  0.383
              DOUBLE ZERO FREQ =   1.008      HZ; DAMPING COEFF = -0.208E-04

TOTAL FILTER GAIN =  -986.3      (V/V)   59.9      (DBV)
    (CAUTION: TOTAL GAIN IS SIMPLE PRODUCT. CHECK FILTER TYPE
    TO DETERMINE ACTUAL COMPOSITE GAIN.)
FILTER INVERTS SIGNAL

RESULTS STORED IN FILE DX1:DUMMY.DAT  CHANNEL  1
```

Table E-7 Example 2 - FCHECK System Console Transactions

```
.RUN FCHECK

SDAS SIGNAL CONDITIONING CARD ANALYSIS PROGRAM

 STAGE TO BE ENTERED (0=ENTIRE BOARD)?0

STAGE 1:
R101 (KOHMS) = ? 10.1

R102 (KOHMS) = ? 100.03

DC GAIN =   9.904      (V/V)    [  19.9      (DBV)]
POLE FREQ (HZ) = ? 670.


ENTER AGAIN (Y/N) ? N

STAGE 2:
FILTER TYPE (NONE=0, LP=1, HP=2, BP=3, BR=4)?4

SECOND ORDER BAND REJECT FILTER
NOMINAL POLE FREQ (HZ) = ? .25

NOMINAL ZERO FREQ (HZ) = ? 1.

R201    (KOHMS) = ? 346.6

R202    (KOHMS) = ? 635.6

R203    (KOHMS) = ? 633.4

R204    (KOHMS) = ? 1158.

R205    (KOHMS) = ? 9.78

R206    (KOHMS) = ? 1.23

R208    (KOHMS) = ? 30.8

ADDITIONAL CAPACITORS ADDED (Y/N)?N

DC GAIN =   4.772      (V/V)    [  13.6      (DB)]
     NOTE: STAGE INVERTS SIGNAL
ZERO FREQ (HZ) =  0.9616     , ZERO DAMPING COEF =  0.137E-01
POLE FREQ (HZ) =  3.2508     , POLE DAMPING COEF =  0.915

REPEAT CHECK (Y/N) ? N

STAGE 3:
SECOND ORDER LOW PASS FILTER
R301    (KOHMS) = ? 4.59

R302    (KOHMS) = ? 4.52

R303    (KOHMS) = ? 4.55
```

Table E-7 Example 2 FCHECK System Console Transactions (contd)

```
R304    (KOHMS) = ? 4.512

ADDITIONAL CAPACITORS ADDED (Y/N)?N

DC GAIN =   1.008      (V/V)    [ 0.728E-01 (DB)]
     NOTE: STAGE INVERTS SIGNAL
POLE FREQ (HZ) =   35.1      , DAMPING COEF =  0.494
MORE CHECKS (Y/N) ? N

FOURTH STAGE:
R306 (KOHMS) = ? 9.867

R309 (KOHMS) = ? 102.3

C301 (UFD) (=0. IF NOT USED) = ? .052

DC GAIN =   10.37      (V/V)    [  20.3      (DBV)]
    NOTE: STAGE INVERTS SIGNAL
POLE FREQ =   29.92      HZ

ENTER AGAIN (Y/N) ? N

STAGE 5:
FILTER TYPE (NONE=0, LP=1, HP=2, BP=3, BR=4)?3

SECOND ORDER BAND PASS FILTER
R401    (KOHMS) = ? 2.

R402    (KOHMS) = ? 2.

R403    (KOHMS) = ? 3.

R404    (KOHMS) = ? 4.

R405    (KOHMS) = ? 5.

ADDITIONAL CAPACITORS ADDED (Y/N)?N

CENTER FREQ GAIN =  0.3798      (V/V)    [ -8.41      (DB)]
ZERO FREQ (HZ) =  0.6497E-02
POLE FREQ (HZ) =   64.97      , POLE DAMPING COEF =  0.612
REPEAT CHECK (Y/N) ? N

ANY CHANGES (Y/N)?Y

STAGE TO BE CHANGED?5

STAGE 5:
FILTER TYPE (NONE=0, LP=1, HP=2, BP=3, BR=4)?4

SECOND ORDER BAND REJECT FILTER
NOMINAL POLE FREQ (HZ) = ? .25

NOMINAL ZERO FREQ (HZ) = ? 1.
```

Error. Wrong filter type number entered. Redone below.

Stage 5 rerun using correct stage type number.

Table E-7 Example 2 FCHECK System Console Transactions (contd)

```
R401    (KOHMS) = ? 411.3

R402    (KOHMS) = ? 315.

R403    (KOHMS) = ? 312.4

R404    (KOHMS) = ? 3435.

R405    (KOHMS) = ? 10.8

R406    (KOHMS) = ? .506

R408    (KOHMS) = ? 80.78

ADDITIONAL CAPACITORS ADDED (Y/N)?Y

CAPACITOR VALUE (BOTH ASSUMED EQUAL) - (UFD)?1.

DC GAIN =   1.921      (V/V)    [  5.67      (DB)]
     NOTE: STAGE INVERTS SIGNAL
ZERO FREQ (HZ) =  0.9993     , ZERO DAMPING COEF =  0.101E-01
POLE FREQ (HZ) =  0.2537     , POLE DAMPING COEF =  0.381

REPEAT CHECK (Y/N) ? N

ANY CHANGES (Y/N) ?N

RESISTOR AND PARAMETER PRINTOUT (Y/N) ?Y

PRINTOUT ID (<40 CHAR)?EXAMPLE 2

STORE PARAMETERS ON DISK (Y/N) ? N

RERUN PROGRAM (Y/N) ? N

STOP --
```

Table E-8 Example 2 - FCHECK Value and Parameter Table

```
     SDAS SIGNAL CONDITIONING CARD RESISTOR VALUES AND FILTER PARAMETERS
29-FEB-80                    ACTUAL COMPONENT VALUES
                          EXAMPLE 2

STAGE 1:                          -- GAIN --
      R101 =   10.10     KOHMS
      R102 =   100.0     KOHMS

               DC GAIN =   9.904     (V/V)    [  19.9     (DBV)]
               POLE FREQ =   670.0     HZ

STAGE 2:                          -- BAND REJECT --
      R201 =   346.6     KOHMS
      R202 =   635.6     KOHMS
      R203 =   633.4     KOHMS
      R204 =   1158.     KOHMS
      R205 =   9.780     KOHMS
      R206 =   1.230     KOHMS
      R208 =   30.80     KOHMS

               DC GAIN =  -4.772     (V/V)    [  13.6     (DBV)]
               DOUBLE POLE FREQ =  0.2508     HZ; DAMPING COEFF =  0.915
               DOUBLE ZERO FREQ =  0.9616     HZ; DAMPING COEFF =  0.137E-01

STAGE 3:                          -- LOW PASS --
      R301 =   4.590     KOHMS
      R302 =   4.520     KOHMS
      R303 =   4.550     KOHMS
      R304 =   4.512     KOHMS

               DC GAIN =   1.008     (V/V)    [ 0.728E-01 (DBV)]
               DOUBLE POLE FREQ =   35.09     HZ; DAMPING COEFF =  0.494

STAGE 4:                          -- LOW PASS --
      R306 =   9.867     KOHMS
      R309 =   102.3     KOHMS
      C301 =  0.5200E-01 UFD

               DC GAIN =  -10.37     (V/V)    [  20.3     (DBV)]
               POLE FREQ =   29.92     HZ

STAGE 5:                          -- BAND REJECT --
      R401 =   411.3     KOHMS
      R402 =   315.0     KOHMS
      R403 =   312.4     KOHMS
      R404 =   3435.     KOHMS
      R405 =   10.80     KOHMS
      R406 =  0.5060     KOHMS
      R408 =   80.78     KOHMS

               DC GAIN =  -1.921     (V/V)    [  5.67     (DBV)]
               DOUBLE POLE FREQ =  0.2537     HZ; DAMPING COEFF =  0.381
               DOUBLE ZERO FREQ =  0.9993     HZ; DAMPING COEFF =  0.101E-01

TOTAL FILTER GAIN =  -949.2     (V/V)   59.5     (DBV)
    (CAUTION: TOTAL GAIN IS SIMPLE PRODUCT. CHECK FILTER TYPE
    TO DETERMINE ACTUAL COMPOSITE GAIN.)
FILTER INVERTS SIGNAL
```

Appendix F

Signal Conditioning Circuit Card Design Software

F.1 PROGRAM OVERVIEW

The following sections list the signal conditioning card design software. *The SDAS computer* was used for all software development. This software was written in FORTRAN (Digital Equipment Company [DEC] FORTRAN IV version V01C-3A) running under DEC's RT-11 operating system (RT-11FB, version V02C-02B).

The design program calculates the required plug-in resistor and capacitor values for configuring a signal conditioning card. It accepts filter type and parameter information from the user. After calculating and displaying the optimum resistor/capacitor values, the program allows the user to enter readily-available component values. The program then uses these values to calculate the stage's filter parameters and displays them for the user. Hints on component effects and warnings for values causing performance degradation (see Appendix D) are also displayed. After component values are settled on, the program prints out a table of component values and filter parameters for the card to aid in board configuration and documentation. Finally, the program can store the card filter parameters in a floppy disk file for use by other programs.

In all its calculations, the program assumes 10KΩ values for the fixed resistors associated with the filter stages. It also assumes 1.0 μF values for all fixed capacitors. However, since capacitor values can be changed (either by replacement or, in the case of stage 3, by adding a second capacitor in parallel with the fixed ones), the program asks if additional capacitors are added. If a "Y" reply is given to the question, the capacitor value is asked for. Since the entered value is added to the fixed value, a smaller capacitor can be reflected by entering as a negative value the difference between

1.Ø μF and the value used on the card. (Both capacitors are assumed to be equal.)

In stages 2 and 5, stage gain can be achieved through two amplifiers. Stage gain is therefore split evenly between the two by the program. In stage 3, only one amplifier can be used for gain. A comment that the stage gain capability is half of the other stages' is displayed when the stage is processed.

Equations used in this program are covered in Appendix D. Since the program was designed for low frequency (under 5ØØ Hz) filter designs with moderate stage gains, no allowances for parasitics or amplifier gain-bandwidth product limitations are included.

This program consists of a main program with 14 subroutines. The main program contains all user interfaces; it relies on subroutines to perform the actual calculations and data printouts. Both the main program and the subroutines use a COMMON block to store component values and filter parameters. This block is defined by the statement

```
COMMON R(5,8),CAP(5,3),AV(5,2),FP(5),DP(5),FZ(5),DZ(5),NTY(5)
```

The arrays in this common block are defined in Table F-1.

F.2 MAIN DESIGN PROGRAM

The main program handles overall communications with the user. It also calculates the component values for stages 1 and 4. Subroutines are called to do the calculations for stages 2, 3, and 5 as well as for table printout and disk filter parameter storage.

Table F-2 contains the main resistor calculation program.

F.3 SUBROUTINE DC

This subroutine calculates resistor values for stages 2 and 5 for providing gain only. The subroutine accepts a stage gain value from the user and calculates the resistor value required to achieve that gain. If the user wants to check the effect of using resistor values other than those calculated, subroutine DCCHK is called to perform the needed calculations. After a satisfactory resistor value is reached, the subroutine stores the value and the appropriate stage parameters in COMMON and returns to the calling program.

Table F-3 contains this subroutine.

F.4 SUBROUTINE DCCHK

This subroutine calculates stage gain from user-entered resistor values for stages 2 and 5. The routine includes provisions for repeating the calculation should the user wish to check the effects

of other resistor values. After a satisfactory resistor value is reached, the subroutine returns to the calling subroutine.

Table F-4 contains this subroutine.

F.5 SUBROUTINE LP

This subroutine is called by the main program to calculate the required resistor values for forming a second order (two pole) lowpass filter as discussed in Appendix D, Section D.2. It is usable for stages 2, 3, or 5. The subroutine accepts a stage gain value and filter parameters from the user and calculates the resistor values required to achieve that response. (See Section D.2.1 of Appendix D for a discussion of the design equations used in this subroutine.) The calculated resistor values are displayed on the system console together with hints on parameters effected by resistor selections. If the user wants to check the effect of using resistor values other than those calculated, subroutine LPCHK is called to perform the needed calculations. After satisfactory resistor values are reached, the subroutine stores the values and the appropriate stage parameters in COMMON and returns to the calling program.

Table F-5 contains the subroutine.

F.6 SUBROUTINE LPCHK

This subroutine calculates the lowpass filter parameters from user-entered resistor and capacitor values for stages 2, 3, and 5. (See Section D.2.2 of Appendix D for a discussion of the equations implemented in this subroutine.) The calculated filter parameters are displayed on the system console. The routine includes provisions for repeating the calculation should the user wish to check the effects of other resistor values. After a satisfactory resistor value is reached, the subroutine returns to the calling subroutine.

Table F-6 contains this subroutine.

F.7 SUBROUTINE HP

This subroutine is called by the main program to calculate the required resistor values for forming a second order (two pole) highpass filter as discussed in Appendix D, Section D.4. It is usable for stages 2 or 5.

The subroutine accepts a stage gain value and filter parameters from the user and calculates the resistor values required to achieve that response. (See Section D.4.1 of Appendix D for a discussion of the design equations used in this subroutine.) The calculated values are displayed on the system console together with hints on parameters effected by resistor selection and on resistor ratios for proper filter operation (see Appendix D, Section D.4.2 for more on ratios).

If the user wants to check the effect of using resistor values other than those calculated, subroutine HPCHK is called to perform the needed calculations. If no checks are made, the program uses FZERO = FPOLE/10,000 and DAMPZ=0 (zero frequency and damping coefficient, respectively) to model the ideal highpass response. (This modeling is used for compatability with programs using these values to calculate system transfer function information.) If a check of resistor values is made, the calculated FZERO and DAMPZ vales are substituted for the ideal values. After satisfactory resistor values are reached, the subroutine stores the values and the appropriate stage parameters in COMMON and returns to the calling program.

Table F-7 contains the subroutine.

F.8 SUBROUTINE HPCHK

This subroutine calculates the highpass filter parameters from user-entered resistor values for stages 2 and 5. (See Section D.4.2 of Appendix D for a discussion of the equations implemented in this subroutine.) The highpass response is modeled by a double pole at FPOLE and a double zero at either the calculated FZERO or FPOLE/10,000, whichever is greater. (This modeling of FZERO is used to ease calculations in programs to calculate system transfer function responses.) The calculated filter parameters are displayed on the system console. The program also checks for a negative damping coefficient, as discussed in Appendix D, Section D.4.2, and displays a message if appropriate. The routine includes provisions for repeating the calculation should the user wish to check the effects of other resistor values. After satisfactory resistor values are reached, the subroutine returns to the calling subroutine.

Table F-8 contains this subroutine.

F.9 SUBROUTINE BP

This subroutine is called by the main program to calculate the required resistor values for forming a second order (two pole) bandpass filter as discussed in Appendix D, Section D.3. It is usable for stages 2 or 5. The subroutine accepts a stage gain value and filter parameters from the user and calculates the resistor values required to achieve that response. (See Section D.3.1 of Appendix D for a discussion of the design equations used in this subroutine.) The calculated values are displayed on the system console together with hints on parameters effected by resistor selection.

If the user wants to check the effect of using resistor values other than those calculated, subroutine BPCHK is called to perform the needed calculations. If no checks are made, the program uses FZERO = FPOLE/10,000 (zero frequency) to model the ideal highpass response. (This modeling is used to allow compatability with programs used to calculate system transfer functions.) If a check of resistor values is made, the calculated FZERO is substituted for the ideal value. After satisfactory resistor values are reached, the subroutine stores the values and the appropriate stage parameters in

COMMON and returns to the calling program.

Table F-9 contains the subroutine.

F.10 SUBROUTINE BPCHK

This subroutine calculates the bandpass filter parameters from user-entered resistor values for stages 2 and 5. (See Section D.3.2 of Appendix D for a discussion of the equations implemented in this subroutine.) The actual bandpass response is modeled by a double pole at FPOLE and a single zero (FZERO) at FPOLE/10,000. (This modeling of FZERO is used to ease calculations in programs using these filter parameters to calculate system response information.) The calculated filter parameters are displayed on the system console. The routine includes provisions for repeating the calculation should the user wish to check the effects of other resistor values. After satisfactory resistor values are reached, the subroutine returns to the calling subroutine.

Table F-10 contains this subroutine.

F.11 SUBROUTINE BR

This subroutine is called by the main program to calculate the required resistor values for forming a second order band reject filter as discussed in Appendix D, Section D.6. It is usable for stages 2 or 5.

The subroutine accepts a stage gain value and filter parameters from the user and calculates the resistor values required to achieve that response.(See Sections D.6.1.1 and D.6.2.1 of Appendix D for a discussion of the design equations used in this subroutine.) The calculated values are displayed on the system console together with hints on parameters effected by resistor selection and on resistor ratios for proper filter operation (see Appendix D, Sections D.6.1.2 and D.6.2.2 for more on ratios). If the user wants to check the effect of using resistor values other than those calculated, subroutine BRCHK is called to perform the needed calculations. After satisfactory resistor values are reached, the subroutine stores the values and stage parameters in COMMON and returns to the calling program.

Table F-11 contains the subroutine.

F.12 SUBROUTINE BRCHK

This subroutine calculates the band reject filter parameters from user-entered resistor values for stages 2 and 5. (See Sections D.6.1.2 and D.6.2.2 of Appendix D for a discussion of the equations implemented in this subroutine.) The calculated filter parameters are displayed on the system console. The program also checks for a

negative damping coefficient and for a negative ωz value, as discussed in Appendix D, Sections D.6.1.2 and D.6.2.2, and displays a message if appropriate. The routine allows repeating the calculation should the user wish to check the effects of other resistor values. After satisfactory resistor values are reached, the subroutine returns to the calling subroutine.

Table F-12 contains this subroutine.

F.13 SUBROUTINE PRINT

This subroutine prints on the line printer a table of resistor values and filter parameters. A user-entered title is added to the printout to allow its positive identification. It uses subroutine RPRINT to print out the table details for stages 2, 3, and 5. The subroutine also calculates a simple total for stage gain and prints it at the bottom of the table. (The total is a product of the stage gains. Since they do not all occur at the same frequency, the total may not accurately reflect gain at a given frequency.)

Table F-13 contains the subroutine.

F.14 SUBROUTINE RPRINT

This subroutine is called by subroutine PRINT to print resistor and filter parameter values for stages 2, 3, and 5. It also prints out hints on effects of component selection on filter parameters.

Table F-14 contains this subroutine.

F.15 SUBROUTINE STORE

This subroutine is called by the main program store filter parameter values in disk files for use by other programs. The files must have been created prior to using this subroutine. The DEC FORTRAN program listed in Table F-15 create a file of the proper format and loads it with zeroes.

Subroutine STORE accepts a file name and channel number from the user. It then calls subroutine SPECFI to read the file into COMMON /SPECS/ (The format of COMMON /SPECS/ is defined in Section E.16.) STORE checks the status flag supplied by SPECFI to see if the record was blank. If the record was blank, the program then clears COMMON /SPECS/. Then it checks which filter stages have data in them, loads the data into COMMON /SPECS/ and calls SPECFI to write the information back to the file. (Note: The convention used in COMMON /SPECS/ for stage gain storage is to store all gains as zero frequency gains. Therefore, the subroutine converts highpass and bandpass filter stage gains to dc gains prior to storage.)

Table F-16 contains subroutine STORE.

F.16 SUBROUTINE SPECFI

This subroutine is called by STORE to read from and write to disk files. The subroutine is general in nature and thus has features not used by STORE. It is designed to handle files containing models of an entire data collection system (sensors, preamps, and signal conditioning cards). Only the signal conditioning card information is used by STORE. Table F-17 gives the definitions of all elements of COMMON /SPECS/.

Subroutine SPECFI creates and reads 16-record files. When initially creating a file, all records not being filled from COMMON /SPECS/ are loaded with zeroes. Data from COMMON /SPECS/ is stored in the file as a 104-word record. The first word in the record is set to 1 to indicate data in the record, while the last four words are used to store the LOGICAL*1 array UNITS through the use of an equivalence statement.

Table F-18 contains the subroutine.

Table F-1 Common Block Definitions

R(5,8) = Resistor values in KΩ
Resistor numbers versus array location (R(X,Y)):

		Y							
		1	2	3	4	5	6	7	8
	1	101	102						
	2	201	202	203	204	205	206	207	208
X	3	301	302	303	304				
	4	306	309						
	5	401	402	403	404	405	406	407	408

C(5,3) = Capacitor values in μF.
Capacitor numbers versus array location (C(X,Y)):

		Y		
		1	2	3
	1			
	2	C1'	C2'	
X	3	C3'	C4'	
	4	C301		
	5	C5'	C6'	

Note: C1'-C6' are values of additional capacitors paralleled with C1-C6 (if C1-C6 are replaced with capacitors that are smaller than 1.0 μF, a negative value of C1'-C6' gives the difference between the new values and 1.0 μF).

AV(5,2) = Voltage gains. For each stage, two values of gain are given as follows:

AV(ST-,1) = V/V gain (- value implies stage inverts)
AV(ST-,2) = dBV gain

FP(5) = Stage pole frequencies (Hz).

DP(5) = Stage pole damping coefficients.

Note: DP(N) = 0.0 implies stage has single pole;
DP(N) ≠ 0.0 implies stage has double pole.

FZ(5) = Stage zero frequencies (Hz).

Note: - Value implies negative ωz - see Appendix D.

DZ(5) = Zero damping coefficients.

Note: DZ(N) = 0.0 implies stage has single zero;
DZ(N) ≠ 0.0 implies stage has double zero.

Table F-2 FILTER - Main Program Listing

```
      PROGRAM FILTER CARD RESISTOR CALCULATIONS
      COMMON R(5,8),CAP(5,3),AV(5,2),FP(5),DP(5),FZ(5),DZ(5),NTY(5)
      LOGICAL*1 ANS,YES,NO
      DATA YES/1HY/,NO/1HN/
      TWOPI=6.2831853
      TYPE 10
10    FORMAT (' SDAS SIGNAL CONDITIONING CARD DESIGN PROGRAM')
      NST=0
C     Restart point for redesigning entire board
      GOTO 11000
10000 NST=1
C     Clear COMMON for initial program use
11000 DO 900 N=1,5
      DO 800 M=1,8
      R(N,M)=0.
800   CONTINUE
      CAP(N,1)=0.
      CAP(N,2)=0.
      CAP(N,3)=0.
      AV(N,1)=0.
      AV(N,2)=0.
      FP(N)=0.
      DP(N)=0.
      FZ(N)=0.
      DZ(N)=0.
900   CONTINUE
C
C     Begin.  The program asks for the stage to be designed and then
C     jumps to that stage.
C
      IF(NST.EQ.1) GOTO 1000
      TYPE 40
40    FORMAT ('0 STAGE TO BE DESIGNED (0=ENTIRE BOARD) = ? ',$)
      ACCEPT 50,NST
50    FORMAT (I1)
      NST=NST+1
20000 GOTO (1000,1000,2000,3000,4000,5000) NST
C
C     Stage 1. Stage 1 can only be used for gain. The value of stage gain and
C     of one of the gain-setting resistors is gotten from the user and the
```

Table F-2 FILTER - Main Program Listing (contd)

```
C       other resistor value is calculated. The program then allows
C       the resistor values to be entered to recalculate gain.  When a satis-
C       factory gain is reached, the program then accepts a pole frequency for
C       the stage. This frequency is determined by the values of the frequency-
C       limiting components used on the circuit board and is user-entered.
C       The program next stores the component and parameter values in
C       the proper COMMON locations.  If the entire board is not being
C       designed, the program jumps to the closeout section; otherwise,
C       the next stage is designed
C
1000    TYPE 110
110     FORMAT (' STAGE 1:')
        TYPE 120
120     FORMAT ('$DC GAIN (V/V) = ? ')
        ACCEPT 130,GAIN
130     FORMAT (E12.5)
        IF (GAIN.EQ.0.) GOTO 1100
        TYPE 140
140     FORMAT ('$R102 (OPTIMUM = 100) (K OHMS) = ? ')
        ACCEPT 130,RS
        RG=RS/GAIN
        TYPE 150,RG
150     FORMAT (' R101 = ',G11.4,' KOHMS')
        TYPE 160
160     FORMAT ('0 CHECK ACTUAL COMPONENTS (Y/N) ? ',$)
        ACCEPT 170,ANS
170     FORMAT (A1)
        IF (ANS.NE.YES) GOTO 1900
1100    TYPE 180
180     FORMAT ('$R101 (KOHMS) = ? ')
        ACCEPT 130,RG
        TYPE 140
        ACCEPT 130,RS
        GAIN=RS/RG
        DBG=20.*(ALOG10(GAIN))
        TYPE 190,GAIN,DBG
190     FORMAT (' DC GAIN = ',G11.4,' (V/V)   [',G10.3,' (DB)]')
        TYPE 195
195     FORMAT ('0CHECK AGAIN (Y/N) ? ',$)
        ACCEPT 170,ANS
```

Table F-2 FILTER - Main Program Listing (contd)

```
      IF (ANS.EQ.YES) GOTO 1100
1900  TYPE 198
198   FORMAT ('$POLE FREQ (HZ) = ? ')
      ACCEPT 130,FREQ
      R(1,1)=RG
      R(1,2)=RS
      FP(1)=FREQ
      AV(1,1)=GAIN
      AV(1,2)=20.*(ALOG10(GAIN))
      NTY(1)=2
      IF (NST.NE.1) GOTO 6000
C
C     Stage 2.  This stage can be used for any type of filter. The
C     program accepts the filter type and then calls the appropriate sub-
C     routine to perform the actual calculations.  If the entire board is
C     not being designed, the program jumps to the closeout section;
C     otherwise, the next stage is designed.
C
2000  TYPE 200
200   FORMAT (' STAGE 2:')
2100  TYPE 210
210   FORMAT ('$FILTER TYPE (NONE=0, LP=1, HP=2, BP=3, BR=4)= ? ')
      ACCEPT 220,NTYP
220   FORMAT (I1)
      NTYP=NTYP+1
      GOTO (2200,2300,2400,2500,2600) NTYP
      GOTO 2100  !REPEAT ABOVE IF GOTO OUT OF RANGE
2200  CALL DC(2)
      GOTO 2900
2300  CALL LP(2)
      GOTO 2900
2400  CALL HP(2)
      GOTO 2900
2500  CALL BP(2)
      GOTO 2900
2600  CALL BR(2)
      GOTO 2900
2900  IF (NST.NE.1) GOTO 6000
C
C     Stage 3.  This stage can only be used as a lowpass filter.
```

Table F-2 FILTER - Main Program Listing (contd)

```
C       If the entire board is not being designed,  after subroutine return
C       the program jumps to the closeout section; otherwise, the next stage
C       is designed.
C
3000    TYPE 300
300     FORMAT (' STAGE 3:')
        TYPE 310
310     FORMAT (' GAIN CAPABILITY 1/2 OTHER STAGES')
        CALL LP(3)
        IF (NST.NE.1) GOTO 6000
C
C       Stage 4.  This stage can be used for gain or for gain and a
C       single lowpass pole only. The program accepts values for stage
C       gain and for one of the gain-setting resistors. It calculates
C       and displays the value of the other resistor. After accepting a
C       lowpass frequency value (0 implying no filter), the program checks
C       for a nonzero frequency. If it finds one, it calculates and displays
C       the required capacitor size.  After allowing iterative component
C       entries and parameter calculations, the program stores the component
C       and parameter values in the proper COMMON locations.  If the entire
C       board is not being designed, the program jumps to the closeout
C       section; otherwise, the next stage is designed.
C
4000    TYPE 400
400     FORMAT (' FOURTH STAGE:')
        TYPE 410
410     FORMAT (' GAIN AND/OR SINGLE LP POLE ONLY')
        TYPE 120
        ACCEPT 130, GAIN
C       Component calculation:
        TYPE 420
420     FORMAT ('$R309 (KOHMS) = ? ')
        ACCEPT 130,RF
        R1=RF/GAIN
        TYPE 430,R1
430     FORMAT (' R306 = ',G11.4,' KOHMS')
        TYPE 435
435     FORMAT ('0 NOTE: STAGE INVERTS SIGNAL')
        TYPE 440
440     FORMAT ('0 FILTER FREQ (ENTER 0.0 FOR GAIN ONLY) (HZ) = ? ',$)
```

Table F-2 FILTER - Main Program Listing (contd)

```
        ACCEPT 130,FREQ
        C=0.0
        IF (FREQ.EQ.0.) GOTO 4100
        C=1/(TWOPI*1000.*RF*FREQ)
        C=C*1.E+06
        TYPE 450,C
450     FORMAT (' C301 (UFD) = ',G12.5)
4100    TYPE 160
        ACCEPT 170,ANS
        IF (ANS.NE.YES) GOTO 4900
C       Parameter calculation:
4200    IF (FREQ.NE.0.) GOTO 4300
        TYPE 460
460     FORMAT ('$R306 (KOHMS) = ? ')
        ACCEPT 130,R1
        TYPE 420
        ACCEPT 130,RF
        GAIN=RF/R1
        DBG=20.*(ALOG10(GAIN))
        TYPE 190,GAIN,DBG
        TYPE 435
        GOTO 4800
4300    TYPE 460
        ACCEPT 130,R1
        TYPE 420
        ACCEPT 130,RF
        TYPE 480
480     FORMAT ('$C301 (UFD) = ? ')
        ACCEPT 130,C
490     FORMAT (3E12.5)
        GAIN=RF/R1
        DBG=20.*(ALOG10(GAIN))
        TYPE 190,GAIN,DBG
        IF (C.EQ.0.0) GOTO 4800
        TYPE 435
        FREQ=1000./(TWOPI*C*RF)
        TYPE 495,FREQ
495     FORMAT (' POLE FREQ = ',G11.4,' HZ')
4800    TYPE 195
        ACCEPT 170,ANS
```

Table F-2 FILTER - Main Program Listing (contd)

```
      IF (ANS.EQ.YES) GOTO 4200
4900  R(4,1)=R1
      R(4,2)=RF
      CAP(4,1)=C
      AV(4,1)=-GAIN
      AV(4,2)=20.*(ALOG10(GAIN))
      FP(4)=FREQ
      DP(4)=0.
      NTY(4)=1
      IF (FREQ.NE.0.) NTY(4)=2
      IF (NST.NE.1) GOTO 6000
C
C     Stage 5.  This stage can be used for any type of filter. The
C     program accepts the filter type and then calls the appropriate sub-
C     routine to perform the actual calculations.
C
5000  TYPE 500
500   FORMAT (' STAGE 5:')
5100  TYPE 210
      ACCEPT 220,NTYP
      NTYP=NTYP+1
      GOTO (5200,5300,5400,5500,5600) NTYP
      GOTO 5100 ! REPEAT ABOVE IF GOTO OUT OF RANGE
5200  CALL DC(5)
      GOTO 6000
5300  CALL LP(5)
      GOTO 6000
5400  CALL HP(5)
      GOTO 6000
5500  CALL BP(5)
      GOTO 6000
5600  CALL BR(5)
C
C     Closeout section. This section allows the user to change any
C     stage in case of error or changed specifications. This change will
C     affect only the stage selected; all other stages' component and
C     parameter values stored in COMMON will be unchanged. Once all
C     stages are satisfactory, the program allows the user the
C     options of printing out a table of component values and of
```

Table F-2 FILTER - Main Program Listing (contd)

```
C       storing stage parameters in a floppy disk file. Finally, the program
C       allows the user the option of restarting the program to design a new
C       filter card.
C
6000    TYPE 600
600     FORMAT ('0 ANY CHANGES (Y/N) ? ',$)
        ACCEPT 170,ANS
        IF (ANS.NE.YES) GOTO 7000
        TYPE 610
610     FORMAT ('$STAGE TO BE CHANGED (1-5) = ? ')
        ACCEPT 50,NST
        NST=NST+1
        GOTO 20000
7000    TYPE 620
620     FORMAT ('$RESISTOR AND PARAMETER PRINTOUT (Y/N) ? ')
        ACCEPT 170,ANS
        IF (ANS.EQ.YES) CALL PRINT
7100    TYPE 630
630     FORMAT ('$STORE PARAMETERS ON DISK (Y/N) ? ')
        ACCEPT 170,ANS
        IF (ANS.NE.YES) GOTO 7200
        CALL STORE
        GOTO 7100
7200    PRINT 640
640     FORMAT ('1')
        CALL CLOSE (6)
        TYPE 650
650     FORMAT ('$RESTART PROGRAM (Y/N) ? ')
        ACCEPT 170,ANS
        IF(ANS.EQ.YES) GOTO 10000
        END
```

Table F-3 Subroutine DC Listing

```
      SUBROUTINE DC (NST)
C
C     NST = Stage number (2,5) passed from calling program.
C
      COMMON R(5,8),CAP(5,3),AV(5,2),DUMMY(20),NTY(5)
      LOGICAL*1 ANS,YES
      DATA YES/1HY/
      TYPE 100
100   FORMAT (' GAIN ONLY')
      TYPE 110
110   FORMAT ('$DC GAIN (V/V) = ? ')
      ACCEPT 120,GAIN
120   FORMAT (E12.5)
      R8=10./GAIN
      IF (NST.EQ.5) GOTO 1000
      TYPE 130,208,R8
130   FORMAT (' R',I3,' = ',G10.3,' KOHMS')
      GOTO 1100
1000  TYPE 130,408,R8
1100  TYPE 140
140   FORMAT ('0NOTE: STAGE INVERTS SIGNAL')
      TYPE 150
150   FORMAT ('0CHECK ACTUAL COMPONENTS (Y/N) ? ',$)
      ACCEPT 160, ANS
160   FORMAT (A1)
      IF (ANS.NE.YES) GOTO 1400
      CALL DCCHK (NST,R8,GAIN)
1400  R(NST,8)=R8
      AV(NST,1)=-GAIN
      AV(NST,2)=20.*(ALOG10(GAIN))
      NTY(NST)=1
      RETURN
      END
```

Table F-4 Subroutine DCCHK Listing

```
      SUBROUTINE DCCHK (NST,R8,GAIN)
C
C     NST = Stage number (2,5) passed from calling subroutine.
C     R8 = Gain setting resistor value passed to calling subroutine.
C     GAIN = Stage gain (V/V) passed to calling subroutine.
C
      LOGICAL*1 ANS,YES
      DATA YES/1HY/
      NLAB=208
      IF (NST.EQ.5) NLAB=408
1000  TYPE 100,NLAB
100   FORMAT (' R',I3,'  (KOHMS) = ?',$)
      ACCEPT 110,R8
110   FORMAT (E12.5)
      GAIN = 10./R8
      DBG=20.*(ALOG10(GAIN))
      TYPE 120,GAIN,DBG
120   FORMAT (' GAIN = ',G11.4,' (V/V)  ',G10.3,' (DB)')
      TYPE 130
130   FORMAT (' REPEAT CHECK (Y/N)?',$)
      ACCEPT 140,ANS
140   FORMAT (A1)
      IF (ANS.EQ.YES) GOTO 1000
      RETURN
      END
```

Table F-5 Subroutine LP Listing

```
      SUBROUTINE LP (NST)
C
C     NST = Stage number (2,3,5) passed from calling program.
C
      COMMON R(5,8),CAP(5,3),AV(5,2),FP(5),DP(5),DUMMY(10),NTY(5)
      LOGICAL*1 ANS,YES
      DATA YES/1HY/
      TWOPI=6.2831853
C     C = Value of fixed capacitor on circuit board in farads.
      C=1.0E-06
C     C2 = Value of added fixed capacitor.
      C2=0.0
C
C     Get values from user:
C
      TYPE 100
100   FORMAT (' SECOND ORDER LOW PASS FILTER')
      TYPE 110
110   FORMAT ('$ADDITIONAL CAPACITORS ADDED (Y/N) ? ')
      ACCEPT 120,ANS
120   FORMAT (A1)
      IF (ANS.NE.YES) GOTO 1500
      TYPE 130
130   FORMAT ('$CAPACITOR VALUE (UFD) (BOTH ASSUMED EQUAL) = ? ')
      ACCEPT 150,C2
      C=C+(C2*1.0E-06)
1500  TYPE 140
```

Table F-5 Subroutine LP Listing (contd)

```
140     FORMAT ('$DC GAIN (V/V) = ? ')
        ACCEPT 150,GAIN
150     FORMAT (E12.5)
        TYPE 160
160     FORMAT (' POLE FREQ (HZ), DAMPING COEFF = ? ',$)
        ACCEPT 170,FPOL,DAMP
170     FORMAT (2E12.5)
C
C       Calculate resistor values (R's in kOhms):
C
        R1=1./(2000.*TWOPI*FPOL*C*DAMP)
        R2=1./(1000.*TWOPI*FPOL*C)
        R3=R2
        R4=1./(1000.*TWOPI*FPOL*C*SQRT(GAIN))
        R6=10./SQRT(GAIN)
        IF (NST.EQ.3) R4=R4/SQRT(GAIN)            !CORRECT FOR LACK OF A4
        IF (NST.EQ.3) R6=0.
C
C       Display resistor values:
C
        NN=NST*100
        IF (NST.EQ.5) NN=400
        TYPE 200,NN+1,R1
200     FORMAT (' R',I3,' = ',G10.3,' KOHMS')
        TYPE 200,NN+2,R2
        TYPE 200,NN+3,R3
        TYPE 200,NN+4,R4
        IF (NST.EQ.3) GOTO 1600
        TYPE 200,NN+6,R6
1600    TYPE 210
210     FORMAT ('0RX01 INFLUENCES DAMPING, RX04 / RX06 GAIN')
        TYPE 220
220     FORMAT ('      NOTE: STAGE INVERTS SIGNAL')
C
C       Check affects of components selected:
C
        TYPE 230
230     FORMAT ('0CHECK ACTUAL COMPONENTS (Y/N) ? ',$)
        ACCEPT 120,ANS
        IF (ANS.NE.YES) GOTO 4000
        CALL LPCHK (NST,R1,R2,R3,R4,R6,C2,GAIN,FPOL,DAMP)
4000    R(NST,1)=R1
        R(NST,2)=R2
        R(NST,3)=R3
        R(NST,4)=R4
        R(NST,6)=R6
        CAP(NST,1)=C2
        CAP(NST,2)=C2
        AV(NST,1)=-GAIN
        IF (NST.EQ.3) AV(NST,1)=GAIN
        AV(NST,2)=20.*(ALOG10(GAIN))
        FP(NST)=FPOL
        DP(NST)=DAMP
        NTY(NST)=2
        RETURN
        END
```

Table F-6 Subroutine LPCHK Listing

```
      SUBROUTINE LPCHK (NST,R1,R2,R3,R4,R6,C2,GAIN,FPOL,DAMP)
C
C     NST = Stage number (2,3,5) passed from calling program.
C     R1-R6 = Resistor values passed to calling program.
C     C2 = Additional capacitor value passed to calling program.
C     GAIN = Stage gain (V/V) passed to calling program.
C     FPOL = Stage pole frequency (Hz) passed to calling program.
C     DAMP = Stage damping coefficient passed to calling program.
C
      TWOPI=6.2831853
      LOGICAL*1 ANS,YES
      DATA YES/1HY/
C
C     Get values from user:
C     C = Value of fixed capacitor on filter board in uF.
C
2000  C=1.
      C2=0.
      GAIN=1.
      NN=NST*100
      IF (NST.EQ.5) NN=400
      TYPE 100,NN+1
100   FORMAT (' R',I3,'   (KOHMS) = ? ',$)
      ACCEPT 110,R1
110   FORMAT (E12.5)
      TYPE 100,NN+2
      ACCEPT 110,R2
      TYPE 100,NN+3
      ACCEPT 110,R3
      TYPE 100,NN+4
      ACCEPT 110,R4
      IF (NST.EQ.3) GOTO 2100
      TYPE 100,NN+6
      ACCEPT 110,R6
2100  TYPE 120
120   FORMAT (' ADDITIONAL CAPACITORS ADDED (Y/N)?',$)
      ACCEPT 130,ANS
130   FORMAT (A1)
      IF (ANS.NE.YES) GOTO 2200
      TYPE 150
150   FORMAT (' CAPACITOR VALUE (BOTH ASSUMED EQUAL) - (UFD)?',$)
      ACCEPT 160,C2
      C=C+C2
C
C     Calculate GAIN, FPOL, and DAMP:
C
2200  GAIN=R3/R4
      IF (NST.EQ.3) R6=10.
      GAIN=GAIN*(10./R6)
2400  DBG=20.*(ALOG10(GAIN))
      TYPE 160,GAIN,DBG
160   FORMAT (' GAIN = ',G11.4,' (V/V)   ',G10.3,' (DB)')
      FPOL=1./(TWOPI*SQRT(1.E-06*R2*R3*C*C))
```

Table F-6 Subroutine LPCHK Listing (contd)

```
        DAMP=(SQRT(R2*R3))/(2.*R1)
        TYPE 170,FPOL,DAMP
170     FORMAT (' POLE FREQ (HZ) = ',G10.3,', DAMPING COEF = ',G10.3)
        TYPE 180
180     FORMAT (' REPEAT CHECK (Y/N)?',$)
        ACCEPT 130,ANS
        IF (ANS.EQ.YES) GOTO 2000
        IF (NST.EQ.3) R6=0.0
        RETURN
        END
```

Table F-7 Subroutine HP Listing

```
        SUBROUTINE HP(NST)
C
C       NST = Stage number (2,5) passed from calling program
C
        COMMON R(5,8),CAP(5,3),AV(5,2),FP(5),DP(5),FZ(5),DZ(5),NTY(5)
        LOGICAL*1 ANS,YES
        DATA YES/1HY/
        TWOPI=6.2831853
C       C = Value of fixed capacitor on circuit board in farads.
        C=1.0E-06
C       C2 = Value of additional capacitor on circuit board in farads.
        C2 =0.
C
C       Get values from user:
C
        TYPE 100
100     FORMAT (' SECOND ORDER HIGH PASS FILTER')
        TYPE 110
110     FORMAT (' ADDITIONAL CAPACITORS ADDED (Y/N)?',$)
        ACCEPT 120,ANS
120     FORMAT (A1)
        IF (ANS.NE.YES) GOTO 1000
        TYPE 130
130     FORMAT (' CAPACITOR VALUE (BOTH ASSUMED EQUAL) - (UFD)?',$)
        ACCEPT 140,C2
140     FORMAT (E12.5)
        C=C+(C2*1.E-06)
1000    TYPE 150
150     FORMAT ('$HI FREQ GAIN (V/V) = ? ')
        ACCEPT 140,GAIN
        TYPE 160
160     FORMAT ('$POLE FREQ (HZ), DAMPING COEFF = ? ')
        ACCEPT 170,FPOLE,DAMPP
170     FORMAT (2E12.5)
C
C       Calculate resistor values (R's in kOhms):
C
        R1=1./(2000.*TWOPI*FPOLE*C*DAMPP)
        R2=1./(1000.*TWOPI*FPOLE*C)
        R3=R2
        R4=1./(2000.*TWOPI*FPOLE*C*DAMPP*GAIN)
        R5=10.
```

Table F-7 Subroutine HP Listing (contd)

```
      R7=20.*DAMPP
      R8=10./GAIN
      FZERO=FPOLE*1.E-04
      DAMPZ=1.
C
C     Display resistor values and hints:
C
      NN=200
      IF (NST.EQ.5) NN=400
      TYPE 200,NN+1,R1
200   FORMAT (' R',I3,' = ',G10.3,' KOHMS')
      TYPE 200,NN+2,R2
      TYPE 200,NN+3,R3
      TYPE 200,NN+4,R4
      TYPE 200,NN+5,R5
      TYPE 200,NN+7,R7
      TYPE 200,NN+8,R8
      TYPE 210
210   FORMAT ('0RX01 / RX05 INFLUENCE DAMPING; RX07 ZERO FREQ;
     + RX08 GAIN')
      TYPE 220
220   FORMAT (' ****** FOR PROPER LOW FREQ ATTEN, RX04*RX07 =
     + RX03*RX08')
      TYPE 230
230   FORMAT (7X,' AND RX01*RX08 > RX04*RX05 ******')
      TYPE 240
240   FORMAT ('0     NOTE: STAGE INVERTS SIGNAL')
C
C     Check affects of components selected:
C
      TYPE 245
245   FORMAT ('0CHECK ACTUAL COMPONENTS  (Y/N) ? ',$)
      ACCEPT 120,ANS
      IF (ANS.NE.YES) GOTO 4000
      CALL HPCHK (NST,R1,R2,R3,R4,R5,R7,R8,C2,
     GAIN,FPOLE,DAMPP,FZERO,DAMPZ)
4000  R(NST,1)=R1
      R(NST,2)=R2
      R(NST,3)=R3
      R(NST,4)=R4
      R(NST,5)=R5
      R(NST,7)=R7
      R(NST,8)=R8
      CAP(NST,1)=C2
      CAP(NST,2)=C2
      AV(NST,1)=-GAIN
      AV(NST,2)=20.*(ALOG10(GAIN))
      FP(NST)=FPOLE
      DP(NST)=DAMPP
      FZ(NST)=FZERO
      DZ(NST)=DAMPZ
      NTY(NST)=3
      RETURN
      END
```

Table F-8 Subroutine HPCHK Listing

```
      SUBROUTINE HPCHK (NST,R1,R2,R3,R4,R5,R7,R8,C2,GAIN,
     +FPOLE,DAMPP,FZERO,DAMPZ)
C
C       NST = Stage number (2,5) passed from calling program.
C       R1-R8 = Resistor values passed to calling program.
C       GAIN = Stage gain (V/V) passed to calling program.
C       FPOLE = Stage pole frequency (Hz) passed to calling program.
C       DAMPP = Stage pole damping coefficient passed to calling program.
C       FZERO = Stage zero frequency (Hz) passed to calling program.
C       DAMPZ= Stage zero damping coefficient passed to calling program.
C
        TWOPI=6.2831853
        LOGICAL*1 ANS,YES
        DATA YES/1HY/
        TWOPI=6.2831853
C       C = Value of fixed capacitor in uF.
        C=1.
C       C2 = Value of additional capacitor in uF.
        C2=0.
C
C       Get values from user:
C
        NN=200
        IF (NST.EQ.5) NN=400
2000    TYPE 240,NN+1
240     FORMAT (' R',I3,'    (KOHMS) = ? ',$)
        ACCEPT 160,R1
160     FORMAT (E12.5)
        TYPE 240,NN+2
        ACCEPT 160,R2
        TYPE 240,NN+3
        ACCEPT 160,R3
        TYPE 240,NN+4
        ACCEPT 160,R4
        TYPE 240,NN+5
        ACCEPT 160,R5
        TYPE 240,NN+7
        ACCEPT 160,R7
        TYPE 240,NN+8
        ACCEPT 160,R8
        TYPE 170
170     FORMAT (' ADDITIONAL CAPACITORS ADDED (Y/N)?',$)
        ACCEPT 180,ANS
180     FORMAT (A1)
        IF (ANS.NE.YES) GOTO 2200
        TYPE 190
190     FORMAT (' CAPACITOR VALUE (BOTH ASSUMED EQUAL) - (UFD)?',$)
        ACCEPT 160,C2
        C=C+C2
C
C       Calculate and display filter parameters:
C
2200    AMULT=1.
        GAIN=10./R8
        DBG=20.*(ALOG10(GAIN))
        TYPE 250,GAIN,DBG
250     FORMAT (' HI FREQ GAIN = ',G11.4,' (V/V)    ',G10.3,' (DB)')
        FPOLE=1./(TWOPI*SQRT(1.E-06*R2*R3*C*C))
```

Table F-8 Subroutine HPCHK Listing (contd)

```
      DAMPP=(SQRT(R2*R3))/(2.*R1)
      RT=(R4*R7)-(R3*R8)
      IF (RT.GT.0.0) GOTO 2100
      AMULT=-1.
      RT=-RT
2100  FZERO=FPOLE*SQRT(RT/(R4*R7))
      DAMPZ=SQRT((R2*R3*R7)/(R4*RT))
      DAMPZ=DAMPZ*((R4*R5)-(R1*R8))/(2.*R1*R5)
      IF (FZERO.GT.(FPOLE*1.E-04)) GOTO 2500
      FZERO=FPOLE*1.E-04
      DAMPZ=1.
2500  FZERO=AMULT*FZERO
      TYPE 260,FZERO,DAMPZ
260   FORMAT (' ZERO FREQ (HZ) = ',G11.4,', ZERO DAMPING COEF = ',G10.3)
      TYPE 265,FPOLE,DAMPP
265   FORMAT (' POLE FREQ (HZ) = ',G10.3,', POLE DAMPING COEF = ',G10.3)
      IF (AMULT.EQ.-1.) TYPE 270
270   FORMAT ('0****** WARNING! POOR LOW FREQ REJECTION - RX03*RX08
     + > RX04*RX07 ******')
      IF (DAMPZ.LT.0.) TYPE 275
275   FORMAT ('0****** WARNING! LOW FREQ PHASE ERROR
     + RX01*RX08 < RX04*RX05 ******')
      TYPE 280
280   FORMAT ('0REPEAT CHECK (Y/N)?',$)
      ACCEPT 180,ANS
      IF (ANS.EQ.YES) GOTO 2000
      RETURN
      END
```

Table F-9 Subroutine BP Listing

```
      SUBROUTINE BP(NST)
C
C     NST = Stage number (2,5) passed from calling program
C
      COMMON R(5,8),CAP(5,3),AV(5,2),FP(5),DP(5),FZ(5),DZ(5),NTY(5)
      LOGICAL*1 ANS,YES
      DATA YES/1HY/
      TWOPI=6.2831853
C     C = Value of fixed capacitor on circuit board in farads.
      C=1.0E-06
C     C2 = Value of additional capacitor in farads.
      C2 = 0.
C
C     Get values from user:
C
      TYPE 100
100   FORMAT (' SECOND ORDER BAND PASS FILTER')
      TYPE 110
110   FORMAT (' ADDITIONAL CAPACITORS ADDED (Y/N)?',$)
      ACCEPT 120,ANS
120   FORMAT (A1)
      IF (ANS.NE.YES) GOTO 1000
      TYPE 130
130   FORMAT (' CAPACITOR VALUE (BOTH ASSUMED EQUAL) - (UFD)?',$)
      ACCEPT 140,C2
```

Table F-9 Subroutine BP Listing (contd)

```
140     FORMAT (E12.5)
        C=C+(C2*1.E-06)
1000    TYPE 150
150     FORMAT ('$CENTER FREQ GAIN (V/V) = ? ')
        ACCEPT 140,GAIN
        TYPE 160
160     FORMAT ('$CENTER FREQ (HZ), DAMPING COEFF = ? ')
        ACCEPT 170,FPOLE,DAMPP
170     FORMAT (2E12.5)
C
C       Calculate resistor values (in kOhms):
C
        R1=1./(2000.*TWOPI*FPOLE*C*DAMPP)
        R2=1./(1000.*TWOPI*FPOLE*C)
        R3=R2
        R4=1./(2000.*TWOPI*FPOLE*(1.+DAMPP)*C*SQRT(GAIN))
        R5=10./SQRT(GAIN)
        FZERO=FPOLE*1.E-04
        DAMPZ=0.
C
C       Display resistor values:
C
        NN=200
        IF (NST.EQ.5) NN=400
        TYPE 200,NN+1,R1
200     FORMAT (' R',I3,' = ',G10.3,' KOHMS')
        TYPE 200,NN+2,R2
        TYPE 200,NN+3,R3
        TYPE 200,NN+4,R4
        TYPE 200,NN+5,R5
        TYPE 210
210     FORMAT ('0RX01 INFLUENCES DAMPING; RX04 / RX05 GAIN')
C
C       Check affects of resistor selection:
C
        TYPE 230
230     FORMAT ('0CHECK ACTUAL COMPONENTS  (Y/N) ? ',$)
        ACCEPT 120,ANS
        IF (ANS.NE.YES) GOTO 4000
        CALL BPCHK (NST,R1,R2,R3,R4,R5,C2,GAIN,FPOLE,
      +DAMPP,FZERO,DAMPZ)
4000    R(NST,1)=R1
        R(NST,2)=R2
        R(NST,3)=R3
        R(NST,4)=R4
        R(NST,5)=R5
        CAP(NST,1)=
        CAP(NST,2)=C
        AV(NST,1)=-GAIN
        AV(NST,2)=20.*(ALOG10(GAIN))
        FP(NST)=FPOLE
        DP(NST)=DAMPP
        FZ(NST)=FZERO
        DZ(NST)=DAMPZ
        NTY(NST)=4
        RETURN
        END
```

Table F-10 Subroutine BPCHK Listing

```
      SUBROUTINE BPCHK (NST,R1,R2,R3,R4,R5,C2,GAIN,FPOLE,
     +DAMPP,FZERO,DAMPZ)
C
C       NST = Stage number (2,5) passed from calling program.
C       R1-R5 = Resistor values passed to calling program.
C       GAIN = Stage gain (V/V) passed to calling program.
C       FPOLE = Stage pole frequency (Hz) passed to calling program.
C       DAMPP = Stage pole damping coefficient passed to calling program.
C       FZERO = Stage zero frequency (Hz) passed to calling program.
C       DAMPZ= Stage zero damping coefficient passed to calling program.
C
        TWOPI=6.2831853
        LOGICAL*1 ANS,YES
        DATA YES/1HY/
        NN=200
        IF (NST.EQ.5) NN=400
C       C = Value of fixed capacitor on board in uF.
        C=1.
C       C2 = Value of additional capacitor in uF.
        C2 = 0.
C
C       Get values from user:
C
1000    TYPE 100,NN+1
100     FORMAT (' R',I3,'   (KOHMS) = ? ',$)
        ACCEPT 110,R1
110     FORMAT (E12.5)
        TYPE 100,NN+2
        ACCEPT 110,R2
        TYPE 100,NN+3
        ACCEPT 110,R3
        TYPE 100,NN+4
        ACCEPT 110,R4
        TYPE 100,NN+5
        ACCEPT 110,R5
        TYPE 120
120     FORMAT (' ADDITIONAL CAPACITORS ADDED (Y/N)?',$)
        ACCEPT 130,ANS
```

Table F-10 Subroutine BPCHK Listing (contd)

```
130     FORMAT (A1)
        IF (ANS.NE.YES) GOTO 1100
        TYPE 140
140     FORMAT (' CAPACITOR VALUE (BOTH ASSUMED EQUAL) - (UFD)?',$)
        ACCEPT 110,C2
        C=C+C2
C
C       Calculate and display filter parameters:
C
1100    GAIN=(10.*R1)/(R4*R5)
        GAIN=GAIN*(SQRT(R2*R3))/(2.*R1+SQRT(R2*R3))
        DBG=20.*(ALOG10(GAIN))
        TYPE 250,GAIN,DBG
250     FORMAT (' CENTER FREQUENCY GAIN = ',G11.4,' (V/V)   ',G10.3,' (DB)')
        FPOLE=1./(TWOPI*SQRT(1.E-06*R2*R3*C*C))
        DAMPP=(SQRT(R2*R3))/(2.*R1)
        FZERO=FPOLE*1.E-04
        DAMPZ=0.
2500    TYPE 260,FZERO
260     FORMAT (' ZERO FREQ (HZ) = ',G11.4)
        TYPE 265,FPOLE,DAMPP
265     FORMAT (' POLE FREQ (HZ) = ',G11.4,', POLE DAMPING COEF = ',G10.3)
        TYPE 270
270     FORMAT (' REPEAT CHECK (Y/N)?',$)
        ACCEPT 130,ANS
        IF (ANS.EQ.YES) GOTO 1000
        RETURN
        END
```

Table F-11 Subroutine BR Listing

```
      SUBROUTINE BR(NST)
C
C     NST = Stage number (2,5) passed from calling program
C
      COMMON R(5,8),CAP(5,3),AV(5,2),FP(5),DP(5),FZ(5),DZ(5),NTY(5)
      LOGICAL*1 ANS,YES
      DATA YES/1HY/
      TWOPI=6.2831853
C     C = Value of fixed capacitor on circuit board, in farads.
      C=1.0E-06
C     C2 = Value of additional capacitor in farads.
      C2 = 0.
C
C     Get values from user:
C
      TYPE 100
100   FORMAT (' SECOND ORDER BAND REJECT FILTER')
      TYPE 110
110   FORMAT (' ADDITIONAL CAPACITORS ADDED (Y/N)?',$)
      ACCEPT 120,ANS
120   FORMAT (A1)
      IF (ANS.NE.YES) GOTO 1000
      TYPE 130
130   FORMAT (' CAPACITOR VALUE (BOTH ASSUMED EQUAL) - (UFD)?',$)
      ACCEPT 140,C2
140   FORMAT (E12.5)
      C=C+(C2*1.E-06)
1000  TYPE 150
150   FORMAT ('$DC GAIN (V/V) = ? ')
      ACCEPT 140,GAIN
      TYPE 160
160   FORMAT ('$ZERO FREQ (HZ) = ? ')
      ACCEPT 140,FZERO
      TYPE 170
170   FORMAT ('$POLE FREQ (HZ), DAMPING COEFF = ? ')
      ACCEPT 180,FPOLE,DAMPP
180   FORMAT (2E12.5)
C     Determine case:
      NCASE=1
      IF (FPOLE.LT.FZERO) NCASE=2
C
C     Calculate resistor values, in kOhms:
C
      R1=1./(2000.*TWOPI*FPOLE*C*DAMPP)
      R2=1./(1000.*TWOPI*FPOLE*C)
      R3=R2
      RT=2000.*TWOPI*(FPOLE**3)*DAMPP*C*GAIN
      R4=(FZERO*FZERO)/RT
      R5=10.
C     Case I (FPOLE equal to or greater than FZERO):
      R6=0.
      RT=ABS((FPOLE*FPOLE)-(FZERO*FZERO))
      R7=(20.*DAMPP*FPOLE*FPOLE)/RT
      IF (NCASE.EQ.1) GOTO 1100
C     Case II (FPOLE less than FZERO):
      R6=R7
      R7=0.0
1100  R8=((FZERO/FPOLE)**2)*(10./GAIN)
C
```

Table F-11 Subroutine BR Listing (contd)

```
C       Display resistor values and hints:
C
        NN=200
        IF (NST.EQ.5) NN=400
        TYPE 200,NN+1,R1
200     FORMAT (' R',I3,' = ',G10.3,' KOHMS')
        TYPE 200,NN+2,R2
        TYPE 200,NN+3,R3
        TYPE 200,NN+4,R4
        TYPE 200,NN+5,R5
        IF (NCASE.EQ.2) GOTO 1200
C       Case I:
        TYPE 200,NN+7,R7
        GOTO 1300
C       Case II:
1200    TYPE 200,NN+6,R6
1300    TYPE 200,NN+8,R8
        TYPE 210
210     FORMAT ('0RX01 INFLUENCES DAMPING; RX08 GAIN')
        TYPE 215
215     FORMAT (' ****** FOR BEST FREQ REJECTION, RX01*RX08 SHOULD
     + EQUAL RX04*RX05 ******')
        IF (NCASE.EQ.1) TYPE 220
220     FORMAT ('0****** FOR PROPER OPERATION, RX04*RX07 >
     +RX03*RX08 ******')
        IF (NCASE.EQ.1) GOTO 1400
        TYPE 225
225     FORMAT (' NOTE: STAGE INVERTS SIGNAL')
C
C       Check affects of components selected:
C
1400    TYPE 230
230     FORMAT ('0CHECK ACTUAL COMPONENTS  (Y/N)?',$)
        ACCEPT 120,ANS
        DAMPZ=-1.
        IF (ANS.NE.YES) GOTO 4000
        CALL BRCHK (-NST,R1,R2,R3,R4,R5,R6,R7,R8,C2,GAIN,
     +FPOLE,DAMPP,FZERO,DAMPZ)
4000    R(NST,1)=R1
        R(NST,2)=R2
        R(NST,3)=R3
        R(NST,4)=R4
        R(NST,5)=R5
        R(NST,6)=R6
        R(NST,7)=R7
        R(NST,8)=R8
        CAP(NST,1)=C2
        CAP(NST,2)=C2
        AV(NST,1)=GAIN
        IF (FPOLE.GE.FZERO) GOTO 4100
        AV(NST,1)=-GAIN
4100    AV(NST,2)=20.*(ALOG10(GAIN))
        FP(NST)=FPOLE
        DP(NST)=DAMPP
        FZ(NST)=FZERO
        DZ(NST)=DAMPZ
        NTY(NST)=5
        RETURN
        END
```

Table F-12 Subroutine BRCHK Listing

```
      SUBROUTINE BRCHK (NST,R1,R2,R3,R4,R5,R6,R7,R8,C2,GAIN,
     +FPOLE,DAMPP,FZERO,DAMPZ)
C
C       NST = Stage number (2,5) passed from calling program.
C             (- value for NST implies FPOLE and FZERO already contain
C             values from calling program).
C       R1-R8 = Resistor values passed to calling program.
C       GAIN = Stage gain (V/V) passed to calling program.
C       FPOLE = Stage pole frequency (Hz) passed to calling program.
C       DAMPP = Stage pole damping coefficient passed to calling program.
C       FZERO = Stage zero frequency (Hz) passed to calling program.
C       DAMPZ= Stage zero damping coefficient passed to calling program.
C
        LOGICAL*1 ANS,YES
        DATA YES/1HY/
        TWOPI=6.2831853
        IF (NST.LT.0) GOTO 1000
C       Get values of FPOLE and FZERO to determine case:
        TYPE 100
100     FORMAT (' NOMINAL POLE FREQ (HZ) = ?',$)
        ACCEPT 110,FPOLE
110     FORMAT (E12.5)
        TYPE 120
120     FORMAT (' NOMINAL ZERO FREQ (HZ) = ?',$)
        ACCEPT 110,FZERO
        GOTO 1020
C       Already have FPOLE and FZERO:
1000    NST=-NST
1020    NCASE=1
        IF (FPOLE.LT.FZERO) NCASE=2
C
C       Get resistor values from user:
C
        NN=200
        IF (NST.EQ.5) NN=400
C       C = Value of fixed capacitor on board, in uF.
2000    C=1.
C       C2 = Value of additional capacitors, in uF.
        C2 = 0.
        AMULT=1.
        TYPE 130,NN+1
130     FORMAT (' R',I3,'   (KOHMS) = ? ',$)
        ACCEPT 110,R1
        TYPE 130,NN+2
        ACCEPT 110,R2
        TYPE 130,NN+3
        ACCEPT 110,R3
        TYPE 130,NN+4
        ACCEPT 110,R4
        TYPE 130,NN+5
        ACCEPT 110,R5
        IF (NCASE.EQ.2) GOTO 1100
        TYPE 130,NN+7
        ACCEPT 110,R7
        R6=0.0
        GOTO 1200
```

Table F-12 Subroutine BRCHK Listing (contd)

```
1100    TYPE 130,NN+6
        ACCEPT 110,R6
        R7=0.0
1200    TYPE 130,NN+8
        ACCEPT 110,R8
        TYPE 140
140     FORMAT (' ADDITIONAL CAPACITORS ADDED (Y/N)?',$)
        ACCEPT 150,ANS
150     FORMAT (A1)
        IF (ANS.NE.YES) GOTO 1220
        TYPE 160
160     FORMAT (' CAPACITOR VALUE (BOTH ASSUMED EQUAL) - (UFD)?',$)
        ACCEPT 110,C2
        C=C+C2
C
C       Calculate and display filter parameters:
C
1220    IF (NCASE.EQ.2) GOTO 1300
C       Case I:
        RTI=(R3*R8)/(R4*R7)
        IF (RTI.LT.1.) GOTO 1250
        AMULT=-1.
1250    GAIN=AMULT*(10./R8)*(1.-RTI)
        GOTO 1400
C       Case II:
1300    RTII=(R3*R8)/(R4*R6)
        GAIN=(10./R8)*(RTII+1.)
1400    DBG=20.*(ALOG10(GAIN))
        TYPE 250,GAIN,DBG
250     FORMAT (' DC GAIN = ',G11.4,' (V/V)    ',G10.3,' (DB)')
        FPOLE=1./(TWOPI*SQRT(1.E-06*R2*R3*C*C))
        DAMPP=(SQRT(R2*R3))/(2.*R1)
        IF (NCASE.EQ.2) GOTO 1500
C       Case I:
        FZERO=SQRT(FPOLE*FPOLE*ABS(1.-RTI))
        GOTO 1600
C       Case II:
1500    FZERO=SQRT(FPOLE*FPOLE*(1.+RTII))
1600    RT=(R1*R8)/(R4*R5)
        DAMPZ=(1.-RT)/(2.E-03*R1*C*TWOPI*FZERO)
        FZERO=AMULT*FZERO
        TYPE 260,FZERO,DAMPZ
260     FORMAT (' ZERO FREQ (HZ) = ',G11.4,' ZERO DAMPING COEF = ',G10.3)
        TYPE 265,FPOLE,DAMPP
265     FORMAT (' POLE FREQ (HZ) = ',G11.4,' POLE DAMPING COEF = ',G10.3)
AMPING COEF = ',G10.3)
        IF (AMULT.EQ.-1.) TYPE 270
270     FORMAT ('0****** WARNING - IMPROPER OPERATION POSSIBLE!
    +RX03*RX08 > RX04*RX07 ******')
        TYPE 280
280     FORMAT ('0MORE CHECKS (Y/N) ? ',$)
        ACCEPT 150,ANS
        IF (ANS.EQ.YES) GOTO 2000
        RETURN
        END
```

Table F-13 Subroutine PRINT Listing

```
      SUBROUTINE PRINT
      COMMON R(5,8),CAP(5,3),AV(5,2),FP(5),DP(5),FZ(5),DZ(5),NTY(5)
      LOGICAL*1 DAT(9),TITLE(40)
C
C     Subroutine DATE is part of DEC's FORTRAN and loads the current
C     date into array DAT.
C
      CALL DATE(DAT)
50    FORMAT ('0','STAGE ',I1,':',20X,'-- GAIN --')
60    FORMAT ('0','STAGE ',I1,':',20X,'-- LOW PASS --')
70    FORMAT ('0','STAGE ',I1,':',20X,'-- HIGH PASS --')
80    FORMAT ('0','STAGE ',I1,':',20X,'-- BAND PASS --')
90    FORMAT ('0','STAGE ',I1,':',20X,'-- BAND REJECT --')
C
C     Print header:
C
      PRINT 100
100   FORMAT ('0',5X,'SDAS SIGNAL CONDITIONING CARD
     +RESISTOR VALUES AND FILTER PARAMETERS')
      TYPE 115
115   FORMAT (' PRINTOUT ID (<40 CHAR)?',$)
      ACCEPT 118,(TITLE(N),N=1,40)
118   FORMAT (40A1)
      PRINT 120,DAT,TITLE
120   FORMAT (1X,9A1,15X,40A1)
C
C     Stage 1:
C
      PRINT 50,1
      PRINT 140,101,R(1,1)
140   FORMAT (1X,T8,'R',I3,' = ',G11.4,' KOHMS')
      PRINT 140,102,R(1,2)
      PRINT 150,(AV(1,N),N=1,2)
150   FORMAT ('0',T16,'DC GAIN = ',G11.4,' (V/V)  [',
     +G10.3,' (DBV)]')
      PRINT 160,FP(1)
160   FORMAT (1X,T16,'SINGLE POLE FREQ = ',G11.4,' HZ')
      AVP=AV(1,1)
      AVS=AV(1,2)
C
C     Stage 2:
C
      GOTO (1100,1200,1300,1400,1500) NTY(2)
1100  PRINT 50,2
      GOTO 1600
1200  PRINT 60,2
      GOTO 1600
1300  PRINT 70,2
      GOTO 1600
1400  PRINT 80,2
      GOTO 1600
1500  PRINT 90,2
1600  CALL RPRINT (2)
```

Table F-13 Subroutine PRINT Listing (contd)

```
      AVP=AVP*AV(2,1)
      AVS=AVS+AV(2,2)
C
C     Stage 3:
C
      PRINT 60,3
      CALL RPRINT (3)
      AVP=AVP*AV(3,1)
      AVS=AVS+AV(3,2)
C
C     Stage 4:
C
      IF (NTY(4).EQ.2) GOTO 2000
      PRINT 50,4
      GOTO 2100
2000  PRINT 60,4
2100  PRINT 440,R(4,1)
440   FORMAT (1X,T8,'R306 = ',G11.4,' KOHMS')
      PRINT 445,R(4,2)
445   FORMAT (1X,T8,'R309 = ',G11.4,' KOHMS')
      IF (CAP(4,1).NE.0.0) PRINT 450,CAP(4,1)
450   FORMAT (1X,T8,'C301 = ',G11.4,' UFD')
      PRINT 150,(AV(4,N),N=1,2)
      IF(FP(4).NE.0.) PRINT 250,FP(4)
250   FORMAT (1X,T16,'POLE FREQ = ',G11.4,' HZ')
      AVP=AVP*AV(4,1)
      AVS=AVS+AV(4,2)
C
C     Stage 5:
C
      GOTO (3100,3200,3300,3400,3500) NTY(5)
3100  PRINT 50,5
      GOTO 3600
3200  PRINT 60,5
      GOTO 3600
3300  PRINT 70,5
      GOTO 3600
3400  PRINT 80,5
      GOTO 3600
3500  PRINT 90,5
3600  CALL RPRINT (5)
      AVP=AVP*AV(5,1)
      AVS=AVS+AV(5,2)
      PRINT 600,AVP,AVS
600   FORMAT ('0','TOTAL FILTER GAIN = ',G11.4,' (V/V) ',G10.3,' (DBV)')
      PRINT 610
610   FORMAT (5X,'(CAUTION: TOTAL GAIN IS SIMPLE PRODUCT. CHECK
     + FILTER TYPE ')
      PRINT 620
620   FORMAT (5X,'TO DETERMINE ACTUAL COMPOSITE GAIN.)')
      IF(AVP.LT.0.) PRINT 630
630   FORMAT (' FILTER INVERTS SIGNAL')
      RETURN
      END
```

Table F-14 Subroutine RPRINT Listing

```
      SUBROUTINE RPRINT (NST)
C
C     NST = Stage number (2,3,5) passed from calling program.
C
      COMMCN R(5,8),CAP(5,3),AV(5,2),FP(5),DP(5),FZ(5),DZ(5),NTY(5)
C
      NN=NST*100
      IF (NST.EQ.5) NN=400
C
C     Print resistor values:
C
      DO 1000,N=1,8
      IF(R(NST,N).EQ.0.) GOTO 1000
      PRINT 100,NN+N,R(NST,N)
100   FORMAT (1X,T8,'R',I3,' = ',G11.4,' KOHMS')
1000  CONTINUE
C
C     Print capacitor values:
C
      NUM=NST
      IF (NST.EQ.2) NUM=1
      PRINT 110,NUM,CAP(NST,1)
110   FORMAT (1X,T8,'C',I1,'' = ',G11.4,' UFD')
      PRINT 110,NUM+1,CAP(NST,2)
C
C     Print resistor effects hints:
C
1150  GOTO (2000,1200,1300,1400,1500) NTY(NST)
1200  PRINT 130
130   FORMAT (12X,'RX01 CHANGES DAMPING; RX04 / RX06 GAIN')
      GOTO 2000
1300  PRINT 140
140   FORMAT (12X,'RX01 / RX05 CHANGE DAMPING; RX07 ZERO FREQ;
     + RX08 GAIN')
      PRINT 145
145   FORMAT (14X,'****** FOR BEST LOW FREQ PERFORMANCE,
     + RX04*RX07 = RX03*RX08')
      PRINT 148
148   FORMAT (21X,'AND RX01*RX08 < RX04*RX05 ******')
      GOTO 2000
1400  PRINT 150
150   FORMAT (12X,'RX01 CHANGES DAMPING; RX04 / RX05 GAIN')
      GOTO 2000
1500  PRINT 160
160   FORMAT (12X,'RX01 CHANGES DAMPING; RX08 GAIN')
      PRINT 165
165   FORMAT (14X,'****** FOR BEST FREQ REJECTION, RX01*RX08
     + = RX04*RX05 ******')
      TEMP=ABS(FZ(NST))
      IF (FP(NST).GT.TEMP) PRINT 168
168   FORMAT (14X,'****** FOR PROPER OPERATION, RX04*RX07
     + > RX03*RX08 ******')
C
C     Print stage gain:
C
2000  IF (NTY(NST).EQ.3) GOTO 2100
      IF (NTY(NST).EQ.4) GOTO 2200
      PRINT 170,(AV(NST,N),N=1,2)
170   FORMAT ('0',T16,'DC GAIN = ',G11.4,' (V/V)   [',
     +G10.3,' (DBV)]')
```

Table F-14 Subroutine RPRINT Listing (contd)

```
      GOTO 2300
2100  PRINT 180,(AV(NST,N),N=1,2)
180   FORMAT ('0',T16,'HI FREQ GAIN = ',G11.4,' (V/V)   [',
     +G10.3,' (DBV)]')
      GOTO 2300
2200  PRINT 190,(AV(NST,N),N=1,2)
190   FORMAT ('0',T16,'ZERO FREQ GAIN = ',G11.4,' (V/V)   [',
     +G10.3,' (DBV)]')
C
C     Print pole, zero, and damping coefficient information:
C
2300  IF(FP(NST).EQ.0.) GOTO 3000
C     POLES
      IF(DP(NST).NE.0.) GOTO 2400
      PRINT 200,FP(NST)
200   FORMAT (1X,T16,'SINGLE POLE FREQ = ',G11.4,' HZ')
      GOTO 3000
2400  IF (DP(NST).EQ.-1.) GOTO 2500
      PRINT 210,FP(NST),DP(NST)
210   FORMAT (1X,T16,'DOUBLE POLE FREQ = ',G11.4,' HZ; DAMPING COEFF = '
     +,G10.3)
      GOTO 3000
2500  PRINT 220,FP(NST)
220   FORMAT (1X,T16,'COMPLEMENTARY POLE PAIR FREQ = ',G11.4,' HZ')
C     ZEROS
3000  IF (FZ(NST).EQ.0.) GOTO 4000
      IF (DZ(NST).NE.0.) GOTO 3100
      PRINT 300,FZ(NST)
300   FORMAT (1X,T16,'SINGLE ZERO FREQ = ',G11.4,' HZ')
      GOTO 4000
3100  IF (DZ(NST).EQ.-1.) GOTO 3200
      PRINT 310,FZ(NST),DZ(NST)
310   FORMAT (1X,T16,'DOUBLE ZERO FREQ = ',G11.4,' HZ; DAMPING COEFF = '
     +,G10.3)
      GOTO 4000
3200  PRINT 320,FZ(NST)
320   FORMAT (1X,T16,'COMPLEMENTARY ZERO PAIR FREQ = ',G11.4,' HZ')
4000  RETURN
      END
```

Table F-15 Disk File Loading Program Listing

```
      PROGRAM CREATE
      LOGICAL*1 TITLE(13)
      DIMENSION TEMP(104)
      TYPE 10
10    FORMAT ('$DISK FILE NAME (FORM: DXN:XXXXX.YYY) ? ')
      ACCEPT 20,TITLE
20    FORMAT (13A1)
      CALL ASSIGN (2,TITLE,13,'NEW')
      DEFINE FILE 2 (16,208,U,NCH)
      DO 100 N=1,104
      TEMP(N) = 0.0
100   CONTINUE
      NCH=1
      DO 200 N=1,16
      WRITE (2'NCH) TEMP
200   CONTINUE
      END
```

Table F-16 Subroutine STORE Listing

```
      SUBROUTINE STORE
C
      COMMON DUMMY(55),AV(5,2),FP(5),DP(5),FZ(5),DZ(5),NTYP(5)
      COMMON /SPECS/SENS(3,3), PREAM(5,3), FILT(5,5,3), UNITS
      LOGICAL*1 TITLE(13),UNITS(16),NULL
      DATA NULL/1H /
C
C     Get file name and channel (record) number:
C
      TYPE 100
100   FORMAT ('$DISK FILE NAME (FORM:DXN:XXXXX.YYY) ? ')
      ACCEPT 110,TITLE
110   FORMAT (13A1)
      TYPE 120
120   FORMAT ('$CHANNEL NUMBER (1-16) = ? ')
      ACCEPT 130,NCH
130   FORMAT (I2)
C
C     Load COMMON /SPECS/ from file:
C
      CALL SPECFI (2,NCH,NSTA,TITLE)
      NCH=NCH-1
      IF (NSTA.NE.0) GOTO 2000
C
C     Blank channel (record); clear COMMON /SPECS/:
C
      DO 1000 N=1,3
      DO 1000 M=1,5
      SENS (N,M) = 0.
1000  CONTINUE
      DO 1100 N=1,5
      DO 1100 M=1,5
      PREAM (N,M) = 0.
1100  CONTINUE
      DO 1200 M=1,16
      UNITS(M)=NULL
1200  CONTINUE
      DO 1300 M=1,5
      DO 1300 N=1,5
      DO 1300 NN=1,3
      FILT(M,N,NN)=0.0
1300  CONTINUE
C
C     Check which stages have filter parameters stored in them
C     and load the parameters into COMMON /SPECS/:
C
2000  DO 7000 M=1,5
      IF (AV(M,1).EQ.0.) GOTO 7000
C     Clear FILTER array for stage with parameters:
      DO 2100 N=1,5
      DO 2100 NN=1,3
      FILT (M,N,NN)=0.0
2100  CONTINUE
```

Table F-16 Subroutine STORE Listing (contd)

```
C
C       Load FILTER with parameters:
C
C       Stage gains:
C
        GAIN=AV(M,2)
        IF (NTYP(M).EQ.3) GOTO 3100
        IF (NTYP(M).EQ.4) GOTO 3200
        GOTO 3300
C       Change highpass gain to dc gain:
3100    GAIN=GAIN-40.*ALOG10(FP(M)/ABS(FZ(M)))
        GOTO 3300
C       Change bandpass gain to dc gain:
3200    GAIN=GAIN-20.*ALOG10(FP(M)/ABS(FZ(M)))
        GAIN=GAIN+20.*ALOG10((200.+200.*DP(M))/(100.1+2.*DP(M)))
3300    FILT(M,1,1)=1.
        FILT(M,1,2)=GAIN
        FILT(M,1,3)=0.
        IF (AV(M,1).LT.0.) FILT(M,1,3)=180.
C
C       Pole frequencies and damping coefficients:
C
        NEL=2.
        IF (FP(M).E).0.) GOTO 4200
        IF (DP(M).NE.0.) GOTO 4100
        FILT(M,NEL,1)=2.
        FILT(M,NEL,2)=FP(M)
        FILT(M,NEL,3)=0.
        NEL=NEL+1
        GOTO 4200
4100    FILT(M,NEL,1)=3.
        FILT(M,NEL,2)=FP(M)
        FILT(M,NEL,3)=DP(M)
        IF (DP(M).EQ.-1.) FILT(M,NEL,3)=0.
        NEL=NEL+1
4200    CONTINUE
C
C       Zero frequencies and damping coefficients:
C
        IF (FZ(M).EQ.0.) GOTO 5200
        IF (DZ(M).NE.0.) GOTO 5100
        FILT(M,NEL,1)=4.
        FILT(M,NEL,2)=FZ(M)
        FILT(M,NEL,3)=0.
        NEL=NEL+1
        GOTO 5200
5100    FILT(M,NEL,1)=5.
        FILT(M,NEL,2)=FZ(M)
        FILT(M,NEL,3)=DZ(M)
        IF (DZ(M).EQ.-1.) FILT(M,NEL,3)=0.
        NEL=NEL+1
5200    CONTINUE
7000    CONTINUE
C
C       Store COMMON /SPECS/ in file:
```

Table F-16 Subroutine STORE Listing (contd)

```
C
      CALL SPECFI (3,NCH,NSTA,TITLE)
      NCH=NCH-1
C
C     Note file and channel on printout:
C
      PRINT 140,TITLE,NCH
140   FORMAT ('ØRESULTS STORED IN FILE ',13A1,'  CHANNEL ',I2)
      RETURN
      END
```

Table F-17 COMMON /SPECS/ Definitions

COMMON definition statement:

COMMON /SPECS/ SENS(3,3), PREAM(5,3), FILT(5,5,3), UNITS

Where:

SENS (3,3) = Parameters of sensor
PREAM (5,3) = Parameters of preamplifier
FILT (5,5,3) = Parameters of signal conditioning card
UNITS = Units of sensor (e.g. /IN/SEC)
(UNITS is a LOGICAL*1 15-element array)

Array definitions:

SENS(Y,Z), PREAM(Y,Z), FILT(X,Y,Z)

Where:

X = Stage on signal conditioning card

Y = Parameter number

Z = Parameter identifier/data as follows
(For FILT, same pattern used for each X):

Y,1 = Type of parameter

Ø = Ignore
1 = Ø Hz gain/phase
2 = Single pole
3 = Double pole
4 = Single zero
5 = Double zero

Y,2 = Ø Hz gain (dB) / pole/zero frequency (Hz)
Y,3 = Ø Hz phase (deg) / pole/zero damping coefficient

Table F-18 Subroutine SPECFI Listing

```
      SUBROUTINE SPECFI(NFUN,NCH,NSTA,TITLE)
C
C     NFUN = Function ID passed from calling program:
C          1 = Create and write COMMON /SPECS/ into new file.
C          2 = Load COMMON /SPECS/ from old file.
C          3 = Write COMMON /SPECS/ into old file.
C     NCH  = Channel number (1-16) to be written/read passed from
C            calling program. NCH + 1 passed to calling program upon
C            exit.
C     NSTA = Record status passed to calling program.
C          0 = Blank record.
C          1 = Data in record.
C     TITLE = File name (13 element LOGICAL*1 array; form: XXX:YYYYY.ZZZ)
C
      COMMON /SPECS/SENS(3,3),PREAM(5,3),FILT(5,5,3),UNITS
      LOGICAL*1 TITLE(13),UNITS(16)
      EQUIVALENCE (UNITS,TEM1)
      DIMENSION TEMP(104),ZERO(104),TEM1(4)
      NSTA=1
C
C     Open file:
C
      IF(NFUN.EQ.1) GOTO 1000
      CALL ASSIGN(2,TITLE,13,'OLD')
      GOTO 1100
1000  CALL ASSIGN(2,TITLE,13,'NEW')
1100  DEFINE FILE 2 (16,208,U,NCH)
      GOTO (3000,2000,3000),NFUN
C
C     Read from file to COMMON /SPECS/ via array TEMP (NFUN = 2):
C
2000  READ(2'NCH) TEMP
      NSTA=TEMP(1)
      NCNT=2
      DO 2200 J=1,3
      DO 2200 K=1,3
      SENS(J,K)=TEMP(NCNT)
      NCNT=NCNT+1
2200  CONTINUE
      DO 2300 J=1,5
      DO 2300 K=1,3
      PREAM(J,K)=TEMP(NCNT)
      NCNT=NCNT+1
2300  CONTINUE
      DO 2400 J=1,5
      DO 2400 K=1,5
      DO 2400 L=1,3
      FILT(J,K,L)=TEMP(NCNT)
      NCNT=NCNT+1
2400  CONTINUE
      DO 2500 N=1,4
      TEM1(N)=TEMP(NCNT)
      NCNT=NCNT+1
```

Table F-18 Subroutine SPECFI Listing (contd)

```
2500    CONTINUE
        GOTO 4000
C
C       Write to file from COMMON /SPECS/ via array TEMP (NFUN = 1,3):
C
3000    TEMP(1)=NSTA
        NCNT=2
        DO 3100 J=1,3
        DO 3100 K=1,3
        TEMP(NCNT)=SENS(J,K)
        NCNT=NCNT+1
3100    CONTINUE
        DO 3200 J=1,5
        DO 3200 K=1,3
        TEMP(NCNT)=PREAM(J,K)
        NCNT=NCNT+1
3200    CONTINUE
        DO 3300 J=1,5
        DO 3300 K=1,5
        DO 3300 L=1,3
        TEMP(NCNT)=FILT(J,K,L)
        NCNT=NCNT+1
3300    CONTINUE
        DO 3350 N=1,4
        TEMP(NCNT)=TEM1(N)
        NCNT=NCNT+1
3350    CONTINUE
        IF(NFUN.EQ.1) GOTO 3400
        WRITE(2'NCH) TEMP
        GOTO 4000
C       Fill rest of file with zeroes (NFUN = 1):
3400    DO 3500 N=1,100
        ZERO(N)=0.
3500    CONTINUE
        IF(NCH.NE.1) GOTO 3700
        WRITE(2'NCH) TEMP
        DO 3600 N=1,15
        WRITE(2'NCH) ZERO
3600    CONTINUE
        GOTO 4000
3700    M=NCH
        NCH=1
3800    WRITE(2'NCH) ZERO
        IF(NCH.NE.M) GOTO 3800
        WRITE(2'NCH) TEMP
3900    IF(NCH.EQ.17) GOTO 4000
        WRITE(2'NCH) ZERO
        GOTO 3900
C
C       Close file:
C
4000    CALL CLOSE (2)
        RETURN
        END
```

Appendix G

Signal Conditioning Circuit Card Analysis Software

G.1 PROGRAM OVERVIEW

The following sections list the signal conditioning card analysis software. The standalone system computer was used for all software development. This software was written in FORTRAN (Digital Equipment Company [DEC] FORTRAN IV, version V01C-3A) running under DEC's RT-11 operating system (RT-11FB, version V02C-02B).

The program uses user-entered component values to calculate the filter parameters for a signal conditioning card. After the parameters are calculated, they are displayed on the system console for the user. Hints on component effects and warnings for values causing performance degradation (see Appendix D) are also displayed. The program then allows the user to reenter component values for error correction. After component values are settled on, the program prints out a table of component values and filter parameters for the card to aid in board configuration documentation. Finally, the program can store the complete card filter parameters in a floppy disk file for use by other programs.

In all its calculations, the program assumes 10KΩ values for the fixed resistors associated with the filter stages. It also assumes 1.0 μF values for all fixed capacitors. However, since capacitor values can be changed (either by replacement or, in the case of stage 3, by adding a second capacitor in parallel with the fixed ones), the program asks if additional capacitors are added. If a "Y" reply is given to the question, the capacitor value is asked for. Since the entered value is added to the fixed value, a smaller capacitor can be reflected by entering (as a negative value) the difference between 1.0 μF and the value used on the card.

Equations used in this program are covered in Appendix D. Since the program was designed for low frequency filter designs with moderate stage gains, no allowances for parasitics or amplifier gain-bandwidth product limitations are included in it.

This program consists of a main program with nine subroutines. The main program contains all user interfaces; it relies on subroutines to perform the actual calculations and data printouts. Both the main program and the subroutines use a COMMON block to store component values and filter parameters. This block is defined in Appendix F, Section F.2.

G.2 MAIN ANALYSIS PROGRAM

The main program handles overall communications with the user. It calculates the filter parameters for stages 1 and 4. Subroutines are called to handle calculations for stages 2, 3, and 5 as well as for table printout and disk filter parameter storage.

Table G-1 contains the main parameter calculation program.

G.3 SUBROUTINE VDC

This subroutine calculates stage gain for stage 2 or 5 when that stage is not used as a filter. It accepts resistor values from the user and calculates the gain. After displaying the result, it allows the user to reenter the values to correct errors. When satisfactory values are reached, the program stores the resistor values and stage gain in COMMON and returns to the calling program.

Table G-2 contains this subroutine.

G.4 SUBROUTINE VLP

This subroutine is called by the main program to calculate the lowpass filter parameters from user-entered resistor and capacitor values for stages 2, 3, and 5. After calculating and displaying the resulting filter parameters, the program allows the user to reenter values to correct errors. (See Section D.2.2 of Appendix D for a discussion of the equations used in this routine.) When satisfactory values are reached, the program stores the resistor values and stage parameters in COMMON and returns to the calling program.

Table G-3 contains this subroutine.

G.5 SUBROUTINE VHP

This subroutine is called by the main program to calculate the highpass filter parameters from user-entered resistor and capacitor

values for stages 2 or 5. (See Section D.4.2 of Appendix D for a discussion of the equations implemented in this subroutine.) The filter's reponse is modeled by a double pole at FPOLE and a double zero at the greater of the calculated FPOLE/10,000. (This modeling of FZERO is used to ease calculations in programs to calculate system transfer function responses.) After calculating and displaying the resulting filter parameters, the program allows the user to reenter values to correct errors. Should a negative value of ωz result from the calculations, a message to the user is displayed warning of improper filter response as discussed in Section D.4.2. (Such a value is also indicated by a negative frequency pole frequency in the display and array.) When satisfactory values are reached, the program stores the resistor values and stage parameters in COMMON and returns to the calling program.

Table G-4 contains the listing for this subroutine.

G.6 SUBROUTINE VBP

This subroutine is called by the main program to calculate the bandpass filter parameters from user-entered resistor and capacitor stages 2 or 5. (See Section D.5.2 of Appendi: D for a discussion of the equations implemented in this subroutine.) The filter's reponse is modeled by a double pole at FPOLE and a single zero at FPOLE/10,000. (This modeling of FZERO is used to ease calculations in programs to calculate system transfer function responses.) After calculating and displaying the resulting filter parameters, the program allows the user to reenter values to correct errors. When satisfactory values are reached, the program stores the resistor values and stage parameters in COMMON and returns to the calling program.

Table G-5 contains this subroutine.

G.7 SUBROUTINE VBR

This subroutine is called by the main program to calculate the band reject filter parameters from user-entered resistor values for stages 2 or 5. (See Section D.6.1.2 and D.6.2.2 of Appendix D for a discussion of the equations implemented in this subroutine.) VBR initially asks for nominal pole and zero frequency values to determine the proper case for the filter. It then accepts the relevant component values. After calculating and displaying the resulting filter parameters, the program allows the user to reenter values to correct errors. The program also checks for a negative damping coefficient and for a negative ωz value as discussed in Sections D.6.1.2 and D.6.2.2 of Appendix D. If such a value is detected, a message is displayed on the system console to alert the user. When satisfactory values are reached, the program stores the resistor values and stage parameters in COMMON and returns to the calling program.

Table G-6 contains this subroutine.

G.8 SUBROUTINE VPRINT

This subroutine prints on the line printer a table of resistor values and filter parameters. A user-entered title is added to the printout to allow positive identification. The routine used subroutine VRPRIN to print out the tables for stages 2, 3, and 5. The total conditioning card gain is calculated and printed out at the bottom of the page. The value printed is a simple total and thus may not reflect the actual card gain at a given frequency.

Table G-7 contains subroutine VPRINT.

G.9 SUBROUTINE VRPRIN

This subroutine is called by subroutine VPRINT to print resistor and filter parameter values for stages 2, 3, and 5.

Table G-8 contains this subroutine.

G.10 SUBROUTINES STORE AND SPECFI

These subroutines handle the storage of filter parameter values in a floppy disk file. They are fully documented in Appendix F, *Sections F.15 and F.16*.

Table G-1 FCHECK - Main Program Listing

```
      PROGRAM FILTER CARD RESISTOR VERIFICATION
      COMMON R(5,8),CAP(5,3),AV(5,2),FP(5),DP(5),FZ(5),DZ(5),NTY(5)
      LOGICAL*1 ANS,YES
      DATA YES/1HY/
      TWOPI=6.2831853
      TYPE 100
100   FORMAT (' SDAS SIGNAL CONDITIONING CARD ANALYSIS PROGRAM')
C
C     Clear common; reentrant point for recalculating entire board:
C
1000  DO 1300 N=1,5
      DO 1200 M=1,8
      R(N,M)=0.
1200  CONTINUE
      CAP(N,1)=0.
      CAP(N,2)=0.
      CAP(N,3)=0.
      AV(N,1)=0.
      AV(N,2)=0.
      FP(N)=0.
      DP(N)=0.
      FZ(N)=0.
      DZ(N)=0.
1300  CONTINUE
C
C     Begin. The program asks for the stage to be calculated and
C     then jumps to that stage.
C
      TYPE 110
110   FORMAT ('0 STAGE TO BE ENTERED (0=ENTIRE BOARD)?',$)
      ACCEPT 120,NST
120   FORMAT (I1)
      NST=NST+1
1400  GOTO (1500,1500,2000,3000,4000,5000) NST
C
C     Stage 1. Stage 1 can only be used for gain. The program requests the
C     resistor values for the stage and calculates the stage gain.  After
C     displaying the gain, it requests a value for the stage pole frequency.
C     This frequency is determined by values of the stage frequency-limiting
C     components on the circuit board and must be determined by the user.
```

Table G-1 FCHECK - Main Program Listing (contd)

```
C     (If no value is desired, 0.0 can be entered.) The program allows
C     all component values to be reentered in case an error was made on the
C     first try. When satisfactory values have been entered, the program
C     stores the component and parameter values in the proper COMMON
C     locations.  If the entire board is not being designed, the program
C     jumps to the closeout section; otherwise, the next stage is designed.
C
1500  TYPE 130
130   FORMAT (' STAGE 1:')
1600  TYPE 140
140   FORMAT ('$R101 (KOHMS) = ? ')
      ACCEPT 150,RG
150   FORMAT (E12.5)
      TYPE 160
160   FORMAT ('$R102 (KOHMS) = ? ')
      ACCEPT 150,RS
      GAIN=RS/RG
      DBG=20.*(ALOG10(GAIN))
      TYPE 170,GAIN,DBG
170   FORMAT (' DC GAIN = ',G11.4,' (V/V)   [',G10.3,' (DBV)]')
      TYPE 185
185   FORMAT ('$POLE FREQ (HZ) = ? ')
      ACCEPT 150,FREQ
      TYPE 180
180   FORMAT ('0ENTER AGAIN (Y/N) ? ',$)
      ACCEPT 190,ANS
190   FORMAT (A1)
      IF (ANS.EQ.YES) GOTO 1600
      R(1,1)=RG
      R(1,2)=RS
      FP(1)=FREQ
      AV(1,1)=GAIN
      AV(1,2)=20.*(ALOG10(GAIN))
      NTY(1)=2
      IF (NST.NE.1) GOTO 6000
C
C     Stage 2.  This stage can be used for any type of filter. The
C     program accepts the filter type and then calls the appropriate sub-
C     routine to perform the actual calculations.  If the entire board is
C     not being designed, the program jumps to the closeout section;
```

Table G-1 FCHECK - Main Program Listing (contd)

```
C     otherwise, the next stage is designed.
C
2000 TYPE 200
200   FORMAT (' STAGE 2:')
2100 TYPE 210
210   FORMAT (1X, 'FILTER TYPE (NONE=0, LP=1, HP=2, BP=3, BR=4)?',$)
      ACCEPT 120,NTYP
      NTYP=NTYP+1
      GOTO (2200,2300,2400,2500,2600) NTYP
      GOTO 2100       !REPEAT ABOVE IF GOTO OUT OF RANGE
2200 CALL VDC(2)
      GOTO 2900
2300 CALL VLP(2)
      GOTO 2900
2400 CALL VHP(2)
      GOTO 2900
2500 CALL VBP(2)
      GOTO 2900
2600 CALL VBR(2)
2900 IF (NST.NE.1) GOTO 6000
C
C     Stage 3.  This stage can only be used as a lowpass filter.
C     If the entire board is not being designed,  after subroutine return
C     the program jumps to the closeout section; otherwise, the next stage
C     is designed.

3000 TYPE 300
300   FORMAT (' STAGE 3:')
      CALL VLP(3)
      IF (NST.NE.1) GOTO 6000
C
C     Stage 4.  This stage can be used for gain or for gain and a single
C     lowpass pole only. The program accepts the stage's resistor values
C     and calculates the stage gain. After displaying the stage gain on the
C     system console, the program requests a capacitor value for the stage.
C     (If none is used, a 0.0 should be entered.) If a capacitor is used,
C     the program calculates and displays the pole frequency. It then
C     provides an opportunity for the user to reenter stage values for
C     error correction. After satisfactory values have been entered, the
C     program stores the component and parameter values in the proper COMMON
```

Table G-1 FCHECK - Main Program Listing (contd)

```
C     locations.  If the entire board is not being designed, the program
C     jumps to the closeout section; otherwise, the next stage is designed.
C
4000  TYPE 400
400   FORMAT (' FOURTH STAGE:')
4100  TYPE 410
410   FORMAT ('$R306 (KOHMS) = ? ')
      ACCEPT 150,R1
      TYPE 420
420   FORMAT ('$R309 (KOHMS) = ? ')
      ACCEPT 150,RF
      GAIN=RF/R1
      DBG=20.*(ALOG10(GAIN))
      FREQ=0.
      TYPE 430
430   FORMAT ('$C301 (UFD) (=0. IF NOT USED) = ? ')
      ACCEPT 150,C
      TYPE 170,GAIN,DBG
      TYPE 440
440   FORMAT (5X,'NOTE: STAGE INVERTS SIGNAL')
      IF (C.EQ.0.) GOTO 4200
      FREQ=1000./(TWOPI*C*RF)
      TYPE 450,FREQ
450   FORMAT (' POLE FREQ = ',G11.4,' HZ')
4200  TYPE 180
      ACCEPT 190,ANS
      IF (ANS.EQ.YES) GOTO 4100
      R(4,1)=R1
      R(4,2)=RF
      CAP(4,1)=C
      AV(4,1)=-GAIN
      AV(4,2)=20.*(ALOG10(GAIN))
      FP(4)=FREQ
      DP(4)=0.
      NTY(4)=1
      IF (FREQ.NE.0.) NTY(4)=2
      IF (NST.NE.1) GOTO 6000
C
C     Stage 5.  This stage can be used for any type of filter. The
C     program accepts the filter type and then calls the appropriate sub-
```

Table G-1 FCHECK - Main Program Listing (contd)

```
C     routine to perform the actual calculations.
C
5000 TYPE 500
500  FORMAT (' STAGE 5:')
5100 TYPE 210
     ACCEPT 120,NTYP
     NTYP=NTYP+1
     GOTO (5200,5300,5400,5500,5600) NTYP
     GOTO 5100 ! REPEAT ABOVE IF GOTO OUT OF RANGE
5200 CALL VDC(5)
     GOTO 6000
5300 CALL VLP(5)
     GOTO 6000
5400 CALL VHP(5)
     GOTO 6000
5500 CALL VBP(5)
     GOTO 6000
5600 CALL VBR(5)
C
C     Closeout section. This section allows the user to change any
C     stage in case of error or changed specifications. This change will
C     affect only the stage selected; all other stage's component and
C     parameter values stored in COMMON will be unchanged. Once all
C     stages are satisfactory, the program allows the user the
C     options of printing out a table of component values and of
C     storing stage parameters (SPECS) in a floppy disk file.
C     Finally, the program allows the user the option of restarting
C     the program to design a new filter card.
C
6000 TYPE 600
600  FORMAT ('0ANY CHANGES (Y/N)?',$)
     ACCEPT 190,ANS
     IF (ANS.NE.YES) GOTO 7000
     TYPE 610
610  FORMAT (' STAGE TO BE CHANGED?',$)
     ACCEPT 120,NST
     NST=NST+1
     GOTO 1400
7000 TYPE 620
```

Table G-1 FCHECK - Main Program Listing (contd)

```
620  FORMAT (' RESISTOR AND PARAMETER PRINTOUT (Y/N)?',$)
     ACCEPT 190,ANS
     IF (ANS.EQ.YES) CALL VPRINT
7100 TYPE 630
630  FORMAT ('$STORE PARAMETERS ON DISK (Y/N) ? ')
     ACCEPT 190,ANS
     IF (ANS.NE.YES) GOTO 7200
     CALL STORE
     GOTO 7100
7200 PRINT 640
640  FORMAT ('1')
     CALL CLOSE (6)
     TYPE 650
650  FORMAT (' RERUN PROGRAM (Y/N)?',$)
     ACCEPT 190,ANS
     IF(ANS.EQ.YES) GOTO 1000
     END
```

Table G-2 Subroutine VDC Listing

```
      SUBROUTINE VDC (NST)
C
C     NST = Stage number (2,5) passed from calling program.
C
      COMMON R(5,8),CAP(5,3),AV(5,2),DUMMY(20),NTY(5)
      LOGICAL*1 ANS,YES
      DATA YES/1HY/
      TYPE 100
100   FORMAT (' GAIN ONLY')
      NLAB=208
      IF (NST.EQ.5) NLAB=408
1000  TYPE 110,NLAB
110   FORMAT ('$R',I3,'  (KOHMS) = ? ')
      ACCEPT 120,R8
120   FORMAT (E12.5)
      GAIN = 10./R8
      DBG=20.*(ALOG10(GAIN))
      TYPE 130,GAIN,DBG
130   FORMAT (' DC GAIN = ',G11.4,' (V/V)   [',G10.3,' (DB)]')
      TYPE 140
140   FORMAT ('0NOTE: STAGE INVERTS SIGNAL')
      TYPE 150
150   FORMAT (' REPEAT CHECK (Y/N)?',$)
      ACCEPT 160,ANS
160   FORMAT (A1)
      IF (ANS.EQ.YES) GOTO 1000
      R(NST,8)=R8
      AV(NST,1)=-GAIN
      AV(NST,2)=20.*(ALOG10(GAIN))
      NTY(NST)=1
      RETURN
      END
```

Table G-3 Subroutine VLP Listing

```
      SUBROUTINE VLP(NST)
C
C     NST = Stage number (2,3,5) passed from calling program.
C
      COMMON R(5,8),CAP(5,3),AV(5,2),FP(5),DP(5),DUMMY(10),NTY(5)
      LOGICAL*1 ANS,YES
      DATA YES/1HY/
      TWOPI=6.2831853
      C2=0.0
      TYPE 100
100   FORMAT (' SECOND ORDER LOW PASS FILTER')
C     C = Value of fixed capacitors in uF.
1000  C=1.
      GAIN=1.
      NN=NST*100
      IF (NST.EQ.5) NN=400
C
C     Get values from user:
C
      TYPE 110,NN+1
```

Table G-3 Subroutine VLP Listing (contd)

```
110   FORMAT ('$R',I3,'   (KOHMS) = ? ')
      ACCEPT 120,R1
120   FORMAT (E12.5)
      TYPE 110,NN+2
      ACCEPT 120,R2
      TYPE 110,NN+3
      ACCEPT 120,R3
      TYPE 110,NN+4
      ACCEPT 120,R4
      IF (NST.EQ.3) GOTO 1100
      TYPE 110,NN+6
      ACCEPT 120,R6
      GOTO 1200
1100  TYPE 130
130   FORMAT (' ADDITIONAL CAPACITORS ADDED (Y/N)?',$)
      ACCEPT 140,ANS
140   FORMAT (A1)
      IF (ANS.NE.YES) GOTO 1200
      TYPE 150
150   FORMAT (' CAPACITOR VALUE (BOTH ASSUMED EQUAL) - (UFD)?',$)
      ACCEPT 120,C2
      C=C+C2
C
C     Calculate and display parameters:
C
1200  GAIN=R3/R4
      IF (NST.EQ.3) R6=10.
      GAIN=GAIN*(10./R6)
      DBG=20.*(ALOG10(GAIN))
      TYPE 160,GAIN,DBG
160   FORMAT (' DC GAIN = ',G11.4,' (V/V)   [',G10.3,' (DB)]')
      TYPE 170
170   FORMAT ('       NOTE: STAGE INVERTS SIGNAL')
      FPOL=1./(TWOPI*SQRT(1.E-06*R2*R3*C*C))
      DAMP=(SQRT(R2*R3))/(2.*R1)
      TYPE 180,FPOL,DAMP
180   FORMAT (' POLE FREQ (HZ) = ',G10.3,', DAMPING COEF = ',G10.3)
C
C     Check for reentry; store values:
C
      TYPE 190
190   FORMAT ('$MORE CHECKS (Y/N) ? ')
      ACCEPT 140,ANS
      IF (ANS.EQ.YES) GOTO 1000
      IF (NST.EQ.3) R6=0.0
      R(NST,1)=R1
      R(NST,2)=R2
      R(NST,3)=R3
      R(NST,4)=R4
      R(NST,6)=R6
      CAP(NST,1)=C2
      CAP(NST,2)=C2
      AV(NST,1)=-GAIN
      IF (NST.EQ.3) AV(NST,1)=GAIN
      AV(NST,2)=20.*(ALOG10(GAIN))
      FP(NST)=FPOL
      DP(NST)=DAMP
      NTY(NST)=2
      RETURN
      END
```

Table G-4 Subroutine VHP Listing

```
      SUBROUTINE VHP(NST)
C
C     NST = Stage number (2,5) passed from calling program.
C
      COMMON R(5,8),CAP(5,3),AV(5,2),FP(5),DP(5),FZ(5),DZ(5),NTY(5)
      LOGICAL*1 ANS,YES
      DATA YES/1HY/
      TWOPI=6.2831853
C     C = Value of fixed capacitor on circuit board in uF.
      C=1.
      C2=0.0
      AMULT=1.
      TYPE 100
100   FORMAT (' SECOND ORDER HIGH PASS FILTER')
      NN=200
      IF (NST.EQ.5) NN=400
C
C     Get values from user:
C
1000  TYPE 110,NN+1
110   FORMAT ('$R',I3,'   (KOHMS) = ? ')
      ACCEPT 120,R1
120   FORMAT (E12.5)
      TYPE 110,NN+2
      ACCEPT 120,R2
      TYPE 110,NN+3
      ACCEPT 120,R3
      TYPE 110,NN+4
      ACCEPT 120,R4
      TYPE 110,NN+5
      ACCEPT 120,R5
      TYPE 110,NN+7
      ACCEPT 120,R7
      TYPE 110,NN+8
      ACCEPT 120,R8
      TYPE 130
130   FORMAT (' ADDITIONAL CAPACITORS ADDED (Y/N)?',$)
      ACCEPT 140,ANS
140   FORMAT (A1)
      IF (ANS.NE.YES) GOTO 1050
      TYPE 150
150   FORMAT (' CAPACITOR VALUE (BOTH ASSUMED EQUAL) - (UFD)?',$)
      ACCEPT 120,C2
      C=C+C2
C
C     Calculate and display filter parameters:
C
1050  GAIN=10./R8
      DBG=20.*(ALOG10(GAIN))
      TYPE 160,GAIN,DBG
160   FORMAT (' HI FREQ GAIN = ',G11.4,' (V/V)   [',
     +G10.3,' (DB)]')
      TYPE 170
```

Table G-4 Subroutine VHP Listing (contd)

```
170   FORMAT ('       NOTE: STAGE INVERTS SIGNAL')
      FPOLE=1./(TWOPI*SQRT(1.E-06*R2*R3*C*C))
      DAMPP=(SQRT(R2*R3))/(2.*R1)
      RT=(R4*R7)-(R3*R8)
      IF (RT.GT.0.0) GOTO 1100
      AMULT=-1.
      RT=-RT
1100  FZERO=FPOLE*SQRT(RT/(R4*R7))
      DAMPZ=SQRT((R2*R3*R7)/(R4*RT))
      DAMPZ=DAMPZ*((R4*R5)-(R1*R8))/(2.*R1*R5)
      IF (FZERO.GT.(FPOLE*1.E-04)) GOTO 1200
      FZERO=FPOLE*1.E-04
      DAMPZ=1.
1200  TYPE 180,AMULT*FZERO,DAMPZ
180   FORMAT (' ZERO FREQ (HZ) = ',G11.4,', ZERO DAMPING COEF = ',G10.3)
      TYPE 190,FPOLE,DAMPP
190   FORMAT (' POLE FREQ (HZ) = ',G10.3,', POLE DAMPING COEF = ',G10.3)
      IF (AMULT.EQ.-1.) TYPE 200
200   FORMAT ('0****** WARNING! POOR LOW FREQUENCY REJECTION -
     + RX03*RX08 > RX04*RX07 ******')
      IF (DAMPZ.LT.0.0) TYPE 210
210   FORMAT ('0****** WARNING!! LOW FREQ PHASE ERROR -
     +RX01*RX08 < RX04*RX05 ******')
C
C     Check for reentry; store values:
C
      TYPE 220
220   FORMAT ('0REPEAT CHECK (Y/N) ? ',$)
      ACCEPT 140,ANS
      IF (ANS.EQ.YES) GOTO 1000
      R(NST,1)=R1
      R(NST,2)=R2
      R(NST,3)=R3
      R(NST,4)=R4
      R(NST,5)=R5
      R(NST,7)=R7
      R(NST,8)=R8
      CAP(NST,1)=C2
      CAP(NST,2)=C2
      AV(NST,1)=-GAIN
      AV(NST,2)=20.*(ALOG10(GAIN))
      FP(NST)=FPOLE
      DP(NST)=DAMPP
      FZ(NST)=AMULT*FZERO
      DZ(NST)=DAMPZ
      NTY(NST)=3
      RETURN
      END
```

Table G-5 Subroutine VBP Listing

```
      SUBROUTINE VBP(NST)
C
C     NST = Stage number (2,5) passed from calling program
C
      COMMON R(5,8),CAP(5,3),AV(5,2),FP(5),DP(5),FZ(5),DZ(5),NTY(5)
      LOGICAL*1 ANS,YES
      DATA YES/1HY/
      TWOPI=6.2831853
C     C = Value of fixed filter capacitor on board, in uF.
      C=1.0
      C2=0.0
      TYPE 100
100   FORMAT (' SECOND ORDER BAND PASS FILTER')
      NN=200
      IF (NST.EQ.5) NN=400
C
C     Get resistor values from user:
C
1000  TYPE 110,NN+1
110   FORMAT ('$R',I3,'   (KOHMS) = ? ')
      ACCEPT 120,R1
120   FORMAT (E12.5)
      TYPE 110,NN+2
      ACCEPT 120,R2
      TYPE 110,NN+3
      ACCEPT 120,R3
      TYPE 110,NN+4
      ACCEPT 120,R4
      TYPE 110,NN+5
      ACCEPT 120,R5
      TYPE 130
130   FORMAT (' ADDITIONAL CAPACITORS ADDED (Y/N)?',$)
      ACCEPT 140,ANS
140   FORMAT (A1)
      IF (ANS.NE.YES) GOTO 1100
      TYPE 150
150   FORMAT (' CAPACITOR VALUE (BOTH ASSUMED EQUAL) - (UFD)?',$)
      ACCEPT 120,C2
      C=C+C2
C
C     Calculate and display filter parameters:
C
1100  GAIN=(10.*R1)/(R4*R5)
      GAIN=GAIN*(SQRT(R2*R3))/(2.*R1+SQRT(R2*R3))
      DBG=20.*(ALOG10(GAIN))
      TYPE 160,GAIN,DBG
160   FORMAT (' CENTER FREQ GAIN = ',G11.4,' (V/V)   [',
     +G10.3,' (DB)]')
      FPOLE=1./(TWOPI*SQRT(1.E-06*R2*R3*C*C))
      DAMPP=(SQRT(R2*R3))/(2.*R1)
      FZERO=FPOLE*1.E-04
      DAMPZ=0.
      TYPE 170,FZERO
```

Table G-5 Subroutine VBP Listing (contd)

```
170  FORMAT (' ZERO FREQ (HZ) = ',G11.4)
     TYPE 180,FPOLE,DAMPP
180  FORMAT (' POLE FREQ (HZ) = ',G11.4,', POLE DAMPING COEF = ',G10.3)
C
C    Check for subroutine repeat; store parameters and exit:
C
     TYPE 190
190  FORMAT ('$REPEAT CHECK (Y/N) ? ')
     ACCEPT 140,ANS
     IF (ANS.EQ.YES) GOTO 1000
     R(NST,1)=R1
     R(NST,2)=R2
     R(NST,3)=R3
     R(NST,4)=R4
     R(NST,5)=R5
     CAP(NST,1)=C2
     CAP(NST,2)=C2
     AV(NST,1)=GAIN
     AV(NST,2)=20.*(ALOG10(GAIN))
     FP(NST)=FPOLE
     DP(NST)=DAMPP
     FZ(NST)=FZERO
     DZ(NST)=DAMPZ
     NTY(NST)=4
     RETURN
     END
```

Table G-6 Subroutine VBR Listing

```
     SUBROUTINE VBR(NST)
C
C    NST = Stage number (2,5) pass from calling program.
C
     COMMON R(5,8),CAP(5,3),AV(5,2),FP(5),DP(5),FZ(5),DZ(5),NTY(5)
     LOGICAL*1 ANS,YES
     DATA YES/1HY/
     TWOPI=6.2831853
C    C = Value of fixed filter capacitors on board, in uF.
     C=1.0
     C2=0.0
     AMULT=1.
     TYPE 100
100  FORMAT (' SECOND ORDER BAND REJECT FILTER')
C
C    Get nominal values of FPOLE and FZERO to determine filter case:
C
     TYPE 110
110  FORMAT ('$NOMINAL POLE FREQ (HZ) = ? ')
     ACCEPT 120,FPOLE
120  FORMAT (E12.5)
     TYPE 130
130  FORMAT ('$NOMINAL ZERO FREQ (HZ) = ? ')
     ACCEPT 120,FZERO
     NCASE=1
     IF (FPOLE.LT.FZERO) NCASE=2
```

Table G-6 Subroutine VBR Listing (contd)

```
C
C     Get resistor values:
C
      NN=200
      IF (NST.EQ.5) NN=400
1000  TYPE 140,NN+1
140   FORMAT ('$R',I3,'    (KOHMS) = ? ')
      ACCEPT 120,R1
      TYPE 140,NN+2
      ACCEPT 120,R2
      TYPE 140,NN+3
      ACCEPT 120,R3
      TYPE 140,NN+4
      ACCEPT 120,R4
      TYPE 140,NN+5
      ACCEPT 120,R5
      IF (NCASE.EQ.2) GOTO 1100
      TYPE 140,NN+7
      ACCEPT 120,R7
      R6=0.0
      GOTO 1200
1100  TYPE 140,NN+6
      ACCEPT 120,R6
      R7=0.0
1200  TYPE 140,NN+8
      ACCEPT 120,R8
      TYPE 150
150   FORMAT (' ADDITIONAL CAPACITORS ADDED (Y/N)?',$)
      ACCEPT 160,ANS
160   FORMAT (A1)
      IF (ANS.NE.YES) GOTO 1250
      TYPE 170
170   FORMAT (' CAPACITOR VALUE (BOTH ASSUMED EQUAL) - (UFD)?',$)
      ACCEPT 120,C2
      C=C+C2
C
C     Calculate and display filter parameters:
C
1250  IF (NCASE.EQ.2) GOTO 1300
C     Case I:
      RTI=(R3*R8)/(R4*R7)
      IF (RTI.LT.1.) GOTO 1275
      AMULT=-1.
1275  GAIN=AMULT*(10./R8)*(1.-RTI)
      GOTO 1400
C     Case II:
1300  RTII=(R3*R8)/(R4*R6)
      GAIN=(10./R8)*(RTII+1.)
1400  DBG=20.*(ALOG10(GAIN))
      TYPE 180,GAIN,DBG
180   FORMAT (' DC GAIN = ',G11.4,' (V/V)   [',G10.3,' (DB)]')
      IF (NCASE.EQ.1) GOTO 1500
      TYPE 190
190   FORMAT ('      NOTE: STAGE INVERTS SIGNAL')
1500  FPOLE=1./(TWOPI*SQRT(1.E-06*R2*R3*C*C))
      DAMPP=(SQRT(R2*R3))/(2.*R1)
      IF (NCASE.EQ.2) GOTO 1600
```

Table G-6 Subroutine VBR Listing (contd)

```
C     Case I:
      FZERO=SQRT(FPOLE*FPOLE*ABS(RTI-1.))
      GOTO 2000
C     Case II:
1600  FZERO=SQRT(FPOLE*FPOLE*(1.+RTII))
2000  RT=(R1*R8)/(R4*R5)
      DAMPZ=(1-RT)/(2.E-03*R1*C*TWOPI*FZERO)
      TYPE 200,AMULT*FZERO,DAMPZ
200   FORMAT (' ZERO FREQ (HZ) = ',G11.4,', ZERO DAMPING COEF = ',G10.3)
      TYPE 210,FPOLE,DAMPP
210   FORMAT (' POLE FREQ (HZ) = ',G11.4,', POLE DAMPING COEF = ',G10.3)
      IF (AMULT.EQ.-1.) TYPE 220
220   FORMAT ('0****** WARNING!! POOR FREQUENCY REJECTION -
     +RX03*RX08 > RX04*RX07 ******')
C
C     Check for subroutine repeat and store results:
C
      TYPE 230
230   FORMAT ('0REPEAT CHECK (Y/N) ? ',$)
      ACCEPT 160,ANS
      IF (ANS.EQ.YES) GOTO 1000
      R(NST,1)=R1
      R(NST,2)=R2
      R(NST,3)=R3
      R(NST,4)=R4
      R(NST,5)=R5
      R(NST,6)=R6
      R(NST,7)=R7
      R(NST,8)=R8
      CAP(NST,1)=C2
      CAP(NST,2)=C2
      AV(NST,1)=-GAIN
      AV(NST,2)=20.*(ALOG10(GAIN))
      FP(NST)=FPOLE
      DP(NST)=DAMPP
      FZ(NST)=AMULT*FZERO
      DZ(NST)=DAMPZ
      NTY(NST)=5
      RETURN
      END
```

Table G-7 Subroutine VPRINT Listing

```
      SUBROUTINE VPRINT
      COMMON R(5,8),CAP(5,3),AV(5,2),FP(5),DP(5),FZ(5),DZ(5),NTY(5)
      LOGICAL*1 DAT(9),TITLE(40)
      CALL DATE(DAT)
      AVP=1.
      AVS=0.
50    FORMAT ('0','STAGE ',I1,':',20X,'-- GAIN --')
60    FORMAT ('0','STAGE ',I1,':',20X,'-- LOW PASS --')
70    FORMAT ('0','STAGE ',I1,':',20X,'-- HIGH PASS --')
80    FORMAT ('0','STAGE ',I1,':',20X,'-- BAND PASS --')
90    FORMAT ('0','STAGE ',I1,':',20X,'-- BAND REJECT --')
```

Table G-7 Subroutine VPRINT Listing (contd)

```
C
C     Print header:
C
      PRINT 100
100   FORMAT ('0         SDAS SIGNAL CONDITIONING CARD
     + RESISTOR VALUES AND FILTER PARAMETERS')
      TYPE 115
115   FORMAT (' PRINTOUT ID (<40 CHAR)?',$)
      ACCEPT 118,(TITLE(N),N=1,40)
118   FORMAT (40A1)
      PRINT 120 DAT
120   FORMAT (1X,9A1,20X,'ACTUAL COMPONENT VALUES')
      PRINT 130,TITLE
130   FORMAT (25X,40A1)
C
C     Stage 1:
C
      IF (AV(1,1).EQ.0.0) GOTO 1100
      PRINT 50,1
      PRINT 140,101,R(1,1)
140   FORMAT (1X,T8,'R',I3,' = ',G11.4,' KOHMS')
      PRINT 140,102,R(1,2)
      PRINT 150,(AV(1,N),N=1,2)
150   FORMAT ('0',T16,'DC GAIN = ',G11.4,' (V/V)   [',
     +G10.3,' (DBV)]')
      PRINT 160,FP(1)
160   FORMAT (1X,T16,'POLE FREQ = ',G11.4,' HZ')
      AVP=AV(1,1)
      AVS=AV(1,2)
C
C     Stage 2:
C
1000  IF (AV(2,1).EQ.0.0) GOTO 1800
      GOTO (1100,1200,1300,1400,1500) NTY(2)
1100  PRINT 50,2
      GOTO 1600
1200  PRINT 60,2
      GOTO 1600
1300  PRINT 70,2
      GOTO 1600
1400  PRINT 80,2
      GOTO 1600
1500  PRINT 90,2
1600  CALL VRPRIN (2)
      AVP=AVP*AV(2,1)
      AVS=AVS+AV(2,2)
C
C     Stage 3:
C
1800  IF (AV(3,1).EQ.0.0) GOTO 1900
      PRINT 60,3
      CALL VRPRIN (3)
      AVP=AVP*AV(3,1)
      AVS=AVS+AV(3,2)
C
C     Stage 4:
C
1900  IF (AV(4,1).EQ.0.0) GOTO 3000
```

Table G-7 Subroutine VPRINT Listing (contd)

```
      IF (NTY(4).EQ.2) GOTO 2000
      PRINT 50,4
      GOTO 2100
2000  PRINT 60,4
2100  PRINT 440,R(4,1)
440   FORMAT (1X,T8,'R306 = ',G11.4,' KOHMS')
      PRINT 445,R(4,2)
445   FORMAT (1X,T8,'R309 = ',G11.4,' KOHMS')
      IF (CAP(4,1).NE.0.0) PRINT 450,CAP(4,1)
450   FORMAT (1X,T8,'C301 = ',G11.4,' UFD')
      PRINT 150,(AV(4,N),N=1,2)
      IF(FP(4).NE.0.) PRINT 250,FP(4)
250   FORMAT (1X,T16,'POLE FREQ = ',G11.4,' HZ')
      AVP=AVP*AV(4,1)
      AVS=AVS+AV(4,2)
C
C     Stage 5:
C
3000  IF (AV(5,1).EQ.0.0) GOTO 4000
      GOTO (3100,3200,3300,3400,3500) NTY(5)
3100  PRINT 50,5
      GOTO 3600
3200  PRINT 60,5
      GOTO 3600
3300  PRINT 70,5
      GOTO 3600
3400  PRINT 80,5
      GOTO 3600
3500  PRINT 90,5
3600  CALL VRPRIN (5)
      AVP=AVP*AV(5,1)
      AVS=AVS+AV(5,2)
      PRINT 600,AVP,AVS
600   FORMAT ('0','TOTAL FILTER GAIN = ',G11.4,' (V/V) ',G10.3,' (DBV)')
      PRINT 610
610   FORMAT (5X,'(CAUTION: TOTAL GAIN IS A SIMPLE PRODUCT. CHECK
      + FILTER TYPE')
      PRINT 620
620   FORMAT (5X,'TO DETERMINE ACTUAL COMPOSITE GAIN.)')
      IF(AVP.LT.0.) PRINT 630
630   FORMAT (' FILTER INVERTS SIGNAL')
4000  RETURN
      END
```

Table G-8 Subroutine VRPRIN Listing

```
      SUBROUTINE VRPRIN (NST)
C
C     NST = Stage number (2,3,5) passed from calling program.
C
      COMMON R(5,8),CAP(5,3),AV(5,2),FP(5),DP(5),FZ(5),DZ(5),NTY(5)
      NN=NST*100
      IF (NST.EQ.5) NN=400
C
C     Print resistor values:
C
```

Table G-8 Subroutine VRPRIN Listing (contd)

```
      DO 1000,N=1,8
      IF(R(NST,N).EQ.0.) GOTO 1000
      PRINT 100,NN+N,R(NST,N)
100   FORMAT (1X,T8,'R',I3,' = ',G11.4,' KOHMS')
1000  CONTINUE
C
C     Print capacitor values:
C
      NUM=NST
      IF (NST.EQ.2) NUM=1
      PRINT 110,NUM,CAP(NST,1)
110   FORMAT (1X,T8,'C',I1,'' = ',G11.4,' UFD')
      PRINT 110,NUM+1,CAP(NST,2)
C
C     Print stage gain:
C
1200  IF (NTY(NST).EQ.3) GOTO 1220
      IF (NTY(NST).EQ.4) GOTO 1240
      PRINT 125,(AV(NST,N),N=1,2)
125   FORMAT ('0',T16,'DC GAIN = ',G11.4,' (V/V)   [',
     +G10.3,' (DBV)]')
      GOTO 1260
1220  PRINT 130,(AV(NST,N),N=1,2)
130   FORMAT ('0',T16,'HI FREQ GAIN = ',G11.4,' (V/V)   [',
     +G10.3,' (DBV)]')
      GOTO 1260
1240  PRINT 135,(AV(NST,N),N=1,2)
135   FORMAT ('0',T16,'ZERO FREQ GAIN = ',G11.4,' (V/V)   [',
     +G10.3,' (DBV)]')
C
C     Print pole, zero, and damping coefficient information:
C
1260  IF(FP(NST).EQ.0.) GOTO 1500
      IF(DP(NST).NE.0.) GOTO 1300
      PRINT 140,FP(NST)
140   FORMAT (1X,T16,'SINGLE POLE FREQ = ',G11.4,' HZ')
      GOTO 1500
1300  IF (DP(NST).EQ.-1.) GOTO 1400
      PRINT 150,FP(NST),DP(NST)
150   FORMAT (1X,T16,'DOUBLE POLE FREQ = ',G11.4,' HZ; DAMPING COEFF = '
     +,G10.3)
      GOTO 1500
1400  PRINT 160,FP(NST)
160   FORMAT (1X,T16,'COMPLEMENTARY POLE PAIR FREQ = ',G11.4,' HZ')
1500  IF (FZ(NST).EQ.0.) GOTO 1800
      IF (DZ(NST).NE.0.) GOTO 1600
      PRINT 170,FZ(NST)
170   FORMAT (1X,T16,'SINGLE ZERO FREQ = ',G11.4,' HZ')
      GOTO 1800
1600  IF (DZ(NST).EQ.-1.) GOTO 1700
      PRINT 180,FZ(NST),DZ(NST)
180   FORMAT (1X,T16,'DOUBLE ZERO FREQ = ',G11.4,' HZ; DAMPING COEFF = '
     +,G10.3)
      IF (NTY(NST).EQ.3.AND.FZ(NST).LT.0.) PRINT 190
190   FORMAT ('0****** WARNING! POOR LOW FREQUENCY REJECTION -
     + RX03*RX08 > RX04*RX07 ******')
      IF (NTY(NST).EQ.5.AND.FZ(NST).LT.0.) PRINT 200
```

Table G-8 Subroutine VRPRIN Listing (contd)

```
200   FORMAT ('0****** WARNING!! POOR FREQUENCY REJECTION -
     +RX03*RX08 > RX04*RX07 ******')
      IF (DZ(NST).LT.0.0) PRINT 210
210   FORMAT ('0****** WARNING!! LOW FREQ PHASE ERROR -
     +RX01*RX08 < RX04*RX05 ******')
      GOTO 1800
1700  PRINT 220,FZ(NST)
220   FORMAT (1X,T16,'COMPLEMENTARY ZERO PAIR FREQ = ',G11.4,' HZ')
1800  RETURN
      END
```

Appendix H

System Controller Chassis Signal Wiring Details

H.1 PARALLEL INTERFACE SIGNAL WIRING

The following information pertains to connectors J3-J11 on the system controller rear panel (see Chapter 5, Figure 16) when used with Digital Equipment Co. (DEC) DRV-11 parallel interfaces.

J3 through J11 consist of 50-pin ribbon cable connectors. Attached to these is a 50-conductor ribbon cable (3M # 3365). Since the DEC parallel interfaces accept 40-pin ribbon connectors, the wires connected to pins 41 through 50 of J3-J11 are not used for signals but are available for other uses. The 50-wire ribbon cable is therefore split, with wires 41 through 50 tied off. The other 40 wires are terminated with a 3M #3417-6040 plug for connection to the parallel line interface. Pin 1 of the two connectors must be connected to the same edge of the ribbon cable.

The following two tables identify the signals appearing on the pins of J3-J11. Table H-1 applies when the cable is connected to J2 on the DRV-11 parallel interface. Table H-2 applies when the cable is connected to J1 on the DRV-11. Pin 1 (indicated by an arrow on the connector) of the 3M #3417 connector must be connected to pin A of J1/J2 of the DRV-11.

H.2 SERIAL INTERFACE SIGNAL WIRING

Connectors J15 - J17 provide both RS-232 and 20 mA current loop serial interfaces. The serial connector format given below DOES NOT conform to either the RS-232 or the 20 mA current loop pin

assignments, due to common use of the same pins by both standards. Therefore, a unique pin assignment has been developed to allow either type of interface with no pin assignment conflict.

J15-J17 each consist of a 25-pin "D" connector for connecting to an input/output device. The "D" connector is mounted on an adapter board which, in turn, is connected to a 40-pin ribbon cable through a 3M #3432 connector (on the adapter) and a 3M #3417-6040 plug on the cable. The other end of the ribbon cable is terminated with a 3M #3417-6040 plug also. It is plugged into the DEC DLV-11 serial interface mounted in the computer card rack. Both plugs are attached to the ribbon cable so that the corresponding pins on each are connected. Pin 1 of the cable (indicated by an arrow on the plug) is connected to pin 1 of the adapter (also indicated by an arrow on the receptacle) and pin A of the DLV-11 connector.

In addition to connecting the I/O device signal lines to the correct pins on device cable plug (DB-25P), two other connections must be made. First, a jumper must be connected between two pins in the DB-25P as indicated below. Second, the DLV-11 interface card must be set up to match both the I/O device interface parameters and the digital addresses needed to be compatible with operational software. (See reference 3 for specification and configuration information of the DLV-11.) Table H-3 gives both the "D" connector and 40-pin connector pin assignments. Also listed in the table is the signal name appearing on the DB-25 pins and the corresponding signal from the I/O device that should be connected to it for proper operation.

H.3 A/D SIGNAL WIRING

J13 and J14 provide signal inputs and outputs between the A/D card mounted in the controller computer card rack and the signal conditioning subsystem. The connectors used are Cannon DD-50S "D" type; they are connected to shielded ribbon cables. The cables, in turn, are terminated in 40-pin ribbon plugs (3M #3417-6040). The entire cable assembly is supplied with the A/D board. (The assembly can be purchased separately from ADAC, Inc, Woburn, MA as part no. W-1 for their DEC 600LSH-16-PDA data acquisition subsystem.) Listed in Table H-4 are the pin definitions for both the 50-pin "D" connector and the 40-pin ribbon cable connectors.

Table H-1 System Controller Parallel Input Connector (J3-J11) Pin Identification

J3-J11 Connector: 3M #3331-0000 Mating Connector: 3M #3425		
Pin	Signal	Direction
3	Data accepted pulse	Out **
5	Input bit 2	In
7	Input bit 2	In
8	Ground	-
9	CSR Ø	Out
10	Ground	-
11	Input bit 15	In
12	Input bit 14	In
13	Input bit 13	In
14	Ground	-
15	REQ B	In
16	Ground	-
17	Input bit 12	In
18	Input bit 11	In
19	Input bit 10	In
20	Ground	-
21	Input bit 9	In
22	Input bit 8	In
23	Ground	-
24	Input bit 3	In
25	Input bit 7	In
26	Ground	-
27	Input bit 6	In
29	Input bit 5	In
30	Ground	-
31	Input bit 4	In
32	Input bit 1	In
33	Ground	-
34	Initialize	Out
35	Ground	-
36	Initialize	Out
37	Ground	-
38	Input bit Ø	In
39	Ground	-

** "Out" direction refers to signals put out by the interface card; "In" refers to signals accepted or read by the card.

Notes:

-- Pins not listed are not used.
-- All signal levels are TTL positive logic (5 Vdc = 1, Ø Vdc = Ø). Bit 15 is MSB, bit Ø is LSB.
-- Refer to reference 3 for further details on signals.

AD-A100 253 AIR FORCE GEOPHYSICS LAB HANSCOM AFB MA F/G 9/3
THE AIR FORCE GEOPHYSICS LABORATORY STANDALONE DATA ACQUISITION--ETC(U)
OCT 80 P G VON GLAHN
UNCLASSIFIED AFGL-TR-80-0317 NL

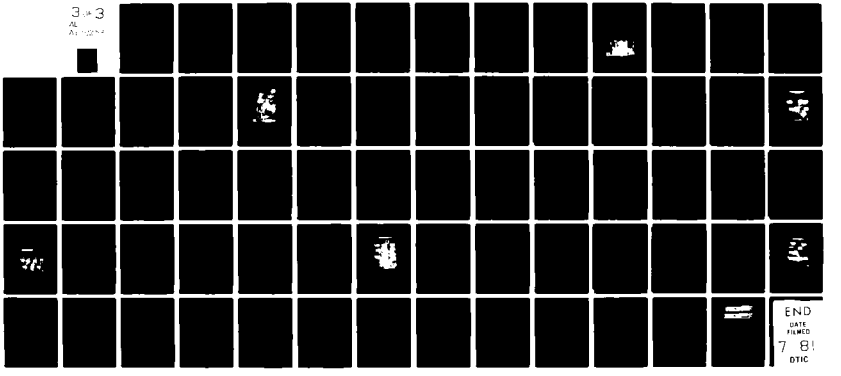


Table H-2 System Controller Parallel Output Connector (J3-J11) Pin Identification

J3-J11 Connector: 3M #3331-0000
Mating Connector: 3M #3425

Pin	Signal	Direction
3	Output bit Ø	Out *
8	Ground	-
9	Output bit 1	Out
1Ø	Output bit 4	Out
11	Ground	-
12	Output bit 5	Out
13	Initialize	Out
14	Output bit 6	Out
15	Ground	-
16	Output bit 7	Out
17	Output bit 3	Out
18	Ground	-
19	Output bit 8	Out
2Ø	Output bit 9	Out
21	Ground	-
22	Output bit 1Ø	Out
23	Output bit 11	Out
24	Output bit 12	Out
25	Ground	-
26	CSR 1	Out
27	Ground	-
28	Output bit 13	Out
29	Output bit 14	Out
3Ø	Output bit 15	Out
31	Ground	-
32	REQ A	In
33	Ground	-
34	Output bit 2	Out
35	Ground	-
36	Output bit 2	Out
37	Ground	-
39	Ground	-
4Ø	New data ready pulse	Out
49**	1ØØ PPS	In
5Ø**	Ground	-

* "Out" direction refers to signals put out by the interface card; "In" refers to signals accepted or read by the card.

** J6 (ERC WRITE) only.

Notes:

-- Pins not listed are not used.
-- All signal levels are TTL positive logic (5 Vdc = 1, Ø Vdc = Ø). Bit 15 is MSB, bit Ø is LSB.
-- Refer to reference 3 for further details on signals.

Table H-3 System Controller Serial Input/Output
Connector (J15-J17) Pin Identification

J15-J17 Connector: Cannon DB-25S Mating Connector: Cannon DB-25P				
DB-25 Pin	Ribbon Pin	Signal	I/O Device	
			Direction	Signal
1	40	Protective ground	-	Protective ground
2	6	RS232 Tx data	Out *	RS232 Rx data
3	8	RS232 Rx data	In	RS232 Tx data
4	18	RS232 REQUEST TO SEND	Out	RS232 CLEAR TO SEND
5	16	RS232 CLEAR TO SEND	In	RS232 REQUEST TO SEND
6	22	RS232 DATA SET READY	In	RS232 DATA TERM READY
7	39	Signal ground	-	Signal ground
8	24	RS232 CARRIER	In	RS232 BUSY
9	23	20 mA Tx data +	Out	20 mA Rx data +
10	9	20 mA Rx data +	In	20 mA Tx data +
11	31	20 mA Tx data -	Out	20 mA Rx data -
12	15	20 mA Rx data -	In	20 mA Tx data -
14	1	Protective ground	-	Protective ground
16	2	Signal ground	-	Signal ground
17 **	11	RS232 TTL Rx data	Out	-
18 ***	7	20 mA TTL Rx data	Out	-
19	5	TTL Rx data	In	-
20	26	RS232 DATA TERMINAL READY	Out	RS232 DATA SET READY
21	35	Reader enable +	Out	Reader enable +
24	27	Reader enable -	Out	Reader enable -
25	3	RS232 BUSY	Out	RS232 CARRIER

* "Out" direction refers to signals put out by the interface card;
"In" refers to signals accepted by the card.
** Jumper to DB25 pin 19 for RS232 operation.
*** Jumper to DB25 pin 19 for 20 mA operation.

Notes:
-- Pins not listed are not used.
-- Tx = transmit; Rx = receive.
-- Connector set up for active 20 mA current loop operation.
-- Refer to reference 3 for further details on signals.

Table H-4 System Controller A/D Input/Output Connector (J13-J14) Pin Identification

J13-J14 Connector: Cannon DD50S Mating Connector: Cannon DD50P			
DD-50 Pin	Ribbon Pin	Signal	Direction
16	31	Channel 0/0a *	Input **
15	29	Channel 1/1a	Input
14	27	Channel 2/2a	Input
13	25	Channel 3/3a	Input
12	23	Channel 4/4a	Input
11	21	Channel 5/5a	Input
10	19	Channel 6/6a	Input
9	17	Channel 7/7a	Input
33	32	Channel 8/0b	Input
32	30	Channel 9/1b	Input
31	28	Channel 10/2b	Input
30	26	Channel 11/3b	Input
29	24	Channel 12/4b	Input
28	22	Channel 13/5b	Input
27	20	Channel 14/6b	Input
26	18	Channel 15/7b	Input
1	1	Channel 16/8a	Input
2	3	Channel 17/9a	Input
3	5	Channel 18/10a	Input
4	7	Channel 19/11a	Input
5	9	Channel 20/12a	Input
6	11	Channel 21/13a	Input
7	13	Channel 22/14a	Input
8	15	Channel 23/15a	Input
18	2	Channel 24/8b	Input
19	4	Channel 25/9b	Input
20	6	Channel 26/10b	Input
21	8	Channel 27/11b	Input
22	10	Channel 28/12b	Input
23	12	Channel 29/13b	Input
24	14	Channel 30/14b	Input
25	16	Channel 31/15b	Input
46	37	D/A 1	Output
45	38	D/A 1 Return	-
44	39	D/A 2	Output
42	41	Shield	-
43	40	D/A 2 Return	-
48	35	Signal Return	-
49	34	Power Return	-
50	33	Channel 0-31 Common	-

* Number alone is single-ended input channel number; number and letter is differential input channel number ("a" is high, "b" is low level signal).

** "Input" refers to signals accepted by the A/D converter; "Output" refers to signals put out by the D/A converter.

Notes:

-- See reference 4 for further information on the A/D converter board.

Appendix I

System Controller Computer Details

I.1 APPENDIX OVERVIEW

This appendix presents information on the system computer. Specifically, it covers the computer card cage jumpering (to connect the two backplanes together)and the card cage priority assignment procedures. Next, the section defines a minimum computer configuration, a standardized address assignment for the configuration, and a listing of the module jumpering needed to set up the configuration. Finally, a modification to the parallel interface card for use with the printer/plotter is described.

The information included herein is not meant to be all-inclusive; rather it is designed to provide sufficient detail to allow the system user to correctly configure a minimum SDAS without reference to other documents. For those requiring more detailed information on the LSI-11 family of modules and backplanes, references 2 and 3 are recommended.

I.2 INTERFACE CIRCUIT BOARD DESCRIPTION

I.2.1 BACKPLANE JUMPERING

As discussed in Chapter 5, the LSI-11 card cage consists of two DEC H9270 card racks with integral backplanes. The backplanes of these two racks must be jumpered together using wire wrap jumpers connected to the backplane pins. Table I-1 gives the pins jumpered.

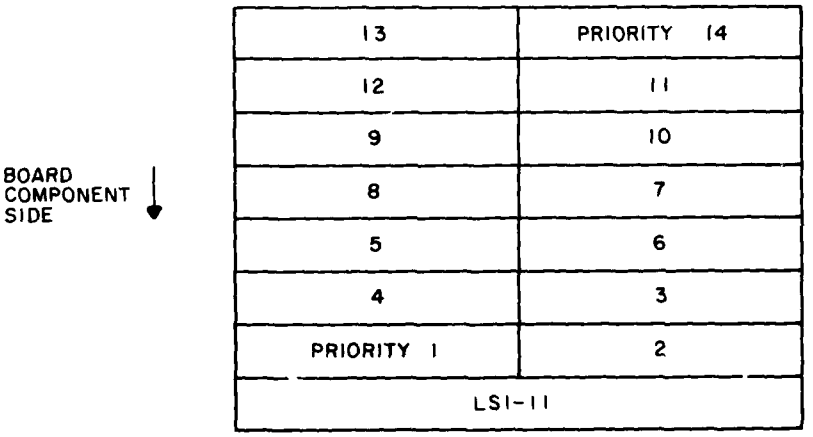
I.2.2 BACKPLANE INTERRUPT PRIORITY ASSIGNMENT

The LSI-11 computer system uses a daisy-chain interrupt priority system. Interrupt priority assigned to a given module is determined by its position in the chain. Those modules that are electrically closer on the chain to the computer will have a higher priority. Priority assignment is determined, then, by the position of the module in the backplane. Figure I-1 gives the priority structure of the double-backplane card cage used in the SDAS. It represents a view of the cage looking through the controller chassis access door. (The cards are oriented horizontally, component side down; each rectangle is a double-height module.)

Table I-1 System Controller LSI-11 Backplane Jumper List

AA1	AJ1	AT1	BF2	BP1
AB1	AJ2	AT2	BH2	BP2
AB2	AK2	AU2	BJ2	BR1
AC1	AL2	AV2	BK2	BR2
AD1	AN1	BA1	BL2	BS2
AE2	AP1	BB1	BM2	BT2
AF2	AP2	BB2	BN1	BU2
AH2	AR1	BE2	BN2	BV2

CPU backplane AN2 - second backplane AM2
CPU backplane AS2 - second backplane AR2
CPU backplane CH1 - second backplane AF1



I-1. System Controller Computer Backplane Interrupt Priority Assignment

I.3 SYSTEM CLOCK MODIFICATION DESCRIPTION

1.3.1 CONFIGURATION DEFINITION

A minimum SDAS computer configuration is made up of those modules needed to acquire and convert 16 channels of analog data, record it on digital tape, analyze the data, and print out the results. The modules included in a minimum configuration are given in Table I-2. Note that 32K words of RAM are called for. The software can run on less, if necessary.

A suggested module priority arrangement is given in Figure I-2. The exact priority scheme used for a given application would be dictated by software and timing considerations peculiar to that application.

Table I-2 System Controller
Minimum Computer Module List

Qty	Module	Use
1	LSI-11	System computer
1	A/D	Data conversion
1	32K RAM	Program/data storage
1	DLV-11	System console serial interface
1	DLV-11	Printer/plotter serial interface
1	DRV-11	Tape recorder parallel interface
1	DRV-11	System clock parallel interface
1	RXV-11	Floppy disk interface
1	REV-11A	Bus terminator

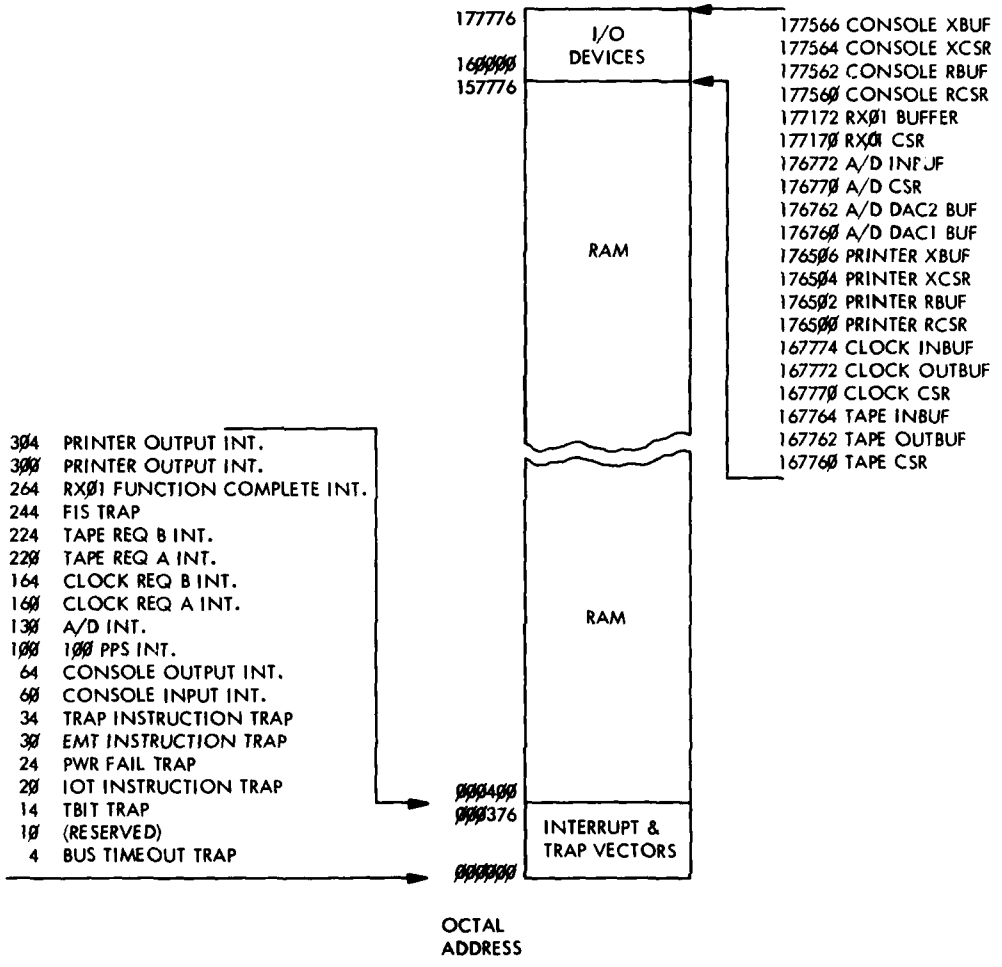
BOARD COMPONENT SIDE ↓

(BLANK)	(BLANK)
(BLANK)	(BLANK)
REV-11 TERMIN.	(BLANK)
DLV-11 PRINTER	DLV-11 CONSOLE
A/D CONVERTER	
DRV-11 TAPE	DRV-11 CLOCK
32K RAM	RXV-11
LSI-11 PROCESSOR	

I-2. System Controller Minimum System Computer
Suggested Module Locations

I.3.2 ADDRESS ASSIGNMENTS AND MEMORY MAP

A memory map of the minimum system is given in Figure I-3. The LSI-11 computer system uses the highest page in memory for input/output (I/O) module register addresses, as shown in the figure. Also, the LSI-11 uses the base page for interrupt vector locations, with the vector address jumpered on the individual modules. To insure software compatib. lity, I/O register addresses and vector locations have been standardized to those given in the figure. (See reference 2 for register definitions.)



I-3. System Controller Minimum System Computer Memory Map

I.3.3 MODULE JUMPERING

In order to implement the minimum system under discussion here, numerous jumpers on the various modules must be inserted. Table I-3 gives those jumpers that must be inserted for system operation. Module address and interrupt vector assignments are as given in Figure I-3.

I.4 SYSTEM CLOCK SYNCHRONIZATION PROCEDURES

The DRV-11 serial interface used with the SDAS printer/plotter (Bedford Computer System 75) has been modified. The modification allows a reduction of system software overhead in servicing this printer.

The System 75 is a buffered unit; it can receive data to be printed at a higher rate than it can be printed. When the buffer is full, the printer sets to zero the DATA TERMINAL READY interface line. This line is connected to the DATA SET READY input line of the DRV-11. It is read by the computer from the DATA SET READY bit of the interface status word. When the bit is zero, the software executes a wait loop until it goes to one, indicating more room in the buffer. A byte is then loaded into the interface's UART (Universal Asynchronous Receiver/Transmitter) which transmits it to the System 75. When the transmission is completed, the UART interrupts the computer and signals that it is ready for another byte.

Table I-3 System Controller
Minimum Computer Module Jumpers

Module	Jumpers Installed	Comments
Computer	W2, W11	
RXV11	W2, W5, W7, W12, W13	
DRV-11 (Clock)	A12, V3, V4, V7	
DRV-11 (Tape)	A3, A12, V3, V7	
DLV-11 (Console)	A3, A7, V3, V6, V7, FEH, EIA, FR0, FR1, FR2	9600 baud, RS232
DLV-11 (Printer)	A3, A4, A5, A7, A9, V3, V4, V5, 2SB, FEH, EIA, FR2	1200 baud, RS232
A/D	A/D RANGE: 1-4, 3-5, B-G, E-U MUX: 1-2, D-N, 3-4* D/A RANGE: A-B, E-F, M-B	-10 to +10 Vdc 16 CH PSEUDO DIFF'L -10 to +10 Vdc

* Jumpered with 0.01 μF capacitor

The modification consists of breaking the lead between the UART and the backplane interrupt input. A two-input AND gate is inserted into the line. The DATA SET READY signal is connected to the second input of the gate. As a result, the computer is only interrupted when both the UART TRANSMIT READY and the DATA SET READY (printer/plotter DATA TERMINAL READY) signals are present.

The modification procedure is given below. Figure I-4 shows the locations of the affected components on the DLV-11.

DLV-11 Modification Procedures

1. Cut pin 11 of IC E35.
2. Solder a bridge between pins 11 and 12 of IC E23.
3. Cut pin 6 of IC E23.
4. Connect pin 11 of IC E35 to pin 6 of IC E23.
5. Cut pin 4 of IC E32.
6. Jumper pin 9 of IC E33 to pin 4 of IC E32.

CAUTION:

Should a modified DLV-11 be used with an I/O device not providing a DATA TERMINAL READY signal, the interface DATA SET READY input must be tied to either the interface REQUEST TO SEND or the interface DATA TERMINAL READY outputs (DB25P pins 6, 4, and 20, respectively). Otherwise, the UART TRANSMIT READY line will never interrupt the computer.

This modification was developed by The Life Support Systems Group, Ltd., 2432 N.W. Johnson, Portland, Oregon 97210.

I-4. DLV-11 Modification Component Locations

Appendix J

System Controller Power Control Board Details

J.1 APPENDIX OVERVIEW

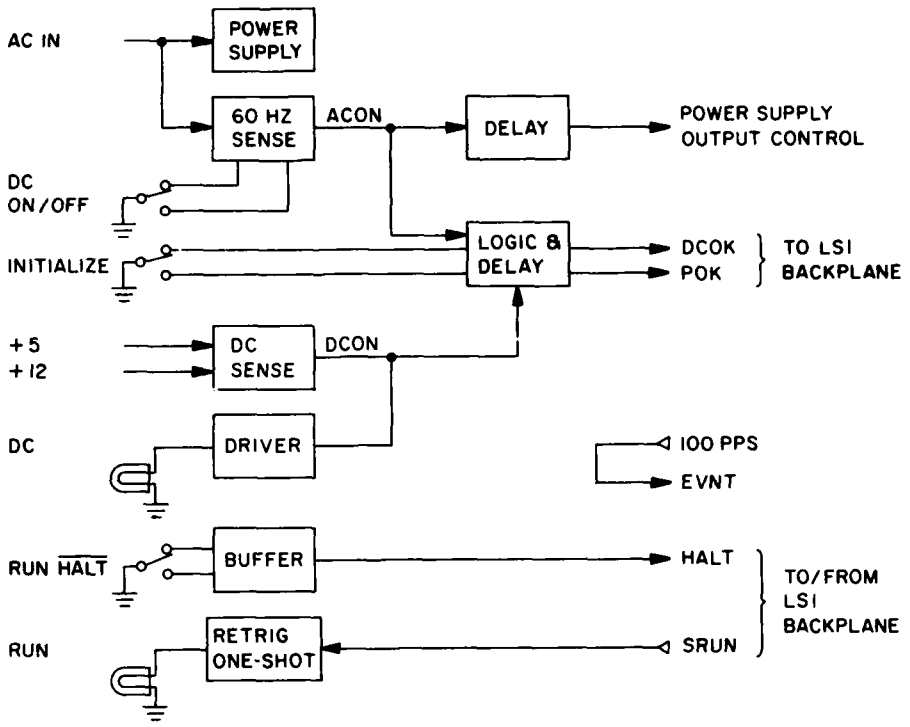
This appendix covers the circuitry needed to provide power status and control signals for the system control computer and power supplies. These signals meet the timing requirements specified by DEC in reference 2. All circuitry, excluding switches and indicator lamps, is mounted on a single printed circuit board. The following sections document the circuit functions, schematics, and parts included on this board.

J.2 POWER CONTROL CIRCUIT FUNCTIONAL DESCRIPTION

J.2.1 CIRCUIT BLOCK DIAGRAM

Figure J-1 gives a block diagram of the signal conditioning card. As shown on the diagram, the board has its own power supply which runs of 12.6 Vac, 60 Hz power. This 60 Hz power also runs to a sensing circuit as do the leads from the dc ON/OFF front panel switch. The circuit puts out a ACON signal when the power is present and the dc ON/OFF switch is on. This signal is delayed and provides the control signal for the controller chassis power supplies.

The outputs from the chassis power supplies are fed to a second sensing circuit. This circuit puts out a DCON signal when both voltages are at operating level (over 90% of final value). This signal also goes to a driver which controls the dc front panel light. The DCON and ACON signals together with the leads from the front



J-1. System Controller Power Control Board Block Diagram

panel INITIALIZE switch are fed to a logic and delay circuit. There, the signals are combined to form the DCOK and POK signals which provide power status information to the computer through its backplane.

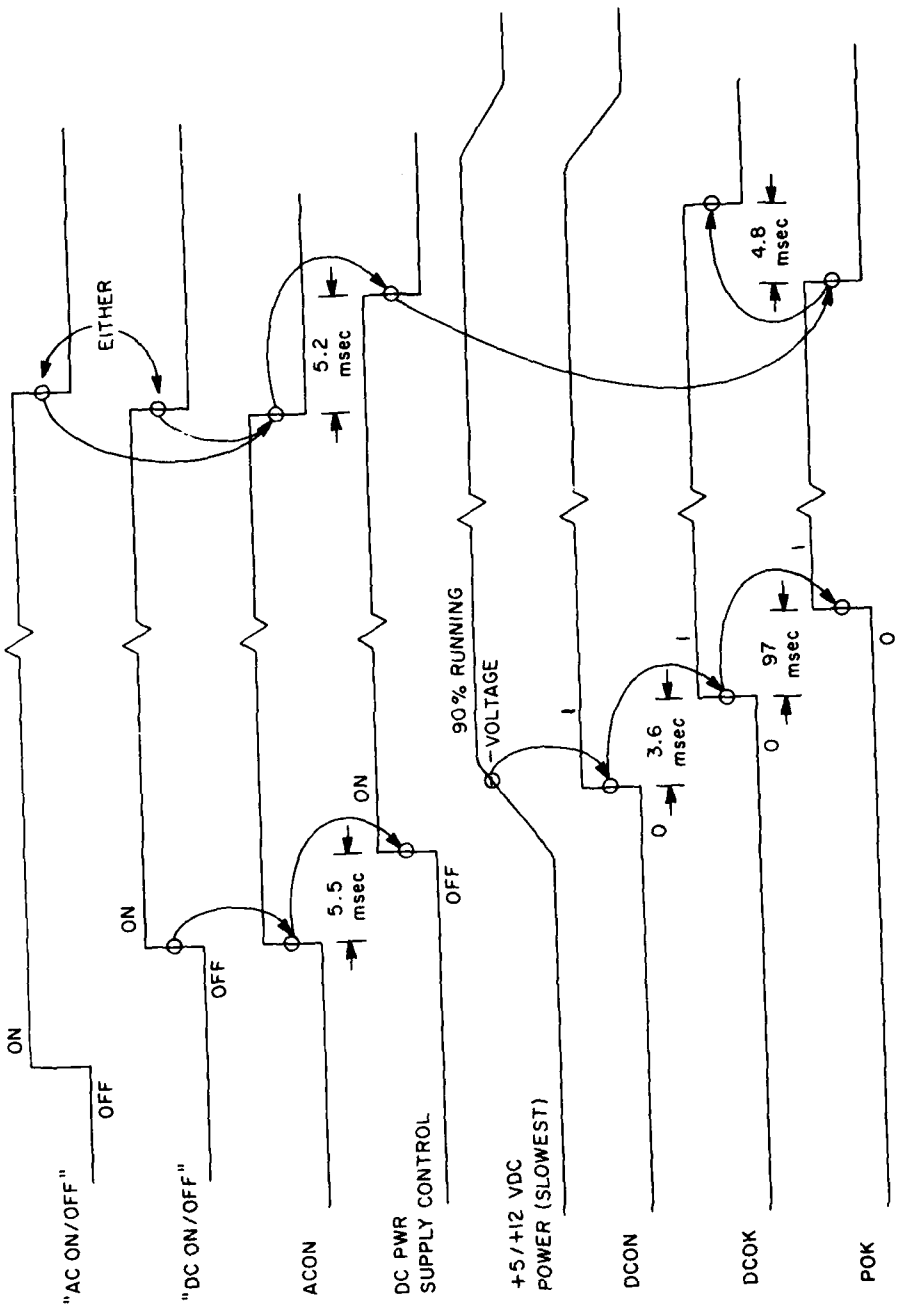
A buffer on the board converts the output of the RUN/HALT front panel switch to the HALT signal for the computer.

The SRUN signal from the computer is fed to a retriggerable oneshot multivibrator on the board. (SRUN consists of a pulse train that is present when the computer is running. The oneshot output drives the RUN lamp on the front panel.

Finally, one pin on the board edge connector is used as a junction point. Connected to it are the 100 pps signal from the system clock and the EVNT line to the computer.

J.2.2 CIRCUIT TIMING INFORMATION

A timing diagram for key signals on the control card is given by Figure J-2. As shown in the figure, turning on system power (via the ac ON/OFF switch) is a prerequisite for circuit operation. When the dc ON/OFF switch is thrown, the ACON signal goes high, indicating the



J-2. System Controller Power Control Board Timing Diagram

presence of ac power and initiating the power up timing sequence. This signal is delayed by 5.5 msec to provide the control signal for the chassis power supplies. When the slowest of the two supplies reaches 90% of full scale output, the DCON signal goes high. This signal is delayed by 3.6 msec and becomes the DCOK signal for the computer. A further 97 msec delay results in the POK signal, which is also sent to the computer.

The power down timing sequence begins with either a shut off or failure of ac power or a throwing of the dc ON/OFF switch. Either action results in the negation of the ACON signal. Following a 5.2 msec delay from this negation, both the power supply control signal and the POK are negated. After a further 4.8 msec delay, the DCOK signal is negated and the power down sequence is completed.

J.3 POWER CONTROL CIRCUIT SCHEMATIC

The schematic for the power control card is shown in Figure J-3. Relating the schematic to the block diagram, diodes CR1-CR4 together with capacitor C1 and voltage regulator U1 make up the onboard 5 Vdc power supply. Note that an external diode must be mounted between the output of this supply (at pin 12 on the edge connector) and the +5 V input to the dc sense circuit (pin 20). This diode allows the chassis power supply to power the circuit card after ac power fails. Since the chassis power supply has a longer decay time than the onboard supply, this connection insures orderly power-down timing.

Zener diode VR1 along with R1-R3, C2, and Q3 convert the incoming 12.6 Vac power to a 5 Vdc pulse train for the ac sense circuit. The sense circuit is made up of a dual monostable multivibrator (U2) and associated components. The monostables have pulse widths of approximately 10 msec. They are triggered by opposite rising edges of the pulse train from Q3. Both monostables are either enabled or disabled by the dc ON/OFF switch which is debounced by two sections of a hex inverter, U7. When enabled, the two pulse trains are combined by an OR gate (U3) to form the ACON signal. This signal is buffered by an open collector NAND gate (U5) and fed to a RC timing circuit made up of R9 and C5. The voltage across C5 is compared to a reference by comparator U6. When the voltage exceeds the threshold, U6 trips and generates the control signal for the control signal for the chassis power supplies, DCONC. DCONC is also inverted by U5 to allow control of power supplies requiring the opposite polarity signal. A jumper allows selection of control signal polarity.

Comparators U9 and R15-R22 make up the dc sense circuit. The two power supply outputs are connected to resistive dividers. The outputs of these two dividers are compared to a reference voltage (generated by R19 and R20 from the +5 V power line) by the comparators. The comparators outputs are combined by U8 to yield the DCON signal. This signal feeds the dc lamp driver made up of a R32 and Q2.

Comparators U10 and associated components, as well as gates U8 and U3 make up the logic and delay circuits that generate the DCOK and POK signals for the computer. As for the DCONC signal, delays are generated through RC delays feeding the two comparators. C11 and C12 on the two comparators provide positive feedback to insure clean switching of the comparators' outputs.

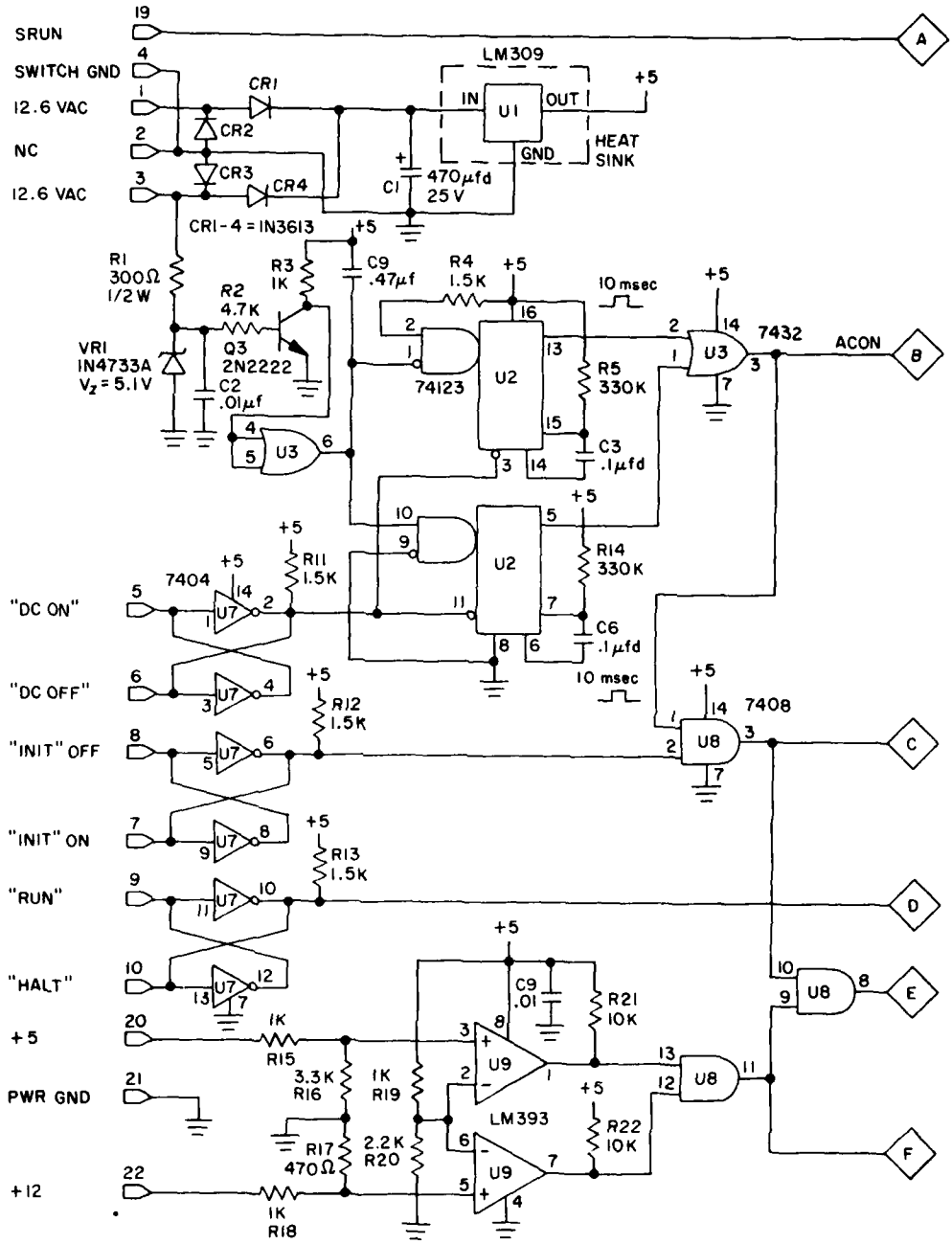
Two sections of hex inverter U7 and one section of an open collector NAND gate (U5) buffer the RUN/HALT switch output. The resulting signal feeds the BHALT signal to the system computer.

A retriggerable monostable multivibrator (U4) provides the pulse to level conversion for the RUN lamp driver made up of R8 and Q1. The monostable pulse width of 80 msec is considerably wider than the SRUN signal period so the monostable is continually retriggered as long as SRUN is present.

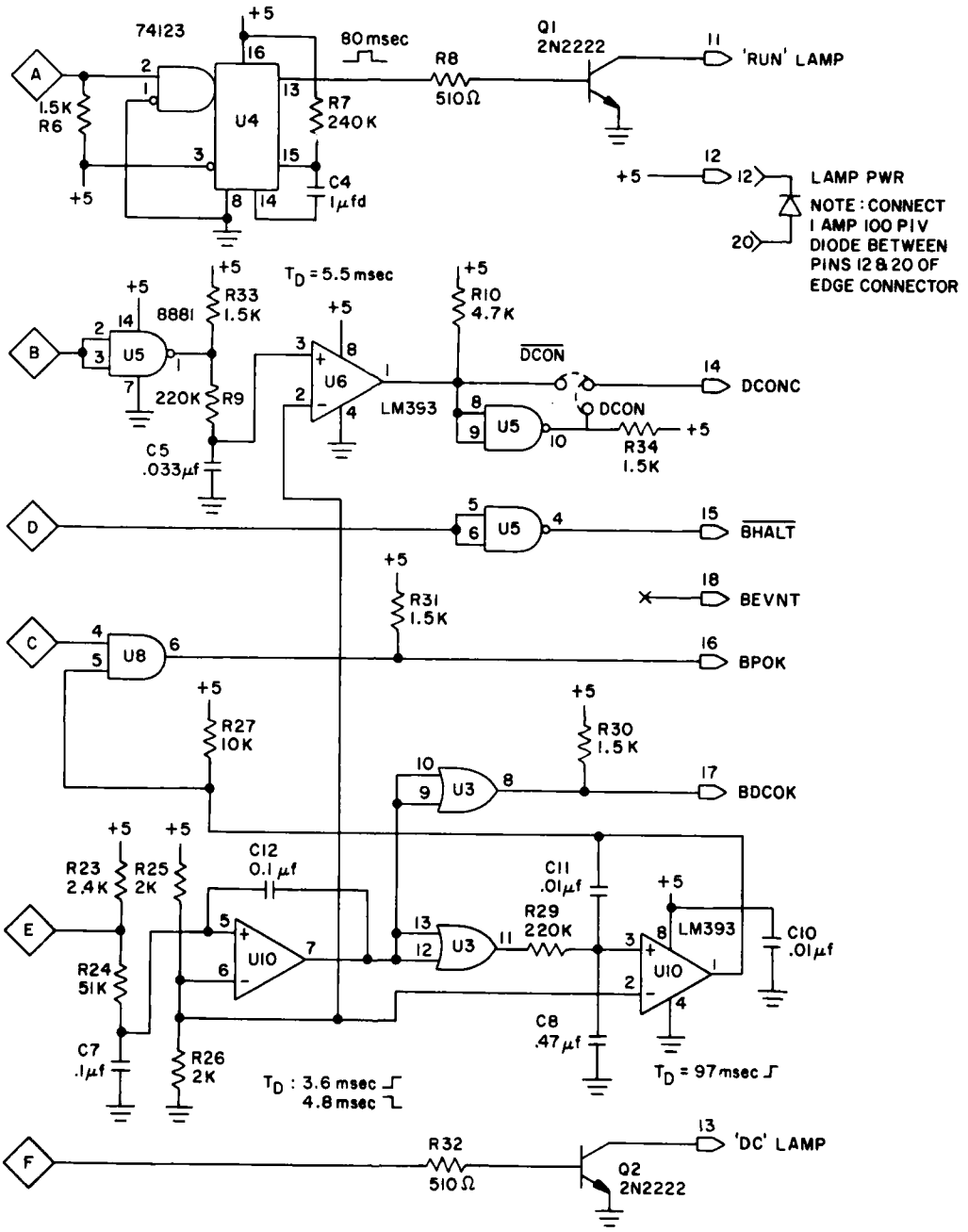
J.4 POWER CONTROL CIRCUIT BOARD DESCRIPTION AND PARTS LIST

All components for the power control circuits are mounted on a single 4.5 x 6.5 in. (11.4 x 16.5 cm), double-sided printed circuit board. Signal and power connections to the board are made through a 44-pin edge connector. A photograph of the board is given in Figure J-4. Parts locations are identified on the photograph; a detailed parts list is given in Table J-1.

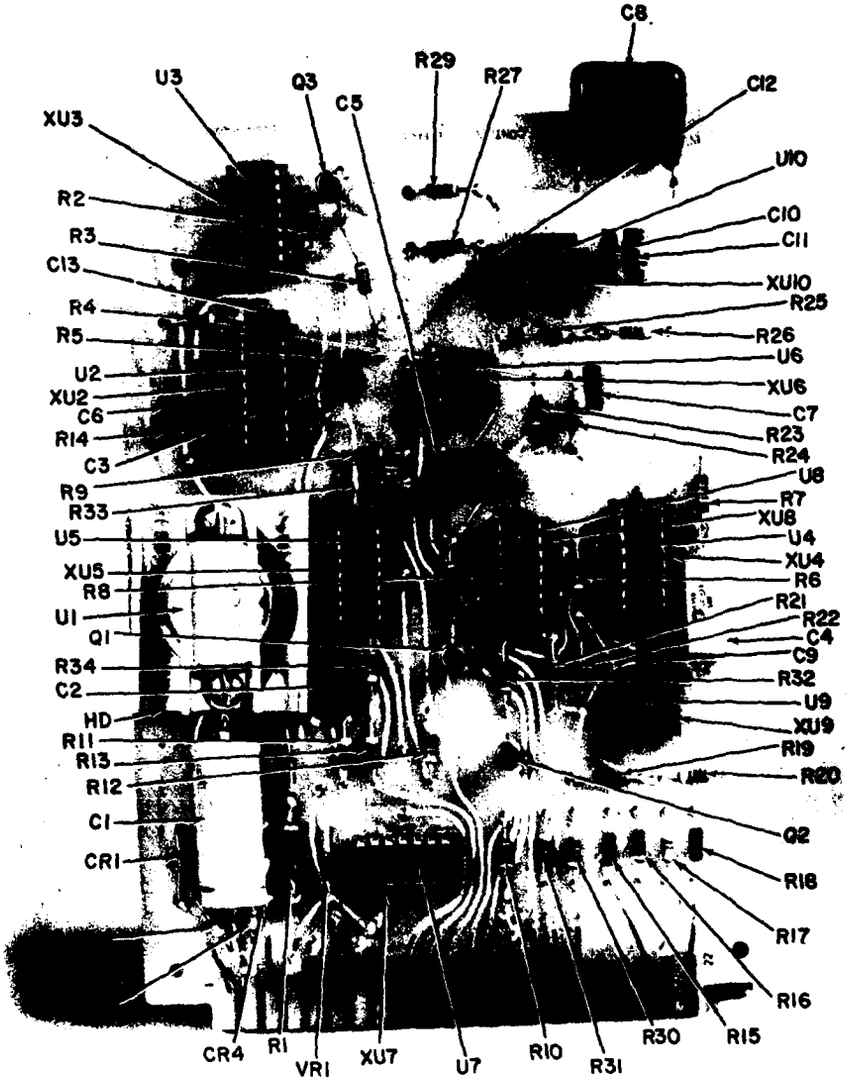
Table J-2 gives the pin identification for the control card edge connector.



J-3. System Controller Power Control Board *Schematic*



J-3. System Controller Power Control Board Schematic (Cont.)



J-4. System Controller Power Control Board
Component Locations

Table J-1 System Controller Power Control Board Parts List

Part	Noun	Mfgr Part No.	Manufacturer
XU2, XU4	Low profile DIP IC socket, 16-pin	516-AG10D	Augat
XU3,5,7,8	Low profile DIP IC socket, 14-pin	514-AG10D	Augat
XU6,9,10	Low profile DIP IC socket, 8-pin	508-AG10D	Augat
R1	Resistor, 300 Ω, 1/2 W, 2%, metal film	C5	Corning
R2,10	Resistor, 4.7K Ω, 1/4 W, 2%, metal film	C4	Corning
R3,15,18,19	Resistor, 1K Ω, 1/4 W, 2%, metal film	C4	Corning
R4,6,11-13, 30,31,33,34	Resistor, 1.5K Ω, 1/4 W, 2%, metal film	C4	Corning
R5,14	Resistor, 330K Ω, 1/4 W, 2%, metal film	C4	Corning
R7	Resistor, 240K Ω, 1/4 W, 2%, metal film	C4	Corning
R8,32	Resistor, 510 Ω, 1/4 W, 2%, metal film	C4	Corning
R9,29	Resistor, 220K Ω, 1/4 W, 2%, metal film	C4	Corning
R16	Resistor, 3.3K Ω, 1/4 W, 2%, metal film	C4	Corning
R17	Resistor, 470 Ω, 1/4 W, 2%, metal film	C4	Corning
R20	Resistor, 2.2K Ω, 1/4 W, 2%, metal film	C4	Corning
R21,22,27	Resistor, 10K Ω, 1/4 W, 2%, metal film	C4	Corning
R23	Resistor, 2.4K Ω, 1/4 W, 2%, metal film	C4	Corning
R24	Resistor, 51K Ω, 1/4 W, 2%, metal film	C4	Corning
R25,26	Resistor, 2K Ω, 1/4 W, 2%, metal film	C4	Corning
C1	Capacitor, 100 μF, 30 V, 20%, tantalum	69F935	GE
C2,9-12	Capacitor, 0.01 μF, 200 V	CKR06	AVX
C3,6,7	Capacitor, 0.1 μF, 200 V		AVX
C4	Capacitor, 1 μF, 50 V, 5%, polycarbonate	625B-1-a-105-J	Electrocube
C5	Capacitor, 0.033 μF, 50 V, 10%, polyester	601PE	TRW
C8	Capacitor, 0.47 μF, 50 V, 10%, polyester	601PE	TRW
C13	Capacitor, 0.47 μF, 50 V		AVX
Q1-3	Transistor, NPN	2N2222	TI
CR1-4	Diode, 1 A, 400 V	1N3613	Unitrode
VR1	Diode, zener, 5.1 V	1N4733	Motorola
U1	Voltage Regulator, 5 V	LM309K	Nat'l Semi.
U2,4	Dual Monostable multivibrator, TTL	74123	TI
U3	Quad 2-input OR gate, TTL	7432	TI
U5	Quad 2-input NOR gate bus driver, TTL	8881	DEC
U6,9,10	Dual comparator	LM393AN	Nat'l Semi.
U7	Hex Inverter, TTL	7404	TI
U8	Quad 2-input AND gate, TTL	7408	TI
HD	Heat sink, TO-3		

Table J-2 System Controller Power Control Board
Edge Connector Pin Identification

Pin	Signal	Direction
1	12.6 Vac	In *
2	Ground	-
3	12.6 Vac	In
4	Switch ground	-
5	DC ON switch contact	In
6	DC OFF switch contact	In
7	INITIALIZE ON switch contact	In
8	INITIALIZE OFF switch contact	In
9	RUN switch contact	In
10	HALT switch contact	In
11	RUN lamp return	In
12	5 Vdc lamp power	Out
13	Dc lamp return	In
14	DCONC (power supply control)	Out
15	BHALT	Out
16	BPOK	Out
17	BDCOK	Out
20	+5 Vdc power	In
21	Ground	-
22	+12 Vdc power	In

* "In" refers to signals accepted by board;
"Out" refers to signals put out by board.

Appendix K

System Clock Interface Details

K.1 APPENDIX OVERVIEW

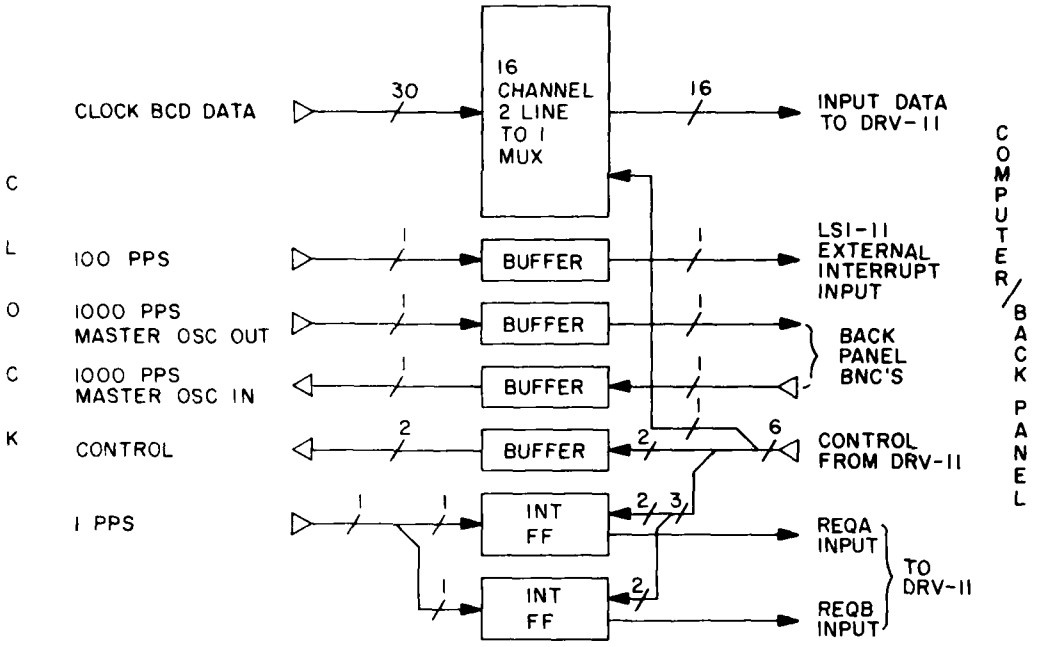
This appendix covers details of the system clock interface. It includes block and schematic diagrams of the interface circuit and gives specifications and a parts list for the interface circuit board. Card edge connector pin identifications are given in tabular form. The modifications necessary for external access to the clock oscillator chain are detailed as are procedures for using the resulting signal for system synchronization. Another section of this appendix covers software interface considerations, giving interface register location and bit identification information. A short computer program for checking out the interface is also included.

K.2 COMPUTER BACKPLANE

K.2.1 CIRCUIT DESCRIPTION

A block diagram of the clock interface is given in Figure K-1. The interface consists of a 16-channel 2 to 1 multiplexer to connect the clock BCD data to the LSI-11 parallel input port. Buffers for the 100 and 1000 pps bit streams are included as are buffers for the two clock control lines. Two flipflops are used to connect the 1 pps signal to the parallel port card interrupt inputs. They are reset by three signals from the computer.

Figure K-2 contains the schematic diagram of the circuits needed to implement this block diagram. Note that both interrupt flipflops (U6) are reset by the initialize signal from the computer.



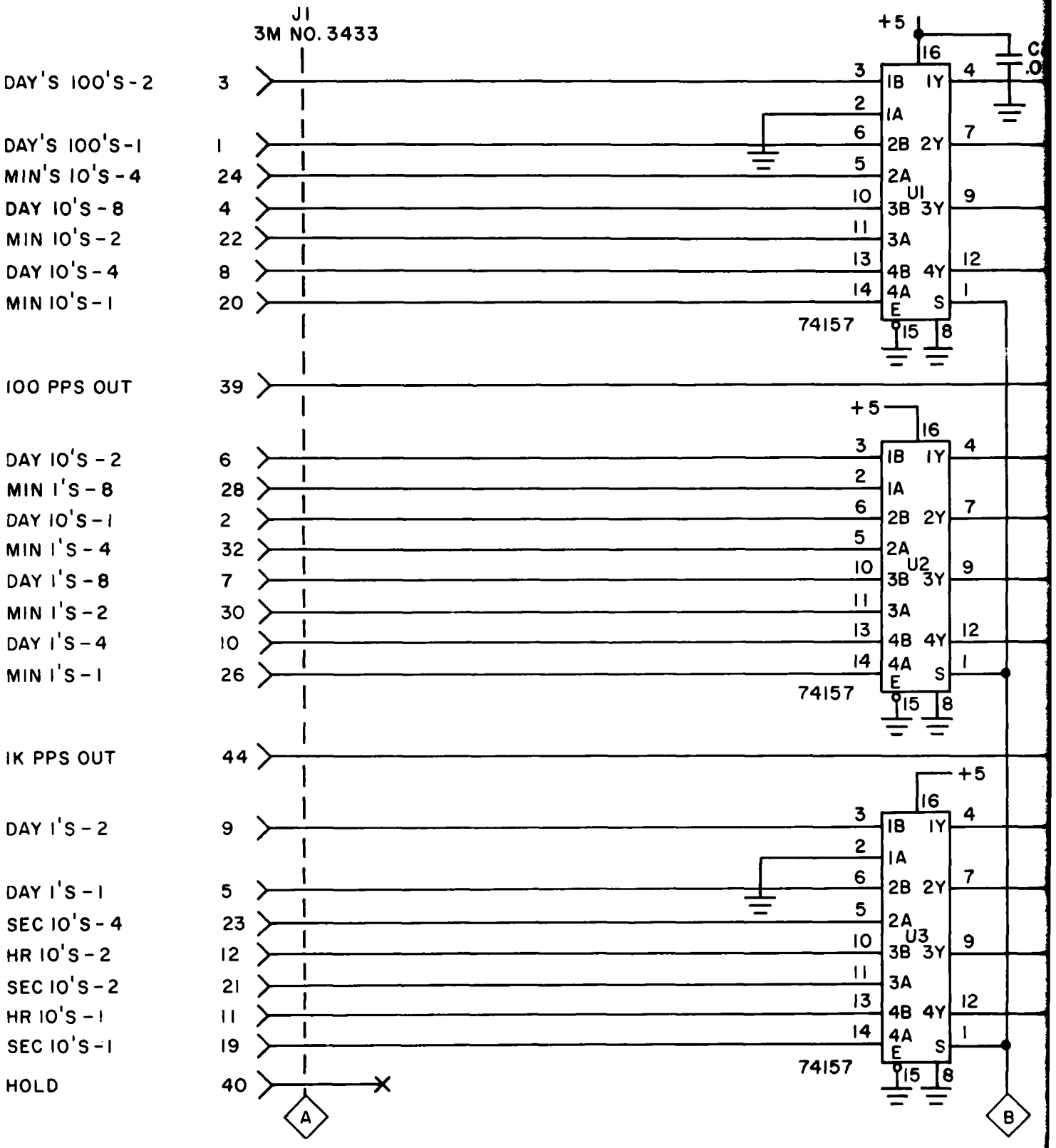
K-1. System Clock Interface Block Diagram

K.2.2 PHYSICAL DESCRIPTION

All components for the interface are mounted on a single 4.5 x 6.5 in. (11.4 x 16.5 cm) double-sided printed circuit board. Power connections to the board are made through the board's edge connector as are connections between the board and J6 and J7 on the interface chassis rear panel. (Ribbon cables connect these sockets to a DRV-11 parallel interface card located in the controller chassis.) Connections between the card and the system clock are made through a ribbon cable socket mounted on the card . Figure K-3 is a photograph of the interface card with parts identified. Table K-1 gives the board parts list and is keyed to the board photograph.

Connections between the interface card and the clock take place over a 50-conductor ribbon cable. One end of the cable is terminated with a 3M #3425-3000 50-pin plug for connecting to the card. The other cable end is split and connected to the two circuit board connectors on the back of the clock. Table K-2 gives the signal assignments of this cable, referenced to the ribbon cable socket on the circuit board.

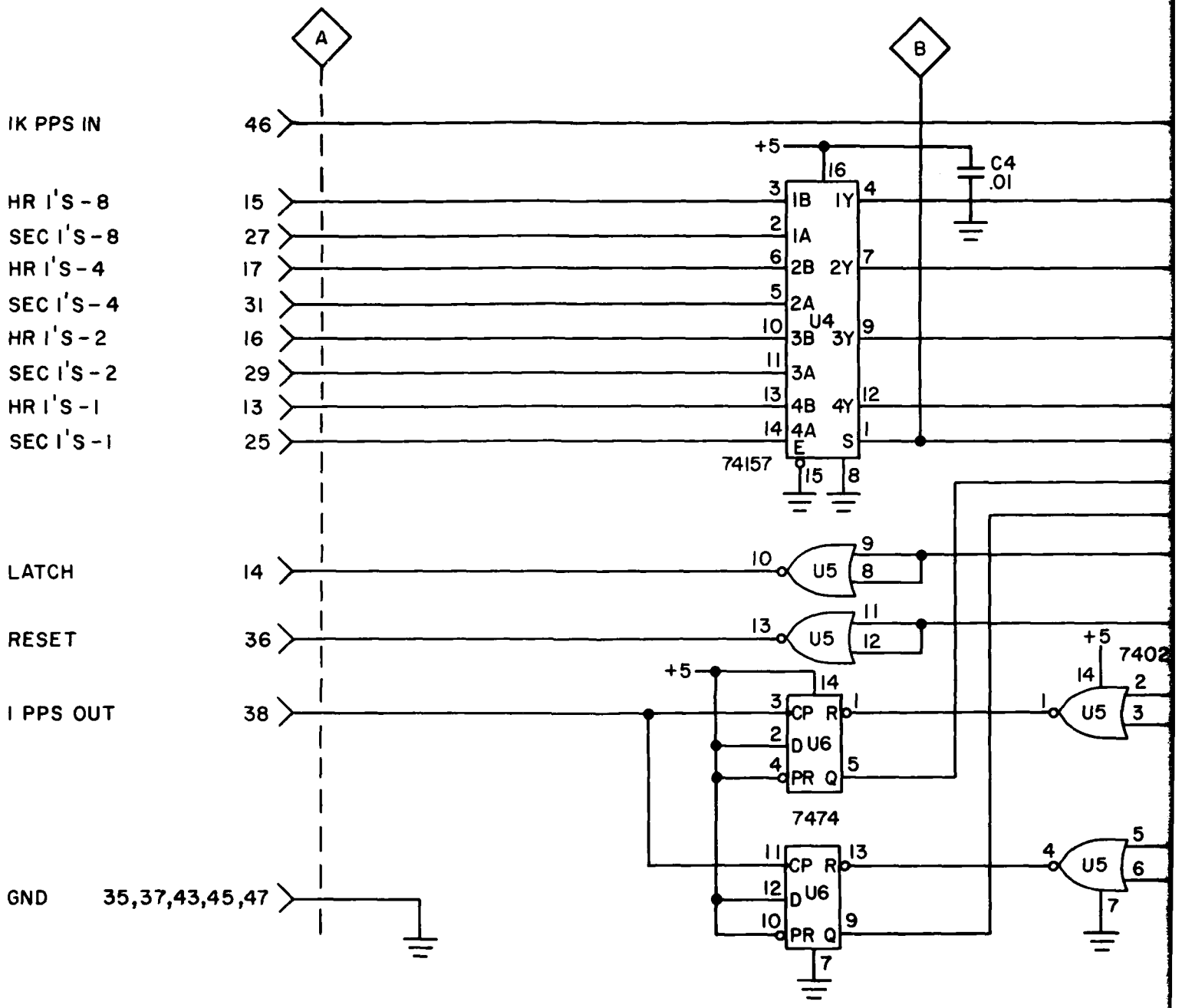
Connections between the interface card and the chassis back panel are made through the card edge connector, as are power and ground connections. The back panel connections are made via a 50-conductor ribbon cable. The card end of the cable is terminated with a 3M



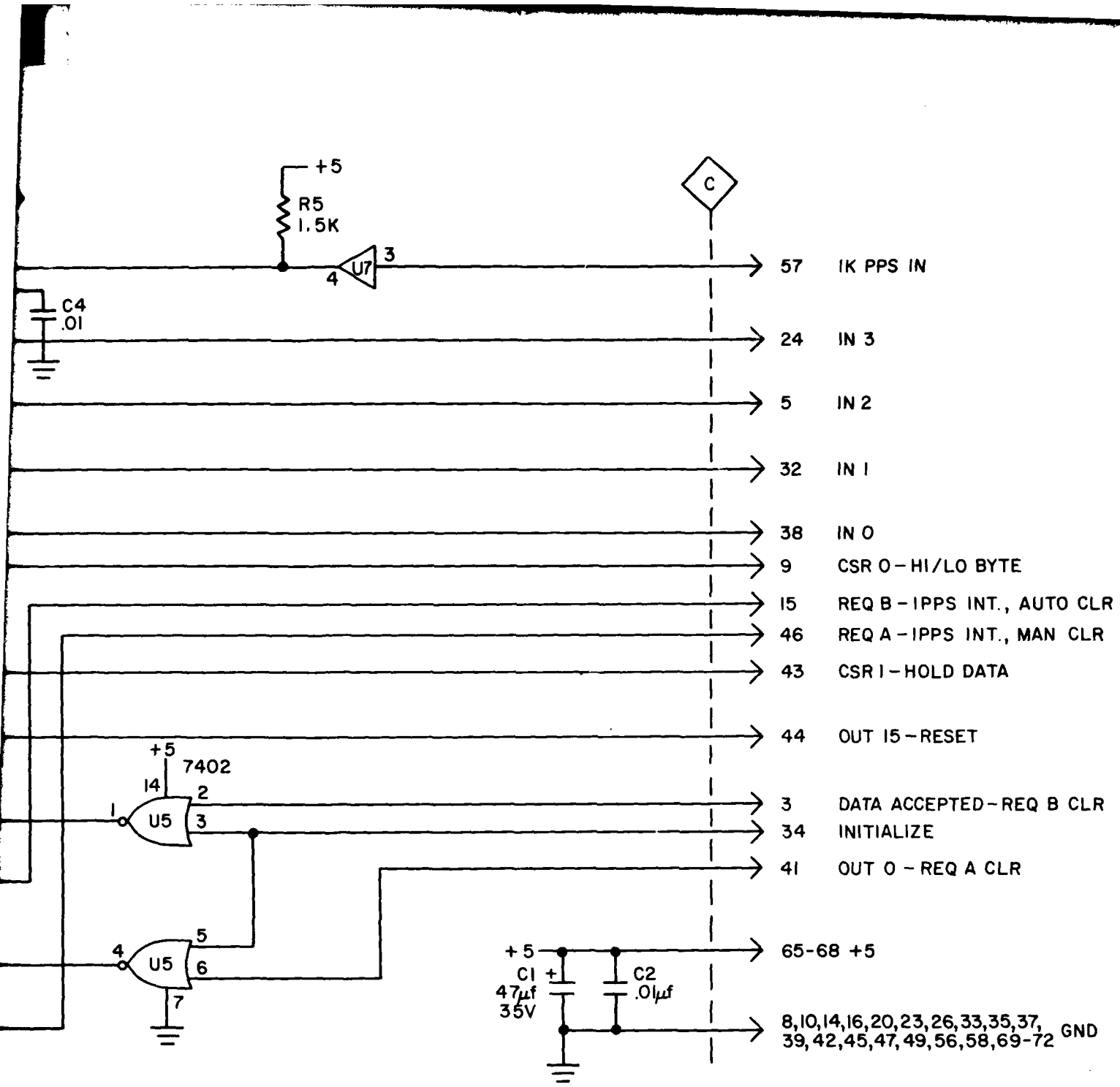
K-2. System Clock Interface Schematic

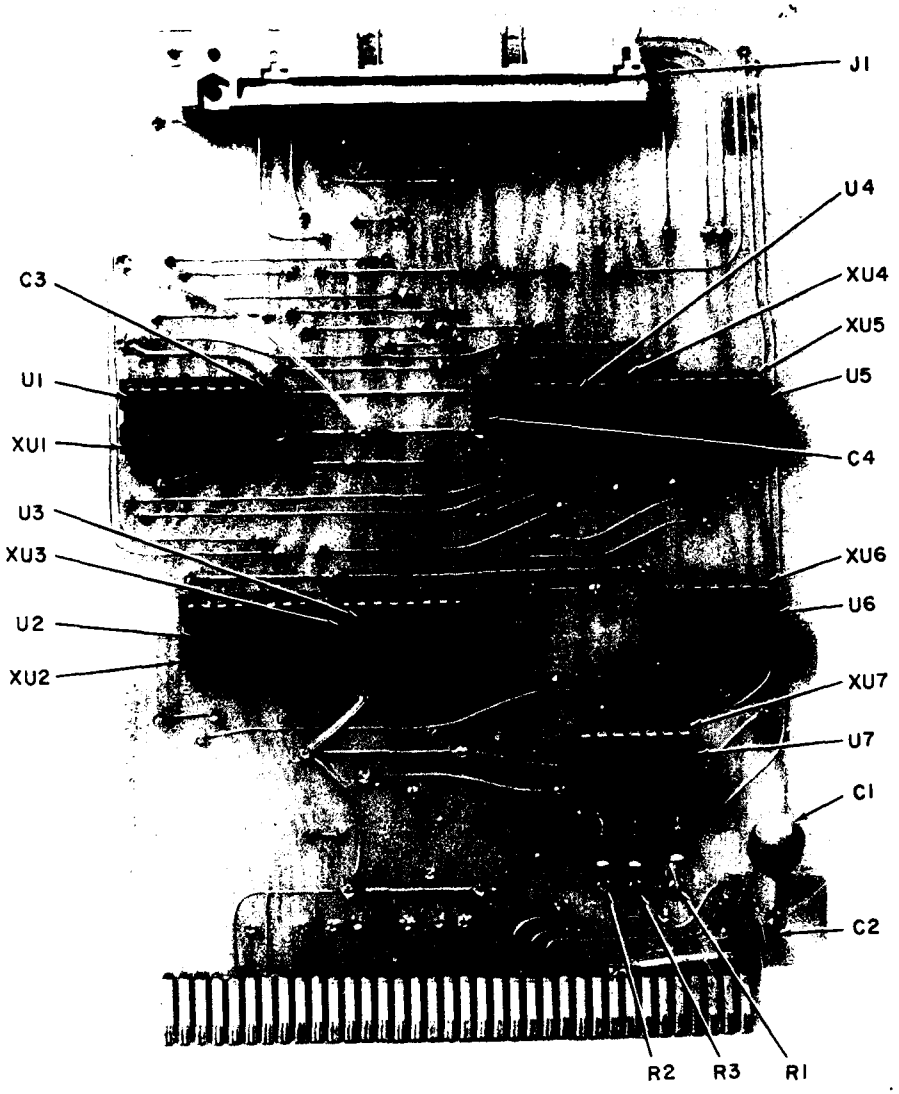
+5
C3
.01
U1
74157
R2
1.5K
U7
U2
R4
1.5K
7407
U3
EDGE
CONNECTOR
11 IN15
12 IN14
13 IN13
17 IN12
48 100 PPS
18 IN11
19 IN10
21 IN9
22 IN8
55 IK PPS
25 IN7
27 IN6
29 IN5
31 IN4
B
C

2



K-2. System Clock Interface Schematic (Cont.)


+5
R5
1.5K
U7
3
4
C
C4
.01
57 IK PPS IN
24 IN 3
5 IN 2
32 IN 1
38 IN 0
9 CSR 0 - HI/LO BYTE
15 REQ B - IPPS INT., AUTO CLR
46 REQ A - IPPS INT., MAN CLR
43 CSR 1 - HOLD DATA
44 OUT 15 - RESET
+5
7402
14
2
1
U5
3
3 DATA ACCEPTED - REQ B CLR
34 INITIALIZE
41 OUT 0 - REQ A CLR
5
4
U5
6
7
+5
C1
47μf
35V
C2
.01μf
65-68 +5
8,10,14,16,20,23,26,33,35,37,
39,42,45,47,49,56,58,69-72 GND



K-3. System Clock Interface Component Locations

#3307-0000 socket that plugs directly onto the edge connector socket. The other end of the cable is split, with the first 40 wires terminated in a 3M #3331 socket. This socket appears as J7 on the chassis rear panel. The other 10 wires in the cable are soldered to a second #3331 socket on the chassis rear panel (J6). Table K-3 identifies the signals appearing on the edge connector together with their ultimate destination.

Table K-1 System Clock Interface Parts List

Part	Noun	Mfgr Part No.	Manufacturer
XU1-XU4	Low profile DIP IC socket, 16-pin	516-AG10D	Augat
XU5-XU7	Low profile DIP IC socket, 14-pin	514-AG10D	Augat
R1-R3	Resistor, 1.5K Ω, 1/2 W, 2%, metal film	C5	Corning
C1	Capacitor, 47 μF, 35 V, tantalum	199D476X0035A2	Sprague
C2-C4	Capacitor, 0.01 μF, 200 V	CKR06	AVX
U1-U4	Quad 2-input data selector, TTL	74157	TI
U5	Quad 2-input NOR gate, TTL	7402	TI
U6	Dual D-type flipflop, TTL	7474	TI
U7	Hex open collector buffer, TTL	7407	TI
J1	Socket, 50-pin ribbon cable	3433-10[illegible]2	3M

Table K-2 System Clock Cable Pin Identification

Connector: 3M #3433-1002
Mating Connector: 3M #3425-3000

Clock Connectors (J1 AND J2): Vector R644

Interface			Clock	
Pin	Signal	Direction	Connector	Pin
1	Day 100's 1	In *	J1	W
2	Day 10's 1	In	J1	19
3	Day 100's 2	In	J1	V
4	Day 10's 8	In	J1	18
5	Day 1's 1	In	J1	U
6	Day 10's 2	In	J1	17
7	Day 1's 8	In	J1	T
8	Day 10's 4	In	J1	16
9	Day 1's 2	In	J1	S
10	Day 1's 4	In	J1	R
11	Hour 10's 1	In	J1	P
12	Hour 10's 2	In	J1	N
13	Hour 1's 1	In	J1	M
14	LATCH command	Out	J1	11
15	Hour 1's 8	In	J1	L
16	Hour 1's 2	In	J1	K
17	Hour 1's 4	In	J1	J
19	Sec 10's 1	In	J1	H
20	Min 10's 1	In	J1	7
21	Sec 10's 2	In	J1	F
22	Min 10's 2	In	J1	6
23	Sec 10's 4	In	J1	E
24	Min 10's 4	In	J1	5
25	Sec 1's 1	In	J1	D
26	Min 1's 1	In	J1	4
27	Sec 1's 8	In	J1	C
28	Min 1's 8	In	J1	3
29	Sec 1's 2	In	J1	B
30	Min 1's 2	In	J1	2
31	Sec 1's 4	In	J1	A
32	Min 1's 4	In	J1	1
35	Ground	-	J2	2,B
36	RESET command	Out	J2	3,C
37	Ground	-	J2	2,B
38	1 pps clock	In	J2	4,D
39	100 pps clock	In	J2	5,E
40	HOLD command	Out	J2	6,F
43	Ground	-	J2	21,Y
44	1000 pps clock	In	J2	16,T
45	Ground	-	J2	21,Y
46	1000 pps clock	Out	J2	15,S
47	Ground	-	J2	21,Y

* "In" refers to signals accepted by the interface circuits from the clock; "Out" refers to signals put out to the clock.

K.3 MINIMUM SYSTEM COMPUTER CONFIGURATION

To allow time synchronization between the SDAS and other systems, an access to the SDAS clock master oscillator is useful. Once the oscillator signal is brought out of the clock, it can be used in a number of ways for synchronization, as discussed below. Figure K-4 contains an excerpt from the SDAS clock schematic diagram showing the frequency divider chain of the clock. The crystal oscillator frequency of 1.0 MHz is repeatedly divided by 10 to yield the 1 pps

Table K-3 System Clock Interface
Edge Connector Pin Identification

Interface			Rear Panel	
Pin	Signal	Direct	Conn/Pin	Signal
3	REQ B interrupt clear	In *	J7/3	Data accepted pulse
5	Hr 1's 4 / Sec 1's 4	Out	J7/5	Input bit 2
8	Ground	-	J7/8	Ground
9	Mux control signal	In	J7/9	CSR 0
10	Ground	-	J7/10	Ground
11	Day 100's 2 / High	Out	J7/11	Input bit 15
12	Day 100's 1 / Min 10's 4	Out	J7/12	Input bit 14
13	Day 10's 8 / Min 10's 2	Out	J7/13	Input bit 13
14	Ground	-	J7/14	Ground
15	1 pps interrupt	Out	J7/15	REQ B Input
16	Ground	-	J7/16	Ground
17	Day 10's 4 / Min 10's 1	Out	J7/17	Input bit 12
18	Day 10's 2 / Min 1's 8	Out	J7/18	Input bit 11
19	Day 10's 1 / Min 1's 4	Out	J7/19	Input bit 10
20	Ground	-	J7/20	Ground
21	Day 1's 8 / Min 1's 2	Out	J7/21	Input bit 9
22	Day 1's 4 / Min 1's 1	Out	J7/22	Input bit 8
23	Ground	-	J7/23	Ground
24	Hr 1's 4 / Sec 1's 4	Out	J7/24	Input bit 3
25	Day 1's 2 / High	Out	J7/25	Input bit 7
26	Ground	-	J7/26	Ground
27	Day 1's 1 / Sec 10's 4	Out	J7/27	Input bit 6
29	Hr 10's 2 / Sec 10's 2	Out	J7/29	Input bit 5
30	Ground	-	J7/30	Ground
31	Hr 10's 1 / Sec 10's 1	Out	J7/31	Input bit 4
32	Hr 1's 2 / Sec 1's 2	Out	J7/32	Input bit 1
33	Ground	-	J7/33	Ground
34	Clear interrupts	In	J7/34	Initialize
35	Ground	-	J7/35	Ground
37	Ground	-	J7/37	Ground
38	Hr 1's 1 / Sec 1's 1	In	J7/38	Input bit 0
39	Ground	-	J7/39	Ground
41	REQ A interrupt clear	In	J6/3	Output bit 0
42	Ground	-	J6/25	Ground
43	LATCH control	In	J6/26	CSR 1
44	RESET control	In	J6/30	Output bit 15
45	Ground	-	J6/31	Ground
46	1 pps interrupt	Out	J6/32	REQ A input
47	Ground	-	J6/33	Ground
48	100 pps	Out	J6/49	BEVNT**
49	Ground	-	J6/50	Ground**

Table K-3 System Clock Interface Edge Connector
Pin Identification (contd)

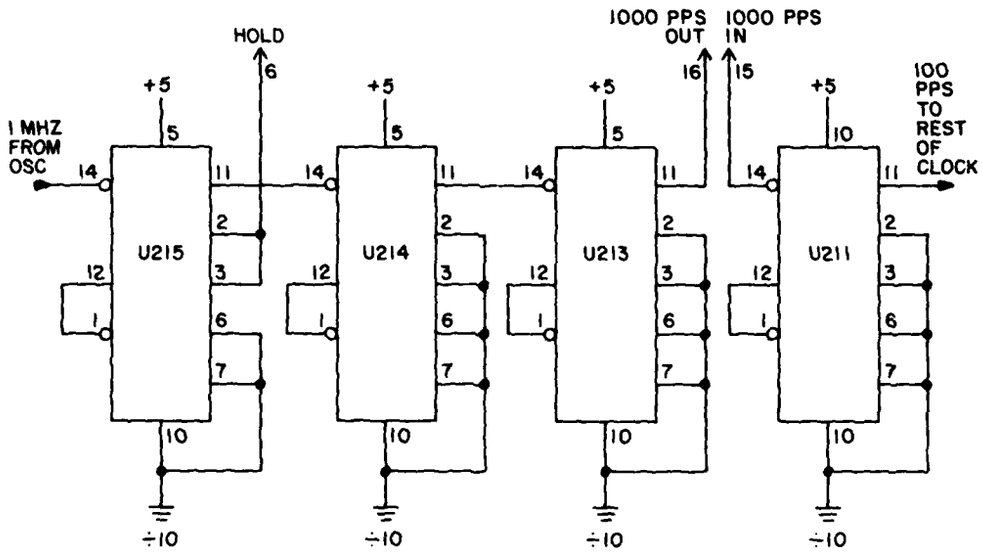
55	1000 pps	Out	J10	1000 pps out
56	Ground	-	J10	Ground
57	1000 pps	In	J11	1000 pps in
58	Ground	-	J11	Ground
65-68	+5 Vdc power	-		
69-72	Power ground	-		

* "Out" refers to signals put out by the clock interface card;
"In" refers to signals accepted by the card

** Destination is power control card edge connector.

Note:

-- External and internal pin numbers same as connector pin numbers.
-- 1's, 10's, 100's refer to digit of seconds, minutes, hours, and days data.
-- 1, 2, 4, 8 refer to BCD bit (eg. "Hr 1's 1" is bit 1 of digit 1 of the hour data segment).



K-4. System Clock Schematic Excerpt

input for the clock counters. As shown in the figure, the modification consists of breaking the chain at the 1000 pps point and feeding the 1000 pps stream to pin 16 on the edge connector (J2). Pin 15 on the connector is run to the input to the next counter stage input.

These two signals (1000 pps output and input) are buffered on the interface card and run to the interface edge connector. From there, they run via coaxial cable to a pair of BNC connectors (J10 and J11) on the rear panel of the interface chassis. For normal use, a short piece of coax (with BNC connectors on both ends) is jumpered between these connectors.

K.4 DRV-11 MODIFICATION INFORMATION

Several methods for time synchronization between the SDAS and another system using the 1000 pps clock signal are discussed below. The simplest method is to insert a BNC "T" connector in the jumper between J10 and J11 on the chassis rear panel. This signal can then be fed to the other system for its use.

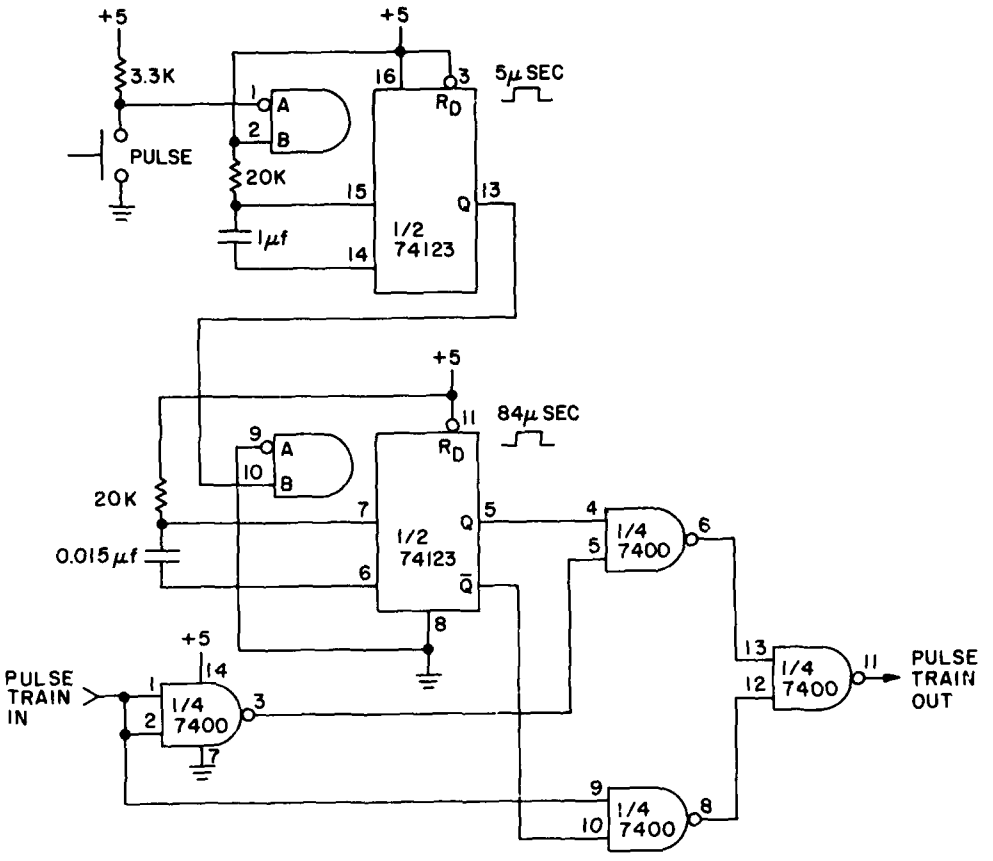
Alternatively, a 1000 pps TTL-level signal from an oscillator on another system can be connected to J11, with nothing connected to J10. The SDAS system clock would then be slaved to that oscillator.

A more flexible, if more complex, synchronization scheme involves the use of a pulse insertion circuit, such as the one shown in Figure K-5.

This circuit consists of a dual retriggerable oneshot multivibrator that puts out one pulse every time the "PULSE" button is pushed. The first oneshot debounces the "PULSE" button while the second provides the actual output pulse. Two-input NAND gates are used to add the pulse to the clock pulse train. If this circuit is connected to J11 and the oscillator output (either from J10 or an external source), one additional pulse is added to the pulse stream with each button push. This pulse advances the SDAS clock relative to the oscillator output by 1 msec. If the 100 or 1 pps clock output signals is compared with a similar frequency signal from another source (using an oscilloscope or a high-speed chart recorder), the SDAS clock can be advanced to bring the two into synch.

Figure K-6 shows an instance where this circuit could be used. As shown, an external system with its own digital clock is to be synchronized with the SDAS. A 1000 pps signal from this system functions as the master oscillator for the SDAS clock. The SDAS clock is manually set to be slightly slower than the external clock. By observing the 1 pps SDAS clock output and a time signal from the external clock (such as an IRIG serial time code) on the oscilloscope, the relative timing of the two can be noted. Pulses are then inserted into the SDAS clock stream to advance the SDAS clock until the two signals are in synch, thus synchronizing the two systems.

The above represent three of the simplest synchronization procedures. More sophisticated ones can be developed as the application dictates.



K-5. Pulse Insertion Circuit Schematic

K.5.1 INTERFACE REGISTER CONTENTS

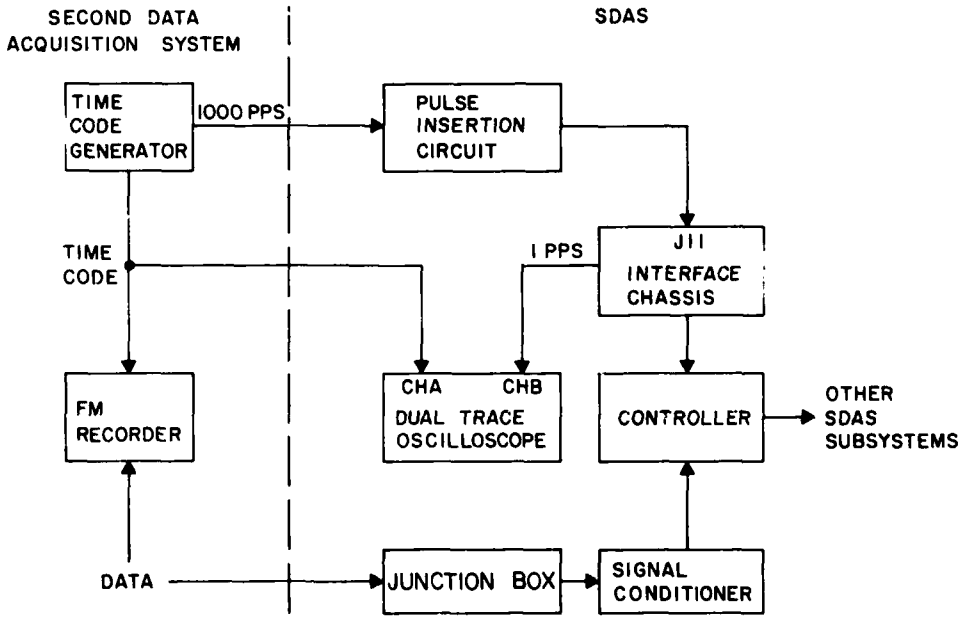
The SDAS system clock interface described above is connected to a single DRV-11 parallel line interface module in the controller computer. System software has access to the three registers (control and status, input, and output) on the module for reading and controlling the clock. Tables K-4 through K-6 give bit identification for these registers; register addresses are as shown in Appendix I, Figure I-3. (Bit Ø is LSB, bit 15 is MSB.)

K.5.2 CLOCK INTERFACE CHECKOUT SOFTWARE

Listed in Tables K-7 and K-8 is a simple program to checkout the clock interface. The program was written in FORTRAN (DEC FORTRAN IV, version V01C-3A) under DEC's RT-11 operating system (RT-11FB, version V02C-02B). Also listed is a subroutine (GETIME) written in DEC's PDP-11 operating system (MACRO). This subroutine is called from the main program to reformat the clock data prior to display. IPEEK and IPOKE are two DEC FORTRAN subroutines to read and write, respectively, data to/from specific memory locations. EXIT is a DEC subroutine to return to the operating system. They are contained in DEC's SYSLIB FORTRAN utility library which must be linked to the program.

When the program is loaded and executed, it responds with TYPE D TO EXIT, ANYTHING TO READ TIME. If D<cr> is typed on the console, the program returns to the operating system. If any other entry (or none) is made followed by <cr>, the program will display current time as ERC TIME = DDD HH:MM:SS and will repeat the opening message.

To check out the clock interface, the clock should be manually set to 000 00:00:xx, 111 11:11:xx, 222 22:22:xx, 344 04:44:xx, 388 08:08:xx and the time read out by the program. This tests all the day, hour, and minute data bits. Since the seconds bits cannot be manually set, sufficient readings should be taken to verify that all are connected properly.



K-6. Multisystem Synchronization Example

Table K-4 *System* Clock Control and Status Register Bit Identification

Bit	DEC Bit Name	Type	Functional Description
Ø	CSRØ	R/W	HI/LO SELECT. When loaded high, hours and days read; when loaded low, minutes and seconds read.
1	CSR1	R/W	DATA HOLD. Input data latched when loaded high; when low, data follows time count. Full time signal (days, hrs, mins, and secs) latched.
5	INT ENB B	R/W	1 pps INTERRUPT ENABLE B. Computer interrupted at 1 pps rate when bit loaded high; no interrupt when loaded low. Interrupt cleared automatically when time data read.
6	INT ENB A	R/W	1 pps INTERRUPT ENABLE A. Computer interrupted at 1 pps rate when bit loaded high; no interrupt when bit low. Interrupt must be cleared by program using output bit Ø.
7	REQ A	R	INTERRUPT A FLAG. Shows status of 1 pps input connected to REQ A. Cleared under program control using output bit Ø.
15	REQ B	R	INTERRUPT B FLAG. Shows status of 1 pps input connected to REQ B. Cleared when time read.

Note:
-- *Under* TYPE, "R" implies that bit status can be read under program control; "W" implies that bit can be loaded by the program.

Table K-5 System Clock Output Register Bit Identification

Bit	Functional Description
Ø	CLEAR INTERRUPT. Clears 1 pps interrupt connected to REQ B.
15	RESET. Reset clock to 000 00:00:00.

Table K-6 System Clock Input
Register Bit Identification

Bit	Contents
0	Hour 1's 1 / Second 1's 1
1	Hour 1's 2 / Second 1's 2
2	Hour 1's 4 / Second 1's 4
3	Hour 1's 8 / Second 1's 8
4	Hour 10's 1 / Second 10's 1
5	Hour 10's 2 / Second 10's 2
6	Day 1's 1/ Second 10's 4
7	Day 1's 2 / High
8	Day 1's 4 / Minute 1's 1
9	Day 1's 8 / Minute 1's 2
10	Day 10's 1 / Minute 1's 4
11	Day 10's 2 / Minute 1's 8
12	Day 10's 4 / Minute 10's 1
13	Day 10's 8 / Minute 10's 2
14	Day 100's 1 / Minute 10's 4
15	Day 100's 2 / High

Notes:

-- 1's, 10's, and 100's refer to digit of time unit.
-- 1, 2, 4, and 8 refer to BCD bit of digit value.
-- "High" implies tied permanently to +5 Vdc.

Table K-7 System Clock Interface Checkout Program Listing

```
        PROGRAM ERC CLOCK CHECK
C
C       PROGRAM READS TIME FROM ERC CLOCK INTO ARRAY INTIME AND CALLS
C       SUBROUTINE GETIME TO CONVERT TO ARRAY ITIME FOR DISPLAY ON
C       CONSOLE. MUST BE LINKED WITH GETIME AND SYSLIB.
C
        DIMENSION INTIME(2),ITIME(4)
        LOGICAL*1 ANS,DONE
        DATA DONE/1HD/
100     TYPE 10
10      FORMAT (' TYPE D TO EXIT, ANYTHING TO READ TIME')
        ACCEPT 20,ANS
20      FORMAT (A1)
        IF (ANS.EQ.DONE) CALL EXIT
        CALL IPOKE ("167770,3)
        INTIME (1)=IPEEK ("167774)
        CALL IPOKE ("167770,2)
        INTIME (2)=IPEEK ("167774)
        CALL IPOKE ("167770,0)
        CALL GETIME (INTIME,ITIME)
        TYPE 30,(ITIME(N),N=1,4)
30      FORMAT (' ERC TIME = ',I3,':',I2,':',I2,':',I2)
        GOTO 100
        END
```

Table K-8 Subroutine GETIME Listing

```
          .TITLE GETIME SUBR FOR FORTRAN  LSI-11 VERSION
          .MCALL .REGDEF
          .GLOBL GETIME,GETIM1
          ;
          ;REQUIREMENTS FOR USE:
          ;    THE RAW TIME MUST BE PASSED INTO THIS SUBROUTINE IN
          ;    AN ARRAY OF DIMENSION 2.   THIS ARRAY MUST BE THE FIRST
          ;    ARGUMENT IN THE SUBROUTINE CALL STATEMENT.
          ;    TIME IS RETURNED IN AN INTEGER ARRAY OF DIMENSION 4 WHOSE
          ;    ADDRESS MUST BE PASSED THROUGH SUBROUTINE CALL STATEMENT
          ;
          .REGDEF
          .ENABL  LSB
GETIME:   MOVB (R5)+,RØ         ;GET   ARGUMENTS TRANSFERRED
          SUB  2,RØ
          BNE 5$                ;BRANCH IF NOT 2 ARGUMENTS
          INC R5
          MOV (R5)+,R4          ;ADDR OF INPUT TIME
          MOV @R5,R5            ;ARRAY ADDR FOR RETURNED TIME
GETIM1:   MOV  TABLE,R1         ;GETIM1 IS ENTRY POINT FROM SUBR GETSTM
2$:       MOVB (R4)+,-(SP)      ;GET WORD OF RAW TIME
          MOVB (R4)+,1(SP)
          MOV (SP)+,R3
3$:       CLR R2                ;CLEAR HIGH SHIFT REGISTER
          MOVB (R1)+,RØ         ;SHIFT COUNT
          ASHC RØ,R2            ;SHIFT BITS FOR THIS DIGIT INTO R2
          MOV R2,-(SP)          ;SAVE ON STACK
          CMP @SP, 1Ø.          ;MAKE SURE NO STUCK BITS
          BLT 33$
          SUB  1Ø.,@SP
33$:      TSTB @R1              ;MORE DIGITS IN THIS TIME UNIT?
          BGT 3$                ;BRANCH BACK IF SO
          MOV  SUM,RØ
          MOVB (R1)+,R2         ;MAX. POWER OF TEN NEEDED (NEGATED)
          MOV (SP)+,(RØ)+       ;STORE LEAST SIGNIFICANT DIGIT
          MOV R3,(RØ)+          ;STORE REMAINDER OF TIME WORD
4$:       MOV (SP)+,R3          ;NEXT SIGINIFICANT BIT
          MUL (RØ)+,R3          ;TIMES TENS POWER
          ADD R3,SUM            ;ADD TO SUM
          INC R2                ;DONE ALL DIGITS FOR THIS UNIT?
          BNE 4$                ;NO - BRANCH BACK
          MOV SUM,(R5)+         ;RETURN UNIT TO ARRAY
          MOV SUM+2,R3          ;GET REMAINDER OF TIME WORD
          TSTB @R1              ;DONE WITH THIS WORD?
          BGT 3$                ;NO - BRANCH
          TSTB (R1)+            ;DONE BOTH INPUT WORDS OF TIME?
          BLT 2$                ;NO - BRANCH
5$:       RTS PC                ;YES - RETURN
          .DSABL LSB
SUM:      .BLKW 2
TENS:     .WORD 1Ø.,1ØØ.
TABLE:    .BYTE 2,4,4,-2,2,4,-1,-7,4,4,-1,4,4,-1,Ø
          .END
```

Appendix L

Tape Recorder Interface Details

L.1 APPENDIX OVERVIEW

This appendix provides detailed information on the interface circuitry for the magnetic tape recorder used with the SDAS. It includes block diagrams and schematics of the circuits, parts lists, and connector pin identifications. It also includes a discussion of software interface considerations and a listing of a short interface/recorder checkout program.

L.2 REPLACEMENT WRITE ADAPTER CIRCUIT BOARD

The replacement write interface card plugs into the rear of the Kennedy tape recorder. It replaces the board supplied by the manufacturer. Mounted on the board are six dual differential line receivers (see Figure L-1). The receivers accept differential digital signals from the write interface and convert them to TTL levels for the Kennedy inputs. The response of each receiver is tailored to the timing requirements of the signal being received. Also included on the board are four jumpers (S1 through S4) to configure the recorder as listed in Table L-1.

Figure L-2 gives a view of the component side of the circuit board. A parts list for the board, keyed to the figure, is contained in Table L-2.

Connections between the interface card and the Kennedy recorder are made through the card edge connector. See schematic diagram for connector board, type 4463-001, in the recorder operation and

maintenance manual for details on the edge connector pin identification.

One additional wire must be added to the Kennedy formatter chassis to supply power to the new write card. A wire-wrap jumper must be installed between pin 18 on the write card socket and pin D of the socket for Kennedy card 3607-003. This card is located immediately above the write interface card in the formatter card cage.

Signals between this card and the write interface card in the interface chassis flow through J1. Pin identification on this connector is identical to that on J13 on the interface chassis back panel (see Table L-8 below).

L.3 INTERFACE CIRCUIT BOARDS

L.3.1 INTERFACE BLOCK DIAGRAM

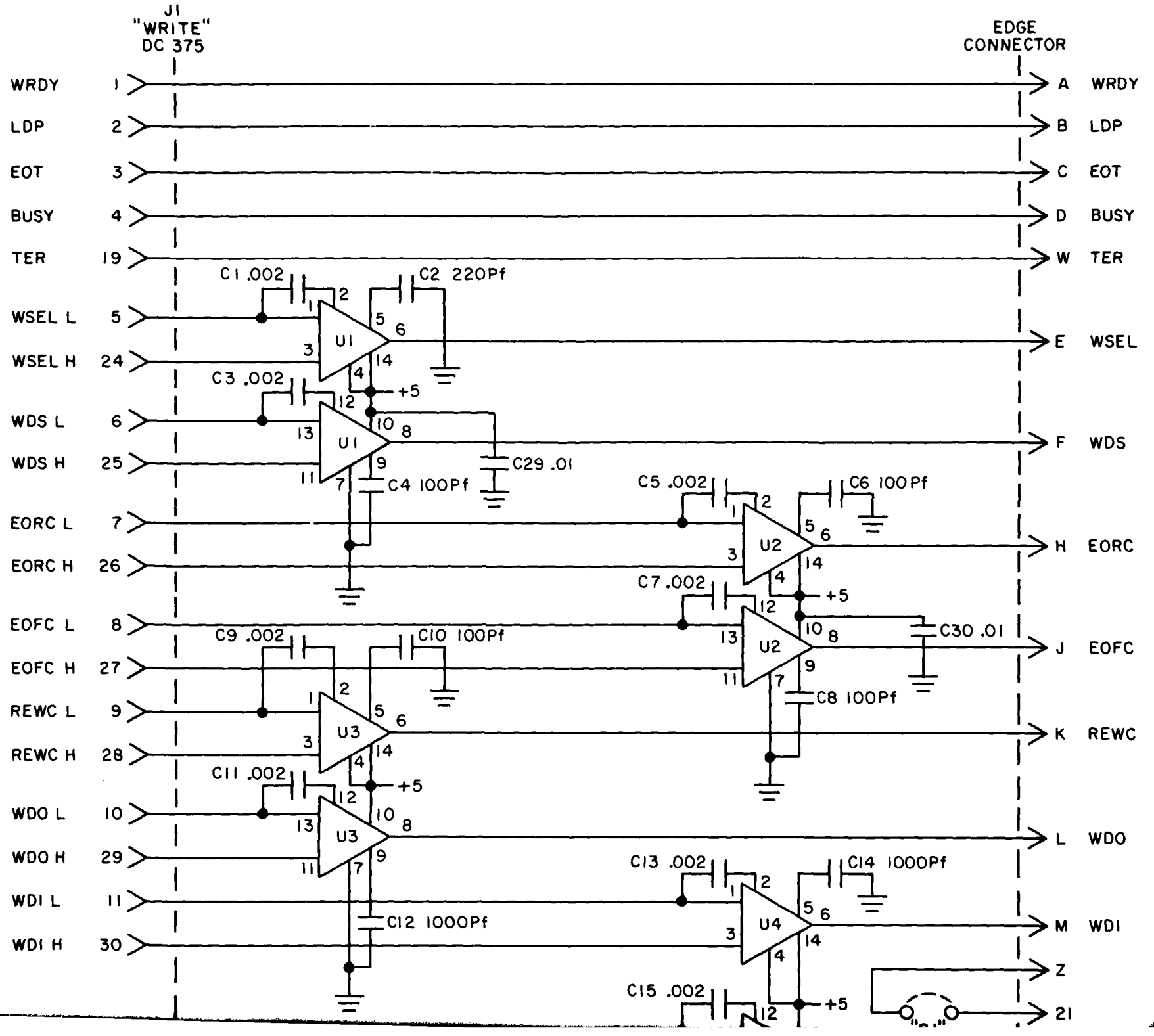
The read and write interface cards, located in the interface chassis card cage, provide the digital interfaces between the tape recorder and the parallel line card in the system computer. The read, write, status, and control interface functions performed by the interface are split between the two cards. Figure L-3 shows an overall block diagram of the interface circuitry; it is discussed below.

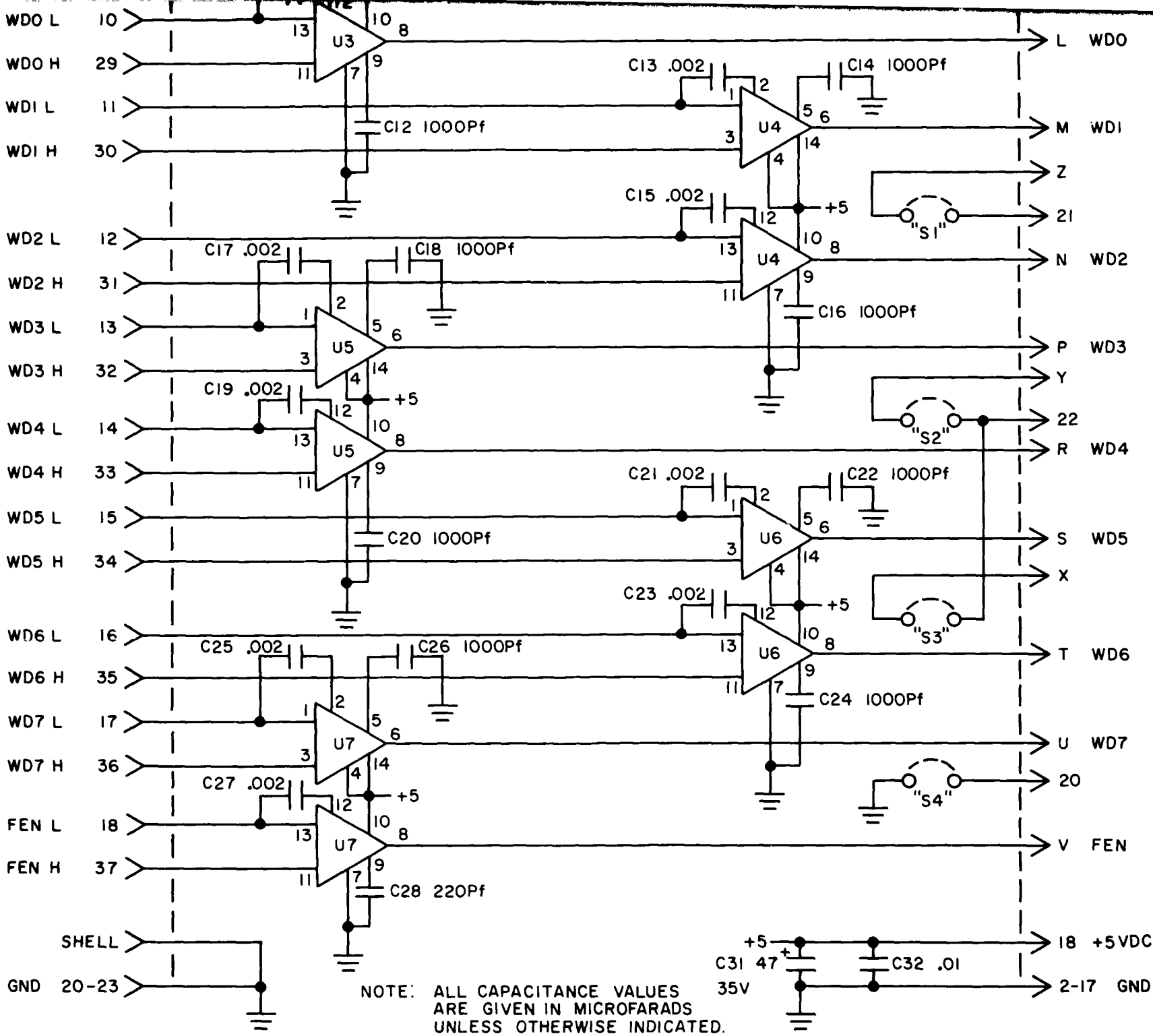
Byte-parallel data for recording comes from the DRV-11 parallel interface card in the system controller. The signals are conditioned on the cards and fed to the recorder in differential form. The differential line drivers on the card are connected to provide signal inversions to match the DRV-11 positive logic to the negative (low true) logic required by the recorder.

The recorder output signals use negative logic also. Therefore, the byte-parallel read data and all recorder status lines are inverted to be compatible with the computer's positive logic. Also, all recorder output lines use open collector line drivers, so pullup resistor networks are used to provide proper signal termination.

Two of the status lines from the recorder are pulses as opposed to levels. To insure that the computer reads these properly, pulse-to-level conversion flipflops are used. These and other recorder status signals are combined to yield a composite error signal. This signal is fed to the computer for error interrupt and identification purposes.

Most commands to the recorder are in the form of pulses. A pulse-generator oneshot multivibrator converts a level change from the computer to a pulse. This pulse is combined with command and status bits from the DRV-11 to generate the 10 control signals for the recorder. Six of these signals are associated with writing data to tape. They are converted to differential form to match the differential line receivers added to the recorder.


J1
"WRITE"
DC 375
EDGE
CONNECTOR
WRDY 1
LDP 2
EOT 3
BUSY 4
TER 19
WSEL L 5
WSEL H 24
WDS L 6
WDS H 25
EORC L 7
EORC H 26
EOFC L 8
EOFC H 27
REWC L 9
REWC H 28
WDO L 10
WDO H 29
WDI L 11
WDI H 30
A WRDY
B LDP
C EOT
D BUSY
W TER
E WSEL
F WDS
H EORC
J EOFC
K REWC
L WDO
M WDI
Z
21
C1 .002
C2 220Pf
U1
C3 .002
C4 100Pf
C29 .01
+5
C5 .002
C6 100Pf
U2
C7 .002
C8 100Pf
C30 .01
C9 .002
C10 100Pf
U3
C11 .002
C12 1000Pf
C13 .002
C14 1000Pf
U4
C15 .002



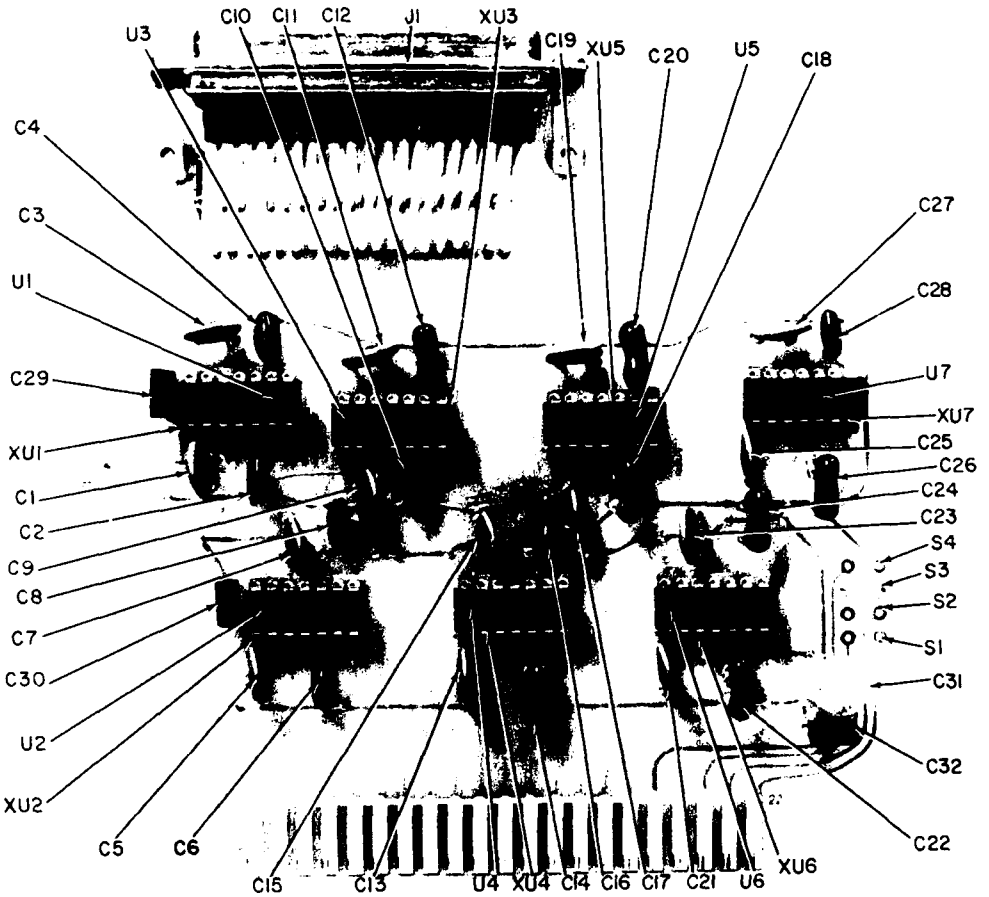
L-1. Tape Recorder Write Adapter Schematic

Table L-1 Tape Recorder Write Adapter Jumper Identification

Jumper	Installed	Removed
S1	7 track	9 track
S2	7 track	9 track
S3	9 track	7 track
S4	RAW disable	RAW enable

Notes:

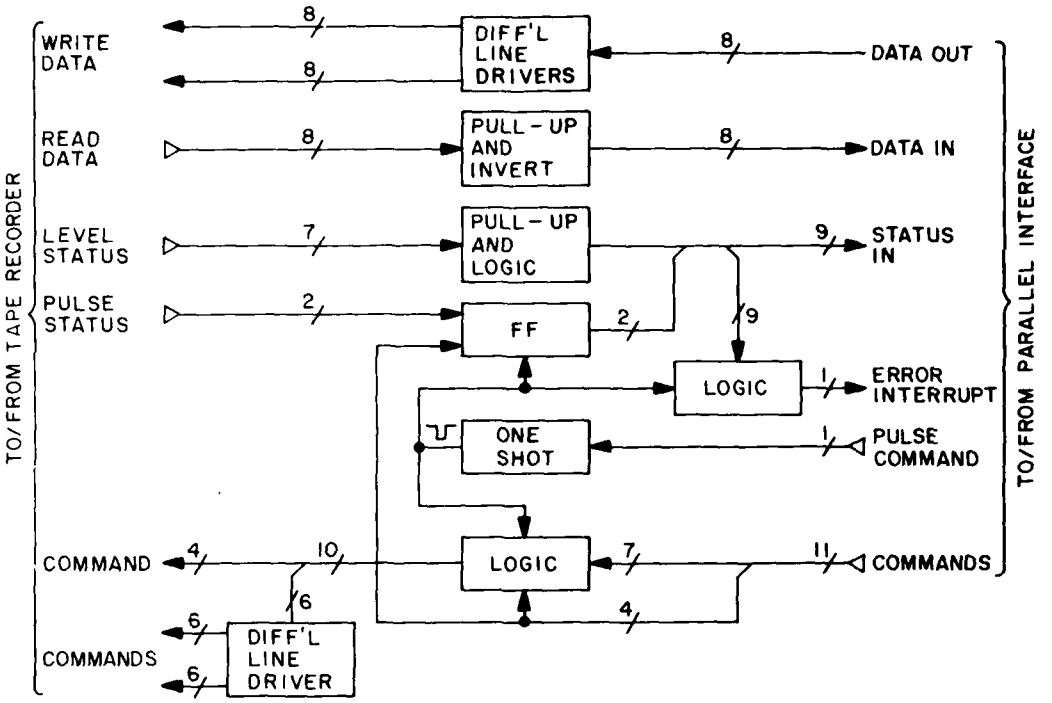
-- "7 track" implies 7 track tape record/playback.
-- "9 track" implies 9 track tape record/playback.
-- RAW = Read After Write error check.



L-2. Tape Recorder Write Adapter Component Locations

Table L-2 Tape Recorder Write Adapter Parts List

Part	Noun	Mfgr Part No.	Manufacturer
XU1-XU7	Low profile DIP IC socket, 14-pin	514-AG10D	Augat
C1,3,5,7,9,11, 13,15,17,19,21, 23,25,27	Capacitor, 0.002 μF, 1 kV, 20%, ceramic	DD202	Centralab
C2,28	Capacitor, 220 pF, 50 V, 5%, mica	CM05F221J03	Arco
C4,6,8,10	Capacitor, 100 pF, 500 V, mica	CM4FD101G0	Cornell-Dubilier
C12,14,16,18, 20,22,24,26	Capacitor, 1000 pF, 100 V, 2%, mica	DL-15-102G	Arco
C31	Capacitor, 47 μF, 35 V, tantalum	199D476X0035A2	Sprague
C29,30,32	Capacitor, 0.01 μF, 200 V	CKR06	AVX
U1-U7	Dual differential line receiver	DS8820N	Nat'l Semic.
J1	Socket, 37-pin "D" type	DD37S	Cannon



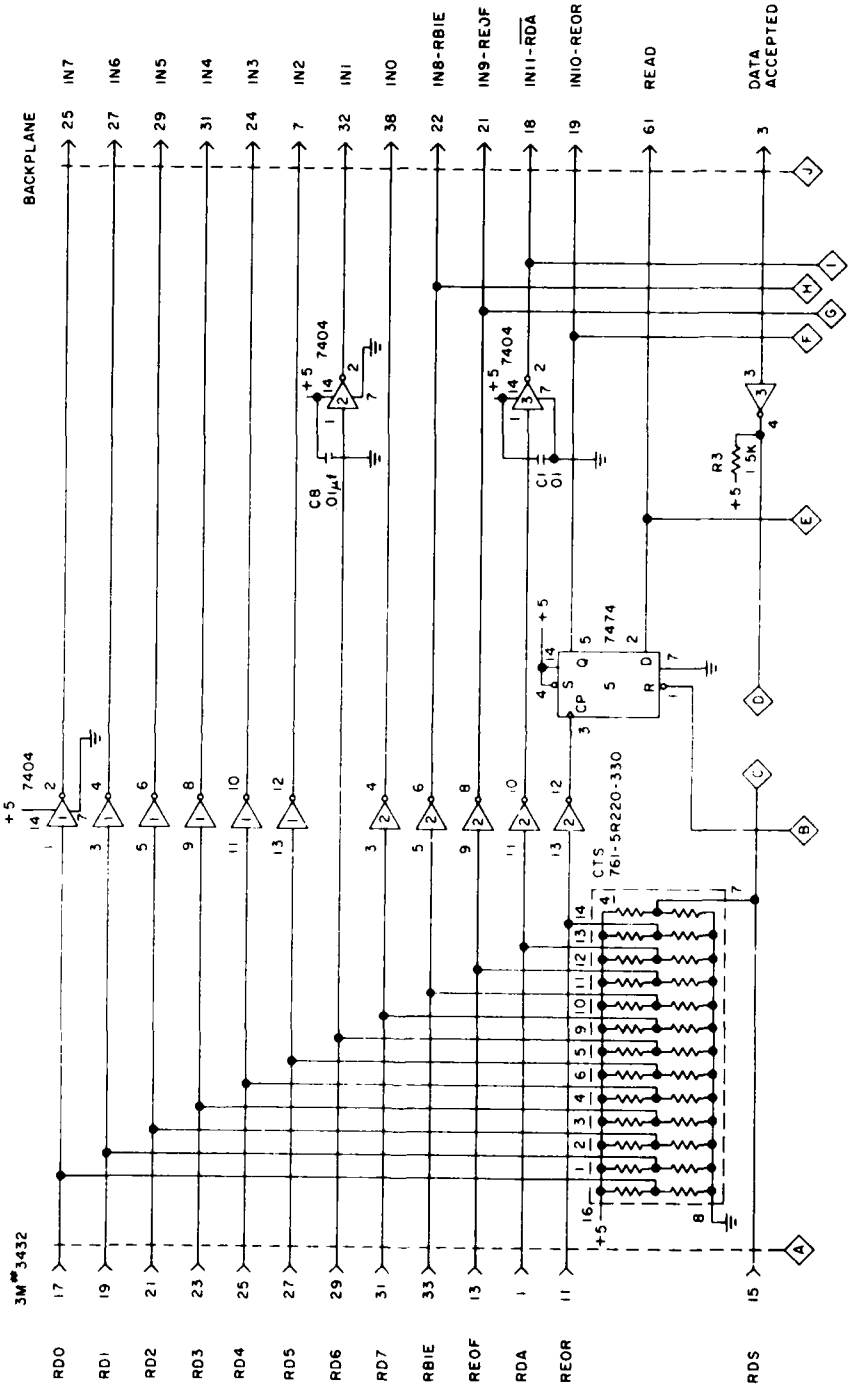
L-3. Tape Recorder Interface Block Diagram

L.3.2 READ INTERFACE CIRCUIT BOARD

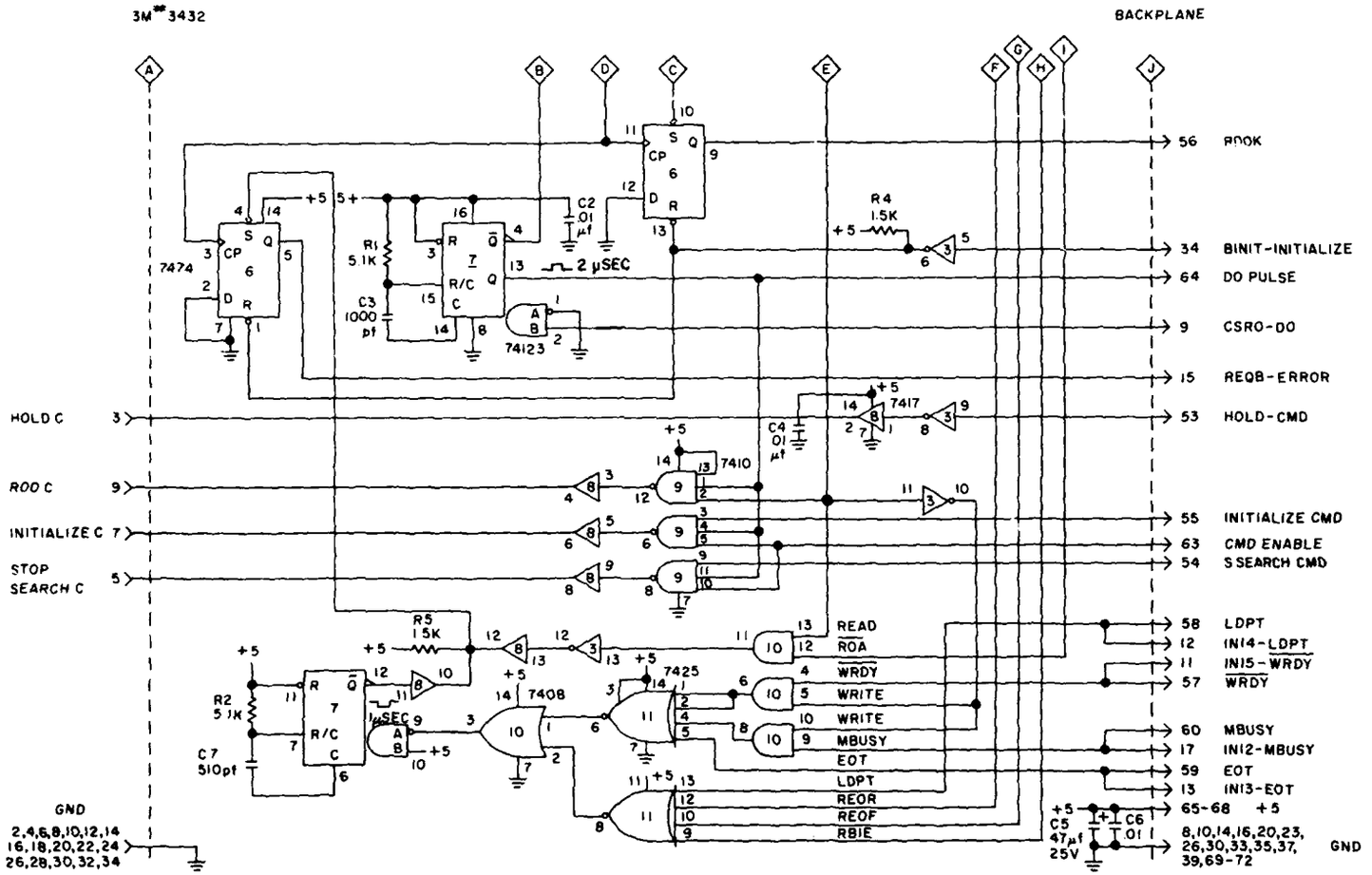
L.3.2.1 Circuit Description

Figure L-4 contains the schematic diagram of the read interface circuit board.

Inverters U1 and U2 together with resistor network U4 buffer the data and signal lines coming from the recorder. Half of each of two dual D flipflops are used to convert the REOR (Read End of Record) and RDS (Read Data Strobe) status lines (which arrive as pulses) to levels for reading by the DRV-11. The REOR flipflop is cleared by the command execute pulse (which is generated by half of a dual *monostable multivibrator* U7). The RDS flipflop, on the other hand, is cleared by either the INITIALIZE or DATA ACCEPTED signals from the computer. The command execute pulse also feeds triple-input NAND gates (U9) to generate three of the pulsed recorder commands. These are buffered by open collector buffers U8.



L-4. Tape Recorder Read Interface Schematic



L-4. Tape Recorder Read Interface Schematic (Cont.)

The majority of the remaining logic on the board is associated with error signal processing. U10 and U11 combine the recorder status signals to form the input to a monostable multivibrator (U7). This in turn puts out a 1 usec pulse to set the error flipflop U6. The pulse is ORed with the signal from pin 11 of U10. This signal is true whenever the recorder is in the read mode and read data is not available. The effect of this ORing is to hold the error flipflop high as long as the condition persists. The flipflop is normally reset by either the INITIALIZE or DATA ACCEPTED signal from the DRV-11. Since the DATA ACCEPTED signal occurs each time the computer reads the DRV-11 input data word, reading the status bits in this word normally clears the error flag. ORing the read data not available signal into the flipflop insures that it is not reset as long as the condition holds.

L.3.2.2 Circuit Board Description

All components for the interface are mounted on a single 4.5 x 6.5 in. (11.4 x 16.5 cm) double-sided printed circuit board. Power connections to the board are made through the board's edge connector as are connections between this and the write interface card. Connections between the board and J12 on the interface chassis rear panel are also made through the edge connector. Connections between the card and the recorder read connector are made through a ribbon cable socket mounted on the card edge. Figure L-5 is a photograph of the interface card with parts identified. Table L-3 gives the board parts list keyed to the board photograph.

The card edge connector is used for connecting power and ground to the board. It also connects signals going between the card and the computer parallel interface. Also run through the edge connector are signals that flow between the two interface cards (read and write). Table L-4 gives the signal assignments for this edge connector together with their sources/destinations on the card.

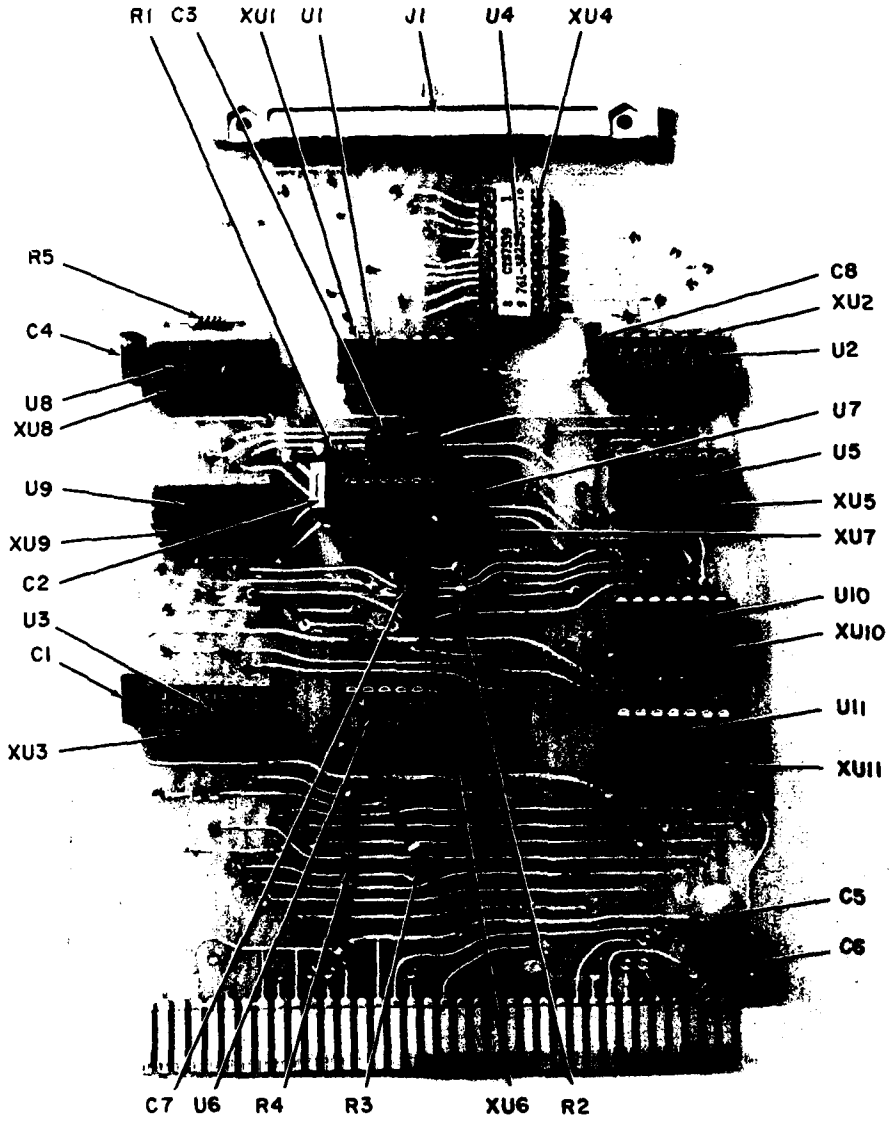
Connections between the card and the Kennedy recorder are made via J1 on the card. Spectra-Strip #455-248-40 40-conductor twisted pair ribbon cable is used for the connection. Both ends of the cable are terminated with 3M #3425-3000 plugs. A printed circuit adapter is mounted on the chassis rear panel connector (J12) to convert the ribbon cable to the 37-pin connector used by the recorder. Table L-5 lists the pin identification for the signals appearing on J1. It also identifies their origin on the board and where they appear on J12.

L.3.3 WRITE INTERFACE CIRCUIT BOARD

L.3.3.1 Circuit Description

Figure L-6 contains the schematic diagram of the write interface circuit board.

This card contains the differential line drivers for interfacing with the modified tape recorder. It also contains pull-up resistors and inverting buffers for those status signals that appear on the write connector. These status signals are routed to the read interface.



L-5. Tape Recorder Read Interface Component Locations

L.3.3.2 Circuit Board Description

All components for the interface are mounted on a single 4.5 x 6.5 in. (11.4 x 16.5 cm) double-sided printed circuit board. Power connections to the board are made through the board's edge connector as are connections between this and the read interface card. Connections between the board and J13 on the interface chassis rear

Table L-3 Tape Recorder Read Interface Parts List

Part	Noun	Mfgr Part No.	Manufacturer
XU1,2,3,5, 6,8-11	Low profile DIP IC socket, 14-pin	514-AG10D	Augat
XU4,XU7	Low profile DIP IC socket, 16-pin	516-AG10D	Augat
R1,R2	Resistor, 5.1K Ω, 1/2 W, 2%, metal film	C5	Corning
R3-R5	Resistor, 1.5K Ω, 1/2 W, 2%, metal film	C5	Corning
C1,2,4,6,8	Capacitor, 0.01 μF, 200 V	CKR06	AVX
C3	Capacitor, 1000 pF, 100 V, 2%, mica	DL-15-102G	Arco
C5	Capacitor, 47 μF, 35 V, tantalum	199D476X0035A2	Sprague
C7	Capacitor, 510 pF, 500 V, 5%, mica	DL-15-511	Arco
U1,2,3	Hex inverter, TTL	7404	Texas Instrument
U4	Resistor network	761-5R220-330	CTS
U5,6	Dual D-type flipflop, TTL	7474	Texas Instrument
U7	Dual Monostable multivibrator, TTL	74123	Texas Instrument
U8	Hex open collector buffer, TTL	7417	Texas Instrument
U9	Triple 3-input NAND gate, TTL	7410	Texas Instrument
U10	Quad 2-input AND gate, TTL	7408	Texas Instrument
U11	Dual 4-input NOR gate, TTL	7425	Texas Instrument
J1	Socket, 40-pin ribbon cable	3432-1002	3M

Table L-4 Tape Recorder Read Interface
Edge Connector Pin Identification

Interface			Destination	
Pin	Signal	Direct	Conn/Pin	Signal
3	Data accepted pulse	In *	J9/3 **	Data accepted pulse
7	Read data bit 2	Out	J9/7	Input bit 2
8	Ground	-	J9/8	Ground
9	Gen command pulse	In	J9/9	CSR Ø
1Ø	Ground	-	J9/1Ø	Ground
11	Not write ready	Out	J9/11	Input bit 15
12	Load point	Out	J9/12	Input bit 14
13	End of tape	Out	J9/13	Input bit 13
14	Ground	-	J9/14	Ground
15	Error	Out	J9/15	Req B input
16	Ground	-	J9/16	Ground
17	Memory busy	Out	J9/17	Input bit 12
18	Read data not avail	Out	J9/18	Input bit 11
19	End of record read	Out	J9/19	Input bit 1Ø
2Ø	Ground	-	J9/2Ø	Ground
21	End of file read	Out	J9/21	Input bit 9
22	Read block error	Out	J9/22	Input bit 8
23	Ground	-	J9/23	Ground
24	Read data bit 4	Out	J9/24	Input bit 3
25	Read data bit Ø	Out	J9/25	Input bit 7
26	Ground	-	J9/26	Ground
27	Read data bit 1	Out	J9/27	Input bit 6
29	Read data bit 2	Out	J9/29	Input bit 5
3Ø	Ground	-	J9/3Ø	Ground
31	Read data bit 3	Out	J9/31	Input bit 4
32	Read data bit 6	Out	J9/32	Input bit 1
33	Ground	-	J9/33	Ground
34	Initialize	In	J9/34	Initialize
35	Ground	-	J9/35	Ground
37	Ground	-	J9/37	Ground
38	Read data bit 7	Out	J9/38	Input bit Ø
39	Ground	-	J9/39	Ground
53	HOLD command	In	WI/53 ***	HOLD command
54	STOP SEARCH command	In	WI/54	STOP SEARCH comm
55	INITIALIZE command	In	WI/55	INITIALIZE comm
57	Not write ready	In	WI/57	Not write rdy in
58	Load point	In	WI/58	Load point
59	End of tape read	In	WI/59	EOT read
6Ø	Memory busy	In	WI/6Ø	Memory busy
63	Command enable	In	WI/63	Command enable
64	Command pulse	Out	WI/64	Command pulse
65/68		+ 5 Vdc	Power	
69/72		Ground		

* "In" refers to signals accepted by on/board circuitry;
"Out" refers to signals generated by card.

** "J9" refers to interface chassis back panel connector J9.

*** "WI" refers to tape write interface edge connector.

Notes:
-- All signals TTL level.
-- Edge connector pins not listed are not used.

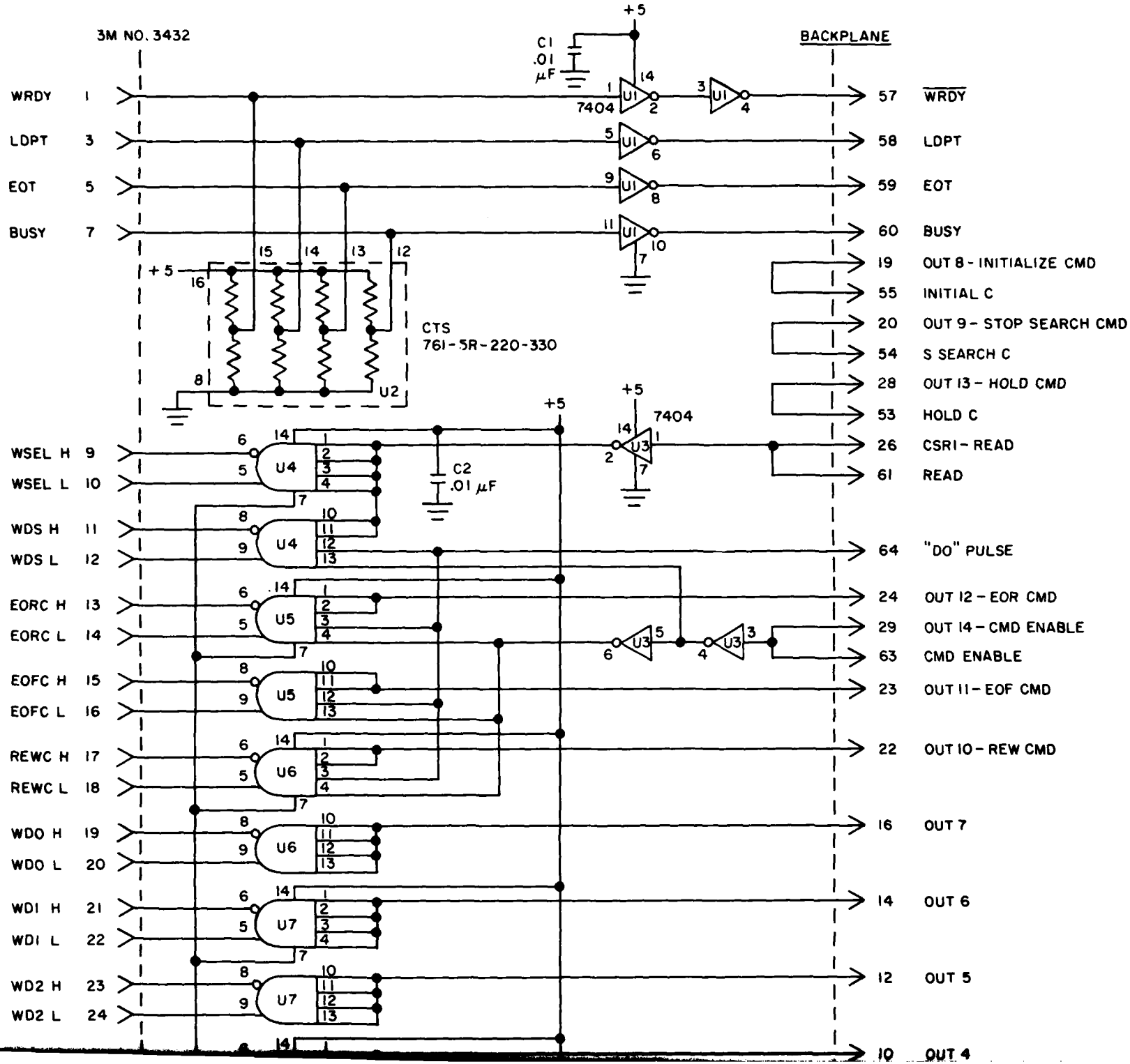
Table L-5 Tape Recorder Read Interface
Output Connector Pin Identification

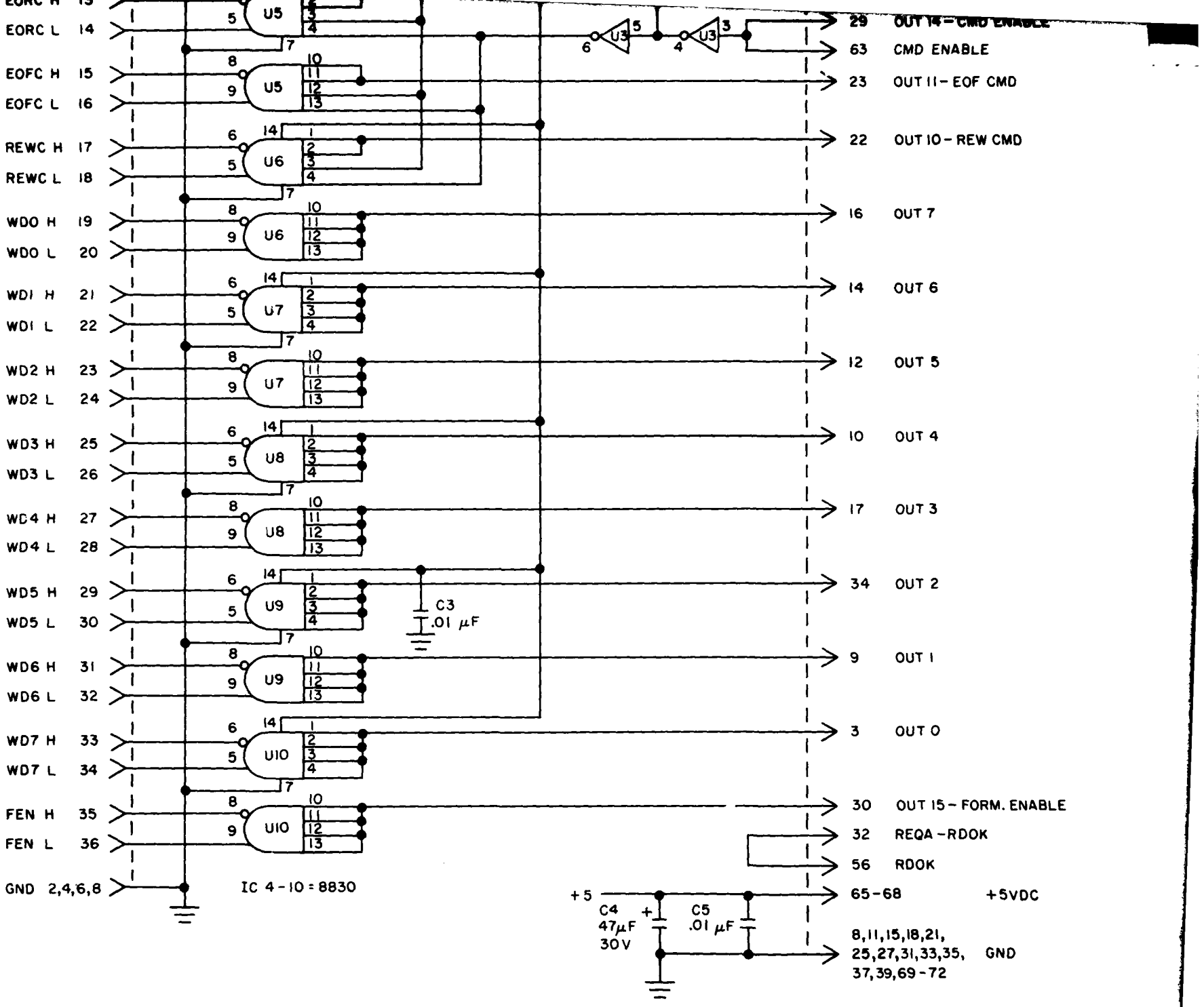
Pin	Signal	Direct	J12 Pin
1	Read data available	In *	1
2	Ground	-	20
3	HOLD command	Out	2
4	Ground	-	21
5	STOP SEARCH command	Out	3
6	Ground	-	22
7	INTIALIZE command	Out	4
8	Ground	-	23
9	READ ONE CHARACTER command	Out	6
10	Ground	-	24
11	End of record	In	7
12	Ground	-	25
13	End of file	In	8
14	Ground	-	26
15	Read data strobe	In	9
16	Ground	-	27
17	Read data bit 0	In	10
18	Ground	-	28
19	Read data bit 1	In	11
20	Ground	-	29
21	Read data bit 2	In	12
22	Ground	-	30
23	Read data bit 3	In	13
24	Ground	-	31
25	Read data bit 4	In	14
26	Ground	-	32
27	Read data bit 5	In	15
28	Ground	-	33
29	Read data bit 6	In	16
30	Ground	-	34
31	Read data bit 7	In	17
32	Ground	-	35
33	Read data block error	In	18
34	Ground	-	36

* "In" refers to signals accepted by onboard circuitry;
"Out" refers to signals generated by card.

Notes:

-- All signals TTL level.
-- Connector pins not listed are not used.
-- Bit numbers refer to recorder rather than user bit identifications.


3M NO. 3432
BACKPLANE
+5
C1
.01 μF
7404
WRDY 1
LDPT 3
EOT 5
BUSY 7
57 WRDY
58 LDPT
59 EOT
60 BUSY
CTS
761-5R-220-330
U2
19 OUT 8 - INITIALIZE CMD
55 INITIAL C
20 OUT 9 - STOP SEARCH CMD
54 S SEARCH C
28 OUT 13 - HOLD CMD
53 HOLD C
26 CSR1 - READ
61 READ
WSEL H 9
WSEL L 10
WDS H 11
WDS L 12
C2
.01 μF
64 "DO" PULSE
EORC H 13
EORC L 14
24 OUT 12 - EOR CMD
29 OUT 14 - CMD ENABLE
63 CMD ENABLE
EOFC H 15
EOFC L 16
23 OUT 11 - EOF CMD
REWC H 17
REWC L 18
22 OUT 10 - REW CMD
WDO H 19
WDO L 20
16 OUT 7
WD1 H 21
WD1 L 22
14 OUT 6
WD2 H 23
WD2 L 24
12 OUT 5
10 OUT 4



L-6. Tape Recorder Write Interface Schematic

panel are also made through the edge connector. Connections between the card and the recorder write interface card connector are made through a ribbon cable socket mounted on the card edge. Figure L-7 is a photograph of the interface card with parts identified. Table L-6 gives the board parts list and is keyed to the board photograph.

The card edge connector is used for connecting power and ground to the board as well as for connecting signals between the card and the computer parallel interface. Also run through the edge connector are signals that flow between the two interface cards (read and write). Table L-7 gives the signal assignments for this edge connector together with their sources/destinations on the card.

Connections between the card and the recorder are made via J1 on the card. Spectra Strip #455-248-40 40-conductor twisted pair ribbon cable is used for the connection. Both ends of the cable are terminated with 3M #3425-3000 plugs. A printed circuit adapter is mounted on the chassis rear panel connector (J13) to convert the ribbon cable to the 37-pin connector used by the recorder. Table L-8 lists the pin identification for the signals appearing on J1. It also identifies their origin on the board and where they appear on J13.

L.4 TAPE RECORDER INTERFACE SOFTWARE CONSIDERATIONS

L.4.1 INTERFACE REGISTER CONTENTS

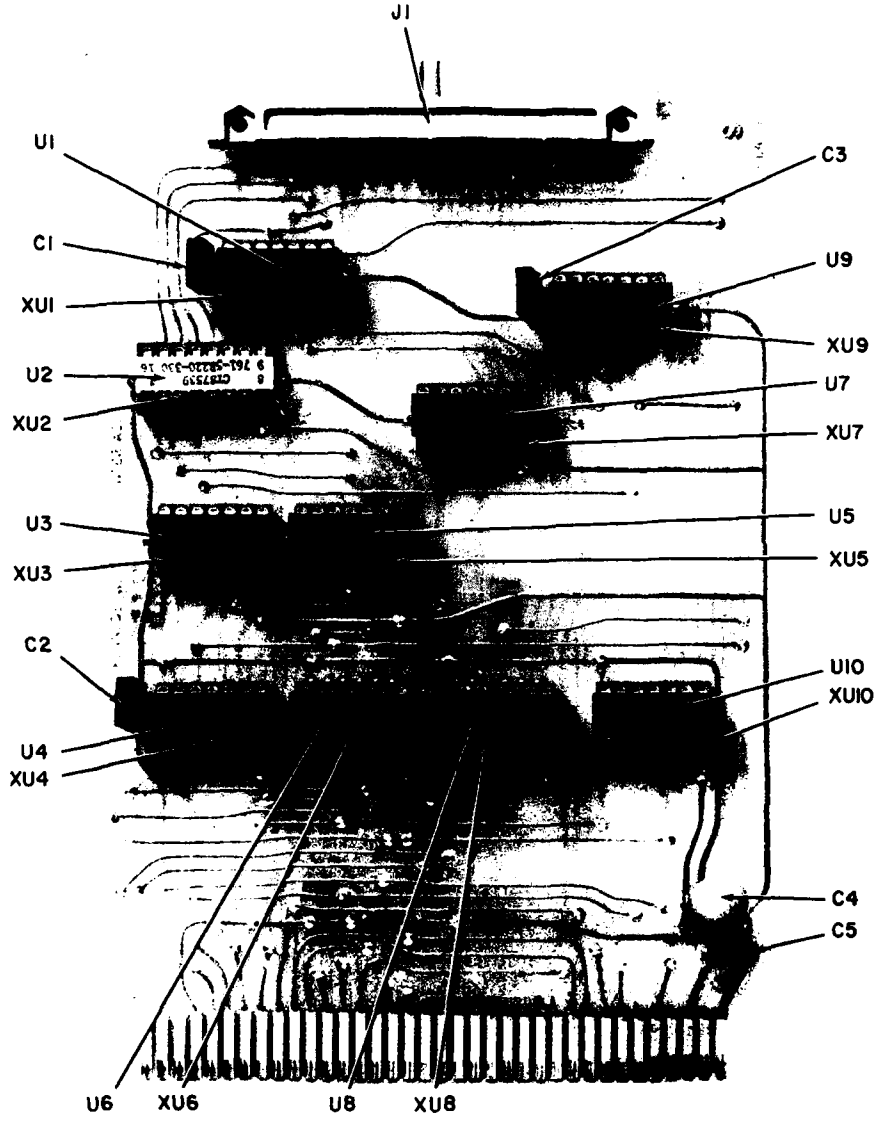
The SDAS system tape recorder interfaces described above are connected to a single DRV-11 parallel line interface module in the controller computer. System software has access to the three registers (control and status, input, and output) on the module. Tables L-9 through L-11 give bit identification for these registers; register addresses are as shown in Appendix I, Figure I-3. (Bit 0 is LSB, bit 15 is MSB.)

L.4.2 TAPE RECORDER INTERFACE CHECKOUT SOFTWARE

Listed in Table L-12 is a short tape recorder checkout program (NEWKEN). The program was written in DEC's assembly language (RT-11 MACRO, version VM02-12) running under DEC's RT-11 operating system (RT-11FB, version V02C-02B). The program records and plays back a known pattern and displays the results of the test.

Prior to running the program, a tape must be loaded onto the tape recorder and the recorder put ON LINE. After being loaded and executed, NEWKEN rewinds the tape and reports LOAD POINT when the load point is reached. It then records 100 records of data on the tape. An ascending count is used as the bit pattern, with the count reset when it reaches 10,240. The count is repeated 100 times to get 1000 records of 1024 characters each.

When the recording is completed, the tape is rewound with LOAD POINT reported to signal completion. The program then reports READ TEST and proceeds to read back the tape, comparing the read count pattern with an internally generated one. If a discrepancy occurs,



L-7. Tape Recorder Write Interface Component Locations

Table L-6 Tape Recorder Write *Interface* Parts List

Part	Noun	Mfgr Part No.	Manufacturer
XU1, XU3-XU10	Low profile DIP IC socket, 14-pin	514-AG10D	Augat
XU2	Low profile DIP IC socket, 16-pin	516-AG10D	Augat
C1-C3,C5	Capacitor, 0.01 μF, 200 V	CKR06	AVX
C4	Capacitor, 47 μF, 35 V, tantalum	199D476X0035A2	Sprague
U1, U3	Hex inverter, TTL	7404	TI
U2	Resistor network	761-5R220-330	CTS
U4-U10	Dual differential line driver	DS8830N	Nat'l Semic.
J1	Socket, 40-pin ribbon cable	3432-1002	3M

Table L-7 Tape Recorder Write Interface
Edge Connector Pin Identification

Interface			Destination	
Pin	Signal	Direct	Conn/Pin	Signal
3	Write data bit 7	In *	J8/3 **	Output bit Ø
8	Ground	-	J8/8	Ground
9	Write data bit 6	In	J8/9	Output bit 1
1Ø	Write data bit 3	In	J8/1Ø	Output bit 4
11	Ground	-	J8/11	Ground
12	Write data bit 2	In	J8/12	Output bit 5
14	Write data bit 1	In	J8/14	Output bit 6
15	Ground	-	J8/15	Ground
16	Write data bit Ø	In	J8/16	Output bit 7
17	Write data bit 4	In	J8/17	Output bit 3
18	Ground	-	J8/18	Ground
19	INITIALIZE command	In	J8/19	Output bit 8
2Ø	STOP SEARCH command	In	J8/2Ø	Output bit 9
21	Ground	-	J8/21	Ground
22	REWIND command	In	J8/22	Output bit 1Ø
23	WRITE END OF FILE comm	In	J8/23	Output bit 11
24	WRITE END OF RECORD comm	In	J8/24	Output bit 12
25	Ground	-	J8/25	Ground
26	READ command	In	J8/26	CSR 1
27	Ground	-	J8/27	Ground
28	HOLD command	In	J8/28	Output bit 13
29	Command enable	In	J8/29	Output bit 14
3Ø	FORMATTER ENABLE command	In	J8/3Ø	Output bit 15
31	Ground	-	J8/31	Ground
32	READ DATA GOOD	Out	J8/32	REQ A
33	Ground	-	J8/33	Ground
34	Write data bit 5	In	J8/34	Output bit 2
35	Ground	-	J8/35	Ground
37	Ground	-	J8/37	Ground
53	HOLD command	In	RI/53 ***	HOLD command
54	STOP SEARCH command	Out	RI/54	STOP SEARCH comm
55	INITIALIZE command	Out	RI/55	INITIALIZE comm
57	Not write ready	Out	RI/57	Not write ready
58	Load point	Out	RI/58	Load point
59	End of tape read	Out	RI/59	EOT read
6Ø	Memory busy	Out	RI/6Ø	Memory busy
63	Command enable	Out	RI/63	Command enable
64	Command pulse	In	RI/64	Command pulse
65-68	+ 5 Vdc	Power		
69-72	Ground	-		

* "In" refers to sig[illegible]ccepted by onboard circuitry;
"Out" refers to signa[illegible]nerated by card.
** "J8" refers to interface chassis rear panel connector J8.
*** "RI" refers to tape recorder read interface edge connector.

Notes:
-- All signals TTL level.
-- Edge connector pins not listed are not used.

Table L-8 Tape Recorder Write Interface
Output Connector Pin Identification

Pin	Interface Signal	Direct	J13 Pin
1	Write ready	In *	1
2	Ground	-	20
3	Load point	In	2
4	Ground	-	21
5	End of tape	In	3
6	Ground	-	22
7	Memory busy	In	4
8	Ground	-	23
9	WRITE - H **	Out	24
10	WRITE - L	Out	5
11	WRITE DATA cmd - H	Out	25
12	WRITE DATA cmd - L	Out	6
13	END OF RECORD cmd - H	Out	26
14	END OF RECORD cmd - L	Out	7
15	END OF FILE cmd - H	Out	27
16	END OF FILE cmd - L	Out	8
17	REWIND Command - H	Out	28
18	REWIND Command - L	Out	9
19	Write data bit 0 - H	Out	29
20	Write data bit 0 - L	Out	10
21	Write data bit 1 - H	Out	30
22	Write data bit 1 - L	Out	11
23	Write data bit 2 - H	Out	31
24	Write data bit 2 - L	Out	12
25	Write data bit 3 - H	Out	32
26	Write data bit 3 - L	Out	13
27	Write data bit 4 - H	Out	33
28	Write data bit 4 - L	Out	14
29	Write data bit 5 - H	Out	34
30	Write data bit 5 - L	Out	15
31	Write data bit 6 - H	Out	35
32	Write data bit 6 - L	Out	16
33	Write data bit 7 - H	Out	36
34	Write data bit 7 - L	Out	17
35	FORMATTER ENABLE - H	Out	37
36	FORMATTER ENABLE - L	Out	18

* "In" refers to signals accepted by onboard circuitry;
"Out" refers to signals generated by card.

** "H" and "L" refer to inverting and noninverting differential line driver outputs, respectively.

Notes:

-- All signals TTL level.
-- Connector pins not listed are not used.
-- Bit numbers refer to recorder rather than user bit identifications.

the program halts and displays 001444. To check the expected versus read character, typing R4/ on the console will result in the display of the contents of the parallel line card input buffer. The read data will be in the lower order bite. Typing R5/ displays the expected data value, again in the lower order byte.

If no errors are encountered while reading the data, the program will display END OF FILE and THAT'S ALL FOLKS followed by 001566, signifying program completion. To reenter the operating system, the user types P<cr>. To restart the program at the beginning, the user types R7/. When the computer responds with 001566, the user types 1052<cr>P and the program restarts. (To restart the program at the tape reading section, the user types 1000<cr>P.)

To change the number of records recorded/read, the contents of memory location 001156_8 must be changed. The program initially loads 100_{10} (144_8) as the number of 1024_{10}-character blocks recorded. To record/read a full tape, 1274 is loaded into location 001156_8.

Table L-9 Tape Recorder Interface
Control and Status Register Bit Identification

Bit	DEC Bit Name	Type	Functional Description
0	CSR0	R/W *	INITIATE COMMAND PULSE. Two sec pulse generated on read interface card on low to high transition of line. Pulse used to generate recorder commands and to reset END OF RECORD READ flipflop.
1	CSR1	R/W	READ/WRITE. Tape read when loaded high; recorded when cleared.
5	INT ENB B	R/W	ERROR INTERRUPT ENABLE. Computer interrupted when error occurs when bit set high. Interrupt cleared by reading input buffer or by issuing reset command.
6	INT ENB A	R/W	Not used.
7	REQ A	R	Not used.
15	REQ B	R	INTERRUPT B FLAG. Shows status of ERROR signal connected to REQ B input. ERROR cleared when input buffer read or when RESET command issued.

* "R" implies that bit status can be read under program control;
"W" implies that bit can be loaded by the program.

Table L-10 Tape Recorder Interface
Output Register Bit Identification

Bit	Functional Description
0	Write data bit 0.
1	Write data bit 1.
2	Write data bit 2.
3	Write data bit 3.
4	Write data bit 4.
5	Write data bit 5.
6	Write data bit 6.
7	Write data bit 7.
8	INITIALIZE command*
9	STOP SEARCH command*
10	REWIND command*
11	WRITE END OF FILE command*
12	WRITE END OF RECORD command*
13	HOLD command
14	COMMAND ENABLE. Must be set high to enable issuing any commands to recorder.
15	FORMATTER ENABLE. Must be set high to read, write, or command tape recorder.

* Require low-to-high transistion of status register bit 0 for commands to be performed.

Note:

-- Data bit order given is that seen by the system computer. The bit ordering recorded on tape is opposite to that given (i.e., write data bit 0 is written as bit 7 on the tape).

Table L-11 Tape Recorder Interface
Input Register Bit Identification

Bit	Contents
0	Read data bit 0
1	Read data bit 1
2	Read data bit 2
3	Read data bit 3
4	Read data bit 4
5	Read data bit 5
6	Read data bit 6
7	Read data bit 7
8	Read data block error
9	End of file read
10	End of record read
11	Read data not available
12	Memory busy (valid only for write mode)
13	End of tape
14	Tape at load point
15	Write not ready

Notes:

-- All signals use positive logic (High = 1).
-- Bit order given is that seen by the system computer. The bit ordering recorded on tape is opposite to that given (i.e., read data bit 0 is read as bit 7 on the tape).

Table L-12 Tape Recorder Interface
Checkout Program Listing

```
        .TITLE NEWKEN
        .SBTTL KENNEDY TEST  20-SEP-77
        .MCALL ..V2..,.REGDEF,.PRINT,.EXIT
        ..V2..
        .REGDEF
        CSR=167760
        OUTBUF=CSR+2
        INBUF=CSR+4
        MTPS  200                ;START HERE JUST TO REWIND & READ
        MOV  1,RFLAG             ;SET READ FLAG
        MOV  2,CSR
        MOVB  301,OUTBUF+1       ;LOAD INIT COMMAND
        INC CSR                  ;DO
        CLR CSR
        MOV  3,R4
        CLR R5
        JSR PC,REWIND
        BR READ2
START:  MTPS  200
        CLR RFLAG                ;SET WRITE FLAG
        CLR CSR
        MOVB  301,OUTBUF+1       ;INIT COMMAND
        INC CSR                  ;DO
        CLR CSR
        CLR R5                   ;INITIALIZE OUTPUT BIT PATTERN
        CLR R2
        MOV  1,R4                ;WRITE MODE & DO
        JSR PC,REWIND            ;REWIND
        MOV  1000.,R3
READY:  MOV INBUF,R1             ;GET STATUS
        BIT  100000,R1           ;WRITE READY?
        BEQ GO                   ;YES - BRANCH
        SOB R3,READY             ;NO - WAIT
        JSR PC,ERROR1            ;REPORT ERROR
        HALT
        BR START
GO:     MOVB  200,OUTBUF+1       ;LEAVE FEN UP
        MOV  100.,R3             ;COUNTER FOR FOLLOWING LOOP - OUTPUTS
                                 ;  1000 RECORDS.  TO FILL TAPE CHANGE
                                 ;  TO 1274 OCTAL.
;       CHARACTER OUTPUT EVERY 64US   (23 NOV 76)
;       REMOVE COMMENT CHAR. TO HALT IF MEMORY BUSY SIGNAL COMES UP
;                                OUTPUT RATE 83US WITH THIS TEST
1$:     CLR CSR                  ;CLEAR DO BIT
2$:     MOV INBUF,R1             ;GET STATUS
        BIT  130000,R1           ;WRITE NOT READY,EOT,OR MEM BSY?
        BEQ 3$                   ;NO - BRANCH
        BIT  10000,R1            ;MEMORY BUSY?
        BNE 2$                   ;BRANCH IF SO
        JSR PC,ERROR1            ;REPORT ERROR
        BIT  20000,R1            ;EOT?
        BNE READ                 ;YES - BRANCH
```

Table L-12 Tape Recorder Interface Checkout
Program Listing (contd)

```
        HALT                    ;NO - QUIT
        BR 2$                   ;TRY AGAIN IF WRITE NOT READY
3$:     MOVB R5,OUTBUF          ;LOAD OUTPUT BYTE
        INC CSR                 ;DO
        INC R5                  ;INCREMENT OUTPUT BIT PATTERN
        CMP R5, 10240.          ;DONE 10 RECORDS?
        BLT 1$                  ;NO - BRANCH
        CLR R5                  ;YES - CLEAR BIT PATTERN
        SOB R3,1$               ;LOOP TILL RECORD COUNTER EXHAUSTED
4$:     BIT  10000,INBUF        ;MEMORY BUSY?
        BNE 4$                  ;WAIT IF SO
        CLR CSR                 ;CLEAR DO BIT
        MOVB  310,OUTBUF+1      ;LOAD EOF COMMAND
        INC CSR                 ;DO
        TST CSR                 ;ERROR?
        BPL READ                ;NO - BRANCH
        JSR PC,ERROR            ;YES - REPORT IT & STOP
        HALT
        .ENABL LSB
READ:   CLR CSR                 ;CLEAR DO
        MOV  1,RFLAG            ;SET READ FLAG
        MOV  177777,R5
        SOB R5,.                ;DELAY BEFORE ISSUING NEXT COMMAND
        MOV  3,R4               ;READ MODE & DO
        JSR PC,REWIND           ;REWIND
READ2:  MOV  RTEST,R0
        JSR PC,PRINT
        MOVB  200,OUTBUF+1      ;ONLY LEAVE FEN UP
        BIT  4000,INBUF         ;READ DATA AVAILABLE?
        BNE .-6                 ;NO - WAIT
        BR 4$                   ;YES - BRANCH (1ST BYTE IS IN OUTBUF)
1$:     INC R5                  ;BUMP PATTERN FOR EXPECTED BYTE
2$:     CLR @ NTRY              ;CLEAR RDA RETRY COUNTER
        MOV  2,CSR              ;SET READ MODE & CLEAR DO
        INC CSR                 ;READ OUT ONE CHARACTER
        TST CSR                 ;ERROR?
        BMI 10$                 ;YES - BRANCH
3$:     TSTB CSR                ;WAIT FOR DONE
        BPL 3$
4$:     MOV INBUF,R4            ;GET STATUS & DATA
CHECK:  INC @ LENGTH            ;  CHARACTERS IN RECORD
        CMPB R5,R4              ;CHAR READ MATCH EXPECTED VALUE?
        BEQ 1$                  ;YES - LOOP
        HALT                    ;NO - LOW BYTE OF R4 CONTAINS ACTUAL
                                ;     LOW BYTE OF R5 CONTAINS EXPECTED
        JMP @ 1$
10$:    MOV INBUF,R4            ;GET STATUS & READ DATA
        BIT  1000,R4            ;EOF?
        BNE 13$                 ;YES - BRANCH
        BIT  2000,R4            ;EOR?
        BNE 20$                 ;YES - BRANCH
        BIT  4000,R4            ;READ DATA NOT AVAILABLE?
        BEQ TENA                ;NO - BRANCH
        INC @ NTRY              ;RETRY COUNTER + 1
        CMP @ NTRY, 2000.       ;RETRIED 2000 TIMES? (APPRX 100MS)
```

Table L-12 Tape Recorder Interface Checkout
Program Listing (contd)

```
        BLT 10$                 ;NO - TRY AGAIN
        BR 11$
TENA:   TST @ NTRY              ;WAITING FOR READ DATA AVAILABLE?
        BNE 2$                  ;YES - BRANCH IT'S AVALIABLE
11$:    JSR PC,ERROR            ;REPORT ERROR
        BIT  67400,R4           ;ANY DRINBUF BITS UP? (READ ERROR ONLY)
        BNE 12$                 ;YES - BRANCH
        HALT                    ;NO - STOP
        BR 2$                   ;CONTINUE LOOP
12$:    HALT
        BR 2$                   ;CONTINUE
13$:    MOV  REOF,R0
        JSR PC,PRINT
        MOV  DONE,R0            ;GOT EOF - FINISHED
        JSR PC,PRINT
        HALT
        .EXIT                   ;BACK TO RT MONITOR
20$:    INC @ NRECS             ;END OF RECORD
        CMP @ LENGTH, 1024.     ;CORRECT LENGTH?
        BEQ 22$                 ;YES - BRANCH
        MOV @ NRECS,R1          ;NO - GET RECORD COUNTER
        JSR R0,@ OTOAD          ;CONVERT TO DECIMAL OCTAL
        ONRECS
        MOV @ LENGTH,R1         ;LENGTH
        JSR R0,@ OTOAD          ;TO OCTAL
        OLEN
        MOV  BADLEN,R0
        JSR PC,PRINT            ;OUTPUT MESSAGE
22$:    CLR R5                  ;CLEAR BIT PATTERN
        CLR @ LENGTH
        BR CHECK                ;GO CHECK CHARACTER READ
        .DSABL LSB
REWIND: MOVB  304,OUTBUF+1      ;LOAD REWIND COMMAND
        MOV R4,CSR              ;SELECTED MODE & DO BIT
1$:     MOV INBUF,R1            ;GET STATUS
        BIT  40000,R1           ;LOAD POINT?
        BEQ 1$                  ;NO - WAIT FOR IT
        JSR PC,ERROR1           ;REPORT LOAD POINT
        CLR @ NTRY              ;CLEAR RETRY COUNTER
        CLR @ NRECS             ;  & RECORD COUNTER
        CLR @ LENGTH            ;  & CHARACTER COUNTER
        RTS PC
ERROR:  MOV R4,R1               ;STATUS TO R1
ERROR1: BIT  110000,R1          ;MEMORY BUSY OR WRITE NOT READY?
        BEQ ERROR2              ;NO - BRANCH
        TST RFLAG               ;YES - ARE WE READING?
        BEQ ERROR2              ;NO - BRANCH
        BIC  110000,R1          ;YES - DON'T REPORT WRITE ERRORS
ERROR2: CLR R2
1$:     ROL R1                  ;ROTATE TILL A BIT IS UP
        BCS 2$                  ;BRANCH WHEN UP
        INC R2
        CMP R2, 8.              ;DONT'T OVER DO IT
        BLO 1$                  ;DON'T BRANCH IF NO ERROR BITS ARE UP
2$:     ASL R2                  ;OFFSET INTO ERROR MESSAGE TABLE
```

Table L-12 Tape Recorder Interface Checkout
Program Listing (contd)

```
        MOV ERRORS(R2),RØ
        JSR PC,PRINT            ;PRINT ERROR MESSAGE
        RTS PC                  ;RETURN
PRINT:  TSTB @ 177564
        BPL PRINT
        MOVB (RØ)+,@ 177566
        BNE PRINT
        RTS PC
RFLAG:  .WORD Ø
NRECS:  .WORD Ø
LENGTH: .WORD Ø
NTRY:   .WORD Ø
        .NLIST BEX
ERRORS: .WORD NOTRDY,LOADPT,EOT,MEMBSY,NORDA,REOR,REOF,RBIE,NOERR
NOTRDY: .ASCIZ /WRITE NOT READY/<15><12>
LOADPT: .ASCIZ /LOAD POINT/<15><12>
EOT:    .ASCIZ /END OF TAPE/<15><12>
MEMBSY: .ASCIZ /MEMORY BUSY/<15><12>
NORDA:  .ASCIZ /READ DATA NOT AVAILABLE/<15><12>
REOR:   .ASCIZ /END OF RECORD/<15><12>
REOF:   .ASCIZ /END OF FILE/<15><12>
RBIE:   .ASCIZ /READ BLOCK IN ERROR/<15><12>
NOERR:  .ASCIZ /ERROR - NO DRINBUF BIT SET/<15><12>
DONE:   .ASCIZ /THAT'S ALL FOLKS/<15><12>
BADLEN: .ASCII /RECORD/
ONRECS: .BLKB 6
        .ASCII /  -   LENGTH/
OLEN:   .BLKB 6
        .BYTE 15,12,Ø
RTEST:  .ASCIZ /READ TEST/<15><12>
        .LIST BEX
        .NLIST
        .EVEN
;SUBROUTINE OTOAD
;CONVERTS OCTAL WORD IN R1 TO DECIMAL ASCII.
;ENTER WITH C BIT CLEAR TO TREAT AS SIGNED NUMBER.
;THE RESULTING STRING IS 6 BYTES LONG INCLUDING SIGN.
;LEADING ZEROES ARE SUPPRESSED.
;SUBROUTINE CALL:        JSR RØ,@ OTOAD
 ;                      .WORD STRING ;ADDR OF RESULTING ASCII STRING
OTOAD:  MOV R5,-(SP)            ;SAVE THE REGISTERS
        MOV R4,-(SP)
        MOV R3,-(SP)
        MOV R2,-(SP)
        MOV R1,-(SP)
        MOV (RØ)+,R5            ;WHERE TO PUT THE RESULTING STRING
        MOV RØ,-(SP)            ;SUBR RETURN ADDR
OTOAD1: MOVB  ' ,(R5)+          ;ASSUME POSITIVE
        BCS 1$                  ;BRANCH IF HE DOEN'T WANT SIGN
        TST R1
        BPL 1$
        MOVB  '-,-1(R5)         ;IT'S NEGATIVE - MOVE MINUS SIGN
        NEG R1                  ;MAKE IT POSITIVE FOR CONVERSION
1$:     CLR R2                  ;INDICATES START OF SIGNIFICANCE
        MOV  TENS+10,R3         ;POINTERS TO TENS POWERS
```

Table L-12 Tape Recorder Interface Checkout
Program Listing (contd)

```
        MOV  4,R4
2$:     CLR R0                  ;CLEAR HIGH ORDER DIVIDEND
        DIV -(R3),R0            ;DIVIDE BY TENS POWER
        BNE 3$
        TST R2                  ;HAS SIGNIFICANCE STARTED?
        BNE 3$                  ;BRANCH IF IT HAS
        MOVB  ' ,(R5)+          ;SUPPRESS LEADING ZEROES
        BR 4$
3$:     ADD  60,R0              ;MAKE IT ASCII
        MOVB R0,(R5)+           ;STORE IT
        INC R2                  ;WE DON'T HAVE TO SUPPRESS ZEROES
4$:     SOB R4,2$
        ADD  60,R1              ;REMAINDER IS LAST DIGIT
        MOVB R1,(R5)+
        MOV (SP)+,R0            ;RETURN ADDR TO R0
        MOV (SP)+,R1
        MOV (SP)+,R2
        MOV (SP)+,R3
        MOV (SP)+,R4
        MOV (SP)+,R5
        RTS R0
TENS:   .WORD 10.,100.,1000.,10000.
        .LIST
        .END START
```

Appendix M

Visicorder Preamplifier Details

As discussed in Chapter 7, a padding network has to be added to the Visicorder preamplifiers to reduce their sensitivity. Without the network, the preamplifier can be adjusted for a minimum sensitivity of 1.Ø V/in. A divide by 4Ø pad allows a minimum sensitivity of 4Ø V/in. Thus, 18 channels of 2Ø V peak-to-peak can be recorded on the 8-in. (2Ø.3 cm) wide chart with minimum overlap. (The linear range of the system A/D converter is 2Ø V.)

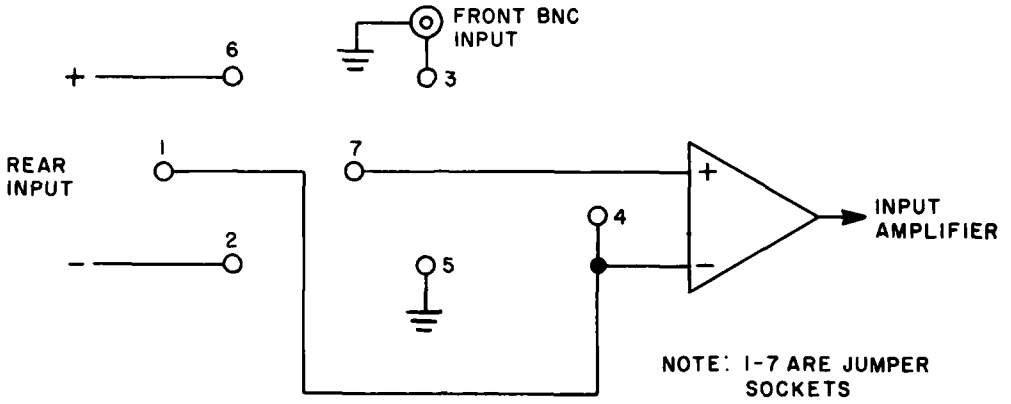
Input connections to the preamp module can be made through either rear-panel mounted connectors or through a female BNC connector on the preamp front panel. Rear-panel inputs can be differentially amplified while the BNC input can only feed a single-ended amplifier. Jumpers within the preamp select the input and its polarity. When the padding circuit is used with the preamp, the jumpers are removed and the circuit plugged in their place.

Figure M-1 shows the input jumper socket arrangement. Table M-1 gives the jumper insertion requirements for the various input/polarity combinations. Normal polarity results in a left trace displacement (viewed while facing the Visicorder) with positive voltage; reverse results in right displacement.

The input padding circuit is shown in Figure M-2. It consists of a dual resistive voltage divider and provides a rear-input standard polarity input. The circuit is built up on locally-fabricated modules that plug into the preamp. Figure M-3 shows the inside view of the preamp with both the standard input jumpers and the padding circuit installed.

The input sensitivity of the preamplifier can be set using two adjustments on the front panel of the unit. These adjustments allow the minimum sensitivity to be set to 1 V/in. (with sensitivity switch

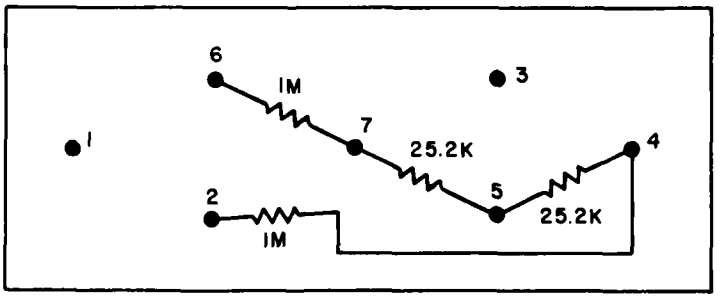
set to Ø.5 V/DIV). Either a calibrated square wave or dc voltage source can be used for the calibration. Table M-2 gives the sensitivities resulting from both standard and minimum sensitivity adjustments with and without the padding circuit installed.



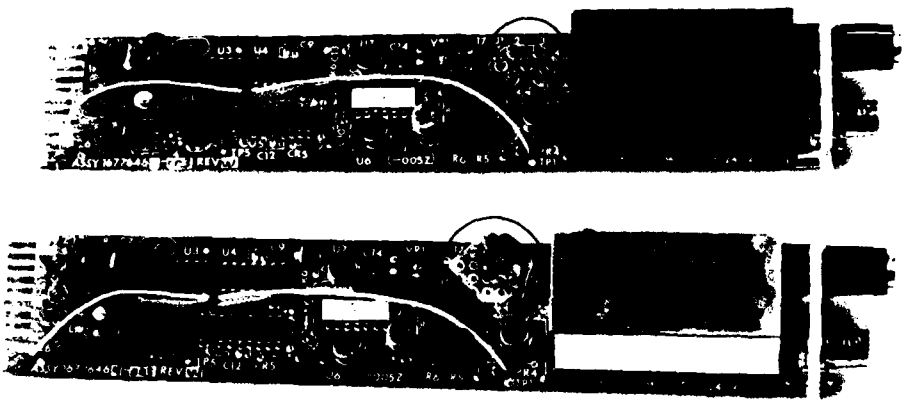
M-1. Visicorder Preamp Input Schematic

Table M-1 Visicorder Preamp Input Jumper Insertion

Input	Jumpers
Rear Input, Standard Polarity	1-2, 6-7
Rear Input, Reverse Polarity	1-6, 2-7
Front Input, Standard Polarity	3-7, 4-5
Front Input, Reverse Polarity	3-4, 5-7



M-2. Visicorder Preamp Padding Module Schematic



M-3. Visicorder Preamp Internal Views

Table M-2 Visicorder Preamp Sensitivities

Gain Switch Position	Resulting Sensitivity (V/in.)			
	Unpadded		Padded	
	Standard Sensitivity	Minimum Sensitivity	Standard Sensitivity	Minimum Sensitivity
.5	0.5	1.0	20	40
.2	0.2	0.4	8	16
.1	0.1	0.2	4	8
.05	0.05	0.1	2	4

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