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CARNEGIE-MELLON UNIV PITTSBURGH PA DEPT OF COMPUTER --ETC F/6 9/2
CMU-11 ENGINEERING DOCUMENTATION.(U)

JAN 77 S H FULLER, T M MCWILLIAMS

F44620-73-C-0074

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CMU-11 ENGINEERING DOCUMENTATION

S. H. Fuller, T. M. McWilliams, and W. H. Sherwood
Department of Computer Science
Carnegie-Mellon University
Pittsburgh, PA 15213

January 1977

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ABSTRACT

The CMU-11 is a microprogrammable processor built with the Intel 3000 microcomputer set that emulates the PDP-11 architecture. In addition, it has been designed to provide full Unibus support. The enclosed documentation gives the details of the CMU-11 design. This documentation has been generated in conjunction with the Stanford Drawing System, the SAGE simulator, and the Intel 3000 microassembler. Those hoping to do any further development of the CMU-11 design are encouraged to also use these design aids and all of the CMU-11 design information shown here (and other information such as ROM contents and wirelists) are available on magnetic tape. See the following report for an introductory discussion and evaluation of the CMU-11:

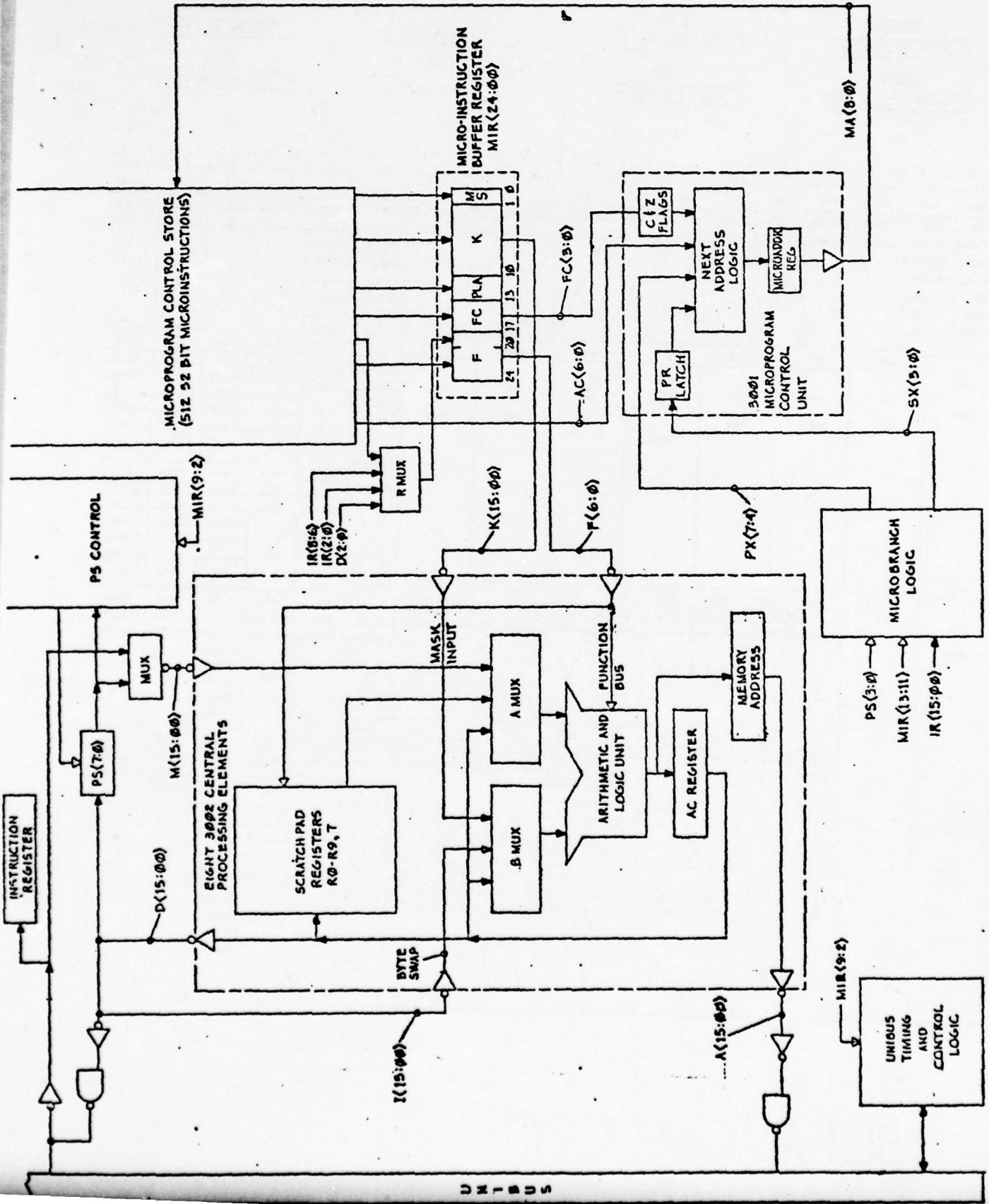
McWilliams, T. M., S. H. Fuller, and W. H. Sherwood, "Using LSI Processor Bit-Slice to Build a PDP-11: A Case Study in Microcomputer Design," Technical Report, Department of Computer Science, Carnegie-Mellon University, Pittsburgh, PA, January 1976.

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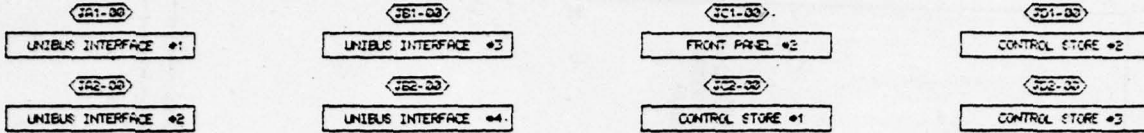
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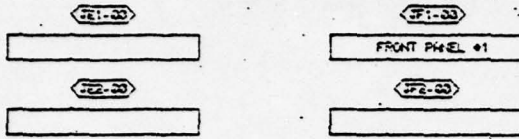


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3	UNINT	UNINT												UNINT	UNINT													
4	UNINT	UNINT												UNINT	UNINT													
5	UNINT	UNINT												UNINT	UNINT													
6	UNINT	UNINT												UNINT	UNINT													
7	UNINT	UNINT												UNINT	UNINT													
8	AA09													CC09	CC09													
9		AD10	AG10	BJ10	BD10	BE10	CA10	CD10						CC09	CC09	DB10	DC10	DF10	DH10									
10	OPE													24S11	24S20	2400	2422	2427	24S22									
11		OPE	OPE	OPE	LOOK AHEAD CARRY		OPE	OPE	OPE	OPE				MIC01	DET10													
12	3002													PSR	PSR	UNINT	SPLINE	SPLINE	BUS04									
13		3002	3002	3002			3002		3002	3002				MIC10		UNINT	SPLINE	SPLINE	UNINT									
14																MASTER	BUS04	UNINT	MASTER									
15														CC12		CL001	CL00					PSH1						
16																												
17														24S28	CC17													
18														SPLINE	24S28	DB16	DC16	DF16	DH16									
19															CL001	2430	24S28	24S18	24S22									
20															MIC10	PSR		SPLINE	PSR									
21														PSR				MIC10	MIC10	CL00								
22														PSR				MIC10	BUS04	CL00								
23																		CL00										
24	AA24													CC25	CC25													
25														24S18	3002	3002	3002	3002	24S17E	24S17E	24S17A	24S28	24S28	24S27	24S27			
26	OPE													MIC02	CTLSTO	CTLSTO	CTLSTO	INSPE2	INSPE2	FLINE2	PIPE01	PIPE02	CL00	BUS04	24S15			
27	3002																											
28																		CL00	BUS04	PSR	1-8	1-8	SPLINE	SPLINE				
29																					1-8	1-7						
30																					MIC01							
31																					1-4	1-4						
32																					CTLSTO							
33																												
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E									F								
A	B	C	D	E	F	G	H	J	A	B	C	D	E	F	G	H	J
EA01	EA01	EA01	EA01	EA01	EA01	EA01	EA01	EA01	FB01	FB01	FB01	FB01	FB01	FB01	FB01	FB01	FB01
7451EB	7451EP	7452	7451E1	7451ZE	7451ZE	7414B	74524	7454									
UNIMUX	PSH1	PSH2	QA.001	INSEPG	INSEPG	MICINI	QA.001	MASTER									
			QA.001				QA.001	MASTER									
			PSH1					CLOCK									
			PSH2					PSH1									
			PSH2					PSH2									
EA10	EA10	EA10	EA10	EA10	EA10	EA10	EA10	EA10	FB10	FB10	FB10	FB10	FB10	FB10	FB10	FB10	FB10
7410	74504	74507	74508	74572	74503	74574	74574	74574									
SEL.INE	BUSO4	MICR01	QA.001	MICIN2	MICIN2	BUSO4P	BUSO4P	MICIN2									
DAT10	BUSO4C	MICR01	DAT10	MICIN2	MICIN2	BUSO4P	DAT10	MICIN2									
MASTER	DAT10	MICR01	PSH1	CLOCK	MICIN2												
	SEL.INE	MICR01	QA.001	BYDEG1	MICIN2												
	CLOCK																
	CLOCK																
EA18	EA18	EA18	EA18	EA18	EA18	EA18	EA18	EA18	FB18	FB18	FB18	FB18	FB18	FB18	FB18	FB18	FB18
74511	7470	74574	7427	74520	7474	74507	74574	74500									
SEL.INE	PSH1	BUSO4C	MICIN2	PSH2	PSH2	MICR01	MICIN2	SEL.INE									
BUSO4C		DAT10	PSH2	PSH2	BYDEG2	SEL.INE	MASTER	SEL.INE									
BUSO4C			BUSO4C			UNIMUX		SEL.INE									
EA26	EA26	EA26	EA26	EA26	EA26	EA26	EA26	EA26	FB26	FB26	FB26	FB26	FB26	FB26	FB26	FB26	FB26
74512B	7414B	74517B	74517B	74517B	74517B	74574	74517B	74504									
MICR02	BUSO4C	BUSO4C	1-4	PSH2	MASTER	MICIN2	MICIN2	QA.001									
			2														
			UNIMUX														
			MICR02														
			1-4														
			1-4														
			1-4														
EA36	EA36	EA36	EA36	EA36	EA36	EA36	EA36	EA36	FB36	FB36	FB36	FB36	FB36	FB36	FB36	FB36	FB36
74520	7427	74520	74520	74574	74520	74504	74520	74520									
MU	MU	BUSO4C	BUSO4C	BUSO4C	BUSO4C	UNIMUX	UNIMUX	QA.001									
MASTER	BUSO4C	DAT10	BUSO4C	DAT10	BUSO4C	UNIMUX	UNIMUX	QA.001									
	MICR01	MICIN2	CLOCK	INSEPG	INSEPG	UNIMUX	UNIMUX	QA.001									
		MICR01	QA.001	DAT10	UNIMUX	UNIMUX	MICIN2										
					UNIMUX	UNIMUX											
EA43	EA43	EA43	EA43	EA43	EA43	EA43	EA43	EA43	FB43	FB43	FB43	FB43	FB43	FB43	FB43	FB43	FB43
74127	74127	7427	7452	74512E	7412E	74520	74512A	745127									
MICIN2	MICIN2	MICR01	MICR01	BUSO4C	PSH1	PSH1	PSH1	MICIN2									
MICIN2	BYDEG2																

D43

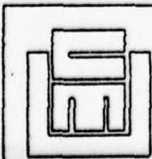
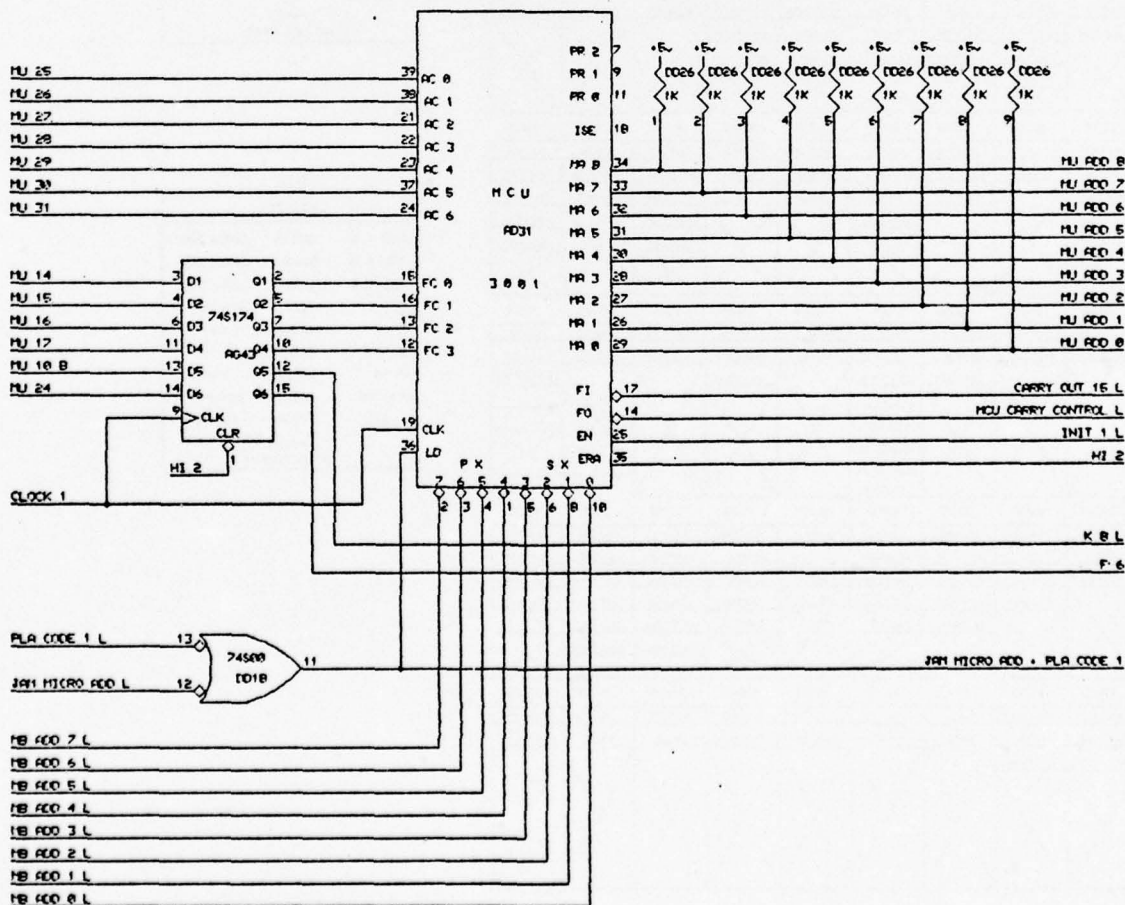
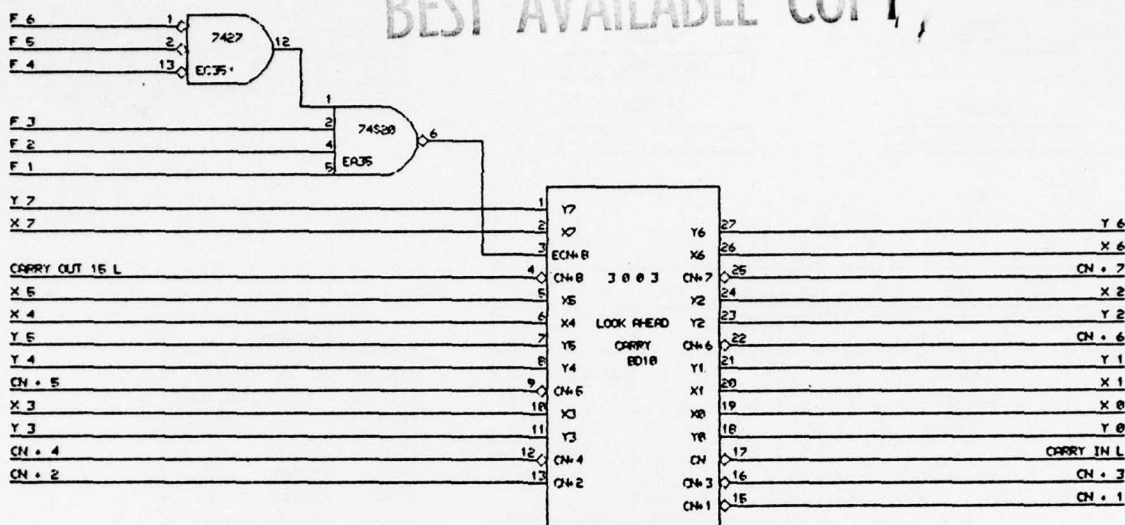
INSET		
RC0 1,2	MICIN2	3.3u 18K
RC0 4,5	MICIN2	3.3u 8.2K
RC 7,10	MICIN2	680P, 12K
R 9	MASTER	18K
R 11	PIPRG2	18K
R 12	BUSO4C	18K
R 14	BUSO4C	5.1K
POT 15	BUSO4C	20K POT
- 3,6	DAT10	POWER
74123		
RC NETWORKS		

D43

INSET		
RC0 1,2	DAT10	.006u 20K
RC0 4,5	BUSO4C	.006u 20K
RC0 7,8	CLOCK	3.3u 12K
POT 9	CLOCK	20K POT
R 11	CLOCK	18K
R 12	CLOCK	5.1K
R 14	DAT10	20K
POT 15	DAT10	20K POT
- 3,6	DAT10	POWER
74123		
RC NETWORKS		

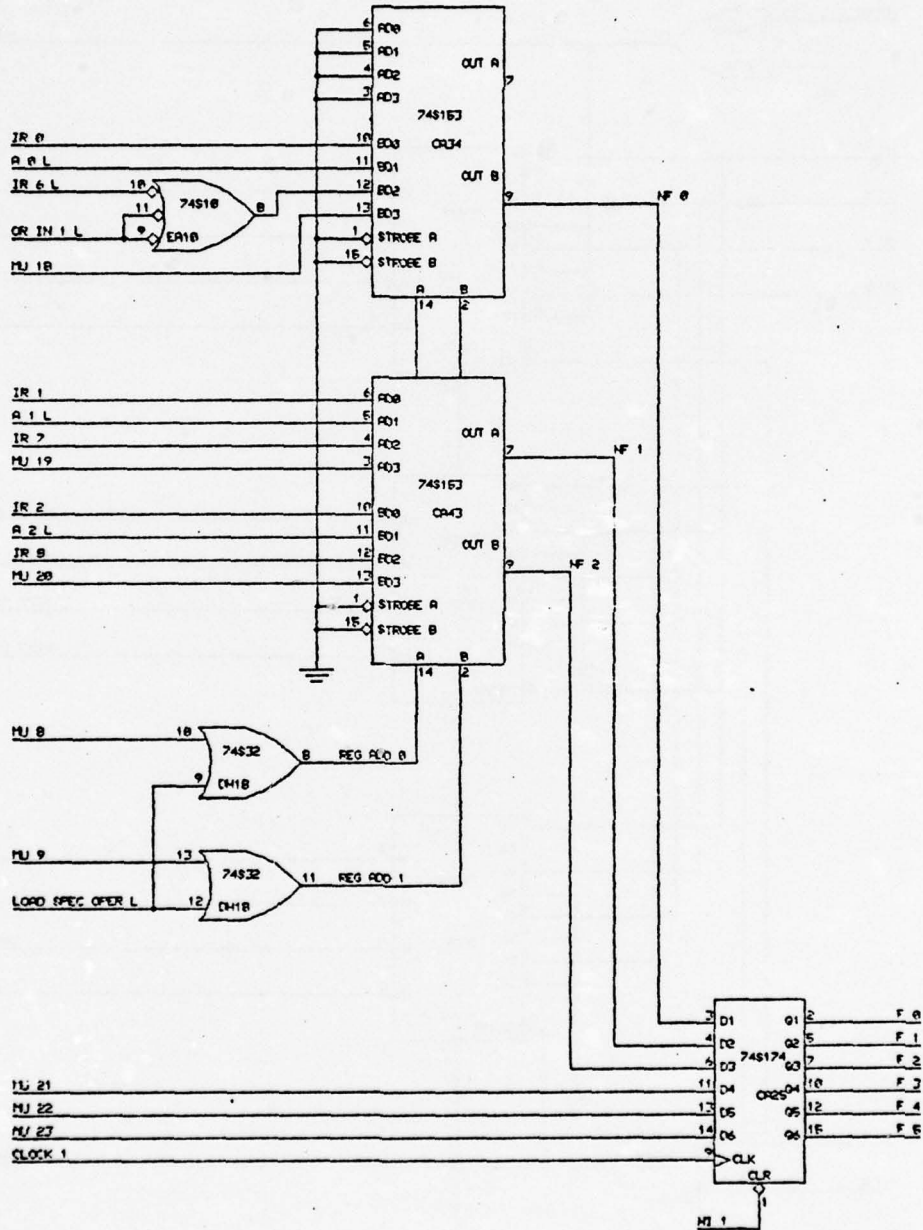
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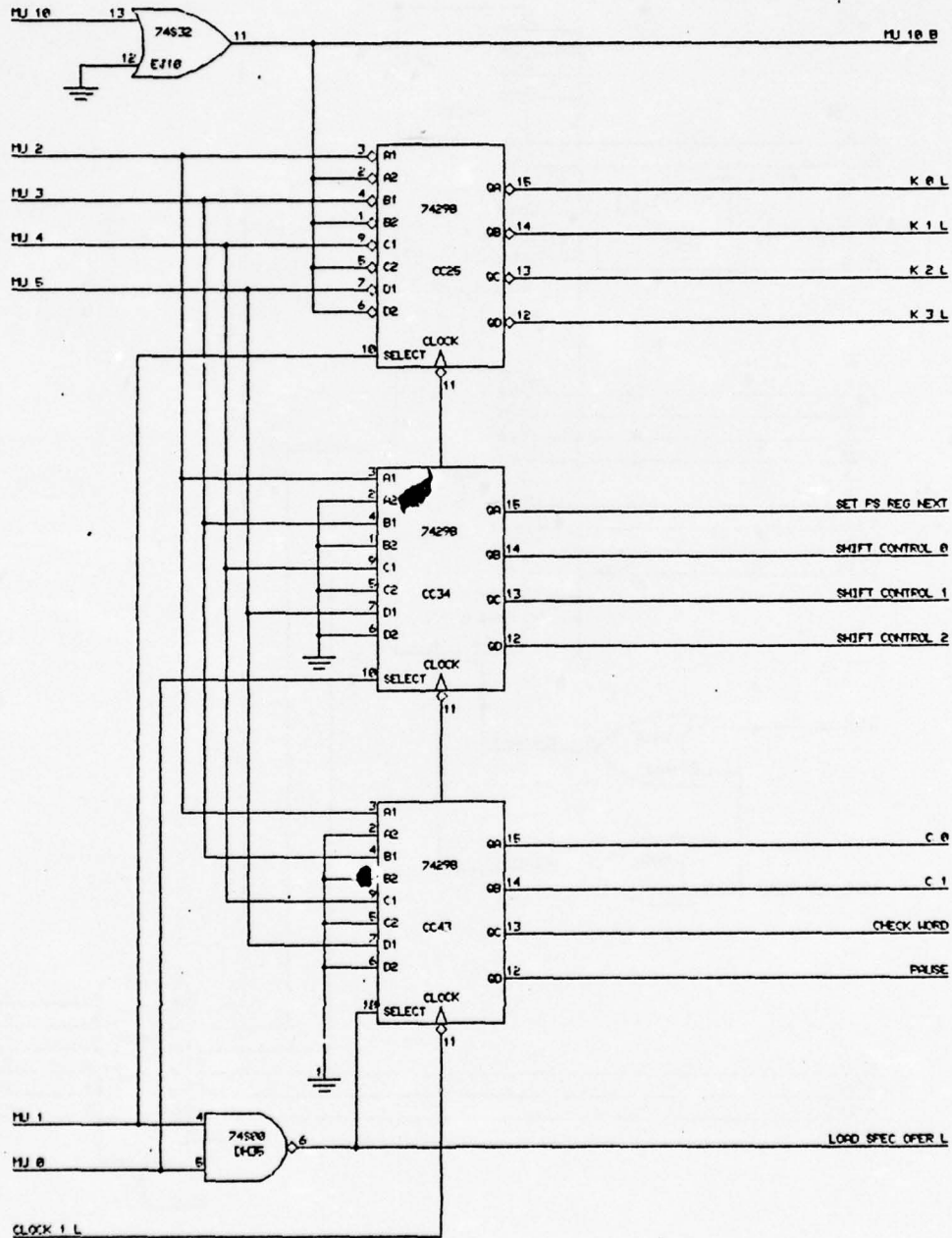


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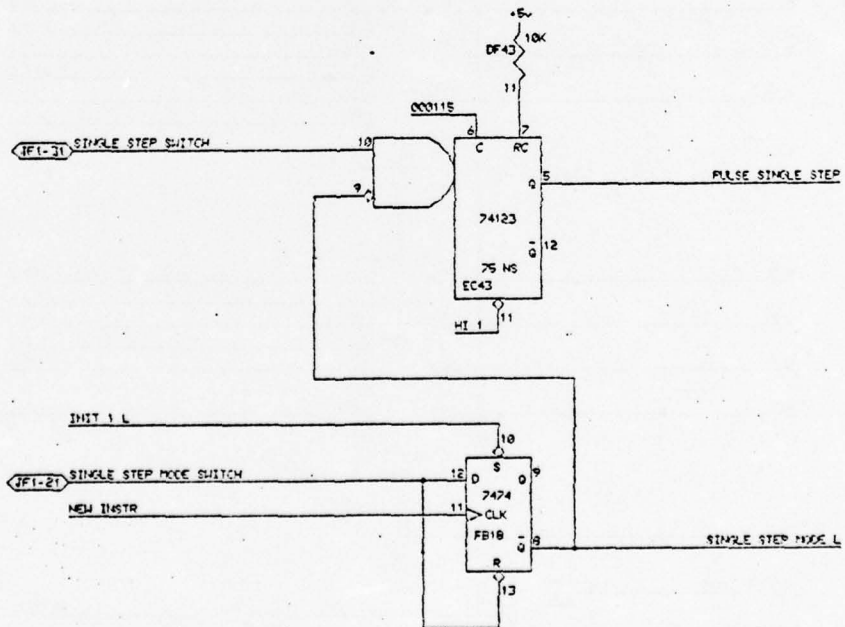
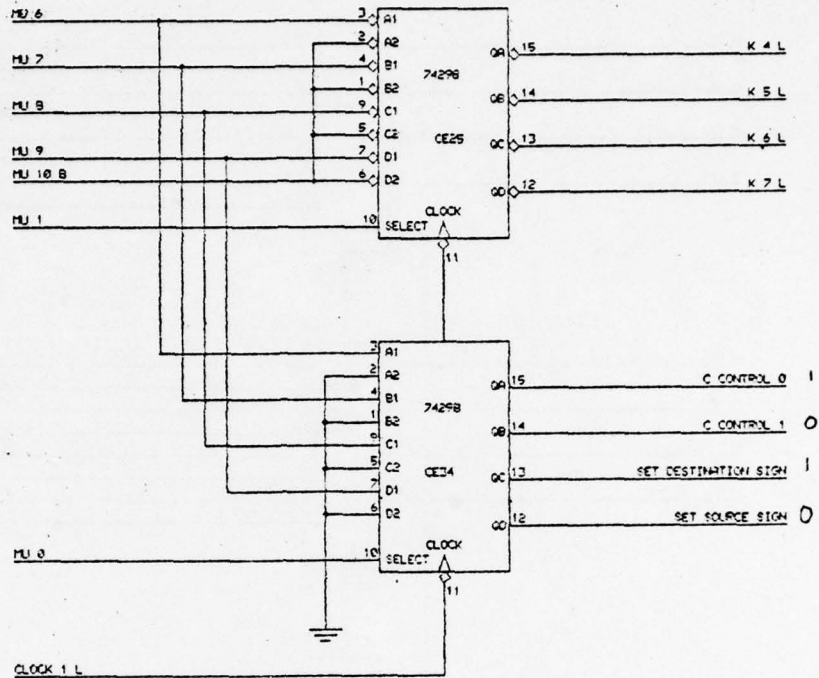


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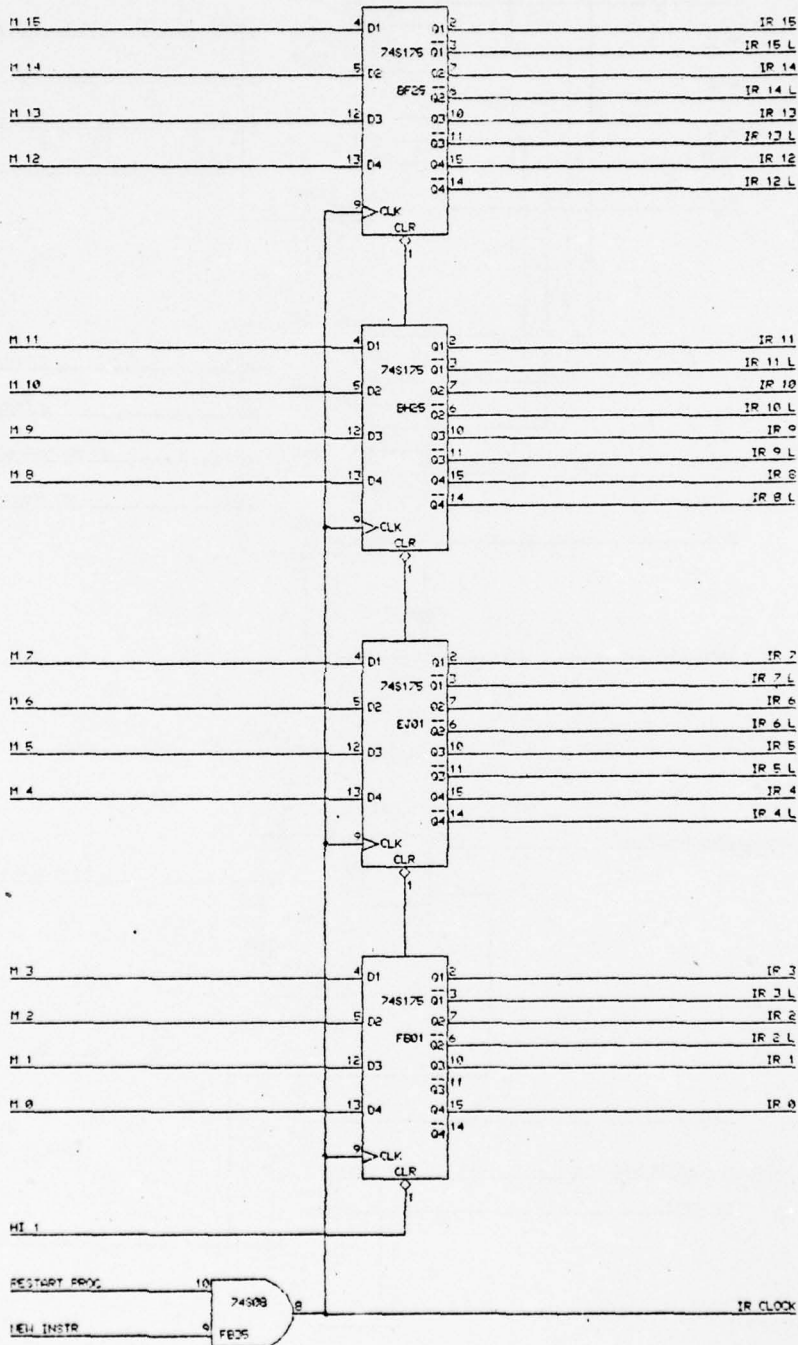


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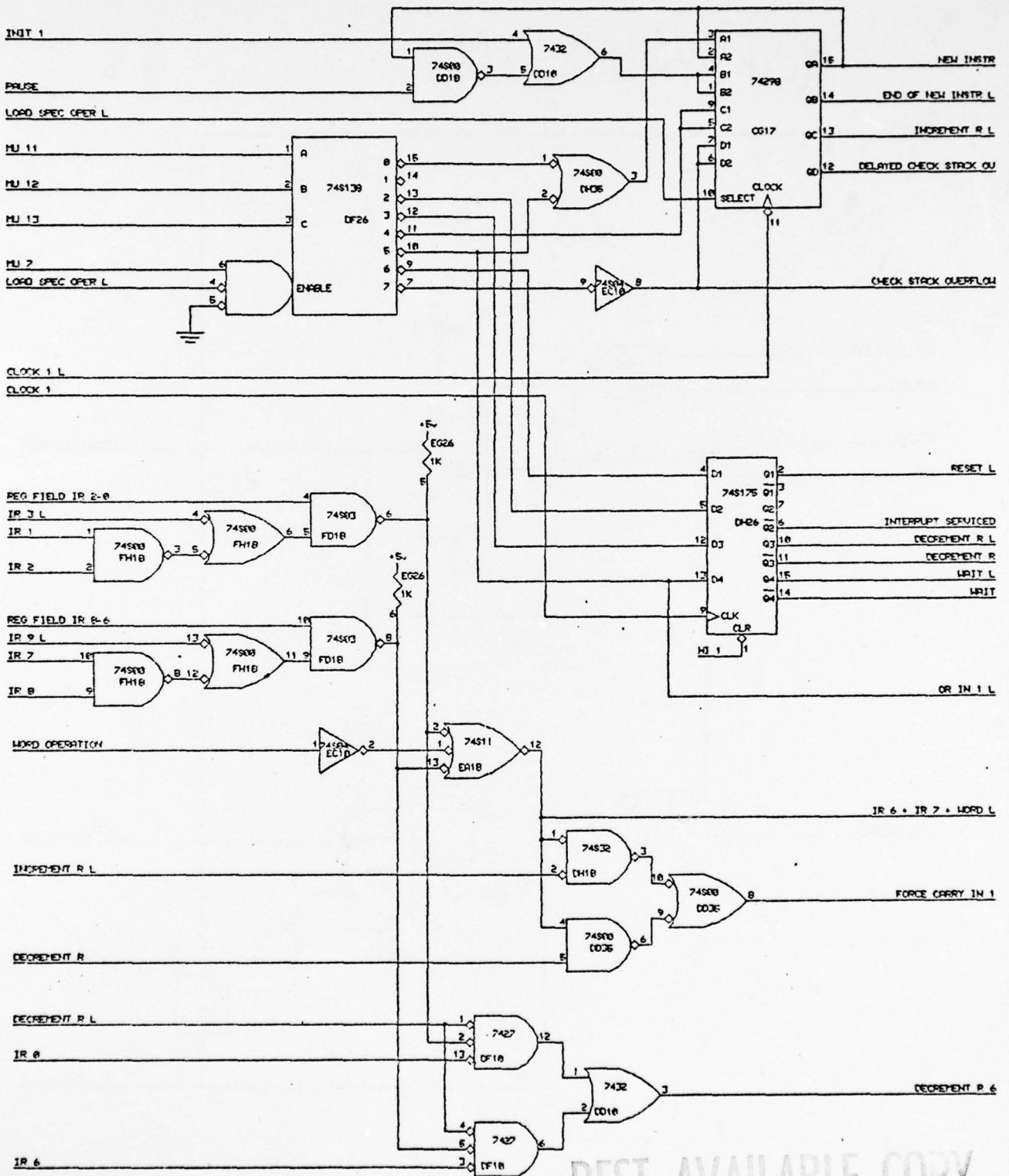


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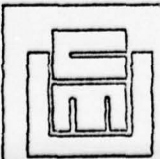


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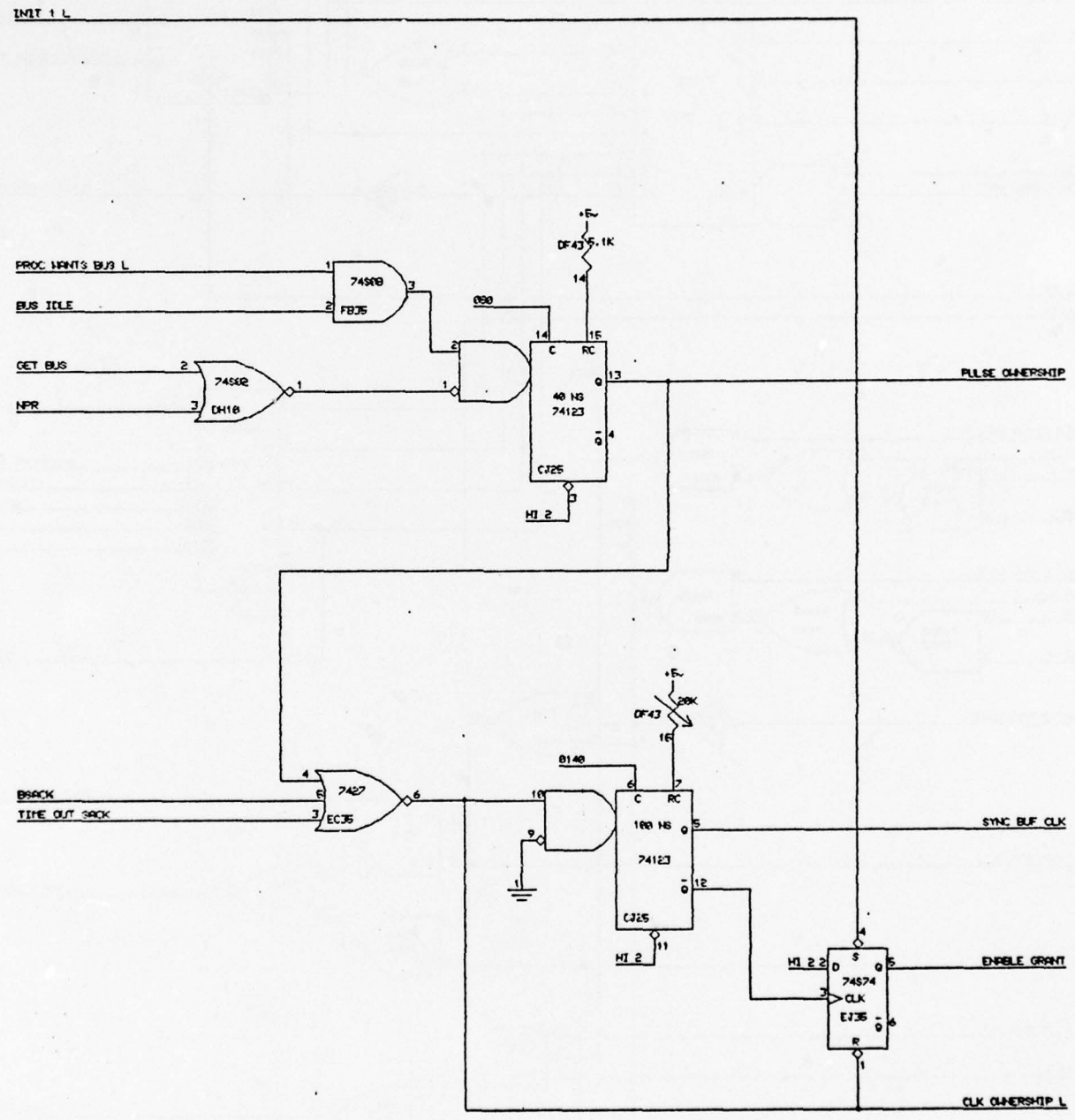


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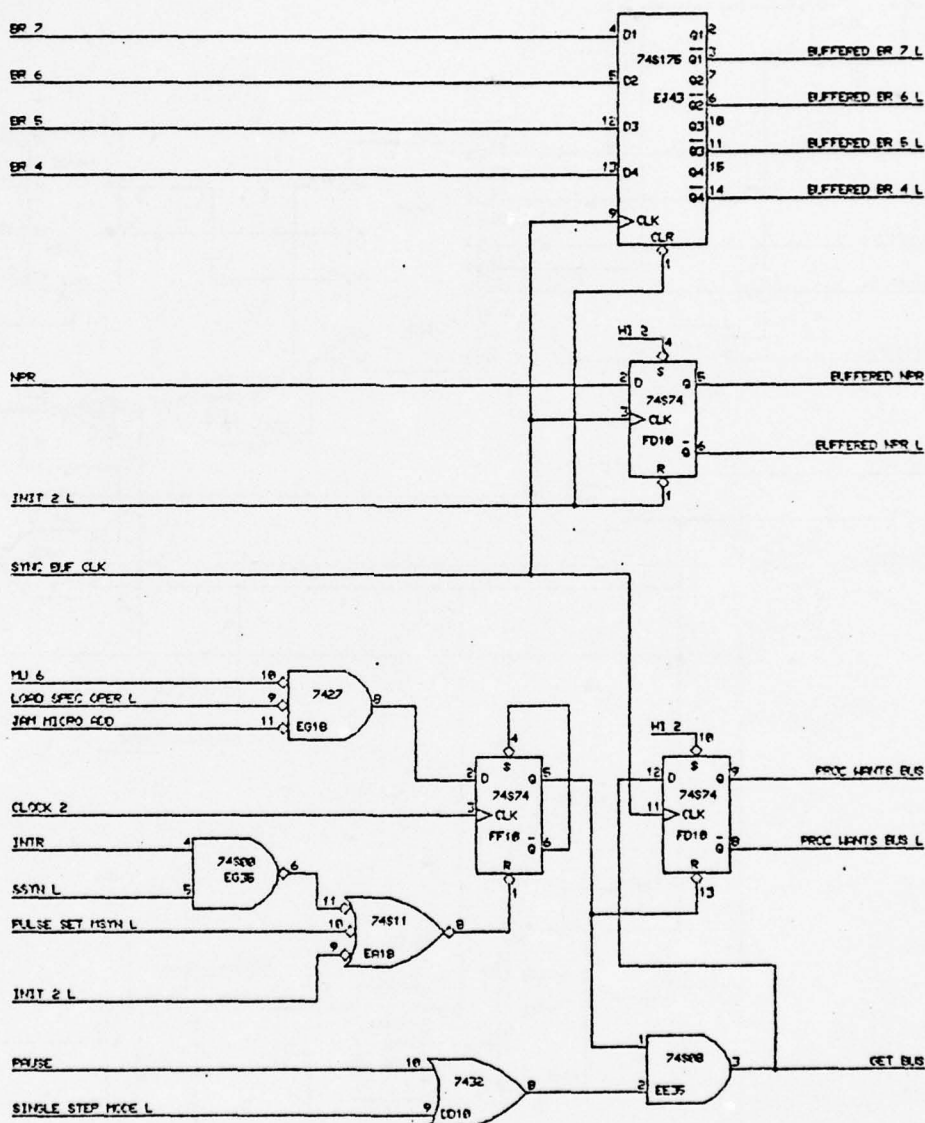
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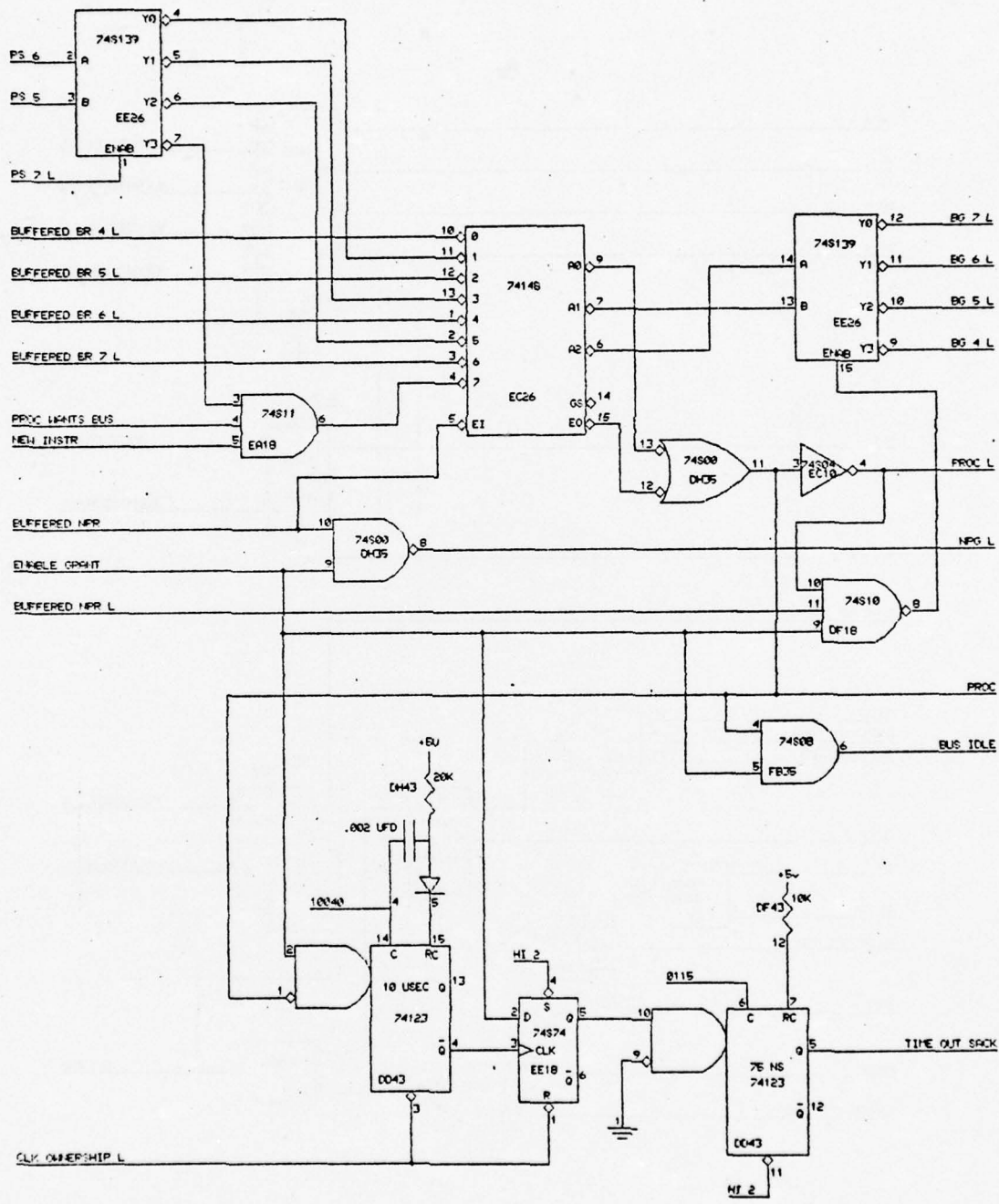


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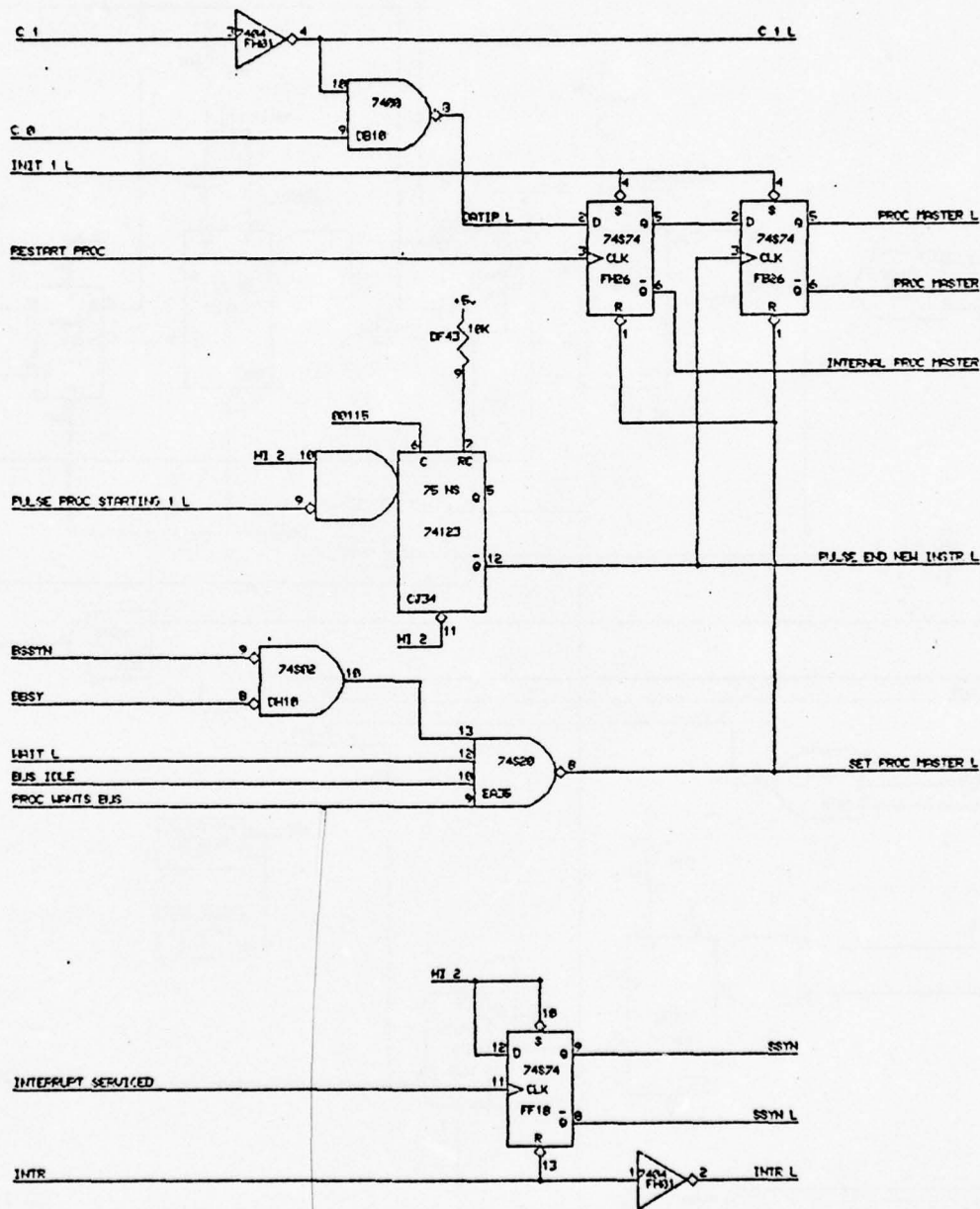
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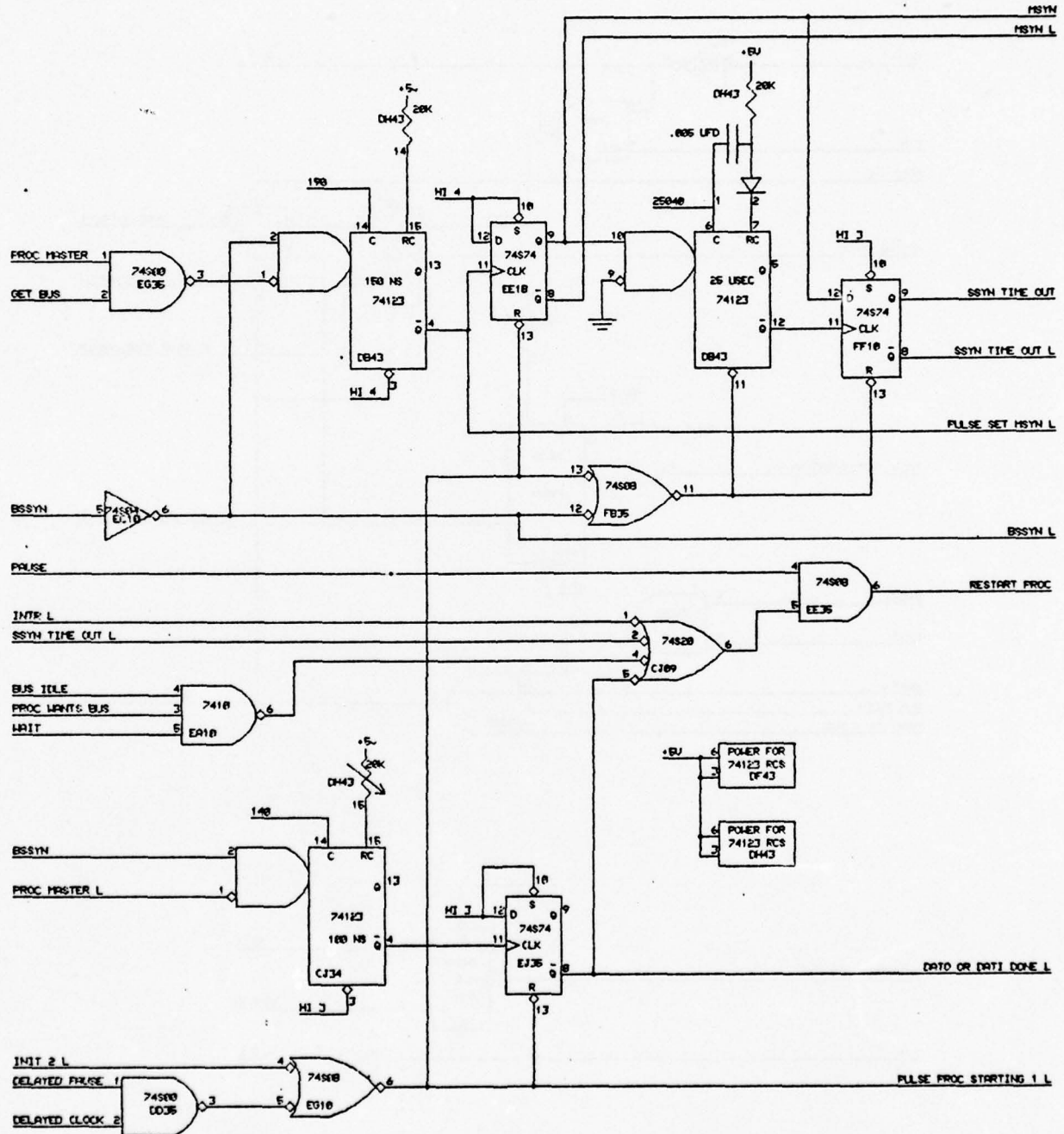
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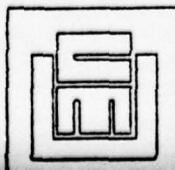
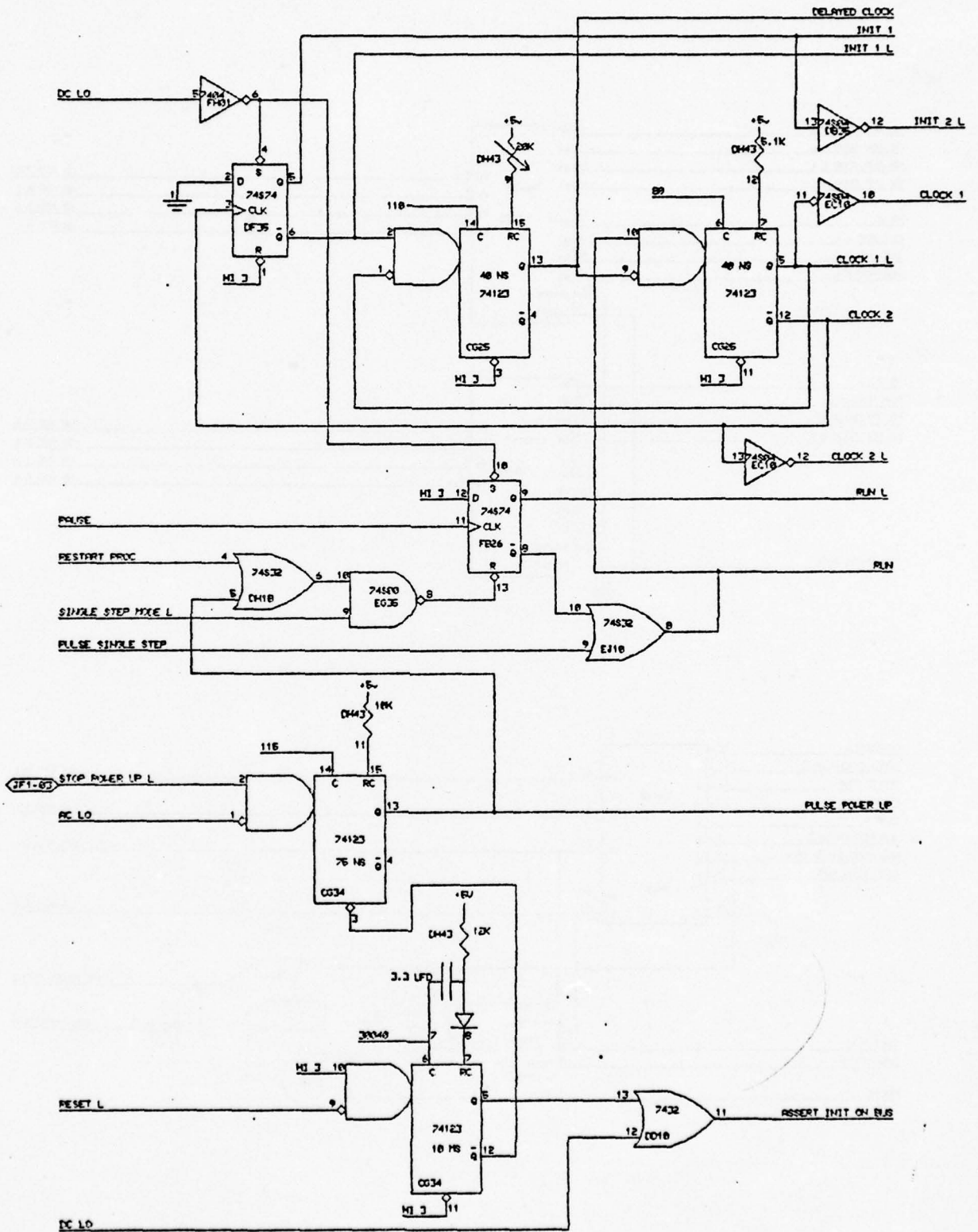
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CARRIE-HELLON UNIVERSITY PITTSBURGH, PENNSYLVANIA 15213		



COMPUTER SCIENCE ENGINEERING LAB			
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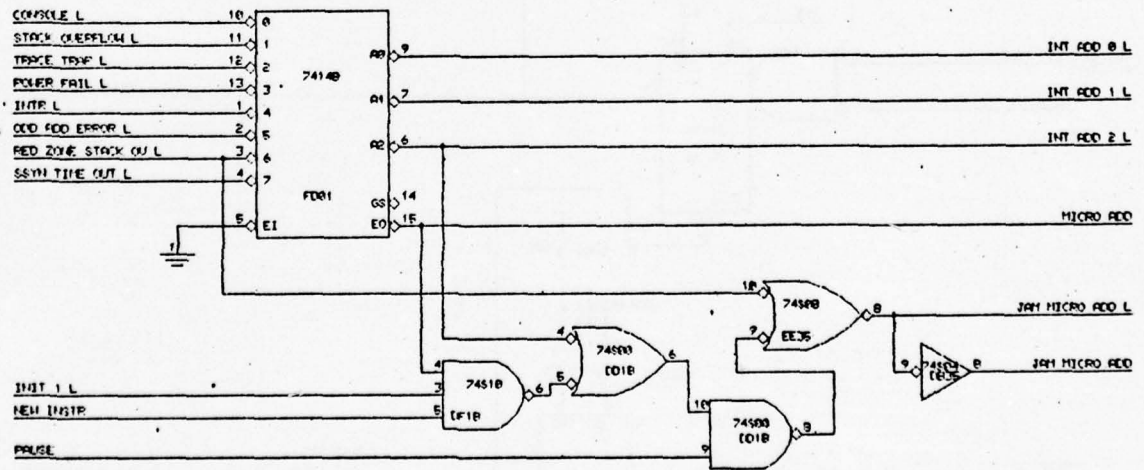
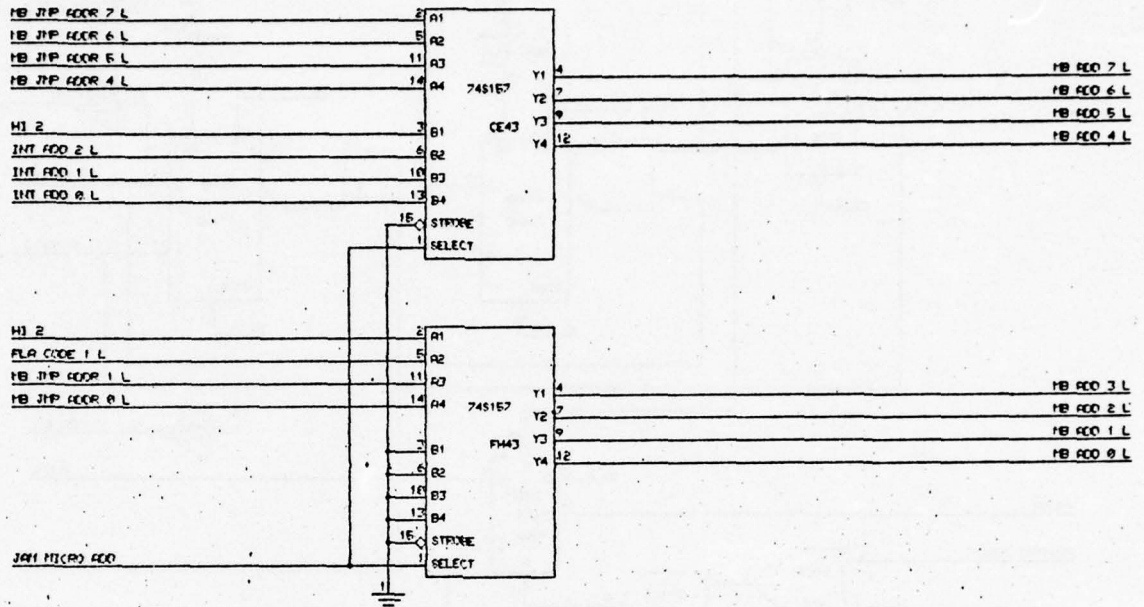
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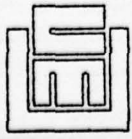


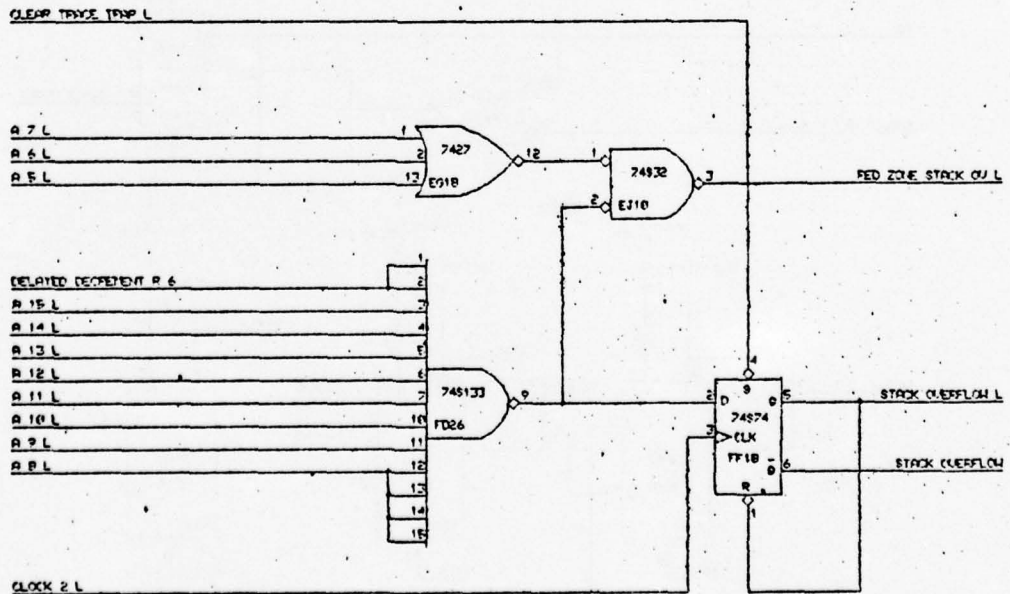
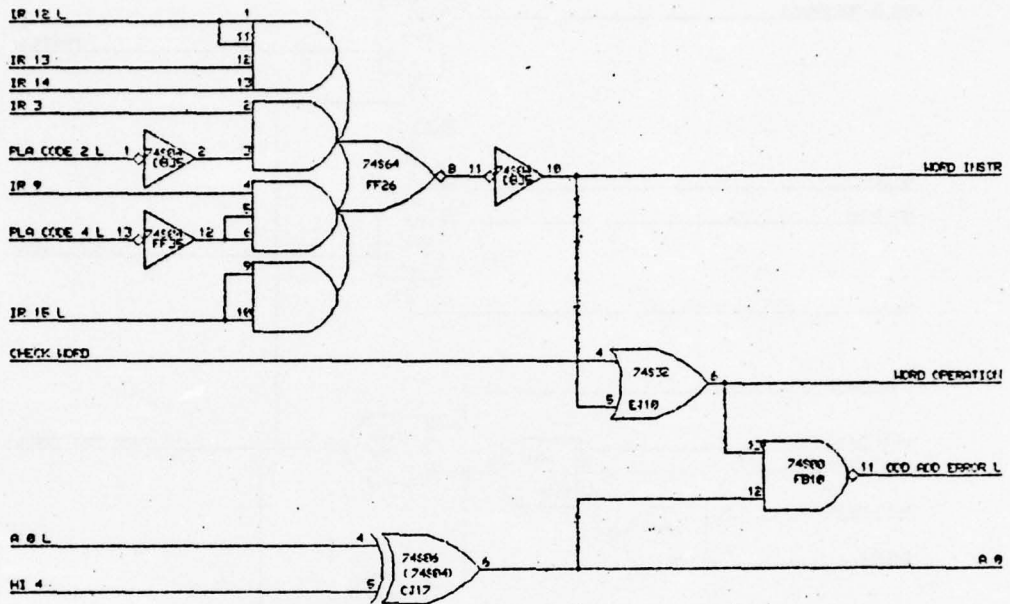
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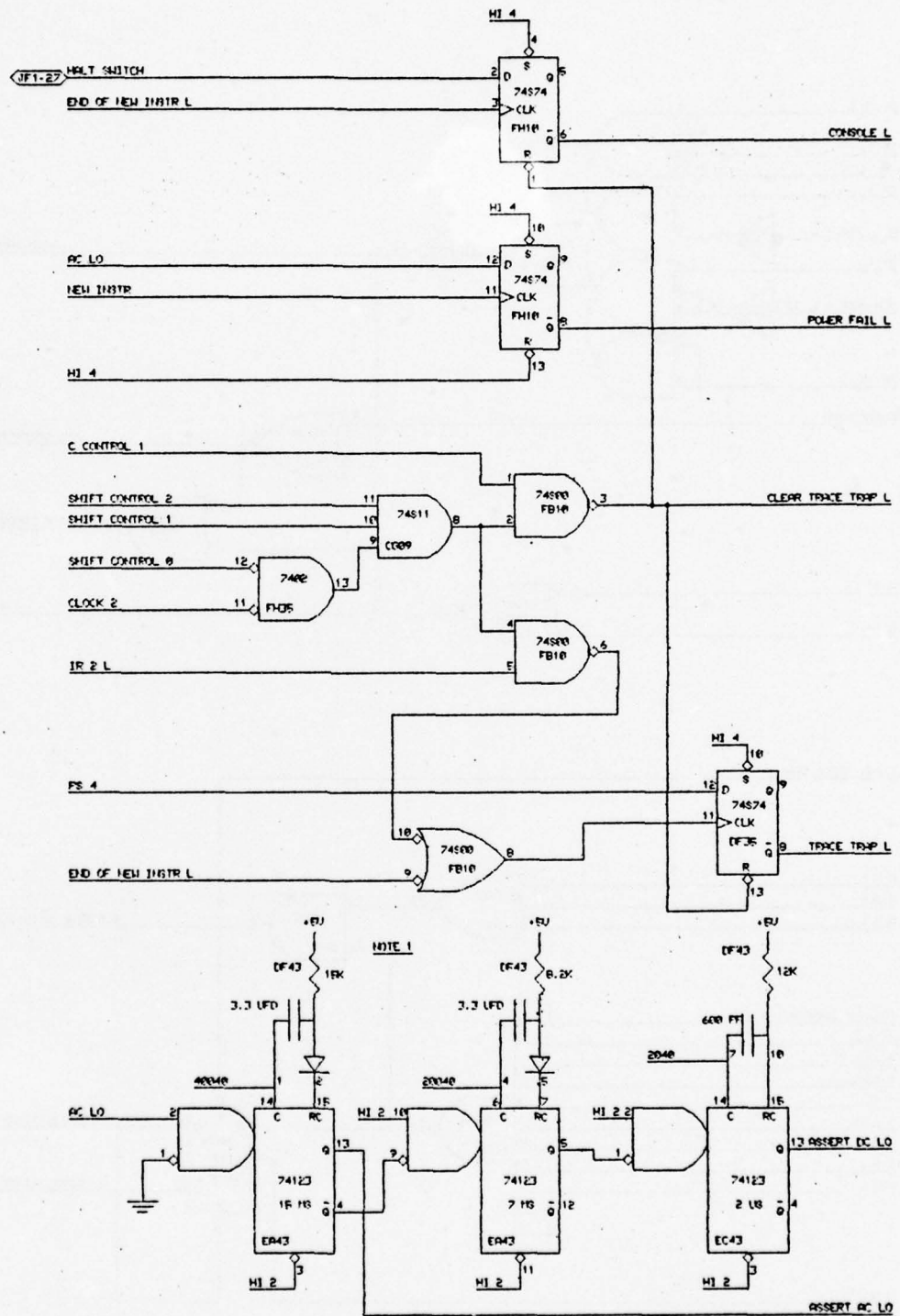
PROCESSOR CLOCK AND INITIALIZATION

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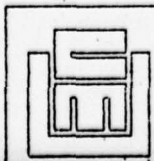


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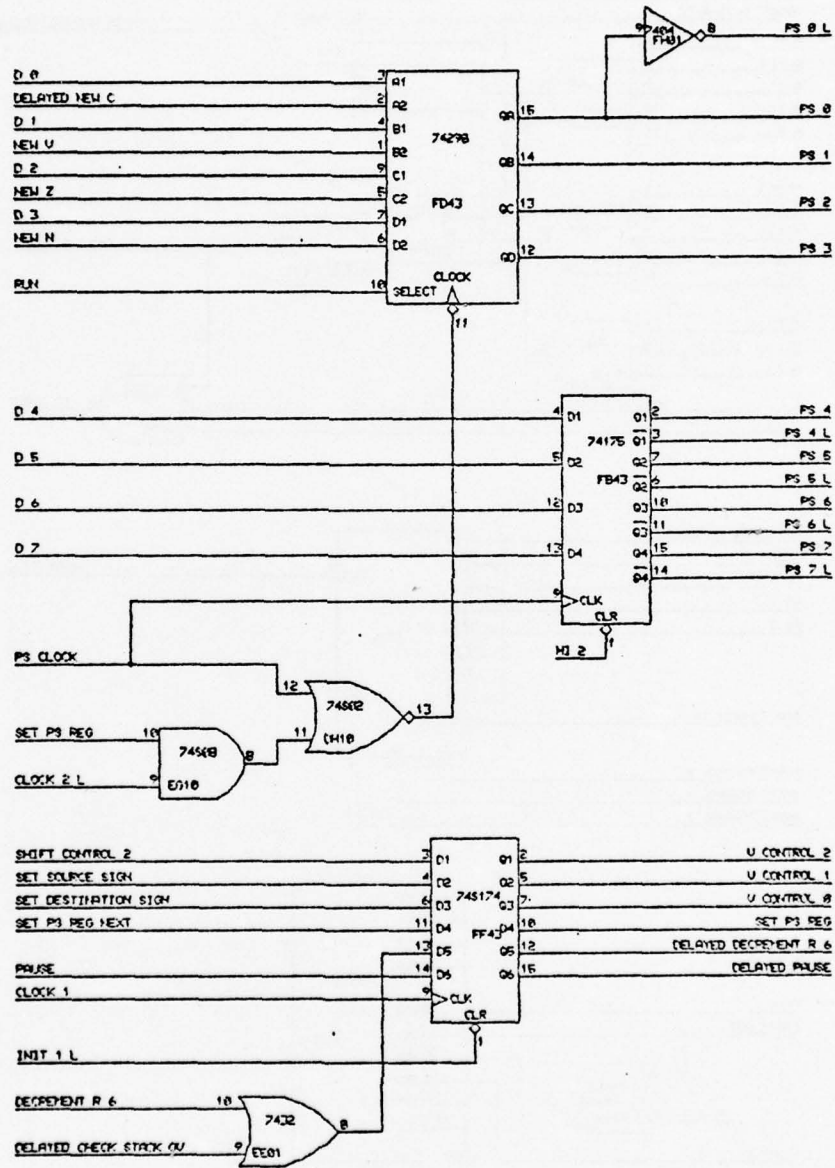


NOTE 1 THIS LOGIC IS TO AVOID EFFECTS OF MULTIPLE AC POWER GLITCHES

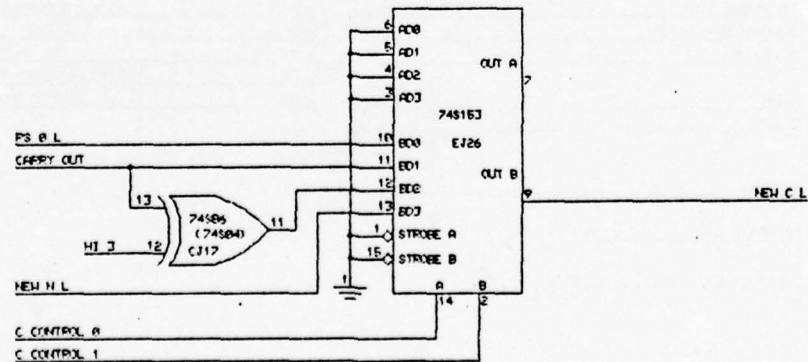
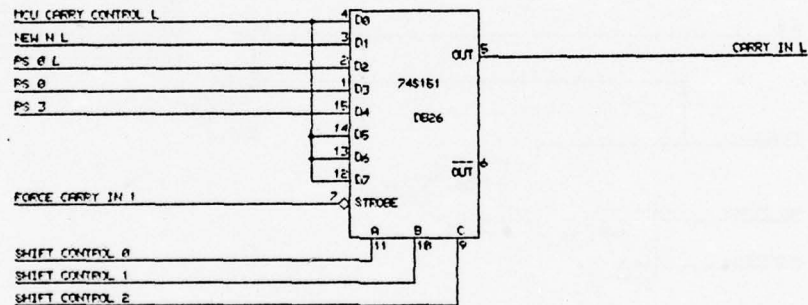
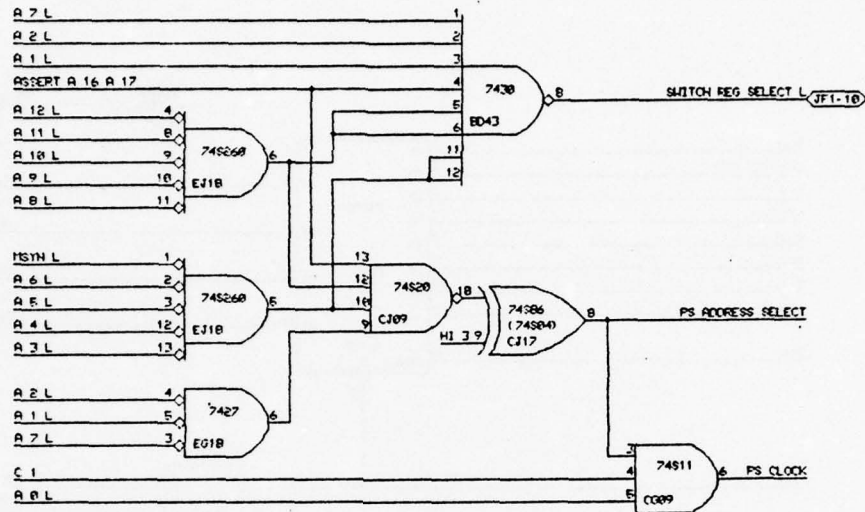


COMPUTER SCIENCE ENGINEERING LAB

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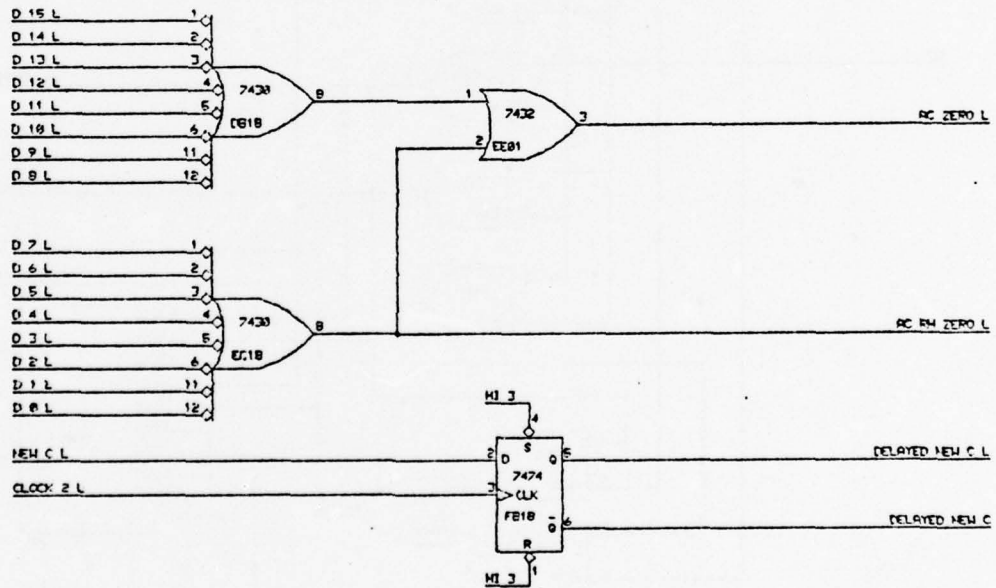
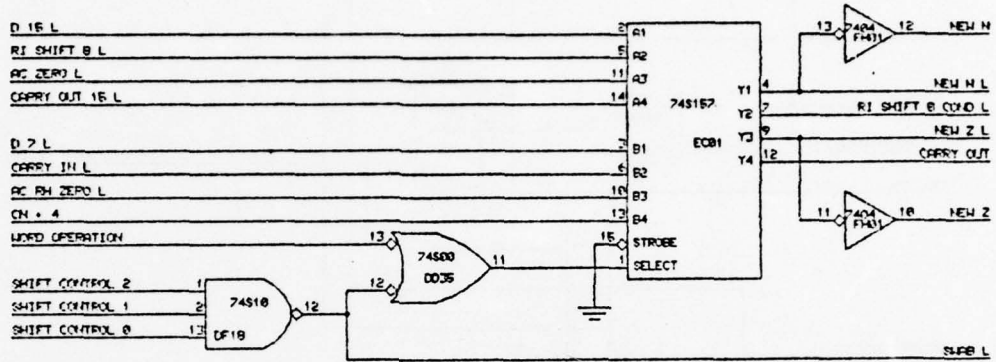


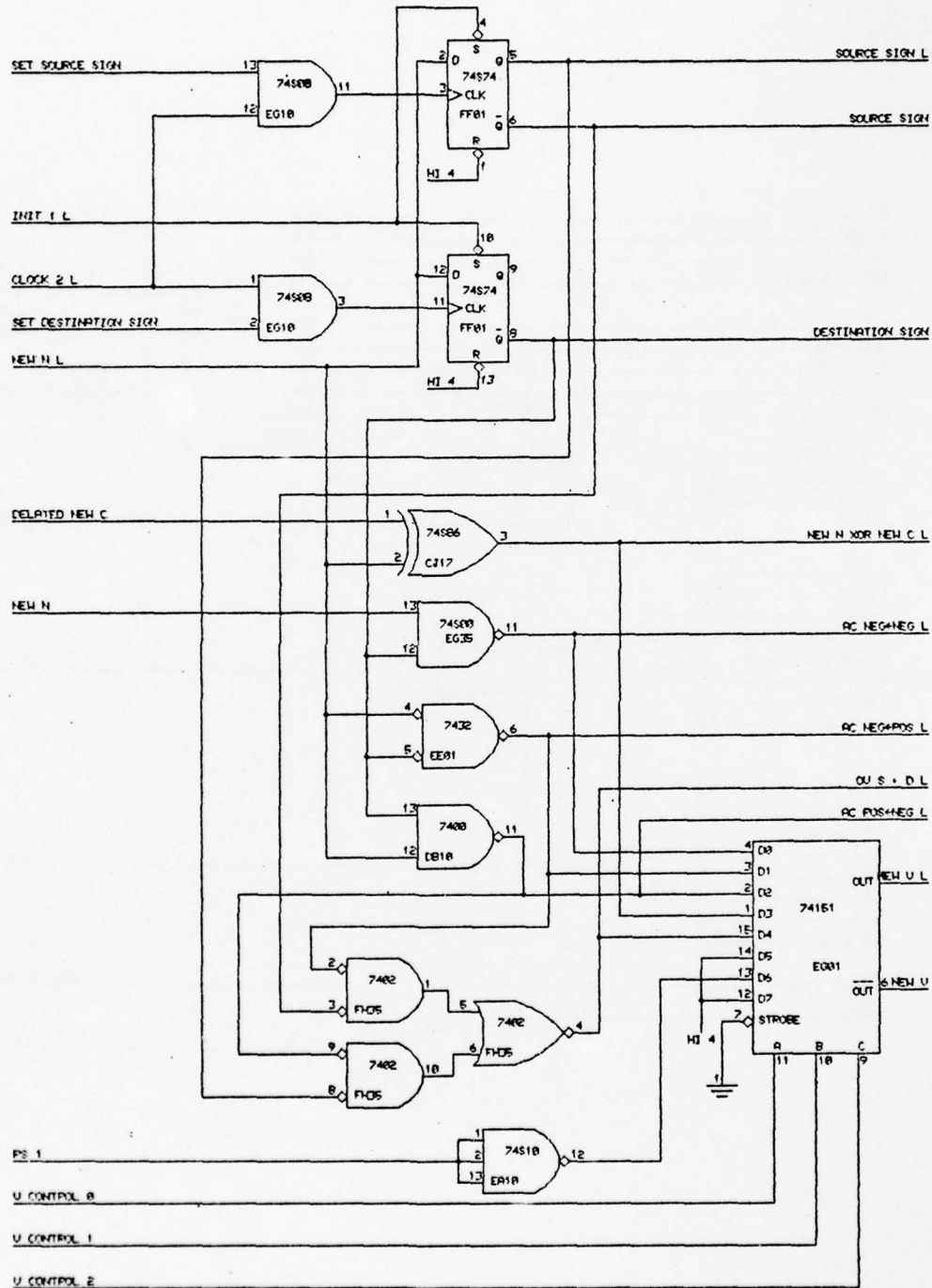
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PROJECT: PDP-11 USING THE INTEL 3000 MICROPROCESSOR			
DESIGN BY: SHERWOOD	CHECKED BY:	DATE:	OF:
WORKING FILE: PSU11 N210TM051	WORKING NUMBER:	DATE: 30-DEC-75	21:55



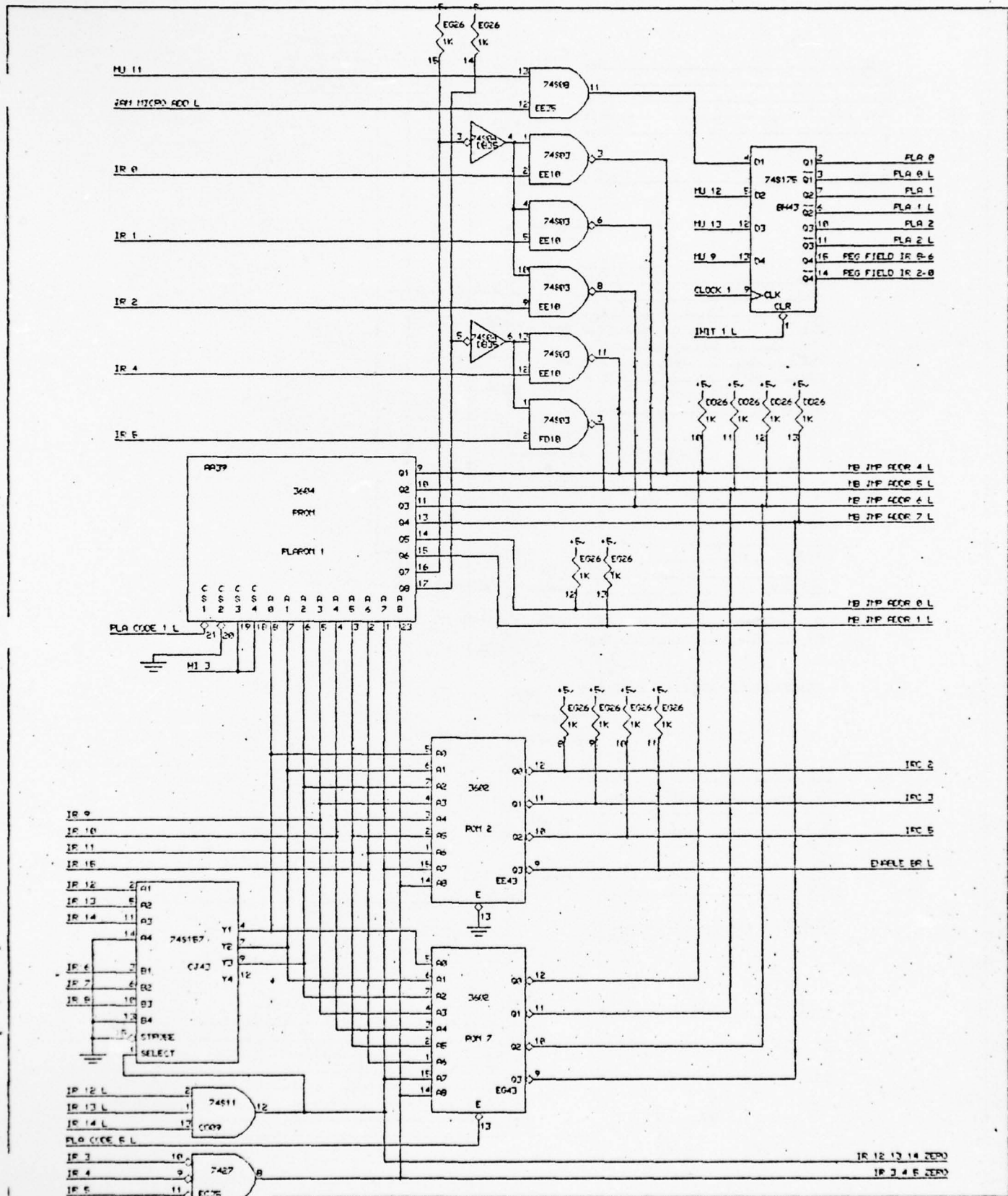
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	TITLE: PS ADDRESS AND CARRY IN CONTROL		
	PROJECT: PDP-11 USING THE INTEL 3000 MICROPROCESSOR		
	DESIGN BY: SHERWOOD	CHECKED BY:	PAGE OF
	PROJECT FILE: PSW2[N210TM05]	PROJECT NUMBER:	DATE: 04-JAN-76 01:07

PITTSBURGH, PENNSYLVANIA 15213



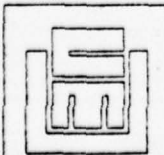
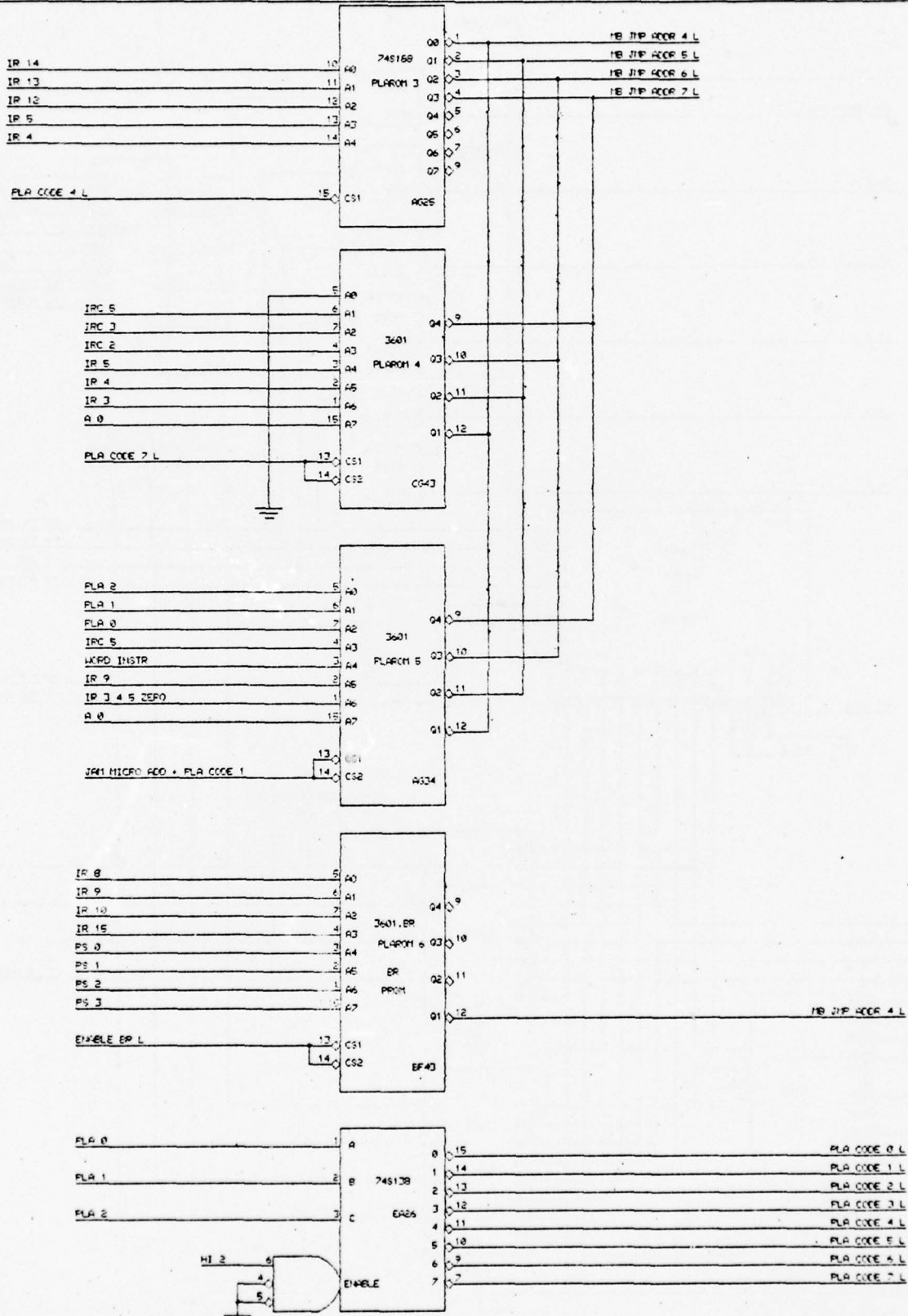


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	PROJECT: PDP-11 USING THE INTEL 3000 MICROPROCESSOR		
	DESIGNED BY: SHERWOOD	CHECKED BY:	PAGE: CF
	DATE: 04-JAN-76 04:57	ISSUING NUMBER:	DATE: 04-JAN-76 04:57
CARNEGIE-MELLON UNIVERSITY			
PITTSBURGH, PENNSYLVANIA 15213			



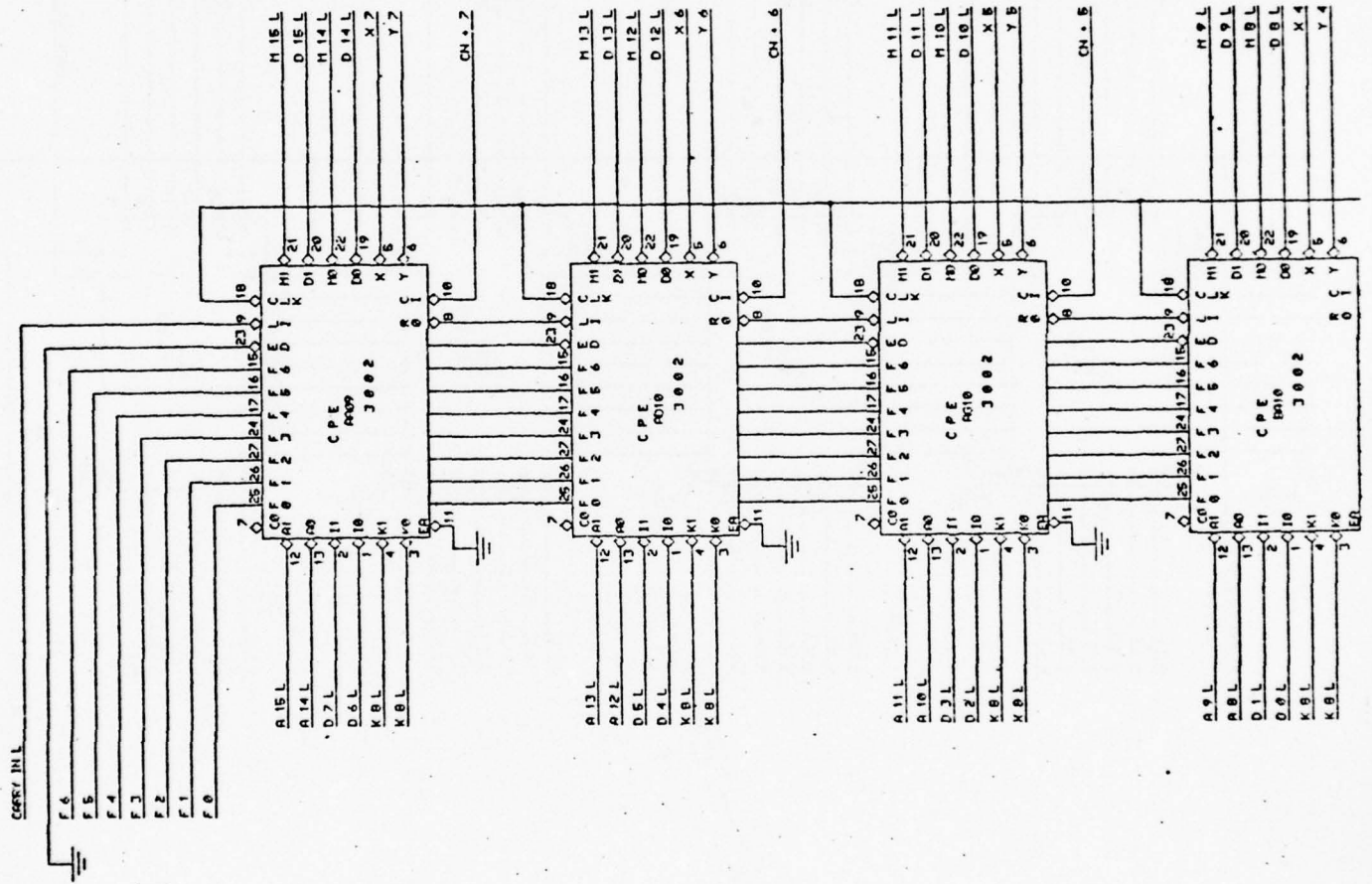
COMPUTER SCIENCE ENGINEERING LAB

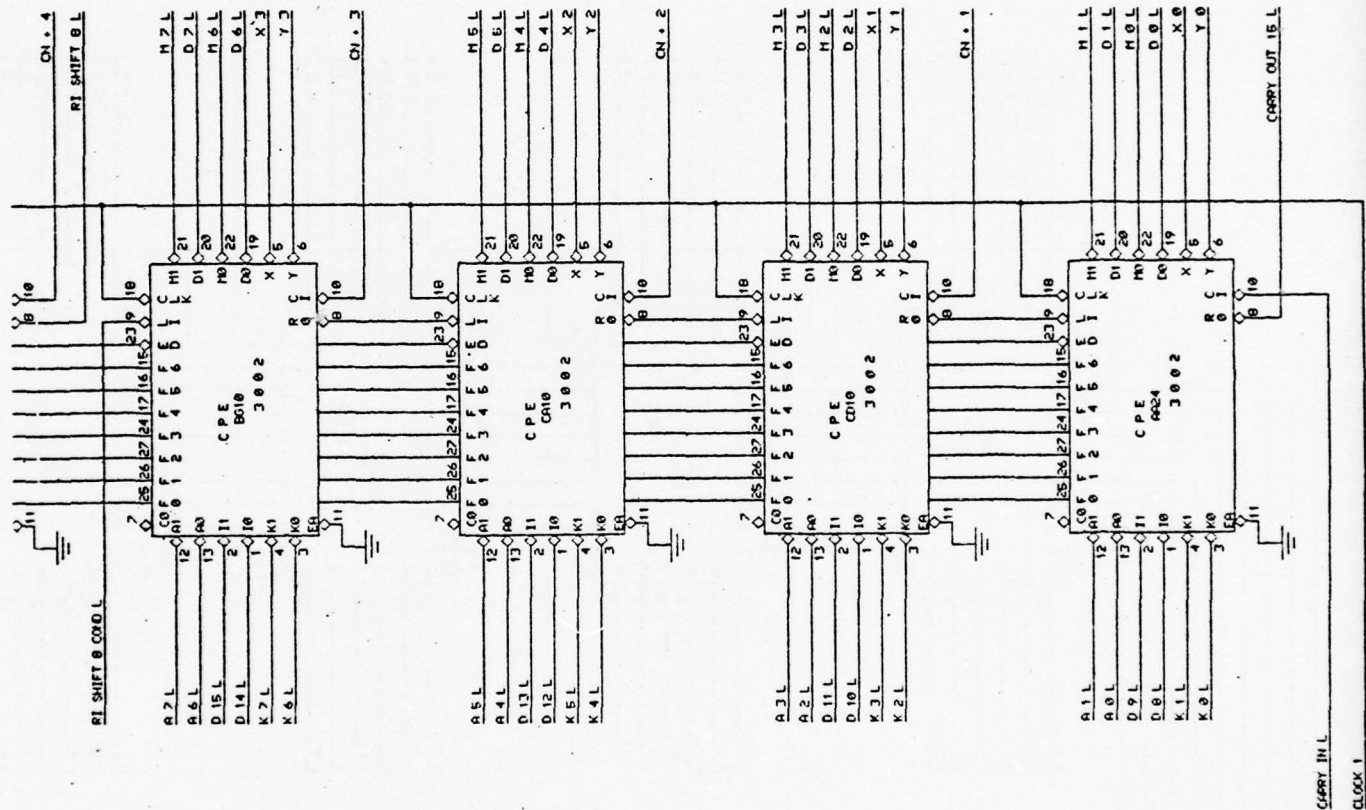
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PROJECT:			
(PRINT BY)	SHERWOOD	CHECKED BY:	
(PRINT FILE)	NEWER1[N210TM05]	(ASSIGN NUMBER)	
PAGE	OF	DATE	
			26-JUN-75 23:02



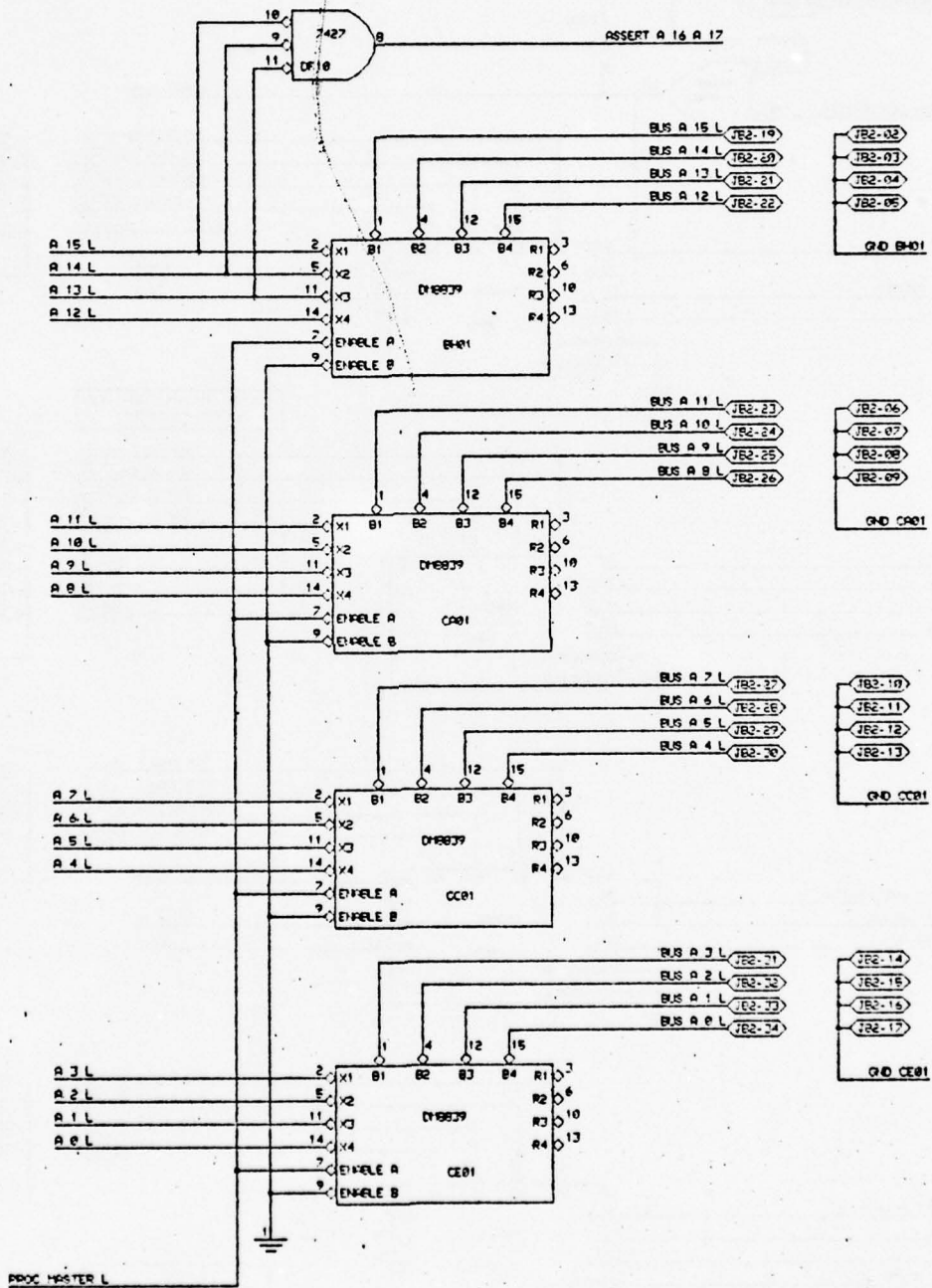
COMPUTER SCIENCE ENGINEERING LAB

TITLE: MICRO CODE BRANCH LOGIC
 PROJECT: PDP-11 USING THE INTEL 3000 MICROPROCESSOR
 DRAWN BY: SHERWOOD
 CHECKED BY:
 DATE: 19-JUN-75 07:41
 CARROLL NUMBER:
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 CARROLL NUMBER:
 DATE:
 PITTSBURGH, PENNSYLVANIA 15213

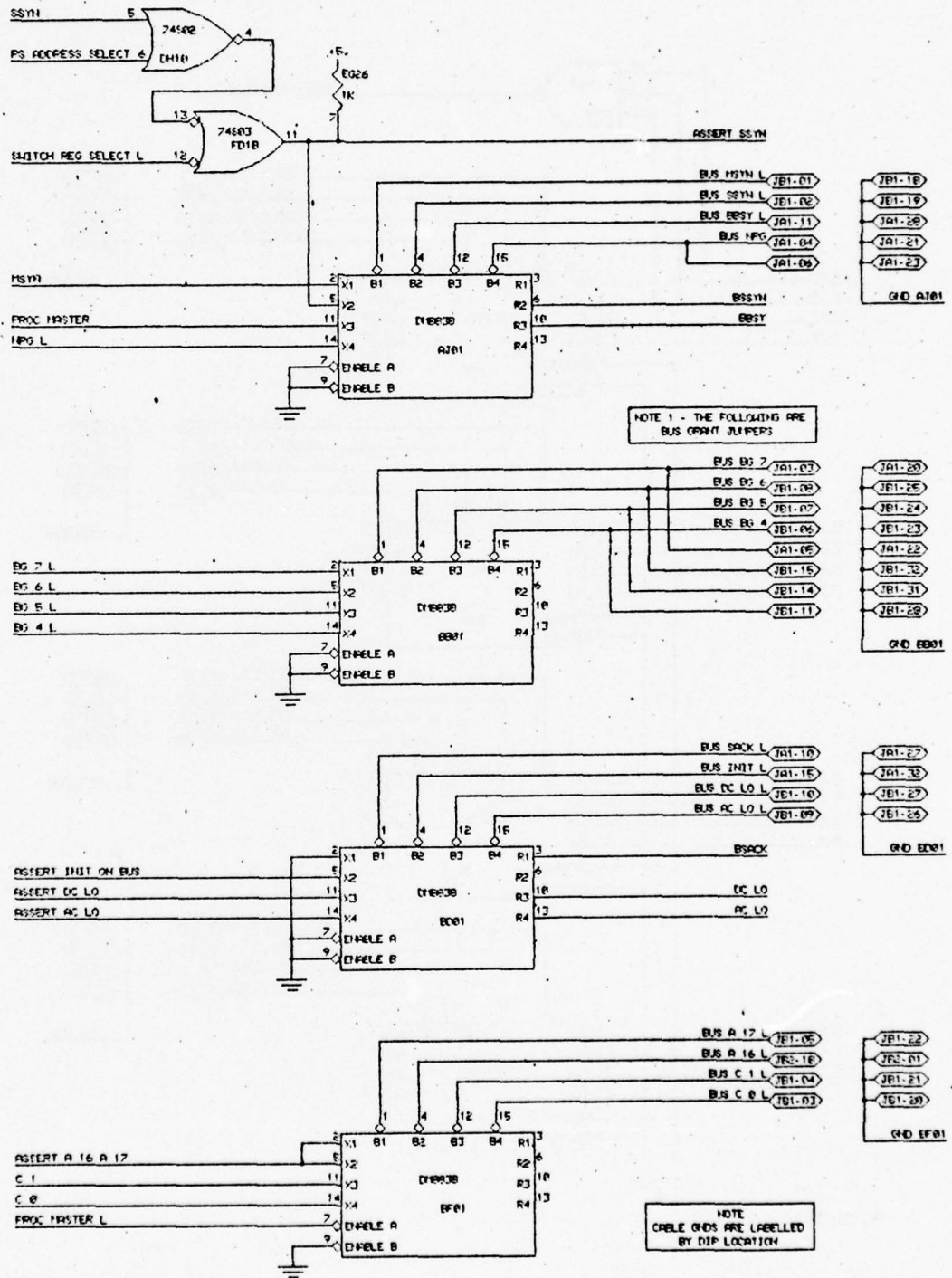




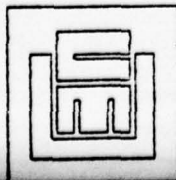
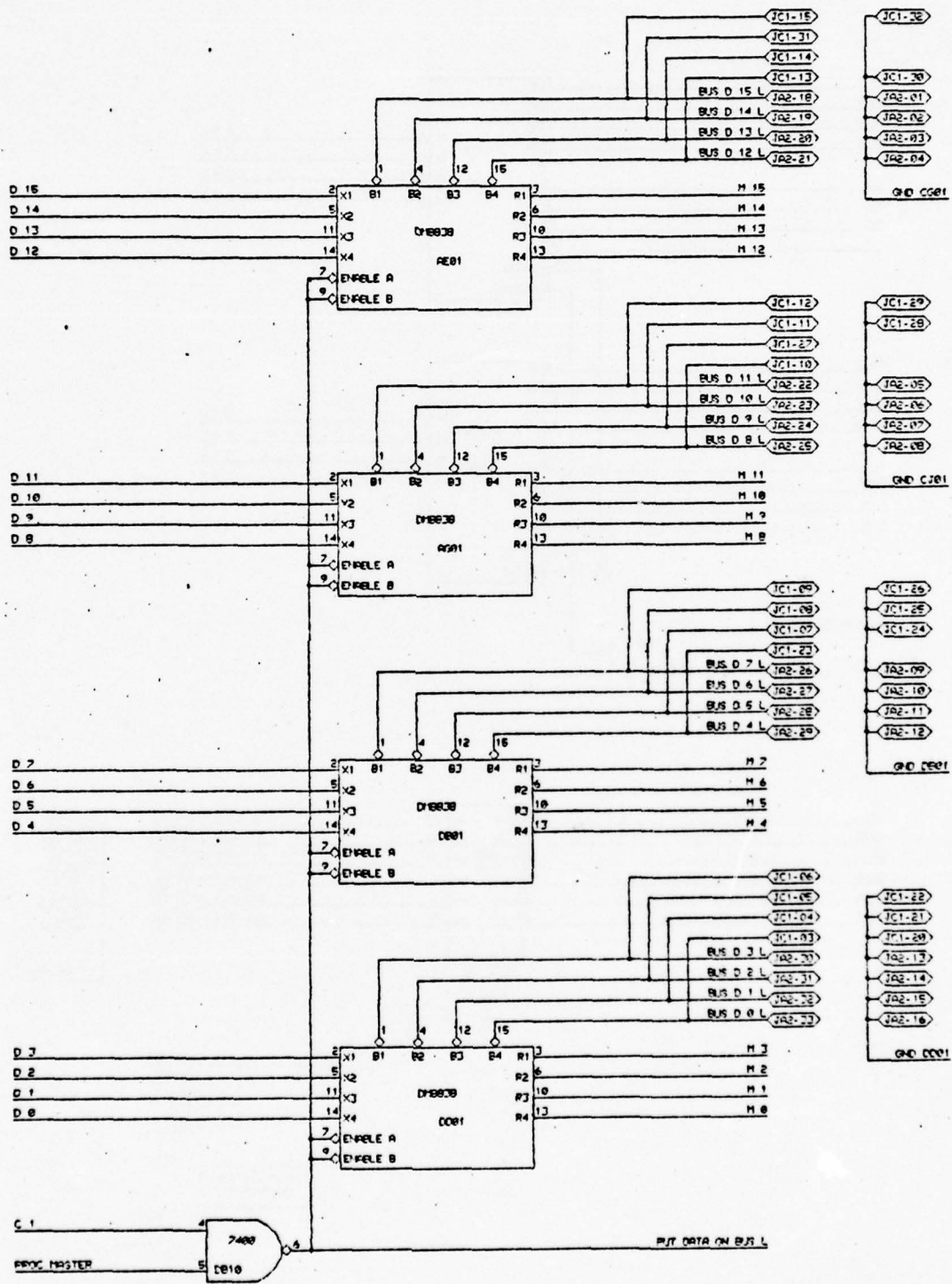
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PROJECT:			
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DATE:		PAGE:	
19-MAY 5 21:36			
PITTSBURGH, PENNSYLVANIA			



COMPUTER SCIENCE ENGINEERING LAB			
TITLE:		UNIBUS ADDRESS	
PROJECT:		FDP-11 USING THE INTEL 3000 MICROPROCESSOR	
DESIGN BY:	SHERWOOD	CHECKED BY:	
DRAWING FILE:	UN1A00(N210TM05)	DRAWING NUMBER:	
		PAGE	OF
		DATE:	02-JUN-75 17:46

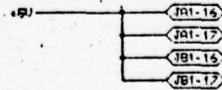
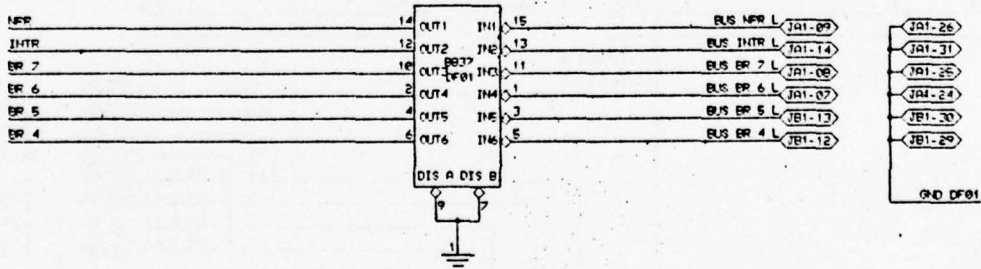
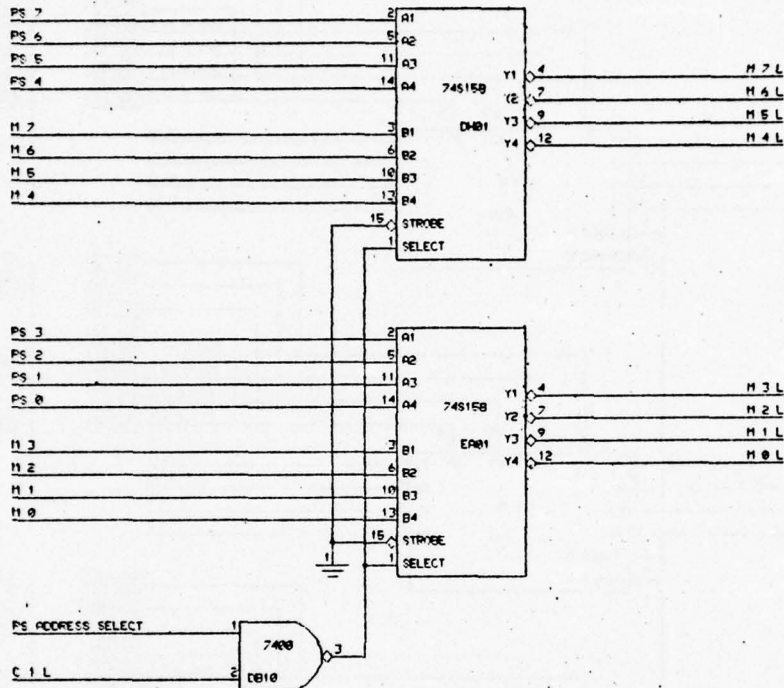


	COMPUTER SCIENCE ENGINEERING LAB	
	UNIBUS CONTROL LINE INTERFACE	
	PROJECT: PDP-11 USING THE INTEL 3000 MICROPROCESSOR	
	DESIGNED BY: SHERWOOD	CHECKED BY:
DATE: 02-JUN-75 18:00	DATE:	
CARNegie-MELLON UNIVERSITY		PITTSBURGH, PENNSYLVANIA

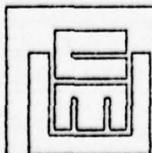


COMPUTER SCIENCE ENGINEERING LAB

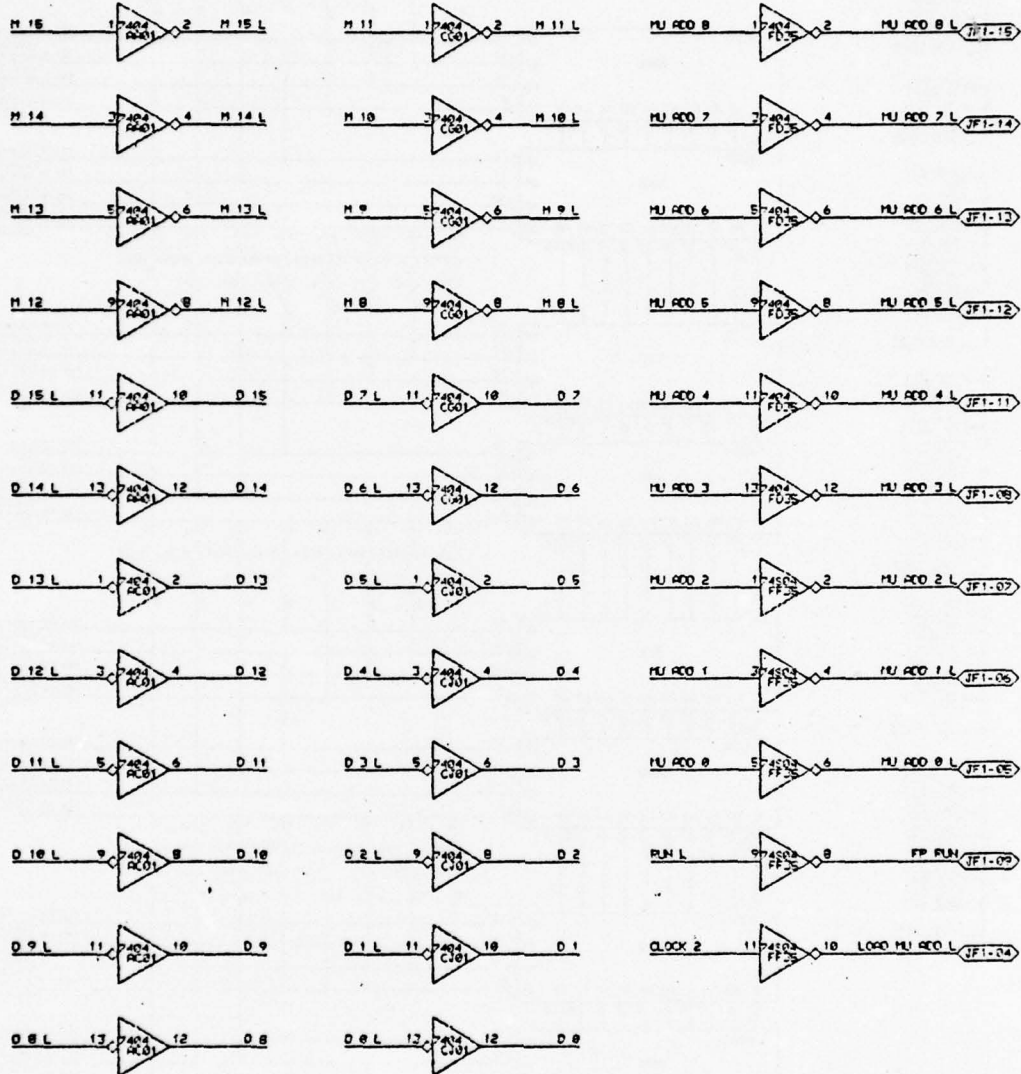
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PROJECT:	PDP-11 USING THE INTEL 3000 MICROPROCESSOR		
DESIGN BY:	SHERWOOD	CHECKED BY:	
DRAWING FILE:	UNIDAT(N210TM05)	DRAWING NUMBER:	
PAGE:		OF:	
DATE:	11-JUN-75 01:59		



POWER FOR BUS TERMINATOR

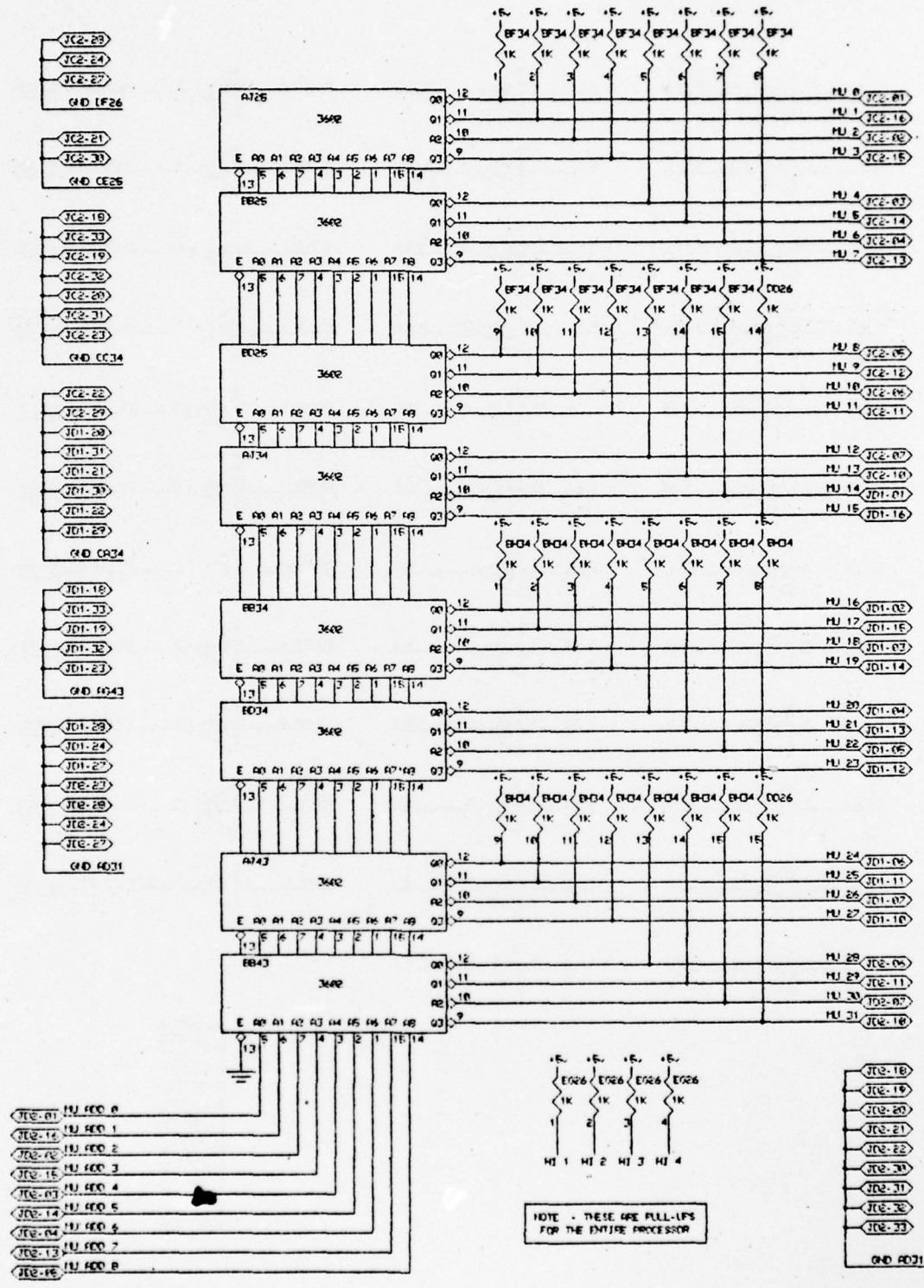


COMPUTER SCIENCE ENGINEERING LAB			
UNIBUS DATA INTERFACE			
PROJECT: FDP-11 USING THE INTEL 3000 MICROPROCESSOR			
DESIGNED BY:	SHERWOOD	CHECKED BY:	
DATE:	UNIFLUX [N210TM05]	CREATING NUMBER:	
		PAGE:	OF
		DATE:	02-JUN-75 18:06
<small>CARNEGIE-MELLON UNIVERSITY PITTSBURGH, PENNSYLVANIA 15213</small>			

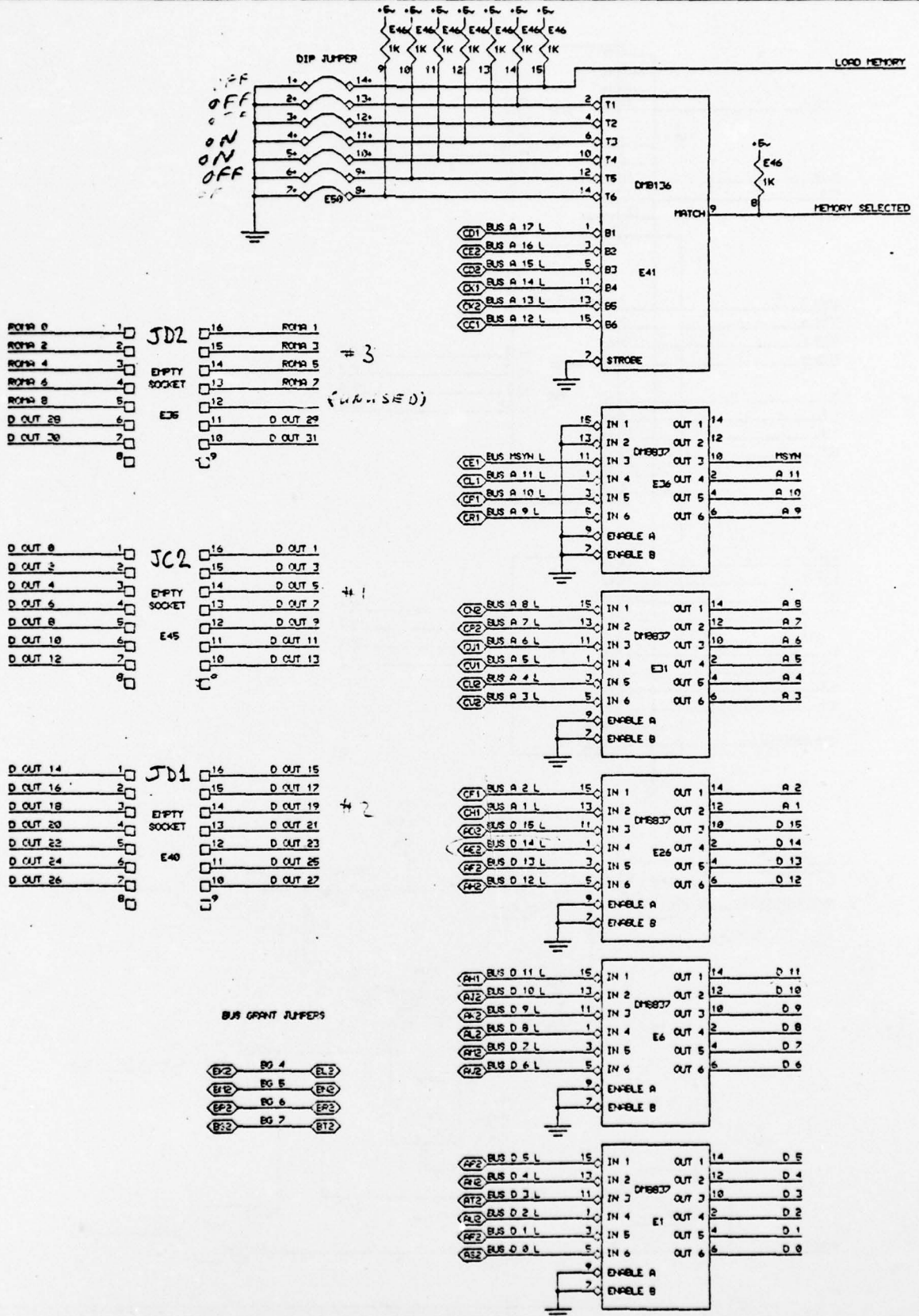


- JF1-20
 - JF1-22
 - JF1-24
 - JF1-25
 - JF1-26
 - JF1-28
 - JF1-29
 - JF1-30
 - JF1-32
- Q00 F03E

	COMPUTER SCIENCE ENGINEERING LAB		
	TITLE: INVERTERS FOR UNIBUS INTERFACE		
	PROJECT: PDP-11 USING THE INTEL 3000 MICROPROCESSOR		
	DRAWN BY: SHERWOOD	CHECKED BY:	PAGE OF
DRAWING FILE: UNIN(N210TM05)	DRAWING NUMBER:	DATE: 12-JUN-75 03:13	



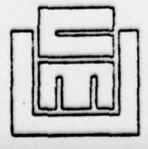
	COMPUTER SCIENCE ENGINEERING LAB	
	PROM CONTROL STORE	
	PDP-11 USING THE INTEL 3000 MICROPROCESSOR	
	DESIGNED BY: SHERWOOD	CHECKED BY:
	DATE: 10/11/75 CTLSTO(N210TM05)	DATE: 30-MAY-75 08:02 PITTSBURGH, PENNSYLVANIA 15213

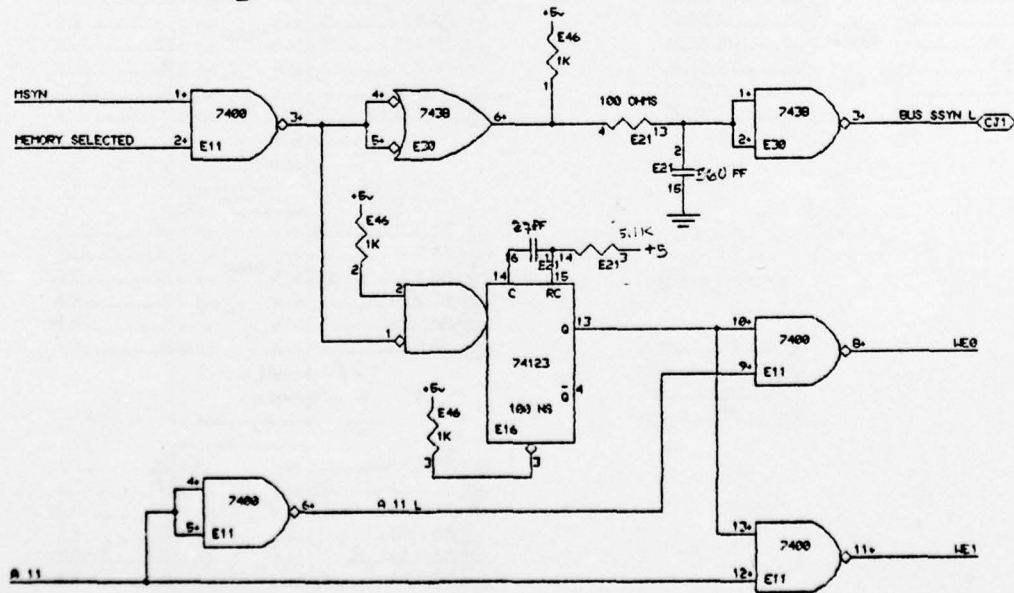
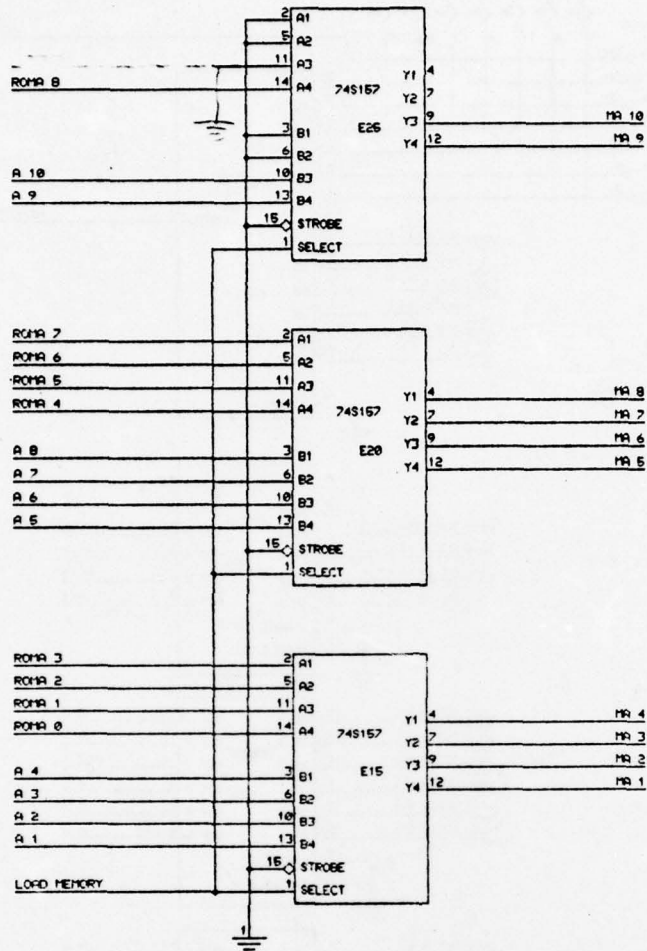


COMPUTER SCIENCE ENGINEERING LAB

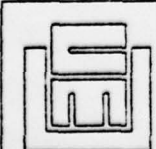
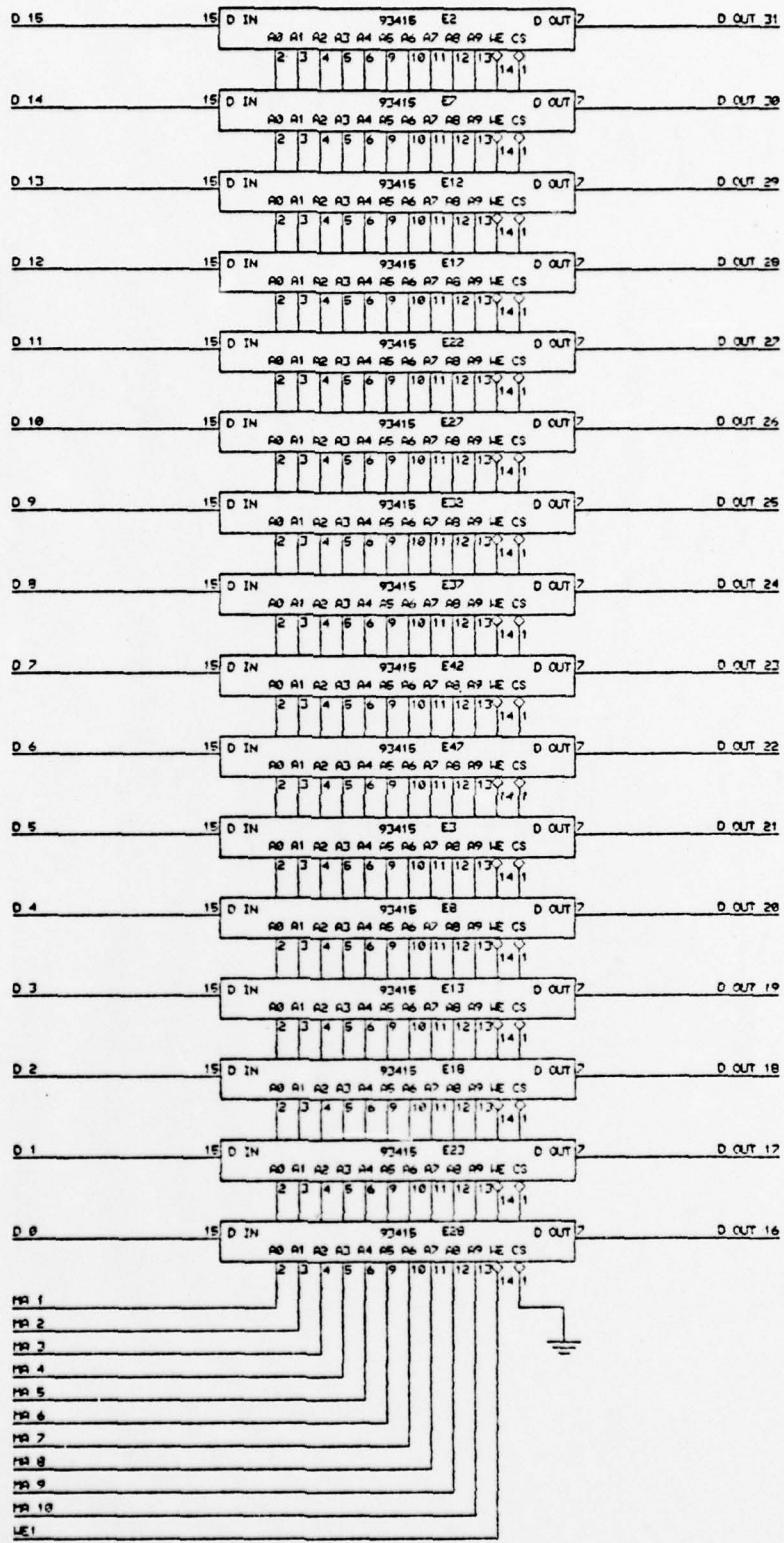
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 PROJECT: PDP-11 USING THE INTEL 3000 MICROPROCESSOR

DESIGNED BY: SHERWOOD CHECKED BY:
 DRAWING FILE: STORE J[N210WS03] CASSING NUMBER:
 DATE: 15-MAR-75 04:41





COMPUTER SCIENCE ENGINEERING LAB			
TITLE:			
PROJECT:			
DESIGN BY:	SHERWOOD	CHECKED BY:	
DATE:	11-MAR-75 03:52	LAB NUMBER:	
STORE 4 [N210WS03]		PITTSBURGH, PENNSYLVANIA 15261	



COMPUTER SCIENCE ENGINEERING LAB

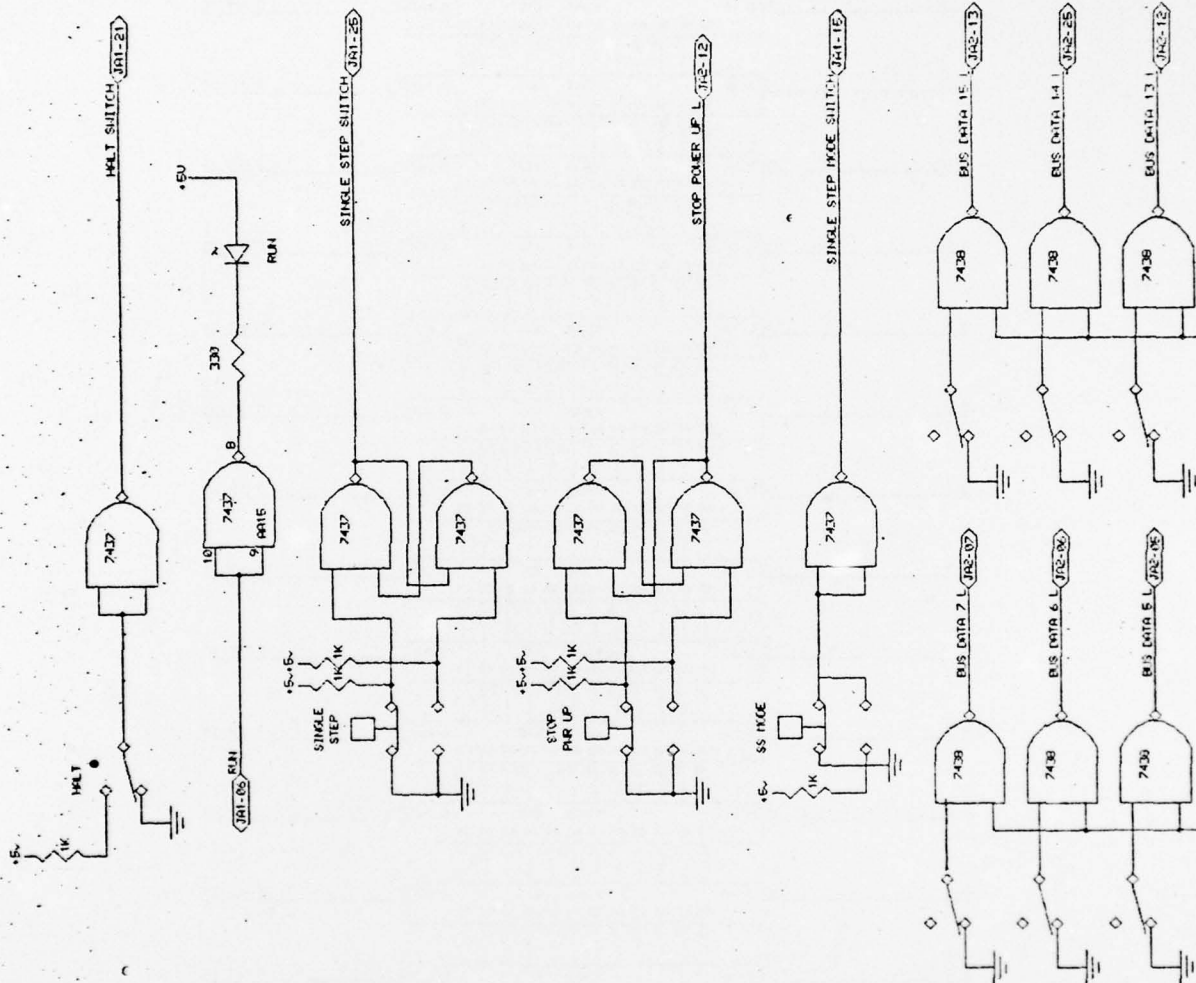
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 PROJECT: PDP-11 USING THE INTEL 3000 MICROPROCESSOR

DRAWN BY: SHERWOOD
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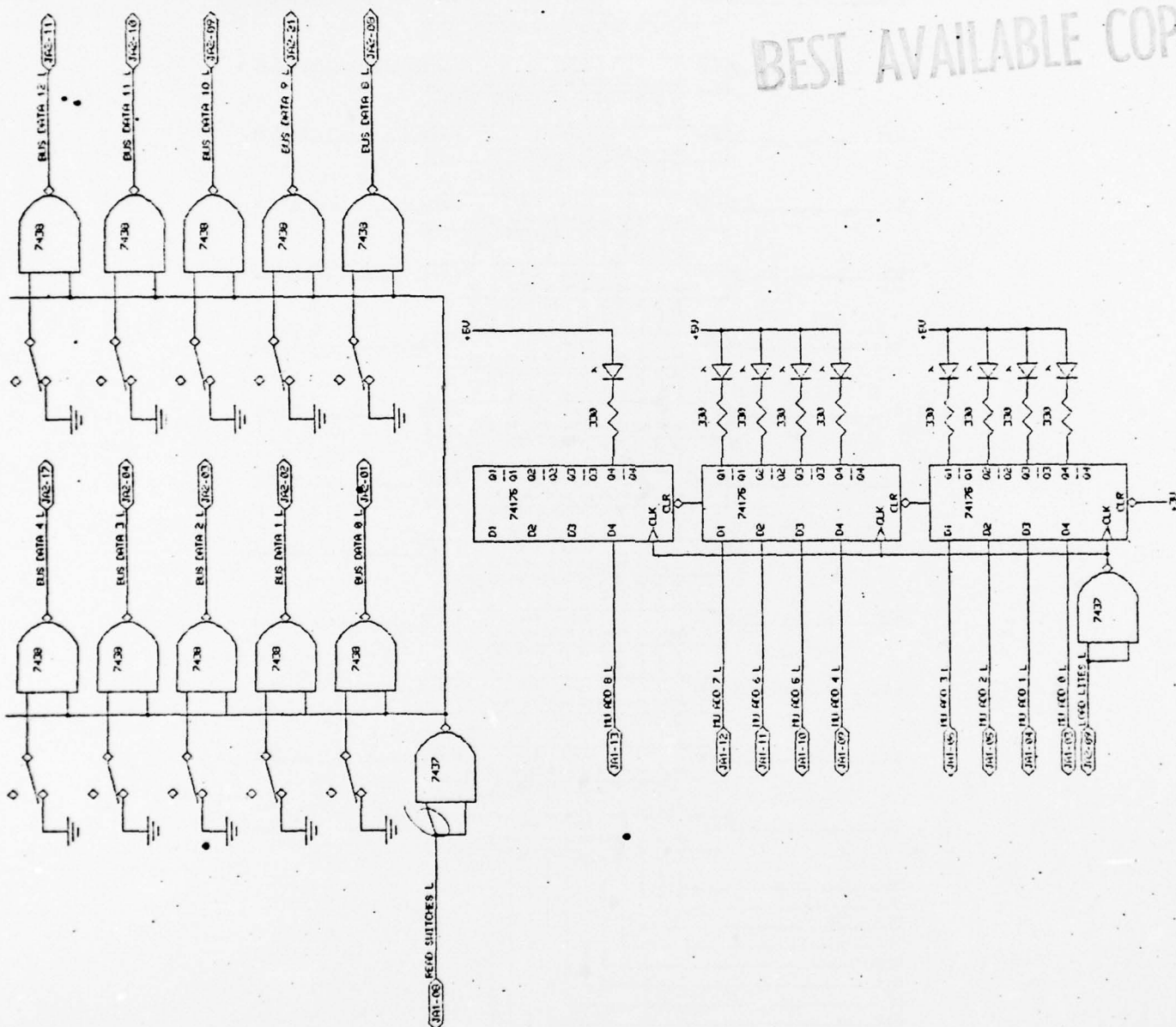
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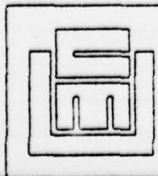
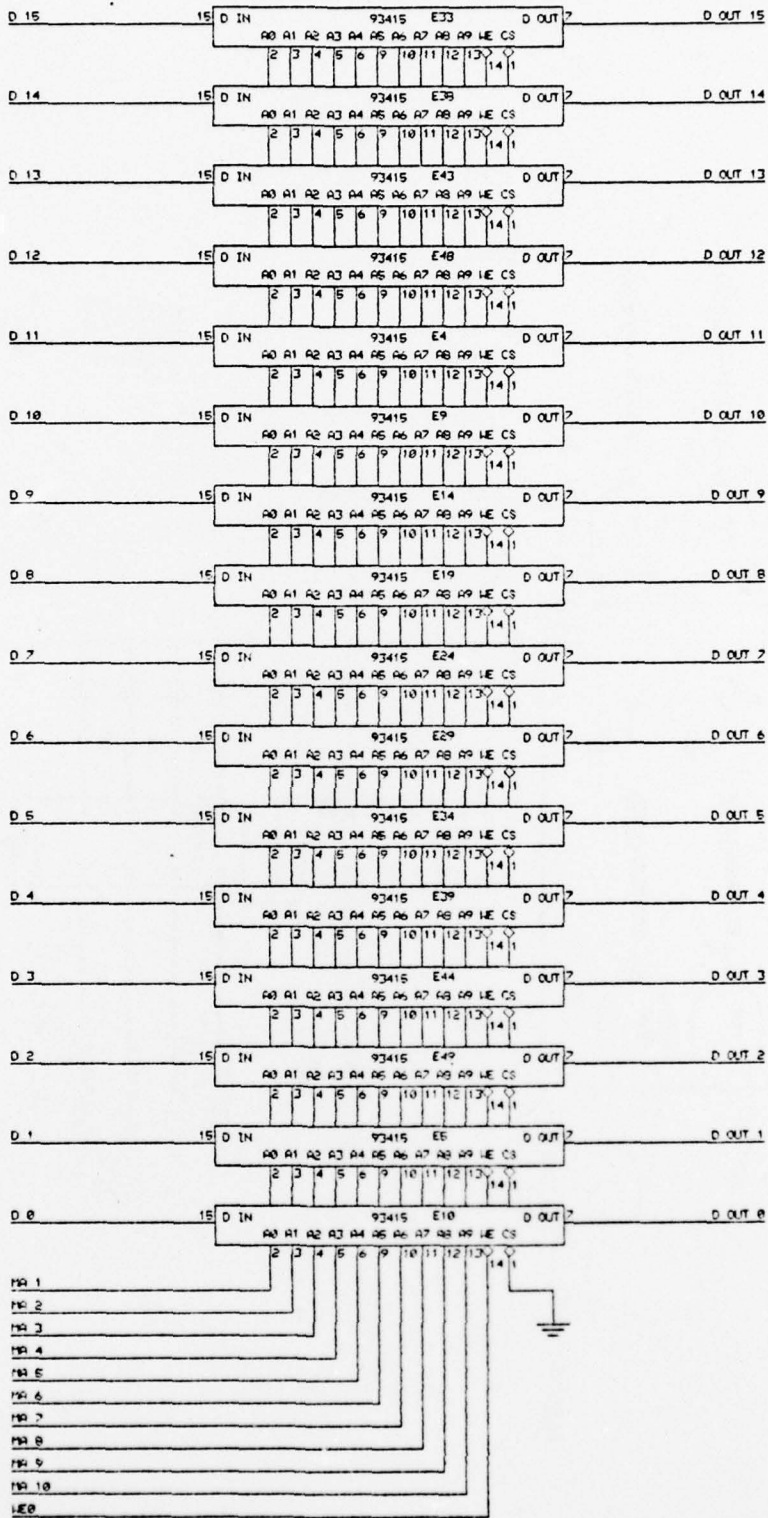
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	COMPUTER SCIENCE ENGINEERING LAB		
	TITLE: FRONT PANEL		
PROJECT:			
DESIGNED BY:	CREATED BY:	PAGE _____ OF _____	
DRAWING FILE: FRANEL(N210TM05)	DRAWING NUMBER:	DATE: 19-JUN-75 03:53	
CARNEGIE-MELLON UNIVERSITY		PITTSBURGH, PENNSYLVANIA 15213	



COMPUTER SCIENCE ENGINEERING LAB			
TITLE:		WRITEABLE CONTROL STORE	
PROJECT: PDF-11 USING THE INTEL 3000 MICROPROCESSOR			
DESIGN BY:	SHERWOOD	CREATED BY:	
ORIGINATING FILE:	STORE2[N210WS03]	ORIGINATING NUMBER:	
PAGE		OF	
DATE:		10-MAR-75 22:29	
PITTSBURGH, PENNSYLVANIA 15213			

ASSEMBLY OF MICRO.DAT ON 6-Jan-76 AT 10:48

ADDRESS JMCD OPCD CYCD PLA KURGMULTF
0000000 0011111 1111 122 2 22 22222333
1234567 8901234 5678 901 2 34 56789012

MICRO CODE TO MAKE A PDP-11/40 OUT OF THE INTEL 3800
MICRO PROCESSOR CHIPS.

PROGRAMMING CONVENTIONS USED IN CODE:

- 1. ZERO IS KEPT IN R9 SO THAT TRAP ADDRESSES CAN EASILY BE PUT IN IT TO CALL THE TRAP SEQUENCE. THE TRAP SEQUENCE PUTS ZERO BACK IN R9 WHEN IT IS DONE.
2. THE Z BIT IS USED TO DETECT DOUBLE BUS ERRORS AND TO INDICATE THAT THE PROCESSOR IS IN CONSOLE MODE. IF IT IS SET AND A TRAP OCCURS, THE MICROPROCESSOR WILL JUMP TO THE CONSOLE CODE.

FIELD PLA 3,0:PLA1=1,PLA2=2,PLA3=3,PLA4=4,PLA5=5,PLA6=6,PLA7=7,&
NINST=0,INTSR=2,DECR=3,INCR=4,BUSWT=5,BREST=6,STKOV=7,&
WIF1B=4,WIF13=2

FIELD KUB 1,1:KA1=0,KL1=0 ;NOTE: ALL K LINES ARE INVERTED.
FIELD PG12 2,3:PG1=2,PG2=0,PGD=1,KM00=3,KM01=2,KM10=1,KM11=0,&
KTY=2,SETS1=2,SETD1=1,&
SCLR1=1,STST1=1,SCM1=1,SINC1=1,SDEC1=2,SMEG1=0,&
SASR1=3,SASL1=3,SPDR1=3,SPOL1=3,SADC1=1,SSBC1=2,&
SMOV1=1,SBIT1=1,SBSC1=1,SKOR1=1,SSXT1=1,SCMP1=0,&
SSUB1=0,SADD1=0,SSWB1=3,&
PSVS=1,PSVN=2

MICRO WORD FOR I/O INSTRUCTIONS IS (8 BITS):
EXTENDED INSTRUCTION GET BUS (ASSERTED LOW), PAUSE, CHECK WORD, C(1:0), 11B

FIELD MULTF 8,1000011B:EINS=11000011B,EGPD=10110011B,EGWD=10010011B,&
EPWD1=11110011B,EWD1=11010011B,PAUSE=1100011B,EGPWT=10100011B,&
EGD1=10000011B,EPASE=11100011B,&
GPWD1=110011B,GPWDP=110111B,GPWDO=111011B,GPWDB=111111B,&
GPD1=100011B,GPD1P=100111B,GPDO=101011B,GPOB=101111B,&
GWD1=010011B,GWD1P=010111B,GWDO=011011B,GWDB=011111B,&
GDI=000011B,GDIP=000111B,GDO=001011B,GDOB=001111B,&
PWD1=1110011B,PWD1P=111011B,PWDO=111011B,PWDB=111111B,&
PDI=1100011B,PDIP=110011B,PDO=1101011B,PDOB=110111B,&
WDI=1010011B,WDIP=101011B,WDO=101011B,WDOB=101111B,&
DIP=1000011B,DIP=100011B,DO=1001011B,DOB=100111B,&
EDI=11000011B,EDIP=1100011B,EDO=11001011B,EDOB=11001111B,&
K0=11111101B,KR1=01B,KR2=101B,K1=11111001B,&
K2=11110101B,K4=1110101B,K7=11100001B,&
K10=11011101B,K14=11001101B,K17=11000001B,K20=1011101B,&
K21=10111001B,K24=10101101B,&
K30=10011101B,K34=10001101B,K35=10001001B,&
K40=01111101B,K57=01000001B,&
K60=111101B,K66=00100101B,K70=11101B,K71=00011001B,&
K77=01B,KCR=11001001B,KLF=11010101B,KPB=101B,&
KQM=01B,KZERO=00111101B,KSLSH=01000001B,&
KTKS=111101B,KTKB=110101B,KTP5=101101B,KTPB=100101B,&
SETS2=2,SETD2=2,&
SCLR2=0110110B,STST2=0110110B,SCM2=1010110B,&
SINC2=00000110B,SDEC2=00000110B,SMEG2=10000110B,&
SASR2=01001110B,SASL2=11000110B,SPDR2=01010110B,&
SPOL2=11010110B,SADC2=01010110B,SSBC2=10011110B,&
SMOV2=00101110B,SBIT2=00101110B,SBSC2=00101110B,&
SKOR2=00101110B,SSXT2=00100110B,SCMP2=10101110B,&
SSUB2=10101110B,SADD2=01101110B,SSWB2=10111110B,&
SETTT=00110010B,CLRTT=10110010B,SSWB3=00111010B,&
PSCS=01111110B,PSCN=00111110B,PSCIN=00010010B

PUT RESULT OF LAST INSTRUCTION IN MEMORY
AND FETCH NEXT INSTRUCTION.

Table with 4 columns: Address, Instruction, Comment, and Hex Value. Rows include instructions like WDSR, WDSRB, WDSW, and ODDAD.

```

;ODD ADDRESSING ERROR.
;
3 WDE0B: LDI AC,1,KAI ;3 ODD BYTE, SWAP HALVES /000B4/ 00000011 010010 010111 1111 000 0 11 01000011
2 WDE5B: NOP GP00B.JMP FETCH ;2 M(MAR)=AC, BYTE /000B5/ 00000010 010101 0001101 0011 000 1 11 00101111
;
;
11 FETCH: LMI R7,EGDI ; MAR=R(7) /000B8/ 00001011 010011 001011 0011 000 1 11 10000011
7 FFET: ADR R7,1,EINS ;7 R(7)=R(7)+1 /000B9/ 00000011 010110 011011 1111 000 1 11 11000011
359 AMA T,EPNDI ;547 T=INSTRUCTION /000C0/ 10110011 011110 0001010 0011 000 1 11 11110011
366 ADR R7,1,PLA1 ;556 WAIT FOR INSTRUCTION DECOD/000C1/ 10110110 0010101 011011 1111 001 1 11 01000011
350 LMI R7,0 STZ,PLA7,JMP 350 ;536 DO INITIAL DECODE /000C2/ 10101110 0010101 001011 0001 111 1 11 01000011
;
;ON INSTRUCTION BY USING THE
;MICRO INTERRUPT FEATURE.
;MAR=R7,Z=0
;
;-----;
;LOAD SOURCE OPERAND INTO T. FORMAT IS S5DD
;INSTRUCTION CLASS 1
;-----;
;REGISTER MODE=0: R(N)
;
80 SOP0: ILR R0,RG1,PLA2 ;120 AC=R(N) /00104/ 00101000 0111100 0000000 0011 010 1 10 01000011
92 NOP PLA4,JPX 64 ;132 /00105/ 00101110 1111000 0001101 0011 100 1 11 01000011
;
;REGISTER MODE=1: (R(N))+
;
81 SOP1: LMI R0,RG1,EGDI,INCR ;121 MAR=R(N), R(N)=R(N)+CONDIN/00109/ 00101001 0111011 0010000 0011 100 1 10 10000011
91 ILR R0,1,PG1,PLA2,JMP SRCHR ;R(N),AC=R(N)+1 /00110/ 00101101 0111101 0000000 1111 010 1 10 01000011
;
;REGISTER MODE=2: -(R(N))
;
82 SOP2: LMI R0,KAI,PG1 ;122 R(N)=R(N)-1 /00114/ 00101010 0011010 0010000 0011 000 0 10 01000011
418 LMI R0,KAI,PG1,EINS,DECR ;R(N)=R(N)-1+CONDECR /00115/ 11010010 0111101 0010000 0011 011 0 10 11000011
429 LMI R0,PG1,GDI,JMP SRCH1 ;MAR=R(N) /00116/ 11010110 0010100 0010000 0011 000 1 10 00000011
;
;REGISTER MODE=3: X(R(N))
;
83 SOP3: LMI P7,1,GMDI ;123 MAR=R(7), R(7)=R(7)+1, /00120/ 00101001 0111111 0010111 1111 000 1 11 00010011
95 ILR R7,1,WDI ;R(7)=R(7)+1 /00121/ 00101111 0010001 0000111 1111 000 1 11 01010011
287 ILR R0,PG1,WDI ;AC=R(N1) /00122/ 10001111 0111110 0000000 0011 000 1 10 01010011
286 AMA AC,KAI,PWDI ;AC=AC+M(MAR) /00123/ 10001110 0010100 0001011 0011 000 0 11 01110011
334 LMI AC,GDI ;MAR=AC /00124/ 10100110 0111101 0011101 0011 000 1 11 00000011
333 SRCH1: NOP PLA2,DI ;ALLOWS ADDR LINES TO SETTLE /00125/ 10100110 0000101 0001101 0011 010 1 11 01000011
93 SRCHR: LTM AC,KAI,POI,PLA4,JPX 64 ;135 AC=M(MAR) /00126/ 00101110 1111000 1011011 0011 100 0 11 01100011
;
65 SIRB: SDR T,1,KAI,PLA7,SETS1,SETS2,JPX 64 /00128/ 00100001 1111000 0101100 1111 111 0 10 00000010
;101 DO CALCULATE SECOND OPERAND
;PUT SOURCE OPERAND INTO T AND
;SET SOURCE SIGN BIT.
;
;INDIRECT BIT SET
;
66 SDEF: LMI AC,GDI ;102 MAR=AC /00135/ 00100010 0010000 0011101 0011 000 1 11 00000011
258 NOP DI ;NEEDED TO DO ADDRESSING /00136/ 10000010 0111110 0001101 0011 000 1 11 01000011
270 LTM AC,KAI,PLA3,POI /00137/ 10000110 0000101 1011011 0011 011 0 11 01100011
94 NOP PLA4,JPX 64 ;T=M(MAR) /00138/ 00101110 1111000 0001101 0011 100 1 11 01000011
;
67 SOBYS: LDI AC,1,KAI,PLA4,JMP SIRB ;103 AC=AC SWAPPED /00140/ 00100001 0110001 0101111 1111 100 0 11 01000011
;
;-----;
;LOAD DESTINATION'S ORIGINAL VALUE INTO AC IF USED ;
;IN INSTRUCTION.
;INSTRUCTION CLASS 2
;-----;
;REGISTER MODE=0: R(N)
;
68 DUSE0: ILR R0,PG2,JPX DU1RB ;104 AC=R(NZ) /00150/ 00100010 1111011 0000000 0011 000 1 00 01000011
;
;REGISTER MODE=1: (R(N))+
;
69 DUSE1: LMI R0,1,PG2,GDIP ;105 MAR=R(N), R(N)=R(N)+1, /00154/ 00100010 0011001 0010000 1111 000 1 00 00000111
405 ILR R0,PG2,EDIP,INCR ;R(N),AC=R(N)+CONDINCR /00155/ 11001010 0110110 0000000 0011 100 1 00 11000111
406 NOP PLA7,DIP,JMP DESHR /00156/ 11001010 0000111 0001101 0011 111 1 11 01000111
;
;REGISTER MODE=2: -(R(N))
;
70 DUSE2: LMI R0,KAI,PG2 ;106 R(N)=R(N)-1 /00160/ 00100010 0011011 0010000 0011 000 0 00 01000011
430 LMI R0,KAI,PG2,EINS,DECR ;666 R(N)=R(N)-1+CONDECR /00161/ 11011010 0010100 0010000 0011 011 0 00 11000011
326 LMI R0,PG2,GDIP,JMP DESM1 ;526 MAR=R(N) /00162/ 10100010 0011010 0010000 0011 000 1 00 00000111
;
;REGISTER MODE=3: X(R(N))
;
71 DUSE3: LMI P7,1,GMDI ;107 MAR=R(7), R(7)=R(7)+1 /00166/ 00100011 0010101 0010111 1111 000 1 11 00010011
343 ILR R7,1,WDI ;R(7)=R(7)+1 /00167/ 10101011 0110101 0000111 1111 000 1 11 01010011
341 ILR R0,PG2,WDI ;AC=R(NZ) /00168/ 10101010 0010110 0000000 0011 000 1 00 01010011
357 AMA AC,KAI,PWDI ;AC=AC+M(MAR) /00169/ 10110010 0110110 0001011 0011 000 0 11 01110011

```

```

350      LMI AC,GDIP          ;546 MAR=AC          /00170/ 101100110 0011010 0011101 0011 000 1 11 00000111
422 DESM1: NOP PLA7,DIP      ;ALLOWS ADDR LINES TO SETTLE /00171/ 110100110 0000111 0001101 0011 111 1 11 01000111
118 DESM2: LTM AC,KAI,WIF13,PDIP,JPX DU1RB ;166 AC=M(MAR) /00172/ 001110110 1111011 1011011 0011 010 0 11 01100111
;
112 DU1RB: NOP SETD1,SETD2,PLAS ;160 JUMP TO INSTRUCTIONS ADC. /00175/ 001110000 0101101 0001101 0011 101 1 01 00000010
13 DU1B1: NOP JPX ADC        ;15 /00176/ 000001101 1111001 0001101 0011 000 1 11 01000011
;
;INDIRECT BIT SET
;
113 DUDEF: NOP GDO           ;161 DIP MUST BE FOLLOWED BY A D/00180/ 001110001 0011000 0001101 0011 000 1 11 00001011
305      NOP /00181/ 110000001 0111011 0001101 0011 000 1 11 01000011
395      NOP PDD /00182/ 110001011 0000111 0001101 0011 000 1 11 01101011
123 DUDEF: LMI AC,GDIP,PLAS ;173 MAR=AC /00183/ 001111011 0111100 0011101 0011 110 1 11 00000111
124      LTM AC,KAI,PDIP,JPX DU1RB /00184/ 001111100 1111011 1011011 0011 000 0 11 01100111
;
114 DUOB: LDI AC,1,KAI,PLAS,JMP DU1B1 ;162 ODD BYTE /00186/ 001110010 0101101 0101111 1111 101 0 11 01000011
;
;-----;
;CALCULATE DESTINATION'S ADDRESS AND PUT IT IN MAR AND AC;
;INSTRUCTION CLASS 3
;-----;
;
;REGISTER MODE=0: R(N)
;
72 DA0:  ILR R0,RG2,JPX DU1RB ;110 AC=R(N) /00195/ 001001000 1111011 0000000 0011 000 1 00 01000011
;
;REGISTER MODE=1: (R(N))+
;
73 DA1:  ILR R0,RG2 /00199/ 001001001 0011100 0000000 0011 000 1 00 01000011
457     ADR R0,REG2,EINS,INCR ;R(N)=R(N)+CONDINCR /00200/ 111001001 0111111 0110000 0011 100 1 00 11000011
463     ADR R0,1,REG2,PLA7 ;R(N)=R(N)+1 /00201/ 111001111 0000111 0110000 1111 111 1 00 01000011
127 JDURB: LMI AC,JPX DU1RB ;177 MAR=AC /00202/ 001111111 1111011 0011101 0011 000 1 11 01000011
;
;REGISTER MODE=2: -(R(N))
;
74 DA2:  LMI R0,KAI,RG2 ;112 R(N)=R(N)-1 /00206/ 001001010 0000011 0010000 0011 000 0 00 01000011
58      LMI R0,KAI,RG2,EINS,DECR ;R(N)=R(N)-1+CONDECR /00207/ 000111010 0111111 0010000 0011 011 0 00 11000011
63      ILR R0,RG2,PLA7,JMP JDURB ;AC=R(N) /00208/ 000111111 0000111 0000000 0011 111 1 00 01000011
;
;REGISTER MODE=3: X(R(N))
;
75 DA3:  LMI R7,1,GDOI ;113 MAR=R(7), R(7)=R(7)+1. /00212/ 001001011 0000010 0010111 1111 000 1 11 00010011
43      ADR R7,1,GDOI ;R(7)=R(7)+1 /00213/ 000101011 0111100 0110111 1111 000 1 11 01010011
44      ILR R0,RG2,GDOI ;AC=R(N2) /00214/ 000101100 0111111 0000000 0011 000 1 00 01010011
47      AMA AC,KAI,PLA7,PMOI,JMP JDURB ;AC=AC+M(MAR) /00215/ 000101111 0000111 0001011 0011 111 0 11 01110011
;
116 DA1RB: NOP SETD1,SETD2,PLAS ;164 /00217/ 001110100 0101001 0001101 0011 101 1 01 00000010
9        NOP JPX SXT ;JUMP TO INSTRUCTIONS SXT, ... /00218/ 000001001 1111010 0001101 0011 000 1 11 01000011
;
;INDIRECT BIT SET
;
117 DADEF: AMA AC,GPMOI ;165 /00222/ 001110101 0111110 0001011 0011 000 1 11 00110011
126 DADEF: LMI AC,JMP DA1RB ;MAR=AC /00223/ 001111110 0110100 0011101 0011 000 1 11 01000011
;
;-----;
;LOAD SOURCE OPERAND INTO AC. FORMAT IS SS;
;INSTRUCTION CLASS 5
;-----;
;
;REGISTER MODE=0: R(N)
;
76 LSOP0: ILR R0,RG2,JPX DU1RB ;114 AC=R(N) /00232/ 001001100 1111011 0000000 0011 000 1 00 01000011
;
;REGISTER MODE=1: (R(N))+
;
77 LSOP1: LMI R0,RG2,EGDI,INCR ;115 MAR=R(N), R(N)=R(N)+CONDIN /00236/ 001001101 0000111 0010000 0011 100 1 00 10000011
125     ILR R0,1,RG2,DI,PLA7,JMP LSOP1 ;R(N),AC=R(N)+1 /00237/ 001111101 0110111 0000000 1111 111 1 00 01000011
;
;REGISTER MODE=2: -(R(N))
;
78 LSOP2: LMI R0,KAI,RG2 ;116 R(N)=R(N)-1 /00241/ 001001110 0010011 0010000 0011 000 0 00 01000011
318     LMI R0,KAI,RG2,EINS,DECR ;R(N)=R(N)-1+CONDECR /00242/ 100111110 0011101 0010000 0011 011 0 00 11000011
478     LMI R0,RG2,GDI,JMP LSOP1 ;MAR=R(N) /00243/ 111011110 0110111 0010000 0011 000 1 00 00000011
;
;REGISTER MODE=3: X(R(N))
;
79 LSOP3: LMI R7,1,GDOI ;117 MAR=R(7), R(7)=R(7)+1. /00247/ 001001111 0010110 0010111 1111 000 1 11 00010011
367     ILR R7,1,GDOI ;R(7)=R(7)+1 /00248/ 101101111 0111101 0000111 1111 000 1 11 01010011
365     ILR R0,RG2,GDOI ;AC=R(N2) /00249/ 101101101 0011000 0000000 0011 000 1 00 01010011
397     AMA AC,PMOI,KAI ;AC=AC+M(MAR) /00250/ 110001101 0110111 0001011 0011 000 0 11 01110011
391     LMI AC,GDI ;MAR=AC /00251/ 110001111 0011101 0011101 0011 000 1 11 00000011
471 LSOP1: NOP PLA7 ;ADDR LINES SETTLE /00252/ 111010111 0000111 0001101 0011 111 1 11 01000011
119 LSOP1: LTM AC,KAI,WIF13,PDIP,JPX DU1RB ;167 AC=M(MAR) /00253/ 001110111 1111011 1011011 0011 010 0 11 01100011
;
120 LS1PB: NOP SETD1,SETD2,PLAS ;170 JUMP TO INSTRUCTIONS TST. /00255/ 001111000 0101100 0001101 0011 101 1 01 00000010
12 LS1B1: LMI R7,JPX TST ;14 MAR=PC /00256/ 000001100 1111011 0010111 0011 000 1 11 01000011
;

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INDIRECT BIT SET

121	LSDEF:	LMI AC,GDI	:171 MAR=AC	/00260/	001111001 0110011 0011101 0011 000 1 11 00000011
115		NOP DI,PLAG	:ADDR LINES SETTLE	/00261/	001110011 0000110 0001101 0011 110 1 11 01000011
99		LTM AC,KAI,POI,JPX,DUIPB		/00262/	001100011 1111011 1011011 0011 000 0 11 01100011
122	LSOB:	LOI AC,I,KAI,PLAS,JMP,LSIBI	:172 ODD BYTE - SWAP AC	/00264/	001111010 0101100 0101111 1111 101 0 11 01000011

 TRAP DEFINITIONS START HERE

:PUSH PS ON STACK
 :R9 CONTAINS TRAP ADDRESS
 :R8 IS USED TO HOLD THE ADDRESS OF THE PSM
 :IF Z BIT IS SET, JUMP TO CONSOLE CODE.
 :
 :JUMP HERE ON ODD ADDRESS AND SSYN TIME OUT

248	BETRP:	LMI R9,K4	:370 TRAP TO LOC 4	/00278/	011111000 0111101 0011001 0011 000 1 11 11101101
253		SDR R8,I STZ,CLR,T,JZF,GRP1,DBERR	:DBERR	/00279/	011111101 1011111 0101000 1101 000 1 11 10110010
			:R8=0, TEST AND SET Z BIT		
			:CLEAR TRACE TRAP F.F.		

:JUMP HERE FOR ALL OTHER TRAPS

10	GTRAP:	ANR R8,0 STZ,CLRTT	:12 R8=0,Z=0,CLEAR TRACE TRAP F	/00285/	000001010 0001111 1001000 0001 000 1 11 10110010
250	GTRP1:	LMI R8,KL1,KM11,KNZ	:372 R8=MAR=17776	/00286/	011111010 0000010 0011000 0011 000 0 00 00000101
42		AMA AC,GWDI	:412 AC=M(17776)	/00287/	000101010 0111000 0001011 0011 000 1 11 00110011
40		LMI R6,KL1,KM11,KNZ	:400 R6=R6-2	/00288/	000101000 0011100 0010110 0011 000 0 00 00000101
456		LMI R6,EINS,STKOV	:401 MAR=R6	/00289/	111001000 0011110 0010110 0011 111 1 11 11000011
400		NOP	:403 WAIT FOR RED ZONE STACK :OVERFLOW MICRO INTERRUPT	/00290/	111101000 0011111 0001101 0011 000 1 11 01000011
504		NOP GWDD	:404 WAIT FOR TRAP	/00292/	111111000 0111101 0001101 0011 000 1 11 00011011
509		NOP PWDD	: M(R6)=PS	/00293/	111111101 0110101 0001101 0011 000 1 11 01111011

:PUSH PC ON STACK

501		LMI R6,KL1,KM11,KNZ	:405 R6=R6-2	/00297/	111110101 0110000 0010110 0011 000 0 00 00000101
456		LMI R6,EINS,STKOV	:406 MAR=R6	/00298/	111110000 0010011 0010110 0011 111 1 11 11000011
304		NOP	:407 WAIT FOR RED ZONE STACK :OVERFLOW MICRO INTERRUPT.	/00299/	100110000 0110110 0001101 0011 000 1 11 01000011
310	TSVPC:	ILR R7,GWDD	:667 M(R6)=PC	/00301/	100110110 0010000 0000111 0011 000 1 11 00011011
262		NOP PWDD	:662 WAIT FOR BUS	/00302/	100000110 0110100 0001101 0011 000 1 11 01111011

:PICK UP NEW PC
 :POWER FAIL TRAP ENTERS HERE

260	PFTRP:	LMI R9,I,GWDI	:404 MAR=R9,RS=R9+1	/00307/	100000100 0110111 0011001 1111 000 1 11 00010011
263		ADR R9,I,WDI	:RS=R9+1	/00308/	100000111 0111111 0111001 1111 000 1 11 01010011
271		AMA AC,PWDI	:AC=M(MAR)	/00309/	100001111 0001101 0001011 0011 000 1 11 01110011
223		SDR R7,I,KAI	:R7=AC	/00310/	011011111 0001001 0100111 1111 000 0 11 01000011

:PICK UP NEW PS

159		LMI R9,GWDI	:MAR=R9	/00314/	010011111 0111110 0011001 0011 000 1 11 00010011
150		AMA AC,PWDI	:AC=NEW PS	/00315/	010011110 0010010 0001011 0011 000 1 11 01110011
302		LMI R8,GWDD	:MAR=PSW	/00316/	100101110 0010111 0011000 0011 000 1 11 00011011
302		SDR R9,I,PWDD,JMP,FETCH	:PS=0; SET PSW	/00317/	101111110 0101011 0101001 1111 000 1 11 01111011

:DOUBLE BUS ERROR WHEN DOING A TRAP, OR BUS
 :ERROR WHEN IN CONSOLE MODE.

251	DBERR:	ANR R9		/00322/	011111011 0111110 1001001 0011 000 1 11 01000011
254		LMI R9,KTPS,KL1,KTY	:373 MAR=PUNCH STATUS REG :OUTPUT A "?" AND JUMP TO :CONSOLE.	/00323/	011111110 0001110 0011001 0011 000 0 10 00101101

230	OUTOM:	AMA AC,GWDI,JFL,TSTOM,OMRDY	:PUNCH READY	/00326/	011101110 1001110 0001011 0011 000 1 11 00110011
234	TSTOM:	TZR AC,KM10,K0,JMP,OUTOM		/00327/	011101010 0111110 1011101 0011 000 1 01 11111101
235	OMRDY:	ANR AC		/00328/	011101011 0110111 0011101 0011 000 1 11 01000011
231		LMI AC,KOM	:AC="?"	/00329/	011100111 0111100 0011101 0011 000 1 11 00000001
236		LMI R9,KTPB,KL1,KTY	:MAR=PUNCH	/00330/	011101100 0111101 0011001 0011 000 0 10 00100101
237		ANR R9,GWDD,JMP,CONSL	:OUTPUT BUFFER	/00331/	011101101 0101110 1001001 0011 000 1 11 00111011

 INSTRUCTION DEFINITIONS START HERE

:SPECIAL CODE TO MAKE MOV, CMP, ADD, AND SUB RR MODE GO FAST

04	MOVRR:	ILR R0,RG1	:AC=5	/00342/	001010100 0011000 0000000 0011 000 1 10 01000011
000		NOP SMOV1,SMOV2,JMP,WDESR	:MAR=PC,SET PSW	/00343/	110000100 0000000 0001101 0011 000 1 01 00101101
05	CHPRR:	ILR R0,RG2,EGWDI	:AC=0	/00345/	001010101 0011010 0000000 0011 000 1 00 10010011

```

421      CIA AC          ;AC=NOT AC          /00346/  110100101 0011100 0011111 0011 000 1 11 01000011
453      SDR T.1.KA1.SETD1.SETD2          ;T=AC          /00347/  111000101 0011101 0101100 1111 000 0 01 00000010
469      ILR R0.RG1          ;AC=S          /00348/  111010101 0111111 0000000 0011 000 1 10 01000011
479      NOP SETS1.SETS2          /00349/  111011111 0011001 0001101 0011 000 1 10 00000010
415      ILR T.1.KA1.SCMP1.SCMP2          ;AC=(NOT D)+S+1 /00350/  110011111 0111101 0001100 1111 000 0 00 10110110
413 TFFET:  NOP JMP FFET          ;PS TIME TO PROP /00351/  110011101 0100111 0001101 0011 000 1 11 01000011
;
86 ADDR:  ILR R0.RG1          ;AC=S          /00353/  001010110 0011100 0000000 0011 000 1 10 01000011
454      SDR T.1.KA1.SETS1.SETS2          ;T=AC          /00354/  111000110 0110100 0101100 1111 000 0 10 00000010
452      ILR R0.RG2          ;AC=D          /00355/  111000100 0011110 0000000 0011 000 1 00 01000011
484      NOP SETD1.SETD2          /00356/  111100100 0110110 0001101 0011 000 1 01 00000010
486      ILR T.KA1.SADD1.SADD2.JMP WDES R ;AC=S+D          /00357/  111100110 0100100 0001100 0011 000 0 00 01101110
;
87 SUBRR:  ILR R0.RG1          ;AC=S          /00359/  001010111 0010111 0000000 0011 000 1 10 01000011
375      CIA AC          ;AC=NOT AC          /00360/  101110111 0110110 0011111 0011 000 1 11 01000011
374      SDR T.1.KA1.SETS1.SETS2          ;T=AC          /00361/  101110110 0000010 0101100 1111 000 0 10 00000010
38      JLR R0.RG2          ;AC=D          /00362/  000100110 0110011 0000000 0011 000 1 00 01000011
35      NOP SETD1.SETD2          /00363/  000100011 0000011 0001101 0011 000 1 01 00000010
51      ILR T.1.KA1.SSUB1.SSUB2.JMP WDES R ;AC=D+(NOT S)+1 /00364/  000110011 0100100 0001100 1111 000 0 00 10110110
;
48 TST:   NOP STS1.STS2.JZR FETCH          ;D=D          /00366/  000110000 0101011 0001101 0011 000 1 01 01101110
;
50 BIT:   ANR T.KA1.EGWDI          ;T=T AND AC          /00368/  000110010 0111100 1001100 0011 000 0 11 10010011
60      ILR T.SBIT1.SBIT2.JZR FETCH          ;AC=T          /00369/  000111100 0101011 0001100 0011 000 1 01 00101110
;
104 HALT:  NOP JZR CONSL          /00371/  001101000 0101110 0001101 0011 000 1 11 01000011
;
105 WAIT:  NOP EGPWT.BUSWT          ;CAUSES BUS OWNERSHIP TO WAIT /00373/  001101001 0000010 0001101 0011 101 1 11 10100011
41      NOP JMP WAIT          ;FOR INTERRUPT. /00374/  000101001 0000110 0001101 0011 000 1 11 01000011
;
;POP PC OFF OF STACK
106 RTJ:   LMJ R6.1.GWDI          ;152 MAR=R6, R6=R6+1 /00377/  001101010 0000101 0010110 1111 000 1 11 00010011
90      ADR R6.1.WDI          ;132 R6=R6+1 /00378/  001011010 0111000 0110110 1111 000 1 11 01010011
88      AMA AC.PMDI          ;131 AC=M(MAR) /00379/  001011000 0001000 0001011 0011 000 1 11 01110011
136      SDR R7.1.KA1          ;130 R7=NEW PC /00380/  010001000 0110111 0001111 1111 000 0 11 01000011
;POP PS OFF OF STACK
135      LMJ R6.1.GWDI          ;127 MAR=R6, R6=R6+1 /00382/  010000111 0110110 0010110 1111 000 1 11 00010011
134      ADR R6.1.WDI          ;126 R6=R6+1 /00383/  010000110 0001001 0110110 1111 000 1 11 01010011
150      AMA AC.PMDI          ;125 AC=M(MAR) /00384/  010010110 0110111 0001011 0011 000 1 11 01110011
151      LMJ R9.KL1.KM11.KNZ          ;124 MAR=177776 /00385/  010010111 0111000 0011001 0011 000 0 00 00000101
152      SDR R9.1.GPMD0          ;144 R9=R, AND SET PSW /00386/  010011000 0001010 0101001 1111 000 1 11 00111011
160      NOP SETTT.JMP FETCH          ;151 SET TRACE TRAP F.F. IF RTI /00387/  010101000 0101011 0001101 0011 000 1 11 00110010
;
107 BPT:   LMI R9.K14.JZR GTRAP          ;DO TRAP TO LOC 14 /00389/  001101011 0101010 0011001 0011 000 1 11 11001101
;
108 IDT:   LMI R9.K20.JZR GTRAP          ;DO TRAP TO LOC 20 /00391/  001101100 0101010 0011001 0011 000 1 11 10111101
;
109 RESET:  NOP EPASE.BPES T.JZR FETCH          ;155 DO A RESET ON BUS /00393/  001101101 0101011 0001101 0011 110 1 11 11100011
;
110 RTT:   NOP JMP RTI          ;LOGIC ONLY SETS TRACE TRAP F.F. /00395/  001101110 0111010 0001101 0011 000 1 11 01000011
;IF RTI INSTRUCTION IN IR REG
;
102 MARK:  ILR T          ;AC=INST          /00398/  001100110 0010001 0001100 0011 000 1 11 01000011
278      JLR AC.KA1          ;INST=INST+2 /00399/  100010110 0110000 0001101 0011 000 0 11 01000011
272      TZR AC.KM01.K77          ;INST=INST AND 177 /00400/  100010000 0001110 1011101 0011 000 1 10 00000001
224      ADR R6.KA1          ;SP=SP+2*NN /00401/  011100000 0001101 0110110 0011 000 0 11 01000011
208      ILR R5          ;AC=R5          /00402/  011010000 0110001 0000101 0011 000 1 11 01000011
209      SDR R7.1.KA1          ;R7=R5          /00403/  011010001 0001110 0100111 1111 000 0 11 01000011
;POP OLD PS OFF OF STACK
225      LMJ R6.1.GWDI          ;MAR=R6, R6=R6+1 /00405/  011100001 0001011 0010110 1111 000 1 11 00010011
177      ADR R6.1.WDI          ;R6=R6+1 /00406/  010110001 0111101 0110110 1111 000 1 11 01010011
189      AMA AC.PMDI          ;AC=M(MAR) /00407/  010111101 0001001 0001011 0011 000 1 11 01110011
157      SDR R5.1.KA1.JZR FETCH          ;R5=AC          /00408/  010011101 0101011 0100101 1111 000 0 11 01000011
;
64 INV11:  LMI R9.K10.JZR GTRAP          ;1100 INVALID INSTRUCTION /00410/  001000000 0101010 0011001 0011 000 1 11 11011101
466 INV12:  LMI R9.K10.JZR GTRAP          ;TRAP TO LOC 10 /00411/  111010010 0101010 0011001 0011 000 1 11 11011101
111 INV13:  LMI R9.K10.JZR GTRAP          ;1157 /00412/  001101111 0101010 0011001 0011 000 1 11 11011101
;
97 YESBR:  ILR T          ;141 AC=T+INSTRUCTION /00414/  001100001 0010101 0001100 0011 000 1 11 01000011
417      TZR T.KM11.K77          ;T=T AND 377 /00415/  110100001 0110100 1011100 0011 000 1 00 00000001
420      TZR AC.KM10.K0          ;AC=GARBAGE, AC(7)=J /00416/  110100100 0011111 1011101 0011 000 1 00 11111101
500      SDR AC.JFL.BS100.BS101          ;AC=-J /00417/  111110100 1001100 0101101 0011 000 1 11 01000011
450 BS100:  SDR AC.J          ;702 AC=0, SIGN=0 /00418/  111000010 0110011 0101101 1111 000 1 11 01000011
451 BS101:  ILR T.KL1.K0          ;703 AC=SIGN EXTEND OFFSET /00419/  111000011 0110000 0001100 0011 000 0 11 11111101
448 BRNEG:  ILR AC.KA1          ;AC=OFFSET+2 /00420/  111000000 0110001 0001101 0011 000 0 11 01000011
449      ILR R7.KA1.JMP FETCH          ;R7=R7+OFFSET+2 /00421/  111000001 0101011 0000111 0011 000 0 11 01000011
;
96 NOBR:   NOP EGWDI.JMP FFET          ;NO BRANCH /00423/  001100000 0100111 0001101 0011 000 1 11 10010011
;
; EITHER SET OR CLR COND. CODES:
98 CL:     ILR T          ;142 AC=T (INSTRUCTION) /00426/  001100010 0011111 0001100 0011 000 1 11 01000011
498      TZR AC.K10          ;VALID INSTR TEST /00427/  111110010 0110011 1011101 0011 000 1 11 01111101
499      ILR T.JFL INV12.SECL0          ;RESTORE AC+T, JUMP ILLEGAL /00428/  111110011 1001101 0001100 0011 000 1 11 01000011
467 SECL0:  TZR AC.K17          ;AC=AC AND 17 /00429/  111010011 0110000 1011101 0011 000 1 11 11000001
464      TZR T.K20          ;TEST IF SET/CLR /00430/  111010000 0011110 1011100 0011 000 1 11 10111101
480      LMI R9.KL1.KM11.KNZ.JFL SECL1,SECL2 ;1740 MAR=177776 /00431/  111100000 1001110 0011001 0011 000 0 00 00000101
;
; CLEAR CC

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482 SECL1: CIA AC,GWDIP          :742 AC=NOT AC          /00434/ 111100010 0111001 0011111 0011 000 1 11 00010111
489 ANM AC,KAI,PWDIP,JMP SEZ    :442 AC=AC AND PS      /00435/ 111101001 0110101 1001011 0011 000 0 11 01110111
;
; SET CC
483 SECL2: ORM AC,KAI,GPWDP      :743 AC=AC OR PS      /00438/ 111100011 0110101 1101011 0011 000 0 11 00110111
485 SEZ: SDR R9.1,JMP WDESH      :443 563 R9=0         /00439/ 111100101 0100000 0101001 1111 000 1 11 01000011
;
100 ENT: LMI R9.K30,JZR GTRAP    :TRAP TO LOC 30       /00441/ 001100100 0101010 0011001 0011 000 1 11 10011101
;
101 TRAP: LMI R9.K34,JZR GTRAP   :145 TRAP TO LOC 34   /00443/ 001100101 0101010 0011001 0011 000 1 11 10001101
;
103 SOB: ILR R0.PG1              :147 AC=R(N)          /00445/ 001100111 0011001 0000000 0011 000 1 10 01000011
407 SDR R0.PG1.KAI              :627 R(N)=AC-1        /00446/ 110010111 0011111 0100000 0011 000 0 10 01000011
503 TZR R0.PG1.KAI              :622 R(N) ZERO?       /00447/ 111110111 0111110 1010000 0011 000 0 10 01000011
510 ILR T.JFL SOBPO.SOBP1        :462 AC=T...JUMP FOR ZERO /00448/ 111111110 1001010 0001100 0011 000 1 11 01000011
426 SOBPO: LMI R7.EGWDI,JMP FFET  :503 NO.CO TO FETCH   /00449/ 110101010 0100111 0010111 0011 000 1 11 10010011
427 SOBRI: TZR AC,KM90.K77       :502 AC=AC AND 77     /00450/ 110101011 0110000 1011101 0011 000 1 11 00000001
416 CIA AC.1,JMP BRNEG          :AC= -(AC)            /00451/ 110100000 0011100 0011111 1111 000 1 11 01000011
;
20 ROR: SRA AC,SPOR1,SPOR2.JPX 0 :DO A ROR              /00453/ 000010100 1111000 0001111 0011 000 1 11 01010110
;
21 ROL: ILR AC,KAI,SR0L1,SP0L2.JPX 0 :DO A ROL              /00455/ 000010101 1111000 0001101 0011 000 0 11 11010110
;
22 ASR: SRA AC,SASR1,SASR2.JPX 0 :26 DO A ASR           /00457/ 000010110 1111000 0001111 0011 000 1 11 01001110
;
23 ASL: ILR AC,KAI,SASL1,SASL2.JPX 0 :DO A ASL              /00459/ 000010111 1111000 0001101 0011 000 0 11 11000110
;
89 RTS: ILR R0.PG2              :AC=R(N)              /00461/ 001011001 0010111 0000000 0011 000 1 00 01000011
377 SDR R7.1,KAI                :R7=AC                /00462/ 101111001 0011000 0100111 1111 000 0 11 01000011
;POP TOP ELEMENT OFF OF STACK
393 LMI R6.1,GWDI                :MAR=R6,R6=R6+1      /00464/ 110001001 0011010 0010110 1111 000 1 11 00010011
425 ADR R6.1,WDI                :R6=R6+1              /00465/ 110101001 0111000 0110110 1111 000 1 11 01010011
424 AMA AC,PWDI                 :AC=M(MAR)            /00466/ 110101000 0110111 0001011 0011 000 1 11 01110011
423 SDR R0.1,KAI,PG2,JZR FETCH   :R(N)=AC              /00467/ 110100111 0101011 0100000 1111 000 0 00 01000011
;
19 SWAB: LDI AC.1,KAI,SSWB1,SSWB2 :AC=AC EXCHANGED     /00469/ 000010011 0101000 0101111 1111 000 0 11 10111110
8 NOP SSWB3.JPX 0              :TO FIX TIMING BUG   /00470/ 000001000 1111000 0001101 0011 000 1 11 00110100
;
18 COM: CIA AC,SCOM1,SCOM2.JPX 0 :D=NOT D              /00472/ 000010010 1111000 0011111 0011 000 1 01 10101110
;
26 INC: ILR AC.1,SINC1,SINC2.JPX 0 :D=D+1                /00474/ 000011010 1111000 0001101 1111 000 1 01 00000110
;
27 DEC: SDR AC,KAI,SDEC1,SDEC2.JPX 0 :D=D-1                /00476/ 000011011 1111000 0101101 0011 000 0 10 00000110
;
28 NEG: CIA AC.1,SNEG1,SNEG2.JPX 0 :D=(NOT D)+1         /00478/ 000011100 1111000 0011111 1111 000 1 00 10000110
;
16 ADC: ILR AC,SADC1,SADC2.JPX 0 :HARDWARE HANDLES C IN /00480/ 000010000 1111000 0001101 0011 000 1 01 01010110
;
17 SBC: SDR AC,KAI,SSBC1,SSBC2.JPX 0 :HARDWARE HANDLES C IN /00482/ 000010001 1111000 0101101 0011 000 0 10 10011110
;
24 BIC: CIA T                    :S=NOT S              /00484/ 000011000 0000011 0011110 0011 000 1 11 01000011
56 ANR T,KAI,JMP RTWD           :T=(NOT S) AND D      /00485/ 000111000 0111001 1001100 0011 000 0 11 01000011
;
25 BIS: ORR T,KAI                :T=S OR D              /00487/ 000011001 0000011 1101100 0011 000 0 11 01000011
57 RTWD: ILR T,SBC51,SBC52.JPX 0 :AC=T                  /00488/ 000111001 1111000 0001100 0011 000 1 01 00101110
;
30 ADD: ILR T,KAI,SA0D1,SA0D2.JPX 0 :D=D+S                /00490/ 000011110 1111000 0001100 0011 000 0 00 01101110
;
31 SUB: SDR R0.1,KAI              :R0=AC-D              /00492/ 000011111 0010111 0101000 1111 000 0 11 01000011
383 ILR T                          :AC=T-S                /00493/ 101111111 0011000 0001100 0011 000 1 11 01000011
399 CIA AC                          :S=NOT S                /00494/ 110001111 0111110 0011111 0011 000 1 11 01000011
398 NOP SETS1,SETS2                /00495/ 110001110 0101111 0001101 0011 000 1 10 00000010
15 ILR R0.1,KAI,SSUB1,SSUB2.JPX 0 /00496/ 000001111 1111000 0001000 1111 000 0 00 10110110
;
29 XOR: SDR T.1,KAI              :T=AC                  /00498/ 000011101 0000011 0101100 1111 000 0 11 01000011
61 ILR R0.PG1                      :AC=R(N)              /00499/ 000111101 0111110 0000000 0011 000 1 10 01000011
62 XNP T,KAI                        :T=T XNOR AC          /00500/ 000111110 0000010 1111100 0011 000 0 11 01000011
46 ILR T                          :AC=T                  /00501/ 000101110 0111110 0001100 0011 000 1 11 01000011
45 CIA AC,SXOR1,SXOR2.JPX 0       :55 AC=NOT AC         /00502/ 000101101 1111000 0011111 0011 000 1 01 00101110
;
33 IJMP: SDR R7.1,KAI,JZR FETCH   :R(7)=D ADDRESS      /00504/ 000100001 0101011 0100111 1111 000 0 11 01000011
;
36 JSR: SDR T.1,KAI              :T=D ADDRESS, T IS TMP /00506/ 000100100 0010111 0101100 1111 000 0 11 01000011
372 ILR R0.PG1                      :AC=R(N)              /00507/ 101110100 0110101 0000000 0011 000 1 10 01000011
373 LMI R6.KM2,KL1,KM11           :R6=R6-2              /00508/ 101110101 0111000 0010110 0011 000 0 00 00000101
376 LMI R6.EINS,STKOV            :MAR=R(6)             /00509/ 101111000 0011000 0010110 0011 111 1 11 11000011
392 NOP                              :WAIT FOR RED ZONE STACK /00510/ 110001000 0111100 0001101 0011 000 1 11 01000011
;
396 NOP GWD0                        /00512/ 110001100 0011001 0001101 0011 000 1 11 00011011
412 NOP PHDD                        /00513/ 110011100 0011010 0001101 0011 000 1 11 01110111
428 LMI T                          :MAR=NEXT PC         /00514/ 110101100 0111110 0011100 0011 000 1 11 01000011
430 ILR R7.EGWDI                  :AC=R7                 /00515/ 110101110 0111111 0000111 0011 000 1 11 10010011
431 SDR R0.1,KAI,PG1              :R(N)=R7               /00516/ 110101111 0011011 0100000 1111 000 0 10 01000011
447 ILR T                          :AC=T(TMP)            /00517/ 110111111 0111110 0001100 0011 000 1 11 01000011
446 SDR R7.1,KAI,JMP FFET         :R7=TMP                /00518/ 110111110 0100111 0100111 1111 000 0 11 01000011
;
34 CLR: TZR AC,SCLR1,SCLR2.JPX 0   :42 D=0                /00520/ 000100010 1111000 1011101 0011 000 1 01 01101110
;

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20. ABSTRACT (Continue on reverse side if necessary and identify by block number) The CMU-11 is a microprogram- mable processor built with the Intel 3000 microcomputer set that emulates the PDP-11 architecture. In addition, it has been designed to provide full Unibus support. The enclosed documentation gives the details of the CMU-11 design. This documentation has been generated in conjunction with the Stanford Drawing System, the SAGE simulator, and the Intel 3000 microassembler. Those hoping to do any further development of the CMU-11 design are encouraged to also use these design aids and all of the CMU-11 design information shown here (and other in- formation such as ROM contents and wirelists) are available on magnetic tape. See the following report for an introductory discussion and evaluation of the (continued)		

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CMU-11:

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