Model Name: SOM-DB5830

ADVANTECH

Title: COVER		
Size	Document Number: SOM-DB5830	Rev: A3
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COM-Express Type 6 Rev. 3.1

SOM Module

LVDS1 (DF13) — 85ohm — *Default
eDP (DF13) — 85ohm — Optional
PCIE4x x4 Slot 0 — 85ohm — Port 0-3
PCIE4x x4 Slot 1 — 85ohm — Port 4-5 / Port 6-7 from Row C, D
LAN0 RJ-45 stack USB3.1 x 2 — 100ohm
USB 2.0 x 2 LAN0 stack USB3.1 Port 0-1 — 85ohm — Port 0-1
USB 2.0 x 2 Pair with USB3.1 Port 2-3 — 85ohm — Port 2-3
USB 2.0 x 4 QUADRUPLE STACKED Connector — 85ohm — Port 4-7
Audio Jack Line-in, Line-out, MIC
SPDIF
HD Audio Codec REALTEK ALC888S-VD2-GR — 50ohm
GPIO1 Pin Header 10P — 50ohm — *Default
SDIO1 microSD Conn. 8P — 50ohm — Function select by jumper / Optional
LPC1 Pin Header 6x2P — 50ohm — LPC/eSPI
VGA1 HDMI_19P + DSUB_15P — 50ohm
COM1 Box Header 5x2P — 50ohm — Port 0
COM2 Box Header 5x2P — 50ohm — *Default Port 1
CAN1 Box Header 5x2P — 50ohm — Optional
BIOS1 SPI Socket — 50ohm
BIOS1 Pin Header 7P — 50ohm
SATA Gen3 SATA Conn. 0 / SATA Conn. 1 / SATA Conn. 2 / SATA Conn. 3 — 85ohm — Port
SMBUS1 Wafer Box 4P — 50ohm
I2C1 Wafer Box 4P — 50ohm
EEPROM 2 Kbit (256 bytes)
Port 80

LVDS
PCIEX1 Port 0-5
LAN
USB 2.0 Port 0-7
HDA
GPIO
LPC /eSPI
CRT
Serial Port
SPI
SATA
SMBus
I2C

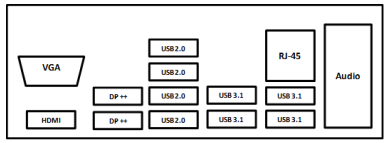
Connector Row A,B
Connector Row C,D

PCIEX16 — PCIE x16 x16 Slot 0 — 85ohm
PCIEX1 Port 6-7 — Port 6-7 / Port 4-5 from Row A, B — PCIE4x x4 Slot 1 — 85ohm
DDI[1:3] — DDI1 — Display Port DP Conn. 1 — 85ohm
DDI2 — Display Port DP Conn. 2 — 85ohm
DDI3 — 85ohm — DP to HDMI retimer TI_SN65DP159RGZT — 100ohm — HDMI Conn. HDMI_19P + DSUB_15P
USB 3.1 — 80ohm — COMe R3.0 only support USB 3.0.
Port 0-1 — USB3.1 10 Gbps Redriver ON_NB7NPQ7042MMUTWG — Port 0-1 — USB 3.1 x 2 LAN0 stack USB3.1 Port 0-1 — 80ohm
Port 2-3 — USB3.1 10 Gbps Redriver ON_NB7NPQ7042MMUTWG — Port 2-3 — USB 3.1 x 2 DUAL STACKED Connector — 80ohm

Smart Fan

SYS Fan1

Power/Reset/Sleep/LID Button,
WDTOUT LED, Thermal Alerm LED,
Battery low LED, Power Good Signal.



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Title: Block Diagram

Size: | Document Number: SOM-DB5830 | Rev: A3

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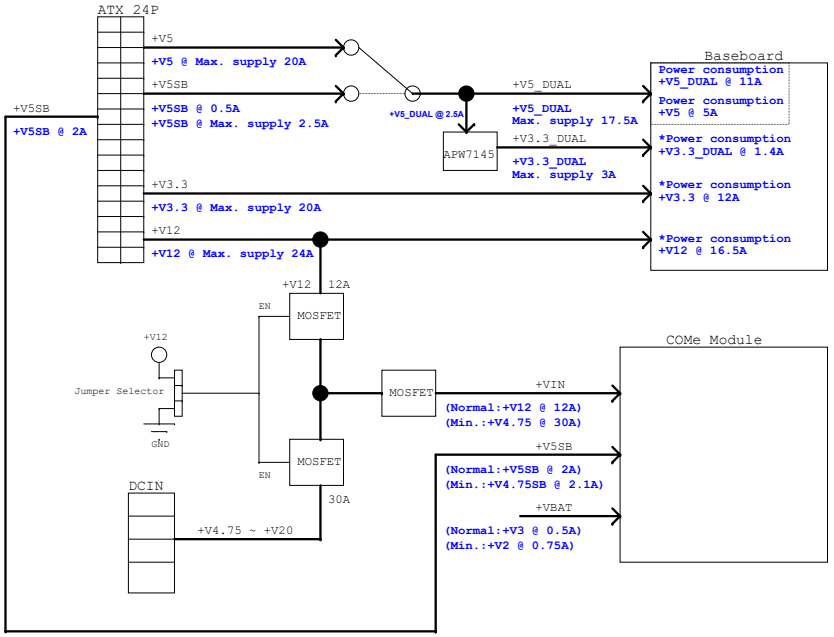

Table 57: PCIe Connector Power and Bulk Decoupling Requirements

Power Rail	PCIe x1, x4 or x8 Connector	PCIe x16 Connector
VCC_12V	2.1A @ 1000uF bulk	5.5A @ 2000uF bulk
VCC_3V3	3.0A @ 1000uF bulk	3.0A @ 1000uF bulk
VCC_3V3_SB	375mA @ 150uF bulk	375mA @ 150uF bulk

Table 7.2: Input Power - Pin-Out Type 6/7 Modules (Dual Connector, 440 pins)

Power Rail	Module Pin Current Capability (Amps)	Nominal Input (Volts)	Input Range (Volts)	Derated Input (Volts)	Max Input Ripple (mV)	Max Module Input Power (w. derated input) (Watts)	Assumed Conversion Efficiency	Max Load Power (Watts)
VCC_12V	12	12	11.4 - 12.6	11.4	+/-100	137	85%	116
VCC_5V_SBY	2	5	4.75 - 5.25	4.75	+/-50	9		
VCC_RTC	0.5	3	2 0 - 3.3		+/-20			

ATX12V Power Supply Design Guide

Table 4. Typical Power Distribution for a 300 W ATX12V Configuration

Output	Min. Current (amps)	Max. Current (amps)	Peak Current (amps)
+12 V1DC[1, 2]	1.0	8.0	10.0
+12 V2DC[1, 2]	1.0	14.0	
+5 VDC	0.3	20.0	
+3.3 VDC	0.5	20.0	
-12 VDC	0.0	0.3	
+5 VSB	0.0	2.0	2.5

Note: Total combined output of 3.3 V and 5 V is ≤ 120 W
Peak currents may last up to 17 seconds with not more than one occurrence per minute
[1]12V1DC and 12V2DC should have separate current limit circuits to meet 240VA safety requirements.
[2]12V2 supports processor power requirements and must have a separate current limit

LVDS PWR

+V12 → +V12 +VLVDS_PANEL_PWR 1A (40mils)
+V5 → +V5 +VLVDS_PANEL_PWR 1A (40mils)
+V3.3 → +V3.3 +VLVDS_PANEL_PWR 1A (40mils)

System FAN / Smart FAN

+V12 → 2.2 x2 = 4.4A 4.4A (176mils)

PCIE Slot

+V12 → +V12 PCIe X16 x1 + PCIe X4 x2 5.5A + (2.1A x2) = 9.7A (388mils)
+V3.3 → +V3.3 PCIe X16 x1 + PCIe X4 x2 3A + (3A x2) = 9A (360mils)
+V3.3_DUAL → +V3.3_DUAL PCIe X16 x1 + PCIe X4 x2 375mA + (375mA x2) = 1125mA (45mils)

BUZZER

+V5 → +V5 50mA (2mils)

ON_NCP45521IMNTWG-H

+V3.3 → +V3.3 1A (40mils)
+V3.3_SDIO ← +V3.3_SDIO 1A (40mils)

VGA

+V5 → +V5 1A (40mils)

ANPEC_APW7145KAI-TRG

+V5_DUAL → +V5_DUAL 2.5A (100mils)
+V3.3_DUAL ← +V3.3_DUAL 3 A (120mils)

REALTEK_ALC888S-VD2-GR

+V3.3 → +V3.3 20.47mA (0.82mils)
+V5_DUAL → +V5_DUAL 237mA (10mils)

USB3.0 x 4 port

+V5_DUAL → +V5_DUAL 900mA x4 = 3.6A (144mils)

USB2.0 x 8 port

+V5_DUAL → +V5_DUAL 500mA x8 = 4A (160mils)

PCIE Clock Buffer

+V3.3 → +V3.3 187mA (7.48mils)

SN65HVD251DR

+V5 → +V5 65mA (2.6mils)

ON_NB7NPQ7042MMUTXG

+V3.3_DUAL → +V3.3_DUAL 130mA x2 = 260mA (10.4mils)

LVDS INVERTER

+V5 → +V5 1A (40mils)
+V12 → +V12 1A (40mils)

MAXIM_MAX6958AAEE+

+V3.3 → +V3.3 275mA (11mils)

SMBUS Pin Header

+V3.3_DUAL → +V3.3_DUAL(pin Header) 80mA (3.2mils)

I2C Pin Header + ST_M24C02-RMN6TP

+V3.3_DUAL → +V3.3_DUAL(pin Header) 82mA (4mils)

(From Module) SPI Flash + Pin Header

+V3.3_DUAL ← +V3.3_DUAL 100mA (4mils)

HDMI retimer

+V3.3 → +V3.3 70mA (2.8mils)
+V1.1_DP159 → +V1.1_DP159 325mA (13mils)

HDMI Connector

+V5 → +V5 55mA (2.2mils)

DP Connector x2

+V3.3 → +V3.3 500mA x2 = 1A (40mils)

SP3243EUEY-L

+V5 → +V5 100mA (4mils)

ATX Connector

+V12 ← +V12 24A (960mils)
+V3.3 ← +V3.3 20A (800mils)
+V5 ← +V5 15A (600mils)
+V5SB ← +V5SB 2.5A (100mils)

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Title: Power Map
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COMe Rev. 3.0 PN:00A0000209

A201-1 : Change COMe symbol to rev 3.1

CN1A

+VIN(SOM A/B/C/D) total:
+V12 @ 12A
+V4.75 @ 30A

+V5SB@ 2A

1.TEST PAD TP28
PN: 0030000085

2.TEST PAD TP-10
PN: 0030000032

TRI_ETXE-BP_REV3.1_SOM-COM-E
<Characteristic>

Title	COMe R3.0 Type6 RAW A/B
Size	Document Number SOM-DB5830 Rev A3
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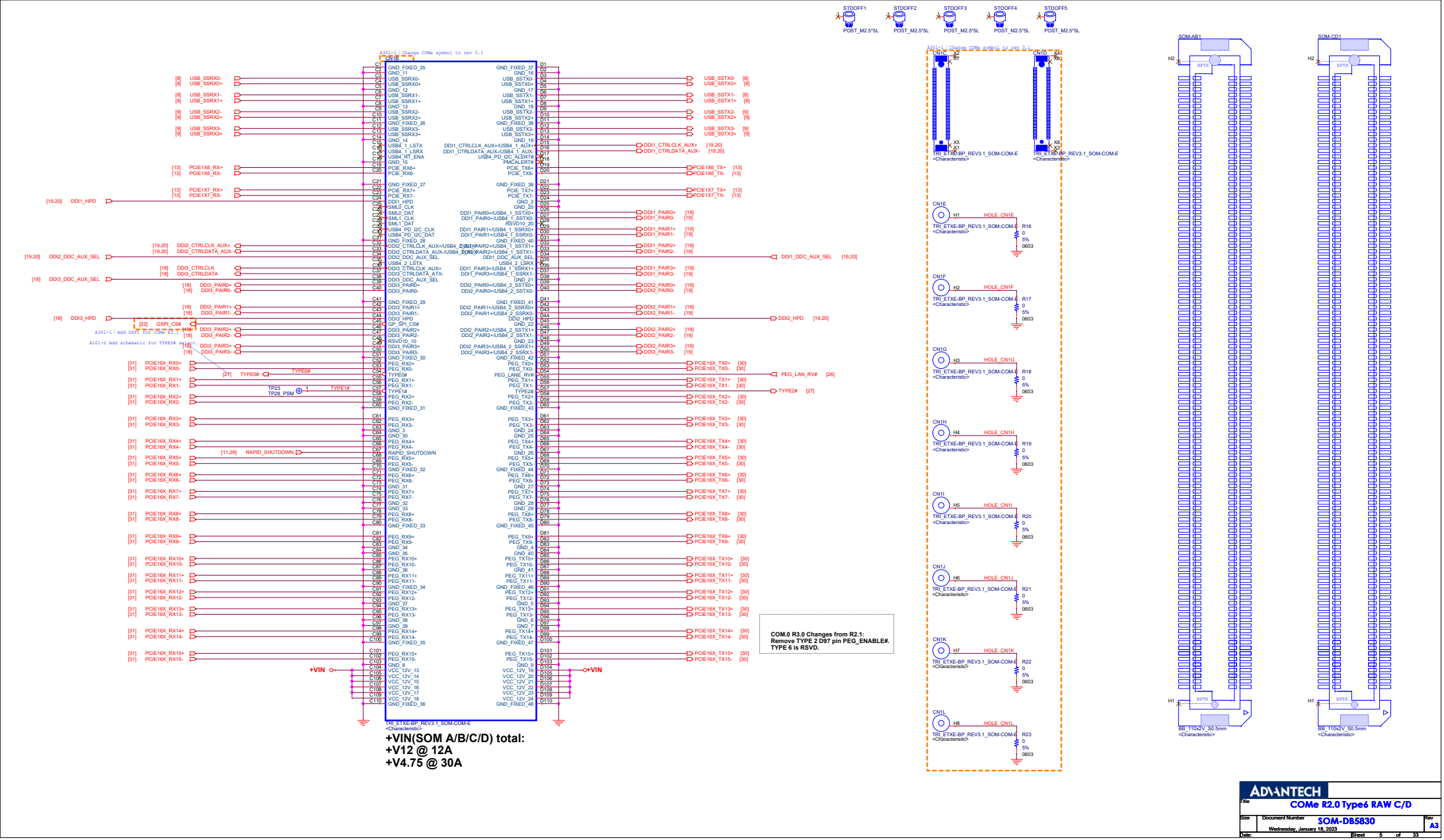
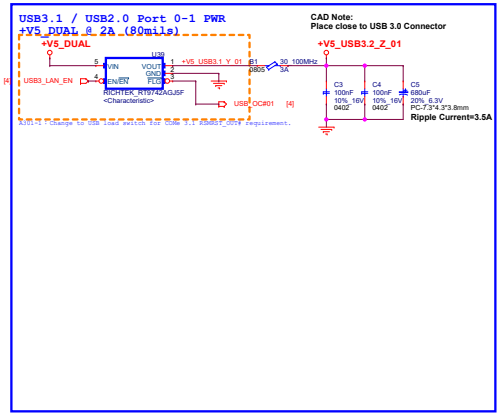
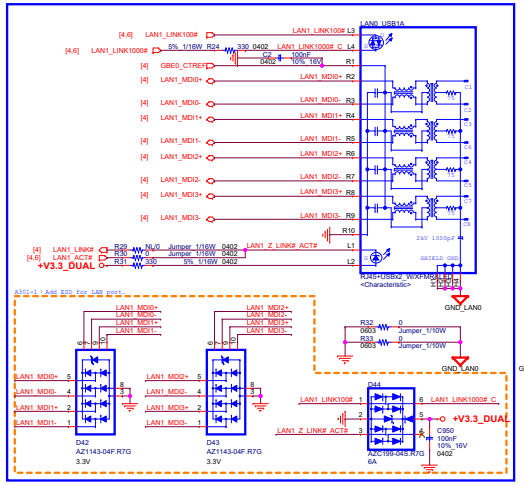

STDOFF1
STDOFF2
STDOFF3
STDOFF4
STDOFF5
POST_M2.5*5L
SOM-AB1
SOM-CD1
CN1C
CN1D
TRI_ETXE-BP_REV3.1_SOM-COM-E
<Characteristic>
CN1E
CN1F
CN1G
CN1H
CN1I
CN1J
CN1K
CN1L
HOLE_CN1E
HOLE_CN1F
HOLE_CN1G
HOLE_CN1H
HOLE_CN1I
HOLE_CN1J
HOLE_CN1K
HOLE_CN1L
R16
R17
R18
R19
R20
R21
R22
R23
BB_110x2V_S0.5mm
COM.0 R3.0 Changes from R2.1:
Remove TYPE 2 D97 pin PEG_ENABLE#.
TYPE 6 is RSVD.
+VIN(SOM A/B/C/D) total:
+V12 @ 12A
+V4.75 @ 30A
ADVANTECH
COMe R2.0 Type6 RAW C/D
SOM-DB5830
A3
Wednesday, January 18, 2023
Sheet 5 of 33

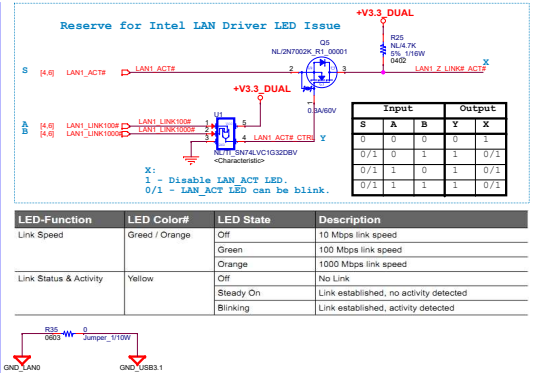
LAN0
RJ-45 (w/ USB3.1 x2)

A201-1 change connector to 2.5G

LAN0

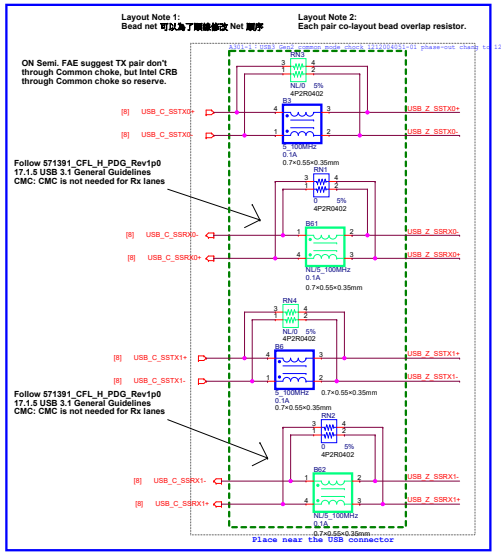


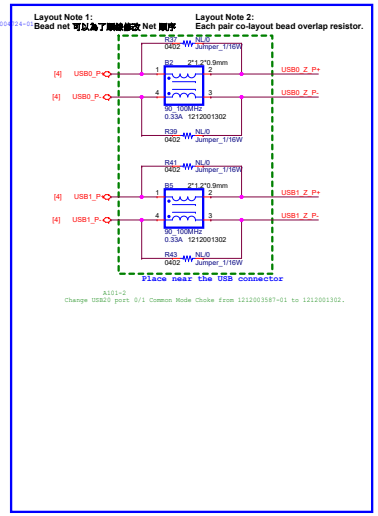


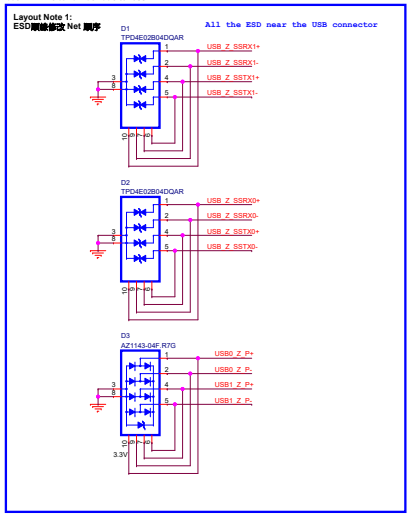


Input			Output	
S	A	B	Y	X
0	0	0	0	1
0/1	0	1	1	0/1
0/1	1	0	1	0/1
0/1	1	1	1	0/1

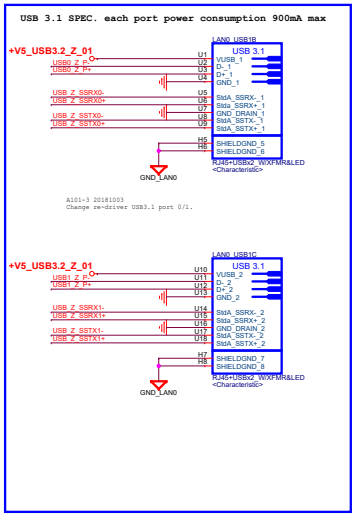
LED-Function	LED Color#	LED State	Description
Link Speed	Greed / Orange	Off	10 Mbps link speed
		Green	100 Mbps link speed
		Orange	1000 Mbps link speed
Link Status & Activity	Yellow	Off	No Link
		Steady On	Link established, no activity detected
		Blinking	Link established, activity detected







USB3.2 Gen2 / USB2.0



ADVANTECH

Title	LAN0/USB 3.1 Port 0-1	
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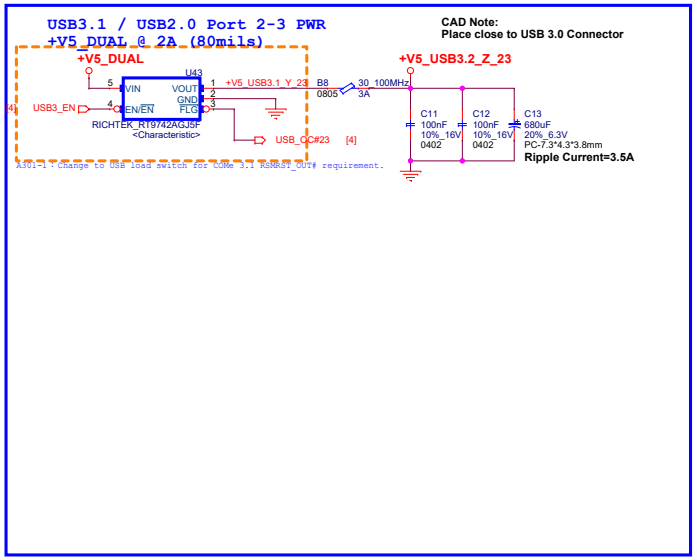
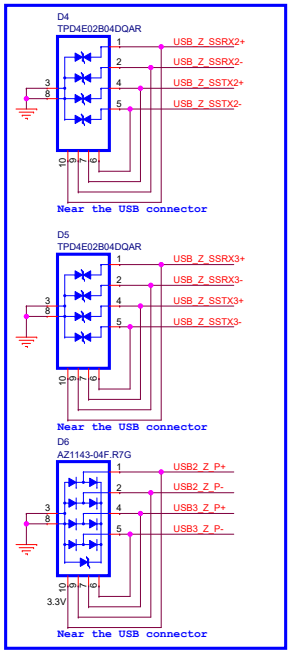
USB3.1 x2

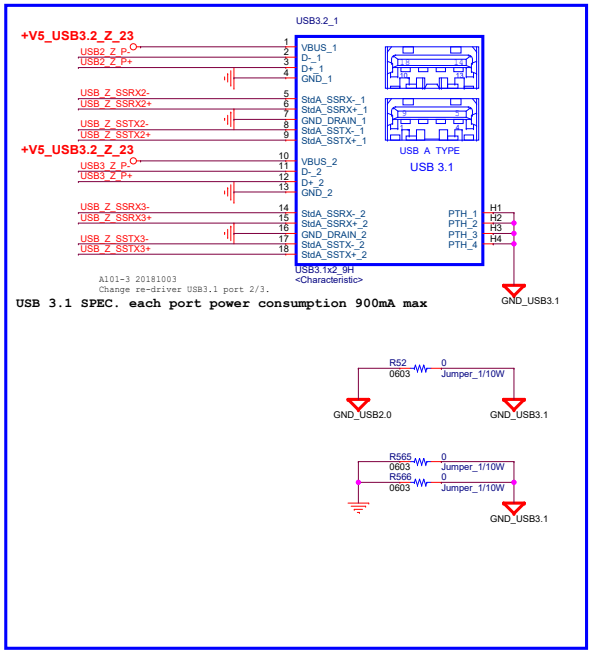


A101-1 170915
After ON Semi. review, ESD should work OK, but will limit bandwidth due to loss.

Layout Note:
ESD net 可以為了順線修改 Net 順序

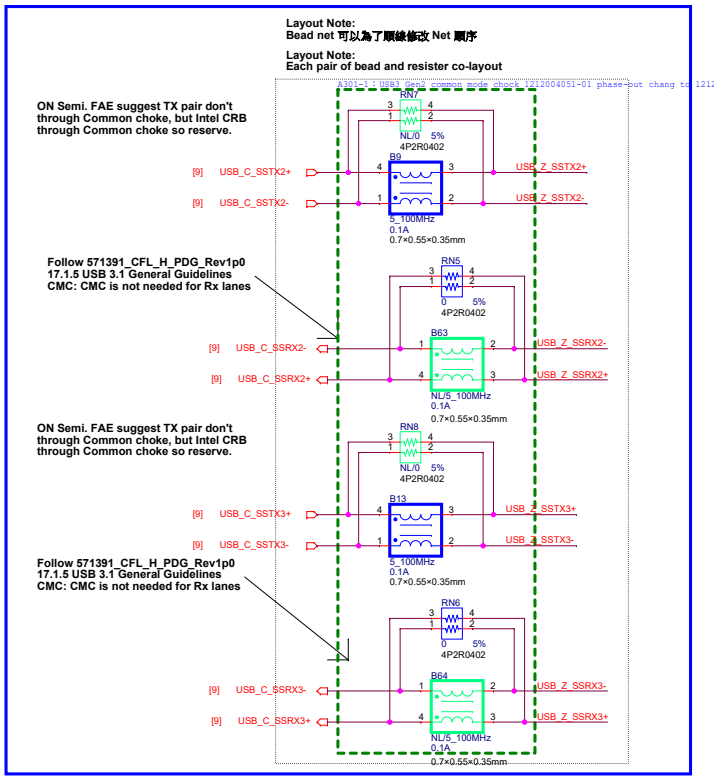


USB3.2 Connector Port 2-3



Layout Note:
Bead net 可以為了順線修改 Net 順序

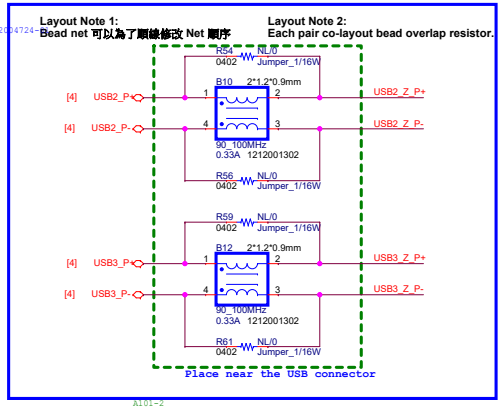
Layout Note:
Each pair of bead and resister co-layout



A101-2
Reserve Common Mode Choke co-layout for USB3.1 RX Port2/3 signal.

Layout Note 1:
Bead net 可以為了順線修改 Net 順序

Layout Note 2:
Each pair co-layout bead overlap resistor.



A101-2
Change USB20 port 2/3 Common Mode Choke from 1212003587-01 to 1212001302.

ADVANTECH

Title	USB3.1 Port 2-3	
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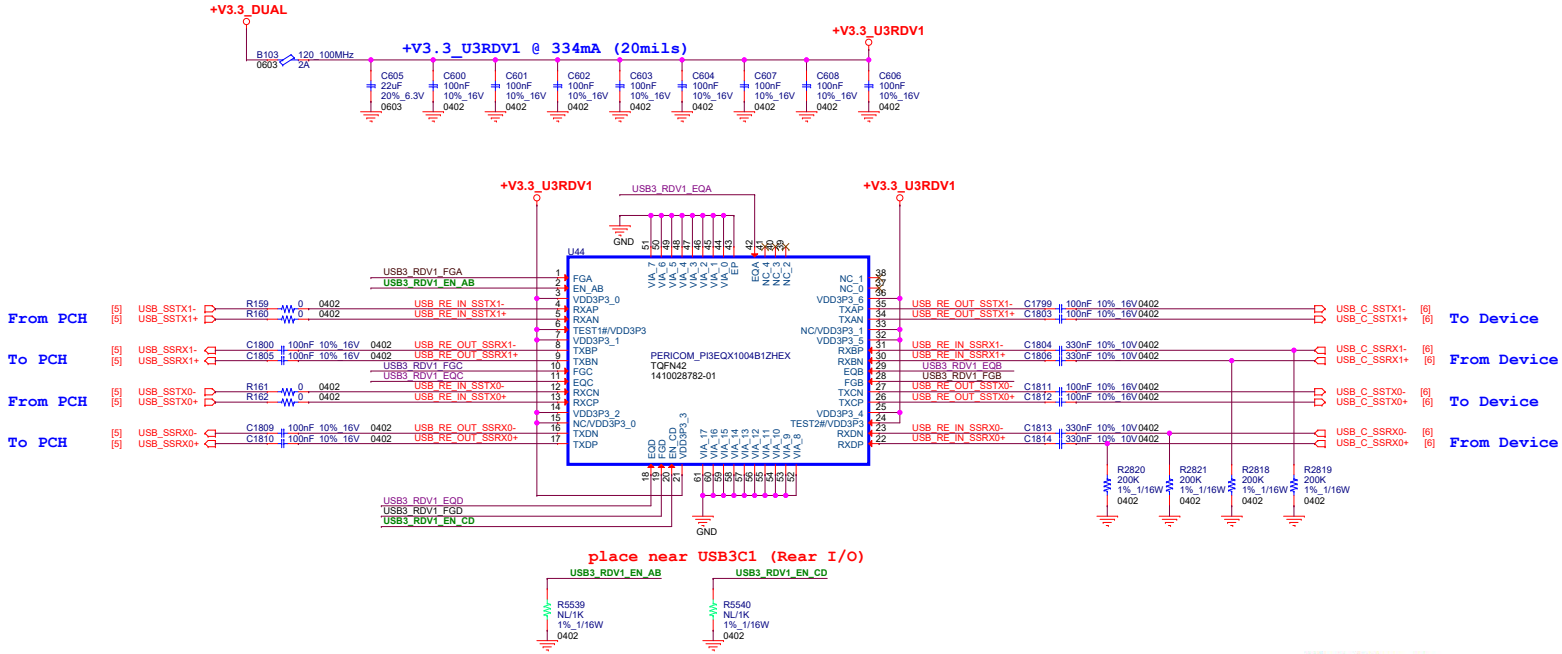
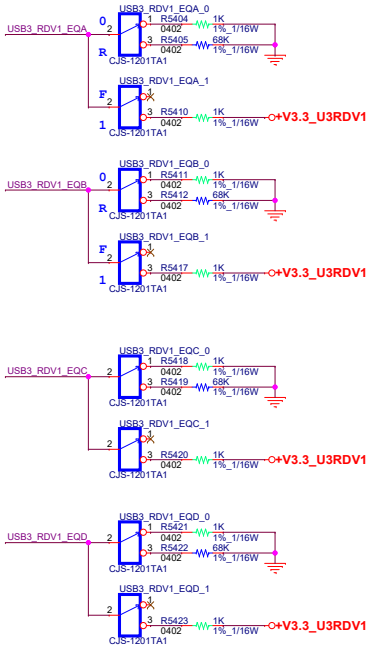
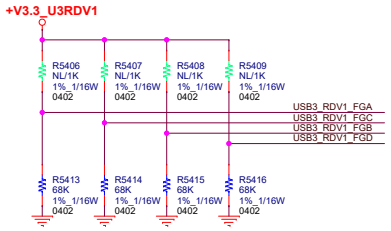
A301-1 : Change Re-driver to Pericom PERICOM PI3EQX1004B1ZHEX (1410028782-01)

USB3.1 Gen2 Redriver for USB3.2 x2 Port 0-1

IP:IIOT-22







3-pad colay

Equalization Setting:

EQA/B/C/D are the selection pins for the equalization selection

	Equalizer setting (dB)	
EQA/B/C/D	*@2.5GHz*	*@5GHz*
0 (Tie 0Ω to GND)	6.7	12.4
R (Tie Rext to GND)	3.5	8.0
F (Leave Open)	5.3	10.6
1 (Tie 0Ω to VDD)	8.4	14.6

Flat Gain Setting:

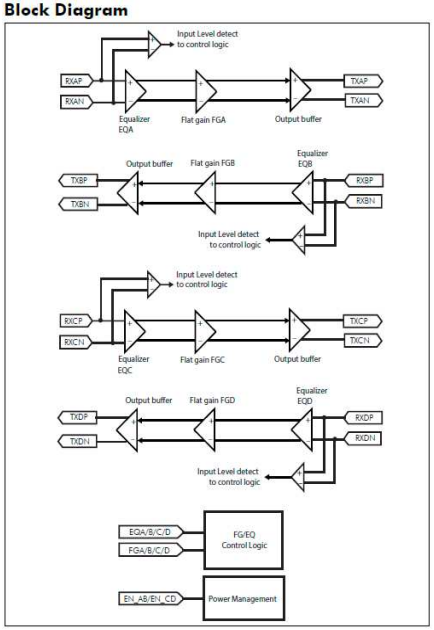
FGA/B/C/D are the selection pins for the DC gain

	Flat Gain Settings
FGA/B/C/D	*dB*
0 (Tie 0Ω to GND)	-1.6
R (Tie Rext to GND)	-0.5
F (Leave Open)	1.0
1 (Tie 0Ω to VDD)	2.7

Control pin Specifications (VDD = 3.3 ± 0.3V TA = 0 to 70°C)

Symbol	Parameter	Min.	Typ.	Max.	Units
2-level control pins					
V_{IH}	DC input logic High	VDD*0.65			V
V_{IL}	DC input logic Low			VDD*0.35	V
I_{IH}	Input High current			25	uA
I_{IL}	Input Low current	-25			uA
4-level control pins					
V_{IH}	DC input logic "High"	0.92*VDD	VDD		V
V_{IF}	DC input logic "Float"	0.59*VDD	0.67*VDD	0.75*VDD	V
V_{IR}	DC input logic "With Rext to GND"	0.25*VDD	0.33*VDD	0.41*VDD	V
V_{IL}	DC input logic "Low"		GND	0.08*VDD	V
I_{IH}	Input High current			50	uA
I_{IL}	Input Low current	-50			uA
Rext	External resistor connects to GND (±5%)	64.6	68	71.4	kΩ

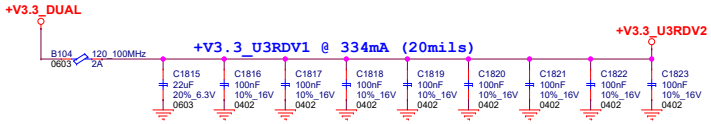
Block Diagram

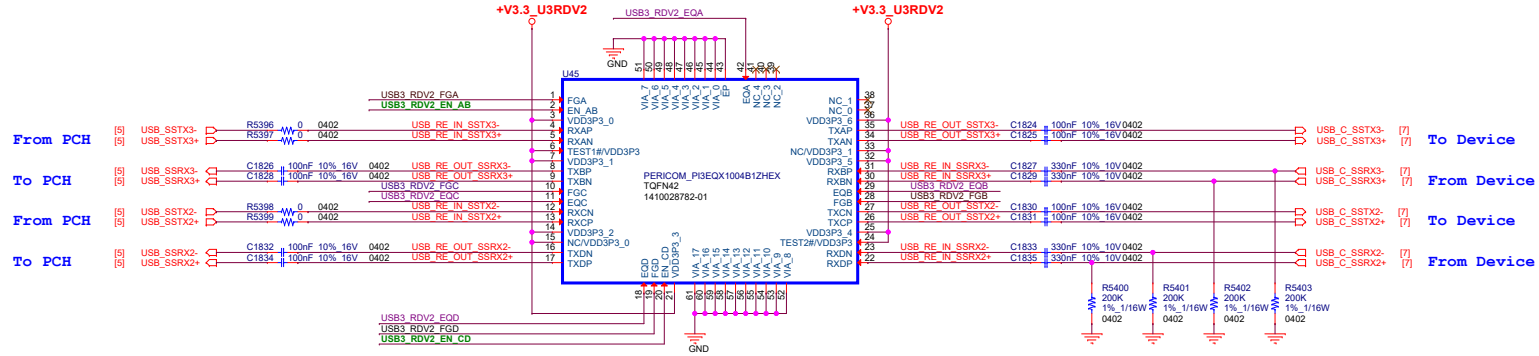


ADVANTECH					
Title	USB3.1 Redriver Port 0-1				
Size	Document Number	SOM-DB5830			Rev A3
Date:	Wednesday, January 18, 2023	Sheet 8 of 33			

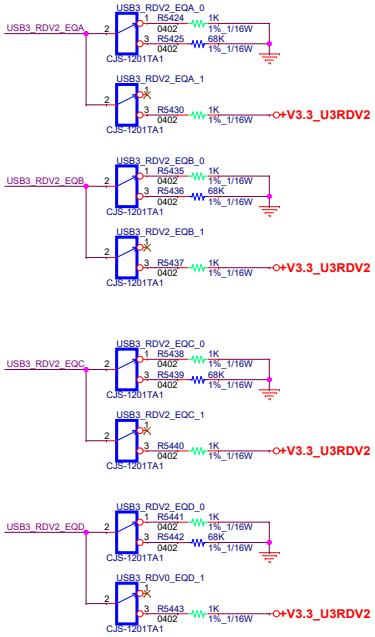
USB3.2 Gen2 Redriver for USB3.2 x2 Port 2-3

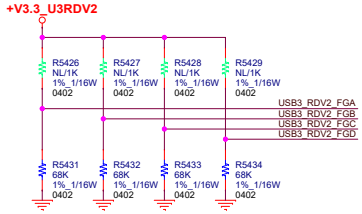
IP:IIOT-22





place near USB3C1 (Rear I/O)





3-pad colay

Equalization Setting:

EQA/B/C/D are the selection pins for the equalization selection

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EQA/B/C/D	*@2.5GHz*	*@5GHz*
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Flat Gain Setting:

FGA/B/C/D are the selection pins for the DC gain

	Flat Gain Settings
FGA/B/C/D	*dB*
0 (Tie 0Ω to GND)	-1.6
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F (Leave Open)	1.0
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Control pin Specifications (VDD = 3.3 ± 0.3V TA = 0 to 70°C)

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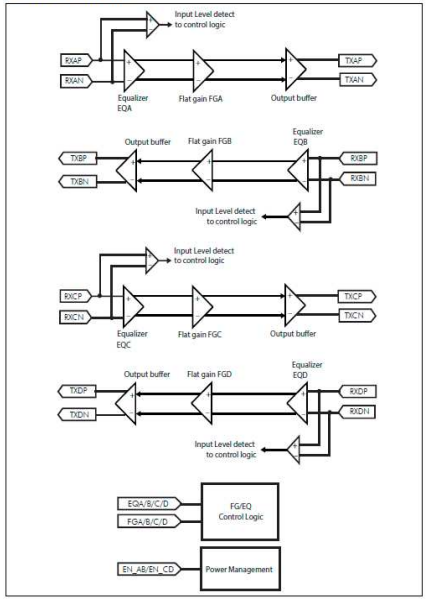
I_{IL}	Input Low current	-25			uA
4-level control pins					
V_{IH}	DC input logic "High"	0.92*VDD	VDD		V
V_{IF}	DC input logic "Float"	0.59*VDD	0.67*VDD	0.75*VDD	V
V_{IR}	DC input logic "With Rext to GND"	0.25*VDD	0.33*VDD	0.41*VDD	V
V_{IL}	DC input logic "Low"		GND	0.08*VDD	V
I_{IH}	Input High current			50	uA
I_{IL}	Input Low current	-50			uA
Rext	External resistor connects to GND (±5%)	64.6	68	71.4	kΩ

Block Diagram



ADVANTECH

Title	USB3.1 Redriver Port 2-3	
Size	Document Number SOM-DB5830	Rev A3
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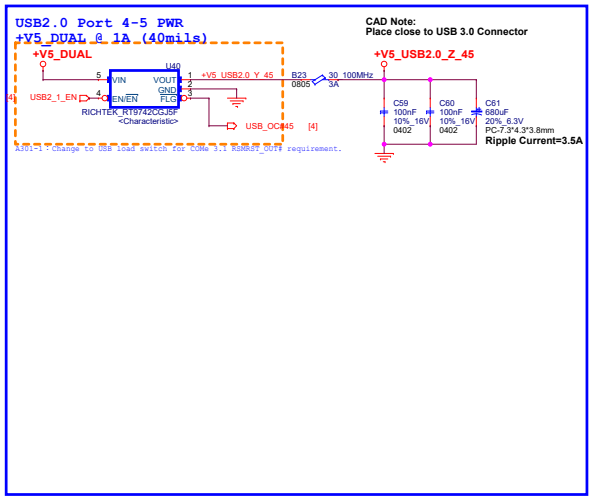
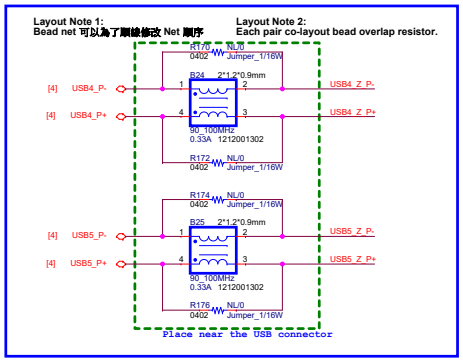
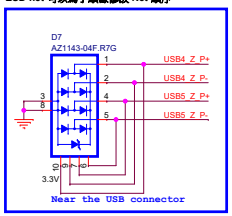
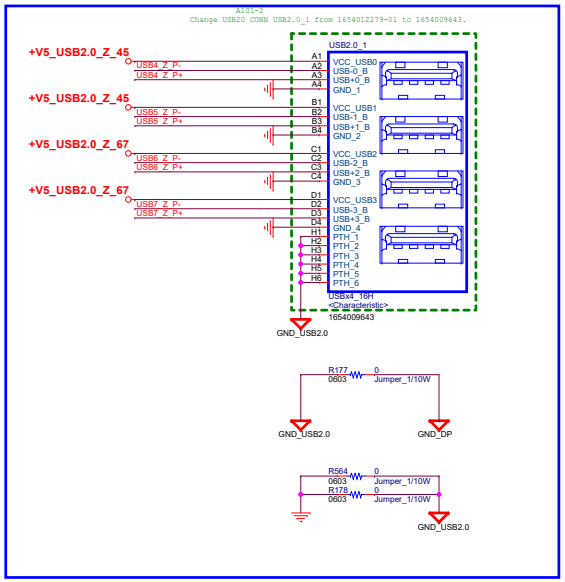
USB2.0 Port 4-5 PWR



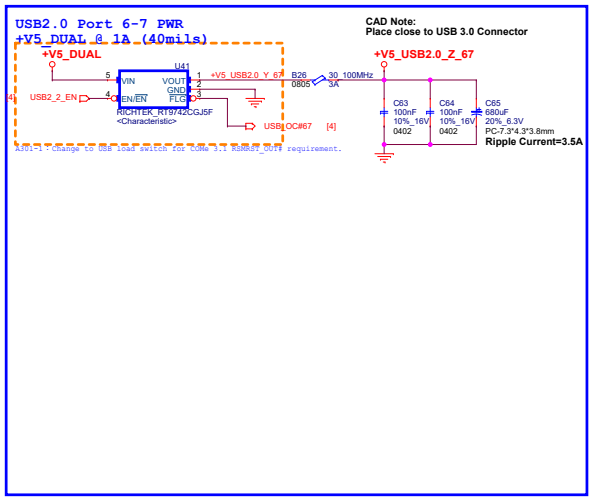


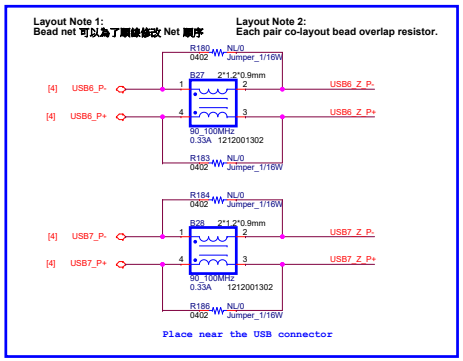


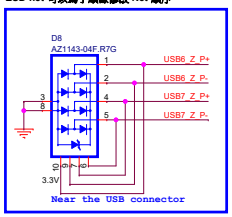
USB2.0 Port 4-7



USB2.0 Port 6-7 PWR







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Title	USB2.0 Port 4-7		
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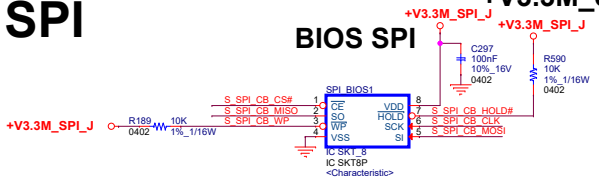
SPI

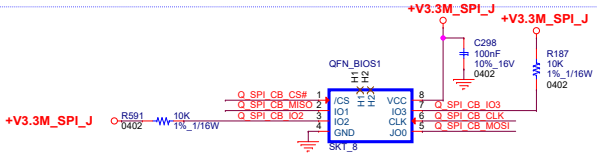
+V3.3M_SPI @ 100mA

BIOS SPI

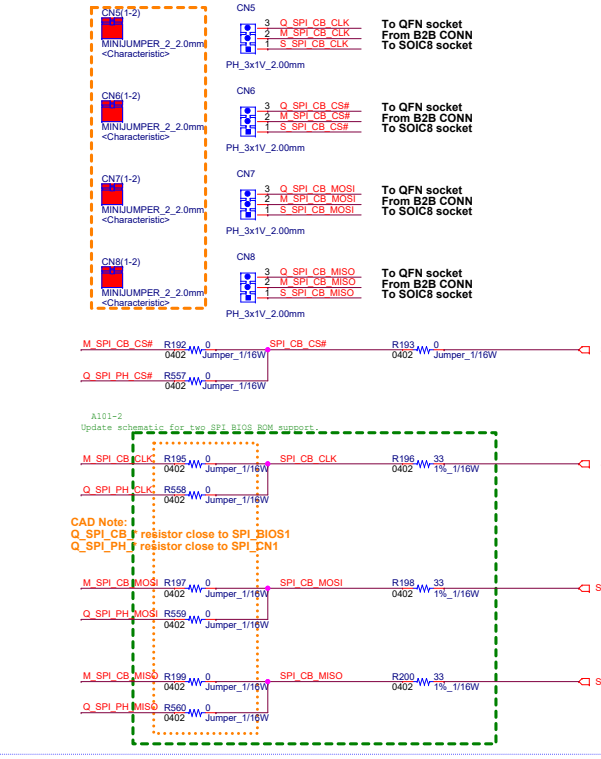
With COM.0 Rev 3, the SPI interface maybe either 3.3V or 1.8V, as is best for the Module chipset at hand.

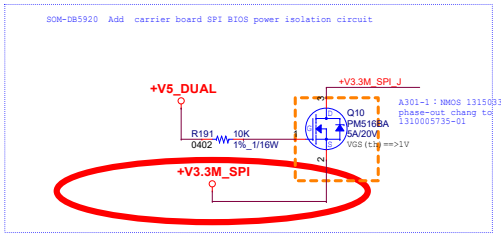


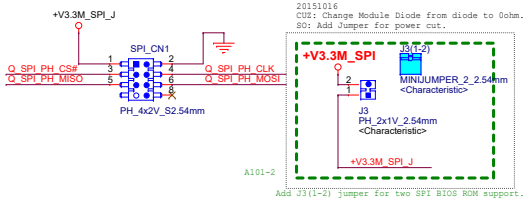
A201-1 change to 2 BIOS socket SOT&QFN



A301-1 : 1653005287-01 phase-out, change to 1653008397-01



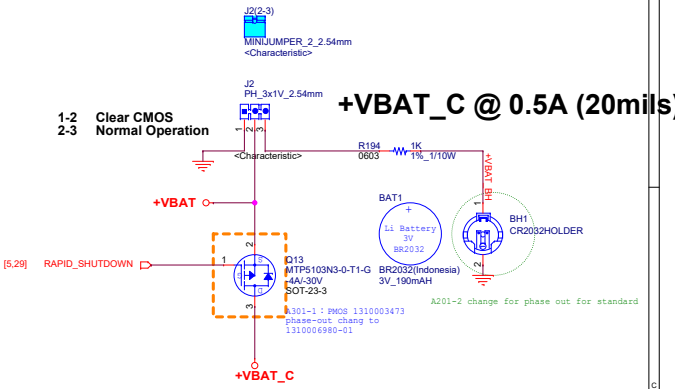




RTC BATTERY

+VBAT_C @ 0.5A (20mils)

1-2 Clear CMOS
2-3 Normal Operation

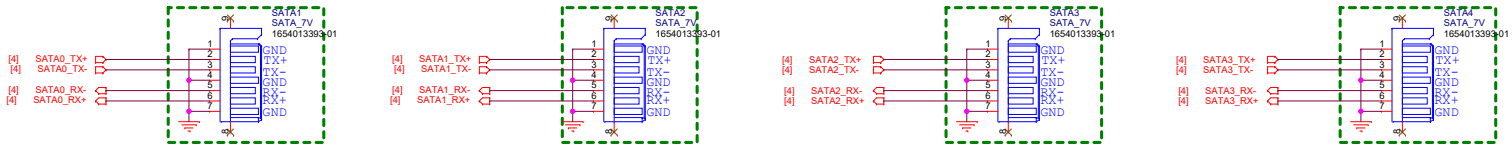


SATA

P/N: 1654005955
PIN length 3.3mm

P/N: 1654013393-01
PIN length 2.1mm

A101-2
Change SATA1~SATA4 from 1654005955 to 1654013393-01 for DFM request.



ADVANTECH

Title	BIOS socket/SATA/RTC	
Size	Document Number: SOM-DB5830	Rev: A3
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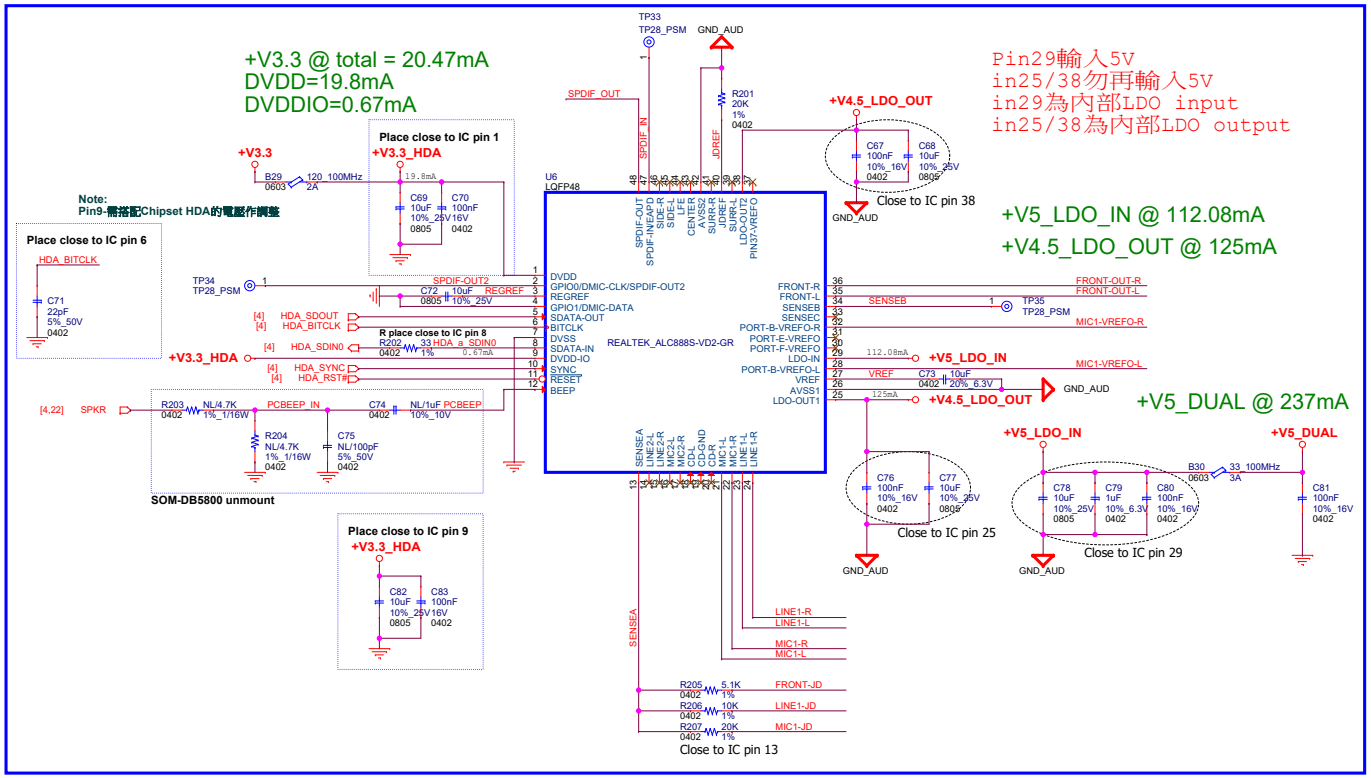
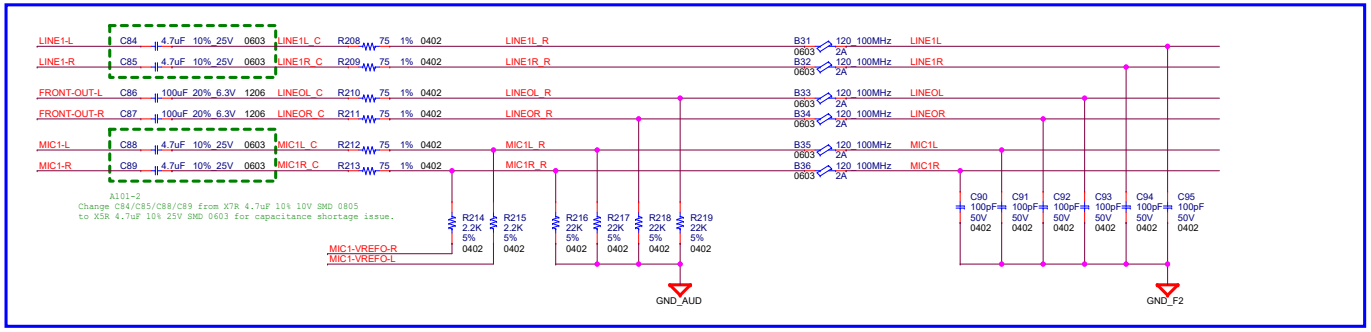
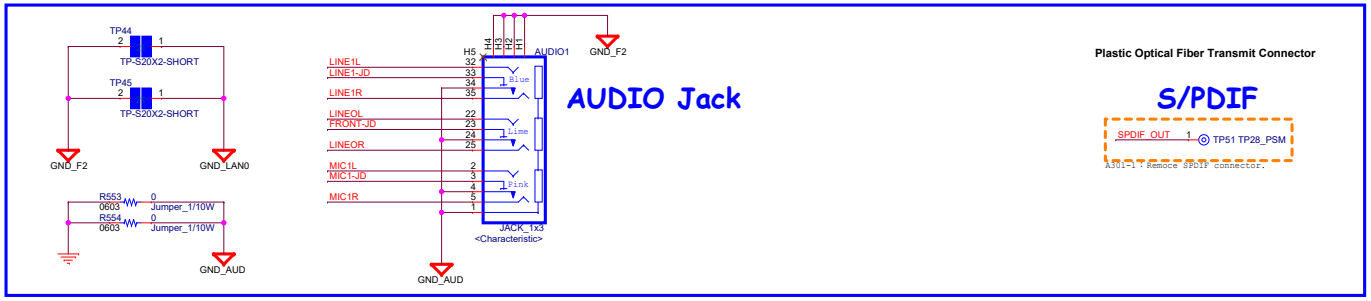
HD Audio Codec REALTEK ALC888S-VD2-GR







ADVANTECH			
Title	HD Audio Codec ALC888		
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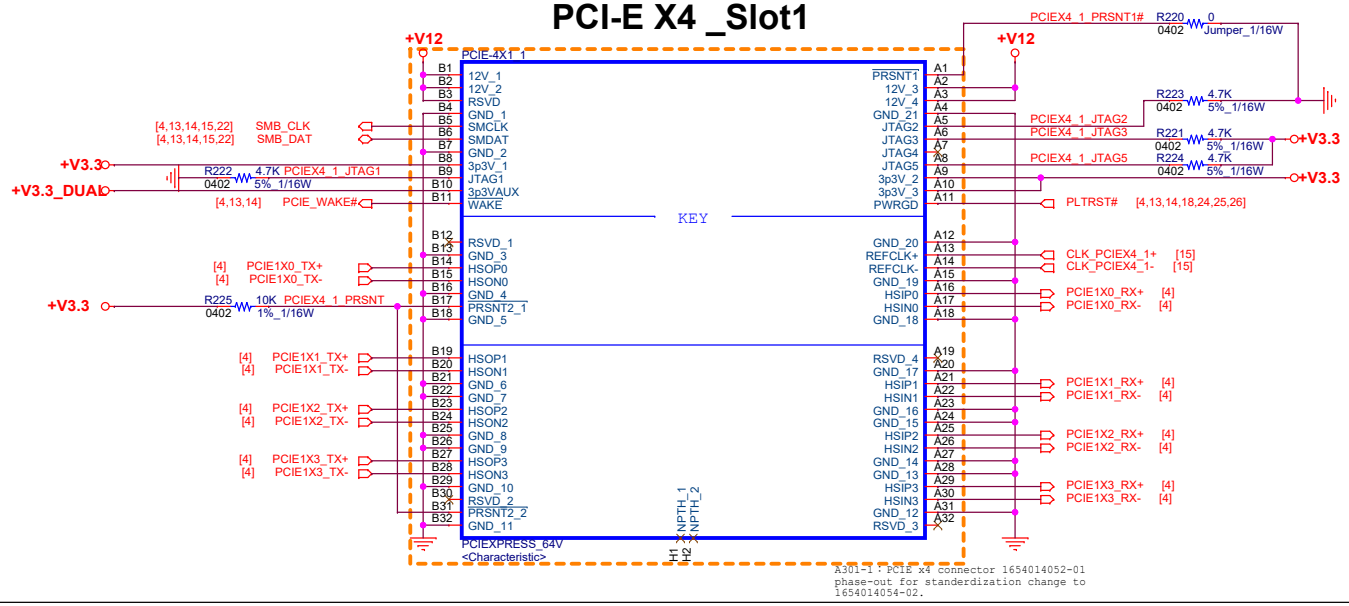
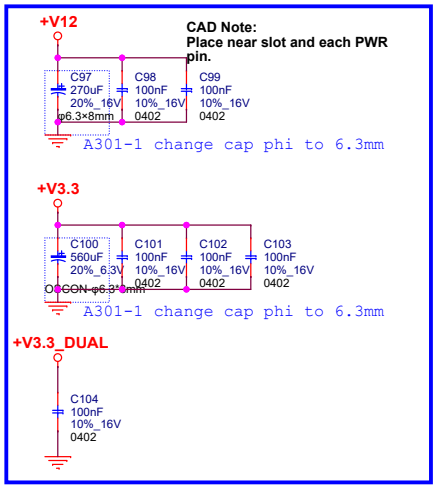
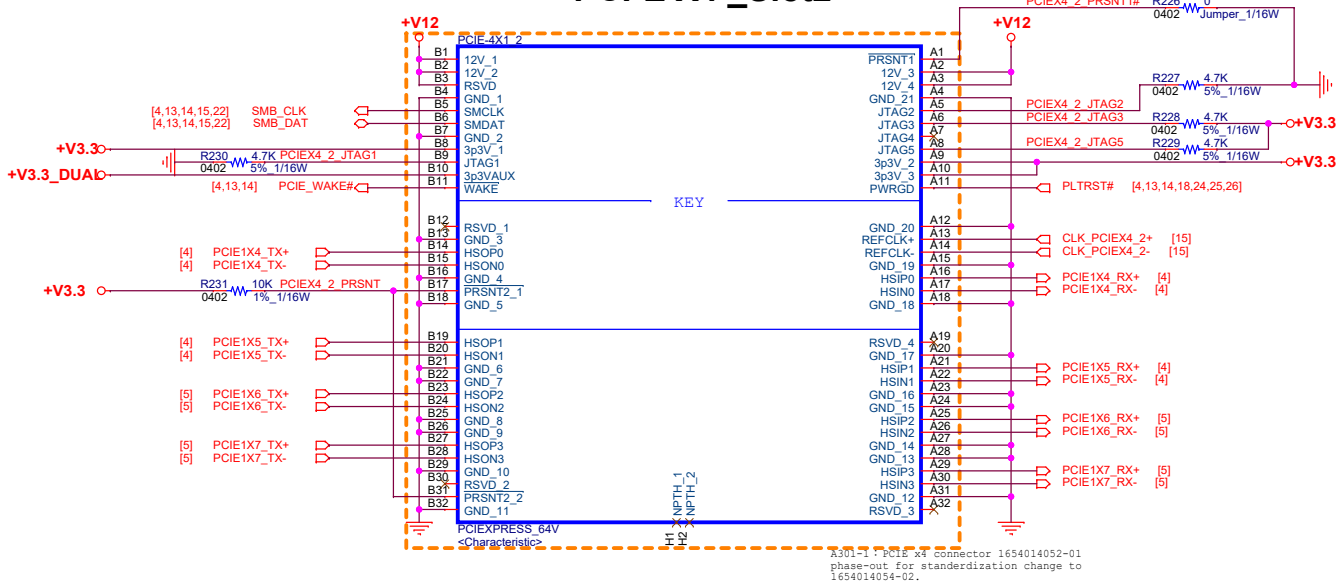
PCI-E X4 _Slot1



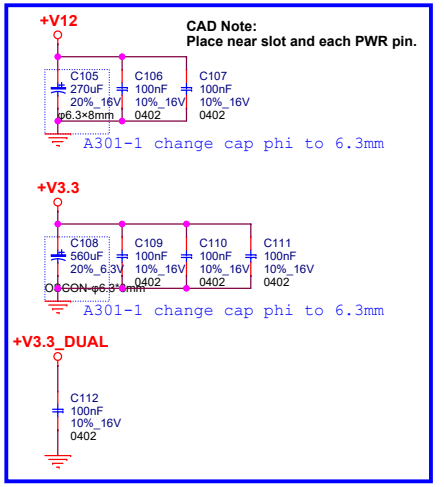
A301-1 : PCIE x4 connector 1654014052-01 phase-out for standerdization change to 1654014054-02.



PCI-E X4 _Slot2



A301-1 : PCIE x4 connector 1654014052-01 phase-out for standerdization change to 1654014054-02.



ADVANTECH

Title	PCIe X4 Slot 1-2	
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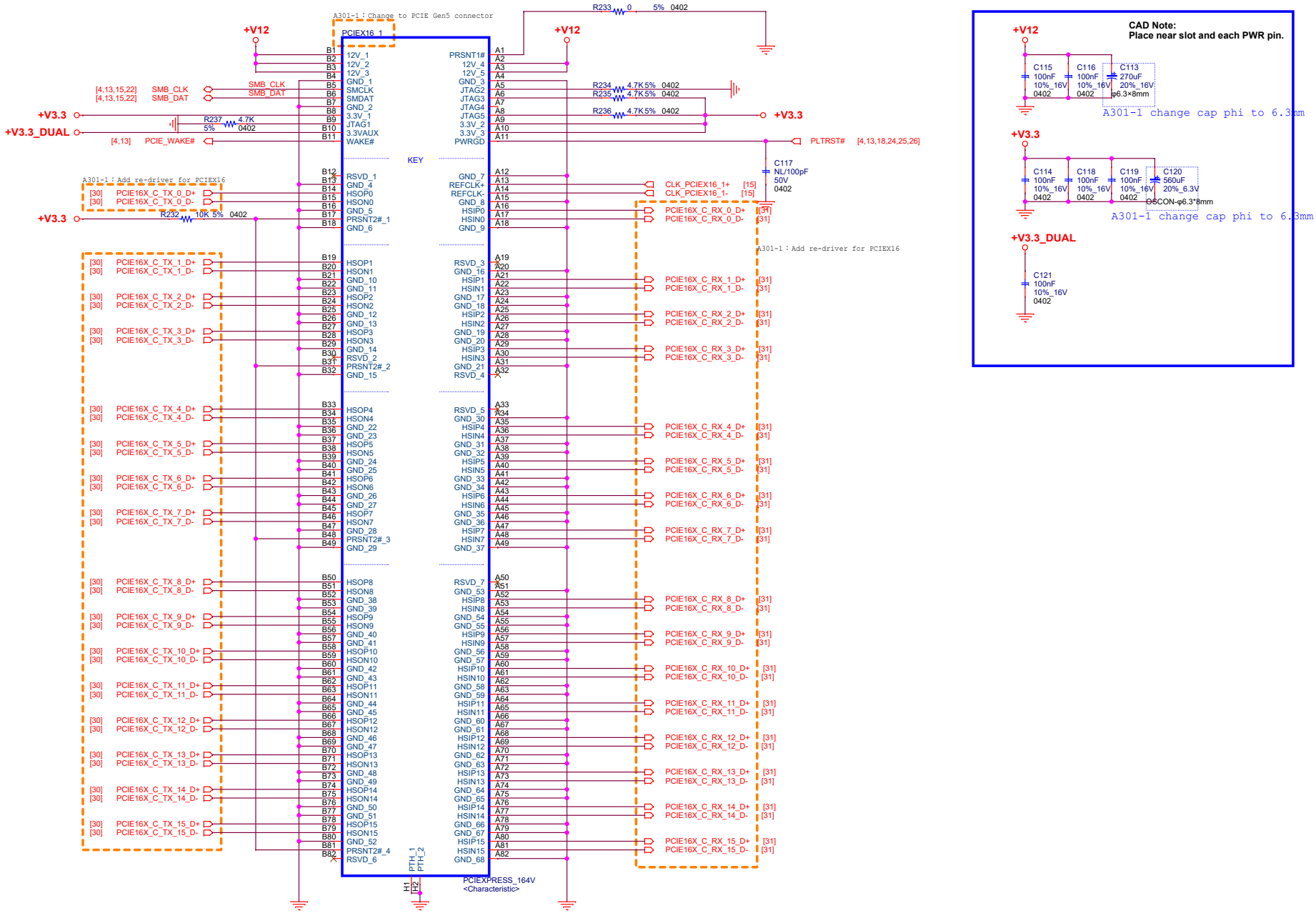

ADVANTECH

Title: PCI Express X16 Slot

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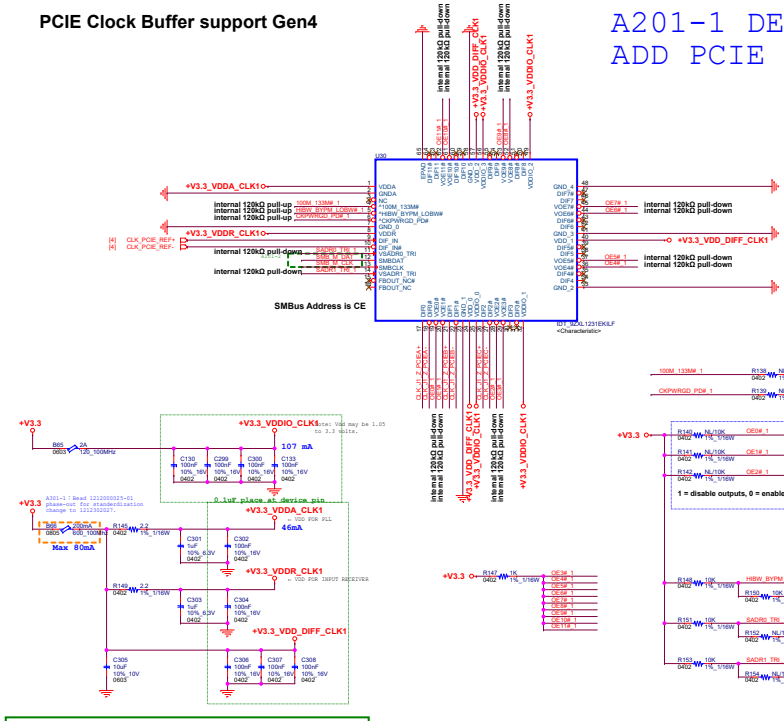
PCIE Clock Buffer support Gen4

A201-1 DEL PCIE GEN3 clock buffer
ADD PCIE GEN4 clock buffer



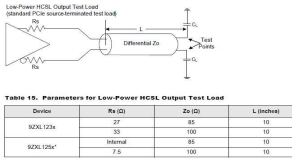


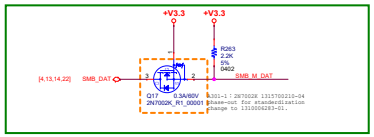
Table 15. Parameters for Low-Power HCSL Output Test Load

Device	Rs (Ω)	Zo (Ω)	L (inches)	C_L (pF)
9ZXL123x	27	85	10	2
	33	100	10	2
9ZXL125x*	Internal	85	10	2
	7.5	100	10	2

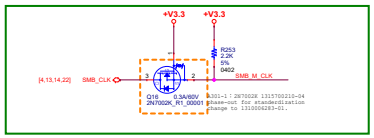
SMBus Addressing

SMB_A1_tri	SMB_A0_tri	SMBus Address
0	0	D8
0	M	DA
0	1	DE
M	0	C2
M	M	C4
M	1	C6
1	0	CA
1	M	CC
1	1	CE

*Default



Swap U7 SMB_M_CLK and SMB_M_DAT for connect mistake.



Functionality at Power-Up (PLL Mode)

100M_133M#	DIF_IN MHz	DIF[x]
1	100.00	DIF_IN
0	133.33	DIF_IN

PLL Operating Mode Readback

HIBW_BYPM_LOBW#	Byte0, bit 7	Byte 0, bit 6
Low (Low BW)	0	0
Mid (Bypass)	0	1
High (High BW)	1	1

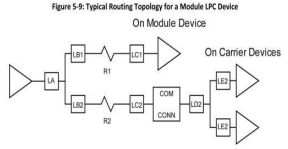
*Default Bypass

5.4.9 *Carrier Board LPC Devices*

Carrier Board LPC devices ***should*** be clocked with the LPC clock provided by the Module interface. If the Carrier Board has two loads on the LPC clock these loads ***should*** be connected to the common clock without a buffer. The Carrier Board ***should*** not have more than two loads on the LPC clock.
Carrier Board LPC devices ***should*** be reset with signal CB_RESET#.

A typical routing topology for a Module LPC device and two Carrier Board LPC devices clock is shown below. This topology is used by Modules that start and stop the LPC clock on the fly. In this case, a buffer cannot be used and all LPC devices must share a common clock.

Figure 5-9: Typical Routing Topology for a Module LPC Device



LA 500 mils max
LB1 = LB2 = 150 mils max
LC1 = 8.88"+LC2
LC2 = .25" max
LE2 = 1" max
LD2 + LE2 (note 2 instances of LE2) = 8.88"
R1 = R2 = 22Ω

Figure 192. LPC_CLK[0] or LPC_CLK[1]Routing Topology—2 Branches Using One Clock as Output

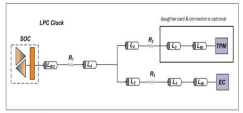


Table 132. LPC_CLK[1:0] Signals Trace Routing—2 Branches (Sheet 1 of 2)

Parameter	Trace Width (mils)	Minimum Trace Spacing (mils)	Trace Length (mils)
Breakout L_{B1} and Breakin L_{B2}	3.50	3.50	0-500
L1 Main Route	4mils PIS 4.5mils DSL	15	500-7500
L2 Main Route	4mils PIS 4.5mils DSL	15	500-2800
L3 Main Route	4mils PIS 4.5mils DSL	15	500-2500

A201-1 DEL LPC CLK buffer .

ADVANTECH
Title: Clock Buffer PCI-E/PCI
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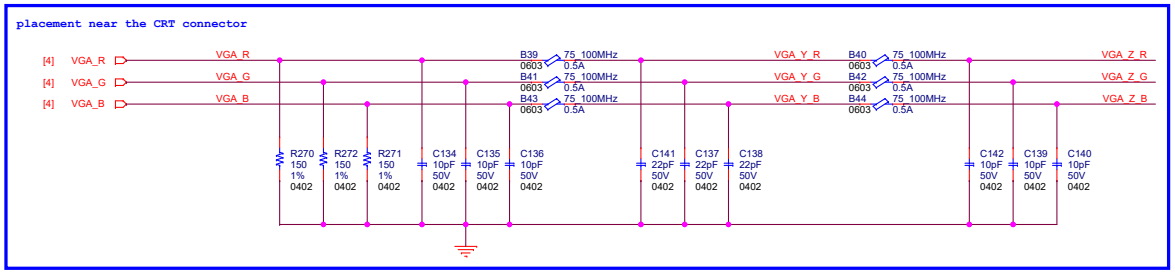
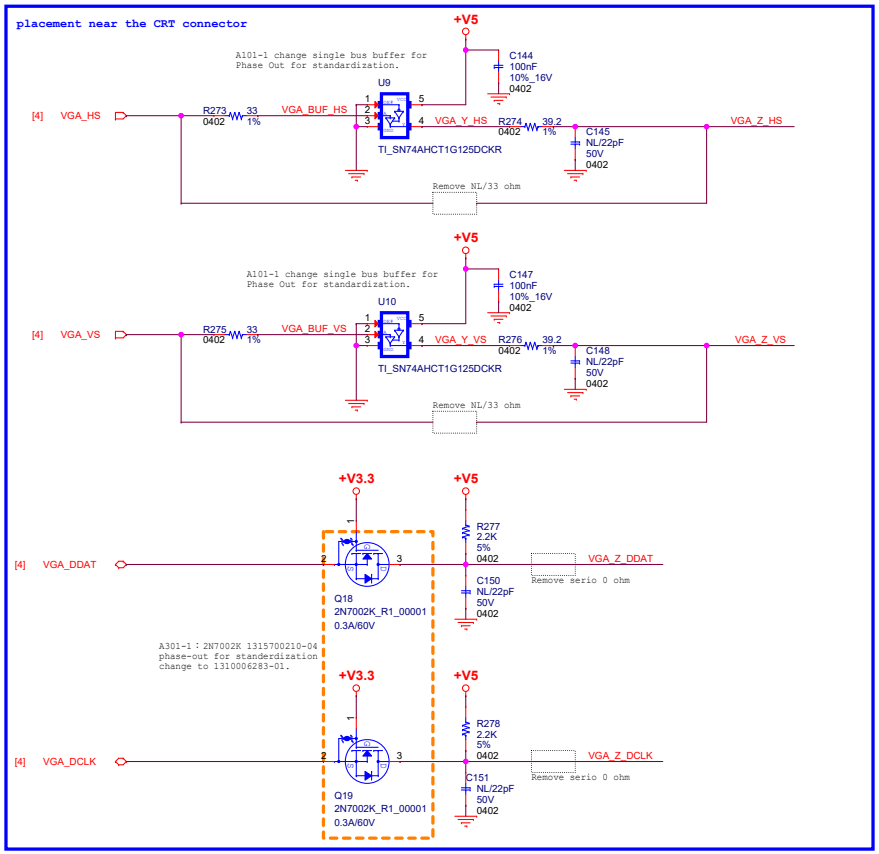
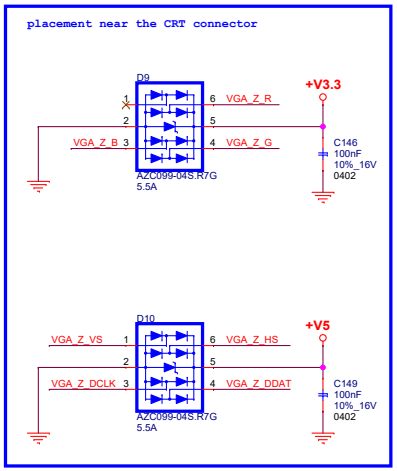
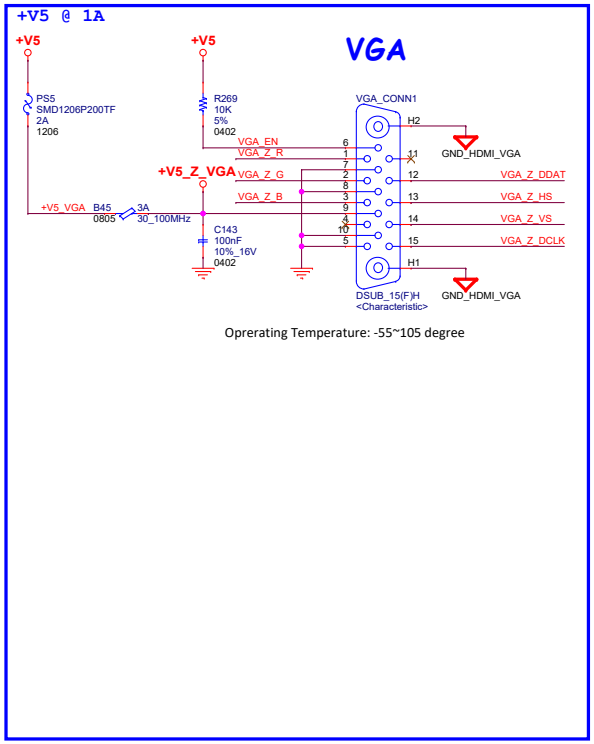
VGA









ADVANTECH		
Title	VGA	
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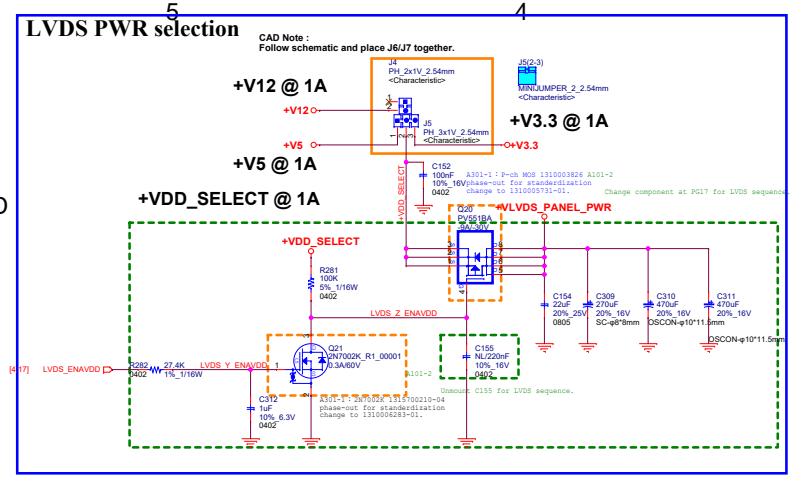
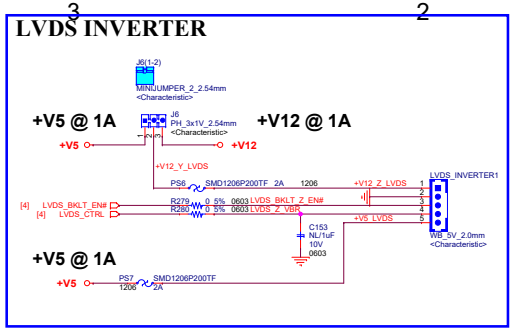
LVDS PWR selection

CAD Note :
Follow schematic and place J6/J7 together.

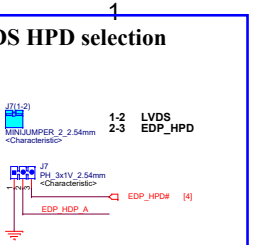
+V12 @ 1A
+V5 @ 1A
+VDD_SELECT @ 1A
+V3.3 @ 1A



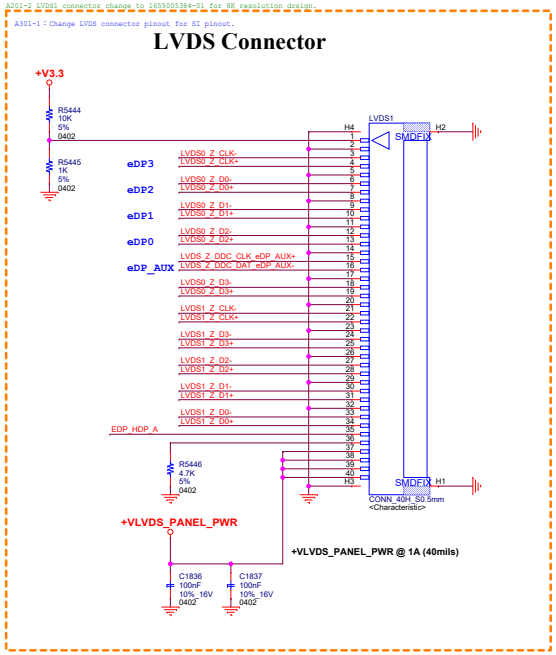
LVDS INVERTER



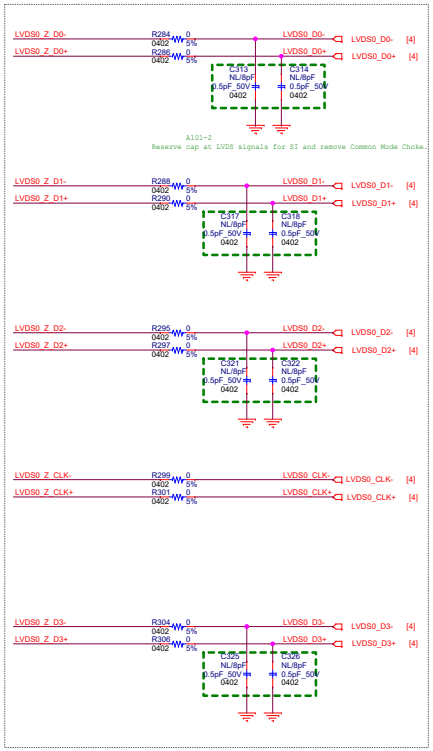
EDP / LVDS HPD selection



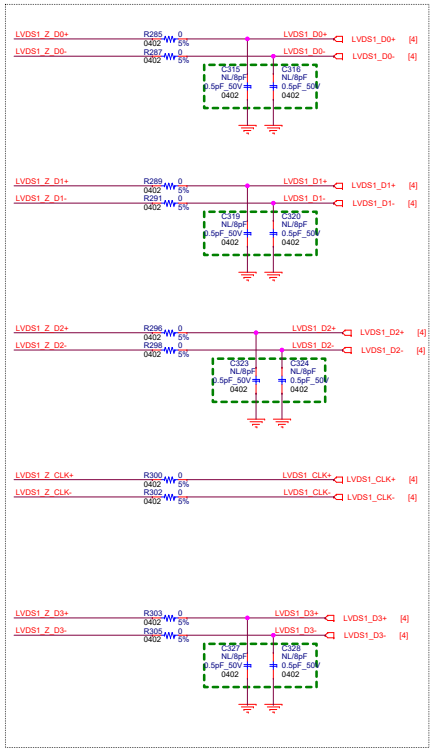
LVDS Connector



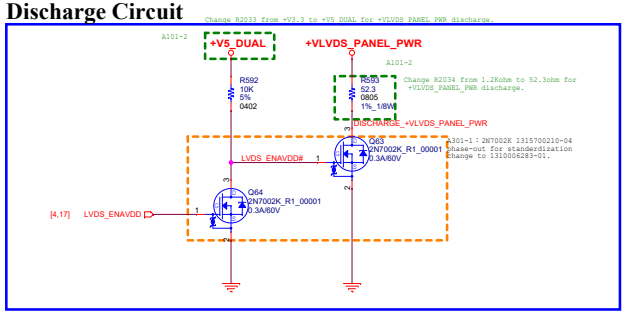
Layout Note: Each pair of bead and resister co-layout



Layout Note: Each pair of bead and resister co-layout



Discharge Circuit



ADVANTECH			
Title: LVDS Connector			
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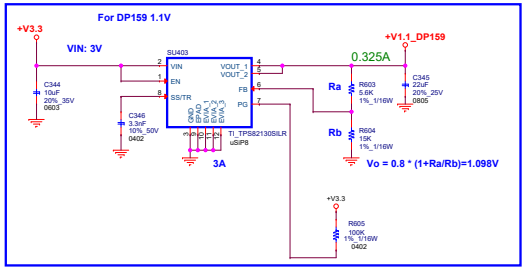
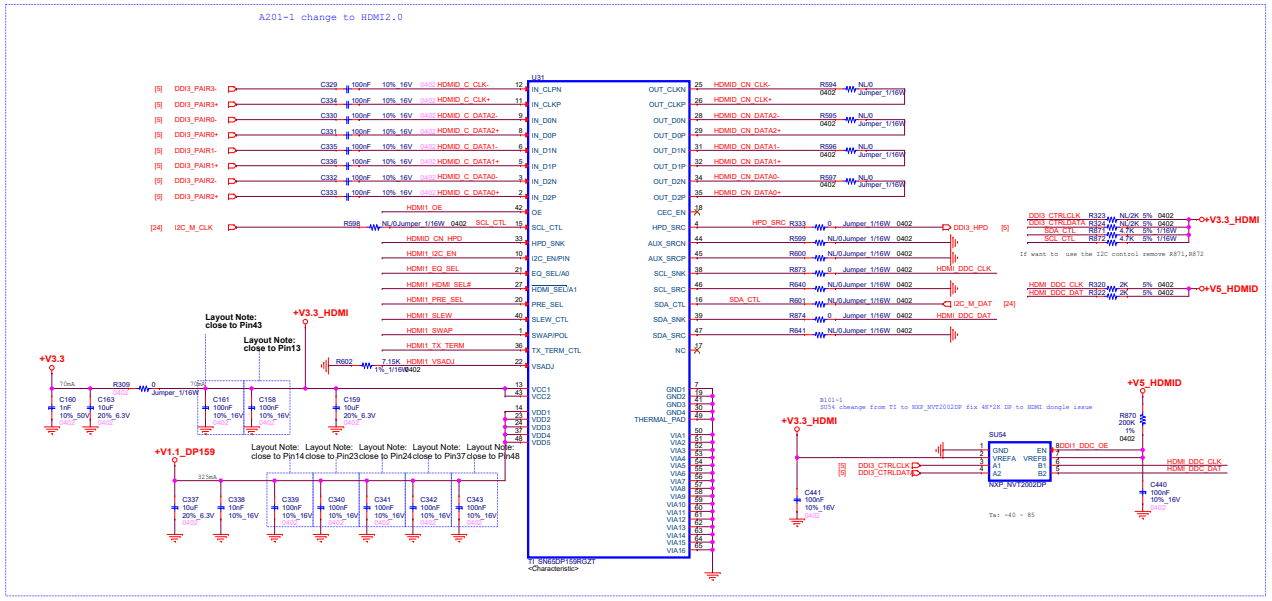
Table 11: Display Port / HDMI / DVI Pin-out of Type 10 and Type 6

COM Express Pin Name	DDI0 Type 10	DDI1 Type 6	DDI2 Type 6	DDI3 Type 6	Function (DDIX) DisplayPort	Function (DDIX) HDMI / DVI
DDIX_PAIR0+	B71	D26	D39	C39	DPX_LANE0+	TMDSX_DATA2+
DDIX_PAIR0-	B72	D27	D40	C40	DPX_LANE0-	TMDSX_DATA2-
DDIX_PAIR1+	B73	D29	D42	C42	DPX_LANE1+	TMDSX_DATA1+
DDIX_PAIR1-	B74	D30	D43	C43	DPX_LANE1-	TMDSX_DATA1-
DDIX_PAIR2+	B75	D32	D46	C46	DPX_LANE2+	TMDSX_DATA0+
DDIX_PAIR2-	B76	D33	D47	C47	DPX_LANE2-	TMDSX_DATA0-
DDIX_PAIR3+	B81	D36	D49	C49	DPX_LANE3+	TMDSX_CLK+
DDIX_PAIR3-	B82	D37	D50	C50	DPX_LANE3-	TMDSX_CLK-
DDIX_HPD	B89	C24	D44	C44	DPX_HPD	HDMIX_HPD
DDIX_CTRLCLK_AUX+	B98	D15	C32	C36	DPX_AUX+	HDMIX_CTRLCLK
DDIX_CTRLDATA_AUX-	B99	D16	C33	C37	DPX_AUX-	HDMIX_CTRLDATA
DDIX_DDC_AUX_SEL	B95	D34	C34	C38		





SWAP	Input lane SWAP
NC	normal working Default Setting
1	receive lane polarity swap(retimer mode only)
0	receive lane swap(retimer and redriver mode)

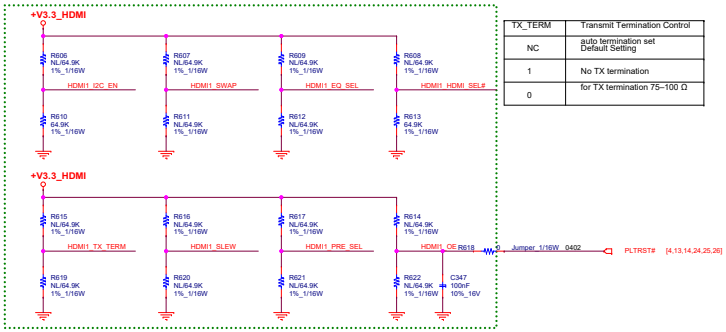
EQ_SEL	EQ_SEL
NC	Adaptive EQ Default Setting
1	for Fixed at 14 dB
0	for Fixed EQ at 7.5 dB

HDMI_SEL#	HDMI_SEL
NC	Weak internal pull down
1	DVI mode
0	Normal mode Default Setting

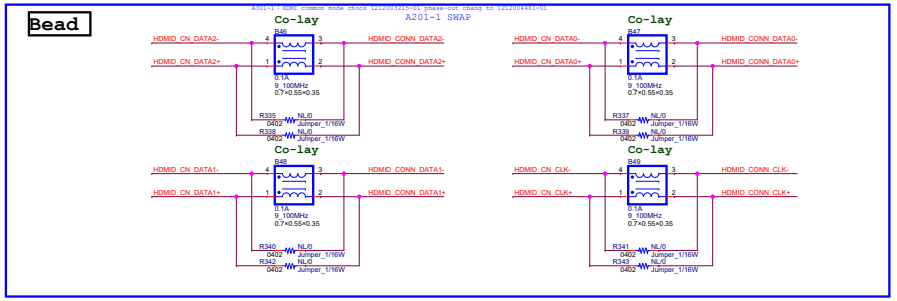
SLEW	Slew rate control
NC	for 10 ps slow Default Setting
1	fastest data rate
0	for 5 ps slow

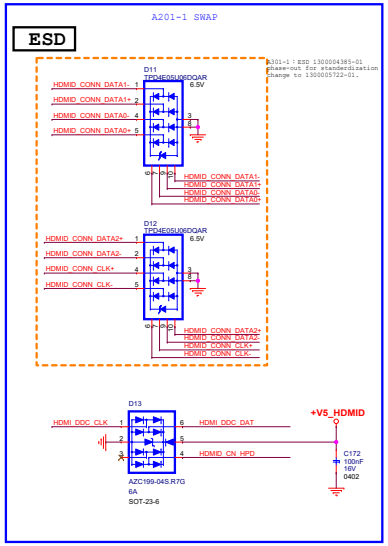
PRE_SEL	De-emphasis
NC	0dB Default Setting
1	Reserved
0	-2 dB

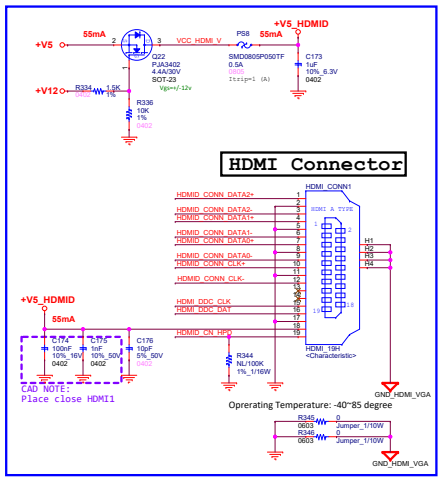
I2C_EN	I2C_EN
NC	Weak internal pull down
1	for I2C ENABLE
0	for PIN STRAP Default Setting



TX_TERM	Transmit Termination Control
NC	auto termination set Default Setting
1	No TX termination
0	for TX termination 75~100 Ω







ADVANTECH

Title	HDMI Conn. DDI3	
Size	Document Number SOM-DB5830	Rev A3
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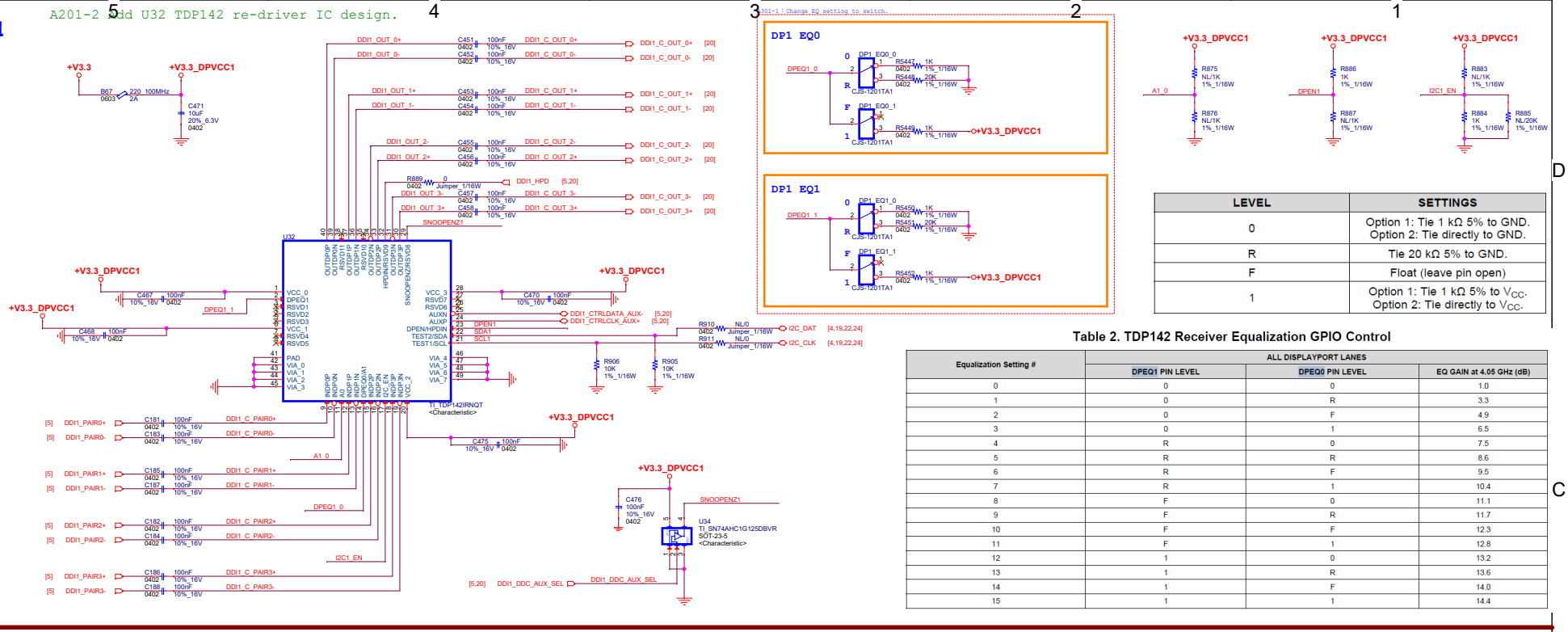

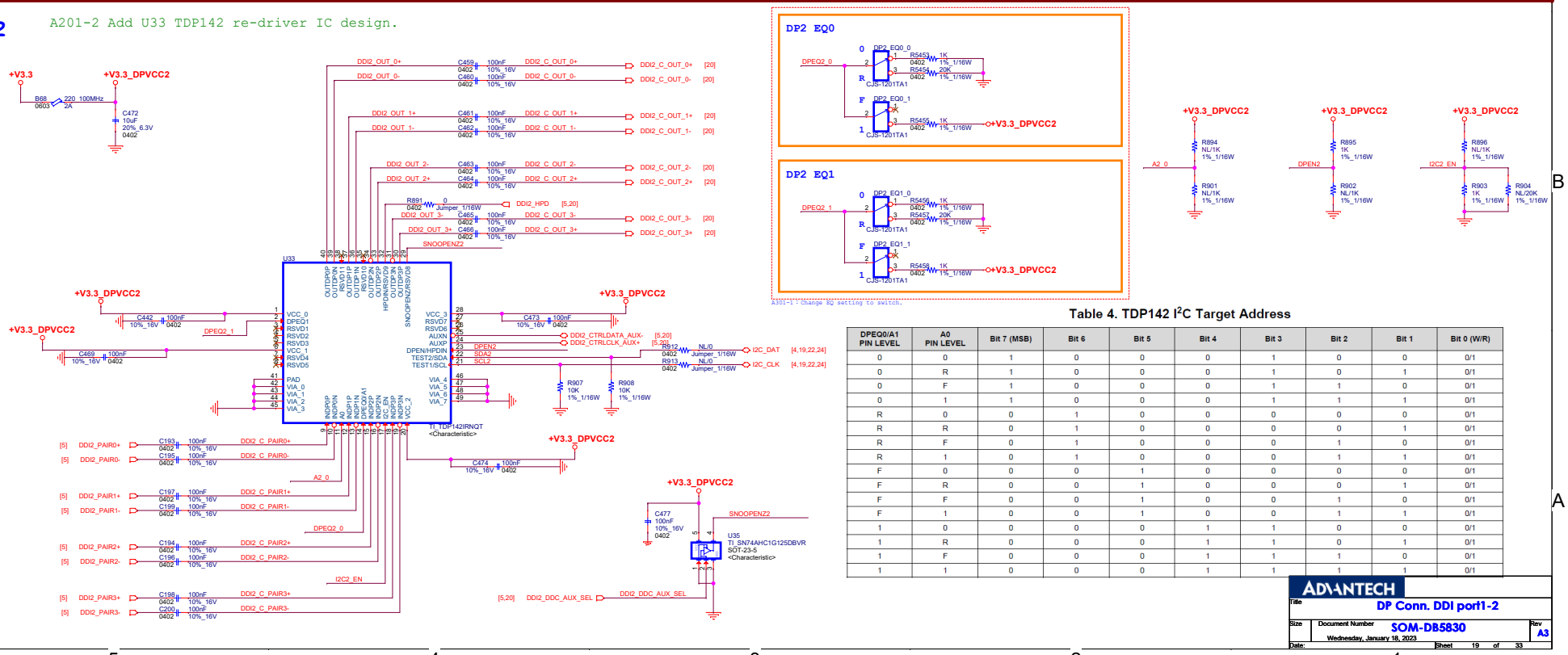

LEVEL	SETTINGS
0	Option 1: Tie 1 kΩ 5% to GND. Option 2: Tie directly to GND.
R	Tie 20 kΩ 5% to GND.
F	Float (leave pin open)
1	Option 1: Tie 1 kΩ 5% to V_{CC}. Option 2: Tie directly to V_{CC}.

Table 2. TDP142 Receiver Equalization GPIO Control

Equalization Setting #	ALL DISPLAYPORT LANES		
	DPEQ1 PIN LEVEL	DPEQ0 PIN LEVEL	EQ GAIN at 4.05 GHz (dB)
0	0	0	1.0
1	0	R	3.3
2	0	F	4.9
3	0	1	6.5
4	R	0	7.5
5	R	R	8.6
6	R	F	9.5
7	R	1	10.4
8	F	0	11.1
9	F	R	11.7
10	F	F	12.3
11	F	1	12.8
12	1	0	13.2
13	1	R	13.6
14	1	F	14.0
15	1	1	14.4

Table 4. TDP142 I²C Target Address

DPEQ0/A1 PIN LEVEL	A0 PIN LEVEL	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (W/R)
0	0	1	0	0	0	1	0	0	0/1
0	R	1	0	0	0	1	0	1	0/1
0	F	1	0	0	0	1	1	0	0/1
0	1	1	0	0	0	1	1	1	0/1
R	0	1	0	0	0	0	0	0	0/1
R	R	0	1	0	0	0	0	1	0/1
R	F	0	1	0	0	0	1	0	0/1
R	1	0	1	0	0	0	1	1	0/1
F	0	0	0	1	0	0	0	0	0/1
F	R	0	0	1	0	0	0	1	0/1
F	F	0	0	1	0	0	1	0	0/1
F	1	0	0	1	0	0	1	1	0/1
1	0	0	0	0	1	1	0	0	0/1
1	R	0	0	0	1	1	0	1	0/1
1	F	0	0	0	1	1	1	0	0/1
1	1	0	0	0	1	1	1	1	0/1

ADVANTECH

Title	DP Conn. DDI port1-2
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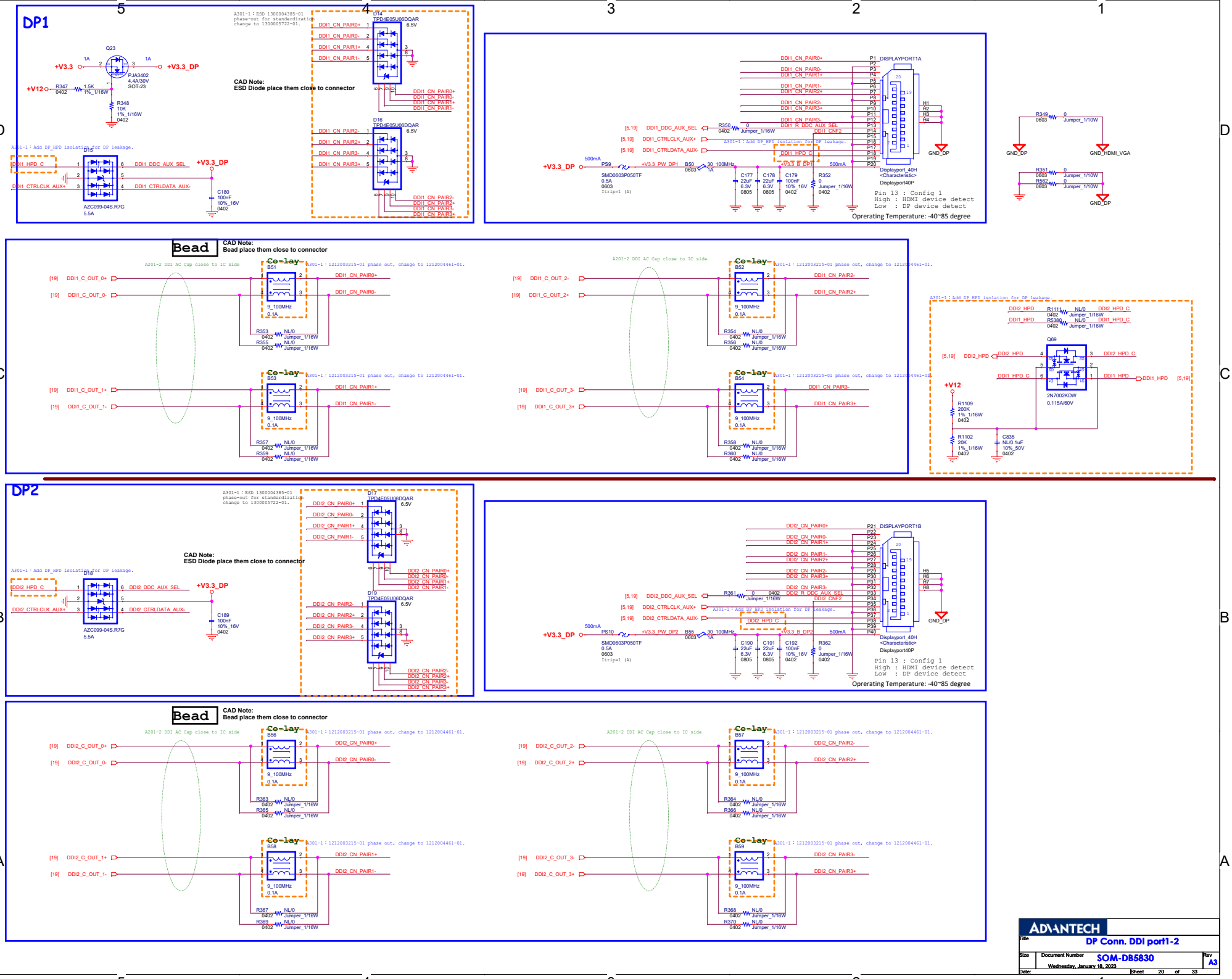
DP1
CAD Note:
ESD Diode place them close to connector
Bead
CAD Note:
Bead place them close to connector
DP2
CAD Note:
ESD Diode place them close to connector
Bead
CAD Note:
Bead place them close to connector
Pin 13 : Config 1
High : HDMI device detect
Low : DP device detect
Oprerating Temperature: -40~85 degree
ADVANTECH
DP Conn. DDI port1-2
SOM-DB5830
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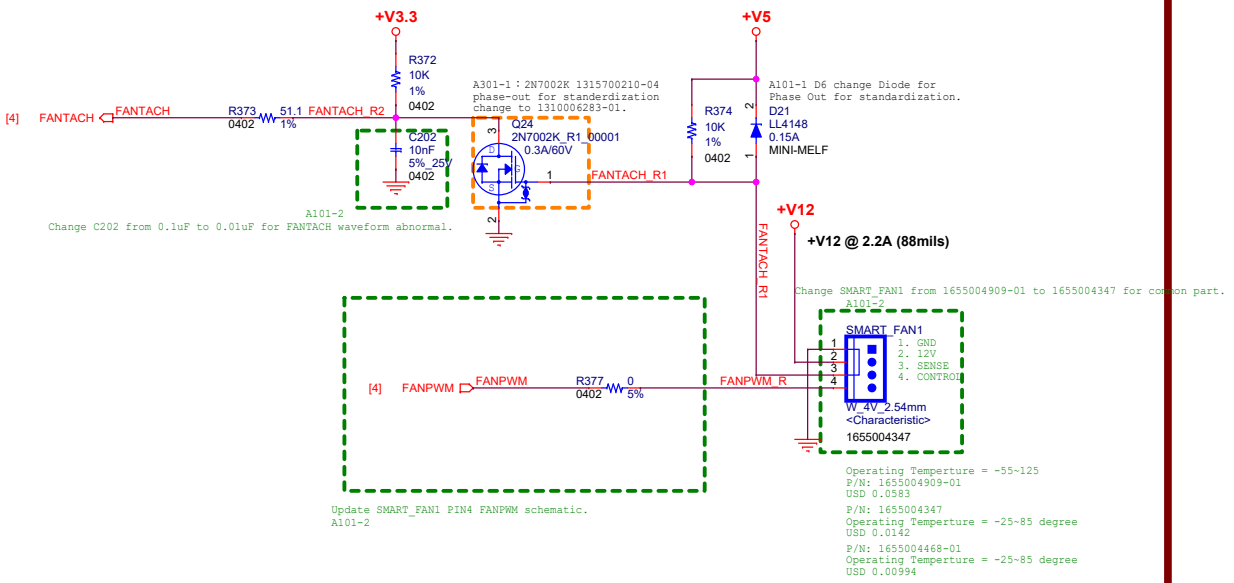
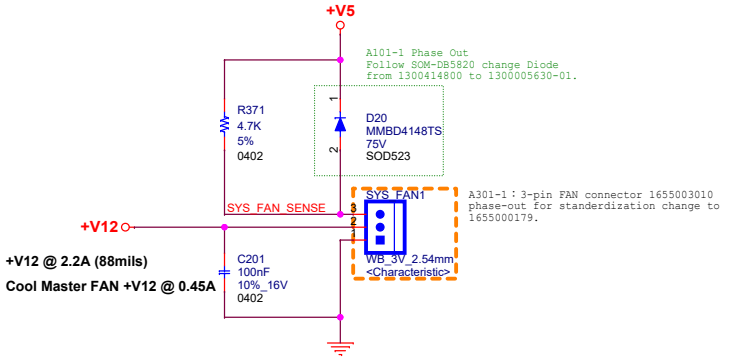
SMART FAN



SYSTEM FAN



ADVANTECH

Title	SYS FAN / SMART FAN	
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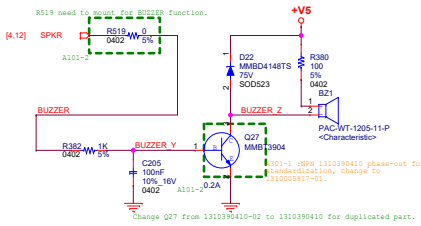
BUZZER



GPIO CONN

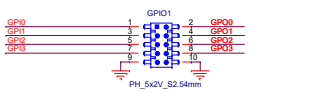
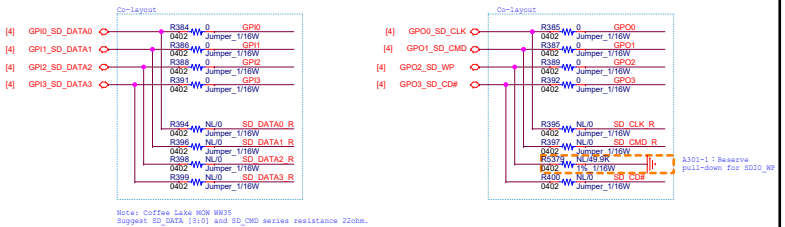


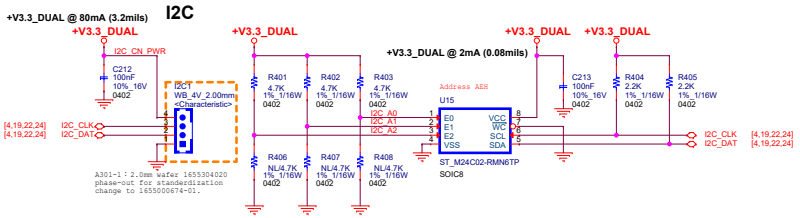
Table 4.30: SD Card Interface Signals

COM Express Signal	SD card interface signals	Comments
GPI0	SD_DATA0	Bidirectional signal
GPI1	SD_DATA1	Bidirectional signal
GPI2	SD_DATA2	Bidirectional signal
GPI3	SD_DATA3	Bidirectional signal
GPO0	SD_CLK	Output from COM Express, input to SD
GPO1	SD_CMD	Output from COM Express, input to SD
GPO2	SD_WP	Input to COM Express when used as SD_WP
GPO3	SD_CD#	Input to COM Express when used as SD_CD#

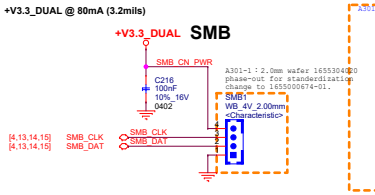
GPIO / SD colay



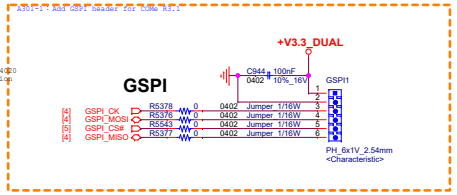
I2C



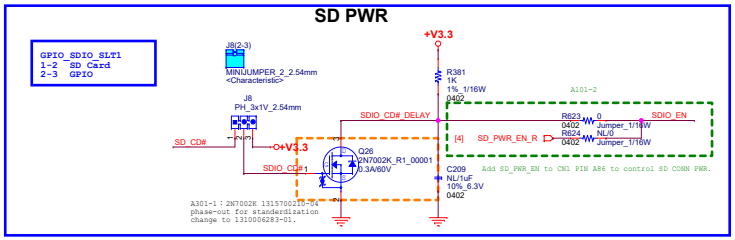
SMB

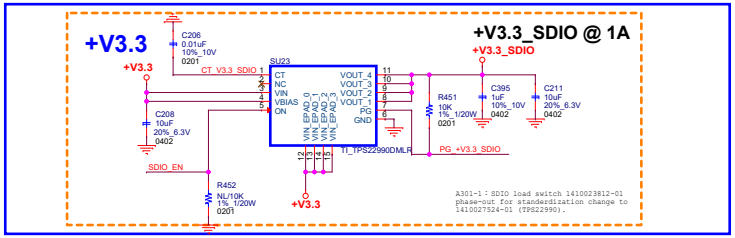


GSPI

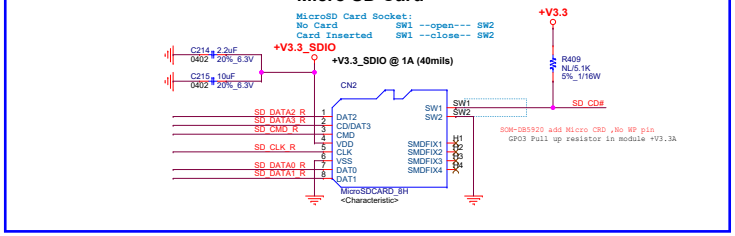


SD PWR





Micro SD Card

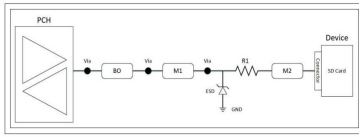


S71006_CFL_MOW_WW38_2017 S7139L_CFL_H_PDG_Rev1p0

6.3.6 CFL U/S/H SDXC Guidelines Change

Description: CFL-U, S and H PCH SDXC guidelines has changed.

Resistor R1 (22 ohms) is added in the below topology diagram to be placed on SD_DATA [3:0] and SD_CMD within 12.7 mm away from the device.



Following PDGs will be updated in the next release.

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Title	GPIO/SMBus/I2C/MicroSD/BZ	
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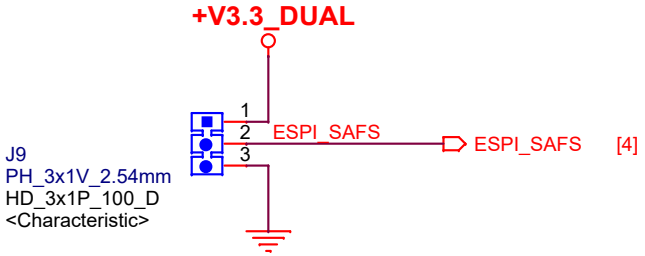
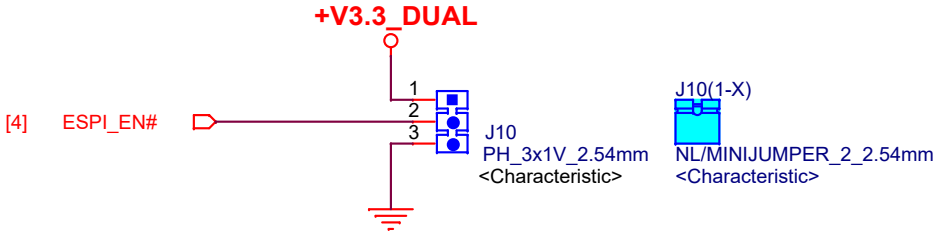
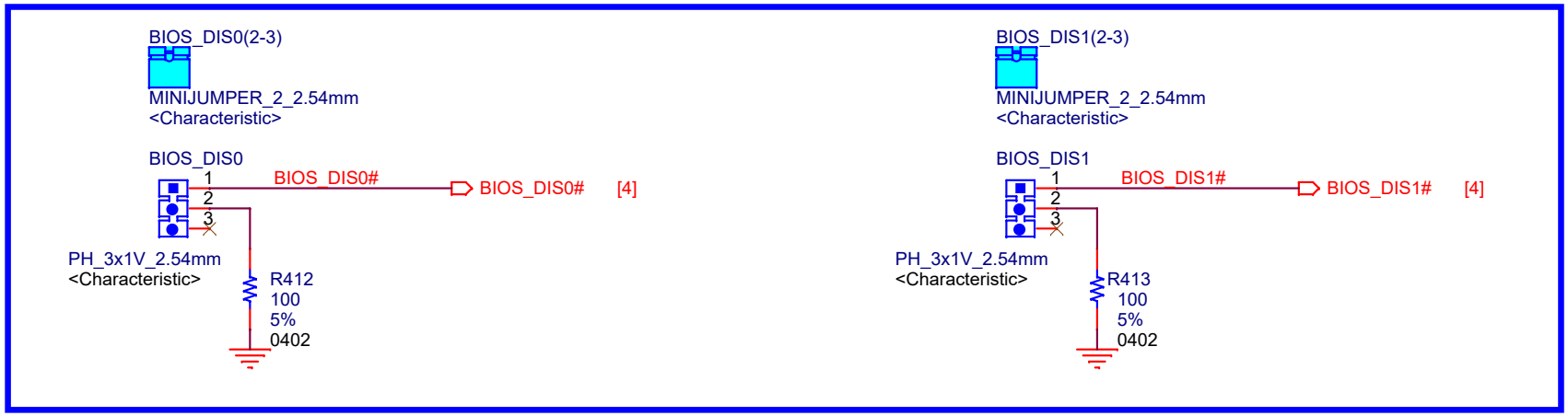
ESPI selection / BIOS selection

For COM.0 R3, the Module Carrier based BIOS options have been expanded to support eSPI devices. A third pin that affects the BIOS location, named ESPI_EN#, works in conjunction with BIOS_DIS1# and BIOS_DIS0# to define the BIOS boot path.





1.The Carrier shall leave the ESPI_EN# unconnected on the Carrier for LPC operation.
2. The Carrier shall tie ESPI_EN# to GND for eSPI operation.



ADVANTECH

Title	BIOS / eSPI selection	
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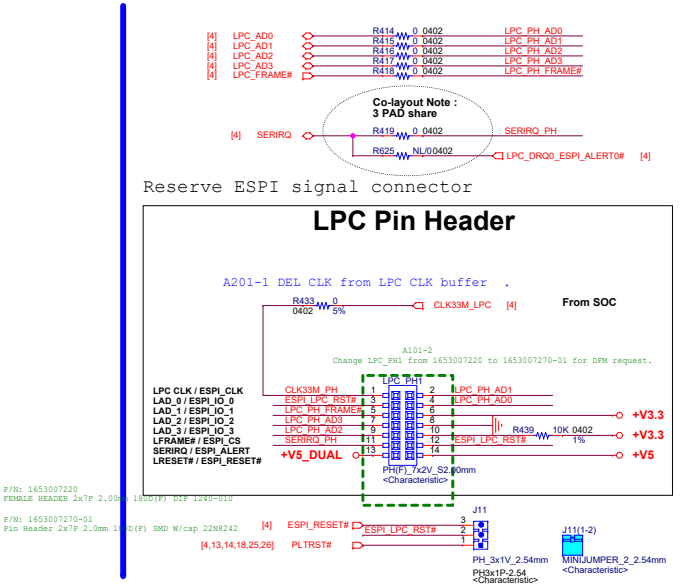
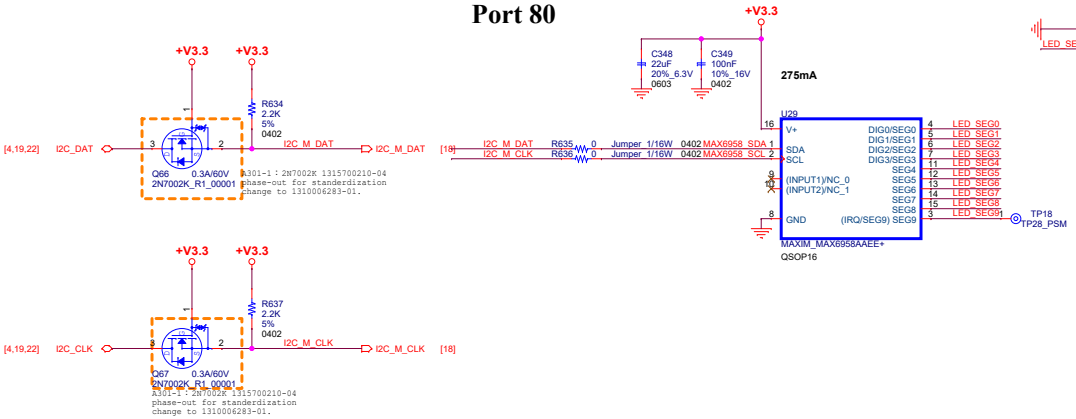
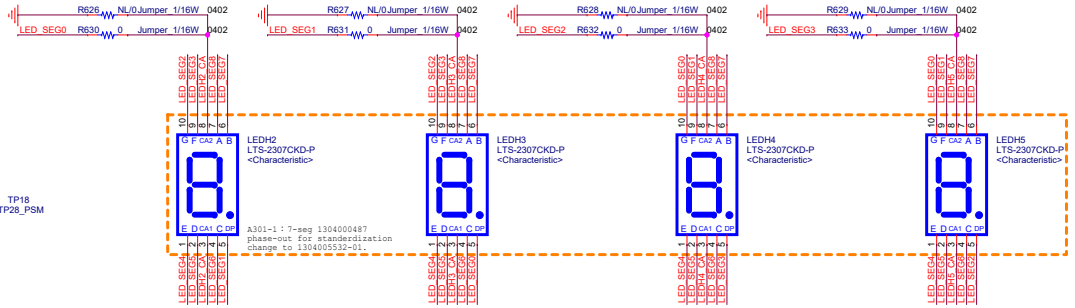
A201-1 DEL LPC to PORT 80
ADD I2C to PORT 80



I2C to PORT 80



A201-1 DEL TPM IC .



Title	Port 80/ LPC PH / TPM		
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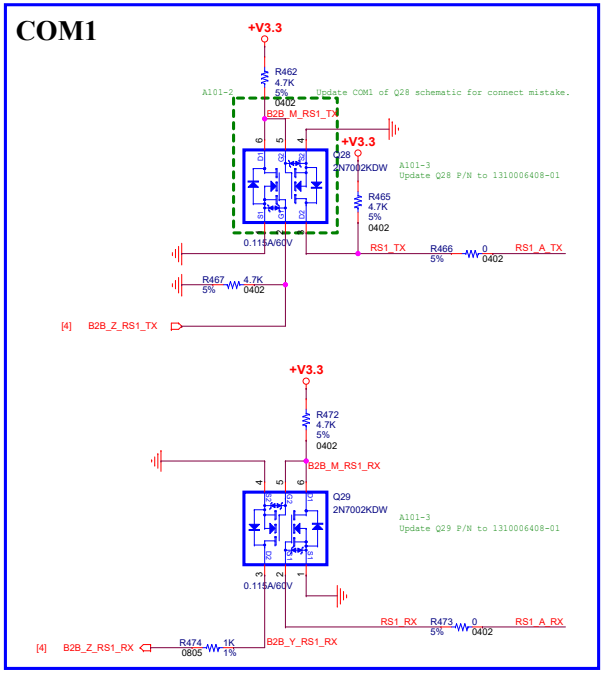
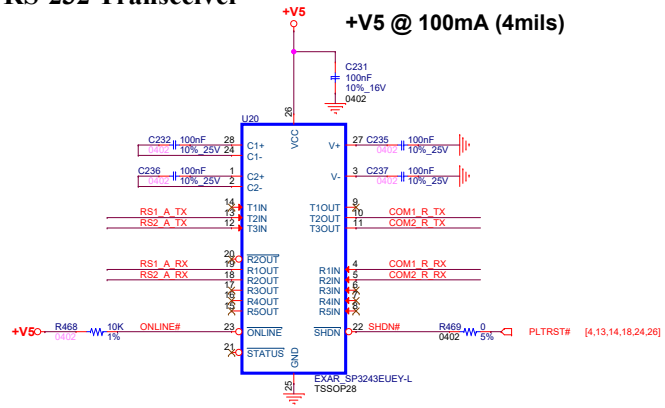
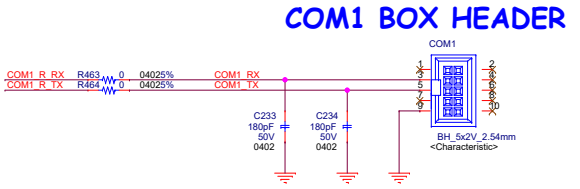
COM1



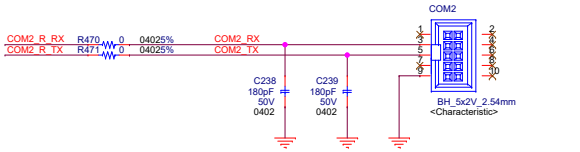
RS-232 Transceiver



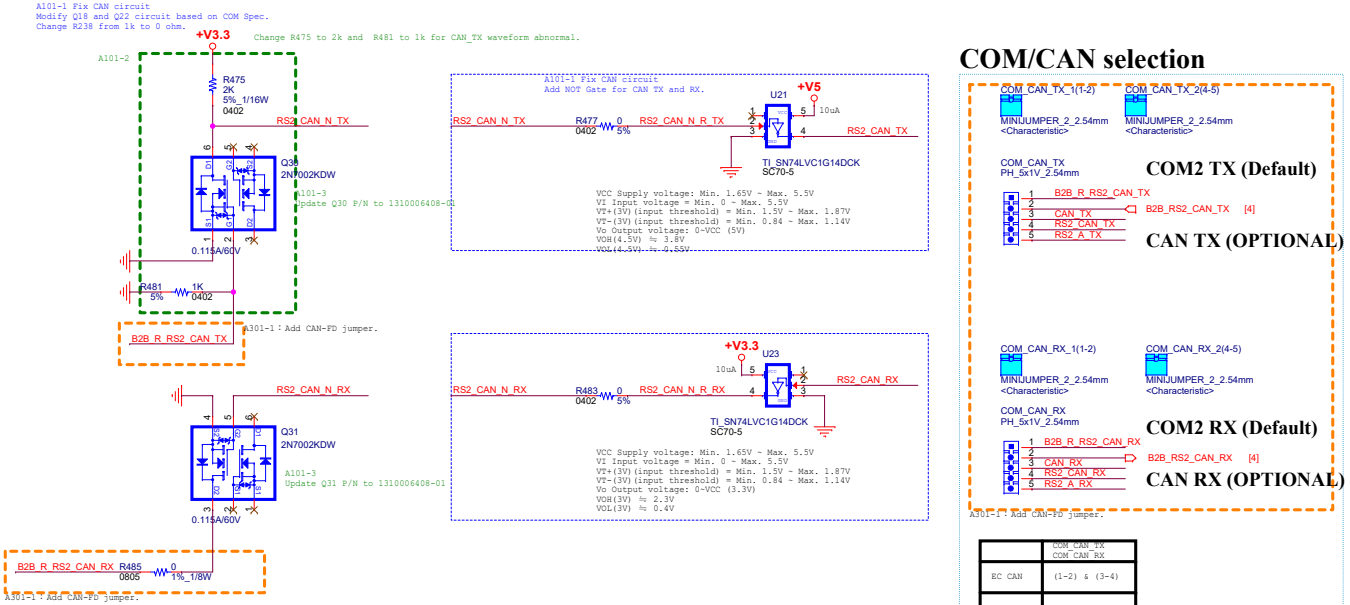
COM1 BOX HEADER



COM2 BOX HEADER



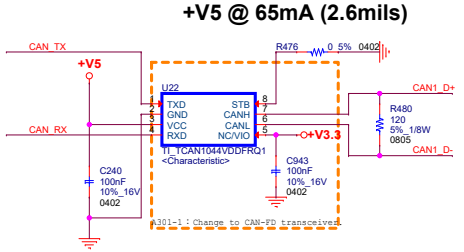
COM2 (Default) / CAN (OPTIONAL)



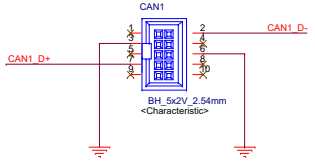
COM/CAN selection

	COM_CAN_TX COM_CAN_RX
EC CAN	(1-2) & (3-4)
EC COM (Default)	(1-2) & (4-5)
CAN FD	(2-3)

CAN Transceiver



CAN BOX HEADER



DE-9

9 Pin (male) D-Sub CAN Bus PinOut

Pin #	Signal names	Signal Description
1	Reserved	Upgrade Path
2	CAN_L	Dominant Low
3	CAN_GND	Ground
4	Reserved	Upgrade Path
5	CAN_SHLD	Shield, Optional
6	GND	Ground, Optional
7	CAN_H	Dominant High
8	Reserved	Upgrade Path
9	CAN_V+	Power, Optional

ADVANTECH

Title	COM Port 1-2 / CAN	
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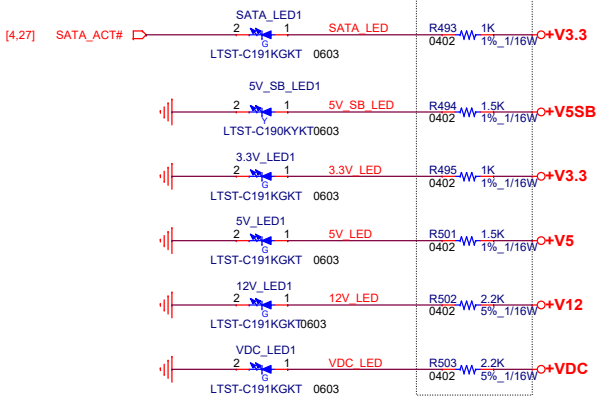
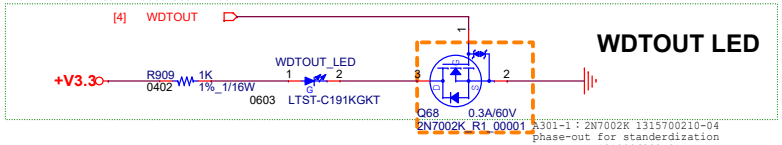
LED

A101-1 20170906
Change R value for each LED brightness.

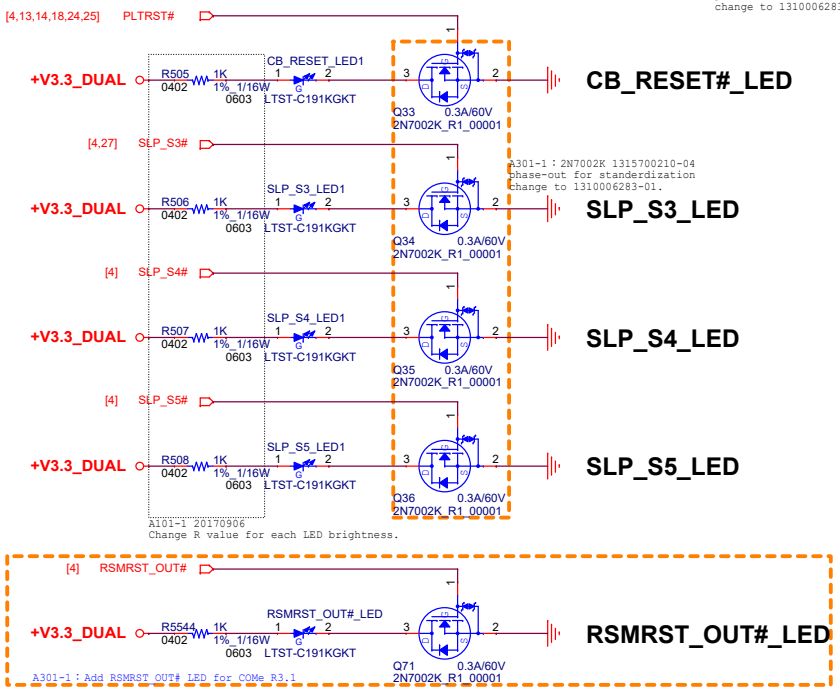


A201-2 Follow SOM-DB5800 add WDTOUT LED



A301-1 : 2N7002K 1315700210-04
phase-out for standerdization
change to 1310006283-01.

A301-1 : 2N7002K 1315700210-04
phase-out for standerdization
change to 1310006283-01.

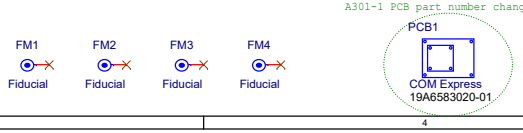


A301-1 : 2N7002K 1315700210-04
phase-out for standerdization
change to 1310006283-01.

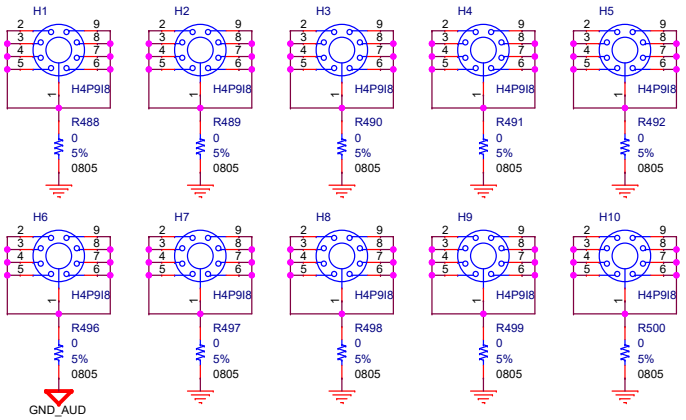
A101-1 20170906
Change R value for each LED brightness.

FM/PCB

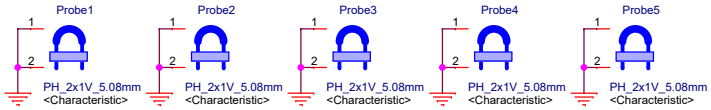
A301-1 PCB part number change to 19A6583020-01



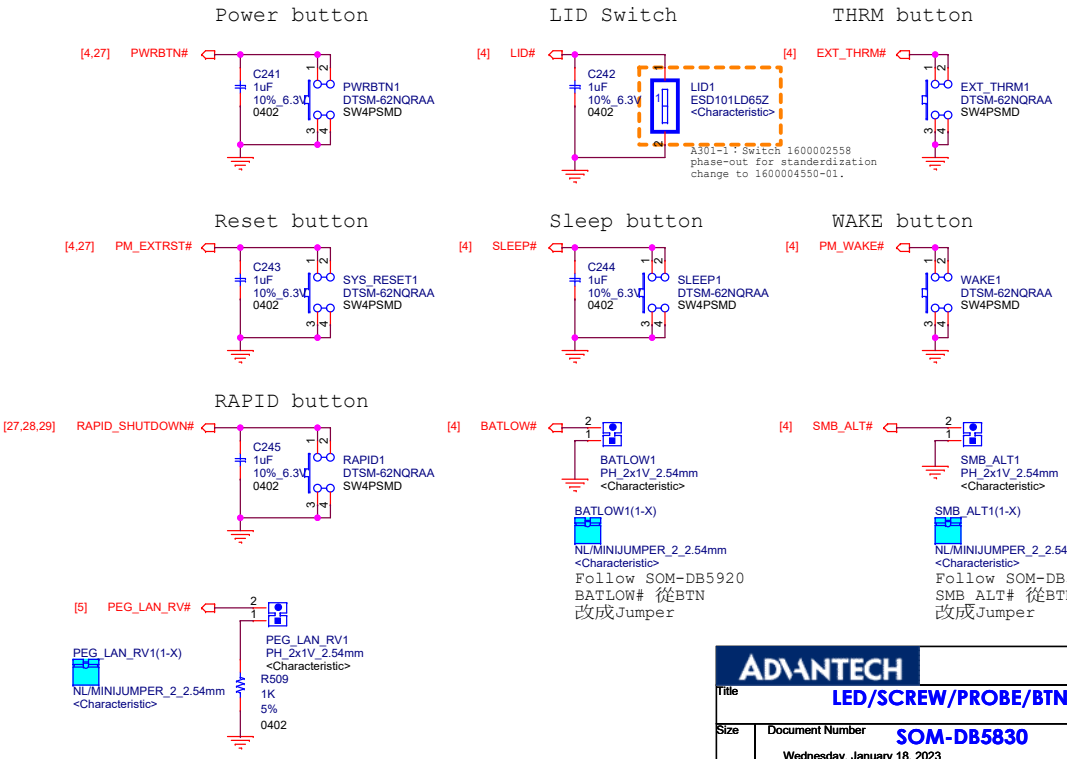
SCREW HOLE



PROBE



Button / Pin Header / Switch



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Title	LED/SCREW/PROBE/BTN/PCB/FM	
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+V12 @ 24A
+V5 @ 15A
+V3.3 @ 20A
+V5SB @ 2.5A

ATX12V POWER

ATX1

ATX_12x2V_4.2mm

-V12 not used

PSON1 Power Setting
1-2 AT Mode
2-3 ATX Mode

Type2#	Type1#	Type0#	COMe R3.0 support Type	SOM-DB5830 remark
X	X	X	Pin-out Type10	Support
NC	NC	NC	Pin-out Type2	Does not support
GND	NC	NC	Pin-out Type6	Support
GND	NC	GND	Pin-out Type7	Does not support

XOR Gate Table

Pin1	Pin2	Out
0	0	0
0	1	1
1	0	1
1	1	0

Add schematic for TYPE2# & TYPE0# select.

Layout note: Placement close ATX1

+V5@16A
24D14 VIA *16

+V5_DUAL@16A
24D14 VIA *16

+V5SB from PWR Supply
+V5SB @ 2.5A
VIA24D14 Via X 3

+V5SB_CB @ 2.5A
VIA24D14 Via X 3

A101-1 20170906
Reserve those pin header after RD internal meeting.

PWRBTN Pin Header

SYS RESET Pin Header

SATA ACT# Pin Header

Power LED Pin Header

文字面標註正極

Title	ATX power / +V5_DUAL
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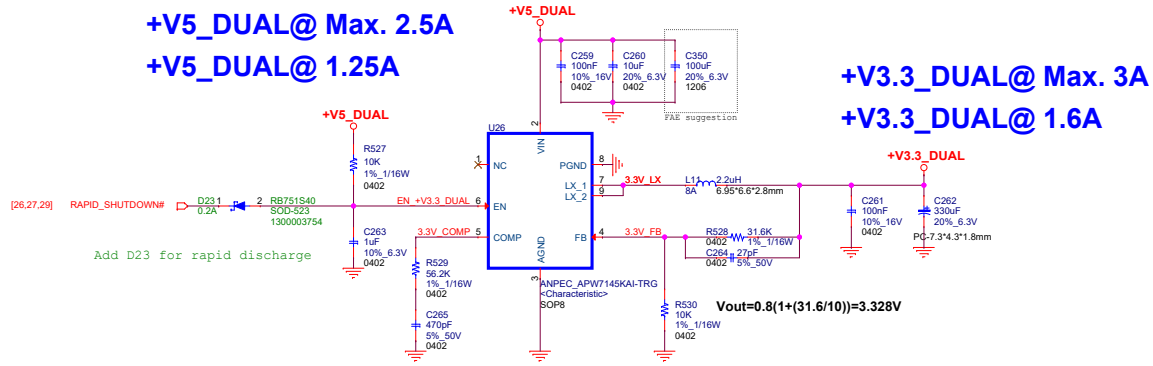

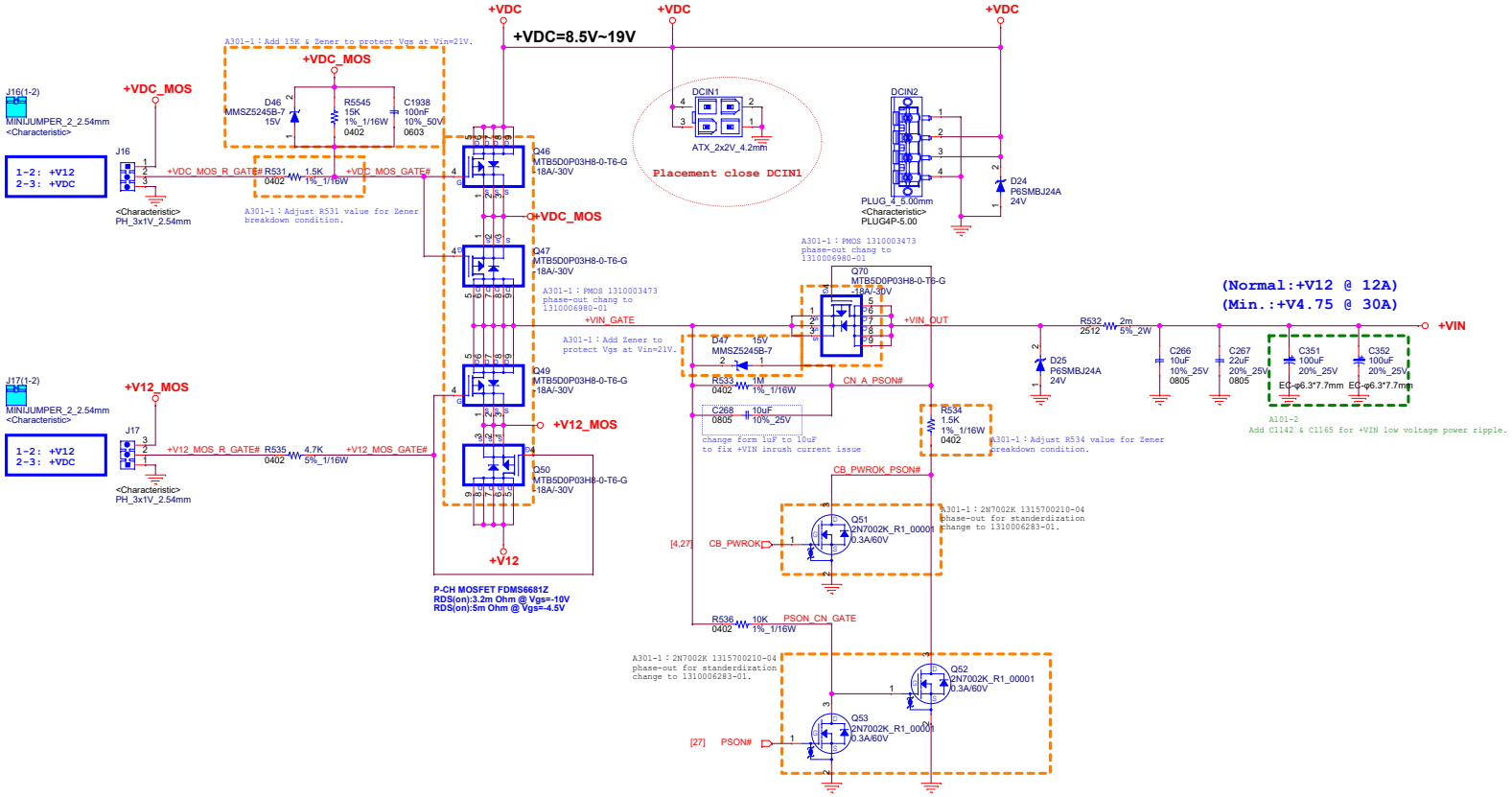

ADVANTECH

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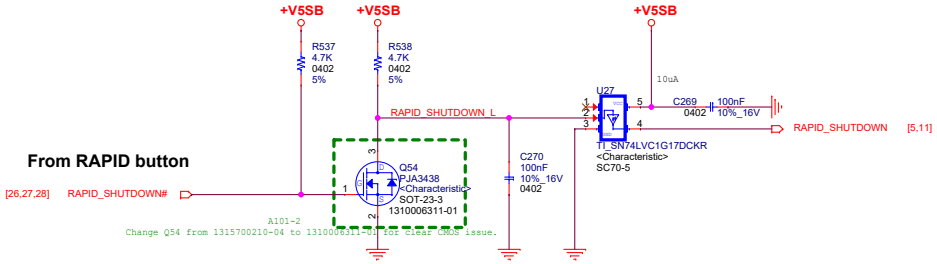
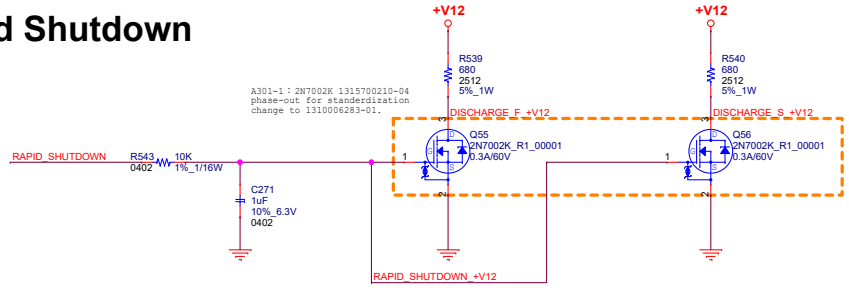
Rapid Shutdown



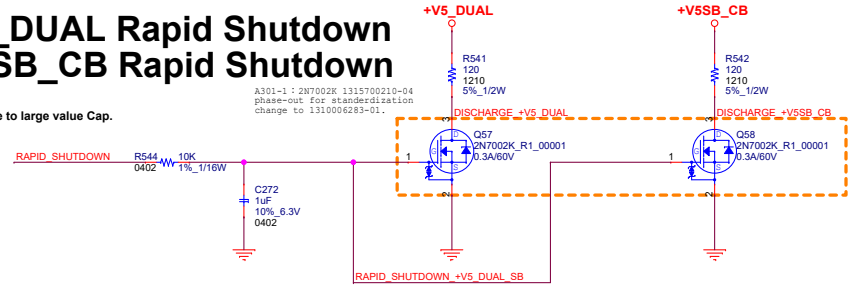
+V12 Rapid Shutdown

CAD Note:
Place close to large value Cap.



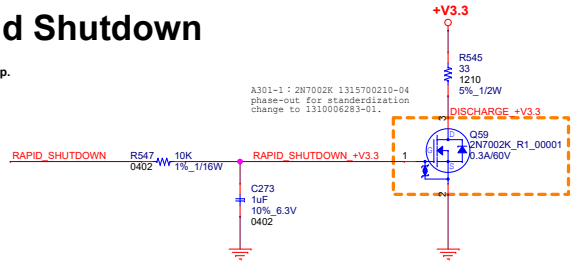
+V5_DUAL Rapid Shutdown
+V5SB_CB Rapid Shutdown

CAD Note:
Place close to large value Cap.



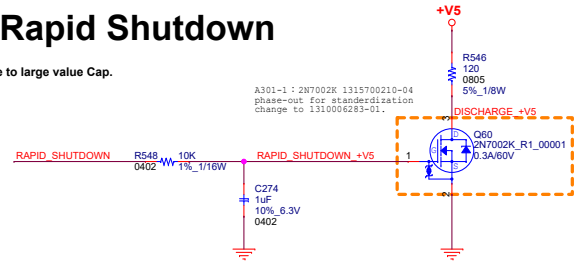
+V3.3 Rapid Shutdown

CAD Note:
Place close to large value Cap.



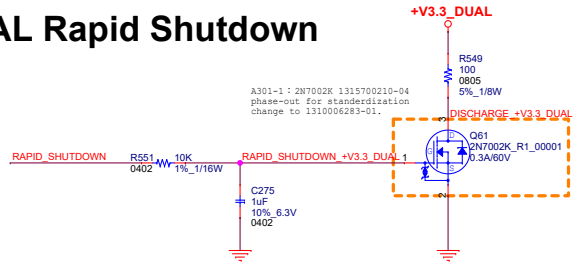
+V5 Rapid Shutdown

CAD Note:
Place close to large value Cap.



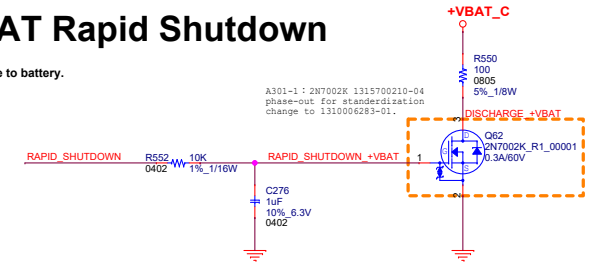
+V3.3_DUAL Rapid Shutdown

CAD Note:
Place close to large value Cap.



+VBAT Rapid Shutdown

CAD Note:
Place close to battery.



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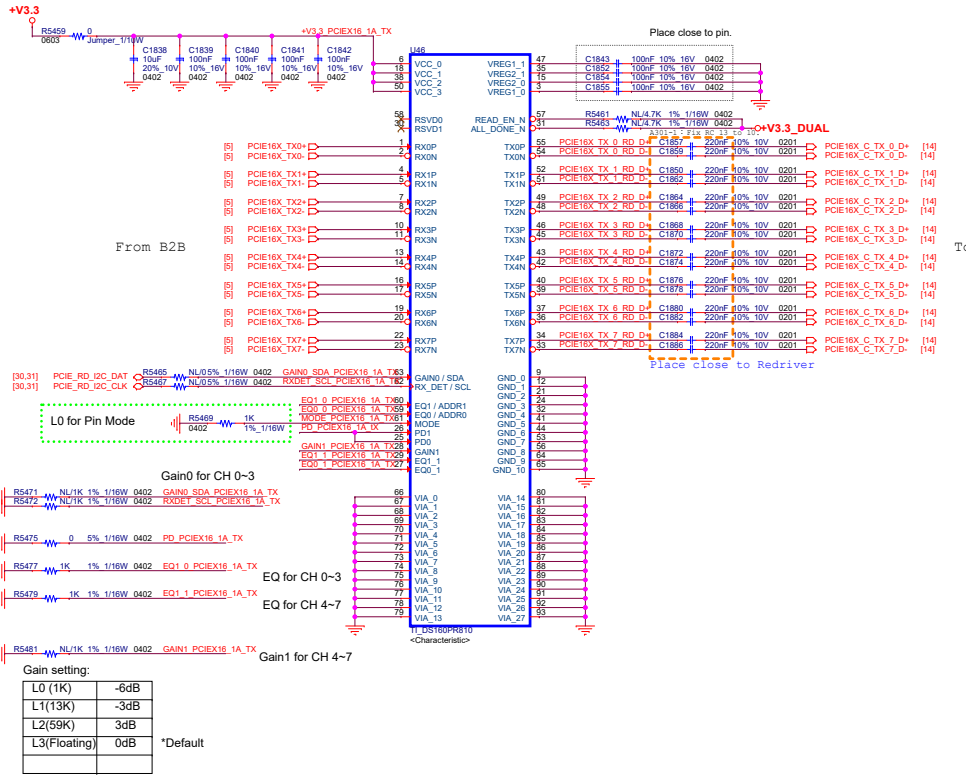
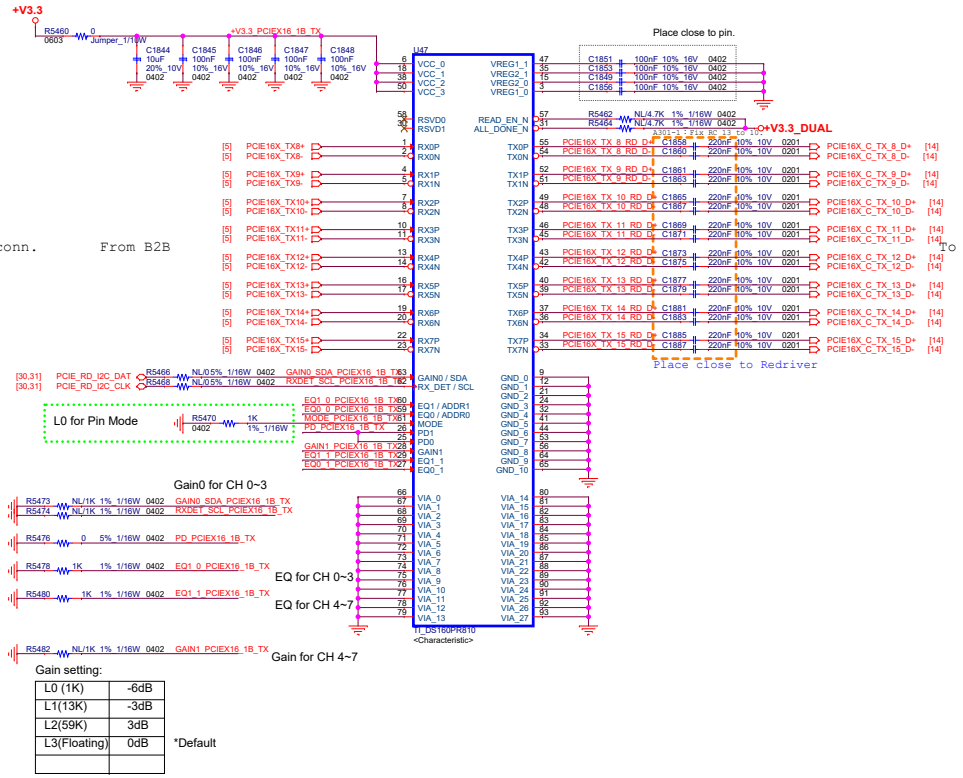
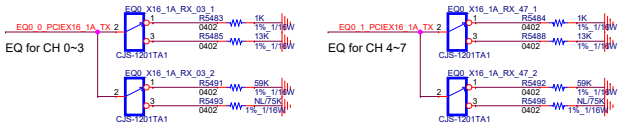
PCIe Redriver for J1 PCIEX16_1 TX

A301-1 : Add re-driver for PCIEX16







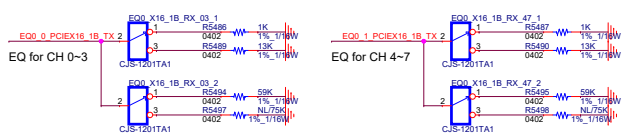


Table 3. 4-Level Control Pin Settings

LEVEL	SETTING
L0	1 kΩ to GND
L1	13 kΩ to GND
L2	59 kΩ to GND
L3	F (Float)

Table 2. Receiver Detect State Machine Settings

PD0	PD1	RX_DET	Channels 0-3 RX Common-mode Impedance	Channels 4-7 RX Common-mode Impedance	COMMENTS
L	L	L0	Always 50Ω	Always 50Ω	PCI Express RX detection state machine is disabled. Recommended for non PCIe interface use case where the DS160PR810 is used as buffer with equalization.
L	L	L1	Pre Detect: Hi-Z Post Detect: 50 Ω.	Pre Detect: Hi-Z Post Detect: 50 Ω.	Outputs polls until 3 consecutive valid detections
L	L	L2	Pre Detect: Hi-Z Post Detect: 50 Ω.	Pre Detect: Hi-Z Post Detect: 50 Ω.	Outputs polls until 2 consecutive valid detections
L	L	L3 (Float)	Pre Detect: Hi-Z Post Detect: 50 Ω.	Pre Detect: Hi-Z Post Detect: 50 Ω.	TX polls every ~150us until valid termination is detected. RX CM impedance held at Hi-Z until detection Reset by asserting PD0/1 high for 200µs then low.
H	L	X	Hi-Z	Reset Channels 0-3 signal path and set their RX impedance to Hi-Z	
L	H	X	Pre Detect: Hi-Z Post Detect: 50 Ω.	Hi-Z	Reset Channels 4-7 signal path and set their RX impedance to Hi-Z
H	H	X	Hi-Z	Hi-Z	

Table 1. Equalization Control Settings

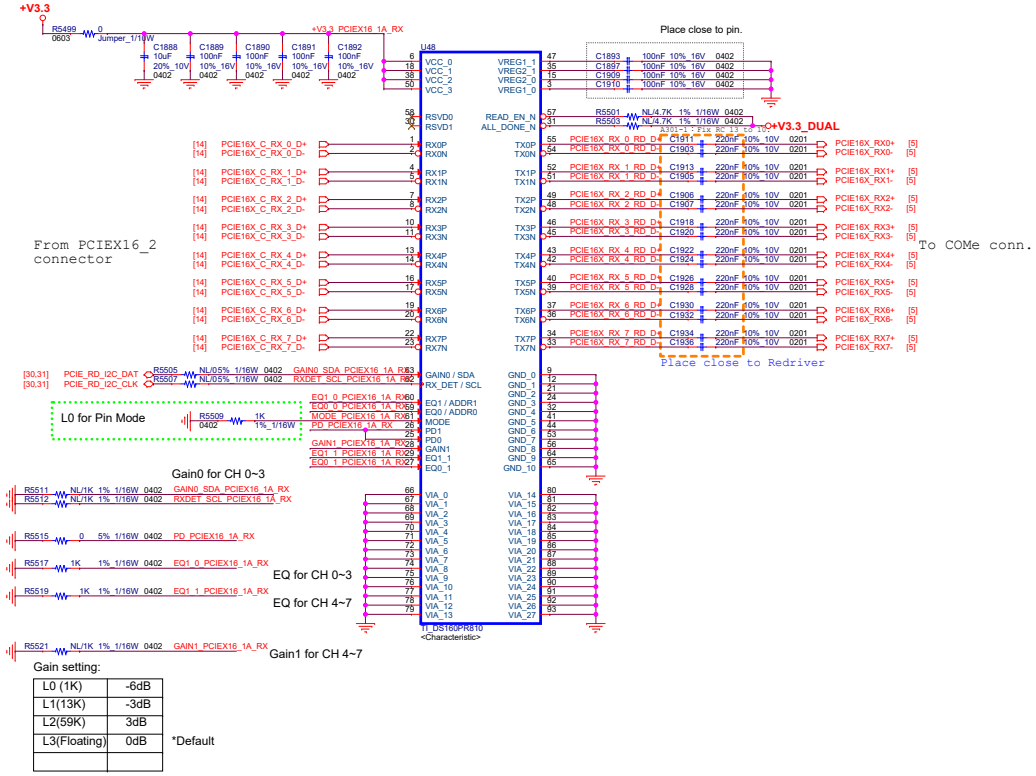
EQUALIZATION SETTING			TYPICAL EQ BOOST (dB)	
EQ INDEX	EQ1_0 (Ch 0-3) / EQ1_1 (Ch 4-7)	EQ0_0 (Ch0-3) / EQ0_1 (Ch 4-7)	@ 4 GHz	@ 8 GHz
0	L0	L0	-0.25	-0.5
1	L0	L1	2.0	4.0
2	L0	L2	2.5	5.0
3	L0	L3	3.0	6.0
4	L1	L0	4.0	7.0
5	L1	L1	4.5	7.5
6	L1	L2	5.0	8.0
7	L1	L3	6.0	9.5
8	L2	L0	7.0	10
9	L2	L1	8.0	11
10	L2	L2	8.5	12.5
11	L2	L3	9.0	13
12	L3	L0	9.5	14.5
13	L3	L1	10.0	15
14	L3	L2	10.5	16
15	L3	L3	12.0	18

Table 4. SMBUS/I2C Slave Address Settings

ADDR1	ADDR0	7-bit Slave Address Channels 0-3	7-bit Slave Address Channels 4-7
L0	L0	0x18	0x19
L0	L1	0x1A	0x1B
L0	L2	0x1C	0x1D
L0	L3	0x1E	0x1F
L1	L0	0x20	0x21
L1	L1	0x22	0x23
L1	L2	0x24	0x25
L1	L3	0x26	0x27
L2	L0	0x28	0x29
L2	L1	0x2A	0x2B
L2	L2	0x2C	0x2D
L2	L3	0x2E	0x2F
L3	L0	0x30	0x31
L3	L1	0x32	0x33
L3	L2	0x34	0x35
L3	L3	0x36	0x37

PCIe Redriver for J1 PCIEX16_1 RX

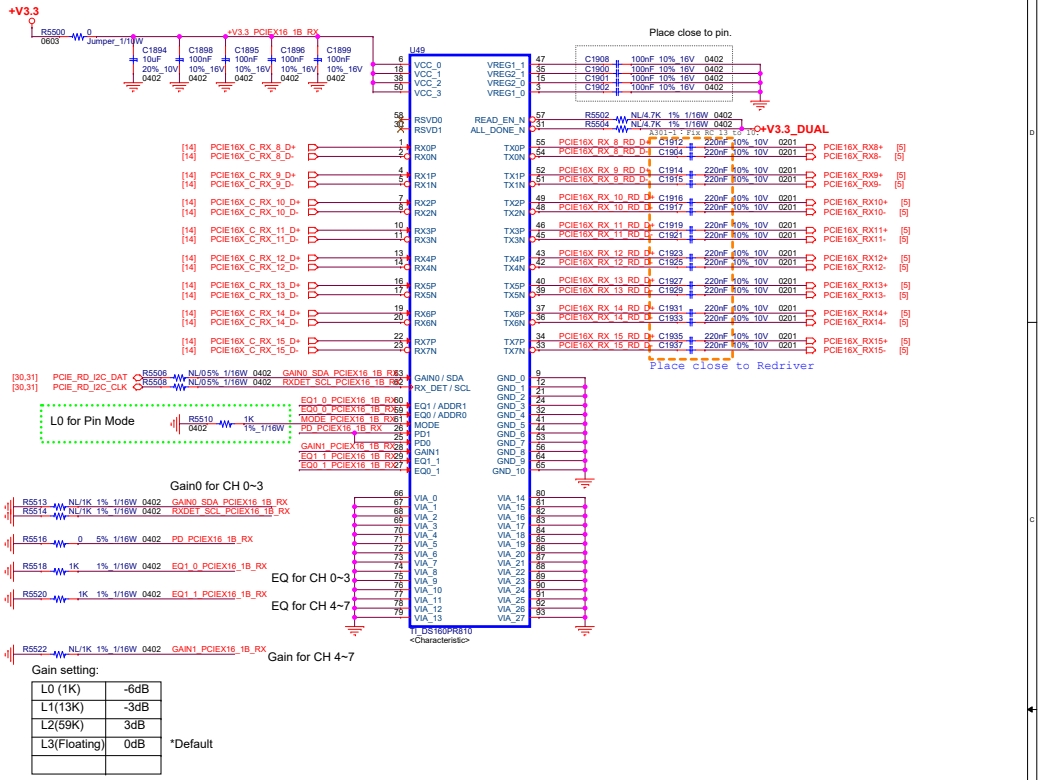
A301-1 : Add re-driver for PCIEX16



Gain setting:

L0 (1K)	-6dB
L1(13K)	-3dB
L2(59K)	3dB
L3(Floating)	0dB

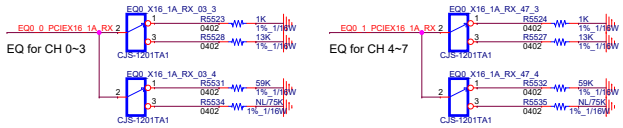
*Default



Gain setting:

L0 (1K)	-6dB
L1(13K)	-3dB
L2(59K)	3dB
L3(Floating)	0dB

*Default



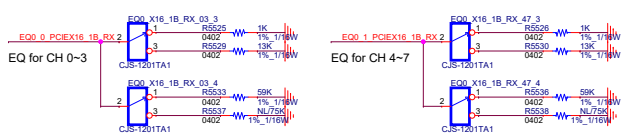


Table 3. 4-Level Control Pin Settings

LEVEL	SETTING
L0	1 kΩ to GND
L1	13 kΩ to GND
L2	59 kΩ to GND
L3	F (Float)

Table 2. Receiver Detect State Machine Settings

PD0	PD1	RX_DET	Channels 0-3 RX Common-mode Impedance	Channels 4-7 RX Common-mode Impedance	COMMENTS
L	L	L0	Always 50Ω	Always 50Ω	PCI Express RX detection state machine is disabled. Recommended for non PCIe interface use case where the DS160PR810 is used as buffer with equalization.
L	L	L1	Pre Detect: Hi-Z Post Detect: 50 Ω.	Pre Detect: Hi-Z Post Detect: 50 Ω.	Outputs polls until 3 consecutive valid detections
L	L	L2	Pre Detect: Hi-Z Post Detect: 50 Ω.	Pre Detect: Hi-Z Post Detect: 50 Ω.	Outputs polls until 2 consecutive valid detections
L	L	L3 (Float)	Pre Detect: Hi-Z Post Detect: 50 Ω.	Pre Detect: Hi-Z Post Detect: 50 Ω.	TX polls every ~150us until valid termination is detected. RX CM impedance held at Hi-Z until detection Reset by asserting PD0/1 high for 200µs then low.
H	L	X	Hi-Z	Pre Detect: Hi-Z Post Detect: 50 Ω.	Reset Channels 0-3 signal path and set their RX impedance to Hi-Z
L	H	X	Pre Detect: Hi-Z Post Detect: 50 Ω.	Hi-Z	Reset Channels 4-7 signal path and set their RX impedance to Hi-Z
H	H	X	Hi-Z	Hi-Z	

Table 1. Equalization Control Settings

EQUALIZATION SETTING			TYPICAL EQ BOOST (dB)	
EQ INDEX	EQ1_0 (Ch 0-3) / EQ1_1 (Ch 4-7)	EQ0_0 (Ch0-3) / EQ0_1 (Ch 4-7)	@ 4 GHz	@ 8 GHz
0	L0	L0	-0.25	-0.5
1	L0	L1	2.0	4.0
2	L0	L2	2.5	5.0
3	L0	L3	3.0	6.0
4	L1	L0	4.0	7.0
5	L1	L1	4.5	7.5
6	L1	L2	5.0	8.0
7	L1	L3	6.0	9.5
8	L2	L0	7.0	10
9	L2	L1	8.0	11
10	L2	L2	8.5	12.5
11	L2	L3	9.0	13
12	L3	L0	9.5	14.5
13	L3	L1	10.0	15
14	L3	L2	10.5	16
15	L3	L3	12.0	18

Table 4. SMBUS/I2C Slave Address Settings

ADDR1	ADDR0	7-bit Slave Address Channels 0-3	7-bit Slave Address Channels 4-7
L0	L0	0x18	0x19
L0	L1	0x1A	0x1B
L0	L2	0x1C	0x1D
L0	L3	0x1E	0x1F
L1	L0	0x20	0x21
L1	L1	0x22	0x23
L1	L2	0x24	0x25
L1	L3	0x26	0x27
L2	L0	0x28	0x29
L2	L1	0x2A	0x2B
L2	L2	0x2C	0x2D
L2	L3	0x2E	0x2F
L3	L0	0x30	0x31
L3	L1	0x32	0x33
L3	L2	0x34	0x35
L3	L3	0x36	0x37

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SOM-DB5830 A1 01-1 PCB:19A6583000-01, 96 BOM:96965830000 Date: 2017/10/13

SOM-DB5830 A1 01-2 PCB:19A6583001-01, 96 BOM:96965830000 Date: 2018/03/26

PG21: R519 need to mount for BUZZER function.
PG20: Change SMART_FAN1 from 1655004909-01 to 1655004347 for common part.
PG27: Add C1142 & C1165 for +VIN low voltage power ripple.
PG17: Change component at PG17 for LVDS sequence.
PG18: Correct name error from SW_HMDI_EQ1 to SW_HDMI_EQ1.
PG04: change J1 from 1653006504-01 to 1653002200 for duplicated part.
PG20: Update SMART_FAN1 PIN4 FANPWM schematic.
PG20: Change C202 from 0.1uF to 0.01uF for FANTACH waveform abnormal.
PG24: Update COM1 of Q28 schematic for connect mistake.
PG24: Change R475 to 2k and R481 to 1k for CAN_TX waveform abnormal.
PG11: Change SATA1~SATA4 from 1654005955 to 1654013393-01 for DFM request.
PG11: Update schematic for two SPI BIOS ROM support.
PG11: Add J3(1-2) jumper for two SPI BIOS ROM support.
PG21: Add SD_PWR_EN to CN1 PIN A86 to control SD CONN PWR.
PG26: Add schematic for TYPE2# & TYPE0# select.
PG15: Swap U7 SMB_M_CLK and SMB_M_DAT for connect mistake.
PG17: Change R2033 from +V3.3 to +V5_DUAL for +VLVDS_PANEL_PWR discharge.
PG17: Change R2034 from 1.2Kohm to 52.3ohm for +VLVDS_PANEL_PWR discharge.
PG23: Change TPM(U19) from 1410028322-01(FW5.61) to 1410028322-11(FW5.62).
PG23: Change R459 from 33k to 4.7k for FAE recommend.
PG23: Change LPC_PH1 from 1653007220 to 1653007270-01 for DFM request.
PG17: Reserve cap at LVDS signals for SI and remove Common Mode Choke.
PG09: Change HW Strap setting of equalization and flat gain for USB3.1 GEN2 TX.
PG21: Change Q27 from 1310390410-02 to 1310390410 for duplicated part.
PGXX: Change 2N7002 from 1315700214 to 1315700214-01 for part shortage issue.
PG06: Reserve Common Mode Choke co-layout for USB3.1 RX Port 0/1 signal.
PG07: Reserve Common Mode Choke co-layout for USB3.1 RX Port 2/3 signal.
PG10: Change USB20 port 4~7 Common Mode Choke from 1212003587-01 to 1212001302.
PG06: Change USB20 port 0/1 Common Mode Choke from 1212003587-01 to 1212001302.
PG07: Change USB20 port 2/3 Common Mode Choke from 1212003587-01 to 1212001302.
PG10: Change USB20 CONN USB2.0_1 from 1654012279-01 to 1654009643.
PG29: Change C84/C85/C88/C89 from X7R 4.7uF 10% 10V SMD 0805 to X5R 4.7uF 10% 25V SMD 0603 for capacitance shortage issue.

PG17: Unmount C155 for LVDS sequence.
PG28: Change Q54 from 1315700210-04 to 1310006311-01 for clear CMOS issue.

SOM-DB5830 A101-3 PCB:19A6583002-01, 96 BOM:96965830000 Date: 2018/10/03

PG6: Change re-driver USB3.1 port 0/1.
PG7: Change re-driver USB3.1 port 2/3.
PG8: Change re-driver USB3.1 port 0/1.
PG9: Change re-driver USB3.1 port 2/3.

SOM-DB5830 A101-4 PCB:19A6583003-01, 96 BOM:96965830000 Date: 2019/05/09

PGXX: Exchange SOM-AB1 and SOM-CD1 location at layout board file.

SOM-DB5830 A201-1 PCB:19A6583010-01, 96 BOM:96965830010 Date: 2020/05/07

PG04: change pin header for phase out for standardization
PG05: change to 16G COM E connector
PG06: change to 2.5G LAN connector
PG11: change to 2 BIOS socket SOT&QFN
PG13: change to GEN4 SLOT
PG14: change to GEN4 SLOT
PG15: change to use Gen4 clock buffer
PG18: Change to HDMI2.0 spec
PG23: DEL LPC to PORT 80, ADD I2C to PORT 80, DEL TPM IC .

SOM-DB5830 A201-2 PCB:19A6853011-01 96 BOM:96965830010 Date: 2020/10/20

PG19: Add U32/U33 DP Re-driver for Display 8.1Gbps.
PG26: Add WDTOUT LED design for EC requirement. Update PCB part number.
PG17: Change LVDS1 connector from 1653006918-01 to 1655005384-01 and modify pin define.
PG06: USB3.1 description change to USB3.2.
PG07: USB3.1 description change to USB3.2.
PG11: BH1 change to 1760000571 for phase out component.

SOM-DB5830 A201-2 PCB:19A6583012-01 96 BOM:96965830010 Date: 2022/12/5

PG14, PG30, PG31: Add PCIE Gen4 re-driver.

PG04: Change R11, R15 pull-up to +V3.3_DUAL

PG25: U22 Change to CAN-FD transceiver. (1410030897-01)

PG27: U25 VCC pin change to +V3.3_DUAL

PG22: Reserve pull-down for SDIO_WP. (R5379)

PG20: Add DP_HPD isolation for DP leakage.

PG04: Add RSMRST_OUT# for COMe R3.1

PG06, 07, 10: Change to USB load switch for COMe 3.1 RSMRST_OUT# requirement.

PG06: Add ESD for LAN port.

PG25: Add jumper for CAN-FD.

PG08, PG09: Change Re-driver to Pericom PERICOM_PI3EQX1004B1ZHEX (1410028782-01)

PG19, PG08, PG09: Change EQ setting to switch.

PG17: Change LVDS connector pinout for SI pinout.

PG20: DP common mode chock 1212003215-01 phase out, change to 1212004461-01.

PG11: 2.0mm jumper 1653005287-01 phase-out, change to 1653008397-01

PG06, PG07: USB3 Gen2 common mode chock 1212004051-01 phase-out change to 1212004724-01

PG18: HDMI common mode chock 1212003215-01 phase-out change to 1212004461-01

PG28: PMOS 1310003473 phase-out change to 1310006980-01

PG11: NMOS 1315033500 phase-out chang to 1310005735-01

PG27: Fix RC 13 to 10.

PG24: 7-seg 1304000487 phase-out for standerdization change to 1304005532-01.

PG22: 2.0mm wafer 1655304020 phase-out for standerdization change to 1655000674-01.

PG18, PG20: ESD 1300004385-01 phase-out for standerdization change to 1300005722-01.

PG26: Switch 1600002558 phase-out for standerdization change to 1600004550-01.

PG22 :SDIO load switch 1410023812-01 phase-out for standerdization change to 1410027524-01 (TPS22990).

PG15, PG16, PG17, PG20, PG21, PG22, PG24, PG26, PG27, PG28, PG29 :
2N7002K 1315700210-04 phase-out for standerdization change to 1310006283-01.

PG13 :PCIE x4 connector 1654014052-01 phase-out for standerdization change to 1654014054-02.

PG12 :Remoce SPDIF connector.

PG04, PG05 :Change COMe symbol to rev 3.1

PG26 :Add RSMRST_OUT# LED for COMe R3.1

PG14 :Change to PCIE Gen5 connector

PG22 :Add GSPI connector

PG22 :NPN 1310390410 phase-out for standardization, change to 1310005817-01.

PG28 :Add 15K & Zener to protect Vgs at Vin=21V.

PG28 :Adjust R531, R534 value for Zener breakdown condition.

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