Product Introduction

Anritsu

MG3681A

Digital Modulation Signal Generator

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Digital Modulation Signal Generator

Product Introduction

Anritsu Corporation

December 2009 Ver 10.0

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Product outline

- Product outline
- Feature
- Application
- Option

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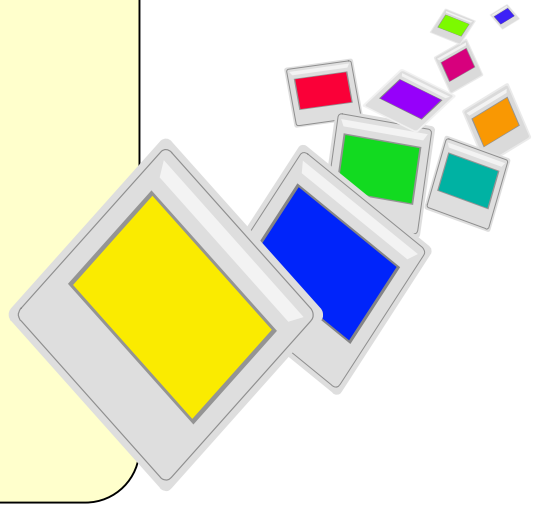


For evaluating Base station, Mobile phone and Components for high-speed and wideband digital mobile communications systems

The digital mobile communications systems are evolved to higher speed and wider band.

- The interference to other systems of adjacent frequency band and the adjacent channel of the same system is minimized, and the modulation type with efficient transmission is adopted, in order to communicate at higher speed in the limited frequency resources.

- **This signal generator that performed excellent adjacent channel leakage power ratio, wideband/high-accuracy vector modulation and various basebands is utilizable for the evaluation of high-speed digital mobile communications equipment and components in future.**

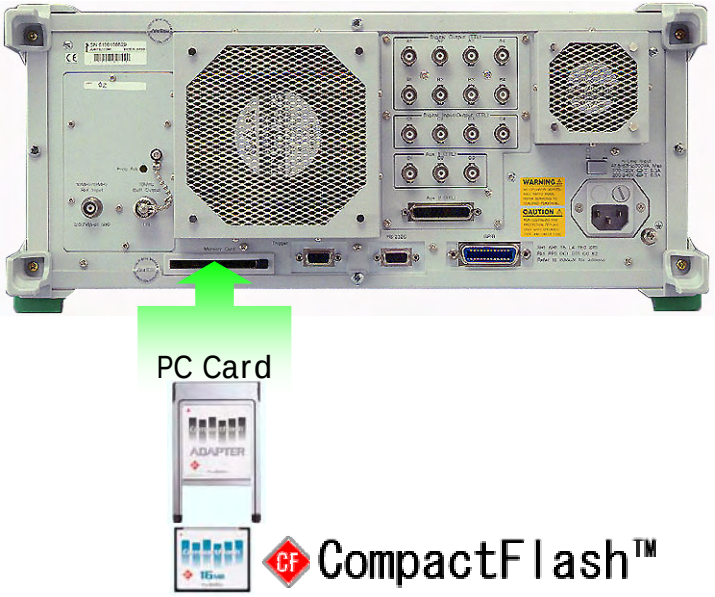
For evaluating Base station, Mobile phone and Components for high-speed and wideband digital mobile communications systems

- **The sensitivity(demodulation) test of base station and mobile phone receivers needs to be evaluated by wanted signal generator. Also, the receiver interference test needs to be evaluated by interference signal generator and wanted signal generator.**

- **Path characteristics and distortion of the components such as power amplifier, RF module and baseband need to be evaluated by signal generator and signal analyzer.**

Almighty support to 3G mobile communications systems (Product concept)

- **Excellent expansible platform**
  - » Various modulation signals and AWGN are outputted by installing required expansion unit for baseband.
  - » Due to the main logic circuit of expansion unit which consists of reconfigurable FPGA(Field Programmable Gate Array), users can upgrade easily by downloading the firmware including FPGA circuit data and DSP(Digital Signal Processor) program in the expansion unit.



Almighty support to 3G mobile communications systems (Product concept)

- **Successor of MG3670 series Signal Generator for second generation mobile communications systems**
  - » 4/5 downsizing
  - » 20% cost down

MG3681A (250k~3GHz)
Digital and Analog modulation
30MHz wideband vector modulation

MG3670 series (300k~2.75GHz)
Released in 1993, greatly contributed to the digitizing of mobile communication systems

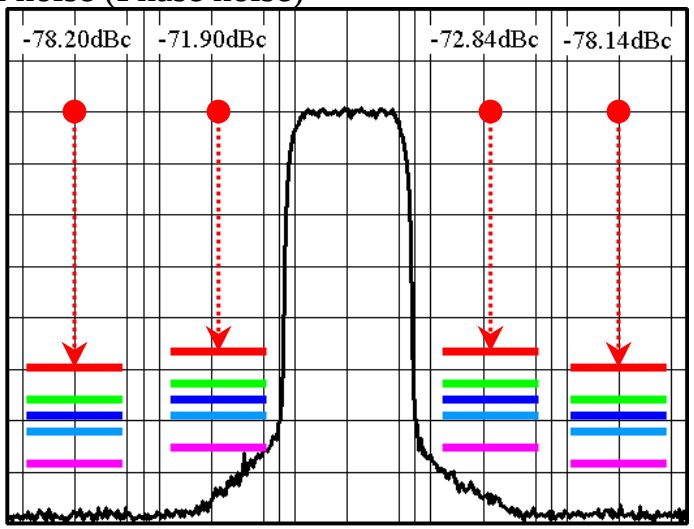
MG3641/42A (125k~2.08GHz)

Excellent analog basic performance (Product concept)

- **Adjacent Channel Leakage Power Ratio**

  In W-CDMA system, the adjacent channel leakage power ratio must be minimized in order to reduce the interference to adjacent PHS system. Extremely low adjacent channel leakage power ratio is required especially for TX power amplifier of BTS. The measurement of adjacent channel leakage power ratio of TX power amplifier requires excellent adjacent channel leakage power ratio of signal source.

  – -68 dBc/3.84MHz typ. : 5MHz offset
    - Due to Intermodulation distortion
  – -75 dBc/3.84MHz typ. : 10MHz offset
    - Due to Residual noise (Phase noise)



BS ACLR minimum requirement
BS ACLR manufacture target (e.g. -6 dB)
TX amplifier minimum requirement (e.g. -9 dB)
TX amplifier manufacture target (e.g. -12 dB)
Signal source minimum requirement (e.g. -16 dB)

Excellent analog basic performance (Product concept)

- **Output level resolution**
  - 0.01 dB : at all level range

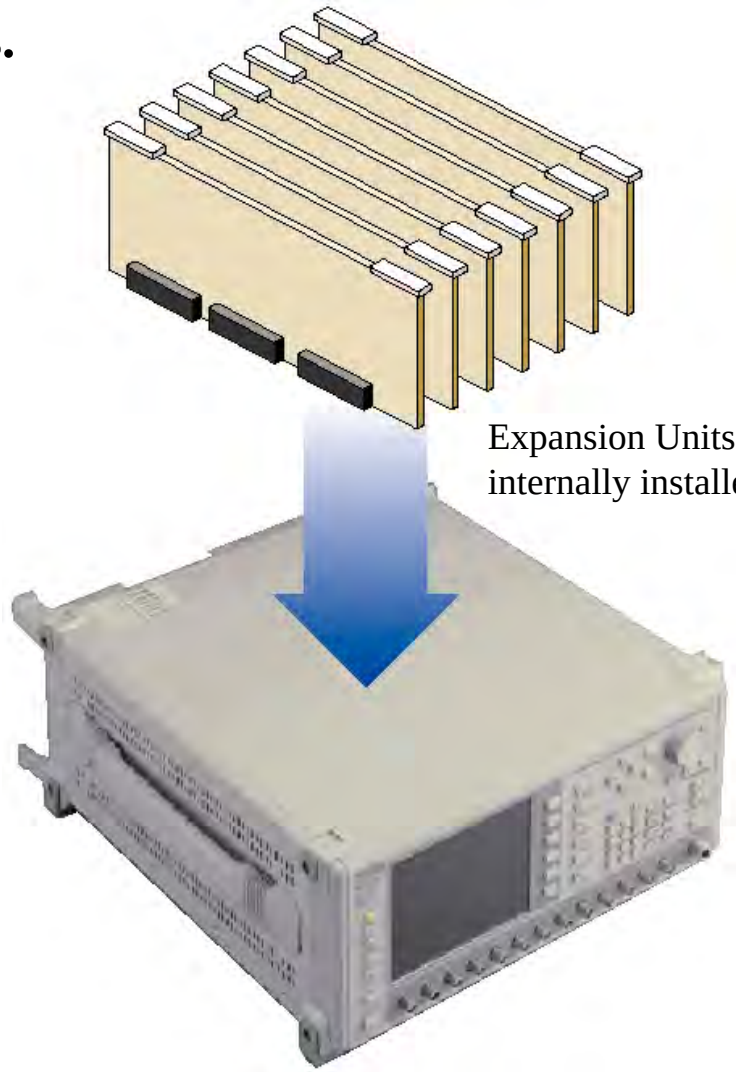
Useful for fine level adjustment in components test and level calibration by power meter.

Various expansion unit

The Platform with Excellent Expandability

Expansion Units is installable up to seven slots.

Expansion unit	Software
MU368010A TDMA Modulation Unit	MX368011A PDC Software
	MX368012A GSM Device Test Software
MU368040A CDMA Modulation Unit	MX368041B W-CDMA Software
	MX368042A IS-95 Device Test Software
MU368030A Universal Modulation Unit	MX368031A Device Test Signal Generation Software
	MX368033A CDMA2000 1xEV-DO Signal Generation Software
	MX368034A PDC Packet Software
	MX368035A PHS Generation Software
MU368060A AWGN Unit	



Expansion Units are internally installed.

Expansion Unit and Software

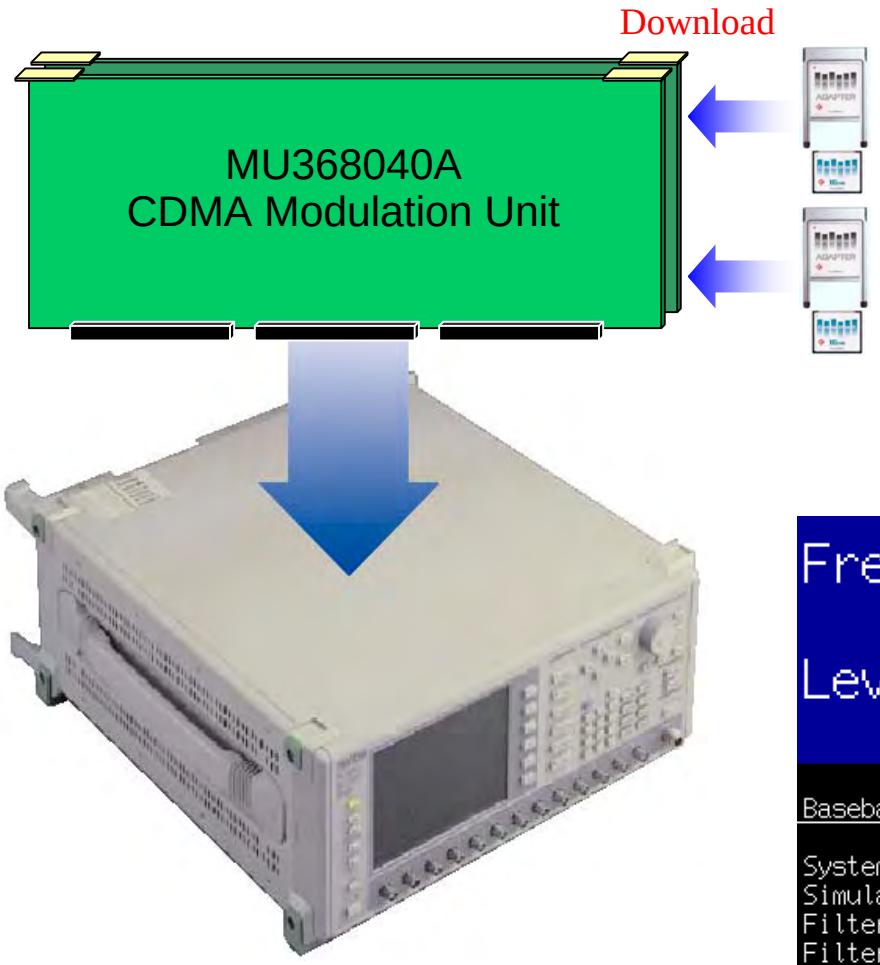
Communication system	Software (CompactFlash™)	Expansion unit
W-CDMA / 3GPP(FDD)	MX368041B W-CDMA Software	MU368040A CDMA Modulation Unit + MU368060A AWGN Unit
cdmaOne	MX368042A IS-95 Device Test Software	MU368040A CDMA Modulation Unit + MU368060A AWGN Unit
PDC	MX368011A PDC Software	MU368010A TDMA Modulation Unit
GSM	MX368012A GSM Device Test Software	MU368010A TDMA Modulation Unit
CDMA2000 1xEV-DO[*1], CDMA2000 1X[*2] GSM/EDGE[*3], PDC[*3], PHS[*3], NADC[*3]	MX368031A Device Test Signal Generation Software	MU368030A Universal Modulation Unit
CDMA2000 1xEV-DO	MX368033A CDMA2000 1xEV-DO Signal Generation Software	MU368030A Universal Modulation Unit
PDC Packet	MX368034A PDC Packet Software	MU368030A Universal Modulation Unit
PHS	MX368035A PHS Signal Generation Software	MU368030A Universal Modulation Unit

*1: Only 16QAM modulation is available in Forward, 8PSK and QPSK modulations are not available.
Neither Forward or Reverse is utilizable for receiver sensitivity test as coding format is not performed.
*2: Reverse is utilizable for receiver sensitivity test (RC1 & 3) in BS manufacturing as coding format is performed.
Forward is not utilizable for receiver sensitivity test as coding format is not performed.
*3: Continuous modulation signal based on the communication system.

The software is provided pre-installed in the expansion unit. Also, a PC memory card is provided for backup.
The software changes instantly by selecting the installed software.
At the software for the MU368030A, the signal format to output is selectable by downloading signal pattern files included in the software from a PC memory card to the waveform memory of the MU368030A Universal Modulation Unit.

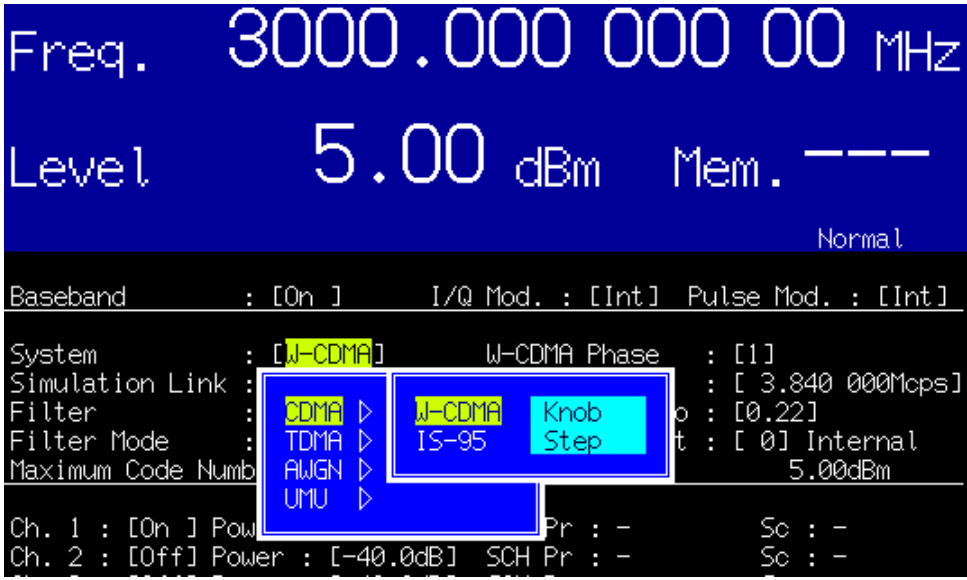
MU368040A CDMA Modulation Unit

Dual output Baseband generator for Real time output and Waveform memory output



MX368041B
W-CDMA Software

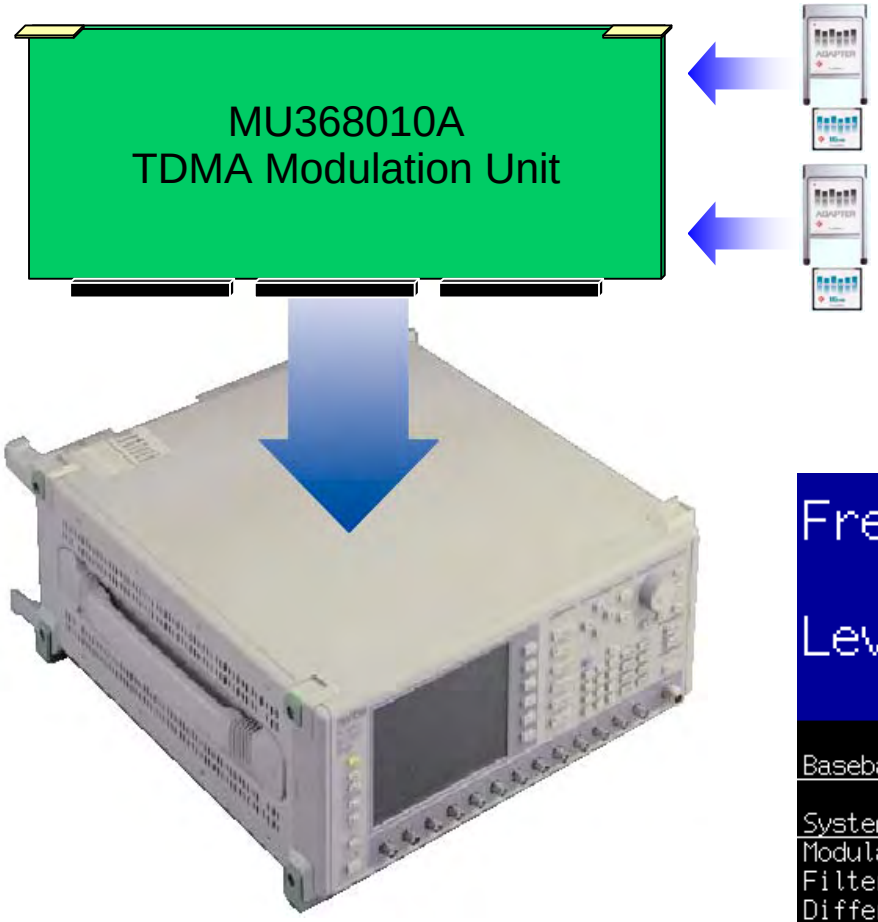
MX368042A
IS-95 Device Test Software



MU368010A TDMA Modulation Unit

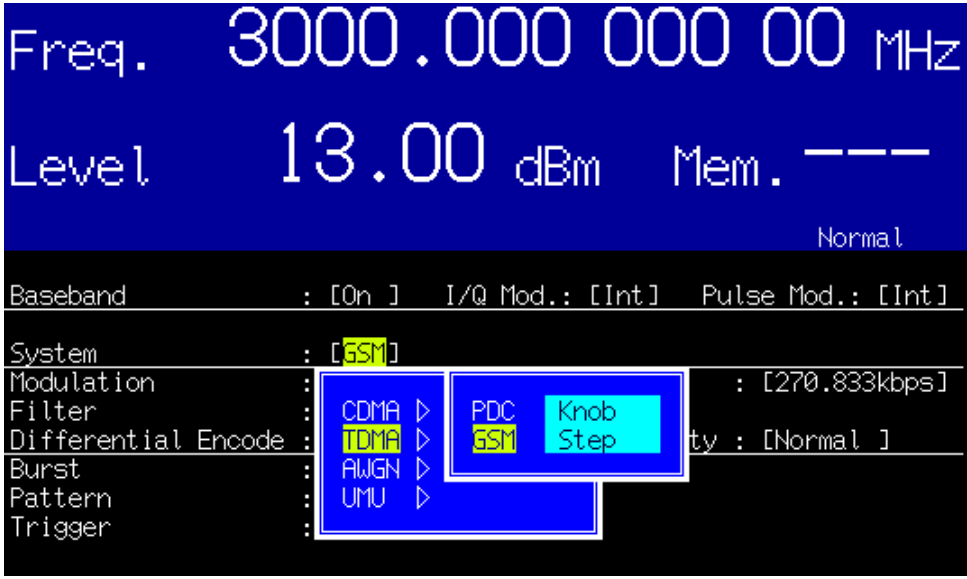
Baseband generator for Real time output

Download



MX368011A
PDC Software

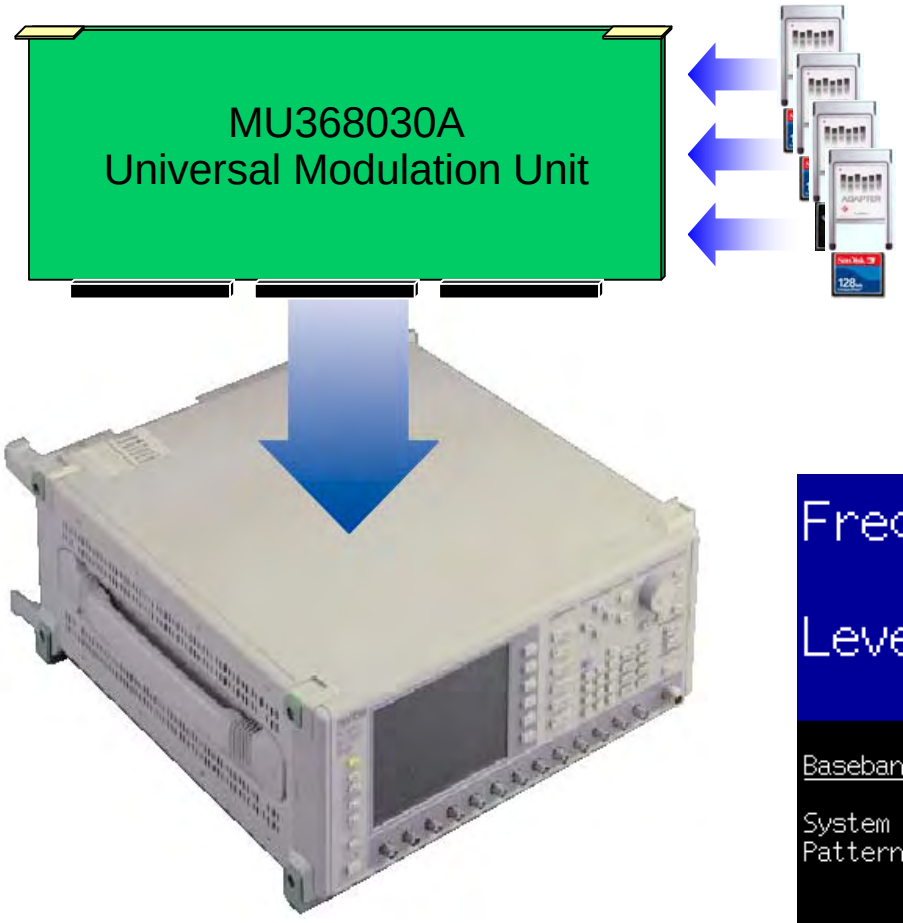
MX368012A
GSM Device Test Software



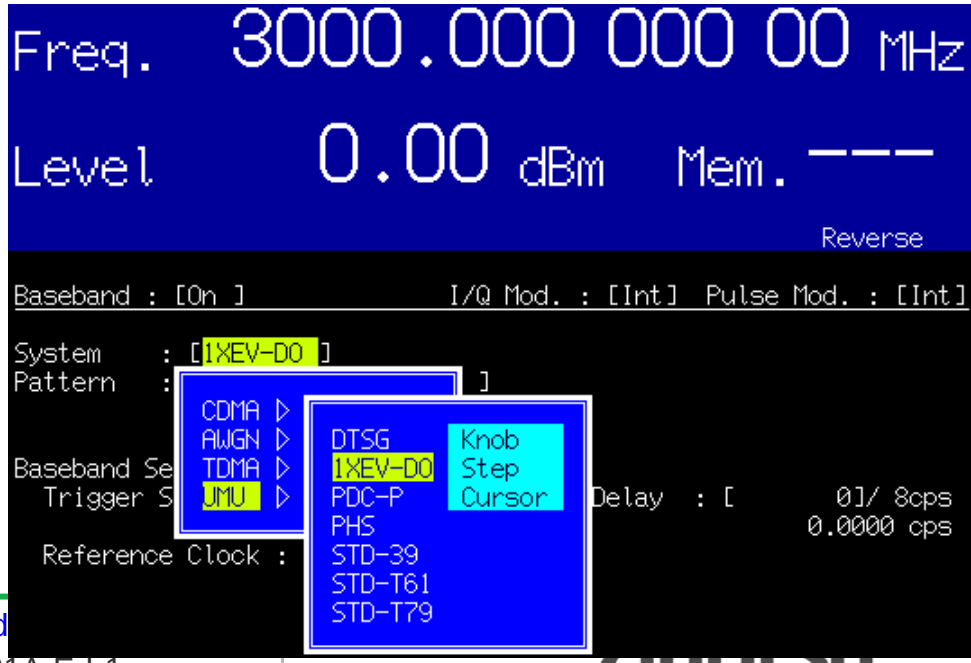
MU368030A Universal Modulation Unit

Baseband generator for Waveform memory output

Download

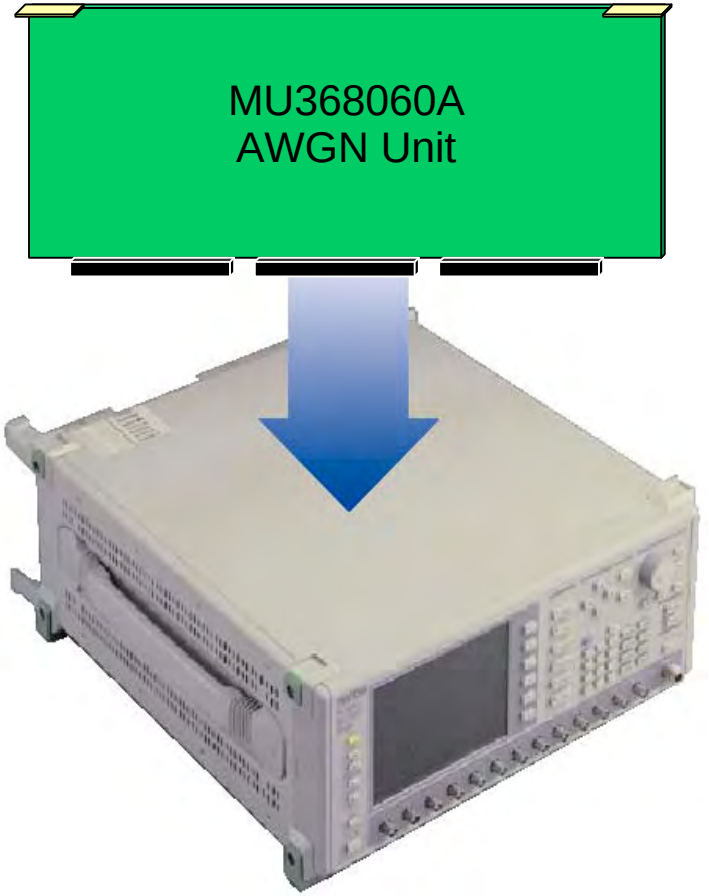


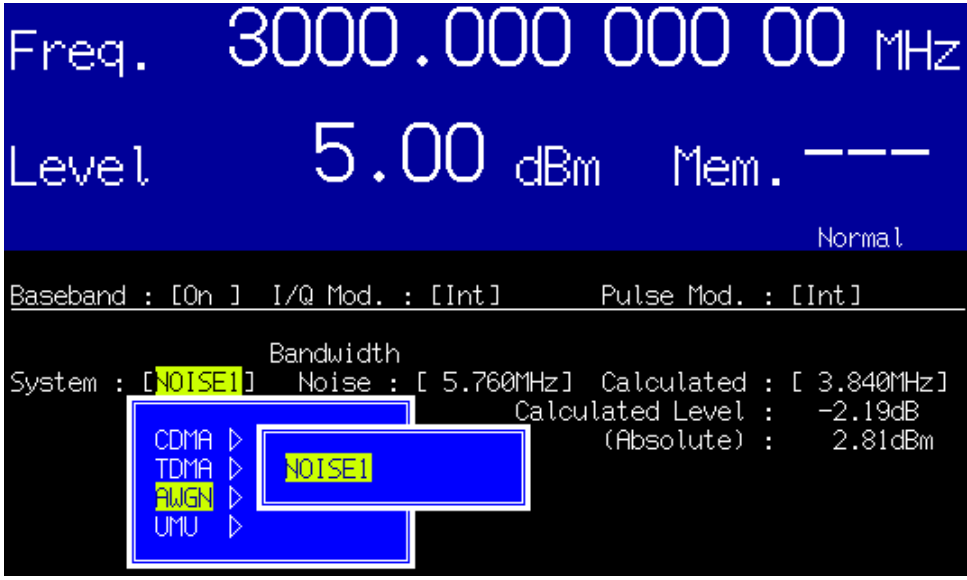
MX368031A
Device Test Signal Generation Software
MX368033A
CDMA2000 1xEV-DO Signal Generation Software
MX368034A
PDC Packet Software
MX368035A
PHS Signal Generation Software



MU368060A AWGN Unit

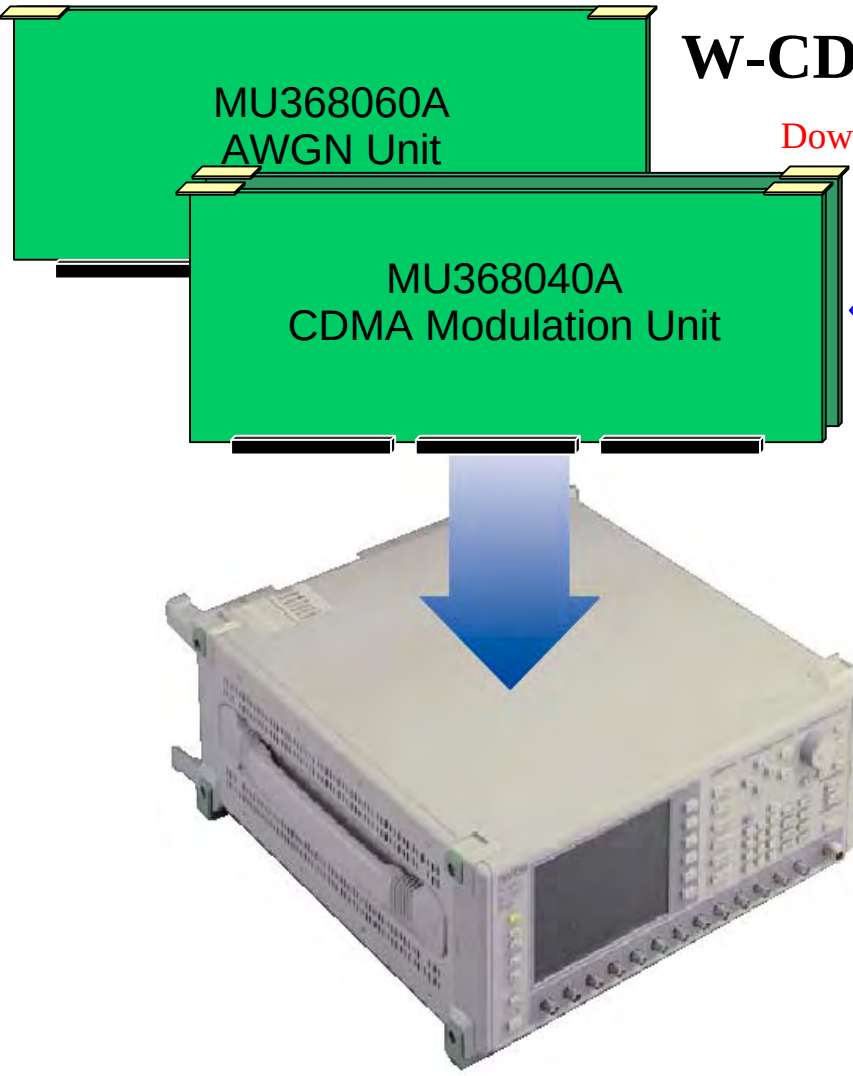
AWGN source for Real time output





MU368040A + MX368041A + MU368060A

W-CDMA and AWGN mixing output



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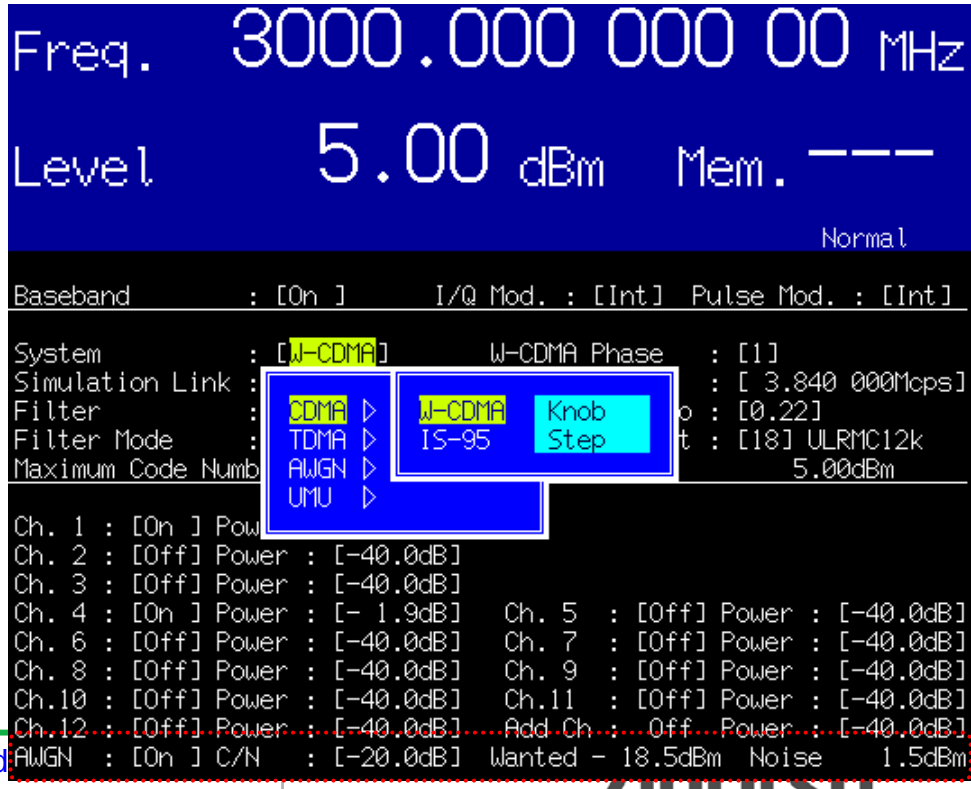
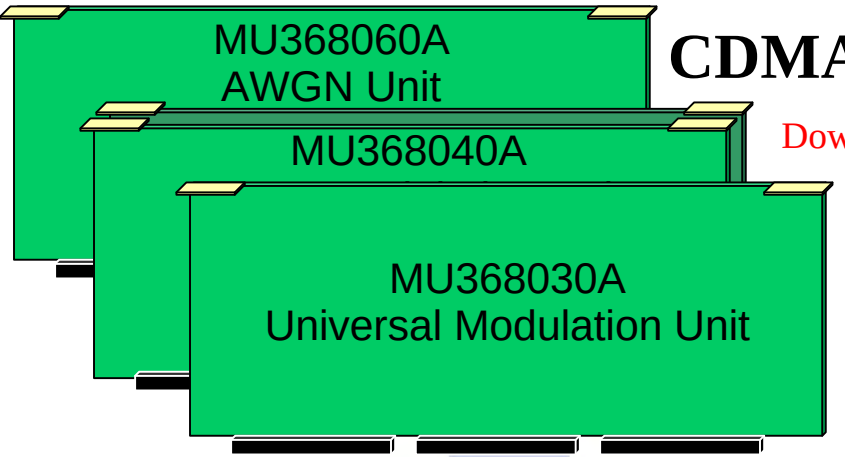
MX368041B
W-CDMA Software



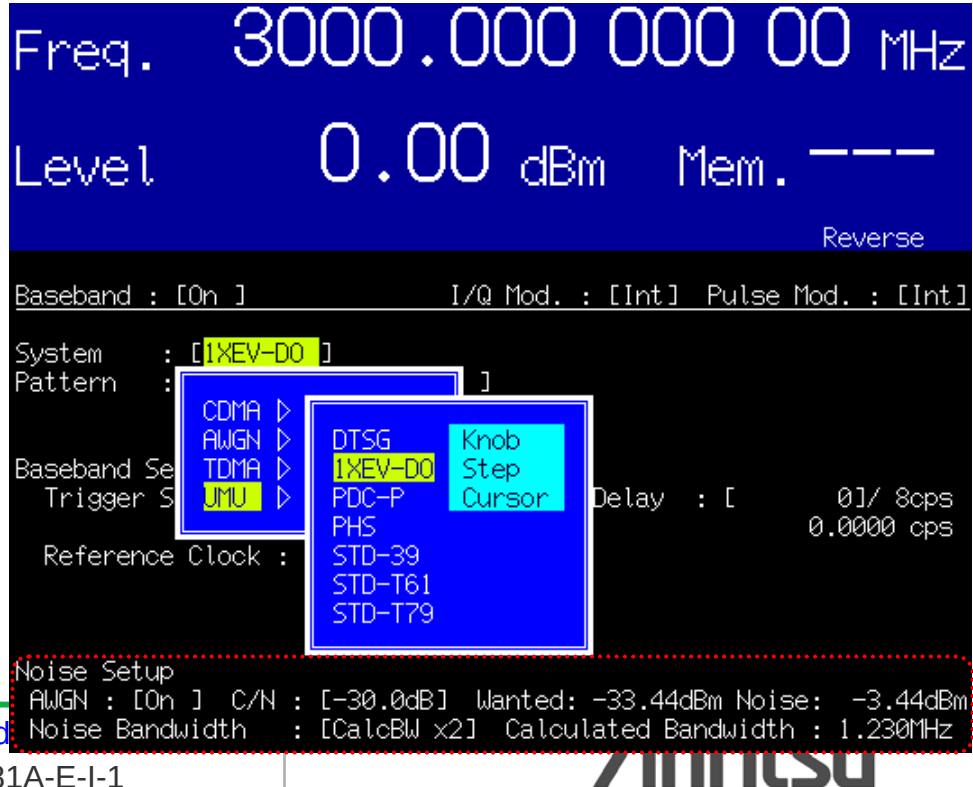
MU368030A + MU368040A + MU368060A

CDMA2000 and AWGN mixing output



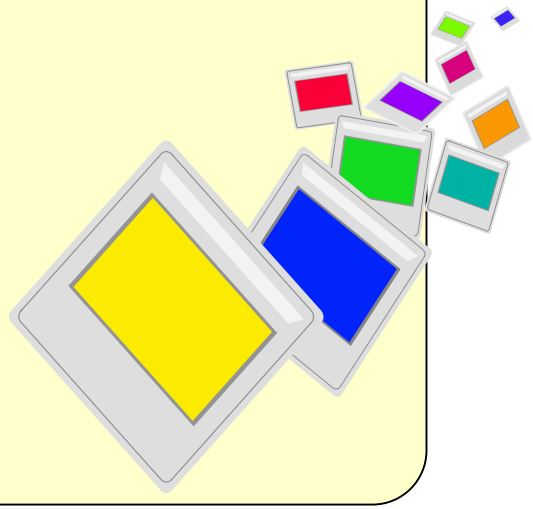
Download

MX368031A
Device Test Signal Generation Software
MX368033A
CDMA2000 1xEV-DO Signal Generation Software



Feature

- Product outline
- Feature
- Application
- Option



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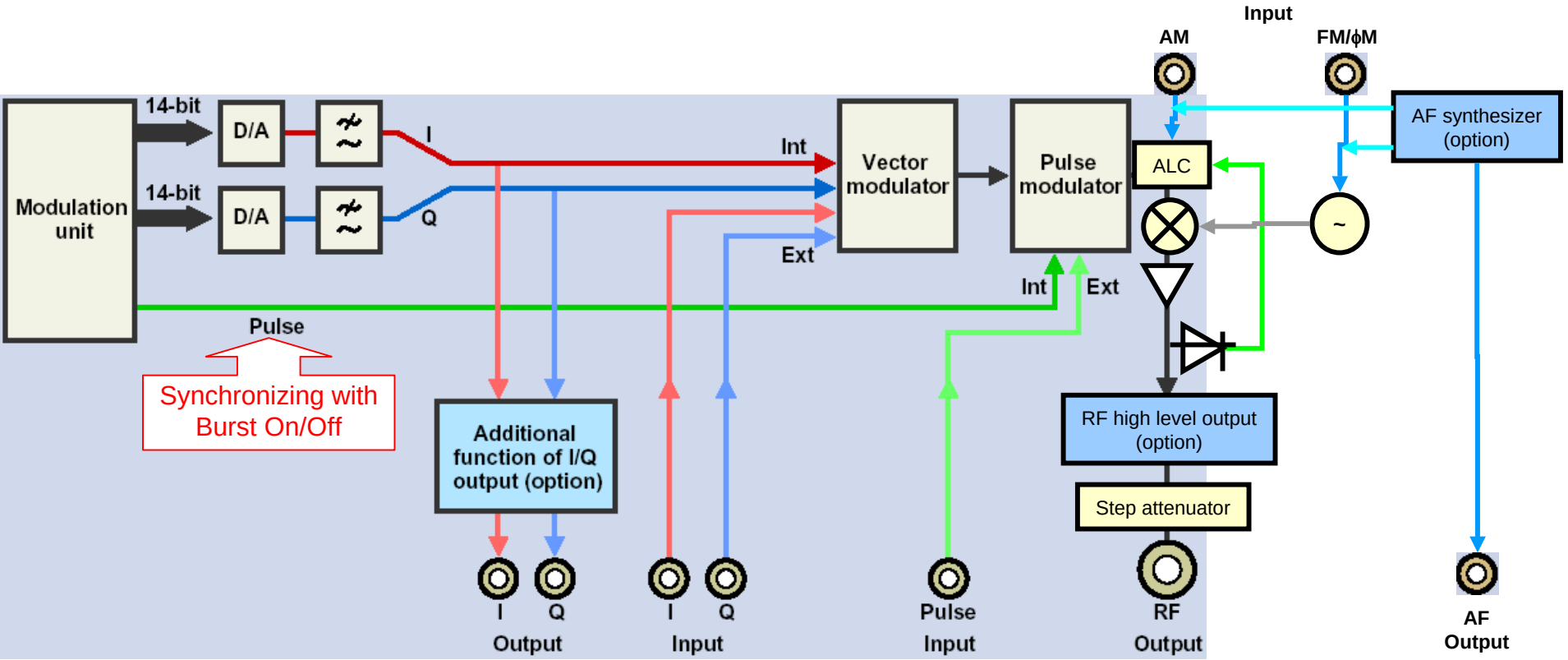
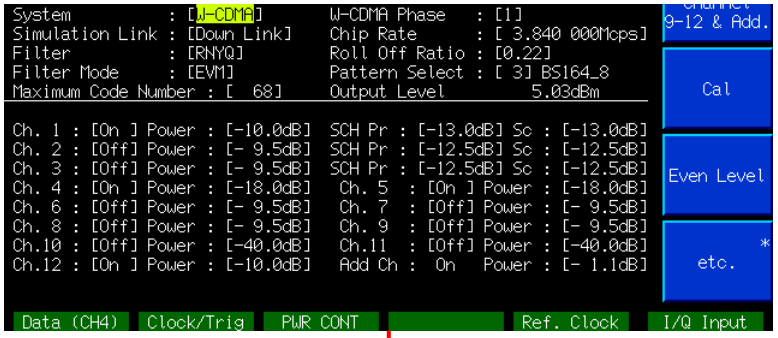
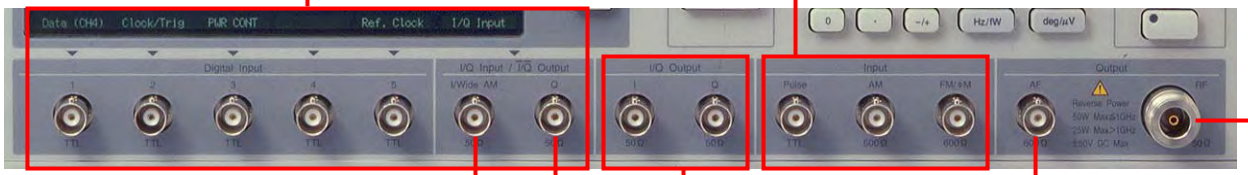
MG3681A Block diagram



Connectivity Front panel

- **Display functions according to the used software and settings**
- **External modulation Input**
  - » Pulse, AM, FM, ϕM

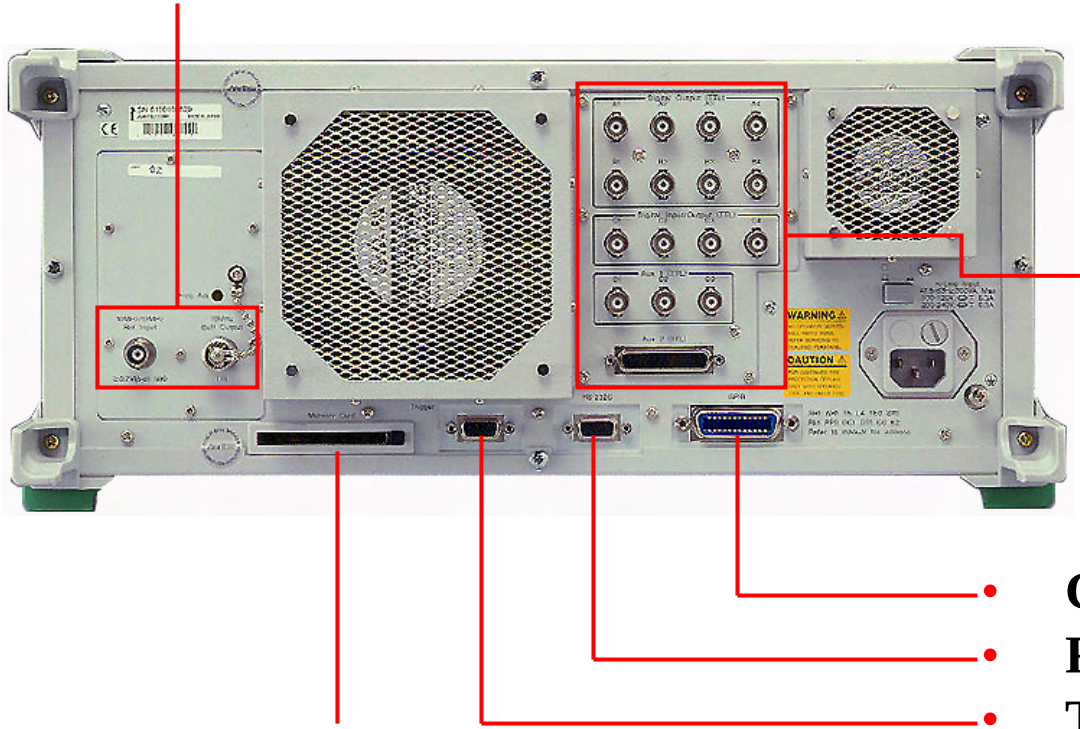




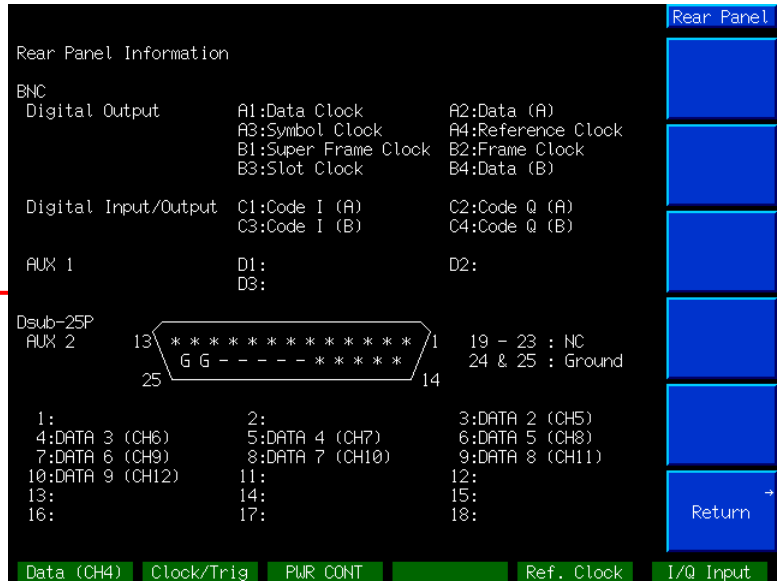
- **External I/Q Input**
  Differential I/Q Output (Option)
- **I/Q Output**
- **AF Output**
- **RF Output**

Connectivity Rear panel

- **External timebase reference clock**
  - » 10MHz/13MHz



- **Display functions according to the used software and settings**



- **GPIB remote control**
- **RS-232C remote control**
- **Trigger remote control**
  - » Frequency, Output level, Parameter memory (BPM number) Up/Down, RF output On/Off

- **PC memory card**
  - » PCMCIA interface

Excellent level accuracy signal

For outputting with precise level

- **High-stability ALC(Automatic Level Control) circuit**

  Detectable at vector modulation (internal/external modulation) also

  - The temperature stability of ALC circuit is almost decided by temperature response of detector. The temperature response of detector has been improved by heating the detection diode with heater circuit in low temperature, which is due to the big influence of detection voltage drift especially in low temperature.

- **High-accuracy and high-reliability step attenuator**

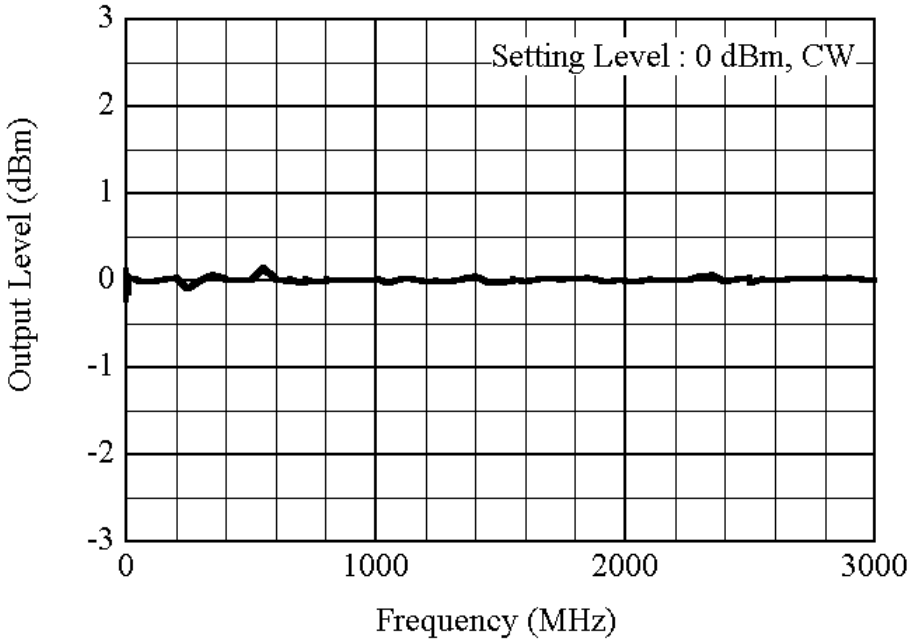
  - Mechanical attenuator with excellent attenuation accuracy, small path loss and no signal distortion.
    - 1dB step, up to 140dB attenuation

- **Per-unit correction**

  - Frequency response, linearity error of ALC circuit and attenuation error of step attenuator are measured by the power meter and calibration receiver, then the data is inputted to correction table.

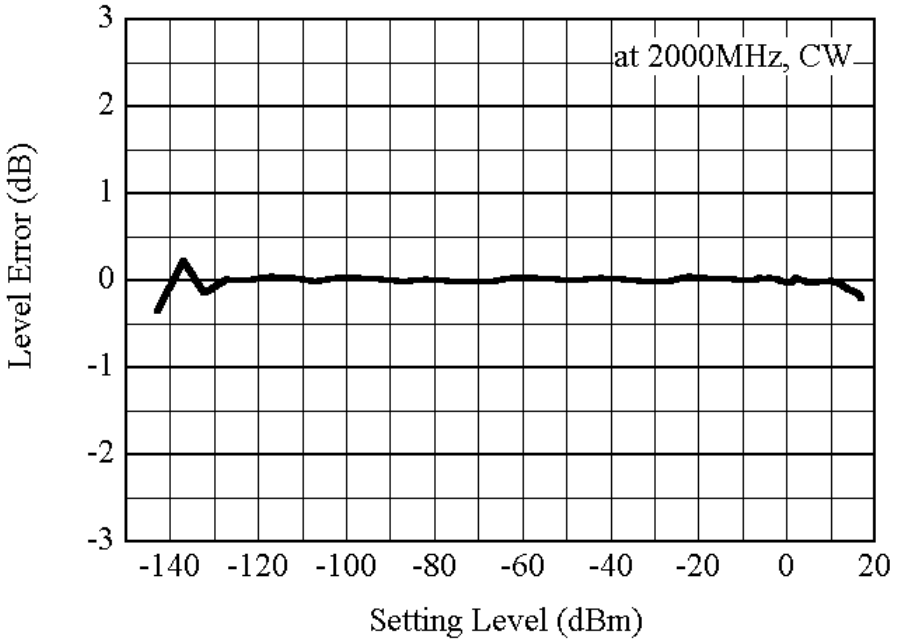
Typical level accuracy

- **Frequency response**



» ≤ ±0.2 dB

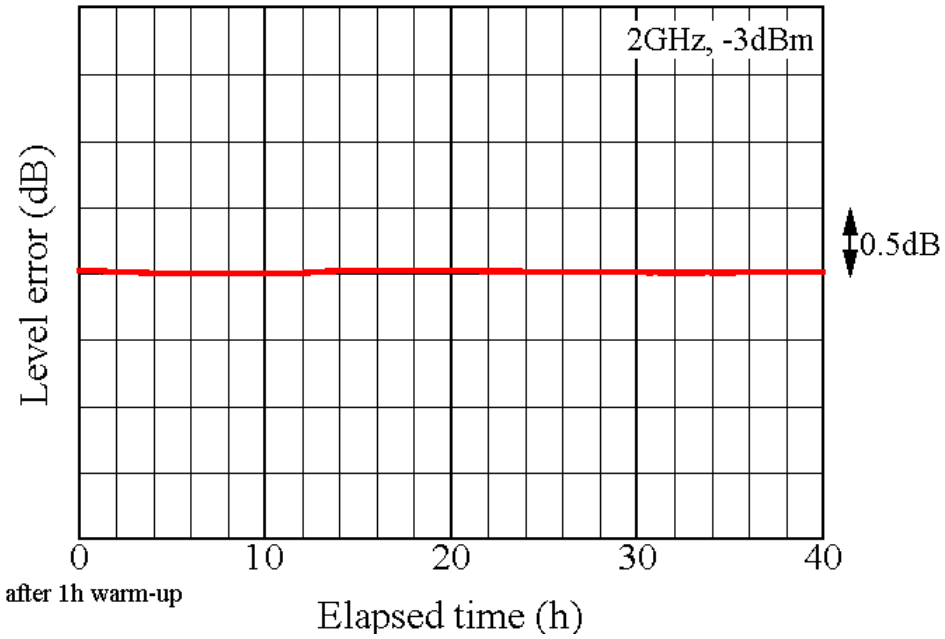
- **Linearity**



» ≤ ±0.1 dB (-127 ~ +13 dBm)

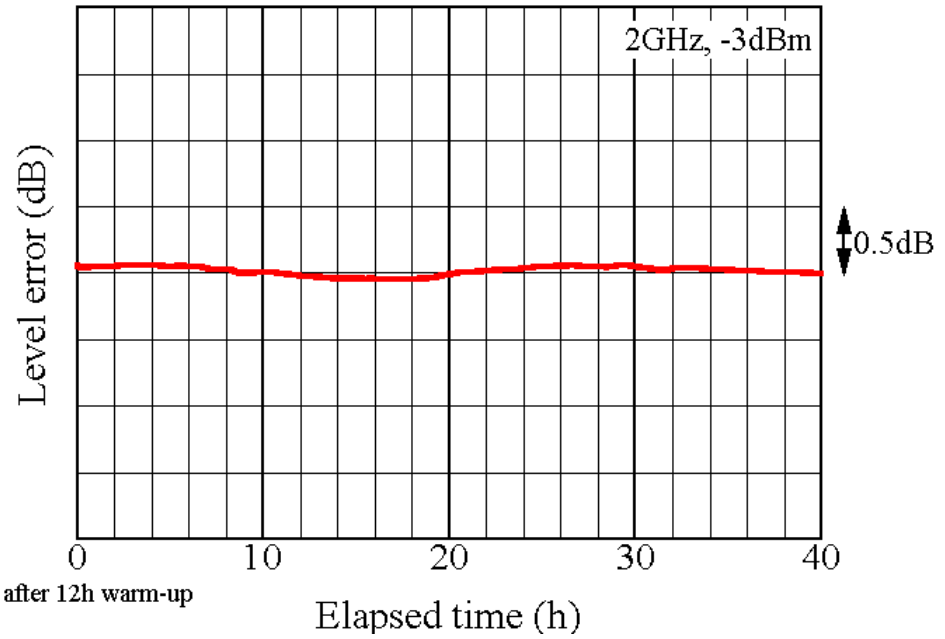
Typical level stability

- **Aging**
  - » CW, ALC on (default setting)



  - » Almost no variation

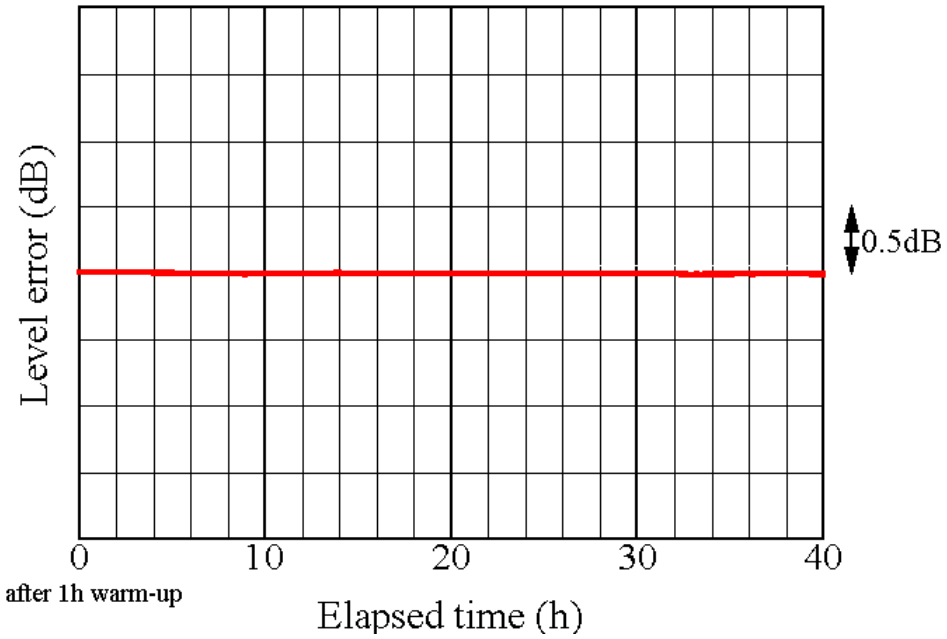
- **Aging**
  - » CW, ALC off



  - » ≤ ±0.1 dB
    - – at ALC off
      - High-speed level switching

Typical level stability

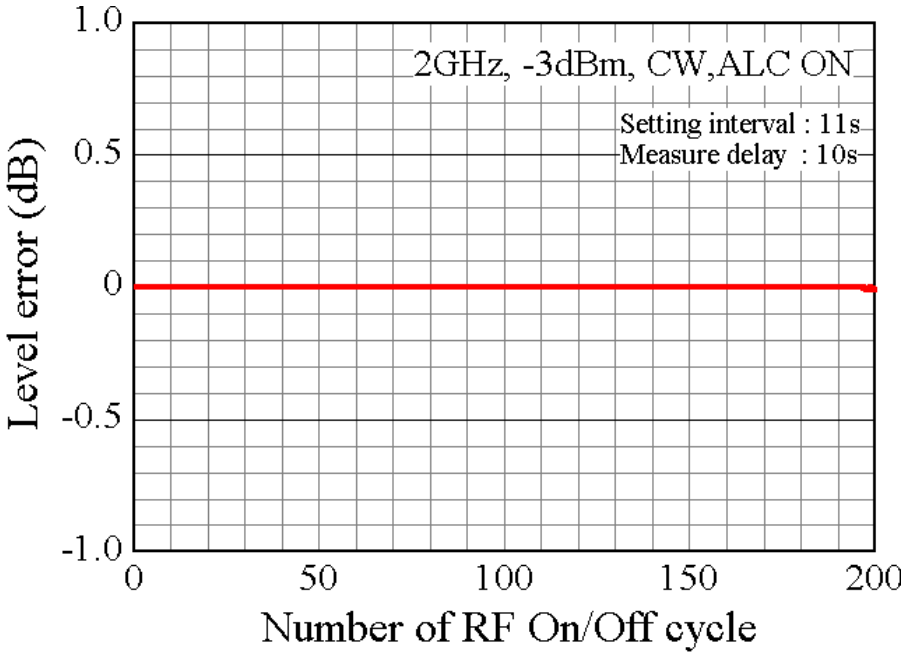
- **Aging**
  - » W-CDMA modulation, ALC on



  - » Almost no variation (same as CW)

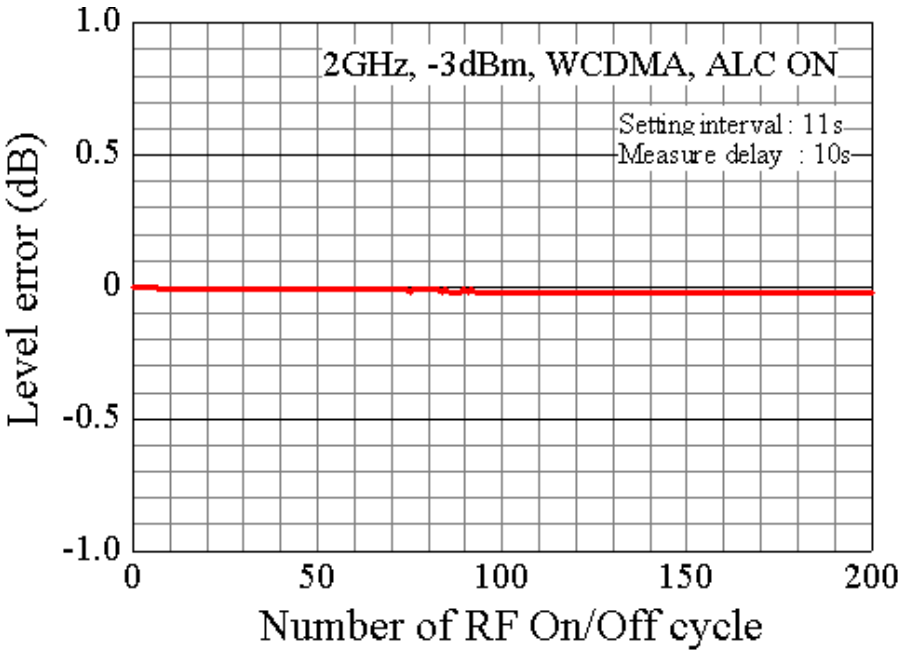
Typical level repeatability

- **RF off → on ([on] off [on] off ...)**
  - » CW



  - » Almost no variation

- **RF off → on ([on] off [on] off ...)**
  - » W-CDMA modulation

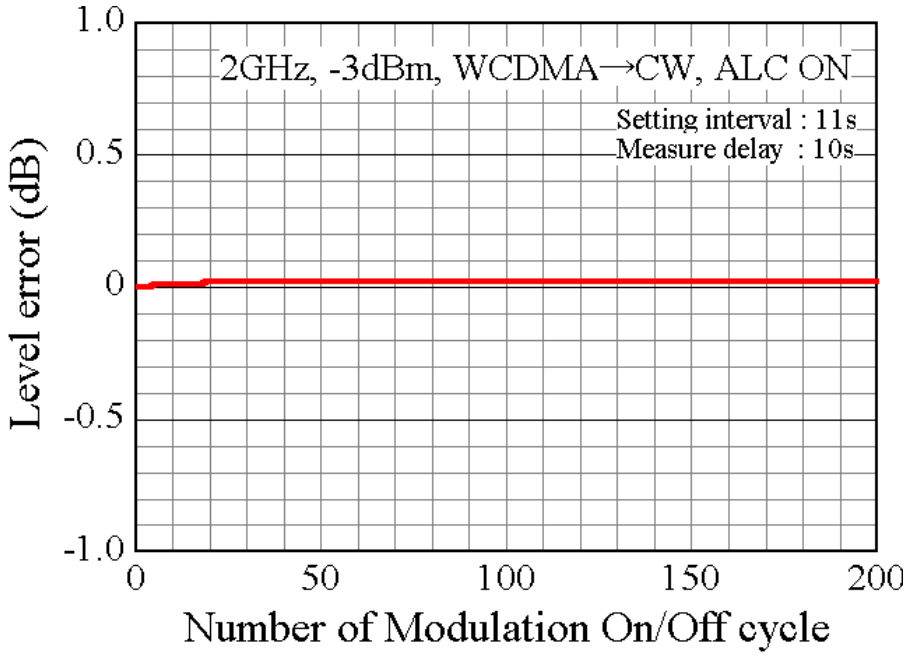


  - » ≤ 0.02 dB

1st measurement level = reference(0 dB)

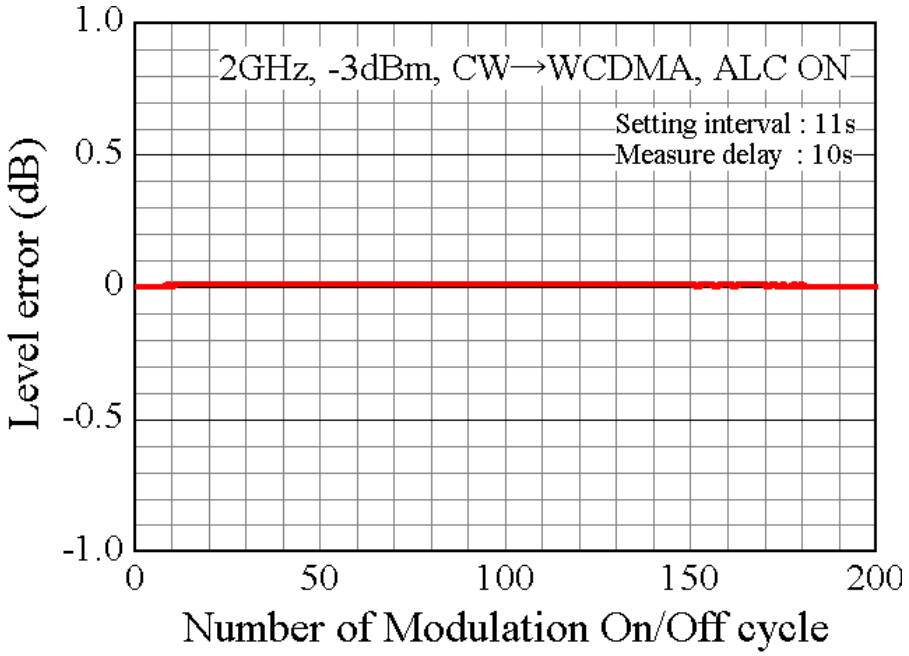
Typical level repeatability

- **Modulation on → off**
  ([off(CW)] on(W-CDMA) [off] on ...)



» ≤ 0.02 dB

- **Modulation off → on**
  ([on(W-CDMA)] off(CW) [on] off ...)



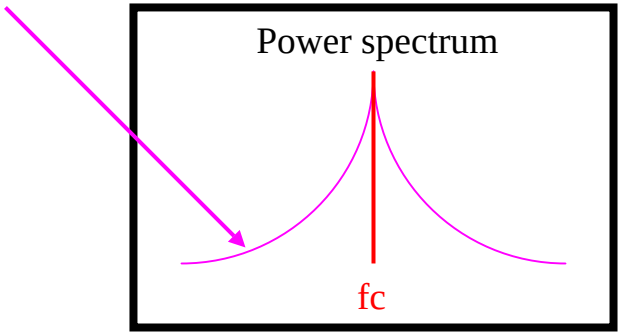
» ≤ 0.02 dB

1st measurement level = reference(0 dB)

Excellent signal Purity

Alternate adjacent channel leakage power ratio is mainly due to phase noise.

- » Phase noise [dBc/Hz]



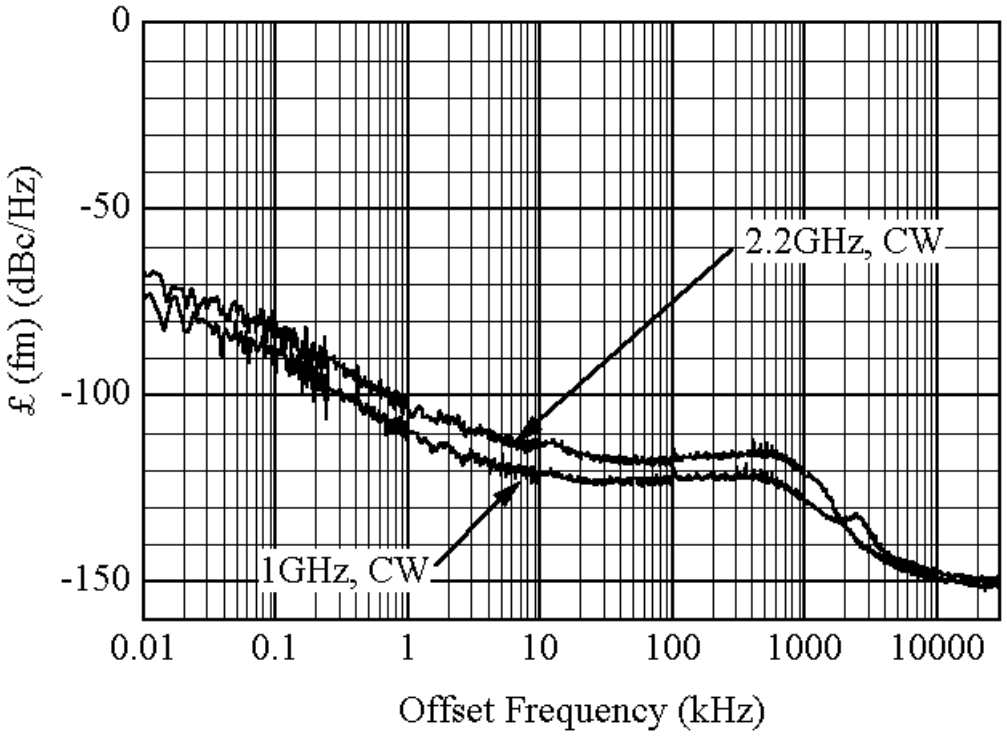
For attenuating the residual noise

- **Optimization of level diagram and components**
  - » Circuit has been simplified to minimize the influence of non-linear components.
  - » High-speed 14 bit D/A converter has been adopted, and the quantization noise leading to the residual noise has been reduced.
  - » The smoothing filter which set the cutoff frequency according to the modulation band has been passed, and out-band spurious and noise have been eliminated.

SSB(Single Side Band) phase noise

Noise of wide-band modulation signal for 3G has been lowered.

- **C/N characteristic of excellent purity VCO has been applied.**
  - » Alternate adjacent channel leakage power ratio is excellent.
    - – -145 dBc/Hz typ. : 5MHz offset
    - – -150 dBc/Hz typ. : 20MHz offset



Changing Phase noise

The compression of phase noise is changed by switching the loop characteristic of PLL synthesizer circuit. Thus noise of narrow band modulation signal for 2G can be lowered also.

- PLL Mode: Normal

  The phase noise up to 100 kHz offset is improved.

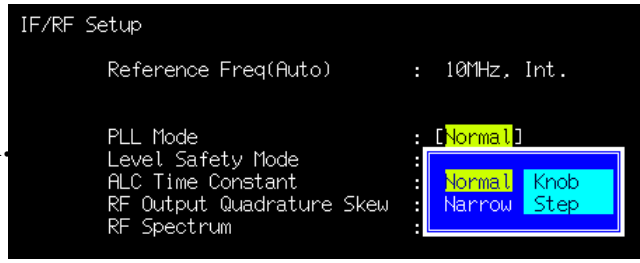
- PLL Mode: Narrow

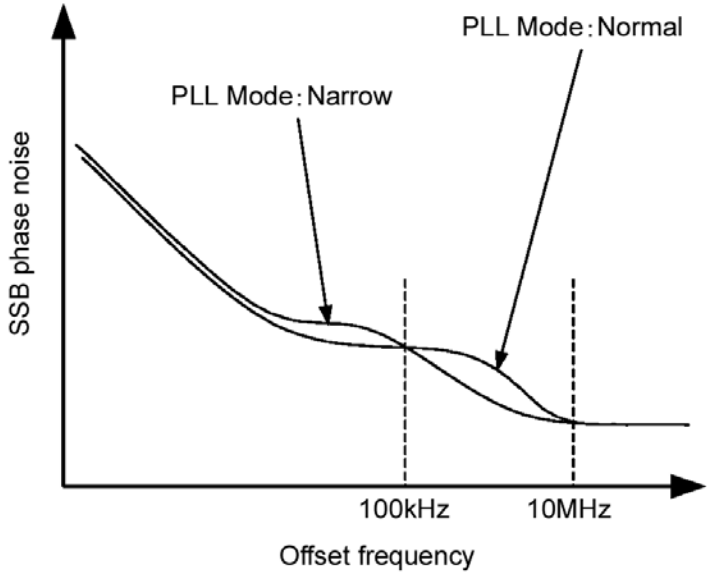
  The phase noise of 100 k to 10 MHz offset is improved.

Changing by the communication system is useful.

e.g.

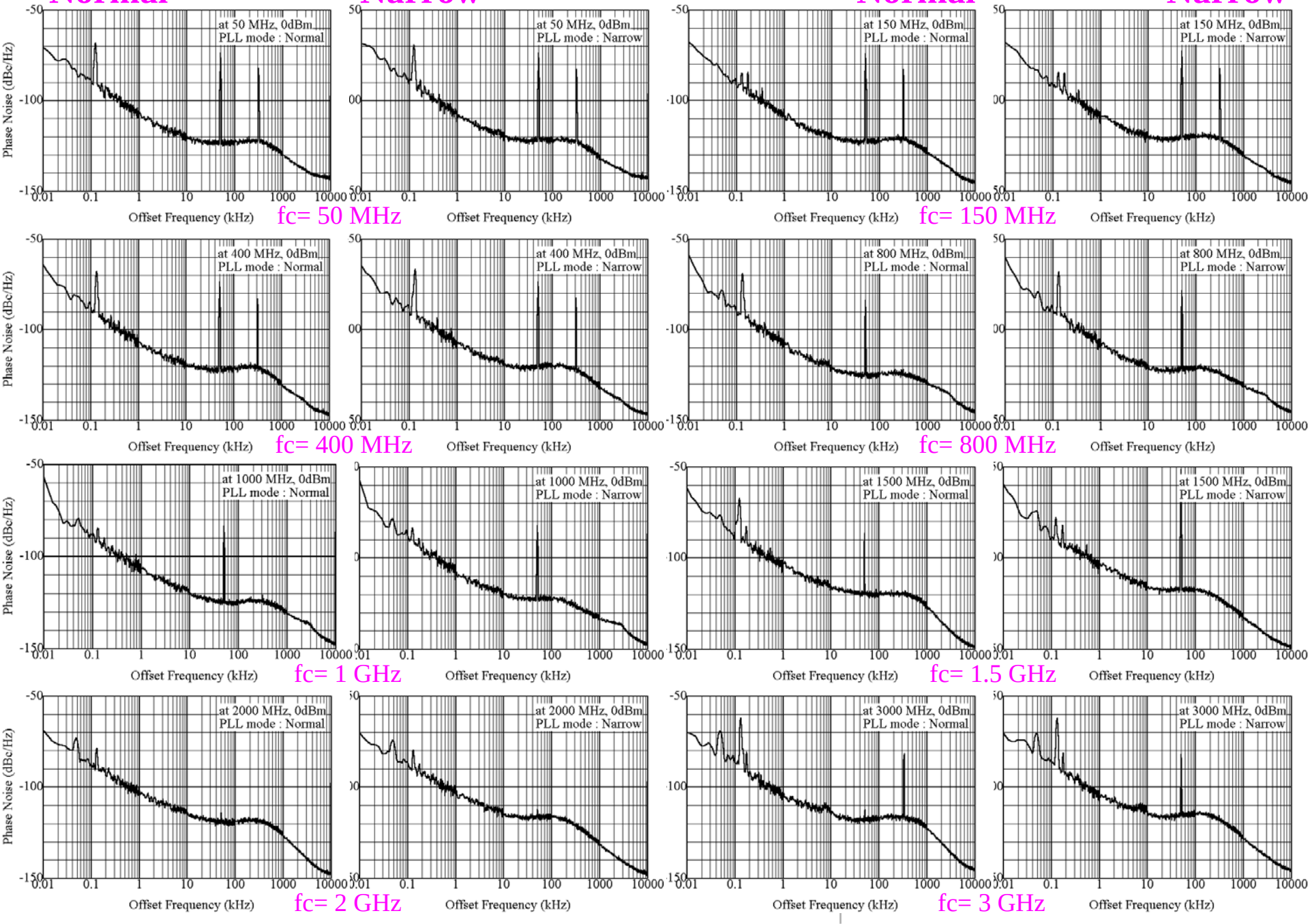
- W-CDMA: Normal
- CDMA2000: Narrow
- GSM/EDGE: Narrow
- PHS : Narrow
- PDC : Normal
- NADC(IS-136): Normal





Typical phase noise

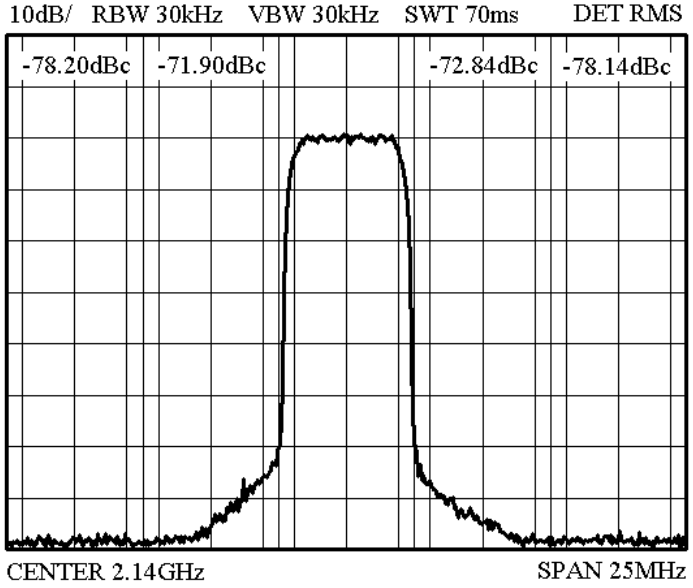
Normal Narrow Normal Narrow



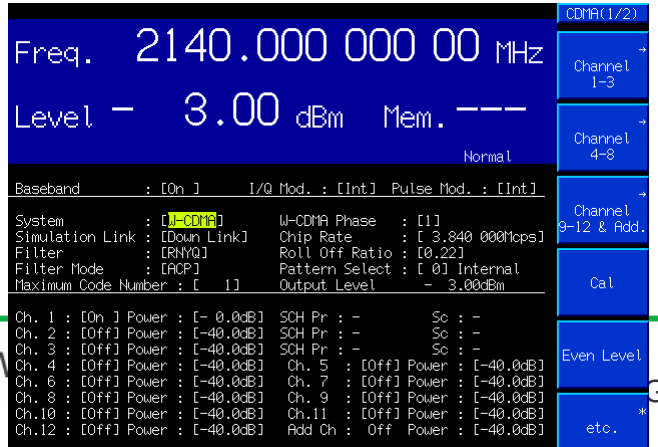
Adjacent channel leakage power ratio

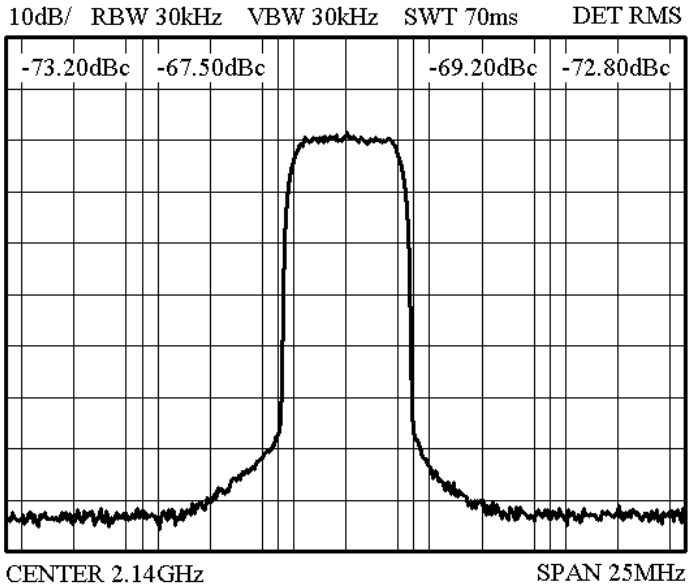
W-CDMA, ≤ -3 dBm (≤ +5 dBm at installing Option42)

Adjacent channel leakage power ratio was achieved at top level.

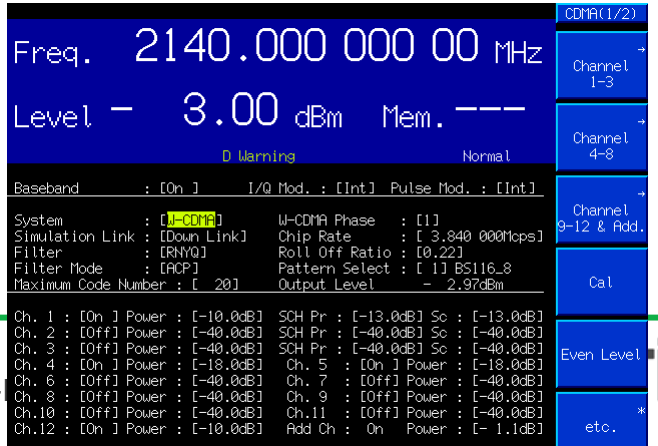


Frequency 2.140GHz
Output Level -3dBm
Pattern 1 code PN9





Frequency 2.14GHz
Output Level -3dBm
Pattern 3G TS25.141 V3.5.0 (2001-03) 6.2.1.1.1
Test Model 1 = P-CCPCH+SCH+P-CPICH+PICH+S-CCPCH+DPCH × 16codes



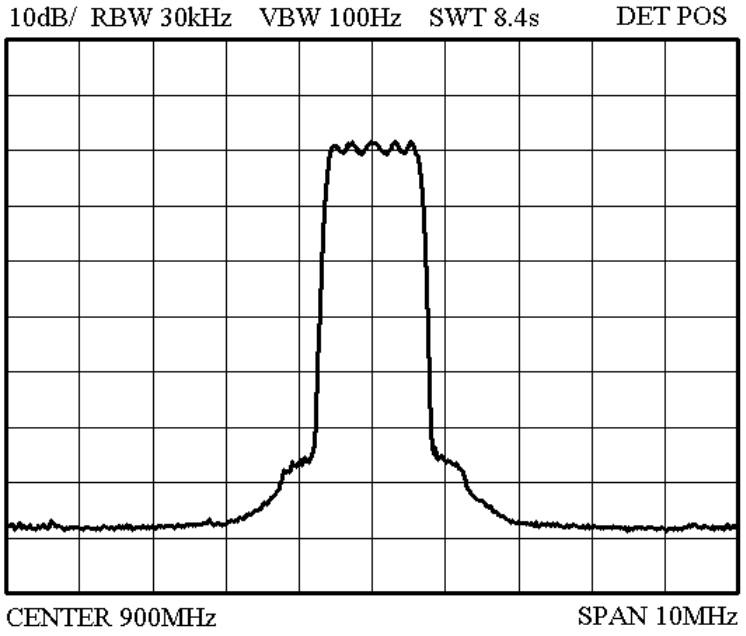
Adjacent channel leakage power ratio
IS-95, ≤ -1 dBm (≤ +7 dBm at installing Option42)

Forward

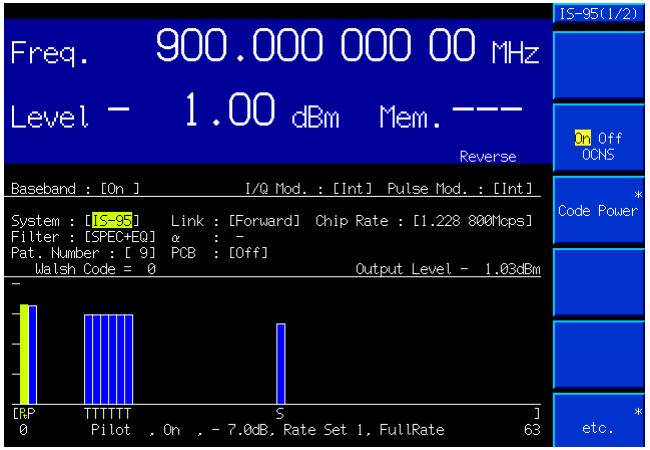
9 channels	64 channels
– ≤ -63 dBc	≤ -63 dBc
– ≤ -69 dBc	≤ -68 dBc
– ≤ -77 dBc	≤ -75 dBc

Reverse

full rate	
≤ -65 dBc/30kHz	: 0.885 ~ 1.25 MHz offset
≤ -70 dBc/30kHz	: 1.25 ~ 1.98 MHz offset
≤ -77 dBc/30kHz	: 1.98 ~ 5 MHz offset



Frequency	900MHz
Output Level	0dBm
Pattern	Base Station Test Model, Nominal

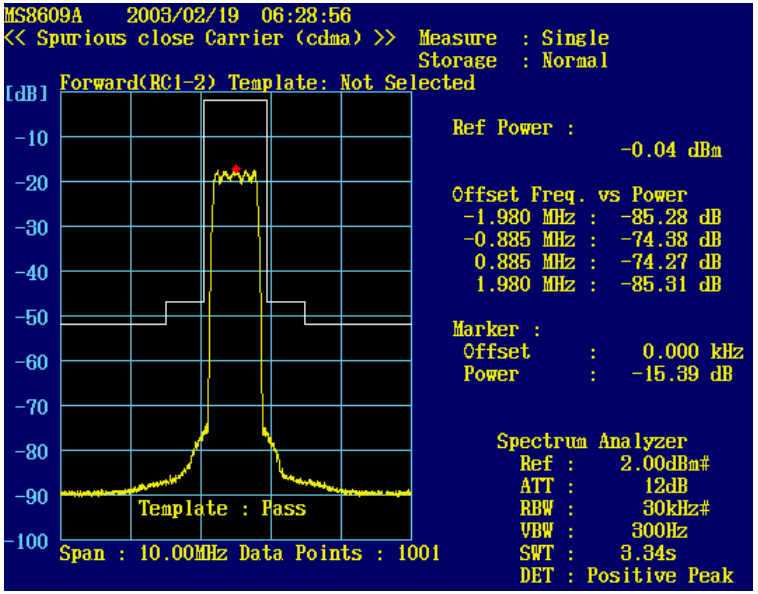


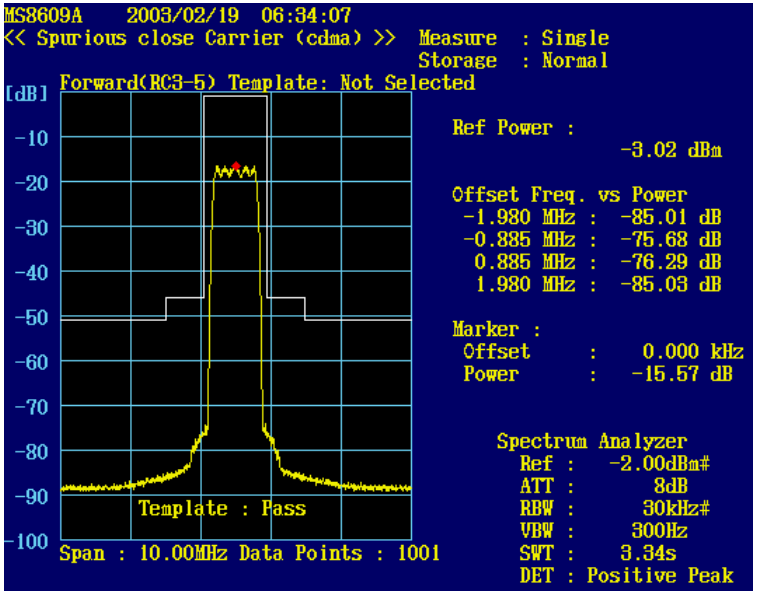
Adjacent channel leakage power ratio

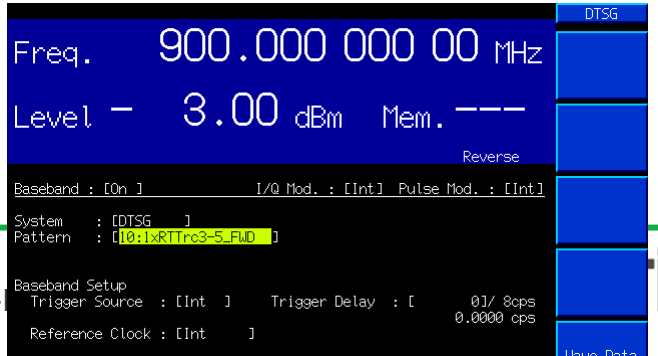
CDMA2000 1X (RC1-2), ≤ 0 dBm (≤ +8 dBm at installing Option42)

CDMA2000 1X (RC3-5), ≤ -3 dBm (≤ +5 dBm at installing Option42)

	Forward		Reverse	
	RC1 & 2	RC3 ~ 5	RC1 & 3	
–	≤ -62 dBc	≤ -62 dBc/30kHz	≤ -62 dBc/30kHz	: 0.885 ~ 1.98 MHz offset
–	≤ -67 dBc	≤ -70 dBc/30kHz	≤ -70 dBc/30kHz	: 1.98 ~ 2.5 MHz offset
–	≤ -77 dBc	≤ -77 dBc/30kHz	≤ -77 dBc/30kHz	: 2.5 ~ 5 MHz offset



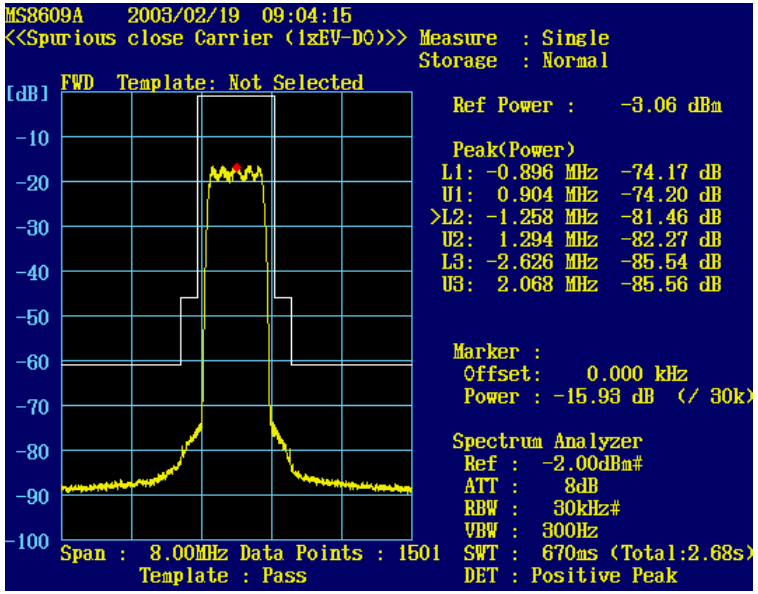


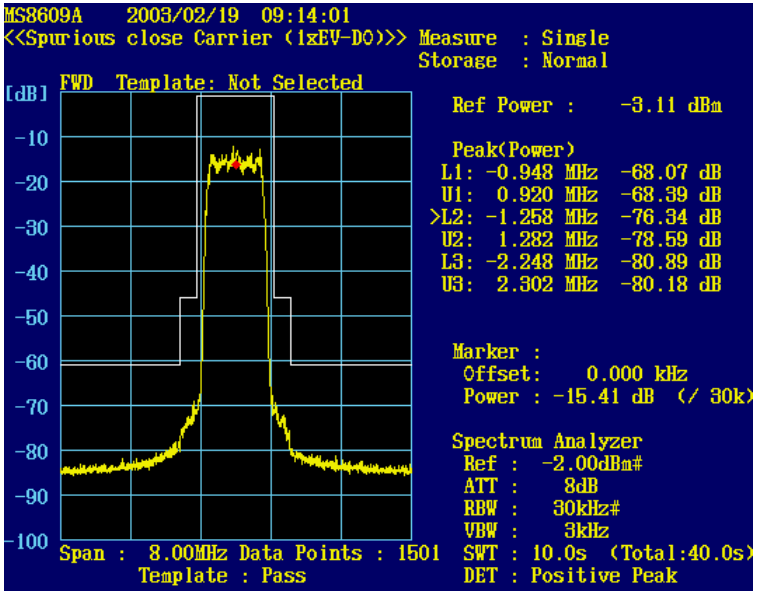


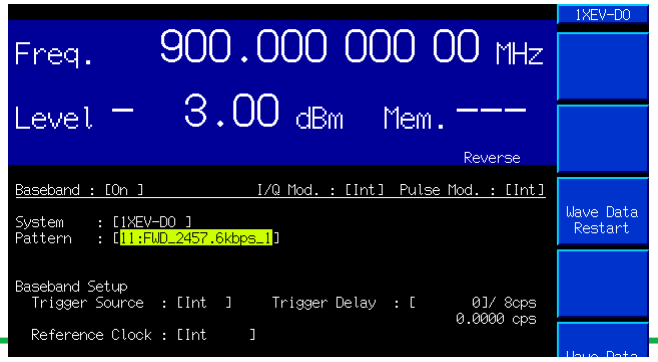
Adjacent channel leakage power ratio

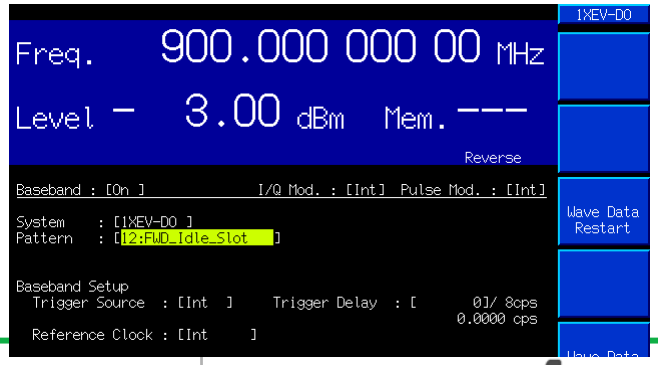
CDMA2000 1xEV-DO, ≤ -3 dBm (≤ +5 dBm at installing Option42)

- ≤ -65 dBc/30kHz : 0.885 ~ 1.98 MHz offset
- ≤ -70 dBc/30kHz : 1.98 ~ 2.5 MHz offset
- ≤ -77 dBc/30kHz : 2.5 ~ 5 MHz offset





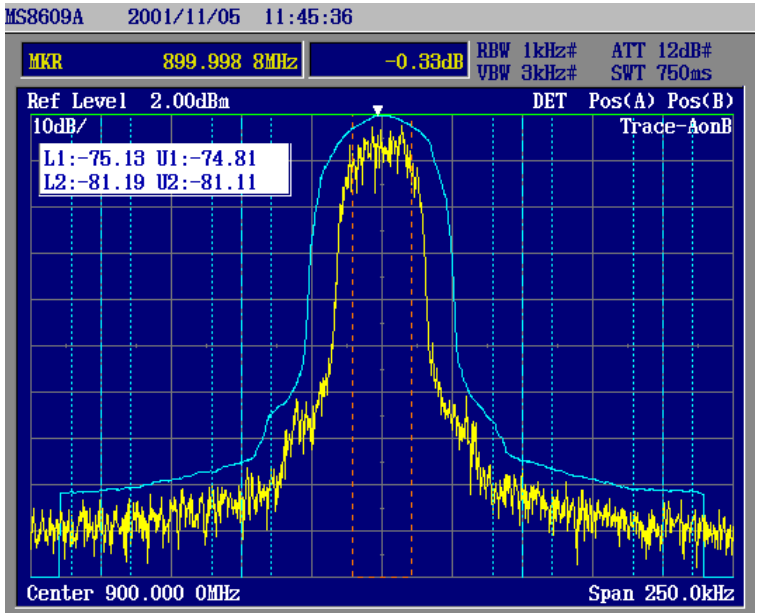


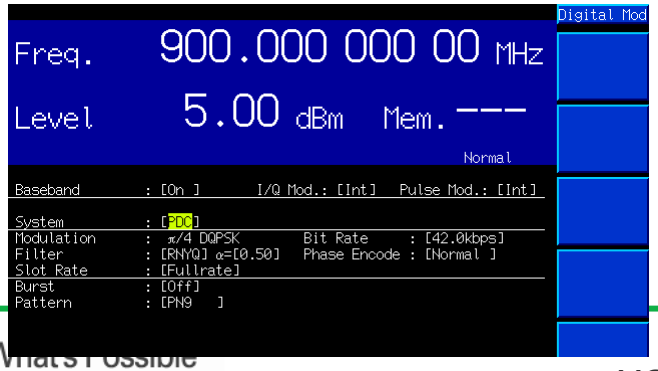


Adjacent channel leakage power ratio PDC, ≤ +5 dBm

MX368011A

- ≤ -64 dBc/21kHz
- ≤ -68 dBc/21kHz

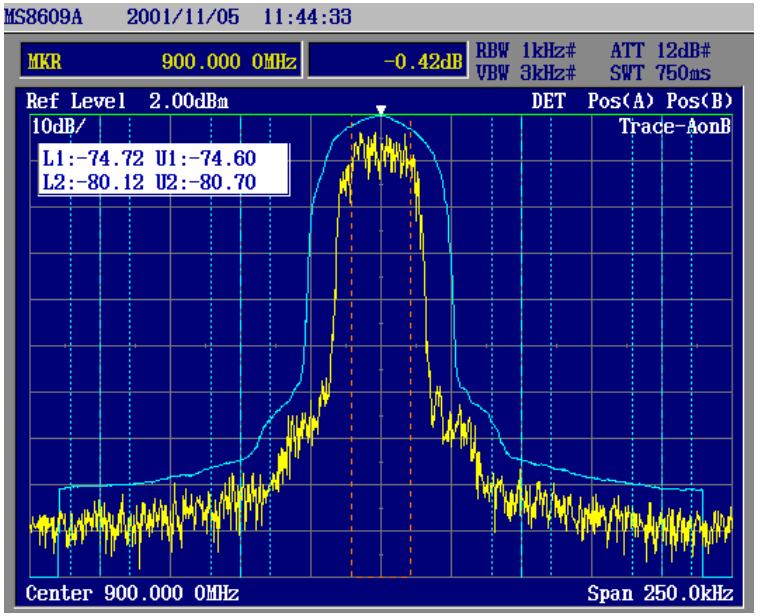


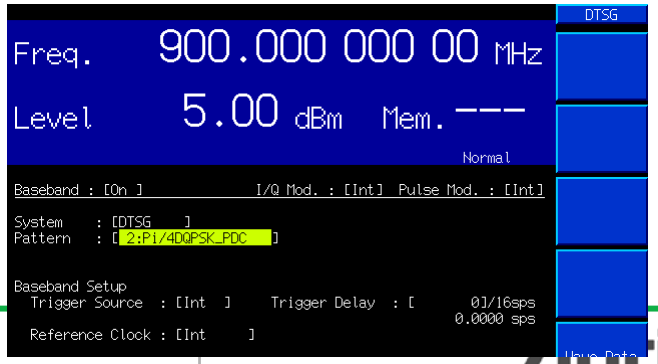


MX368031A

≤ -63 dBc/21kHz : 50 kHz offset

≤ -67 dBc/21kHz : 100 kHz offset

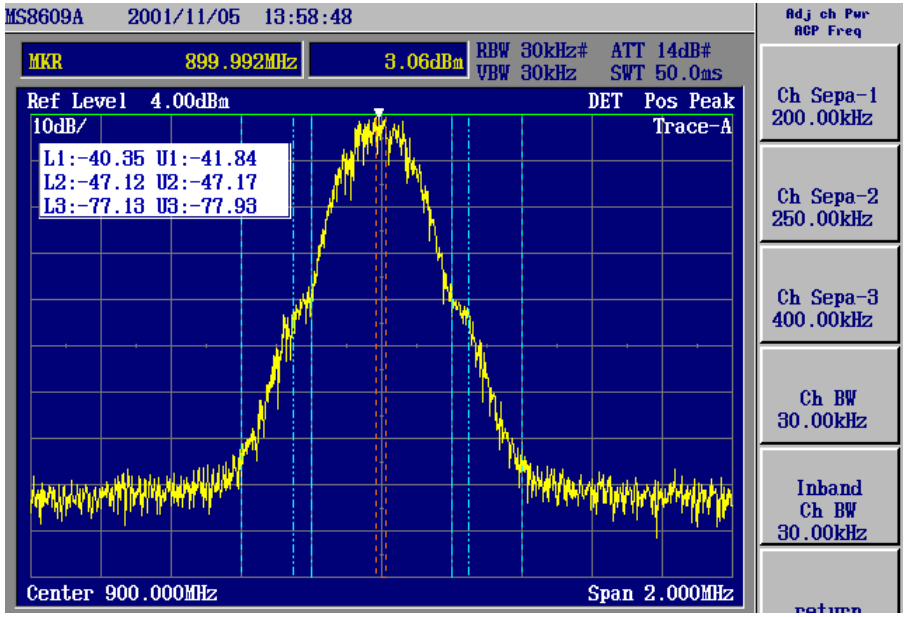




Adjacent channel leakage power ratio GSM/EDGE(GMSK), ≤ +5 dBm

MX368012A

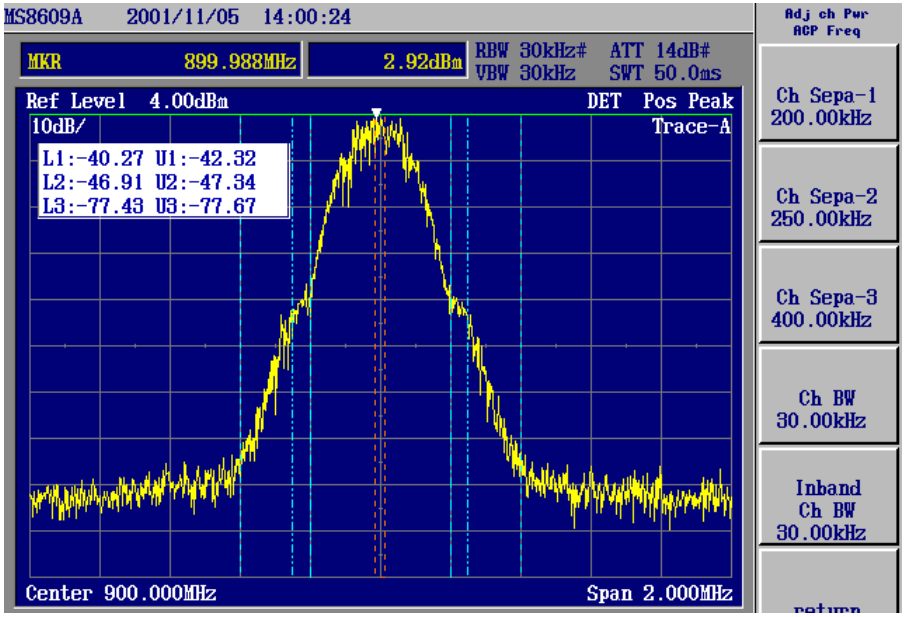
- ≤ -35 dBc/30kHz
- ≤ -66 dBc/30kHz

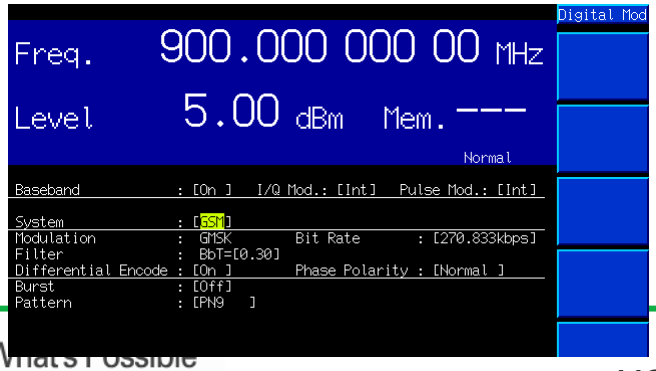


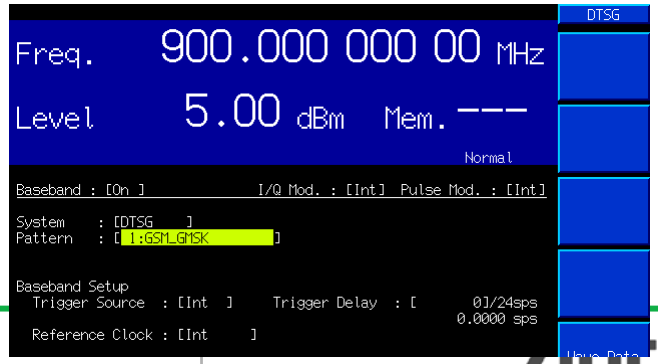
MX368031A

≤ -35 dBc/30kHz : 200 kHz offset

≤ -66 dBc/30kHz : 400 kHz offset

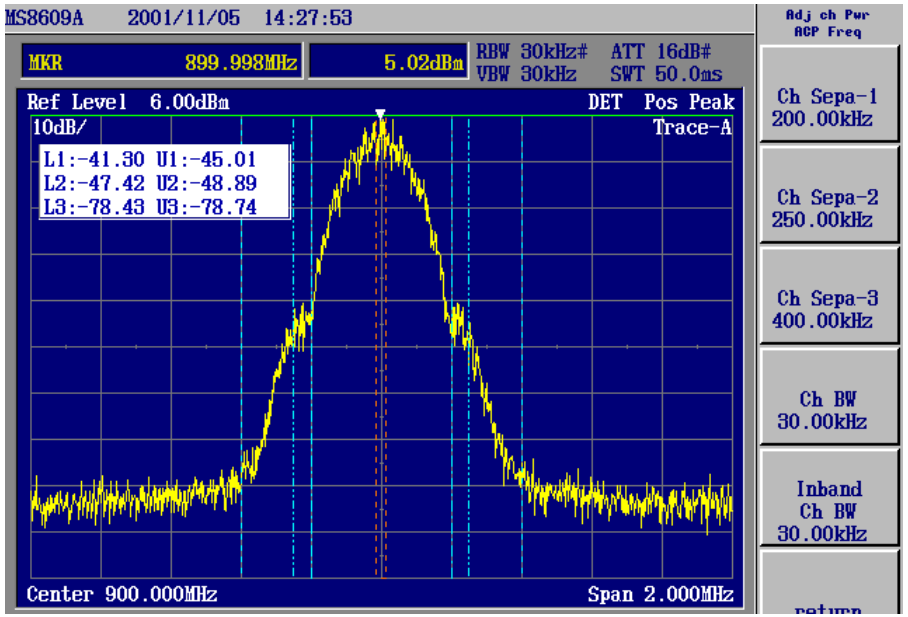


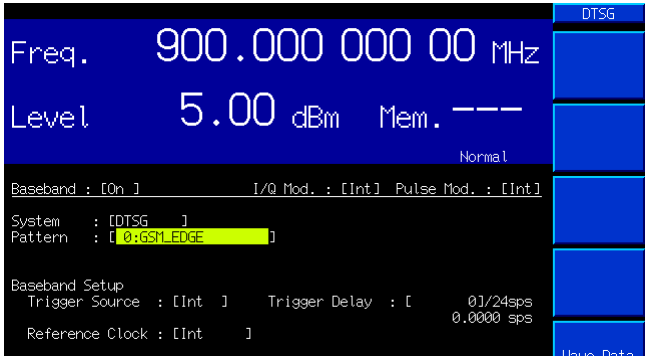




Adjacent channel leakage power ratio GSM/EDGE(8PSK), ≤ +5 dBm

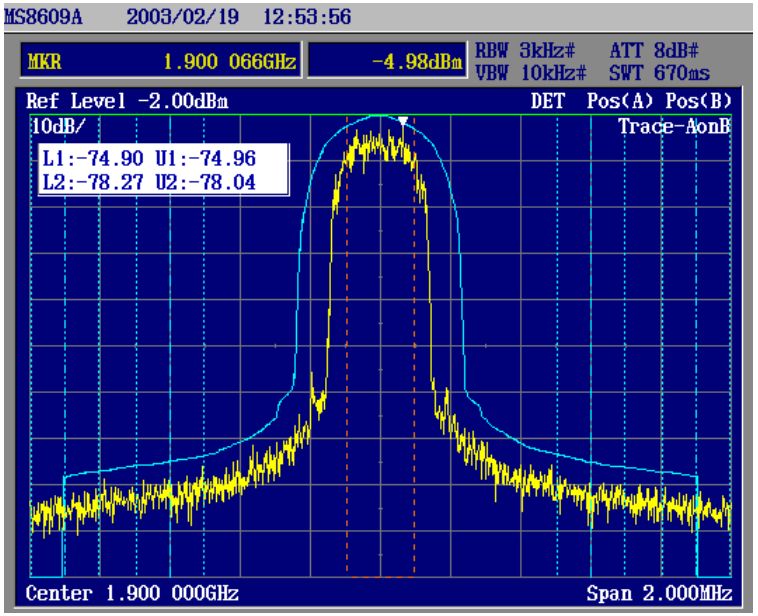
- ≤ -38 dBc/30kHz : 200 kHz offset
- ≤ -67 dBc/30kHz : 400 kHz offset

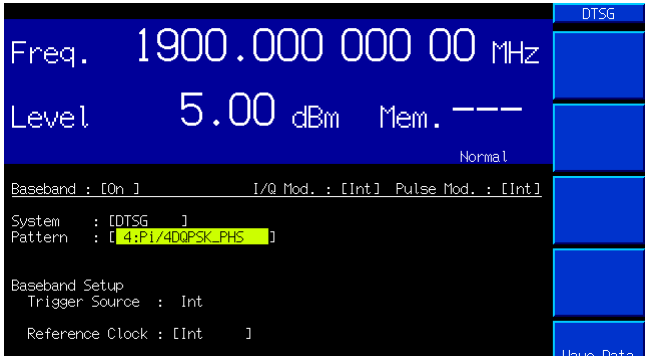




Adjacent channel leakage power ratio
PHS, ≤ +5 dBm

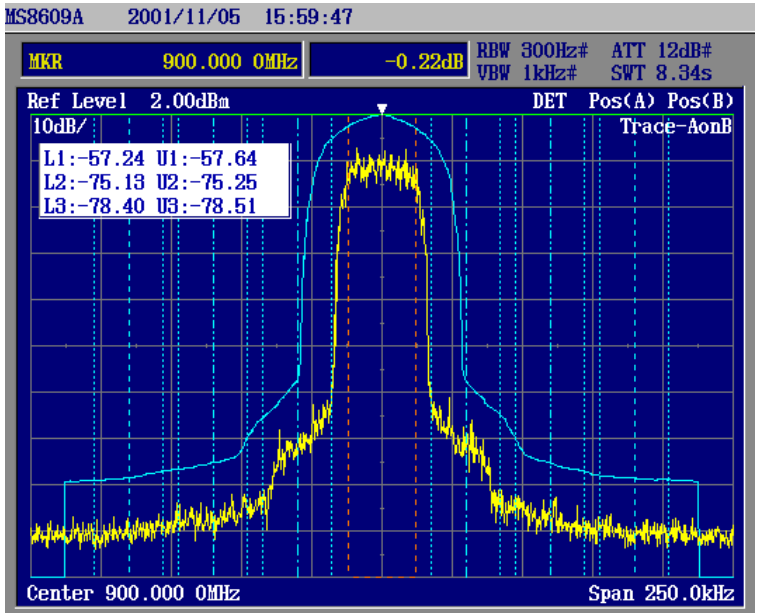
- ≤ -66 dBc/192kHz : 600 kHz offset
- ≤ -69 dBc/192kHz : 900 kHz offset

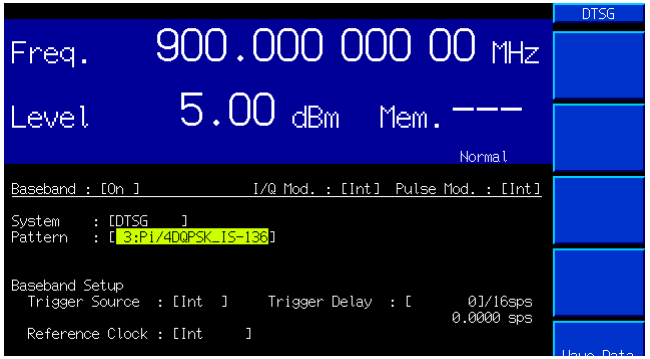




Adjacent channel leakage power ratio NADC(IS-136), ≤ +5 dBm

- ≤ -42 dBc/24.3kHz : 30 kHz offset
- ≤ -64 dBc/24.3kHz : 60 kHz offset
- ≤ -64 dBc/24.3kHz : 90 kHz offset

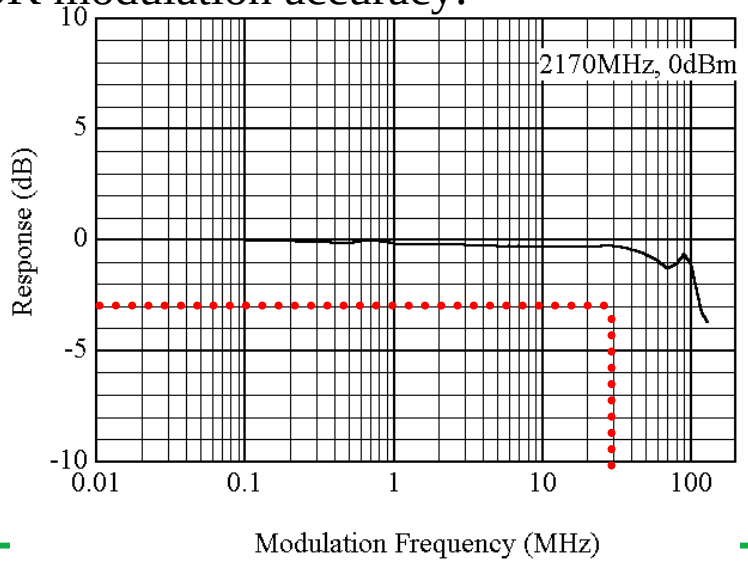


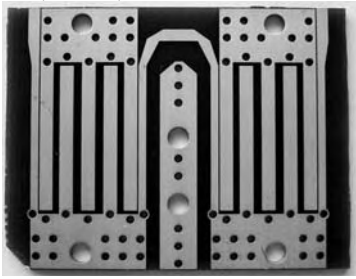


Wide-band and Excellent accuracy vector modulation

The filter group according to the output frequency is switched in RF circuit to attenuate the spurious close to carrier.
This filter group is the inter-digital band pass filter which can configure multi-stages in small area to satisfy out-band attenuation characteristic to eliminate the spurious in near-band, frequency response of vector modulation, pass band amplitude and group delay characteristic not to deteriorate vector modulation accuracy.

- Vector modulation frequency response (3 dB bandwidth): ≥ 30 MHz
- 3.84 Msps QPSK modulation accuracy: ≤ 2.5 %(rms)

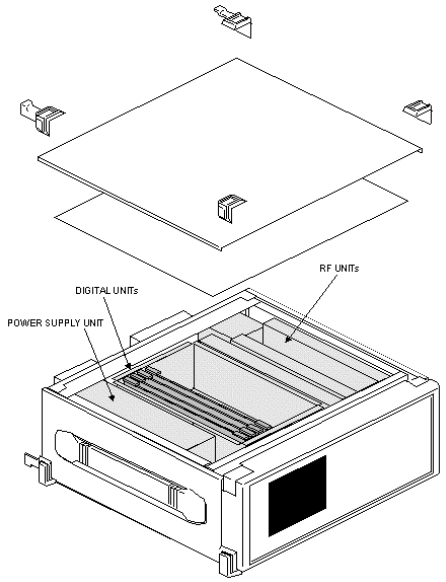




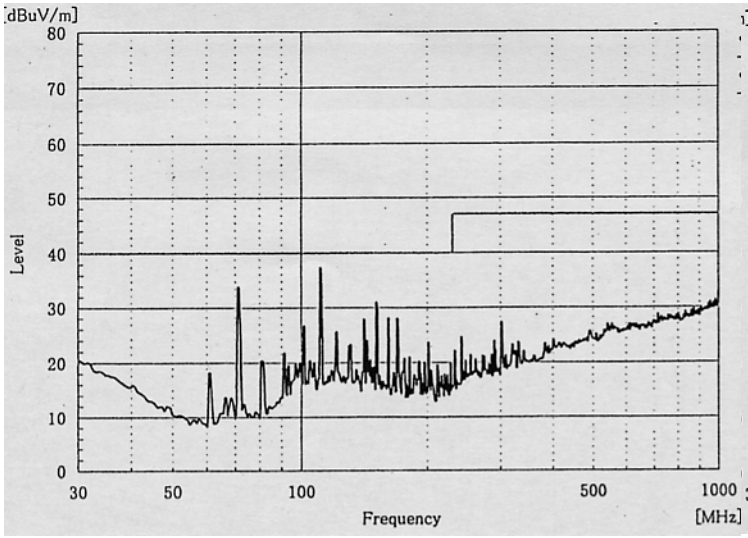
Leakage emissions policy

The shield of signal generator is important in minimizing the signal generator's leakage emissions which interfere to the receiver in receiver sensitivity test at low level.

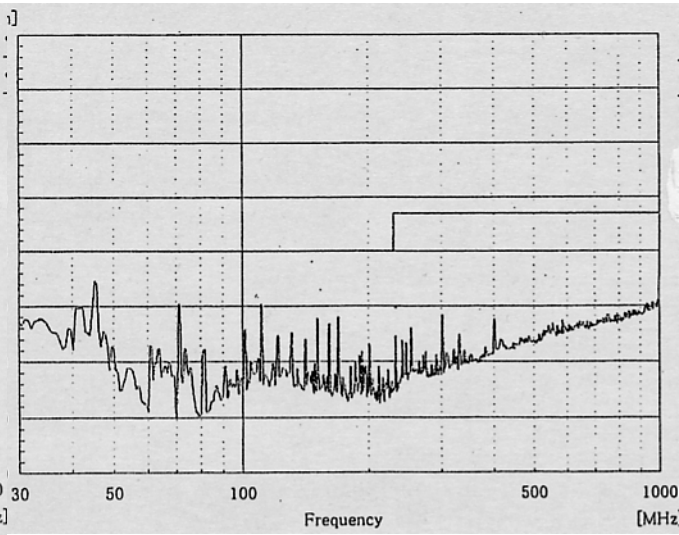
- » Mainframe cabinet has been structured with double shields.
- » The circuit units installed in mainframe have been mounted in the shield case, respectively.
- » Shield net has been equipped to display.
- » PC memory card interface has been equipped to rear panel.



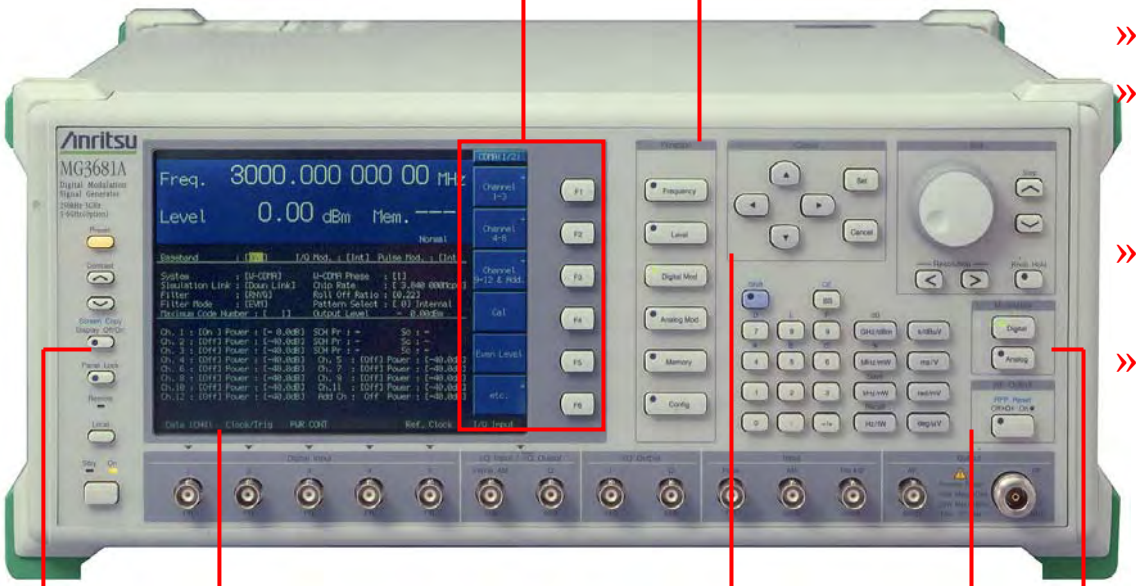
Horizontal



Vertical



Operability

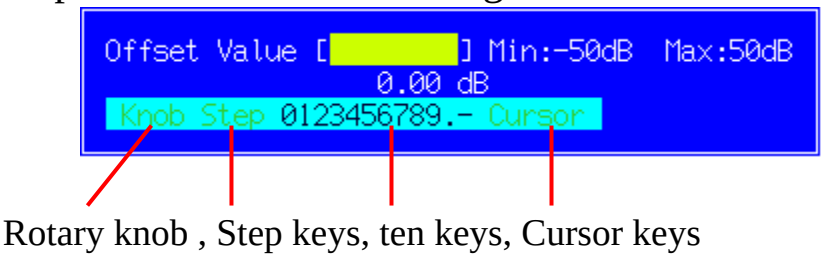


- **Function keys**
- **Editing keys**
  - » Frequency
  - » Output level
  - » Modulation parameters (Baseband)
    - – Digital
    - – Analog
  - » Internal memory administration
    - – Saving/Recall the setting situation
  - » System setting

    Main settings
    - – Screen saver ⇒ Power-saving
    - – Remote control
    - – Version information
    - – Operation time/count check
- **Cursor keys**
- **Color LCD**
  - » Color bmp files storage
    - – 640 x 480 pixel
- **Modulation On/Off**
  - – Digital
  - – Analog
- **RF output On/Off**

Operability

- **Panel key layout and role**
  - » Operability has been improved by panel layout considering smooth operation flow of [Selecting functions] → [Moving cursor] → [Editing(input/select)] → [Setting]
- **Operation guidance display**
  - » Panel operations include the parameter settings such as item selection, data input and character input. Available key types are displayed as guidance in pop-up window during parameter setting, in order to enable the operation without confusion.
    - Example of Level Offset setting



Operability

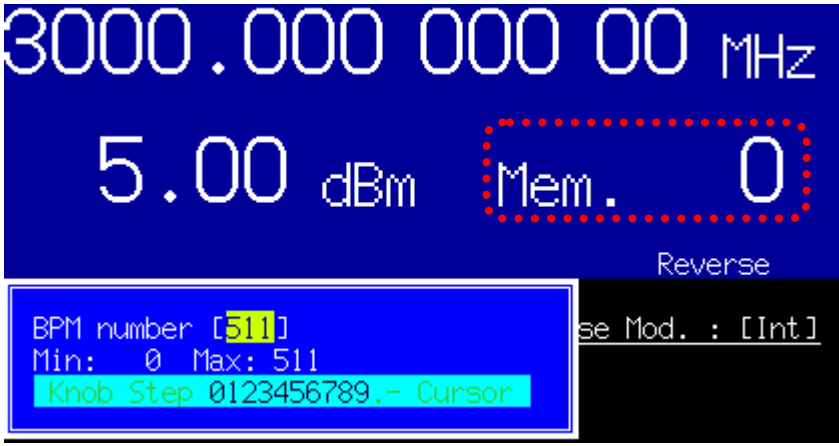
- **Modulation On/Off**
  - Digital: Vector modulation, Pulse modulation
  - Analog: AM, FM, ϕM
    - Internal analog modulation with AF signals of sine, triangular, square and sawtooth wave is possible at installing Option21 AF Synthesizer.

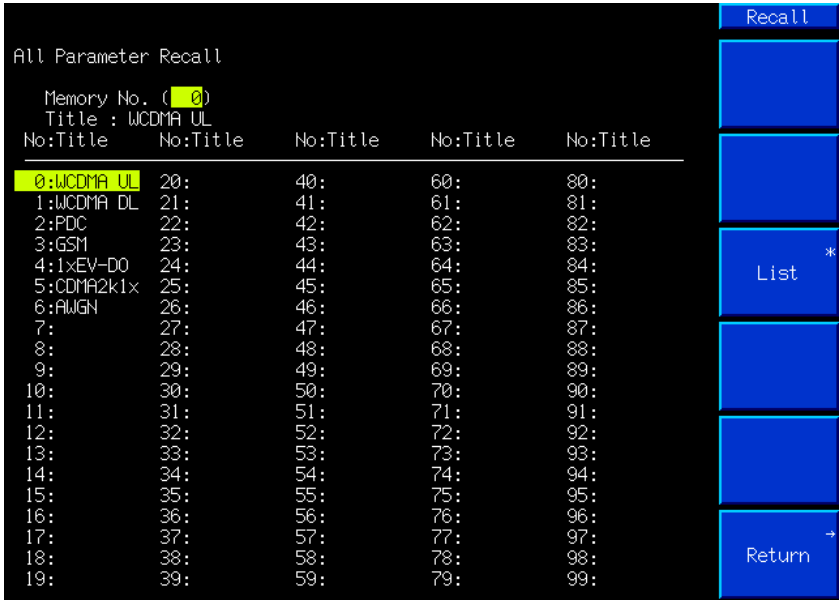
» These modulations are switched On or Off by one touch.

» The combination of digital modulation and analog modulation can achieve external ALC function by AM, also it is useful for the simulation of amplitude variation by AM and frequency variation by FM.

Operability

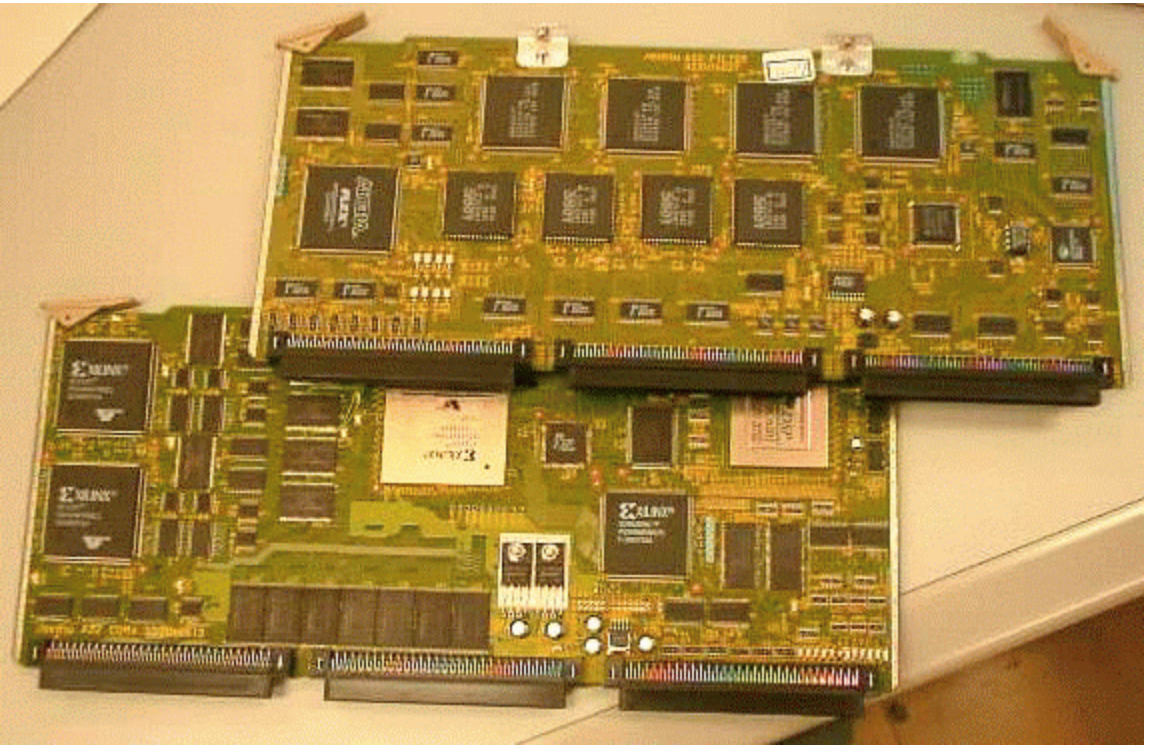
- **Internal memory administration**
  - » Basic Parameter Memory (BPM)
    - – 512 types of frequency and output level are savable.
    - – Sweepable continuous recall and high-speed recall by external trigger signal are performable.
  - » All Parameter Memory (APM)
    - – all settings including the modulation parameter setting of baseband in addition to frequency and output level are savable.
    - – 100 types of settings are savable regardless of the quantity of installed expansion units.
    - – Max. 8 characters can be inputted each title for easy confirmation.
  - » Memory Export/Import
    - – It is useful for copying to other MG3681A and backup of memory, because BPM and APM can be save in PC memory card and recalled from PC memory card.

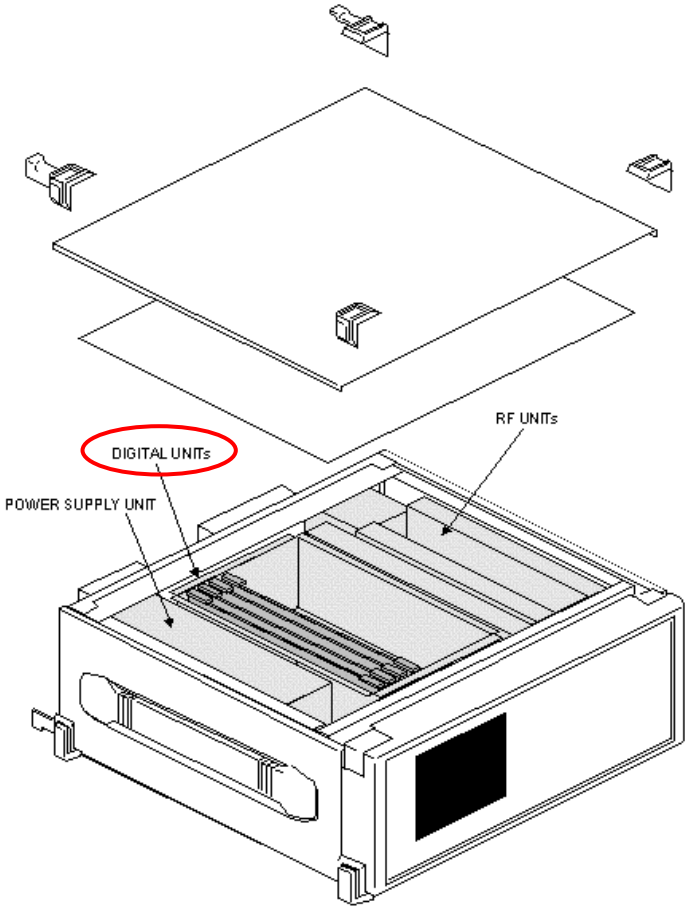




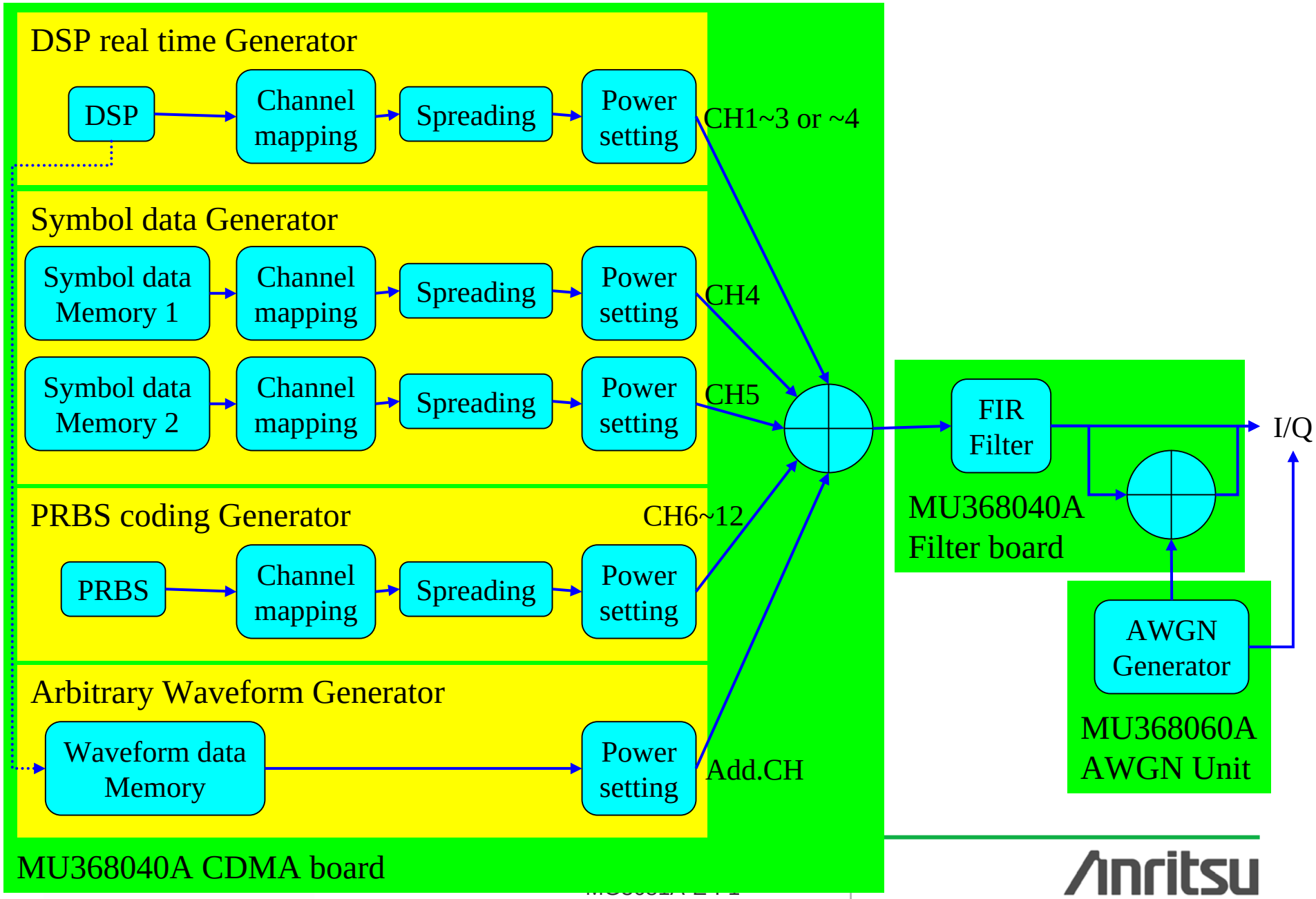
Expansion unit

- **Expansion unit is the digital board to generate digital I/Q signal of baseband.**
  - » Digital I/Q signal is converted to analog I/Q signal by D/A converter.





MU368040A CDMA Modulation Unit Block diagram



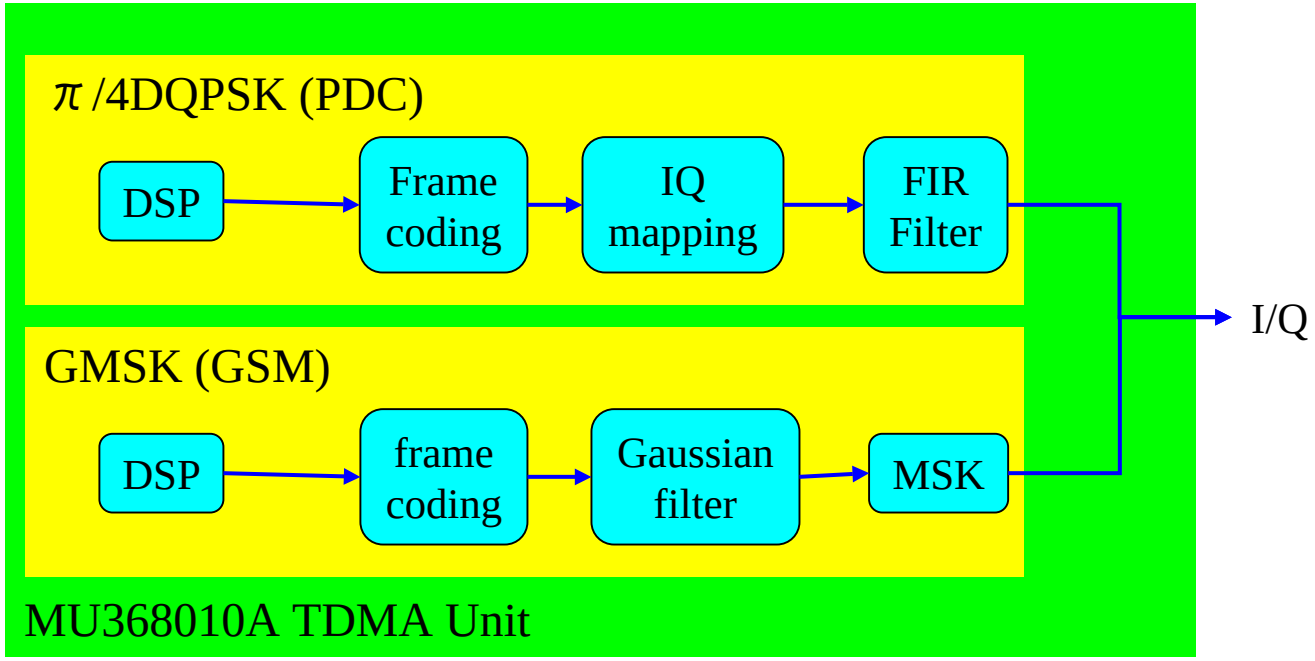
MU368040A CDMA Modulation Unit

- **DSP real time Generator**
  - » Mapping physical layer data achieved real-time coding by DSP to physical channel
- **Symbol data Generator**
  - » For the channels which require power/burst control per symbol such as W-CDMA DL-DPCH and PRACH
  - » Symbol signal pattern files of physical layer before spreading
    - – Downloading from PC memory card to internal memory
      - Internal memory capacity CH4: 4Mbit, CH5: 4Mbit
        - – W-CDMA Downlink ≤ 512 ksymbol e.g. DL-DPCH 30ksps: 1747 frame
        - – W-CDMA Uplink ≤ 1 Msymbol
- **PRBS coding Generator**
  - » Mapping PRBS(Pseudo-random Binary Sequence) data to physical channel
- **Arbitrary Waveform Generator**
  - » For multiple channels such as W-CDMA DPCH and OCNS
  - » Signal pattern files of physical layer before FIR filtering (before over sampling) *W-CDMA over sampling rate: 8× 3.84 Mcps = 30.72 MHz
    - – Downloading from PC memory card to internal memory
      - Internal memory capacity 512 ksamples/channel (2 Mbyte)
        - – W-CDMA 3.84 Mcps ≤ 13 frame (130 ms)

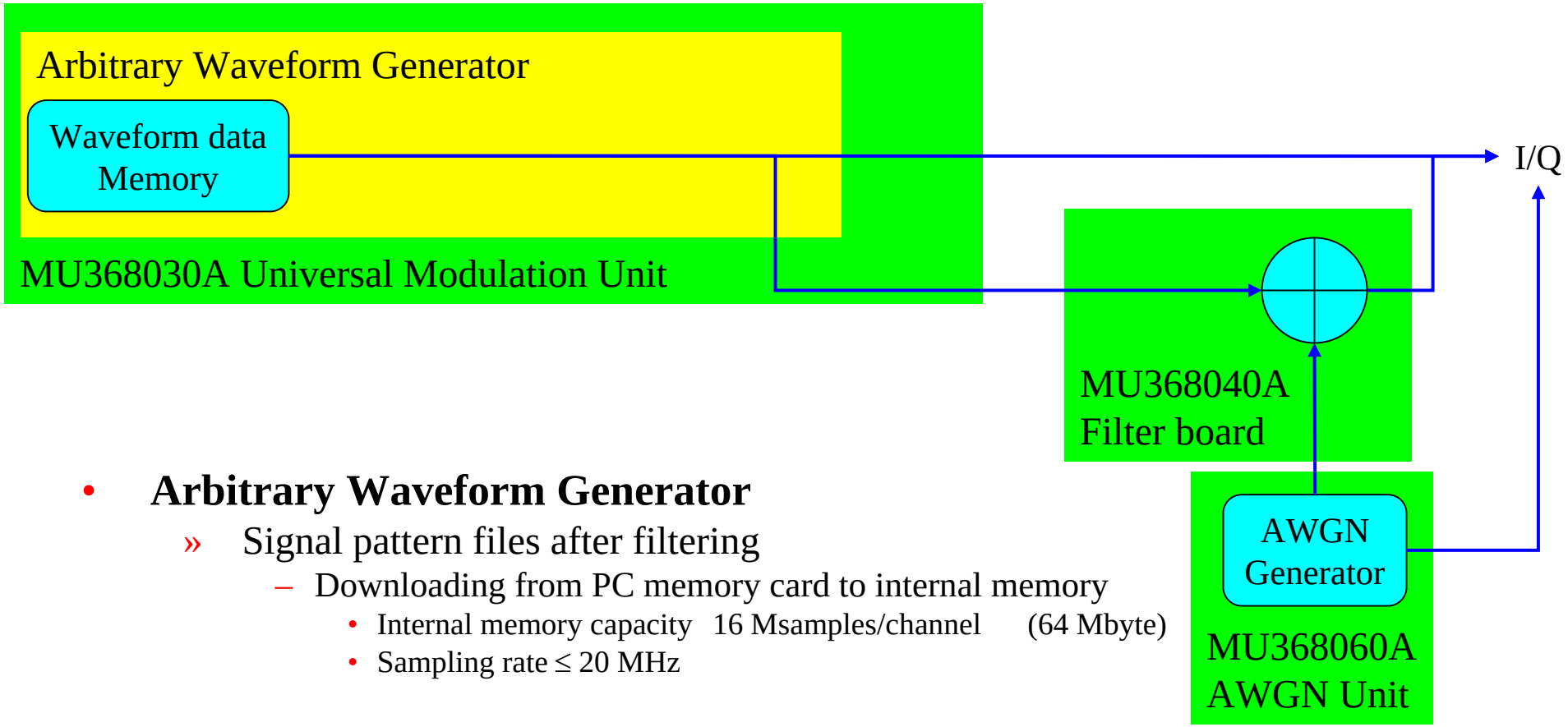
MU368040A CDMA Modulation Unit

- **Firmware configuration for flexible system support**
  - » Low-rate signal processor before spreading switches 2 methods according to the usage.
    - – Real-time coding method by DSP
    - – Memory method for downloading by cycle output of external created data pattern
  - » Signal processor from high-speed spreading to FIR filtering has been adopted high accumulation FPGA of 1M gates for flexible system support.
  - » These DSP programs, Signal pattern files for downloading and FPGA configuration data can be rewritten from PC memory card.
  - » FIR filter which requires high-speed processing has adopted the dedicated IC, as there is not the necessity for functional change.
- **High-speed data transmission**
  - – High-speed signal processing ability is required for baseband as W-CDMA specifies high-speed data communication up to 384kbps in moving state and up to 2Mbps in static state.
  - » Max. 1600MIPS of high-performance DSP has been adopted for real-time coding. It enables the real-time channel coding up to 384kbps.

MU368010A TDMA Modulation Unit Block diagram



MU368030A Universal Modulation Unit Block diagram



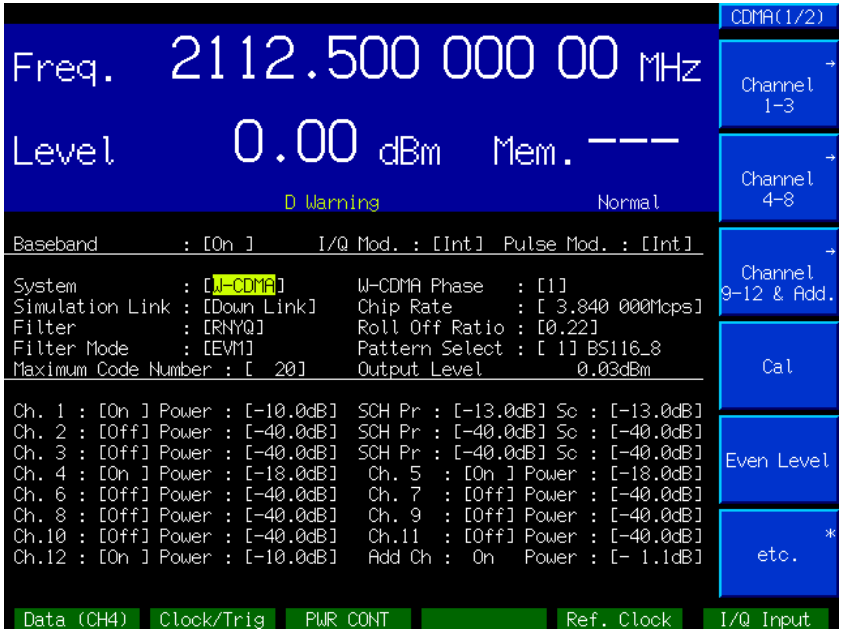
- **Arbitrary Waveform Generator**
  - » Signal pattern files after filtering
    - – Downloading from PC memory card to internal memory
      - Internal memory capacity 16 Msamples/channel (64 Mbyte)
      - Sampling rate ≤ 20 MHz

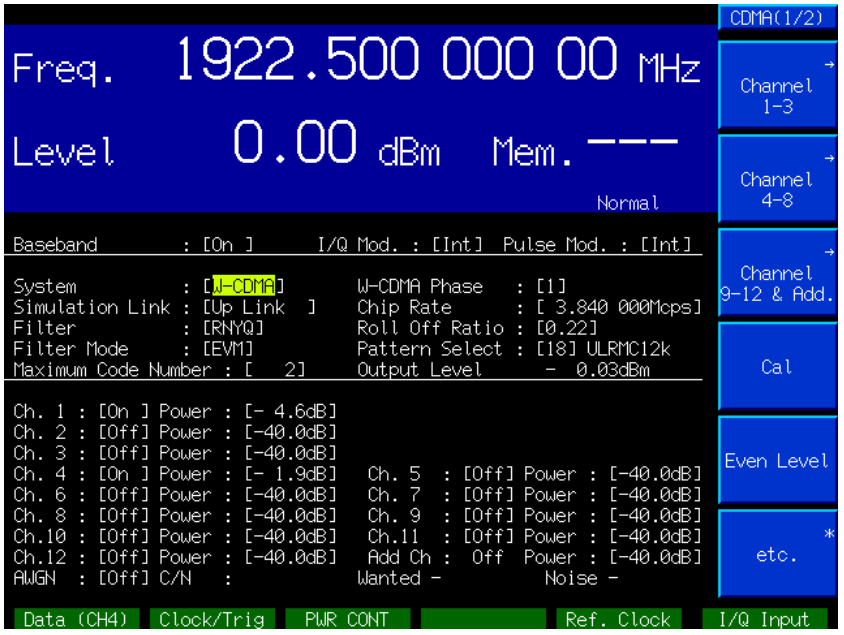
Software

- MX368041B W-CDMA Software 54
  - MX368041B-11 HSDPA Signal Pattern 56
  - MX368141A HSDPA IQ producer 73
- MX368042A IS-95 Device Test Software 77
- MX368011A PDC Software 84
- MX368012A GSM Device Test Software 92
- MX368031A Device Test Signal Generation Software 102
- MX368033A CDMA2000 1xEV-DO Signal Generation Software 111
  - » MX368133A CDMA2000 1xEV-DO IQproducer™ 120
- MX368034A PDC Packet Software 126
- MX368035A PHS Signal Generation Software 133
- MU368060A AWGN 141

MX368041B W-CDMA Software

- **Downlink/Uplink W-CDMA test signals for 3GPP(FDD) standard can be outputted by installing the MX368041B W-CDMA Software in the MU368040A CDMA Modulation Unit.**
- **In R&D/production process of components, base stations (BS) and user equipment (UE), the functions to support various applications are provided as the signal source for components, the wanted signal source and the interfering signal source for receiver test.**





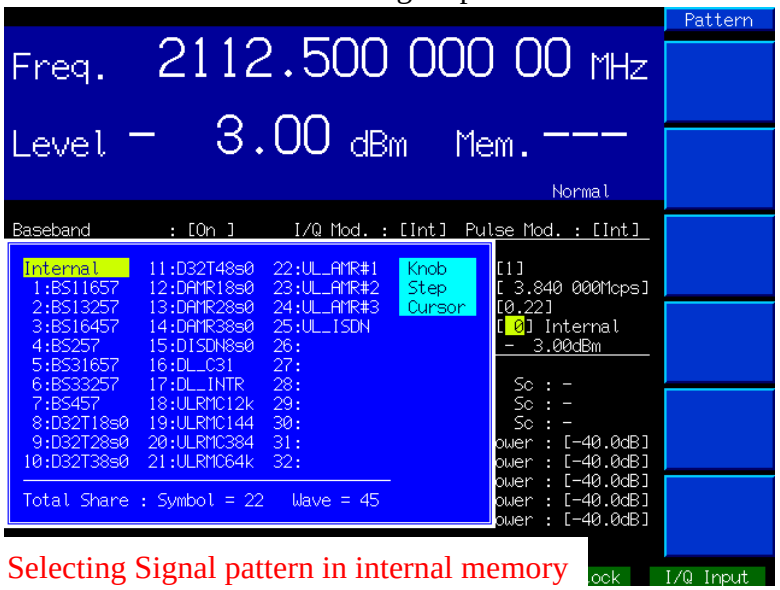
Support of test signal format

- **Just to select the signal patterns for TS 25.141 and TS 34.121 test specifications without setting complicated parameters of 3GPP!**

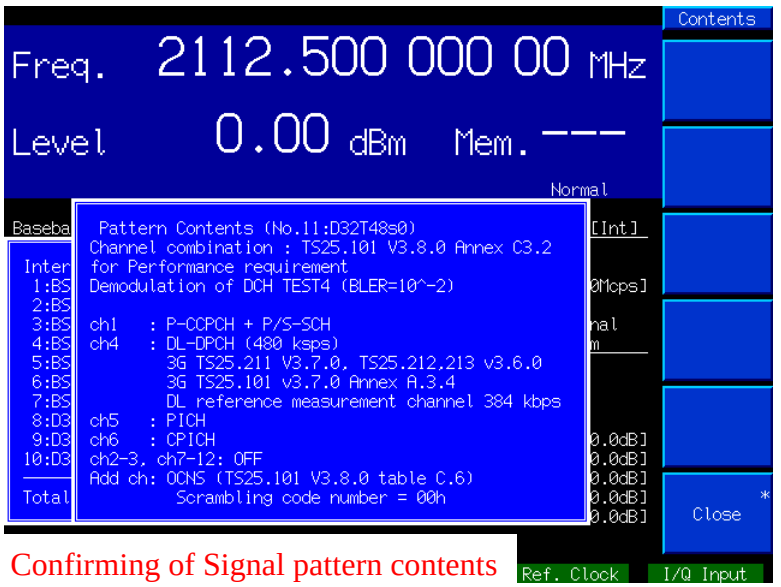
  Simple operation

- **Quick support is provided by updating the signal pattern files saved from PC memory card to internal memory and DSP program for real-time coding.**
  - » Supporting 3GPP update and special signal patterns
    - – "Product Introduction MX368041A/B Update News" is provided.

      Version-up History, How to check Version, How to upgrade, File configuration in PC memory card, Signal pattern List



Selecting Signal pattern in internal memory

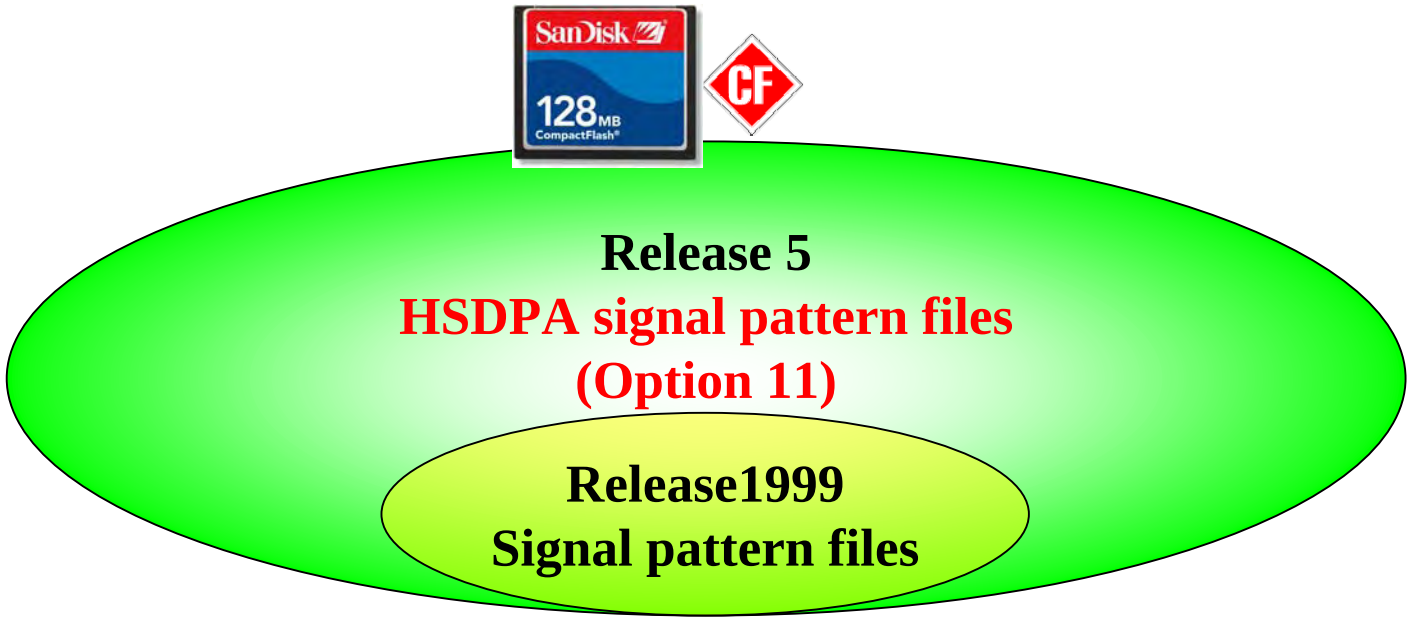


Confirming of Signal pattern contents

Pattern files of test signal format

MX368041B-11 (Option)　HSDPA Signal Pattern

» This package added the signal pattern file specified in Release5 to Release1999 signal pattern file of an appendix in MX368041B.



Signal patterns For evaluating components in BS transmitter

Test item	Channel combination	Parameter	Patt. name	Added by option11	
TS25.141 6.1.1 Transmitter Test Models	TS25.141 6.1.1.1 Test Model 1	16 DPCH	BS11657 BS116571 BS116572 BS116573	B11657d B11657d2	
		32 DPCH	BS13257 BS132571 BS132572 BS132573	B13257d B13257d2	
		64 DPCH	BS16457 BS164571 BS164572 BS164573	B16457d B16457d2	
	TS25.141 6.1.1.2 Test Model 2	-	BS257 BS2571 BS2572 BS2573		
	TS25.141 6.1.1.3 Test Model 3	16 DPCH	BS31657 BS316571 BS316572 BS316573		
		32 DPCH	BS33257 BS332571 BS332572 BS332573		
	TS25.141 6.1.1.4 Test Model 4	-	BS457 BS4571 BS4572 BS4573		
	TS25.141 6.1.1.4A Test Model 5	2 HS-PDSCH + 6 DPCH		BS5_257 BS5_2571 BS5_2572 BS5_2573	B5_257d B5_257d2
		4 HS-PDSCH + 14 DPCH		BS5_457 BS5_4571 BS5_4572 BS5_4573	B5_457d B5_457d2
		8 HS-PDSCH + 30 DPCH		BS5_857 BS5_8571 BS5_8572 BS5_8573	B5_857d B5_857d2

» Test Models

– 6.1.1.1
Test Model 1 Multi-carrier
(2 carriers)

2 carriers
******d: for lower freq.
******d2: for higher freq.

– 6.1.1.4A
Test Model 5 (HSDPA)
- Multi-carrier (2 carriers)

Signal patterns For receiver and performance testing for BS

Test item	Channel combination	Parameter	Patt. name	Added by option11	
TS25.141	TS25.141 Annex A.1	TS25.141 Annex A.2	ULRMC12k		
7 Receiver characteristics		TS25.141 Annex A.3	ULRMC64k		
8 Performance requirement		TS25.141 Annex A.4	ULRMC144		
		TS25.141 Annex A.5	ULRMC384		
8.8.1 RACH preamble	TS25.211 5.2.2.1	TS25.213 4.3.3		PRE	
8.8.3 RACH message		TS25.141 Annex A.7		R168	R360
8.9.3 CPCH message	TS25.211 5.2.2.2	TS25.141 Annex A.8		C168	C360
8.10 SSDT	TS25.141 Annex A.1	TS25.141 Annex A.2		SSDTa	SSDTb
-	TS25.104 Annex A.1	TR25.944 4.1.2.2.1.1 DCCH 4.1.2.2.1.2 AMR TFCS#1 4.1.2.2.2.2	UL_AMR#1		
		TR25.944 4.1.2.2.1.1 DCCH 4.1.2.2.1.2 AMR TFCS#2 4.1.2.2.2.2	UL_AMR#2		
		TR25.944 4.1.2.2.1.1 DCCH 4.1.2.2.1.2 AMR TFCS#3 4.1.2.2.2.2	UL_AMR#3		
		TR25.944 4.1.2.2.1.1 DCCH 4.1.2.2.1.6 ISDN 4.1.2.2.2.2	UL_ISDN		

- 8.8 RACH performance
  - 8.8.1 RACH preamble detection in static propagation conditions
  - 8.8.2 RACH preamble detection in multipath fading case 3
  - 8.8.3 Demodulation of RACH message in static propagation conditions
  - 8.8.4 Demodulation of RACH message in multipath fading case 3
- 8.9 CPCH Performance
  - 8.9.3 Demodulation of CPCH message in static propagation conditions
  - 8.9.4 Demodulation of CPCH message in multipath fading case 3
- 8.10 Site Selection Diversity Transmission (SSDT) Mode

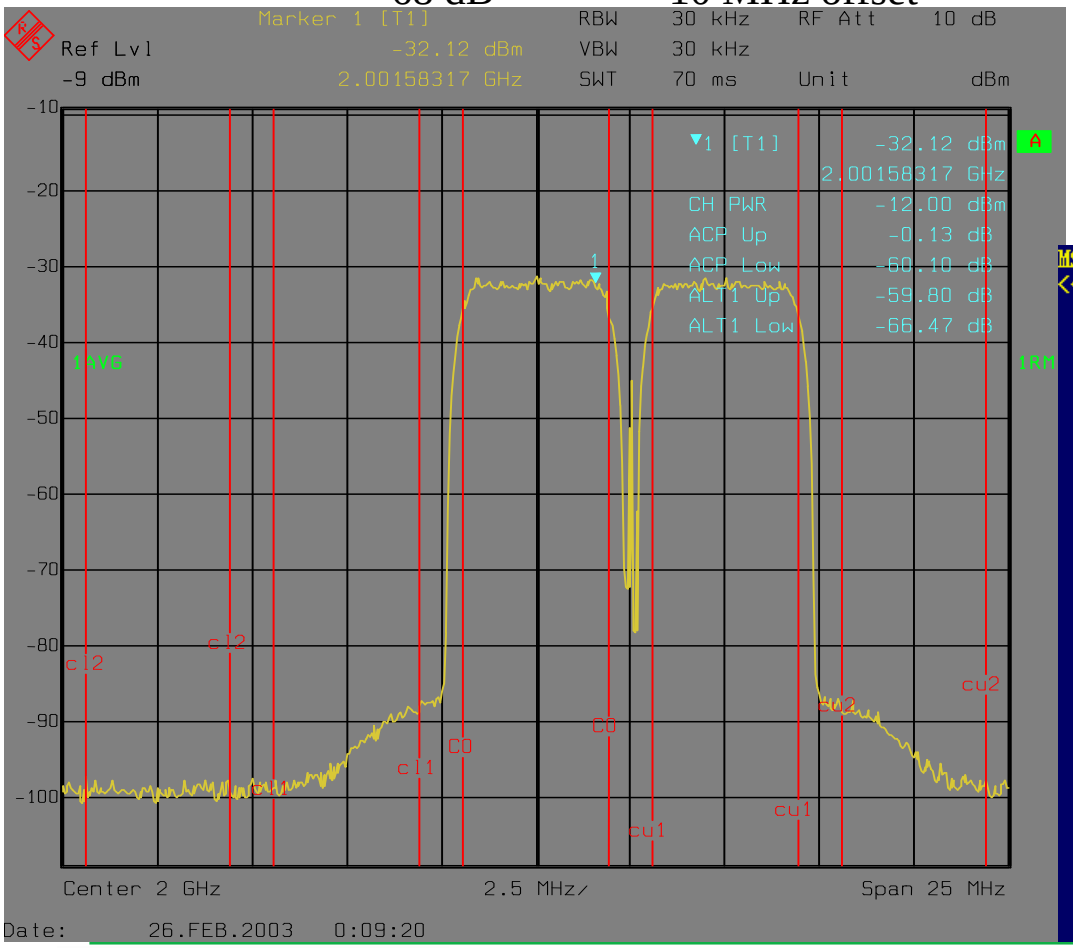
Signal patterns For receiver and performance testing for UE

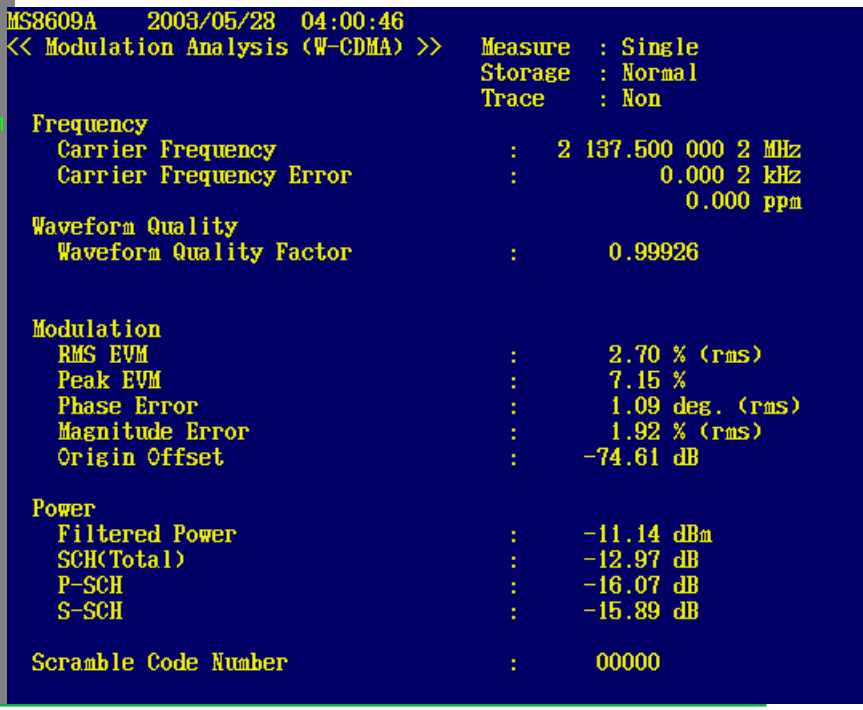
Test item	Channel combination	Parameter	Patt. name	Added by option11				
TS25.101	TS25.101 Annex C.3.1	TS25.101 Annex A.3.1	DL_C31					
7 Receiver characteristics 8 Performance requirement	TS25.101 Annex C.3.2		D32T18s0 D32T18s8 D32T18s9					
		TS25.101 Annex A.3.2	D32T28s0 D32T28s8 D32T28s9					
		TS25.101 Annex A.3.3	D32T38s0 D32T38s8 D32T38s9					
		TS25.101 Annex A.3.4	D32T48s0 D32T48s8 D32T48s9					
	TS25.101 Annex C.4		DL_INTR					
8.3 in multi-path (Case7) Test21~25	TS25.101 Annex C.3.5	TS25.101 Annex A.4A		4Ps0 4Ps8 4Ps9				
8.6.1 open-loop transmit diversity	TS25.101 Annex C.3.3	TS25.101 Annex A.3.1		OTD1s0 OTD1s8 OTD1s9	OTD2s0 OTD2s8 OTD2s9			
8.9 Downlink compressed mode	TS25.101 Annex C.3.2	TS25.101 Annex A.5		DCP11540 DCP11548 DCP11549	DCP12540 DCP12548 DCP12549	DCP21540 DCP21548 DCP21549	DCP22540 DCP22548 DCP22549	DCP23540 DCP23548 DCP23549
8.10 BTFD		TS25.101 Annex A.4		BTFD1s0 BTFD1s8 BTFD1s9	BTFD2s0 BTFD2s8 BTFD2s9	BTFD3s0 BTFD3s8 BTFD3s9		
8.12 PCH		TS25.101 Annex A.6		PCHs0 PCHs8 PCHs9				
7.4.2 Maximum input level HS-PDSCH 9 Performance requirement (HSDPA)	TS25.101 Annex C.5.1 Table C.8	TS25.101 Annex A.7.1		F1P0s0 F1A0s0 F2P0s0 F2A0s0 F3P0s0 F3A0s0 F4P0s0 F5P0s0				
-	TS25.101 Annex C.3.2	TR25.944 4.1.1.3.1.1 DCCH 4.1.1.3.1.2 AMR TFCS#1 4.1.1.3.2.2	DAMR18s0 DAMR18s8 DAMR18s9					
		TR25.944 4.1.1.3.1.1 DCCH 4.1.1.3.1.2 AMR TFCS#2 4.1.1.3.2.2	DAMR28s0 DAMR28s8 DAMR28s9					
		TR25.944 4.1.1.3.1.1 DCCH 4.1.1.3.1.2 AMR TFCS#3 4.1.1.3.2.2	DAMR38s0 DAMR38s8 DAMR38s9					
		TR25.944 4.1.1.3.1.1 DCCH 4.1.1.3.1.6 ISDN 4.1.1.3.2.5	DISDN8s0 DISDN8s8 DISDN8s9					

- 8.3
  Demodulation of DCH in multi-path fading propagation conditions
  - (Case 7) Test 21~25
- 8.6
  Demodulation of DCH in downlink Transmit diversity modes
  - 8.6.1
    Demodulation of DCH in open-loop Transmit diversity mode
- 8.9
  Downlink compressed mode
- 8.10
  Blind transport format detection (BTFD)
- 8.12
  Demodulation of Paging Channel (PCH)
- 7.4
  Maximum input level
  - 7.4.2 HS-PDSCH for 16QAM
- 9
  Performance requirement (HSDPA)

Multi-carrier typical ACLR

- **Test Model 1: 64 DPCH, ≤ -8 dBm**
  - -60 dB 5 MHz offset
  - -68 dB 10 MHz offset





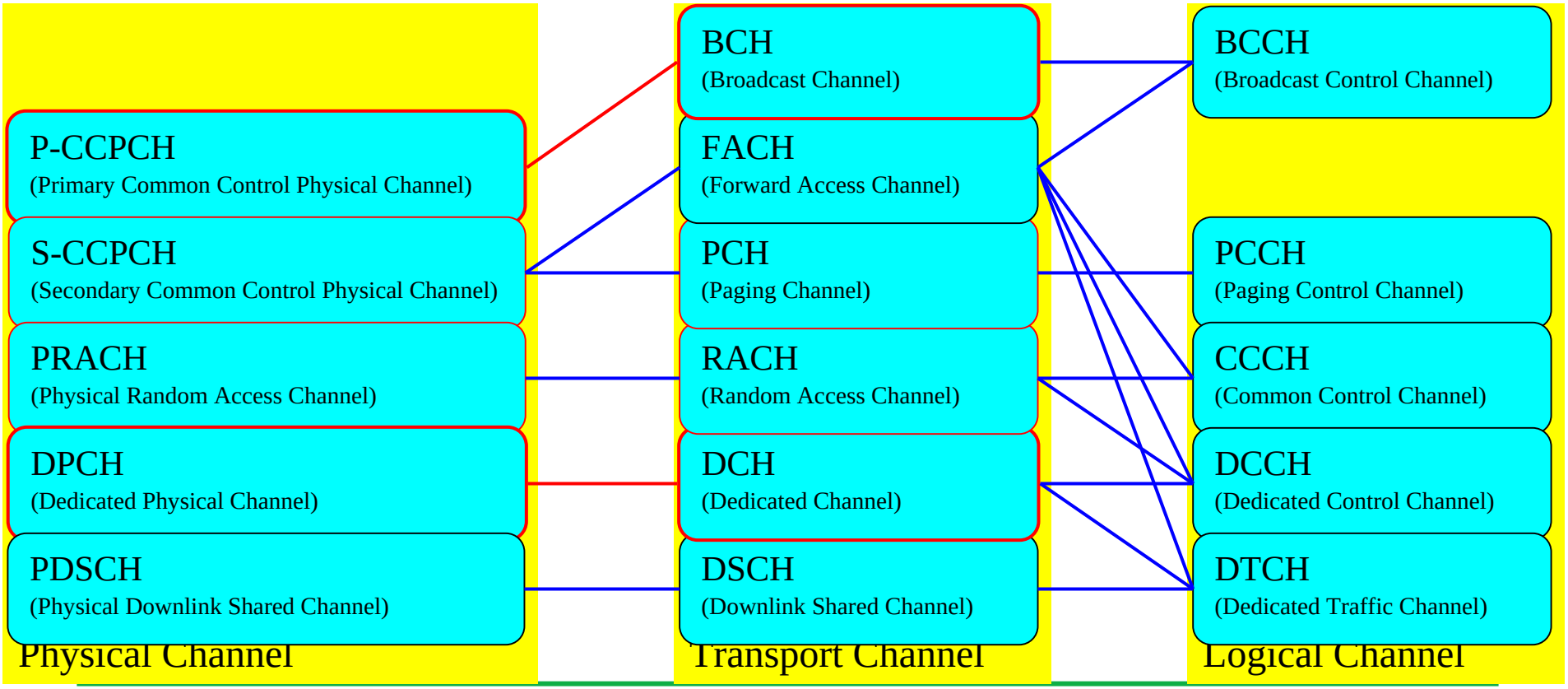
Real-time generation of test signal format

- **Simple editing on display**

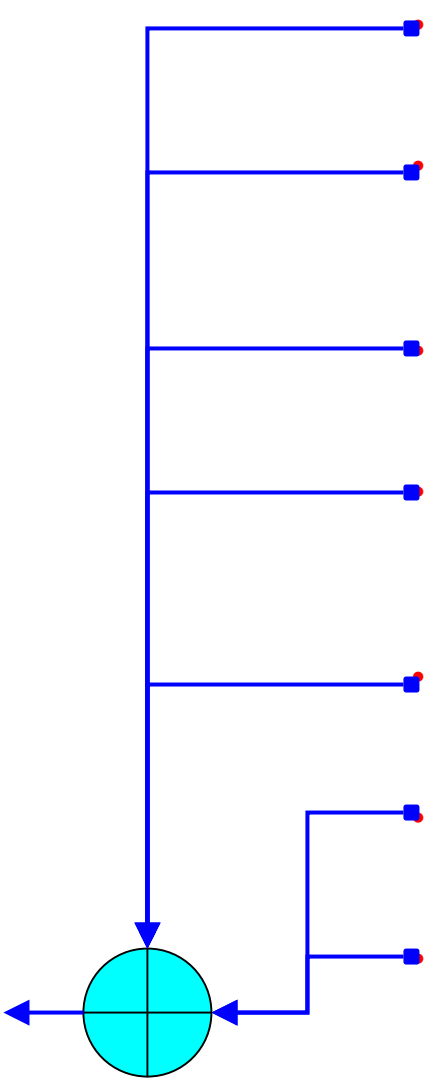
  Supporting various test cases

  » Parameters for 5 types of physical channels and 2 types of transport channels

For reference) Mapping relations among main physical channels, transport channels and logical channels

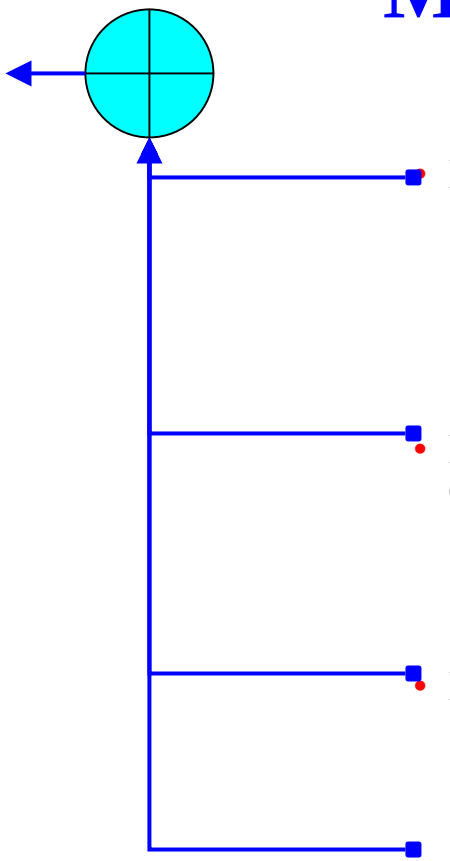


Main physical channels for test



- P-CPICH (Primary Common Pilot Channel)
  - Downlink common channel
  - Used as a phase reference for downlink channel estimation
- S-CPICH (Secondary Common Pilot Channel)
  - Downlink common channel
  - Used when applying Adaptive Array Antenna
  - Phase reference of S-CPICH during test: P-CPICH180° offset
- P-CCPCH (Primary Common Control Physical Channel)
  - Downlink common channel
  - Sends the system and cell information
- S-CCPCH (Secondary Common Control Physical Channel)
  - Downlink common channel
  - Sends PCH Paging Channel for paging signal and FACH Forward Access Channel for control information and user data (low rate)
- PICH (Page Indication Channel)
  - Downlink common channel
  - Sends Paging indicator for notifying existence of paging to UE
- P-SCH (Primary Synchronization Channel)
  - Downlink common channel
  - Used for UE cell search (slot synchronization)
- S-SCH (Secondary Synchronization Channel)
  - Downlink common channel
  - Used for UE cell search (frame synchronization and knowing Scrambling code group)

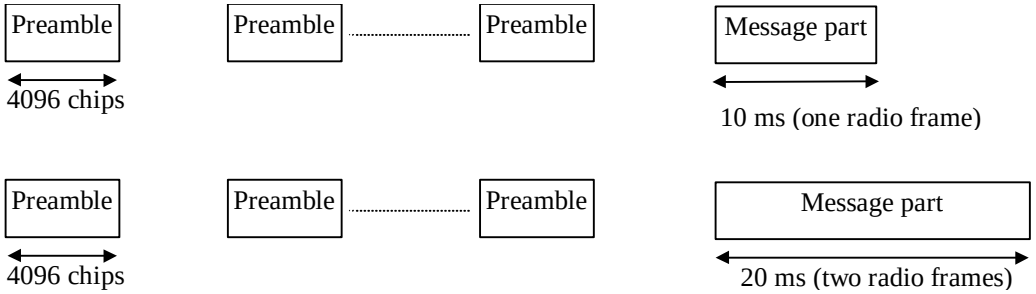
Main physical channels for test



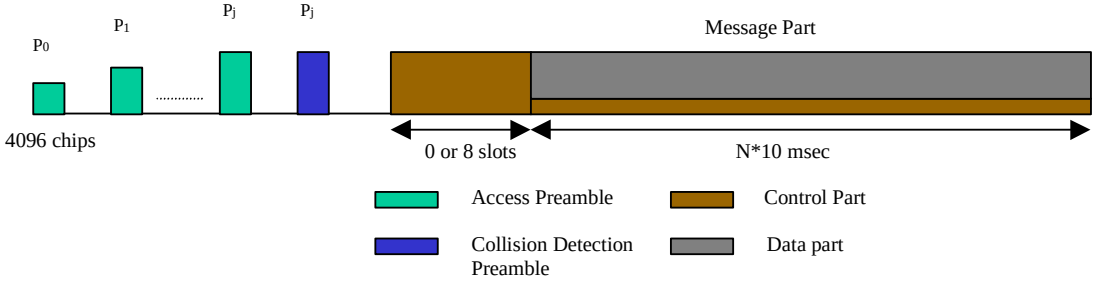
- DPCH (Dedicated Physical Channel)
  - Allocated to each UE
  - Downlink: Time multiplexing of DPDCH Dedicated Physical Data Channel and DPCCH Dedicated Physical Control Channel in time slot
  - Uplink: I/Q multiplexing of DPDCH, DPCCH and HS-DPCCH Dedicated Physical Control Channel (uplink) for HSDPA
- HS-SCCH (Shared Control Channel for HS-DSCH High Speed Downlink Shared Channel)
  - Downlink common channel for HSDPA
  - Maximum of 4 channels per HS-SCCH set
  - Used for HS-PDSCH allocation
- HS-PDSCH (High Speed Physical Downlink Shared Channel)
  - Downlink common channel for HSDPA
  - Sends HS-DSCH for packet data
  - Slot format #0: QPSK, 1#: 16QAM
- OCNS (Orthogonal Channel Noise Simulator)
  - Interfering channel to simulate other users channels on downlink

Main physical channels for test

- PRACH (Physical Random Access Channel)
  - Uplink common channel
  - Sends RACH for control information and user data (low rate)



- PCPCH (Physical Common Packet Channel)
  - Uplink common channel
  - Sends CPCH for user packet data (high rate)



Real-time generation of Downlink physical channel

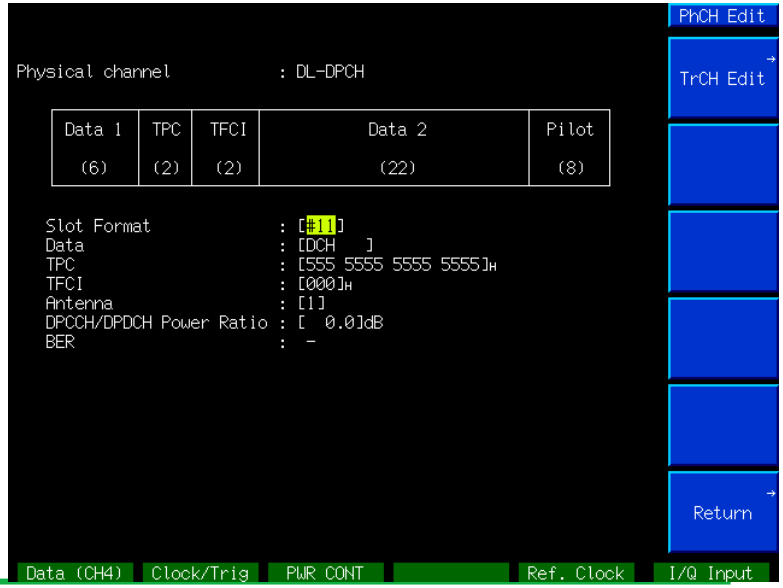
- P-CCPCH (CH1~3)
  - BCH transport channel mapping
  - SCH TSDT: On, Off
    - TSDT
      - Time Switched TX Diversity
      - Open loop mode
      - Switching TX antenna (SCH) per slot
- CPICH (CH1~3)
  - Antenna: 1,2
    - For TX diversity
    - STTD encoding (Antenna: 2)
    - STTD
      - Space Time Block Coding Based Transmit Antenna Diversity
      - Open loop mode
      - Controlling Symbol patterns on antenna2 side
- DPCH (CH4)
  - DCH transport channel mapping
  - Slot format: #0 to #15
  - TPC: TPC command of 4 frames (60 slots) cycle
    - TPC
      - Transmit Power Control
      - Closed loop power control

        * Inner loop power control

        Controlling to equalize with target SIR

        * Outer loop power control

        Correcting target SIR to equalize with target BER/BLER



Real-time generation of Uplink physical channel

- DPCCH (CH1~3)
  - Slot format: #0, #2, #5
  - TPC: TPC command of 4 frames (60 slots) cycle
    - TPC
      - Transmit Power Control
      - Closed loop power control

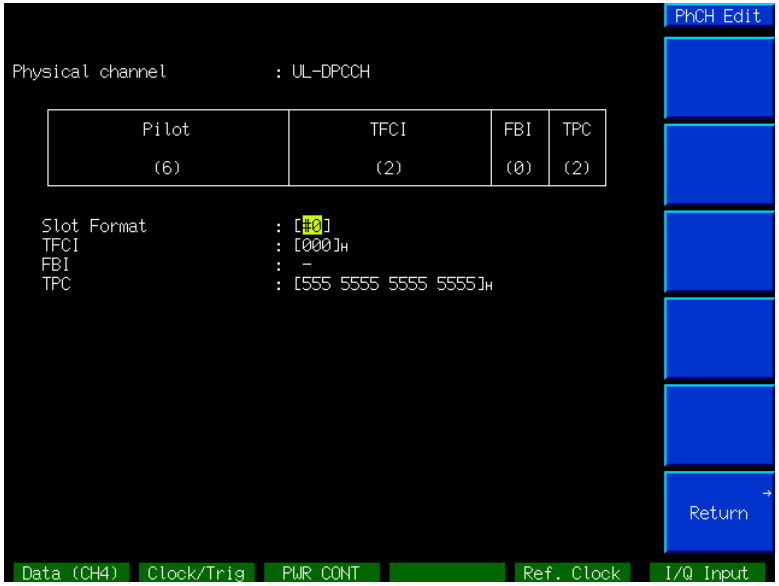
        * Inner loop power control

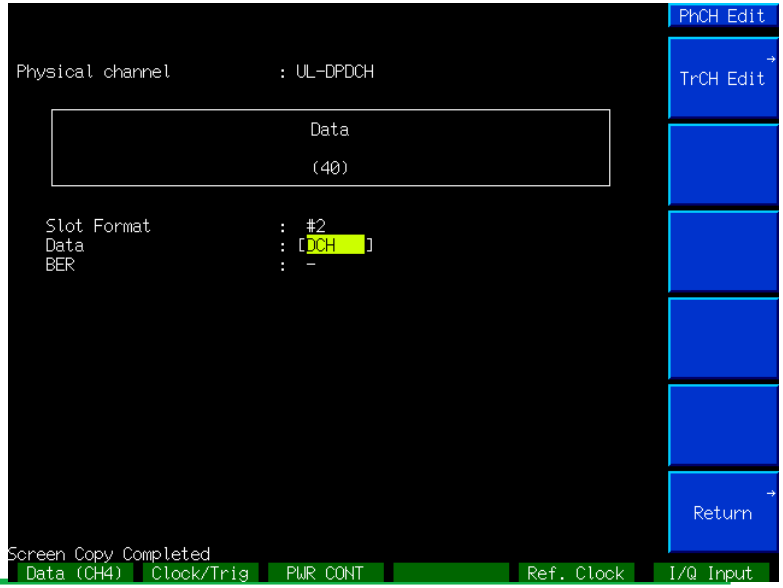
        Controlling to equalize with target SIR

        * Outer loop power control

        Correcting target SIR to equalize with target BER/BLER

- DPDCH (CH4)
  - DCH transport channel mapping





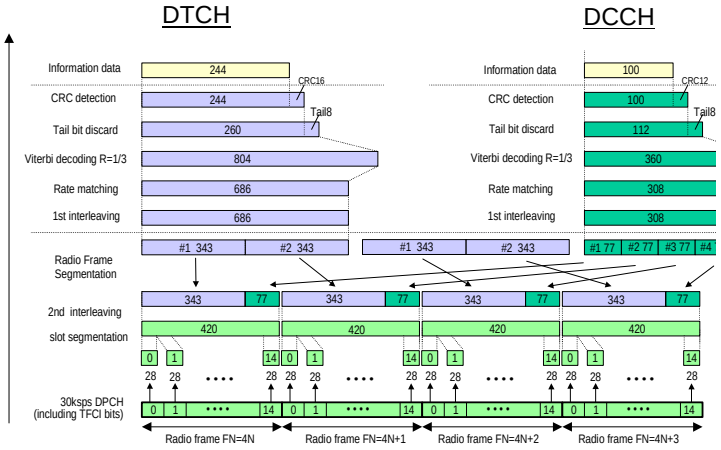
Real-time generation of Downlink transport channel

- BCH (P-CCPCH data)
  - 3GPP TS 25.944

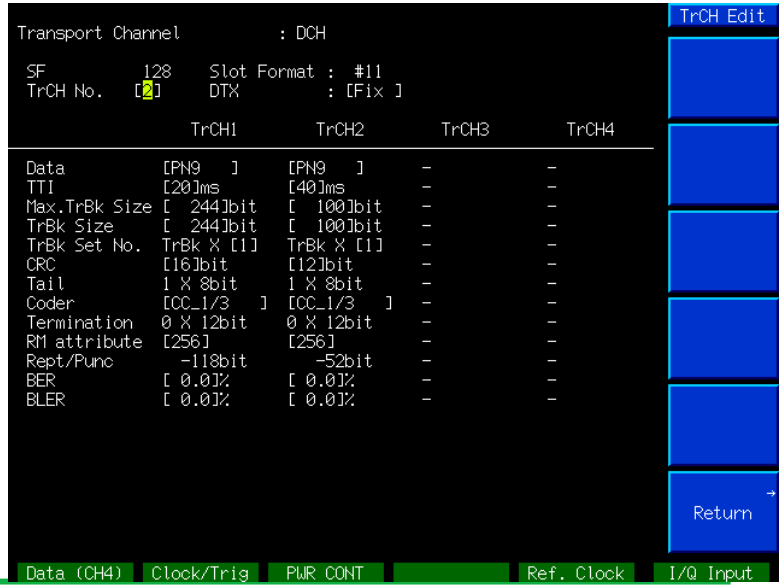
Transport block size	246
CRC	16 bits
Coding	CC, coding rate = 1/2
TTI	20 ms
The number of codes	1
SF	256

- DCH (DPCH data)
  - 3GPP TS 25.101

Parameter	TrCH1 DTCH	TrCH2 DCCH
Transport Channel Number	1	2
Transport Block Size	244	100
Transport Block Set Size	244	100
Transmission Time Interval	20 ms	40 ms
Type of Error Protection	Convolution Coding	Convolution Coding
Coding Rate	1/3	1/3
Rate Matching attribute	256	256
Size of CRC	16	12
Position of TrCH in radio frame	fixed	fixed



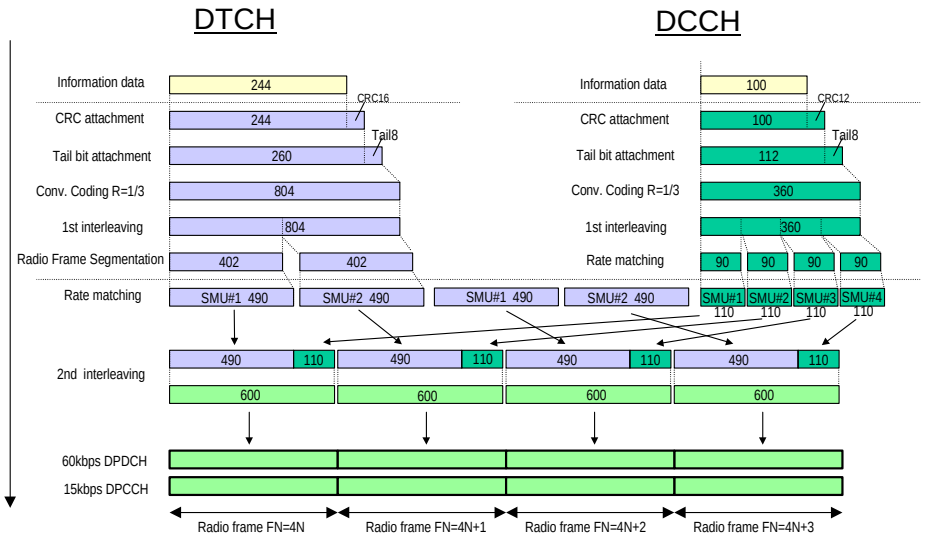
- BER, BLER
  - Generating the error
  - 0 to 10 %, 0.1 % resolution

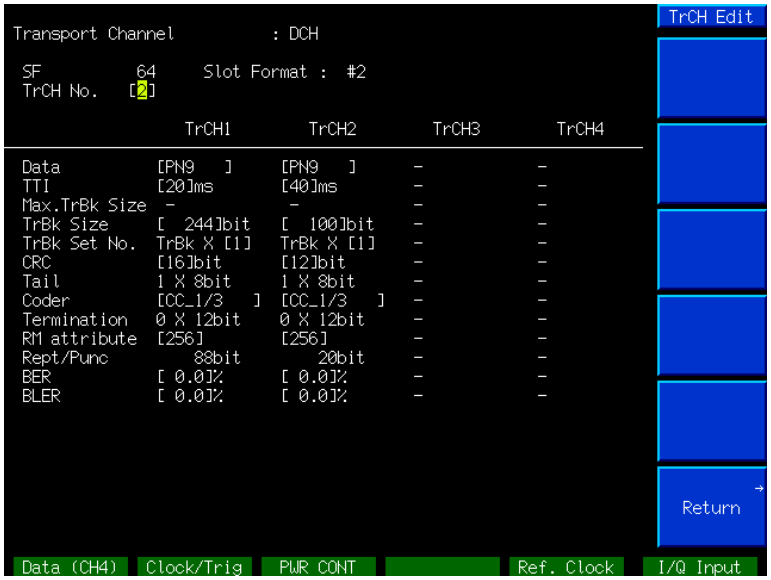


Real-time generation of Uplink transport channel

- DCH (DPDCH data)
  - 3GPP TS 25.101

	TrCH1	TrCH2
Parameters	**DTCH**	**DCCH**
Transport Channel Number	1	2
Transport Block Size	244	100
Transport Block Set Size	244	100
Transmission Time Interval	20 ms	40 ms
Type of Error Protection	Convolution Coding	Convolution Coding
Coding Rate	1/3	1/3
Rate Matching attribute	256	256
Size of CRC	16	12



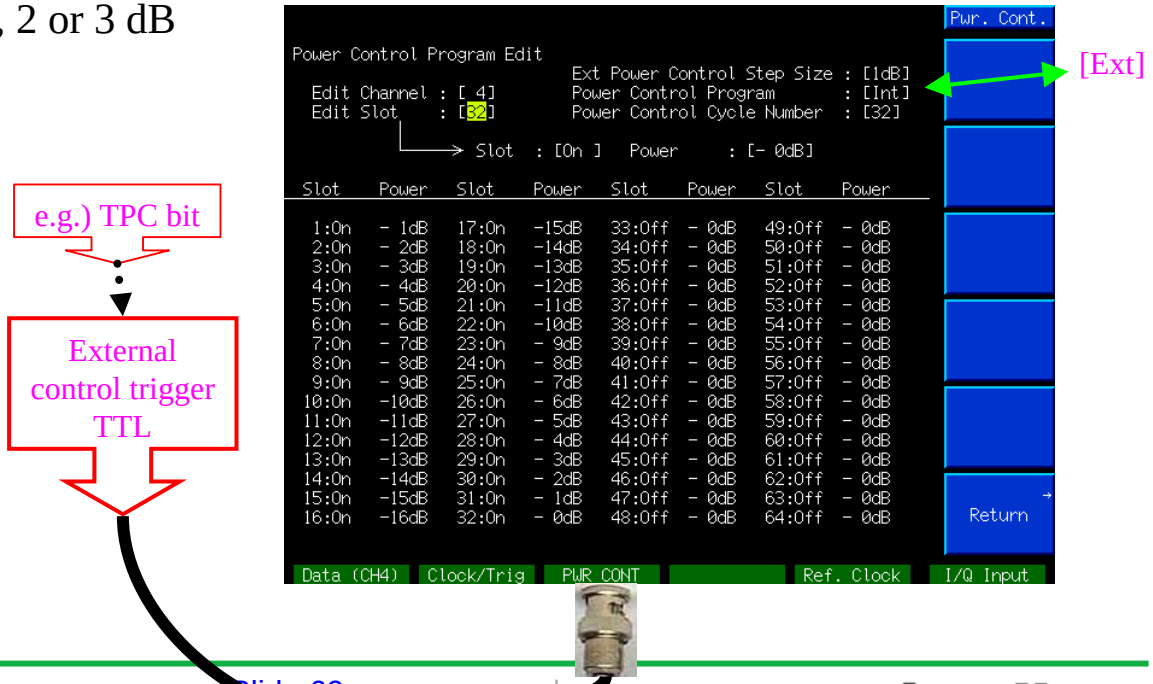


  - BER, BLER
    - Generating the error
    - 0 to 10 %, 0.1 % resolution

Power control function

Operation check of closed loop power control is performable.

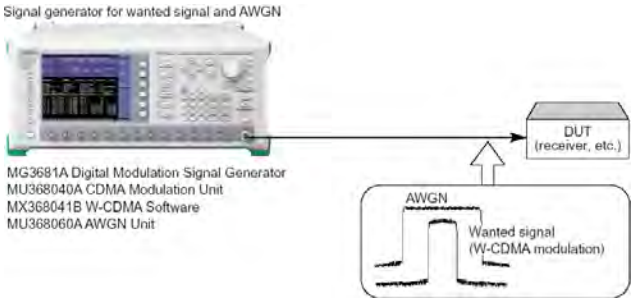
- **The slot power of each channel is programmable up to 64 slot cycle by editing on display.**
  - » Editing the slot power for each channel of CH4~12
    - – -40 to 0 dB (reference: channel power), 1 dB resolution
- **The slot power of each channel is controlled up/down by external control trigger input.**
  - » Controlling the slot power of specified channel among CH4~12
    - – Up & Down in 1, 2 or 3 dB



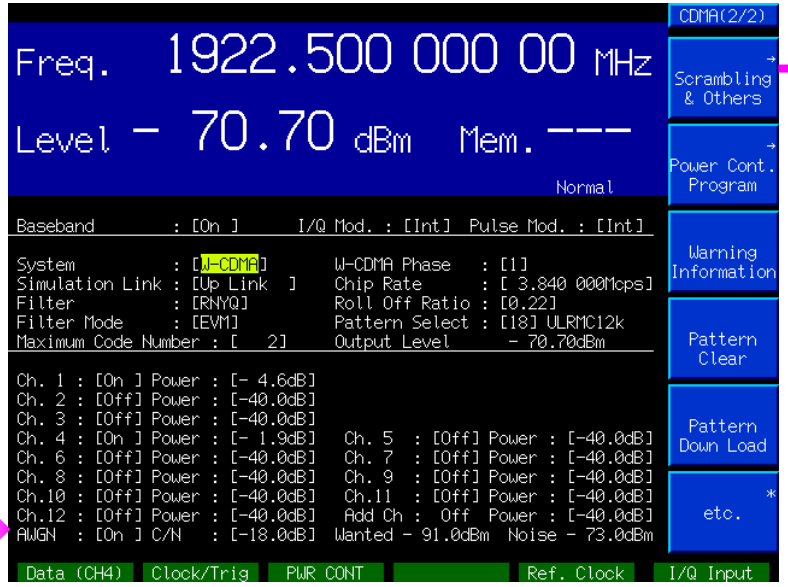
AWGN mixing

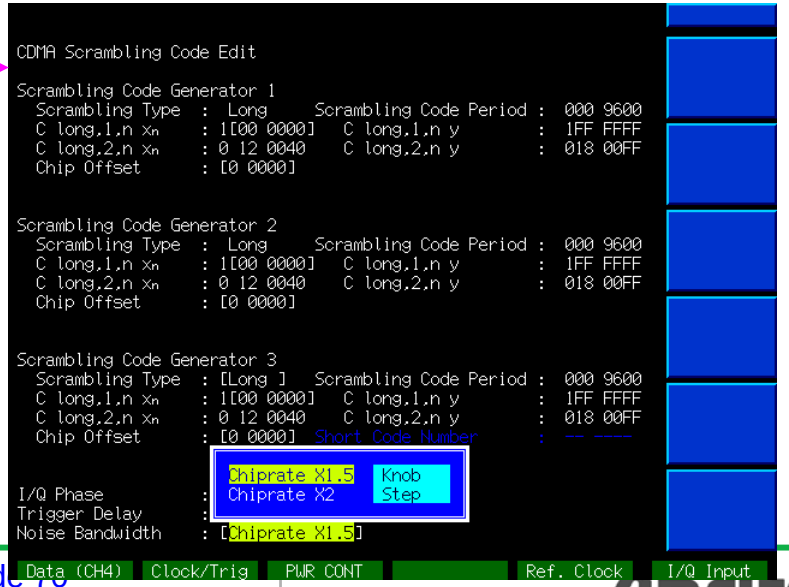
Single unit is performable dynamic range test of BS receiver.

- **Mixing AWGN to Uplink wanted signal**
  - AWGN: Additive White Gaussian Noise
- **High-accuracy and high-stability C/N**
  - » -30 to -20 dB, 0.2 dB resolution
    -19.9 to -8 dB, 0.1 dB resolution



- **Selecting AWGN bandwidth**
  - » 1.5× 3.84MHz(Chip rate) = 5.76 MHz
  - » 2× 3.84MHz(Chip rate) = 7.68 MHz





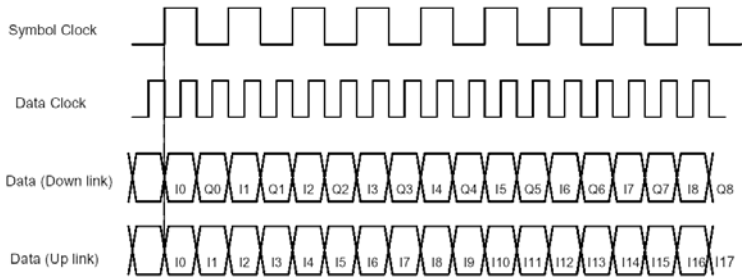
Auxiliary signal Input

- Front panel
  - Data (CH4)
    - Symbol data
  - Clock/Trig
    - Synchronization of external frame clock
    - Frame trigger or start trigger is selectable
      - Used at BS receiver test
  - PWR CONT
    - Refer to “Power Control Function” on previous pages
  - Ref. Clock
    - Synchronization of external baseband reference clock
    - 1×, 2×, 4× chip rate is selectable
      - Used at start trigger
        External reference clock input on rear panel (10/13MHz) is also available

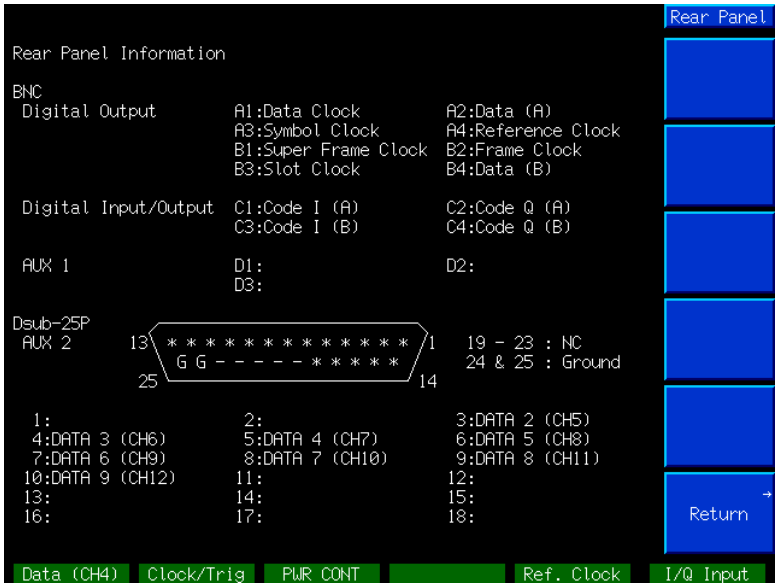
Auxiliary signal Output

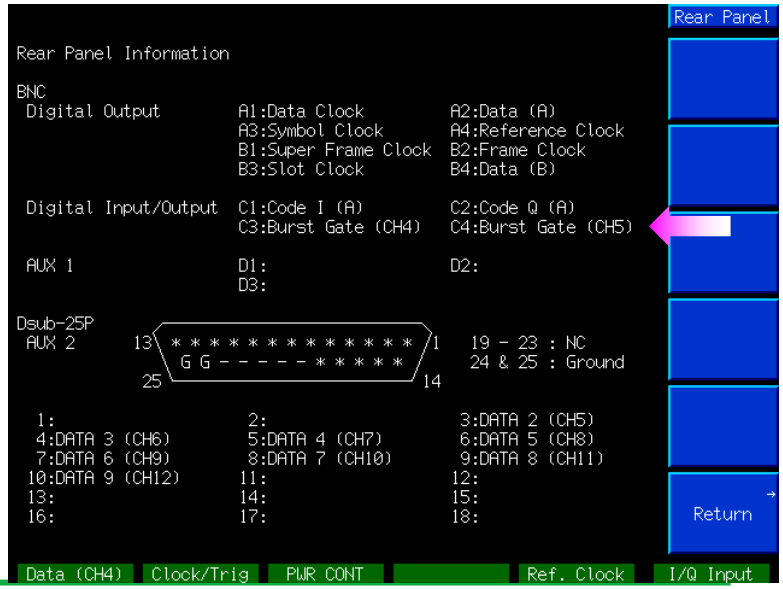
- Rear panel
  - Data (A),(B), Code I/Q (A),(B)
    - Data & code of CH1~12 are selectable
      - Data: The data before spreading(Symbol) or after spreading(Chip) is selectable

      At CH1~3
      - (A) Data & code of P-CCPCH and P-SCH
      - (B) Data & code of P-CCPCH and S-SCH
  - Reference Clock
    - Baseband reference clock
      - 1×, 2×, 4×, 8× chip rate is selectable
  - Symbol Clock, Data Clock



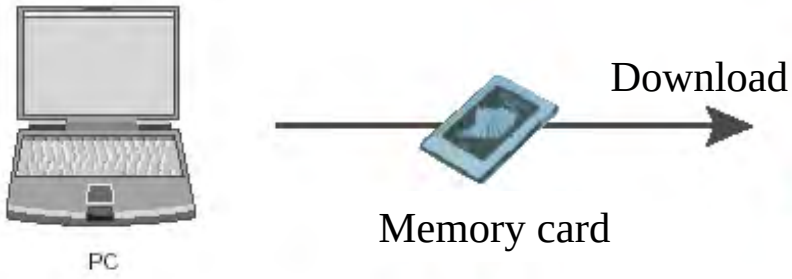
  - At selecting the data & code of channels except CH1~3





MX368141A HSDPA IQproducer™

- MX368141A HSDPA IQproducer™ is the PC application software that generates 3GPP HSDPA compliant signal patterns outputted from MG3681A Digital Modulation Signal Generator.
- MG3681A Digital Modulation Signal Generator that has MU368040A CDMA MODULATION UNIT and MX368041B W-CDMA Software is required for the use of generated signal patterns.
- Since multiple pattern files that are generated can be downloaded into MG3681A mainframe, users can switch over signal patterns easily by selecting them.

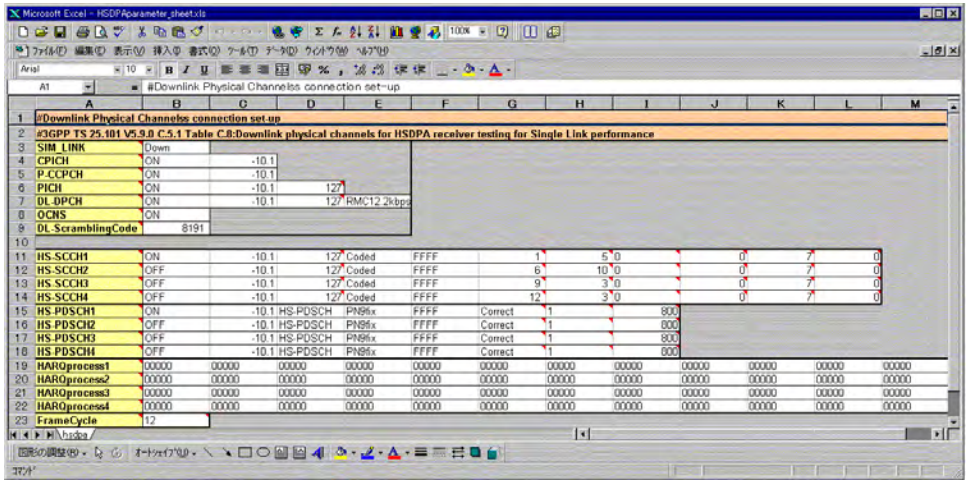


MX368141A
HSDPA IQproducer™

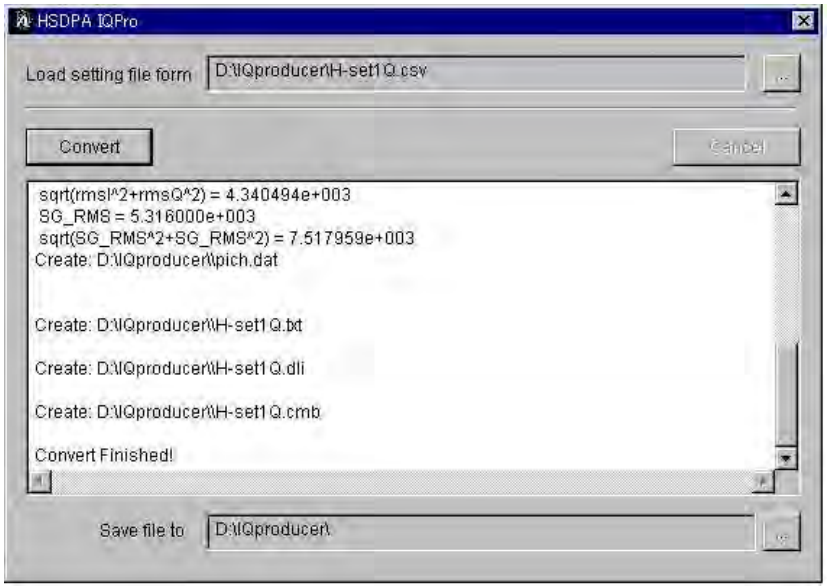
MG3681A
Digital Modulation Signal Generator
+ MU368040A
CDMA Modulation Unit
+ MX368041B
W-CDMA Software

Easy to generate signal patterns with the setting file included

- With the MX368141A HSDPA IQproducer™, users can generate signal patterns by editing a setting file (csv format) that determines HSDPA-system signal patterns with Excel program and converting the edited setting file.
- With the setting file of standard signal patterns (Fixed Reference Channel*) included in the software, users can generate signal patterns easily only by editing the parameter they wish to change.



MX368141A HSDPA IQproducer™
setting file edit screen

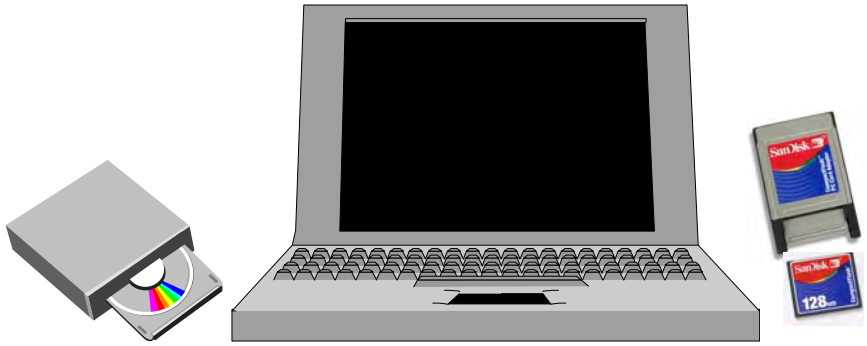


MX368141A HSDPA IQproducer™
setting file convert screen

Operating environment

Personal computer

- **OS: Windows 2000/XP**
- **CPU: Pentium 300MHz or faster**
- **Memory size: ≥128MB**
- **HDD: Occupation≤200MB**
- **Display: 800×600 pixels or more**
- **Peripheral equipment :**
  It be possible to read CD-R.
  It be possible to save in Compact-Flash (PC card adapter is required for download to MG3681A)



Comparison of MX368141A HSDPA IQproducer and MX368041A-11 HSDPA signal pattern

The functional difference about HSDPA

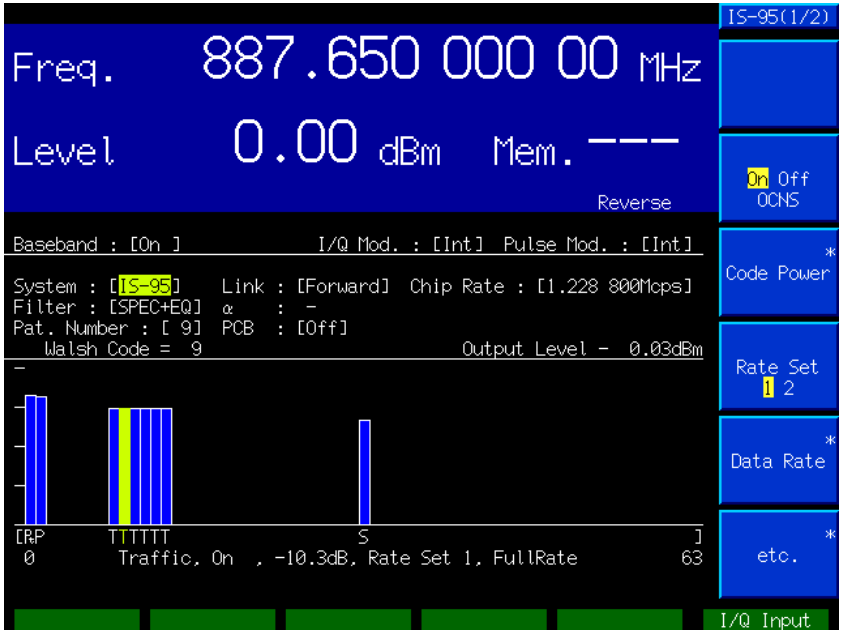
Model **- Baseband** **- Software** **- HSDPA application software**	**MG3681A** **- MU368040A** **- MX368041A/B** **- MX368141A**	**MG3681A** **- MU368040A** **- MX368041A/B** **- MX368041A/B-11**
Type of software	**IQproducer** *** Change of a parameter is possible.**	**Signal pattern** *** Change of a parameter is impossible.**
Component test for Down-Link of HSDPA	**No**	**Yes** **(Supports test model 5)**
Component test for Up-Link of HSDPA	**Yes** **(Supports HS-DPCCH)**	**No**
Supports HSDPA channels	**HS-PDSCH** **HS-SCCH** **HS-DPCCH**	**HS-PDSCH** **HS-SCCH**

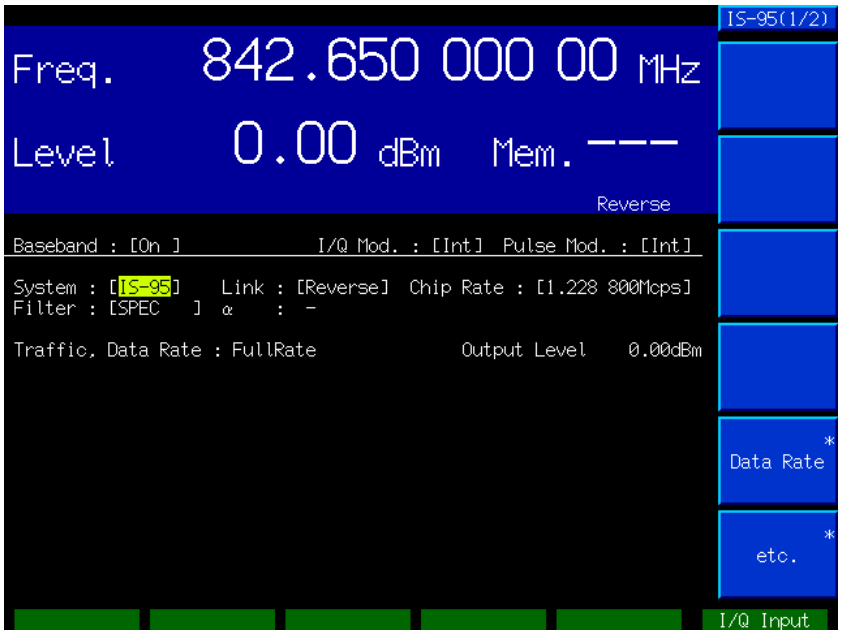
MX368141A can change a parameter and supports HS-DPCCH of HSDPA Uplink.

MX368040A-11 support "Test Model 5" of the component test of HSDPA Downlink.

MX368042A IS-95 Device Test Software

- **Forward/Reverse cdmaOne test signals for IS-95A/B(3GPP2 C.S0002 RC1 & 2) standard can be outputted by installing the MX368042A IS-95 Device Test Software in the MU368040A CDMA Modulation Unit.**
- **In R&D/production process of components, base stations (BS) and mobile stations (MS), the functions to support various applications are provided as the signal source for components and the interfering signal source for receiver test.**





Generation of test signal format

- **Test Mode 1 & 2 signals in IS-97A/B(3GPP2 C.S0010 RC1 & 2) test specifications can be simply set without setting complicated parameters of IS-95A/B(3GPP2 C.S0002 RC1 & 2).**

Caution

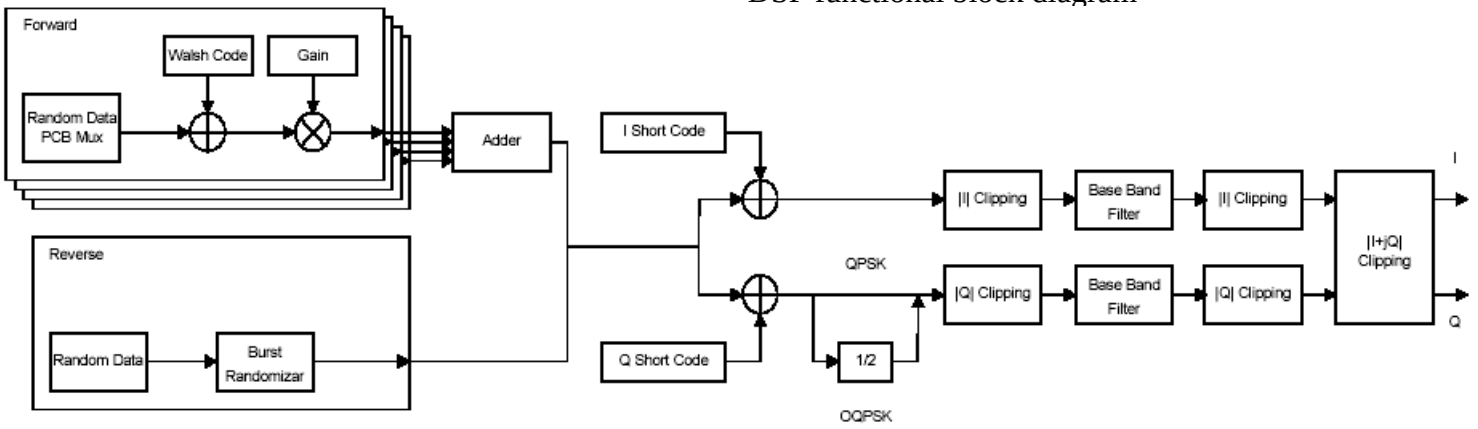
  - » Channel coding is not supported
    (FER Frame Error Rate test is not performable)

Table 6.5.2-1. Base Station Test Model, Nominal for Main Path

Channel Type	Number of Channels	Fraction of Power (linear)	Fraction of Power (dB)	Comments
Forward Pilot	1	0.2000	-7.0	Code channel W_0^{128}
Sync	1	0.0471	-13.3	Code channel W_{32}^{64}; always 1/8 rate
Paging	1	0.1882	-7.3	Code channel W_1^{64}; full rate only
Traffic	6	0.09412	-10.3	Variable code channel assignments; full rate only

- **DSP stores the I/Q mapping data of 98304 chip (4 frames) /4× over sampling in Waveform data Memory according to the parameter set on display.**

DSP functional block diagram



Generation of test signal format

- **Simple editing on display**

Support various test cases

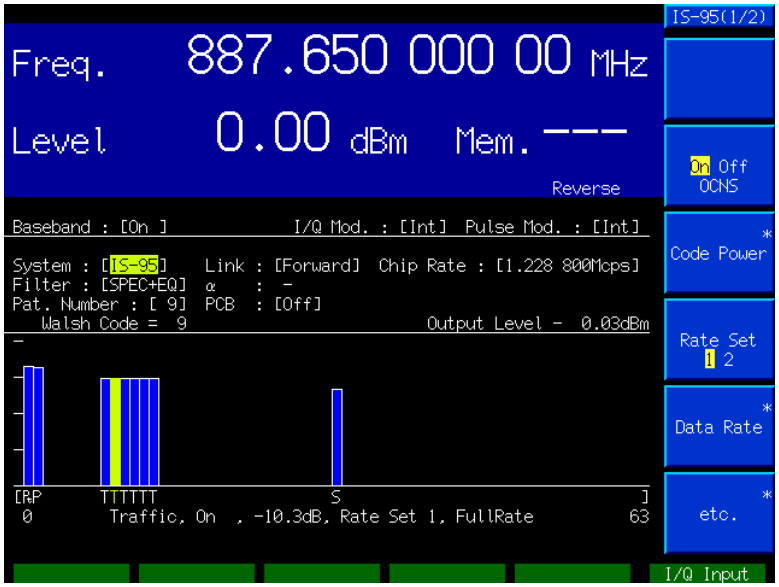
Channel Type	Walsh Code	Function
Pilot	0	Symbol Data is "0".
Sync	32	Symbol Data is Random. Symbol Rate is 4.8 ksps.
Paging	1 to 7	Symbol Data is Random. Symbol Rate is 19.2 ksps.
Traffic	8 to 31, 33 to 63	Symbol Data is Random. Symbol Rate is 19.2 ksps. Settings of Data Rate and Rate Set are enabled. Setting PCB to On allows PCB bit to be inserted.

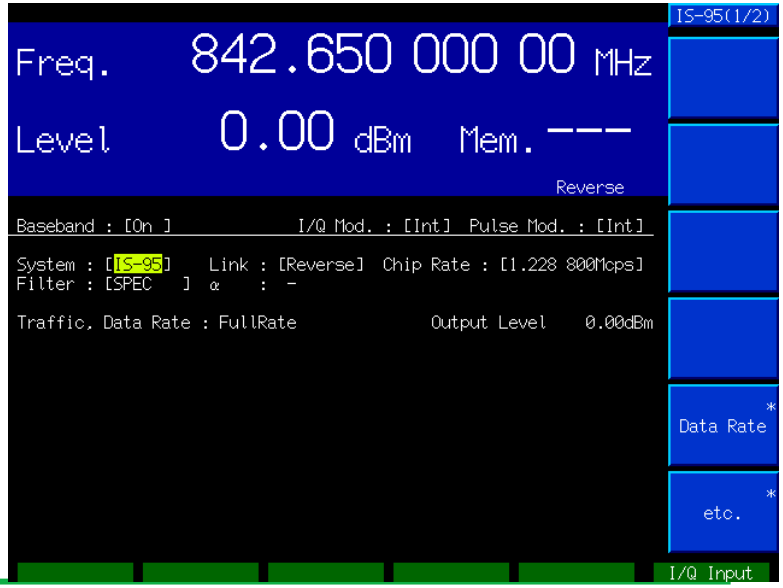
Forward

» Multiple channels
  – 1 to 64
» Per Walsh code (0 to 63)
  – On, Off, OCNS
  – Code Domain Power
    • -40 to 0 dB, 0.1 dB resolution
» Traffic channels
  – Rate set
    • 1 (RC1), 2 (RC2)
  – Data rate
    • Full, Half, Quarter, Eighth
      9.6 , 4.8 , 2.4 , 1.2 kbps (Rate set 1)
      14.4, 7.2 , 3.6 , 1.8 kbps (Rate set 2)

Reverse

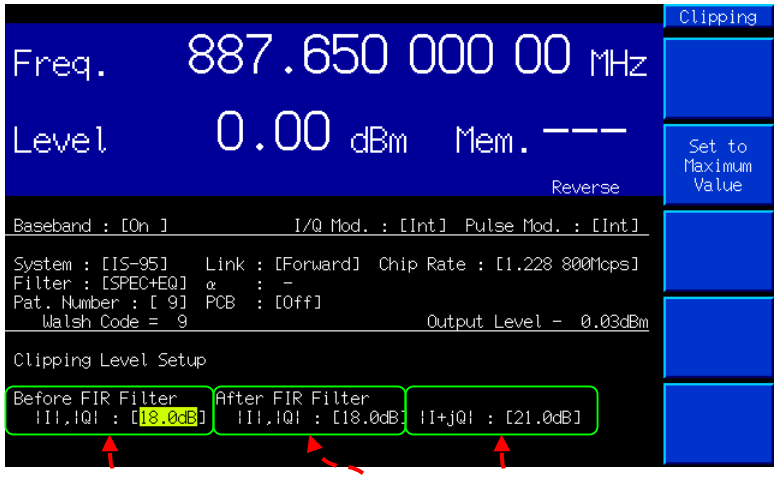
  – Data rate
    • Full, Half, Quarter, Eighth
      9.6 , 4.8 , 2.4 , 1.2 kbps (Rate set 1)

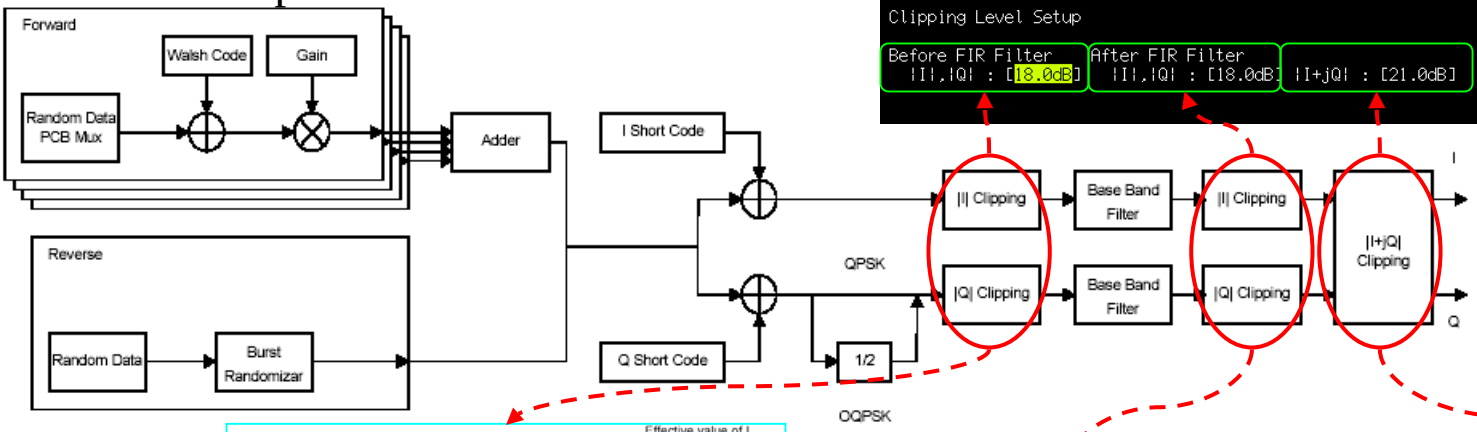


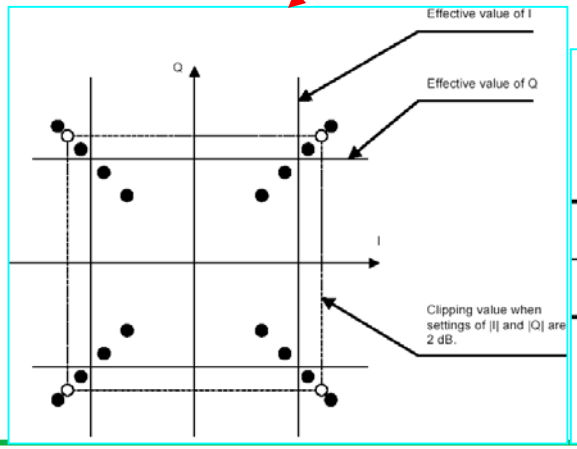


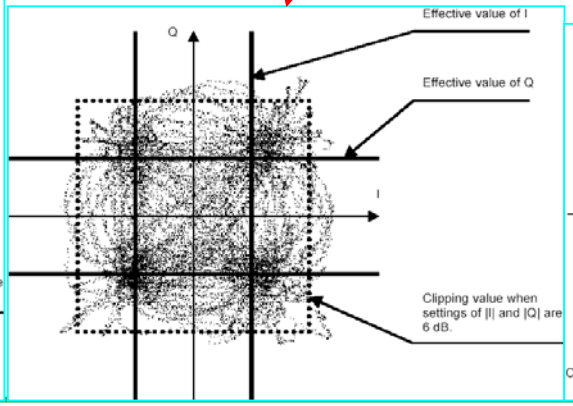
Peak Clipping of test signal

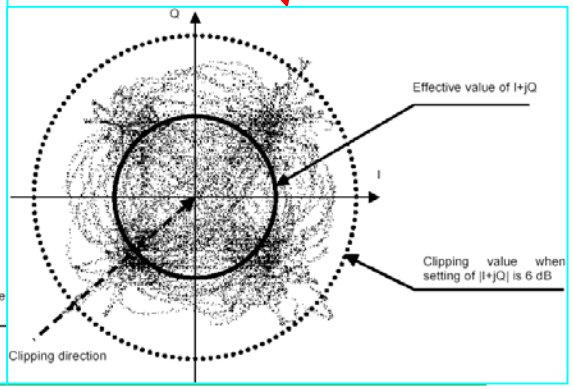
- **Useful for the evaluation of crest factor(CCDF) at components**
  - » Limiting the peak level of I/Q amplitude









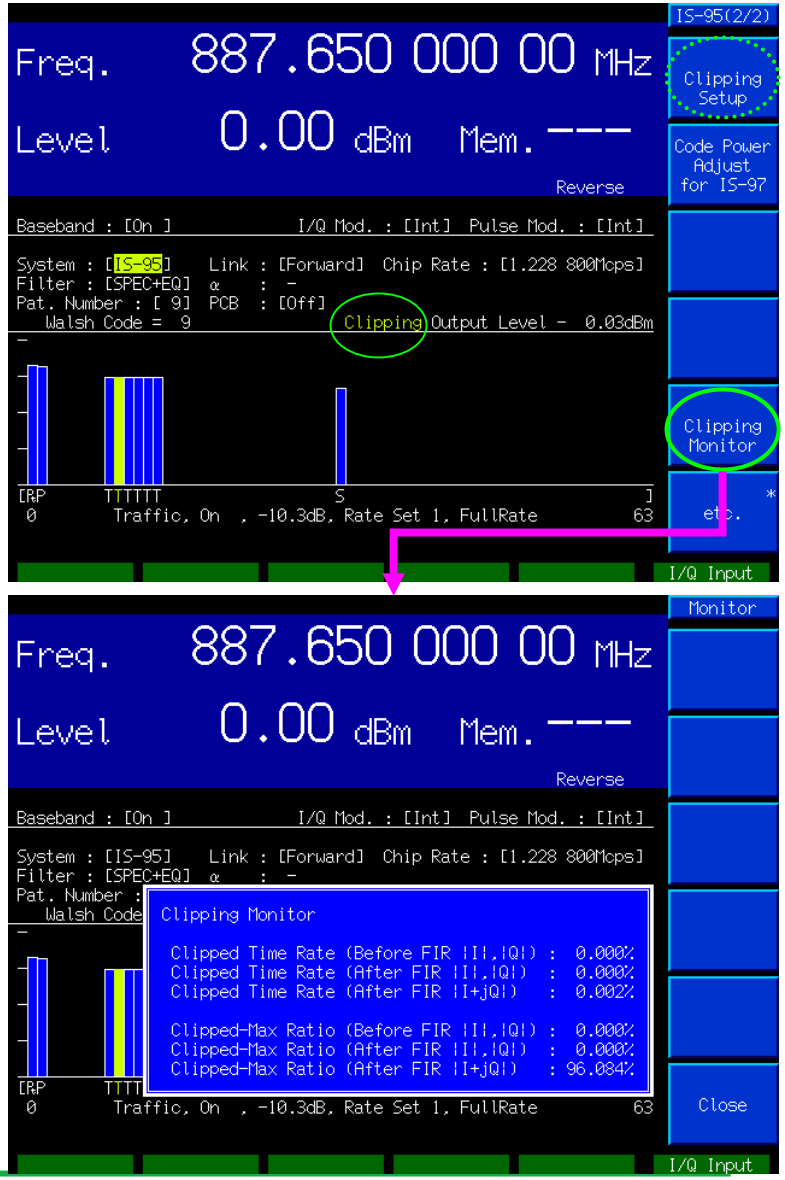


Peak Clipping of test signal

- **Clipping before FIR filtering**
  - » ACLR of output signals is not deteriorated because of no distortion caused by clipping.
    - – Extreme clipping deteriorates waveform quality.
  - » FIR filtering may cause the peak exceeding limited level. Large peak is caused especially at few multiplex number.
- **Clipping after FIR filtering**
  - » Clipping causes distortion and deteriorates the ACLR of output signals.
- **Scalar clipping**
  - » Limiting I or Q amplitude level
- **Vector clipping**
  - » Limiting RMS $\sqrt{(I^2+Q^2)}$ level

Peak Clipping Monitor of test signal

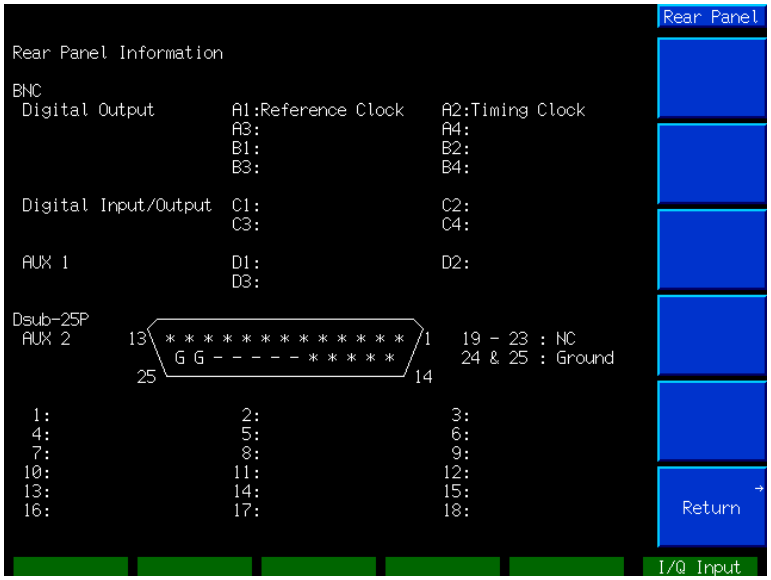
- **“Clipping” is indicated when vector amplitude is attenuated by Clipping**
  - » Selectable “Clipping Monitor”



- **Checking Attenuated time and vector amplitude**
  - » Clipped Time Rate
    - – Percentage of attenuated sampling point
  - » Clipped Max Ratio
    - – Attenuation percentage of max. vector amplitude
      - 100% indicates the vector amplitude without attenuation

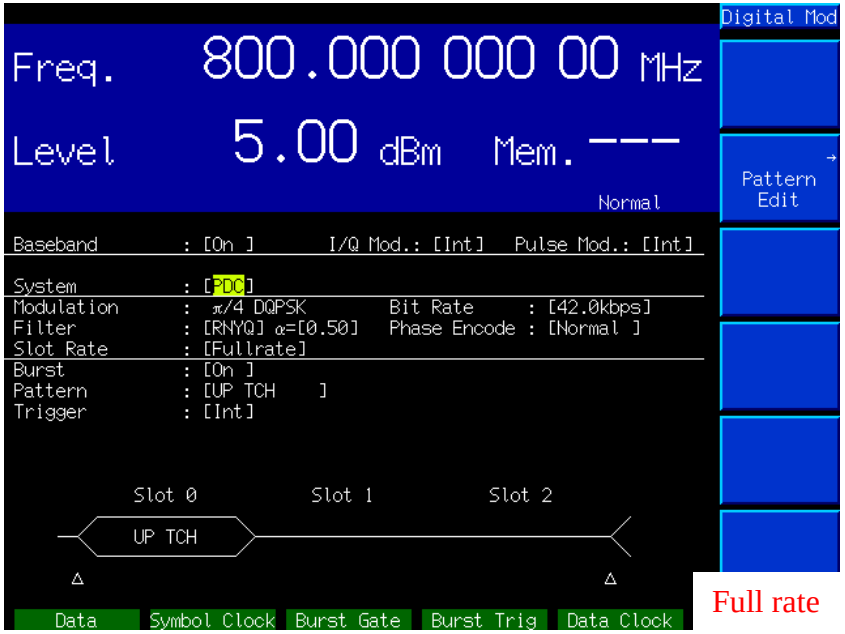
Auxiliary signal Output

- Rear panel
  - Reference Clock
    - Baseband reference clock
      - Chip rate
  - Timing Clock
    - 20ms, 26.7ms, 80ms, 2sec is selectable

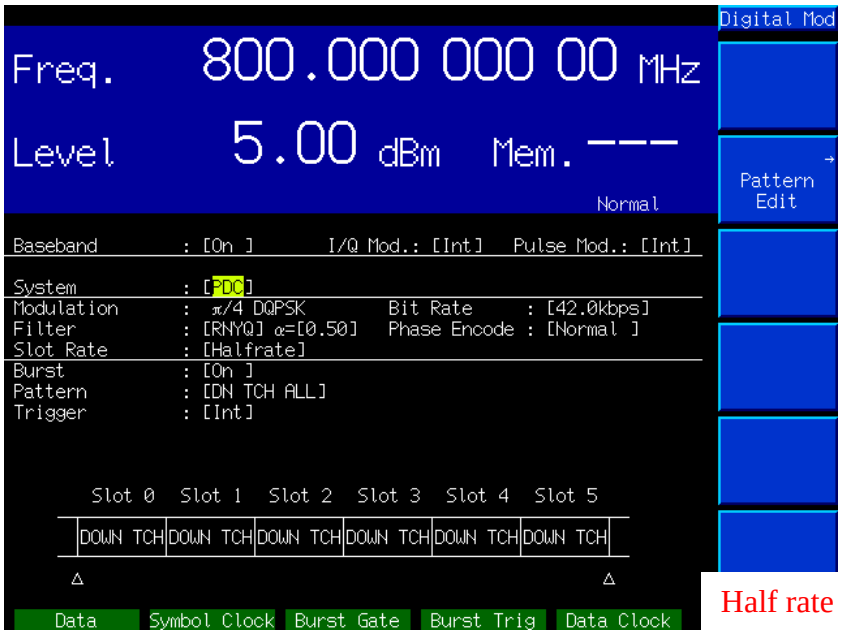


MX368011A PDC Software

- **Downlink/Uplink PDC test signals (TCH, VOX) for RCR STD-27 standard can be outputted by installing the MX368011A PDC Software in the MU368010A TDMA Modulation Unit.**
- **In R&D/production process of components, base stations (BS) and mobile stations (MS), the functions to support various applications are provided as the signal source for components, the wanted signal source and the interfering signal source for receiver test.**



Full rate



Half rate

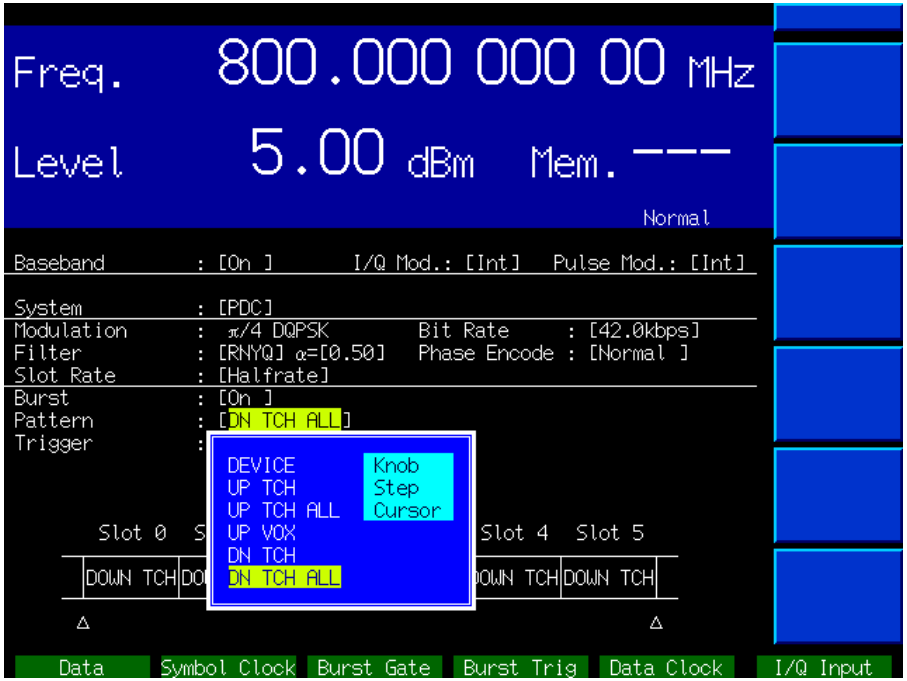
Emulation of MG3670 series

MG3670 series/MG3660A

- **MG0301C π/4DQPSK Modulation Unit**
- **MG0303B Burst Function Unit**

Equal functions

- **Display**
- **Remote control**



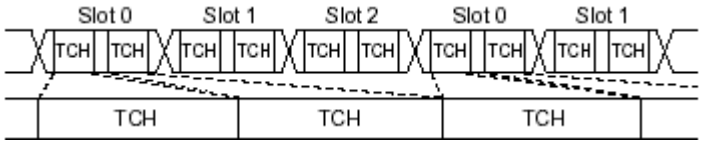
Real-time generation of test signal format

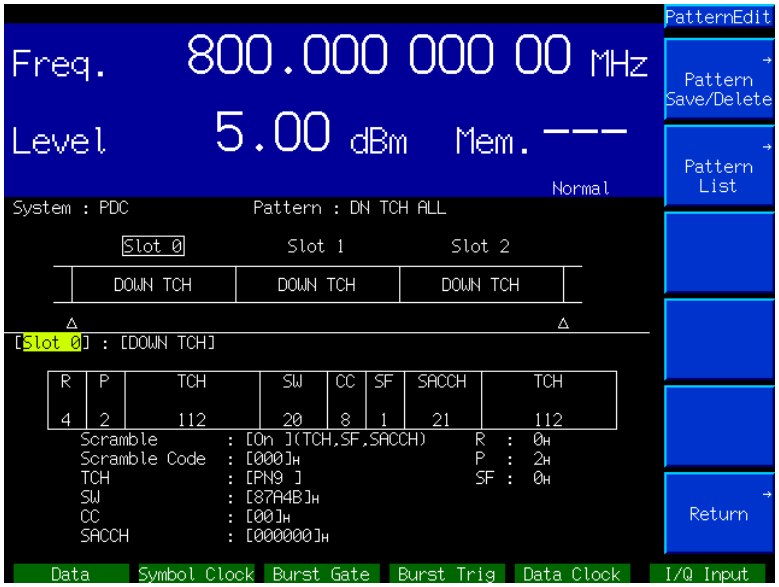
- **Simple editing on display**

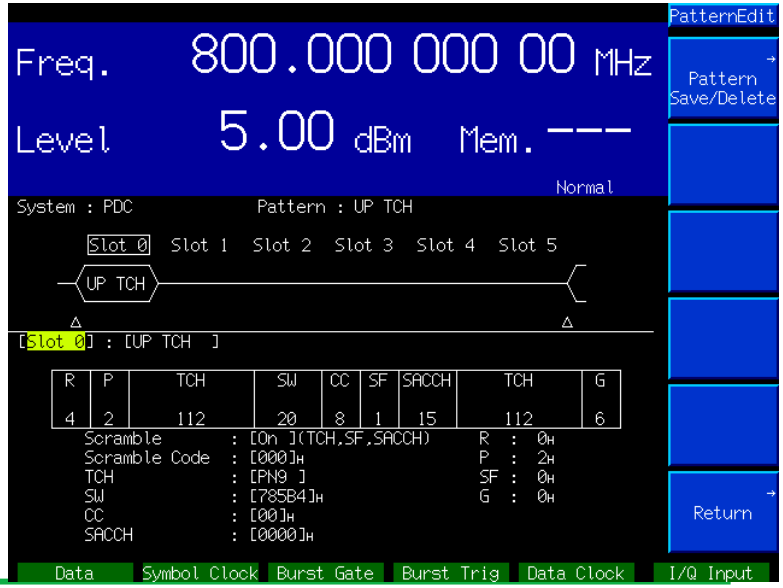
  Support various test cases

  - » Full rate/Half rate
  - » Slot On/Off
  - » Parameter

- **PRBS data of TCH**
  - » Continuous in the same slot
  - » Phase is shifted per slot
    - – When invalid slot is received, PRBS data becomes discontinuous and detectable by BER test

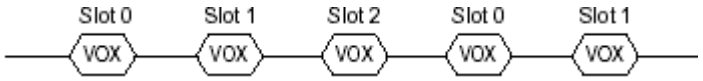




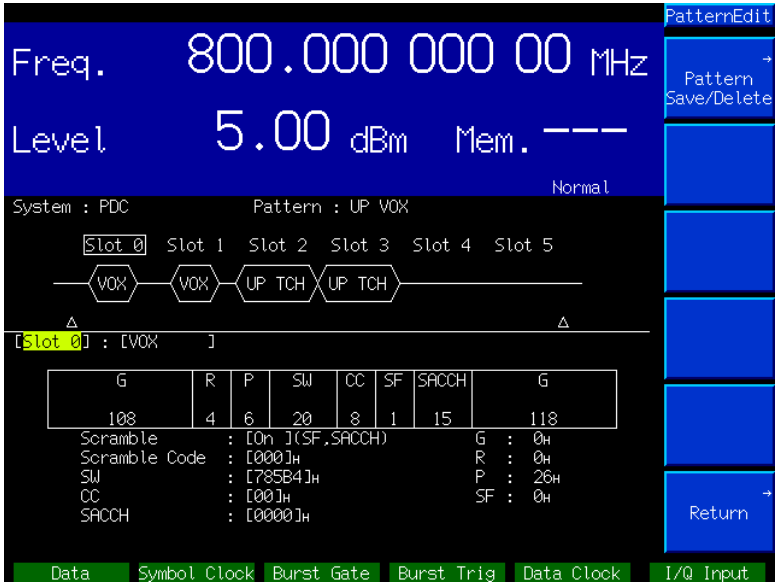


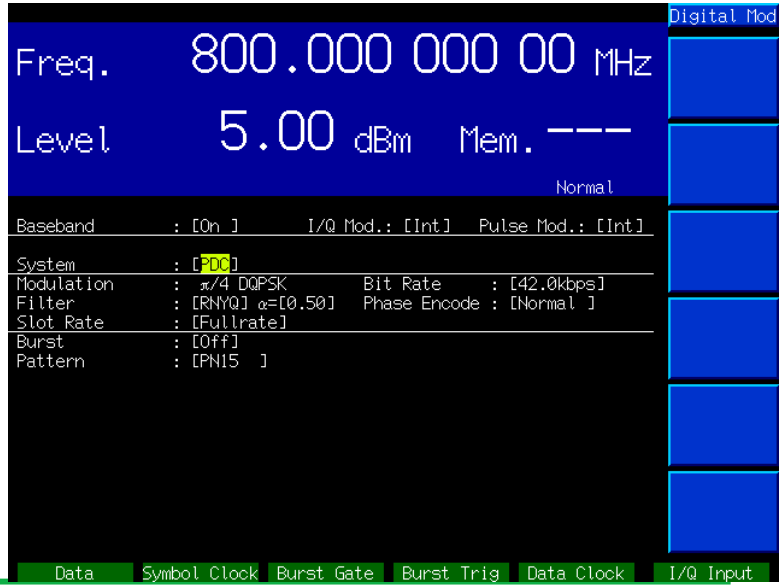
Real-time generation of test signal format

- **VOX(Voice Operated Transmission)**
  - » Controlling to transmit voice signal in voice period and not to transmit voice signal in voiceless period for power saving of MS.



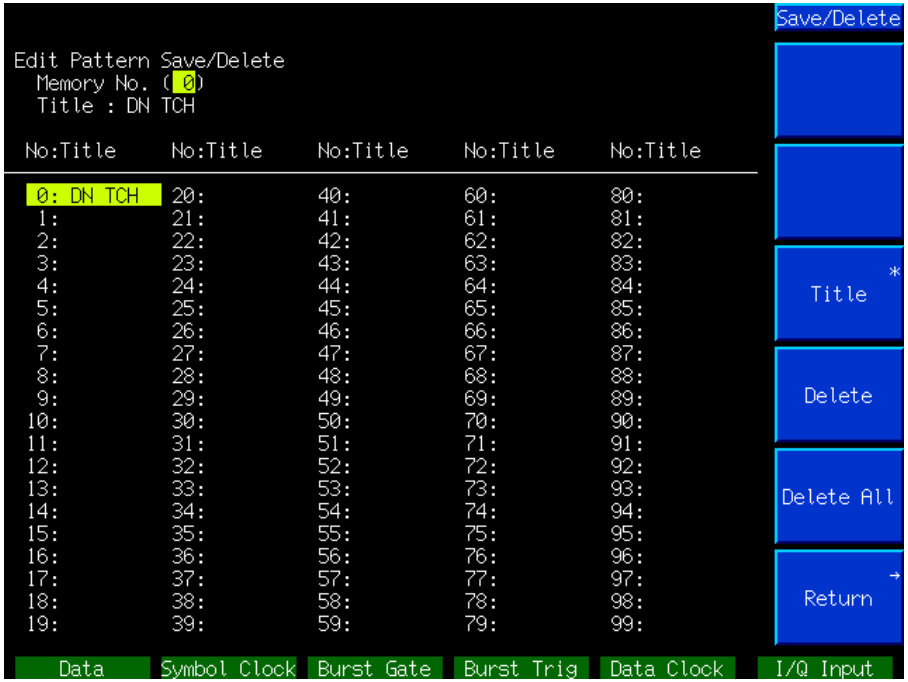
- **Interfering signal for receiver test**

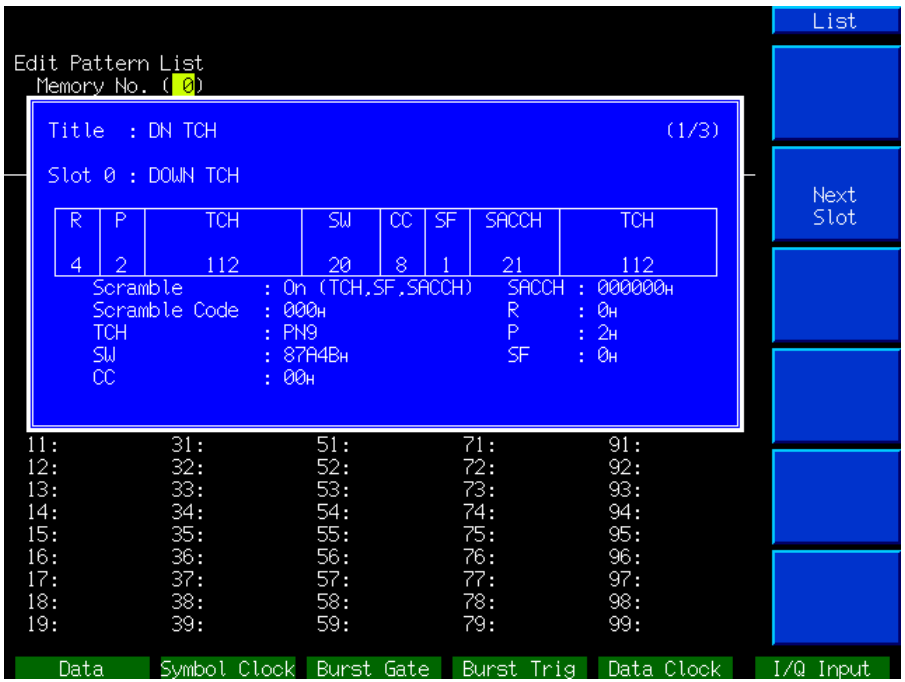




Pattern memory (MU368010A internal memory)

- **Parameter settings up to 100 types on Pattern Edit screen can be saved.**
- **Title up to 8 characters can be inputted for easy confirmation.**
  - » Saved parameter setting window

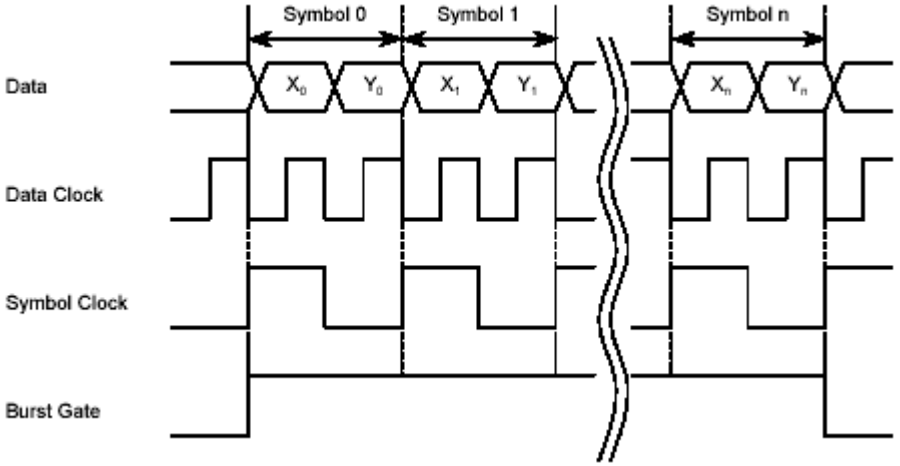




External data input

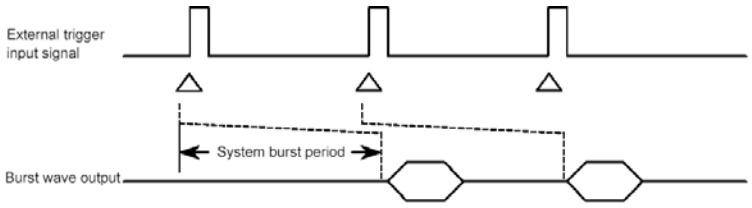
π/4DQPSK modulation signal of arbitrary frame format can be outputted by utilizing the pulse pattern generator.


```
Base Band Setup

        Data                        : [Ext]
        Data Clock                  : [Ext]

    Ext Mod Input
        Data                        : [Positive]
        Data Clock                  : [Rise]
        Symbol Clock                : [Rise]
        Burst Gate                  : [Positive]

    Ext Mod Output
        Data                        : [Positive]
        Data Clock                  : [Rise]
        Symbol Clock                : [Rise]
        Burst Gate                  : [Positive]

        Burst Trigger Input         : [Rise]
        Burst Trigger Output        : [Rise]
        Pattern Sync Output         : [PN Clock]
```



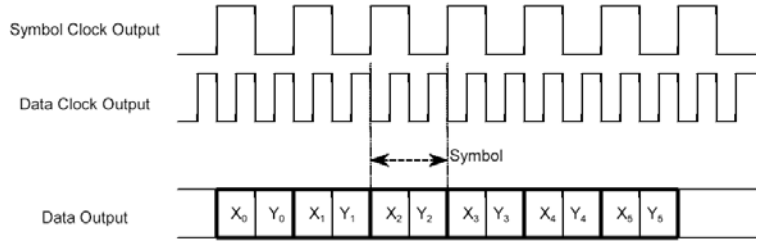
Auxiliary signal Input

- Front panel
  - Data, Symbol Clock, Burst Gate, Data Clock
    - Refer to “External Data Input” on previous pages
  - Burst Trig
    - Synchronization of external burst trigger
      - Used at BS receiver test

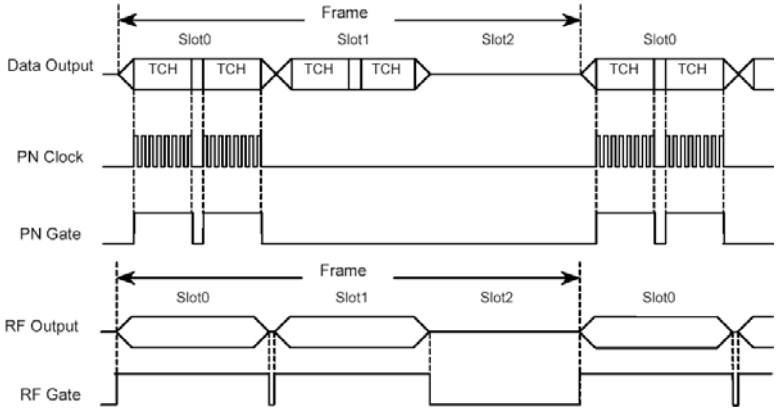


Auxiliary signal Output

- Rear panel
  - Data, Data Clock, Symbol Clock

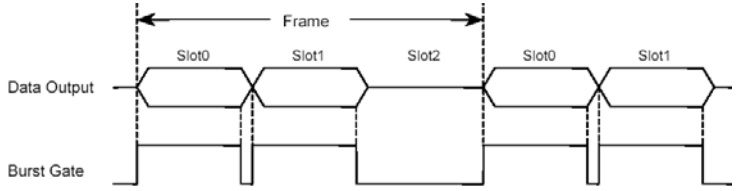


  - Pattern Sync
    - PN Clock, PN Gate, RF Gate is selectable
      - at Burst On

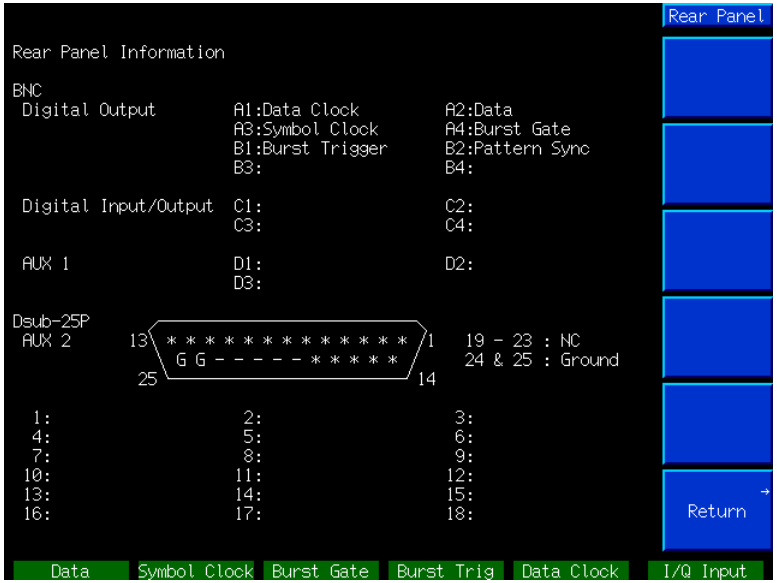


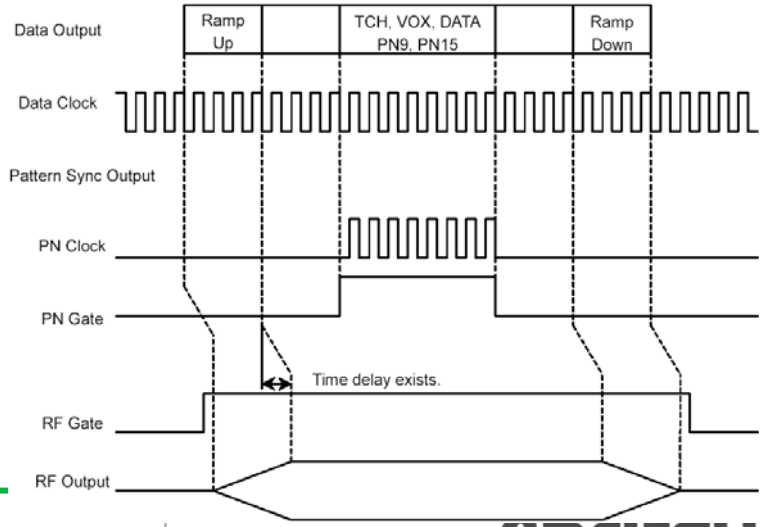
Control signal of internal pulse modulator

  - Burst Gate



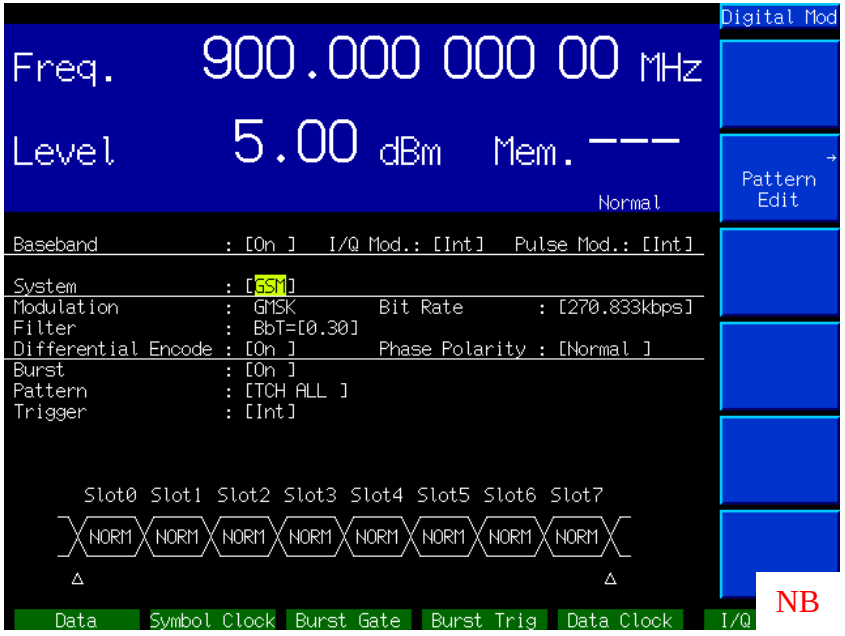
  - Burst Trigger
    - Full/Half rate: 20 / 40 ms clock

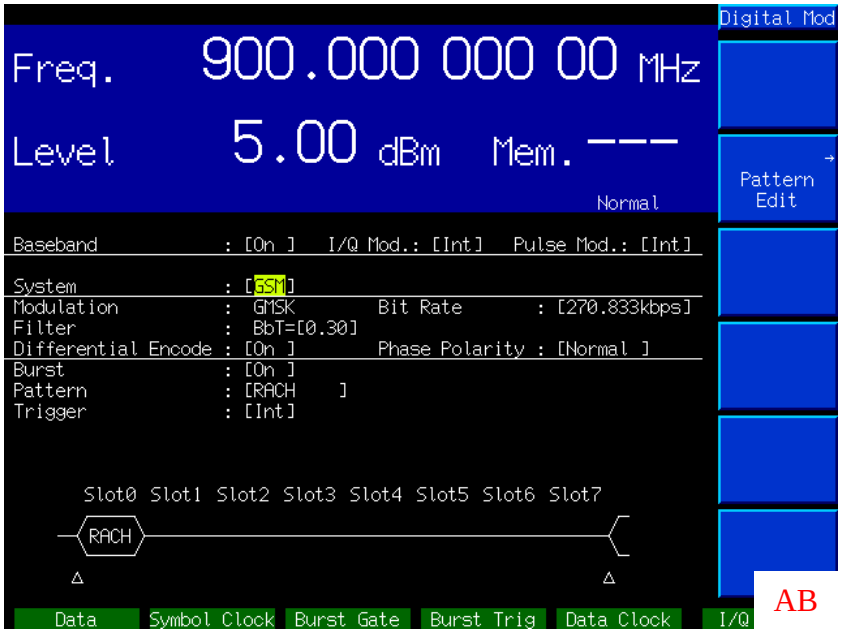




MX368012A GSM Device Test Software

- **Downlink/Uplink GSM test signals (NB Normal Burst, AB Access Burst) for 3GPP TS (GSM) 05.01 standard can be outputted by installing the MX368012A GSM Device Test Software in the MU368010A TDMA Modulation Unit.**
- **In R&D/production process of components, base stations (BS) and mobile stations (MS), the functions to support various applications are provided as the signal source for components and the interfering signal source for receiver test.**





Emulation of MG3670 series

MG3670 series/MG3660A

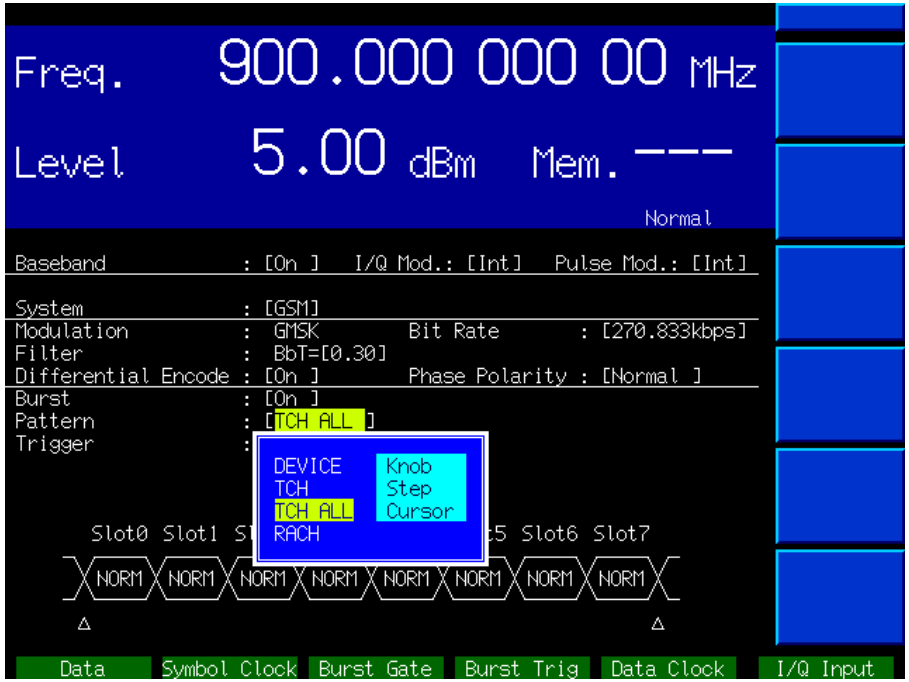
- **MG0302A GMSK Modulation Unit**
- **MG0303B Burst Function Unit**

Equal functions

- **Display**
- **Remote control**

Additional function

- **RACH format**
  - » Access Burst

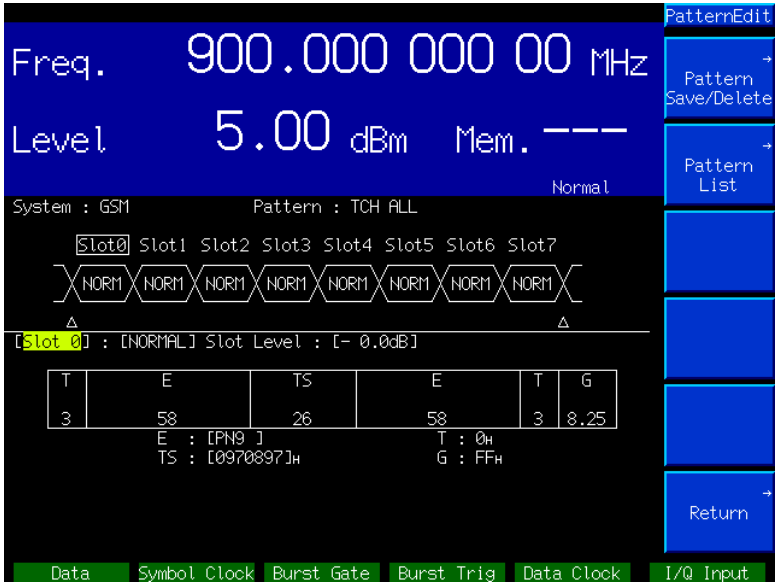


Real-time generation of test signal format

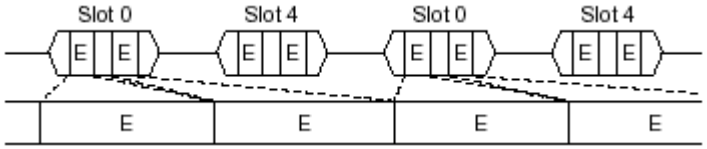
- **Simple editing on display**

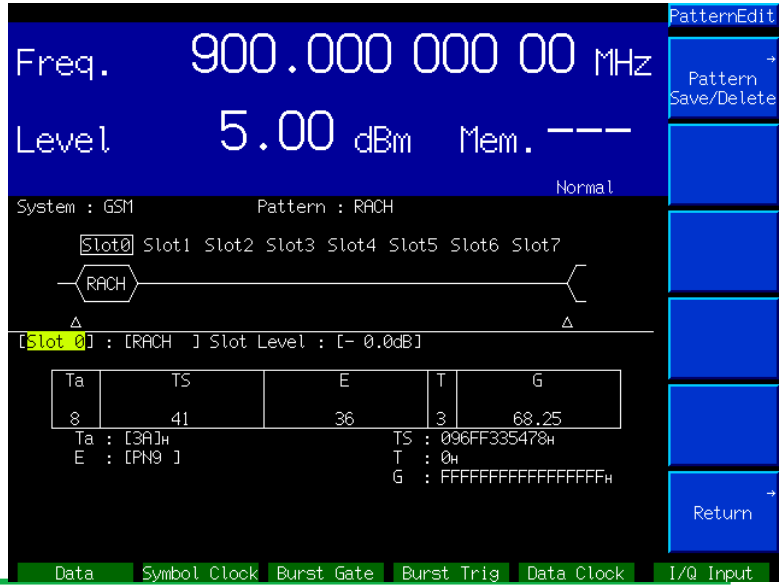
  Support various test cases

  - » Slot On/Off
  - » Slot level
    - – -20 to 0 dB, 0.1 dB resolution
  - » Differential Encode
    - Differential encoding in 3GPP TS (GSM) 05.04
  - » Parameter



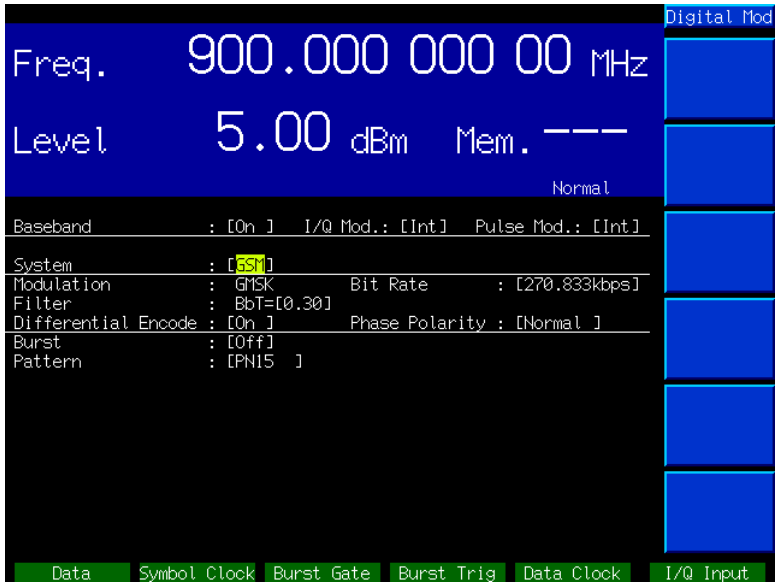
- **PRBS data of E(Encrypted bits)**
  - » Continuous in the same slot
  - » Phase is shifted per slot
    - – When invalid slot is received, PRBS data becomes discontinuous and detectable by BER test





Real-time generation of test signal format

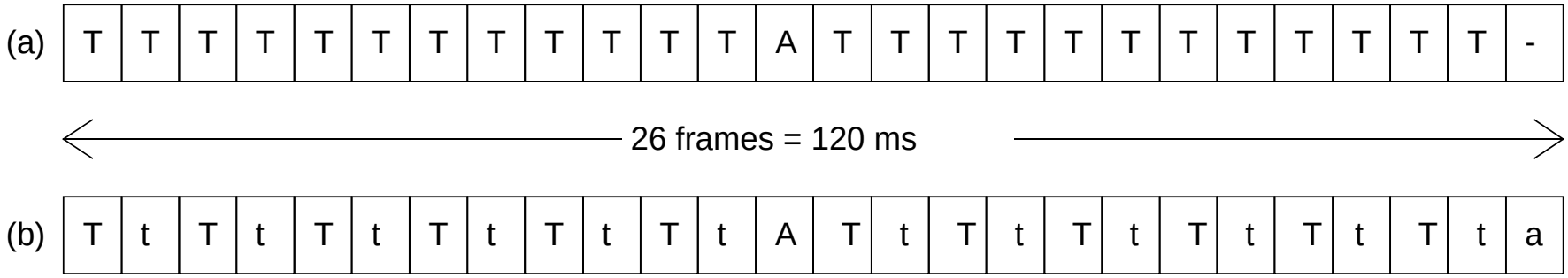
- **Interfering signal for receiver test**



Channel coding of test signal format

Caution

- 3GPP TS (GSM) 05.03 Channel Coding is not supported.
  - Traffic Channels (TCH)
    - TCH/FS (Speech channel at full rate)
    - TCH/EFS (Speech channel at enhanced full rate)
  - Control Channels
    - SACCH (Slow associated control channel)
    - RACH (Random access channel)
  - Packet Switched Channels
    - PDTCH (Packet data traffic channel)
- Multiframe format is not supported.



(a) case of one full rate TCH

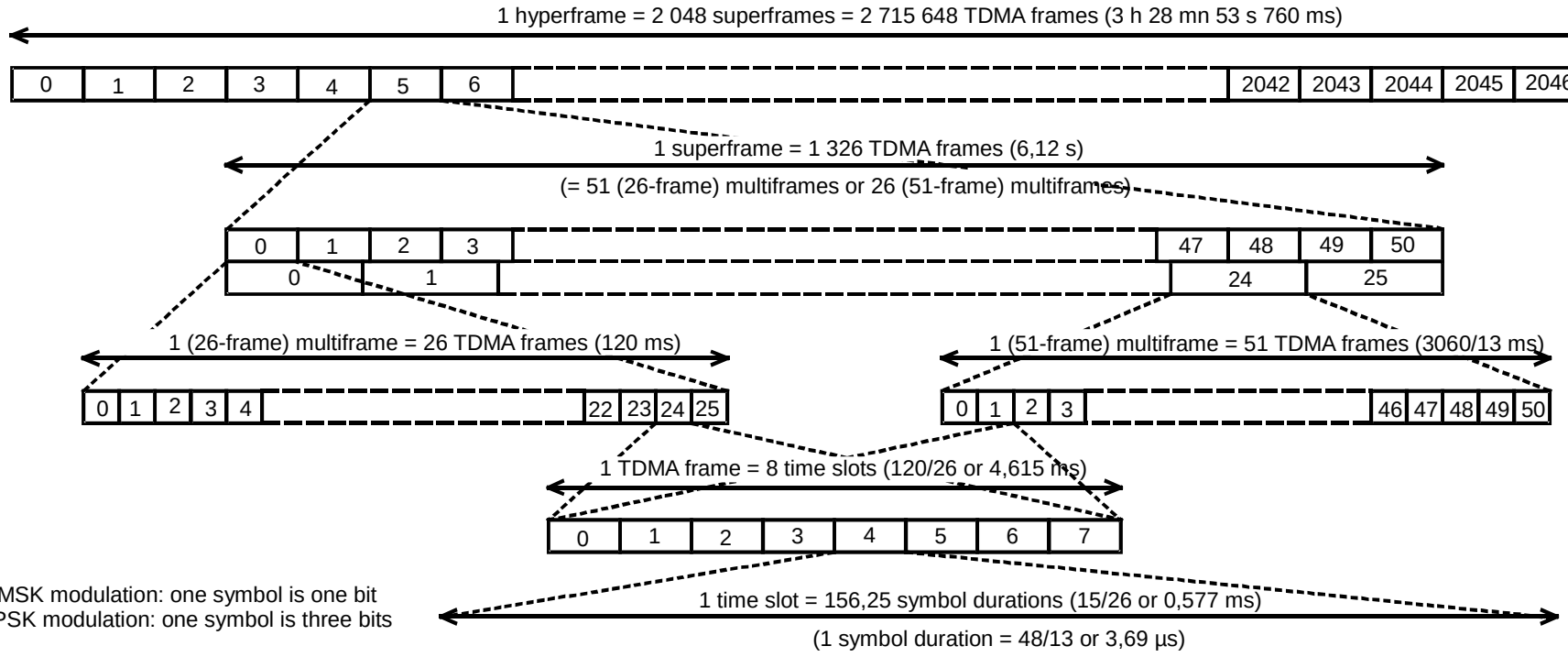
(b) case of two half rate TCHs

T, t: TDMA frame for TCH

-: idle TDMA frame

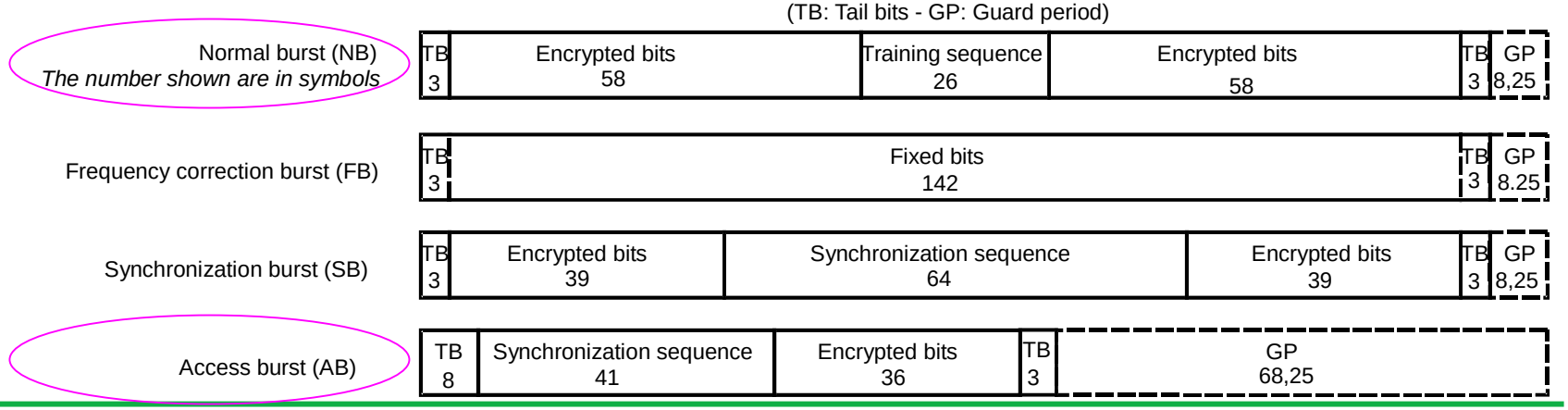
A, a: TDMA frame for SACCH/T

Time slot configuration in 3GPP TS 05.01



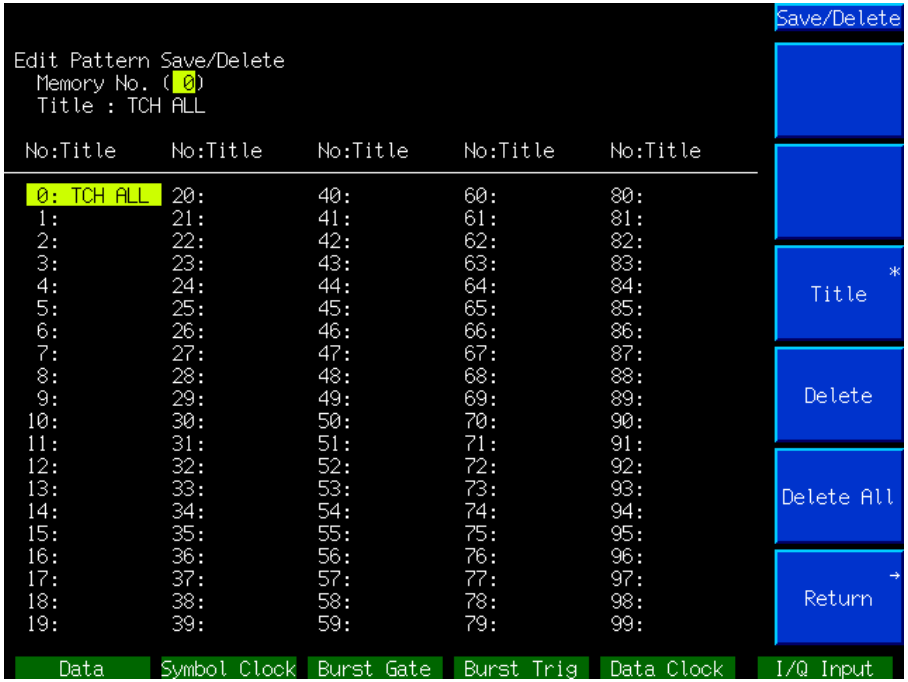
NOTE: GMSK modulation: one symbol is one bit
8PSK modulation: one symbol is three bits

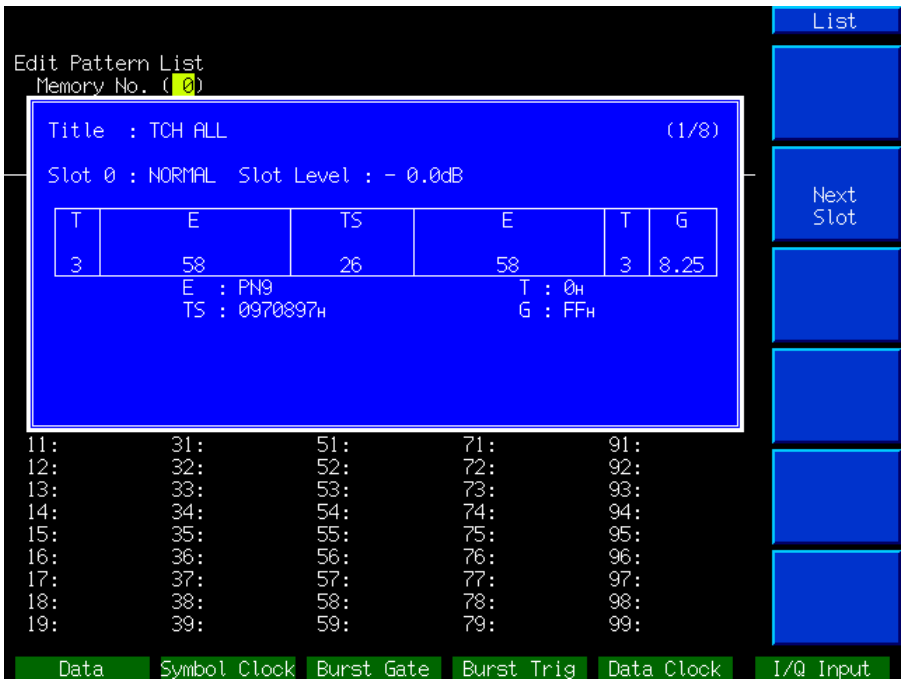
(TB: Tail bits - GP: Guard period)



Pattern memory (MU368010A internal memory)

- **Parameter settings up to 100 types on Pattern Edit screen can be saved.**
- **Title up to 8 characters can be inputted for easy confirmation.**
  - » Saved parameter setting window

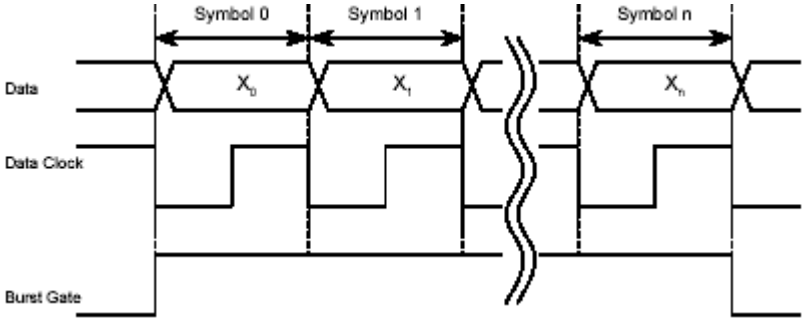




External data input

GMSK modulation signal of arbitrary frame format can be outputted by utilizing the pulse pattern generator.


```
Base Band Setup

        Data                        : [Ext]
        Data Clock                  : [Ext]

    Ext Mod Input
        Data                        : [Positive]
        Data Clock                  : [Rise]
        Symbol Clock                : [Rise]
        Burst Gate                  : [Positive]

    Ext Mod Output
        Data                        : [Positive]
        Data Clock                  : [Rise]
        Symbol Clock                : [Rise]
        Burst Gate                  : [Positive]

        Burst Trigger Input         : [Rise]
        Burst Trigger Output        : [Rise]
        Pattern Sync Output         : [PN Clock]
```

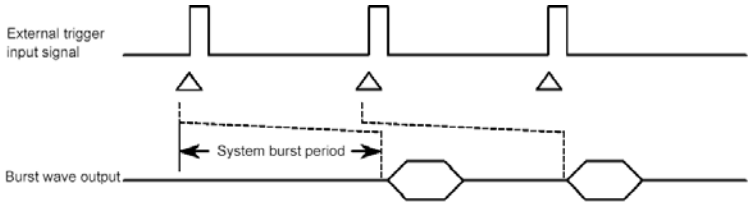


Data Burst Gate Data Clock

Pulse Pattern Generator

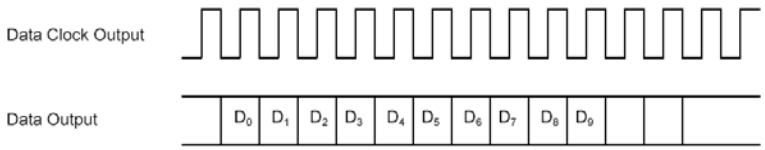
Auxiliary signal Input

- Front panel
  - Data, Burst Gate, Data Clock
    - Refer to “External Data Input” on previous pages
  - Symbol Clock
    - Same as Data Clock
  - Burst Trig
    - Synchronization of external burst trigger
      - Used at BS receiver test

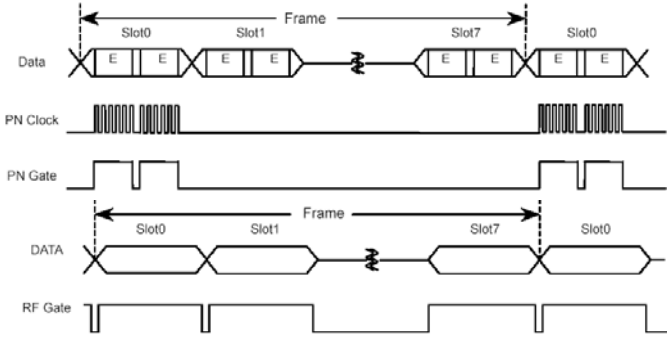


Auxiliary signal Output

- Rear panel
  - Data, Data Clock
    - Symbol Clock is the same as Data Clock

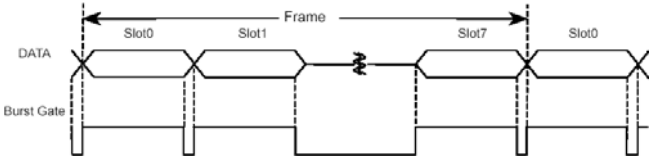


  - Pattern Sync
    - PN Clock, PN Gate, RF Gate is selectable
      - at Burst On

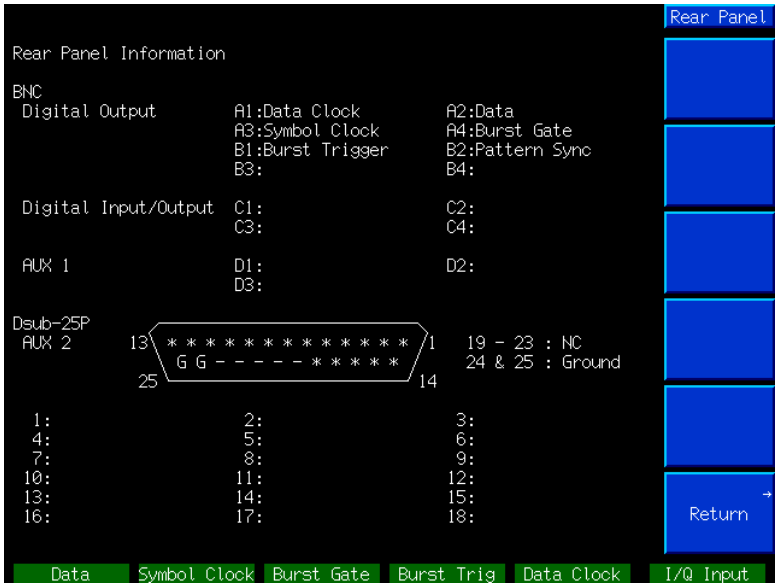


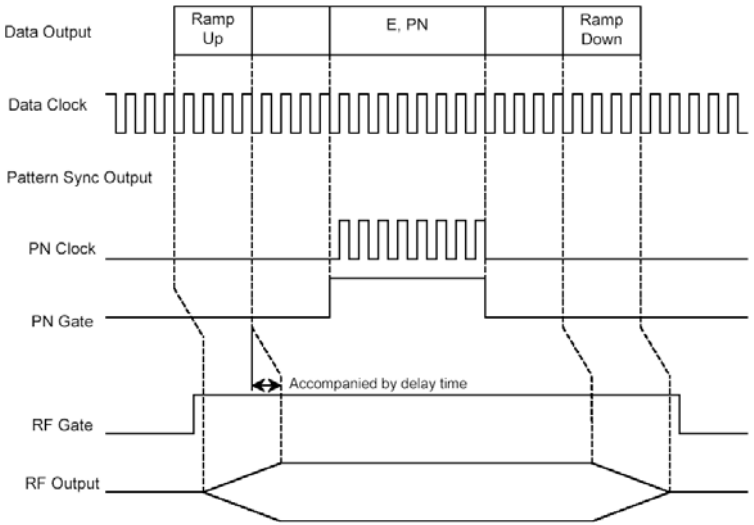
Control signal of internal pulse modulator

  - Burst Gate



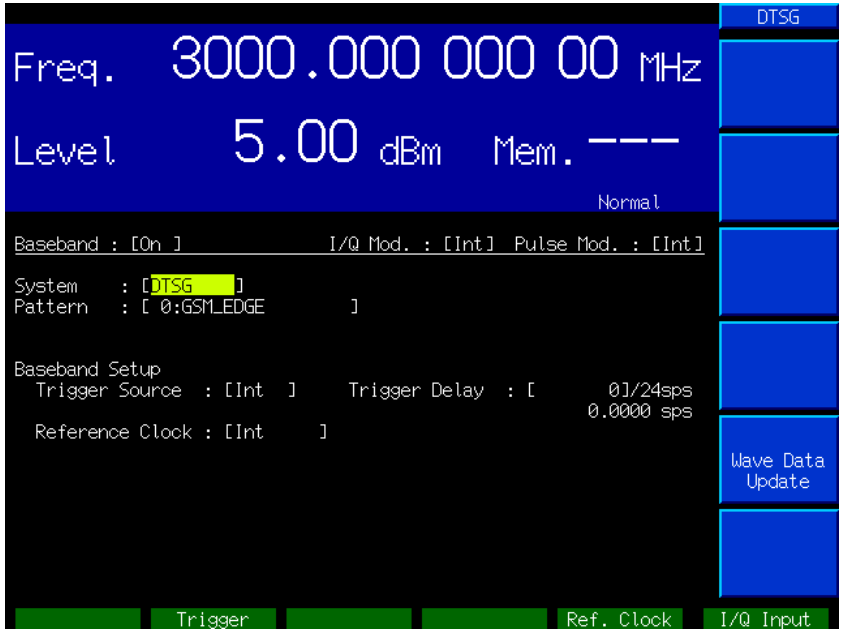
  - Burst Trigger
    - 4.615 ms clock

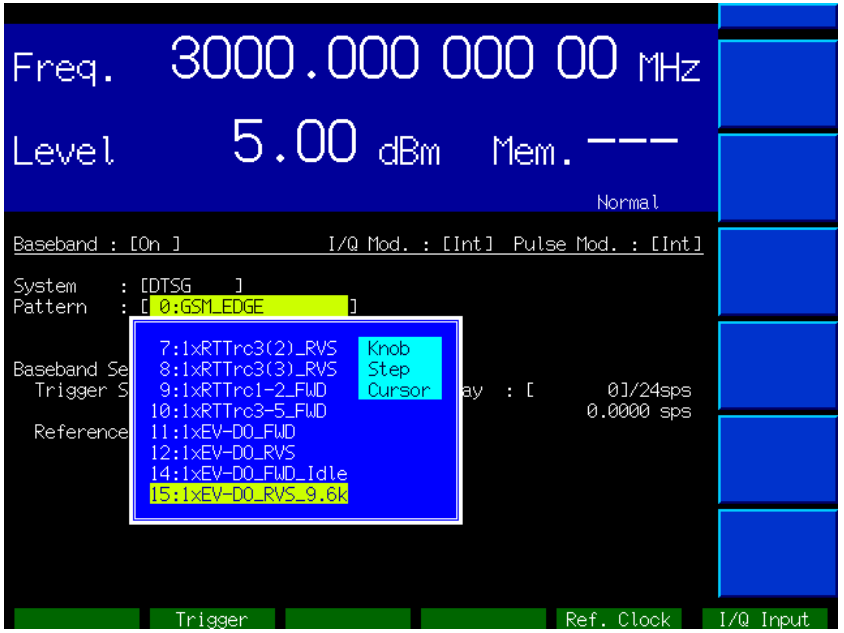




MX368031A Device Test Signal Generation Software

- **The test signals for worldwide main communications systems can be outputted by installing the MX368031A Device Test Signal Generation Software in the MU368030A Universal Modulation Unit.**
- **In production process of components, the function is provided as the signal source for components.**
- **In production process of CDMA2000 1X BS, the function is provided as the wanted signal source for receiver test.**
- **In R&D/production process of CDMA2000 1X MS, CDMA2000 1xEV-DO AN Access Network and AT Access Terminal, the function is provided as the interfering signal source for receiver test.**





Support of test signal format

- **Just to select the signal patterns saved in large-capacity waveform memory without setting complicated parameters of communication systems!** **Simple operation**
- **High-speed change among TDMA 5 signal patterns and CDMA2000 10 signal patterns < 1 sec**
  - » TDMA: GSM/EDGE (2), PDC, IS-136, PHS
  - » CDMA2000: CDMA2000 1X (5), 1xEV-DO (4)
- **Quick support is provided by updating the signal pattern files saved from PC memory card to internal memory.**
  - IQ signal pattern file is downloaded to MG3681A via PC memory card (CompactFlash).
    - The I/Q mapping data of over sampling is stored in Waveform data Memory.

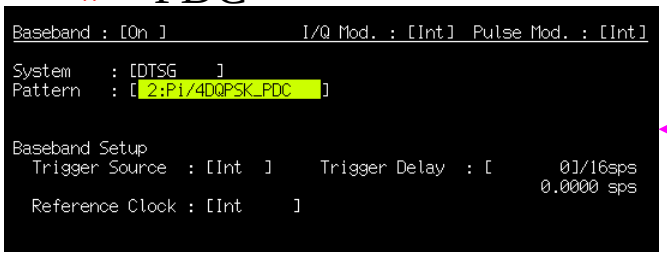
Signal patterns

• **TDMA**		**Modulation**	**Modulation data, Parameter**
Frame coding -not supported			
»	GSM/EDGE:	8PSK	PN9 cont. modulation, Linearized Gaussian, 270.833ksps
		GMSK	PN9 cont. modulation, Gaussian (Bbt: 0.3), 270.833ksps
»	PDC:	π/4DQPSK	PN9 cont. modulation, Root Nyquist (α: 0.5), 21ksps
»	NADC(IS-136):	π/4DQPSK	PN9 cont. modulation, Root Nyquist (α: 0.35), 24.3ksps
»	PHS:	π/4DQPSK	PN9 cont. modulation, Root Nyquist (α: 0.5), 192ksps
• **CDMA2000 1X**			
»	Reverse:	Channel coding -supported (Utilizable for FER test of BS)	
–	RC1:	BPSK→OQPSK	Traffic(TCH)
–	RC3 (1):	BPSK→HPSK	Fundamental(FCH) + Pilot(PICH)
–	RC3 (2):	BPSK→HPSK	Fundamental(FCH) + Supplemental(SCH) + Pilot(PICH)
–	RC3 (3):	BPSK→HPSK	Dedicated Control(DCCH) + Pilot(PICH)
»	Forward:	Channel coding -not supported	
–	RC1-2:	BPSK→QPSK	Pilot(PICH) + SYNC + Paging(PCH) + Traffic(TCH)x6
–	RC3-5:	BPSK/QPSK→QPSK	Pilot(PICH) + SYNC + Paging(PCH) + Traffic(TCH)x6
• **CDMA2000 1xEV-DO**			
Channel coding -not supported			
»	Forward:		
–	Active Slot:	BPSK/16QAM→QPSK	Pilot(PICH) + MAC + Data
–	Idle Slot:	BPSK→QPSK	Pilot(PICH) + MAC
»	Reverse:	BPSK→HPSK	Pilot(PICH) + DRC + ACK + Data
–	9.6 kbps:	DRCChannelGain 3 dB, ACKChannelGain 3 dB, DataChannelGain 3.75 dB	
–	153.6 kbps:	DRCChannelGain 3 dB, ACKChannelGain 3 dB, DataChannelGain 18.5 dB	

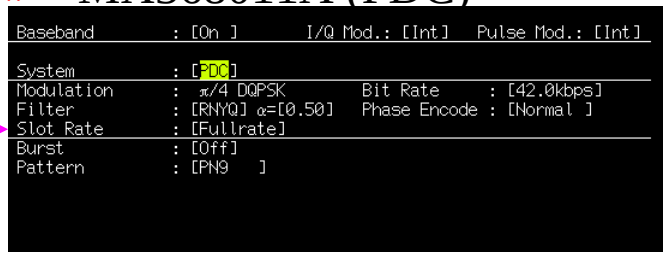
PDC, GSM, PHS Identical signal patterns

MX368031A

» PDC

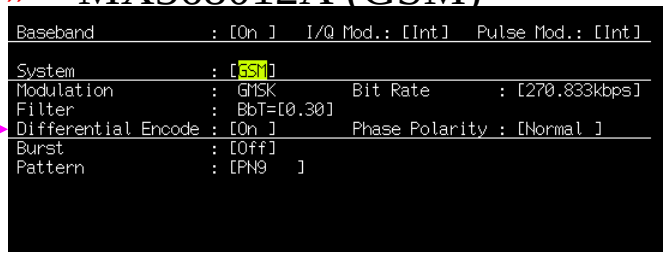


» MX368011A (PDC)

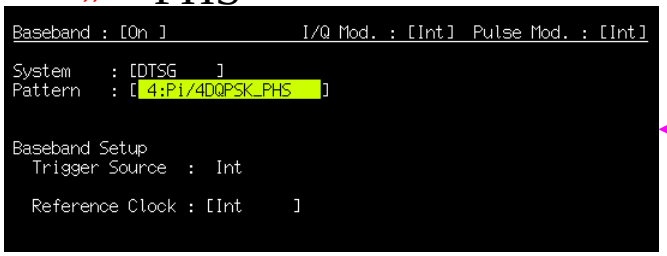


» GSM

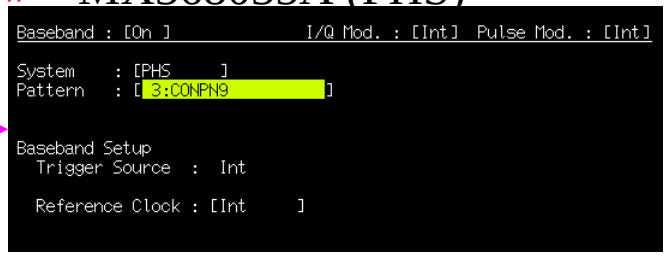
» MX368012A (GSM)



» PHS



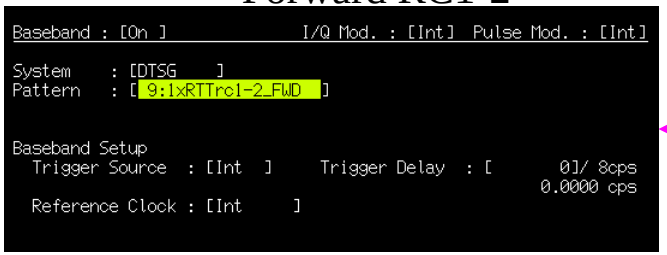
» MX368035A (PHS)



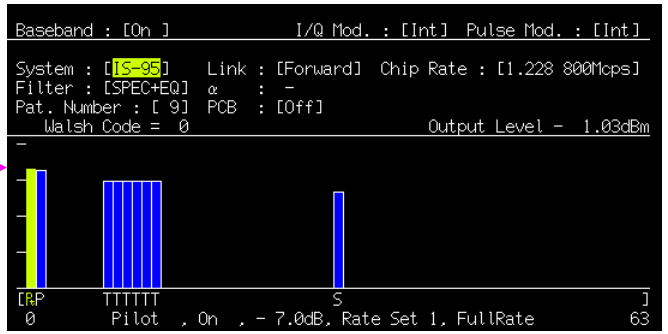
CDMA2000 1X Identical signal patterns

MX368031A

- » CDMA2000 1X
  - – Forward RC1-2



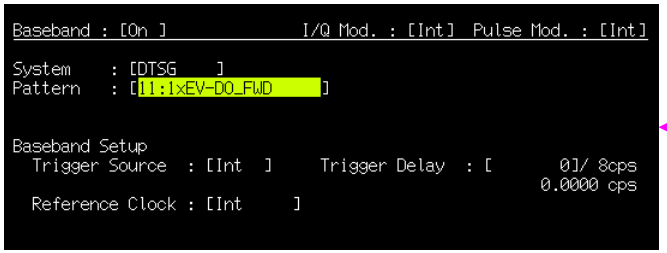
- » MX368042A (IS-95)



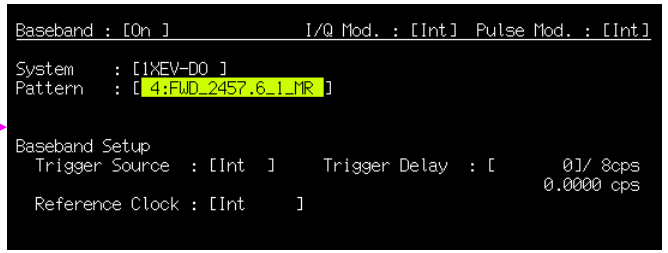
CDMA2000 1xEV-DO Identical signal patterns

MX368031A

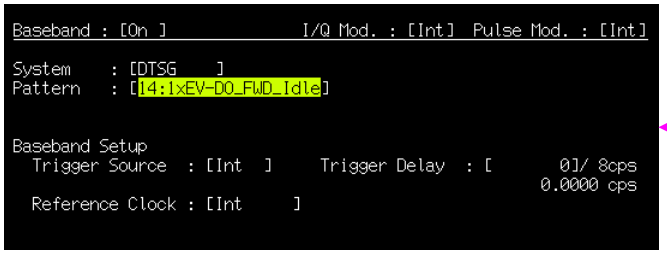
- CDMA2000 1xEV-DO
  - Forward Active Slot

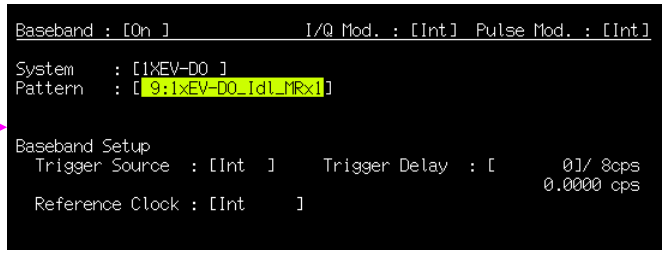


- MX368033A (1xEV-DO)

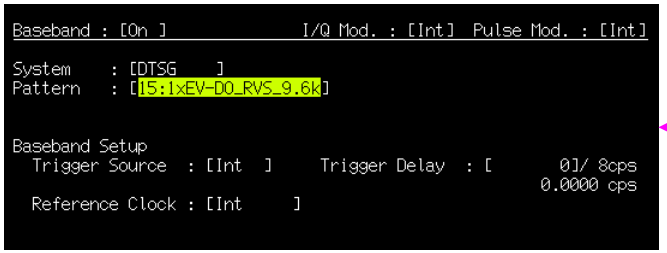


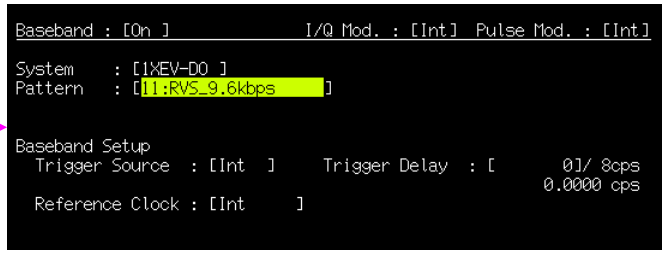
  - Forward Idle Slot



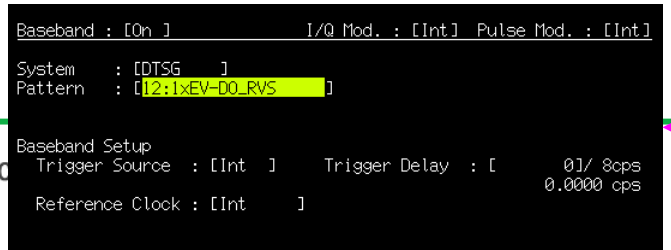


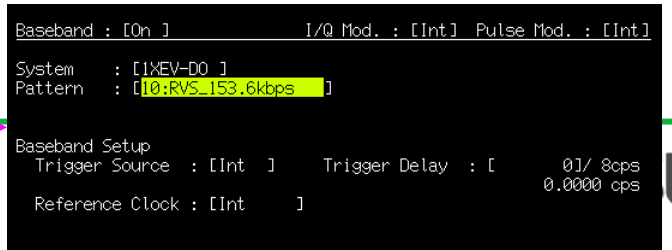
  - Reverse 9.6 kbps





  - Reverse 153.6 kbps



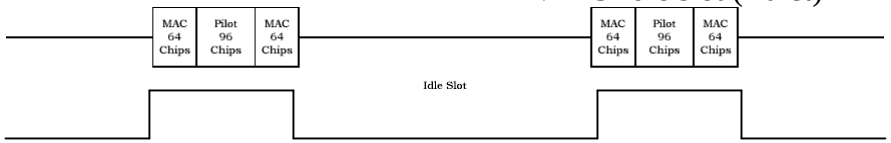


Auxiliary signal Input

- Front panel
  - Trigger
    - Available at CDMA2000 1X Reverse signal
    - Synchronization of external frame clock
    - Frame trigger or start trigger is selectable
      - Used at BS receiver test
  - Ref. Clock
    - Available at CDMA2000 signal
    - Synchronization of external baseband reference clock
    - 8× chip rate (8× 1228.4 kcps = 9830.4 kHz)
      - Used at start trigger
        External reference clock input on rear panel (10/13MHz) is also available

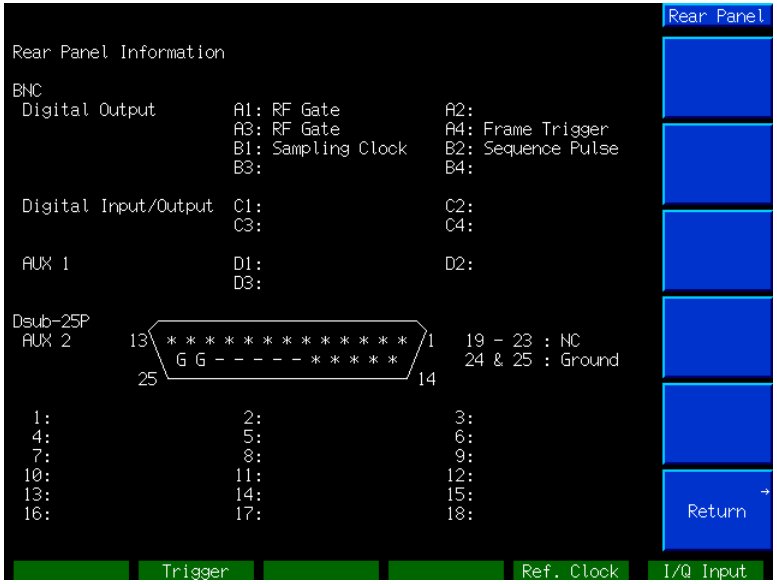
Auxiliary signal Output

- Rear panel
  - RF Gate
    - 1xEV-DO Idle slot (Burst)



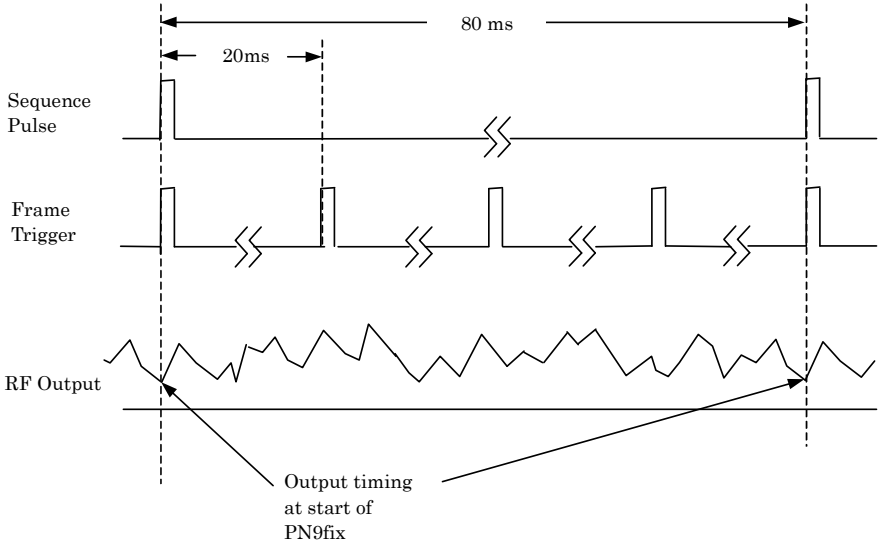
Control signal of internal pulse modulator

  - Sampling Clock
    - Available at CDMA2000 signal
    - Baseband reference clock
      - 8× chip rate
        (8× 1228.4 kcps = 9830.4 kHz)

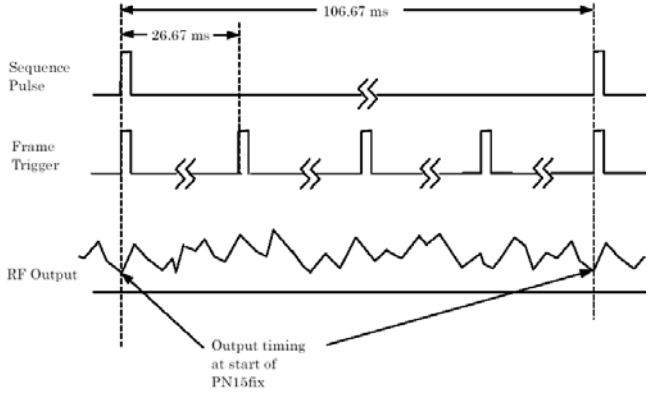


Auxiliary signal Output

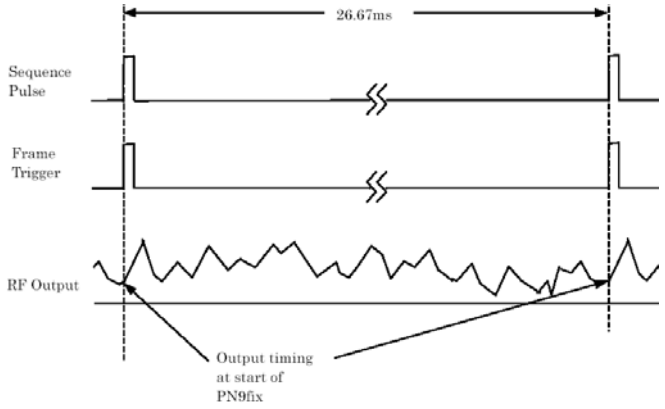
- Rear panel
  - Frame Trigger, Sequence Pulse
    - CDMA2000 1X



  - 1xEV-DO (Active/Idle)

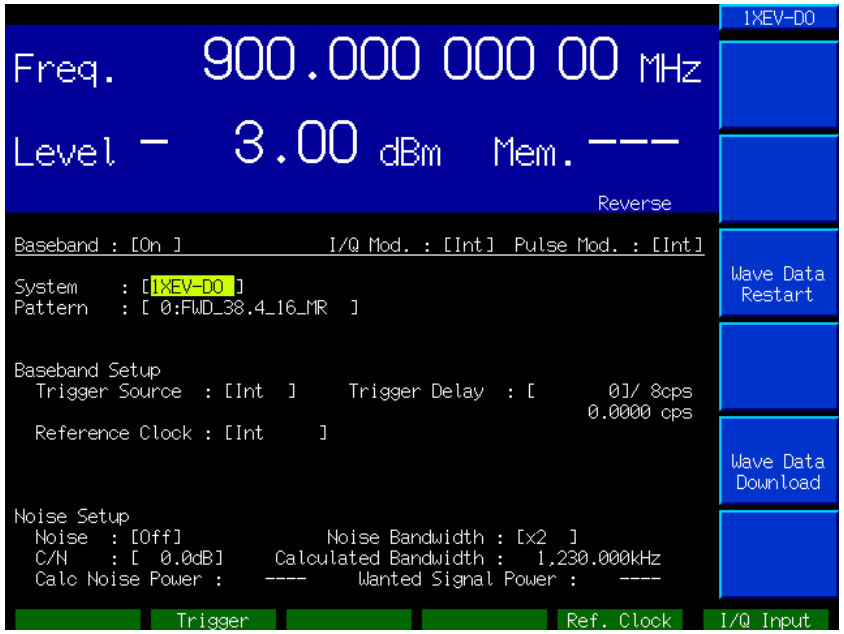


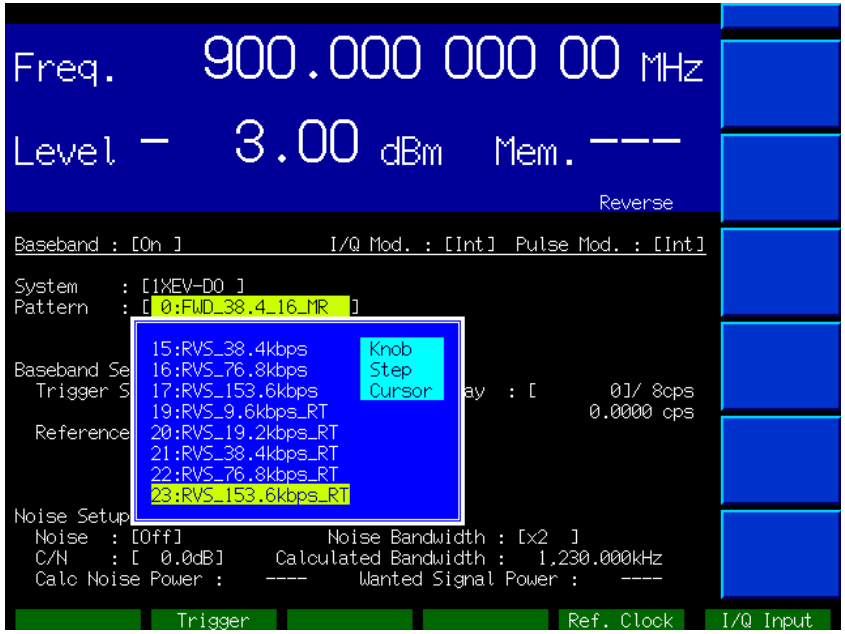
  - 1xEV-DO Reverse



MX368033A CDMA2000 1xEV-DO Signal Generation Software

- **Forward/Reverse CDMA2000 1xEV-DO test signals for 3GPP2 C.S0024 standard can be outputted by installing the MX368033A CDMA2000 1xEV-DO Signal Generation Software in the MU368030A Universal Modulation Unit.**
- **In R&D/production process of components, AN Access Network and AT Access Terminal, the functions to support various applications are provided as the signal source for components and the wanted signal source for receiver test.**



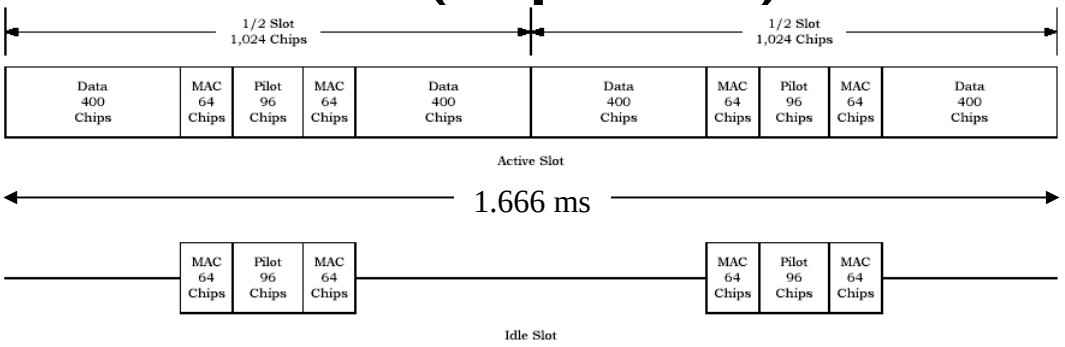


Support of test signal format

- **Receiver test (PER Packet Error Rate) for 3GPP2 C.S0032 (Sector) and C.S0033 (AT) test specifications is performable due to the Coding format (Frame/Slot structuring, CRC addition, turbo coding, interleave) based on 3GPP2 C.S0024.**
- **Just to select the signal patterns saved in large-capacity waveform memory without setting complicated parameters of 3GPP2! Simple operation**
- **High-speed change among Forward 13 data rate signal patterns (with Idle Slot) and Reverse 5 data rate signal patterns < 1 sec**
- **Supporting multi-carrier up to 8×**
- **Quick support is provided by updating the signal pattern files saved from PC memory card to internal memory.**
  - IQ signal pattern file is downloaded to MG3681A via PC memory card (CompactFlash).
    - The I/Q mapping data of 8× over sampling is stored in Waveform data Memory.
      - 16× over sampling at multi-carrier

Signal patterns

- **Forward (13 patterns)**



12 patterns

Data Rate (kbps)	Number of Values per Physical Layer Packet				
	Slots	Bits	Code Rate	Modulation Type	TDM Chips (Preamble, Pilot, MAC, Data)
38.4	16	1,024	1/5	QPSK	1,024 3,072 4,096 24,576
76.8	8	1,024	1/5	QPSK	512 1,536 2,048 12,288
153.6	4	1,024	1/5	QPSK	256 768 1,024 6,144
307.2	2	1,024	1/5	QPSK	128 384 512 3,072
614.4	1	1,024	1/3	QPSK	64 192 256 1,536
307.2	4	2,048	1/3	QPSK	128 768 1,024 6,272
614.4	2	2,048	1/3	QPSK	64 384 512 3,136
1,228.8	1	2,048	1/3	QPSK	64 192 256 1,536
921.6	2	3,072	1/3	8-PSK	64 384 512 3,136
1,843.2	1	3,072	1/3	8-PSK	64 192 256 1,536
1,228.8	2	4,096	1/3	16-QAM	64 384 512 3,136
2,457.6	1	4,096	1/3	16-QAM	64 192 256 1,536

- **Reverse (10 patterns)**
  - » for receiver test of Sector
  - » for transmitter test of AT

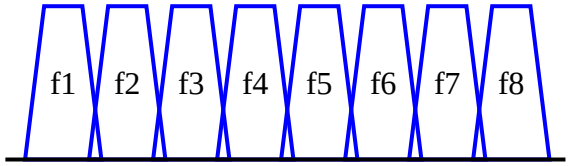
Data Rate (kbps)	9.6	19.2	38.4	76.8	153.6
Reverse Rate Index	1	2	3	4	5
Code Rate	1/4	1/4	1/4	1/4	1/2
Bits per Physical Layer Packet	256	512	1,024	2,048	4,096
Number of Turbo Encoder Input Symbols	250	506	1,018	2,042	4,090
Turbo Encoder Code Rate	1/4	1/4	1/4	1/4	1/2
Encoder Output Block Length (Code Symbols)	1,024	2,048	4,096	8,192	8,192

Multi-carrier

Multi-carrier are stored in PC memory card as sample signal patterns.

- Forward Active Slot multi-carrier (8×, 4×, 3×, 2×, 1×)
- Forward Idle Slot multi-carrier (8×, 4×, 3×, 2×, 1×)
  - Frequency offset: 1.25 MHz
  - Pilot Channel:
    - PN Offset Index = 0 (f1), 1 (f2), 2 (f3), 3 (f4), 4 (f5), 5 (f6), 6 (f7), 7 (f8)
  - MAC Channel:
    - MACIndex = RA, 13 RPC Channel

4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16, 17	(f1)
4, 18, 19, 20, 21, 22, 23, 24, 25, 26, 27, 28, 29, 30	(f2)
4, 31, 32, 33, 34, 35, 36, 37, 38, 39, 40, 41, 42, 43	(f3)
4, 44, 45, 46, 47, 48, 49, 50, 51, 52, 53, 54, 55, 56	(f4)
4, 57, 58, 59, 60, 61, 62, 63, 5, 6, 7, 8, 9, 10	(f5)
4, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20, 21, 22, 23	(f6)
4, 24, 25, 26, 27, 28, 29, 30, 31, 32, 33, 34, 35, 36	(f7)
4, 37, 38, 39, 40, 41, 42, 43, 44, 45, 46, 47, 48, 49	(f8)

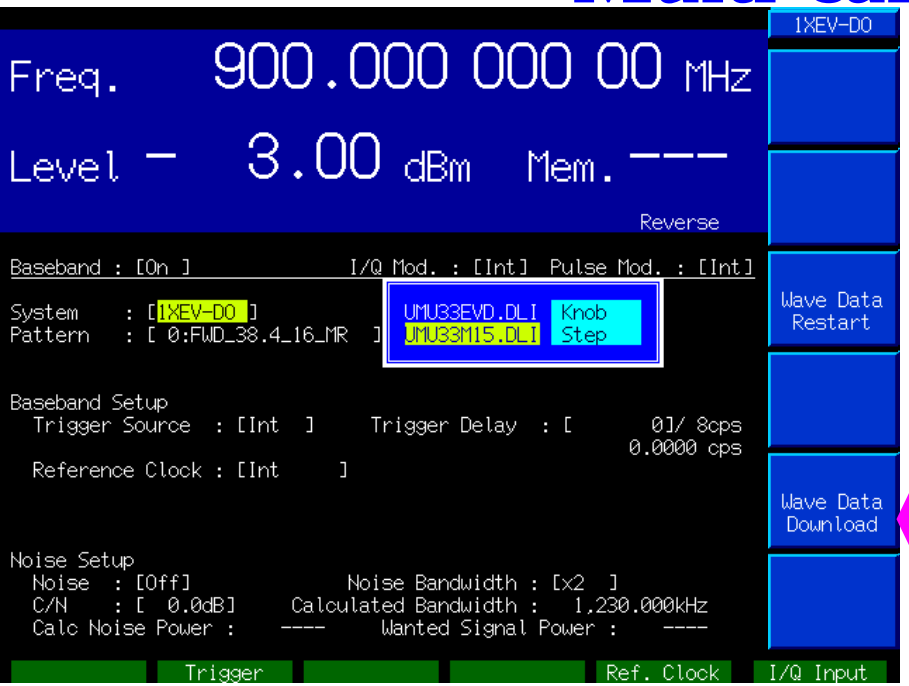


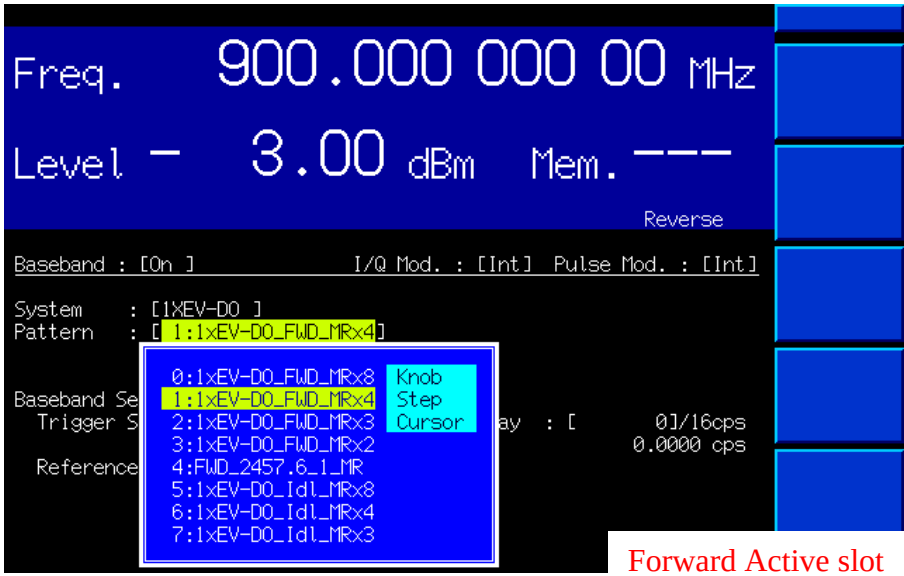
    - RABit = PRBS
    - RPCBit = PRBS
  - Frame length: 3 frame (Active Slot), 1 frame (Idle Slot)

Active Slot

- Traffic Channel: PN15fix
- Data Rate: 2457.6 kbps
- Preamble: 64 chip
- Modulation: 16QAM

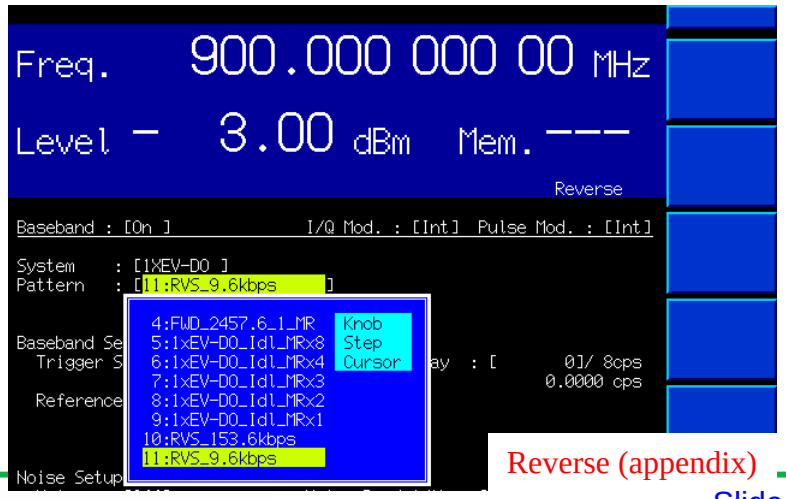
Multi-carrier select



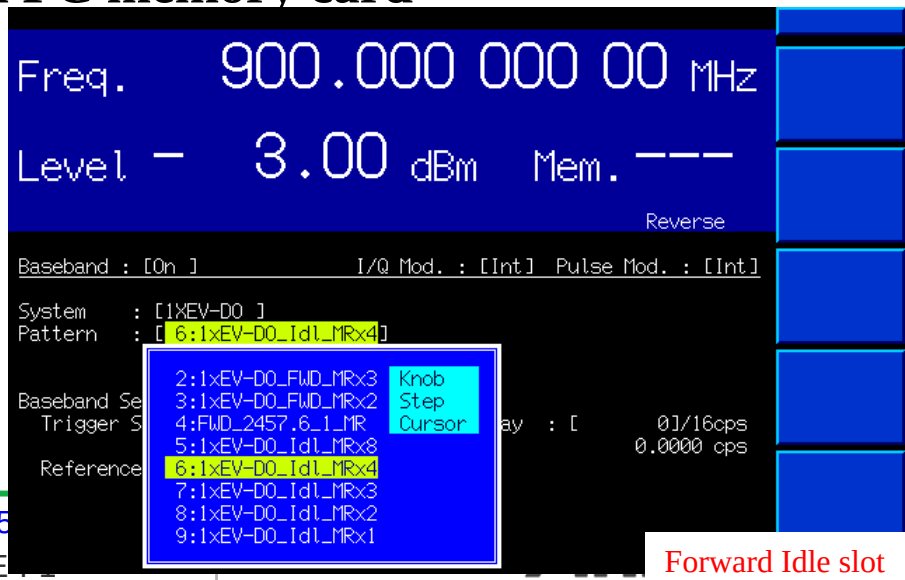


Forward Active slot

Downloading the signal pattern file from PC memory card

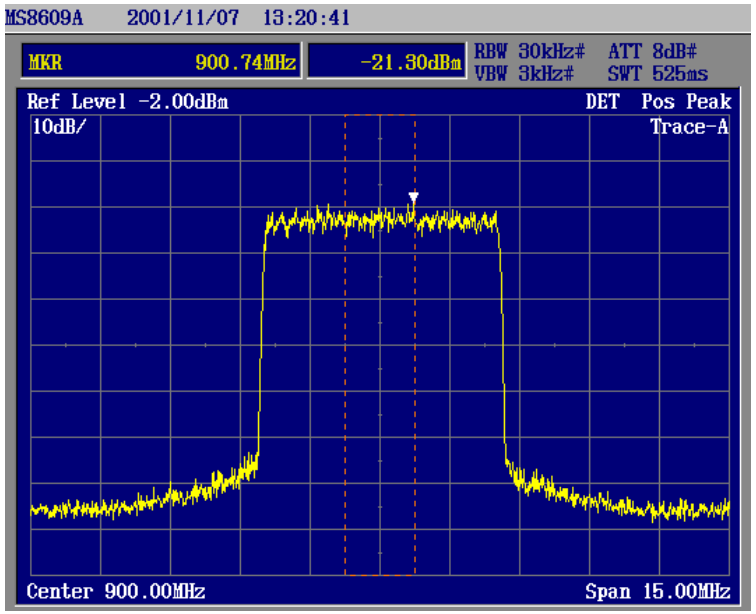


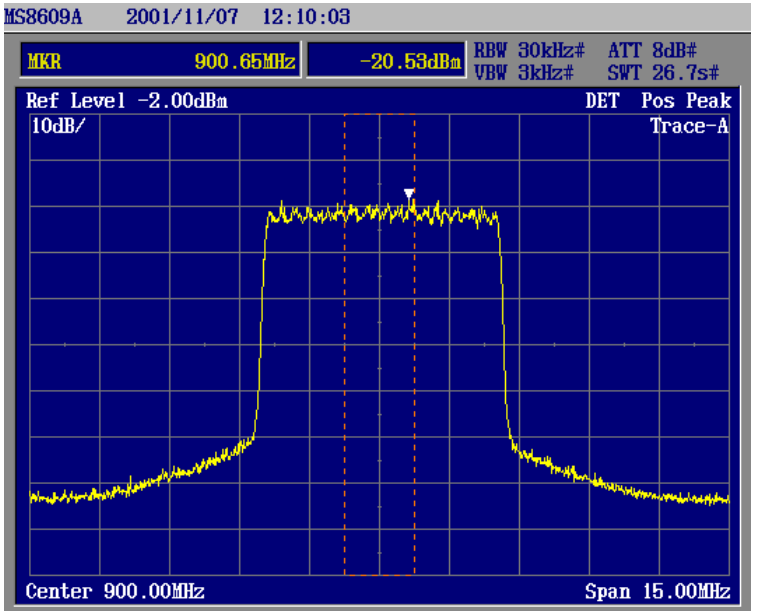
Reverse (appendix)



Forward Idle slot

4 carriers Spurious Emissions (typ.)





Forward Active Slot

L* / U* dBc/30kHz

1: -69.35 / -70.81

2: -73.78 / -74.87

3: -74.96 / -75.36

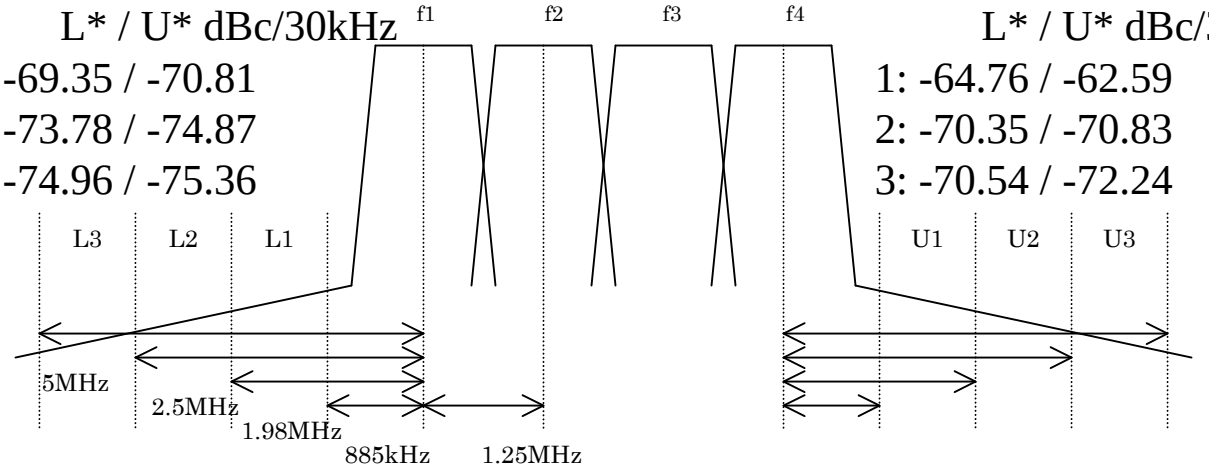
Forward Idle Slot

L* / U* dBc/30kHz

1: -64.76 / -62.59

2: -70.35 / -70.83

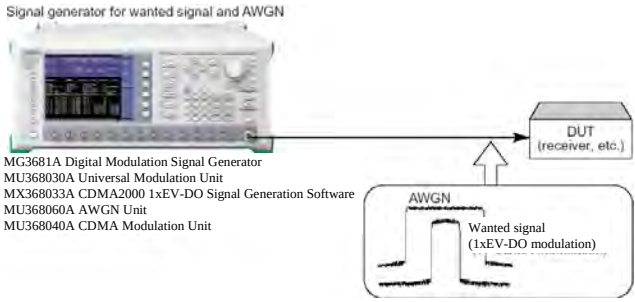
3: -70.54 / -72.24



AWGN mixing

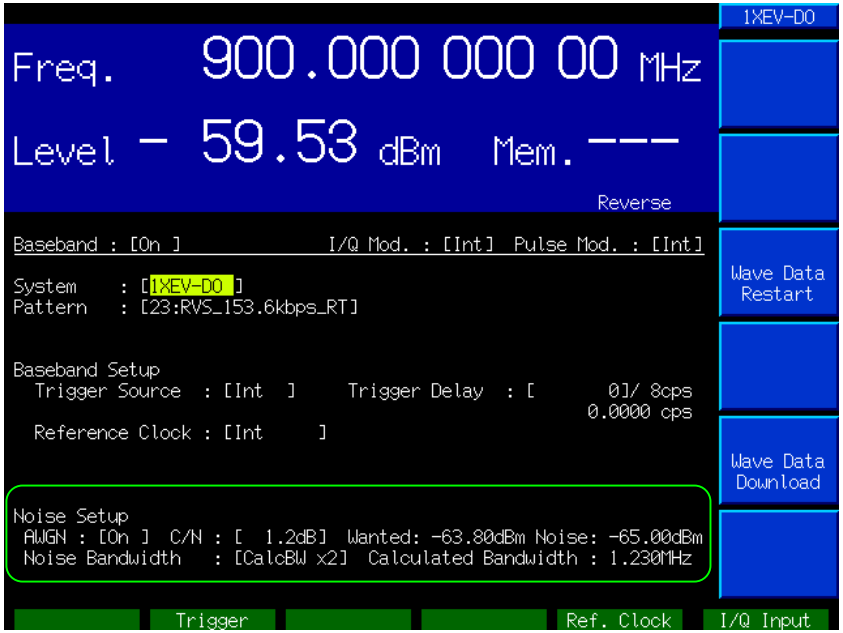
Single unit is performable dynamic range test of BS receiver.

- **Mixing AWGN to CDMA2000 wanted signal**
- **High-accuracy and high-stability C/N**
  - » -30 ~ -30 dB, 0.1 dB resolution



MG3681A Digital Modulation Signal Generator
MU368030A Universal Modulation Unit
MX368033A CDMA2000 1xEV-DO Signal Generation Software
MU368060A AWGN Unit
MU368040A CDMA Modulation Unit

- **Selecting AWGN bandwidth**
  - » 2× 1.23MHz = 2.46 MHz
  - » 3× 1.23MHz = 3.69 MHz
  - » 4× 1.23MHz = 4.92 MHz

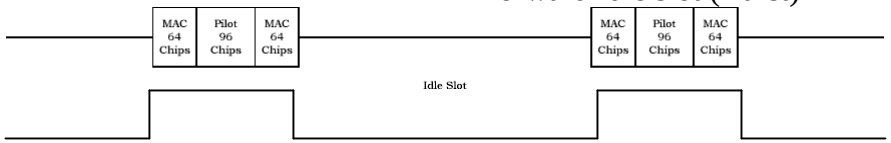


Auxiliary signal Input

- Front panel
  - Trigger
    - Synchronization of external frame clock
    - Frame trigger or start trigger is selectable
      - Used at Sector receiver test
  - Ref. Clock
    - Available at single carrier
    - Synchronization of external baseband reference clock
    - 8× chip rate (8× 1228.4 kcps = 9830.4 kHz)
      - Used at start trigger
        External reference clock input on rear panel (10/13MHz) is also available

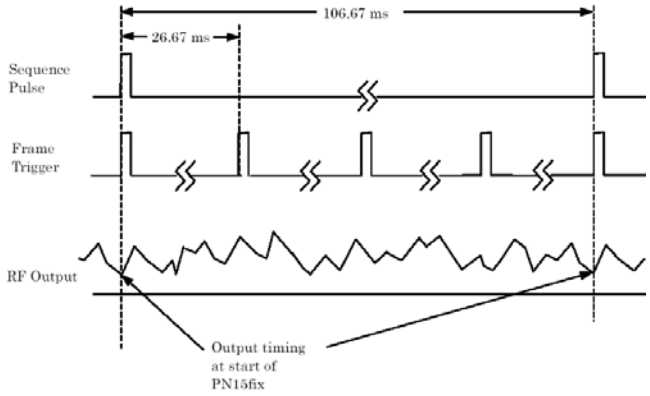
Auxiliary signal Output

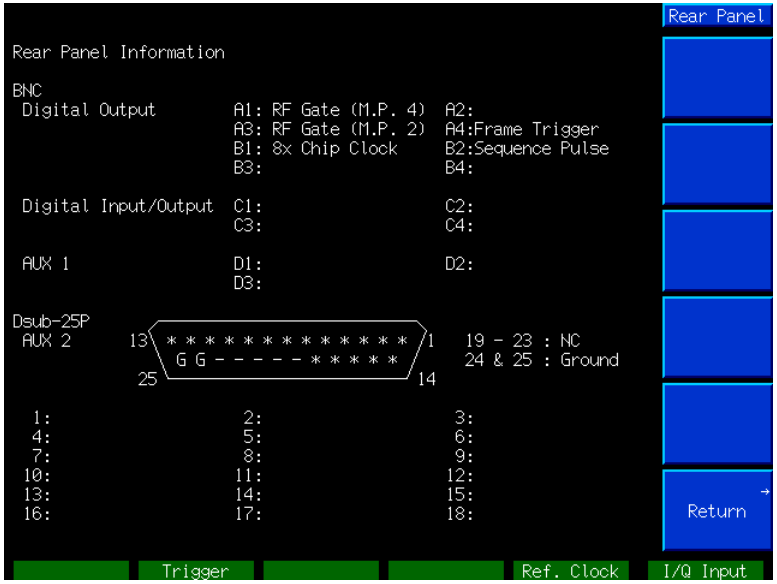
- Rear panel
  - RF Gate
    - Forward Idle slot (Burst)



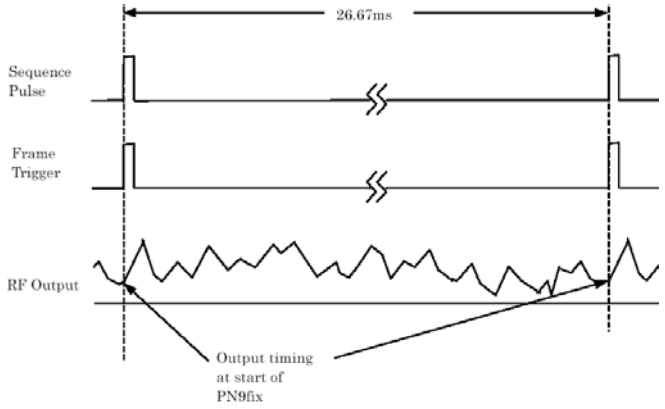
Control signal of internal pulse modulator

  - 8x Chip Clock
    - Available at single carrier
    - Baseband reference clock
      - 8× chip rate
        (8× 1228.4 kcps = 9830.4 kHz)
  - Frame Trigger, Sequence Pulse
    - Forward (Active/Idle)



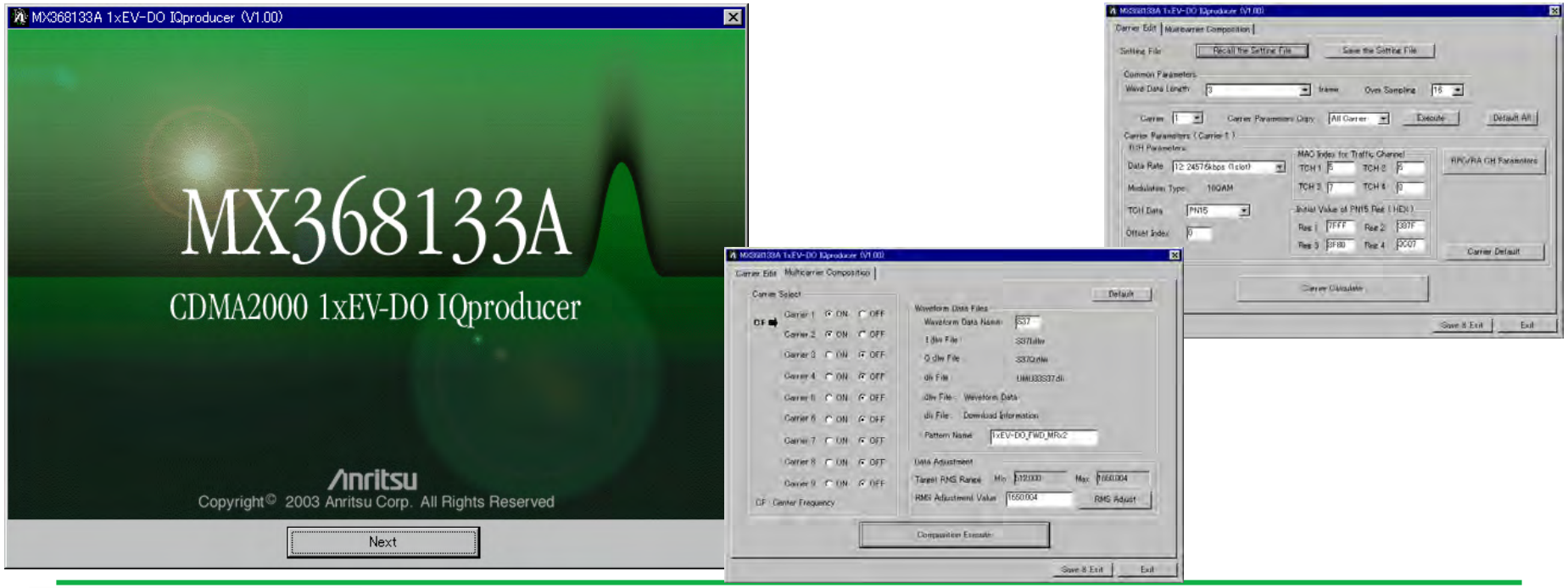


  - Reverse



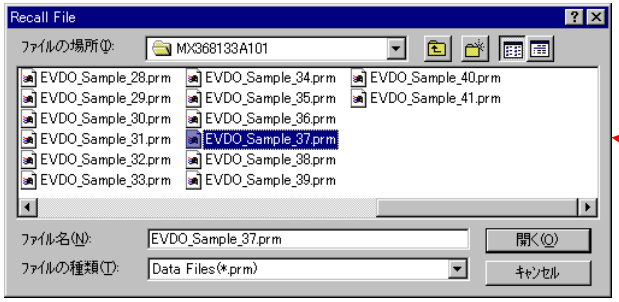
MX368133A CDMA2000 1xEV-DO IQproducer™

- It is Windows application software which upgrades the functioning of MX368033A installed in the MG3681A.
- The IQ mapping data file for signal patterns, which are generated by MU368030A Universal Modulation Unit incorporated in the MG3681A is created.
- In R&D process of components, AN and AT, the functions to perform various evaluation of power amplifier and demodulation test are supported.



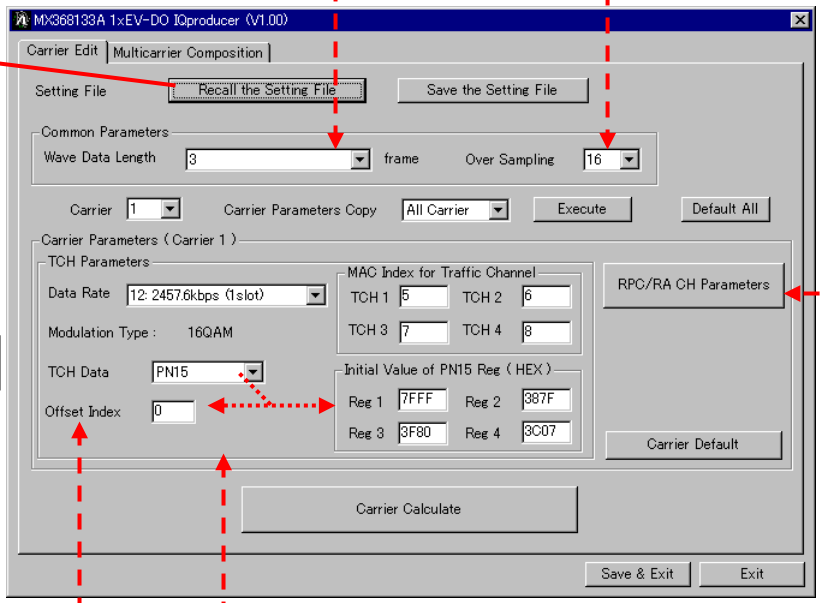
Reference setting files for easy setup

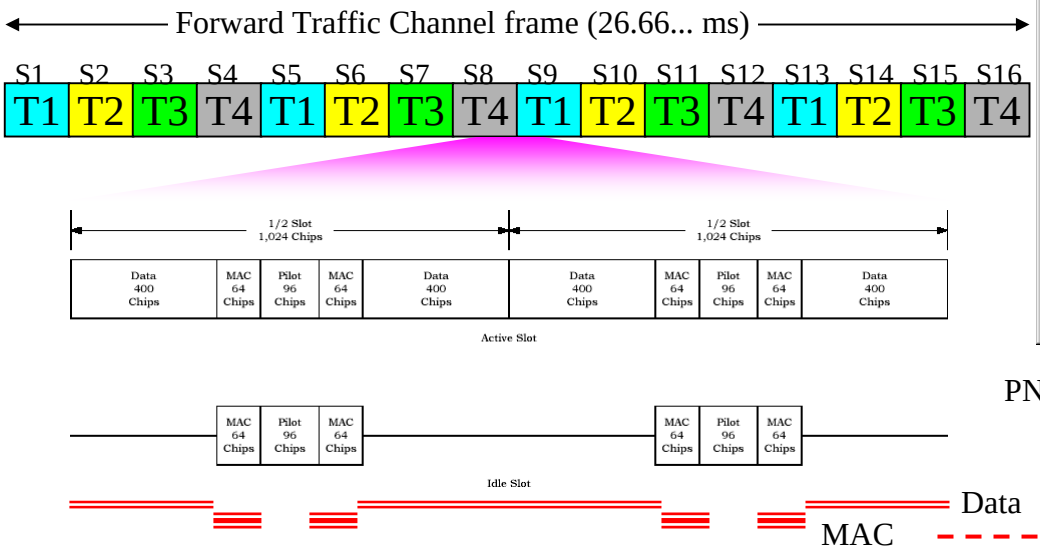
- **Since the reference setting files for signal patterns of standard MX368033A is recorded, a signal pattern can be created easily only by editing a parameter changing.**



× 26.66...ms

× 1.23 MHz(Chip rate)





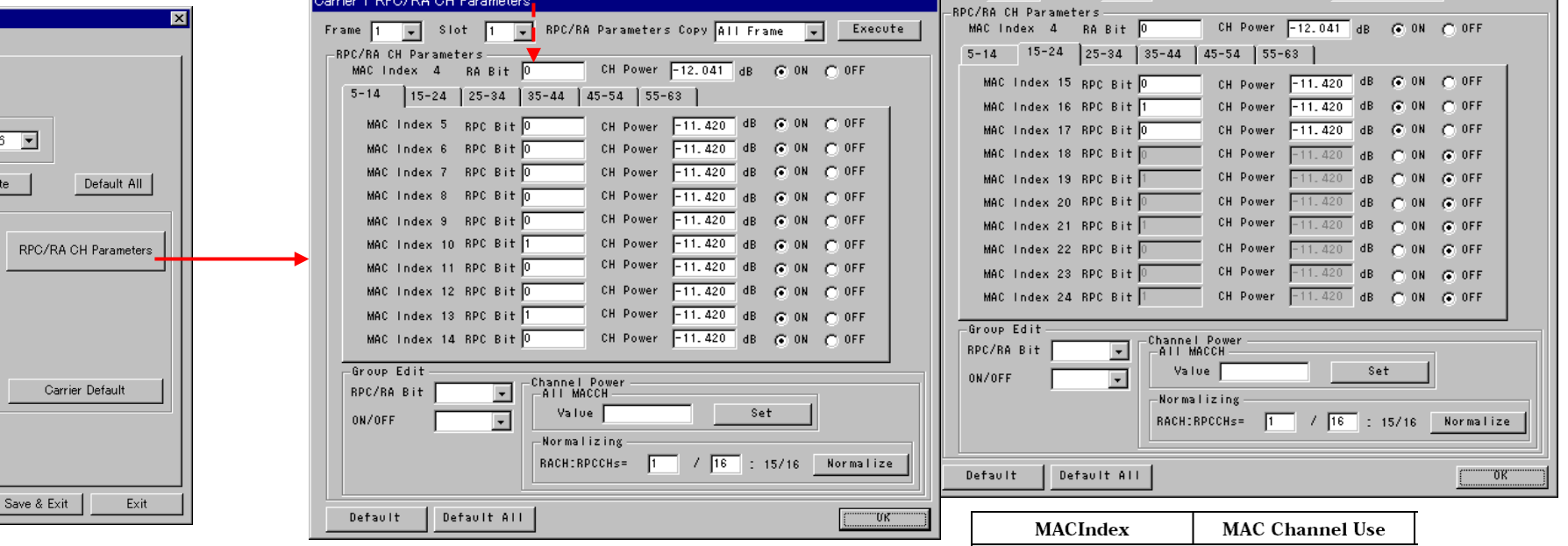
PN Offset Index

Data

MAC

Editing of various MAC channels

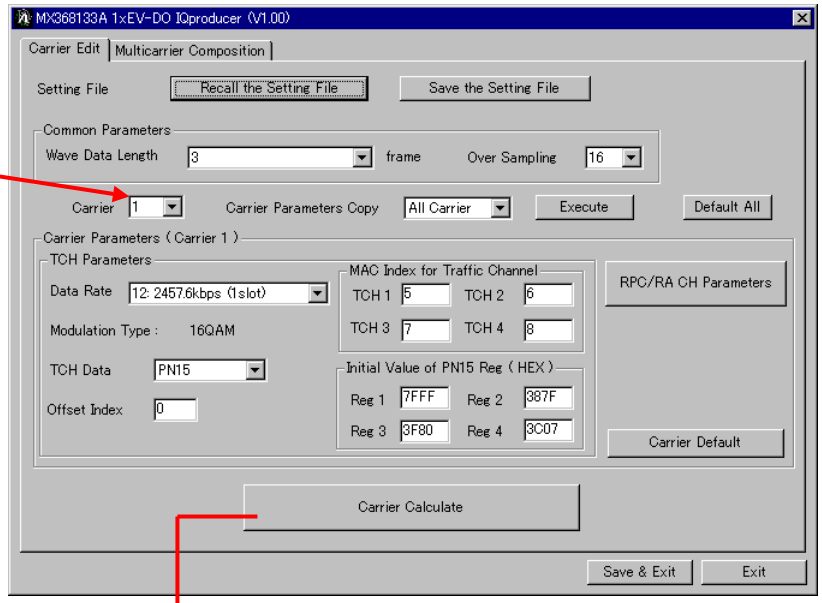
- **Able to edit parameters for each frame and slot**
- **Multiplex of RA channels and RPC channels**

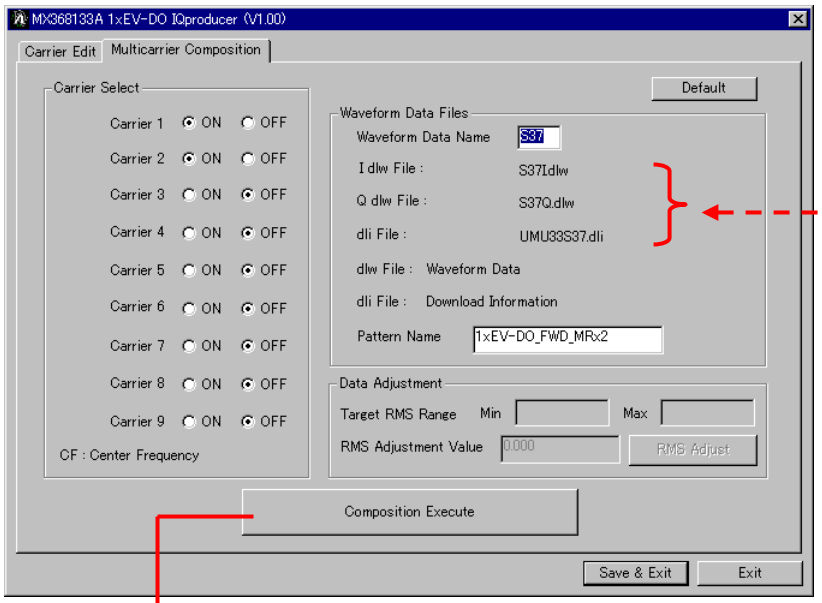


MACIndex	MAC Channel Use
0 and 1	Not Used
2	Not Used
3	Not Used
4	RA Channel
5-63	Available for RPC Channel and DRCLock Channel Transmissions

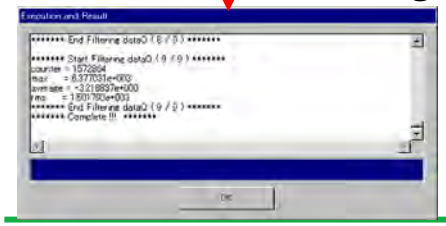
Creating Forward multi-carrier

- **Able to edit parameters for each carrier**
  - » 1 ~ 9
- **Up to 9 carriers**
  - » 1.25MHz offset

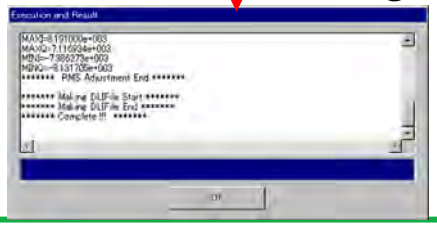




calculating the IQ mapping data



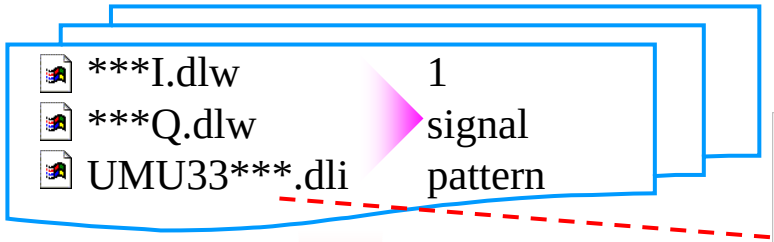
creating 3 files



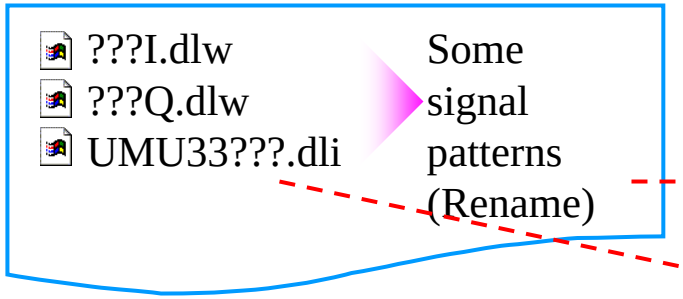
- I data
- Q data
- Configuration file for download

Signal pattern combiner

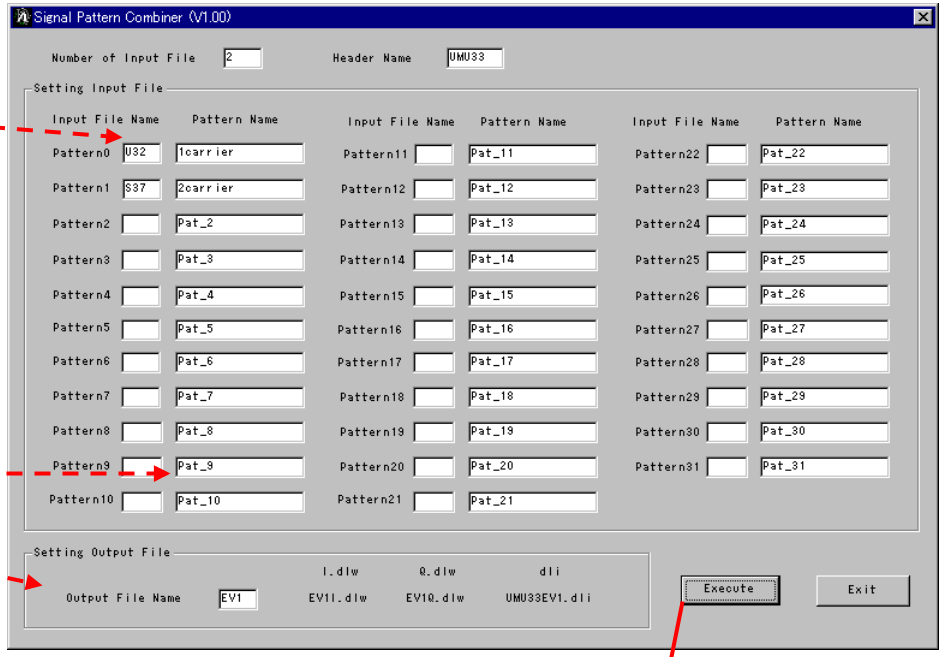
Created signal pattern files

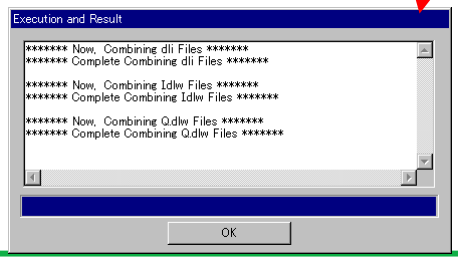


Combined signal pattern file



- **Performable high-speed change of signal pattern**





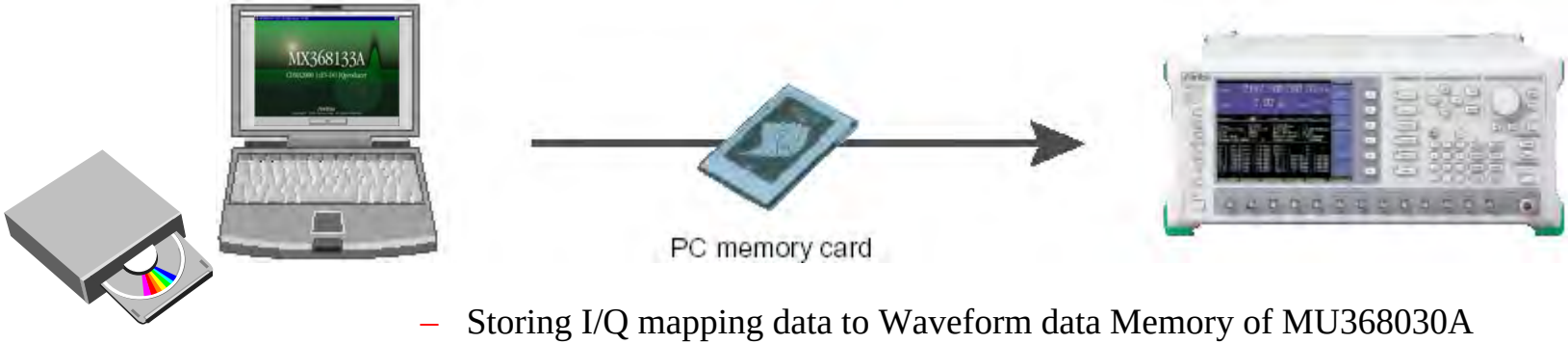
Operating requirements

Personal computer

- **OS: Windows 2000, XP recommendation**
- **CPU: ≧ 300MHz**
- **Memory: ≧ 128MB recommendation**
- **HDD: ≦ 512MB Occupied**
- **Display: ≧ 800×600 pixel**
- **Peripheral equipment:**

  Reading CD-R

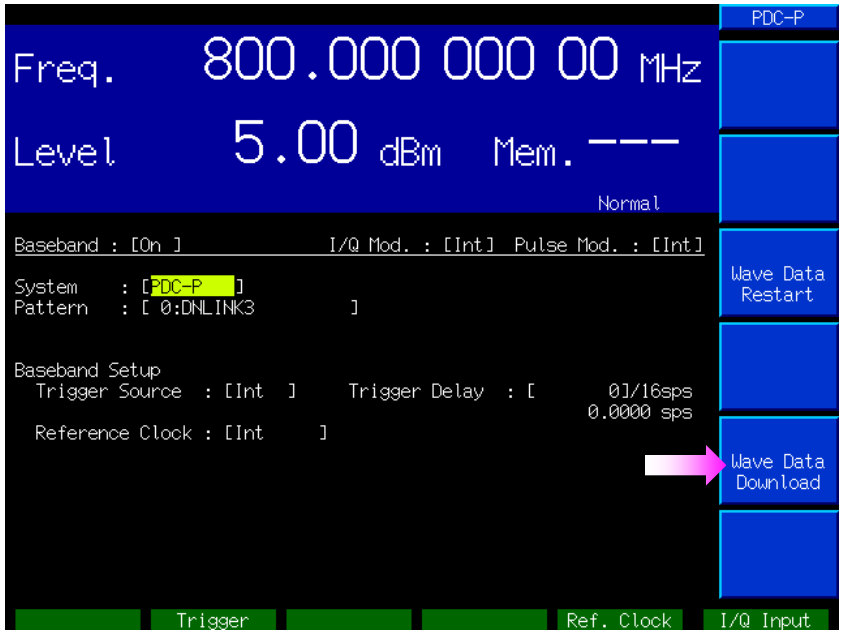
  Saving to PC memory card(CompactFrash+PC card adapter)

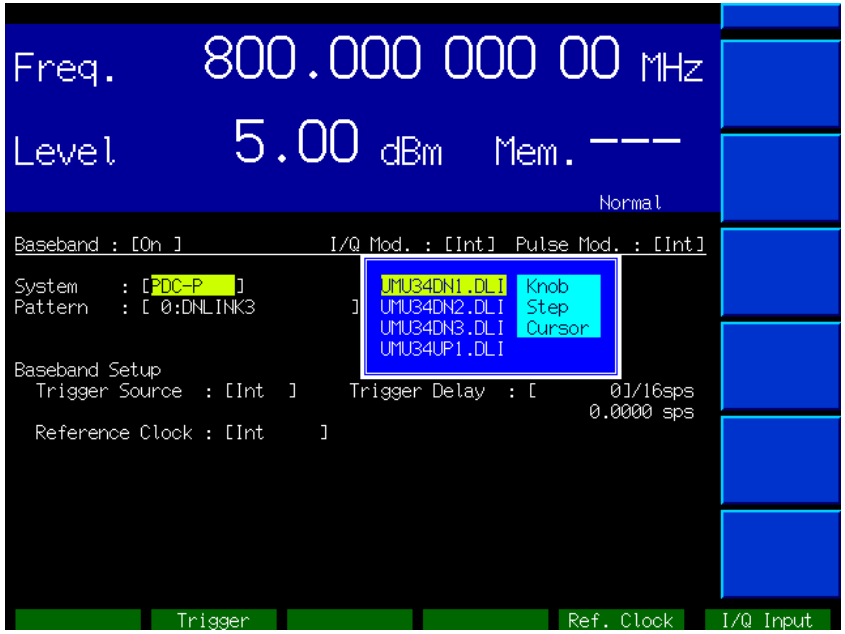


– Storing I/Q mapping data to Waveform data Memory of MU368030A

MX368034A PDC Packet Software

- **Downlink/Uplink PDC user packet channel (UPCH) test signals for RCR STD-27 standard can be outputted by installing the MX368034A PDC Packet Software in the MU368030A Universal Modulation Unit.**
- **In R&D/production process of components, base stations (BS) and mobile stations (MS), the functions to support various applications are provided as the signal source for components and the wanted signal source for receiver test.**



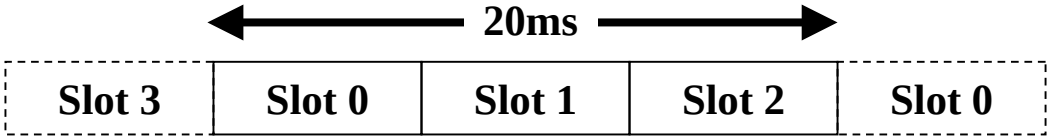


Support of test signal format

- **Packet (Downlink up to 28.8 kbps) receiver test (BER) for BS/MS is performable due to the Frame/Slot format based on RCR STD-27.**
- **Just to select the signal patterns saved in large-capacity waveform memory without setting complicated parameters of RCR STD-27! Simple operation**
- **Changing among Downlink 3 data rate signal patterns and Uplink 1 data rate signal pattern (approx. 10 min)**
- **UPCH ⇔ TCH (MX368011A) High-speed change < 10 sec**
- **Quick support is provided by updating the waveform data saved from PC memory card to internal memory.**
  - IQ signal pattern file is downloaded to MG3681A via PC memory card (CompactFlash).
    - The I/Q mapping data of 16× over sampling is stored in Waveform data Memory.

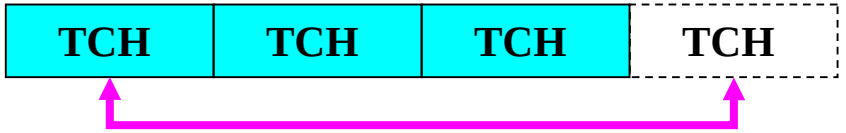
Signal patterns frame configuration

- **Physical channel for packet communication (UPCH)**

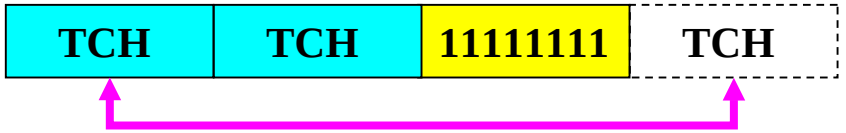


Patterns

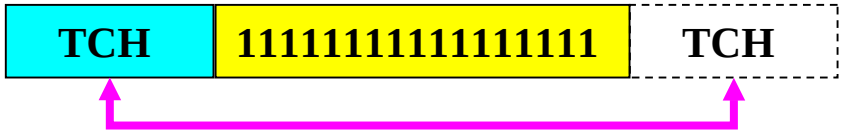
» Downlink 3 slots



» Downlink 2 slots



» Downlink 1 slot



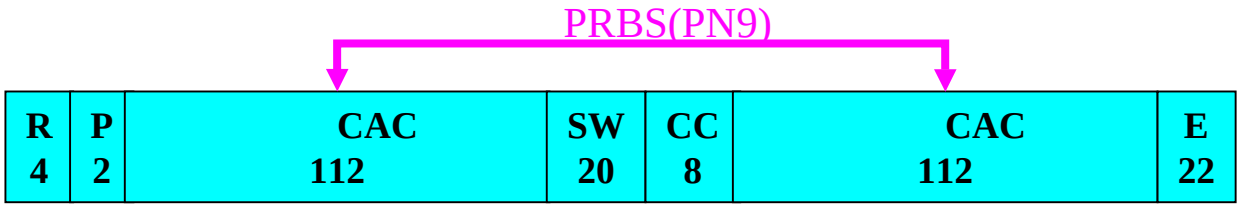
PRBS(PN9) in the same slot

» Uplink 1 slot

- Super-frame is not supported

Signal patterns slot configuration

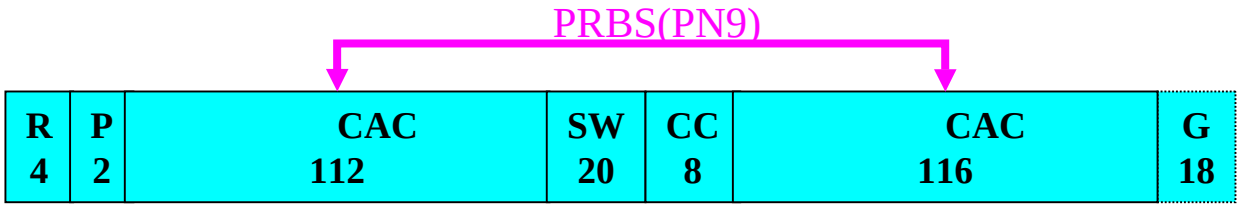
- **Downlink physical channel for packet communication (UPCH)**
  - » 280 bit
    - Scrambling Off



- » R Guard time for burst transient response 0000
- » P Preamble 10
- » SW Synchronous word
  - – Slot 0: S1(87A4B)
  - – Slot 1: S2(9D236)
  - – Slot 2: S3(81D75)
- » CC Color code 00000000
- » E Collision control bit

Signal patterns slot configuration

- **Uplink physical channel for packet communication (UPCH)**
  - » 280 bit
    - Scrambling Off

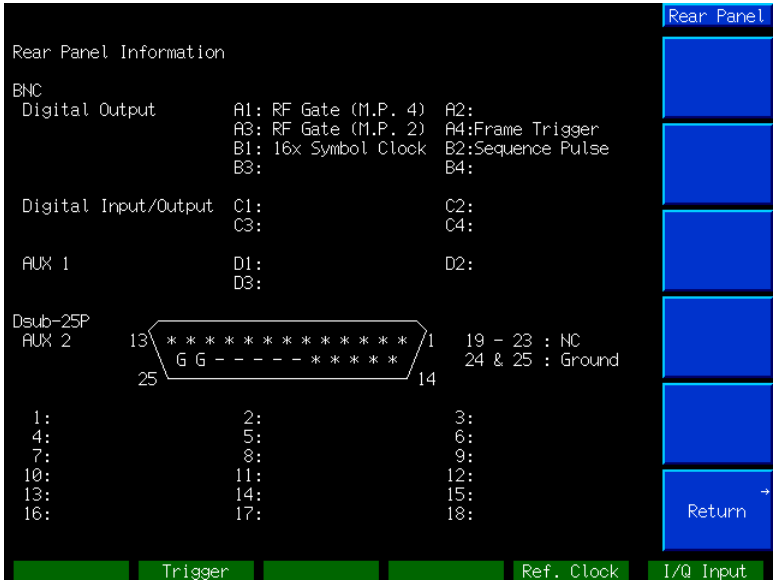


- » R Guard time for burst transient response 0000
- » P Preamble 10
- » SW Synchronous word
  - – Slot 0: S1’(785B4)
- » CC Color code 00000000
- » G Guard time

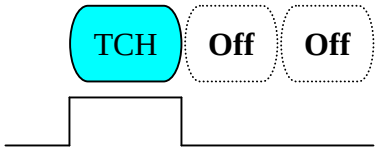
Auxiliary signal Input

- Front panel
  - Trigger
    - Synchronization of external frame clock
    - Frame trigger or start trigger is selectable
      - Used at BS receiver test
  - Ref. Clock
    - Synchronization of external baseband reference clock
    - 16× symbol rate (16× 21 ksps = 336 kHz)
      - Used at start trigger
        External reference clock input on rear panel (10/13MHz) is also available

Auxiliary signal Output



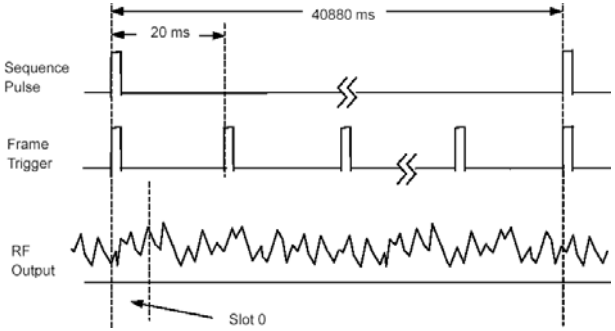
- » Rear panel
  - – RF Gate
    - – Uplink (Burst)



Control signal of internal pulse modulator

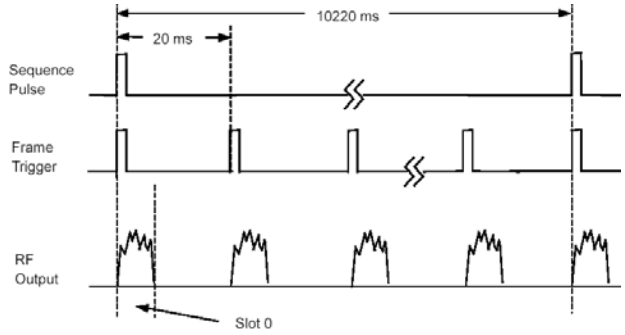
  - – 16x Symbol Clock
    - • Baseband reference clock
      - – 16× symbol rate
        (16× 21 ksps = 336 kHz)
  - – Frame Trigger, Sequence Pulse
    - – Downlink

2044 frames



- – Uplink

511 frames



MX368035A PHS Signal Generation Software

- **Downlink/Uplink PHS test signals (TCH) for RCR STD-28 standard can be outputted by installing the MX368035A PHS Signal Generation Software in the MU368030A Universal Modulation Unit.**
- **In R&D/production process of components, CS and PS, the functions to support various applications are provided as the signal source for components, the wanted signal source and the interfering signal source for receiver test.**

Support of test signal format

- **Receiver test (BER) for CS/PS test specifications is performable due to the π/4DQPSK Frame/Slot format based on RCR STD-28 Version 4.0.**
- **Just to select the signal patterns saved in large-capacity waveform memory without setting complicated parameters of RCR STD-28!**

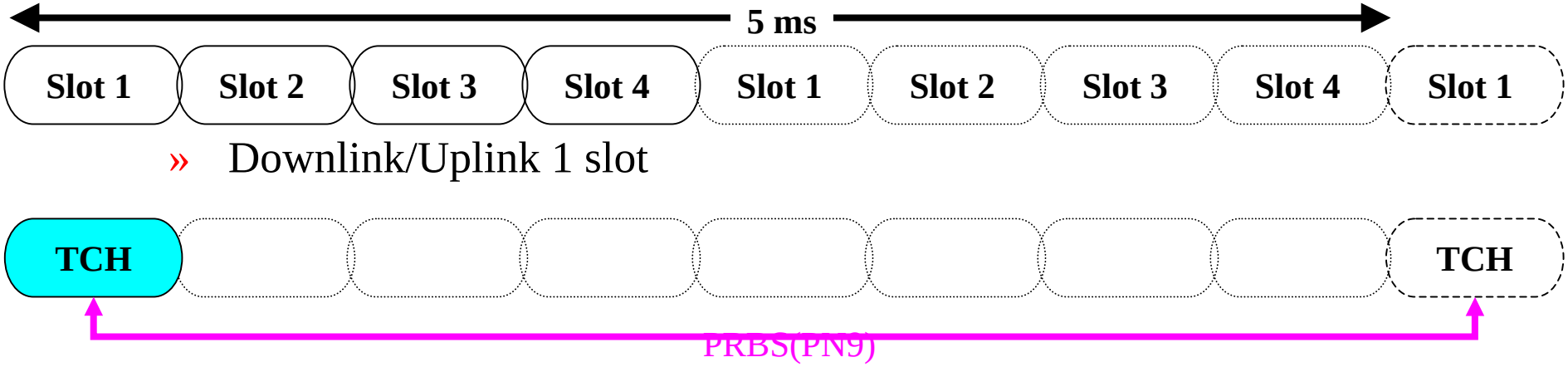
  Simple operation
- **High-speed change the signal patterns < 1 sec**
- **Continuous modulated signal patterns for Advanced PHS on RCR STD-28 Version 4.0 are appended as sample file.**

	16QAM	8PSK	QPSK	BPSK	kHzBW	ksps	α
– 1x:	PN9/15	PN9/15	PN9/15	PN9/15	: 288	192	0.5
– 3x:	PN9/15	PN9/15	PN9/15	PN9/15	: 884	640	0.38

- **Quick support is provided by updating the signal pattern files saved from PC memory card to internal memory.**
  - IQ signal pattern file is downloaded to MG3681A via PC memory card (CompactFlash).
    - The I/Q mapping data of 20× over sampling is stored in Waveform data Memory.

Signal patterns frame configuration

- π/4DQPSK Traffic channel (TCH)



» Downlink/Uplink 1 slot

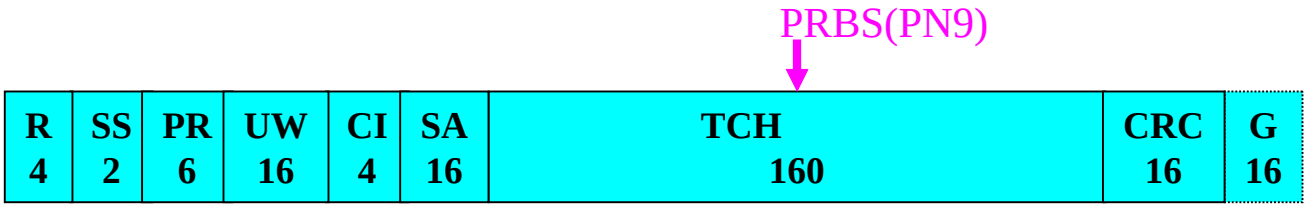
- Super-frame is not supported

– for the wanted signal source for receiver test

- **π/4DQPSK PN9 continuous modulation**
  - for the signal source for compornents
- **π/4DQPSK PN15 continuous modulation**
  - for the interfering signal source for receiver test

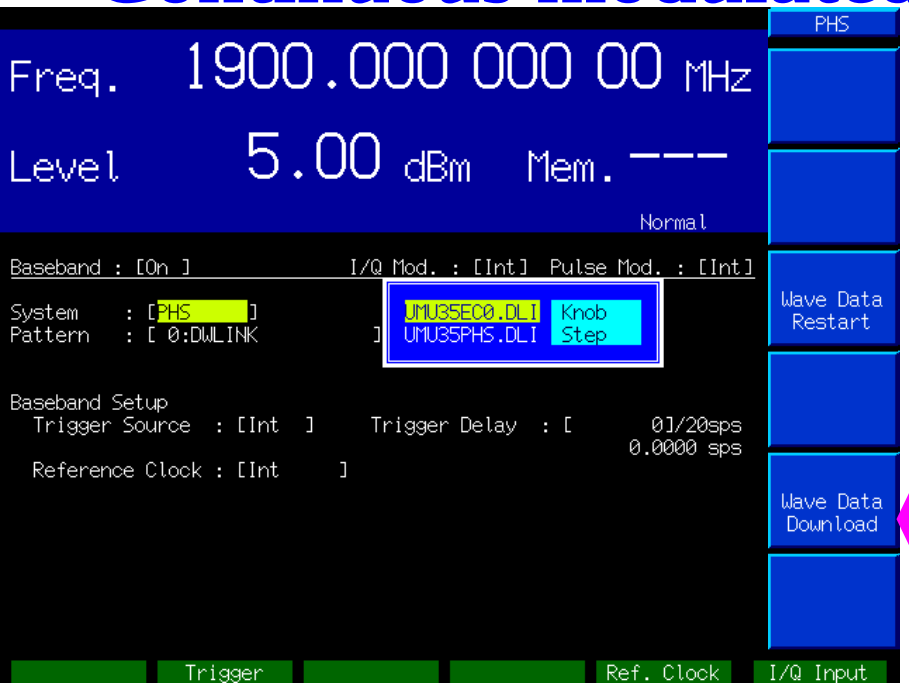
Signal patterns slot configuration

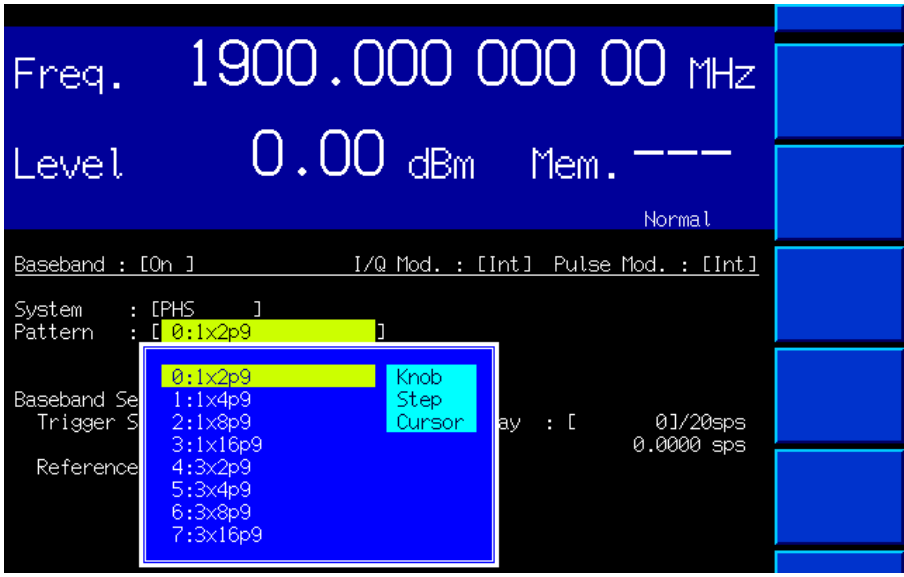
- **π/4DQPSK Traffic channel (TCH)**
  - 240 bit, 625 ms
    - Scrambling Off



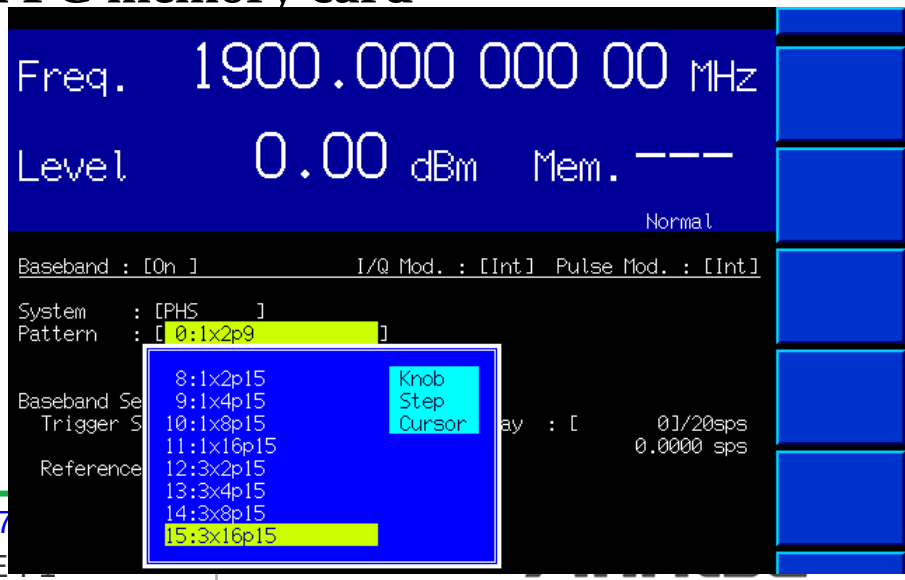
- R Ramp time for transient response
- SS Start symbol 10
- PR Preamble 011001
- UW Unique word
  - Uplink: E149
  - Downlink: 3D4C
- CI Channel identifier 0000 (TCH)
- SA SACCH All “0”
- G Guard time

Continuous modulated signal patterns select

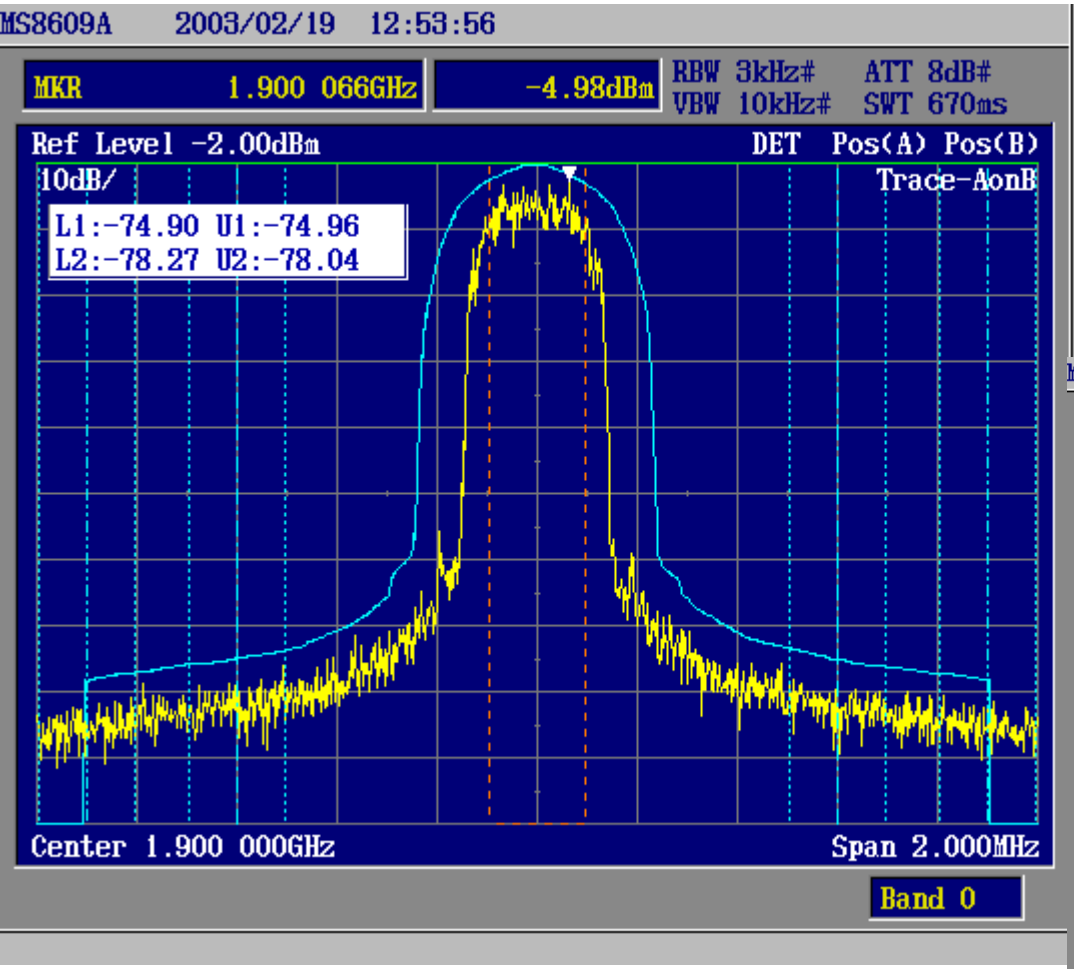


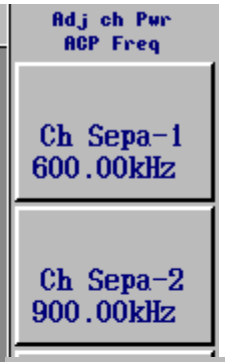


Downloading the signal pattern file from PC memory card

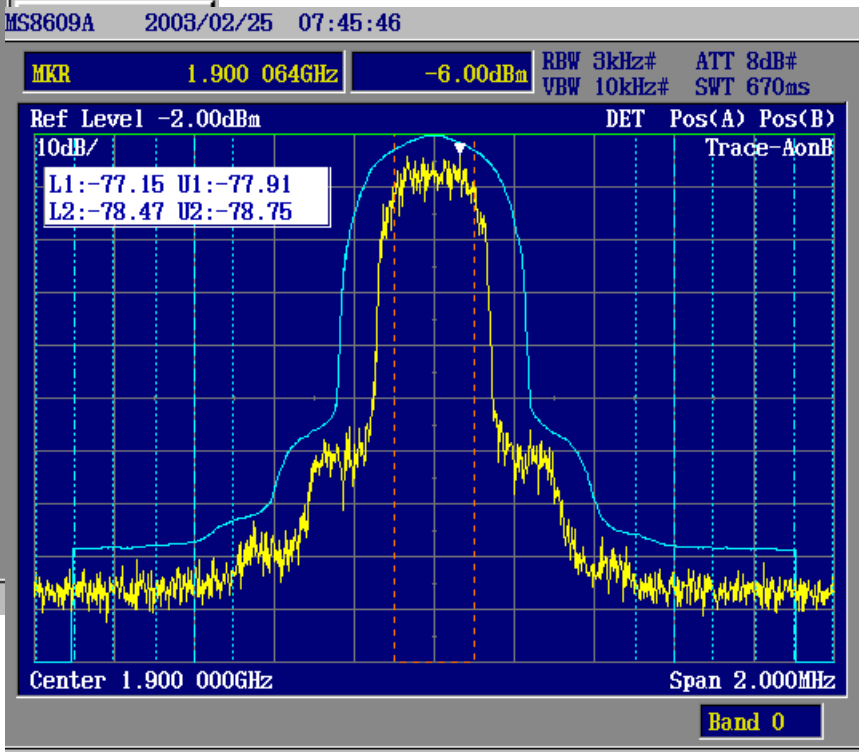


Contrast of typical ACLR
≤ +5 dBm, Continuous modulation





MG3670B

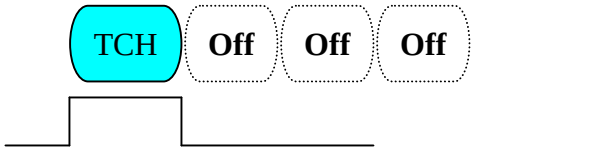


Auxiliary signal Input

- Front panel
  - Trigger
    - Synchronization of external frame clock
    - Frame trigger or start trigger is selectable
      - Used at CS receiver test
  - Ref. Clock
    - Synchronization of external baseband reference clock
    - 20× symbol rate (20× 192 ksps = 3,840 kHz)
      - Used at start trigger
        External reference clock input on rear panel (10/13MHz) is also available

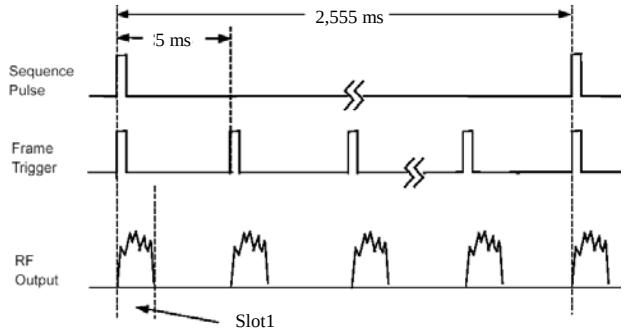
Auxiliary signal Output

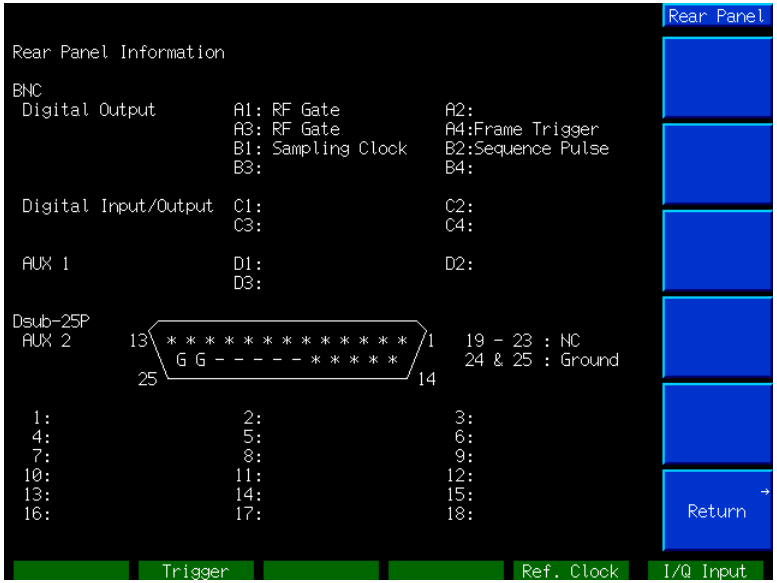
- Rear panel
  - RF Gate



Control signal of internal pulse modulator

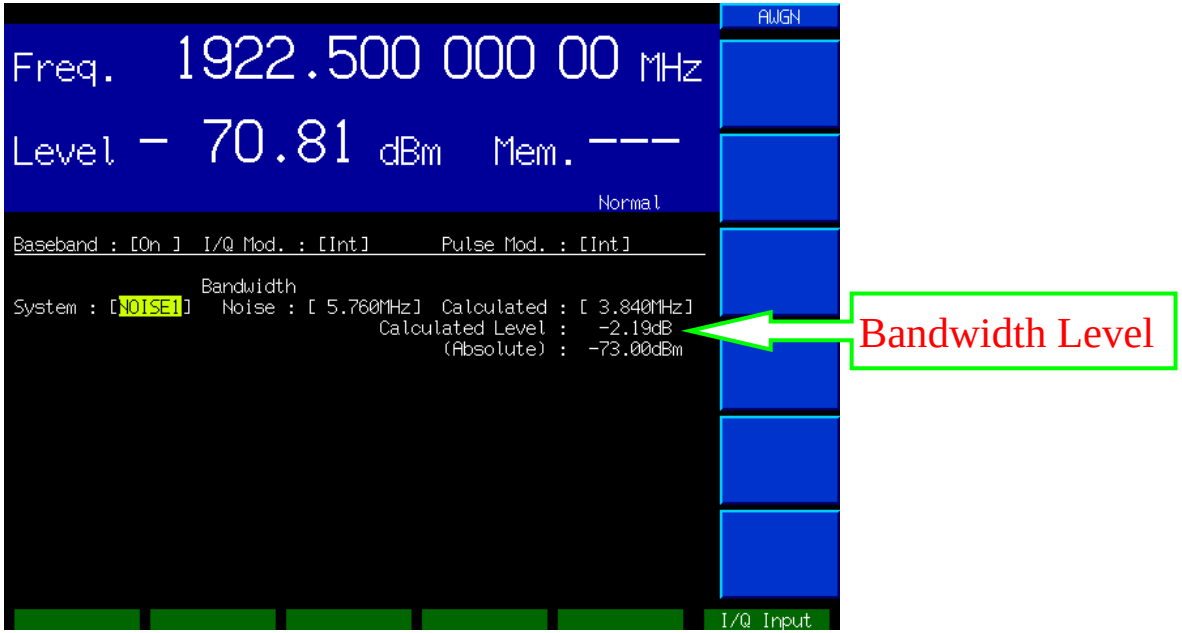
  - Sampling Clock
    - Baseband reference clock
      - 20× symbol rate
        (20× 192 ksps = 3,840 kHz)
  - Frame Trigger, Sequence Pulse
    511 frames





MU368060A AWGN

- **AWGN for 3GPP(FDD/TDD) and 3GPP2(CDMA2000) standards can be outputted at real time by installing the MU368060A AWGN Unit in the MG3681A Digital Modulation Signal Generator.**
- **In R&D/production process of base stations(BS) and user equipment(UE), the function is provided as the AWGN source for receiver test.**



AWGN test support

- **3GPP(FDD)**
  - » At mounting MX368041B W-CDMA Software installed in MU368040A CDMA Modulation Unit together...
    - – Wanted signal source (W-CDMA modulation)
    - – Interfering signal source (W-CDMA modulation, CW)
    - – AWGN source

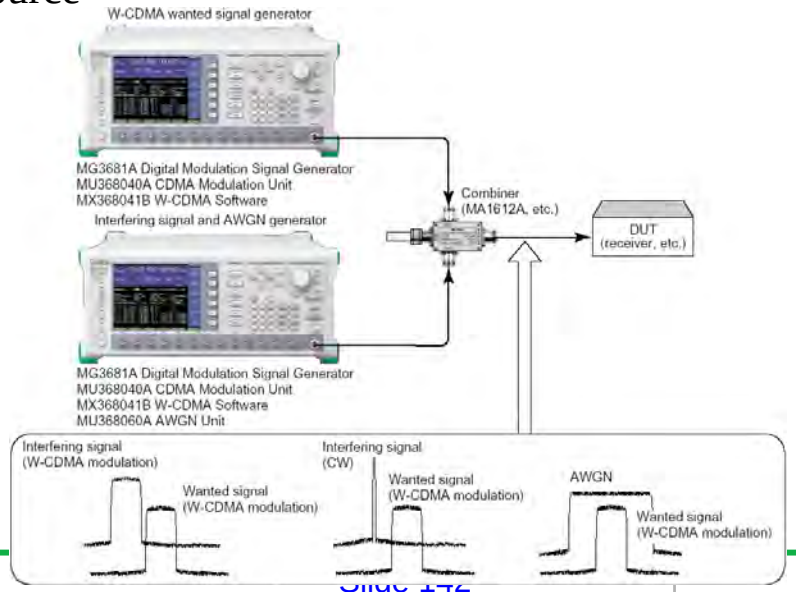
Single unit is performable

change < 10 sec

- **3GPP2(CDMA2000)**
  - » At mounting MX368033A CDMA2000 1xEV-DO Signal Generation Software installed in MU368030A Universal Modulation Unit together...
    - – Wanted signal source (CDMA2000 1xEV-DO modulation)
    - – Interfering signal source (CDMA2000 modulation, CW)
    - – AWGN source

Single unit is performable

change < 10 sec



Ioc bandwidth level

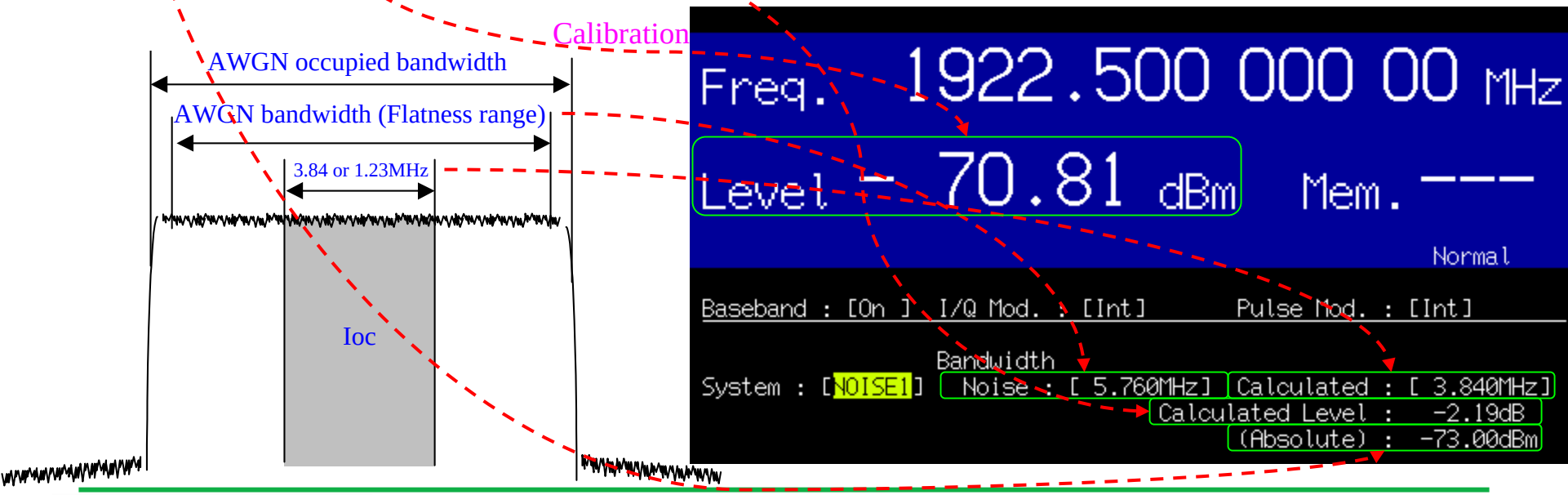
Ioc [dBm] = AWGN level of 3.84MHz(3GPP) or 1.23MHz(3GPP2) bandwidth

- **To measure for high-accuracy**
  - » By spectrum analyzer
    - – Measuring total level (Pt)[dBm]
    - – Measuring 3.84MHz or 1.23MHz bandwidth level (Pb)[dBm]
  - » By power meter
    - – Measuring total level (Pm)[dBm]
  - » Ioc = Pm + (Pb - Pt)

Measuring per frequency

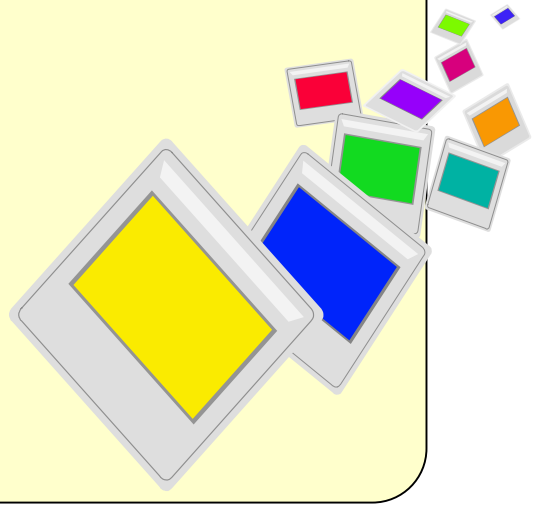
Spectrum analyzer needlessness (accuracy ≤ ±0.6 dB)

Calibration



Application

- Product outline
- Feature
- Application
- Option



- **3GPP**
  - » W-CDMA 3GPP(FDD) 145
  - » GSM/EDGE 186
- **3GPP2**
  - » CDMA2000 1xEV-DO 188
  - » CDMA2000 1X 211
- **ARIB**
  - » PHS 226
  - » PDC 235
- **TIA**
  - » NADC 246

3GPP TS 25.141 (Release 5)
6 Transmitter
7 Receiver
8 Performance requirement

W-CDMA 3GPP(FDD) BS testing

Section	Test	Wanted signal generator	Interfering signal generator	CW generator	AWGN generator	Others
6.4 6.4.2 6.4.3	Output power dynamics Power control steps Power control dynamic range	MG3681A +MU368040A +MX368041B				Code domain analyzer
6.6	Transmit intermodulation		MG3681A +MU368040A +MX368041B (+MG3681A-42)			Spectrum analyzer Circulator
7.2	Reference sensitivity level	MG3681A +MU368040A +MX368041B				
7.3	Dynamic range				+MU368060A	
7.4	Adjacent Channel Selectivity (ACS)		MG3681A +MU368040A +MX368041B			MP1201C BERT
7.5	Blocking characteristics		MG3681A +MU368040A +MX368041B (+MU368010A) (+MX368012A)	MG3692A 20GHz or MG3642A 2.08GHz		MA1612A 3GHz Combiner
7.6	Intermodulation characteristics					
7.8	Verification of the internal BER calculation					
8.2	Demodulation in static propagation conditions				+MU368060A	
8.3	Demodulation of DCH in multipath fading conditions				MG3681A +MU368060A	Fading simulator
8.4	Demodulation of DCH in moving propagation conditions					
8.5	Demodulation of DCH in birth/death propagation conditions					
8.6	Verification of the internal BLER calculation					
8.8 8.8.1 8.8.2 8.8.3 8.8.4	RACH performance RACH preamble detection in static propagation conditions RACH preamble detection in multipath fading case 3 Demodulation of RACH message in static propagation conditions Demodulation of RACH message in multipath fading case 3				(MG3681A) +MU368060A	(Fading simulator)
8.9 8.9.3 8.9.4	CPCH performance Demodulation of RACH message in static propagation conditions Demodulation of RACH message in multipath fading case 3					
8.10	Site Selection Diversity Transmission (SSDT) Mode				+MU368060A	

Transmitter test　　Connection example

Wanted signal generator
MG3681A
+MU368040A+MX368041B

Code domain analyzer
MS8608A/8609A
+MX860801B/860901B

Start trigger

Reference clock

Controller

Power control test

Interfering signal generator
MG3681A
+MU368040A+MX368041B
(+MG3681A-42)

Spectrum analyzer
MS8608A/8609A
+MX860801B/860901B

Circulator

Controller

Transmit intermodulation test

- Controller
  - Launches the Inner loop power control in the possible state by FTM Factory Test Mode control.
  - Launches in the transmitting state by FTM Factory Test Mode control.

Receiver test　Connection example

Interfering signal generator
CW generator
(AWGN generator)
MG3681A
+MU368040A+MX368041B
(+MU368010A+MX368012A)
(+MU368060A)

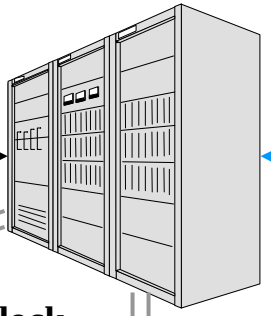
Wanted signal generator
(+ AWGN generator)
MG3681A
+MU368040A+MX368041B
(+MU368060A)

CW generator
(MG3692A)



Combiner
(MA1612A)

Start trigger



Controller

Reference clock

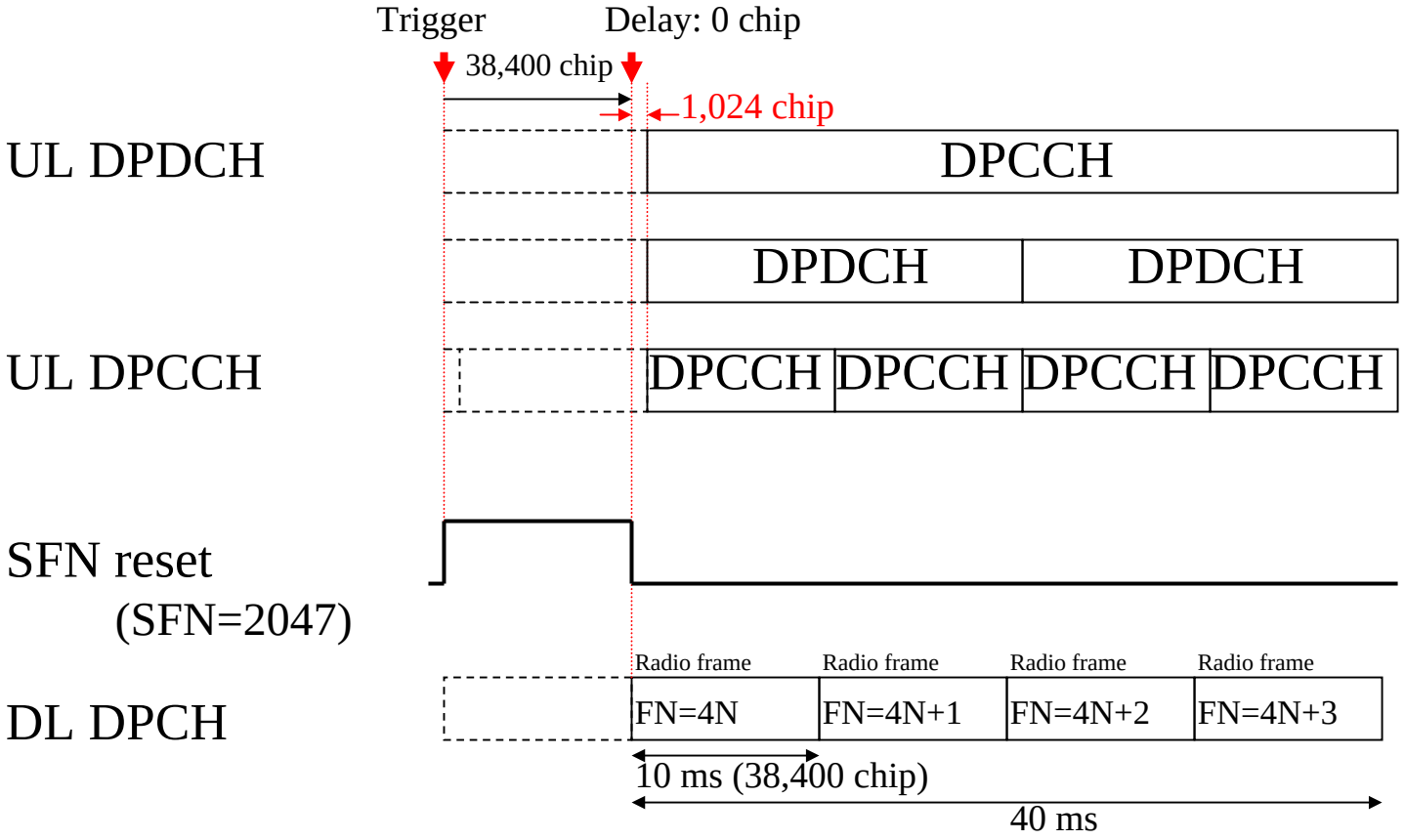
Demoduladed
(DTCH) data　**Clock**

BERT
(MP1201C)

- Start trigger
  - Front panel [Clock/Trig] Input
    - 40 ms × n clock
      e.g. SFN reset timing of Downlink BCHの (2044 frame ×10 ms), BFN timing(4096 frame ×10 ms)
- Reference clock
  Apply only one
  - Front panel [Ref. Clock] Input
    - 3.84 MHz, 2× 3.84 MHz (7.68 MHz), 4× 3.84 MHz (15.36 MHz)
  - Rear panel [10MHz/13MHz Ref] Input
    - 10 MHz, 13 MHz
- Controller
  - Launches UL RMC in the receivable state by FTM Factory Test Mode control.
  - Checks the CRC per demodulated transport block (DTCH) and calculates the BLER.

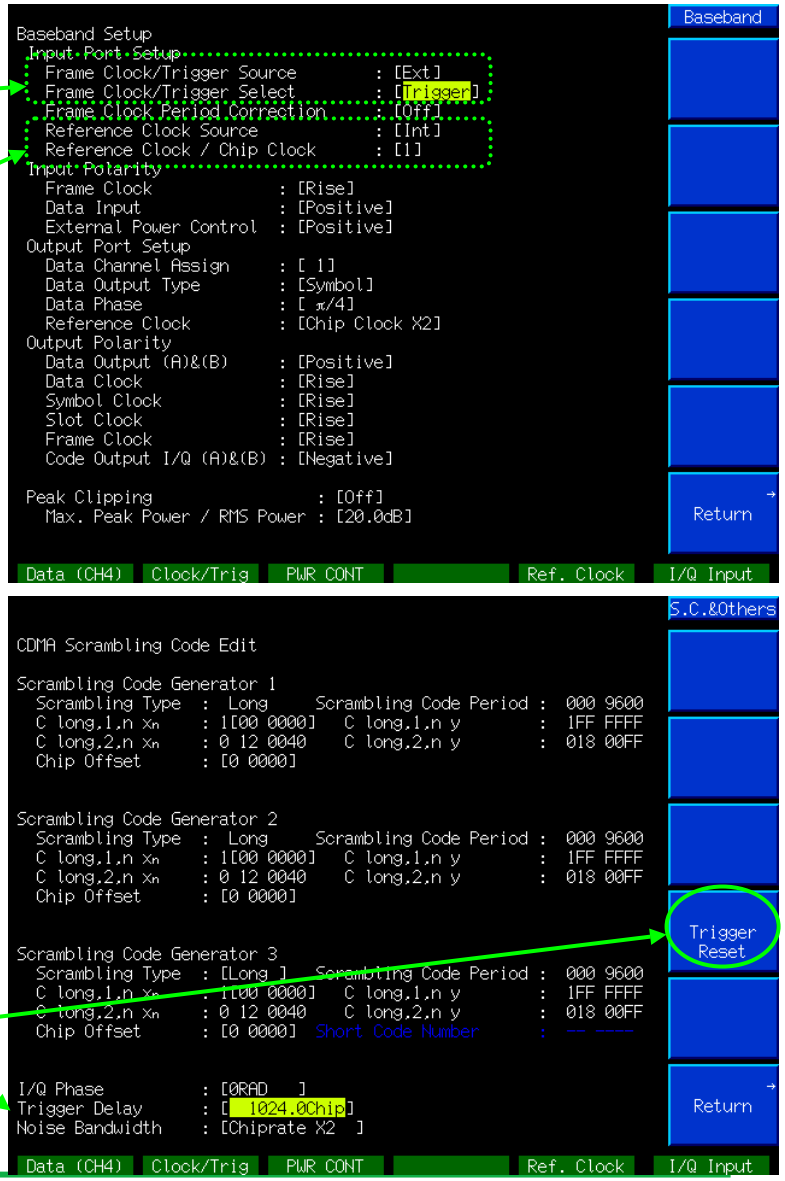
Timing synchronization Setup example

- **Start trigger delay**
  - » Set the timing to which BS can receive UL RMC



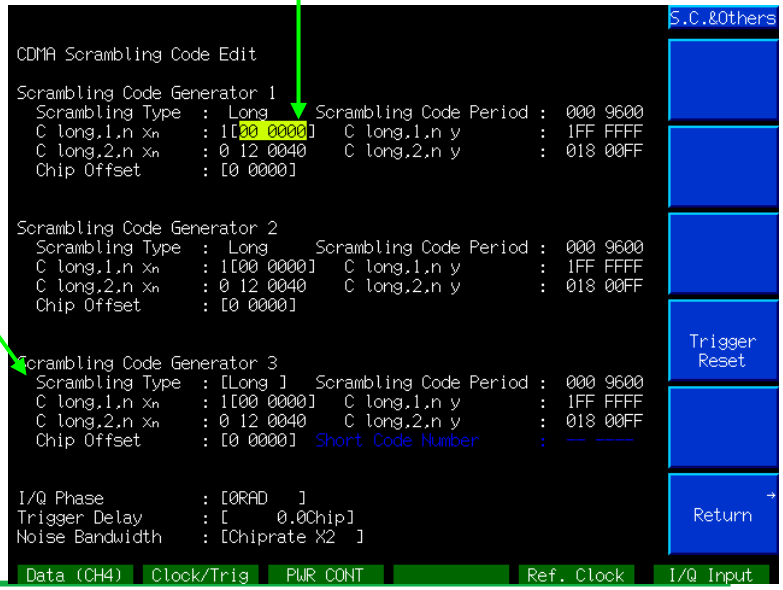
Timing sync. Setup example

- **Setting External Start trigger**
  - » Captures/ Synchronizes the Trigger only once
- **Reference clock:**
  - » [Ref. Clock] Input applicable case
    - – Reference Clock Source : [Ext]
    - – Reference Clock / Chip Clock:
      - [1] at 3.84 MHz
      - [2] at 2× 3.84 MHz
      - [4] at 4× 3.84 MHz
  - » [10MHz/13MHz Ref] Input applicable case
    - – Reference Clock Source : [Int]
- **Start trigger delay**
  - » -38,353.5 ~ +65,536 chip
    1/2 chip resolution
- **Trigger recapture/ synchronization**



Scrambling code sync. Setup example

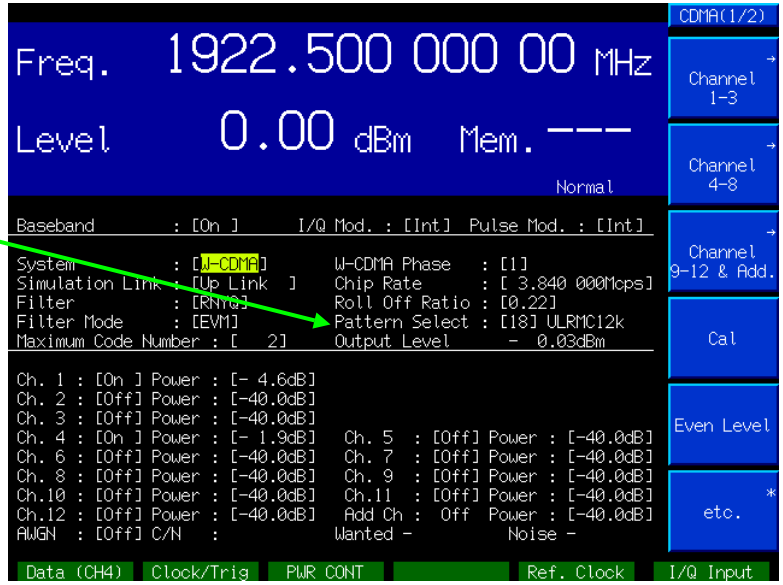
- **Long scrambling code**
  - » 38,400 chip (10 ms) length
    - – Created from two (x_n, y) binary m-sequences of 25 bit length
  - » Applies HPSK modulation at spreading
    - – HPSK: QPSK modulation and π/2BPSK modulation alternate per chip timing.
      - Crest factor is lowered without shifting the phase by 180°.
- **Set $x_n(23) \sim x_n(0)$ receivable by BS in hexadecimal**
  - » $C_{long,2,n}$ shifts $C_{long,1,n}$ by 16,777,232 chip
- **Short scrambling code**
  - » To mitigate the reception processing of BS when applying interference canceler
  - » 256 chip length

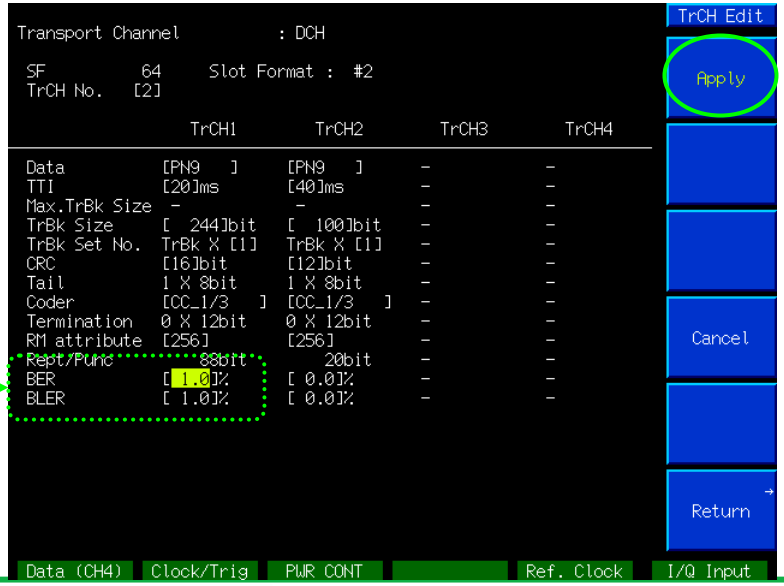


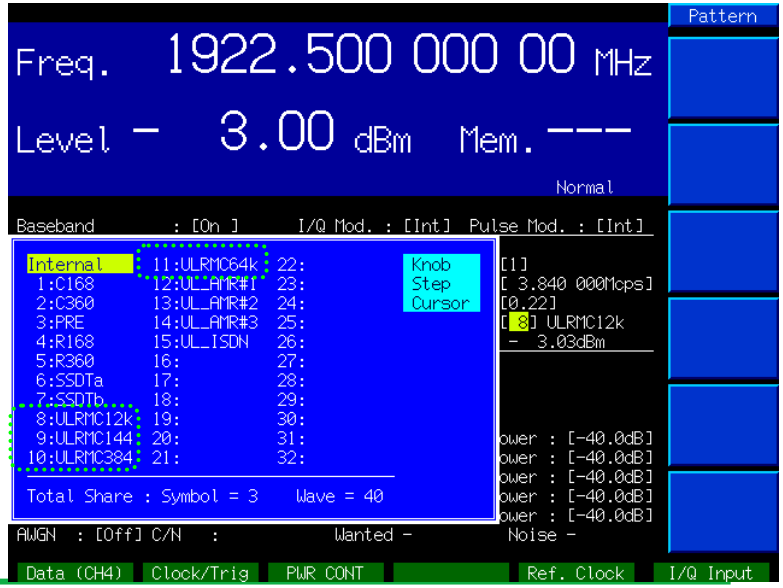
Wanted signal generator Setup example

- **UL RMC 12.2 kbps**
- **UL RMC 64 kbps**
- **UL RMC 144 kbps**
- **UL RMC 384 kbps**

- **Generating the error 1% in DTCH**
  - » Verification of the internal BER/BLER calculation test



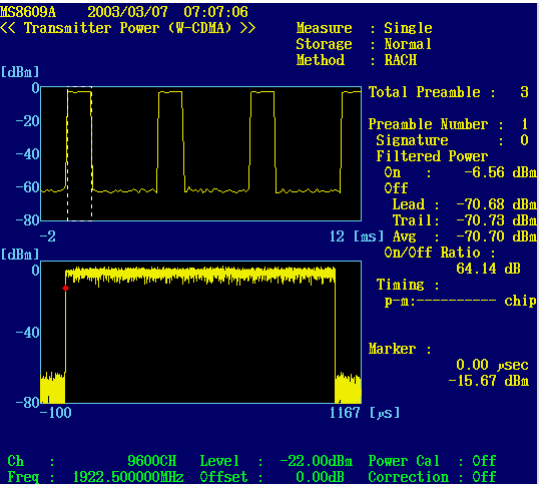


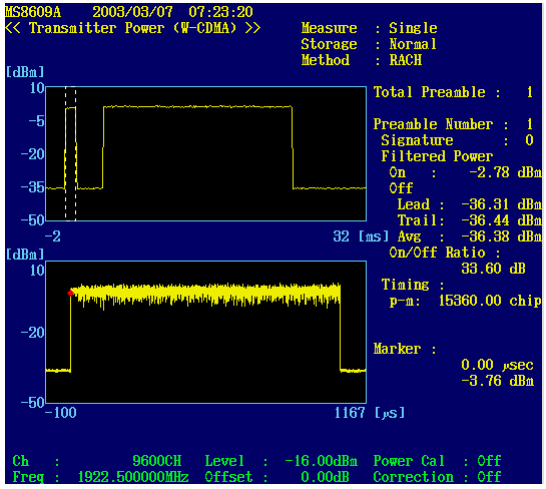


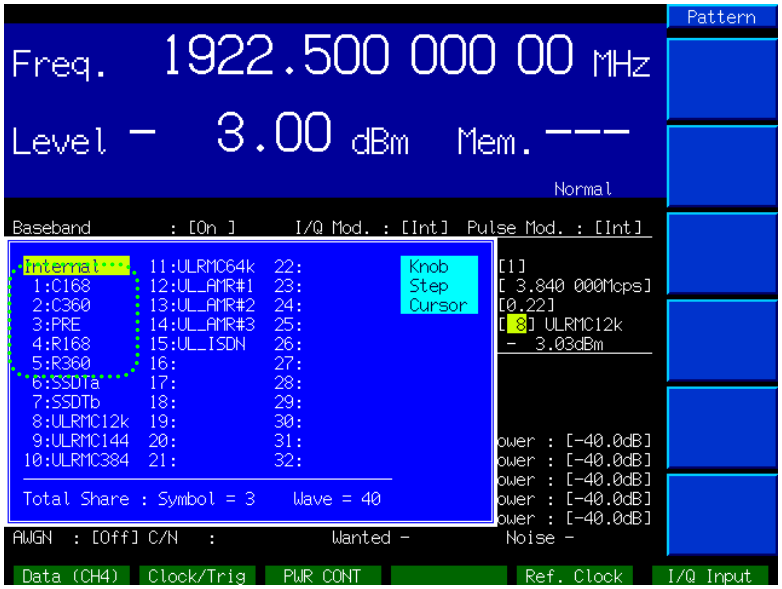
Wanted signal generator Setup example

- **UL RMC RACH**
  - » Preamble

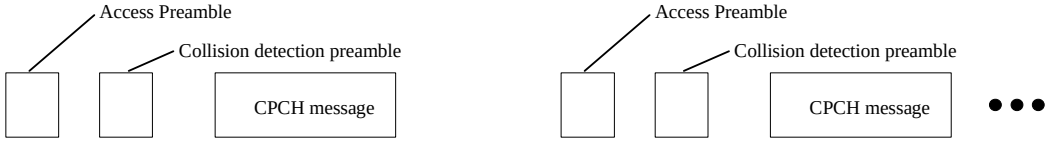
  - » Message
    - – TB size: 168 bits, 360 bits





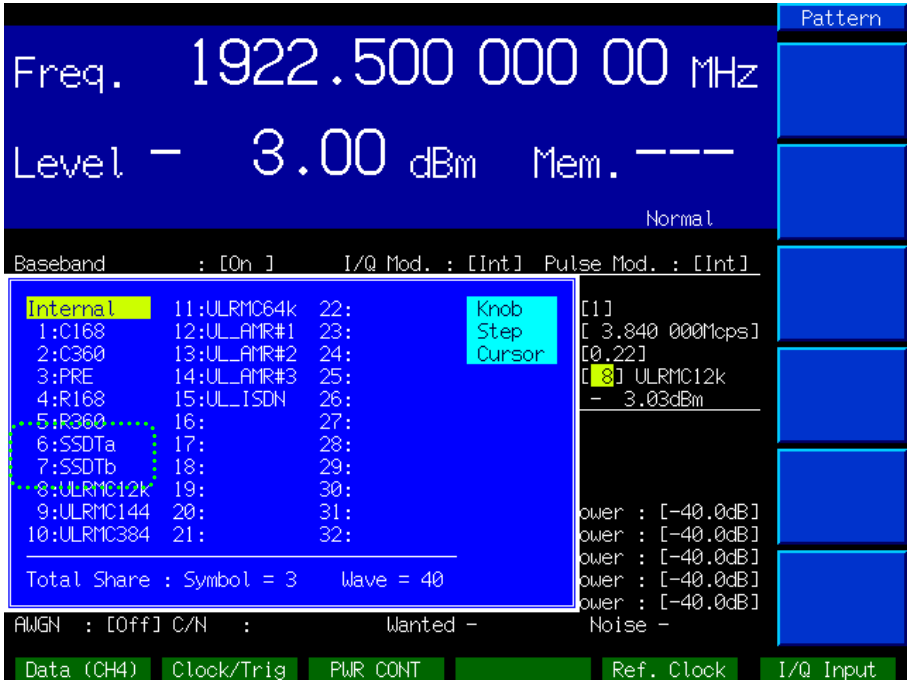


- **UL RMC CPCH**
  - – TB size: 168 bits, 360 bits



Wanted signal generator Setup example

- **UL RMC 12.2 kbps**
  - » SSDT test
    - – Cell ID transmitted by UE: A, B



Wanted signal generator Setup example

- **Set TPC command for Inner loop power control**
  - » 60 TPC command (60 slots) cycle
    - – Power control steps test

      Transmitter power control step tolerance
      - [555 5555 5555 5555] $_{H}$

        0101 0101 ... 0101

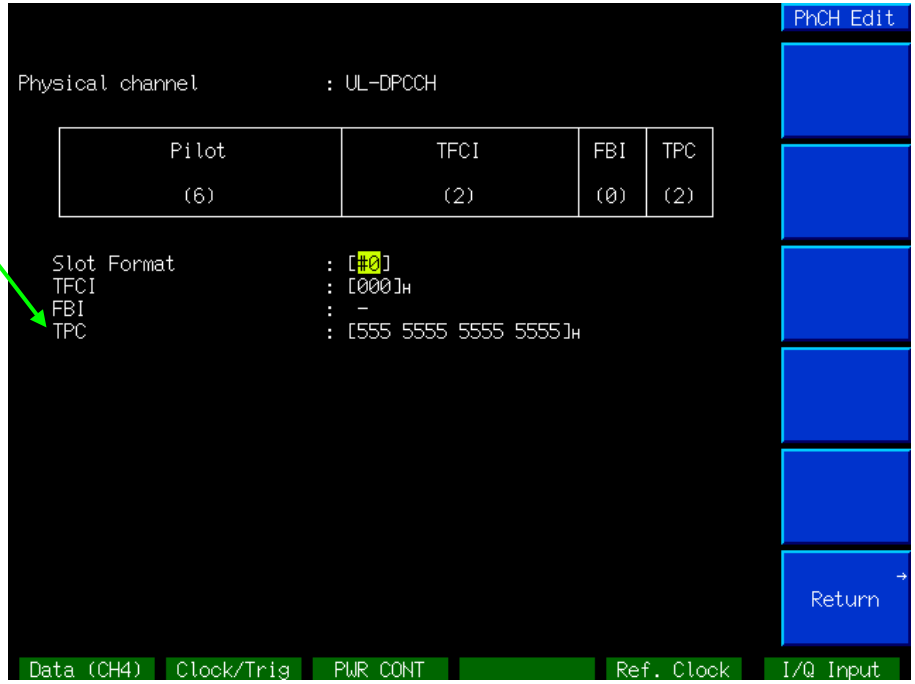
      Transmitter aggregated power control step range
      - [003 FF00 3FF0 03FF] $_{H}$

        0000 0000 0011 1111 1111

        0000 ... 1111
    - – Power control dynamic range test
      - [000 0000 3FFF FFFF] $_{H}$

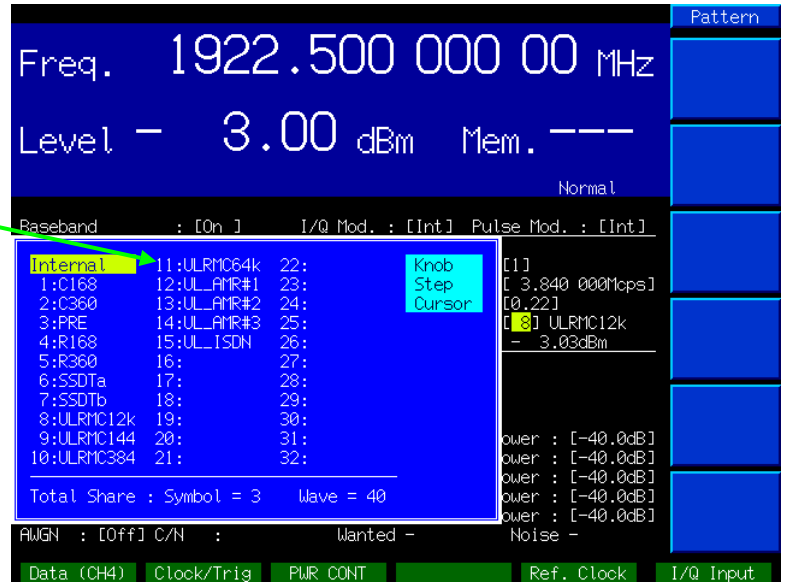
        0000 ... 0011 ... 1111

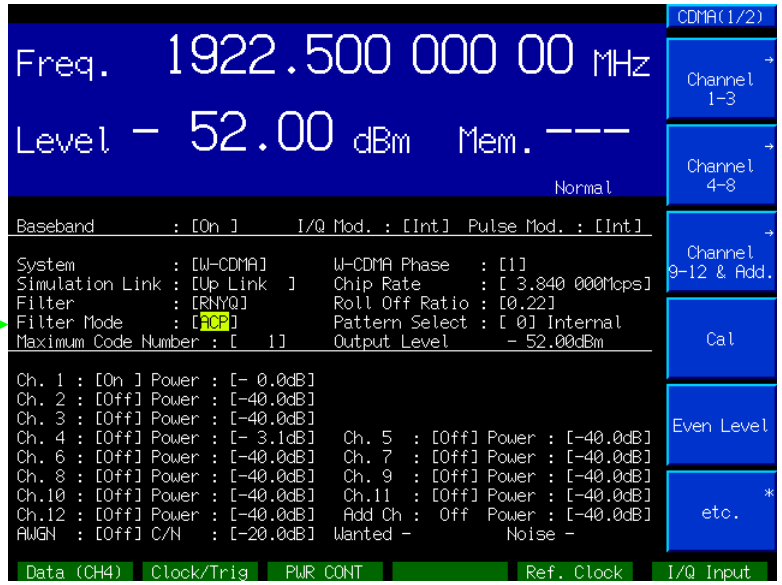
        ($0^{30bits}1^{30bits}$)



Interfering signal generator Setup example

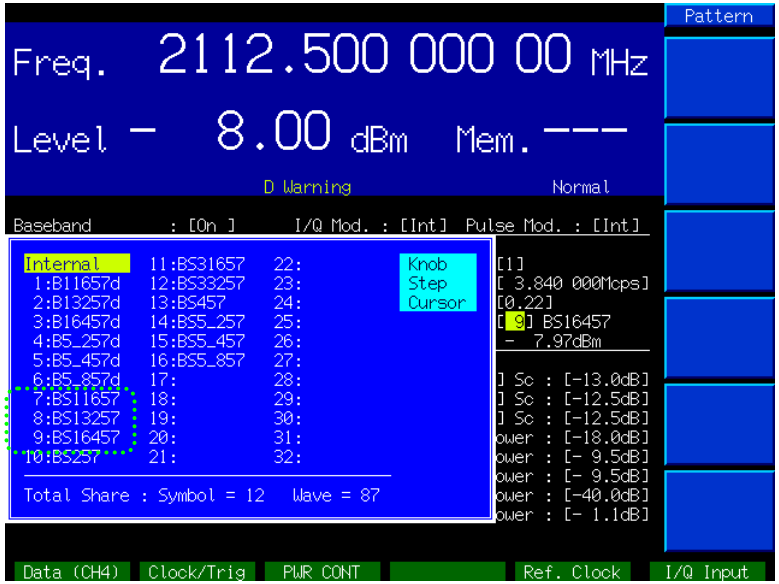
- **W-CDMA**
  - » UL RMC 64 kbps
  - » Set the scrambling code different from wanted signal
    - – [00 0010]
      - in case of Wanted signal: [00 0000]
  - » ACP priority filter



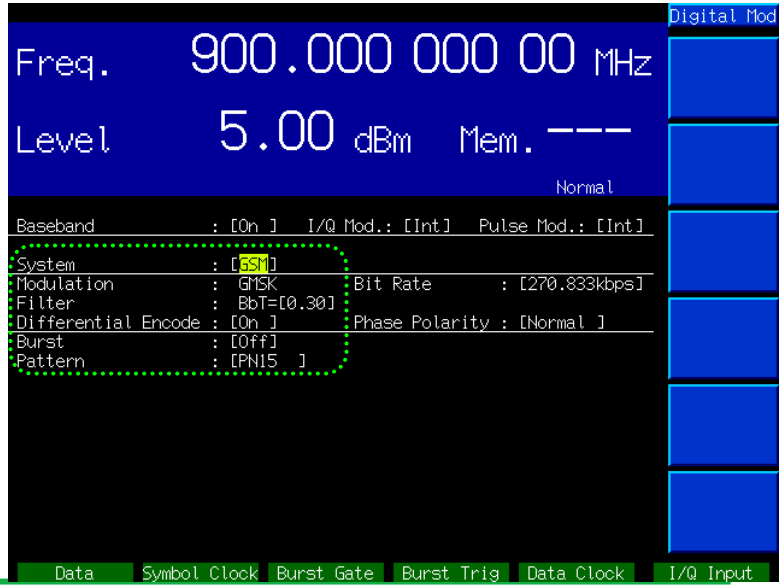


Interfering signal generator Setup example

- **Test Model 1**
  - » Transmit intermodulation test
  - » ACP priority filter



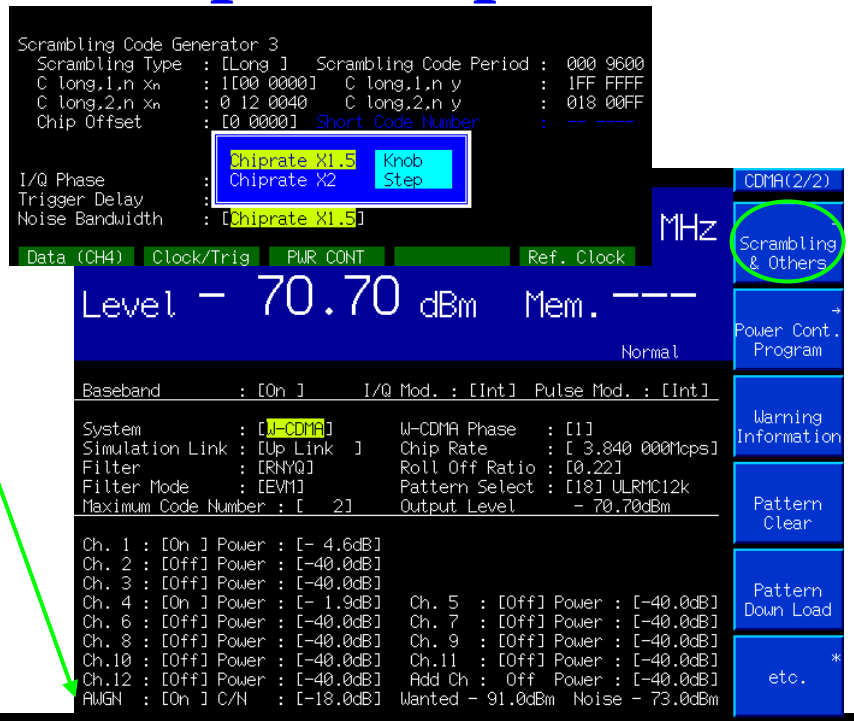
- **GMSK modulation**
  - » Blocking characteristics, Intermodulation characteristics test



AWGN generator Setup example

- **AWGN mixing**
  - » C/N = Wanted signal/AWGN
    - – Dynamic range test
      - C/N: [-16.8dB]
        Wanted -89.8dBm Noise -73.0dBm
    - – Demodulation in static propagation conditions test
      - C/N: [-19.5dB]
        Wanted -103.5dBm Noise -84.0dBm
        (R_b:12.2 kbps, E_b/N_o: 5.5 dB)
        = $10\log_{10}(R_b/3.84\times10^6)+E_b/N_o$

        12.2 kbps: -24.98
        64 kbps: -17.78
        144 kbps: -14.26
        384 kbps: -10



- **AWGN source**
  - » Ioc =
    Total level
    + Bandwidth level

W-CDMA 3GPP(FDD) UE testing

3GPP TS 25.101 (Release 5)
- 6 Transmitter
- 7 Receiver

* TS 34.121 (Release 5)
- * 5 Transmitter
- * 6 Receiver

Section	Test	Wanted signal generator	Interfering signal generator	CW generator	AWGN generator	Others
6.4 6.4.2 6.4.3	Output power dynamics Inner loop power control in the uplink Minimum output power	MG3681A +MU368040A +MX368041B				(Slot) Pwr meter Circulator
7.3	Reference sensitivity level					MP1201C BERT MA1612A 3GHz Combiner
7.4 7.4.1 7.4.2	Maximum input level DPCH HS-PDSCH for 16QAM					
7.5	Adjacent Channel Selectivity (ACS)		MG3681A +MU368040A +MX368041B			
7.6	Blocking characteristics		MG3681A +MU368040A +MX368041B +(MU368010A) +(MX368012A)	MG3692A 20GHz or MG3633A 2.7GHz		
7.7	Spurious response					
7.8	Intermodulation characteristics		MG3681A +MU368040A +MX368041B			

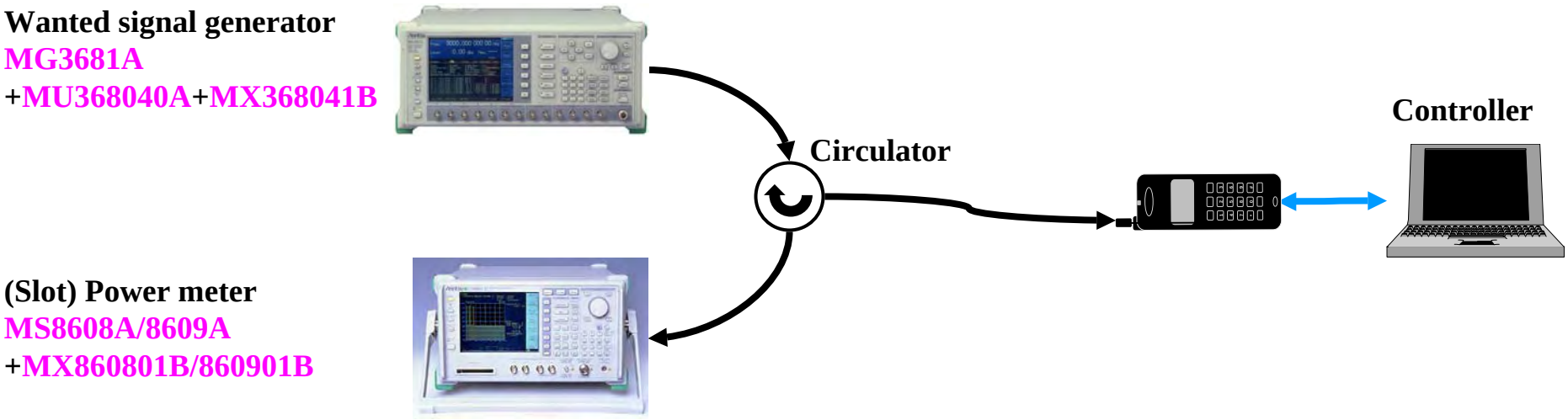
W-CDMA 3GPP(FDD) UE testing

3GPP TS 25.101 (Release 5)
8 Performance requirement
9 Performance requirement (HSDPA)

* TS 34.121 (Release 5)
* 7 Performance requirements

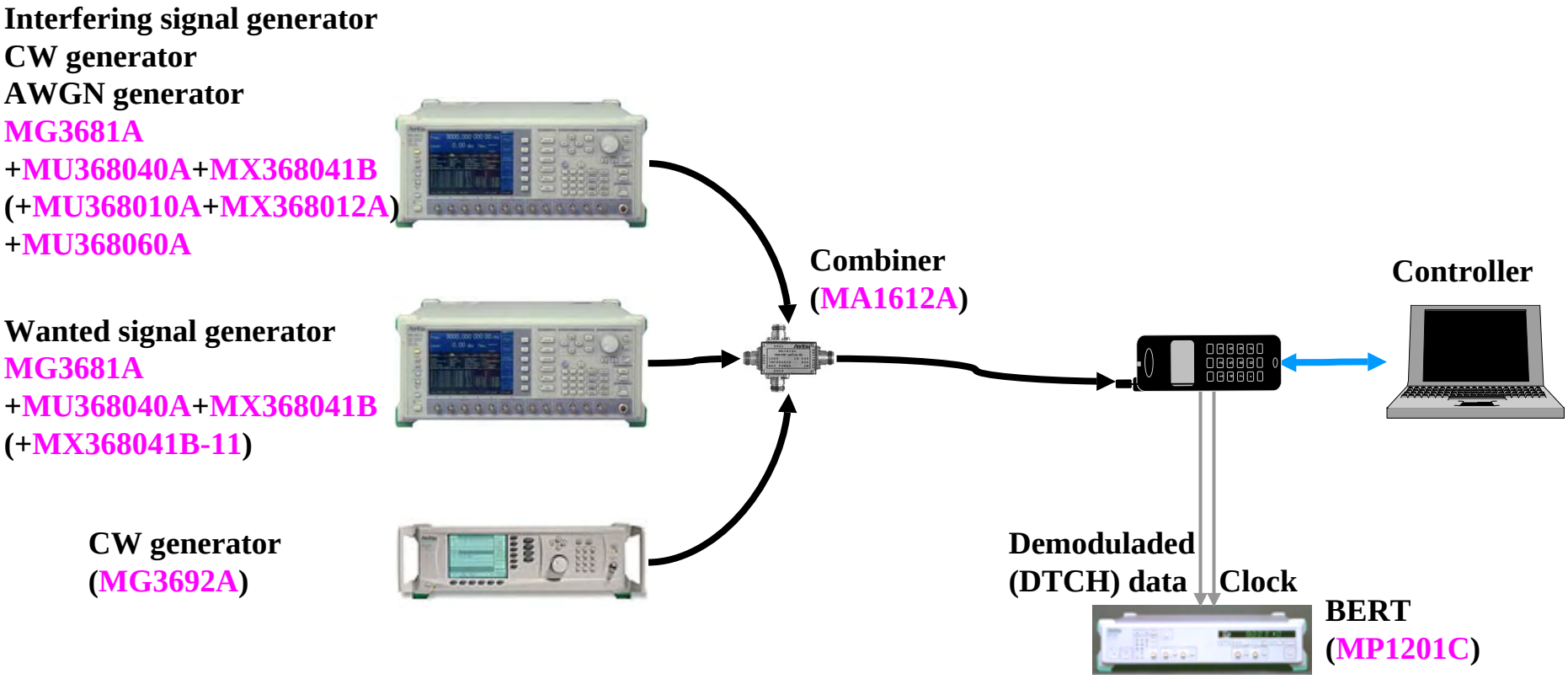
Section	Test	Wanted signal generator	Interfering signal generator	CW generator	AWGN generator	Others
8.2 8.2.3	Demodulation in static propagation conditions Demodulation in Dedicated Channel (DCH)	MG3681A +MU368040A +MX368041B			MG3681A +MU368060A	
8.3	Demodulation of DCH in multi-path fading propagation conditions					MA1612A 3GHz Combiner Fading simulator
8.4	Demodulation of DCH in moving propagation conditions					
8.5	Demodulation of DCH in birth-death propagation conditions					
8.6 8.6.1	Demodulation of DCH in downlink Transmit diversity modes Demodulation of DCH in open-loop transmit diversity modes	MG3681A x2 +MU368040A +MX368041B				
8.9	Downlink compressed mode	MG3681A +MU368040A +MX368041B				(Fading simulator)
8.10	Blind transport format detection					
8.12	Demodulation of Paging Channel					
9.2 9.2.1	Demodulation of HS-DSCH (FRC) Single Link performance					MA1612A 3GHz Combiner
9.3	Reporting of Channel Quality Indicator (CQI)					(Fading simulator)

Transmitter test Connection example



– Controller
  - Launches the Inner loop power control in the possible state by FTM Factory Test Mode control.

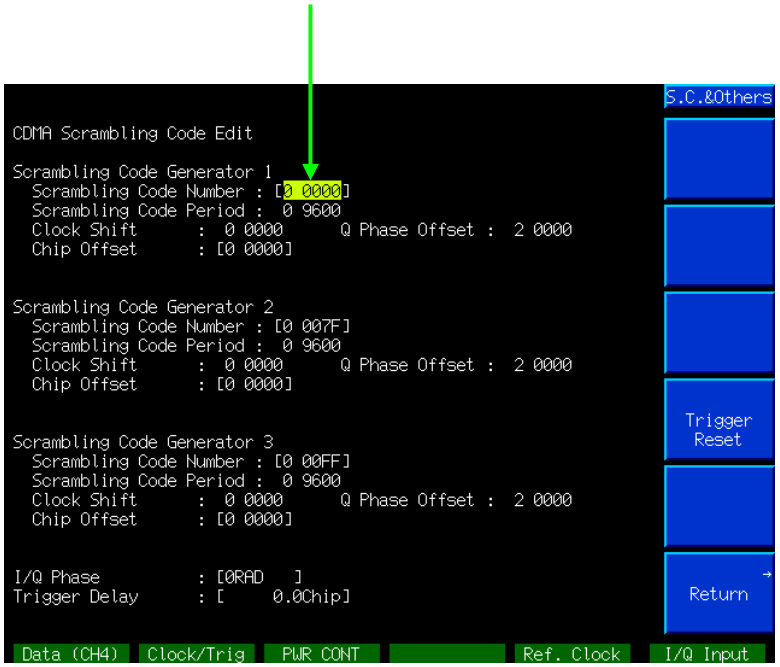
Receiver test Connection example



- Controller
  - Launches DL RMC in receivable state by FTM Factory Test Mode control.
  - Checks the CRC per demodulated transport block (DTCH) and calculates the BLER.

Scrambling code sync. Setup example

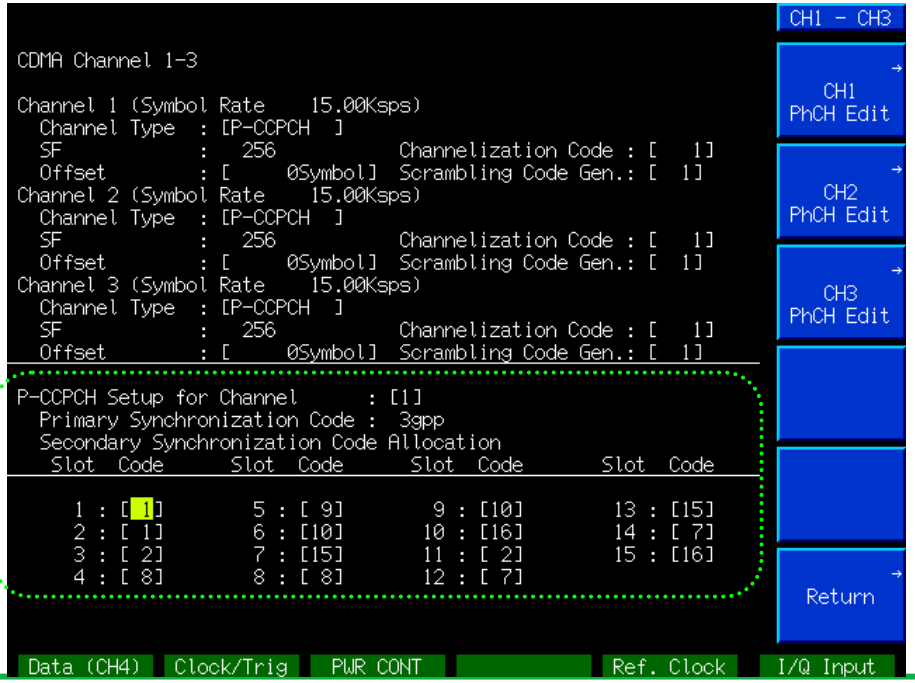
- **Long scrambling code**
  - Created from Gold sequences of 18 bit length
  - » Applies QPSK modulation at spreading
- **Set the Scrambling code receivable by UE in hexadecimal**
  - » 0 ~ 3FFFF (2^{18}-1)
    - Primary scrambling code: $16 \times (8 \times j + k)$ = 0 ~ 01FF0
    - Secondary scrambling code: $16 \times (8 \times j + k) + (1\sim15)$
      - 512 codes (i= 0 ~ 511)
        - 64 Scrambling code group j= 0 ~ 63
        - 8 Primary scrambling code k= 0 ~ 7



Synchronization code sync. Setup example

Applicable codes for SCH spreading modulation

- **When scrambling code group (j) was changed...**
  Set in reference to 3GPP TS 25.213 5.2.3.2
  Table 4: Allocation of SSCs for secondary SCH
  - » Due to the pair with SSC Secondary Synchronisation Code allocation for S-SCH.



For reference: 3GPP TS 25.213 (Release 5) Table 4

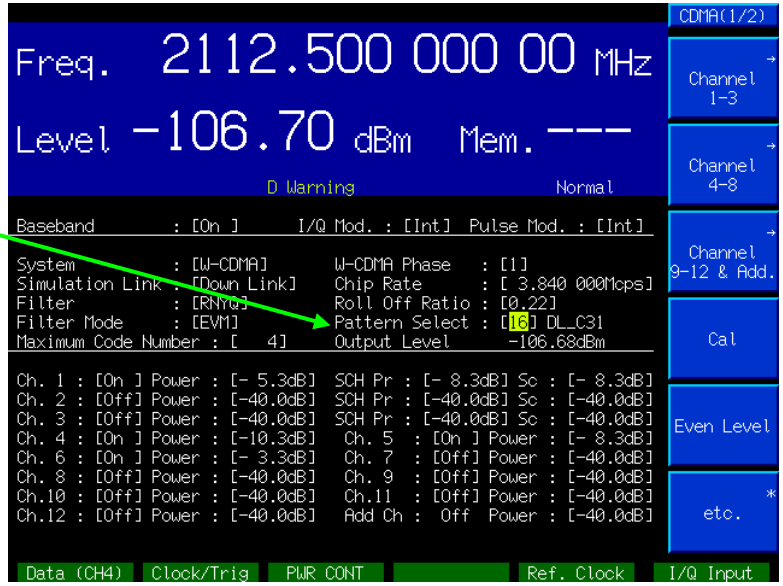
Group 0: Default setting

Scrambling Code Group	slot number														
	#0	#1	#2	#3	#4	#5	#6	#7	#8	#9	#10	#11	#12	#13	#14
Group 0	1	1	2	8	9	10	15	8	10	16	2	7	15	7	16
Group 1	1	1	5	16	7	3	14	16	3	10	5	12	14	12	10
Group 2	1	2	1	15	5	5	12	16	6	11	2	16	11	15	12
Group 3	1	2	3	1	8	6	5	2	5	8	4	4	6	3	7
Group 4	1	2	16	6	6	11	15	5	12	1	15	12	16	11	2
Group 5	1	3	4	7	4	1	5	5	3	6	2	8	7	6	8
Group 6	1	4	11	3	4	10	9	2	11	2	10	12	12	9	3
Group 7	1	5	6	6	14	9	10	2	13	9	2	5	14	1	13
Group 8	1	6	10	10	4	11	7	13	16	11	13	6	4	1	16
Group 9	1	6	13	2	14	2	6	5	5	13	10	9	1	14	10
Group 10	1	7	8	5	7	2	4	3	8	3	2	6	6	4	5
Group 11	1	7	10	9	16	7	9	15	1	8	16	8	15	2	2
Group 12	1	8	12	9	9	4	13	16	5	1	13	5	12	4	8
Group 13	1	8	14	10	14	1	15	15	8	5	11	4	10	5	4
Group 14	1	9	2	15	15	16	10	7	8	1	10	8	2	16	9
Group 15	1	9	15	6	16	2	13	14	10	11	7	4	5	12	3
Group 16	1	10	9	11	15	7	6	4	16	5	2	12	13	3	14
Group 17	1	11	14	4	13	2	9	10	12	16	8	5	3	15	6
Group 18	1	12	12	13	14	7	2	8	14	2	1	13	11	8	11
Group 19	1	12	15	5	4	14	3	16	7	8	6	2	10	11	13
Group 20	1	15	4	3	7	6	10	13	12	5	14	16	8	2	11
Group 21	1	16	3	12	11	9	13	5	8	2	14	7	4	10	15
Group 22	2	2	5	10	16	11	3	10	11	8	5	13	3	13	8
Group 23	2	2	12	3	15	5	8	3	5	14	12	9	8	9	14
Group 24	2	3	6	16	12	16	3	13	13	6	7	9	2	12	7
Group 25	2	3	8	2	9	15	14	3	14	9	5	5	15	8	12
Group 26	2	4	7	9	5	4	9	11	2	14	5	14	11	16	16
Group 27	2	4	13	12	12	7	15	10	5	2	15	5	13	7	4
Group 28	2	5	9	9	3	12	8	14	15	12	14	5	3	2	15
Group 29	2	5	11	7	2	11	9	4	16	7	16	9	14	14	4
Group 30	2	6	2	13	3	3	12	9	7	16	6	9	16	13	12
Group 31	2	6	9	7	7	16	13	3	12	2	13	12	9	16	6

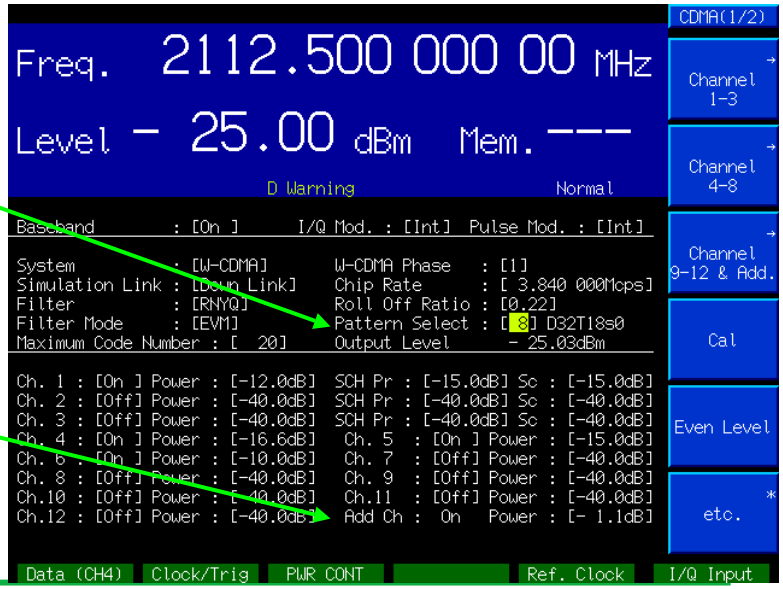
Scrambling Code Group	slot number														
	#0	#1	#2	#3	#4	#5	#6	#7	#8	#9	#10	#11	#12	#13	#14
Group 32	2	7	12	15	2	12	4	10	13	15	13	4	5	5	10
Group 33	2	7	14	16	5	9	2	9	16	11	11	5	7	4	14
Group 34	2	8	5	12	5	2	14	14	8	15	3	9	12	15	9
Group 35	2	9	13	4	2	13	8	11	6	4	6	8	15	15	11
Group 36	2	10	3	2	13	16	8	10	8	13	11	11	16	3	5
Group 37	2	11	15	3	11	6	14	10	15	10	6	7	7	14	3
Group 38	2	16	4	5	16	14	7	11	4	11	14	9	9	7	5
Group 39	3	3	4	6	11	12	13	6	12	14	4	5	13	5	14
Group 40	3	3	6	5	16	9	15	5	9	10	6	4	15	4	10
Group 41	3	4	5	14	4	6	12	13	5	13	6	11	11	12	14
Group 42	3	4	9	16	10	4	16	15	3	5	10	5	15	6	6
Group 43	3	4	16	10	5	10	4	9	9	16	15	6	3	5	15
Group 44	3	5	12	11	14	5	11	13	3	6	14	6	13	4	4
Group 45	3	6	4	10	6	5	9	15	4	15	5	16	16	9	10
Group 46	3	7	8	8	16	11	12	4	15	11	4	7	16	3	15
Group 47	3	7	16	11	4	15	3	15	11	12	12	4	7	8	16
Group 48	3	8	7	15	4	8	15	12	3	16	4	16	12	11	11
Group 49	3	8	15	4	16	4	8	7	7	15	12	11	3	16	12
Group 50	3	10	10	15	16	5	4	6	16	4	3	15	9	6	9
Group 51	3	13	11	5	4	12	4	11	6	6	5	3	14	13	12
Group 52	3	14	7	9	14	10	13	8	7	8	10	4	4	13	9
Group 53	5	5	8	14	16	13	6	14	13	7	8	15	6	15	7
Group 54	5	6	11	7	10	8	5	8	7	12	12	10	6	9	11
Group 55	5	6	13	8	13	5	7	7	6	16	14	15	8	16	15
Group 56	5	7	9	10	7	11	6	12	9	12	11	8	8	6	10
Group 57	5	9	6	8	10	9	8	12	5	11	10	11	12	7	7
Group 58	5	10	10	12	8	11	9	7	8	9	5	12	6	7	6
Group 59	5	10	12	6	5	12	8	9	7	6	7	8	11	11	9
Group 60	5	13	15	15	14	8	6	7	16	8	7	13	14	5	16
Group 61	9	10	13	10	11	15	15	9	16	12	14	13	16	14	11
Group 62	9	11	12	15	12	9	13	13	11	14	10	16	15	14	16
Group 63	9	12	10	15	13	14	9	14	15	11	11	13	12	16	10

Wanted signal generator Setup example

- **DL RMC 12.2 kbps**
  - » Receiver test



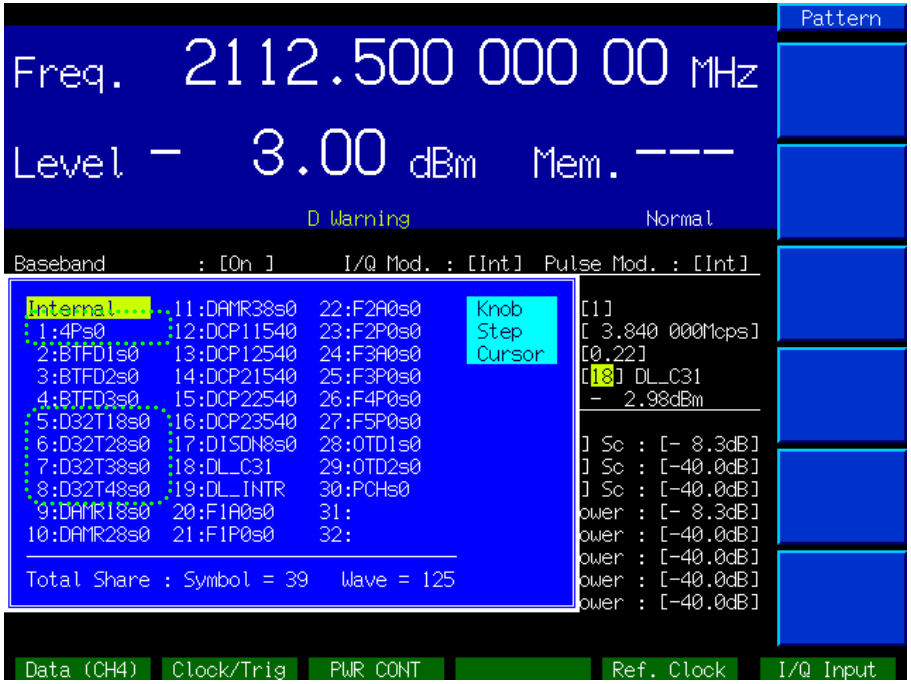
- **DL RMC 12.2 kbps**
  - » Maximum input level (DPCH), Performance requirement test
    - – OCNS multiplexing



Wanted signal generator Setup example

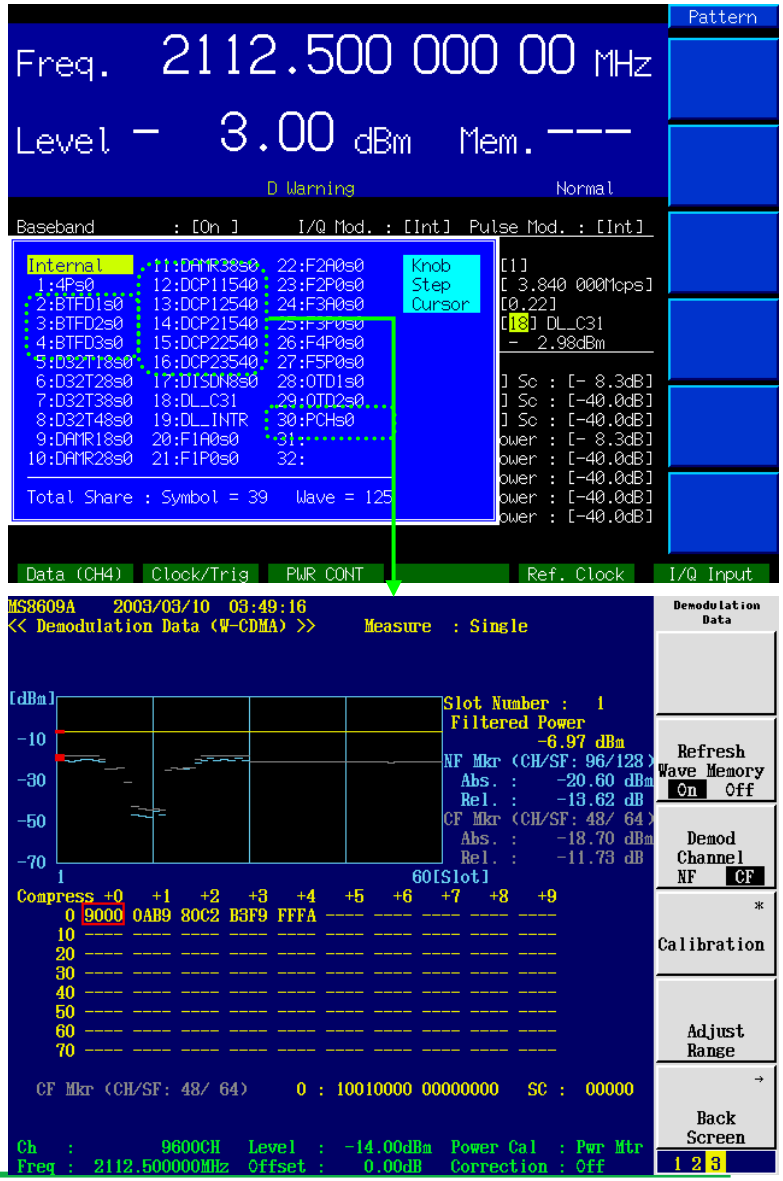
- **DL RMC 12.2 kbps**
- **DL RMC 64 kbps**
- **DL RMC 144 kbps**
- **DL RMC 384 kbps**
  - » Performance requirement test

- **DL RMC 12.2 kbps DPCCH with 4 pilot bits as phase reference**
  - » Demodulation of DCH in multi-path fading propagation conditions (Case 7) Test 21~25 test



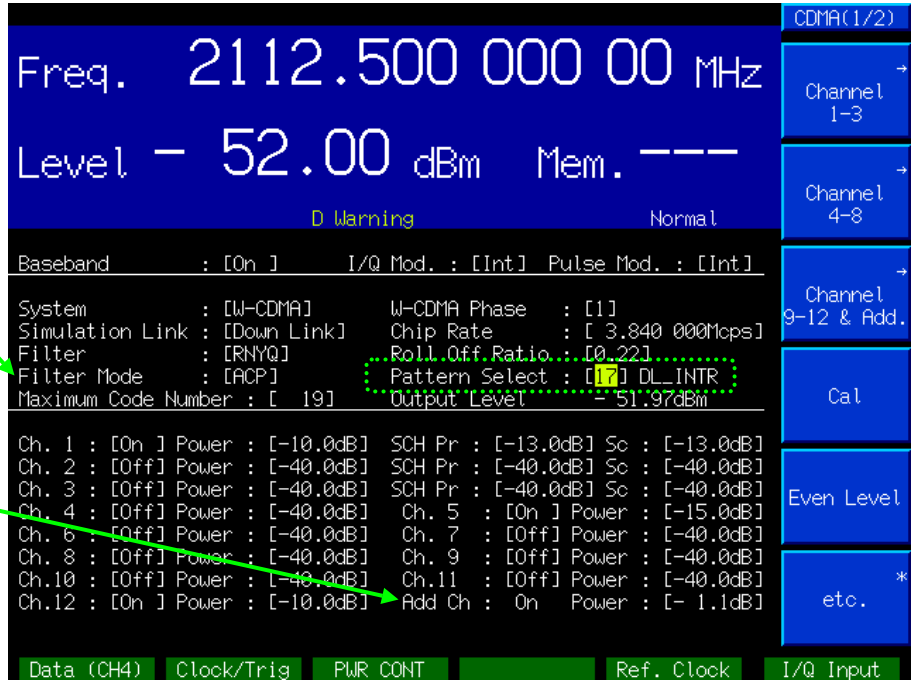
Wanted signal generator Setup example

- **DL compressed mode**
  - » Downlink compressed mode test
    - – Test 1,2: Reference pattern 1 Set 1
      - DL SF/2 (Spreading factor reduction)
    - – Test 3,4: Reference pattern 1 Set 2
      - DL Puncturing
    - – Reference pattern 2 Set 1
    - – Reference pattern 2 Set 2
      - DL SF/2 (Spreading factor reduction)
    - – Reference pattern 2 Set 3
      - DL Puncturing
- **DL RMC BTFD**
  - » Blind transport format detection test
    - – Test 1,4: 12.2 kbps (Rate 1)
    - – Test 2,5: 7.95 kbps (Rate 2)
    - – Test 3,6: 1.95 kbps (Rate 3)
- **DL PCH**
  - » Demodulation of Paging Channel test



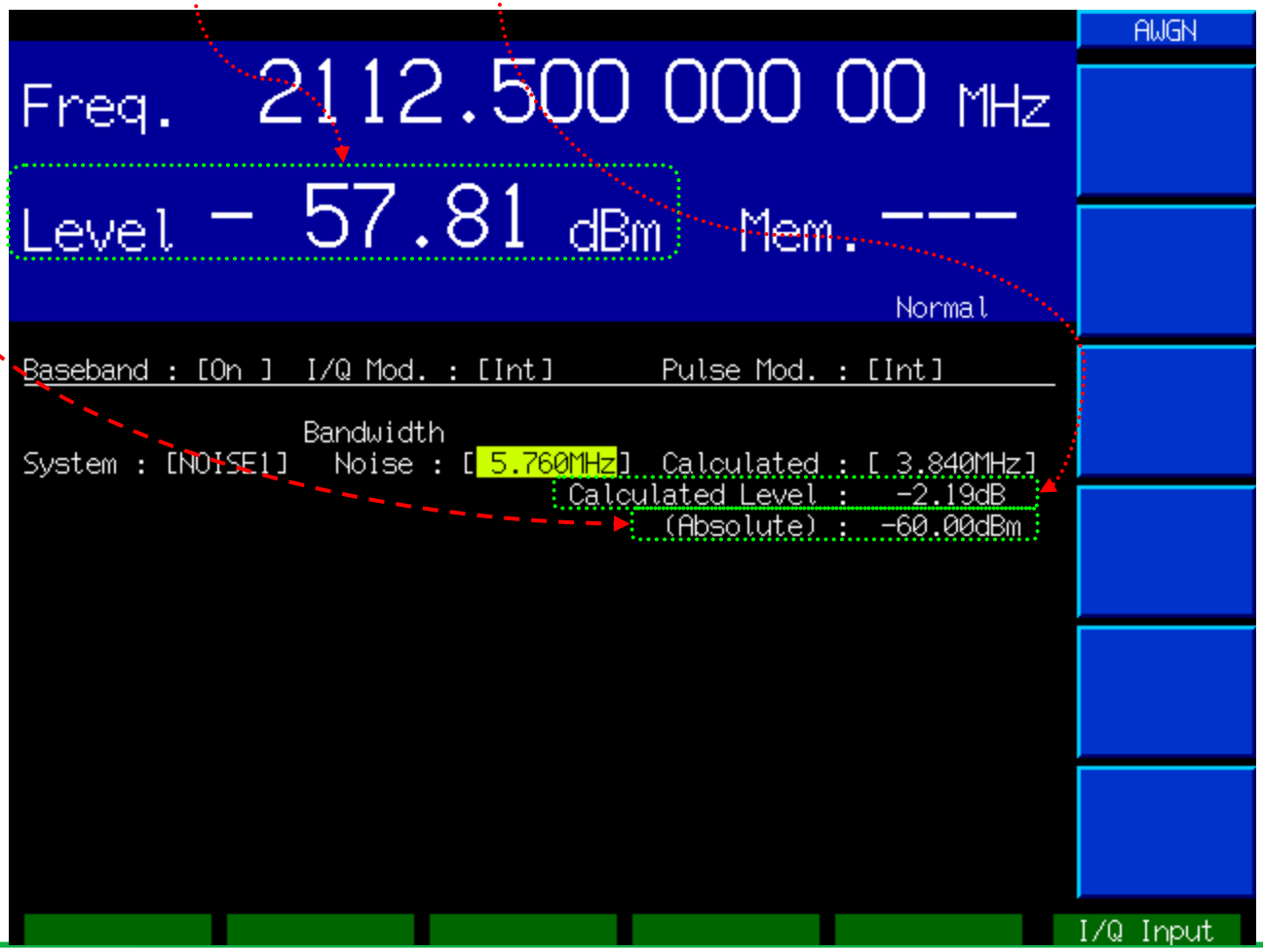
Interfering signal generator Setup example

- **ACP priority filter**
  - » OCNS multiplexing

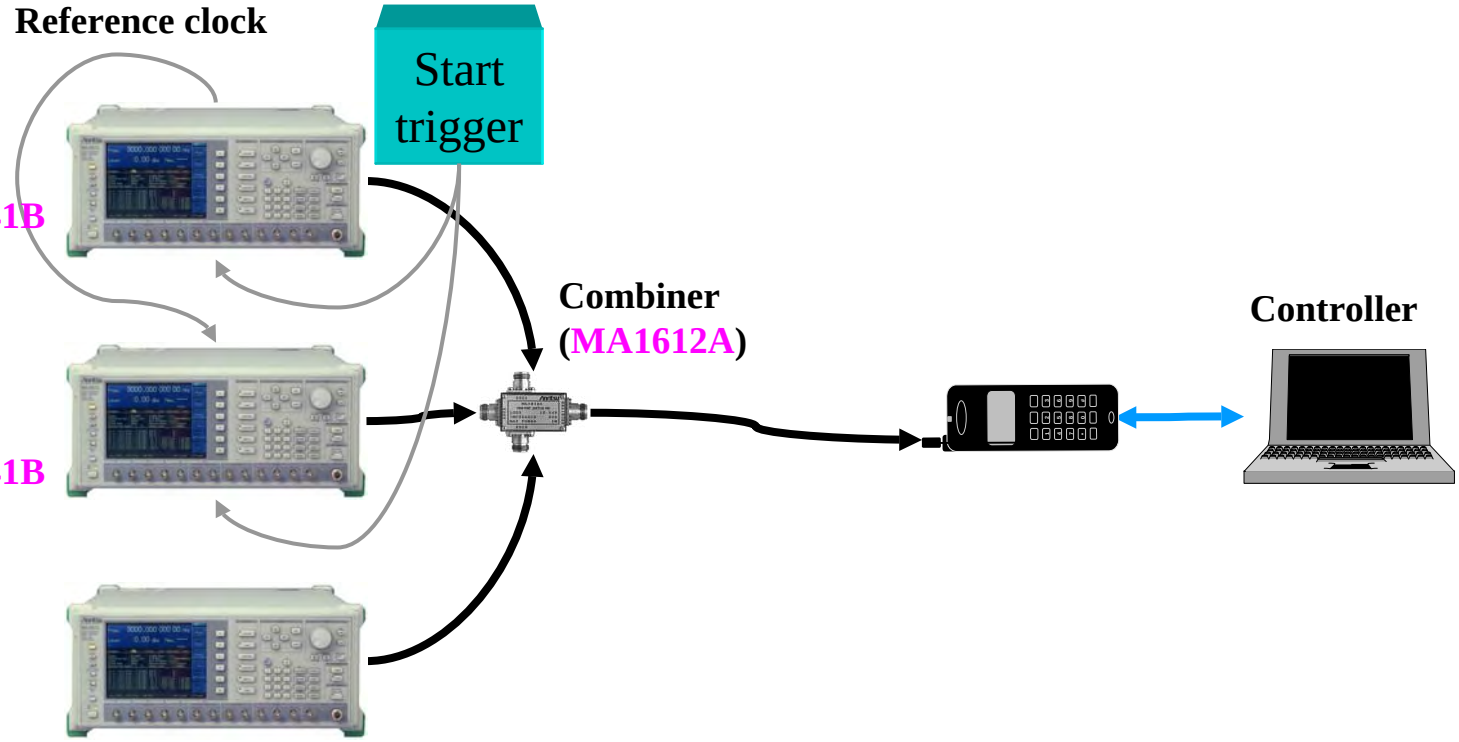


AWGN generator Setup example

- **AWGN source**
  - » Ioc = Total level + Bandwidth level



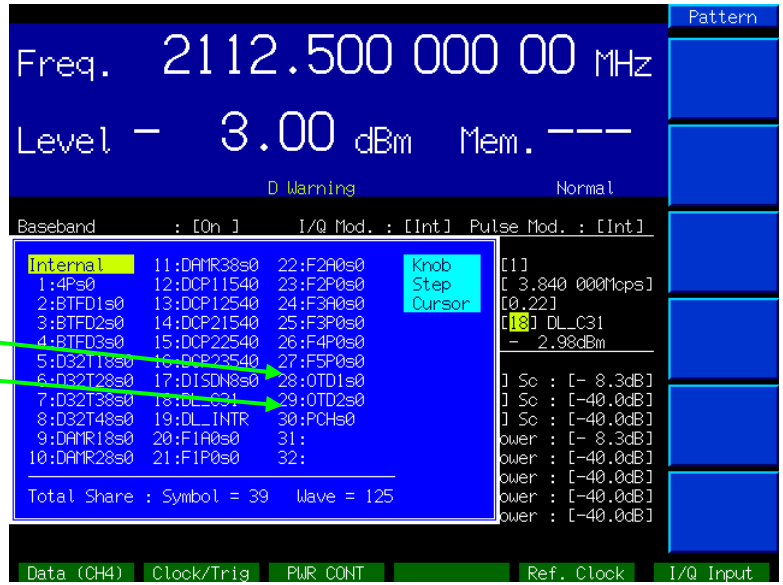
Open-loop TX Diversity mode test Connection example

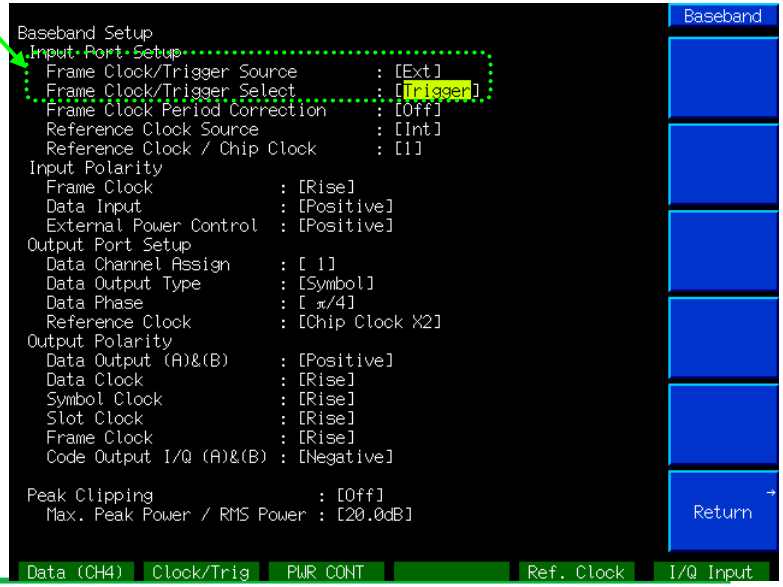


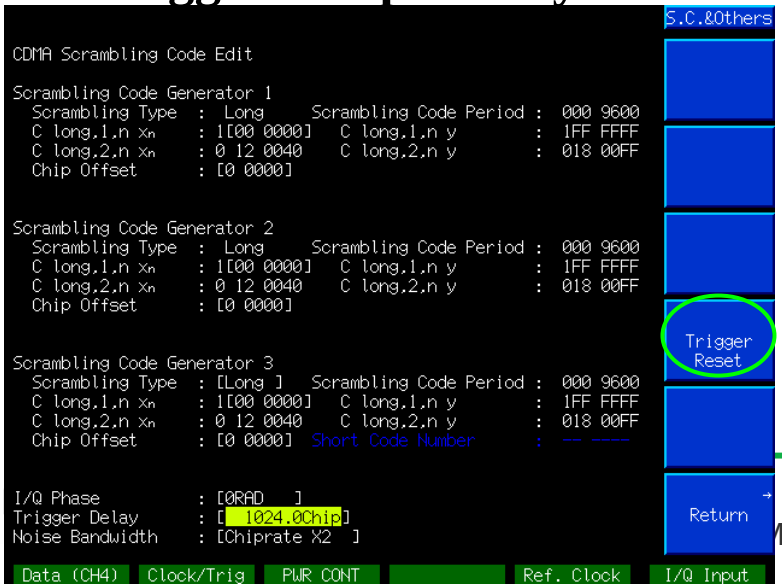
- Start trigger
  - Front panel [Clock/Trig] Input
- Reference clock
  - Rear panel [10MHz Buff] Output
  - Rear panel [10MHz/13MHz Ref] Input
- Controller
  - Launches DL RMC in receivable state by FTM Factory Test Mode control.
  - Checks the CRC per demodulated transport block (DTCH) and calculates the BLER.

Wanted signal generator Setup example

- **DL RMC 12.2 kbps**
  - » Demodulation of DCH in open-loop Transmit diversity mode test
    - – Antenna 1
    - – Antenna 2
- **Setting External Start trigger**
  - » Captures/ Synchronizes the Trigger only once
- **Trigger recapture/ synchronization**

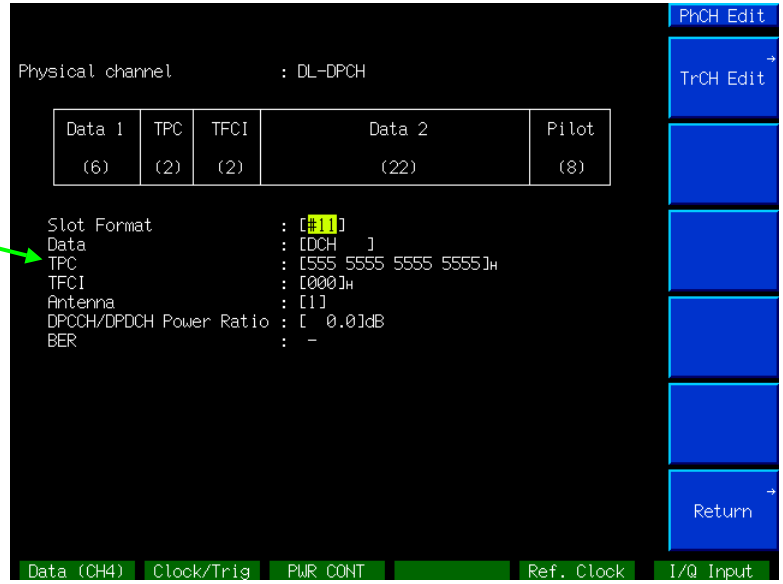






Wanted signal generator Setup example

- **Set TPC command for Inner loop power control**
  - » 60 TPC command (60 slots) cycle
    - – Step A (1 dB step {0})
      - [82A BE82 ABE8 2ABE] $_H$
        1000 0010 1010 1011 1110 ...
    - – Step B (1 dB step {0,0,0,0,+1})
      - [FFF FFFF FFFF FFFF] $_H$
        1111 1111 1111 ...
    - – Step C (1 dB step {0,0,0,0,-1})
      - [000 0000 0000 0000] $_H$
        0000 0000 0000 ...
    - – Step D (1 dB step {+1})
      - [FFF FFFF FFFF FFFF] $_H$
        1111 1111 1111 ...
    - – Step E (1 dB step {-1})
      - [000 0000 0000 0000] $_H$
        0000 0000 0000 ...
    - – Step F (1 dB step {+1})
      - [FFF FFFF FFFF FFFF] $_H$
        1111 1111 1111 ...



- – Step G (2 dB step {-1})
  - [000 0000 0000 0000] $_H$
    0000 0000 0000 ...
- – Step F (2 dB step {+1})
  - [FFF FFFF FFFF FFFF] $_H$
    1111 1111 1111 ...

- – Minimum output power test
  - [000 0000 0000 0000] $_H$
    0000 0000 0000 ...

HSDPA demodulation test Connection example

Wanted signal generator
MG3681A
+MU368040A+MX368041B
+MX368041B-11

Signal analyzer
(MS8600/MS2680)

RF

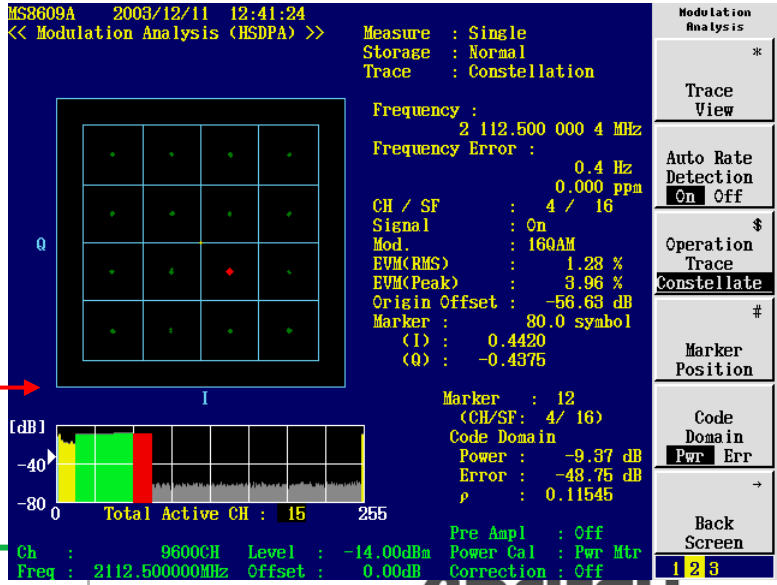
RX module (Demodulator)

I/Q

– EVM test
  • HS-PDSCH, DPCH, ...

Table C.8: Downlink physical channels for HSDPA receiver testing for Single Link performance.

Physical Channel	Parameter	Value	Note
P-CPICH	P-CPICH_Ec/Ior	-10dB	
P-CCPCH	P-CCPCH_Ec/Ior	-12dB	Mean power level is shared with SCH.
SCH	SCH_Ec/Ior	-12dB	Mean power level is shared with P-CCPCH – SCH includes P- and S-SCH, with power split between both. P-SCH code is S_dl,0 as per TS25.213 S-SCH pattern is scrambling code group 0
PICH	PICH_Ec/Ior	-15dB	
DPCH	DPCH_Ec/Ior	Test-specific	12.2 kbps DL reference measurement channel as defined in Annex A.3.1
HS-SCCH_1	HS-SCCH_Ec/Ior	Test-specific	Specifies fraction of Node-B radiated power transmitted when TTI is active (i.e. due to minimum inter-TTI interval).
HS-SCCH_2	HS-SCCH_Ec/Ior	DTX'd	No signalling scheduled, or power radiated, on this HS-SCCH, but signalled to the UE as present.
HS-SCCH_3	HS-SCCH_Ec/Ior	DTX'd	As HS-SCCH_2.
HS-SCCH_4	HS-SCCH_Ec/Ior	DTX'd	As HS-SCCH_2.
HS-PDSCH	HS-PDSCH_Ec/Ior	Test-specific	.
OCNS		Necessary power so that total transmit power spectral density of Node B (Ior) adds to one	OCNS interference consists of 6 dedicated data channels as specified in table C.12.



HSDPA Baseband test Connection example

Wanted signal generator
MG3681A
+MG3681A-11
+MU368040A+MX368041B
+MX368041B-11

I/Q

A/D

Baseband module

Controller

- Inf. Bit
  - PN15
    - Reset to initial value per subframe
      - All subframes are the same data

- Decoding test
  - Inf. Bit checking
- BLER test
  - CRC checking

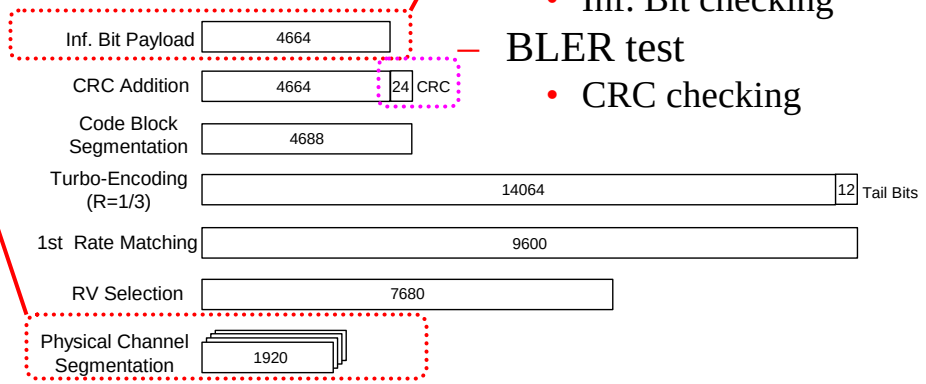
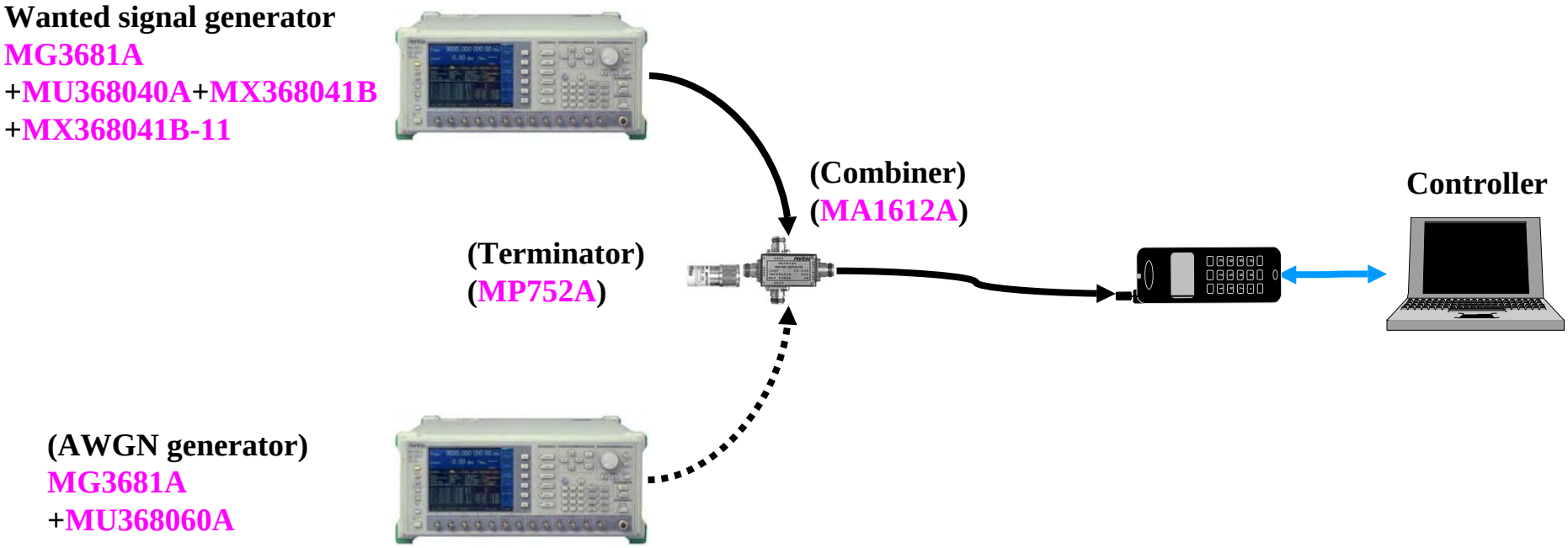


Figure A.17: Coding rate for Fixed reference Channel H-Set 3 (16QAM)

HSDPA CQI test Connection example

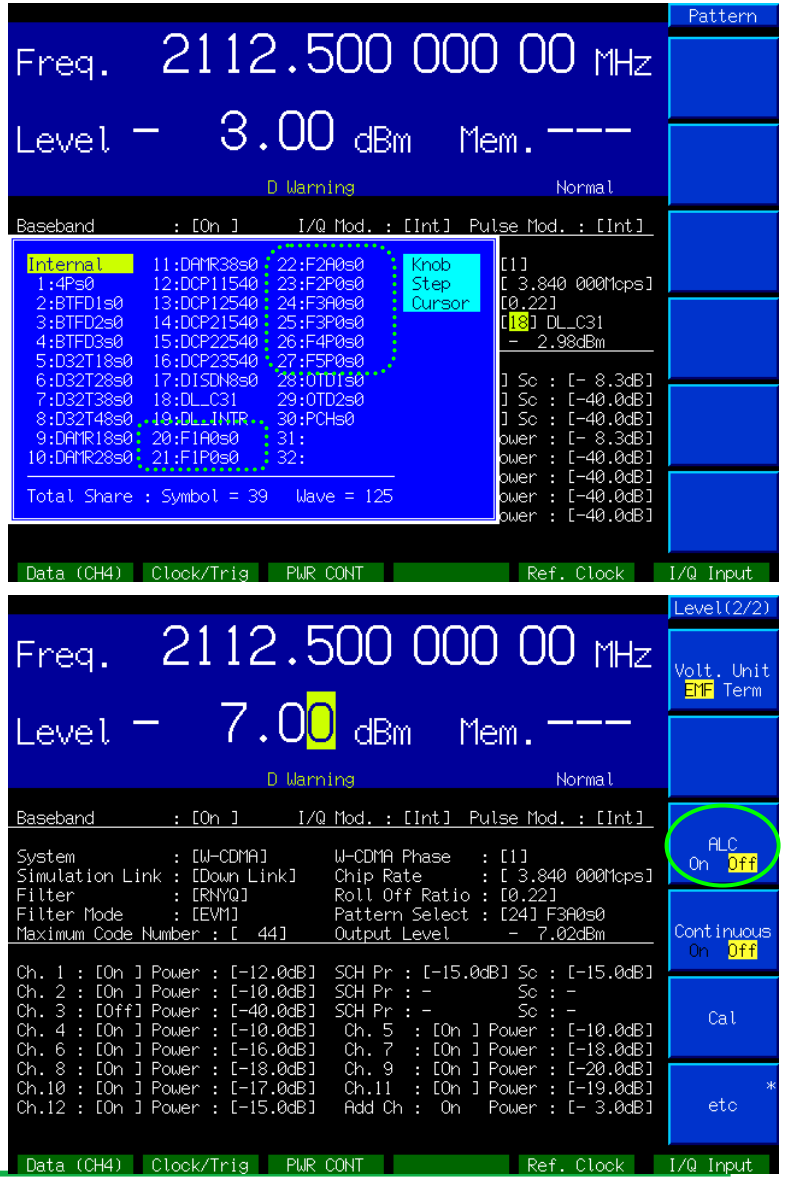


- Controller
  - Launches DL FRC in receivable state by FTM Factory Test Mode control.
  - Monitors CQI Channel Quality Indicator on UL HS-DPCCH and calculates BLER of DL HS-PDSCH.

Wanted signal generator Setup example

- **DL FRC**
  - » H-Set 1
    - – 16QAM
    - – QPSK
  - » H-Set 2
    - – 16QAM
    - – QPSK
  - » H-Set 3
    - – 16QAM
    - – QPSK
  - » H-Set 4
    - – QPSK
  - » H-Set 5
    - – QPSK

- **ALC Off**

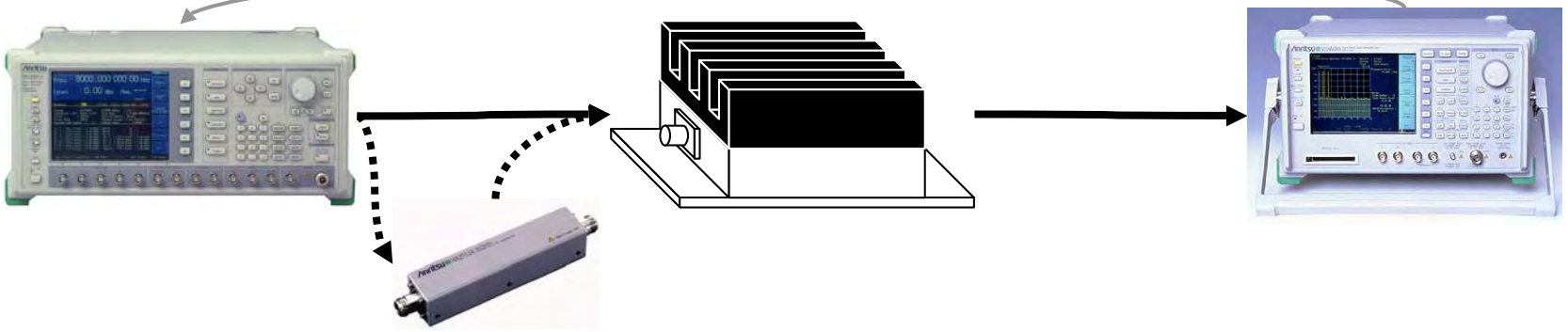


RF/IF components test Connection example

Signal source
MG3681A
+MU368040A+MX368041B

Signal analyzer
(MS8600/MS2680)

Reference clock



Spurious elimination filter
(MA2512A)

- Unwanted signals can be eliminated by connecting the filter if the spurious of signal source obstructs the evaluation.

Spurious of MG3681A
- 660 MHz (IF leakage)
- +660 MHz offset (Local leakage)
- 2×freq./3×freq. (2nd/3rd harmonics)

Downlink signal Setup example

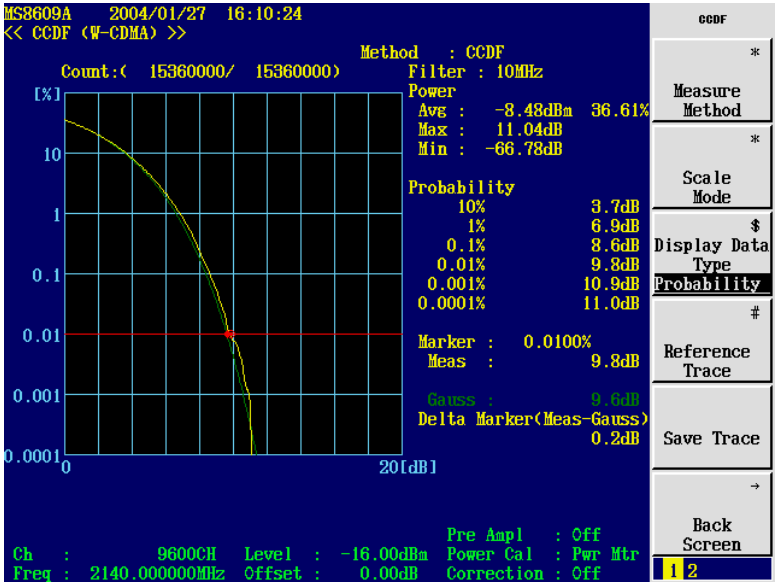
BS transmitter test

- **Test Model 1**
  - » Single carrier
  - » multi-carrier (2 carriers)
- **Test Model 2**
- **Test Model 3**
- **Test Model 4**
- **Test Model 5**
  - » Single carrier
  - » multi-carrier (2 carriers)

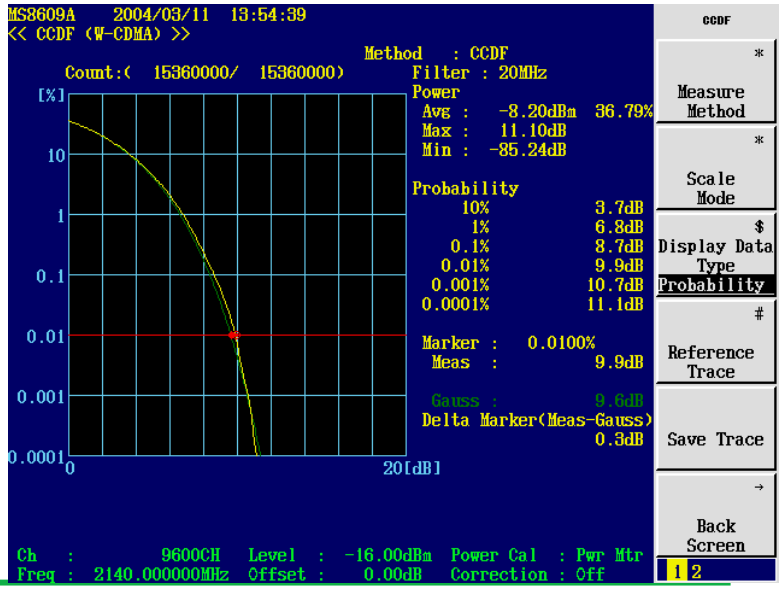
- **ACP priority filter**
  - » Spectrum emission mask
  - » ACLR
  - » Spectrum emissions

CCDF

- **Test Model 1**
  - » 64 DPCH
    - – Single carrier

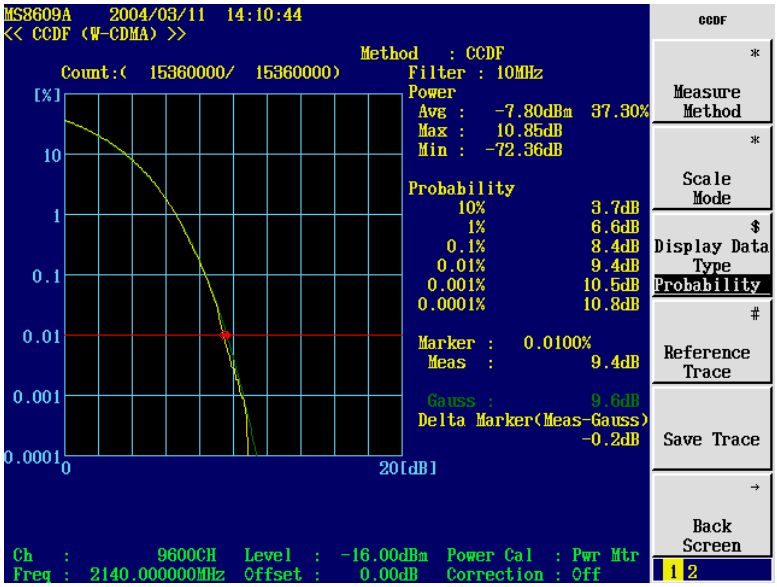


- – 2 carriers

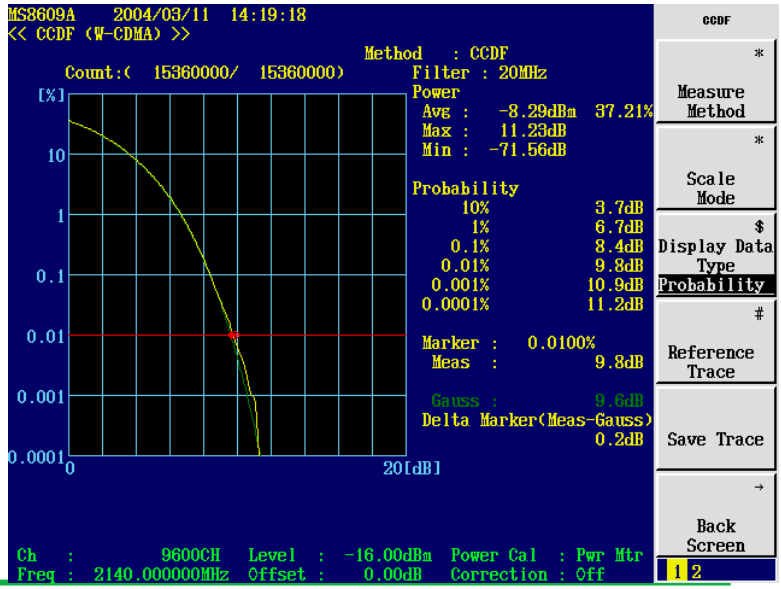


CCDF

- **Test Model 5**
  - » 30 DPCH + 8 HS-PDSCH
    - – Single carrier



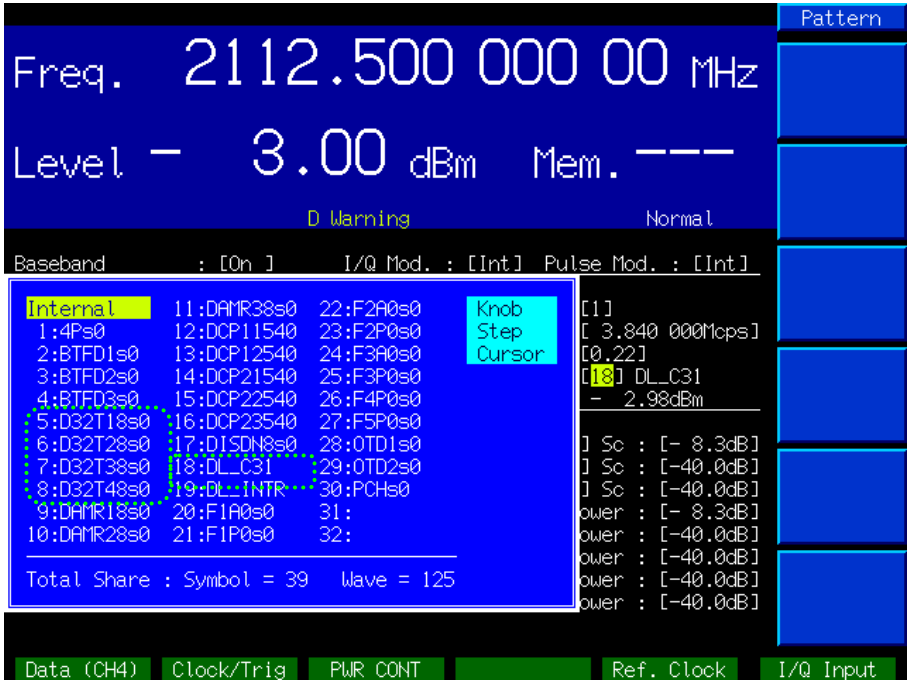
- – 2 carriers



Downlink signal Setup example

UE receiver test

- **DL RMC 12.2 kbps**
  - » for RX test
  - » for Performance test
- **DL RMC 64 kbps**
- **DL RMC 144 kbps**
- **DL RMC 384 kbps**

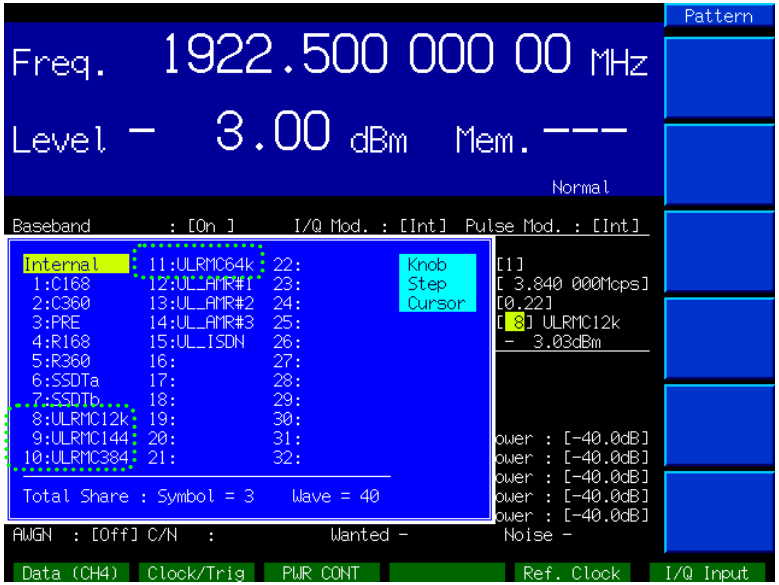


Uplink signal Setup example

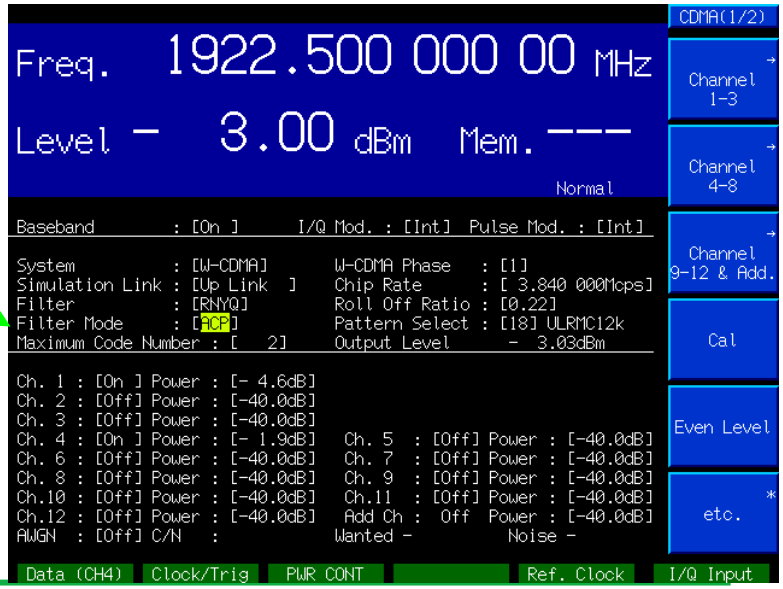
UE transmitter test

BS receiver test

- **UL RMC 12.2 kbps**
- **UL RMC 64 kbps**
- **UL RMC 144 kbps**
- **UL RMC 384 kbps**



- **ACP priority filter**
  - Transmitter test
    - » Spectrum emission mask
    - » ACLR
    - » Spectrum emissions

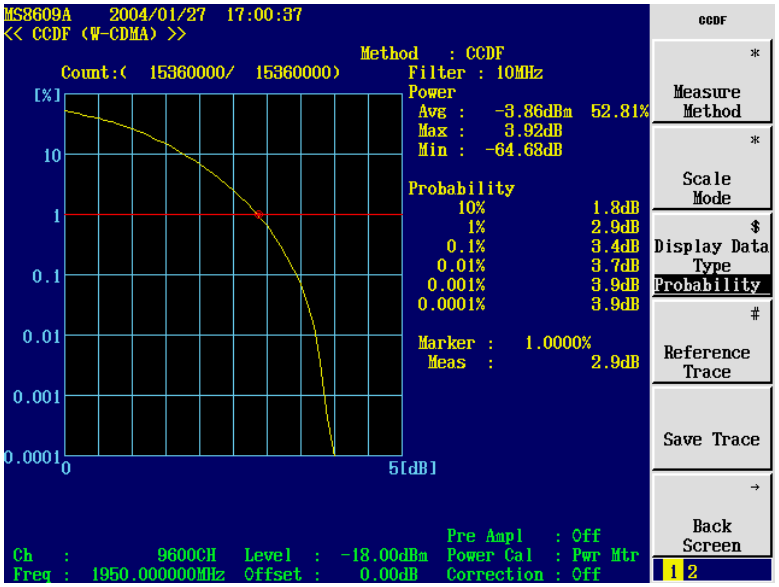


CCDF

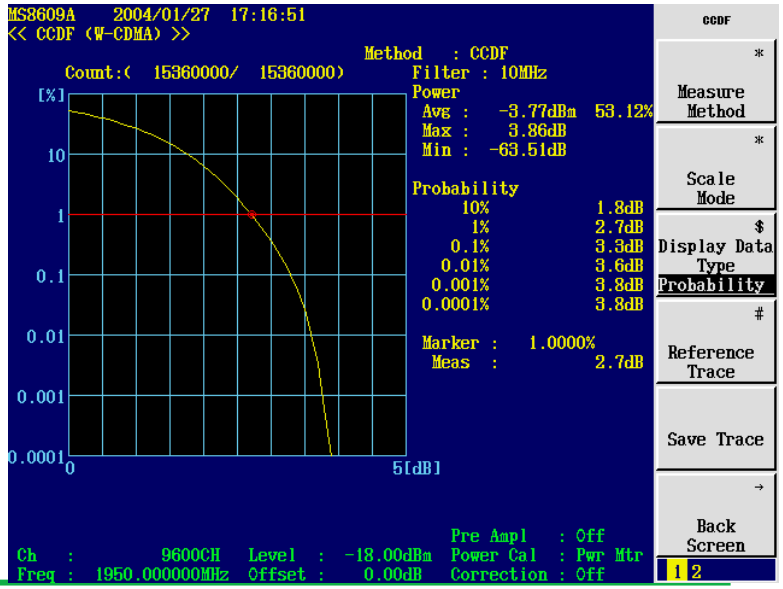
- **UL RMC**
  - » 12.2 kbps

Table A.1: Reference measuremet channels for UL DCH

Parameter		DCH for DTCH / DCH for DCCH					Unit
DPDCH	Information bit rate	12,2/2,4	64/2,4	144/2,4	384/2,4	2048/2,4	kbps
	Physical channel	60/15	240/15	480/15	960/15	960/15	kbps
	Spreading factor	64	16	8	4	4	
	Repetition rate	22/22	19/19	8/9	-18/-17	-7/-7	%
	Interleaving	20	40	40	40	80	ms
	Number of DPDCHs	1	1	1	1	6	
DPCCH	Dedicated pilot	6					bit/slot
	Power control	2					bit/slot
	TFCI	2					bit/slot
	FBI	0 / 2					bit/slot
	Spreading factor	256					
Power ratio of DPCCH/DPDCH		-2,69	-5,46	-9,54	-9,54	-9,54	dB
Amplitude ratio of DPCCH/DPDCH		0,7333	0,5333	0,3333	0,3333	03333	
Note:	Combination of TFCI bit of 0 bit/slot and FBI bit of 2 bit /slot is applied in test of Site Selection Diversity Transmission specified in 8.10.						

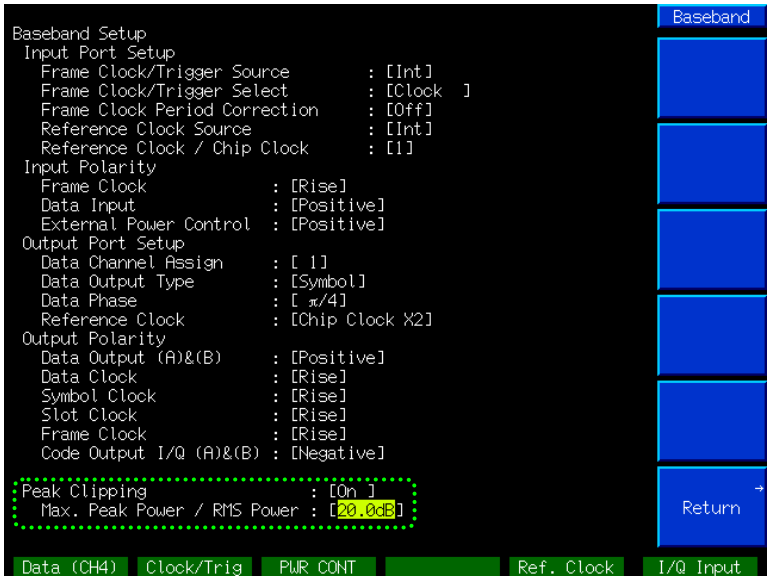


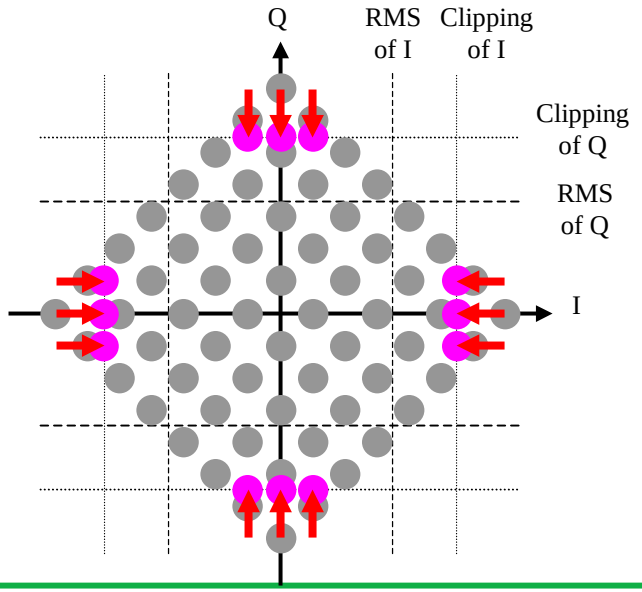
- » 384 kbps



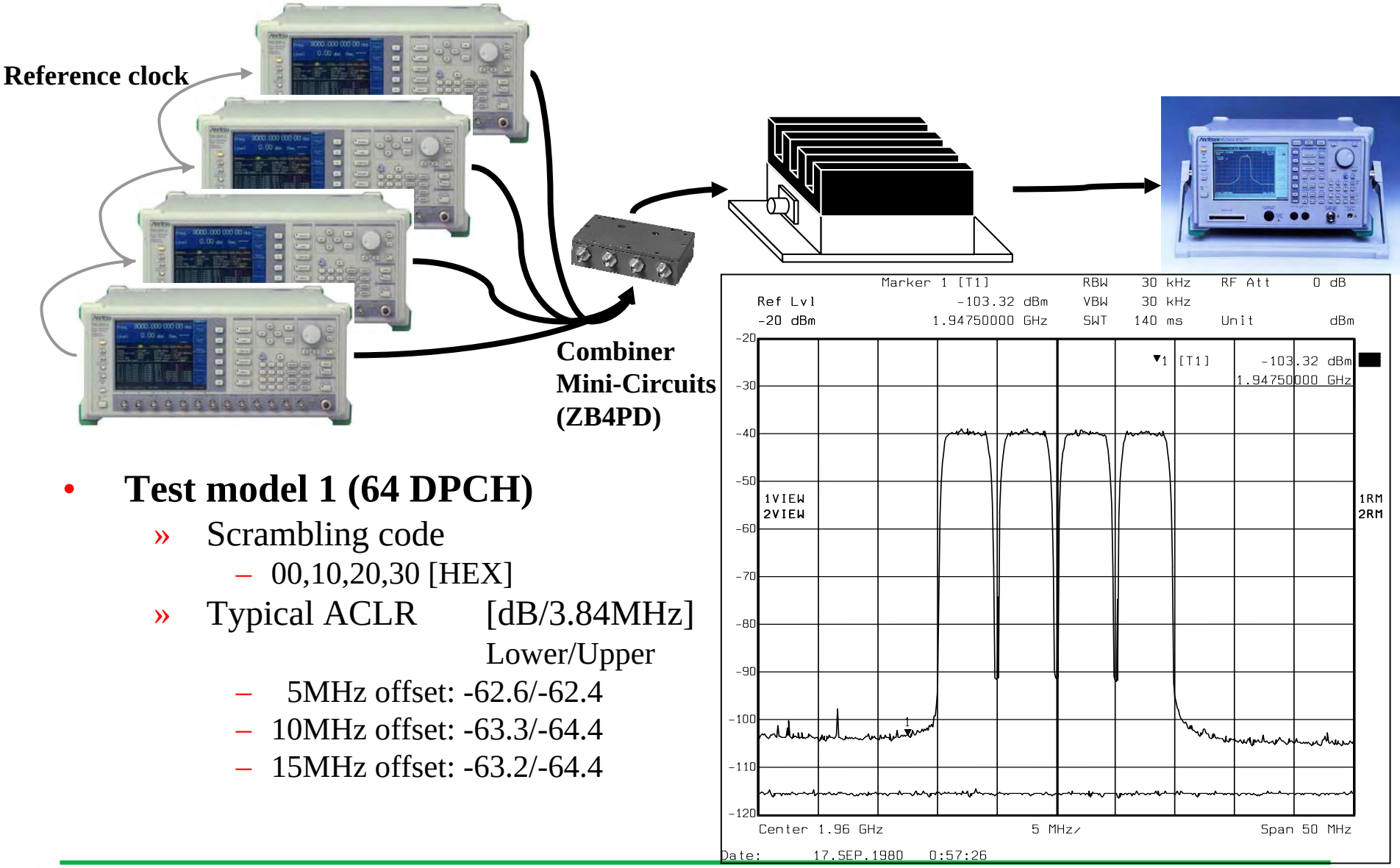
Peak Clipping of modulation signal Setup example

- **Useful for the evaluation of crest factor (CCDF)**
  - » Limiting the peak level of I/Q amplitude before FIR filtering
    - – I or Q RMS level
      +
      0 ~ 20 dB, 0.1 dB resolution
      - Measure CCDF of output signal (after FIR filtering) by signal analyzer (MS8608A/09A), and adjust the level to limit.
    - – ACLR of output signals is not deteriorated because of no distortion caused by clipping.
      - Extreme clipping deteriorates waveform quality.
  - » Scalar clipping
    - – Limiting I or Q amplitude level





Multi-carrier signal source



- **Test model 1 (64 DPCH)**
  - » Scrambling code
    - – 00,10,20,30 [HEX]
  - » Typical ACLR [dB/3.84MHz]
    Lower/Upper
    - – 5MHz offset: -62.6/-62.4
    - – 10MHz offset: -63.3/-64.4
    - – 15MHz offset: -63.2/-64.4

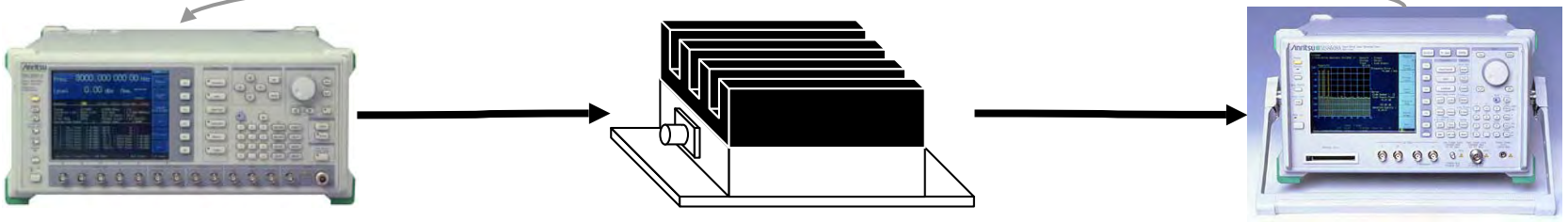
GSM/EDGE

RF/IF components test Connection example

Signal source
MG3681A
+MU368010A+MX368012A
or
+MU368030A+MX368031A

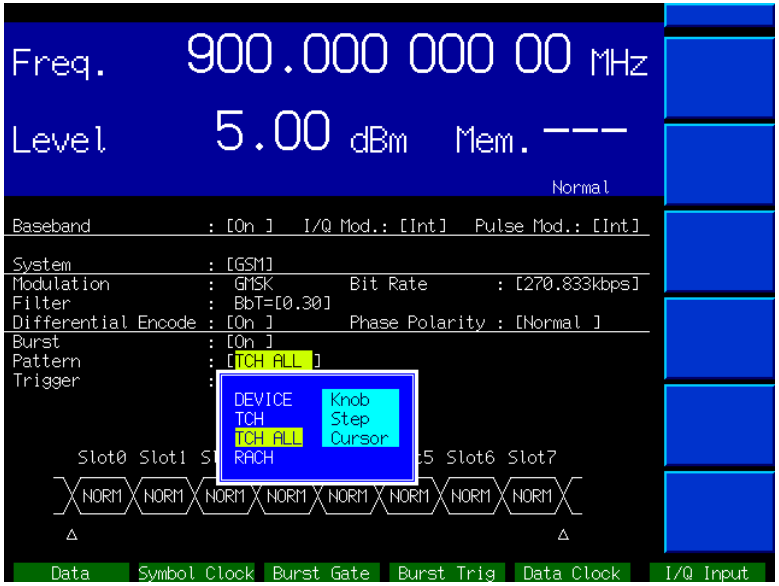
Signal analyzer
(MS8600/MS2680)

Reference clock

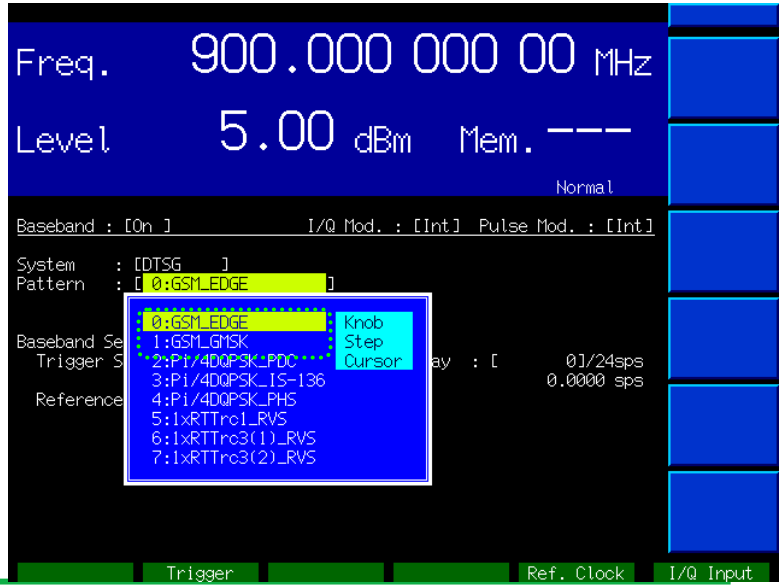


Downlink/Uplink signal Setup example

- **MX368012A**
  - » GMSK modulation
    - – Data + GP Guard period (8.25 symbol) Burst format
    - – Normal burst format for TCH
    - – Access burst format for RACH
    - – Continuous modulation format



- **MX368031A**
  - » 8PSK modulation
    - – Continuous modulation format
  - » GMSK modulation
    - – Continuous modulation format



CDMA2000 1xEV-DO 3GPP2
AN Access Network testing

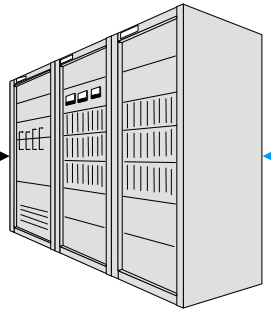
3GPP2 C.S0032 -0 v2.0
3.1.1 Receiver Minimum Standards
3.1.1 Transmitter Minimum Standards

Section	Test	Wanted signal generator	Interfering signal generator	CW generator	AWGN generator	Others
3.1.1.3.1	Data Channel Demodulation Performance (Case 1: without closed loop power control)	MG3681A +MU368030A +MX368033A			+MU368060A +MU368040A	
3.1.1.4.1	Receiver Sensitivity					
3.1.1.4.2	Receiver Dynamic Range				+MU368060A +MU368040A	
3.1.1.4.3	Single Tone Desensitization		MG3681A or 3GHz	MG3642A 2.08GHz		MA1612A 3GHz Combiner
3.1.1.4.4	Intermodulation Spurious Response Attenuation		MG3681A			
3.1.1.4.5	Adjacent Channel Selectivity		MG3681A +MU368030A +MX368031A			
3.1.1.4.6	Receiver Blocking Characteristics		MG3681A or 3GHz	MG3692A 20GHz or MG3642A 2.08GHz		
3.1.1.6	Received Signal Quality Indicator (RSQI)				+MU368060A +MU368040A	
3.1.2.4.3	Inter-Sector Transmitter Intermodulation		MG3681A +MU368030A +MX368031A (+MG3681A-42)			Spectrum analyzer Circulator

Inter-Sector Transmitter Intermodulation test Connection example

Interfering signal generator
MG3681A
+MU368030A+MX368031A
(+MG3681A-42)

Circulator



Controller

Spectrum analyzer
MS8608A/8609A
+MX860804A/860904A

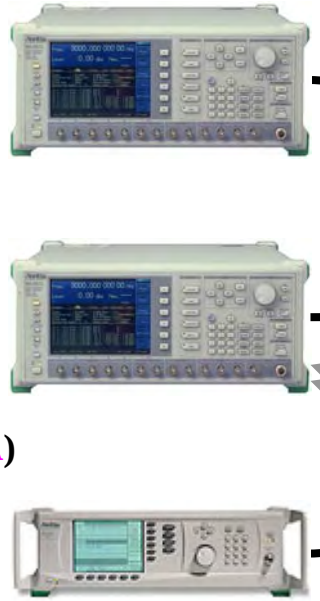
- Controller
  - Launches in the transmitting state by FTM Factory Test Mode control.

Receiver test Connection example

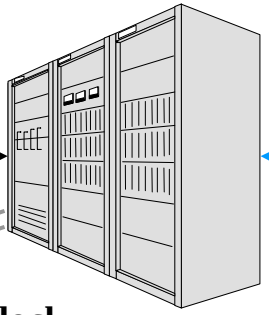
Interfering signal generator
CW generator
(AWGN generator)
MG3681A
+MU368030A+MX368031A
(+MU368060A)

Wanted signal generator
(+ AWGN generator)
MG3681A
+MU368030A+MX368033A
(+MU368060A+MU368040A)

CW generator
(MG3692A)



Combiner
(MA1612A)



Controller
PER calculation

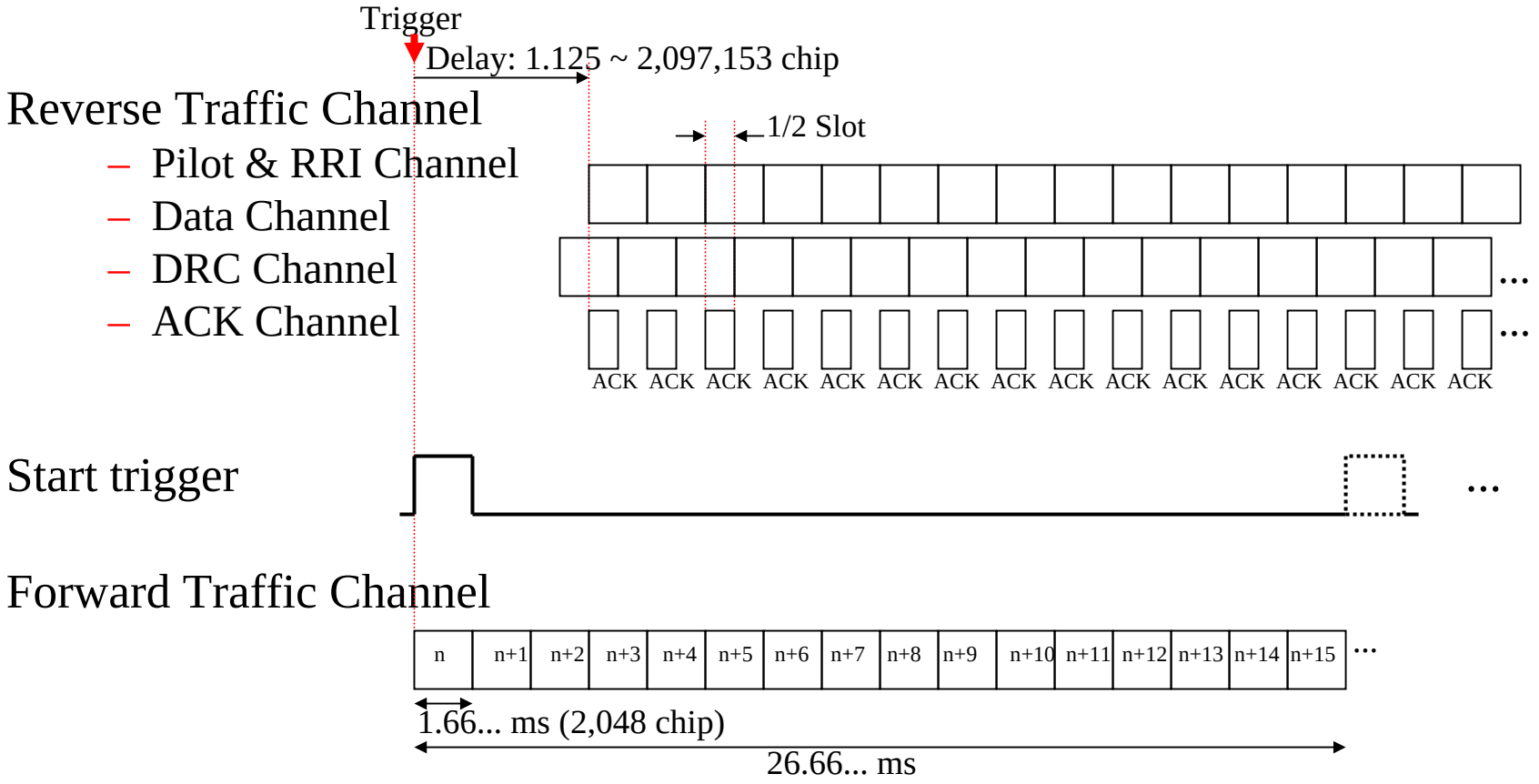
Start trigger

Reference clock

- Start trigger
  - Front panel [Trigger] Input
    Apply only one
    - 26.66... ms clock (Short sequence rollover)
    - 426.66... ms clock (Control Channel Cycle)
    - 2 sec (Even second time mark)
- Reference clock
  Apply only one
  - Front panel [Ref. Clock] Input
    - 8× 1.2288 MHz (9.8304 MHz)
  - Rear panel [10MHz/13MHz Ref] Input
    - 10 MHz, 13 MHz
- Controller
  - Launches Reverse Traffic channel in receivable state by FTM Factory Test Mode control.
  - Checks the CRC per demodulated Traffic channel packet and calculates the PER.

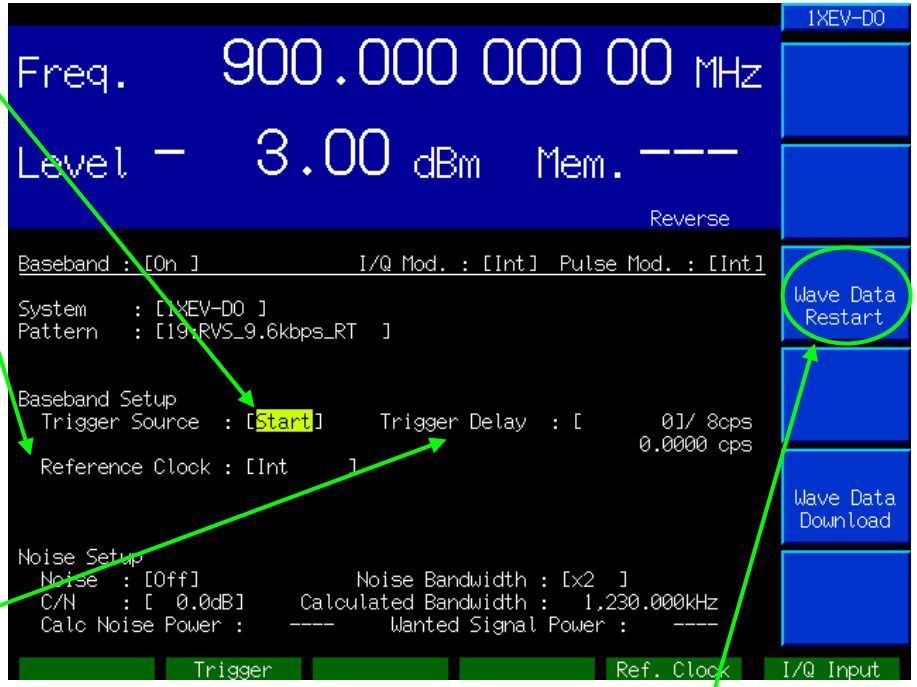
Timing synchronization Setup example

- **Start trigger delay**
  - » Set the timing to which AN can receive Reverse Traffic channel



Timing sync. Setup example

- **Setting External Start trigger**
  - » Captures/ Synchronizes the Trigger only once
- **Reference clock:**
  - » [Ref. Clock] Input applicable case
    - – Reference Clock : [Ext(TTL)]
      - 8× 1.2288 MHz (9.8304 MHz)
  - » [10MHz/13MHz Ref] Input applicable case
    - – Reference Clock : [Int]



- **Start trigger delay**
  - » 0 ~ 16,777,215 /8 chip
    1/8 chip resolution
  - » Delay from Trigger
    + 9/8 chip
    - – 1.125 ~ 2,097,153 chip

- **Trigger recapture/ synchronization**

Long Code Mask sync.

- **Reverse Traffic Channel Long Code Mask**
  - 42-bit MI_{RTCMAC}

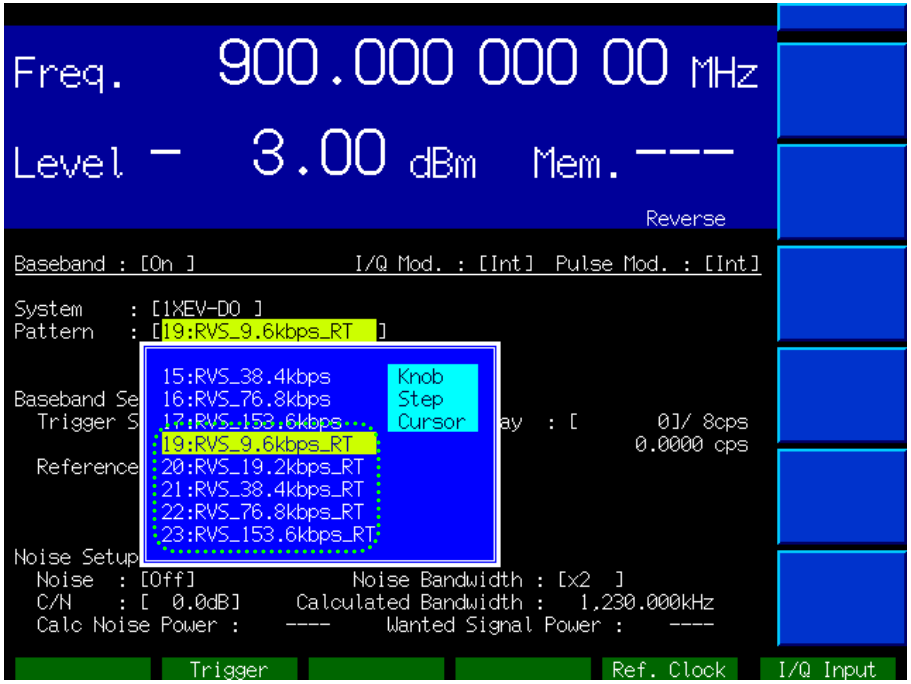
BIT	41	40	39	38	37	36	35	34	33	32	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
MI_{RTCMAC}	1	1	1	1	1	1	1	1	1	1	Permuted (ATI_{LCM})																															

  - 42-bit MQ_{RTCMAC}
    - Derived from MI_{RTCMAC}
      - $MQ_{RTCMAC}[k] = MI^{RTCMAC}[k-1]$, for k = 1,…,41
      - $MQ_{RTCMAC}[0] = MI_{RTCMAC}[0] \oplus MI_{RTCMAC}[1] \oplus MI_{RTCMAC}[2] \oplus MI_{RTCMAC}[4] \oplus MI_{RTCMAC}[5] \oplus MI_{RTCMAC}[6] \oplus MI_{RTCMAC}[9] \oplus MI_{RTCMAC}[15] \oplus MI_{RTCMAC}[16] \oplus MI_{RTCMAC}[17] \oplus MI_{RTCMAC}[18] \oplus MI_{RTCMAC}[20] \oplus MI_{RTCMAC}[21] \oplus MI_{RTCMAC}[24] \oplus MI_{RTCMAC}[25] \oplus MI_{RTCMAC}[26] \oplus MI_{RTCMAC}[30] \oplus MI_{RTCMAC}[32] \oplus MI_{RTCMAC}[34] \oplus MI_{RTCMAC}[41]$
    - ⊕: XOR

- **Setting AN**
  - MI_{RTCMAC} 3FF00000000
  - MQ_{RTCMAC} 3FE00000001

Wanted signal generator Setup example

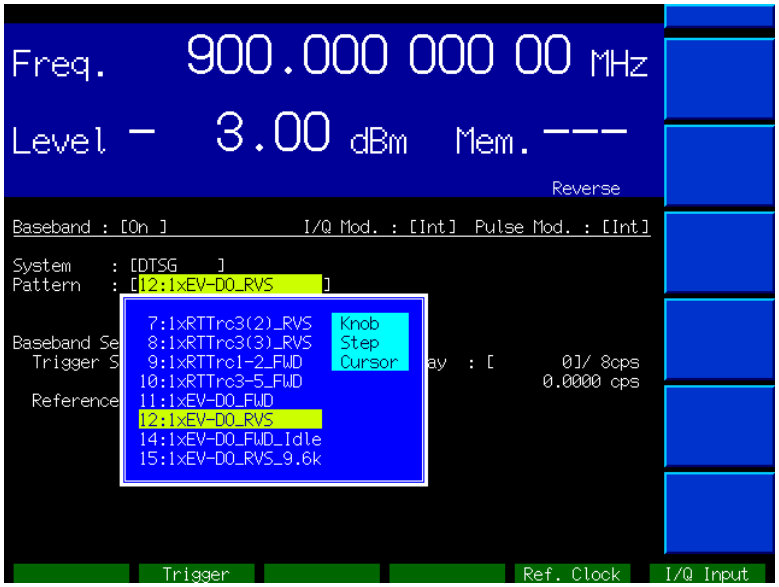
- **Reverse Traffic Channel**
  Data Rate
  - » 9.6 kbps
  - » 19.2 kbps
  - » 38.4 kbps
  - » 76.8 kbps
  - » 153.6 kbps

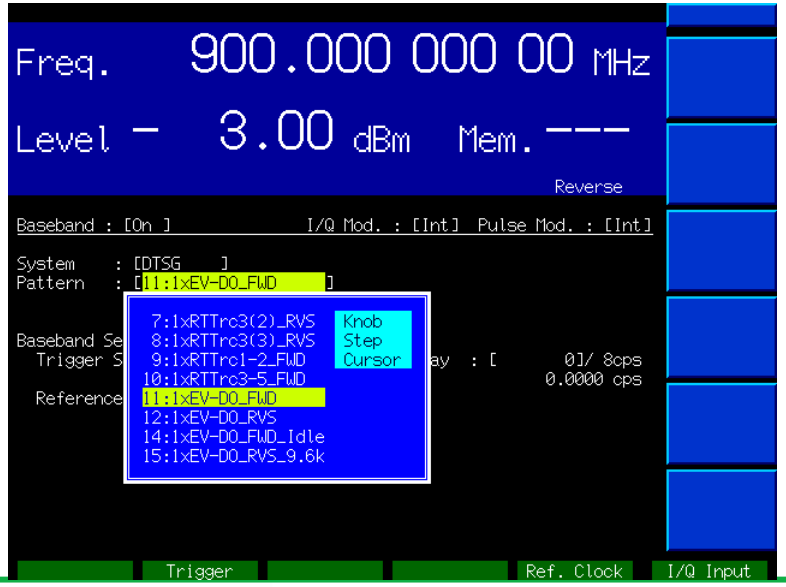


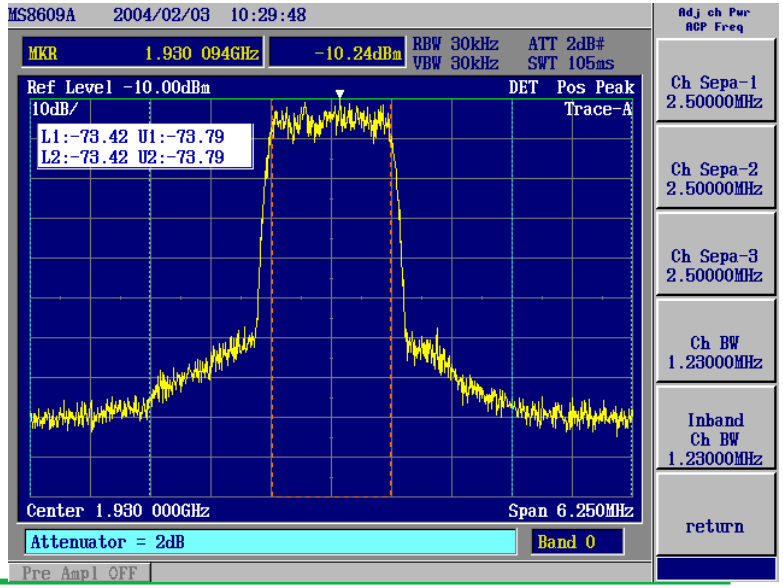
Interfering signal generator Setup example

- **HRPD signal**
  - CDMA2000 1xEV-DO Reverse Traffic Channel
    - » Adjacent Channel Selectivity test

- **Sector 2 (Interferer)**
  - » Inter-Sector Transmitter Intermodulation test



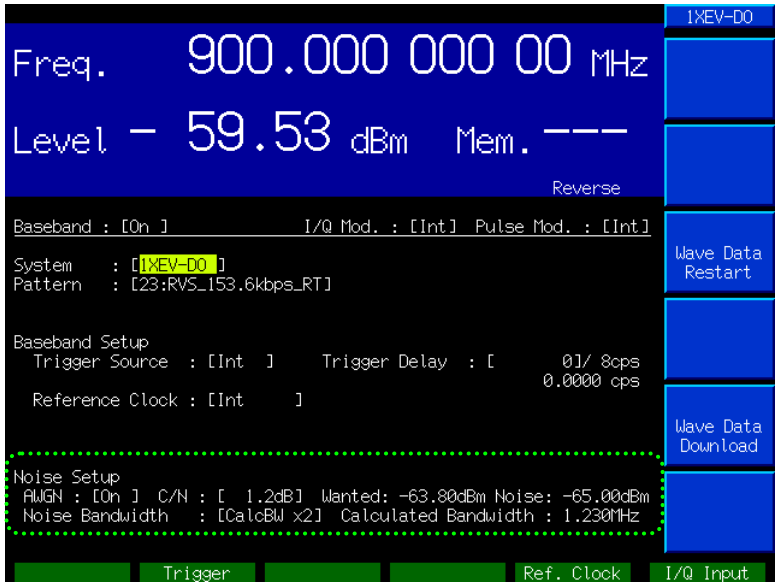




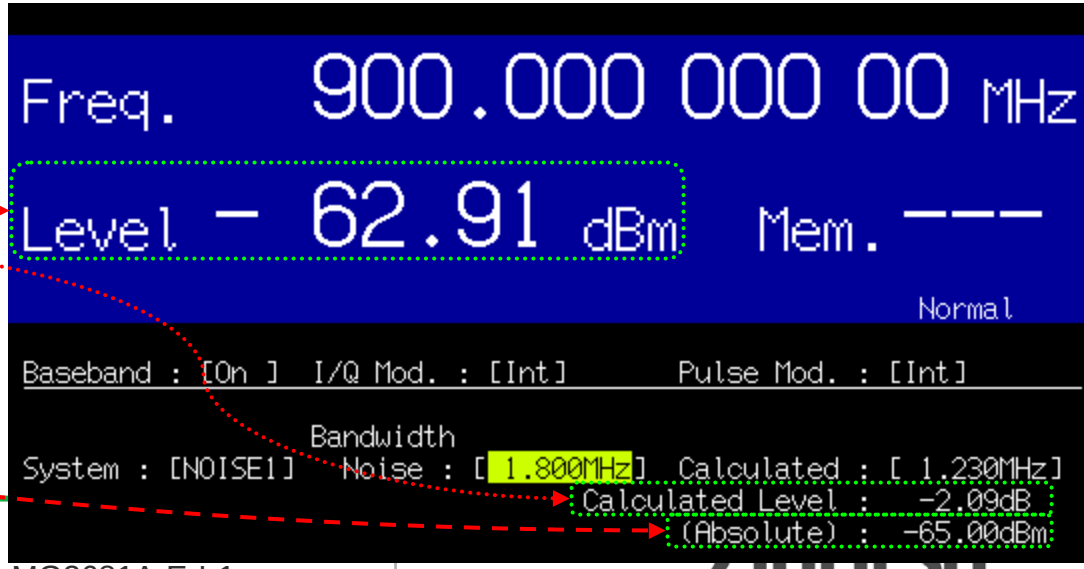
AWGN generator Setup example

- **AWGN mixing**
  - » C/N = Wanted signal/AWGN
    - – Dynamic range test
      - C/N: [1.2dB]
        Wanted -63.8dBm Noise -65.0dBm
    - – RSQI test
      - C/N: [1.0dB]
        Wanted -83.0dBm Noise -84.0dBm
        (Data rate:153.6 kbps,
        Data E_b/N_t: 8 dB,
        DataChannelGain: 18.5 dB)

$$\frac{\hat{I}_{or}}{I_{oc}} = N_t \times 1.23\times10^6 \times \frac{E_b}{\text{Data rate}} \times \frac{1+\text{ChannelGain}}{\text{ChannelGain}}$$



- **AWGN source**
  - » Ioc =
    Total level
    + Bandwidth level



CDMA2000 1xEV-DO 3GPP2 AT Access Terminal testing

3GPP2 C.S0033 -0 v2.0

3.1.1 Receiver Minimum Standards

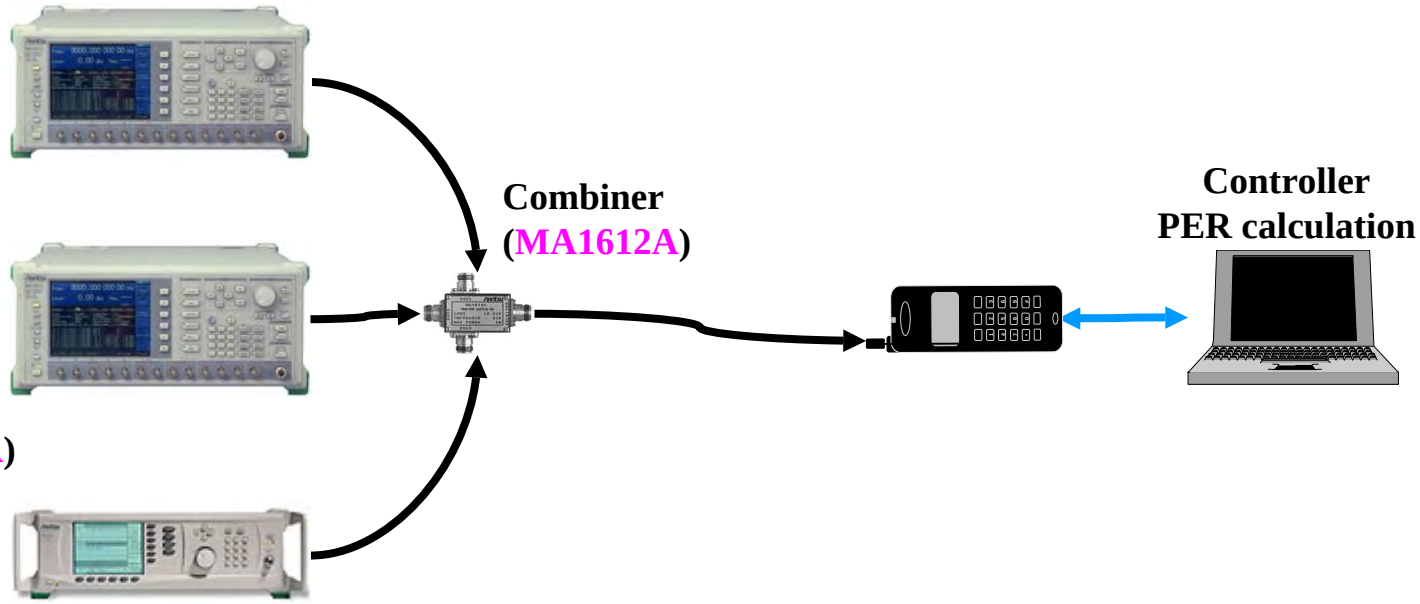
Section	Test	Wanted signal generator	Interfering signal generator	CW generator	AWGN generator	Others
3.1.1.2.1	Demodulation of Forward Traffic Channel in AWGN	MG3681A +MU368030A +MX368033A			+MU368060A +MU368040A	
3.1.1.2.2	Demodulation of Forward Traffic Channel in Multipath Fading Channel				MG3681A +MU368060A	Channel simulator, Combiner
3.1.1.3.1	Receiver Sensitivity and Dynamic Range					
3.1.1.3.2	Single Tone Desensitization		MG3681A or 3GHz	MG3642A 2.08GHz		MA1612A 3GHz Combiner
3.1.1.3.3	Intermodulation Spurious Response Attenuation		MG3681A			
3.1.1.3.4	Adjacent Channel Selectivity		MG3681A +MU368030A +MX368031A			
3.1.1.4.5	Receiver Blocking Characteristics		MG3681A or 3GHz	MG3692A 20GHz or MG3642A 2.08GHz		

Receiver test Connection example

Interfering signal generator
CW generator
(AWGN generator)
MG3681A
+MU368030A+MX368031A
(+MU368060A)

Wanted signal generator
(AWGN generator)
MG3681A
+MU368030A+MX368033A
(+MU368060A+MU368040A)

CW generator
(MG3692A)



Combiner
(MA1612A)

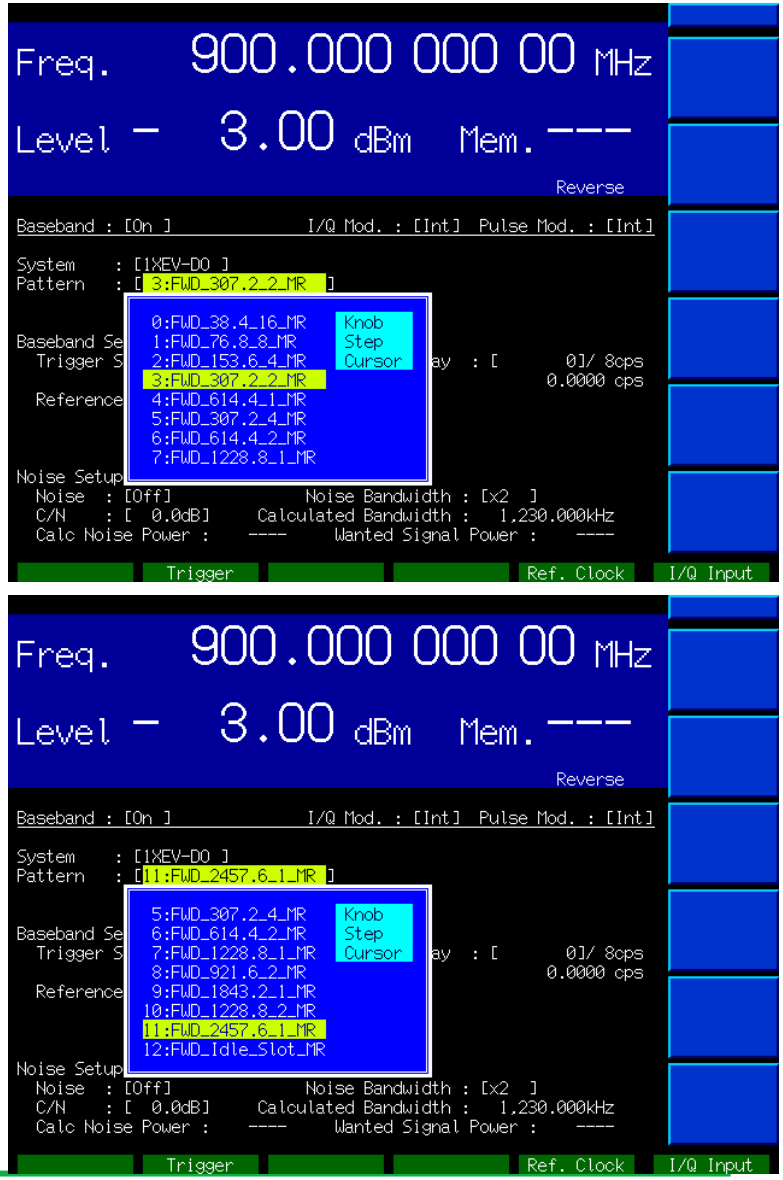
Controller
PER calculation

- Controller
  - Launches Forward Traffic channel in receivable state by FTM Factory Test Mode control.
  - Checks the CRC per demodulated Traffic channel packet and calculates the PER.

Wanted signal generator Setup example

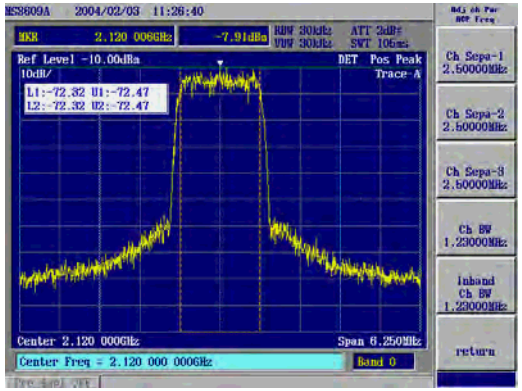
- **Forward Traffic Channel**

Data Rate	Slots per Physical Layer Packet
» 38.4 kbps	16
» 76.8 kbps	8
» 153.6 kbps	4
» 307.2 kbps	2
» 614.4 kbps	1
» 307.2 kbps	4
» 614.4 kbps	2
» 1,228.8 kbps	1
» 921.6 kbps	2
» 1,843.2 kbps	1
» 1,228.8 kbps	2
» 2,457.6 kbps	1



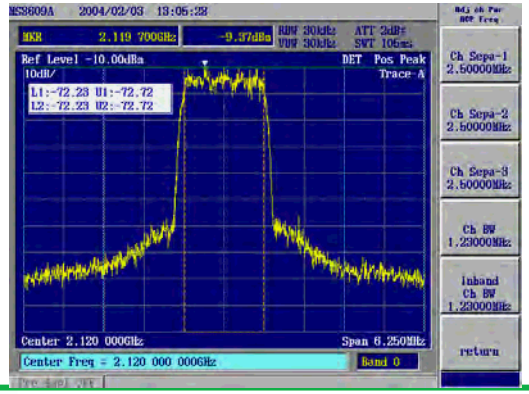
Interfering signal generator Setup example

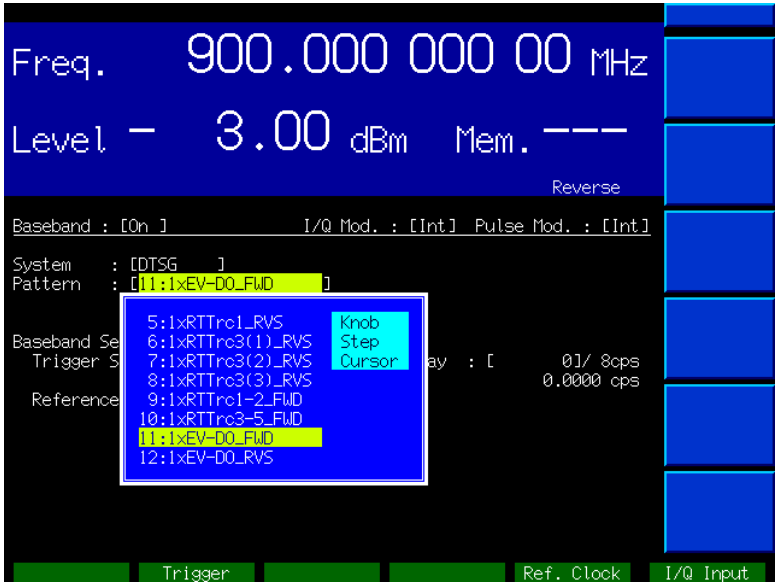
- **HRPD signal**
  - CDMA2000 1xEV-DO
    Forward Traffic Channel

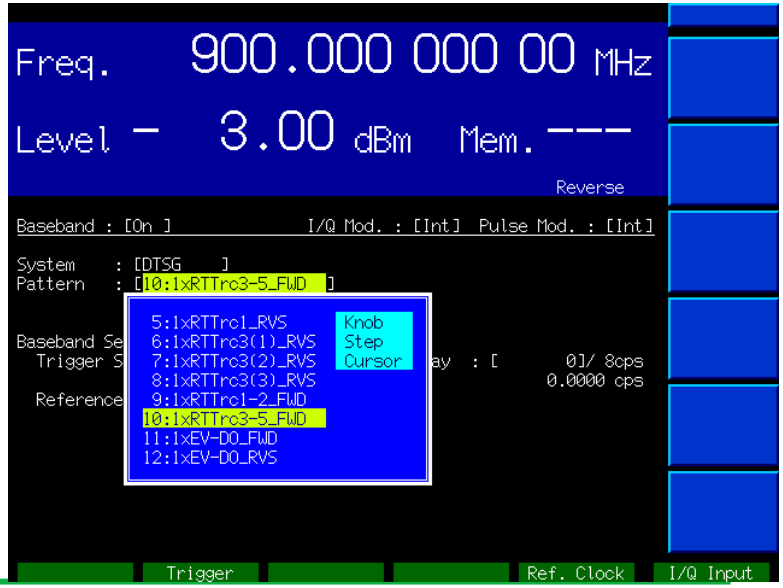


or

- **CDMA signal**
  - CDMA2000 1X
    Forward Traffic Channel

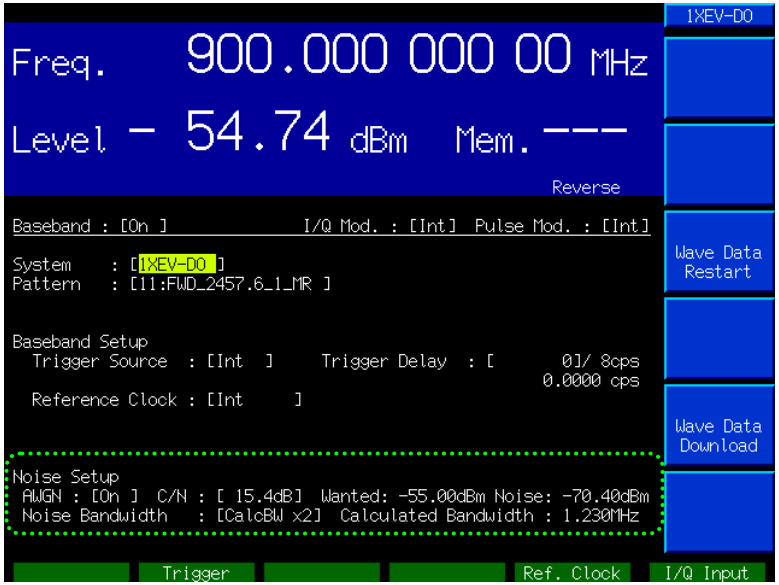




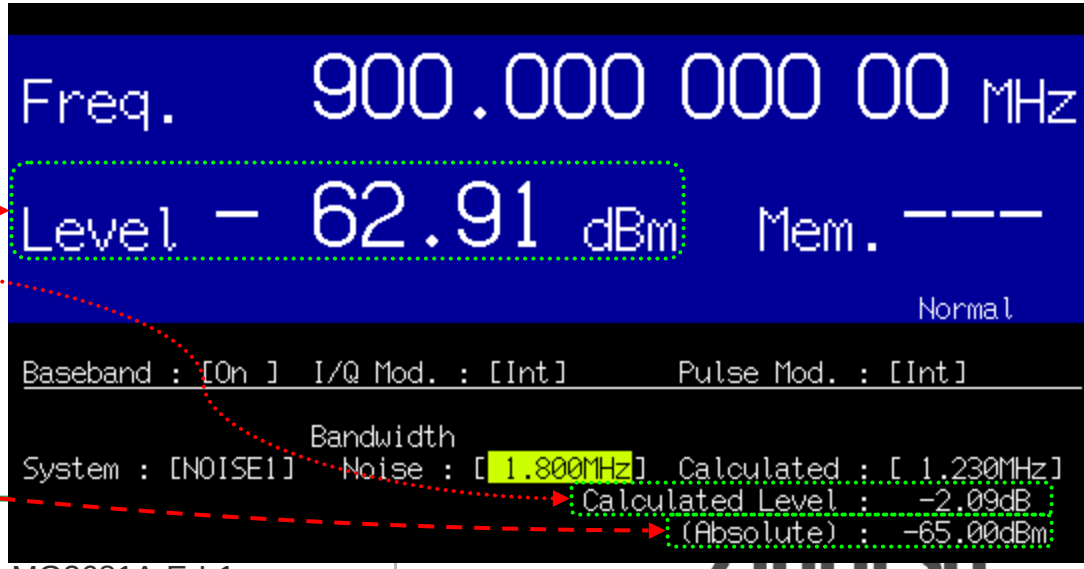


AWGN generator Setup example

- **AWGN mixing**
  - » C/N = Wanted signal/AWGN
    - – Demodulation of FTC in AWGN test
      - C/N: Îor/Ioc



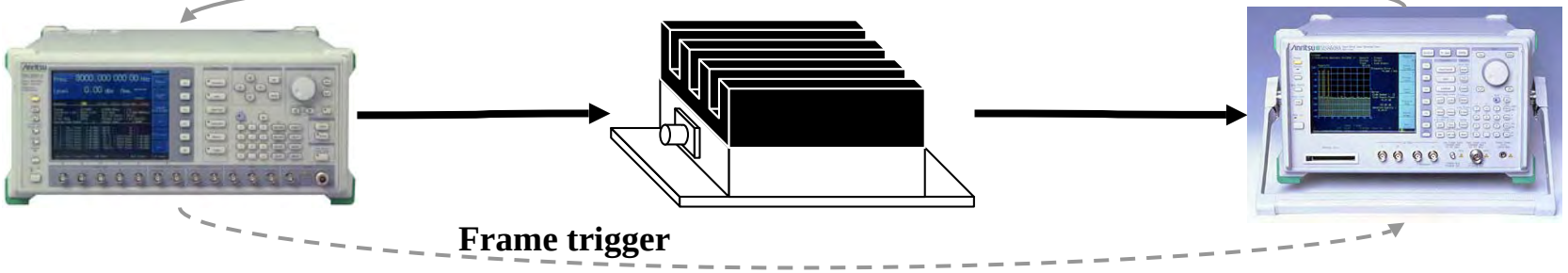
- **AWGN source**
  - » Ioc =
    - Total level
    - + Bandwidth level



RF/IF components test Connection example

Signal source
MG3681A
+MU368030A+MX368033A
or MX368031A

Signal analyzer
(MS8600/MS2680)



- Frame trigger
  - Required when performing modulation analysis of Reverse signal by MS8608A/8609A
    - Because, it cannot catch Pilot Channel when DataChannelGain is high.
  - Rear panel A4[Frame Trigger] or B2[Sequence Pulse] Output
    - To MS8608A/8609A rear panel [Trigger] Input
    - 26.66... ms clock

Rate (kbps)	DataChannelGain (dB)
9.6	3.75
19.2	6.75
38.4	9.75
76.8	13.25
153.6	18.50

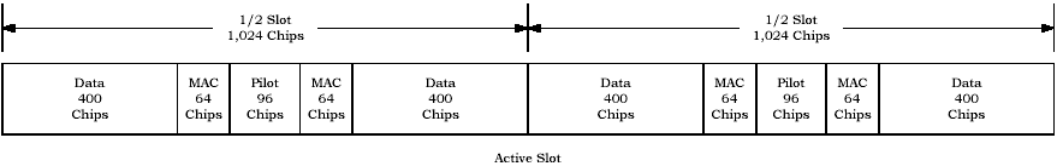
Field	Value (Decimal)
DRCLength	0 (1 slot)
DRCChannelGain	6 (3 dB)
ACKChannelGain	6 (3 dB)

Forward signal Setup example

AN transmitter test

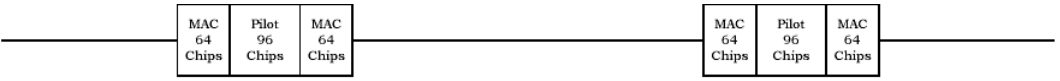
AT receiver test

- **MX368033A**
  - » Active Slot: 8,4,3,2,1 carrier
    - – 2,457.6 kbps, 16QAM



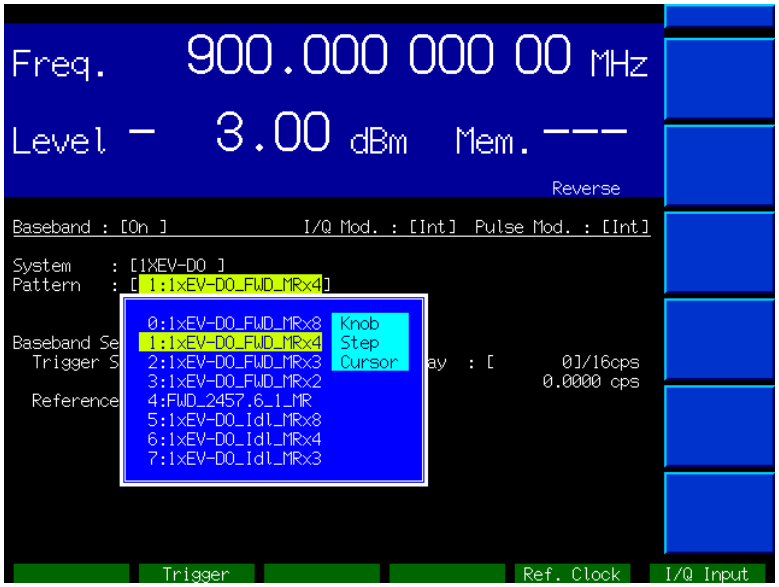
Active Slot

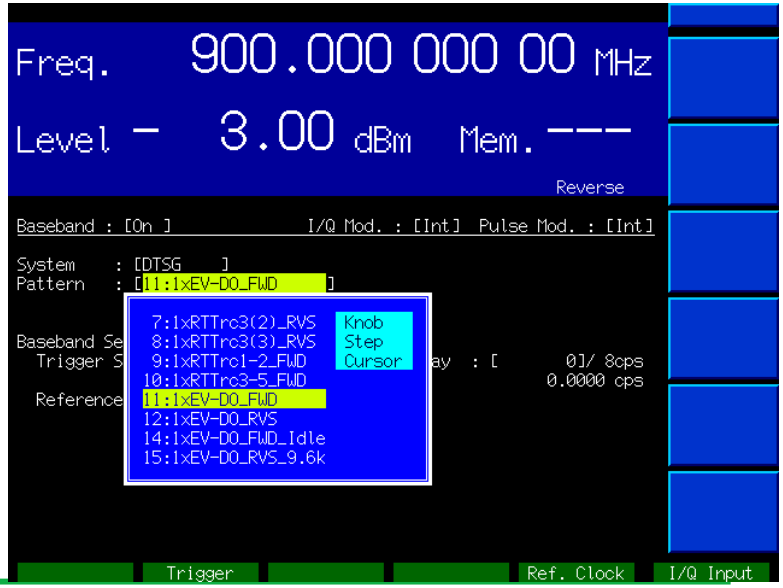
  - » Idle Slot: 8,4,3,2,1 carrier
    - – Burst signal



Idle Slot

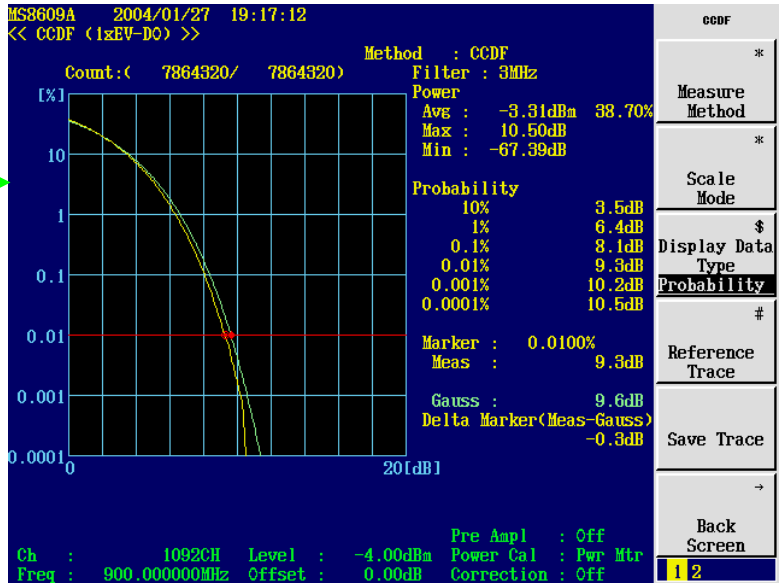
- **MX368031A**
  - » Active Slot: single carrier
    - – 2,457.6 kbps, 16QAM
  - » Idle Slot: single carrier
    - – Burst signal

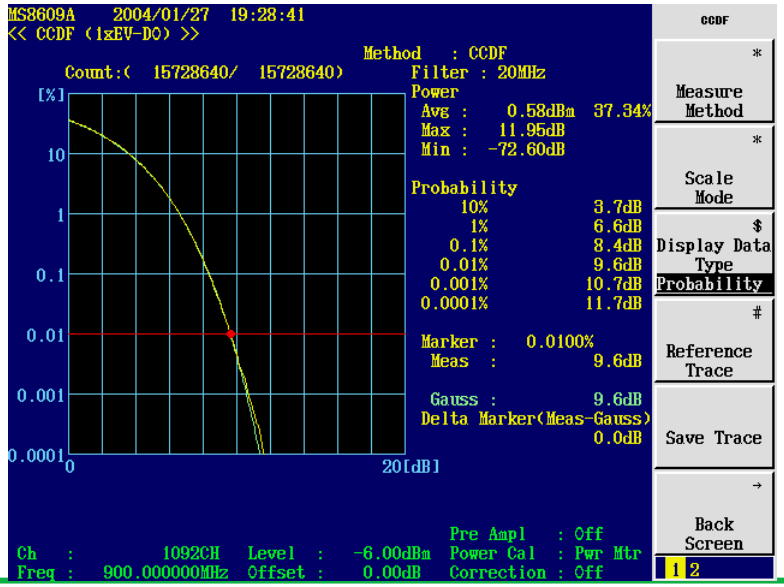


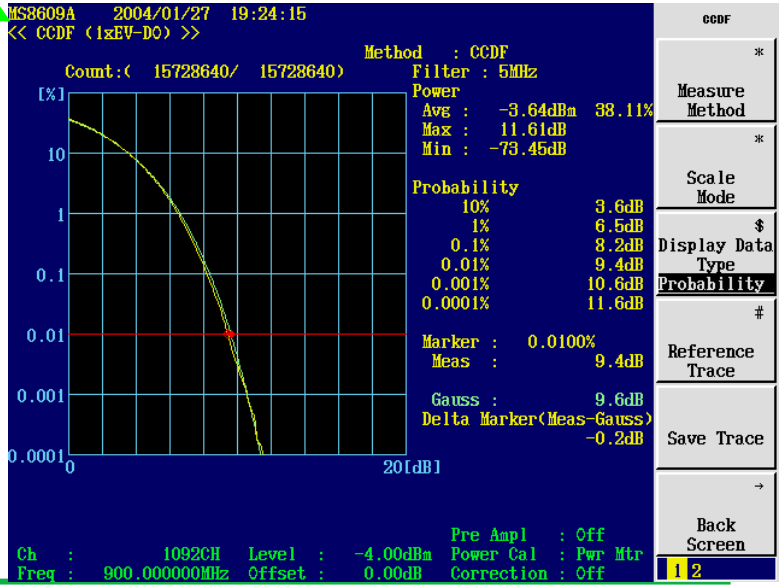


CCDF

- **Active slot**
  - » Single carrier
  - » 2 carriers
  - » 8 carriers





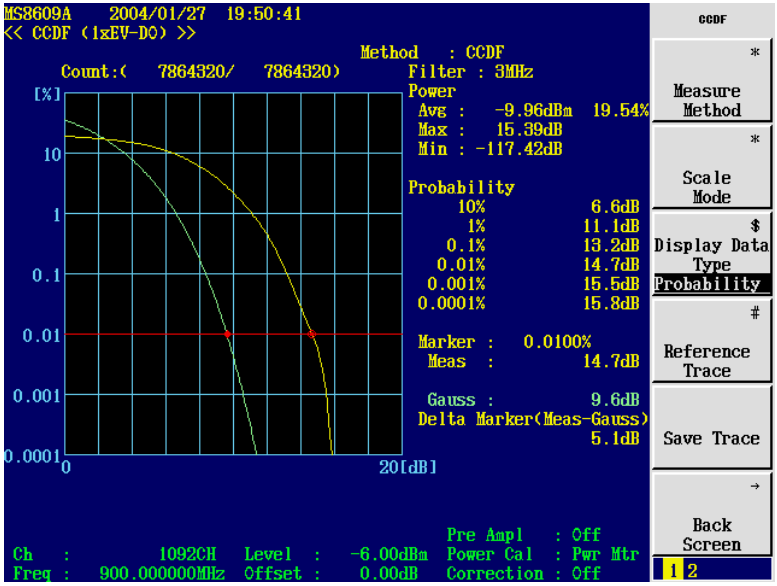


CCDF

- **Idle slot**
  - » Single carrier
    - – Mean power of the ensemble average ≈

      Mean power of the Pilot/MAC channel ensemble average

      - 6.6 dB

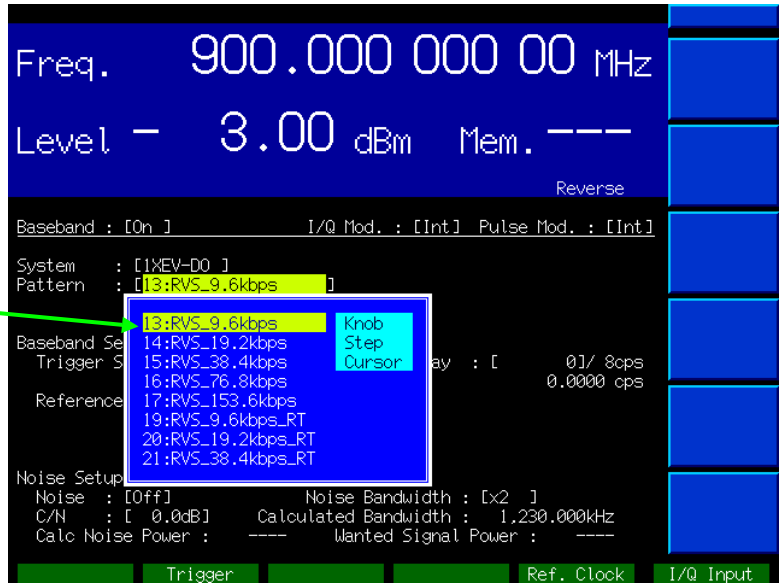


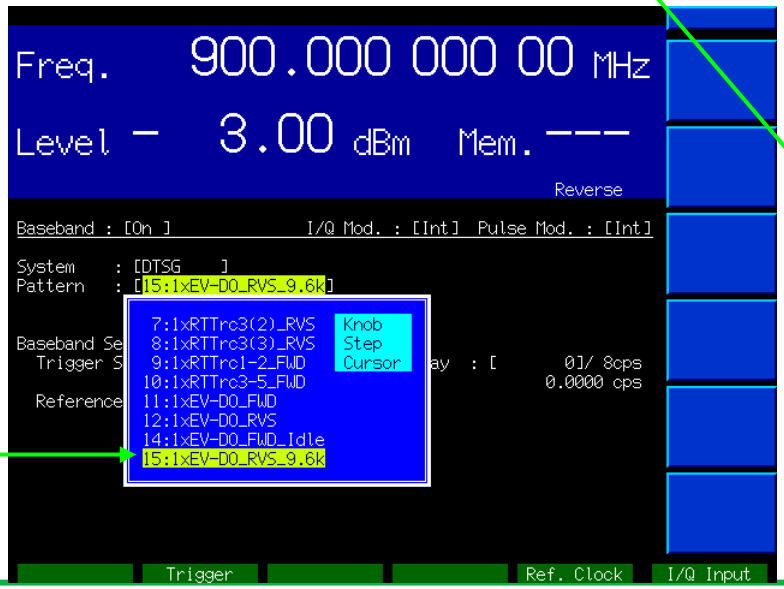
Reverse signal Setup example

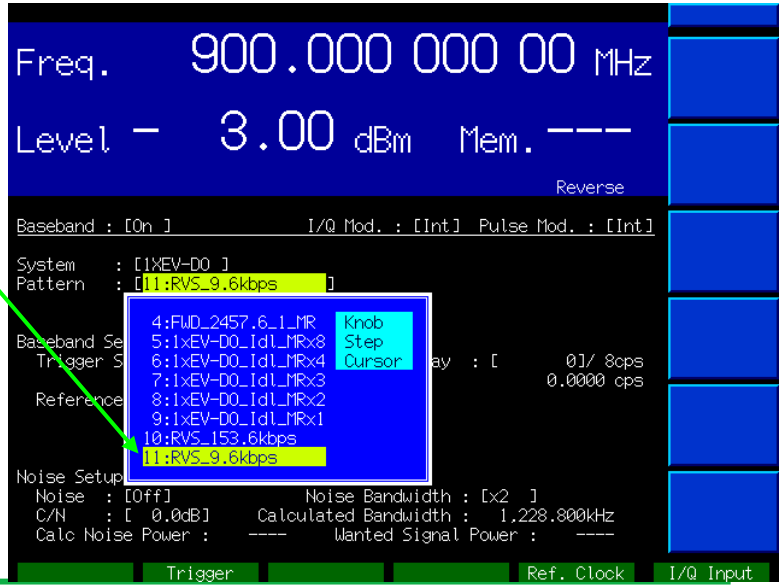
AT transmitter test

AN receiver test

- **MX368033A**
  - » 9.6 kbps
  - » 153.6 kbps
- **MX368031A**
  - » 9.6 kbps
  - » 153.6 kbps

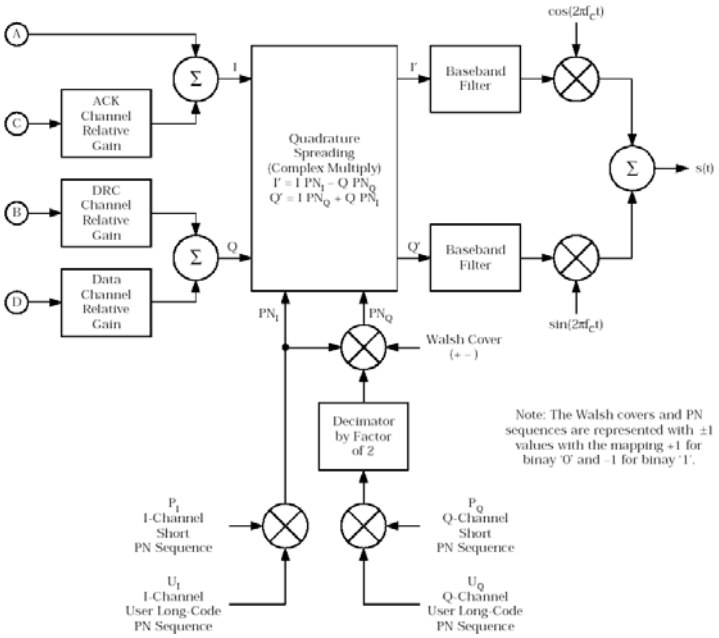






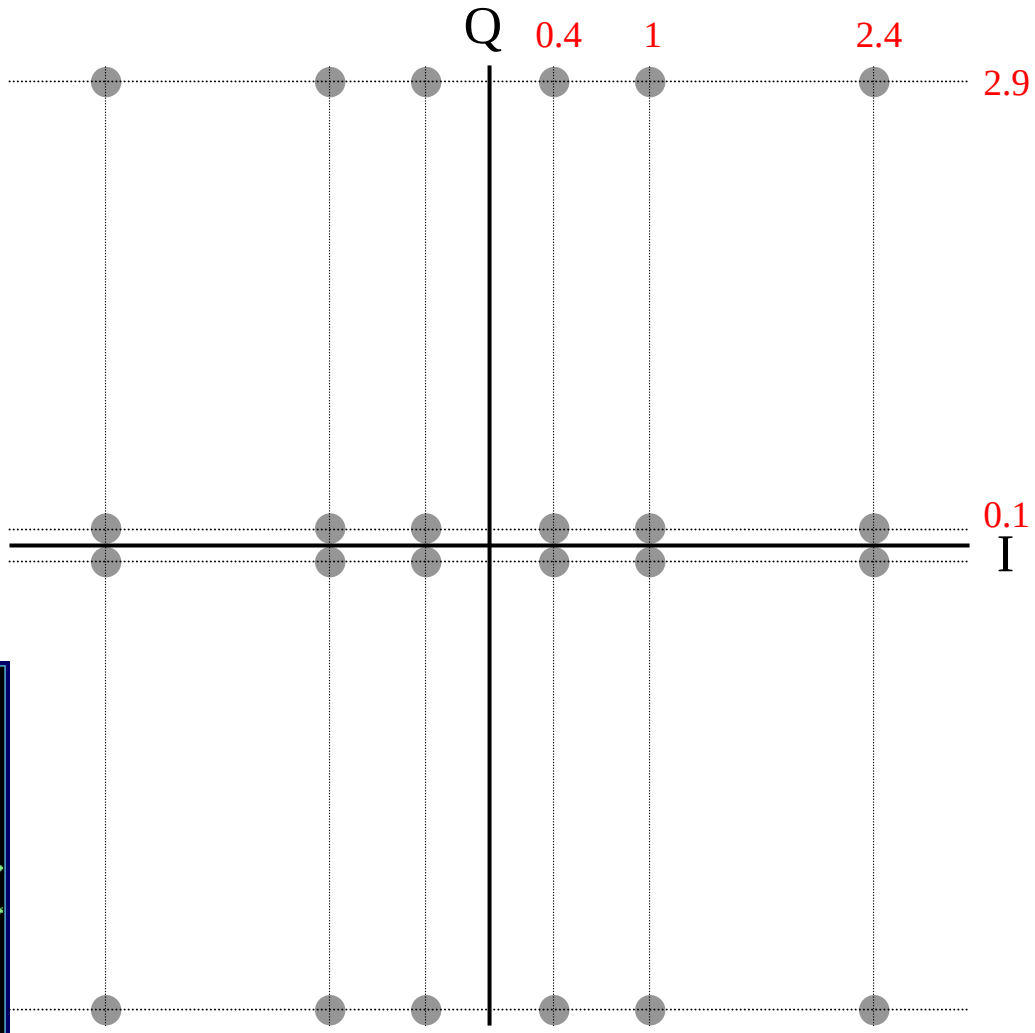
Investigation of Reverse signal (9.6 / 153.6 kbps)

- **I**
  - » Pilot Channel 0 dB
  - » ACK Channel 3 dB
- **Q**
  - » DRC Channel 3 dB
  - » Data Channel 3.75 dB (9.6 kbps)
    6.75 dB (19.2 kbps)
    9.75 dB (38.4 kbps)
    13.25 dB(76.8 kbps)
    18.5 dB (153.6 kbps)

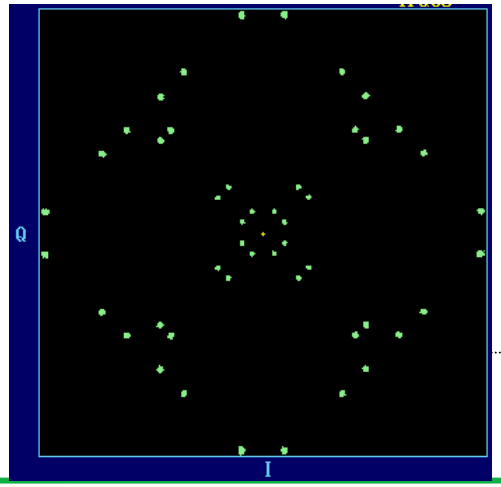


9.6 kbps Constellation

- **I**
  - » Pilot Channel 1
  - » ACK Channel ≈1.4
    - – Half-slot transmission
- **Q**
  - » DRC Channel ≈ 1.4
  - » Data Channel ≈ 1.5

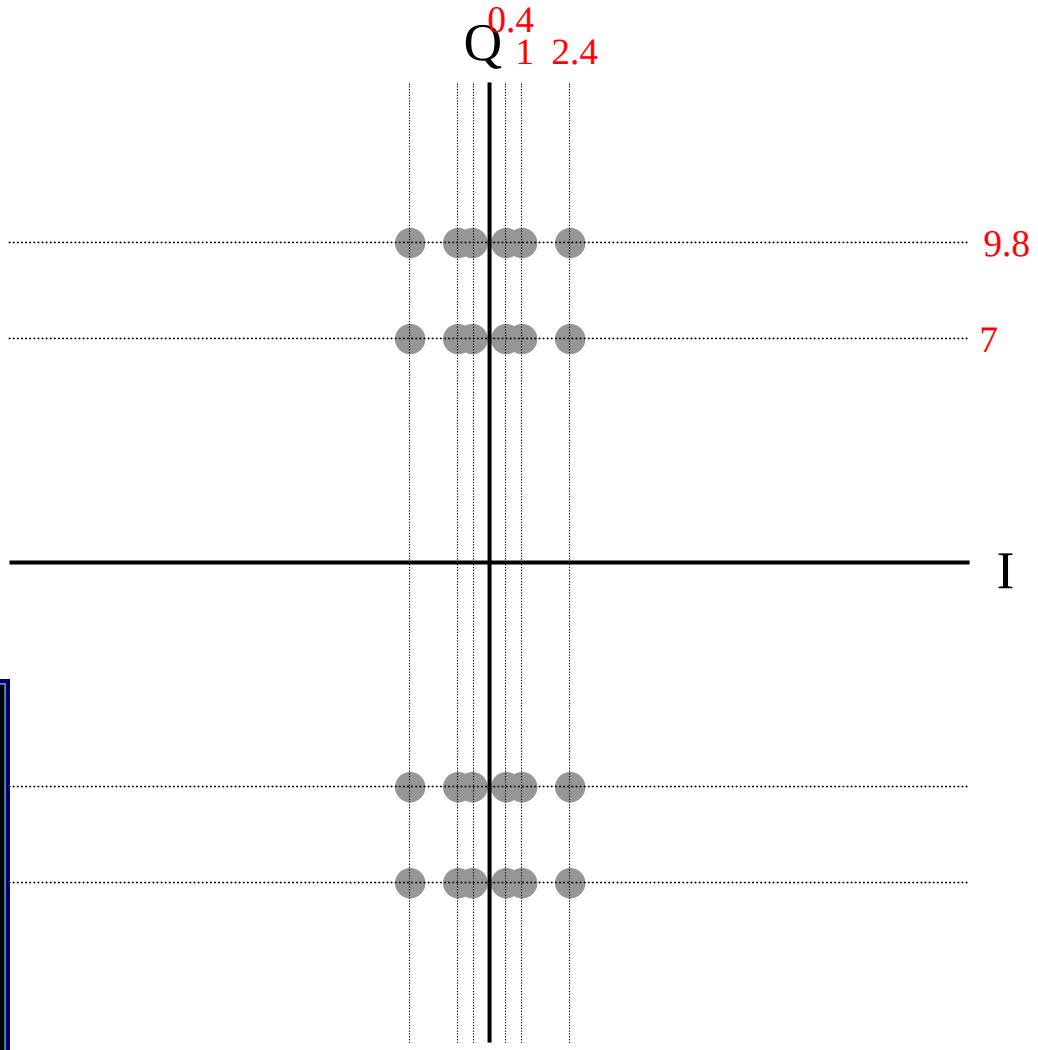


The right figure which plotted IQ inclines 45° in Spreading, and rotates 90°.

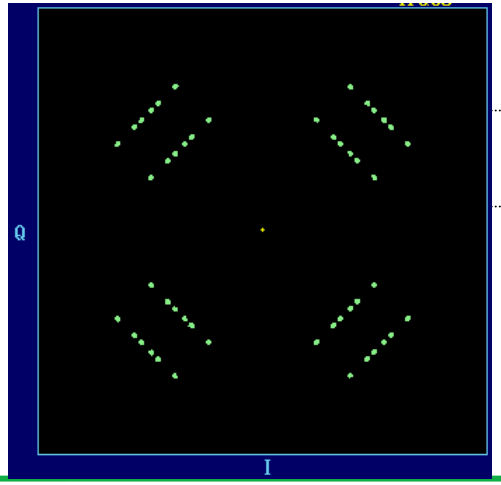


153.6 kbps Constellation

- **I**
  - » Pilot Channel 1
  - » ACK Channel ≈1.4
    - – Half-slot transmission
- **Q**
  - » DRC Channel ≈ 1.4
  - » Data Channel ≈ 8.4



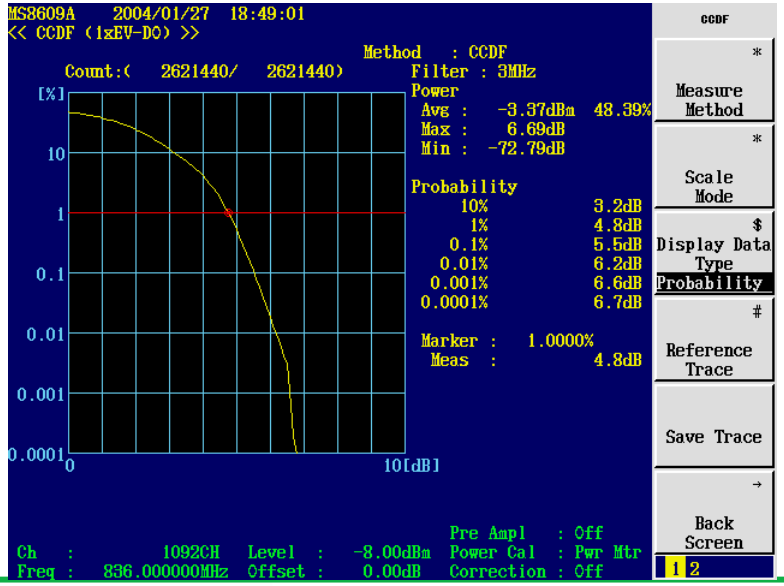
The right figure which plotted IQ inclines 45° in Spreading, and rotates 90°.



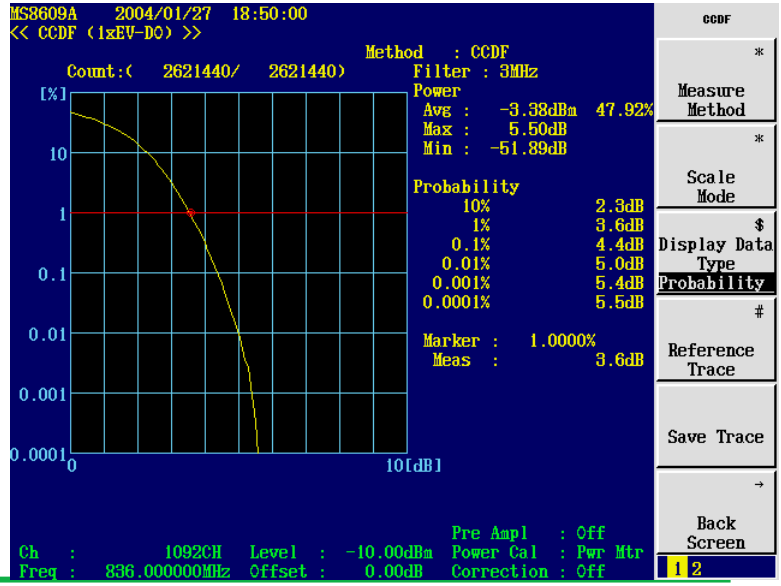
CCDF

- **On the result of Constellation, 9.6kbp side tends to generate the peak.**
- **Although specified that ρ test is 9.6 kbps and Spurious test is 153.6 kbps in 3GPP2, it is necessary to consider also 9.6 kbps which the peak tends to generate.**

9.6 kbps



153.6 kbps



CDMA2000 1X 3GPP2 BS testing

3GPP2 C.S0010 -B v1
3 Receiver Minimum Standards
4 Transmitter Minimum Standards

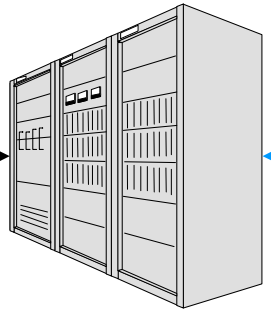
Section	Test	Wanted signal generator	Interfering signal generator	CW generator	AWGN generator	Others
3.4 3.4.1	Reverse Traffic Channel Demodulation Performance Performance in AWGN	MG3681A +MU368030A +MX368031A			MG3681A +MU368060A	MA1612A 3GHz Combiner
3.5.1	Receiver Sensitivity					
3.5.2	Receiver Dynamic Range				MG3681A +MU368060A	MA1612A 3GHz Combiner
3.5.3	Single Tone Desensitization		MG3681A or 3GHz	MG3642A 2.08GHz		
3.5.4	Intermodulation Spurious Response Attenuation		MG3681A			
3.5.5	Adjacent Channel Selectivity		MG3681A +MU368030A +MX368031A			
3.5.6	Receiver Blocking		MG3681A or 3GHz	MG3692A 20GHz or MG3642A 2.08GHz		
3.7	Received Signal Quality Indicator (RSQI)				MG3681A +MU368060A	
4.4.3	Inter-Base Station Transmitter Intermodulation		MG3681A +MU368030A +MX368031A (+MG3681A-42)			Spectrum analyzer Circulator

Inter-Base Station Transmitter Intermodulation test Connection example

Interfering signal generator
MG3681A
+MU368030A+MX368031A
(+MG3681A-42)

Circulator

Controller



Spectrum analyzer
MS8608A/8609A
+MX860803A/860903A

- Controller
  - Launches in the transmitting state by FTM Factory Test Mode control.

Receiver test Connection example

Interfering signal generator
CW generator
AWGN generator
MG3681A
+MU368030A+MX368031A
+MU368060A

Wanted signal generator
MG3681A
+MU368030A+MX368031A

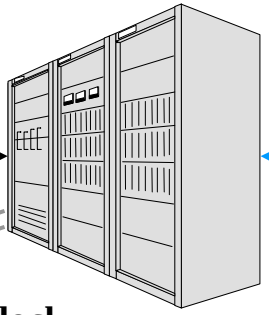
CW generator
(MG3692A)



Combiner
(MA1612A)

Start trigger

Reference clock

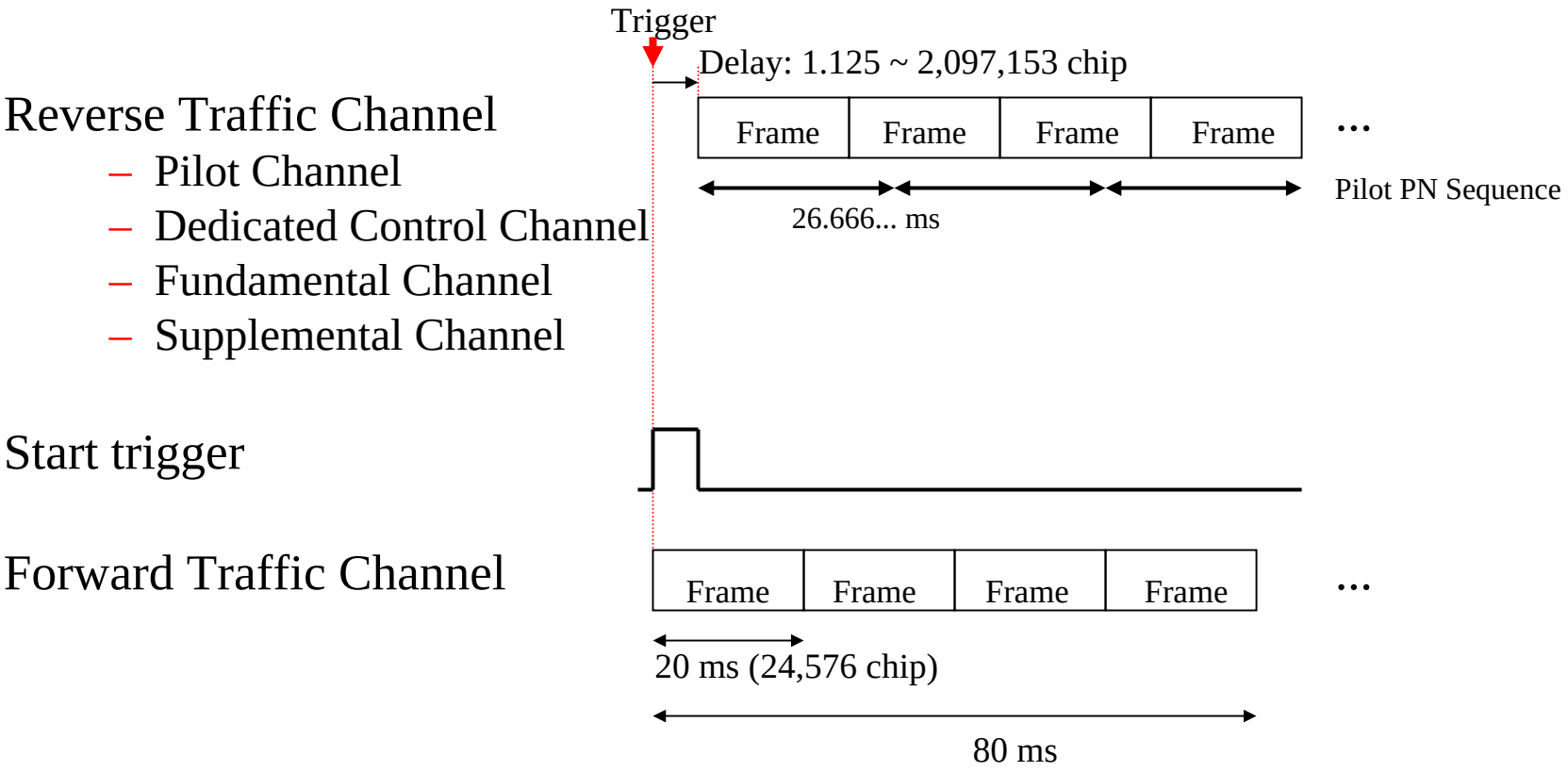


Controller
FER calculation

- Start trigger
  - Front panel [Trigger] Input
    Apply only one
    - 20 ms frame clock
    - 80 ms clock (Alignment of frame clock and zero PN offset 26.67 ms clock)
    - 2 sec clock (Even second time mark)
- Reference clock
  Apply only one
  - Front panel [Ref. Clock] Input
    - 8× 1.2288 MHz (9.8304 MHz)
  - Rear panel [10MHz/13MHz Ref] Input
    - 10 MHz, 13 MHz
- Controller
  - Launches Reverse Traffic channel in receivable state by FTM Factory Test Mode control.
  - Checks the CRC per demodulated Traffic channel frame and calculates the FER.

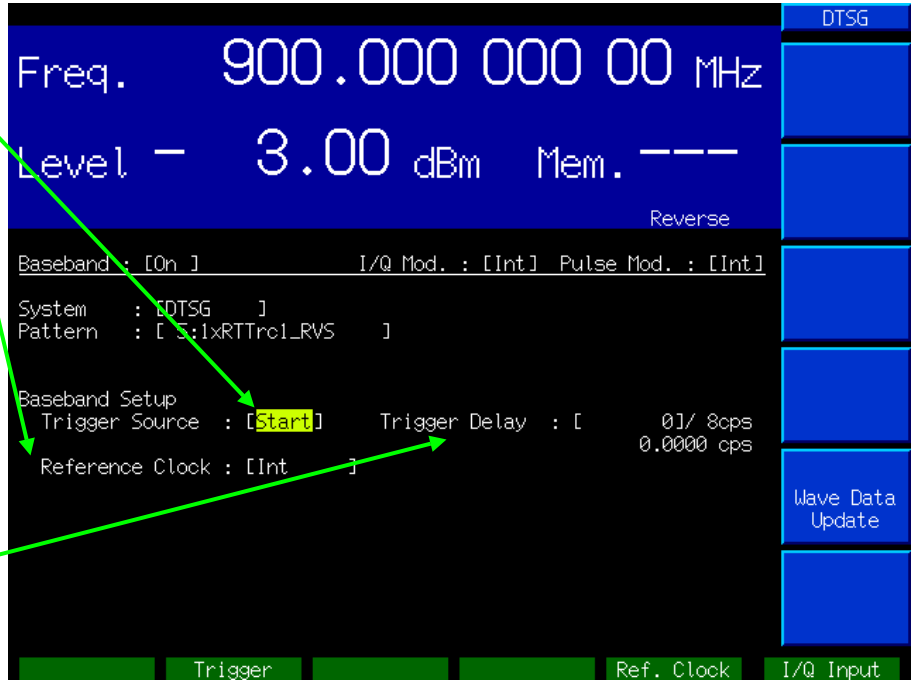
Timing synchronization Setup example

- **Start trigger delay**
  - » Set the timing to which MS can receive Reverse Traffic channel



Timing sync. Setup example

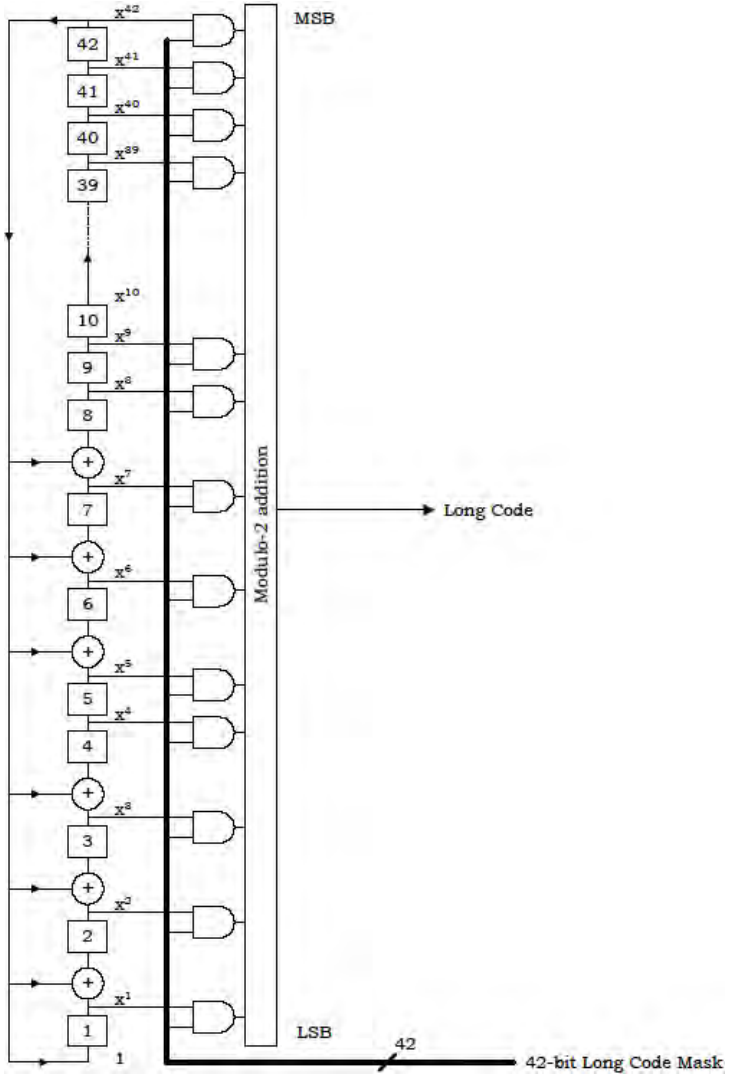
- **Setting External Start trigger**
  - » Captures/ Synchronizes the Trigger only once
- **Reference clock:**
  - » [Ref. Clock] Input applicable case
    - – Reference Clock : [Ext(TTL)]
      - 8× 1.2288 MHz (9.8304 MHz)
  - » [10MHz/13MHz Ref] Input applicable case
    - – Reference Clock : [Int]



- **Start trigger delay**
  - » 0 ~ 16,777,215 /8 chip
    1/8 chip resolution
  - » Delay from Trigger
    + 9/8 chip
    - – 1.125 ~ 2,097,153 chip

Long Code Mask sync.

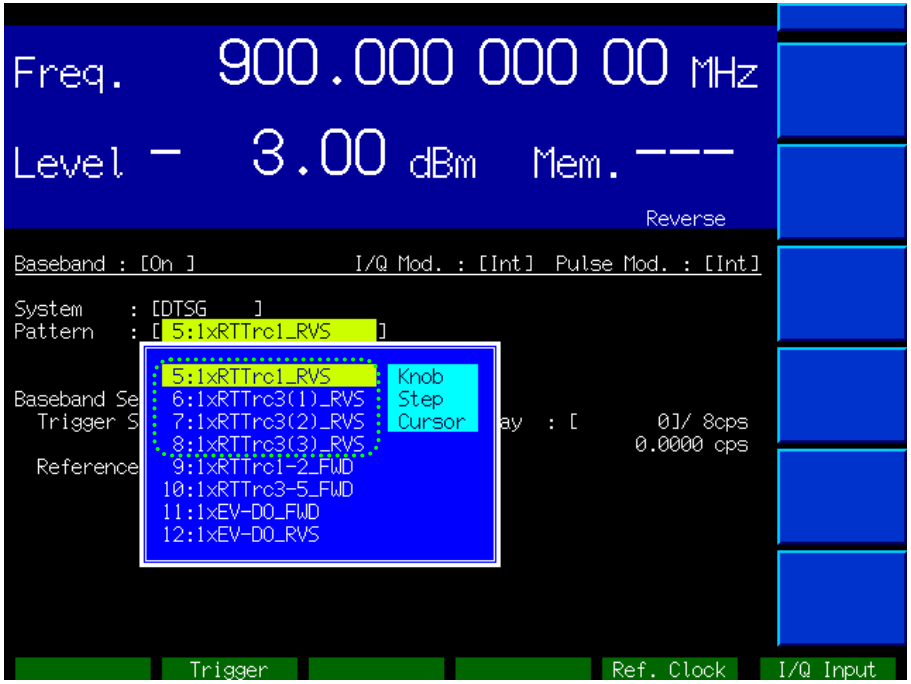
- **Reverse Traffic Channel Long Code Mask**
  - » 42-bit PN sequence
- **Setting BS**
  - » 00000000000



Wanted signal generator Setup example

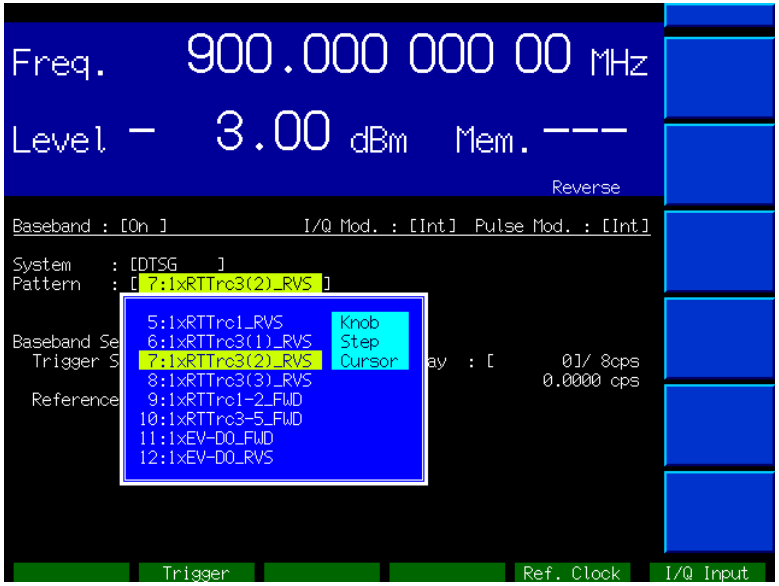
- **Reverse Traffic Channel**

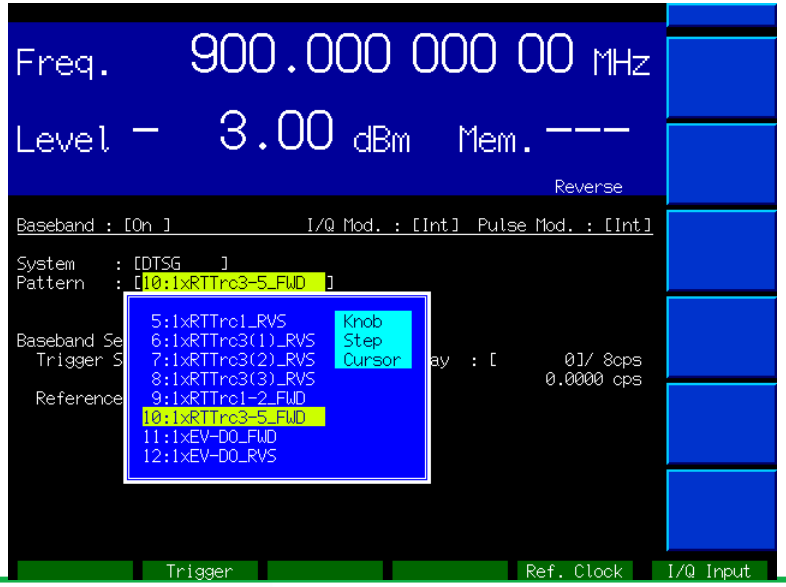
Test Mode	Forward Traffic Channel Radio Configuration	Reverse Traffic Channel Radio Configuration
1	1	1
2	2	2
3	3	3
4	4	3
5	5	4
6	6	5
7	7	5
8	8	6
9	9	6

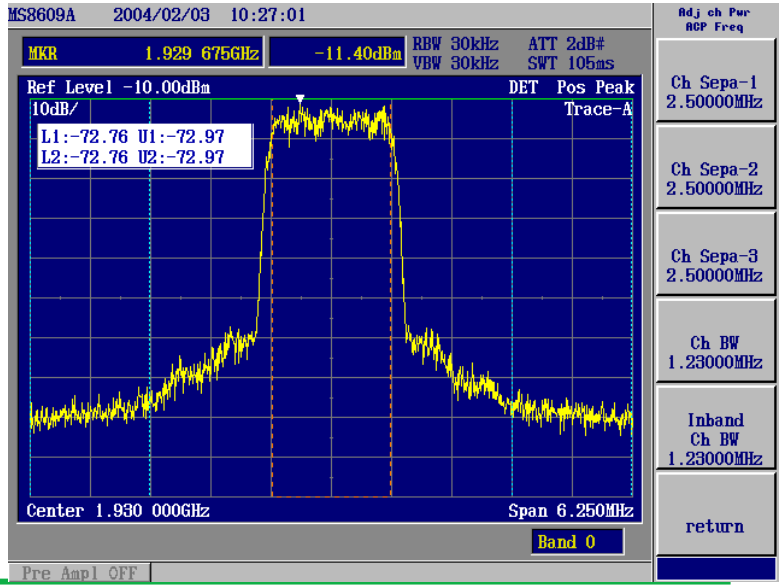


Interfering signal generator Setup example

- **RC 3 signal**
  - » Adjacent Channel Selectivity test
- **External Base Station**
  - » Inter-Sector Transmitter Intermodulation test

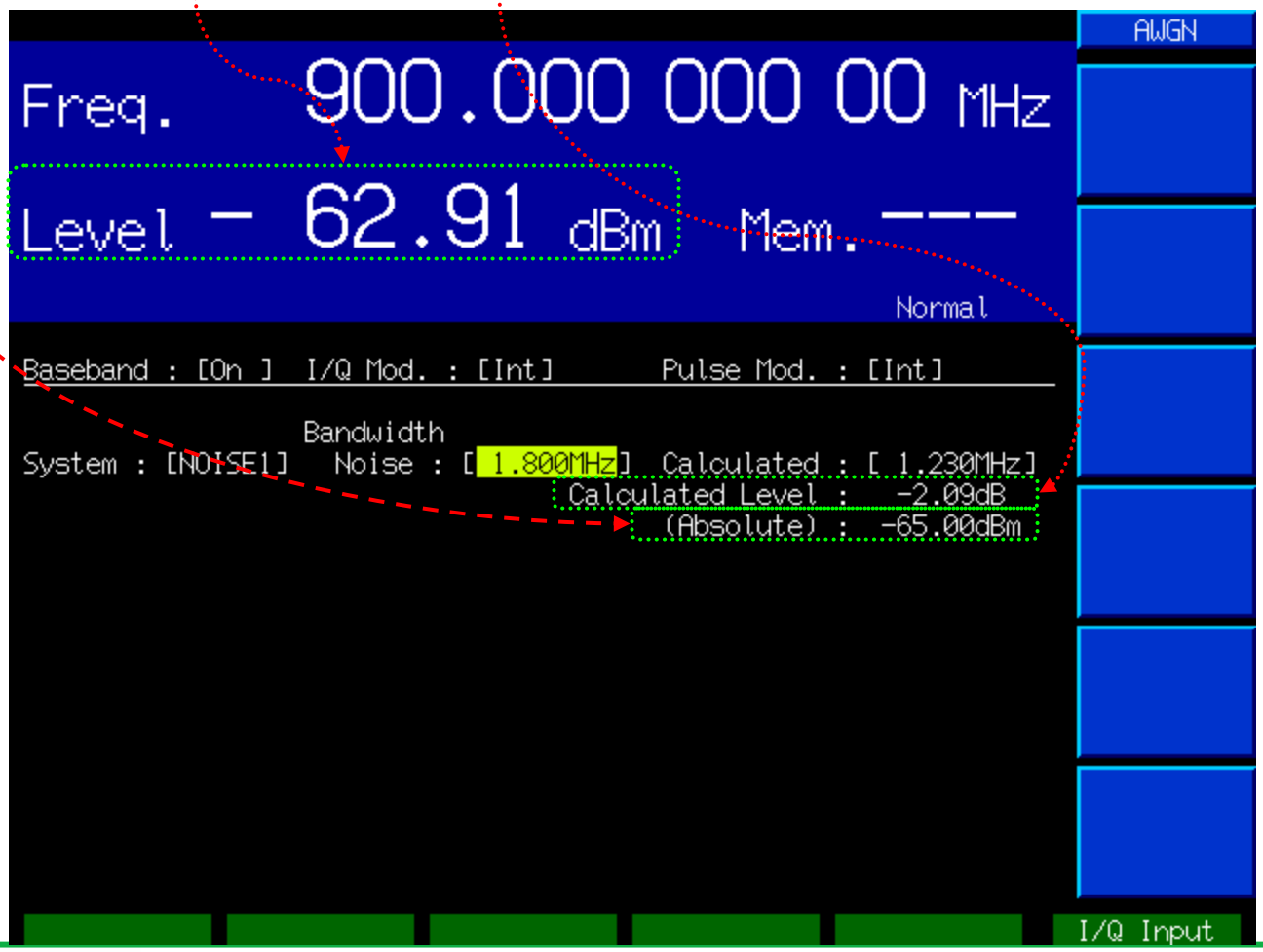






AWGN generator Setup example

- **AWGN source**
  - » Ioc = Total level + Bandwidth level

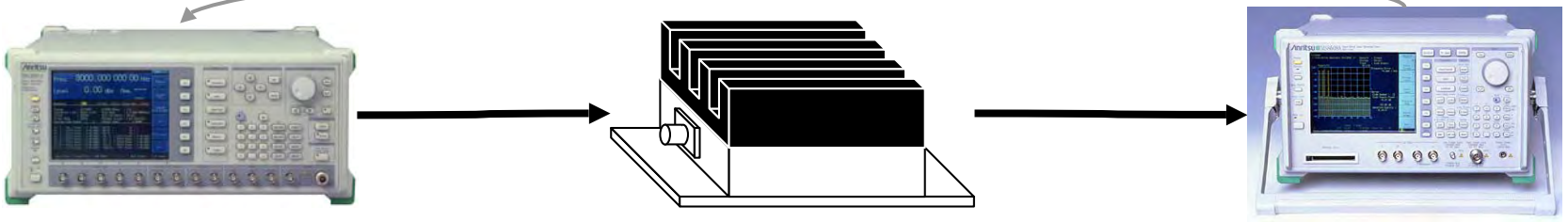


RF/IF components test　Connection example

Signal source
MG3681A
+MU368030A+MX368031A
or
+MU368040A+MX368042A

Signal analyzer
(MS8600/MS2680)

Reference clock



Forward signal Setup example

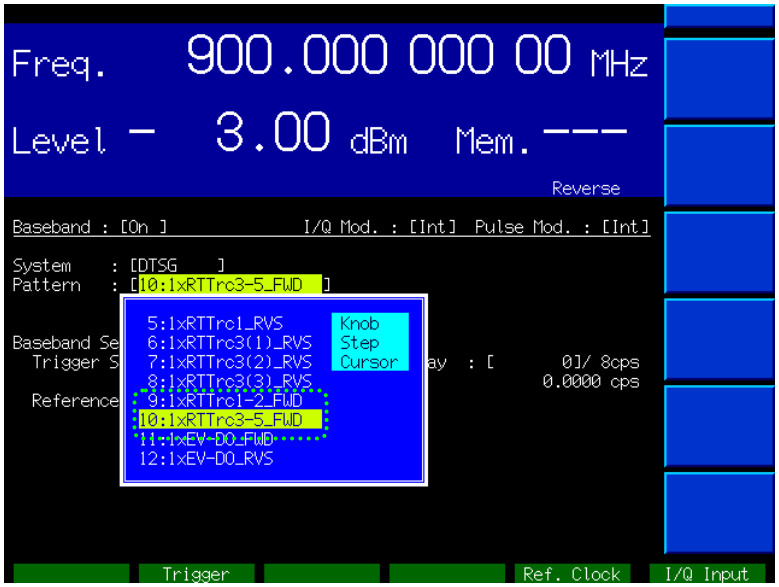
BS transmitter test

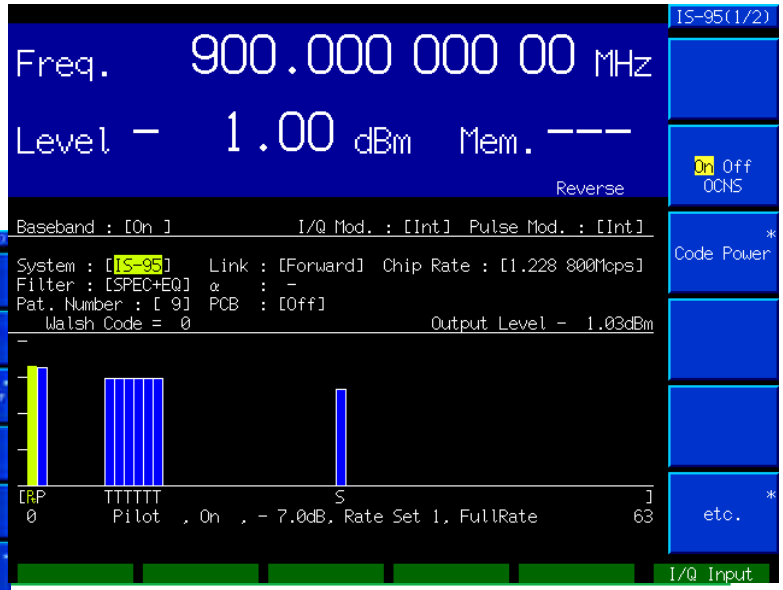
MS receiver test

- **MX368031A**
  - » RC 1/2
  - » RC 3/4/5

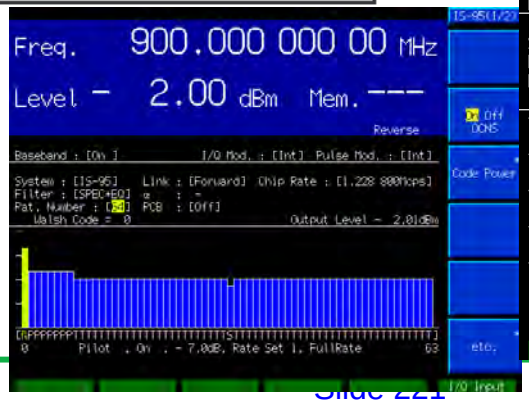
Table 6.5.2-3. Base Station Test Model, General

Channel Type	Relative Power
Pilot	0.2 of total power (linear)
Sync+Paging+Traffic	Remainder (0.8) of total power (linear)
Sync	3 dB less than one Fundamental Traffic Channel; always 1/8 rate
Paging	3 dB greater than one Fundamental Traffic Channel; full rate only
Traffic	Equal power in each Fundamental Traffic Channel; full rate only



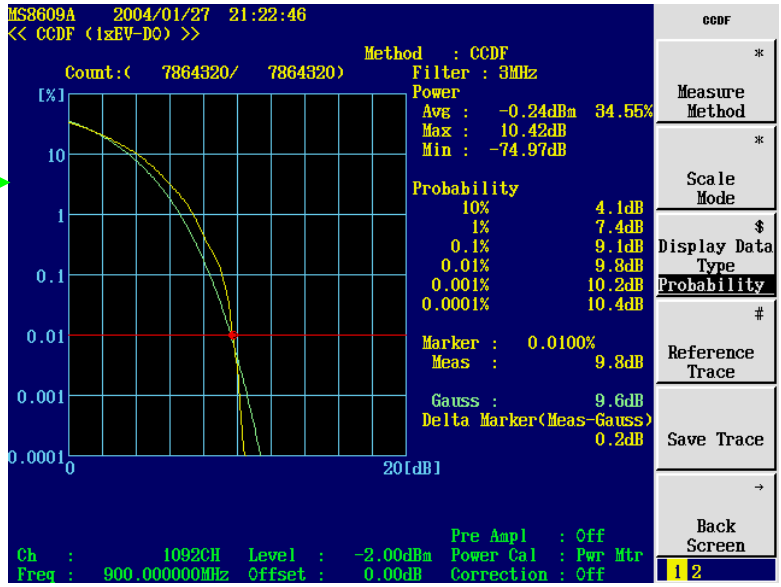


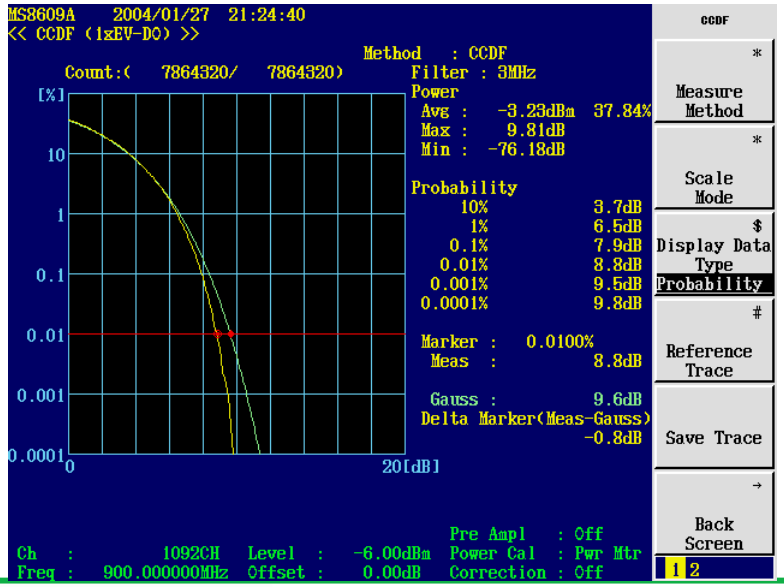
- **MX368042A**
  - » RC 1
  - » RC 2

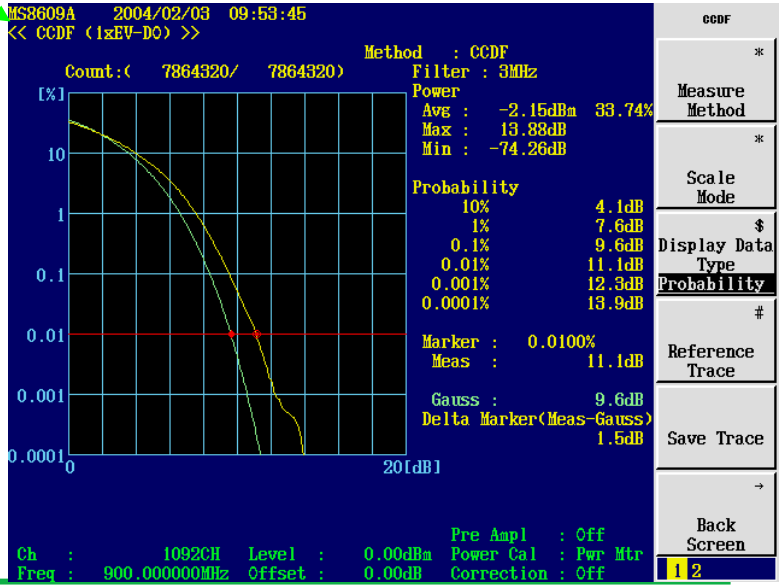


CCDF

- **RC 1/2**
  - » 9 channels
  - » 64 channels
- **RC 3/4/5**







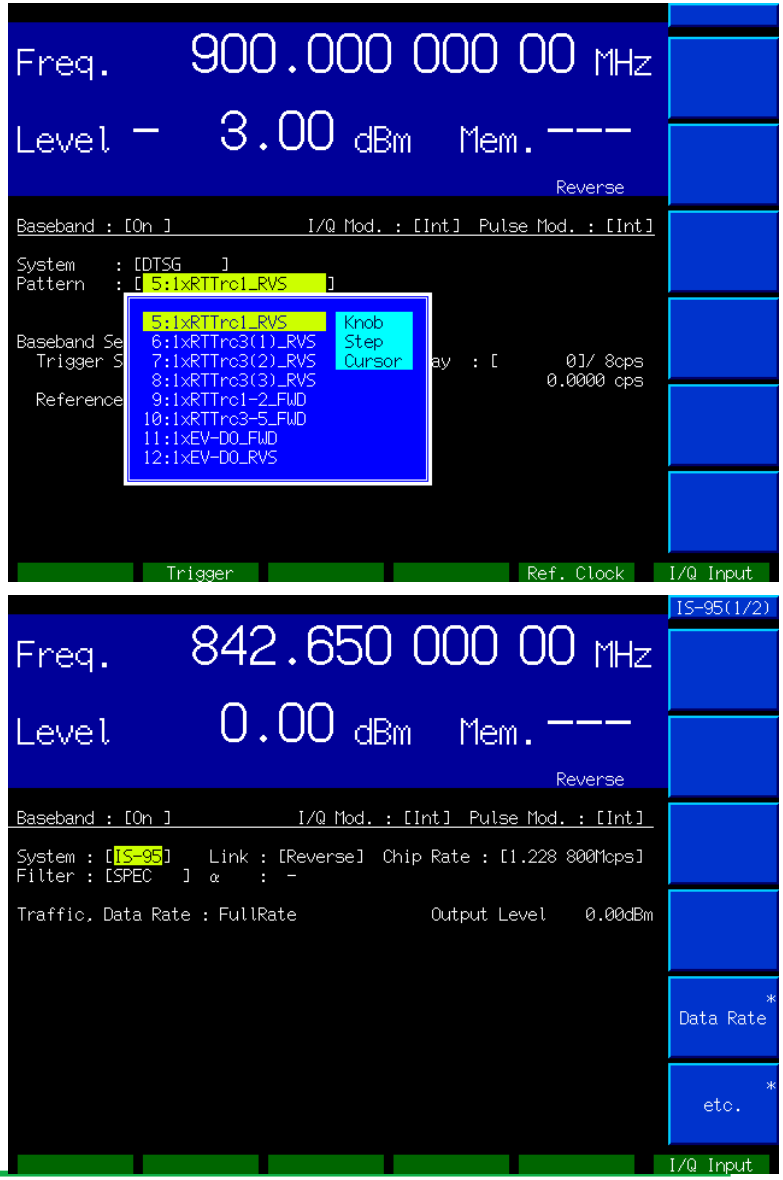
Reverse signal Setup example

MS transmitter test

BS receiver test

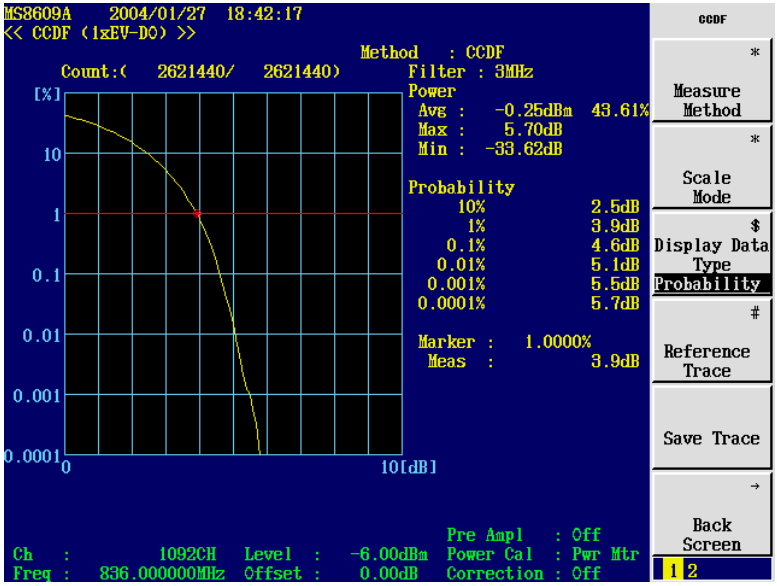
- **MX368031A**
  - » RC 1
  - » RC 3
    - – FCH + PICH
    - – FCH + SCH + PICH
    - – DCCH + PICH

- **MX368042A**
  - » RC 1



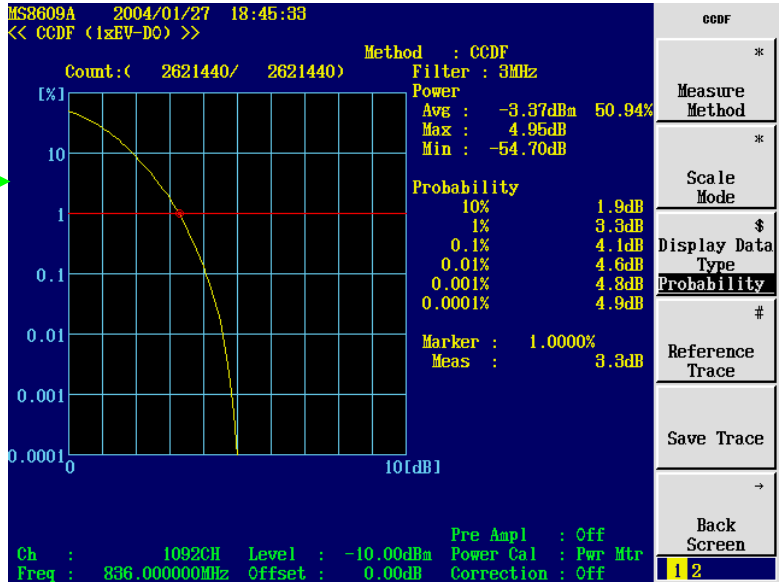
CCDF

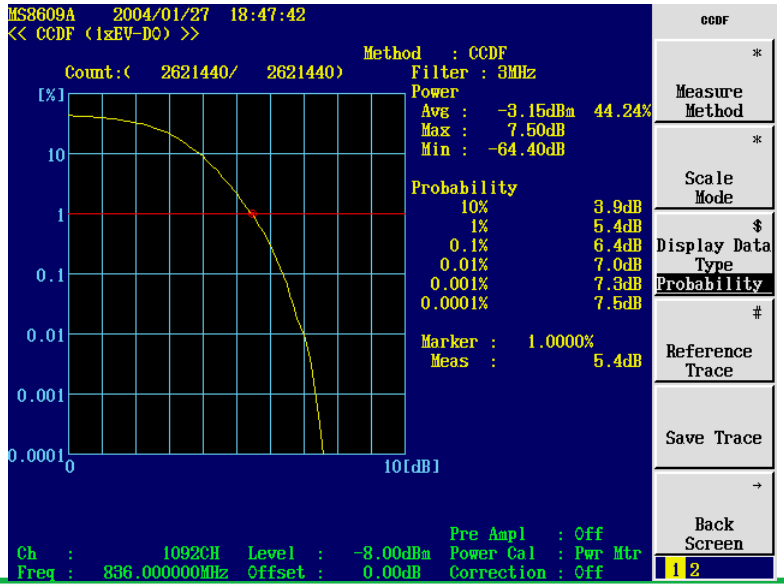
- **RC 1/2**

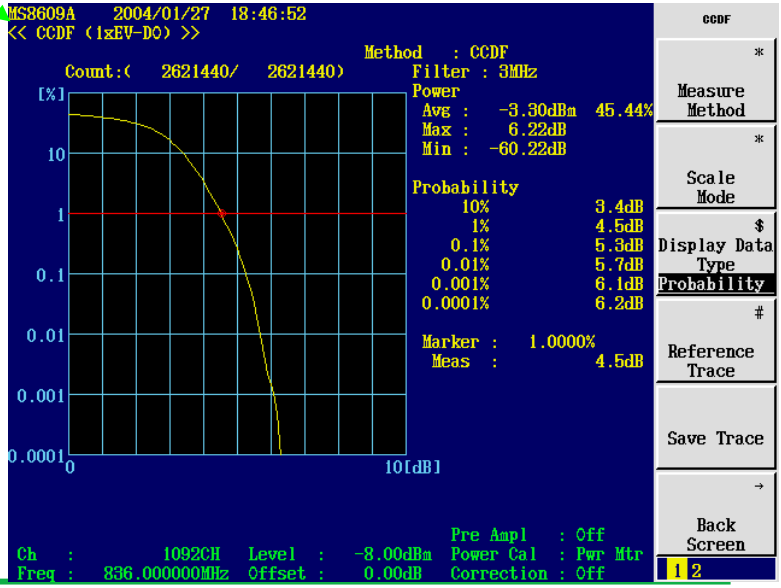

MS8609A 2004/01/27 18:42:17
<< CCDF (1xEV-DO) >>
Method : CCDF
Count:(2621440/ 2621440) Filter : 3MHz
Power
Avg : -0.25dBm 43.61%
Max : 5.70dB
Min : -33.62dB
Probability
10% 2.5dB
1% 3.9dB
0.1% 4.6dB
0.01% 5.1dB
0.001% 5.5dB
0.0001% 5.7dB
Marker : 1.0000%
Meas : 3.9dB
[%]
10
1
0.1
0.01
0.001
0.0001
0
10[dB]
Ch : 1092CH Level : -6.00dBm Pre Ampl : Off
Freq : 836.000000MHz Offset : 0.00dB Power Cal : Pwr Mtr
Correction : Off
CCDF
Measure Method
Scale Mode
Display Data Type
Probability
Reference Trace
Save Trace
Back Screen
1 2

CCDF

- **RC 3**
  - » FCH + PICH
  - » FCH + SCH + PICH
  - » DCCH + PICH





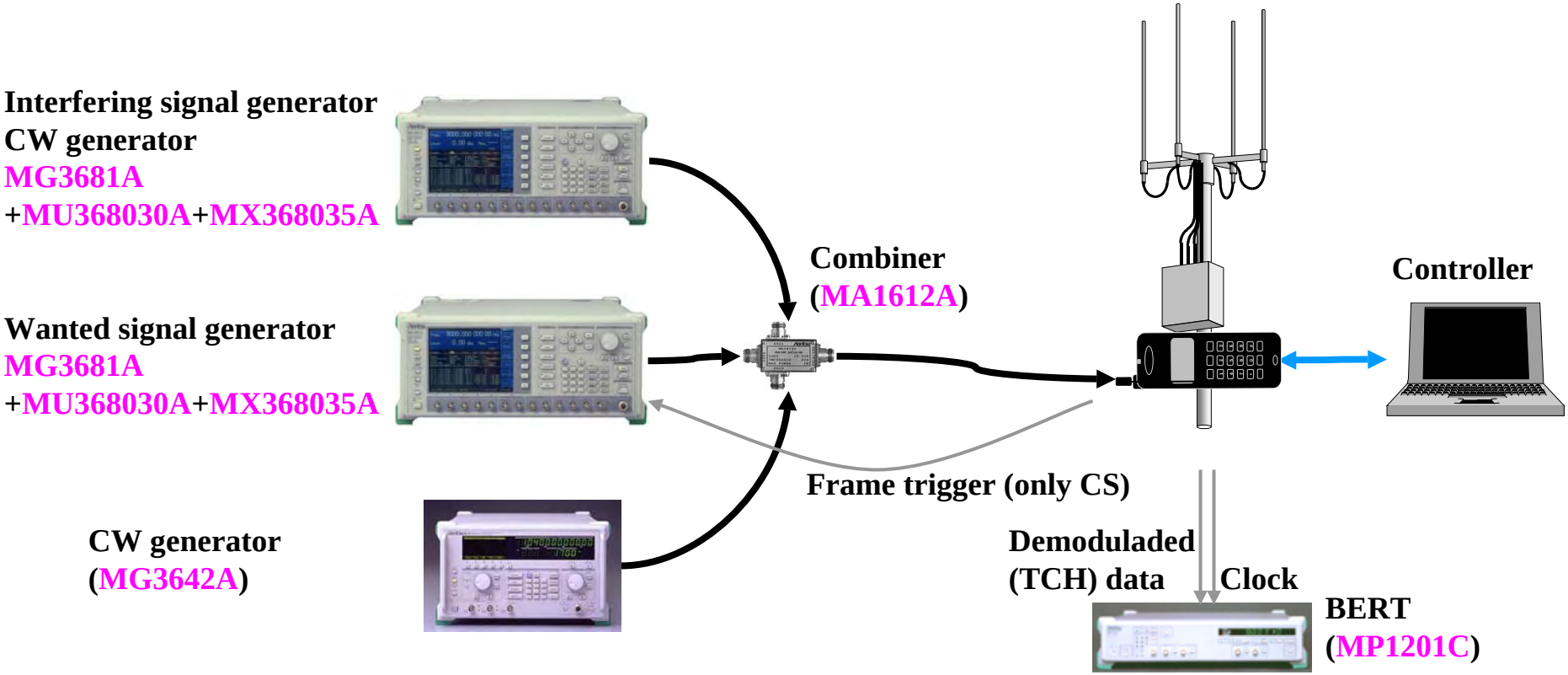


PHS RCR STD-28 CS/PS testing

RCR STD-28 V4.0
3.4.3 7.2 Receiver Test

Requirements	Meas. Methods	Test	Wanted signal generator	Interfering signal generator	CW generator	BERT	Others
3.4.3.2	7.2.1	Sensitivity	MG3681A +MU368030A +MX368035A			MP1201C	
3.4.3.4	7.2.2	Adjacent channel selectivity		MG3681A +MU368030A +MX368035A			MA1612A 3GHz
3.4.3.5	7.2.3	Intermodulation characteristics		MG3681A	MG3642A		
3.4.3.6	7.2.4	Spurious response		MG3681A or 3GHz	MG3642A 2.08GHz		
3.4.3.9	7.2.8 7.2.8.3	Receive signal strength indicator accuracy Reception level value is display					
3.4.3.10	7.2.9	Bit error rate floor characteristics				MP1201C	

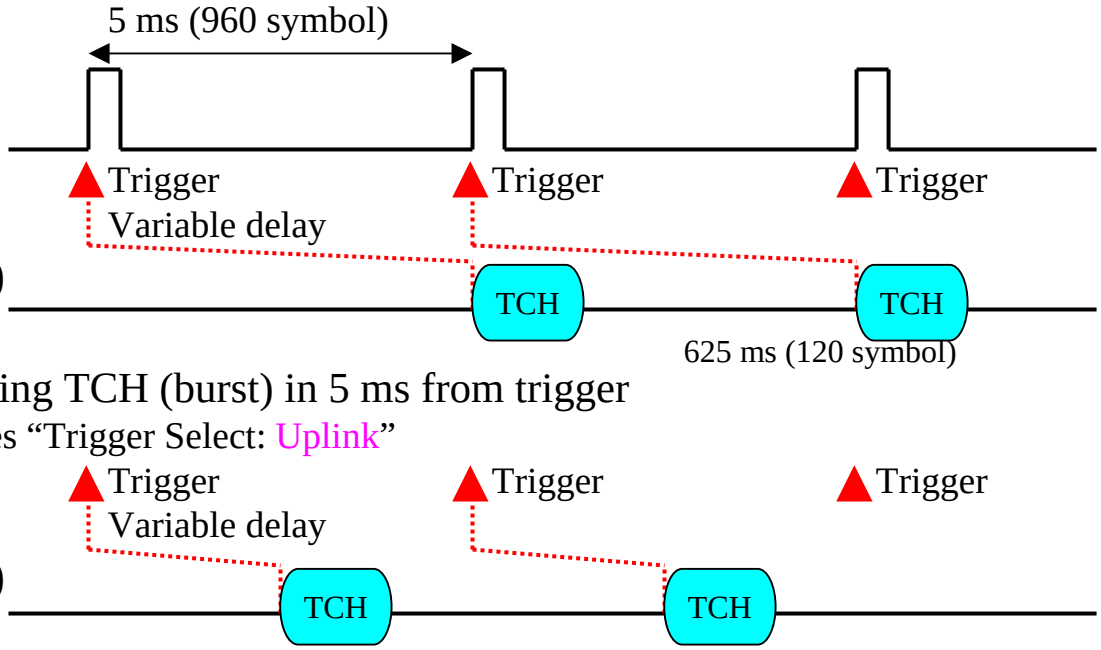
Receiver test Connection example



- Frame trigger
  - Front panel [Trigger] Input
    - 5 ms clock
- Controller
  - Launches TCH in the receivable state by FTM Factory Test Mode control.

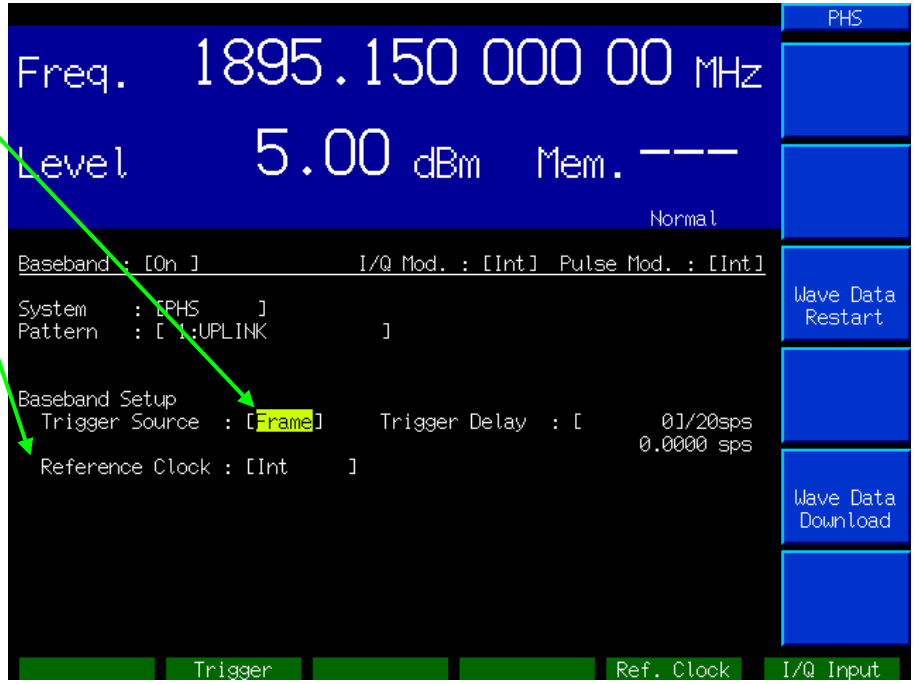
CS receiver Timing sync. Setup example

- **Frame trigger delay**
  - » Set the timing to which CS can receive Uplink TCH
    - – Frame trigger Input
    - – Uplink TCH (burst) Output
      - In case of outputting TCH (burst) in 5 ms from trigger
        - – MG3670 series “Trigger Select: Uplink”
    - – Uplink TCH (burst) Output
      - In case of outputting TCH (burst) in 2.5 ms from trigger
        - – MG3670 series “Trigger Select: Downlink”



CS receiver Timing sync. Setup example

- **Setting External Frame trigger**
  - » Captures/ Synchronizes the Trigger of 5 ms clock
- **Reference clock:**
  Apply to cancel the jitter of within ±1/20 symbol of synchronous errors
  - – MG3670 series is the jitter within ±1/16 symbol
  - » [Ref. Clock] Input applicable case
    - – Reference Clock : [Ext(TTL)]
      - 20× 192 kHz (3,840 kHz)
  - » [10MHz/13MHz Ref] Input applicable case
    - – Reference Clock : [Int]

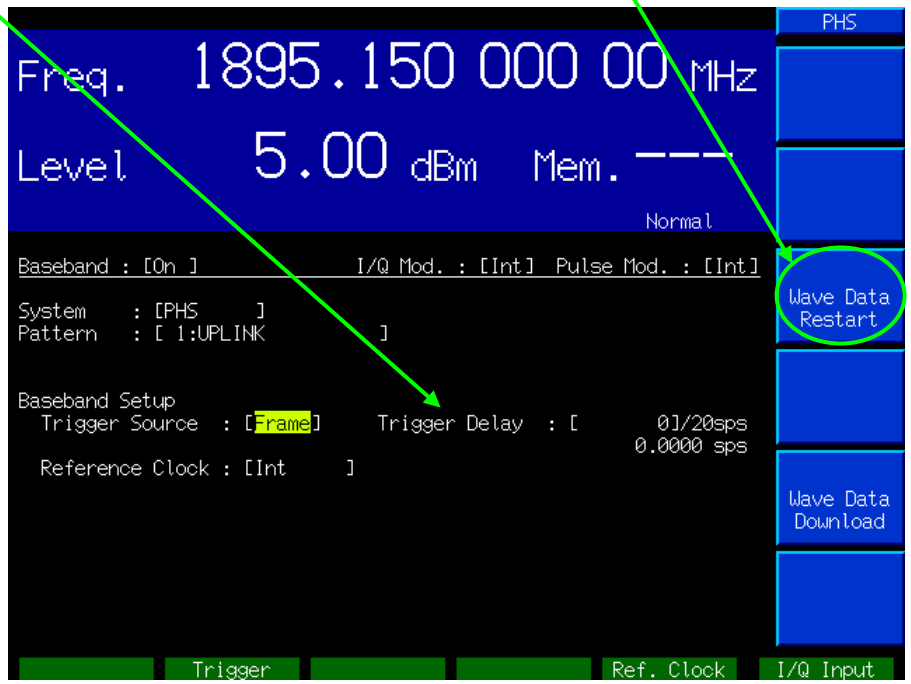


CS receiver Timing sync. Setup example

- **Frame trigger delay**
  - » 0 ~ +16,777,215 /20 symbol
    1/20 symbol
    resolution
  - » Delay from trigger
    + 2.55 symbol
    – 2.55 ~ 838,863.3 symbol

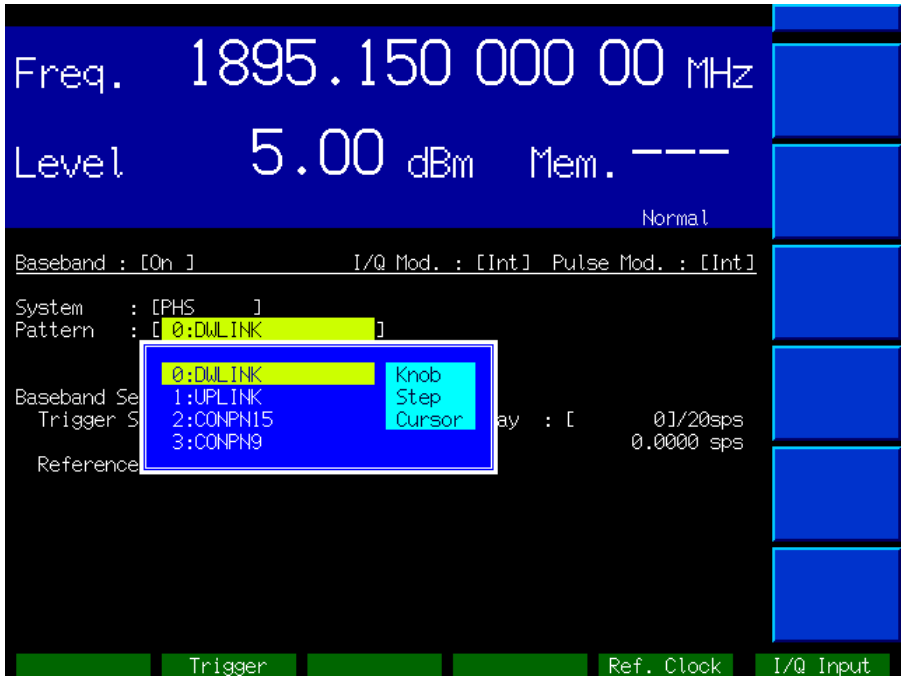
  e.g.
  - » In case of outputting TCH (burst) in 5 ms from trigger
    - 19,149 /20 symbol
    – Equivalent to MG3670 series “Trigger Select: Uplink”
      - 19,171 /20 symbol
        – + 0.614 + 0.5 symbol
  - » In case of outputting TCH (burst) in 2.5 ms from trigger
    - 9,549 /20 symbol
    – Equivalent to MG3670 series “Trigger Select: Downlink”
      - 9,571 /20 symbol
        – + 0.614 + 0.5 symbol

- **Trigger recapture/ synchronization**



Wanted/Interfering signal generator Setup example

- **Wanted signal generator**
  - » CS test
    - – Uplink
  - » PS test
    - – Downlink
- **Interfering signal generator**
  - – CONPN15

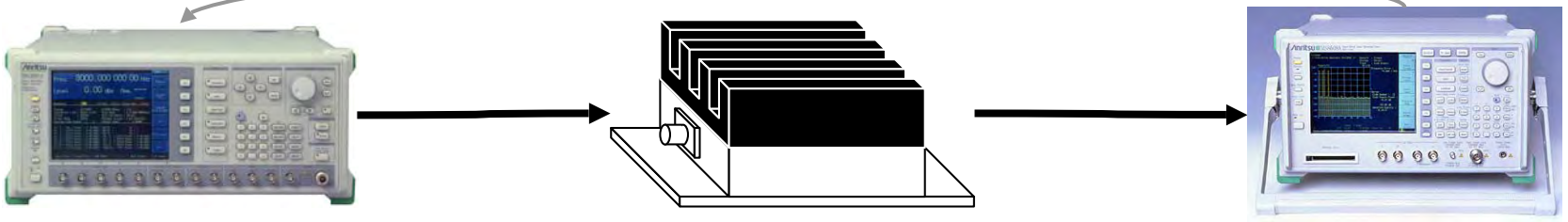


RF/IF components test　Connection example

Signal source
MG3681A
+MU368030A+MX368035A
or
+MU368030A+MX368031A

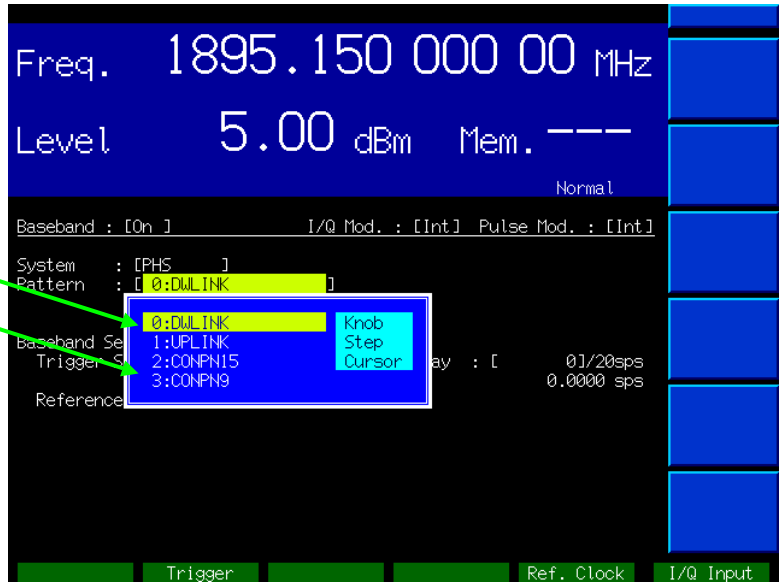
Signal analyzer
(MS8600/MS2680)

Reference clock

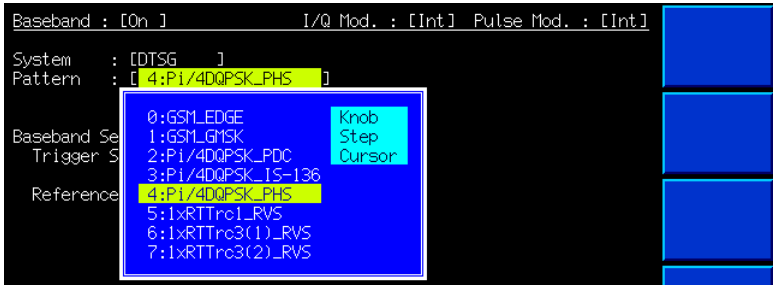


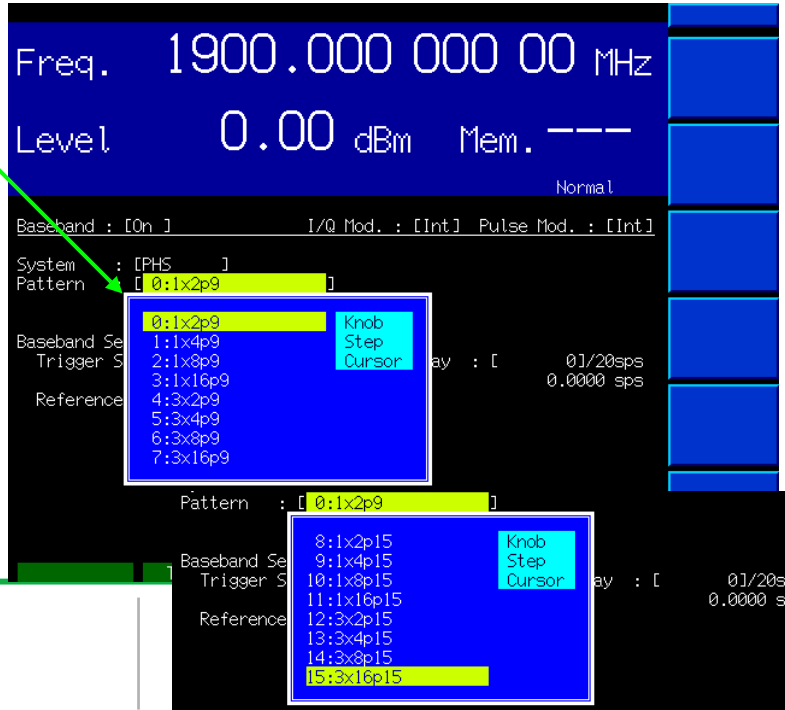
Signal Setup example

- **MX368035A**
  - » π/4DQPSK modulation
    - – TCH (burst) format
    - – Continuous modulation format
  - » 16QAM modulation
  - » 8PSK modulation
  - » QPSK modulation
  - » BPSK modulation
    - – Continuous modulation format



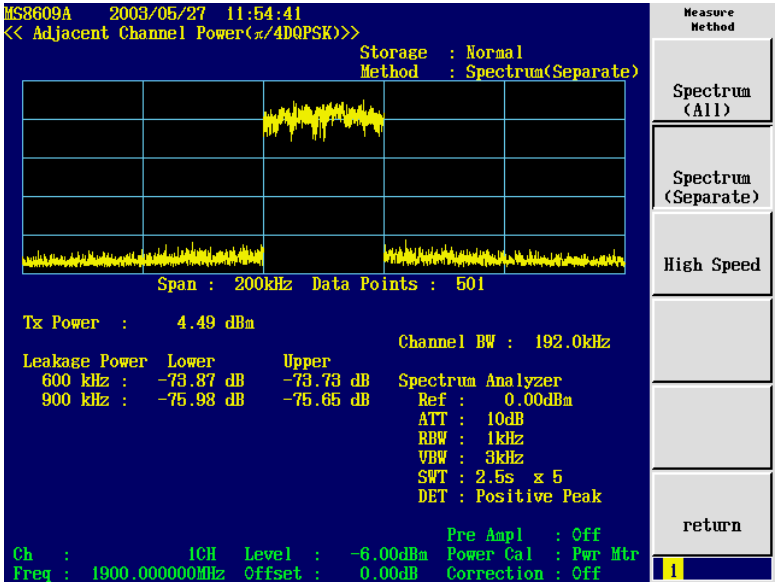
- **MX368031A**
  - » π/4DQPSK modulation
    - – Continuous modulation format



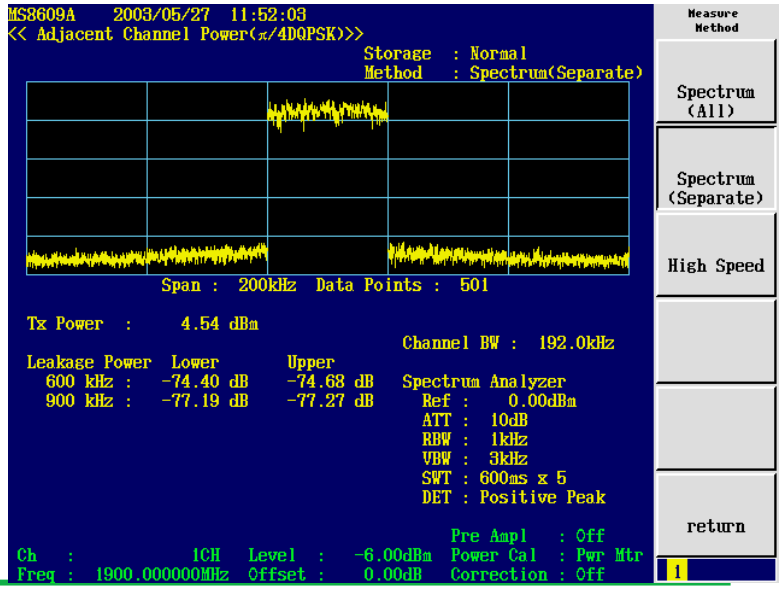


Contrast of typical ACLR

- **Burst (TCH) format**
  - » 600 kHz: +0.5 ~ +1 dB
  - » 900 kHz: +1 ~ +2 dB



- **Continuous modulation format**



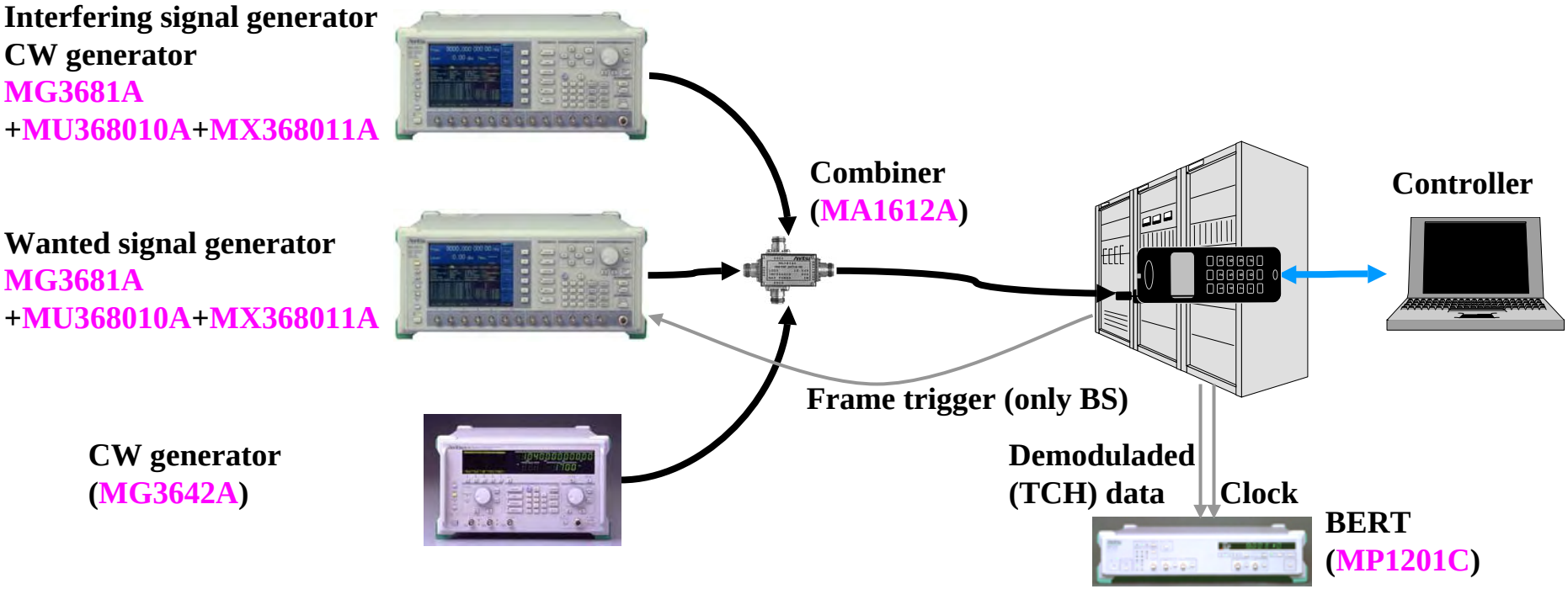
PDC RCR STD-27 BS/MS testing

RCR STD-27K

3.4.3 6.2 Receiver Test

Requirements	Meas Methods	Test	Wanted signal generator	Interfeing signal generator	CW generator	BERT	Others
3.4.3.2	6.2.1	Sensitivity	MG3681A +MU368010A +MX368011A			MP1201C	
3.4.3.4	6.2.2	Adjacent channel selectivity		MG3681A +MU368010A +MX368011A			MA1612A 3GHz
3.4.3.5	6.2.3	Intermodulation characteristics		MG3681A	MG3642A 2.08GHz		
3.4.3.6	6.2.4	Spurious response		MG3681A or 3GHz			
3.4.3.8	6.2.6	Interference level (CIR)		MG3681A +MU368010A +MX368011A			
3.4.3.10	6.2.8	Reception level detection					
3.4.3.11	6.2.9	Network quality detection accuracy				MP1201C	

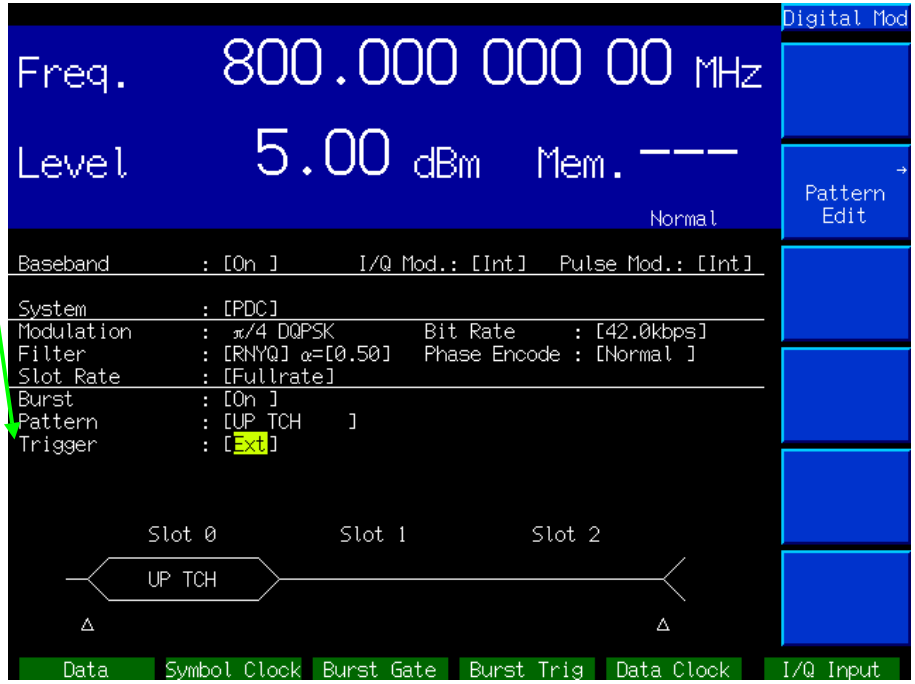
Receiver test Connection example



- Frame trigger
  - Front panel [Burst Trig] Input
    - 20 ms clock (Full rate), 40 ms clock (Half rate)
- Controller
  - Launches TCH in the receivable state by FTM Factory Test Mode control.

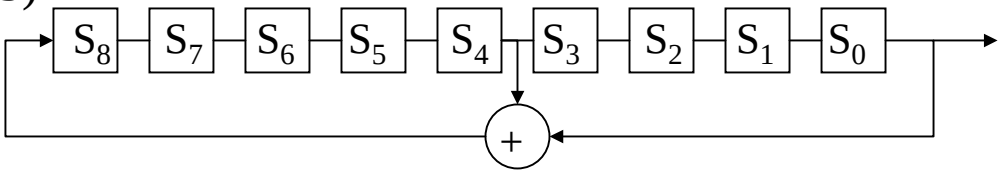
BS receiver Timing sync. Setup example

- **Setting External Frame trigger**
  - » Captures/ Synchronizes the Trigger of 20 ms clock (Full rate)/ 40 ms clock (Half rate)
- **[10MHz/13MHz Ref] Input:**
  Apply to cancel the jitter of within ±1/16 symbol of synchronous errors
  - – MG3670 series is the jitter within ±1/16 symbol

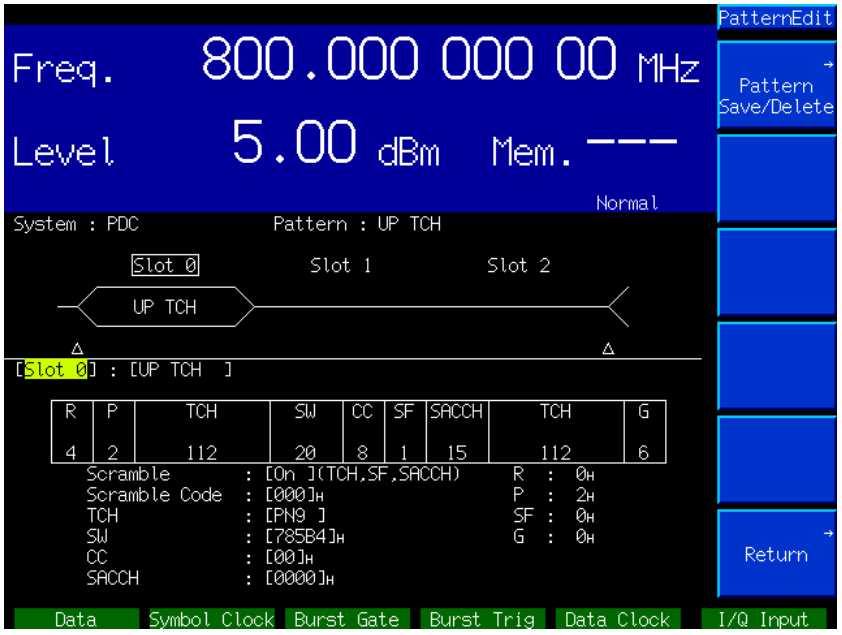


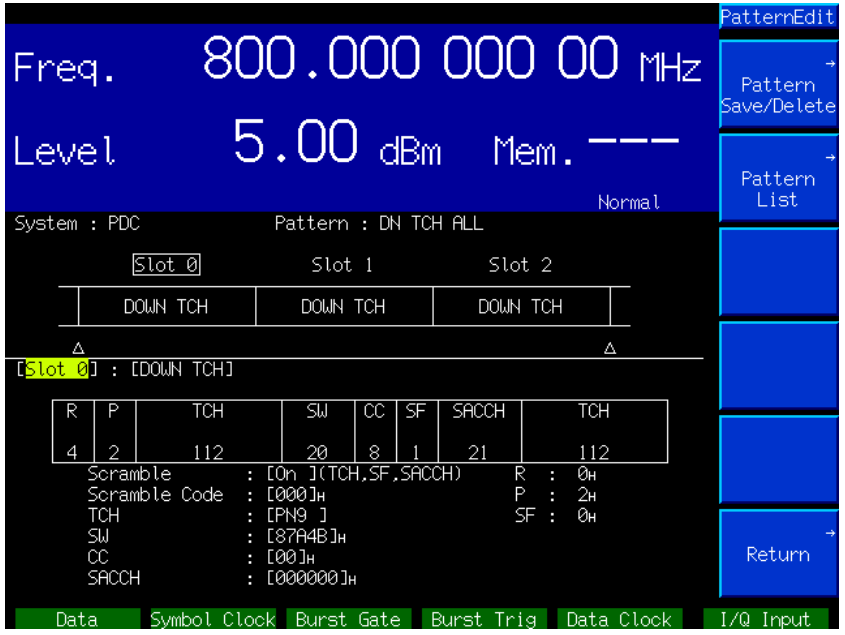
Scramble pattern sync. Setup example

- **Scramble pattern**
  - » PN(9,5)



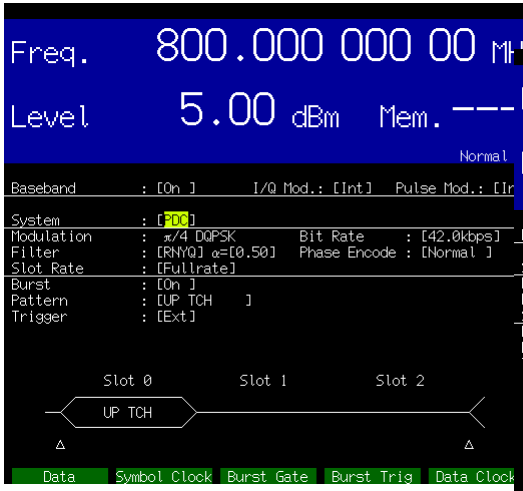
  - » Register initial data(S_8 ~ S_0) = CC

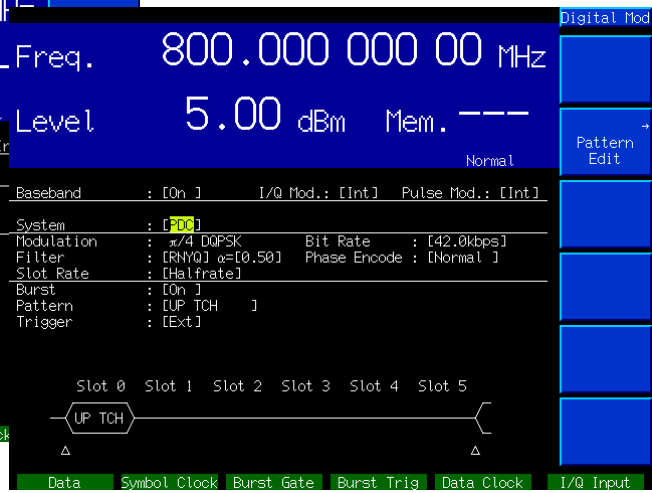




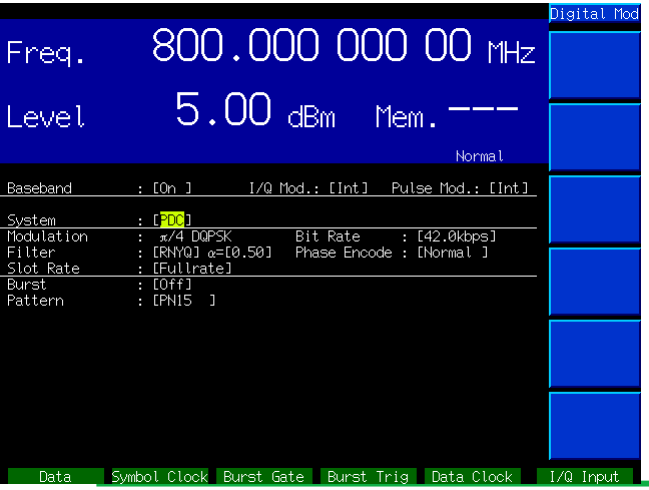
Wanted/Interfering signal generator Setup example

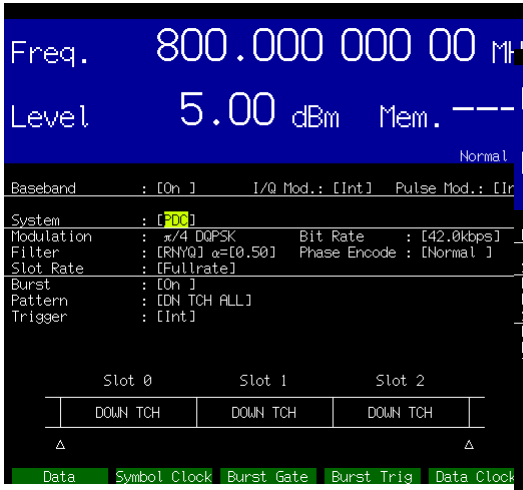
- **Wanted signal generator**
  - » BS test
    - – UP TCH
  - » MS test
    - – DN TCH ALL

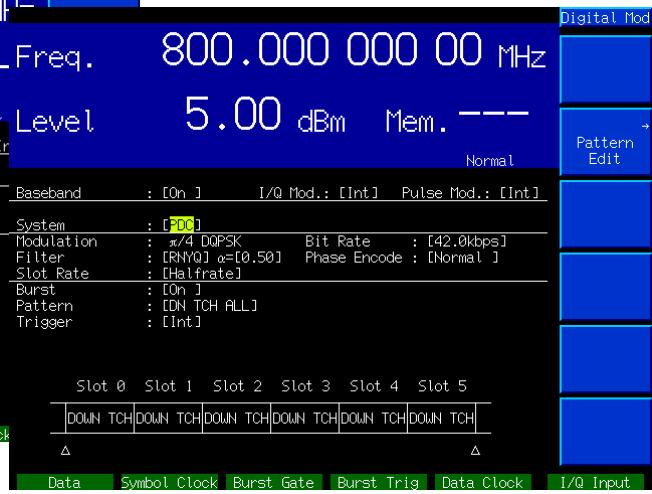




- **Interfering signal generator**

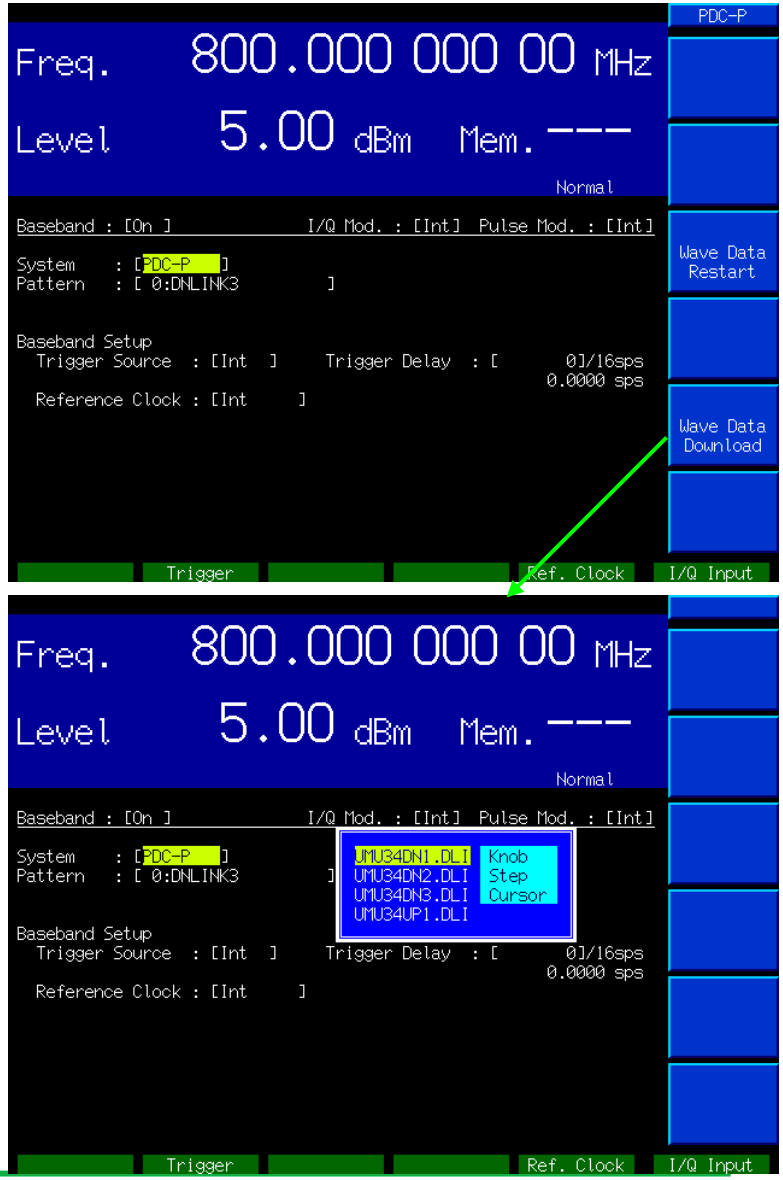






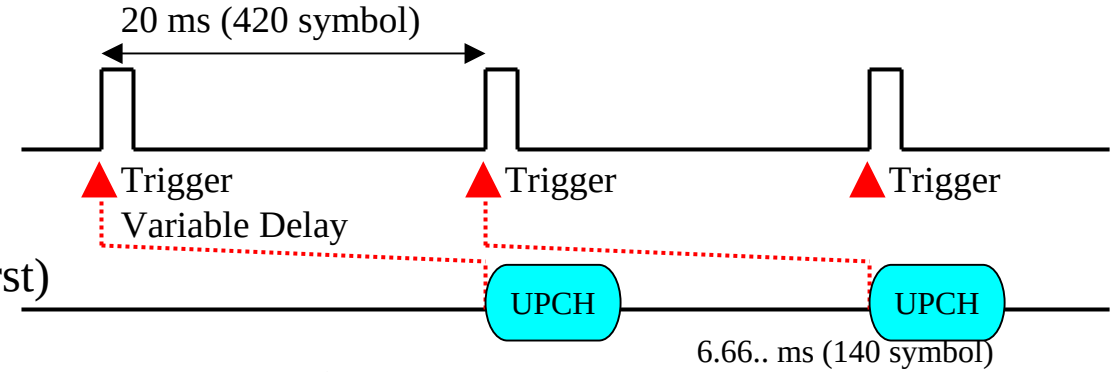
Packet communication Receiver test Setup example

- **Wanted signal generator**
  MG3681A
  + MU368030A + MX368034A
  - » BS test
    Uplink UPCH
    - – UP1
  - » MS test
    Downlink UPCH
    - – DN1
    - – DN2
    - – DN3



BS receiver Timing sync. Setup example

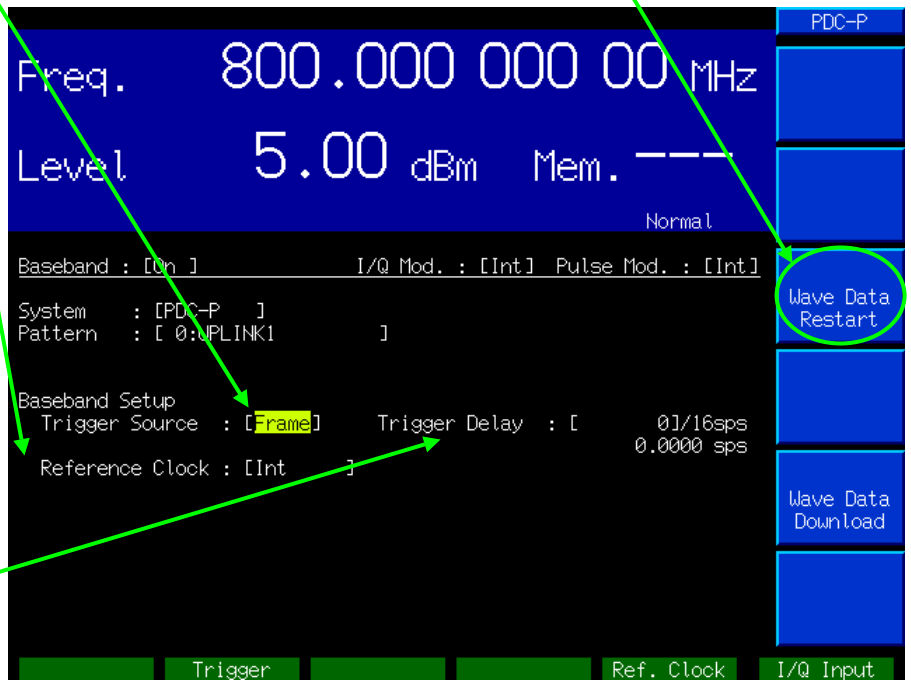
- **Frame trigger delay**
  - » Set the timing to which BS can receive Uplink UPCH
    - – Frame trigger Input
    - – Uplink UPCH (burst) Output
      - Outputting UPCH (burst) in 20 ms from trigger



BS receiver Timing sync. Setup example

- **Setting External Frame trigger**
  - » Captures/ Synchronizes the Trigger of 20 ms clock
- **Reference clock:**
  - Apply to cancel the jitter of within ±1/16 symbol of synchronous errors
  - » [Ref. Clock] Input applicable case
    - – Reference Clock : [Ext(TTL)]
      - 16× 21 kHz (336 kHz)
  - » [10MHz/13MHz Ref] Input applicable case
    - – Reference Clock : [Int]
- **Frame trigger delay**
  - » 0 ~ +16,777,215 /16 symbol
    1/16 symbol resolution
  - » Delay from trigger
    + 3.7 symbol
    - – 3.7 ~ 1,048,579.6 symbol

- **Trigger recapture/ synchronization**



e.g.

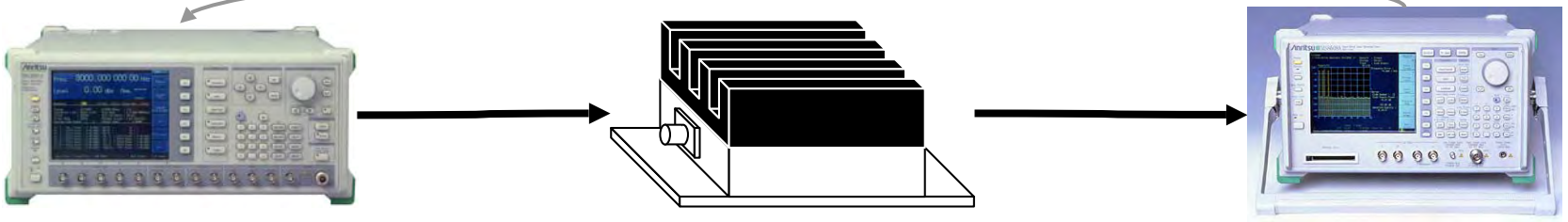
- » In case of outputting UPCH (burst) in 20 ms from trigger
  - 6,661 /16 symbol

RF/IF components test　Connection example

Signal source
MG3681A
+MU368010A+MX368011A
or
+MU368030A+MX368031A

Signal analyzer
(MS8600/MS2680)

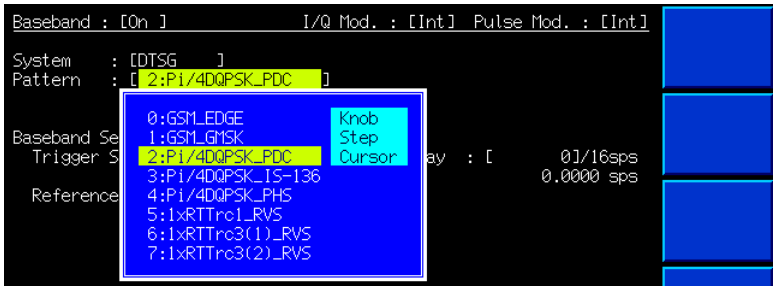
Reference clock

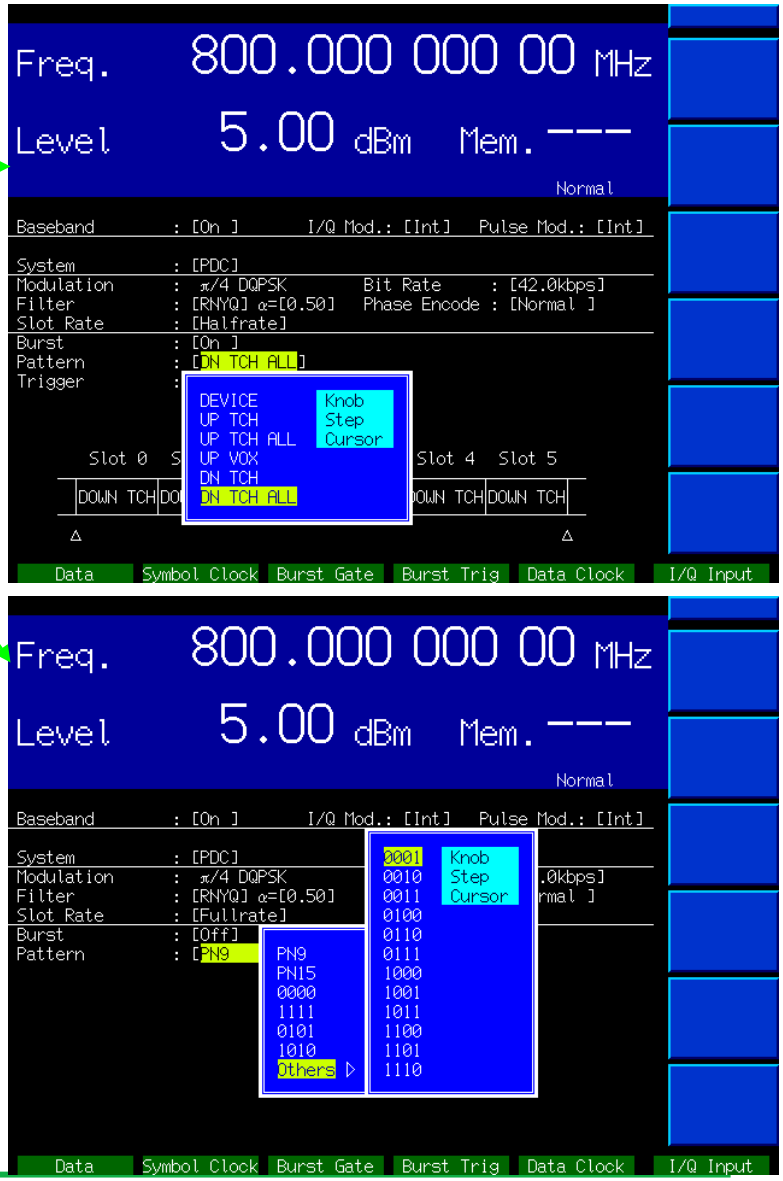


Signal Setup example

- **MX368011A**
  - » Burst format
  - » Continuous modulation format

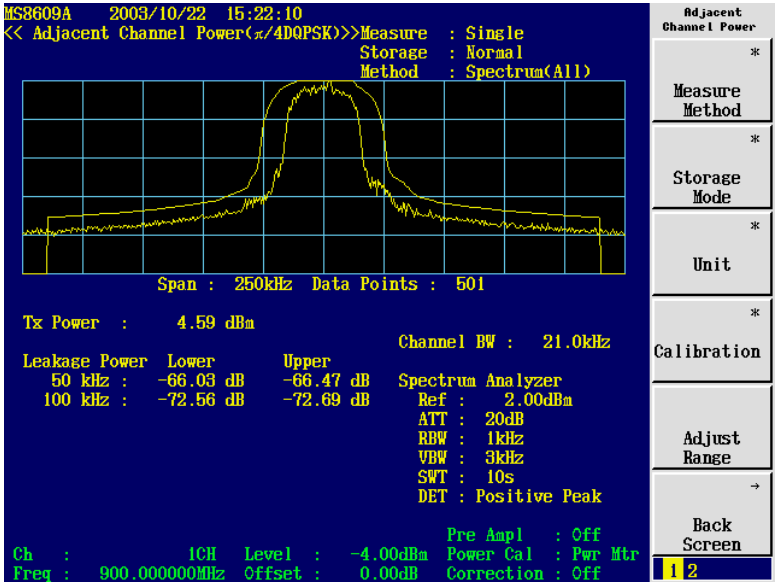
- **MX368031A**
  - » Continuous modulation format



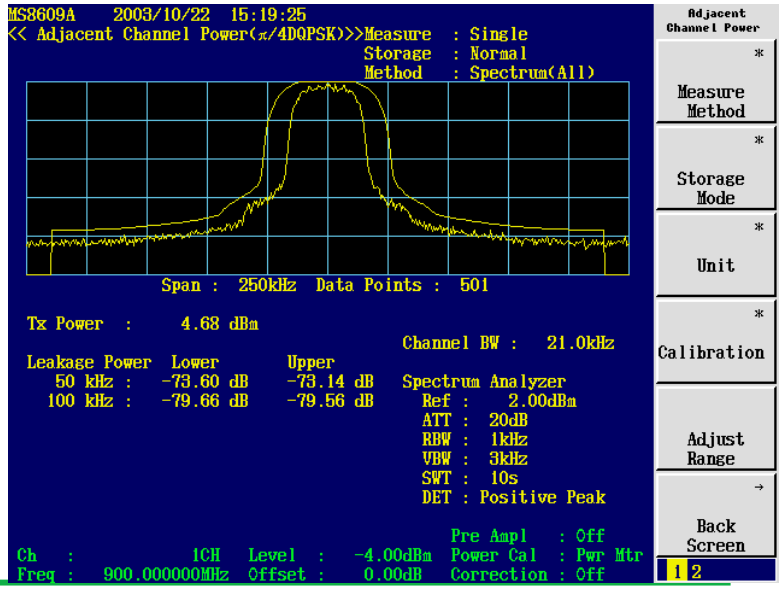


Contrast of typical ACLR

- **Burst (TCH) format**
  - » 50 kHz: +7 dB
  - » 100 kHz: +7 dB



- **Continuous modulation format**



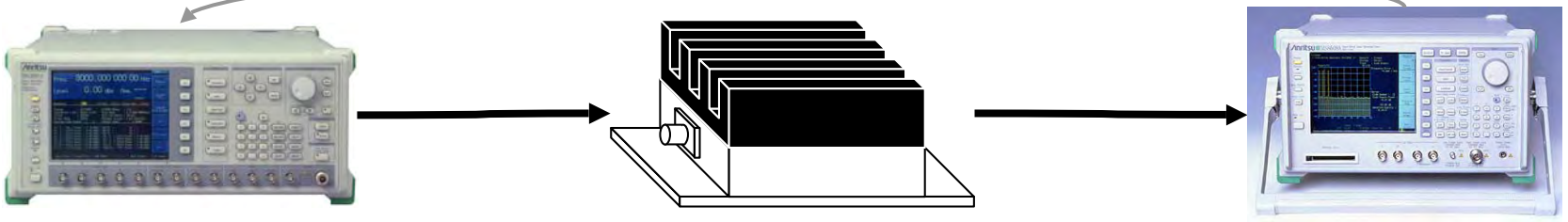
NADC IS-136

RF/IF components test Connection example

Signal source
MG3681A
+MU368030A+MX368031A

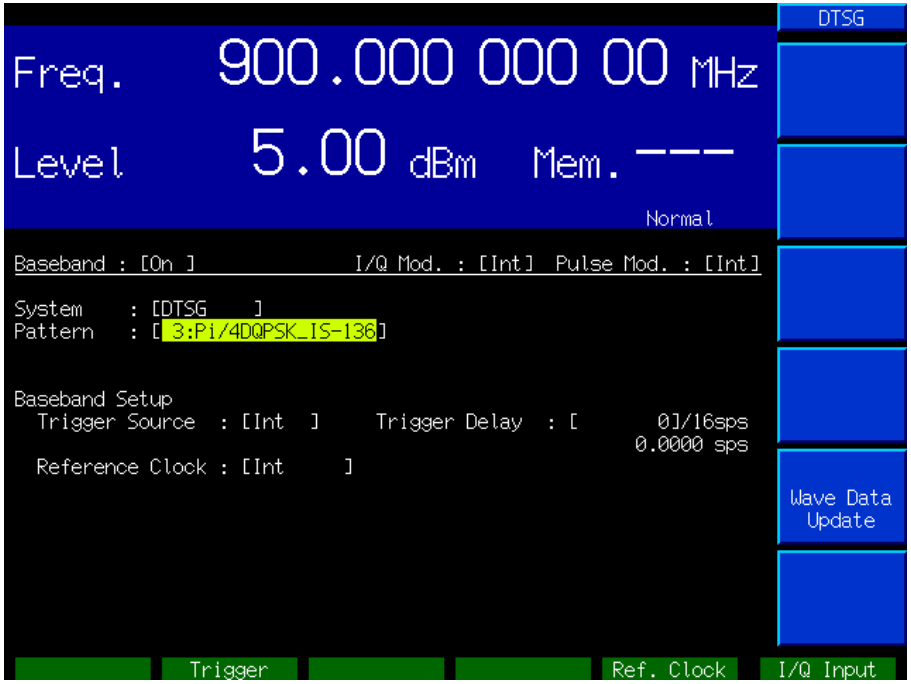
Signal analyzer
(MS8600/MS2680)

Reference clock



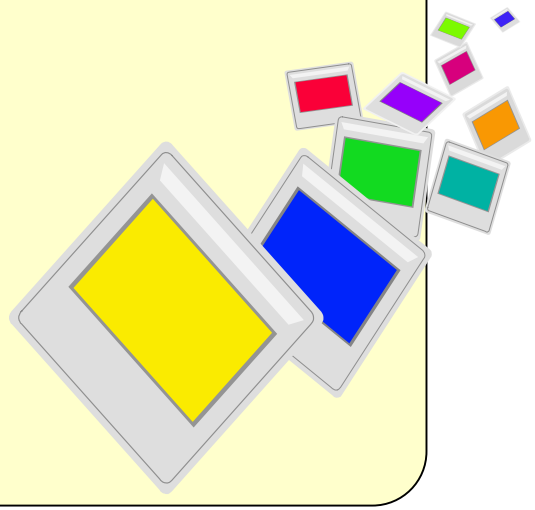
Signal Setup example

- **Continuous modulation format**



Option

- Product outline
- Feature
- Application
- Option



- **MG3681A-01, 02** 249
  - » Reference oscillator
- **MG3681A-11** 252
  - » Additional function of I/Q output
- **MG3681A-21** 256
  - » AF synthesizer
- **MG3681A-42** 259
  - » RF high level output

- **MA2512A** 264
  - » Band Pass Filter

MG3681A-01, 02 Reference oscillator

- **Exchangeable to long-term stable internal reference oscillator**

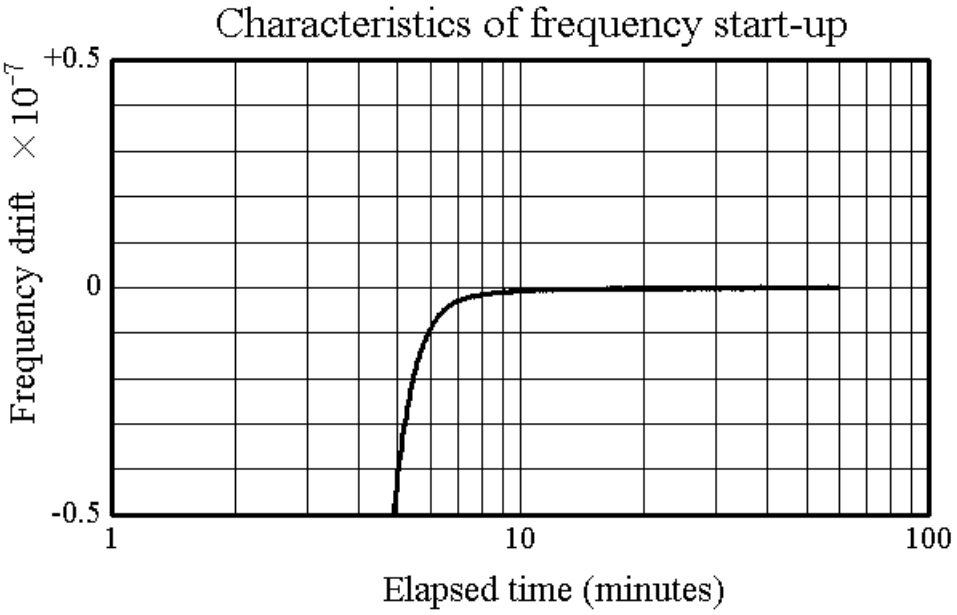
	Standard	MG3681A-01	MG3681A-02
Aging rate	$\pm 1 \times 10^{-6}$ /year	$\pm 5 \times 10^{-9}$ /day ($\pm 5 \times 10^{-8}$ /year)	$\pm 5 \times 10^{-10}$ /day ($\pm 2 \times 10^{-8}$ /year)
Warm-up stability		$\pm 1 \times 10^{-7}$	$\pm 1 \times 10^{-7}$
Temperature stability (0 ~ 50 °C)	$\pm 1 \times 10^{-6}$	$\pm 3 \times 10^{-8}$	$\pm 5 \times 10^{-9}$

* Warm-up stability: After 10 minute (compared to frequency after 24 hours)

- **Frequency accuracy is specified by the aging rate of reference oscillator.**
  - » Frequency accuracy
    = ± Output frequency × Aging rate × Time since last calibrated
    e.g. 2 GHz 1 year
    = ± 2 kHz * Standard
    = ± 40 Hz * MG3681A-02

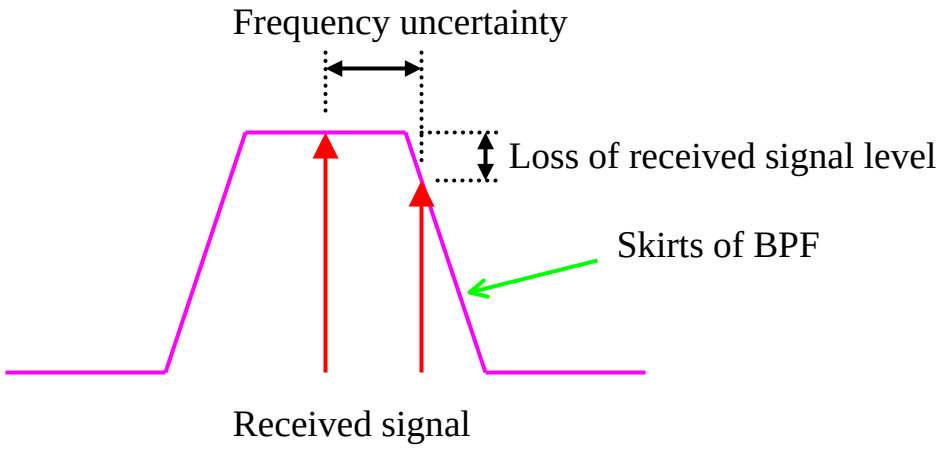
Warm-up stability

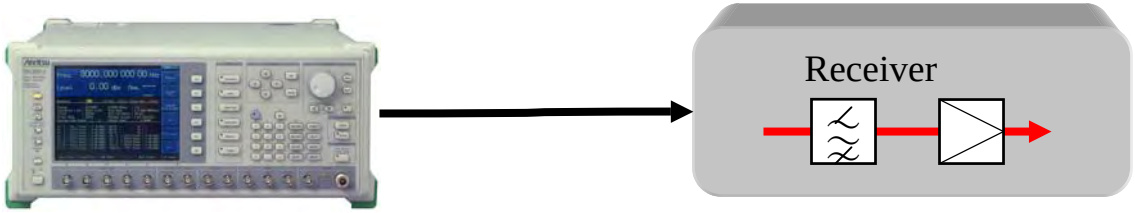
- **The long-term stable internal reference oscillator of MG3681A-01 and 02 uses OCXO of the oven system which stabilizes frequency only 10 minutes after the main power ON.**
  - » Since oven is preheated in power standby state, frequency is stabilized immediately after power ON from only 10 minutes standby state.
- **Standard internal reference oscillator uses TCXO with unnecessary preheating.**



Effect of frequency accuracy on receiver sensitivity test

- **In case of more frequency uncertainty (poor frequency accuracy), receiver is tested as deteriorated sensitivity than true value.**
  - » The level of the signal is lost when the received signal is located in the skirt of BPF in a receiver by frequency uncertainty.

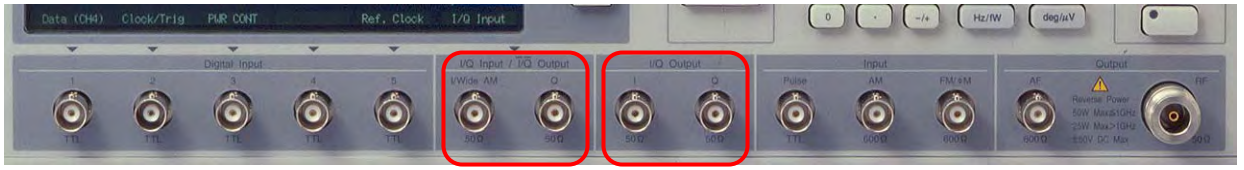




MG3681A-11 Additional function of I/Q output

- **Variable of voltage level of I/Q signals output, DC offset and quadrature degree**
  - » Voltage level: 80 ~ 120 % resolution 0.1 %
    - – RMS level ($\sqrt{I^2+Q^2}$) is specified in each system software.
  - » DC offset: -0.5 ~ +1.5 V resolution 0.5 mV
  - » Quadrature degree: -5 ~ +5 ° resolution 0.5 °

- **Differential I/Q signals can be outputted.**
  - » $\bar{I}/\bar{Q}$ signals which are reversal signals (amplitude is equal and polarity is reverse) of I/Q signals are outputted.



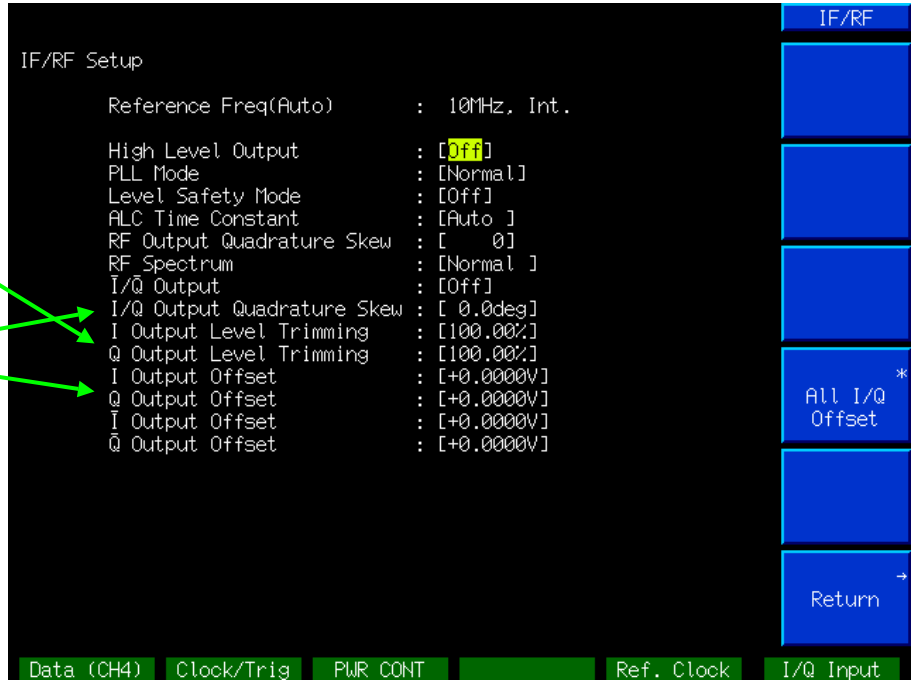
$\bar{I}/\bar{Q}$ signals output I/Q signals output

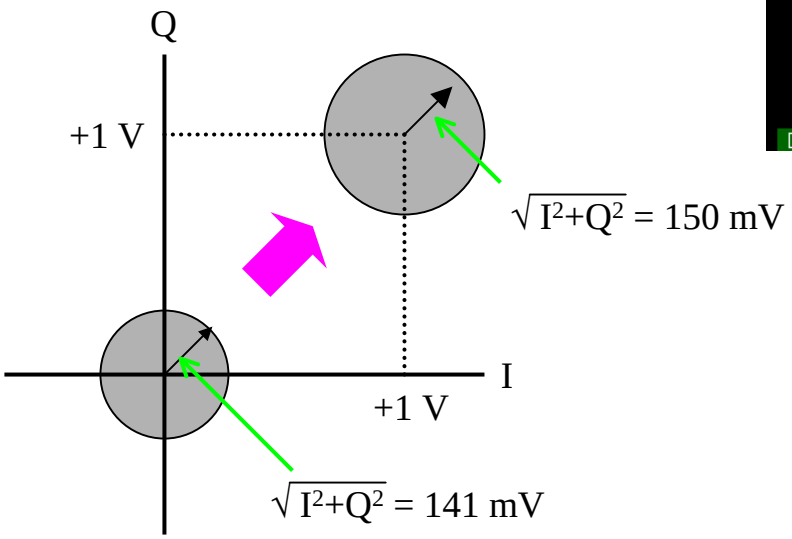
Variable application of voltage level of I/Q signals output, DC offset and quadrature degree

- **In order to test the vector modulator, the setup of vector magnitude, drive DC voltage and I/Q quadrature degree is required for the signal source.**
  - » Vector Magnitude
    - – Voltage level is set as RMS level of the vector modulator.
  - » Drive DC voltage
    - – In order to drive the vector modulator of the single power supply system, DC offset is set as drive voltage.
  - » Quadrature degree
    - – In order to cancel the error of I/Q quadrature degree (90 °) of the vector modulator, quadrature degree is set.

Variable of voltage level of I/Q signals output, DC offset and quadrature degree

- **Setup example**
  - » Voltage level
    - – Specified 141 mV(rms)
      → 150 mV(rms) ≈ 106 %
  - » DC offset
    - – +1 V
  - » Quadrature degree
    - – Fine tuning





Application of differential I/Q signals

- **In order to test the vector modulator and baseband LSI for balanced device, the output of I, I, Q and Q balance is required for the signal source.**

- **In I/Q input device, the balanced input has the advantage which can reduce the amplitude error and the noise compared with I and Q unbalanced input (single end).**
  - » Reduction of the amplitude error by the grand loop
    - – The cause is that the ground of the signal source and the ground of the input device are not equivalent potential.
  - » Reduction of a signal line noise
    - – The cause is that the environmental noise is picked up on the signal line.

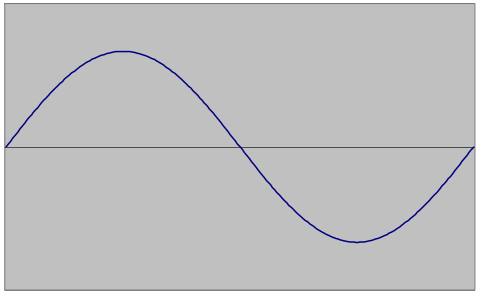
- **For outputting differential I/Q signals**
  - » I/Q Output: [On]

MG3681A-21 AF synthesizer

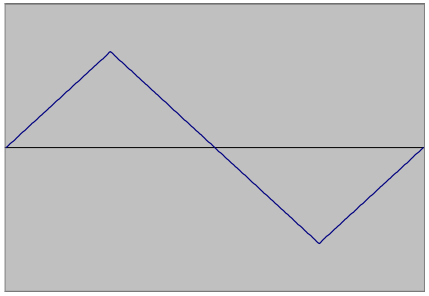
- **AF can be outputted.**

» 0.01 Hz ~ 400 kHz resolution 0.01 Hz

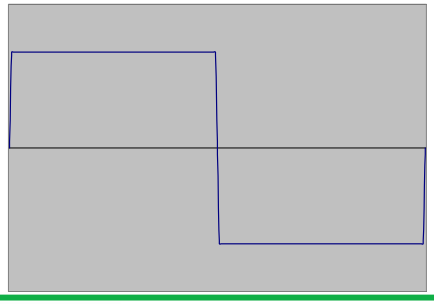
Sine wave



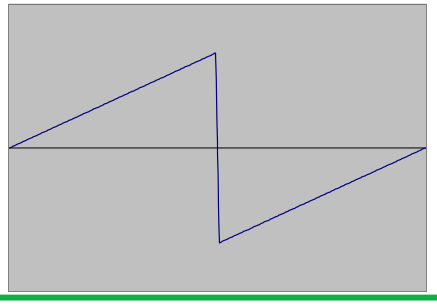
Triangle wave



Square wave

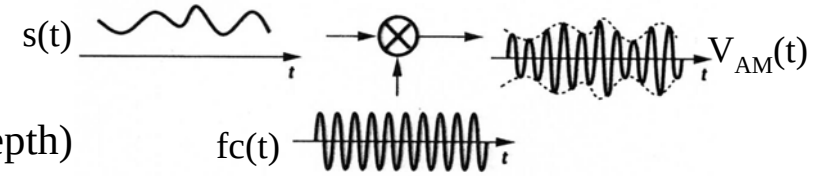


Sawtooth wave

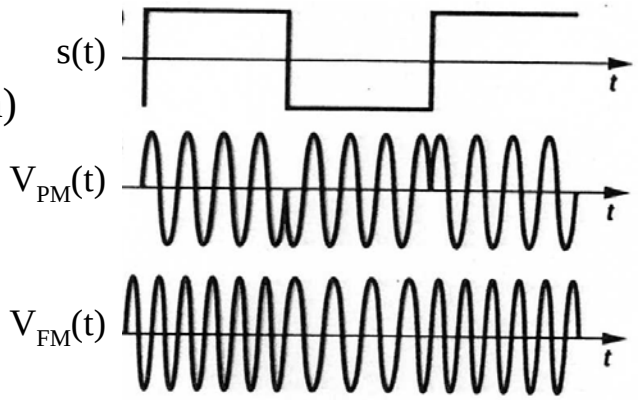


MG3681A-21 AF synthesizer

- **Internal analog modulation signal can be outputted.**
  - » AM
    - – $V_{AM}(t) = Ac\,[1 + m\,s(t)]\cos(2\pi fc\,t)$
      - m: Modulation index (Modulation depth)



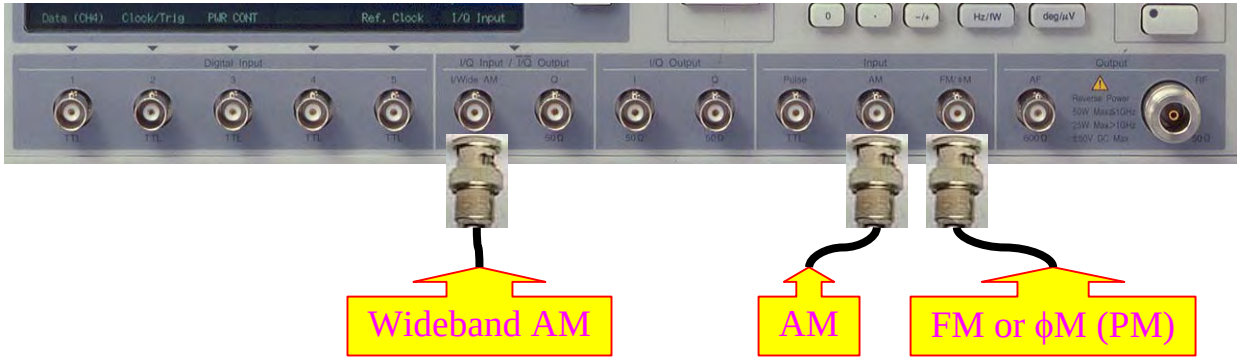
  - » FM
    - – $V_{FM}(t) = Ac\cos[2\pi fc\,t + m\int s(t)dt]$
      - m: Frequency modulation index (Frequency deviation)
  - » ϕM (PM)
    - – $V_{PM}(t) = Ac\cos[2\pi fc\,t + m\,s(t)]$
      - m: Phase modulation index (Phase deviation)



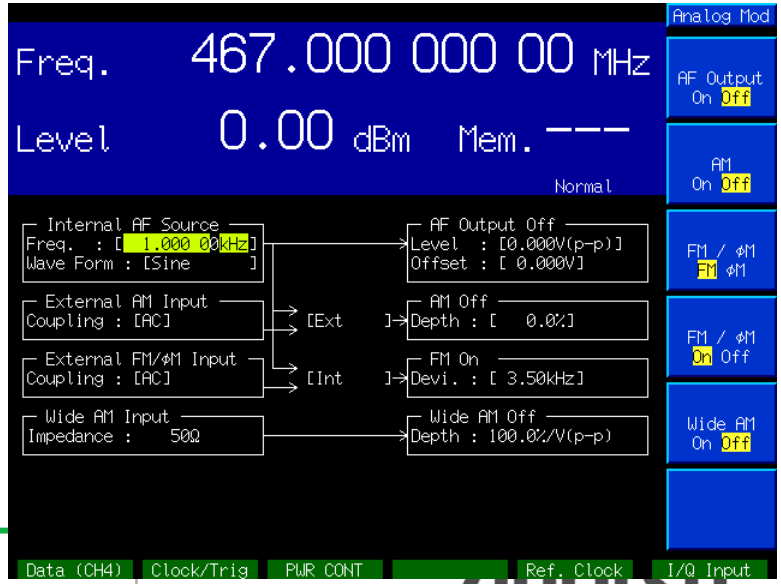
      - Ac: Carrier amplitude
      - s(t): Modulation signal (AF)
      - fc: Carrier frequency (RF)

External analog modulation

- **Input Modulation signal (AF).**

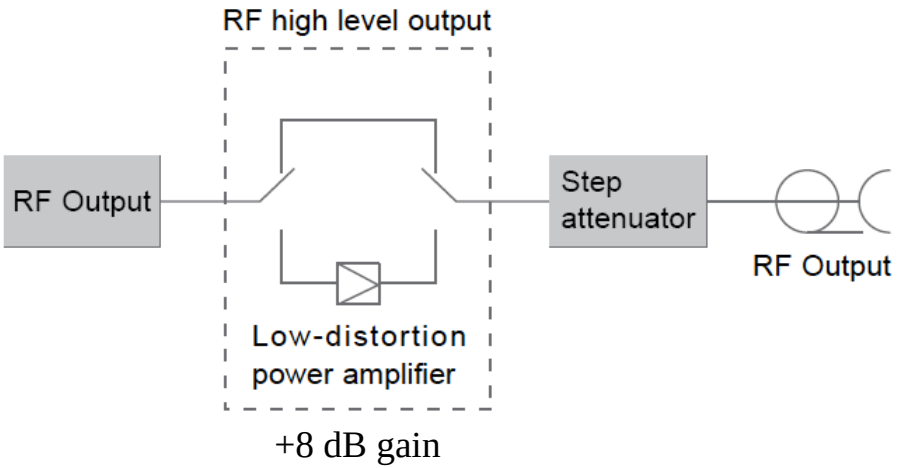


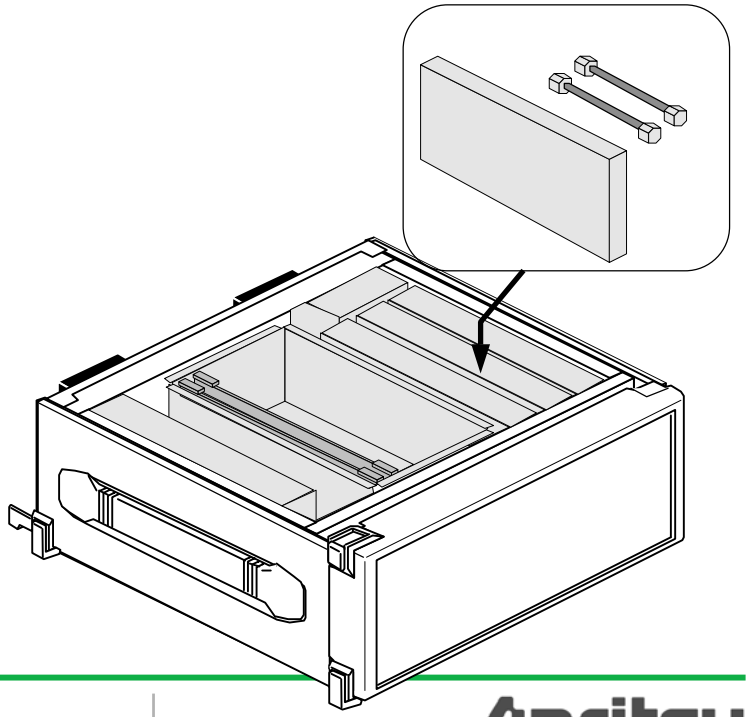
- **Wideband AM**
  - » Applicable to wideband (high-speed) video modulation
  - » ASK modulation is achieved by AM.
    - – Modulation signal
    - – ASK



MG3681A-42 RF high level output

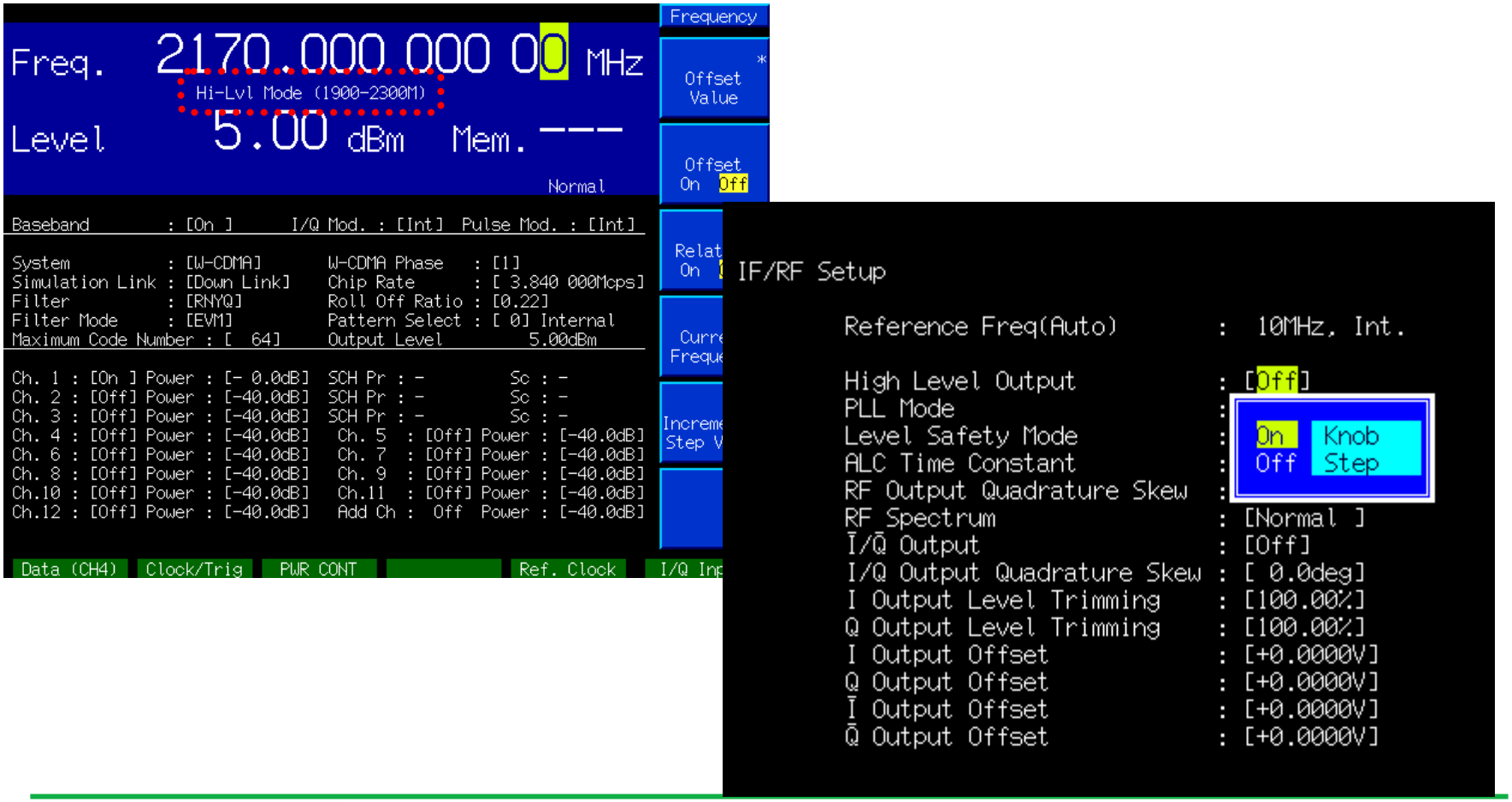
- **RF output level range in CDMA modulation signals can be gained 8 dB without degrading the adjacent channel leakage power ratio.**
  - » at outputting 1.9 to 2.3 GHz used as the frequency band for IMT-2000 systems
  - » ACLR does not degrade up to +5 dBm in W-CDMA/CDMA2000 modulation.





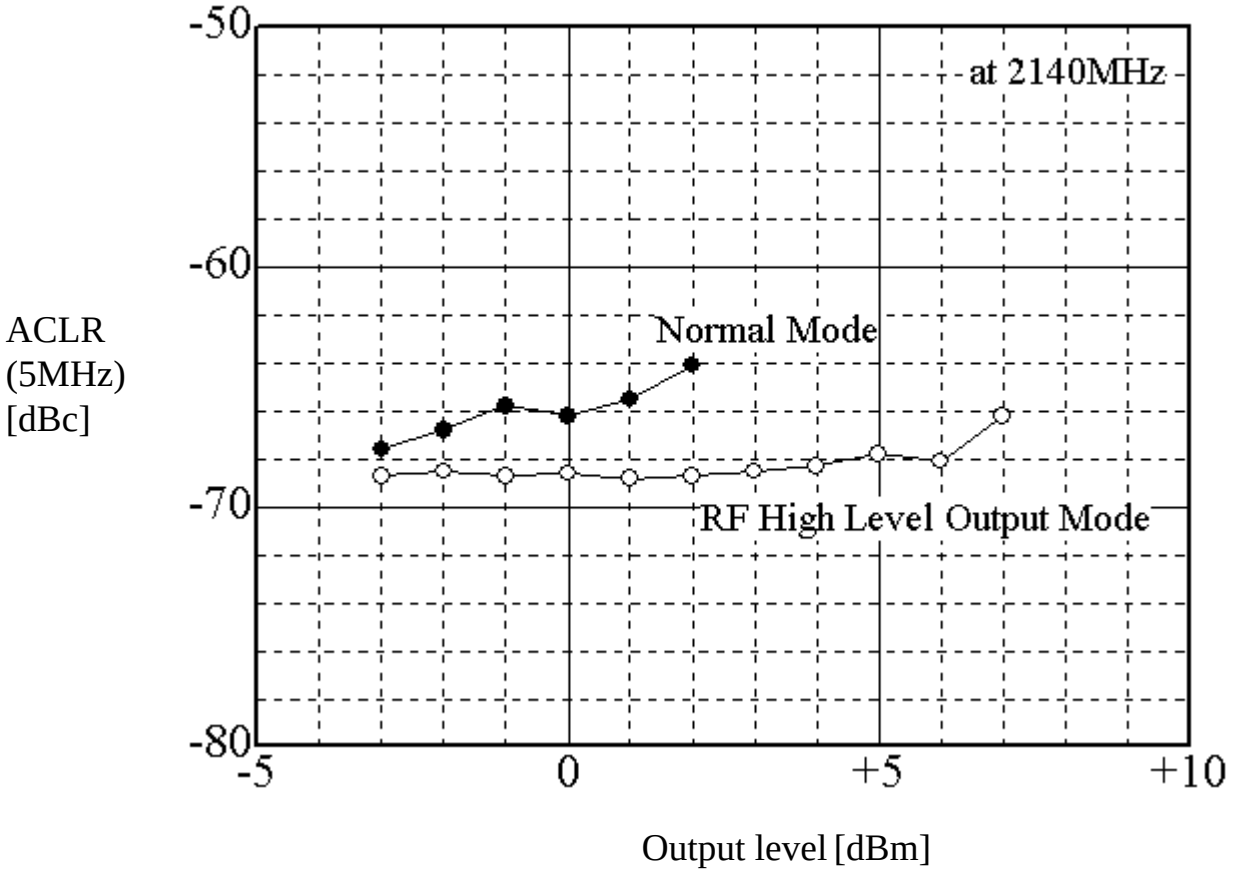
Application

- **Useful for signal source of power amplifier requiring a high input level**



Typ. ACLR

- **W-CDMA**
  - » Test Model 1: 16 DPCH

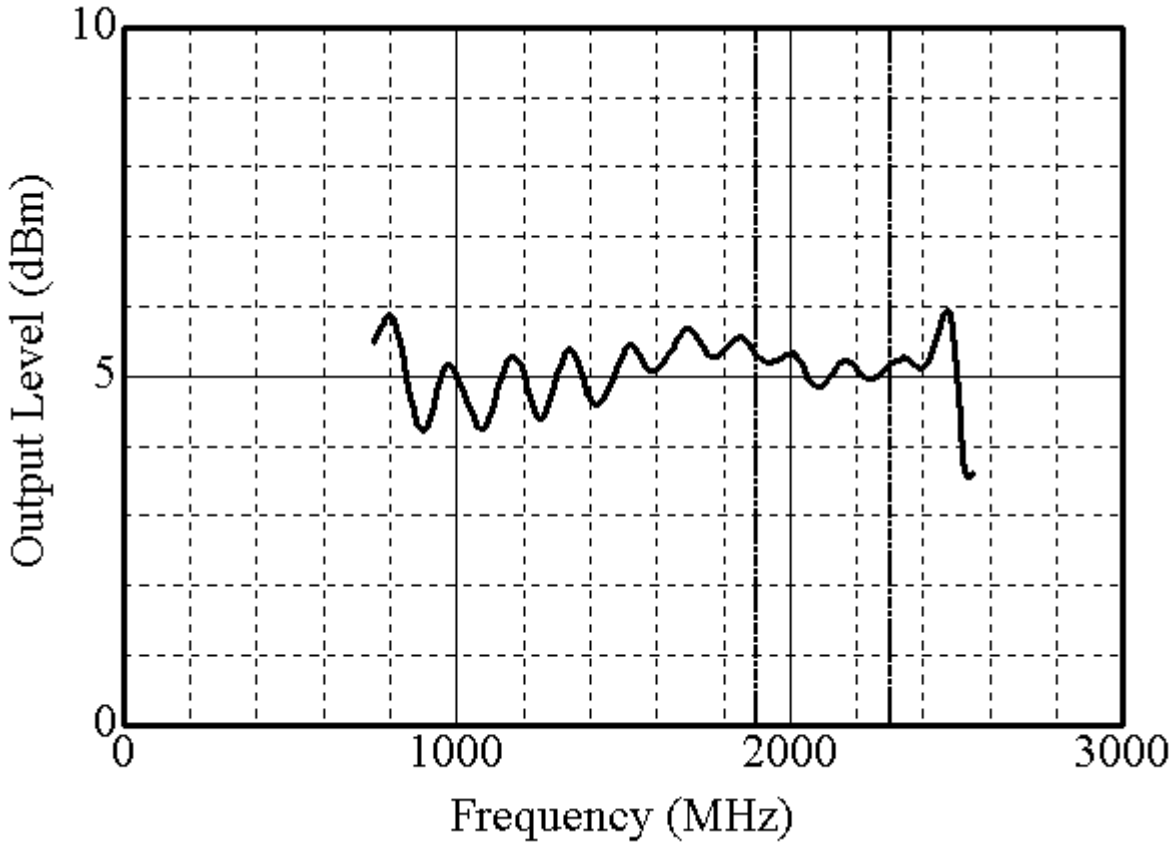


Maximum output level (1.9~2.3 GHz)

		Standard		MG3681A-42
• **W-CDMA modulation**			+8 dB gain	
Number of multiplex channel:		dBm		dBm
» 1~7	:	+5		+13
» 8~12	:	+4		+12
» 13~15	:	+3		+11
» 16~19	:	+2.14		+10.14
» 20~31	:	+2		+10
» 32~50	:	+1		+9
» 51~	:	0		+8
• **CDMA2000 modulation**				
»		+5		+13
• **CW**			without gain	
»		+17		Typ.+19 (Setting: +25)

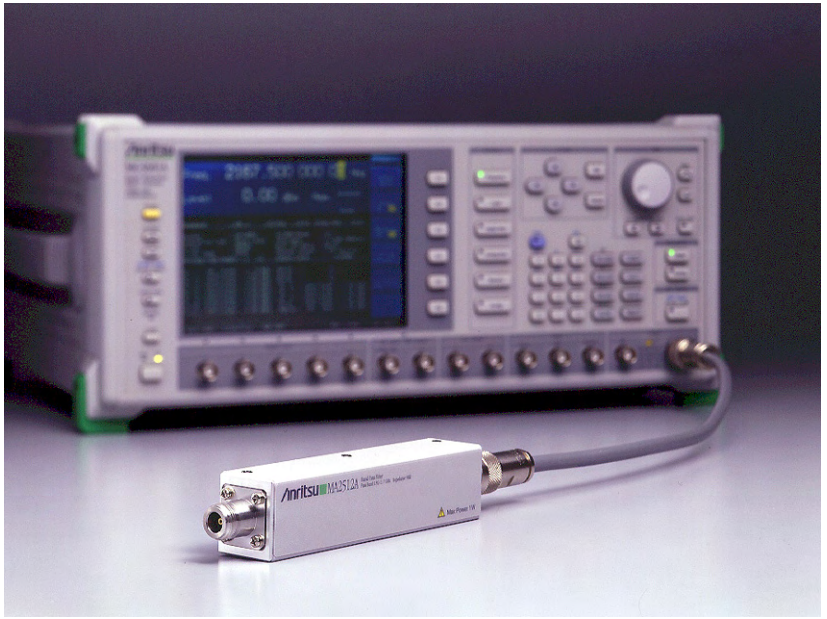
Typ. output level frequency response

- **Level +5 dBm setting (CW)**



MA2512A Band Pass Filter

- **The unnecessary spurious signal of a signal generator can be attenuated.**
  - » at outputting 1.92 to 2.17 GHz used as the frequency band for IMT-2000 systems
  - » Excellent amplitude ripple and group delay characteristics don't degrade modulation accuracy of the signal.



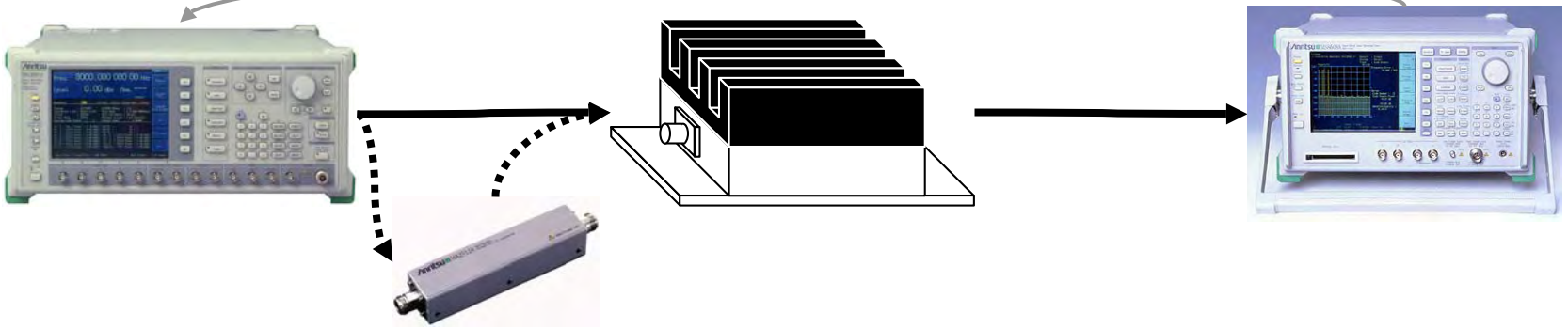
Application

- **When spurious signals hinder components evaluation**
  - » Spurious signals of MG3681A
    - – 660 MHz (IF leakage)
    - – +660 MHz offset (Local leakage)
    - – 2×frequency/3×frequency (2nd/3rd harmonics)

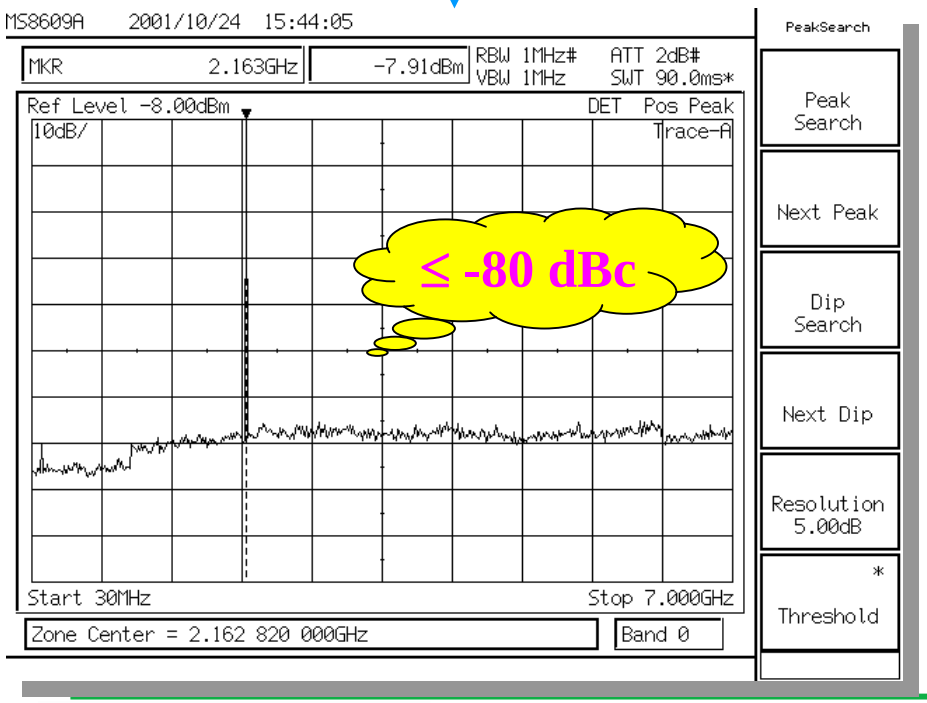
Signal source
MG3681A
+MU368040A+MX368041B

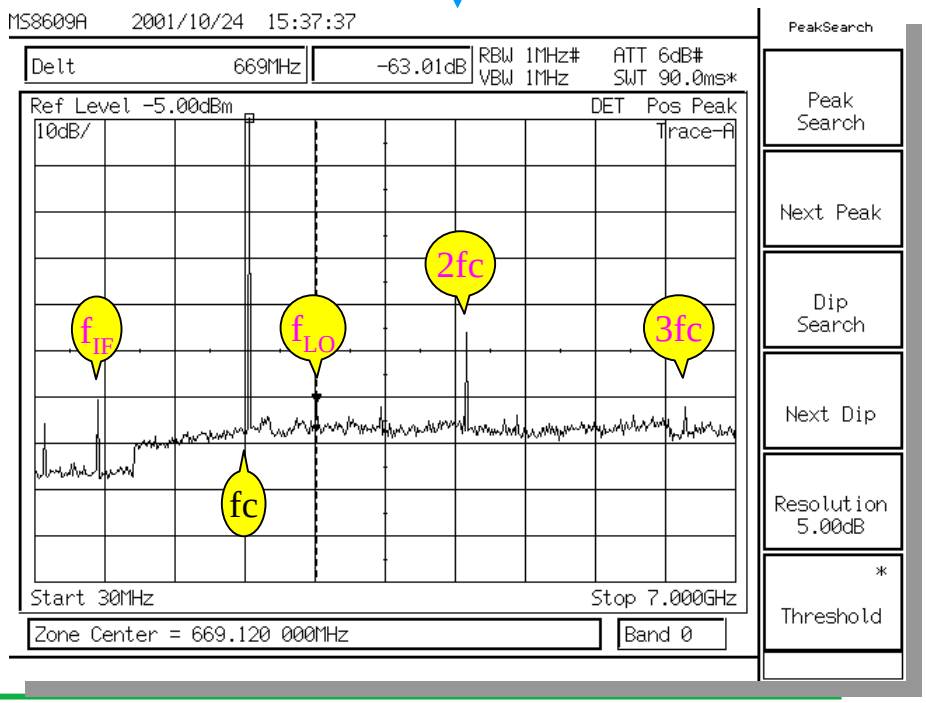
Reference clock

Signal analyzer
(MS8600/MS2680)



Improvement of spurious





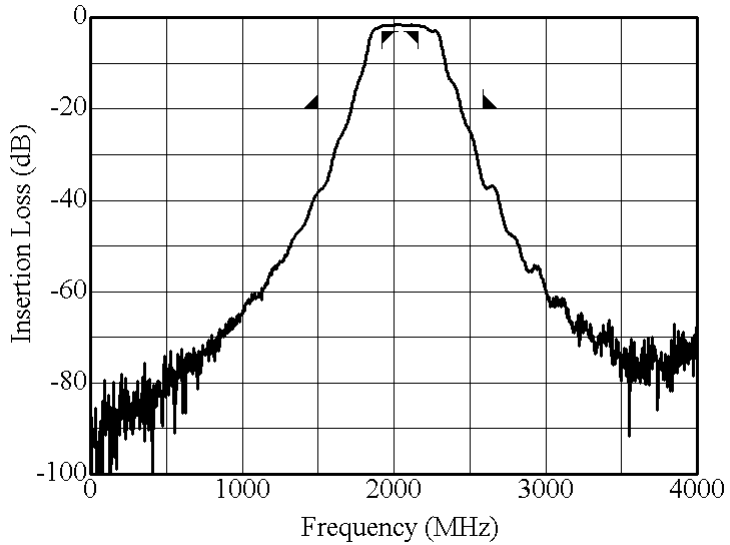
Loss frequency response

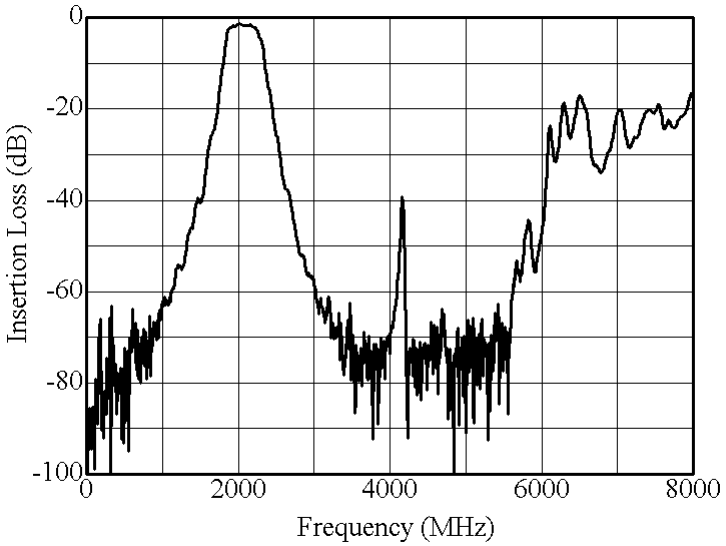
Pass band

- **1.92~2.17 GHz**
  (IMT-2000 system band)
- **Insertion loss ≤ 3.5 dB**
- **Return loss ≥ 15 dB**

Filter band

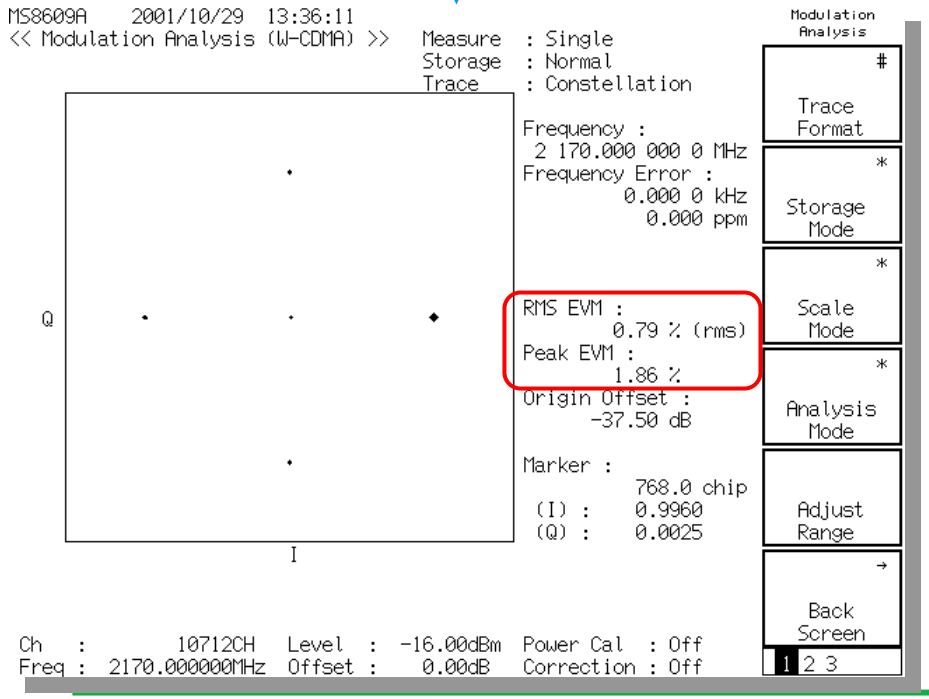
- **DC ~ 1.5 G, 2.58 ~ 7 GHz**
- **Attenuation ≥ 20 dB (< 5 GHz)**
  ≥ 10 dB (≥ 5 GHz)

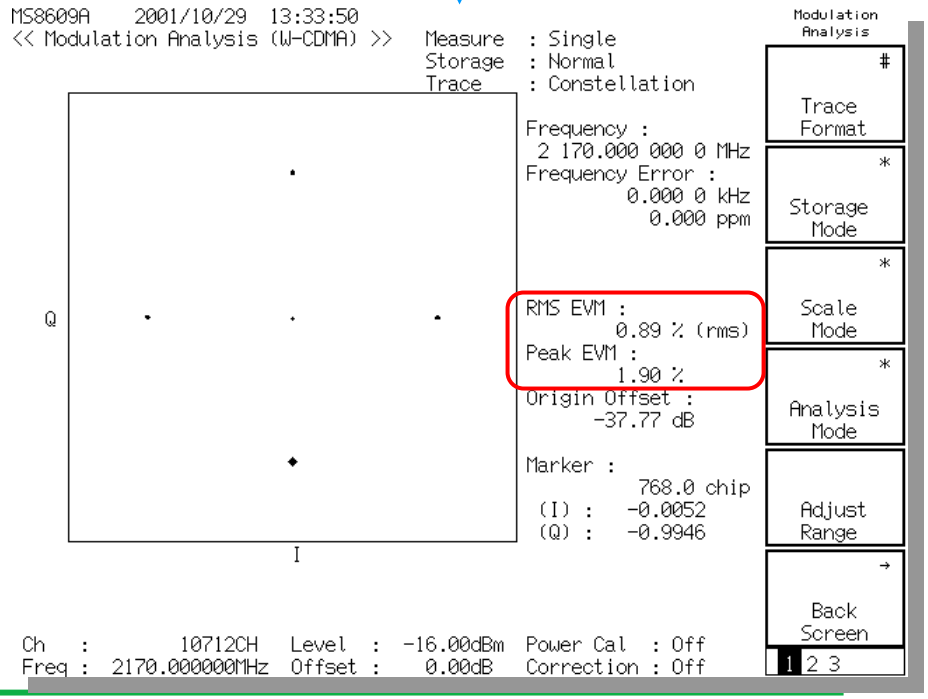




Modulation accuracy not degrading

- **Amplitude ripple**
  - » ≤ 0.2 dB (5 MHzBW)
- **Group delay**
  - » ≤ 1 ns (5 MHzBW)





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