32-bit Cortex-M0+ based General Purpose Microcontroller

FlashROM 64·128·256 KB / SRAM 16KB

A31G31x

USER MANUAL

Version 1.0.10

2022.01.14.

Revision History:

Date	By	Version	Description
2018/5/3	Donghyo Shin	1.0.0	Published the standard version of this document
2018/5/29	Donghyo Shin	1.0.1	- A31G314 → A31G31x - Added description for each flash memory options. - Update user manual format - Typo about number of ADC channel In ADC block is modified.
2018/7/19	Donghyo Shin	1.0.2	-DAC synchronization with TIMER10/11 match signal -> DAC synchro-nization withTIMER10/11 rising edge of Timer out signal - FMC Self PGM description is modified -Nomenclature is modified
2019/9/24	Hyogeun Song	1.0.3	- Delete USB, ADPCM Function
2019/9/24	Yuncheol Choi	1.0.4	- Minor bug fixes.
2020/2/4	Hyogeun Song	1.0.5	- To change VDD33 pin to VDD pin. - Added description for PORT n Debounce Control Register. - To change document disclaimer and distributor.
2020/8/5	Hyogeun Song	1.0.6	- Added description for external oscillator load capacitor value. - Correction of typos in relation to LSI characteristics.
2021/8/11	ABOV	1.0.7	- TS_TRIM_OSC, TS_TRIM_A_OSC modified
2021/11/17	ABOV	1.0.8	- 1.3 Main Features Endurance modified - Table 25.13 Supply Current Characteristics modified
2021/12/22	ABOV	1.0.9	18.4.1 Conversion timing modified
2022/01/14	ABOV	1.0.10	Added 22.3.3 LCD_BSSR VLE_EN[11]

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CHAPTER 1. OVERVIEW

1.1 Overview

A31G31x is designed for the main controller of various appliances.

In particular, accordance with the tendency that the microcontroller is becoming more complicated and high performance in consumer electronics, ARM's high-speed 32-bit Cortex-M0+ Core is used. And for handling more features, this microcontroller has a variety of peripheral devices and large amounts of flash memory. Powerful and various external serial interfaces help to communicate with on-board sensors and devices.

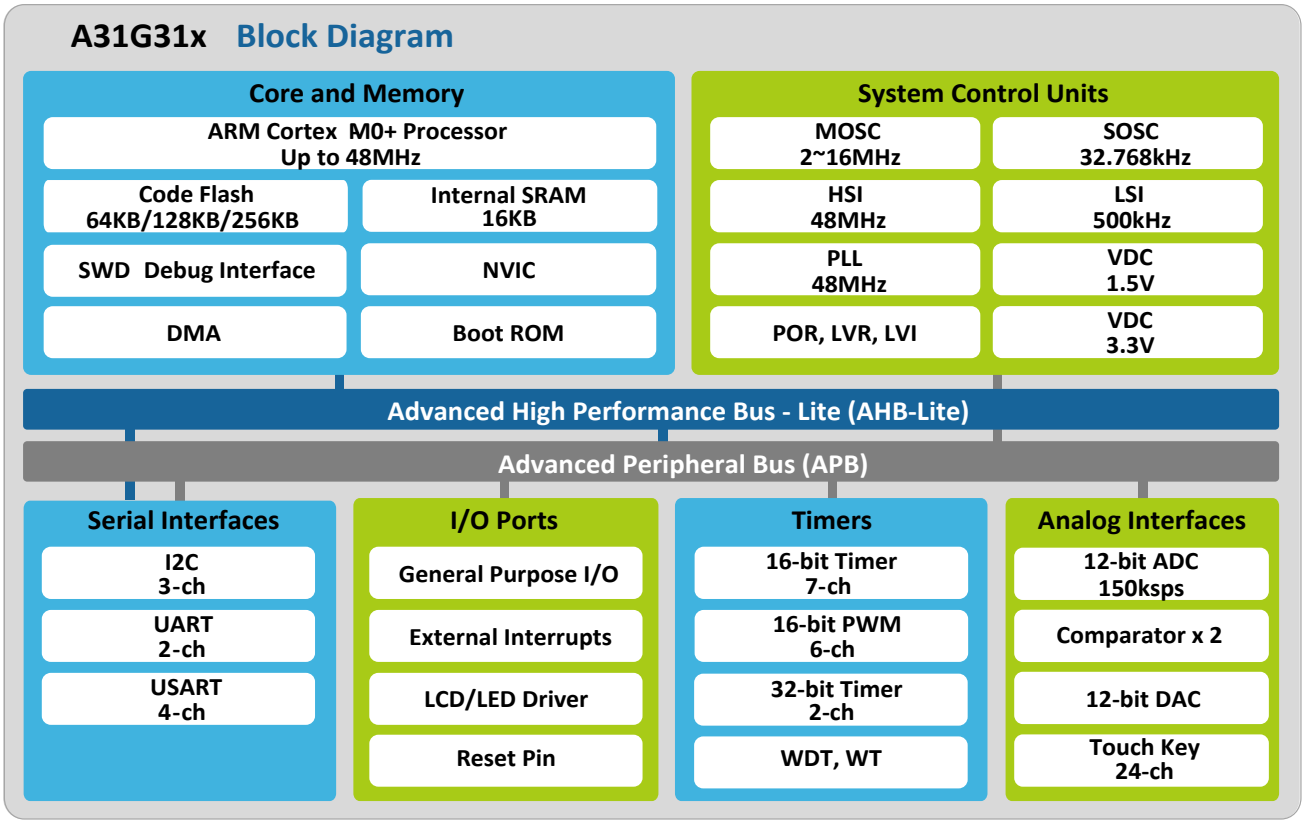


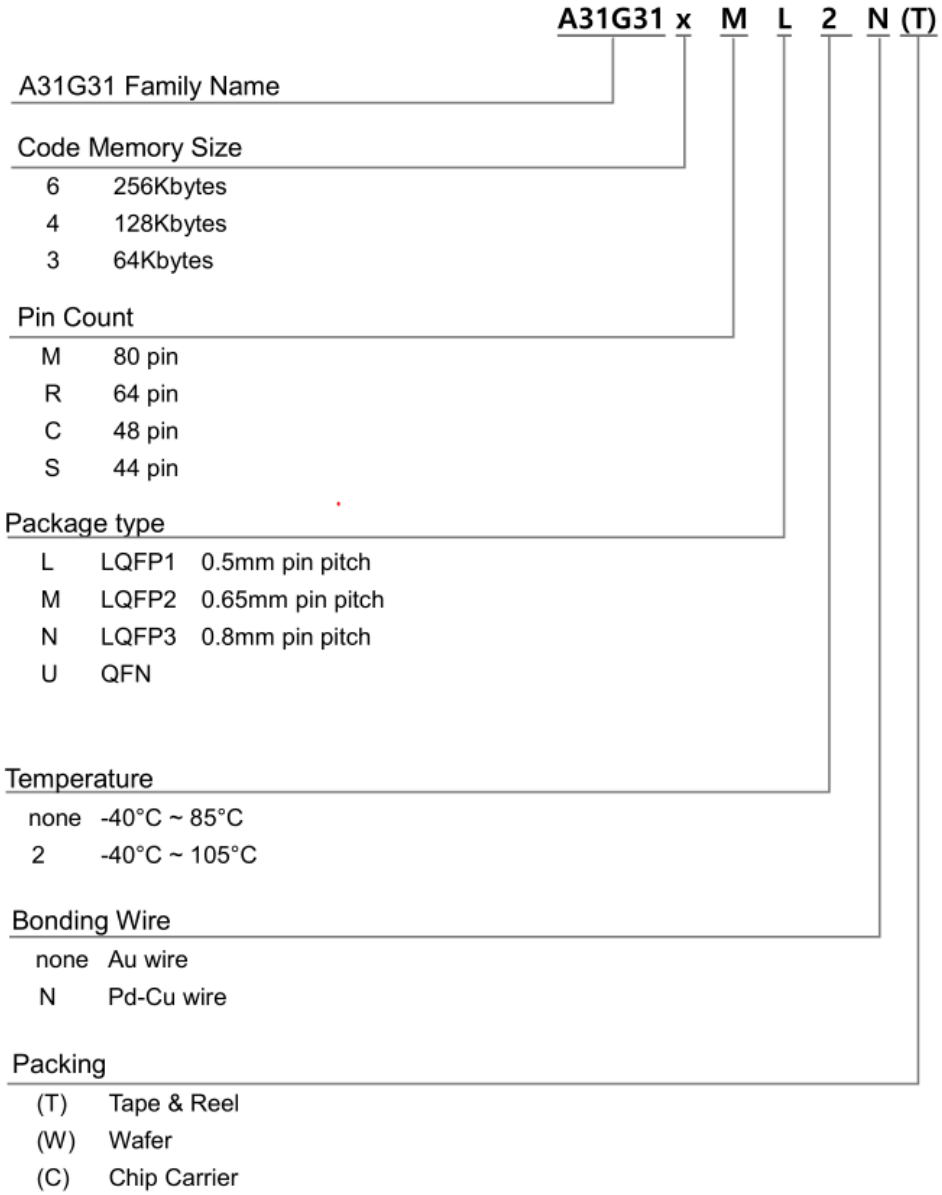
Figure 1.1 Block diagram

1.2 Ordering Information

Table 1.1. Ordering Information

Product Name	CODE Flash [KB]	SRAM [KB]	UART [ch]	USART [ch]	I2C [ch]	TIMER [ch]	PWM [ch]	12-bit ADC [ch]	I/O Ports [ch]	Package
A31G316MMN	256KB	16KB	2	4	3	7(16bit)/ 2(32bit)	6	14	74	80LQFP14
A31G316MLN	256KB	16KB	2	4	3	7(16bit)/ 2(32bit)	6	14	74	80LQFP12
A31G316RMN	256KB	16KB	2	3	3	7(16bit)/ 2(32bit)	6	14	58	64LQFP12
A31G316RLN	256KB	16KB	2	3	3	7(16bit)/ 2(32bit)	6	14	58	64LQFP10
A31G314MMN	128KB	16KB	2	4	3	7(16bit)/ 2(32bit)	6	14	74	80LQFP14
A31G314MLN	128KB	16KB	2	4	3	7(16bit)/ 2(32bit)	6	14	74	80LQFP12
A31G314RMN	128KB	16KB	2	3	3	7(16bit)/ 2(32bit)	6	14	58	64LQFP12
A31G314RLN	128KB	16KB	2	3	3	7(16bit)/ 2(32bit)	6	14	58	64LQFP10
A31G314CLN	128KB	16KB	2	2	2	7(16bit)/ 2(32bit)	6	11	43	48LQFP
A31G314CUN	128KB	16KB	2	2	2	7(16bit)/ 2(32bit)	6	11	43	48QFN
A31G314SNN	128KB	16KB	2	2	2	7(16bit)/ 2(32bit)	6	9	39	44LQFP
A31G313RMN	64KB	16KB	2	3	3	7(16bit)/ 2(32bit)	6	14	58	64LQFP12
A31G313RLN	64KB	16KB	2	3	3	7(16bit)/ 2(32bit)	6	14	58	64LQFP10
A31G313CLN	64KB	16KB	2	2	2	7(16bit)/ 2(32bit)	6	11	43	48LQFP
A31G313CUN	64KB	16KB	2	2	2	7(16bit)/ 2(32bit)	6	11	43	48QFN
A31G313SNN	64KB	16KB	2	2	2	7(16bit)/ 2(32bit)	6	9	39	44LQFP

Device Nomenclature



1.3 Main Features

Product features of A31G31x is below

- High Performance Low-power Cortex-M0+ Core
- 64KB/128KB/256KB Code Flash Memory
  - Endurance : 10,000 times
  - Retention : 10 years
- 16KB SRAM
- General Purpose I/O (GPIO)
  - 74 Ports (PA[11:9,7:0], PB[15:0], PC[12:0], PD[5:0], PE[15:0], PF[11:0]) : 80-Pin
  - 58 Ports (PA[11:9,7:0], PB[11:0], PC[12:11,6:0], PD[5:0], PE[11:0], PF[7:0]) : 64-Pin
  - 43 Ports (PA[7:0], PB[7:0], PC[4:0], PD[5:0], PE[11:0], PF[7:0]) : 48-Pin
  - 39 Ports (PA[7:5,2:0], PB[7:0], PC[4:0], PD[4:0], PE[6:0], PF[7:0]) : 44-Pin
- LCD Driver
  - 42 SEG x 8 COM LCD Driver
  - "1/3, 1/4, 1/5, 1/6, 1/8" duty selectable, "1/2, 1/3, 1/4" resistor bias, 16-step contrast control, and automatic bias control
- LED Driver
  - 11 ISEG x 27 ICOM LED Driver
  - ICOM 26.4mA, ISEG 2.4mA @3.3V
- Timer
  - 16 Bit 7-ch, Periodic timer mode, One-shot timer mode, PWM pulse mode, Capture mode
  - 32 Bit 2-ch, Periodic timer mode, One-shot timer mode, PWM pulse mode, Capture mode
- PWM
  - 16 Bit 6-ch, Periodic timer mode, Back-to-Back mode, Capture mode
- Watchdog Timer
  - 24 Bit 1-ch, WDTRC 31.250kHz
- Watch Timer
  - 14 Bit divider with extended 12 Bit counter 1-ch
- External communication ports:
  - 2-ch UART, 4-ch USART, 3-ch I^2C : 80-Pin
  - 2-ch UART, 3-ch USART, 3-ch I^2C : 64-Pin
  - 2-ch UART, 2-ch USART, 2-ch I^2C : 48-Pin, 44-Pin
- Direct Memory Access Controller
  - 4-ch
- 150kSPS 12-bit ADC
  - 14-ch : 80-Pin, 64-Pin
  - 11-ch : 48-Pin
  - 9-ch : 44-Pin
- Comparator
  - 1 reference 1 input comparator 1-ch
  - 1 reference 3 input comparator 1-ch
- 12-bit DAC
- Capactive Touch Switch
  - 24-ch : 80-Pin
  - 20-ch : 64-Pin
  - 13-ch : 48-Pin
  - 11-ch : 44-Pin
- On-Chip RC-Oscillator

- HSI : 48MHz(±3.5% @-40 ~ +85℃)
- LSI : 500kHz(±20% @-40 ~ +85℃)

- External main crystal oscillator
  - 2MHz ~16MHz
- System Fail-Safe function by Clock Monitoring
- XTAL OSC Fail monitoring
- CRC
  - CRC-CCITT, CRC-16
- Power On Reset
- Programmable Low Voltage Reset, Low Voltage Indicator
- Debug and Emergency stop function
- SWD Debugger
- Power Down Mode
  - IDLE, STOP Mode
- Sub-Active mode
  - System used external 32.768kHz crystal or system used internal 500kHz LSI
- Operating Frequency
  - 500kHz ~ 48MHz
  - External 32.768kHz crystal
  - PLL 48MHz
- Operating Voltage
  - 1.8V ~ 5.5V
- Operating Temperature
  - -40 ~ +85℃
- package options
  - A31G316(FLASH 256KB) : 80LQFP14/80LQFP12/64LQFP12/64LQFP10
  - A31G314(FLASH 128KB) : 80LQFP14/80LQFP12/64LQFP12/64LQFP10/ 48LQFP / 48QNF / 44LQFP
  - A31G313(FLASH 64KB) : 64LQFP12/64LQFP10/48LQFP/48QFN/44LQFP

1.3.1 Functional Description

The following section provides an overview of the features of A31G31x microcontroller.

ARM Cortex-M0+

ARM powered Cortex-M0+ Core based on ARMv6M architecture which is optimized for small size and low power system.
On core system timer (SYSTICK) provides a simple 24-bit timer easy to manage the system operation
Thumb-compatible Thumb-2 only instruction set processor core makes code high-density.
Hardware division and single-cycle multiplication is present
Integrated Nested Vectored Interrupt Controller (NVIC) provides deterministic interrupt handling.
SWD debugging features are provided.
Max 48MHz operating frequency with one wait execution

Nested Vector-Interrupt Controller (NVIC)

The ARM Nested Vectored Interrupt Controller (NVIC) on the ARM Cortex-M0+ core is included which handles all the internal and external exceptions. When interrupt condition is detected, the processor state is automatically stored to the stack and automatically restored from the stack at the end of interrupt service routine.

The vector is fetched in parallel to the state saving, which enables efficient interrupt entry.

The processor supports tail-chaining, which enables back-to-back interrupts to be performed without the overhead of state saving and restoring.

128KB Internal Code Flash Memory

The A31G31x provides internal 128KB code flash memory and its controller. This is enough to control the general system. Self-programming is available and ISP and SWD programming is also supported in boot or debugging mode.

Instruction and data cache buffer are present and overcome the low bandwidth flash memory. The CPU can access flash memory with one wait state up to 48 MHz bus frequency.

16KB 0-wait Internal SRAM

On chip 16KB 0-wait SRAM can be used for working memory space and program code can be loaded on this SRAM.

DMA Controller

The DMA controller performs direct memory transfer by sharing the system bus with CPU core.

Boot Logic

The smart boot logic supports the flash programming. The A31G31x can be entered by external boot pin and UART and SPI programming are available in boot mode. USART10 is used in boot mode communication.

System Control Unit (SCU)

The SCU block manages internal power, clock, reset and operation mode. It also controls analog blocks (Oscillator Block, VDC, LVR and LVI)

32-bit Watchdog Timer (WDT)

The watchdog timer performs system monitoring function. It will generate internal reset or interrupt to notice abnormal status of the system.

Multi-purpose 16/32-bit Timer

Seven-channel 16-bit and Two-channel 32-bit general purpose timers supports below functions.

- Periodic timer mode
- Counter mode
- PWM mode
- Capture mode

16-bit Timer with 6 Channel PWMs

The 16-bit timer has 6 channel PWMs for 3-phase motor application. 16-bit up/down counter with prescaler supports both of triangular and saw tooth waveform.

The PWM has ability to generate internal ADC trigger signal to measure the signal on time.

Dead time insertion and emergency stop functionality help that the chip and system are under safety conditions.

Universal Asynchronous Receiver/Transmitter (UART)

The A31G31x has 2 channels UART block. For accurate baud rate control, the fractional baud rate generator is provided.

Universal Asynchronous Receiver/Transmitter and Serial Peripheral Interface (USART: UART and SPI)

The USART supports UART and SPI mode. The A31G31x series has 4 channel USART modules.

Boot mode will use this USART block to download flash program.

Inter-Integrated Circuit Interface (I^2C)

The A31G31x has 3 channel I^2C block and it supports up to 400 kHz I^2C communication. The master and the slave mode are supported.

General PORT I/Os

11-bit PA, 16-bit PB, 13-bit PC, 6-bit PD, 16-bit PE and 12-bit PF ports are available and provide multiple functionality.

- General I/O port
- Independent bit set/clear function
- External interrupt input port
- Programmable pull-up and open-drain selection
- On-chip input debounce filter

LCD Driver

LED Driver

12-bit Analog-to-Digital Converter (ADC)

One built-in ADC can convert analog signal up to 150kSPS(sample per second) conversion rate. 14-channel analog MUX provides various combinations from external analog signals.

12-bit Digital-to-Analog Converter (DAC)

Touch

16-bit Cyclic Redundancy Check (CRC) Generator

The A31G31x series has two polynominals for CRC generator. They are CRC-CCITT and CRC-16.

1.4 Block Diagram

A31G31x is shown as below consists of a variety of peripheral devices.

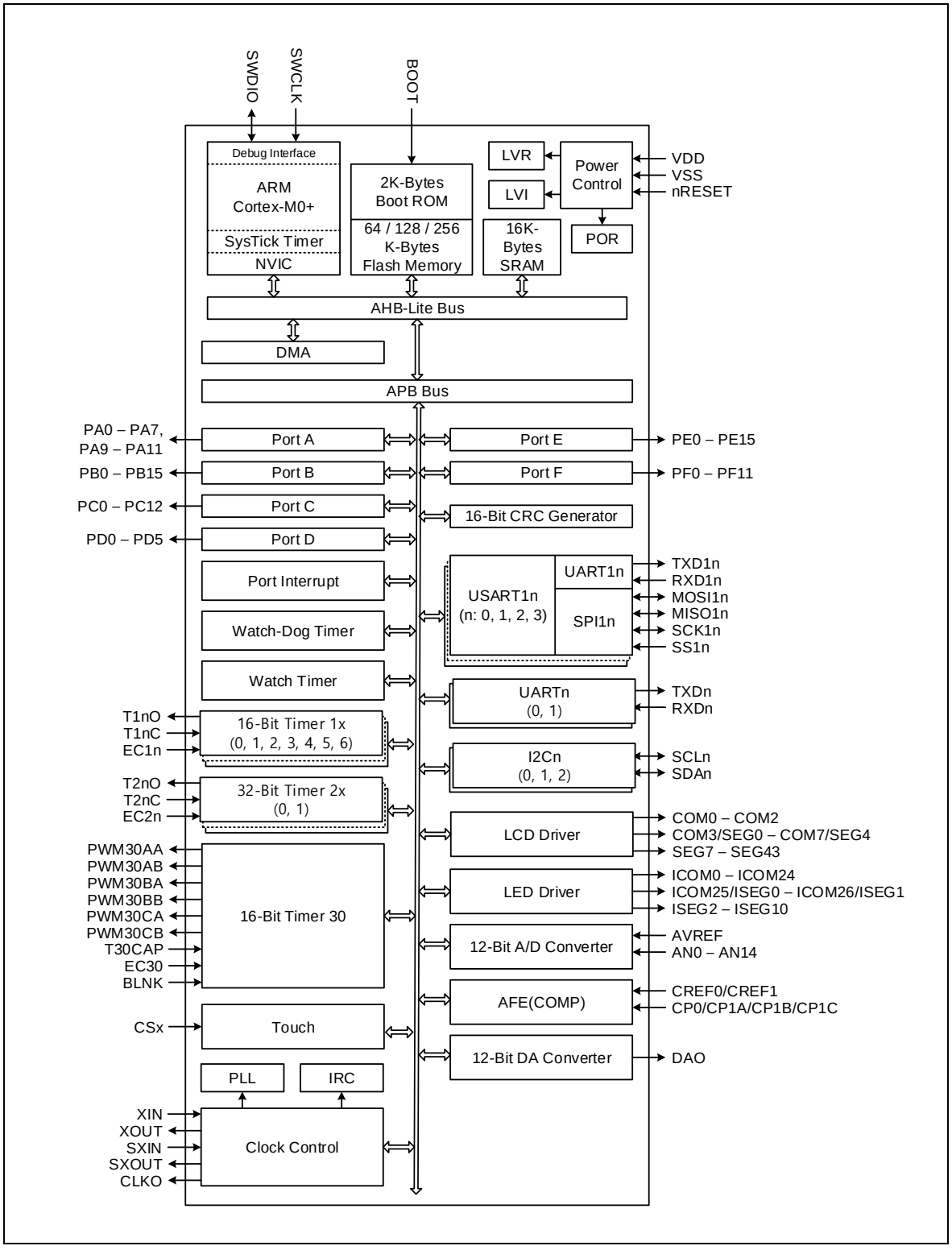


Figure 1.2 Internal block diagram of A31G31x MCUs

1.5 Pin Layout of Packages

1.5.1 A31G31xMMN (80LQFP14)

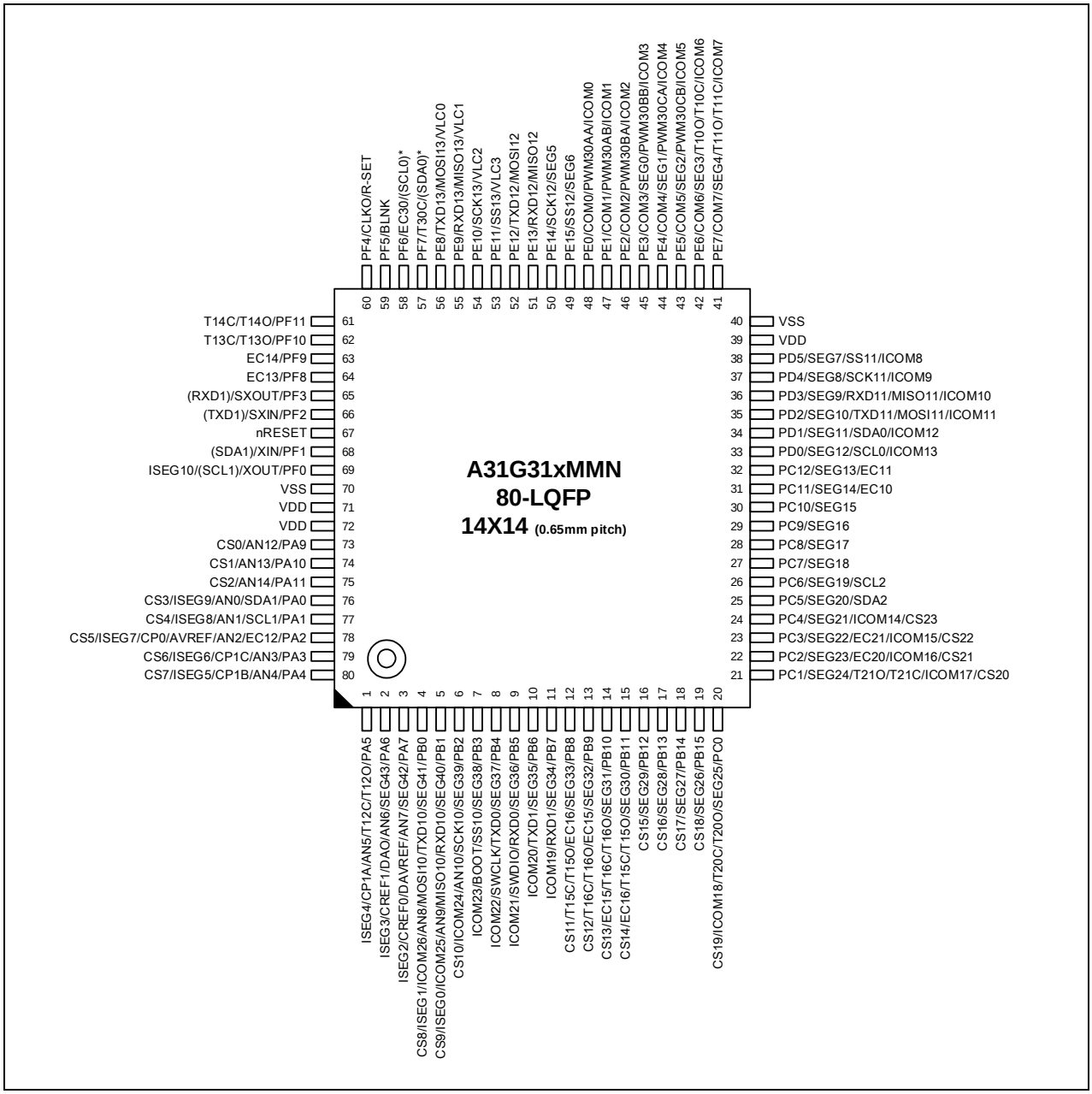


Figure 1.3 PIN LAYOUT (80LQFP14)

1.5.2 A31G31xMLN (80LQFP12)

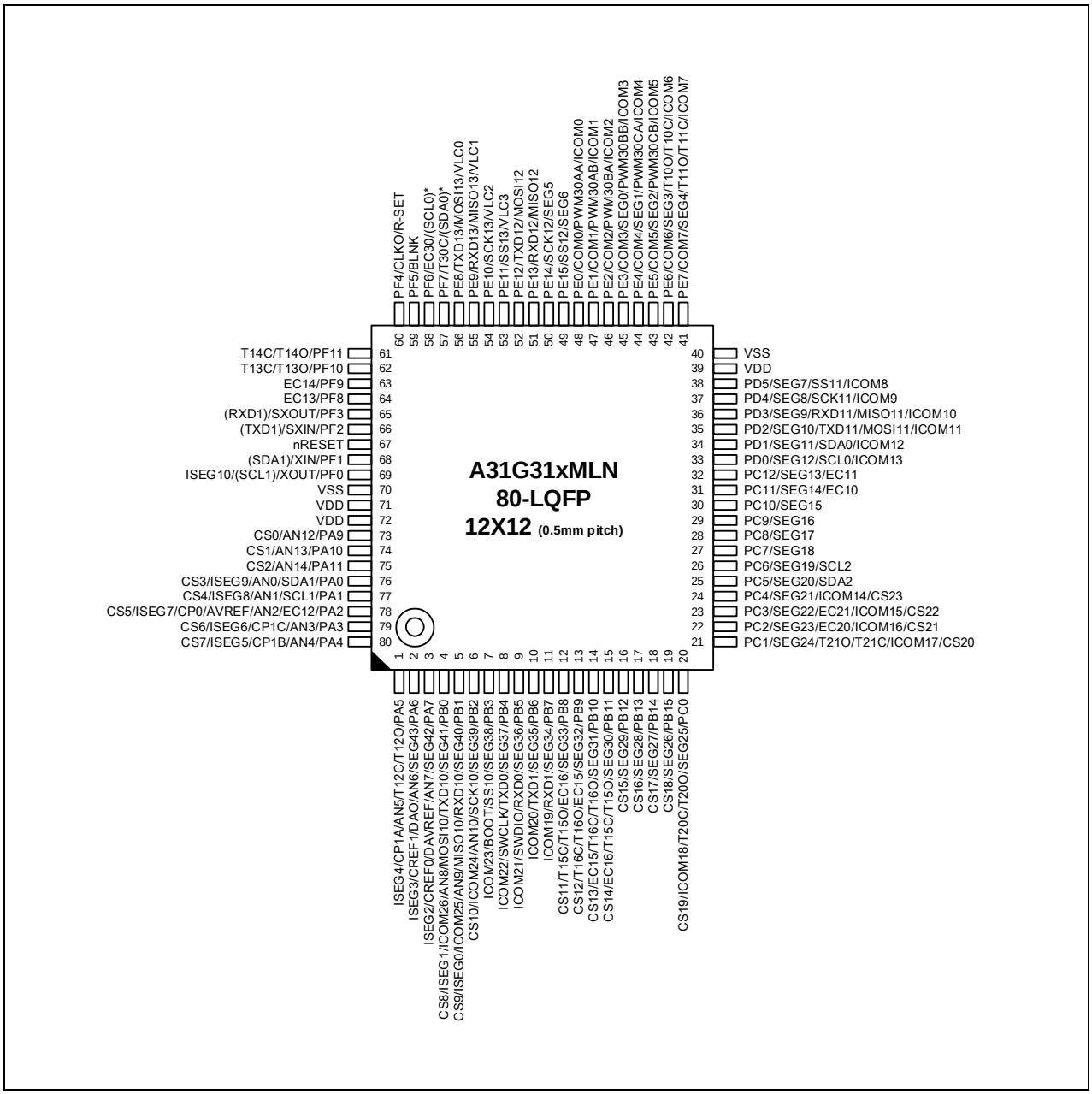


Figure 1.4 PIN LAYOUT (80LQFP12)

1.5.3 A31G31xRMN (64LQFP12)

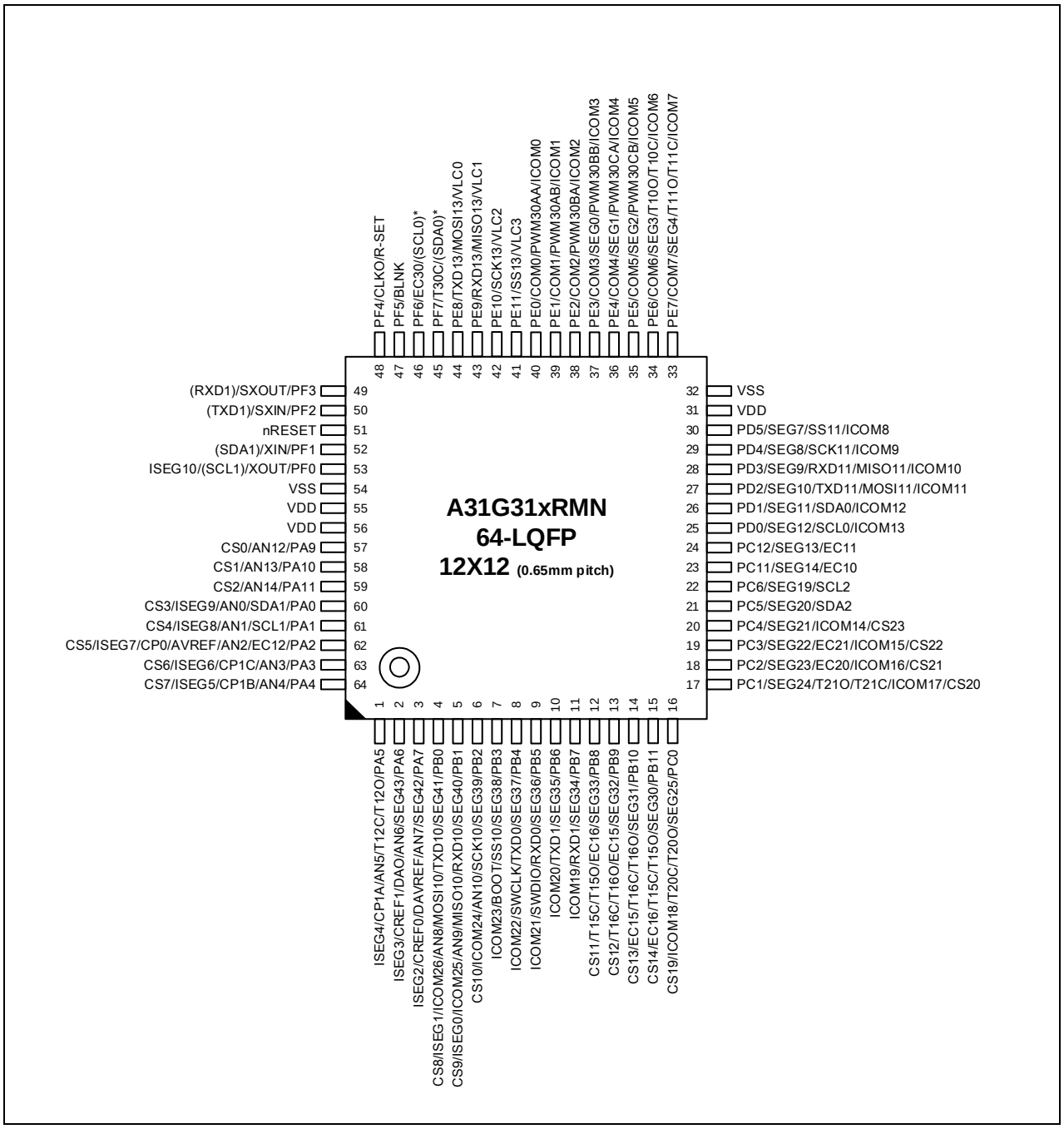


Figure 1.5 PIN LAYOUT (64LQFP12)

1.5.4 A31G31xRLN (64LQFP10)

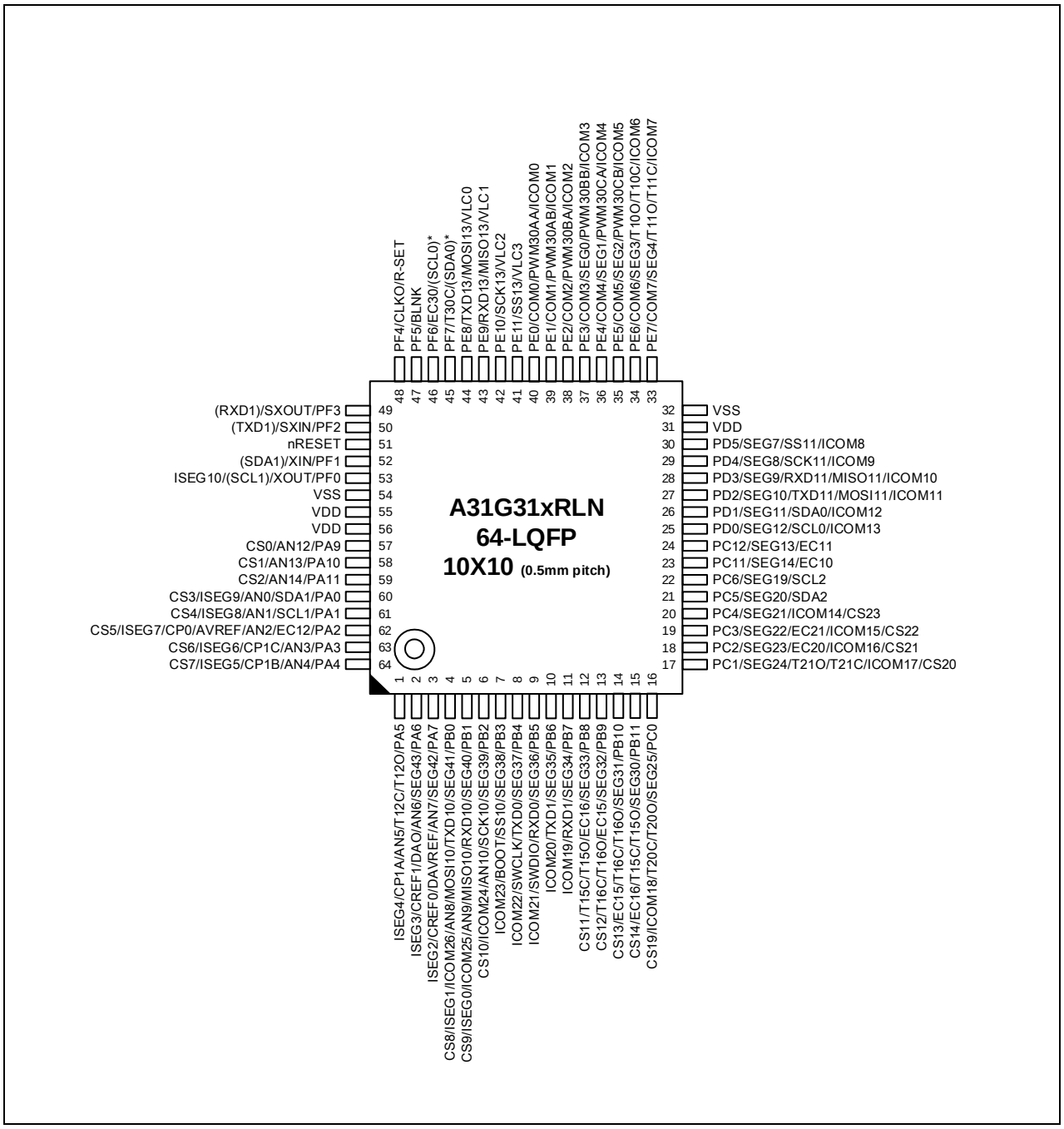


Figure 1.6 PIN LAYOUT (64LQFP10)

1.5.5 A31G31xCLN (48LQFP)

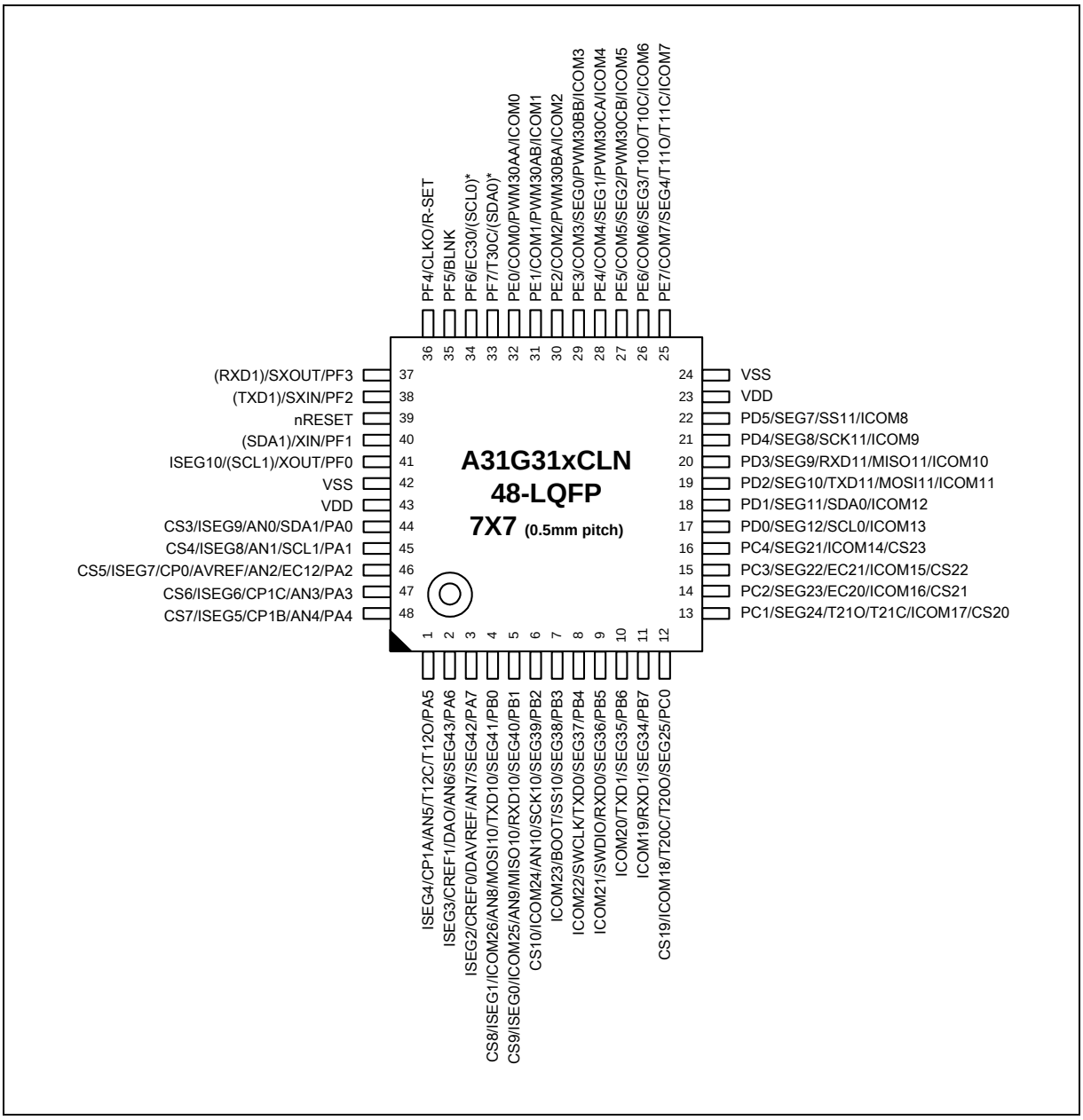


Figure 1.7 PIN LAYOUT (48LQFP)

1.5.6 A31G31xCUN (48QFN)

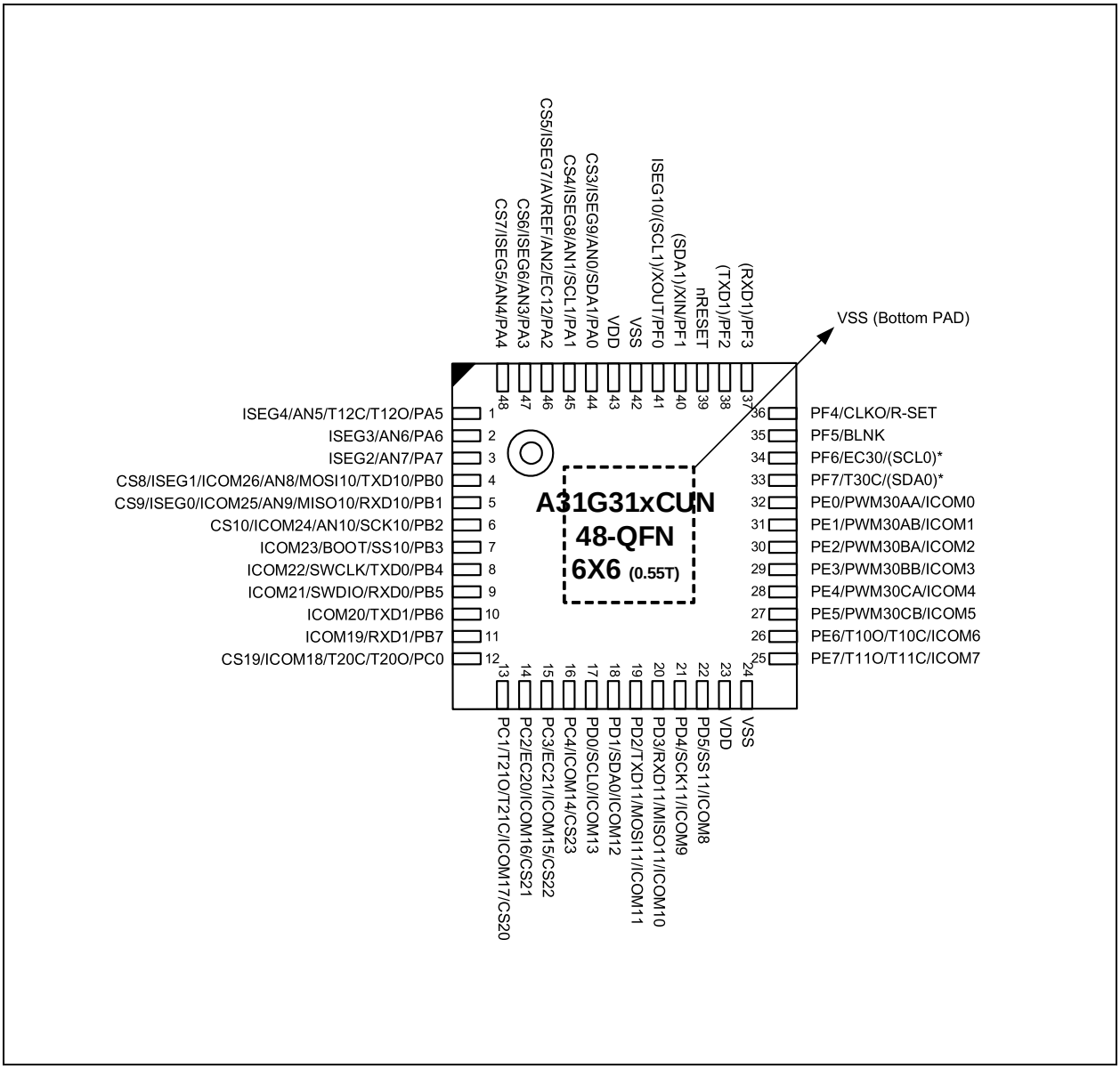


Figure 1.8 PIN LAYOUT (48QFN)

1.5.7 A31G31xSNN (44LQFP)

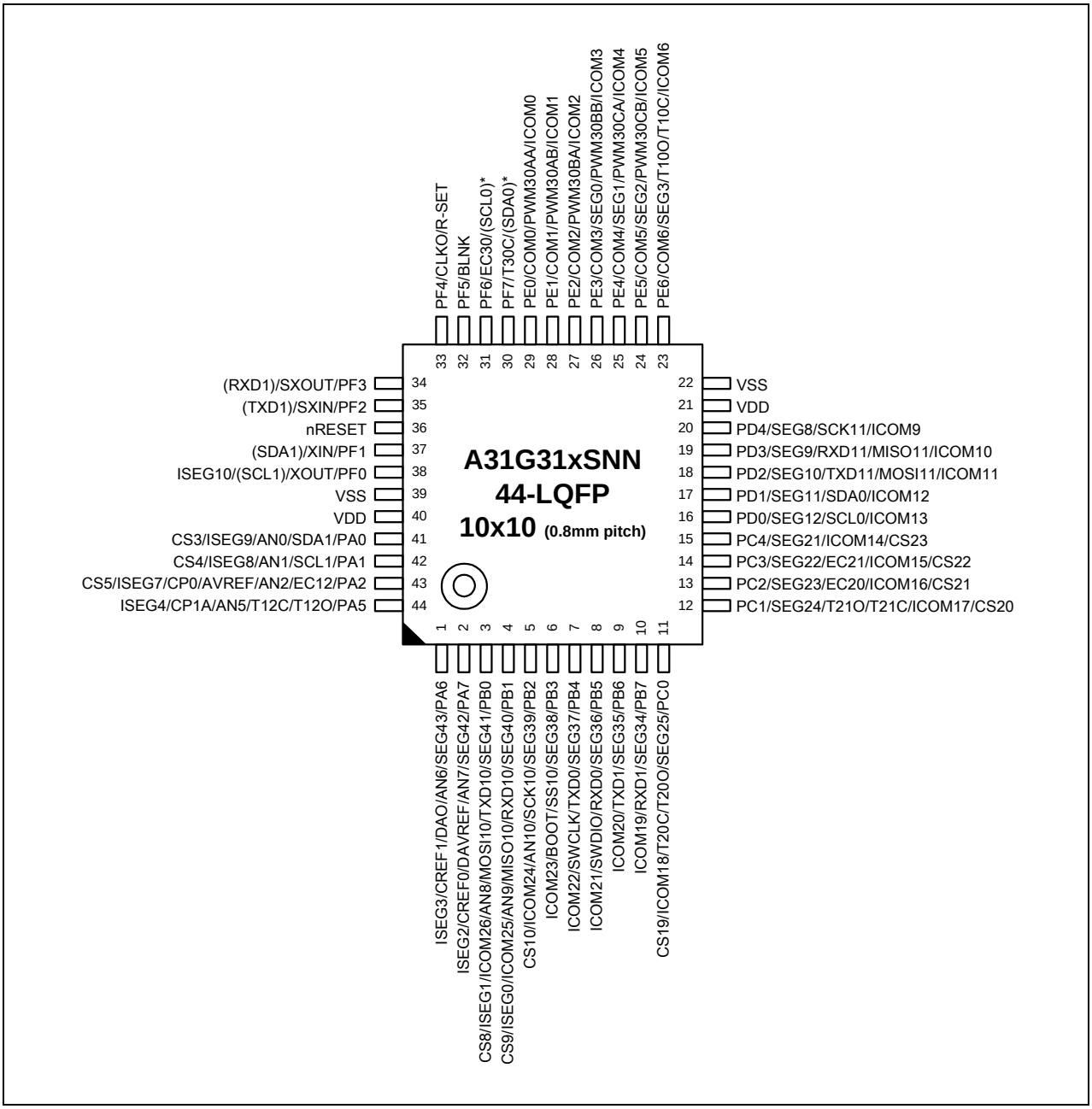


Figure 1.9 PIN LAYOUT (44LQFP)

1.6 Pin Configuration

Depending on the package type of each A31G31x microcontroller, there are some differences in the number of pins and configurations.
The pin configuration of A31G31x MCUs is as follows.

Table 1.2 Pin Configuration

Pin No				Pin Name	Type	Description	Remark
80LQFP14 80LQFP12	64LQFP12 64LQFP10	48LQFP 48QFN	44LQFP				
1	1	1	44	PA5*	IOUDS	PORT A Bit 5 Input/Output	
				T12O	O	Timer 12 Output	
				T12C	I	Timer 12 Capture Input	
				AN5	IA	Analog Input 5	
				CP1A	IA	Comparator input 1A	
				ISEG4	O	LED Segment Signal 4 Output	
2	2	2	1	PA6*	IOUDS	PORT A Bit 6 Input/Output	
				SEG43	O	LCD Segment Signal 43 Output	
				AN6	IA	Analog Input 6	
				DAO	OA	Digital to analog output	
				CREF1	IA	Comparator 1 Reference Input	
				ISEG3	O	LED Segment Signal 3 Output	
3	3	3	2	PA7*	IOUDS	PORT A Bit 7 Input/Output	
				SEG42	O	LCD Segment Signal 42 Output	
				AN7	IA	Analog Input 7	
				DAVREF	IA	D/A converter reference input	
				CREF0	IA	Comparator 0 Reference Input	
				ISEG2	O	LED Segment Signal 2 Output	
4	4	4	3	PB0	IOUDS	PORT B Bit 0 Input/Output	
				SEG41	O	LCD Segment Signal 41 Output	
				TXD10*	O	UART Channel 10 TxD Input	
				MOSI10	I/O	SPI Channel 10 Master Out / Slave In	
				AN8	IA	Analog Input 8	
				ICOM26	O	LED Common Signal 26 Output	
				ISEG1	O	LED Segment Signal 1 Output	
				CS8	IA	Capacitive Touch switch input 8	
5	5	5	4	PB1	IOUDS	PORT B Bit 1 Input/Output	
				SEG40	O	LCD Segment Signal 40 Output	
				RXD10*	I	UART Channel 10 RxD Input	
				MISO10	I/O	SPI10 Master-Input/Slave-Output Data signal	
				AN9	IA	Analog Input 9	
				ICOM25	O	LED Common Signal 25 Output	
				ISEG0	O	LED Segment Signal 0 Output	
				CS9	IA	Capacitive Touch switch input 9	
6	6	6	5	PB2*	IOUDS	PORT B Bit 2 Input/Output	
				SEG39	O	LCD Segment Signal 39 Output	
				SCK10	I/O	SPI10 Data Clock Input/Output	
				AN10	IA	Analog Input 10	
				ICOM24	O	LED Common Signal 24 Output	
				CS10	IA	Capacitive Touch switch input 10	
7	7	7	6	PB3	IOUDS	PORT B Bit 3 Input/Output	
				SEG38	O	LCD Segment Signal 38 Output	
				SS10	I/O	SPI Channel 10 Slave Select signa	

				BOOT*	I	Boot mode Selection Input	Pull-up
				ICOM23	O	LED Common Signal 23 Output	
8	8	8	7	PB4	IOUDS	PORT B Bit 4 Input/Output	
				SEG37	O	LCD Segment Signal 37 Output	
				TXD0	O	UART Channel 0 TxD Input	
				SWCLK*	I	SWD Clock Input	Pull-up
				ICOM22	O	LED Common Signal 22 Output	
9	9	9	8	PB5	IOUDS	PORT B Bit 5 Input/Output	
				SEG36	O	LCD Segment Signal 36 Output	
				RXD0	I	UART Channel 0 RxD Input	
				SWDIO*	I/O	SWD Data Input/Output	Pull-up
				ICOM21	O	LED Common Signal 21 Output	
10	10	10	9	PB6*	IOUDS	PORT B Bit 6 Input/Output	
				SEG35	O	LCD Segment Signal 35 Output	
				TXD1	O	UART Channel 1 TxD Input	
				ICOM20	O	LED Common Signal 20 Output	
11	11	11	10	PB7*	IOUDS	PORT B Bit 7 Input/Output	
				SEG34	O	LCD Segment Signal 34 Output	
				RXD1	I	UART Channel 1 RxD Input	
				ICOM19	O	LED Common Signal 19 Output	
12	12	-	-	PB8*	IOUDS	PORT B Bit 8 Input/Output	
				SEG33	O	LCD Segment Signal 33 Output	
				EC16	I	Timer 16 Event Count Input	
				T15O	O	Timer 15 Output	
				T15C	I	Timer 15 Capture Input	
				CS11	IA	Capacitive Touch switch input 11	
13	13	-	-	PB9*	IOUDS	PORT B Bit 9 Input/Output	
				SEG32	O	LCD Segment Signal 32 Output	
				EC15	I	Timer 15 Event Count Input	
				T16O	O	Timer 16 Output	
				T16C	I	Timer 16 Capture Input	
				CS12	IA	Capacitive Touch switch input 12	
14	14	-	-	PB10*	IOUDS	PORT B Bit 10 Input/Output	
				SEG31	O	LCD Segment Signal 31 Output	
				T16O	O	Timer 16 Output	
				T16C	I	Timer 16 Capture Input	
				EC15	I	Timer 15 Event Count Input	
				CS13	IA	Capacitive Touch switch input 13	
15	15	-	-	PB11*	IOUDS	PORT B Bit 11 Input/Output	
				SEG30	O	LCD Segment Signal 30 Output	
				T15O	O	Timer 15 Output	
				T15C	I	Timer 15 Capture Input	
				EC16	I	Timer 16 Event Count Input	
				CS14	IA	Capacitive Touch switch input 14	
16	-	-	-	PB12*	IOUDS	PORT B Bit 12 Input/Output	
				SEG29	O	LCD Segment Signal 29 Output	
				CS15	IA	Capacitive Touch switch input 15	
17	-	-	-	PB13*	IOUDS	PORT B Bit 13 Input/Output	
				SEG28	O	LCD Segment Signal 28 Output	
				CS16	IA	Capacitive Touch switch input 16	
18	-	-	-	PB14*	IOUDS	PORT B Bit 14 Input/Output	
				SEG27	O	LCD Segment Signal 27 Output	

				CS17	IA	Capacitive Touch switch input 17	
19	-	-	-	PB15*	IOUDS	PORT B Bit 15 Input/Output	
				SEG26	O	LCD Segment Signal 26 Output	
				CS18	IA	Capacitive Touch switch input 18	
20	16	12	11	PC0*	IOUDS	PORT C Bit 0 Input/Output	
				SEG25	O	LCD Segment Signal 25 Output	
				T20O	O	Timer 20 Output	
				T20C	I	Timer 20 Capture Input	
				ICOM18	O	LED Common Signal 18 Output	
				CS19	IA	Capacitive Touch switch input 19	
21	17	13	12	PC1*	IOUDS	PORT C Bit 1 Input/Output	
				SEG24	O	LCD Segment Signal 24 Output	
				T21O	O	Timer 21 Output	
				T21C	I	Timer 21 Capture Input	
				ICOM17	O	LED Common Signal 17 Output	
				CS20	IA	Capacitive Touch switch input 20	
22	18	14	13	PC2*	IOUDS	PORT C Bit 2 Input/Output	
				SEG23	O	LCD Segment Signal 23 Output	
				EC20	I	Timer 20 Event Count Input	
				ICOM16	O	LED Common Signal 16 Output	
				CS21	IA	Capacitive Touch switch input 21	
23	19	15	14	PC3*	IOUDS	PORT C Bit 3 Input/Output	
				SEG22	O	LCD Segment Signal 22 Output	
				EC21	I	Timer 21 Event Count Input	
				ICOM15	O	LED Common Signal 15 Output	
				CS22	IA	Capacitive Touch switch input 22	
24	20	16	15	PC4*	IOUDS	PORT C Bit 4 Input/Output	
				SEG21	O	LCD Segment Signal 21 Output	
				ICOM14	O	LED Common Signal 14 Output	
				CS23	IA	Capacitive Touch switch input 23	
25	21	-	-	PC5*	IOUDS	PORT C Bit 5 Input/Output	
				SEG20	O	LCD Segment Signal 20 Output	
				SDA2	O	I^2C Channel 2 SDA In/Out	
26	22	-	-	PC6*	IOUDS	PORT C Bit 6 Input/Output	
				SEG19	O	LCD Segment Signal 19 Output	
				SCL2	O	I^2C Channel 2 SCL In/Out	
27	-	-	-	PC7*	IOUDS	PORT C Bit 7 Input/Output	
				SEG18	O	LCD Segment Signal 18 Output	
28	-	-	-	PC8*	IOUDS	PORT C Bit 8 Input/Output	
				SEG17	O	LCD Segment Signal 17 Output	
29	-	-	-	PC9*	IOUDS	PORT C Bit 9 Input/Output	
				SEG16	O	LCD Segment Signal 16 Output	
30	-	-	-	PC10*	IOUDS	PORT C Bit 10 Input/Output	
				SEG15	O	LCD Segment Signal 15 Output	
31	23	-	-	PC11*	IOUDS	PORT C Bit 11 Input/Output	
				SEG14	O	LCD Segment Signal 14 Output	
				EC10	I	Timer 10 Event Count Input	
32	24	-	-	PC12*	IOUDS	PORT C Bit 12 Input/Output	
				SEG13	O	LCD Segment Signal 13 Output	
				EC11	I	Timer 11 Event Count Input	
33	25	17	16	PD0*	IOUDS	PORT D Bit 0 Input/Output	
				SEG12	O	LCD Segment Signal 12 Output	
				SCL0	O	I^2C Channel 0 SCL In/Out	

				ICOM13	O	LED Common Signal 13 Output	
34	26	18	17	PD1*	IOUDS	PORT D Bit 1 Input/Output	
				SEG11	O	LCD Segment Signal 11 Output	
				SDA0	O	I²C Channel 0 SDA In/Out	
				ICOM12	O	LED Common Signal 12 Output	
35	27	19	18	PD2*	IOUDS	PORT D Bit 2 Input/Output	
				SEG10	O	LCD Segment Signal 10 Output	
				TXD11	O	UART Channel 11 TxD Input	
				MOSI11	I/O	SPI Channel 11 Master Out / Slave In	
				ICOM11	O	LED Common Signal 11 Output	
36	28	20	19	PD3*	IOUDS	PORT D Bit 3 Input/Output	
				SEG9	O	LCD Segment Signal 9 Output	
				RXD11	I	UART Channel 11 RxD Input	
				MISO11	I/O	SPI11 Master-Input/Slave-Output Data signal	
				ICOM10	O	LED Common Signal 10 Output	
37	29	21	20	PD4*	IOUDS	PORT D Bit 4 Input/Output	
				SEG8	O	LCD Segment Signal 8 Output	
				SCK11	I/O	SPI11 Data Clock Input/Output	
				ICOM9	O	LED Common Signal 9 Output	
38	30	22	-	PD5*	IOUDS	PORT D Bit 5 Input/Output	
				SEG7	O	LCD Segment Signal 7 Output	
				SS11	I/O	SPI Channel 11 Slave Select signa	
				ICOM8	O	LED Common Signal 8 Output	
39	31	23	21	VDD	P	VDD	
40	32	24	22	VSS	P	VSS	
41	33	25	-	PE7*	IOUDS	PORT E Bit 7 Input/Output	
				COM7	O	LCD Common Signal 7 Outputs	
				SEG4	O	LCD Segment Signal 4 Output	
				T11O	O	Timer 11 Output	
				T11C	I	Timer 11 Capture Input	
				ICOM7	O	LED Common Signal 7 Output	
42	34	26	23	PE6*	IOUDS	PORT E Bit 6 Input/Output	
				COM6	O	LCD Common Signal 6 Output	
				SEG3	O	LCD Segment Signal 3 Output	
				T10O	O	Timer 10 Output	
				T10C	I	Timer 10 Capture Input	
				ICOM6	O	LED Common Signal 6 Output	
43	35	27	24	PE5*	IOUDS	PORT E Bit 5 Input/Output	
				COM5	O	LCD Common Signal 5 Output	
				SEG2	O	LCD Segment Signal 2 Output	
				PWM30CB	O	Timer 30 PWM Output	
				ICOM5	O	LED Common Signal 5 Output	
44	36	28	25	PE4*	IOUDS	PORT E Bit 4 Input/Output	
				COM4	O	LCD Common Signal 4 Output	
				SEG1	O	LCD Segment Signal 1 Output	
				PWM30CA	O	Timer 30 PWM Output	
				ICOM4	O	LED Common Signal 4 Output	
45	37	29	26	PE3*	IOUDS	PORT E Bit 3 Input/Output	
				COM3	O	LCD Common Signal 3 Output	
				SEG0	O	LCD Segment Signal 0 Output	

				PWM30BB	O	Timer 30 PWM Output	
				ICOM3	O	LED Common Signal 3 Output	
46	38	30	27	PE2*	IOUDS	PORT E Bit 2 Input/Output	
				COM2	O	LCD Common Signal 2 Output	
				PWM30BA	O	Timer 30 PWM Output	
				ICOM2	O	LED Common Signal 2 Output	
47	39	31	28	PE1*	IOUDS	PORT E Bit 1 Input/Output	
				COM1	O	LCD Common Signal 1 Output	
				PWM30AB	O	Timer 30 PWM Output	
				ICOM1	O	LED Common Signal 1 Output	
48	40	32	29	PE0*	IOUDS	PORT E Bit 0 Input/Output	
				COM0	O	LCD Common Signal 0 Output	
				PWM30AA	O	Timer 30 PWM Output	
				ICOM0	O	LED Common Signal 0 Output	
49	-	-	-	PE15*	IOUDS	PORT E Bit 15 Input/Output	
				SS12	I/O	SPI Channel 12 Slave Select signal	
				SEG6	O	LCD Segment Signal 6 Output	
50	-	-	-	PE14*	IOUDS	PORT E Bit 14 Input/Output	
				SCK12	I/O	SPI12 Data Clock Input/Output	
				SEG5	O	LCD Segment Signal 5 Output	
51	-	-	-	PE13*	IOUDS	PORT E Bit 13 Input/Output	
				RXD12	I	UART Channel 12 RxD Input	
				MISO12	I/O	SPI12 Master-Input/Slave-Output Data signal	
52	-	-	-	PE12*	IOUDS	PORT E Bit 12 Input/Output	
				TXD12	O	UART Channel 12 TxD Input	
				MOSI12	I/O	SPI Channel 12 Master Out / Slave In	
53	41	-	-	PE11*	IOUDS	PORT E Bit 11 Input/Output	
				SS13	I/O	SPI Channel 13 Slave Select signal	
				VLC3	IA	External LCD Voltage bias 3	
54	42	-	-	PE10*	IOUDS	PORT E Bit 10 Input/Output	
				SCK13	I/O	SPI13 Data Clock Input/Output	
				VLC2	IA	External LCD Voltage bias 2	
55	43	-	-	PE9*	IOUDS	PORT E Bit 9 Input/Output	
				RXD13	I	UART Channel 13 RxD Input	
				MISO13	I/O	SPI13 Master-Input/Slave-Output Data signal	
				VLC1	IA	External LCD Voltage bias 1	
56	44	-	-	PE8*	IOUDS	PORT E Bit 8 Input/Output	
				TXD13	O	UART Channel 13 TxD Input	
				MOSI13	I/O	SPI Channel 13 Master Out / Slave In	
				VLC0	IA	External LCD Voltage bias 0	
57	45	33	30	PF7*	IODS	PORT F Bit 7 Input/Output	Open-drain
				T30C	I	Timer 30 Capture Input	
				(SDA0)	O	I²C Channel 0 SDA In/Out	
58	46	34	31	PF6*	IODS	PORT F Bit 6 Input/Output	Open-drain
				EC30	I	Timer 30 Event Count Input	
				(SCL0)	O	I²C Channel 0 SCL In/Out	
59	47	35	32	PF5*	IODS	PORT F Bit 5 Input/Output	Open-drain
				BLINK	I	External Sync Signal Input for T30 PWM	
60	48	36	33	PF4*	IOUDS	PORT F Bit 4 Input/Output	

				CLKO	O	System Clock Output	
				R-SET	IA	LED Segment current setting	
61	-	-	-	PF11*	IOUDS	PORT F Bit 11 Input/Output	
				T14O	O	Timer 14 Output	
				T14C	I	Timer 14 Capture Input	
62	-	-	-	PF10*	IOUDS	PORT F Bit 10 Input/Output	
				T13O	O	Timer 13 Output	
				T13C	I	Timer 13 Capture Input	
63	-	-	-	PF9*	IOUDS	PORT F Bit 9 Input/Output	
				EC14	I	Timer 14 Event Count Input	
64	-	-	-	PF8*	IOUDS	PORT F Bit 8 Input/Output	
				EC13	I	Timer 13 Event Count Input	
65	49	37	34	PF3*	IOUDS	PORT F Bit 3 Input/Output	
				SXOUT	O	Sub Oscillator Output	
				(RXD1)	I	UART Channel 1 RxD Input	
66	50	38	35	PF2*	IOUDS	PORT F Bit 2 Input/Output	
				SXIN	I	Sub Oscillator Input	
				(TXD1)	O	UART Channel 1 TxD Input	
67	51	39	36	nRESET	IU	External Reset Input	Pull-up
68	52	40	37	PF1*	IOUDS	PORT F Bit 1 Input/Output	
				XIN	I	Main Oscillator Input	
				(SDA1)	O	I²C Channel 2 SDA In/Out	
69	53	41	38	PF0*	IOUDS	PORT F Bit 0 Input/Output	
				XOUT	O	Main Oscillator Output	
				(SCL1)	O	I²C Channel 2 SCL In/Out	
				ISEG10	O	LED Segment Signal 26 Output	
70	54	42	39	VSS	P	VSS	
71	55	43	40	VDD	P	VDD	
72	56	-	-	VDD	P	VDD	
73	57	-	-	PA9*	IOUDS	PORT A Bit 9 Input/Output	
				AN12	IA	Analog Input 12	
				CS0	IA	Capacitive Touch switch input 0	
74	58	-	-	PA10*	IOUDS	PORT A Bit 10 Input/Output	
				AN13	IA	Analog Input 13	
				CS1	IA	Capacitive Touch switch input 1	
75	59	-	-	PA11*	IOUDS	PORT A Bit 11 Input/Output	
				AN14	IA	Analog Input 14	
				CS2	IA	Capacitive Touch switch input 2	
76	60	44	41	PA0*	IOUDS	PORT A Bit 0 Input/Output	
				SDA1	O	I²C Channel 1 SDA In/Out	
				AN0	IA	Analog Input 0	
				ISEG9	O	LED Segment Signal 9 Output	
				CS3	IA	Capacitive Touch switch input 3	
				-	-	-	
77	61	45	42	PA1*	IOUDS	PORT A Bit 1 Input/Output	
				SCL1	O	I²C Channel 1 SCL In/Out	
				AN1	IA	Analog Input 1	
				ISEG8	O	LED Segment Signal 8 Output	
				CS4	IA	Capacitive Touch switch input 4	
				-	-	-	
78	62	46	43	PA2*	IOUDS	PORT A Bit 2 Input/Output	
				EC12	I	Timer 12 Event Count Input	

				AN2	IA	Analog Input 2	
				AVREF	IA	A/D Converter Reference Input	
				CP0	IA	Comparator plus input 0	
				ISEG7	O	LED Segment Signal 7 Output	
				CS5	IA	Capacitive Touch switch input 5	
79	63	47	-	PA3*	IOUDS	PORT A Bit 3 Input/Output	
				AN3	IA	Analog Input 3	
				CP1C	IA	Comparator plus input 1C	
				ISEG6	O	LED Segment Signal 22 Output	
				CS6	IA	Capacitive Touch switch input 6	
80	64	48	-	PA4*	IOUDS	PORT A Bit 4 Input/Output	
				AN4	IA	Analog Input 4	
				CP1B	IA	Comparator plus input 1B	
				ISEG5	O	LED Segment Signal 21 Output	
				CS7	IA	Capacitive Touch switch input 7	

Notation: I=Input, O=Output, U=Pull-up, D=Pull-down,
S=Schmitt-Trigger Input Type, C=CMOS Input Type, A=Analog, P=Power
(*) Selected pin function after reset condition
Pin order may be changed with revision notice

1.7 Memory Map

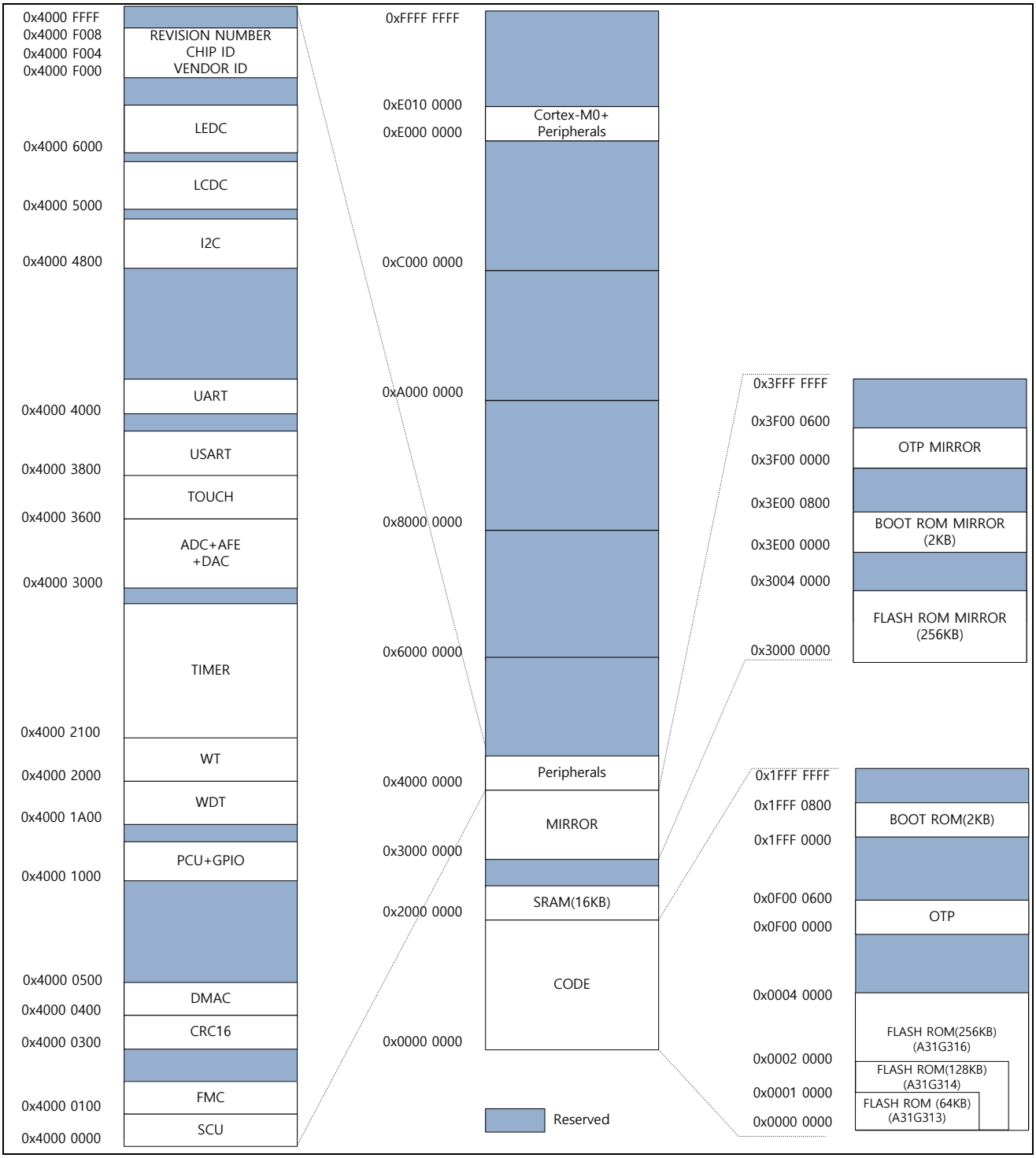


Figure 1.10 Memory Map

CHAPTER 2. CPU

2.1 Cortex-M0+ Core

The ARM® Cortex®-M0+ processor is the most energy-efficient ARM processor available. It builds on the very successful Cortex-M0+ processor, retaining full instruction set and tool compatibility, while further reducing energy consumption and increasing performance. Document “DDI 0484C” from ARM provides detail information of Cortex-M0+.

2.2 Interrupt Controller

Table 2.1 Interrupt Vector Map

Priority	Vector Address	Interrupt Source
-16	0x0000_0000	Stack Pointer
-15	0x0000_0004	Reset Address
-14	0x0000_0008	NMI Handler
-13	0x0000_000C	Hard Fault Handler
-12	0x0000_0010	Reserved
-11	0x0000_0014	
-10	0x0000_0018	
-9	0x0000_001C	
-8	0x0000_0020	
-7	0x0000_0024	
-6	0x0000_0028	
-5	0x0000_002C	SVCall Handler
-4	0x0000_0030	Reserved
-3	0x0000_0034	
-2	0x0000_0038	PenSV Handler
-1	0x0000_003C	SysTick Handler
0	0x0000_0040	LVI
1	0x0000_0044	SYSCLKFAIL
2	0x0000_0048	WDT
3	0x0000_004C	GPIOA,B
4	0x0000_0050	GPIOC,D
5	0x0000_0054	GPIOE
6	0x0000_0058	GPIOF
7	0x0000_005C	TIMER10
8	0x0000_0060	TIMER11
9	0x0000_0064	TIMER12
10	0x0000_0068	I2C0
11	0x0000_006C	USART10
12	0x0000_0070	WT
13	0x0000_0074	TIMER30
14	0x0000_0078	I2C1
15	0x0000_007C	TIMER20
16	0x0000_0080	TIMER21
17	0x0000_0084	USART11
18	0x0000_0088	ADC
19	0x0000_008C	UART0
20	0x0000_0090	UART1
21	0x0000_0094	TIMER13
22	0x0000_0098	TIMER14

23	0x0000_009C	TIMER15
24	0x0000_00A0	TIMER16
25	0x0000_00A4	I2C2
26	0x0000_00A8	USART12/USART13
27	0x0000_00AC	DAC
28	0x0000_00B0	LED
29	0x0000_00B4	TOUCH
30	0x0000_00B8	Reserved
31	0x0000_00BC	COMP/CRC

(Note)

Each interrupt has an associated priority-level register. Each of them is 2 bits wide, occupying the two MSBs of the Interrupt Priority Level Registers. Each Interrupt Priority Level Register occupies 1 byte (8 bits). NVIC registers in the Cortex-M0+ processor can only be accessed using word-size transfers, so for each access, four Interrupt Priority Level Registers are accessed at the same time.

** __NVIC_PRIO_BITS = 2

CHAPTER 3. Boot Mode

3.1 Boot Mode Pins

A31G31x has boot mode option to program internal flash memory.

Boot mode can be entered by setting BOOT pin to 'L' at reset timing. (Normal state is 'H')

The boot mode supports UART boot and SPI boot.

UART boot uses TXD10/RXD10 port, and SPI boot uses MOSI10/MISO10/SCK10/SS10 port.

The pins for boot mode are listed as following:

Table 3.1 Boot mode pin list

Block	Pin Name	Dir	Description
SYSTEM	nRESET	I	Reset Input signal
	BOOT/PB3	I	'0' to enter Boot mode
UART mode of USART10	RXD10/PB1	I	UART Boot Receive Data
	TXD10/PB0	O	UART Boot Transmit Data
SPI mode of USART10	SS10/PB3	I	SPI Boot Slave Selectable after Boot ROM
	SCK10/PB2	I	SPI Boot Clock Input
	MISO10/PB1	I	SPI Boot Data Input with function exchange
	MOSI10/PB0	O	SPI Boot Data Output with function exchange

3.2 Boot Mode Connections

User can design target board using any of boot mode ports – UART or SPI mode of USART10.
Followings are sample connection diagrams of boot mode.

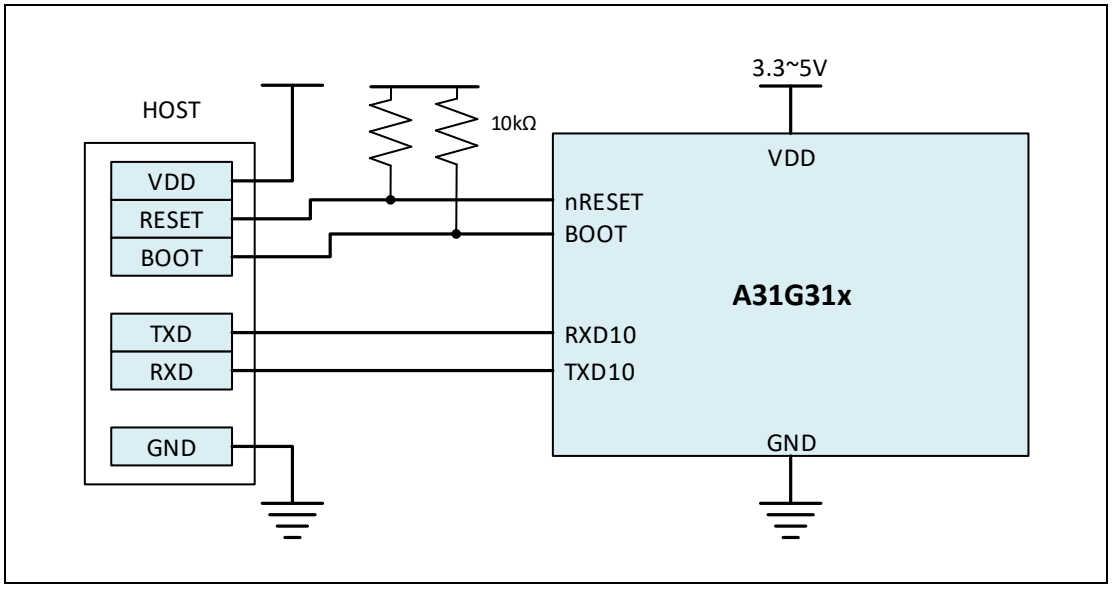
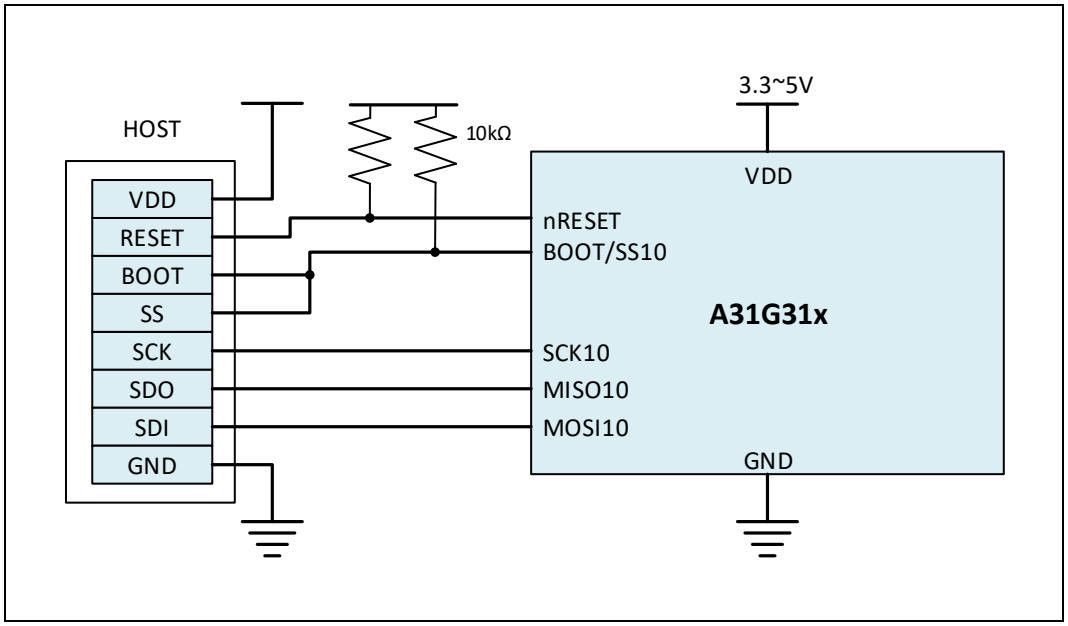


Figure 3.1 Connection diagram of UART Boot



NOTE) The MISO 10 and MOSI 10 exchange options are activated automatically in boot mode. MISO 10 must be HIGH level for using SPI Boot.

Figure 3.2 Connection diagram of SPI Boot

3.3 SWD Mode Connections

User can use the SWD mode for writing with E-PGM+.
This can be used for writing & debugging.

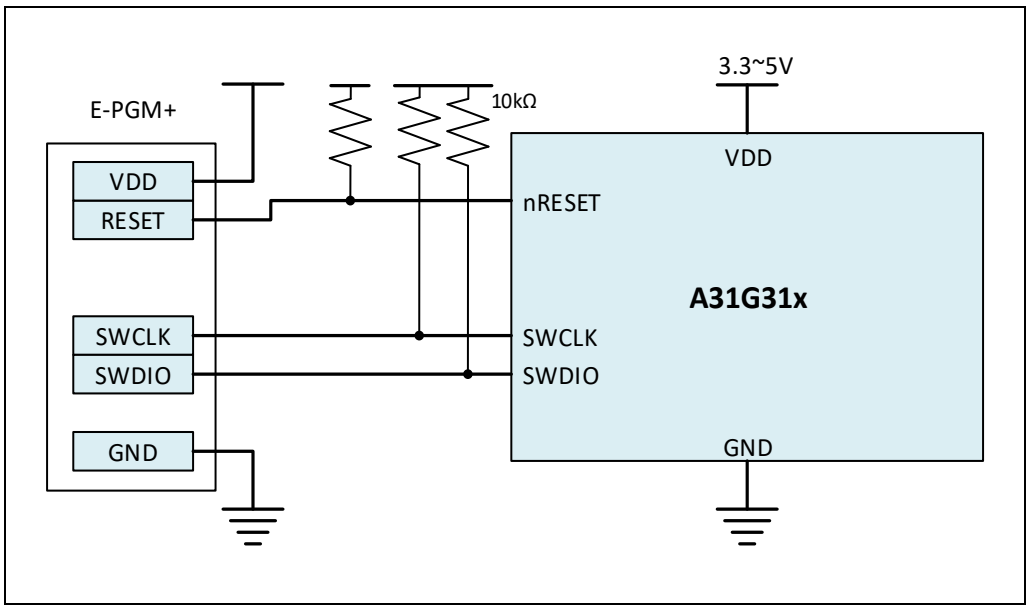


Figure 3.3 Connection diagram of E-PGM+ and SWD Port

CHAPTER 4. SYSTEM CONTROL UNIT (SCU)

4.1 OVERVIEW

The A31G31x has built-in intelligent power control block which manages system analog blocks and operating modes

Internal reset and clock signals are controlled by SCU block to maintain optimize system performance and power dissipation.

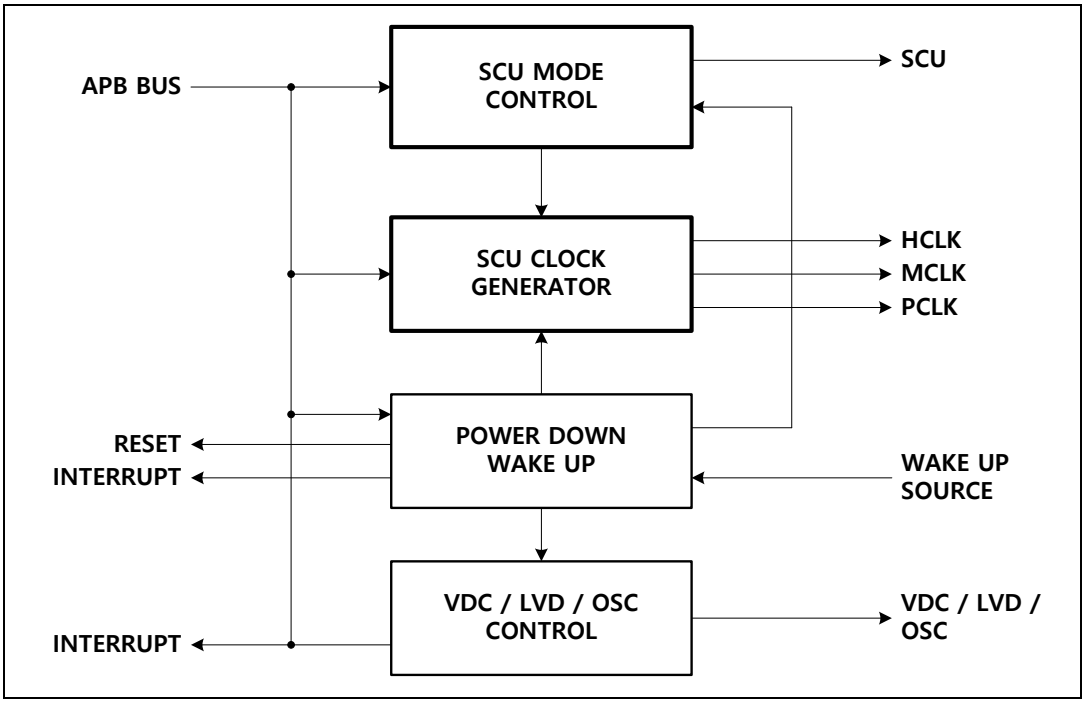


Figure 4.1 SCU Block Diagram

4.2 CLOCK SYSTEM

A31G31x has two main operating clocks. One is HCLK which supplies the clock to CPU and AHB bus system. The other one is PCLK which supplies the clock to Peripheral systems.

User can control the clock system variation by software. The below figure shows the clock system of the chip. And the below table shows clock source descriptions.

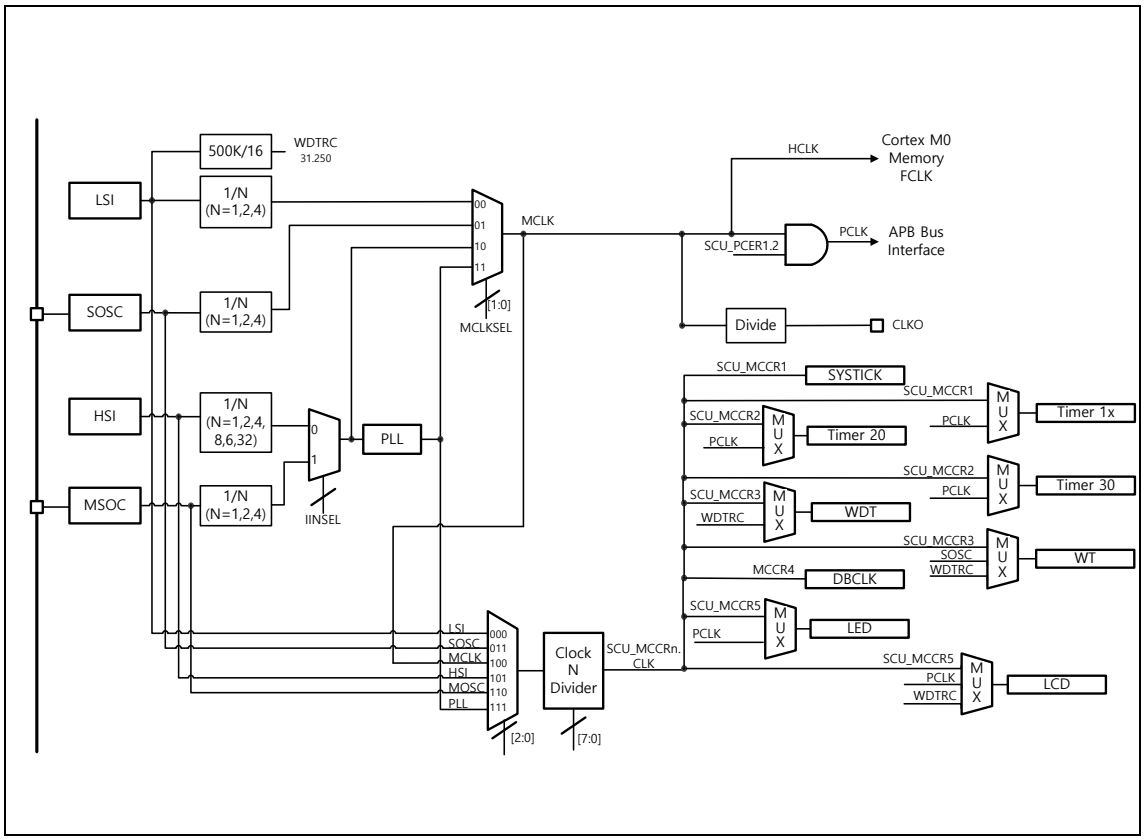


Figure 4.2 Clock Tree Configuration

All mux to switch clock source have a glitch-free circuit in each. So clock can be switched without glitch risks. When you try to change the clock mux control, both of clock sources should be alive. If one of them is not alive, clock change operation is stopped and system will be halted and not be recovered.

Table 4.1 Clock sources

Clock name	Frequency	Description
MOSC	2-16 MHz	External Crystal OSC
SOSC	32.768 kHz	External Sub Crystal OSC
HSI	48 MHz	High Speed Internal OSC
LSI	500 kHz	Low Speed Internal OSC

4.2.1 HCLK clock domain

HCLK clock feeds the clock to the CPU and AHB bus. Cortex-M0+ CPU requires 2 clocks related with HCLK clock. FCLK and HCLK. FCLK is free running clock and it is always running except power down mode. HCLK can be stopped in the sleep mode and power down mode.

BUS system and memory systems operated by MCLK clock. Max bus operating clock speed is 48MHz.

4.2.2 PCLK clock domain

PCLK is master clock of all the peripheral. Each peripheral clocks enabled by SCU_PCER1 and SCU_PCER2 registers can be used by each peripheral. Before enabling the PCLK input clock of each block, it can't be accessible even reading its registers. It can be stopped in power down mode.

4.2.3 Clock configuration procedure

After power up, the default system clock is feed by LSI (500kHz) clock. LSI is default enabled at power up sequence. The other clock sources will be enabled by user controls with the LSI system clock.

HSI (48MHz) clock can be enabled by SCU_CSCR register.

MOSC (2-16MHz) clock can be enabled by SCU_CSCR register. Before enable MOSC block, the pin mux configuration should be set for XIN, XOUT function. PF1 and PF0 pins are shared with MOSC's XIN and XOUT function – PF.MOD and PF.AFSR1 registers should be configured properly. After enabling the MOSC block, you must wait for more than 5msec time to ensure stable operation of crystal oscillation.

SOSC (32.768kHz) clock can be enabled by SCU_CSCR register. Before enable SOSC block, the pin mux configuration should be set for SXIN, SXOUT function. PF2 and PF3 pins are shared with SOSC's SXIN and SXOUT function – PF_MOD and PF_AFSR1 registers should be configured properly. After enabling the SOSC block, you must wait for more than 10msec time to ensure stable operation of crystal oscillation.

You can change the MCLK by SCU_SCCR Register.

You can find an example flow chart to configure the system clock in below Figure.

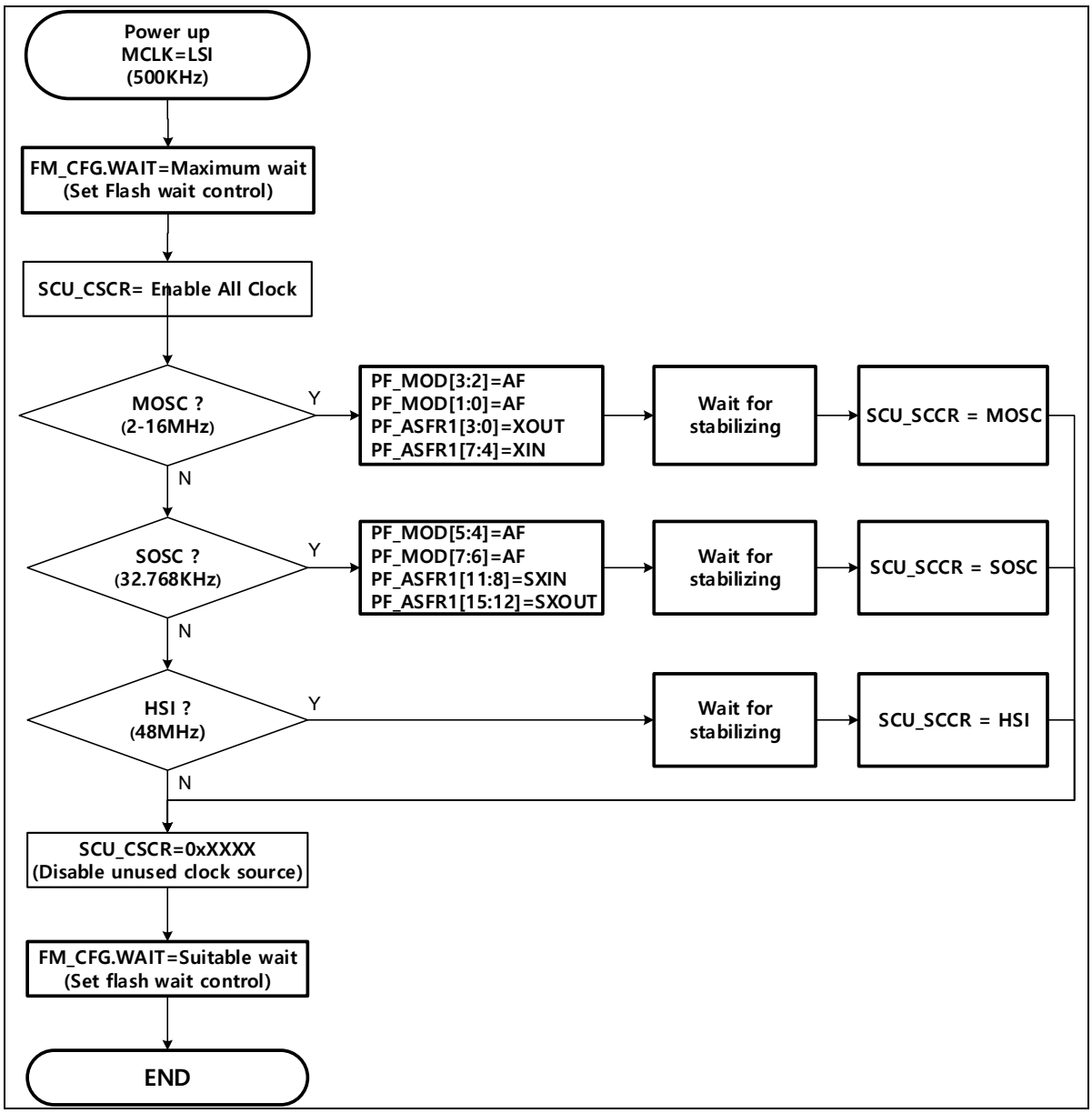


Figure 4.3 Clock change procedure

When you speed up the system clock until max operating frequency, you should check flash wait control configuration. Flash read access time is one of limitation factor for the performance. The wait control recommendation is provided in below table

Table 4.2 Flash wait control recommendation

FM.CFG.WAIT	FLASH Access Wait	Available Max System clock frequency
00	0 clock wait	~20MHz
01	1 clock wait	~40MHz
10	2 clock wait	~48MHz

4.3 RESET

A31G31x has two system reset. One is the cold reset by POR which is effective during power up or down sequence. The other reset is the warm reset which is generated by several reset sources. The reset events make the chip to turn initial state.

The cold reset has only one reset source which is POR.

The warm reset has several reset sources as below

- nRESET pin
- WDT reset
- LVD reset
- MCLK Fail reset
- MOSC Fail reset
- S/W reset
- CPU request reset

4.3.1 The Cold Reset

The cold reset is important feature of the chip when power is up. This characteristic will globally affect the system boot. Internal VDC is enabled when VDDEXT power is turn on. Internal POR trigger level is 1.6V of VDDEXT voltage out level. At this time, boot operation is started. The LSI clock is enabled and counts 4.25msec time for internal VDC level stabilizing. In this time, VDDEXT voltage level should be over than initial LVD level (1.6V). After 4.25msec counting, the cold reset is released and counts 0.4msec time for warm reset synchronizing. After released cold and warm reset, BOOTROM and CPU are running.

The below figure shows power up sequence and internal reset waveform.

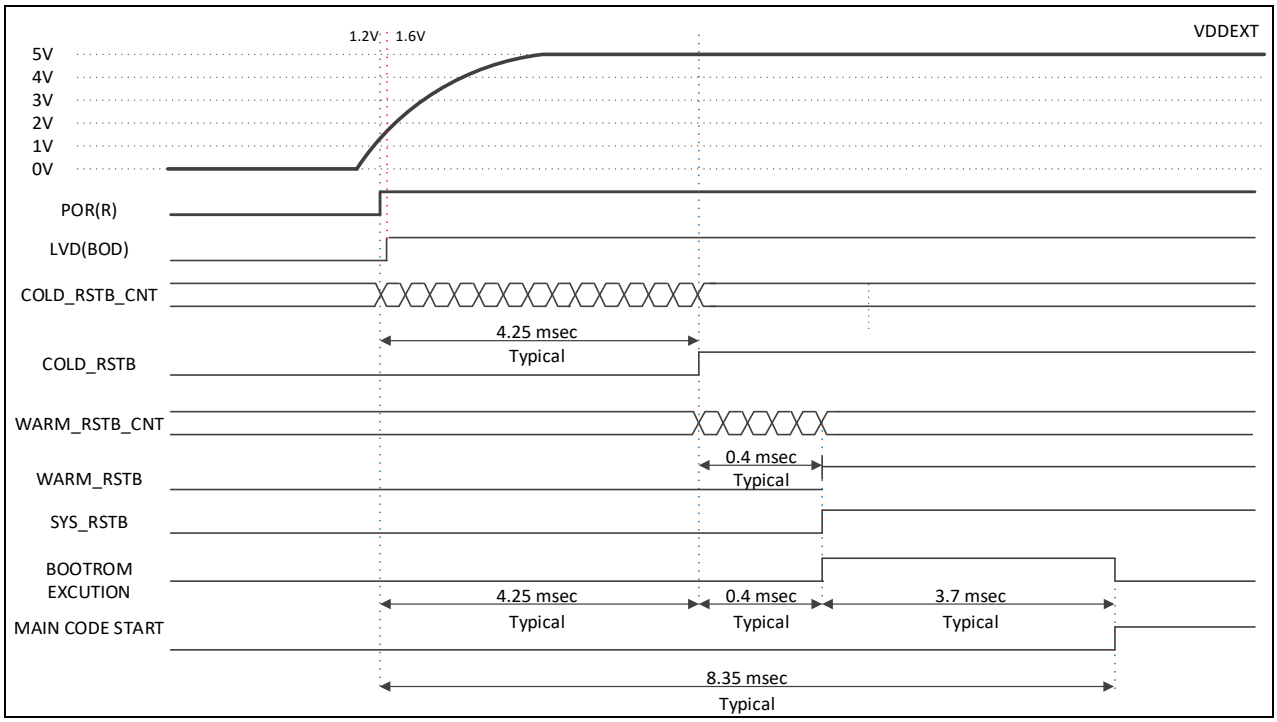


Figure 4.4 Power up procedure

4.3.2 The Warm Reset

The warm reset event has several reset sources and some parts of chip returns to initial state when warm reset condition is occurred.

The warm reset source is controlled by SCU_RSER register and the status is appeared in SCU_RSSR register. The reset for each peripheral blocks is controlled by SCU_PRER register. The reset can be masked independently.

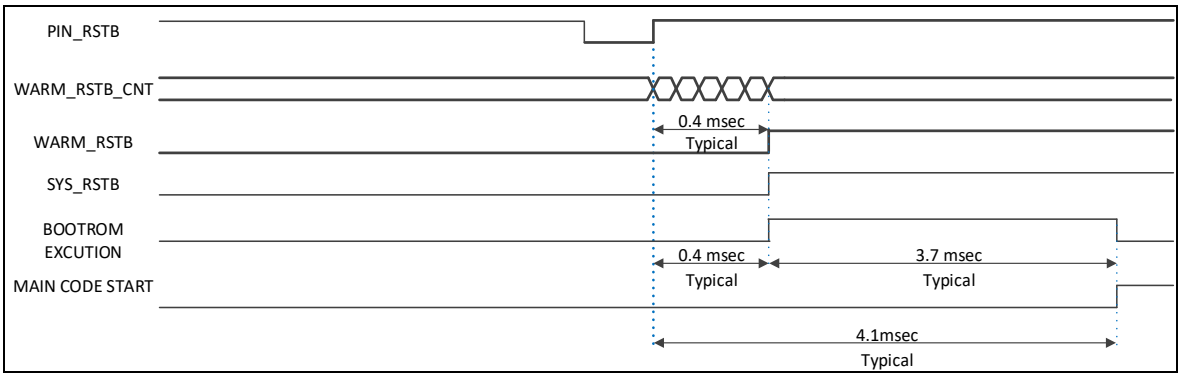


Figure 4.5 Warm reset diagram

4.3.3 The LVR Reset

The voltage level of LVR is set by the low voltage reset configuration register (SCULV_LVRCNFG).

The LVR reset status is appeared in SCU_RSSR register. The reset for LVR is controlled by SCULV_LVRCR register. The register is cleared to “0x00” on POR reset.

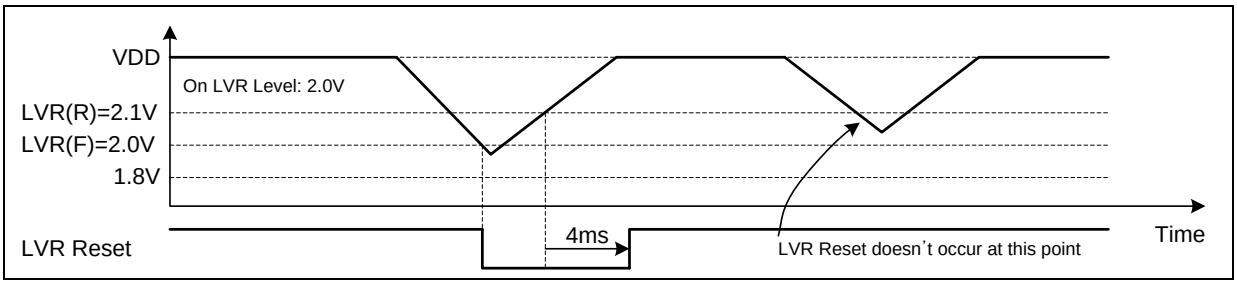


Figure 4.6 LVR Reset Timming Diagram

4.3.4 Reset Tree

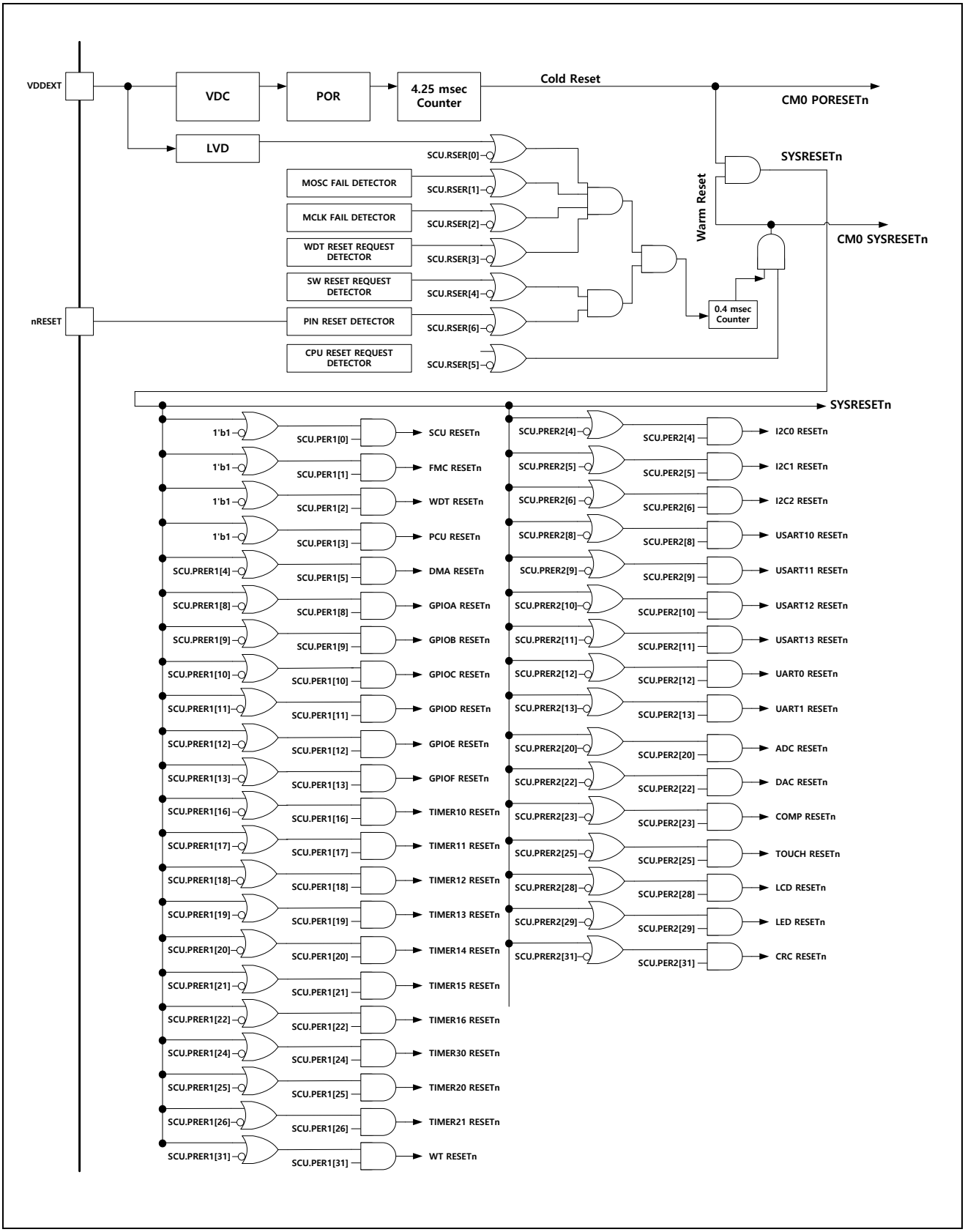


Figure 4.7 Reset tree configuration

4.4 Operation Mode

The INIT mode is initial state of the chip when reset is asserted. The RUN mode is max performance of the CPU with high-speed clock system. And the SLEEP and the PD mode can be used as the low power consumption mode. The low power consumption is achieved by halting processor core and unused peripherals.

Figure 4.8 shows the operation mode transition diagram.

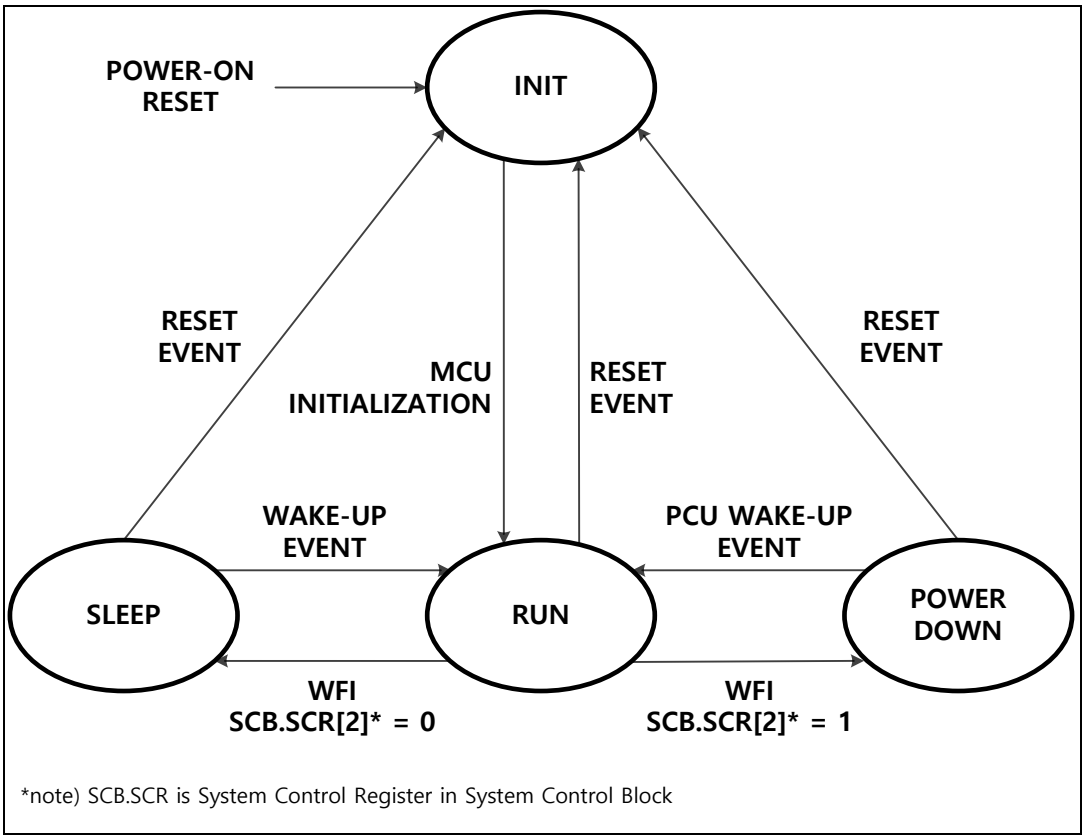


Figure 4.8 Operation Mode Block Diagram

4.4.1 RUN Mode

This mode is to operate the CPU and the peripheral hardware by using the high-speed clock. After reset followed by INIT state, it is entered into RUN mode.

4.4.2 SLEEP Mode

Only the CPU is stopped in this mode. Each peripheral function can be enabled by the function enable and clock enable bit in the SCU_PER and SCU_PCER register.

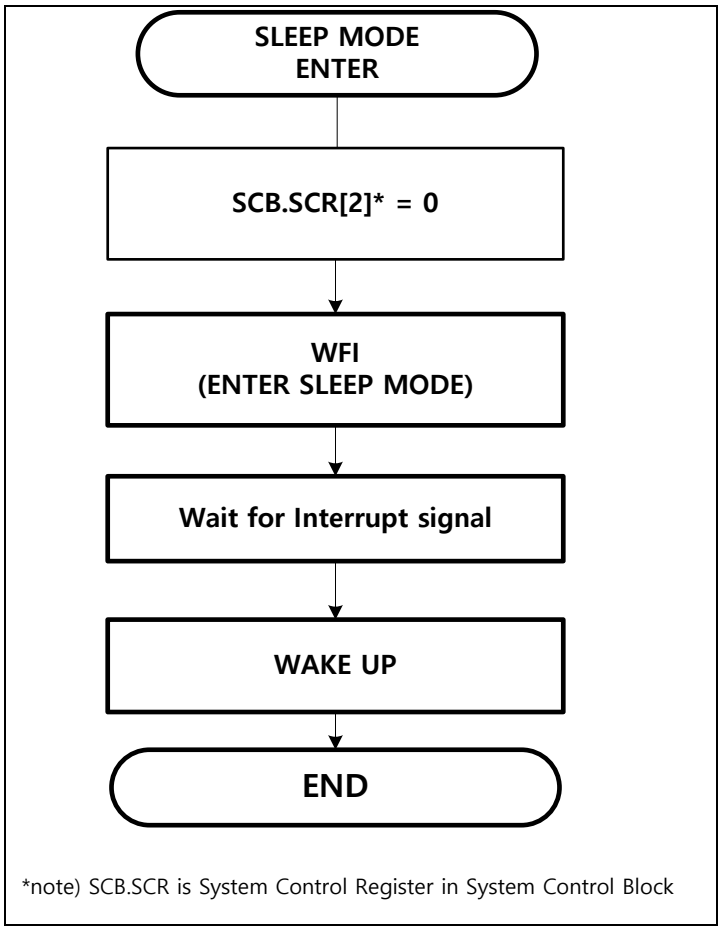


Figure 4.9 Sleep mode sequence

4.4.3 POWER-DOWN Mode

All the internal circuits are entered the stop state.

Power down operation has special power off sequence as below picture.

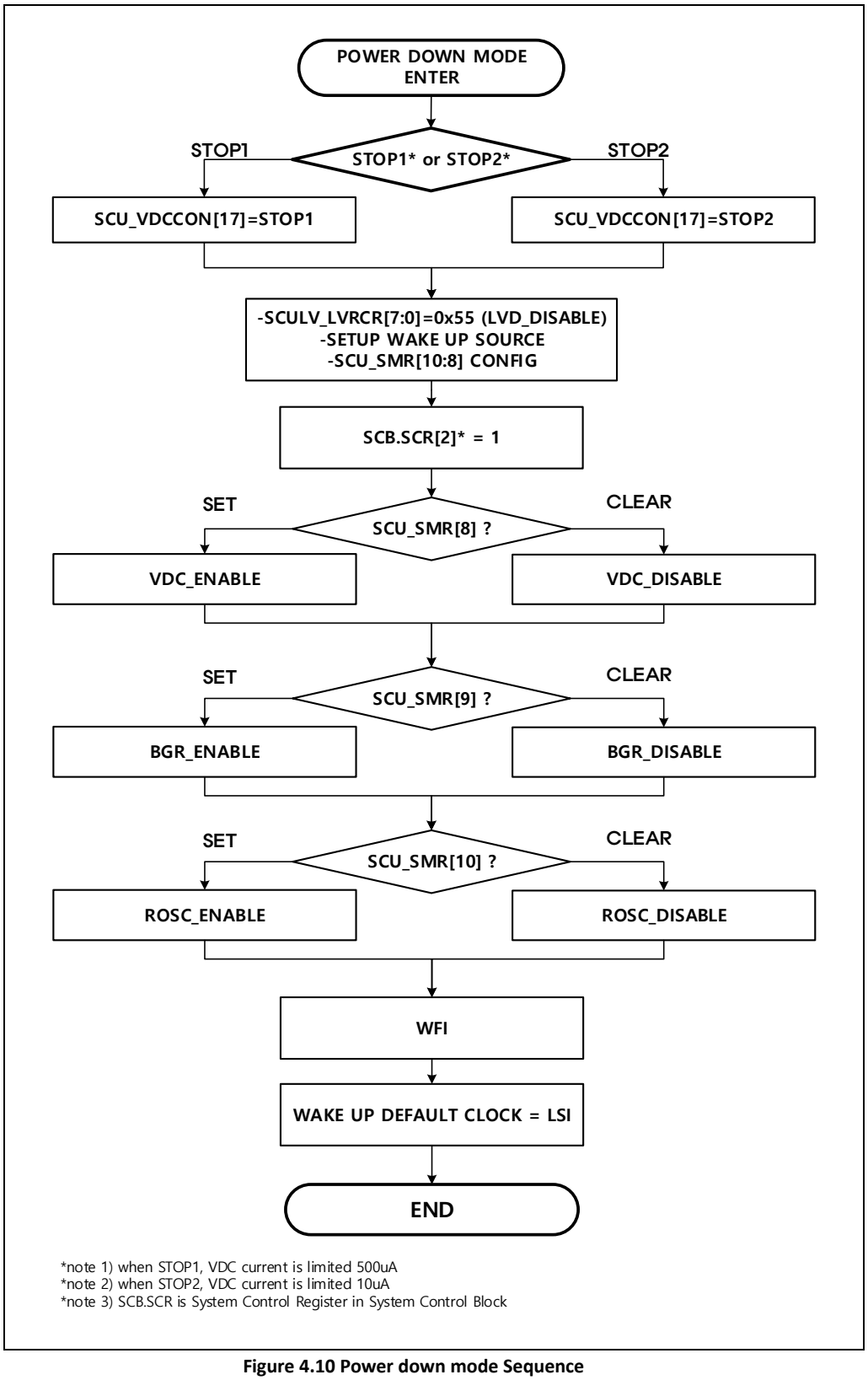


Figure 4.10 Power down mode Sequence

4.5 PIN DESCRIPTION

Table 4.3 SCU pins

PIN NAME	TYPE	DESCRIPTION
nRESET	I	External Reset Input
XIN/XOUT	OSC	External Crystal Oscillator
SXIN/SXOUT	OSC	External sub-Crystal Oscillator
CLKO	O	Clock Output Monitoring Signal

4.6 REGISTERS

Base addresse of System Control Unit(Chip Configuration) is as below.

Table 4.4 Base address of SCU

NAME	BASE ADDRESS
SCUCC (Chip Configuration)	0x4000_F000

Table 4.5 SCU Register Map (Chip Configuration)

Register Name	Offset	Access Type	Description	Initial Value	Ref
SCUCC_VENDORID	0x00	RO	Vendor Identification Register	0x4142_4F56	4.6.1
SCUCC_CHIPID	0x04	RO	Chip Identification Register	0x4D31_A00x	4.6.2
SCUCC_REVNR	0x08	RO	Revision Number Register	0x0000_0001	4.6.3

Base addresse of System Control Unit is as below.

Table 4.6. Base address of SCU

NAME	BASE ADDRESS
SCU	0x4000_0000

Table 4.7 SCU Register Map

Register Name	Offset	Access Type	Description	Initial Value	Ref
SCU_SMR	0x04	RW	System Mode Register	0x0000_0000	4.6.4
SCU_SCR	0x08	RW	System Control Register	0x0000_0000	4.6.5
SCU_WUER	0x10	RW	Wake Up source Enable Register	0x0000_0000	4.6.6
SCU_WUSR	0x14	RO	Wake Up source Status Register	0x0000_0000	4.6.7
SCU_RSER	0x18	RW	Reset Source Enable Register	0x0000_0069	4.6.8
SCU_RSSR	0x1C	RW	Reset Source Status Register	0x0000_0080*	4.6.9
SCU_PRER1	0x20	RW	Peripheral Reset Enable Register 1	0x877F_3F1F*	4.6.10
SCU_PRER2	0x24	RW	Peripheral Reset Enable Register 2	0xB3D3_3F70*	4.6.11
SCU_PER1	0x28	RW	Peripheral Enable Register 1	0x0000_000F*	4.6.12
SCU_PER2	0x2C	RW	Peripheral Enable Register 2	0x0000_0100*	4.6.13
SCU_PCER1	0x30	RW	Peripheral Clock Enable Register 1	0x0000_000F*	4.6.14
SCU_PCER2	0x34	RW	Peripheral Clock Enable Register 2	0x0000_0100*	4.6.15
SCU_PPCLKSR	0x38	RW	Peripheral Clock Selection Register	0x0000_0000	4.6.16
SCU_CSCR	0x40	RW	Clock Source Control Register	0x0000_0800	4.6.17
SCU_SCCR	0x44	RW	System Clock Control Register	0x0000_0000	4.6.18
SCU_CMR	0x48	RW	Clock Monitoring Register	0x0000_0090	4.6.19
SCU_NMIR	0x4C	RW	NMI control Register	0x0000_0000	4.6.20
SCU_COR	0x50	RW	Clock Output control Register	0x0000_000F	4.6.21
SCU_PLLCON	0x60	RW	PLL Control Register	0x0000_0000	4.6.22
SCU_VDCCON	0x64	RW	VDC Control Register	0x0000_007F	4.6.23
SCU_LSICON	0x6C	RW	Low Speed Internal OSC Control Register	0x0000_0001	4.6.24
SCU_EOSCR	0x80	RW	External Oscillator control Register	0x0000_1014	4.6.25
SCU_EMODR	0x84	RW	External mode pin read Register	0x0000_0000	4.6.26
SCU_RSTDBCR	0x88	RW	Pin Reset Debounce Control Register	0x0000_0000	4.6.27
SCU_MCCR1	0x90	RW	Misc Clock Control Register 1	0x0000_0000	4.6.28

SCU_MCCR2	0x94	RW	Misc Clock Control Register 2	0x0000_0000	4.6.29
SCU_MCCR3	0x98	RW	Misc Clock Control Register 3	0x0000_0000	4.6.30
SCU_MCCR4	0x9C	RW	Misc Clock Control Register 4	0x0000_0000	4.6.31
SCU_MCCR5	0xA0	RW	Misc Clock Control Register 5	0x0000_0000	4.6.32

Base addresse of LVI/LVR unit is as below.

Table 4.8 LVI/LVR base address

NAME	BASE ADDRESS
SCULV (LVI/LVR)	0x4000_5100

Table 4.9 LVI/LVR Register map

Register Name	Offset	Access Type	Description	Initial Value	Ref
SCULV_LVICR	0x00	RW	Low Voltage Indicator Control Register	0x0000_0000	4.6.34
SCULV_LVRCR	0x04	RW	Low Voltage Reset Control Register	0x0000_0000	4.6.35
SCULV_LVRCNFIG	0x08	RW	Configuration for Low Voltage Reset	0x0000_000F	4.6.36

4.6.1 SCUCC_VENDORID Vendor ID Register

SCUCC_VENDERID Register shows Vendor identification information.

This register is 32-bit read-only register.

SCUCC_VENDORID=0x4000_F000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VENDID																															
0x4142_4F56																															
RO																															

31 0	VENDID	Vendor Identification bits. 0x4142_4F56

4.6.2 SCUCC_CHIPID Chip ID Register

SCUCC_CHIPID Register shows Chip identification information.

This register is 32-bit read-only register.

SCU_CHIPID=0x4000_F004

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CHIPID																															
0x4D31_A003 or 0x4D31_A004 or 0x4D31_A005																															
RO																															

31 0	CHIPID	Chip Identification bits.	
		0x4D31A003	128k bytes flash memory for program
		0x4D31A004	64k bytes flash memory for program
		0x4D31A005	256k bytes flash memory for program

4.6.3 SCUCC_REVNR Revision Number Register

Revision Number register is 32-bit read-only register. This Register is able to 32/16/8-bit access.

SCUCC_REVNR is a 32-bit read-only register which is 32/16/8-bit accessible.

SCU_REVNR=0x4000_F008

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																								REVNO							
-																								0x01							
-																								RO							

7 0	REVNO	Chip Revision Number. These bits are fixed by manufacturer.

4.6.4 SCU_SMR System Mode Register

Current operating mode is shown in this SCU mode register. The previous operating mode will be saved in this register after reset event. There is VDC On/Off control bit in power down mode.

Power/internal OSC-related setting with power down mode can be set up in this SCU_SMR. The previous operating mode will be saved in this register after reset event.

SCU_SMR=0x4000_0004

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																					LSIAON	BGRAON	VDCAON	Reserved		PREVMODE		Reserved			
-																					0	0	0	-		00		-			
-																					RW	RW	RW	-		RO		-			

Bits	Name	Function
10	LSIAON	LSI Always on select bit in power down mode
		0 LSI is automatically off entering power down mode
		1 LSI isn't automatically off entering power down mode
9	BGRAON	BGR Always on select bit in power down mode
		0 BGR is automatically off entering power down mode
		1 BGR isn't automatically off entering power down mode
8	VDCAON	VDC Always on select bit in power down mode
		0 VDC is automatically off entering power down mode
		1 VDC isn't automatically off entering power down mode
5	PREVMODE	Previous operating mode before current reset event
4		00 Previous operating mode was RUN mode
		01 Previous operating mode was SLEEP mode
		10 Previous operating mode was Power Down mode
		11 Previous operating mode was INIT mode

4.6.5 SCU_SCR System Control Register

It is possible to reset MCU as SWRST bit set.

System Mode Register is 32-bit register.

It is possible to reset MCU as SWRST bit in SCU_SCR set which is a 32-bit register.

SCU_SCR=0x4000_0008

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
WTIDKY																Reserved															SWRST
0x0000																-															0
WO																-															RW

Bits	Name	Function
31 16	WTIDKY	Write Identification Key On writes, write 0x9EB3 to these bits, otherwise the write is ignored.
0	SWRST	Internal soft reset activation bit (check RSER[4] for reset) 0 Normal operation 1 Internal soft reset generated and auto cleared

4.6.6 SCU_WUER Wakeup Source Enable Register

Enable wakeup source when the chip is in the Power Down mode. Wakeup sources which will be used the source of chip wakeup should be enabled in each bit field. If the source is used as a wakeup source, the corresponding bit should be written with '1'. If the source is not used as a wakeup source, the bit should be written with '0'.

Wakeup sources which will be used the source of chip wakeup from power down mode should be enabled in each bit field in this SCU_WUER. If the source is used as a wakeup source, the corresponding bit should be written with '1' otherwise '0'.

SCU_WUER=0x4000_0010

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																		GPIOFWUE	GPIOEWUE	GPIODWUE	GPIOCWUE	GPIOBWUE	GPIOAWUE	Reserved					WTWUE	WDTWUE	LVDWUE
-																		0	0	0	0	0	0	-					0	0	0
-																		RW	RW	RW	RW	RW	RW	-					RW	RW	RW

Bits	Name	Function
13	GPIOFWUE	Enable wakeup source of GPIOF port pin change event
		0 Not used for wakeup source
		1 Enable the wakeup event generation
12	GPIOEWUE	Enable wakeup source of GPIOE port pin change event
		0 Not used for wakeup source
		1 Enable the wakeup event generation
11	GPIODWUE	Enable wakeup source of GPIOD port pin change event
		0 Not used for wakeup source
		1 Enable the wakeup event generation
10	GPIOCWUE	Enable wakeup source of GPIOC port pin change event
		0 Not used for wakeup source
		1 Enable the wakeup event generation
9	GPIOBWUE	Enable wakeup source of GPIOB port pin change event
		0 Not used for wakeup source
		1 Enable the wakeup event generation
8	GPIOAWUE	Enable wakeup source of GPIOA port pin change event
		0 Not used for wakeup source
		1 Enable the wakeup event generation
2	WTWUE	Enable wakeup source of watch timer event
		0 Not used for wakeup source
		1 Enable the wakeup event generation
1	WDTWUE	Enable wakeup source of watchdog timer event
		0 Not used for wakeup source
		1 Enable the wakeup event generation
0	LVDWUE	Enable wakeup source of LVD event
		0 Not used for wakeup source
		1 Enable the wakeup event generation

4.6.7 SCU_WUSR Wakeup Source Status Register

When the system is waked up by any wakeup source, the wakeup source is identified by reading this register. When a bit is set 1, the related wakeup source issues the wake-up instruction to the SCU. The bit will be cleared when the event source is cleared by the software.

SCU_WUSR=0x4000_0014

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																		GPIOFWU	GPIOEWU	GPIODWU	GPIOCWU	GPIOBWU	GPIOAWU	Reserved					WTWU	WDTWU	LVDWU
-																		0	0	0	0	0	0	-					0	0	0
-																		RO	RO	RO	RO	RO	RO	-					RO	RO	RO

Bits	Name	Function
13	GPIOFWU	Status of wakeup source of GPIOF port pin change event
		0 No wakeup event
		1 Wakeup event was generated
12	GPIOEWU	Status of wakeup source of GPIOE port pin change event
		0 No wakeup event
		1 Wakeup event was generated
11	GPIODWU	Status of wakeup source of GPIOD port pin change event
		0 No wakeup event
		1 Wakeup event was generated
10	GPIOCWU	Status of wakeup source of GPIOC port pin change event
		0 No wakeup event
		1 Wakeup event was generated
9	GPIOBWU	Status of wakeup source of GPIOB port pin change event
		0 No wakeup event
		1 Wakeup event was generated
8	GPIOAWU	Status of wakeup source of GPIOA port pin change event
		0 No wakeup event
		1 Wakeup event was generated
2	WTWU	Status of wakeup source of watch timer event
		0 No wakeup event
		1 Wakeup event was generated
1	WDTWU	Status of wakeup source of watchdog timer event
		0 No wakeup event
		1 Wakeup event was generated
0	LVDWU	Status of wakeup source of LVD event
		0 No wakeup event
		1 Wakeup event was generated

4.6.8 SCU_RSER Reset Source Enable Register

Reset source to the CPU can be selected by SCU_RSER register. When writing '1' in the bit field of each reset source, the reset source event will be transferred to reset generator. When writing '0' in the bit field of each reset source, the reset source event will be masked and not generate the reset event.

SCU_RSER=0x4000_0018

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																									PINRST	CPURST	SWRST	WDTRST	MCKFRST	MOFRST	LVDRST
-																									1	1	0	1	0	0	1
-																									RW	RW	RW	RW	RW	RW	RW

Bits	Name	Function
6	PINRST	External pin reset enable bit
		0 Reset from this event is masked
		1 Reset from this event is enabled
5	CPURST	CPU request reset enable bit
		0 Reset from this event is masked
		1 Reset from this event is enabled
4	SWRST	Software reset enable bit
		0 Reset from this event is masked
		1 Reset from this event is enabled
3	WDTRST	Watchdog Timer reset enable bit
		0 Reset from this event is masked
		1 Reset from this event is enabled
2	MCKFRST	MCLK Clock fail reset enable bit
		0 Reset from this event is masked
		1 Reset from this event is enabled
1	MOFRST	MOSC Clock fail reset enable bit
		0 Reset from this event is masked
		1 Reset from this event is enabled
0	LVDRST	LVD reset enable bit
		0 Reset from this event is masked
		1 Reset from this event is enabled

4.6.9 SCU_RSSR Reset Source Status Register

This SCU_RSSR shows that the reset source information when reset event is occurred. '1' shows that reset event was exist and '0' shows that reset event is not exist for corresponding reset source.

Write '1' into the corresponding bit will clear the reset status.

SCU_RSSR=0x4000_001C

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																								PORST	PINRST	CPURST	SWRST	WDTRST	MCKFRST	MOFRST	LVDRST
-																								1	0	0	0	0	0	0	0
-																								RW	RW	RW	RW	RW	RW	RW	RW

Bits	Name	Function
7	PORST	Power on reset status bit
		0 Read : Reset from this event was not exist Write : no effect
		1 Read :Reset from this event was occurred Write : Clear the status
6	PINRST	External pin reset status bit
		0 Read : Reset from this event was not exist Write : no effect
		1 Read :Reset from this event was occurred Write : Clear the status
5	CPURST	CPU request reset status bit
		0 Read : Reset from this event was not exist Write : no effect
		1 Read :Reset from this event was occurred Write : Clear the status
4	SWRST	Software reset status bit
		0 Read : Reset from this event was not exist Write : no effect
		1 Read :Reset from this event was occurred Write : Clear the status
3	WDTRST	Watchdog Timer reset status bit
		0 Read : Reset from this event was not exist Write : no effect
		1 Read :Reset from this event was occurred Write : Clear the status
2	MCKFRST	MCLK Clock fail reset status bit
		0 Read : Reset from this event was not exist Write : no effect
		1 Read :Reset from this event was occurred Write : Clear the status
1	MOFRST	MOSC Clock fail reset status bit
		0 Read : Reset from this event was not exist Write : no effect
		1 Read :Reset from this event was occurred Write : Clear the status
0	LVDRST	LVD reset status bit
		0 Read : Reset from this event was not exist Write : no effect
		1 Read :Reset from this event was occurred Write : Clear the status

4.6.10 SCU_PRER1 Peripheral Reset Enable Register 1

The reset of each peripheral by event reset, can be masked by user setting. SCU_PRER1/SCU_PRER2 registers will control the enablement of the event reset. If the corresponding bit is '1', the peripheral corresponded with this bit, accepts the reset event. Otherwise, the peripheral is protected from reset event and maintain current operation.

SCU_PRER1=0x4000_0020

31	30 29 28 27	26	25	24	23	22	21	20	19	18	17	16	15 14	13	12	11	10	9	8	7 6 5	4	3	2	1	0
WT	Reserved	TIMER21	TIMER20	TIMER30	Reserved	TIMER16	TIMER15	TIMER14	TIMER13	TIMER12	TIMER11	TIMER10	Reserved	GPIOF	GPIOE	GPIOD	GPIOC	GPIOB	GPIOA	Reserved	DMA	PCU	WDT	FMC	SCU
1	-	1	1	1	-	1	1	1	1	1	1	1	-	1	1	1	1	1	1	-	1	1	1	1	1
RW	-	RW	RW	RW	-	RW	RW	RW	RW	RW	RW	RW	-	RW	RW	RW	RW	RW	RW	-	RW	RW	RW	RW	RW

Bits	Name	Function
31	WT	WT reset mask
26	TIMER21	TIMER21 reset mask
25	TIMER20	TIMER20 reset mask
24	TIMER30	TIMER30 reset mask
22	TIMER16	TIMER16 reset mask
21	TIMER15	TIMER15 reset mask
20	TIMER14	TIMER14 reset mask
19	TIMER13	TIMER13 reset mask
18	TIMER12	TIMER12 reset mask
17	TIMER11	TIMER11 reset mask
16	TIMER10	TIMER10 reset mask
13	GPIOF	GPIOF reset mask
12	GPIOE	GPIOE reset mask
11	GPIOD	GPIOD reset mask
10	GPIOC	GPIOC reset mask
9	GPIOB	GPIOB reset mask
8	GPIOA	GPIOA reset mask
4	DMA	DMA reset mask
3	PCU	Port controller reset mask
2	WDT	Watchdog Timer reset mask
1	FMC	Flash memory controller reset mask
0	SCU	Power Management Unit reset mask

4.6.11 SCU_PRER2 Peripheral Reset Enable Register 2

Peripheral Reset Enable Register 2 is 32-bit register.

SCU_PRER2=0x4000_0024

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CRC	Reserved	LED	LCD	Reserved		TOUCH	Reserved	COMP	DAC	Reserved	ADC	Reserved				Reserved		UART1	UART0	USART13	USART12	USART11	USART10	Reserved	I2C2	I2C1	I2C0	Reserved			
1	-	1	1	-		1	-	1	1	-	1	-				-		1	1	1	1	1	1	-	1	1	1	-			
RW	-	RW	RW	-		RW	-	RW	RW	-	RW	-				-		RW	RW	RW	RW	RW	RW	-	RW	RW	RW	-			

Bits	Name	Function
31	CRC	CRC reset enable
29	LED	LED reset enable
28	LCD	LCD reset enable
25	TOUCH	TOUCH reset enable
23	COMP	COMP reset enable
22	DAC	DAC reset enable
20	ADC	ADC reset enable
13	UART1	UART1 reset enable
12	UART0	UART0 reset enable
11	USART13	USART13 reset enable
10	USART12	USART12 reset enable
9	USART11	USART11 reset enable
8	USART10	USART10 reset enable
6	I2C2	I2C2 reset enable
5	I2C1	I2C1 reset enable
4	I2C0	I2C0 reset enable

4.6.12 SCU_PER1 Peripheral Enable Register 1

To use peripheral unit, it should be activated by writing '1' to the correspond bit in the SCU_PER1/SCU_PER2 registers. Before the activation, the peripheral will stay in reset state.

All the peripherals enabled by default. To disable the peripheral unit, write '0' to the correspond bit in the SCU_PER1/SCU_PER2 registers, and then the peripheral enter the reset state.

SCU_PER1=0x4000_0028

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
WT	Reserved				TIMER21	TIMER20	TIMER30	Reserved	TIMER16	TIMER15	TIMER14	TIMER13	TIMER12	TIMER11	TIMER10	Reserved		GPIOF	GPIOE	GPIOD	GPIOC	GPIOB	GPIOA	Reserved			DMA	Reserved			
0	-				0	0	0	0	0	0	0	0	0	0	0	-		0	0	0	0	0	0				0	1111			
RW	-				RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	-		RW	RW	RW	RW	RW	RW	-			RW	RO			

Bits	Name	Function
31	WT	WT function enable
26	TIMER21	TIMER21 function enable
25	TIMER20	TIMER20 function enable
24	TIMER30	TIMER30 function enable
22	TIMER16	TIMER16 function enable
21	TIMER15	TIMER15 function enable
20	TIMER14	TIMER14 function enable
19	TIMER13	TIMER13 function enable
18	TIMER12	TIMER12 function enable
17	TIMER11	TIMER11 function enable
16	TIMER10	TIMER10 function enable
13	GPIOF	GPIOF function enable
12	GPIOE	GPIOE function enable
11	GPIOD	GPIOD function enable
10	GPIOC	GPIOC function enable
9	GPIOB	GPIOB function enable
8	GPIOA	GPIOA function enable
4	DMA	DMA function enable

4.6.13 SCU_PER2 Peripheral Enable Register 2

To use peripheral unit, it should be activated by writing '1' to the correspond bit in the SCU_PER1/SCU_PER2 registers. Before the activation, the peripheral will stay in reset state.

All the peripherals enabled by default. To disable the peripheral unit, write '0' to the correspond bit in the SCU_PER1/SCU_PER2 registers, and then the peripheral enter the reset state.

SCU_PER2=0x4000_002C

31	30	29	28	27 26	25	24	23	22	21	20	19 18 17 16	15 14	13	12	11	10	9	8	7	6	5	4	3 2 1 0
CRC	Reserved	LED	LCD	Reserved	TOUCH	Reserved	COMP	DAC	Reserved	ADC	Reserved	Reserved	UART1	UART0	USART13	USART12	USART11	USART10	Reserved	I2C2	I2C1	I2C0	Reserved
0	-	0	0	-	0	-	0	0	-	0	-	-	0	0	0	0	0	1		0	0	0	-
RW	-	RW	RW	-	RW	-	RW	RW	-	RW	-	-	RW	RW	RW	RW	RW	RW	-	RW	RW	RW	-

Bits	Name	Function
31	CRC	CRC function enable
29	LED	LED function enable
28	LCD	LCD function enable
25	TOUCH	TOUCH function enable
23	COMP	COMP function enable
22	DAC	DAC function enable
20	ADC	ADC function enable
13	UART1	UART1 function enable
12	UART0	UART0 function enable
11	USART13	USART13 function enable
10	USART12	USART12 function enable
9	USART11	USART11 function enable
8	USART10	USART10 function enable
6	I2C2	I2C2 function enable
5	I2C1	I2C1 function enable
4	I2C0	I2C0 function enable

4.6.14 SCU_PCER1 Peripheral Clock Enable Register 1

To use peripheral unit, its clock should be activated by writing '1'to the corresponding bit in the SCU_PCER1/SCU_PCER2 register. Before enablement its clock, the peripheral won't operate properly.

To disable the clock of the peripheral unit, write '0'to the correspond bit in the SCU_PCER1/ SCU_PCER2 register, and then the clock of the peripheral is stopped.

SCU_PCER1=0x4000_0030

31	30 29 28 27	26	25	24	23	22	21	20	19	18	17	16	15 14	13	12	11	10	9	8	7 6 5	4	3 2 1 0
WT	Reserved	TIMER21	TIMER20	TIMER30	Reserved	TIMER16	TIMER15	TIMER14	TIMER13	TIMER12	TIMER11	TIMER10	Reserved	GPIOF	GPIOE	GPIOD	GPIOC	GPIOB	GPIOA	Reserved	DMA	Reserved
0	-	0	0	0	-	0	0	0	0	0	0	0	-	0	0	0	0	0	0	-	0	1111
RW	-	RW	RW	RW	-	RW	RW	RW	RW	RW	RW	RW	-	RW	RW	RW	RW	RW	RW	-	RW	RO

Bits	Name	Function
31	WT	WT clock enable
26	TIMER21	TIMER21 clock enable
25	TIMER20	TIMER20 clock enable
24	TIMER30	TIMER30 clock enable
22	TIMER16	TIMER16 clock enable
21	TIMER15	TIMER15 clock enable
20	TIMER14	TIMER14 clock enable
19	TIMER13	TIMER13 clock enable
18	TIMER12	TIMER12 clock enable
17	TIMER11	TIMER11 clock enable
16	TIMER10	TIMER10 clock enable
13	GPIOF	GPIOF clock enable
12	GPIOE	GPIOE clock enable
11	GPIOD	GPIOD clock enable
10	GPIOC	GPIOC clock enable
9	GPIOB	GPIOB clock enable
8	GPIOA	GPIOA clock enable
4	DMA	DMA clock enable

4.6.15 SCU_PCER2 Peripheral Clock Enable Register 2

To use peripheral unit, its clock should be activated by writing '1'to the corresponding bit in the SCU_PCER1/SCU_PCER2 register. Before enablement its clock, the peripheral won't operate properly.

To disable the clock of the peripheral unit, write '0'to the correspond bit in the SCU_PCER1/ SCU_PCER2 register, and then the clock of the peripheral is stopped.

SCU_PCER2=0x4000_0034

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CRC	Reserved	LED	LCD	Reserved		TOUCH	Reserved	COMP	DAC	Reserved	ADC	Reserved				Reserved		UART1	UART0	USART13	USART12	USART11	USART10	Reserved	I2C2	I2C1	I2C0	Reserved			
0	-	0	0	-		0	-	0	0	-	0	-				-		0	0	0	0	0	1	-	0	0	0	-			
RW	-	RW	RW	-		RW	-	RW	RW	-	RW	-				-		RW	RW	RW	RW	RW	RW	-	RW	RW	RW	-			

Bits	Name	Function
31	CRC	CRC clock enable
29	LED	LED clock enable
28	LCD	LCD clock enable
25	TOUCH	TOUCH clock enable
23	COMP	COMP clock enable
22	DAC	DAC clock enable
20	ADC	ADC clock enable
13	UART1	UART1 clock enable
12	UART0	UART0 clock enable
11	USART13	USART13 clock enable
10	USART12	USART12 clock enable
9	USART11	USART11 clock enable
8	USART10	USART10 clock enable
6	I2C2	I2C2 clock enable
5	I2C1	I2C1 clock enable
4	I2C0	I2C0 clock enable

4.6.16 SCU_PPCLKSR Peripheral Clock Selection Register

SCU_PPCLKSR is a 32-bit register. This Register is able to 32/16/8-bit access.

This register sets the clock source for peripherals.

SCU_PPCLKSR =0x4000_0038

31 30 29 28 27 26 25 24	23	22	21	20	19	18	17	16	15 14 13 12 11	10	9	8	7	6	5	4	3	2	1	0
Reserved		T1xCLK	Reserved	T20CLK	Reserved		T30CLK		Reserved	LEDCLK	Reserved		LCDCLK		Reserved	WTCLK		Reserved		WDTCLK
-		0	-	0	-		0		-	0	-		00		-	00		-		0
-		RW	-	RW	-		RW		-	RW	-		RW		-	RW		-		RW

22	T1xCLK	Timer 1x Clock Selection bit
		0 MCCR1 Timer1x clock
		1 PCLK clock
20	T20CLK	Timer 20 Clock Selection bit
		0 MCCR2 Timer20 clock
		1 PCLK clock
17	T30CLK	Timer 30 Clock Selection bit
		0 MCCR2 Timer30 clock
		1 PCLK clock
10	LEDCLK	LED Clock Selection bit
		0 MCCR5 LED clock
		1 PCLK clock
7 6	LCDCLK	LCD Driver Clock Selection bit
		00 MCCR5 LCD clock
		01 SOSC clock
		10 WDTRC clock
		11 Reserved
4 3	WTCLK	Watch Timer Clock Selection bit
		00 MCCR3 WT clock
		01 SOSC clock
		10 WDTRC clock
		11 Reserved
		Note) 1. These bits should be changed during the WTEN bit of watch timer control register (WTCR) is “0b”.
0	WDTCLK	Watch-dog Timer Clock Selection bit
		0 WDTRC clock
		1 MCCR3 WDT clock

4.6.17 SCU_CSCR Clock Source Control Register

The A31G31x has multiple clock sources to generate internal operating clocks. Each clock sources can be controlled by SCU_CSCR register.

SCU_CSCR=0x4000_0040

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
WTIDKY		SOSCCON	LSICON	HSICON	MOSCCON
0x0000		0000	1000	0000	0000
WO		RW	RW	RW	RW

Bits	Name	Function
31 16	WTIDKY	Write Identification Key On writes, write 0xA507 to these bits, otherwise the write is ignored.
15 12	SOSCCON	External crystal sub oscillator control 0XXX Disable external sub crystal oscillator 1000 Enable external sub crystal oscillator 1001 Enable external sub crystal oscillator divide by 2 1010 Enable external sub crystal oscillator divide by 4 Other Reserved Note) Divided SOSC(/2 /4) cannot use as MCLK with clock monitoring block. For Divided SOSC(/2, /4) is used as MCLK, Clock monitoring must be turn off before clock change.
11 8	LSICON	Low speed internal oscillator control 0XXX Disable low speed internal oscillator 1000 Enable low speed internal oscillator 1001 Enable low speed internal oscillator divide by 2 1010 Enable low speed internal oscillator divide by 4 Other Reserved
7 4	HSICON	High speed internal oscillator control 0XXX Disable high speed internal oscillator 1000 Enable high speed internal oscillator 1001 Enable high speed internal oscillator divide by 2 1010 Enable high speed internal oscillator divide by 4 1011 Enable high speed internal oscillator divide by 8 1100 Enable high speed internal oscillator divide by 16 1101 Enable high speed internal oscillator divide by 32 1111 Reserved
3 0	MOSCCON	External crystal main oscillator control 0XXX Disable external main crystal oscillator 1000 Enable external main crystal oscillator 1001 Enable external main crystal oscillator divide by 2 1010 Enable external main crystal oscillator divide by 4 Other Reserved

4.6.18 SCU_SCCR System Clock Control Register

Select the system clock source in SCU_SCCR, and selected clock source becomes MCLK. Before changing clock, clock sources have to be alive by SCU_CSCR register.

SCU_SCCR=0x4000_0044

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
WTIDKY																Reserved													FINSEL	MCLKSEL	
0x0000																-													0	00	
WO																-													RW	RW	

Bits	Name	Function
31 16	WTIDKY	Write Identification Key On writes, write 0x570A to these bits, otherwise the write is ignored.
2	FINSEL	PLL input source FIN select register
		0 HSI clock is used as FIN clock
		1 MOSC clock is used as FIN clock
1 0	MCLKSEL	System clock select register
		00 LSI (500kHz)
		01 SOSC XTAL (32kHz)
		10 PLL bypassed clock
		11 PLL output clock

Note) When change MCLKSEL, both clock sources should be alive.
Ex) Both of HSI and MOSC should be alive, otherwise the chip will do malfunction.

4.6.19 SCU_CMR Clock Monitoring Register

The clock can be monitored by LSI for security purpose.

SCU_CMR=0x4000_0048

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																MCLKREC	Reserved			SOSCMNT	SOSCIE	SOSCFAIL	SOSCSTS	MCLKMNT	MCLKIE	MCLKFAIL	MCLKSTS	MOSCMNT	MOSCIE	MOSCFAIL	MOSCSTS
-																0	-			0	0	0	0	1	0	0	1	0	0	0	0
-																RW	-			RW	RW	RC	RO	RW	RW	RC	RO	RW	RW	RC	RO

Bits	Name	Function
15	MCLKREC	MCLK fail auto recovery
	0	MCLK is changed to LSI by default when MCLKFAIL issued
	1	MCLK auto recovery is disabled
11	SOSCMNT	External sub oscillator monitoring enable
	0	External sub oscillator monitoring disabled
	1	External sub oscillator monitoring enabled
10	SOSCIE	External sub oscillator fail interrupt enable
	0	External sub oscillator fail interrupt disabled
	1	External sub oscillator fail interrupt enabled
9	SOSCFAIL	External sub oscillator fail interrupt
	0	External sub oscillator fail interrupt not occurred
	1	Read : External sub oscillator fail interrupt is pending Write : Clear pending interrupt
8	SOSCSTS	External sub oscillator status
	0	Not oscillate
	1	External sub oscillator is working normally
		NOTE) This bit operates only when SOSCMNT is enabled.
7	MCLKMNT	MCLK monitoring enable
	0	MCLK monitoring disabled
	1	MCLK monitoring enabled
6	MCLKIE	MCLK fail interrupt enable
	0	MCLK fail interrupt disabled
	1	MCLK fail interrupt enabled
5	MCLKFAIL	MCLK fail interrupt
	0	MCLK fail interrupt not occurred
	1	Read : MCLK fail interrupt is pending Write : Clear pending interrupt
4	MCLKSTS	MCLK clock status
	0	No clock is present on MCLK
	1	Clock is present on MCLK
		NOTE) This bit operates only when MCLKMNT is enabled.
3	MOSCMNT	External main oscillator monitoring enable
	0	External main oscillator monitoring disabled
	1	External main oscillator monitoring enabled
2	MOSCIE	External main oscillator fail interrupt enable
	0	External main oscillator fail interrupt disabled
	1	External main oscillator fail interrupt enabled
1	MOSCFAIL	External main oscillator fail interrupt
	0	External main oscillator fail interrupt not occurred
	1	Read : External main oscillator fail interrupt is pending Write : Clear pending interrupt
0	MOSCSTS	External main oscillator status
	0	Not oscillate
	1	External main oscillator is working normally

4.6.20 SCU_NMIR NMI Control Register

SCU_NMIR is the non-maskable interrupt configuration register which can be set by software. There are three kinds of interrupt sources from WDT and SCU. It will jump to NMI handler if Selected NMI event occurred and it must check event status. For clearing occurred status, it should clear the interrupt flags of that peripheral occurred.

Write access key is required 0xA32C on SCU_NMIR[31:16] when write register.

SCU_NMIR=0x4000_004C

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ACCESSCODE																Reserved					WDTINTSTS	MCLKFAILSTS	LVDSTS	Reserved					WDTINTEN	MCLKFAILEN	LVDEN
-																-					0	0	0	-					0	0	0
WO																-					RO	RO	RO	-					RW	RW	RW

31 16	ACCESSCODE	This field enables writing access to this register. Writing 0xA32C is to enable writing.
10	WDTINTSTS	WDT Interrupt condition status bit This bit can't invoke NMI interrupt without enable bit
		0 Not occurred
		1 Event occurred
9	MCLKFAILSTS	MCLK Fail condition status bit This bit can't invoke NMI interrupt without enable bit
		0 Not occurred
		1 Event occurred
8	LVDSTS	LVD condition status bit This bit can't invoke NMI interrupt without enable bit
		0 Not occurred
		1 Event occurred
2	WDTINTEN	WDT Interrupt condition enable for NMI interrupt
		0 Disable
		1 Enable
1	MCLKFAILEN	MCLK Fail condition enable for NMI interrupt
		0 Disable
		1 Enable
0	LVDEN	LVD Fail condition enable for NMI interrupt
		0 Disable
		1 Enable

4.6.21 SCU_COR Clock Output Register

The A31G31x can drive the clock from internal MCLK clock with dedicated post divider. To use CLKO output function, it should be set as CLKO that has output mode in PF4 Pin-Mux. Clock Output Register is 8-bit register.

SCU_COR=0x4000_0050

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																											CLKOEN	CLKODIV				
-																											0	1111			
-																											RW	RW			

4	CLKOEN	Clock output enable
		0 CLKO is disabled and stay “L” output
		1 CLKO Is enabled
3 0	CLKODIV	Clock output divider value CLKO = MCLK (CLKODIV = 0) $\mathrm{CLKO} = \frac{MCLK}{2 * (\mathrm{CLKODIV} + 1)} \quad (CLKODIV > 0)$

4.6.22 SCU_PLLCON PLL Control Register

Integrated PLL will synthesize high speed clock for extremely high performance of the CPU. The PLL controlled by register SCU_PLLCON setting.

PLL Control Register is 32-bit register.

SCU_PLLCON=0x4000_0060

31	30 29 28 27 26 25 24	23	22	21	20	19	18 17 16	15 14 13 12 11 10 9 8	7 6 5 4	3 2 1 0
LOCKSTS	Reserved	PLLRSTB	PLLEN	BYPASSB	PLLMODE	Reserved	PREDIV	POSTRIV1	POSTDIV2	OUTDIV
0	-	0	0	0	0	-	000	0000_0000	0000	0000
RO	-	RW	RW	RW	RW	-	RW	RW	RW	RW

31	LOCK	LOCK status
		0 PLL is not locked
		1 PLL is locked
23	PLLRSTB	PLL reset
		0 PLL reset is asserted
		1 PLL reset is negated
22	PLLEN	PLL enable
		0 PLL is disabled
		1 PLL is enabled
21	BYPASSB	FIN bypass
		0 FOUT is bypassed as FIN
		1 FOUT is PLL output
20	PLLMODE	PLL VCO mode
		0 VCO is the same with FOUT
		1 VCO frequency is x2 of FOUT
18 16	PREDIV	FIN predivider I
		0~7 FIN divided by (PREDIV + 1), (FIN/1 ~ FIN/8)
15 8	POSTDIV1	Feedback control 1 (N1)
		0x00 N1 = 0 (N1 + 1)
		0xFF N1 = 255 (N1 + 1)
7 4	POSTDIV2	Feedback control 1 (N2)
		0x0 N2 = 0 (N2 + 1)
		0xF N2 = 15 (N2 + 1)
3 0	OUTDIV	output divider control (P)
		0x0 P = 0 (P+1)
		0xF P = 15 (P+1)

$$F_{out} = \frac{F_{IN} * (N_1 + 1)}{(R + 1) * (N_2 + 1) * (P + 1)} * (D + 1)$$

Symbol	Description
R	Pre Divider Counter Value
N_1	Post Divider1 Counter Value
N_2	Post Divider2 Counter Value
P	Output Divider Counter Value
D	Frequency Doubler

[Calculating the PLL output frequency value]

The PLL of the A31G31x can accurately set the output frequency, F_{OUT}, in 1MHz increments. The formula for the F_{IN} input to the F_{VCO} input of the PLL is as follows, and the input range of the F_{IN} frequency is between 1MHz and 3MHz. However, it is recommended to set the input frequency (FIN) to 2MHz as much as possible.

$$\mathrm{FIN} = \frac{\mathrm{PLLINCLK}}{(\mathrm{R}+1)}, \qquad \text{Where } 1\mathrm{MHz} \le \mathrm{FIN} \le 3\mathrm{MHz}\ (\text{Recommanded FIN} = 2\mathrm{MHz})$$

At this time, the range of F_{VCO} output frequency should be set to 200MHz or less, and the calculation formula is as follows.

$$\mathrm{F_{VCO}} = \mathrm{FIN} \times (\mathrm{N_1}+1), \quad \mathrm{VCO} \le 200\mathrm{MHz}\ if\ \mathrm{D}=0$$

PLLCON also supports the Doubler function which can double the F_{VCO} output through the bit setting of VCOMODE. When using this doubler function, the output of F_{VCOx2} should be set to 250MHz or less.

$$V_{VCOX2} = \mathrm{VCO} \times (\mathrm{D}+1), \qquad \mathrm{VCOx2} \le 250\mathrm{MHz}\ if\ \mathrm{D}=1$$

As a result, the final frequency of PLL, F_{OUT}, can be obtained from the formula below using the formula above.

$$\mathrm{F_{OUT}} = \frac{\mathrm{PLLINCLK} \times (\mathrm{N_1}+1)}{(\mathrm{R}+1) \times (\mathrm{N_2}+1) \times (\mathrm{P}+1)} \times (\mathrm{D}+1) = \frac{\mathrm{FIN} \times (\mathrm{N_1}+1)}{(\mathrm{N_2}+1) \times (\mathrm{P}+1)} \times (\mathrm{D}+1)$$

4.6.23 SCU_VDCCON VDC Control Register

SCU_VDCCON is a Onchip VDC control register. VDCWDLY value can be written with writing '1' to VDCWDLY_WEN bit simultaneously.

Each Writekey must be entered in order to set VDC33 and VDC15 related registers.

SCU_VDCCON=0x4000_0064

31 30 29 28 27 26 25 24	23 22 21 20	19	18	17	16	15	14 13 12 11 10 9	8	7 6 5 4 3 2 1 0
Reserved	VDC15 WTIDKY	VDC15_PDBGR	Reserved	VDC15_STOP	VDC15_IDLE	VDC15_LOCK	Reserved	VDCWDLY_WEN	VDCWDLY
-	0000	0	-	0	0	0	-	0	0111_1111
-	WO	RW	-	RW	RW	RW	-	WO	RW

23 20	**VDC15 WTIDKY**	**VDC15 Write Identification Key** **On writes, write 0x5 to these bits, otherwise the write is ignored.**
19	**VDC15_PDBGR**	VDC15 1.2V BGR / 1.0V Buffer Power Down Signal *In BGR on → off, VDCLOCK_I should be 0
		0 BGR/Buffer ON (RUN/IDLE/STOP1)
		1 BGR/Buffer OFF (STOP2)
17	**VDC15_STOP**	VDC15 STOP Mode Control Signal
		0 STOP1 Mode
		1 STOP2 Mode
16	**VDC15_IDLE**	VDC15 IDLE Mode Control Signal
		0 no IDLE Mode (RUN or STOP1 or STOP2 Mode)
		1 IDLE Mode
15	**VDC15_LOCK**	VDC15 VDCLOCK Control Signal for *BGR Stabilization *In BGR off → on Sequence, VDCLOCK_I should be 0 during 120usec
		0 VDC Using BGR Reference Voltage
		1 VDC Using BMR Reference Voltage
8	**VDCWDLY_WEN**	**VDCWDLY value write enable. VDCWDLY value can be written with writing '1' to VDCWDLY_WEN bit simultaneously.**
7 0	**VDCWDLY**	**VDC warm-up delay count value.** **When SCU is waked up from powerdown mode, the warm-up delay is inserted for VDC output being stabilized.** **The amount of delay can be defined with this register value 7F : 4msec**

4.6.24 SCU_LSICON Low Speed Internal OSC Control Register

SCU_LSICON controls the internal LDO and Level shifter using for LSI operation.

SCU_LSICON=0x4000_006C

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																														EN_LDO	SKIP_LS
-																														0	1
-																														RW	RW

1	EN_LDO	Internal LDO On/Off	
		0	Disable
		1	Enable
0	SKIP_LS	Internal Level Shifter control signal	
		0	Enable
		1	Disable

4.6.25 SCU_EOSCR External Oscillator Control Register

External main crystal oscillator has two characteristics. For the noise immunity, NMOS amplifier type is recommended and for the low power characteristic, INV amplifier type is recommended.

SCU_EOSCR=0x4000_0080

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15	14	13 12	11 10 9	8	7	6	5 4	3 2	1	0
Reserved		ESEN	Reserved	ESISEL	Reserved	ESNCBYPS	EMEN	Reserved	ISEL	NCOPT	Reserved	NCSKIP
-		0	-	01	-	0	0	-	01	01	-	0
-		WO	-	RW	-	RW	WO	-	RW	RW	-	RW

15	ESEN	Write enable for External SOSC
		0 Write access disabled
		1 Write access enabled
13 12	ESISEL	Select current for External SOSC
		00 1.57uA
		01 1.79uA
		10 1.93uA
		11 2.04uA
8	ESNCBYPS	Noise Cancel Bypass enable for External SOSC
		0 Disable
		1 Enable (Noise Cancel bypassed)
7	EMEN	Write enable for External MOSC
		0 Write access disabled
		1 Write access enabled
5 4	ISE	Select current for External MOSC
		00 12MHz < MOSC ≤ 16MHz
		01 8MHz < MOSC ≤ 12MHz
		10 4MHz < MOSC ≤ 8MHz
		11 1MHz < MOSC ≤ 4MHz
3 2	NCOPT	Noise Cancel delay Option for External MOSC
		00 23ns (1MHz < MOSC ≤ 4MHz)
		01 18ns (4MHz < MOSC ≤ 8MHz)
		10 13ns (8MHz < MOSC ≤ 12MHz)
		11 11ns (12MHz < MOSC ≤ 16MHz)
0	NCSKIP	Noise Cancel SKIP enable for External MOSC
		0 Disable
		1 Enable (Noise Cancel skipped)

4.6.26 SCU_EMODR External Mode Status Register

SCU_EMODR shows external mode pin status while booting.

This register is 8-bit register.

SCU_EMODR=0x4000_0084

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																															BOOT
-																															-
-																															RO-

0	BOOT	BOOT pin level	
		0	BOOT (PB3) pin is low
		1	BOOT (PB3) pin is high

4.6.27 SCU_RSTDBCR Pin Reset Debounce Control Register

Pin Reset Debounce Control Register.

SCU_RSTDBCR=0x4000_0088

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
WTIDKY																Reserved		CLKCNT						Reserved							EN
0x0000																-		00_0000						-							0
WO																-		RW						-							RW

31	WTIDKY	Write Identification Key
16		On writes, write 0x0514 to these bits, otherwise the write is ignored.
13	CLKCNT	Noise Cancel delay Option for External MOSC
8		N N clock checking for debounce by LSI (500kHz)
0	EN	Pin reset debounce enable bit
		0 Disable
		1 Enable

NOTE)

1. If user want to oprate pin reset debounce, user must enable LSI (500kHz). Because pin reset debounce use LSI for clock source.

4.6.28 SCU_MCCR1 Miscellaneous Clock Control Register 1

The A31G31x can drive the clock from internal MCLK clock with dedicated post divider. STCSEL and STCDIV bits of SCU_MCCR1 are used as SYSTICK external clock source. TEXT1CSEL and TEXT1DIV bits of SCU_MCCR1 are used as TIMER1n external clock source. This register is 32-bit register.

SCU_MCCR1=0x4000_0090

31 30 29 28 27	26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11	10 9 8	7 6 5 4 3 2 1 0
Reserved	TEXT1CSEL	TEXT1DIV	Reserved	STCSEL	SYSTICKDIV
-	000	0000_0000	-	000	0000_0000
-	RW	RW	-	RW	RW

26 24	TEXT1CSEL	TIMER1n EXT Clock source select bit 0xx LSI 500kHz 011 SOSC (32kHz) 100 MCLK (bus clock) 101 HSI 48MHz 110 MOSC 111 PLL Clock
23 16	TEXT1DIV	TIMER1n EXT Clock N divider 8'h0 disabled 8'hN (selected clock) / N To change the value, set 0x0 first without changing TEXT1CSEL Note) Clock is not activated during TEXT1DIV bit is disabled.
10 8	STCSEL	SYSTIC Clock source select bit 0xx LSI 500kHz 011 SOSC (32kHz) 100 MCLK (bus clock) 101 HSI 48MHz 110 MOSC 111 PLL Clock
7 0	STDIV	SYSTICK Clock N divider 8'h0 disabled 8'hN (selected clock) / N To change the value, set 0x0 first without changing STCSEL Note) Clock is not activated during STDIV bit is disabled.

4.6.29 SCU_MCCR2 Miscellaneous Clock Control Register 2

The A31G31x can drive the clock from internal MCLK clock with dedicated post divider. TEXT2CSEL and TEXT2DIV bits of SCU_MCCR2 are used as TIMER20 external clock source. TEXT3CSEL and TEXT3DIV bits of SCU_MCCR2 are used as TIMER30 external clock source. This register is 32-bit register.

SCU_MCCR2=0x4000_0094

31 30 29 28 27	26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11	10 9 8	7 6 5 4 3 2 1 0
Reserved	TEXT3CSEL	TEXT3DIV	Reserved	TEXT2CSEL	TEXT2DIV
-	000	0000_0000	-	000	0000_0000
-	RW	RW	-	RW	RW

26 24	TEXT3CSEL	TIMER 30 EXT Clock source select bit 0xx LSI 500kHz 011 SOSC (32kHz) 100 MCLK (bus clock) 101 HSI 48MHz 110 MOSC 111 PLL Clock
23 16	TEXT3DIV	TIMER 30 EXT Clock N divider 8'h0 disabled 8'hN (selected clock) / N To change the value, set 0x0 first without changing TEXT3DIV Note) Clock is not activated during TEXT3DIV bit is disabled.
10 8	TEXT2CSEL	TIMER 20 EXT Clock source select bit 0xx LSI 500kHz 011 SOSC (32kHz) 100 MCLK (bus clock) 101 HSI 48MHz 110 MOSC 111 PLL Clock
7 0	TEXT2DIV	TIMER 20 EXT Clock N divider 8'h0 disabled 8'hN (selected clock) / N To change the value, set 0x0 first without changing TEXT2CSEL Note) Clock is not activated during TEXT2DIV bit is disabled.

4.6.30 SCU_MCCR3 Miscellaneous Clock Control Register 3

The A31G31x can drive the clock from internal MCLK clock with dedicated post divider. WDTCSEL and WDTDIV bits of SCU_MCCR3 are used as WDT external clock source. WTEXTCSEL and WTEXTCDIV bits of SCU_MCCR3 are used as WT external clock source. This register is 32-bit register.

SCU_MCCR3=0x4000_0098

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved					WTEXTCSEL			WTEXTCDIV								Reserved					WDTCSEL			WDTDIV							
-					000											-					000			0000_0000							
-					RW			RW								-					RW			RW							

26 24	WTEXTCSEL	WT External Clock source select bit 0xx LSI 500kHz 011 SOSC (32kHz) 100 MCLK (bus clock) 101 HSI 48MHz 110 MOSC 111 PLL Clock
23 16	WTEXTCDIV	WT External Clock N divider 8'h0 disabled 8'hN (selected clock) / N To change the value, set 0x0 first without changing WTEXTCSEL Note) Clock is not activated during WTEXTCDIV bit is disabled.
10 8	WDTCSEL	WDT Clock source select bit 0xx LSI 500kHz 011 SOSC (32kHz) 100 MCLK (bus clock) 101 HSI 48MHz 110 MOSC 111 PLL Clock
7 0	WDTDIV	WDT Clock N divider 8'h0 disabled 8'hN (selected clock) / N To change the value, set 0x0 first without changing WDTCSEL Note) Clock is not activated during WDTDIV bit is disabled.

4.6.31 SCU_MCCR4 Miscellaneous Clock Control Register 4

The A31G31x can drive the clock from internal MCLK clock with dedicated post divider. PD0CSEL and PD0DIV bits of SCU_MCCR4 are used as PA, PB and PC Debounce Clock source. PD1CSEL and PD1DIV bits of SCU_MCCR4 are used as PD, PE and PF Debounce Clock source. This register is 32-bit register.

SCU_MCCR4=0x4000_009C

31 30 29 28 27	26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11	10 9 8	7 6 5 4 3 2 1 0
Reserved	PD1CSEL	PD1DIV	Reserved	PD0CSEL	PD0DIV
-	000	0000_0000	-	000	0000_0000
-	RW	RW	-	RW	RW

26 24	PD1CSEL	Debounce Clock for PORT source select bit (PD,PE,PF) 0xx LSI 500kHz 011 SOSC (32kHz) 100 MCLK (bus clock) 101 HSI 48MHz 110 MOSC 111 PLL Clock
23 16	PD1DIV	PORT Debounce Clock N divider (PD,PE,PF) 8'h0 Disabled 8'hN (selected clock) / N To change the value, set 0x0 first without changing PD1CSEL Note) Clock is not activated during PD1DIV bit is disabled.
10 8	PD0CSEL	Debounce Clock for PORT source select bit (PA,PB,PC) 0xx LSI 500kHz 011 SOSC (32kHz) 100 MCLK (bus clock) 101 HSI 48MHz 110 MOSC 111 PLL Clock
7 0	PD0DIV	PORT Debounce Clock N divider (PA,PB,PC) 8'h0 Disabled 8'hN (selected clock) / N To change the value, set 0x0 first without changing PD0CSEL Note) Clock is not activated during PD0DIV bit is disabled.

4.6.32 SCU_MCCR5 Miscellaneous Clock Control Register 5

The A31G31x can drive the clock from internal MCLK clock with dedicated post divider. LEDCSEL and LEDDIV bits of SCU_MCCR5 are used as LED Clock source. LCDCSEL and LCDDIV bits of SCU_MCCR5 are used as LCD Clock source. This register is 32-bit register.

SCU_MCCR5=0x4000_00A0

31 30 29 28 27	26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11	10 9 8	7 6 5 4 3 2 1 0
Reserved	LCDCSEL	LCDDIV	Reserved	LEDCSEL	LEDDIV
-	000	0000_0000	-	000	0000_0000
-	RW	RW	-	RW	RW

26 24	LCDCSEL	LCD Clock source select bit 0xx LSI 500kHz 011 SOSC (32kHz) 100 MCLK (bus clock) – not valid for LCD 101 HSI 48MHz – not valid for LCD 110 MOSC – not valid for LCD 111 PLL Clock – not valid for LCD
23 16	LCDDIV	LCD Clock N divider 8'h0 Disabled 8'hN (selected clock) / N To change the value, set 0x0 first without changing LCDCSEL Note) Clock is not activated during LCDDIV bit is disabled.
10 8	LEDCSEL	LED Clock source select bit 0xx LSI 500khz 011 SOSC (32kHz) 100 MCLK (bus clock) 101 HSI 48MHz 110 MOSC 111 PLL Clock
7 0	LEDDIV	LED Clock N divider 8'h0 Disabled 8'hN (selected clock) / N To change the value, set 0x0 first without changing LEDCSEL Note) Clock is not activated during LEDDIV bit is disabled.

4.6.33 SCULV_LVICR Low Voltage Indicator Control Register

Low Voltage Indicator Control Register is 32-bit register which is 32/16/8-bit accessible.

LVICR=0x4000_5100

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																								LVIEN	Reserved	LVINTEN	LVIFLAG	LVIVS			
-																								0	-	0	0	0000			
-																								RW	-	RW	RW	RW			

7	LVIEN	LVI Enable bit.	
		0	Disable low voltage indicator.
		1	Enable low voltage indicator.
5	LVINTEN	LVI Interrupt Enable bit.	
		0	Disable low voltage indicator interrupt.
		1	Enable low voltage indicator interrupt.
4	LVIFLAG	LVI Interrupt Flag bit.	
		0	No request occurred.
		1	Request occurred, This bit is cleared to '0' when write '1'.
3	LVIVS	LVI Voltage Selection bits.	
0		0000	1.60V
		0001	1.69V
		0010	1.78V
		0011	1.90V
		0100	1.99V
		0101	2.12V
		0110	2.30V
		0111	2.47V
		1000	2.67V
		1001	3.04V
		1010	3.18V
		1011	3.59V
		1100	3.72V
		1101	4.03V
		1110	4.20V
		1111	4.48V

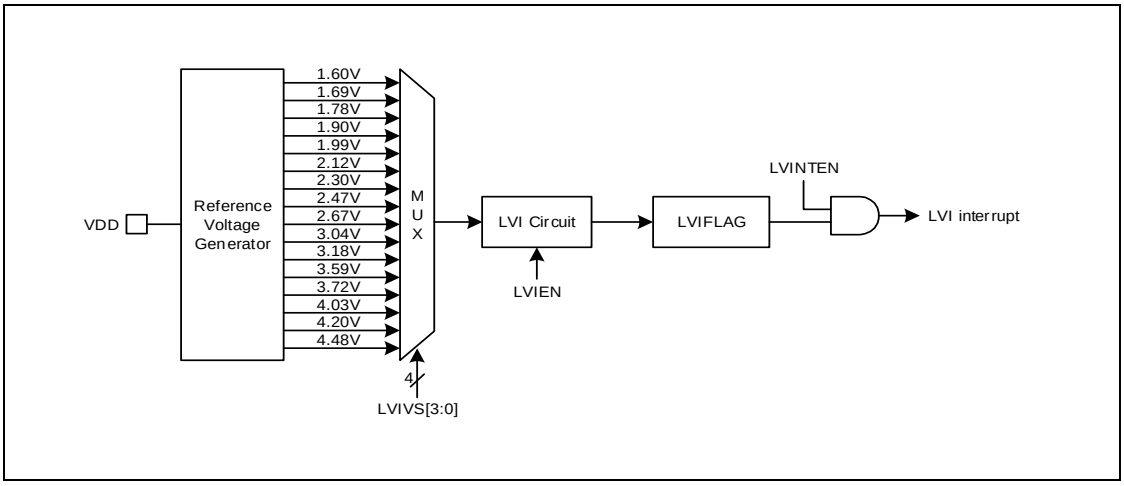


Figure 4.11 LVI Block Diagram

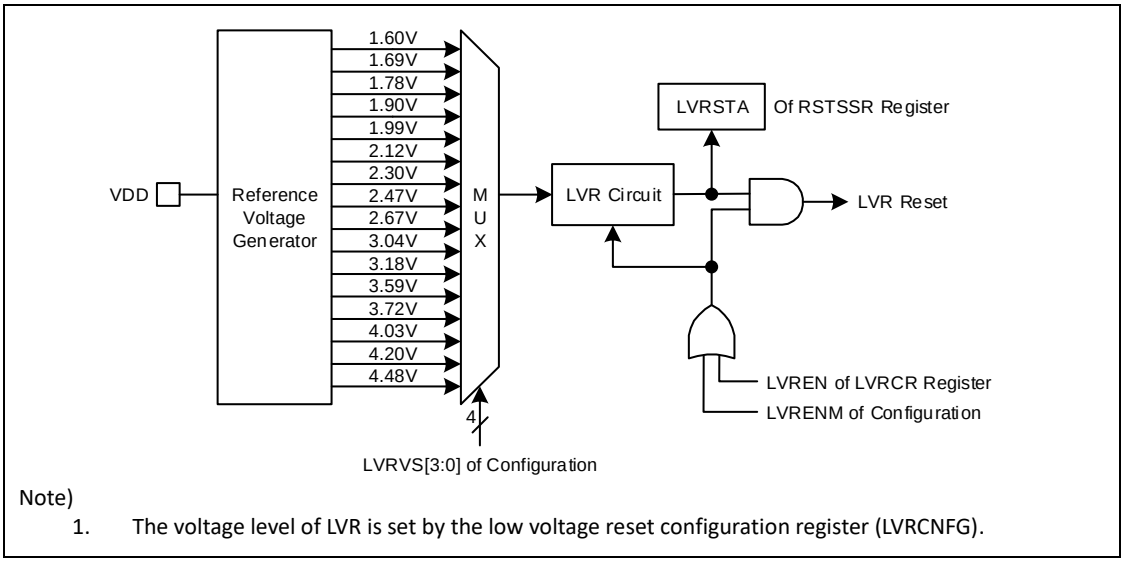
4.6.34 SCULV_LVRCR Low Voltage Reset Control Register

Low Voltage Reset Control Register is 32-bit register which is 32/16/8-bit accessible.

LVRCR=0x4000_5104

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																								LVREN							
-																								0000_0000							
-																								RW							

7	**LVREN**	**LVR Enable bits. These bits are cleared to 0x00 by only POR and retained by other reset signals.**	
0		**0x55**	**Disable low voltage reset.**
		Others	**Enable low voltage reset.**



Note)

1. The voltage level of LVR is set by the low voltage reset configuration register (LVRCNFG).

Figure 4.12 LVR Block Diagram

4.6.35 LVRCNFIG Configuration for Low Voltage Reset

Low Voltage Indicator Control Register is a 32-bit register which is 32/16/8-bit accessible.

LVRCNFIG=0x4000_5108

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4	3 2 1 0
WTIDKY		LVRENM	Reserved	LVRVS
0x0000		0000_0000	-	1111
WO		RW	-	RW

31	WTIDKY	Write Identification Key	
24		On writes, write 0x72A5 to these bits, otherwise the write is ignored.	
15	LVRENM	LVR Reset Operation Control Master Configuration	
8		0xAA	LVR operation is decided by the LVREN of LVRCR register
		Ohters	Master enable LVR operation
3	LVRVS	LVR Voltage Selection bits.	
0		1111	1.60V
		1110	1.69V
		1101	1.78V
		1100	1.90V
		1011	1.99V
		1010	2.12V
		1001	2.30V
		1000	2.47V
		0111	2.67V
		0110	3.04V
		0101	3.18V
		0100	3.59V
		0011	3.72V
		0010	4.03V
		0001	4.20V
		0000	4.48V

CHAPTER 5. PORT CONTROL UNIT (PCU) & GPIO

5.1 OVERVIEW

PCU(Port Control Unit) controls the external I/Os as below

- Set external signal directions of each pins
- Set interrupt trigger mode for each pins
- Set internal pull-up/down register control and open drain control

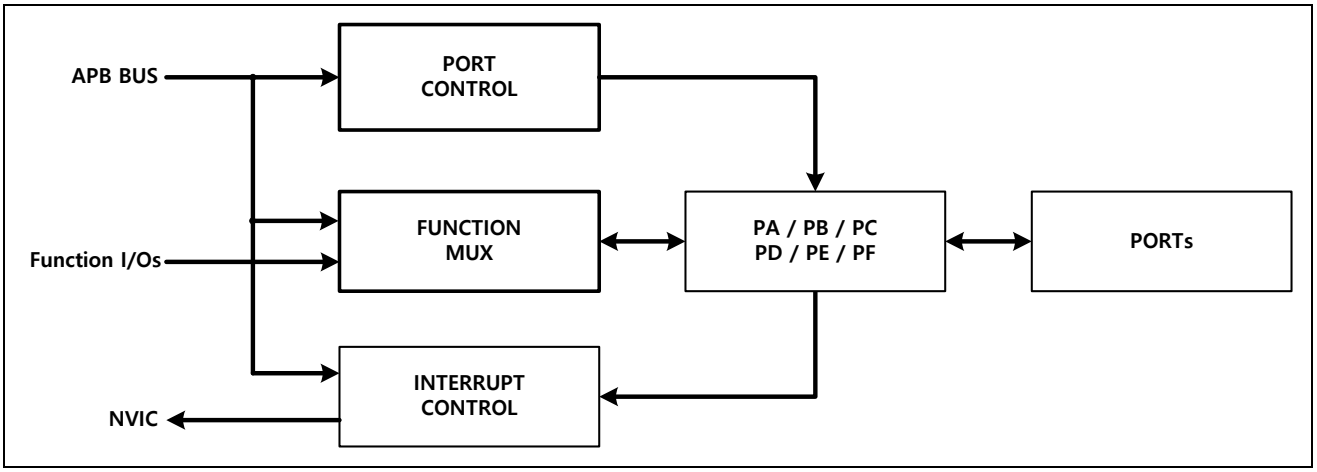


Figure 5.1 Port Control Uint Block Diagram m

Most of pins except dedicated function pins can be used general I/O ports. General input/output ports are controlled by GPIO block.

- Output signal level (H/L) select
- External interrupt interface
- Pull up/down enable or disable

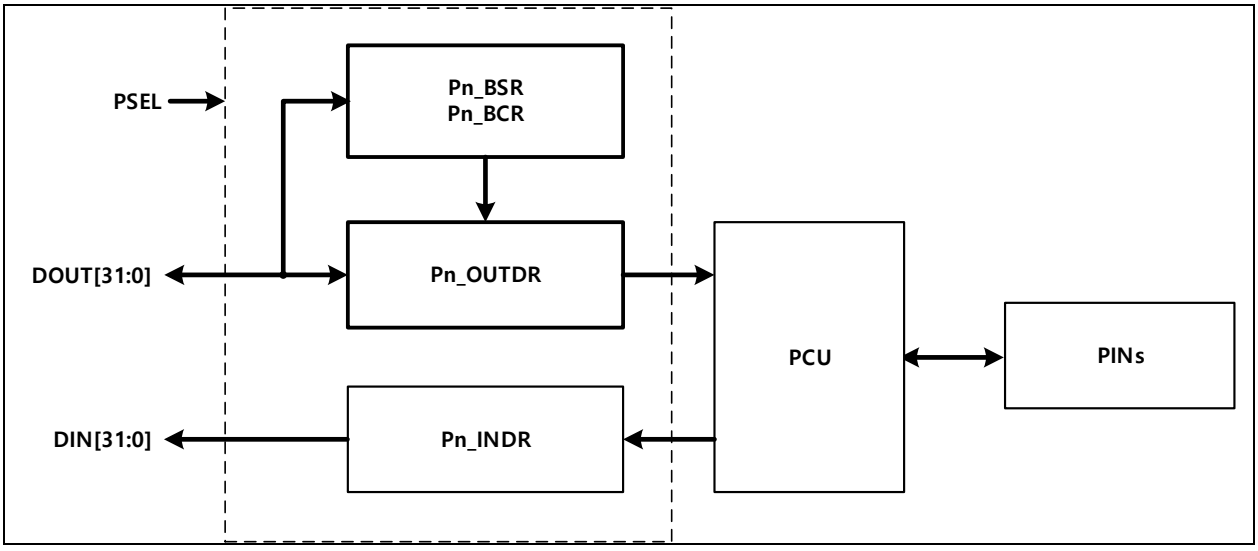


Figure 5.2 GPIO Block diagram

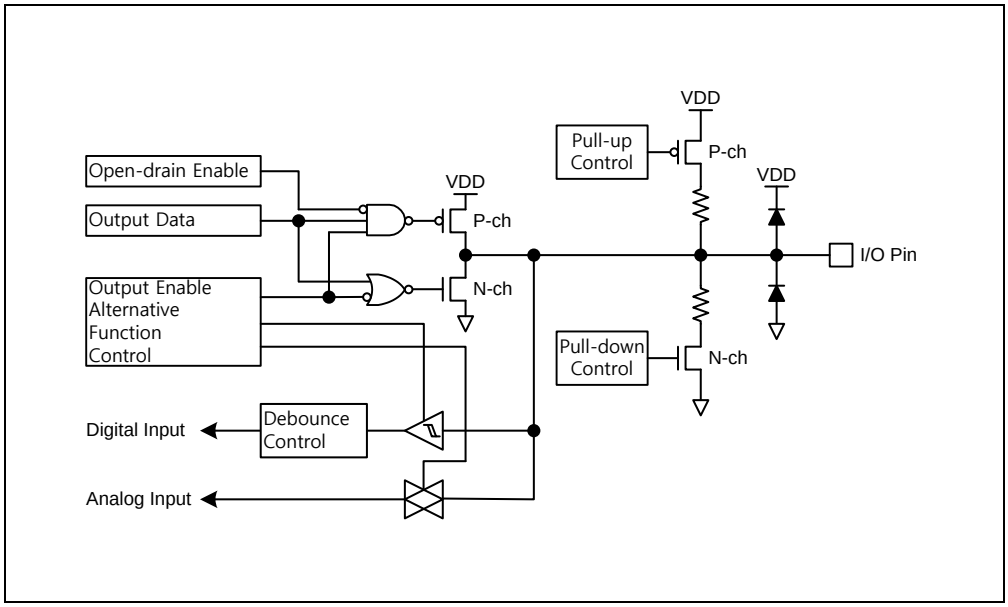


Figure 5.3 I/O Port Block Diagram (External Interrupt I/O pins)

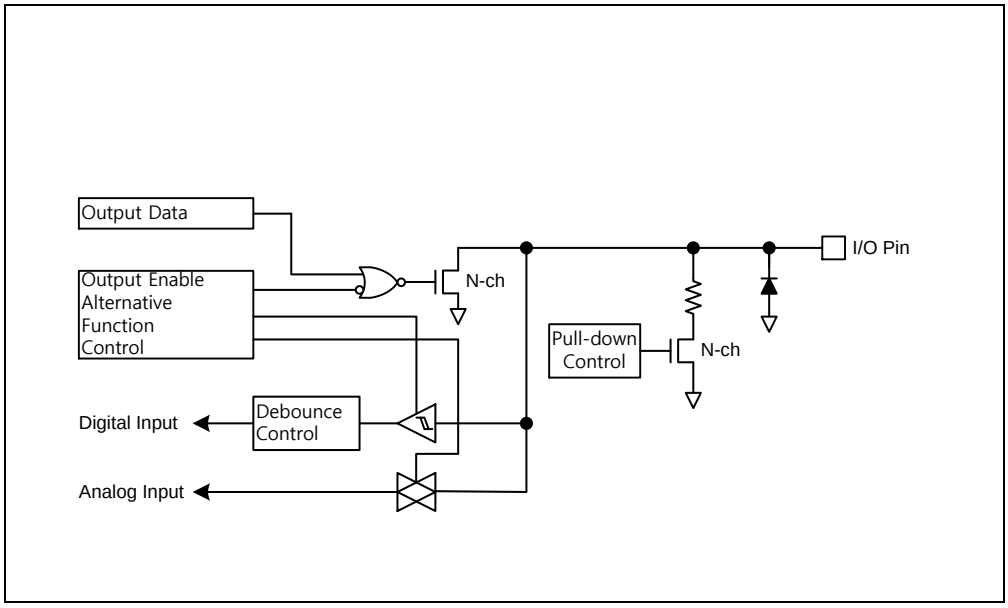


Figure 5.4 I/O Port Block Diagram (PF5, PF6, PF7 I/O pins)

5.2 Pin Multiplexing

GPIO pins have alternative function pins. Below table shows pin multiplexing information.

Table 5.1 GPIO Alternative function

Pin Names	Alternative Functions				
	AF0	AF1	AF2	AF3	AF4
PA0		SDA1		AN0	CS3/ISEG9
PA1		SCL1		AN1	CS4/ISEG8
PA2		EC12		AN2/AVREF/CP0	CS5/ISEG7
PA3				AN3/CP1C	CS6/ISEG6
PA4				AN4/CP1B	CS7/ISEG5
PA5		T12O	T12C	AN5/CP1A	ISEG4
PA6	SEG43			AN6/CREF1 /DAO	ISEG3
PA7	SEG42			AN7/CREF0 /DAVREF	ISEG2
-					
PA9				AN12	CS0
PA10				AN13	CS1
PA11				AN14	CS2
PB0	SEG41	TXD10	MOSI10	AN8	CS8/ICOM26 /ISEG1
PB1	SEG40	RXD10	MISO10	AN9	CS9/ICOM25 /ISEG0
PB2	SEG39		SCK10	AN10	CS10/ICOM24
PB3	SEG38	BOOT	SS10		ICOM23
PB4	SEG37	TXD0	SWCLK		ICOM22
PB5	SEG36	RXD0	SWDIO		ICOM21
PB6	SEG35	TXD1			ICOM20
PB7	SEG34	RXD1			ICOM19
PB8	SEG33	T15O	T15C	EC16	CS11/EC16
PB9	SEG32	T16O	T16C	EC15	CS12/EC15
PB10	SEG31	T16C	EC15	T16O	CS13/T16O
PB11	SEG30	T15C	EC16	T15O	CS14/T15O
PB12	SEG29				CS15
PB13	SEG28				CS16
PB14	SEG27				CS17
PB15	SEG26				CS18

Table 5.2 GPIO Alternative function

Pin Names	Alternative Functions				
	AF0	AF1	AF2	AF3	AF4
PC0	SEG25	T20O	T20C		CS19/ICOM18
PC1	SEG24	T21O	T21C		CS20/ICOM17
PC2	SEG23	EC20			CS21/ICOM16
PC3	SEG22	EC21			CS22/ICOM15
PC4	SEG21				CS23/ICOM14
PC5	SEG20	SDA2			
PC6	SEG19	SCL2			
PC7	SEG18				
PC8	SEG17				
PC9	SEG16				
PC10	SEG15				
PC11	SEG14	EC10			
PC12	SEG13	EC11			
PD0	SEG12	SCL0			ICOM13
PD1	SEG11	SDA0			ICOM12
PD2	SEG10	TXD11	MOSI11		ICOM11
PD3	SEG9	RXD11	MISO11		ICOM10
PD4	SEG8		SCK11		ICOM9
PD5	SEG7		SS11		ICOM8

Table5.3 GPIO Alternative function

Pin Names	Alternative Functions				
	AF0	AF1	AF2	AF3	AF4
PE0	COM0	PWM30AA			ICOM0
PE1	COM1	PWM30AB			ICOM1
PE2	COM2	PWM30BA			ICOM2
PE3	COM3/SEG0	PWM30BB			ICOM3
PE4	COM4/SEG1	PWM30CA			ICOM4
PE5	COM5/SEG2	PWM30CB			ICOM5
PE6	COM6/SEG3	T10O	T10C		ICOM6
PE7	COM7/SEG4	T11O	T11C		ICOM7
PE8		TXD13	MOSI13	VLC0	
PE9		RXD13	MISO13	VLC1	
PE10			SCK13	VLC2	
PE11			SS13	VLC3	
PE12		TXD12	MOSI12		
PE13		RXD12	MISO12		
PE14	SEG5		SCK12		
PE15	SEG6		SS12		
PF0		SCL1		XOUT	ISEG10
PF1		SDA1		XIN	
PF2		TXD1		SXIN	
PF3		RXD1		SXOUT	
PF4		CLKO		R-SET	
PF5		BLNK			
PF6		EC30	SCL0		
PF7		T30C	SDA0		
PF8		EC13			
PF9		EC14			
PF10		T13O	T13C		
PF11		T14O	T14C		

Notes)

1. On connection with debugger host, The SWCLK and SWDIO pins are always for SW-DP pins. So, the corresponding bits of PB_MOD/PB_TYP/PB_AFSR1/PB_PUPD registers may not be written by software.

5.3 PIN DESCRIPTION

Table 5.4 External signal

PIN NAME	TYPE	DESCRIPTION
PA	IO	PA0 – PA7, PA9 – PA11
PB	IO	PB0 – PB15
PC	IO	PC0 – PC12
PD	IO	PD0 – PD5
PE	IO	PE0 – PE15
PF	IO	PF0 – PF10

5.4 REGISTERS

Base addresse of Port Register is as below.

Table 5.5 Base address of port control

NAME	BASE ADDRESS	DESCRIPTION
PA	0x4000_1000	General Port A
PB	0x4000_1100	General Port B
PC	0x4000_1200	General Port C
PD	0x4000_1300	General Port D
PE	0x4000_1400	General Port E
PF	0x4000_1500	General Port F

Table 5.6 Port Register map

Register Name	Offset	Access Type	Description	Initial Value	Ref
Pn_MOD	0x00	RW	Port n Mode Register	PA:0x00FF_FFFF PB:0xFFFF_FAB3 PC:0x03FF_FFC3 PD:0x0000_0FFF PE:0xFFFF_FFFF PF:0x00FF_FFFF	5.4.1
Pn_TYP	0x04	RW	Port n Output Type Selection Register	0x0000_0000	5.4.2
Pn_AFSR1	0x08	RW	Port n Alternative Function Selection Register 1	Pn:0x0000_0000 PB:0x0022_1000	5.4.3
Pn_AFSR2	0x0C	RW	Port n Alternative Function Selection Register 2	0x0000_0000	5.4.4
Pn_PUPD	0x10	RW	Port n Pull-up/down Resistor Selection Register	Pn:0x0000_0000 PB:0x0000_0540 PC:0x0000_0014	5.4.5
Pn_INDR	0x14	RO	Port n Input Data Register	0x0000_XXXX	5.4.6
Pn_OUTDR	0x18	RW	Port n Output Data Register	0x0000_0000	5.4.7
Pn_BSR	0x1C	WO	Port n Output Bit Set Register	0x0000_0000	5.4.8
Pn_BCR	0x20	WO	Port n Output Bit Clear Register	0x0000_0000	5.4.9
Pn_OUTDMSK	0x24	RW	Port n Output Data Mask Register	0x0000_0000	5.4.10
Pn_DBCR	0x28	RW	Port n Debounce Control Register	0x0000_0000	5.4.11
Pn_IER	0x2C	RW	Port n interrupt enable register	0x0000_0000	5.4.12
Pn_ISR	0x30	RW	Port n interrupt status register	0x0000_0000	5.4.13
Pn_ICR	0x34	RW	Port n interrupt control register	0x0000_0000	5.4.14
PF_PLSR	0x38	RW	Port F level select register	0x0000_0000	5.4.15

Note: Where n = A, B, C, D, E, and F.

Base addresse of Port Control Unit is as below.

Table 5.7 Base address of port control

NAME	BASE ADDRESS	DESCRIPTION
PCU	0x4000_1540	Port Control Unit

Table 5.8 PCU Register map

Register Name	Address	Access Type	Description	Initial Value	Ref
PCU_PORTEN	0x4000_0FF0	WO	Port Access Enable	0x0000_0000	5.4.17

5.4.1 Pn_MOD PORT n Mode Register

Input or output control of each port pin. Each pin can be configured as input pin, output pin or alternative function pin.
Pn_MOD Register is 32-bit register which is 32/16/8-bit accessible. (n = A to F)

PA_MOD=0x4000_1000, PB_MOD=0x4000_1100, PC_MOD=0x4000_1200
PD_MOD=0x4000_1300, PE_MOD=0x4000_1400, PF_MOD=0x4000_1500

-	31 30	29 28	27 26	25 24	23 22	21 20	19 18	17 16	15 14	13 12	11 10	9 8	7 6	5 4	3 2	1 0
	MODE15	MODE14	MODE13	MODE12	MODE11	MODE10	MODE9	MODE8	MODE7	MODE6	MODE5	MODE4	MODE3	MODE2	MODE1	MODE0
PA	00	00	00	00	11	11	11	11	11	11	11	11	11	11	11	11
PB	11	11	11	11	11	11	11	11	11	11	10	10	10	11	00	11
PC	00	00	00	11	11	11	11	11	11	11	11	11	11	00	00	11
PD	00	00	00	00	00	00	00	00	00	00	11	11	11	11	11	11
PE	11	11	11	11	11	11	11	11	11	11	11	11	11	11	11	11
PF	00	00	00	00	11	11	11	11	11	11	11	11	11	11	11	11
	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Bits	Name	Function	
2x+1	MODEx	Port n Mode Selection bits, x:0 to 15	
2x		00	Input mode
		01	Output mode
		10	Alternative function mode
		11	Reserved

5.4.2 Pn_TYP PORT n Output Type Selection Register

Push-pull or Open-drain output control of each port pin.

Port n Mode Register is 32-bit register. This Register is able to 32/16/8-bit access. (n = A to F)

PA_TYP=0x4000_1004, PB_TYP=0x4000_1104, PC_TYP=0x4000_1204
PD_TYP=0x4000_1304, PE_TYP=0x4000_1404, PF_TYP=0x4000_1504

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																TYP15	TYP14	TYP13	TYP12	TYP11	TYP10	TYP9	TYP8	TYP7	TYP6	TYP5	TYP4	TYP3	TYP2	TYP1	TYP0
-																0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
-																RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Bits	Name	Function
x	TYPx	Port n Output Type Selection bits, x:0 to 15
		0 Push-pull output
		1 Open-drain output

5.4.3 Pn_AFSR1 PORT n Alternative Function Selection Register 1

Pn port Alternative Function select register. This register must be set properly before use the port. Otherwise the port can't guarantee its functionality.

Port n Alternative Function Selection Register 0 is 32-bit register. This Register is able to 32/16/8-bit access.

PA_AFSR1=0x4000_1008, PB_AFSR1=0x4000_1108, PC_AFSR1=0x4000_1208
PD_AFSR1=0x4000_1308, PE_AFSR1=0x4000_1408, PF_AFSR1=0x4000_1508

	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
	AFSB7	AFSB6	AFSB5	AFSB4	AFSB3	AFSB2	AFSB1	AFSB0
Pn	0000	0000	0000	0000	0000	0000	0000	0000
PB	0000	0000	0010	0010	0001	0000	0000	0000
	RW	RW	RW	RW	RW	RW	RW	RW

Bits	Name	Function	
4x+3	AFSBx	Port n Alternative Function Selection bits, x:0 to 7	
4x		0000	Alternative Function 0 (AF0)
		0001	Alternative Function 1 (AF1)
		0010	Alternative Function 2 (AF2)
		0011	Alternative Function 3 (AF3)
		0100	Alternative Function 4 (AF4)
		Others	Reserved

5.4.4 Pn_AFSR2 PORT n Alternative Function Selection Register 2

Pn port Alternative Function select register. This register must be set properly before use the port. Otherwise the port can't guarantee its functionality.

Port n Alternative Function Selection Register 1 is 32-bit register. This Register is able to 32/16/8-bit access.

PA_AFSR2=0x4000_100C, PB_AFSR2=0x4000_110C, PC_AFSR2=0x4000_120C
PD_AFSR2=0x4000_130C, PE_AFSR2=0x4000_140C, PF_AFSR2=0x4000_150C

31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
AFSB15	AFSB14	AFSB13	AFSB12	AFSB11	AFSB10	AFSB9	AFSB8
0000	0000	0000	0000	0000	0000	0000	0000
RW	RW	RW	RW	RW	RW	RW	RW

Bits	Name	Function	
4(x-8)+3 4(x-8)	AFSRx	Port n Alternative Function Selection bits, x:8 to 15	
		0000	Alternative Function 0 (AF0)
		0001	Alternative Function 1 (AF1)
		0010	Alternative Function 2 (AF2)
		0011	Alternative Function 3 (AF3)
		0100	Alternative Function 4 (AF4)
		Others	Reserved

5.4.5 Pn_PUPD PORT n Pull-up/down Resistor Selection Register

Every pin in the port has on-chip pull-up/down resistors which can be configured by PnPUPD registers.

Port n Pull-up/down Resistor Selection Register is 32-bit register. This Register is able to 32/16/8-bit access. (n = A to F)

PA_PUPD=0x4000_1010, PB_PUPD=0x4000_1110, PC_PUPD=0x4000_1210
PD_PUPD=0x4000_1310, PE_PUPD=0x4000_1410, PF_PUPD=0x4000_1510

	31 30	29 28	27 26	25 24	23 22	21 20	19 18	17 16	15 14	13 12	11 10	9 8	7 6	5 4	3 2	1 0
	PUPD15	PUPD14	PUPD13	PUPD12	PUPD11	PUPD10	PUPD9	PUPD8	PUPD7	PUPD6	PUPD5	PUPD4	PUPD3	PUPD2	PUPD1	PUPD0
Pn	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
PB	00	00	00	00	00	00	00	00	00	00	01	01	01	00	00	00
PC	00	00	00	00	00	00	00	00	00	00	00	00	00	01	01	00
	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Bits	Name	Function	
2x+1	PUPDx	Port n Pull-up/down Resistor Selection bits, x:0 to 15	
2x		00	Disable pull-up/down resistor
		01	Enable pull-up resistor
		10	Enable pull-down resistor
		11	Reserved

5.4.6 Pn_INDR PORT n Input Data Register

Each pin level status can be read in the PnINDR register. Even if the pin is alternative mode except analog mode and output in alternative mode, the pin level can be detected in the PnINDR register.

Port n Input Data Register is 32-bit register. This Register is able to 32/16/8-bit access. (n = A to F).

PA_INDR=0x4000_1014, PB_INDR=0x4000_1114, PC_INDR=0x4000_1214
PD_INDR=0x4000_1314, PE_INDR=0x4000_1414, PF_INDR=0x4000_1514

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved		INDR15	INDR14	INDR13	INDR12	INDR11	INDR10	INDR9	INDR8	INDR7	INDR6	INDR5	INDR4	INDR3	INDR2	INDR1	INDR0
-		x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
-		RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO

Bits	Name	Function
x	INDRx	Port n Input Data bit, x:0 to 15

5.4.7 Pn_OUTDR PORT n Output Data Register

When the pin is set as output and GPIO mode, the pin output level is defined by PnOUTDR registers.

Port n Output Data Register is 32-bit register. This Register is able to 32/16/8-bit access. (n = A to F)

PA_OUTDR=0x4000_1018, PB_OUTDR=0x4000_1118, PC_OUTDR=0x4000_1218
PD_OUTDR=0x4000_1318, PE_OUTDR=0x4000_1418, PF_OUTDR=0x4000_1518

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																OUTDR15	OUTDR14	OUTDR13	OUTDR12	OUTDR11	OUTDR10	OUTDR9	OUTDR8	OUTDR7	OUTDR6	OUTDR5	OUTDR4	OUTDR3	OUTDR2	OUTDR1	OUTDR0
-																0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
-																RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Bits	Name	Function
x	OUTDRx	Port n Output Data bit, x:0 to 15 The OUTDR bits can be individually set/cleared by writing to the PnBSR/PnBCR register

5.4.8 Pn_BSR PORT n Output Bit Set Register

PnBSR is a register for control each bit of PnOUTDR register. Writing a '1' into the specific bit will set a corresponding bit of PnOUTDR to '1'. Writing '0' in this register has no effect.

Port n Output Bit Set Register is 32-bit register. This Register is able to 32/16/8-bit access. (n = A to F)

PA_BSR=0x4000_101C, PB_BSR=0x4000_111C, PC_BSR=0x4000_121C
PD_BSR=0x4000_131C, PE_BSR=0x4000_141C, PF_BSR=0x4000_151C

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																BSR15	BSR14	BSR13	BSR12	BSR11	BSR10	BSR9	BSR8	BSR7	BSR6	BSR5	BSR4	BSR3	BSR2	BSR1	BSR0
-																0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
-																WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO

Bits	Name	Function	
x	BSRx	Port n Output Set bit, x:0 to 15. These bits are always read to 0x00	
		0	No effect
		1	Set the corresponding OUTDRx bit (automatically cleared to 0)

5.4.9 Pn_BCR PORT n Output Bit Clear Register

PnBCR is a register for control each bit of PnOUTDR register. Writing a '1' into the specific bit will set a corresponding bit of PnOUTDR to '0'. Writing '0' in this register has no effect.

Port n Output Bit Clear Register is 32-bit register. This Register is able to 32/16/8-bit access. (n = A to F).

PA_BCR=0x4000_1020, PB_BCR=0x4000_1120, PC_BCR=0x4000_1220
PD_BCR=0x4000_1320, PE_BCR=0x4000_1420, PF_BCR=0x4000_1520

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																BCR15	BCR14	BCR13	BCR12	BCR11	BCR10	BCR9	BCR8	BCR7	BCR6	BCR5	BCR4	BCR3	BCR2	BCR1	BCR0
-																0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
-																WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO

Bits	Name	Function
X	BCRx	Port n Output Clear bit, x:0 to 15. These bits are always read to 0x00
		0 No effect
		1 Clear the corresponding OUTDRx bit (automatically cleared to 0)

5.4.10 Pn_OUTDMSK PORT n Output Data Mask Register

PnOUTDMSK is a register for protection each bit of PnOUTDR register. Writing a '1' into the specific bit will protect a corresponding bit of PnOUTDR. Writing '0' in this register is unmasked.

Port n Output Data Mask Register is 32-bit register. This Register is able to 32/16/8-bit access. (n = A to F)

PA_OUTDMSK=0x4000_1024, PB_OUTDMSK=0x4000_1124, PC_OUTDMSK=0x4000_1224
PD_OUTDMSK=0x4000_1324, PE_OUTDMSK=0x4000_1424, PF_OUTDMSK=0x4000_1524

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																OUTDMSK15	OUTDMSK14	OUTDMSK13	OUTDMSK12	OUTDMSK11	OUTDMSK10	OUTDMSK9	OUTDMSK8	OUTDMSK7	OUTDMSK6	OUTDMSK5	OUTDMSK4	OUTDMSK3	OUTDMSK2	OUTDMSK1	OUTDMSK0
-																0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
-																RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Bits	Name	Function
x	OUTDMSKx	Port n Output Data Mask bit, x:0 to 15.
		0 Unmask. The corresponding OUTDR bit can be changed.
		1 Mask. The corresponding OUTDRx bit is protected.

5.4.11 Pn_DBCR PORT n Debounce Control Register

Port n Debounce Control Register is 32-bit register. This Register is able to 32/16/8-bit access. (n = A to F)

PA_DBCR=0x4000_1028, PB_DBCR=0x4000_1128, PC_DBCR=0x4000_1228
PD_DBCR=0x4000_1328, PE_DBCR=0x4000_1428, PF_DBCR=0x4000_1528

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																DBEN15	DBEN14	DBEN13	DBEN12	DBEN11	DBEN10	DBEN9	DBEN8	DBEN7	DBEN6	DBEN5	DBEN4	DBEN3	DBEN2	DBEN1	DBEN0
-																0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
-																RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Bits	Name	Function	
x	DBENx	Port n Debounce Enable bit, x:0 to 15.	
		0	Disable debounce filter
		1	Enable debounce filter

Note) 1. It needs to check clock source when using the Port n Debounce Function.
The clock source is selected by SCU_MCCR4 register. (The selected clock should be enabled)
LSI, SOSC, MCLK, HSI, MOSC and PLL clock are selectable as clock source through this SCU_MCCR4 register.
2. If a level is not detected on an enabled pin three or more times in a row at the sampling clock, the signal is eliminated as noise.
3. The port debounce should be disabled before deep sleep mode. If it is not disable, wake-up is not occurred.

5.4.12 Pn_IER PORT n Interrupt Enable Register

The entire pin can be an external interrupt source. Both of edge trigger interrupt and level trigger interrupt are supported. The interrupt mode can be configured by setting Pn_IER registers

PA_IER=0x4000_102C, PB_IER=0x4000_112C, PC_IER=0x4000_122C
PD_IER=0x4000_132C, PE_IER=0x4000_142C, PF_IER=0x4000_152C

31 30	29 28	27 26	25 24	23 22	21 20	19 18	17 16	15 14	13 12	11 10	9 8	7 6	5 4	3 2	1 0
PIE15	PIE14	PIE13	PIE12	PIE11	PIE10	PIE9	PIE8	PIE7	PIE6	PIE5	PIE4	PIE3	PIE2	PIE1	PIE0
00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Bits	Name	Function
2x+1	PIEx	Port n Pin interrupt Enable Selection bits, x:0 to 15
2x		00 Disable Interrupt
		01 Enable interrupt as level trigger mode
		10 Reserved
		11 Enable interrupt as edge trigger mode

5.4.13 Pn_ISR PORT n Interrupt Status Register

When an interrupt is delivered to the CPU, the interrupt status can be detected by reading Pn_ISR register. Pn_ISR register will report a source pin of interrupt and a type of interrupt.

PA_ISR=0x4000_1030, PB_ISR=0x4000_1130, PC_ISR=0x4000_1230
PD_ISR=0x4000_1330, PE_ISR=0x4000_1430, PF_ISR=0x4000_1530

31 30	29 28	27 26	25 24	23 22	21 20	19 18	17 16	15 14	13 12	11 10	9 8	7 6	5 4	3 2	1 0
PIS15	PIS14	PIS13	PIS12	PIS11	PIS10	PIS9	PIS8	PIS7	PIS6	PIS5	PIS4	PIS3	PIS2	PIS1	PIS0
00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Bits	Name	Function
2x+1	PISx	Port n Pin interrupt Status bits, x:0 to 15
2x		00 No interrupt event
		01 Low level interrupt or Falling edge interrupt event is present.
		10 High level interrupt or Ralling edge interrupt event is present.
		11 Both of rising and falling interrupt event is present in edge trigger interrupt mode. Not available in level trigger interrupt mode.

5.4.14 Pn_ICR PORT n Interrupt Control Register

Port Pin Interrupt mode control register.

PA_ICR=0x4000_1034, PB_ICR=0x4000_1134, PC_ICR=0x4000_1234
PD_ICR=0x4000_1334, PE_ICR=0x4000_1434, PF_ICR=0x4000_1534

31 30	29 28	27 26	25 24	23 22	21 20	19 18	17 16	15 14	13 12	11 10	9 8	7 6	5 4	3 2	1 0
PIC15	PIC14	PIC13	PIC12	PIC11	PIC10	PIC9	PIC8	PIC7	PIC6	PIC5	PIC4	PIC3	PIC2	PIC1	PIC0
00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Bits	Name	Function	
2x+1	PICx	Port n Pin interrupt Control bits, x:0 to 15	
2x		00	Prohibit external interrupt
		01	Low level interrupt or Falling edge interrupt mode
		10	High level interrupt or Ralling edge interrupt mode
		11	Both of rising and falling edge interrupt mode Not support for level trigger interrupt mode.

5.4.15 PF_PLSR Port F Level Select Register

PORT F level select register. PF5, PF6, PF7 are open-drain only pins. If user use these pins for 1.8V level instead VDD, These bits must be set.

PF_PLSR=0x4000_1538

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																													PF7LSB	PF6LSB	PF5LSB
-																													0	0	0
-																													RW	RW	RW

Bits	Name	Function	
2	PF7LSB	PORTF 7 Level Select bit.	
		0	VDD level (default)
		1	1.8V level
1	PF6LSB	PORTF 6 Level Select bit.	
		0	VDD level (default)
		1	1.8V level
0	PF5LSB	PORTF 5 Level Select bit.	
		0	VDD level (default)
		1	1.8V level

5.4.16 PCU_PORTEN Port Access Enable Register

PORTEN enables register writing permission of all PCU registers.

PCU_PORTEN=0x4000_0FF0

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																								PORTEN							
-																								--							
-																								WO							

7 0	PORTEN	Writing the sequence of 0x15 and 0x51 in this register enables writing to PCU registers, and writing other values protects all PCU registers from writing.

Note) how to use PORTEN.

```
PORTEN=0x15; PORTEN=0x51;    // enable PORTEN
…                            // set Pn.MOD, Pn.TYP, Pn.AFSR1,2, Pn.PUPD. Pn.DBCR, Pn.IER, Pn.ICR
PORTEN=0;                    // disable PORTEN
```

5.5 Functional Description

When the input functions of I/O port is used by Pin Control Register, the output function of I/O port is disabled.

The Port Function different according to the Alteranative Function Selection Register.

The Input Data Register capture the data present on the I/O pin or Debounced input data at every GPIO Clock cycle.

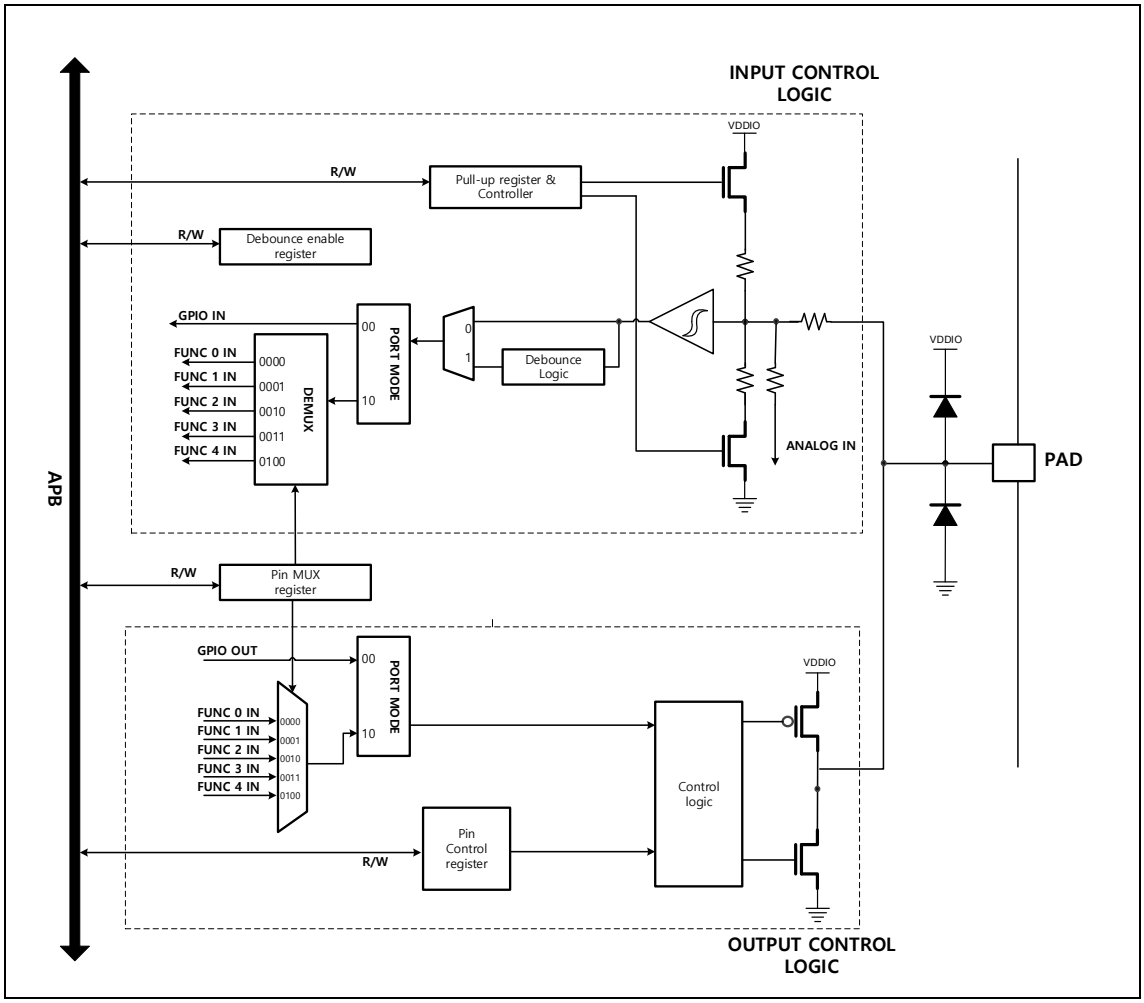


Figure 5.5 Port diagram

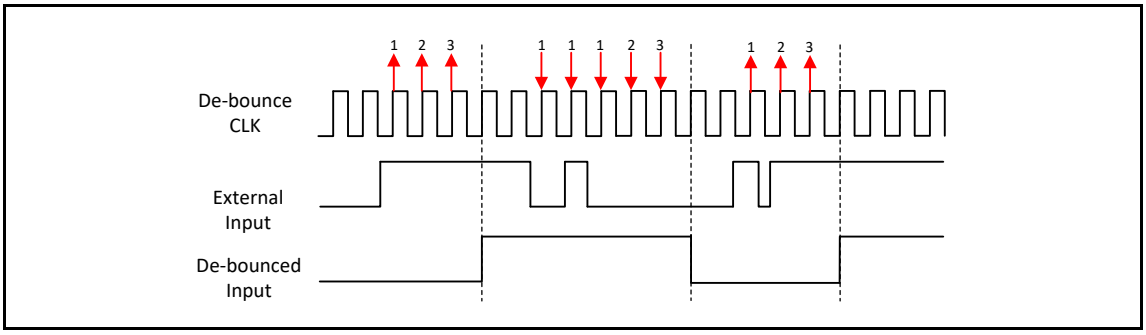


Figure 5.6 Debounce function

When configured as output, the value written to the GPIO Ouput Data Register is output on the I/O Pin.

When set the Bit Set Register, GPIO Output Data Register set the high.

When set the Bit Clr Register, GPIO Output Data Register set the Low.

The Input Data Register capture the data present on the I/O pin or Debounced input data at every GPIO Clock cycle.

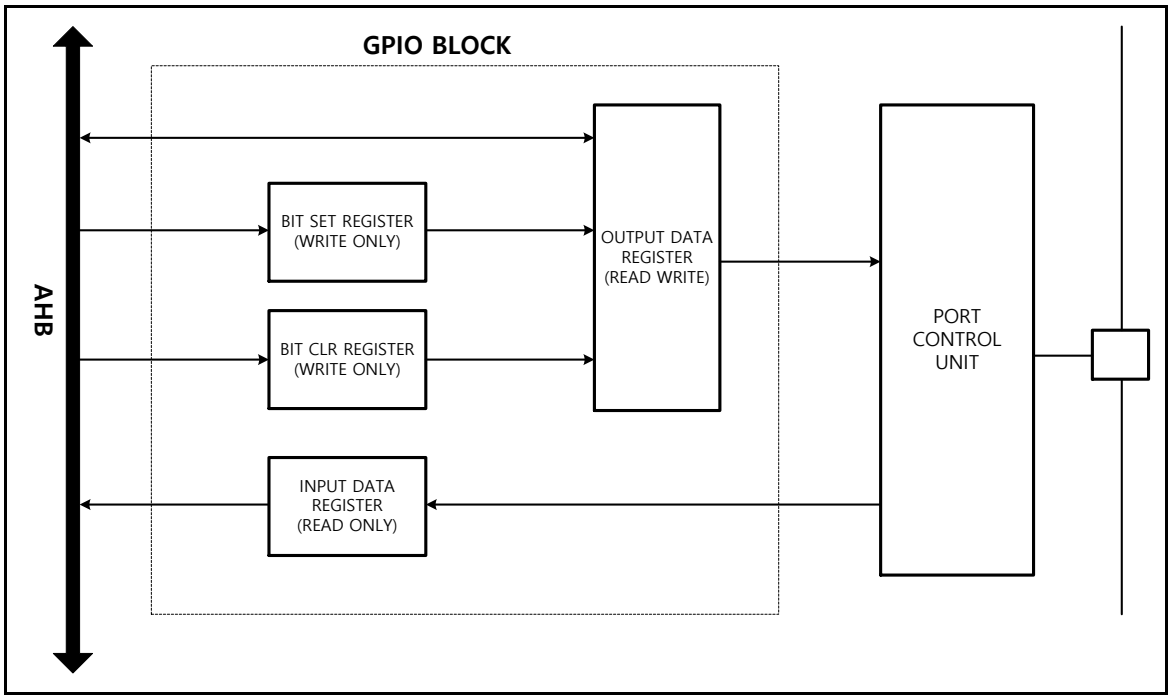


Figure 5.7 GPIO diagram

CHAPTER 6. FLASH MEMORY CONTROLLER

6.1 OVERVIEW

Flash Memory Controller is an internal flash memory interface controller.

- 0-wait, 1-wait, 2-wait(default)
- Read protection support
- Self Program support
- User option area
  - 3-page (each 512 Bytes)
  - Erase, Program in user mode

Item	Decription
Size	64KB / 128KB / 256KB
Start Address	0x0000_0000
End Address	0x0002_0000
Page Size	512-byte
Total Page Count	256 pages
PGM Unit	512-byte
Erase Unit	512-byte / 1KB / 4KB / bulk

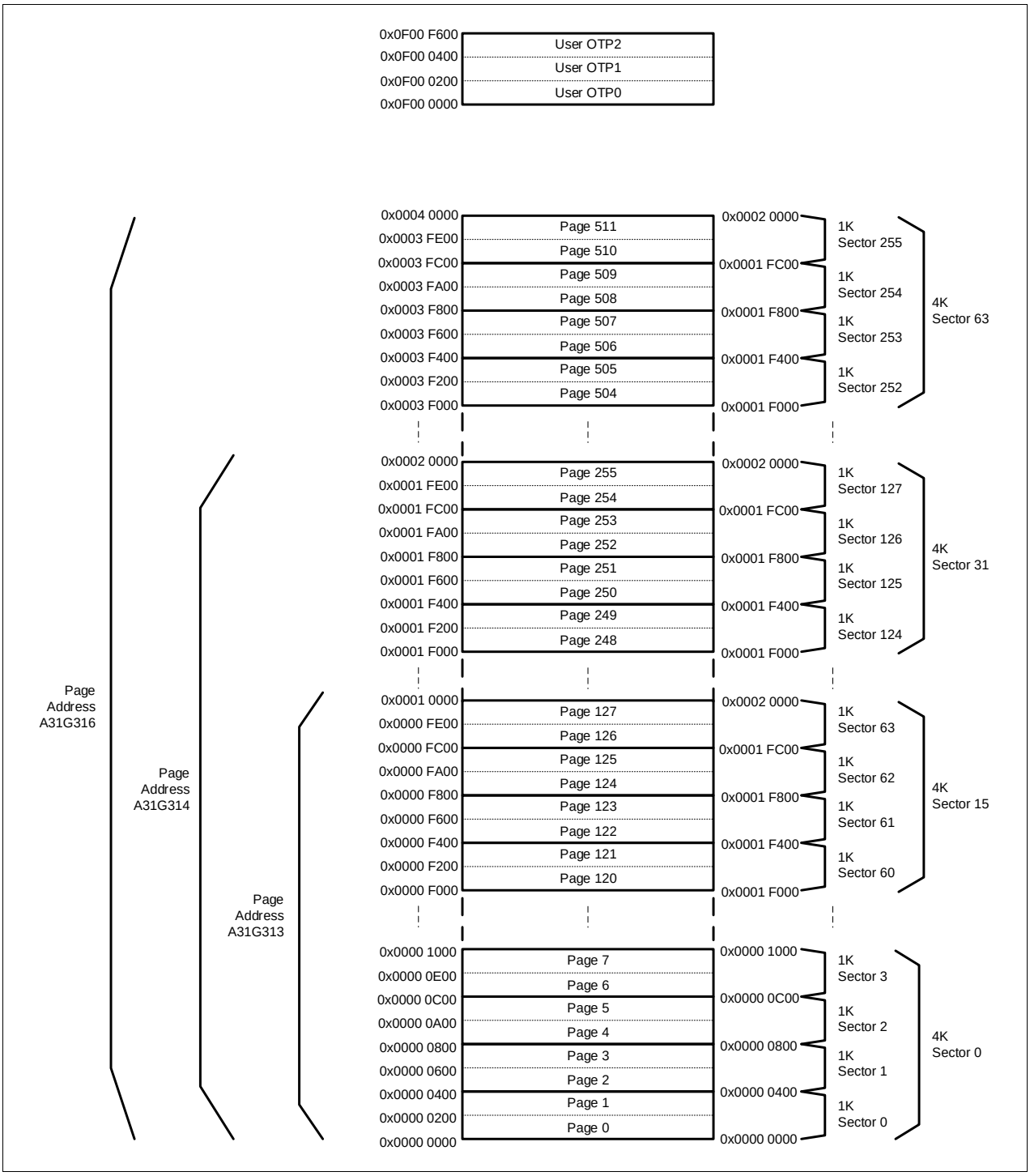


Figure 6.1 Flash Memory Map

6.2 REGISTERS

Base address of Flash Memory Controller is below.

Table 6.1 Flash Memory Controller base address

NAME	BASE ADDRESS
Flash Controller	0x4000_0100

Table 6.2 FMC Register map

Register Name	Offset	Access Type	Description	Initial Value	Ref
FMC_MR	0x04	R/W	Flash Memory Mode Select register	0x0100_0000	6.2.1
FMC_CR	0x08	R/W	Flash Memory Control register	0x0000_0000	6.2.2
FMC_AR	0x0C	R/W	Flash Memory Address register	0x0000_0000	6.2.3
FMC_DR	0x10	R/W	Flash Memory Data register	0x0000_0000	6.2.4
FMC_BUSY	0x18	R/W	Flash Write Busy Status Register	0x0000_0000	6.2.5
FMC_CRC	0x20	R/W	Flash CRC16 check value	0x0000_FFFF	6.2.6
FMC_CFG	0x30	R/W	Flash Memory Config Register	0x0000_8200	6.2.7
FMC_WPROT	0x34	R/W	Write Protection Register	0xFFFF_FFFF	6.2.8
FMC_LOCK	0x3C	R/W	Flash LOCK register	0x0000_00FF	6.2.9

6.2.1 FMC_MR Flash Memory Mode Register

Internal flash memory mode register. This register is 32-bit register.

FMC_MR=0x4000_0104

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																								ACODE							
-																								0x00							
-																								RW							

7	ACODE	5A → A5	Flash mode entry
0		A5 → 5A	Trim mode entry
		81 → 28	AMBA mode entry
		66 → 99	PROT mode entry

6.2.2 FMC_CR Flash Memory Control Register

Internal flash memory control register.

FMC_CR=0x4000_0108

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved							LOCKSEL	SELFPGM	Reserved										IFEN	Reserved			BBLOCK	MAS	SECT4K	SECT1K	PMODE	WADCK	PGM	ERS	HVEN
-							0	0	-										0	-			0	0	0	0	0	0	0	0	0
-							RW	RW	-										RW	-			RW	RW	RW	RW	RW	RW	RW	RW	RW

24	LOCKSEL		LOCK(read protection) access enable.
23	SELFPGM		When this bit is set("1"), PGM/ERS/HVEN will be cleared automatically after WRBUSY falling edge. It also enable CPU wait control when HVEN bit is set(1) (start of program or erase operation) It also affects to PMODE bit operation.
12	IFEN	0	Info(OTP1/2/3) block enable
		1	OTP1/2/3 area enable (it works with OTP3EN ~ OTP1EN) for PMODE operation
8	BBLOCK	0	Boot Block(1st 4KB) not protected from Mass(Bulk) Erase
		1	Boot Block(1st 4KB) protection enable from Mass(bulk) erase
7	MAS	0	Mass(bulk) erase disable
		1	Mass(bulk) erase enable.
6	SECT4K	0	Sector 4K erase disable
		1	Sector 4K erase enable
5	SECT1K	0	Sector 1K erase disable
		1	Sector 1K erase enable
4	PMODE	0	Normal mode
		1	PMODE enable(Flash Address path is connected with FMAR) PMODE only valid when SELFPGM bit was not set(when SELFPGM = 0)
3	WADCK	0	Program/Erase address data latch clock disable
		1	Program/Erase address data latch clock enable, this bit assert for one system clock period so user can not read
2	PGM	0	Program mode disable
		1	Program mode enable
1	ERS	0	Erase mode disable
		1	Erase mode enable
0	HVEN	0	High Voltage cycle disable
		1	High Voltage cycle enable (start program or erase cycle) User must set and clear in PMODE. In SELFPGM mode, user must set HVEN then HVEN will be cleared automatically after WRBUSY goes low.

6.2.3 FMC_AR Flash Memory Address Register

Internal flash memory program, erase address register

FMC_AR=0x4000_010C

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																FADDR															
-																0x0000															
-																RW															

16 0	FADDR	Word(32-bit) base address : 64K-word address for 256KB Flash. Auto Incremental after WADCK trigger (after latching of target address).

6.2.4 FMC_DR Flash Data Input register

Internal flash memory Data Input register

FMC_DR=0x4000_0110

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FDATA																															
0x00000000																															
RW																															

31 0	FDATA	Word size(32-bit)

6.2.5 FMC_BUSY Flash Write Busy Status Register

Flash write(program/erase) busy status monitor register. This register is 1-bit read only register.

FMC_BUSY=0x4000_0118

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																															WRBUSY
-																															0
-																															RO

0	WRBUSY	Write Busy status bit FLBUSY bit goes high after set HVEN bit (in CTRL register). FLBUSY bit goes low when WRBUSY becomes low after program(or erase) complete.

6.2.6 FMC_CRC Flash CRC check register

Internal flash memory Burst Mode channel selection register

FMC_CRC=0x4000_0120

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																CRC16															
-																0xFFFF															
-																RW															

15 0	CRC16		CRC16 check value read register polynomial: (1 + x5 + x12 + x16) data width: 32 (the first serial bit is D[31])

6.2.7 FMC_CFG Flash Memory Config Register

Internal flash memory Config register. This register has the same address with FMTRIM0 register

FMC_CFG=0x4000_0130

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
WTIDKY																Reserved						WAIT		CRCINIT	CRCEN	Reserved					
0x0000																-						1		0	0	-					
RW																-						RW		RW	RW	-					

31 16	WTIDKY		Write Identification Key. On writes, write 0x7858 to these bits, otherwise the write is ignored.
9 8	WAIT		This bits only be written in AMBA mode and MSB 16-bit (bit [31:16]) must be 0x7858
		00	WAIT is 00, flash access in 1 cycle (0-wait)
		01	WAIT is 01, flash access in 2 cycles (1-wait)
		10	WAIT is 10, flash access in 3 cycles (2-wait) – default
		11	WAIT is 11, flash access in 4 cycles (3-wait)
7	CRCINIT	0	When this bit is set('1'), CRC register will be initialized It should be reset again before read flash to generate CRC16 calculation (Initial value of FMCRC is 0xFFFF)
6	CRCEN	0	CRC16 enable CRC value will be calculated at every flash read timing

6.2.8 FMC_WPROT Write Protection Register

Internal flash memory write protection register.

FMC_WPROT=0x4000_0134

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																WPROT (A31G316)															
-																0xFFFF															
-																RW															
Reserved																								WPROT (A31G314)							
-																								1111_1111							
-																								RW							
Reserved																														WPROT (A31G313)	
-																														1111	
-																														RW	

31 0	WPROT	Write protection each 16 KB segments for whole memory address Note 1) Protection Range = WPROT[n] : (n*16kB) ~ (16kB * (n+1) - 1) Note 2) The FM_WPROT register can only be modified in PROT (FM_MR = 66-> 99) mode.

6.2.9 FMC_LOCK Flash LOCK register

Internal flash memory read protection register.

FMC_LOCK=0x4000_013C

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																								RPROT							
-																								1111_1111							
-																								RW							

7 0	RPROT	Read protection 0x0000_00FF is Default. Any other value will lock falsh(enable read protection) In user mode, 0xFF can not be written To unlock, user must erase LOCK area of Flash next to MAS(bulk) erase - 1st MAS(bult) erase and then erase LOCK area - To unlock the flash, pin reset or power on reset required Note) The FM_WPROT register can only be modified in PROT (FM_MR = 66-> 99) mode.

6.3 Functional Description

6.3.1 Flash Erase and Program examples

The basic step of Flash memory program consists with following three steps. Minimum Program or Erase unit is a Page and 32-word (5-byte) become a page.

(1) Page Erase
(2) Page Program
(3) Self Page Erase
(4) Self Page Program

For every erase operations, pre-program operation is needed to prevent over erase of flash memory cells.
User must enable 48MHz internal oscillator first to erase or program flash.

(1) Erase example
- A. Flash mode enable to write FM.FMCR register (write 0x5A and then write 0xA5 into FM.FMMR)
- B. Set target Page address in FM.FMAR
- C. Set PMODE bit first
- D. Set ERS , WADCK, HVEN bits of FM.FMCR
- E. Wait until IDLE bit of FM.FMMR register become “0” after erase
- F. Clear ERS, HVEN bits of FM.FMCR
- G. Set 0x80 to FM.FMBUSY
- H. Clear FM.FMCR
- I. Clear Flash mode (write 0x00 and then write 0x00 into FM.FMMR)

(2) Program example
- A. Flash mode enable to write FM.FMCR register (write 0x5A and then write 0xA5 into FM.MR)
- B. Set PMODE bit first
- C. Set target Page address in FM.AR
- D. Set PGM bits of FM.FMCR
- E. Write word(32-bit) data into FM.DR, address increased automatically based on word address
- F. Set WADCK, HVEN bits of FM.CR
- G. Wait until IDLE bit of FM.MR register become “0” after program
- H. Clear HVEN bits of FM.CR
- I. Set 0x80 to FM.FMBUSY
- J. Clear PGM bits of FM.FMCR
- K. Clear FM.FMCR
- L. Clear Flash mode (write 0x00 and then write 0x00 into FM.FMMR)

(3) Self Erase example
- A. Flash mode enable to write FM.CR register (write 0x5A and then write 0xA5 into FM.MR)
- B. Set SELFPGM, ERS bits of FM.CR
- C. Wait 5-clock
- D. Write “0xFFFFFFFF” into target address.
- E. Wait 5-clock
- F. Clear ERS bits of FM.CR
- G. Clear FM.FMCR
- H. Wait 5-clock

I. Clear Flash mode (write 0x00 and then write 0x00 into FM.FMMR

(4) Self Program example

A. Flash mode enable to write FM.CR register (write 0x5A and then write 0xA5 into FM.MR)
B. Set SELFPGM, PGM bits of FM.CR
C. Wait 5-clock
D. Write word(32-bit) data into target address.
E. Wait 5-clock
F. Clear PGM bits of FM.CR
G. Clear FM.FMCR
H. Wait 5-clock
I. Clear Flash mode (write 0x00 and then write 0x00 into FM.FMMR

CHAPTER 7. INTERNAL SRAM

7.1 OVERVIEW

The A31G31x has a block of 0-wait on-chip SRAM. The size of SRAM is 16KB.

The SRAM base address is 0x2000_0000

The SRAM memory area is usually used for data memory and stack memory. Sometimes the code is dumped into the SRAM memory for fast operation or flash erase/pgm operation.

This device does not support memory remap strategy. So jump and return is required to perform the code in SRAM memory area.

CHAPTER 8. DIRECT MEMORY ACCESS CONTROLLER (DMAC)

8.1 OVERVIEW

DMA is direct memory access controller

The A31G31x's DMA can access UART Tx & Rx and CRC blocks.

DMA transfers data from RAM to peripheral devices or transfers data from peripheral devices to RAM.

- 4 Channels
- Single transfer only
- Support 8/16/32-bit data size
- Support multiple buffer with same size
- Interrupt condition is transferred through peripheral interrupt

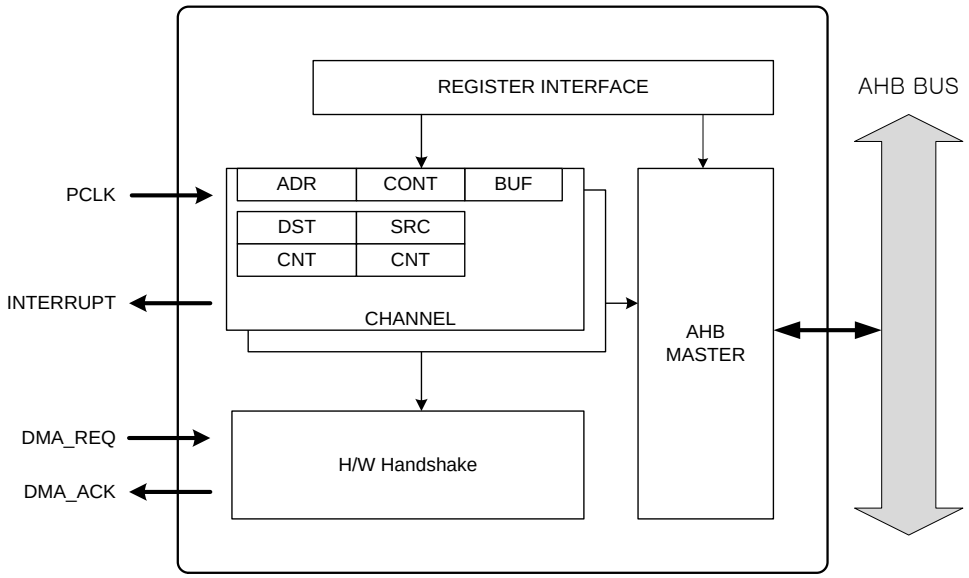


Figure 8.1. Block Diagram

8.2 REGISTERS

Base addresse of DMAC unit is as below.

Table 8.1 DMAC base address

NAME	BASE ADDRESS
DMA0	0x4000_0400
DMA1	0x4000_0410
DMA2	0x4000_0420
DMA3	0x4000_0430

Table 8.2 DMAC Register map

Register Name	Offset	Access Type	Description	Initial Value	Ref
DMAn_CR	0x00	RW	DMA Channel n Control Register	0x0000_0000	8.2.1
DMAn_SR	0x04	RW	DMA Channel n Status Register	0x0000_0000	8.2.2
DMAn_PAR	0x08	RO	DMA Channel n Peripheral Address	0x4000_0000	8.2.3
DMAn_MAR	0x0C	RW	DMA Channel n Memory Address	0x2000_0000	8.2.4

8.2.1 DMAn_CR DMA Controller Configuration Register

DMA operation control register is 32-bit register.

DMA0_CR=0x4000_0400, DMA1_CR=0x4000_0410
DMA2_CR=0x4000_0420, DMA3_CR=0x4000_0430

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2	1	0
Reserved	TRANSCNT	Reserved	PERSEL	Reserved	SIZE	DIR	Reserved
-	0x000	-	0000	-	00	0	-
-	RW	-	RW	-	RW	RW	-

27 16	TRANSCNT	Number of DMA transfer remained Required transfer number should be written before enable DMA transfer.
		0 DMA transfer is done.
		N N transfers are remained
15 8	PERISEL	Peripheral selction
		N Associated peripheral selection. Refer to DMA Peripheral connection table
3 2	SIZE	Bus transfer size.
		00 DMA transfer is byte size transfer
		01 DMA transfer is half word size transfer
		10 DMA transfer is word size transfer
		11 Reserved
1	DIR	Select transfer direction.
		0 Transfer direction is from memory to peripheral. (TX)
		1 Transfer direction is from peripheral to memory (RX)

A DMA channel will be connected with selected peripheral. Below table shows peripheral selction numbers.
This PERISEL field should be set with proper number of peripheral which will be connected with DMA interface.

PERISEL[3:0]	Associatec Peipheral
0	CHANNEL IDLE
1	UART0 RX
2	UART0 TX
3	UART1 RX
4	UART1 TX
5	CRC
Others	N/A

PERISEL can not have same value in different channels. If same PERISEL value wriiten in more than one channel, the proper operation is not guaranteed.
Not used channel should have CHANNEL IDLE value in PERISEL bit postions.

8.2.2 DMAn_SR DMA Controller Status register

DMA Controller Status Register is 8-bit register.

This register represents the current status of DMA Controller and enables DMA function.

DMA0_SR=0x4000_0404 , DMA1_SR=0x4000_0414
DMA2_SR=0x4000_0424 , DMA3_SR=0x4000_0434

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																								EOT	Reserved						DMAEN
-																								1	-						0
-																								RO	-						RW

7	EOT	End of transfer.	
		0	Data to be transferred is existing. TRANSCNT shows non zero value
		1	All data is transferred. TRANSCNT shows now 0
0	DMAEN	DMA Enable	
		0	DMA is in stop or hold state
		1	DMA is running or enabled

8.2.3 DMAn_PAR DMA Controller Peripheral Address register

These registers represent the peripheral address.

DMA0_PAR=0x4000_0408 , DMA1_PAR=0x4000_0418
DMA2_PAR=0x4000_0428 , DMA3_PAR=0x4000_0438

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Peripheral BASE OFFSET																PAR															
0x4000																0x0000															
RO																RW															

15 0	PAR	Target Peripheral address of transmit buffer or receive buffer. Address is fixed address when each transfer is done. If DIR is “0” this address is destination address of data transfer. If DIR is “1”, this address is source address of data transfer.

8.2.4 DMAn_MAR DMA Controller Memory Address register

These registers represent the memory address.

DMA0_MAR=0x4000_040C , DMA1_MAR=0x4000_041C
DMA2_MAR=0x4000_042C , DMA3_MAR=0x4000_043C

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Memory BASE OFFSET																MAR															
0x2000																0x0000															
RO																RW															

31 0	MAR	Target memory address of data transfer. Address is automatically incremented according to SIZE bits when each transfer is done. If DIR is “0” this address is source address of data transfer. If DIR is “1”, this address is destination address of data transfer.

8.3 Functional Description

The DMA controller performs direct memory transfer by sharing the system bus with CPU core. The system bus is shared by 2 AHB masters following the round-robin priority strategy. So the DMA controller can share the half of system bandwidth.

The DMA controller can be triggered only peripheral request. When a peripheral request the transfer to the DMA controller, related channel is activate and access the bus to transfer requested data from memory to peripheral data buffer or from peripheral data buffer to memory space.

- User set both of peripheral address and memory address
- User configure DMA operation mode and transfer count.
- User enable DMA channel
- DMA request is occurred from peripheral.
- DMA activate channel which was requested
- DMA read data from source address and save it internal buffer.
- DMA write the buffered data to destination address.
- Transfer count number is decreased by 1.
- When Transfer count is 0, EOT flag is set and notice to peripheral to issue the interrupt
- DMA does not have interrupt source, the interrupt related DMA status can be shown from assigned peripheral interrupt.

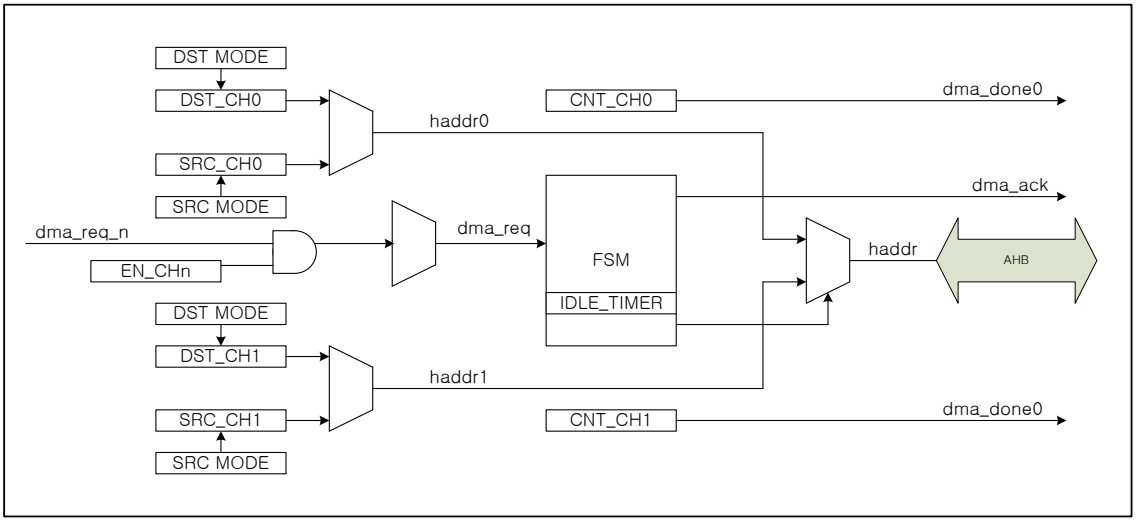
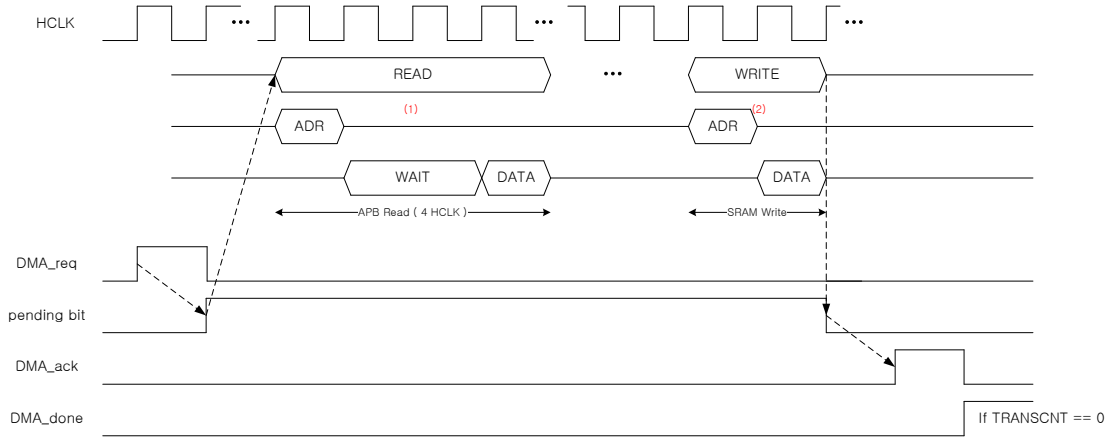
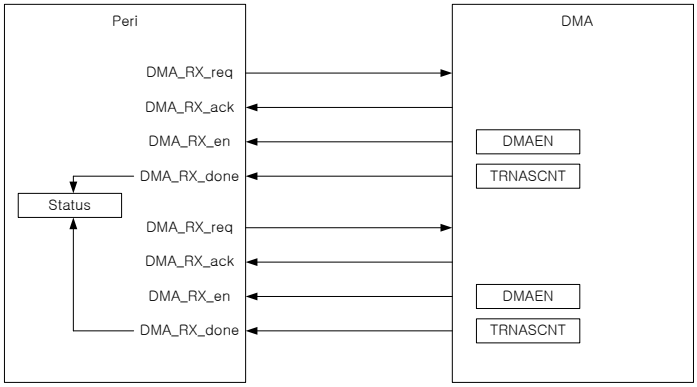


Figure 8.2. DMA Block Diagram


HCLK
READ
WRITE
(1)
ADR
(2)
ADR
WAIT
DATA
DATA
APB Read (4 HCLK)
SRAM Write
DMA_req
pending bit
DMA_ack
DMA_done
If TRANSCNT == 0

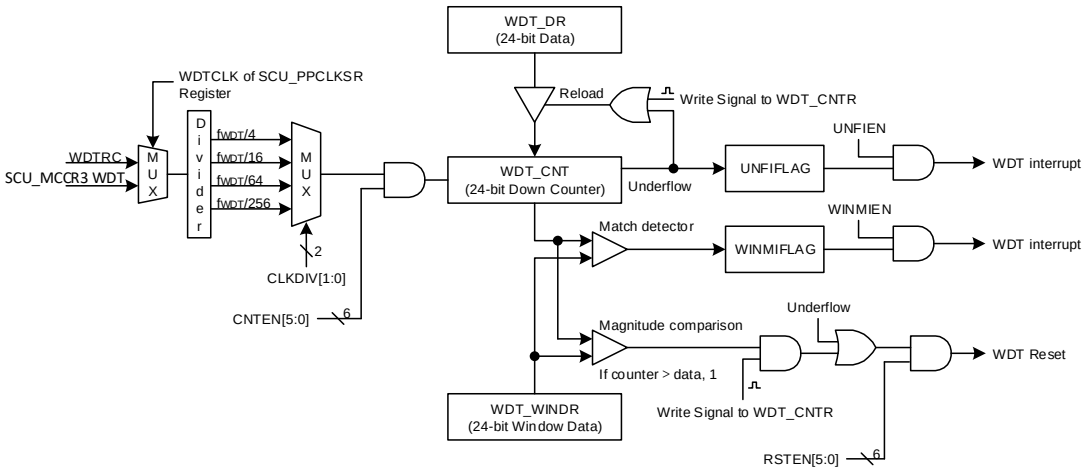

Peri
DMA
DMA_RX_req
DMA_RX_ack
DMA_RX_en
DMA_RX_done
DMAEN
TRNASCNT
Status
DMA_RX_req
DMA_RX_ack
DMA_RX_en
DMA_RX_done
DMAEN
TRNASCNT

CHAPTER 9. WATCH-DOG TIMER (WDT)

9.1 OVERVIEW

The watchdog timer rapidly detects the CPU malfunction such as endless looping caused by noise or something like that and resumes the CPU to the normal state. The watchdog timer signal for malfunction detection can be used as either a CPU reset or an interrupt request. When the watchdog timer is not being used for malfunction detection, it can be used as a timer to generate an interrupt at fixed intervals. When WDT_CNT value is reached WDT_WINDR value, a watchdog interrupt can be generated. The underflow time of the watchdog timer can set by WDT_DR. If an underflow occurs, an internal reset is generated. The watchdog timer operates on the WDTRC embedded RC oscillator clock.

- 24-bit down counter (WDT_CNT)
- Select reset or periodic interrupt
- Count clock selection
- Watchdog overflow output signal
- Include Conuter Window function



Note)

1. If a reload signal is generated, the WDT_DR value reloads to WDT_CNT register after 1-clock delay with the clock which is selected by the CLKDIV bits

Figure 9.1 Block diagram

9.2 REGISTERS

Initial watchdog time-out period is set to 2,000-milisecond.

Base addresse of Watch Dog Timer is as below.

Table 9.1 Base address of SCU

NAME	BASE ADDRESS
WDT	0x4000_1A00

Table 9.2 Watchdog timer register map

Register Name	Offset	Access Type	Description	Initial Value	Ref
WDT_CR	0x00	RW	Watch-dog Timer Control Register	0x0000_0000	9.2.1
WDT_SR	0x04	RW	Watch-dog Timer Status Register	0x0000_0080	9.2.2
WDT_DR	0x08	RW	Watch-dog Timer Data Register	0x0000_3D09	9.2.3
WDT_CNT	0x0C	RO	Watch-dog Timer Counter Register	0x0000_0FFF	9.2.4
WDT_WINDR	0x10	RW	Watch-dog Timer Window Data Register	0x0000_FFFF	9.2.5
WDT_CNTR	0x14	WO	Watch-dog Timer Counter Reload Register	0x0000_0000	9.2.6

9.2.1 WDT_CR Watch-dog Timer Control Register

WDT module should be configured properly before running. WDT module can make reset event or assert interrupt signal to system.

WDT_CR=0x4000_1A00

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10	9 8	7 6 5 4	3	2	1 0
WTIDKY		RSTEN	CNTEN		WINMIEN	UNFIEN	CLKDIV
0x0000		000000	000000		0	0	00
WO		RW	RW		RW	RW	RW

31 16	WTIDKY	Write Identification Key. On writes, write 0x5A69 to these bits, otherwise the write is ignored.
15 10	RSTEN	Watch-dog Timer Reset Enable bits. 0x25 Disable watch-dog timer reset. Others Enable watch-dog timer reset.
9 4	CNTEN	Watch-dog Timer Counter Enable bits. 0x1A Disable watch-dog timer counter. Others Enable window data match interrupt.
3	WINMIEN	Watch-dog Timer Window Match Interrupt Enable bit. 0 Disable window data match interrupt. 1 Enable window data match interrupt.
2	UNFIEN	Watch-dog Timer Underflow Interrupt Enable bit. 0 Disable watch-dog timer underflow interrupt. 1 Enable watch-dog timer underflow interrupt.
1 0	CLKDIV	Watch-dog Timer Clock Divider bits, The clock which is selected by PPCLKSR[0]. 00 fWDT/4 01 fWDT/16 10 fWDT/64 11 fWDT/256

9.2.2 WDT_SR Watch-dog Timer Status Register

This register is used to set the WDT operation at CPU halt,and make sure the WDT flag.

WDT_SR=0x4000_1A04

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																								DBGCNTEN	Reserved					WINMIFLAG	UNFIFLAG
-																								1	-					0	0
-																								RW	-					RW	RW

7	DBGCNTEN	Watch-dog Timer Counter Enable bit When the core is halted in the debug mode.
	0	The watch-dog timer counter continues even if the core is halted.
	1	The watch-dog timer counter is stopped when the core is halted.
	Note) 1. This bit is set to “1b” by POR reset.	
1	WINMIFLAG	Watch-dog Timer Window Match Interrupt Flag bit.
	0	No request occurred.
	1	Request occurred, This bit is cleared to ‘0’ when write ‘1’.
0	UNFIFLAG	Watch-dog Timer Underflow Interrupt Flag bit.
	0	No request occurred.
	1	Request occurred, This bit is cleared to ‘0’ when write ‘1.

9.2.3 WDT_DR Watch-dog Timer Data Register

The WDT_DR register is used to update WDT_CNT register. When a value is input to the When reloading using WDT_CNTR, WDT_CNT is updated to WDT_DR value.

WDT_DR=0x4000_1A08

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved								DATA																							
-								0x003D09																							
-								RW																							

23 0	DATA	Watch-dog Timer Data bits. The range is 0x000000 to 0xFFFFFF.

Note)

1. Once any value is written to this data register, the register can't be changed until a system reset.

9.2.4 WDT_CNT Watch-dog Timer Counter Register

The WDT_CNT register represents the current count value of 32-bit down counter. When the counter value reach to 0, the interrupt or reset will be asserted.

WDT_CNT=0x4000_1A0C

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved								CNT																							
-								0x000FFF																							
-								RO																							

23 0	CNT	Watch-dog Timer Counter bits.

9.2.5 WDT_WINDR Watch-dog Timer Window Data Register

The WDT_WINDR register is used to compare with WDTCNT for WINDOW function.

if WDT_CNT is updated by WDT_CNTR when WDT_CNT value is bigger than WDT_WINDR value, WDT reset or WDT interrupt is occured.

WDT_WINDR=0x4000_1A10

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved								WDATA																							
-								0x00FFFF																							
-								RW																							

23 0	WDATA	Watch-dog Timer Data bits. The range is 0x000000 to 0xFFFFFF.

Note)

1. Once any value is written to this data register, the register can't be changed until a system reset.

9.2.6 WDT_CNTR Watch-dog Timer Counter Reload Register

The WDT_CNTR register is used to make reload signal. If reload signal is occured, WDT_DR Value is reloaded to WDT_CNT.

WDT_CNTR=0x4000_1A14

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																								CNTR							
-																								0x00							
-																								WO							

7 0	CNTR	Watch-dog Timer Counter Reload bits.	
		0x6A	Reload the WDTDR value to watch-dog timer counter and re-start. (Automatically cleared to "0x00" after operation)
		Others	No effect

9.3 Functional Description

The watchdog timer count can be enabled by CNTEN (WDT_CR[9:4]) set as any value other than 0x1A. As the watchdog timer activates, the down counter will start counting from the load value. If the RSTEN (WDT_CR[15:10]) is set as any value other than 0x25, WDT reset would be asserted when the WDT counter value reaches 0(underflow event) from WDT_DR value. Before WDT counter reaches 0, software can write 0x6A to WDT_CNTR register in order to reload WDT counter when the counter value is less than or equal to the value of window data register. WDT reset may be asserted if the reload occurs when counter > window data.

9.3.1 Timing diagram

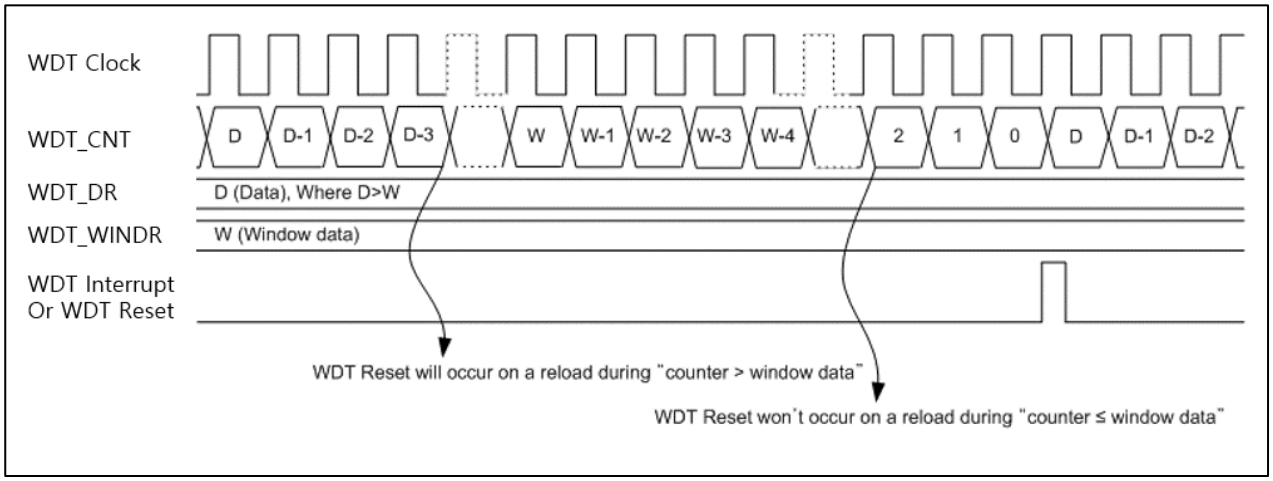


Figure 9.2 WDT Interrupt and WDT Reset Timing diagram

9.3.2 Prescale table

The WDT includes a 24-bit down counter with programmable pre-scaler to define different time-out intervals.

The clock sources of watchdog timer can be WDTRC or PCLK. PCLK can be selected by WDTCLK (SCU_PPCLKSR[0]) set to '1' and then the WDTCNFIG[2] bit of configure option page 1 is cleared to logic "0b".

To make a WDT counter base clock, user can control 2-bit pre-scaler CLKDIV [1:0] in the WDTCR register, and the maximum pre-scaled value is "clock source frequency/256". The pre-scaled WDT counter clock frequency values are listed in the following table.

Selectable clock source (40 kHz ~ 48 MHz) and time-out interval at a single count

Time-out period = (Load Value + 1) * (1/pre-scaled WDT counter clock frequency)

*Time out period (when the Load Value reaches 0, underflow flag is set to '1')

Table 9.3 Pre-scaled WDT counter clock frequency

Clock source	WDTCLKIN	WDTCLKIN /4	WDTCLKIN /16	WDTCLKIN /64	WDTCLKIN /256
WDTRC	31.250 kHz	7.8125 kHz	1.953125 kHz	488.28125 Hz	122.0703125 Hz
SCU_MCCR3 WDT	MCCR3 WDT	MCCR3 WDT/4	MCCR3 WDT/16	MCCR3 WDT/64	MCCR3 WDT/256

CHAPTER 10. WATCH TIMER

10.1 OVERVIEW

The watch timer has the function for RTC (Real Time Clock) operation. It is generally used for RTC design. The internal structure of the watch timer consists of the clock source select circuit, timer counter circuit, output select circuit and watch timer control register. To operate the watch timer, determine the input clock source, output interval and set WTEN as '1' in watch timer control register (WT_CR). It is able to execute simultaneously or individually. To stop or reset WT, clear the WTEN bit in WT_CR register. Even if CPU is STOP mode, sub clock is able to be alive and so WT can continue the operation. The watch timer counter circuits is composed of 26-bit counter. Low 14-bit is binary counter and high 12-bit is auto reload counter in order to raise resolution. In WTR, it can control WT clear and set Interval value at write time, and it can read 12-bit WT counter value at read time.

- 14-bit Divider
- 12-bit up-counter
- RTC function

Figure shows the block diagram of a watch timer block.

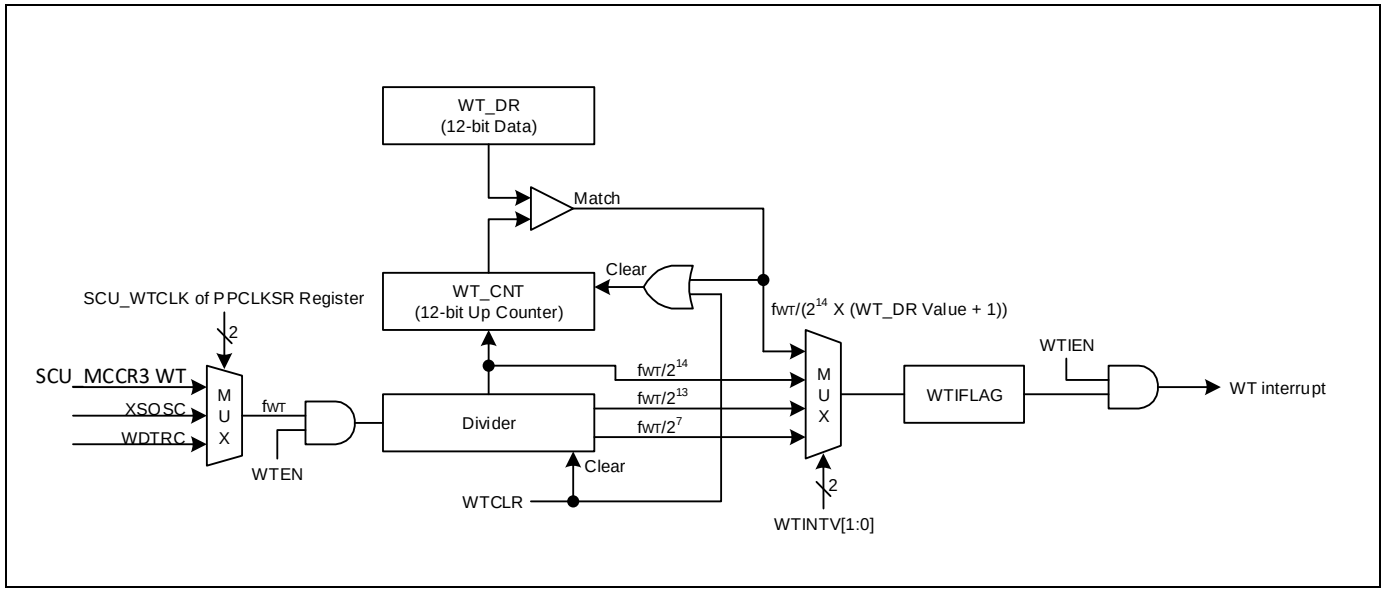


Figure 10.1 Block diagram

10.2 REGISTERS

Base addresse of Watch Timer is as below.

Table 10.1 Base Address of Watch Timer

NAME	BASE ADDRESS
WT	0x4000_2000

Table 10.2 Timer Register Map

Register Name	Offset	Access Type	Description	Initial Value	Ref
WT_CR	0x00	RW	Watch Timer Control Register	0x0000_0000	10.2.1
WT_DR	0x04	RW	Watch Timer Data Register	0x0000_0FFF	10.2.2
WT_CNT	0x08	RO	Watch Timer Counter Register	0x0000_0000	10.2.3

10.2.1 WT_CR Watch Timer Control Register

Watch Timer Control Register is 32-bit register.

WT_CR=0x4000_2000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																								WTEN	Reserved	WTINTV		WTIEN	Reserved	WTIFLAG	WTCLR
-																								0	-	00		0	-	0	0
-																								RW	-	RW		RW	-	RW	RW

7	WTEN	Watch Timer Operation Enable bit.
		0 Disable watch timer operation.
		1 Enable watch timer operation.
5 4	WTINTV	Watch Timer Interval Selection bits. 00 $fWT/2^7$ 01 $fWT/2^{13}$ 10 $fWT/2^{14}$ 11 $fWT/(2^{14}x(WTDR\ value + 1))$ Note) 1. These bits should be changed during WTEN bit is “0b”.
3	WTIEN	Watch Timer Interrupt Enable bit.
		0 Disable watch timer interrupt.
		1 Enable watch timer interrupt.
1	WTIFLAG	Watch Timer Interrupt Flag bit.
		0 No request occurred.
		1 Request occurred, This bit is cleared to ‘0’ when write ‘1’.
0	WTCLR	Watch Timer Counter and Divider Clear bit.
		0 No effect.
		1 Clear the counter and divider (Automatically cleared to “0b” after operation)

10.2.2 WT_DR Watch Timer Data Register

Watch Timer Data Register is 32-bit register.

Match value of Watch timer. If value of WT_CNT is matched by WT_DR, WT matched event is ocurred.

WT_DR=0x4000_2004

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																				WTDATA											
-																				0xFFF											
-																				RW											

11 0	WTDATA	Watch Timer Data bits. The range is 0x001 to 0xFFF.

10.2.3 WT_CNT Watch Timer Counter Register

Watch Timer Counter Register is 32-bit register.

WT_CNT=0x4000_2008

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																				CNT											
-																				0x000											
-																				RW											

11 0	CNT	Watch Timer Counter bits.

CHAPTER 11. 16-BIT TIMER

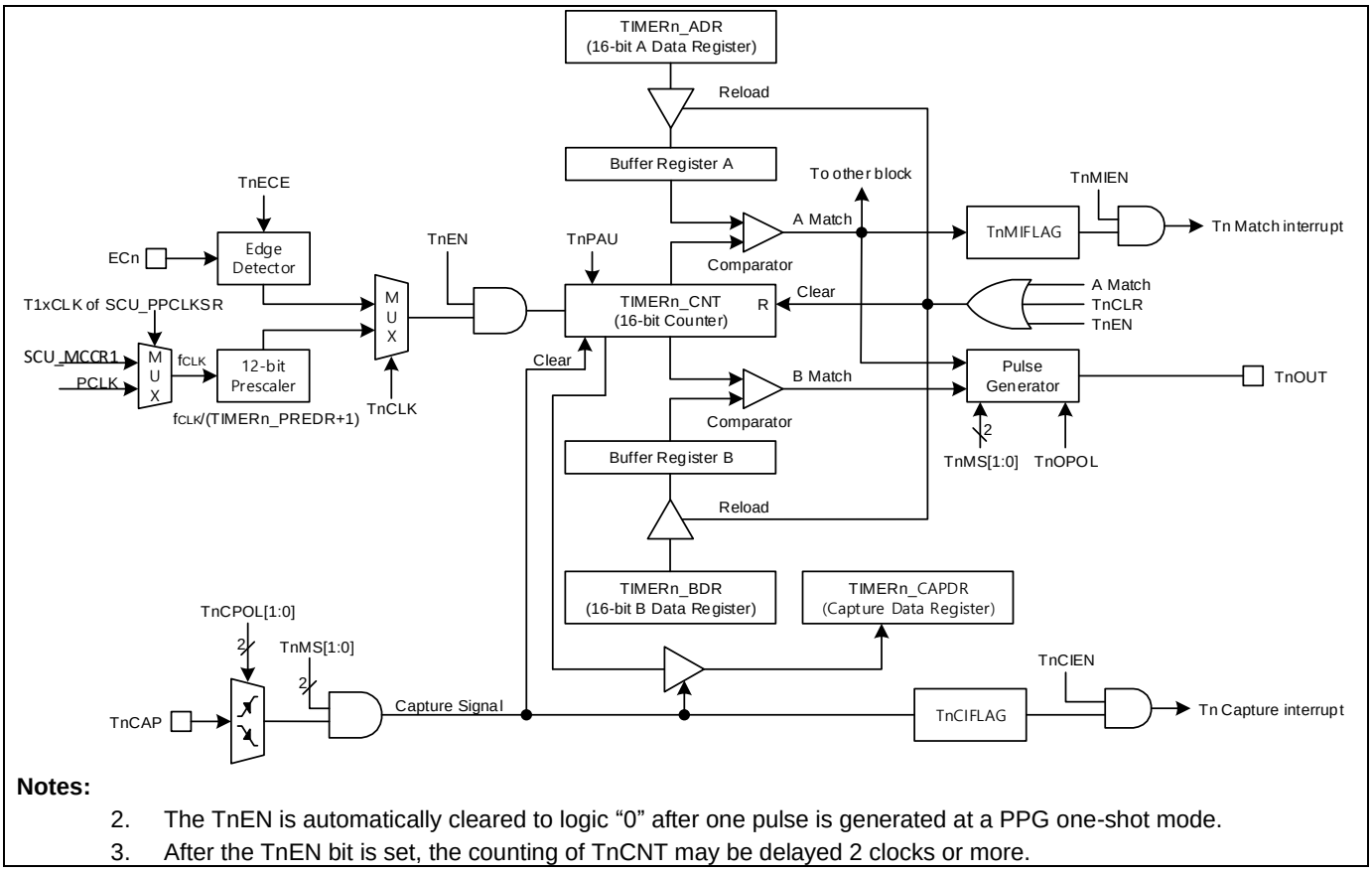
11.1 OVERVIEW

The timer block is consisted with 7 channels of 16 bit General purpose timers. They have independent 16 bit counter and dedicated prescaler feeds counting clock. They can support periodic timer, PWM pulse, one-shot timer and capture mode. They can be synchronized together.

One more optional free-run timer is provided. The main purpose of this timer is a periodical tick timer or a wake-up source.

- 16-bit up-counter
- Periodic timer mode
- One-shot timer mode
- PWM pulse mode
- Capture mode
- 12-bit prescaler
- Synchronous start and clear function

Figure shows the block diagram of a unit timer block.



Notes:

2. The TnEN is automatically cleared to logic “0” after one pulse is generated at a PPG one-shot mode.
3. After the TnEN bit is set, the counting of TnCNT may be delayed 2 clocks or more.

Figure 11.1 Block diagram

11.2 Pin Description

Table 11.1 External pin (n = 10, 11, 12, 13, 14, 15 and 16)

PIN NAME	TYPE	DESCRIPTION
ECn	I	Timer 1n External clock input
TnC	I	Timer 1n Capture input
TnO	O	Timer 1n Output

11.3 REGISTERS

Base addresse of 16-Bit Timer is as below.

Table 11.1 Base Address of each channel

NAME	BASE ADDRESS
TIMER10	0x4000_2100
TIMER11	0x4000_2200
TIMER12	0x4000_2300
TIMER13	0x4000_2700
TIMER14	0x4000_2800
TIMER15	0x4000_2900
TIMER16	0x4000_2A00

Table 11.2 Timer Register Map

Register Name	Offset	Access Type	Description	Initial Value	Ref
TIMERn_CR	0x00	RW	Timer/Counter n Control Register	0x0000_0000	11.3.1
TIMERn_ADR	0x04	RW	Timer/Counter n A Data Register	0x0000_FFFF	11.3.2
TIMERn_BDR	0x08	RW	Timer/Counter n B Data Register	0x0000_FFFF	11.3.3
TIMERn_CAPDR	0x0C	RO	Timer/Counter n Capture Data Register	0x0000_0000	11.3.4
TIMERn_PREDR	0x10	RW	Timer/Counter n Prescaler Data Register	0x0000_0FFF	11.3.5
TIMERn_CNT	0x14	RO	Timer/Counter n Counter Register	0x0000_0000	11.3.6

Note: Where n = 10, 11, 12, 13, 14, 15 and 16.

11.3.1 TIMERn_CR Timer/Counter n Control Register

Timer/Counter n Control Register is 32-bit register.

Timer module should be configured properly before running. When target purpose is defined, the timer can be configured in the TIMERn_CR register

After configuring this register, you can start or stop the timer fuction by TIMERn_CR register.

This Register is able to 32/16/8-bit access. (n = 10, 11, 12, 13, 14, 15 and 16)

TIMER10_CR=0x4000_2100, TIMER11_CR=0x4000_2200, TIMER12_CR=0x4000_2300
TIMER13_CR=0x4000_2700, TIMER14_CR=0x4000_2800, TIMER15_CR=0x4000_2900, TIMER16_CR=0x4000_2A00

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																TnEN	TnCLK	TnMS		TnECE	Reserved		TnOPOL	TnCPOL		TnMIEN	TnCIEN	TnMIFLAG	TnCIFLAG	TnPAU	TnCLR
-																0	0	00		0	-		0	00		0	0	0	0	0	0
-																RW	RW	RW		RW	-		RW	RW		RW	RW	RW	RW	RW	RW

15	TnEN	Timer n Operation Enable bit.
		0 Disable timer n operation.
		1 Enable timer n operation. (Counter clear and start)
14	TnCLK	Timer n Clock Selection bit.
		0 Select an internal prescaler clock.
		1 Select an external clock.
		Note) 1. This bit should be changed during TnEN bit is “0b”.
13 12	TnMS	Timer n Operation Mode Selection bits.
		00 Timer/Counter mode. (TnOUT: toggle at A-match)
		01 Capture mode. (The A-match interrupt can occur)
		10 PPG one-shot mode. (TnOUT: Programmable pulse output)
		11 PPG repeat mode. (TnOUT: Programmable pulse output)
		Note) 1. This bit should be changed during TnEN bit is “0b”.
11	TnECE	Timer n External Clock Edge Selection bit.
		0 Select falling edge of external clock.
		1 Select rising edge of external clock.
8	TnOPOL	TnOUT Polarity Selection bit.
		0 Start high. (TnOUT is low level at disable)
		1 Start low. (TnOUT is high level at disable)
7 6	TnCPOL	Timer n Capture Polarity Selection bits.
		00 Capture on falling edge.
		01 Capture on rising edge.
		10 Capture on both of falling and rising edge.
		11 Reserved.
5	TnMIEN	Timer n Match Interrupt Enable bit.
		0 Disable timer n match interrupt.
		1 Enable timer n match interrupt.
4	TnCIEN	Timer n Capture Interrupt Enable bit.
		0 Disable timer n capture interrupt.
		1 Enable timer n capture interrupt.
3	TnMIFLAG	Timer n Match Interrupt Flag bit.
		0 No request occurred.
		1 Request occurred, This bit is cleared to ‘0’ when write ‘1’.

2	TnCIFLAG	Timer n Capture Interrupt Flag bit.	
		0	No request occurred.
		1	Request occurred, This bit is cleared to ‘0’ when write ‘1’.
1	TnPAU	Timer n Counter Temporary Pause Control bit.	
		0	Continue counting.
		1	Temporary pause.
0	TnCLR	Timer n Counter and Prescaler Clear bit.	
		0	No effect.
		1	Clear timer n counter and prescaler. (Automatically cleared to “0b” after operation)

11.3.2 TIMERn_ADR Timer/Counter n A Data Register

Timer/Counter n A Data Register is 32-bit register. This Register is able to 32/16/8-bit access. (n = 10, 11, 12, 13, 14, 15 and 16)

TIMER10_ADR=0x4000_2104, TIMER11_ADR =0x4000_2204, TIMER12_ADR =0x4000_2304
TIMER13_ADR =0x4000_2704, TIMER14_ADR =0x4000_2804, TIMER15_ADR =0x4000_2904, TIMER16_ADR =0x4000_2A04

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																ADATA															
-																0xFFFF															
-																RW															

15 0	ADATA	Timer/Counter n A Data bits. The range is 0x0002 to 0xFFFF. Note) 1. Do not write “0000H” in the TnADR register when PPG mode.

11.3.3 TIMERn_BDR Timer/Counter n B Data Register

Timer/Counter n B Data Register is 32-bit register. This Register is able to 32/16/8-bit access. (n = 10, 11, 12, 13, 14, 15 and 16)

TIMER10_BDR=0x4000_2108, TIMER11_BDR =0x4000_2208, TIMER12_BDR =0x4000_2308
TIMER13_BDR =0x4000_2708, TIMER14_BDR =0x4000_2808, TIMER15_BDR =0x4000_2908, TIMER16_BDR =0x4000_2A08

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																BDATA															
-																0xFFFF															
-																RW															

15 0	BDATA	Timer/Counter n B Data bits. The range is 0x0000 to 0xFFFF.

11.3.4 TIMERn_CAPDR Timer/Counter n Capture Data Register

Timer/Counter n Capture Data Register is 32-bit register. This Register is able to 32/16/8-bit access. (n = 10, 11, 12, 13, 14, 15 and 16)

TIMER10_CAPDR=0x4000_210C, TIMER11_CAPDR =0x4000_220C, TIMER12_CAPDR =0x4000_230C
TIMER13_CAPDR=0x4000_270C, TIMER14_CAPDR=0x4000_280C, TIMER15_CAPDR=0x4000_290C,
TIMER16_CAPDR =0x4000_2A0C

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																CAPD															
-																0x0000															
-																RO															

15 0	CAPD	Timer/Counter n Capture Data bits.

11.3.5 TIMERn_PREDR Timer/Counter n Prescaler Data Register

Timer/Counter n Prescaler Data Register is 32-bit register. This Register is able to 32/16/8-bit access. (n = 10, 11, 12, 13, 14, 15 and 16)

TIMER10_PREDR=0x4000_2110, TIMER11_ PREDR =0x4000_2210, TIMER12_PREDR =0x4000_2310
TIMER13_PREDR=0x4000_2710, TIMER14_PREDR=0x4000_2810, TIMER15_PREDR=0x4000_2910,
TIMER16_PREDR =0x4000_2A10

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																				PRED											
-																				0xFFF											
-																				RW											

11 0	PRED	Timer/Counter n Prescaler Data bits.

11.3.6 TIMERn_CNT Timer/Counter n Counter Register

Timer/Counter n Counter Register is 32-bit register. This Register is able to 32/16/8-bit access. (n = 10, 11, 12, 13, 14, 15 and 16)

TIMER10_CNT=0x4000_2114, TIMER11_CNT =0x4000_2214, TIMER12_CNT =0x4000_2314
TIMER13_CNT=0x4000_2714, TIMER14_CNT=0x4000_2814, TIMER15_CNT=0x4000_2914,
TIMER16_CNT =0x4000_2A14

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																CNT															
-																0x0000															
-																RO															

15 0	CNT	Timer/Counter n Counter bits.

11.4 Functional Description

11.4.1 Timer Counter 10/11/12/13/14/15/16

The timer/counter n can be clocked by an internal or an external clock source (Ecn). The clock source is selected by clock selection logic which is controlled by the clock selection bits (TnCLK). (n = 10, 11, 12, 13, 14, 15 and 16)

- TIMER n clock source: {f_{CLK}/(TIMERn_PREDR +1), Ecn

In the capture mode, by TnCAP, the data is captured into input capture data register (TIMERn_CAPDR). Timer n outputs the comparison result between counter and data register through TnOUT port in timer/counter mode. Also Timer n outputs PWM wave form through TnOUT port in the PPG mode.

Table 11.3 Timer n Operating Modes (n = 10, 11,12,13,14,15 and 16/ x = 0 to F)

TnEN	Alternative Mode	TnMS[1:0]	TnPREDR	Timer n
1	Pn_AFSR1 = AF1	00	0xXXX	16-bit Timer/Counter Mode
1	Pn_AFSR1 = AF2	01	0xXXX	16-bit Capture Mode
1	Pn_AFSR1 = AF1	10	0xXXX	16-bit PPG Mode(one-shot mode)
1	Pn_AFSR1 = AF1	11	0xXXX	16-bit PPG Mode(repeat mode)

11.4.2 16-bit Timer/Counter Mode

The 16-bit timer/counter mode is selected by control register as shown in Figure 7.2.

The 16-bit timer has counter and data register. The counter register is increased by internal or External clock input. Timer n can use the input clock with 12-bit prescaler division rates (TIMERn_PREDR) and External Clock (Ecn). When the values of TIMERn_CNT and TIMERn_ADR are identical in timer n, a match signal is generated and the interrupt of Timer n occurs. The TIMERn_CNT values are automatically cleared by match signal. It can be also cleared by software (TnCLR).

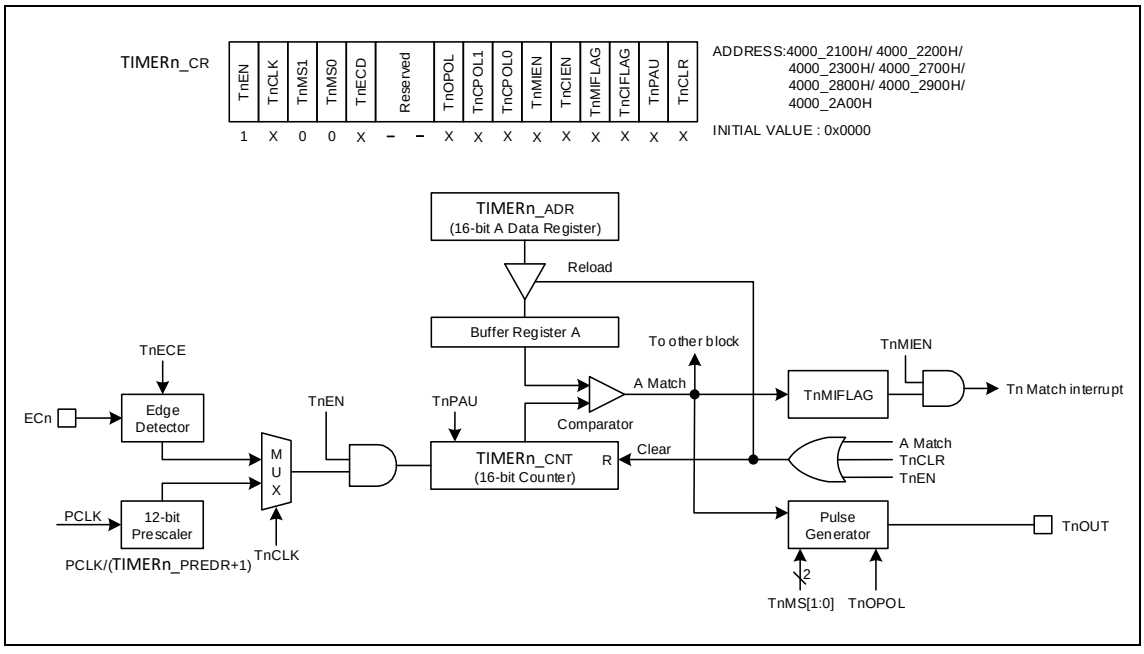


Figure 11.2 16-bit Timer/Counter Mode for Timer n (n = 10, 11,12,13,14,15 and 16)

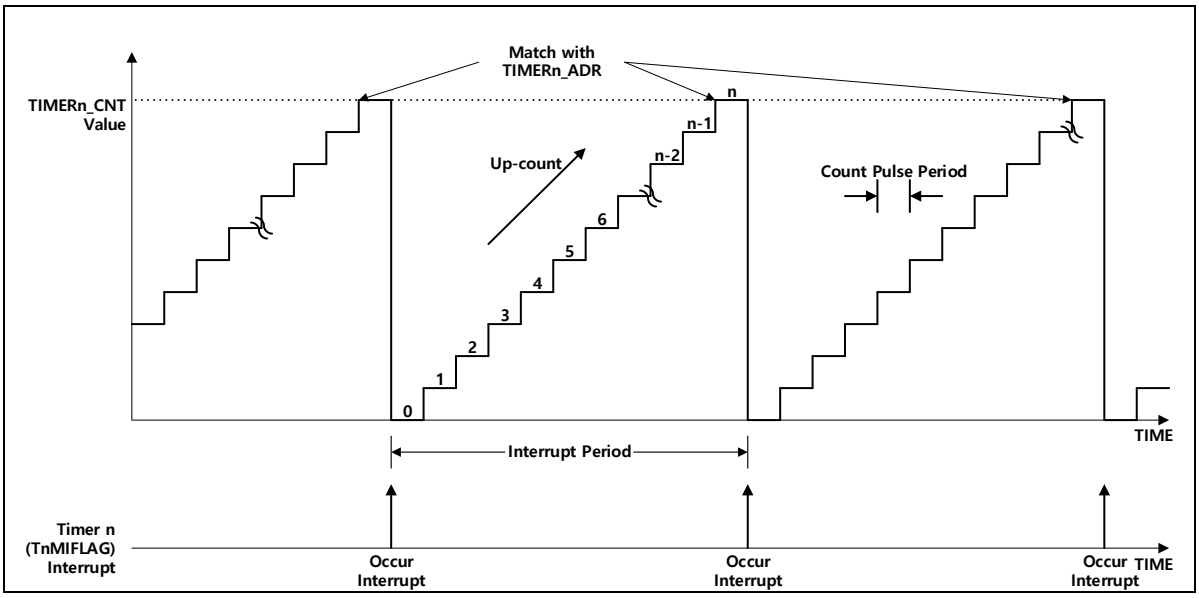


Figure 11.3 16-bit Timer/Counter n Example (n = 10, 11,12,13,14,15 and 16)

11.4.3 16-bit Capture Mode

The timer n capture mode is evoked by setting TnMS[1:0] as '01'. The clock source can use the internal clock. Basically, it has the same function as the 16-bit timer/counter mode and the interrupt occurs when TIMERn_CNT is equal to TIMERn_ADR. TIMERn_CNT values are automatically cleared by match signal and it can be also cleared by software (TnCLR).

This timer interrupt in capture mode is very useful when the pulse width of captured signal is wider than the maximum period of timer.

The capture result is loaded into TnBDR. In the timer n capture mode, timer n output (TnOUT) waveform is not available.

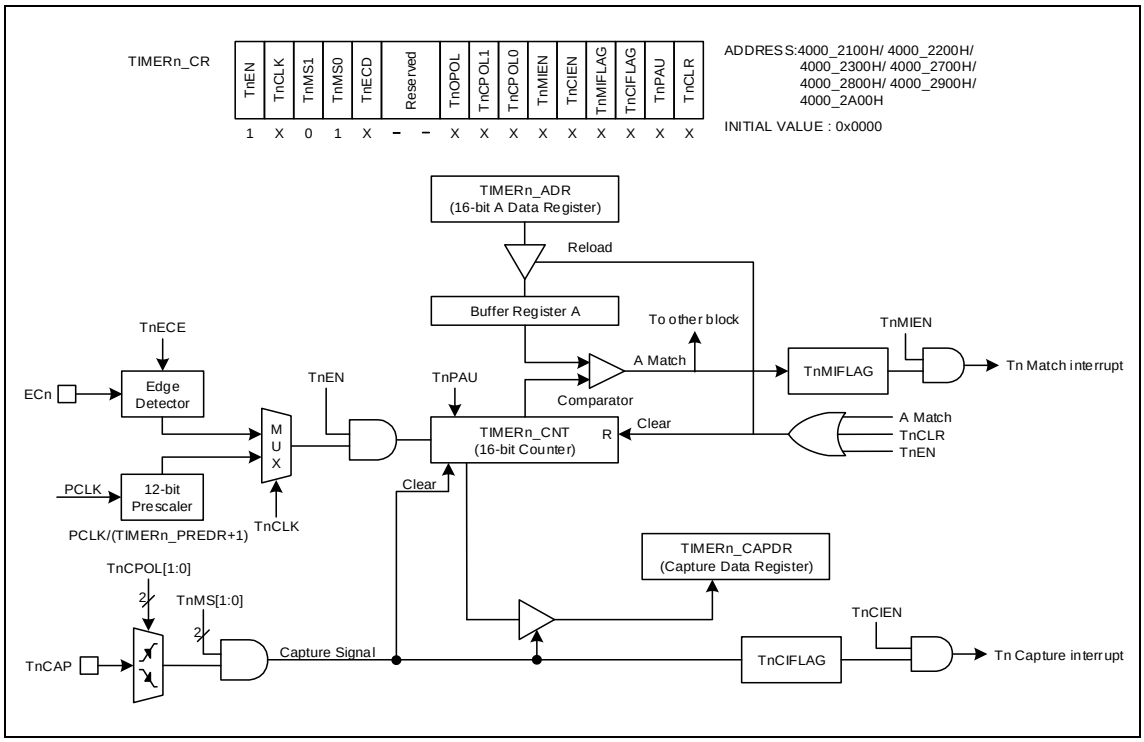


Figure 11.4 16-bit Capture Mode for Timer n (n = 10, 11,12,13,14,15 and 16)

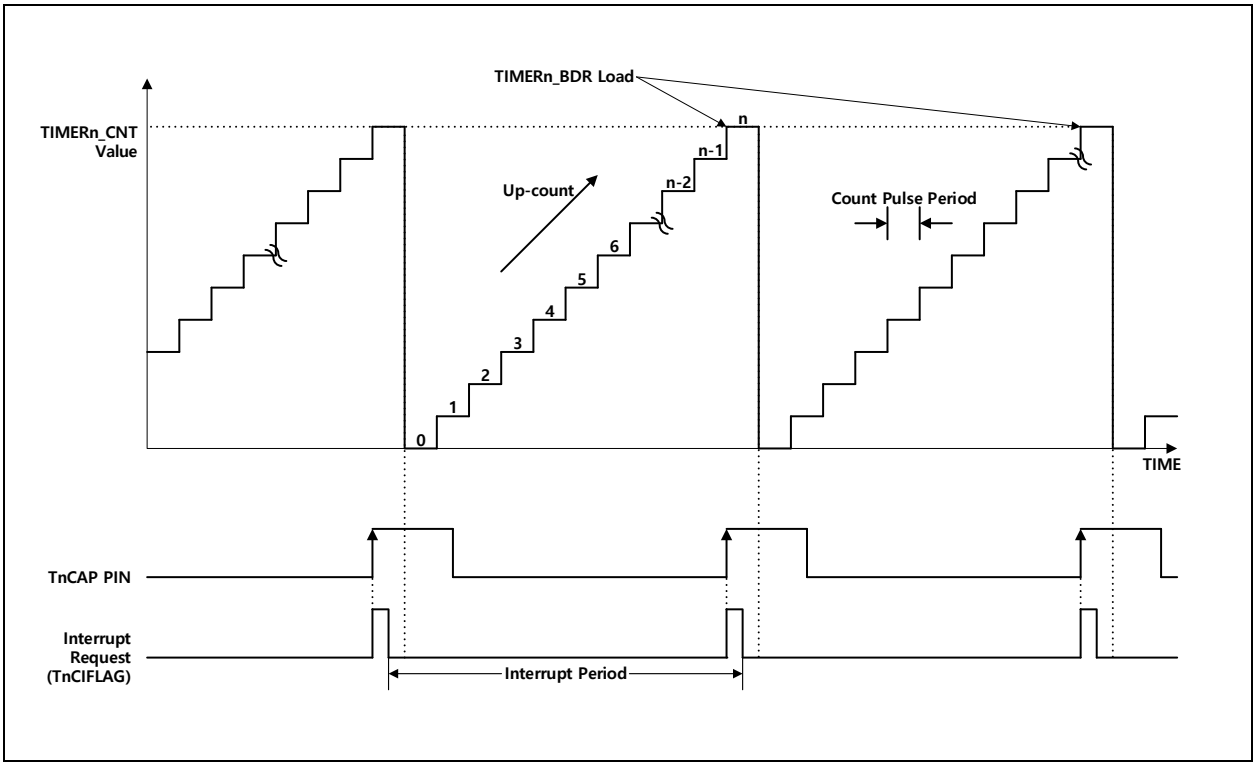


Figure 11.5 16-bit Capture Mode for Timer n (n = 10, 11,12,13,14,15 and 16)

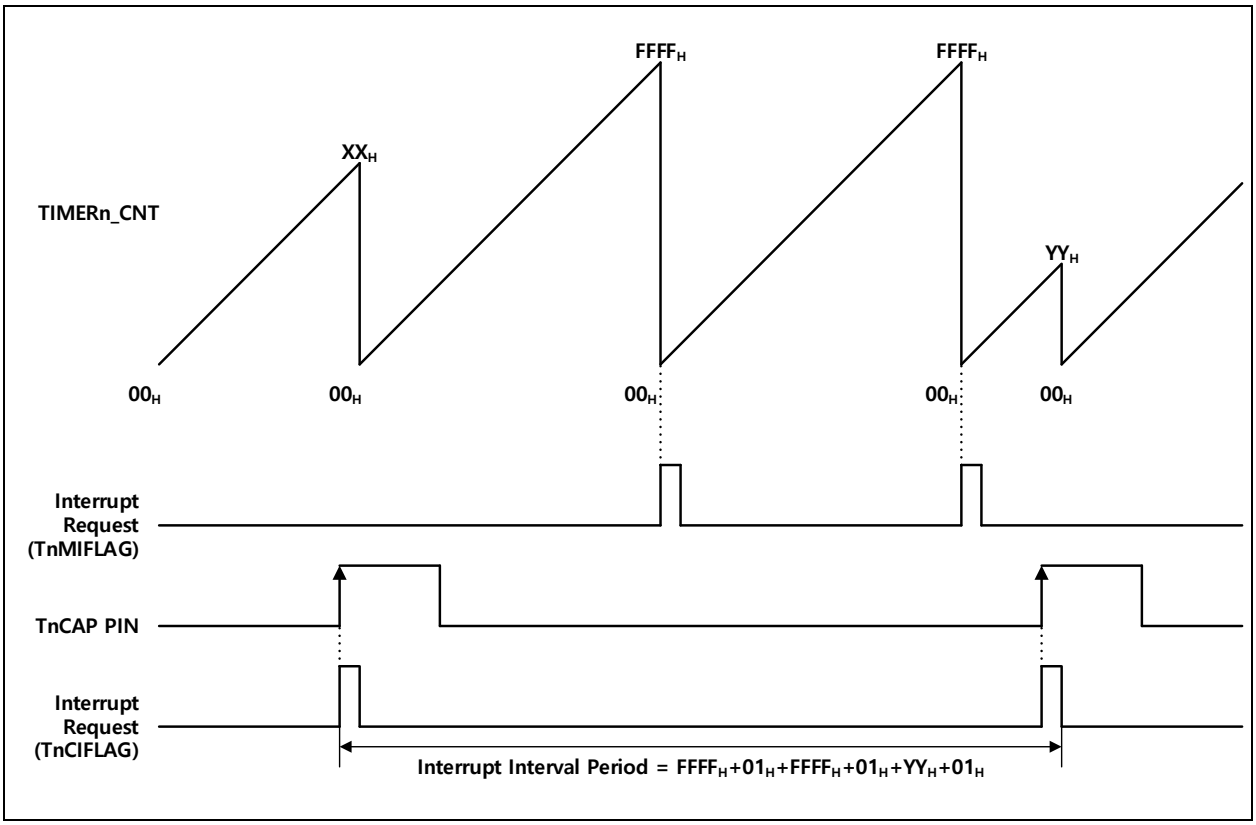
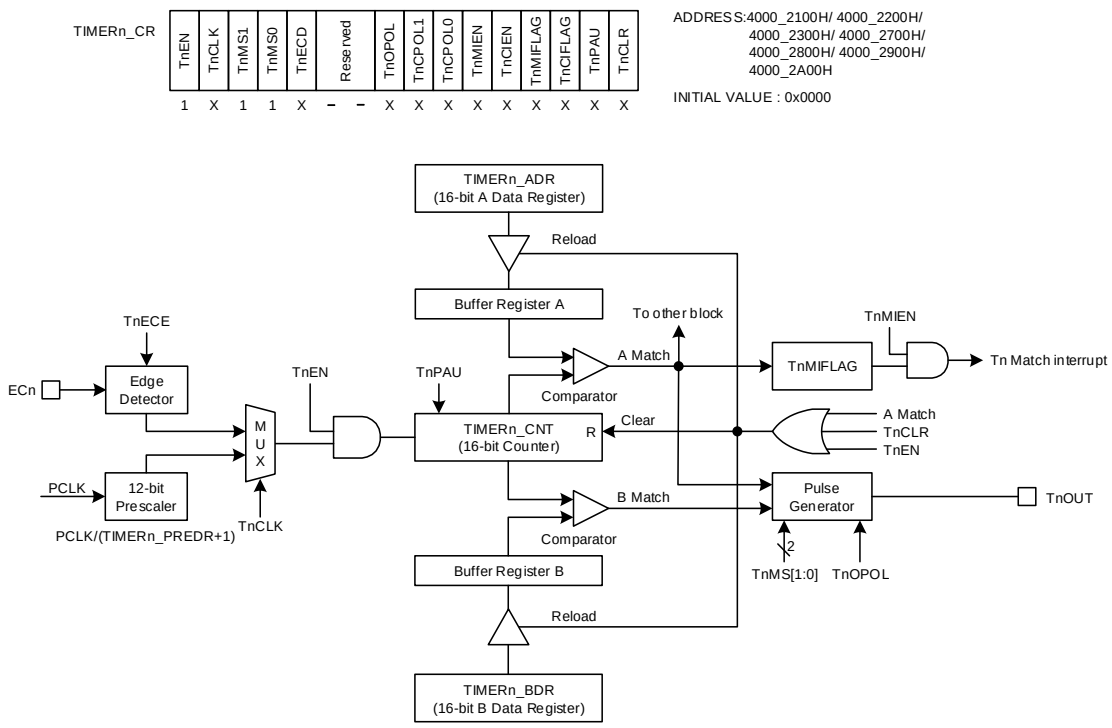


Figure 11.6 Express Timer Overflow in Capture Mode (n = 10, 11,12,13,14,15 and 16)

11.4.4 16-bit PPG Mode

The timer n has a PPG (Programmable Pulse Generation) function. In PPG mode, the TnOUT pin outputs up to 16-bit resolution PWM output. This pin should be configured as a PWM output by set corresponding Pn_AFSR1 to 'AF1'. The period of the PWM output is determined by the TIMERn_ADR. And the duty of the PWM output is determined by the TIMERn_BDR. (x : A to F)



NOTE)

1. The TnEN is automatically cleared to logic "0" after one pulse is generated at a PPG one-shot mode.

Figure 11.7 16-bit Capture Mode for Timer n (n = 10, 11,12,13,14,15 and 16)

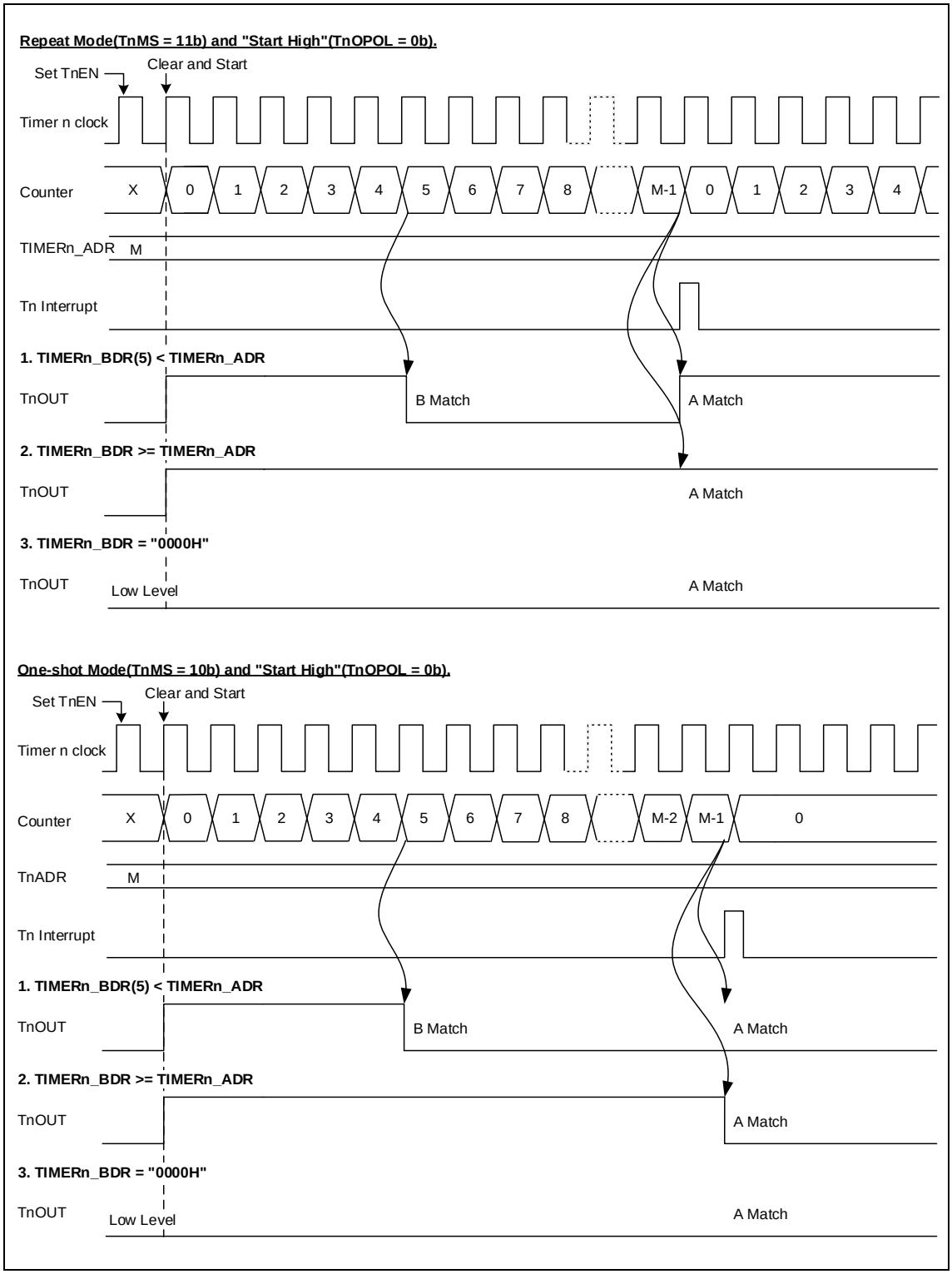


Figure 11.8 16-bit PPG Mode Timming chart for Timer n (n = 10, 11,12,13,14,15 and 16)

CHAPTER 12. 32-BIT TIMER 20

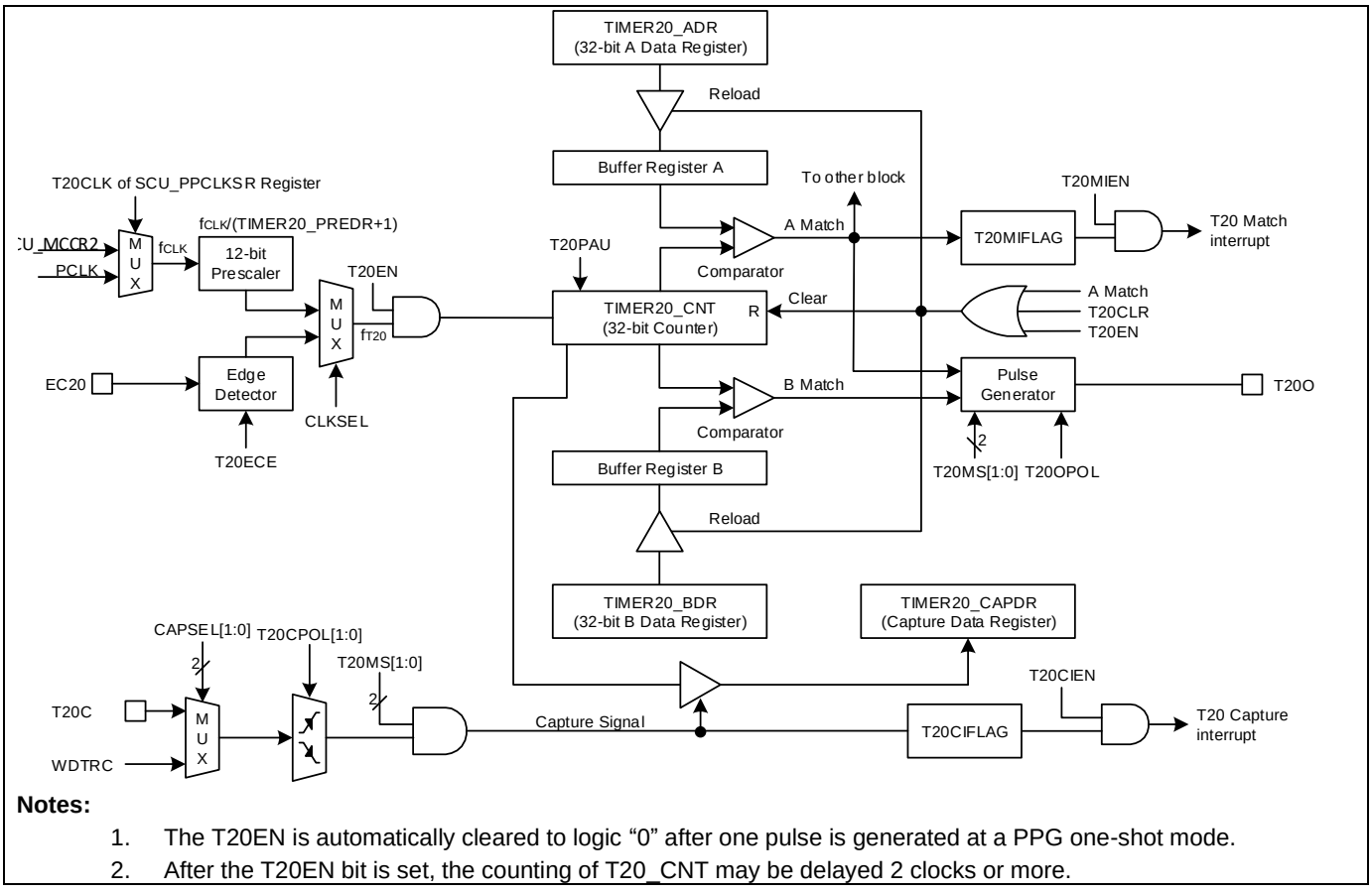
12.1 OVERVIEW

The timer block is consisted with 1 channel of 32 bit General purpose timers. They have independent 32 bit counter and dedicated prescaler feeds counting clock. It supports periodic timer, PWM pulse, one-shot timer and capture mode.

One more optional free-run timer is provided. The main purpose of this timer is a periodical tick timer.

- 32-bit up-counter
- Periodic timer mode
- One-shot timer mode
- PWM pulse mode
- Capture mode
- 12-bit prescaler
- Synchronous start and clear function

Figure shows the block diagram of a unit timer block.



Notes:

1. The T20EN is automatically cleared to logic “0” after one pulse is generated at a PPG one-shot mode.
2. After the T20EN bit is set, the counting of T20_CNT may be delayed 2 clocks or more.

Figure 12.1 Block diagram

12.2 Pin Description

Table 12.1 External pin

PIN NAME	TYPE	DESCRIPTION
EC20	I	External Clock input
T20C	I	Capture input
T20O	O	Timer/PWM/one-shot output

12.3 REGISTERS

Base addresse of 32-Bit Timer 20 is as below.

Table 12.2 Base Address of TIMER20

NAME	BASE ADDRESS
TIMER20	0x4000_2500

Table 12.3 Timer Register Map

Register Name	Offset	Access Type	Description	Initial Value	Ref
TIMER20_CR	0x00	RW	Timer/Counter 20 Control Register	0x0000_0000	12.3.1
TIMER20_ADR	0x04	RW	Timer/Counter 20 A Data Register	0xFFFF_FFFF	12.3.2
TIMER20_BDR	0x08	RW	Timer/Counter 20 B Data Register	0xFFFF_FFFF	12.3.3
TIMER20_CAPDR	0x0C	RO	Timer/Counter 20 Capture Data Register	0x0000_0000	12.3.4
TIMER20_PREDR	0x10	RW	Timer/Counter 20 Prescaler Data Register	0x0000_0FFF	12.3.5
TIMER20_CNT	0x14	RO	Timer/Counter 20 Counter Register	0x0000_0000	12.3.6

12.3.1 TIMER20_CR Timer/Counter 20 Control Register

Timer/Counter 20 Control Register is 32-bit register.

Timer module should be configured properly before running. When target purpose is defined, the timer can be configured in the TIMER20_CR register

After configuring this register, you can start or stop the timer fuction by TIMER20_CR register.

This Register is able to 32/16/8-bit access.

TIMER20_CR=0x4000_2500

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15	14	13 12	11	10 9	8	7 6	5	4	3	2	1	0
Reserved		T20EN	T20CLK	T20MS	T20ECE	CAPSEL	T20OPOL	T20CPOL	T20MIEN	T20CIEN	T20MIFLAG	T20CIFLAG	T20PAU	T20CLR
-		0	0	00	0	00	0	00	0	0	0	0	0	0
-		RW	RW	RW	RW	-	RW	RW	RW	RW	RW	RW	RW	RW

15	T20EN	Timer 20 Operation Enable bit.
	0	Disable timer 20 operation.
	1	Enable timer 20 operation. (Counter clear and start)
14	T20CLK	Timer 20 Clock Selection bit.
	0	Select an internal prescaler clock.
	1	Select an external clock.
	Note) 1. This bit should be changed during T20EN bit is “0b”.	
13 12	T20MS	Timer 20 Operation Mode Selection bits.
	00	Timer/Counter mode. (T20OUT: toggle at A-match)
	01	Capture mode. (The A-match interrupt can occur)
	10	PPG one-shot mode. (T20OUT: Programmable pulse output)
	11	PPG repeat mode. (T20OUT: Programmable pulse output)
	Note) 1. This bit should be changed during T20EN bit is “0b”.	
11	T20ECE	Timer 20 External Clock Edge Selection bit.
	0	Select falling edge of external clock.
	1	Select rising edge of external clock.
10 9	CAPSEL	Timer 20 Capture Signal Selection bits.
	00	Select an external capture signal.
	01	Select the XSOSC (External sub oscillator) signal.
	10	Select the WDTRC (Watch-dog timer RC oscillator) signal.
	11	Not used
	Note) 1. This bit should be changed during T20EN bit is “0b”.	
8	T20OPOL	T20OUT Polarity Selection bit.
	0	Start high. (T20OUT is low level at disable)
	1	Start low. (T20OUT is high level at disable)
7 6	T20CPOL	Timer 20 Capture Polarity Selection bits.
	00	Capture on falling edge.
	01	Capture on rising edge.
	10	Capture on both of falling and rising edge.
	11	Reserved.
5	T20MIEN	Timer 20 Match Interrupt Enable bit.
	0	Disable timer 20 match interrupt.
	1	Enable timer 20 match interrupt.
4	T20CIEN	Timer 20 Capture Interrupt Enable bit.
	0	Disable timer 20 capture interrupt.
	1	Enable timer 20 capture interrupt.
3	T20MIFLAG	Timer 20 Match Interrupt Flag bit.
	0	No request occurred.
	1	Request occurred, This bit is cleared to ‘0’ when write ‘1’.

2	T20CIFLAG	Timer 20 Capture Interrupt Flag bit.	
		0	No request occurred.
		1	Request occurred, This bit is cleared to ‘0’ when write ‘1’.
1	T20PAU	Timer 20 Counter Temporary Pause Control bit.	
		0	Continue counting.
		1	Temporary pause.
0	T20CLR	Timer 20 Counter and Prescaler Clear bit.	
		0	No effect.
		1	Clear timer 20 counter and prescaler. (Automatically cleared to “0b” after operation)

12.3.2 TIMER20_ADR Timer/Counter 20 A Data Register

Timer/Counter 20 A Data Register is 32-bit register. This Register is able to 32/16/8-bit access.

TIMER20_ADR=0x4000_2504

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADATA																															
0xFFFF_FFFF																															
RW																															

15 0	ADATA	Timer/Counter 20 A Data bits. The range is 0x0002 to 0xFFFFFFFF. Note) 1. Do not write “0000H” in the T20ADR register when PPG mode.

12.3.3 TIMER20_BDR Timer/Counter 20 B Data Register

Timer/Counter 20 B Data Register is 32-bit register. This Register is able to 32/16/8-bit access.

TIMER20_BDR=0x4000_2508

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BDATA																															
0xFFFF_FFFF																															
RW																															

15 0	BDATA	Timer/Counter 20 B Data bits. The range is 0x0000 to 0xFFFFFFFF.

12.3.4 TIMER20_CAPDR Timer/Counter 20 Capture Data Register

Timer/Counter 20 Capture Data Register is 32-bit register. This Register is able to 32/16/8-bit access.

TIMER20_CAPDR=0x4000_250C

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CAPD																															
0x0000_0000																															
RO																															

15 0	CAPD	Timer/Counter 20 Capture Data bits.

12.3.5 TIMER20_PREDR Timer/Counter 20 Prescaler Data Register

Timer/Counter 20 Prescaler Data Register is 32-bit register. This Register is able to 32/16/8-bit access.

TIMER20_PREDR =0x4000_2510

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																				PRED											
-																				0xFFF											
-																				RW											

11 0	PRED	Timer/Counter 20 Prescaler Data bits.

12.3.6 TIMER20_CNT Timer/Counter 20 Counter Register

Timer/Counter 20 Counter Register is 32-bit register. This Register is able to 32/16/8-bit access.

TIMER20_CNT=0x4000_2514

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CNT																															
0x0000_0000																															
RO																															

15 0	CNT	Timer/Counter 20 Counter bits.

12.4 Functional Description

12.4.1 Timer Counter 20

The timer/counter 20 can be clocked by an internal or an external clock source (EC20). The clock source is selected by clock selection logic which is controlled by the clock selection bits (T20CLK).

- TIMER 20 clock source: {PCLK/(TIMER20_PREDR +1), EC20

In the capture mode, by TIMER20_CAP, the data is captured into input capture data register (TIMER20_CAPDR). Timer 20 outputs the comparison result between counter and data register through T20OUT port in timer/counter mode. Also Timer 20 outputs PWM wave form through T20OUT port in the PPG mode.

Table 12.4 Timer 20 Operating Modes

T20EN	Alternative Mode	T20MS[1:0]	TIMER20_PREDR	Timer 20
1	PC_AFSR1[3:0] = AF1	00	0xXXX	32-bit Timer/Counter Mode
1	PC_AFSR1[3:0] = AF2	01	0xXXX	32-bit Capture Mode
1	PC_AFSR1[3:0] = AF1	10	0xXXX	32-bit PPG Mode(one-shot mode)
1	PC_AFSR1[3:0] = AF1	11	0xXXX	32-bit PPG Mode(repeat mode)

12.4.2 32-bit Timer/Counter Mode

The 32-bit timer/counter mode is selected by control register as shown in Figure 8.2.

The 32-bit timer has counter and data register. The counter register is increased by internal or External clock input. Timer 20 can use the input clock with 12-bit prescaler division rates (TIMER20_PREDR) and External Clock (EC20). When the values of TIMER20_CNT and TIMER20_ADR are identical in timer 20, a match signal is generated and the interrupt of Timer 20 occurs. The TIMER20_CNT values are automatically cleared by match signal. It can be also cleared by software (T20CLR).

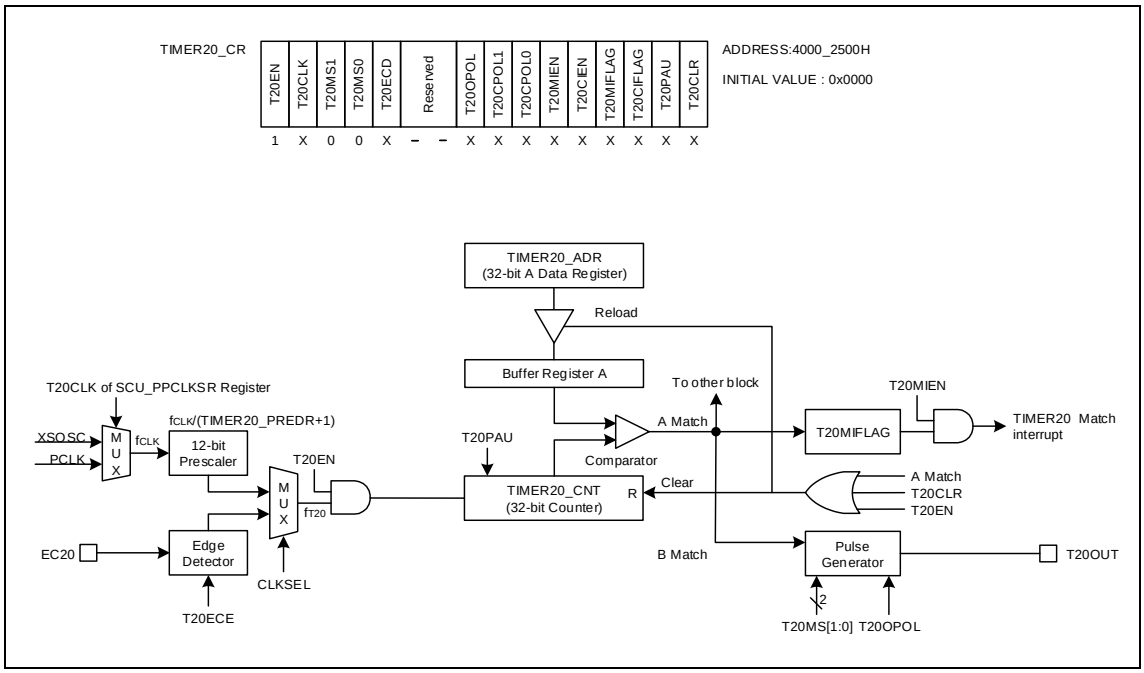


Figure 12.2. 32-bit Timer/Counter Mode for Timer 20

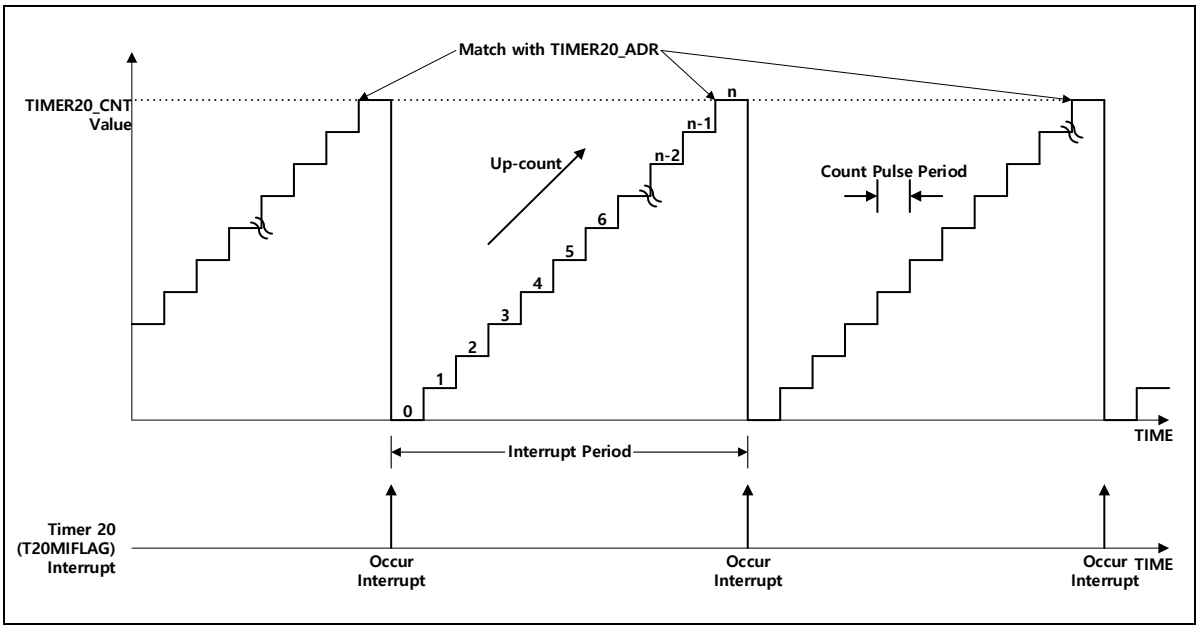


Figure 12.3. 32-bit Timer/Counter 20 Example

12.4.3 32-bit Capture Mode

The timer 20 capture mode is evoked by setting T20MS[1:0] as '01'. The clock source can use the internal clock. Basically, it has the same function as the 32-bit timer/counter mode and the interrupt occurs when TIMER20_CNT is equal to TIMER20_ADR. TIMER20_CNT values are cleared by software (T20CLR).

This timer interrupt in capture mode is very useful when the pulse width of captured signal is wider than the maximum period of timer.

The capture result is loaded into TIMER20_BDR. In the timer 20 capture mode, timer 20 output (T20OUT) waveform is not available.

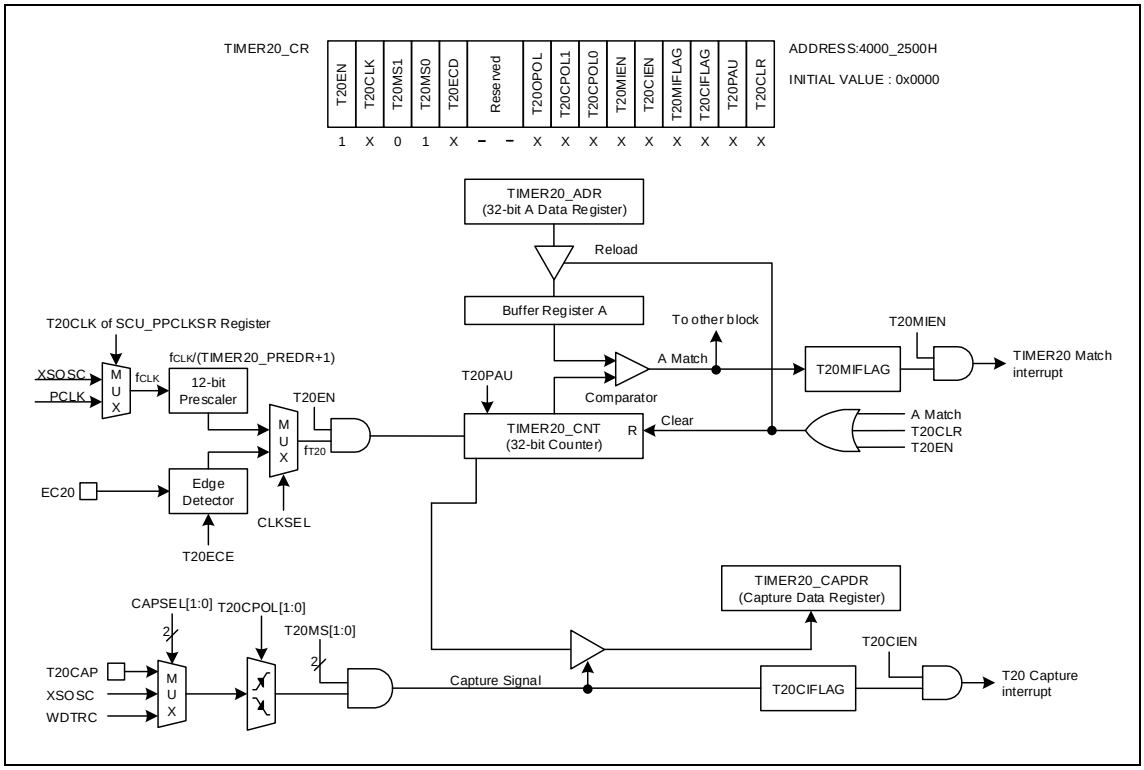


Figure 12.4 32-bit Capture Mode for Timer 20

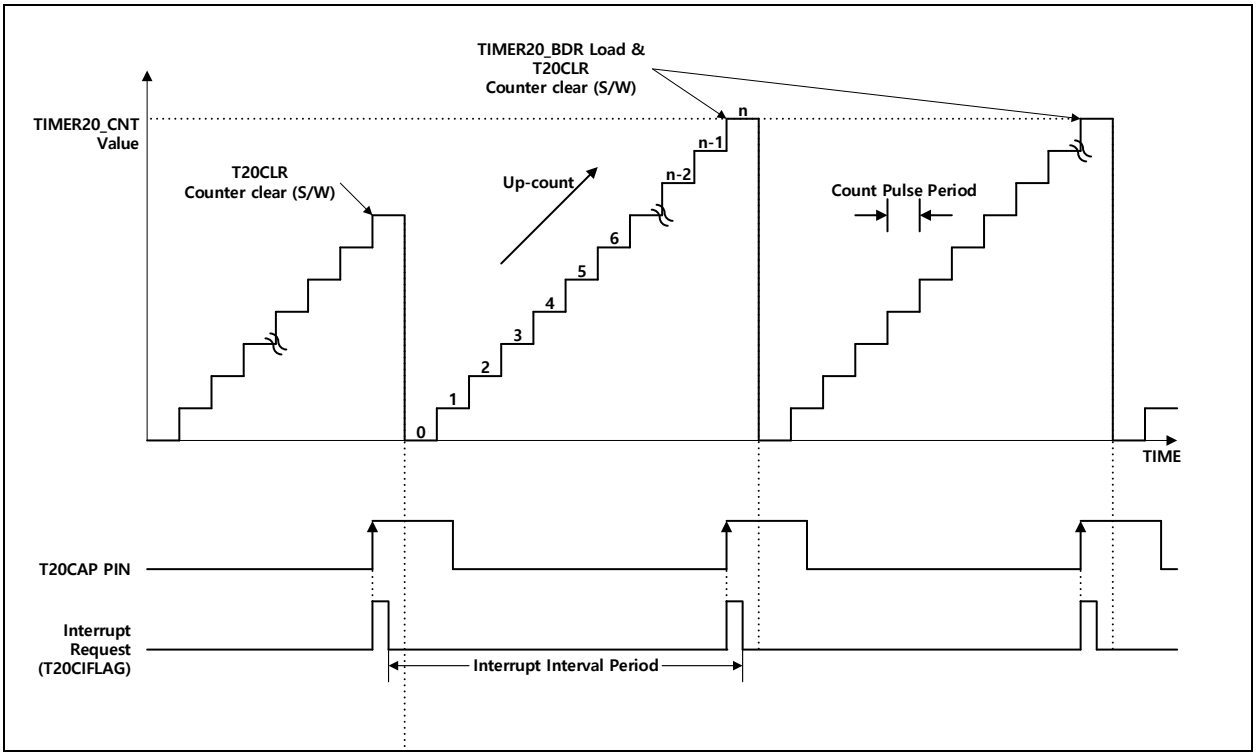


Figure 12.5 32-bit Capture Mode for Timer 20

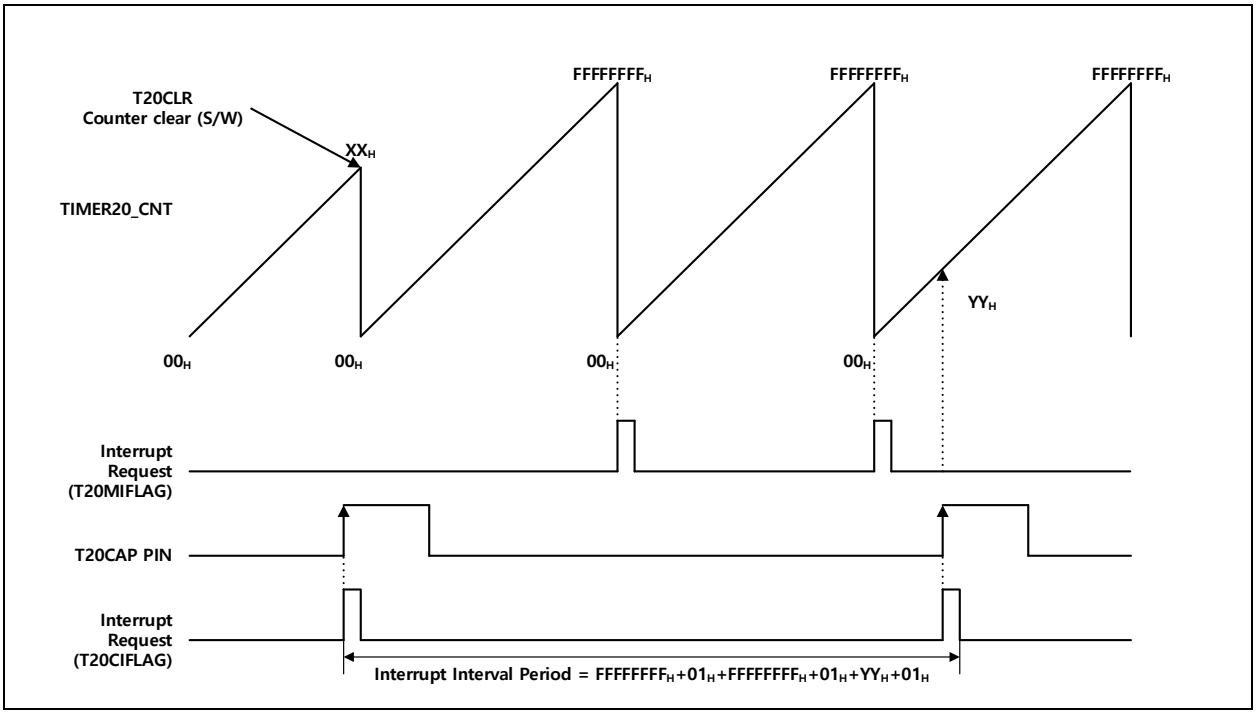
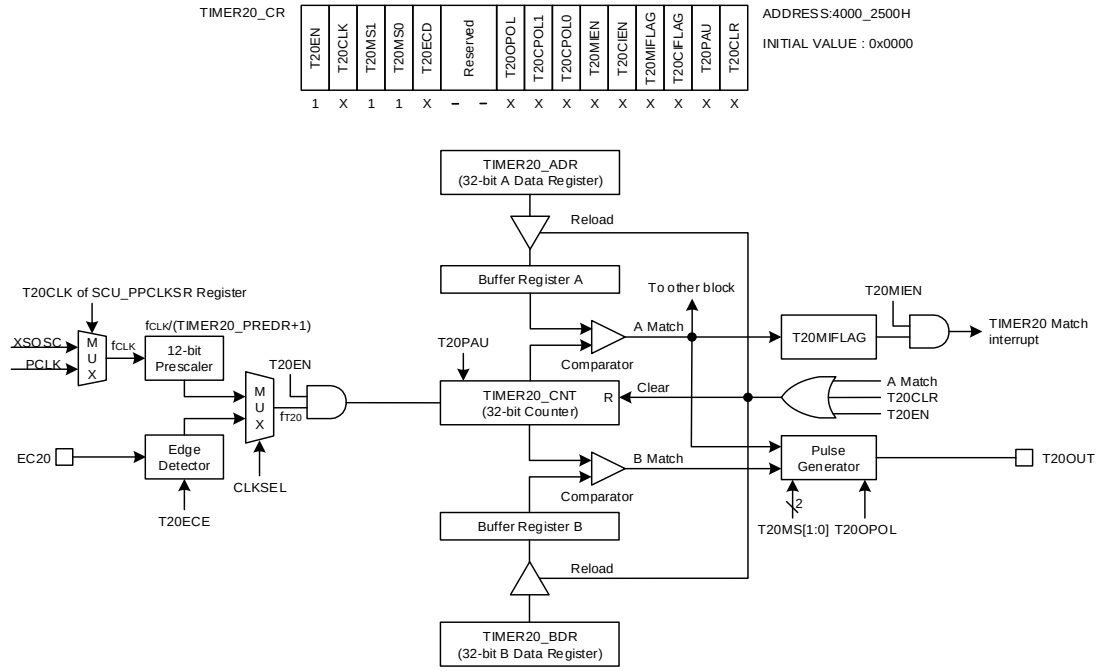


Figure 12.6 Express Timer Overflow in Capture Mode

12.4.4 32-bit PPG Mode

The timer 20 has a PPG (Programmable Pulse Generation) function. In PPG mode, the T20OUT pin outputs up to 32-bit resolution PWM output. This pin should be configured as a PWM output by set PC_AFSR1[3:0] to 'AF1'. The period of the PWM output is determined by the TIMER20_ADR. And the duty of the PWM output is determined by the TIMER20_BDR.



NOTE)

1. The T20EN is automatically cleared to logic "0" after one pulse is generated at a PPG one-shot mode.

Figure 12.7 32-bit Capture Mode for Timer 20

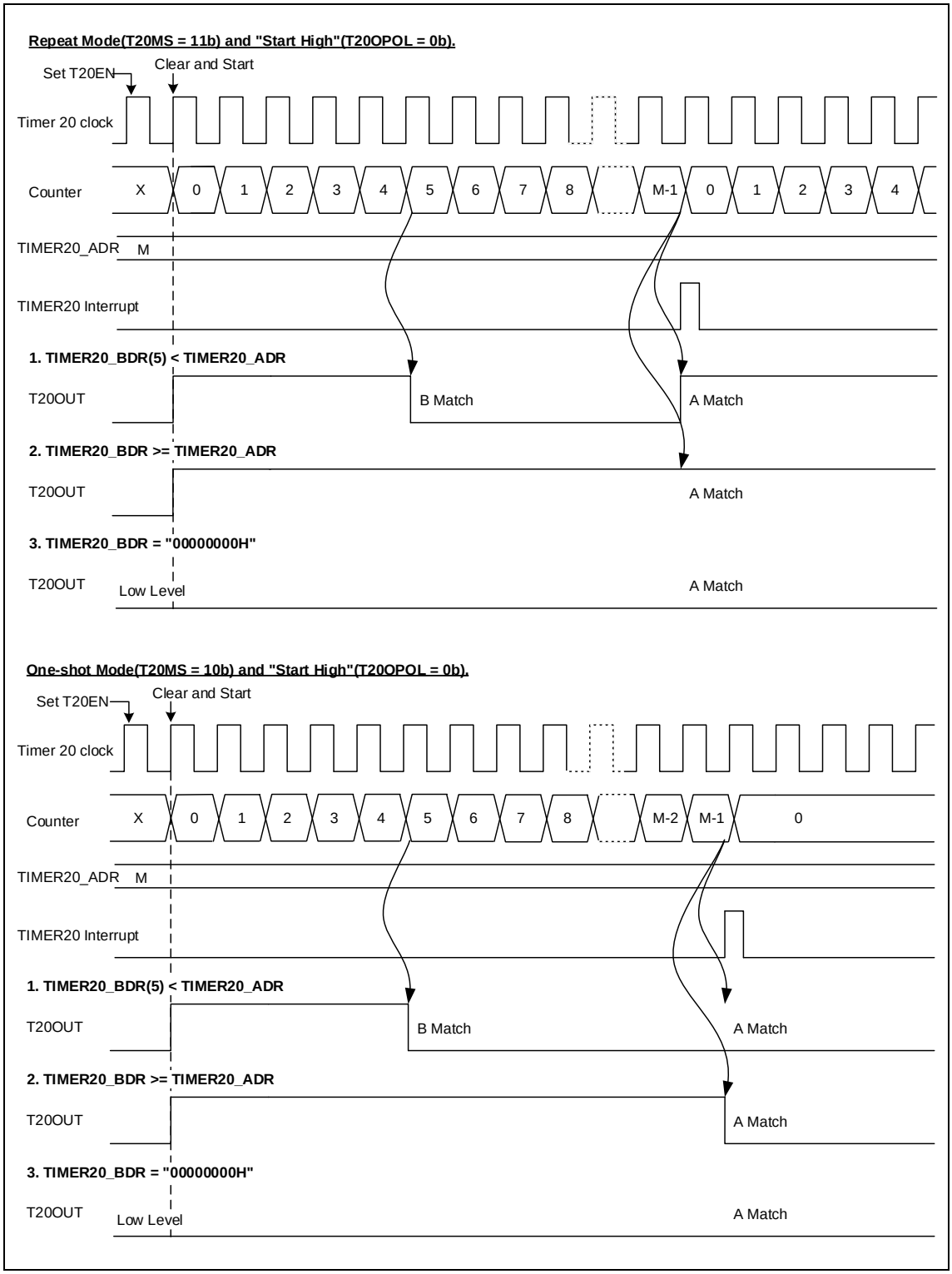


Figure 12.8 32-bit PPG Mode Timming chart for Timer 20

CHAPTER 13. 32-BIT TIMER 21

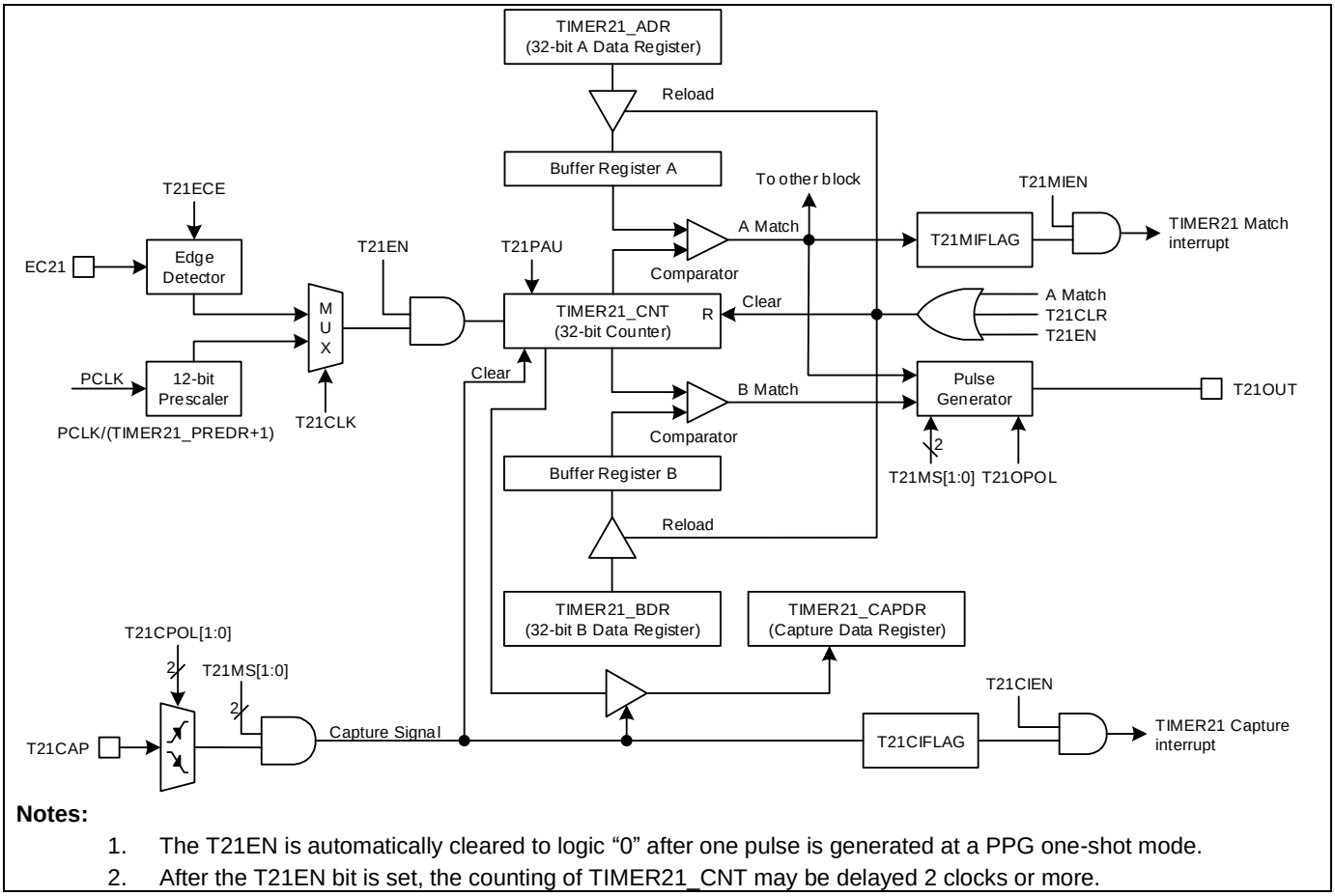
13.1 OVERVIEW

The timer block is consisted with 1 channel of 32 bit General purpose timers. They have independent 32 bit counter and dedicated prescaler feeds counting clock. They can support periodic timer, PWM pulse, one-shot timer and capture mode. They can be synchronized together.

One more optional free-run timer is provided. The main purpose of this timer is a periodical tick timer or a wake-up source.

- 32-bit up-counter
- Periodic timer mode
- One-shot timer mode
- PWM pulse mode
- Capture mode
- 12-bit prescaler
- Synchronous start and clear function

Figure shows the block diagram of a unit timer block.



Notes:

1. The T21EN is automatically cleared to logic “0” after one pulse is generated at a PPG one-shot mode.
2. After the T21EN bit is set, the counting of TIMER21_CNT may be delayed 2 clocks or more.

Figure 13.1 Block diagram

13.2 Pin Description

Table 13.1 External pin

PIN NAME	TYPE	DESCRIPTION
EC21	I	External Clock input
T21C	I	Capture input
T21O	O	Timer/PWM/one-shot output

13.3 REGISTERS

Base addresse of 32-Bit Timer 21 is as below.

Table 13.2 Base Address of T20

NAME	BASE ADDRESS
TIMER21	0x4000_2600

Table 13.3 Timer Register Map

Register Name	Offset	Access Type	Description	Initial Value	Ref
TIMER21_CR	0x00	RW	Timer/Counter 21 Control Register	0x0000_0000	13.3.1
TIMER21_ADR	0x04	RW	Timer/Counter 21 A Data Register	0xFFFF_FFFF	13.3.2
TIMER21_BDR	0x08	RW	Timer/Counter 21 B Data Register	0xFFFF_FFFF	13.3.3
TIMER21_CAPDR	0x0C	RO	Timer/Counter 21 Capture Data Register	0x0000_0000	13.3.4
TIMER21_PREDR	0x10	RW	Timer/Counter 21 Prescaler Data Register	0x0000_0FFF	13.3.5
TIMER21_CNT	0x14	RO	Timer/Counter 21 Counter Register	0x0000_0000	13.3.6

13.3.1 TIMER21_CR Timer/Counter 21 Control Register

Timer/Counter 21 Control Register is 32-bit register.

Timer module should be configured properly before running. When target purpose is defined, the timer can be configured in the TIMER21_CR register

After configuring this register, you can start or stop the timer fuction by TIMER21_CR register.

This Register is able to 32/16/8-bit access.

TIMER21_CR=0x4000_2600

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15	14	13 12	11	10 9	8	7 6	5	4	3	2	1	0
Reserved		T21EN	T21CLK	T21MS	T21ECE	Reserved	T21OPOL	T21CPOL	T21MIEN	T21CIEN	T21MIFLAG	T21CIFLAG	T21PAU	T21CLR
-		0	0	00	0	-	0	00	0	0	0	0	0	0
-		RW	RW	RW	RW	-	RW	RW	RW	RW	RW	RW	RW	RW

15	T21EN	Timer 21 Operation Enable bit.
		0 Disable timer 21 operation.
		1 Enable timer 21 operation. (Counter clear and start)
14	T21CLK	Timer 21 Clock Selection bit.
		0 Select an internal prescaler clock.
		1 Select an external clock.
		Note) 1. This bit should be changed during T21EN bit is “0b”.
13 12	T21MS	Timer 21 Operation Mode Selection bits.
		00 Timer/Counter mode. (T21OUT: toggle at A-match)
		01 Capture mode. (The A-match interrupt can occur)
		10 PPG one-shot mode. (T21OUT: Programmable pulse output)
		11 PPG repeat mode. (T21OUT: Programmable pulse output)
		Note) 1. This bit should be changed during T21EN bit is “0b”.
11	T21ECE	Timer 21 External Clock Edge Selection bit.
		0 Select falling edge of external clock.
		1 Select rising edge of external clock.
8	T21OPOL	T21OUT Polarity Selection bit.
		0 Start high. (T21OUT is low level at disable)
		1 Start low. (T21OUT is high level at disable)
7 6	T21CPOL	Timer 21 Capture Polarity Selection bits.
		00 Capture on falling edge.
		01 Capture on rising edge.
		10 Capture on both of falling and rising edge.
		11 Reserved.
5	T21MIEN	Timer 21 Match Interrupt Enable bit.
		0 Disable timer 21 match interrupt.
		1 Enable timer 21 match interrupt.
4	T21CIEN	Timer 21 Capture Interrupt Enable bit.
		0 Disable timer 21 capture interrupt.
		1 Enable timer 21 capture interrupt.
3	T21MIFLAG	Timer 21 Match Interrupt Flag bit.
		0 No request occurred.
		1 Request occurred, This bit is cleared to ‘0’ when write ‘1’.

2	T21CIFLAG	Timer 21 Capture Interrupt Flag bit.	
		0	No request occurred.
		1	Request occurred, This bit is cleared to ‘0’ when write ‘1’.
1	T21PAU	Timer 21 Counter Temporary Pause Control bit.	
		0	Continue counting.
		1	Temporary pause.
0	T21CLR	Timer 21 Counter and Prescaler Clear bit.	
		0	No effect.
		1	Clear timer 21 counter and prescaler. (Automatically cleared to “0b” after operation)

13.3.2 TIMER21_ADR Timer/Counter 21 A Data Register

Timer/Counter 21 A Data Register is 32-bit register. This Register is able to 32/16/8-bit access.

TIMER21_ADR=0x4000_2604

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADATA																															
0xFFFF_FFFF																															
RW																															

31 0	ADATA	Timer/Counter 21 A Data bits. The range is 0x00000002 to 0xFFFFFFFF. Note) 1. Do not write “0000H” in the T21ADR register when PPG mode.

13.3.3 TIMER21_BDR Timer/Counter 21 B Data Register

Timer/Counter 21 B Data Register is 32-bit register. This Register is able to 32/16/8-bit access.

TIMER21_BDR=0x4000_2608

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BDATA																															
0xFFFF_FFFF																															
RW																															

31 0	BDATA	Timer/Counter 21 B Data bits. The range is 0x00000000 to 0xFFFFFFFF.

13.3.4 TIMER21_CAPDR Timer/Counter 21 Capture Data Register

Timer/Counter 21 Capture Data Register is 32-bit register. This Register is able to 32/16/8-bit access.

TIMER21_CAPDR=0x4000_260C

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CAPD																															
0x0000_0000																															
RO																															

31 0	CAPD	Timer/Counter 21 Capture Data bits.

13.3.5 TIMER21_PREDR Timer/Counter 21 Prescaler Data Register

Timer/Counter 21 Prescaler Data Register is 32-bit register. This Register is able to 32/16/8-bit access.

TIMER21_PREDR =0x4000_2610

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																				PRED											
-																				0xFFF											
-																				RW											

11 0	PRED	Timer/Counter 21 Prescaler Data bits.

13.3.6 TIMER21_CNT Timer/Counter 21 Counter Register

Timer/Counter 21 Counter Register is 32-bit register. This Register is able to 32/16/8-bit access.

TIMER21_CNT=0x4000_2614

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CNT																															
0x0000_0000																															
RO																															

31 0	CNT	Timer/Counter 21 Counter bits.

13.4 Functional Description

13.4.1 Timer Counter 21

The timer/counter 21 can be clocked by an internal or an external clock source (EC21). The clock source is selected by clock selection logic which is controlled by the clock selection bits (T21CLK).

- TIMER 21 clock source: {PCLK/(TIMER21_PREDR +1), EC21

In the capture mode, by T21CAP, the data is captured into input capture data register (TIMER21_CAPDR). Timer 21 outputs the comparison result between counter and data register through T21OUT port in timer/counter mode. Also Timer 21 outputs PWM wave form through T21OUT port in the PPG mode.

Table 13.4 Timer 21 Operating Modes

T21EN	Alternative Mode	T21MS[1:0]	T21PREDR	Timer 21
1	PCAFSR1[7:4]= AF1	00	0xXXX	32-bit Timer/Counter Mode
1	PCAFSR1[7:4] = AF2	01	0xXXX	32-bit Capture Mode
1	PCAFSR1[7:4] = AF1	10	0xXXX	32-bit PPG Mode(one-shot mode)
1	PCAFSR1[7:4] = AF1	11	0xXXX	32-bit PPG Mode(repeat mode)

13.4.2 32-bit Timer/Counter Mode

The 32-bit timer/counter mode is selected by control register as shown in Figure 9.2.

The 32-bit timer has counter and data register. The counter register is increased by internal or External clock input. Timer 21 can use the input clock with 12-bit prescaler division rates (TIMER21_PREDR) and External Clock (EC21). When the values of TIMER21_CNT and TIMER21_ADR are identical in timer 21, a match signal is generated and the interrupt of Timer 21 occurs. The TIMER21_CNT values are automatically cleared by match signal. It can be also cleared by software (T21CLR).

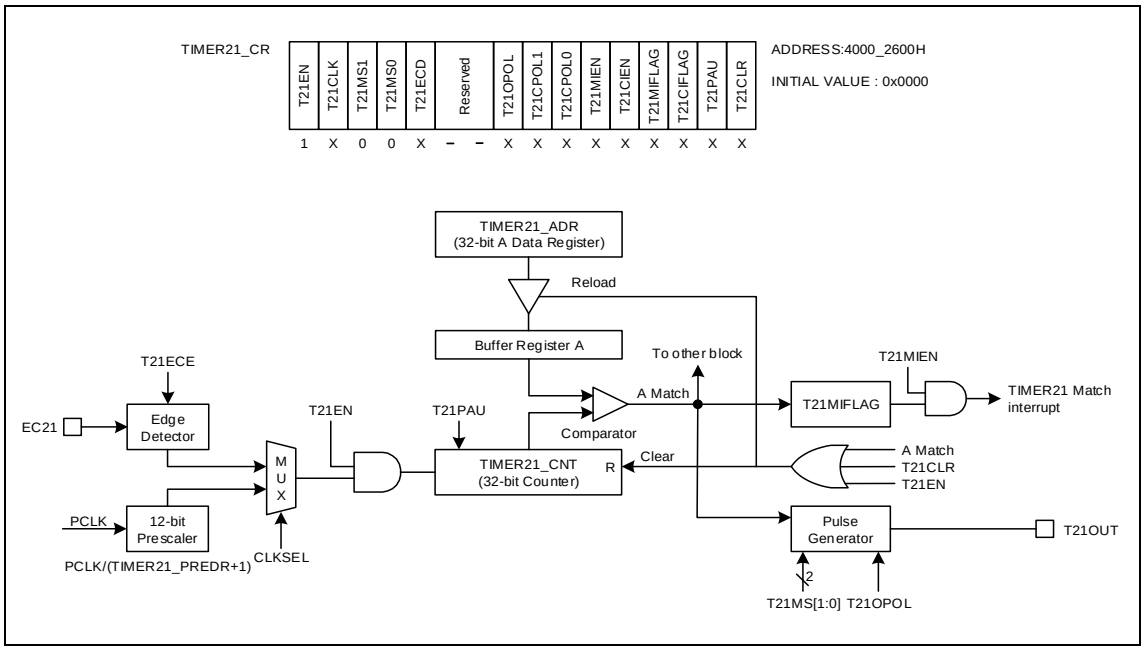


Figure 13.2 32-bit Timer/Counter Mode for Timer 21

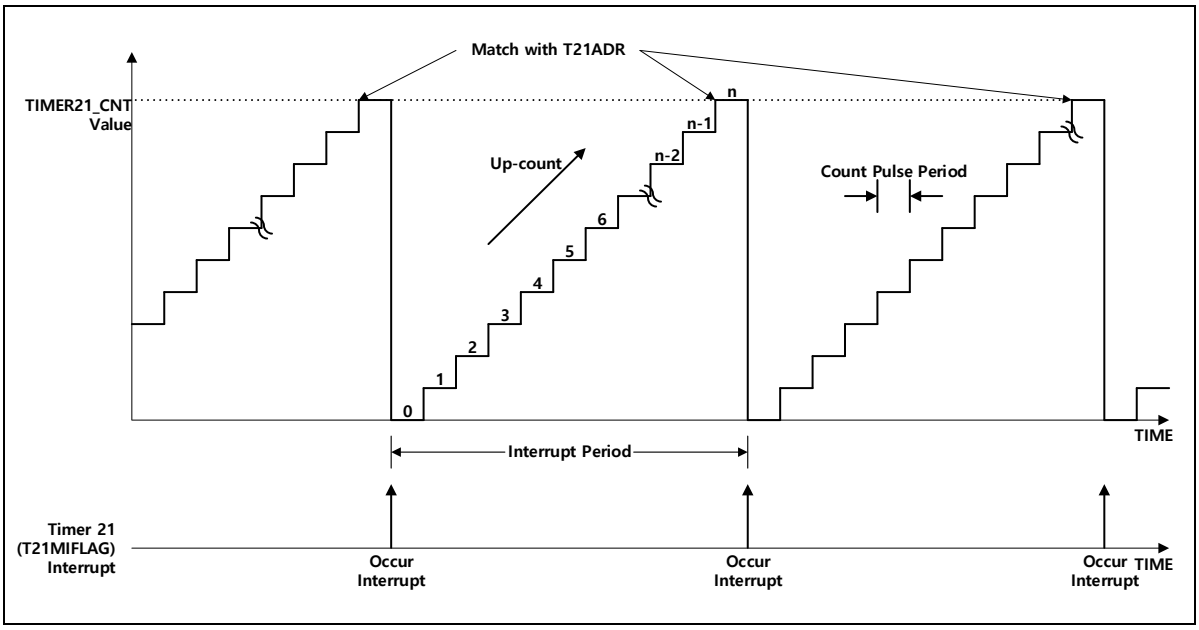


Figure 13.3. 32-bit Timer/Counter 21 Example

13.4.3 32-bit Capture Mode

The timer 21 capture mode is evoked by setting T21MS[1:0] as '01'. The clock source can use the internal clock. Basically, it has the same function as the 32-bit timer/counter mode and the interrupt occurs when TIMER21_CNT is equal to TIMER21_ADR. TIMER21_CNT values are cleared by software (T21CLR).

This timer interrupt in capture mode is very useful when the pulse width of captured signal is wider than the maximum period of timer.

The capture result is loaded into TIMER21_BDR. In the timer 21 capture mode, timer 21 output (T21OUT) waveform is not available.

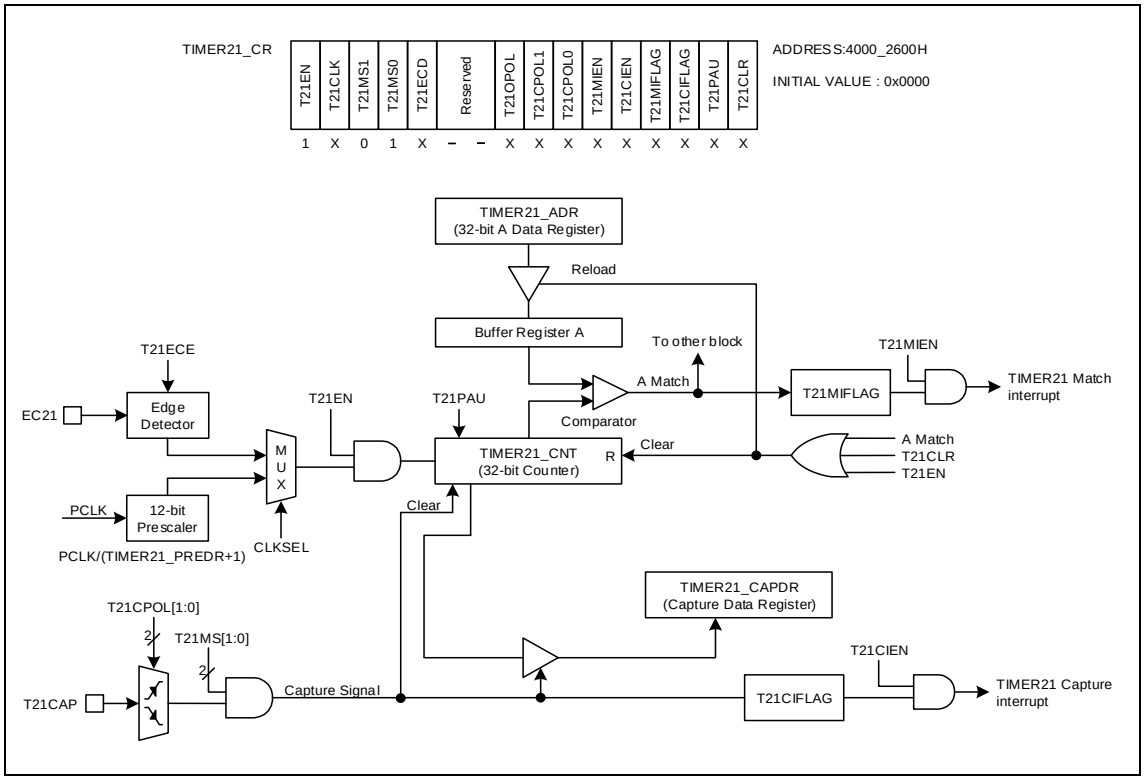


Figure 13.4 32-bit Capture Mode for Timer 21

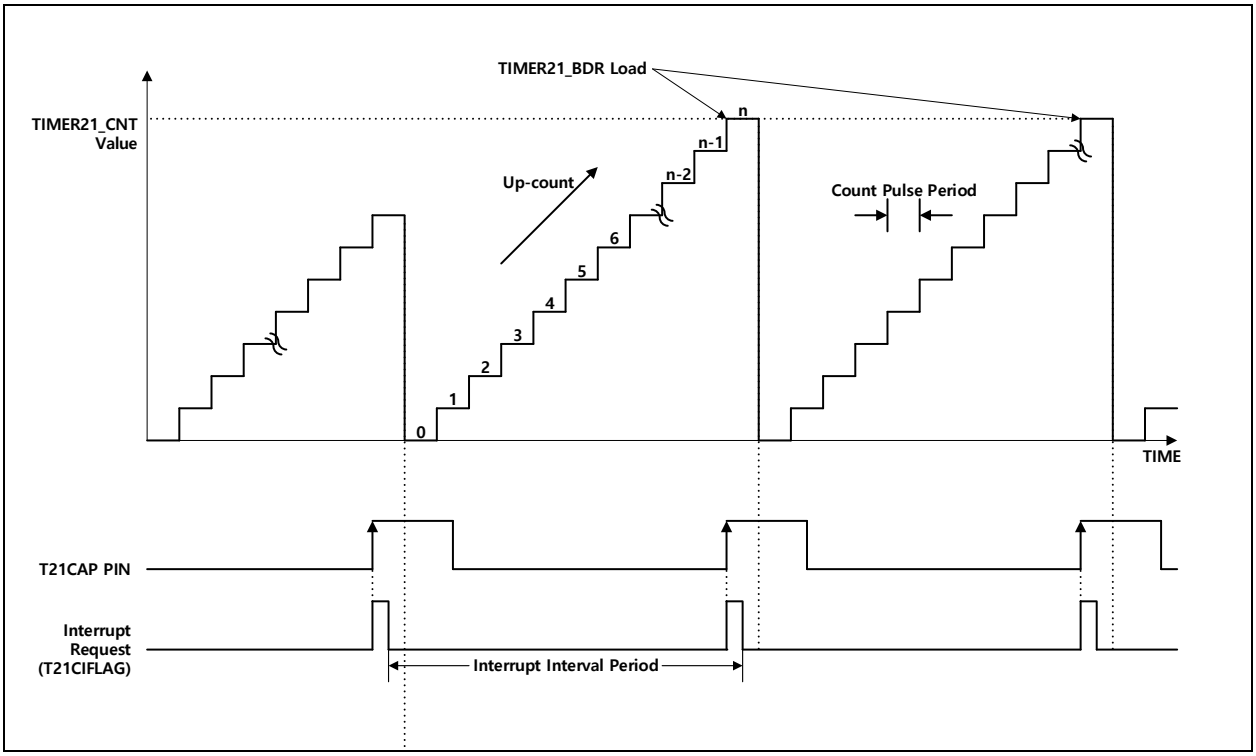


Figure 13.5 32-bit Capture Mode for Timer 21

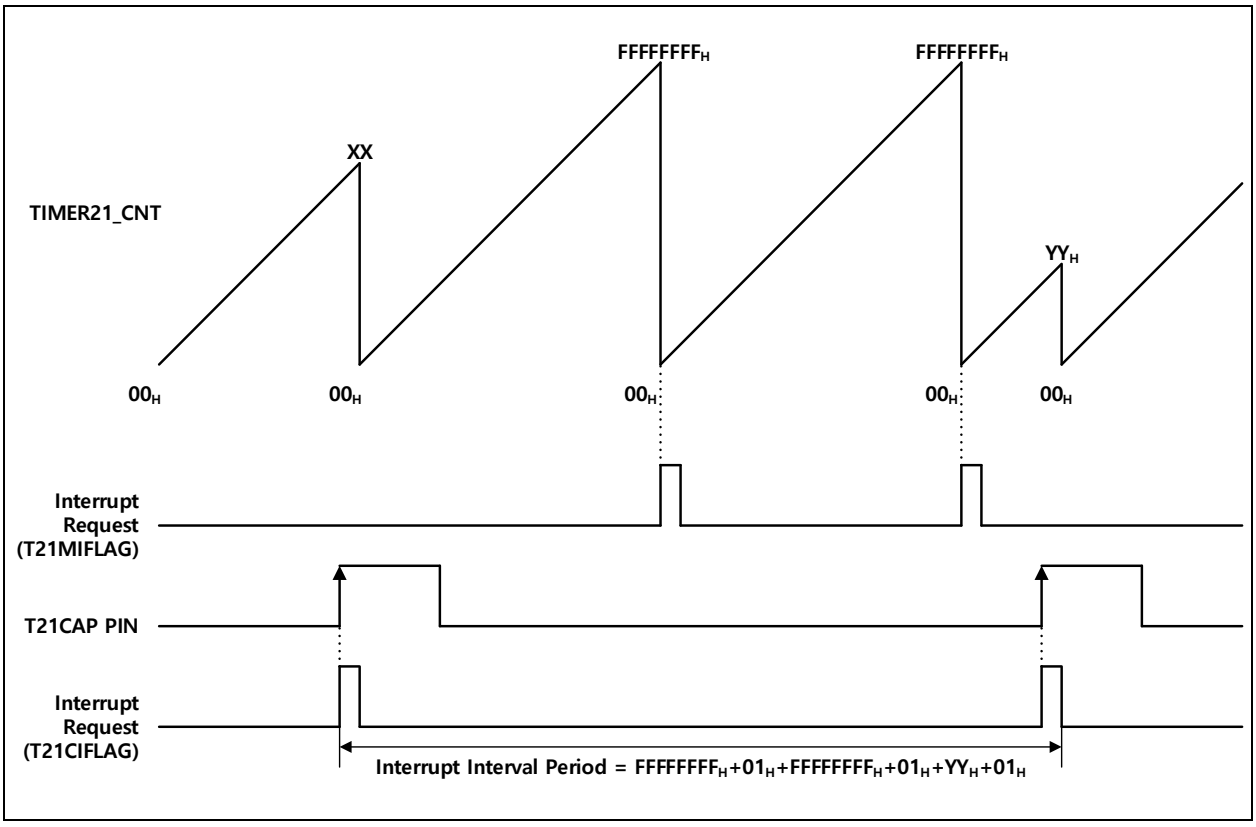
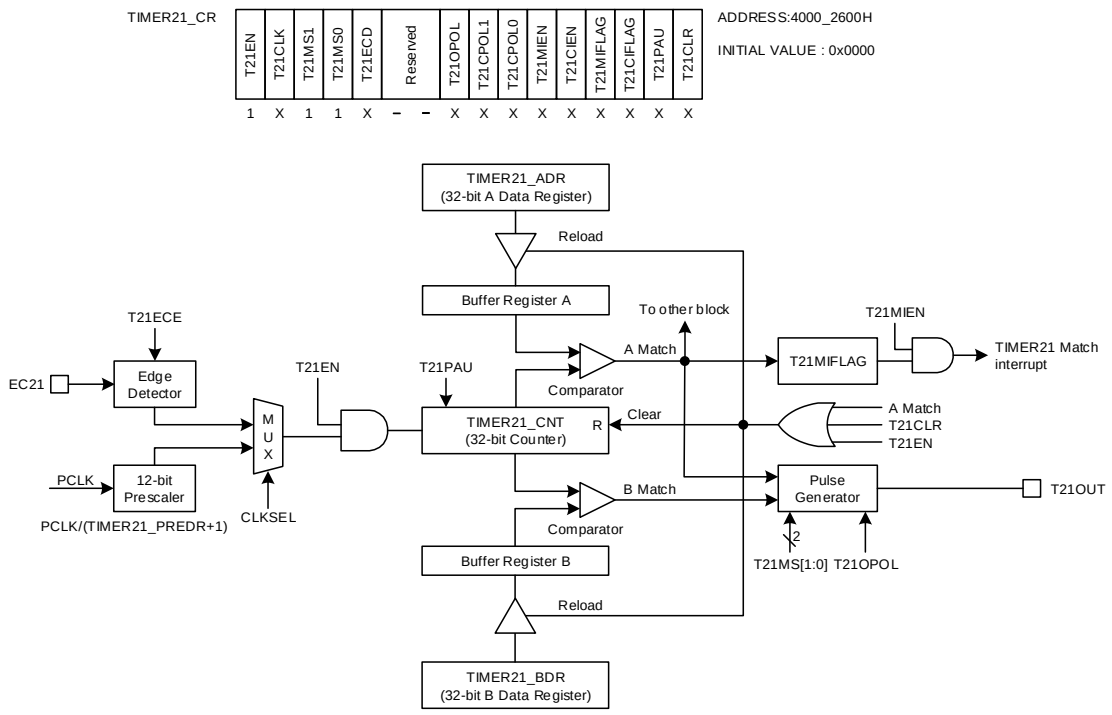


Figure 13.6 Express Timer Overflow in Capture Mode

13.4.4 32-bit PPG Mode

The timer 21 has a PPG (Programmable Pulse Generation) function. In PPG mode, the T21OUT pin outputs up to 32-bit resolution PWM output. This pin should be configured as a PWM output by set PC_AFSR1[7:4] to 'AF1'. The period of the PWM output is determined by the TIMER21_ADR. And the duty of the PWM output is determined by the TIMER21_BDR.



NOTE)

1. The T21EN is automatically cleared to logic "0" after one pulse is generated at a PPG one-shot mode.

Figure 13.7 32-bit Capture Mode for Timer 21

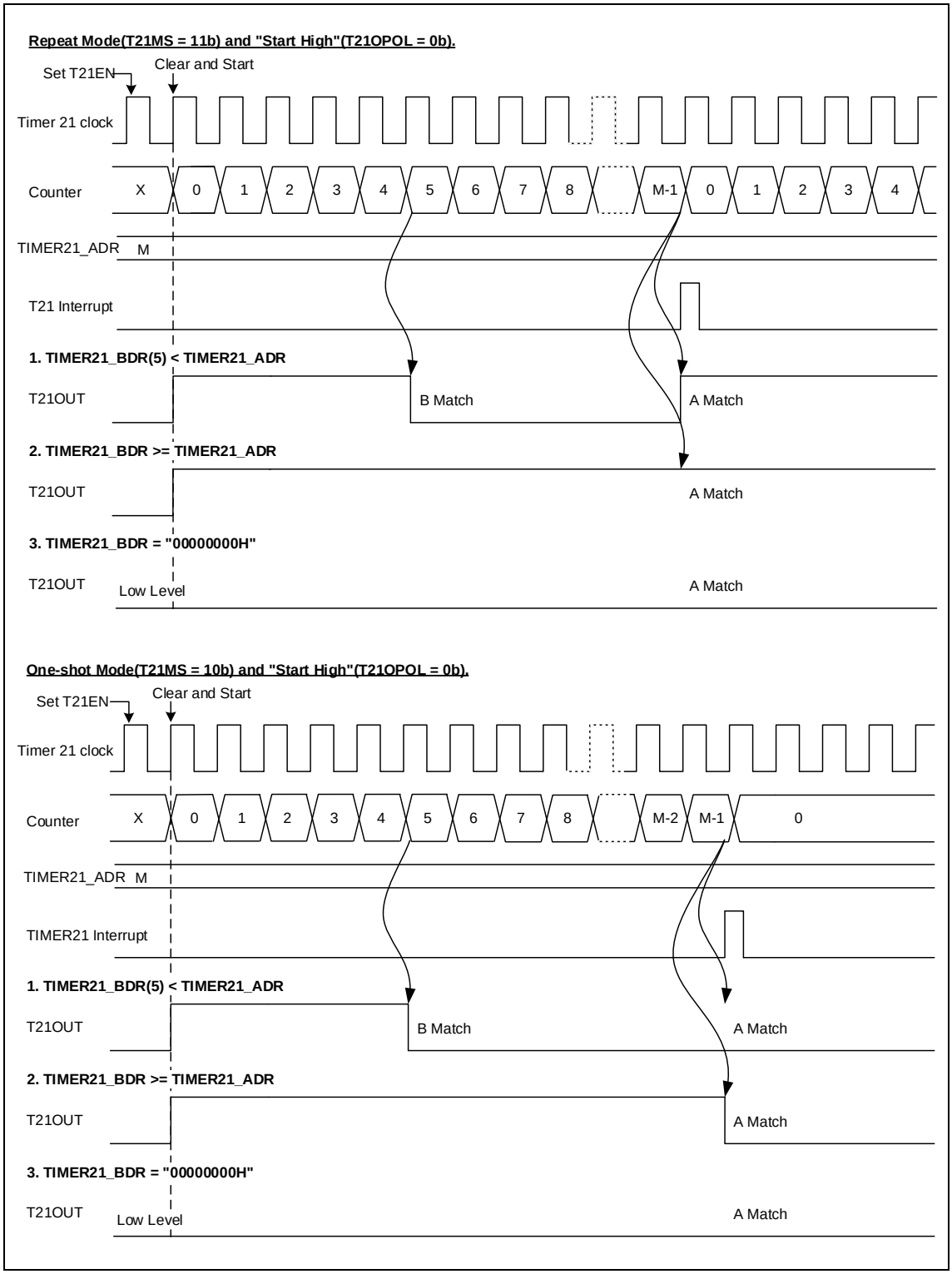


Figure 13.8 32-bit PPG Mode Timming chart for Timer 21

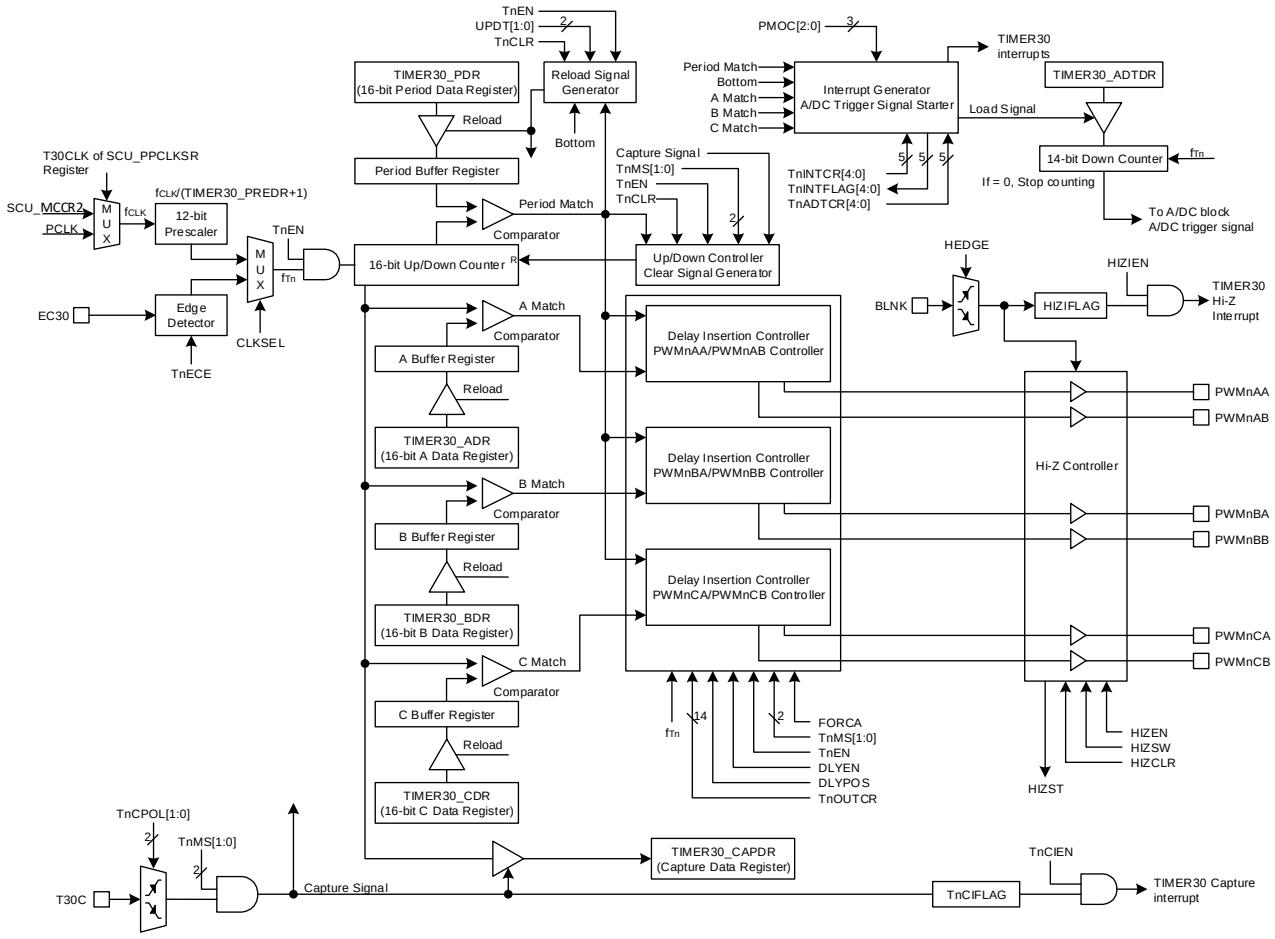
CHAPTER 14. TIMER COUNTER 30

14.1 OVERVIEW

The 16-bit timer 30 module has multiplexer, comparator, 16-bit timer data register A/B/C, 16-bit timer period data register, timer 30 output control register, timer 30 control register, timer 30 PWM output delay register, timer 30 interrupt control register, timer 30 interrupt flag register, timer 30 A/DC trigger control register, timer 30 A/DC trigger generator data register and timer 30 high-Impedance control register (T30ADR, T30BDR, T30CDR, T30PDR, T30OUTCR, T30CR, T30DLY, T30INTCR, T30INTFLAG, T30ADTCR, T30ADTDR, T30HIZCR).

- 16-bit up/down-counter
- Periodic timer mode
- Back-to-Back mode
- Capture mode
- 12-bit prescaler

Figure shows the block diagram of a unit timer block.



Notes:

1. The Period/A/B/C match interrupts except for Bottom can occur in the interval mode.
2. The Period match interrupt only can occur in the capture mode.
3. The 16-bit up/down counter in the capture mode is cleared to “0000H” after the counter value is loaded to the TIMER30_CAPDR register at valid edge.
4. The HIZSW (high-impedance output software setting) bit can be used for debugging mode. That is, All TIMER30 PWM outputs can be high-impedance state with setting the HIZSW bit to ‘1’ by the UI of debugger.
5. After the TnEN bit is set, the counting of TIMER30_CNT may be delayed 2 clocks or more.

Figure 14.1 Block diagram

14.2 Pin Description

Table 14.1 External pin

PIN NAME	TYPE	DESCRIPTION
EC30	I	External clock input
T30C	I	Capture input
BLNK	I	External Sync Signal Input
PWM30AA	O	PWM output
PWM30AB	O	PWM output
PWM30BA	O	PWM output
PWM30BB	O	PWM output
PWM30CA	O	PWM output
PWM30CB	O	PWM output

14.3 REGISTERS

Base addresse of 3-Phase PWM Timer30 is as below.

Table 14.1 Base Address of T30

NAME	BASE ADDRESS
TIMER30	0x4000_2400

Table 14.2 Timer Register Map

Register Name	Offset	Access Type	Description	Initial Value	Ref
TIMER30_CR	0x00	RW	Timer/Counter30 Control Register	0x0000_0000	14.3.1
TIMER30_PDR	0x04	RW	Timer/Counter30 Period Data Register	0x0000_FFFF	14.3.2
TIMER30_ADR	0x08	RW	Timer/Counter30 A Data Register	0x0000_FFFF	14.3.3
TIMER30_BDR	0x0C	RW	Timer/Counter30 B Data Register	0x0000_FFFF	14.3.4
TIMER30_CDR	0x10	RW	Timer/Counter30 C Data Register	0x0000_FFFF	14.3.5
TIMER30_CAPDR	0x14	RO	Timer/Counter30 Capture Data Register	0x0000_0000	14.3.6
TIMER30_PREDR	0x18	RW	Timer/Counter30 Prescaler Data Register	0x0000_0FFF	14.3.7
TIMER30_CNT	0x1C	RO	Timer/Counter30 Counter Register	0x0000_0000	14.3.8
TIMER30_OUTCR	0x20	RW	Timer/Counter30 Output Control Register	0x0000_0000	14.3.9
TIMER30_DLY	0x24	RW	Timer/Counter30 PWM Output Delay Data Register	0x0000_0000	14.3.10
TIMER30_INTCR	0x28	RW	Timer/Counter30 Interrupt Control Register	0x0000_0000	14.3.11
TIMER30_INTFLAG	0x2C	RW	Timer/Counter30 Interrupt Flag Register	0x0000_0000	14.3.12
TIMER30_HIZCR	0x30	RW	Timer/Counter30 High-Impedance Control Register	0x0000_0000	14.3.13
TIMER30_ADTCR	0x34	RW	Timer/Counter30 A/DC Trigger Control Register	0x0000_0000	14.3.14
TIMER30_ADTDR	0x38	RW	Timer/Counter30 A/DC Trigger Generator Data Register	0x0000_0000	14.3.15

14.3.1 TIMER30_CR Timer/Counter 30 Control Register

Timer/Counter30 Control Register is 32-bit register.

Timer module should be configured properly before running. When target purpose is defined, the timer can be configured in the TIMER30_CR register

After configuring this register, you can start or stop the timer fuction by TIMER30_CR register.

This Register is able to 32/16/8-bit access.

TIMER30_CR=0x4000_2400

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15	14	13 12	11	10	9	8	7 6	5 4	3 2 1	0
Reserved		T30EN	T30CLK	T30MS	T30ECE	FORCA	DLYEN	DLYPOS	T30CPOL	UPDT	PMOC	T30CLR
-		0	0	00	0	0	0	0	00	00	000	0
-		RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

15	T30EN	Timer 30 Operation Enable bit.
	0	Disable timer 30 operation.
	1	Enable timer 30 operation. (Counter clear and start)
14	T30CLK	Timer 30 Clock Selection bit.
	0	Select an internal prescaler clock.
	1	Select an external clock.
	Note) 1. This bit should be changed during T30EN bit is “0b”.	
13 12	T30MS	Timer 30 Operation Mode Selection bits.
	00	Interval mode. (All match interrupts can occur)
	01	Capture mode. (The Period-match interrupt can occur)
	10	Back-to-back mode. (All interrupts can occur)
	11	Not used.
	Note) 1. This bit should be changed during T30EN bit is “0b”.	
11	T30ECE	Timer 30 External Clock Edge Selection bit.
	0	Select falling edge of external clock.
	1	Select rising edge of external clock.
10	FORCA	Timer 30 Output Mode Selection bit. This bit should be changed when the T30EN is “0b”.
	0	6-Channel mode (The PWM30xA/PWM30xB pins are output according to the T30xDR registers, respectively)
	1	Force A-Channel mode (The all PWM30xA/PWM30xB pins are output according to the only T30ADR registers)
9	DLYEN	Delay Time Insertion Enable bit.
	0	Disable to insert delay time to the PWM30xA/PWM30xB.
	1	Enable to insert delay time to the PWM30xA/PWM30xB.
8	DLYPOS	Delay Time Insertion Position.
	0	Insert at front of PWM30xA and at back of PWM30xB pins.
	1	Insert at back of PWM30xA and at front of PWM30xB pins.
7 6	T30CPOL	Timer 30 Capture Polarity Selection bits.
	00	Capture on falling edge.
	01	Capture on rising edge.
	10	Capture on both of falling and rising edge.
	11	Reserved

6 4	UPDT	Data Reload Time Selection bits. 00 Update data to buffer at the time of writing. 01 Update data to buffer at period match. 10 Update data to buffer at bottom. 11 Not used.
3 1	PMOC	Period Match Interrupt Occurrence Selection. 000 Once every period match. 001 Once every 2 period match. 010 Once every 3 period match. 011 Once every 4 period match. 100 Once every 5 period match. 101 Once every 6 period match. 110 Once every 7 period match. 111 Once every 8 period match. Note) 1. A period match counter is cleared as 0x00 when the T3nCLR bit is set.
0	T30CLR	Timer 30 Counter and Prescaler Clear bit. 0 No effect. 1 Clear timer 30 counter and prescaler (Automatically cleared to “0b” after operation)

14.3.2 TIMER30_PDR Timer/Counter 30 Period Data Register

Timer/Counter 30 Period Data Register is 32-bit register. This Register is able to 32/16/8-bit access.

TIMER30_PDR=0x4000_2404

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																PDATA															
-																0xFFFF															
-																RW															

15 0	PDATA	Timer/Counter 30 Period Data bits. The range is 0x0002 to 0xFFFF. Note) 1. Do not write “0000H” in the T30PDR register when PPG mode.

14.3.3 TIMER30_ADR Timer/Counter 30 A Data Register

Timer/Counter 30 A Data Register is 32-bit register. This Register is able to 32/16/8-bit access.

TIMER30_ADR=0x4000_2408

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																ADATA															
-																0xFFFF															
-																RW															

15 0	ADATA	Timer/Counter 30 A Data bits. The range is 0x0000 to 0xFFFF.

14.3.4 TIMER30_BDR Timer/Counter 30 B Data Register

Timer/Counter 30 B Data Register is 32-bit register. This Register is able to 32/16/8-bit access.

TIMER30_BDR=0x4000_240C

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																BDATA															
-																0xFFFF															
-																RW															

15 0	BDATA	Timer/Counter 30 B Data bits. The range is 0x0000 to 0xFFFF.

14.3.5 TIMER30_CDR Timer/Counter 30 C Data Register

Timer/Counter 30 C Data Register is 32-bit register. This Register is able to 32/16/8-bit access.

TIMER30_CDR=0x4000_2410

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																CDATA															
-																0xFFFF															
-																RW															

15 0	CDATA	Timer/Counter 30 C Data bits. The range is 0x0000 to 0xFFFF.

14.3.6 TIMER30_CAPDR Timer/Counter 30 Capture Data Register

Timer/Counter 30 Capture Data Register is 32-bit register. This Register is able to 32/16/8-bit access.

TIMER30_CAPDR=0x4000_2414

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																CAPD															
-																0x0000															
-																RO															

15 0	CAPD	Timer/Counter 30 Capture Data bits.

14.3.7 TIMER30_PREDR Timer/Counter 30 Prescaler Data Register

Timer/Counter 30 Prescaler Data Register is 32-bit register. This Register is able to 32/16/8-bit access.

TIMER30_PREDR=0x4000_2418

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																				PRED											
-																				0xFFF											
-																				RW											

11 0	PRED	Timer/Counter 30 Prescaler Data bits.

14.3.8 TIMER30_CNT Timer/Counter 30 Counter Register

Timer/Counter 30 Counter Register is 32-bit register. This Register is able to 32/16/8-bit access.

TIMER30_CNT=0x4000_241C

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																CNT															
-																0x0000															
-																RO															

15 0	CNT	Timer/Counter 30 Counter bits.

14.3.9 TIMER30_OUTCR Timer/Counter 30 Output Control Register

Timer/Counter 30 Output Control Register is 32-bit register. This Register is able to 32/16/8-bit access.

TIMER30_OUTCR=0x4000_2420

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
WTIDKY																POLB	POLA	PABOE	PBBOE	PCBOE	PAAOE	PBAOE	PCAOE	Reserved	LVLAB	LVLBB	LVLCB	Reserved	LVLAA	LVLBA	LVLCA
0x0000																0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
WO																RW	RW	RW	RW	RW	RW	RW	RW	-	RW	RW	RW	-	RW	RW	RW

31 16	WTIDKY	Write Identification Key. On writes, write 0xE06C to these bits, otherwise the write is ignored.
15	POLB	PWM30xB Output Polarity Selection bit. (x : A, B and C) 0 Low level start. (The PWM30xB pins are started with low level after counting) 1 High level start. (The PWM30xB pins are started with high level after counting)
14	POLA	PWM30xA Output Polarity Selection bit. (x : A, B and C) 0 Low level start. (The PWM30xA pins are started with low level after counting) 1 High level start. (The PWM30xA pins are started with high level after counting)
13	PABOE	PWM30AB Output Enable bit. 0 Disable output. 1 Enable output.
12	PBBOE	PWM30BB Output Enable bit. 0 Disable output. 1 Enable output.
11	PCBOE	PWM30CB Output Enable bit. 0 Disable output. 1 Enable output.
10	PAAOE	PWM30AA Output Enable bit. 0 Disable output. 1 Enable output.
9	PBAOE	PWM30BA Output Enable bit. 0 Disable output. 1 Enable output.
8	PCAOE	PWM30CA Output Enable bit. 0 Disable output. 1 Enable output.
6	LVLAB	Configure PWM30AB output When Disable. 0 Low level 1 High level
5	LVLBB	Configure PWM30BB output When Disable. 0 Low level 1 High level
4	LVLCB	Configure PWM30CB output When Disable. 0 Low level 1 High level

2	LVLAA	Configure PWM30AA output When Disable.
		0 Low level
		1 High level
1	LVLBA	Configure PWM30BA output When Disable.
		0 Low level
		1 High level
0	LVLCA	Configure PWM30CA output When Disable.
		0 Low level
		1 High level

14.3.10 TIMER30_DLY Timer/Counter 30 PWM Output Delay Data Register

Timer/Counter 30 PWM Output Delay Data Register is 32-bit register. This Register is able to 32/16/8-bit access.

TIMER30_DLY=0x4000_2424

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																						DLY									
-																						0x000									
-																						RW									

9	DLY	Timer/Counter 30 PWM Delay Data bits. Delay time:
0		(DLY[9:0]+1)÷fT30

14.3.11 TIMER30_INTCR Timer/Counter 30 Interrupt Control Register

Timer/Counter 30 Interrupt Control Register is 32-bit register. This Register is able to 32/16/8-bit access.

TIMER30_INTCR=0x4000_2428

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																								HIZIEN	T30CIEN	T30BTIEN	T30PMIEN	T30AMIEN	T30BMIEN	T30CMIEN	
-																								0	0	0	0	0	0	0	
-																								RW	RW	RW	RW	RW	RW	RW	

6	HIZIEN	Timer 30 Output High-Impedance Interrupt Enable bit.
		0 Disable timer 30 output high-impedance interrupt.
		1 Enable timer 30 output high-impedance interrupt.
5	T30CIEN	Timer 30 Capture Interrupt Enable bit.
		0 Disable timer 30 capture interrupt.
		1 Enable timer 30 capture interrupt.
4	T30BTIEN	Timer 30 Bottom Interrupt Enable bit.
		0 Disable timer 30 period interrupt.
		1 Enable timer 30 period interrupt.
3	T30PMIEN	Timer 30 Period Match Interrupt Enable bit.
		0 Disable timer 30 period interrupt.
		1 Enable timer 30 period interrupt.
2	T30AMIEN	Timer 30 A-ch Match Interrupt Enable bit.
		0 Disable timer 30 A-ch match interrupt.
		1 Enable timer 30 A-ch match interrupt.
1	T30BMIEN	Timer 30 B-ch Match Interrupt Enable bit.
		0 Disable timer 30 B-ch match interrupt.
		1 Enable timer 30 B-ch match interrupt.
0	T30CMIEN	Timer 30 C-ch Match Interrupt Enable bit.
		0 Disable timer 30 C-ch match interrupt.
		1 Enable timer 30 C-ch match interrupt.

14.3.12 TIMER30_INTFLAG Timer/Counter 30 Interrupt Flag Register

Timer/Counter 30 Interrupt Flag Register is 32-bit register. This Register is able to 32/16/8-bit access.

TIMER30_INTFLAG=0x4000_242C

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																									HIZIFLAG	T30CIFLAG	T30BTIFLAG	T30PMIFLAG	T30AMIFLAG	T30BMIFLAG	T30CMIFLAG
-																									0	0	0	0	0	0	0
-																									RW	RW	RW	RW	RW	RW	RW

6	HIZIFLAG	Timer 30 Output High-Impedance Interrupt Flag bit.
		0 No request occurred.
		1 Request occurred, This bit is cleared to '0' when write '1'.
5	T30CIFLAG	Timer 30 Capture Interrupt Flag bit.
		0 No request occurred.
		1 Request occurred, This bit is cleared to '0' when write '1'.
4	T30BTIFLAG	Timer 30 Bottom Interrupt Flag bit.
		0 No request occurred.
		1 Request occurred, This bit is cleared to '0' when write '1'.
3	T30PMIFLAG	Timer 30 Period Match Flag Enable bit.
		0 No request occurred.
		1 Request occurred, This bit is cleared to '0' when write '1'.
2	T30AMIFLAG	Timer 30 A-ch Match Interrupt Flag bit.
		0 No request occurred.
		1 Request occurred, This bit is cleared to '0' when write '1'.
1	T30BMIFLAG	Timer 30 B-ch Match Interrupt Flag bit.
		0 No request occurred.
		1 Request occurred, This bit is cleared to '0' when write '1'.
0	T30CMIFLAG	Timer 30 C-ch Match Interrupt Flag bit.
		0 No request occurred.
		1 Request occurred, This bit is cleared to '0' when write '1'.

14.3.13 TIMER30_HIZCR Timer/Counter 30 High-Impedance Control Register

Timer/Counter 30 High-Impedance Control Register is 32-bit register. This Register is able to 32/16/8-bit access.

TIMER30_HIZCR=0x4000_2430

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																								HIZEN	Reserved		HIZSW	Reserved	HEDGE	HIZSTA	HIZCLR
-																								0	-		0	-	0	0	0
-																								RW	-		RW	-	RW	RW	RW

7	HIZEN	PWM30xA/PWM30xB Output High-Impedance Enable bit.	
		0	Disable to control the output high-impedance.
		1	Enable to control the output high-impedance.
4	HIZSW	High-Impedance Output Software Setting.	
		0	No effect.
		1	PWM30xA/PWM30xB pins go into high impedance. (Automatically cleared to “0b” after operation)
2	HEDGE	High-Impedance Edge Selection.	
		0	Falling edge of the BLNK pin.
		1	Rising edge of the BLNK pin.
1	HIZSTA	High-Impedance Status.	
		0	Indicates that the pins are not under a Hi-Z state.
		1	Indicates that the pins are under a Hi-Z state.
0	HIZCLR	High-Impedance Output Clear bit.	
		0	No effect.
		1	Clear high-impedance output. (The PWM30xA/PWM30xB pins are back to output and this bit is automatically cleared to “0b” after operation)

Note)

1. Where x = A, B, and C.

14.3.14 TIMER30_ADTCR Timer/Counter 30 A/DC Trigger Control Register

Timer/Counter 30 A/DC Trigger Control Register is 32-bit register. This Register is able to 32/16/8-bit access.

TIMER30_ADTCR=0x4000_2434

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																											T30BTTG	T30PMTG	T30AMTG	T30BMTG	T30CMTG
-																											0	0	0	0	0
-																											RW	RW	RW	RW	RW

4	T30BTTG	Select Timer 30 Bottom for A/DC Trigger Signal Generator.
	0	Disable A/DC trigger signal generator by bottom.
	1	Enable A/DC trigger signal generator by bottom.
3	T30PMTG	Select Timer 30 Period Match for A/DC Trigger Signal Generator.
	0	Disable A/DC trigger signal generator by period match.
	1	Enable A/DC trigger signal generator by period match.
2	T30AMTG	Select Timer 30 A-ch Match for A/DC Trigger Signal Generator.
	0	Disable A/DC trigger signal generator by A-ch match.
	1	Enable A/DC trigger signal generator by A-ch match.
1	T30BMTG	Select Timer 30 B-ch Match for A/DC Trigger Signal Generator.
	0	Disable A/DC trigger signal generator by B-ch match.
	1	Enable A/DC trigger signal generator by B-ch match.
0	T30CMTG	Select Timer 30 C-ch Match for A/DC Trigger Signal Generator.
	0	Disable A/DC trigger signal generator by C-ch match.
	1	Enable A/DC trigger signal generator by C-ch match.

Notes)

1. A trigger signal generation is not related with the PMOC[2:0] bits of T30CR register.
2. If several source for trigger is selected, a signal can be lost in case of the trigger generation counter is reloaded by another signal.

14.3.15 TIMER30_ADTDR Timer/Counter 30 A/DC Trigger Generator Data Register

Timer/Counter 30 A/DC Trigger Generator Data Register is 32-bit register. This Register is able to 32/16/8-bit access.

TIMER30_ADTDR=0x4000_2438

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																		ADTDATA													
-																		0x0000													
-																		RW													

13 0	ADTDATA	Timer/Counter 30 A/DC Trigger Generation Data bits.

14.4 Functional Description

14.4.1 Timer Counter 30

The timer/counter 30 can be clocked by an internal or an external clock source (EC30). The clock source is selected by clock selection logic which is controlled by the clock selection bits (T30CLK).

- TIMER 30 clock source: {PCLK/(TIMER30_PREDR +1), EC30

In the capture mode, by T30C, the data is captured into input capture data register (TIMER30_CAPDR).
The PWM wave form to PWM30AA, PWM30AB, PWM30BA, PWM30BB, PWM30CA, PWM3CB Port(6-channel).

Table 14.3 Timer 30 Operating Modes

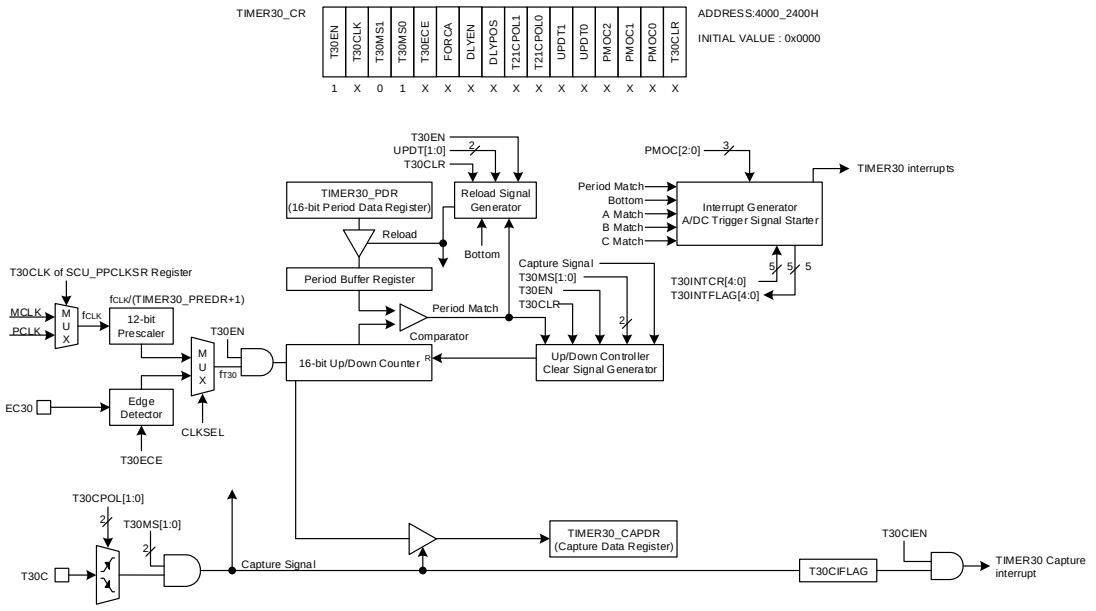
T30EN	T30MS[1:0]	T30PREDR	Timer 30
1	00	0xXXX	16-bit Interval Mode
1	01	0xXXX	16-bit Capture Mode
1	10	0xXXX	16-bit back-to-back Mode

14.4.2 Timer 30 Capture Mode

The 16-bit timer 30 capture mode is set by T30MS[1:0] as '01'. The clock source can use the internal or External clock input. Basically, it has the same function as the 16-bit interval mode and the interrupt occurs when TIMER30 16-bit up/down counter is equal to TIMTER30_PDR. The T30 16-bit up/down counter values are automatically cleared by match signal. It can be also cleared by software (T30CLR).

This timer interrupt in capture mode is very useful when the pulse width of captured signal is wider than the maximum period of timer.

The capture result is loaded into TIMER30_CAPDR.



Notes)

1. The Period match only can occur in the capture mode.
2. The 16-bit up/down counter in the capture mode is cleared to "0000H" after the counter value is loaded to the TIMER30_CAPDR register at valid edge.

Figure 14.2 16-bit Capture Mode for Timer 30

14.4.3 Timer 30 Interval Mode

The interval mode is set by T30MS[1:0] as '00'. The timer 30 has counter and data register. The 16-bit up/down counter is increased by internal or External clock input. The timer 30 can use the input clock with 12-bit prescaler division rates (TIMER30_PREDR[11:0]). When the value of T30 16-bit up/down counter and the value of T30PDR are identical in timer 30, a match signal is generated and the period match interrupt of timer 30 is occurred. The period match interrupt can be occurred which once every 1, 2, 3, 4, 5, 6, 7, or 8 period match (PMOC[2:0]). The 16-bit up/down counter value is automatically cleared by match signal. It can be also cleared by software (T30CLR).

The timer 30 Interval mode can be operates for BLDC motor control. It has 6-channel pins output up to 16-bit resolution PWM output. When the value of 16-bit up/down counter and T30PDR are identical in timer 30, a period match signal is generated and the period match interrupt of timer 30 is occurred. The timer 30 A, B, and C match signals are generated and the A, B, and C match interrupts of timer 30 are occurred, when the 16-bit counter value are identical to the value of TIMER30_xDR. The period and duty of the PWM output is determined by the TIMER30_PDR (PWM period register), and TIMER30_xDR (each channel PWM duty register).

PWM Period = [TIMER30_PDR] X Source Clock
PWM Duty(A-ch) = [TIMER30_ADR] X Source Clock
PWM Duty(B-ch) = [TIMER30_BDR] X Source Clock
PWM Duty(C-ch) = [TIMER30_CDR] X Source Clock

The POLA/POLB bit of TIMER30_OUTCR register decides the polarity of PWM output. If the POLA/POLB bit is set to '1b', the PWM30xA/PWM30xB output is high level start, respectively. And if the POLA/POLB bit is cleared to '0b', the PWM30xA/PWM30xB output is low level start, respectively.

Table 14.4 PWM Channel Polarity

PxAOE	PxBOE	POLxA	POLxB	PWM3xA Pin Output	PWM3xB Pin Output
1	1	0	0	Low level start	Low level start
		0	1	Low level start	High level start
		1	0	High level start	Low level start
		1	1	High level start	High level start

Note)
1. Where x = A, B, and C.

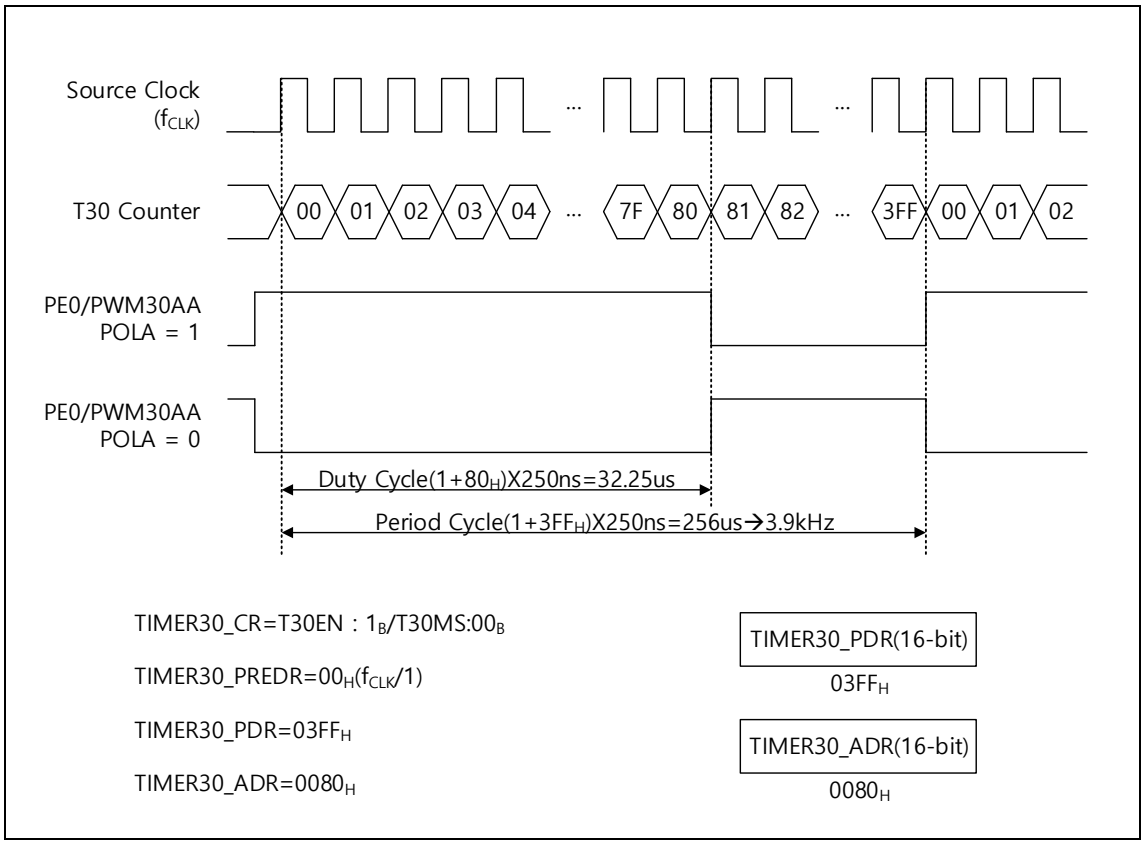
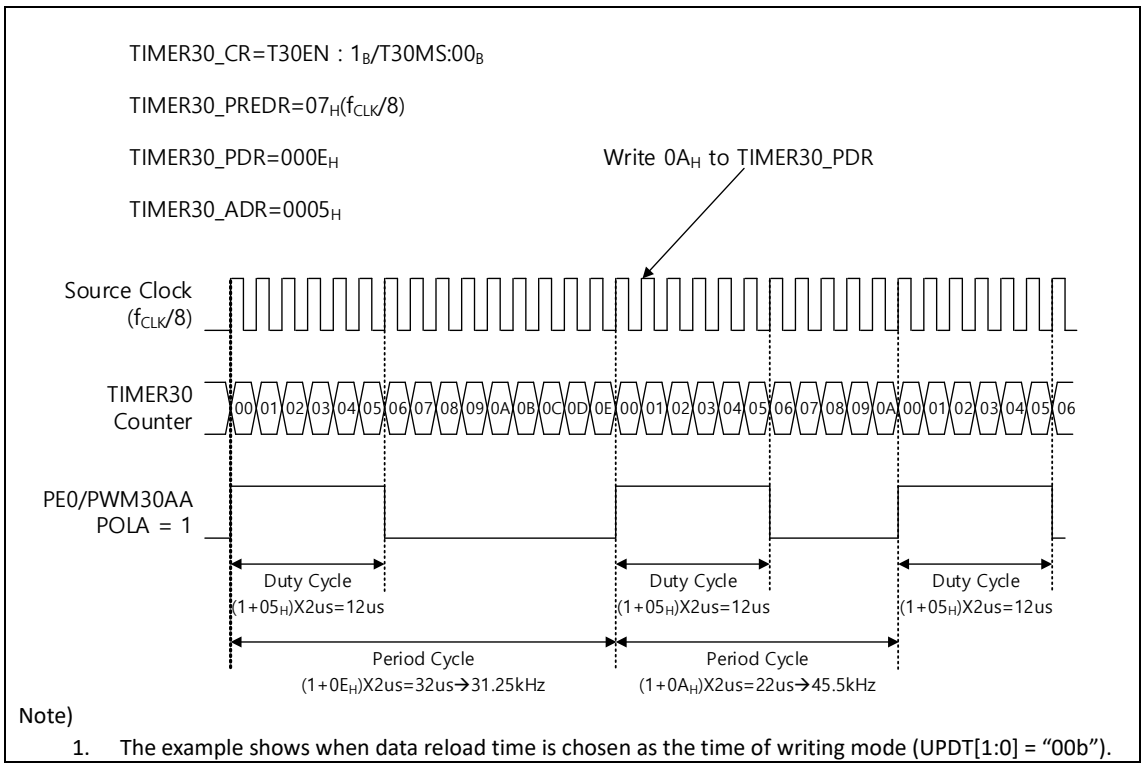


Figure 14.3 Example of PWM at 4 MHz



Note)

1. The example shows when data reload time is chosen as the time of writing mode (UPDT[1:0] = “00b”).

Figure 14.4 Example of Changing the Period in Absolute Duty Cycle at 4 MHz

14.4.3.1 Data Reload Time Selection

The data reload time can choose among “update data to buffer at the time of writing”, “update data to buffer at period match”, or “update data to buffer at bottom”.

14.4.3.2 PWM output Delay

If using the DLYEN bit, DLYPOS bit, and TIMER30_DLY register, it can delay the PWM output. The DLYPOS setting to ‘0’, the delay Inserts at front of PWM30xA and at back of PWM30xB pins. The DLYPOS setting to ‘1’, the delay Inserts at back of PWM30xA and at front of PWM30xB pins. The settings of DLYEN bit, DLYPOS bit, and TIMER30_DLY register are applied equally to all PWM channels.

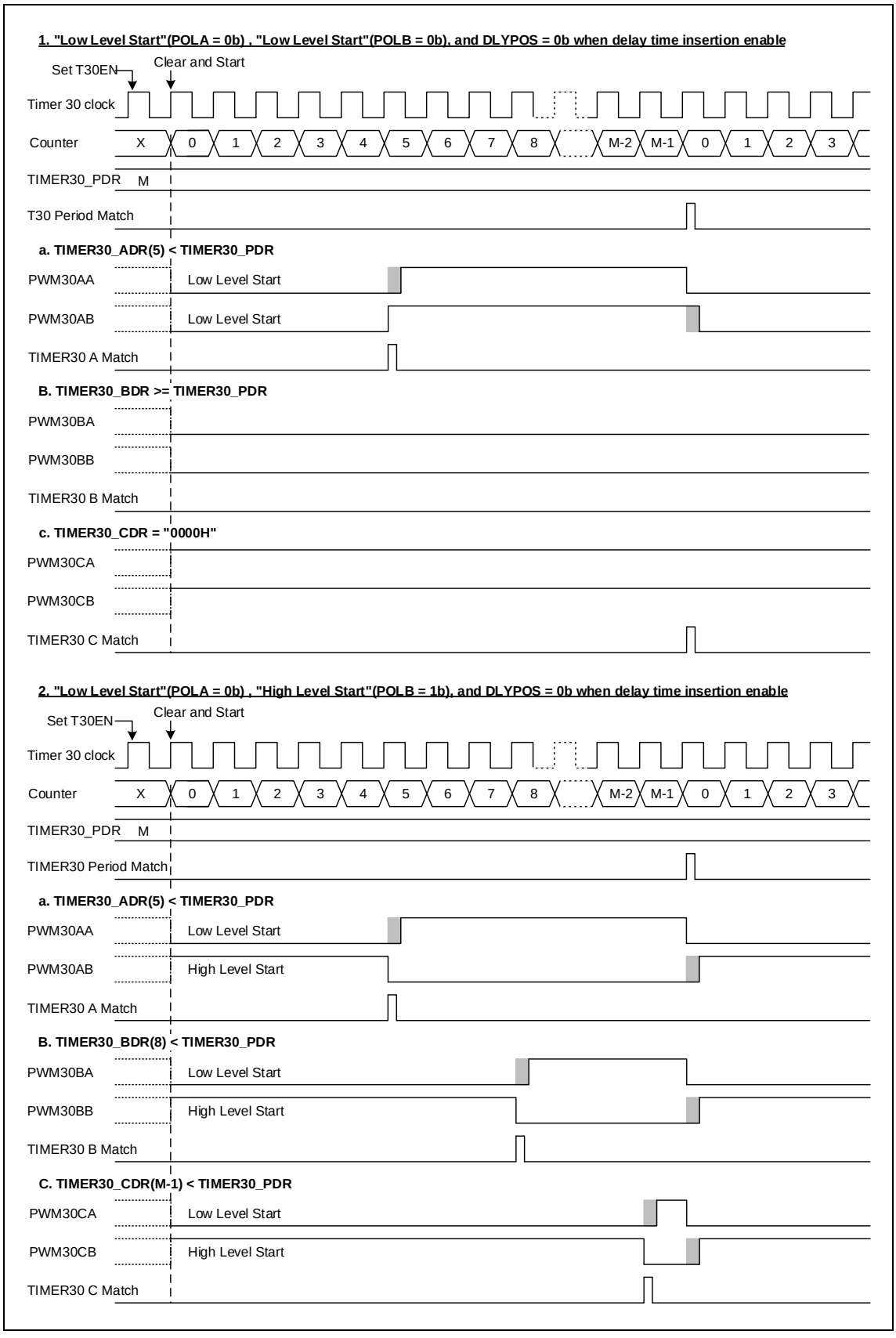


Figure 14.5 Interval Mode Timing Chart With "DLYPOS = 0"

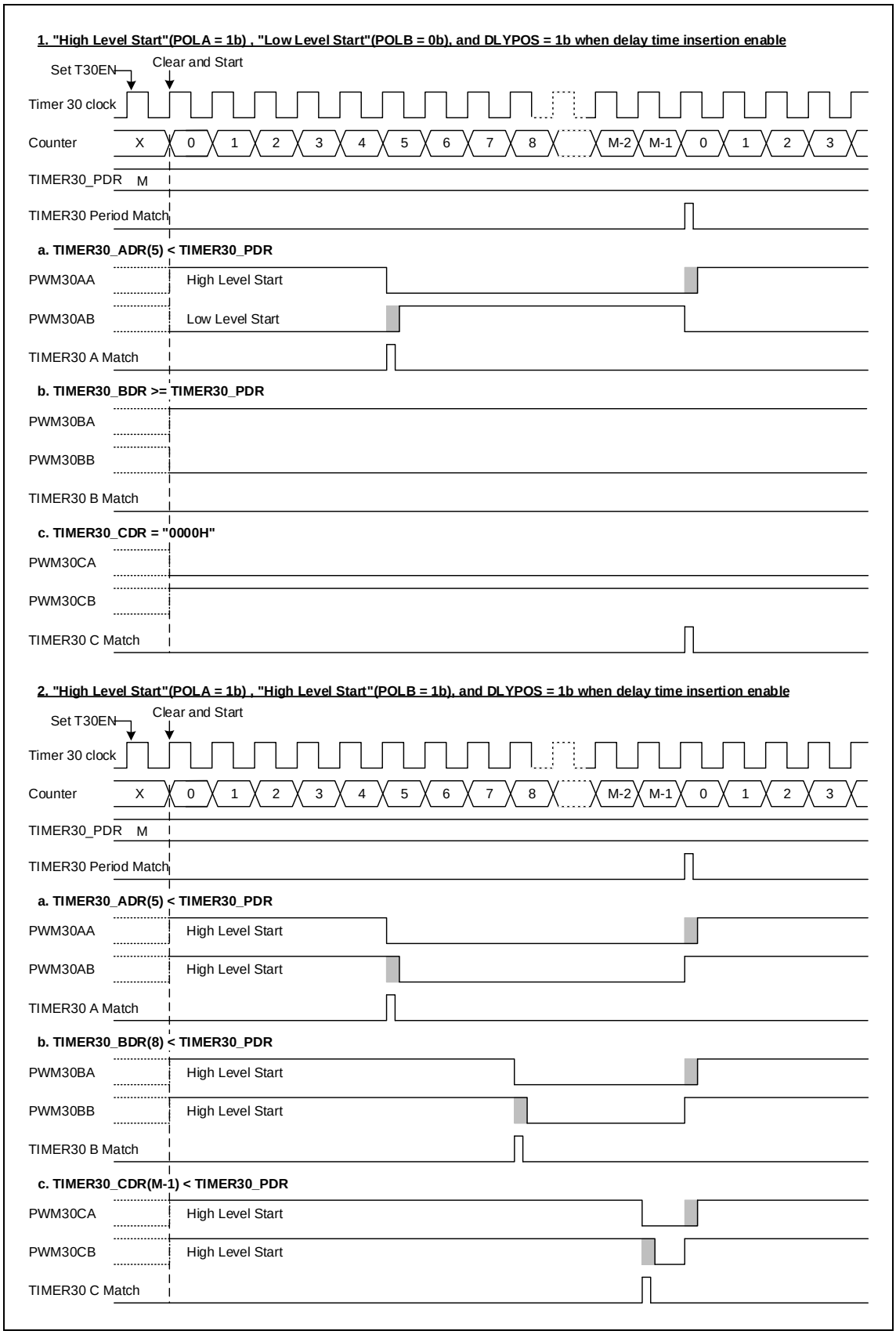


Figure 14.6 Interval Mode Timing Chart With "DLYPOS = 1

14.4.3.3 Back-to-Back Mode

The back-to-back mode is set by T30MS[1:0] as '10'. In the back-to-back mode, the 16-bit up/down counter repeats up/down count. In fact, the effective duty and period becomes twofold of the register set values. If the TIMER30_PDR's data value is set to "3210H, 16-bit up/down counter will increament until it reaches 3210H. At this point, a period match signal is generated and the period match interrupt occurs. And then the 16-bit up/down counter will decreament until it reaches 0000H. At this point, the bottom interrupt occurs. It is repeated in this way.

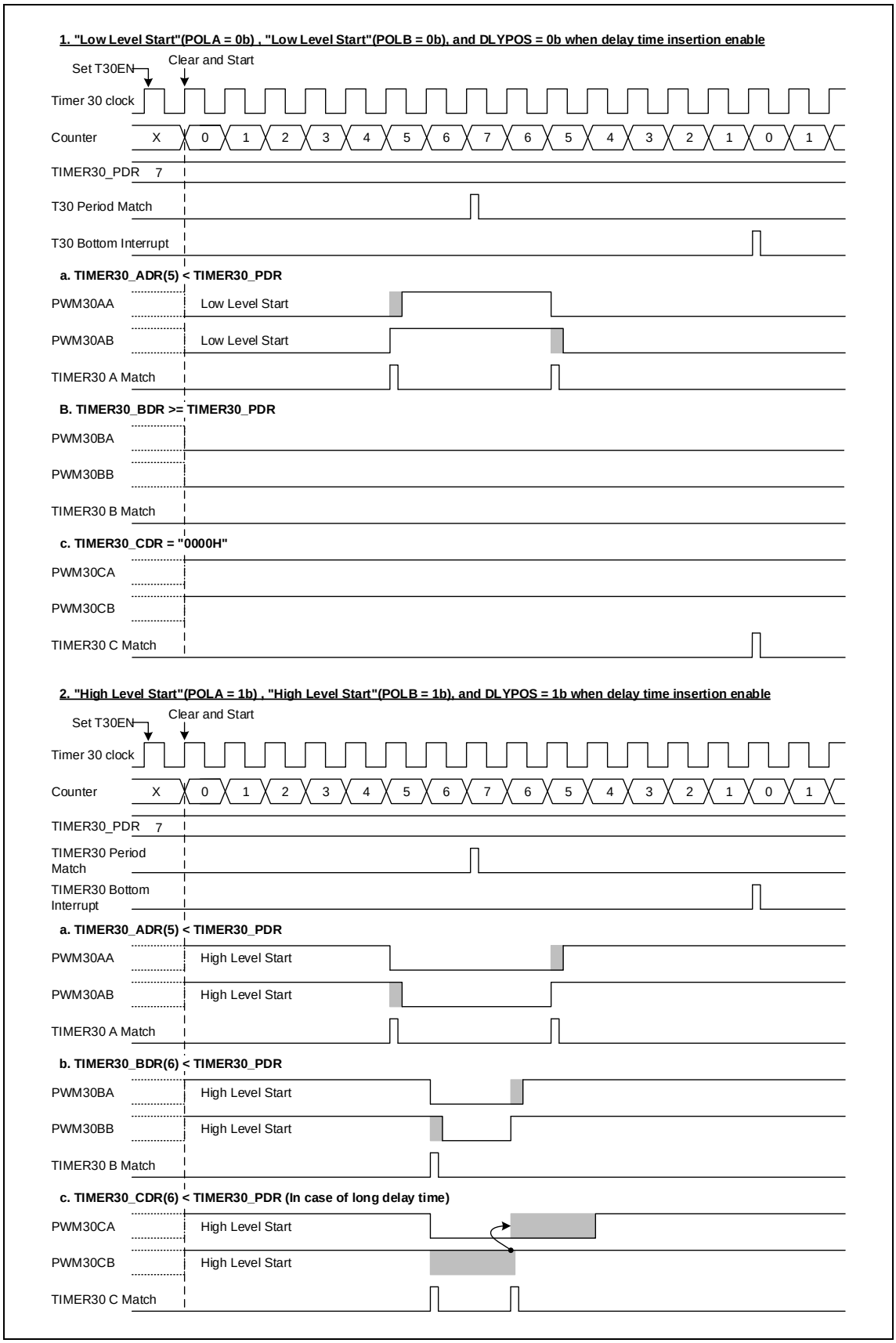


Figure 14.7 Back-to-Back Mode Timing Chart

14.4.3.4 Emergency Protective Function

This protective function is used for emergency stop, when the PWM30xA/PWM30xB output high-impedance enable bit, HIZEN is enabled. When the signal on the external BLNK input pin or internal comparator 3 output goes active (falling or rising edge triggered), the PWM30xA/PWM30xB ports are immediately disabled high-impedance against output and a high-impedance interrupt is occurred. The TIMER30_HIZCR register is used for high-impedance control. The high-impedance source is the external BLNK input pin. The high-impedance edge can be selected by HEDGE bit as falling or rising edge. If the HIZST read value is '1', it indicates that the pins are under a high-impedance state. To return from the high-impedance state, the HIZCLR bit set to '1'. If HIZSW bit is set to '1', PWM30xA/PWM30xB pins go into high impedance by software. It can be used for debugging. (x : A, B and C)

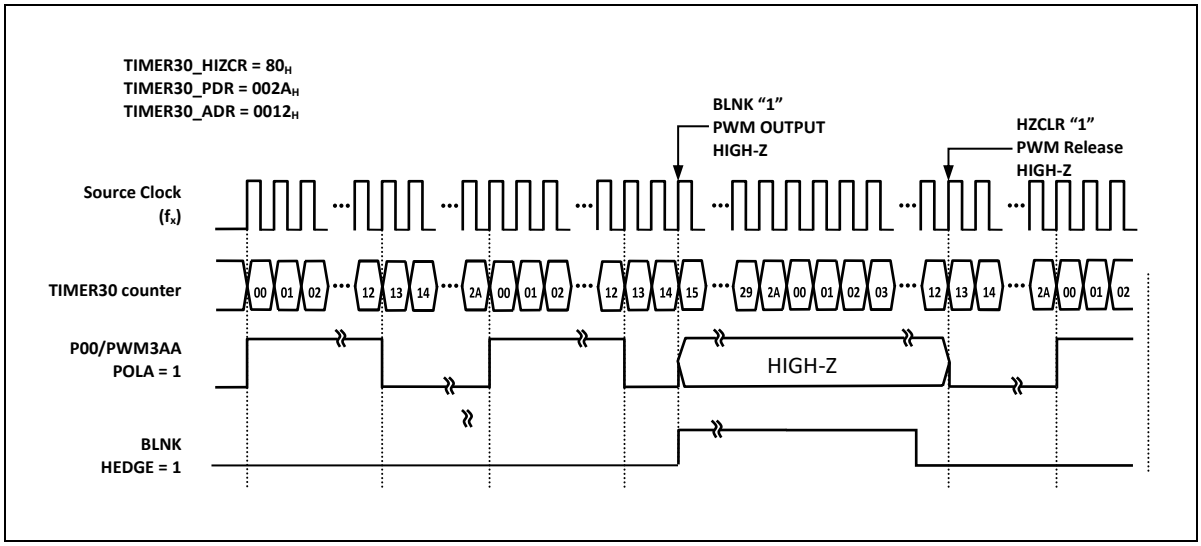


Figure 14.8 Example of PWM External Synchronization with BLNK Input (x : A, B and C)

14.4.3.5 FORCE A-Channel Mode

If FORCA bit sets to '1', it is possible to enable or disable all PWM output pins through PWM outputs which occur from A-ch duty counter. It is noted that the inversion outputs of A, B, C channel have the same A-ch output waveform.

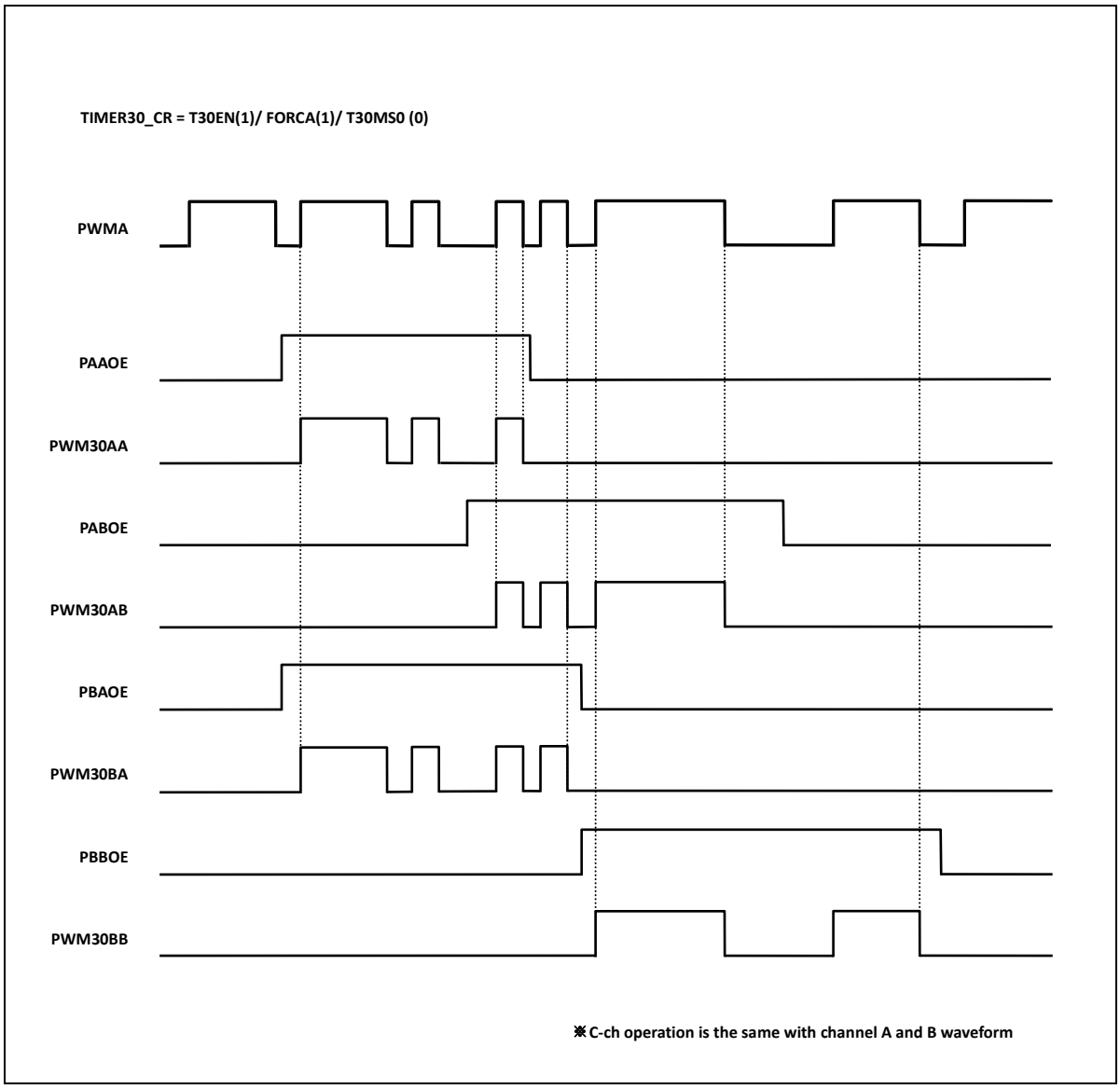


Figure 14.9 Example of Force A-Channel Mode

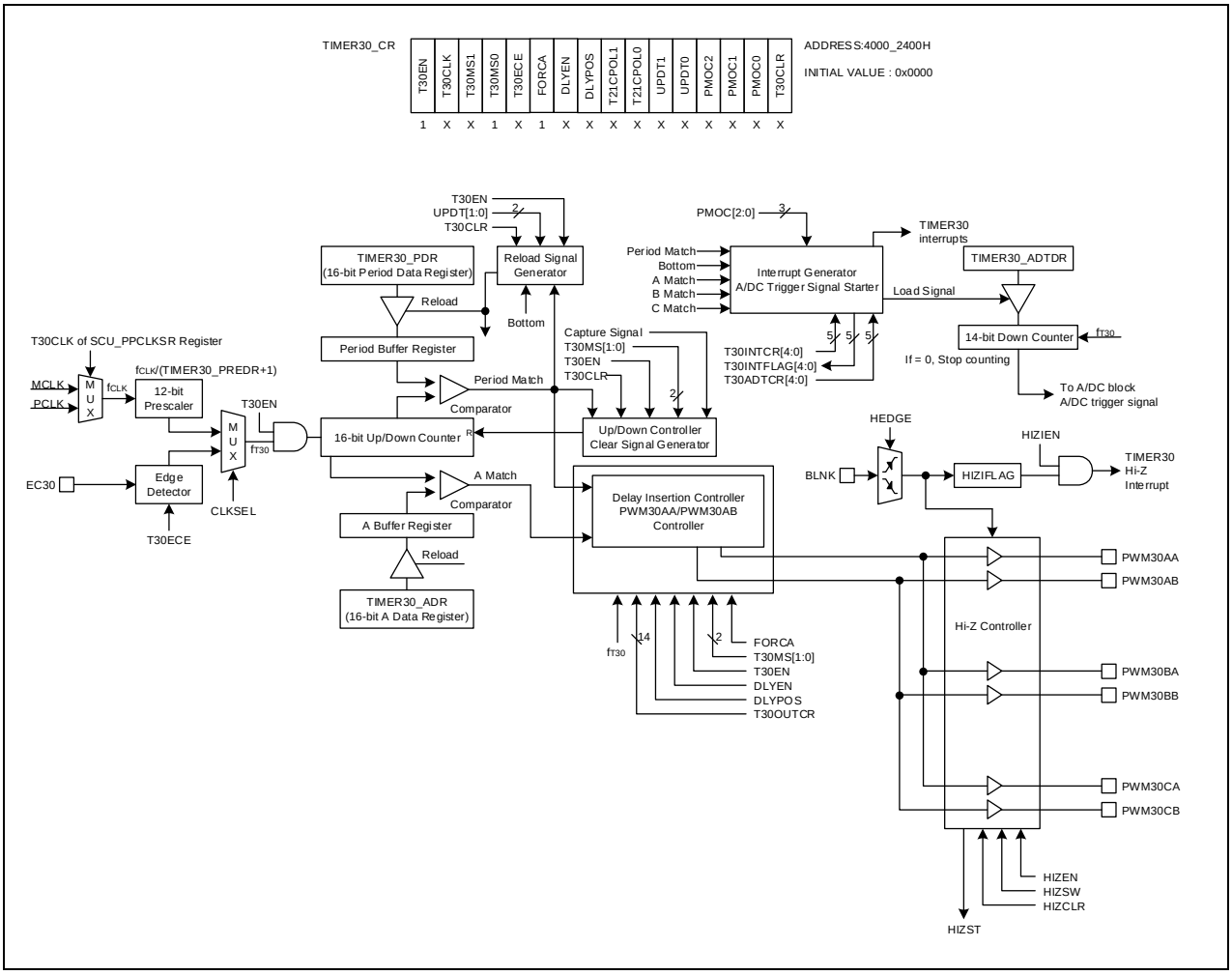


Figure 14.10 Force A-Channel Mode

14.4.3.6 6-Channel Mode

If FORCA bit sets to '0', it is possible to enable or disable PWM output pin and inversion output pin generated through the duty counter of each channel. The inversion output is the reverse phase of the PWM output. A AA/AB output of the A-channel duty register, a BA/BB output of the B-channel duty register, a CA/CB output of the C-channel duty register are controlled respectively.

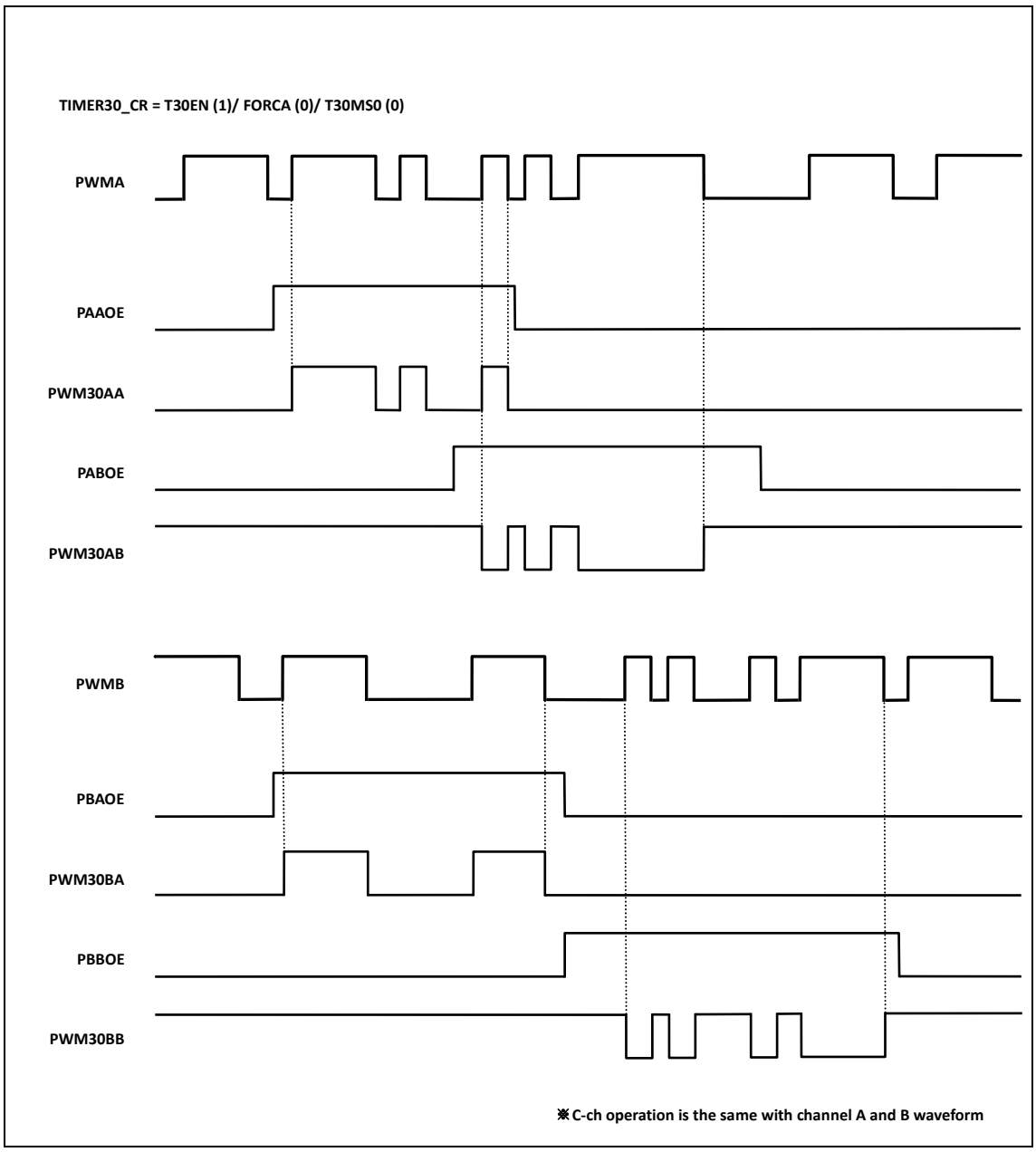


Figure 14.11 Example of 6-Channel Mode

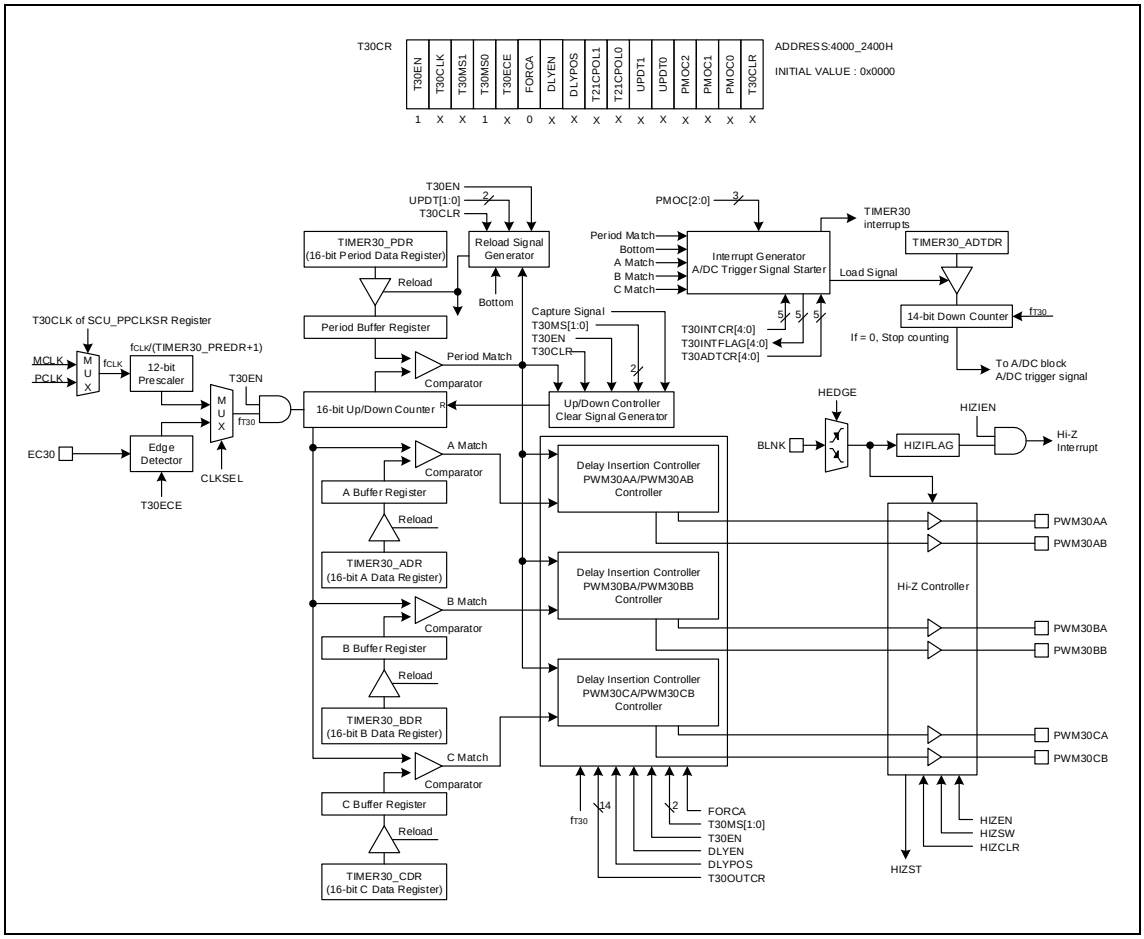


Figure 14.12 6-Channel Mode

CHAPTER 15. UNIVERSAL SYNCHRONOUS/ASYNCHRONOUS RECEIVER/TRANSMITTER (USART)

15.1 OVERVIEW

The Universal Synchronous and Asynchronous serial Receiver and Transmitter (USART) is a highly flexible serial communication device. The main features are listed below.

- Full Duplex Operation. (Independent Serial Receive and Transmit Registers)
- Asynchronous or Synchronous Operation.
- Baud Rate Generator.
- Supports Serial Frames with 5,6,7,8, or 9 Data bits and 1 or 2 Stop bits.
- Odd or Even Parity Generation and Parity Check are Supported by Hardware.
- Data OverRun Detection.
- Framing Error Detection.
- Three Separate Interrupts on TX Completion, TX Data Register Empty and RX Completion.
- Double Speed Asynchronous communication mode.

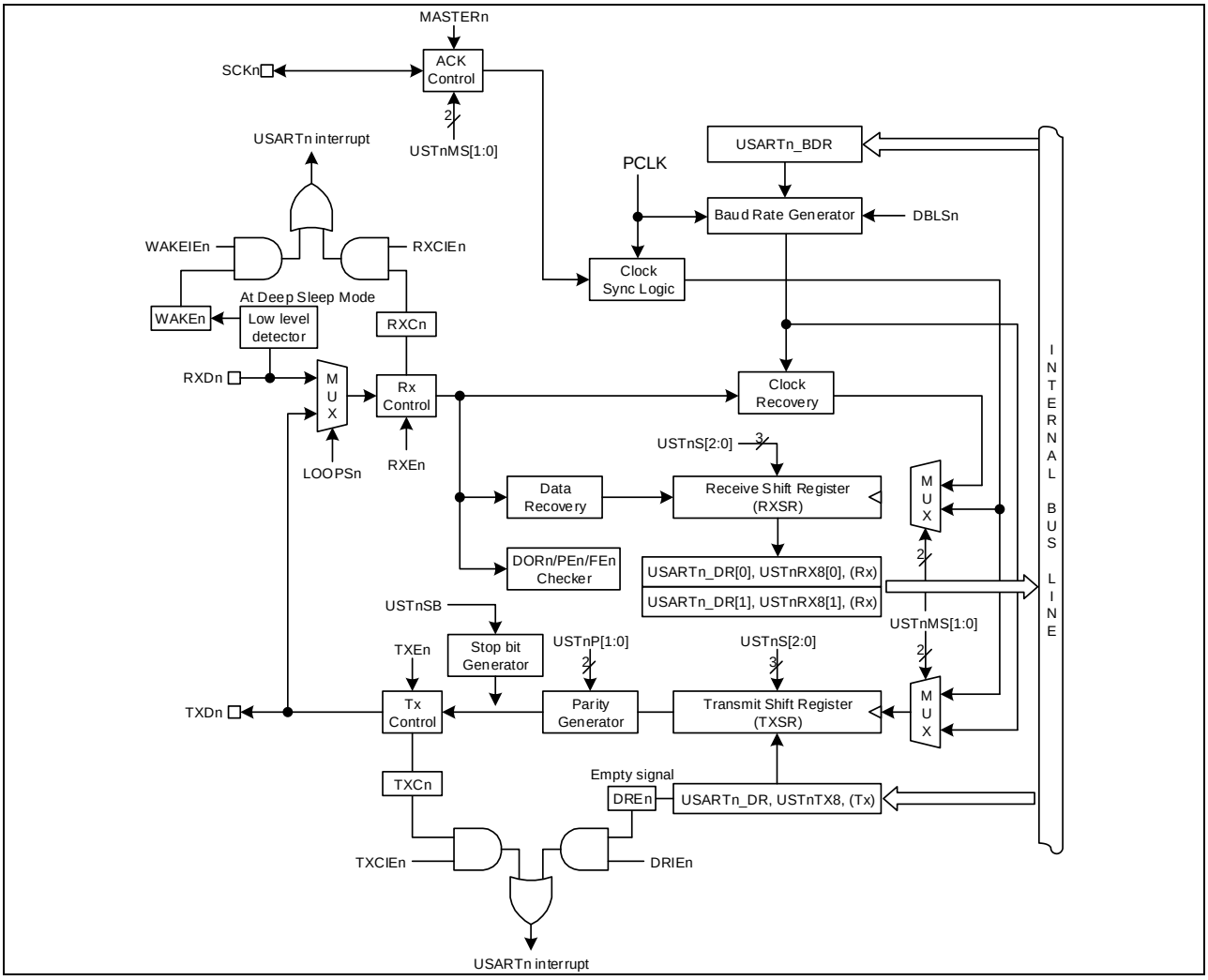


Figure 15.1. UART Block diagram (Where n = 10, 11, 12 and 13)

Figure shows the block diagram of a SPI block

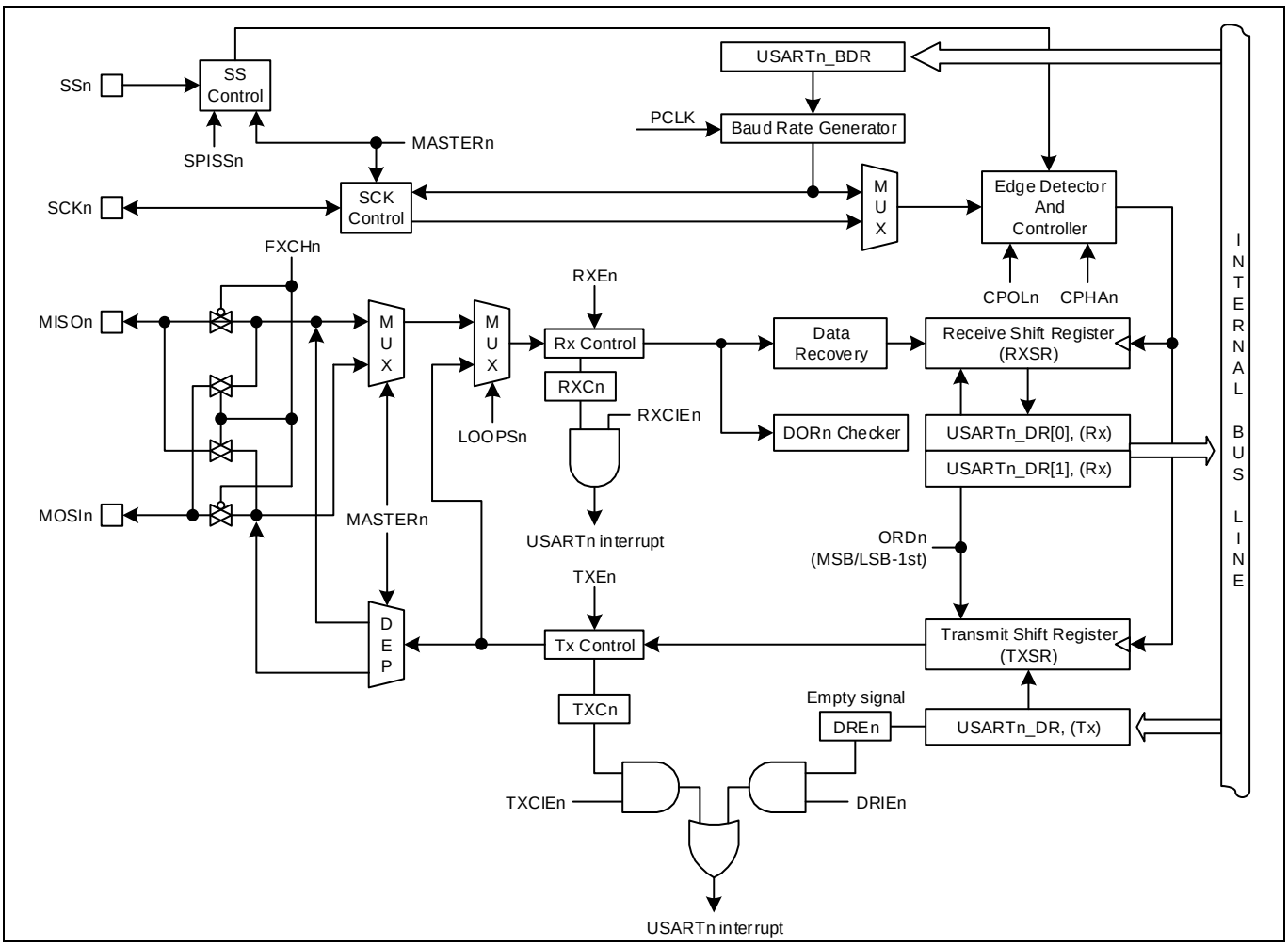


Figure15.2. SPIn Block diagram (Where n = 10, 11, 12, and 13)

15.2 Pin Description

Table 15.1 External pin (n = 10, 11, 12 and 13)

PIN NAME	TYPE	DESCRIPTION
TXDn	O	UART Channel n transmit output
RXDn	I	UART Channel n receive input
SSn	I/O	SPIn Slave select input / output
SCKn	I/O	SPIn Serial clock input / output
MOSIn	I/O	SPIn Serial data (Master output, Slave input)
MISOn	I/O	SPIn Serial data (Master input, Slave output)

15.3 REGISTERS

Base addresse of USART is as below.

Table 15.1 Base address of each port

NAME	BASE ADDRESS
USART10	0x4000_3800
USART11	0x4000_3900
USART12	0x4000_3A00
USART13	0x4000_3B00

Table 15.2 UART Register Map

Register Name	Offset	Access Type	Description	Initial Value	Ref
USARTn_CR1	0x00	RW	USARTn Control Register 1	0x0000_0000	15.3.1
USARTn_CR2	0x04	RW	USARTn Control Register 2	0x0000_0000	15.3.2
USARTn_ST	0x0C	RW	USARTn Status Register	0x0000_0080	15.3.3
USARTn_BDR	0x10	RW	USARTn Baud Rate Generation Register	0x0000_0FFF	15.3.4
USARTn_DR	0x14	RW	USARTn Data Register	0x0000_0000	15.3.5

Note: Where n = 10, 11, 12, and 13.

15.3.1 USARTn_CR1 USARTn Control Register 1

USART module should be configured properly before running. USARTn Control Register 1 is 32-bit register.

This Register is able to 32/16/8-bit access. (n = 10, 11, 12 and 13)

USART10_CR1=0x4000_3800, USART11_CR1=0x4000_3900, USART12_CR1=0x4000_3A00, USART13_CR1=0x4000_3B00

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																USTnMS		USTnP		USTnS			ORDn	CPOLn	CPHAn	DRIEn	TXCIEn	RXCIEn	WAKEIEn	TXEn	RXEn
-																00		00		000			0	0	0	0	0	0	0	0	0
-																RW		RW		RW			RW	RW	RW	RW	RW	RW	RW	RW	RW

15 14	USTnMS	USARTn Operation Mode Selection bits.			
		00	Asynchronous Mode. (UART)		
		01	Synchronous Mode.		
		10	Reserved.		
		11	SPI mode		
13 12	USTnP	Selects Parity Generation and Check method. (only UART mode)			
		00	No parity.		
		01	Reserved.		
		10	Even parity.		
		11	Odd parity.		
11 9	USTnS	Selects the length of data bit in a frame when Asynchronous or Synchronous mode.			
		000	5 bit.		
		001	6 bit.		
		010	7 bit.		
		011	8 bit.		
		111	9 bit.		
		Others	Reserved.		
8	ORDn	Selects the first data bit to be transmitted. (only SPI mode)			
		0	LSB-first.		
		1	MSB-first.		
7	CPOLn	Selects the clock polarity of ACK in synchronous or SPI mode.			
		0	TXD Change @Rising Edge, RXD Change @Falling Edge.		
		1	TXD Change @Falling Edge, RXD Change @Rising Edge.		
6	CPHAn	The CPOLn and this bit determine if data are sampled on the leading or trailing edge of SCK. (only SPI mode)			
		CPOLn	CPHAn	Leading edge	Trailing edge
		0	0	Sample (Rising)	Setup (Falling)
		0	1	Setup (Rising)	Sample (Falling)
		1	0	Sample (Falling)	Setup (Rising)
		1	1	Setup (Falling)	Sample (Rising)
5	DRIEn	Transmit Data Register Empty Interrupt Enable bit.			
		0	Disable the transmit data empty interrupt.		
		1	Enable the transmit data empty interrupt.		
4	TXCIEn	Transmit Complete Interrupt Enable bit.			
		0	Disable transmit complete interrupt.		
		1	Enable transmit complete interrupt.		
3	RXCIEn	Receive Complete Interrupt Enable bit.			
		0	Disable receive complete interrupt.		
		1	Enable receive complete interrupt.		

2	**WAKEIEn**	Asynchronous Wake-up Interrupt Enable bit in Deep Sleep Mode. When device is in deep sleep mode, if RXDn goes to low level, an interrupt can be requested to wake-up system. (only UART mode)	
		0	Disable asynchronous wake-up interrupt.
		1	Enable asynchronous wake-up interrupt.
1	**TXEn**	Enables the Transmitter unit.	
		0	Transmitter is disabled.
		1	Transmitter is enabled.
0	**RXEn**	Enables the Receiver unit.	
		0	Receiver is disabled.
		1	Receiver is enabled.

Note)

1. The CPOLn and CPHAn bits should be changed during the TXEn and RXEn bits are “0b”

15.3.2 USARTn_CR2 USARTn Control Register 2

USART module should be configured properly before running. USARTn Control Register 2 is 32-bit register.

This Register is able to 32/16/8-bit access. (n = 10, 11, 12 and 13)

USART10_CR2=0x4000_3804, USART11_CR2=0x4000_3904, USART12_CR2=0x4000_3A04, USART13_CR2=0x4000_3B04

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																						USTnEN	DBLSn	MASTERn	LOOPSn	DISSCKn	USTnSSEN	FXCHn	USTnSB	USTnTX8	USTnRX8
-																						0	0	0	0	0	0	0	0	0	0
-																						RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

9	USTnEN	Activate USARTn Block by supplying.
		0 Disable USARTn block.
		1 Enable USARTn block.
8	DBLSn	Selects receiver sampling rate. (only UART mode)
		0 Normal asynchronous operation.
		1 Double speed asynchronous operation.
7	MASTERn	Selects master or slave in SPIn or Synchronous mode and controls the direction of SCKn pin.
		0 Slave operation. (External clock for SCKn)
		1 Master operation. (Internal clock for SCKn)
6	LOOPSn	Control the Loop Back mode of USARTn for test mode.
		0 Normal operation.
		1 Loop Back mode.
5	DISSCKn	In synchronous mode operation, selects the waveform of SCKn output.
		0 SCKn is free-running while USARTn is enabled in synchronous master mode.
		1 SCKn is active while any frame is on transferring.
4	USTnSSEN	This bit controls the SSn pin operation. (only SPI mode)
		0 Disable.
		1 Enable.
3	FXCHn	SPIn port function exchange control bit. (only SPI mode)
		0 No effect.
		1 Exchange MOSIn and MISOn function.
2	USTnSB	Selects the length of stop bit in Asynchronous or Synchronous mode.
		0 1 Stop bit.
		1 2 Stop bit.
1	USTnTX8	The ninth bit of data frame in Asynchronous or Synchronous mode of operation. Write this bit first before loading the USTnDR register.
		0 MSB (9^{th} bit) to be transmitter is '0'.
		1 MSB (9^{th} bit) to be transmitter is '1'.
0	USTnRX8	The ninth bit of data frame in Asynchronous or Synchronous mode of operation. Read this bit first before reading the receive buffer (only UART mode)
		0 MSB (9^{th} bit) to be received is '0'.
		1 MSB (9^{th} bit) to be received is '1'.

15.3.3 USARTn_ST USARTn Status Register

USARTn Status Register is 32-bit register. This Register is able to 32/16/8-bit access. (n = 10, 11, 12 and 13)

USART10_ST=0x4000_380C, USART11_ST=0x4000_390C, USART12_ST=0x4000_3A0C, USART13_ST=0x4000_3B0C

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																								DREn	TXCn	RXCn	WAKEn	Reserved	DORn	Fen	Pen
-																								1	0	0	0	-	0	0	0
-																								RW	RW	RW	RW	-	RW	RW	RW

7	DREn	Transmit Data Register Empty Interrupt Flag. The DRE flag indicates if the transmit data register (USTnDR) is ready to receive new data. If DRE is '1', the data register is empty and ready to be written.
	0	Transmit buffer is not empty.
	1	Transmit buffer is empty. This bit is cleared to '0' when write '1'.
6	TXCn	Transmit Complete Interrupt Flag. This flag is set when the entire frame in the transmit shift register has been shifted out and there is no new data currently present in the transmit buffer.
	0	No request occurred.
	1	Transmit buffer is empty and the data in transmit shift register are shifted out completely. This bit is cleared to '0' when write '1'.
5	RXCn	Receive Complete Interrupt Flag. This flag is set when there are unread data in the receive buffer and cleared when all the data in the receive buffer are read.
	0	There is no data unread in the receive buffer.
	1	There are more than 1 data in the receive buffer.
4	WAKEn	Asynchronous Wake-up Interrupt Flag. This flag is set when the RXD pin is detected low while the CPU is in deep sleep mode. (only UART mode)
	0	No request occurred.
	1	Request occurred, This bit is cleared to '0' when write '1'.
2	DORn	This bit is set if data OverRun occurs. While this bit is set, the incoming data frame is ignored. This flag is valid until the receive buffer is read.
	0	No Data OverRun.
	1	Data OverRun detected.
1	Fen	This bit is set if the first stop bit of next character in the receive buffer is detected as '0'. This bit is valid until the receive buffer is read. (only UART mode)
	0	No Frame Error.
	1	Frame Error detected.
0	Pen	This bit is set if the next character in the receive buffer has a Parity Error while parity is checked. This bit is valid until the receive buffer is read. (only UART mode)
	0	No Parity Error.
	1	Parity Error detected.

15.3.4 USARTn_BDR USARTn Baud Rate Generation Register

USARTn Baud Rate Generation Register is 32-bit register. This Register is able to 32/16/8-bit access. (n = 10, 11, 12 and 13)

USART10_BDR=0x4000_3810, USART11_BDR=0x4000_3910, USART12_BDR=0x4000_3A10, USART13_BDR=0x4000_3B10

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																				BDATA											
-																				0xFFF											
-																				RW											

11 0	BDATA	The value in this register is used to generate internal baud rate in UART mode or to generate SCK clock in SPI mode. To prevent malfunction, do not write '0' in UART mode and do not write '0' or '1' in synchronous or SPI mode.

15.3.5 USARTn_DR USARTn Data Register

USARTn Data Register is 32-bit register. This Register is able to 32/16/8-bit access. (n = 10, 11, 12 and 13)

USART10_DR=0x4000_3814, USART11_DR=0x4000_3914, USART12_DR=0x4000_3A14, USART13_DR=0x4000_3B14

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																								DATA							
-																								0x00							
-																								RW							

7 0	DATA	The USART Transmit buffer and Receive buffer share the same I/O address with this DATA register. The Transmit Data Buffer is the destination for data written to the USTnDR register. Reading the USTnDR register returns the contents of the Receive Buffer. Write to this register only when the DRE flag is set. In SPI master mode, the SCK clock is generated when data are written to this register. Note) 1. This byte won't be written when the block is disabled or the both of TXEn and RXEn bits are "0b".

15.4 Functional Description

The USART comprises clock generator, transmitter and receiver. The clock generation logic consists of synchronization logic for external clock input used by synchronizing or SPI slave operation, and the baud rate generator for asynchronous or master (synchronous or SPI) operation.

The Transmitter consists of a single write buffer, a serial shift register, parity generator and control logic for handling different serial frame formats.The write buffer allows continuous transfer of data without any delay between frames. The receiver is the most complex part of the UART module due to its clock and data recovery units. The recovery unit is used for asynchronous data reception. In addition to the recovery unit, the receiver includes a parity checker, a shift register, a two-level receive FIFO (USARTn_DR) and control logic. The receiver supports the same frame formats as the transmitter and can detect frame error, data overrun and parity errors. (n : 10, 11, 12 and 13)

15.4.1 USART Clock Generation

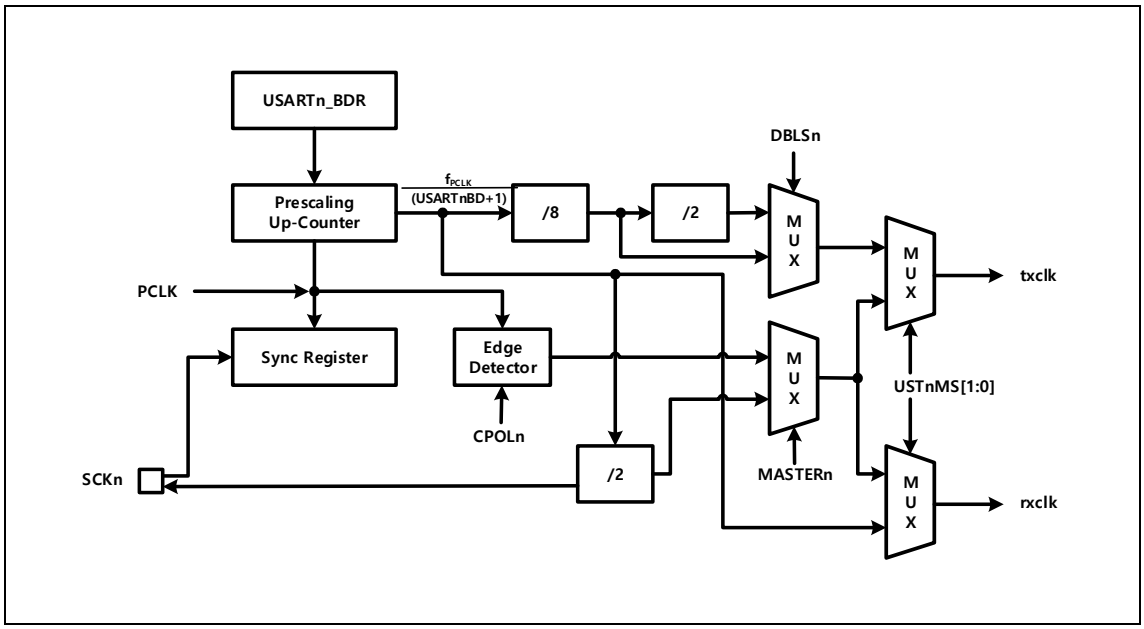


Figure 15.3. Clock Generation Block Diagram (USART, n = 10,11,12 and 13)

The clock generation logic generates the base clock for the transmitter and receiver. The USART supports four modes of clock operation and those are normal asynchronous, double speed asynchronous, master synchronous and slave synchronous mode. The clock generation scheme for master SPI and slave SPI mode is the same as master synchronous and slave synchronous operation mode. The USTnMS[1:0] bits in USARTn_CR1 register selects asynchronous or synchronous operation. Asynchronous double speed mode is controlled by the DBLS bit in the USARTn_CR2 register. The MASTER bit in USARTn_CR2 register controls whether the clock source is internal (master mode, output pin) or external (slave mode, input pin). The SCKn pin is active only when the USART operates in synchronous or SPI mode.

Following table shows the equations for calculating the baud rate (in bps).

Table 15.3 Equations for Calculating USART Baud Rate Register Setting (USART, n = 10,11,12 and 13)

Operating Mode	Equation for Calculating Baud Rate
Asynchronous Normal Mode (DBLSn=0)	Baud Rate= PCLK/(16(USARTn_BDR+1))
Asynchronous Double Speed Mode (DBLSn=1)	Baud Rate= PCLK/(8(USARTn_BDR+1))
Synchronous or SPI Master Mode	Baud Rate= PCLK/(2(USARTn_BDR+1))

15.4.2 External Clock (SCKn)

External clocking is used in the synchronous or SPI slave mode of operation.

External clock input from the SCKn pin is sampled by a synchronization logic to remove meta-stability. The output from the synchronization logic must be passed through an edge detector before it is used by the transmitter and receiver. This process introduces two CPU clock period delay. The maximum frequency of the external SCKn pin is limited up-to 1MHz.

15.4.3 Synchronous mode operation

External clocking is used in the synchronous or SPI slave mode of operation.

When synchronous or SPI mode is used, the SCKn pin will be used as either clock input (slave) or clock output (master). Data sampling and transmitter is issued on the different edge of SCKn clock each other. For example, if data input on RXDn (MISOn in SPI mode) pin is sampled on the rising edge of SCKn clock, data output on TXDn (MOSIn in SPI mode) pin is altered on the falling edge.

The CPOLn bit in USARTn_CR1 register selects which SCKn clock edge is used for data sampling and which is used for data change. As shown in the figure below, when CPOLn is zero, the data will be changed at rising SCKn edge and sampled at falling SCKn edge.

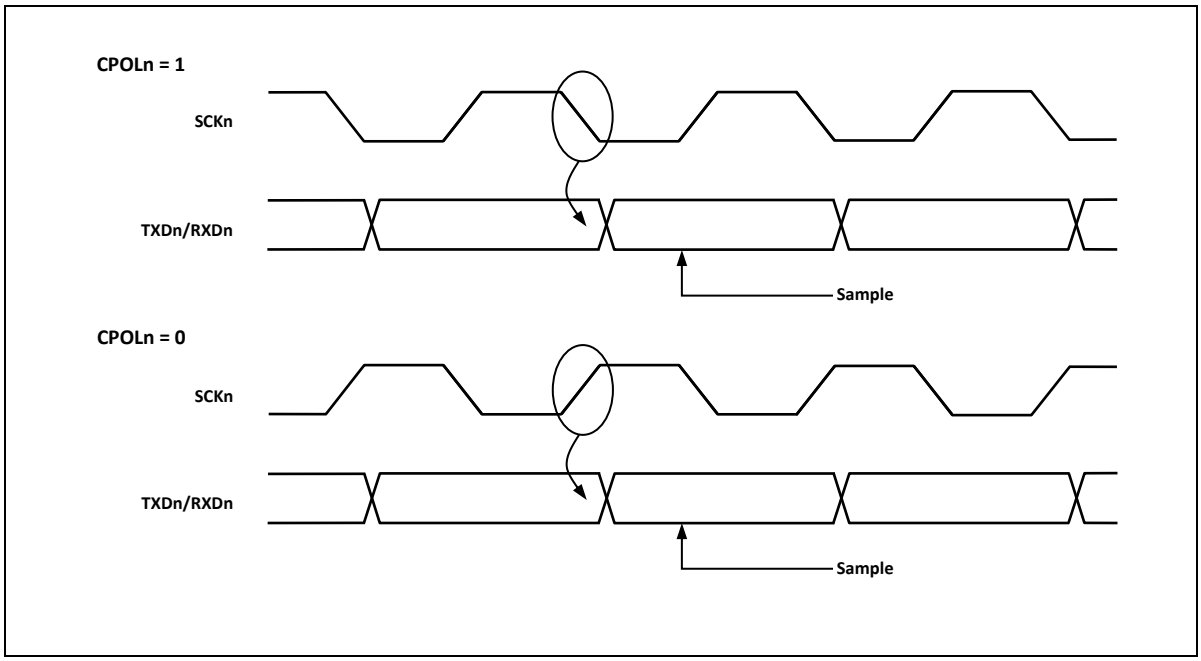


Figure 15.4. Synchronous Mode SCKn Timing (USART, n = 10,11,12 and 13)

15.4.4 UART Data format

A serial frame is defined to be one character of data bits with synchronization bits (start and stop bits), and optionally a parity bit for error detection.

The USART supports all 30 combinations of the following as valid frame formats.

- 1 start bit
- 5, 6, 7, 8 or 9 data bits
- no, even or odd parity bit.
- 1 or 2 stop bits.

A frame starts with the start bit followed by the least significant data bit (LSB). Then the next data bits, up to nine, are succeeding, ending with the most significant bit (MSB). If parity function is enabled, the parity bit is inserted between the last data bit and the stop bit. A high-to-low transition on data pin is considered as start bit. When a complete frame is transmitted, it can be directly followed by a new frame, or the communication line can be set to an idle state. The idle means high state of data pin. The following figure shows the possible combinations of the frame formats. Bits inside brackets are optional.

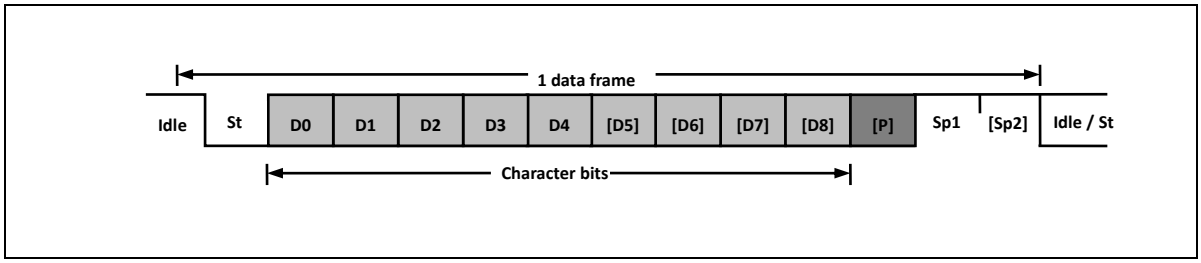


Figure 15.5. Frame Format (USART)

1 data frame consists of the following bits

- Idle: No communication on communication line (TXDn/RXDn)
- St : Start bit (Low)
- Dm : Data bits (0~8)
- Parity bit ---------- Even parity, Odd parity, No parity
- Stop bit(s) ---------- 1 bit or 2 bits

The frame format used by the UART is set by the USTnS[2:0], USTnP[1:0] bits in USARTn_CR1 register and USTnSB bit in USARTn_CR2 register. The transmitter and receiver use the same figures. (n = 10, 11, 12 and 13)

15.4.5 UART Parity bit

The parity bit is calculated by doing an exclusive-OR of all the data bits. If odd parity is used, the result of the exclusive-OR is inverted. The parity bit is located between the MSB and first stop bit of a serial frame.

- Peven = Dm-1 ^ … ^ D3 ^ D2 ^ D1 ^ D0 ^ 0
- Podd = Dm-1 ^ … ^ D3 ^ D2 ^ D1 ^ D0 ^ 1
- Peven : Parity bit using even parity
- Podd : Parity bit using odd parity
- Dm : Data bit n of the character

15.4.6 UART Transmitter

The UART transmitter is enabled by setting the TXEn bit in USARTn_CR1 register. When the Transmitter is enabled, the TXDn pin should be set to TXDn function for the serial output pin of UART by the PB_AFSR1/PD_AFSR1 and PBMOD/PDMOD. The baud-rate, operation mode and frame format must be set up once before doing any transmission. In synchronous operation mode, the SCKn pin is used as transmission clock, so it should be selected to do SCKn function by PB_AFSR1/PD_AFSR1 and PB_MOD/PD_MOD. (n = 10, 11, 12 and 13)

15.4.6.1 UART Sending TX data

A data transmission is initiated by loading the transmit buffer (USARTn_DR register I/O location) with the data to be transmitted. The data be written in transmit buffer is moved to the shift register when the shift register is ready to send a new frame. The shift register is loaded with the new data if it is in idle state or immediately after the last stop bit of the previous frame is transmitted. When the shift register is loaded with new data, it will transfer one complete frame according to the settings of control registers. If the 9-bit characters are used in asynchronous or synchronous operation mode, the ninth bit must be written to the USARTn_TX8 bit in USARTn_CR2 register before it is loaded to the transmit buffer (USARTn_DR register). (n = 10, 11, 12 and 13)

15.4.6.2 UART Transmitter flag and interrupt

The USART transmitter has two flags which indicate its state. One is USART data register empty flag (DREn) and the other is transmit completion flag (TXCn). Both flags can be interrupt sources.
DREn flag indicates whether the transmit buffer is ready to receive new data. This bit is set when the transmit buffer is empty and cleared when the transmit buffer contains data to be transmitted but has not yet been moved into the shift register. And also this flag can be cleared by writing '0' to this bit position. Writing '1' to this bit position is prevented.
When the data register empty interrupt enable (DRIEn) bit in USARTn_CR1 register is set and the global interrupt is enabled, USARTn_ST status register empty interrupt is generated while DREn flag is set.
The transmit complete (TXCn) flag bit is set when the entire frame in the transmit shift register has been shifted out and there is no more data in the transmit buffer. The TXCn flag is automatically cleared when the transmit complete interrupt serve routine is executed, or it can be cleared by writing '0' to TXCn bit in USARTn_ST register.
When the transmit complete interrupt enable (TXCIEn) bit in USARTn_CR1 register is setand the global interrupt is enabled, UART transmit complete interrupt is generated while TXCn flag is set. (n = 10, 11, 12 and 13)

15.4.6.3 UART Parity Generator

The parity generator calculates the parity bit for the serial frame data to be sent. When parity bit is enabled (USTnP1=1), the transmitter control logic inserts the parity bit between the MSB and the first stop bit of the frame to be sent. (n = 10, 11, 12 and 13)

15.4.6.4 UART Disabling Transmitter

Disabling the transmitter by clearing the TXEn bit will not become effective until on going transmission is completed. When the Transmitter is disabled, the TXDn pin can be used as a normal general purpose I/O (GPIO). (n = 10, 11, 12 and 13)

15.4.7 UART Receiver

The USART receiver is enabled by setting the RXEn bit in the USARTn_CR1 register. When the receiver is enabled, the RXDn pin should be set to RXDn function for the serial input pin of UART by PB_AFSR1/PD_AFSR1 and PB_MOD/PD_MOD. The baud-rate, mode of operation and frame format must be set before serial reception. In synchronous or SPI operation mode the SCKn pin is used as transfer clock input, so it should be selected to do SCKn function by PB_AFSR1/PD_AFSR1 and PB_MOD/PD_MOD. In SPI operation mode the SSn input pin in slave mode or can be configured as SSn output pin in master mode. This can be done by setting USTnSSEN bit in USARTn_CR2 register. (n = 10, 11, 12 and 13)

15.4.7.1 UART Receiving RX data

When UART is in synchronous or asynchronous operation mode, the receiver starts data reception when it detects a valid start bit (LOW) on RXDn pin. Each bit after start bit is sampled at pre-defined baud-rate (asynchronous) or sampling edge of SCKn (synchronous), and shifted into the receive shift register until the first stop bit of a frame is received. Even if there's the second stop bit in the frame, the second stop bit is ignored by the receiver. That is, receiving the first stop bit means that a complete serial frame is presented in the receiver shift register and contents of the shift register are to be moved into the receive buffer. The receive buffer is read by reading the USTnDR register.

If 9-bit characters are used (USTnS[2:0] = "111"), the ninth bit is stored in the USTnRX8 bit position in the USARTn_CR2 register. The nineth bit must be read from the USTnRX8 bit before reading the low 8 bits from the USnTDR register. Likewise, the error flags Fen, DORn, Pen must be read before reading the data from USARTn_DR register. It's because the error flags are stored in the same FIFO position of the receive buffer. (n = 10, 11, 12 and 13)

15.4.7.2 UART Receiver Flag and Interrupt

The UART receiver has one flag that indicates the receiver state.

The receive complete (RXCn) flag indicates whether there are unread data in the receive buffer. This flag is set when there is unread data in the receive buffer and cleared when the receive buffer is empty. If the receiver is disabled (RXEn=0), the receiver buffer is flushed and the RXCn flag is cleared.

When the receive complete interrupt enable (RXCIEn) bit in the USARTn_CR1 register is set and global interrupt is enabled, the UART receiver complete interrupt is generated while RXCn flag is set.

The UART receiver has three error flags which are frame error (Fen), data overrun (DORn) and parity error (Pen). These error flags can be read from the USARTn_ST register. As received datas are stored in the 2-level receive buffer, these error flags are also stored in the same position of receive buffer. So, before reading received data from USARTn_DR register, read the USARTn_ST register first which contains error flags.

The frame error (Fen) flag indicates the state of the first stop bit. The Fen flag is '0' when the stop bit was correctly detected as "1", and the Fen flag is "1" when the stop bit was incorrect, i.e. detected as "0". This flag can be used for detecting out-of-sync conditions between data frames.

The data overrun (DORn) flag indicates data loss due to a receive buffer full condition. DORn occurs when the receive buffer is full, and another new data is presented in the receive shift register which are to be stored into the receive buffer. After the DORn flag is set, all the incoming data are lost. To avoid data loss or clear this flag, read the receive buffer.

The parity error (Pen) flag indicates that the frame in the receive buffer had a parity error when received. If parity check function is not enabled (USTnP1=0), the Pen bit is always read "0". (n = 10, 11, 12 and 13)

15.4.7.3 UART Parity Checker

If parity bit is enabled (USTnP1=1), the Parity Checker calculates the parity of the data bits in incoming frame and compares the result with the parity bit from the received serial frame. (n = 10, 11, 12 and 13)

15.4.7.4 UART Disabling Receiver

In contrast to transmitter, disabling the Receiver by clearing RXEn bit makes the Receiver inactive immediately. When the receiver is disabled, the receiver flushes the receive buffer, the remaining data in the buffer is all reset, and the RXDn pin can be used as a normal general purpose I/O (GPIO). (n = 10, 11, 12 and 13)

15.4.7.5 Asynchronous Data Reception

To receive asynchronous data frame, the USART includes a clock and data recovery unit. Theclock recovery logic is used for synchronizing the internally generated baud-rate clock to the incoming asynchronous serial frame on the RXDn pin.
The data recovery logic does sampling and low pass filtering the incoming bits, and removing the noise of RXDn pin.
The next figure illustrates the sampling process of the start bit of an incoming frame. The sampling rate is 16 times of the baud-rate in normal mode and 8 times the baud-rate for double speed mode (DBLSn=1). The horizontal arrows show the synchronization variation due to the asynchronous sampling process. Note that larger time variation is shown when using the double speed mode. (n = 10, 11, 12 and 13)

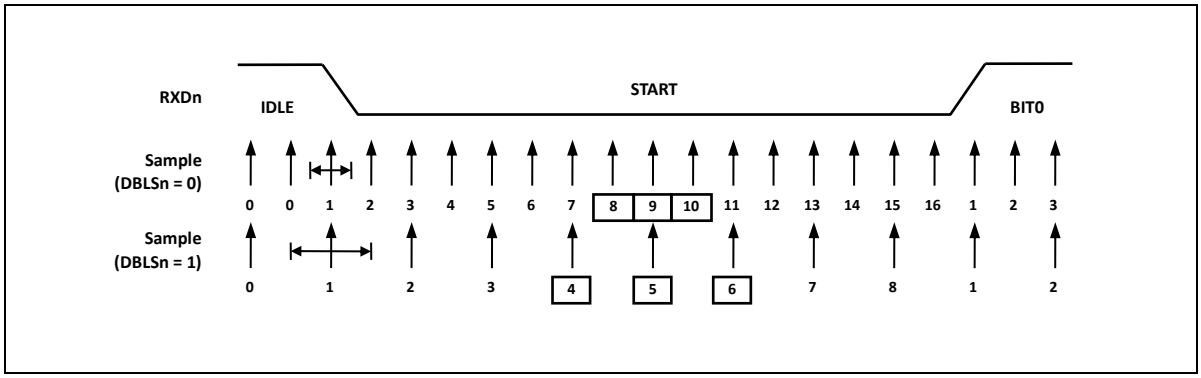


Figure 15.6. Asynchronous Start Bit Sampling (n = 10,11,12 and 13)

When the receiver is enabled (RXEn=1), the clock recovery logic tries to find a high-to-low transition on the RXDn line, the start bit condition. After detecting high to low transition on RXDn line, the clock recovery logic uses samples 8, 9 and 10 for normal mode to decide if a valid start bit is received. If more than 2 samples have logical low level, it is considered that a valid start bit is detected and the internally generated clock is synchronized to the incoming data frame. And the data recovery can begin. The synchronization process is repeated for each start bit.
As described above, when the receiver clock is synchronized to the start bit, the data recovery can begin. Data recovery process is almost same to the clock recovery process. The data recovery logic samples 16 times for each incoming bits for normal mode and 8 times for double speed mode, and uses sample 8, 9 and 10 to decide data value. If more than 2 samples have low levels, the received bit is considered to a logic '0' and if more than 2 samples have high levels, the received bit is considered to a logic '1'. The data recovery process is then repeated until a complete frame is received including the first stop bit. The decided bit value is stored in the receive shift register in order. Note that the Receiver only uses the first stop bit of a frame. Internally, after receiving the first stop bit, the Receiver is in idle state and waiting to find start bit. (n = 10, 11, 12 and 13)

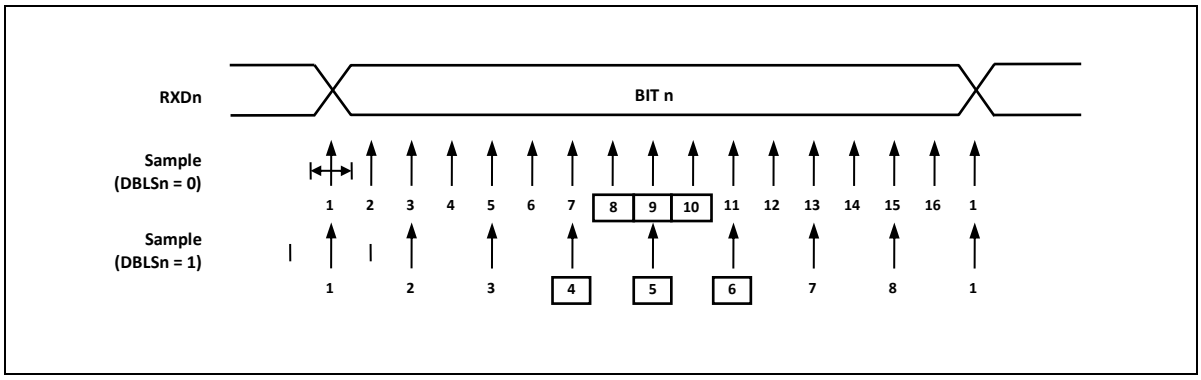


Figure 15.7. Asynchronous Sampling of Data and Parity Bit (n = 10, 11, 12 and 13)

The process for detecting stop bit is same as clock and data recovery process. That is, if 2 or more samples of 3 center values have high level, correct stop bit is detected, else a frame error (Fen) flag is set. After deciding whether the first stop bit is valid or not, the Receiver goes to idle state and monitors the RXDn line to check a valid high to low transition is detected (start bit detection). (n = 10, 11, 12 and 13)

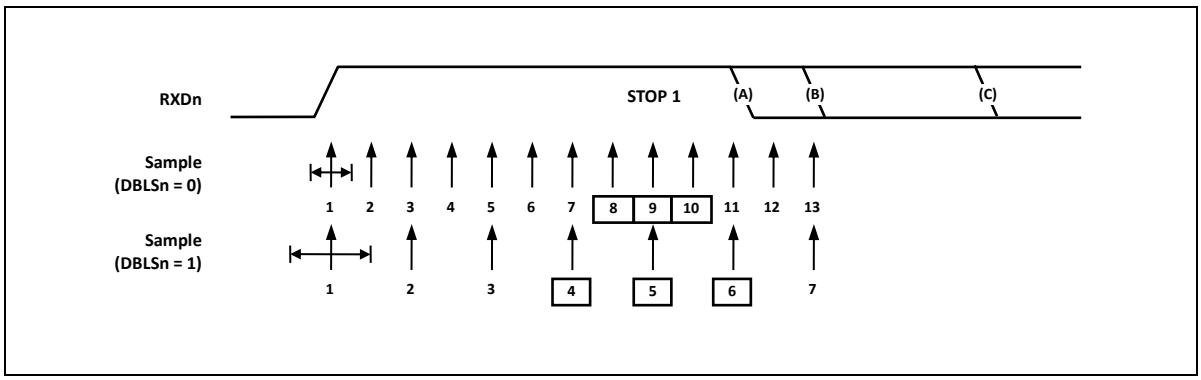


Figure 15.8. Stop Bit Sampling and Next Start Bit Sampling(n = 10, 11, 12 and 13)

15.4.8 SPI Mode

The USART can be set to operate in industrial standard SPI compliant mode. The SPI mode has the following features

- **Full Duplex, Three-wire synchronous data transfer.**
- **Mater and Slave Operation.**
- **Supports all four SPI modes of operation (mode 0, 1, 2, and 3).**
- **Selectable LSB first or MSB first data transfer.**
- **Double buffered transmit and receive.**
- **Programmable transmit bit rate.**

When SPI mode is enabled (USTnMS[1:0]=”11”), the slave select (SSn) pin becomes active LOW input in slave mode operation, or can be output in master mode operation if USTnSSEN bit is set to ‘0’.
Note that during SPI mode of operation, the pin RXDn is renamed as MISOn and TXDn is renamed as MOSIn for compatibility to other SPI devices. (n = 10, 11, 12 and 13)

15.4.9 SPI Clock Formats and Timing

To accommodate a wide variety if synchronous serial peripherals from different manufacturers, the USART has a clock polarity bit (CPOLn) and a clock phase control bit (CPHAn) to select one of four clock formats for data transfers. CPOLn selectively insert an inverter in series with the clock. CPHAn chooses between two different clock phase relationships between the clock and data. Note that CPHAn and CPOLn bits in USARTn_CR1 register have different meanings according to the USTnMS[1:0] bits which decides the operating mode of USART.
Table below shows four combinations of CPOLn and CPHAn for SPI mode 0, 1, 2, and 3. (n = 10, 11, 12 and 13)

Table 15.4 CPOL Functionality (n = 10 and 11)

SPIn Mode	CPOLn	CPHAn	Leading Edge	Trailing Edge
0	0	0	Sample (Rising)	Setup (Falling)
1	0	1	Setup (Rising)	Sample (Falling)
2	1	0	Sample (Falling)	Setup (Rising)
3	1	1	Setup (Falling)	Sample (Rising)

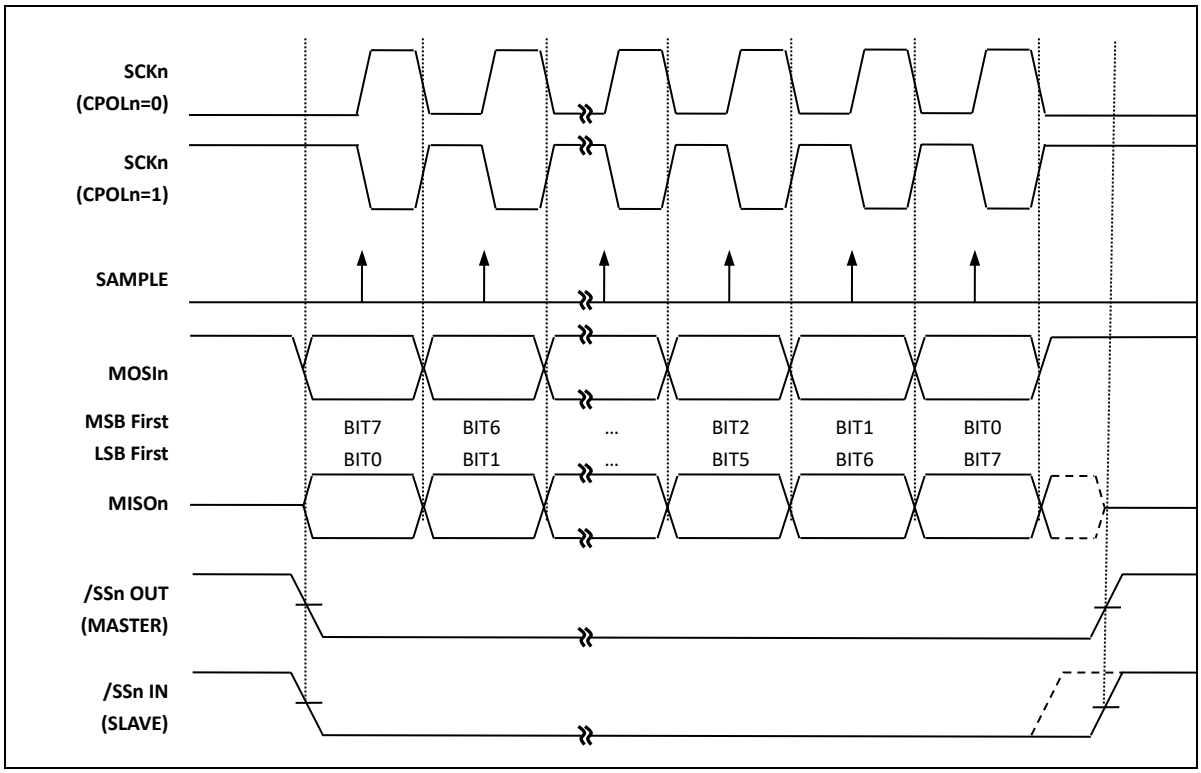


Figure 15.9. USART SPIn Clock Formats when CPHAn=0 (n = 10, 11, 12 and 13)

When CPHAn=0, the slave begins to drive its MISOn output with the first data bit value when SSn goes to active low. The first SCKn edge causes both the master and the slave to sample the data bit value on their MISOn and MOSIn inputs, respectively. At the second SCKn edge, the USART shifts the second data bit value out to the MOSIn and MISOn outputs of the master and slave, respectively. Unlike the case of CPHAn=1, when CPHAn=0, the slave's SSn input must go to its inactive high level between transfers. This is because the slave can prepare the first data bit when it detects falling edge of SSn input. (n = 10, 11, 12 and 13)

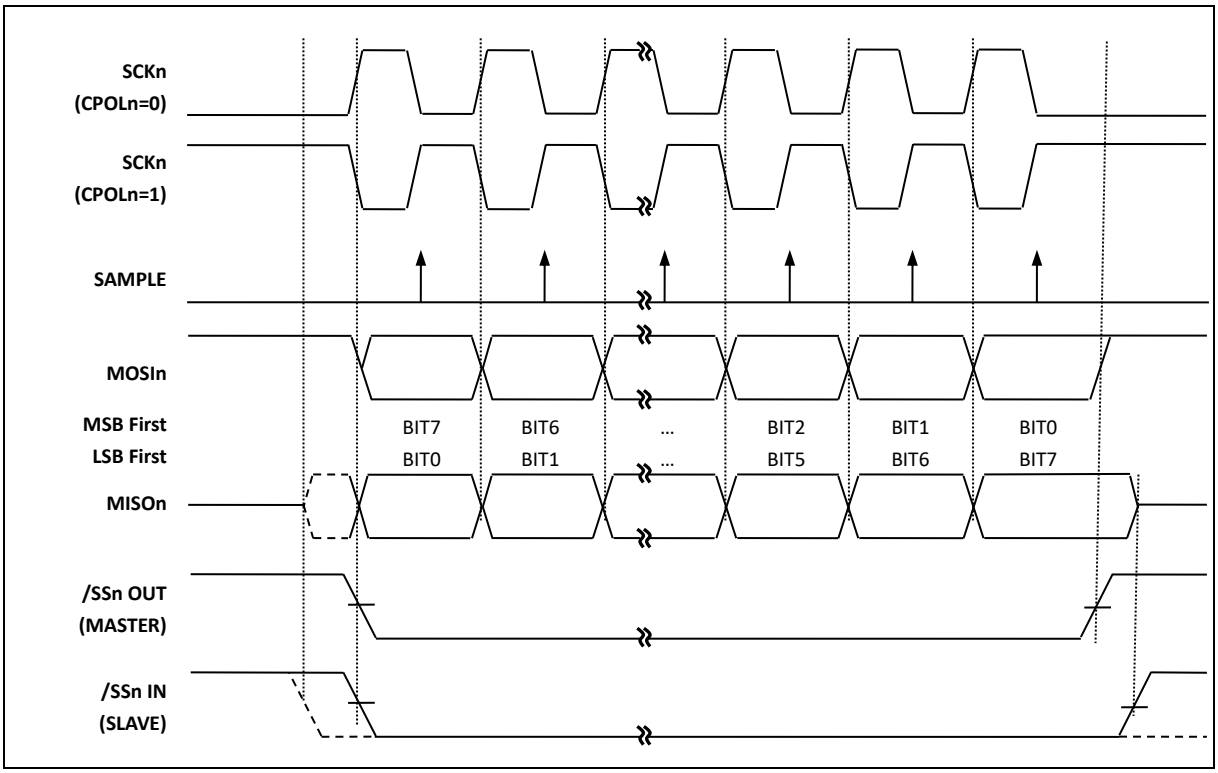


Figure 15.10. USART SPIn Clock Formats when CPHAn=1 (n = 10, 11, 12 and 13)

When CPHAn=1, the slave begins to drive its MISOn output when SSn goes active low, but the data is not defined until the first SCKn edge. The first SCKn edge shifts the first bit of data from the shifter onto the MOSIn output of the master and the MISOn output of the slave. The next SCKn edge causes both the master and slave to sample the data bit value on their MISOn and MOSIn inputs, respectively. At the third SCKn edge, the USART shifts the second data bit value out to the MOSIn and MISOn output of the master and slave respectively. When CPHAn=1, the slave's SSn input is not required to go to its inactive high level between transfers.

Because the SPIn logic reuses the USART resources, SPIn mode of operation is similar to that of synchronous or asynchronous operation. An SPIn transfer is initiated by checking for the USART Data Register Empty flag (DREn=1) and then writing a byte of data to the USARTn_DR Register. In master mode of operation, even if transmission is not enabled (TXEn=0), writing data to the USARTn_DR register is necessary because the clock SCKn is generated from transmitter block

CHAPTER 16. UNIVERSAL ASYNCHRONOUS RECEIVER/TRANSMITTER (UART)

16.1 OVERVIEW

2-channel UART (Universal Asynchronous Receiver/Transmitter) modules are provided. UART operation status including error status can be read from status register. The prescaler which generates proper baud rate, is exist for each UART channel. The prescaler can divide the UART clock source which is PCLK, from 1 to 65535. And baud rate generation is by clock which internally divided by 16 of the prescaled clock and 8-bit precision clock tuning function.

Programmable interrupt generation function will help to control the communication via UART channel

- Compatible with 16450
- Standard asynchronous control bit (start, stop, and parity) configurable
- Programmable 16-bit fractional baud generator
- Programmable serial communication
- 5-, 6-, 7- or 8- bit data transfer
- Even, odd, or no-parity bit insertion and detection
- 1-, 1.5- or 2-stop bit-insertion and detection
- 16-bit baud rate generation with 8-bit fraction control
- Hardware inter-frame delay function
- Stop bit error detection
- Detail status register

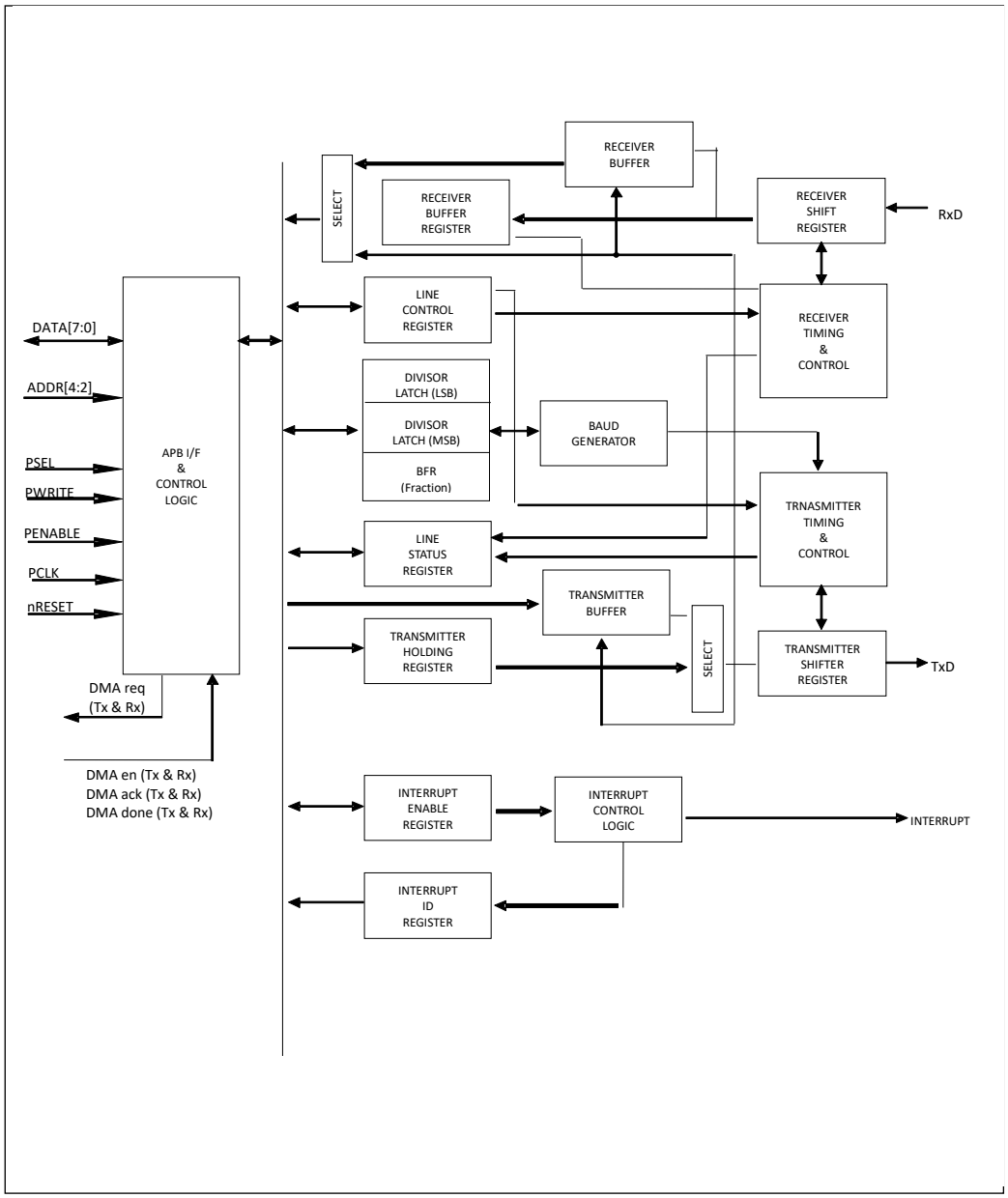


Figure16.1. Block diagram

16.2 Pin Description

Table 16.1 External pin (n = 0, 1)

PIN NAME	TYPE	DESCRIPTION
TXDn	O	UART Channel 0 transmit output
RXDn	I	UART Channel 0 receive input

16.3 REGISTERS

Base addresse of UART is as below.

Table 16.1 Base address of each port

NAME	BASE ADDRESS
UART0	0x4000_4000
UART1	0x4000_4100

Table 16.2 UART Register Map

Register Name	Offset	Access Type	Description	Initial Value	Ref
UARTn_RBR	0x00	RO	Receive data buffer register	0x0000_0000	16.3.1
UARTn_THR	0x00	WO	Transmit data hold register	0x0000_0000	16.3.2
UARTn_IER	0x04	RW	Interrupt enable register	0x0000_0000	16.3.3
UARTn_IIR	0x08	RO	Interrupt ID register	0x0000_0001	16.3.4
UARTn_LCR	0x0C	RW	Line control register	0x0000_0000	16.3.5
UARTn_DCR	0x10	RW	Data Control Register	0x0000_0000	16.3.6
UARTn_LSR	0x14	RO	Line status register	0x0000_0060	16.3.7
UARTn_BDR	0x20	RW	Baud rate Divisor Latch Register	0x0000_0000	16.3.8
UARTn_BFR	0x24	RW	Baud rate Fractional Counter Value	0x0000_0000	16.3.9
UARTn_IDTR	0x30	RW	Inter-frame Delay Time Register	0x0000_0080	16.3.10

Note: Where n = 0 and 1

16.3.1 UARTn_RBR UARTn Receive Data Buffer Register

UARTn Receive Data Buffer Register is 32-bit register. Received data will be read out from this register. Maximum length of data is 8 bits. Last data received will be maintained in this register until a new byte is received. This Register is able to 32/16/8-bit access. (n = 0 and 1)

UART0_RBR=0x4000_4000, UART1_RBR=0x4000_4100

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																								RBR							
-																								0x00							
-																								RO							

7	RBR	UARTn Receive Data Buffer bits
0		

16.3.2 UARTn_THR UARTn Transmit Data Hold Register

UARTn Receive Data Buffer Register is 32-bit register. This Register is able to 32/16/8-bit access. (n = 0 and 1)

UART0_THR=0x4000_4000, UART1_THR=0x4000_4100

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																								THR							
-																								0x00							
-																								WO							

7	THR	UARTn Transmit Data Hold bits
0		

16.3.3 UARTn_IER UARTn Interrupt Enable Register

UARTn Interrupt Enable Register is 32-bit register. This Register is able to 32/16/8-bit access. (n = 0 and 1)

UART0_IER=0x4000_4004, UART1_IER=0x4000_4104

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																												TXEIE	RLSIE	THREIE	DRIE
-																												0	0	0	0
-																												RW	RW	RW	RW

3	TXEIE	Transmit Register Empty Interrupt Enable.	
		0	Disable transmit register empty interrupt.
		1	Enable transmit register empty interrupt.
2	RLSIE	Receiver Line Status Interrupt Enable bit.	
		0	Disable receiver line status interrupt.
		1	Enable receiver line status interrupt.
1	THREIE	Transmit Holding Register Empty Interrupt Enable bit.	
		0	Disable transmit holding register empty interrupt.
		1	Enable transmit holding register empty interrupt.
0	DRIE	Data Receive Interrupt Enable bit.	
		0	Disable data receive interrupt.
		1	Enable data receive interrupt.

16.3.4 UARTn_IIR UARTn Interrupt ID Register

UARTn Interrupt ID Register is 32-bit register. This Register is able to 32/16/8-bit access. (n = 0 and 1)

UART0_IIR=0x4000_4008, UART1_IIR=0x4000_4108

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																											TXE	Reserved	IID		IPEN
-																											0	-	00		1
-																											RO	-	RO		RO

4	**TXE**	**Transmit Complete Interrupt Source ID bit.**
2	**IID**	**UARTn Interrupt ID bits.**
1		**Note)**
		1. The UARTn supports 3-priority interrupt generation and the interrupt source ID register shows one interrupt source which has highest priority among pending interrupts. The priority is defined as below.
		- Receive line status interrupt.
		- Receive data ready interrupt and Character timeout interrupt.
		- Transmit hold register empty interrupt.
0	**IPEN**	**Interrupt Pending bit.**
		0 Interrupt is pending.
		1 No interrupt is pending.

Table 16.3 Interrupt ID and control

Priority	TXE	IID		IPEN	Interrupt sources		
	Bit 4	Bit 2	Bit 1	Bit 0	Interrupt	Interrupt condition	Interrupt clear
-	0	0	0	1	None	-	-
1	0	1	1	0	Receiver Line Status	Overrun, Parity, Framing or Break Error	Read LSR register
2	0	1	0	0	Receiver Data Available	Receive data is available.	Read receive register or read IIR register
3	0	0	1	0	Transmitter Holding Register Empty	Transmit buffer empty	Write transmit hold register or read IIR register
4	1	X	X	X	Transmitter Register Empty	Transmit register empty	Write transmit hold register or read IIR register

Note)

1. After check the above bits, Read data buffer to avoid losing interrupt source.

16.3.5 UARTn_LCR UARTn Line Control Register

UARTn Line Control Register is 32-bit register. This Register is able to 32/16/8-bit access. (n = 0 and 1)

UART0_LCR=0x4000_400C, UART1_LCR=0x4000_410C

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																									BREAK	STICKP	PARITY	PEN	STOPBIT	DLEN	
-																									0	0	0	0	0	00	
-																									RW	RW	RW	RW	RW	RW	

6	BREAK	Transfer Break Control bit. The TXDn pin will be driven at low state in order to notice the alert to the receiver.
	0	Normal transfer mode.
	1	Break transmit mode.
5	STICKP	Force Parity bit. This bit is effective when the PEN bit is set to “1b”.
	0	Disable parity stuck.
	1	Enable parity stuck. A parity is always the value of the PARITY bit.
4	PARITY	Parity Mode and Parity Stuck Selection bit.
	0	Odd parity mode.
	1	Even parity mode.
3	PEN	Parity Bit Transfer Enable bit.
	0	Disable parity transfer.
	1	Enable parity transfer.
2	STOPBIT	Stop Bit Length Selection bit.
	0	1 stop bit.
	1	1.5 or 2 stop bit. 1.5 stop bit in case of 5-bit data length and 2 stop bit in case of 6/7/8-bit data length.
1 0	DLEN	Data Length Selection bits.
	00	5-bit data length
	01	6-bit data length
	10	7-bit data length
	11	8-bit data length

Parity bit will be generated according to bit 3,4,5 of UARTn_LCR register. The table shows the variation of parity bit generation.

Table 16.4 Interrupt ID and control

STICKP	PARITY	PEN	Parity
X	X	0	No Parity
0	0	1	Odd Parity
0	1	1	Even Parity
1	0	1	Force parity as “1”
1	1	1	Force parity as “0”

16.3.6 UARTn_DCR UARTn Data Control Register

UARTn Data Control Register is 32-bit register. This Register is able to 32/16/8-bit access. (n = 0 and 1)

UART0_RBR=0x4000_4010, UART1_RBR=0x4000_4110

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																											LBON	RXINV	TXINV	Reserved		
-																											0	0	0	-		
-																											RW	RW	RW	-		

4	LBON	Local Loopback Test Mode Enable bit.
	0	Normal mode.
	1	Local loopback mode. TXDn connected to RXDn internally.
3	RXINV	Receive Data Inversion Selection bit.
	0	Normal receive data input.
	1	Inverted receive data input.
2	TXINV	Transmit Data Inversion Selection bit.
	0	Normal transmit output.
	1	Inverted transmit output.

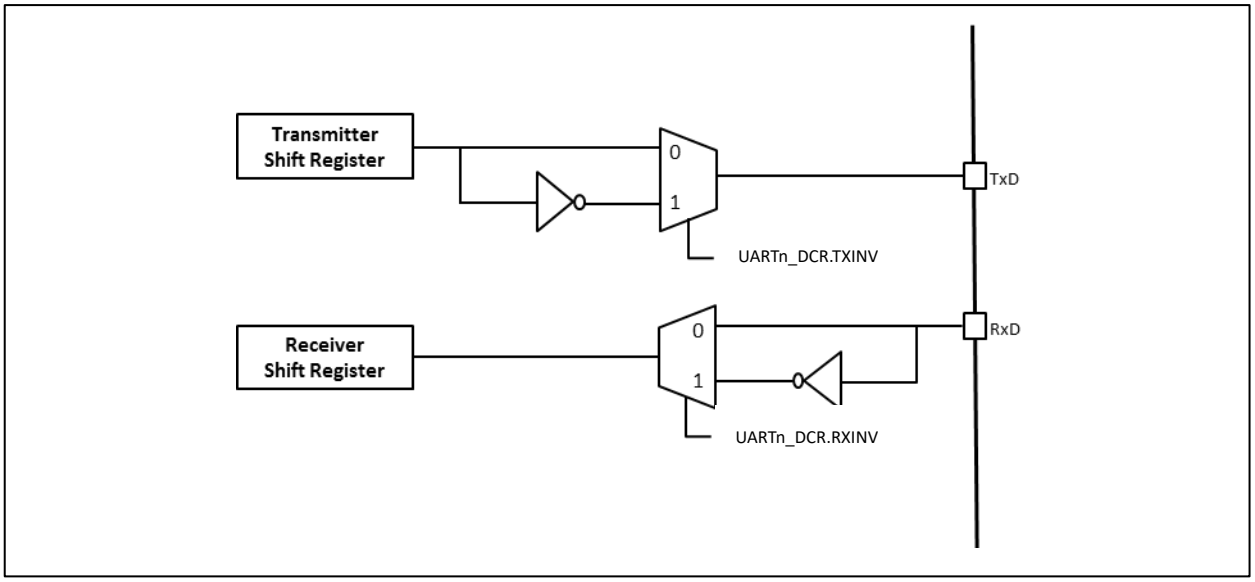


Figure 13.2. Data inversion control diagram

16.3.7 UARTn_LSR UARTn Line Status Register

UARTn Line Status Register is 32-bit register. This Register is able to 32/16/8-bit access. (n = 0 and 1)

UART0_LSR=0x4000_4014, UART1_LSR=0x4000_4114

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																									TEMT	THRE	BI	FE	PE	OE	DR
-																									1	1	0	0	0	0	0
-																									RO	RO	RO	RO	RO	RO	RO

6	TEMT	Transmit Empty bit.
		0 Transmit register has data or is transferring.
		1 Transmit register is empty.
5	THRE	Transmit Holding Empty bit.
		0 Transmit holding register is not empty.
		1 Transmit holding register is empty
		Note) 1. This bit will be set to “1b” when it starts transmit.
4	BI	Break Condition Indication bit.
		0 Normal status.
		1 Break condition is detected.
3	FE	Frame Error Indicator bit.
		0 No frame error.
		1 Frame error occurs. The receive character did not have a valid stop bit.
2	PE	Parity Error Indicator bit.
		0 No parity error.
		1 Parity error occurs. The receive character have not correct parity information.
1	OE	Overrun Error Indicator bit.
		0 No overrun error.
		1 Overrun error occurs. Additional data arrive while the RHR is full.
0	DR	Data Receive Indicator bit.
		0 No data in receive holding register.
		1 Data has been received and is saved in the receive holding register.

This register provides the status of data transfers between transmitter and receiver. User can get the line status information from this register and can handle the next process. Bit 1,2,3,4 will arise the line status interrupt when RLSIE bit in UARTn_IER register is set. Other bits can generate its interrupt when its interrupt enable bit in UARTn_IER register is set.

16.3.8 UARTn_BDR UARTn Baud Rate Divisor Latch Register

UARTn Baud Rate Divisor Latch Register is 32-bit register. This Register is able to 32/16/8-bit access. (n = 0 and 1)

UART0_BDR=0x4000_4020, UART1_BDR=0x4000_4120

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																BDR															
-																0x0000															
-																RW															

15 0	BDR	Baud Rate Divider Latch Value Baud rate = fUARTnCLK/(16 x BDR[15:0] x 2). Note) 1. The UART block won't work if the BDR[15:0] ≤ 0x0003.

To establish the communication with UART channel, the baud rate should be set properly. The programmable baud rate generate is provided to give from 1 to 65535 divider number. The 16 bit divider register (UARTn_BDR) should be written for expected baud rate. $UART_{clock}$ is PCLK.

Baud rate calculation formula is below.

$$\mathrm{BDR} = \frac{UART_{clock}}{16 \times BaudRate \times 2}$$

In case of 48 MHz $UART_{clock}$ speed, the divider value and error rate is described in table

Table 16.5 Example of baud rate calculation (without BFR)

$UART_{clock}$=48 MHz		
Baud rate	**Divider**	**Error (%)**
1200	1250	0.0%
2400	625	0.0%
4800	312	0.16%
9600	156	0.16%
19200	78	0.16%
38400	39	0.16%
57600	26	0.16%
115200	13	0.16%

16.3.9 UARTn_BFR UARTn Baud Rate Fraction Counter Register

UARTn Baud Rate Fraction Counter Register is 32-bit register. This Register is able to 32/16/8-bit access. (n = 0 and 1)

UART0_BFR=0x4000_4024, UART1_BFR=0x4000_4124

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																								BFR							
-																								0x00							
-																								RW							

7 0	BFR	Fraction Counter value. 0 Disable fraction counter. N Fraction compensation mode is operating. Fraction counter is incremented by FCNT. Note) 1. 8-bit fractional counter will count up by FCNT value every (baud rate)/16 period and whenever fractional counter overflow is happen, the divisor value will increment by 1. So this period will be compensated. Then next period, the divisor value will return to original set value.

Table 16.6 Example of baud rate calculation

$UART_{clock}$ =48 MHz			
Baud rate	Divider	FCNT	Error (%)
1200	1250	0	0.00%
2400	625	0	0.00%
4800	312	128	0.00%
9600	156	64	0.00%
19200	78	32	0.00%
38400	39	16	0.00%
57600	26	10	0.01%
115200	13	5	0.01%

$$\mathrm{FCNT} = \mathrm{Float} * 256$$

FCNT value can calculated above equation. For example, the target baud rate is 4800 bps and $UART_{clock}$ is 40MHz case, the BDR value is 520.8333. The integer number 520 should be the BDR value and the floating number 0.8333 will make the FNCT value as below.

FCNT = 0.8333 * 256 = 213.3333, so the FCNT value is 213.

8-bit fractional counter will count up by FCNT value every (baud rate)/16 periods and whenever fractional counter overflow is happen, the divisor value will increment by 1. So this period will be compensated. Then next period, the divisor value will return to original set value.

16.3.10 UARTn_IDTR UARTn Inter-Frame Delay Time Register

UARTn Inter-Frame Delay Time Register is 32-bit register. This Register is able to 32/16/8-bit access. (n = 0 and 1)

UART0_IDTR=0x4000_4030, UART1_IDTR=0x4000_4130

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																								SMS	DMS	Reserved			WAITVAL		
-																								1	0	-			000		
-																								RW	RW	-			RW		

7	SMS	Start Bit Multi Sampling Enable bit.
		0 Multi sampling is disable for start bit, Single sample will be done at 8/16 baud rate for the start bit.
		1 Multi sampling is enabled for start bit. Sampling is done 3 times at 7/16, 8/16 and 9/16 baud rate. Dominant value of 3 samples will be selected for the start bit.
6	DMS	Data Bit Multi sampling enable.
		0 Multi sampling is disable for data bit, Single sample will be done at 8/16 baud rate for the data bit.
		1 Multi sampling is enabled for data bit. Sampling is done 3 times at 7/16, 8/16 and 9/16 baud rate. Dominant value of 3 samples will be selected for the data bit.
2 0	WAITVAL	Wait Time Value. Dummy delay can be inserted between 2 Continuous Transmits.
		Wait Time = WAITVAL[2:0]/(Baud Rate)

16.4 Functional Description

The UART module is compatible with 16450 UART. Additionally fractional baud rate compensation logic is provided. It doesn't have internal FIFO block. So data transfer will establish interactively support.

16.4.1 Receiver Sampling Timing

The UARTs operates as following timing.

If the falling edge on the receive line, UART judges as the start bit. From the start timing, UART oversamples 16 times of 1-bit and detect the bit value at the 7th sample of 16 samples.

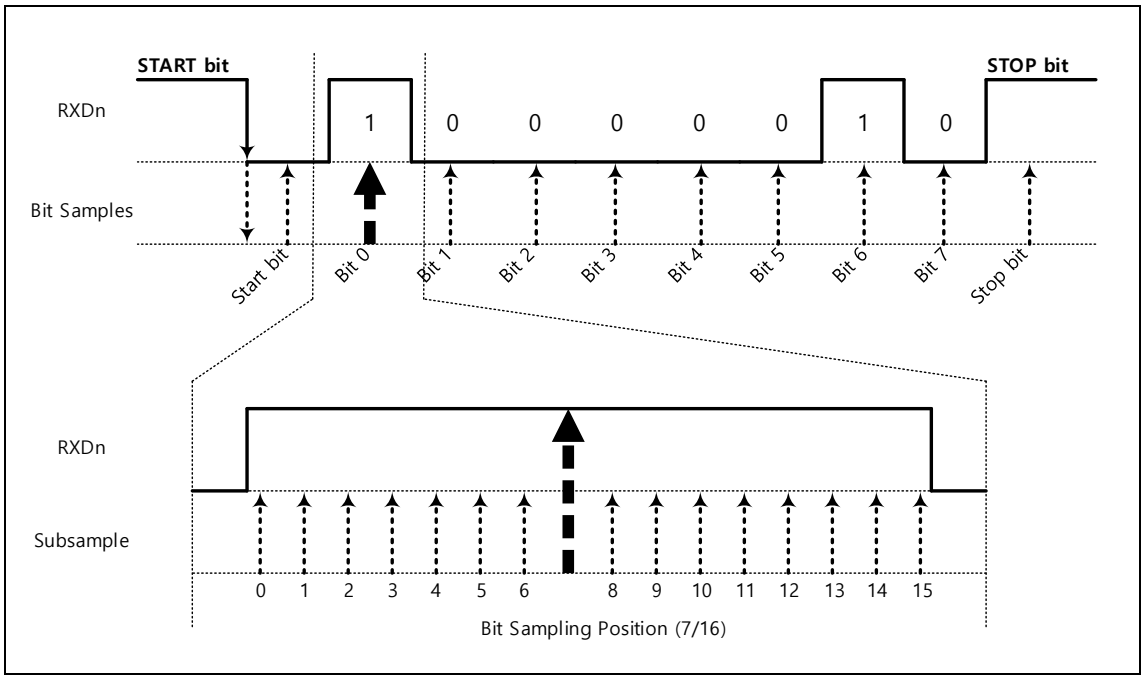


Figure 16.3 The Sampling Timing of UART Receiver

1. It is recommended to enable debounce settings in the PCU block to reinforce the immunity of external glitch noise.

16.4.2 Transmitter

The transmitter has data transmit function. The start bit, data bits, optional parity bit and stop bit are serially shifted, least significant bit first.

The number of data bit is selected in the DLAN[1:0] filed in UARTn_LCR register.

The parity bit is set according to the PARITY and PEN bit filed in UARTn_LCR register. If the parity type is even then the parity bit depends on the one bit sum of all data bits. For odd parity, the parity bit is the inverted sum of all data bits.

The number of stop bits is selected in the STOPBIT filed in UARTn_LCR register.

The example of transmit data format is below.

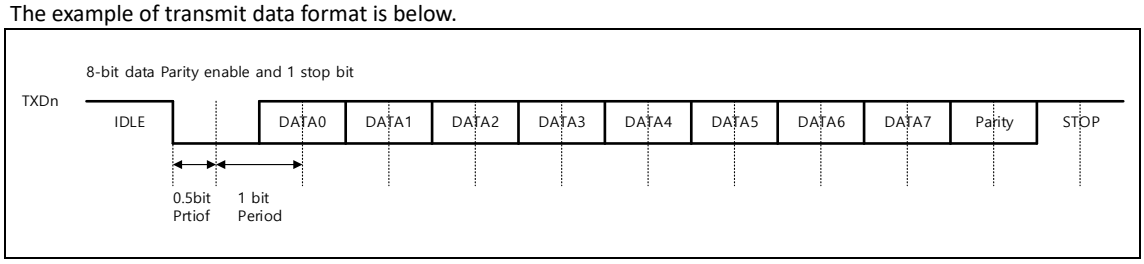


Figure 16.4 Transmit data format example

16.4.3 Inter-frame delay transmission

The inter-frame delay function allows the transmitter to insert an idle state on the TXD line between 2 characters. The width of the idle state is defined in WAITVAL field in UARTn_IDTR register. When this field is set 0, no time-delay is generated. Otherwise, the transmitter holds a high level on TXD after each transmitted character during the number of bit periods defined in WATIVAL field.

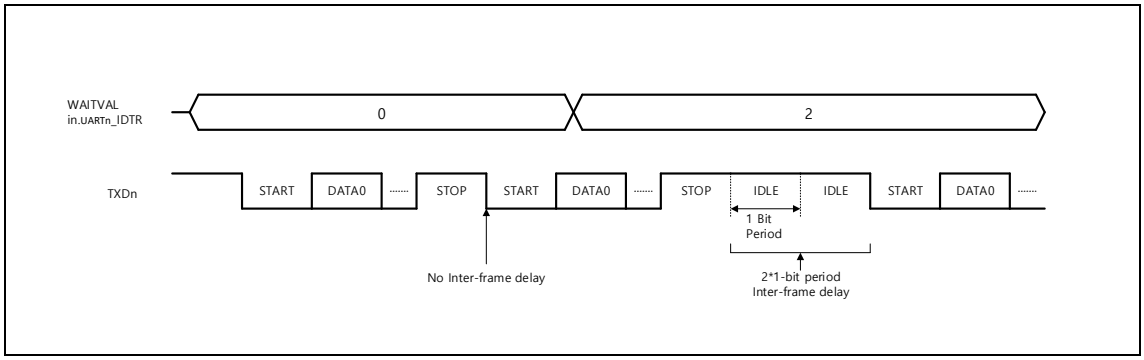


Figure 16.5 Inter-frame delay timing diagram

16.4.4 Transmit Interrupt

The transmit operation makes some kind of interrupt flags. When transmitter holding register is empty, the THRE interrupt flag will be set. When transmitter shifter register is empty, the TXE interrupt flag will be set. User can select which interrupt timing is best for the application.

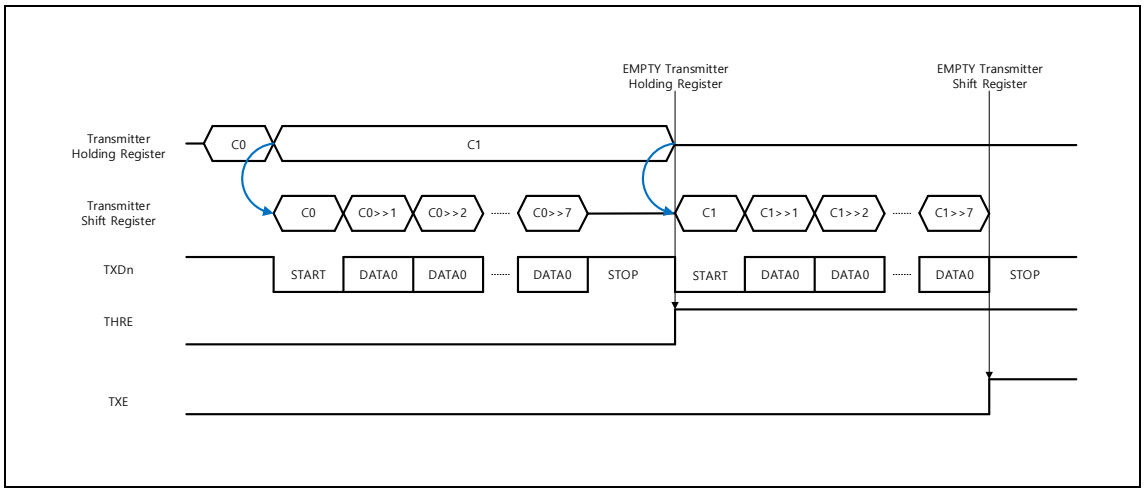


Figure 16.6 Transmit interrupt timing diagram

16.4.5 DMA Transfers

The UART support DMA interface function. It is optionally provided depends on the device. The start memory address for transfer data and the length of transfer data are programmd in the registers in DMA block.
The end of transfer is notified related transfer done flag.
The transmit with DMA operation will invoke the DMA TX done flag DTX.UnIIR and will set DMA TX done interrupt ID when all the transmit data are written to transmit holding register. 2 transmit data are remained in registers in UART block after DMA transfer done interrupt.
The receive with DMA operation will invoke the DMA RX done flag RXT.UnIIR and will set DMA RX done interrupt ID when all the receive data are written to the destination memory. So, UART RXD signal is already IDLE state when the DMA RX done interrupt is issued.

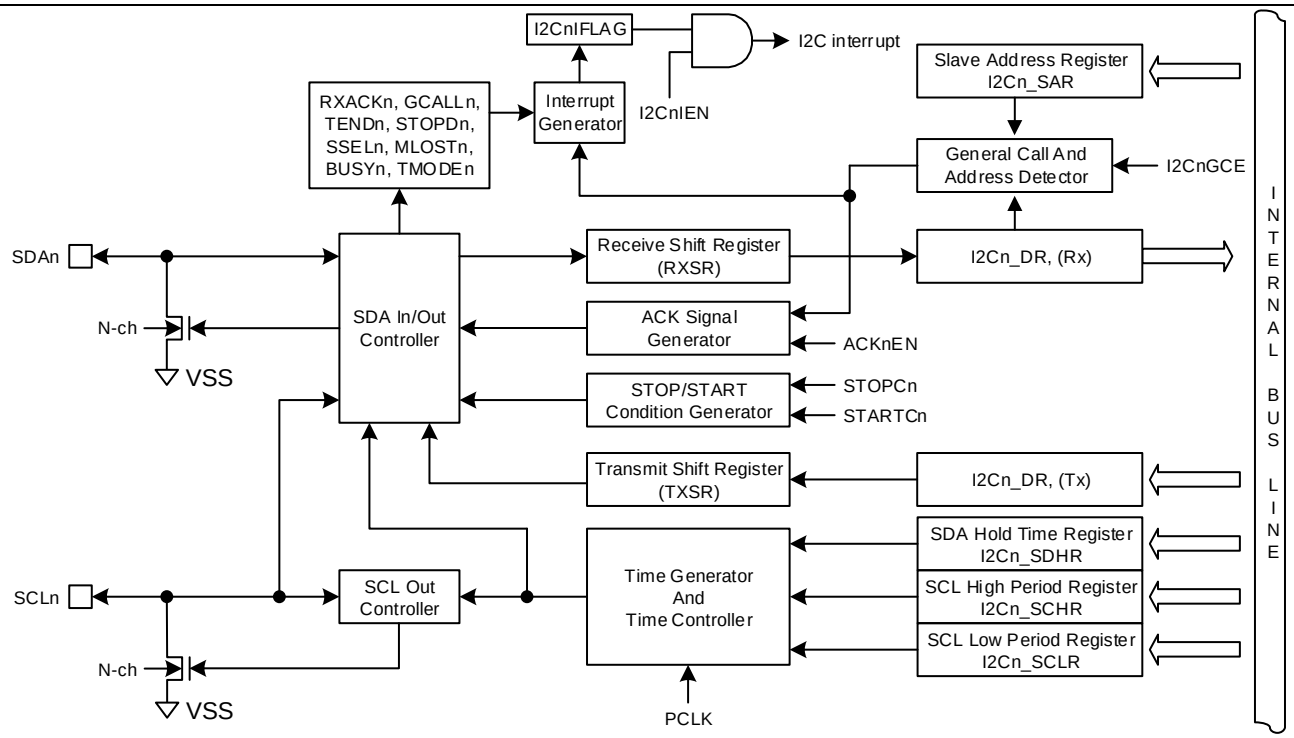
CHAPTER 17. I²C Interface

17.1 OVERVIEW

The I2C is one of industrial standard serial communication protocols, and which uses 2 bus lines Serial Data Line (SDAn) and Serial Clock Line (SCLn) to exchange data. Because both SDAn and SCLn lines are open-drain output, each line needs pull-up resistor. The features are as shown below. (n = 0 and 1)

- Compatible with I2C bus standard.
- Multi-master operation.
- Up to 400kHz data transfer read speed.
- 7-bit address.
- Support two slave address.
- Both master and slave operation.
- Bus busy detection

Figure shows the block diagram of a I2C block



Note: When the corresponding port of I2C is a sub-function for SCL/SDA pin, the SCL/SDA pins are automatically set to the N-channel open-drain outputs and the input latch is read in the case of reading the pins. The corresponding pull-up resistor is determined by the control register.

Figure 17.1. I2C Block diagram

17.2 Pin Description

Table 17.1 External pin (n = 0, 1, 2)

PIN NAME	TYPE	DESCRIPTION
SCL0(PF6)	I/O	I2C channel 0 Serial clock bus line (open-drain)
SDA0(PF7)	I/O	I2C channel 0 Serial data bus line (open-drain)
SCLn	I/O	I2C channel n Serial clock bus line
SDAn	I/O	I2C channel n Serial data bus line

17.3 REGISTERS

Base addresse of I²C is as below.

Table 17.1 I²C interface base address

NAME	BASE ADDRESS
I²C0	0x4000_4800
I²C1	0x4000_4900
I²C2	0x4000_4A00

Table 17-2 I²C register map

Register Name	Offset	Access Type	Description	Initial Value	Ref
I2Cn_CR	0x00	RW	I2Cn Control Register	0x0000_0000	17.3.1
I2Cn_ST	0x04	RW	I2Cn Status Register	0x0000_0000	17.3.2
I2Cn_SAR1	0x08	RW	I2Cn Slave Address Register 0	0x0000_0000	17.3.3
I2Cn_SAR2	0x0C	RW	I2Cn Slave Address Register 1	0x0000_0000	17.3.4
I2Cn_DR	0x10	RW	I2Cn Data Register	0x0000_0000	17.3.5
I2Cn_SDHR	0x14	RW	I2Cn SDA Hold Time Register	0x0000_0001	17.3.6
I2Cn_SCLR	0x18	RW	I2Cn SCL Low Period Register	0x0000_003F	17.3.7
I2Cn_SCHR	0x1C	RW	I2Cn SCL High Period Register	0x0000_003F	17.3.8

Note: Where n = 0, 1, and 2

17.3.1 I2Cn_CR I2Cn Control Register

The register can be set to configure I2C operation mode and simultaneously allowed for I2C transactions to be kicked off. I2Cn Control Register Register is 32-bit register. This Register is able to 32/16/8-bit access. (n = 0, 1 and 2)

I2C0_CR=0x4000_4800, I2C1_CR=0x4000_4900, I2C2_CR=0x4000_4A00

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																								I2CnEN	TXDLYENBn	I2CnIEN	I2CnIFLAG	ACKnEN	IMASTERn	STOPCn	STARTCn
-																								0	0	0	0	0	0	0	0
-																								RW	RW	RW	RO	RW	RO	RW	RW

7	I2CnEN	Activate I2Cn Block by supplying.
		0 Disable I2Cn block.
		1 Enable I2Cn block.
6	TXDLYENBn	I2CnSDHR Register Control bit.
		0 Enable I2Cn_SDHR register.
		1 Disable I2Cn_SDHR register.
5	I2CnIEN	I2Cn Interrupt Enable bit.
		0 Disable I2Cn interrupt.
		1 Enable I2Cn interrupt.
4	I2CnIFLAG	I2Cn Interrupt Flag bit. This bit is cleared when all interrupt source bits in the I2Cn_ST register are cleared to “0b”.
		0 No request occurred.
		1 Request occurred.
3	ACKnEN	Controls ACK signal generation at ninth SCL period.
		0 No ACK signal is generated. (SDA = 1)
		1 ACK signal is generated. (SDA = 0)
		Notes) ACK signal is output (SDA = 0) for the following 3 cases. Where x = 0 and 1. 1. When received address packet equals to SLAx[6:0] bits in I2CnSARx register. 2. When received address packet equals to value 0x00 with GCALLn enabled. 3. When I2Cn operates as a receiver (master or slave)
2	IMASTERn	Represent Operation Mode of I2Cn. This bit is cleared to “0b” on STOP condition.
		0 I2Cn is in slave mode.
		1 I2Cn is in master mode.
1	STOPCn	STOP Condition Generation When I2Cn is master.
		0 No effect.
		1 STOP condition is to be generated.
0	STARTCn	START Condition Generation When I2Cn is master.
		0 No effect.
		1 START or Repeated START condition is to be generated.

17.3.2 I2Cn_ST I2Cn Status Register

I2Cn Status Register Register is 32-bit register. This Register is able to 32/16/8-bit access. (n = 0, 1 and 2)

I2C0_ST=0x4000_4804, I2C1_ST=0x4000_4904, I2C2_ST=0x4000_4A04

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																								GCALLn	TENDn	STOPDn	SSELn	MLOSTn	BUSYn	TMODEn	RXACKn
-																								0	0	0	0	0	0	0	0
-																								RW	RW	RW	RW	RW	RW	RO	RW

7	GCALLn	This bit has different meaning depending on whether I2C is master or slave. When I2C is a master, this bit represents whether it received AACK (address ACK) from slave.
	0	No AACK is received. (Master mode)
	1	AACK is received (Master mode). It may be set to “1b” after address transmission.
	When I2C is a slave, this bit is used to indicate general call.	
	0	General call address is not detected. (Slave mode)
	1	General call address is detected. (Slave mode)
6	TENDn	This bit is set when 1-byte of data is transferred completely.
	0	1 byte of data is not completely transferred.
	1	1 byte of data is completely transferred.
5	STOPDn	This bit is set when a STOP condition is detected.
	0	A STOP condition is not detected.
	1	A STOP condition is detected.
4	SSELn	This bit is set when I2C is addressed by other master.
	0	I2C is not selected as a slave.
	1	I2C is addressed by other master and acts as a slave.
3	MLOSTn	This bit represents the result of bus arbitration in master mode.
	0	I2C maintains bus mastership.
	1	I2C has lost bus mastership during arbitration process.
2	BUSYn	This bit reflects bus status.
	0	I2C bus is idle, so a master can issue a START condition.
	1	I2C bus is busy.
1	TMODEn	This bit is used to indicate whether I2C is transmitter or receiver.
	0	I2C is a receiver.
	1	I2C is a transmitter.
0	RXACKn	This bit shows the state of ACK signal.
	0	No ACK is received.
	1	ACK is received at ninth SCL period.

Notes)

1. The GCALLn, TENDn, STOPDn, SSELn, and MLOSTn bits can be source of interrupt.
2. When an I2C interrupt occurs except for deep sleep mode, the SCL line is held low. To release SCL, Clear to “0b” all interrupt source bits in I2Cn_ST register.
3. The GCALLn, TENDn, STOPDn, SSELn, MLOSTn, and RXACKn bits are cleared when “1b” is written to the corresponding bit.

17.3.3 I2Cn_SAR1 I2Cn Slave Address Register 1

I2Cn Slave Address Register 1 is 32-bit register. This Register is able to 32/16/8-bit access. (n = 0, 1 and 2)

I2C0_SAR1=0x4000_4808, I2C1_SAR1=0x4000_4908, I2C2_SAR1=0x4000_4A08

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																								SLAn							GCALLnEN
-																								0000_000							0
-																								RW							RW

7 1	SLAn	These bits configure the slave address 0 in slave mode.
0	GCALLnEN	This bit decides whether I2Cn allows general call address 0 or not in I2Cn slave mode.
		0 Ignore general call address 0.
		1 Allow general call address 0.

17.3.4 I2Cn_SAR2 I2Cn Slave Address Register 2

I2Cn Slave Address Register 2 is 32-bit register. This Register is able to 32/16/8-bit access. (n = 0, 1 and 2)

I2C0_SAR2=0x4000_480C, I2C1_SAR2=0x4000_490C, I2C2_SAR2=0x4000_4A0C

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																								SLAn							GCALLnEN
-																								0000_000							0
-																								RW							RW

7 1	SLAn	These bits configure the slave address 1 in slave mode.
0	GCALLnEN	This bit decides whether I2Cn allows general call address 1 or not in I2Cn slave mode.
		0 Ignore general call address 1.
		1 Allow general call address 1.

17.3.5 I2Cn_DR I2Cn Data Register

I2Cn Data Register is 32-bit register. This Register is able to 32/16/8-bit access. (n = 0, 1 and 2)

I2C0_DR=0x4000_4810, I2C1_DR=0x4000_4910, I2C2_DR=0x4000_4A10

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																								DATA							
-																								0x00							
-																								RW							

7 0	DATA	The I2Cn_DR Transmit buffer and Receive buffer share the same I/O address with this DATA register. The Transmit Data Buffer is the destination for data written to the I2Cn_DR register. Reading the I2Cn_DR register returns the contents of the Receive Buffer.

17.3.6 I2Cn_SDHR I2Cn SDA Hold Time Register

I2Cn SDA Hold Time Register is 32-bit register. This Register is able to 32/16/8-bit access. (n = 0, 1 and 2)

I2C0_SDHR=0x4000_4814, I2C1_SDHR=0x4000_4914, I2C2_SDHR=0x4000_4A14

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																				HLDT											
-																				0x001											
-																				RW											

11 0	HLDT	This register is used to control SDA output timing from the falling edge of SCL. Note that SDA is changed after tPCLK X (I2Cn_SDHR+2). In master mode, load half the value of I2Cn_SCLR to this register to make SDA change in the middle of SCL. In slave mode, configure this register regarding the frequency of SCL from master. The SDA is changed after tPCLK X (I2Cn_SDHR+2) in master mode. So, to insure operation in slave mode, the value tPCLK X (I2Cn_SDHR + 2) must be smaller than the period of SCL.

17.3.7 I2Cn_SCLR I2Cn SCL Low Period Register

I2Cn SCL Low Period Register is 32-bit register. This Register is able to 32/16/8-bit access. (n = 0, 1 and 2)

I2C0_SCLR=0x4000_4818, I2C1_SCLR=0x4000_4918, I2C2_SCLR=0x4000_4A18

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																				SCLL											
-																				0x03F											
-																				RW											

11 0	SCLL	This register defines the low period of SCL in master mode. The base clock is PCLK and the period is calculated by the formula: tPCLK X (4 X I2Cn_SCLR + 2) where tPCLK is the period of PCLK.

17.3.8 I2Cn_SCHR I2Cn SCL High Period Register

I2Cn SCL High Period Register is 32-bit register. This Register is able to 32/16/8-bit access. (n = 0, 1 and 2)

I2C0_SCHR=0x4000_481C, I2C1_SCHR=0x4000_491C, I2C2_SCHR=0x4000_4A1C

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																				SCLH											
-																				0x03F											
-																				RW											

11 0	SCLH	This register defines the high period of SCL in master mode. The base clock is PCLK and the period is calculated by the formula: tPCLK X (4 X I2Cn_SCHR + 2) where tPCLK is the period of PCLK.

17.4 Functional Description

17.4.1 I2C bit transfer

The data on the SDAn line must be stable during HIGH period of the clock, SCLn. The HIGH or LOW state of the data line can only change when the clock signal on the SCLn line is LOW. The exceptions are START(S), repeated START(Sr) and STOP(P) condition where data line changes when clock line is high.

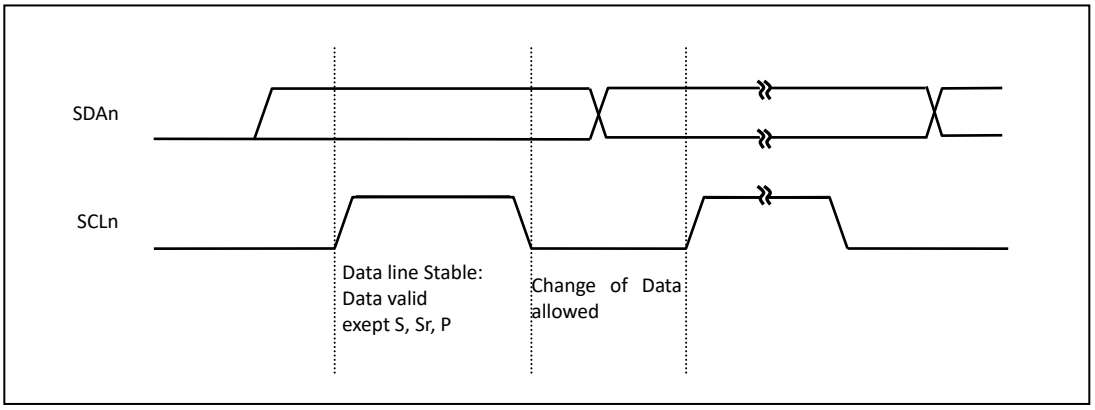


Figure 17.2 I2C Bus bit transfer (n = 0, 1 and 2)

17.4.2 START/Repeated START/STOP

One master can issue a START (S) condition to notice other devices connected to the SCLn, SDAn lines that it will use the bus. A STOP (P) condition is generated by the master to release the bus lines so that other devices can use it.

A high to low transition on the SDAn line while SCLn is high defines a START (S) condition.

A low to high transition on the SDAn line while SCLn is high defines a STOP (P) condition.

START and STOP conditions are always generated by the master. The bus is considered to be busy after START condition. The bus is considered to be free again after STOP condition, ie, the bus is busy between START and STOP condition. If a repeated START condition (Sr) is generated instead of STOP condition, the bus stays busy. So, the START and repeated START conditions are functionally identical.

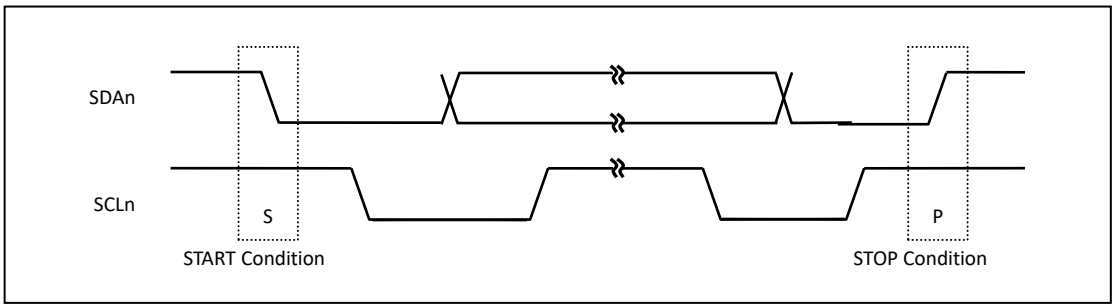


Figure 17.3 START and STOP condition (n = 0, 1 and 2)

17.4.3 Data Transfer

Every byte put on the SDAn line must be 8-bits long. The number of bytes that can be transmitted per transfer is unlimited. Each byte has to be followed by an acknowledge bit. Data is transferred with the most significant bit (MSB) first. If a slave can't receive or transmit another complete byte of data until it has performed some other function, it can hold the clock line SCLn LOW to force the master into a wait state. Data transfer then continues when the slave is ready for another byte of data and releases clock line SCLn.

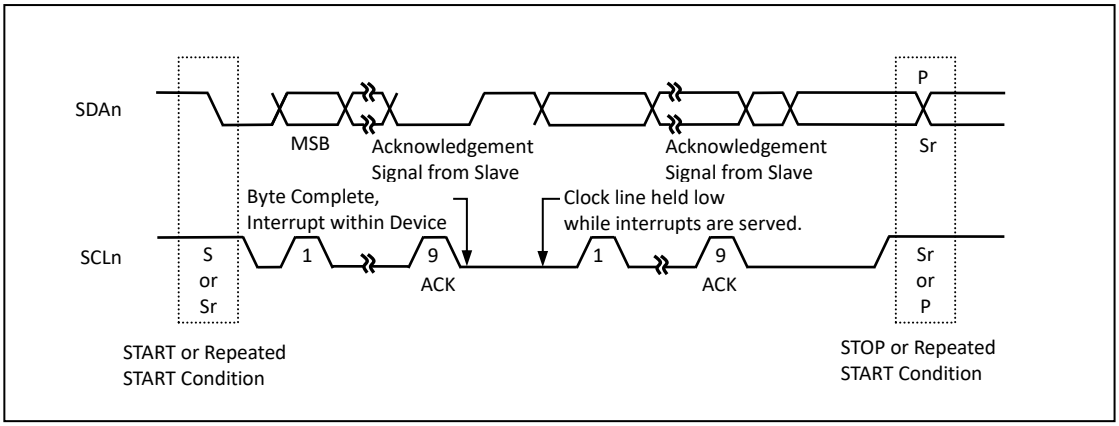


Figure 17.4 I2C Bus data transfer (n = 0, 1 and 2)

17.4.4 Acknowledge

The acknowledge related clock pulse is generated by the master. The transmitter releases the SDAn line (HIGH) during the acknowledge clock pulse. The receiver must pull down the SDAn line during the acknowledge clock pulse so that it remains stable LOW during the HIGH period of this clock pulse. When a slave is addressed by a master (Address Packet), and if it is unable to receive or transmit because it's performing some real time function, the data line must be left HIGH by the slave. And also, when a slave addressed by a master is unable to receive more data bits, the slave receiver must release the SDAn line (Data Packet). The master can then generate either a STOP condition to abort the transfer, or a repeated START condition to start a new transfer.

If a master receiver is involved in a transfer, it must signal the end of data to the slave transmitter by not generating an acknowledge on the last byte that was clocked out of the slave. The slave transmitter must release the data line to allow the master to generate a STOP or repeated START condition.

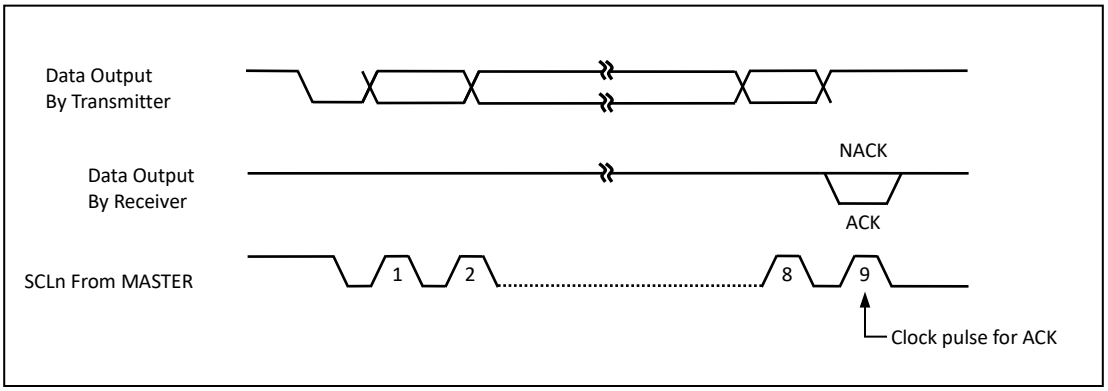


Figure 17.5 I2C bus acknowledge (n = 0, 1 and 2)

17.4.5 Synchronization/ Arbitration

Clock synchronization is performed using the wired-AND connection of I2C interfaces to the SCLn line. This means that a HIGH to LOW transition on the SCLn line will cause the devices concerned to start counting off their LOW period and it will hold the SCLn line in that state until the clock HIGH state is reached. However the LOW to HIGH transition of this clock may not change the state of the SCLn line if another clock is still within its LOW period. In this way, a synchronized SCLn clock is generated with its LOW period determined by the device with the longest clock LOW period, and its HIGH period determined by the one with the shortest clock HIGH period.

A master may start a transfer only if the bus is free. Two or more masters may generate a START condition. Arbitration takes place on the SDAn line, while the SCLn line is at the HIGH level, in such a way that the master which transmits a HIGH level, while another master is transmitting a LOW level will switch off its DATA output state because the level on the bus doesn't correspond to its own level. Arbitration continues for many bits until a winning master gets the ownership of I2C bus. Its first stage is comparison of the address bits.

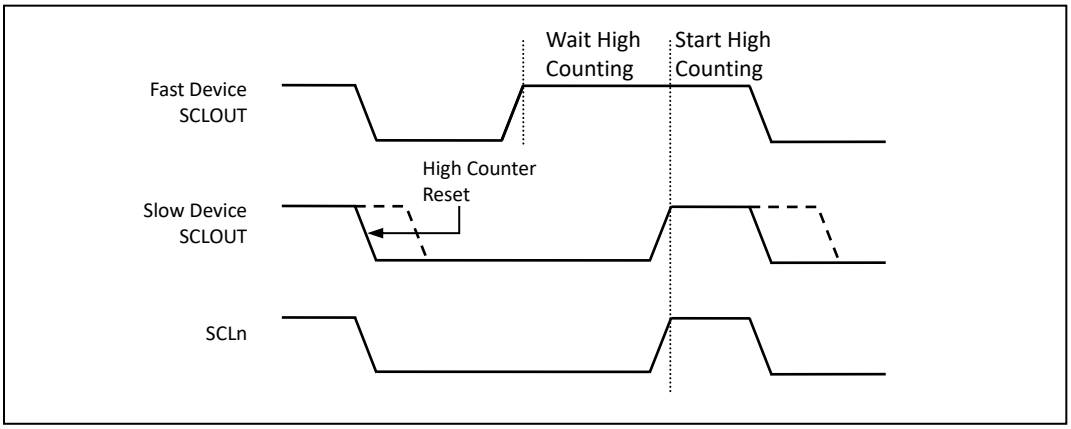


Figure 17.6. Clock synchronization during the arbitration procedure (n = 0, 1 and 2)

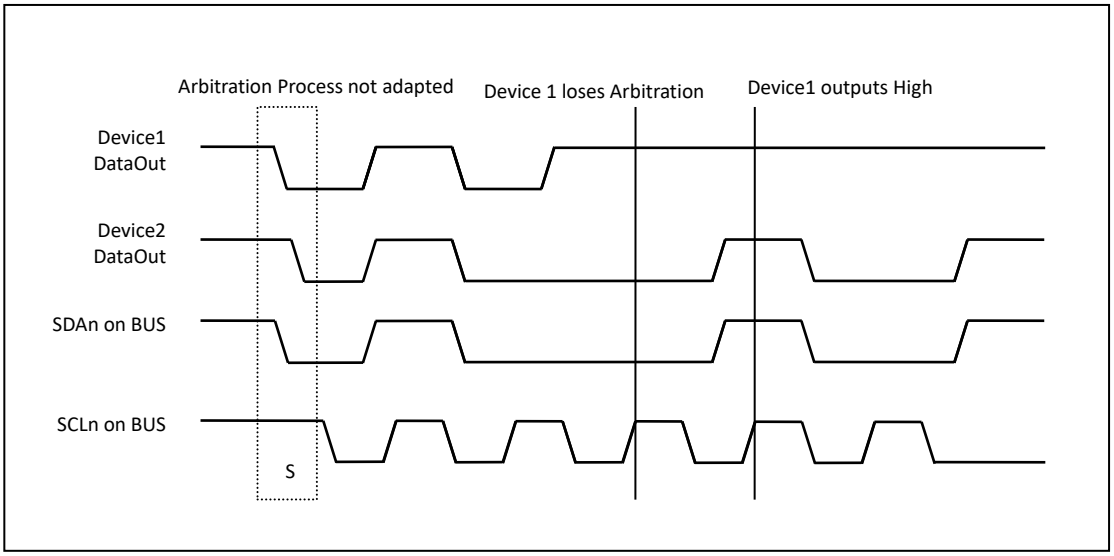


Figure 17.7. Arbitration procedure between two masters (n = 0, 1 and 2)

17.4.6 I2C OPERATION

The I2C is byte-oriented and interrupt based. Interrupts are issued after all bus events except for a transmission of a START condition. Because the I2C is interrupt based, the application software is free to carry on other operations during a I2C byte transfer.

Note that when a I2C interrupt is generated, I2CnIFLAG flag in I2CnIEN register is set, it is cleared when all interrupt source bits in the I2Cn_ST register are cleared to “0b”. When I2C interrupt occurs, the SCLn line is hold LOW until clearing “0b” all interrupt source bits in I2Cn_ST register. When the I2CnIFLAG flag is set, the I2Cn_ST contains a value indicating the current state of the I2C bus. According to the value in I2Cn_ST, software can decide what to do next.

I2C can operate in 4 modes by configuring master/slave, transmitter/receiver. The operating mode is configured by a winning master. A more detailed explanation follows below. (n = 0, 1 and 2)

1.1.1.1 Master Transmitter

To operate I2C in master transmitter, follow the recommended steps below.

1. Enable I2C by setting I2CnEN bit in I2Cn_CR. This provides main clock to the peripheral.
2. Load SLA+W into the I2Cn_DR where SLA is address of slave device and W is transfer direction from the viewpoint of the master. For master transmitter, W is ‘0’. Note that I2CnDR is used for both address and data.
3. Configure baud rate by writing desired value to both I2Cn_SCLR and I2Cn_SCHR for the Low and High period of SCLn line.
4. Configure the I2Cn_SDHR to decide when SDAn changes value from falling edge of SCLn. If SDA should change in the middle of SCLn LOW period, load half the value of I2Cn_SCLR to the I2Cn_SDHR.
5. Set the STARTCn bit in I2Cn_CR. This transmits a START condition. And also configure how to handle interrupt and ACK signal. When the STARTCn bit is set, 8-bit data in I2Cn_DR is transmitted out according to the baud-rate.
6. This is ACK signal processing stage for address packet transmitted by master. When 7-bit address and 1-bit transfer direction is transmitted to target slave device, the master can know whether the slave acknowledged or not in the 9th high period of SCLn. If the master gains bus mastership, I2C generates GCALL interrupt regardless of the reception of ACK from the slave device. When I2C loses bus mastership during arbitration process, the MLOSTn bit in I2Cn_ST is set, and I2C waits in idle state or can be operate as an addressed slave. To operate as a slave when the MLOSTn bit in I2Cn_ST is set, the ACKnEN bit in I2Cn_CR must be set and the received 7-bit address must equal to the SLAn bits in I2Cn_SAR1/2. In this case I2C operates as a slave transmitter or a slave receiver (go to appropriate section). In this stage, I2C holds the SCLn LOW. This is because to decide whether I2C continues serial transfer or stops communication. The following steps continue assuming that I2C does not lose mastership during first data transfer.

   I2C (Master) can choose one of the following cases regardless of the reception of ACK signal from slave.

   1) Master receives ACK signal from slave, so continues data transfer because slave can receive more data from master. In this case, load data to transmit to I2Cn_DR.
   2) Master stops data transfer even if it receives ACK signal from slave. In this case, set the STOPC bit in I2Cn_CR.

   3) Master transmits repeated START condition with not checking ACK signal. In this case, load SLA+R/W into the I2Cn_DR and set STARTCn bit in I2Cn_CR.

   After doing one of the actions above, clear to “0b” all interrupt source bits in I2Cn_ST to release SCLn line. In case of 1), move to step 7. In case of 2), move to step 9 to handle STOP interrupt. In case of 3), move to step 6 after transmitting the data in I2Cn_DR and if transfer direction bit is ‘1’ go to master receiver section.
7. 1-Byte of data is being transmitted. During data transfer, bus arbitration continues.
8. This is ACK signal processing stage for data packet transmitted by master. I2C holds the SCLn LOW. When I2C loses bus mastership while transmitting data arbitrating other masters, the MLOSTn bit in I2Cn_ST is set. If then, I2C waits in idle state. When the data in I2Cn_DR is transmitted completely, I2C generates TENDn interrupt.

I2C can choose one of the following cases regardless of the reception of ACK signal from slave.

1) Master receives ACK signal from slave, so continues data transfer because slave can receive more data from master. In this case, load data to transmit to I2Cn_DR.
2) Master stops data transfer even if it receives ACK signal from slave. In this case, set the STOPCn bit in I2Cn_CR.
3) Master transmits repeated START condition with not checking ACK signal. In this case, load SLA+R/W into the I2Cn_DR and set the STARTCn bit in I2Cn_CR.

After doing one of the actions above, clear to "0b" all interrupt source bits in I2Cn_ST to release SCL line. In case of 1), move to step 7. In case of 2), move to step 9 to handle STOP interrupt. In case of 3), move to step 6 after transmitting the data in I2Cn_DR, and if transfer direction bit is '1' go to master receiver section.

9. This is the final step for master transmitter function of I2C, handling STOP interrupt. The STOP bit indicates that data transfer between master and slave is over. To clear I2Cn_ST, write "0" to I2CnST. After this, I2C enters idle state.

1.1.1.2 Master Receiver

To operate I2C in master receiver, follow the recommended steps below.

1. Enable I2C by setting I2CnEN bit in I2Cn_CR. This provides main clock to the peripheral.
2. Load SLA+R into the I2Cn_DR where SLA is address of slave device and R is transfer direction from the viewpoint of the master. For master receiver, R is '1'. Note that I2Cn_DR is used for both address and data.
3. Configure baud rate by writing desired value to both I2Cn_SCLR and I2Cn_SCHR for the Low and High period of SCLn line.
4. Configure the I2Cn_SDHR to decide when SDAn changes value from falling edge of SCLn. If SDAn should change in the middle of SCLn LOW period, load half the value of I2Cn_SCLR to the I2Cn_SDHR.
5. Set the STARTCn bit in I2Cn_CR. This transmits a START condition. And also configure how to handle interrupt and ACK signal. When the STARTCn bit is set, 8-bit data in I2Cn_DR is transmitted out according to the baud-rate.
6. This is ACK signal processing stage for address packet transmitted by master. When 7-bit address and 1-bit transfer direction is transmitted to target slave device, the master can know whether the slave acknowledged or not in the 9th high period of SCLn. If the master gains bus mastership, I2C generates GCALL interrupt regardless of the reception of ACK from the slave device. When I2C loses bus mastership during arbitration process, the MLOSTn bit in I2Cn_ST is set, and I2C waits in idle state or can be operate as an addressed slave. To operate as a slave when the MLOSTn bit in I2Cn_ST is set, the ACKnEN bit in I2Cn_CR must be set and the received 7-bit address must equal to the SLAn bits in I2Cn_SAR1/2. In this case I2C operates as a slave transmitter or a slave receiver (go to appropriate section). In this stage, I2C holds the SCLn LOW. This is because to decide whether I2C continues serial transfer or stops communication. The following steps continue assuming that I2C does not lose mastership during first data transfer.

   I2C (Master) can choose one of the following cases according to the reception of ACK signal from slave.

   1) Master receives ACK signal from slave, so continues data transfer because slave can prepare and transmit more data to master. Configure ACKnEN bit in I2Cn_CR to decide whether I2C Acknowledges the next data to be received or not.
   2) Master stops data transfer because it receives no ACK signal from slave. In this case, set the STOPCn bit in I2Cn_CR.
   3) Master transmits repeated START condition due to no ACK signal from slave. In this case, load SLA+R/W into the I2Cn_DR and set STARTCn bit in I2Cn_CR.

   After doing one of the actions above, clear to "0b" all interrupt source bits in I2Cn_ST to release SCLn line. In case of 1), move to step 7. In case of 2), move to step 9 to handle STOP interrupt. In case of 3), move to step 6 after transmitting the data in I2Cn_DR and if transfer direction bit is '0' go to master transmitter section.

7. 1-Byte of data is being received.
8. This is ACK signal processing stage for data packet transmitted by slave. I2C holds the SCLn LOW. When 1-Byte of data is received completely, I2C generates TENDn interrupt.
   I2C can choose one of the following cases according to the RXACKn flag in I2Cn_ST.

   1) Master continues receiving data from slave. To do this, set ACKnEN bit in I2CnCR to Acknowledge the next data to be received.
   2) Master wants to terminate data transfer when it receives next data by not generating ACK signal. This can be done by clearing ACKnEN bit in I2Cn_CR.
   3) Because no ACK signal is detected, master terminates data transfer. In this case, set the STOPCn bit in I2Cn_CR.
   4) No ACK signal is detected, and master transmits repeated START condition. In this case, load SLA+R/W into the I2Cn_DR and set the STARTCn bit in I2Cn_CR.

   After doing one of the actions above, clear to “0b” all interrupt source bits in I2Cn_ST to release SCLn line. In case of 1) and 2), move to step 7. In case of 3), move to step 9 to handle STOP interrupt. In case of 4), move to step 6 after transmitting the data in I2Cn_DR, and if transfer direction bit is ‘0’ go to master transmitter section.
9. This is the final step for master receiver function of I2C, handling STOP interrupt. The STOP bit indicates that data transfer between master and slave is over. To clear I2Cn_ST, write “0” value to I2Cn_ST. After this, I2C enters idle state.

1.1.1.3 Slave Transmitter

To operate I2C in slave transmitter, follow the recommended steps below.

1. If the main operating clock (SCLK) of the system is slower than that of SCLn, load value 0x00 into I2Cn_SDHR to make SDAn change within one system clock period from the falling edge of SCLn. Note that the hold time of SDAn is calculated by SDAH x period of SCLK where SDAH is multiple of number of SCLK coming from I2Cn_SDHR. When the hold time of SDAn is longer than the period of SCLK, I2C (slave) cannot transmit serial data properly.
2. Enable I2C by setting I2CnIEN bit and I2CnEN bit in I2Cn_CR. This provides main clock to the peripheral.
3. When a START condition is detected, I2C receives one byte of data and compares it with SLAn bits in I2Cn_SAR1/2. If the GCALLnEN bit in I2Cn_SAR1/2 is enabled, I2C compares the received data with value 0x00, the general call address.
4. If the received address does not equal to SLAn bits in I2Cn_SAR, I2C enters idle state ie, waits for another START condition. Else if the address equals to SLAn bits and the ACKnEN bit is enabled, I2C generates SSELn interrupt and the SCLn line is held LOW. Note that even if the address equals to SLAn bits, when the ACKnEN bit is disabled, I2C enters idle state. When SSELn interrupt occurs, load transmit data to I2Cn_DR and clear to “0b” all interrupt source bits in I2Cn_ST to release SCLn line.
5. 1-Byte of data is being transmitted.
6. In this step, I2C generates TENDn interrupt and holds the SCLn line LOW regardless of the reception of ACK signal from master. Slave can select one of the following cases.

   1) No ACK signal is detected and I2C waits STOP or repeated START condition.
   2) ACK signal from master is detected. Load data to transmit into I2Cn_DR.

   After doing one of the actions above, clear to “0b” all interrupt source bits in I2Cn_ST to release SCLn line. In case of 1) move to step 7 to terminate communication. In case of 2) move to step 5. In either case, a repeated START condition can be detected. For that case, move step 4.
7. This is the final step for slave transmitter function of I2C, handling STOP interrupt. The STOPCn bit indicates that data transfer between master and slave is over. To clear I2Cn_ST, write “0” to I2Cn_ST. After this, I2C enters idle state.

1.1.1.4 Slave Receiver

To operate I2C in slave receiver, follow the recommended steps below.

1. If the main operating clock (SCLK) of the system is slower than that of SCLn, load value 0x00 into I2Cn_SDHR to make SDAn change within one system clock period from the falling edge of SCLn. Note that the hold time of SDAn is calculated by SDAH x period of SCLK where SDAH is multiple of number of SCLK coming from I2Cn_SDHR. When the hold time of SDAn is longer than the period of SCLK, I2C (slave) cannot transmit serial data properly.
2. Enable I2C by setting I2CnIEN bit in I2Cn_CR. This provides main clock to the peripheral.
3. When a START condition is detected, I2C receives one byte of data and compares it with SLA bits in I2C_SAR. If the GCALLnEN bit in I2Cn_SAR1/2 is enabled, I2C compares the received data with value 0x00, the general call address.
4. If the received address does not equal to SLAn bits in I2Cn_SAR1/2, I2C enters idle state ie, waits for another START condition. Else if the address equals to SLAn bits and the ACKnEN bit is enabled, I2C generates SSELn interrupt and the SCLn line is held LOW. Note that even if the address equals to SLA bits, when the ACKnEN bit is disabled, I2C enters idle state. When SSELn interrupt occurs and I2C is ready to receive data, clear to “0b” all interrupt source bits in I2Cn_ST to release SCLn line.
5. 1-Byte of data is being received.
6. In this step, I2C generates TENDn interrupt and holds the SCLn line LOW regardless of the reception of ACK signal from master. Slave can select one of the following cases.

   1) No ACK signal is detected (ACKnEN=0) and I2C waits STOP or repeated START condition.
   2) ACK signal is detected (ACKnEN=1) and I2C can continue to receive data from master.

   After doing one of the actions above, clear to “0b” all interrupt source bits in I2Cn_ST to release SCLn line. In case of 1) move to step 7 to terminate communication. In case of 2) move to step 5. In either case, a repeated START condition can be detected. For that case, move step 4.
7. This is the final step for slave receiver function of I2C, handling STOP interrupt. The STOPCn bit indicates that data transfer between master and slave is over. To clear I2Cn_ST, write “0” to I2Cn_ST. After this, I2C enters idle state.

CHAPTER 18. 12-BIT A/D CONVERTER

18.1 OVERVIEW

The analog-to-digital converter (A/D) allows conversion of an analog input signal to corresponding 12-bit digital value. The A/D module has eleven analog inputs.The output of the multiplexer is the input into the converter which generates the result through successive approximation. The A/D module has three registers which are the A/D converter control register (ADC_CR), A/D converter data register (ADC_DR), and A/D converter prescaler data register (ADC_PREDR). The channels to be converted are selected by setting ADSEL[3:0]. The register ADC_DR contains the results of the A/D conversion. When the conversion is completed, the result is loaded into the ADC_DR, the A/D conversion status bit AFLAG is set to '1', and the A/D interrupt is set. During A/D conversion, AFLAG bit is read as '0'.

- 14 channels of analog inputs
- S/W (ADST) and Timer trigger (TIMER10/TIMER11/TIMER12 A match, ADC trigger signal from TIMER30) support
- Conversion time : 34 clock
- 6-bit Prescaler

Figure shows the block diagram of a A/D converter block.

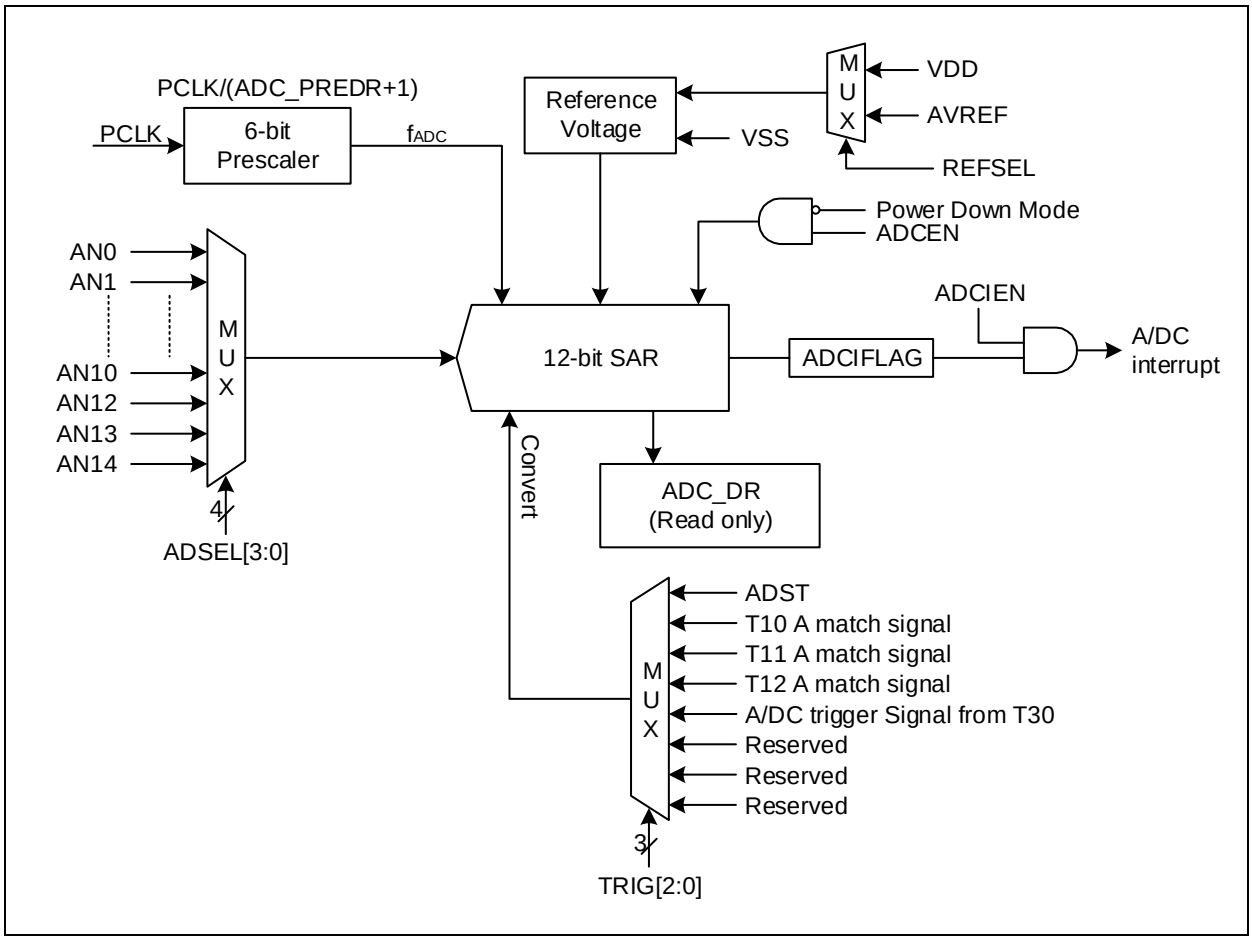


Figure 18.1. Block Diagram

18.2 Pin Description

Table 18.1 External pin

PIN NAME	TYPE	DESCRIPTION
VDD	P	Digital Power
VSS	P	Digital GND
AVREF	P	Analog Reference Voltage
AN0	A	ADC Input 0
AN1	A	ADC Input 1
AN2	A	ADC Input 2
AN3	A	ADC Input 3
AN4	A	ADC Input 4
AN5	A	ADC Input 5
AN6	A	ADC Input 6
AN7	A	ADC Input 7
AN8	A	ADC Input 8
AN9	A	ADC Input 9
AN10	A	ADC Input 10
AN12	A	ADC Input 12
AN13	A	ADC Input 13
AN14	A	ADC Input 14

18.3 REGISTERS

Base addresses of ADC units are as below.

Table 18.1 ADC base address

NAME	BASE ADDRESS
ADC	0x4000_3000

Table 18.2 ADC Register map

Register Name	Offset	Access Type	Description	Initial Value	Ref
ADC_CR	0x00	RW	A/D Converter Control Register	0x0000_0000	18.3.1
ADC_DR	0x04	RO	A/D Converter Data Register	Unknown	18.3.2
ADC_PREDR	0x08	RW	A/D Converter Prescaler Data Register	0x0000_000F	18.3.3

18.3.1 ADC_CR A/D Converter Control Register

A/D Converter module should be configured properly before running. A/D Converter Control Register is 32-bit register. This Register is able to 32/16/8-bit access.

ADC_CR=0x4000_3000

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15	14	13 12 11	10	9	8	7 6	5	4	3 2 1 0
Reserved		ADCEN	Reserved	TRIG	REFSEL	Reserved	ADST	Reserved	ADCIEN	ADCIFLAG	ADSEL
-		0	-	000	0	-	0	-	0	0	0000
-		RW	-	RW	RW	-	RW	-	RW	RW	RW

15	ADCEN	A/DC Module Enable bit. (The A/DC is automatically disabled at power down mode)
	0	Disable A/DC module operation.
	1	Enable A/DC module operation.
13 11	TRIG	A/DC Trigger Signal Selection bits.
	000	ADST.
	001	Timer 10 A-match signal.
	010	Timer 11 A-match signal.
	011	Timer 12 A-match signal.
	100	A/DC trigger signal from timer 30
	Others	Reserved
10	REFSEL	A/DC Reference Selection bit.
	0	Select analog power. (VDD)
	1	Select external reference. (AVREF)
8	ADST	A/DC Conversion Start bit. This bit is automatically cleared to “0b” after operation.
	0	No effect.
	1	Trigger signal generation for conversion start.
	Note) Before ADST is set, ADCEN must be set.	
5	ADCIEN	A/DC Interrupt Flag bit.
	0	Disable A/DC interrupt.
	1	Enable A/DC interrupt.
4	ADCIFLAG	A/DC Interrupt Flag bit.
	0	No request occurred.
	1	Request occurred, This bit is cleared to ‘0’ when write ‘1’.
3 0	ADSEL	A/D Converter Channel Selection bits.
	0000	AN0
	0001	AN1
	0010	AN2
	0011	AN3
	0100	AN4
	0101	AN5
	0110	AN6
	0111	AN7
	1000	AN8
	1001	AN9
	1010	AN10
	1011	Reserved
	1100	AN12
	1101	AN13
	1110	AN14
	Others	Reserved

18.3.2 ADC_DR A/D Converter Data Register

A/D Converter Data Register is 32-bit register. This Register is able to 32/16/8-bit access.

ADC_DR=0x4000_3004

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																				ADDATA											
-																				Unknown											
-																				RO											

11 0	ADDATA	A/D Converter Result Data bits.

18.3.3 ADC_PREDR A/D Converter Prescaler Data Register

A/D Converter Prescaler Data Register is 32-bit register. This Register is able to 32/16/8-bit access.

ADC_PREDR=0x4000_3008

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																										PRED					
-																										00_0000					
-																										RW					

5 0	PRED	A/D Converter Prescaler Data bits.

18.4 Functional Description

18.4.1 Conversion Timing

The A/D conversion process requires 2 steps to convert each bit and 30 clocks
the conversion rate is calculated as follows:
4 Clocks sample time + 26 Clocks Conversion Time = 30 clock
Conversion Time : MCLK * 30 clock = 4.5MHz*30=6.67us
(Maximum 4.5MHz conversion rate)

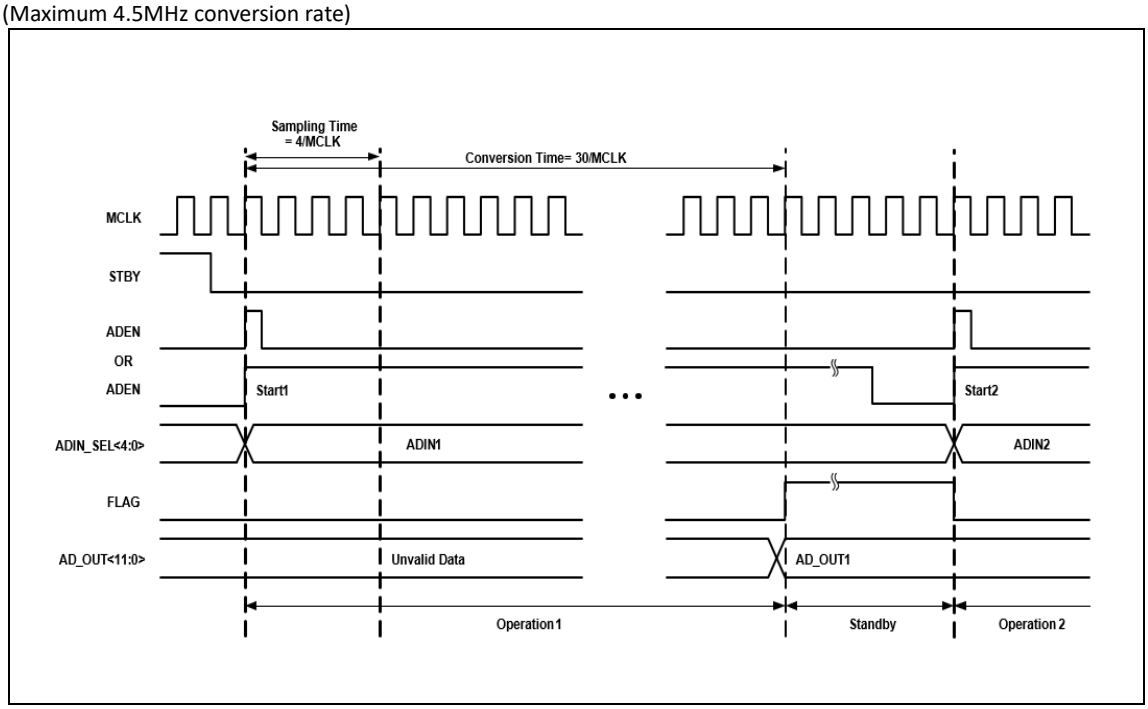
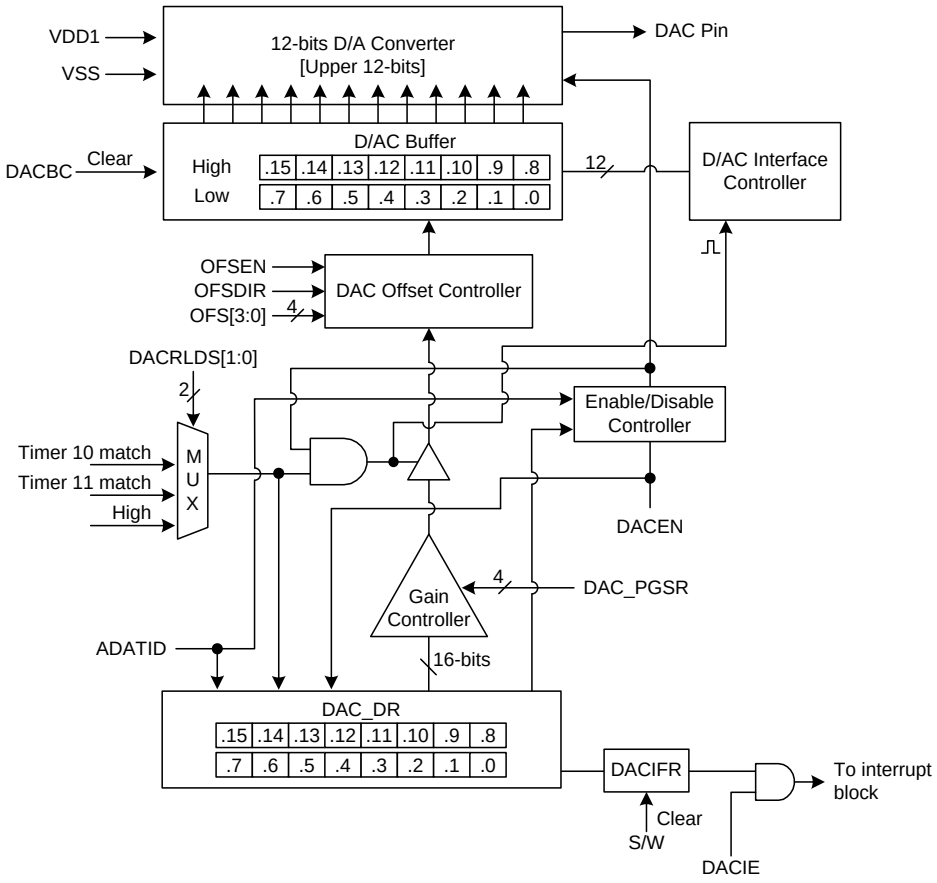


Figure 18.2. 12-bit ADC Converter Timing Chart

CHAPTER 19. 12-BIT D/A CONVERTER

19.1 OVERVIEW

The digital-to-analog converter (D/A) uses successive approximation logic to convert 12-bit digital value to an analog output level. The D/A module has six registers which are the D/A converter control register (DAC_CR), D/A converter data register (DAC_DR), D/A converter buffer register (DAC_BR), and programmable gain selection register (DAC_PGSR).



NOTE)

1. The DODRH/L register is a binary format with 16-bits length.
2. The gain controller converts data like the below order.
   - Get the DAC_DR[15:0] value
   - Adjust the data by selection gain
   - Write the data to the D/AC buffer
3. The D/AC interface block doesn't work when DACRLDS bits of the DAC_CR register are set to "00b"

Figure 19.1 Block Diagram

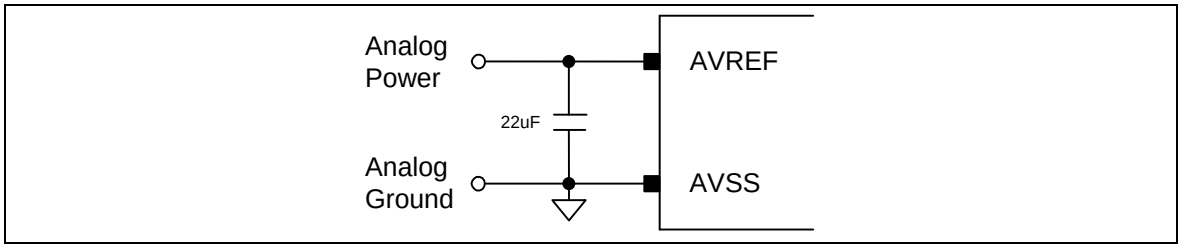


Figure 19.2 Analog Power (AVREF) Pin with Capacitor

19.2 Pin Description

Table 19.1 External pin

PIN NAME	TYPE	DESCRIPTION
DAO	A	D/A converter Output
DAVREF	P	D/A converter reference input

19.3 REGISTERS

Base addresse of D/A Converter is as below

Table 19.1 DAC base address

NAME	BASE ADDRESS
DAC	0x4000_3450

Table 19.2 DAC Register map

Register Name	Offset	Access Type	Description	Initial Value	Ref
DAC_DR	0x00	RW	D/A Converter Data Register	0x0000_0000	19.3.1
DAC_BR	0x04	RO	D/A Converter Buffer Register	0x0000_0000	19.3.2
DAC_CR	0x08	RW	D/A Converter Control Register	0x0000_0000	19.3.3
DAC_PGSR	0x0C	RW	Programmable Gain Selection Register	0x0000_0005	19.3.4
DAC_OFSCR	0x10	RW	D/A Converter Offset Control Register	0x0000_0000	19.3.5

19.3.1 DAC_DR D/A Converter Data Register

DAC_DR=0x4000_3150

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																DACDR															
-																0x0000															
-																RW															

15	DACDR	D/A Converter Data (16-bit)
0		The DACDR[15:0] is a binary format.

19.3.2 DAC_BR D/A Converter Buffer Register

DAC_BR=0x4000_3154

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																DACBR															
-																0x0000															
-																RO															

15	DACBR	D/A Converter Buffer Data (16-bit)
0		The DACBR[15:0] is a binary format.

19.3.3 DAC_CR D/A Converter Control Register

DAC_CR=0x4000_3158

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10	9	8	7	6	5	4	3	2 1	0
Reserved			AMPBYPASS	REFSEL	DACIE	DACIFR	ADATID	DACBC	Reserved	DACRLDS	DACEN
-			0	0	0	0	0	-	0	0	0
-			RW	RW	RW	RW	RW	-	RW	RW	RW

9	AMPBYPASS	DAC Internal AMP Bypass enable
	0	AMP Path active
	1	AMP Bypass
		NOTE) DAC characteristic is better to bypass the AMP than the AMP Path is active. So, it always recommend this bit is '1'.
8	REFSEL	DAC Reference Selection
	0	AVDD (Internal)
	1	DAVREF Pin (External)
7	DACIE	Enable or Disable D/AC Interrupt
	0	Disable
	1	Enable
6	DACIFR	When D/AC Interrupt occurs, this bit becomes '1'. The flag is cleared only by writing a '0' to the bit. So, the flag should be cleared by software. This interrupt is for a result that the DAC_DR register automatically increments to "0x800" or decrements to "0x000". Write '1' has no effect.
	0	D/AC interrupt no generation
	1	D/AC interrupt generation
5	ADATID	Automatically D/A Converter Data Increment/Decrement
	0	Disable automatically D/AC data increment/decrement
	1	Automatically D/AC data increment from DAC_DR value to "0x800" when DACEN bit is changed to "1". Automatically D/AC data decrement from DAC_DR value to "0x000" when DACEN bit is changed to "0".
4	DACBC	D/A Converter Buffer Clear
	0	No effect.
	1	Clear the D/AC buffer (When write, automatically cleared to '0' after being cleared)
2 1	DACRLDS	D/A Converter Reload Selection. These bits select a reload signal to load data from D/AC data register to buffer.
	00	Always
	10	Rising edge of Timer 10 out signal
	11	Rising edge of Timer 11 out signal
0	DACEN	D/A Converter Enable Bit
	0	Stop D/AC operation (Low level output)
	1	Start D/AC operation

19.3.4 DAC_PGSR D/A Converter Programmable Gain Control Register

DAC_PGSR=0x4000_315C

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																												PGS3	PGS2	PGS1	PGS0
-																												0	1	0	1
-																												RW	RW	RW	RW

3	PGS	Programmable Gain Selection	
0		0000	-30dB
		0001	-24dB
		0010	-18dB
		0011	-12dB
		0100	-6dB
		0101	0dB
		0110	+6dB
		0111	+12dB
		1000	+18dB
		1001	+24dB
		1010	+30dB
		Others	Reserved

19.3.5 DAC_OFSCR D/A Converter Offset Control Register

DAC_OFSCR=0x4000_3160

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																								OFSEN	OFSDIR	Reserved		OFS			
-																								0	0	-		0			
-																								RW	RW	-		RW			

7	OFSEN	D/AC Offset Control Enable Bit
		0 Disable
		1 Enable
6	OFSDIR	D/AC Offset Direction Selection Bit
		0 D/AC buffer data are subtracted by (n + 1)
		1 D/AC buffer data are added by (n + 1)
		NOTE) Where n is the OFS value and n=0,1,2,,,,, 15.
3 0	OFS	D/AC Offset Value

19.4 Functional Description

The D/A converter has R-2R structure and the data regiser is a binary format.

The 16-bit digital value of the D/AC data register goes into D/AC buffer register through the programmable gain controller every a reload signal. The reload signal is one of the “Always”, “Timer 0 match signal” and “Timer 1 match signal”. The signal is selected by the DACRLDS[1:0] bits. The programmable gain controller has eleven step (-30dB, -24dB, -18dB, -12dB, -6dB, 0dB, +6dB, +12dB, +18dB, +24dB and +30dB) and the gain is selected by the programmable gain register (DAC_PGSR). The value of the D/A converter data register can be automatically incremented from the current data value to “0x800” when the D/A converter is enabled by DACEN bit set to “1” and vice vesa. At that time, the D/A converter interrupt flag bit (DACIFR) is set to “1”. The auto-increment/decrement structure for D/A converter data is useful to remove a pop noise when a speaker is turn on/off. Two kinds External D/AC Converter is be accessed

19.4.1 D/A Converter Data and Buffer Registers

The D/A converter data and buffer registers are 16-bits, repectively. But only the upper 12-bits of the D/A converter buffer register specifies to generate DAC output signal. The reset value of the data and buffer is “0x0000”. The D/A converter output value, VDAC, is calculated by the following formula.

VDAC = VDD X (n ÷ 4096), (n = 0, 1, 2,,,,, 4095. That is DAC_BR[15:4] value)

19.4.2 Automatically D/AC Data Increment/Decrement

The “automatically D/AC data increment/decrement” function is important to remove a pop noise when voice prompt play. If this function is not embedded, a programmer have to code to reduce a pop noise on speaker. The DAC_DR[15:4] value increases a curret D/AC data value to 0x800 with “automatically D/AC data increment” when the ADATID bit is set to “1” and the DACEN bit is changed to “1” from “0”. The DAC_DR[15:4] value decreases a curret D/AC data value to 0x000 with “automatically D/AC data decrement” when the ADATID bit is set to “1” and the DACEN bit is changed to “0” from “1”.

How to remove a pop noise when a speaker is turn on:
- Write “0x05” for 0dB to DAC_PGSR register
- Write “0x0000” to D/A converter data register
- Clear D/A converter buffer register by DACBC bit set to “1”
- Start D/AC operation by DACEN bit set to “1”

How to remove a pop noise when a speaker is turn off:
- Write “0x05” for 0dB to DAC_PGSR register
- Keep the value of DACRLDS[1:0] bits set when speaker is turn on
- Stop D/AC operation by DACEN bit set to “0”

19.4.3 Programmable Gain Controller

There are 11 selectable step in the programmable gain controller. The steps are -30dB, -24dB, -18dB, -12dB, -6dB, 0dB, +6dB, +12dB, +18dB, +24dB and +30dB. The gain is selected by the programmable gain register (DAC_PGSR).

The gain controller converts the value of the DAC_DR[15:0] by the following procedure.
- Get the value of the D/A converter data register (DAC_DR[15:0])
- Change the data into a 16-bit signed format
- Adjust the data by a selected gain
- Modify the data into a 16-bit binary format
- Write the data to the D/A converter buffer register (DAC_BR[15:0])

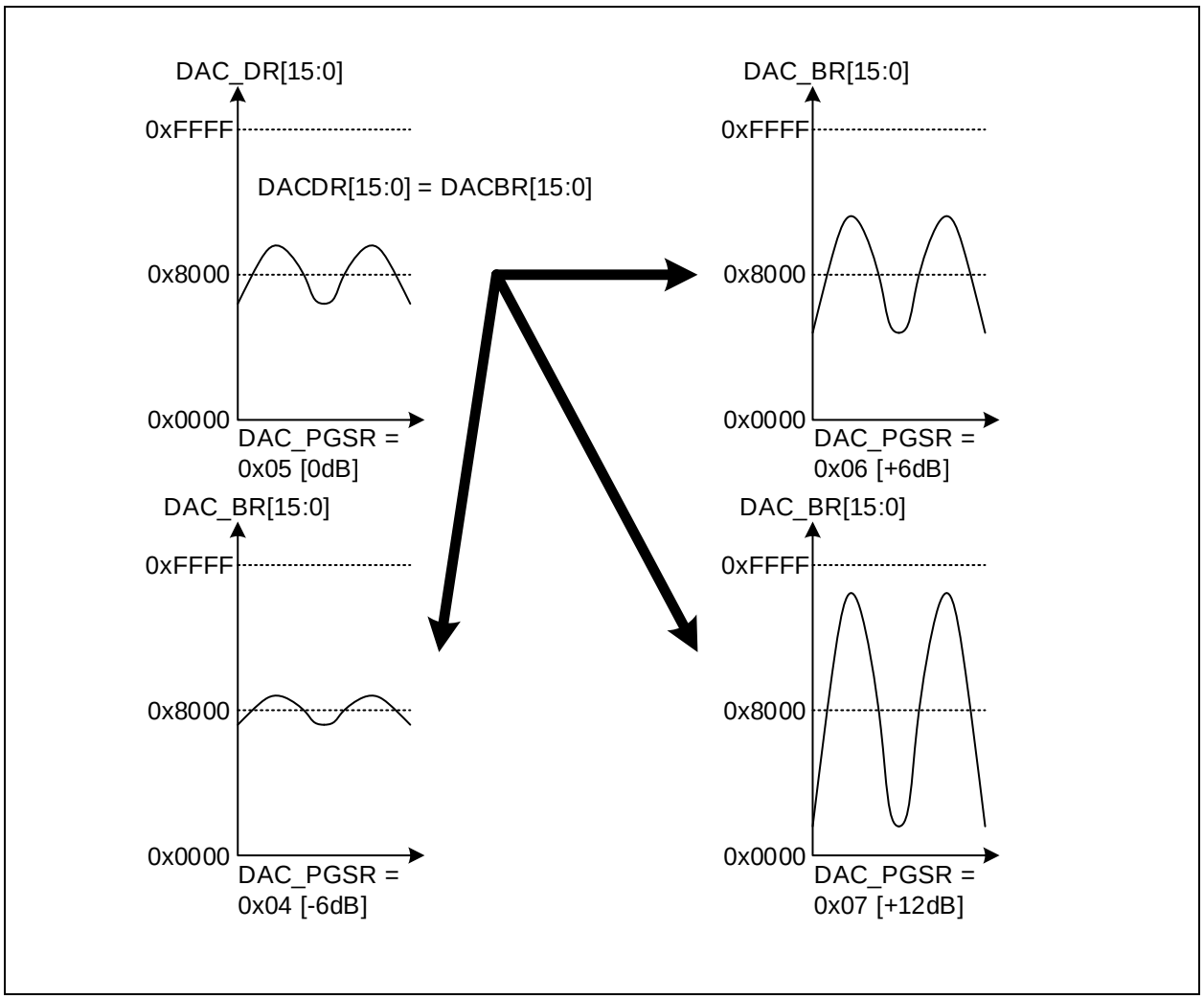


Figure 19.3. The DAC_BR[15:0] Value by a Selected Gain

CHAPTER 20. COMPARATOR

20.1 OVERVIEW

The Comparator compares one analogue voltage level with External reference voltage, or internal reference voltage, or DAC output voltage.

The Comparator has following features:

- 2 Comparators
- Internal BGR reference for comparator
- Comparator output de-bounce function
- Level and edge interrupt mode support for comparator

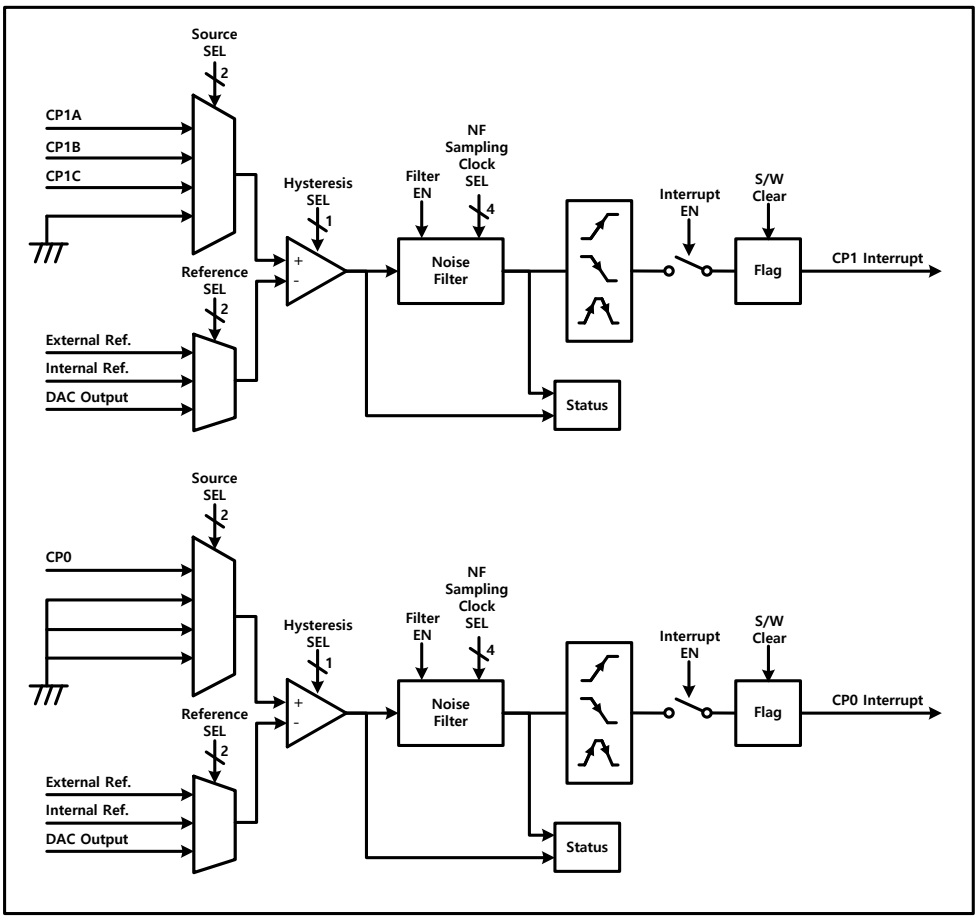


Figure 20.1. Block Diagram

20.2 Pin Description

Table 20.1 External pin

PIN NAME	TYPE	DESCRIPTION
CP0	A	Comparator input 0
CREF0	A	Comparator 0 Reference
CP1A	A	Comparator input 1A
CP1B	A	Comparator input 1B
CP1C	A	Comparator input 1C
CREF1	A	Comparator 1 Reference

20.3 REGISTERS

Base addresses of Comparator units are as below.

Table 20.1 Comparator base address

NAME	BASE ADDRESS
CMP	0x4000_3420

Table 20.2 Comparator Register map

Register Name	Offset	Access Type	Description	Initial Value	Ref
CMP_CMP0CR	0x00	RW	Comparator 0 Control Register	0x0000_0000	21.3.1
CMP_CMP1CR	0x04	RW	Comparator 1 Control Register	0x0000_0000	21.3.2
CMP_DBNC	0x10	RW	Comparator Debounce Register	0x0000_0000	21.3.3
CMP_ICON	0x14	RW	Comparator Interrupt Control Register	0x0000_0000	21.3.4
CMP_IEN	0x18	RW	Comparator Interrupt Enable Register	0x0000_0000	21.3.5
CMP_IST	0x1C	RO	Comparator Interrupt Status Register	0x0000_0000	21.3.6
CMP_ICLR	0x20	RW	Comparator Interrupt Clear Register	0x0000_0000	21.3.7

20.3.1 CMP_CMP0CR Comparator 0 Control Register

CMP0_CR=0x4000_3420

31 30 29 28 27 26 25 24	23 22 21	20	19 18 17	16	15 14 13	12	11 10 9 8	7 6	5 4	3 2	1 0
Reserved		HYSEN0	Reserved	HYSSEL0	Reserved	COMP0EN	Reserved		C0INNSEL	Reserved	C0INPSEL
-		0	-	0	-	0	-		0	-	0
-		RW	-	RW	-	RW	-		RW	-	RW

20	HYSEN0	Comparator Hysteresis Enable	
		0	Disable Hysteresis
		1	Enable Hysteresis
16	HYSSEL0	Comparator Hysteresis Select	
		0	5mV Hysteresis
		1	20mV Hysteresis
12	COMP0EN	Comparator Enable bits	
		0	Disable Comparator
		1	Enable Comparator
5	C0INNSEL	Comparator Reference(input -) Selection bit	
4		00	CREF0
		01	BGR 1V
		10	DAC OUT
		11	Reserved
1	C0INPSEL	Comparator Input(input +) Selection bit	
0		00	CP0 (PA2)
		01	CP1B (PA4)
		10	CP1C (PA3)
		11	Reserved

20.3.2 CMP_CMP1CR Comparator 1 Control Register

CMP1_CR=0x4000_3424

31 30 29 28 27 26 25 24	23 22 21	20	19 18 17	16	15 14 13	12	11 10 9 8	7 6	5 4	3 2	1 0
Reserved		HYSEN1	Reserved	HYSSEL1	Reserved	COMP1EN	Reserved		C1INNSEL	Reserved	C1INPSEL
-		0	-	0	-	0	-		0	-	0
-		RW	-	RW	-	RW	-		RW	-	RW

20	HYSEN1	Comparator Hysteresis Enable
		0 Disable Hysteresis
		1 Enable Hysteresis
16	HYSSEL1	Comparator Hysteresis Select
		0 5mV Hysteresis
		1 20mV Hysteresis
12	COMP1EN	Comparator Enable bits
		0 Disable Comparator
		1 Enable Comparator
5	C1INNSEL	Comparator Reference(input -) Selection bit
4		00 CREF1
		01 BGR 1V
		10 DACOUT
		11 Reserved
1	C1INPSEL	Comparator Input(input +) Selection bit
0		00 CP1A (PA5)
		01 CP1B (PA4)
		10 CP1C (PA3)
		11 Reserved

20.3.3 CMP_DBNC Comparator Debounce Register

CMP_DBNC=0x4000_3430

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DBNCTB																Reserved								C1DBNC				C0DBNC			
0																-								0000				0000			
RW																-								RW				RW			

31 16	DBNCTB	Debounce time base counter System clock/(DBNCTB *2) becomes shift clock of debounce logic When DBNCTB is 0, system clock would be debounce clock.
7 4	C1DBNC	Debounce shift Selection When it is 0x0, debounce function is disable Shift number of debounce logic is (C1DBNC + 1) when C1DBNC is more than 1
3 0	C0DBNC	Debounce shift Selection When it is 0x0, debounce function is disable Shift number of debounce logic is (C0DBNC + 1) when C0DBNC is more than 1

20.3.4 CMP_ICON Comparator Interrupt Control Register

CMP_ICON=0x4000_3434

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14	13	12	11 10	9	8	7 6 5 4	3 2	1 0
Reserved			TPOL1	TPOL0	Reserved	IPOL1	IPOL0	Reserved	C1IMODE	C0IMODE
-			0	0	-	0	0	-	0	0
-			RW	RW	-	RW	RW	-	RW	RW

13	TPOL1	Comparator Trigger output polarity(to trigger other IP)	
		0	output normal (comparator out high activates trigger)
		1	output inverted (XOR)
12	TPOL0	Comparator Trigger output polarity(to trigger other IP)	
		0	output normal (comparator out high activates trigger)
		1	output inverted (XOR)
9	IPOL1	Comparator 1 interrupt polarity(level mode)	
		0	interrupt at comparator out high
		1	interrupt at comparator out low
8	IPOL0	Comparator 0 interrupt polarity(level mode)	
		0	interrupt at comparator out high
		1	interrupt at comparator out low
3	C1IMODE	Comparator 1 Interrupt Flag bit.	
2		00	level interrupt (by IPOL1)
		01	rising edge interrupt
		10	falling edge interrupt
		11	both edge interrupt A/D Converter Prescaler Data bits.
1	C0IMODE	Comparator 0 Interrupt Flag bit.	
0		00	level interrupt (by IPOL0)
		01	rising edge interrupt
		10	falling edge interrupt
		11	both edge interrupt A/D Converter Prescaler Data bits.

20.3.5 CMP_IEN Comparator Interrupt Enable Register

CMP_IEN=0x4000_3438

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																														C1IEN	C0IEN
-																														0	0
-																														RW	RW

Bits	Name	Function	
1	C1IEN	Comparator 1 Enable	
		0	Disable
		1	Enable
0	C0IEN	Comparator 0 Enable	
		0	Disable
		1	Enable

20.3.6 CMP_IST Comparator Interrupt Status Register

CMP_IST=0x4000_343C

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																														C1IRQ	C0IRQ
-																														0	0
-																														RO	RO

Bits	Name	Function	
1	C1IRQ	Comparator 1 interrupt Status	
		0	No Comparator Interrupt
		1	Comparator Interrupt asserted
0	C0IRQ	Comparator 0 interrupt Status	
		0	No Comparator Interrupt
		1	Comparator Interrupt asserted

20.3.7 CMP_ICLR Comparator Interrupt Clear Register

CMP_ICLR=0x4000_3440

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																														C1CLR	C0CLR
-																														0	0
-																														RW	RW

Bits	Name	Function
13	C1ICLR	Comparator 1 Interrupt Clear (write “1” to clear C1IRQ)
12	C0ICLR	Comparator 0 Interrupt Clear (write “1” to clear C0IRQ)

CHAPTER 21. TOUCH

21.1 OVERVIEW

Capacitive touch sensor systems are typical human machine interfaces (HMI) which operate by detecting changes in electrostatic capacitance produced by the touch of a finger or other conductor.

The use of capacitive touch technology can easily improve reliability in product design, and enhance the end-user experience. It also enables manufacturing costs to be lowered in a wide range of fields such as household appliances (white goods), healthcare devices, and other electric and electronic equipment.

- . Self-Capacitive Touch Key Sensor.
- . Total 24-channel Touch Key Support.
- . 16-bits Sensing Resolutions.
- . Fast Initial Self Calibration.
- . Key Detection Mode : Single/Multi-Mode.
- . The Improvement of the SNR by Bias-Calibration in Analog Sensing Block

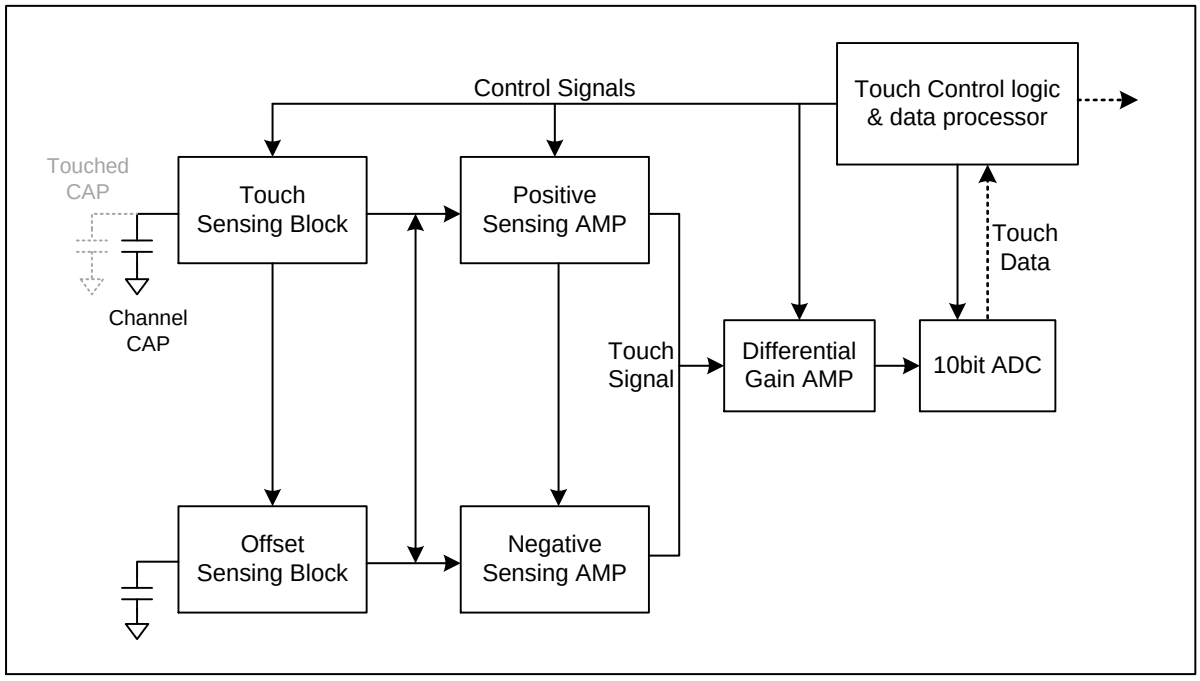


Figure 21.1 Block Diagram

21.2 Pin Description

Table 21.1 External pin

PIN NAME	TYPE	DESCRIPTION
CS0 ~ CS23	IA	Capacitive Touch switch input

21.3 REGISTERS

Base addresses of TOUCH unit are as below.

Table 21-1 TOUCH base address

NAME	BASE ADDRESS
TS	0x4000_3600

Table 21-2 TOUCH Register map

Register Name	Offset	Access Type	Description	Initial Value	Ref
TS_SUM_CHn	0x000 -0x05C	RO	Touch Sensor Channel n(0~23) Sum Register	0x0000_0000	22.3.1
TS_SCOn	0x060 -0x0BC	RW	Touch Sensor Offset Capacitor Selection Register for Channel n(0~23)	0x0000_0000	22.3.2
TS_CON	0x100	RW	Touch Sensor Control Register	0x0000_0000	22.3.3
TS_MODE	0x104	RW	Touch Sensor Mode Register	0x0000_0010	22.3.4
TS_SUM_CNT	0x108	RW	Touch Sensor Sum Repeat Count Register	0x0000_0001	22.3.5
TS_CH_SEL	0x10C	RW	Touch Sensor Channel Selection Register	0x0000_0000	22.3.6
TS_SLP_CR	0x114	RW	Touch Sensor Low Pass Filter Control Register	0x0000_0001	22.3.7
TS_ADC_CH_SEL	0x118	RW	ADC Channel Selection Register	0x0000_0000	22.3.8
TS_INTEG_CNT	0x11C	RW	Touch Sensor Sensing Integration Count Register	0x0000_0032	22.3.9
TS_FREQ_NUM	0x120	RW	Touch Sensor Frequency Number Register	0x0000_00FF	22.3.10
TS_FREQ_DEL	0x124	RW	Touch Sensor Frequency Delta Register	0x0000_0000	22.3.11
TS_CLK_CFG	0x128	RW	Touch Sensor Clock Configuration Register	0x0000_0030	22.3.12
TS_TRIM_OSC	0x12C	RW	Touch Sensor RING Oscillator Trimming Selection Register	0x0000_00B8	22.3.13
TS_TRIM_A_OSC	0x130	RW	Touch Sensor RING Oscillator Trimming for ADC Register	0x0000_00FF	22.3.14
TS_SCI	0x134	RW	Touch Sensor Input Capacitor Selection Register	0x0000_0034	22.3.15
TS_SCC	0x138	RW	Touch Sensor Conversion Capacitor Selection Register	0x0000_0004	22.3.16
TS_SVREF	0x13C	RW	Touch Sensor VREF Resistor Selection Register	0x0000_0004	22.3.17
TS_TAR	0x140	RW	Touch Sensor Integration AMP Reset Register	0x0000_0020	22.3.18
TS_TRST	0x144	RW	Touch Sensor Reset time of Sensing Register	0x0000_0003	22.3.19
TS_TDRV	0x148	RW	Touch Sensor Sample time of Sensing Register	0x0000_0003	22.3.20
TS_TINT	0x14C	RW	Touch Sensor Integration time of Sensing Register	0x0000_0014	22.3.21
TS_TD	0x150	RW	Touch Sensor Differential AMP Sampling Register	0x0000_0020	22.3.22
TS_TWR	0x154	RW	Touch Sensor Wait time Register	0x0000_0010	22.3.23
TS_TLED	0x158	RW	LED stable time Register	0x0000_0300	22.3.24

21.3.1 TS_SUM_CHn Touch Sensor Channel n Sum Register

Touch Sensor Channel n Sum or ADC Register

TS_SUM_CH00=0x4000_3600, TS_SUM_CH01=0x4000_3604, TS_SUM_CH02=0x4000_3608, TS_SUM_CH03=0x4000_360C
TS_SUM_CH04=0x4000_3610, TS_SUM_CH05=0x4000_3614, TS_SUM_CH06=0x4000_3618, TS_SUM_CH07=0x4000_361C
TS_SUM_CH08=0x4000_3620, TS_SUM_CH09=0x4000_3624, TS_SUM_CH10=0x4000_3628, TS_SUM_CH11=0x4000_362C
TS_SUM_CH12=0x4000_3630, TS_SUM_CH13=0x4000_3634, TS_SUM_CH14=0x4000_3638, TS_SUM_CH15=0x4000_363C
TS_SUM_CH16=0x4000_3640, TS_SUM_CH17=0x4000_3644, TS_SUM_CH18=0x4000_3648, TS_SUM_CH19=0x4000_364C
TS_SUM_CH20=0x4000_3650, TS_SUM_CH21=0x4000_3654, TS_SUM_CH22=0x4000_3658, TS_SUM_CH23=0x4000_365C

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
Reserved		SUM_CH_DATA	
-		0x0000	
-		RO	

15 0	SUM_CH_DATA	Touch Sensor Channel n Sum or ADC Data

21.3.2 TS_SCOn Touch Sensor Offset Capacitor Selection Register for CHn

Touch Sensor Offset Capacitor Selection Register for CHn

TS_SCO00=0x4000_3660, TS_SCO01=0x4000_3664, TS_SCO02=0x4000_3668, TS_SCO03=0x4000_366C
TS_SCO04=0x4000_3670, TS_SCO05=0x4000_3674, TS_SCO06=0x4000_3678, TS_SCO07=0x4000_367C
TS_SCO08=0x4000_3680, TS_SCO09=0x4000_3684, TS_SCO10=0x4000_3688, TS_SCO11=0x4000_368C
TS_SCO12=0x4000_3690, TS_SCO13=0x4000_3694, TS_SCO14=0x4000_3698, TS_SCO15=0x4000_369C
TS_SCO16=0x4000_36A0, TS_SCO17=0x4000_36A4, TS_SCO18=0x4000_36A8, TS_SCO19=0x4000_36AC
TS_SCO20=0x4000_36B0, TS_SCO21=0x4000_36B4, TS_SCO22=0x4000_36B8, TS_SCO23=0x4000_36BC

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
Reserved			SCO
-			0000_0000
-			RW

8 0	SCO	Touch Sensor Offset Capacitor Selection	
		0_0000_0000b	0pF
		0_0000_0001b	0.1pF
		0_0000_0010b	0.2pF
		0_0000_0100b	0.4pF
		0_0000_1000b	0.8pF
		0_0001_0000b	1.6pF
		0_0010_0000b	3.2pF
		0_0100_0000b	6.4pF
		0_1000_0000b	12.8pF
		1_0000_0000b	25.6pF
		-	-
		1_1111_1111b	51.1pF

21.3.3 TS_CON Touch Sensor Control Register

Touch Sensor Control Register.

This register is 8-bit register.

TS_CON=0x4000_3700

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																											OSC_EN	BGR_EN	TS_IF	Reserved	TS_RUN
-																											0	0	0	-	0
-																											RW	RW	RW	-	RW

4	OSC_EN	Oscillator Enable 0 Oscillator Disable (Default) 1 Oscillator Enable
3	BGR_EN	Band Gap Reference Enable 0 BGR Disable (Default) 1 BGR Enable
2	TS_IF	Touch Sensor Interrupt Flag 0 No new sensing results 1 In normal mode, this flag indicates that the new sensing results are generated. For next sensing, this flag must be cleared.
1	-	-
0	TS_RUN	Touch Sensor Enable 0 Touch Sensor Disable (Default) 1 Touch Sensor Enable

21.3.4 TS_MODE Touch Sensor Mode Register

Touch Sensor Mode Register.

This register is 8-bit register.

TS_MODE=0x4000_3704

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																								SREF	SC_GAIN	SAP1	SAP0	Reserved		PORT1	PORT0
-																								0	0	0	1	-		0	0
-																								RW	RW	RW	RW	-		RW	RW

7	SREF	External Reference Offset Enable 0 Disable 1 Enable
6	SC_GAIN	Gain Calibration Capacitor Enable 0 Gain Calibration Capacitor Disable (Default) 1 Gain Calibration Capacitor Enable
5 4	SAP[1:0]	Touch Sensor Selection 01 Touch Sensor mode Select (Default) 10 ADC. The result of ADC is stored only at SUM_CH0 register (Note) - It is highly recommended not to use this case - If you need ADC, please use the dedicated ADC.
2	-	-
1 0	PORT[1:0]	Port Configuration During Inactive Status 00 Input Floating 01 Output Low 10 Output High

21.3.5 TS_SUM_CNT Touch Sensor Sum Repeat Count Register

Touch Sensor Sum Repeat Count Register.

This register is 8-bit register.

TS_SUM_CNT=0x4000_3708

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																								TS_SUM_CNT							
-																								0000_0001							
-																								RW							

7 0	TS_SUM_CNT	Touch Sensor Sum Repeat Count

21.3.6 TS_CH_SEL Touch Sensor Channel Selection Register

Touch Sensor Channel Selection Register

TS_CH_SEL=0x4000_370C

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved								CH23_SEL	CH22_SEL	CH21_SEL	CH20_SEL	CH19_SEL	CH18_SEL	CH17_SEL	CH16_SEL	CH15_SEL	CH14_SEL	CH13_SEL	CH12_SEL	CH11_SEL	CH10_SEL	CH09_SEL	CH08_SEL	CH07_SEL	CH06_SEL	CH05_SEL	CH04_SEL	CH03_SEL	CH02_SEL	CH01_SEL	CH00_SEL
-								0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
-								RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

23	CH[23:0]_SEL	Touch Sensor Channel Selection Register	
0		0	Disable (Default)
		1	Enable Touch Key

21.3.7 TS_SLP_CR Touch Sensor Low Pass Filter Control Register

Touch Sensor Low Pass Filter Control Register

This register is 8-bit register.

TS_SLP_CR=0x4000_3714

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																									SLP_C2	SLP_C1	SLP_C0	SLP_R3	SLP_R2	SLP_R1	SLP_R0
-																									0	0	0	0	0	0	1
-																									RW	RW	RW	RW	RW	RW	RW

6	SLP_C[2:0]	Capacitor Trimming for Input Low Pass Filter	
4		000	0pF
		001	4pF
		010	8pF
		011	12pF
		100	16pF
		101	20pF
		110	24pF
		111	28pF
3	SLP_R[3:0]	Resistor Trimming for Input Low Pass Filter	
0		0000	Channel open
		0001	0k
		0010	5k
		0100	10k
		1000	20k
		1110	2.8k
		0110	3.3k
		1010	4.0k
		1100	6.7k

21.3.8 TS_ADC_CH_SEL ADC Channel Selection Register

ADC Channel Selection Register

TS_ADC_CH_SEL=0x4000_3718

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved								CH23_SEL	CH22_SEL	CH21_SEL	CH20_SEL	CH19_SEL	CH18_SEL	CH17_SEL	CH16_SEL	CH15_SEL	CH14_SEL	CH13_SEL	CH12_SEL	CH11_SEL	CH10_SEL	CH09_SEL	CH08_SEL	CH07_SEL	CH06_SEL	CH05_SEL	CH04_SEL	CH03_SEL	CH02_SEL	CH01_SEL	CH00_SEL
-								0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
-								RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

23 0	CH[23:0]_SEL	ADC Channel Selection	
		0	Disable (Default)
		1	Enable

21.3.9 TS_INTEG_CNT Touch Sensor Sensing Integration Count Register

Touch Sensor Integration Count Register.

This register is 8-bit register.

TS_INTEG_CNT=0x4000_371C

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																								TS_INTEG_CNT							
-																								0x32							
-																								RW							

7 0	TS_INTEG_CNT	Touch Sensor Sensing Integration Count

21.3.10 TS_FREQ_NUM Touch Sensor Frequency Number Register

Touch Sensor Frequency Number Register.

This register is 8-bit register.

TS_FREQ_NUM=0x4000_3720

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																								TS_INTEG_CNT							
-																								0xFF							
-																								RW							

7 0	TS_FREQ_NUM	Touch Sensor Frequency Number

This register indicates the number of steps for frequency delta

21.3.11 TS_FREQ_DEL Touch Sensor Frequency Delta Register

Touch Sensor Frequency Delta Register.

This register is 8-bit register.

TS_FREQ_DEL=0x4000_3724

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																								TS_FREQ_DEL							
-																								0x00							
-																								RW							

7 0	TS_FREQ_DEL	Touch Sensor Frequency Delta Register

NOTE) This register indicates the frequency difference in every integration

21.3.12 TS_CLK_CFG Touch Sensor Clock Configuration Register

Touch Sensor Clock Configuration Register

This register is 8-bit register.

TS_CLK_CFG=0x4000_3728

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																								ACLKSEL	ACLKDIV2	ACLKDIV1	ACLKDIV0	TSCLKOE	TSCLKDIV2	TSCLKDIV1	TSCLKDIV0
-																								0	0	1	1	0	0	0	0
-																								RW	RW	RW	RW	RW	RW	RW	RW

7	ACLKSEL	ADC Clock Source Select
		0 Touch Sensor Clock
		1 System MCU Clock
6 4	ACLKDIV[2:0]	ADC Clock Divider
		000 OSC_{sys} / 1 (48MHz)
		001 OSC_{sys} / 2 (24MHz)
		010 OSC_{sys} / 4 (12MHz)
		011 OSC_{sys} / 8 (6MHz, default)
		100 OSC_{sys} / 16
		101 OSC_{sys} / 32
		110 OSC_{sys} / 64
		111 OSC_{sys} / 128
3	TSCLKOE	Divided Touch Sensor Clock Output Enable
		0 Clock Output Disable (Default)
		1 Clock Output Enable
2 0	TSCLKDIV[2:0]	Touch Sensor Clock Divider
		000 OSC_{ts} / 1 (27MHz)
		001 OSC_{ts} / 2
		010 OSC_{ts} / 4
		011 OSC_{ts} / 8
		100 OSC_{ts} / 16
		101 OSC_{ts} / 32
		110 OSC_{ts} / 64
		111 OSC_{ts} / 128

After TS_RUN is cleared, please change the clock divide.

21.3.13 TS_TRIM_OSC Touch Sensor RING Oscillator Trimming Selection Register

Touch Sensor RING Oscillator Trimming Selection Register.

This register is 8-bit register.

TRIM_OSC=0x4000_372C

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																								TRIM_OSC							
-																								0xB8							
-																								RW							

7	TRIM_OSC	Touch Sensor RING Oscillator Trimming Selection	
0		0x00	35MHz (maximum)
		0xB8	20MHz (default)
		0xFF	3.5MHz (minimum)

21.3.14 TS_TRIM_A_OSC Touch Sensor RING Oscillator Trimming for ADC Register

Touch Sensor RING Oscillator Trimming for ADC Register.

This register is 8-bit register.

TRIM_A_OSC=0x4000_3730

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																								TRIM_A_OSC							
-																								0xFF							
-																								RW							

7	TRIM_A_OSC	Touch Sensor RING Oscillator Trimming for ADC	
0		0x00	35MHz (maximum)
		0xB8	20MHz (default)
		0xFF	3.5MHz (minimum)

21.3.15 TS_SCI Touch Sensor Clock Configuration Register

Touch Sensor Input Capacitor Selection Register

This register is 8-bit register.

TS_SCI=0x4000_3734

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																								IBIAS_TRIM3	IBIAS_TRIM2	IBIAS_TRIM1	IBIAS_TRIM0	Reserved	SCI2	SCI1	SCI0
-																								0	0	1	1	-	1	0	0
-																								RW	RW	RW	RW	-	RW	RW	RW

7	IBIAS_TRIM[3:0]	BGR Current Bias Control
4		000
		001
		010
		011
		100
		101
		110
		111
2	SCI[2:0]	Touch Sensor Input Capacitor Selection
0		000 1.2pF
		001 2.4pF
		010 3.6pF
		011 4.8pF
		100 6.0pF
		101 7.2pF
		110 8.4pF
		111 9.6pF

21.3.16 TS_SCC Touch Sensor Conversion Capacitor Selection Register

Touch Sensor Conversion Capacitor Selection Register

This register is 8-bit register.

TS_SCC=0x4000_3738

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																													SCC2	SCC1	SCC0
-																													1	0	0
-																													RW	RW	RW

2	SCC[2:0]	Touch Sensor Conversion Capacitor Selection
0		000 2.4pF
		001 4.8pF
		010 7.2pF
		011 9.6pF
		100 12.0pF
		101 14.4pF
		110 16.8pF
		111 19.2pF

21.3.17 TS_SVREF Touch Sensor VREF Resistor Selection Register

Touch Sensor VREF Resistor Selection Register

This register is 8-bit register.

TS_SVREF=0x4000_373C

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																												SVREF3	SVREF2	SVREF1	SVREF0
-																												0	1	0	0
-																												RW	RW	RW	RW

3	SVREF[3:0]	Touch Sensor VREF Resistor Selection
0	0000	Open
	0001	2.5k
	0010	5k
	0100	10k
	1000	20k
	1111	1.3k

21.3.18 TS_TAR Touch Sensor Integration AMP Reset Register

Touch Sensor Integration AMP Reset Register.

This register is 8-bit register.

TS_TAR=0x4000_3740

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																								TAR							
-																								0x20							
-																								RW							

7	TAR	Touch Sensor Integration AMP Reset Register
0		

21.3.19 TS_TRST Touch Sensor Reset time of Sensing Register

Touch Sensor Reset time of Sensing Register.

This register is 8-bit register.

TS_TRST=0x4000_3744

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																								TRST							
-																								0x03							
-																								RW							

7	TRST	Touch Sensor Reset time of Sensing
0		

21.3.20 TS_TDRV Touch Sensor Driving time of Sensing Register

Touch Sensor Driving time of Sensing Register.

This register is 8-bit register.

TS_TDRV=0x4000_3748

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																								TDRV							
-																								0x03							
-																								RW							

7	TDRV	Touch Sensor Driving time of Sensing
0		

21.3.21 TS_TINT Touch Sensor Integration time of Sensing Register

Touch Sensor Integration time of Sensing Register.

This register is 8-bit register.

TS_TINTP=0x4000_374C

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																								TINT							
-																								0x14							
-																								RW							

7	TINT	Touch Sensor Integration time of Sensing
0		

21.3.22 TS_TD Touch Sensor Differential AMP Sampling Register

Touch Sensor Differential AMP Sampling Register

This register is 8-bit register.

TS_TDIFP=0x4000_3750

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																								TD							
-																								0x20							
-																								RW							

7	TD	Touch Sensor Differential AMP Sampling
0		

21.3.23 TS_TWR Touch Sensor Wait Time Register

Touch Sensor Wait Time Register

This register is 8-bit register.

TS_TWR=0x4000_3754

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																								TWR							
-																								0x10							
-																								RW							

7	TWR	Touch Sensor Wait Time
0		

21.3.24 TS_TLED LED stable time Register

LED stable Time Register

This register is 8-bit register.

TS_TLED=0x4000_3758

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																								TLED							
-																								0x00							
-																								RW							

7	TLED	LED stable Time
0		

CHAPTER 22. LCD DRIVER

22.1 OVERVIEW

The LCD driver is controlled by the LCD control register (LCD_CR) and LCD driver bias and contrast control register (LCD_BCCR). The LCLK[1:0] determines the frequency of COM signal scanning of each segment output. A RESET clears the LCD control register LCD_CR and LCD_BCCR values to logic '0'.

The LCD display can continue operating during IDLE and STOP modes.

The clock and duty for LCD driver is automatically initialized by hardware, whenever LCD_CR register data value is rewritten. So, don't rewrite LCD_CR frequently.

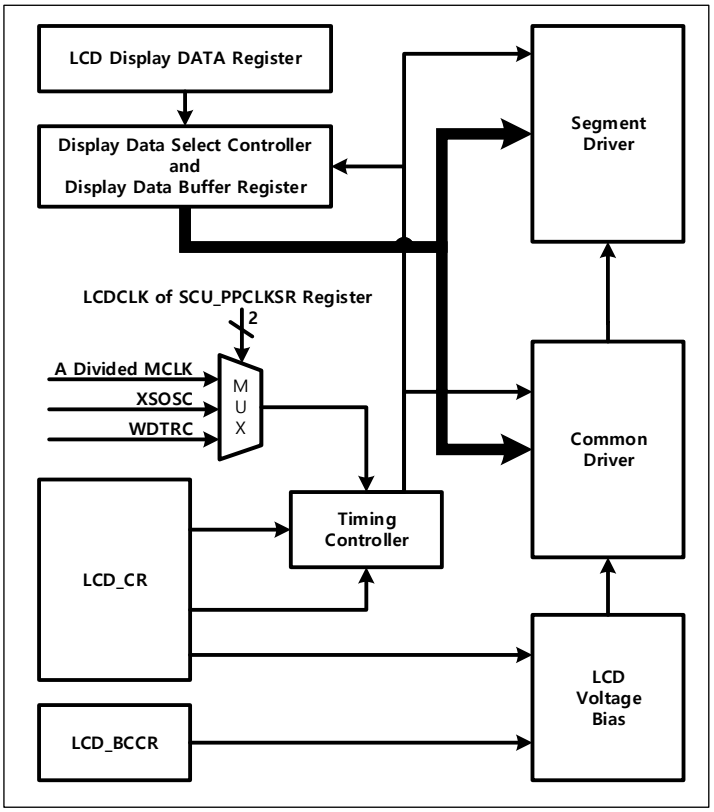


Figure 22.1 Block Diagram

22.2 Pin description

Table 22.1 LCD Driver External Signals

PIN NAME	TYPE	DESCRIPTION
VLC0~3	A	LCD External Bias volatage input
COM0 ~ 7	O	LCD common signal outputs
SEG0 ~ SEG43	O	LCD segment signal outputs

22.3 REGISTERS

Base address of LCD driver is below.

Table 22.2 LCD driver base address

NAME	BASE ADDRESS
LCD	0x4000_5000

Table 22.3 LCD driver Register map

Register Name	Offset	Access Type	Description	Initial Value	Ref
LCD_CR	0x00	RW	LCD Driver Control Register	0x0000_0000	23.3.1
LCD_BCCR	0x04	RW	LCD Automatic Bias and Contrast Control Register	0x0000_0000	23.3.2
LCD_BSSR	0x0C	RW	LCD Bias Source Selection Register	0x0000_0000	23.3.3
LCD_DRn (n=0-27)	0x10-0x2B	RW	LCD Display Data Register 0 – 27	Unknown	23.3.4

22.3.1 LCD_CR LCD Driver Control Register

LCD Driver Control Register is 32-bit register. This Register is able to 32/16/8-bit access.

LCD_CR=0x4000_5000

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6	5 4 3	2 1	0
Reserved			IRSEL	DBS	LCLK	DISP
-			00	000	00	0
-			RW	RW	RW	RW

7	IRSEL	Internal LCD Bias Dividing Resistor Selection bits.	
6		00	RLCD3: 105/105/80[kΩ] @(1/2)/(1/3)/(1/4) bias.
		01	RLCD1: 10/10/10[kΩ] @(1/2)/(1/3)/(1/4) bias.
		10	RLCD2: 66/66/50[kΩ] @(1/2)/(1/3)/(1/4) bias.
		11	RLCD4: 320/320/240[kΩ] @(1/2)/(1/3)/(1/4) bias.
5	DBS	LCD Duty and Bias Selection bits.	
3		000	1/8 duty, 1/4 bias.
		001	1/6 duty, 1/4 bias.
		010	1/5 duty, 1/3 bias.
		011	1/4 duty, 1/3 bias.
		100	1/3 duty, 1/3 bias.
		101	1/3 duty, 1/2 bias
		Others	Reserved.
2	LCLK	LCD Clock Selection bits (When fLCD = 32.768kHz).	
1		00	128Hz.
		01	256Hz.
		10	512Hz.
		11	1024Hz.
0	DISP	LCD Display Control bit.	
		0	Display off.
		1	Normal display on.

22.3.2 LCD_BCCR LCD Automatic Bias and Contrast Control Register

LCD Automatic Bias and Contrast Control Register is 32-bit register. This Register is able to 32/16/8-bit access.

LCD_BCCR=0x4000_5004

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13	12	11	10 9 8	7 6	5	4	3 2 1 0
Reserved			LCDABC	Reserved	BMSEL	Reserved	LCTEN	Reserved	VLCD
-			0	-	000	-	0	-	0000
-			RW	-	RW	-	RW	-	RW

12	LCDABC	LCD Automatic Bias Control bit.	
		0	LCD automatic bias is off.
		1	LCD automatic bias is on.
10 8	BMSEL	"Bias Mode A" Time Selection bits. Refer to the figure "LCD automatic bias control".	
		000	"Bias Mode A" for 1-clock of fLCD.
		001	"Bias Mode A" for 2-clock of fLCD.
		010	"Bias Mode A" for 3-clock of fLCD.
		011	"Bias Mode A" for 4-clock of fLCD.
		100	"Bias Mode A" for 5-clock of fLCD.
		101	"Bias Mode A" for 6-clock of fLCD.
		110	"Bias Mode A" for 7-clock of fLCD.
		111	"Bias Mode A" for 8-clock of fLCD.
5	LCTEN	LCD Driver Contrast Control bit.	
		0	Disable LCD driver contrast.
		1	Enable LCD driver contrast.
3 0	VLCD	VLC0 Voltage Control when the contrast is enabled.	
		0000	LVC0 = VDD x 16/31 step
		0001	LVC0 = VDD x 16/30 step
		0010	LVC0 = VDD x 16/29 step
		0011	LVC0 = VDD x 16/28 step
		0100	LVC0 = VDD x 16/27 step
		0101	LVC0 = VDD x 16/26 step
		0110	LVC0 = VDD x 16/25 step
		0111	LVC0 = VDD x 16/24 step
		1000	LVC0 = VDD x 16/23 step
		1001	LVC0 = VDD x 16/22 step
		1010	LVC0 = VDD x 16/21 step
		1011	LVC0 = VDD x 16/20 step
		1100	LVC0 = VDD x 16/19 step
		1101	LVC0 = VDD x 16/18 step
		1110	LVC0 = VDD x 16/17 step
		1111	LVC0 = VDD x 16/16 step

Note)

1. The above LCD contrast step is based on 1/3 bias with 66kΩ RLCD and on 1/4 bias with 50kΩ RLCD.

22.3.3 LCD_BSSR LCD Bias Source Selection Register

LCD Bias Source Selection Register is 32-bit register. This Register is able to 32/16/8-bit access.

LCD_BSSR=0x4000_500C

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																				VLE_EN	Reserved	LCDDR	LCDEPEN	VLC3EN	VLC2EN	VLC1EN	VLC0EN	Reserved			
-																				0	-	0	0	0	0	0	0	-			
-																				RW	-	RW	RW	RW	RW	RW	RW	-			

11	VLE_EN	External bias test register.
	0	Test mode is on and external bias cannot be used
	1	External bias can be used normally with test mode off
9	LCDDR	LCD Driving Resistor for Bias Select
	0	Internal LCD driving resistors for bias
	1	External LCD driving resistors for bias
8	LCDEPEN	LCD External Bias Path Enable bit
	0	disable
	1	Enable
7	VLC3EN	Extenal Bias VLC3 Enable bit
	0	Disable VLC3
	1	Enable VLC3
6	VLC2EN	Extenal Bias VLC2 Enable bit
	0	Disable VLC2
	1	Enable VLC2
5	VLC1EN	Extenal Bias VLC1 Enable bit
	0	Disable VLC1
	1	Enable VLC1
4	VLC0EN	Extenal Bias VLC0 Enable bit
	0	Disable VLC0
	1	Enable VLC0

22.3.4 LCD_DRx LCD Display Data Register x

LCD Display Data Register x are 32-bit register. This Register is able to 32/16/8-bit access. (x = 0 to 10)

LCD_DRx=0x4000_5010 to 0x4000_502B

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LCDDR(4xn+3)								LCDDR(4xn+2)									LCDDR(4xn+1)							LCDDR(4xn+0)							
0x00								0x00									0x00							0x00							
RW								RW									RW							RW							

31 24	LCDDR(4xn+3)	LCD Display Data bits.
23 16	LCDDR(4xn+2)	LCD Display Data bits.
15 8	LCDDR(4xn+1)	LCD Display Data bits.
7 0	LCDDR(4xn+0)	LCD Display Data bits.

22.4 Functional Description

22.4.1 LCD Display RAM Organization

Display data are stored to the display data area in the external data memory.

The display data which stored to the display external data area (address 0x4000_5010-0x4000_503B) are read automatically and sent to the LCD driver by the hardware. The LCD driver generates the segment signals and common signals in accordance with the display data and drive method. Therefore, display patterns can be changed by only overwriting the contents of the display external data area with a program.

Figure 23.2 shows the correspondence between the display external data area and the COM/SEG pins. The LCD is turned on lights when the display data is “1” and turned off when “0”.

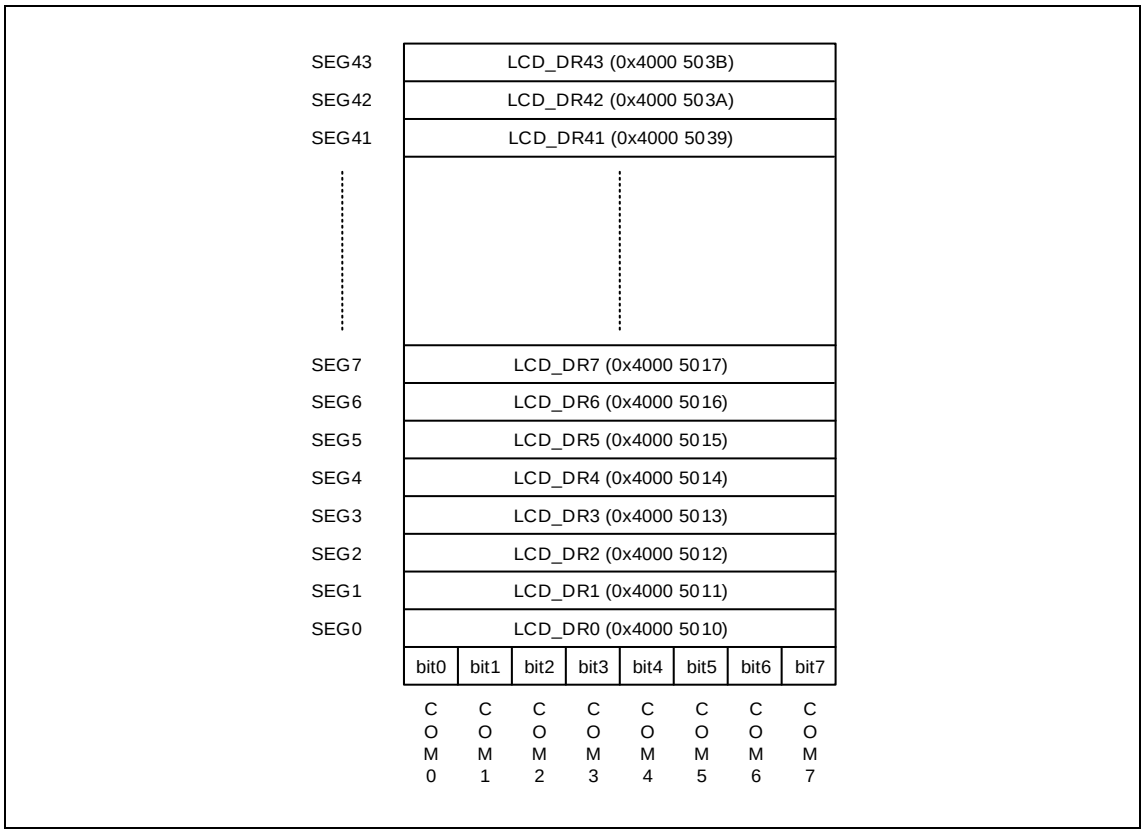


Figure 22.2. LCD Display RAM

22.4.2 LCD Signal Waveform

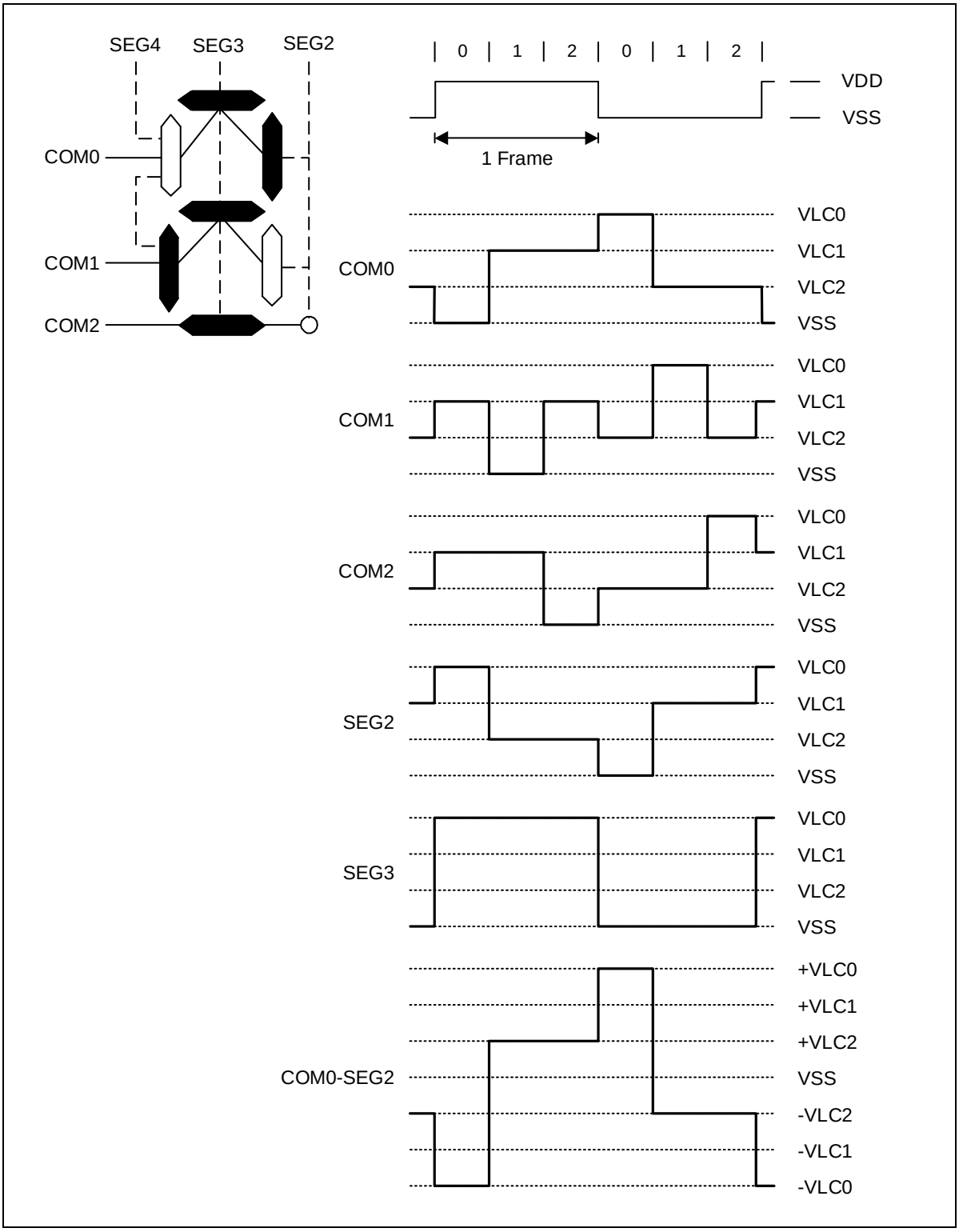


Figure 22.3. LCD Signal Waveforms (1/3 Duty, 1/3 Bias)

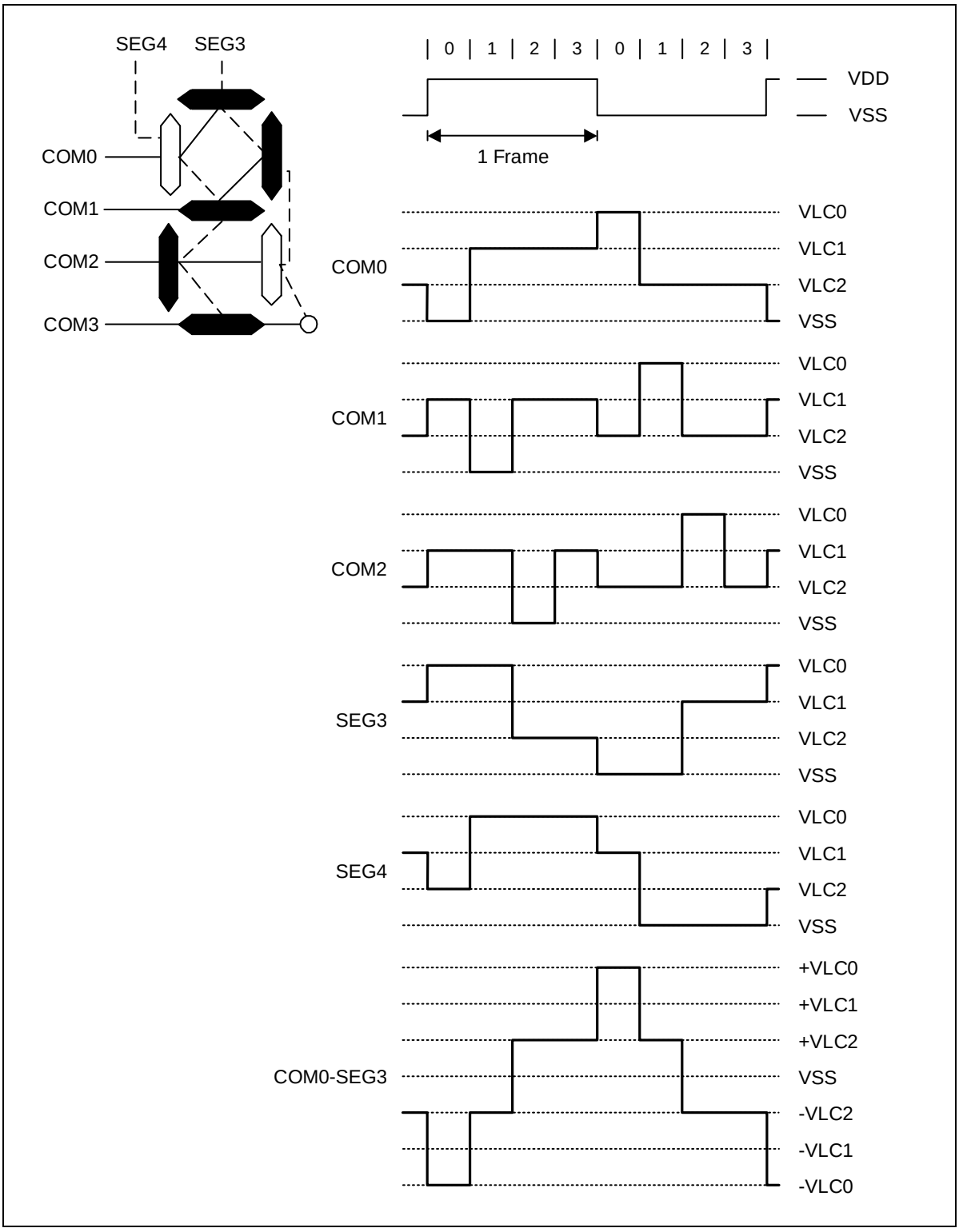


Figure 22.4. LCD Signal Waveforms (1/4 Duty, 1/3 Bias)

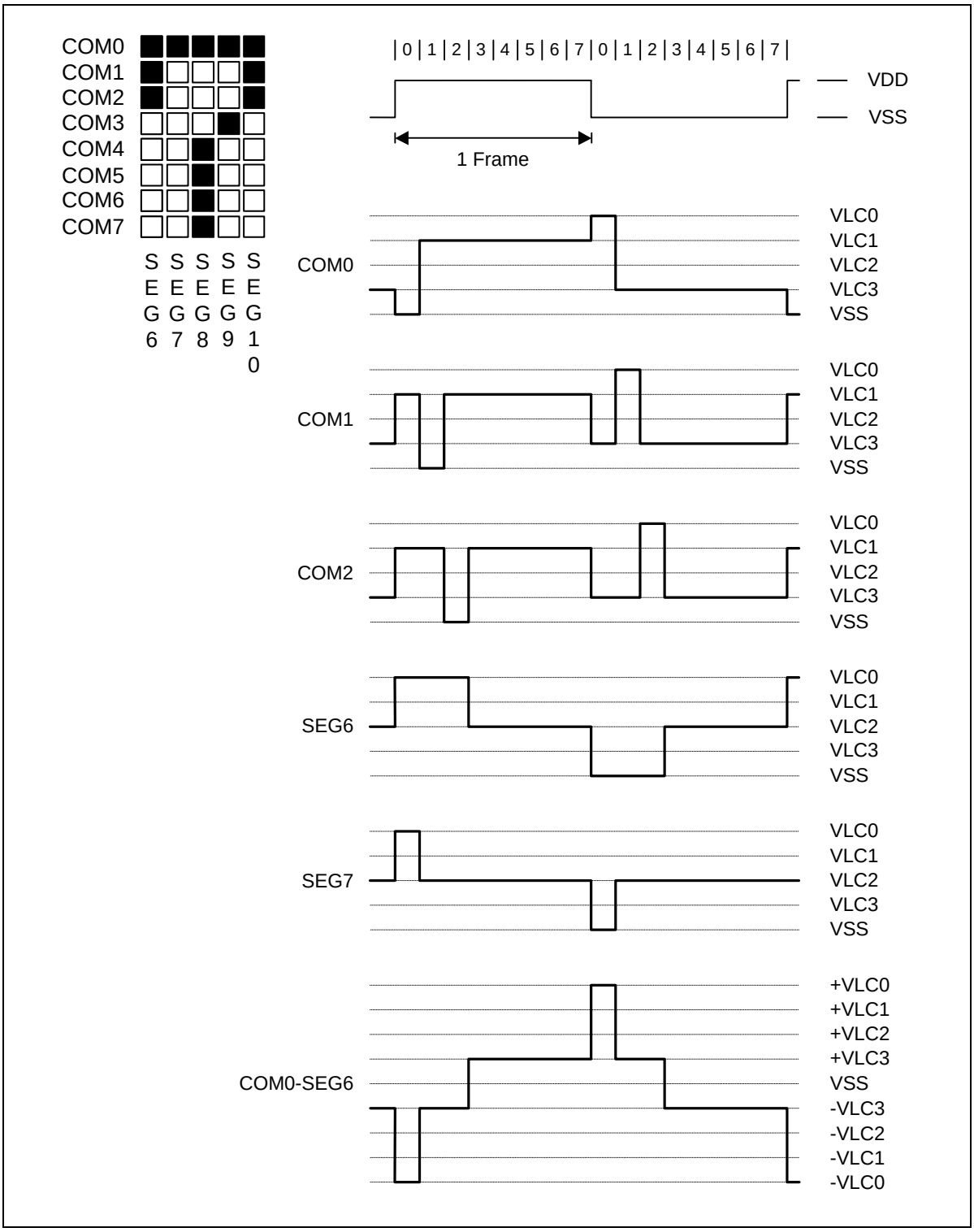
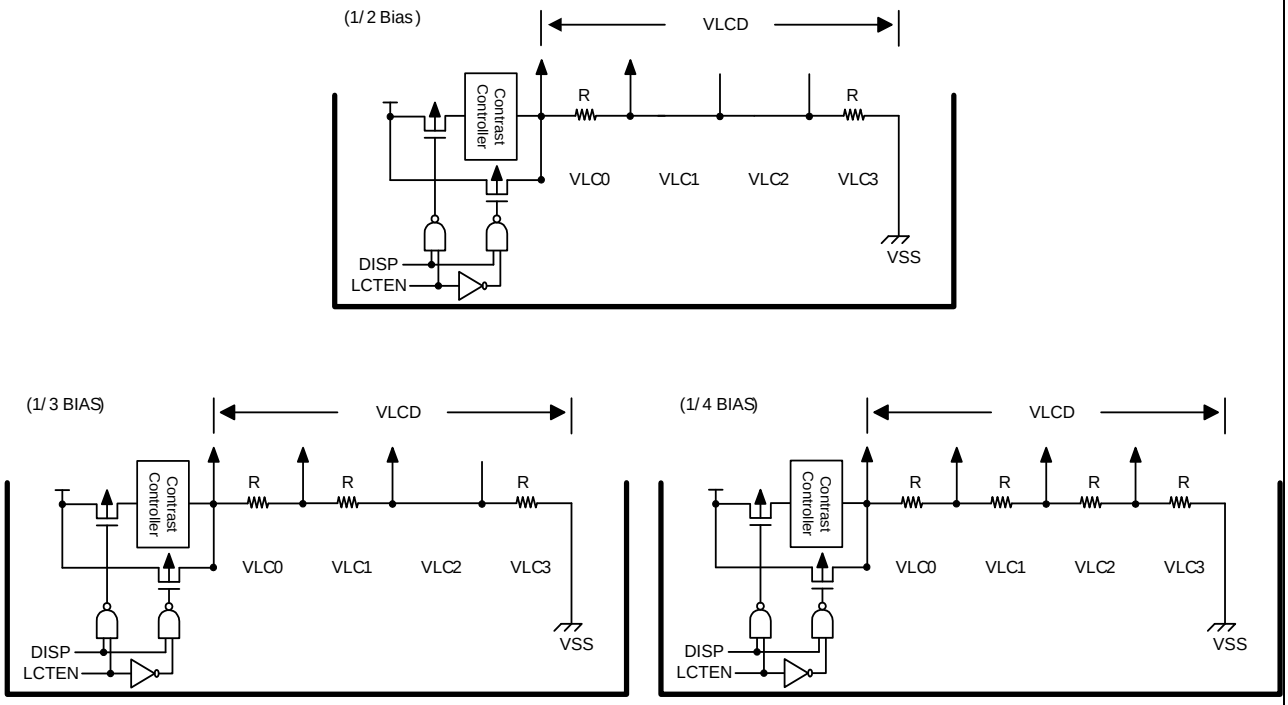


Figure 22.5. LCD Signal Waveforms (1/8 Duty, 1/4 Bias)

22.4.3 Internal Resistor Bias Connection

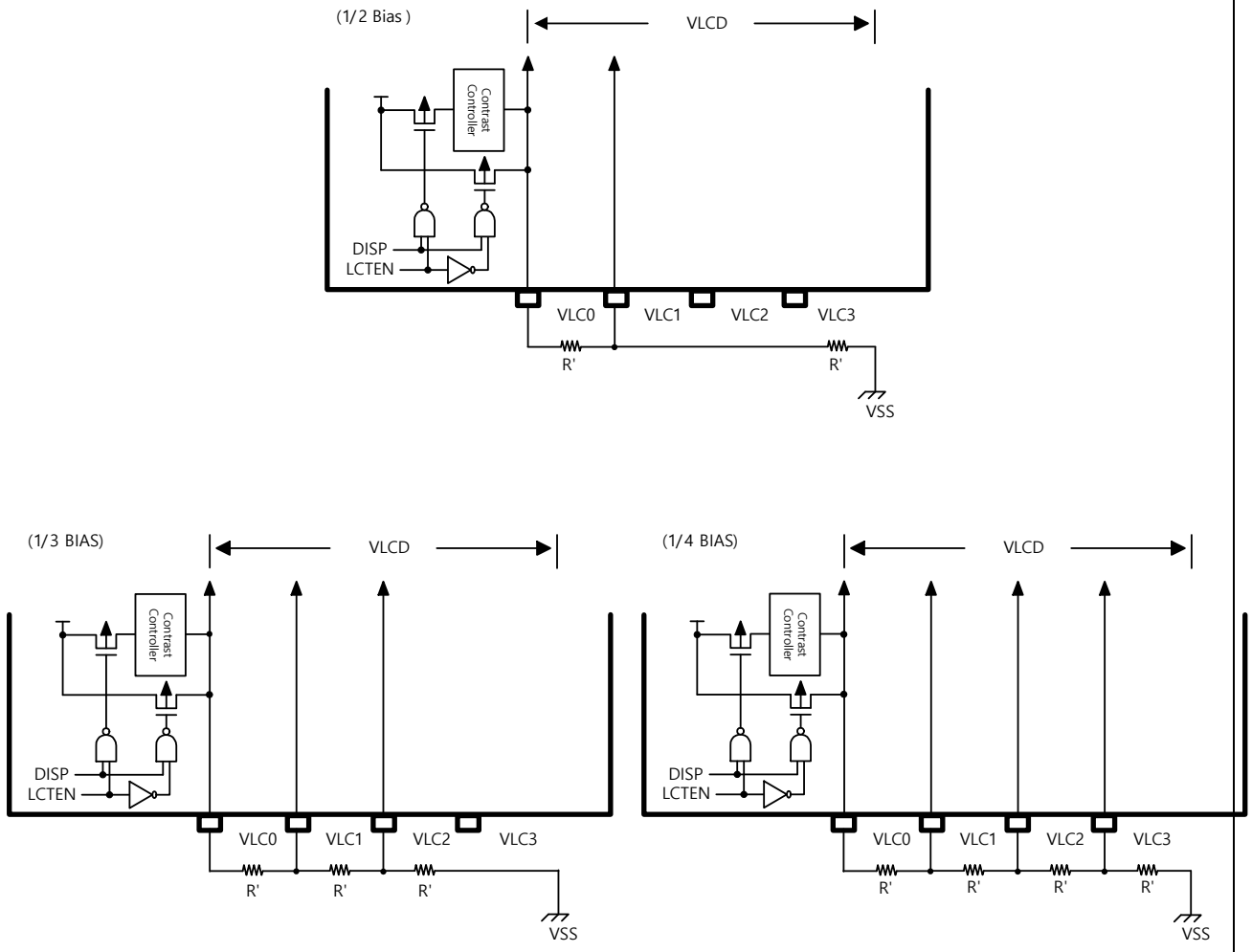


NOTE)

1. When 1/2 bias are selected, the VLC1, VLC2 and VLC3 are internally connected.
2. When 1/3 bias are selected, the VLC2 and VLC3 are internally connected.
3. When the internal resistors are selected, all the P73/VLC0, P72/VLC1, P71/VLC2 and P70/VLC3 pins can be used for normal I/O.

Figure 22.6. Internal Resistor Bias Connection

22.4.4 External Resistor Bias Connection

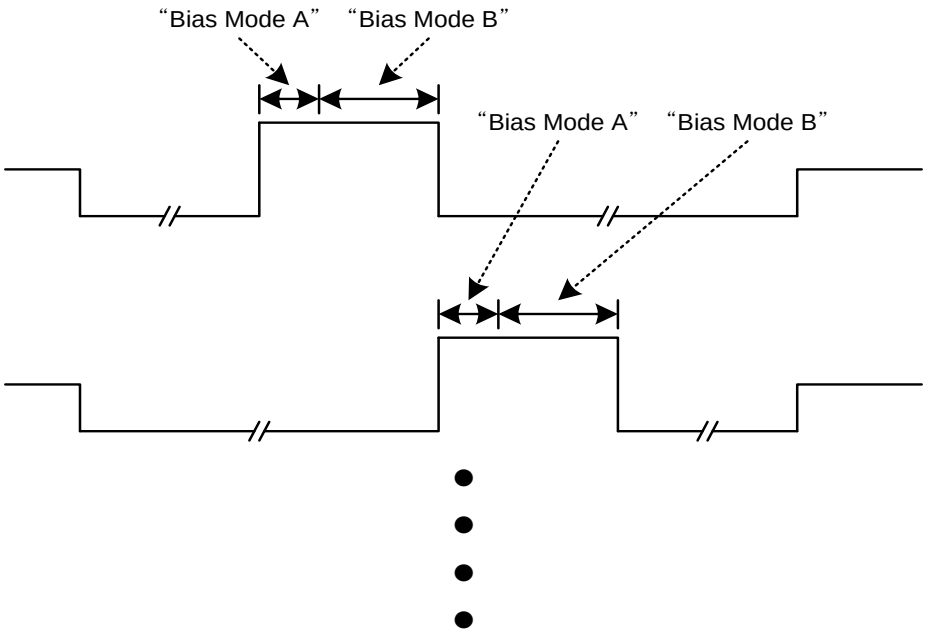


NOTE)

1. When the external resistor bias is selected, the internal resistors for bias are disconnected.
2. When the external resistor bias is selected, the dividing resistors should be connected like the above figure and the needed bias pins should be selected as the LCD bias function pins (VLC0, VLC1, VLC2 and VLC3) by PE_MOD & PE_ASFR1 register.
3. it must set the LCDDR LCDEN VLCnEN of the LCD_BSSR register to '1'. And the others must be set to '0'.

Figure 22.7. External Resistor Bias Connection

22.4.5 LCD Automatic Bias Control Timing



Notes)

Refer to the below when the LCD automatic bias is on

1. “Bias Mode A”: Always RLCD1 (10kΩ).
2. “Bias Mode B”: A LCD bias dividing resistor which is selected by IRSEL[1:0] bits

Figure 22.8. LCD Automatic Bias Control Timing Diagram

CHAPTER 23. LED DRIVER

23.1 OVERVIEW

LED drive contains a 27 ICOM X 11 ISEG output pin. It is also shared with Touch pin.

By setting LED CONTROL REGISTER1, there are two mode that can be shared with touch function.

The controller consists of display data RAM memory, COM and SEG generator.

ICOM0-ICOM26 and ISEG0-ISEG11 pin can also be used as I / O pins. COMOE1, COMOE2, COMOE3, COMOE4 and SEGOE1,SEGOE2 registers are used to select ISEG0-10, ICOM0 – ICOM26.

During the power-on reset , reset pin, low voltage reset or watchdog reset , LED is turned off

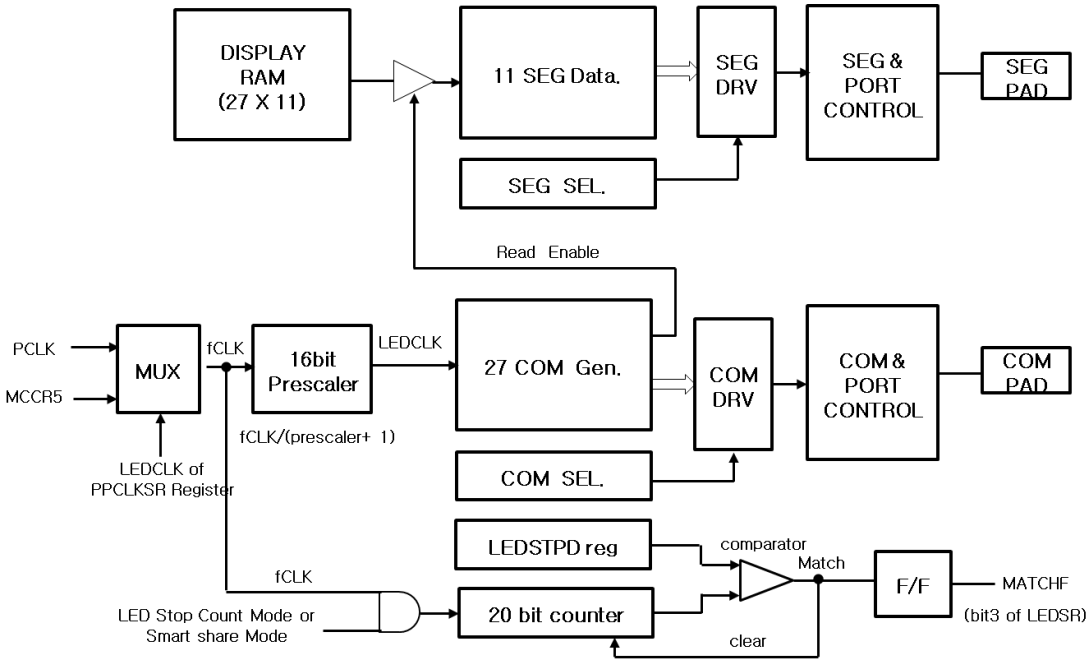


Figure 23.1. Block Diagram

23.2 Pin Description

Table 23.1 External pin

PIN NAME	TYPE	DESCRIPTION
ICOM0 ~ ICOM27	O	LED common signal outputs
ISEG0 ~ ISEG10	O	LED segment signal outputs
R-SET	A	LED Segment current setting

NOTE) For using the LED block, Resistor of 4.7 kOhm must be in between R-set and GND.

23.3 REGISTERS

Base address of LED driver is below.

It is strongly recommended LEDEN(bit1 of LEDCON1) to be set before other registers set and LEDST(bit0 of LEDCON1) to be set at the end of other registers set.

Table 23.1 Base Address of each channel

NAME	BASE ADDRESS
LED	0x4000_6000

Table 23.2 LED Register map

Register Name	Offset	Access Type	Description	Initial Value	Ref
LED _COMOE	0x00	RW	COM Ouput Enable Register	0x0000_0000	24.3.1
LED _SEGOE	0x04	RW	SEG Output Enable Register	0x0000_0000	24.3.2
LED _PRESD	0x08	RW	LED Prescaler Data Register	0x0000_0000	24.3.3
LED _COMER	0x0C	RW	COM Enable Register	0x0000_0000	24.3.4
LED _COMPWID	0x10	RW	COM Pulse Width Control Register	0x0000_0000	24.3.5
LED _DIMM0	0x14	RW	COM Dimming Control Register0	0x0000_0000	24.3.6
LED _DIMM1	0x18	RW	COM Dimming Control Register1	0x0000_0000	24.3.7
LED _DIMM2	0x1C	RW	COM Dimming Control Register2	0x0000_0000	24.3.8
LED _DIMM3	0x20	RW	COM Dimming Control Register3	0x0000_0000	24.3.9
LED _DIMM4	0x24	RW	COM Dimming Control Register4	0x0000_0000	24.3.10
LED _DIMM5	0x28	RW	COM Dimming Control Register5	0x0000_0000	24.3.11
LED _DIMM6	0x2C	RW	COM Dimming Control Register6	0x0000_0000	24.3.12
LED _STPD	0x30	RW	LED STOP Duration Register	0x0000_0000	24.3.13
LED _SR	0x34	RW	LED STATUS Register	0x0000_0001	24.3.14
LED _CON2	0x38	RW	LED Control Register2	0x0000_0000	24.3.15
LED _CON1	0x3C	RW	LED Control Register1	0x0000_0000	24.3.16

23.3.1 LED_COMOE COM Output Enable Register

COM Output enable Register is 27-bit register. This Register is able to 32/16/8-bit access.

LED_COMOE=0x4000_6000

31 30 29 28 27	26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
Reserved	COMOE4	COMOE3	COMOE2	COMOE1
-	0x00	0000_0000	0000_0000	0000_0000
-	RW	RW	RW	RW

26 24	COMOE4	Port Mode Select4	
		0	Normal I/O PORT Select
		7	COM[26:24] Select
23 16	COMOE3	Port Mode Select3	
		00	Normal I/O PORT Select
		FF	COM[23:16] Select
15 8	COMOE2	Port Mode Select2	
		00	Normal I/O PORT Select
		FF	COM[15:8] Select
7 0	COMOE1	Port Mode Select1	
		00	Normal I/O PORT Select
		FF	COM[7:0] Select

23.3.2 LED_SEGOE SEG Output Enable Register

SEG Output enable Register is 11-bit register. This Register is able to 32/16/8-bit access.

LED_SEGOE=0x4000_6004

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																					SEGOE2			SEGOE1							
-																					000			0000_0000							
-																					RW			RW							

10 8	SEGOE2	Port Mode Select2	
		0	Normal I/O PORT Select
		7	SEG10:8] Select
7 0	SEGOE1	Port Mode Select1	
		0	Normal I/O PORT Select
		FF	SEG[7:0] Select

23.3.3 LED_PRESD LED Prescaler Data Register

LED Prescaler Data Register is 16-bit register. This Register is able to 32/16/8-bit access.

LED_PRESD =0x4000_6008

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																PRESD2								PRESD1							
-																0000_0000								0000_0000							
-																RW								RW							

15 0	PRESD	Pre-scale value of LED clock(PRESD = {PRESD2,PRESD1}) LED Clock = fCLK/(PRESD + 1) (fCLK is a selected input clock)

23.3.4 LED_COMER COM Enable Register

COM Enable Register is 27-bit register. This Register is able to 32/16/8-bit access.

LED_COMER=0x4000_600C

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved					COM26	COM25	COM24	COM23	COM22	COM21	COM20	COM19	COM18	COM17	COM16	COM15	COM14	COM13	COM12	COM11	COM10	COM9	COM8	COM7	COM6	COM5	COM4	COM3	COM2	COM1	COM0
-					0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
-					RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

26 0	COMER[26:0]	Only Selected COM of COM0 and COM26 is active and displayed.
Only COM to use should be written to “1”. Only One COM is allowed.		

23.3.5 LED_COMPWID COM Pulse Width Control Register

COM Pulse Width Control Register is 8-bit register. This Register is able to 32/16/8-bit access.

LED_COMPWID=0x4000_6010

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																								COMPWID							
-																								0000_0000							
-																								RW							

7 0	COMPWID	COM Pulse Width Control bits COM Width= LED CLK/(COMPWID + 1) (LED CLK is Prescaler output clock)

23.3.6 LED_DIMM0 COM Dimming Control Register0

DIMM0 Dimming Control Register is 32-bit register. This Register is able to 32/16/8-bit access.

LED_DIMM0=0x4000_6014

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COMDIMM3								COMDIMM2								COMDIMM1								COMDIMM0							
0000_0000								0000_0000								0000_0000								0000_0000							
RW								RW								RW								RW							

31 24	COMDIMM3	COM3 Dimming Control bits
	00~FF	Dimmed COM Width = COMPWID - Overlaptime – LEDCLK* COMDIMM3
23 16	COMDIMM2	COM2 Dimming Control bits
	00~FF	Dimmed COM Width = COMPWID - Overlaptime – LEDCLK*COMDIMM2
15 8	COMDIMM1	COM1 Dimming Control bits
	00~FF	Dimmed COM Width = COMPWID - Overlaptime – LEDCLK*COMDIMM1
7 0	COMDIMM0	COM0 Dimming Control bits
	00~FF	Dimmed COM Width = COMPWID - Overlaptime – LEDCLK*COMDIMM0

All COMDIMM should be less than (COMPWID – Overlaptime)
If not, COM is not displayed!!!

23.3.7 LED_DIMM1 COM Dimming Control Register1

DIMM1 Dimming Control Register are 32-bit register. This Register is able to 32/16/8-bit access.

LED_DIMM1=0x4000_6018

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
COMDIMM7	COMDIMM6	COMDIMM5	COMDIMM4
0000_0000	0000_0000	0000_0000	0000_0000
RW	RW	RW	RW

31 24	COMDIMM7	COM7 Dimming Control bits 00~FF	Dimmed COM Width = COMPWID - Overlaptime – LEDCLK*COMDIMM7
23 16	COMDIMM6	COM6 Dimming Control bits 00~FF	Dimmed COM Width = COMPWID - Overlaptime – LEDCLK*COMDIMM6
15 8	COMDIMM5	COM5 Dimming Control bits 00~FF	Dimmed COM Width = COMPWID - Overlaptime – LEDCLK*COMDIMM5
7 0	COMDIMM4	COM4 Dimming Control bits 00~FF	Dimmed COM Width = COMPWID - Overlaptime – LEDCLK*COMDIMM4

All COMDIMM should be less than (COMPWID – Overlaptime)
If not, COM is not displayed!!!

23.3.8 LED_DIMM2 COM Dimming Control Register2

DIMM2 Dimming Control Register is 32-bit register. This Register is able to 32/16/8-bit access.

LED_DIMM2=0x4000_601C

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COMDIMM11								COMDIMM10								COMDIMM9								COMDIMM8							
0000_0000								0000_0000								0000_0000								0000_0000							
RW								RW								RW								RW							

31 24	COMDIMM11	COM11 Dimming Control bits
	00~FF	Dimmed COM Width = COMPWID - Overlaptime – LEDCLK*COMDIMM11
23 16	COMDIMM10	COM10 Dimming Control bits
	00~FF	Dimmed COM Width = COMPWID - Overlaptime – LEDCLK*COMDIMM10
15 8	COMDIMM9	COM9 Dimming Control bits
	00~FF	Dimmed COM Width = COMPWID - Overlaptime – LEDCLK*COMDIMM9
7 0	COMDIMM8	COM8 Dimming Control bits
	00~FF	Dimmed COM Width = COMPWID - Overlaptime – LEDCLK*COMDIMM8
All COMDIMM should be less than (COMPWID – Overlaptime) If not, COM is not displayed!!!		

23.3.9 LED_DIMM3 COM Dimming Control Register3

DIMM3 Dimming Control Register is 32-bit register. This Register is able to 32/16/8-bit access.

LED_DIMM3=0x4000_6020

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COMDIMM15								COMDIMM14								COMDIMM13								COMDIMM12							
0000_0000								0000_0000								0000_0000								0000_0000							
RW								RW								RW								RW							

31 24	COMDIMM15	COM15 Dimming Control bits	
		00~FF	Dimmed COM Width = COMPWID - Overlaptime – LEDCLK*COMDIMM15
23 16	COMDIMM14	COM14 Dimming Control bits	
		00~FF	Dimmed COM Width = COMPWID - Overlaptime – LEDCLK*COMDIMM14
15 8	COMDIMM13	COM13 Dimming Control bits	
		00~FF	Dimmed COM Width = COMPWID - Overlaptime – LEDCLK*COMDIMM13
7 0	COMDIMM12	COM12 Dimming Control bits	
		00~FF	Dimmed COM Width = COMPWID - Overlaptime – LEDCLK*COMDIMM12
All COMDIMM should be less than (COMPWID – Overlaptime) If not, COM is not displayed!!!			

23.3.10 LED_DIMM4 COM Dimming Control Register4

DIMM4 Dimming Control Register is 32-bit register. This Register is able to 32/16/8-bit access.

LED_DIMM4=0x4000_6024

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COMDIMM19								COMDIMM18								COMDIMM17								COMDIMM16							
0000_0000								0000_0000								0000_0000								0000_0000							
RW								RW								RW								RW							

31 24	COMDIMM19	COM19 Dimming Control bits
	00~FF	Dimmed COM Width = COMPWID - Overlaptime – LEDCLK*COMDIMM19
23 16	COMDIMM18	COM18 Dimming Control bits
	00~FF	Dimmed COM Width = COMPWID - Overlaptime – LEDCLK*COMDIMM18
15 8	COMDIMM17	COM17 Dimming Control bits
	00~FF	Dimmed COM Width = COMPWID - Overlaptime – LEDCLK*COMDIMM17
7 0	COMDIMM16	COM16 Dimming Control bits
	00~FF	Dimmed COM Width = COMPWID - Overlaptime – LEDCLK*COMDIMM16
All COMDIMM should be less than (COMPWID – Overlaptime) If not, COM is not displayed!!!		

23.3.11 LED_DIMM5 COM Dimming Control Register5

DIMM5 Dimming Control Register is 32-bit register. This Register is able to 32/16/8-bit access.

LED_DIMM5=0x4000_6028

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
COMDIMM23	COMDIMM22	COMDIMM21	COMDIMM20
0000_0000	0000_0000	0000_0000	0000_0000
RW	RW	RW	RW

31 24	COMDIMM23	COM23 Dimming Control bits	
		00~FF	Dimmed COM Width = COMPWID - Overlaptime – LEDCLK*COMDIMM23
23 16	COMDIMM22	COM22 Dimming Control bits	
		00~FF	Dimmed COM Width = COMPWID - Overlaptime – LEDCLK* COMDIMM22
15 8	COMDIMM21	COM21 Dimming Control bits	
		00~FF	Dimmed COM Width = COMPWID - Overlaptime – LEDCLK* COMDIMM21
7 0	COMDIMM20	COM20 Dimming Control bits	
		00~FF	Dimmed COM Width = COMPWID - Overlaptime – LEDCLK*COMDIMM20
All COMDIMM should be less than (COMPWID – Overlaptime) If not, COM is not displayed!!!			

23.3.12 LED_DIMM6 COM Dimming Control Register6

DIMM6 Dimming Control Register is 32-bit register. This Register is able to 32/16/8-bit access.

LED_DIMM6=0x4000_602C

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
Reserved	COMDIMM26	COMDIMM25	COMDIMM24
-	0000_0000	0000_0000	0000_0000
-	RW	RW	RW

23 16	COMDIMM26	COM26 Dimming Control bits	
		00~FF	Dimmed COM Width = COMPWID - Overlaptime – LEDCLK*COMDIMM26
15 8	COMDIMM25	COM25 Dimming Control bits	
		00~FF	Dimmed COM Width = COMPWID - Overlaptime – LEDCLK*COMDIMM25
7 0	COMDIMM24	COM24 Dimming Control bits	
		00~FF	Dimmed COM Width = COMPWID - Overlaptime – LEDCLK*COMDIMM24
All COMDIMM should be less than (COMPWID – Overlaptime) If not, COM is not displayed!!!			

23.3.13 LED_STPD LED STOP Duration Register

LED STOP Duration Register is 20-bit register.

LED_STPD=0x4000_6030

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved												LEDSTPD																			
-												0x00000																			
-												RW																			

19 0	LEDSTPD	LED STOP Duration Register (since LED Start) LED STOP Count mode or Smart share mode 1) In LED STOP Count mode, this register is used as LED STOP duration value. The counter will automatically start to count after COM display - When the counter value is matched with this value, LED can re-start. It mean that touch key scan operation should be stop(refer to Figure 24.5 of Mode Function) 2) In Smart Share mode, this register is used as LED STOP duration value. The counter will automatically start to count after COM display - Although the counter value is matched with this value LED can't re-start until pending touch key ends. (refer to Figure 24.6 of Mode Function) 3) This register value is applicable only in LED STOP Count Mode or Smart Share modes -.LED STOP Duration Width= fCLK/(LEDSTPD + 1) (fCLK is selected mux output clock) For example If fCLK = 24MHZ and LEDSTPD =3a8c0h, STOP duration is about 10ms (24MHZ/(239,808 +1))

23.3.14 LED_SR LED STATUS Register

LED STATUS Register is 4-bit register. This Register is able to 32/16/8-bit access.

LED_SR=0x4000_6034

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																												MATCHF	LED_INT	LED_INTE	LED_ENDF
-																												0	0	0	1
-																												RW	RW	RW	RW

3	MATCHF	Flag to occur when LEDSTPD reg match with counter	
		0	Not Matched
		1	Matched
2	LED_INT	LED Interrupt Flag(in LED_INTE=1)	
		0	LED Interrupt not Generated
		1	LED Interrupt Generated
1	LED_INTE	LED Interrupt Enable	
		0	Disable
		1	Enable
0	LED_ENDF	LED Operation End Flag	
		1	Under LED no Operation
		0	Under LED Operation

-.MATCHF flag is clear as “0” after matched not only by write “0” but also by LED operation end

-.LED_INT isn’t clear as “0” after interrupt generated as long as does’nt write “0”

-.Under Following Condition, LED_ENDF bit is set as “1”
1)after reset release
2)when write “1” LED_ENDF
3)when LED operation end since LED start
4)write “0” LEDEN(bit1 of LEDCON1) or LEDST(bit0 of LEDCON1)

-.Under Following Condition, LED_ENDF bit is set as “0”
1)when write “0” LED_ENDF
2)when LED is operating since LED start

23.3.15 LED_CON2 LED Control Register2

LED Control Register2 is 6-bit register. This Register is able to 32/16/8-bit access.

LED_CON2=0x4000_6038

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																										COM_SEGN1	COM_SEGN0	OVERLAP	OVERTS2	OVERTS1	OVERTS0
-																										0	0	0	0	0	1
-																										RW	RW	RW	RW	RW	RW

5	COM_SEGN	COM & SEG Share Pin Select	
4		00	SEG0:SEG1
		01	SEG0:COM26
		10	COM25:SEG1
		11	COM25:COM26
3	OVERLAP	OVERLAP TIME Select	
		0	Select (OVERLAP Time = fCLK/8 ~ fCLK/1024)
		1	Non-Select (OVERLAP Time = fCLK/2)
2	OVERTS	OVERLAP TIME Select	
1		000	fCLK/1024
0		001	fCLK/512
		010	fCLK/256
		011	fCLK/128
		100	fCLK/64
		101	fCLK/32
		110	fCLK/16
		111	fCLK/8
Overlap time is recommended to be within range of 5us~60us.			

23.3.16 LED_CON1 LED Control Register1

LED Control Register1 is 4-bit register. This Register is able to 32/16/8-bit access.

LED_CON1=0x4000_603C

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																												MD1	MD0	LEDEN	LEDST
-																												0	0	0	0
-																												RW	RW	RW	RW

3	MD[1:0]	Mode Select	
2		00	LED Alone Mode
		01	Hand Shake(with touch) Mode
		10	LED Stop Count Mode(since LED Start)
		11	Smart Share(with touch) Mode
1	LEDEN	LED Enable	
		0	LED Disable
		1	LED Enable
0	LEDST	LED START, STOP Operation	
		0	Stop LED Operation
		1	Start LED Operation

-.LED Operation is possible only after LEDEN(bit1 of LEDCON1 reg) is set “1”

-.Under Following Condition, LEDST bit is set as “1”

1)when write “1” LEDST

2)when TOUCH_END from touch is generated in hand shake mode or smart share mode

3)when LEDSTPD reg is matched with counter in LED Stop count Mode or smart share mode

-.Under Following Condition, LEDST bit is clear as “0”

1)when write “0” LEDEN

2)when write “0” LEDST

3)when LED operation is terminated

-.MD is changed to “00” only when write “0” LEDEN.
Otherswise MD is holding previous written value.

23.4 Functional Description

23.4.1 LED Display RAM Organization

Display data are stored to the display data area in the external data memory.

The display data which stored to the display external data area (address 0x4000_6044-0x4000_60AC) are read automatically and sent to the LED driver by the hardware. The LED driver generates the segment signals and com signals in accordance with the display data and drive method. Therefore, display patterns can be changed by only overwriting the contents of the display external data area with a program.

Figure 20.4 shows the correspondence between the display external data area and the ICOM/ISEG pins. The LED is turned on lights when the display data is “1” and turned off when “0”. Bit 31~11 is not implemented.

Table 23.2 LED Display RAM

Name	Address	Bit						
		31	---	10	---	2	1	0
DISPRAM0	0x4000_6044	---	---	SEG10	---	SEG2	SEG1	SEG0
DISPRAM1	0x4000_6048	---	---	SEG10	---	SEG2	SEG1	SEG0
DISPRAM2	0x4000_604C	---	---	SEG10	---	SEG2	SEG1	SEG0
DISPRAM3	0x4000_6050	---	---	SEG10	---	SEG2	SEG1	SEG0
DISPRAM4	0x4000_6054	---	---	SEG10	---	SEG2	SEG1	SEG0
DISPRAM5	0x4000_6058	---	---	SEG10	---	SEG2	SEG1	SEG0
DISPRAM6	0x4000_605C	---	---	SEG10	---	SEG2	SEG1	SEG0
DISPRAM7	0x4000_6060	---	---	SEG10	---	SEG2	SEG1	SEG0
DISPRAM8	0x4000_6064	---	---	SEG10	---	SEG2	SEG1	SEG0
DISPRAM9	0x4000_6068	---	---	SEG10	---	SEG2	SEG1	SEG0
DISPRAM10	0x4000_606C	---	---	SEG10	---	SEG2	SEG1	SEG0
DISPRAM11	0x4000_6070	---	---	SEG10	---	SEG2	SEG1	SEG0
DISPRAM12	0x4000_6074	---	---	SEG10	---	SEG2	SEG1	SEG0
DISPRAM13	0x4000_6078	---	---	SEG10	---	SEG2	SEG1	SEG0
DISPRAM14	0x4000_607C	---	---	SEG10	---	SEG2	SEG1	SEG0
DISPRAM15	0x4000_6080	---	---	SEG10	---	SEG2	SEG1	SEG0
DISPRAM16	0x4000_6084	---	---	SEG10	---	SEG2	SEG1	SEG0
DISPRAM17	0x4000_6088	---	---	SEG10	---	SEG2	SEG1	SEG0
DISPRAM18	0x4000_608C	---	---	SEG10	---	SEG2	SEG1	SEG0
DISPRAM19	0x4000_6090	---	---	SEG10	---	SEG2	SEG1	SEG0
DISPRAM20	0x4000_6094	---	---	SEG10	---	SEG2	SEG1	SEG0
DISPRAM21	0x4000_6098	---	---	SEG10	---	SEG2	SEG1	SEG0
DISPRAM22	0x4000_609C	---	---	SEG10	---	SEG2	SEG1	SEG0
DISPRAM23	0x4000_60A0	---	---	SEG10	---	SEG2	SEG1	SEG0
DISPRAM24	0x4000_60A4	---	---	SEG10	---	SEG2	SEG1	SEG0
DISPRAM25	0x4000_60A8	---	---	SEG10	---	SEG2	SEG1	SEG0
DISPRAM26	0x4000_60AC	---	---	SEG10	---	SEG2	SEG1	SEG0

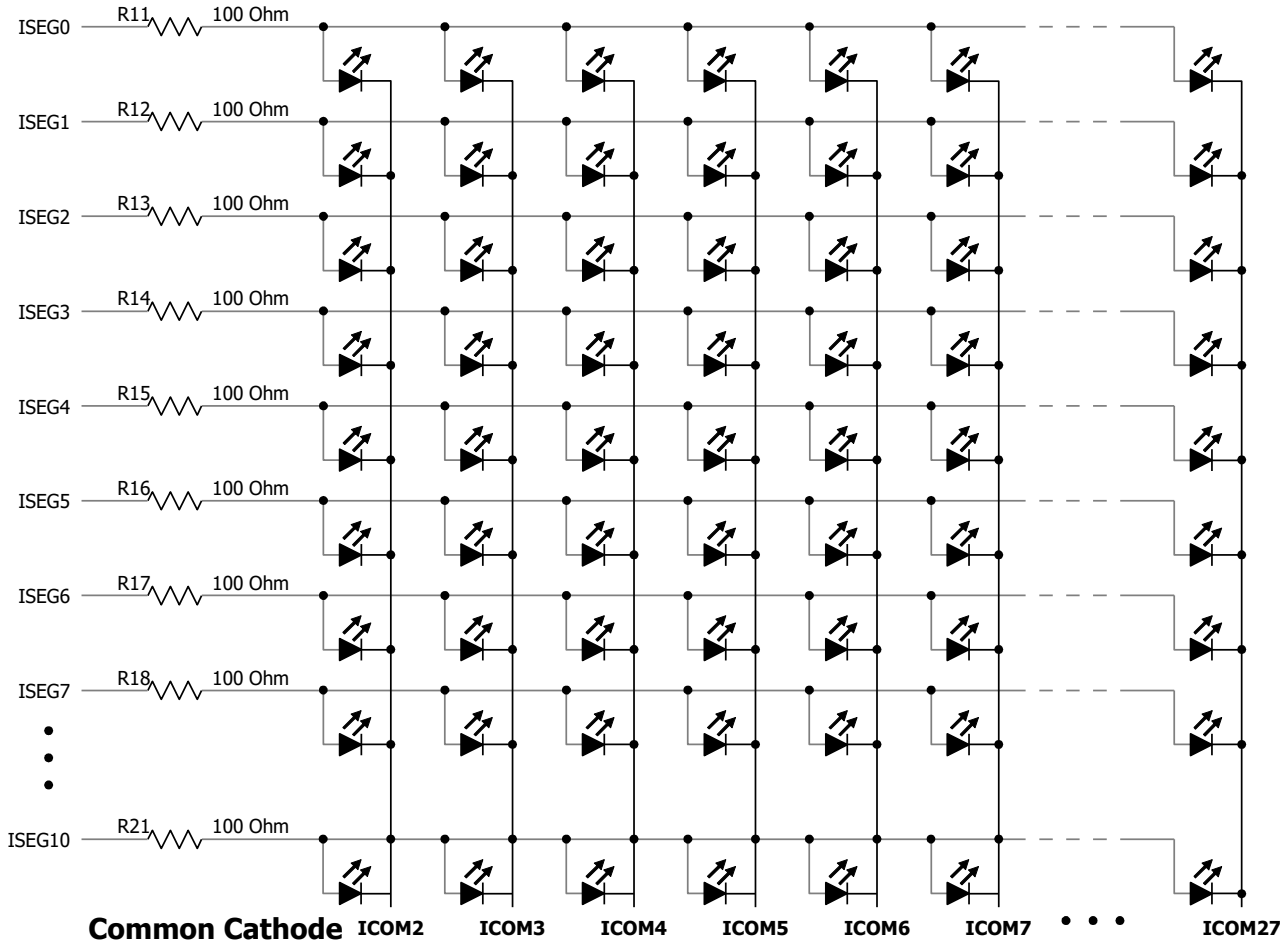


Figure 23.2. LED Shematics example

23.4.2 MODE Function

By depending on how set MD values(bit3, 2 of LED CONTROL REGISTER1), there are fourth modes.
First mode is LED alone mode irrelevant to touch function that can re-start by write “1” LEDST by program.
Below all mode is possible only after LEDEN(bit1 of LED_CON1)is set “1”.
Figure 24.3 show the LED alone mode in case of LED_COMER reg = 000_0000_0000_0000_0000_0100_0001
(k) shows the overlaptime that exists between the COM and the COM that are controllable by the program.
The larger the value of the COMDIMM, the smaller the COM width in the direction of arrow like in (j).
An interrupt occurs at point (A) where the LED operation terminated when LED_INTE is set.
When enabling the LED by rewrite LEDST “1” as in (B), LED can starts again.

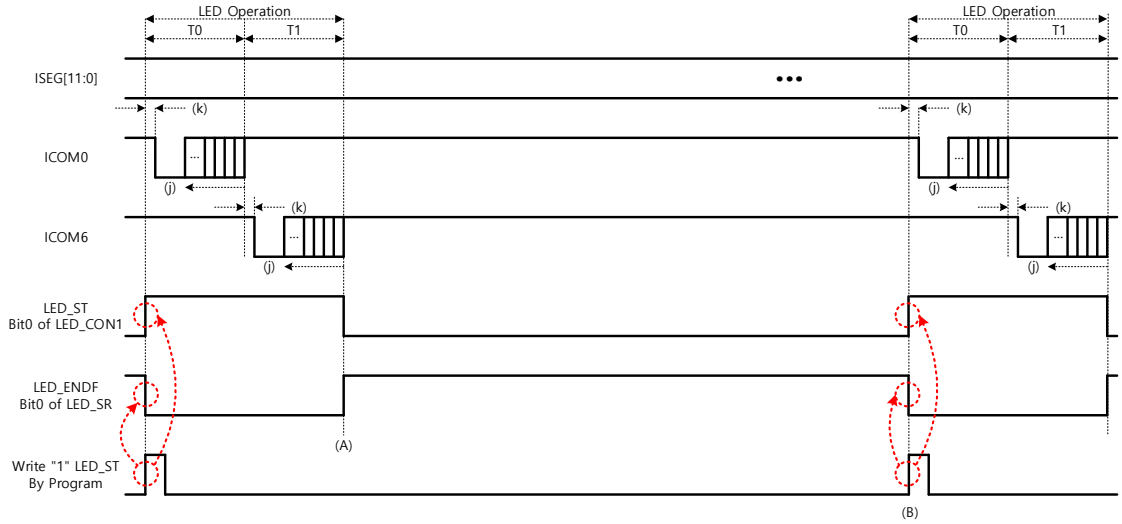


Figure 23.3. LED alone Mode

The second mode is hand shake mode to inform the touch when the LED is finished and to make LED start again by the TOUCH_END signal from the touch.
Figure 24.4 show the hand shake mode in the case of COMER reg = 000_0000_0000_0000_0000_0000_0001.
Frame cycle is defined by sum of LED operation (1) and touch key scan (2). It is the minimum cycle without flicker
An interrupt occurs at point (A) where the LED operation terminated when LED_INTE is set.
Touch continues to send the “1” until LED_ENDF changes to “0” in (B), and then LED start again.

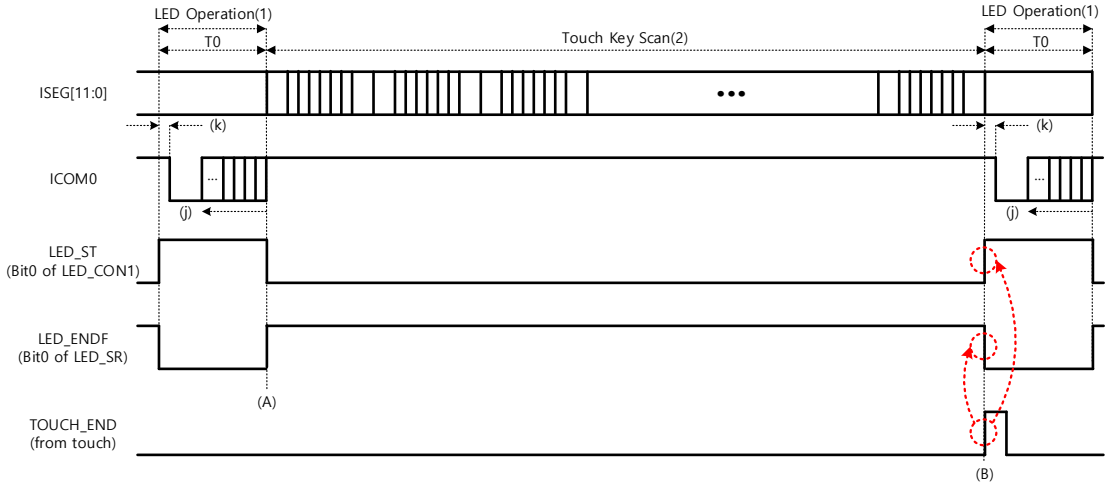


Figure 23.4. Hand Shake Mode

The third mode is LED stop count mode that the beginning of the next LED operation is determined by LED stop duration register value after the previous LED operation end.

It is need when deciding the period of frame that LED can operate without flicker

Figure 24.5 show LED STOP Count mode in case of LED_COMER reg = 000_0000_0000_0000_0100_0000_0000.

An interrupt occurs at point (A) here the LED operation terminated when LED_INTE is set.

At the same time, 20-bit counter starts to increase by the internal enable bit

If 20-bit LEDSTPD register is matched with the counter, MATCHF(bit3 of LED_SR) is set “1”,

LED_ENDF is cleared “0”, 20-bit counter is cleared “0” and LED start again as in (B)

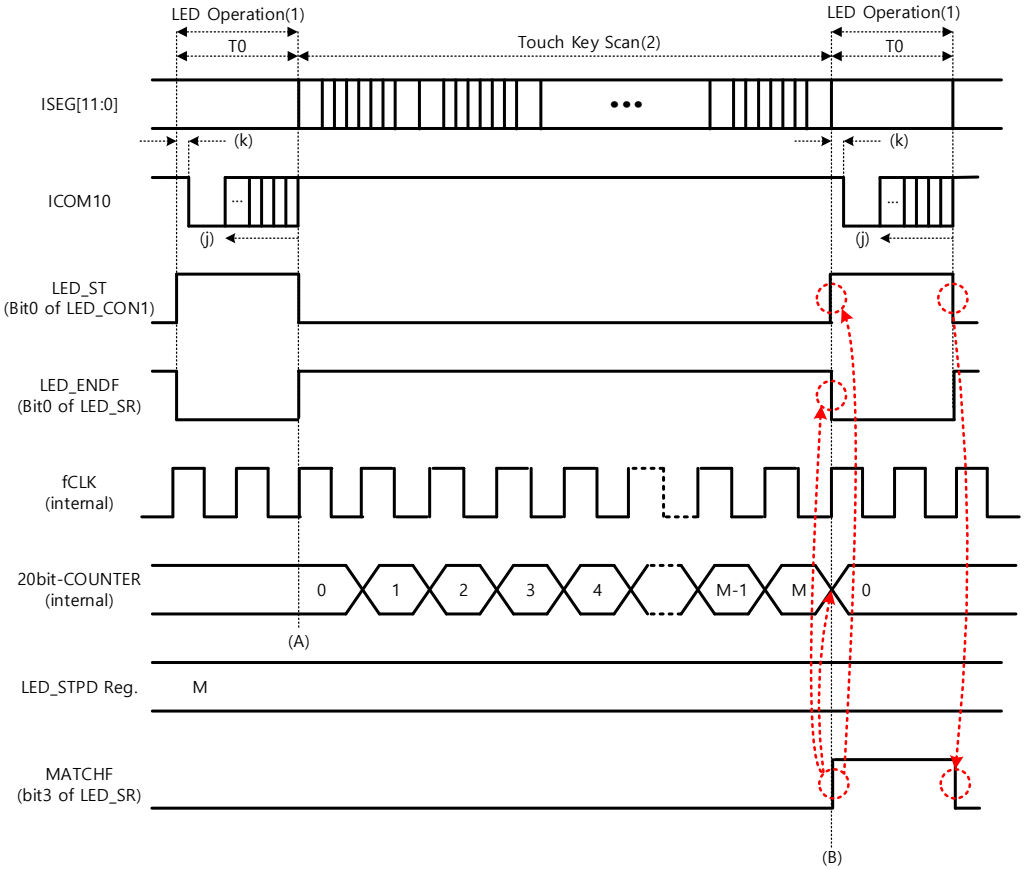


Figure 23.5. LED STOP Count Mode

The fourth mode is smart share mode that the beginning of the next LED operation can't do until current pending touch key scan ends although MATCHF(bit3 of LED_SR) generate after the previous LED operation end.

It is need when as many as touch key scan want to be executed during touch key scan time.

Figure 24.6 show smart share mode in case of LED_COMER reg = 000_0000_0000_0000_0100_0000_0000.

An interrupt occurs at point (A) here the LED operation terminated when LED_INTE is set.

At the same time, 20-bit counter starts to increase by the internal enable bit although 20-bit LED_STPD register is matched with the counter and then MATCHF(bit3 of LED_SR) is set "1", LED_ENDF can't clear "0" and LED can't start again until the TOUCH_END signal from the touch is active.

If any more LED display is not needed, it is highly recommended LEDEN(bit1 of LED_CON1) setting as "0" to be executed between the end of LED operation (A) and LED restart (B) to prevent flicker.

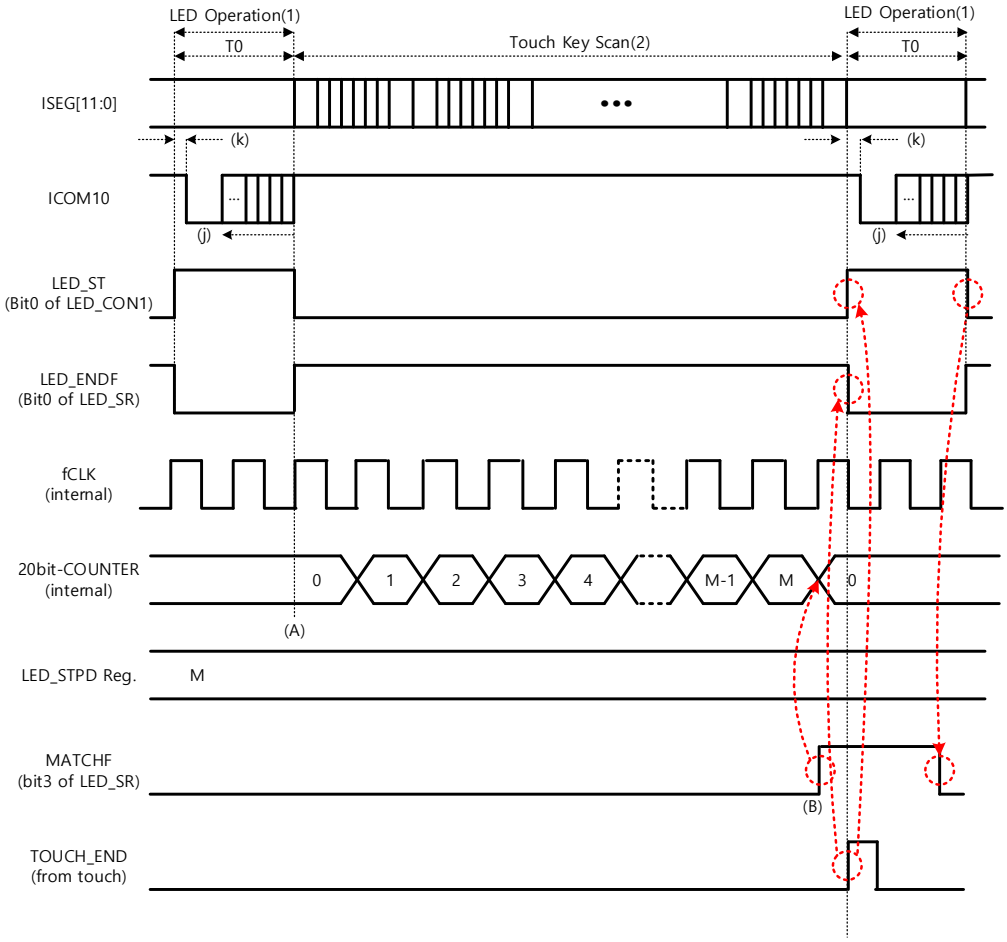


Figure 23.6. Smart Share Mode

CHAPTER 24. CYCLIC REDUNDANCY CHECK AND CHECKSUM

24.1 OVERVIEW

The CRC (cyclic redundancy check) generator is used to get a 16-bit CRC code from Flash ROM and a generator polynomial.

Among other applications, CRC-based techniques are used to verify data transmission or storage integrity. In the scope of the functional safety standards, they offer a means of verifying the Flash memory integrity. The CRC generator helps compute a signature of the software during runtime, to be compared with a reference signature.

The CRC generator has following features:

- Auto CRC and User CRC Mode.
- Polynomial : CRC-CCITT ($G_1(x) = x^{16} + x^{12} + x^5 + 1$), CRC-16 ($G_2(x) = x^{16} + x^{15} + x^2 + 1$)
- CRC Mode and Checksum Mode.

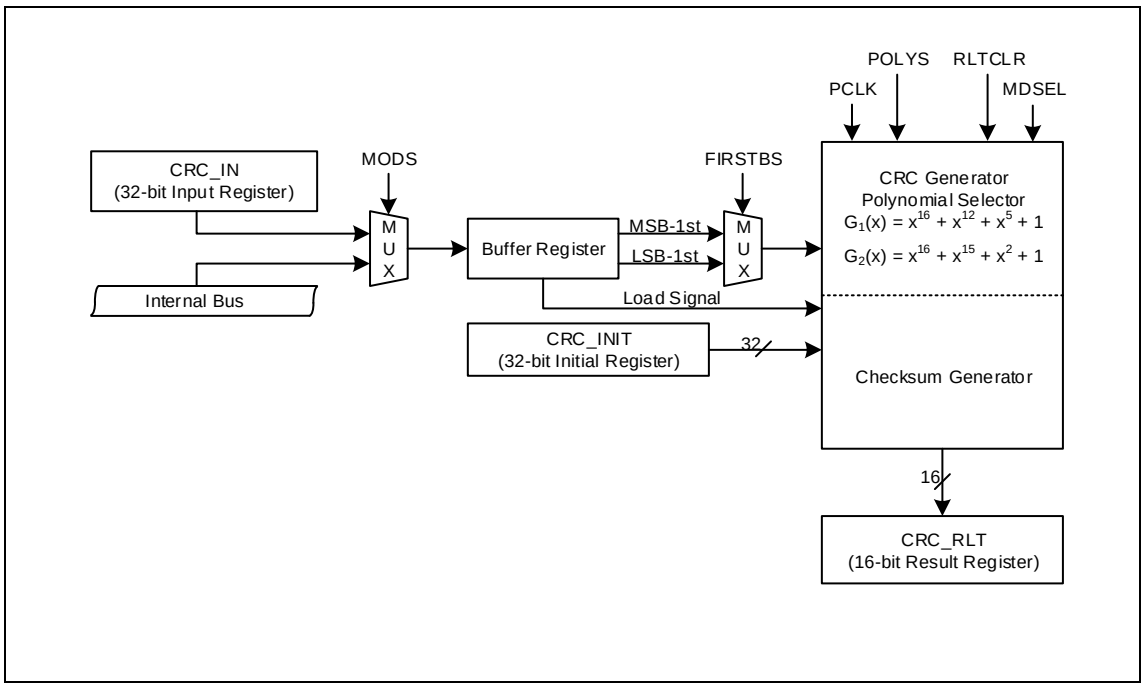


Figure 24.1 Block Diagram

24.2 REGISTERS

The base address of CRC and Checksum block is as below.

Table 25.1 CRC base address

NAME	BASE ADDRESS
CRC	0x4000_0300

Table 24.2 CRC Register map

Register Name	Offset	Access Type	Description	Initial Value	Ref
CRC_CR	0x00	RW	CRC/Checksum Control Register	0x0000_0000	25.2.1
CRC_IN	0x04	RW	CRC/Checksum Input Data Register	0x0000_0000	25.2.2
CRC_RLT	0x08	RO	CRC/Checksum Result Data Register	0x0000_FFFF	25.2.3
CRC_INIT	0x0C	RW	CRC/Checksum Initial Data Register	0x0000_0000	25.2.4

24.2.1 CRC_CR CRC Control Register

CRC/Checksum Control Register Register is 32-bit register. This Register is able to 32/16/8-bit access.

CRC_CR=0x4000_0300

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																						CRCINTEN	CRCINTF	MODS	RLTCLR	MDSEL	POLYS	Reserved		FIRSTBS	CRCRUN
-																						0	0	0	0	0	0	-		0	0
-																						RW	RW	RW	RW	RW	RW	-		RW	RW

9	CRCINTEN	CRC interrupt enable bit
		0 Disable
		1 Enable
8	CRCINTF	CRC interrupt flag bit
		0 No request occurred
		1 Request occurred, This bit is cleared to '0' when write '1'.
7	MODS	User/Auto Mode Selection bit.
		0 User mode. (Calculation every writing data to the CRCIN register)
		1 Auto mode. (Calculation till CRCSADR == CRCEADR)
6	RLTCLR	CRC/Checksum Result Data Register (CRCRLT) Initialization bit.
		0 No effect.
		1 Initialize the CRCRLT register with the value of CRCINIT (This bit is automatically cleared to "0b" after operation)
5	MDSEL	CRC/Checksum Selection bit.
		0 Select CRC.
		1 Select checksum.
4	POLYS	Polynomial Selection bit. (CRC only)
		0 Select CRC-CCITT ($G_1(x) = x^{16} + x^{12} + x^5 + 1$)
		1 Select CRC-16 ($G_2(x) = x^{16} + x^{15} + x^2 + 1$)
1	FIRSTBS	First Shifted-in Selection bit. (CRC only)
		0 MSB-1st.
		1 LSB-1st.
0	CRCRUN	CRC/Checksum Start Control and Busy bit.
		0 Not busy. The CRC operation can be finished by writing "0b" to this bit on running.
		1 Start CRC operation. This bit is automatically cleared to "0b" when the value of CRCSADR register reaches the value of CRCEADR register.
		Note) 1. The 4 "NOP instruction" should be executed immediately after this bit is set to "1b".

Notes)

1. The CRCRLT register and the CRC/Checksum block should be initialized by writing "1b" to the RLTCLR bit before a new CRC/Checksum calculation.
2. The CRCRUN bit should be set to "1b" last time after setting appropriate values to the registers.
3. On the user mode, it will be calculated every writing data to the CRCIN register during CRCRUN=1.
4. It is prohibited writing any data to the CRCIN register during CRCRUN=0.
5. The checksum is calculated by byte unit. Ex) On 0x34A7E991, CRCRLT = 0x34 + 0xA7 + 0xE9 + 0x91.
6. The 4 "NOP Instruction" should follow immediately after CRCRUN bit is set to "1b".

24.2.2 CRC_IN CRC Input Data Register

CRC Input Data Register is 32-bit register.

CRC_IN=0x4000_0304

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INDATA																															
0x00000000																															
RW																															

31 0	INDATA	CRC Input Data bits.

Note)

1. The CRCIN register should be written by 1-word (32-bits).

24.2.3 CRC_RLT CRC Result Data Register

CRC Result Data Register is 32-bit register. This Register is able to 32/16/8-bit access.

CRC_RLT=0x4000_0308

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																RLTDATA															
-																0xFFFF															
-																RW															

15 0	RLTDATA	CRC Result Data bits.

24.2.4 CRC_INIT CRC Initial Data Register

CRC Initial Data Register is 32-bit register. This Register is able to 32/16/8-bit access.

CRC_INIT=0x4000_030C

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																INIDATA															
-																0x0000															
-																RW															

15 0	INIDATA	CRC Initial Data bits.

24.3 Functional Description

24.3.1 CRC polynomial structure

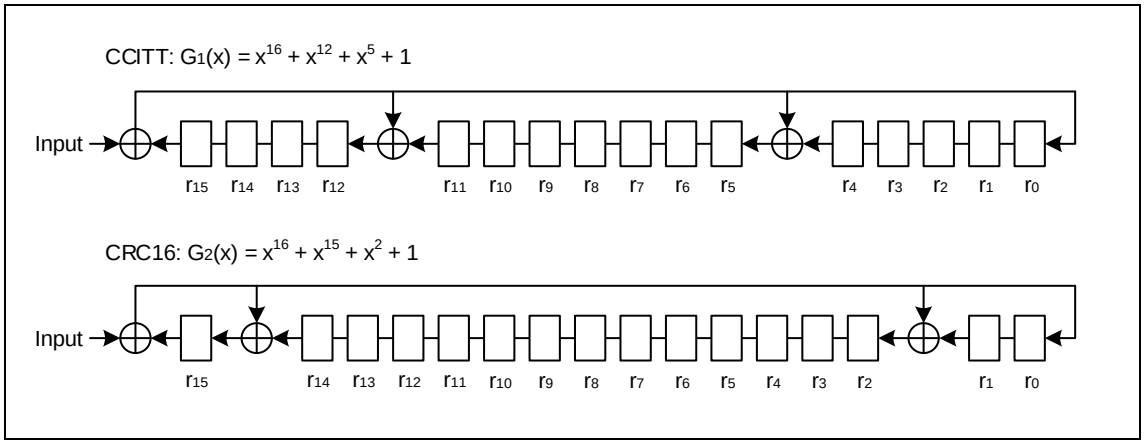


Figure 24.2 CRC polynomial structure

24.3.2 The CRC operation procedure in User CRC/Checksum mode

1. CRC/Checksum Enable and Clock Enable
2. Set CRC initial data register. (CRCINIT)
3. Select User CRC/Checksum Mode and CRC
4. CRC operation starts. (CRCRUN = 1)
5. Input CRC Data at CRCIN.
6. CRC Stop and read CRC result.

CHAPTER 25. Electrical Characteristics

25.1 DC Characteristics

25.1.1 ABSOLUTE MAXIMUM RATINGS

Absolute maximum ratings are limiting values of operating and environmental conditions which should not be exceeded under the worst possible conditions.

Table 25.1 Absolute maximum rating

Parameter	Symbol	Ratings	Unit	Note
Supply Voltage	VDD	-0.3 – +6.5	V	–
Normal Pin	V_I	-0.3 – VDD+0.3	V	Voltage on any pin with respect to VSS
	V_O	-0.3 – VDD+0.3	V	
	I_{OH}	5	mA	Maximum current output sourced by (I_{OH} per I/O pin)
	ΣI_{OH}	40	mA	Maximum current (ΣI_{OH})
	I_{OL}	10	mA	Maximum current sunk by (I_{OL} per I/O pin)
	ΣI_{OL}	80	mA	Maximum current (ΣI_{OL})
Total Power Dissipation	T_P	300	mW	–
Storage Temperature	T_{STG}	-45 – +125	°C	–

25.1.2 RECOMMENDED OPERATING CONDITIONS

Table 25.2 Recommended Operating Condition

Parameter	Symbol	Condition	Min	Typ.	Max	Unit
Supply Voltage	VDD	-	1.8	-	5.5	V
		Touch	2.7	-	5.5	V
		LED	3.3	-	5.5	V
Operating Frequency	FREQ	MOSC	4	-	16	MHz
		SOSC	-	32.768	-	kHz
		HSI	46.32	48	49.68	MHz
		LSI	400	500	600	kHz
Operating Temperature	Top	Top	-40	-	+85	℃

25.1.3 A/D CONVERTER CHARACTERISTICS

Table 25.3 ADC Electrical Characteristics (Temperature: -40 ~ +85℃)

Parameter	Symbol	Condition	Min	Typ.	Max	unit
Operating Voltage	AVDD		2.4	5	5.5	V
Resolution				12		Bit
Operating Current	IDDA	VDD=5.0V		1	2	mA
Analog Input Range	VAN		VSS		AVREF	V
Conversion Rate	fCON			-	150	kSPS
Operating Frequency	ACLK				4.5	MHz
Integral Non-Linearity	INL	AVDD=2.4V < AVDD < 5.5V, T_A = 25 °C		±4	±10	LSB
Differential Non-Linearity	DNL			±1	±4	LSB
Top Offset Error(FSE)	TOE			±6	±12	LSB
Zero Offset Error	ZOE			±4	±8	LSB

25.1.4 POWER ON RESET CHARACTERISTICS

Table 25.4 POR Electrical Characteristics (Temperature: -40 ~ +85℃)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Operating Current	I_{DD}	–	-	60	-	uA
POR Set Level	V_{set}	–	1.05	1.2	1.35	V
POR Reset Level	V_{reset}	–	1.0	1.1	1.2	V

25.1.5 LOW VOLTAGE RESET CHARACTERISTICS

Table 25.5 Low Voltage Reset Characteristics (Temperature: -40 ~ +85℃)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Detection Level	V_{LVR}	T_A = – 40 °C to + 85 °C, Falling Voltage (error rate 5%)		1.60		V
				1.69		
				1.78		
				1.90		
				1.99		
				2.12		
				2.30		
				2.47		
				2.67		
				3.04		
				3.18		
				3.59		
				3.72		
				4.03		
				4.20		
				4.48		
Hysteresis	-		-	100	200	mV
Noise cancelling time	-		-	2	-	us
Operation Current	I_{DD}		-	3.5	5	uA
Operation Current(STOP)	$I_{DD, STOP}$		-	2.5	3	nA

25.1.6 LOW VOLTAG INDICATOR CHARATERISTICS

Table 25.6 Low Voltage Indicator Characteristics (Temperature: -40 ~ +85℃)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Detection Level	V_{LVI}	T_A = – 20 °C to + 85 °C, Falling Voltage (error rate 5%)		1.60		V
				1.69		
				1.78		
				1.90		
				1.99		
				2.12		
				2.30		
				2.47		
				2.67		
				3.04		
				3.18		
				3.59		
				3.72		
				4.03		
				4.20		
				4.48		
Hysteresis	-		-	100	200	mV
Noise cancelling time	-		-	2	-	Us
Operation Current	I_{DD}		-	3.5	5	uA
Operation Current(STOP)	$I_{DD, STOP}$		-	2.5	3	nA

25.1.7 HIGH FREQUENCY INTERNAL RC OSCILLATOR CHARACTERISTICS

Table 25.7 High Frequency Internal RC Oscillator Characteristics (Temperature: -40 ~ +85℃)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Frequency	f_{HSI}	VDD = 1.8V to 5.5V	–	48	–	MHz
Tolerance		T_A = – 40 °C to + 85 °C	–	–	±3.5	%
Clock Duty Ratio	T_{OD}	–	–	50	–	%
Stabilization Time	t_{HFS}	–	–	–	100	us
IRC Current	I_{HSI}	Enable	–	190	–	uA
		Disable	–	1	–	uA

25.1.8 LOW FREQUENCY INTERNAL RC OSCILLATOR CHARACTERISTICS

Table 25.8 Low Frequency Internal RC Oscillator Characteristics (Temperature: -40 ~ +85℃)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Frequency	f_{LIRC}	VDD = 1.8V to 5.5V	400	500	600	kHz
IRC Current	I_{LIRC}	Enable	–	1.5	2	uA
		Disable	–	1	20	nA

25.1.9 LCD VOLTAGE CHARACTERISTICS

Table 25.9 LCD Voltage Characteristics (Temperature: -40 ~ +85℃)

Parameter	Symbol	Conditions		Min	Typ	Max	Units
LCD Voltage	VLC0	LCD contrast disabled, 1/4 bias					V
		LCD contrast enabled, 1/4 bias, No Panel load	VLCD[3:0]=00H	Typx0.94	VDDx16/31	Typx1.06	V
			VLCD[3:0]=01H		VDDx16/30		
			VLCD[3:0]=02H		VDDx16/29		
			VLCD[3:0]=03H		VDDx16/28		
			VLCD[3:0]=04H		VDDx16/27		
			VLCD[3:0]=05H		VDDx16/26		
			VLCD[3:0]=06H		VDDx16/25		
			VLCD[3:0]=07H		VDDx16/24		
			VLCD[3:0]=08H		VDDx16/23		
			VLCD[3:0]=09H		VDDx16/22		
			VLCD[3:0]=0AH		VDDx16/21		
			VLCD[3:0]=0BH		VDDx16/20		
			VLCD[3:0]=0CH		VDDx16/19		
			VLCD[3:0]=0DH		VDDx16/18		
			VLCD[3:0]=0EH		VDDx16/17		
			VLCD[3:0]=0FH		VDDx16/16		
LCD Mid Bias Voltage(note)	VLC1	VDD = 2.7V to 5.5V, LCD clock = 0Hz, 1/4 bias, No panel load		Typ-0.2	3/4xVLC0	Typ+0.2	V
	VLC2			Typ-0.2	2/4xVLC0	Typ+0.2	
	VLC3			Typ-0.2	1/4xVLC0	Typ+0.2	
LCD Driver Output Impedance	R_{LO}	VLCD=3V		–	5	10	kΩ
LCD Bias Dividing Resistor	RLCD1	1/4 bias, T_A = 25˚C		7.5	10	12.5	kΩ
	RLCD2			38	50	62	
	RLCD3			60	80	100	
	RLCD4			180	240	300	

Note)

1. It is middle output voltage when the VDD and the VLC0 node are connected.

25.1.10 TOUCH SWITCH CHARACTERISTICS

Table 25.10 Touch Switch Characteristics (Temperature: -40 ~ +85℃)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Operating Voltage	V_{DD}	–	2.7	-	5.5	V
	V_{DDA}	–	2.7	-	5.5	V
VDC Voltage	V_{CCL}	From MCU	–	1.9	–	V
SNR(Signal-toNoise Ratio)	SNR	–	–	20	–	dB
Self-Calibration Time	T_{CAL}	–	–	10	–	ms
Scan Speed	T_{SCAN}	–	–	10	–	ms
Supply Current	I_{DD}	–	–	1	–	mA
Operation Temperature	T_{OPER}	–	-40	–	+85	℃

25.1.11 LED DRIVER CHARACTERISTICS

Table 25.11 LED Driver Characteristics

Parameter	Symbol	Conditions		Min	Typ	Max	Units
Operating Voltage	V_{Ddext}			3.3	–	5.5	V
Operating Temperature	T_A			-40	25	85	℃
COM output leakage	I_{CLKG}			-1		1	uA
SEG output leakage	I_{SLKG}			-1		1	uA
SEG Current Matching (I_{SEG}-I_{SEGAVR}) / I_{SEGAVR}	ITOSEG			-6	+/-1.5	6	%
SEG Current	I_{SEG}	@ RSET value (4.7kΩ)	V_{DDEXT} = 3.3V V_{OH_LED} = 3.05V	2.1	–	–	mA
			V_{DDEXT} = 5 V V_{OH_LED} = 3.73V	3.3[NOTE1)]	–	–	
COM Current	I_{COM}	V_{OL_LED} = 0.3V		23.1	–	–	mA

NOTE

1) V_{ddext} 3.3V is a worst case and proved by experiment. However, in case of V_{ddext} 5V condition, it is the value measured in simulation.

2) At minimum current conditions, The difference voltage between SEG and COM is 2.7V at least .

25.1.12 DC ELECTRICAL CHARACTERISTICS

Table 25.12 DC Electrical Characteristics (Temperature: -40 ~ +85℃)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Input High Voltage	V_{IH1}	All input pins, nRESET	0.8VDD	-	VDD	V
	V_{IH2}	PF5,PF6,PF7 are input 1.8V level	0.9	-	VDD	
Input Low Voltage	V_{IL1}	All input pins, nRESET	0	-	0.2VDD	V
	V_{IL2}	PF5,PF6,PF7 are input 1.8V level	0	-	0.6	
Output High Voltage	V_{OH1}	VDD=5V, I_{OH1} = – 2.36mA PA0, PA1, PA2, PA3, PA4, PA5, PF0	0.8VDD	-	VDD	V
	V_{OH2}	VDD=5V, I_{OH2} = – 4.38mA PA6, PA7	0.8VDD	-	VDD	
	V_{OH3}	VDD=5V, I_{OH3} = – 4.38mA PB0, PB1	0.8VDD	-	VDD	
	V_{OH4}	VDD=5V, I_{OH4} = – 4.1mA PB2, PB3, PB4, PB5, PB6, PB7, PC0, PC1, PC2, PC3, PC4, PD0, PD1, PD2, PD3, PD4, PD5	0.8VDD	-	VDD	
	V_{OH5}	VDD=5V, I_{OH5} = – 10.9mA PE0, PE1, PE2, PE3, PE4, PE5, PE6, PE7	0.8VDD	-	VDD	
	V_{OH6}	VDD=5V, I_{OH6} = – 2.93mA PA9, PA10, PA11, PF1, PF2, PF3, PF4, PF8, PF9, PF10, PF11, PE8, PE9, PE10, PE11, PE12, PE13	0.8VDD	-	VDD	
	V_{OH7}	VDD=5V, I_{OH7} = – 4.1mA PB8, PB9, PB10, PB11, PB12, PB13, PB14, PB15, PC5, PC6, PC7, PC8, PC9, PC10, PC11, PC12, PE15, PE14	0.8VDD	-	VDD	
Output Low Voltage	V_{OL1}	VDD=5V, I_{OL1} = 4.86mA PA0, PA1, PA2, PA3, PA4, PA5, PF0, PF5, PF6, PF7	0	-	0.2VDD	V
	V_{OL2}	VDD=5V, I_{OL2} = 19.1mA PA6, PA7	0	-	0.2VDD	
	V_{OL3}	VDD=5V, I_{OL3} = 19.1mA PB0, PB1	0	-	0.2VDD	
	V_{OL4}	VDD=5V, I_{OL4} = 19.1mA PB2, PB3, PB4, PB5, PB6, PB7, PC0, PC1, PC2, PC3, PC4, PD0, PD1, PD2, PD3, PD4, PD5	0	-	0.2VDD	
	V_{OL5}	VDD=5V, I_{OL5} = 19.1mA PE0, PE1, PE2, PE3, PE4, PE5, PE6, PE7	0	-	0.2VDD	
	V_{OL6}	VDD=5V, I_{OL6} = 4.86mA PA9, PA10, PA11, PF1, PF2, PF3, PF4, PF8, PF9, PF10, PF11, PE8, PE9, PE10, PE11, PE12, PE13	0	-	0.2VDD	

	V_{OL7}	VDD=5V, I_{OL7} = 19.1mA PB8, PB9, PB10, PB11, PB12, PB13, PB14, PB15, PC5, PC6, PC7, PC8, PC9, PC10, PC11, PC12, PE15, PE14	0	-	0.2VDD	
Input high leakage current	I_{IH}	All Input ports	-4	-	-	uA
Input low leakage current	I_{IL}	All Input ports	-	-	+4	uA
Pull-up resistor	R_{PU}	V_I=0V, T_A=25°C, All Input ports	10	-	60	kΩ
		V_I=0V, T_A=25°C, nRESET PIN		250		
Pull-down resistor	R_{PD}	V_I=VDD, T_A=25°C, All Input ports	40	-	70	kΩ
OSC feedback resistor	R_{X1}	XIN=VDD, XOUT=VSS, T_A=25°C, VDD=3.3V		1		MΩ

25.1.13 SUPPLY CURRENT CHARACTERISTICS

Table 25.13 Supply Current Characteristics (Temperature: -40 ~ +85℃)

Parameter	Symbol	Conditions		Typ	Max	Units
Supply Current	I_{DD1} (Run)	f_{XIN} = 8MHz	VDD=5V	4.0	12.0	mA
		f_{HSI} = 48MHz		10.0	30.0	
		f_{HSI} = 12MHz		3.5	10.0	
		f_{LSI} = 500kHz		200	600	uA
		f_{SOSC} = 32.768kHz		140	300	
	I_{DD2} (Sleep)	f_{XIN} = 8MHz		5	15	mA
		f_{HSI} = 48MHz		6	18	
		f_{HSI} = 12MHz		2	6	
		f_{LSI} = 500kHz		180	500	uA
		f_{SOSC} = 32.768kHz		130	400	
	I_{DD3} (Deep Sleep)	WDT(WDTRC) = ON, LVD = ON T_A = 25 °C		17	-	uA
	I_{DD4} (Deep Sleep)	WDT(WDTRC) = ON, LVD = OFF NOTE3 T_A = 25 °C		15	-	uA
	I_{DD4} (Deep Sleep)	WDT(WDTRC) = OFF, LVD = ON, T_A = 25 °C		4	-	uA
	I_{DD5} (Deep Sleep)	WDT(WDTRC) = OFF, LVD = OFF NOTE3, T_A = 25 °C		2	-	uA

Notes)

1. All supply current items don't include the current of an low frequency internal RC oscillator and a peripheral block.
2. All supply current items include the current of the power-on reset (POR) block.
3. LVD = OFF indicates that LVR reset function , LVR block and LVI block are disabled.
   SCU_RSER<LVDRST> = 0
   SCULV_LVRCR<LVREN> = 0x55
   SCULV_LVICR< LVIEN> = 0

25.1.14 USART SPI CHARCTERISTICS

Table 25.14 SPI Characteristics (Temperature: -40 ~ +85℃, VDD = 2.7 – 5.5V)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Output Clock Pulse Period	t_{SCK}	Internal SCK source	400	–	–	ns
Input Clock Pulse Period		External SCK source	400	–	–	
Output Clock High, Low Pulse Width	t_{SCKH}, t_{SCKL}	Internal SCK source	180	–	–	
Input Clock High, Low Pulse Width		External SCK source	180	–	–	
First Output Clock Delay Time	t_{FOD}	Internal/External SCK source	200	–	–	
Output Clock Delay Time	t_{DS}	–	–	–	100	
Input Setup Time	t_{DIS}	–	180	–	–	
Input Hold Time	t_{DIH}	–	180	–	–	

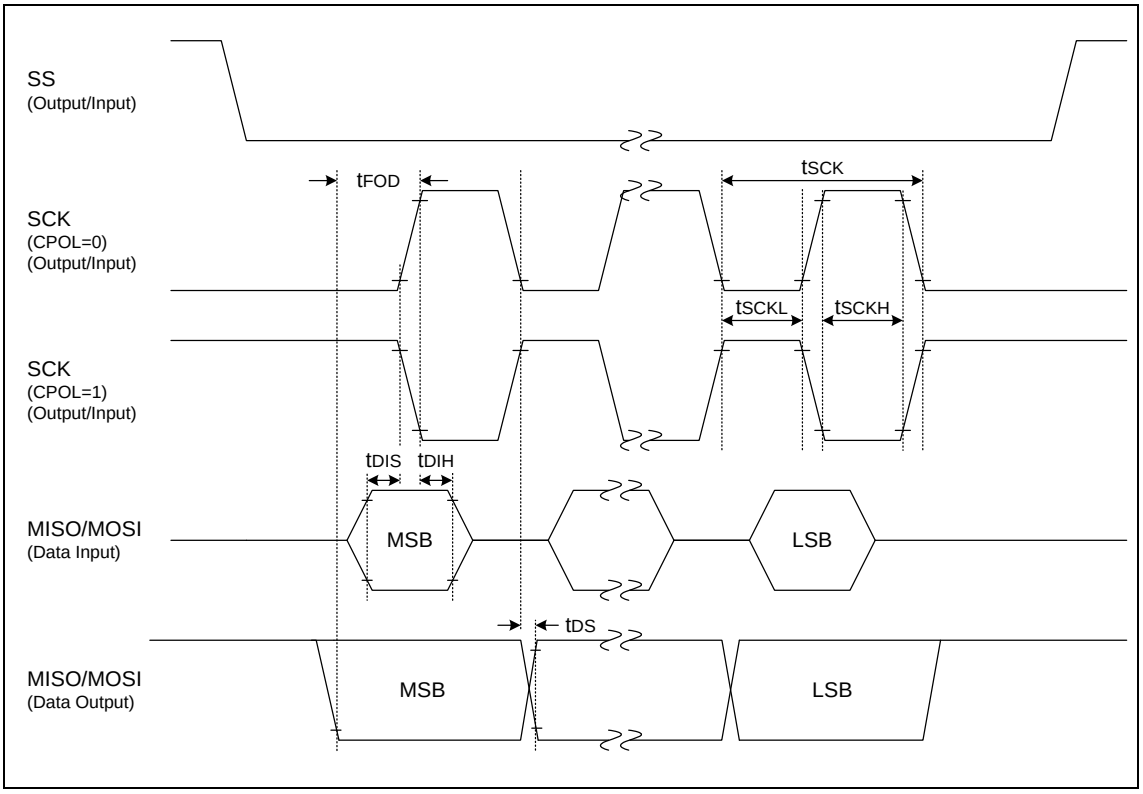


Figure 25.1 SPI Timing

25.1.15 I2C CHARACTERISTICS

Table 25.15 I2C Characteristics (Temperature: -40 ~ +85℃, VDD = 1.8 – 5.5V)

Parameter	Symbol	Min	Max	Units
Clock frequency	t_{SCL}	0	400	kHz
Clock High Pulse Width	t_{SCLH}	0.6	–	us
Clock Low Pulse Width	t_{SCLL}	1.3	–	
Bus Free Time	t_{BF}	1.3	–	
Start Condition Setup Time	t_{STSU}	0.6	–	
Start Condition Hold Time	t_{STHD}	0.6	–	
Stop Condition Setup Time	t_{SPSU}	0.6	–	
Stop Condition Hold Time	t_{SPHD}	0.6	–	
Output Valid from Clock	t_{VD}	0	–	
Data Input Hold Time	t_{DIH}	0	1.0	
Data Input Setup Time	t_{DIS}	100	–	ns

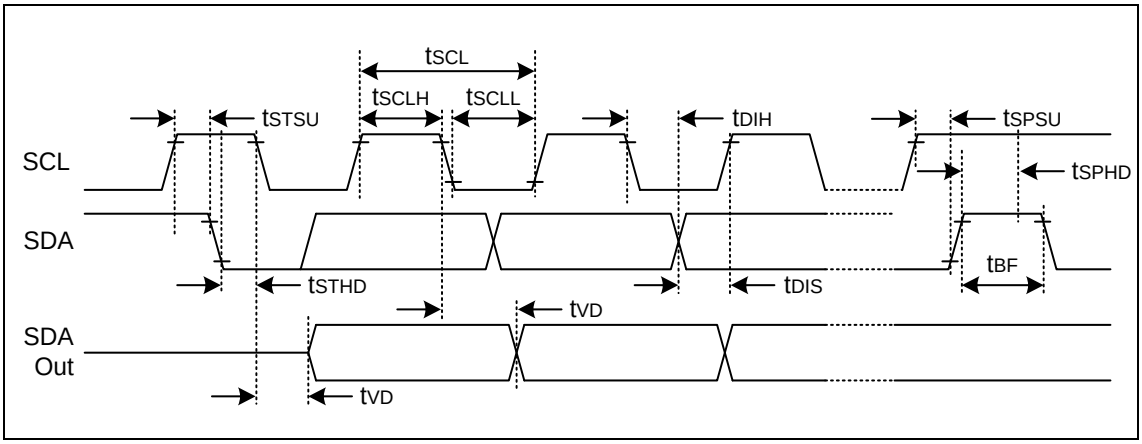


Figure 25.2 I2C Timing

25.1.16 USART UART TIMING CHARACTERISTICS

Table 25.16 UART Timing Characteristics (Temperature: -40 ~ +85℃, VDD = 1.8 – 5.5V)

Parameter	Symbol	Min	Typ	Max	Units
Serial port clock cycle time	t_{SCK}	1250	t_{CPU} x 16	1650	ns
Output data setup to clock rising edge	t_{S1}	590	t_{CPU} x 13	–	
Clock rising edge to input data valid	t_{S2}	–	–	590	
Output data hold after clock rising edge	t_{H1}	t_{CPU} – 50	t_{CPU}	–	
Input data hold after clock rising edge	t_{H2}	0	–	–	
Serial port clock High, Low level width	t_{HIGH}, t_{LOW}	470	t_{CPU} x 8	970	

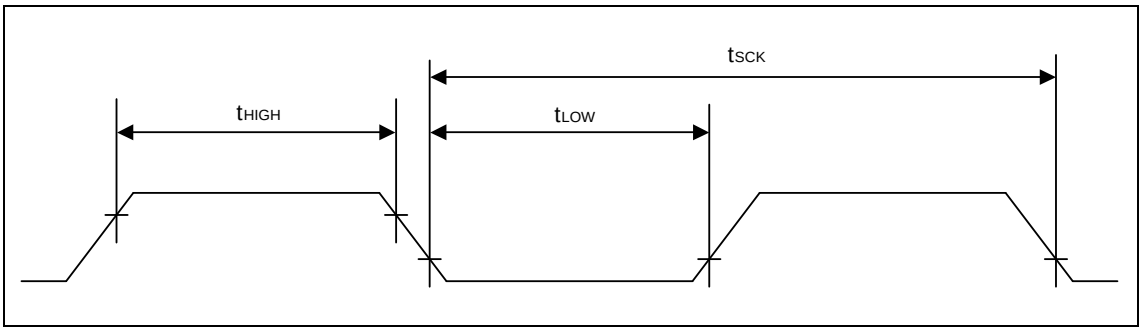


Figure 25.3 Waveform for UART Timing Characteristics

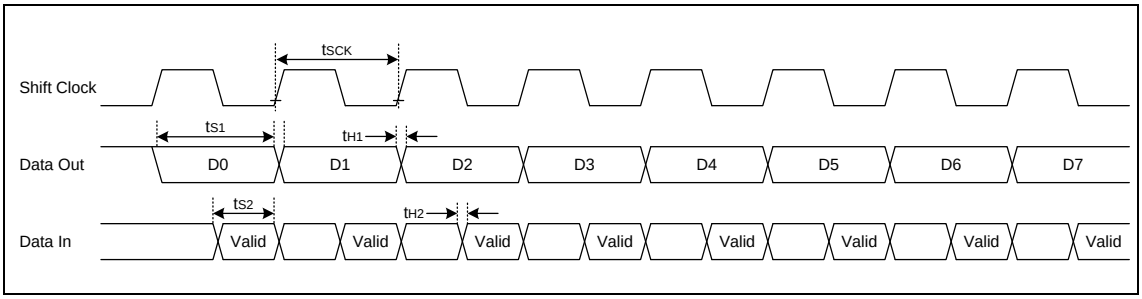


Figure 25.4 Timing Waveform for UART Module

25.1.17 INTERNAL FLASH ROM CHARACTERISTICS

Table 25.1 Internal Flash ROM Characteristics (Temperature: -40 ~ +85℃)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Reset Cycle Time	fRSTBUSY	–	5.6	8	10.4	us
Fuse Program Cycle Time	fFRDBUSY		4.2	6	7.8	
Normal Program Cycle Time	tPGMBUSY		21	30	42	
Normal Page Erase Cycle Time	tPERSBUSY		2.8	4	5.2	ms
Sector Erase Cycle Time	tSERSBUSY		2.8	4	5.2	
Chip Erase Cycle Time	tMERSBUSY	–	5.6	8	10.4	
Flash Program Voltage	V_{PGM}	On erase/write	2.7	–	3.6	V
Endurance of Write/Erase	N_{FWE}	T_A=25 °C, Page unit	10,000	–	–	Times
Retention Time	t_{FRT}		10	–	–	Years

25.1.18 MAIN OSCILLATOR CHARACTERISTICS

Table 25.17 Main Oscillator Characteristics (Temperature: -40 ~ +85℃)

Oscillator	Parameter	Conditions	Min	Typ	Max	Units
Crystal	Main oscillation frequency	1.8 V – 5.5 V	2.0	–	16.0	MHz
Ceramic Oscillator	Main oscillation frequency	1.8 V – 5.5 V	2.0	–	16.0	
External load capacitor	C1, C2	1MHz < fout ≤ 4MHz	18	30	35	pF
		4MHz < fout ≤ 12MHz	10	22	30	pF
		12MHz < fout ≤ 16MHz	7	18	22	pF

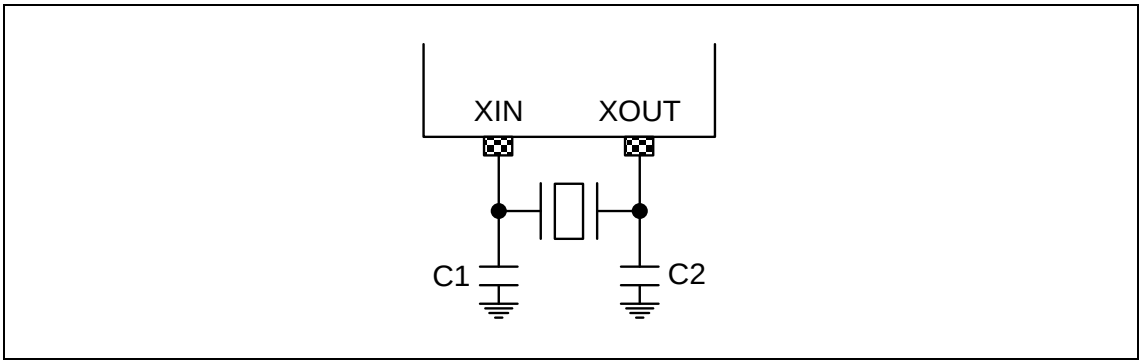


Figure 25.5 Crystal/Ceramic Oscillator

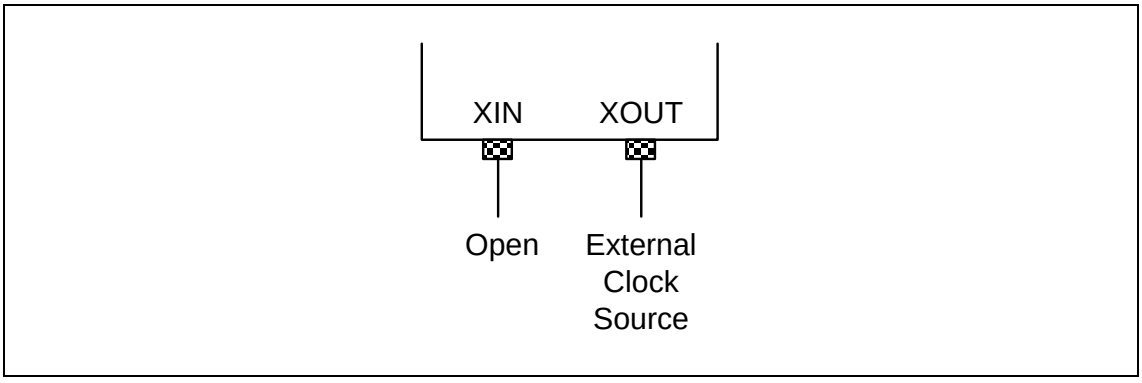


Figure 25.6 External Clock

25.1.19 SUB OSCILLATOR CHARACTERISTICS

Table 25.18 Sub Oscillator Characteristics (Temperature: -40 ~ +85℃)

Oscillator	Parameter	Conditions	Min	Typ	Max	Units
Crystal	Sub oscillation frequency	1.8 V – 5.5 V	32	32.768	38	kHz
External load capacitor	C1, C2	1.8 V – 5.5 V	5	15	35	pF

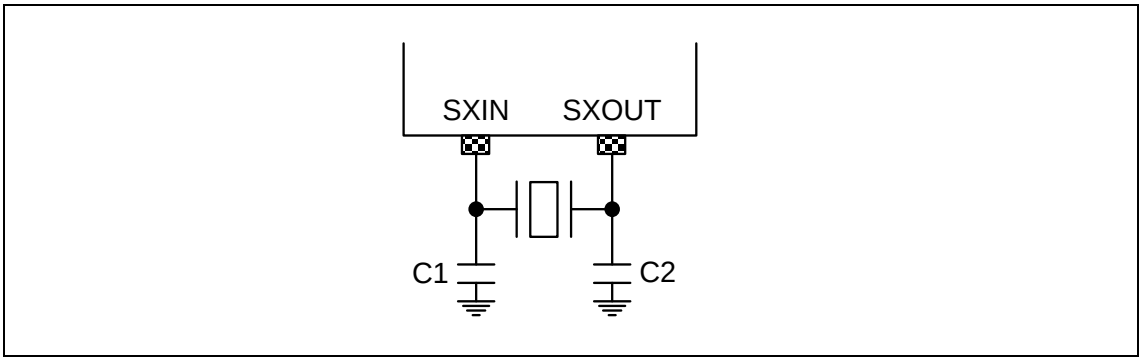


Figure 25.7 Crystal Oscillator

25.1.20 Operating Voltage Range

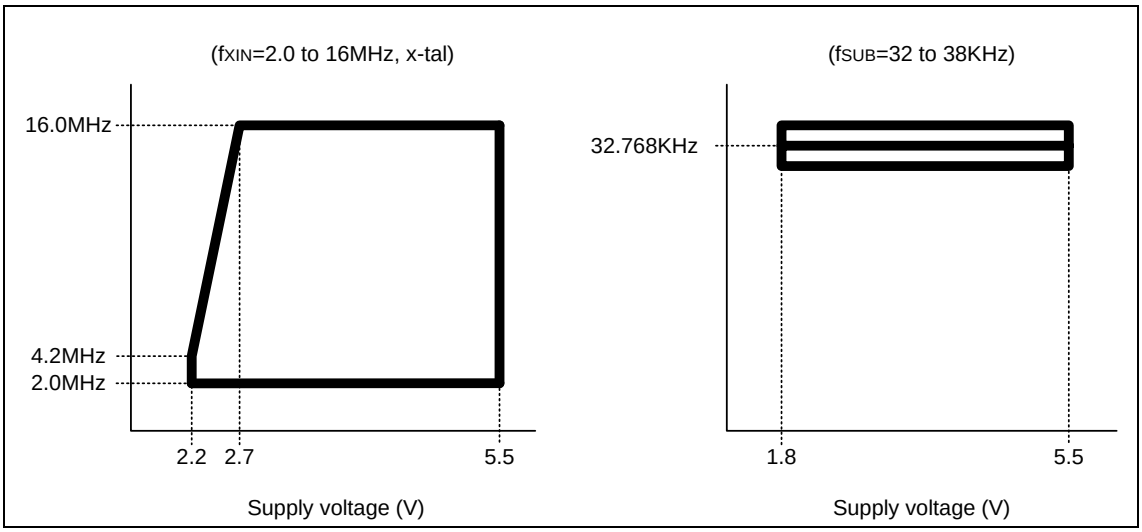


Figure 25.8 Operating Voltage Range

25.1.21 PLL ELECTRICAL CHARACTERISTICS

Table 25.19 PLL Electrical Characteristics (Temperature: -40 ~ +85℃)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Output Frequency	f_{OUT}	–	-	-	48	MHz
Operating Current	I_{DD}	@50MHz	–	-	1	mA
Duty	f_{DUTY}		40	–	60	%
VCO	f_{VCO}		0.8	–	192	MHz
Input Frequency	f_{IN}		2	8	16	MHz
Locking Time	t_{LOCK}				60	us

25.1.22 COMPARATOR CHARACTERISTICS

Table 25.20 Comparator Characteristics (Temperature: -40 ~ +85℃)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Operating Voltage	VDDEXT		2.0		5.5	V
Input Offset Voltage	VOS	VDDEDXT=5V, VIN=1/2 VDDEXT, Before Offset Calibration	-	±10	±20	mV
		VDDEDXT=5V, VIN=1/2 VDDEXT, After Offset Calibration			±5	mV
Propagation Delay	$t_{PD}(t_{PHL}, t_{PLH})$	V_{ov} > 10mV	-	0.5	2	us
Comparator Input Voltage	V_{CIN}		GND+50	-	VDDEXT-50	mV
Hysteresis	V_{OS}	VDDEDXT=5V, HYSSEL=0	-	±5	±25	mV
		VDDEDXT=5V, HYSSEL=1		±20	±60	mV
Comparator Current	$IDD_{(RMS)}$	V_{DD} =5V		70	100	uA

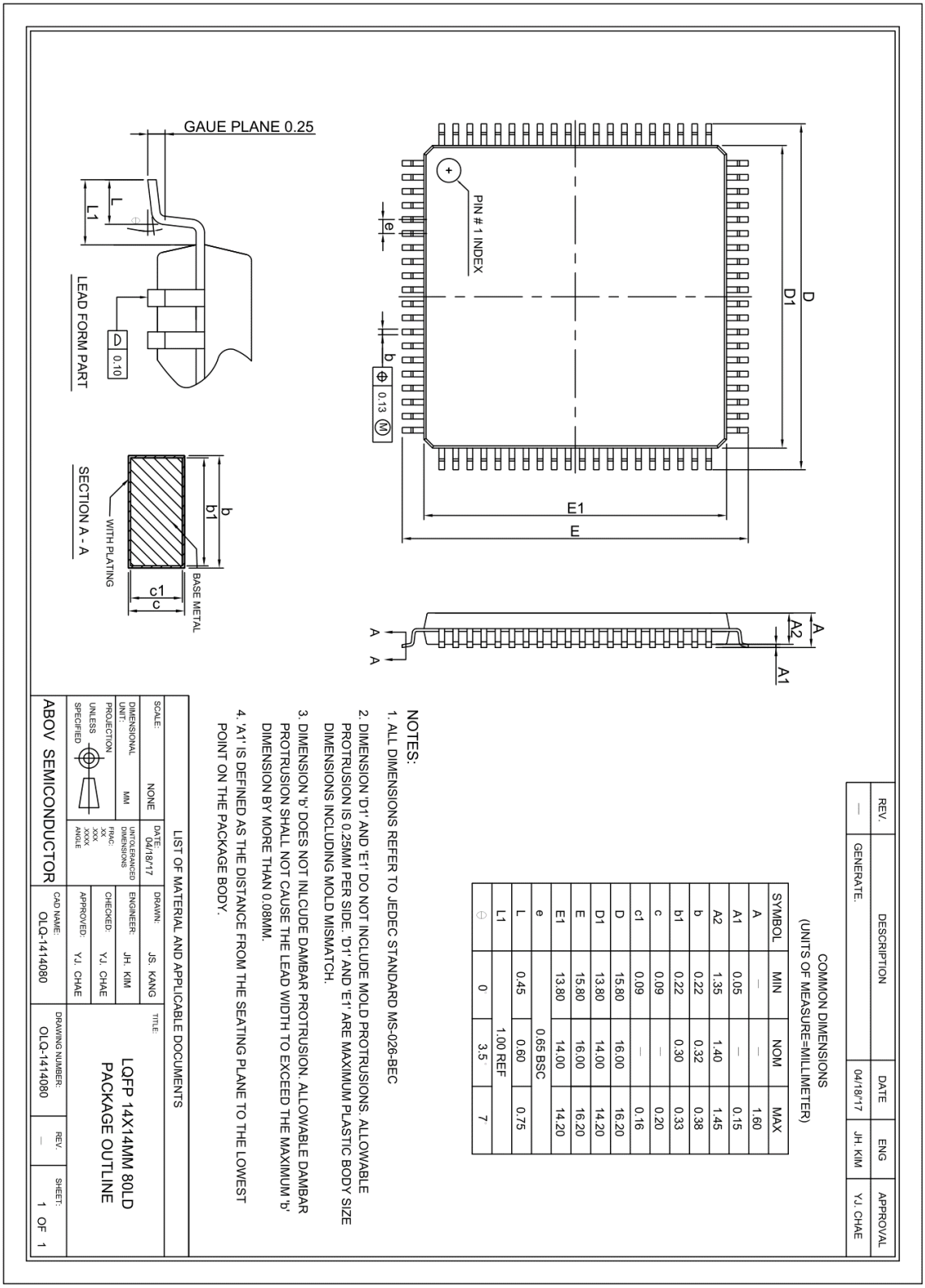
25.1.23 D/A CONVERTER CHARACTERISTICS

Table 25.21 D/A Converter Characteristics (Temperature: -40 ~ +85℃, V_{DD}=1.8-5.5V, V_{DD}=DAVREF, V_{ss}=0)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Resolution	-	-	-	-	12	Bit
Analog Output Voltage	D_{AOUT}		GND+0.1	-	AV_{DD}-0.1	V
Reference Input Voltage	EXTREF		2.7	-	AV_{DD}	V
Integral Nonlinearity	INL	@AVDD=5V or EXTREF_A=5V	-	-±6	±10	LSB
Differential Nonlinearity	DNL		-	±6	±10	LSB
D/AC Current	I_{DAC}		-	0.6	0.8	mA
Conversion Time	-		-	-	2	Us

CHAPTER 26. Package

26.1 **80LQFP14 Package dimension**



COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	—	—	1.60
A1	0.05	—	0.15
A2	1.35	1.40	1.45
b	0.22	0.32	0.38
b1	0.22	0.30	0.33
c	0.09	—	0.20
c1	0.09	—	0.16
D	15.80	16.00	16.20
D1	13.80	14.00	14.20
E	15.80	16.00	16.20
E1	13.80	14.00	14.20
e		0.65 BSC	
L	0.45	0.60	0.75
L1		1.00 REF	
θ	0°	3.5°	7°

NOTES:
1. ALL DIMENSIONS REFER TO JEDEC STANDARD MS-026-BEC
2. DIMENSION 'D1' AND 'E1' DO NOT INCLUDE MOLD PROTRUSIONS. ALLOWABLE PROTRUSION IS 0.25MM PER SIDE. 'D1' AND 'E1' ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.
3. DIMENSION 'b' DOES NOT INLCUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUM 'b' DIMENSION BY MORE THAN 0.08MM.
4. 'A1' IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.

REV.	DESCRIPTION	DATE	ENG	APPROVAL
—	GENERATE.	04/18/17	JH. KIM	YJ. CHAE

LIST OF MATERIAL AND APPLICABLE DOCUMENTS

SCALE: NONE	DATE: 04/18/17	DRAWN: JS. KANG	TITLE: LQFP 14X14MM 80LD PACKAGE OUTLINE
DIMENSIONAL UNIT: MM	UNTOLERANCED DIMENSIONS	ENGINEER: JH. KIM	
PROJECTION	FRAC: XX XXX XXXX ANGLE	CHECKED: YJ. CHAE	
UNLESS SPECIFIED		APPROVED: YJ. CHAE	
ABOV SEMICONDUCTOR	CAD NAME: OLQ-1414080	DRAWING NUMBER: OLQ-1414080	REV: —
			SHEET: 1 OF 1

Figure 26.1 Package dimension (80LQFP14)

26.2 **80LQFP12 Package dimension**

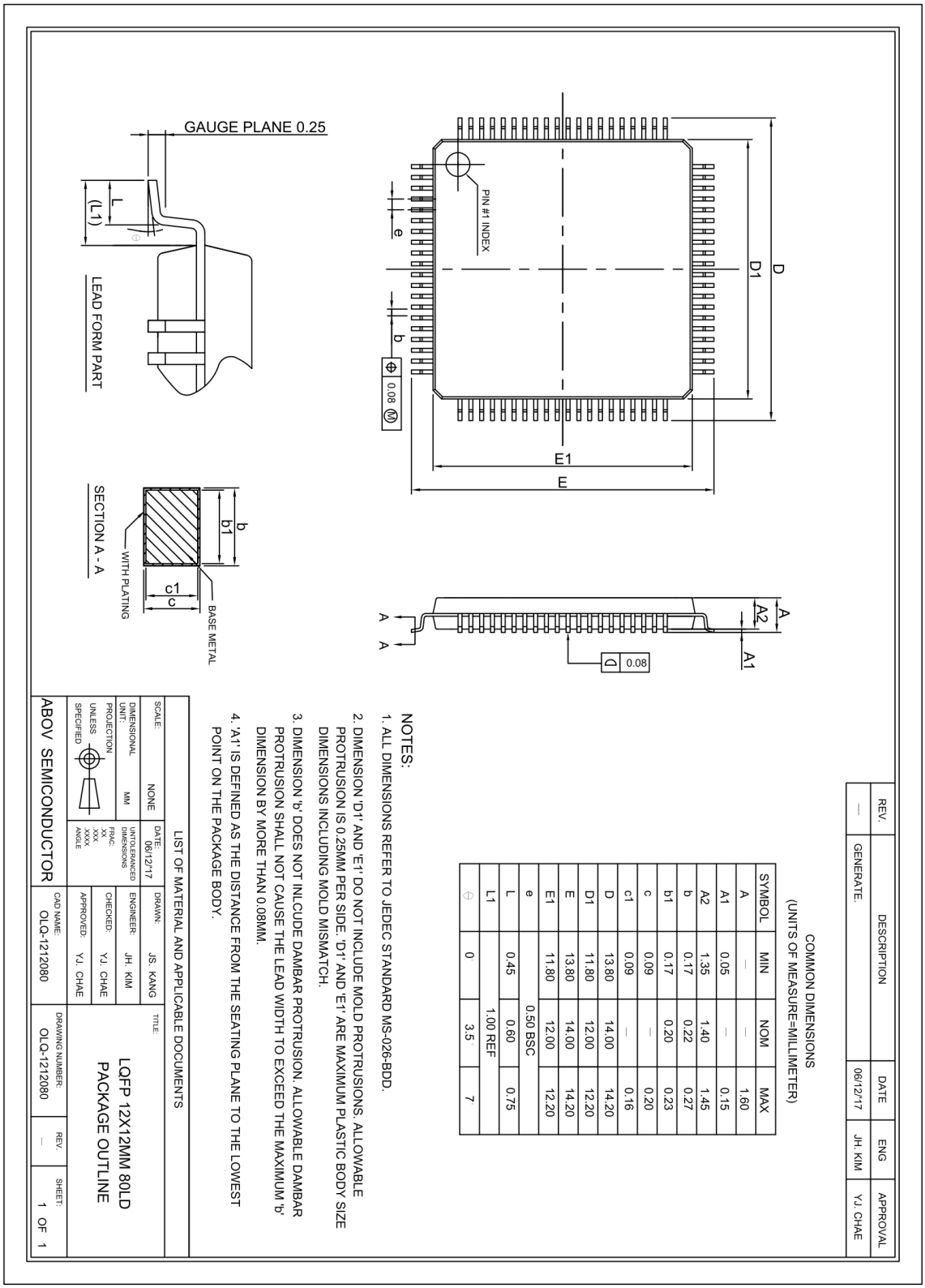


Figure 26.2 Package dimension (80LQFP12)

26.3 64LQFP12 Package dimension

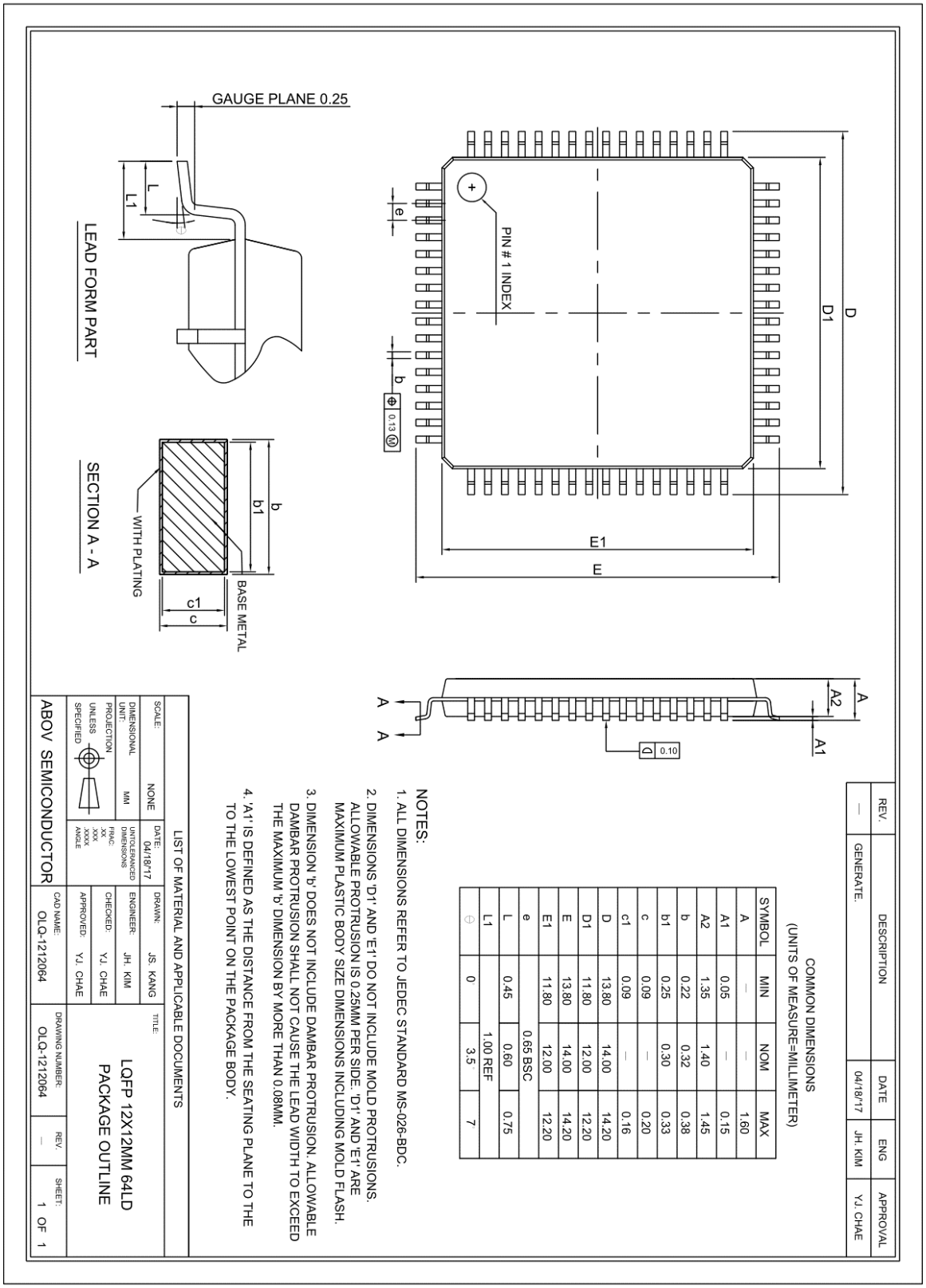


Figure 26.3 Package dimension (64LQFP12)

26.4 64LQFP10 Package dimension

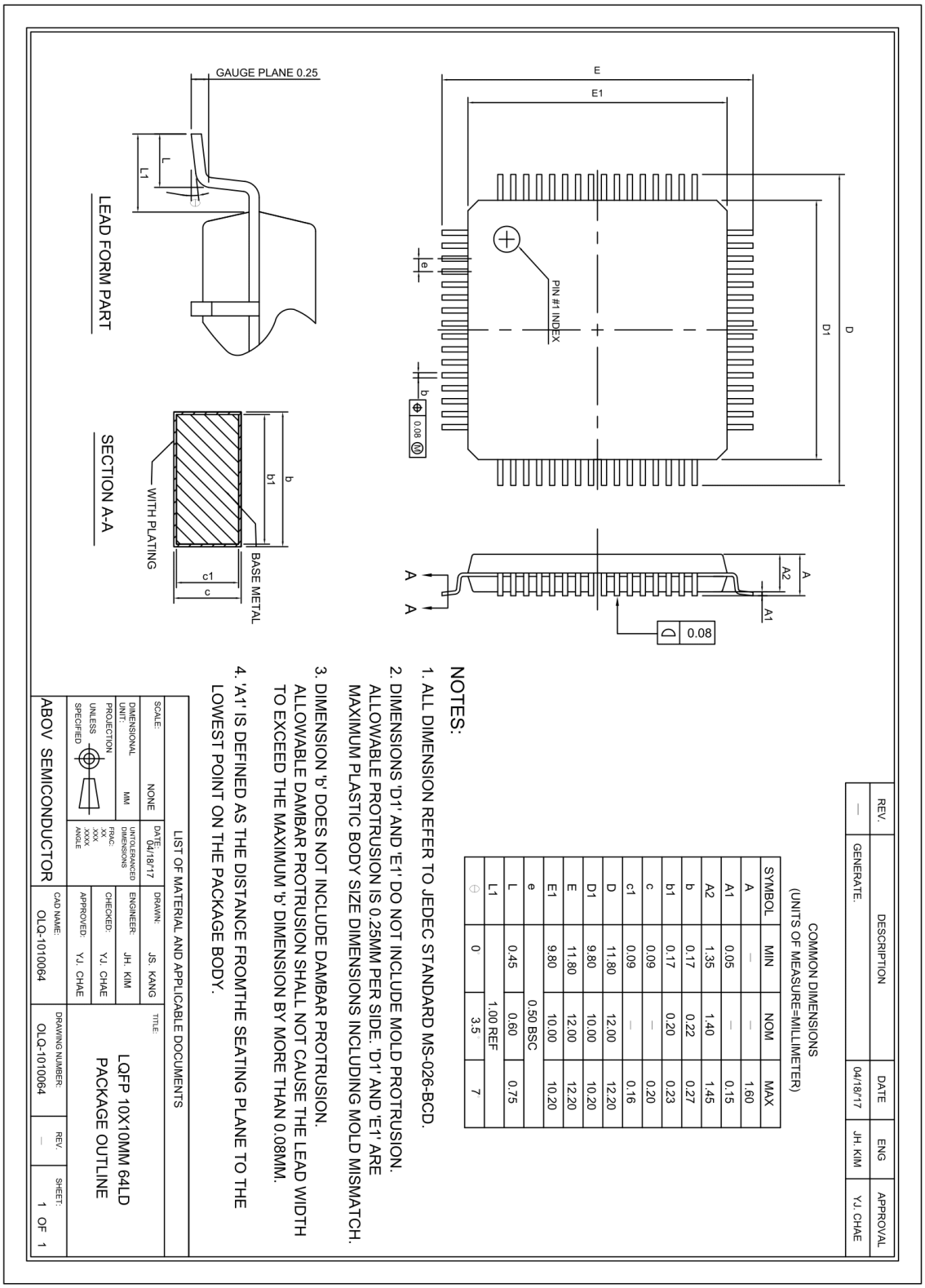


Figure 26.4 Package dimension (64LQFP10)

26.5 48LQFP Package dimension

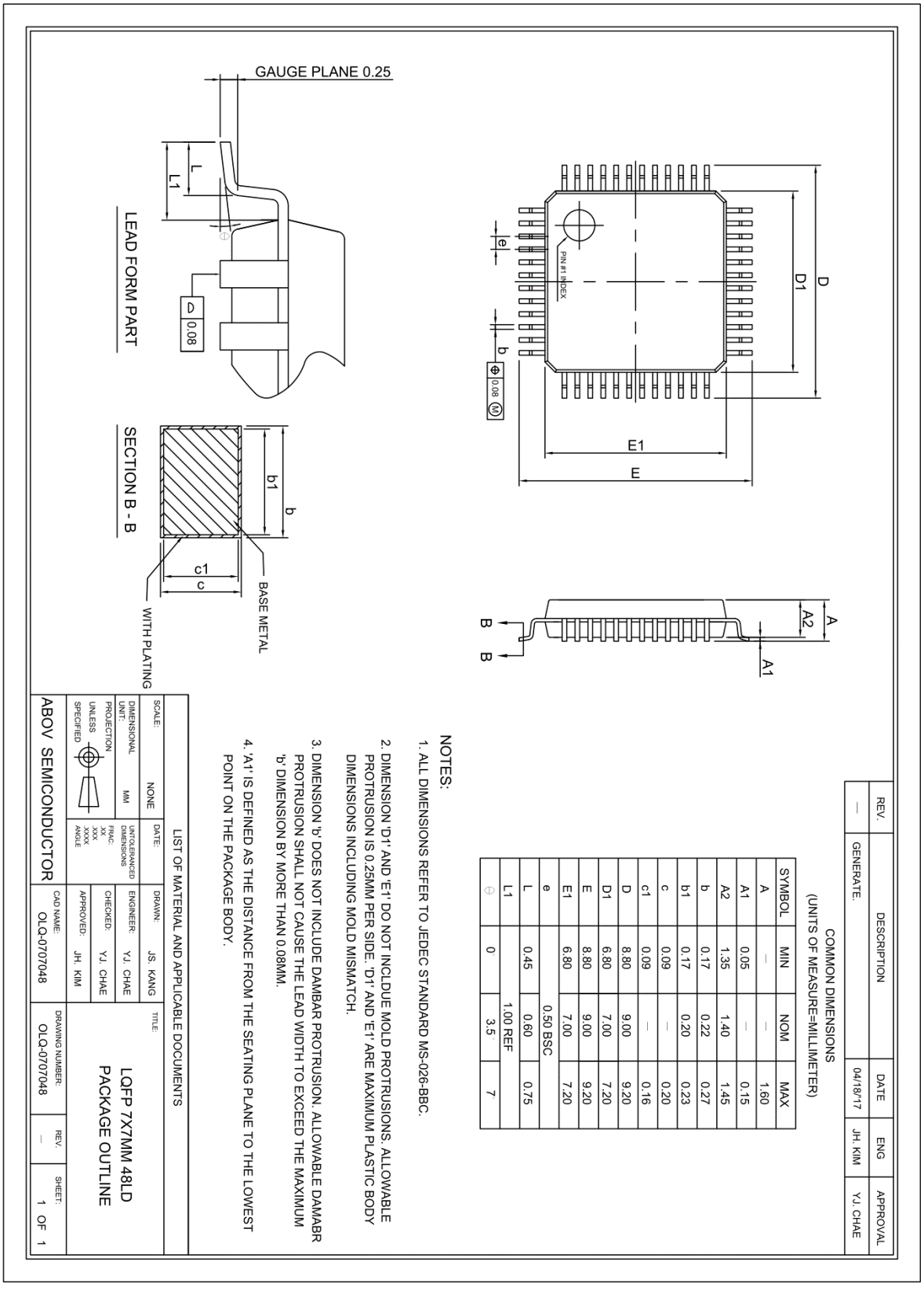


Figure 26.5 Package dimension (48LQFP)

26.6 48QFN Package dimension

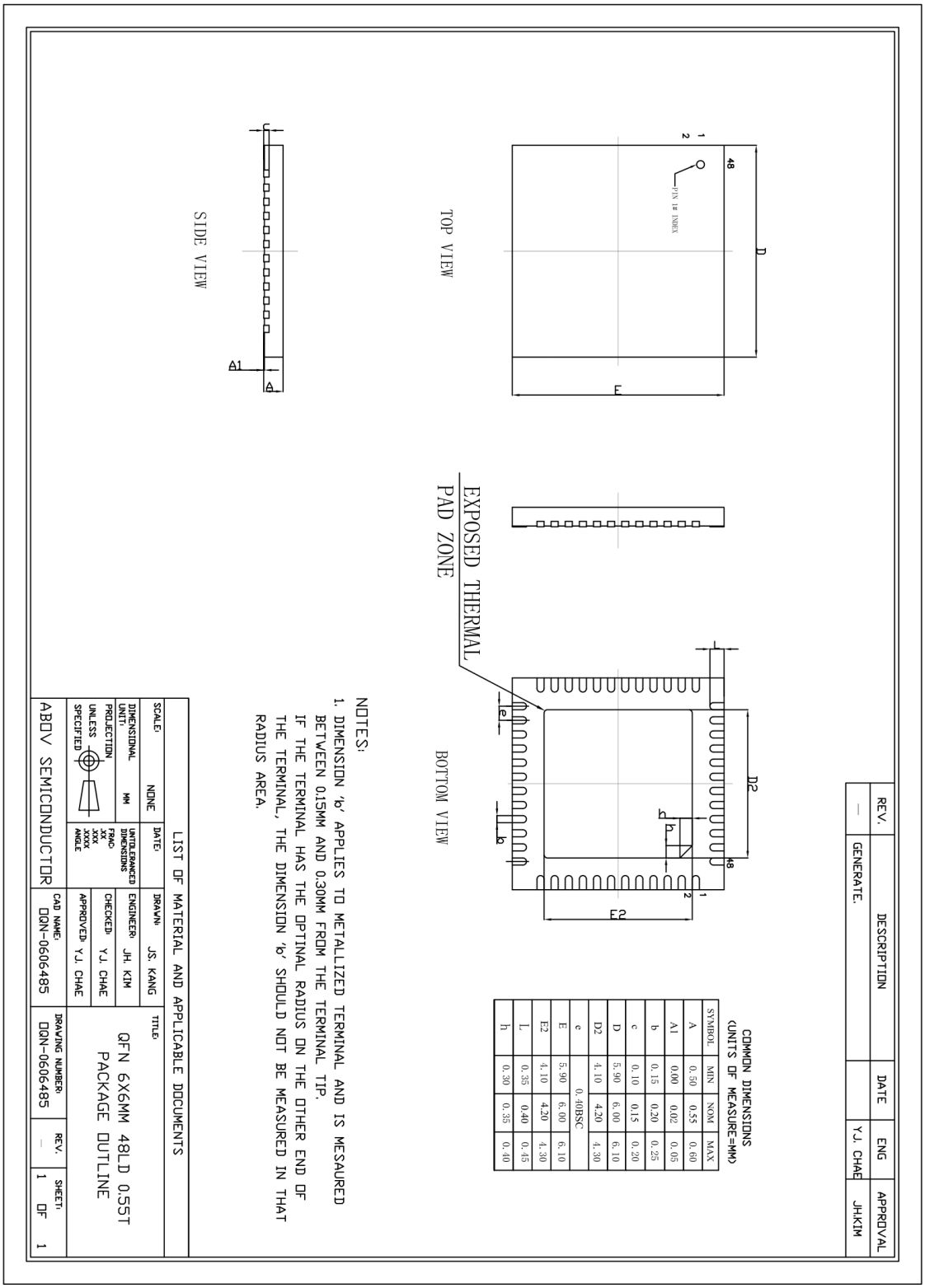
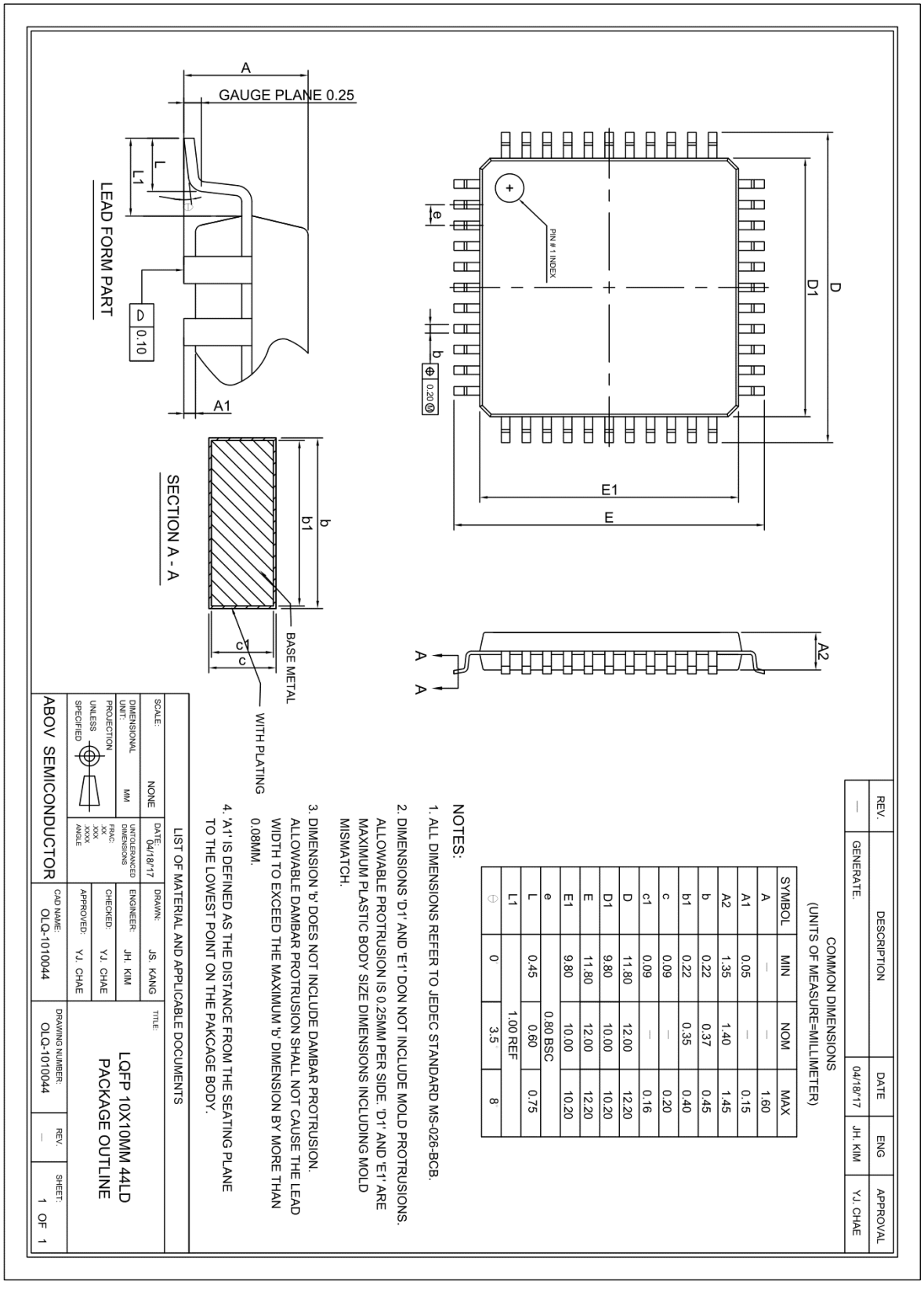


Figure 26.6 Package dimension (48QFN)

26.7 44LQFP Package dimension



COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	—	—	1.60
A1	0.05	—	0.15
A2	1.35	1.40	1.45
b	0.22	0.37	0.45
b1	0.22	0.35	0.40
c	0.09	—	0.20
c1	0.09	—	0.16
D	11.80	12.00	12.20
D1	9.80	10.00	10.20
E	11.80	12.00	12.20
E1	9.80	10.00	10.20
e		0.80 BSC	
L	0.45	0.60	0.75
L1		1.00 REF	
θ	0	3.5	8

NOTES:

1. ALL DIMENSIONS REFER TO JEDEC STANDARD MS-026-BCB.
2. DIMENSIONS 'D1' AND 'E1' DON NOT INCLUDE MOLD PROTRUSIONS. ALLOWABLE PROTRUSION IS 0.25MM PER SIDE. 'D1' AND 'E1' ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.
3. DIMENSION 'b' DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUM 'b' DIMENSION BY MORE THAN 0.08MM.
4. 'A1' IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PAKCAGE BODY.

REV.	DESCRIPTION	DATE	ENG	APPROVAL
—	GENERATE.	04/18/17	JH. KIM	YJ. CHAE

LIST OF MATERIAL AND APPLICABLE DOCUMENTS

SCALE:	NONE	DATE: 04/18/17	DRAWN:	JS. KANG
DIMENSIONAL UNIT:	MM	UNTOLERANCED DIMENSIONS	ENGINEER:	JH. KIM
PROJECTION		FRAC:	CHECKED:	YJ. CHAE
UNLESS SPECIFIED		X .XX .XXX .XXXX ANGLE	APPROVED:	YJ. CHAE

ABOV SEMICONDUCTOR

CAD NAME: OLQ-1010044

TITLE: LQFP 10X10MM 44LD PACKAGE OUTLINE

DRAWING NUMBER: OLQ-1010044

REV: —

SHEET: 1 OF 1

Figure 26.7 Package dimension (44LQFP)