

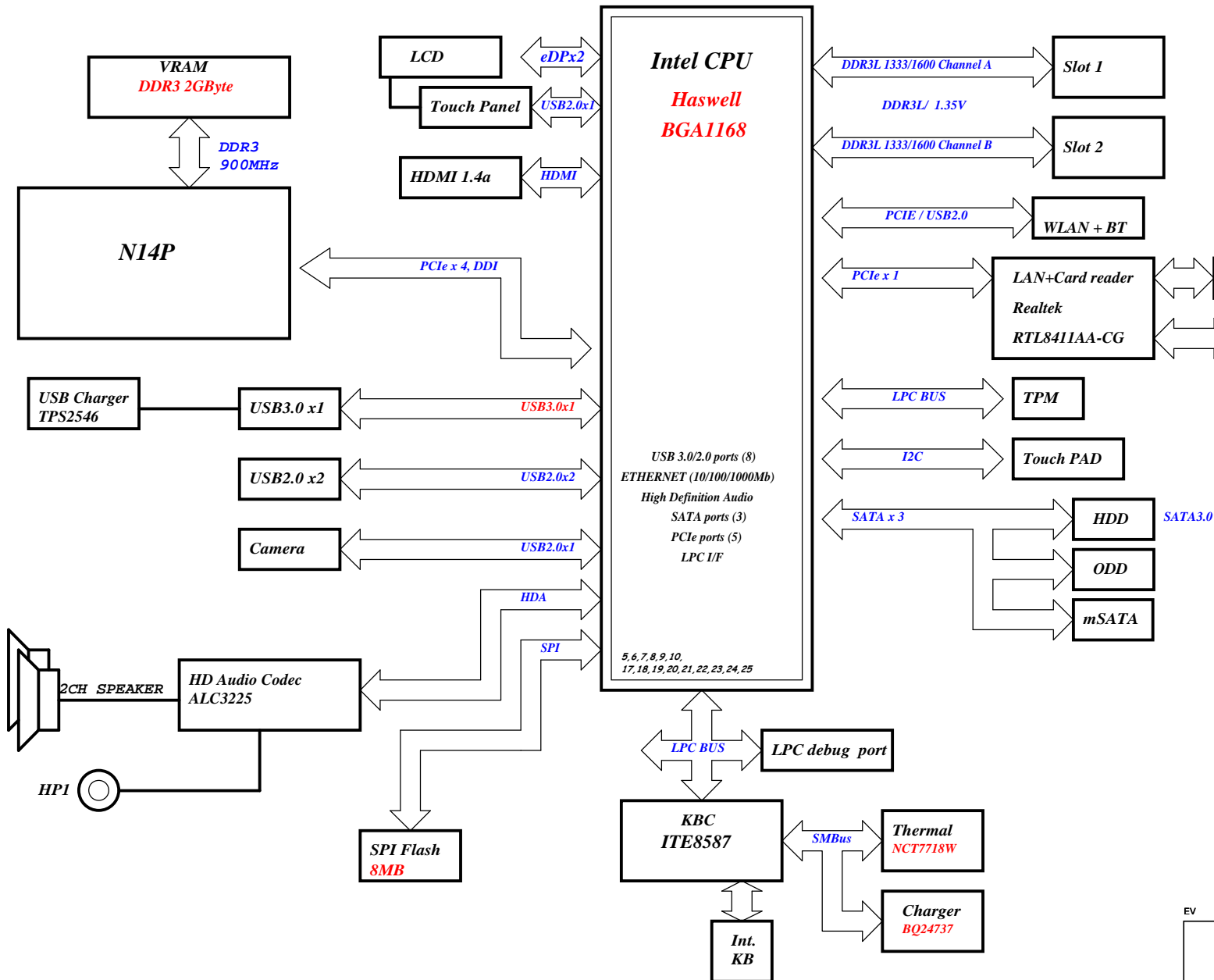
EA40_HU_ULT Schematics Document

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EV		A	
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Title			
Cover Page			
Size	Document Number	Rev	
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Date:	Monday, May 13, 2013	Sheet	1 of 102

EA40-HW ULV Board Block Diagram

Project code : 91.4YN01.001
 PCB P/N : 12243
 Revision : 1



CHARGER	
BQ24737	44
INPUTS	OUTPUTS
DCBATOUT	BT+
SYSTEM DC/DC	
TPS51225 45	
INPUTS	OUTPUTS
DCBATOUT	5V_Charger
	3d3V_S5
CPU DC/DC	
TPS51622 46-47	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE
SYSTEM DC/DC	
SYS8208A 48	
INPUTS	OUTPUTS
DCBATOUT	1D05V_VTT
SYSTEM DC/DC	
RT8207 49	
INPUTS	OUTPUTS
DCBATOUT	1D35V_S3
SYSTEM DC/DC	
SYW232 50	
INPUTS	OUTPUTS
DCBATOUT	1D8V_S0
SYSTEM DC/DC	
SYW232 51	
INPUTS	OUTPUTS
DCBATOUT	1D5V_S0
TPS51728RHAR 82	
INPUTS	OUTPUTS
DCBATOUT	VGA_CORE
Switches 83	
INPUTS	OUTPUTS
3D3V_S0	3D3V_VGA_S0
1D8V_S0	1D8V_VGA_S0
1V_S0	1V_VGA_S0
TPS51728RHAR 83	
INPUTS	OUTPUTS
DCBATOUT	1D5V_VGA_S0
PCB LAYER	
L1:Top	L4:Signal
L2:VCC	L5:GND
L3:Signal	L6:Bottom

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Title Block Diagram	
Size	Document Number
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Date: Monday, May 13, 2013	Rev 1
Date: Monday, May 13, 2013 Sheet 2 of 102	

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SSTP = CPU

vinafix

D

D

C

C

B

B

A

A

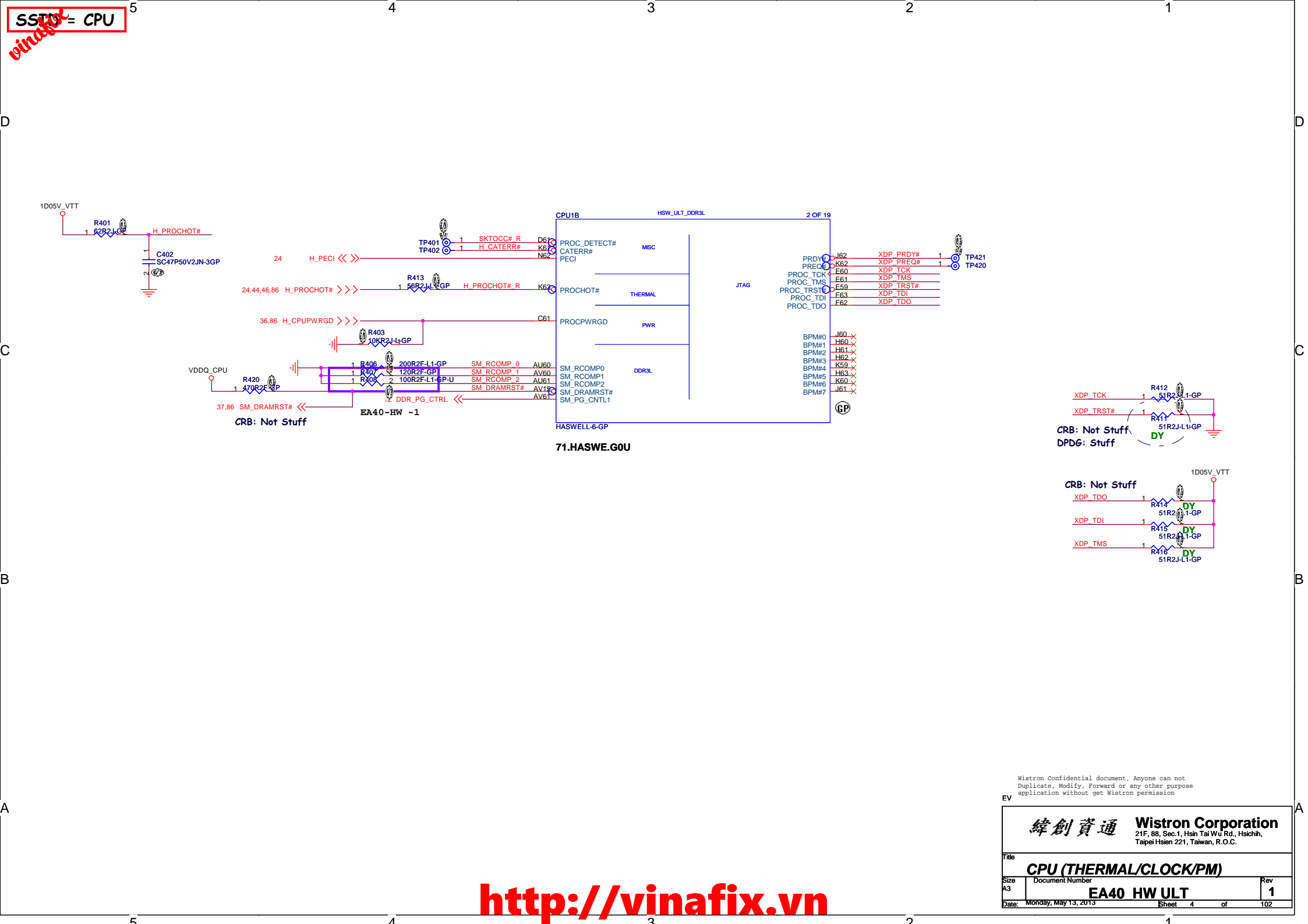
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CPU (Reserved)			
Size	Document Number	Rev	
A3	EA40 HW ULT	1	
Date:	Monday, May 13, 2013	Sheet	3 of 102

<http://vinafix.vn>

SSTN = CPU



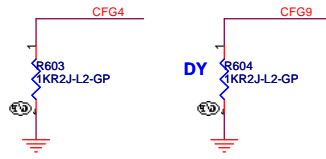
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CPU (THERMAL/CLOCK/PM)	
Title	
Size A3	Document Number
Date: Monday, May 13, 2013	Rev 1
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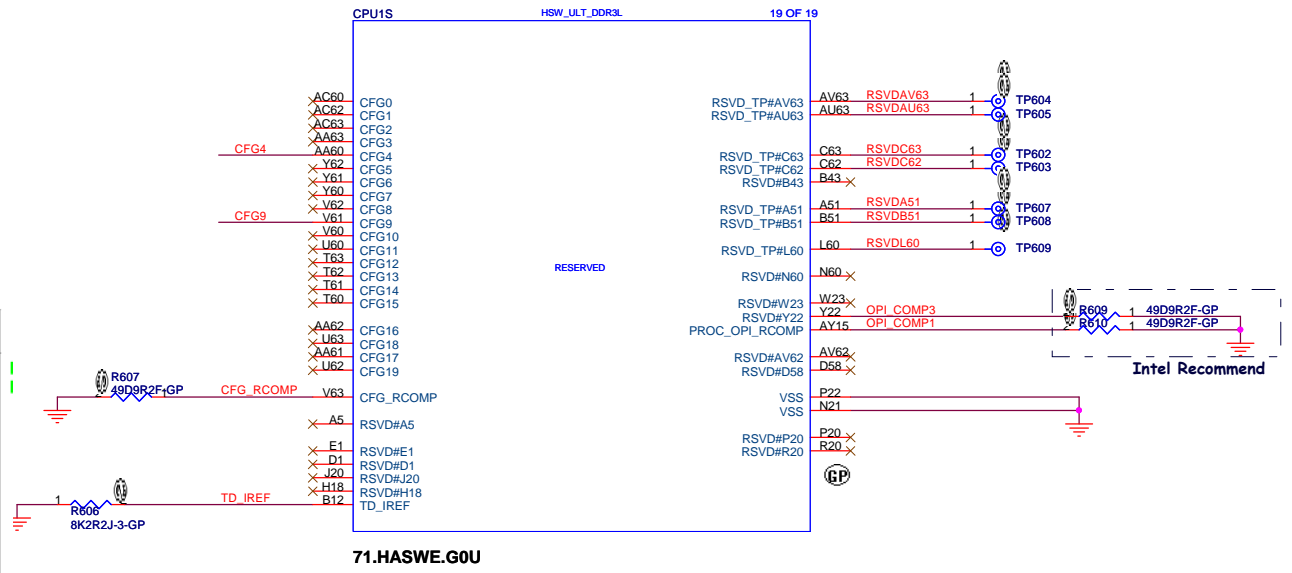
RSVD = CPU

eDP Enable	
CFG4	1:Disable
	0:Enable



Signal Name	Description	Direction/Buffer Type
CFG[19:0]	<p>Configuration Signals:</p> <p>The CFG signals have a default value of '1' if not terminated on the board. Refer to the appropriate platform design guide for pull-down recommendations when a logic low is desired.</p> <ul style="list-style-type: none"> • CFG[3:0]: Reserved configuration lane. A test point may be placed on the board for these lanes. • PCI Express* Static x16 Lane Numbering Reversal. — — • CFG[4]: eDP enable <ul style="list-style-type: none"> — 1 = Disabled — 0 = Enabled • [19:5]: Reserved configuration lanes. A test point may be placed on the board for these lands. 	I/O GTL
CFG_RCOMP	Configuration resistance compensation.	-
FC_x	FC signals are signals that are available for compatibility with other processors. A test point may be placed on the board for these lands. Refer to the appropriate platform design guide for implementation details.	

continued...



71.HASWE.G0U

7.4 Reserved or Unused Signals

The following are the general types of reserved (RSVD) signals and connection guidelines:

- RSVD – these signals should not be connected
- RSVD_TP – these signals should be routed to a test point
- RSVD_NCTF – these signals are non-critical to function and may be left unconnected

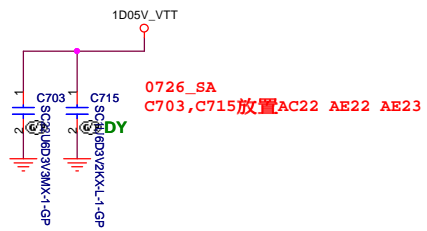
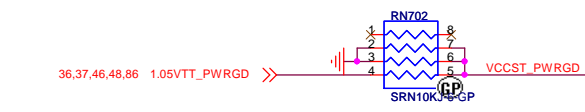
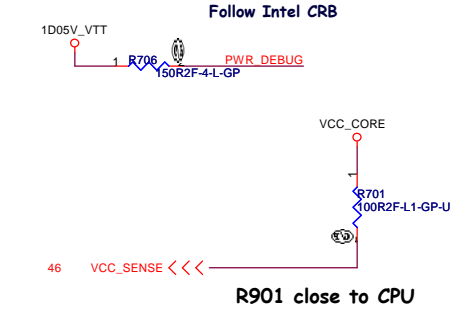
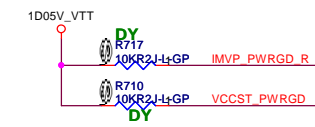
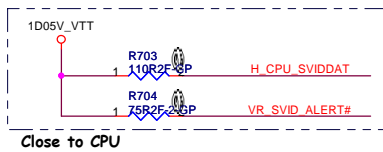
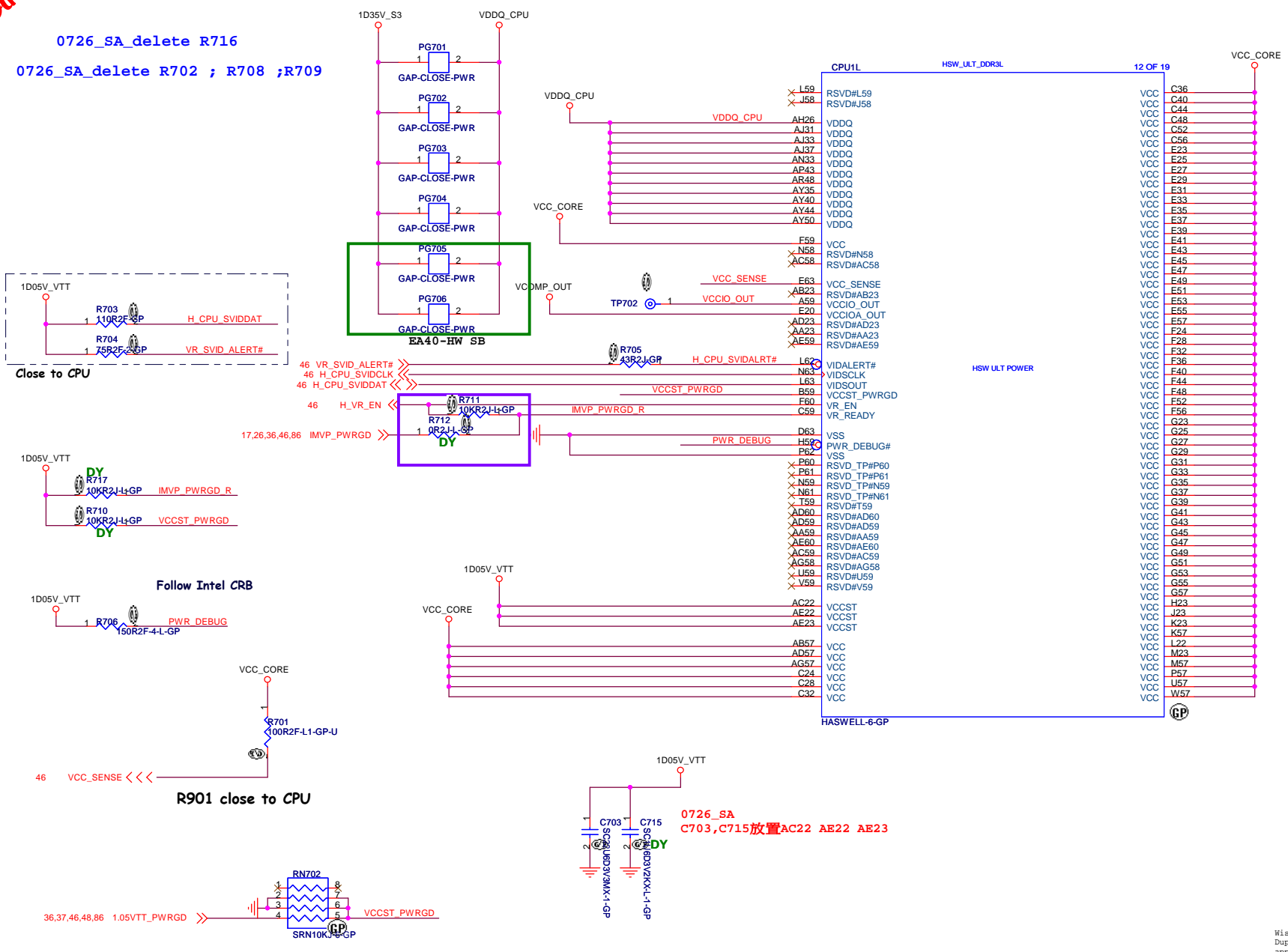
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CPU (CFG)			
Size Custom	Document Number		Rev
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SECRET = CPU

0726_SA_delete R716
0726_SA_delete R702 ; R708 ;R709

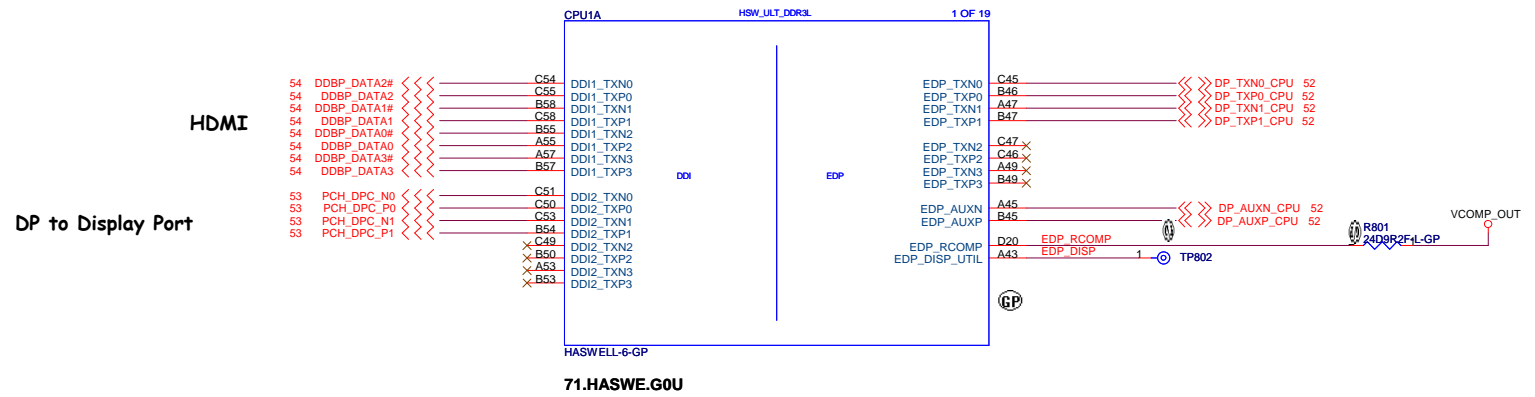


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Title CPU (VCC CORE)			
Size A3	Document Number	EA40 HW ULT	
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		Rev	1

SS = CPU

windot



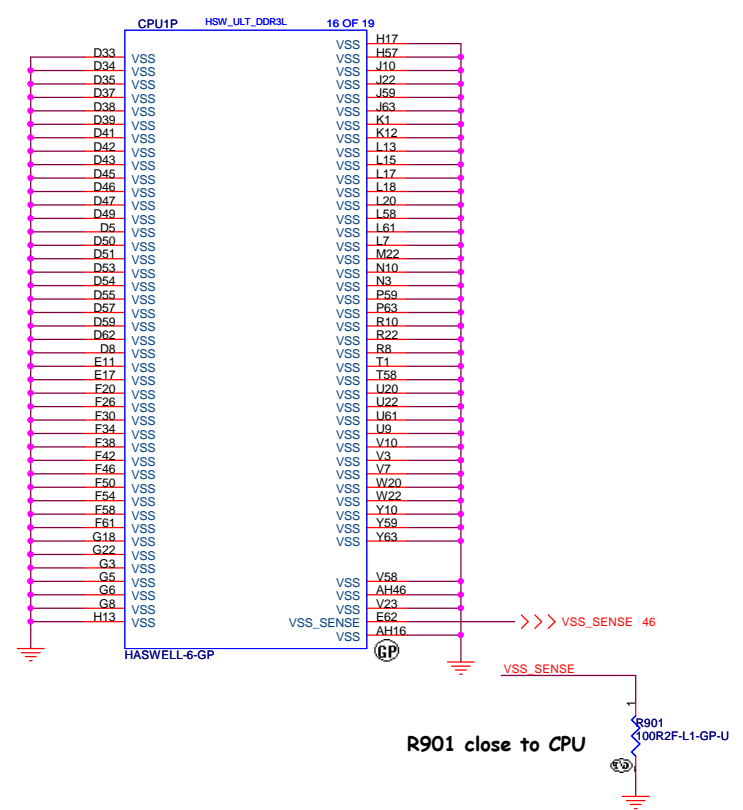
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Title CPU (DDI/EDP)		
Size Custom	Document Number EA40 HW ULT	Rev 1
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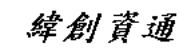
<http://vinafix.vn>

SSD = CPU

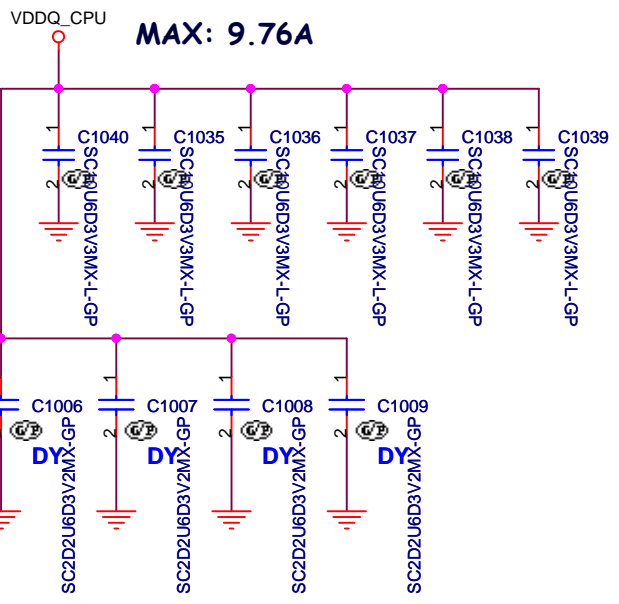


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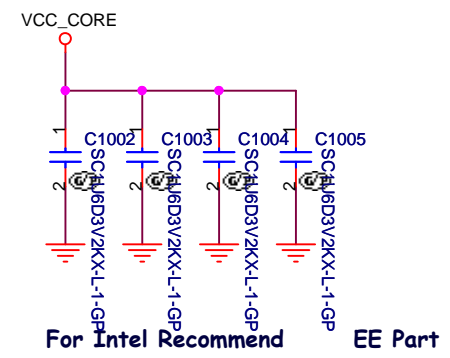
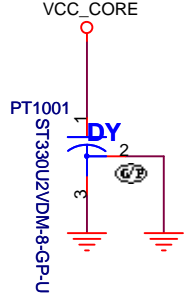
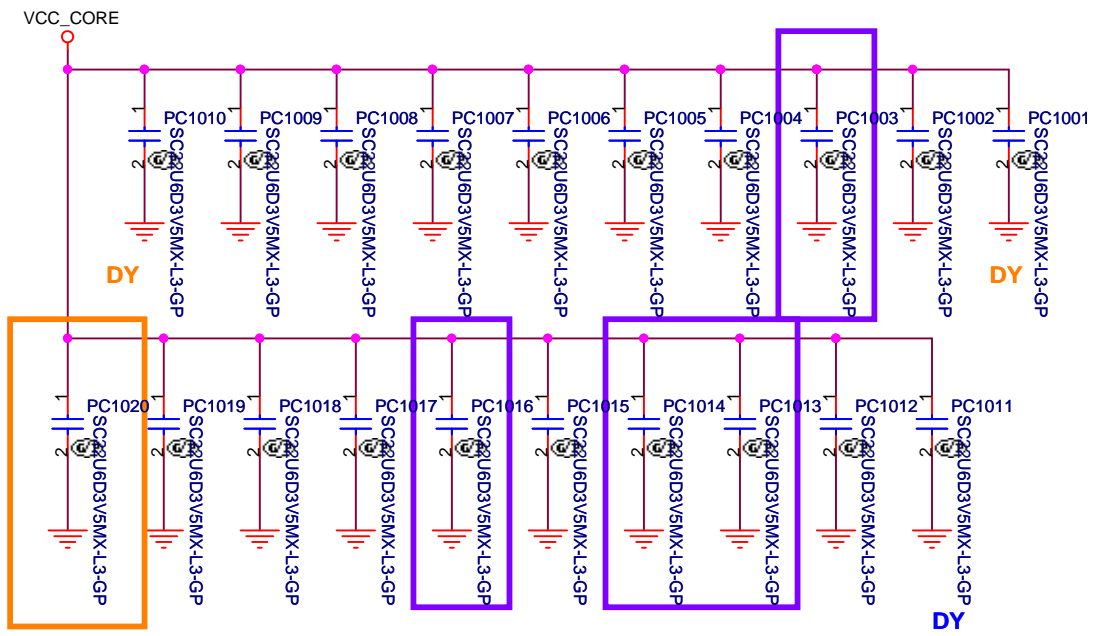
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CPU (VSS)	
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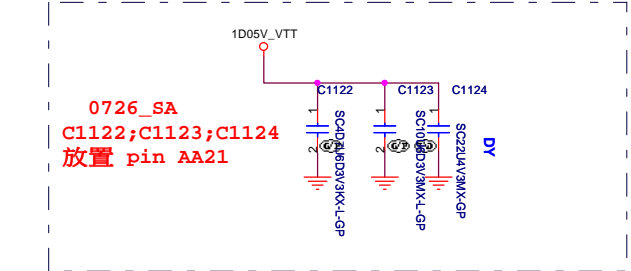
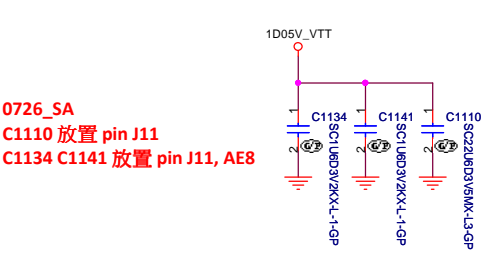
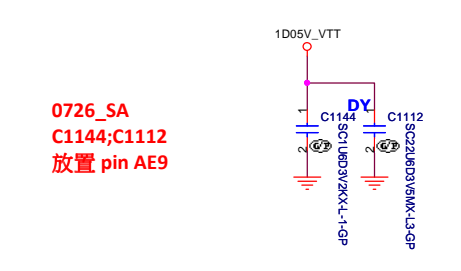
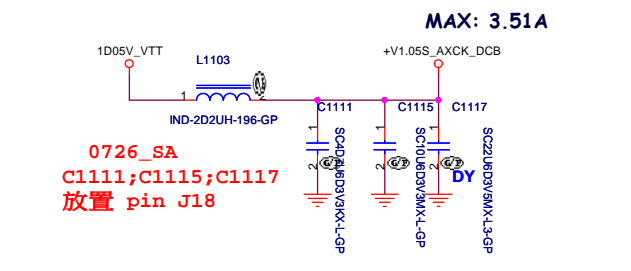
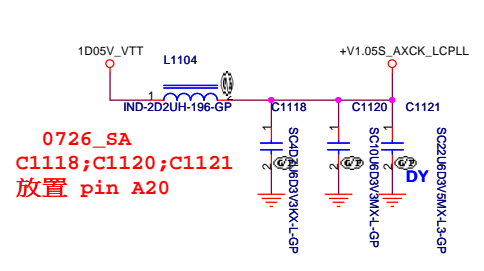
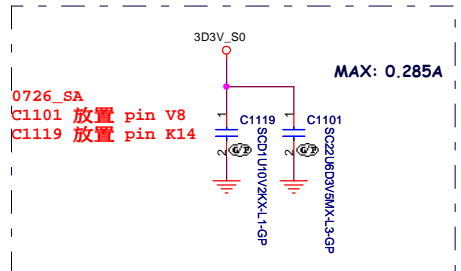
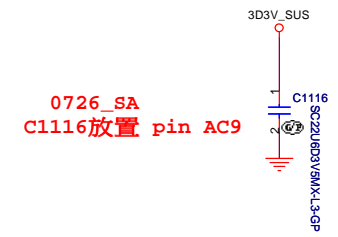
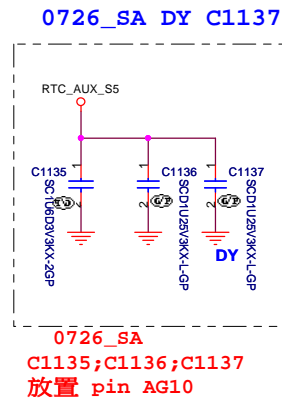
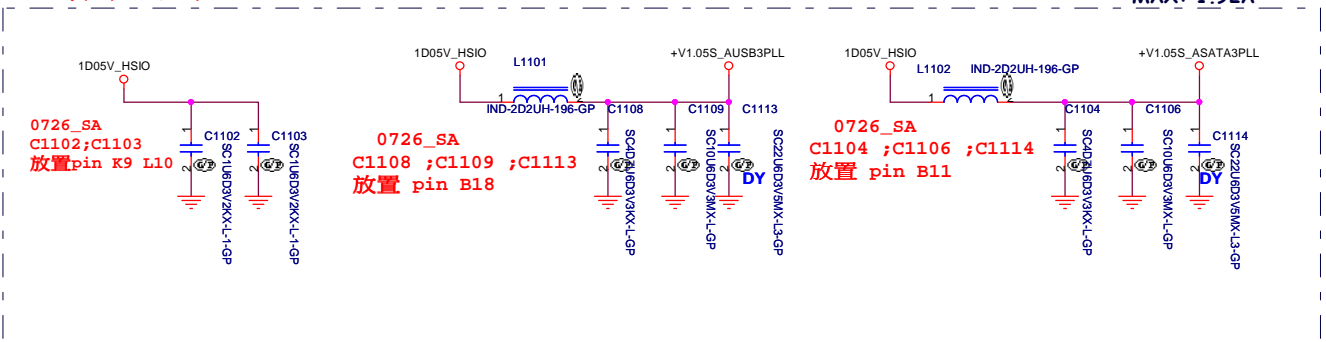


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CPU (Power CAP1)			
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0726_SA 擺放電容的位置請參考Page 21
每個位置如下



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		CPU (Power CAP2)	
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5 M.A.[A15:0] 5

M.A.A0	98	A0
M.A.A1	97	A1
M.A.A2	96	A2
M.A.A3	95	A3
M.A.A4	94	A4
M.A.A5	93	A5
M.A.A6	92	A6
M.A.A7	91	A7
M.A.A8	90	A8
M.A.A9	89	A9
M.A.A10	88	A10
M.A.A11	87	A11
M.A.A12	86	A12
M.A.A13	85	A13
M.A.A14	84	A14
M.A.A15	83	A15
M.A.A16/BA2	79	A16/BA2

5 M.A.BS2 >>>

5 M.A.BS0

5 M.A.BS1

M.A.DD13<	5	DQ0
M.A.DD14<	6	DQ1
M.A.DD15<	7	DQ2
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M.A.DM0_ODT0	116	ODT0
M.A.DM0_ODT1	120	ODT1
VREF_CA	126	VREF_CA
VREF_DQ	1	VREF_DQ
RESET#	30	RESET#
VTT1	203	VTT1
VTT2	204	VTT2

62.10017.Z61

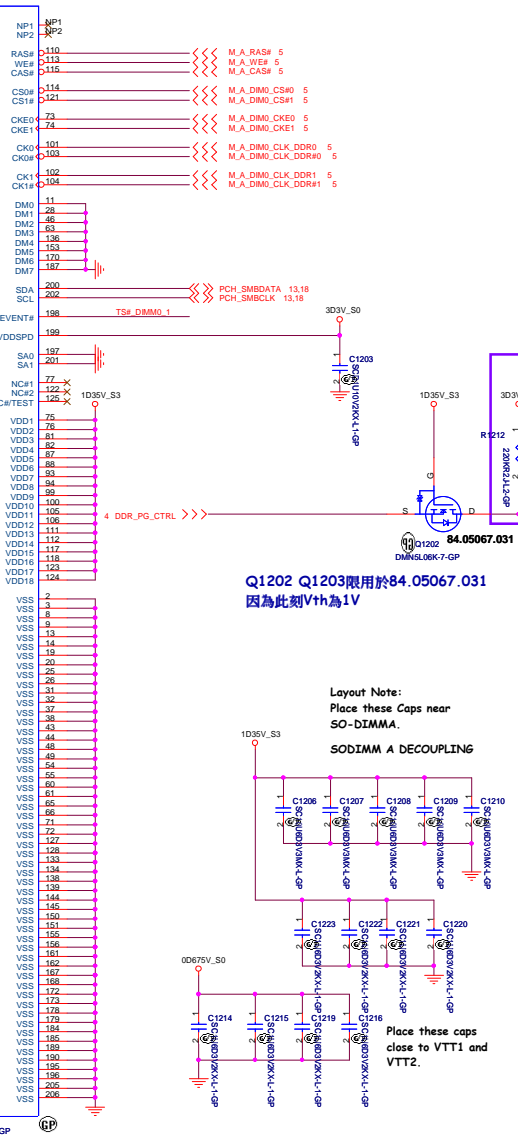
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3rd = 62.10024.M51

4th = 62.10017.X31

H = 4mm

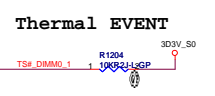
DDR3-204P-123-GP



0726_SA

Note:
If SA0_DIM0 = 0, SA1_DIM0 = 0
SO-DIMMA SPD Address is 0xA0
SO-DIMMA TS Address is 0x30

If SA0_DIM0 = 1, SA1_DIM0 = 0
SO-DIMMA SPD Address is 0xA2
SO-DIMMA TS Address is 0x32

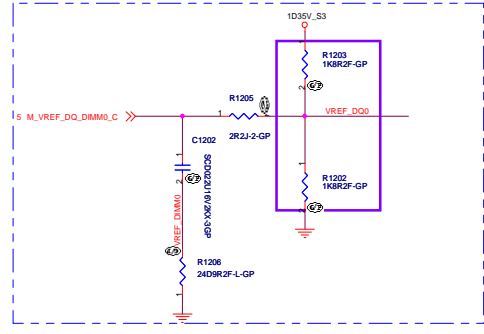
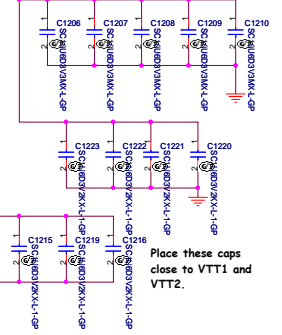


ODT resistor must be 66.5 ohm



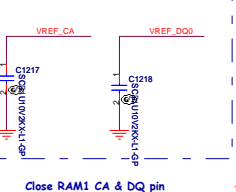
Q1202 Q1203 限用于 84.05067.031
因为此刻Vth为1V

Layout Note:
Place these Caps near SO-DIMMA.
SODIMM A DECOUPLING



For Intel Recommend Close to DIMM

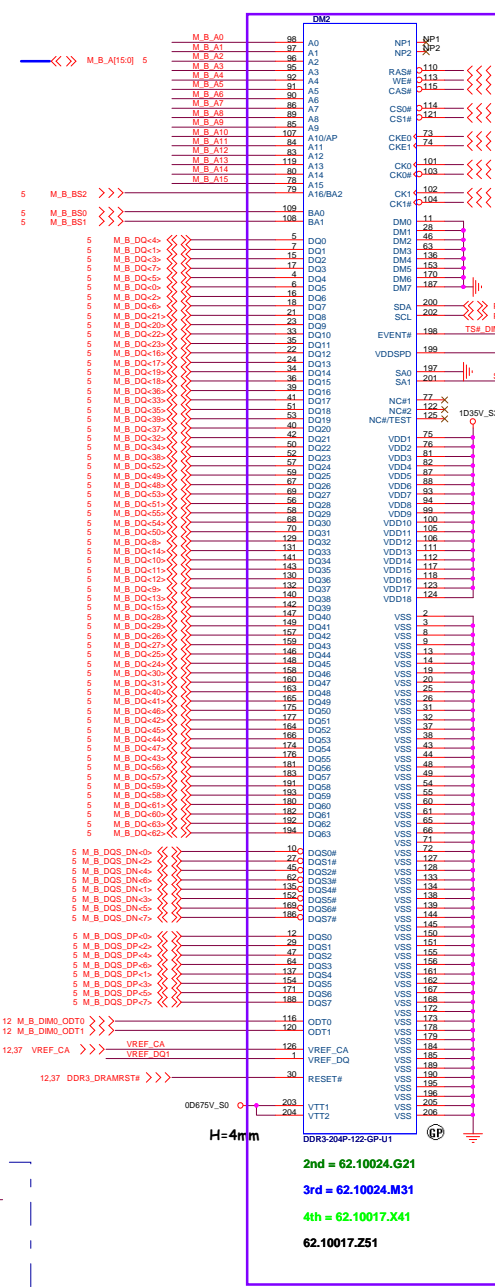
Place these caps close to VTT1 and VTT2.



Close RAM1 CA & DQ pin

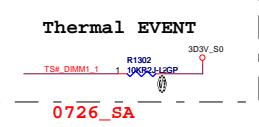
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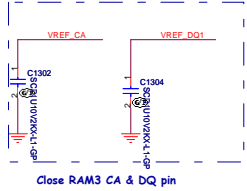
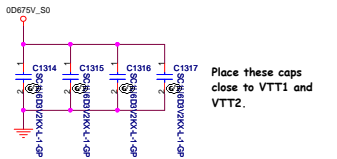
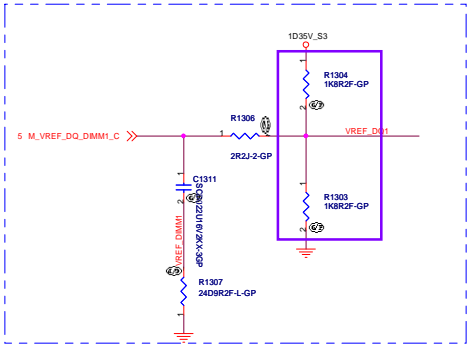
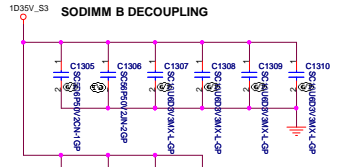


Note:
 SO-DIMMB SPD Address is 0x44
 SO-DIMMB TS Address is 0x34

SO-DIMMB is placed farther from the Processor than SO-DIMMA



Layout Note:
 Place these Caps near SO-DIMMB.



H=4mm
 DDR3-204P-122-GP-U1
 2nd = 62.10024.G21
 3rd = 62.10024.M31
 4th = 62.10017.X41
 62.10017.Z51

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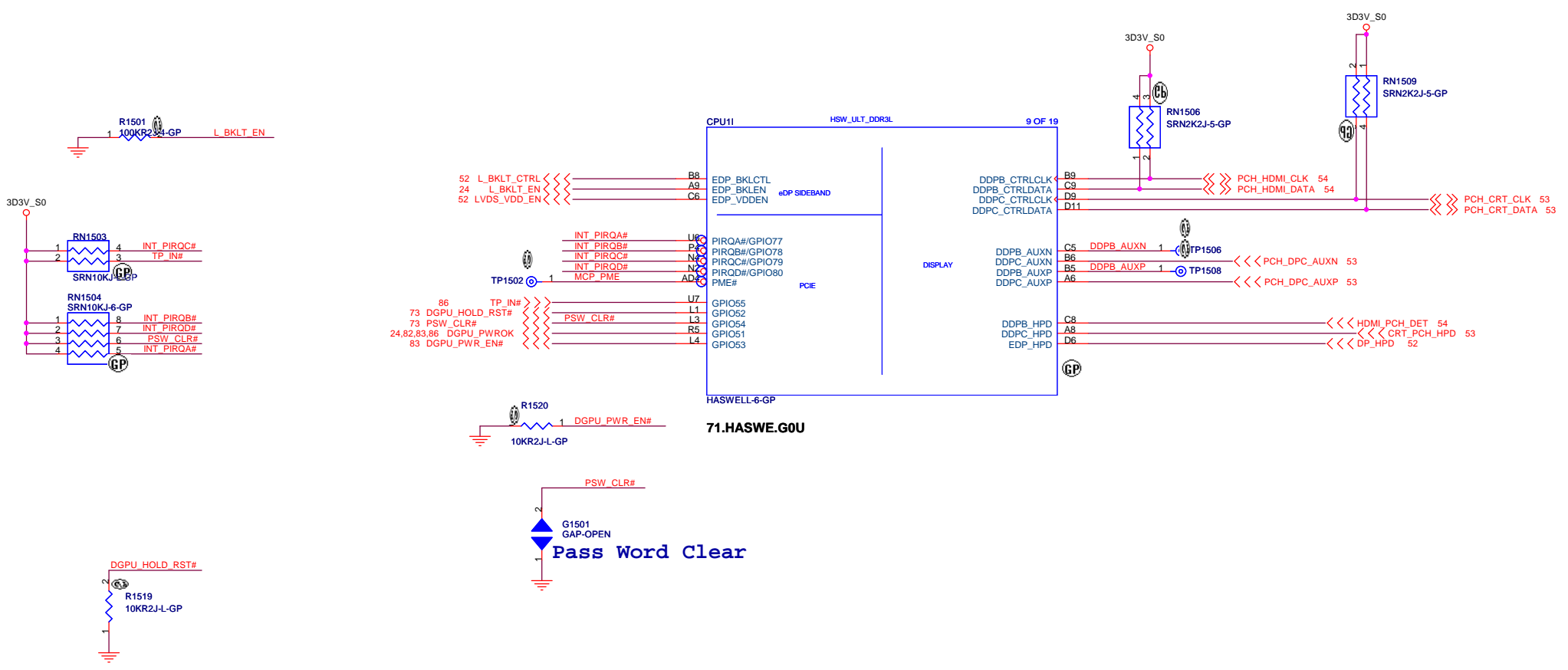
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Title		
(Reserved) SODIMM_SODIMM4		
Size	Document Number	Rev
A4	EA40 HW ULT	1
Date:	Monday, May 13, 2013	Sheet 14 of 102

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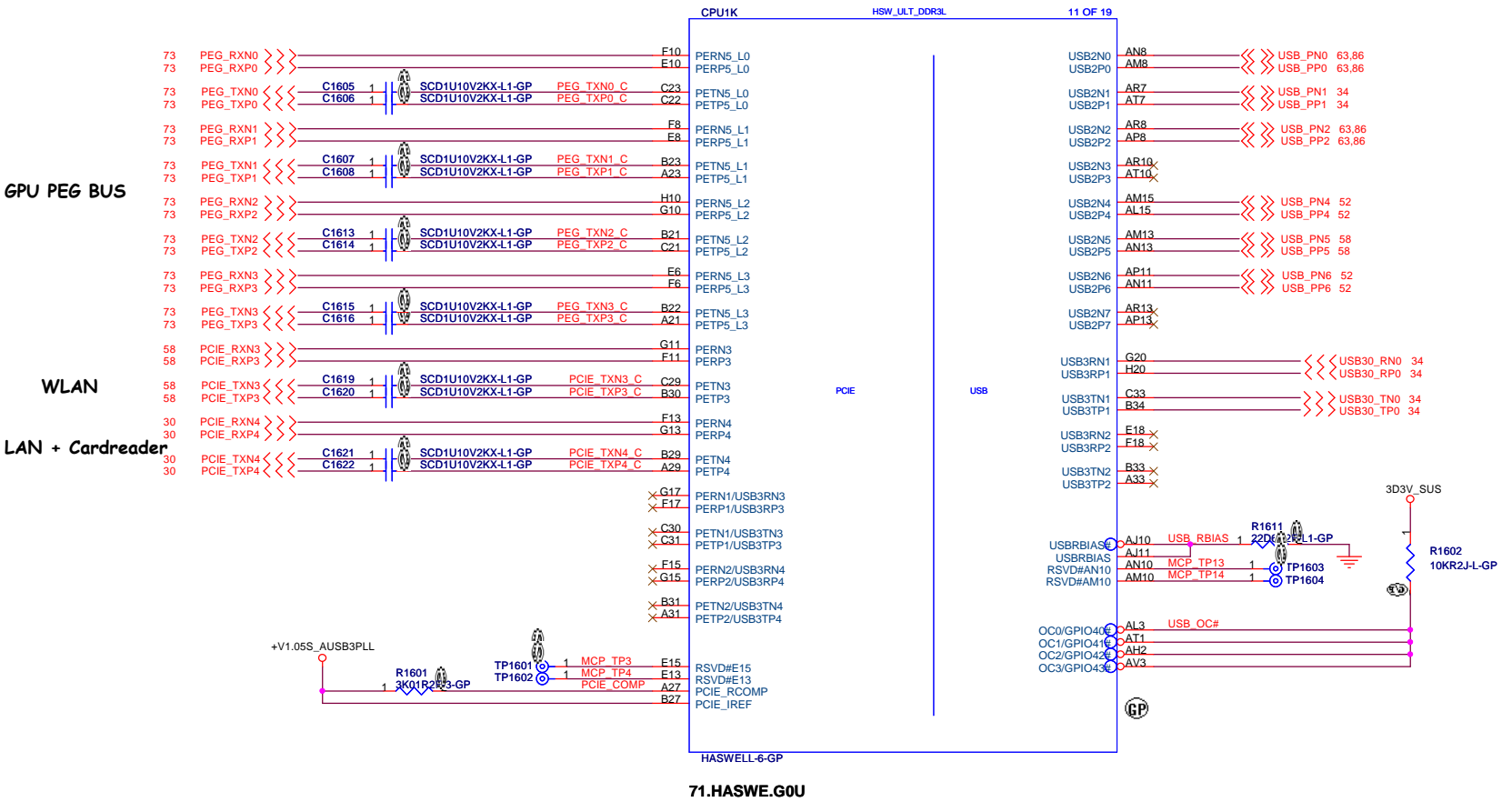
EV

緯創資通		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title CPU(EDP SIDEBAND/GPIO/DDI)			
Size A3	Document Number EA40 HW ULT		Rev 1
Date: Monday, May 13, 2013	Sheet 15	of	102

SSID = PCH

USB Table

Pair	Device
0	USB2.0 Port 1
1	USB3.0 Port 2(USB2.0)
2	USB2.0 Port 3
4	CCD
5	WLAN(Bluetooth)
6	Touch Penal
7	



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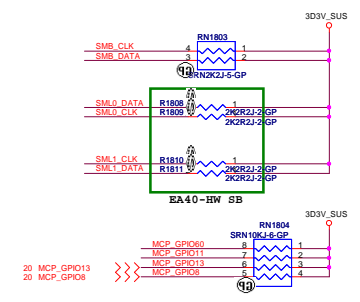
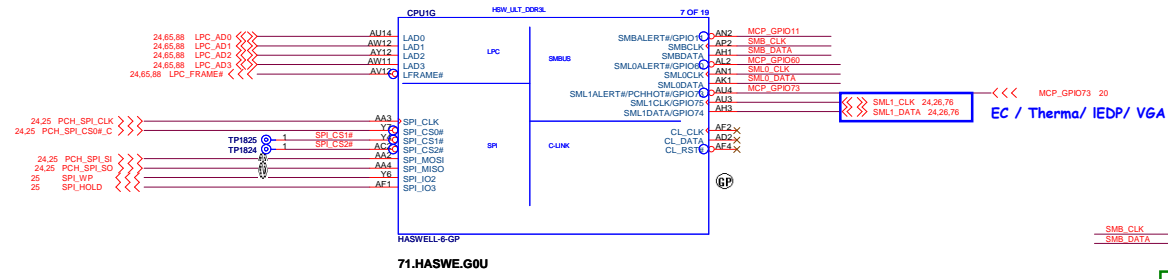
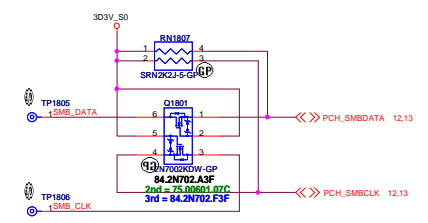
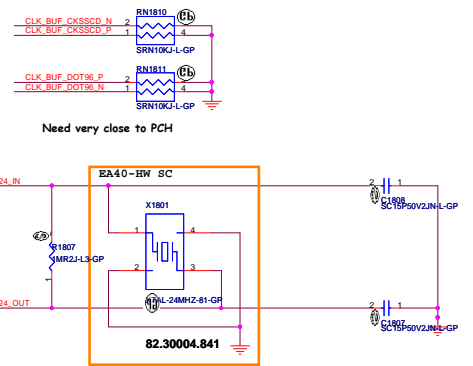
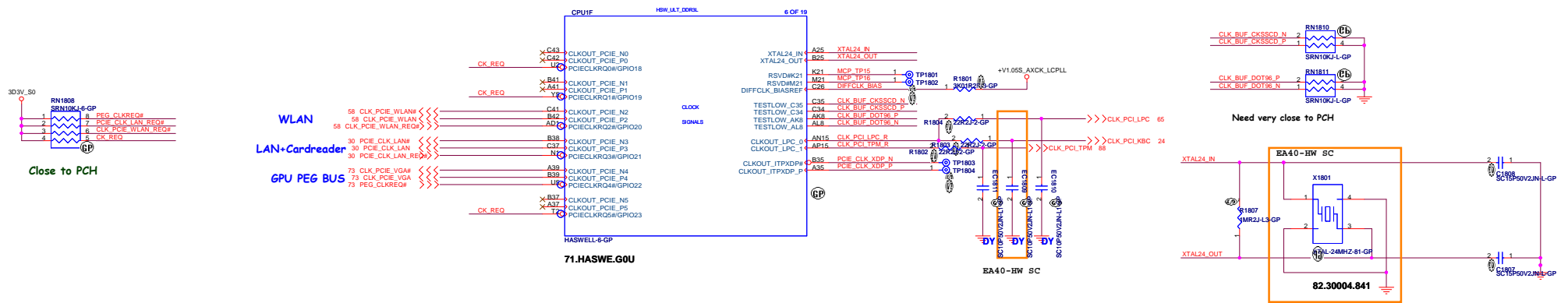
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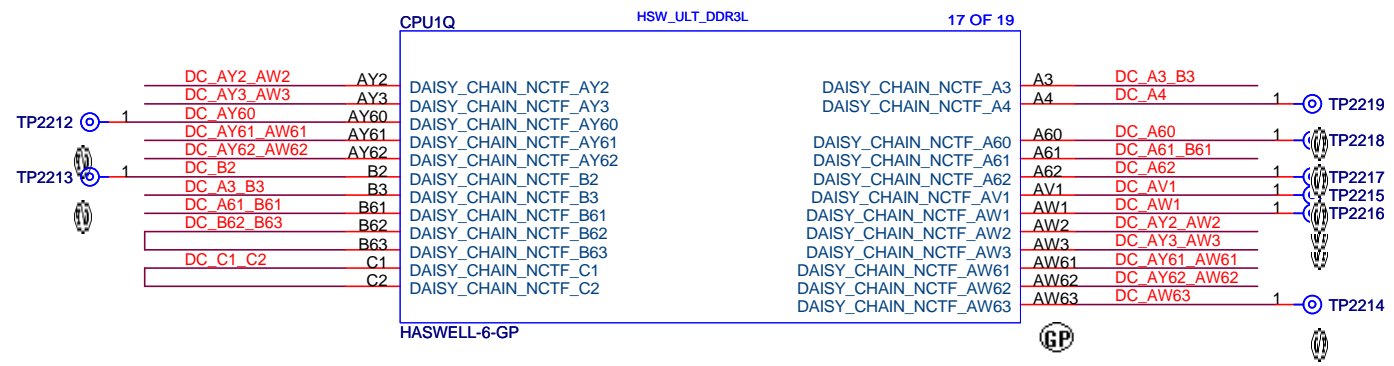
Title: **CPU (PCI/USB)**

Size A3	Document Number	Rev
	EA40 HW ULT	1
Date: Monday, May 13, 2013	Sheet 16	of 102

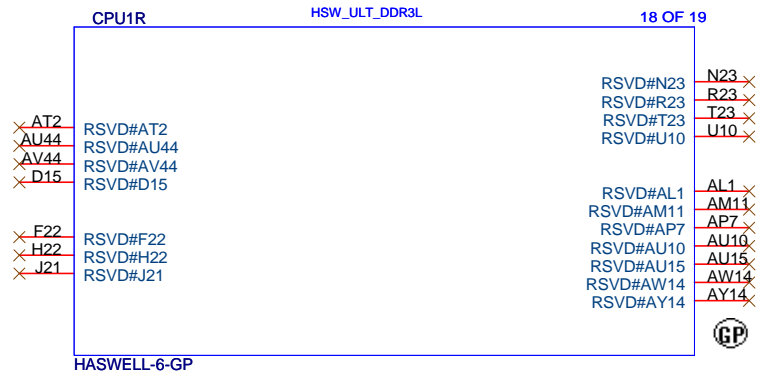
winafix.vn



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71.HASWE.G0U



71.HASWE.G0U

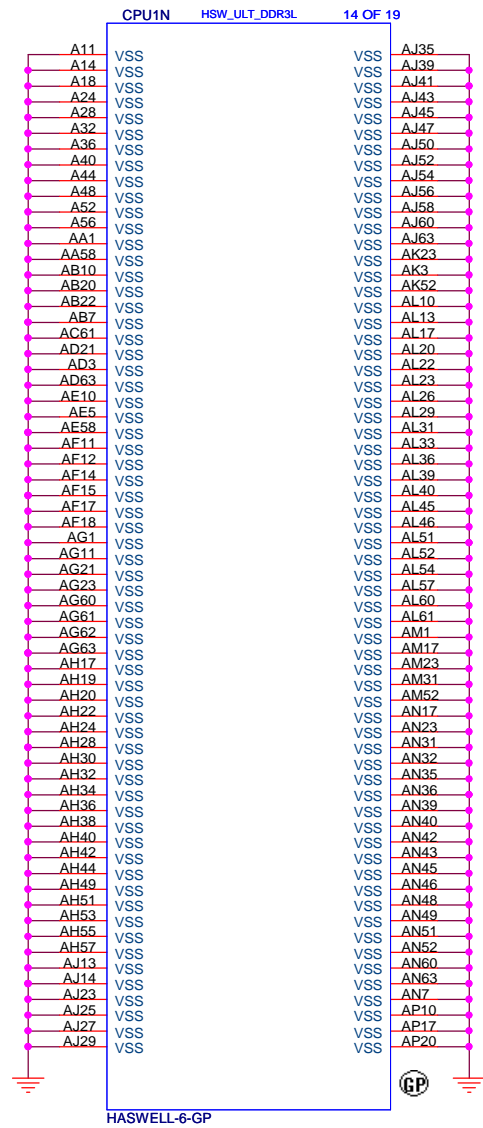
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EV

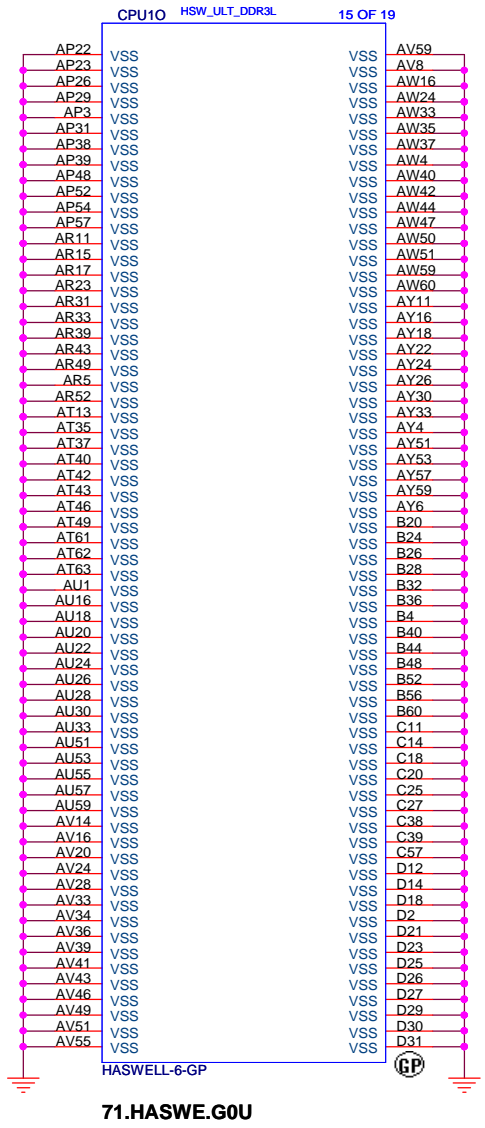
緯創資通		Wistron Corporation	
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Title			
CPU (RSVD)			
Size	Document Number	Rev	
Custom	EA40 HW ULT	1	
Date	May 13, 2013	Sheet	22 of 102

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VINAFIX
SSID = PCH



71.HASWE.G0U

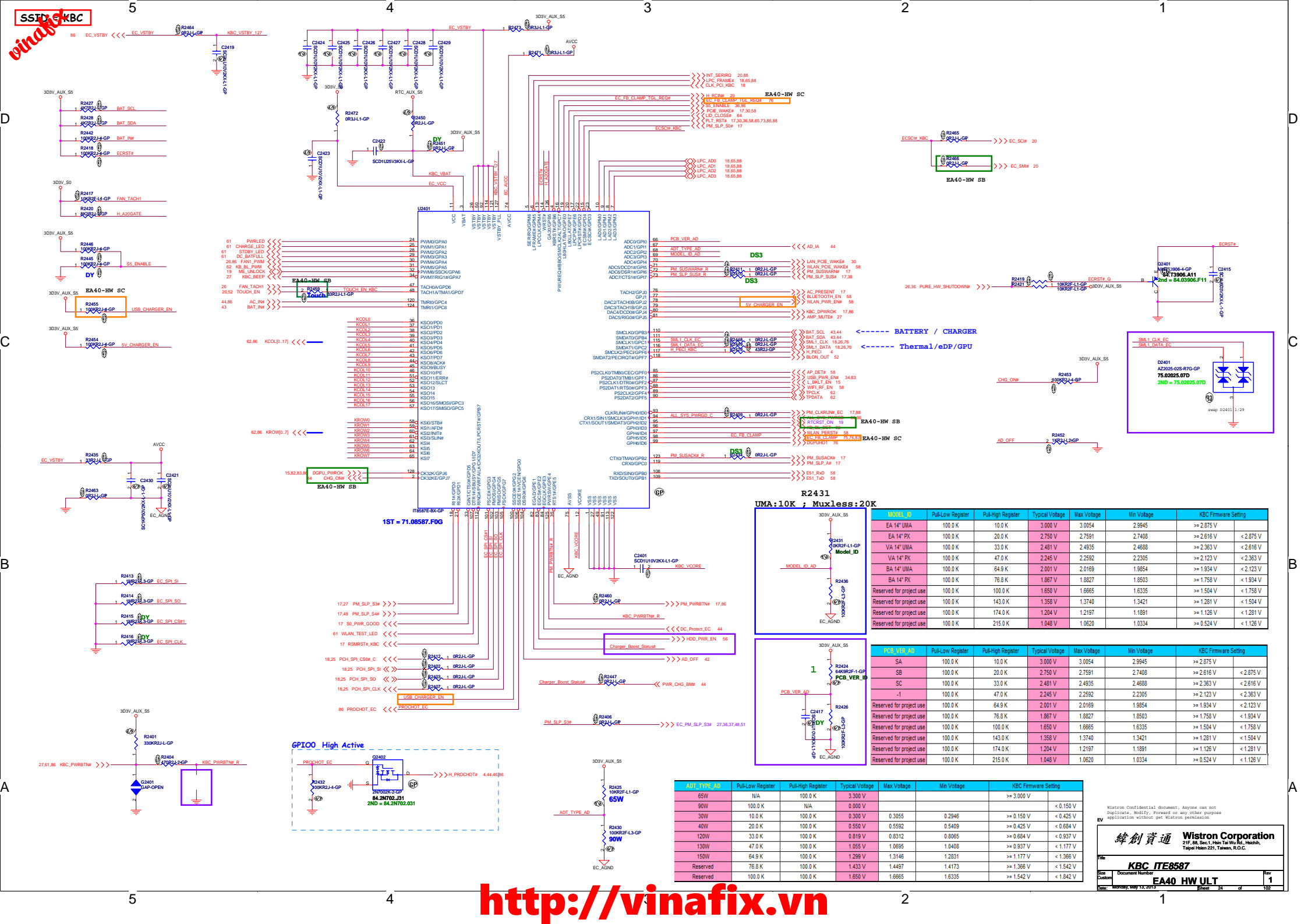


71.HASWE.G0U

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EV

Title	
CPU (VSS)	
Size	Document Number
Custom	EA40 HW ULT
Date:	Monday, May 13, 2013
Sheet	23 of 102
Rev	1



ADT_VTYP_AD	Pu-Low Register	Pu-High Register	Typical Voltage	Max Voltage	Min Voltage	KBC Firmware Setting
65W	N/A	100.0 K	3.300 V			>= 3.000 V
90W	100.0 K	N/A	0.000 V			< 0.150 V
30W	10.0 K	100.0 K	0.300 V	0.3055	0.2946	>= 0.150 V < 0.425 V
40W	20.0 K	100.0 K	0.550 V	0.5592	0.5409	>= 0.425 V < 0.684 V
120W	33.0 K	100.0 K	0.819 V	0.8065	0.8212	>= 0.684 V < 0.937 V
130W	47.0 K	100.0 K	1.055 V	1.0695	1.0408	>= 0.937 V < 1.177 V
150W	64.9 K	100.0 K	1.290 V	1.3146	1.2831	>= 1.177 V < 1.366 V
Reserved	76.8 K	100.0 K	1.433 V	1.4497	1.4173	>= 1.366 V < 1.542 V
Reserved	100.0 K	100.0 K	1.650 V	1.6665	1.6335	>= 1.542 V < 1.842 V

MODEL_ID	Pu-Low Register	Pu-High Register	Typical Voltage	Max Voltage	Min Voltage	KBC Firmware Setting
EA 14" UMA	100.0 K	10.0 K	3.000 V	3.0054	2.9945	>= 2.875 V
EA 14" FX	100.0 K	20.0 K	2.750 V	2.7591	2.7408	>= 2.616 V < 2.875 V
VA 14" UMA	100.0 K	33.0 K	2.481 V	2.4935	2.4688	>= 2.363 V < 2.616 V
VA 14" FX	100.0 K	47.0 K	2.245 V	2.2592	2.2305	>= 2.123 V < 2.363 V
BA 14" UMA	100.0 K	64.9 K	2.001 V	2.0169	1.9854	>= 1.934 V < 2.123 V
BA 14" FX	100.0 K	76.8 K	1.867 V	1.8827	1.8503	>= 1.758 V < 1.934 V
Reserved for project use	100.0 K	100.0 K	1.650 V	1.6665	1.6335	>= 1.504 V < 1.758 V
Reserved for project use	100.0 K	143.0 K	1.350 V	1.3740	1.3421	>= 1.281 V < 1.504 V
Reserved for project use	100.0 K	174.0 K	1.204 V	1.2197	1.1891	>= 1.126 V < 1.281 V
Reserved for project use	100.0 K	215.0 K	1.048 V	1.0620	1.0334	>= 0.924 V < 1.126 V

PCB_VER_AD	Pu-Low Register	Pu-High Register	Typical Voltage	Max Voltage	Min Voltage	KBC Firmware Setting
SA	100.0 K	10.0 K	3.000 V	3.0054	2.9945	>= 2.875 V
SB	100.0 K	20.0 K	2.750 V	2.7591	2.7408	>= 2.616 V < 2.875 V
SC	100.0 K	33.0 K	2.481 V	2.4935	2.4688	>= 2.363 V < 2.616 V
SC	100.0 K	33.0 K	2.481 V	2.4935	2.4688	>= 2.363 V < 2.616 V
-1	100.0 K	47.0 K	2.245 V	2.2592	2.2305	>= 2.123 V < 2.363 V
Reserved for project use	100.0 K	64.9 K	2.001 V	2.0169	1.9854	>= 1.934 V < 2.123 V
Reserved for project use	100.0 K	76.8 K	1.867 V	1.8827	1.8503	>= 1.758 V < 1.934 V
Reserved for project use	100.0 K	100.0 K	1.650 V	1.6665	1.6335	>= 1.504 V < 1.758 V
Reserved for project use	100.0 K	143.0 K	1.350 V	1.3740	1.3421	>= 1.281 V < 1.504 V
Reserved for project use	100.0 K	174.0 K	1.204 V	1.2197	1.1891	>= 1.126 V < 1.281 V
Reserved for project use	100.0 K	215.0 K	1.048 V	1.0620	1.0334	>= 0.924 V < 1.126 V

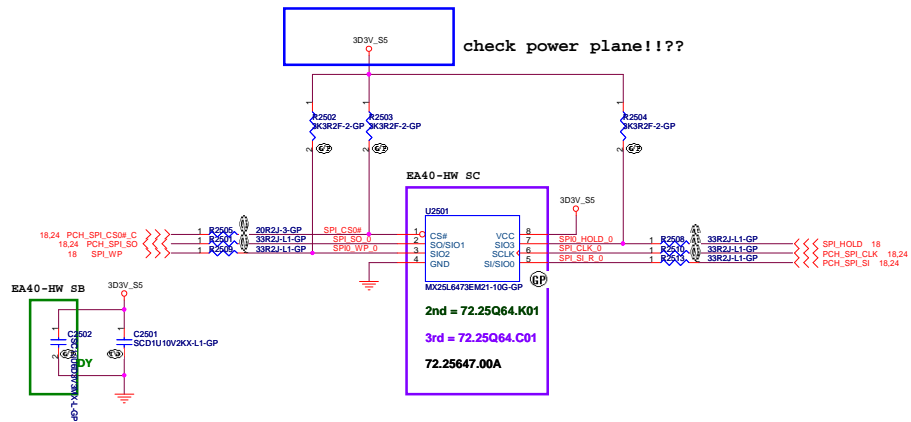
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File: **KBC ITE8587**
Doc Number: **EA40 HW ULT**
Rev: **1**
Date: **Monday, May 16, 2016** Sheet **24** of **102**

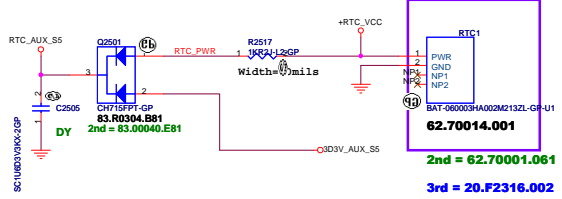
SST49 Flash.ROM SPI FLASH ROM (8M byte) for PCH

SPI ROM Equal length need to less than 500mil



check power plane!!??

SSID = RBAT



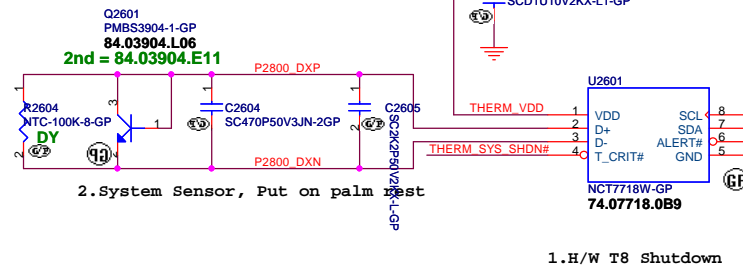
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<p>緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsiehsh, Taipei Hsien 221, Taiwan, R.O.C.</p>	
<p>Flash(KBC+PCH)/RTC</p>	
<p>Size: 42</p>	<p>Document Number: EA40 HW ULT</p>
<p>Date: Monday, May 13, 2013</p>	<p>Rev: 1</p>

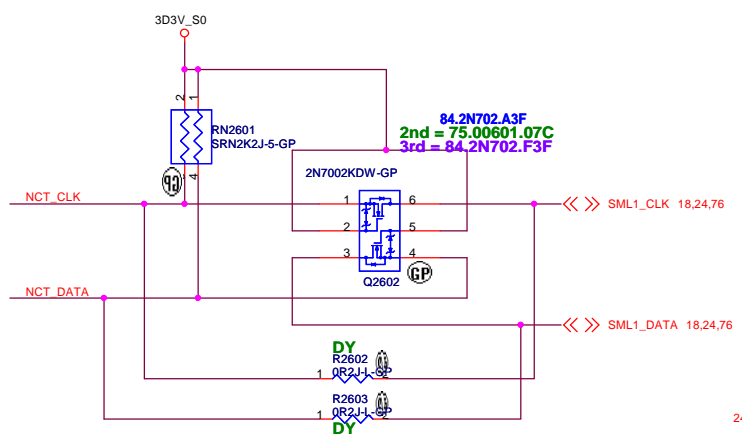
SID = Thermal

Thermal sensor NCT 7718W

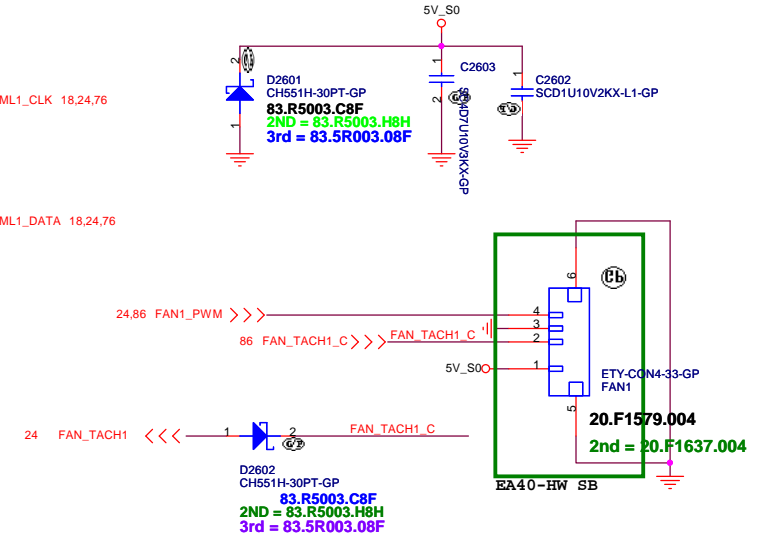
Layout notice :
Both DXN and DXP routing 10 mil trace width and 10 mil spacing.



1.H/W T8 Shutdown



Layout 15 mil

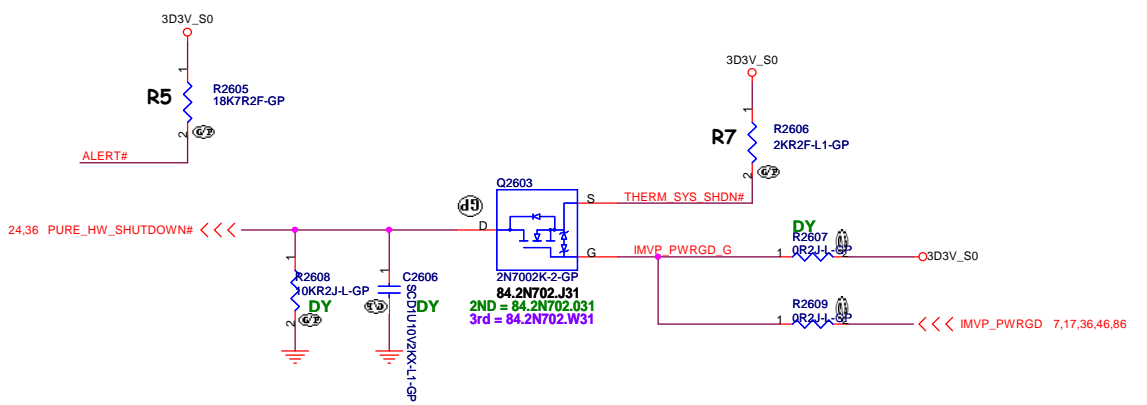


ALERT# /T CRIT#
Pull-up Resistor

R5	77°C	87°C	97°C	107°C	117°C
2Kohm	77°C	87°C	97°C	107°C	117°C
7.5Kohm	79°C	89°C	99°C	109°C	119°C
10.5Kohm	81°C	91°C	101°C	111°C	121°C
14Kohm	83°C	93°C	103°C	113°C	123°C
18.7Kohm	85°C	95°C	105°C	115°C	125°C

T_CRIT temperature strapping point

T8=85 degree



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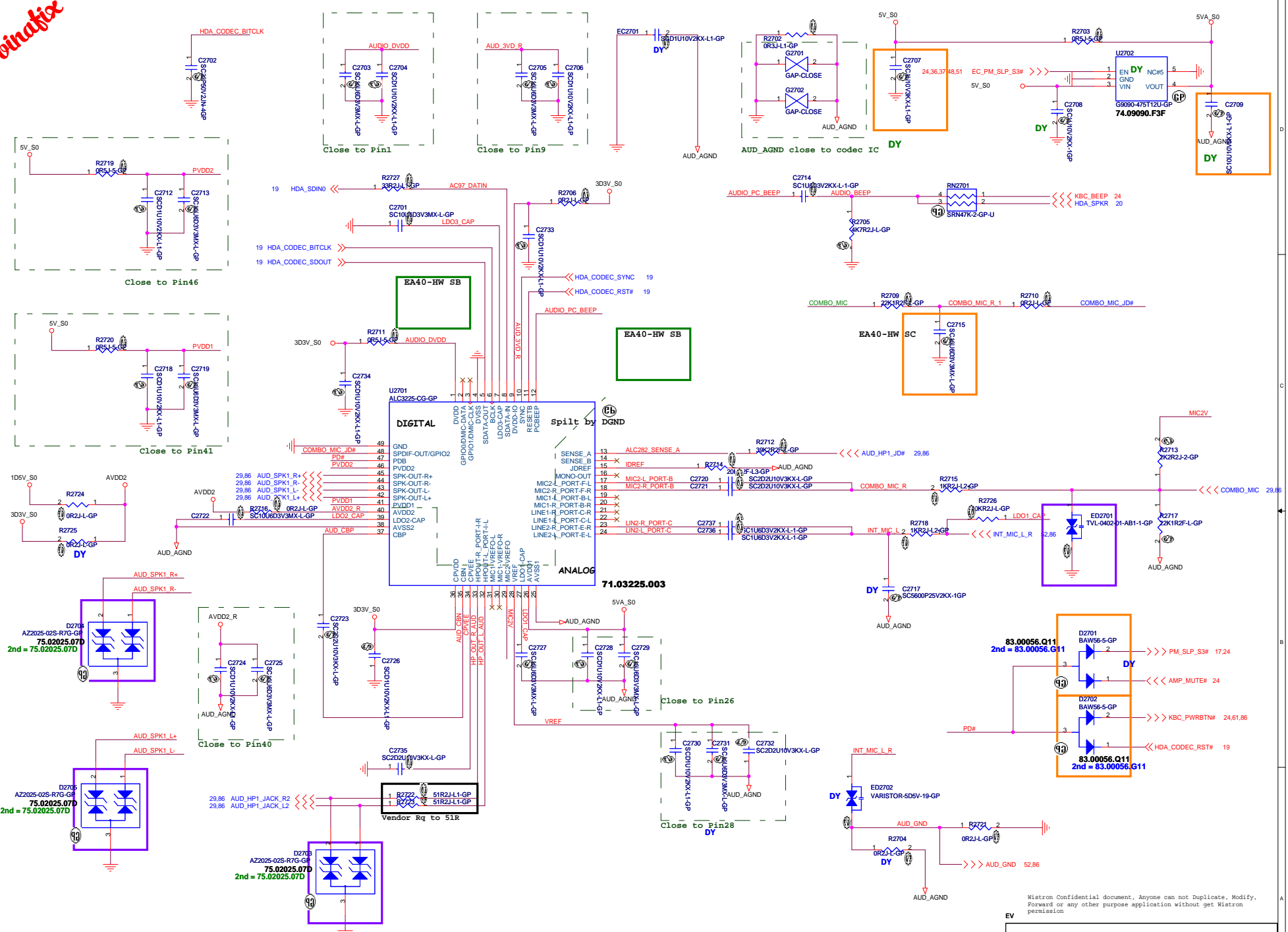
Title: Thermal 7718/Fan Controller P2793

Size A3 Document Number EA40 HW ULT Rev 1

Date: Monday, May 13, 2013 Sheet 26 of 102

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Audio Codec ALC3225	
Title	Rev
EA40 HW ULT	
Size	Document Number
Custom	EA40 HW ULT
Date: Monday, May 13, 2013	Sheet 27 of 102

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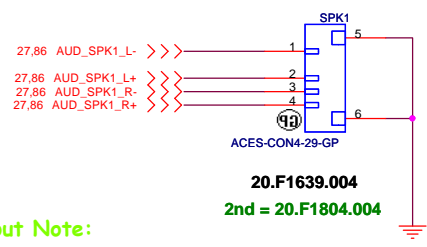
緯創資通 **Wistron Corporation**
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Taipei Hsien 221, Taiwan, R.O.C.

Title		
Audio AMP 1001		
Size	Document Number	Rev
A4	EA40 HW ULT	1
Date:	Monday, May 13, 2013	Sheet 28 of 102

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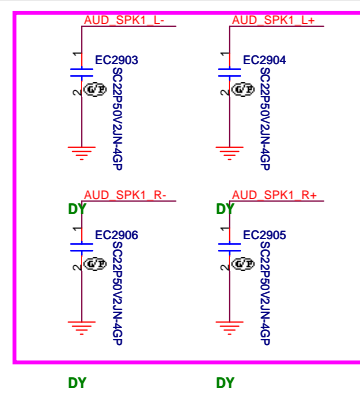
SPK1 = AUDIO

Speaker

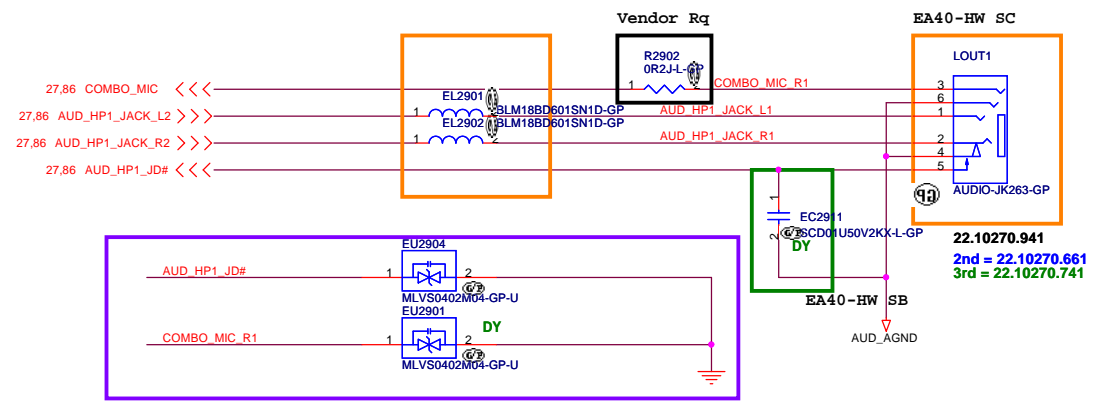


Layout Note:

Trace width=40mil



Combo Jack



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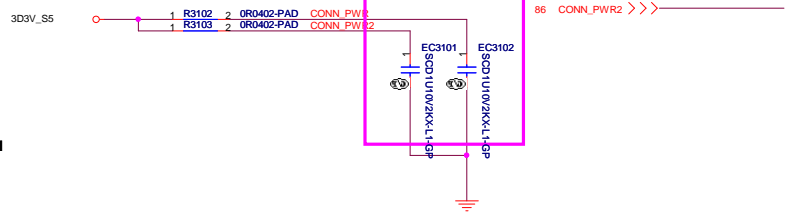
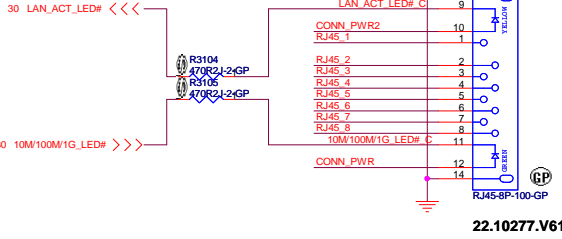
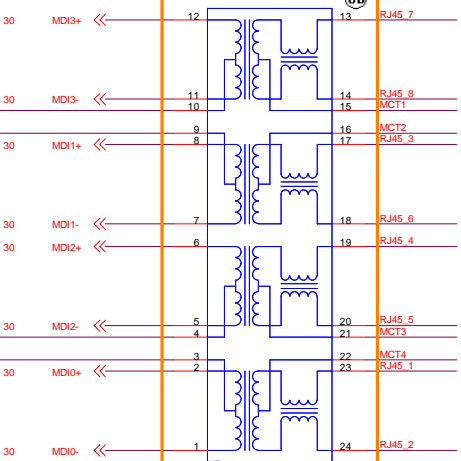
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Size	Document Number	Date	Rev
Custom	EA40 HW ULT	Monday, May 13, 2013	1
Date:		Monday, May 13, 2013	Sheet 29 of 102

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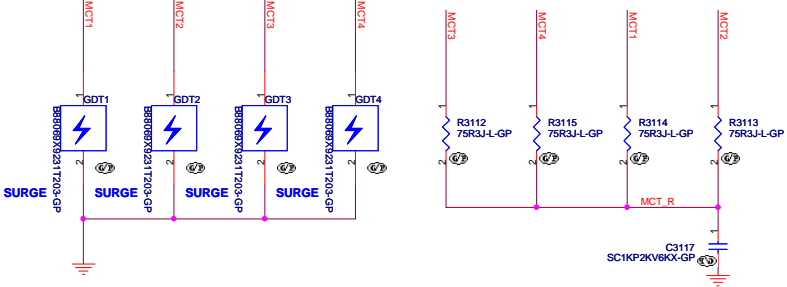
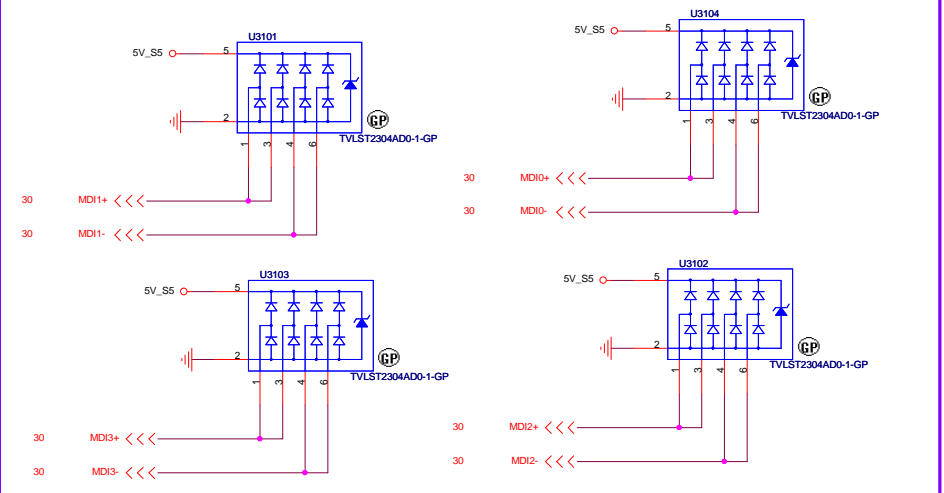
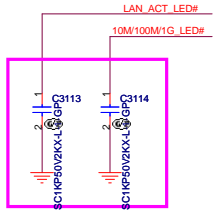
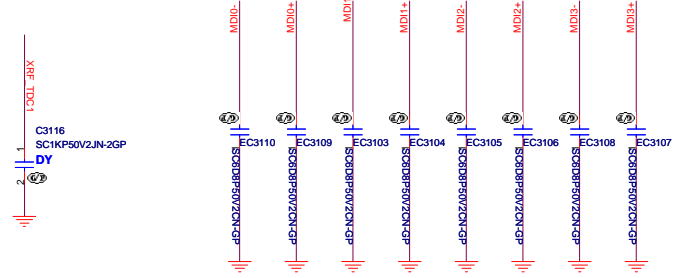
Source = LAN

EA40-HW SC

3rd = 68.00069.30A
2nd = 68.1H115.30A
68.63241.301
XF0RM-270-GP-U



- 86 RJ45_1 >>>
- 86 RJ45_2 >>>
- 86 RJ45_3 >>>
- 86 RJ45_4 >>>
- 86 RJ45_5 >>>
- 86 RJ45_6 >>>
- 86 RJ45_7 >>>
- 86 RJ45_8 >>>
- 86 LAN_ACT_LED# C >>>
- 86 10M/100M/1G_LED# C >>>
- 86 CONN_PWR >>>
- 86 CONN_PWR2 >>>



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(LAN+VGA) CONNECTOR		
Title		
Size	Document Number	Rev
Custom	EA40 HW ULT	1
Date:	Monday, May 13, 2013	Sheet 31 of 102

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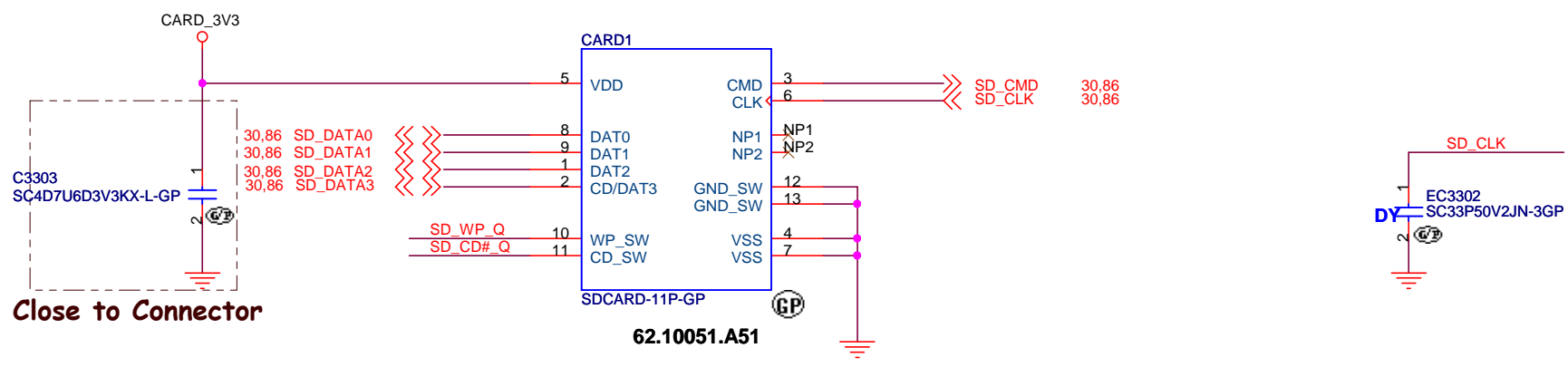
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RTS5229(CARD READER)		
Size A4	Document Number EA40 HW ULT	Rev 1
Date: Monday, May 13, 2013	Sheet 32 of	102

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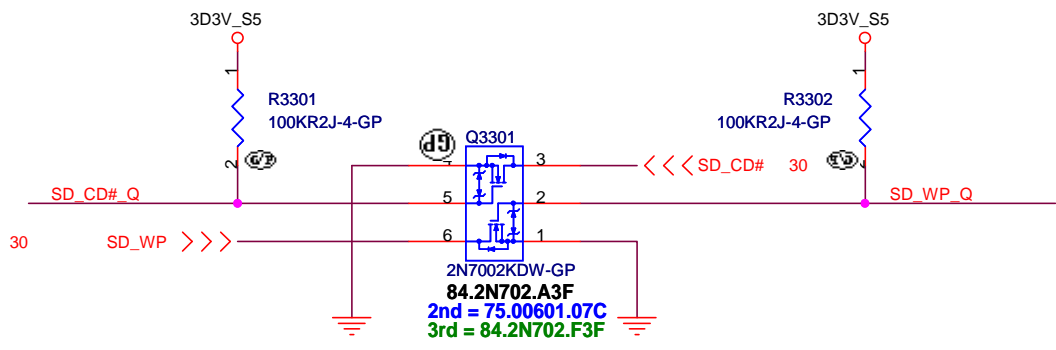
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SSID = SDIO

SD//MS Card Reader



Close to Connector



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Title			
CARD Reader CONN			
Size	Document Number	Rev	
Custom	EA40_HW_ULT	1	
Date:	Monday, May 13, 2013	Sheet	33 of 102

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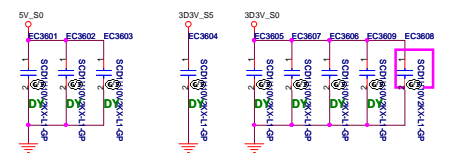
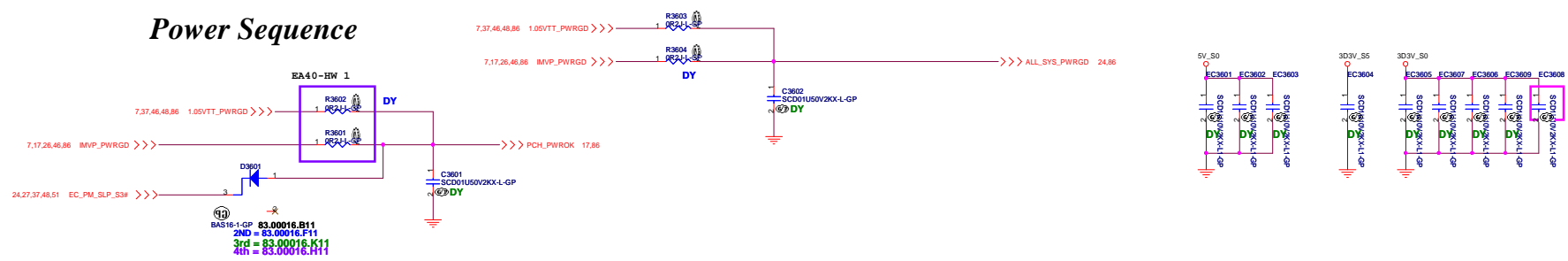
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Taipei Hsien 221, Taiwan, R.O.C.

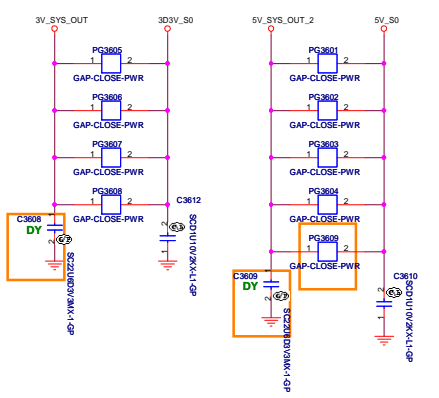
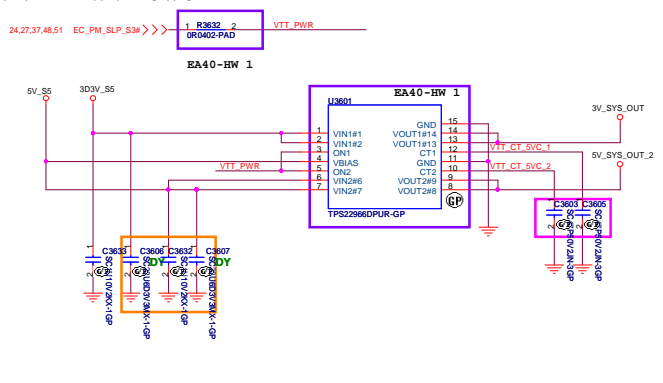
Title		
USB CHARGER		
Size A4	Document Number EA40 HW ULT	Rev 1
Date: Monday, May 13, 2013	Sheet 35	of 102

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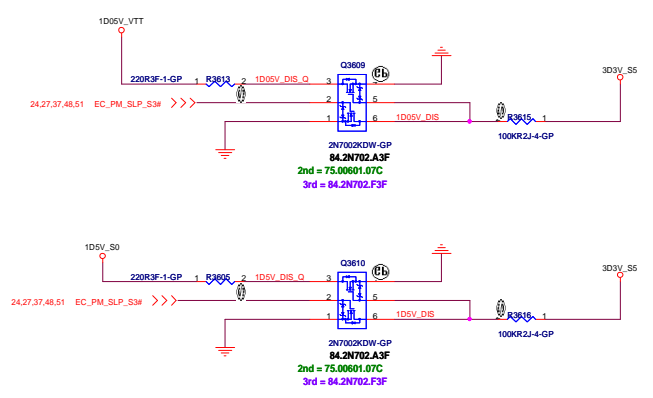
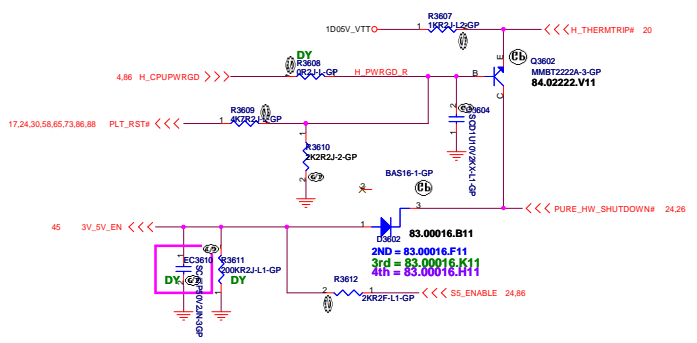
Power Sequence



ANNIE Run Power

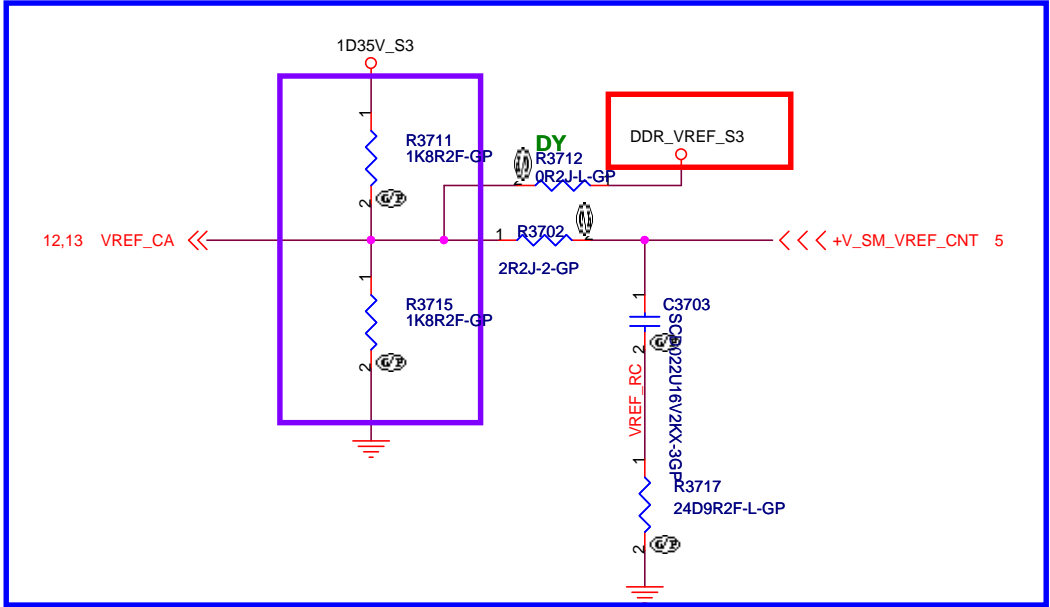
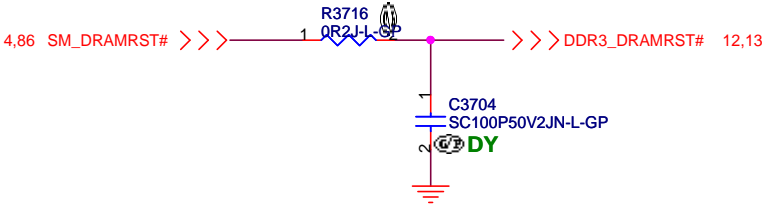


Discharge circuit



DY 3D3V_S0 discharge circuit

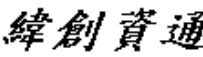
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For Intel Recommend Close to DIMM

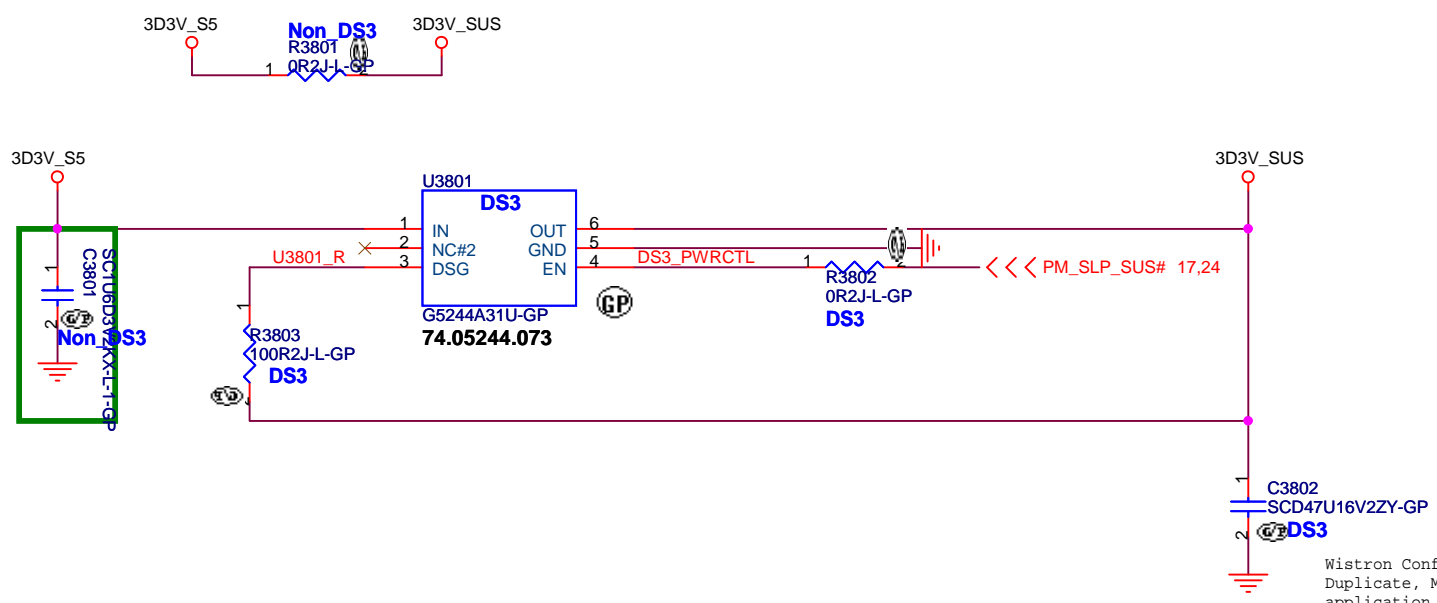
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Title ADAPTER OCP / S3 reduction		
Size Custom	Document Number EA40 HW ULT	Rev 1
Sheet 37 of		102

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Title			
DS3			
Size A4	Document Number EA40 HW ULT	Rev 1	
Date: Monday, May 13, 2013	Sheet 38	of	102

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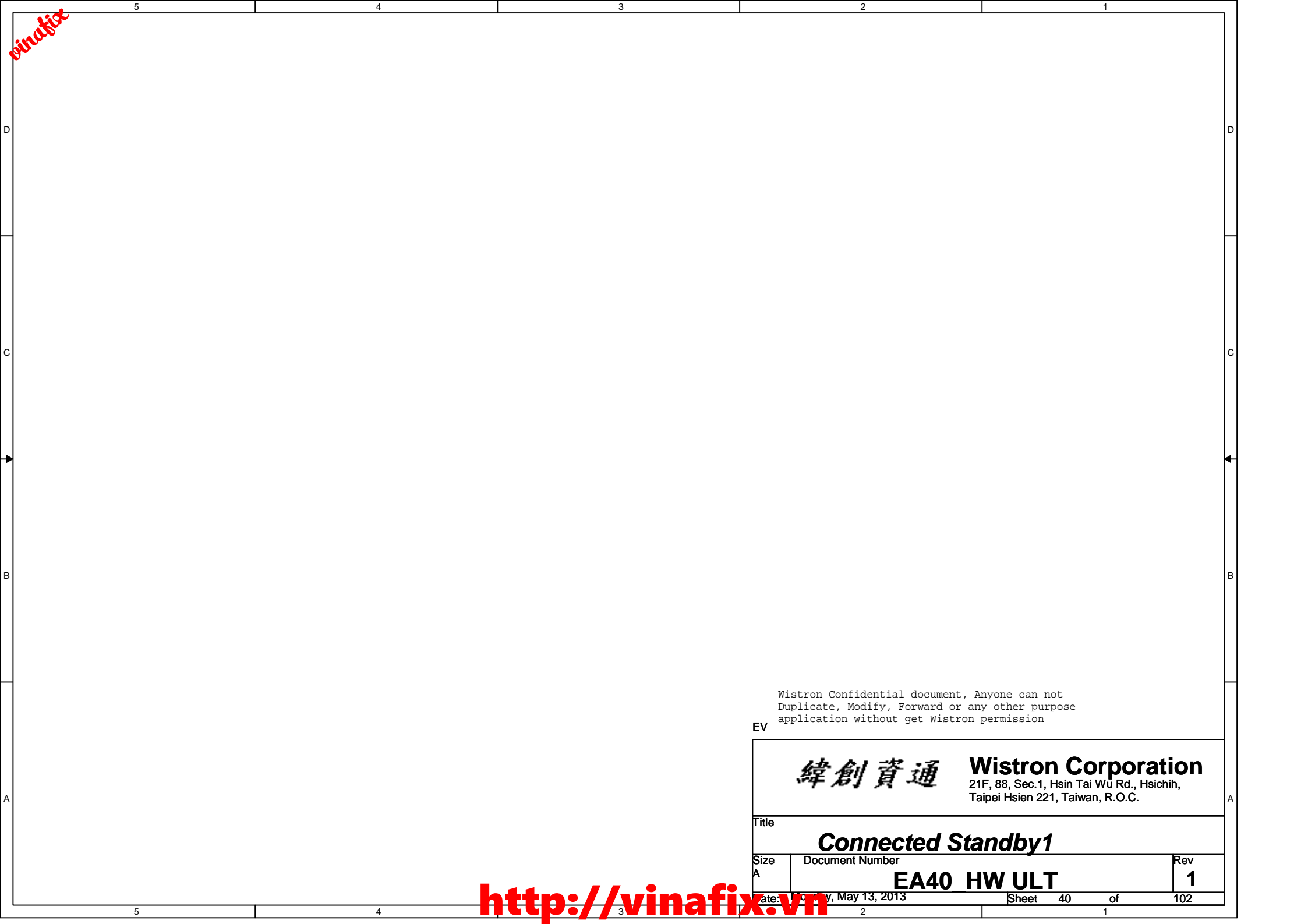
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Power Sequence

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		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
1D05 M			
Size	Document Number	Rev	
Custom	EA40 HW ULT	1	
Date:	Monday, May 13, 2013	Sheet	39 of 102

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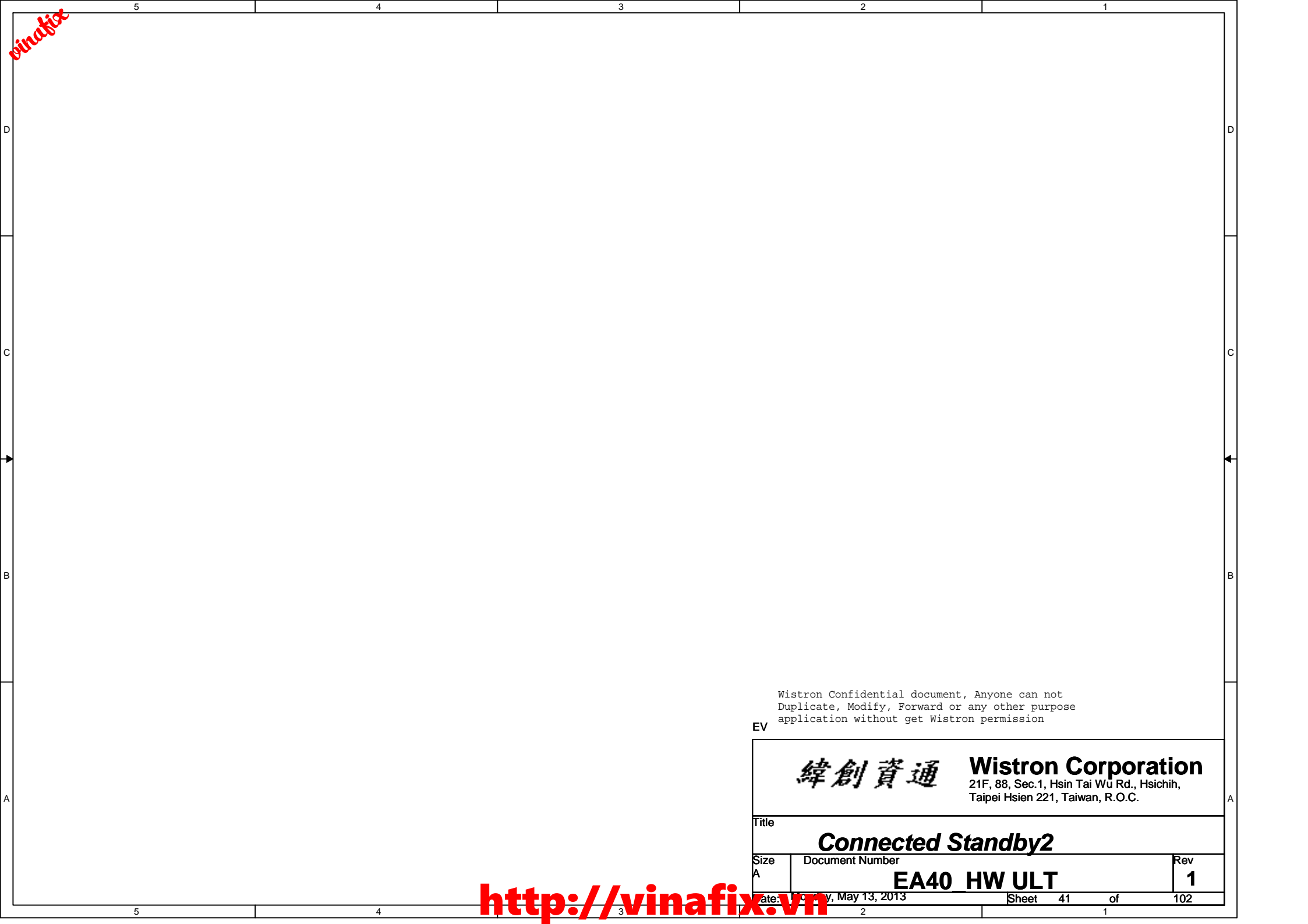
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Title			
Connected Standby1			
Size	Document Number		Rev
A	EA40 HW ULT		1
Date: May, May 13, 2013		Sheet 40	of 102

<http://vinafix.vn>



vinafix

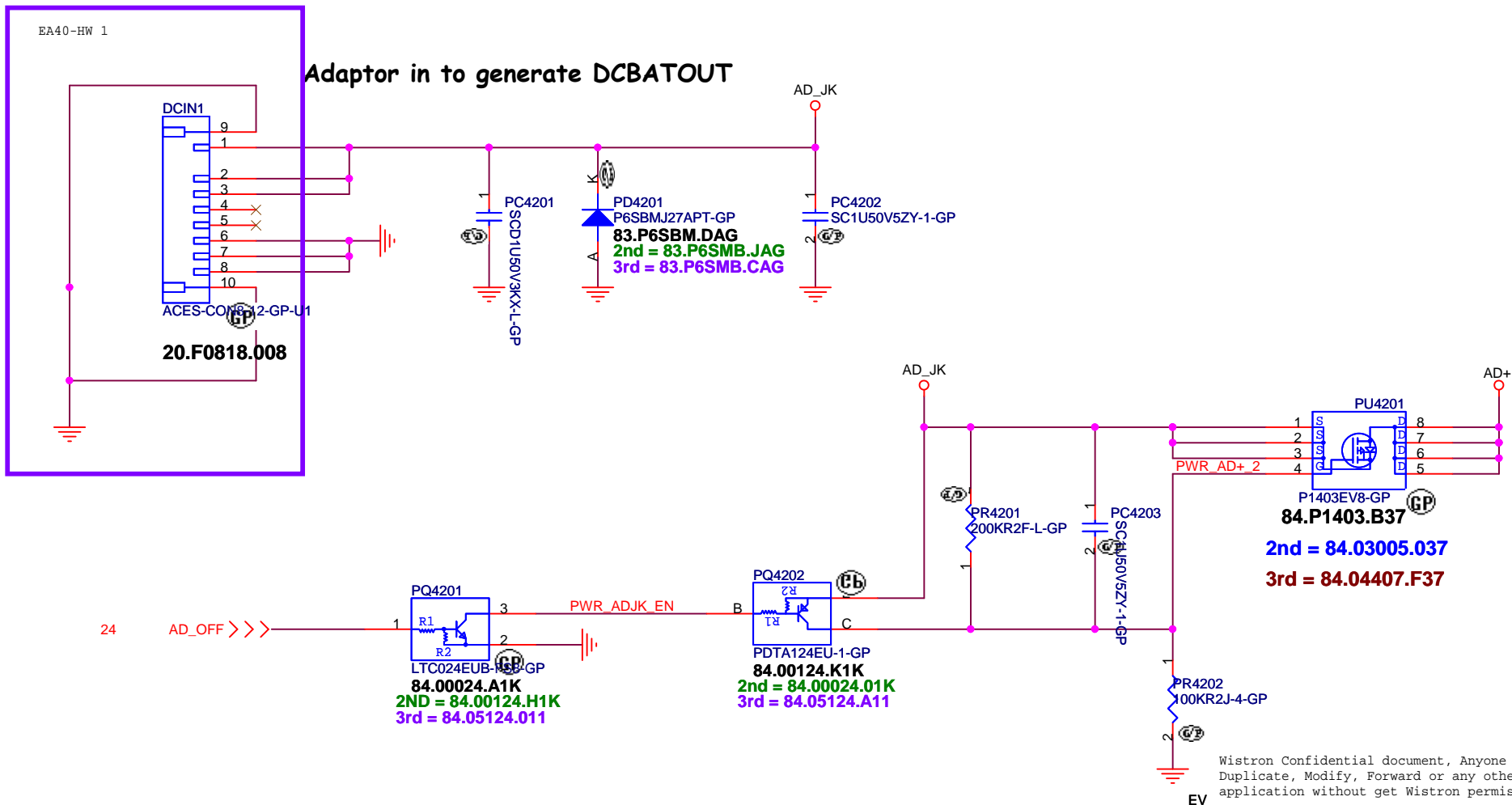
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緯創資通		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
Connected Standby2			
Size	Document Number		Rev
A	EA40 HW ULT		1
Date: May 13, 2013		Sheet 41	of 102

<http://vinafix.vn>

ANNIE solution



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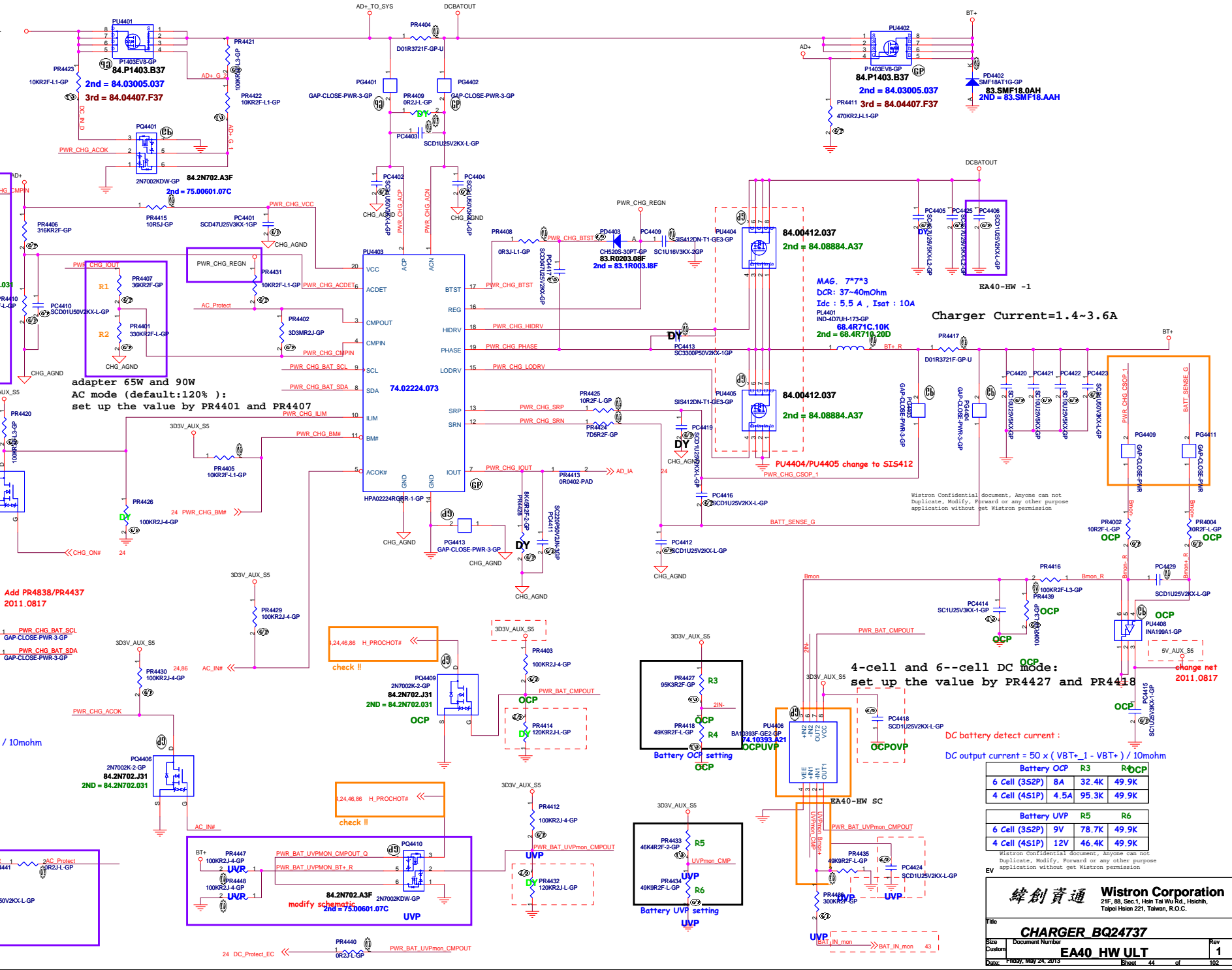
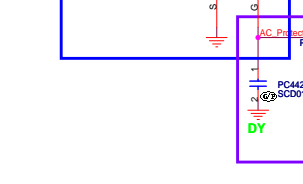
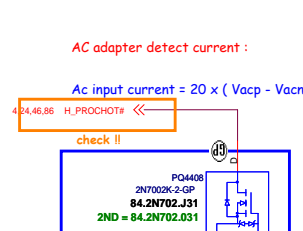
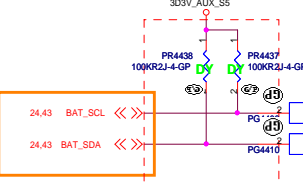
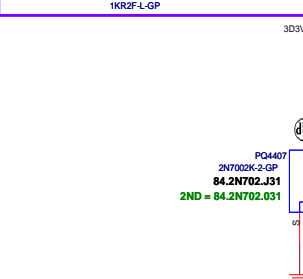
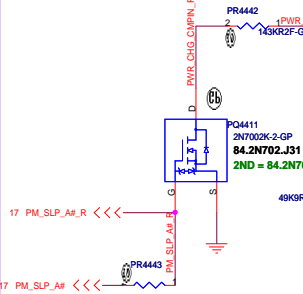
緯創資通		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
DCIN JACK			
Size A4	Document Number EA40 HW ULT		Rev 1
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SS14 = Charger

vinafix

AD+ total power	R1	R2
65w	36K	100K
90w	90K9	100K

change the table



adapter 65w and 90w
AC mode (default:120%):
set up the value by PR4401 and PR4407

MAG. 7*7*3
DCR: 37-40mOhm
I_{dc}: 5.5 A , I_{sat}: 10A
Charger Current=1.4~3.6A

4-cell and 6--cell DC mode:
set up the value by PR4427 and PR4418

Battery OCP	R3	R6CP
6 Cell (3S2P)	8A	32.4K 49.9K
4 Cell (4S1P)	4.5A	95.3K 49.9K

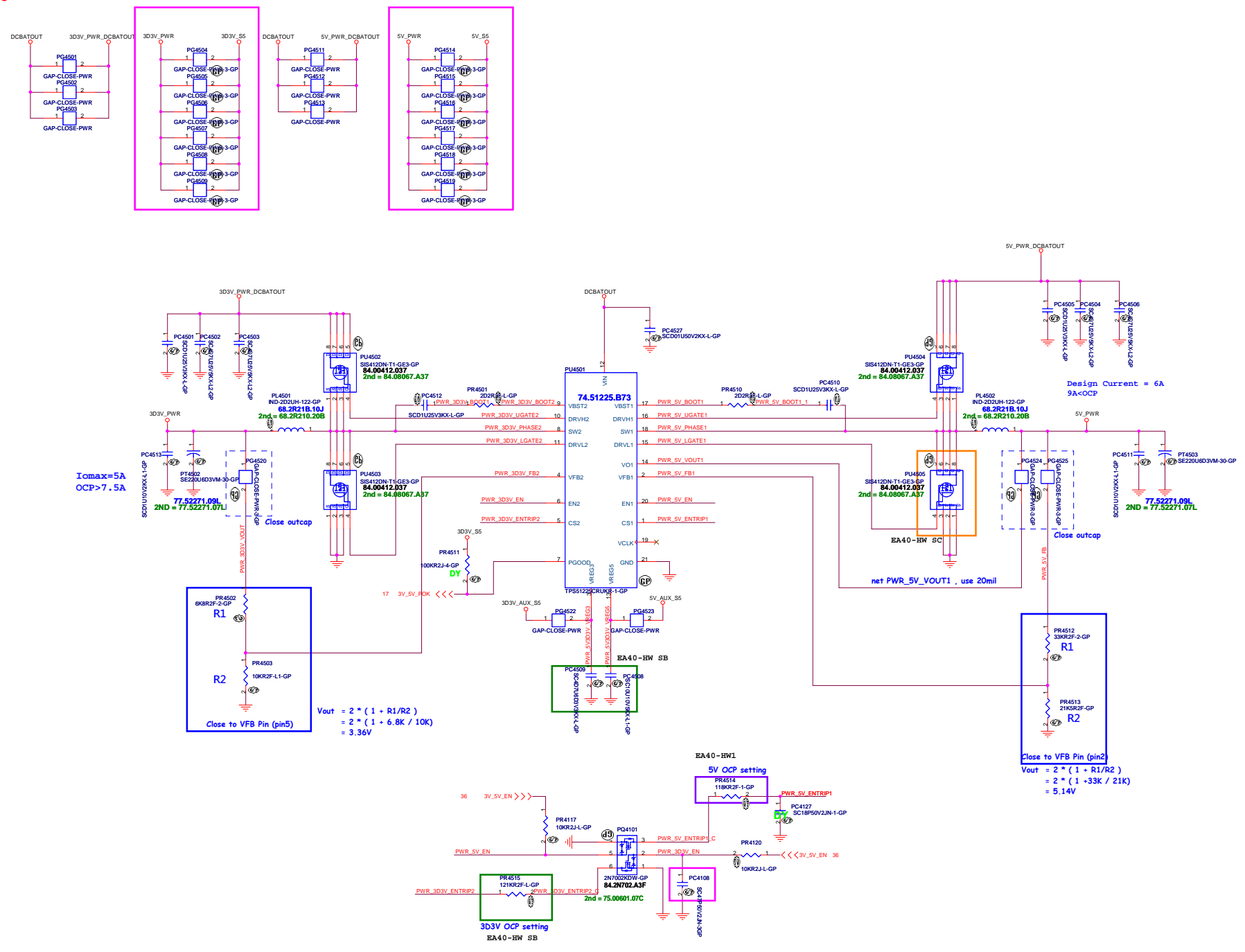
Battery UVP	R5	R6
6 Cell (3S2P)	9V	78.7K 49.9K
4 Cell (4S1P)	12V	46.4K 49.9K

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CHARGER BQ24737		Rev
File	Document Number	1
Size	Custom	
EA40 HW ULT		
Date: Friday, May 24, 2013	Sheet: 44	of 102

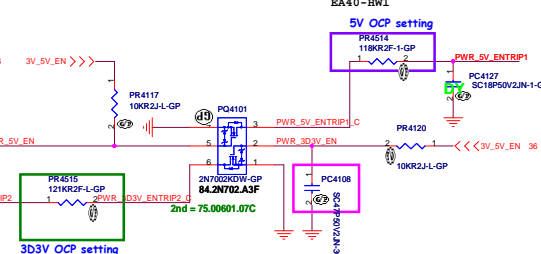
vinafix

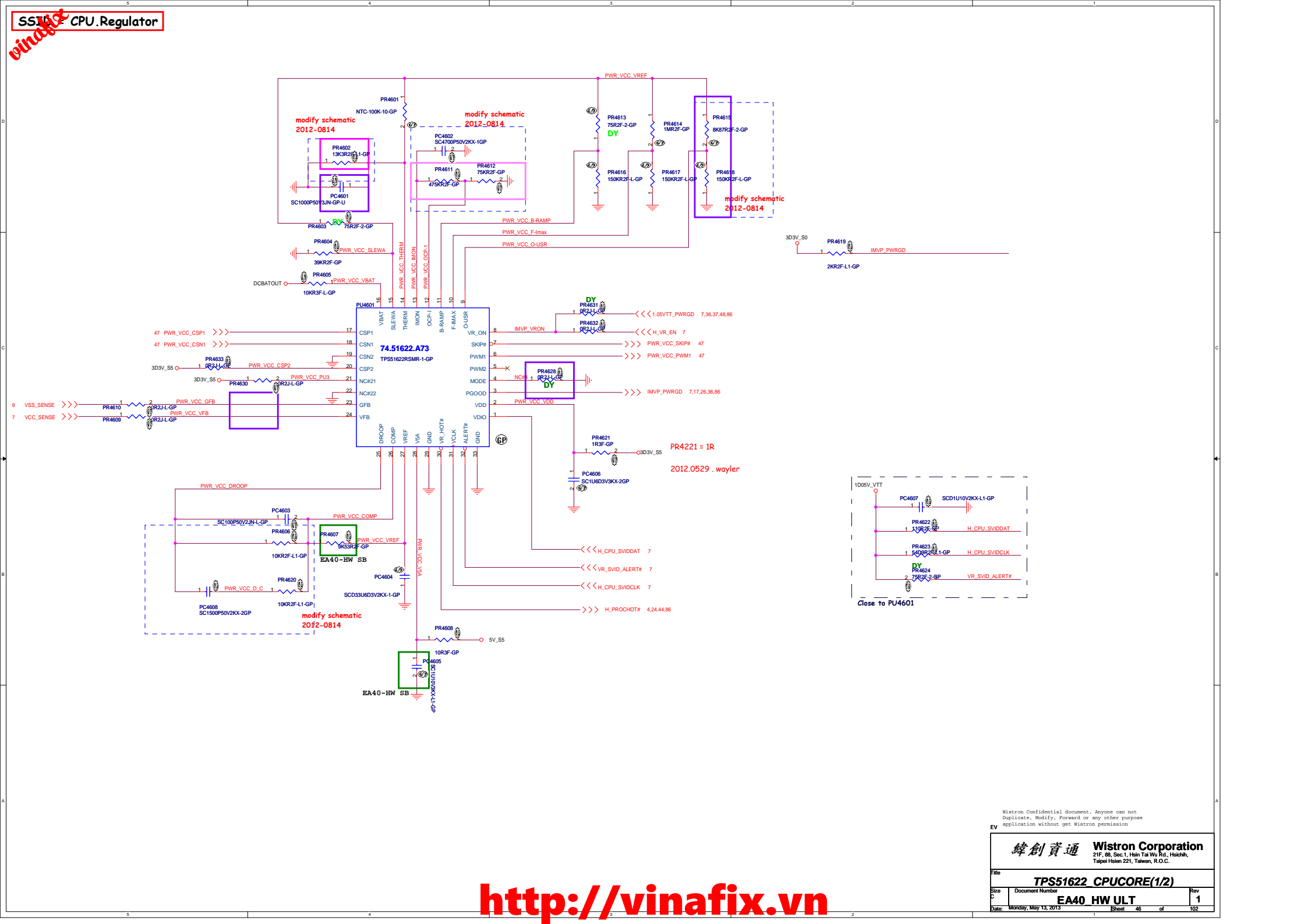


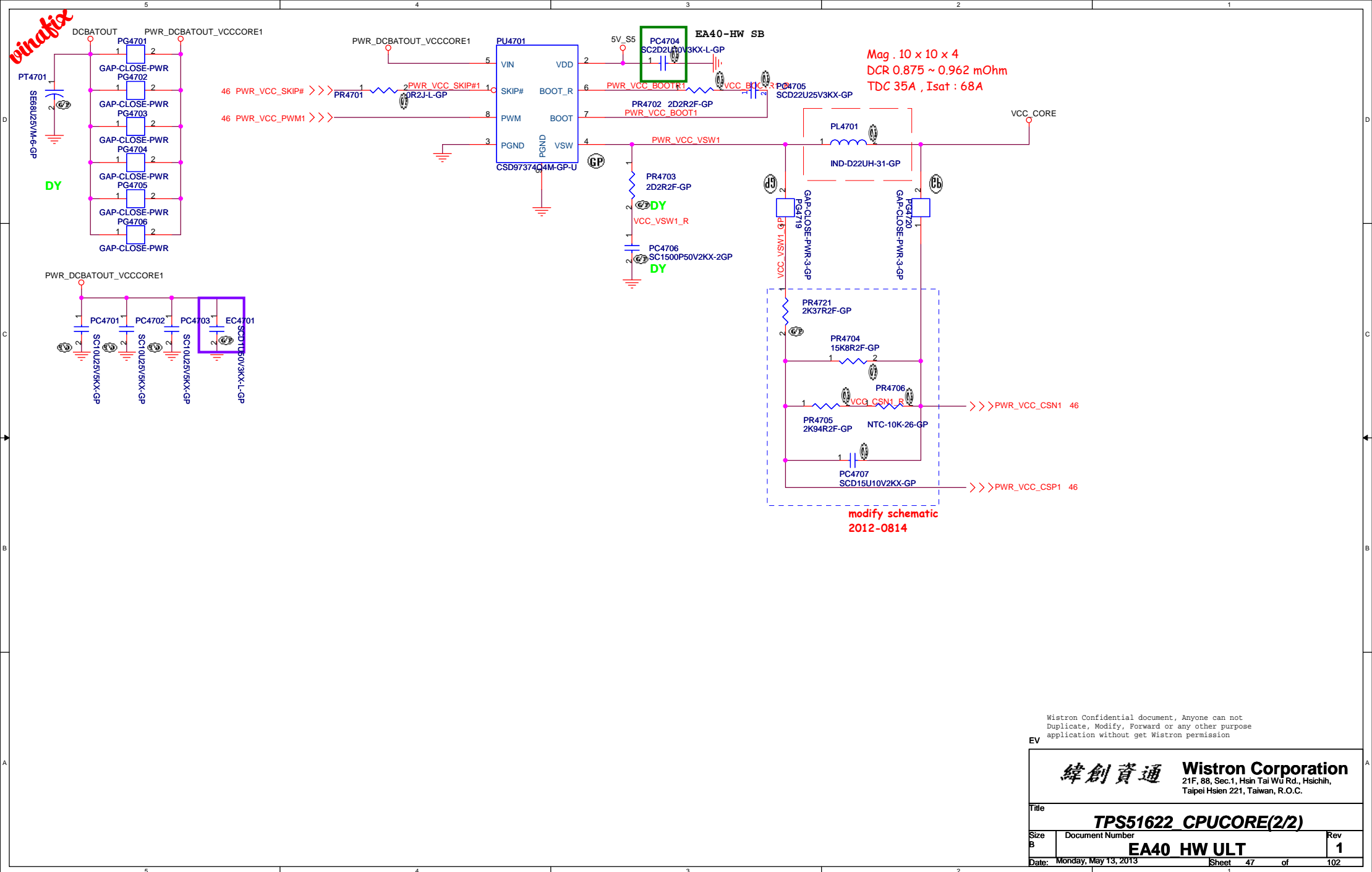
Iomax=5A
OCP>7.5A

$$V_{out} = 2 * (1 + R1/R2) = 2 * (1 + 6.8K / 10K) = 3.36V$$

$$V_{out} = 2 * (1 + R1/R2) = 2 * (1 + 33K / 21K) = 5.14V$$



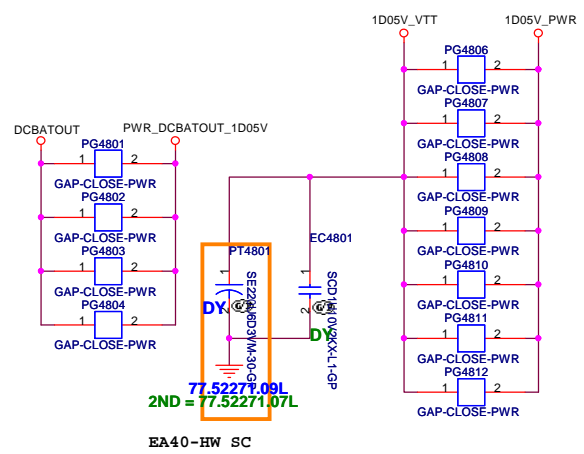




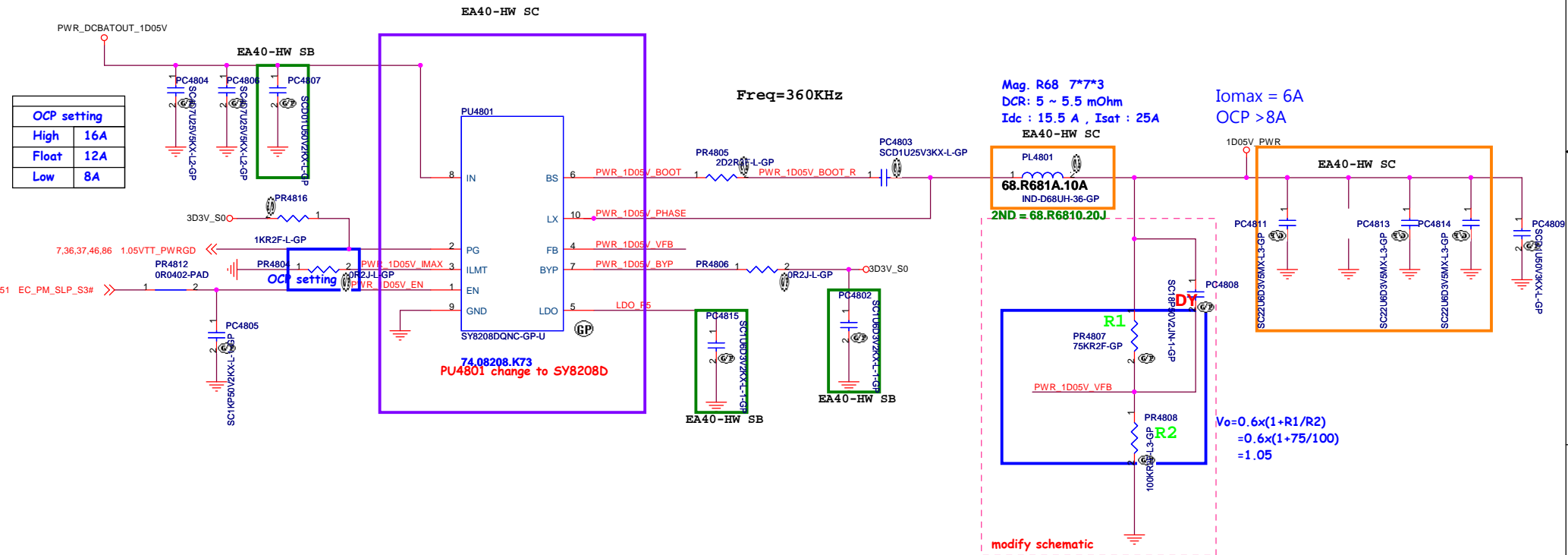
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Title			
TPS51622 CPU CORE(2/2)			
Size	Document Number		Rev
B	EA40 HW ULT		1
Date:	Monday, May 13, 2013	Sheet	47 of 102

SY8208D for 1D05V



EA40-HW SC

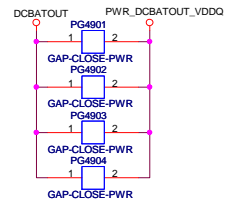


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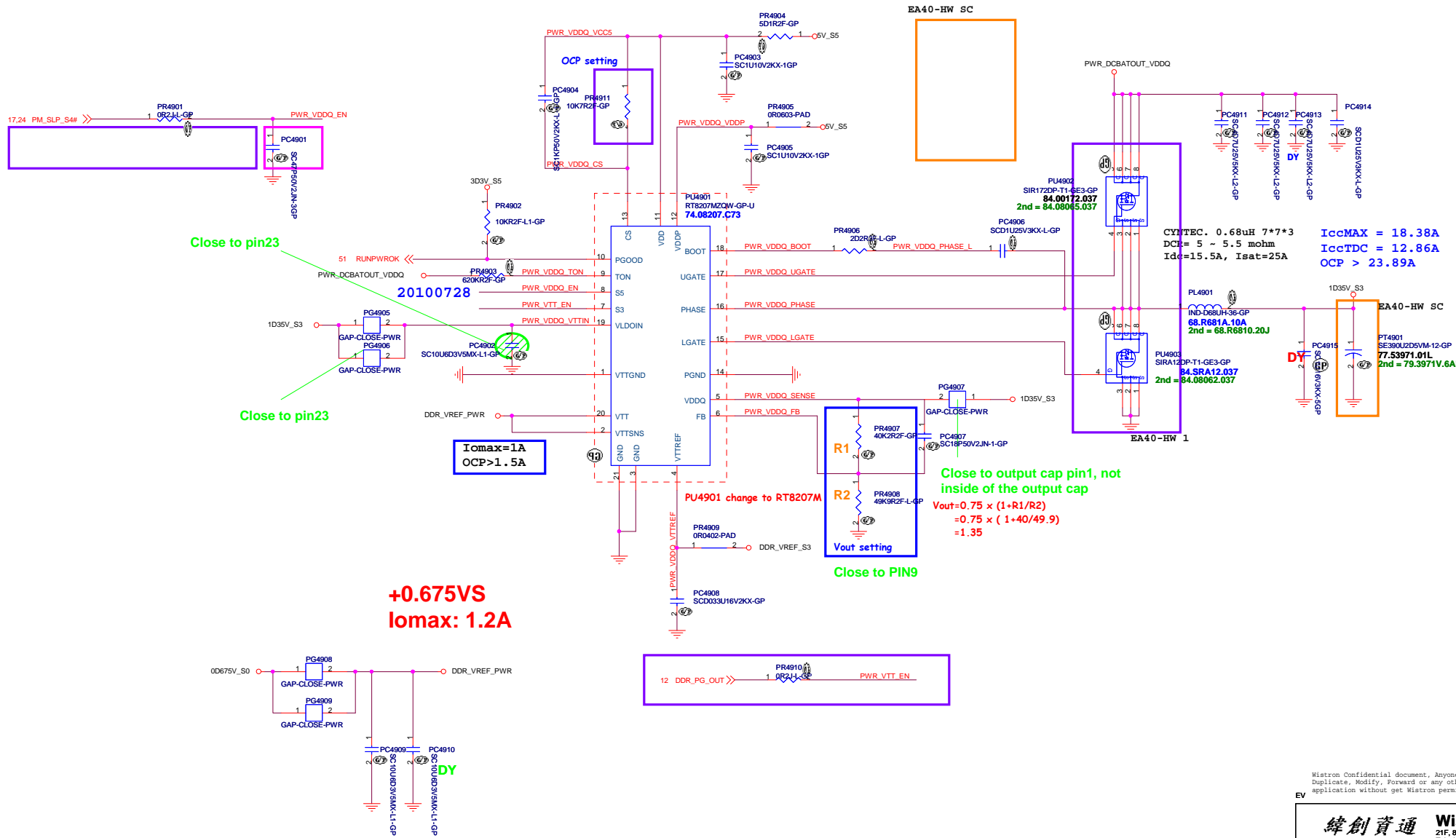
EV

緯創資通 Wistron Corporation	
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
DC to DC 1D05V(SY8208D)	
Title	Rev
Size A3	Document Number
EA40 HW ULT	
Date: Friday, May 24, 2013	Sheet 48 of 102

SSID = PWR.Plane.Regulator_lp2v0p6v



RT8207L for VDDQ



Close to pin23

Close to pin23

Iomax=1A
OCP>1.5A

+0.675VS
Iomax: 1.2A

Close to output cap pin1, not inside of the output cap

$$V_{out} = 0.75 \times (1 + R1/R2) = 0.75 \times (1 + 40/49.9) = 1.35$$

CYRTEC. 0.68uH 7*7*3
DCR = 5 - 5.5 mohm
Ide = 15.5A, Isat = 25A
IccMAX = 18.38A
IccTDC = 12.86A
OCP > 23.89A

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<p>緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</p>		
Title	RT8207(VDDQ VTT)	
Size	Document Number	Rev
Custom	EA40_HW_UL	1
Date: Monday, May 13, 2013	Sheet 49 of	102

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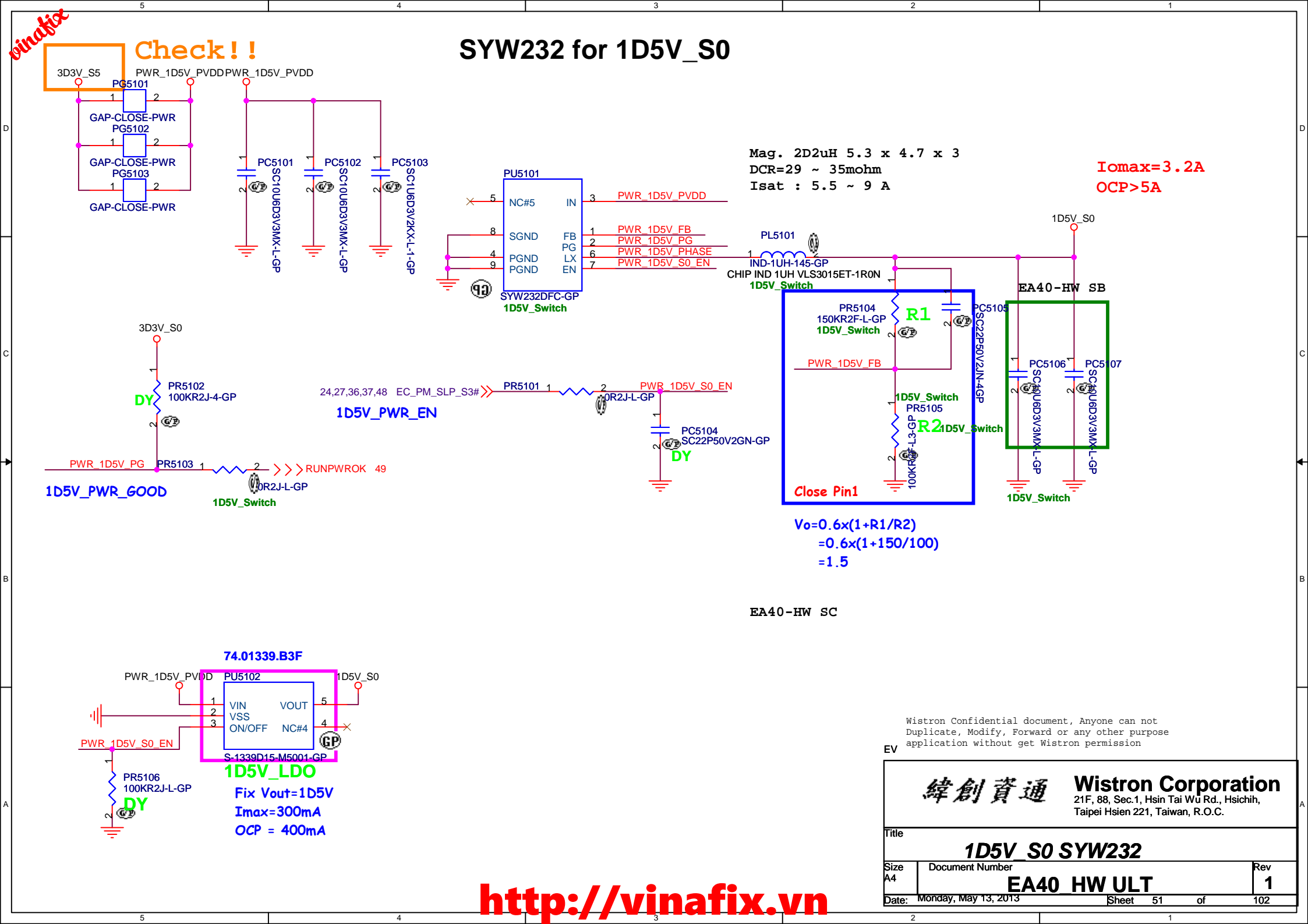
SYW232 for 1D8V_S0

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EV

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Title			
1D8V_S0 SYW232			
Size	Document Number		Rev
A4	EA40 HW ULT		1
Date:	Monday, May 13, 2013	Sheet 50	of 102

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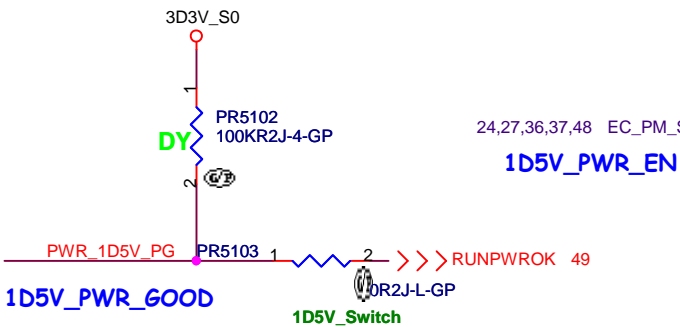
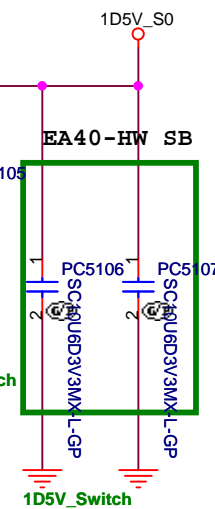
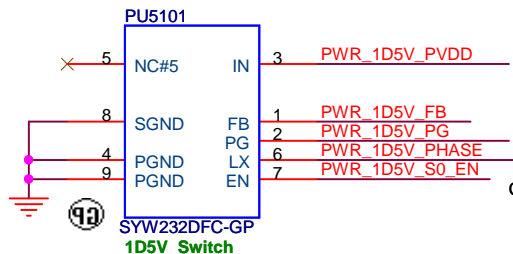
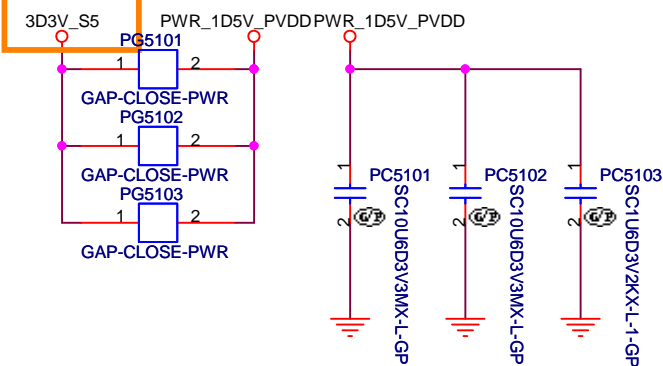


SYW232 for 1D5V_S0

Check!!

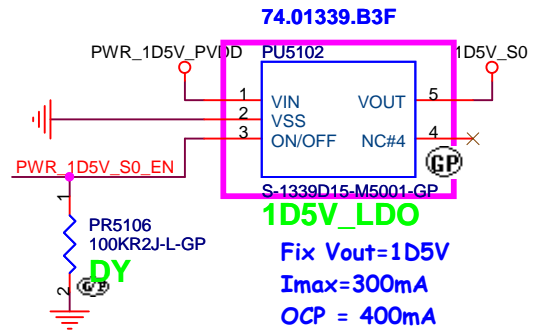
Mag. 2D2uH 5.3 x 4.7 x 3
 DCR=29 ~ 35mohm
 Isat : 5.5 ~ 9 A

Iomax=3.2A
OCP>5A



$$V_o = 0.6 \times (1 + R1/R2) = 0.6 \times (1 + 150/100) = 1.5$$

EA40-HW SC



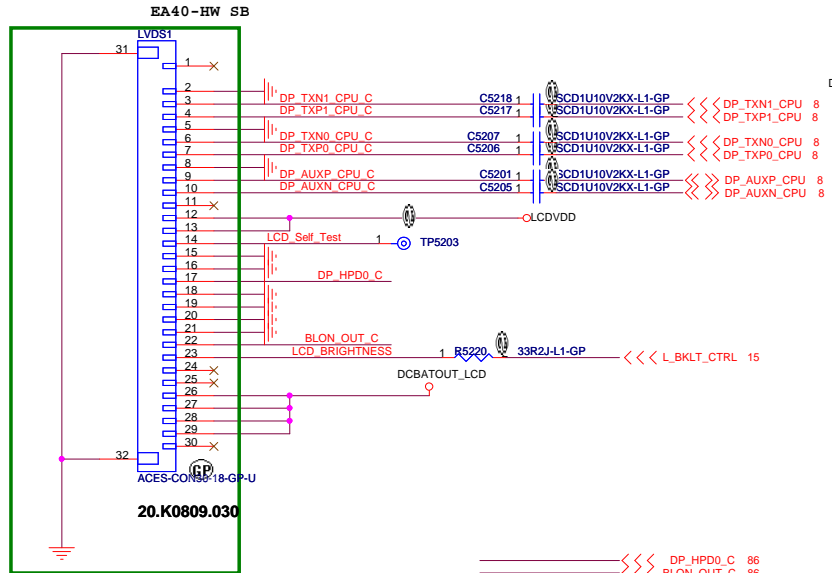
Fix Vout=1D5V
I_{max}=300mA
OCP = 400mA

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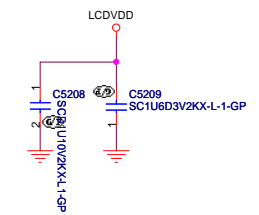
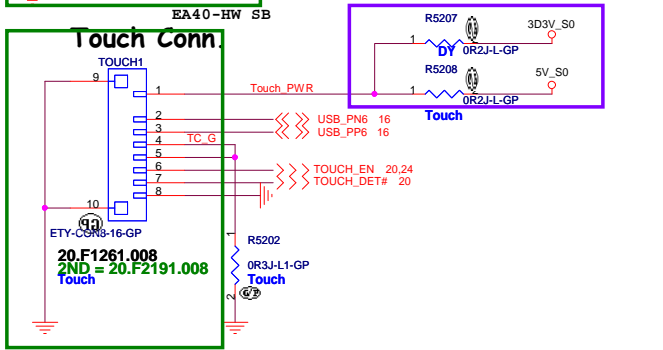
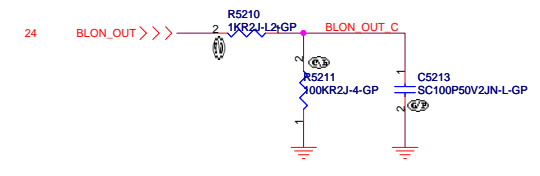
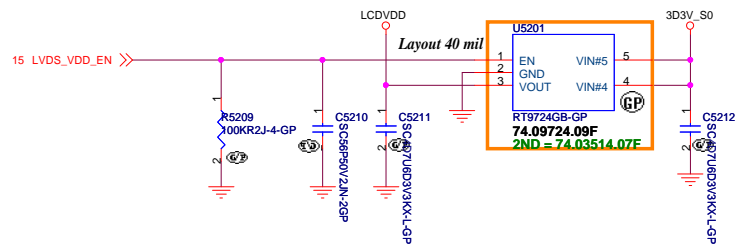
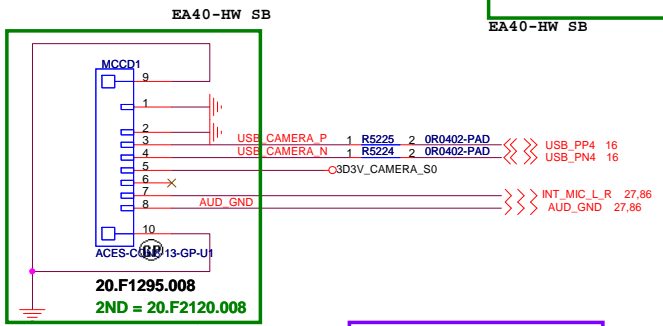
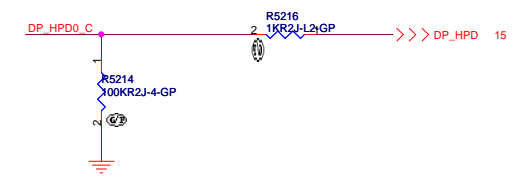
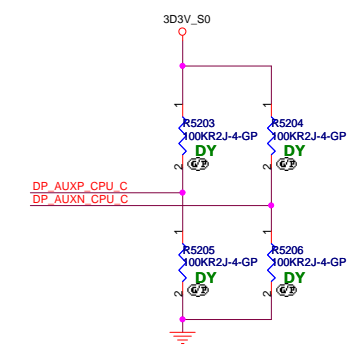
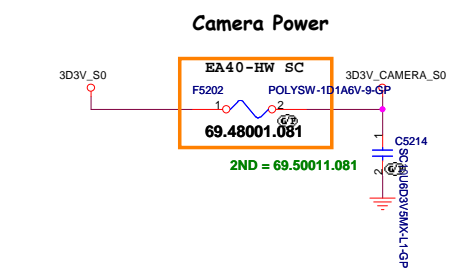
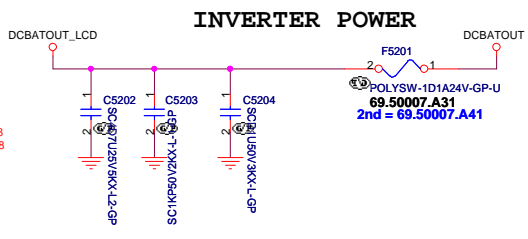
緯創資通		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
1D5V_S0 SYW232			
Size A4	Document Number EA40 HW ULT	Rev 1	
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VIDEO = VIDEO



- DP_HPDD_C 86
- BLON_OUT_C 86
- LCD_BRIGHTNESS 86
- DP_TXN1_CPU_C 86
- DP_TXP1_CPU_C 86
- DP_TXN0_CPU_C 86
- DP_TXP0_CPU_C 86
- DP_AUXP_CPU_C 86
- DP_AUXN_CPU_C 86



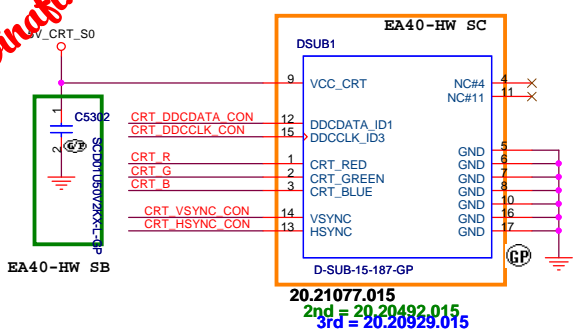
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Title			Rev		
LCD Connector			1		
Size Custom			EA40 HW ULT		
Date:	Thursday, May 30, 2013	Sheet	52	of	102

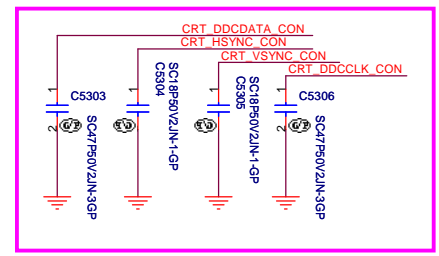
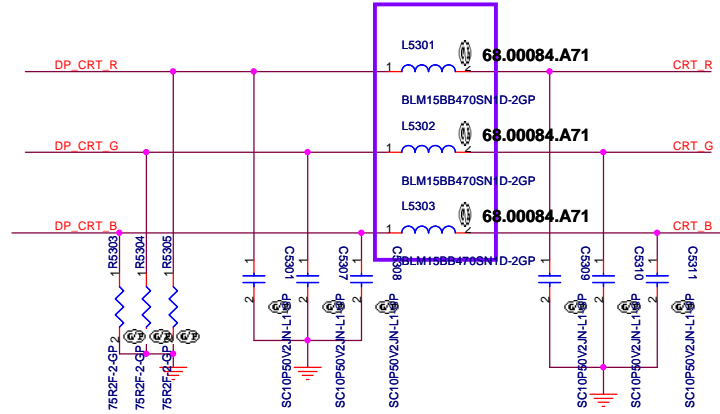
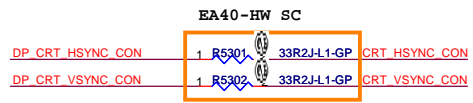
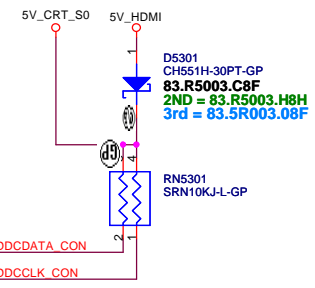
<http://vinafix.vn>

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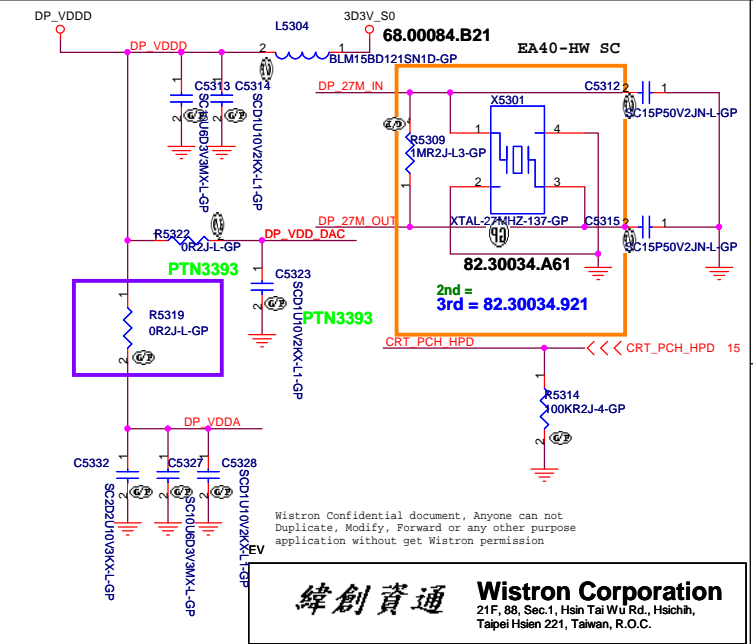
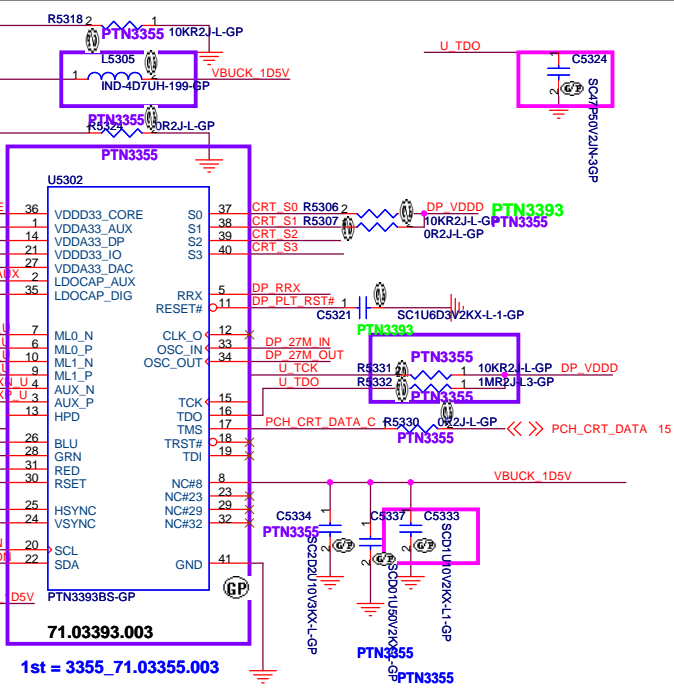
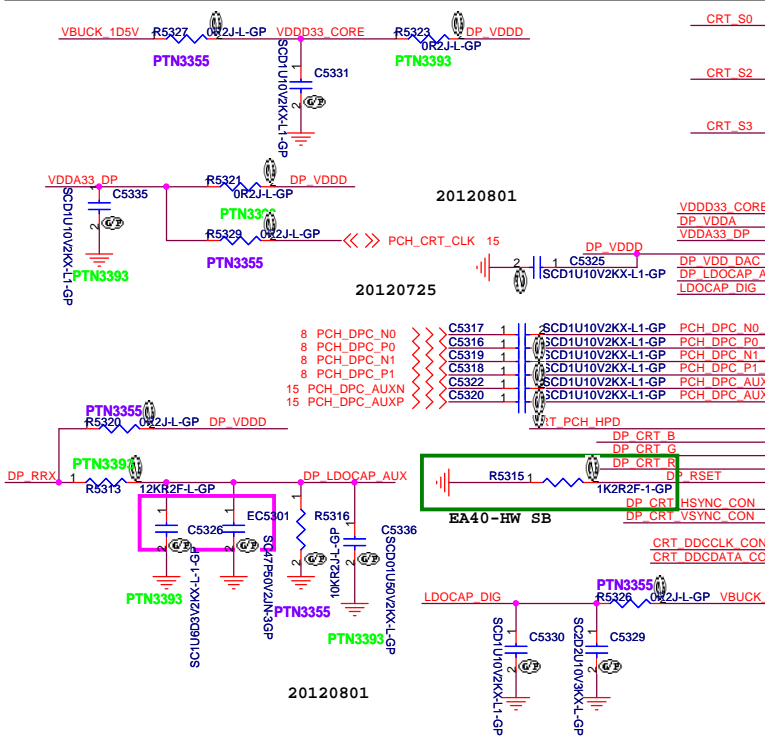
CRT DDCDATA & DDCCLK level shift



20.21077.015
2nd = 20.20492.015
3rd = 20.20829.015



EA40-HW SB



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Title		
CRT Board Connector		
Size	Document Number	Rev
A3	EA40 HW ULT	1
Date:	Monday, May 13, 2013	Sheet 53 of 102

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Title

Display Port

Size Custom

Document Number

EA40 HW ULT

Rev

1

Date: Monday, May 13, 2013

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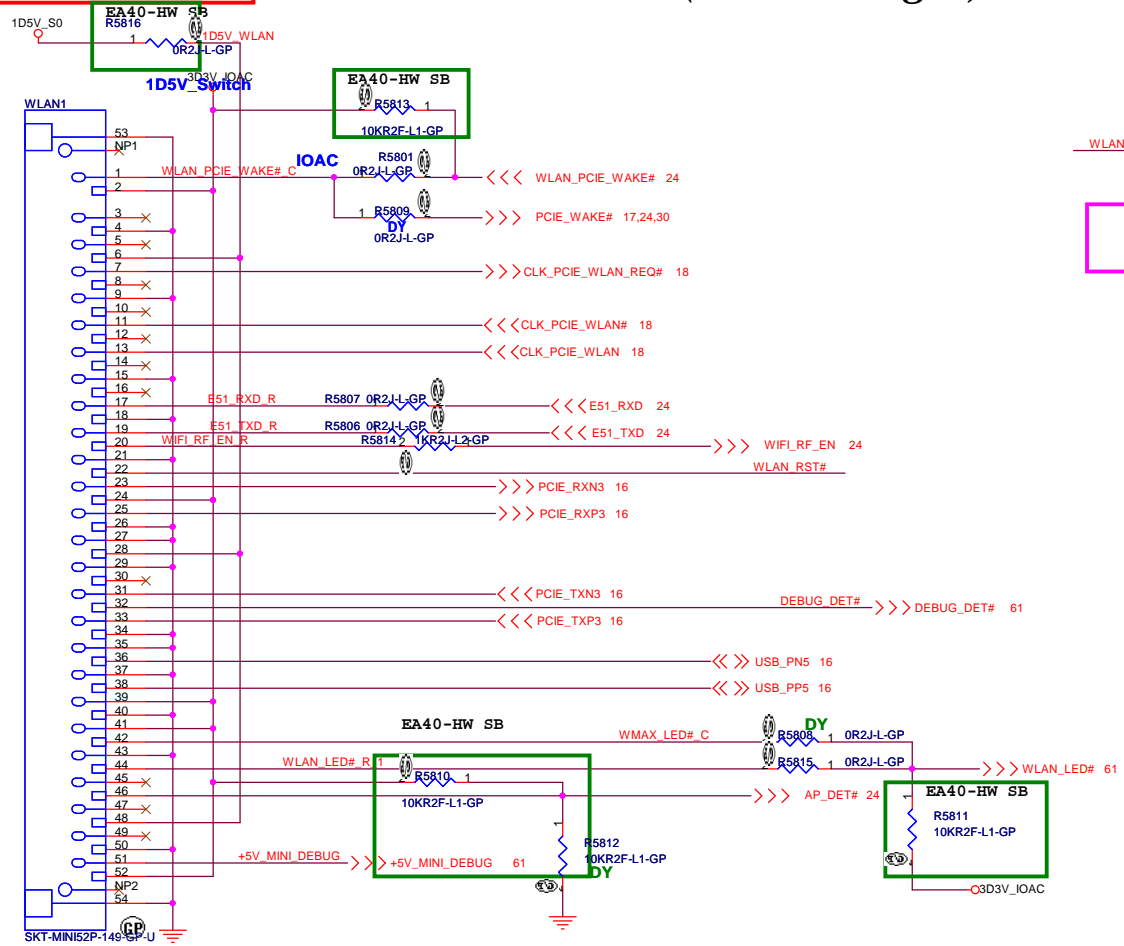
EV

緯創資通		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
E-SATA			
Size A4	Document Number EA40 HW ULT		Rev 1
Date: Monday, May 13, 2013		Sheet 57	of 102

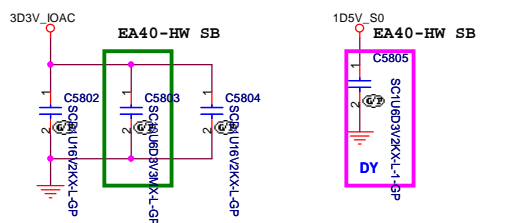
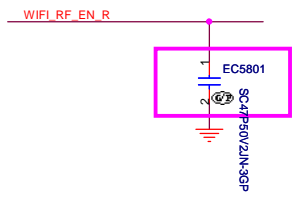
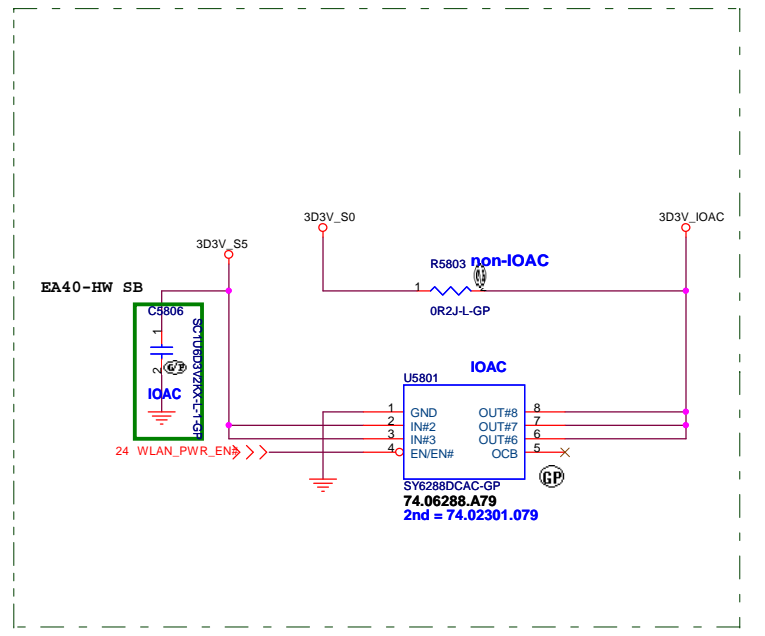
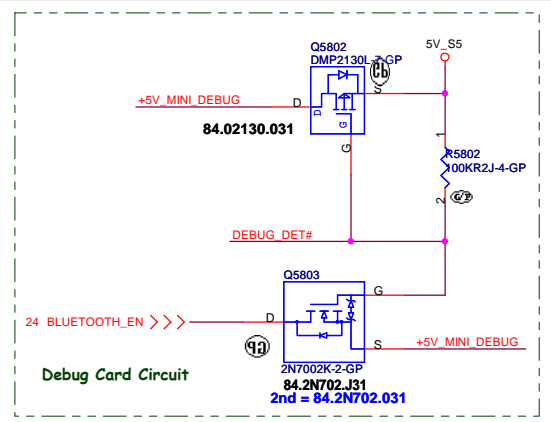
<http://vinafix.vn>

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SSID = Wireless Mini Card Connector(802.11a/b/g/n)



62.10043.I31
 2nd = 62.10043.I51
 3rd = 62.10043.K81



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Title		MINICARD(WLAN)	
Size	Document Number	Rev	
Custom	EA40 HW ULT	1	
Date:	Monday, May 13, 2013	Sheet	58 of 102

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SSID = Wireless

Mini Card Connector(mSATA)

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Title			
WWAN CONN			
Size A4	Document Number EA40 HW ULT		Rev 1
Date: Monday, May 13, 2013		Sheet 59	of 102

SSID = mSATA

Mini Card Connector(mSATA)

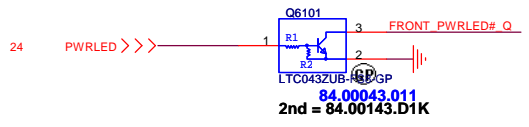
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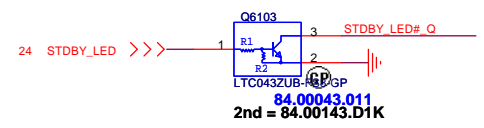
緯創資通		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
mSATA Connector			
Size A4	Document Number EA40 HW ULT		Rev 1
Date: Monday, May 13, 2013		Sheet 60	of 102

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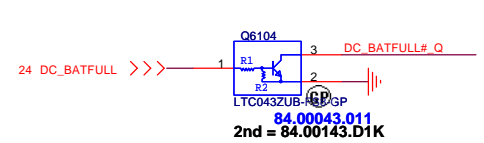
Power button LED



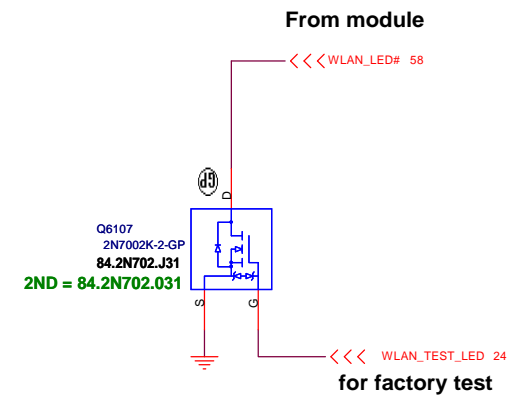
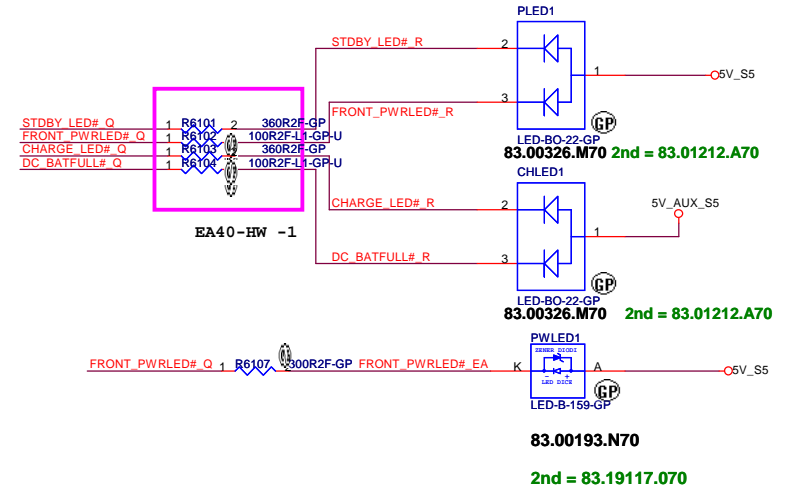
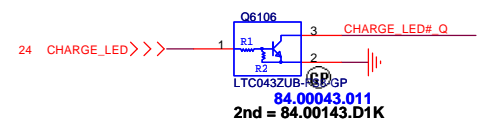
Power STDBY_LED



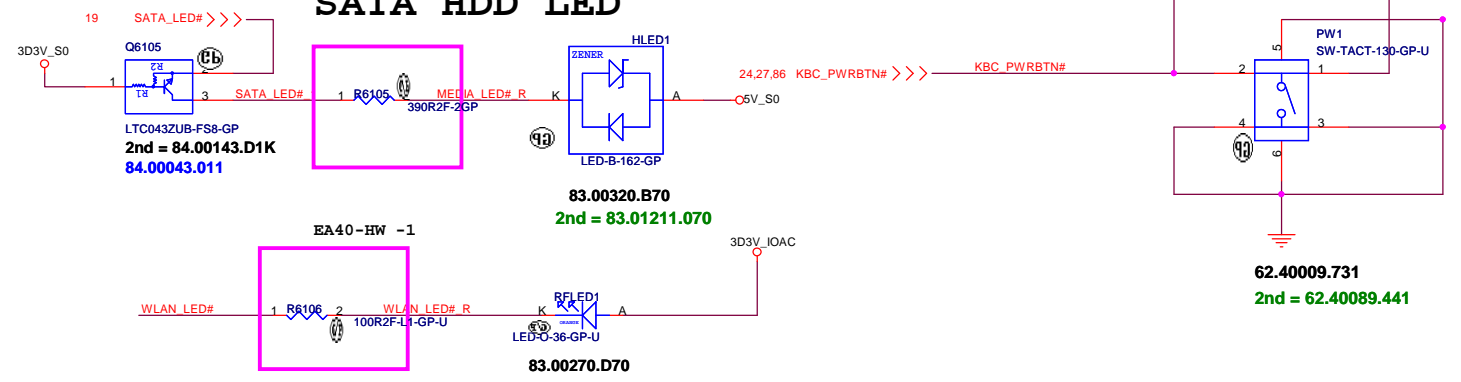
Battery LED2 (DC_BATFULL)



Battery LED1 (CHARGE)



SATA HDD LED

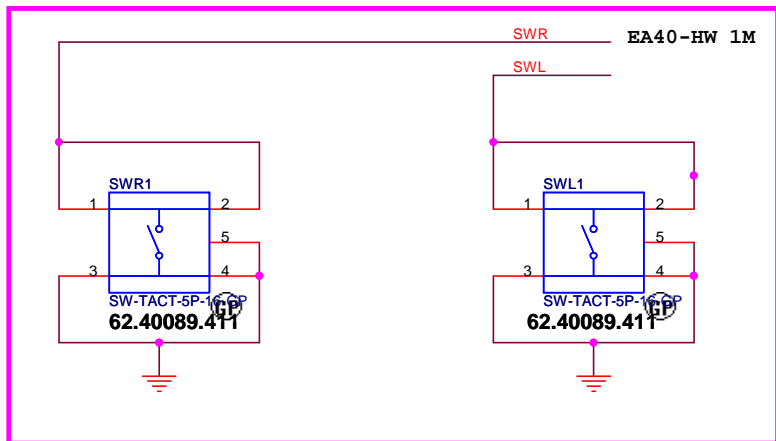


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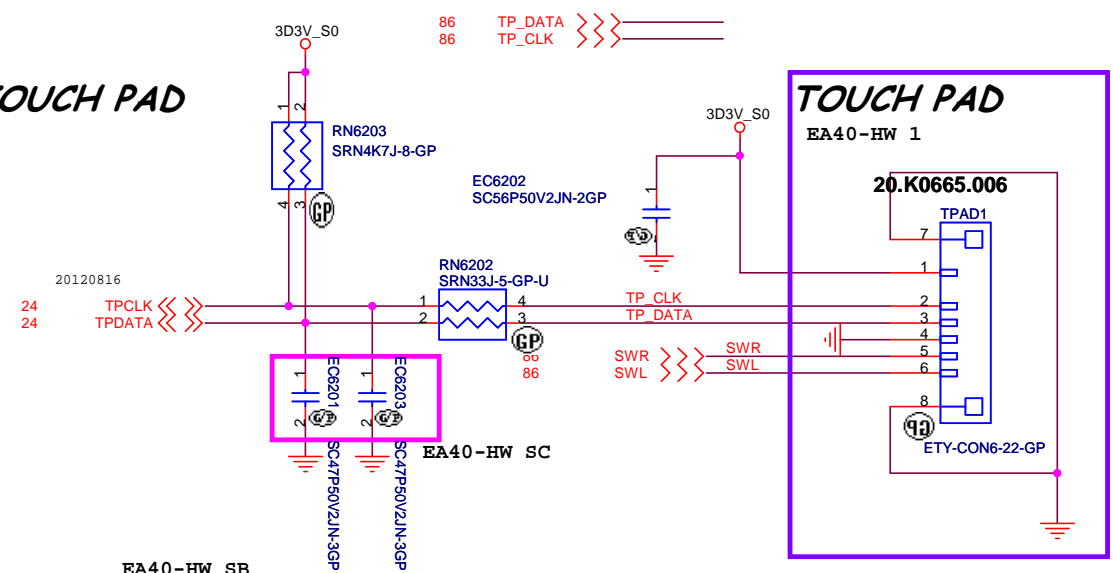
EV		Title	
Size A3		Document Number	
Date: Monday, May 13, 2013		Sheet 61 of 102	
<p>緯創資通 Wistron Corporation</p> <p>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</p>		<p>LED Bard/Power Button</p> <p>EA40 HW ULT</p> <p>Rev 1</p>	

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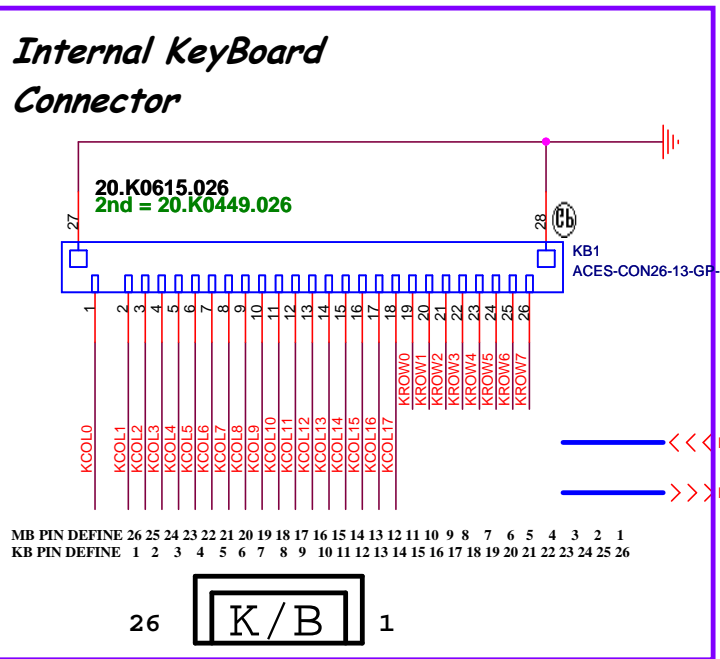
SSID = KBC



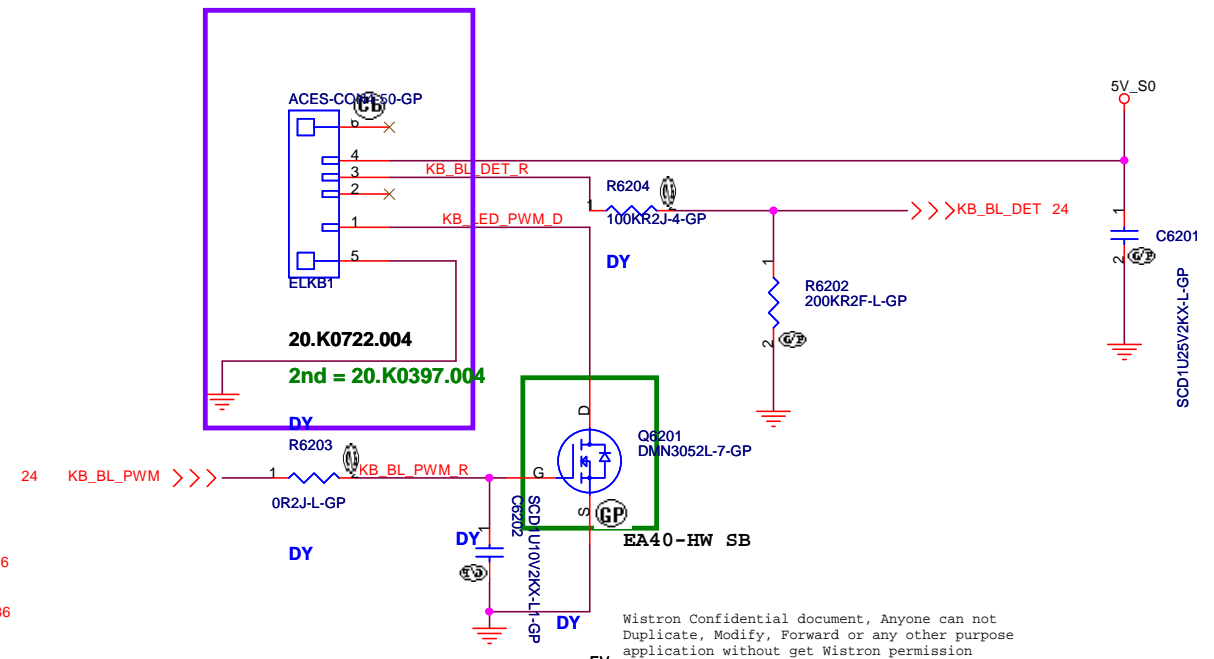
TOUCH PAD



EA40-HW SB



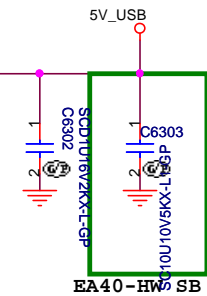
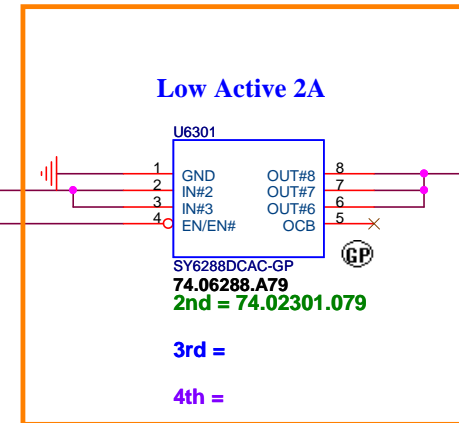
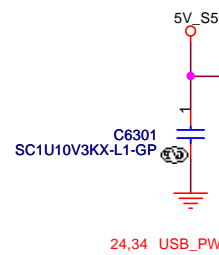
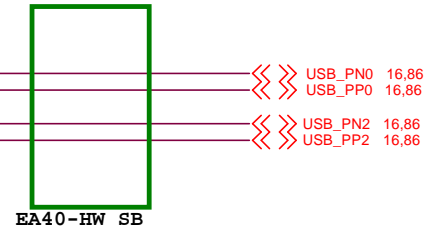
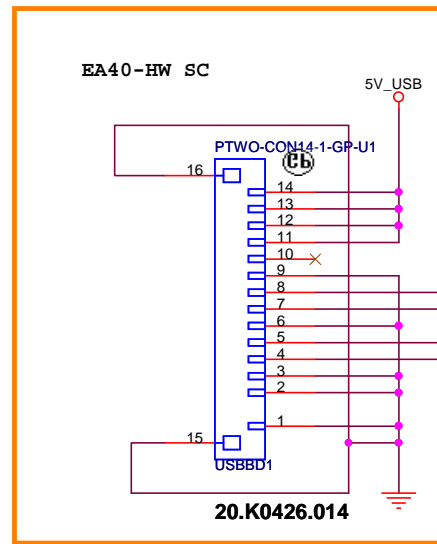
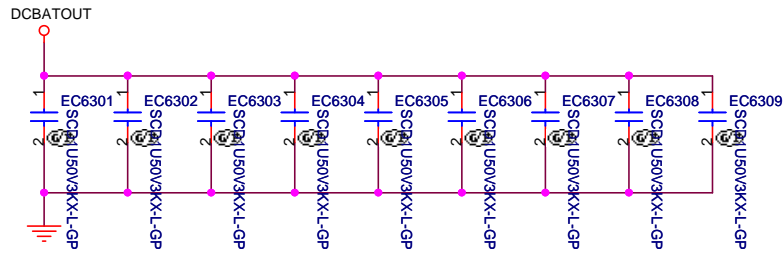
EA40-HW SB



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Title			
Key Board/Touch Pad			
Size	Document Number		Rev
Custom	EA40 HW ULT		1
Date:	Monday, May 13, 2013	Sheet 62 of	102

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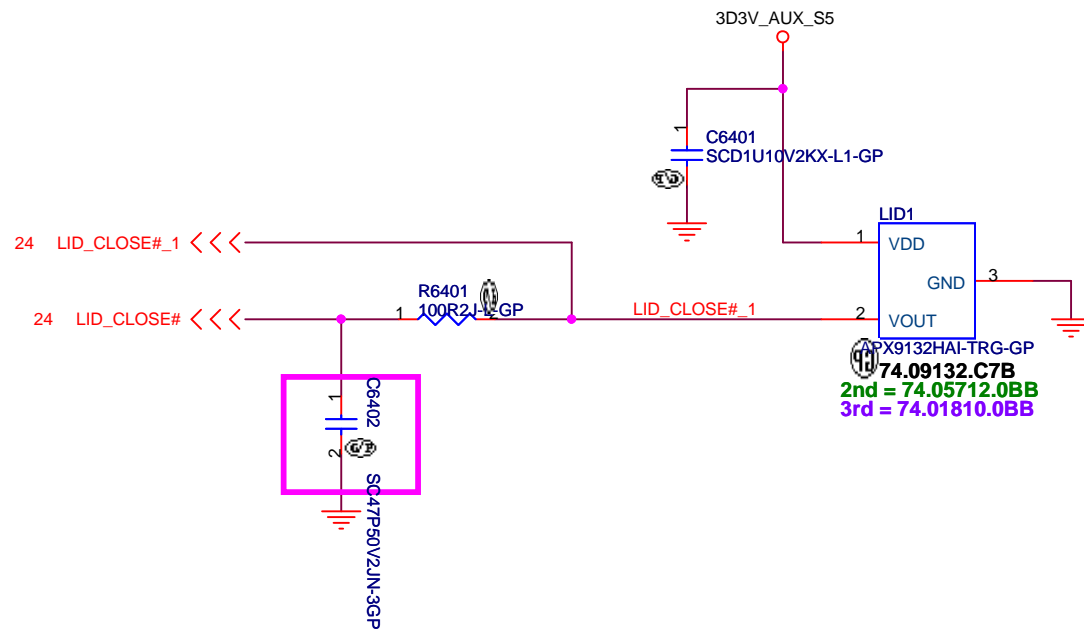
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Title IO Board Connector			
Size Custom	Document Number	Rev	
	EA40 HW ULT	1	
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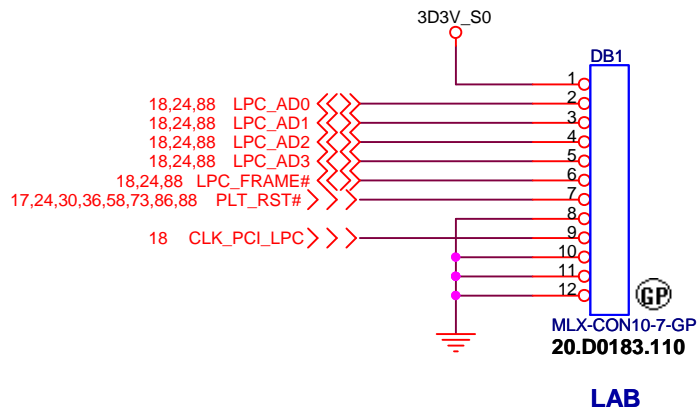


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Dubug connector			
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Title			
SENSOR HUB			
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Free Fall Sensor

Note

- no via, trace, under the sensor (keep out area around 2mm)
- stay away from the screw hole or metal shield soldering joints
- design PCB pad based on our sensor LGA pad size (add 0.1mm)
- solder stencil opening to 90% of the PCB pad size
- mount the sensor near the center of mass of the NB as possible as you can

SDO="H"; address="3Ah"
 *SDO="L"; address="38h"

*CS="H"; mode="I2C"
 CS="L"; mode="SPI"

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Title		
G Sensor		
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Thunderbolt (1/5)			
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D

D

C

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B

B

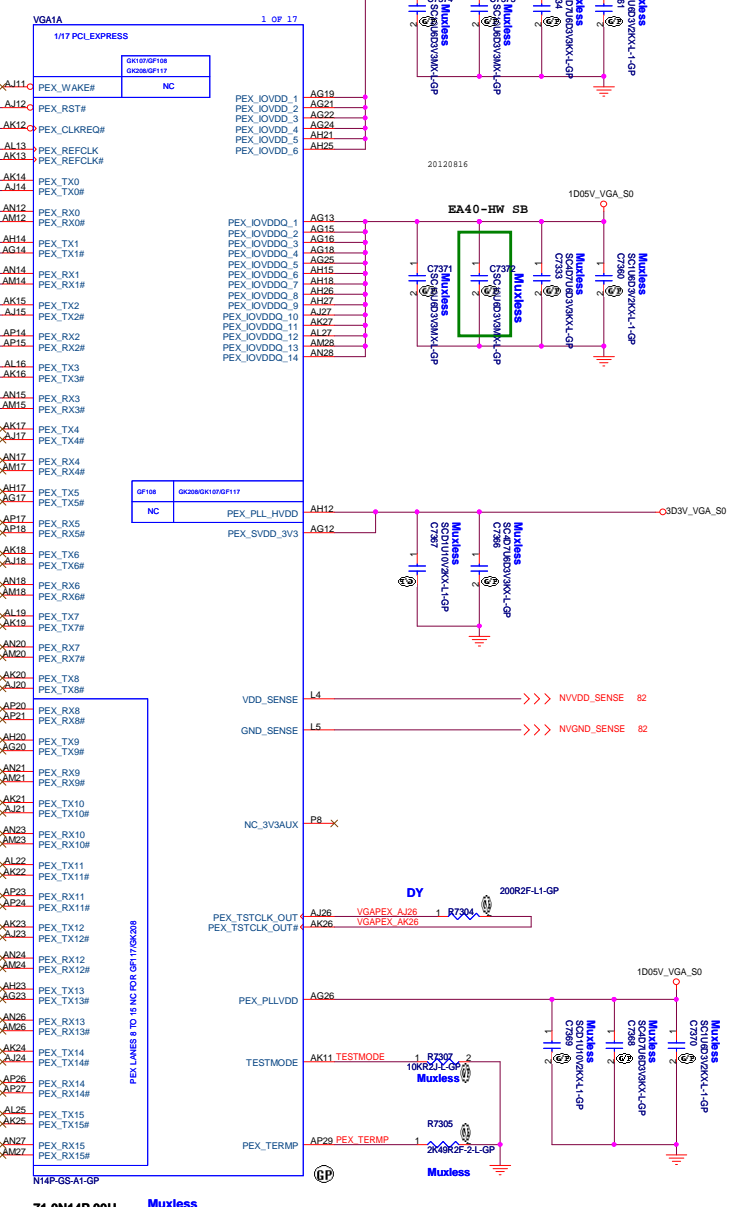
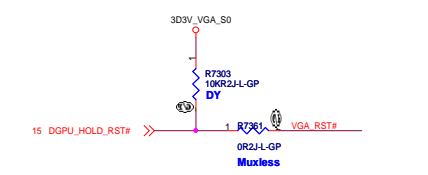
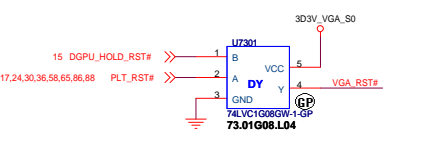
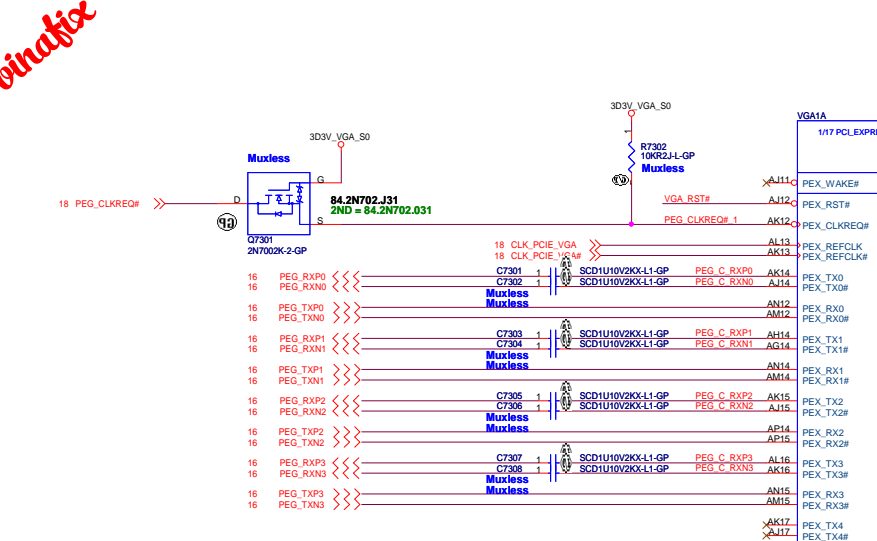
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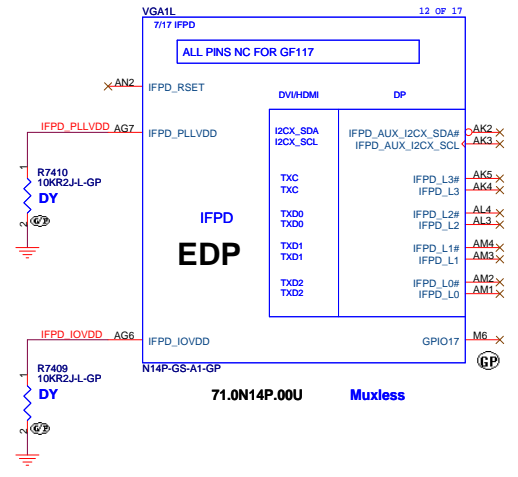
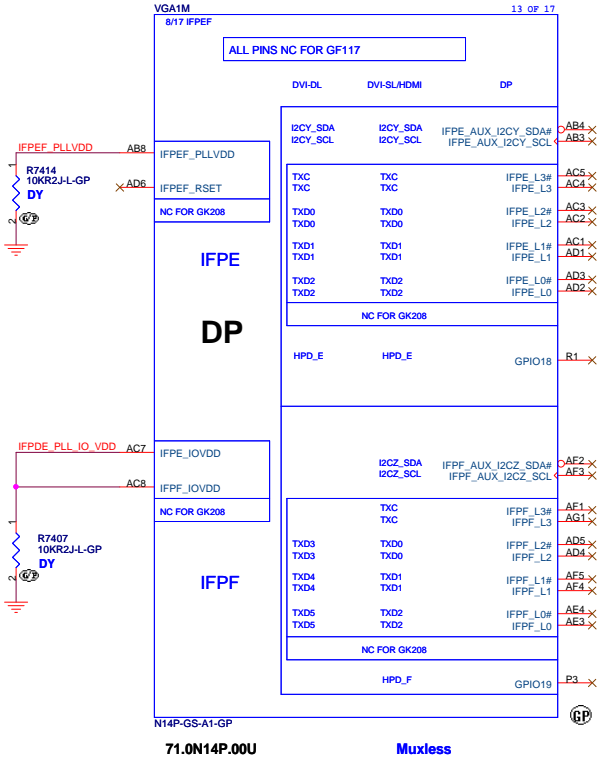
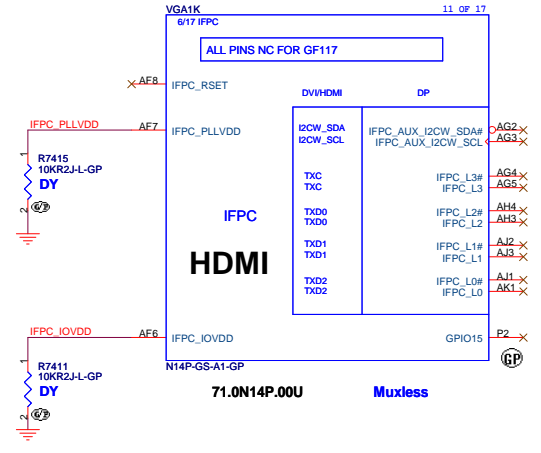
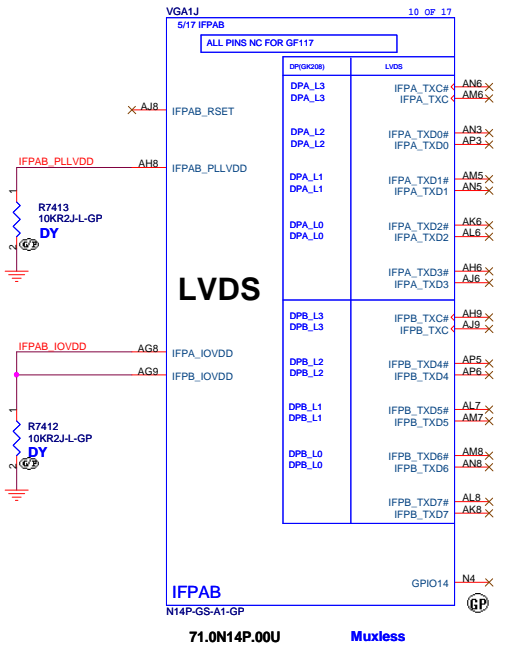
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A4	EA40 HW ULT		1
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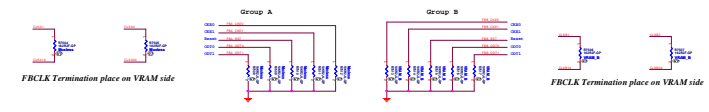
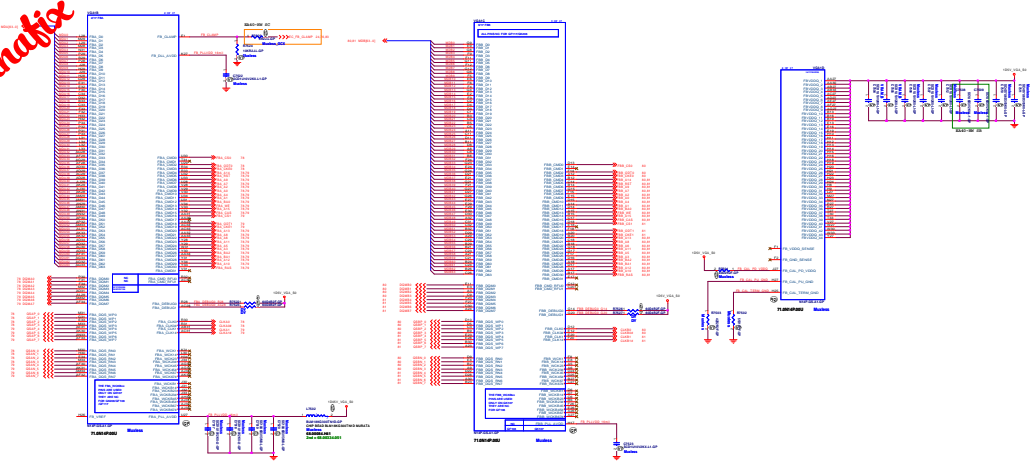
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GPU(PEG)		EA40 HW ULT	
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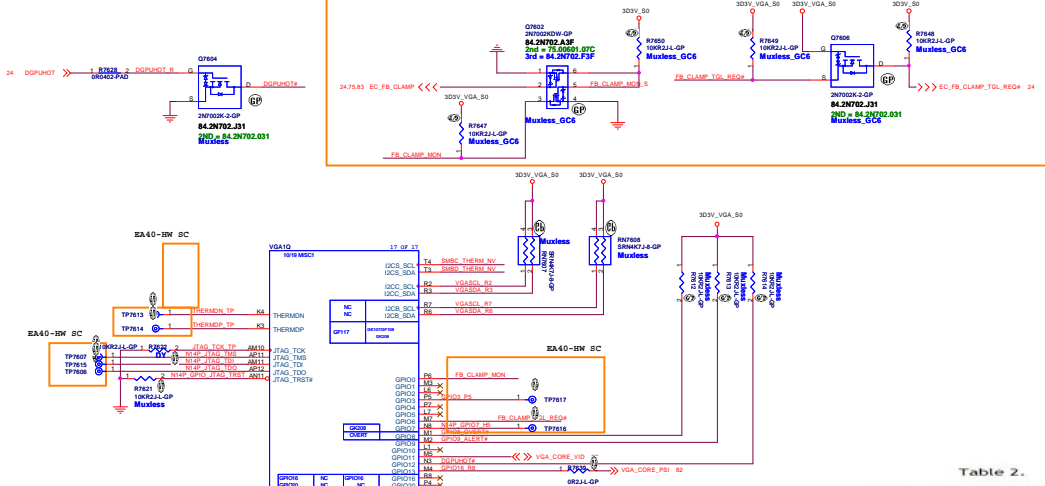
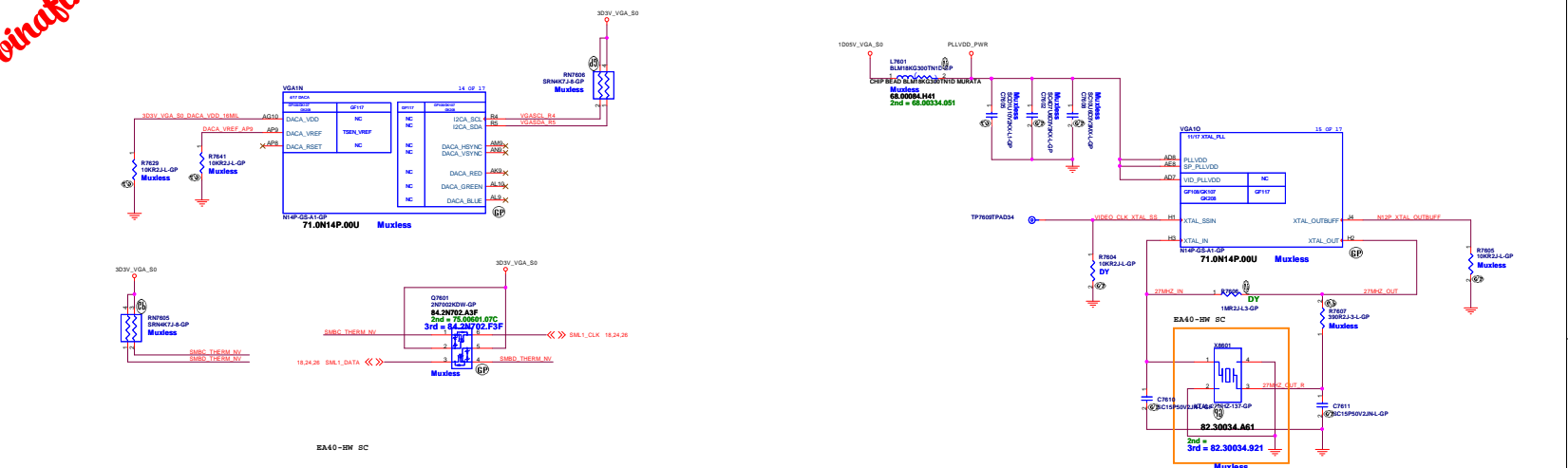
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Title: GPU (DIGITALOUT)
Size: Document Number: EA40 HW ULT Rev: 1
Date: Monday, May 13, 2013 Sheet: 74 of 102



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WIPI/VRAM PCB	1
6A-01-0001A.T	



N14M-GE use Binary Strap. Please see the below information.

Table 122 Binary Strap Mode Mapping

Strap Pin Name	Strap Mapping	Resistance	Polarity
ROM_SCLK	SMB_ALT_ADDR	10k Ω	Pull-down to GND
ROM_S1	SUB_VENDOR	10k Ω	Pull-up to 3V3 if VBIOS ROM exists Pull-down to GND if no VBIOS ROM
ROM_S0	VGA_DEVICE	10k Ω	Pull-down to GND (no display)
STRAP0	RAM_CFG[0]	10k Ω	See Note below
STRAP1	RAM_CFG[1]	10k Ω	See Note below
STRAP2	RAM_CFG[2]	10k Ω	See Note below
STRAP3	RAM_CFG[3]	10k Ω	See Note below
STRAP4	PCIE_MAX_SPEED	10k Ω	Pull-down to GND

Strap Pin Name	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0
ROM_SCLK	PCI_DEV[4]	SUB_VENDOR	PCI_DEV[5]	PEX_PLL_EN_TERM
ROM_S1	RAM_CFG[3]	RAM_CFG[2]	RAM_CFG[1]	RAM_CFG[0]
ROM_S0	FB[1]	FB[0]	SMB_ALT_ADDR	VGA_DEVICE
STRAP 0	USER[3]	USER[2]	USER[1]	USER[0]
STRAP 1	SGIO_PADCFG[3]	SGIO_PADCFG[2]	SGIO_PADCFG[1]	SGIO_PADCFG[0]
STRAP 2	PCI_DEV[3]	PCI_DEV[2]	PCI_DEV[1]	PCI_DEV[0]
STRAP 3	SOB2_EXPOSED	SOB2_EXPOSED	SOB1_EXPOSED	SOB0_EXPOSED
STRAP 4	RESERVED	PCIE_SPEED_CHANGE_EN[3]	PCIE_MAX_SPEED	DF_PLL_VDD33V

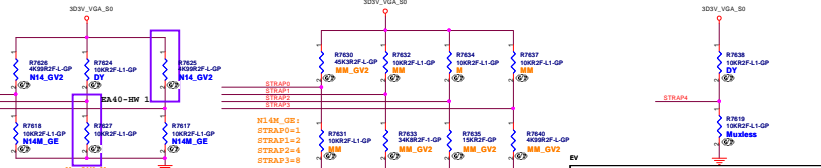
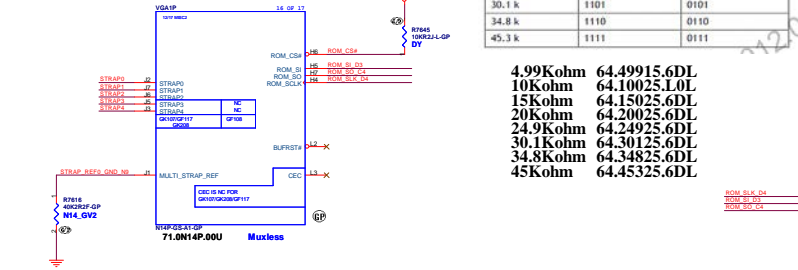
Table 113. Resistance Mapping to Hex Values

Resistor Values	Pull-up to VDD33	Pull-down to GND
4.99 k	1000	0000
10.0 k	1001	0001
15.0 k	1010	0010
20.0 k	1011	0011
24.9 k	1100	0100
30.1 k	1101	0101
34.8 k	1110	0110
45.3 k	1111	0111

- 4.99kOhm 64.49915.6DL
- 10kOhm 64.10025.L0L
- 15kOhm 64.15025.6DL
- 20kOhm 64.20025.6DL
- 24.9kOhm 64.24925.6DL
- 30.1kOhm 64.30125.6DL
- 34.8kOhm 64.34825.6DL
- 45.3kOhm 64.45325.6DL

Table 2. N14M-GE/GL DDR3 Recommended Memories 256Mx16 Configuration

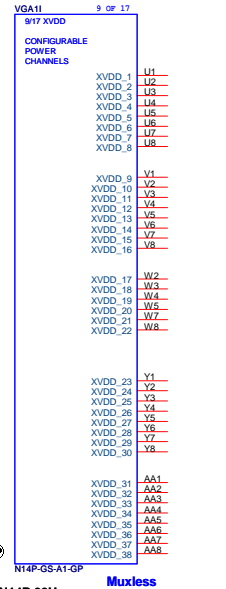
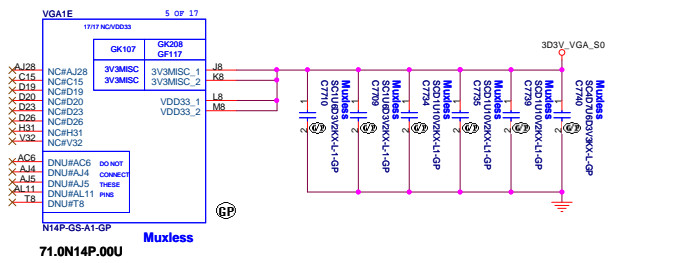
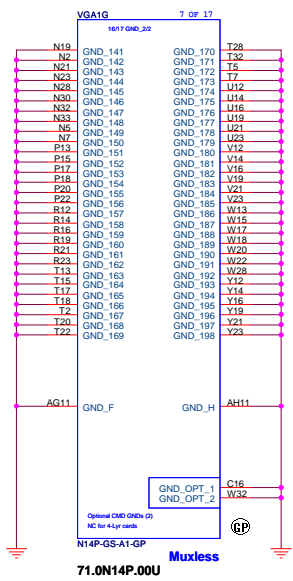
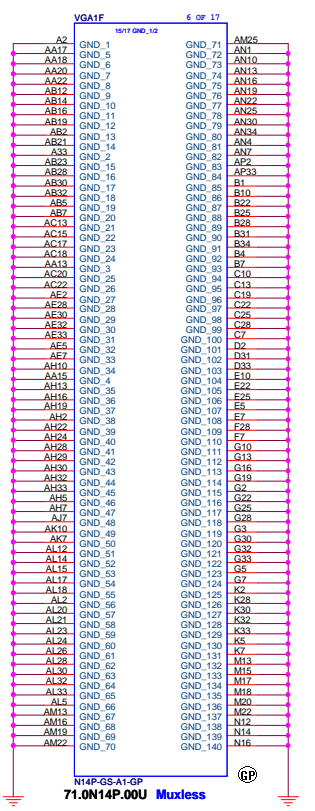
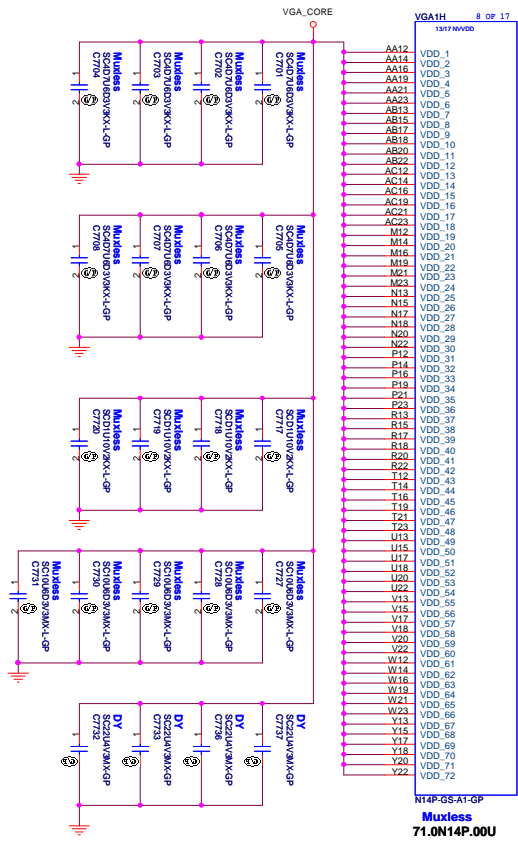
Configuration	Vendor	Strap	FBVDD/ FBVDDQ	Manufacturer Part Number	Max Speed CK (MHz)	Memory Date Code Minimum	Status
256Mx16 DDR3	Samsung	0x8	1.5 V / 1.5 V	K4W4G1646B-HC11	900	N/A	Production ready
		0xD	1.5 V / 1.5 V	MT41K256M16HA-1075LE	900	N/A	Production ready
	Micron	0x3	1.5V / 1.5V	H5TQ4G63MFR-11C	900	N/A	Production ready
		0x4	1.5V / 1.5V	H5TQ4G63AFR-11C	900	N/A	Future Production Candidate
128Mx16 DDR3	Micron	0x1	1.5 V / 1.5 V	MT41K128M16HT-0935E	1000	12/14	Production ready
		0x5	1.5 V / 1.5 V	K4W4G128M16CT-1075E	900	11/50	Production ready
	Samsung	0x5	1.5 V / 1.5 V	K4W4G1646E-BC1A	1000	1204	Production Candidate
		0x6	1.5V / 1.5V	K4W4G1646E-BC1T	900	1204	Production ready
Hynix	0x6	1.5V / 1.5V	H5TQ4G63DFE-H0C	1000	N/A	Production ready	
	0x6	1.5V / 1.5V	H5TQ4G63DFE-11C	900	N/A	Production ready	



ROM_SCLK	Strap2	Strap3	Strap4
N14P-GT1-A2	0x0FE4	0010	15k ohm pull-down
N14P-GV2-B-A1	0x1252	1000	3k ohm pull-up

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217, 218, 219, 220, 221, 222, 223, 224, 225, 226, 227, 228, 229, 230, 231, 232, 233, 234, 235, 236, 237, 238, 239, 240, 241, 242, 243, 244, 245, 246, 247, 248, 249, 250, 251, 252, 253, 254, 255, 256, 257, 258, 259, 260, 261, 262, 263, 264, 265, 266, 267, 268, 269, 270, 271, 272, 273, 274, 275, 276, 277, 278, 279, 280, 281, 282, 283, 284, 285, 286, 287, 288, 289, 290, 291, 292, 293, 294, 295, 296, 297, 298, 299, 300, 301, 302, 303, 304, 305, 306, 307, 308, 309, 310, 311, 312, 313, 314, 315, 316, 317, 318, 319, 320, 321, 322, 323, 324, 325, 326, 327, 328, 329, 330, 331, 332, 333, 334, 335, 336, 337, 338, 339, 340, 341, 342, 343, 344, 345, 346, 347, 348, 349, 350, 351, 352, 353, 354, 355, 356, 357, 358, 359, 360, 361, 362, 363, 364, 365, 366, 367, 368, 369, 370, 371, 372, 373, 374, 375, 376, 377, 378, 379, 380, 381, 382, 383, 384, 385, 386, 387, 388, 389, 390, 391, 392, 393, 394, 395, 396, 397, 398, 399, 400, 401, 402, 403, 404, 405, 406, 407, 408, 409, 410, 411, 412, 413, 414, 415, 416, 417, 418, 419, 420, 421, 422, 423, 424, 425, 426, 427, 428, 429, 430, 431, 432, 433, 434, 435, 436, 437, 438, 439, 440, 441, 442, 443, 444, 445, 446, 447, 448, 449, 450, 451, 452, 453, 454, 455, 456, 457, 458, 459, 460, 461, 462, 463, 464, 465, 466, 467, 468, 469, 470, 471, 472, 473, 474, 475, 476, 477, 478, 479, 480, 481, 482, 483, 484, 485, 486, 487, 488, 489, 490, 491, 492, 493, 494, 495, 496, 497, 498, 499, 500, 501, 502, 503, 504, 505, 506, 507, 508, 509, 510, 511, 512, 513, 514, 515, 516, 517, 518, 519, 520, 521, 522, 523, 524, 525, 526, 527, 528, 529, 530, 531, 532, 533, 534, 535, 536, 537, 538, 539, 540, 541, 542, 543, 544, 545, 546, 547, 548, 549, 550, 551, 552, 553, 554, 555, 556, 557, 558, 559, 560, 561, 562, 563, 564, 565, 566, 567, 568, 569, 570, 571, 572, 573, 574, 575, 576, 577, 578, 579, 580, 581, 582, 583, 584, 585, 586, 587, 588, 589, 590, 591, 592, 593, 594, 595, 596, 597, 598, 599, 600, 601, 602, 603, 604, 605, 606, 607, 608, 609, 610, 611, 612, 613, 614, 615, 616, 617, 618, 619, 620, 621, 622, 623, 624, 625, 626, 627, 628, 629, 630, 631, 632, 633, 634, 635, 636, 637, 638, 639, 640, 641, 642, 643, 644, 645, 646, 647, 648, 649, 650, 651, 652, 653, 654, 655, 656, 657, 658, 659, 660, 661, 662, 663, 664, 665, 666, 667, 668, 669, 670, 671, 672, 673, 674, 675, 676, 677, 678, 679, 680, 681, 682, 683, 684, 685, 686, 687, 688, 689, 690, 691, 692, 693, 694, 695, 696, 697, 698, 699, 700, 701, 702, 703, 704, 705, 706, 707, 708, 709, 710, 711, 712, 713, 714, 715, 716, 717, 718, 719, 720, 721, 722, 723, 724, 725, 726, 727, 728, 729, 730, 731, 732, 733, 734, 735, 736, 737, 738, 739, 740, 741, 742, 743, 744, 745, 746, 747, 748, 749, 750, 751, 752, 753, 754, 755, 756, 757, 758, 759, 760, 761, 762, 763, 764, 765, 766, 767, 768, 769, 770, 771, 772, 773, 774, 775, 776, 777, 778, 779, 780, 781, 782, 783, 784, 785, 786, 787, 788, 789, 790, 791, 792, 793, 794, 795, 796, 797, 798, 799, 800, 801, 802, 803, 804, 805, 806, 807, 808, 809, 810, 811, 812, 813, 814, 815, 816, 817, 818, 819, 820, 821, 822, 823, 824, 825, 826, 827, 828, 829, 830, 831, 832, 833, 834, 835, 836, 837, 838, 839, 840, 841, 842, 843, 844, 845, 846, 847, 848, 849, 850, 851, 852, 853, 854, 855, 856, 857, 858, 859, 860, 861, 862, 863, 864, 865, 866, 867, 868, 869, 870, 871, 872, 873, 874, 875, 876, 877, 878, 879, 880, 881, 882, 883, 884, 885, 886, 887, 888, 889, 890, 891, 892, 893, 894, 895, 896, 897, 898, 899, 900, 901, 902, 903, 904, 905, 906, 907, 908, 909, 910, 911, 912, 913, 914, 915, 916, 917, 918, 919, 920, 921, 922, 923, 924, 925, 926, 927, 928, 929, 930, 931, 932, 933, 934, 935, 936, 937, 938, 939, 940, 941, 942, 943, 944, 945, 946, 947, 948, 949, 950, 951, 952, 953, 954, 955, 956, 957, 958, 959, 960, 961, 962, 963, 964, 965, 966, 967, 968, 969, 970, 971, 972, 973, 974, 975, 976, 977, 978, 979, 980, 981, 982, 983, 984, 985, 986, 987, 988, 989, 990, 991, 992, 993, 994, 995, 996, 997, 998, 999, 1000.

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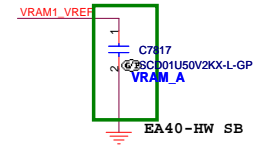
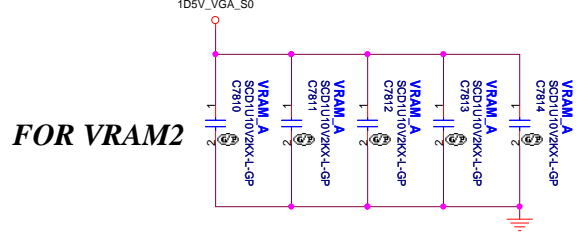
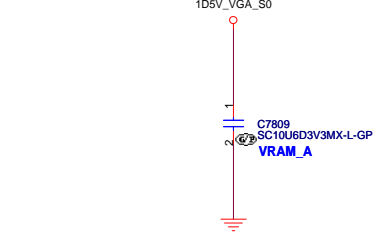
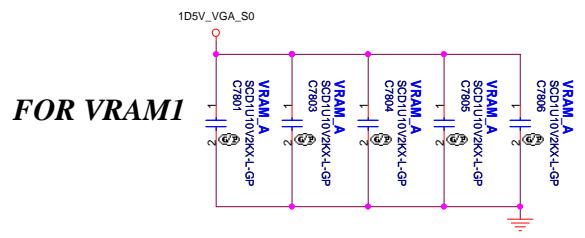
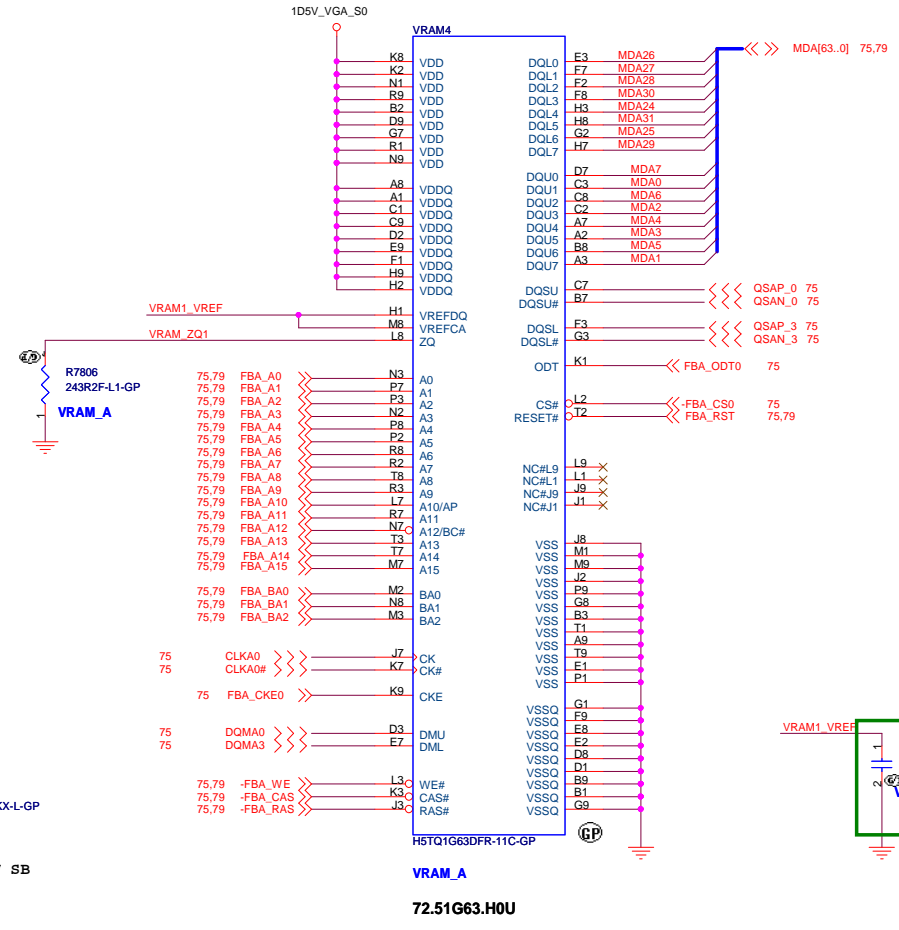
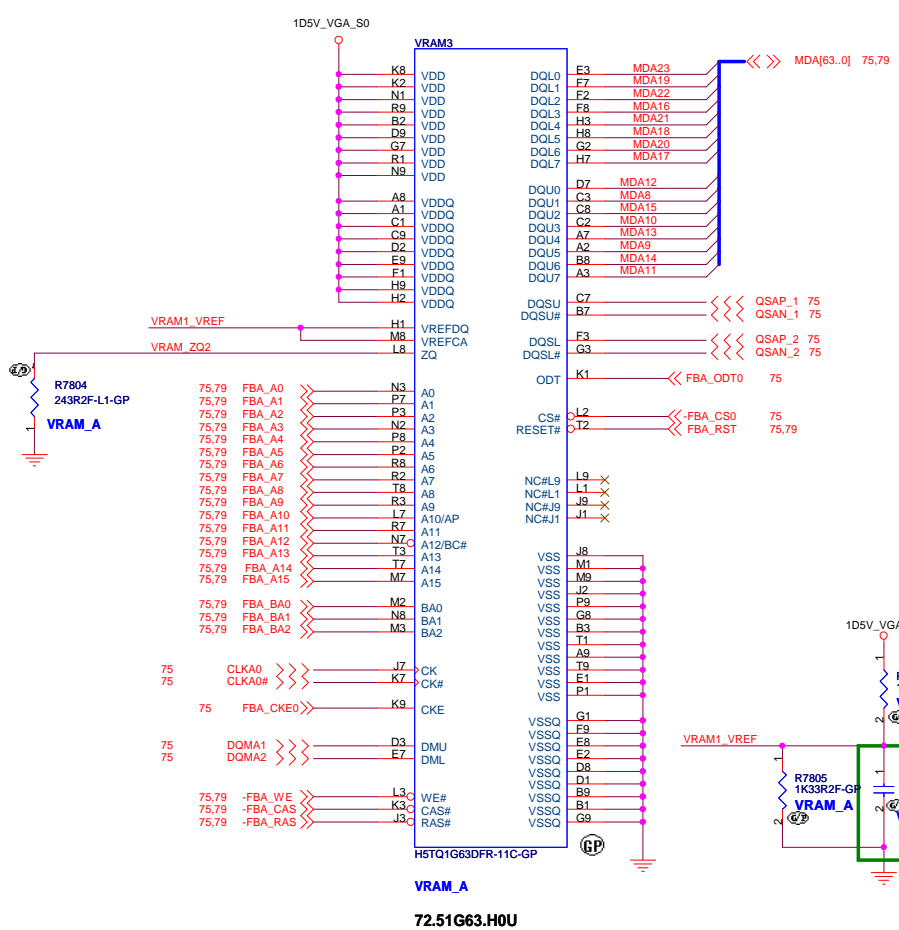
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Title: GPU (POWER/GND)
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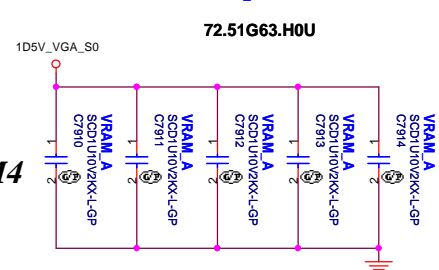
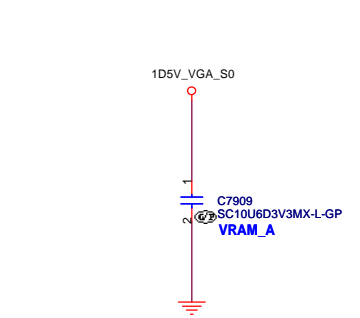
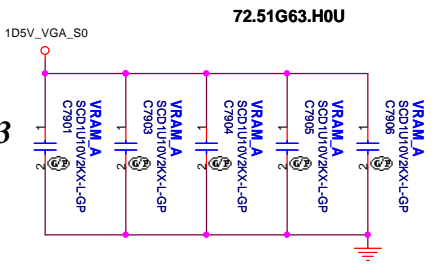
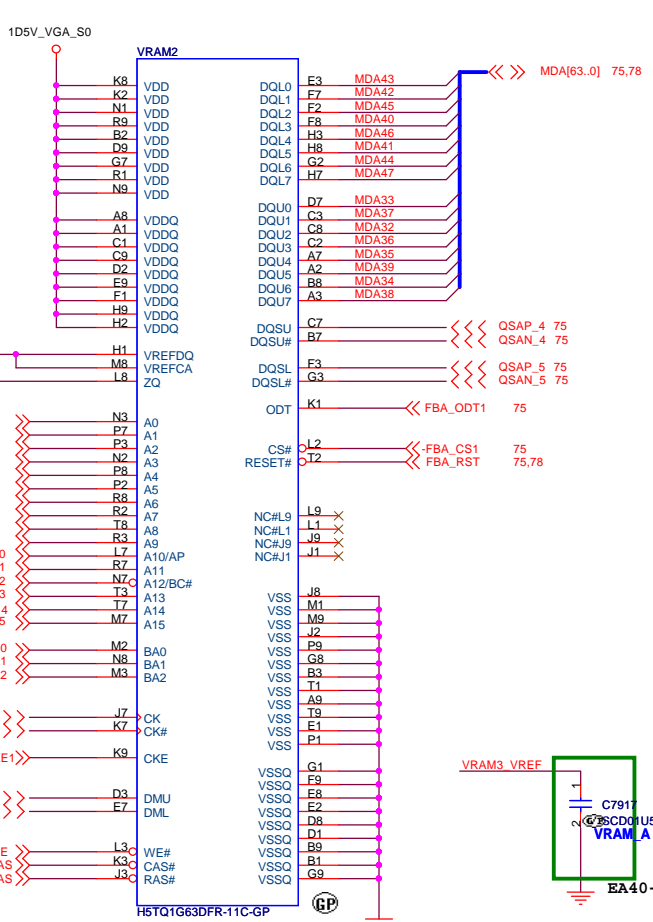
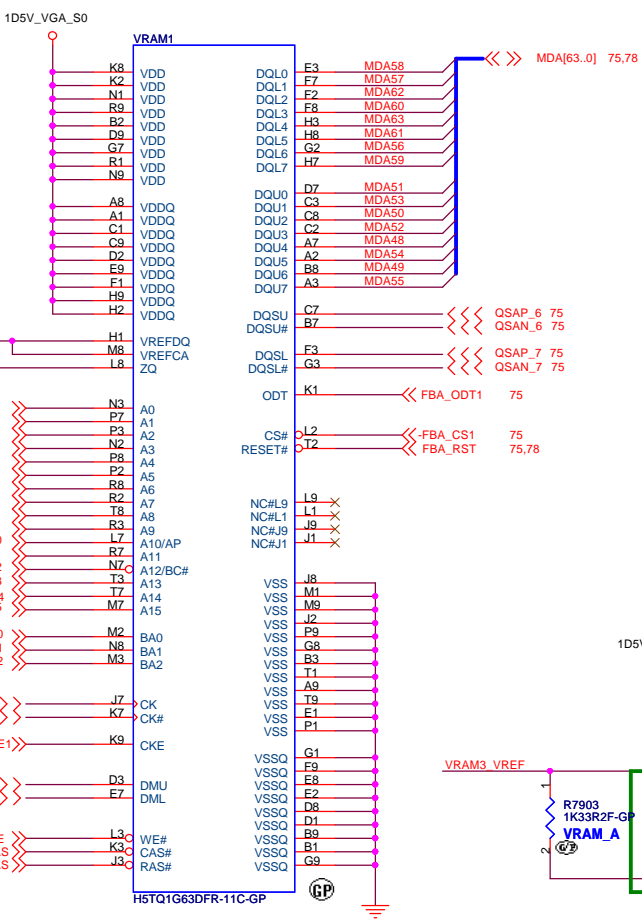
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<p>Title: GPU-VRAM1,2 (1/4)</p>	
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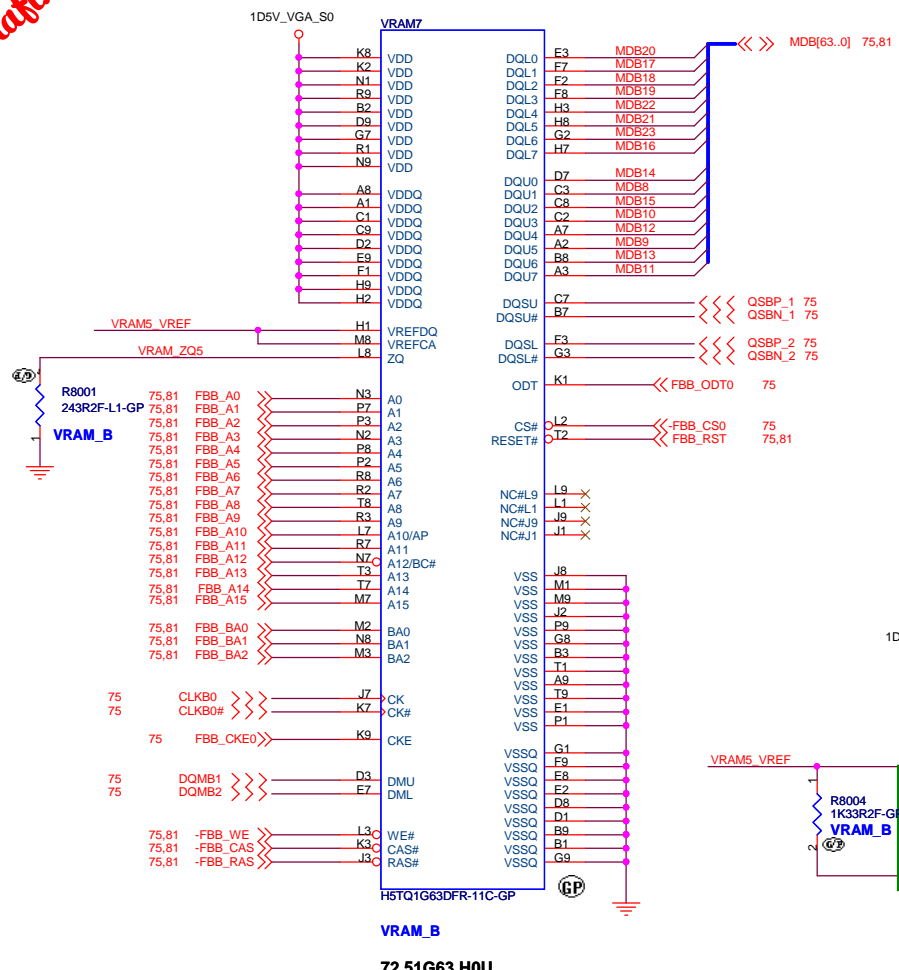


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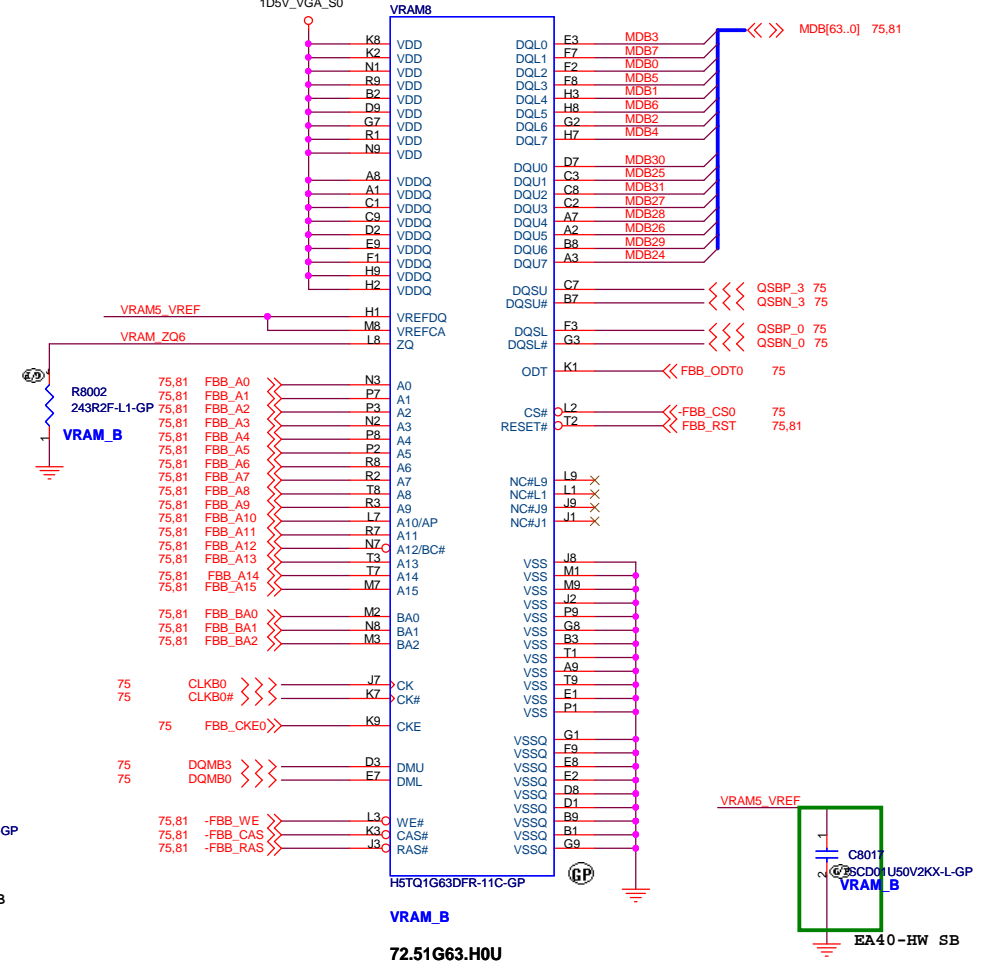
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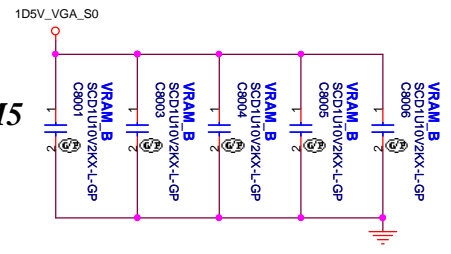


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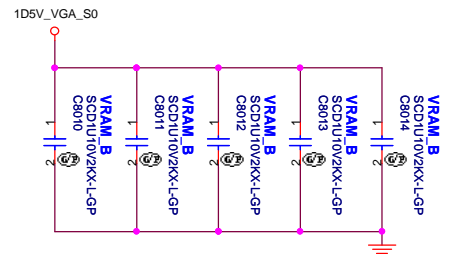
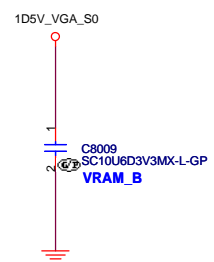


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FOR VRAM5



FOR VRAM6



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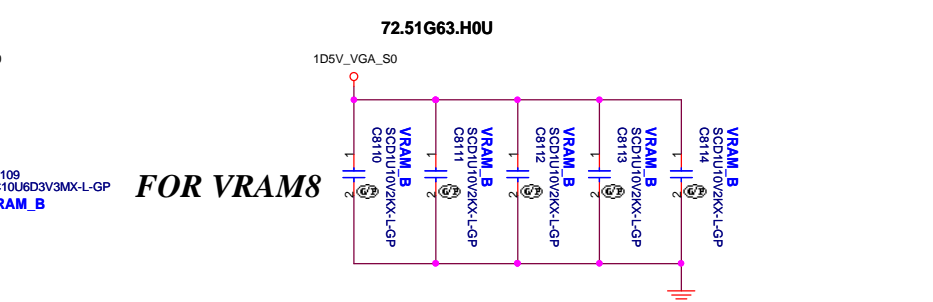
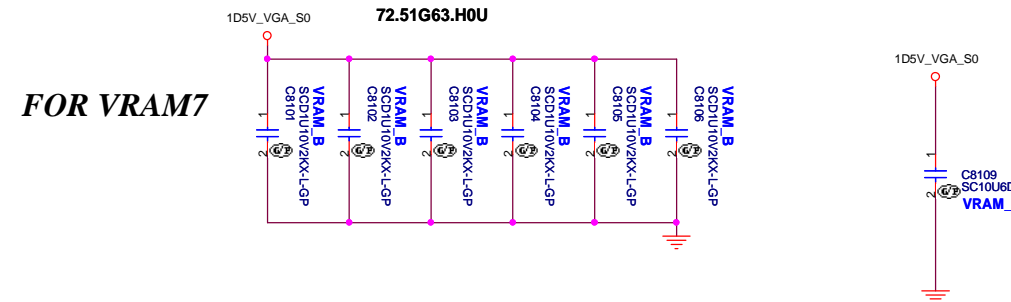
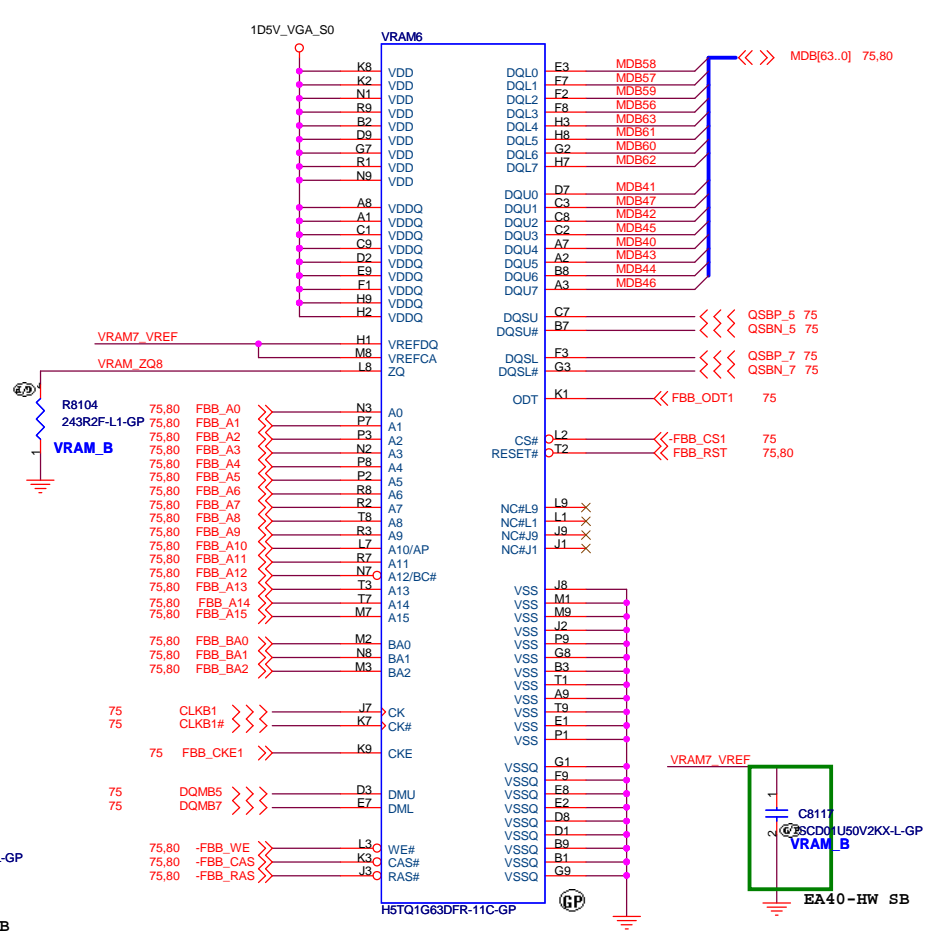
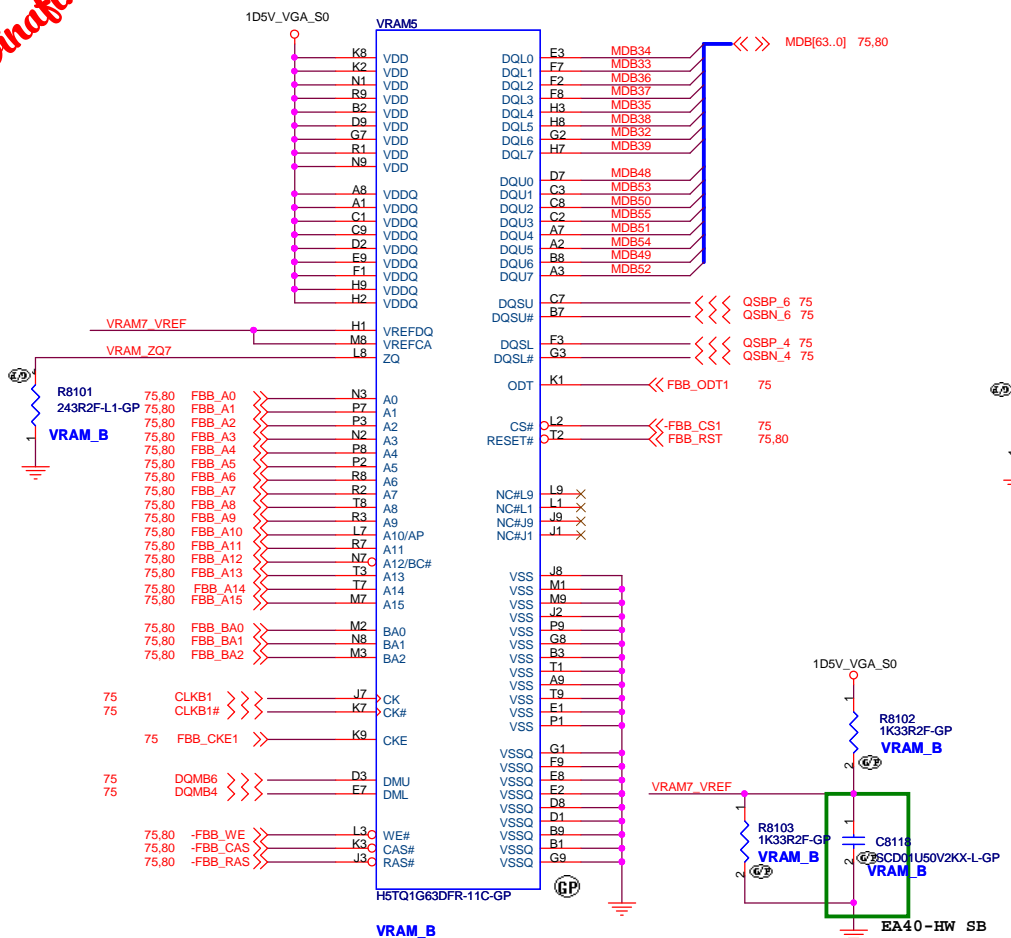
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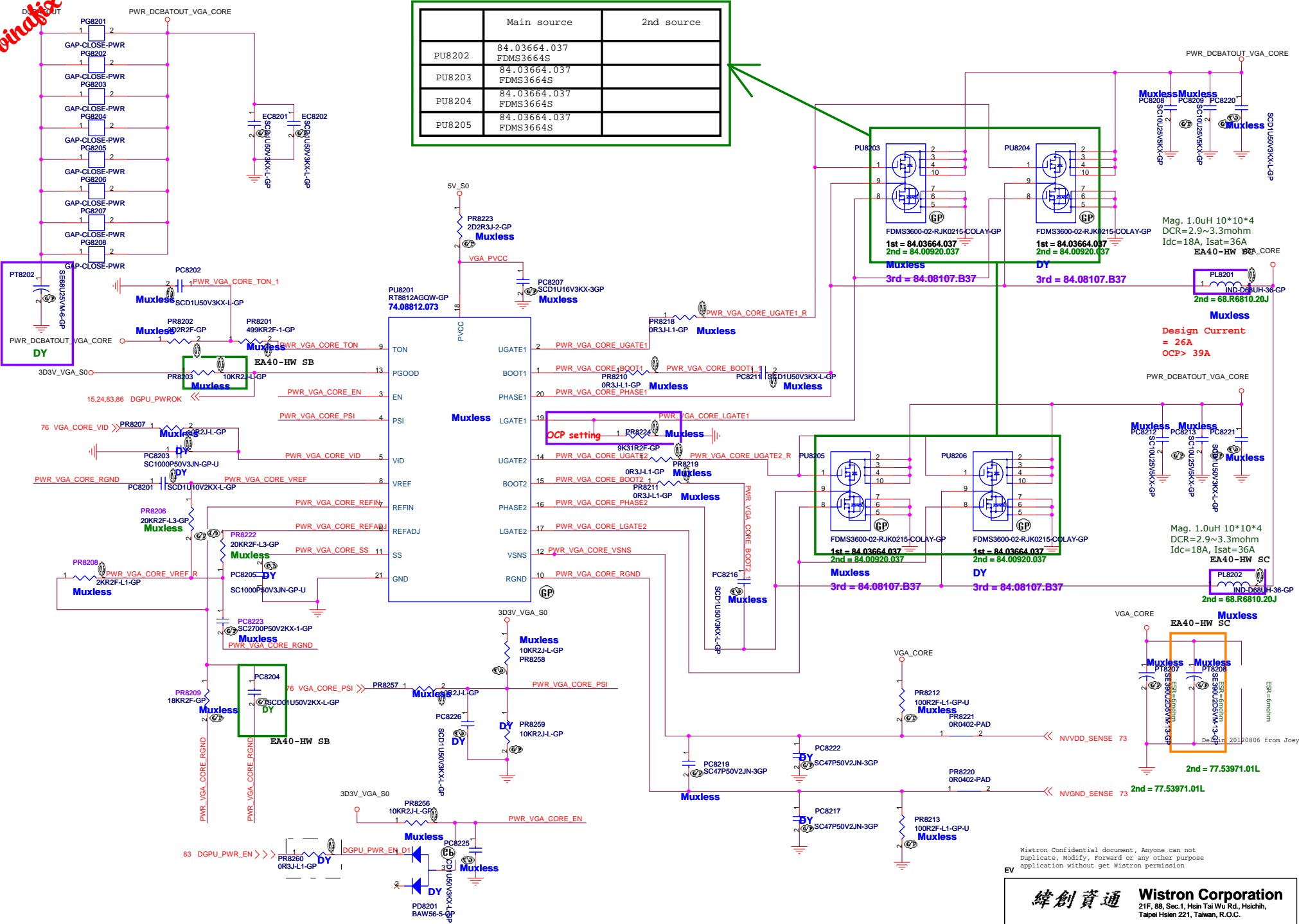
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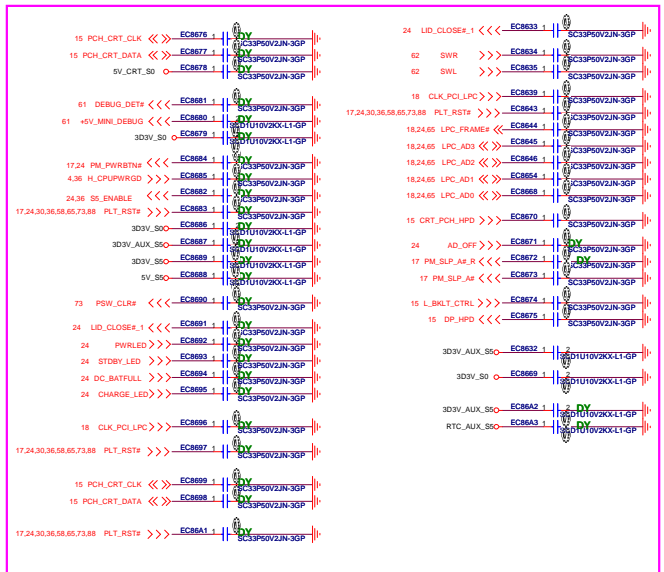
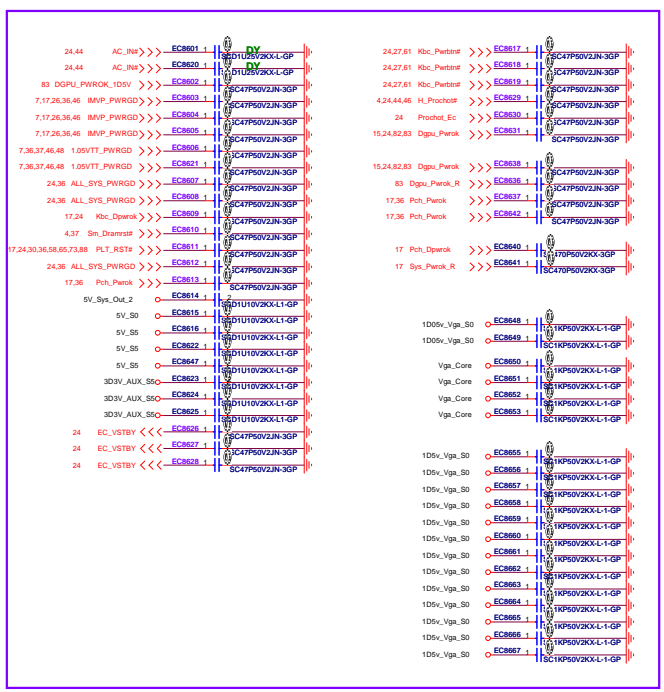
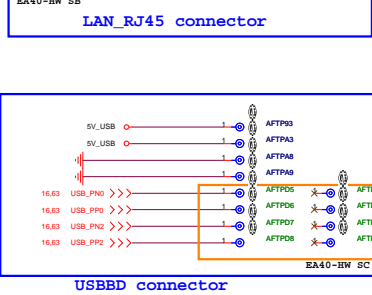
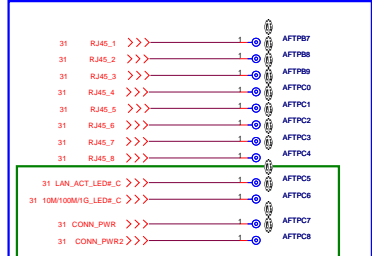
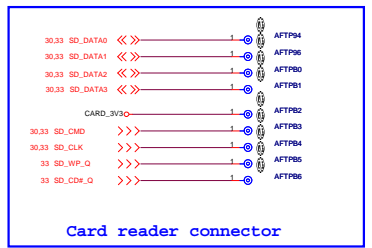
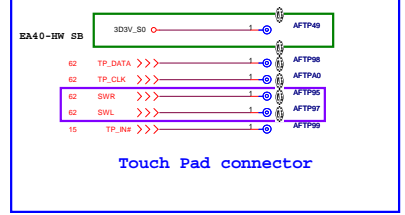
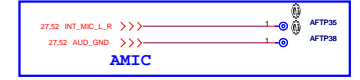
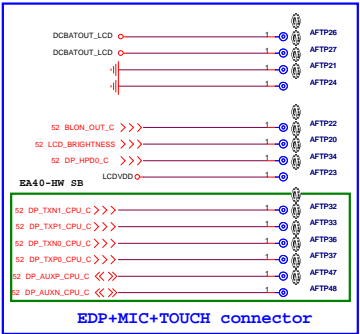
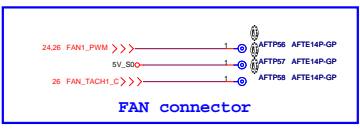
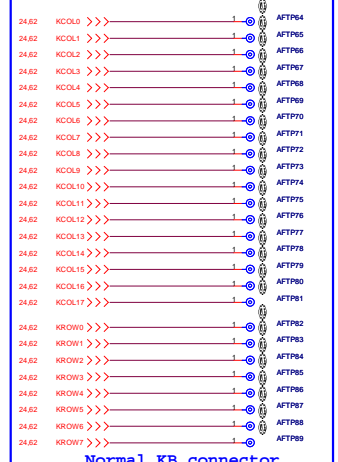
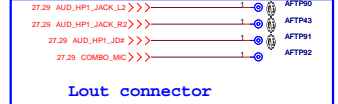
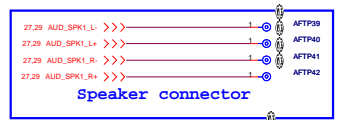
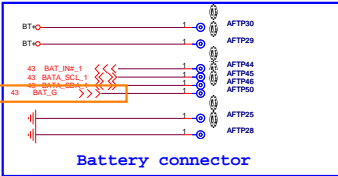
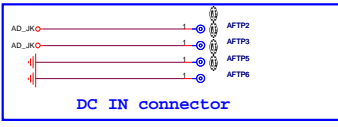
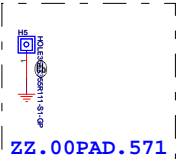
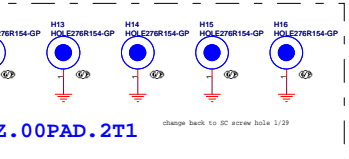
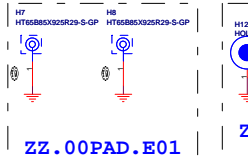
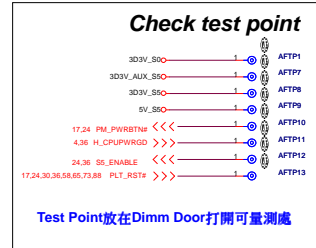
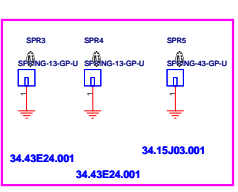
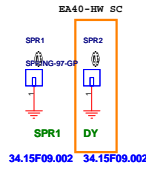
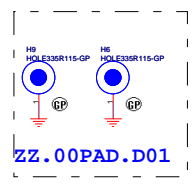
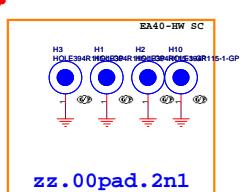
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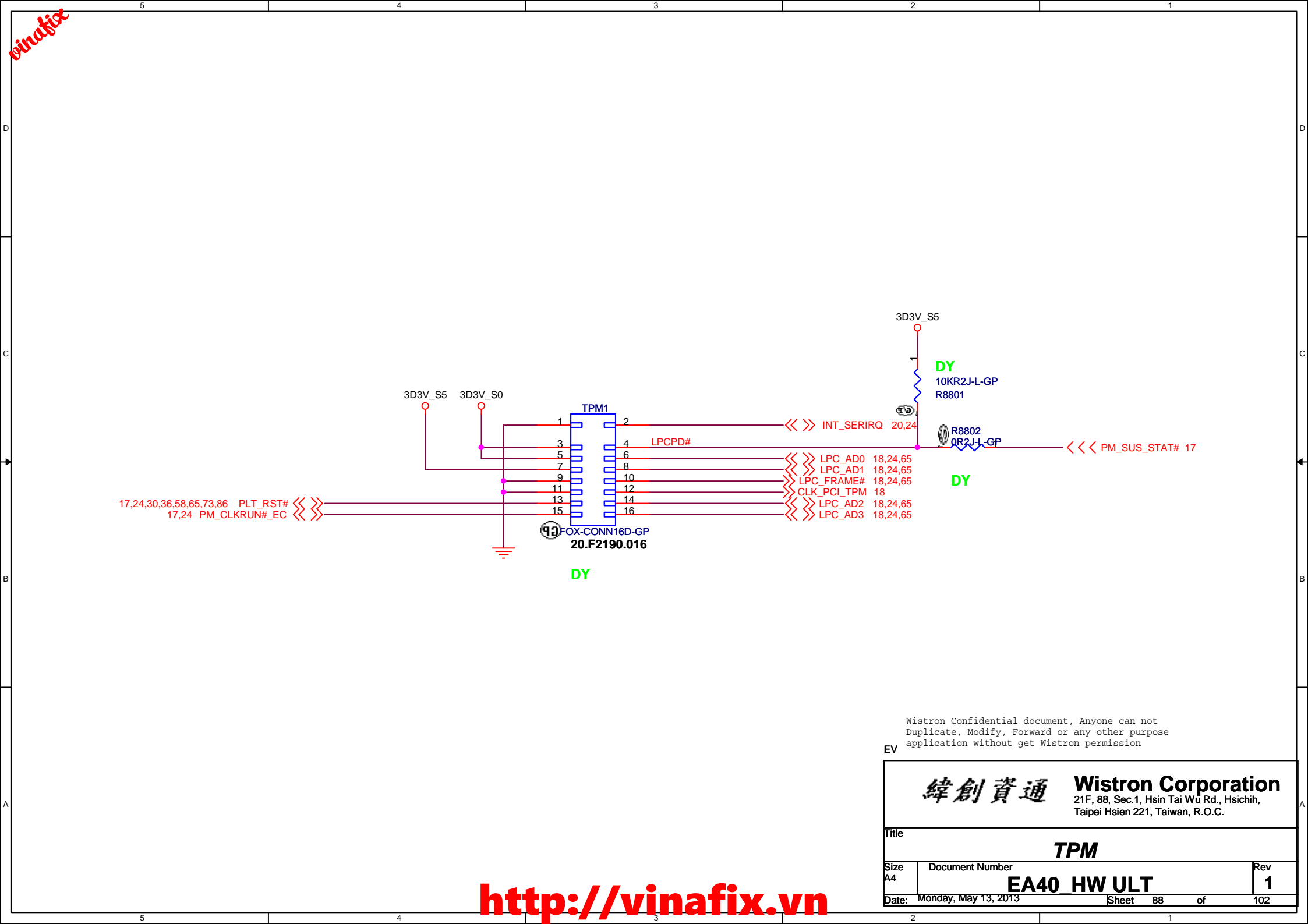
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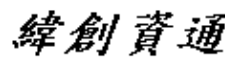
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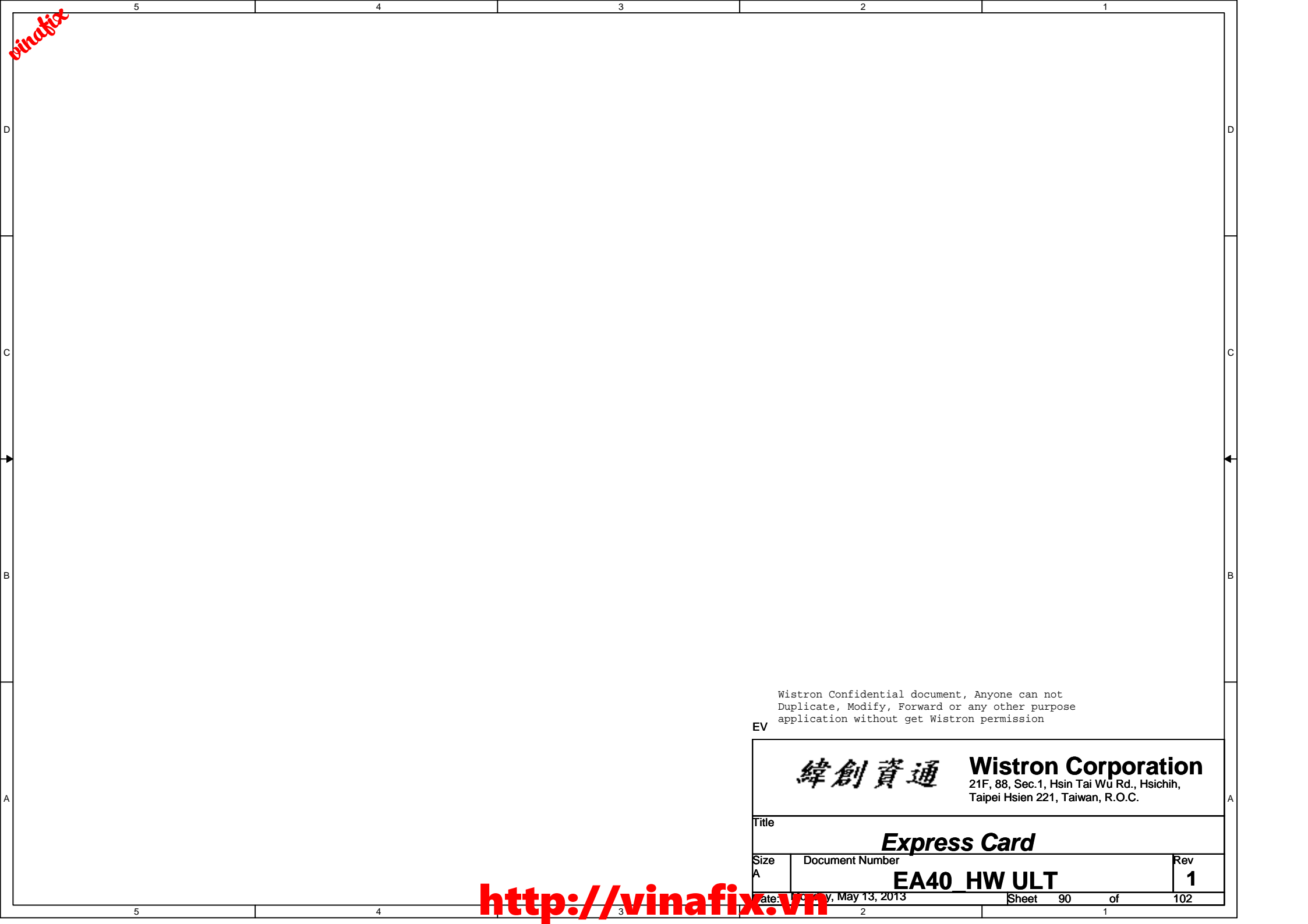
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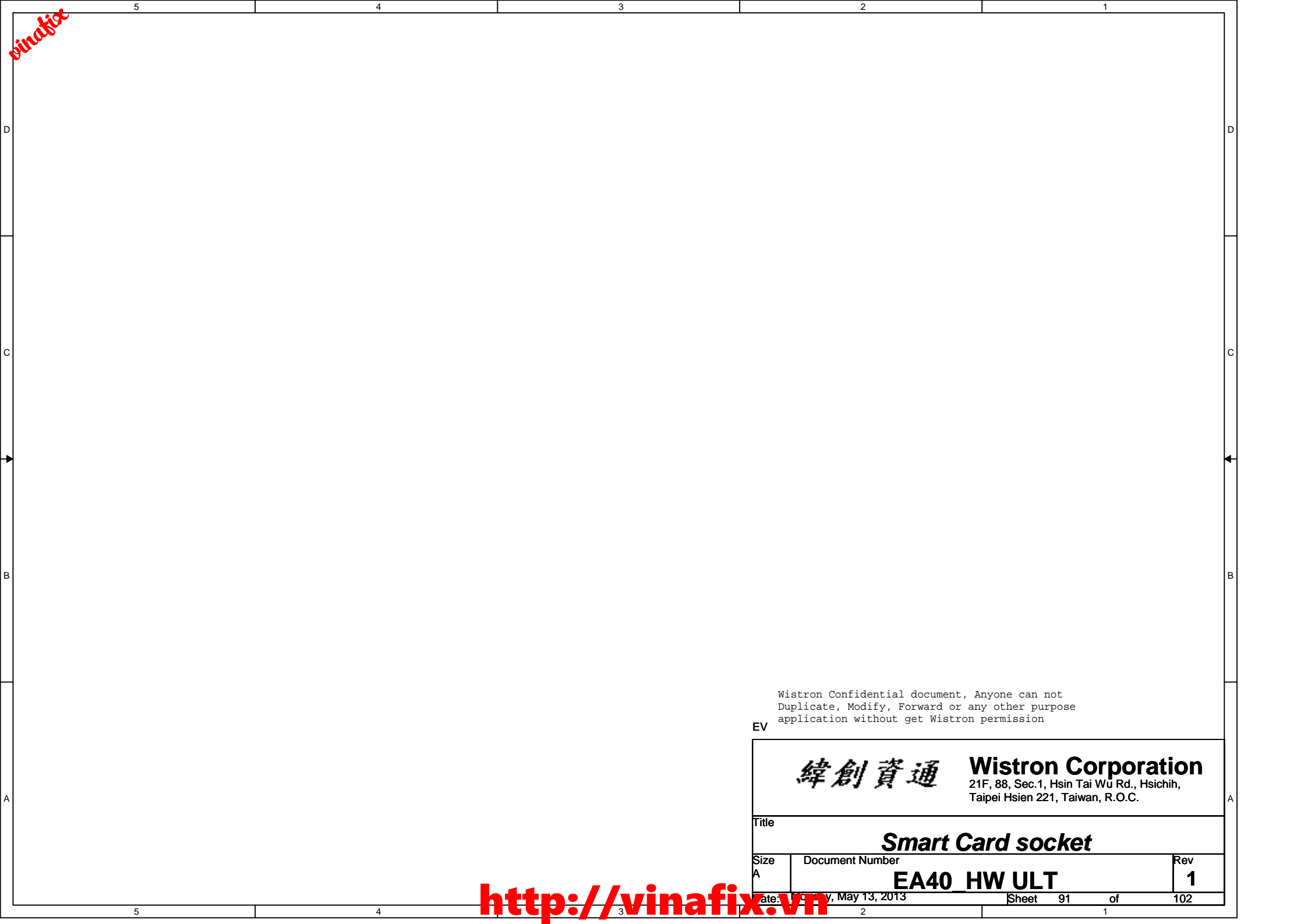
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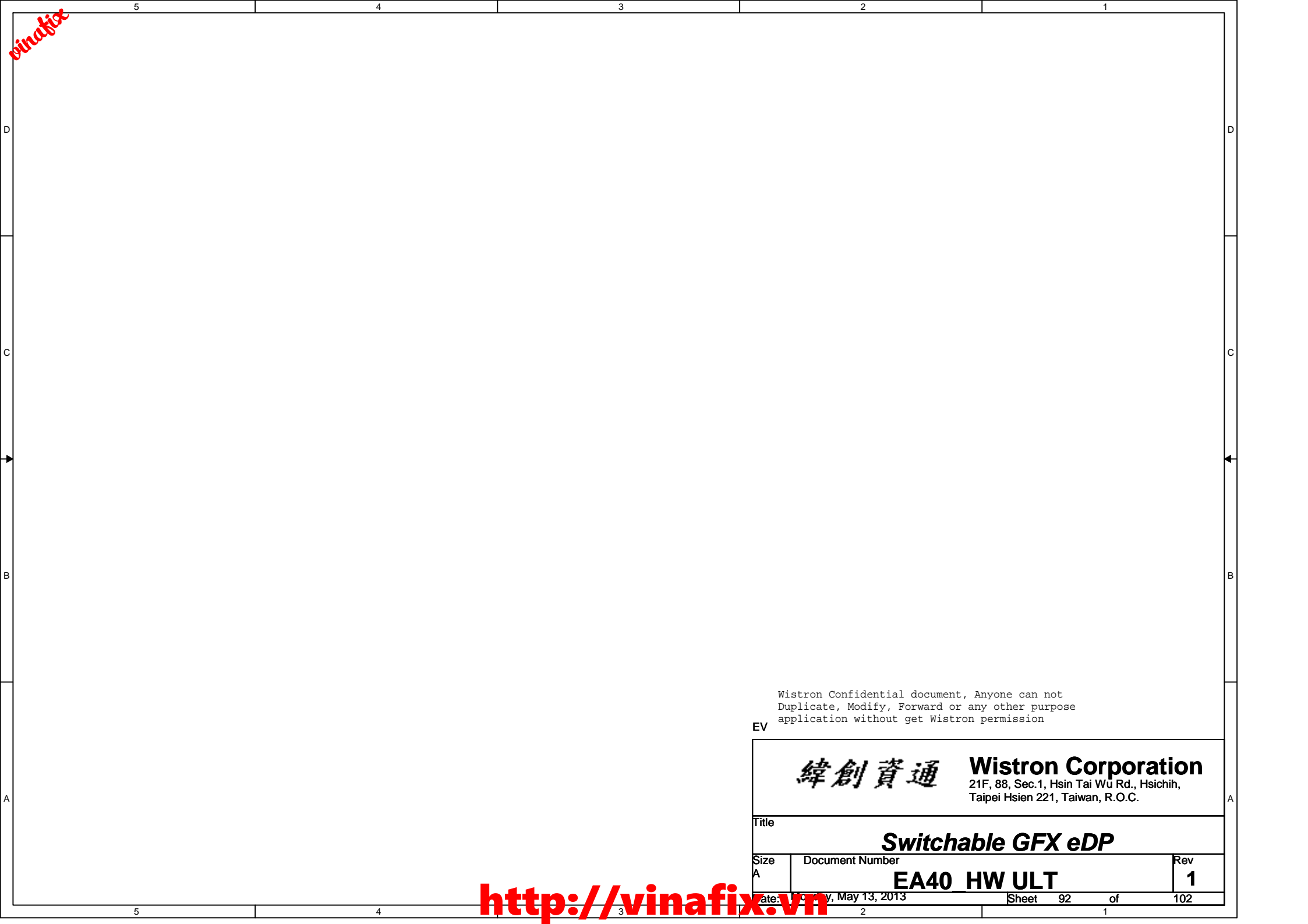
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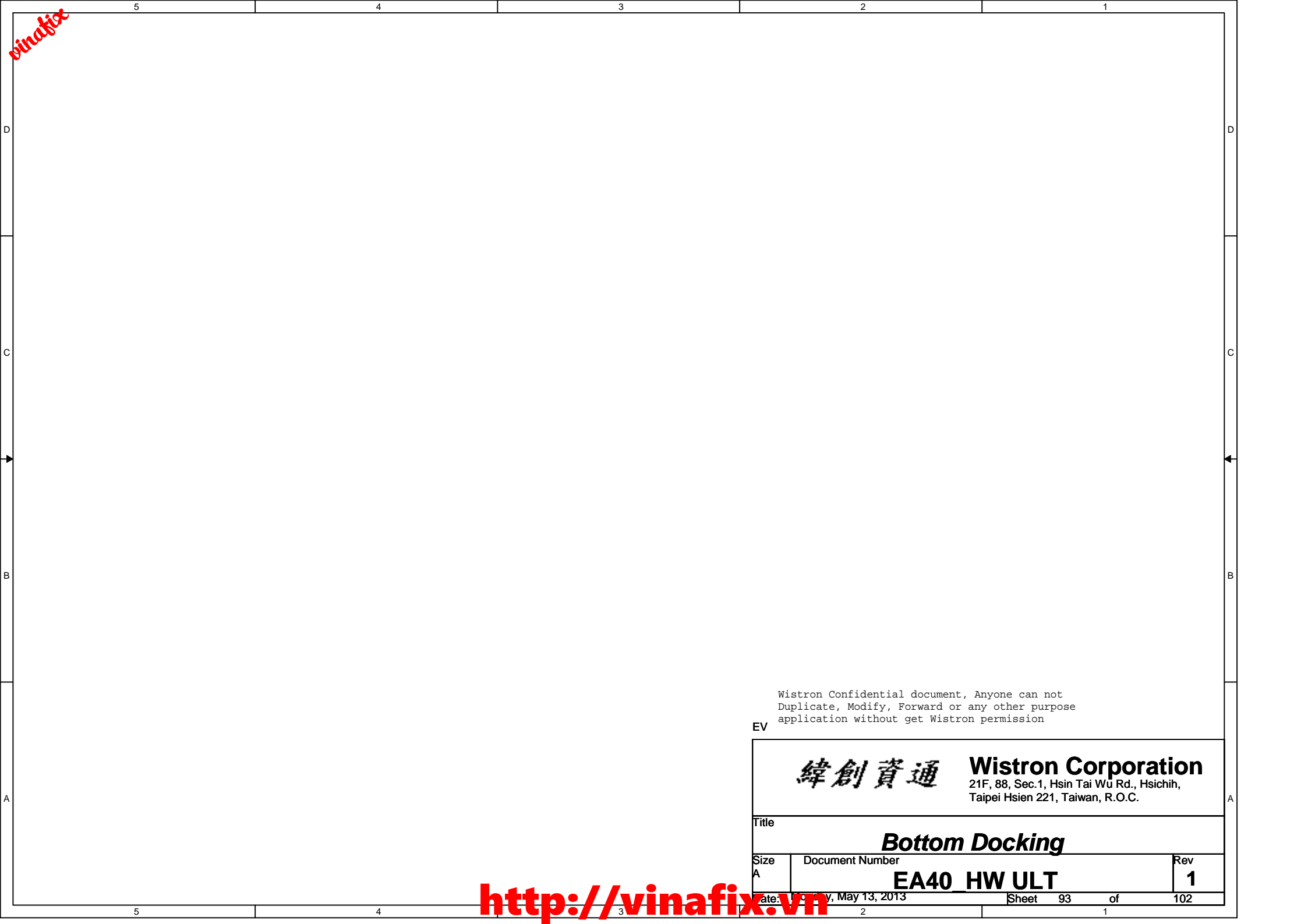
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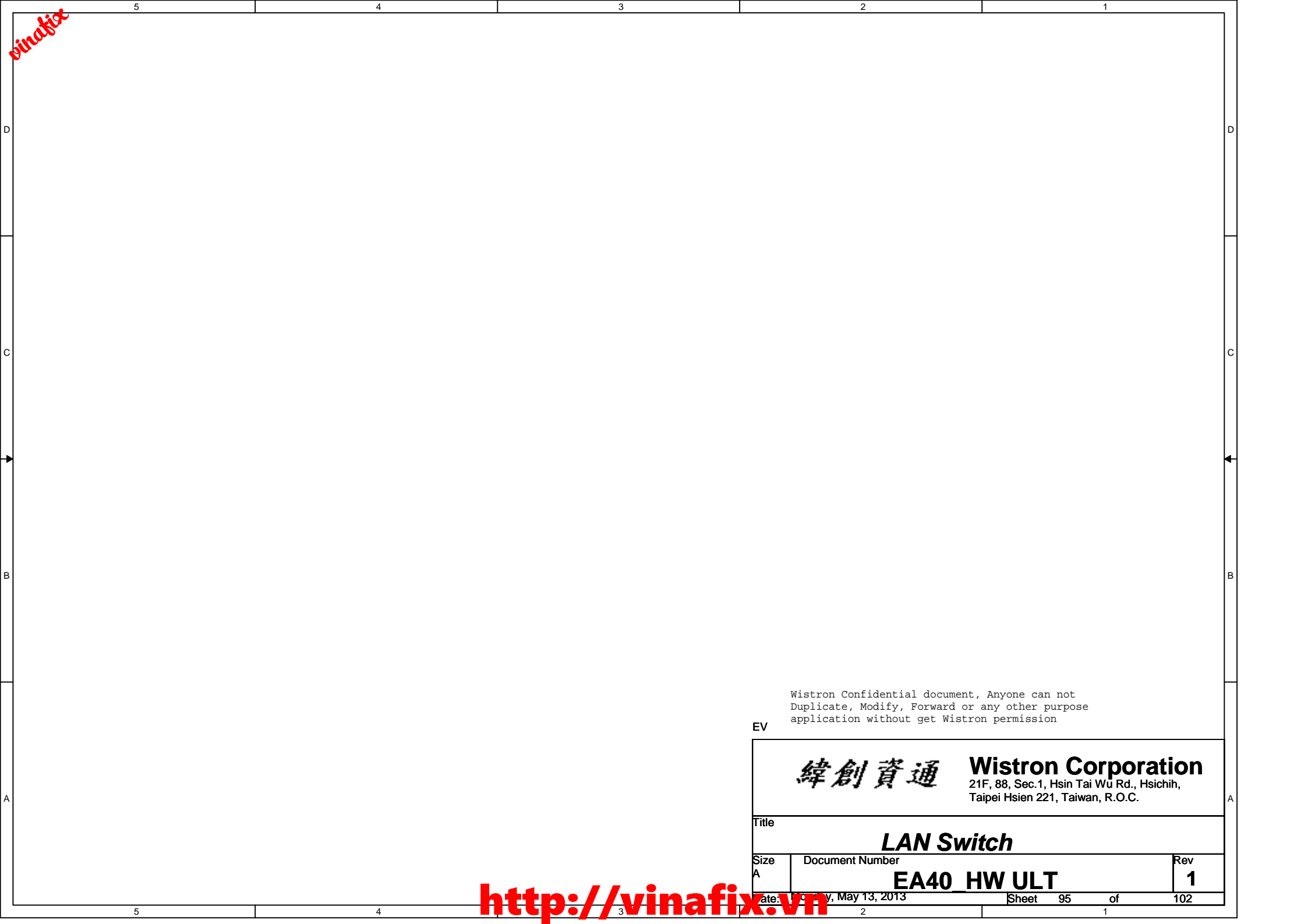
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Pin	XDP Signal Name	Target Signal	I/O	Device	Pin	XDP Signal Name	Target Signal	I/O	Device
1	OBSFN_A0	Open	I/O		2	OBSFN_A1	Open	I/O	
3	GND	GND	NA		4	OBSDATA_A[0]	Open	I/O	
5	OBSDATA_A[1]	Open	I/O		6	GND	GND	NA	
7	OBSDATA_A[2]	Open	I/O		8	OBSDATA_A[3]	Open	I/O	
9	GND	GND	NA		10	HOOK0 ¹	RSMRST#	I	System
11	HOOK1	BP_PWRGD_RST# ¹	O	System	12	HOOK2	Open	NA	
13	HOOK3	Open	NA		14	HOOK4 ¹	1.05V core	NA	
15	HOOK5	Open	NA		16	VCCOBS_AB	3.3V SUS	I	System
17	HOOK6	RSMRST# ¹	O	System	18	HOOK7	DBR# ¹	O	System
19	GND	GND	NA		20	TDO	JTAG_TDO	I	PCH
21	TRSTn	Open	NA		22	TDI	JTAG_TDI	O	PCH
23	TMS	JTAG_TMS	O	PCH	24	TCK1	Open	NA	
25	GND	GND	NA		26	TCK0	Open	NA	

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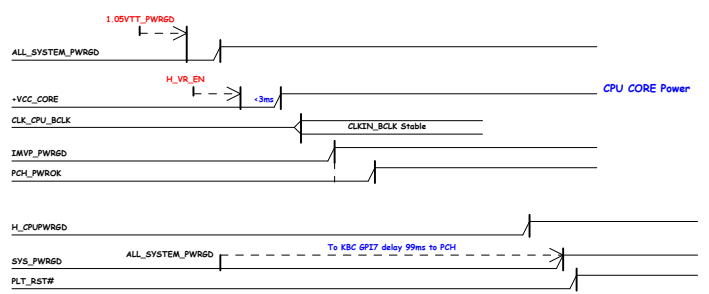
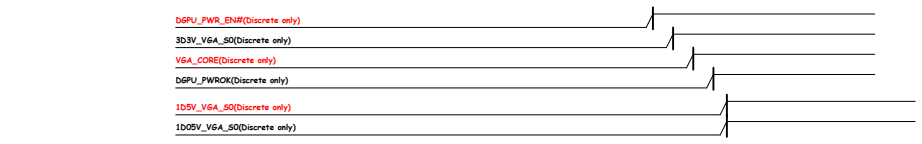
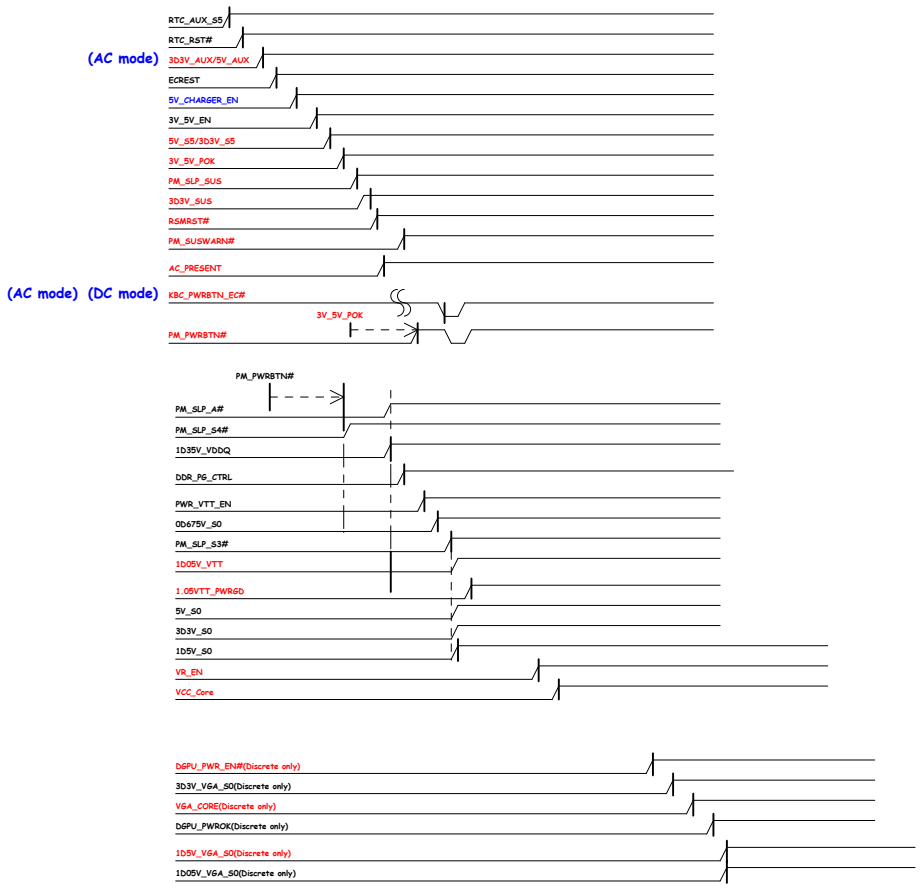
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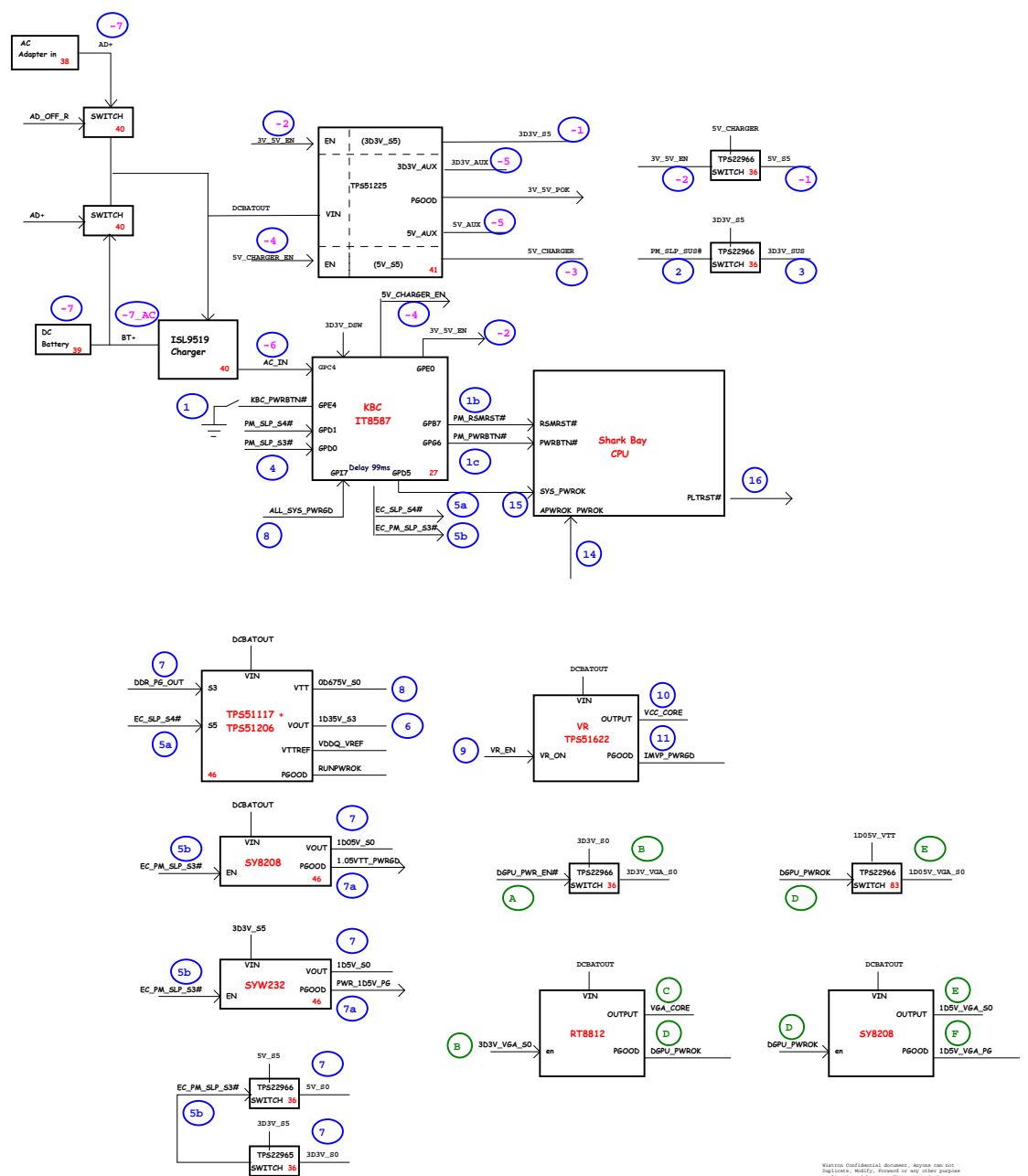
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Intel-Power Up Sequence

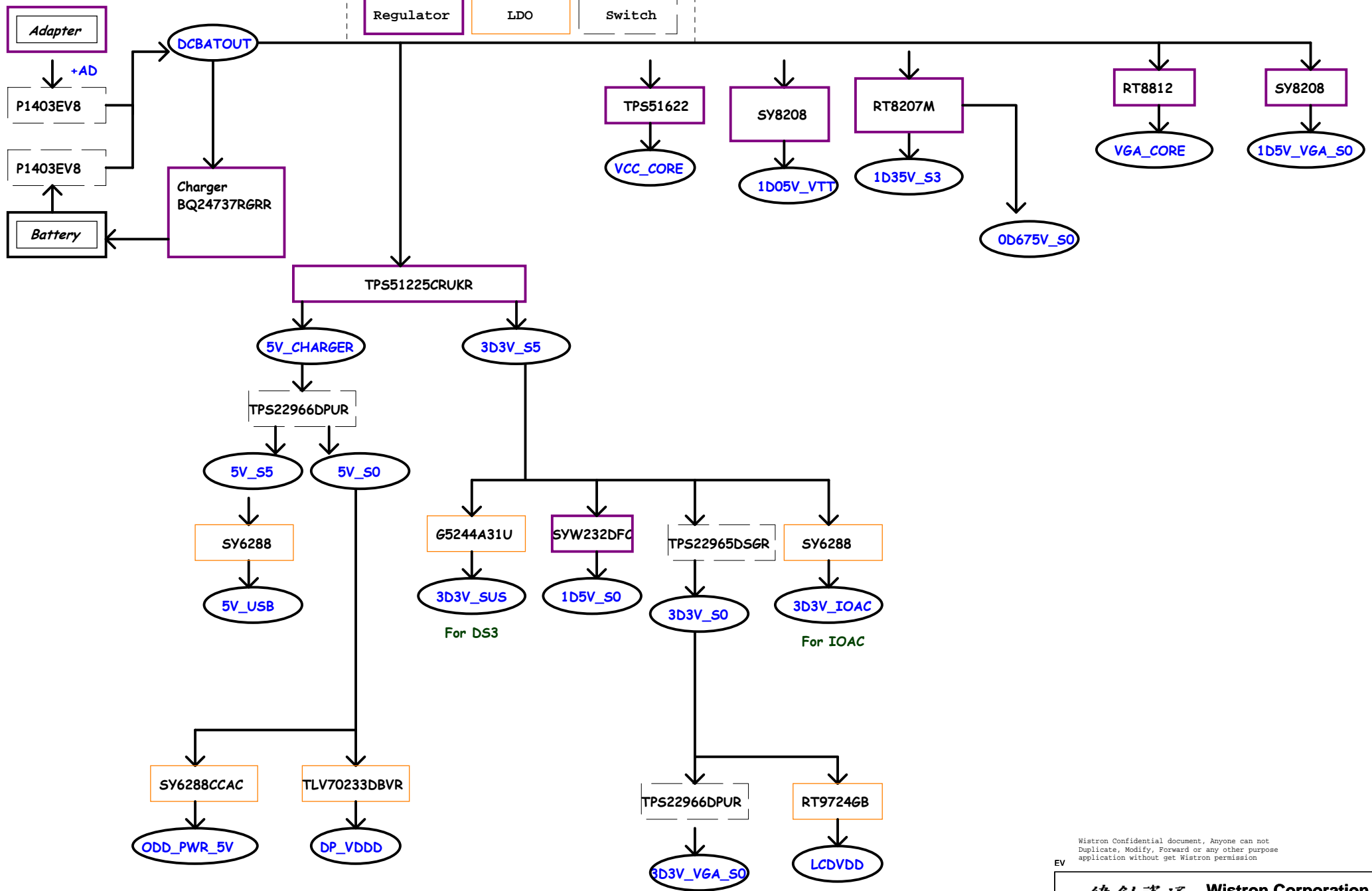


SHARK BAY POWER UP SEQUENCE DIAGRAM



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Power Shape



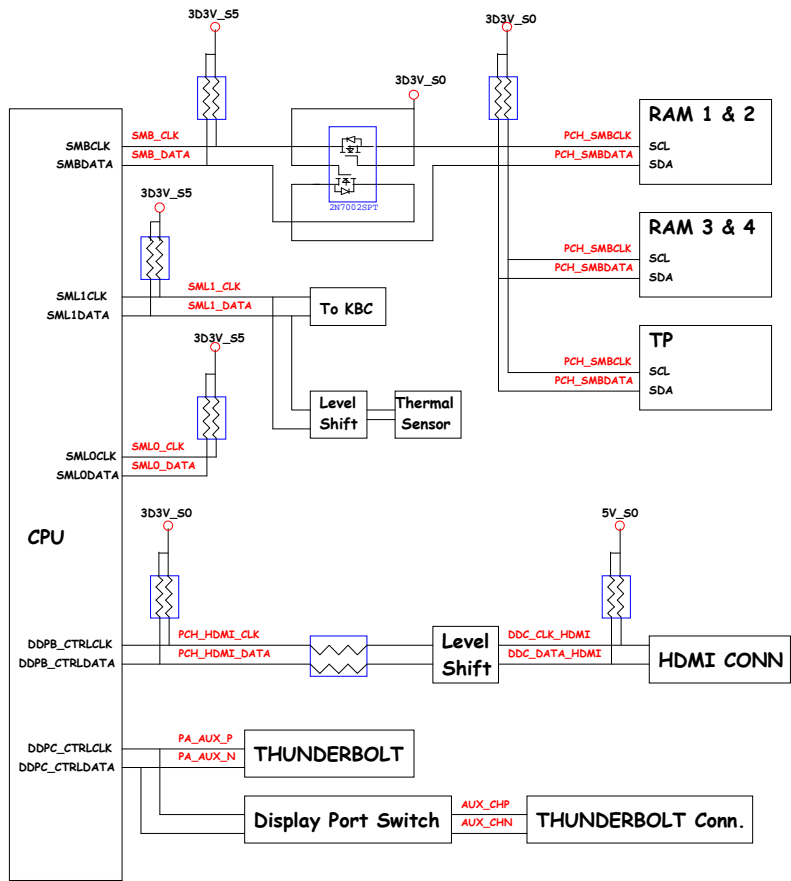
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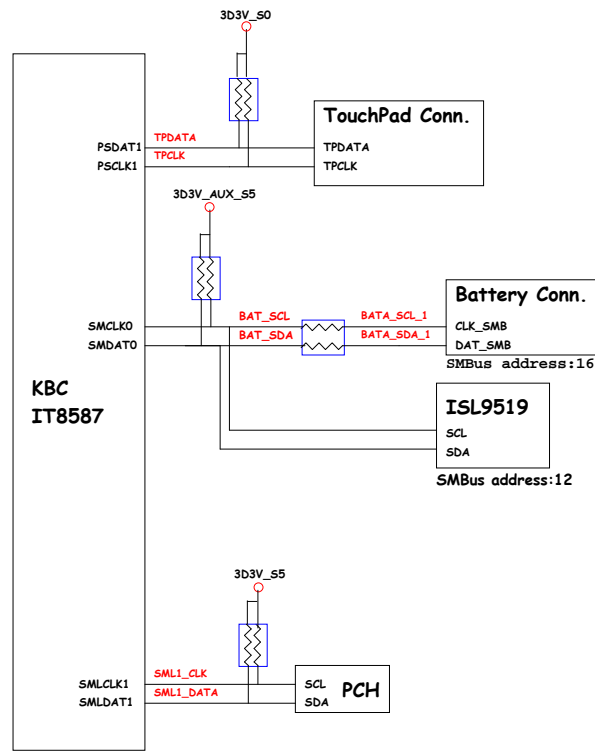
Title Power Block Diagram		
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vinafix PCH SMBus Block Diagram



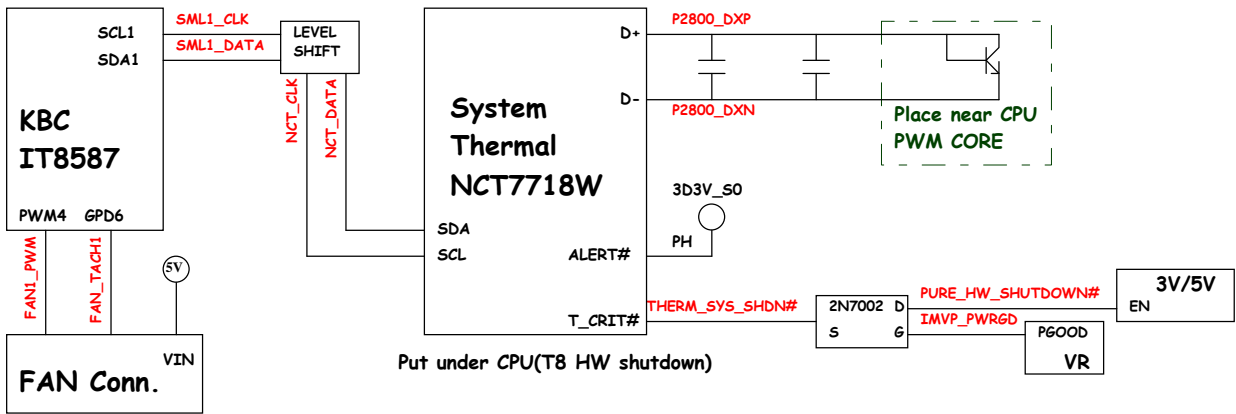
KBC SMBus Block Diagram



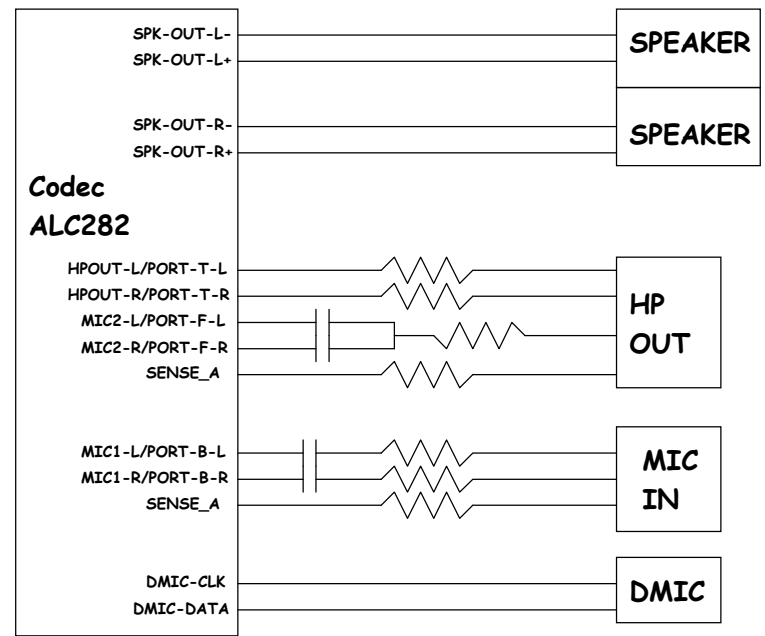
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Thermal Block Diagram



Audio Block Diagram



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