

## Features

288-pin JEDEC-compliant DIMM, 133.35 mm wide by 31.25 mm high

Operating Voltage: VDD/VDDQ = 1.2V (1.14V to 1.26V)

VPP = 2.5V (2.375V to 2.75V)

VDDSPD = 2.25V to 2.75V

I/O Type: 1.2 V signaling

On-board I<sup>2</sup>C temperature sensor with integrated Serial Presence-Detect (SPD) EEPROM

Data Transfer Rate: 21.3 Gigabytes/sec

Data Bursts: 8 and burst chop 4 mode

ZQ Calibration for Output Driver and On-Die Termination (ODT)

Programmable ODT / Dynamic ODT during Writes

Programmable CAS Latency: 10, 12, 13, 14, 15, 16, 17, 18 and 19

Bi-directional Differential Data Strobe signals

Per DRAM Addressability is supported

Write CRC is supported at all speed grades

ALERT Flag Supported

CA parity (Command/Address Parity) mode is supported

Supports ECC error correction and detection

16 Internal Banks (4 Bank Groups)

SDRAM Addressing (Row/Col/BG/BA): 17/10/2/2

Fully RoHS Compliant

## Identification

DTM68306-S 8Gx72

64G 4DRx4 PC4-2666V-L19

## Performance range

Clock / Module Speed / CL-t<sub>RCD</sub> -t<sub>RP</sub>

1333 MHz / PC4-2666 / 19-19-19

1200 MHz / PC4-2400 / 18-18-18

1200 MHz / PC4-2400 / 17-17-17

1067MHz / PC4-2133 / 16-16-16

1067MHz / PC4-2133 / 15-15-15

933 Hz / PC4-1866 / 14-14-14

933 Hz / PC4-1866 / 13-13-13

800 Hz / PC4-1600 / 12-12-12

667 MHz / PC4-1600 / 10-10-10

## Description

DTM68306-S is a load reduced 8Gx72 memory module, which conforms to JEDEC's DDR4-2666, PC4-2666 standard. The assembly is Quad-Rank containing – thirty-six Samsung 4Gbx4 DDR4-2666 DDP SDRAMs. One 4K-bit EEPROM is used for Serial Presence Detect and a Registering Clock Driver, with Address and Command Parity, is also used as well as data buffers to reduce the overall loading on the data bus.

Both output driver strength and input termination impedance are programmable to maintain signal integrity on the I/O signals in a Fly-by topology. A thermal sensor accurately monitors the DIMM module and can prevent exceeding the maximum operating temperature of 95C.

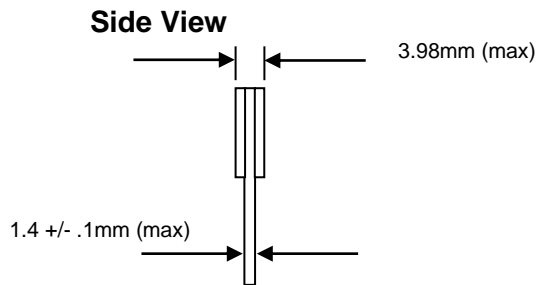
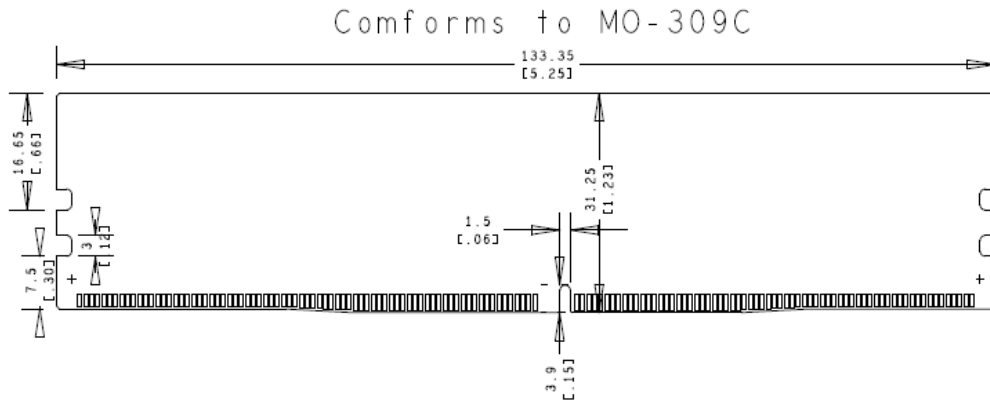
## Pin Configuration

Front Side						Back Side									
1	12V,NC	37	V <sub>SS</sub>	73	V <sub>DD</sub>	109	V <sub>SS</sub>	145	12V,NC	181	DQ29	217	V <sub>DD</sub>	253	DQ41
2	V <sub>SS</sub>	38	DQ24	74	CK0_t	110	DQS14_t	146	V <sub>REFCA</sub>	182	V <sub>SS</sub>	218	CK1_t	254	V <sub>SS</sub>
3	DQ4	39	V <sub>SS</sub>	75	CK0_c	111	DQS14_c	147	V <sub>SS</sub>	183	DQ25	219	CK1_c	255	DQS5_c
4	V <sub>SS</sub>	40	DQS12_t	76	V <sub>DD</sub>	112	V <sub>SS</sub>	148	DQ5	184	V <sub>SS</sub>	220	V <sub>DD</sub>	256	DQS5_t
5	DQ0	41	DQS12_c	77	V <sub>TT</sub>	113	DQ46	149	V <sub>SS</sub>	185	DQS3_c	221	V <sub>TT</sub>	257	V <sub>SS</sub>
6	V <sub>SS</sub>	42	V <sub>SS</sub>	78	EVENT_n	114	V <sub>SS</sub>	150	DQ1	186	DQS3_t	222	PARITY	258	DQ47
7	DQS9_t	43	DQ30	79	A0	115	DQ42	151	V <sub>SS</sub>	187	V <sub>SS</sub>	223	V <sub>DD</sub>	259	V <sub>SS</sub>
8	DQS9_c	44	V <sub>SS</sub>	80	V <sub>DD</sub>	116	V <sub>SS</sub>	152	DQS0_t	188	DQ31	224	BA1	260	DQ43
9	V <sub>SS</sub>	45	DQ26	81	BA0	117	DQ52	153	DQS0_c	189	V <sub>SS</sub>	225	A10 / AP	261	V <sub>SS</sub>
10	DQ6	46	V <sub>SS</sub>	82	RAS_n / A16	118	V <sub>SS</sub>	154	V <sub>SS</sub>	190	DQ27	226	V <sub>DD</sub>	262	DQ53
11	V <sub>SS</sub>	47	CB4	83	V <sub>DD</sub>	119	DQ48	155	DQ7	191	V <sub>SS</sub>	227	RFU	263	V <sub>SS</sub>
12	DQ2	48	V <sub>SS</sub>	84	CS0_n	120	V <sub>SS</sub>	156	V <sub>SS</sub>	192	CB5	228	WE_n / A14	264	DQ49
13	V <sub>SS</sub>	49	CB0	85	V <sub>DD</sub>	121	DQS15_t	157	DQ3	193	V <sub>SS</sub>	229	V <sub>DD</sub>	265	V <sub>SS</sub>
14	DQ12	50	V <sub>SS</sub>	86	CAS_n / A15	122	DQS15_c	158	V <sub>SS</sub>	194	CB1	230	SAVE_n,NC	266	DQS6_c
15	V <sub>SS</sub>	51	DQS17_t	87	ODT0	123	V <sub>SS</sub>	159	DQ13	195	V <sub>SS</sub>	231	V <sub>DD</sub>	267	DQS6_t
16	DQ8	52	DQS17_c	88	V <sub>DD</sub>	124	DQ54	160	V <sub>SS</sub>	196	DQS8_c	232	A13	268	V <sub>SS</sub>
17	V <sub>SS</sub>	53	V <sub>SS</sub>	89	CS1_n	125	V <sub>SS</sub>	161	DQ9	197	DQS8_t	233	V <sub>DD</sub>	269	DQ55
18	DQS10_t	54	CB6	90	V <sub>DD</sub>	126	DQ50	162	V <sub>SS</sub>	198	V <sub>SS</sub>	234	A17, NC	270	V <sub>SS</sub>
19	DQS10_c	55	V <sub>SS</sub>	91	ODT1	127	V <sub>SS</sub>	163	DQS1_c	199	CB7	235	C2,NC	271	DQ51
20	V <sub>SS</sub>	56	CB2	92	V <sub>DD</sub>	128	DQ60	164	DQS1_t	200	V <sub>SS</sub>	236	V <sub>DD</sub>	272	V <sub>SS</sub>
21	DQ14	57	V <sub>SS</sub>	93	CS2_n,C0,NC	129	V <sub>SS</sub>	165	V <sub>SS</sub>	201	CB3	237	CS3_n,C1,NC	273	DQ61
22	V <sub>SS</sub>	58	RESET_n	94	V <sub>SS</sub>	130	DQ56	166	DQ15	202	V <sub>SS</sub>	238	SA2	274	V <sub>SS</sub>
23	DQ10	59	V <sub>DD</sub>	95	DQ36	131	V <sub>SS</sub>	167	V <sub>SS</sub>	203	CKE1	239	V <sub>SS</sub>	275	DQ57
24	V <sub>SS</sub>	60	CKE0	96	V <sub>SS</sub>	132	DQS16_t	168	DQ11	204	V <sub>DD</sub>	240	DQ37	276	V <sub>SS</sub>
25	DQ20	61	V <sub>DD</sub>	97	DQ32	133	DQS16_c	169	V <sub>SS</sub>	205	RFU	241	V <sub>SS</sub>	277	DQS7_c
26	V <sub>SS</sub>	62	ACT_n	98	V <sub>SS</sub>	134	V <sub>SS</sub>	170	DQ21	206	V <sub>DD</sub>	242	DQ33	278	DQS7_t
27	DQ16	63	BG0	99	DQS13_t	135	DQ62	171	V <sub>SS</sub>	207	BG1	243	V <sub>SS</sub>	279	V <sub>SS</sub>
28	V <sub>SS</sub>	64	V <sub>DD</sub>	100	DQS13_c	136	V <sub>SS</sub>	172	DQ17	208	ALERT_n	244	DQS4_c	280	DQ63
29	DQS11_t	65	A12 / BC_n	101	V <sub>SS</sub>	137	DQ58	173	V <sub>SS</sub>	209	V <sub>DD</sub>	245	DQS4_t	281	V <sub>SS</sub>
30	DQS11_c	66	A9	102	DQ38	138	V <sub>SS</sub>	174	DQS2_c	210	A11	246	V <sub>SS</sub>	282	DQ59
31	V <sub>SS</sub>	67	V <sub>DD</sub>	103	V <sub>SS</sub>	139	SA0	175	DQS2_t	211	A7	247	DQ39	283	V <sub>SS</sub>
32	DQ22	68	A8	104	DQ34	140	SA1	176	V <sub>SS</sub>	212	V <sub>DD</sub>	248	V <sub>SS</sub>	284	V <sub>DDSPD</sub>
33	V <sub>SS</sub>	69	A6	105	V <sub>SS</sub>	141	SCL	177	DQ23	213	A5	249	DQ35	285	SDA
34	DQ18	70	V <sub>DD</sub>	106	DQ44	142	V <sub>PP</sub>	178	V <sub>SS</sub>	214	A4	250	V <sub>SS</sub>	286	V <sub>PP</sub>
35	V <sub>SS</sub>	71	A3	107	V <sub>SS</sub>	143	V <sub>PP</sub>	179	DQ19	215	V <sub>DD</sub>	251	DQ45	287	V <sub>PP</sub>
36	DQ28	72	A1	108	DQ40	144	RFU	180	V <sub>SS</sub>	216	A2	252	V <sub>SS</sub>	288	V <sub>PP</sub>

## PIN DESCRIPTION

Name	Function
CB[7:0]	Data Check Bits
DQ[63:0]	Data Bits
DQS[17:0]_t, DQS[17:0]_c	Differential Data Strobes
CK_t[1:0], CK_c[1:0]	Differential Clock Inputs
CKE[1:0]	Clock Enables
CAS_n / A15	Multiplexed: Column Address Strobe or Address 15
RAS_n / A16	Multiplexed: Row Address Strobe or Address 16
CS[3:0]_n	Chip Selects
ACT_n	Activate Command Input
WE_n / A14	Multiplexed: Write Enable or Address 14
C[2:0]	Chip ID Inputs
A[17:0]	Address Inputs
BA[1:0]	Bank Address select Inputs
BG[1:0]	Bank Group select Inputs
ODT[1:0]	On Die Termination Inputs
SA[2:0]	SPD Address
SCL	SPD Clock Input
SDA	SPD Data Input/Output
EVENT_n	Temperature Sensing
RESET_n	Reset for register and DRAMs
PARITY	Parity bit input for Addr/Ctrl
ALERT_n	CRC Error Flag or CMD/Addr Parity Flag Output
A12 / BC_n	Combination Input: Address12/Burst Chop
A10 / AP	Combination Input: Addr10/Auto-precharge
12V*	Optional Power Supply*
V <sub>PP</sub>	Charge Pump Power
V <sub>SS</sub>	Ground
V <sub>DD</sub>	Power
V <sub>DDSPD</sub>	SPD EEPROM Power
V <sub>REFCA</sub>	Reference Voltage for CA
V <sub>TT</sub>	Termination Voltage
NC	No Connection
RFU	Reserved for Future Use

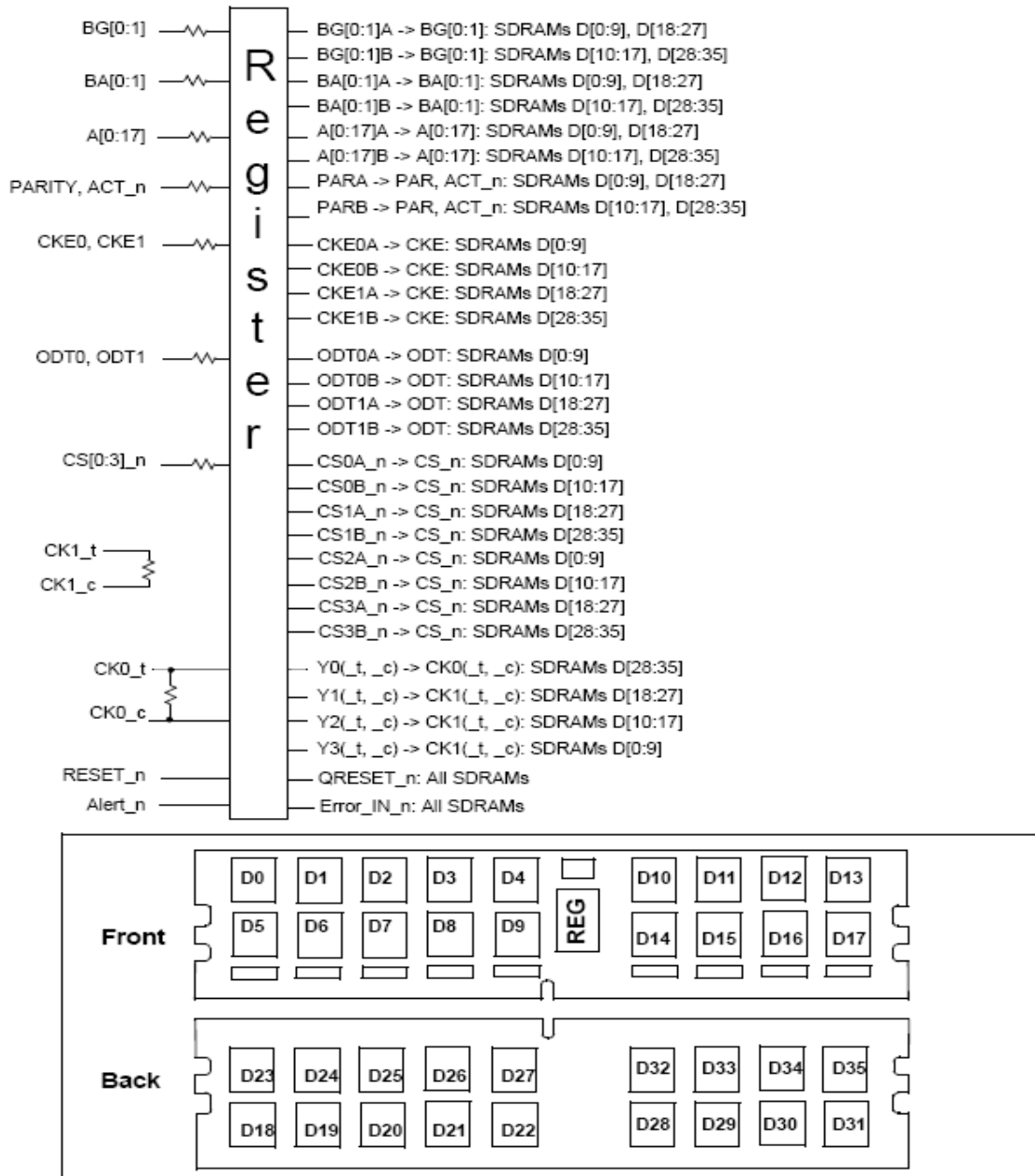
\* Not used



**Notes:**

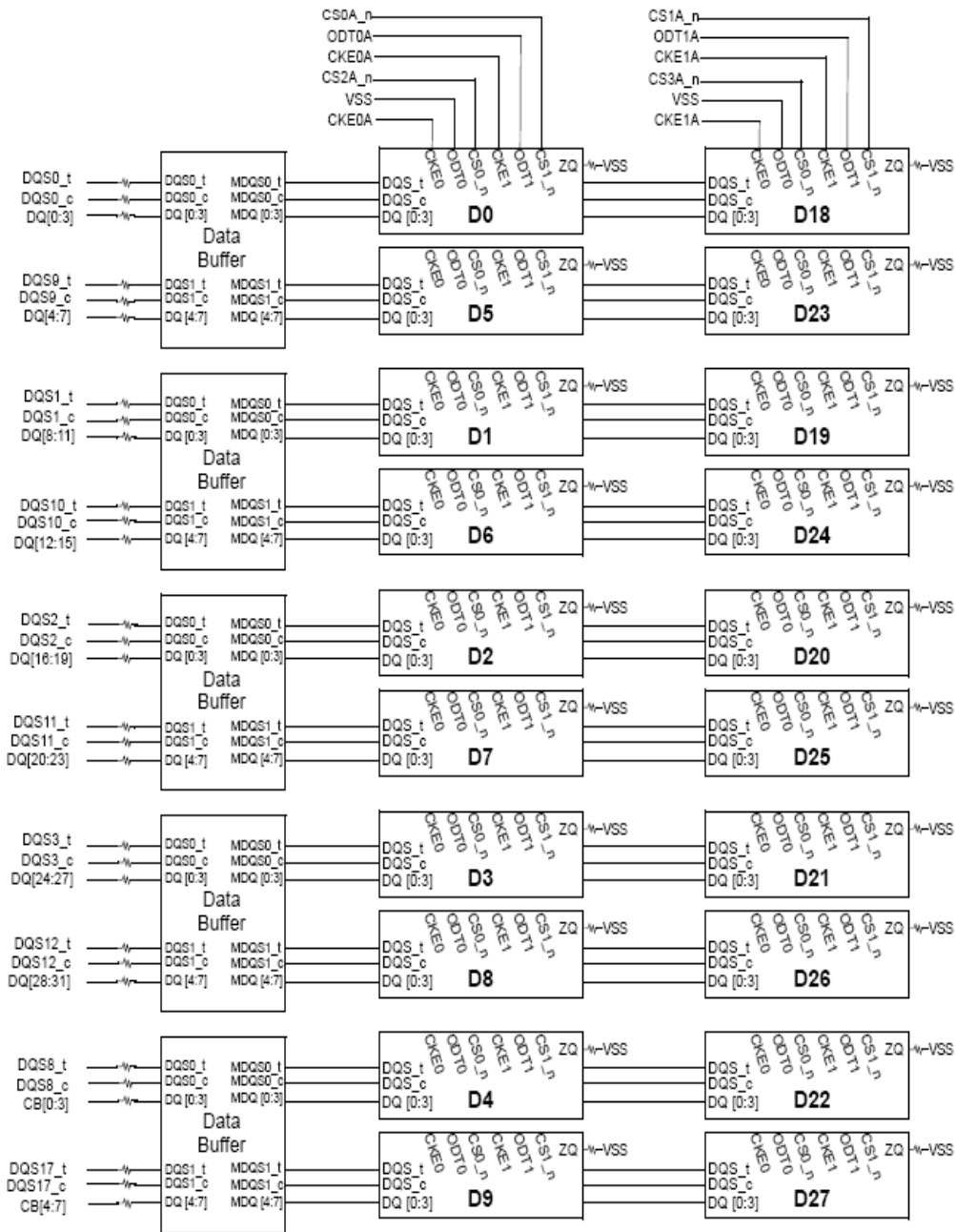
1. Tolerances on all dimensions except where otherwise indicated are  $\pm .13$ . Reference JEDEC standard MO-309C.
2. All dimensions are expressed: millimeters [inches]

## Functional Diagram



### Notes:

1. CK0\_t, CK0\_c terminated with 120Ω ± 5% resistor.
2. CK1\_t, CK1\_c terminated with 120Ω ± 5% resistor but not used.
3. Unless otherwise noted resistors are 22Ω ± 5%.



**Notes:**

1. ZQ resistors are 240Ω ±1%. For all other resistor values refer to the appropriate wiring diagram.
2. See the Net Structure diagrams for all resistors associated with the command, address and control bus.
3. TEN Pin of SDRAMs is tied to VSS
4. DQ stub resistors are 15Ω ±5%. For all other resistor values refer to the appropriate wiring diagram.



# DTM68306B

64GB - 288-Pin 4Rx4 Load Reduced ECC DDR4  
LRDIMM

---



DATARAM Memory, USA Corporate Headquarters, P.O. Box 7528, Princeton, NJ 08543-7528;  
Voice: 609-799-0071, Fax: 609-799-6734; [www.dataram.com](http://www.dataram.com)

All rights reserved.

The information contained in this document has been carefully checked and is believed to be reliable. However, Dataram assumes no responsibility for inaccuracies.

The information contained in this document does not convey any license under the copyrights, patent rights or trademarks claimed and owned by Dataram.

No part of this publication may be copied or reproduced in any form or by any means, or transferred to any third party without prior written consent of Dataram.