DTM68132-H

32GB - 288-Pin 2Rx4 Registered ECC DDR4 DIMM

Features

- 288-pin JEDEC-compliant DIMM, 133.35 mm wide by 31.25 mm high
- Operating Voltage: VDD/VDDQ = 1.2V (1.14V to 1.26V)
- VPP = 2.5V (2.375V to 2.75V)
- VDDSPD = 2.25V to 2.75V
- I/O Type: 1.2 V signaling
- On-board I^2C temperature sensor with integrated Serial Presence-Detect (SPD) EEPROM
- Data Transfer Rate: 21.3 Gigabytes/sec
- Data Bursts: 8 and burst chop 4 mode
- ZQ Calibration for Output Driver and On-Die Termination (ODT)
- Programmable ODT / Dynamic ODT during Writes
- Programmable CAS Latency: 10, 12, 13, 14, 15, 16, 17, 18 and 19
- Bi-directional Differential Data Strobe signals
- Per DRAM Addressability is supported
- Write CRC is supported at all speed grades
- DBI (Data Bus Inversion) is supported(x8 only)
- CA parity (Command/Address Parity) mode is supported
- Supports ECC error correction and detection
- 16 internal banks
- SDRAM Addressing (Row/Col/BG/BA): 17/10/2/2
- Fully RoHS Compliant

Identification

DTM68132-H 4Gx72
32G 2Rx4 PC4-2666V-R19

Performance range

Clock / Module Speed / CL-t_{RCD} -t_{RP}
1333 MHz / PC4-2666 / 19-19-19
1200 MHz / PC4-2400 / 18-18-18
1200 MHz / PC4-2400 / 17-17-17
1067MHz / PC4-2133 / 16-16-16
1067MHz / PC4-2133 / 15-15-15
933 Hz / PC4-1866 / 14-14-14
933 Hz / PC4-1866 / 13-13-13
800 Hz / PC4-1600 / 12-12-12
667 MHz / PC4-1600 / 10-10-10

Description

DTM68132-H is a registered 4Gx72 memory module, which conforms to JEDEC's PC4-2666 standard. The assembly is Dual-Rank with each rank containing of eighteen SKHynix 2Gbx4 DDR4-2666 SDRAMs. One 4K-bit EEPROM is used for Serial Presence Detect and a combination register/PLL, with Address and Command Parity, is also used.

Both output driver strength and input termination impedance are programmable to maintain signal integrity on the I/O signals in a Fly-by topology. A thermal sensor accurately monitors the DIMM module and can prevent exceeding the maximum operating temperature of 95C.

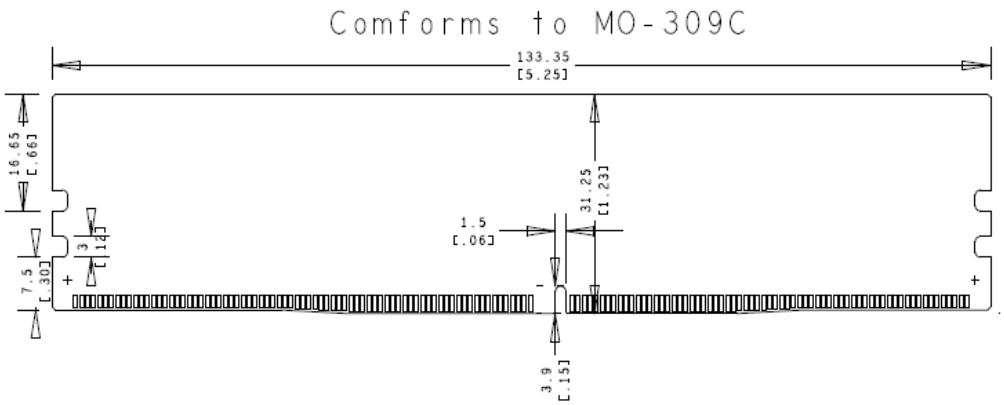
Pin Configuration

Front Side								Back Side							
1	12V,NC	37	V_{SS}	73	V_{DD}	109	V_{SS}	145	12V,NC	181	DQ29	217	V_{DD}	253	DQ41
2	V_{SS}	38	DQ24	74	CK0_t	110	DQS14_t	146	V_{REFCA}	182	V_{SS}	218	CK1_t	254	V_{SS}
3	DQ4	39	V_{SS}	75	CK0_c	111	DQS14_c	147	V_{SS}	183	DQ25	219	CK1_c	255	DQS5_c
4	V_{SS}	40	DQS12_t	76	V_{DD}	112	V_{SS}	148	DQ5	184	V_{SS}	220	V_{DD}	256	DQS5_t
5	DQ0	41	DQS12_c	77	V_{TT}	113	DQ46	149	V_{SS}	185	DQS3_c	221	V_{TT}	257	V_{SS}
6	V_{SS}	42	V_{SS}	78	EVENT_n	114	V_{SS}	150	DQ1	186	DQS3_t	222	PARITY	258	DQ47
7	DQS9_t	43	DQ30	79	A0	115	DQ42	151	V_{SS}	187	V_{SS}	223	V_{DD}	259	V_{SS}
8	DQS9_c	44	V_{SS}	80	V_{DD}	116	V_{SS}	152	DQS0_t	188	DQ31	224	BA1	260	DQ43
9	V_{SS}	45	DQ26	81	BA0	117	DQ52	153	DQS0_c	189	V_{SS}	225	A10 / AP	261	V_{SS}
10	DQ6	46	V_{SS}	82	RAS_n / A16	118	V_{SS}	154	V_{SS}	190	DQ27	226	V_{DD}	262	DQ53
11	V_{SS}	47	CB4	83	V_{DD}	119	DQ48	155	DQ7	191	V_{SS}	227	RFU	263	V_{SS}
12	DQ2	48	V_{SS}	84	CS0_n	120	V_{SS}	156	V_{SS}	192	CB5	228	WE_n / A14	264	DQ49
13	V_{SS}	49	CB0	85	V_{DD}	121	DQS15_t	157	DQ3	193	V_{SS}	229	V_{DD}	265	V_{SS}
14	DQ12	50	V_{SS}	86	CAS_n / A15	122	DQS15_c	158	V_{SS}	194	CB1	230	SAVE_n,NC	266	DQS6_c
15	V_{SS}	51	DQS17_t	87	ODT0	123	V_{SS}	159	DQ13	195	V_{SS}	231	V_{DD}	267	DQS6_t
16	DQ8	52	DQS17_c	88	V_{DD}	124	DQ54	160	V_{SS}	196	DQS8_c	232	A13	268	V_{SS}
17	V_{SS}	53	V_{SS}	89	CS1_n	125	V_{SS}	161	DQ9	197	DQS8_t	233	V_{DD}	269	DQ55
18	DQS10_t	54	CB6	90	V_{DD}	126	DQ50	162	V_{SS}	198	V_{SS}	234	A17, NC	270	V_{SS}
19	DQS10_c	55	V_{SS}	91	ODT1	127	V_{SS}	163	DQS1_c	199	CB7	235	C2,NC	271	DQ51
20	V_{SS}	56	CB2	92	V_{DD}	128	DQ60	164	DQS1_t	200	V_{SS}	236	V_{DD}	272	V_{SS}
21	DQ14	57	V_{SS}	93	CS2_n,C0,NC	129	V_{SS}	165	V_{SS}	201	CB3	237	CS3_n,C1,NC	273	DQ61
22	V_{SS}	58	RESET_n	94	V_{SS}	130	DQ56	166	DQ15	202	V_{SS}	238	SA2	274	V_{SS}
23	DQ10	59	V_{DD}	95	DQ36	131	V_{SS}	167	V_{SS}	203	CKE1	239	V_{SS}	275	DQ57
24	V_{SS}	60	CKE0	96	V_{SS}	132	DQS16_t	168	DQ11	204	V_{DD}	240	DQ37	276	V_{SS}
25	DQ20	61	V_{DD}	97	DQ32	133	DQS16_c	169	V_{SS}	205	RFU	241	V_{SS}	277	DQS7_c
26	V_{SS}	62	ACT_n	98	V_{SS}	134	V_{SS}	170	DQ21	206	V_{DD}	242	DQ33	278	DQS7_t
27	DQ16	63	BG0	99	DQS13_t	135	DQ62	171	V_{SS}	207	BG1	243	V_{SS}	279	V_{SS}
28	V_{SS}	64	V_{DD}	100	DQS13_c	136	V_{SS}	172	DQ17	208	ALERT_n	244	DQS4_c	280	DQ63
29	DQS11_t	65	A12 / BC_n	101	V_{SS}	137	DQ58	173	V_{SS}	209	V_{DD}	245	DQS4_t	281	V_{SS}
30	DQS11_c	66	A9	102	DQ38	138	V_{SS}	174	DQS2_c	210	A11	246	V_{SS}	282	DQ59
31	V_{SS}	67	V_{DD}	103	V_{SS}	139	SA0	175	DQS2_t	211	A7	247	DQ39	283	V_{SS}
32	DQ22	68	A8	104	DQ34	140	SA1	176	V_{SS}	212	V_{DD}	248	V_{SS}	284	V_{DDSPD}
33	V_{SS}	69	A6	105	V_{SS}	141	SCL	177	DQ23	213	A5	249	DQ35	285	SDA
34	DQ18	70	V_{DD}	106	DQ44	142	V_{PP}	178	V_{SS}	214	A4	250	V_{SS}	286	V_{PP}
35	V_{SS}	71	A3	107	V_{SS}	143	V_{PP}	179	DQ19	215	V_{DD}	251	DQ45	287	V_{PP}
36	DQ28	72	A1	108	DQ40	144	RFU	180	V_{SS}	216	A2	252	V_{SS}	288	V_{PP}

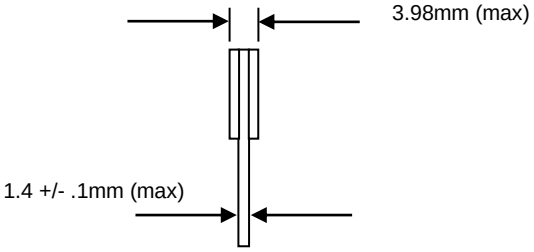
PIN DESCRIPTION

Name	Function
CB[7:0]	Data Check Bits
DQ[63:0]	Data Bits
DQS[17:0]_t, DQS[17:0]_c	Differential Data Strobes
CK_t[1:0], CK_c[1:0]	Differential Clock Inputs
CKE[1:0]	Clock Enables
CAS_n / A15	Multiplexed: Column Address Strobe or Address 15
RAS_n / A16	Multiplexed: Row Address Strobe or Address 16
CS[3:0]_n	Chip Selects
ACT_n	Activate Command Input
WE_n / A14	Multiplexed: Write Enable or Address 14
C[2:0]	Chip ID Inputs
A[17:0]	Address Inputs
BA[1:0]	Bank Address select Inputs
BG[1:0]	Bank Group select Inputs
ODT[1:0]	On Die Termination Inputs
SA[2:0]	SPD Address
SCL	SPD Clock Input
SDA	SPD Data Input/Output
EVENT_n	Temperature Sensing
RESET_n	Reset for register and DRAMs
PARITY	Parity bit input for Addr/Ctrl
ALERT_n	CRC Error Flag or CMD/Addr Parity Flag Output
A12 / BC_n	Combination Input: Address12/Burst Chop
A10 / AP	Combination Input: Addr10/Auto-precharge
12V*	Optional Power Supply*
V_{PP}	Charge Pump Power
V_{SS}	Ground
V_{DD}	Power
V_{DDSPD}	SPD EEPROM Power
V_{REFCA}	Reference Voltage for CA
V_{TT}	Termination Voltage
NC	No Connection
RFU	Reserved for Future Use

* Not used



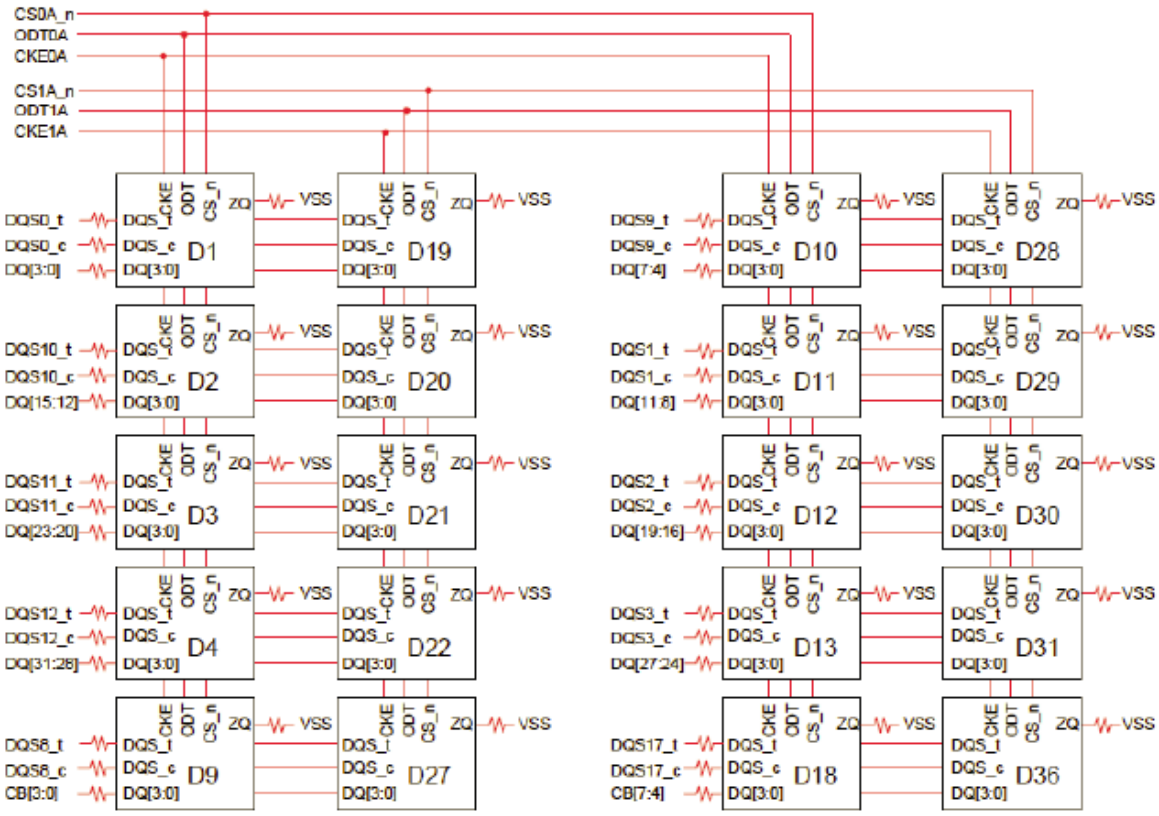
Side View

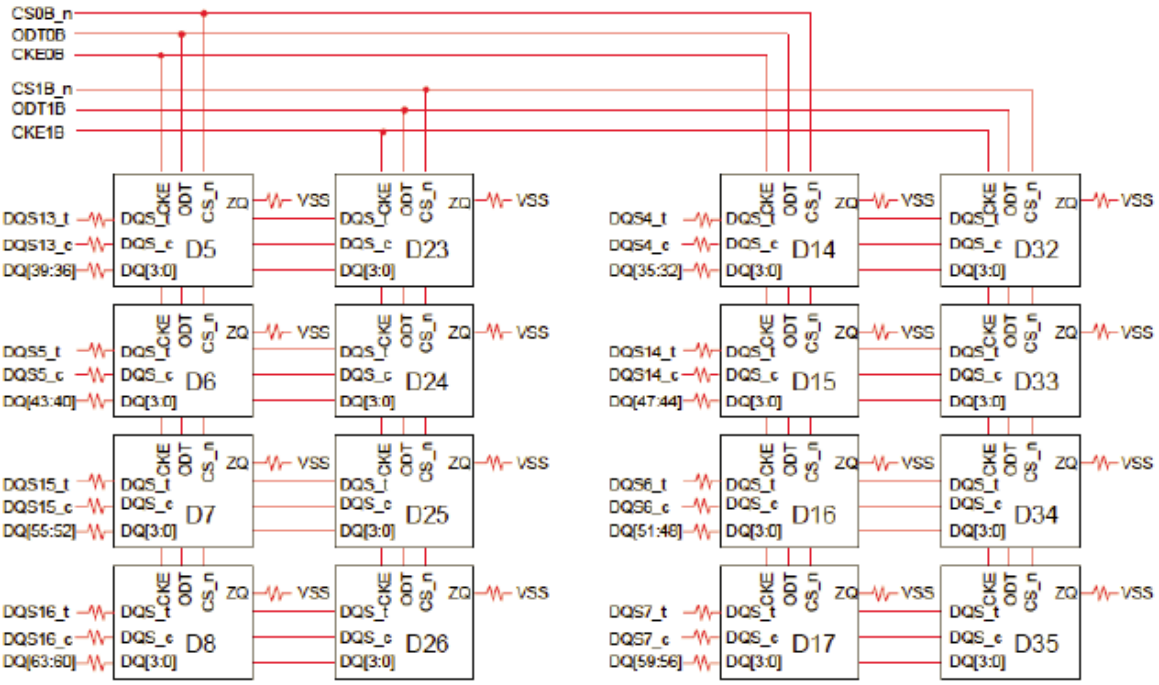


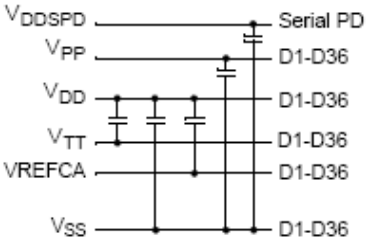
Notes:

1. Tolerances on all dimensions except where otherwise indicated are ±.13. Reference JEDEC standard MO-309C.
2. All dimensions are expressed: millimeters [inches]

Functional Diagram

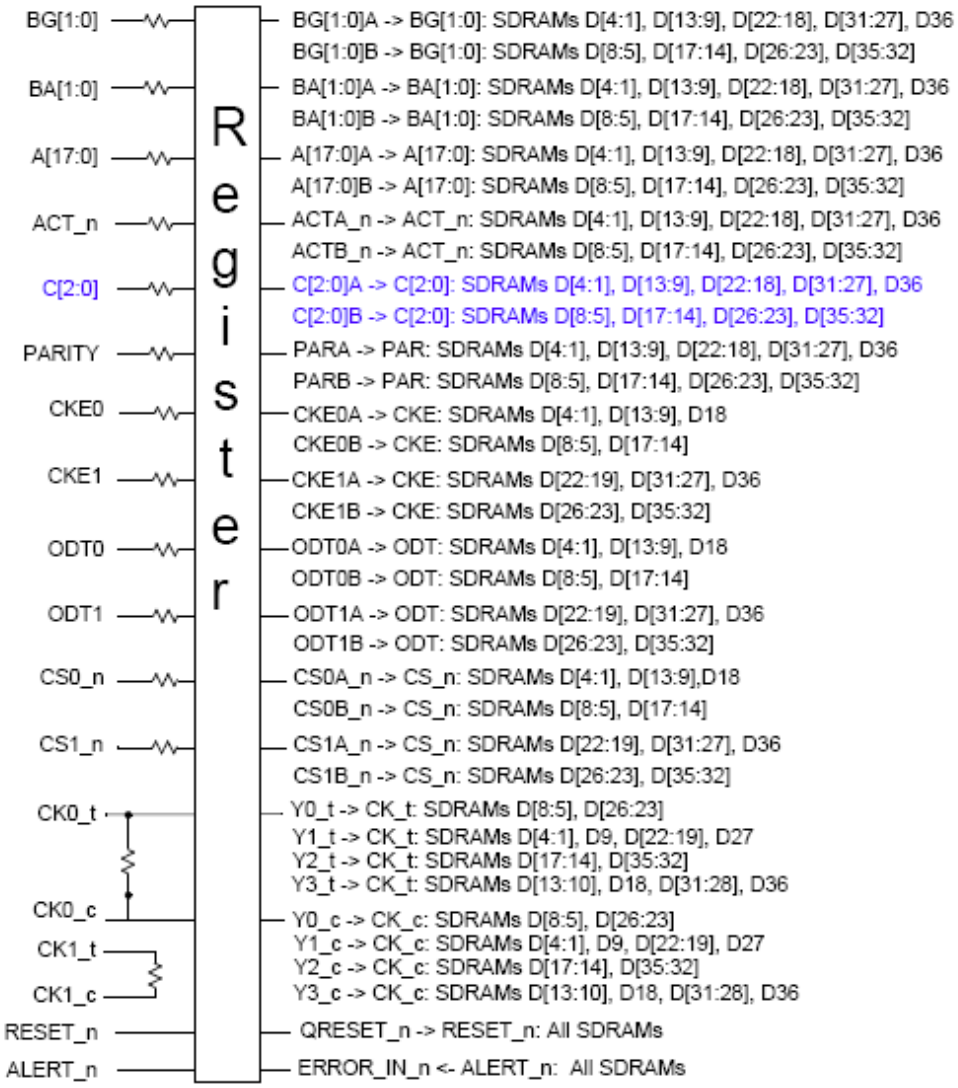






Notes:

1. Unless otherwise noted, resistor values are 15Ω ± 5%.
2. See the Net Structure diagrams for all resistors associated with the command, address and control bus.
3. ZQ resistors are 240Ω ±1%. For all other resistor values refer to the appropriate wiring diagram.
4. TEN pin of SDRAMs is tied to VSS.



Notes:

1. CK0_t, CK0_c terminated with 120Ω ± 5% resistor.
2. CK1_t, CK1_c terminated with 120Ω ± 5% resistor but not used.
3. Unless otherwise noted resistors are 22Ω ± 5%.
4. Register input CS1_n is tied to VDD. Register inputs ODT1 and CKE1 are tied to VSS.

DATARAM Memory, USA Corporate Headquarters, P.O. Box 7528, Princeton, NJ 08543-7528;
Voice: 609-799-0071, Fax: 609-799-6734; www.dataram.com