

Features

288-pin JEDEC-compliant DIMM, 133.35 mm wide by 31.25 mm high

Operating Voltage: VDD/VDDQ = 1.2V (1.14V to 1.26V)

VPP = 2.5V (2.375V to 2.75V)

VDDSPD = 2.25V to 2.75V

I/O Type: 1.2 V signaling

On-board I²C temperature sensor with integrated Serial Presence-Detect (SPD) EEPROM

Data Transfer Rate: 21.3 Gigabytes/sec

Data Bursts: 8 and burst chop 4 mode

ZQ Calibration for Output Driver and On-Die Termination (ODT)

Programmable ODT / Dynamic ODT during Writes

Programmable CAS Latency: 10, 12, 13, 14, 15, 16, 17, 18 and 19

Bi-directional Differential Data Strobe signals

Per DRAM Addressability is supported

Write CRC is supported at all speed grades

DBI (Data Bus Inversion) is supported(x8 only)

CA parity (Command/Address Parity) mode is supported

Supports ECC error correction and detection

16 internal banks

SDRAM Addressing (Row/Col/BG/BA): 16/10/2/2

Fully RoHS Compliant

Identification

DTM68127-H 1Gx72

8GB 1Rx8 PC4-2666V-R19

Performance range

Clock / Module Speed / CL-t_{RCD} -t_{RP}

1333 MHz / PC4-2666 / 19-19-19

1200 MHz / PC4-2400 / 18-18-18

1200 MHz / PC4-2400 / 17-17-17

1067MHz / PC4-2133 / 16-16-16

1067MHz / PC4-2133 / 15-15-15

933 Hz / PC4-1866 / 14-14-14

933 Hz / PC4-1866 / 13-13-13

800 Hz / PC4-1600 / 12-12-12

667 MHz / PC4-1600 / 10-10-10

Description

DTM68127-H is a registered 1Gx72 memory module, which conforms to JEDEC's PC4-2666 standard. The assembly is Single-Rank with a rank containing: nine SKHynix 1Gbx8 DDR4-2666 SDRAMs. One 4K-bit EEPROM is used for Serial Presence Detect and a combination register/PLL, with Address and Command Parity is also used.

Both output driver strength and input termination impedance are programmable to maintain signal integrity on the I/O signals in a Fly-by topology. A thermal sensor accurately monitors the DIMM module and can prevent exceeding the maximum operating temperature of 95C.

Speed Bin Table

Speed Bin			DDR4-2666V		Unit	NOTE
CL-nRCD-nRP			19-19-19			
Parameter	Symbol		min	max		
Internal read command to first data	tAA		14.25 ¹³ (13.75) ^{5,11}	18.00	ns	11
Internal read command to first data with read DBI enabled	tAA_DBI		tAA(min) + 3nCK	tAA(max) + 3nCK	ns	11
ACT to internal read or write delay time	tRCD		14.25 ¹³ (13.75) ^{5,11}	-	ns	11
PRE command period	tRP		14.25 ¹³ (13.75) ^{5,11}	-	ns	11
ACT to PRE command period	tRAS		32	9 x tREFI	ns	11
ACT to ACT or REF command period	tRC		46.25 (45.75) ^{5,11}	-	ns	11
	Normal	Read DBI				
CWL = 9	CL = 9	CL = 11	tCK(AVG)	Reserved	ns	1,2,3,4,10
	CL = 10	CL = 12	tCK(AVG)	1.5 1.6	ns	1,2,3,10
CWL = 9,11	CL = 10	CL = 12	tCK(AVG)	Reserved	ns	4
	CL = 11	CL = 13	tCK(AVG)	1.25 <1.5	ns	1,2,3,4,9
	CL = 12	CL = 14	tCK(AVG)	1.25 <1.5	ns	1,2,3,9
CWL = 10,12	CL = 12	CL = 14	tCK(AVG)	Reserved	ns	4
	CL = 13	CL = 15	tCK(AVG)	1.071 <1.25	ns	1,2,3,4,9
	CL = 14	CL = 16	tCK(AVG)	1.071 <1.25	ns	1,2,3,9
CWL = 11,14	CL = 14	CL = 17	tCK(AVG)	Reserved	ns	4
	CL = 15	CL = 18	tCK(AVG)	0.937 <1.071	ns	1,2,3,4,9
	CL = 16	CL = 19	tCK(AVG)	0.937 <1.071	ns	1,2,3,9
CWL = 12,16	CL = 15	CL = 18	tCK(AVG)	Reserved	ns	4
	CL = 16	CL = 19	tCK(AVG)	Reserved	ns	1,2,3,4,9
	CL = 17	CL = 20	tCK(AVG)	0.883 <938	ns	1,2,3,4,9
	CL = 18	CL = 21	tCK(AVG)	0.883 <938	ns	1,2,3
CWL = 14,18	CL = 17	CL = 20	tCK(AVG)	Reserved	ns	1,2,3,4
	CL = 18	CL = 21	tCK(AVG)	Reserved	ns	1,2,3,4
	CL = 19	CL = 22	tCK(AVG)	0.75 <0.833	ns	1,2,3
	CL = 20	CL = 23	tCK(AVG)	0.75 <0.833	ns	1,2,3
Supported CL Settings			10,11,12,13,14,15, 16, 17,18,19,20		nCK	
Supported CL Settings with read DBI			12,13,14,15, 16,17 18,19,20,21,22,23		nCK	

Supported CWL Settings	9,10,11,12,14,16,18	nCK	
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Speed Bin Table Notes

Absolute Specification

- VDDQ = VDD = 1.20V +/- 0.06 V
- VPP = 2.5V +0.25/-0.125 V
- The values defined with above-mentioned table are DLL ON case.
- DDR4-1600, 1866, 2133 and 2400 Speed Bin Tables are valid only when Geardown Mode is disabled.
 1. The CL setting and CWL setting result in tCK(avg).MIN and tCK(avg).MAX requirements. When making a selection of tCK(avg), both need to be fulfilled: Requirements from CL setting as well as requirements from CWL setting.
 2. tCK(avg).MIN limits: Since CAS Latency is not purely analog - data and strobe output are synchronized by the DLL - all possible intermediate frequencies may not be guaranteed. An application should use the next smaller JEDEC standard tCK(avg) value (1.5, 1.25, 1.071, 0.938 or 0.833 ns) when calculating CL [nCK] = tAA [ns] / tCK(avg) [ns], rounding up to the next 'Supported CL', where tAA = 12.5ns and tCK(avg) = 1.3 ns should only be used for CL = 10 calculation.
 3. tCK(avg).MAX limits: Calculate tCK(avg) = tAA.MAX / CL SELECTED and round the resulting tCK(avg) down to the next valid speed bin (i.e. 1.5ns or 1.25ns or 1.071 ns or 0.938 ns or 0.833 ns). This result is tCK(avg).MAX corresponding to CL SELECTED.
 4. 'Reserved' settings are not allowed. User must program a different value.
 5. 'Optional' settings allow certain devices in the industry to support this setting; however, it is not a mandatory feature. Refer to supplier's data sheet and/or the DIMM SPD information if and how this setting is supported.
 6. Any DDR4-1866 speed bin also supports functional operation at lower frequencies as shown in the table which are not subject to Production Tests but verified by Design/Characterization.
 7. Any DDR4-2133 speed bin also supports functional operation at lower frequencies as shown in the table which are not subject to Production Tests but verified by Design/Characterization.
 8. Any DDR4-2400 speed bin also supports functional operation at lower frequencies as shown in the table which are not subject to Production Tests but verified by Design/Characterization.
 9. Any DDR4-2666 speed bin also supports functional operation at lower frequencies as shown in the table which are not subject to Production Tests but verified by Design/Characterization.
 10. DDR4-1600 AC timing apply if DRAM operates at lower than 1600 MT/s data rate.
 11. Parameters apply from tCK(avg)min to tCK(avg)max at all standard JEDEC clock period values as stated in the Speed Bin Tables.
 12. CL number in parentheses, it means that these numbers are optional.
 13. DDR4 SDRAM supports CL=9 as long as a system meets tAA(min).
 14. Each speed bin lists the timing requirements that need to be supported in order for a given DRAM to be JEDEC compliant. JEDEC compliance does not require support for all speed bins within a given speed. JEDEC compliance requires meeting the parameters for a least one of the listed speed bins.

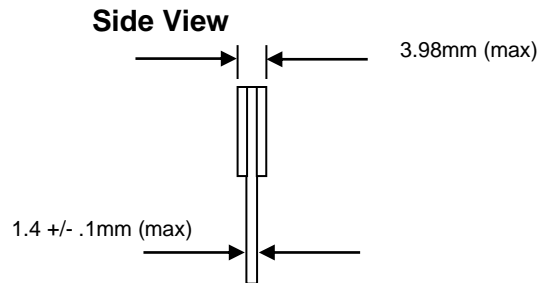
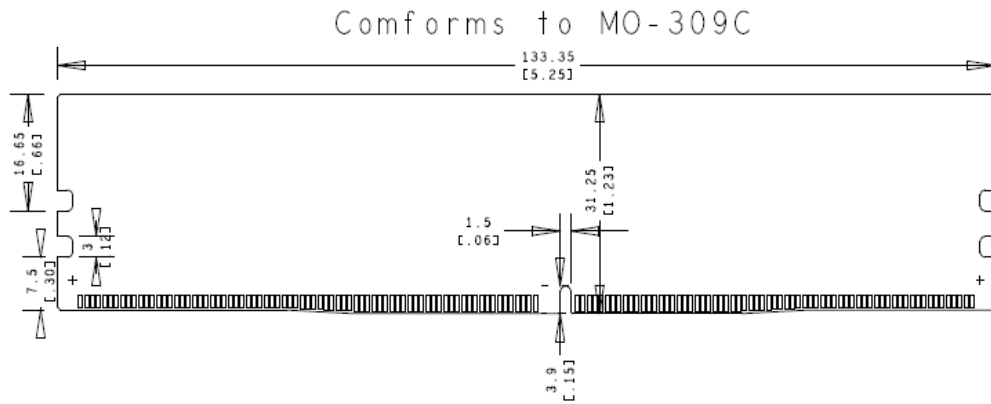
Pin Configuration

Front Side					Back Side										
1	12V,NC	37	V _{SS}	73	V _{DD}	109	V _{SS}	145	12V,NC	181	DQ29	217	V _{DD}	253	DQ41
2	V _{SS}	38	DQ24	74	CK0_t	110	DM5_n	146	V _{REFCA}	182	V _{SS}	218	CK1_t	254	V _{SS}
3	DQ4	39	V _{SS}	75	CK0_c	111	NC	147	V _{SS}	183	DQ25	219	CK1_c	255	DQS5_c
4	V _{SS}	40	DM3_n	76	V _{DD}	112	V _{SS}	148	DQ5	184	V _{SS}	220	V _{DD}	256	DQS5_t
5	DQ0	41	NC	77	V _{TT}	113	DQ46	149	V _{SS}	185	DQS3_c	221	V _{TT}	257	V _{SS}
6	V _{SS}	42	V _{SS}	78	EVENT_n	114	V _{SS}	150	DQ1	186	DQS3_t	222	PARITY	258	DQ47
7	DM0_n	43	DQ30	79	A0	115	DQ42	151	V _{SS}	187	V _{SS}	223	V _{DD}	259	V _{SS}
8	NC	44	V _{SS}	80	V _{DD}	116	V _{SS}	152	DQS0_t	188	DQ31	224	BA1	260	DQ43
9	V _{SS}	45	DQ26	81	BA0	117	DQ52	153	DQS0_c	189	V _{SS}	225	A10 / AP	261	V _{SS}
10	DQ6	46	V _{SS}	82	RAS_n / A16	118	V _{SS}	154	V _{SS}	190	DQ27	226	V _{DD}	262	DQ53
11	V _{SS}	47	CB4	83	V _{DD}	119	DQ48	155	DQ7	191	V _{SS}	227	RFU	263	V _{SS}
12	DQ2	48	V _{SS}	84	CS0_n	120	V _{SS}	156	V _{SS}	192	CB5	228	WE_n / A14	264	DQ49
13	V _{SS}	49	CB0	85	V _{DD}	121	DM6_n	157	DQ3	193	V _{SS}	229	V _{DD}	265	V _{SS}
14	DQ12	50	V _{SS}	86	CAS_n / A15	122	NC	158	V _{SS}	194	CB1	230	SAVE_n,NC	266	DQS6_c
15	V _{SS}	51	DM8_n	87	ODT0	123	V _{SS}	159	DQ13	195	V _{SS}	231	V _{DD}	267	DQS6_t
16	DQ8	52	NC	88	V _{DD}	124	DQ54	160	V _{SS}	196	DQS8_c	232	A13	268	V _{SS}
17	V _{SS}	53	V _{SS}	89	CS1_n	125	V _{SS}	161	DQ9	197	DQS8_t	233	V _{DD}	269	DQ55
18	DM1_n	54	CB6	90	V _{DD}	126	DQ50	162	V _{SS}	198	V _{SS}	234	A17, NC	270	V _{SS}
19	NC	55	V _{SS}	91	ODT1	127	V _{SS}	163	DQS1_c	199	CB7	235	C2,NC	271	DQ51
20	V _{SS}	56	CB2	92	V _{DD}	128	DQ60	164	DQS1_t	200	V _{SS}	236	V _{DD}	272	V _{SS}
21	DQ14	57	V _{SS}	93	CS2_n,C0,NC	129	V _{SS}	165	V _{SS}	201	CB3	237	CS3_n,C1,NC	273	DQ61
22	V _{SS}	58	RESET_n	94	V _{SS}	130	DQ56	166	DQ15	202	V _{SS}	238	SA2	274	V _{SS}
23	DQ10	59	V _{DD}	95	DQ36	131	V _{SS}	167	V _{SS}	203	CKE1	239	V _{SS}	275	DQ57
24	V _{SS}	60	CKE0	96	V _{SS}	132	DM7_n	168	DQ11	204	V _{DD}	240	DQ37	276	V _{SS}
25	DQ20	61	V _{DD}	97	DQ32	133	NC	169	V _{SS}	205	RFU	241	V _{SS}	277	DQS7_c
26	V _{SS}	62	ACT_n	98	V _{SS}	134	V _{SS}	170	DQ21	206	V _{DD}	242	DQ33	278	DQS7_t
27	DQ16	63	BG0	99	DM4_n	135	DQ62	171	V _{SS}	207	BG1	243	V _{SS}	279	V _{SS}
28	V _{SS}	64	V _{DD}	100	NC	136	V _{SS}	172	DQ17	208	ALERT_n	244	DQS4_c	280	DQ63
29	DM2_n	65	A12 / BC_n	101	V _{SS}	137	DQ58	173	V _{SS}	209	V _{DD}	245	DQS4_t	281	V _{SS}
30	NC	66	A9	102	DQ38	138	V _{SS}	174	DQS2_c	210	A11	246	V _{SS}	282	DQ59
31	V _{SS}	67	V _{DD}	103	V _{SS}	139	SA0	175	DQS2_t	211	A7	247	DQ39	283	V _{SS}
32	DQ22	68	A8	104	DQ34	140	SA1	176	V _{SS}	212	V _{DD}	248	V _{SS}	284	V _{DDSPD}
33	V _{SS}	69	A6	105	V _{SS}	141	SCL	177	DQ23	213	A5	249	DQ35	285	SDA
34	DQ18	70	V _{DD}	106	DQ44	142	V _{PP}	178	V _{SS}	214	A4	250	V _{SS}	286	V _{PP}
35	V _{SS}	71	A3	107	V _{SS}	143	V _{PP}	179	DQ19	215	V _{DD}	251	DQ45	287	V _{PP}
36	DQ28	72	A1	108	DQ40	144	RFU	180	V _{SS}	216	A2	252	V _{SS}	288	V _{PP}

PIN DESCRIPTION

Name	Function
CB[7:0]	Data Check Bits
DQ[63:0]	Data Bits
DQS[8:0]_t, DQS[8:0]_c	Differential Data Strobes
DM[8:0]_n	Data Masks
CK_t[1:0], CK_c[1:0]	Differential Clock Inputs
CKE[1:0]	Clock Enables
CAS_n / A15	Multiplexed: Column Address Strobe or Address 15
RAS_n / A16	Multiplexed: Row Address Strobe or Address 16
CS[1:0]_n, CS[3:2]*	Chip Selects
ACT_n	Activate Command Input
WE_n / A14	Multiplexed: Write Enable or Address 14
C[2:0]	Chip ID Inputs
A[17:0]	Address Inputs
BA[1:0]	Bank Address select Inputs
BG[1:0]	Bank Group select Inputs
ODT[1:0]	On Die Termination Inputs
SA[2:0]	SPD Address
SCL	SPD Clock Input
SDA	SPD Data Input/Output
EVENT_n	Temperature Sensing
RESET_n	Reset for register and DRAMs
PARITY	Parity bit input for Addr/Ctrl
ALERT_n	CRC Error Flag or CMD/Addr Parity Flag Output
A12 / BC_n	Combination Input: Address12/Burst Chop
A10 / AP	Combination Input: Addr10/Auto-precharge
12V*	Optional Power Supply*
V _{PP}	Charge Pump Power
V _{SS}	Ground
V _{DD}	Power
V _{DDSPD}	SPD EEPROM Power
V _{REFCA}	Reference Voltage for CA
V _{TT}	Termination Voltage
NC	No Connection
RFU	Reserved for Future Use

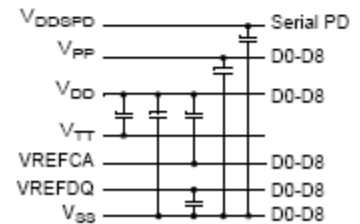
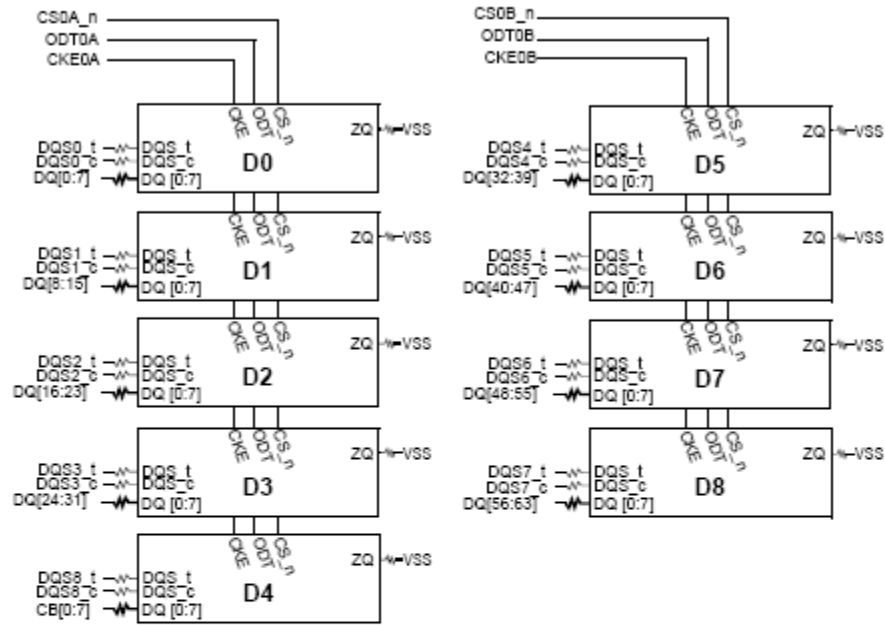
* Not used



Notes:

1. Tolerances on all dimensions except where otherwise indicated are ± 0.13 . Reference JEDEC standard MO-309C.
2. All dimensions are expressed: millimeters [inches]

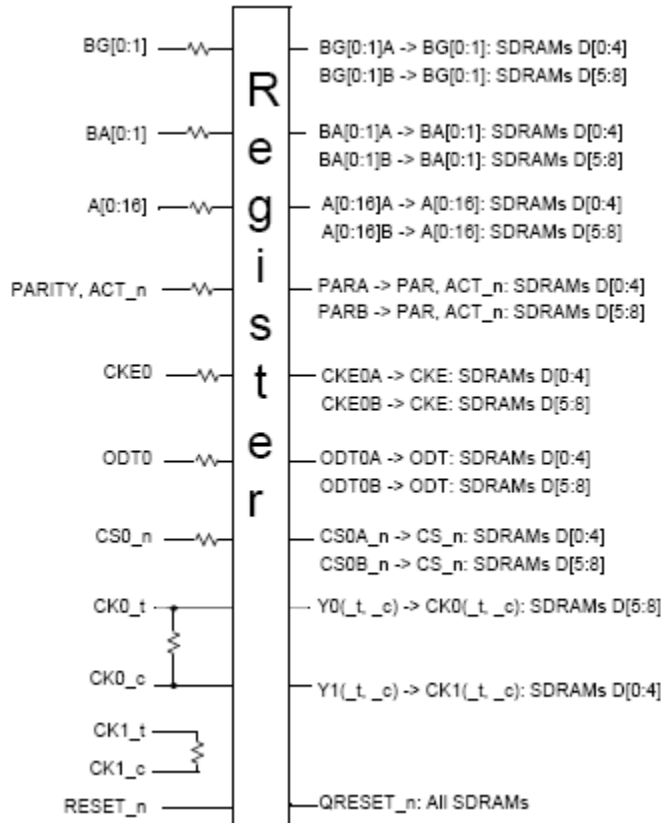
Functional Diagram



Note 1: Unless otherwise noted, resistor values are 15Ω ± 5%.

Note 2: See the Net Structure diagrams for all resistors associated with the command, address and control bus.

Note 3: ZQ resistors are 240Ω ± 1%. For all other resistor values refer to the appropriate wiring diagram.



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DTM68127-H

8GB - 288-Pin 1Rx8 Registered ECC DDR4 DIMM



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