4) Peripheral Chips for timing control - 8254/8253

Programmable timer device 8253

Intel’s programmable counter/timer device (8253) facilitates the generation of accurate time delays.

When 8253 is used as timing and delay generation peripheral, the microprocessor becomes free from the tasks related to the counting process and execute the programs in memory, while the timer device may perform the counting tasks.

This minimizes the software overhead on the microprocessor.

Architecture and Signal Descriptions

The programmable timer device 8253 contains three independent 16-bit counters, each with a maximum count rate of 2.6 MHz.

It is thus possible to generate three totally independent delays or maintain three independent counters simultaneously.

All the three counters may be independently controlled by programming the three internal command word registers.

The 8-bit, bidirectional data buffer interfaces internal circuit of 8253 to microprocessor systems bus.

Data is transmitted or received by the buffer upon the execution of IN or OUT instruction.

The read/write logic controls the direction of the data buffer depending upon whether it is a read or a write operation.

It may be noted that IN instruction reads data while OUT instruction writes data to a peripheral. The internal block diagram and pin diagram of 8253 are shown in Fig.

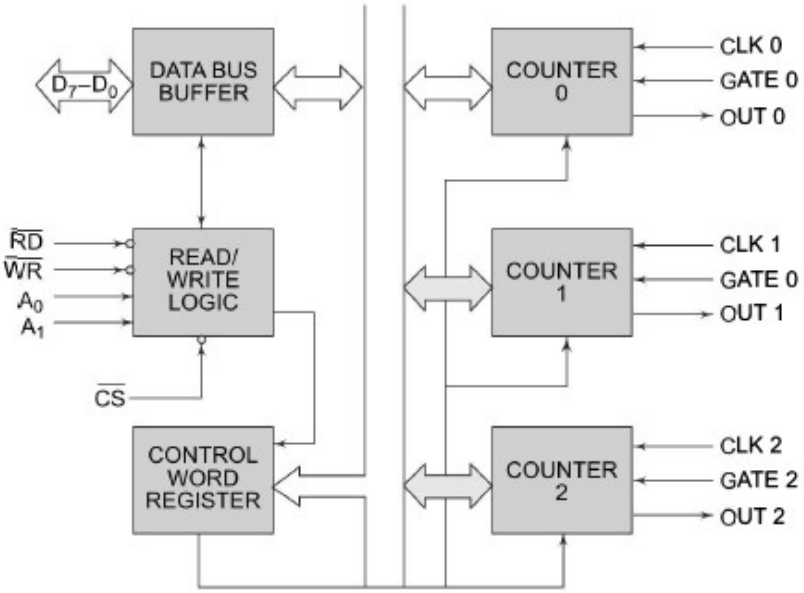
The three counters available in 8253 are independent of each other in operation, but they are identical to each other in organization.

These are all 16-bit presettable, down counters, able to operate either in BCD or in hexadecimal mode.

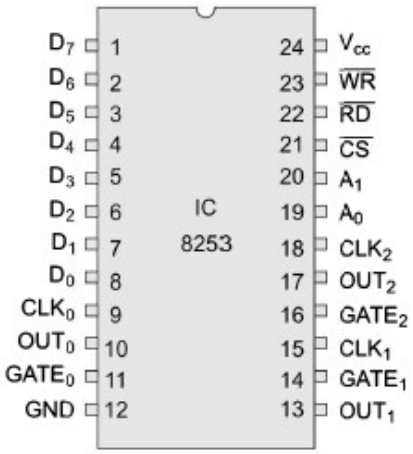
The mode control word register contains the information that can be used for writing or reading the count value into or from the respective count register using the OUT and IN instructions.

The specialty of the 8253 counters is that they can be easily read on line without disturbing the clock input to the counter.

This facility is called as "on the fly" reading of counters, and is invoked using a mode control word.
A0, Al pins are the address input pins and are required internally for addressing the mode control word registers and the three counter registers.



Internal Block Diagram of 8254



Pin Configuration of 8254

A low on CS line enables the 8253.

No operation will be performed by 8253 till it is enabled.

Table 1 shows the selected operations for various control inputs.

CS	RD	WR	A_1	A_0	Selected Operations
0	1	0	0	0	Write Counter 0
0	1	0	0	1	Write Counter 1
0	1	0	1	0	Write Counter 2
0	1	0	1	1	Write control Word
0	0	1	0	0	Read Counter 0
0	0	1	0	1	Read Counter 1
0	0	1	1	0	Read Counter 2
0	0	1	1	1	No Operation
0	1	1	X	X	No Operation
1	X	X	X	X	Disabled

A control word register accepts the 8-bit control word written by the microprocessor and stores it for controlling the complete operation of the specific counter.

It may be noted that, the control word register can only be written and cannot be read.

The CLK, GATE and OUT pins are available for each of the three timer channels.

Control Word Register

The 8253 can operate in anyone of the six different modes.

A control word must be written in the respective control word register by the microprocessor to initialize each of the counters of 8253 to decide its operating mode.

All the counters can operate in anyone of the modes or they may be even in different modes of operation, at a time.

The control word format is presented, along with the definition of each bit, in Fig.

While writing a count in the counter, it should be noted that, the count is written in the counter only after the data is put on the data bus, and a falling edge appears at the clock pin of the peripheral thereafter.

Any reading operation of the counter, before the falling edge appears may result in garbage data.

Programming and Interfacing 8253

There may be two types of write operations in 8253, viz. (i) writing a control word into a control word register and (ii) writing a count value into a count register.

The control word register accepts data from the data buffer and initializes the counters, as required.

The control word register contents are used for (a) initialising the operating modes (mode0-mode4) (b) selection of counters (counter0-counter2) (c) choosing binary BCD counters (d) loading of the counter registers.

The mode control register is a write only register and the CPU cannot read its contents.

One can directly write the mode control word for counter 2 or counter 1 prior to writing the control word for counter0.

Mode control word register has a separate address, so that it can be written independently.

A count register must be loaded with the count value, in the same byte sequence that was programmed in the mode control word of that counter, using the bits RL0 and RL1.

The loading of the count registers of different counters is again sequence independent.

One can directly write the 16-bit count register for count 2 before writing count 0 and count 1, but the two bytes in a count must be written in the byte

sequence programmed

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
SC1	SC0	RL1	RL0	M2	M1	M0	BCD

Control Word Format

SC_1	SC_0	OPERATION
0	0	Select Counter 0
0	1	Select Counter 1
1	0	Select Counter 2
1	1	Illegal

SC-Select Counter Bit Definitions

RL_1	RL_0	OPERATION
0	0	Latch Counter for 'ON THE FLY' reading
0	1	Read/Load Least Significant Byte only
1	0	Read/Load MSB only
1	1	Read/Load LSB first then MSB

RL-Read/Load Bit Definitions

M_2	M_1	M_0	Selected Mode
0	0	0	Mode 0
0	0	1	Mode 1
x	1	0	Mode 2
x	1	1	Mode 3
1	0	0	Mode 4
1	0	1	Mode 5

$M_2M_1M_0$ Mode Select Bit Definitions

BCD	Operation
0	Hexadecimal Count
1	BCD Count

HEX/BCD Bit Definition

Control Word Format and Bit Definitions

using RL0 and RL1 bits of the mode control word of the counter.

All the counters in 8253 are down counters, hence their count values go on decrementing if the CLK input pin is applied with a valid clock signal.

A maximum count is obtained by loading all zeros into a count register, i.e. 2^{16} for binary counting and 10^4 for BCD counting.

The 8253 responds to the negative clock edge of the clock input.

The maximum operating clock frequency of 8253 is 2.6 MHz.

For higher frequencies one can use timer 8254, which operates up to 10 MHz, maintaining pin compatibility with 8253.

<u>Selection of Count Registers and Control Word Register with A1 and A0</u>

In most of the practical applications, the counter is to be read and depending on the contents of the counter a decision is to be taken.

In case of 8253, the 16-bit contents of the counter can simply be read using successive 8-bit IN operations.

The mode control register cannot be read for any of the counters.

There are two methods for reading 8253 counter registers.

In the first method, either the clock or the counting procedure (using GATE) is inhibited to ensure a stable count.

Then the contents are read by selecting the suitable counter using A0, Al and executing using IN instructions.

The first IN instruction reads the least significant byte and the second IN instruction reads the most significant byte.

Internal logic of 8253 is designed in such a way that the programmer has to complete the reading operation as programmed by him, using RL0 and RLl bits of control word.

In the second method of reading a counter, the counter can be read while counting is in progress.

This method, as already mentioned is called as reading on fly.

In this method, neither clock nor the counting needs to be inhibited to read the counter.

The content of a counter can be read 'on fly' using a newly defined control word register format for online reading of the count register.

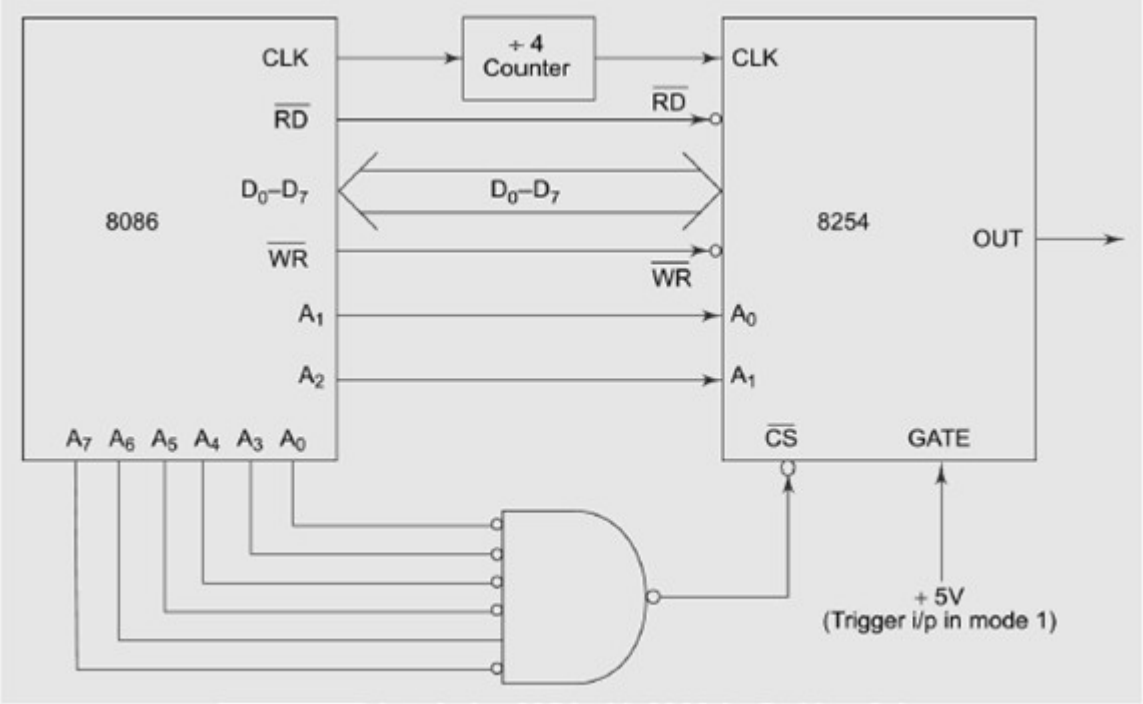
Writing a suitable control word, in the mode control register internally latches the contents of the counter.

After latching the content of a counter using this method, the programmer can read it using IN instructions.

D7-D6 = SC1,SC0 - Specify the counter to be selected
D5-D4 = 00 - Designate counter latching operation
X -Don't Care - All other bits are neglected

Mode Control Word for Latching Count

Selected Register	A_1	A_0
Mode Control Word Counter0	1	1
Mode Control Word Counter1	1	1
Mode Control Word Counter2	1	1
Counter Register Byte Counter 2 LSB	1	0
Counter Register Byte Counter 2 MSB	1	0
Counter Register Byte Counter 1 LSB	0	1
Counter Register Byte Counter 1 MSB	0	1
Counter Register Byte Counter 0 LSB	0	0



Interfacing 8254 with 8086

Interfacing 8254 with 8086

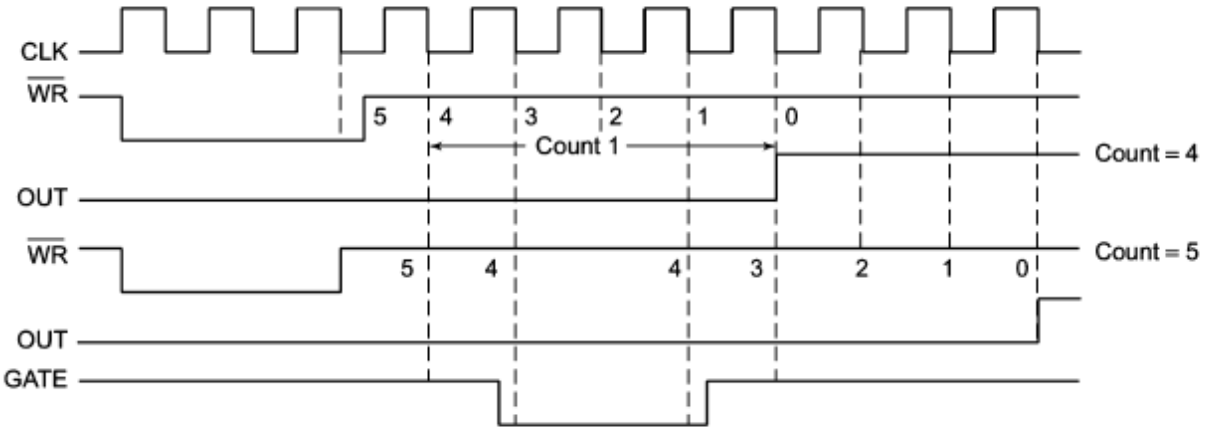
Neglecting the higher order address lines (A_{16}–A_8), the interfacing circuit diagram is shown in Fig. The 8254 is interfaced with lower order data bus (D_0–D_7), hence A_0 is used for selecting the even bank. The A_0 and A_1 of the 8254 are connected with A_1 and A_2 of the processor. The counter addresses can be decoded as given below. If A_0 is 1, the 8254 will not be selected at all.

A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	
0	1	0	0	0	0	0	0	= 40H Counter 0
					0	1	0	= 42H Counter 1
					1	0	0	= 44H Counter 2
					1	1	0	= 46H Control word Reg.

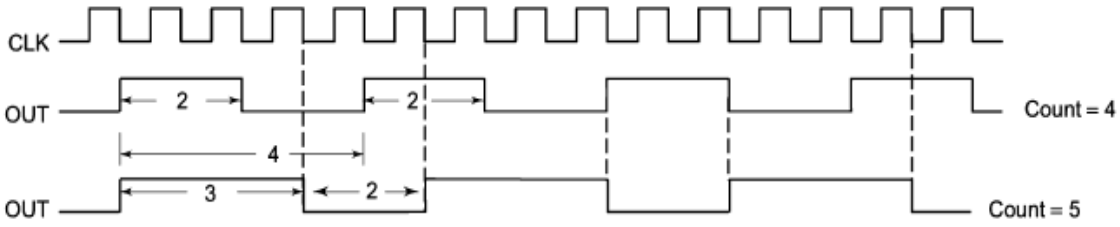
For generating a square wave, 8254 should be used in mode 3.

Let us select counter 0 for this purpose, that will be operated in BCD mode (may even be operated in HEX mode). Now suitable count is to be calculated for generating 1 ms time period.

Operating modes of 8254 are Mode0, Mode 1, Mode 2 , Mode 3 , Mode 4 and Mode 5.



Waveforms of $\overline{WR}$, OUT and GATE in Mode 0



Waveforms for Mode 3