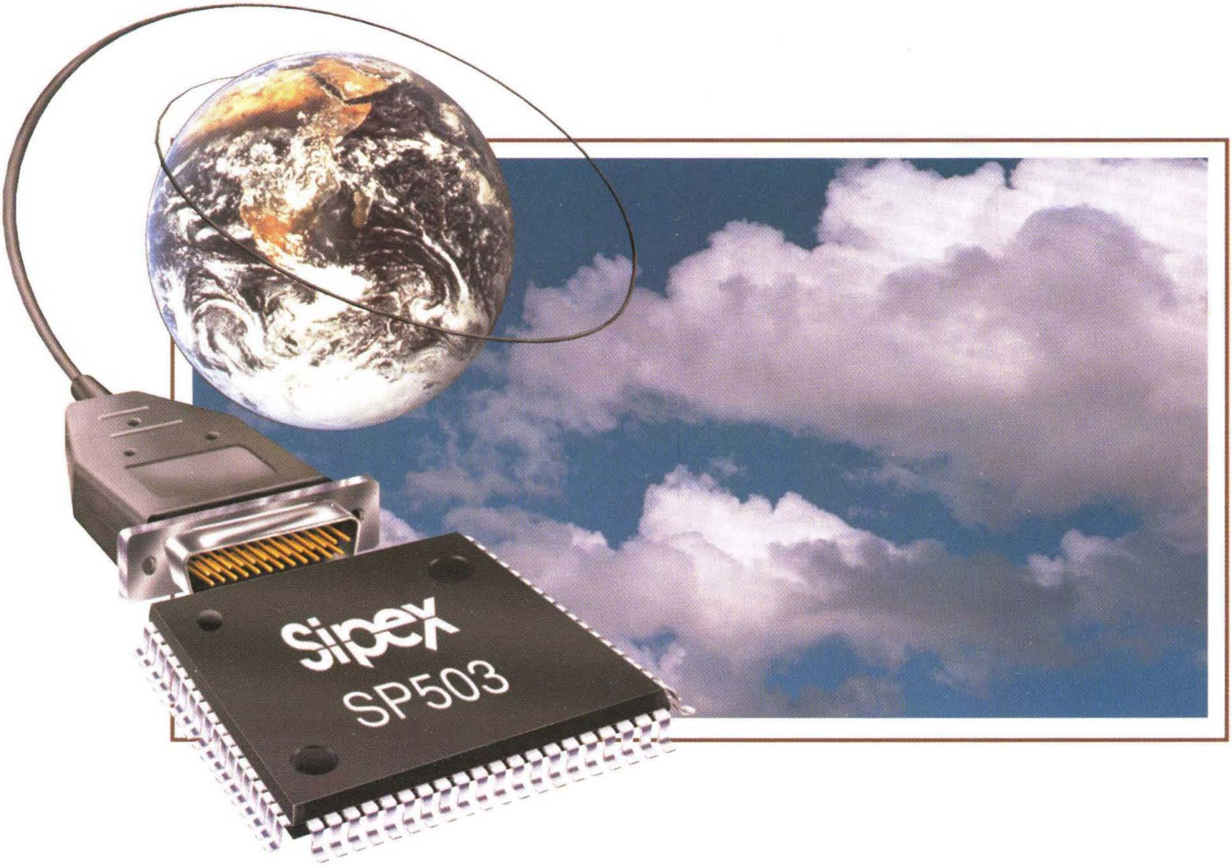
Catalog Supplement

Interface Products Supplement



Sipex

Sipex Corporation
SIGNAL PROCESSING EXCELLENCE

Model **Description** **Page**

TABLE OF CONTENTS

*IPC - Refer to Interface Products Catalog – Copyright 1994-1

CONTENTS

*IPC - Refer to Interface Products Catalog – Copyright 1994-1

INTERFACE PRODUCTS

INTERFACE PRODUCT SELECTION TABLE

+5V High–Speed RS-232 Transceivers with 0.1µF Capacitors

Model	No. Drivers	No. Receivers	Ext. Caps.	Shutdown (No.*)	Wakeup	TTL Tri–State	Page
SP200	5	0	4	Yes (0)	No	No	1
SP204	4	0	4	No	No	No	1
SP205	5	5	None	Yes(0)	No	Yes	1
SP205B	5	5	None	Yes (5)	Yes	Yes	1
SP206	4	3	4	Yes (0)	No	Yes	1
SP206B	4	3	4	Yes (3)	Yes	Yes	1
SP207	5	3	4	No	No	No	1
SP207B	5	3	4	Yes (3)	Yes	Yes	1
SP208	4	4	4	No	No	No	1
SP211	4	5	4	Yes (0)	No	Yes	1
SP211B	4	5	4	Yes (5)	Yes	Yes	1
SP213	4	5	4	Yes (2)	Yes	Yes	1

+5V 400 kbps RS-232 Transceivers with 0.1µF Capacitors

Model	No. Drivers	No. Receivers	Ext. Caps.	Shutdown (No.*)	Wakeup	TTL Tri–State	Page
SP207H	5	3	4	No	No	No	17
SP207HB	5	3	4	Yes (3)	Yes	Yes	17
SP211H	4	5	4	Yes (0)	No	Yes	17
SP211HB	4	5	4	Yes (5)	Yes	Yes	17

+5V/+12V Powered, Enhanced RS-232 Drivers/Receivers

Model	No. Drivers	No. Receivers	Ext. Caps.	Shutdown (No.*)	Wakeup	TTL Tri–State	Page
SP231A	2	2	2	No	No	No	IPC
SP239A	3	5	2	No	No	Yes	IPC

+5V Powered, Enhanced RS-232 Drivers/Receivers

Model	No. Drivers	No. Receivers	Ext. Caps.	Shutdown (No.*)	Wakeup	TTL Tri–State	Page
SP232A	2	2	4	No	No	No	IPC
SP233A	2	2	None	No	No	No	IPC
SP310A	2	2	4	Yes (0)	No	No	IPC

+5V Powered, Enhanced RS-232 Drivers/Receivers, with Receiver Enable, Shutdown and Wakeup

Model	No. Drivers	No. Receivers	Ext. Caps.	Shutdown (No.*)	Wakeup	TTL Tri–State	Page
SP241C	3	5	4	Yes (0)	Yes	Yes	IPC
SP312A	2	2	4	Yes (2)	Yes	Yes	IPC

+5V Powered RS-232 Drivers/Receivers

Model	No. Drivers	No. Receivers	Ext. Caps.	Shutdown (No.*)	Wakeup	TTL Tri–State	Page
SP230A	5	0	4	Yes (0)	No	No	IPC
SP234A	4	0	4	No	No	No	IPC
SP235A	5	5	None	Yes (0)	No	Yes	IPC
SP235B	5	5	None	Yes (5)	Yes	Yes	IPC
SP236A	4	3	4	Yes (0)	No	Yes	IPC
SP236B	4	3	4	Yes (3)	Yes	Yes	IPC
SP237A	5	3	4	No	No	No	IPC
SP238A	4	4	4	No	No	No	IPC
SP240A	5	5	4	Yes (0)	No	Yes	IPC
SP240B	5	5	4	Yes (5)	Yes	Yes	IPC
SP241A	4	5	4	Yes (0)	No	Yes	IPC
SP241B	4	5	4	Yes (5)	Yes	Yes	IPC

RS-232/RS-422 Line Drivers/Receivers

Model	No. RS-232 Ch.	No. RS-422 Ch.	Mode Select	Loopback Test	Page
SP301	2	2	Software	Yes	IPC
SP302	4	2	Software	Yes	IPC

Enhanced RS-232/RS-422 Line Drivers/Receivers

Model	No. RS-232 Ch.	No. RS-422 Ch.	Mode Select	Loopback Test	Page
SP304	4	2	Software	Yes	IPC

* Number of active receivers in Shutdown mode.

INTERFACE PRODUCT SELECTION TABLE

RS-232/AppleTalk™ Serial Transceiver

Model	No. RS-232 Drivers.	No. RS-232 Receivers	Macintosh™ Port	Mode Select	Page
SP303	4	4	1	Software	IPC

RS-422/RS423 Line Drivers/Receiver

Model	No. RS-232 Drivers.	No. RS423 Ch.	Mode Select	Loopback Test	Page
SP306	2	2	Software	Yes	IPC

V.35 Transceiver

Model	No. RS232 Drivers.	No. RS-232 Receivers	No. V.35 Drivers	No. V.35 Receivers	TL Tri–State	Page
SP320	4	4	2	2	Yes	27

+5V Powered RS-232/RS-485 Line Driver/Receiver

Model	No. RS-232 CH.	No. RS-485 Ch	Mode Select	Loopback Test	Page
SP332	4	2	Software	Yes	39

+5V Powered RS-232/AppleTalk™ Serial Transceivers

Model	No. RS-232 Drivers.	No. RS-232 Receivers	Mode Select	Macintosh™ Port	Page
SP333	4	4	Software	1	49

+3.3V Powered EIA562 Line Drivers/Receivers

Model	No. Drivers.	No. Receivers	Shutdown (No.*)	WakeUp	TTL Tri–State	Page
SP341	3	5	Yes (0)	Yes	Yes	IPC

RS485/RS422 Half–Duplex Interface Transceivers

Model	No. Drivers.	No. Receivers	Shutdown (No.*)	Low Power	Low EMI	Driver Enable	Rcvr Enable	Page
SP481	1	1	Yes	Yes	No	Yes	Yes	61
SP483	1	1	Yes	Yes	Yes	Yes	Yes	61
SP485	1	1	No	Yes	No	Yes	Yes	61

RS-485/RS-422 Line Drivers

Model	No. Drivers.	Driver Enable	Page
SP486	4	Common	IPC
SP487	4	Independent	IPC

RS-485/RS-422 Line Receivers

Model	No. Receivers.	Receiver Enable	Page
SP488	4	Common	IPC
SP489	4	Dual Pair	IPC

RS-485 Full–Duplex Interface Transceivers

Model	No. Drivers.	No. Receivers	Shutdown	Low Power	Driver Enable	Rcvr Enable	Page
SP490	1	1	No	Yes	No	No	69
SP491	1	1	No	Yes	Yes	Yes	69

RS-485/RS-422 Line Drivers/Receivers

Model	No. Drivers.	No. Receivers	Driver Enable	Rcvr Enable	Page
SP495	4	4	Independent	Independent	77

Multi–Protocol/Multi–Mode Serial Line Drivers/Receivers

Model	Protocols.	Drivers	Receivers	Internal V.35 Terminator	Tri-State Control	Page
SP501	11	6	7	No	Driver	IPC
SP502	6	6	7	No	Driver	IPC
SP503	6	7	7	No	Driver	83
SP504	8	7	7	Yes	Driver/Receiver	125

CMOS Asynchronous to Synchronous Converter

Model	Page
MAS7838	IPC

* Number of active receivers in Shutdown mode.

EIA STANDARDS

Specification		RS-232D	RS-423A	RS-422	RS-485	RS-562
Mode of Operation		Single-Ended	Single-Ended	Differential	Differential	Single–Ended
Number of Drivers and Receivers Allowed on One Line		1 Driver 1 Receiver	1 Driver 10 Receivers	1 Driver 10 Receivers	32 Drivers 32 Receivers	1 Driver 1 Receiver
Maximum Cable Length		50 feet	4,000 feet	4,000 feet	4,000 feet	C≤2500pF @ ≤20kb/s C≤1000pF @ ≥20kb/s
Maximum Data Rate		20kb/s	100kb/s	10Mb/s	10Mb/s	64kb/s
Driver Output Maximum Voltage		±25V	±6V	-0.25V to +6V	-7V to +12V	-3.7 to +13.2V
Driver Output Signal Level	Loaded	±5V	±3.6V	±2V	±1.5V	±3.7V
	Unloaded	±15V	±6V	±5V	±5V	±13.2V
Driver Load Impedance		3kΩ to 7kΩ	450Ω min.	100Ω	54Ω	3kΩ to 7kΩ
Maximum Driver Output Current (High Impedance State)	Power On	—— ——	—— ——	—— ——	±100µA	—— ——
	Power Off	V_{MAX} /300	100µA	±100µA	±100µA	—— ——
Slew Rate		30V/µs max.	Controls Provided	—— ——	—— ——	30V/µs max.
Receiver Input Voltage Range		±15V	±12V	-7V to +7V	-7V to +12V	±15V
Receiver Input Sensistivity		±3V	±200mV	±200mV	±200mV	±3V
Receiver Input Resistance		3kΩto 7kΩ	4kΩ min.	4kΩ min.	12kΩ min.	3kΩ to 7kΩ

Sipex
Corporation
SIGNAL PROCESSING EXCELLENCE

Commonly–Used Data Communications Interfaces††

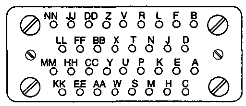
		RS-232		EIA-530		RS-449		EIA-561		EIA-574		V.35	
Signal Name	***Source***	***Mnemonic***	***Pin***	***Mnemonic***	***Pin***	***Mnemonic***	***Pin***	***Mnemonic***	***Pin***	***Mnemonic***	***Pin***	***Mnemonic***	***Pin***
Shield	—	—	1	—	1	—	1	—	—	—	—	—	A
Transmitted Data	DTE	BA	2	BA (A)	2	SD (A)	4	103	6	103	3	103	P
				BA (B)	14	SD (B)	22					103	S
Received Data	DCE	BB	3	BB (A)	3	RD (A)	6	104	5	104	2	104	R
				BB (B)	16	RD (B)	24					104	T
Request To Send	DTE	CA	4	CA (A)	4	RS (A)	7	105/133†	8	105/133†	7	105	C
				CA (B)	19	RS (B)	25						
Clear To Send	DCE	CB	5	CB (A)	5	CS (A)	9	106	7	106	8	106	D
				CB (B)	13	CS (B)	27						
DCE Ready (DSR)	DCE	CC	6	CC (A)	6	DM (A)	11	—	—	107	6	107	E
				CC (B)	22	DM (B)	29						
DTE Ready (DTR)	DTE	CD	20	CD (A)	20	TR (A)	12	108	3	108	4	108	H *
				CD (B)	23	TR (B)	30						
Signal Ground	—	AB	7	AB	7	SG	19	102	4	102	5	102	B
Recv. Line Sig. Det. (DCD)	DCE	CF	8	CF (A)	8	RR (A)	13	109	2	109	1	109	F
				CF (B)	10	RR (B)	31						
Trans. Sig. Elemt. Timing	DCE	DB	15	DB (A)	15	ST (A)	5	—	—	—	—	114	Y
				DB (B)	12	ST (B)	23					114	AA
Recv. Sig. Elemt. Timing	DCE	DD	17	DD (A)	17	RT (A)	8	—	—	—	—	115	V
				DD (B)	9	RT (B)	26					115	X
Local Loopback	DTE	LL	18	LL	18	LL	10	—	—	—	—	141	L *
Remote Loopback	DTE	RL	21	RL	21	RL	14	—	—	—	—	140	N *
Ring Indicator	DCE	CE	22	—	—	—	—	125	1	125	9	125	J *
Trans. Sig. Elemt. Timing	DTE	DA	24	DA (A)	24	TT (A)	17	—	—	—	—	113	U *
				DA (B)	11	TT (B)	35					113	W *
Test Mode	DCE	TM	25	TM	25	TM	18	—	—	—	—	142	NN *

METACOMP

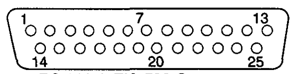
** Pins are specified in ISO 2593 but are not included in CCITT v.35*

† When hardware flow control is required, Circuit 105 may take on the functionality of Circuit 133.

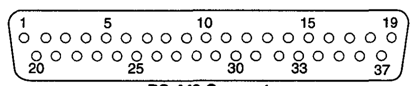
†† Some less–commonly used signals are not shown. METACOMP and SIPEX make no representation as to the accuracy or reliability of the information provided herein.



V.35/ISO-2593 Connector
DTE Connector Face — 34 Pin Male



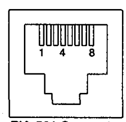
RS-232 & EIA-530 Connector
DTE Connector Face — DB-25 Pin Male



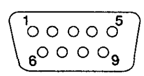
RS-449 Connector
DTE Connector Face — DB-37 Pin Male

Interchange Voltage States

Notation	***Negative***	***Positive***
BinaryState	1	0
Signal Condition	Marking	Spacing
Function	Off	On



EIA-561 Connector
Equip. Connector Face
RJ-45 8 Pin Female



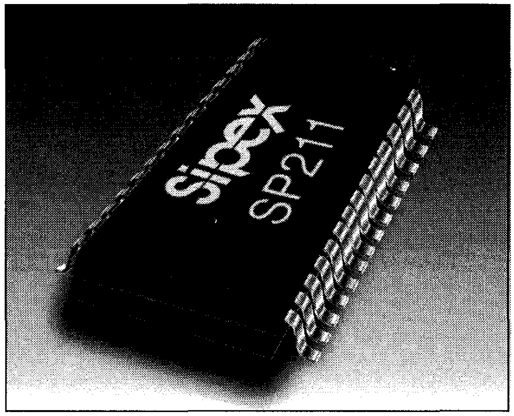
EIA-574 Connector
DTE Connector Face
DB-9 Pin Male

THIS PAGE LEFT INTENTIONALLY BLANK

SP200/204/205/206/207/208/211/213

+5V High–Speed RS-232 Transceivers with 0.1μF Capacitors

- 0.1μF External Charge Pump Capacitors
- 120Kbps Data Rate
- Standard SOIC and SSOP Packages
- Multiple Drivers and Receivers
- Single 5V Supply Operation
- 1μA Shutdown Mode
- WakeUp Feature in Shutdown Mode
- Tri–State Receiver Outputs
- Meets All RS-232 and V.28 Specifications
- Improved Driver Output Capacity for Mouse Applications
- ±10KV ESD Protection*



DESCRIPTION...

The **SP200 Series** are multi–channel RS-232 line transceivers in a variety of configurations to fit most communication needs. All models in this Series feature low–power CMOS construction and **Sipex**–patented (5,306,954) on-board charge pump circuitry to generate the ±10V RS-232 voltage levels, using 0.1μF charge pump capacitors to save board space and reduce circuit cost. The **SP200, SP205, SP206, SP207B, SP211** and **SP213** models feature a low–power shutdown mode, which reduces power supply drain to 1μA. A WakeUp function keeps the receivers active in the shutdown mode.

Model	Number of RS-232 Drivers	Number of RS-232 Receivers	No. of Receivers Active in Shutdown	No. of External 0.1μF Capacitors	Shutdown	WakeUp	TTL Tri–State
SP200	5	0	0	4	Yes	No	No
SP204	4	0	0	4	No	No	No
SP205	5	5	0	None	Yes	No	Yes
SP205B	5	5	5	None	Yes	Yes	Yes
SP206	4	3	0	4	Yes	No	Yes
SP206B	4	3	3	4	Yes	Yes	Yes
SP207	5	3	0	4	No	No	No
SP207B	5	3	3	4	Yes	Yes	Yes
SP208	4	4	0	4	No	No	No
SP211	4	5	0	4	Yes	No	Yes
SP211B	4	5	5	4	Yes	Yes	Yes
SP213	4	5	2	4	Yes	Yes	Yes

Table 1. Model Selection Table
**All driver outputs and receiver inputs characterized per MIL-STD-883C Method 3015.7*

ABSOLUTE MAXIMUM RATINGS

These are stress ratings only and functional operation of the device at these or any other above those indicated in the operation sections of the specifications below is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

V_{CC} .... +6V
V^+ .... (V_{CC} – 0.3V) to +13.2V
V^- 13.2V
Input Voltages
T_{IN} .... –0.3V to (V_{CC} +0.3V)
R_{IN} .... ±20V
Output Voltages
T_{OUT} .... (V^+, +0.3V) to (V^-, –0.3V)
R_{OUT} .... –0.3V to (V_{CC} +0.3V)
Short Circuit Duration on T_{OUT} .... Continuous
Power Dissipation
Plastic DIP 375mW
(derate 7mW/°C above +70°C)
Small Outline 375mW
(derate 7mW/°C above +70°C)

SPECIFICATIONS

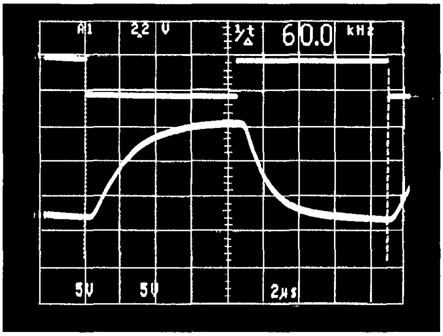
V_{CC} at nominal ratings; 0.1µF charge pump capacitors; T_{MIN} to T_{MAX}, unless otherwise noted.

PARAMETER	MIN.	TYP.	MAX.	UNIT	CONDITIONS
TTL INPUTS					T_{IN}, EN, SD
Logic Threshold					
V_{IL}			0.8	Volts	
V_{IH}	2.0			Volts	
Logic Pullup Current		15	200	µA	T_{IN} = 0V
Data Rate			120	Kbps	C_L = 2,500pF, R_L = 3KΩ
TTL OUTPUTS					
Compatibility		TTL/CMOS			
V_{OL}			0.4	Volts	I_{OUT} = 3.2mA; V_{CC} = +5V
V_{OH}	3.5			Volts	I_{OUT} = –1.0mA
Leakage Current		0.05	±10	µA	EN = V_{CC}; 0V ≤ R_{OUT} ≤ V_{CC}; T_A = +25°C
RS-232 OUTPUT					
Output Voltage Swing	±5	±7		Volts	All transmitter outputs loaded with 3KΩ to ground
Output Resistance	300			Ohms	V_{CC} = 0V; V_{OUT} = ±2V
Output Short Circuit Current		±25		mA	Infinite duration
RS-232 INPUT					
Voltage Range	–15		+15	Volts	
Voltage Threshold					
Low	0.8	1.2		Volts	V_{CC} = 5V, T_A = +25°C
High		1.7	2.4	Volts	V_{CC} = 5V, T_A = +25°C
Hysteresis	0.2	0.5	1.0	Volts	V_{CC} = +5V
Resistance	3	5	7	KΩ	±15V; T_A = +25°C
DYNAMIC CHARACTERISTICS					
Propagation Delay		1.5		µs	RS-232–to–TTL
Instantaneous Slew Rate			30	V/µs	C_L = 50pF, R_L = 3–7KΩ; T_A = +25°C
Transition Region Slew Rate		5		V/µs	C_L = 2,500pF, R_L = 3KΩ; measured from +3V to –3V or –3V to +3V
Output Enable Time		400		ns	
Output Disable Time		250		ns	

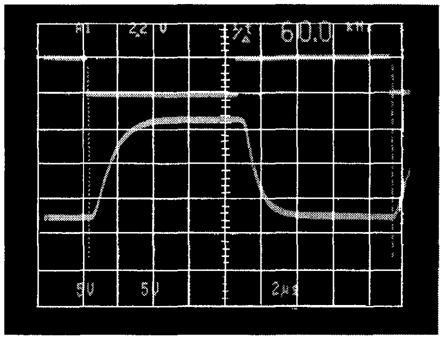
SPECIFICATIONS

V_{CC} at nominal ratings; 0.1µF charge pump capacitors; T_{MIN} to T_{MAX}, unless otherwise noted.

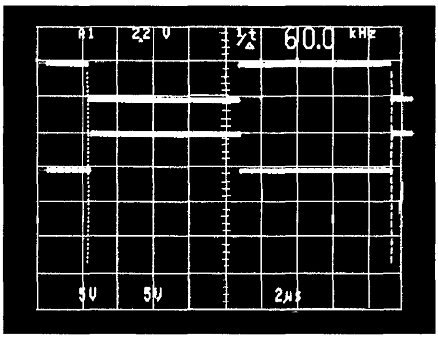
PARAMETER	MIN.	TYP.	MAX.	UNIT	CONDITIONS
POWER REQUIREMENTS					
V_{CC}					
SP200, SP205, SP207 and SP207B	4.75	5.00	5.25	Volts	
All other parts	4.50	5.00	5.50	Volts	
I_{CC}					T_A = +25°C
		4	10	mA	No load; V_{CC} = ±10%
		20		mA	All transmitters R_L = 3KΩ
Shutdown Current		1	10	µA	T_A = +25°C
ENVIRONMENTAL AND MECHANICAL					
Operating Temperature					
Commercial, –C	0		+70	°C	
Extended, –E	–40		+85	°C	
Storage Temperature	–65		+125	°C	
Package					
–A	Shrink (SSOP) small outline				
–T	Wide (SOIC) small outline				



Transmitter Output
R_L=3KΩ, C_L=5,000pF

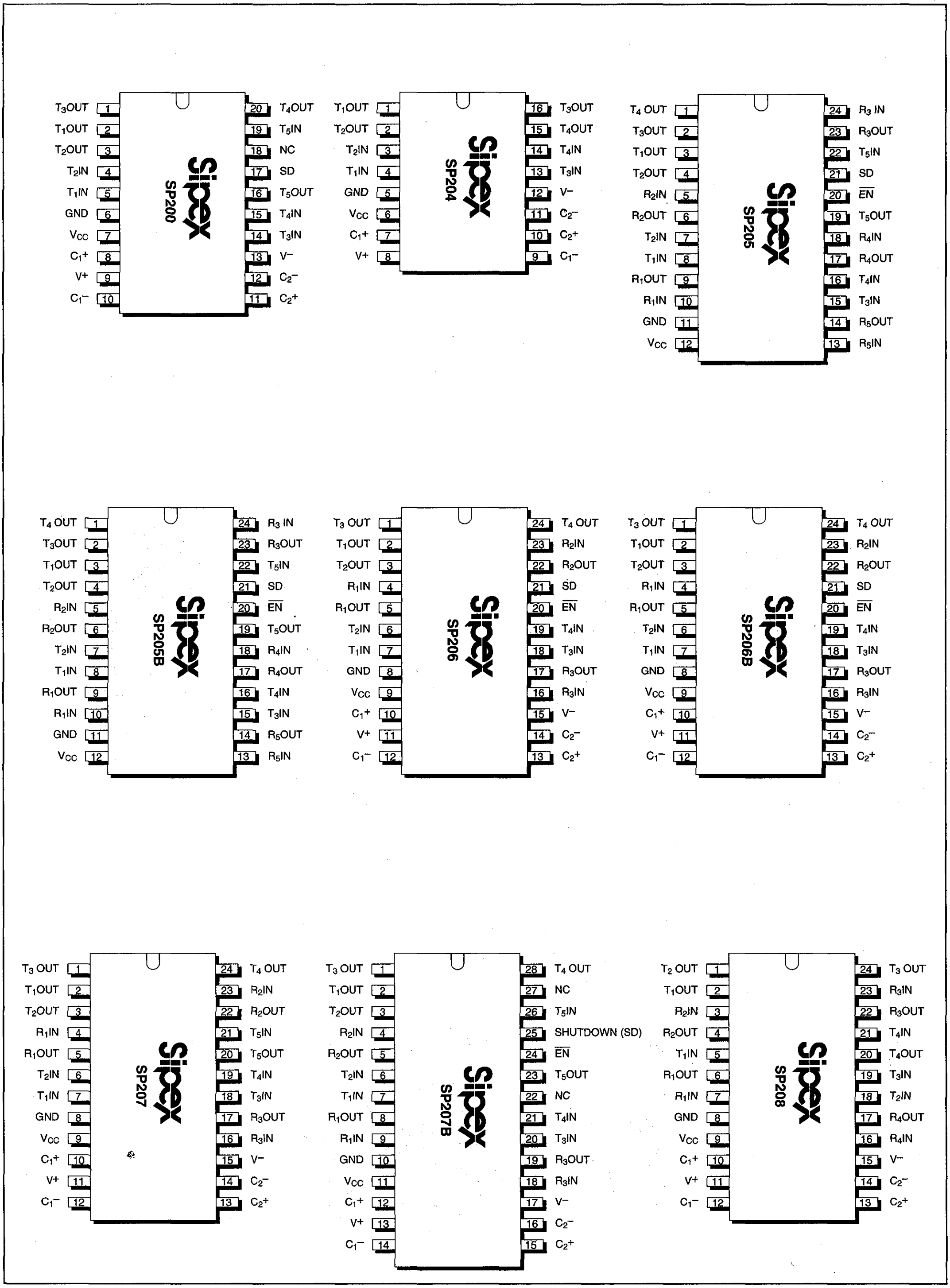


Transmitter Output
R_L=3KΩ, CL=2,500pF

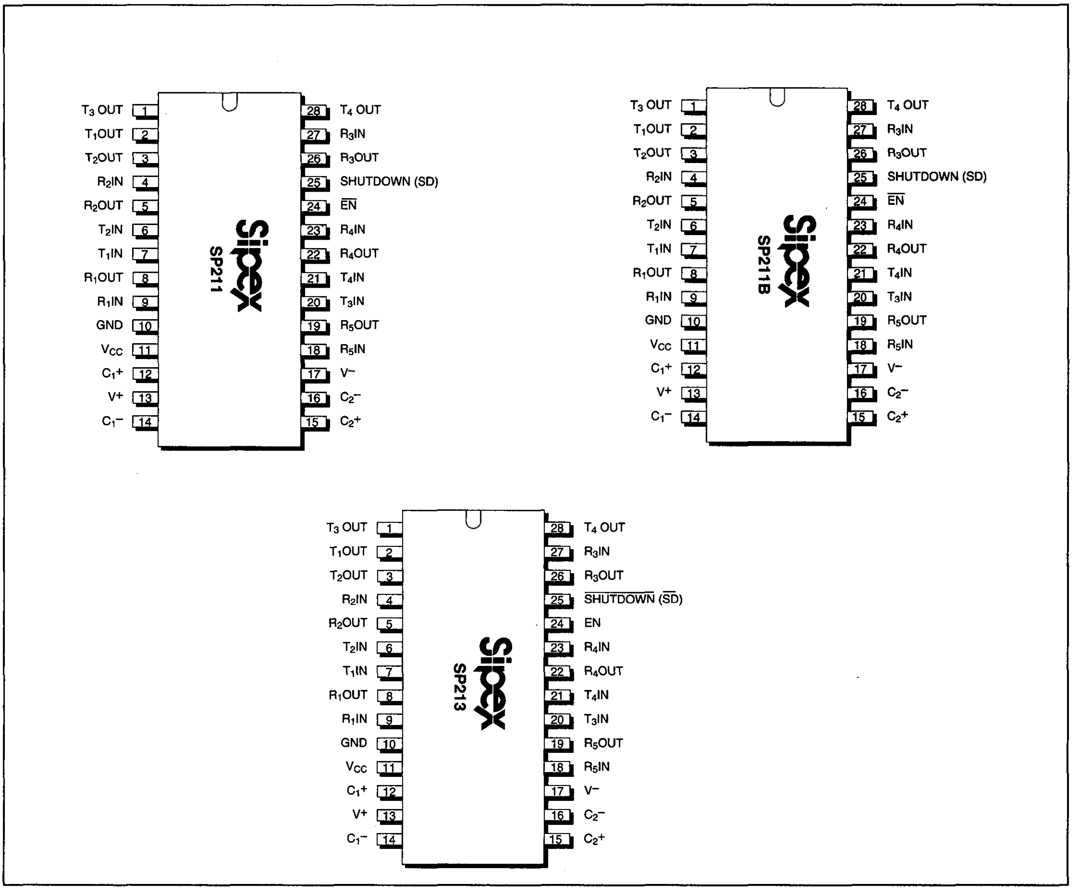


Receiver Output

PINOUT


Sipex SP200
T_3OUT 1
T_1OUT 2
T_2OUT 3
T_2IN 4
T_1IN 5
GND 6
V_{CC} 7
C_1+ 8
V+ 9
C_1− 10
20 T_4OUT
19 T_5IN
18 NC
17 SD
16 T_5OUT
15 T_4IN
14 T_3IN
13 V−
12 C_2−
11 C_2+
Sipex SP204
T_1OUT 1
T_2OUT 2
T_2IN 3
T_1IN 4
GND 5
V_{CC} 6
C_1+ 7
V+ 8
16 T_3OUT
15 T_4OUT
14 T_4IN
13 T_3IN
12 V−
11 C_2−
10 C_2+
9 C_1−
Sipex SP205
T_4 OUT 1
T_3OUT 2
T_1OUT 3
T_2OUT 4
R_2IN 5
R_2OUT 6
T_2IN 7
T_1IN 8
R_1OUT 9
R_1IN 10
GND 11
V_{CC} 12
24 R_3 IN
23 R_3OUT
22 T_5IN
21 SD
20 $\overline{EN}$
19 T_5OUT
18 R_4IN
17 R_4OUT
16 T_4IN
15 T_3IN
14 R_5OUT
13 R_5IN
Sipex SP205B
T_4 OUT 1
T_3OUT 2
T_1OUT 3
T_2OUT 4
R_2IN 5
R_2OUT 6
T_2IN 7
T_1IN 8
R_1OUT 9
R_1IN 10
GND 11
V_{CC} 12
24 R_3 IN
23 R_3OUT
22 T_5IN
21 SD
20 $\overline{EN}$
19 T_5OUT
18 R_4IN
17 R_4OUT
16 T_4IN
15 T_3IN
14 R_5OUT
13 R_5IN
Sipex SP206
T_3 OUT 1
T_1OUT 2
T_2OUT 3
R_1IN 4
R_1OUT 5
T_2IN 6
T_1IN 7
GND 8
V_{CC} 9
C_1+ 10
V+ 11
C_1− 12
24 T_4 OUT
23 R_2IN
22 R_2OUT
21 SD
20 $\overline{EN}$
19 T_4IN
18 T_3IN
17 R_3OUT
16 R_3IN
15 V−
14 C_2−
13 C_2+
Sipex SP206B
T_3 OUT 1
T_1OUT 2
T_2OUT 3
R_1IN 4
R_1OUT 5
T_2IN 6
T_1IN 7
GND 8
V_{CC} 9
C_1+ 10
V+ 11
C_1− 12
24 T_4 OUT
23 R_2IN
22 R_2OUT
21 SD
20 $\overline{EN}$
19 T_4IN
18 T_3IN
17 R_3OUT
16 R_3IN
15 V−
14 C_2−
13 C_2+
Sipex SP207
T_3 OUT 1
T_1OUT 2
T_2OUT 3
R_1IN 4
R_1OUT 5
T_2IN 6
T_1IN 7
GND 8
V_{CC} 9
C_1+ 10
V+ 11
C_1− 12
24 T_4 OUT
23 R_2IN
22 R_2OUT
21 T_5IN
20 T_5OUT
19 T_4IN
18 T_3IN
17 R_3OUT
16 R_3IN
15 V−
14 C_2−
13 C_2+
Sipex SP207B
T_3 OUT 1
T_1OUT 2
T_2OUT 3
R_2IN 4
R_2OUT 5
T_2IN 6
T_1IN 7
R_1OUT 8
R_1IN 9
GND 10
V_{CC} 11
C_1+ 12
V+ 13
C_1− 14
28 T_4 OUT
27 NC
26 T_5IN
25 SHUTDOWN (SD)
24 $\overline{EN}$
23 T_5OUT
22 NC
21 T_4IN
20 T_3IN
19 R_3OUT
18 R_3IN
17 V−
16 C_2−
15 C_2+
Sipex SP208
T_2 OUT 1
T_1OUT 2
R_2IN 3
R_2OUT 4
T_1IN 5
R_1OUT 6
R_1IN 7
GND 8
V_{CC} 9
C_1+ 10
V+ 11
C_1− 12
24 T_3 OUT
23 R_3IN
22 R_3OUT
21 T_4IN
20 T_4OUT
19 T_3IN
18 T_2IN
17 R_4OUT
16 R_4IN
15 V−
14 C_2−
13 C_2+

PINOUT



FEATURES...

The **SP200 Series** multi–channel RS-232 line transceivers provide a variety of configurations to fit most communication needs, especially those applications where ±12V is not available. All models in this Series feature low–power CMOS construction and **Sipex**–proprietary on-board charge pump circuitry to generate the ±10V RS-232 voltage levels. The ability to use 0.1µF charge pump capacitors saves board space and reduces circuit cost. Different models within the Series provide different driver/receiver combinations to match any application requirement.

The **SP200**, **SP205**, **SP206**, **SP207B**, **SP211** and **SP213** models feature a low–power shutdown mode, which reduces power supply drain to 1µA. The WakeUp function keeps the receivers active in the shutdown mode, unless disabled by the EN pin. Models with –B suffix are equipped with the WakeUp function.

Models in the Series are available in 28–pin SO (wide) and SSOP (shrink) small outline packages. Devices can be specified for commercial (0°C to +70°C) and industrial/extended (–40°C to +85°C) operating temperatures.

THEORY OF OPERATION

Charge–Pump

The charge pump is a **Sipex**–patented design (5,306,954) and uses a unique approach compared to older less–efficient designs. The charge pump still requires four external capacitors, but uses a four–phase voltage shifting technique to

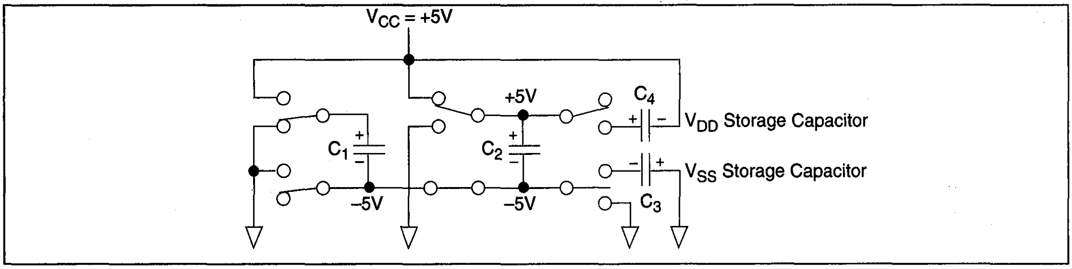


Figure 1. Charge Pump — Phase 1

attain symmetrical 10V power supplies. *Figure 3a* shows the waveform found on the positive side of capcitor C_2, and *Figure 3b* shows the negative side of capcitor C_2. There is a free–running oscillator that controls the four phases of the voltage shifting. A description of each phase follows.

Phase 1

— V_{SS} charge storage —During this phase of the clock cycle, the positive side of capacitors C_1 and C_2 are initially charged to +5V. C_1^+ is then switched to ground and the charge in C_1^- is transferred to C_2^-. Since C_2^+ is connected to +5V, the voltage potential across capacitor C_2 is now 10V.

Phase 2

— V_{SS} transfer — Phase two of the clock connects the negative terminal of C_2 to the V_{SS} storage capacitor and the positive terminal of C_2 to ground, and transfers the generated –10V to C_3. Simultaneously, the positive side of capacitor C_1 is switched to +5V and the negative side is connected to ground.

Phase 3

— V_{DD} charge storage — The third phase of the clock is identical to the first phase — the charge transferred in C_1 produces –5V in the negative terminal of C_1, which is applied to the negative side of capacitor C_2. Since C_2^+ is at +5V, the voltage potential across C_2 is 10V.

Phase 4

— V_{DD} transfer — The fourth phase of the clock connects the negative terminal of C_2 to ground, and transfers the generated 10V across C_2 to C_4, the V_{DD} storage capacitor. Again, simultaneously with this, the positive side of capacitor C_1 is switched to +5V and the negative side is connected to ground, and the cycle begins again.

Since both V^+ and V^- are separately generated from V_{CC}; in a no–load condition V^+ and V^- will be symmetrical. Older charge pump approaches that generate V^- from V^+ will show a decrease in the magnitude of V^- compared to V^+ due to the inherent inefficiencies in the design.

The clock rate for the charge pump typically operates at 15kHz. The external capacitors can be as low as 0.1µF with a 16V breakdown voltage rating.

The **SP200 Series** devices are made up of three basic circuit blocks — 1) transmitter/driver, 2) receiver and 3) the **Sipex**–proprietary charge

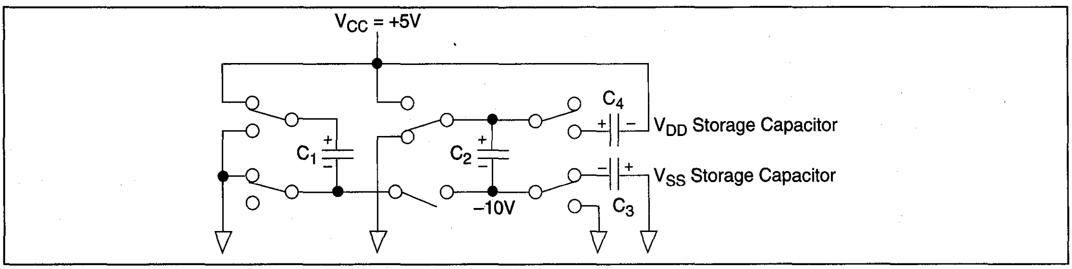


Figure 2. Charge Pump — Phase 2

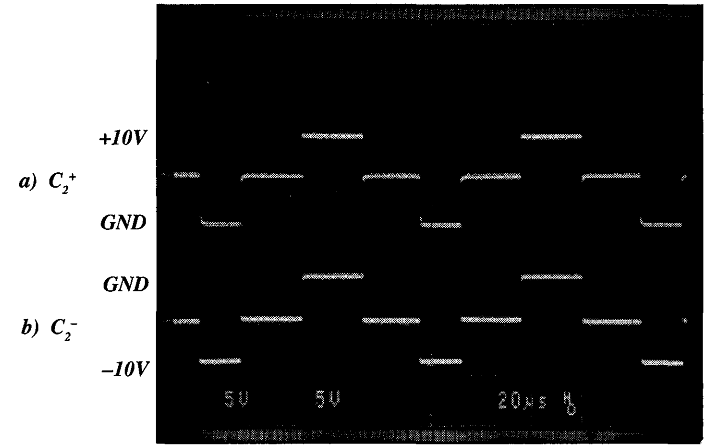


Figure 3. Charge Pump Waveforms

pump. Each model within the Series incorporates variations of these circuits to achieve the desired configuration and performance.

Transmitter/Driver

The drivers are inverting transmitters, which accept either TTL or CMOS inputs and output the RS-232 signals with an inverted sense relative to the input logic levels. Typically, the RS-232 output voltage swing is ±9V with no load, and ±5V minimum with full load. The transmitter outputs are protected against infinite short–circuits to ground without degradation in reliability. The drivers of the **SP200**, **SP205**, **SP205B**, **SP206**, **SP206B**, **SP207B, SP211**, **SP211B** and **SP213** can be tri–stated by using the SHUTDOWN function.

In the "power off" state, the output impedance will remain greater than 300 ohms, again satisfying the RS232 specifications. Should the input of the driver be left open, an internal 400Kohm pullup resistor to V_{CC} forces the input high, thus committing the output to a low state. The slew rate of the transmitter output is internally limited to a maximum of 30V/µs in order to meet the EIA standards (EIA RS-232D 2.1.7, Paragraph 5). The transition of the loaded output from high to low also meets the monotonicity requirements of the standard.

Receivers

The receivers convert RS-232 input signals to inverted TTL signals. Since the input is usually from a transmission line where long cable lengths and system interference can degrade the signal, the inputs have a typical hysteresis margin of 500mV. This ensures that the receiver is virtually immune to noisy transmission lines. Should an input be left unconnected, a 5Kohm pulldown resistor to ground will commit the output of the receiver to a high state.

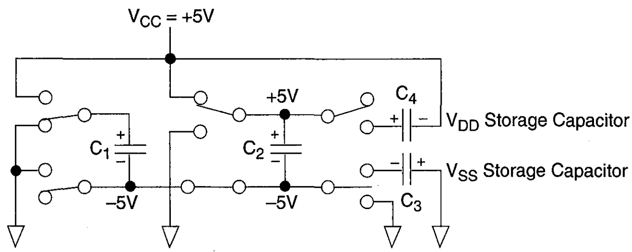


Figure 4. Charge Pump — Phase 3

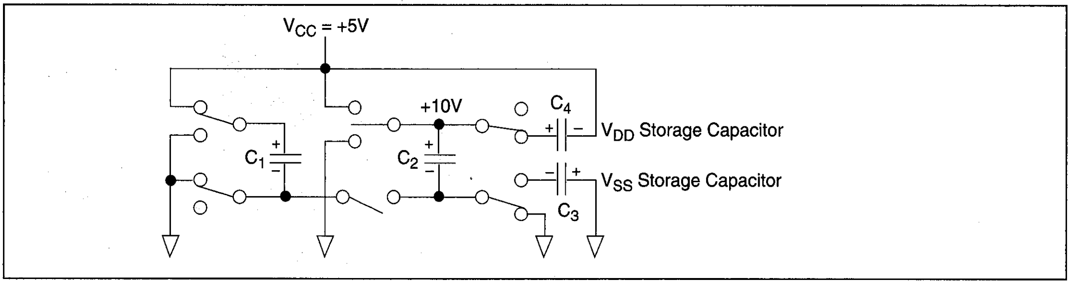


Figure 5. Charge Pump — Phase 4

SHUTDOWN MODE

The **SP200**, **SP205**, **SP205B**, **SP206**, **SP206B**, **SP207B**, **SP211**, **SP211B** and **SP213** all feature a control input which will disable the device and reduce the power supply current to less than 10μA, making the parts ideal for battery–powered systems. In the "shutdown" mode the receivers and transmitters will both be tri–stated. The V^+ output of the charge pump will discharge to V_{CC}, and the V^- output will discharge to ground. Products with the WakeUp function can enable or disable the receivers during shutdown.

For complete shutdown to occur and the 10μA power drain to be realized, the following conditions must be met:

SP200, **SP205/B**, **SP206/B**, **SP207B** and **SP211/B**:

- +5V must be applied to the SD pin
- ENABLE must be either 0V, +5.0V or not connected
- the transmitter inputs must be either +5.0V or not connected
- V_{CC} must be +5V
- Receiver inputs must be >0V and <+5V

SP213:

- 0V must be applied to the SD pin
- ENABLE must be either 0V, +5.0V or not connected
- the transmitter inputs must be either +5.0V or not connected
- V_{CC} must be +5V
- Receiver inputs must be >0V and <+5V

ENABLE

The **SP205/B**, **SP206/B**, **SP207/B**, **SP211** and **SP213** all feature an enable input, which allows the receiver outputs to be either tri–stated or enabled. This can be especially useful when the receiver is tied directly to a microprocessor data bus. For the **SP205/B**, **SP206/B**, **SP207/B** and **SP211**, enable is active low; that is, 0V applied to the ENABLE pin will enable the receiver outputs. For the **SP213**, enable is active high; that is, +5V applied to the ENABLE pin will enable the receiver outputs.

		SP213 Only		Power	Receiver
SD	$\overline{EN}$	$\overline{SD}$	EN	Up/Down	Outputs
0	0	1	1	Up	Enable
0	1	1	0	Up	Tri–state
1	0	0	1	Down	Enable
1	1	0	0	Down	Tri–state

Table 2. Wake–Up Truth Table

WAKEUP FUNCTION

The **SP205B**, **SP206B**, **SP207B**, **SP211B** and **SP213** have a wake–up feature that keeps two or more receivers in an enabled state when the device is in the shutdown mode. The **SP213** has two receivers active (R_4 and R_5), while the **SP205B**, **SP207B** and **SP211B** have all receivers active during shutdown. With only the receivers active during shutdown, the devices draw 5–10μA of supply current.

A typical application of this function would be where a modem is interfaced to a computer in a power–down mode. The ring indicator signal from the modem could be passed through an active receiver in the **SP2XXB/SP213** that is itself in the shutdown mode. The ring indicator signal would propagate through the **SP2XXB/SP213** to the power management circuitry of the computer to power up the microprocessor and the **SP2XXB/SP213** drivers. After the supply voltage to the **SP2XXB/SP213** reaches +5.0V, the SHUTDOWN pin can be disabled, taking the **SP2XXB/SP213** out of the shutdown mode.

All receivers that are active during shutdown maintain 500mV (typ.) of hysteresis.

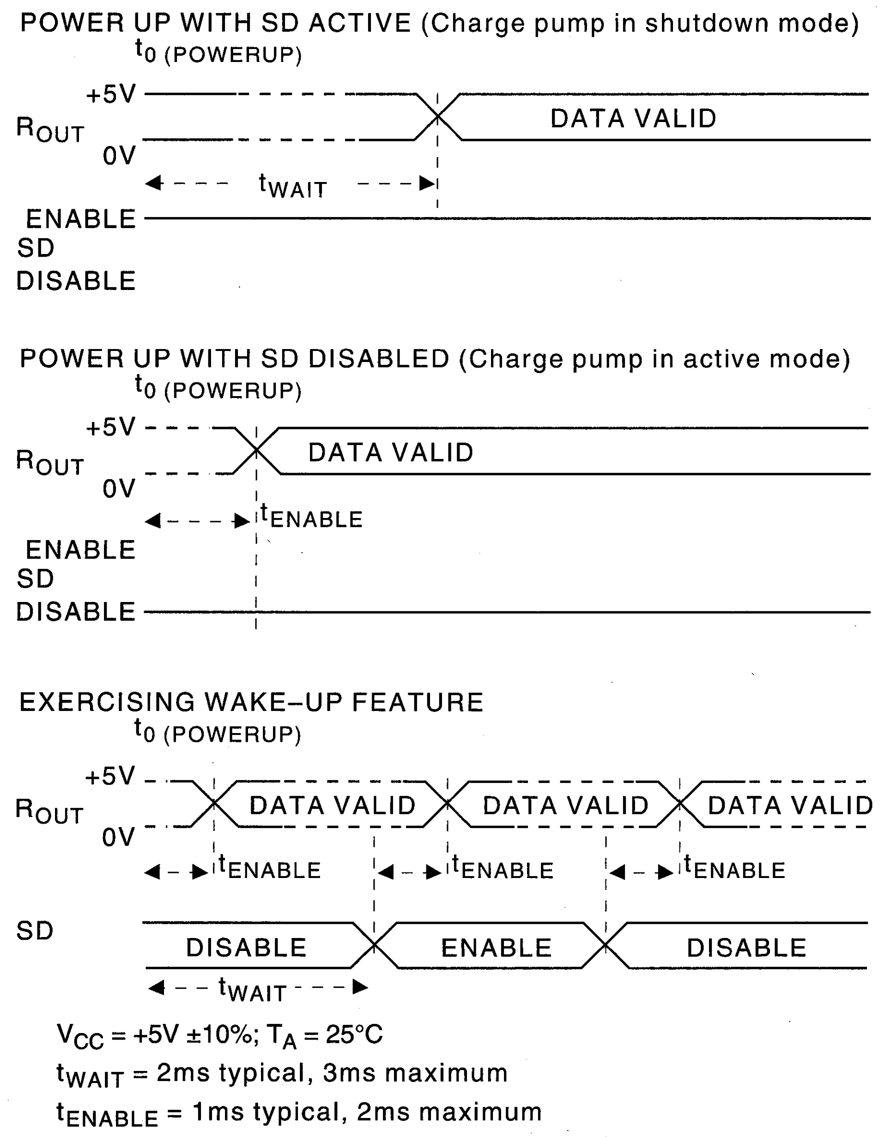


Figure 6. Wake–Up Timing

Specification	RS-232D	RS-423A	RS-422	RS-485	RS-562
Mode of Operation	Single-Ended	Single-Ended	Differential	Differential	Single-Ended
No. of Drivers and Receivers Allowed on One Line	1 Driver 1 Receiver	1 Driver 10 Receivers	1 Driver 10 Receivers	32 Drivers 32 Receivers	1 Driver 1 Receiver
Maximum Cable Length	50 feet	4,000 feet	4,000 feet	4,000 feet	C ≤ 2,500pF @ <20Kbps; C ≤1,000pF @ >20Kbps
Maximum Data Rate	20Kb/s	100Kb/s	10Mb/s	10Mb/s	64Kb/s
Driver output Maximum Voltage	±25V	±6V	–0.25V to +6V	–7V to +12V	–3.7V to +13.2V
Driver Output Signal Level Loaded Unloaded	 ±5V ±15V	 ±3.6V ±6V	 ±2V ±5V	 ±1.5V ±5V	 ±3.7V ±13.2V
Driver Load Impedance	3 – 7Kohm	450 ohm	100 ohm	54 ohm	3–7Kohm
Max. Driver Output Current (High Impedance State) Power On Power Off	 V_{MAX}/300	 100µA	 ±100µA	 ±100µA ±100µA	
Slew Rate	30V/µs max.	Controls Provided			30V/µs max.
Receiver Input Voltage Range	±15V	±12V	–7V to +7V	–7V to +12V	±15V
Receiver Input Sensitivity	±3V	±200mV	±200mV	±200mV	±3V
Receiver Input Resistance	3–7Kohm	4Kohm min.	4Kohm min.	12Kohm min.	3–7Kohm

Table 3. EIA Standard Definitions

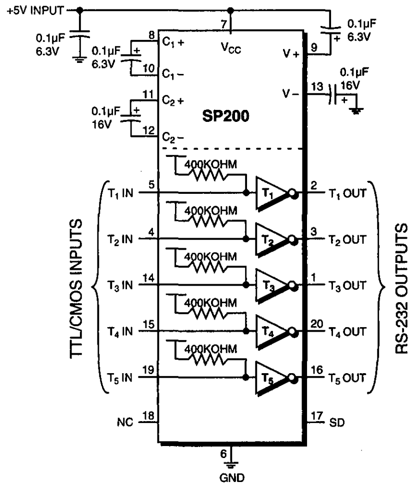
EIA STANDARDS

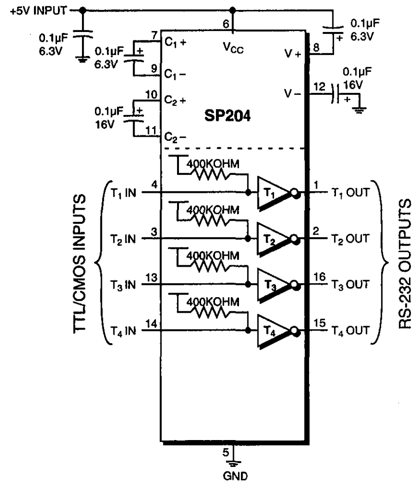
The Electronic Industry Association (EIA) developed several standards of data transmission which are revised and updated in order to meet the requirements of the industry. In data processing, there are two basic means of communicating between systems and components. The RS-232 standard was first introduced in 1962 and, since that time, has become an industry standard.

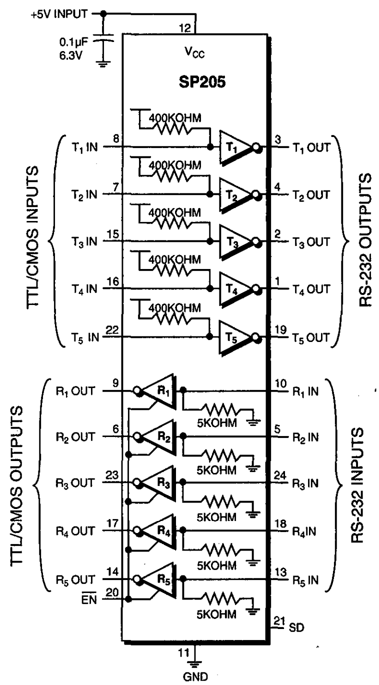
The RS-232 is a relatively slow data exchange protocol, with a maximum baud rate of only 20Kbaud, which can be transmitted over a maximum copper wire cable length of 50 feet. The **SP200** through **SP213** Series of data communications interface products have been designed to meet both the EIA protocol standards, and the needs of the industry.

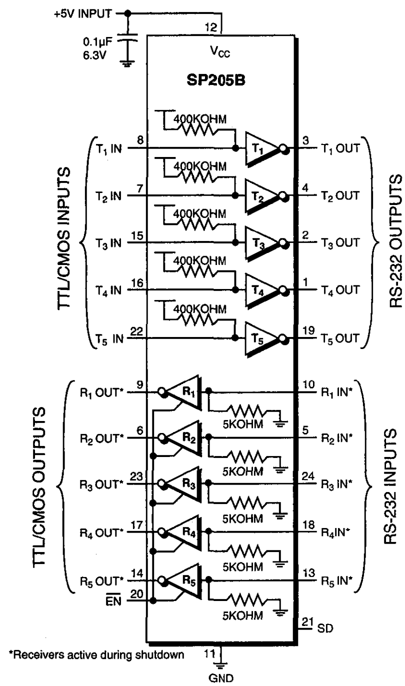
±10KV ESD PROTECTION

The **SP200** Series is equipped with **Sipex**-proprietary ESD protection circuitry on all RS-232 inputs and outputs. The **SP200** Series has been characterized using MIL-STD-883C Method 3015.7 Human Body Model. Each device in the family can withstand up to ±10KV of static discharge on all RS-232 inputs and outputs. All other pins of each device will maintain ≥ ±2KV of ESD protection.

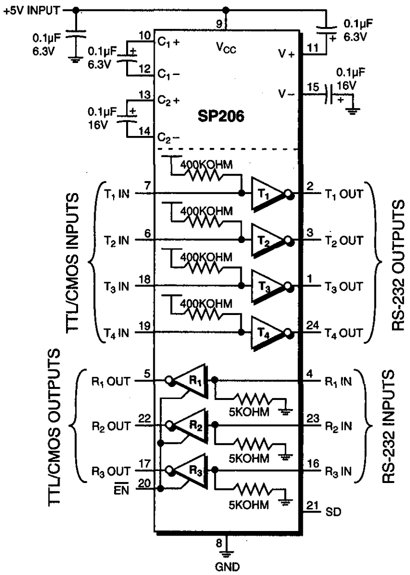

+5V INPUT
0.1μF 6.3V
0.1μF 6.3V
0.1μF 16V
SP200
V_{CC}
C_1+
C_1–
C_2+
C_2–
V+
V–
400KOHM
TTL/CMOS INPUTS
RS-232 OUTPUTS
T_1 IN
T_2 IN
T_3 IN
T_4 IN
T_5 IN
T_1 OUT
T_2 OUT
T_3 OUT
T_4 OUT
T_5 OUT
NC
SD
GND

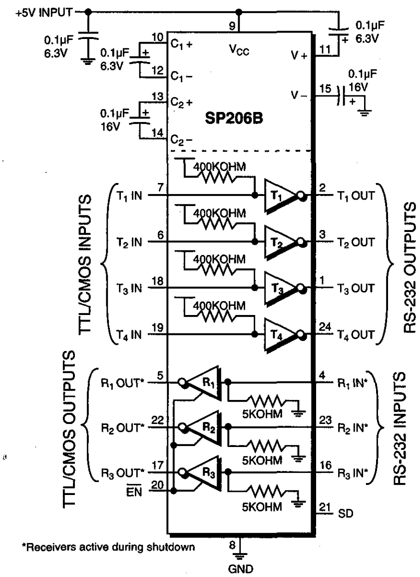

+5V INPUT
0.1μF 6.3V
0.1μF 6.3V
0.1μF 16V
SP204
V_{CC}
C_1+
C_1–
C_2+
C_2–
V+
V–
400KOHM
TTL/CMOS INPUTS
RS-232 OUTPUTS
T_1 IN
T_2 IN
T_3 IN
T_4 IN
T_1 OUT
T_2 OUT
T_3 OUT
T_4 OUT
GND

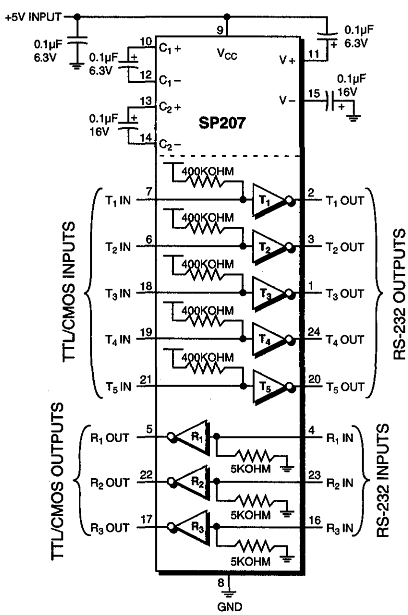

+5V INPUT
0.1μF 6.3V
V_{CC}
SP205
400KOHM
5KOHM
TTL/CMOS INPUTS
RS-232 OUTPUTS
TTL/CMOS OUTPUTS
RS-232 INPUTS
T_1 IN
T_2 IN
T_3 IN
T_4 IN
T_5 IN
T_1 OUT
T_2 OUT
T_3 OUT
T_4 OUT
T_5 OUT
R_1 OUT
R_2 OUT
R_3 OUT
R_4 OUT
R_5 OUT
$\overline{EN}$
R_1 IN
R_2 IN
R_3 IN
R_4IN
R_5 IN
SD
GND

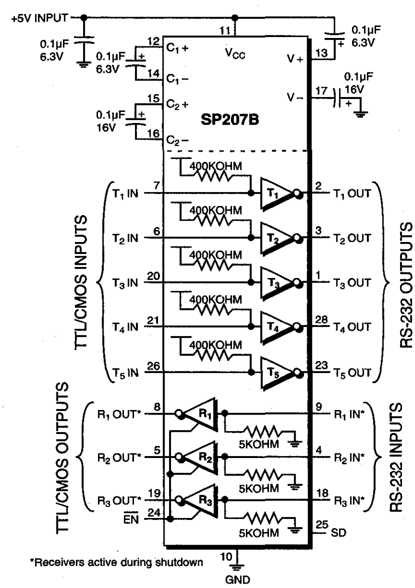

+5V INPUT
0.1μF 6.3V
V_{CC}
SP205B
400KOHM
5KOHM
TTL/CMOS INPUTS
RS-232 OUTPUTS
TTL/CMOS OUTPUTS
RS-232 INPUTS
T_1 IN
T_2 IN
T_3 IN
T_4 IN
T_5 IN
T_1 OUT
T_2 OUT
T_3 OUT
T_4 OUT
T_5 OUT
R_1 OUT*
R_2 OUT*
R_3 OUT*
R_4 OUT*
R_5 OUT*
$\overline{EN}$
R_1 IN*
R_2 IN*
R_3 IN*
R_4IN*
R_5 IN*
SD
*Receivers active during shutdown
GND

TYPICAL APPLICATION CIRCUITS



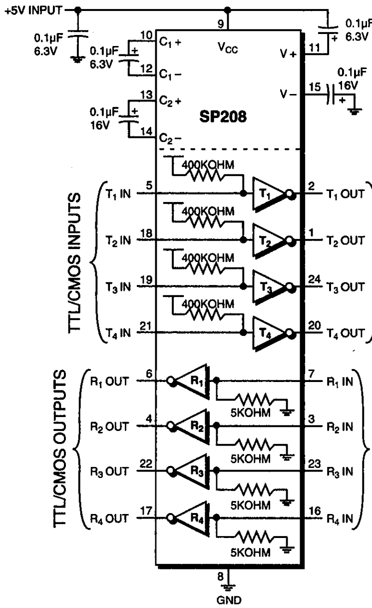


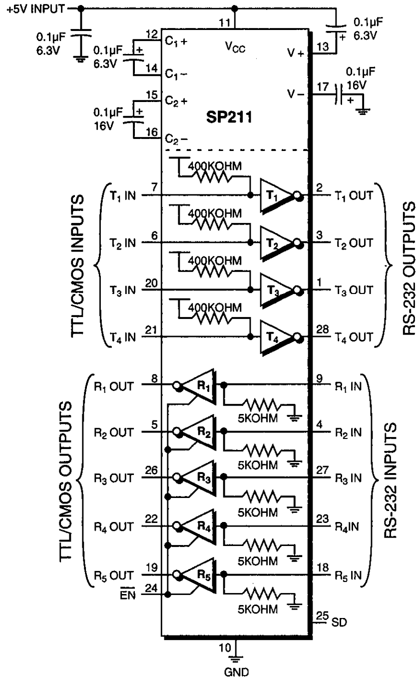


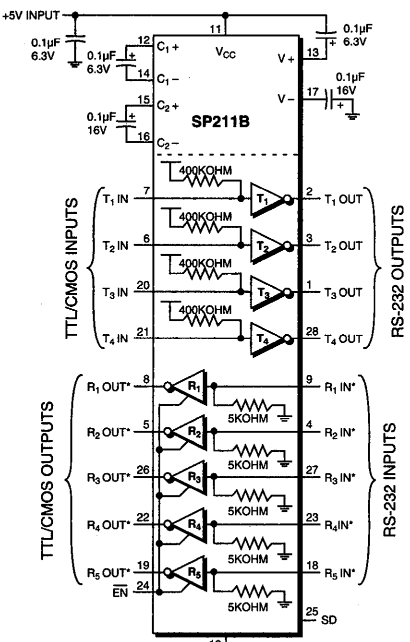


The **SP207B** is offered in a 28–pin SOIC or 28–pin SSOP package.

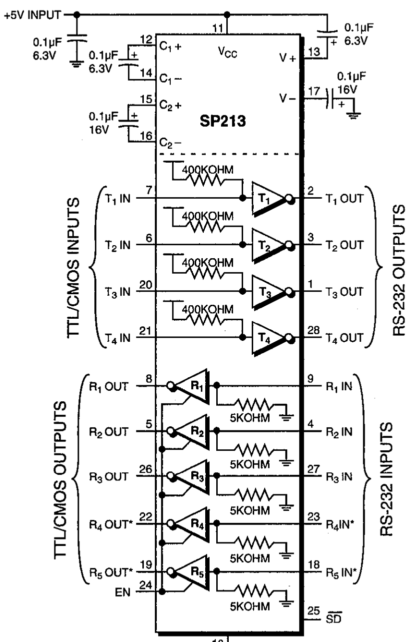
TYPICAL APPLICATION CIRCUITS







*Receivers active during shutdown



*Receivers active during shutdown

ORDERING INFORMATION

RS-232 Transceivers:

Model	Drivers	Receivers	Temperature Range	Package Type
SP207CA	5	3	0°C to +70°C	24–pin SSOP
SP207CP	5	3	0°C to +70°C	24–pin Plastic DIP
SP207CT	5	3	0°C to +70°C	24–pin SOIC
SP207EA	5	3	–40°C to +85°C	24–pin SSOP
SP207EP	5	3	–40°C to +85°C	24–pin Plastic DIP
SP207ET	5	3	–40°C to +85°C	24–pin SOIC
SP208CA	4	4	0°C to +70°C	24–pin SSOP
SP208CP	4	4	0°C to +70°C	24–pin Plastic DIP
SP208CT	4	4	0°C to +70°C	24–pin SOIC
SP208EA	4	4	–40°C to +85°C	24–pin SSOP
SP208EP	4	4	–40°C to +85°C	24–pin Plastic DIP
SP208ET	4	4	–40°C to +85°C	24–pin SOIC

RS-232 Transmitters:

Model	Drivers	Receivers	Temperature Range	Package Type
SP204CP	4	0	0°C to +70°C	16–pin Plastic DIP
SP204CT	4	0	0°C to +70°C	16–pin SOIC
SP204EP	4	0	–40°C to +85°C	16–pin Plastic DIP
SP204ET	4	0	–40°C to +85°C	16–pin SOIC

RS-232 Transmitters with Low–Power Shutdown:

Model	Drivers	Receivers	Temperature Range	Package Type
SP200CP	5	0	0°C to +70°C	20–pin Plastic DIP
SP200CT	5	0	0°C to +70°C	20–pin SOIC
SP200EP	5	0	–40°C to +85°C	20–pin Plastic DIP
SP200ET	5	0	–40°C to +85°C	20–pin SOIC

RS-232 Transceivers with Low–Power Shutdown and Tri–state Enable:

Model	Drivers	Receivers	Temperature Range	Package Type
SP205CP	5	5	0°C to +70°C	24–pin Plastic Double–Width DIP
SP205EP	5	5	–40°C to +85°C	24–pin Plastic Double–Width DIP
SP206CA	4	3	0°C to +70°C	24–pin SSOP
SP206CP	4	3	0°C to +70°C	24–pin Plastic DIP
SP206CT	4	3	0°C to +70°C	24–pin SOIC
SP206EA	4	3	–40°C to +85°C	24–pin SSOP
SP206EP	4	3	–40°C to +85°C	24–pin Plastic DIP
SP206ET	4	3	–40°C to +85°C	24–pin SOIC
SP211CA	4	5	0°C to +70°C	28–pin SSOP
SP211CT	4	5	0°C to +70°C	28–pin SOIC
SP211EA	4	5	–40°C to +85°C	28–pin SSOP
SP211ET	4	5	–40°C to +85°C	28–pin SOIC

ORDERING INFORMATION

RS-232 Transceivers with Low–Power Shutdown, Tri–state Enable, and Wake–Up Function:

Model	Drivers	Receivers	Temperature Range	Package Type
SP205BCP	5	5, with 5 active in Shutdown	0°C to +70°C	24–pin Plastic Double–WidthDIP
SP205BEP	5	5, with 5 active in Shutdown	–40°C to +85°C	24–pin Plastic Double–Width DIP
SP206BCA	4	3, with 3 active in Shutdown	0°C to +70°C	24–pin SSOP
SP206BCP	4	3, with 3 active in Shutdown	0°C to +70°C	24–pin Plastic DIP
SP206BCT	4	3, with 3 active in Shutdown	0°C to +70°C	24–pin SOIC
SP206BEA	4	3, with 3 active in Shutdown	–40°C to +85°C	24–pin SSOP
SP206BEP	4	3, with 3 active in Shutdown	–40°C to +85°C	24–pin Plastic DIP
SP206BET	4	3, with 3 active in Shutdown	–40°C to +85°C	24–pin SOIC
SP207BCA	5	3, with 3 active in Shutdown	0°C to +70°C	28–pin SSOP
SP207BCT	5	3, with 3 active in Shutdown	0°C to +70°C	28–pin SOIC
SP207BEA	5	3, with 3 active in Shutdown	–40°C to +85°C	28–pin SSOP
SP207BET	5	3, with 3 active in Shutdown	–40°C to +85°C	28–pin SOIC
SP211BCA	4	5, with 5 active in Shutdown	0°C to +70°C	28–pin SSOP
SP211BCT	4	5, with 5 active in Shutdown	0°C to +70°C	28–pin SOIC
SP211BEA	4	5, with 5 active in Shutdown	–40°C to +85°C	28–pin SSOP
SP211BET	4	5, with 5 active in Shutdown	–40°C to +85°C	28–pin SOIC
SP213CA	4	5, with 2 active in Shutdown	0°C to +70°C	28–pin SSOP
SP213CT	4	5, with 2 active in Shutdown	0°C to +70°C	28–pin SOIC
SP213EA	4	5, with 2 active in Shutdown	–40°C to +85°C	28–pin SSOP
SP213ET	4	5, with 2 active in Shutdown	–40°C to +85°C	28–pin SOIC

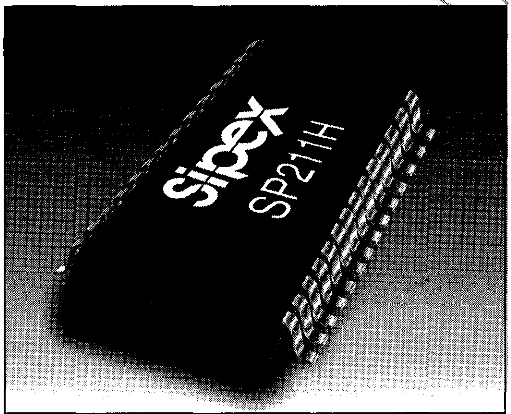
THIS PAGE LEFT INTENTIONALLY BLANK

SP207H/SP211H

+5V 400 kbps RS-232 Transceivers

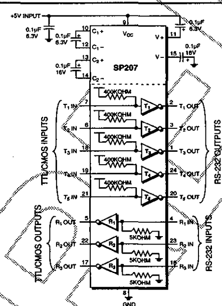
- Single 5V Supply Operation
- 0.1µF External Charge Pump Capacitors
- 400kbps Data Rate
- Standard SOIC and SSOP Packages
- SP207H - Five (5) Drivers and Three (3) Receivers

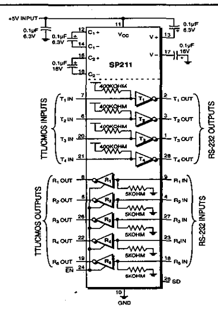
  SP211H - Four (4) Drivers and Five (5) Receivers
- 1µA Shutdown Mode
- WakeUp Feature in Shutdown Mode
- Tri–State Receiver Outputs
- Ideal for V.34 and High Speed RS-232 Type Applications



DESCRIPTION...

The **SP207H** and **SP211H** are multi–channel RS-232 line transceivers configured to fit most communication needs. The "H" series is based on **Sipex**'s **SP200** Series transceivers and has been enhanced for speed. The data rate is improved to over 400kbps which easily meets the 230.4kbps data rates for V.34. The **SP207H** and **SP211H** use the same on-board charge pump to provide ±10V voltage levels, using 0.1µF charge pump capacitors to save board space and reduce circuit cost. The **SP207HB**, **SP211H** and **SP211HB** feature a low–power shutdown mode, which reduces power supply drain to 1µA. A WakeUp function keeps the receivers active in the shutdown mode (**SP207HB** and **SP211HB** only).





Model	Number of RS-232 Drivers	Number of RS-232 Receivers	No. of Receivers Active in Shutdown	No. of External 0.1µF Capacitors	Shutdown	WakeUp	TTL Tri–State
SP207H	5	3	0	4	No	No	No
SP207HB	5	3	3	4	Yes	Yes	Yes
SP211H	4	5	0	4	Yes	No	Yes
SP211HB	4	5	5	4	Yes	Yes	Yes

Table 1. Model Selection Table

ABSOLUTE MAXIMUM RATINGS

These are stress ratings only and functional operation of the device at these or any other above those indicated in the operation sections of the specifications below is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

V_{CC} .... +6V
V^+ .... (V_{CC} – 0.3V) to +13.2V
V^- 13.2V
Input Voltages
T_{IN} .... –0.3V to (V_{CC} +0.3V)
R_{IN} .... ±20V
Output Voltages
T_{OUT} .... (V^+, +0.3V) to (V^-, –0.3V)
R_{OUT} .... –0.3V to (V_{CC} +0.3V)
Short Circuit Duration on T_{OUT} .... Continuous
Power Dissipation
Plastic DIP 375mW
(derate 7mW/°C above +70°C)
Small Outline 375mW
(derate 7mW/°C above +70°C)

SPECIFICATIONS

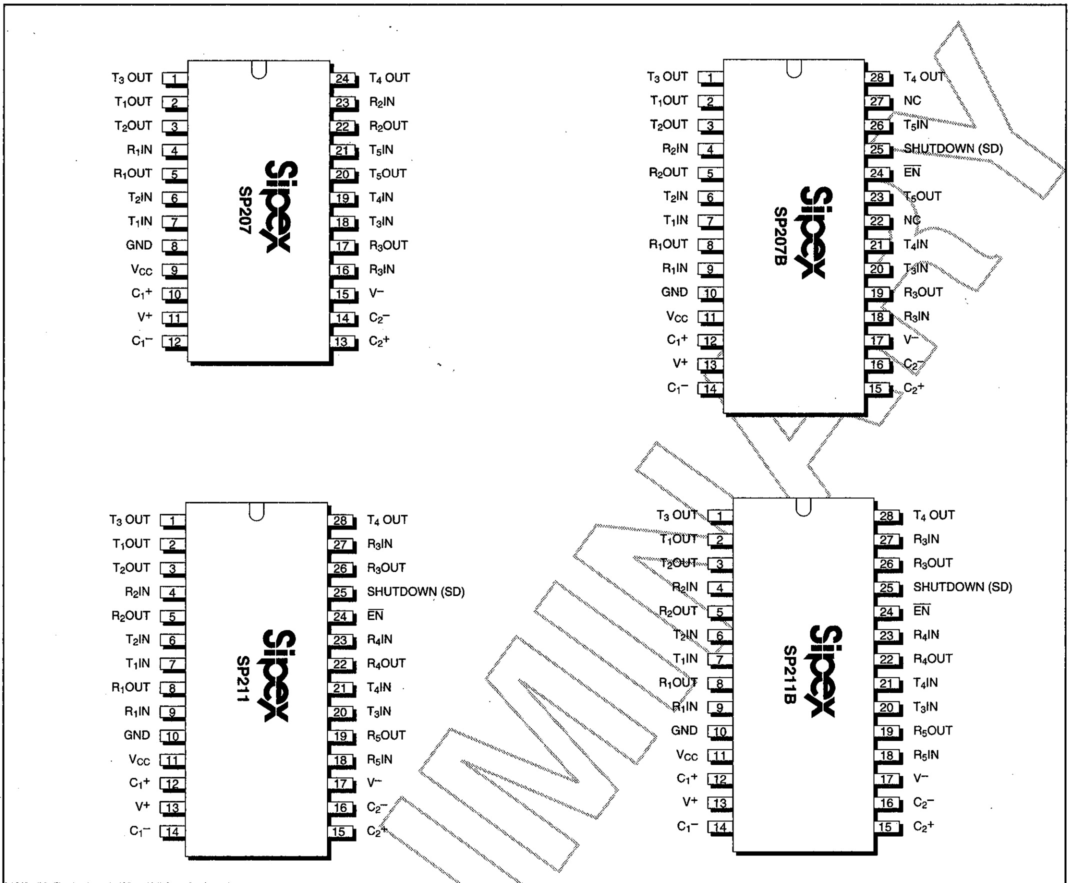
V_{CC} at nominal ratings; 0.1μF charge pump capacitors; T_{MIN} to T_{MAX}, unless otherwise noted.

PARAMETER	MIN.	TYP.	MAX.	UNIT	CONDITIONS
TTL INPUTS (DRIVER)					T_{IN}, EN, SD
Logic Threshold					
V_{IL}			0.8	Volts	
V_{IH}	2.0			Volts	
Logic Pullup Current		1.5	10.0	μA	T_{IN} = 0V
Data Rate		400		kbps	C_L = 2,500pF, R_L = 3KΩ
TTL OUTPUTS (RECEIVER)					R_{OUT}
Compatibility		TTL/CMOS			
V_{OL}			0.4	Volts	I_{OUT} = 3.2mA; V_{CC} = +5V
V_{OH}	3.5			Volts	I_{OUT} = –1.0mA
Leakage Current		0.05	±10	μA	EN = V_{CC}; 0V ≤ R_{OUT} ≤ V_{CC}; T_A = +25°C
RS-232 OUTPUT (DRIVER)					
Output Voltage Swing	±5	±7		Volts	All transmitter outputs loaded with 3KΩ to ground
Output Resistance	300			Ohms	V_{CC} = 0V; V_{OUT} = ±2V
Output Short Circuit Current		±25		mA	Infinite duration
RS-232 INPUT (RECEIVER)					
Voltage Range	–15		+15	Volts	
Logic Pull Down Current		3.0	10.0	μA	
Voltage Threshold					
Low	0.8	1.2		Volts	V_{CC} = +5V, T_A = +25°C
High		1.7	2.4	Volts	V_{CC} = +5V, T_A = +25°C
Hysteresis	0.2	0.5	1.0	Volts	V_{CC} = +5V
Resistance	3	5	7	KΩ	V_{IN} = ±15V; T_A = +25°C
Data Rate		400		kbps	
DYNAMIC CHARACTERISTICS					
Propagation Delay		1.0		μS	TTL–to–RS-232
		1.5		μs	RS-232–to–TTL
Instantaneous Slew Rate		60		V/μs	C_L = 50pF, R_L = 3–7KΩ; T_A = +25°C
Transition Region Slew Rate		5		V/μs	C_L = 2,500pF, R_L = 3KΩ; measured from +3V to –3V or –3V to +3V

SPECIFICATIONS

V_{CC} at nominal ratings; 0.1µF charge pump capacitors; T_{MIN} to T_{MAX}, unless otherwise noted.

PARAMETER	MIN.	TYP.	MAX.	UNIT	CONDITIONS
Output Enable Time		400		ns	
Output Disable Time		250		ns	
POWER REQUIREMENTS					
V_{CC}	4.75	5.00	5.25	Volts	
I_{CC}					T_A = +25°C
		5		mA	No load; V_{CC} = ±10%
		20		mA	All transmitters R_L = 3KΩ
Shutdown Current		1	10	µA	T_A = +25°C
ENVIRONMENTAL AND MECHANICAL					
Operating Temperature					
Commercial, –C	0		+70	°C	
Extended, –E	–40		+85	°C	
Storage Temperature	–65		+125	°C	
Package					
–A	Shrink (SSOP) small outline				
–T	Wide (SOIC) small outline				



FEATURES...

The **SP207H** and **SP211H** line transceivers provide a variety of configurations to fit most communication needs, especially those applications where ±12V is not available. Both products feature low–power CMOS construction and **Sipex**–proprietary on-board charge pump circuitry to generate the ±10V RS-232 voltage levels. The ability to use 0.1µF charge pump capacitors saves board space and reduces circuit cost.

The **SP207HB** and **SP211H** models feature a low–power shutdown mode, which reduces power supply drain to 1µA. The **SP207HB** and **SP211HB** are equipped with the WakeUp function. The WakeUp function keeps the receivers active in the shutdown mode, unless disabled by the $\overline{EN}$ pin.

THEORY OF OPERATION

The **SP207H** and **SP211H** are made up of three basic circuit blocks — 1) transmitter/driver, 2) receiver and 3) the **Sipex**–proprietary charge pump.

Charge–Pump

The charge pump is a **Sipex**–patented design (5,306,954) and uses a unique approach compared to older less–efficient designs. The charge pump still requires four external capacitors, but uses a four–phase voltage shifting technique to attain symmetrical 10V power supplies. *Figure 3a* shows the waveform found on the positive side of capcitor C_2, and *Figure 3b* shows the

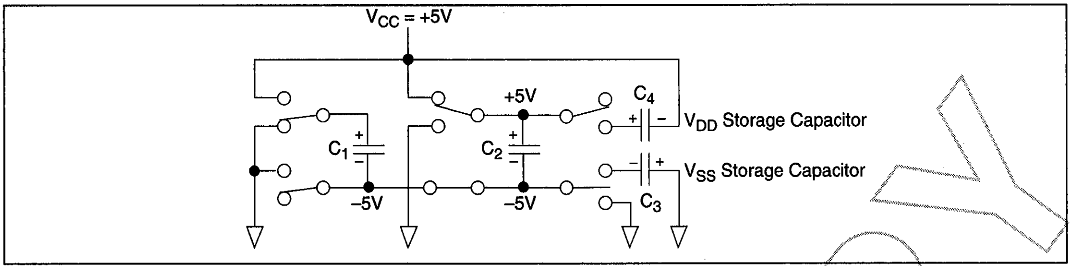


Figure 1. Charge Pump — Phase 1

negative side of capcitor C_2. There is a free–running oscillator that controls the four phases of the voltage shifting. A description of each phase follows.

Phase 1

— V_{SS} charge storage —During this phase of the clock cycle, the positive side of capacitors C_1 and C_2 are initially charged to +5V. C_1^+ is then switched to ground and the charge in C_1^- is transferred to C_2^-. Since C_2^+ is connected to +5V, the voltage potential across capacitor C_2 is now 10V.

Phase 2

— V_{SS} transfer — Phase two of the clock connects the negative terminal of C_2 to the V_{SS} storage capacitor and the positive terminal of C_2 to ground, and transfers the generated –10V to C_3. Simultaneously, the positive side of capacitor C_1 is switched to +5V and the negative side is connected to ground.

Phase 3

— V_{DD} charge storage — The third phase of the clock is identical to the first phase — the charge transferred in C_1 produces –5V in the negative terminal of C_1, which is applied to the negative side of capacitor C_2. Since C_2^+ is at +5V, the voltage potential across C_2 is 10V.

Phase 4

— V_{DD} transfer — The fourth phase of the clock connects the negative terminal of C_2 to ground, and transfers the generated 10V across C_2 to C_4, the V_{DD} storage capacitor. Again, simultaneously with this, the positive side of capacitor C_1 is switched to +5V and the negative side is connected to ground, and the cycle begins again.

Since both V^+ and V^- are separately generated from V_{CC}; in a no–load condition V^+ and V^- will be symmetrical. Older charge pump approaches that generate V^- from V^+ will show a decrease in the magnitude of V^- compared to V^+ due to the inherent inefficiencies in the design.

The clock rate for the charge pump typically operates at 15kHz. The external capacitors can be as low as 0.1μF with a 16V breakdown voltage rating.

Transmitter/Driver

The drivers are inverting transmitters which have been improved for speed over the **SP200 Series**. The transmitters accept either TTL or CMOS inputs and output the RS-232 signals at data rates over 400kbps. Typically, the RS-232 output volt-

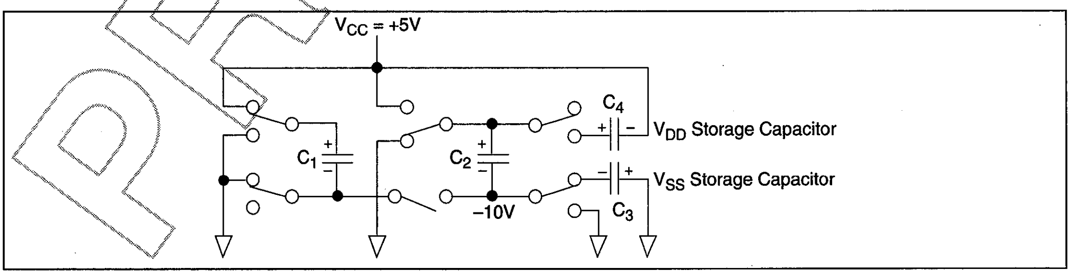


Figure 2. Charge Pump — Phase 2

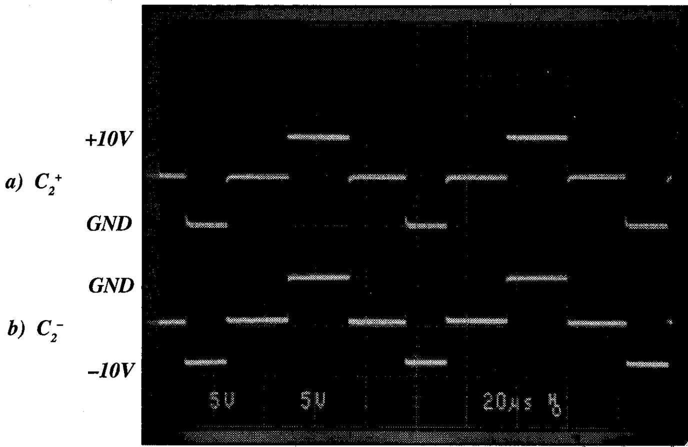


Figure 3. Charge Pump Waveforms

age swing is ±9V with no load, and ±5V minimum with full load. The transmitter outputs are protected against infinite short–circuits to ground without degradation in reliability. The **SP207HB, SP211H** and **SP211HB** drivers can be tri–stated by using the SHUTDOWN function.

In the "power off" state, the output impedance will remain greater than 300 ohms, again satisfying the RS-232 specifications. Should the input of the driver be left open, an internal 400Kohm pullup resistor to V_{CC} forces the input high, thus committing the output to a low state.

Because of the increased speed, the slew rate is typically 60V/µS which is above the RS-232 specifcation of 30V/µS. This is the only parameter that exceeds the RS-232 limits.

Receivers

The receivers convert RS-232 input signals to inverted TTL signals. Since the input is usually from a transmission line where long cable lengths and system interference can degrade the signal, the inputs have a typical hysteresis margin of 500mV. This ensures that the receiver is virtually immune to noisy transmission lines. Should an input be left unconnected, a 5Kohm pulldown resistor to ground will commit the output of the receiver to a high state.

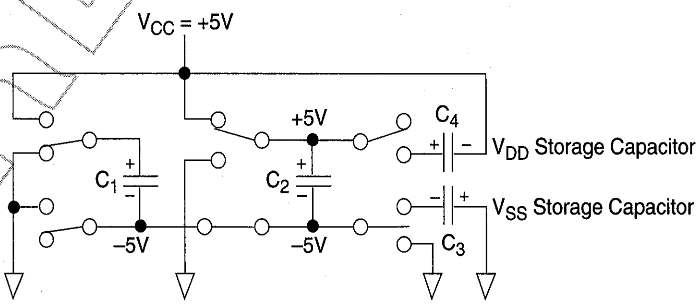


Figure 4. Charge Pump — Phase 3

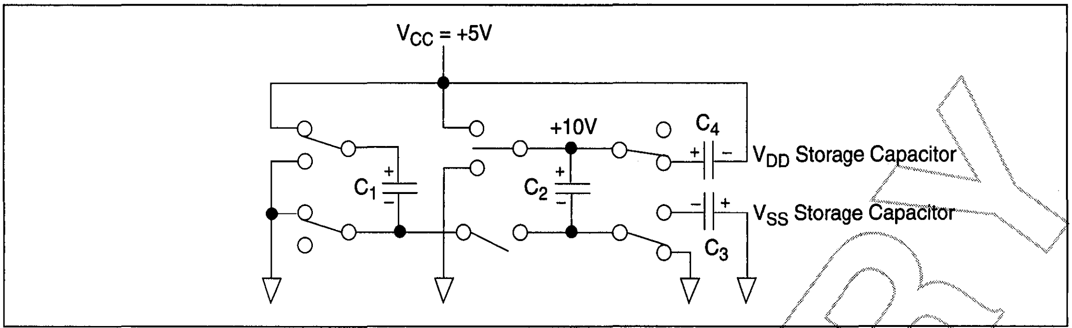


Figure 5. Charge Pump — Phase 4

SHUTDOWN MODE

The **SP207HB**, **SP211H** and **SP211HB** all feature a control input which will disable the device and reduce the power supply current to less than 10µA, making the parts ideal for battery–powered systems. In the "shutdown" mode the receivers and transmitters will both be tri–stated. The V^+ output of the charge pump will discharge to V_{CC}, and the V^- output will discharge to ground.

For complete shutdown to occur and the 10µA power drain to be realized, the following conditions must be met:

- +5V must be applied to the SD pin
- ENABLE must be either 0V, +5.0V or not connected
- the transmitter inputs must be either +5.0V or not connected
- V_{CC} must be +5V
- Receiver inputs must be >0V and <+5V

ENABLE

The **SP207HB, SP211H** and **SP211HB** feature an enable input pin, which allows the receiver outputs to be either tri–stated or enabled. This can be especially useful when the receiver is tied directly to a microprocessor data bus. The enable is active low; that is, 0V applied to the ENABLE pin will enable the receiver outputs.

WAKEUP FUNCTION

The **SP207HB** and **SP211HB** have a wake–up feature that keeps all the receivers in an enabled state when the device is in the shutdown mode. With only the receivers active during shutdown, the devices draw 5–10µA of supply current. A typical application of this function would be where a modem is interfaced to a computer in a power–down mode. The ring indicator signal from the modem could be passed through an active receiver that is in the shutdown mode. The ring indicator signal would propagate through the receiver to the power management circuitry of the computer to power up the microprocessor and the **SP207HB/SP211HB** drivers. After the supply voltage to the transceivers reaches +5.0V, the SHUTDOWN pin can be disabled. All receivers that are active during shutdown maintain 500mV (typ.) of hysteresis.

SD	$\overline{EN}$	Power Up/Down	Receiver Outputs
0	0	Up	Enable
0	1	Up	Tri–state
1	0	Down	Tri-state
1	1	Down	Tri–state

Table 2. Truth Table for SP2xxH

SD	$\overline{EN}$	Power Up/Down	Receiver Outputs
0	0	Up	Enable
0	1	Up	Tri–state
1	0	Down	Enable
1	1	Down	Tri–state

Table 3. Wake–Up Truth Table for SP2xxHB

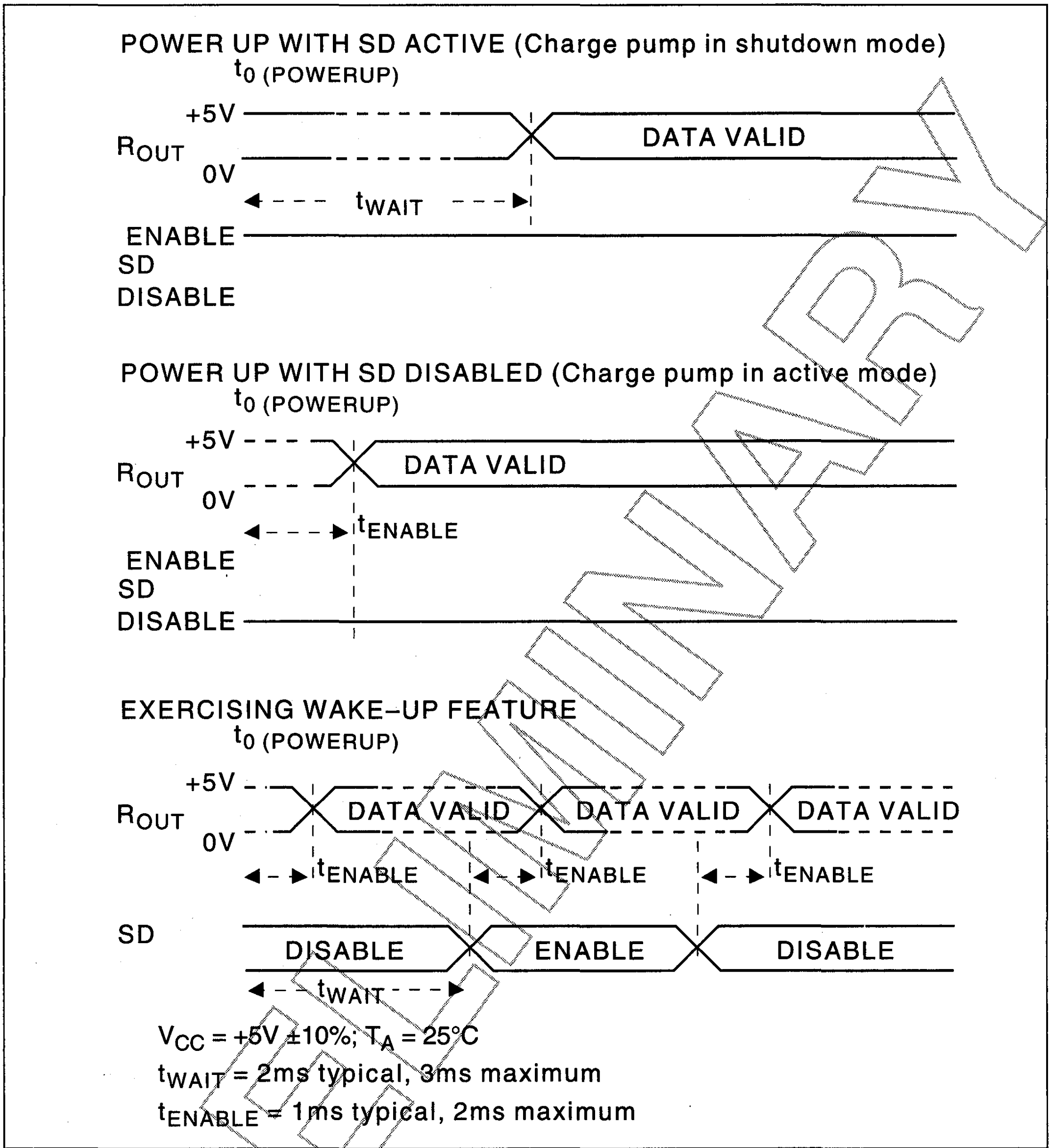
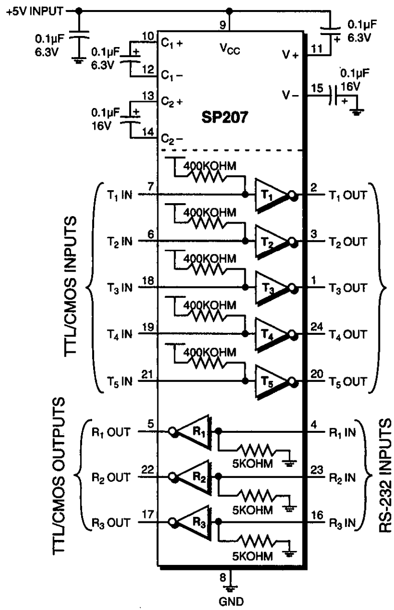
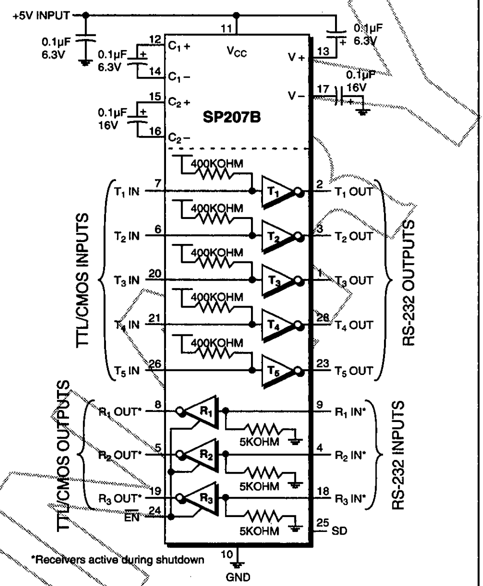
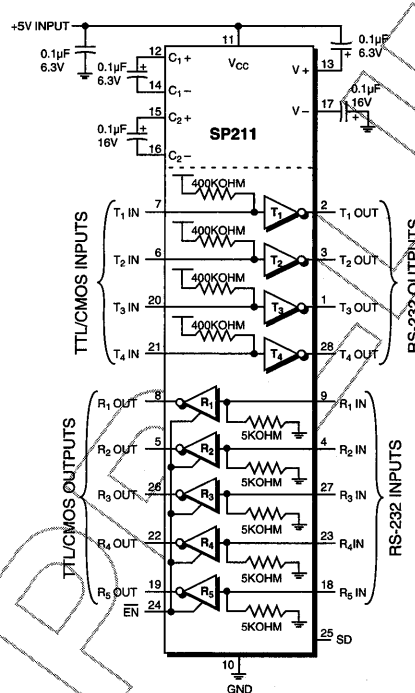


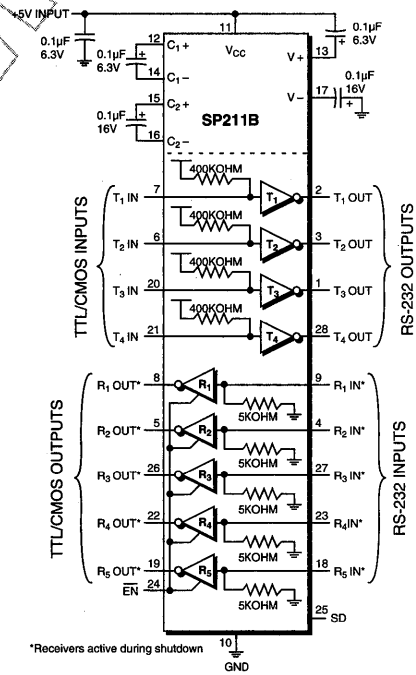
Figure 6. Wake–Up Timing





The SP207B is offered in a 28–pin SOIC or 28–pin SSOP package.





ORDERING INFORMATION

RS-232 Transceivers:

Model	Drivers	Receivers	Temperature Range	Package Type
SP207HCA	5	3	0°C to +70°C	24–pin SSOP
SP207HCP	5	3	0°C to +70°C	24–pin Plastic DIP
SP207HCT	5	3	0°C to +70°C	24–pin SOIC
SP207HEA	5	3	–40°C to +85°C	24–pin SSOP
SP207HEP	5	3	–40°C to +85°C	24–pin Plastic DIP
SP207HET	5	3	–40°C to +85°C	24–pin SOIC

RS-232 Transceivers with Low–Power Shutdown and Tri–state Enable:

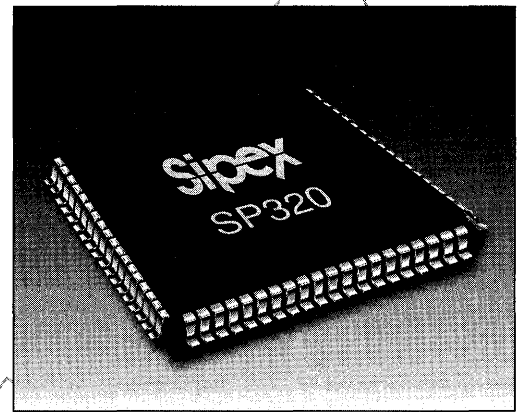
Model	Drivers	Receivers	Temperature Range	Package Type
SP211HCA	4	5	0°C to +70°C	28–pin SSOP
SP211HCT	4	5	0°C to +70°C	28–pin SOIC
SP211HEA	4	5	–40°C to +85°C	28–pin SSOP
SP211HET	4	5	–40°C to +85°C	28–pin SOIC

RS-232 Transceivers with Low–Power Shutdown, Tri–state Enable, and Wake–Up Function:

Model	Drivers	Receivers	Temperature Range	Package Type
SP207HBCA	5	3, with 3 active in Shutdown	0°C to +70°C	28–pin SSOP
SP207HBCT	5	3, with 3 active in Shutdown	0°C to +70°C	28–pin SOIC
SP207HBEA	5	3, with 3 active in Shutdown	–40°C to +85°C	28–pin SSOP
SP207HBET	5	3, with 3 active in Shutdown	–40°C to +85°C	28–pin SOIC
SP211HBCA	4	5, with 5 active in Shutdown	0°C to +70°C	28–pin SSOP
SP211HBCT	4	5, with 5 active in Shutdown	0°C to +70°C	28–pin SOIC
SP211HBEA	4	5, with 5 active in Shutdown	–40°C to +85°C	28–pin SSOP
SP211HBET	4	5, with 5 active in Shutdown	–40°C to +85°C	28–pin SOIC

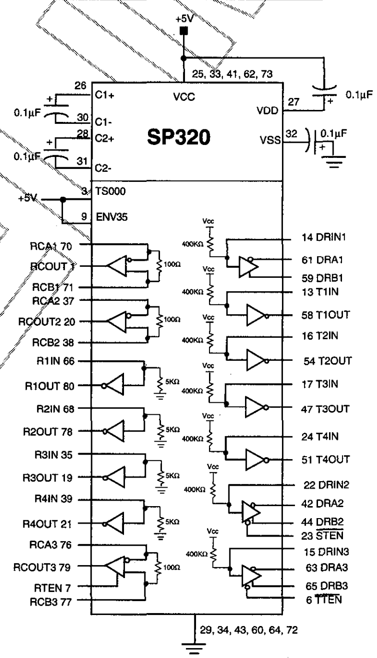
Complete +5V Only V.35 Interface with RS-232 (V.28) Control Lines

- +5V Only
- 3 Drivers 3 Receivers – V.35
- 4 Drivers 4 Receivers – RS-232
- No External V.35 Termination Resistors
- 80 pin QFP Surface Mount Packaging



DESCRIPTION...

The **SP320** is a complete V.35 interface transceiver offering 3 drivers and 3 receivers of V.35, and 4 drivers and 4 receivers of RS-232 (V.28). A **Sipex**-patented charge pump allows +5V only low power operation. RS-232 drivers and receivers are specified to operate at 120Kbps, all V.35 drivers and receivers operate up to 5Mbps.



ABSOLUTE MAXIMUM RATINGS

These are stress ratings only and functional operation of the device at these ratings or any other above those indicated in the operation sections of the specifications below is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

V_{CC} .... +7V
Input Voltages
- Logic .... -0.3V to (V_{CC}+0.5V)
- Drivers .... -0.3V to (V_{CC}+0.5V)
- Receivers .... ±15V

Output Voltages
- Logic .... -0.3V to (V_{CC}+0.5V)
- Drivers .... ±14V
- Receivers .... -0.3V to (V_{CC}+0.5V)

Storage Temperature .... -65°C to +150°C
Power Dissipation 1500mW
Package Derating
- $Ø_{JC}$ .... 16 •C/W
- $Ø_{JA}$ .... 46 •C/W

SPECIFICATIONS

Typical at 25°C and V_{CC} = 5V±5% unless otherwise noted.

PARAMETER	MIN.	TYP.	MAX.	UNITS	CONDITIONS
V.35 DRIVER					
TTL Input Levels					
V_{IL}			0.8	Volts	
V_{IH}	2.0			Volts	
Voltage Outputs					
Differential Outputs	±0.44	±0.55	±0.66	Volts	R_L=100Ω from A to B
Source Impedance	50	100	150	Ohms	
Short Circuit Impedance	135	150	165	Ohms	Measured from A=B to Gnd, V_{OUT}=-2V to +2V
Voltage Output Offset	-0.6		+0.6	Volts	V_{Offset}={[|V_A|+|V_B|]/2}
AC Characteristics					
Transition Time		40		ns	Rise/fall time, 10% to 90%
Transmission Rate			5	Mbps	R_L=100Ω, $V_{DIFF\ OUT}$= .55V±20%
Propagation Delay					
t_{PHL}		200		ns	Measured from 1.5V of V_{IN} to 50% of V_{OUT}
t_{PLH}		200		ns	Measured from 1.5V of V_{IN} to 50% of V_{OUT}
V.35 RECEIVER					
TTL Output Levels					
V_{OL}			0.4	Volts	I_{OUT}=-3.2mA
V_{OH}	2.4			Volts	I_{OUT}=1.0mA
Receiver Inputs					
Differential Input Threshold	-0.2		+0.2	Volts	
Input Impedance	90	100	110	Ohms	
Short Circuit Impedance	135	150	165	Ohms	Measured from A=B to Gnd V_{IN}=-2V to +2V
AC Characteristics					
Transmission Rate			5	Mbps	R_L = 100Ω from A to B
Propagation Delay					
t_{PHL}		200		ns	Measured from 50% of V_{IN} to 1.5V of R_{OUT}
t_{PLH}		200		ns	Measured from 50% of V_{IN} to 1.5V of R_{OUT}

SPECIFICATIONS (CONTINUED)

Typical at 25°C and V_{CC} = 5V±5% unless otherwise noted.

PARAMETER	MIN.	TYP.	MAX.	UNITS	CONDITIONS
RS-232 DRIVER					
TTL Input Levels					
V_{IL}			0.8	Volts	
V_{IH}	2.0			Volts	
Voltage Outputs					
High Level Output	+5.0		+15.0	Volts	R_L=3KΩ to Gnd
Low Level Output	-15.0		-5.0	Volts	R_L=3KΩ to Gnd
Open Circuit Output	-15		+15	Volts	R_L=∞
Short Circuit Current	-100		+100	mA	R_L=Gnd
Power Off Impedance	300			Ohms	V_{CC}=0V; V_{OUT}= ±2V
AC Characteristics					
Slew Rate			30	V/µS	R_L=3KΩ, C_L=50pF; From +3V to -3V or -3V to +3V
Transmission Rate			120	Kbps	R_L=3KΩ, 2500pF to GND, V_{OUT}=±5V
Transition Time			1.56	µS	Rise/fall time, between ±3V R_L=3KΩ, C_L=2500pF
Propagation Delay					
t_{PHL}		2	8	µS	R_L=3KΩ, C_L=2500pF; From 1.5V of T_{IN} to 50% of V_{OUT}
t_{PLH}		2	8	µS	R_L=3KΩ, C_L=2500pF; From 1.5V of T_{IN} to 50% of V_{OUT}
RS-232 RECEIVER					
TTL Output Levels					
V_{OL}			0.4	Volts	
V_{OH}	2.4			Volts	
Receiver Input					
Input Voltage Range	-15		+15	Volts	
High Threshold		1.7	3.0	Volts	
Low Threshold	0.8	1.2		Volts	
Hysteresis	0.2	0.5	1	Volts	V_{CC}=5V; T_A=+25°C
Receiver Input Circuit Bias			+2.0	Volts	
Input Impedance	3	5	7	KOhms	V_{IN}=±15V
AC Characteristics					
Transmission Rate			120	Kbps	
Propagation Delay					
t_{PHL}		100	1	µS	From 50% of R_{IN} to 1.5V of R_{OUT}
t_{PLH}		100	1	µS	From 50% of R_{IN} to 1.5V of R_{OUT}
POWER REQUIREMENTS					
No Load V_{CC} Supply Current		35		mA	No load; V_{CC}=5.0V; T_A=25°C
Full Load V_{CC} Supply Current		60		mA	RS-232 drivers R_L=3KΩ to Gnd; DC Input V.35 drivers R_L=100Ω from A to B; DC Input
Shutdown Current		1.5		mA	T5000 = ENV35 = 0V

THEORY OF OPERATION...

The **SP320** is a single chip +5V only serial transceiver that supports all the signals necessary to implement a full V.35 interface. Three V.35 drivers and three V.35 receivers make up the clock and data signals. Four RS-232 (V.28) drivers and four RS-232 (V.28) receivers are used for control line signals for the interface.

V.35 Drivers...

The V.35 drivers are +5V only, low power voltage output transmitters. The drivers do not require any external resistor networks, and will meet the following requirements:

1. Source impedance in the range of 50Ω to 150Ω.

2. Resistance between short-circuited terminals and ground is 150Ω ±15Ω.

3. When terminated with a 100Ω resistive load the terminal to terminal voltage will be 0.55 volts ±20% so that the A terminal is positive to the B terminal when binary 0 is transmitted, and the conditions are reversed to transmit binary 1.

4. The arithmetic mean of the voltage of the A terminal with respect to ground, and the B terminal with respect to ground will not exceed 0.6 volts when terminated as in 3.

The V.35 drivers can operate at data rates as high as 5Mbps. The driver outputs are protected against short-circuits between the A and B outputs and short circuits to ground.

Two of the V.35 drivers, DRIN2 and DRIN3 are equipped with enable control lines. When the enable pins are high the driver outputs are disabled, the output impedance of a disabled driver will nominally be 300Ω. When the enable pins are low, the drivers are active.

V.35 Receivers...

The V.35 receivers are +5V only, low power differential receivers which meet the following requirements:

1. Input impedance in the range of 100Ω ±10Ω.

2. Resistance to ground of 150Ω ±15Ω, measured from short-circuited terminals.

All of the V.35 receivers can operate at data rates as high as 5Mbps. The sensitivity of the V.35 receiver inputs is ±200mV which applies over a common mode range of +12V to -7V.

RS-232 (V.28) Drivers

The RS-232 drivers are inverting transmitters, which accept either TTL or CMOS inputs and output the RS-232 signals with an inverted sense relative to the input logic levels. Typically, the RS-232 output voltage swing is ±9V with no load, and ±5V minimum with full load. The transmitter outputs are protected against infinite short-circuits to ground without degradation in reliability.

In the power off state, the output impedance of the RS-232 drivers will be greater than 300Ω over a ±2V range. Should the input of a driver be left open, an internal 400KΩ pullup resistor to V_{CC} forces the input high, thus committing the output to a low state. The slew rate of the transmitter output is internally limited to a maximum of 30V/µS in order to meet the EIA standards. The RS-232 drivers are rated for 120Kbps data rates.

RS-232 (V.28) Receivers...

The RS-232 receivers convert RS-232 input signals to inverted TTL signals. Each of the four receivers features 500mV of hysteresis margin to minimize the effects of noisy transmission lines. The inputs also have a 5KΩ resistor to ground; in an open circuit situation the input of the receiver will be forced low, committing the output to a logic high state. The input resistance will maintain 3KΩ-7KΩ over a ±15V range. The maximum operating voltage range for the receiver is ±30V, under these conditions the input current to the receiver must be limited to less than 100mA. The RS-232 receivers can operate up to 120Kbps.

CHARGE PUMP...

The charge pump is a **Sipex**-patented design (5,306,954) and uses a unique approach compared to older less-efficient designs. The charge pump still requires four external capacitors, but uses a four-phase voltage shifting technique to attain symmetrical 10V power supplies. The capacitors can be as low as 0.1µF with a 16 volt rating. Polarized or non-polarized capacitors can be used.

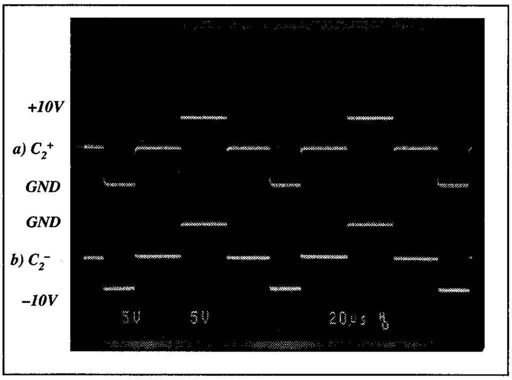


Figure 1. Charge Pump Waveforms

Figure 1a shows the waveform found on the positive side of capacitor C2, and *Figure 1b* shows the negative side of capacitor C2. There is a free-running oscillator that controls the four phases of the voltage shifting. A description of each phase follows.

Phase 1

-Vss charge storage- During this phase of the clock cycle, the positive side of capactors C1 and C2 are initially charged to +5V. C1+ is then switched to ground and charge in C1- is transferred to C2-. Since C2+ is connected to +5V, the voltage potential across capacitor C2 is now 10V.

Phase 2

-Vss transfer- Phase two of the clock connects the negative terminal of C2 to the Vss storage capacitor and the positive terminal of C2 to ground, and transfers the generated -10V to C3. Simultaneously, the positive side of capacitor C1 is switched to +5V and the negative side is connected to ground.

Phase 3

-Vdd charge storage- The third phase of the clock is identical to the first phase- the transferred charge in C1 produces -5V in the negative terminal of C1, which is applied to the negative side of capacitor C2. Since C2+ is at +5V, the voltage potential across C2 is 10V.

Phase 4

-Vdd transfer- The fourth phase of the clock connects the negative terminal of C2 to ground and transfers the generated 10V across C2 to C4, the Vdd storage capacitor. Again, simultaneously with this, the positive side of capacitor C1 is switched to +5V and the negative side is connected to ground, and the cycle begins again.

Since both V+ and V- are separately generated from Vcc in a no load condition, V+and V- will be symmetrical. Older charge pump approaches that generate V- from V+ will show a decrease in the magnitude of V- compared to V+ due to the inherent inefficiencies in the design.

The clock rate for the charge pump typically operates at 15KHZ. The external capacitors must be 0.1µF with a 16V breakdown rating.

Shutdown Mode

The **SP320** can be put into a low power shutdown mode by bringing both TS000 (pin 3) and ENV35 (pin 9) low. In shutdown mode, the SP320 will draw less than 2mA of supply current. For normal operation, both pins should be connected to +5V.

External Power Supplies

For applications that do not require +5V only, external supplies can be applied at the V+ and V- pins. The value of the external supply voltages must be no greater than ±10V. The current drain from the ±10V supplies is used for the RS-232 drivers. For the RS-232 driver the current requirement will be 3.5mA per driver. It is critical the external power supplies provide a power supply sequence of: +10V, +5V and then -10V.

Applications Information

The **SP320** is a single chip device that can implement a complete V.35 interface. Three (3) V.35 drivers and three (3) V.35 receivers are used for clock and data signals and four (4) RS-232 (V.28) drivers and four (4) RS-232 (V.28) receivers can be used for the control signals of the interface. The following examples show the SP320 configured in either a DTE or DCE application.

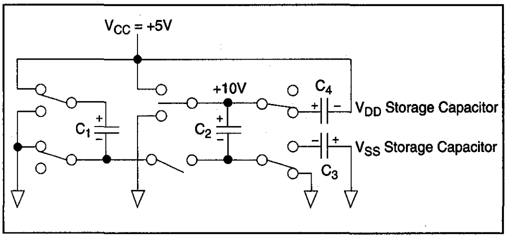


Figure 2. Charge Pump Phase 1

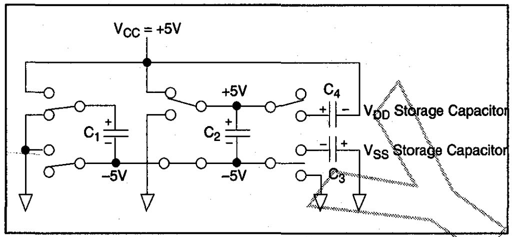


Figure 3. Charge Pump Phase 2

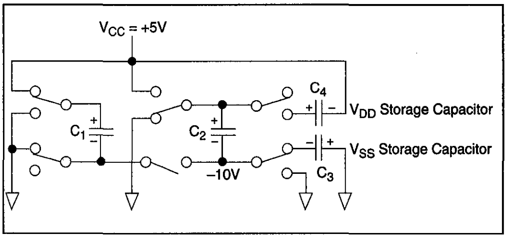


Figure 4. Charge Pump Phase 3

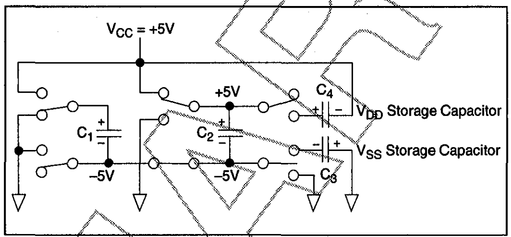


Figure 5. Charge Pump Phase 4

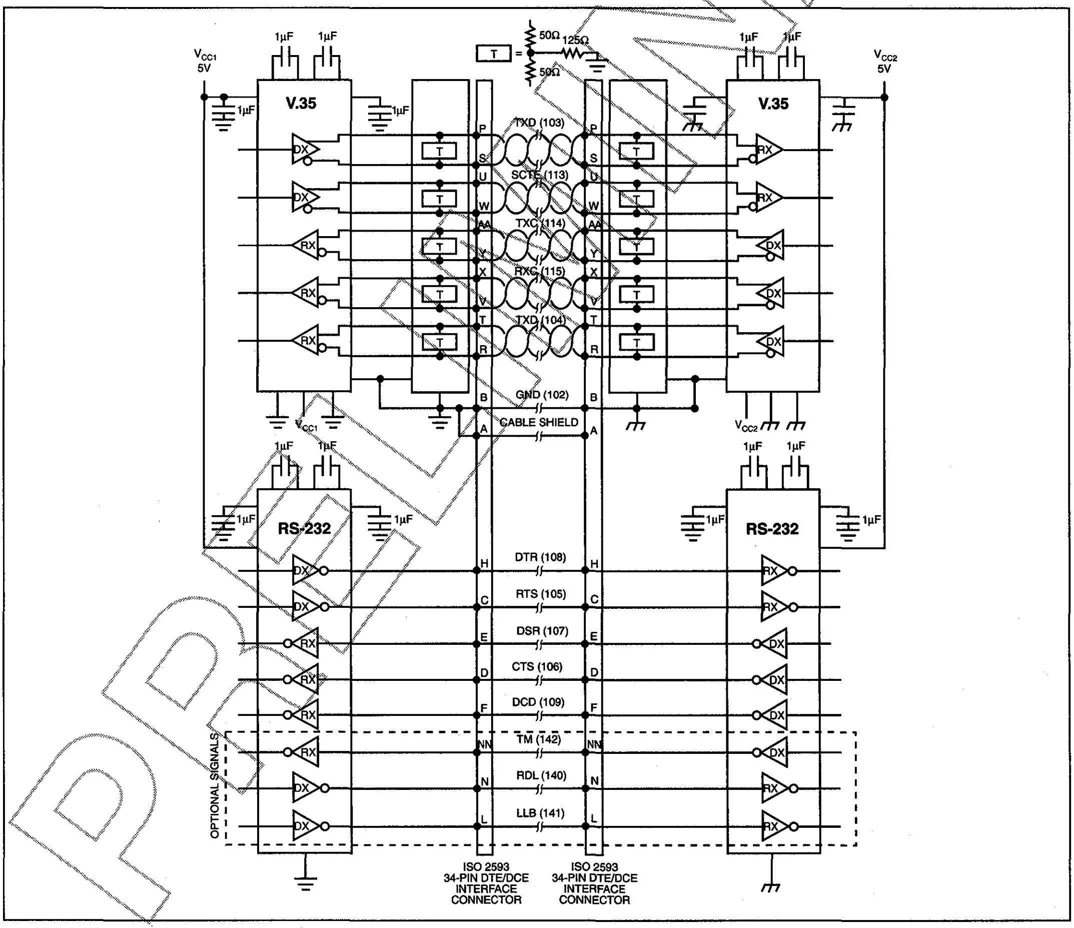


Figure 6. A Competitor's Typical V.35 Solution Using Six Components.

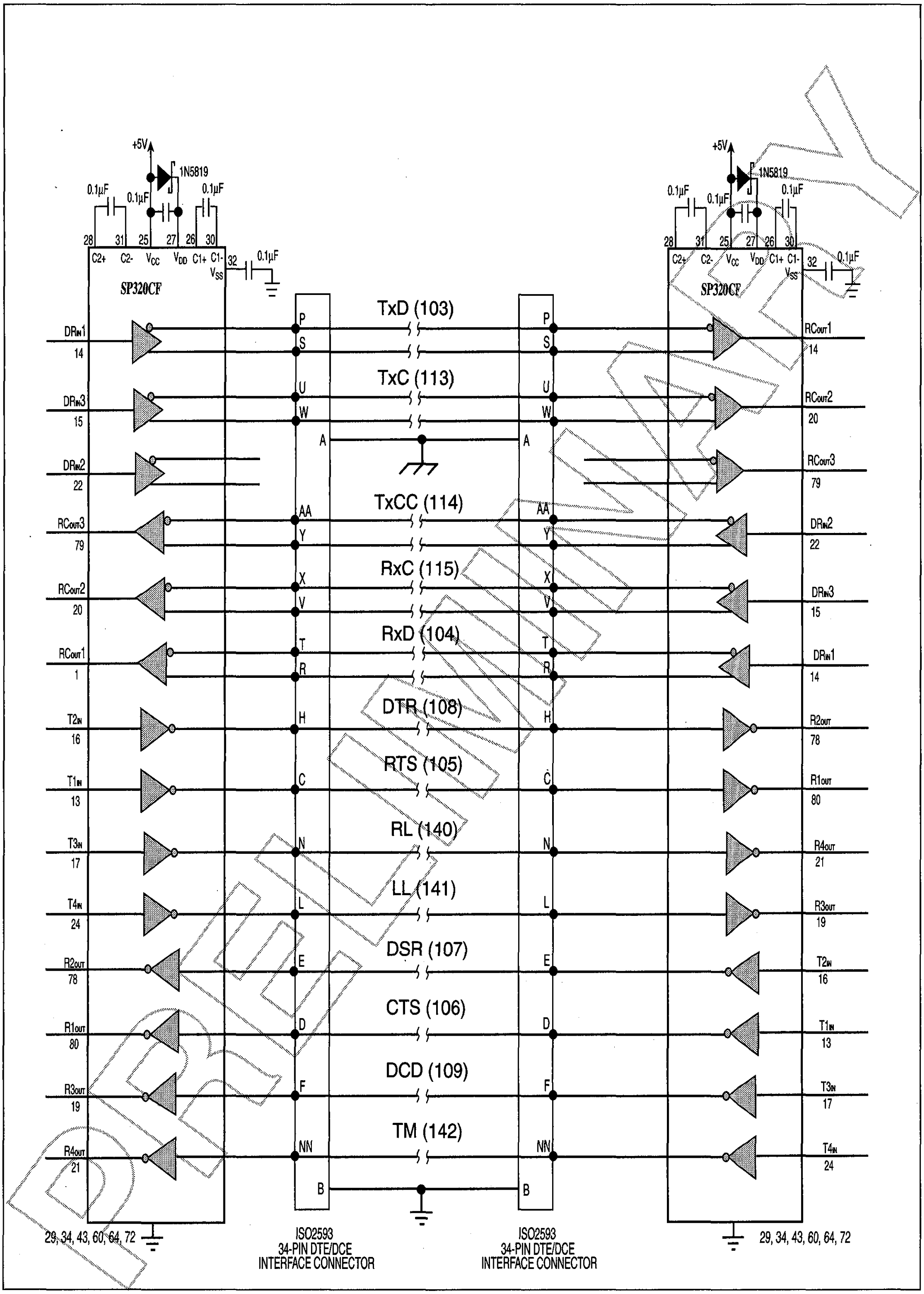
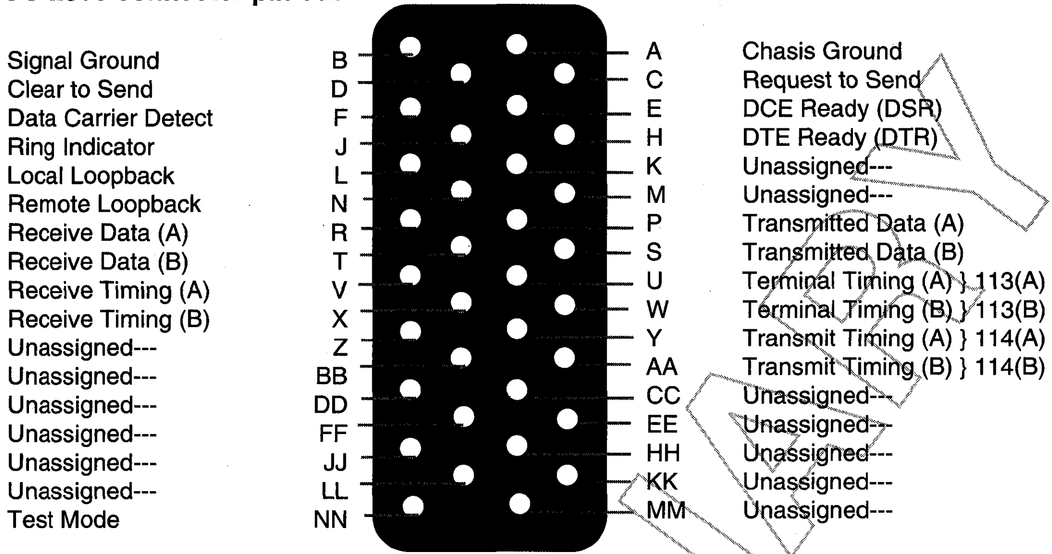
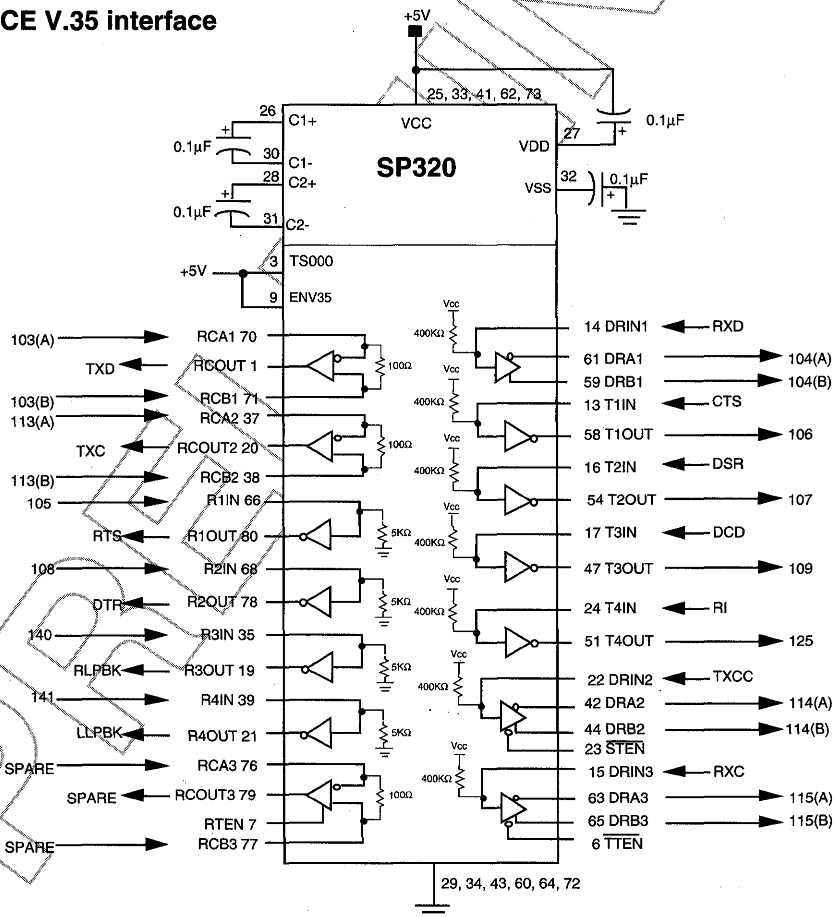


Figure 7. Typical DTE-DCE V.35 Connection with the SP320

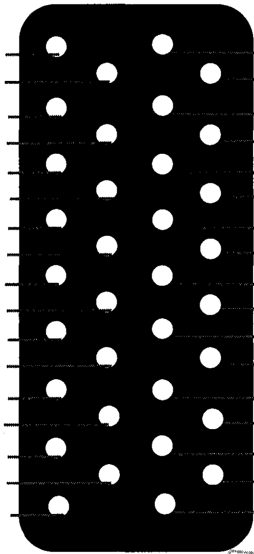
ISO-2593 connector pin out



Typical DCE V.35 interface

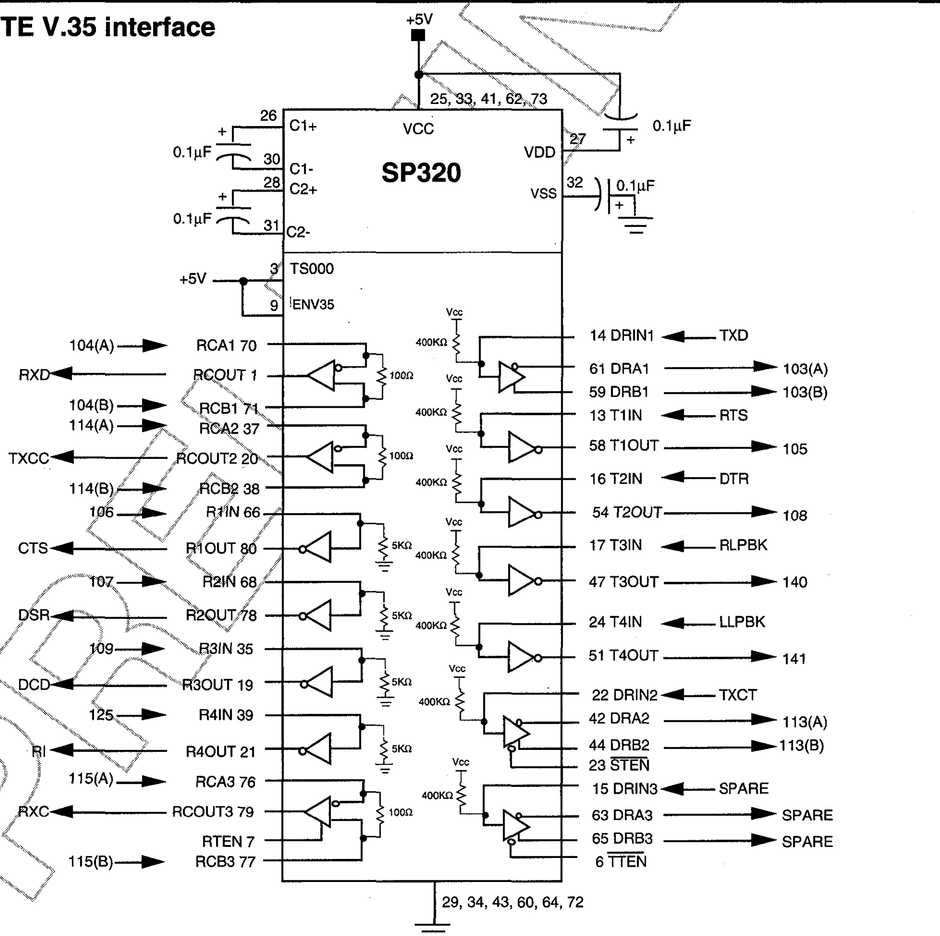


ISO-2593 connector pin out

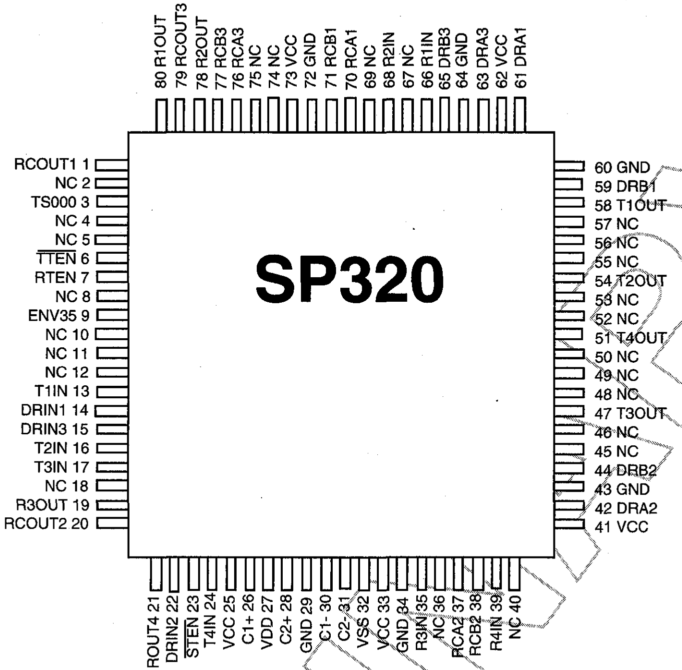


Signal Ground	B	A	Chasis Ground
Clear to Send	D	C	Request to Send
Data Carrier Detect	F	E	DCE Ready (DSR)
Ring Indicator	J	H	DTE Ready (DTR)
Local Loopback	L	K	Unassigned---
Remote Loopback	N	M	Unassigned---
Receive Data (A)	R	P	Transmitted Data (A)
Receive Data (B)	T	S	Transmitted Data (B)
Receive Timing (A)	V	U	Terminal Timing (A) } 113(A)
Receive Timing (B)	X	W	Terminal Timing (B) } 113(B)
Unassigned---	Z	Y	Transmit Timing (A) } 114(A)
Unassigned---	BB	AA	Transmit Timing (B) } 114(B)
Unassigned---	DD	CC	Unassigned---
Unassigned---	FF	EE	Unassigned---
Unassigned---	JJ	HH	Unassigned---
Unassigned---	LL	KK	Unassigned---
Test Mode	NN	MM	Unassigned---

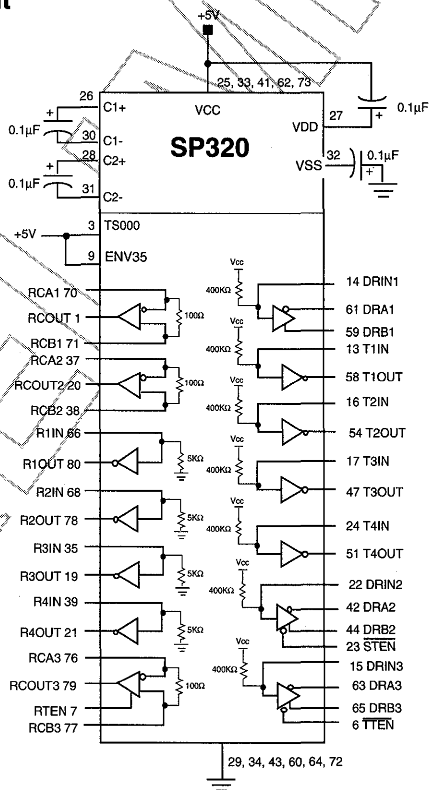
Typical DTE V.35 interface



Pin configuration



Typical application circuit



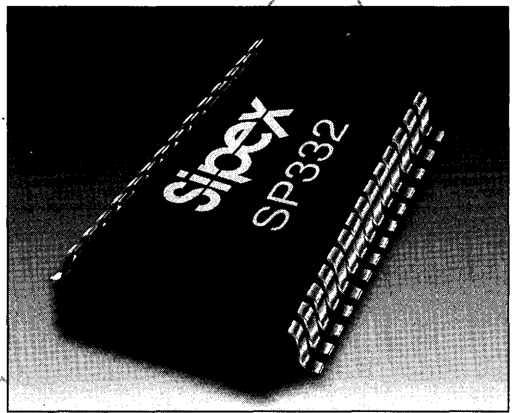
ORDERING INFORMATION

Model	Temperature Range	Package Types
SP320CF	0˚C to +70˚C	80-pin QFP

THIS PAGE LEFT INTENTIONALLY BLANK

RS-232/RS-485 Multi-Mode Serial Transceiver

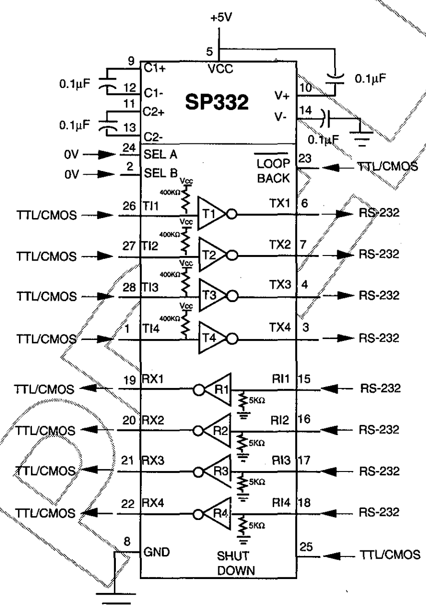
- +5V Only
- 4 Drivers, 4 Receivers RS-232
- 2 Drivers, 2 Receivers RS-485
- Loop Back Function for Self Test
- 28 Pin SOIC Packaging



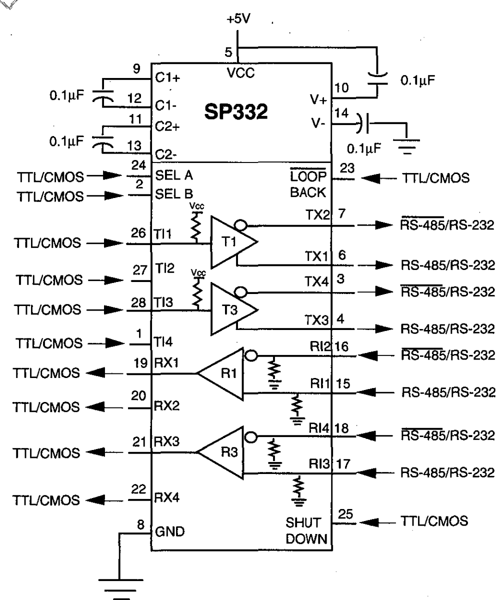
DESCRIPTION...

The **SP332** is a monolithic device that contains both RS-232 and RS-485 line drivers and receivers. The configuration of the **SP332** can be changed at any time by changing the logic state of two control input pins. The device also includes a loop back function which internally connects driver outputs to receiver inputs for a chip self test. A **Sipex**-patented charge pump (5,306,954) allows +5V only operation.

RS-232 Mode



Full Duplex RS-485



ABSOLUTE MAXIMUM RATINGS

These are stress ratings only and functional operation of the device at these ratings or any other above those indicated in the operation sections of the specifications below is not implied. Exposure to absolute maximum *rating conditions for extended periods of time may affect reliability.*

V_{CC}..........+12V
Input Voltages
- Logic..........-0.5V to (V_{CC}+0.5V)
- Drivers..........-0.5V to (V_{CC}+0.5V)
- Receivers..........±30V @ ≤100mA

Driver Outputs..........±15V
Storage Temperature..........-65˚C to +150˚C
Power Dissipation..........1000mW

SPECIFICATIONS

T_{MIN} to T_{MAX} and V_{CC} = 5V±5% unless otherwise noted.

PARAMETER	MIN.	TYP.	MAX.	UNITS	CONDITIONS
RS-485 DRIVER					
DC Characteristics					
Differential Output Voltage	GND		V_{CC}	Volts	Unloaded; R=∞; *see figure 1*
Differential Output Voltage	2.0		5.0	Volts	With Load; R=50Ω (RS-422); *see figure 1*
Differential Output Voltage	1.5		5.0	Volts	With Load; R=27Ω (RS-485); *see figure 1*
Change in Magnitude of Driver Differential Output Voltage for Complementary States			0.2	Volts	R=27Ω or R=50Ω; *see figure 1*
Driver Common-Mode Output Voltage			3	Volts	R=27Ω or R=50Ω; *see figure 1*
Input High Voltage	2.0			Volts	Applies to transmitter inputs, SEL A, SEL B, SD, $\overline{LB}$
Input Low Voltage			0.8	Volts	Applies to SEL A, SEL B, SD, $\overline{LB}$
Input Current			±10	µA	Applies to:
Pull-Up Current		1.5		µA	transmitter inputs, $\overline{LB}$
Pull-Down Current		3.0		µA	SEL A, SEL B, SD,
Driver Short-Circuit Current					
V_{OUT}= HIGH	35		250	mA	-7V≤V_O≤10V
V_{OUT}= LOW	35		250	mA	-7V≤V_O≤10V
AC Characteristics					
Driver Data Rate			10	Mbps	
Driver Input to Output	20	60		ns	t_{PLH}; R_{DIFF}=54Ω, C_{L1}=C_{L2}=100pF; *see figures 3 and 6*
Driver Input to Output	20	60		ns	t_{PHL}; R_{DIFF}=54Ω, C_{L1}=C_{L2}=100pF; *see figures 3 and 6*
Driver Skew		5	10	ns	From output to output; *see figures 3 and 6*
Driver Rise or Fall Time	3	15	40	ns	From 10% to 90%; R_{DIFF}=54Ω, C_{L1}=C_{L2}=100pF; *see figures 3 and 6*
RS-485 RECEIVER					
DC Characteristics					
Differential Input Threshold	-0.2		+0.2	Volts	-7V≤V_{CM}≤12V
Input Hysteresis		70		mV	V_{CM}=0V
Output Voltage High	3.5			Volts	I_O=-4mA, V_{ID}=+200mV
Output Voltage Low			0.4	Volts	I_O=+4mA, V_{ID}=-200mV
Input Resistance	12	15		kΩ	-7V≤V_{CM}≤12V
Input Current (A, B); V_{IN}= 12V			+1.0	mA	V_{IN}= 12V, A is the non-inverting receiver input. B is the inverting receiver input
Input Current (A, B); V_{IN}= -7V			-0.8	mA	V_{IN}= -7V
Short Circuit Current			85	mA	0V≤V_{CM}≤V_{CC}

SPECIFICATIONS (CONTINUED)

T_{MIN} to T_{MAX} and V_{CC} = 5V±5% unless otherwise noted.

PARAMETER	MIN.	TYP.	MAX.	UNITS	CONDITIONS
AC Characteristics					
Receiver Data Rate			10	Mbps	
Receiver Input to Output		90		ns	t_{PLH}; R_{DIFF}=54Ω, C_{L1}=C_{L2}=100pF; *Figures 3 and 8*
Receiver Input to Output		90		ns	t_{PLH}; R_{DIFF}=54Ω, C_{L1}=C_{L2}=100pF; *Figures 3 and 7*
Diff. Receiver Skew $\vert t_{PLH}$-$t_{PHL}\vert$		13		ns	R_{DIFF}=54Ω, C_{L1}=C_{L2}=100pF; *Figures 3 and 7*
RS-232 DRIVER					
DC Characteristics					
TTL Input Levels					
V_{IL}			0.8	Volts	Applies to transmitter inputs, SEL A, SEL B, SD, LB
V_{IH}	2.0			Volts	Applies to transmitter inputs, SEL A, SEL B, SD, LB
Voltage Outputs					
High Level Output	+5.0		+15.0	Volts	R_L=3KΩ to Gnd
Low Level Output	-15.0		-5.0	Volts	R_L=3KΩ to Gnd
Open Circuit Output			±15	Volts	R_L=∞
Short Circuit Current			±100	mA	V_{OUT} = 0V
Power Off Impedance	300			Ohms	V_{CC}=0V; V_{OUT}= ±2V
AC Characteristics					
Transmission Rate			120	Kbps	
Transition Time			1.56	µS	Rise/fall time, +3V to -3V; -3V to +3V R_L=3KΩ, C_L=2500pF
Propagation Delay					
t_{PHL}		2		µS	R_L=3KΩ, C_L=2500pF; From 1.5V of T_{IN} to 50% of V_{OUT}
t_{PLH}		1.5		µS	R_L=3KΩ, C_L=2500pF; From 1.5V of T_{IN} to 50% of V_{OUT}
Slew Rate		10	30	V/µS	R_L=3KΩ, C_L=50pF; From +3V to -3V or -3V to +3V
RS-232 RECEIVER					
TTL Output Levels					
V_{OL}			0.4	Volts	I_{SINK} = 4mA
V_{OH}	3.5				I_{SOURCE} = -4mA
Receiver Input					
High Threshold		1.7	3.0	Volts	
Low Threshold	0.8	1.2		Volts	
Input Voltage Range	-30		+30	Volts	±30V input @I_{IN}<100mA
Input Impedance	3	5	7	KOhms	V_{IN}=±15V
Hysteresis	0.2	0.5	1.0	Volts	V_{CC}=+5V
AC Characteristics					
Transmission Rate			120	Kbps	
Transition Time		50		ns	Rise/fall time 10% to 90%
Propagation Delay					
t_{PHL}		100		ns	From 50% of V_{IN} to 1.5V of R_{OUT}
t_{PLH}		100		ns	From 50% of V_{IN} to 1.5V of R_{OUT}
POWER REQUIREMENTS					
No Load Supply Current		19	25	mA	No load; V_{CC}=5.0V; T_A=25°C
Full Load Supply Current		90	120	mA	RS-232 drivers R_L=3KΩ to Gnd; DC Input RS-485 drivers R_L=54Ω from A to B; DC Input
Shutdown Supply Current		20		µA	T_A=25°C, V_{CC}=5.0V

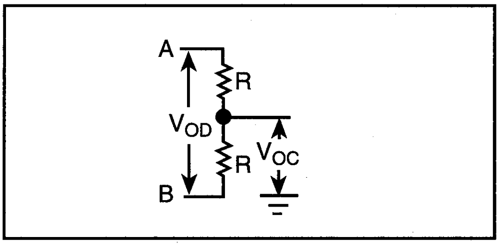


Figure 1. RS-485 Driver DC Test Load Circuit

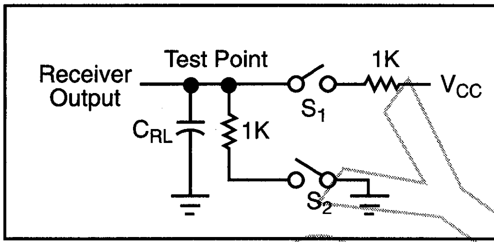


Figure 2. Receiver Timing Test Load Circuit

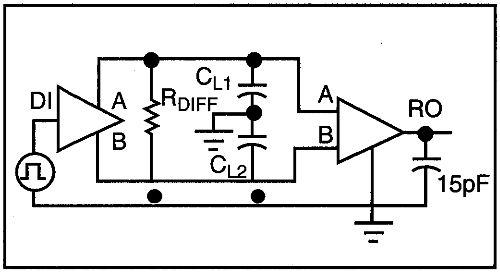


Figure 3. RS-485 Driver/Receiver Timing Test Circuit

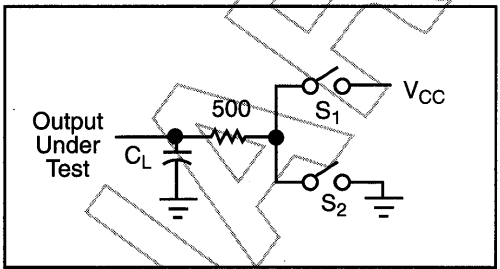


Figure 4. RS-485 Driver Timing Test Load #2 Circuit

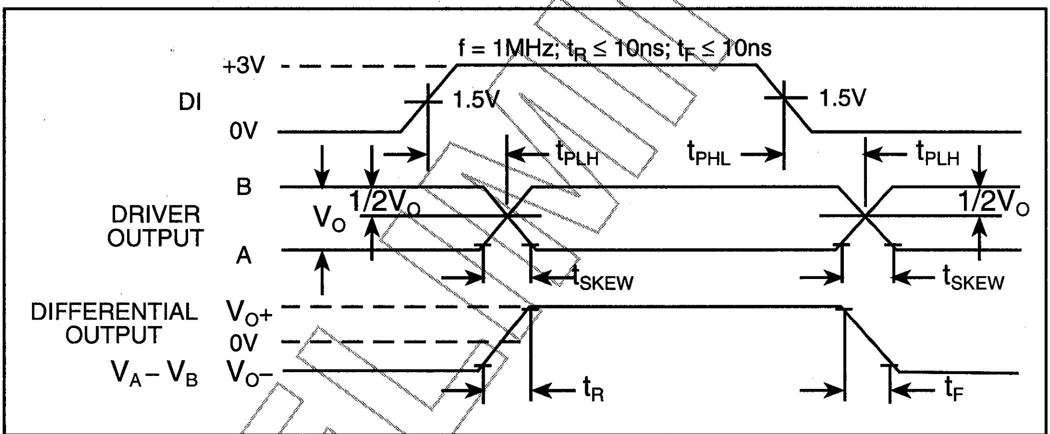


Figure 6. RS-485 Driver Propagation Delays

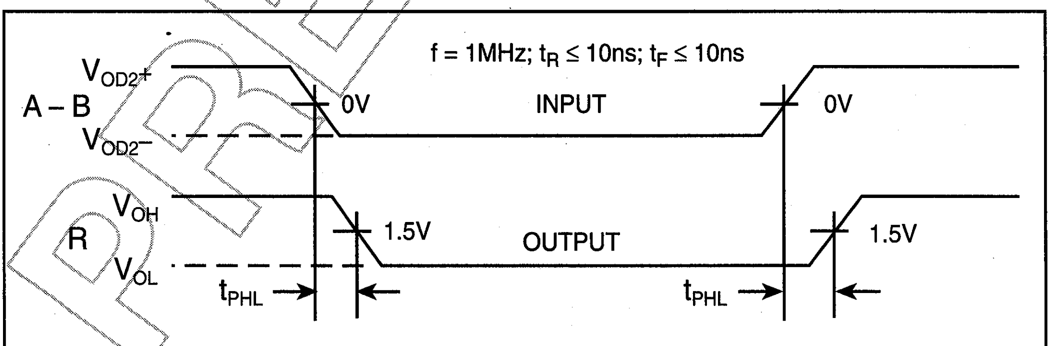


Figure 7. RS-485 Receiver Propagation Delays

THEORY OF OPERATION...

The **SP332** is a single chip device that can be configured via software for either RS-232, RS-485 or both interface modes at any time. The **SP332** is made up of three basic circuit elements, single-ended drivers and receivers, differential drivers and receivers and charge pump.

DIFFERENTIAL DRIVER/RECEIVER...

RS-485, RS-422 Drivers...

The differential drivers and receivers comply with the RS-485 and RS-422 standards. The driver circuits are able to drive a minimum of 1.5V when terminated with a 54Ω resistor across the two outputs. The typical propagation delay from the driver input to output is 60nS. The driver outputs are current limited to less than 250mA, and can tolerate short circuits to ground, or to any voltage within a +10V to -7V range with no damage.

RS-485, RS-422 Receivers...

The differential receivers of the **SP332** comply with the RS-485, RS-422 and V.11 standards. The input to the receiver is equipped with a common mode range of +12V to -7V. The input threshold over this range is a minimum of ±200mV. The differential receivers can receive data up to 10Mbps. The typical propagation delay from the receiver input to output is 90nS.

SINGLE ENDED DRIVER/RECEIVER...

RS-232 (V.28) Drivers...

The single-ended drivers and receivers comply the with the RS-232E and V.28 standards. The drivers are inverting transmitters which accept either TTL or CMOS inputs and output the RS-232 signals with an inverted sense relative to the input logic levels. Typically, the RS-232 driver output voltage swing is ±9V with no load and is guaranteed to be greater than ±5V under full load. The drivers rely on the V+ and V- voltages generated by the on-chip charge pump to maintain proper RS-232 output levels. With worst case load conditions of 3KΩ and 2500pF, the four RS-232 drivers can still maintain ±5V output levels. The drivers can operate up to 120Kbps; the propagation delay from input to output is typically 2µS.

RS-232 (V.28) Receivers...

The RS-232 receivers convert RS-232 input signals to inverted TTL signals. Each of the four receivers features 500mV of hysteresis margin to minimize the affects of noisy tranmission lines. The inputs also have a 5KΩ resistor to ground, in an open circuit situation the input of the receiver will be forced low, committing the output to a logic high state. The input resistance will maintain 3KΩ-7KΩ over a ±15V range. The maximum operating voltage range for the receiver is ±30V, under these conditions the input current to the receiver must be limited to less than 100mA. Due to the on-chip ESD protection circuitry, the receiver inputs will be clamped to ±15V levels. The RS-232 receivers can operate up to 120Kbps.

CHARGE PUMP...

The charge pump is a **Sipex**-patented design (5,306,954) and uses a unique approach compared to older less-efficient designs. The charge pump still requires four external capacitors, but uses a four-phase voltage shifting technique to attain symmetrical 10V power supplies. *Figure 8a* shows the waveform found on the positive side of capacitor C2, and *Figure 8b* shows the negative side of capacitor C2. There is a free-running oscillator that controls the four phases of the voltage shifting. A description of each phase follows.

Phase 1

-Vss charge storage- During this phase of the clock cycle, the positive side of capacitors C1 and C2 are initially charged to +5V. C1+ is then switched to ground and charge in C1- is transferred to C2-. Since C2+ is connected to +5V, the voltage potential across capacitor C2 is now 10V.

Phase 2

-Vss transfer- Phase two of the clock connects the negative terminal of C2 to the Vss storage capacitor and the positive terminal of C2 to ground, and transfers the generated -10V to C3. Simultaneously, the positive side of capacitor C1 is switched to +5V and the negative side is connected to ground.

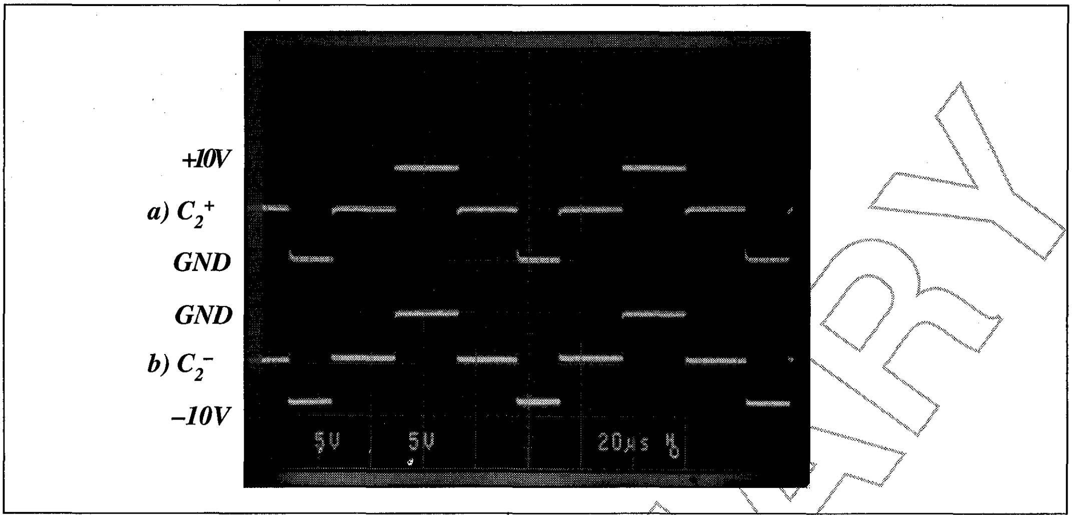


Figure 8. Charge Pump Waveforms

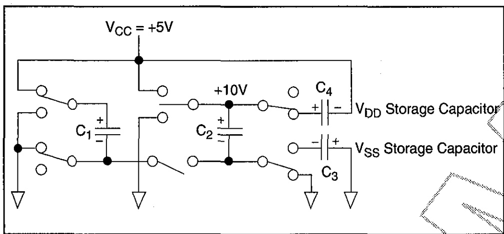


Figure 9. Charge Pump Phase 1

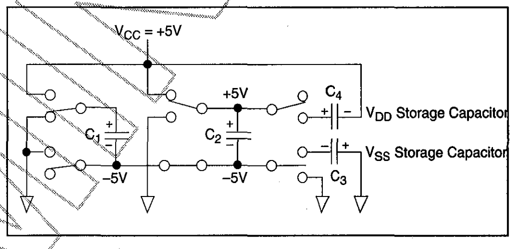


Figure 10. Charge Pump Phase 2

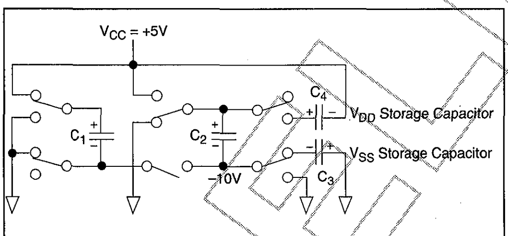


Figure 11. Charge Pump Phase 3

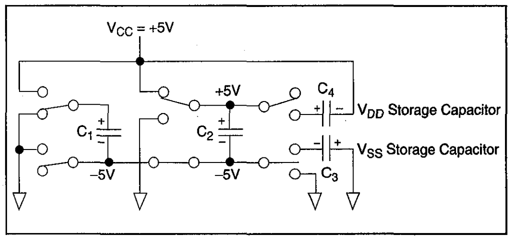


Figure 12. Charge Pump Phase 4

Phase 3

-Vdd charge storage- The third phase of the clock is identical to the first phase- the transferred charge in C1 produces -5V in the negative terminal of C1, which is applied to the negative side of capacitor C2. Since C2+ is at +5V, the voltage potential across C2 is 10V.

Phase 4

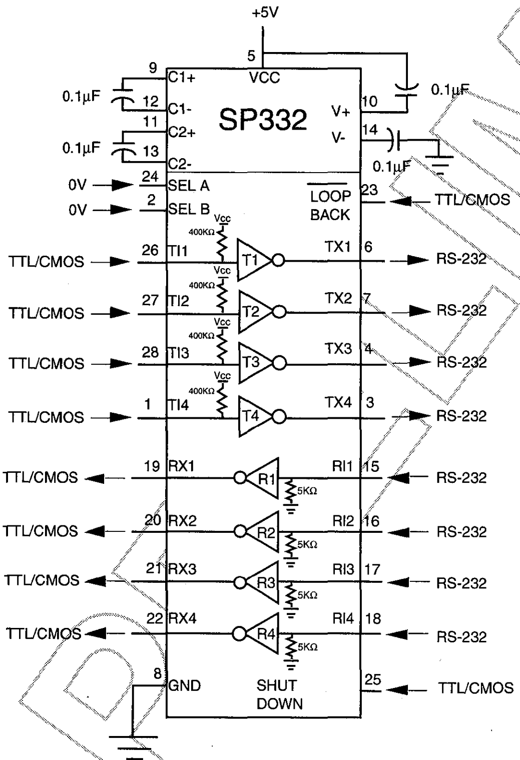
-Vdd transfer- The fourth phase of the clock connects the negative terminal of C2 to ground and transfers the generated 10V across C2 to C4, the Vdd storage capacitor. Simultaneously with this, the positive side of capacitor C1 is switched to +5V and the negative side is connected to ground, and the cycle begins again.

Since both V+ and V- are separately generated from Vcc in a no load condition, V+ and V- will be symmetrical. Older charge pump approaches that generate V- from V+ will show a decrease in the magnitude of V- compared to V+ due to the inherent inefficiencies in the design.

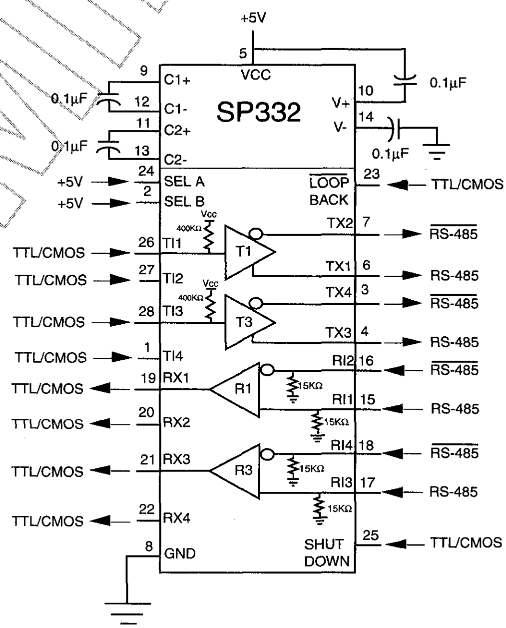
The clock rate for the charge pump typically operates at 15KHZ. The external capacitors must be 0.1μF with a 16V breakdown rating.

SP332 TYPICAL OPERATING CIRCUIT

RS-232 Mode

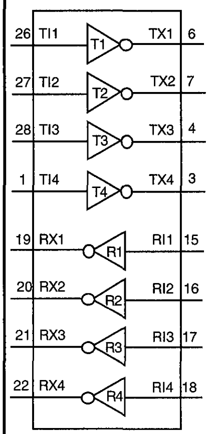


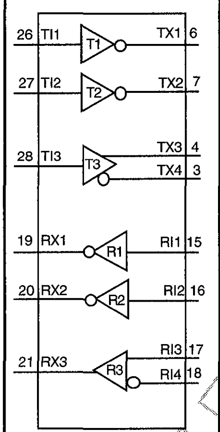
RS-485 Mode

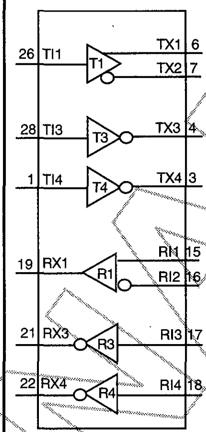


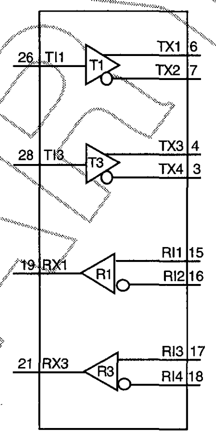
SP332 CONTROL LOGIC CONFIGURATION

SEL A	0	0	1	1
SEL B	0	1	0	1
LOOPBACK	1	1	1	1
SHUTDOWN	0	0	0	0

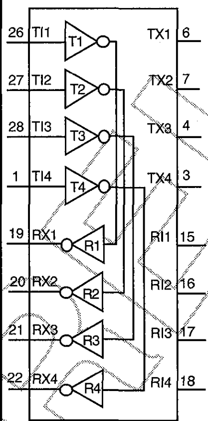


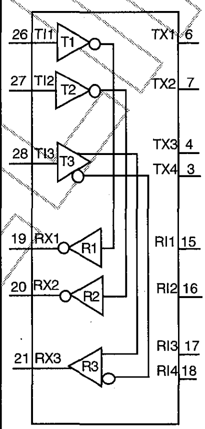


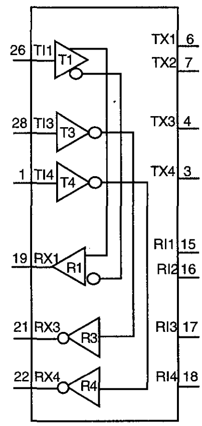


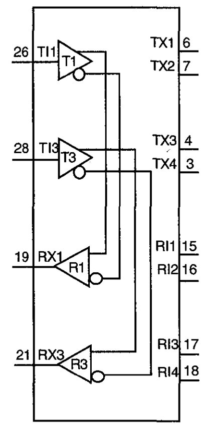


SEL A	0	0	1	1
SEL B	0	1	0	1
LOOPBACK	0	0	0	0
SHUTDOWN	0	0	0	0

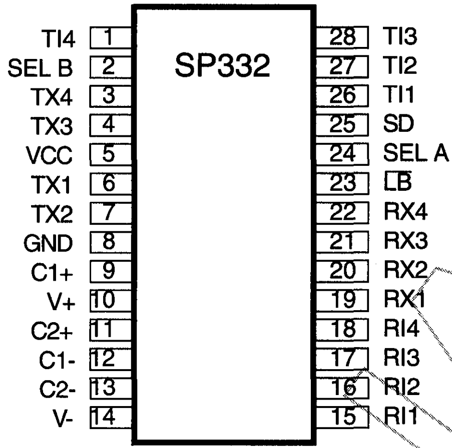








Receiver Inputs are inactive in Loopback Mode ($\overline{\text{LOOPBACK}}$ = 0)
Driver Outputs are Tri-Stated in Loopback Mode ($\overline{\text{LOOPBACK}}$ = 0)
Unused Outputs are Tri-Stated

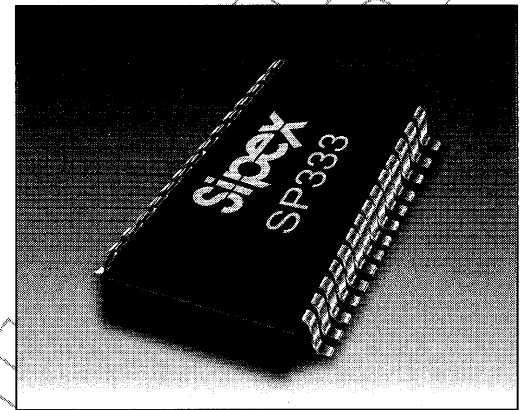

SP332
TI4 1
SEL B 2
TX4 3
TX3 4
VCC 5
TX1 6
TX2 7
GND 8
C1+ 9
V+ 10
C2+ 11
C1- 12
C2- 13
V- 14
28 TI3
27 TI2
26 TI1
25 SD
24 SEL A
23 LB
22 RX4
21 RX3
20 RX2
19 RX1
18 RI4
17 RI3
16 RI2
15 RI1

ORDERING INFORMATION

Model	Temperature Range	Package Types
SP332CT	0˚C to +70˚C	28-Pin SOIC
SP332ET	-40˚C to +85˚C	28-Pin SOIC

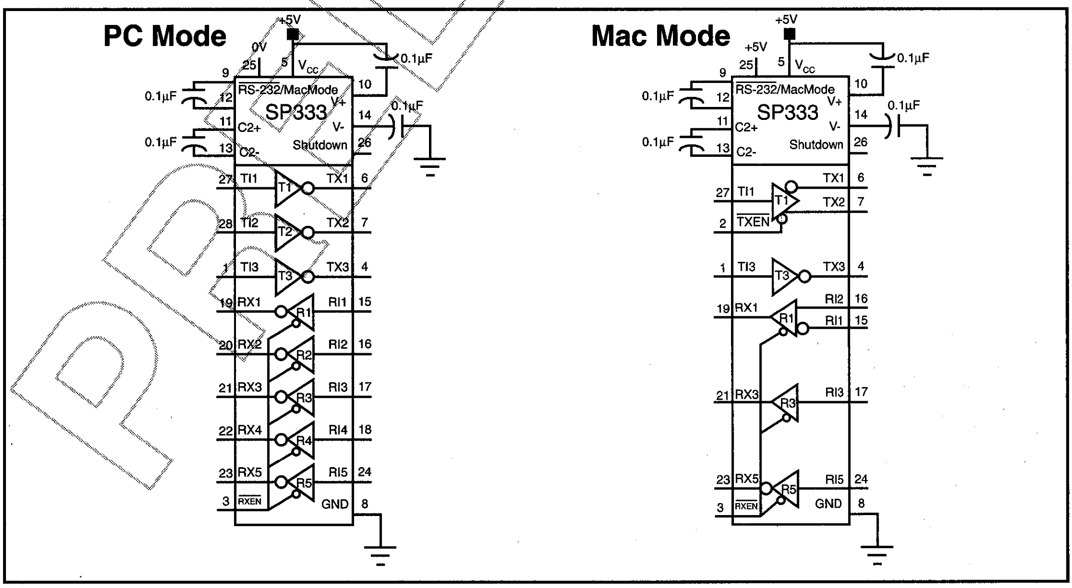
+5V Only RS-232/AppleTalk™ Programmable Transceiver

- +5V Only
- Low Power Shutdown
- 28-Pin SOIC Packaging
- 3 Drivers, 5 Receivers – RS-232
- Complete AppleTalk™ Interface
- High Data Rates
  10Mbps Differential Transceivers
  400kbps Single-Ended Transceivers



DESCRIPTION...

The **SP333** is a monolithic device that supports both Macintosh™ and PC serial interfaces. RS-232 mode offers three (3) RS-232 drivers and five (5) RS-232 receivers. Mac Mode includes a differential driver and a single-ended inverting driver. Receivers in Mac mode include one differential receiver, one non-inverting single-ended receiver and one inverting single-ended receiver. An on-chip charge pump allows +5V only operation, and a low power shutdown mode makes the **SP333** ideal for battery powered applications. The interface mode can be changed at any time by a mode select pin.



ABSOLUTE MAXIMUM RATINGS

These are stress ratings only and functional operation of the device at these ratings or any other above those indicated in the operation sections of the specifications below is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

V_{CC} .... +12V
Input Voltages
- Logic .... -0.3V to (V_{CC}+0.5V)
- Drivers .... -0.3V to (V_{CC}+0.5V)
- Receivers .... ±15V

Driver Outputs .... ±14V
Storage Temperature .... -65°C to +150°C
Power Dissipation 1000mW

SPECIFICATIONS

T_{MIN} to T_{MAX} and V_{CC} = 5V±5% unless otherwise noted.

PARAMETER	MIN.	TYP.	MAX.	UNITS	CONDITIONS
MAC Mode (pin 25 = +5V)					
Differential Driver					
High Level Output Voltage			+3.6	Volts	I_{OH} = 8mA
Low Level Output Voltage	–3.6			Volts	I_{OH} = –8mA
Differential Output Load		±5V		Volts	R_L = 450Ω (between TX outputs)
Differential Output No Load			±10	Volts	R_L = ∞
Driver Short Circuit Current		±40		mA	–7V≤V_O≤+7V; $V_{IN\ LOW}$≤0.8V or $V_{IN\ HIGH}$≥2.0V
Output Leakage Current			±10	µA	–7V≤V_O≤+7V; $\overline{TxEN}$ = V_{CC}
Input High Voltage	2.0			Volts	Applies to differential driver inputs
Input Low Voltage			0.8	Volts	Applies to differential driver inputs
Input Current			±10	µA	
Transition Time		30		ns	R_L = 450Ω, C_L = 50pF; Rise/Fall 10% – 90%
Propagation Delay					
t_{PHL}		100		ns	R_L = 450Ω, C_L = 50pF
t_{PLH}		100		ns	R_L = 450Ω, C_L = 50pF
Data Rate			10	Mbps	R_L = 450Ω, C_L = 50pF
Single-Ended Inverting Driver					
High Level Output Voltage	+3.6		+6.0	Volts	R_L = 450Ω to GND; $V_{IN\ LOW}$≤0.8V or $V_{IN\ HIGH}$≥2.0V
Low Level Output Voltage	–6.0		–3.6	Volts	R_L = 450Ω to GND; $V_{IN\ LOW}$≤0.8V or $V_{IN\ HIGH}$≥2.0V
Driver Open Circuit Voltage			±10	Volts	R_L = ∞
Driver Short Circuit Current		±40		mA	–7V≤V_O≤+7V; Infinite duration
Input High Voltage	2.0			Volts	Applies to differential driver inputs
Input Low Voltage			0.8	Volts	Applies to differential driver inputs
Input Current			±10	µA	
Transition Time		30		ns	R_L = 450Ω, C_L = 50pF; Rise/Fall 10% – 90%
Propagation Delay					
t_{PHL}		100		ns	R_L = 450Ω, C_L = 50pF
t_{PLH}		100		ns	R_L = 450Ω, C_L = 50pF
Data Rate			10	Mbps	R_L = 450Ω, C_L = 50pF
Differential Receiver					
Differential Input Threshold	-0.2		+0.2	Volts	-7V≤V_{CM}≤+7V
Input Hysteresis		70		mV	V_{CM}=0V
Input Resistance	12			kΩ	-7V≤V_{CM}≤+7V
Output Voltage High	3.5			Volts	I_{SOURCE} = –4mA
Output Voltage Low			0.4	Volts	I_{SINK} = +4mA
Short Circuit Current			85	mA	0V≤V_{OUT}≤V_{CC}

SPECIFICATIONS (CONTINUED)

T_{MIN} to T_{MAX} and V_{CC} = 5V±5% unless otherwise noted.

PARAMETER	MIN.	TYP.	MAX.	UNITS	CONDITIONS
Differential Receiver					
Propagation Delay					
t_{PHL}		100		ns	R_L = 450Ω, C_L = 50pF
t_{PLH}		100		ns	R_L = 450Ω, C_L = 50pF
Data Rate			10	Mbps	R_L = 450Ω, C_L = 50pF
Single-Ended Inverting Receiver					
Input Voltage Range	–15		+15	Volts	
Input Threshold Low	0.8	1.2		Volts	
Input Threshold High		1.7	3.0	Volts	
Hysteresis		70		mV	
Input Impedance	3	5	7	kΩ	
Output Voltage High	3.5			Volts	I_{SOURCE} = –4mA
Output Voltage Low			0.4	Volts	I_{SINK} = +4mA
Propagation Delay					
t_{PHL}		100		ns	
t_{PLH}		100		ns	
Data Rate			10	Mbps	
Single-Ended Non-Inverting Receiver					
Input Voltage Range	–7		+7	Volts	
Input Threshold Low	-0.2			Volts	
Input Threshold High			+0.2	Volts	
Hysteresis		70		mV	
Input Impedance	12	15		kΩ	
Output Voltage High	3.5			Volts	I_{SOURCE} = –4mA
Output Voltage Low			0.4	Volts	I_{SINK} = +4mA
Propagation Delay					
t_{PHL}		100		ns	
t_{PLH}		100		ns	
Data Rate			10	Mbps	
PC Mode (pin 25 = GND)					
RS-232 Driver					
TTL Input Levels					
V_{IL}			0.8	Volts	Applies to transmitter inputs
V_{IH}	2.0			Volts	Applies to transmitter inputs
High Level Voltage Output	+5.0		+15.0	Volts	R_L = 3KΩ to Gnd
Low Level Voltage Output	-15.0		-5.0	Volts	R_L = 3KΩ to Gnd
Open Circuit Output			±15	Volts	R_L = ∞
Short Circuit Current			±100	mA	V_{OUT} = Gnd
Power Off Impedance	300			Ohms	V_{CC}=0V; V_{OUT}= ±2V
Slew Rate		60		V/µS	R_L=3KΩ, C_L=50pF; From +3V to -3V or -3V to +3V
Transition Time			1.56	µS	Rise/fall time, between +3V & –3V ; R_L=3KΩ, C_L=2500pF
Propagation Delay					
t_{PHL}		1.5		µS	R_L=3KΩ, C_L=2500pF; From 1.5V of T_{IN} to 50% of V_{OUT}
t_{PLH}		1.3		µS	R_L=3KΩ, C_L=2500pF; From 1.5V of T_{IN} to 50% of V_{OUT}
Data Rate		400		Kbps	R_L=3KΩ, C_L=2500pF
RS-232 Receiver					
TTL Output Levels					
V_{OL}			0.4	Volts	I_{SINK} = 4mA
V_{OH}	2.4				I_{SOURCE} = -4mA
Receiver Input High Threshold		1.7	3.0	Volts	

SPECIFICATIONS (CONTINUED)

T_{MIN} to T_{MAX} and V_{CC} = 5V±5% unless otherwise noted.

PARAMETER	MIN.	TYP.	MAX.	UNITS	CONDITIONS
RS-232 Receiver					
Low Threshold	0.8	1.2		Volts	
Input Voltage Range	-15		+15	Volts	
Input Impedance	3	5	7	KOhms	V_{IN}=±15V
Hysteresis	0.2	0.5	1.0	Volts	V_{CC}=+5V
Transmission Rate			10	Mbps	
Transition Time		50		ns	Rise/fall time; between +3V & −3V
Propagation Delay					
t_{PHL}		100		ns	From 50% of V_{IN} to 1.5V of R_{OUT}
t_{PLH}		100		ns	From 50% of V_{IN} to 1.5V of R_{OUT}
POWER REQUIREMENTS					
No Load Supply Current		19	25	mA	No load; V_{CC}=5.0V; T_A=25˚C
Shutdown Supply Current			20	µA	T_A=25˚C, V_{CC}=5.0V
AC PARAMETERS					
Driver Delay Time from Enable Mode to Tri-state Mode					
Single-Ended Mode					
t_{PZL}; Enable to Output low		90		ns	C_L=100pF, Figures 2 & 4, S_2 closed
t_{PZH}; Enable to Output high		90		ns	C_L=100pF, Figures 2 & 4, S_1 closed
t_{PLZ}; Disable from Output low		90		ns	C_L=15pF, Figures 2 & 4, S_2 closed
t_{PHZ}; Disable from Output high		90		ns	C_L=15pF, Figures 2 & 4, S_1 closed
Differential Mode					
t_{PZL}; Enable to Output low		90		ns	C_L=100pF, Figures 2 & 4, S_2 closed
t_{PZH}; Enable to Output high		90		ns	C_L=100pF, Figures 2 & 4, S_1 closed
t_{PLZ}; Disable from Output low		90		ns	C_L=15pF, Figures 2 & 4, S_2 closed
t_{PHZ}; Disable from Output high		90		ns	C_L=15pF, Figures 2 & 4, S_1 closed
Receiver Delay Time from Enable Mode to Tri-state Mode					
Single-Ended Mode					
t_{PZL}; Enable to Output low		90		ns	C_{RL}=15pF, Figures 1 & 6, S_1 closed
t_{PZH}; Enable to Output high		90		ns	C_{RL}=15pF, Figures 1 & 6, S_2 closed
t_{PLZ}; Disable from Output low		90		ns	C_{RL}=15pF, Figures 1 & 6, S_1 closed
t_{PHZ}; Disable from Output high		90		ns	C_{RL}=15pF, Figures 1 & 6, S_2 closed
Differential Mode					
t_{PZL}; Enable to Output low		90		ns	C_{RL}=15pF, Figures 1 & 6, S_1 closed
t_{PZH}; Enable to Output high		90		ns	C_{RL}=15pF, Figures 1 & 6, S_2 closed
t_{PLZ}; Disable from Output low		90		ns	C_{RL}=15pF, Figures 1 & 6, S_1 closed
t_{PHZ}; Disable from Output high		90		ns	C_{RL}=15pF, Figures 1 & 6, S_2 closed

Notes:
1. Measured from 2.5V of R_{IN} to 2.5V of R_{OUT}.
2. Measured from one–half of R_{IN} to 2.5V of R_{OUT}.
3. Measured from 1.5V of T_{IN} to one–half of T_{OUT}.
4. Measured from 2.5V of R_O to 0V of A and B.

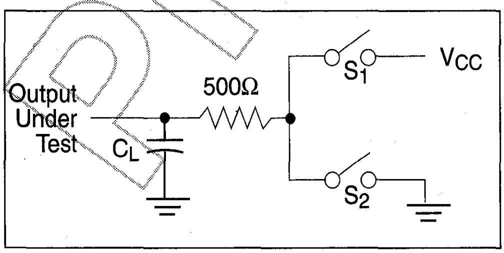


Figure 1. Receiver Timing Test Load Circuit

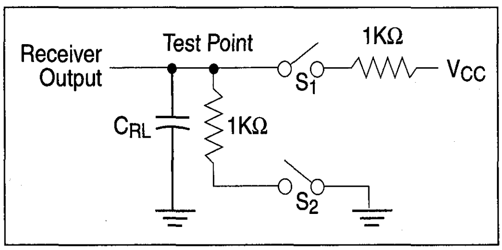


Figure 2. Driver Timing Test Load Circuit

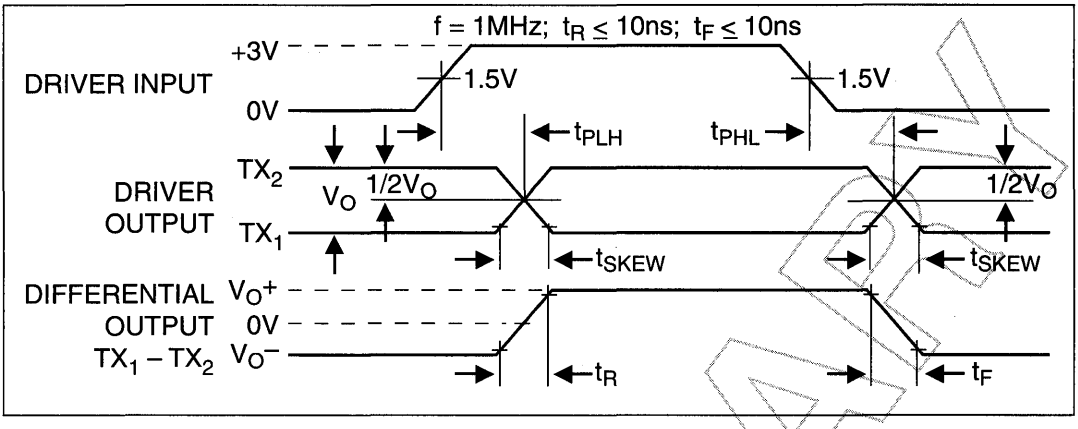


Figure 3. Driver Propagation Delays

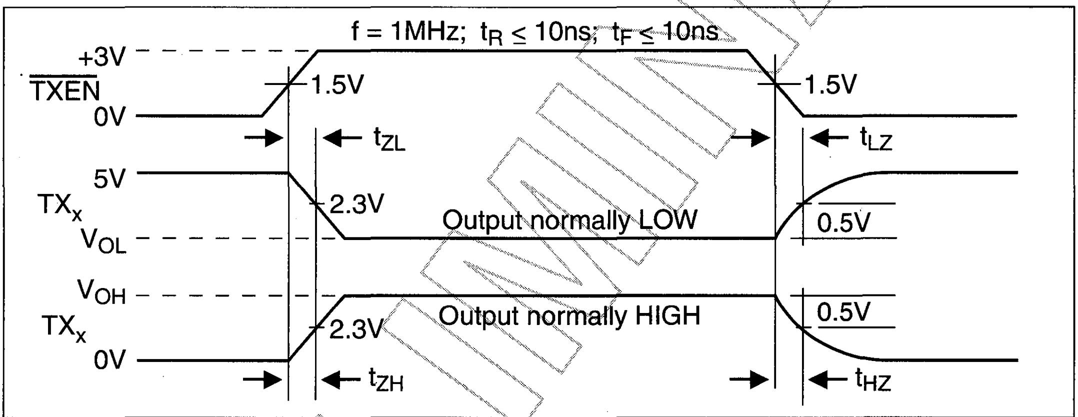


Figure 4. Driver Enable and Disable Times

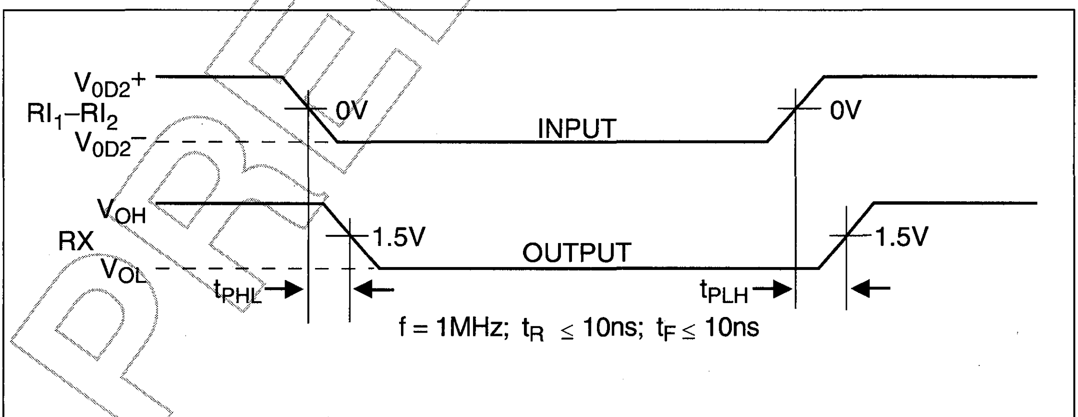


Figure 5. Receiver Propagation Delays

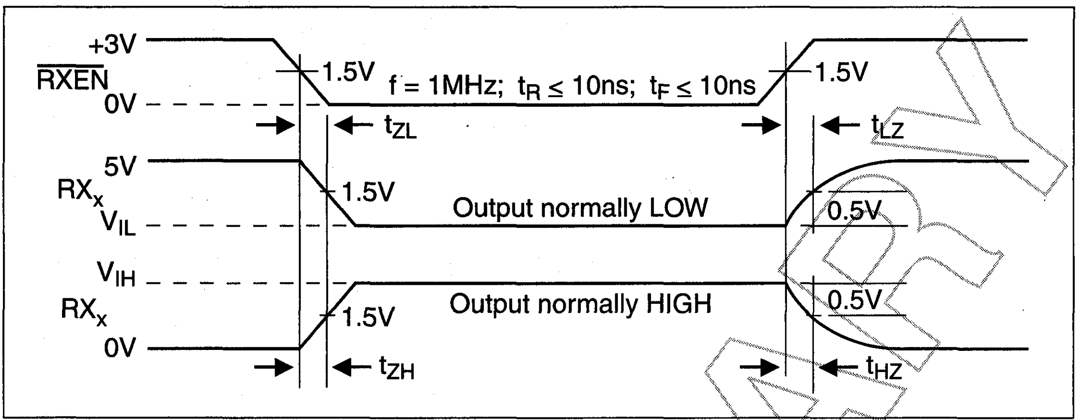


Figure 6. Receiver Enable and Disable Times

THEORY OF OPERATION...

The **SP333** is a single chip device that can be configured via software for either RS-232 or AppleTalk™ interface modes at any time. The **SP333** is made up of three basic circuit elements; single-ended drivers and receivers, differential drivers and receivers and charge pump.

APPLETALK™ DRIVERS/RECEIVERS...

To program the **SP333** for MacMode, pin 25 should be connected to a logic high. In MacMode, the **SP333** offers a complete AppleTalk serial interface.

The driver section of the AppleTalk interface is made up of a differential driver and a single-ended inverting driver. The differential driver has voltage swings that are typically ±5V on each output pin under loaded conditions, and typically ±8V under no-load conditions. The differential driver can maintain ±3.6V (minimum) swings (per pin) under worst case load conditions of 450Ω between the differential output.

The differential driver is equipped with a tri-state control pin. When $\overline{TXEN}$ is a logic low, the differential driver is active. When the $\overline{TXEN}$ pin is a logic high, the differential driver outputs are tri-stated. The $\overline{TXEN}$ pin only functions in MacMode. The differential AppleTalk driver can support data rates up to 10Mbps.

The single-ended AppleTalk driver also has typical voltage output swings of ±5V under loaded conditions, and ±8V under no-load conditions. The single-ended AppleTalk driver can maintain ±3.6V (minimum) swings under worst case conditions of 450Ω to ground. The single-ended AppleTalk driver can support data rates over 400Kbps.

The receiver section of the **SP333** is made up of a differential receiver, a single-ended non-inverting receiver , and a single-ended inverting receiver. The differential receiver has an input sensitivity of ±200mV over a common mode range of ±7V. The receivers have a typical input resistance of 15KΩ (12KΩ minimum). The differential receiver can receive data up to 10Mbps.

The single-ended non-inverting receiver has a ±200mV input threshold, however, the input voltage can vary between ±7V. The typical input resistance of the single-ended non-inverting receiver is 15KΩ (12KΩ minimum). The single-ended non-inverting receiver can also receive data up to 10Mbps.

The **SP333** also has a single-ended inverting receiver input. This receiver is basically an RS-232 receiver (R5 receiver) and is typically used as a GPI (General Purpose Input) in the AppleTalk interface. The GPI input has TTL-compatible input thresholds that can receive signals up to ±15V. The input resistance of the single-ended inverting receiver is typically 5KΩ (3KΩ to 7KΩ). The GPI receiver can operate up to 10Mbps.

SINGLE ENDED DRIVERS/RECEIVERS...

RS-232 (V.28) Drivers...

The single-ended drivers and receivers comply the with the RS-232E and V.28 standards. The drivers are inverting transmitters which accept either TTL or CMOS inputs and output the RS-232 signals with an inverted sense relative to the input logic levels. Typically, the RS-232 driver output voltage swing is ±9V with no load and is guaranteed to be greater than ±5V under full load. The drivers rely on the V+ and V- voltages generated by the on-chip charge pump to maintain proper RS-232 output levels. With worst case load conditions of 3KΩ and 2500pF, the four RS-232 drivers can still maintain ±5V output levels. The drivers can operate over 400Kbps; the propagation delay from input to output is typically 1.5µS. During shutdown, the driver outputs will be put into a high impedance tri-state mode.

RS-232 (V.28) Receivers...

The RS-232 receivers convert RS-232 input signals to inverted TTL signals. Each of the four receivers features 500mV of hysteresis margin to minimize the affects of noisy tranmission lines. The inputs also have a 5KΩ resistor to ground, in an open circuit situation the input of the receiver will be forced low, committing the output to a logic high state. The input resistance will maintain 3KΩ-7KΩ over a ±15V range. The maximum operating voltage range for the receiver is ±30V, under these conditions the input current to the receiver must be limited to less than 100mA. Due to the on chip ESD protection circuitry, the receiver inputs will be clamped to ±15V levels; this should not affect operation at ±30 volts. The RS-232 receivers can operate over 400Kbps.

CHARGE PUMP...

The charge pump is a Sipex-patented design (5,306,954) and uses a unique approach compared to older less-efficient designs. The charge pump still requires four external capacitors, but uses a four-phase voltage shifting technique to attain symmetrical 10V power supplies. The capacitor values of the **SP333** can be as low as 0.1µF. *Figure 11a* shows the waveform found on the positive side of capacitor C2, and *Figure 11b* shows the negative side of capacitor C2. There is a free-running oscillator that controls the four phases of the voltage shifting. A description of each phase follows.

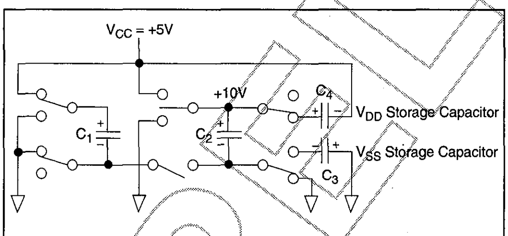


Figure 7. Charge Pump Phase 1

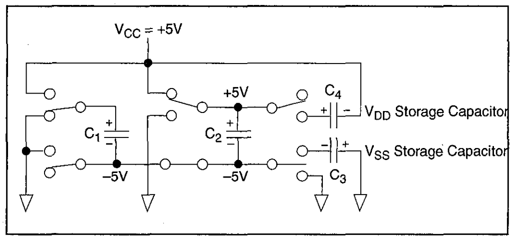


Figure 8. Charge Pump Phase 2

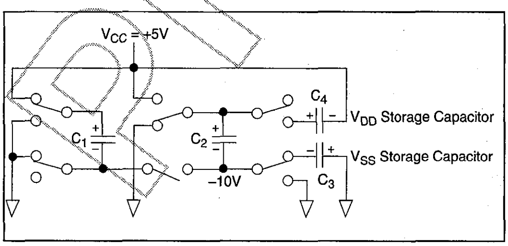


Figure 9. Charge Pump Phase 3

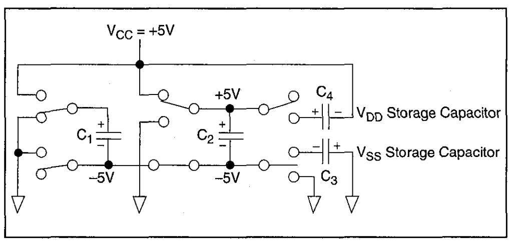


Figure 10. Charge Pump Phase 4

Phase 1

-Vss charge storage- During this phase of the clock cycle, the positive side of capacitors C1 and C2 are initially charged to +5V. C1+ is then switched to ground and charge in C1- is transferred to C2-. Since C2+ is connected to +5V, the voltage potential across capacitor C2 is now 10V.

Phase 2

-Vss transfer- Phase two of the clock connects the negative terminal of C2 to the Vss storage capacitor and the positive terminal of C2 to ground, and transfers the generated -10V to C3. Simultaneously, the positive side of capacitor C1 is switched to +5V and the negative side is connected to ground.

Phase 3

-Vdd charge storage- The third phase of the clock is identical to the first phase- the transferred charge in C1 produces -5V in the negative terminal of C1, which is applied to the negative side of capacitor C2. Since C2+ is at +5V, the voltage potential across C2 is 10V.

Phase 4

-Vdd transfer- The fourth phase of the clock connects the negative terminal of C2 to ground and transfers the generated 10V across C2 to C4, the Vdd storage capacitor. Simultaneously with this, the positive side of capacitor C1 is switched to +5V and the negative side is connected to ground, and the cycle begins again.

Since both V+ and V- are separately generated from Vcc in a no load condition, V+ and V- will be symmetrical. Older charge pump approaches that generate V- from V+ will show a decrease in the magnitude of V- compared to V+ due to the inherent inefficiencies in the design.

The clock rate for the charge pump typically operates at 15KHZ. The external capacitors should be 0.1µF with a 16V breakdown rating.

External Power Supplies

For applications that do not require +5V only, external supplies can be applied at the V+ and V- pins. The value of the external supply voltages must be no greater than ±10V. The current drain from the ±10V supplies is used for the RS-232 drivers. For the RS-232 driver, the current requirement is 3.5mA per driver. The external power supplies should provide a power supply sequence of either: +10V, –10V, and then +5V; or –10V, +10V, and then +5V. It is critical that the ±10V supplies are on before V_{CC}.

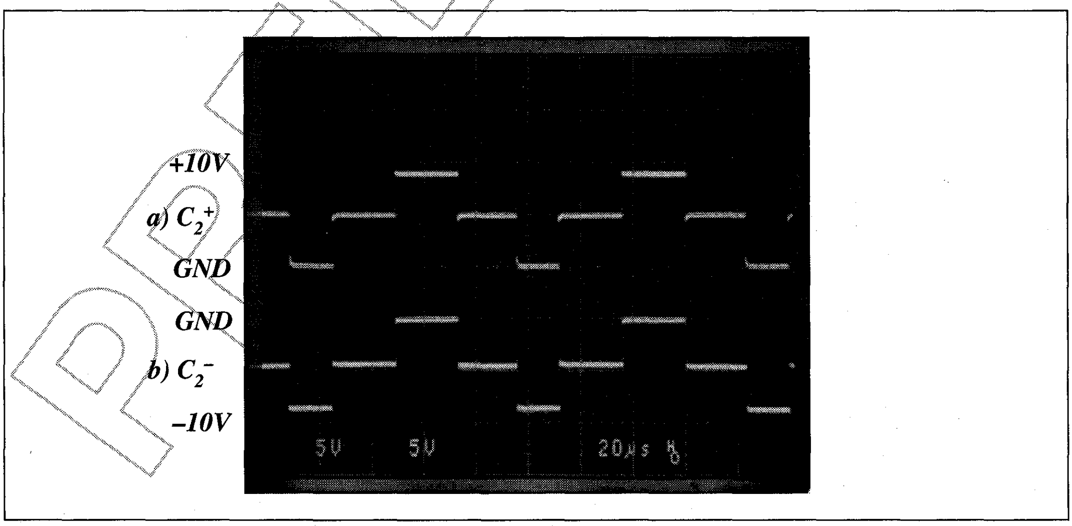


Figure 11. Charge Pump Waveforms

Shutdown Mode

The **SP333** can be put into a low power shutdown mode by connecting the Shutdown pin (SD, pin 26) to a logic high. During shutdown, the driver outputs are put into a high impedance tri-state, and the charge pump is put into standby mode. The supply current drops to less than 10µA during shutdown and can be activated in either RS-232 or AppleTalk mode. For normal operation, the SD pin should be connected to a logic low.

Receiver Enable

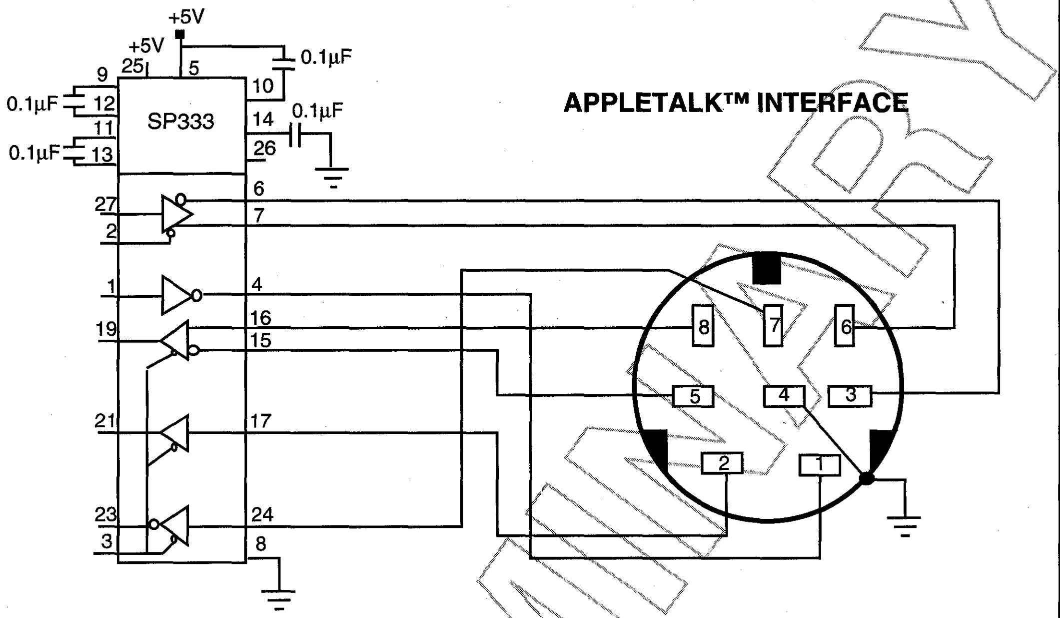
The **SP333** has a control line to enable or disable the receiver outputs. Pin 3 ($\overline{\text{RXEN}}$) is active low; a logic low on pin 3 will enable the receiver outputs. A logic high on pin 3 will disable the receiver outputs. The receiver enable function can be initiated in either RS-232 or AppleTalk mode.

Wake Up

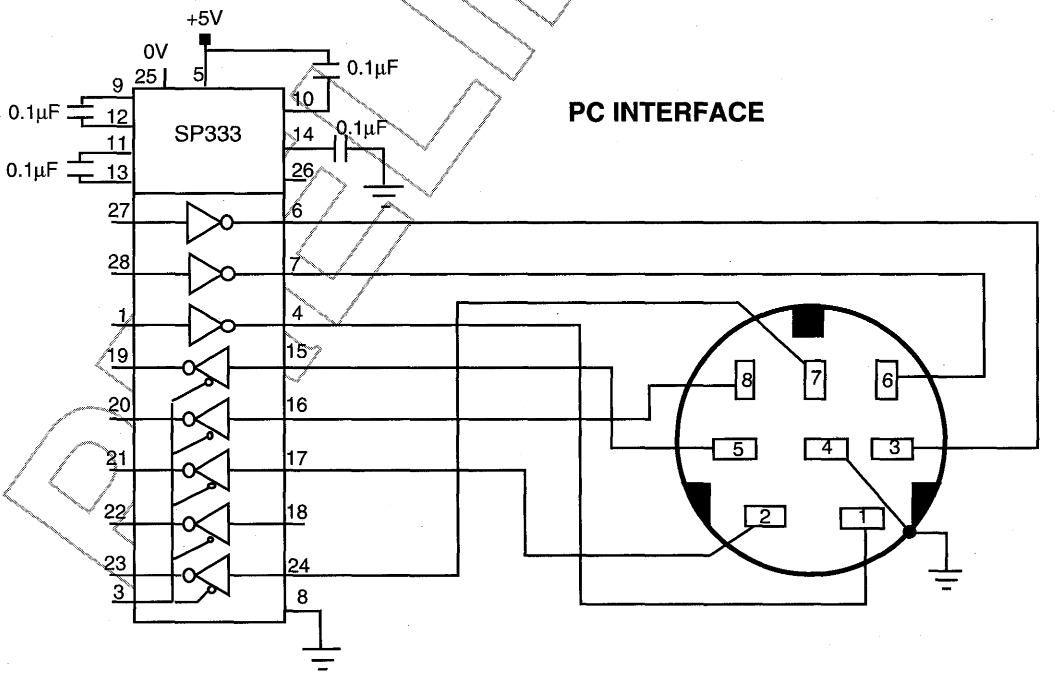
The **SP333** also features a "wake up" function. The wake up function allows the RS-232 receivers to remain active during shutdown mode unless they are disabled by the receiver enable control pin (pin 3). The wake up feature allows users to take advantage of the low power shutdown mode and keep the receivers active to accept an incoming "ring indicator" signal.

SP333 Typical Application for AppleTalk™ and RS-232

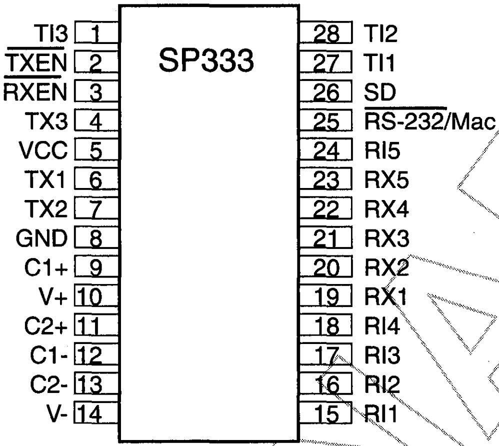
APPLETALK™ INTERFACE



PC INTERFACE

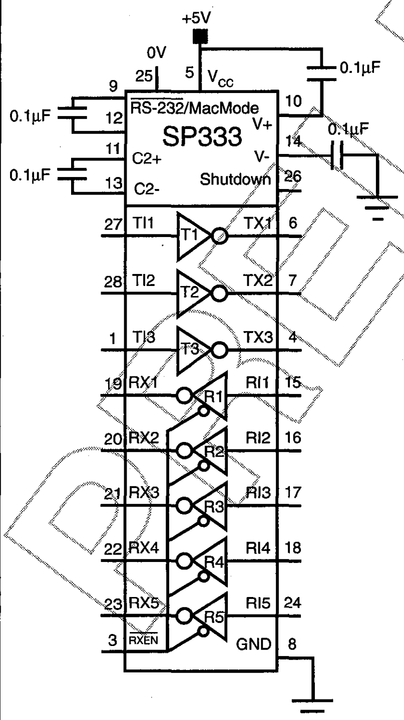


SP333 PIN CONFIGURATION

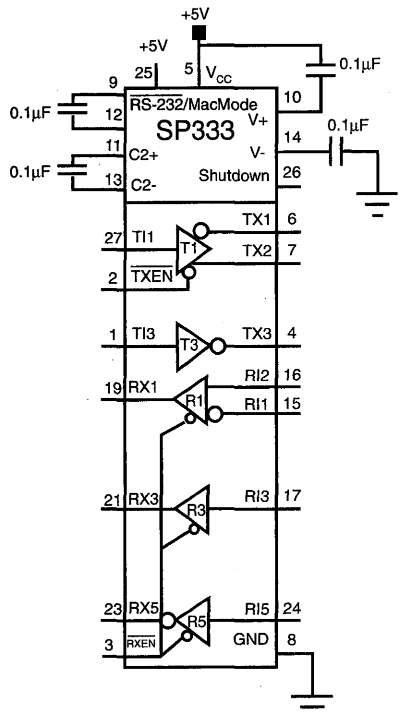


SP333 TYPICAL OPERATING CIRCUIT

PC Mode (RS-232)



Mac Mode (AppleTalk)



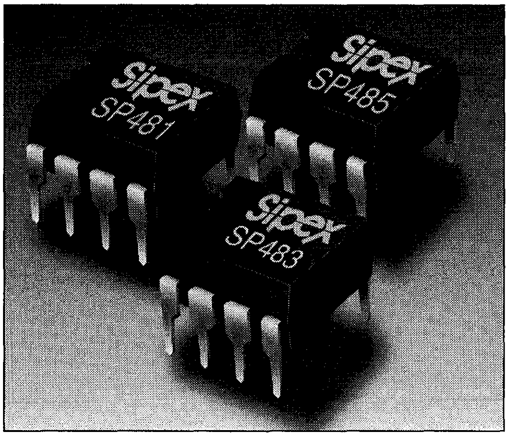
ORDERING INFORMATION

Model	Temperature Range	Package Types
SP333CT	0˚C to +70˚C	28-Pin SOIC
SP333ET	-40˚C to +85˚C	28-Pin SOIC

SP481/SP483/SP485

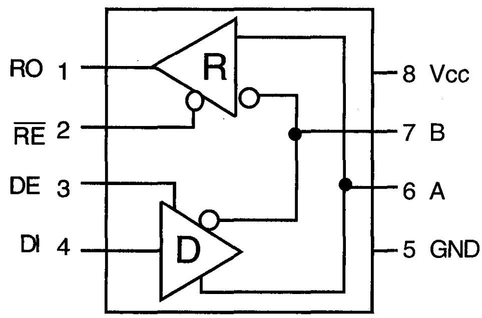
Low Power Half-Duplex RS-485 Transceivers

- +5V Only
- Low Power BiCMOS
- Driver/Receiver Enable
- Slew Rate Limited Driver for Low EMI (SP483)
- Low Power Shutdown Mode (SP481 and SP483)
- RS-485 and RS-422 Drivers/Receivers



DESCRIPTION...

The **SP481**, **SP483**, and the **SP485** are a family of half-duplex transceivers that meet the requirements of RS-485 and RS-422. Their BiCMOS design allows low power operation without sacrificing performance. The **SP481** and **SP485** meet the requirements of RS-485 and RS-422 up to 5Mbps. Additionally, the **SP481** is equipped with a low power Shutdown mode. The **SP483** is internally slew rate limited to reduce EMI and can meet the requirements of RS-485 and RS-422 up to 250kbps. The **SP483** is also equipped with a low power Shutdown mode.



SP481, SP483, and SP485

ABSOLUTE MAXIMUM RATINGS

These are stress ratings only and functional operation of the device at these ratings or any other above those indicated in the operation sections of the specifications below is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

V_{CC} .... ±12V
Input Voltages
- Logic .... -0.3V to (V_{CC}+0.5V)
- Drivers .... -0.3V to (V_{CC}+0.5V)
- Receivers .... ±15V

Output Voltages
- Logic .... -0.3V to (V_{CC}+0.5V)
- Drivers .... ±15V
- Receivers .... -0.3V to (V_{CC}+0.5V)

Storage Temperature .... -65˚C to +150˚C
Power Dissipation 500mW

SPECIFICATIONS

T_{MIN} to T_{MAX} and V_{CC} = 5V ± 5% unless otherwise noted.

PARAMETERS	MIN.	TYP.	MAX.	UNITS	CONDITIONS
SP481/SP483/SP485 DRIVER					
DC Characteristics					
Differential Output Voltage	GND		V_{CC}	Volts	Unloaded; R = ∞ ; *see figure 1*
Differential Output Voltage	2		V_{CC}	Volts	with load; R = 50Ω; (RS422); *see figure 1*
Differential Output Voltage	1.5		V_{CC}	Volts	with load; R = 27Ω; (RS485); *see figure 1*
Change in Magnitude of Driver Differential Output Voltage for Complimentary States			0.2	Volts	R = 27Ω or R = 50Ω; *see figure 1*
Driver Common-Mode Output Voltage			3	Volts	R = 27Ω or R = 50Ω; *see figure 1*
Input High Voltage	2.0			Volts	Applies to DE, DI, $\overline{RE}$
Input Low Voltage			0.8	Volts	Applies to DE, DI, $\overline{RE}$
Input Current			±10	µA	Applies to DE, DI, $\overline{RE}$
Driver Short-Circuit Current					
V_{OUT} = HIGH	35		250	mA	$-7V \leq V_O \leq +12V$
V_{OUT} = LOW	35		250	mA	$-7V \leq V_O \leq +12V$
SP481/SP485 DRIVER					
AC Characteristics					
Driver Data Rate			5	Mbps	$\overline{RE}$ = 5V, DE = 5V
Driver Input to Output	20	30	60	ns	t_{PLH}; R_{DIFF} = 54Ω, $C_{L1} = C_{L2}$ = 100pF; *see figures 3 and 6*
Driver Input to Output	20	30	60	ns	t_{PHL}; R_{DIFF} = 54Ω, $C_{L1} = C_{L2}$ = 100pF; *see figures 3 and 6*
Driver Skew		5	10	ns	From output to output; *see figures 3 and 6*
Driver Rise or Fall Time	3	15	40	ns	From 10% to 90%; R_{DIFF} = 54Ω, $C_{L1} = C_{L2}$ = 100pF; *see figures 3 and 6*
Driver Enable to Output High		40	70	ns	C_L = 100pF; *see figures 4 & 7*; S_2 closed
Driver Enable to Output Low		40	70	ns	C_L = 100pF; *see figures 4 & 7*; S_1 closed
Driver Disable Time from Low		40	70	ns	C_L = 15pF; *see figures 2 & 9*; S_1 closed
Driver Disable Time from High		40	70	ns	C_L = 15pF; *see figures 2 & 9*; S_2 closed
SP481/SP483/SP485 RECEIVER					
DC Characteristics					
Differential Input Threshold	-0.2		+0.2	Volts	$-7V \leq V_{CM} \leq +12V$
Input Hysteresis		10		mV	V_{CM} = 0V
Output Voltage High	3.5			Volts	I_O = -4mA, V_{ID} = +200mV
Output Voltage Low			0.4	Volts	I_O = +4mA, V_{ID} = -200mV
Three-State (High Impedance) Output Current			±1	µA	$0.4V \leq V_O \leq 2.4V$; $\overline{RE}$ = 5V
Input Resistance	12	15		kΩ	$-7V \leq V_{CM} \leq +12V$
Input Current (A, B); V_{IN} = 12V			+1.0	mA	DE = 0V, V_{CC} = 0V or 5.25V, V_{IN} = 12V
Input Current (A, B); V_{IN} = -7V			-0.8	mA	DE = 0V, V_{CC} = 0V or 5.25V, V_{IN} = -7V
Short-Circuit Current	7		95	mA	$0V \leq V_{CM} \leq V_{CC}$

SPECIFICATIONS (continued)

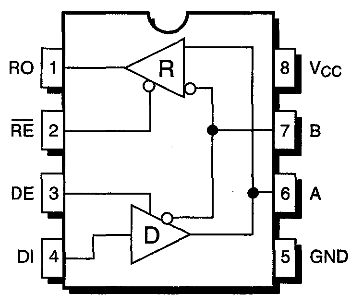
T_{MIN} to T_{MAX} and V_{CC} = 5V ± 5% unless otherwise noted.

PARAMETERS	MIN.	TYP.	MAX.	UNITS	CONDITIONS
SP481/SP485 RECEIVER					
AC Characteristics					
Receiver Data Rate			5	Mbps	$\overline{RE}$ = 0V, DE = 0V
Receiver Input to Output	60	90	200	ns	t_{PLH}; R_{DIFF} = 54Ω, C_{L1} = C_{L2} = 100pF; *Figures 3 & 8*
Receiver Input to Output	60	90	200	ns	t_{PHL}; R_{DIFF} = 54Ω, C_{L1} = C_{L2} = 100pF; *Figures 3 & 8*
Diff. Receiver Skew $\lvert t_{PLH}-t_{PHL}\rvert$		13		ns	R_{DIFF} = 54Ω; C_{L1} = C_{L2} = 100pF; *Figures 3 & 8*
Receiver Enable to Output Low		20	50	ns	C_{RL} = 15pF; *Figures 2 & 9*; S_1 closed
Receiver Enable to Output High		20	50	ns	C_{RL} = 15pF; *Figures 2 & 9*; S_2 closed
Receiver Disable from Low		20	50	ns	C_{RL} = 15pF; *Figures 2 & 9*; S_1 closed
Receiver Disable from High		20	50	ns	C_{RL} = 15pF; *Figures 2 & 9*; S_2 closed
SP481					
Shutdown Timing					
Time to Shutdown	50	200	600	ns	$\overline{RE}$ = 5V, DE = 0V
Driver Enable from Shutdown to Output High		40	100	ns	C_L = 100pF; *See figures 4 & 7;* S_2 closed
Driver Enable from Shutdown to Output Low		40	100	ns	C_L = 100pF; *See figures 4 & 7;* S_1 closed
Receiver Enable from Shutdown to Output High		300	1000	ns	C_L = 15pF; *See figures 2 & 9;* S_1 closed
Receiver Enable from Shutdown to Output Low		300	1000	ns	C_L = 15pF; *See figures 2 & 9;* S_2 closed
POWER REQUIREMENTS					
Supply Voltage	+4.75		+5.25	Volts	
Supply Current					
SP481/485					
No Load		500	900	µA	$\overline{RE}$, DI = 0V or V_{CC}; DE = V_{CC}
		300		µA	$\overline{RE}$ = 0V, DI = 0V or 5V; DE = 0V
SP483					
No Load		350	650	µA	$\overline{RE}$, DI = 0V or V_{CC}; DE = V_{CC}
		250		µA	$\overline{RE}$=0V, DI = 0V or 5V; DE = 0V
SP481/SP483					
Shutdown Mode			10	µA	DE = 0V, $\overline{RE}$=V_{CC}
ENVIRONMENTAL AND MECHANICAL					
Operating Temperature					
Commercial (_C_)	0		+70	°C	
Industrial (_E_)	-40		+85	°C	
Storage Temperature	-65		+150	°C	
Package					
Plastic DIP (_S)					
NSOIC (_N)					

SP483 AC SPECIFICATIONS

T_{MIN} to T_{MAX} and V_{CC} = 5V ± 5% unless otherwise noted.

PARAMETERS	MIN.	TYP.	MAX.	UNITS	CONDITIONS
SP483 DRIVER					
AC Characteristics					
Driver Data Rate			250	kbps	
Driver Input to Output	250	800	2000	ns	t_{PLH}; R_{DIFF} = 54Ω, C_{L1} = C_{L2} = 100pF; *see figures 3 & 6*
Driver Skew	250	800	2000	ns	t_{PHL}; R_{DIFF} = 54Ω, C_{L1} = C_{L2} = 100pF; *see figures 3 & 6*
Driver Rise and Fall Time		100	800	ns	From output to output; *see figures 3 & 6*
	250		2000	ns	From 10% to 90%; R_{DIFF} = 54Ω, C_{L1} = C_{L2} = 100pF, *see figures 3 & 6*
Driver Enable to Output High	250		2000	ns	C_L = 100pF; *See figures 4 & 7;* S_2 closed
Driver Enable to Output Low	250		2000	ns	C_L = 100pF; *See figures 4 & 7;* S_1 closed
Driver Disable Time from Low	300		3000	ns	C_L = 15pF; *See figures 4 & 7;* S_1 closed
Driver Disable Time from High	300		3000	ns	C_L = 15pF; *See figures 4 & 7;* S_2 closed
SP483 RECEIVER					
AC Characteristics					
Receiver Data Rate			250	kbps	
Receiver Input to Output	250		2000	ns	t_{PLH}; R_{DIFF} = 54Ω, C_{L1} = C_{L2} = 100pF; *Figures 3 & 8*
Diff. Receiver Skew $\lvert t_{PLH}-t_{PHL}\rvert$		100		ns	R_{DIFF} = 54Ω, C_{L1} = C_{L2} = 100pF; *Figures 3 & 8*
Receiver Enable to Output Low		20	50	ns	C_{RL} = 15pF; *Figures 2 & 9;* S_1 closed
Receiver Enable to Output High		20	50	ns	C_{RL} = 15pF; *Figures 2 & 9;* S_2 closed
Receiver Disable from Low		20	50	ns	C_{RL} = 15pF; *Figures 2 & 9;* S_1 closed
Receiver Disable from High		20	50	ns	C_{RL} = 15pF; *Figures 2 & 9;* S_2 closed
SP483					
Shutdown Timing					
Time to Shutdown	50	200	600	ns	$\overline{RE}$ = 5V, DE = 0V
Driver Enable from Shutdown to Output High			2000	ns	C_L = 100pF; *See figures 4 & 7;* S_2 closed
Driver Enable from Shutdown to Output Low			2000	ns	C_L = 100pF; *See figures 4 & 7;* S_1 closed
Receiver Enable from Shutdown to Output High			2500	ns	C_L = 15pF; *See figures 4 & 7;* S_1 closed
Receiver Enable from Shutdown to Output Low			2500	ns	C_L = 15pF; *See figures 4 & 7;* S_2 closed



SP481, SP483, SP485
Pinout (Top View)

PIN FUNCTION

Pin#	Name	Description
1	RO	Receiver Output.
2	$\overline{RE}$	Receiver Output Enable Active LOW.
3	DE	Driver Output Enable Active HIGH.
4	DI	Driver Input.
5	GND	Ground Connection.
6	A	Driver Output/Receiver Input Non-inverting.
7	B	Driver Output/Receiver Input Inverting.
8	Vcc	Positive Supply 4.75V<Vcc< 5.25V.

DESCRIPTION...
SP481, SP483, SP485

The **SP481**, **SP483**, and **SP485** are half-duplex differential transceivers that meet the requirements of RS-485 and RS-422. Fabricated with a Sipex proprietary BiCMOS process, all three products require a fraction of the power of older bipolar designs.

The RS-485 standard is ideal for multi-drop applications and for long-distance interfaces. RS-485 allows up to 32 drivers and 32 receivers to be connected to a data bus, making it an ideal choice for multi-drop applications. Since the cabling can be as long as 4,000 feet, RS-485 transceivers are equipped with a wide (-7V to +12V) common mode range to accommodate ground potential differences. Because RS-485 is a differential interface, data is virtually immune to noise in the transmission line.

Drivers...
SP481, SP483, SP485

The driver outputs of the **SP481**, **SP483**, and **SP485** are differential outputs meeting the RS-485 and RS-422 standards. The typical voltage output swing with no load will be 0 volts to +5 volts. With worst case loading of 54Ω across the differential outputs, the drivers can maintain greater than 1.5V voltage levels. The drivers of the **SP481**, **SP483** and **SP485** have an enable control line which is active HIGH. A logic HIGH on DE (pin 5) will enable the differential driver outputs. A logic LOW on DE (pin 5) will tri-state the driver outputs.

The transmitters of the **SP481** and **SP485** will operate up to 5Mbps. The **SP483** has internally slew rate limited driver outputs to minimize EMI. The maximum data rate for the **SP483** driver is 250kbps.

Receivers...
SP481, SP483, SP485

The **SP481**, **SP483**, and **SP485** receivers have differential inputs with an input sensitivity as low as ±200mV. Input impedance of the receivers is typically 15kΩ (12kΩ minimum). A wide common mode range of -7V to +12V allows for large ground potential differences between systems. The receivers of the **SP481**, **SP483** and **SP485** have a tri-state enable control pin. A logic LOW on $\overline{RE}$ (pin 4) will enable the receiver, a logic HIGH on $\overline{RE}$ (pin 4) will disable the receiver.

The receiver for the **SP481** and **SP485** will operate up to 5Mbps. The **SP483** receiver is rated for data rates up to 250kbps. The receiver for each of the three devices is equipped with the fail-safe feature. Fail-safe guarantees that the receiver output will be in a HIGH state when the input is left unconnected.

Shutdown Mode...
SP481/SP483

The **SP481** and **SP483** are equipped with a Shutdown mode. To enable the Shutdown state, both the driver and receiver must be disabled simultaneously. A logic LOW on DE (pin 5) and a logic HIGH on $\overline{RE}$ (pin 4) will put the **SP481** or **SP483** into Shutdown mode. In Shutdown, supply current will drop to typically 1µA.

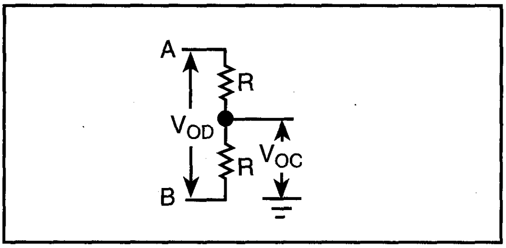


Figure 1. Driver DC Test Load Circuit

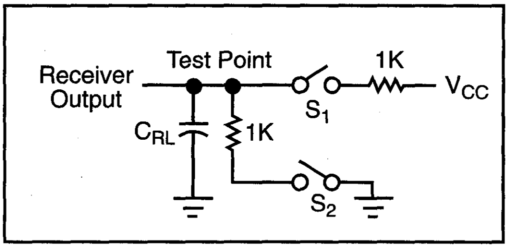


Figure 2. Receiver Timing Test Load Circuit

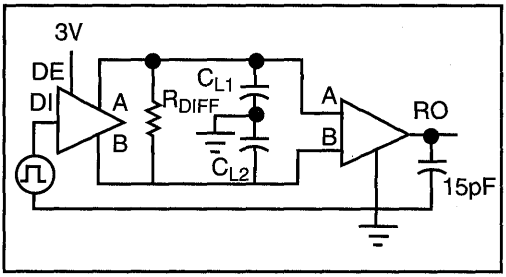


Figure 3. Driver/Receiver Timing Test Circuit

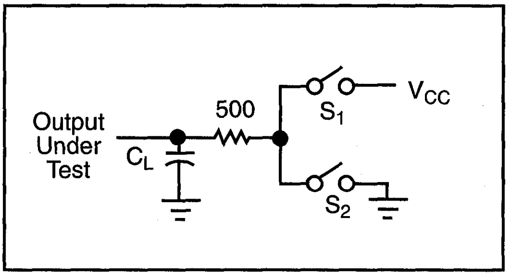


Figure 4. Driver Timing Test Load #2 Circuit

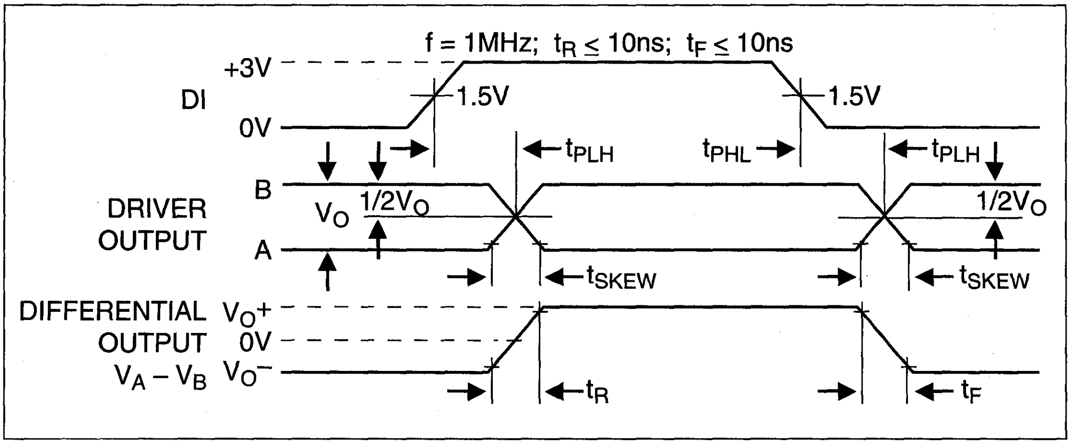


Figure 6. Driver Propagation Delays

INPUTS				OUTPUTS	
$\overline{RE}$	DE	DI	LINE CONDITION	B	A
X	1	1	No Fault	0	1
X	1	0	No Fault	1	0
X	0	X	X	Z	Z
X	1	X	Fault	Z	Z

Table 1. Transmit Function Truth Table

INPUTS			OUTPUTS
$\overline{RE}$	DE	A - B	R
0	0	+0.2V	1
0	0	-0.2V	0
0	0	Inputs Open	1
1	0	X	Z

Table 2. Receive Function Truth Table

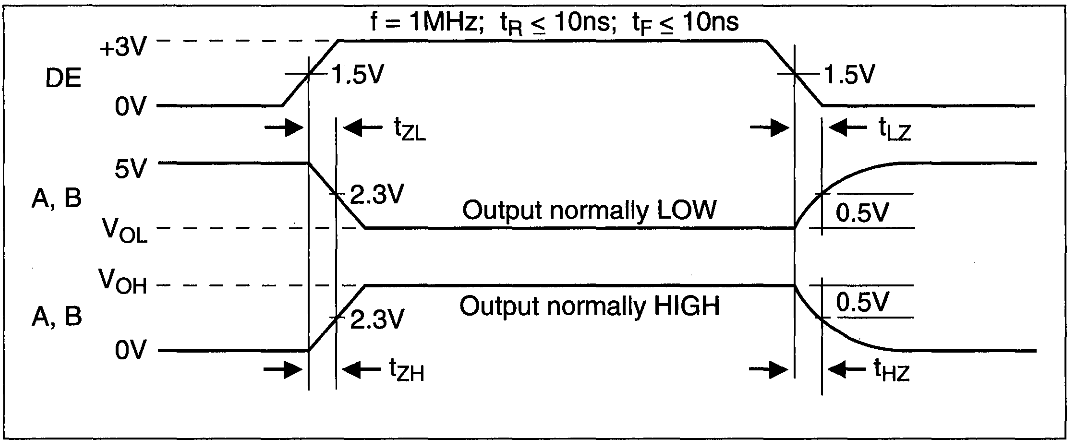


Figure 7. Driver Enable and Disable Times

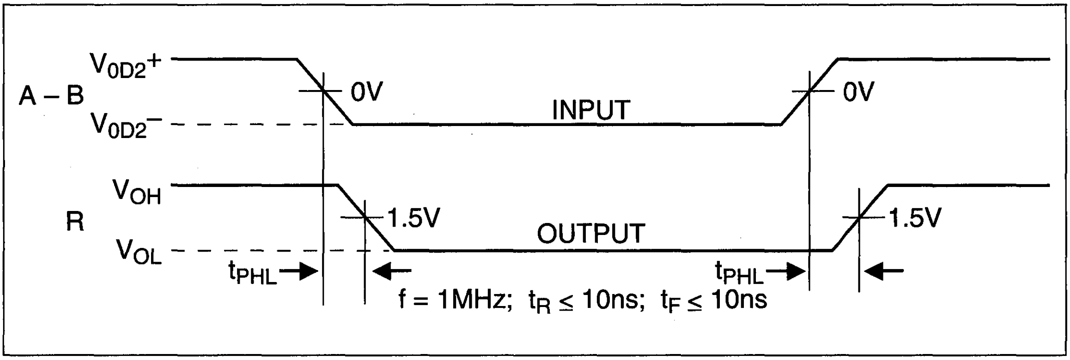


Figure 8. Receiver Propagation Delays

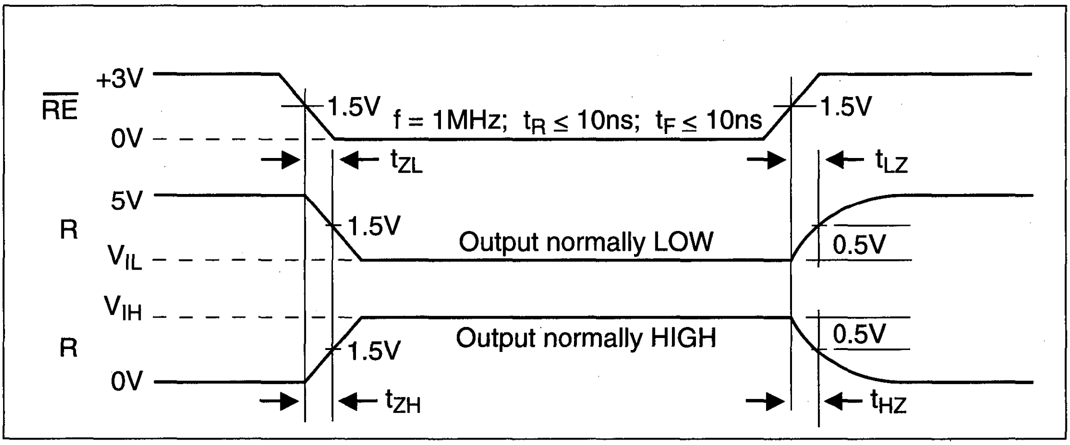


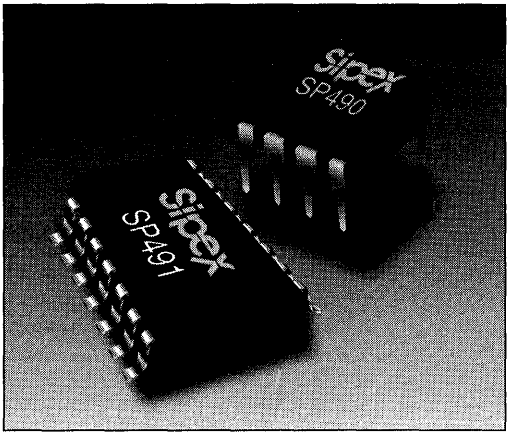
Figure 9. Receiver Enable and Disable Times

ORDERING INFORMATION

Model	Temperature Range	Package
SP481CN	0°C to +70°C	8-pin Narrow SOIC
SP481CS	0°C to +70°C	8-pin Plastic DIP
SP481EN	-40°C to +85°C	8-pin Narrow SOIC
SP481ES	-40°C to +85°C	8-pin Plastic DIP
SP483CN	0°C to +70°C	8-pin Narrow SOIC
SP483CS	0°C to +70°C	8-pin Plastic DIP
SP483EN	-40°C to +85°C	8-pin Narrow SOIC
SP483ES	-40°C to +85°C	8-pin Plastic DIP
SP485CN	0°C to +70°C	8-pin Narrow SOIC
SP485CS	0°C to +70°C	8-pin Plastic DIP
SP485EN	-40°C to +85°C	8-pin Narrow SOIC
SP485ES	-40°C to +85°C	8-pin Plastic DIP

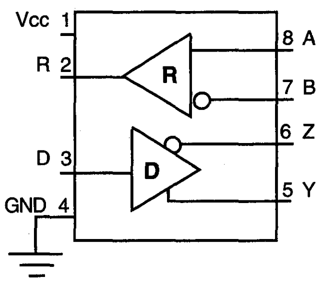
Full Duplex RS-485 Transceivers

- +5V Only
- Low Power BiCMOS
- Driver/Receiver Enable (SP491)
- RS-485 and RS-422 Drivers/Receivers
- Pin Compatible with LTC490 and SN75179 (SP490)
- Pin Compatible with LTC491 and SN75180 (SP491)

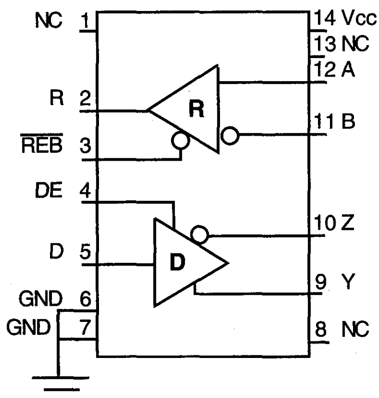


DESCRIPTION...

The **SP490** is a low power differential line driver/receiver meeting RS-485 and RS-422 standards up to 5Mbps. The **SP491** is identical to the **SP490** with the addition of driver and receiver tri-state enable lines. Both products feature ±200mV receiver input sensitivity, over wide common mode range. The **SP490** is available in 8-pin plastic DIP and 8-pin NSOIC packages for operation over the commercial and industrial temperature ranges. The **SP491** is available in 14-pin DIP and 14-pin NSOIC packages for operation over the commercial and industrial temperature ranges.



SP490



SP491

ABSOLUTE MAXIMUM RATINGS

These are stress ratings only and functional operation of the device at these ratings or any other above those indicated in the operation sections of the specifications below is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

V_{CC} .... +12V
Input Voltages
Drivers .... -0.5V to (V_{CC}+0.5V)
Receivers .... ±14V
Output Voltages
Drivers .... ±14V
Receivers .... -0.5V to (V_{CC}+0.5V)
Storage Temperature .... -65°C to +150°
Power Dissipation 1000mW

SPECIFICATIONS

T_{MIN} to T_{MAX} and V_{CC} = 5V ± 5% unless otherwise noted.

PARAMETERS	MIN.	TYP.	MAX.	UNITS	CONDITIONS
SP490 DRIVER					
DC Characteristics					
Differential Output Voltage	GND		V_{CC}	Volts	Unloaded; R = ∞ ; *see figure 1*
Differential Output Voltage	2		V_{CC}	Volts	With Load; R = 50Ω; (RS422); *see figure 1*
Differential Output Voltage	1.5		V_{CC}	Volts	With Load; R = 27Ω; (RS485); *see figure 1*
Change in Magnitude of Driver Differential Output Voltage for Complimentary States			0.2	Volts	R = 27Ω or R = 50Ω; *see figure 1*
Driver Common-Mode Output Voltage			3	Volts	R = 27Ω or R = 50Ω; *see figure 1*
Input High Voltage	2.0			Volts	Applies to D
Input Low Voltage			0.8	Volts	Applies to D
Input Current			±10	µA	Applies to D
Driver Short-Circuit Current					
V_{OUT} = HIGH	35		250	mA	-7V ≤ V_O ≤ +12V
V_{OUT} = LOW	35		250	mA	-7V ≤ V_O ≤ +12V
SP490 DRIVER					
AC Characteristics					
Driver Data Rate			5	Mbps	
Driver Input to Output	20	30	60	ns	t_{PLH}; R_{DIFF} = 54Ω, C_{L1} = C_{L2} = 100pF; *see figures 3 and 6*
Driver Input to Output	20	30	60	ns	t_{PHL}; R_{DIFF} = 54Ω, C_{L1} = C_{L2} = 100pF; *see figures 3 and 6*
Driver Skew		5		ns	From output to output; *see figures 3 and 6*
Driver Rise or Fall Time	3	15	40	ns	From 10% to 90%; R_{DIFF} = 54Ω, C_{L1} = C_{L2} = 100pF; *see figures 3 and 6*
SP490 RECEIVER					
DC Characteristics					
Differential Input Threshold	0.2		+0.2	Volts	-7V ≤ V_{CM} ≤ 12V
Input Hysteresis		70		mV	V_{CM} = 0V
Output Voltage High	3.5			Volts	I_O = -4mA, V_{ID} = +200mV
Output Voltage Low			0.4	Volts	I_O = +4mA, V_{ID} = -200mV
Input Resistance	12	15		kΩ	-7V ≤ V_{CM} ≤ 12V
Input Current (A, B); V_{IN} = 12V			±1.0	mA	V_{IN} = 12V
Input Current (A, B); V_{IN} = -7V			-0.8	mA	V_{IN} = -7V
Short-Circuit Current	7		85	mA	0V ≤ V_O ≤ V_{CC}

SPECIFICATIONS (continued)

T_{MIN} to T_{MAX} and V_{CC} = 5V ± 5% unless otherwise noted.

PARAMETERS	MIN.	TYP.	MAX.	UNITS	CONDITIONS
SP490 RECEIVER					
AC Characteristics					
Receiver Data Rate			5	Mbps	
Receiver Input to Output	60	90	150	ns	t_{PLH}; R_{DIFF} = 54Ω, C_{L1} = C_{L2} = 100pF; *Figures 3 & 8*
Receiver Input to Output	60	90	150	ns	t_{PHL}; R_{DIFF} = 54Ω, C_{L1} = C_{L2} = 100pF; *Figures 3 & 8*
Diff. Receiver Skew $\|t_{PLH}-t_{PHL}\|$		13		ns	R_{DIFF} = 54Ω; C_{L1} = C_{L2} = 100pF; *Figures 3 & 8*
POWER REQUIREMENTS					
Supply Voltage	+4.75		+5.25	Volts	
Supply Current		600		µA	
ENVIRONMENTAL AND MECHANICAL					
Operating Temperature					
Commercial (_C_)	0		+70	°C	
Industrial (_E_)	-40		+85	°C	
Storage Temperature	-65		+150	°C	
Package					
Plastic DIP (_S_)					
NSOIC (_N)					

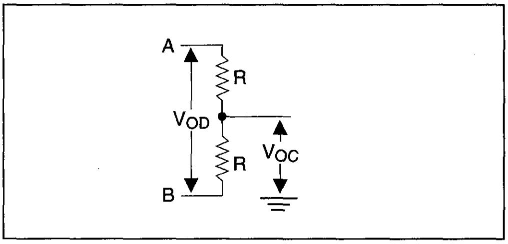


Figure 1. Driver DC Test Load Circuit

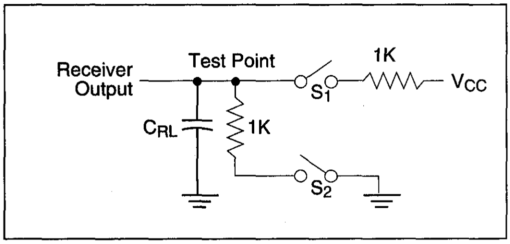


Figure 2. Receiver Timing Test Load Circuit

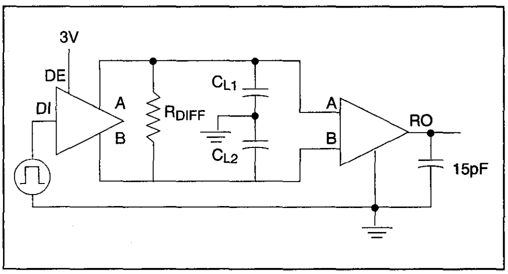


Figure 3. Driver/Receiver Timing Test Circuit

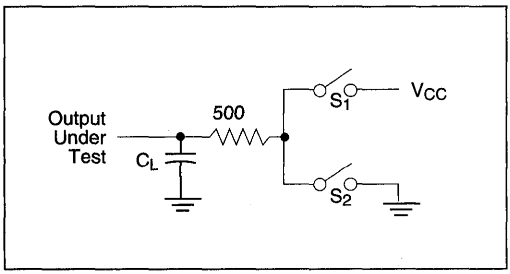


Figure 4. Driver Timing Test Load #2 Circuit

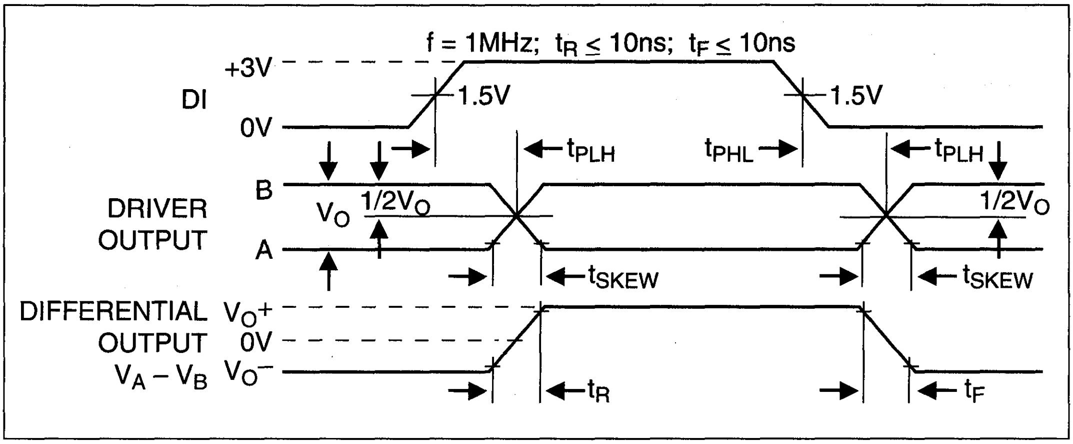


Figure 6. Driver Propagation Delays

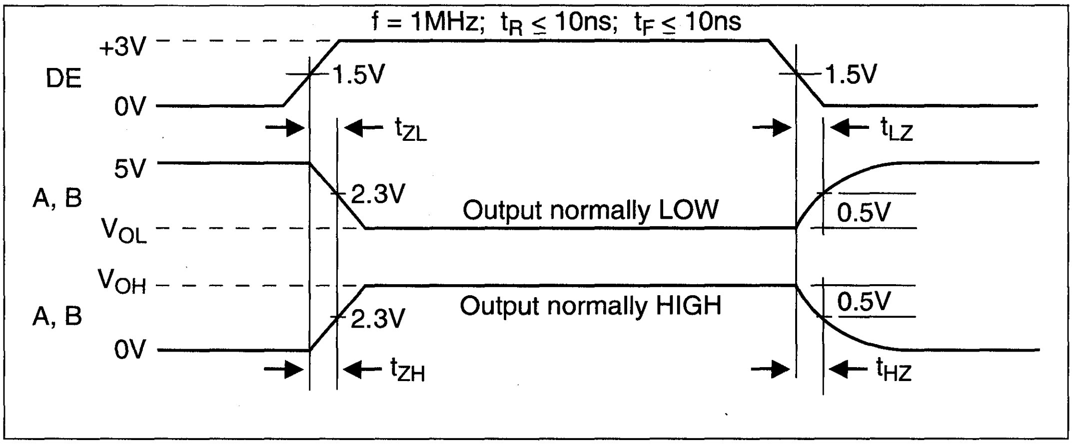


Figure 7. Driver Enable and Disable Times

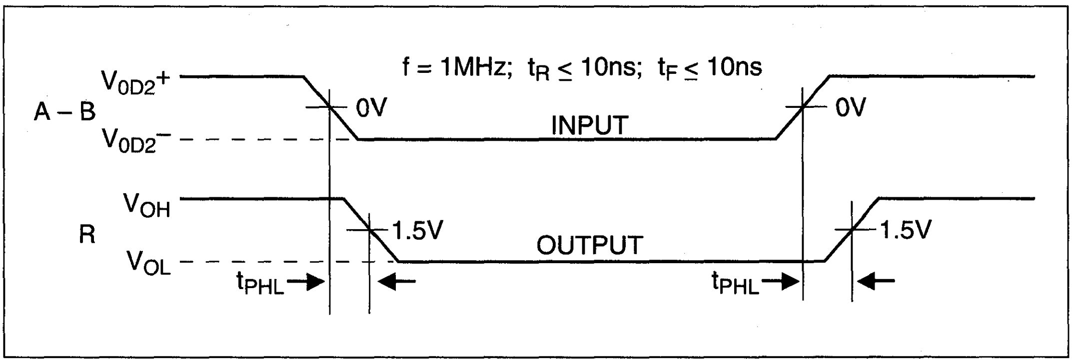


Figure 8. Receiver Propagation Delays

ABSOLUTE MAXIMUM RATINGS

These are stress ratings only and functional operation of the device at these ratings or any other above those indicated in the operation sections of the specifications below is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

V_{CC} .... +12V

Input Voltages
- Logic .... -0.5V to (V_{CC}+0.5V)
- Drivers .... -0.5V to (V_{CC}+0.5V)
- Receivers .... ±14V

Output Voltages
- Logic .... -0.5V to (V_{CC}+0.5V)
- Drivers .... ±14V
- Receivers .... -0.5V to (V_{CC}+0.5V)

Storage Temperature .... -65˚C to +150

Power Dissipation 1000mW

SPECIFICATIONS

T_{MIN} to T_{MAX} and V_{CC} = 5V ± 5% unless otherwise noted.

PARAMETERS	MIN.	TYP.	MAX.	UNITS	CONDITIONS
SP491 DRIVER					
DC Characteristics					
Differential Output Voltage	GND		V_{CC}	Volts	Unloaded; R = ∞ ; *see figure 1*
Differential Output Voltage	2		V_{CC}	Volts	With Load; R = 50Ω; (RS422); *see figure 1*
Differential Output Voltage	1.5		V_{CC}	Volts	With Load; R = 27Ω; (RS485); *see figure 1*
Change in Magnitude of Driver Differential Output Voltage for Complimentary States			0.2	Volts	R = 27Ω or R = 50Ω; *see figure 1*
Driver Common-Mode Output Voltage			3	Volts	R = 27Ω or R = 50Ω; *see figure 1*
Input High Voltage	2.0			Volts	Applies to D, $\overline{REB}$, DE
Input Low Voltage			0.8	Volts	Applies to D, $\overline{REB}$, DE
Input Current			±10	µA	Applies to D, $\overline{REB}$, DE
Driver Short-Circuit Current					
V_{OUT} = HIGH	35		250	mA	-7V ≤ V_O ≤ 12V
V_{OUT} = LOW	35		250	mA	-7V ≤ V_O ≤ 12V
SP491 DRIVER					
AC Characteristics					
Driver Data Rate			5	Mbps	$\overline{REB}$ = 5V, DE = 0V
Driver Input to Output	20	30	60	ns	t_{PLH}; R_{DIFF} = 54Ω, C_{L1} = C_{L2} = 100pF; *see figures 3 and 6*
Driver Input to Output	20	30	60	ns	t_{PHL}; R_{DIFF} = 54Ω, C_{L1} = C_{L2} = 100pF; *see figures 3 and 6*
Driver Skew		5	10	ns	From output to output; *see figures 3 and 6*
Driver Rise or Fall Time	3	15	40	ns	From 10% to 90%; R_{DIFF} = 54Ω, C_{L1} = C_{L2} = 100pF; *see figures 3 and 6*
Driver Enable to Output High		40	70	ns	C_{L1} = C_{L2} = 100pF; *see figures 4 and 7;* S_2 closed
Driver Enable to Output Low		40	70	ns	C_{L1} = C_{L2} = 100pF; *see figures 4 and 7;* S_1 closed
Driver Disable Time from Low		40	70	ns	C_{L1} = C_{L2} = 15pF; *see figures 4 and 7;* S_1 closed
Driver Disable Time from High		40	70	ns	C_{L1} = C_{L2} = 15pF; *see figures 4 and 7;* S_2 closed

SPECIFICATIONS (continued)

T_{MIN} to T_{MAX} and V_{CC} = 5V ± 5% unless otherwise noted.

PARAMETERS	MIN.	TYP.	MAX.	UNITS	CONDITIONS
SP491 RECEIVER					
DC Characteristics					
Differential Input Threshold	-0.2		+0.2	Volts	-7V ≤ V_{CM} ≤ 12V
Input Hysteresis		70		mV	V_{CM} = 0V
Output Voltage High	3.5			Volts	I_O = -4mA, V_{ID} = +200mV
Output Voltage Low			0.4	Volts	I_O = +4mA, V_{ID} = -200mV
Three State (high impedance) Output Current			±1	µA	0.4V ≤ V_O ≤ 2.4V; $\overline{REB}$ = 5V
Input Resistance	12	15		kΩ	-7V ≤ V_{CM} ≤ 12V
Input Current (A, B); V_{IN} = 12V			±1.0	mA	DE = 0V, V_{CC} = 0V or 5.25V, V_{IN} = 12V
Input Current (A, B); V_{IN} = -7V			-0.8	mA	DE = 0V, V_{CC} = 0V or 5.25V, V_{IN} = -7V
Short-Circuit Current	7		85	mA	0V ≤ V_O ≤ V_{CC}
SP491 RECEIVER					
DC Characteristics					
Receiver Data Rate			5	Mbps	$\overline{REB}$ = 0V, DE = 5V
Receiver Input to Output	60	90	150	ns	t_{PLH}; R_{DIFF} = 54Ω, C_{L1} = C_{L2} = 100pF; *Figures 3 & 8*
Receiver Input to Output	60	90	150	ns	t_{PHL}; R_{DIFF} = 54Ω, C_{L1} = C_{L2} = 100pF; *Figures 3 & 8*
Diff. Receiver Skew $\lvert t_{PLH}-t_{PHL}\rvert$		13		ns	R_{DIFF} = 54Ω; C_{L1} = C_{L2} = 100pF; *Figures 3 & 8*
Receiver Enable to Output Low		20	50	ns	C_{RL} = 15pF; *Figures 2 and 9;* S_1 closed
Receiver Enable to Output High		20	50	ns	C_{RL} = 15pF; *Figures 2 and 9;* S_2 closed
Receiver Disable from Low		20	50	ns	C_{RL} = 15pF; *Figures 2 and 9;* S_1 closed
Receiver Disable from High		20	50	ns	C_{RL} = 15pF; *Figures 2 and 9;* S_2 closed
POWER REQUIREMENTS					
Supply Voltage	+4.75		+5.25	Volts	
Supply Current		600		µA	$\overline{REB}$, D = 0V or V_{CC}; DE = V_{CC}
SP491 ENVIRONMENTAL AND MECHANICAL					
Operating Temperature					
Commercial (_C_)	0		+70	°C	
Industrial (_E_)	-40		+85	°C	
Storage Temperature	-65		+150	°C	
Package					
Plastic DIP (_S_)					
NSOIC (_N)					

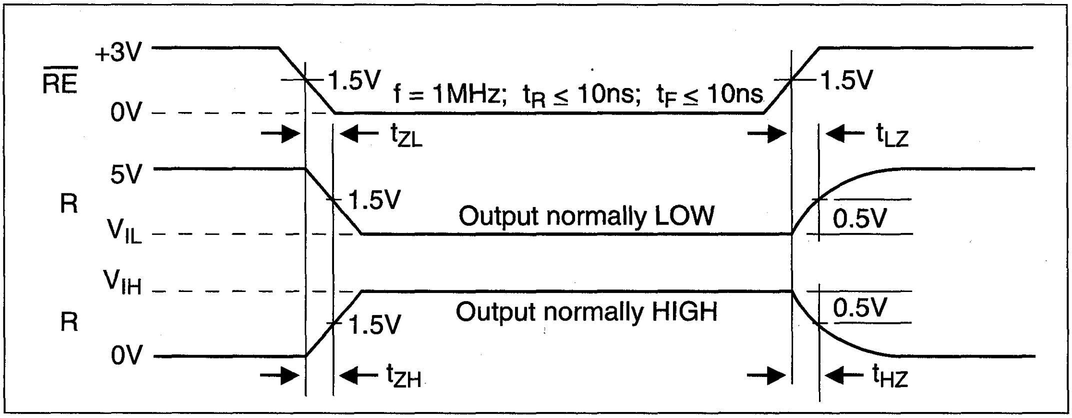


Figure 9. Receiver Enable and Disable Times

DESCRIPTION

The **SP490** and **SP491** are full-duplex differential transceivers that meet the requirements of RS-485 and RS-422. Fabricated with a **Sipex** proprietary BiCMOS process, both products require a fraction of the power of older bipolar designs.

The RS-485 standard is ideal for multi-drop applications or for long-distance interfaces. RS-485 allows up to 32 drivers and 32 receivers to be connected to a data bus, making it an ideal choice for multi-drop applications. Since the cabling can be as long as 4,000 feet, RS-485 transceivers are equipped with a wide (-7V to +12V) common mode range to accommodate ground potential differences. Because RS-485 is a differential interface, data is virtually immune to noise in the transmission line.

Driver...

The drivers for both the **SP490** and **SP491** have differential outputs. The typical voltage output swing with no load will be 0 volts to +5 volts. With worst case loading of 54Ω across the differential outputs, the driver can maintain greater than 1.5V voltage levels.

The driver of the **SP491** has a driver enable control line which is active high. A logic high on DE (pin 4) of the **SP491** will enable the differential driver outputs. A logic low on DE (pin 4) of the **SP491** will tri-state the driver outputs. The **SP490** does not have a driver enable.

Receiver...

The receivers for both the **SP490** and **SP491** have differential inputs with an input sensitivity as low as ±200mV. Input impedance of the receivers is typically 15KΩ (12KΩ minimum). A wide common mode range of -7V to +12V allows for large ground potential differences between systems. The receivers for both the **SP490** and **SP491** are equipped with the fail-safe feature. Fail-safe guarantees that the receiver output will be in a high state when the input is left unconnected.

The receiver of the **SP491** has a receiver enable control line which is active low. A logic low on REB (pin 3) of the SP491 will enable the differential receiver. A logic high on REB (pin 3) of the **SP491** will tri-state the receiver.

ORDERING INFORMATION

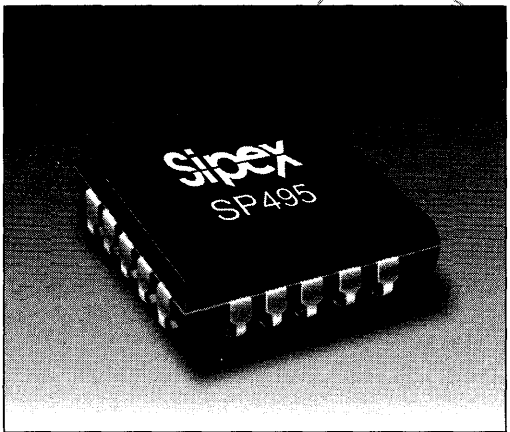
Model	Temperature Range	Package
SP490CN.	0°C to +70°C	8-Pin NSOIC
SP490CS	-40°C to +85°C	8-Pin DIP
SP491CN	0°C to +70°C	14-Pin NSOIC
SP491CS	-40°C to +85°C	14-Pin DIP

Sipex Corporation
SIGNAL PROCESSING EXCELLENCE

SP495

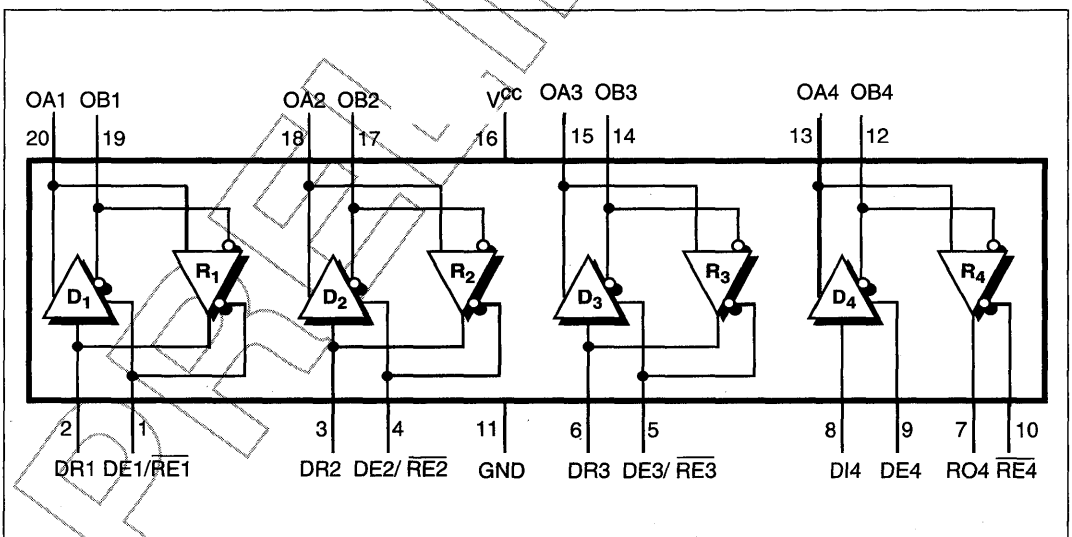
Quad Differential RS-485 Transceiver

- Pinout for SCSI Interface
- Meets EIA-485 Standard for Multipoint Bus Transmission
- +5V-Only Power Supply Required
- Receiver Fail-Safe Mode
- Low Power BiCMOS Technology
- Glitch-Free Power-Up/Down
- Available in 20-Pin Plastic LCC
- Pin Compatible with DS36954



DESCRIPTION...

The **SP495** is a quad differential line driver/receiver meeting both RS-485 and RS-422 standards at data rates beyond 10Mbps. The **SP495** features three half-duplex transceivers suitable for data bus connections and a fourth full-duplex transceiver with independent driver, receiver enables, ideal for use as a control bus transceiver. A complete SCSI initiator or target interface can be implemented using five **SP495s**. Propagation Delay Skew is tightly specified to aid in parallel interface designs. The **SP495** is available in a 20-pin plastic LCC package for operation over the commercial and industrial temperature ranges.



ABSOLUTE MAXIMUM RATINGS

These are stress ratings only and functional operation of the device at these ratings or any other above those indicated in the operation sections of the specifications below is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

V_{CC}	+12V
Input Voltages	
Logic	-0.5V to (V_{CC}+0.5V)
Drivers	-0.5V to (V_{CC}+0.5V)
Receivers	±15V
Output Voltages	
Logic	-0.5V to (V_{CC}+0.5V)
Drivers	±15V
Receivers	-0.5V to (V_{CC}+0.5V)
Storage Temperature	-65°C to +150°C
Power Dissipation	1000mW

SPECIFICATIONS

T_{MIN} to T_{MAX} and V_{CC} = 5V ± 5% unless otherwise noted.

PARAMETERS	MIN.	TYP.	MAX.	UNITS	CONDITIONS
DRIVER					
DC Characteristics					
Differential Output Voltage	GND		V_{CC}	Volts	Unloaded; R = ∞ ; *see figure 1*
Differential Output Voltage	2		V_{CC}	Volts	With Load; R = 50Ω; (RS422); *see figure 1*
Differential Output Voltage	1.5		V_{CC}	Volts	With Load; R = 27Ω; (RS485); *see figure 1*
Change in Magnitude of Driver Differential Output Voltage for Complimentary States			0.2	Volts	R = 27Ω or R = 50Ω; *see figure 1*
Driver Common-Mode Output Voltage			3	Volts	R = 27Ω or R = 50Ω; *see figure 1*
Input High Voltage	2.0			Volts	Applies to DRx, DEx/ $\overline{REx}$
Input Low Voltage			0.8	Volts	Applies to DRx, DEx/ $\overline{REx}$
Input Current			±10	µA	Applies to DRx, DEx/ $\overline{REx}$
Driver Short-Circuit Current					
V_{OUT} = HIGH	35		250	mA	$-7V \le V_O \le 12V$
V_{OUT} = LOW	35		250	mA	$-7V \le V_O \le 12V$
DRIVER					
AC Characteristics					
Driver Data Rate			10	Mbps	DEx/ $\overline{REx}$ = 5V
Driver Input to Output	20	30	60	ns	t_{PLH}; R_{DIFF} = 54Ω, $C_{L1} = C_{L2}$ = 100pF; *see figures 3 and 6*
Driver Input to Output	20	30	60	ns	t_{PHL}; R_{DIFF} = 54Ω, $C_{L1} = C_{L2}$ = 100pF; *see figures 3 and 6*
Driver Skew		10		ns	From output to output; *see figures 3 and 6*
Driver Rise or Fall Time	3	15	40	ns	From 10% to 90%; R_{DIFF} = 54Ω, $C_{L1} = C_{L2}$ = 100pF; *see figures 3 and 6*
Driver Enable to Output High		40	70	ns	$C_{L1} = C_{L2}$ = 100pF; *see figures 4 and 7;* S_2 closed
Driver Enable to Output Low		40	70	ns	$C_{L1} = C_{L2}$ = 100pF; *see figures 4 and 7;* S_1 closed
Driver Disable Time from Low		40	70	ns	$C_{L1} = C_{L2}$ = 15pF; *see figures 4 and 7;* S_1 closed
Driver Disable Time from High		40	70	ns	$C_{L1} = C_{L2}$ = 15pF; *see figures 4 and 7;* S_2 closed
RECEIVER					
DC Characteristics					
Differential Input Threshold	-0.2		+0.2	Volts	$-7V \le V_{CM} \le 12V$
Input Hysteresis		70		mV	V_{CM} = 0V
Output Voltage High	3.5			Volts	I_O = -4mA, V_{ID} = +200mV

SPECIFICATIONS (continued)

T_{MIN} to T_{MAX} and V_{CC} = 5V ± 5% unless otherwise noted.

PARAMETERS	MIN.	TYP.	MAX.	UNITS	CONDITIONS
RECEIVER DC Characteristics					
Output Voltage Low			0.4	Volts	I_O = +4mA, V_{ID} = -200mV
Three State (high impedance) Output Current		±1		µA	0.4V ≤ V_O ≤ 2.4V; DEx/ $\overline{REx}$ = 5V
Input Resistance	12	15		kΩ	-7V ≤ V_{CM} ≤ 12V
Input Current (A, B); V_{IN} = 12V			±1.0	mA	DE = 0V, V_{CC} = 0V or 5.25V, V_{IN} = 12V
Input Current (A, B); V_{IN} = -7V			-0.8	mA	DE = 0V, V_{CC} = 0V or 5.25V, V_{IN} = -7V
Short-Circuit Current	7		85	mA	0V ≤ V_O ≤ V_{CC}
RECEIVER AC Characteristics					
Receiver Data Rate			10	Mbps	DEx/ $\overline{REx}$ = 0V
Receiver Input to Output		60	150	ns	t_{PLH}; R_{DIFF} = 54Ω, C_{L1} = C_{L2} = 100pF; *Figures 3 & 8*
Receiver Input to Output		60	150	ns	t_{PHL}; R_{DIFF} = 54Ω, C_{L1} = C_{L2} = 100pF; *Figures 3 & 8*
Diff. Receiver Skew $\lvert t_{PLH}-t_{PHL}\rvert$		13		ns	R_{DIFF} = 54Ω; C_{L1} = C_{L2} = 100pF; *Figures 3 & 8*
Receiver Enable to Output Low		20	50	ns	C_{RL} = 15pF; *Figures 2 and 9;* S_1 closed
Receiver Enable to Output High		20	50	ns	C_{RL} = 15pF; *Figures 2 and 9;* S_2 closed
Receiver Disable from Low		20	50	ns	C_{RL} = 15pF; *Figures 2 and 9;* S_1 closed
Receiver Disable from High		20	50	ns	C_{RL} = 15pF; *Figures 2 and 9;* S_2 closed
POWER REQUIREMENTS					
Supply Voltage	+4.75		+5.25	Volts	
Supply Current		3		mA	DEx/ $\overline{REx}$, DRx = 0V or V_{CC}
ENVIRONMENTAL AND MECHANICAL					
Operating Temperature					
Commercial (_C_)	0		+70	°C	
Industrial (_E_)	-40		+85	°C	
Storage Temperature	-65		+150	°C	
Package					
Plastic LCC (_L)					

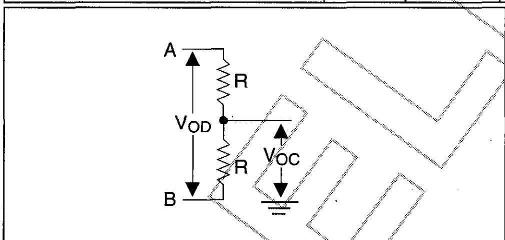


Figure 1. Driver DC Test Load Circuit

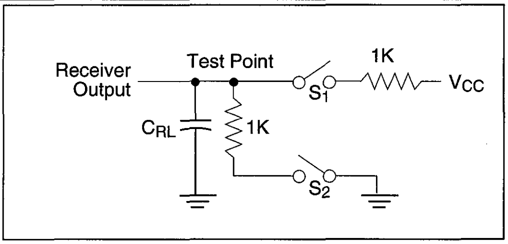


Figure 2. Receiver Timing Test Load Circuit

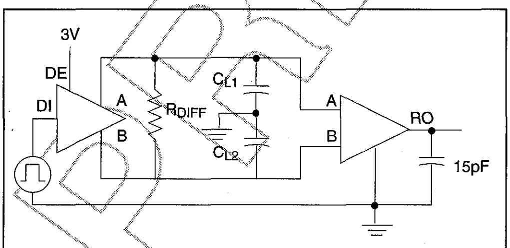


Figure 3. Driver/Receiver Timing Test Circuit

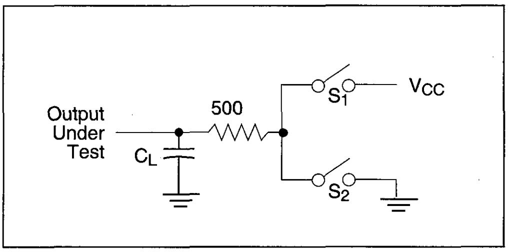


Figure 4. Driver Timing Test Load #2 Circuit

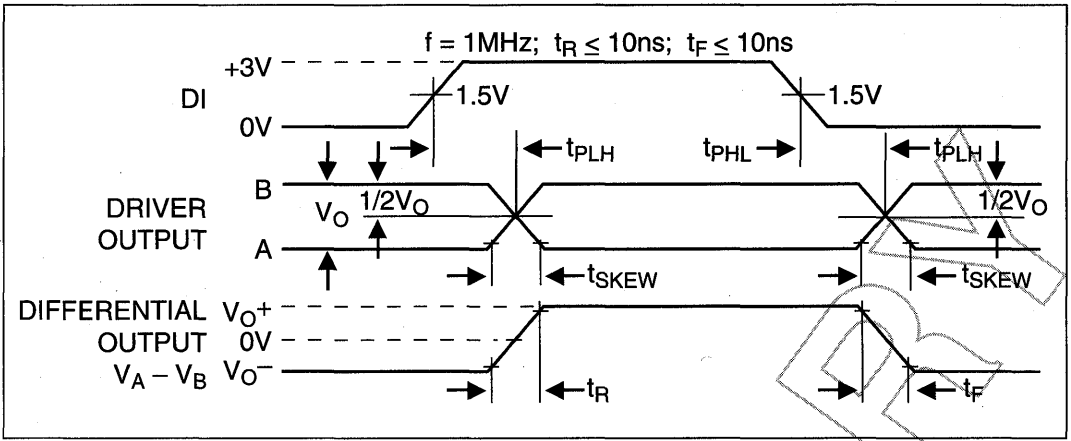


Figure 6. Driver Propagation Delays

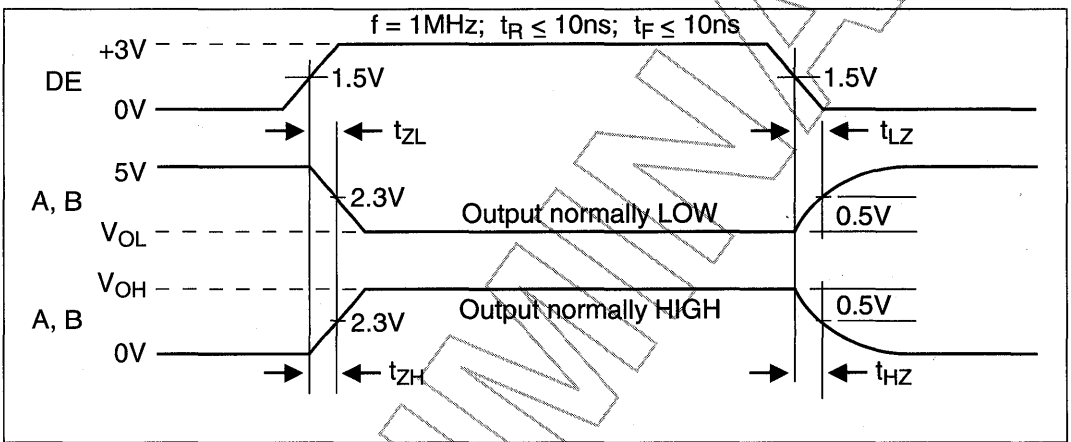


Figure 7. Driver Enable and Disable Times

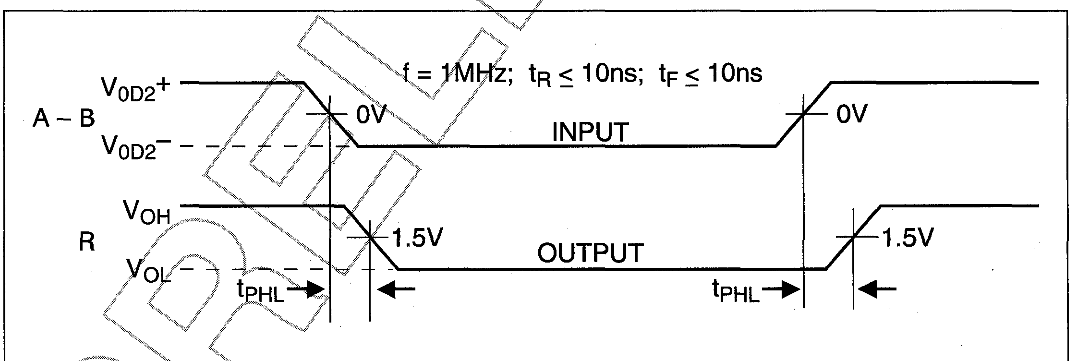


Figure 8. Receiver Propagation Delays

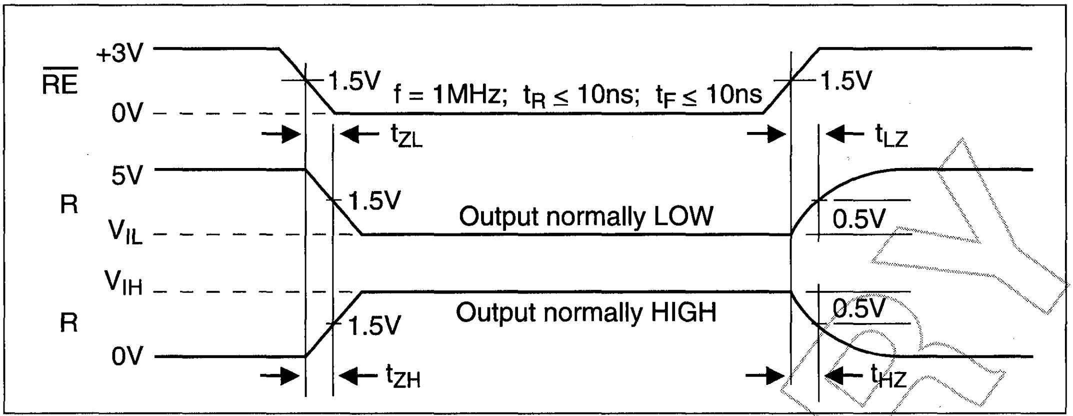


Figure 9. Receiver Enable and Disable Times

DESCRIPTION

General Description...

The **SP495** is a quad differential transceiver that meets the requirements of RS-485, RS-422, and differential SCSI at data rates beyond 10Mbps. Fabricated with a proprietary Sipex BiCMOS process, the **SP495** requires only a fraction of the power of older bipolar designs.

The **SP495** features three half-duplex transceivers suitable for data bus connections and a fourth full-duplex transceiver with independent enables ideal for use as a control bus transceiver. A complete SCSI initiator or target interface can be implemented using five **SP495**s.

The RS-485 standard is ideal for multi-drop applications and for long-distance interfaces. RS-485 allows up to 32 drivers and 32 receivers to be connected to a single data bus, making it an ideal choice for multi-drop applications. Since the cabling can be as long as 4,000 feet, RS-485 transceivers are specified for operation with a wide (-7V to +12V) common mode range to accommodate ground potential differences. Because RS-485 is a low impedance differential interface, data is virtually immune to noise in the transmission line.

Drivers...

The differential drivers for the **SP495** have typical output voltage swings (no load) of 0 to +5Volts. With loading to the RS-485 specification (54Ω), drivers must maintain outputs greater than 1.5V.

The three half-duplex drivers of the **SP495** have independent Driver Enable control lines which are active HIGH. A logic HIGH on DEx (pins 1, 4, or 5 of the **SP495**) will enable the addressed differential driver output. A logic LOW on DEx will tri-state the driver output and enable the receiver. The fourth driver is controlled by its own DE4 Enable line and can be used in half - duplex or full-duplex modes.

Receivers...

The differential receivers for the **SP495** have an input sensitivity of ±200mV. Input impedance is typically 15kΩ (12kΩ minimum). A wide common mode range of -7V to +12V allows for large ground potential differences between widely separated systems. These receivers are equipped with a fail-safe feature which guarantees that the receiver output will be in a HIGH state when the input is left unconnected (note: this feature operates with floating inputs, not terminated inputs).

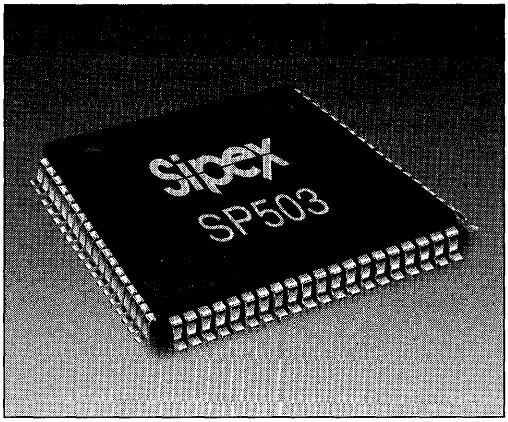
Like the half-duplex drivers, the three half-duplex receivers of the **SP495** have independent Receiver Enable control lines which are active LOW. A logic LOW on $\overline{REx}$ (pins 1, 4, or 5 of the SP495) enables the differential receivers. A logic HIGH on $\overline{REx}$ tri-states the receivers. The fourth receiver is controlled by its own RE4 Enable line and can be used in half -duplex or full-duplex modes.

ORDERING INFORMATION

Model	Temperature Range	Package
SP495CL	0°C to +70°C	20-Pin PLCC
SP495EL	-40°C to +85°C	20-Pin PLCC

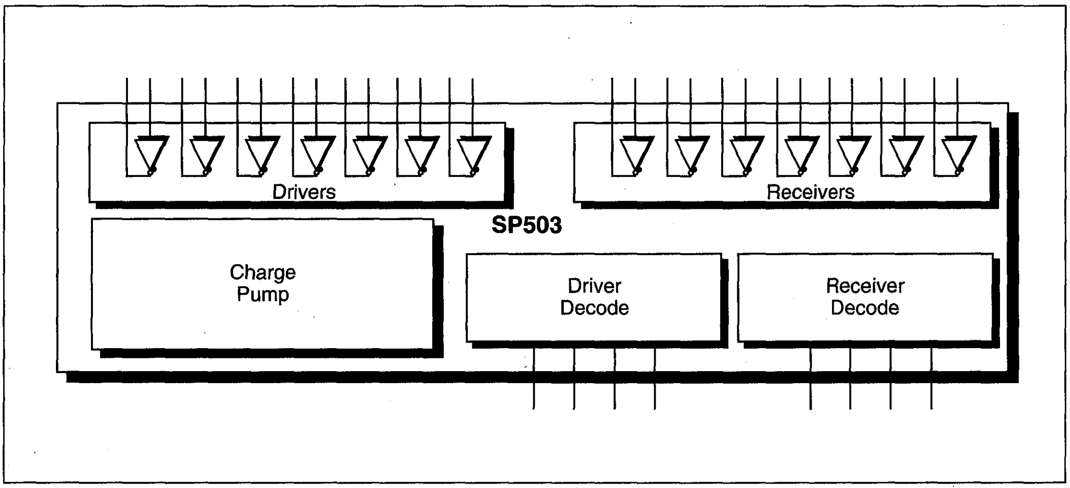
Multi–Mode Serial Transceiver

- Single-Chip Serial Transceiver Supports Industry-Standard
- Software-Selectable Protocols:
  - — RS-232 (V.28)
  - — RS-422A (V.11, X.27)
  - — RS-449
  - — RS-485
  - — V.35
  - — EIA-530
- Programmable Selection of Interface
- Seven (7) Drivers and Seven (7) Receivers
- Surface Mount Packaging



DESCRIPTION...

The **SP503** is a highly integrated serial transceiver that allows software control of its interface modes. It offers hardware interface modes for RS-232 (V.28), RS-422A (V.11), RS-449, RS485, V.35, and EIA-530. The **SP503** is fabricated using low–power BiCMOS process technology, and incorporates a **Sipex**–patented (5,306,954) charge pump allowing +5V only operation. Each device is packaged in an 80–pin Quad FlatPack package.



SPECIFICATIONS

T_{MIN} to T_{MAX} @ Vcc = +5V ±5% unless otherwise noted.

	MIN.	TYP.	MAX.	UNITS	CONDITIONS
LOGIC INPUTS					
V_{IL}			0.8	Volts	
V_{IH}	2.0			Volts	
LOGIC OUTPUTS					
V_{OL}			0.4	Volts	I_{OUT}= 3.2mA
V_{OH}	2.4			Volts	I_{OUT}= 1.0mA
RS-485 DRIVER					
TTL Input Levels					
V_{IL}			0.8	Volts	
V_{IH}	2.0			Volts	
Outputs					
High Level Output			+6.0	Volts	
Low level Output	–0.3			Volts	
Differential Output	±1.5		±5.0	Volts	R_L=54Ω, C_L=50pF
Balance			±0.2	Volts	$\|V_T\| - \|V_T\|$
Open Circuit Voltage			±6.0	Volts	
Output Current	28.0			mA	R_L=54Ω
Short Circuit Current			±250	mA	Terminated in –7V to +12V
Transition Time			120	ns	Rise/fall time, 10%–90%
Transmission Rate			5	Mbps	
Propagation Delay					
t_{PHL}			200	ns	R_L=54Ω
t_{PLH}			200	ns	R_L=54Ω
RS-485 RECEIVER					
TTL Output Levels					
V_{OL}	0		0.4	Volts	
V_{OH}	2.4			Volts	
Input					
High Threshold	+0.2		+12.0	Volts	(a)-(b)
Low Threshold	–7.0		–0.2	Volts	(a)-(b)
Common Mode Range	–7.0		+12.0	Volts	
High Input Current					Refer to graph
Low Input Current					Refer to graph
Receiver Sensitivity			±0.2	Volts	Over –7V to +12V common mode range
Input Impedance	12			KΩ	
Transmission Rate			5	Mbps	
Propagation Delay					
t_{PHL}			200	ns	
t_{PLH}			200	ns	
V.35 DRIVER					
TTL Input Levels					
V_{IL}	0		0.8	Volts	
V_{IH}	2.0			Volts	
Outputs					
Differential Output	±0.44		±0.66	Volts	With termination network in Figure 6; R_L=100Ω
Output Impedance	50		150	Ω	With termination network in Figure 6.
Transition Time			40	ns	
Transmission Rate			5	Mbps	
Propagation Delay					
t_{PHL}			200	ns	R_L=100Ω
t_{PLH}			200	ns	R_L=100Ω

SPECIFICATIONS (Continued)

T_{MIN} to T_{MAX} @ Vcc = +5V ±5% unless otherwise noted.

	MIN.	TYP.	MAX.	UNITS	CONDITIONS
V.35 RECEIVER					
TTL Output Levels					
V_{OL}	0		0.4	Volts	
V_{OH}	2.4			Volts	
Input					
High Threshold	+0.2		+12.0	Volts	(a)-(b)
Low Threshold	–7.0		–0.2	Volts	(a)-(b)
Common Mode Range	–7.0		+12.0	Volts	
Receiver Sensitivity			±0.2	Volts	
Input Impedance	90		110	Ω	With termination network in Figure 6.
Transmission Rate			5	Mbps	
Propagation Delay					
t_{PHL}			200	ns	
t_{PLH}			200	ns	
RS-422 DRIVER					
TTL Input Levels					
V_{IL}	0		0.8	Volts	
V_{IH}	2.0			Volts	
Outputs					
Differential Output	±2.0		±5.0	Volts	R_L=100Ω
Open Circuit Voltage, V_O			±6.0	Volts	
Balance			±0.4	Volts	$\|V_T\| - \|\overline{V_T}\|$
Offset			+3.0	Volts	
Short Circuit Current			±150	mA	$-7V \leq V_{out} \leq +12V$
Power Off Current			±100	µA	V_{cc} = 0V, V_{out} = ±0.25V
Transition Time			60	ns	Rise/fall time, 10%-90%
Transmission Rate			5	Mbps	
Propagation Delay					
t_{PHL}			200	ns	R_L=100Ω
t_{PLH}			200	ns	R_L=100Ω
RS-422 RECEIVER					
TTL Output Levels					
V_{OL}	0		0.4	Volts	
V_{OH}	2.4			Volts	
Input					
High Threshold	+0.2		+6.0	Volts	(a)-(b)
Low Threshold	–6.0		–0.2	Volts	(a)-(b)
Common Mode Range	–7.0		+7.0	Volts	
High Input Current					Refer to graph
Low Input Current					Refer to graph
Receiver Sensitivity			±0.2	Volts	
Input Impedance	4			KΩ	
Transmission Rate			5	Mbps	
Propagation Delay					
t_{PHL}			200	ns	
t_{PLH}			200	ns	
RS-232 DRIVER					
TTL Input Level					
V_{IL}	0		0.8	Volts	
V_{IH}	2.0			Volts	
Outputs					
High Level Output	+5.0		+15	Volts	R_L=3KΩ, V_{IN}=0.8V, V_{cc} = 5V
Low Level Output	–15.0		–5.0	Volts	R_L=3KΩ, V_{IN}=2.0V, V_{cc} = 5V
Open Circuit Voltage	–15		+15	Volts	
Short Circuit Current			±100	mA	
Power Off Impedance	300			Ω	V_{cc} = 0V, V_{out} = ±2.0V

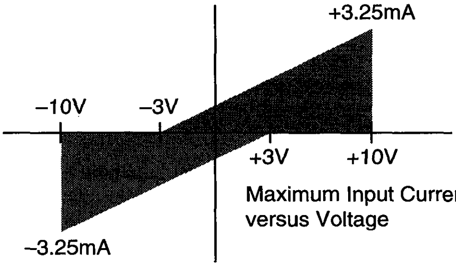
SPECIFICATIONS (Continued)

T_{MIN} to T_{MAX} @ Vcc = +5V ±5% unless otherwise noted.

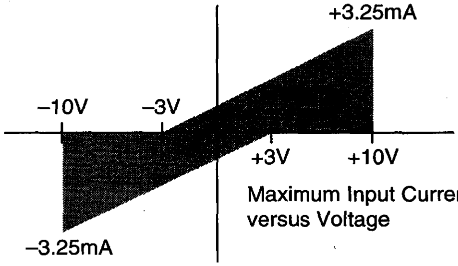
	MIN.	TYP.	MAX.	UNITS	CONDITIONS
Slew Rate			30	V/µs	R_L=3KΩ, C_L=15pF
Transition Time			1.56	µs	R_L=3KΩ, C_L=2500pF
Transmission Rate			120	Kbps	
Propagation Delay					
t_{PHL}		2	8	µS	R_L=3KΩ
t_{PLH}		2	8	µS	R_L=3KΩ
RS-232 RECEIVER					
TTL Output Levels					
V_{OL}	0		0.4	Volts	
V_{OH}	2.4			Volts	
Input					
High Threshold		1.7	2.4	Volts	
Low Threshold	0.8	1.2		Volts	
Receiver Open Circuit Bias	0		+2.0	Volts	
Input Impedance	3	5	7	KΩ	
Transmission Rate			120	Kbps	
Propagation Delay					
t_{PHL}			1	µS	
t_{PLH}			1	µS	
RS-423 DRIVER					
TTL Input Levels					
V_{IL}	0		0.8	Volts	
V_{IH}	2.0			Volts	
Output					
High Level Output	+3.6		+6.0	Volts	R_L=450Ω
Low Level Output	–6.0		–3.6	Volts	R_L=450Ω
Open Circuit Voltage	±4.0		±10.0	Volts	
Short Circuit Current			±150	mA	
Power Off Current			±100	µA	V_{cc} = 0V, V_{out} = ±0.25V
Transition Time	0.8		2.4	µs	Rise/fall time, 10-90%
Transmission Rate			120	Kbps	
Propagation Delay					
t_{PHL}		2	8	µS	R_L=450Ω
t_{PLH}		2	8	µS	R_L=450Ω
RS-423 RECEIVER					
TTL Output Levels					
V_{OL}	0		0.4	Volts	
V_{OH}	2.4			Volts	
Input					
High Threshold	+0.2		+7.0	Volts	
Low Threshold	–7.0		–0.2	Volts	
Common Mode Range	–7.0		+7.0	Volts	
High Input Current					Refer to graph
Low Input Current					Refer to graph
Receiver Sensitivity			±0.2	Volts	V_{CM} = +7V to -7V
Input Impedance	4			KΩ	V_{IN} = +10V to -10V
Transmission Rate			120	Kbps	
Propagation Delay					
t_{PHL}			1	µS	
t_{PLH}			1	µS	
POWER REQUIREMENTS					
V_{CC}	4.75		5.25	Volts	
I_{CC}		20	30	mA	V_{CC}=5V; no interface selected
ENVIRONMENTAL AND MECHANICAL					
Operating Temperature Range	0		+70	°C	
Storage Temperature Range	–65		+150	°C	
Package		80–pin QFP			

RECEIVER INPUT GRAPHS

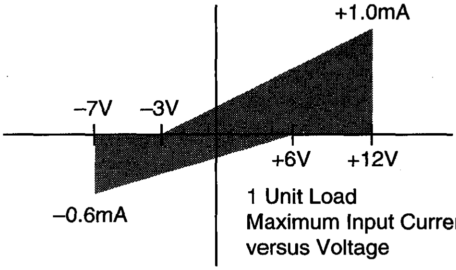
RS-422 RECEIVER



RS-423 RECEIVER



RS-485 RECEIVER



POWER MATRIX

Typical @ 25°C and V_{cc} = +5V unless otherwise noted. Input is applied to one driver.

Mode	Open Input	Input to 5V	Input to GND	AC signal to Input	Input to 5V with load	Input to GND with load	AC Signal with load	Conditions
V.35	47.0mA	48.8mA	47.3mA	54.5mA	104.2mA	100.9mA	100.9mA	With external termination resistor network; Input @ 60kHz, Load is 3kΩ & 2500pF for RS-232 and 100Ω for V.35
RS-232	35.4mA	37.8mA	35.2mA	43.6mA	54.1mA	57.1mA	55.9mA	Input @ 60kHz Load is 3kΩ & 2500pF for RS-232.
RS-422	25.8mA	31.4mA	25.8mA	27.5mA	140.2mA	135.9mA	145.2mA	Input @ 2.5MHz Load is 100Ω.
RS-485	33.4mA	37.91mA	33.51mA	34.81mA	200.3mA	194.8mA	203.3mA	Input @ 2.5MHz Load is 54Ω.
RS-449	37.8mA	40.3mA	41.1mA	42.9mA	142.3mA	138.8mA	147.4mA	Input @ 60kHz Load is 100Ω for RS-422 450Ω for RS-423
EIA-530	45.2mA	48.1mA	44.4mA	50.3mA	148.9mA	145.7mA	147.3mA	Input @ 60kHz Load is 100Ω for RS-422 450Ω for RS-423

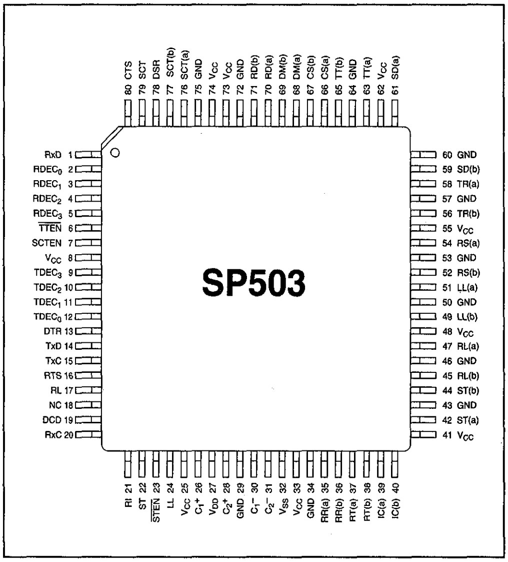
OTHER AC CHARACTERISTICS

(Typical @ 25°C and nominal supply voltages unless otherwise noted)

PARAMETER	MIN.	TYP.	MAX.	UNITS	CONDITIONS
DELAY TIME FROM ENABLE MODE TO TRI–STATE MODE					
SINGLE–ENDED MODE (RS-232, RS-423)					
t_{PZL}; Enable to Output low		190		ns	3KΩ pull–up to output
t_{PZH}; Enable to Output high		130		ns	3KΩ pull–down to output
t_{PLZ}; Disable from Output low		270		ns	5V to input
t_{PHZ}; Disable from Output high		400		ns	GND to input
DIFFERENTIAL MODE (RS-422, RS-485, V.35)					
t_{PZL}; Enable to Output low		100		ns	3KΩ pull–up to output
t_{PZH}; Enable to Output high		100		ns	3KΩ pull–down to output
t_{PLZ}; Disable from Output low		130		ns	5V to input
t_{PHZ}; Disable from Output high		140		ns	GND to input

Notes:
1. Measured from 2.5V of R_{IN} to 2.5V of R_{OUT}.
2. Measured from one–half of R_{IN} to 2.5V of R_{OUT}.
3. Measured from 1.5V of T_{IN} to one–half of T_{OUT}.
4. Measured from 2.5V of R_O to 0V of A and B.

PINOUT...



PIN ASSIGNMENTS...
CLOCK AND DATA GROUP

Pin 1 — RxD — Receive Data; TTL output, sourced from RD(a) and RD(b) inputs.

Pin 14 — TxD — TTL input ; transmit data source for SD(a) and SD(b) outputs.

Pin 15 — TxC — Transmit Clock; TTL input for TT driver outputs.

Pin 20 — RxC — Receive Clock; TTL output sourced from RT(a) and RT(b) inputs.

Pin 22 — ST — Send Timing; TTL input; source for ST(a) and ST(b) outputs.

Pin 37 — RT(a) — Receive Timing; analog input, inverted; source for RxC.

Pin 38 — RT(b) — Receive Timing; analog input, non-inverted; source for RxC.

Pin 42 — ST(a) — Send Timing; analog output, inverted; sourced from ST.

Pin 44 — ST(b) — Send Timing; analog output, non-inverted; sourced from ST.

Pin 59 — SD(b) — Analog Out — Send data, non-inverted; sourced from TxD.

Pin 61 — SD(a) — Analog Out — Send data, inverted; sourced from TxD.

Pin 63 — TT(a) — Analog Out — Terminal Timing, inverted; sourced from TxC

Pin 65 — TT(b) — Analog Out — Terminal Timing, non–inverted; sourced from TxC.

Pin 70 — RD(a) — Receive Data, analog input; inverted; source for RxD.

Pin 71 — RD(b) — Receive Data; analog input; non-inverted; source for RxD.

Pin 76 — SCT(a) — Serial Clock Transmit; analog input, inverted; source for SCT.

Pin 77 — SCT(b) — Serial Clock Transmit: analog input, non–inverted; source for SCT

Pin 79 — SCT — Serial Clock Transmit; TTL output; sources from SCT(a) and SCT(b) inputs.

CONTROL LINE GROUP

Pin 13 — DTR — Data Terminal Ready; TTL input; source for TR(a) and TR(b) outputs.

Pin 16 — RTS — Ready To Send; TTL input; source for RS(a) and RS(b) outputs.

Pin 17 — RL — Remote Loopback; TTL input; source for RL(a) and RL(b) outputs.

Pin 19 — DCD— Data Carrier Detect; TTL output; sourced from RR(a) and RR(b) inputs.

Pin 21 — RI — Ring In; TTL output; sourced from IC(a) and IC(b) inputs.

Pin 24 — LL — Local Loopback; TTL input; source for LL(a) and LL(b) outputs.

Pin 35 — RR(a)— Receiver Ready; analog input, inverted; source for DCD.

Pin 36 — RR(b)— Receiver Ready; analog input, non-inverted; source for DCD.

Pin 39 — IC(a)— Incoming Call; analog input, inverted; source for RI.

Pin 40 — IC(b)— Incoming Call; analog input, non-inverted; source for RI.

Pin 45 — RL(b) — Remote Loopback; analog output, non-inverted; sourced from RL.

Pin 47 — RL(a) — Remote Loopback; analog output inverted; sourced from RL.

Pin 49— LL(b) — Local Loopback; analog output, non-inverted; sourced from LL.

Pin 51 — LL(a) — Local Loopback; analog output, inverted; sourced from LL.

Pin 52 — RS(b) — Ready To Send; analog output, non-inverted; sourced from RTS.

Pin 54 — RS(a) — Ready To Send; analog output, inverted; sourced from RTS.

Pin 56 — TR(b) — Terminal Ready; analog output, non-inverted; sourced from DTR.

Pin 58 — TR(a) — Terminal Ready; analog output, inverted; sourced from DTR.

Pin 66 — CS(a)— Clear To Send; analog input, inverted; source for CTS.

Pin 67 — CS(b)— Clear To Send; analog input, non-inverted; source for CTS.

Pin 68 — DM(a)— Data Mode; analog input, inverted; source for DSR.

Pin 69 — DM(b)— Data Mode; analog input, non-inverted; source for DSR

Pin 78 — DSR— Data Set Ready; TTL output; sourced from DM(a), DM(b) inputs.

Pin 80 — CTS— Clear To Send; TTL output; sourced from CS(a) and CS(b) inputs.

CONTROL REGISTERS

Pins 2–5 — $RDEC_0$ – $RDEC_3$ — Receiver decode register; configures receiver modes; TTL inputs.

Pin 6 — $\overline{TTEN}$ — Enables TT driver, active low; TTL input.

Pin 7 — SCTEN — Enables SCT receiver; active high; TTL input.

Pins 12–9 — $TDEC_0$ – $TDEC_3$ — Transmitter decode register; configures transmitter modes; TTL inputs.

Pin 23 — $\overline{STEN}$ — Enables ST driver; active low; TTL input.

POWER SUPPLIES

Pins 8, 25, 33, 41, 48, 55, 62, 73, 74 — V_{CC} — +5V input.

Pins 29, 34, 43, 46, 50, 53, 57, 60, 64, 72, 75 — GND — Ground.

Pin 27 — V_{DD} +10V Charge Pump Capacitor — Connects from V_{DD} to V_{CC}. Suggested capacitor size is 22μF, 16V.

Pin 32 — V_{SS} –10V Charge Pump Capacitor — Connects from ground to V_{SS}. Suggested capacitor size is 22µF, 16V.

Pins 26 and 30 — C_1^+ and C_1^- — Charge Pump Capacitor — Connects from C_1^+ to C_1^-. Suggested capacitor size is 22µF, 16V.

Pins 28 and 31 — C_2^+ and C_2^- — Charge Pump Capacitor — Connects from C_2^+ to C_2^-. Suggested capacitor size is 22µF, 16V.

NOTE: NC pins should be left floating; internal signals may be present.

FEATURES...

The **SP503** is a highly integrated serial transceiver that allows software control of its interface modes. The **SP503** offers hardware interface modes for RS-232 (V.28), RS-422A (V.11), RS-449, RS-485, V.35, and EIA-530. The interface mode selection is done via an 8–bit switch; four (4) bits control the drivers and four (4) bits control the receivers. The **SP503** is fabricated using low–power BiCMOS process technology, and incorporates a **Sipex**–patented (5,306,954) charge pump allowing +5V only operation. Each device is packaged in an 80–pin Quad FlatPack package.

The **SP503** is ideally suited for wide area network connectivity based on the interface modes offered and the driver and receiver configurations. The **SP503** has seven (7) independent drivers and seven (7) independent receivers. The seventh driver of the **SP503** allows it to support applications which require two separate clock outputs making it ideal for DCE applications.

THEORY OF OPERATION

The **SP503** is made up of four separate circuit blocks — the charge pump, drivers, receivers, and decoder. Each of these circuit blocks is described in more detail below.

Charge–Pump

The charge pump is a **Sipex**–patented design (5,306,954) and uses a unique approach compared to older less–efficient designs. The charge pump still requires four external capacitors, but uses a four–phase voltage shifting technique to attain symmetrical 10V power supplies. Figure 3(a) shows the waveform found on the positive side of capcitor C2, and figure 3(b) shows the negative side of capcitor C2. There is a free–running oscillator that controls the four phases of the voltage shifting. A description of each phase follows.

Phase 1

— V_{SS} charge storage —During this phase of the clock cycle, the positive side of capacitors C_1 and C_2 are initially charged to +5V. C_1^+ is then switched to ground and charge on C_1^- is transferred to C_2^-. Since C_2^+ is connected to +5V, the voltage potential across capacitor C_2 is now 10V.

Phase 2

— V_{SS} transfer — Phase two of the clock connects the negative terminal of C_2 to the V_{SS} storage capacitor and the positive terminal of C_2 to ground, and transfers the generated –l0V to C_3. Simultaneously, the positive side of capacitor C_1 is switched to +5V and the negative side is connected to ground.

Phase 3

— V_{DD} charge storage — The third phase of the clock is identical to the first phase — the charge transferred in C_1 produces –5V in the negative terminal of C_1, which is applied to the negative side of capacitor C_2. Since C_2^+ is at +5V, the voltage potential across C_2 is l0V.

Phase 4

— V_{DD} transfer — The fourth phase of the clock connects the negative terminal of C_2 to ground and transfers the generated l0V across C_2 to C_4, the V_{DD} storage capacitor. Again,

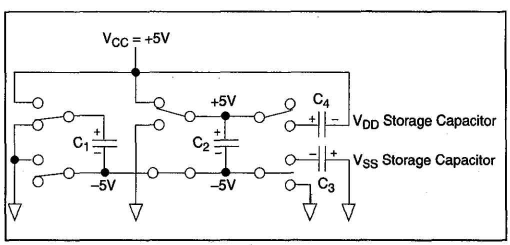


Figure 1. Charge Pump Phase 1.

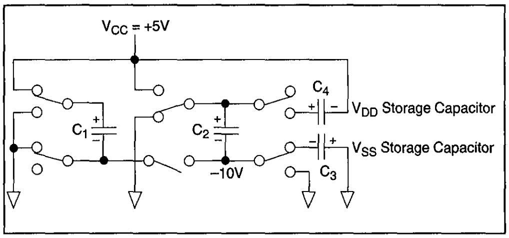


Figure 2. Charge Pump Phase 2.

simultaneously with this, the positive side of capacitor C_1 is switched to +5V and the negative side is connected to ground, and the cycle begins again.

Since both V+ and V^- are separately generated from V_{CC} in a no–load condition, V+ and V^- will be symmetrical. Older charge pump approaches that generate V^- from V+ will show a decrease in the magnitude of V^- compared to V+ due to the inherent inefficiencies in the design.

The clock rate for the charge pump typically operates at 15kHz. The external capacitors must be 22µF with a 16V breakdown rating.

External Power Supplies

For applications that do not require +5V only, external supplies can be applied at the V+ and V^- pins. The value of the external supply voltages must be no greater than ±l0V. The current drain for the ±10V supplies is used for RS232, and RS-423 drivers. For the RS-232 driver the current requirement will be 3.5mA per driver, and for the RS-423 driver the worst case current drain will be 11mA per driver. The external power supplies should provide a power supply sequence of :+l0V, then +5V, followed by –l0V.

Drivers

The **SP503** has seven (7) independent drivers, two of which have separate active–low tri–state controls. If a half-duplex channel is required, this can be achieved with external connections.

Control for the mode selection is done via a four–bit control word. The **SP503** does not have a latch; the control word must be externally latched either high or low to write the appropriate code into the **SP503**. The drivers are prearranged such that for each mode of operation the relative position and functionality of the drivers are set up to accommodate the selected interface mode. As the mode of the drivers is changed, the electrical characteristics will change to support the requirements of clock, data, and control line signal levels. *Table 1* shows a summary of the electrical characteristics of the drivers in the different interface modes. Unused driver inputs can be left floating; however, to ensure a desired state with no input signal, pull–up resistors to +5V or pull–down resistors to ground are suggested. Since the driver inputs are both TTL or CMOS compatible, any value resistor less than 100KΩ will suffice.

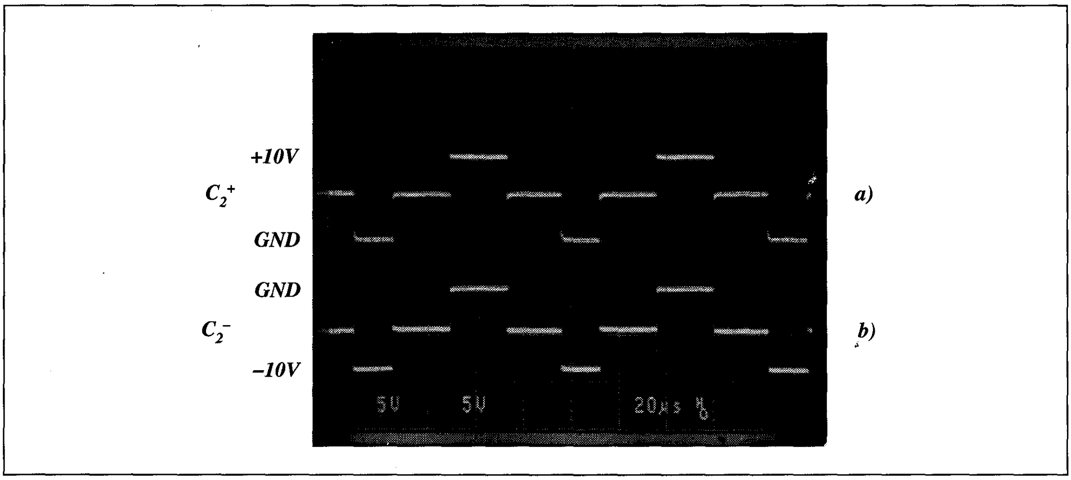


Figure 3. Charge Pump Waveforms

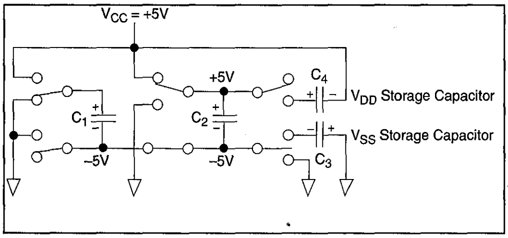


Figure 4. Charge Pump Phase 3.

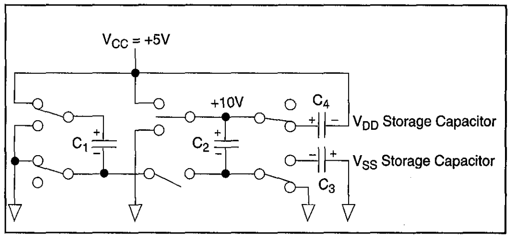


Figure 5. Charge Pump Phase 4.

There are three basic types of driver circuits — RS-232, RS-423, and RS-485. The RS-232 drivers output a minimum of ±5V level single–ended signals (with 3KΩ and 2500pF loading), and can operate up to 120Kbps. The RS232 drivers are used in RS232 mode for all signals, and also in V.35 mode where they are used as the control line signals.

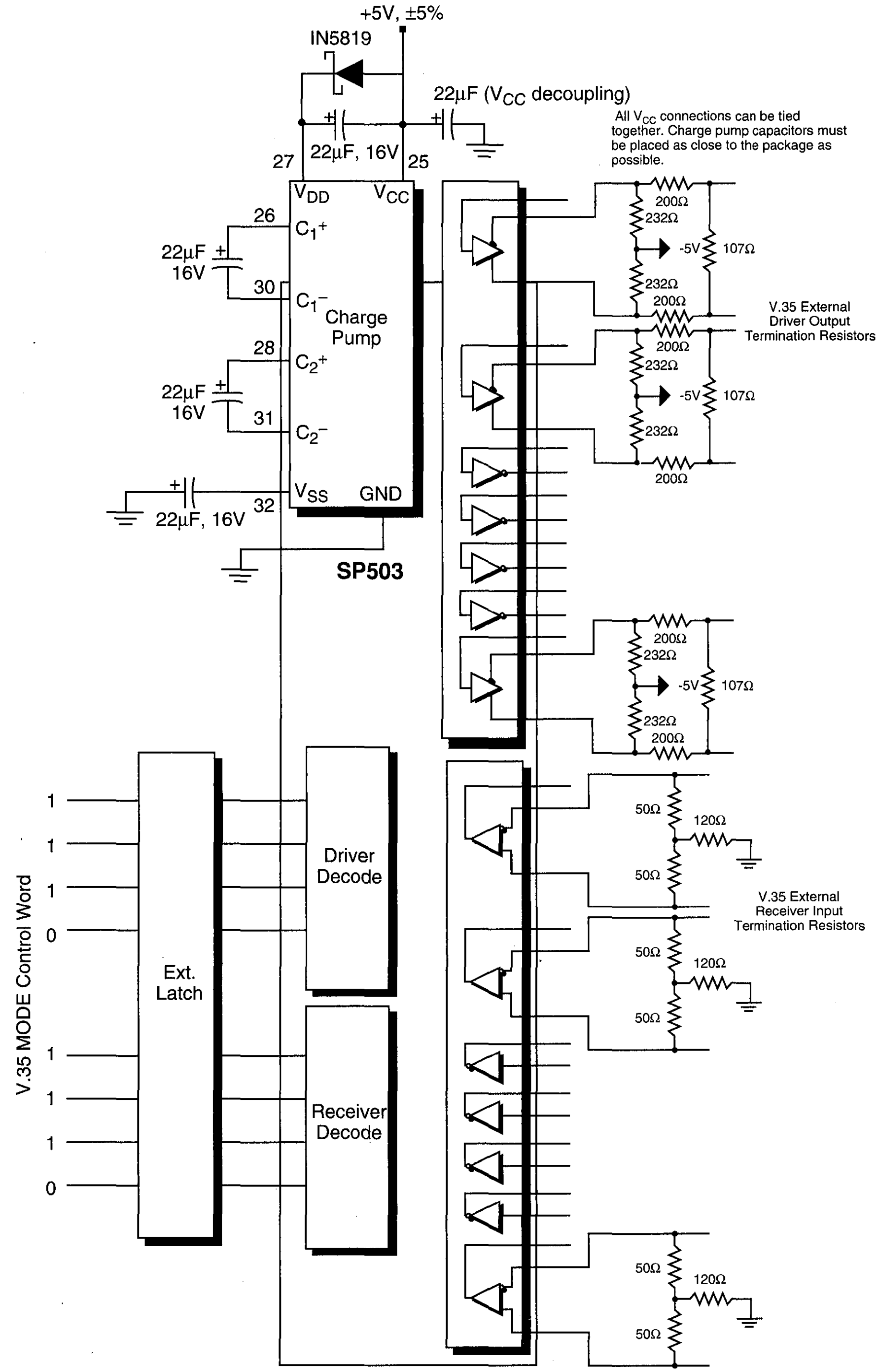
The RS-423 drivers output a minimum of ±3.6V level single–ended signals (with 450Ω loading) and can operate up to 120Kbps. Open circuit V_{OL} and V_{OH} measurements may exceed the ±6V limitation of RS-423. The RS-423 drivers are used in RS-449 and EIA-530 modes as RL and LL outputs.

The third type of driver supports RS-485, which is a differential signal that can maintain ±1.5V differential output levels with a worst case load of 54Ω. The signal levels and drive capability of the RS-485 drivers allow the drivers to also support RS-422 requirements of ±2V differential output levels with 100Ω loads. The RS-422 drivers are used in RS-449 and EIA-530 modes as clock, data, and some control line signals.

The RS-485–type drivers are also used in the V.35 mode. V.35 levels require ±0.55V signals with a load of 100Ω. In order to meet the voltage requirements of V.35, external series resistors with source impedance termination resistors must be implemented to voltage divide the driver outputs from 0 to +5V to 0 to +0.55V. *Figure 6* shows the values of the resistor network and how to connect them. The termination network also achieves the 50Ω to 150Ω source impedance for V.35. For applications that require V.11 signals for clock and data instead of V.35 levels, omit the external termination networks. All of the differential drivers, RS-485, RS-422, and V.35 can operate up to 5Mbps.

Pin Label	Mode:	RS-232	V.35	RS-422	RS-485	RS-449	EIA-530
$TDEC_3$–$TDEC_0$	0000	0010	1110	0100	0101	1100	1101
SD(a)	tri–state	RS-232	V.35–	RS-422–	RS-485–	RS-422–	RS-422–
SD(b)	tri–state	tri–state	V.35+	RS-422+	RS-485+	RS-422+	RS-422+
TR(a)	tri–state	RS-232	RS-232	RS-422–	RS-485–	RS-422–	RS-422–
TR(b)	tri–state	tri–state	tri–state	RS-422+	RS-485+	RS-422+	RS-422+
RS(a)	tri–state	RS-232	RS-232	RS-422–	RS-485–	RS-422–	RS-422–
RS(b)	tri–state	tri–state	tri–state	RS-422+	RS-485+	RS-422+	RS-422+
RL(a)	tri–state	RS-232	RS-232	RS-422–	RS-485–	RS-423	RS-423
RL(b)	tri–state	tri–state	tri–state	RS-422+	RS-485+	tri–state	tri–state
LL(a)	tri–state	RS-232	RS-232	RS-422–	RS-485–	RS-423	RS-423
LL(b)	tri–state	tri–state	tri–state	RS-422+	RS-485+	tri–state	tri–state
ST(a)	tri–state	RS-232	V.35–	RS-422–	RS-485–	RS-422–	RS-422–
ST(b)	tri–state	tri–state	V.35+	RS-422+	RS-485+	RS-422+	RS-422+
TT(a)	tri–state	RS-232	V.35–	RS-422–	RS-485–	RS-422–	RS-422–
TT(b)	tri–state	tri–state	V.35+	RS-422+	RS-485+	RS-422+	RS-422+

Table 1. SP503 Drivers



Note: An external voltage of -5V, ±5% is needed for the driver output termination resistors. These V.35 termination resistors comply with all the parameters specified in CCITT Recommendation V.35. For other termination configurations, please consult factory.

Figure 6. Typical Operating Circuit

Receivers

The **SP503** has seven (7) independent receivers which can be programmed for six (6) different interface modes. One of the seven (7) receivers (SCT) has an active–high enable control, as shown in the Mode Diagrams.

Control for the mode selection is done via a 4–bit control word that is independent from the driver control word. The coding for the drivers and receivers is identical. Therefore, if the modes for the drivers and receivers are supposed to be identical in the application, the control lines can be tied together.

Like the drivers, the receivers are pre-arranged for the specific requirements of the interface. As the operating mode of the receivers is changed, the electrical characteristics will change to support the requirements of clock, data, and control line receivers. *Table 2* shows a summary of the electrical characteristics of the receivers in the different interface modes. Unused receiver inputs can be left floating without causing oscillation. To ensure a desired state of the receiver output, a pull–up resistor of 100KΩ to +5V should be connected to the inverting input for a logic low, or the non–inverting input for a logic high. For single-ended receivers, a pull–down resistor to ground of 5KΩ is internally connected, which will ensure a logic high output.

There are three basic types of receivers — RS-232, RS-423, and RS-485. The RS-232 receiver is a single–ended input with a threshold of 0.8V to 2.4V. The RS-232 receiver has an operating voltage range of ±15V and can receive signals up to 120Kbps. RS-232 receivers are used in RS-232 mode for all signal types, and in V.35 mode for control line signals.

The RS-423 receivers are also single–ended but have an input threshold as low as ±200mV. The input impedance is guaranteed to be greater than 4KΩ, with an operating voltage range of ±7V. The RS-423 receivers can operate up to 120Kbps. RS-423 receivers are used for the IC signal in RS-449 and EIA-530 modes, as shown in *Table 2*.

The third type of receiver supports RS-485, which is a differential interface mode. The RS-485 receiver has an input impedance of 15KΩ and a differential threshold of ±200mV. Since the characteristics of an RS-422 receiver are actually subsets of RS485, the receivers for RS-422 requirements are identical to the RS-485 receivers. RS-422 receivers are used in RS-449 and EIA-530 for receiving clock, data, and some control line signals. The RS-485 receivers are also used for the V.35 mode. V.35 levels require the ±0.55V signals with a load of 100Ω. In order to meet the V.35 input impedance of 100Ω, the external termination network of *Figure 6* must be applied. The threshold of the V.35 receiver is ±200mV. The V.35 receivers

Pin Label	Mode:	RS-232	V.35	RS-422	RS-485	RS-449	EIA-530
$RDEC_3$–$RDEC_0$	0000	0010	1110	0100	0101	1100	1101
RD(a)	Undefined	RS-232	V.35–	RS-422–	RS-485–	RS-422–	RS-422–
RD(b)	Undefined	15KΩ to GND	V.35+	RS-422+	RS-485+	RS-422+	RS-422+
RT(a)	Undefined	RS-232	V.35–	RS-422–	RS-485–	RS-422–	RS-422–
RT(b)	Undefined	15KΩ to GND	V.35+	RS-422+	RS-485+	RS-422+	RS-422+
CS(a)	Undefined	RS-232	RS-232	RS-422–	RS-485–	RS-422–	RS-422–
CS(b)	Undefined	15KΩ to GND	15KΩ to GND	RS-422+	RS-485+	RS-422+	RS-422+
DM(a)	Undefined	RS-232	RS-232	RS-422–	RS-485–	RS-422–	RS-422–
DM(b)	Undefined	15KΩ to GND	15KΩ to GND	RS-422+	RS-485+	RS-422+	RS-422+
RR(a)	Undefined	RS-232	RS-232	RS-422–	RS-485–	RS-422–	RS-422–
RR(b)	Undefined	15KΩ to GND	15KΩ to GND	RS-422+	RS-485+	RS-422+	RS-422+
IC(a)	Undefined	RS-232	RS-232	RS-422–	RS-485–	RS-423	RS-423
IC(b)	Undefined	15KΩ to GND	15KΩ to GND	RS-422+	RS-485+	15KΩ to GND	15KΩ to GND
SCT(a)	Undefined	RS-232	V.35–	RS-422–	RS-485–	RS-422–	RS-422–
SCT(b)	Undefined	15KΩ to GND	V.35+	RS-422+	RS-485+	RS-422+	RS-422+

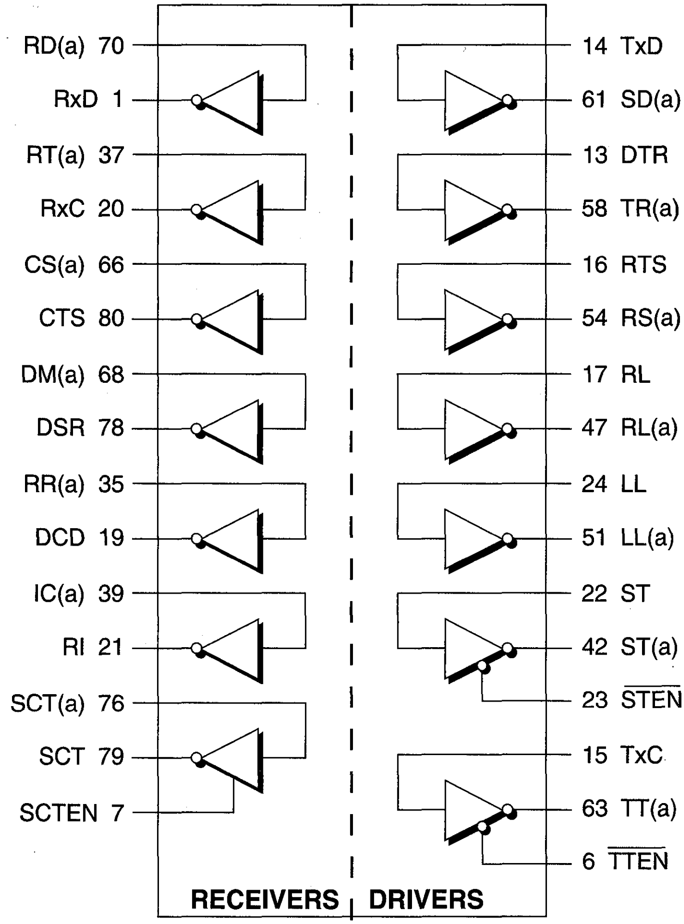
Table 2. SP503 Receivers

can operate up to 5Mbps. All of the differential receivers can receive data up to 5Mbps.

Decoder

The **SP503** has the ability to change the interface mode of the drivers or receivers via an 8–bit switch. The decoder for the drivers and receivers is not latched; it is merely a combinational logic switch. The codes shown in *Tables 1 and 2* are the only specified, valid modes for the **SP503**. Undefined codes may represent other interface modes not specified or random outputs (consult the factory for more information). The drivers are controlled with the data bits labeled $TDEC_3$–$TDEC_0$. The drivers can be put into tri-state mode by writing 0000 to the driver decode switch. The receivers are controlled with data bits $RDEC_3$–$RDEC_0$; the code 0000 written to the receivers will place the outputs in an undetermined state. All receivers, with the exception of SCT, do not have tri-state capability; the outputs will either be high or low depending upon the state of the receiver input.

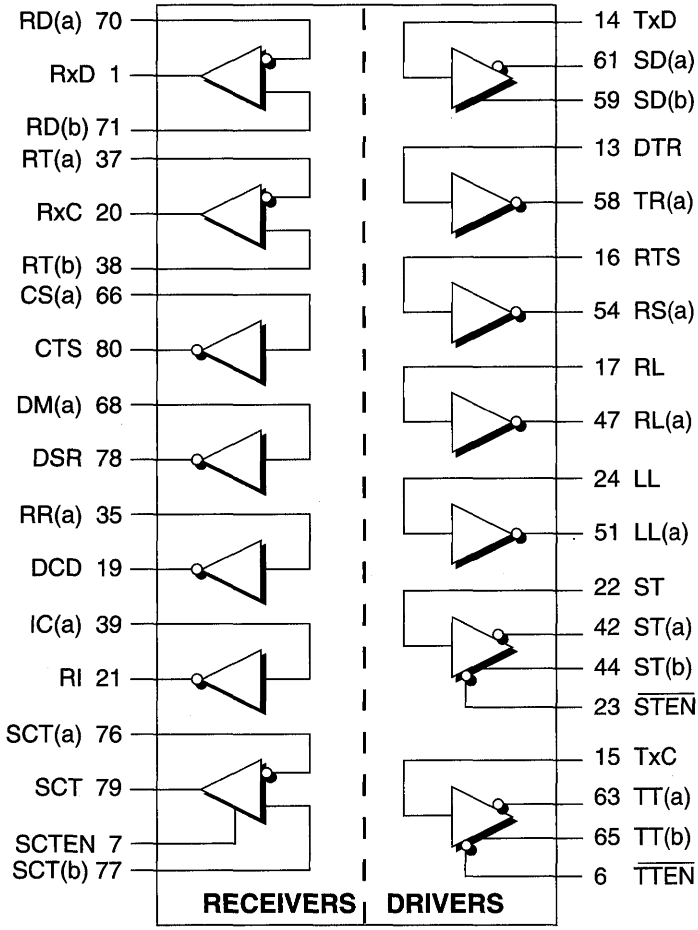
MODE: RS-232							
DRIVER				RECEIVER			
$TDEC_3$	$TDEC_2$	$TDEC_1$	$TDEC_0$	$RDEC_3$	$RDEC_2$	$RDEC_1$	$RDEC_0$
0	0	1	0	0	0	1	0



$\overline{STEN}$	ST	$\overline{TTEN}$	TT	SCTEN	SCT
1	Disabled	1	Disabled	1	Enabled
0	Enabled	0	Enabled	0	Disabled

Figure 7. Mode Diagram — RS-232

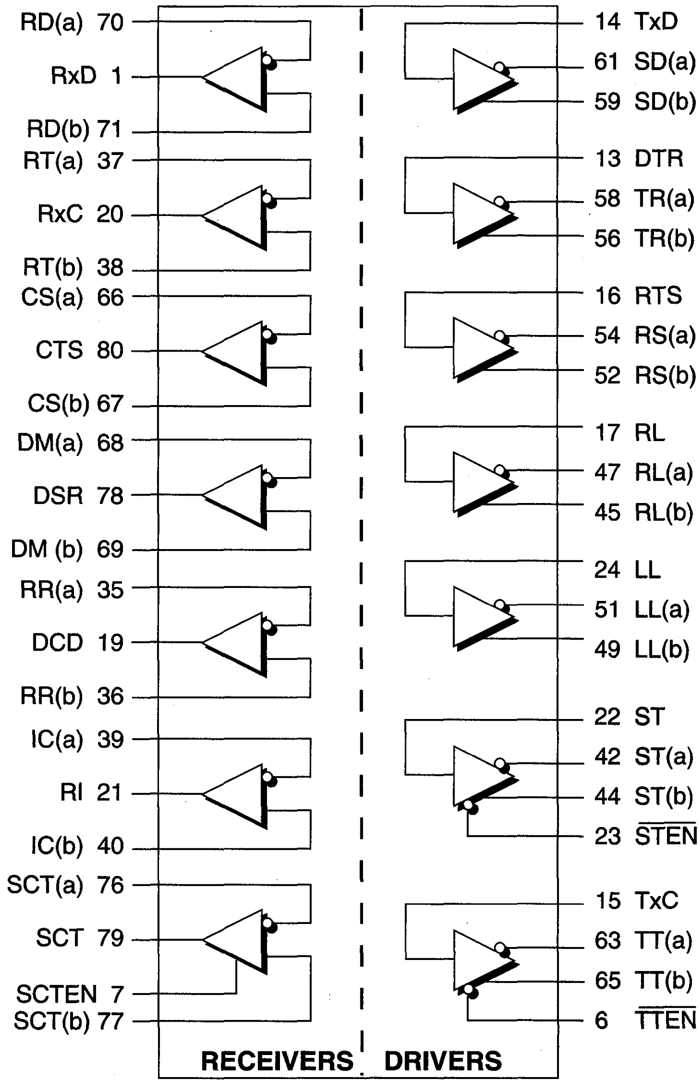
MODE: V.35							
DRIVER				RECEIVER			
$TDEC_3$	$TDEC_2$	$TDEC_1$	$TDEC_0$	$RDEC_3$	$RDEC_2$	$RDEC_1$	$RDEC_0$
1	1	1	0	1	1	1	0



$\overline{STEN}$	ST	$\overline{TTEN}$	TT	SCTEN	SCT
1	Disabled	1	Disabled	1	Enabled
0	Enabled	0	Enabled	0	Disabled

Figure 8. Mode Diagram — V.35

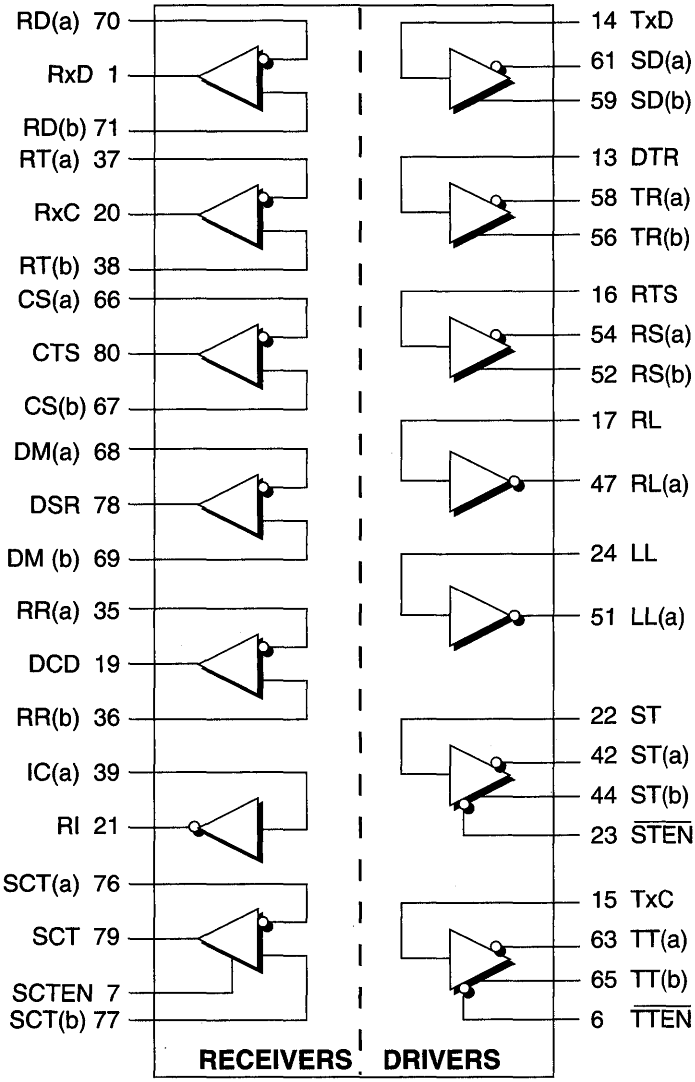
MODE: RS-422							
DRIVER				RECEIVER			
$TDEC_3$	$TDEC_2$	$TDEC_1$	$TDEC_0$	$RDEC_3$	$RDEC_2$	$RDEC_1$	$RDEC_0$
0	1	0	0	0	1	0	0



$\overline{STEN}$	ST	$\overline{TTEN}$	TT	SCTEN	SCT
1	Disabled	1	Disabled	1	Enabled
0	Enabled	0	Enabled	0	Disabled

Figure 9. Mode Diagram — RS-422

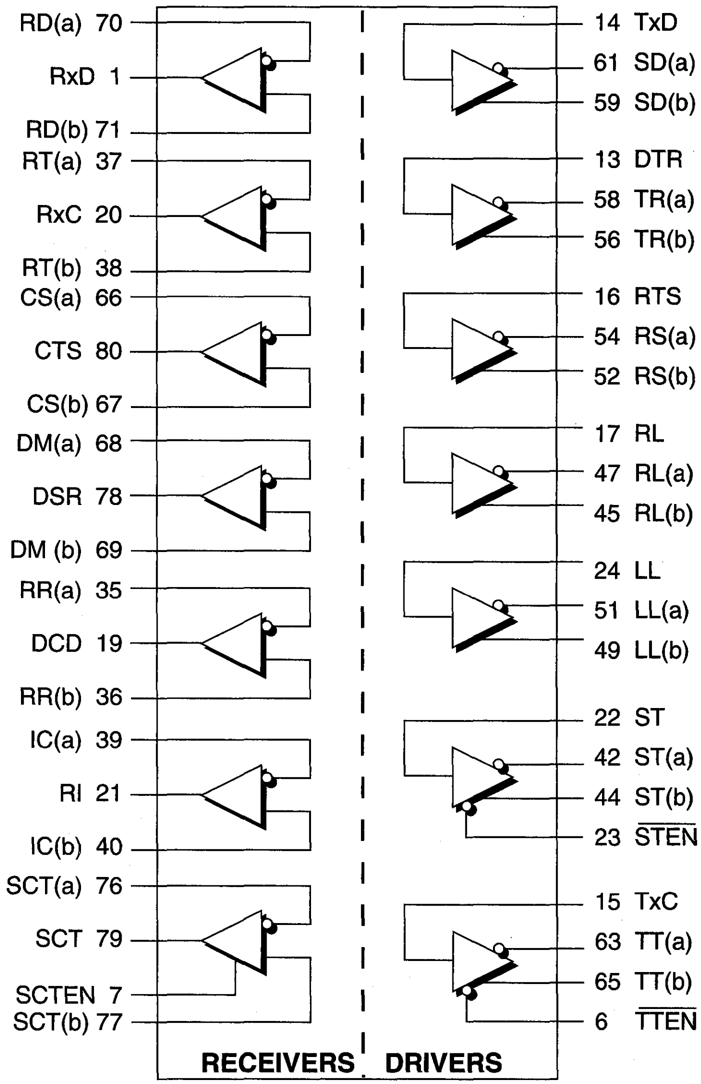
MODE: RS-449							
DRIVER				RECEIVER			
$TDEC_3$	$TDEC_2$	$TDEC_1$	$TDEC_0$	$RDEC_3$	$RDEC_2$	$RDEC_1$	$RDEC_0$
1	1	0	0	1	1	0	0



$\overline{STEN}$	ST	$\overline{TTEN}$	TT	SCTEN	SCT
1	Disabled	1	Disabled	1	Enabled
0	Enabled	0	Enabled	0	Disabled

Figure 10. Mode Diagram — RS-449

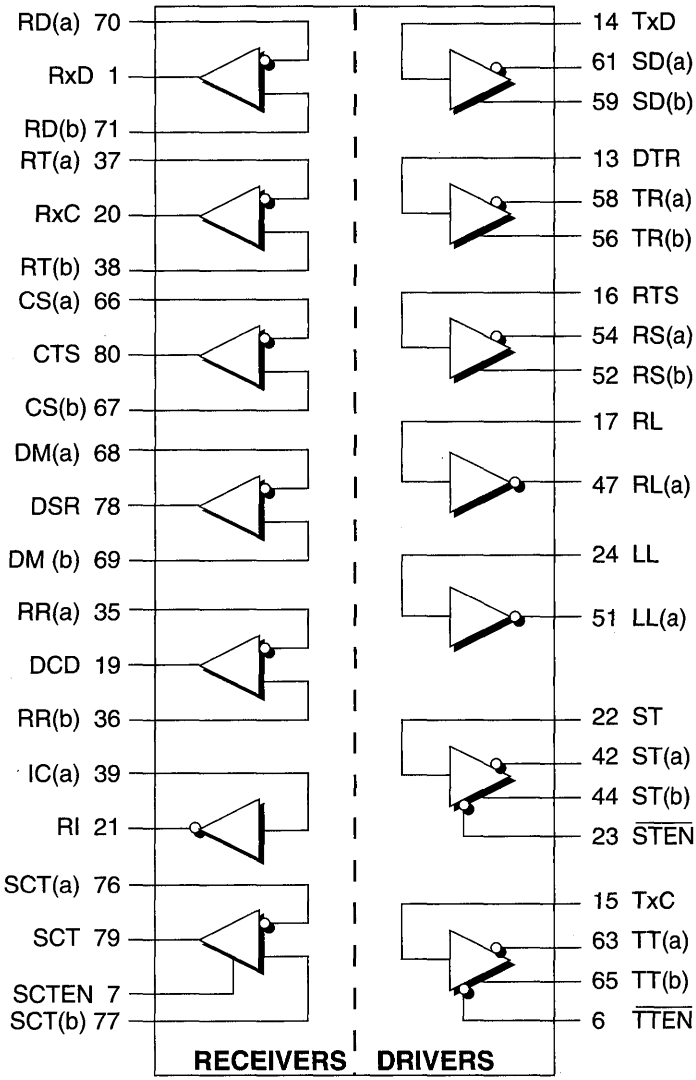
MODE: RS-485							
DRIVER				RECEIVER			
$TDEC_3$	$TDEC_2$	$TDEC_1$	$TDEC_0$	$RDEC_3$	$RDEC_2$	$RDEC_1$	$RDEC_0$
0	1	0	1	0	1	0	1



$\overline{STEN}$	ST	$\overline{TTEN}$	TT	SCTEN	SCT
1	Disabled	1	Disabled	1	Enabled
0	Enabled	0	Enabled	0	Disabled

Figure 11. Mode Diagram — RS-485

MODE: EIA-530							
DRIVER				RECEIVER			
$TDEC_3$	$TDEC_2$	$TDEC_1$	$TDEC_0$	$RDEC_3$	$RDEC_2$	$RDEC_1$	$RDEC_0$
1	1	0	1	1	1	0	1



$\overline{STEN}$	ST	$\overline{TTEN}$	TT	SCTEN	SCT
1	Disabled	1	Disabled	1	Enabled
0	Enabled	0	Enabled	0	Disabled

Figure 12. Mode Diagram — EIA-530

SP502/SP503 EVALUATION BOARD

The **SP502/SP503 Evaluation Board** (EB) Is designed to offer as much flexibility to the user as possible. Each board comes equipped with an 80-pin QFP Zero- Insertion socket to allow for testing of multiple devices. The control lines and inputs and outputs of the device can be controlled either manually or via a data bus under software control. There is a 50-pin connector to allow for easy connection to an existing system via a ribbon cable. There are also open areas on the PC board to add additional circuitry to support application-specific requirements.

Manual Control

The SP502/SP503EB will support both the **SP502** or **SP503** multi-mode serial transceivers. When used for the **SP502,** disregard all notation on the board that is in (brackets) . The **SP502** has a half-duplex connection between the RxT receiver and the TT driver. Due to this internal connection, the RxT receiver inputs can be accessed via the TT(a) and TT(b) pins. If the user needs separate receiver input test pins, jumpers JP1 and JP2 can be inserted to allow for separate receiver inputs located at SCT(a) and SCT(b). The corresponding TTL output for this receiver is labeled as SCT. This test point is tied to pin 79 of the **SP502** or **SP503**. Pin 7 of the evaluation board is connected to the DIP switch, and is labeled as (SCTEN). When used with the **SP502,** this pin should be switched to a low state. When the evaluation board is used with the **SP503,** pin 7 is a tri-state control pin for the SCT receiver.

The transceiver I/O lines are brought out to test pins arranged in the same configuration as shown elsewhere in this data sheet. A top layer silk-screen shows the drivers and receivers to allow direct correlation to the data sheet. The transmitter and receiver decode bits are tied together and are brought out to a DIP switch for manual control of both the driver and receiver interface modes. Since the coding for the drivers and receivers is identical, the bits have been tied together. The DIP switch has 7 positions, four of which are reserved for the TDEC/RDEC control and the other three are used as tri-state control pins. The labels that are in [brackets] apply only to the **SP503**, If a logic one is asserted, the corresponding red LED will be lit. If a zero is asserted, the corresponding red LED will not be lit.

Software Control

A 50-pin connector brings all the analog and digital I/O lines, V_{CC}, and GND to the edge of the card. This can be wired to the user's existing design via a ribbon cable. The pinout for the connector is described in the following section. When the evaluation board is operated under software control, the DIP switch should be set up so that all bits are low (all LEDs off). This will tie 20KΩ pulldown resistors from the inputs to ground and let the external system control the state of the control inputs.

Power and Ground Requirements

The evaluation board layout has been optimized for performance by using basic analog circuit techniques, The four charge-pump capacitors must be 22µF (16V) and be placed as close to the unit as possible; tantalum capacitors are suggested. The decoupling capacitor must be a minimum of 1µF; depending upon the operating environment, 10µF should be enough for worst case situations. The ground plane for the part must be solid, extending completely under the package. The power supplies for the device should be as accurate as possible; for rated performance ±5% is necessary. The power supply current will vary depending upon the selected mode, the amount of loading and the data rate. As a maximum, the user should reserve 200mA for I_{CC}. The worst-case operating mode is RS485 under full load of six (6) drivers supplying 1.6V to 54Ω loads. The power and ground inputs can be supplied through either the banana jacks on the evaluation board (Red = V_{CC} = +5V±5%; Black = GND) or through the connector.

For reference, the 80-pin QFP Socket is a TESCO part number FPQ-80-65-09A. The 50-pin connector is an AMP part number 749075-5.

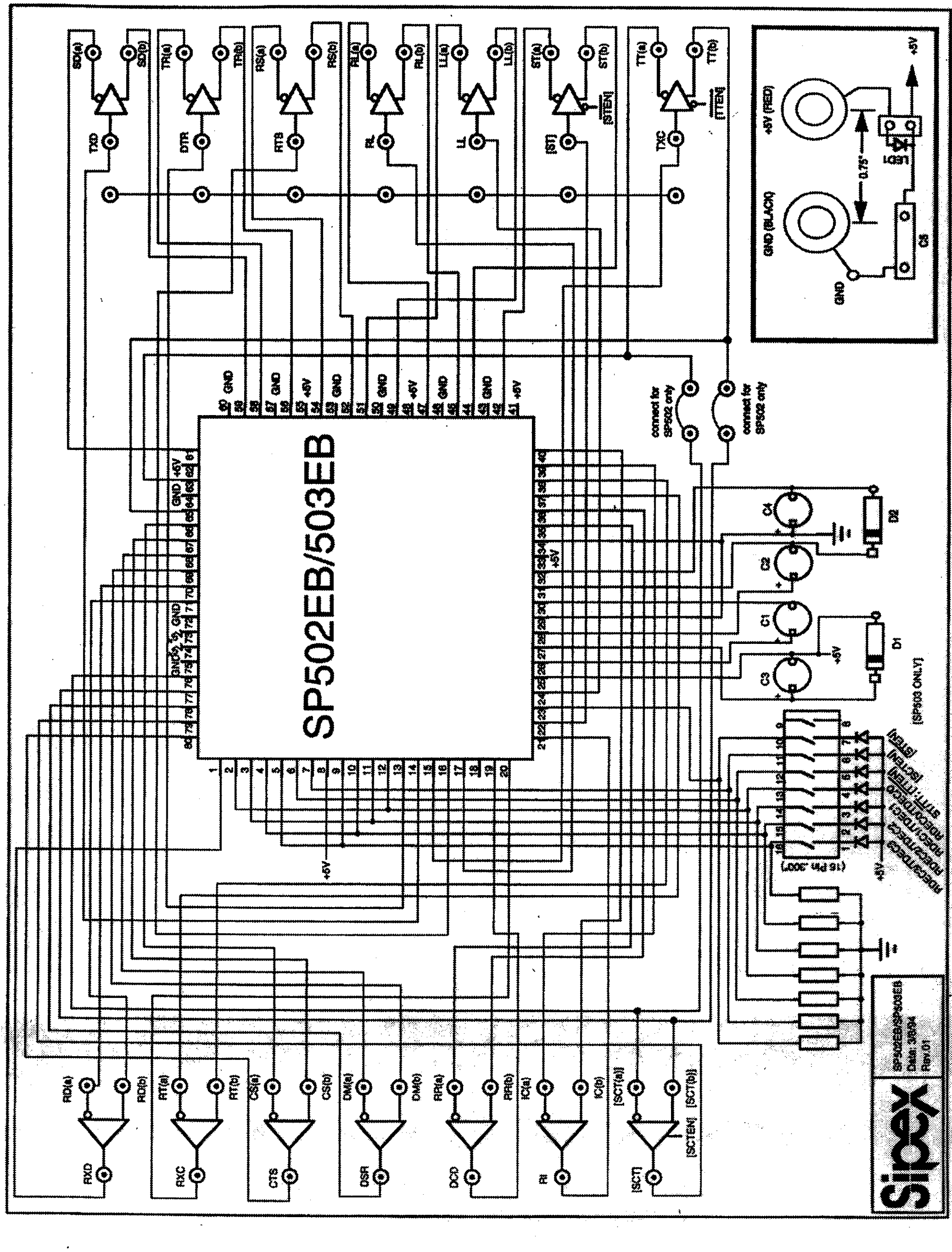


Figure 13. SP502/503 Evaluation Board Schematic

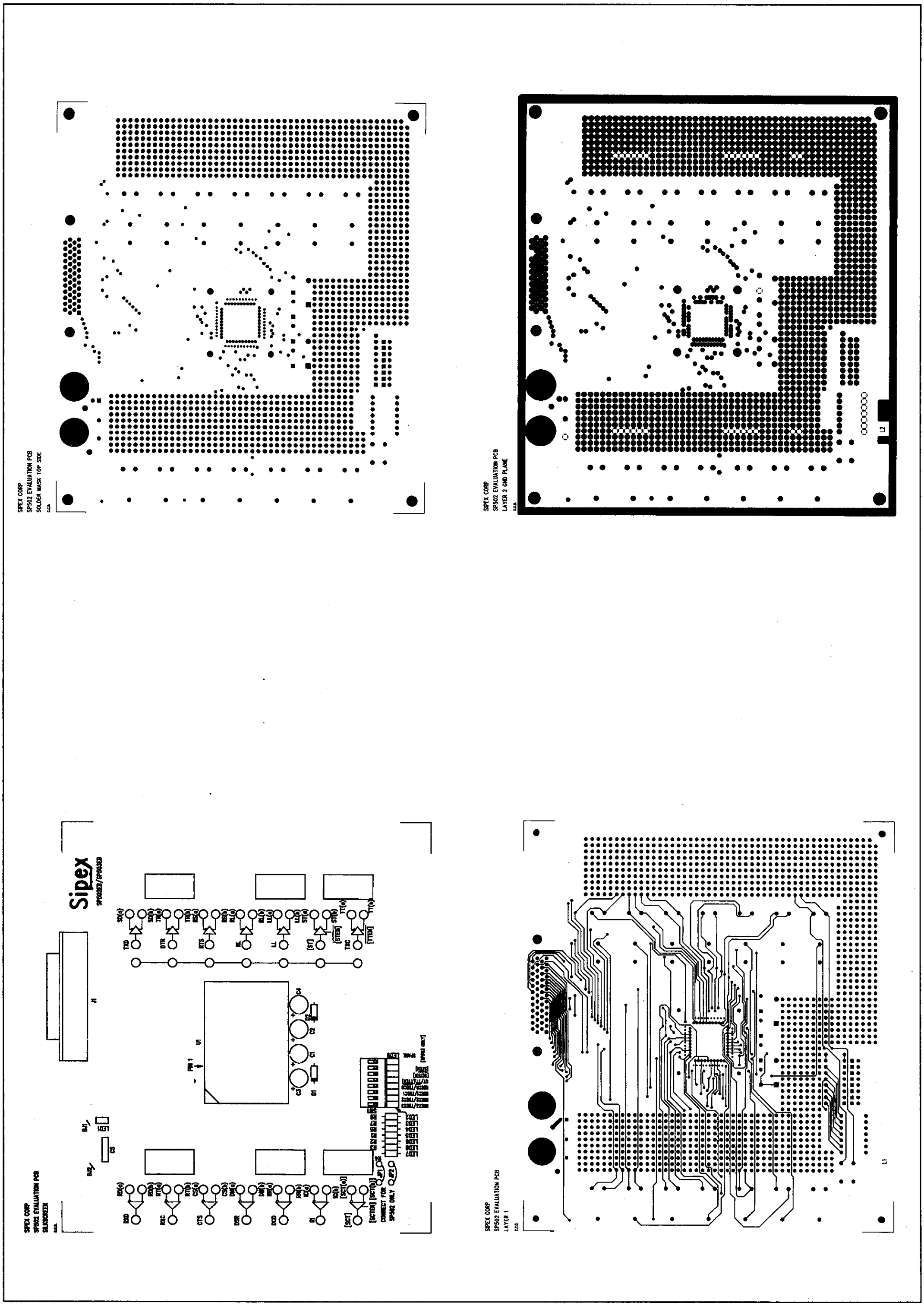
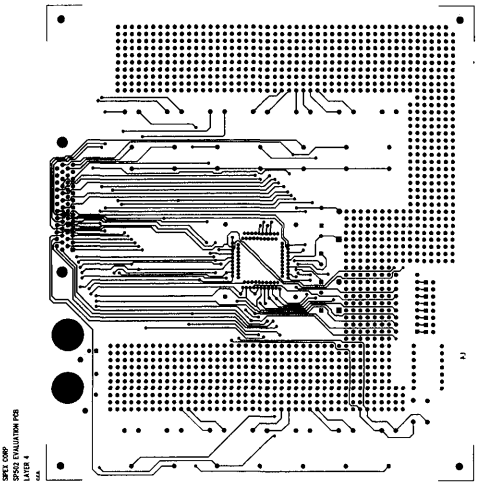
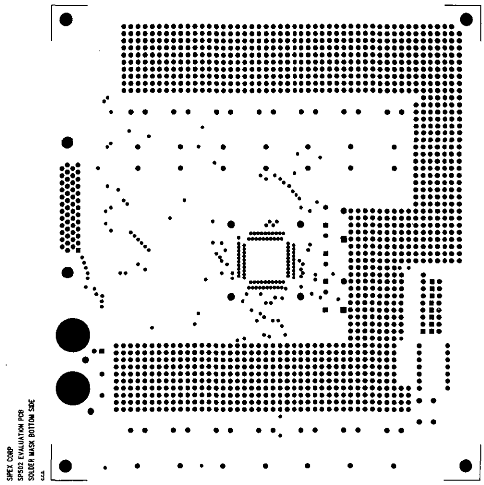


Figure 14a. Evaluation Board — Top Layers





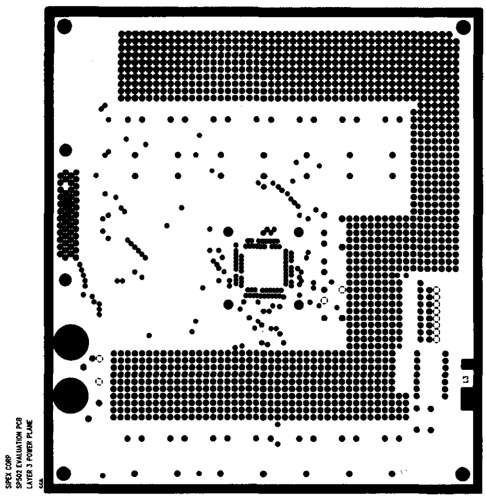


Figure 14b. Evaluation Board — Bottom Layers

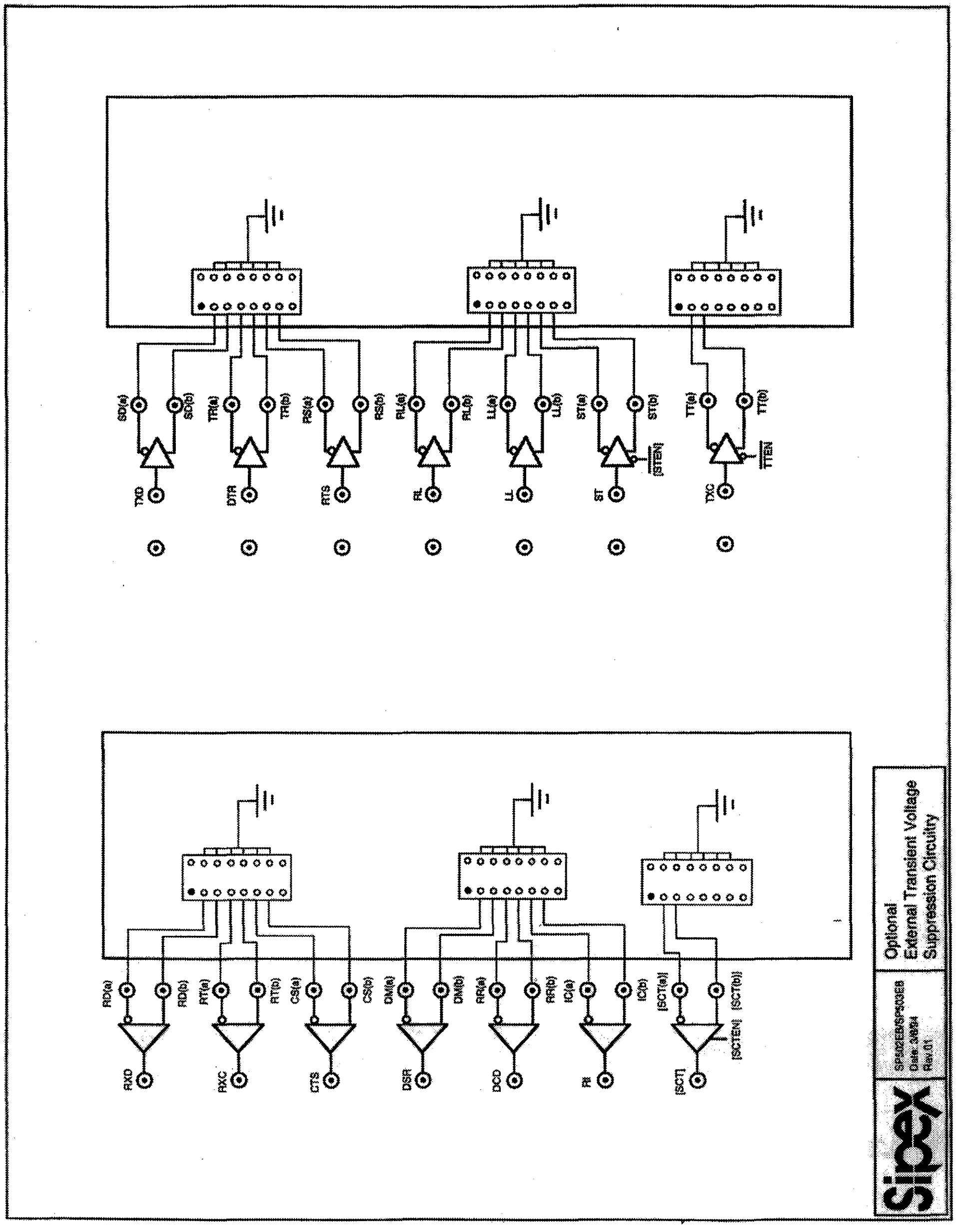
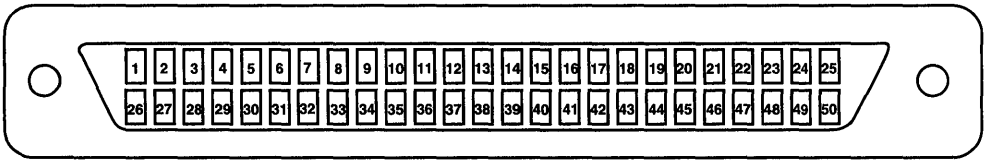
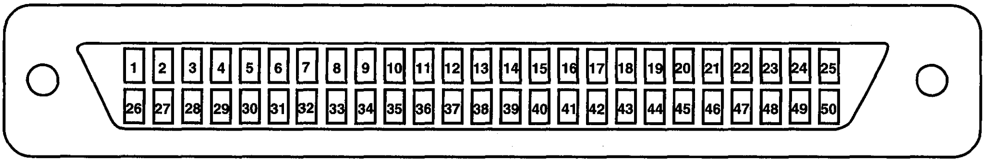


Figure 15. External Transient Suppressors



EDGE CONNECTOR	DUT PIN DESCRIPTIONS
01	TxD (pin 14) –TTL Input – Transmit data; source for SD(a) and SD(b) outputs.
02	DTR (pin 13) – TTL Input – Data terminal ready: source for TR(a) and TR(b) outputs.
03	$ST/\overline{TT}$ (pin 6) –TTL Input – $ST/\overline{TT}$ select pin; enables ST drivers and disables TT drivers when high. Disables ST drivers and enables TT drivers when low.
04	$DEC_3/RDEC_3$ (pin 5) – TTL Input – Transmitter/Receiver decode register.
05	$TDEC_2/RDEC_2$ (pin 4) – TTL Input – Transmitter/Receiver decode register.
06	$TDEC_1/RDEC_1$ (pin 3) – TTL Input – Transmitter/Receiver decode register.
07	$TDEC_0/RDEC_0$ (pin 2) – TTL Input – Transmitter/Receiver decode register.
08	RxD (pin 1) – TTL Output – Receive data; sourced from RD(a) and RD)b) inputs.
09	CTS (pin 80) – TTL Output – Clear to send; sourced from CS(a) and CS(b) inputs.
10	RxT (pin 79) – TTL Output – RxT; sourced from TT(a), TT(b) inputs.
11	DSR (pin 78) – TTL Output – Data set ready; sourced from DM(a) and DM(b) inputs.
12	RD(b) (pin 71) – Analog In – Receive data, non–inverted; source for RxD.

EDGE CONNECTOR	DUT PIN DESCRIPTIONS
13	RD(a) (pin 70) – Analog In – Receive data, inverted: source for RxD.
14	DM(b) (pin 69) – Analog In – Data mode, non–inverted; source for DSR.
15	DM(a) (pin 68) – Analog In – Data mode, inverted; source for DSR.
16	CS(b) (pin 67) – Analog In – Clear to send; non–inverted; source for CTS.
17	CS(a) (pin 66) – Analog In – Clear to send, inverted; source for CTS.
18	TT(b) (pin 65) – Analog Out – Terminal timing, non–inverted: sourced from TxC input.
19	TT(a) (pin 63) – Analog Out – Terminal timing; inverted: sourced from TxC input.
20	TR(a) (pin 58) – Analog Out – Terminal ready, inverted; sourced from DTR.
21	TR(b) (pin 56) – Analog Out – Terminal ready; non–inverted; sourced from DTR.
22	SD(a) (pin 61) – Analog Out – Send data, inverted; sourced from TxD.
23	SD(b) (pin 59) – Analog Out – Send data; non–inverted; sourced from TxD.
24	RS(a) (pin 54) – Analog Out – Ready to send; inverted; sourced from RTS.
25	RS(b) (pin 52) – Analog Out – Ready to send, non–inverted; sourced from RTS.



EDGE CONNECTOR	DUT PIN DESCRIPTIONS
26	ST (pin 22) – TTL Input – Send Timing; source for ST(a) and ST(b) outputs. SP503 only.
27	$\overline{STEN}$ (pin 23) – TTL Input — Driver enable control pin; active low. SP503 only,
28	SCT(a) (pin 76) – Analog Input – Inverting; input for SCT receiver; SP503 only.
29	SCT(b) (pin 77) – Analog Input – Non–inverting; input for SCT receiver. SP503 only.
30	V_{CC} — +5V for all circuitry.
31	GND — signal and power ground.
32	LL(a) (pin 51) – Analog Out – Local loopback, inverted; sourced from LL.
33	LL(b) (pin 49) – Analog Out – Local loopback, non–inverted sourced from LL.
34	RL(a) (pin 47) – Analog Out – Remote loopback; inverted; sourced from RL.
35	RL(b) (pin 45) – Analog Out – Remote loopback; non–inverted; sourced from RL.
36	ST(b) (pin 44) – Analog Out – Send timing, non–inverted; sourced from TxC.
37	ST(a) (pin 42) – Analog Output –Send timing, inverted; sourced from TxC.
38	IC(b) (pin 40) – Analog In – Incoming call; non–inverted; source for RI.
39	IC(a) (pin 39) – Analog In – Incoming call; inverted; source for RI.
40	RT(b) (pin 38) – Analog In – Receive timing, non–inverted; source for RxC.
41	RT(a) (pin 37) – Analog In – Receive timing; inverted; source from RxC.
42	RR(b) (pin 36) – Analog In – Receiver ready; non–inverted; source for DCD.
43	RR(a) (pin 35) – Analog In – Receiver ready; inverted; source for DCD.
44	LL (pin 24) – TTL Input – Local loopback; source for LL(a) and LL(b) outputs.
45	RI (pin 21) – TTL Output – Ring indicator; sourced from IC(a) and IC(b) inputs.
46	RxC (pin 20) – TTL Output – Receive clock; sourced from RT(a) and RT(b) inputs.
47	DCD (pin 19) – TTL Output – Data carrier detect; sourced from RR(a) and RR(b) inputs.
48	RL (pin 17) – Analog Out – Remote loopback; source for RL(a) and RL(b) outputs.
49	RTS (pin 16) – TTL Input – Ready to send; source for RS(a) and RS(b) outputs.
50	TxC (pin 15) – TTL Input – Transmit clock; source for TT(A) and TT(B) outputs.

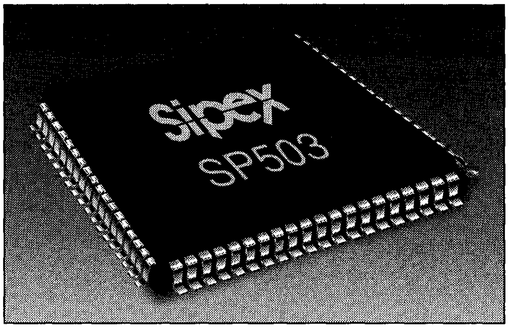
ORDERING INFORMATION

Model	Temperature Range	Package Types
SP503CF	0°C to +70°C	80–pin QFP

THIS PAGE LEFT INTENTIONALLY BLANK

SP503 Application Note

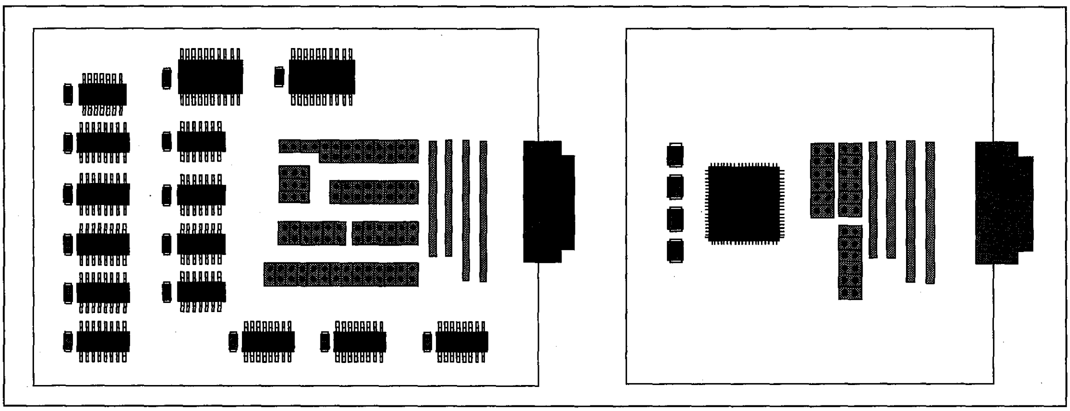
- DTE and DCE configurations with the SP503
- Connecting the SP503 to a DB-25 connector in DTE and DCE modes
- Implementing V.35 with the SP503
- Creating extra single-ended and differential channels with the SP503 using the SP310A and SP485
- Using external supplies with the SP503



Due to its flexibility and programmability, the **SP503** has been finding its way into many new networking products. The **SP503** offers an excellent replacement for discrete solutions on X.25 implementations for frame relay systems, multi-protocol routers and other WAN products where many designs run various modes such as RS-232, RS-422, V.35 or V.36.

For RS-232, the older bipolar 1488 and 1489 parts, or even the newer MAX230 or SP230 series have traditionally been used. For RS-422 or RS-485, the 26LS31, 26LS32, 3488, and 3489 have been seen in many designs. These parts have been also used for V.35 but with external termination resistors. For a typical design, four RS-232 chips would be used for a complete RS-232 port, four RS-422 chips for an RS-422 port and four chips for V.35 with an external resistor network. Port programmability would require relays or switches so that software lines can control whether RS-232 is active or RS-422 is active. The relays increase board capacity as well as cost to the design.

The **SP503** solves board space and cost problems by offering a single packaged part that supports various protocols and also offers software programmability to the port.



Typical discrete solution vs. the SP503

DTE and DCE configurations with the SP503

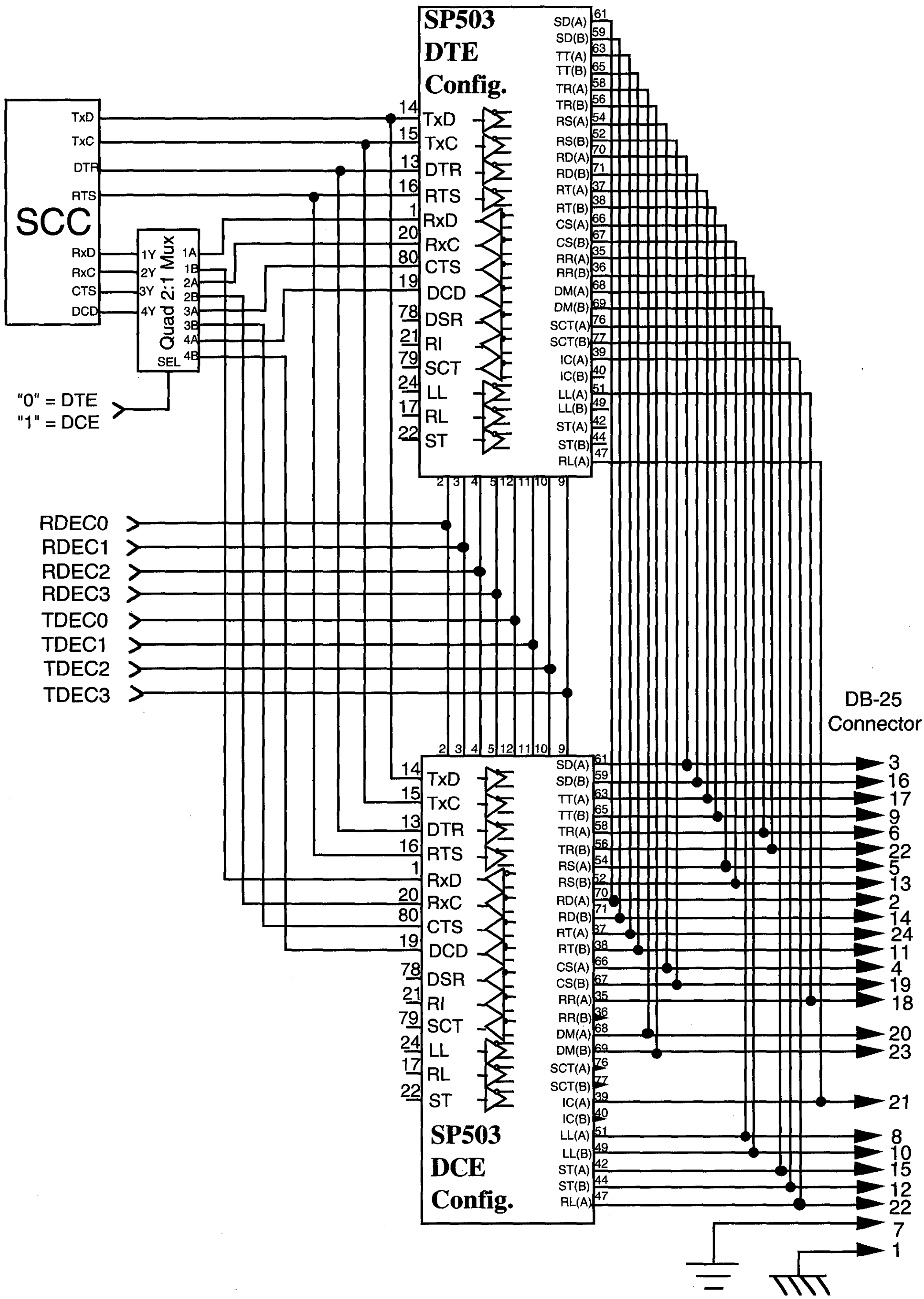
The **SP503** has designated signals such as "Transmit Data", "Clear-to-Send", etc.which designers can easily allocate the appropriate **SP503** transceivers for the corresponding signals. The data signals specified in the EIA standards and CCITT are referenced in the **SP503** datasheet as DTE. Some customers have wondered if they can use the **SP503** for DCE applications. Although it can be confusing at first glance, the DCE implementation is the mirror image of the DTE side. For the DTE, TxD is a driver which drives the data to RxD, a receiver, on the DCE side. TxC or TT is a driver on the DTE side which drives the clock signal to the RxC receiver on the DCE side.

The next three pages illustrate the CCITT signal allocations from the **SP503** in either DTE or DCE to the DB-25 connector. As shown, it is possible to use a DB-25 connector for the various protocols offered by the **SP503**.

DB-25 Connector Pin Assignments for Various Protocols

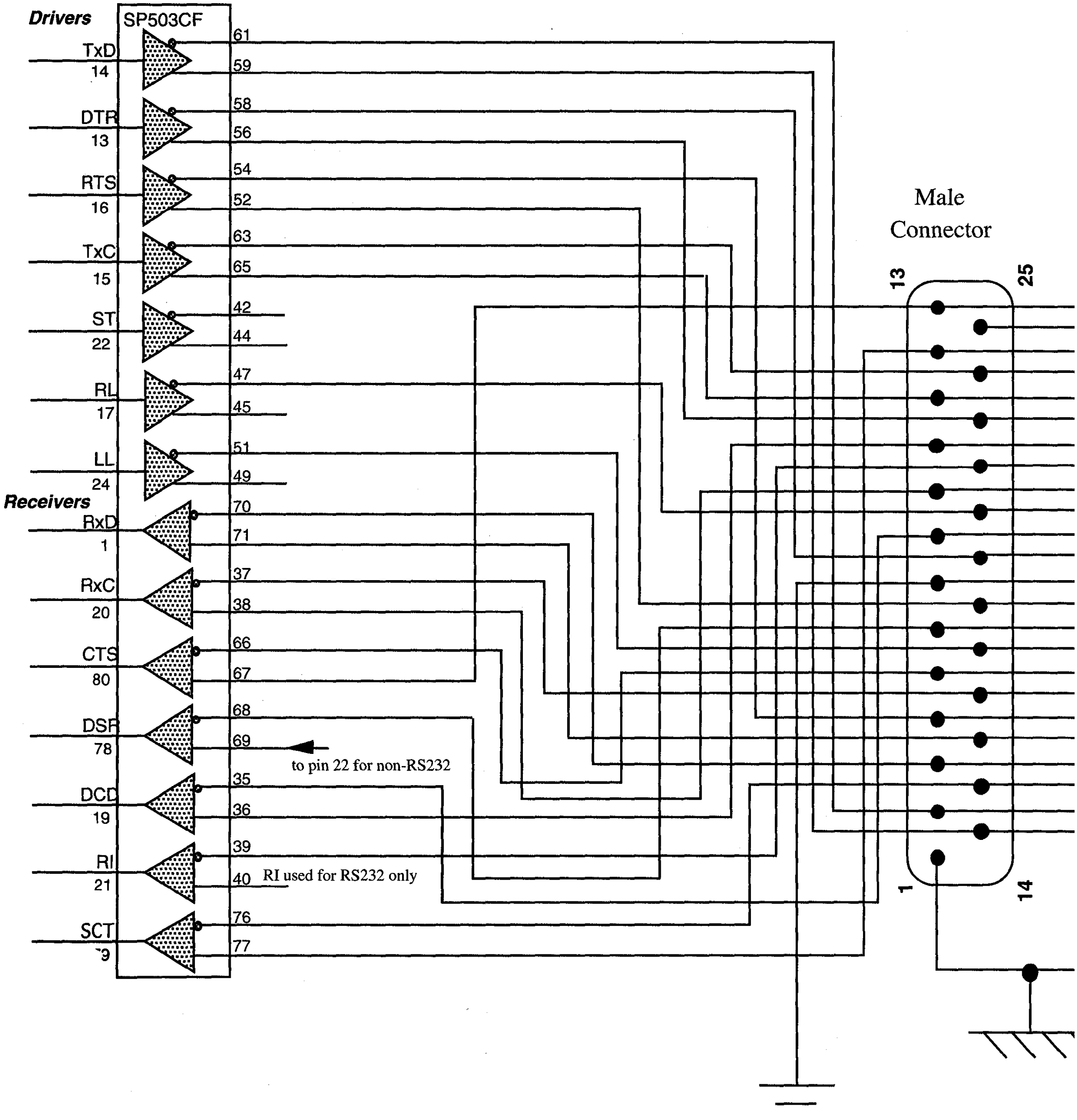
DB-25 Pin #	RS-232	EIA-530	RS-449	RS-422	V.35	V.36
1	shield	shield	shield	shield	CCITT# 101	CCITT# 101
2	TxD	TxD(A)	SD(A)	T(A)	103(A)	103(A)
3	RxD	RxD(A)	RD(A)	R(A)	104(A)	104(A)
4	RTS	RTS(A)	RS(A)	C(A)	105	105(A)
5	CTS	CTS(A)	CS(A)	–	106	106(A)
6	DSR	DSR(A)	DM(A)	–	107	107(A)
7	Signal GND	Signal GND	Signal GND	Signal GND	102	102
8	DCD	RLSD(A)	RR(A)	I(A)	109	109(A)
9	–	RxC(B)	RT(B)	–	115(B)	115(B)
10	–	RLSD(B)	RR(B)	I(B)	–	109(B)
11	–	TxC(B-DTE)	TT(B)	–	113(B)	113(B)
12	DCD (2nd)	TxCC(B-DCE)	ST(B)	S(B)	114(B)	114(B)
13	CTS (2nd)	CTS(B)	CS(B)	–	–	106(B)
14	TxD (2nd)	TxD(B)	SD(B)	T(B)	103(B)	103(B)
15	TxCC (DCE)	TxCC(A-DCE)	ST(A)	S(A)	114(B)	114(B)
16	RxD (2nd)	RxD(B)	RD(B)	R(B)	104(B)	104(B)
17	RxC	RxC(A)	RT(A)	–	115(A)	115(A)
18	LL	LL	LL	–	–	141
19	RTS (2nd)	RTS(B)	RS(B)	C(B)	–	105(B)
20	DTR	DTR(A)	TR(A)	–	–	–
21	RL	RL	RL	–	–	140
22	RI	DSR(B)	DM(B)	–	–	107(B)
23	SRS	DTR(B)	TR(B)	–	–	–
24	TxC (DTE)	TxC(A-DTE)	TT(A)	–	113(A)	113(A)

DTE-DCE flexibility with the SP503 on a DB-25 serial port



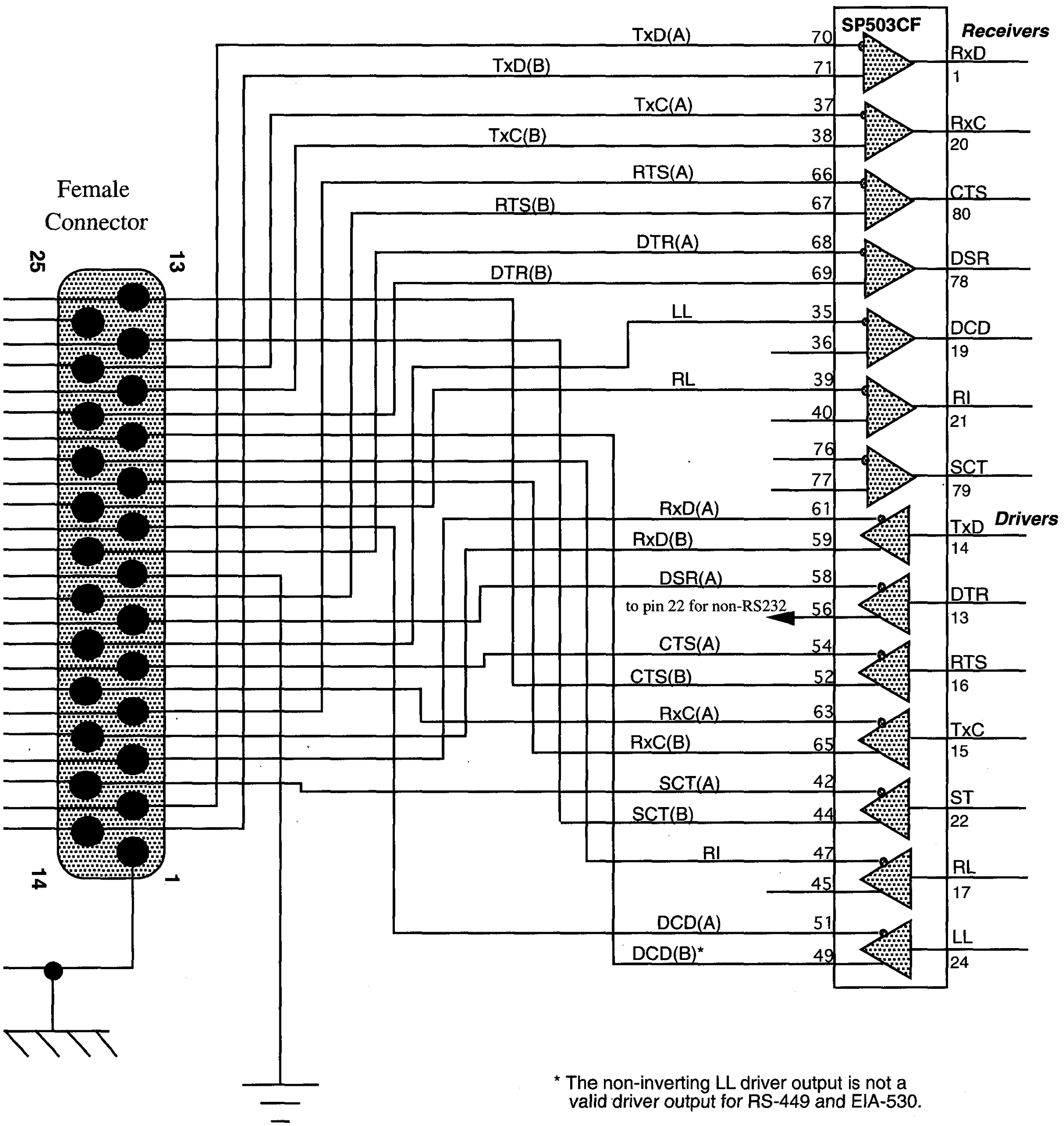
Driver / Receiver Connections to a DB-25 Connector

DTE Mode



Driver / Receiver Connections to a DB-25 Connector

DCE Mode



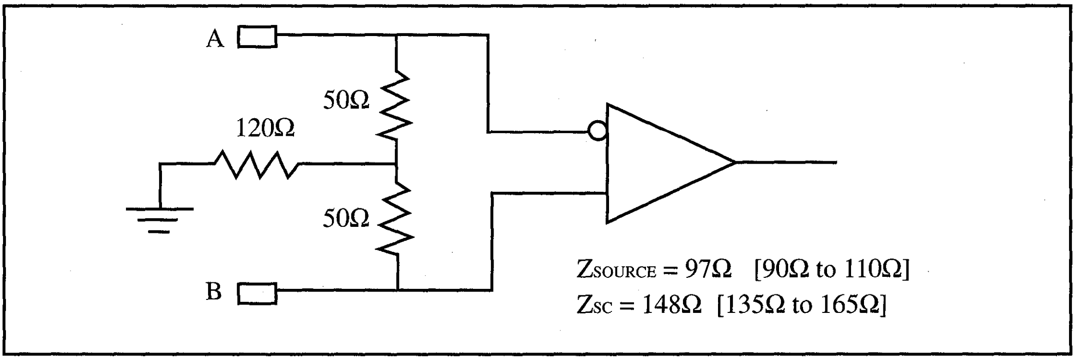
* The non-inverting LL driver output is not a valid driver output for RS-449 and EIA-530.

SP503 V.35 External Termination Resistors

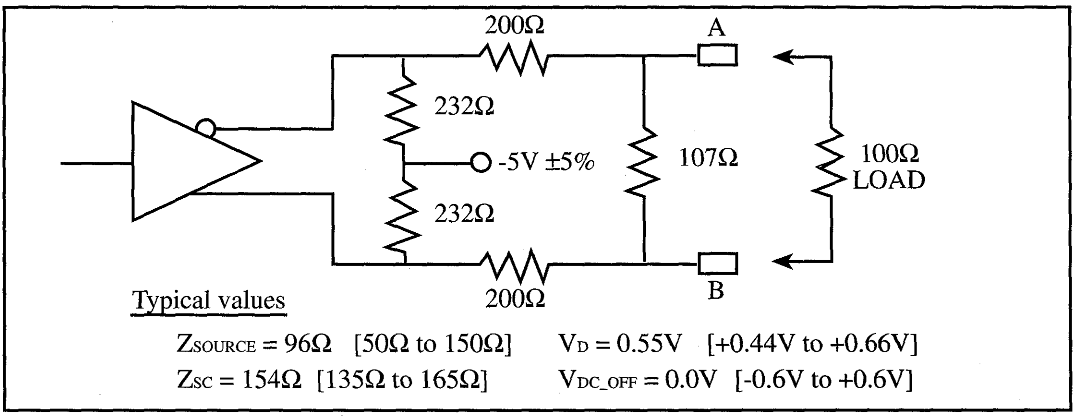
V.35 implementation requires external resistors to be connected to the driver outputs and receiver inputs. The resistors are needed for reducing signal levels and maintaining input and output impedance levels that conform to CCITT Recommendation V.35. The drawings below offer both receiver input termination and driver output termination configurations that will comply to V.35.

As you may know, the termination resistors are for V.35 mode only and have to be disconnected when another mode is programmed. There are a few ways to connect and disconnect the network. One method is to add a daughter-card option slot onto the main printed circuit board where the **SP503** is mounted. This allows the user to add a mini-PC card that contains the V.35 network to be connected to the driver outputs and receiver inputs. Another method is to implant the V.35 network into a cable if the user requires conversion cables to switch from one protocol to another. For example, if the serial port has a DB-25 connector and requires an ISO-2593 connector for V.35; a DB-25 to ISO-2593 conversion cable containing the V.35 network is connected to the port.

Of course this method will not allow programmability to the serial port if the user wants to run various protocols to that port. To actively switch protocols by software control, you can use analog switches or relays. Sipex recommends using low-ON resistance analog switches, such as Siliconix DG643© analog switches for the driver outputs, and solid-state relays such as the AT&T LH1514© for the receiver inputs. See opposite page for an example of the SP503 V.35 configuration.



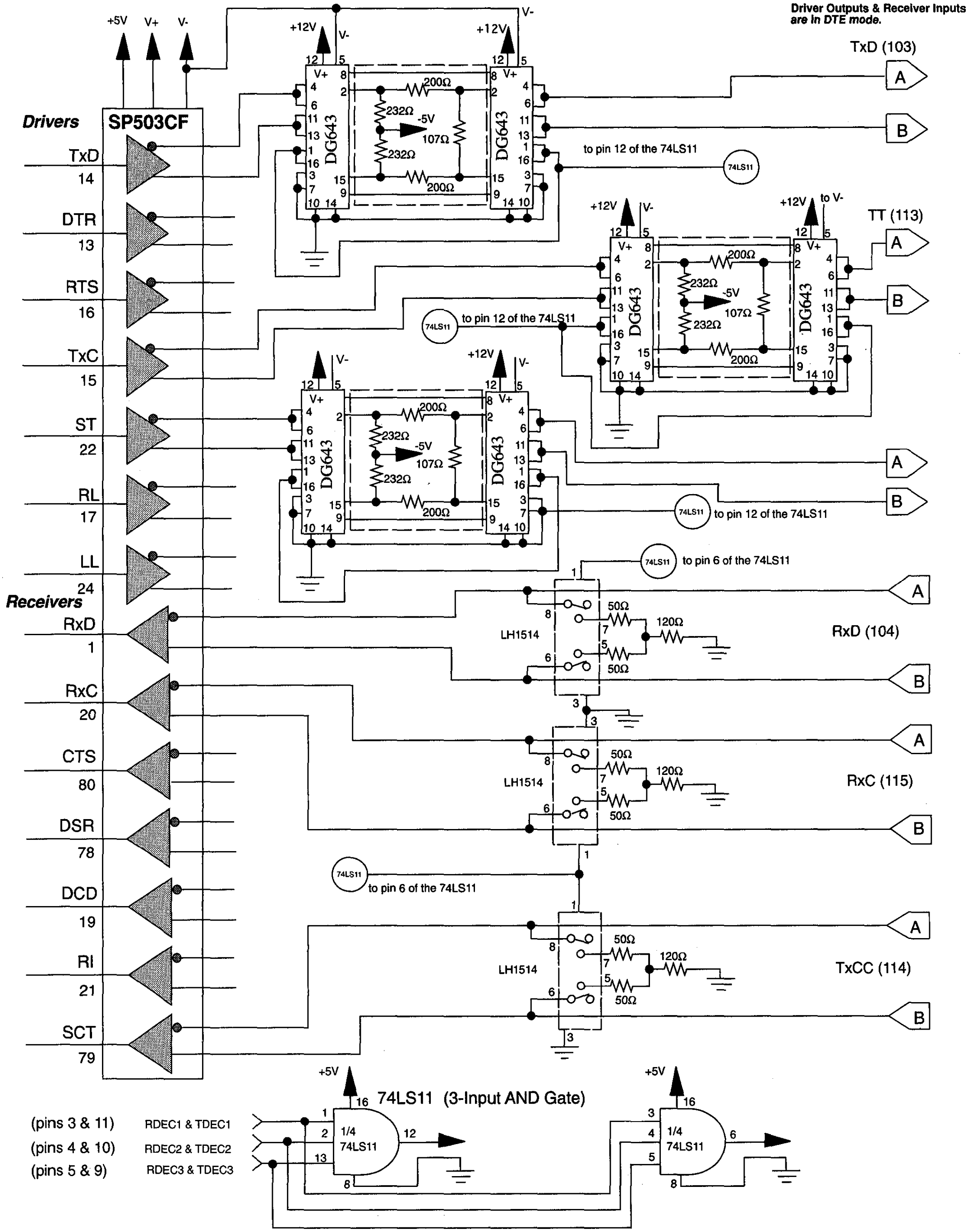
V.35 Receiver Input Termination Resistor Network



V.35 Driver Output Termination Resistor Network

SP503 Switching Configuration for V.35 Implementations

- Switches are **Siliconix DG643DY** analog switches.
- Solid-State Relays are **AT&T, LH1514**.
- Resistors are 1/8W, 1% tolerance.
- External Supplies necessary are: V_{cc} = +5V, V+ = +12V (for V+ on the DG643DY) and V_n = -5V.



Typical Applications Questions on the SP503

Can the **SP503** be used with external power supplies? If so, is there a power up sequence?
The internal charge pump can be bypassed through external supplies to V_{DD} and V_{SS}. The external voltage should be +10V for V_{DD} and -10V for V_{SS}. The tolerance is ±5%. The **SP503** can be powered up in any order without latch-up problems. The absolute minimum limit for the external supplies is ±7V and the absolute maximum limit is ±10.5V.

What is the maximum input voltage applied to the receiver input without damaging the **SP503**?
The receiver inputs can tolerate up to ±16V in any protocol without latching up the device. Since RS-232 ranges from ±5V to ±15V; the **SP503** is well within the accepted range. It may be worthwhile to include 15V clamping diodes or transient voltage suppressors so that the receiver input will be held below ±15V.

What is the maximum short-circuit voltage that can be applied to a **SP503** driver output?
The driver outputs can be shorted up to ±16.0V without causing damage to the driver. Between the ±16V range, the **SP503** adheres to the RS-232 short circuit current limit of 100mA and to the RS-422/RS-423 limit at 150mA. Again, transient voltage suppressors or clamping diodes will protect the **SP503** if exceeding the ±16V range is possible.

What is the state of the **SP503** drivers and receivers when the device is addressed with 0000?
The **SP503** drivers are in a high impedance(over 1MΩ) tri-state condition when "0000" is addressed. The receivers are not tri-stated and the outputs are undefined. This means that they could be floating to either a high or low level depending on the previous state of the receiver input prior to the 0000 addressing change. The receiver input impedance is at 15kΩ for "0000".

Can the **SP503** be programmed for 7 drivers and 7 receivers in RS-423 mode?
The **SP503** can be switched to RS-423 mode by programming $TDEC_3$, $TDEC_2$, $TDEC_1$, $TDEC_0$ to "1000" for the drivers and $RDEC_X$ to "1000" for the receivers. However, external supplies must be used in order to drive RS-423. The internal charge pump can only support up to three RS-423 drivers and three RS-423 receivers.

What is the power dissipation in the **SP503** and in which mode does it consume the most power?
The **SP503** dissipates approximately 400mW to 1.4W depending on the protocol. RS-485 mode consumes the most power at 1.4W. For worst case power dissipation, all seven drivers were driven with a TTL signal and the outputs were looped back into the receiver inputs to generate a TTL output. All drivers and receivers were active.

MODE	P_D
RS-232	0.418W
RS-422	0.970W
RS-485	1.382W
RS-449	0.959W
EIA-530	0.959W
V.35	1.055W

What is the state of the **SP503** drivers and receivers when the device is addressed with 1111?
The address for "1111" is not used in the **SP503**. If the **SP503** is programmed for "1111", the drivers are approximately 1.0V and at a high impedance (approx. 9MΩ). The receivers are not tri-stated and the outputs are undefined. All receiver inputs are at 15kΩ input impedance. The **SP503** can receive a "1111" address while V_{CC} is off. The supply current is approximately 50mA (V_{CC} = +5V) while the address is at "1111".

In the RS-232 signal assignments for the DB-25 connector, where does the **SP503** account for Test Mode(TM) ?

For most RS-232 applications, the signals commonly used are TxD, TxC, RxD, RxC, RTS, CTS, DSR, SG, DCD, DTR and Frame Ground. In DTE mode; TxD, TxC, RTS, DTR are the drivers and RxD, RxC, CTS, DSR, DCD are the receivers. Since there are seven drivers and seven receivers in the **SP503**, the designer can easily use the **SP503** for the above signals. Other RS-232 applications will support diagnostic functions such as LL (driver), RL (driver), and TM (receiver) which may or may not require extra transceivers depending if other signals are not used. Since Test Mode (TM) is a receiver for DTE designs, the Ring Indicator (RI) receiver in the **SP503** (pin 21) can be used for TM if RI is not used. If all the available drivers and receivers are used in the **SP503**, then another RS-232 transceiver can be added. See page 120 and 121 for suggestions on adding Sipex's RS-232 and RS-485 transceivers.

Are the Schottky diodes used on Vcc to Vss and Vdd to C2- in the **SP502** necessary for the **SP503**?

Sipex has incorporated the Schottky diodes needed in the **SP502** into the **SP503** in order to protect against potential start up problems due to fast rate of rise on V_{cc}(1V/µs) and overvoltage to the TTL inputs. However, a negative voltage (V_{in} -5V) applied to the receiver inputs while the **SP503** is powered off will cause start up problems to the charge pump. In order to guard against this condition, an external Schottky diode should be placed from Vcc to Vdd to minimize V_{CC} current injection to the IC substrate and allow the charge pump to operate properly. See page 93 Figure 6 - Typical Operating Circuit, for diode connection schematic.

Can the **SP503** be configured for V.36?

CCITT Recommendation V.36 is similar to RS-449 where certain signals are RS-422 signals and others are RS-423. Depending on different applications; "Transmit Data", "Terminal Timing", "Request-to-Send", "Data Terminal Ready", "Receive Data", "Transmit Clock", "Receive Clock", "Clear-to-Send", "Data Carrier Detect", and "DataSet Ready" are specified as Category 1 Circuits where the protocol is RS-422 for rates over 20kbps. All other circuits are Category 2 Circuits which are specified as RS-423 circuits. Depending on particular signals, the **SP503** can be easily used for V.36.

When the two drivers, ST and TT, are in tri-state mode, what will the driver outputs tolerate for maximum short circuit voltages? And the receiver, SCT, input?

The driver outputs will tolerate up to ±16.0V without any damage to the circuit regardless of whether or not ST and TT are in tri-state mode. The tri-state circuitry does not affect the short circuit protection on the driver outputs. The SCT receiver input will tolerate up to ±16.0V without any damage to the input structure regardless of whether or not SCT is in tri-state mode.

What does Sipex recommend for transient voltage suppression techniques for the **SP503**?

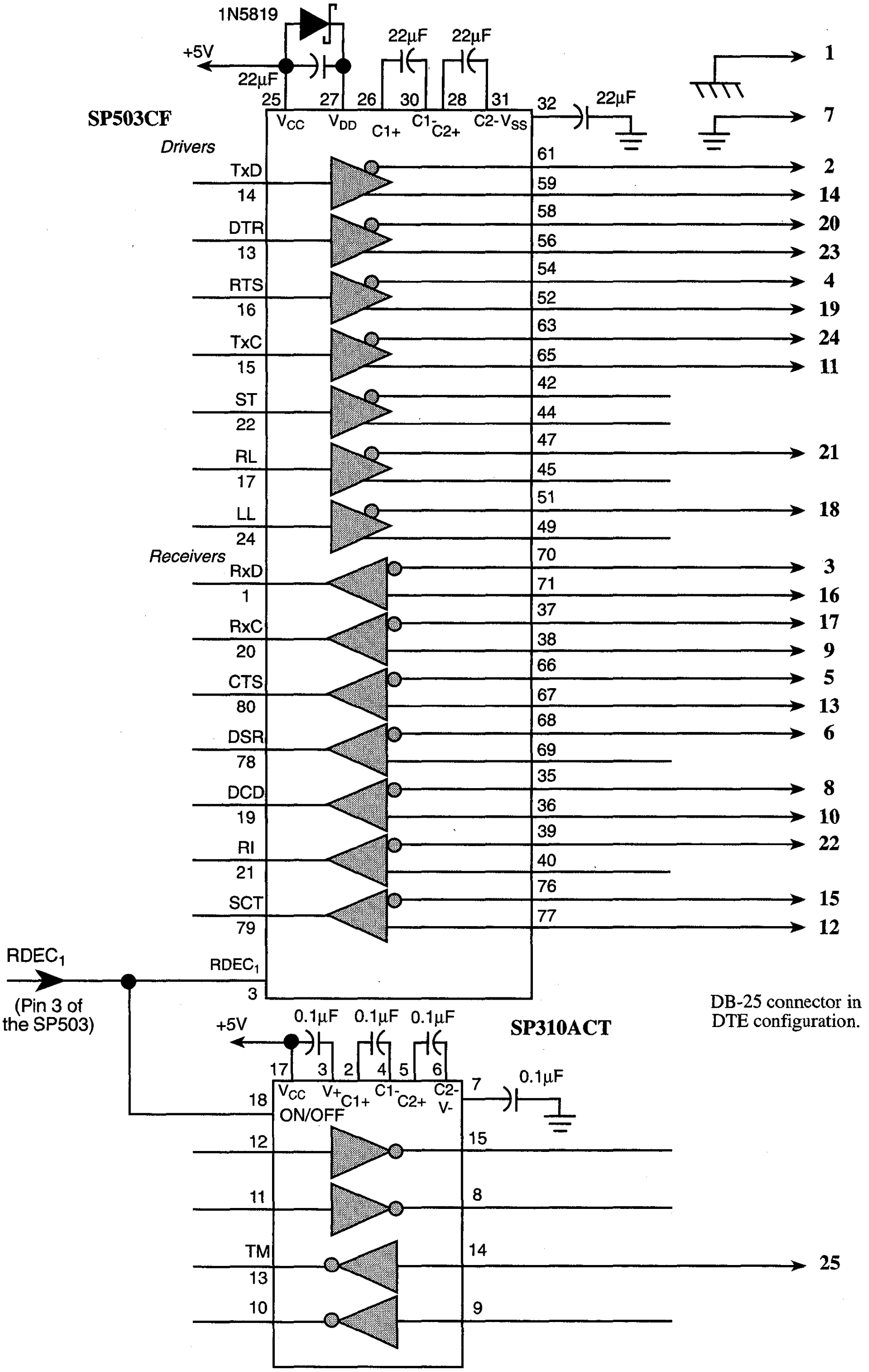
For our evaluation boards, Sipex uses transient voltage suppressor ICs from ProTek Devices, model numbers LCA05C to LCA15C. The two digits in the part number pertain to the rated stand-off voltage, V_{WM}, which is the maximum working DC voltage applied to the device. These TVS devices are especially designed for serial data communications because of their low capacitance and low impedance. Another recommended manufacturer is AVX Corporation TransGuard series of TVS components. AVX offers a variety of surface mount back-to-back diodes.

ProTek Devices • P.O. Box 3129 • Tempe, AZ. 85280 • 602-431-8101

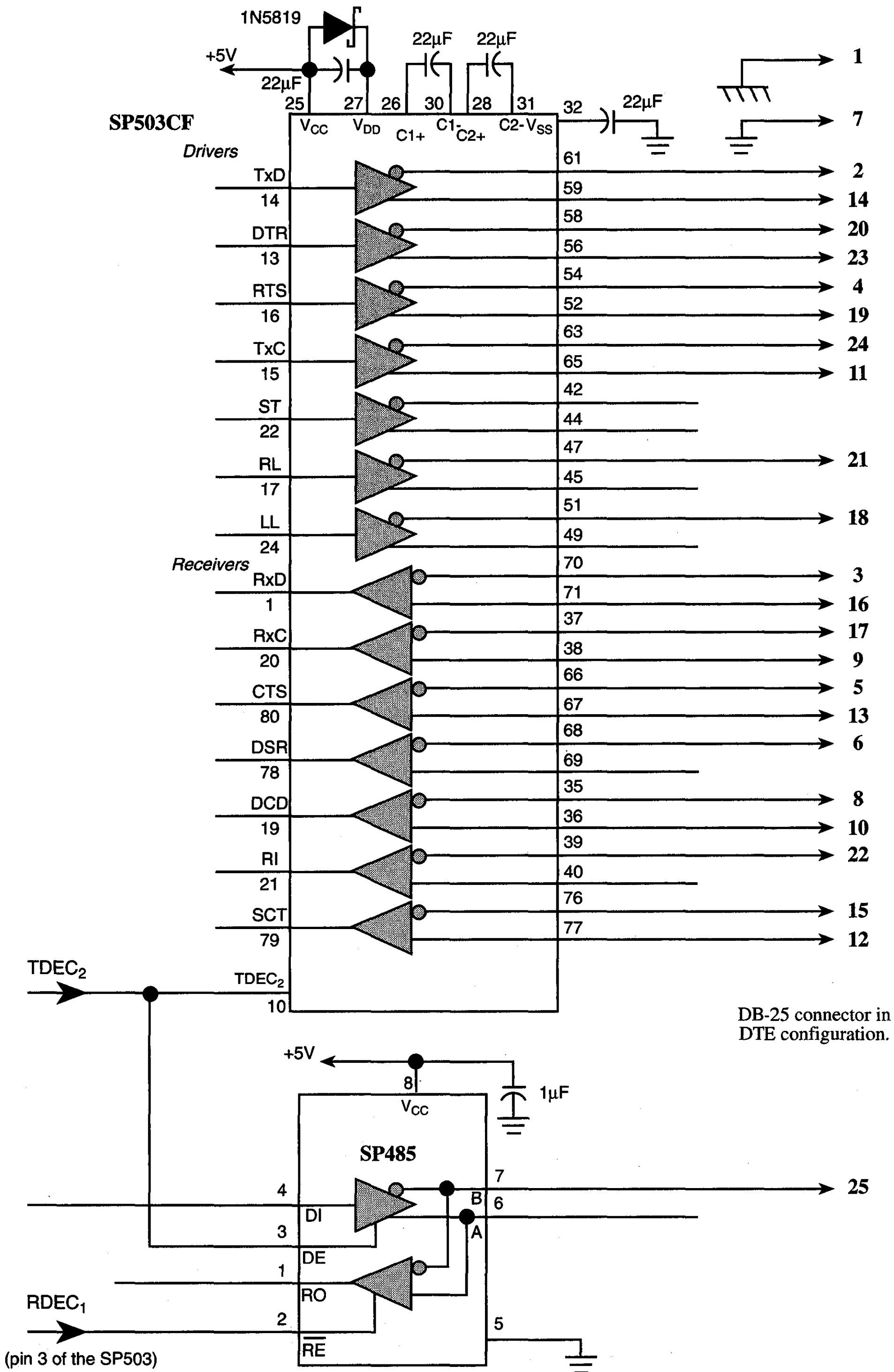
AVX Corporation • Myrtle Beach, SC • 803-448-9411

The drawing on page 122 shows the **SP503** configured with the ProTek LCA12C TVS devices to protect the drivers and receivers from ESD and over-voltage.

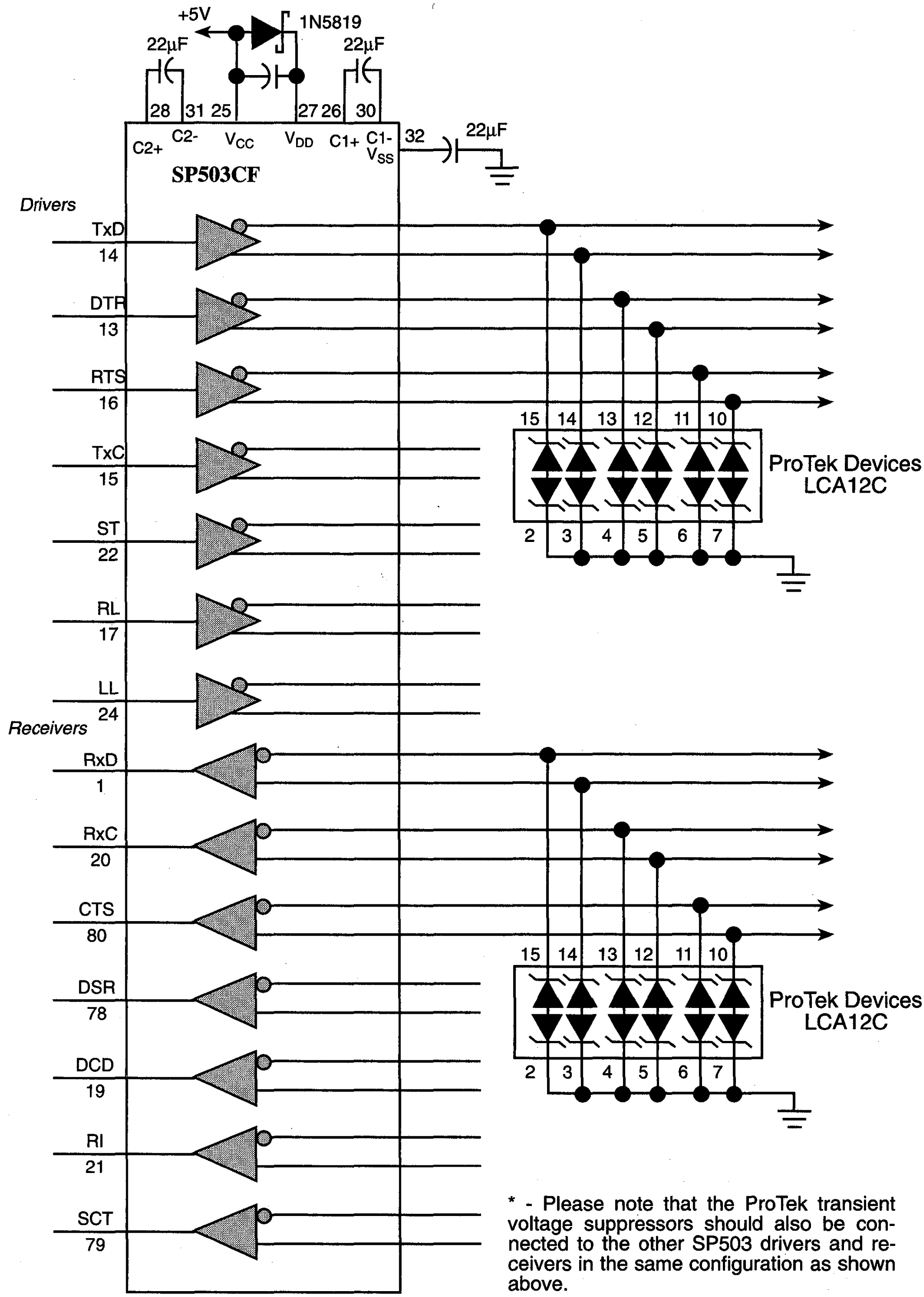
Creating extra RS-232 channels using the SP310A



Creating extra differential channels using the SP485



DB-25 connector in DTE configuration.



* - Please note that the ProTek transient voltage suppressors should also be connected to the other SP503 drivers and receivers in the same configuration as shown above.

ORDERING INFORMATION

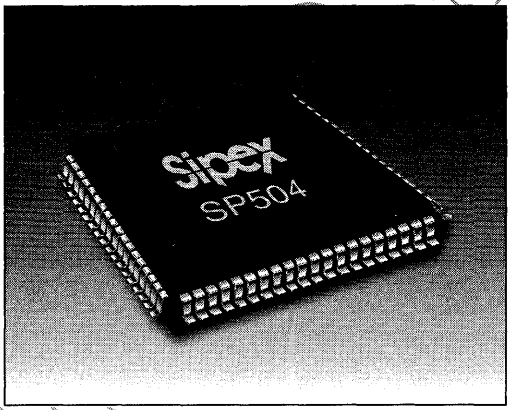
Model	Temperature Range	Package Types
SP503CF	0°C to +70°C	80–pin QFP

THIS PAGE LEFT INTENTIONALLY BLANK

SP504

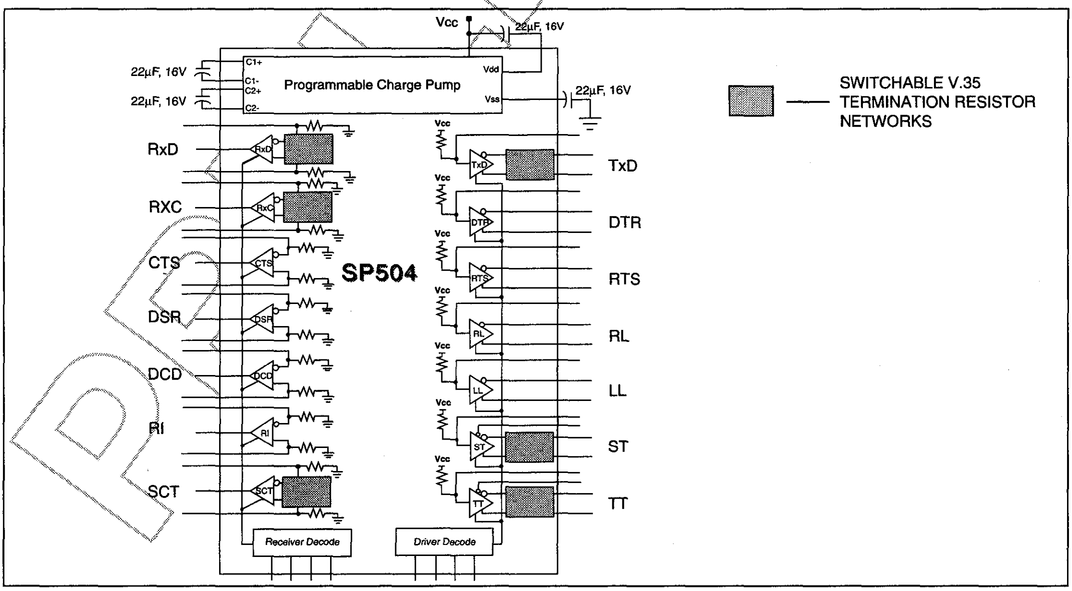
WAN Multi-Mode Serial Transceiver

- +5V Only
- Seven (7) Drivers and Seven (7) Receivers
- Driver and Receiver Tri-State Control
- Reduced V.35 Termination Network
- Pin Compatible with the SP503
- Software Selectable Interface Modes:
  - -RS-232E (V.28)
  - -RS-422A (V.11, X.27)
  - -RS-449
  - -RS-485
  - -V.35
  - -EIA-530
  - -EIA-530A
  - -V.36



DESCRIPTION...

The **SP504** is a single chip device that supports eight (8) of the most popular serial interface standards for Wide Area Network Connectivity. The **SP504** is fabricated using a low power BiCMOS process technology, and incorporates a Sipex patented (5,306,954) charge pump allowing +5V only operation. Seven (7) drivers and seven (7) receivers can be configured via software for any of the above interface modes at any time. The **SP504** requires only one external resistor per V.35 driver for compliant V.35 operation.



SPECIFICATIONS

Typical @ 25°C and nominal supply voltages unless otherwise noted.

	MIN.	TYP.	MAX.	UNITS	CONDITIONS
LOGIC INPUTS					
V_{IL}			0.8	Volts	
V_{IH}	2.0			Volts	
LOGIC OUTPUTS					
V_{OL}			0.4	Volts	I_{OUT}= -3.2mA
V_{OH}	2.4			Volts	I_{OUT}= 1.0mA
RS-485 DRIVER					
TTL Input Levels					
V_{IL}			0.8	Volts	
V_{IH}	2.0			Volts	
Outputs					
High Level Output			+6.0	Volts	
Low level Output	–0.3			Volts	
Differential Output	±1.5		±5.0	Volts	R_L=54Ω, C_L=50pF
Balance		±0.2		Volts	$\|V_T\| - \|\overline{V_T}\|$
Offset		+2.5		Volts	
Open Circuit Voltage			±6.0	Volts	
Output Current	28.0			mA	R_L=54Ω
Short Circuit Current		±250		mA	Terminated in –7V to +12V
Transition Time			120	ns	Rise/fall time, 10%–90%
Transmission Rate			10	Mbps	R_L=54Ω
Propagation Delay					
t_{PHL}		100		ns	Figures 3a and 5; R_{DIFF}=54Ω
t_{PLH}		100		ns	C_{RL}=50pF
RS-485 RECEIVER					
TTL Output Levels					
V_{OL}			0.4	Volts	
V_{OH}	2.4			Volts	
Input					
High Threshold	+0.2		+12	Volts	(a)-(b)
Low Threshold	–7.0		–0.2	Volts	(a)-(b)
Common Mode Range	–7.0		+12.0	Volts	
High Input Current					Refer to Rec. input graph
Low Input Current					Refer to Rec. input graph
Receiver Sensitivity			±0.2	Volts	Over –7V to +12V common mode range
Input Impedance	12			KΩ	
Transmission Rate			10	Mbps	
Propagation Delay					
t_{PHL}		100		ns	Figures 3a and 7; A is inverting and B is non-inverting.
t_{PLH}		100		ns	
V.35 DRIVER					
TTL Input Levels					
V_{IL}			0.8	Volts	
V_{IH}	2.0			Volts	
Outputs					
Differential Output	±0.44		±0.66	Volts	R_L=100Ω
Source Impedance	50	100	150	Ω	
Short-Circuit Impedance	135	150	165	Ω	V_{OUT} = +2V to –2V; w/ 150Ω termination to GND.
Voltage Output Offset	–0.6		+0.6		
Transition Time		40		ns	
Transmission Rate			5	Mbps	R_L=100Ω
Propagation Delay					
t_{PHL}		200		ns	Figures 3b and 5
t_{PLH}		200		ns	

SPECIFICATIONS (Continued)

Typical @ 25°C and nominal supply voltages unless otherwise noted.

	MIN.	TYP.	MAX.	UNITS	CONDITIONS
V.35 RECEIVER					
TTL Output Levels					
V_{OL}			0.4	Volts	
V_{OH}	2.4			Volts	
Input					
Differential Threshold	-0.2		+0.2	Volts	
Input Impedance	90	100	110	Ω	
Short-Circuit Impedance	135	150	165	Ω	V_{IN} = +2V to −2V
Transmission Rate			5	Mbps	
Propagation Delay					
t_{PHL}		200		ns	Figure 3b and 7; A is inverting
t_{PLH}		200		ns	and B is non-inverting.
RS-422 DRIVER					
TTL Input Levels					
V_{IL}			0.8	Volts	
V_{IH}	2.0			Volts	
Outputs					
Differential Output	±2.0		±5.0	Volts	R_L=100Ω
Open Circuit Voltage, V_O			±6.0	Volts	
Balance			±0.4	Volts	$\lvert V_T \rvert - \lvert \overline{V_T} \rvert$
Offset			+3.0	Volts	
Short Circuit Current			±150	mA	V_{out} = 0V
Power Off Current			±100	µA	V_{cc} = 0V, V_{out} = ±0.25V
Transition Time			60	ns	Rise/fall time, 10%-90%
Transmission Rate			10	Mbps	R_L=100Ω
Propagation Delay					
t_{PHL}		100		ns	Figure 3a and 5;
t_{PLH}		100		ns	R_{DIFF}=100Ω
RS-422 RECEIVER					
TTL Output Levels					
V_{OL}			0.4	Volts	
V_{OH}	2.4			Volts	
Input					
High Threshold	+0.2		+6.0	Volts	(a)-(b)
Low Threshold	−6.0		−0.2	Volts	(a)-(b)
Common Mode Range	−7.0		+7.0	Volts	
High Input Current					Refer to Rec. input graph
Low Input Current					Refer to Rec. input graph
Receiver Sensitivity			±0.2	Volts	
Input Impedance	4			KΩ	
Transmission Rate			10	Mbps	
Propagation Delay					
t_{PHL}		100		ns	Figure 3a and 7; A is inverting
t_{PLH}		100		ns	and B is non-inverting.
RS-232 DRIVER					
TTL Input Level					
V_{IL}			0.8	Volts	
V_{IH}	2.0			Volts	
Outputs					
High Level Output	+5.0		+15	Volts	R_L=3KΩ, V_{IN}=0.8V
Low Level Output	−15.0		−5.0	Volts	R_L=3KΩ, V_{IN}=2.0V
Open Circuit Voltage	−15		+15	Volts	
Short Circuit Current			±100	mA	V_{OUT} = 0V
Power Off Impedance	300			Ω	V_{cc} = 0V, V_{out} = ±2.0V
Slew Rate			30	V/µs	R_L=3KΩ, C_L= 50pF
Transition Time			1.56	µs	R_L=3KΩ, C_L=2500pF between ±3V

SPECIFICATIONS (Continued)

Typical @ 25°C and nominal supply voltages unless otherwise noted.

	MIN.	TYP.	MAX.	UNITS	CONDITIONS
RS-232 DRIVER					
Transmission Rate			120	Kbps	R_L=3KΩ, C_L=2500pF
Propagation Delay					
t_{PHL}		2	8	µS	Measured from 1.5V of V_{IN}
t_{PLH}		2	8	µS	to 50% of V_{OUT}; R_L=3KΩ
RS-232 RECEIVER					
TTL Output Levels					
V_{OL}			0.4	Volts	
V_{OH}	2.4			Volts	
Input					
High Threshold		1.7	3.0	Volts	
Low Threshold	0.8	1.2		Volts	
Receiver Open Circuit Bias	0		+2.0	Volts	
Input Impedance	3	5	7	KΩ	
Transmission Rate			120	Kbps	
Propagation Delay					
t_{PHL}			1	µS	Measured from 50% of V_{IN}
t_{PLH}			1	µS	to 1.5V of V_{OUT}.
RS-423 DRIVER					
TTL Input Levels					
V_{IL}			0.8	Volts	
V_{IH}	2.0			Volts	
Output					
High Level Output	+3.6		+6.0	Volts	R_L=450Ω
Low Level Output	–6.0		–3.6	Volts	R_L=450Ω
Open Circuit Voltage	±4.0		±6.0	Volts	
Short Circuit Current			±150	mA	V_{OUT} = 0V
Power Off Current			±100	µA	V_{CC} = 0V, V_{OUT}= ±0.25V
Transition Time			2.4	µs	Rise/fall time, between ±3V
Transmission Rate			120	Kbps	R_L=450Ω
Propagation Delay					
t_{PHL}		2	8	µS	Measured from 1.5V of V_{IN}
t_{PLH}		2	8	µS	to 50% of V_{OUT}; R_L=450Ω
RS-423 RECEIVER					
TTL Output Levels					
V_{OL}			0.4	Volts	
V_{OH}	2.4			Volts	
Input					
High Threshold	+0.2		+7.0	Volts	
Low Threshold	–7.0		–0.2	Volts	
Common Mode Range	–7.0		+7.0	Volts	
High Input Current					Refer to Rec. input graph
Low Input Current					Refer to Rec. input graph
Receiver Sensitivity			±0.2	Volts	V_{CM} = +7V to -7V
Input Impedance	4			KΩ	V_{IN} = +10V to -10V
Transmission Rate			120	Kbps	
Propagation Delay					
t_{PHL}			1	µS	Measured from 50% of V_{IN}
t_{PLH}			1	µS	to 1.5V of V_{OUT}
POWER REQUIREMENTS					
V_{CC}	4.75	5.00	5.25	Volts	
I_{CC}		30		mA	V_{CC}=5V; no interface selected
ENVIRONMENTAL AND MECHANICAL					
Operating Temperature Range	0		+70	°C	
Storage Temperature Range	–65		+150	°C	
Package		80–pin QFP			

OTHER AC CHARACTERISTICS

(Typical @ 25°C and nominal supply voltages unless otherwise noted)

PARAMETER	MIN.	TYP.	MAX.	UNITS	CONDITIONS
DRIVER DELAY TIME BETWEEN ACTIVE MODE AND TRI-STATE MODE					
RS-232 MODE					
t_{PZL}; Tri-state to Output low		800		ns	C_L = 100pF, Fig. 4 ; S_2 closed
t_{PZH}; Tri-state to Output high		400		ns	C_L = 100pF, Fig. 4 ; S_2 closed
t_{PLZ}; Output low to Tri-state		200		ns	C_L = 100pF, Fig. 4 ; S_2 closed
t_{PHZ}; Output high to Tri-state		400		ns	C_L = 100pF, Fig. 4 ; S_2 closed
RS-423 MODE					
t_{PZL}; Tri-state to Output low		200		ns	C_L = 100pF, Fig. 4 ; S_2 closed
t_{PZH}; Tri-state to Output high		200		ns	C_L = 100pF, Fig. 4 ; S_2 closed
t_{PLZ}; Output low to Tri-state		200		ns	C_L = 100pF, Fig. 4 ; S_2 closed
t_{PHZ}; Output high to Tri-state		200		ns	C_L = 100pF, Fig. 4 ; S_2 closed
RS-422, RS-485 MODES					
t_{PZL}; Tri-state to Output low		3000		ns	C_L = 100pF, Fig. 4 & 6; S_1 closed
t_{PZH}; Tri-state to Output high		150		ns	C_L = 100pF, Fig. 4 & 6; S_2 closed
t_{PLZ}; Output low to Tri-state		150		ns	C_L = 15pF, Fig. 4 & 6; S_1 closed
t_{PHZ}; Output high to Tri-state		200		ns	C_L = 15pF, Fig. 4 & 6; S_2 closed
V.35 MODE					
t_{PZL}; Tri-state to Output low		3000		ns	C_L = 100pF, Fig. 4 & 6; S_1 closed
t_{PZH}; Tri-state to Output high		150		ns	C_L = 100pF, Fig. 4 & 6; S_2 closed
t_{PLZ}; Output low to Tri-state		150		ns	C_L = 15pF, Fig. 4 & 6; S_1 closed
t_{PHZ}; Output high to Tri-state		150		ns	C_L = 15pF, Fig. 4 & 6; S_2 closed
RECEIVER DELAY TIME BETWEEN ACTIVE MODE AND TRI-STATE MODE					
RS-232 MODE					
t_{PZL}; Tri-state to Output low		100		ns	C_L = 100pF, Fig. 2 ; S_1 closed
t_{PZH}; Tri-state to Output high		100		ns	C_L = 100pF, Fig. 2 ; S_2 closed
t_{PLZ}; Output low to Tri-state		100		ns	C_L = 100pF, Fig. 2 ; S_1 closed
t_{PHZ}; Output high to Tri-state		100		ns	C_L = 100pF, Fig. 2 ; S_2 closed
RS-423 MODE					
t_{PZL}; Tri-state to Output low		100		ns	C_L = 100pF, Fig. 2 ; S_1 closed
t_{PZH}; Tri-state to Output high		100		ns	C_L = 100pF, Fig. 2 ; S_2 closed
t_{PLZ}; Output low to Tri-state		100		ns	C_L = 100pF, Fig. 2 ; S_1 closed

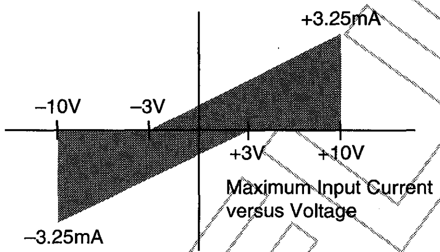
OTHER AC CHARACTERISTICS (Continued)

(Typical @ 25°C and nominal supply voltages unless otherwise noted)

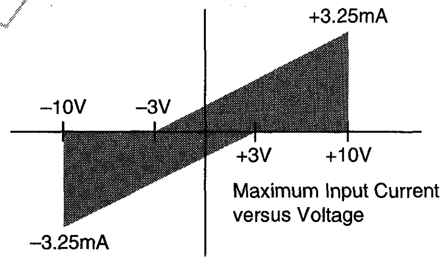
PARAMETER	MIN.	TYP.	MAX.	UNITS	CONDITIONS
RECEIVER DELAY TIME BETWEEN ACTIVE MODE AND TRI-STATE MODE					
t_{PHZ}; Output high to Tri-state		100		ns	C_L = 100pF, Fig. 2 ; S_2 closed
RS-422/RS-485 MODES					
t_{PZL}; Tri-state to Output low		100		ns	C_L = 100pF, Fig. 2 & 8 ; S_1 closed
t_{PZH}; Tri-state to Output high		100		ns	C_L = 100pF, Fig. 2 & 8 ; S_2 closed
t_{PLZ}; Output low to Tri-state		100		ns	C_L = 15pF, Fig. 2 & 8 ; S_1 closed
t_{PHZ}; Output high to Tri-state		100		ns	C_L = 15pF, Fig. 2 & 8; S_2 closed
V.35 MODE					
t_{PZL}; Tri-state to Output low		100		ns	C_L = 100pF, Fig. 2 & 8; S_1 closed
t_{PZH}; Tri-state to Output high		100		ns	C_L = 100pF, Fig. 2 & 8; S_2 closed
t_{PLZ}; Output low to Tri-state		100		ns	C_L = 15pF, Fig. 2 & 8; S_1 closed
t_{PHZ}; Output high to Tri-state		100		ns	C_L = 15pF, Fig. 2 & 8; S_2 closed

RECEIVER INPUT GRAPHS

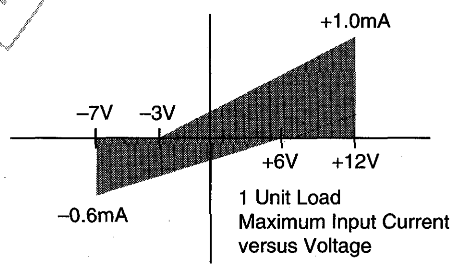
RS-422 RECEIVER



RS-423 RECEIVER



RS-485 RECEIVER



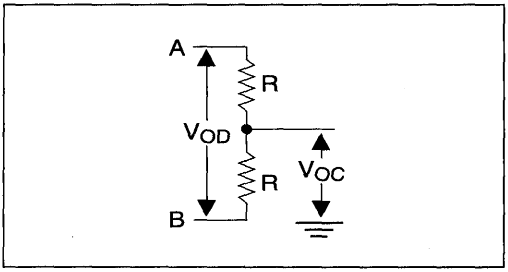


Figure 1. Driver DC Test Load Circuit

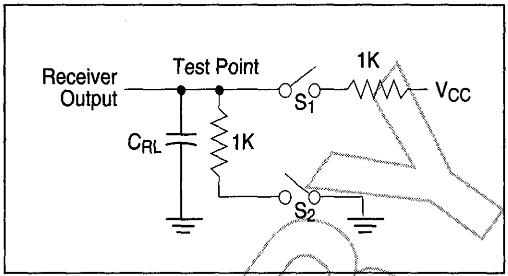


Figure 2. Receiver Timing Test Load Circuit

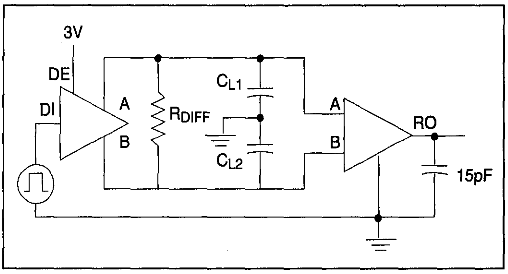


Figure 3a. Driver/Receiver Timing Test Circuit

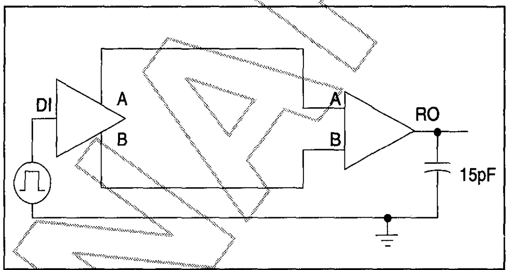


Figure 3b. Timing Test Ckt. (V.35 mode only for SP504)

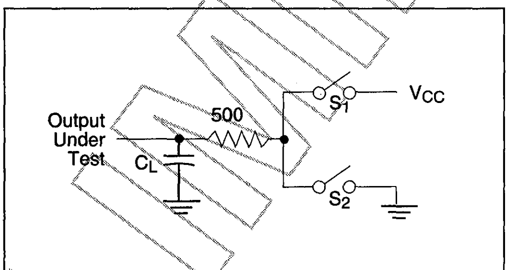


Figure 4. Driver Timing Test Load #2 Circuit

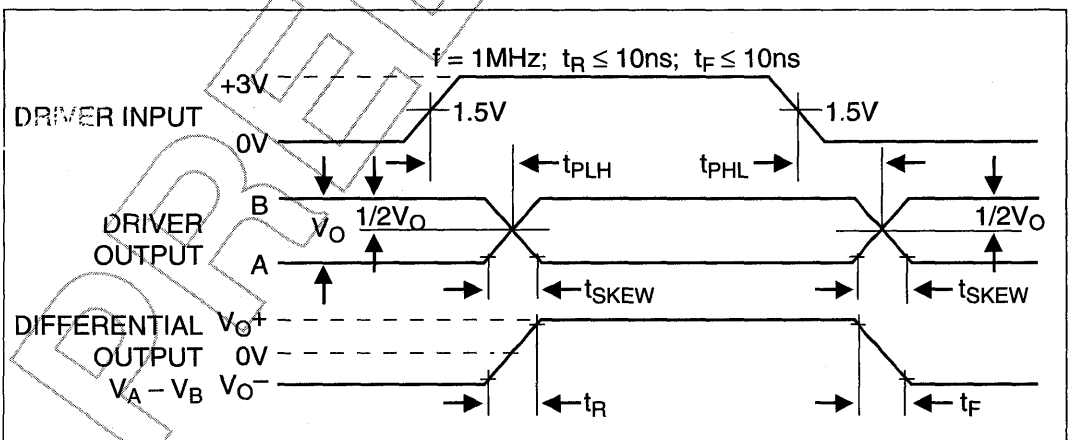


Figure 5. Driver Propagation Delays

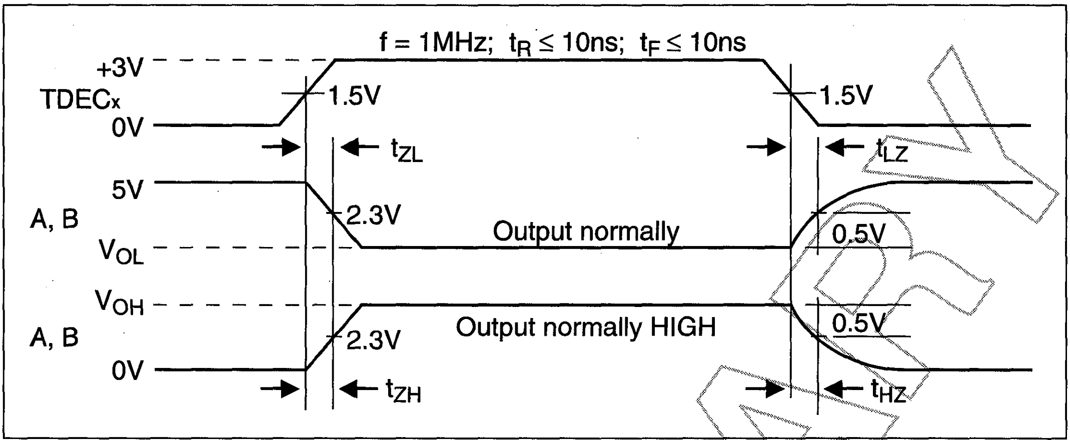


Figure 6. Driver Enable and Disable Times

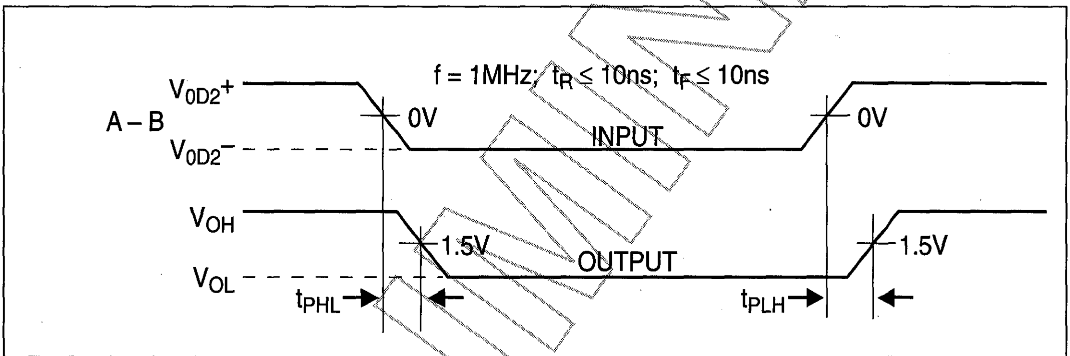


Figure 7. Receiver Propagation Delays

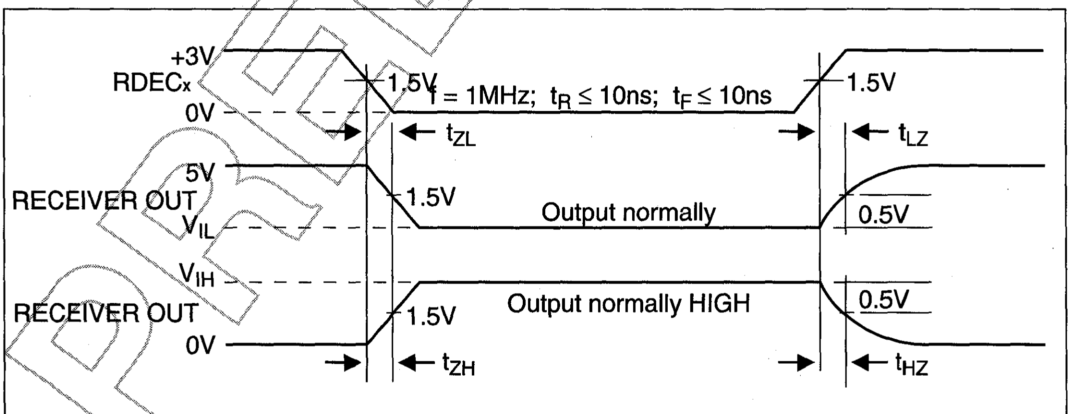


Figure 8. Receiver Enable and Disable Times

ABSOLUTE MAXIMUM RATINGS

These are stress ratings only and functional operation of the device at these ratings or any other above those indicated in the operation sections of the specifications below is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

V_{CC} ....+7V

Input Voltages:

- Logic .... -0.3V to (V_{CC}+0.5V)
- Drivers .... -0.3V to (V_{CC}+0.5V)
- Receivers .... ±15V

Output Voltages:

- Logic .... -0.3V to (V_{CC}+0.5V)
- Drivers .... ±14V
- Receivers .... -0.3V to (V_{CC}+0.5V)

Storage Temperature .... -65°C to +150°C

Power Dissipation 2000mW

Package Derating:

- $Ø_{JA}$ .... 46 °C/W
- $Ø_{JC}$ .... 16°C/W

STORAGE CONSIDERATIONS

Due to the relatively large package size of the 80-pin quad flat-pack, storage in a low humidity environment is preferred. Large high density plastic packages are moisture sensitive and should be stored in Vapor Barrier Bags. Prior to usage, the parts should remain bagged and stored below 40°C and 60%RH. If the parts are removed from the bag, they should be used within 48 hours or stored in an environment at or below 20%RH. If the above conditions cannot be followed, the parts should be baked for four hours at 125°C in order to remove moisture prior to soldering. Sipex ships the 80-pin QFP in Vapor Barrier Bags with a humidity indicator card and desiccant pack. The humidity indicator should be below 30%RH.

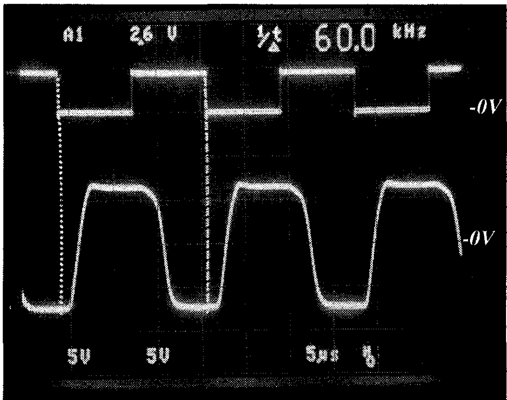


Figure 9. Typical RS-232 Driver Output Waveform

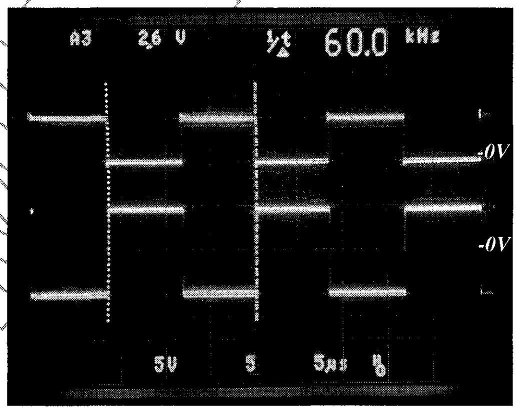


Figure 10. Typical RS-423 Driver Output Waveform

Figure 11. Typical RS-422/485 Driver Output Waveform

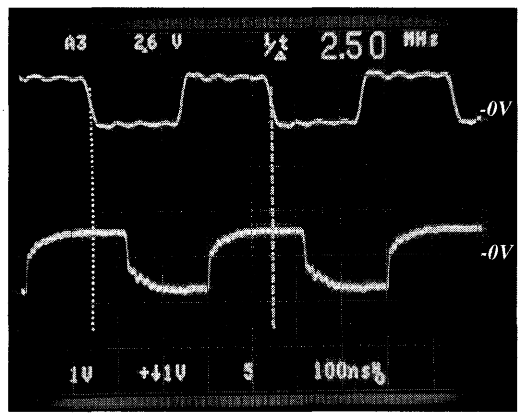
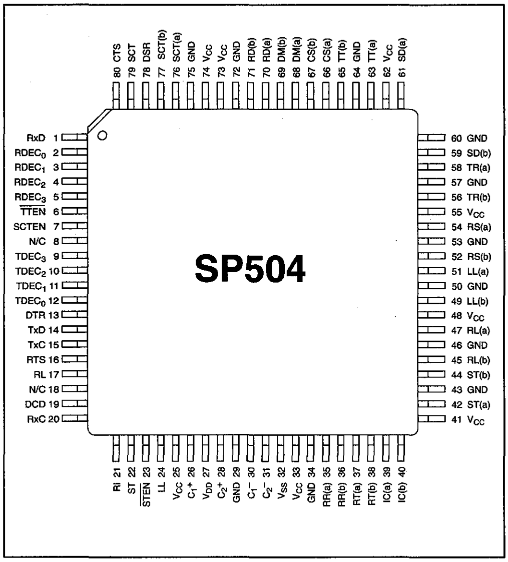


Figure 12. Typical V.35 Driver Output Waveform

PINOUT...



PIN ASSIGNMENTS...
CLOCK AND DATA GROUP

Pin 1 — RxD — Receive Data; TTL output, sourced from RD(a) and RD(b) inputs.

Pin 14 — TxD — TTL input ; transmit data source for SD(a) and SD(b) outputs.

Pin 15 — TxC — Transmit Clock; TTL input for TT driver outputs.

Pin 20 — RxC — Receive Clock; TTL output sourced from RT(a) and RT(b) inputs.

Pin 22 — ST — Send Timing; TTL input; source for ST(a) and ST(b) outputs.

Pin 37 — RT(a) — Receive Timing; analog input, inverted; source for RxC.

Pin 38 — RT(b) — Receive Timing; analog input, non-inverted; source for RxC.

Pin 42 — ST(a) — Send Timing; analog output, inverted; sourced from ST.

Pin 44 — ST(b) — Send Timing; analog output, non-inverted; sourced from ST.

Pin 59 — SD(b) — Analog Out — Send data, non-inverted; sourced from TxD.

Pin 61 — SD(a) — Analog Out — Send data, inverted; sourced from TxD.

Pin 63 — TT(a) — Analog Out — Terminal Timing, inverted; sourced from TxC

Pin 65 — TT(b) — Analog Out — Terminal Timing, non–inverted; sourced from TxC.

Pin 70 — RD(a) — Receive Data, analog input; inverted; source for RxD.

Pin 71 — RD(b) — Receive Data; analog input; non-inverted; source for RxD.

Pin 76 — SCT(a) — Serial Clock Transmit; analog input, inverted; source for SCT.

Pin 77 — SCT(b) — Serial Clock Transmit: analog input, non–inverted; source for SCT

Pin 79 — SCT — Serial Clock Transmit; TTL output; sources from SCT(a) and SCT(b) inputs.

CONTROL LINE GROUP

Pin 13 — DTR — Data Terminal Ready; TTL input; source for TR(a) and TR(b) outputs.

Pin 16 — RTS — Ready To Send; TTL input; source for RS(a) and RS(b) outputs.

Pin 17 — RL — Remote Loopback; TTL input; source for RL(a) and RL(b) outputs.

Pin 19 — DCD— Data Carrier Detect; TTL output; sourced from RR(a) and RR(b) inputs.

Pin 21 — RI — Ring In; TTL output; sourced from IC(a) and IC(b) inputs.

Pin 24 — LL — Local Loopback; TTL input; source for LL(a) and LL(b) outputs.

Pin 35 — RR(a)— Receiver Ready; analog input, inverted; source for DCD.

Pin 36 — RR(b)— Receiver Ready; analog input, non-inverted; source for DCD.

Pin 39 — IC(a)— Incoming Call; analog input, inverted; source for RI.

Pin 40 — IC(b)— Incoming Call; analog input,non-inverted; source for RI.

Pin 45 — RL(b) — Remote Loopback; analog output, non-inverted; sourced from RL.

Pin 47 — RL(a) — Remote Loopback; analog output inverted; sourced from RL.

Pin 49— LL(b) — Local Loopback; analog output, non-inverted; sourced from LL.

Pin 51 — LL(a) — Local Loopback; analog output, inverted; sourced from LL.

Pin 52 — RS(b) — Ready To Send; analog output, non-inverted; sourced from RTS.

Pin 54 — RS(a) — Ready To Send; analog output, inverted; sourced from RTS.

Pin 56 — TR(b) — Terminal Ready; analog output, non-inverted; sourced from DTR.

Pin 58 — TR(a) — Terminal Ready; analog output, inverted; sourced from DTR.

Pin 66 — CS(a)— Clear To Send; analog input, inverted; source for CTS.

Pin 67 — CS(b)— Clear To Send; analog input, non-inverted; source for CTS.

Pin 68 — DM(a)— Data Mode; analog input, inverted; source for DSR.

Pin 69 — DM(b)— Data Mode; analog input, non-inverted; source for DSR

Pin 78 — DSR— Data Set Ready; TTL output; sourced from DM(a), DM(b) inputs.

Pin 80 — CTS— Clear To Send; TTL output; sourced from CS(a) and CS(b) inputs.

CONTROL REGISTERS

Pins 2–5 — $RDEC_0$ – $RDEC_3$ — Receiver decode register; configures receiver modes; TTL inputs.

Pin 6 — $\overline{TTEN}$ — Enables TT driver, active low; TTL input.

Pin 7 — SCTEN — Enables SCT receiver; active high; TTL input.

Pins 12–9 — $TDEC_0$ – $TDEC_3$ — Transmitter decode register; configures transmitter modes; TTL inputs.

Pin 23 — $\overline{STEN}$ — Enables ST driver; active low; TTL input.

POWER SUPPLIES

Pins 25, 33, 41, 48, 55, 62, 73, 74 — V_{CC} — +5V input.

Pins 29, 34, 43, 46, 50, 53, 57, 60, 64, 72, 75 — GND — Ground.

Pin 27 — V_{DD} +10V Charge Pump Capacitor — Connects from V_{DD} to V_{CC}. Suggested capacitor size is 22μF, 16V.

Pin 32 — V_{SS} –10V Charge Pump Capacitor — Connects from ground to V_{SS}. Suggested capacitor size is 22μF, 16V.

Pins 26 and 30 — C_1^+ and C_1^- — Charge Pump Capacitor — Connects from C_1^+ to C_1^-. Suggested capacitor size is 22μF, 16V.

Pins 28 and 31 — C_2^+ and C_2^- — Charge Pump Capacitor — Connects from C_2^+ to C_2^-. Suggested capacitor size is 22μF, 16V.

NOTE: NC pins should be left floating; internal signals may be present.

FEATURES...

The **SP504** is a highly integrated serial transceiver that allows software control of its interface modes. Similar to the **SP503**, the **SP504** offers the same hardware interface modes for RS-232 (V.28), RS-422A (V.11), RS-449, RS-485, V.35, EIA-530 and includes V.36 and EIA-530A. The interface mode selection is done via an 8–bit switch; four (4) bits control the drivers and four (4) bits control the receivers. The **SP504** is fabricated using low–power BiCMOS process technology, and incorporates a **Sipex**–patented (5,306,954) charge pump allowing +5V only operation. Each device is packaged in an 80–pin Quad FlatPack package.

The **SP504** is ideally suited for wide area network connectivity based on the interface modes offered and the driver and receiver configurations. The **SP504** has seven (7) independent drivers and seven (7) independent receivers. In

V.35 mode, the **SP504** includes the necessary components and termination resistors internal within the device for compliant V.35 operation.

THEORY OF OPERATION

The **SP504** is made up of five separate circuit blocks — the charge pump, drivers, receivers, decoder and switching array. Each of these circuit blocks is described in more detail below.

Charge–Pump

The **SP504**'s charge pump design is based on the **SP503** where **Sipex**'s-patented charge pump design (5,306,954) uses a four–phase voltage shifting technique to attain symmetrical 10V power supplies. In addition, the **SP504** charge pump incorporates a "programmable" feature that produces an output of ±10V or ±5V for V_{SS} and V_{DD} depending on the mode of operation. The charge pump still requires external capacitors to store the charge. Figure 17a shows the waveform found on the positive side of capacitor C2, and Figure 17b shows the negative side of capcitor C2. There is a free–running oscillator that controls the four phases of the voltage shifting. A description of each phase follows.

The **SP504** charge pump is used for RS-232 where the output voltage swing is typically ±10V and also used for RS-423. However, RS-423 requires the voltage swing on the driver output be between ±4V to ±6V during an open-circuit (no load). The charge pump would need to be regulated down from ±10V to ±5V. A typical ±10V charge pump would require external clamping such as 5V zener diodes on V_{DD} and V_{SS} to ground. The ±5V output has symmetrical levels as in the ±10V output. The ±5V is used in the following modes where RS-423 levels are used: RS-449, EIA-530, EIA-530A and V.36.

Phase 1 (±10V)

— V_{SS} charge storage — During this phase of the clock cycle, the positive side of capacitors C_1 and C_2 are initially charged to +5V. C_1^+ is then switched to ground and the charge on C_1^- is transferred to C_2^-. Since C_2^+ is connected to +5V, the voltage potential across capacitor C_2 is now 10V.

Phase 1 (±5V)

— V_{SS} & V_{DD} charge storage and transfer — With the C_1 and C_2 capacitors initially charged to +5V, C_1^+ is then switched to ground and charge on C_1^- is transferred to the V_{SS} storage capacitor. Simultaneously the C_2^- is switched to ground and 5V charge on C_2^+ is transferred to the V_{DD} storage capacitor.

Phase 2 (±10V)

— V_{SS} transfer — Phase two of the clock connects the negative terminal of C_2 to the V_{SS} storage capacitor and the positive terminal of C_2 to ground, and transfers the generated –l0V or the generated –5V to C_3. Simultaneously, the positive side of capacitor C_1 is switched to +5V and the negative side is connected to ground.

Phase 2 (±5V)

— V_{SS} & V_{DD} charge storage — C_1^+ is reconnected to V_{CC} to recharge the C_1 capacitor. C_2^+ is switched to ground and C_2^- is connected to C_3. The 5V charge from Phase 1 is now transferred to the V_{SS} storage capacitor. V_{SS} receives a continuous charge from either C_1 or C_2. With the C1 capacitor charged to 5V, the cycle begins again.

Phase 3

— V_{DD} charge storage — The third phase of the

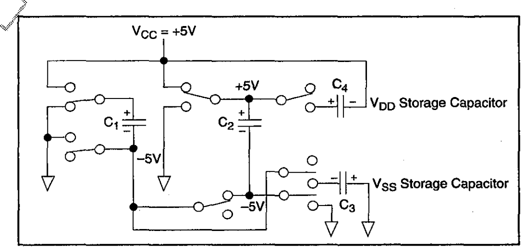


Figure 13a. Charge Pump Phase 1 for ±10V.

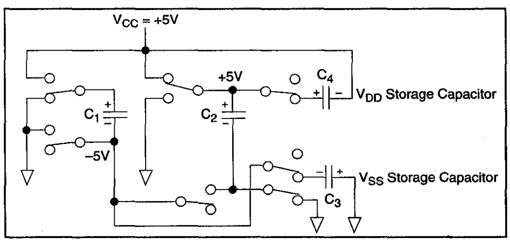


Figure 13b. Charge Pump Phase 1 for ±5V.

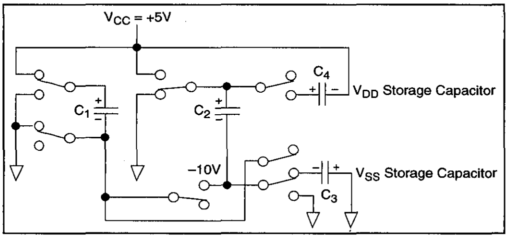


Figure 14a. Charge Pump Phase 2 for ±10V.

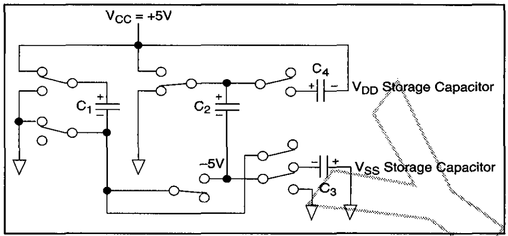


Figure 14b. Charge Pump Phase 2 for ±5V.

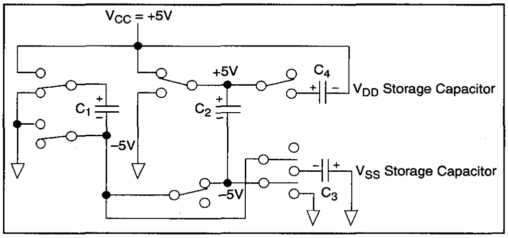


Figure 15. Charge Pump Phase 3.

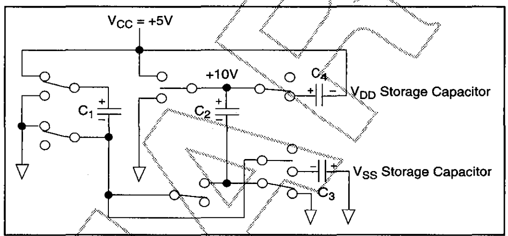


Figure 16. Charge Pump Phase 4.

clock is identical to the first phase — the charge transferred in C_1 produces –5V in the negative terminal of C_1, which is applied to the negative side of capacitor C_2. Since C_2^+ is at +5V, the voltage potential across C_2 is 10V. For the 5V output, C_2^+ is connected to ground so that the potential on C_2 is only +5V.

Phase 4

— V_{DD} transfer — The fourth phase of the clock connects the negative terminal of C_2 to ground and transfers the generated 10V or the generated 5V across C_2 to C_4, the V_{DD} storage capacitor. Again, simultaneously with this, the positive side of capacitor C_1 is switched to +5V and the negative side is connected to ground, and the cycle begins again.

Since both V_{DD} and V_{SS} are separately generated from V_{CC} in a no–load condition, V_{DD} and V_{SS} will be symmetrical. Older charge pump approaches that generate V^- from V^+ will show a decrease in the magnitude of V^- compared to V^+ due to the inherent inefficiencies in the design.

The clock rate for the charge pump typically operates at 15kHz. The external capacitors must

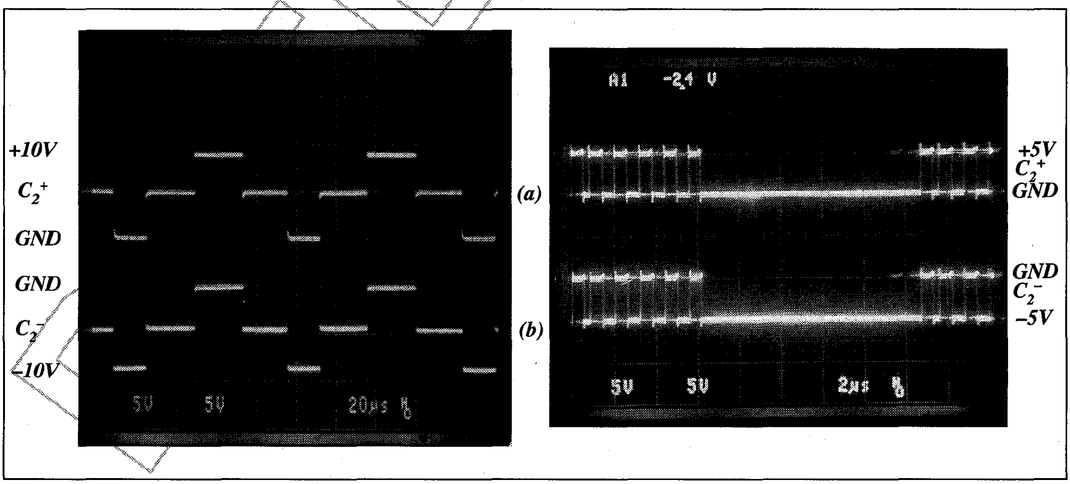


Figure 17. Charge Pump Waveforms

be a minimum of 22µF with a 16V breakdown rating.

External Power Supplies

For applications that do not require +5V only, external supplies can be applied at the V+ and V– pins. The value of the external supply voltages must be no greater than ±10.5V. The tolerance should be ±5% from ±10V. The current drain for the supplies is used for RS-232 and RS-423 drivers. For the RS-232 driver, the current requirement will be 3.5mA per driver. The RS-423 driver worst case current drain will be 11mA per driver. Power sequencing is required for the **SP504**. The supplies must be sequenced accordingly: +5V, +10V and –10V. It is important to prevent V_{SS} from starting up before V_{CC} or V_{DD}.

Drivers

The **SP504** has seven (7) enhanced independent drivers. Control for the mode selection is done via a four–bit control word. The drivers are pre-arranged such that for each mode of operation, the relative position and functionality of the drivers are set up to accommodate the selected interface mode. As the mode of the drivers is changed, the electrical characteristics will change to support the requirements of clock, data, and control line signal levels. *Table 1* shows the mode of each driver in the different interface modes that can be selected.

There are four basic types of driver circuits — RS-232, RS-423, RS-485 and V.35.

The RS-232 drivers output single–ended signals with a minimum of ±5V (with 3KΩ and 2500pF loading), and can operate up to 120Kbps. The RS-232 drivers are used in RS-232 mode for all signals, and also in V.35 mode where they are used as the control line signals such as DTR and RTS.

The RS-423 drivers are also single–ended signals with a minimum voltage output of ±3.6V (with 450Ω loading) and can operate up to 120Kbps. Open circuit V_{OL} and V_{OH} measurements are ±4.0V to ±6.0V. The RS-423 drivers are used in RS-449, EIA530, EIA-530A and V.36 modes as Category II signals from each of their corresponding specifications.

The third type of driver produces a differential signal that can maintain RS-485, ±1.5V differential output levels with a worst case load of 54Ω. The signal levels and drive capability of the RS-485 drivers allow the drivers to also support RS-422 (V.11) requirements of ±2V differential output levels with 100Ω loads. The RS-422 drivers are used in RS-449, EIA530, EIA-530A and V.36 modes as Category I signals which are used for clock and data.

The fourth type of driver is the V.35 driver. V.35 levels require ±0.55V driver output signals with a load of 100Ω. The **SP504** drivers simplify existing V.35 implementations that use external termination schemes. The drivers were specifically designed to comply with the requirements of V.35 as well as the driver output impedance values of V.35. The drivers achieve the 50Ω to 150Ω source impedance. However, an external 150Ω resistor to ground must be connected to the non- inverting outputs; SD(b), ST(b), and TT(b), in order to comply with the 135Ω to 165Ω short-circuit impedance for V.35. The V.35 driver is disabled and transparent when the decoder is in all other modes. All of the differential drivers; RS-485, RS-422, and V.35, can operate up to 10Mbps.

The driver inputs are both TTL or CMOS compatible. Each driver input contains a pull-down resistor to ground so that the output will be at a defined state. Unused driver inputs can be left floating.

Receivers

The **SP504** has seven (7) independent receivers which can be programmed for the different interface modes. Control for the mode selection is done via a 4–bit control word that is independent from the driver control word. The coding for the drivers and receivers is identical. Therefore, if the modes for the drivers and receivers are supposed to be identical in the application, the control lines can be tied together.

Like the drivers, the receivers are pre-arranged for the specific requirements of the interface. As the operating mode of the receivers is changed, the electrical characteristics will change to support the requirements of clock, data, and control line receivers. *Table 2* shows the mode of each receiver in the different interface modes that can be selected.

There are three basic types of receiver circuits — RS-232, RS-423, and RS-485.

The RS-232 receiver is a single–ended input with a threshold of 0.8V to 2.4V. The RS-232 receiver has an operating voltage range of ±15V and can receive signals up to 120Kbps. The input sensitivity complies with EIA-RS-232 and V.28 at +3V to -3V. The input impedance is 3kΩ to 7kΩ. RS-232 receivers are used in RS-232 mode for all data, clock and control signals. They are also used in V.35 mode for control line signals such as CTS and DSR. The RS-423 receivers are also single–ended but have an input threshold as low as ±200mV. The input impedance is guaranteed to be greater than 4KΩ, with an operating voltage range of ±7V. The RS-423 receivers can operate up to 120Kbps. RS423 receivers are used in RS-449, EIA530, EIA-530A and V.36 modes as Category II signals as indicated by their corresponding specifications.

The third type of receiver is a differential which supports RS-485. The RS-485 receiver has an input impedance of 15KΩ and a differential threshold of ±200mV. Since the characteristics of an RS-422 (V.11) receiver are actually subsets of RS-485, the receivers for RS-422 requirements are covered by the RS-485 receivers. RS-422 receivers are used in RS-449, EIA530, EIA-530A and V.36 as Category I signals for receiving clock, data, and some control line signals. The differential receivers can receive data up to 10Mbps.

The RS-485 receivers are also used for the V.35 mode. Unlike the older implementations of differential or V.35 receivers, the **SP504** contains an internal resistor termination network that ensures a V.35 input impedance of 100Ω (±10Ω) and a short-circuit impedance of 150Ω (±15Ω). The traditional V.35 implementations required external termination resistors to acheive the proper V.35 impedances. The internal network is connected via low on-resistance FET switches when the decoder is changed to V.35 mode. The termination network is transparent when all other modes are selected. The V.35 receivers can operate up to 10Mbps.

All receivers include a fail-safe feature that outputs a logic high when the receiver inputs are open. For single-ended RS-232 receivers, there are internal 5kΩ pull-down resistors on the inputs which produces a logic high ("1") at the receiver outputs. The single-ended RS-423 receivers produce a logic low ("0") on the output when the inputs are open. This is due to a pull-up device connected to the input. The differential receivers have the same internal pull-up device on the non-inverting input which produces a logic high ("1") at the receiver output. The three differential receivers when configured in V.35 mode (RxD, RxC & SCT) do not have fail-safe because the internal termination resistor network is connected.

Decoder

The **SP504** has the ability to change the interface mode of the drivers or receivers via an 8–bit switch. The decoder for the drivers and receivers is not latched; it is merely a combinational logic switch.

The control word can be externally latched either high or low to write the appropriate code into the **SP504**. The codes shown in *Tables 1 and 2* are the only specified, valid modes for the **SP504**. Undefined codes may represent other interface modes not specified (consult the factory for more information). The drivers are controlled with the data bits labeled $TDEC_3$–$TDEC_0$. Most of the drivers can be put into tri-state mode by writing 0000 to the driver decode switch. The three drivers TxD, ST and TxC, have a 150Ω pull-down resistor to ground connected at the (b) output. This resistor is part of the V.35 driver circuitry and is always connected regardless of mode. Tri-state is possible for all drivers in RS-232 mode. The receivers are controlled with data bits $RDEC_3$–$RDEC_0$; the code 0000 written to the receivers will place the outputs into tri-state mode. The 0000 decoder word will overide the enable control line for the one receiver (SCT).

SP504 Driver Mode Selection

Pin Label	Mode:	RS-232	V.35	RS-422	RS-485	RS-449	EIA-530	EIA-530A	V.36
$TDEC_3$–$TDEC_0$	0000	0010	1110	0100	0101	1100	1101	1111	0110
SD(a)	tri-state	RS-232	V.35–	RS-422–	RS-485–	RS-422–	RS-422–	RS-422–	RS-422–
SD(b)	tri-state	tri-state	V.35+	RS-422+	RS-485+	RS-422+	RS-422+	RS-422+	RS-422+
TR(a)	tri-state	RS-232	RS-232	RS-422–	RS-485–	RS-422–	RS-422–	RS-423	RS-423
TR(b)	tri-state	tri-state	tri-state	RS-422+	RS-485+	RS-422+	RS-422+	tri-state	tri-state
RS(a)	tri-state	RS-232	RS-232	RS-422–	RS-485–	RS-422–	RS-422–	RS-422–	RS-423
RS(b)	tri-state	tri-state	tri-state	RS-422+	RS-485+	RS-422+	RS-422+	RS-422+	tri-state
RL(a)	tri-state	RS-232	RS-232	RS-422–	RS-485–	RS-423	RS-423	RS-422-	RS-423
RL(b)	tri-state	tri-state	tri-state	RS-422+	RS-485+	tri-state	tri-state	RS-422+	tri-state
LL(a)	tri-state	RS-232	RS-232	RS-422–	RS-485–	RS-423	RS-423	RS-423	RS-423
LL(b)	tri-state	tri-state	tri-state	RS-422+	RS-485+	tri-state	tri-state	tri-state	tri-state
ST(a)	tri-state	RS-232	V.35-	RS-422–	RS-485–	RS-422–	RS-422–	RS-422–	RS-422–
ST(b)	tri-state	tri-state	V.35+	RS-422+	RS-485+	RS-422+	RS-422+	RS-422+	RS-422+
TT(a)	tri-state	RS-232	V.35–	RS-422–	RS-485–	RS-422–	RS-422–	RS-422–	RS-422-
TT(b)	tri-state	tri-state	V.35+	RS-422+	RS-485+	RS-422+	RS-422+	RS-422+	RS-422+

Table 1. Driver Mode Selection.

SP504 Receiver Mode Selection

Pin Label	Mode:	RS-232	V.35	RS-422	RS-485	RS-449	EIA-530	EIA-530A	V.36
$RDEC_3$–$RDEC_0$	0000	0010	1110	0100	0101	1100	1101	1111	0110
RD(a)	R_{out}=tri-state	RS-232	V.35–	RS-422–	RS-485–	RS-422–	RS-422–	RS-422–	RS-422–
RD(b)	R_{out}=tri-state	>12KΩ to GND	V.35+	RS-422+	RS-485+	RS-422+	RS-422+	RS-422+	RS-422+
RT(a)	R_{out}=tri-state	RS-232	V.35–	RS-422–	RS-485–	RS-422–	RS-422–	RS-422–	RS-422–
RT(b)	R_{out}=tri-state	>12KΩ to GND	V.35+	RS-422+	RS-485+	RS-422+	RS-422+	RS-422+	RS-422+
CS(a)	R_{out}=tri-state	RS-232	RS-232	RS-422–	RS-485–	RS-422–	RS-422–	RS-422–	RS-423
CS(b)	R_{out}=tri-state	>12KΩ to GND	>12KΩ to GND	RS-422+	RS-485+	RS-422+	RS-422+	RS-422+	>12KΩ to GND
DM(a)	R_{out}=tri-state	RS-232	RS-232	RS-422–	RS-485–	RS-422–	RS-422–	RS-423	RS-423
DM(b)	R_{out}=tri-state	>12KΩ to GND	>12KΩ to GND	RS-422+	RS-485+	RS-422+	RS-422+	>12KΩ to GND	>12KΩ to GND
RR(a)	R_{out}=tri-state	RS-232	RS-232	RS-422–	RS-485–	RS-422–	RS-422–	RS-422–	RS-423
RR(b)	R_{out}=tri-state	>12KΩ to GND	>12KΩ to GND	RS-422+	RS-485+	RS-422+	RS-422+	RS-422+	>12KΩ to GND
IC(a)	R_{out}=tri-state	RS-232	RS-232	RS-422–	RS-485–	RS-423	RS-423	RS-423	RS-423
IC(b)	R_{out}=tri-state	>12KΩ to GND	>12KΩ to GND	RS-422+	RS-485+	>12KΩ to GND	>12KΩ to GND	>12KΩ to GND	>12KΩ to GND
SCT(a)	R_{out}=tri-state	RS-232	V.35–	RS-422–	RS-485–	RS-422–	RS-422–	RS-422–	RS-422–
SCT(b)	R_{out}=tri-state	>12KΩ to GND	V.35+	RS-422+	RS-485+	RS-422+	RS-422+	RS-422+	RS-422+

Table 2. Receiver Mode Selection.

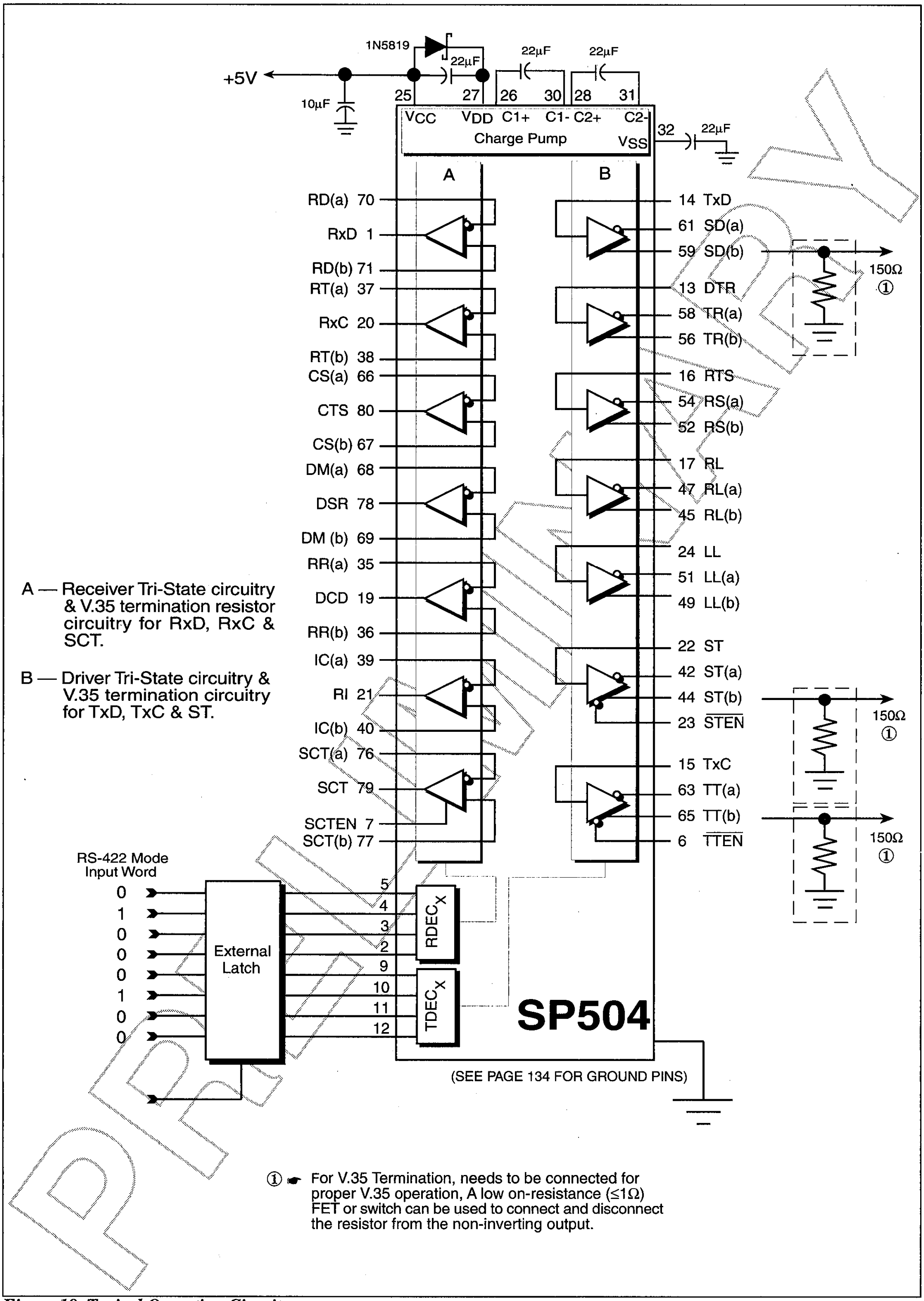
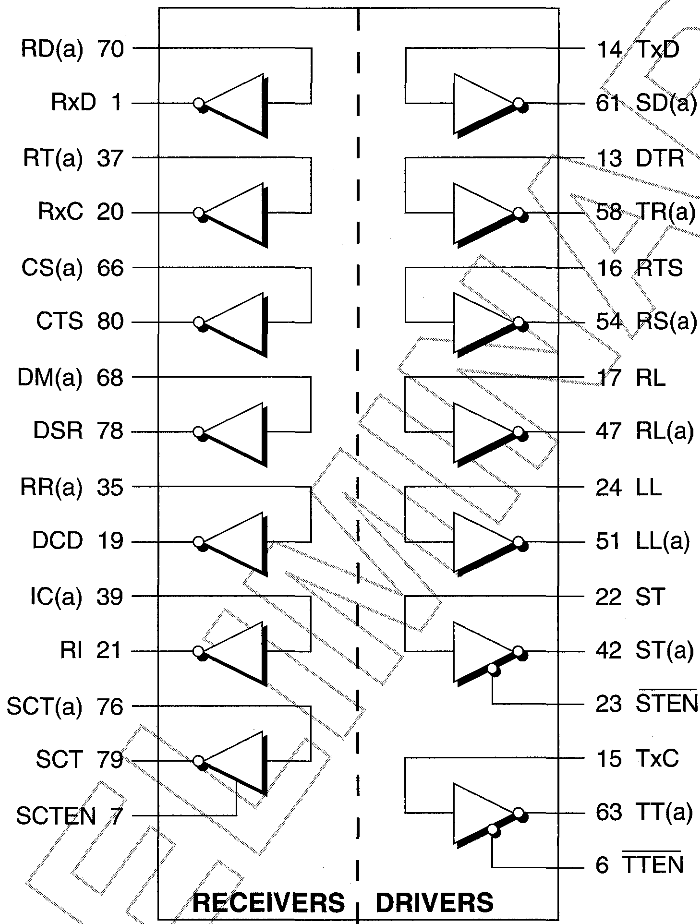


Figure 18. Typical Operation Circuit

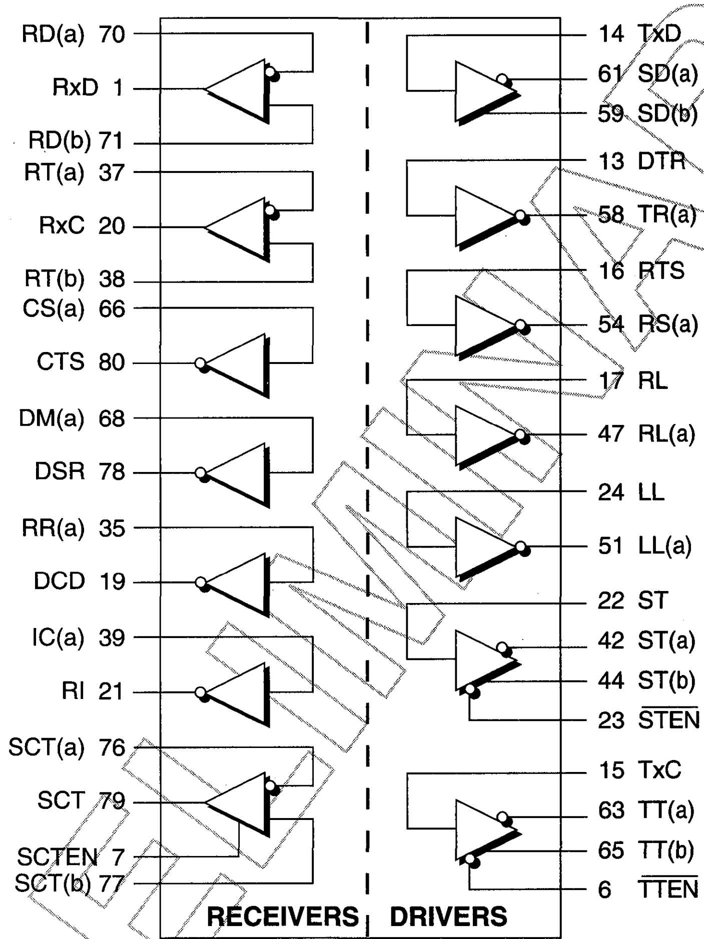
MODE: RS-232							
DRIVER				RECEIVER			
$TDEC_3$	$TDEC_2$	$TDEC_1$	$TDEC_0$	$RDEC_3$	$RDEC_2$	$RDEC_1$	$RDEC_0$
0	0	1	0	0	0	1	0



$\overline{STEN}$	ST	$\overline{TTEN}$	TT	SCTEN	SCT
1	Disabled	1	Disabled	1	Enabled
0	Enabled	0	Enabled	0	Disabled

Figure 19. Mode Diagram — RS-232

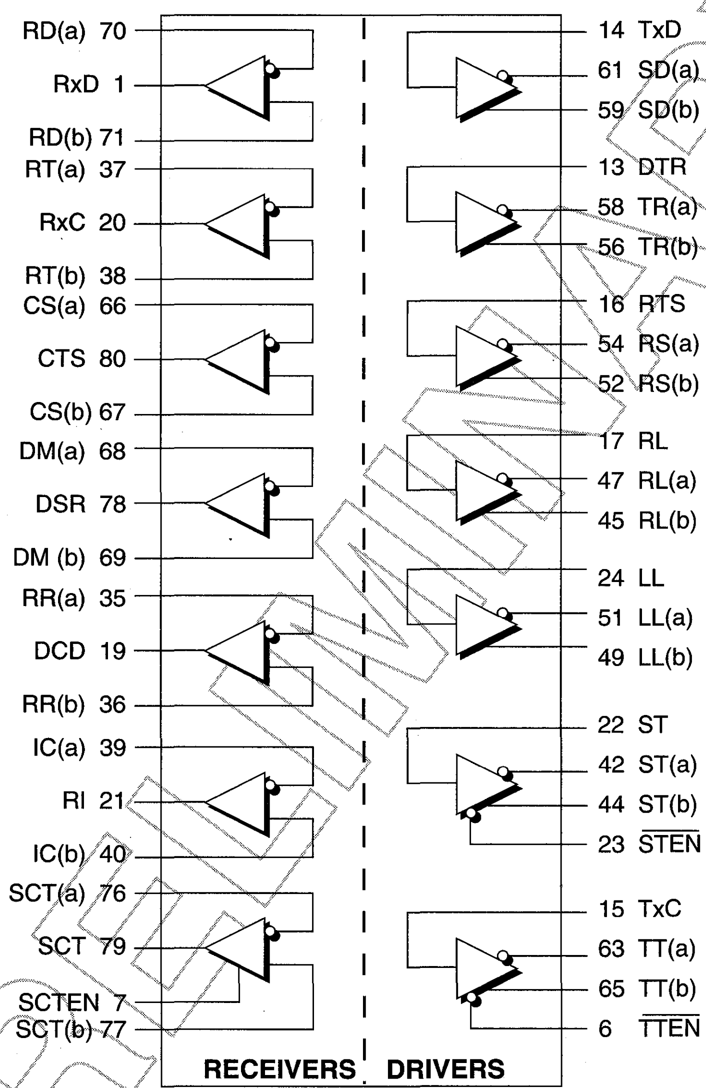
MODE: V.35							
DRIVER				RECEIVER			
$TDEC_3$	$TDEC_2$	$TDEC_1$	$TDEC_0$	$RDEC_3$	$RDEC_2$	$RDEC_1$	$RDEC_0$
1	1	1	0	1	1	1	0



$\overline{STEN}$	ST	$\overline{TTEN}$	TT	SCTEN	SCT
1	Disabled	1	Disabled	1	Enabled
0	Enabled	0	Enabled	0	Disabled

Figure 20. Mode Diagram — V.35

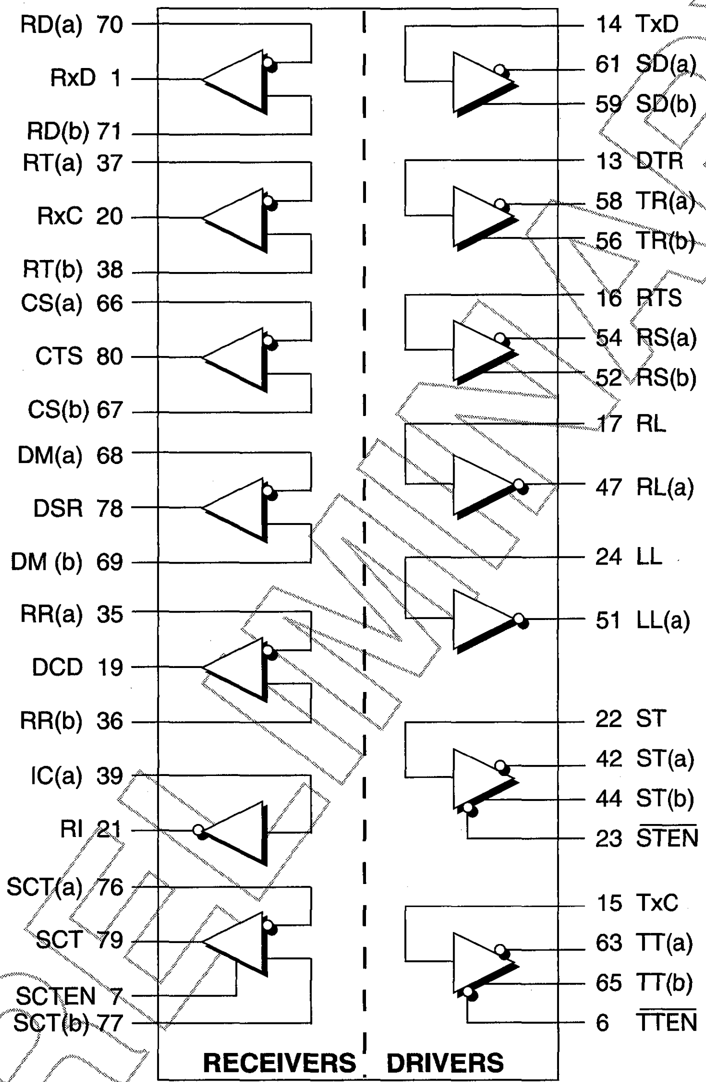
MODE: RS-422							
DRIVER				RECEIVER			
$TDEC_3$	$TDEC_2$	$TDEC_1$	$TDEC_0$	$RDEC_3$	$RDEC_2$	$RDEC_1$	$RDEC_0$
0	1	0	0	0	1	0	0



$\overline{STEN}$	ST	$\overline{TTEN}$	TT	SCTEN	SCT
1	Disabled	1	Disabled	1	Enabled
0	Enabled	0	Enabled	0	Disabled

Figure 21. Mode Diagram — RS-422

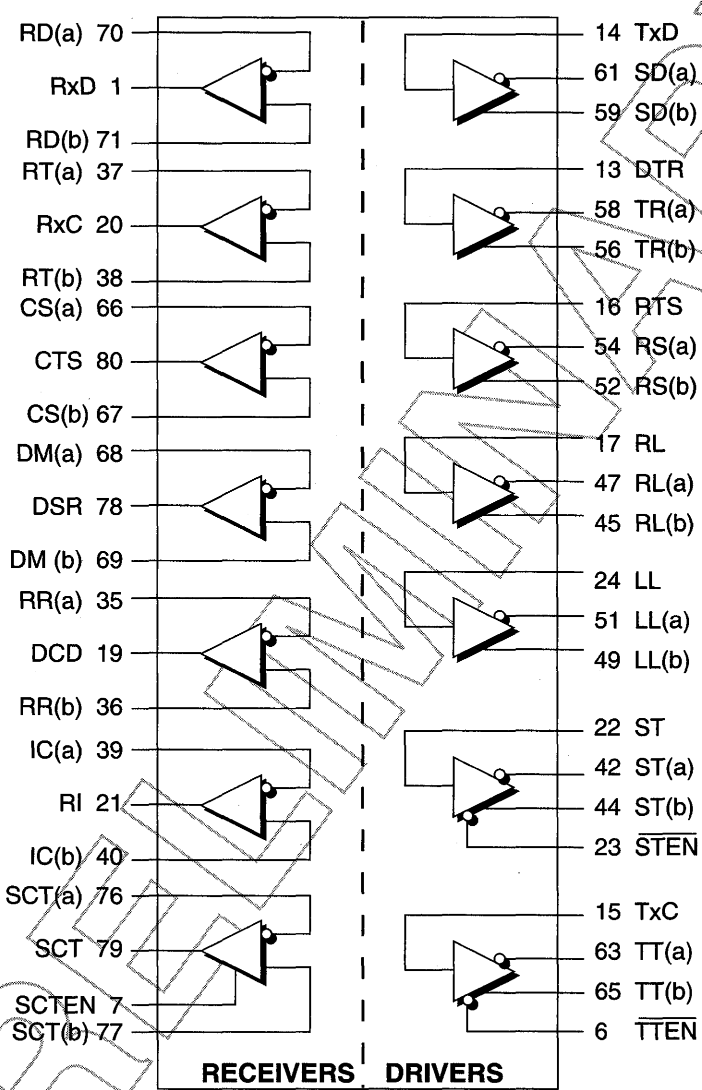
MODE: RS-449							
DRIVER				RECEIVER			
$TDEC_3$	$TDEC_2$	$TDEC_1$	$TDEC_0$	$RDEC_3$	$RDEC_2$	$RDEC_1$	$RDEC_0$
1	1	0	0	1	1	0	0



$\overline{STEN}$	ST	$\overline{TTEN}$	TT	SCTEN	SCT
1	Disabled	1	Disabled	1	Enabled
0	Enabled	0	Enabled	0	Disabled

Figure 22. Mode Diagram — RS-449

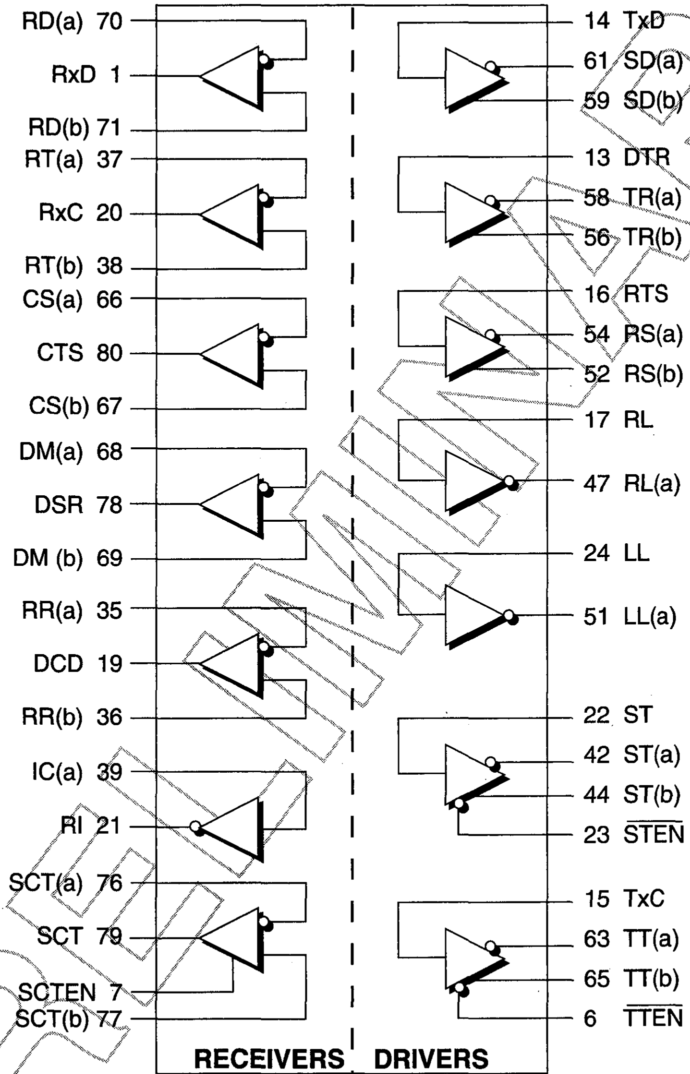
MODE: RS-485							
DRIVER				RECEIVER			
$TDEC_3$	$TDEC_2$	$TDEC_1$	$TDEC_0$	$RDEC_3$	$RDEC_2$	$RDEC_1$	$RDEC_0$
0	1	0	1	0	1	0	1



$\overline{STEN}$	ST	$\overline{TTEN}$	TT	SCTEN	SCT
1	Disabled	1	Disabled	1	Enabled
0	Enabled	0	Enabled	0	Disabled

Figure 23. Mode Diagram — RS-485

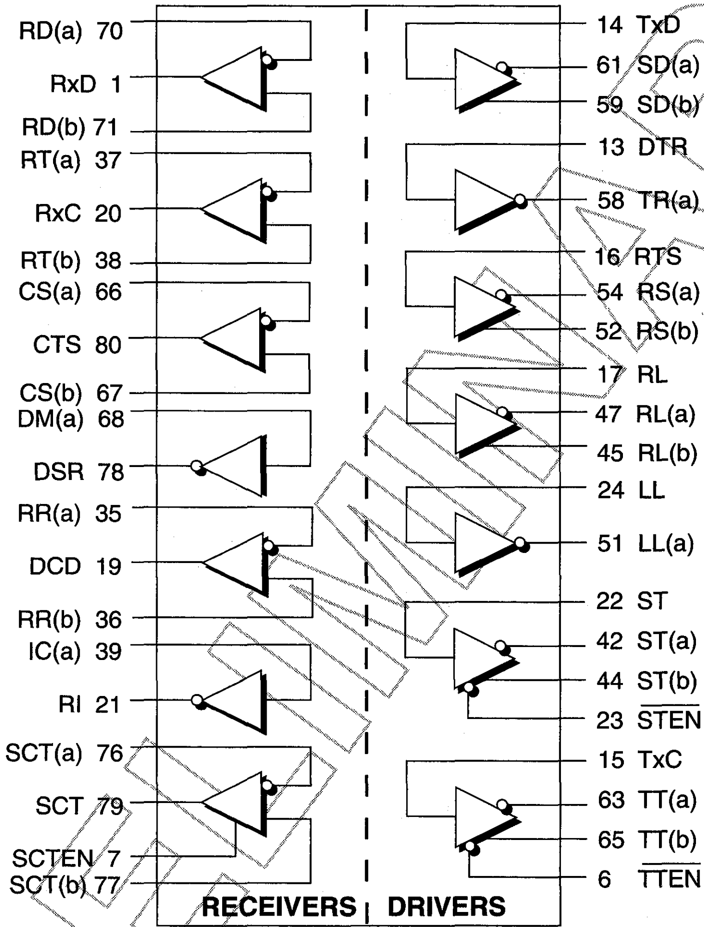
MODE: EIA-530							
DRIVER				RECEIVER			
$TDEC_3$	$TDEC_2$	$TDEC_1$	$TDEC_0$	$RDEC_3$	$RDEC_2$	$RDEC_1$	$RDEC_0$
1	1	0	1	1	1	0	1



$\overline{STEN}$	ST	$\overline{TTEN}$	TT	SCTEN	SCT
1	Disabled	1	Disabled	1	Enabled
0	Enabled	0	Enabled	0	Disabled

Figure 24. Mode Diagram — EIA-530

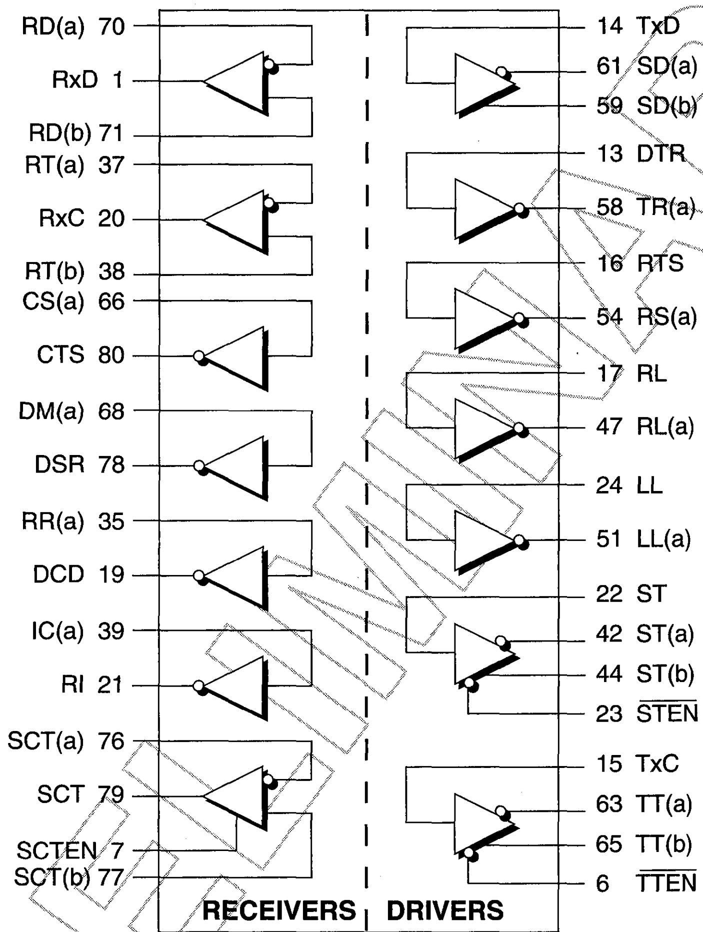
MODE: EIA-530A							
DRIVER				RECEIVER			
$TDEC_3$	$TDEC_2$	$TDEC_1$	$TDEC_0$	$RDEC_3$	$RDEC_2$	$RDEC_1$	$RDEC_0$
1	1	1	1	1	1	1	1



$\overline{STEN}$	ST	$\overline{TTEN}$	TT	SCTEN	SCT
1	Disabled	1	Disabled	1	Enabled
0	Enabled	0	Enabled	0	Disabled

Figure 25. Mode Diagram — EIA-530A

MODE: V.36							
DRIVER				RECEIVER			
$TDEC_3$	$TDEC_2$	$TDEC_1$	$TDEC_0$	$RDEC_3$	$RDEC_2$	$RDEC_1$	$RDEC_0$
0	1	1	0	0	1	1	0



$\overline{STEN}$	ST	$\overline{TTEN}$	TT	SCTEN	SCT
1	Disabled	1	Disabled	1	Enabled
0	Enabled	0	Enabled	0	Disabled

Figure 26. Mode Diagram — V.36

DTE and DCE configurations with the SP504

A serial port can be easily configured for DTE and DCE using two **SP504** parts. The **SP504** allocates signals for data, clock and control lines. The data signals specified in the EIA standards and CCITT are referenced as DTE in the **SP504** datasheet. The DB-25 pin assignment table below is also referenced as DTE. For the DTE, TxD is a driver which drives the data to RxD, a receiver, on the DCE side. TxC or TT is a driver on the DTE side which drives the clock signal to the RxC receiver on the DCE side. The **SP504** offers tri-state control via the decoder address by writing "0000" into $TDEC_X$ or $RDEC_X$. If the serial port is configured to DTE mode, the **SP504** dedicated to DCE must be tri-stated to avoid bus contention problems on the serial port.

As shown on Figure 15, the CCITT signal allocations from the **SP504** in either DTE or DCE to the DB-25 connector. This connector type was selected because of its wide usage. Another connector type can be used as well such as the µDB-26.

DB-25 Connector Pin Assignments for Various Protocols

DB-25 Pin #	RS-232	EIA-530	RS-449	RS-422	V.35	V.36
1	shield	shield	shield	shield	CCITT# 101	CCITT# 101
2	TxD	TxD(A)	SD(A)	T(A)	103(A)	103(A)
3	RxD	RxD(A)	RD(A)	R(A)	104(A)	104(A)
4	RTS	RTS(A)	RS(A)	C(A)	105	105(A)
5	CTS	CTS(A)	CS(A)	–	106	106(A)
6	DSR	DSR(A)	DM(A)	–	107	107(A)
7	Signal GND	Signal GND	Signal GND	Signal GND	102	102
8	DCD	RLSD(A)	RR(A)	I(A)	109	109(A)
9	–	RxC(B)	RT(B)	–	115(B)	115(B)
10	–	RLSD(B)	RR(B)	I(B)	–	109(B)
11	–	TxC(B-DTE)	TT(B)	–	113(B)	113(B)
12	DCD (2nd)	TxCC(B-DCE)	ST(B)	S(B)	114(B)	114(B)
13	CTS (2nd)	CTS(B)	CS(B)	–	–	106(B)
14	TxD (2nd)	TxD(B)	SD(B)	T(B)	103(B)	103(B)
15	TxCC (DCE)	TxCC(A-DCE)	ST(A)	S(A)	114(B)	114(B)
16	RxD (2nd)	RxD(B)	RD(B)	R(B)	104(B)	104(B)
17	RxC	RxC(A)	RT(A)	–	115(A)	115(A)
18	LL	LL	LL	–	–	141
19	RTS (2nd)	RTS(B)	RS(B)	C(B)	–	105(B)
20	DTR	DTR(A)	TR(A)	–	–	–
21	RL	RL	RL	–	–	140
22	RI	DSR(B)	DM(B)	–	–	107(B)
23	SRS	DTR(B)	TR(B)	–	–	–
24	TxC (DTE)	TxC(A-DTE)	TT(A)	–	113(A)	113(A)

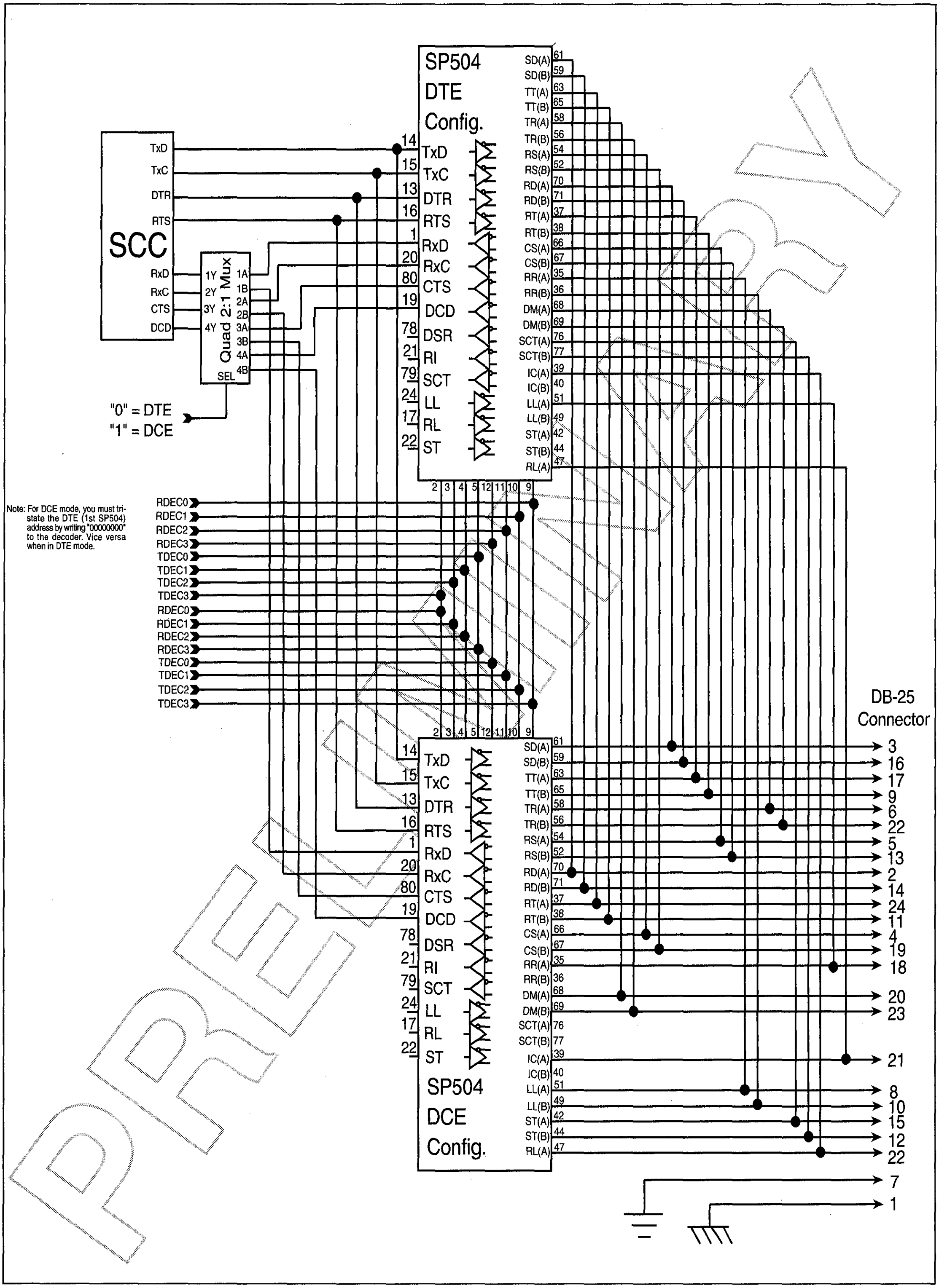


Figure 27. DTE/DCE Application with the SP504

ADDITIONAL TRANSCEIVERS WITH THE SP504

Serial ports usually can have two data signals (SD, RD), three clock signals (TT, ST, RT), and at least eight control signals (CS, RS, etc.). EIA-RS-449 contains twenty six signal types including for a DB-37 connector. A DB-37 serial port design may require thirteen drivers and fourteen receivers[1]. Although many applications do not use all these signals, some applications may need to support extra functions such as diagnostics. The **SP504** supports enough transceivers for the primary channels of data, clock and control signals. Configuring LL, RL and TM would require two additional drivers and one receiver if designing for a DTE (one driver and two receivers for a DCE).

A programmable transceiver such as the **SP332** is a convenient solution in a design that requires a couple extra single ended or differential drivers/receivers. As shown in Figure 16, the **SP332** can be configured to four different variations.

The **SP332** in Figure 17 is configured for two single-ended drivers and one diffferential receiver. For a DTE design, the two drivers are used for LL and RL signals and the receiver is used for the TM signal. This configuration was selected because the two RS-232 drivers can be used for RS-423 by connecting a zener clamping diode to ground on the two driver outputs. The diodes will limit the voltage swing on the outputs so that the $V_{OC} = \pm 4V$ to $\pm 6V$ adheres to the RS-423 specification. The differential receiver can be easily configured to RS-423 by grounding the non-inverting input. The receiver will adhere to the RS-423 specifications.

CIRCUIT MNEMONIC	CIRCUIT NAME	CIRCUIT DIRECTION	CIRCUIT TYPE
SG	SIGNAL GROUND	------------	COMMON
SC	SEND COMMON	TO DCE	
RC	RECEIVE COMMON	FROM DCE	
IS	TERMINAL IN SERVICE	TO DCE	CONTROL
IC	INCOMING CALL	FROM DCE	
TR	TERMINAL READY	TO DCE	
DM	DATA MODE	FROM DCE	
SD	SEND DATA	TO DCE	DATA (PRIMARY CHANNEL)
RD	RECEIVE DATA	FROM DCE	
TT	TERMINAL TIMING	TO DCE	TIMING (PRIMARY CHANNEL)
ST	SEND TIMING	FROM DCE	
RT	RECEIVE TIMING	FROM DCE	
RS	REQUEST TO SEND	TO DCE	CONTROL (PRIMARY CHANNEL)
CS	CLEAR TO SEND	FROM DCE	
RR	RECEIVER READY	FROM DCE	
SQ	SIGNAL QUALITY	FROM DCE	
NS	NEW SIGNAL	TO DCE	
SF	SELECT FREQUENCY	TO DCE	
SR	SIGNAL RATE SELECTOR	TO DCE	
SI	SIGNAL RATE INDICATOR	FROM DCE	
SSD	SECONDARY SEND DATA	TO DCE	DATA (SECONDARY CHANNEL)
SRD	SECONDARY RD	FROM DCE	
SRS	SECONDARY RS	TO DCE	CONTROL (SECONDARY CHANNEL)
SCS	SECONDARY CS	FROM DCE	
SRR	SECONDARY RR	FROM DCE	
LL	LOCAL LOOPBACK	TO DCE	CONTROL
RL	REMOTE LOOPBACK	TO DCE	
TM	TEST MODE	FROM DCE	
SS	SELECT STANDBY	TO DCE	CONTROL
SB	STANDBY INDICATOR	FROM DCE	

[1]RS-449 Interchange Circuits Table

SEL A	0	0	1	1
SEL B	0	1	0	1
LOOPBACK	1	1	1	1
SHUTDOWN	0	0	0	0

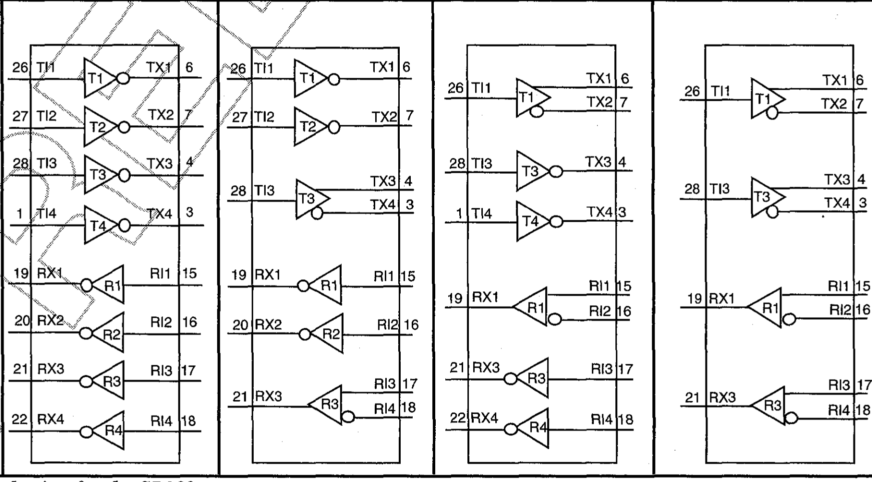


Figure 28. Mode selection for the SP332

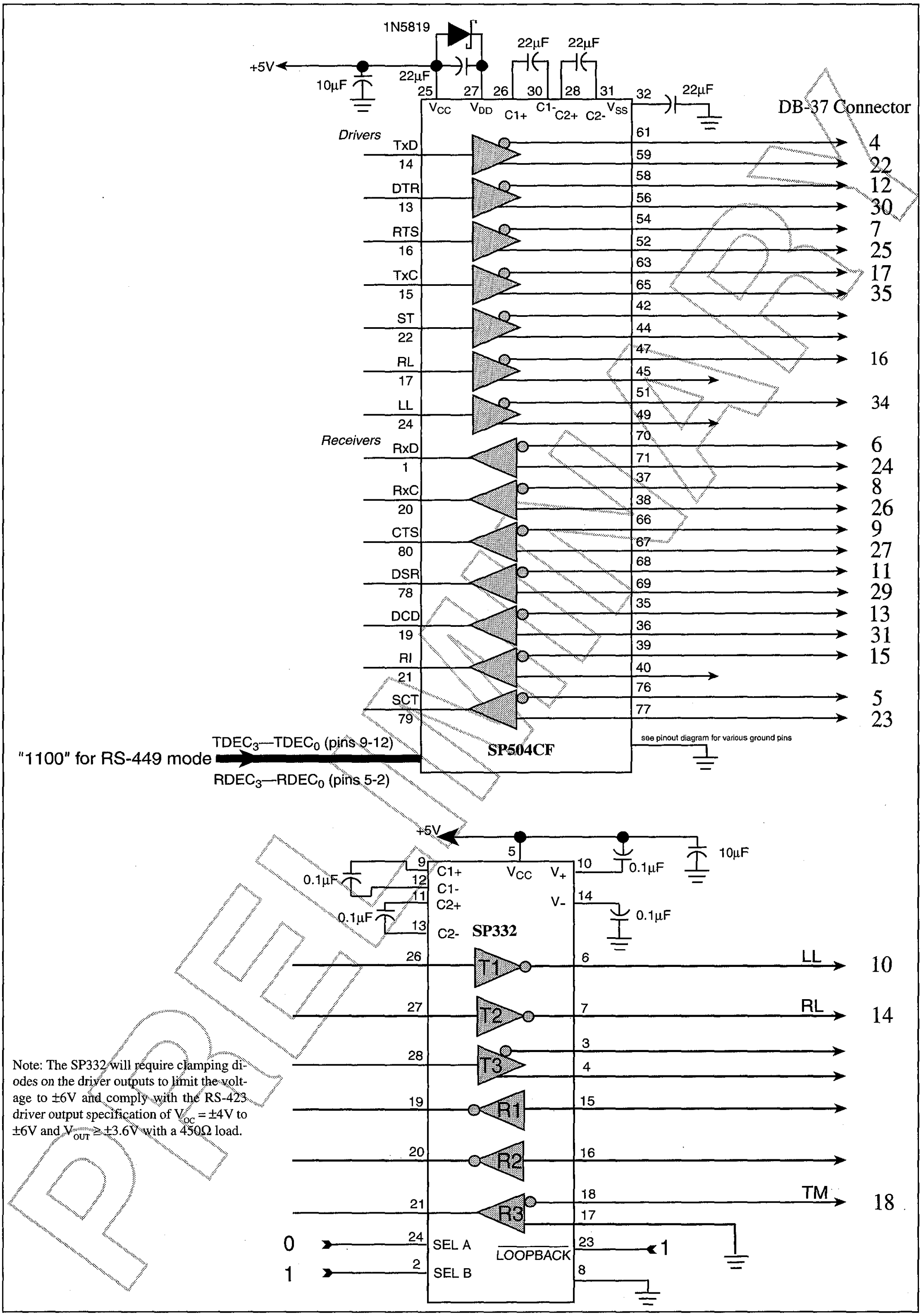


Figure 29. Adding extra differential and single-ended transceivers using the SP332

SP502/SP503 EVALUATION BOARD

The **SP502/SP503 Evaluation Board** (EB) can be used to evaluate the **SP504**. Each board comes equipped with an 80-pin QFP Zero- Insertion socket to allow for testing of multiple devices. The control lines and inputs and outputs of the device can be controlled either manually or via a data bus under software control. There is a 50-pin connector to allow for easy connection to an existing system via a ribbon cable. There are also open areas on the board to add additional circuitry to support application specific requirements.

Manual Control

The SP502/SP503EB will support the **SP502**, **SP503** and **SP504** multi-mode serial transceivers. The transceiver I/O lines are brought out to test pins arranged in the same configuration as shown elsewhere in this data sheet. A top layer silk-screen shows the drivers and receivers to allow direct correlation to the data sheet. The transmitter and receiver decode bits are tied together and are brought out to a DIP switch for manual control of both the driver and receiver interface modes. Since the coding for the drivers and receivers is identical, the bits have been tied together. The DIP switch has 7 positions, four of which are reserved for the TDEC/RDEC control and the other three are used as tri-state control pins. The labels that are in [brackets] apply only to the **SP503** and **SP504**. If a logic one, "1", is asserted, the corresponding red LED will be lit. If a zero is asserted, the corresponding red LED will not be lit.

Software Control

A 50-pin connector brings all the analog and digital I/O lines, V_{CC}, and GND to the edge of the card. This can be wired to the user's existing design via a ribbon cable. A DB-25 adapter is available upon request. The pinout for the connector is described in the following section. When the evaluation board is operated under software control, the DIP switch should be set up so that all bits are low (all LEDs off). This will tie 20KΩ pulldown resistors from the inputs to ground and let the external system control the state of the control inputs.

Power and Ground Requirements

The evaluation board layout has been optimized for performance by using basic analog circuit techniques, The four charge-pump capacitors must be 22µF (16V) and be placed as close to the unit as possible; tantalum capacitors are suggested. The decoupling capacitor must be a minimum of 1µF; depending upon the operating environment, 10µF should be enough for worst case situations. The ground plane for the part must be solid, extending completely under the package. The power supplies for the device should be as accurate as possible; for rated performance ±5% is necessary. The power supply current will vary depending upon the selected mode, the amount of loading and the data rate. As a maximum, the user should reserve 450mA for I_{CC}. The worst-case operating mode is RS-485 under full load of seven drivers supplying 2V to 54Ω loads. The power and ground inputs can be supplied through either the banana jacks on the evaluation board (Red = V_{CC} = +5V±5%; Black = GND) or through the connector.

For reference, the 80-pin QFP Socket is a TESCO part number FPQ-80-65-09A. The 50-pin connector is an AMP part number 749075-5.

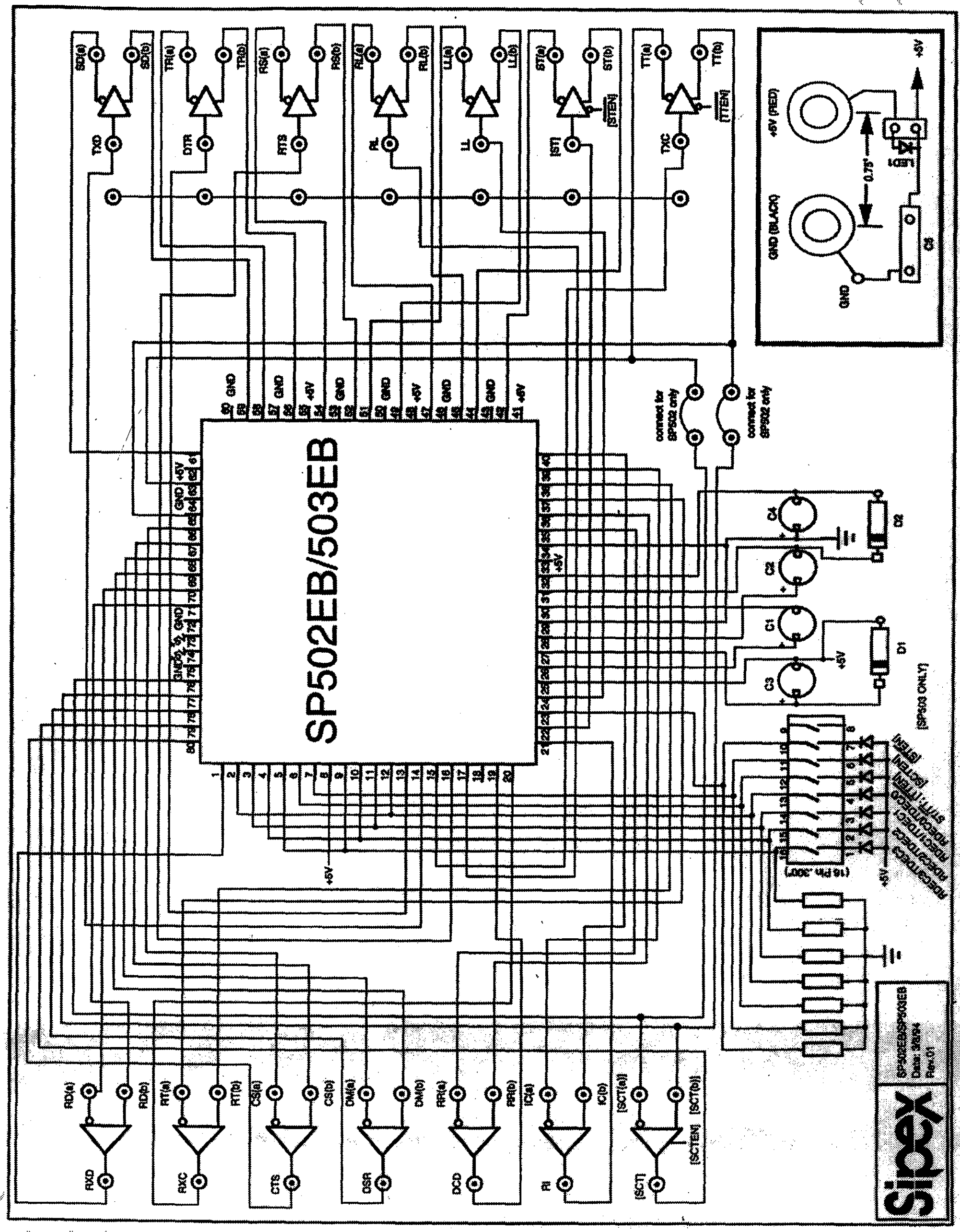
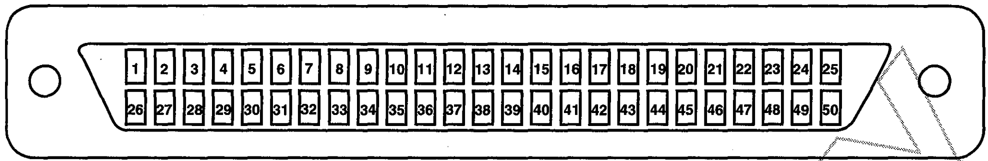
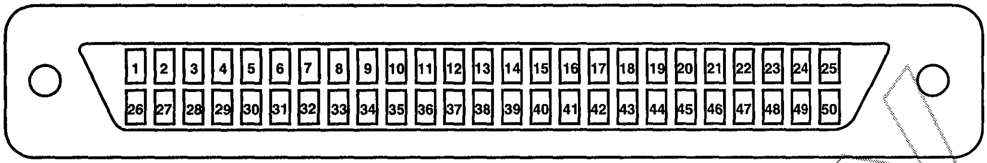


Figure 30. SP502/503 Evaluation Board Schematic



EDGE CONNECTOR	DUT PIN DESCRIPTIONS
01	TxD (pin 14) –TTL Input – Transmit data; source for SD(a) and SD(b) outputs.
02	DTR (pin 13) – TTL Input – Data terminal ready: source for TR(a) and TR(b) outputs.
03	ST/$\overline{TT}$ (pin 6) –TTL Input – ST/$\overline{TT}$ select pin; enables ST drivers and disables TT drivers when high. Disables ST drivers and enables TT drivers when low.
04	$DEC_3/RDEC_3$ (pin 5) – TTL Input – Transmitter/Receiver decode register.
05	$TDEC_2/RDEC_2$ (pin 4) – TTL Input – Transmitter/Receiver decode register.
06	$TDEC_1/RDEC_1$ (pin 3) – TTL Input – Transmitter/Receiver decode register.
07	$TDEC_0/RDEC_0$ (pin 2) – TTL Input – Transmitter/Receiver decode register.
08	RxD (pin 1) – TTL Output – Receive data; sourced from RD(a) and RD)b) inputs.
09	CTS (pin 80) – TTL Output – Clear to send; sourced from CS(a) and CS(b) inputs.
10	RxT (pin 79) – TTL Output – RxT; sourced from TT(a), TT(b) inputs.
11	DSR (pin 78) – TTL Output – Data set ready; sourced from DM(a) and DM(b) inputs.
12	RD(b) (pin 71) – Analog In – Receive data, non–inverted; source for RxD.
13	RD(a) (pin 70) – Analog In – Receive data, inverted: source for RxD.
14	DM(b) (pin 69) – Analog In – Data mode, non–inverted; source for DSR.
15	DM(a) (pin 68) – Analog In – Data mode, inverted; source for DSR.
16	CS(b) (pin 67) – Analog In – Clear to send; non–inverted; source for CTS.
17	CS(a) (pin 66) – Analog In – Clear to send, inverted; source for CTS.
18	TT(b) (pin 65) – Analog In or Out – Terminal timing, non–inverted: sourced from TxC input.
19	TT(a) (pin 63) – Analog In or Out – Terminal timing; inverted: sourced from TxC input.
20	TR(a) (pin 58) – Analog Out – Terminal ready, inverted; sourced from DTR.
21	TR(b) (pin 56) – Analog Out – Terminal ready; non–inverted; sourced from DTR.
22	SD(a) (pin 61) – Analog Out – Send data, inverted; sourced from TxD.
23	SD(b) (pin 59) – Analog Out – Send data; non–inverted; sourced from TxD.
24	RS(a) (pin 54) – Analog Out – Ready to send; inverted; sourced from RTS.
25	RS(b) (pin 52) – Analog Out – Ready to send, non–inverted; sourced from RTS.



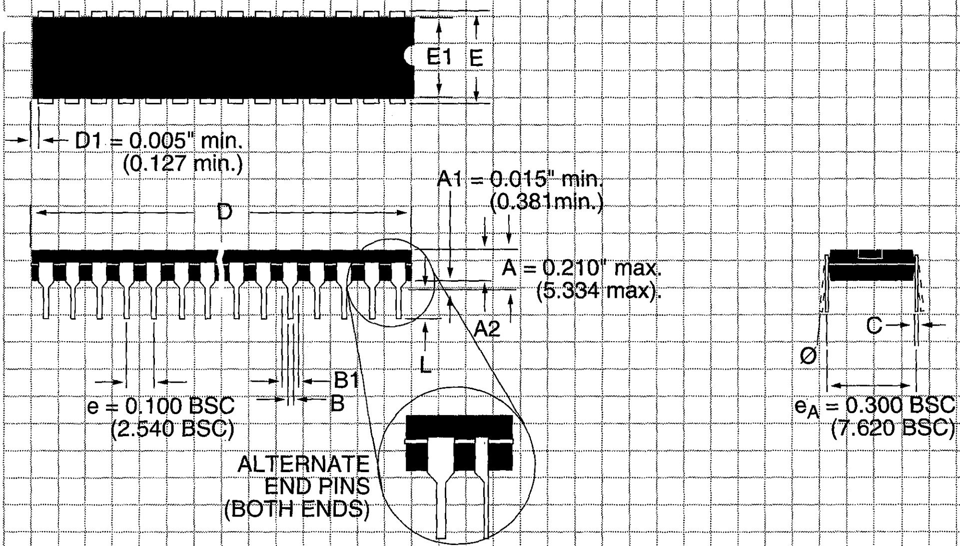
EDGE CONNECTOR	DUT PIN DESCRIPTIONS
26	ST (pin 22) – TTL Input – Send Timing; source for ST(a) and ST(b) outputs.
27	$\overline{STEN}$ (pin 23) – TTL Input — Driver enable control pin; active low.
28	SCT(a) (pin 76) – Analog Input – Inverting; input for SCT receiver.
29	SCT(b) (pin 77) – Analog Input – Non–inverting; input for SCT receiver.
30	V_{CC} — +5V for all circuitry.
31	GND — signal and power ground.
32	LL(a) (pin 51) – Analog Out – Local loopback, inverted; sourced from LL.
33	LL(b) (pin 49) – Analog Out – Local loopback, non–inverted sourced from LL.
34	RL(a) (pin 47) – Analog Out – Remote loopback; inverted; sourced from RL.
35	RL(b) (pin 45) – Analog Out – Remote loopback; non–inverted; sourced from RL.
36	ST(b) (pin 44) – Analog Out – Send timing, non–inverted; sourced from ST.
37	ST(a) (pin 42) – Analog Output –Send timing, inverted; sourced from ST.
38	IC(b) (pin 40) – Analog In – Incoming call; non–inverted; source for RI.
39	IC(a) (pin 39) – Analog In – Incoming call; inverted; source for RI.

EDGE CONNECTOR	DUT PIN DESCRIPTIONS
40	RT(b) (pin 38) – Analog In – Receive timing, non–inverted; source for RxC.
41	RT(a) (pin 37) – Analog In – Receive timing; inverted; source from RxC.
42	RR(b) (pin 36) – Analog In – Receiver ready; non–inverted; source for DCD.
43	RR(a) (pin 35) – Analog In – Receiver ready; inverted; source for DCD.
44	LL (pin 24) – TTL Input – Local loopback; source for LL(a) and LL(b) outputs.
45	RI (pin 21) – TTL Output – Ring indicator; sourced from IC(a) and IC(b) inputs.
46	RxC (pin 20) – TTL Output – Receive clock; sourced from RT(a) and RT(b) inputs.
47	DCD (pin 19) – TTL Output – Data carrier detect; sourced from RR(a) and RR(b) inputs.
48	RL (pin 17) – Analog Out – Remote loopback; source for RL(a) and RL(b) outputs.
49	RTS (pin 16) – TTL Input – Ready to send; source for RS(a) and RS(b) outputs.
50	TxC (pin 15) – TTL Input – Transmit clock; Source for TT(a) and TT(b) driver outputs.

ORDERING INFORMATION		
Model	**Temperature Range**	**Package Types**
SP504CF	0°C to +70°C	80–pin QFP

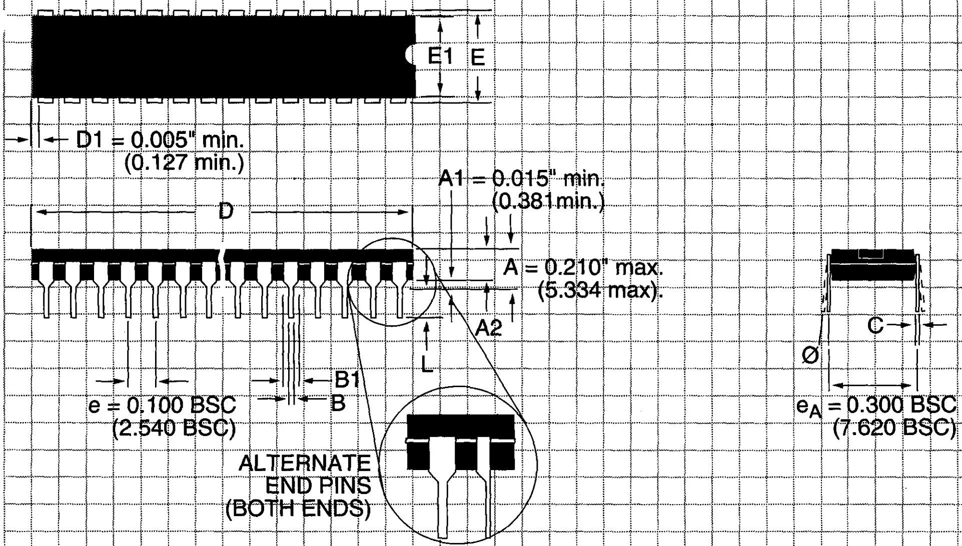
Sipex Corporation
SIGNAL PROCESSING EXCELLENCE

PACKAGE: PLASTIC DUAL-IN-LINE (NARROW)



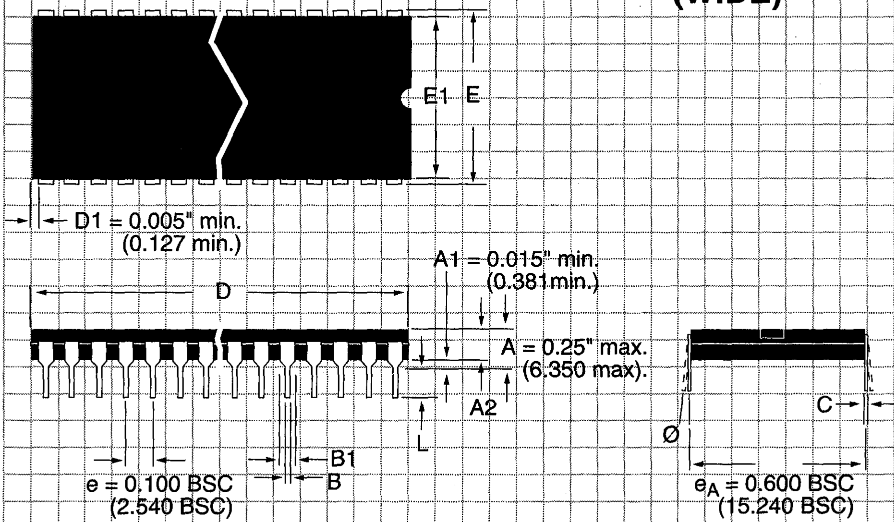
DIMENSIONS (Inches) Minimum/Maximum (mm)	8–PIN	14–PIN	16–PIN	18–PIN	20–PIN	22–PIN
A2	0.115/0.195 (2.921/4.953)	0.115/0.195 (2.921/4.953)	0.115/0.195 (2.921/4.953)	0.115/0.195 (2.921/4.953)	0.115/0.195 (2.921/4.953)	0.115/0.195 (2.921/4.953)
B	0.014/0.022 (0.356/0.559)	0.014/0.022 (0.356/0.559)	0.014/0.022 (0.356/0.559)	0.014/0.022 (0.356/0.559)	0.014/0.022 (0.356/0.559)	0.014/0.022 (0.356/0.559)
B1	0.045/0.070 (1.143/1.778)	0.045/0.070 (1.143/1.778)	0.045/0.070 (1.143/1.778)	0.045/0.070 (1.143/1.778)	0.045/0.070 (1.143/1.778)	0.045/0.070 (1.143/1.778)
C	0.008/0.014 (0.203/0.356)	0.008/0.014 (0.203/0.356)	0.008/0.014 (0.203/0.356)	0.008/0.014 (0.203/0.356)	0.008/0.014 (0.203/0.356)	0.008/0.014 (0.203/0.356)
D	0.355/0.400 (9.017/10.160)	0.735/0.775 (18.669/19.685)	0.780/0.800 (19.812/20.320)	0.880/0.920 (22.352/23.368)	0.980/1.060 (24.892/26.924)	1.145/1.155 (29.083/29.337)
E	0.300/0.325 (7.620/8.255)	0.300/0.325 (7.620/8.255)	0.300/0.325 (7.620/8.255)	0.300/0.325 (7.620/8.255)	0.300/0.325 (7.620/8.255)	0.300/0.325 (7.620/8.255)
E1	0.240/0.280 (6.096/7.112)	0.240/0.280 (6.096/7.112)	0.240/0.280 (6.096/7.112)	0.240/0.280 (6.096/7.112)	0.240/0.280 (6.096/7.112)	0.240/0.280 (6.096/7.112)
L	0.115/0.150 (2.921/3.810)	0.115/0.150 (2.921/3.810)	0.115/0.150 (2.921/3.810)	0.115/0.150 (2.921/3.810)	0.115/0.150 (2.921/3.810)	0.115/0.150 (2.921/3.810)
Ø	0°/ 15° (0°/15°)	0°/ 15° (0°/15°)	0°/ 15° (0°/15°)	0°/ 15° (0°/15°)	0°/ 15° (0°/15°)	0°/ 15° (0°/15°)

PACKAGE: PLASTIC DUAL–IN–LINE (NARROW)



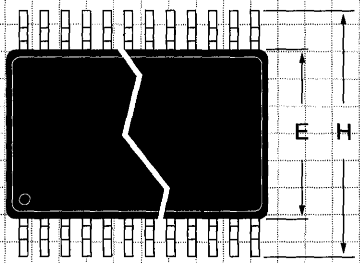
DIMENSIONS (Inches) Minimum/Maximum (mm)	24–PIN	28–PIN				
A2	0.115/0.195 (2.921/4.953)	0.115/0.195 (2.921/4.953)				
B	0.014/0.022 (0.356/0.559)	0.014/0.022 (0.356/0.559)				
B1	0.045/0.070 (1.143/1.778)	0.045/0.070 (1.143/1.778)				
C	0.008/0.014 (0.203/0.356)	0.008/0.014 (0.203/0.356)				
D	1.230/1.280 (31.24/32.51)	1.385/1.405 (35.179/35.687)				
E	0.300/0.325 (7.620/8.255)	0.300/0.325 (7.620/8.255)				
E1	0.240/0.280 (6.096/7.112)	0.240/0.280 (6.096/7.112)				
L	0.115/0.150 (2.921/3.810)	0.115/0.150 (2.921/3.810)				
Ø	0°/ 15° (0°/15°)	0°/ 15° (0°/15°)				

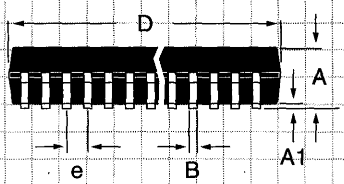
PACKAGE: PLASTIC DUAL–IN–LINE (WIDE)

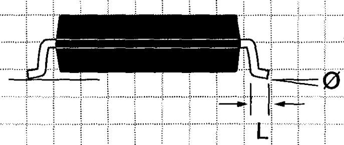


DIMENSIONS (Inches) Minimum/Maximum (mm)	24–PIN	28–PIN	40–PIN	48–PIN		
A2	0.125/0.195 (3.175/4.953)	0.125/0.195 (3.175/4.953)	0.125/0.195 (3.175/4.953)	0.125/0.195 (3.175/4.953)		
B	0.014/0.022 (0.366/0.559	0.014/0.022 (0.366/0.559	0.014/0.022 (0.366/0.559)	0.014/0.022 (0.366/0.559)		
B1	0.030/0.070 (0.762/1.778)	0.030/0.070 (0.762/1.778)	0.030/0.070 (0.762/1.778)	0.030/0.070 (0.762/1.778)		
C	0.008/0.015 (0.203/0.381)	0.008/0.015 (0.203/0.381)	0.008/0.015 (0.203/0.381)	0.008/0.015 (0.203/0.381)		
D	1.150/1.290 (29.21/32.76)	1.380/1.565 (35.05/39.75)	1.980/2.095 (50.29/53.21)	2.385/2.480 (60.57/62.99)		
E	0.600/0.625 (15.24/15.87)	0.600/0.625 (15.24/15.87)	0.600/0.625 (15.24/15.87)	0.600/0.625 (15.24/15.87)		
E1	0.485/0.580 (12.31/14.73)	0.485/0.580 (12.31/14.73)	0.485/0.580 (12.31/14.73)	0.485/0.580 (12.31/14.73)		
L	0.115/0.200 (2.921/5.080)	0.115/0.200 (2.921/5.080)	0.115/0.200 (2.921/5.080)	0.115/0.200 (2.921/5.080)		
Ø	0°/ 15° (0°/15°)	0°/ 15° (0°/15°)	0°/ 15° (0°/15°)	0°/ 15° (0°/15°)		

PACKAGE: PLASTIC SHRINK SMALL OUTLINE (SSOP)

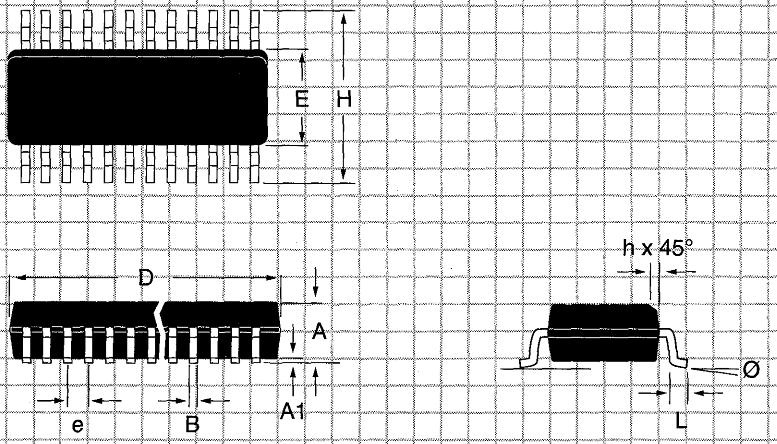






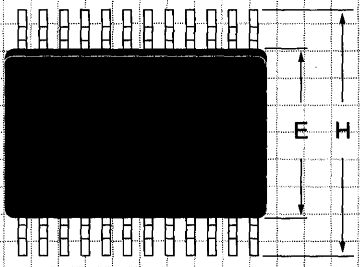
DIMENSIONS (Inches) Minimum/Maximum (mm)	24–PIN	28–PIN				
A	0.068/0.078 (1.73/1.99)	0.068/0.078 (1.73/1.99)				
A1	0.002/0.008 (0.05/0.21)	0.002/0.008 (0.05/0.21)				
B	0.010/0.015 (0.25/0.38)	0.010/0.015 (0.25/0.38)				
D	0.317/0.328 (8.07/8.33)	0.397/0.407 (10.07/10.33)				
E	0.205/0.212 (5.20/5.38)	0.205/0.212 (5.20/5.38)				
e	0.0256 BSC (0.65 BSC)	0.0256 BSC (0.65 BSC)				
H	0.301/0.311 (7.65/7.90)	0.301/0.311 (7.65/7.90)				
L	0.022/0.037 (0.55/0.95)	0.022/0.037 (0.55/0.95)				
Ø	0°/8° (0°/8°)	0°/8° (0°/8°)				

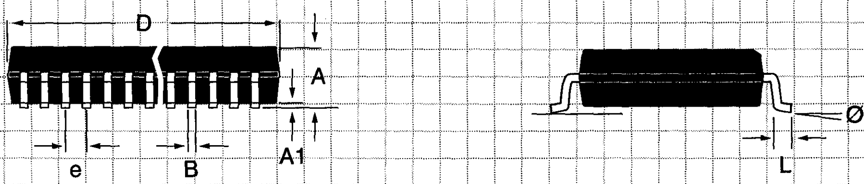
PACKAGE: PLASTIC SMALL OUTLINE (SOIC) (NARROW)



DIMENSIONS (Inches) Minimum/Maximum (mm)	8–PIN	14–PIN	16–PIN			
A	0.053/0.069 (1.346/1.748)	0.053/0.069 (1.346/1.748)	0.053/0.069 (1.346/1.748)			
A1	0.004/0.010 (0.102/0.249	0.004/0.010 (0.102/0.249)	0.004/0.010 (0.102/0.249)			
B	0.014/0.019 (0.35/0.49)	0.013/0.020 (0.330/0.508)	0.013/0.020 (0.330/0.508)			
D	0.189/0.197 (4.80/5.00)	0.337/0.344 (8.552/8.748)	0.386/0.394 (9.802/10.000)			
E	0.150/0.157 (3.802/3.988)	0.150/0.157 (3.802/3.988)	0.150/0.157 (3.802/3.988)			
e	0.050 BSC (1.270 BSC)	0.050 BSC (1.270 BSC)	0.050 BSC (1.270 BSC)			
H	0.228/0.244 (5.801/6.198)	0.228/0.244 (5.801/6.198)	0.228/0.244 (5.801/6.198)			
h	0.010/0.020 (0.254/0.498)	0.010/0.020 (0.254/0.498)	0.010/0.020 (0.254/0.498)			
L	0.016/0.050 (0.406/1.270)	0.016/0.050 (0.406/1.270)	0.016/0.050 (0.406/1.270)			
Ø	0°/8° (0°/8°)	0°/8° (0°/8°)	0°/8° (0°/8°)			

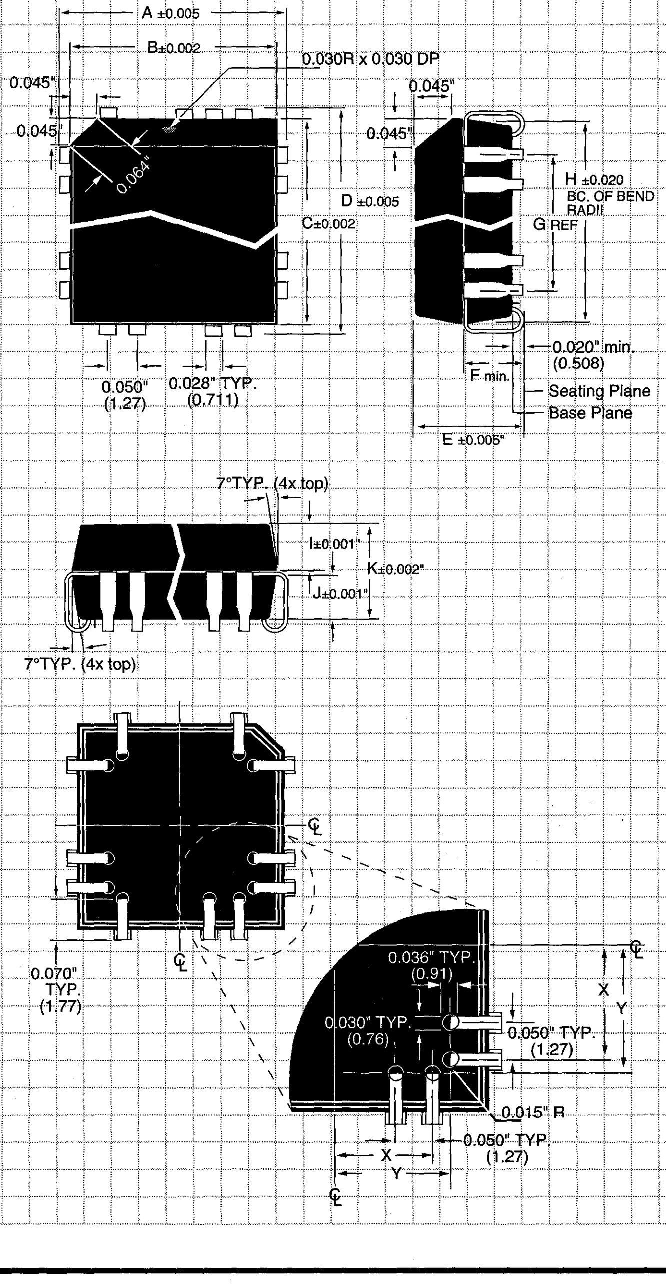
PACKAGE: PLASTIC SMALL OUTLINE (SOIC) (WIDE)





DIMENSIONS (Inches) Minimum/Maximum (mm)	14–PIN	16–PIN	18–PIN	20–PIN	24–PIN	28–PIN
A	0.093/0.104 (2.352/2.649)	0.093/0.104 (2.352/2.649)	0.093/0.104 (2.352/2.649)	0.093/0.104 (2.352/2.649)	0.093/0.104 (2.352/2.649)	0.093/0.104 (2.352/2.649)
A1	0.004/0.012 (0.102/0.300)	0.004/0.012 (0.102/0.300)	0.004/0.012 (0.102/0.300)	0.004/0.012 (0.102/0.300)	0.004/0.012 (0.102/0.300)	0.004/0.012 (0.102/0.300)
B	0.013/0.020 (0.330/0.508)	0.013/0.020 (0.330/0.508)	0.013/0.020 (0.330/0.508)	0.013/0.020 (0.330/0.508)	0.013/0.020 (0.330/0.508)	0.013/0.020 (0.330/0.508)
D	0.348/0.363 (8.83/9.22)	0.398/0.413 (10.10/10.49)	0.447/0.463 (11.35/11.74)	0.496/0.512 (12.60/13.00)	0.599/0.614 (15.20/15.59)	0.697/0.713 (17.70/18.09)
E	0.291/0.299 (7.402/7.600)	0.291/0.299 (7.402/7.600)	0.291/0.299 (7.402/7.600)	0.291/0.299 (7.402/7.600)	0.291/0.299 (7.402/7.600)	0.291/0.299 (7.402/7.600)
e	0.050 BSC (1.270 BSC)	0.050 BSC (1.270 BSC)	0.050 BSC (1.270 BSC)	0.050 BSC (1.270 BSC))	0.050 BSC (1.270 BSC)	0.050 BSC (1.270 BSC)
H	0.394/0.419 (10.00/10.64)	0.394/0.419 (10.00/10.64)	0.394/0.419 (10.00/10.64)	0.394/0.419 (10.00/10.64)	0.394/0.419 (10.00/10.64)	0.394/0.419 (10.00/10.64)
L	0.016/0.050 (0.406/1.270)	0.016/0.050 (0.406/1.270)	0.016/0.050 (0.406/1.270)	0.016/0.050 (0.406/1.270)	0.016/0.050 (0.406/1.270)	0.016/0.050 (0.406/1.270)
Ø	0°/8° (0°/8°)	0°/8° (0°/8°)	0°/8° (0°/8°)	0°/8° (0°/8°)	0°/8° (0°/8°)	0°/8° (0°/8°)

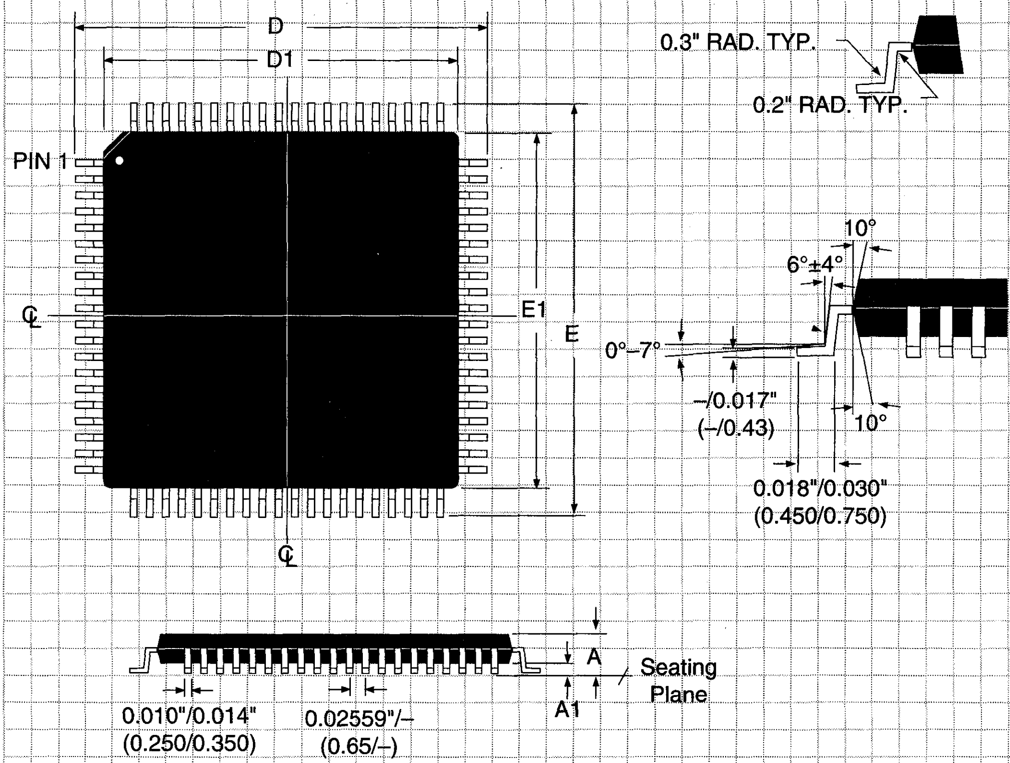
PACKAGE: PLASTIC LEADLESS CHIP CARRIER (PLCC)



PACKAGE: PLASTIC LEADLESS CHIP CARRIER (PLCC)

DIMENSIONS (Inches) Minimum/Maximum (mm)	20–PIN	28–PIN	44–PIN	68–PIN	84–PIN
A	0.385/0.395 (9.77/10.03)	0.485/0.495 (12.31/12.57)	0.685/0.695 (17.39/17.65)	0.985/0.995 (25.02/25.27)	1.185/1.195 (30.09/30.35)
B	0.350/0.355 (8.89/9.017)	0.452/0.456 (11.48/11.58)	0.652/0.656 (16.56/16.61)	0.952/0.956 (24.18/24.28)	1.152/1.156 (29.26/29.36)
C	0.350/0.355 (8.89/9.017)	0.452/0.456 (11.48/11.58	0.652/0.656 (16.56/16.61	0.952/0.956 (24.18/24.28)	1.152/1.156 (29.26/29.36)
D	0.385/0.395 (9.77/10.03)	0.485/0.495 (12.31/12.57)	0.685/0.695 (17.39/17.65	0.985/0.995 (25.02/25.27))	1.185/1.195 (30.09/30.35)
E	0.170/0.180 (4.32/4.57)	0.170/0.180 (4.32/4.57)	0.170/0.180 (4.32/4.57)	0.170/0.180 (4.32/4.57)	0.170/0.180 (4.32/4.57)
F	0.098/– (2.48/–)	0.098/– (2.48/–)	0.098/– (2.48/–)	0.098/– (2.48/–)	0.098/– (2.48/–)
G	0.200 REF (5.08 REF)	0.300 REF (7.62 REF)	0.500 REF (12.7 REF)	0.800 REF (20.32 REF)	1.000 REF (25.44 REF)
H	0.290/0.330 (7.36/8.38)	0.390/0.430 (9.906/10.922)	0.590/0.630 (14.98/16.00)	0.890/0.930 (22.60/23.62)	1.090/1.130 (27.69/28.70)
I	0.065/0.070 (1.65/1.77)	0.070/0.072 (1.77/1.83	0.070/0.072 (1.77/1.83	0.070/0.072 (1.77/1.83)	0.070/0.072 (1.77/1.83
J	0.08/– (2.03/–)	0.070/0.072 (1.77/1.82)	0.070/0.072 (1.77/1.82)	0.070/0.072 (1.77/1.83)	0.070/0.072 (1.77/1.82)
K	0.145/0.156 (3.68/3.96)	0.148/0.152 (3.75/3.86)	0.148/0.152 (3.75/3.86)	0.148/0.152 (3.75/3.86)	0.148/0.152 (3.75/3.86)
X	0.100 REF (2.54 REF)	0.150 REF (3.810 REF)	0.250 REF (6.35 REF)	0.400 REF (10.16 REF)	0.500 REF (12.7 REF)
Y	0.140/0.147 (3.50/3.733)	0.180 REF (4.572 REF)	0.280 REF (7.11 REF)	0.430 REF (10.92 REF)	0.530 REF (13.46 REF)

PACKAGE: QUAD FLATPACK



DIMENSIONS (Inches) Minimum/Maximum (mm)	80–PIN
A	–/0.096 (–/2.450)
A1	–/0.010 (–/0.250)
D	0.620/0.640 (15.750/16.250)
D1	0.547/0.555 (13.900/14.100)
E	0.620/0.640 (15.750/16.250)
E1	0.547/0.555 (13.900/14.100)

APPENDIX CONTENTS

Sipex Corporation
SIGNAL PROCESSING EXCELLENCE

SIPEX DATA CONVERSION PRODUCTS LISTING

For information on any of the following SIPEX Data Conversion Products, please contact the SIPEX Literature Department at (508) 667-8700.

Model **Description**

Analog-to-Digital Converters

HS574A ... 12-Bit, 25µs
SP674A ... 12-Bit, 15µs

Sampling Analog-to-Digital Converters

SP574B ... 12-Bit, 25µs; 20kHz Nyquist Frequency
SP674B ... 12-Bit, 15µs; 33kHz Nyquist Frequency
SP774B ... 12-Bit, 8µs; 62.5kHz Nyquist Frequency
SP1674B . 12-Bit, 10µs; 50kHz Nyquist Frequency
SP7800A . 12-Bit, 3µs; Single +5V Supply
SP8503 .... 12-Bit, 3µs; Bipolar Input
SP8505 .... 12-Bit, 5µs; Bipolar Input
SP8510 .... 12-Bit, 10µs; Bipolar Input
NEW **SP8530 ....** 12-Bit, 7.75µs, Simultaneous Sampling, Single +5V Supply, Serial Output
NEW **SP8531 ....** 12-Bit, 3.75µs, Single +5V Supply, Serial Output
SP8603 .... 12-Bit, 3µs; Unipolar Input
SP8605 .... 12-Bit, 5µs; Unipolar Input
SP8610 .... 12-Bit, 10µs; Unipolar Input

Digital-to-Analog Converters

HS3120 ... 12-Bit, 2µs, Latched, 4-Quadrant Multiplying, Current Output
HS3140 ... 14-Bit, 2µs, 4-Quadrant Multiplying, Current Output
HS3160 ... 16-Bit, 2µs, 4-Quadrant Multiplying, Current Output
SP7512 .... 12-Bit, 2µs, Double-Buffered, 4-Quadrant Multiplying, Current Output
SP7514 .... 14-Bit, 2µs, 4-Quadrant Multiplying, Current Output
SP7516 .... 16-Bit, 2µs, 4-Quadrant Multiplying, Current Output
HS7541A . 12-Bit, 2µs, 4-Quadrant Multiplying, Current Output
SP7545 .... 12-Bit, 2µs, Buffered, 4-Quadrant Multiplying, Current Output
HS7584 ... 12-Bit, 2µs, Quad, Double-Buffered, 4-Quadrant Multiplying, Current Output with Independent Reference Inputs
SP9316 .... 16-Bit, 2µs, Latched, 4-Quadrant Multiplying, Current Output
NEW **SP9500 ....** 12-Bit, 7.5µs, Single +5V Supply, 2 Quadrant Multiplying, Serial Input, Voltage Output
SP9501 .... 12-Bit, 4µs, 4-Quadrant Multiplying, Voltage Output
SP9502 .... 12-Bit, 4µs, Dual, 4-Quadrant Multiplying, Voltage Output
SP9504 .... 12-Bit, 4µs, Quad, 4-Quadrant Multiplying, Voltage Output, Extended Temperature Range
NEW **SP9600 ....** 12-Bit, 20µs, Low Power, +5V Supply, 2 Quadrant Multiplying, Serial Input, Voltage Output
SP9601 .... 12-Bit, 30µs, Low-Power; 4-Quadrant Multiplying, Voltage Output
SP9602 .... 12-Bit, 30µs, Low-Power; Dual, 4-Quadrant Multiplying, Voltage Output
SP9604 .... 12-Bit, 30µs, Low-Power; Quad, 4-Quadrant Multiplying, Voltage Output
SP9840 .... 8-Bit, 0.7µs; Octal, Multiplying, Voltage Output with 3-Wire Serial Interface and 8 Independent Reference Inputs
SP9841 .... 8-Bit, 0.7µs; Octal, 2-Quadrant Multiplying, Voltage Output with 8 Independent Reference Inputs
SP9842 .... 8-Bit, 0.7µs; Octal, Multiplying, Voltage Output with 4 pair of Reference Inputs
SP9843 .... 8-Bit, 0.7µs; Octal, Multiplying, Voltage Output with 3-Wire Serial Interface and 4 Pair Reference Inputs

Sipex Corporation
SIGNAL PROCESSING EXCELLENCE

SIPEX DATA CONVERSION PRODUCTS LISTING

For information on any of the following SIPEX Data Conversion Products, please contact the SIPEX Literature Department at (508) 667-8700.

Data Acquisition Systems

SP8120 .... 8-Channel, 12-Bit, 100KHz, Parallel Out, Monolithic DAS
SP8121 .... 8-Channel, 12-Bit, 100KHz, Parallel Out, Monolithic DAS7
SP8480 .... 8-Channel, 12-Bit, 100KHz, 8/4 Nibble Out, Monolithic DAS
SP8481 .... 8-Channel, 12-Bit, 100KHz, Latched MUX, Nibble Out, Monolithic DAS
NEW **SP8542** .... 2-Channel, 12-Bit, 235KHz, Single +5V Supply, Serial I/O
NEW **SP8544** .... 4-Channel, 12-Bit, 235KHz, Single +5V Supply, Serial I/O

SIPEX... EXCELLENCE IN SIGNAL PROCESSING

Sipex Corporation designs and manufactures Analog Signal Processing Circuits. Utilizing a broad range of technologies including CMOS, Bipolar and BiCMOS, **Sipex** has developed a wide range of monolithic products. **Sipex**'s Standard Products are focused primarily in two areas: Data Converters and Interface Circuits. The Interface Circuits consist of industry standard as well as proprietary products. Data Converter products cover a full range of D/A's, A/D's, and DAS' with primary focus on high speed, high resolution circuits. In addition to **Sipex's** broad standard product offering, the company designs and manufactures custom circuits for unique signal processing needs.

This catalog introduces new **Sipex** Interface Products and is considered a supplement to our full line Interface Products Catalog. If you would like our full line Interface Products Catalog or our Data Conversion Products catalog, please contact the **Sipex** Literature Department at 508-667-8700.

SIPEX INTERFACE PRODUCTS:
Single Interface

Sipex has been serving the +5V Only RS-232 market since 1988. This product line does represent our core product offering and is enhanced and improved as needed to keep pace with the rigorous requirements of industry. In 1993 **Sipex** released the first product in a family of RS-485 transceivers. The SP485 which is a half duplex RS-485 transceiver was the first in a series of RS-485 transceivers.

Multi–Mode Interface

Sipex entered the multimode serial interface market with the industry's first programmable RS-232/422 transceiver in 1990. Based on this technology the 300 series was expanded to support RS-232, RS-422, and AppleTalk™. Single-chip transceivers supporting two interface modes gave us the entree into our newest series — the 500 series supports up to eleven (11) programmable interface standards integrated into easy to use, space saving, single chip solutions.

Whether it's our multimode transceivers or one of our many single interface products, **Sipex** is delivering affordable, reliable solutions to the market today.

RELIABILITY

Quality and reliability have long been inherent to our company. While the majority of our sales today are to Industrial customers, our roots were in the military markets, including demanding space applications.

The disciplines required to successfully service these markets have been carried into all **Sipex**'s products. Quality has always been a 'way of life' at **Sipex**. Outgoing quality levels of our monolithic products are better than 200ppm with our more mature products better than 100ppm. We are proud of our outgoing quality level and are continually striving to improve upon it.

Ordering Information

North America: Orders may be placed through our North American Sales office located at 22 Linnell Circle, Billerica, MA 01821 USA by telephone at 508–667–8700 or by fax at 508–670–9001. Product information may be obtained, and orders placed through **Sipex**'s representatives or distributors whose addresses and telephone numbers are listed in this catalog.

International: Customers outside North America are served by **Sipex** direct sales offices in France, Germany and Japan. **Sipex** is also represented throughout the world by international representatives and distributors whose offices are listed in this catalog.

Terms and Conditions of Sale

Prices and delivery information of any item in this catalog is available from our sales representatives or direct from the Company. Quotations are F.O.B. factory of origin, and are subject to change without notice. On all orders, payment is net 30 days following date of shipment.

Applications Engineering

Sipex maintains a support staff of technical sales engineers, both domestically and internationally, who are expert in specific areas of analog, digital, and microelectronics technology. Staff engineers provide further technical support, as needed, on advanced circuit designs or application problems.

Shipping Instruments

Shipping will be via United Parcel Service or Parcel Post unless other instructions are indicated. For rush service, we will ship by Air Freight, Air Express or Air Parcel Post on request.

Warranty

Sipex warrants its products to be free from defects in material and workmanship for a period of one year from the date of shipment. This warranty shall not apply to any product which has been abused or misused physically or electrically or whose leads have been clipped or soldered. **Sipex's** sole liability and the Purchaser's sole remedy under this warranty is limited to repairing or replacing defective components. **Sipex** shall not be liable for consequential damages under any circumstances.

Returns

When returning material for repair or replacement, it is necessary first to contact Customer Service. Upon acceptance of the request, a return material authorization (RMA#) will be issued. We require a detailed description of the reason for the return; the date and purchase order number on which it was obtained, and the date of receipt.

Specifications

Sipex reserves the right to discontinue items and change specifications without notice.

Sipex Corporation
SIGNAL PROCESSING EXCELLENCE

NORTH AMERICAN MANUFACTURERS REPRESENTATIVES

ALABAMA
Huntsville
EMA
Tel: 205-830--4030
800-633-2920(AL only)
Fax: 205-830-1947

ARIZONA
SOUTHWEST TECHNICAL SALES
Tel: 602-893-1209
Fax: 602-893-1312

ARKANSAS
(Dallas, TX)
MREP
Tel: 214-484-5711
Fax: 214-484-0634

CALIFORNIA
Irvine
SPECTRUM REP COMPANY
Tel: 714-453-1525
Fax: 714-453-1925

Milpitas
SIPEX CORPORATION
Tel: 408-945-9080
Fax: 408-946-6191

Riverside
SIPEX CORPORATION
Tel: 800-828-7818
FAX: 909-681-6754

Westlake Village
SPECTRUM REP COMPANY
Tel: 818-706-2919
Fax: 818-706-2978

COLORADO
Denver
SEALE & ASSOCIATES, INC.
Tel: 303-779-8005
Fax: 303-771-1103

CONNECTICUT
Hamden
DATCOM
Tel: 203-288-7005
Fax: 203-281-4233

DELAWARE
(Horsham, PA)
NEXUS TECHNOLOGY SALES
Tel: 215-675-9600
Fax: 215-675-9604

FLORIDA
Clearwater (Main Office)
ELECTRO–CRAFT, INC.
Tel: 813-530-3788
Fax: 813-530-9252

Apopka
ELECTRO–CRAFT, INC.
Tel: 407-880-7356
Fax: 407-880-7590

Boynton Beach
ELECTRO–CRAFT, INC.
Tel: 407-364-0933
Fax: 407-364-0935

GEORGIA
Roswell
EMA
Tel: 770-992-7240
800-647-3773 (GA only)
Fax: 770-993-3426

IDAHO
(Denver, CO)
SEALE & ASSOCIATES, INC.
Tel: 303-779-8005
Fax: 303-771-1103

ILLINOIS
Oak Brook
ATI LTD.
Tel: 708-574-1771
Fax: 708-572-0907

INDIANA
Indianapolis
MOHRFIELD MARKETING, INC.
Tel: 317-546-6969
Fax: 317-545-4504

Leo
MOHRFIELD MARKETING, INC.
Tel: 219-627-5355
Fax: 219-627-2953

IOWA
(Billerica, MA)
SIPEX CORPORATION
Tel: 508-667-8700
Fax: 508-670-9001

KANSAS
(Billerica, MA)
SIPEX CORPORATION
Tel: 508-667-8700
Fax: 508-670-9001

KENTUCKY
Lexington
MOHRFIELD MARKETING, INC.
Tel: 606-277-7990
Fax: 606-278-1278

LOUISIANA
(Dallas, TX)
MREP
Tel: 214-484-5711
Fax: 214-484-0634

MAINE
(Billerica, MA)
SIPEX CORPORATION
Tel: 508-667-8700
Fax: 508-670-9001

MARYLAND
Pasadena
EES
Tel: 410-255-9686
Fax: 410-255-9688

MASSACHUSETTS
Billerica
SIPEX CORPORATION
Tel: 508-667-8700
Fax: 508-670-9001

MICHIGAN
Plymouth
JAY MARKETING ASSOC.
Tel: 313-459-1200
Fax: 313-459-1697

MINNESOTA
Excelsior
CBR ASSOCIATES
Tel: 612-470-2282
Fax: 612-470-2283

MISSISSIPPI
(Huntsville, AL)
EMA
Tel: 205-830-4030
Fax: 205-830-1947

MISSOURI
(Billerica, MA)
SIPEX CORPORATION
Tel: 508-667-8700
Fax: 508-670-9001

MONTANA
(Denver, CO)
SEALE & ASSOCIATES, INC.
Tel: 303-779-8005
Fax: 303-771-1103

NEBRASKA
(Billerica, MA)
SIPEX CORPORATION
Tel: 508-667-8700
Fax: 508-670-9001

NEVADA
(Milpitas, CA)
SIPEX CORPORATION
Tel: 408-945-9080
Fax: 408-946-6191

NEW HAMPSHIRE
(Billerica, MA)
SIPEX CORPORATION
Tel: 508-667-8700
Fax: 508-670-9001

NEW MEXICO
(Phoenix, AZ)
SOUTHWEST TECHNICAL SALES
Tel: 602-893-1209
Fax: 602-893-1312

NEW YORK/NEW JERSEY (METRO)
(Fort Lee, NJ)
NEXUS TECHNOLOGY SALES
Tel: 201-947-0151
Fax: 201-947-0163

Rochester
MICRO–TECH MARKETING
Tel: 716-426-0806
Fax: 716-426-5535

NORTH AMERICAN MANUFACTURERS REPRESENTATIVES

NORTH CAROLINA
Raleigh
EMA
Tel: 919-846-6888
Fax: 919-847-7360

Charlotte
EMA
Tel: 704-553-0110
Fax: 704-553-0690

NORTH DAKOTA
(Excelsior, MN)
CBR ASSOCIATES
Tel: 612-470-2282
Fax: 612-470-2283

OHIO
New Lebanon
J.N. BAILEY & ASSOC.
Tel: 513-687-1325
Fax: 513-687-2930

Columbus
J.N. BAILEY & ASSOC.
Tel: 614-262-7274
Fax: 614-262-0384

Brunswick
J.N. BAILEY & ASSOC.
Tel: 216-273-3798
Fax: 216-225-1461

OKLAHOMA
Bixby
MREP
Tel: 918-369-6425
Fax: 918-369-5186

OREGON
Beaverton
COMPONENTS WEST
Tel: 503-520-1900
Fax: 503-520-1906

PENNSYLVANIA (EASTERN)
Horsham
NEXUS TECHNOLOGY SALES
Tel: 215-675-9600
Fax: 215-675-9604

PENNSYLVANIA (WESTERN)
New Lebanon, OH
J.N. BAILEY & ASSOC.
Tel: 513-687-1325
Fax: 513-687-2930

RHODE ISLAND
(Billerica, MA)
SIPEX CORPORATION
Tel: 508-667-8700
Fax: 508-670-9001

SOUTH CAROLINA
(Raleigh, NC)
EMA
Tel: 919-846-6888
Fax: 919-847-7360

SOUTH DAKOTA
(Excelsior, MN)
CBR ASSOCIATES
Tel: 612-470-2282
Fax: 612-470-2283

TENNESSEE (EASTERN)
(Roswell, GA)
EMA
Tel: 404-992-7240
Fax: 404-993-3426

TENNESSEE (WESTERN)
(Huntsville, AL)
EMA
Tel: 205-830-4030
Fax: 205-830-1947

TEXAS
Dallas
MREP
Tel: 214-484-5711
Fax: 214-484-0634

UTAH
(Denver, CO)
SEALE & ASSOCIATES, INC.
Tel: 303-779-8005
Fax: 303-771-1103

VERMONT
(Billerica, MA)
SIPEX CORPORATION
Tel: 508-667-8700
Fax: 508-670-9001

VIRGINIA
(Pasadena, MD)
EES
Tel: 410-255-9686
Fax: 410-255-9688

WASHINGTON, DC
(Pasadena, MD)
EES
Tel: 410-255-9686
Fax: 410-255-9688

WASHINGTON
Redmond
COMPONENTS WEST
Tel: 206-885-5880
Fax: 206-882-0642

WEST VIRGINIA
(Pittsburgh, PA)
J.N. BAILEY & ASSOC.
Tel: 412-487-8640
Fax: 412-487-8640

WISCONSIN
(Oak Brook, IL)
ATI Ltd.
Tel: 708-574-1771
Fax: 708-572-0907

WYOMING
(Denver, CO)
SEALE & ASSOCIATES, INC.
Tel: 303-779-8005
Fax: 303-771-1103

CANADA
Mississauga, Ontario
SOURCE ELECTRONICS LTD.
Tel: 905-676-0830
Fax: 905-676-0844

Ottawa
SOURCE ELECTRONICS LTD.
Tel: 819-457-1121
Fax: 819-457-1126

Montreal
SOURCE ELECTRONICS LTD.
Tel: 514-484-6340
Fax: 514-484-7301

NORTH AMERICAN DISTRIBUTORS

ALABAMA:
Huntsville
Future Electronics
Tel: 205-830-2322
Fax: 205-830-6664

Reptron Electronics, Inc.
Tel: 205-722-9500
Fax: 205-722-9565

ARIZONA:
Phoenix
Future Electronics
Tel: 602-968-7140
Fax: 602-968-0334

Jan Devices
Tel: 602-870-1190
Fax: 602-870-8873

Scottsdale
A.V.E.D. Rocky Mountain, Inc.
Tel: 602-951-9788
Fax: 602-951-4182

ARKANSAS:
Ft. Smith
Omni Pro Electronics
Tel: 501-484-5615
Fax: 501-484-5020

CALIFORNIA:
Agoura Hills
Future Electronics
Tel: 818-865-0040
Fax: 818-865-1340

Reptron Electronics, Inc.
Tel: 818-707-0377
Fax: 818-706-7651

Irvine
Bell Microproducts
Tel: 714-470-2900
Fax: 714-470-2929

Future Electronics
Tel: 714-250-4141
Fax: 714-250-4185

Reptron Electronics, Inc.
Tel: 714-450-0300
Fax: 714-450-0227

Reseda
Jan Devices
Tel: 818-757-2000
Fax: 818-708-7436

San Diego
Future Electronics
Tel: 619-625-2800
Fax: 619-625-2810

Reptron Electronics, Inc.
Tel: 619-453-8430
Fax: 619-453-1465

San Jose
Bell Microproducts
Tel: 408-451-9400
Fax: 408-451-1600

Future Electronics
Tel: 408-434-1122
Fax: 408-433-0822

Reptron Electronics, Inc.
Tel: 408-453-9933
Fax: 408-453-9941

Westlake Village
Bell Microproducts
Tel: 805-496-2606
Fax: 805-496-6119

COLORADO:
Lakewood
Future Electronics
Tel: 303-232-2008
Fax: 303-232-2009

Wheat Ridge
A.V.E.D. Rocky Mountain, Inc.
Tel: 303-422-1701
Fax: 303-422-2529

CONNECTICUT:
Cheshire
Future Electronics
Tel: 203-250-0083
Fax: 203-250-0081

Wallingford
Reptron Electronics, Inc.
Tel: 203-265-3134
Fax: 203-265-6765

Sager Electronics
Tel: 1-800-SAGER-800
Fax: 203-265-6865

FLORIDA:
Altamonte Springs
Bell Microproducts
Tel: 407-682-1199
Fax: 407-682-1286

Future Electronics
Tel: 407-865-7900
Fax: 407-865-7660

Seymour Electronics
Tel: 407-767-6974
Fax: 407-767-9667

Deerfield Beach
Bell Microproducts
Tel: 305-429-1001
Fax: 305-481-3586

Future Electronics
Tel: 305-426-4043
Fax: 305-426-3939

Ft. Lauderdale
Reptron Electronics, Inc.
Tel: 305-735-1112
Fax: 305-735-1121

Largo
Future Electronics
Tel: 813-530-1222
Fax: 813-538-9598

Orlando
Sager Electronics
Tel: 1-800-SAGER-800
Fax: 407-354-1137

Tampa
Reptron Electronics, Inc.
Tel: 813-855-4656
Fax: 813-855-7660

GEORGIA:
Norcross
Future Electronics
Tel: 770-441-7676
Fax: 770-441-7580
Reptron Electronics, Inc.
Tel: 770-446-1300
Fax: 770-446-2991

Sager Electronics
Tel: 1-800-SAGER-800
Fax: 770-446-0430

Seymour Electronics
Tel: 770-441-7878
Fax: 770-441-1001

Woodstock
Bell Microproducts
Tel: 770-592-1010
Fax: 770-592-1111

ILLINOIS:
Bensenville
Omni Pro Electronics
Tel: 708-350-0550
Fax: 708-350-0759

Schaumburg
Future Electronics
Tel: 708-882-1255
Fax: 708-490-9290

Marsh Electronics
Tel: 708-303-0100
Fax: 708-303-0023

Reptron Electronics, Inc.
Tel: 708-882-1700
Fax: 708-882-8904

Sager Electronics
Tel: 1-800-SAGER-800
Fax: 708-882-9776

INDIANA:
Carmel
Marsh Electronics
Tel: 317-575-4800
Fax: 317-575-4810

Indianapolis
Custom Service Electronics
Tel: 317-879-9119
Fax: 317-879-9136

Future Electronics
Tel: 317-469-0447
Fax: 317-469-0448

KANSAS:
Overland Park
Future Electronics
Tel: 913-649-1531
Fax: 913-649-1786

MARYLAND:
Berlin
Jan Devices
Tel: 410-208-0500
Fax: 410-641-7450

Columbia
Bell Microproducts
Tel: 410-720-5100
Fax: 410-381-2172

Future Electronics
Tel: 410-290-0600
Fax: 410-290-0328

Reptron Electronics, Inc.
Tel: 410-290-5113
Fax: 410-290-7650

Sager Electronics
Tel: 1-800-SAGER-800
Fax: 410-381-9380

Seymour Electronics
Tel: 410-992-7474
Fax: 410-992-7410

MASSACHUSETTS:
Billerica
Bell Microproducts
Tel: 508-667-2400
Fax: 508-663-7474

Bolton
Future Electronics
Tel: 508-779-3000
Fax: 508-779-3050

Burlington
Reptron Electronics, Inc.
Tel: 617-273-2800
Fax: 617-229-2815

Hingham
Sager Electronics
Tel: 1-800-SAGER-800
Fax: 617-740-2559

Melrose
Jan Devices
Tel: 617-662-3901
Fax: 617-662-0837

Norwood
Gerber Electronics
Tel: 617-769-6000
Fax: 617-762-8931

Wilmington
Sager Electronics
Tel: 1-800-SAGER-800
Fax: 508-657-6559

MICHIGAN:
Grand Rapids
Calder Electronics
Tel: 616-698-7400
Fax: 616-698-9216

Future Electronics
Tel: 616-698-6800
Fax: 616-698-6821

Kentwood
Custom Service Electronics
Tel: 616-285-1060
Fax: 616-285-1065

Livonia
Future Electronics
Tel: 313-261-5270
Fax: 313-261-8175

Reptron Electronics, Inc.
Tel: 313-525-2700
Fax: 313-525-3209

Troy
Marsh Electronics
Tel: 810-689-0299
Fax: 810-689-0139

MINNESOTA:
Bloomington
Marsh Electronics
Tel: 612-948-0464
Fax: 612-948-0467

Eden Prairie
Future Electronics
Tel: 612-944-2200
Fax: 612-944-2520

Edina
Bell Microproducts
Tel: 612-933-3236
Fax: 612-933-3415

Plymouth
Reptron Electronics, Inc.
Tel: 612-559-0000
Fax: 612-553-0753

MISSOURI:
St. Louis
Future Electronics
Tel: 314-469-6805
Fax: 314-469-7226

NEW HAMPSHIRE:
Sager Electronics
Tel: 1-800-SAGER-800
Fax: 603-898-2741

NEW JERSEY:
Clifton
Bell Microproducts
Tel: 201-777-4100
Fax: 201-777-6194

Marlton
Future Electronics
Tel: 609–596–4080
Fax: 609–596–4266

Mount Laurel
Seymour Electronics
Tel: 609-235-7474
Fax: 609-235-4992

Parsippany
Future Electronics
Tel: 201-299–0400
Fax: 201-299-1377

NEW YORK:
Hauppauge
Future Electronics
Tel: 516-234-4000
Fax: 516-234-6183

Sager Electronics
Tel: 1-800-SAGER-800
Fax: 516-348-1006

Rochester
Future Electronics
Tel: 716-387-9550
Fax: 716-387-9563

Smithtown
Bell Microproducts
Tel: 516-543-2000
Fax: 516-543-2030

Syracuse
Future Electronics
Tel: 315-451-2371
Fax: 315-451-7258

Woodbury
Seymour Electronics
Tel: 516-496-7474
Fax: 516-496-0857

NORTH CAROLINA:
Raleigh
Future Electronics
Tel: 919-790-7111
Fax: 919-790-9022

Reptron Electronics, Inc.
Tel: 919-870-5189
Fax: 919-870-5210

Sager Electronics
Tel: 1-800-SAGER-800
Fax: 919-850-9559

OHIO:
Akron
Sager Electronics
Tel: 1-800-SAGER-800
Fax: 216-864-4620

Beavercreek
Future Electronics
Tel: 513-426-0090
Fax: 513-426-8490

Cincinnati
Schuster Electronics
Tel: 513-489-1400
Fax: 513-489-8686

Dayton
Sager Electronics
Tel: 1-800-SAGER-800
Fax: 513-898-4455

Mayfield Heights
Future Electronics
Tel: 216-449-6996
Fax: 216-449-8987

Solon
Reptron Electronics, Inc.
Tel: 216-349-1415
Fax: 216-349-1634

Twinsburg
Schuster Electronics
Tel: 216-425-8134
Fax: 216-425-1863

OREGON:
Beaverton
Future Electronics
Tel: 503-645-9454
Fax: 503-645-1559

Reptron Electronics, Inc.
Tel: 503-629-2082
Fax: 503-629-8645

PENNSYLVANIA:
Ambler
Bell Microproducts
Tel: 215-540-4148
Fax: 215-540-4149

Horsham
Reptron Electronics, Inc.
Tel: 215-672-6055
Fax: 215-672-4966

NORTH AMERICAN DISTRIBUTORS

Langhorne
Sager Electronics
Tel: 1-800-SAGER-800
Fax: 215-750-8327

Pittsburgh (Cranberry Township)
Sager Electronics
Tel: 1-800-SAGER-800
Fax: 412-772-3845

PUERTO RICO:
Florida
Future Electronics
Tel: 800-305-2343
Fax: 305-426-3939

TEXAS:
Austin
Bell Microproducts
Tel: 512-258-0725
Fax: 512-258-6517

Future Electronics
Tel: 512-502-0991
Fax: 512-502-0740

Omni Pro Electronics
Tel: 512-794-9200
Fax: 512-338-9576

Carrollton
Omni Pro Electronics
Tel: 214-233-0500
Fax: 214-732-8743

Houston
Future Electronics
Tel: 713-785-1155
Fax: 713-785-4558

Omni Pro Electronics
Tel: 713-270-1700
Fax: 713-270-8020

Richardson
Bell Microproducts
Tel: 214-783-4191
Fax: 214-783-4192

Future Electronics
Tel: 214-437-2437
Fax: 214-669-2347

Sager Electronics
Tel: 1-800-SAGER-800
Fax: 214-783-4240

UTAH:
Midvale
A.V.E.D. Rocky Mountain, Inc.
Tel: 801-565-8300
Fax: 801-565-9983

Salt Lake City
Future Electronics
Tel: 801-467-4448
Fax: 801-467-3604

VIRGINIA:
Herndon
Bell Microproducts
Tel: 703-834-3696
Fax: 703-834-3698

WASHINGTON:
Bellevue
Reptron Electronics, Inc.
Tel: 206-453-1699
Fax: 206-453-1827

Bothell
Future Electronics
Tel: 206-485-6616
Fax: 206-485-6109

Redmond
Bell Microproducts
Tel: 206-861-5710
Fax: 206-885-5399

WISCONSIN:
Brookfield
Future Electronics
Tel: 414-879-0244
Fax: 414-879-0250

Milwaukee
Marsh Electronics
Tel: 414-475-6000
Fax: 414-771-2847

CANADA:
Pointe Claire, Quebec
Future Electronics
Tel: 514-694-7710
Fax: 514-695-3707

Quebec City, Quebec
Future Electronics
Tel: 418-877-6666
Fax: 418-877-6671

Mississauga, Ontario
Future Electronics
Tel: 905-612-9200
Fax: 905-612-9185

Ottawa, Ontario
Future Electronics
Tel: 613-820-8313
Fax: 613-820-3271

Calgary, Alberta
Future Electronics
Tel: 403-250-5551
Fax: 403-291-7054

Edmonton, Alberta
Future Electronics
Tel: 403-438-2858
Fax: 403-434-0812

Vancouver, British Columbia
Future Electronics
Tel: 604-294-1166
Fax: 604-294-1206

INTERNATIONAL MANUFACTURERS REPRESENTATIVES

AUSTRIA:
CODICO GES. MBH AND CO. KG
Muhlgasse 86-88
A-2380 Perchtoldsdorf
Tel: 43-1-86305-0
Fax: 43-1-86305-98

BELGIUM:
TRADEMARK ELECTRONICS
Bisschoppenhoflaan 357-359
2100 Antwerp, Belgium
Tel: 32-3-325-1910
Fax: 32-3-326-0510

BIH/KROATIEN:
ELATEC
Kucerina 5
HR-41000 Zagreb
Kroatien
Tel: 385-41-453-350
Fax: 385-41-453-356

BULGARIA:
ELATEC
Tzarigradsko shosse 7th KM
BG-1184 Sofia
Tel: 359-2-771-580
Fax: 359-2-772-188

DENMARK:
SUPPLY-TEAM
Handvaerkerbyen 18
DK-2670 Greve
Tel: 45-42-902333
Fax: 45-42-904890

EASTERN EUROPE
(HEADQUARTERS):
ELATEC VERTRIEBS GMBH
Bretonischer Ring 11
D-85630 Grasbrunn
Tel: 49-89-463018
Fax: 49-89-4602403

FINLAND:
INTEGRATED ELECTRONICS OY AB
Turkhaudantie 1
FIN-00700 Helsinki
Tel: 358-0-3513133
Fax: 358-0-3513134

FRANCE:
LINEAR SEMICONDUCTOR
EXCELLENCE (LSX)
30 Rue Du Morvan, SILIC 525
94633 Rungis Cedex
Tel: 33-1-4687-8336
Fax: 33-1-4560-0784

HONG KONG:
ELECTRONIC SCIENTIFIC
ENGINEERING LTD
20/F Shun Tak Centre
200 Connaught Road
Central Hong Kong
Tel: 852-2559-2041
Fax: 852-2858-2555

HUNGARIA:
ELATEC
Peterdy u. 15
Alag Center Pest III-rd floor
H-1071 Budapest
Tel: 36-1-351-75-91
Fax: 36-1-351-75-90

INDIA:
VENTRONICS PVT. LTD
820, 8th Main, 4th Block, BEL Layout
Vidyaranyapura, Jalahalli,
Bangalore-560 097
Tel: 91-80-8382191/8381199
Fax: 91-80-8382191

ISRAEL:
SEG TEC
3 Hametsuda St., Industrial Park
Azur 58001,
Tel: 972-3-556-7458
Fax: 972-3-556-9490

ITALY:
CELTE S.R.L.
V. le Lombardia 15
20131 Milano
Tel: 39-2-266-6295
Fax: 39-2-266-6960

JAPAN:
TOKYO MUSEN KIZAI CO. LTD.
3-7, Sotokanda 2-Chome, Chiyoda-ku
Tokyo 101
Tel: 81-3-3253-0545
Fax: 81-3-3255-2738

NIPPON SIPEX CORPORATION
Haibara Building, 2-3-7 Sotokanda
Chiyoda-ku Tokyo 101
Tel: 81-3-3254-5822
Fax: 81-3-3254-5824

KOREA:
SUNHO CORPORATION
Seoul Young Dong P.O. Box 1846
Seoul
Tel: 822-558-4415
Fax: 822-558-4412

NETHERLANDS:
ADDED VALUE ELECTRONICS
Vissersdijk Beneden 17
3319 GW Dordrecht, Netherlands
Tel: 31-78-6215900
Fax: 31-78-6215815

NORWAY:
BEXAB NORGE
Vestvollveien 10 P.O. Box 84
N–2020 Skedsmokorset
Tel: 47-63874900
Fax: 47-63875900

POLAND:
ELATEC
ul.T. Kantora 5/17
PL-31-445 Krakow
Tel: 48-12-121-359
Fax: 48-12-121-359

ROMANIA:
ELATEC
Peterdy u. 15
Alag Center Pest III-rd floor
H-1071 Budapest
Hungaria
Tel: 36-1-351-75-91
Fax: 36-1-351-75-90

SINGAPORE:
SABRE TECHNOLOGIES PTE. LTD
104 Boon Keng Road
#07-07 Kallang Basin Industrial Estate
Singapore 1233
Tel: 65-2932003
Fax: 65-2930661

SOUTH AFRICA:
COMMUNICA LTD
29011 Sunnyside
0132 Pretoria
Tel: 27-12-3227613/3227621
Fax: 27-12-3223721

SPAIN & PORTUGAL:
ANATRONIC S.A.
Avda. Valladolid 27
28008 Madrid
SPAIN
Tel: 34-1-542-4455
Fax: 34-1-559-6975

SWEDEN:
LAC ELEKTRONIK
Box 5036
131-05 Nacka-Stockholm
Tel: 46-8-642-8300
Fax: 46-8-642-8303

TAIWAN:
KALTEC INT'L LTD
No. 18, Lane 46, Sec 2,
Shuang Shi Road
Panchiao
Taipei
Tel: 886-2-255-5711
Fax: 886-2-253-7636

TSCHECHIAN REPUBLIC:
ELATEC
Prazska 53/II
CZ-566 01 Vysoke Myto
Tel: 42-468-221-60
Fax: 42-468-221-60

UNITED KINGDOM:
MB COMPONENTS LTD.
2 Linden House
Turk Street
ALTON, Hampshire GU34 1AN
ENGLAND
Tel: 44-1420-542500
Fax: 44-1420-542700

INTERNATIONAL DISTRIBUTORS

AUSTRALIA:
AVNET/VSI ELECTRONICS
6-8 Lyon Park Road, Unit C
North Ryde, NSW 2113
Tel: 61-2-878-1299
Fax: 61-2-878-1266

FRANCE:
FUTURE ELECTRONICS
Parc Technopolis - LP 854 Les ULIS
3 Avenue du Canada Bat. Theta 2
91 974 Courtaboeuf Cedex
Tel: 33-1-6982-1111
Fax: 33-1-6982-1100

GERMANY:
FUTURE ELECTRONICS
Munchner Strasse 18
85774 Unterfohring
Tel: 49-89-95727143
Fax: 49-89-95727144

KARL-HEINZ-DREYER
Albert-Schweitzer-Ring 36
D-22045 Hamburg, Germany
Tel: 49-40-6695227+28
Fax: 49-40-6684030

MEV ELEKTRONIK SERVICE GmbH
Heinrich-Hasemeier Str. 26
D-49076 Osnabruck
Tel: 49-541-13908-0
Fax: 49-541-13908-39

IRELAND:
FUTURE ELECTRONICS
26 Merchants Sq.
Ennis, County Clare
Tel: 353-65-41330
Fax: 353-65-40654

ITALY:
COMPREL spa
Via Po 37
20031 Cesano Maderno (MI) Italy
Tel: 39-362-553991
Fax: 39-362-553967

NEW ZEALAND:
VSI ELECTRONICS (NZ) PTY LTD
274 Church Street
Penrose, Aukland
Tel: 64-9-636-7801
Fax: 64-9-636-7803

SINGAPORE:
FUTURE ELECTRONICS
#16-02 BP Tower
396 Alexandra Road
Singapore 0511
Tel: 65-479-1300
Fax: 65-479-3151

SWITZERLAND:
MILGRAY DISTRIBUTION
R. Knuchel Electronics
Weiherweg 45
CH-2562 Port
Tel: 41-32-512064
Fax: 41-32-511359

UNITED KINGDOM:
FUTURE ELECTRONICS
Future House
Poyle Road
Colnbrook
Berkshire SL30EZ
Tel: 44-1753-763000
Fax: 44-1753-689100

HERO ELECTRONICS LTD.
Dunstable Street
Ampthill
Bedfordshire MK45 2JS
England
Tel: 44-1525-405015
Fax: 44-1525-402383

Sipex Corporation

Headquarters and Main Offices:

22 Linnell Circle
Billerica, MA 01821
Tel: (508) 667-8700
Fax: (508) 670-9001

491 Fairview Way
Milpitas, CA 95035
Tel: (408) 945-9080
Fax: (408) 946-6191

North American Sales Offices:

22 Linnell Circle
Billerica, MA 01821
Tel: (508) 667-8700
Fax: (508) 670-9001

International Sales Offices:

FRANCE

Sipex S.A.R.L.
30 Rue du Morvan,
SILIC 525
94633 Rungis Cedex
Tel: 33-1-4687-8336
Fax: 33-1-4560-0784

GERMANY

Sipex GmbH
Gautinger Strasse 10
82319 Starnberg
Tel: 49-8151-89810
Fax: 49-8151-29598

United Kingdom

MB Components Ltd.
2 Linden House
Turk Street
Alton, Hampshire
England GU34 1AN
Tel: 44-1420-542500
Fax: 44-1420-542700

JAPAN

Nippon Sipex Corporation
Haibara Building
2-3-7 Sotokanda
Chiyoda-ku
Tokyo 101
Tel: 81-3-3254-5822
Fax: 81-3-3254-5824

Tokyo Musen Kizai Co. Ltd.
3-7, Sotokanda 2-Chome,
Chiyoda-ku
Tokyo 101
Tel: 81-3-3253-0545
Fax: 81-3-3255-2738

Sipex
22 Linnell Circle
Billerica, MA 01821
508–667–8700
FAX: 508–670–9001

SIGNAL PROCESSING EXCELLENCE