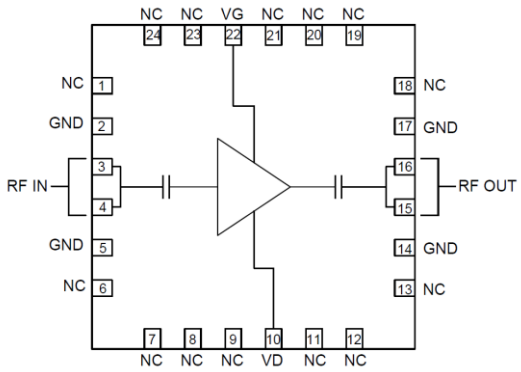
5.0 – 6.0GHz 1 Watt Power Amplifier

Features

- **Frequency Range : 5.0 – 6.0GHz**
- **32 dBm Psat**
- **24 dB Small Signal Gain**
- **35% PAE**
- **Input Return Loss ≥ 10 dB**
- **Output Return Loss ≥ 13 dB**
- **No external matching required**
- **DC decoupled input and output**
- **Package dimension: 4mm x 4mm**

Functional Diagram



Typical Applications

- **RADAR**
- **Military & space**
- **LMDS, VSAT**

Description

The ASL4050P4 is a C-band Power amplifier packaged in 4mm x 4mm QFN package. The PA uses 2 stages of amplification and operates in 5.0 – 6.0GHz frequency range. It features 24dB of gain with input and output return losses of 10dB and 13dB respectively. The PA has output power of 32dBm. This feature enables it to be used in the applications requiring efficiency along with linearity. The chip operates with dual bias supply voltage. The Circuit grounds are provided through vias to the backside metallization.

Absolute Maximum Ratings (1)

Parameter	Absolute Maximum	Units
Drain bias voltage (Vd)	+9	volts
Drain current (Id)	0.6	A
RF input power (RFin at Vd=9V)	30	dBm
Operating temperature	-50 to +85	^{o}C
Storage Temperature	-65 to +150	^{o}C

1. Operation beyond these limits may cause permanent damage to the component

Electrical Specifications [1] @ T_A = 25 °C, V_d = 8V, I_{dq} = 280mA; Z_o =50 Ω

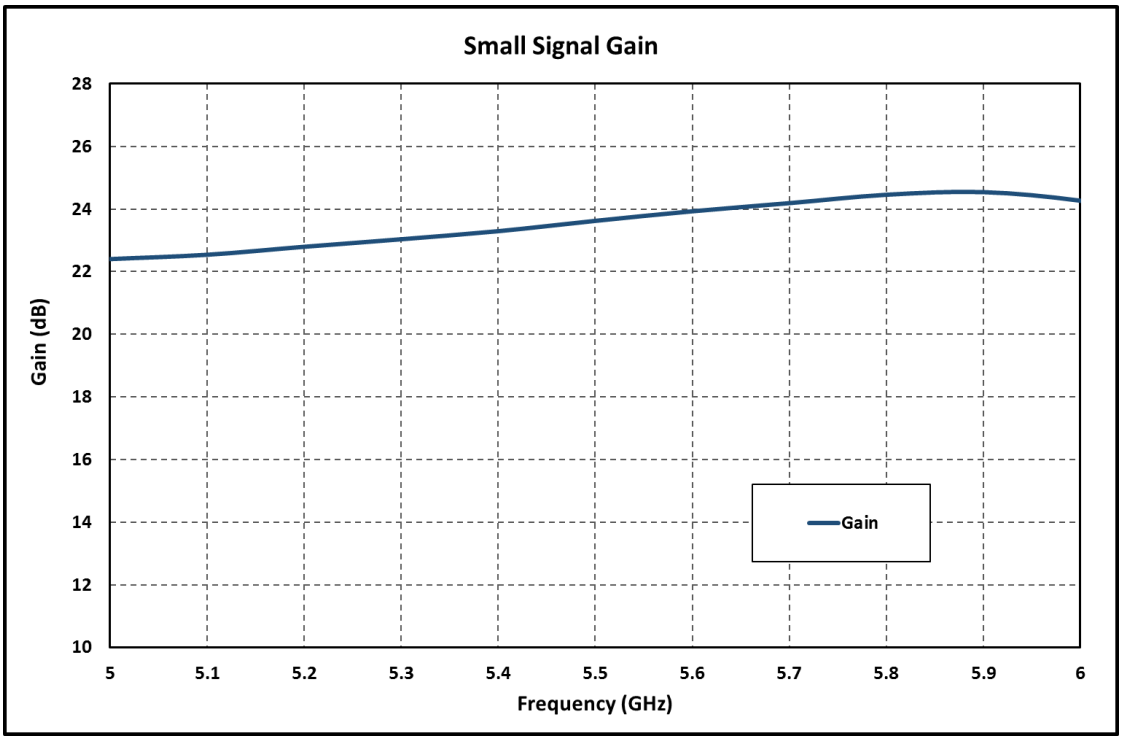
Parameter	Min.	Typ.	Max.	Units
Frequency Range	5.0		6.0	GHz
Gain	22	24		dB
Gain Flatness		+/-1		dB
Output Power (P1 dB)	30.5	31		dBm
Input Return Loss		10		dB
Output Return Loss		14		dB
Saturated output power (Psat)	31.5	32		dBm
Gate Voltage (V_g)	-1.2	-1	-0.7	V
Supply Current(I_{dq})		280[2]		mA
Supply Current(I_{dsat})		480[3]		mA

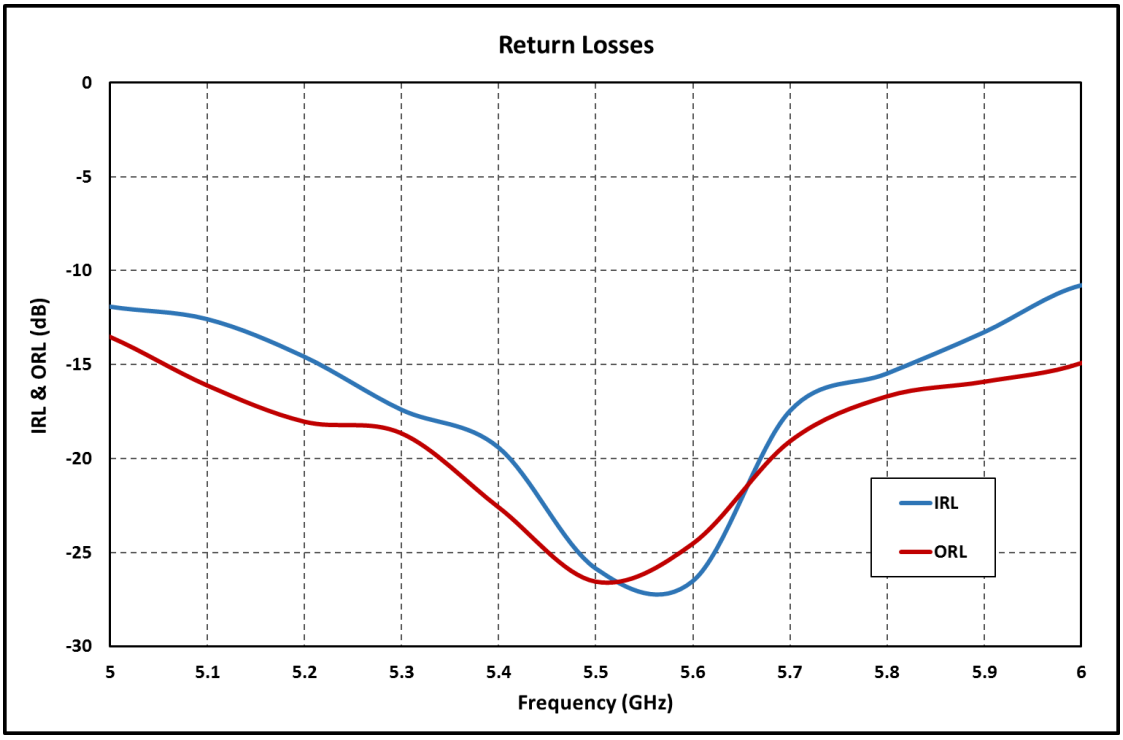
Note:

1. Electrical specifications as measured in test fixture.
2. Gate voltage to be adjusted to meet Idq.
3. I_{dsat} is the maximum current over input RF drive condition.

Test fixture data

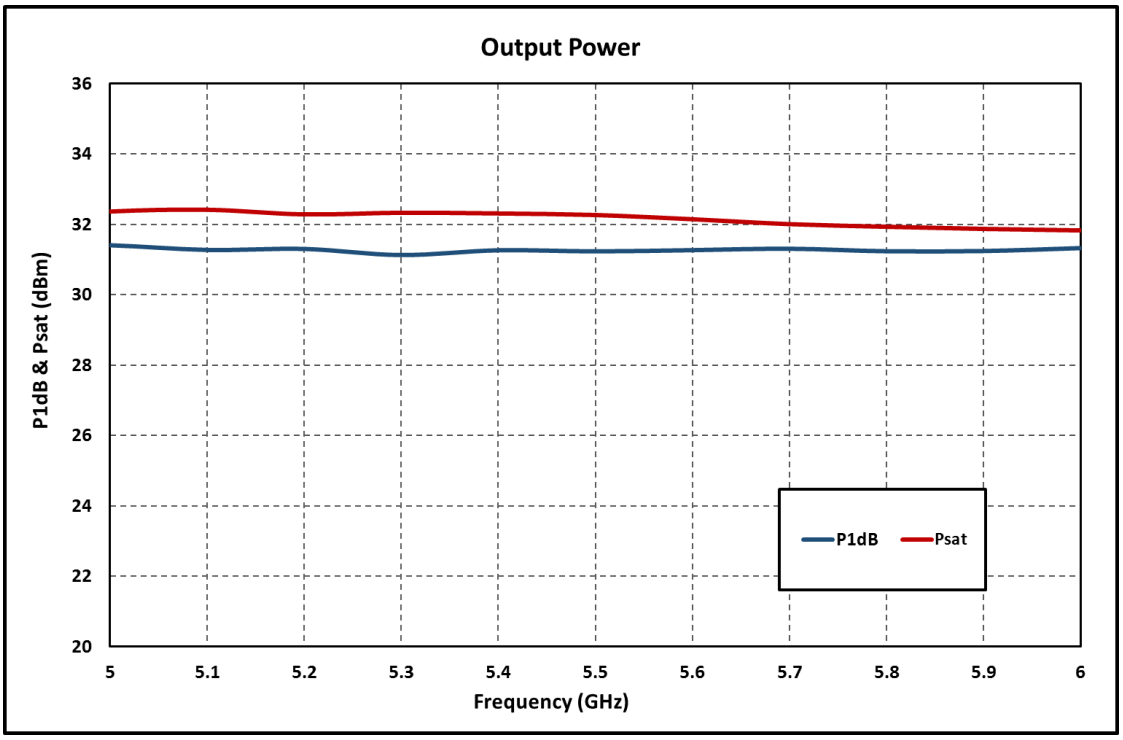
V_d = 8V, V_g = -1V, Total Current (I_{dq}) =280mA, T_A = 25 °C

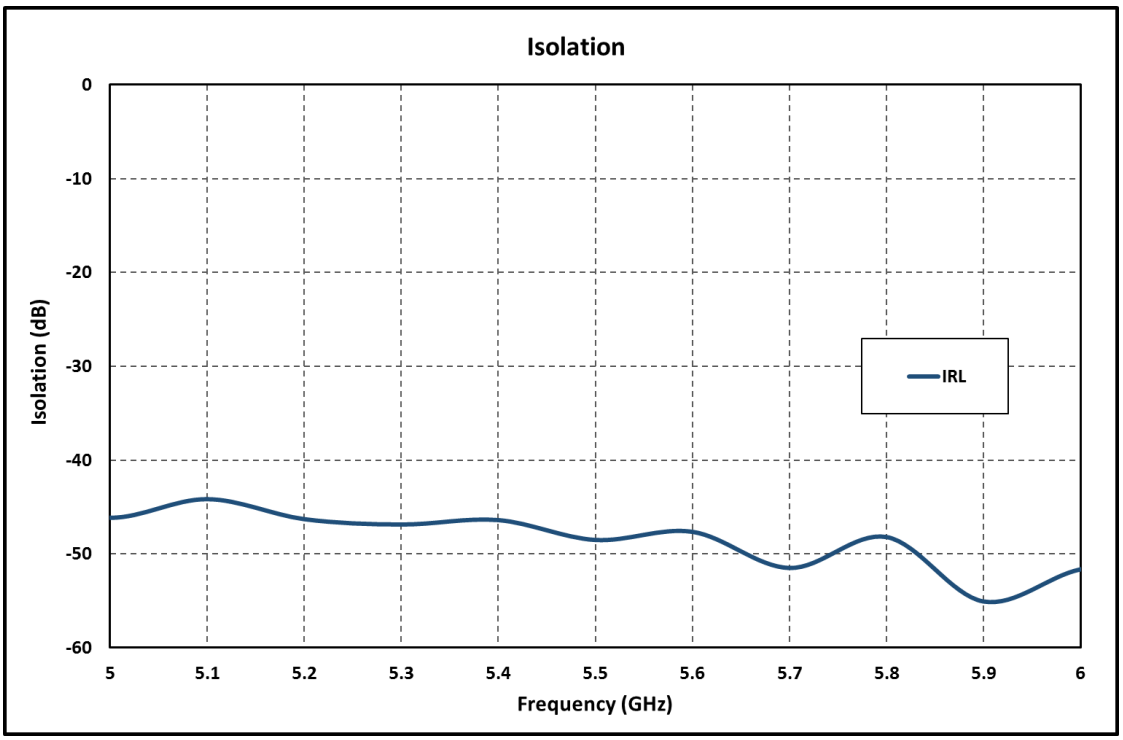




Test fixture data

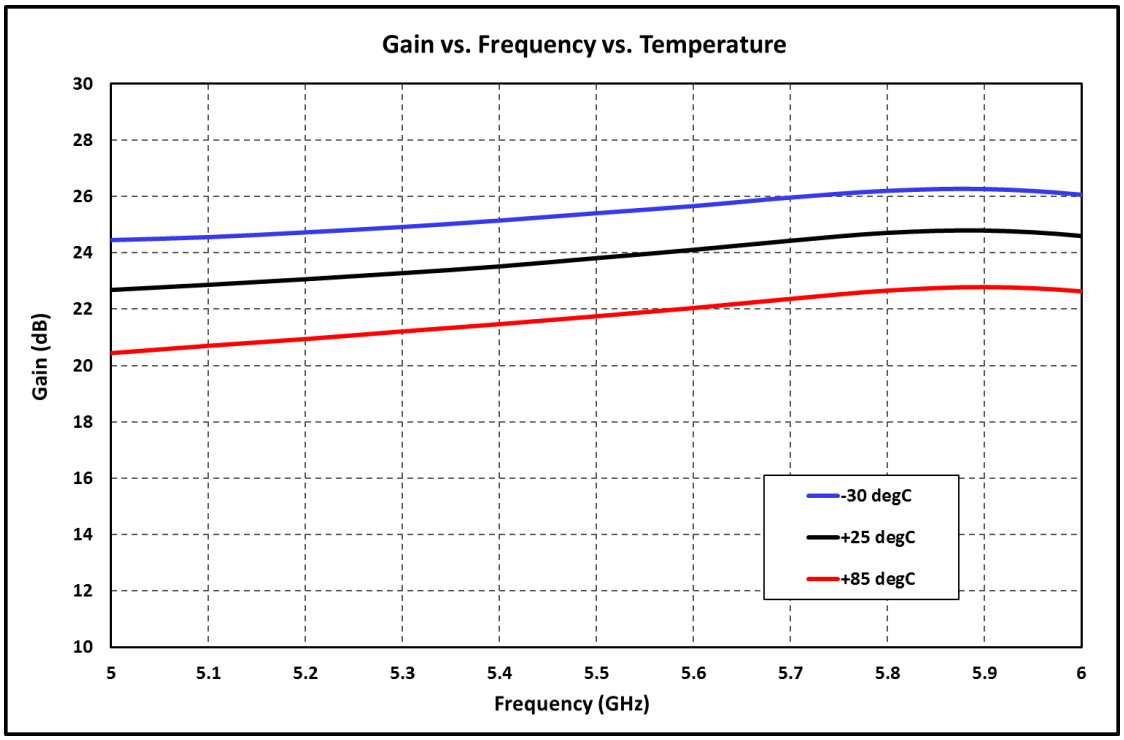
V_d = 8V, V_g = -1V, Total Current (I_{dq}) =280mA, T_A = 25 °C

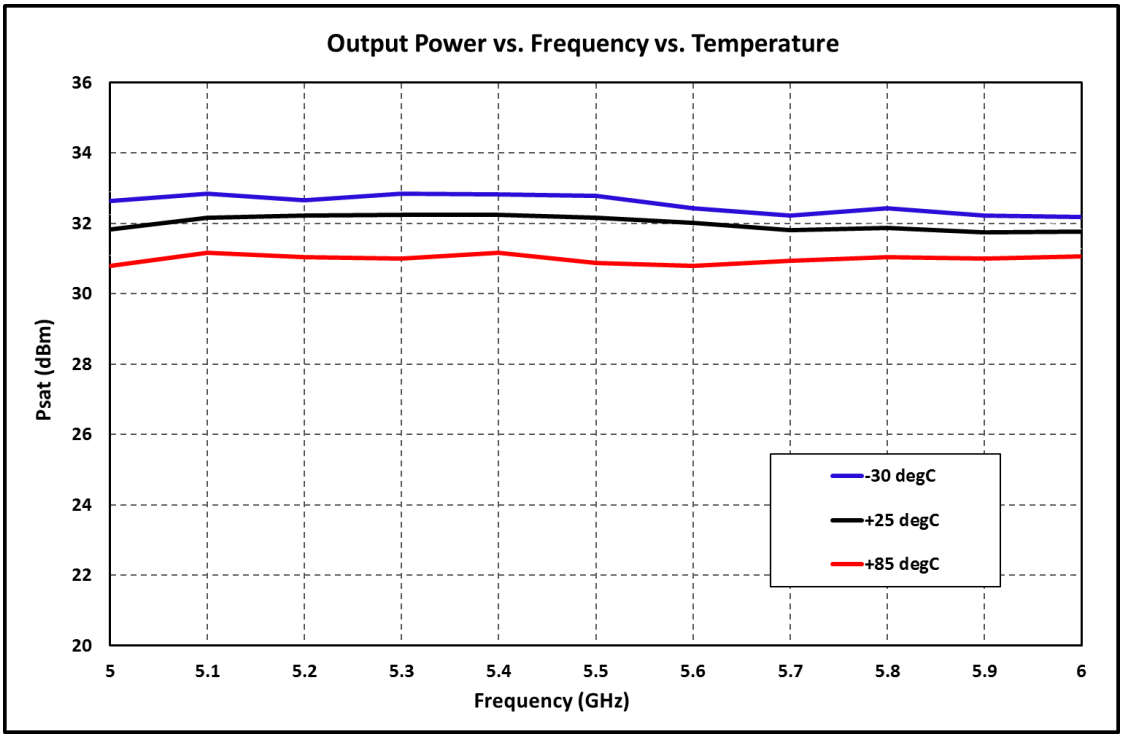




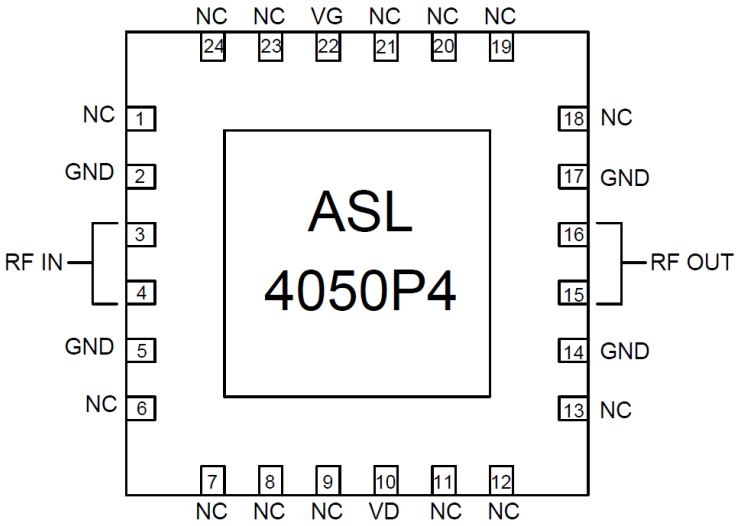
Temperature Analysis data

V_d = 8V, V_g = -1V, Total Current (I_{dq}) =280mA





Pin Configuration Details

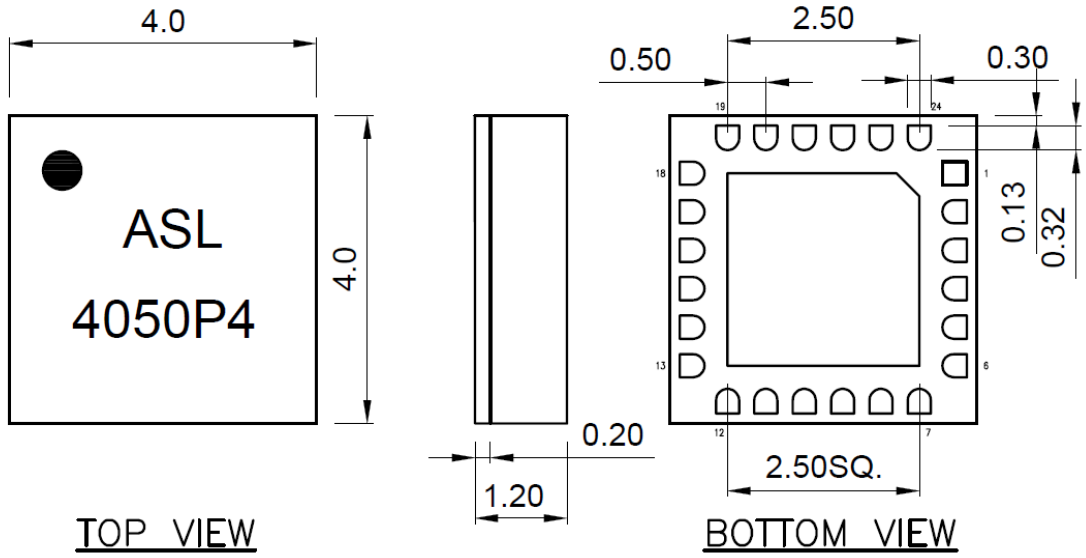


Pin Description:

Pin 3 & 4 : RF IN
Pin 10 : VD (Drain bias voltage)
Pin 15 &16 : RF OUT
Pin 22 : VG (Gate bias voltage)
Pin 2, 5, 14 & 17 : Ground

Remaining all other pins are NC (No Connection)

QFN package outline



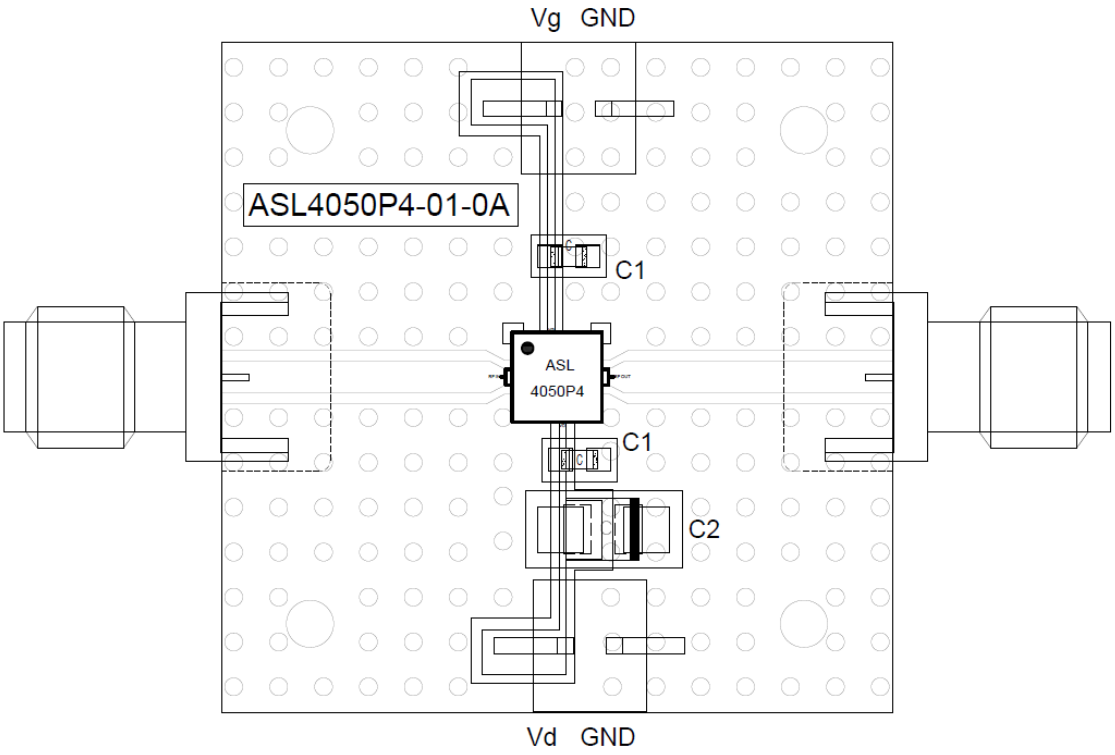
Units: Millimeters.

Package Surface:

1. **Plating (Electroless)**

   Ni/Pd/Au **Ni: 1.27~8.89µm, Pd: 0.07~0.17µm, Au: 0.02~0.08µm.**

Recommended Assembly Diagram



Bill of Material

Component ID	Value	Description	Part Number	QTY.
C1	1 µF	CAP MCC 1UF±10% 16V 0402 X7R	0402X105K160ST	2
C2	1 µF	CAP CHIP TANT 1UF±10% 35V 3528(B)CASESTD	-	1

Note:

1. Input and output 50 ohm lines are on 20mil RT Duroid 5880 substrate.

GaAs MMIC devices are susceptible to Electrostatic discharge. Proper precautions should be observed during handling, assembly & testing

All Information and Specifications are subject to change without prior notice. Before using the product, please refer to the latest datasheet available in the website.