ATMEL AT7913E

SpaceWire Remote Terminal Controller (RTC)

DATASHEET

Features

- LEON2-FT Sparc V8 Processor
  - 5 stage pipeline
  - 4K instruction caches / 4K data caches
  - Meiko FPU
  - Interrupt Controller
  - Uart serial links
  - 32-bit Timers
  - Memory interface
  - General purpose IO
  - Debug Support Unit (DSU)
- FIFO interface
- ADC/DAC interface
  - 24 channels
  - 8bit/16bit wide data bus
- Two CAN interface
  - CAN interface supporting nominal and redundant bus connection
- Two Bidirectional SpaceWire links
  - RMAP support
  - Full duplex communication
  - Transmit rate from 1.25 up to 200 Mbit/s in each direction
- SpaceWire Link Performance
  - At 3.3V : 200Mbit/s full duplex communication
- JTAG Interface
- Operating range
  - Voltages
    - 1.65V to 1.95V - core
    - 3V to 3.6V - I/O
  - Temperature
    - - 55°C to +125°C
- Power consumption : 1W at 50MHz
- Radiation Performance
  - Tested up to a total dose of 300 Krad (Si) according to the MIL-STD883 method 1019
  - No single event latchup below a LET of 80 MeV/mg/cm2
- ESD better than 1000V
- Quality Grades
- QML-Q or V with SMD

- Package:
  - 349 pins MCGA, MLGA
  - 352 pins CQFP

Description

The SpaceWire Remote Terminal Controller (SpW-RTC) ASIC is a single chip embedded system that includes a general purpose LEON2-FT SPARC V8 core with a MEIKO FP unit (IEEE-754). This architecture provides the mixed capability to effectively perform data handling at platform level and powerful data processing at payload level. The SpW-RTC includes both CAN and SpaceWire interfaces which allows bridging traffic from sensor networks onto a high data rate SpaceWire network. Its EDAC protected FIFO and memory interfaces allows interfacing towards peripheral I/O that may perform specialised data processing tasks.

The SpaceWire-RTC device includes an embedded microprocessor, a CAN bus controller, ADC/DAC interfaces for analogue acquisition/conversion, standard interfaces and resources (UARTs, timers, general purpose input output).

The SpaceWire-RTC device can be operated stand-alone or with a number of external devices such as SRAM, PROM and FIFO memories, ADC and DAC converters. The device can be managed locally by the on-chip processor, or remotely via its SpaceWire link interfaces. SpaceWire-RTC device can operate as a single-chip system, with software being uploaded to its on-chip memory via the SpaceWire link interface, forming a compact solution for remotely controlled applications. Or it can operate in a full-size system, with software being decompressed from local PROM and executed from multiple fast and wide SRAM memory banks. The device provides scalability in terms of use of external devices and operating frequency.

Figure 1. AT7913E SpaceWre RTC Block Diagram

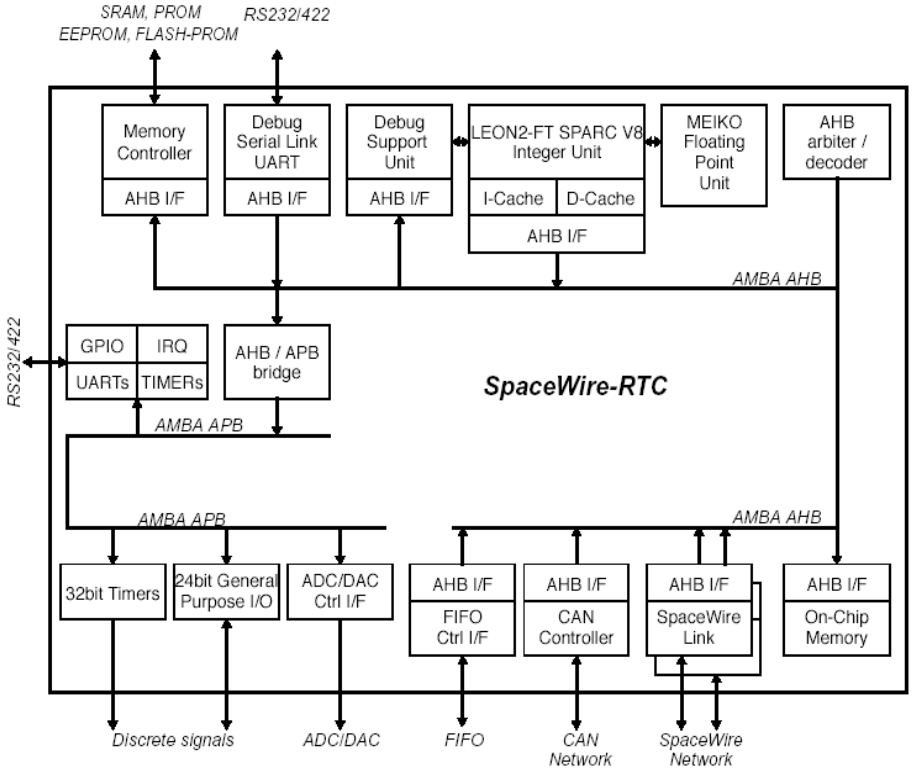


Table of Contents

1. Pin Description

1.1 System

SysClk – Input

System Clock

SysResetN - Input

System Reset

LeonErrorN - IO, open-drain, output

LEON Error - This active low output is asserted when the processor has entered error state and is halted. This happens when traps are disabled and an synchronous (un-maskable) trap occurs.

LeonWDN - IO, open-drain, output

LEON watchdog - This active low output is asserted when the watchdog times-out.

LeonDsuEn - Input

DSU enable - The active high input enables the DSU unit. If de-asserted, the DSU trace buffer will continue to operate but the processor will not enter debug mode.

LeonDsuTx – Output

DSU UART transmit - This active high output provides the data from the DSU communication link transmitter

LeonDsuRx - Input

DSU UART receive - This active high input provides the data to the DSU communication link receiver.

LeonDsuBre - Input

DSU break - A low-to-high transition on this active high input will generate break condition and put the processor in debug mode

LeonDsuAct – Output

DSU active - This active high output is asserted when the processor is in debug mode and controlled by the DSU.

LeonPio[15:0] - IO

LEON Parallel Input / Output - These bi-directional signals can be used as inputs or outputs to control external devices.

Gpio[23:0] - IO

General Purpose Input / Output

TimeClk - Input

External timer clock

TimeTrig[2:1] – Output

External timer trigger - Asserted for 8 system clock periods

1.2 CAN Interface

CanTx[1:0] – Output

CAN transmit

CanRx[1:0] - Input

CAN receive

CanEn[1:0] – Output

CAN transmit enable

1.3 ADC/DAC Interface

ADData[15:0] - IO

ADC/DAC data

ADAddr[7:0] - IO

ADC/DAC address

ADWr - Output

DAC write strobe

ADCs - Output

ADC chip select

ADRc - Output

ADC read/convert

ADRdy - Input

ADC ready

ADTrig - Input

ADC trigger

1.4 Memory Interface

MemA[22:0] – Output

Memory interface address - These active high outputs carry the address during accesses on the memory bus. When no access is performed, the address of the last access is driven (also internal cycles).

MemD[31:0] - IO

Memory interface data - MemD[31:0] carries the data during transfers on the memory bus. The processor only drives the bus during write cycles. During accesses to 8-bit areas, only MemD[31:24] are used.

MemCB[7:0] - IO

Memory interface checkbits MemCB[6:0] carries the EDAC checkbits, MemCB[7] takes the value of TB[7] in the error control register. The processor only drive MemCB[7:0] during write cycles to areas programmed to be EDAC protected

MemCsN[3:0] – Output

SRAM chip select - These active low signals provide an individual output enable for each SRAM bank.

MemOeN[3:0] – Output

SRAM output enable -These active low outputs provide the chip-select signals for each SRAM bank.

MemWrN[3:0] – Output

SRAM byte write strobe - These active low outputs provide individual write strobes for each byte lane. MemWrN[0] controls MemD[31:24], MemWrN[1] controls MemD[23:16], etc.

RomCsN[1:0] – Output

PROM chip select - These active low outputs provide the chip-select signal for the PROM area. RomCsN[0] is asserted when the lower half of the PROM area is accessed (0 - 0x10000000), while RomCsN[1] is asserted for the upper half.

IoCsN – Output

I/O area chip select - This active low output is the chip-select signal for the memory mapped I/O area.

IoOeN – Output

I/O area output enable - This active low output is asserted during read cycles on the memory bus.

IoRead – Output

I/O area read - This active high output is asserted during read cycles on the memory bus.

IoWrN – Output

I/O area write - This active low output provides a write strobe during write cycles on the memory bus.

IoBrdyN - Input

I/O area ready - This active low input indicates that the access to a memory mapped I/O area can be terminated on the next rising clock edge.

MemBExcN -Input

Memory exception - This active low input is sampled simultaneously with the data during accesses on the memory bus. If asserted, a memory error will be generated.

1.5 FIFO Interface

FifoD[15:0] - IO

FIFO data

FifoP[1:0] - IO

FIFO parity

FifoRdN - Output

FIFO read strobe

FifoWrN – Output

FIFO write strobe

FifoFullN - Input

FIFO full

FifoEmpN - Input

FIFO empty

FifoHalfN - Input

FIFO half-full, half-empty

1.6 SpaceWire Interface

SpwClkSrc - Input

SpaceWire transmitter clock source

SpwClkMult[1:0] - Input

SpaceWire clock configuration

SpwClk10Mbit[2:0] - Input

SpaceWire clock configuration

SpwClkPllCnfg[2:0] - Input

SpaceWire clock configuration

SpwClkMuxSel - Input

SpaceWire clock configuration - configuration External clock when 1, internal PLL when 0.

SpwDIn_P[1:0] - Input, LVDS positive

SpaceWire Data input, positive

SpwDIn_N[1:0] - Input, LVDS negative

SpaceWire Data input, negative

SpwSIn_P[1:0] - Input, LVDS positive

SpaceWire Strobe input, positive

SpwSIn_N[1:0] - Input, LVDS negative

SpaceWire Strobe input, negative

SpwDOut_P[1:0] - Output, LVDS positive

SpaceWire Data output, positive

SpwDOut_N[1:0] - Output, LVDS negative

SpaceWire Data output, negative

SpwSOut_P[1:0] - Output, LVDS positive

SpaceWire Strobe output, positive

SpwSOut_N[1:0] - Output, LVDS negative

SpaceWire Strobe output, negative

LvdsRef[0:1] - Power

LVDS reference voltage for SpaceWire channels

1.7 JTAG

TAPTRST - Test Reset

Tap Reset - Resets the test state machine. Can be asynchronous with TCK. Shall be grounded for end application

TAPTCK - Test Clock

TAP clock - Used to clock serial data into boundary scan latches and control sequence of the test state machine. TCK can be asynchronous with CLK

TAPTMS - Test Mode select

Tap Mode select - Resets the test state machine. Can be asynchronous with TCK. Shall be grounded for end application.

TAPTDI - Test data input

TAP data input - Serial input data to the boundary scan latches. Synchronous with TCK.

TAPTDO - Test data output

Tap data output - Serial output data from the boundary scan latches. Synchronous with TCK

1.8 Power Supply

VDA – 1.8V Power Supply

VDA is the power supply input for the AT7913E Core.

PVDDPLL – 1.8V PLL Power Supply

VDA is the power supply input for the AT7913E PLL.

VDB – 3.3V Power Supply

VDB is the power supply input for the AT7913E IOs.

VSA, VSB, PVSSPLL - Ground

2. Architecture

The AT7913E SpaceWire Remote Terminal Controller (RTC) is a bridge between the SpaceWire network and the CAN bus. The AT7913E is based on a LEON2-FT SPARC v8 processor core together with a wide range of interfaces including :

- Debug Support Unit
- LEON2-FT Peripherals
  - Interrupt Controller
  - 32-bit Timer
  - UART Serial Links
  - 16-bit General Purpose Input Output
  - Memory Interface
- On-Chip Memory
- FIFO Interface
- ADC/DAC Interface.
- 32-bit Timers
- 24-bit General Purpose Input Output
- CAN Interface
- SpaceWire Link Interface
- JTAG Interface

2.1 LEON2-FT processor

The SpaceWire-RTC ASIC includes the LEON2-FT Integer Unit (IU) and the MEIKO Floating Point Unit (FPU). The LEON2-FT IU implements the SPARC integer instruction set as defined in the SPARC Architecture Manual Version 8.

The LEON2-FT IU has the following features:

- 5-stage instruction pipeline
- Separate instruction and data cache interface
- Support for 8 register windows
- Multiplier 16x16
- Radix-2 divider (non-restoring)

To allow for software compatibility with existing devices such as the AT697E from Atmel, the AT7913E SpaceWire-RTC includes all standard LEON2-FT peripherals and the debug support unit.

The programming model of the SpaceWire-RTC device is thus compatible with the existing devices, only requiring support for the additional functions and interfaces to be added to the existing software development tools and operating systems.

The SpaceWire-RTC includes a LEON2-FT core with 4kbyte Instruction and Data caches. It also includes a MEIKO FPU (the same one as included in the Atmel AT697device).

2.2 Debug Support Unit

The AT7913E SpaceWire RTC includes a hardware debug support to aid software debugging on target hardware. The support is provided through two modules:

- a debug support unit (DSU)
- a debug communication link

2.2.1 Debug Support Unit

The DSU can put the processor in debug mode, allowing read/write access to all processor registers and cache memories. The DSU also contains a trace buffer which stores executed instructions and/or data transfers on the AMBA AHB bus.

The debug support unit is used to control the trace buffer and the processor debug mode. The DSU is attached to the AHB bus as slave, occupying a 2 Mbyte address space. Through this address space, any AHB master can access the processor registers and the contents of the trace buffer.

The DSU control registers can be accessed at any time, while the processor registers and caches can only be accessed when the processor has entered debug mode. The trace buffer can be accessed only when tracing is disabled/completed. In debug mode, the processor pipeline is held and the processor state can be accessed by the DSU.

2.2.2 Debug communication link

The SpaceWire-RTC device includes a debug support unit communication link that consists of a UART connected to the AHB bus as a master. The debug communications link implements a simple read/write protocol and uses standard asynchronous UART communications. The simple communication protocol is supported to transmit access parameters and data.

A link command consists of a control byte, followed by a 32-bit address, followed by optional write data.

2.3 LEON2-FT Peripherals

The AT7913E SpaceWire-RTC includes all the standard LEON2-FT peripherals.

2.3.1 Interrupt Controller

The Interrupt Controller is used to priorities and propagate interrupt requests from internal or external devices to the integer unit. 15 interrupts are handled, divided on two priority levels.

A Secondary Interrupt Controller is included to support the 32 additional interrupts used by the additional on-chip peripherals of the AT7913E device.

2.3.2 32-bit Timer

The timer unit implements two 32-bit timers, one 32-bit watchdog and one 10-bit shared prescaler. The functionality of the timers has not been modified with respect to existing implementations, to allow for software compatibility.

The watchdog functionality is used for overall software timeout handling and is the basis for error management.

2.3.3 UART Serial Links

Two identical UARTs are provided for serial communications. The UARTs support data frames with 8 data bits, one optional parity bit and one stop bit. To generate the bit-rate, each UART has a programmable 12-bits clock divider. Hardware flow-control is supported through handshake signals.

2.3.4 16-bit General Purpose Input Output

The 16-bit general purpose input output port can be individually programmed as output or input. Two registers are associated with the operation of the port; the combined input/output register, and direction register. When read, the input/output register will return the current value of the port; when written, the value will be driven on the port signals. The direction register defines the direction for each individual port.

2.3.5 Memory Interface

The SpaceWire-RTC memory interface is implemented using the LEON2-FT Memory Controller that supports the following:

- 8-bit PROM with sequential EDAC,
- 8-bit SRAM with sequential EDAC
- 32-bit PROM/SRAM with parallel-EDAC
- 8, 16, 32 bit I/O without-EDAC (wait-state and/or ready handshake)
- 16 bit GPIO (byte-wise) when less than 32 bit memory used

2.4 On-Chip Memory

The SpaceWire-RTC device includes a fault tolerant on-chip SRAM with embedded Error Detection And Correction (EDAC) and AMBA AHB slave interface.

One error is corrected and two errors are detected, which is done by using a (32, 7) BCH code. Some of the features available are single error counter, diagnostic reads and writes and auto-scrubbing (automatic correction of single errors during reads).

The on-chip memory comprises a 32-bit wide memory bank of 64 kbytes of data.

2.5 FIFO Interface

This FIFO memory can be accessed as an on-chip memory or as an external interface of the chip via the Memory Interface.

The FIFO interface supports transmission and reception of blocks of data by use of circular buffers located in memory external to the core. Separate transmit and receive buffers are assumed. Reception and transmission of data can be ongoing simultaneously.

2.6 ADC/DAC Interface

The SpaceWire-RTC includes a combined analogue-to-digital converter (ADC) and digital-to-analogue converter (DAC) interface.

The ADC/DAC interface provides a combined signal interface to parallel ADC and DAC devices. The two interfaces are merged both at the pin/pad level as well as at the interface towards the AMBA bus. The interface supports simultaneously one ADC device and one DAC device in parallel. Address and data signals unused by the ADC and the DAC can be use for general purpose input output, providing 0, 8, 16 or 24 channels.

The ADC interface supports 8 and 16 bit data widths. It provides chip select, read/convert and ready signals. The timing is programmable. It also provides an 8-bit address output. The ADC conversion can be initiated either via the AMBA interface or by internal or external triggers. An interrupt is generated when a conversion is completed.

The DAC interface supports 8 and 16 bit data widths. It provides a write strobe signal. The timing is programmable. It also provides an 8-bit address output.

2.7 32-bit Timers

The SpaceWire-RTC includes a General Purpose Timer Unit that implements one prescaler and two 32-bit decrementing timers.

2.8 24-bit General Purpose Input Output

The SpaceWire-RTC includes a 24-bit General Purpose Input Output core. The AMBA APB bus is used for control and status handling.

The core provides 24 channels. Each channel is individually programmed as input or output. Additionally, 8 of the channels are also programmable as pulse command outputs. The default reset configuration for each channel is as input. The default reset value each channel is logical zero.

The pulse command outputs have a common 20-bit counter for establishing the pulse command length. The pulse command length defines the logical one (active) part of the pulse. It is possible to select which of the channels shall generate a pulse command. The pulse command outputs are generated simultaneously in phase with each other, and with the same length (or duration). It is not possible to generate pulse commands out of phase with each other.

2.9 CAN Interface

The SpaceWire-RTC includes a CAN controller. The CAN protocol is based on the ESA HurriCANe CAN Controller VHDL core.

The controller uses the AMBA APB bus for configuration, control and status handling. The AMBA AHB bus is used for retrieving and storing CAN messages in memory external to the CAN controller. This memory can be located on-chip or external to the chip.

The CAN controller supports transmission and reception of sets of messages by use of circular buffers located in memory external to the core. Separate transmit and receive buffers are assumed. Reception and transmission of sets of messages can be ongoing simultaneously.

2.10 SpaceWire Link Interface

The SpaceWire (SPW2) Module is used for transmitting and receiving data over a SpaceWire link. It provides support for transmitting any type of protocol or data structure using SpaceWire packets.

It provides hardware support for receiving two types of SpaceWire Transfer Protocols, and can relay packets of other protocols to software. The SpaceWire Virtual Channel Transfer Protocol (VCTP) implements multiple virtual channels (only one implemented in SpaceWire-RTC) on a single SpaceWire link. The Remote Memory Access Protocol (RMAP) implements remote memory access to resources in the node via the SpaceWire link.

Data received over the link by the SpaceWire CODEC are temporarily stored in an RxFIFO. Data are then stored to memory by the SpaceWire Module via direct memoryaccess. Multiple Virtual Receive Channels (RxVC) can be used, each with its private memory area to which data are written. In SpaceWire-RTC one channel (RxVC(1)) is used for storing VCTP packets, and one channel (RxVC(0)) is used for storing RMAP responses, RMAP commands not supported by hardware and packets of other types of Transfer Protocols.

All RxVC share the same link. The SpaceWire Module implements hardware support for the RMAP. RMAP is used for remotely accessing resources on the local AMBA bus. The RMAP implementation can receive commands and generate responses, utilizing the aforementioned RxFIFO and the TxFIFO.

Data to be sent are read by the SpaceWire Module from memory via direct memory access. Data are then temporarily stored in a TxFIFO when forwarded to the SpaceWire CODEC for transmission over the link. Multiple Virtual Transmit Channels (TxVC) can be used, each with its private send list stored in memory from which data are read. In SpaceWire-RTC one channel (TxVC(0)) is used for automatic RMAP responses, and another channel (TxVC(1)) is used for transmissions set up by the user. All TxVC share the same link. RMAP responses have priority over transmissions set up by the user. The arbitration is performed for each packet sent.

2.11 JTAG Interface

The JTAG interface (compliant with IEEE-Std-1149.1) is used for the purpose of boundary scan testing during manufacture and test of printed circuit boards hosting the ASIC.

3. Typical Applications

The capabilities of the SpaceWire-RTC device are not limited to support the CAN bus in the instrument controller unit (ICU), but also allows it to be used in an on-board computer (OBC).

The AT7913E SpaceWire RTC is perfectly suited for application requiring cost optimizations as it can be used in both payload and avionics.

3.1 AT7913E in ICU

The SpaceWire-RTC device can be integrated in the instrument controller Unit (ICU) that acts as the payload data processor and mainly receives payload data from instruments and produces processed data to be down linked. The main data communication is performed via the SpaceWire network. The ICU is however controlled and monitored via the CAN network from the On-Board Computer (OBC).

3.2 AT7913E in OBC

The CAN controller in the SpaceWire-RTC device acts as a remote terminal that is being managed by the OBC. Alternatively, the SpaceWire-RTC device can be integrated in the On-Board Computer (OBC). Since the OBC acts as the network manager on the CAN network, the CAN controller carters capability such as node management and time distribution. The OBC also communicates or manages the SpaceWire network via SpaceWire links.

3.3 AT7913E on payload

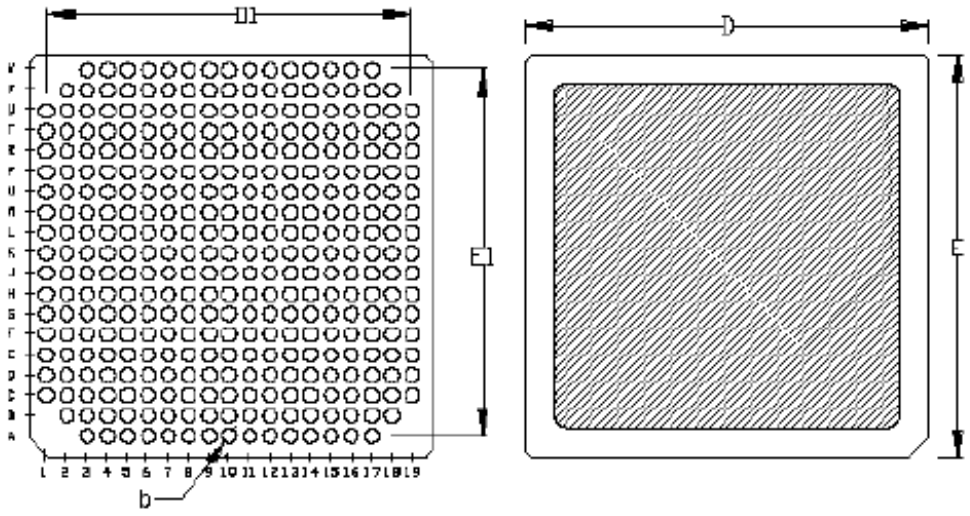
The main application of the SpaceWire-RTC device is however in instruments or individual experiments of the payload. It provides an abundance of interfaces, each with a high degree of programmability and configurability. It is able to acquire analogue and digital data, generated by connected peripherals and to generate discrete commands towards the same peripherals.

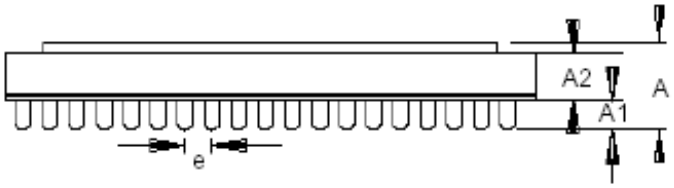
4. Package Information

4.1 Packages Outline

4.1.1 MCGA 349 outline

Figure 4-1. Mechanical description



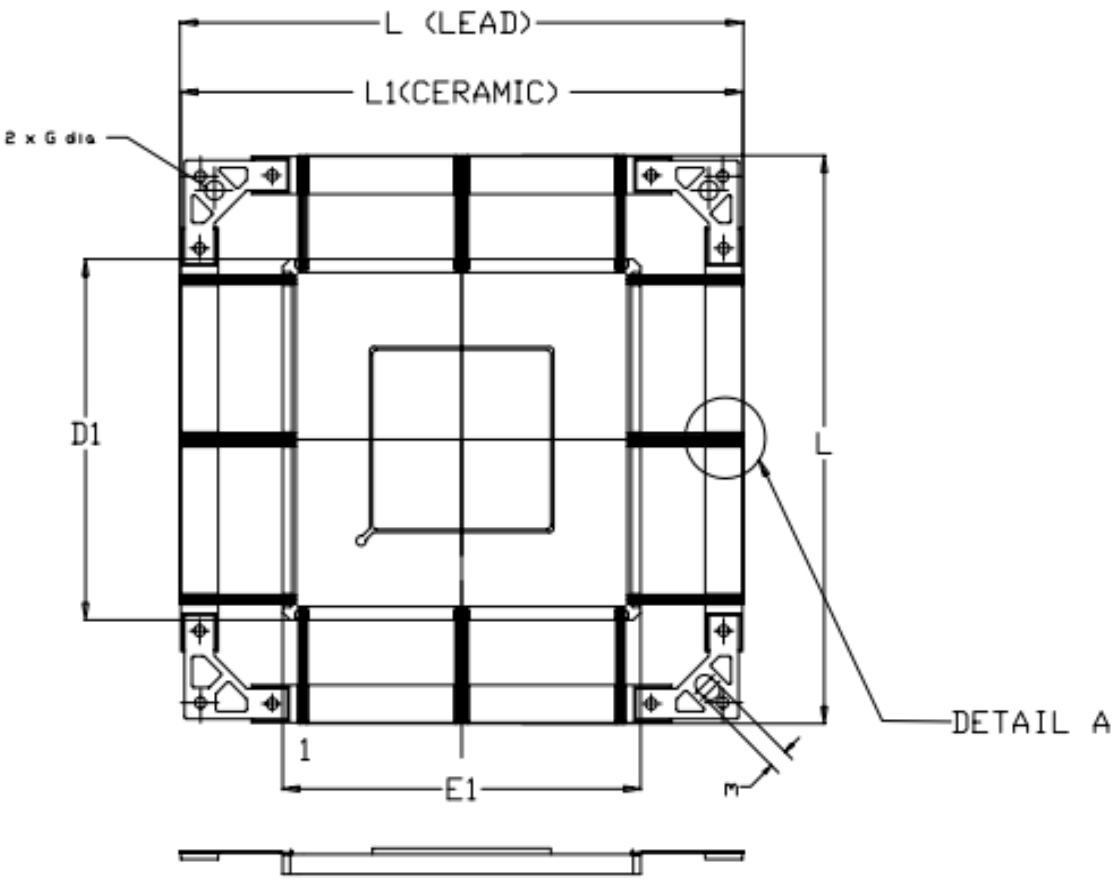


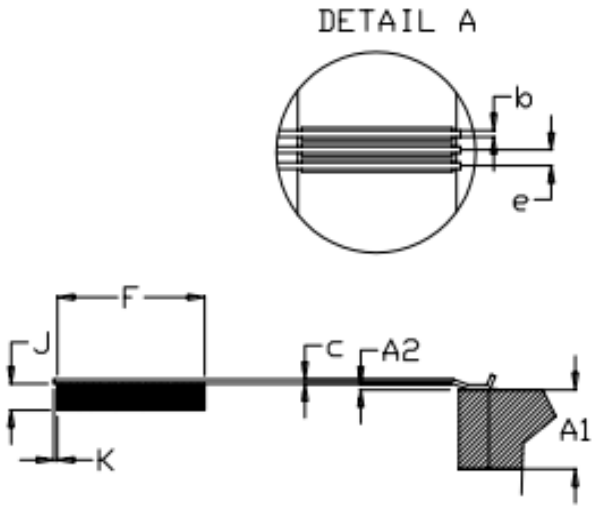
	mm		inch	
	min	max	min	max
D/E	24,8	25,2	0,976	0,992
D1/E1	22,86		0,9	
A1	1,4	1,85	0,055	0,073
A2	2,4	3,45	0,094	0,136
A	4,3	5,9	0,169	0,232
b	0,79	0,99	0,031	0,04
e	1,27		0,05	

Package lid is connected to ground

4.1.2 QFP 352 outline

Table 4-1. Mechanical description





	mm		inch	
	min	max	min	max
m	2.50	2.65	0.098	0.104
L3	65.85	65.95	2.592	2.596
L2	55.60	57.00	2.189	2.244
L1	74.60	75.40	2.947	3.008
L	74.85	76.40	2.947	3.008
K	----	0.50	-----	0.020
J	0.75	1.05	0.029	0.041
G	2.50	2.60	0.098	0.104
F	4.50	5.50	0.177	0.217
e	0.50	BASIC	0.019685	BASIC
D1-E1	47.52	48.48	1.871	1.908
c	0.11	0.20	0.004	0.008
b1	0.18	0.22	0.007	0.009
b	0.19	0.25	0.007	0.010
A2	0.05	0.35	0.002	0.014
A1	2.35	3.15	0.092	0.124
A	2.75	3.75	0.108	0.148

Package lid is connected to ground

4.2 Pin Assignment

4.2.1 Power and Ground

Table 4-2. Power and Ground pin assignement

Pin Name	Packages		Pin Name	Packages		Pin Name	Packages		Pin Name	Packages	
	QFP352	MCGA349		QFP352	MCGA349		QFP352	MCGA349		QFP352	MCGA349
VDA	8	V17	**VSA**	7	V18	**VDB**	16	G12	**VSB**	17	D12
VDA	82	V16	**VSA**	81	V4	**VDB**	24	F10	**VSB**	25	H10
VDA	96	C18	**VSA**	95	D1	**VDB**	31	W8	**VSB**	32	P8
VDA	170	C19	**VSA**	169	D19	**VDB**	41	W9	**VSB**	42	U8
VDA	184	U1	**VSA**	183	T1	**VDB**	63	U10	**VSB**	64	R10
VDA	272	U2	**VSA**	257	T19	**VDB**	91	V11	**VSB**	92	U11
VDA	346	U18	**VSA**	271	U3	**VDB**	118	M11	**VSB**	119	V12
VDA	258	U19	**VSA**	345	U17	**VDB**	127	W13	**VSB**	128	R14
VDA		V3	**VSA**		V2	**VDB**	134	T14	**VSB**	135	U15
VDA		W17	**VSA**		W16	**VDB**	141	N13	**VSB**	142	R18
VDA		W3	**VSA**		W4	**VDB**	150	P18	**VSB**	151	P14
VDA		B17	**VSA**		B18	**VDB**	157	M12	**VSB**	158	N18
VDA		A3	**VSA**		A4	**VDB**	165	A8	**VSB**	166	H9
VDA		A17	**VSA**		A16	**VDB**	175	M13	**VSB**	179	M16
VDA		B3	**VSA**		B2	**VDB**	200	K14	**VSB**	188	K12
VDA		B4	**VSA**		B16	**VDB**	215	J15	**VSB**	195	K18
VDA		C1	**VSA**		C3	**VDB**	223	J16	**VSB**	202	J14
VDA		C2	**VSA**		C17	**VDB**	231	G15	**VSB**	217	H16
						VDB	239	F17	**VSB**	224	G16
						VDB	249	F18	**VSB**	233	G14
PVDDPLL	279	A14				**VDB**	256	G7	**VSB**	240	B5
PVSSPLL	280	F14				**VDB**	267	D17	**VSB**	250	F13
						VDB	288	F1	**VSB**	259	H8
						VDB	303	J8	**VSB**	268	H3
						VDB	349	H6	**VSB**	290	D2
						VDB	187	K6	**VSB**	305	H7
						VDB	324	M2	**VSB**	325	J6
						VDB	194	V5	**VSB**	351	K8
									VSB		N5
									VSB		T3

4.2.2 System and Peripherals

Table 4-3. System and SpaceWire

Pin Name	Packages		Pin Name	Packages		Pin Name	Packages	
	QFP352	MCGA349		QFP352	MCGA349		QFP352	MCGA349
SysClk	83	R1	**SpwClk10Mbit_0**	306	A10	**SpwDIn_N_0**	300	C11
SysResetN	84	R4	**SpwClk10Mbit_1**	307	E11	**SpwDIn_N_1**	212	L17
TapTck	310	E10	**SpwClk10Mbit_2**	308	D10	**SpwDIn_P_0**	299	B11
TapTdi	313	G10	**SpwClkMult_0**	281	D13	**SpwDIn_P_1**	211	L18
TapTdo	312	B10	**SpwClkMult_1**	282	H12	**SpwDOut_N_0**	293	E13
TapTms	309	C10	**SpwClkMuxSel**	287	H11	**SpwDOut_N_1**	205	N15
TapTrstN	311	E9	**SpwClkPllCnfg_0**	284	C14	**SpwDOut_P_0**	291	B12
TestMode	19		**SpwClkPllCnfg_1**	285	A13	**SpwDOut_P_1**	203	M18
TestSE	40		**SpwClkPllCnfg_2**	286	E14	**SpwSIn_N_0**	302	C12
TimeClk	44	J5	**SpwClkSrc**	283	B13	**SpwSIn_N_1**	214	M17
TimeTrig_1	45	K4				**SpwSIn_P_0**	301	A11
TimeTrig_2	46	K3	**LvdsRef0**	298	D11	**SpwSIn_P_1**	213	L19
LeonDsuAct	117	R7	**LvdsRef1**	210	L16	**SpwSOut_N_0**	296	F12
LeonDsuBre	116	V8				**SpwSOut_N_1**	208	M14
LeonDsuEn	113	N8				**SpwSOut_P_0**	294	A12
LeonDsuRx	115	U7				**SpwSOut_P_1**	206	M19
LeonDsuTx	114	T8						
LeonErrorN	85	M7						
LeonWDN	87	N7						

Table 4-4. Memory Interface

Pin Name	Packages		Pin Name	Packages		Pin Name	Packages		Pin Name	Packages	
	QFP352	MCGA349		QFP352	MCGA349		QFP352	MCGA349		QFP352	MCGA349
MemA_0	120	P9	**MemD_0**	182	T17	**MemD_23**	236	H19	**RomCsN_0**	155	N11
MemA_1	121	R8	**MemD_1**	185	R19	**MemD_24**	237	J12	**RomCsN_1**	156	P12
MemA_2	124	N9	**MemD_2**	186	R16	**MemD_25**	238	H18	**MemCsN_0**	172	T15
MemA_3	125	V9	**MemD_3**	189	P16	**MemD_26**	241	G17	**MemCsN_1**	173	N12
MemA_4	126	U9	**MemD_4**	191	P19	**MemD_27**	242	J13	**MemCsN_2**	180	T16
MemA_5	129	P10	**MemD_5**	192	T18	**MemD_28**	243	H14	**MemCsN_3**	181	N14
MemA_6	130	M10	**MemD_6**	193	N16	**MemD_29**	247	F15	**MemOeN_0**	164	P13
MemA_7	131	W10	**MemD_7**	196	P17	**MemD_30**	248	G18	**MemOeN_1**	167	V14
MemA_8	132	R9	**MemD_8**	197	N19	**MemD_31**	251	J11	**MemOeN_2**	168	U16
MemA_9	133	T10	**MemD_9**	198	P15				**MemOeN_3**	171	W15
MemA_10	136	R11	**MemD_10**	199	L12	**MemCB_0**	252	F19	**MemWrN_0**	159	V13
MemA_11	137	V10	**MemD_11**	218	K19	**MemCB_1**	253	D18	**MemWrN_1**	160	U14
MemA_12	138	N10	**MemD_12**	219	L15	**MemCB_2**	254	F16	**MemWrN_2**	161	T13
MemA_13	139	W11	**MemD_13**	220	K16	**MemCB_3**	255	E17	**MemWrN_3**	162	L11
MemA_14	140	U12	**MemD_14**	221	K17	**MemCB_4**	260	E19	**MemBExcN**	276	D14
MemA_15	145	T11	**MemD_15**	222	K15	**MemCB_5**	261	E16	**IoBrdyN**	269	D16
MemA_16	146	P11	**MemD_16**	225	K13	**MemCB_6**	262	H13	**IoCsN**	275	C16
MemA_17	147	L10	**MemD_17**	226	J19	**MemCB_7**	263	G13	**IoOeN**	274	B14
MemA_18	148	R12	**MemD_18**	227	H17				**IoRead**	273	D15
MemA_19	149	W12	**MemD_19**	228	J18				**IoWrN**	270	A15
MemA_20	152	R13	**MemD_20**	230	J17						
MemA_21	153	T12	**MemD_21**	234	K11						
MemA_22	154	U13	**MemD_22**	235	H15						

Table 4-5. Other Peripherals

Pin Name	Packages		Pin Name	Packages		Pin Name	Packages		Pin Name	Packages	
	QFP352	MCGA349		QFP352	MCGA349		QFP352	MCGA349		QFP352	MCGA349
ADAddr_0	47	K5	**FifoD_0**	18	G4	**Gpio_0**	314	A9	**LeonPio_0**	93	P7
ADAddr_1	48	L5	**FifoD_1**	20	G2	**Gpio_1**	317	B9	**LeonPio_1**	94	T4
ADAddr_2	49	K2	**FifoD_10**	33	H5	**Gpio_2**	318	C9	**LeonPio_2**	97	W5
ADAddr_3	50	K7	**FifoD_11**	36	J7	**Gpio_3**	319	D9	**LeonPio_3**	98	T5
ADAddr_4	51	L1	**FifoD_12**	37	J2	**Gpio_4**	320	F9	**LeonPio_4**	99	V6
ADAddr_5	52	M3	**FifoD_13**	38	J3	**Gpio_5**	322	J10	**LeonPio_5**	100	U4
ADAddr_6	53	L2	**FifoD_14**	39	J1	**Gpio_6**	323	E8	**LeonPio_6**	101	T6
ADAddr_7	54	L3	**FifoD_15**	43	K1	**Gpio_7**	326	B8	**LeonPio_7**	104	W6
ADCs	79	P2	**FifoD_2**	21	F3	**Gpio_8**	327	E7	**LeonPio_8**	105	P6
ADData_0	59	K9	**FifoD_3**	22	G1	**Gpio_9**	328	D8	**LeonPio_9**	106	T7
ADData_1	60	M5	**FifoD_4**	23	F5	**Gpio_10**	329	C7	**LeonPio_10**	107	M8
ADData_10	71	N2	**FifoD_5**	26	H4	**Gpio_11**	330	G9	**LeonPio_11**	108	V7
ADData_11	72	P3	**FifoD_6**	27	G3	**Gpio_12**	331	F8	**LeonPio_12**	109	U6
ADData_12	73	N4	**FifoD_7**	28	H2	**Gpio_13**	332	A7	**LeonPio_13**	110	W7
ADData_13	74	L9	**FifoD_8**	29	G5	**Gpio_14**	333	E6	**LeonPio_14**	111	R6
ADData_14	76	T2	**FifoD_9**	30	H1	**Gpio_15**	334	B7	**LeonPio_15**	112	M9
ADData_15	77	P4	**FifoEmpN**	6	D3	**Gpio_16**	335	C6			
ADData_2	61	M1	**FifoFullN**	5	G6	**Gpio_17**	336	D7	**CanEn_0**	3	E2
ADData_3	62	L8	**FifoHalfN**	9	E1	**Gpio_18**	337	J9	**CanEn_1**	4	D4
ADData_4	65	M4	**FifoP_0**	12	F6	**Gpio_19**	338	A6	**CanRx_0**	347	D5
ADData_5	66	N3	**FifoP_1**	13	F4	**Gpio_20**	339	F7	**CanRx_1**	348	G8
ADData_6	67	L7	**FifoRdN**	11	F2	**Gpio_21**	340	D6	**CanTx_0**	343	C4
ADData_7	68	M6	**FifoWrN**	10	E4	**Gpio_22**	341	C5	**CanTx_1**	344	A5
ADData_8	69	N1				**Gpio_23**	342	B6			
ADData_9	70	P5									
ADRc	80	N6									
ADRdy	57	L4									
ADTrig	58	L6									
ADWr	78	R3									

4.2.3 Unconnected Pins

Table 4-6. Unconnected Pins

Pin Name	Packages		Pin Name	Packages		Pin Name	Packages		Pin Name	Packages	
	QFP352	MCGA349		QFP352	MCGA349		QFP352	MCGA349		QFP352	MCGA349
NC	1	B15	**NC**	102	K10	**NC**	209	W14	**NC**	292	
NC	2	C8	**NC**	103	L13	**NC**	216		**NC**	295	
NC	14	C13	**NC**	143	L14	**NC**	229		**NC**	297	
NC	15	C15	**NC**	144	M15	**NC**	232		**NC**	304	
NC	34	E3	**NC**	163	P1	**NC**	244		**NC**	315	
NC	35	E5	**NC**	174	N17	**NC**	245		**NC**	316	
NC	55	E12	**NC**	176	R2	**NC**	246		**NC**	321	
NC	56	E15	**NC**	177	R5	**NC**	264		**NC**	350	
NC	75	E18	**NC**	178	R15	**NC**	265		**NC**	352	
NC	86	F11	**NC**	190	R17	**NC**	266		**NC**	122	
NC	88	G11	**NC**	201	T9	**NC**	277		**NC**	123	
NC	89	G19	**NC**	204	U5	**NC**	278				
NC	90	J4	**NC**	207	V15	**NC**	289				

5. Electrical Characteristics

5.1 Absolute Maximum Ratings

Table: Absolute rating ltside

Supply Voltage I/Os (VDB buffers)……..... -0.3V to +4V

Supply Voltage Core (VDA array).....…….....-0.3V to +2V

Storage Temperature..... -65°C to +150°C

Input/ Output Voltages with respect to Ground..... ..... -0.3V to 4V

Power Dissipation 2W

ESD for I/O .....> 2000V

ESD for Pll ….....> 1000V

*Notice: Stresses at or above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification are not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability

5.2 Operating Range

Table 5-1. Operating Range

Operating Temperature	-55°C to +125°C
VDB – IO Power Supply	3.3V ± 0.3V
VDA - Core Power Supply	1.8V ± 0.15V

5.3 DC characteristics

Table 5-2. DC characteristics

Symbol	Parameter	Test Condition	Min	Typ	Max	Units
VCA	Operating Voltage		1.65	1.8	1.95	V
VCB			3	3.3	3.6	V
VIH	Input HIGH Voltage		2			V
VIL	Input LOW Voltage				0.8	V
IIL	Low Level Input current	Vin = GND	-1		1	µA
IILPD	Low Level Input Pull-down Current	Vin = GND	-5		5	µA
IILPU	Low Level Input Pull-up Current	Vin = GND	-110			µA
IIH	High Level Input Current	Vin = VCB (max)	-1		1	µA
IIHPU	High Level Input Pull-up Current	Vin = VCB (max)	-5		5	µA
IIHPD	High Level Input Pull-down Current	Vin = VCB (max)			600	µA
IOZL	Output Leakage low current	VOUT = GND	-1			µA
IOZH	Output Leakage high current	VOUT = VCB (max)			1	µA
VOH	Output HIGH Voltage	IOL = 2, 4, 8, 12, 16mA / VCC = VCB(min)	VCC-0.4			V
VOL	Output LOW Voltage	IOH = 2, 4, 8, 12, 16mA / VCC = VCB(min)			0.4	V
IOS	Output Short circuit current	VOUT = VCB			23	mA
Vod	Differential Output Delay		247		454	mV
Vos	Common mode output voltage		1125		1375	mV
ICCSBa	Supply current for array when not clocked	VCA(max)			3.5	mA
ICCOPa	Operating supply current for array	VCA(max)			52	mA

5.4 AC characteristics

The following table gives the worst case timings measured by Atmel on the 3.0V to 3.6V operating range

Table 5-3. 3.3V operating range timings

Parameter	Symbol	Min.	Max.	Unit
Propagation delay, SysClk rising to MemCsN falling	Tp0		18	ns
Propagation delay, SysClk rising to CanTx rising	Tp1		29	ns
Propagation delay, SysClk rising to Gpio rising	Tp2		25	ns
Propagation delay, SysClk rising to FifoD rising	Tp3		16	ns
Propagation delay, SpwClkSrc rising to SpwDout_P falling	Tp4		14	ns
Propagation delay, SpwClkSrc rising to SpwDout_N_0 rising	Tp5		14	ns

5.5 Timing Diagrams

Figure 5-1. Static Ram read cycle (0 waitsate)

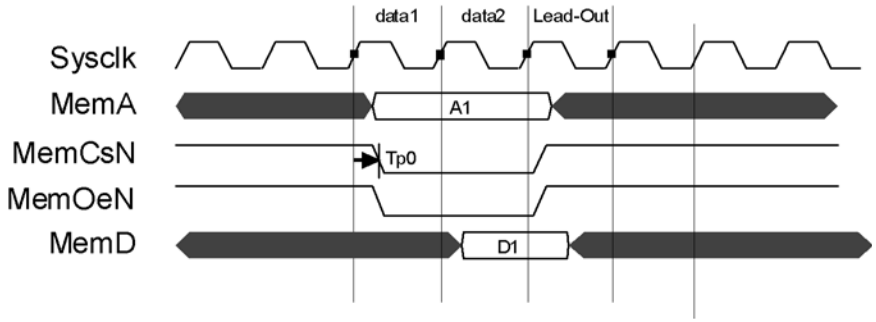


Figure 5-2. FifoD, GPIO and Can_Tx clock delay

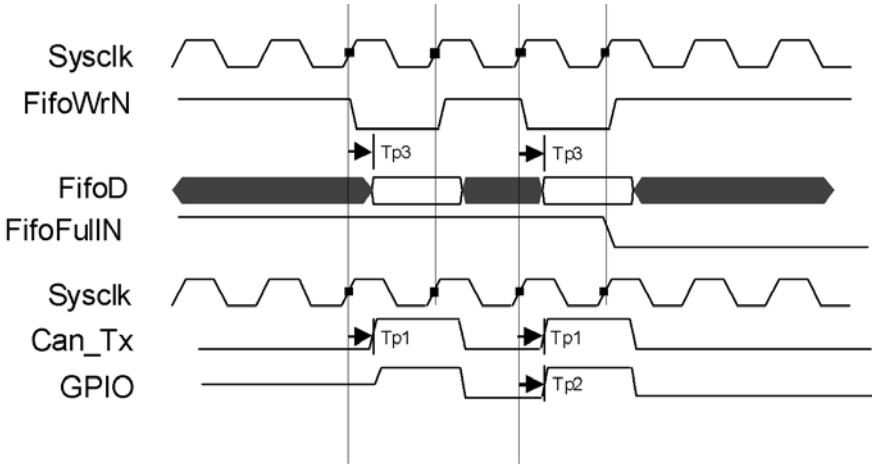
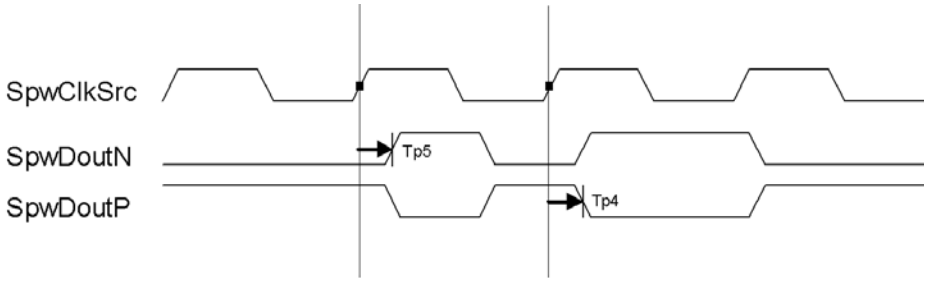


Figure 5-3. Clock to SpaceWire Data Out delay



6. Ordering Information

6.1 AT7913E Ordering Codes

Atmel Ordering Code	Package Type	Temperature Range	Quality Level
AT7913E-2H-E	MCGA349	25°C	Engineering sample
5962-10A0301QXB	MCGA349	-55°C to +125°C	QMLQ
5962-10A0301VXB	MCGA349	-55°C to +125°C	QMLV
5962R10A0301VXB	MCGA349	-55°C to +125°C	QMLV-RHA
AT7913E-2U-E	LGA349	25°C	Engineering sample
5962-10A0301QYC	LGA349	-55°C to +125°C	QMLQ
5962-10A0301VYC	LGA349	-55°C to +125°C	QMLV
5962R10A0301VYC	LGA349	-55°C to +125°C	QMLV-RHA
AT7913E-YC-E	CQFP352	25°C	Engineering sample
AT7913E-YC-MQ*	CQFP352	-55°C to +125°C	QMLQ
AT7913E-YC-SV*	CQFP352	-55°C to +125°C	QMLV

(1) Preliminary ordering code waiting for SMD reference

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