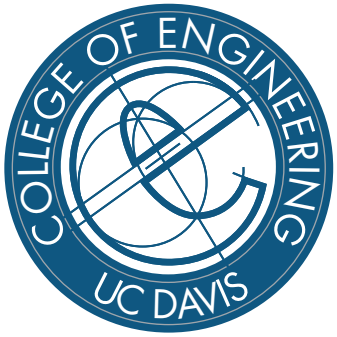

MSEE Thesis Measurement Board
Data Path FPGA ERS

Version: 1.01

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Table 1: Revision History

Revision	Date	Description	Initials
1.00	04/26/2009	First Draft	JWW
1.01	01/17/2009	Updated and re-organized ERS.	JWW

1 Overview

This document is intended to document the Data Path FPGA on the Measurement board.

The Measurement board uses an Xilinx Virtex-5 SX50T XC5VSX50T-3FFG1136 FPGA for controlling high-speed circuits. The FPGA is responsible for:

- High-Speed 16-bit DAC Interface
- High-Speed 12-bit ADC Interface
- Waveform Capture
- Waveform Playback
- RAM Pattern Storage and Retrieval
- Auxiliary Input Gating
- Waveform Inversion
- Waveform Scaling
- Waveform Triggering
- Data Path Registers

The purpose of the Measurement board is to demonstrate the DSP capabilities of the Asynchronous array of Simple Processors Version 2 (AsAPv2). The AsAPv2 is a 167-processor 65 nm computational platform well suited for DSP, communication, and multimedia workloads. It is made up of a homogeneous array of 164 programmable processors and 3 processors dedicated for signal processing:

1. Fast Fourier Transform (FFT)
2. Communication (Viterbi Decoder)
3. Multimedia (Video Motion Estimation)

The Measurement board contains an array of 2 AsAPv2 chips and supports several different operation modes:

1. Baseband Spectrum Analyzer
2. Oscilloscope
3. Arbitrary Waveform Generator
4. Signal Source
5. Network Analyzer

The operation mode can be changed on-the-fly, even when a signal is being measured.

2 Reference Documents

2.1 Schematics

The Measurement board schematics are located at the following url:

http://www.ece.ucdavis.edu/vcl/vclpeople/jwwebb/measbd/docs/sch_p342_blk.pdf

2.2 Datasheets and User Guides

2.2.1 Xilinx Virtex-5 SX50T

Manufacturer: Xilinx, Inc.
Manufactuers Part Number: XC5VSX50T-3FFG1136C

1. **Data Sheet**
   http://www.xilinx.com/support/documentation/data_sheets/ds100.pdf
2. **DC and Switching**
   http://www.xilinx.com/support/documentation/data_sheets/ds202.pdf
3. **User Guide**
   http://www.xilinx.com/support/documentation/user_guides/ug190.pdf
4. **Packaging and Pinout**
   http://www.xilinx.com/support/documentation/user_guides/ug195.pdf
5. **Configuration Guide**
   http://www.xilinx.com/support/documentation/user_guides/ug191.pdf
6. **PCB Designer's Guide**
   http://www.xilinx.com/support/documentation/user_guides/ug203.pdf
7. **System Monitor Guide**
   http://www.xilinx.com/support/documentation/user_guides/ug192.pdf

2.2.2 Xilinx Spartan-3A

Manufacturer: Xilinx, Inc.
Manufactuers Part Number: XC3S1400A-4FGG484C

1. **Data Sheet**
   http://www.xilinx.com/support/documentation/data_sheets/ds529.pdf
2. **User Guide**
   http://www.xilinx.com/support/documentation/user_guides/ug331.pdf
3. **Configuration Guide**
   http://www.xilinx.com/support/documentation/user_guides/ug332.pdf

2.2.3 Micron DDR2 SDRAM SODIMM

1. **MT16HTF25664HY-667E1 Data Sheet**
   http://download.micron.com/pdf/datasheets/modules/ddr2/HTF16C128_256x64H.pdf

2.2.4 Samsung QDR-II SRAM

1. **K7R323684C-EC250 Data Sheet**
   http://www.samsung.com/global/system/business/semiconductor/product/2007/7/30/948789ds_k7r32xx84c_rev11.pdf

2.2.5 Texas Instruments High-Speed 12-bit 500MS/s A/D Converter (ADC)

1. **ADS5463IPFP Data Sheet**
   http://focus.ti.com/lit/ds/symlink/ads5463.pdf

2.2.6 Texas Instruments High-Speed 16-bit 1GS/s D/A Converter (DAC)

1. **DAC5682ZIRGCT Data Sheet**
   http://focus.ti.com/lit/ds/symlink/dac5682z.pdf

2.2.7 Texas Instruments High-Speed Op-Amps

1. **THS4302RGT Data Sheet**
   http://focus.ti.com/lit/ds/symlink/ths4302.pdf
2. **THS4509RGTT Data Sheet**
   http://focus.ti.com/lit/ds/symlink/ths4509.pdf
3. **OPA695IDBV Data Sheet**
   http://focus.ti.com/lit/ds/symlink/opa695.pdf

2.2.8 Texas Instruments Power Supply Regulators and Sequencers

1. **PTH08T220WAZ Data Sheet**
   http://focus.ti.com/lit/ds/symlink/pth08t220w.pdf
2. **PTH08T260WAZ Data Sheet**
   http://focus.ti.com/lit/ds/symlink/pth08t260w.pdf
3. **PTH12050YAZ Data Sheet**
   http://focus.ti.com/lit/ds/symlink/pth12050y.pdf
4. **TPS79601 Data Sheet**
   http://focus.ti.com/lit/ds/symlink/tps79601.pdf
5. **TPS74201 Data Sheet**
   http://focus.ti.com/lit/ds/symlink/tps74201.pdf
6. **TPS73701 Data Sheet**
   http://focus.ti.com/lit/ds/symlink/tps73701.pdf
7. **LP2951D Data Sheet**
   http://focus.ti.com/lit/ds/symlink/lp2951.pdf
8. **TPS72301 Data Sheet**
   http://focus.ti.com/lit/ds/symlink/tps72301.pdf
9. **TL7733BCD Data Sheet**
   http://focus.ti.com/lit/ds/symlink/tl7733b.pdf
10. **TPS3808G25 Data Sheet**
    http://focus.ti.com/lit/ds/symlink/tps3808g25.pdf

2.2.9 Texas Instruments Temperature Sensors and Fan Controllers

1. **AMC6821 Data Sheet**
   http://focus.ti.com/lit/ds/symlink/amc6821.pdf
2. **TMP125 Data Sheet**
   http://focus.ti.com/lit/ds/symlink/tmp125.pdf

2.2.10 Analog Devices Clock PLL IC

1. **AD9516-3BCPZ Data Sheet**
   http://www.analog.com/UploadedFiles/Data_Sheets/AD9516_3.pdf

3 Data Path FPGA Block Diagram

3.1 Xilinx Virtex-5 SX50T XC5VSX50T-3FF1136

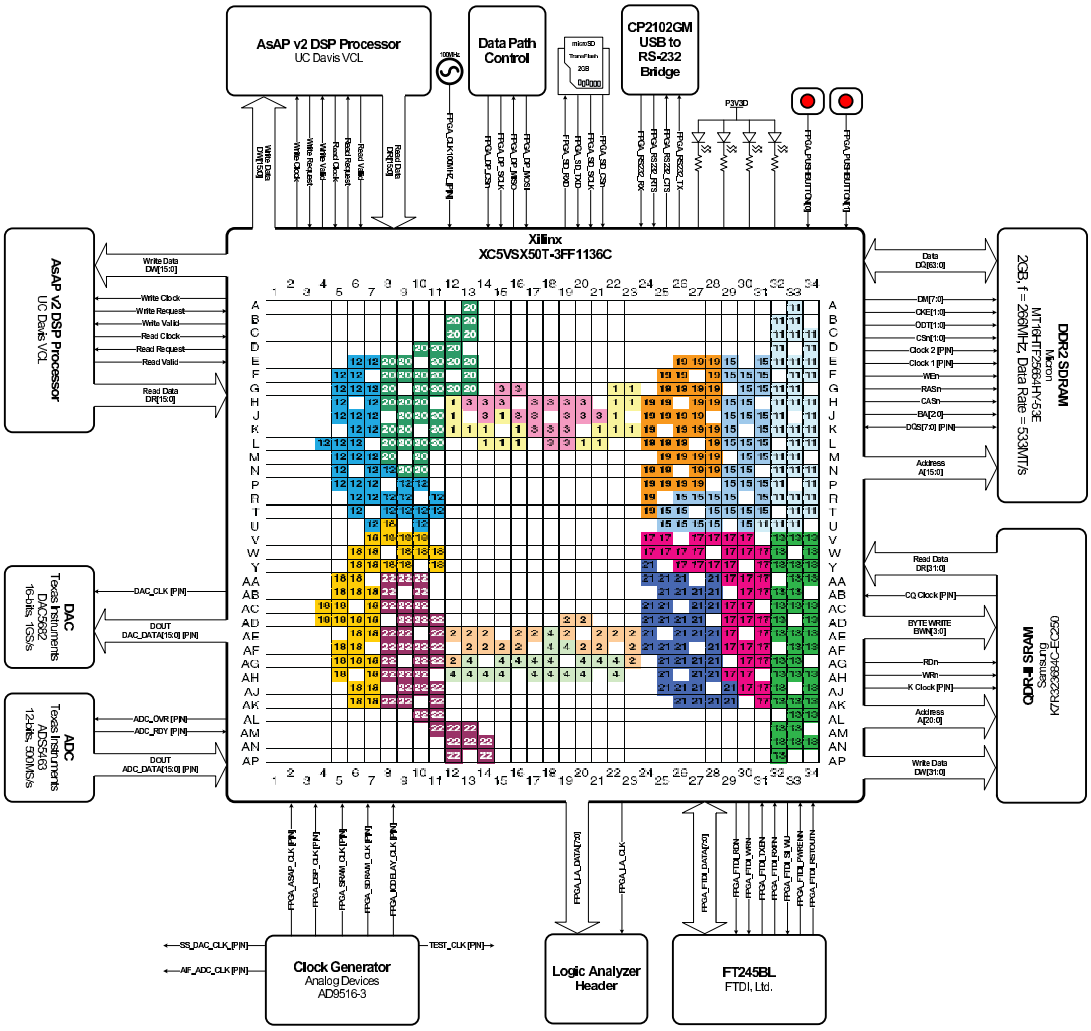


Figure 3.1: Data Path FPGA Block Diagram

4 Measurement Description

4.1 QDR-II SRAM Controller

The QDR-II SRAM Controller is responsible for RAM/User Waveform storage and retrieval from the Samsung 36Mb burst-of-4 QDR-II SRAM (PN: K7R323684C-EC250). The QDR-II SRAM is organized as 1M-word x 36-bits. The QDR-II SRAM Controller is made up of 3 major blocks:

- Xilinx QDR-II SRAM Controller (Section 4.1.1)
- QDR-II SRAM Read Controller (Section 4.1.2)
- QDR-II SRAM Write Controller (Section 4.1.3)

The waveform data is transferred to the Data Path FPGA and written to the QDR-II SRAM in 128-bit packets at a rate of 250MHz. The waveform data is not written in a continuous stream, as the interface between the Control and Data Path FPGAs is a 25MHz SPI link. The Control FPGA must wait for write acknowledgement after each 128-bit packet is sent to the Data Path FPGA, which indicates that a new SRAM write transaction may be initiated. The waveform data is read out of the QDR-II SRAM in burst of 4 (or 144-bits) at 250MHz; however, the manner in which the QDR-II SRAM Read Controller retrieves data the read bandwidth is limited to 125MHz. The bus width of the Data Path FPGA is 128-bits, therefore we only need to use 128-bits of the 144-bit read data. The 4 MSB bits of each 36-bit packet are discarded. The waveform read data is written into a 136-bit wide FIFO along with an 8-bit trigger word. Data is read out of the FIFO using the 125MHz clock, and divided up into 8 16-bit sample points. The 128-bit data is divided up as follows:

- sram7[15:0] = sram_rdata[127:112]
- sram6[15:0] = sram_rdata[111:96]
- sram5[15:0] = sram_rdata[95:80]
- sram4[15:0] = sram_rdata[79:64]
- sram3[15:0] = sram_rdata[63:48]
- sram2[15:0] = sram_rdata[47:32]
- sram1[15:0] = sram_rdata[31:16]
- sram0[15:0] = sram_rdata[15:0]

A top-level block diagram of the QDR-II SRAM Controller is shown in Figure 4.1.

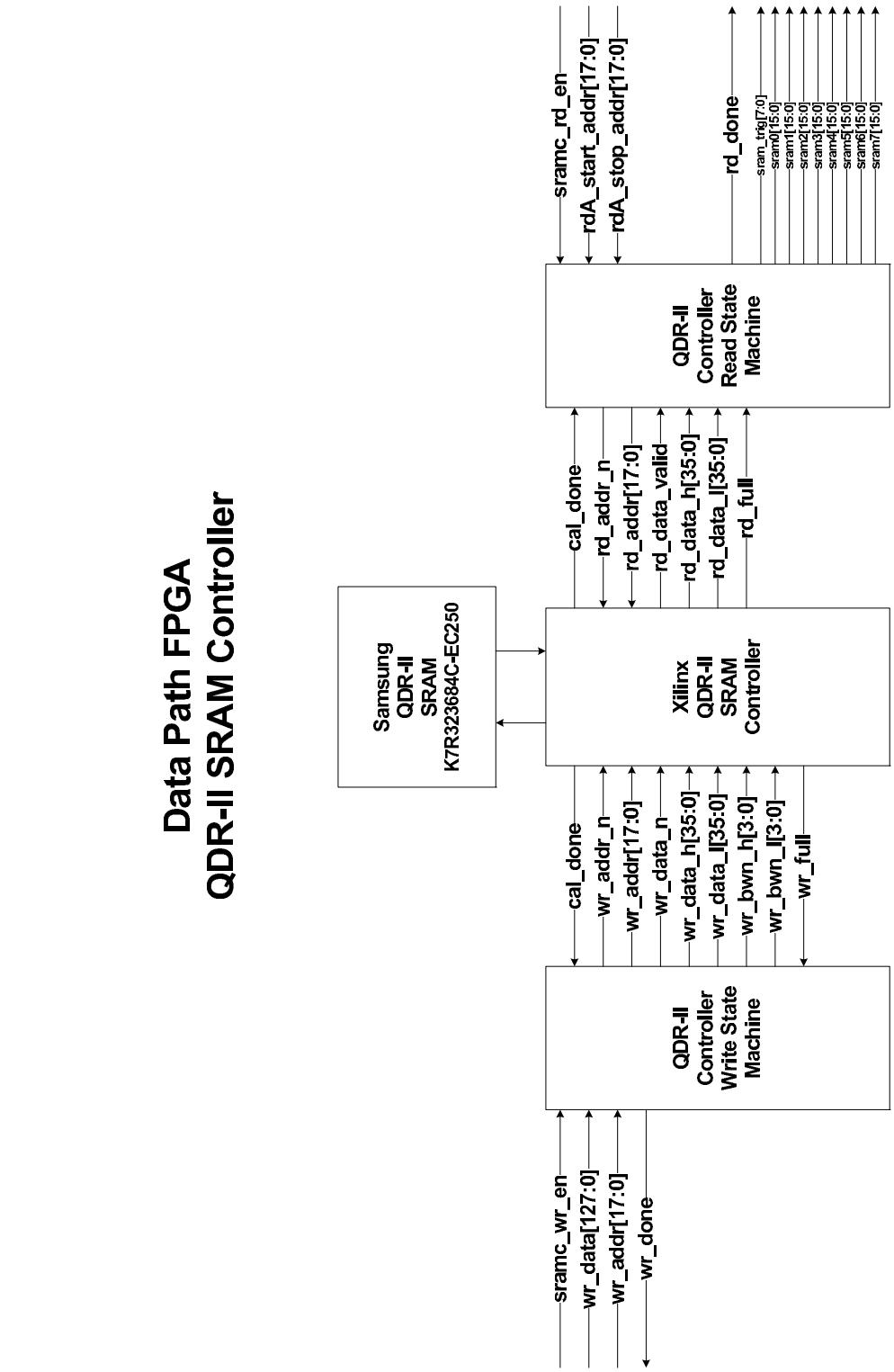


Figure 4.1: QDR-II SRAM Controller Top-Level Block Diagram

4.1.1 Xilinx QDR-II SRAM Controller

The QDR-II SRAM interface is controlled by a Xilinx QDR-II SRAM Controller, which was generated by the Xilinx Memory Interface Generator (MIG) tool. [1] The QDR-II SRAM controller design supports the following:

- A maximum frequency of 300 MHz
- 18-bit, 36-bit, and 72-bit data widths
- Burst lengths of four and two
- Implementation using different Virtex-5 devices
- Support for DCI Cascading
- Operation with 18-bit and 36-bit memory components
- Verilog and VHDL
- With and without a testbench
- With and without a DCM

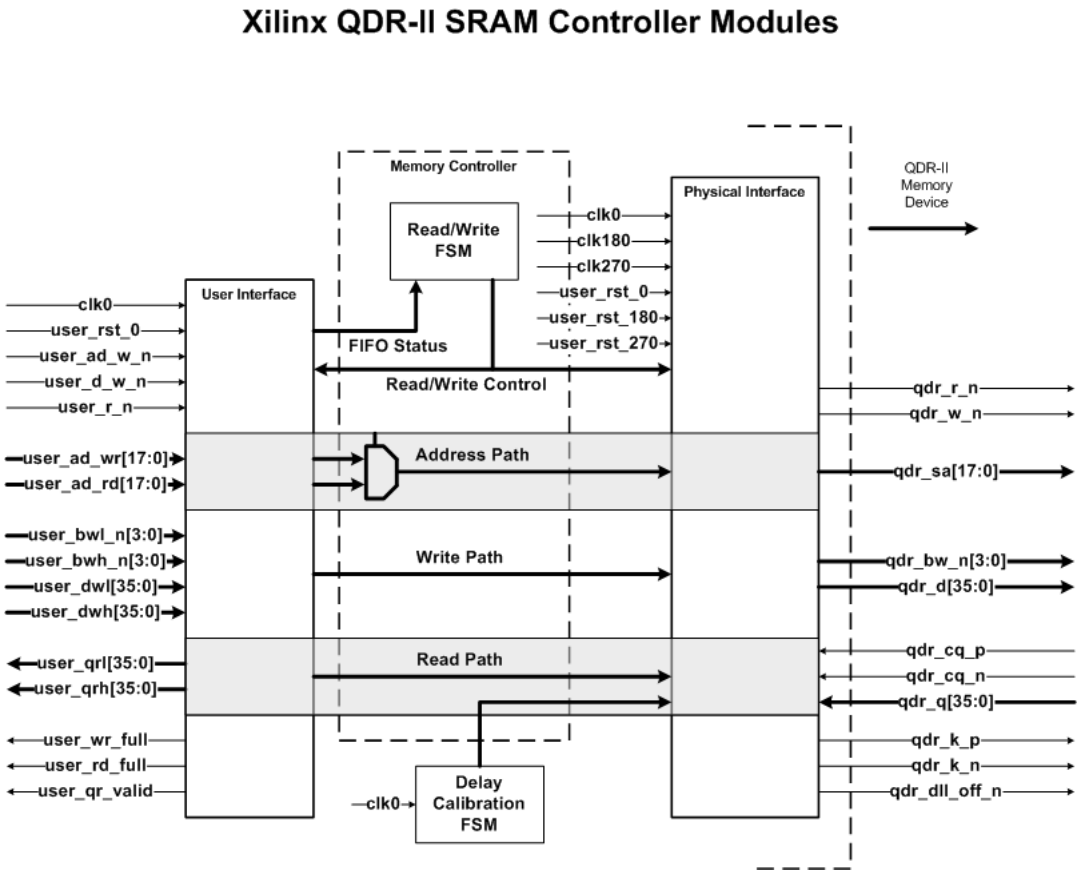


Figure 4.2: Xilinx QDR-II SRAM Controller Block Diagram

4.1.1.1 QDR-II SRAM Initialization and Calibration

QDR-II SRAM memory is initialized through a specified sequence. Following initialization, the relationship between the data and the FPGA clock is calculated using the TAP logic. The calibration logic is explained briefly as follows. [1]

Calibration is done in three stages:

1. The read strobe CQ is edge-aligned with the read data Q from the memory. The read strobe is a free-running clock from the memory. In the first stage of calibration, the read strobe CQ is passed through the BUFIO, which delays the strobe by the amount of delay in the BUFIO. Now the read strobe CQ is out of synchronization with the read data Q.

   A pattern of four bursts of data (with a value of '1' for rise data and '0' for fall data) is written into a particular location in memory. Continuous read commands are issued to the same location of the memory and the read data Q is delayed in the ISERDES, until it is center-aligned with respect to the delayed read strobe CQ.

   The q_init_delay_done signal in the phy_read module indicates the status of the first stage calibration. When q_init_delay_done is asserted High, it indicates the completion of first-stage calibration. Now the CQ clocks are centered with respect to the Read Data Q at the input of the ISERDES.

2. In the second stage of calibration, the read data window is center-aligned with respect to the FPGA clock. Here another pattern of four bursts of data is written into a particular memory location. It is read back continuously from the same memory location, and the read data and the delay clock, CQ, are delayed until the registered read data is center-aligned with the FPGA clock.

   When the registered read data is center-aligned with the FPGA clock, the alignment of the read data Q with respect to the FPGA clock is complete. The dly_cal_done signal in the phy_read module indicates the status of second-stage calibration.

3. In the third stage of calibration, the controller issues non-consecutive read commands to the memory. The internal read command signal generated by the controller is then delayed through a shift register until the delayed read command signal is aligned with the ISERDES read data output. Then another level of calibration is done to ensure alignment between the ISERDES data outputs from all the banks used in the interface. This finishes the calibration of the read data Q, and the cal_done signal is asserted High.

More information can be found on the Xilinx Virtex-5 QDR-II SRAM Controller in the Xilinx MIG User Guide. [1]

4.1.2 QDR-II SRAM Read Controller

The SRAM Read Controller is responsible for the the read interface to the QDR-II SRAM in the Data Path FPGA. The Data Path Board uses a 36-Mb QDR-II SRAM from Samsung (PN: K7R323684C-EC250).

The Control FPGA will write to the following registers:

- sramc_rdA_start_addr[17:0]
- sramc_rdA_stop_addr[17:0]

When the Control FPGA has finished writing to the SRAM Read Address registers, it will write to the SRAM Control register:

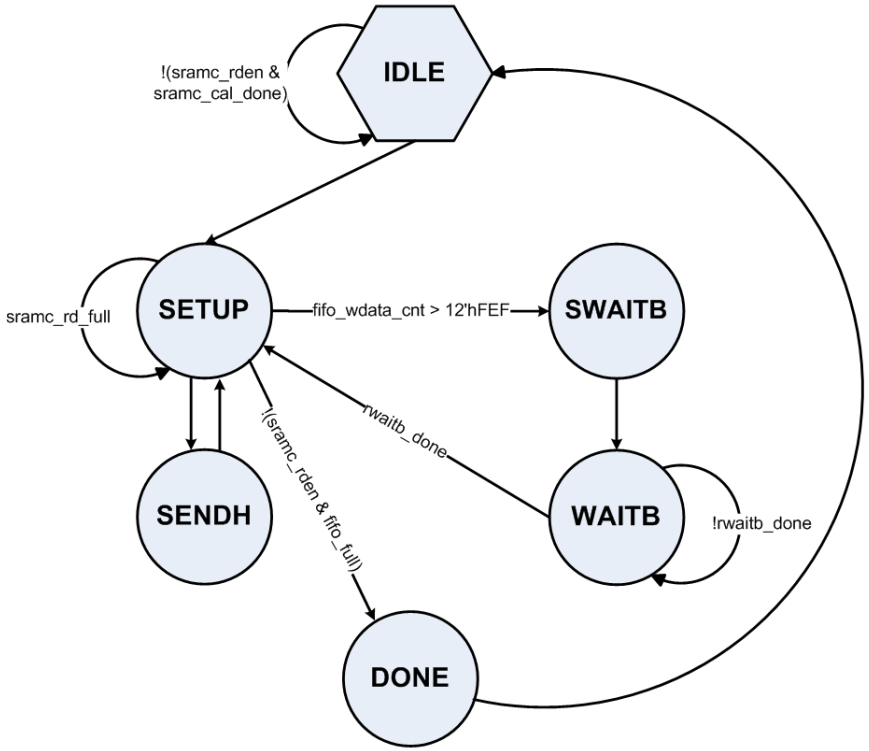
- sramc_rden

The SRAM Read Control register is 1-bit wide, and is active high. When it is set high, the Read SRAM FSM will transition to the SETUP_RD state to clear the done bit and increment the shadow read address counter. The SETUP_RD state is also responsible for keeping track of the read Data Path FIFO data count. If the write FIFO data count is greater than 12'hFEF, then the FSM transitions to the SWAITB_RD to decrement the shadow read address count value. It then transitions to the WAITB_RD state to wait for the write FIFO data count to be less than 12'h100. As soon as the WAITB_RD constraints have been satisified, the FSM will transition back to the SETUP_RD state to continue reading SRAM data from the SRAM Controller. The SWAITB_RD and WAITB_RD states allow for the read Data Path FIFO to avoid the overflow or underflow conditions. Under normal circumstances, the FSM will transition from the SETUP_RD state to the SENDH_RD state to set the 18-bit read address to the shadow address count and the rd_addr_n bit low. The SENDH_RD state will then transition back to the SETUP_RD state. This cycle will continue for as long as the sramc_rden enable is set high.

The trick is to read at a rate that is not too fast that the FIFO fills up, but not to slow that the FIFO empties out. The problem is that the ADC is sampling at 500MHz, so we'll need to decimate-by-4 to achieve a new sample rate of 125MHz. This will allow us to read raw sample data at the maximum QDR-II SRAM rate of 125MHz. The QDR-II SRAM Read rate is actually half of the 250MHz rate, or 125MHz, because of the Xilinx SRAM controller.

It is appealing to stick with the Xilinx SRAM controller, because they take care of auto-calibration of the read data inputs and provide a simple interface for writing/reading data.

SRAM Read State Machine



The sram_read.sv FSM is responsible for reading the 128-bit SRAM Read Data from the Xilinx QDR-II SRAM Controller. The MicroBlaze will wait until the Xilinx QDR-II SRAM Controller's Calibration Done signal goes high. Once this condition is met it will set the sramc_rden enable bit. The Xilinx QDR-II SRAM Controller interfaces with a Samsung K7R323684C-EC250, which is a burst of 4 SRAM.

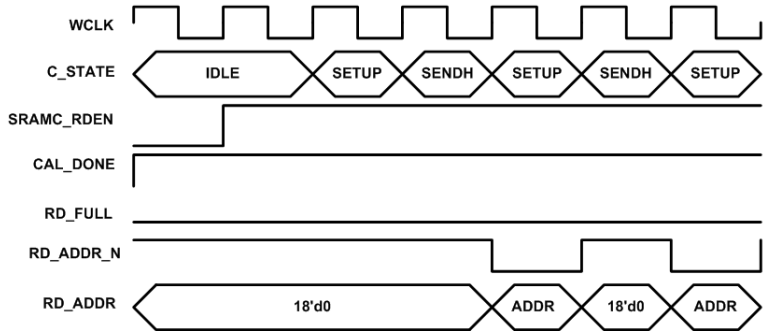


Figure 4.3: QDR-II SRAM Controller Read FSM Block Diagram

4.1.3 QDR-II SRAM Write Controller

The SRAM Read Controller is responsible for the write interface to the QDR-II SRAM in the Data Path FPGA. The Data Path Board uses a 36-Mb QDR-II SRAM from Samsung (PN: K7R323684C-EC250).

The Control FPGA will write to the following registers:

- sramc_wr_data[127:0]
- sramc_wr_addr[17:0]

When the Control FPGA has finished writing to the SRAM Write Data and Write Address registers, it will write to the SRAM Control register:

- sramc_wren

The SRAM Write Control register is 1-bit wide, and is active high. When it is toggled high (i.e., 0->1->0 transition), the Write SRAM FSM will transition to the SETUP state to clear the done bit. It will then transition to the SENDH state to send the top-half of the 128-bit SRAM Controller Write Data, the 18-bit SRAM Controller Write Address, and set the addr_n, data_n, bwn_h, and bwn_l bits low. The next clock cylce the FSM will transition to the SENDL state to send the lower-half of the 128-bit SRAM Controller Write Data, and set the addr_n, data_n, bwn_h, and bwn_l bits high. The FSM will then transition to the DONE state and clear the 128-bit data and 18-bit address registers, and jump to the IDLE state to wait for the Control FPGA to initiate another SRAM write.

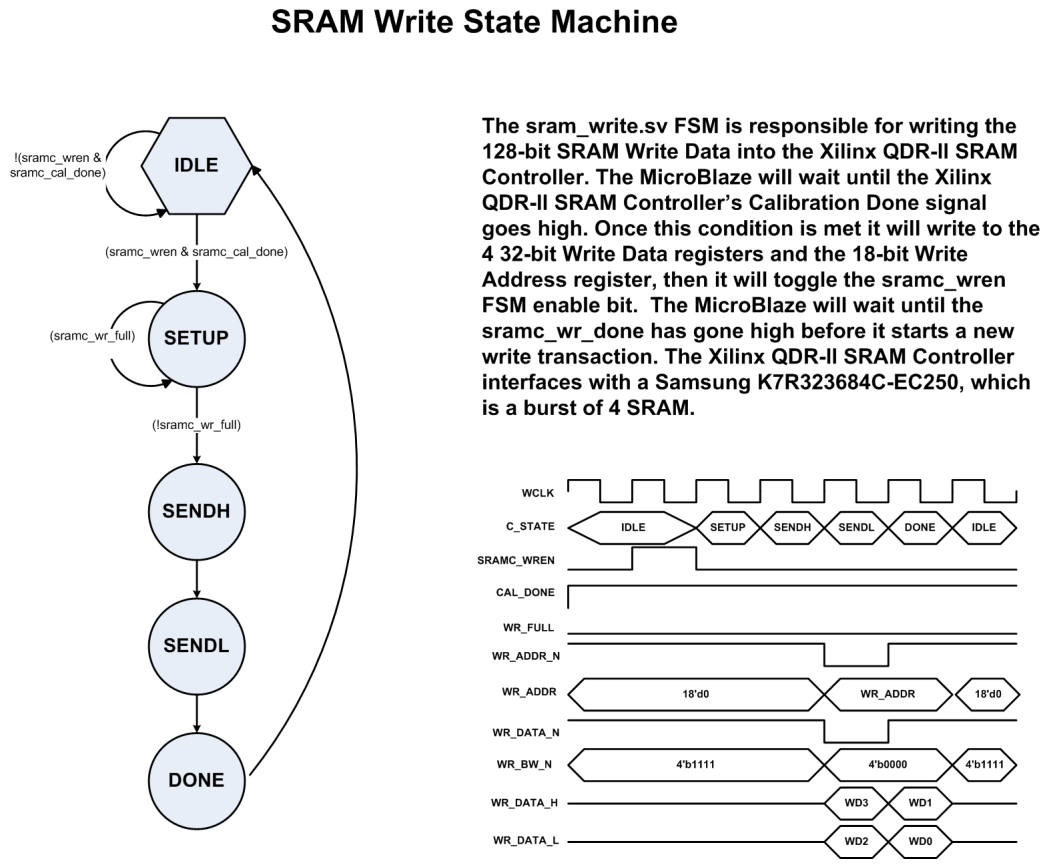


Figure 4.4: QDR-II SRAM Controller Write FSM Block Diagram

4.2 Trigger

The Programmable Waveform Generator has two methods for generating a trigger:

1. Waveform Trigger
2. Divided Clock Trigger

4.2.1 Divided Clock Trigger

The desired divided clock trigger rate can be set to one of the following rates:

- clk: 500MHz
- $\frac{clk}{2}$: 250MHz
- $\frac{clk}{4}$: 125MHz
- $\frac{clk}{8}$: 62.5MHz

The default divided clock rate is $\frac{clk}{64}$. The following fixed binary patterns are used to generate the divided clock rates:

- clk: 8'b10_10_10_10
- $\frac{clk}{2}$: 8'b11_00_11_00
- $\frac{clk}{4}$: 8'b11_11_00_00
- $\frac{clk}{8}$: 8'b11_11_11_11 for 1 $\frac{clk}{4}$, 8'b00_00_00_00 for 1 clk $\frac{clk}{4}$, and repeat.

These fixed binary patterns drive an 8-to-1 OSERDES in DDR Mode. The OSERDES is clocked using a 500MHz to drive the serial output and a clock of 125MHz to drive the slow speed input.

The waveforms in Figure 4.5 show each divided clock rate relative to eachother.

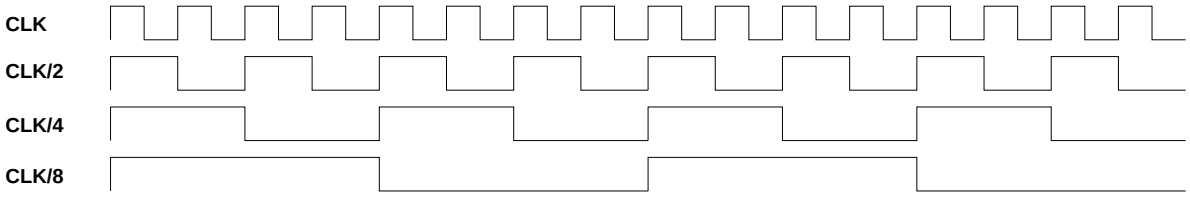


Figure 4.5: Divided Clocks, 0° Phase

The 180 degree versions of the divided clocks are shown in Figure 4.6.

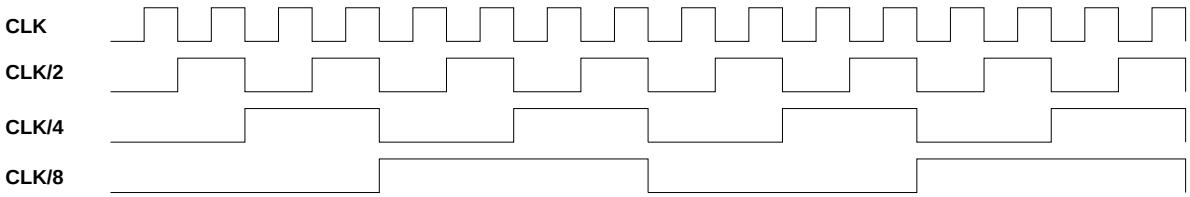


Figure 4.6: Divided Clocks, 180° Phase

4.2.2 Waveform Trigger

The trigger output is set high for 8 high-speed clock cycles when the RAM waveform SRAM address reaches zero. The user will define the trigger sample point in 2's complement.

5 Data Path FPGA Control Description

This chapter describes the sequence of commands and calculations necessary to control the Data Path FPGA. The Data Path FPGA will be controlled by the MicroBlaze Application running on the Control FPGA.

5.1 Reset Routines

5.1.1 Clock and Delay Reset Routine

First reset both the SRAM PLL and the System DCM by writing to the following registers:

1. Write Command: "w 2 DD"
2. Write Command: "w 2 9c"

Now that the reset register bits have been toggled, check the locked status by reading the following register:

1. Read Command: "r a"
2. If the SRAM PLL and System DCM interrupts are enabled a service request should be generated when the DCM and PLL become locked.

Verify that bits 2 and 6 are set high. Once the locked status has been verified, reset teh IDELAY_CTRL blocks used to insert I/O Delay by writing to the following registers:

1. Write Command: "w 10a FF"
2. Write Command: "w 10a 00"

Now that the IDELAY_CTRL blocks have been reset, check the ready bits of each block by reading the following register:

1. Read Command: "r 112"

Verify that bits 3 to 0 are set high. Once the ready status has been verified, reset the external High-Speed Clock Dividers by writing to the followign registers:

1. Write Command: "w 104 0"
2. Write Command: "w 104 3"

Now the Clock and Delay Reset routine has completed.

5.1.2 Xilinx SRAM Controller Reset Routine

Reset the Xilinx SRAM Controller by writing to the following registers:

1. Write Command: "w 2 9e"
2. Write Command: "w 2 9c"

Now the Xilinx SRAM Controller Reset routine has completed.

5.1.3 VCL SRAM Controller Reset Routine

Reset the VCL SRAM Controller by writing to the following registers:

1. Write Command: "w 2 98"
2. Write Command: "w 2 9c"

Now the VCL SRAM Controller Reset routine has completed.

5.1.4 Block RAM Controller Reset Routine

Reset the Block RAM Controller by writing to the following registers:

1. Write Command: "w 2 1c"
2. Write Command: "w 2 9c"

Now the Block RAM Controller Reset routine has completed.

5.2 Initialization

The Control FPGA located on the Data Path Board will need to perform the following initialization of the Data Path FPGA in the order shown:

1. Configure the Data Path FPGA.
2. Execute the Clock and Delay Reset Routine described in Section 5.1.1.
3. Execute the Xilinx SRAM Controller Reset Routine described in Section 5.1.2.
4. Execute the VCL SRAM Controller Reset Routine described in Section 5.1.3.
5. Execute the Block RAM Controller Reset Routine described in Section 5.1.4.
6. Start Pattern
   (a) If the Waveform Mode is set to Block RAM, then transfer the selected pattern from the microSD card to the Block RAM, set the Read Address(s), enable RAM Waveform Mode, enable Block RAM Waveforms and start Block RAM Waveform Playback.
      i. Write Command: "w 380 01FF"
      ii. Write Command: "w 38c 0"
      iii. Write Command: "w 382 [WriteAddress]"
      iv. Write Command: "w 384 [WriteData0]"
      v. Write Command: "w 386 [WriteData1]"
      vi. Write Command: "w 388 [WriteData2]"
      vii. Write Command: "w 38A [WriteData3]"
      viii. Continue writing 128-bit packets until the end of file is reached.
      ix. Write Command: "w 380 0"
      x. Write Command: "w 38E [ReadStartAddress_A]"
      xi. Write Command: "w 390 [ReadStopAddress_A]"
      xii. Write Command: "w 100 60"
      xiii. Write Command: "w 100 20"
      xiv. Write Command: "w 400 1"
      xv. Write Command: "w 40E 1"
      xvi. Write Command: "w 38C 1"
   (b) If the Pattern Mode is set to QDR-II SRAM, then transfer the selected pattern from the microSD card to the QDR-II SRAM, set the Read Address(s), enable RAM Waveform Mode, enable QDR-II SRAM Waveforms and start QDR-II RAM Waveforms Playback.
      i. Write Command: "w 30E 0"
      ii. Write Command: "w 304 [WriteAddress]"
      iii. Write Command: "w 306 [WriteData0]"
      iv. Write Command: "w 308 [WriteData1]"
      v. Write Command: "w 30A [WriteData2]"
      vi. Write Command: "w 30C [WriteData3]"
      vii. Write Command: "w 300 1"
      viii. Write Command: "w 300 0"
      ix. Continue writing 128-bit packets until the end of file is reached.
      x. Write Command: "w 300 0"
      xi. Write Command: "w 312 [ReadStartAddress_A]"
      xii. Write Command: "w 314 [ReadStopAddress_A]"
      xiii. Write Command: "w 100 60"
      xiv. Write Command: "w 100 20"
      xv. Write Command: "w 400 1"
      xvi. Write Command: "w 40E 0"
      xvii. Write Command: "w 30E 1"

5.3 Changing the Block RAM Waveform Selection

The Control FPGA will use one of the Block RAM Patterns uploaded to the microSD card by the user and the Block RAM Pattern Selection.

1. Perform an FPGA reset on the Data Path FPGA.
   (a) Execute the Block RAM Controller Reset Routine described in Section 5.1.4.
2. Enable Block RAM Write Mode.
   (a) Write Command: "w 380 01FF"
3. Disable Block RAM Read Mode.
   (a) Write Command: "w 38C 0"
4. Set the Block RAM Write Address, and 4 32-bit Data Registers.
   (a) Write Command: "w 382 [WriteAddress]"
   (b) Write Command: "w 384 [WriteData0]"
   (c) Write Command: "w 386 [WriteData1]"
   (d) Write Command: "w 388 [WriteData2]"
   (e) Write Command: "w 38A [WriteData3]"
   (f) Continue writing 128-bit packets until the end of file is reached.
5. Disable Block RAM Write Mode
   (a) Write Command: "w 380 0"
6. Set the Read Start/Stop Waveform Address(s).
   (a) Write Command: "w 38E [ReadStartAddress_A]"
   (b) Write Command: "w 390 [ReadStopAddress_A]"
7. Set the Waveform Mode to RAM.
   (a) Write Command: "w 400 1"
8. Set the RAM Mode to Block RAM.
   (a) Write Command: "w 40E 1"
9. Enable Block RAM Read Mode.
   (a) Write Command: "w 38C 1"

5.4 Changing the QDR-II SRAM Waveform Selection

The Control FPGA will use one of the QDR-II SRAM Waveforms uploaded to the microSD card by the user and the QDR-II SRAM Pattern Selection.

1. Perform an FPGA reset on the Data Path FPGA.
   (a) Execute the Xilinx SRAM Controller Reset Routine described in Section 5.1.2.
   (b) Execute the VCL SRAM Controller Reset Routine described in Section 5.1.3.
2. Disable QDR-II SRAM Read Mode.
   (a) Write Command: "w 30E 0"
3. Set the QDR-II SRAM Write Address, and 4 32-bit Data Registers.
   (a) Write Command: "w 304 [WriteAddress]"
   (b) Write Command: "w 306 [WriteData0]"
   (c) Write Command: "w 308 [WriteData1]"
   (d) Write Command: "w 30A [WriteData2]"
   (e) Write Command: "w 30C [WriteData3]"
   (f) Write Command: "w 300 1"
   (g) Write Command: "w 300 0"
   (h) Continue writing 128-bit packets until the end of file is reached.
4. Disable QDR-II SRAM Write Mode
   (a) Write Command: "w 300 0"
5. Set the Read Start/Stop Waveform Address(s).
   (a) Write Command: "w 312 [ReadStartAddress_A]"
   (b) Write Command: "w 314 [ReadStopAddress_A]"
6. Set the Waveform Mode to RAM.
   (a) Write Command: "w 400 1"
7. Set the RAM Mode to QDR-II SRAM.
   (a) Write Command: "w 40E 0"
8. Enable QDR-II SRAM Read Mode.
   (a) Write Command: "w 30E 1"

5.5 Setting Trigger Output

5.5.1 Waveform Trigger

5.5.1.1 Setting the RAM Waveform Trigger

The Control FPGA will enable RAM Waveform Trigger Mode when in selected by the user. The Waveform Mode must be set to RAM Waveforms for the RAM Waveform Trigger to be present on the trigger output (See Section **??**).

1. Set the Trigger Output Mode Register to Pattern.
   (a) Write Command: "w 500 1"
2. Set the Pattern Mode to RAM.
   (a) Write Command: "w 400 1"
3. Set the RAM Mode to either Block RAM or QDR-II SRAM.
   (a) Block RAM Mode = Write Command: "w 40E 1"
   (b) QDR-II SRAM Mode = Write Command: "w 40E 0"
4. Reset the Pattern Trigger Flip-Flop.
   (a) Write Command: "w 50A 0"
   (b) Write Command: "w 50A 2"

5.5.2 Divided Clock Trigger

5.5.2.1 Setting the Divided Clock Trigger

The Control FPGA will use the Divided Clock Trigger Selection provided by the user to set proper bits in the Divided Clock Trigger Control Register (See Section 6.2.5.4).

1. Use a Look Up Table to determine the encoded version of the Divided Clock Trigger selection provided by the user (See Section 6.2.5.4).
2. Set the Divided Clock Trigger Control Register.
   (a) Write Command: "w 50c [DivClkTrig_encoded]"
3. Set the Trigger Output Mode Register to Divided Clock.
   (a) Write Command: "w 500 0"
4. Reset the Pattern Trigger Flip-Flop.
   (a) Write Command: "w 50A 0"
   (b) Write Command: "w 50A 2"

6 Hardware Programming Model

6.1 Control Interface

he Data Path FPGA connects to the Control FPGA via a custom SPI interface.

6.2 Data Path FPGA Memory Map (Register and Bit)

Table 6.1: Hardware Register Addresses

Hardware Register Addresses			
Section	**Sub-System**	**Hardware Registers**	**Dev Address**
6.2.1	Measurement Board	System Registers	0x0000
6.2.2	Measurement Board	IODELAY Control Registers	0x0100
6.2.3	Measurement Board	RAM/User Pattern Control Registers	0x0300
6.2.4	Measurement Board	Auxiliary Input Control Registers	0x0400
6.2.5	Measurement Board	Trigger Control Registers	0x0500
6.2.6	Measurement Board	ADC Control Registers	0x0700
6.2.7	Measurement Board	AsAP Control Registers	0x0800

6.2.1 Base Address: 0x0000, System Registers

6.2.1.1 Safe State, Address: 0x0000

Hardware Function: 0x0
Device Address: 0x0000
Read/Write: Write Only

Writing anything to this register causes all Data Path FPGA registers to go into their reset state. This is the same state that the registers are in when the PED Data Path board assembly first powers up.

6.2.1.2 Instrument Reset Register, Address: 0x0002

Hardware Function: 0x0
Device Address: 0x0002
Read/Write: Read and Write

This is the Instrument Reset register. It is used to reset portions of the Data Path FPGA that may need to be reset during the operation of the instrument. Table 6.2 shows the register bit assignments and the default value. If a bit defaults to a 1, then that bit is active low. If a bit defaults to a 0, then that bit is active high.

Table 6.2: Instrument Reset Register

BIT	NAME	RESET
31:8	RSVD	0
7	WAVE_RST	1
6	ADC_FIFO_RST	0
5	RSVD	0
4	RAM_DAC_RST	1
3	SYS_DCM	0
2	SRAM_CTRL	1
1	XIL_SRAM_CTRL	0
0	SRAM_PLL	0

Table 6.3: Instrument Reset State

Bit	Reset	Description
7	WAVE_RST	Active Low
6	ADC_FIFO_RST	Active High
5	RSVD	Active High
4	RAM_DAC_RST	Active Low
3	SYS_DCM	Active High
2	SRAM_CTRL	Active Low
1	XIL_SRAM_CTRL	Active High
0	SRAM_PLL	Active High

6.2.1.3 Interrupt Register, Address: 0x0004

Hardware Function: 0x0
Device Address: 0x0004
Read/Write: Read Only

The Interrupt Register is used to tell the status of the interrupts of the assembly currently being addressed. It is a read only register.

The bits are assembly specific. A pending interrupt is indicated by the appropriate bit in the Interrupt Register being set. All interrupt bits are latched except for Bit 0. Bit 0 of the Interrupt Register is reserved to tell the status of the Interrupt Service Request (SRQn) output of the assembly. When Bit 0 is enabled, Bit 0 is the OR of the interrupt bits 1 through 31.

Table 6.4: Interrupt Register

BIT	NAME	RESET
31:7	RSVD	0
6	SRAM_CAL_DONE_ON	0
5	SRAM_CAL_DONE_OFF	0
4	SYS_DCM_LOCKED_ON	0
3	SYS_DCM_LOCKED_OFF	0
2	SRAM_DCM_LOCKED_ON	0
1	SRAM_DCM_LOCKED_OFF	0
0	SRQ	1

SRQ - Service Request Bit
0 = SRQn is NOT being driven low.
1 = SRQn is being driven low.
SRAM_DCM_LOCKED_OFF
0 = FALSE
1 = TRUE
SRAM_DCM_LOCKED_ON
0 = FALSE
1 = TRUE
SYS_DCM_LOCKED_OFF
0 = FALSE
1 = TRUE
SYS_DCM_LOCKED_ON
0 = FALSE
1 = TRUE
SRAM_CAL_DONE_OFF
0 = FALSE
1 = TRUE
SRAM_CAL_DONE_ON
0 = FALSE
1 = TRUE

6.2.1.4 Interrupt Enable Register, Address: 0x0006

Hardware Function: 0x0
Device Address: 0x0006
Read/Write: Read and Write

The Interrupt Enable Register is used to enable/disable the individual interrupts of the assembly currently being addressed. It is a write only register.

Each bit of the Interrupt Enable Register has a one to one correspondence with the bits in the Interrupt Register. Bit 0 of the Interrupt Enable Register is reserved to enable/disable the SRQn output of the assembly.

An interrupt is enabled by setting its bit in the Interrupt Enable Register. The enabled interrupts will always show their status in the Interrupt Register. Disabled interrupts do not cause interrupts but do show the latched status of the associated bit in the Interrupt Register. The latched interrupt status bits will still show their status even if the SRQ_EN bit is disabled. This allows the interrupts to be polled without causing the system controller to be interrupted.

Table 6.5: Interrupt Enable Register

BIT	NAME	RESET
31:7	RSVD	0
6	SRAM_CAL_DONE_ON	0
5	SRAM_CAL_DONE_OFF	0
4	SYS_DCM_LOCKED_ON	0
3	SYS_DCM_LOCKED_OFF	0
2	SRAM_DCM_LOCKED_ON	0
1	SRAM_DCM_LOCKED_OFF	0
0	SRQ_EN	1

SRQ - Service Request Bit
0 = SRQn output is disabled.
1 = SRQn output is enabled.
SRAM_DCM_LOCKED_OFF
0 = disabled
1 = enabled
SRAM_DCM_LOCKED_ON
0 = disabled
1 = enabled
SYS_DCM_LOCKED_OFF
0 = disabled
1 = enabled
SYS_DCM_LOCKED_ON
0 = disabled
1 = enabled
SRAM_CAL_DONE_OFF
0 = disabled
1 = enabled
SRAM_CAL_DONE_ON
0 = disabled
1 = enabled

6.2.1.5 Interrupt Clear Register, Address: 0x0008

Hardware Function: 0x0
Device Address: 0x0008
Read/Write: Write Only

The Interrupt Clear Register is used to clear the individual interrupts of the assembly currently being addressed. It is a write only register.

Each bit of the Interrupt Clear Register has a one to one correspondence with the bits in the Interrupt Register. Bit 0 of the Interrupt Clear Register does nothing since the SRQ interrupt is not latched. When the condition causing the interrupt is fixed, the CPU should clear the latched interrupt bit by writing a one to the corresponding bit in the Interrupt Clear Register.

Table 6.6: Interrupt Clear Register

BIT	NAME	RESET
31:7	RSVD	0
6	SRAM_CAL_DONE_ON	0
5	SRAM_CAL_DONE_OFF	0
4	SYS_DCM_LOCKED_ON	0
3	SYS_DCM_LOCKED_OFF	0
2	SRAM_DCM_LOCKED_ON	0
1	SRAM_DCM_LOCKED_OFF	0
0	No Effect	1

SRAM_DCM_LOCKED_OFF
0 = no change
1 = clear interrupt
SRAM_DCM_LOCKED_ON
0 = no change
1 = clear interrupt
SYS_DCM_LOCKED_OFF
0 = no change
1 = clear interrupt
SYS_DCM_LOCKED_ON
0 = no change
1 = clear interrupt
SRAM_CAL_DONE_OFF
0 = no change
1 = clear interrupt
SRAM_CAL_DONE_ON
0 = no change
1 = clear interrupt

6.2.1.6 Status Register, Address: 0x000A

Hardware Function: 0x0
Device Address: 0x000A
Read/Write: Read Only

Table 6.7: Status Register

BIT	NAME	RESET
31:7	RSVD	0
6	SRAM_CAL_DONE_ON	0
5	SRAM_CAL_DONE_OFF	0
4	SYS_DCM_LOCKED_ON	0
3	SYS_DCM_LOCKED_OFF	0
2	SRAM_DCM_LOCKED_ON	0
1	SRAM_DCM_LOCKED_OFF	0
0	No Effect	1

SRAM_DCM_LOCKED_OFF
0 = no change
1 = interrupt
SRAM_DCM_LOCKED_ON
0 = no change
1 = interrupt
SYS_DCM_LOCKED_OFF
0 = no change
1 = clear interrupt
SYS_DCM_LOCKED_ON
0 = no change
1 = clear interrupt
SRAM_CAL_DONE_OFF
0 = no change
1 = clear interrupt
SRAM_CAL_DONE_ON
0 = no change
1 = clear interrupt

6.2.1.7 Debug LED Register, Address: 0x000C

Hardware Function: 0x0
Device Address: 0x000C
Read/Write: Read and Write

This register is used to control the debug LEDs. Writing a 0 to this register will turn an LED on, and writing a 1 will turn an LED off. This register is used only for debugging purposes.

Table 6.8: Debug LED Register

BIT	NAME	RESET
31:4	RSVD	0
3:0	DEBUG_LEDS[3:0]	0x99

6.2.1.8 FPGA Date Code Register, Address: 0x000E

Hardware Function: 0x0
Device Address: 0x000E
Read/Write: Read Only

This is the FPGA Date Code register. It is used to determine what date and time the FPGA was built. The date code is essentially the UNIX time format.

Table 6.9: FPGA Date Code Register

BIT	NAME	RESET
31:0	DATECODE[31:0]	0x00000000

6.2.1.9 FPGA Version Register, Address: 0x0010

Hardware Function: 0x0
Device Address: 0x0010
Read/Write: Read Only

This register is used to determine the version of the FPGA being built. This register will be updated when major or minor changes have been applied to the FPGA. An example version for a first release in integer is 1.0.1.0. and hexadecimal is 0x01.0x01.0x0000

Table 6.10: FPGA Version Register

BIT	NAME	RESET
31:24	REV_MAJOR[31:24]	0x0100
23:16	REV_MINOR[23:16]	0x0001
15:0	REV_DEV[15:0]	0x0001

6.2.2 Base Address: 0x0100, IODELAY Control Registers

6.2.2.1 IDELAY_CTRL Reset Register, Address: 0x0100

Hardware Function: 0x0
Device Address: 0x0100
Read/Write: Read and Write

The IDELAY_CTRL Reset register is used to reset the IDELAY_CTRL blocks used in the Data Path FPGA. The IODELAY blocks will not function until the IDELAY_CTRL blocks are reset. A reset is performed by setting all bits in this register high-then-low.

Table 6.11: IDELAY_CTRL Reset Register

BIT	NAME	RESET
31:6	RSVD	0
5	RESERVED	0
4	RESERVED	0
3	RESERVED	0
2	RESERVED	0
1	ADC_IDLY_RST_CTRL	0
0	DAC_IDLY_RST_CTRL	0

6.2.2.2 IDELAY_CTRL Status Register, Address: 0x0102

Hardware Function: 0x0
Device Address: 0x0102
Read/Write: Read Only

The IDELAY_CTRL Status register is used to report the readiness of the IDELAY_CTRL block. The ready signals are active high.

Table 6.12: IDELAY_CTRL Status Register

BIT	NAME	RESET
31:4	RSVD	0
3	ADC_IDELAY_RDY	0
2	SRAM_Q_IDELAY_RDY	0
1	SRAM_D_IDELAY_RDY	0
0	SRAM_CTRL_IDELAY_RDY	0

6.2.3 Base Address: 0x0300, RAM/User Pattern Control Registers

6.2.3.1 Playback RAM Write Control Register, Address: 0x0300

Hardware Function: 0x0
Device Address: 0x0300
Read/Write: Read and Write

This is the Playback RAM Write Control register. This register initiates an SRAM 4-word burst write. The write data resides in registers 0x0306 to 0x030C, and the write address resides in register 0x0304. When performing an SRAM 4-word burst write, the CPU must toggle this bit high then low. The time between the SRAM Write Enable bit being set high then low is inconsequential, because a one-shot circuit inside the FPGA creates a single pulse one clock period wide when it detects a 0→1 transition on its input.

Table 6.13: Playback RAM Write Control Register

BIT	NAME	RESET
31:1	RSVD	0
0	PLAY_SRAM_WR_EN	0

6.2.3.2 Playback RAM Write Status Register, Address: 0x0302

Hardware Function: 0x0
Device Address: 0x0302
Read/Write: Read Only

This is the Playback RAM Write Status register. The SRAM_CAL_DONE bit indicates when the Xilinx QDR-II SRAM Controller has completed its calibration routine. The Control FPGA must wait until the SRAM_CAL_DONE bit goes high before it performs any SRAM related operations, especially if the PPG is currently in SRAM Pattern mode. The SRAM_WR_DONE bit indicates when a single 128-bit packet has been successfully written to the QDR-II SRAM. The Control FPGA must wait until the SRAM_WR_DONE bit goes high before initiating a new QDR-II SRAM Write Sequence.

Table 6.14: Playback RAM Write Control Register

BIT	NAME	RESET
31:2	RSVD	0
1	PLAY_SRAM_WR_DONE	0
0	SRAM_CAL_DONE	0

6.2.3.3 Playback RAM Write Address Register, Address: 0x0304

Hardware Function: 0x0
Device Address: 0x0304
Read/Write: Read and Write

These are the Playback RAM Write Address registers. These registers comprise a register that is 18-bits wide, and addresses the 4-word burst write transaction.

Table 6.15: Playback RAM Write Address Register

BIT	NAME	RESET
31:18	RSVD	0
17:0	PLAY_WR_ADDR[17:0]	0x00000

6.2.3.4 Playback RAM Write Data 0 Register, Address: 0x0306

Hardware Function: 0x0
Device Address: 0x0306
Read/Write: Read and Write

These are the Playback RAM Write Data 0 registers. These registers comprise a register that is 32-bits wide, and make up one word of the 4-word burst write transaction. This 32-bit packet is the LSB Word in the 128-bit packet.

Table 6.16: Playback RAM Write Data 0 Register

BIT	NAME	RESET
31:0	PLAY_WR0_DATA[31:0]	0x00000000

6.2.3.5 Playback RAM Write Data 1 Register, Address: 0x0308

Hardware Function: 0x0
Device Address: 0x0308
Read/Write: Read and Write

These are the Playback RAM Write Data 1 registers. These registers comprise a register that is 32-bits wide, and make up one word of the 4-word burst write transaction.

Table 6.17: Playback RAM Write Data 1 Register

BIT	NAME	RESET
31:0	PLAY_WR1_DATA[31:0]	0x00000000

6.2.3.6 Playback RAM Write Data 2 Register, Address: 0x030A

Hardware Function: 0x0
Device Address: 0x030A
Read/Write: Read and Write

These are the Playback RAM Write Data 2 registers. These registers comprise a register that is 32-bits wide, and make up one word of the 4-word burst write transaction.

Table 6.18: Playback RAM Write Data 2 Register

BIT	NAME	RESET
31:0	PLAY_WR2_DATA[31:0]	0x00000000

6.2.3.7 Playback RAM Write Data 3 Register, Address: 0x030C

Hardware Function: 0x0
Device Address: 0x030C
Read/Write: Read and Write

These are the Playback RAM Write Data 3 registers. These registers comprise a register that is 32-bits wide, and make up one word of the 4-word burst write transaction. This 32-bit packet is the MSB Word in the 128-bit packet.

Table 6.19: Playback RAM Write Data 3 Register

BIT	NAME	RESET
31:0	PLAY_WR3_DATA[31:0]	0x00000000

6.2.3.8 Playback RAM Read Control Register, Address: 0x030E

Hardware Function: 0x0
Device Address: 0x030E
Read/Write: Read and Write

This is the Playback RAM Read Control register. This register initiates an SRAM read. The read address resides in registers 0x0312 to 0x0318. When performing an SRAM Read initiation, the CPU must toggle this bit high then low. The time between the SRAM Read Enable bit being set high then low is inconsequential, because a one-shot circuit inside the FPGA creates a single pulse one clock period wide when it detects a 0→1 transition on its input.

Table 6.20: Playback RAM Read Control Register

BIT	NAME	RESET
31:1	RSVD	0
0	PLAY_SRAM_RD_EN	0

6.2.3.9 Playback RAM Read Status Register, Address: 0x0310

Hardware Function: 0x0
Device Address: 0x0310
Read/Write: Read Only

This is the Playback RAM Read Status register. This register is a place holder for any important information related to SRAM read operations.

Table 6.21: Playback RAM Read Control Register

BIT	NAME	RESET
31:2	RSVD	0
0	PLAY_SRAM_RD_DONE	0
0	SRAM_CAL_DONE	0

6.2.3.10 Playback RAM Read Start Address Register, Address: 0x0312

Hardware Function: 0x0
Device Address: 0x0312
Read/Write: Read and Write

This is the Playback RAM Read Start Address register. This register indicates the start address for the pattern. It is 18-bits wide, and addresses the 4-word burst read transaction.

Table 6.22: Playback RAM Read Start Address Register

BIT	NAME	RESET
31:18	RSVD	0
17:0	PLAY_RD_START_ADDR[17:0]	0

6.2.3.11 Playback RAM Read Stop Address Register, Address: 0x0314

Hardware Function: 0x0
Device Address: 0x0314
Read/Write: Read and Write

This is the Playback RAM Read Stop Address register. This register indicates the stop address for the pattern. It is 18-bits wide, and addresses the 4-word burst read transaction.

Table 6.23: RAM Read Stop Address (Pattern A) Register

BIT	NAME	RESET
31:18	RSVD	0
17:0	PLAY_RD_STOP_ADDR[17:0]	0

6.2.3.12 Playback RAM Read Increment Address Register, Address: 0x0316

Hardware Function: 0x0
Device Address: 0x0316
Read/Write: Read and Write

This is the Playback RAM Read Increment Address register. This register indicates the value that the SRAM address is incremented when streaming data from SRAM. It is 18-bits wide.

Table 6.24: Playback RAM Read Increment Address Register

BIT	NAME	RESET
31:18	RSVD	0
17:0	PLAY_RD_INC_ADDR[17:0]	0x00001

6.2.3.13 Playback RAM Read Maximum Address Register, Address: 0x0318

Hardware Function: 0x0
Device Address: 0x0318
Read/Write: Read and Write

This is the Playback RAM Read Maximum Address register. This register indicates the maximum initial address, which is used to pre-load the SRAM stream address counter. It is 18-bits wide.

Table 6.25: Playback RAM Read Maximum Address Register

BIT	NAME	RESET
31:18	RSVD	0
17:0	PLAY_RD_MAX_ADDR[17:0]	0x3FFFF

6.2.3.14 Xilinx SRAM Controller Done Status Register, Address: 0x031A

Hardware Function: 0x0
Device Address: 0x031A
Read/Write: Read Only

This is the Xilinx SRAM Controller Done Status register. This register is used troubleshoot the calibration routine in the Xilinx SRAM Controller. The calibration routine is made up of several stages. Each stage of the routine is complete when its status bit goes high.

Table 6.26: Xilinx SRAM Controller Done Status Register

BIT	NAME	RESET
31:8	RSVD	0
7	INIT_COUNT_DONE	0
6	Q_CQp_INIT_DELAY_DONE	0
5	Q_CQn_INIT_DELAY_DONE	0
4	CQp_CAL_DONE	0
3	CQn_CAL_DONE	0
2	WE_CAL_DONE_CQp	0
1	WE_CAL_DONE_CQn	0
0	CAL_DONE	0

6.2.3.15 Xilinx SRAM Controller Count Status Register, Address: 0x031C

Hardware Function: 0x0
Device Address: 0x031C
Read/Write: Read Only

This is the Xilinx SRAM Controller Count Status register. This register is used troubleshoot the calibration routine in the Xilinx SRAM Controller. The calibration routine is made up of several stages. Each stage of the routine calculates a tap count that is used to center the CQ_p clock in the lower 18-bits of read data and the CQ_n clock in the upper 18-bits of read data.

Table 6.27: Xilinx SRAM Controller Count Status Register

BIT	NAME	RESET
31:26	RSVD	0
25:20	Q_CQp_INIT_DELAY_DONE_TAP_CNT[5:0]	0
19:14	Q_CQn_INIT_DELAY_DONE_TAP_CNT[5:0]	0
13:8	CQp_CAL_TAP_CNT[5:0]	0
7:2	CQn_CAL_TAP_CNT[5:0]	0
1	CQp_Q_DATA_VALID	0
0	CQn_Q_DATA_VALID	0

6.2.3.16 Xilinx SRAM Controller Debug Control Register, Address: 0x031E

Hardware Function: 0x0
Device Address: 0x031E
Read/Write: Read Only

This is the Xilinx SRAM Controller Debug Control register. This register is used troubleshoot the calibration routine in the Xilinx SRAM Controller. The signals below allow for manual control of the calibration routines. For a detailed description of the signals below, see the appendix of the Xilinx MIG User's Guide (ug086.pdf). The User Guide can be downloaded here:

http://www.xilinx.com/support/documentation/ip_documentation/ug086.pdf

Table 6.28: Xilinx SRAM Controller Debug Control Register

BIT	NAME	RESET
31:18	RSVD	0
17	DBG_IDEL_UP_ALL	0
16	DBG_IDEL_DOWN_ALL	0
15	DBG_SEL_ALL_IDEL_CQ	0
14	DBG_SEL_IDEL_CQ	0
13	DBG_IDEL_UP_CQ	0
12	DBG_IDEL_DOWN_CQ	0
11	DBG_SEL_ALL_IDEL_CQ_n	0
10	DBG_SEL_IDEL_CQ_n	0
9	DBG_IDEL_UP_CQ_n	0
8	DBG_IDEL_DOWN_CQ_n	0
7	DBG_SEL_ALL_IDEL_Q_CQ	0
6	DBG_SEL_IDEL_Q_CQ	0
5	DBG_SEL_ALL_IDEL_Q_CQ_n	0
4	DBG_IDEL_UP_Q_CQ	0
3	DBG_IDEL_DOWN_Q_CQ	0
2	DBG_SEL_IDEL_Q_CQ_n	0
1	DBG_IDEL_UP_Q_CQ_n	0
0	DBG_IDEL_DOWN_Q_CQ_n	0

6.2.3.17 Centellax SRAM Controller FIFO Status Register, Address: 0x0320

Hardware Function: 0x0
Device Address: 0x0320
Read/Write: Read Only

This is the Centellax SRAM Controller FIFO Status register. This register is used troubleshoot the read data path of the SRAM Controllers. These bits should always be 0.

Table 6.29: Centellax SRAM Controller FIFO Status Register

BIT	NAME	RESET
31:2	RSVD	0
1	SRAM_FIFO_FULL	0
0	SRAM_FIFO_EMPTY	0

6.2.3.18 Playback RAM Write Trigger Data Register, Address: 0x0322

Hardware Function: 0x0
Device Address: 0x0322
Read/Write: Read and Write

This is the Playback RAM Write Trigger Data registers. This register contains trigger location bits that are stored in the MSB 4-bits of each of the 4x 36-bit SRAM words. This trigger data is all ones at the first location in the SRAM, and all zeros at all remaining SRAM locations. This allows the trigger pulse to be synchronous to the SRAM data.

Table 6.30: Playback RAM Write Trigger Data Register

BIT	NAME	RESET
31:16	RSVD	0
15:0	PLAY_TRIG_DATA[15:0]	0x0000

6.2.3.19 Capture RAM Read Control Register, Address: 0x0324

Hardware Function: 0x0
Device Address: 0x0324
Read/Write: Read and Read

This is the Capture RAM Read Control register. This register initiates an SRAM 4-word burst read. The read data resides in registers 0x0328 to 0x032E, and the read address resides in register 0x0326. When performing an SRAM 4-word burst read, the CPU must toggle the CAP_SRAM_RD_EN bit high then low. The time between the Capture SRAM Read Enable bit being set high then low is inconsequential, because a one-shot circuit inside the FPGA creates a single pulse one clock period wide when it detects a 0→1 transition on its input. To enable Capture mode set CAP_NPLAY to a logic high. To enable Playback mode set CAP_NPLAY to a logic low.

Table 6.31: Capture RAM Read Control Register

BIT	NAME	RESET
31:3	RSVD	0
2	CAP_NPLAY	0
1	CAP_SRAM_RD_EN	0
0	RSVD	0

6.2.3.20 Capture RAM Read Address Register, Address: 0x0326

Hardware Function: 0x0
Device Address: 0x0326
Read/Write: Read and Write

These are the Capture RAM Read Address registers. This register is 18-bits wide, and addresses the 4-word burst read transaction.

Table 6.32: Capture RAM Read Address Register

BIT	NAME	RESET
31:18	RSVD	0
17:0	CAP_RD_ADDR[17:0]	0x00000

6.2.3.21 Capture RAM Write Start Address Register, Address: 0x0328

Hardware Function: 0x0
Device Address: 0x0328
Read/Write: Read and Write

This is the Capture RAM Write Start Address register. This register indicates the start address that the data is streamed into the SRAM. It is 18-bits wide.

Table 6.33: Capture RAM Write Start Address Register

BIT	NAME	RESET
31:18	RSVD	0
17:0	CAP_WR_START_ADDR[17:0]	0x00000

6.2.3.22 Capture RAM Write Stop Address Register, Address: 0x032A

Hardware Function: 0x0
Device Address: 0x032A
Read/Write: Read and Write

This is the Capture RAM Write Stop Address register. This register indicates the stop address that the data is streamed into the SRAM. It is 18-bits wide.

Table 6.34: Capture RAM Write Stop Address Register

BIT	NAME	RESET
31:18	RSVD	0
17:0	CAP_WR_STOP_ADDR[17:0]	0x3FFFF

6.2.3.23 Capture RAM Write Increment Address Register, Address: 0x032C

Hardware Function: 0x0
Device Address: 0x032C
Read/Write: Read and Write

This is the Capture RAM Write Increment Address register. This register indicates the value that the SRAM address is incremented when streaming data into the SRAM. It is 18-bits wide.

Table 6.35: Capture RAM Write Increment Address Register

BIT	NAME	RESET
31:18	RSVD	0
17:0	CAP_WR_INC_ADDR[17:0]	0x00001

6.2.3.24 Capture RAM Write Maximum Address Register, Address: 0x032E

Hardware Function: 0x0
Device Address: 0x032E
Read/Write: Read and Write

This is the Capture RAM Write Maximum Address register. This register indicates the maximum initial address, which is used to pre-load the SRAM stream address counter. It is 18-bits wide.

Table 6.36: Capture RAM Read Maximum Address Register

BIT	NAME	RESET
31:18	RSVD	0
17:0	CAP_WR_MAX_ADDR[17:0]	0x3FFFE

6.2.3.25 Capture RAM Read Data 0 Register, Address: 0x0330

Hardware Function: 0x0
Device Address: 0x0330
Read/Write: Read Only

These are the Capture RAM Read Data 0 registers. These registers comprise a register that is 16-bits wide, and make up one word of the 4-word burst read transaction. This 16-bit packet is the LSB Word in the 128-bit packet.

Table 6.37: Capture RAM Read Data 0 Register

BIT	NAME	RESET
31:16	RSVD	0
15:0	CAP_RD0_DATA[15:0]	0x0000

6.2.3.26 Capture RAM Read Data 1 Register, Address: 0x0332

Hardware Function: 0x0
Device Address: 0x0332
Read/Write: Read Only

These are the Capture RAM Read Data 1 registers. These registers comprise a register that is 16-bits wide, and make up one word of the 4-word burst read transaction.

Table 6.38: Capture RAM Read Data 1 Register

BIT	NAME	RESET
31:16	RSVD	0
15:0	CAP_RD1_DATA[15:0]	0x0000

6.2.3.27 Capture RAM Read Data 2 Register, Address: 0x0334

Hardware Function: 0x0
Device Address: 0x0334
Read/Write: Read Only

These are the Capture RAM Read Data 2 registers. These registers comprise a register that is 16-bits wide, and make up one word of the 4-word burst read transaction.

Table 6.39: Capture RAM Read Data 2 Register

BIT	NAME	RESET
31:16	RSVD	0
15:0	CAP_RD2_DATA[15:0]	0x0000

6.2.3.28 Capture RAM Read Data 3 Register, Address: 0x0336

Hardware Function: 0x0
Device Address: 0x0336
Read/Write: Read Only

These are the Capture RAM Read Data 3 registers. These registers comprise a register that is 16-bits wide, and make up one word of the 4-word burst read transaction.

Table 6.40: Capture RAM Read Data 3 Register

BIT	NAME	RESET
31:16	RSVD	0
15:0	CAP_RD3_DATA[15:0]	0x0000

6.2.3.29 Capture RAM Read Data 4 Register, Address: 0x0338

Hardware Function: 0x0
Device Address: 0x0338
Read/Write: Read Only

These are the Capture RAM Read Data 4 registers. These registers comprise a register that is 16-bits wide, and make up one word of the 4-word burst read transaction.

Table 6.41: Capture RAM Read Data 4 Register

BIT	NAME	RESET
31:16	RSVD	0
15:0	CAP_RD4_DATA[15:0]	0x0000

6.2.3.30 Capture RAM Read Data 5 Register, Address: 0x033A

Hardware Function: 0x0
Device Address: 0x033A
Read/Write: Read Only

These are the Capture RAM Read Data 5 registers. These registers comprise a register that is 16-bits wide, and make up one word of the 4-word burst read transaction.

Table 6.42: Capture RAM Read Data 5 Register

BIT	NAME	RESET
31:16	RSVD	0
15:0	CAP_RD5_DATA[15:0]	0x0000

6.2.3.31 Capture RAM Read Data 6 Register, Address: 0x033C

Hardware Function: 0x0
Device Address: 0x033C
Read/Write: Read Only

These are the Capture RAM Read Data 6 registers. These registers comprise a register that is 16-bits wide, and make up one word of the 4-word burst read transaction.

Table 6.43: Capture RAM Read Data 6 Register

BIT	NAME	RESET
31:16	RSVD	0
15:0	CAP_RD6_DATA[15:0]	0x0000

6.2.3.32 Capture RAM Read Data 7 Register, Address: 0x033E

Hardware Function: 0x0
Device Address: 0x033E
Read/Write: Read Only

These are the Capture RAM Read Data 7 registers. These registers comprise a register that is 16-bits wide, and make up one word of the 4-word burst read transaction. This 16-bit packet is the MSB word in the 128-bit data word.

Table 6.44: Capture RAM Read Data 6 Register

BIT	NAME	RESET
31:16	RSVD	0
15:0	CAP_RD7_DATA[15:0]	0x0000

6.2.3.33 Capture RAM Read Data 8 Register, Address: 0x0340

Hardware Function: 0x0
Device Address: 0x0340
Read/Write: Read Only

These are the Capture RAM Read Data 8 registers. These registers comprise a register that is 16-bits wide, and make up one word of the 4-word burst read transaction. This 16-bit packet contains the corresponding overflow flags for the 128-bit packet.

Table 6.45: Capture RAM Read Data 7 Register

BIT	NAME	RESET
31:16	RSVD	0
15:0	CAP_RD8_DATA[15:0]	0x0000

6.2.3.34 Capture RAM Read Status Register, Address: 0x0342

Hardware Function: 0x0
Device Address: 0x0342
Read/Write: Read Only

This is the Capture RAM Read Status register. The CAP_SRAM_RD_DONE bit indicates when a single 128-bit packet has been successfully read from the QDR-II SRAM. The Control FPGA must wait until the CAP_SRAM_RD_DONE bit goes high before initiating a new QDR-II SRAM Read Sequence.

Table 6.46: Capture RAM Read Status Register

BIT	NAME	RESET
31:2	RSVD	0
1	CAP_SRAM_RD_DONE	0
0	RSVD	1

6.2.3.35 Playback RAM FIFO Read Count Register, Address: 0x0344

Hardware Function: 0x0
Device Address: 0x0344
Read/Write: Read Only

This is the Playback RAM FIFO Read Count register. The PLAY_SRAM_FIFO_RD_CNT register indicates how many words are in the SRAM Playback FIFO.

Table 6.47: Playback RAM FIFO Read Count Register

BIT	NAME	RESET
31:12	RSVD	0
11:0	PLAY_SRAM_FIFO_RD_CNT[11:0]	0

6.2.3.36 Playback Block RAM Write Control Register, Address: 0x0380

Hardware Function: 0x0
Device Address: 0x0380
Read/Write: Read and Write

This is the Playback Block RAM Write Control register. This register initiates a Block RAM 128-bit write. When performing a Block RAM 128-bit write, the CPU must set these bits high.

Table 6.48: Playback Block RAM Write Control Register

BIT	NAME	RESET
31:1	RSVD	0
0	PLAY_BRAM_WR_EN	0

6.2.3.37 Playback Block RAM Write Address Register, Address: 0x0382

Hardware Function: 0x0
Device Address: 0x0382
Read/Write: Read and Write

This is the Playback Block RAM Write Address register. This register is 14-bits wide, and addresses the 128-bit write transaction.

Table 6.49: Playback Block RAM Write Address Register

BIT	NAME	RESET
31:14	RSVD	0
13:0	PLAY_BRAM_WR_ADDR[13:0]	0x0000

6.2.3.38 Playback Block RAM Write Data 0 Register, Address: 0x0384

Hardware Function: 0x0
Device Address: 0x0384
Read/Write: Read and Write

This is the Playback Block RAM Write Data 0 register. This register is 32-bits wide, and makes up one word of the 128-bit write transaction. This 32-bit packet is the LSB Word in the 128-bit packet.

Table 6.50: Playback Block RAM Write Data 0 Register

BIT	NAME	RESET
31:0	PLAY_BRAM_WR0_DATA[31:0]	0x00000000

6.2.3.39 Playback Block RAM Write Data 1 Register, Address: 0x0386

Hardware Function: 0x0
Device Address: 0x0386
Read/Write: Read and Write

This is the Playback Block RAM Write Data 1 register. This register is 32-bits wide, and makes up one word of the 128-bit write transaction.

Table 6.51: Playback Block RAM Write Data 1 Register

BIT	NAME	RESET
31:0	PLAY_BRAM_WR1_DATA[31:0]	0x00000000

6.2.3.40 Playback Block RAM Write Data 2 Register, Address: 0x0388

Hardware Function: 0x0
Device Address: 0x0388
Read/Write: Read and Write

This is the Playback Block RAM Write Data 2 register. This register is 32-bits wide, and makes up one word of the 128-bit write transaction.

Table 6.52: Playback Block RAM Write Data 2 Register

BIT	NAME	RESET
31:0	BRAM_WR2_DATA[31:0]	0x00000000

6.2.3.41 Playback Block RAM Write Data 3 Register, Address: 0x038A

Hardware Function: 0x0
Device Address: 0x038A
Read/Write: Read and Write

This is the Playback Block RAM Write Data 3 register. This register is 32-bits wide, and makes up one word of the 128-bit write transaction. This 32-bit packet is the MSB Word in the 128-bit packet.

Table 6.53: Playback Block RAM Write Data 3 Register

BIT	NAME	RESET
31:0	PLAY_BRAM_WR3_DATA[31:0]	0x00000000

6.2.3.42 Playback Block RAM Read Control Register, Address: 0x038C

Hardware Function: 0x0
Device Address: 0x038C
Read/Write: Read and Write

This is the Playback Block RAM Read Control register. This register initiates an Block RAM read. When performing a Block RAM Read initiation, the CPU must set bit 0 high.

Table 6.54: Playback Block RAM Read Control Register

BIT	NAME	RESET
31:1	RSVD	0
0	PLAY_BRAM_RD_EN	0

6.2.3.43 Playback Block RAM Read Start Address Register, Address: 0x038E

Hardware Function: 0x0
Device Address: 0x038E
Read/Write: Read and Write

This is the Playback Block RAM Read Start Address (Pattern A) register. This register is 14-bits wide, and addresses the 4-word burst read transaction.

Table 6.55: Block RAM Read Start Address Register

BIT	NAME	RESET
31:14	RSVD	0
13:0	PLAY_BRAM_RD_START_ADDR[13:0]	0

6.2.3.44 Playback Block RAM Read Stop Address Register, Address: 0x0390

Hardware Function: 0x0
Device Address: 0x0390
Read/Write: Read and Write

These are the Playback Block RAM Read Stop Address register. This register is 14-bits wide, and addresses the 128-bit read transaction.

Table 6.56: Playback Block RAM Read Stop Address Register

BIT	NAME	RESET
31:14	RSVD	0
13:0	PLAY_BRAM_RD_STOP_ADDR[13:0]	0

6.2.3.45 Capture Block RAM Read Data 0 Register, Address: 0x039A

Hardware Function: 0x0
Device Address: 0x039A
Read/Write: Read Only

These are the Capture Block RAM Read Data 0 registers. These registers comprise a register that is 16-bits wide, and make up one word of the 128-bit read transaction. This 16-bit packet is the LSB Word in the 128-bit packet.

Table 6.57: Capture Block RAM Read Data 0 Register

BIT	NAME	RESET
31:16	RSVD	0
15:0	CAP_RD0_DATA[15:0]	0x0000

6.2.3.46 Capture Block RAM Read Data 1 Register, Address: 0x039C

Hardware Function: 0x0
Device Address: 0x039C
Read/Write: Read Only

These are the Capture Block RAM Read Data 1 registers. These registers comprise a register that is 16-bits wide, and make up one word of the 128-bit read transaction.

Table 6.58: Capture Block RAM Read Data 1 Register

BIT	NAME	RESET
31:16	RSVD	0
15:0	CAP_RD1_DATA[15:0]	0x0000

6.2.3.47 Capture Block RAM Read Data 2 Register, Address: 0x039E

Hardware Function: 0x0
Device Address: 0x039E
Read/Write: Read Only

These are the Capture Block RAM Read Data 2 registers. These registers comprise a register that is 16-bits wide, and make up one word of the 128-bit read transaction.

Table 6.59: Capture Block RAM Read Data 2 Register

BIT	NAME	RESET
31:16	RSVD	0
15:0	CAP_RD2_DATA[15:0]	0x0000

6.2.3.48 Capture Block RAM Read Data 3 Register, Address: 0x03A0

Hardware Function: 0x0
Device Address: 0x03A0
Read/Write: Read Only

These are the Capture Block RAM Read Data 3 registers. These registers comprise a register that is 16-bits wide, and make up one word of the 128-bit read transaction.

Table 6.60: Capture Block RAM Read Data 3 Register

BIT	NAME	RESET
31:16	RSVD	0
15:0	CAP_RD3_DATA[15:0]	0x0000

6.2.3.49 Capture Block RAM Read Data 4 Register, Address: 0x03A2

Hardware Function: 0x0
Device Address: 0x03A2
Read/Write: Read Only

These are the Capture Block RAM Read Data 4 registers. These registers comprise a register that is 16-bits wide, and make up one word of the 128-bit read transaction.

Table 6.61: Capture Block RAM Read Data 4 Register

BIT	NAME	RESET
31:16	RSVD	0
15:0	CAP_RD4_DATA[15:0]	0x0000

6.2.3.50 Capture Block RAM Read Data 5 Register, Address: 0x03A4

Hardware Function: 0x0
Device Address: 0x03A4
Read/Write: Read Only

These are the Capture Block RAM Read Data 5 registers. These registers comprise a register that is 16-bits wide, and make up one word of the 128-bit read transaction.

Table 6.62: Capture Block RAM Read Data 5 Register

BIT	NAME	RESET
31:16	RSVD	0
15:0	CAP_RD5_DATA[15:0]	0x0000

6.2.3.51 Capture Block RAM Read Data 6 Register, Address: 0x03A6

Hardware Function: 0x0
Device Address: 0x03A6
Read/Write: Read Only

These are the Capture Block RAM Read Data 6 registers. These registers comprise a register that is 16-bits wide, and make up one word of the 128-bit read transaction.

Table 6.63: Capture Block RAM Read Data 6 Register

BIT	NAME	RESET
31:16	RSVD	0
15:0	CAP_RD6_DATA[15:0]	0x0000

6.2.3.52 Capture Block RAM Read Data 7 Register, Address: 0x03A8

Hardware Function: 0x0
Device Address: 0x03A8
Read/Write: Read Only

These are the Capture Block RAM Read Data 7 registers. These registers comprise a register that is 16-bits wide, and make up one word of the 128-bit read transaction. This 16-bit packet is the MSB word in the 128-bit data word.

Table 6.64: Capture Block RAM Read Data 6 Register

BIT	NAME	RESET
31:16	RSVD	0
15:0	CAP_RD7_DATA[15:0]	0x0000

6.2.3.53 Capture Block RAM Read Data 8 Register, Address: 0x03AA

Hardware Function: 0x0
Device Address: 0x03AA
Read/Write: Read Only

These are the Capture Block RAM Read Data 8 registers. These registers comprise a register that is 16-bits wide, and make up one word of the 128-bit read transaction. This 16-bit packet contains the corresponding overflow flags for the 128-bit packet.

Table 6.65: Capture Block RAM Read Data 7 Register

BIT	NAME	RESET
31:16	RSVD	0
15:0	CAP_RD8_DATA[15:0]	0x0000

6.2.3.54 Capture Block RAM Write Status Register, Address: 0x03AC

Hardware Function: 0x0
Device Address: 0x03AC
Read/Write: Read Only

This is the Capture Block RAM Write Status register. The CAP_BRAM_WR_DONE bit indicates when a single 128-bit packet has been successfully read from the Block RAM. The Control FPGA must wait until the CAP_BRAM_WR_DONE bit goes high before initiating a new Block RAM Write Sequence.

Table 6.66: Capture Block RAM Write Status Register

BIT	NAME	RESET
31:1	RSVD	0
0	CAP_BRAM_WR_DONE	0

6.2.3.55 Playback Block RAM Write Trigger Register, Address: 0x03AE

Hardware Function: 0x0
Device Address: 0x03AE
Read/Write: Read and Write

These are the Playback Block RAM Write Trigger registers. This 16-bit packet is the trigger word for the 128-bit data word.

Table 6.67: Playback Block RAM Write Trigger Register

BIT	NAME	RESET
31:16	RSVD	0
15:0	PLAY_BRAM_WR_TRIG[15:0]	0x0000

6.2.4 Base Address: 0x0400, Miscellaneous Control Registers

6.2.4.1 AUX Input Control Register, Address: 0x0400

Hardware Function: 0x0
Device Address: 0x0400
Read/Write: Read and Write

The AUX Input Control register is used to set the current mode of the external AUX Input. The states of the AUX Input Control register are shown in Table 6.69.

Table 6.68: AUX Input Control Register

BIT	NAME	RESET
31:3	RSVD	0
2:0	AUX_CTRL	0

Table 6.69: AUX Input Control Modes

AUX_CTRL			Mode
2	**1**	**0**	
0	x	x	Disabled
1	0	0	Gating
1	1	0	Sweep

6.2.4.2 RAM Select Register, Address: 0x0402

Hardware Function: 0x0
Device Address: 0x0402
Read/Write: Read and Write

The RAM Select register is used to select between Block RAM patterns and QDR-II SRAM patterns. The states of the RAM Select register are shown in Table 6.76.

Table 6.70: Pattern Select Register

BIT	NAME	RESET
31:1	RSVD	0
0	BRAM_nSRAM	0

Table 6.71: RAM Select Modes

BRAM_nSRAM	Mode
0	QDR-II SRAM Pattern
1	Block RAM Pattern

6.2.4.3 Sweep Control Register, Address: 0x0404

Hardware Function: 0x0
Device Address: 0x0404
Read/Write: Read and Write

This is the Sweep Control register. This register is used to enable sweep.

Table 6.72: Sweep Control Register

BIT	NAME	RESET
31:1	RSVD	0
0	SWEEP	0

6.2.4.4 Gating Control Register, Address: 0x0406

Hardware Function: 0x0
Device Address: 0x0406
Read/Write: Read and Write

This is the Gating Control register. This register is used to enable waveform gating.

Table 6.73: Gating Control Register

BIT	NAME	RESET
31:1	RSVD	0
0	GATE	0

6.2.4.5 Waveform Enable Register, Address: 0x0408

Hardware Function: 0x0
Device Address: 0x0408
Read/Write: Read and Write

This is the Waveform Enable register. This register is used to enable waveform.

Table 6.74: Waveform Enable Register

BIT	NAME	RESET
31:1	RSVD	0
0	WAVE_EN	0

6.2.4.6 DC/RAM Select Register, Address: 0x040A

Hardware Function: 0x0
Device Address: 0x040A
Read/Write: Read and Write

The DC/RAM Select register is used to select between RAM patterns and a DC value of 16'h0000. The states of the DC/RAM Select register are shown in Table **??**.

Table 6.75: Pattern Select Register

BIT	NAME	RESET
31:1	RSVD	0
0	DC_nRAM	0

Table 6.76: RAM Select Modes

BRAM_nSRAM	Mode
0	RAM Pattern
1	DC Value

6.2.4.7 Pattern Shift Register, Address: 0x040C

Hardware Function: 0x0
Device Address: 0x040C
Read/Write: Read and Write

The Pattern Shift register is used to perform a shift by 16-K bits, where the value of this register is 2^K. The states of the Pattern Shift register are shown in Table 6.78.

Table 6.77: Pattern Shift Register

BIT	NAME	RESET
31:16	RSVD	0
15:0	WAVE_SHIFT[15:0]	0x0001

Table 6.78: Pattern Shift Modes

Bits to Shift	Value
0	0x10000
1	0x08000
2	0x04000
3	0x02000
4	0x01000
5	0x00800
6	0x00400
7	0x00200
8	0x00100
9	0x00080
10	0x00040
11	0x00020
12	0x00010
13	0x00008
14	0x00004
15	0x00002
16	0x00001

6.2.4.8 Pattern Invert Register, Address: 0x040E

Hardware Function: 0x0
Device Address: 0x040E
Read/Write: Read and Write

The Pattern Invert register is used to perform a two's complement invert of the current pattern. The states of the Pattern Invert register are shown in Table 6.80.

Table 6.79: Pattern Invert Register

BIT	NAME	RESET
31:16	RSVD	0
15:0	WAVE_INVERT[15:0]	0x0001

Table 6.80: Pattern Invert Modes

PAT_INV	Mode
0x0001	Normal Pattern
0xFFFF	Inverted Pattern

6.2.5 Base Address: 0x0500, Trigger Control Registers

6.2.5.1 Trigger Output Mode Register, Address: 0x0500

Hardware Function: 0x0
Device Address: 0x0500
Read/Write: Read and Write

This is the Trigger Output Mode register. This register controls the type of trigger present on the front panel.

Table 6.81: Trigger Output Mode Register

BIT	NAME	RESET
31:1	RSVD	0
0	TRIG_OUT_MODE	1

Table 6.82: Trigger Output Modes

TRIG_OUT_MODE	Mode
0	Divided Clock Trigger
1	Pattern Trigger

6.2.5.2 Trigger RAM Mode Register, Address: 0x0502

Hardware Function: 0x0
Device Address: 0x0502
Read/Write: Read and Write

This is the Trigger RAM Mode register. This register controls the type of trigger for the RAM Patterns.

Table 6.83: Trigger RAM Mode Register

BIT	NAME	RESET
31:1	RSVD	0
0	TRIG_RAM_MODE	0

Table 6.84: Trigger RAM Modes

TRIG_RAM_MODE	Mode
0	A Only Pattern Trigger
1	A/B Pattern Trigger

6.2.5.3 RAM Pattern A Trigger Address Register, Address: 0x0504

Hardware Function: 0x0
Device Address: 0x0504
Read/Write: Read and Write

This is the RAM Pattern A Trigger Address register. This register is 18-bits wide, and makes up the RAM pattern A trigger address register used by the RAM Pattern Trigger Module.

Table 6.85: RAM Pattern A Trigger Address Register

BIT	NAME	RESET
31:18	RSVD	0
17:0	RAM_APATRN_TRIG[17:0]	0x2AAAA

6.2.5.4 Divided Clock Trigger Control Register, Address: 0x0506

Hardware Function: 0x0
Device Address: 0x0506
Read/Write: Read and Write

This is the Divided Clock Trigger Control register. This register is used to select the divided clock frequency.

Table 6.86: Divided Clock Trigger Control Register

BIT	NAME	RESET
31:2	RSVD	0
1:0	DIV_CLK_TRIG[1:0]	0b01

Table 6.87: Divided Clock Trigger Modes

DIV_CLK_TRIG	Mode	Frequency
00	clk	500MHz
01	$\frac{clk}{2}$ (default)	250MHz
10	$\frac{clk}{4}$	125MHz
11	$\frac{clk}{8}$	62.5MHz

6.2.6 Base Address: 0x0700, ADC Control Registers

6.2.6.1 ADC Data FIFO Empty Register, Address: 0x071A

Hardware Function: 0x0
Device Address: 0x071A
Read/Write: Read and Write

The ADC Data FIFO Empty register is used to read the Empty status of the FIFOs. These will most likely be used for debug only as the FIFOs are continuously filled and emptied.

Table 6.88: ADC Data FIFO Empty Register

BIT	NAME	RESET
31:18	RSVD	0
17:0	MUX_FIFO_EMPTY	0

6.2.6.2 ADC Data FIFO Full Register, Address: 0x071C

Hardware Function: 0x0
Device Address: 0x071C
Read/Write: Read and Write

The ADC Data FIFO Full register is used to read the Full status of the FIFOs. These will most likely be used for debug only as the FIFOs are continuously filled and emptied.

Table 6.89: ADC Data FIFO Full Register

BIT	NAME	RESET
31:18	RSVD	0
17:0	MUX_FIFO_FULL	0

6.2.7 Base Address: 0x0800, AsAP Control Registers

6.2.7.1 AsAP #0 Read Data Register, Address: 0x0800

Hardware Function: 0x0
Device Address: 0x0800
Read/Write: Read Only

The AsAP #0 Read Data register is used to store the data read from AsAP #0.

Table 6.90: AsAP #0 Read Data Register

BIT	NAME	RESET
31:16	RSVD	0
15:0	ASAP0_RD_DATA[15:0]	0

6.2.7.2 AsAP #1 Read Data Register, Address: 0x0802

Hardware Function: 0x0
Device Address: 0x0802
Read/Write: Read Only

The AsAP #1 Read Data register is used to store the data read from AsAP #1.

Table 6.91: AsAP #1 Read Data Register

BIT	NAME	RESET
31:16	RSVD	0
15:0	ASAP1_RD_DATA[15:0]	0

6.2.7.3 AsAP #0 Control Register, Address: 0x0804

Hardware Function: 0x0
Device Address: 0x0804
Read/Write: Read Only

The AsAP #0 Control register is used to control AsAP #0.

Table 6.92: AsAP #0 Control Register

BIT	NAME	RESET
31:1	RSVD	0
0	ASAP0_CTRL	0

6.2.7.4 AsAP #1 Control Register, Address: 0x0806

Hardware Function: 0x0
Device Address: 0x0806
Read/Write: Read Only

The AsAP #1 Control register is used to control AsAP #1.

Table 6.93: AsAP #1 Control Register

BIT	NAME	RESET
31:1	RSVD	0
0	ASAP1_CTRL	0

7 Data Path FPGA Pinout

The Measurement board contains an Xilinx Virtex-5 SX50T FPGA for controlling the high-speed circuitry. The Xilinx part number is: XC5VSX50T-3FFG1136C.

Table 7.1: Virtex-5 SX50T (XC5VSX50T-3FFG1136C) FPGA Pin Out

Virtex-5 SX50T (XC5VSX50T-3FFG1136C) FPGA Pin Out			
Signal Name	**Bank**	**Pin**	**Description**
Bank 0: 27 Pins			
Bank Voltage: +3.3V			
P3V3D_V5	0	AA22	VCCO_0
P3V3D_V5	0	AD23	VCCO_0
No Connect	0	W18	DXP_0
No Connect	0	W17	DXN_0
P2V5REF_FPGA	0	T18	AVDD_0
GNDA_FPGA	0	T17	AVSS_0
VP_VN_SM	0	U18	VP_0
VP_VN_SM	0	V17	VN_0
P2V5REF_FPGA	0	V18	VREFP_0
GNDA_FPGA	0	U17	VREFN_0
P3V3D_V5	0	L23	VBATT_0
V5_PROG_B	0	M22	PROGRAM_B_0
VS_HSWAPEN	0	M23	HSWAPEN_0
S3A_SPI_DATA_TO_V5	0	P15	D_IN_0
V5_CONFIG_DONE	0	M15	DONE_0
V5_CCLK	0	N15	CCLK_0
V5_INIT_B	0	N14	INIT_B_0
FPGA_CS_B	0	N22	CS_B_0
FPGA_RDWR_B	0	N23	RDWR_B_0
GND	0	AB23	RSVD_D0
GND	0	AC23	RSVD_D1
TCK	0	AB15	TCK_0
V5_M[0]	0	AD21	M0_0
V5_M[2]	0	AD22	M2_0
V5_M[1]	0	AC22	M1_0
TMS	0	AC14	TMS_0
TDI_TO_V5	0	AC15	TDI_0
No Connect	0	AD15	D_OUT_BUSY_0
TDO_TO_JTAG	0	AD14	TDO_0
Bank 1: 20 Pins			
Bank Voltage: +3.3V			
P3V3D_V5	1	D13	VCCO_1
P3V3D_V5	1	G14	VCCO_1
FPGA_V5_FTDI_DATA[6]	1	G22	IO_L4P_A11_D27_1
FPGA_DP_CTRL_RNW	1	G23	IO_L8P_CC_A3_D19_1
FPGA_DP_CTRL_DATA_CSN	1	H12	IO_L7N_A4_D20_1
FPGA_V5_FTDI_DATA[5]	1	H22	IO_L4N_VREF_A10_D26_1
FPGA_DP_CTRL_GPIO[2]	1	H23	IO_L8N_CC_A2_D18_1
			Continued on Next Page...

Virtex-5 SX50T (XC5VSX50T-3FFG1136C) FPGA Pin Out			
Signal Name	**Bank**	**Pin**	**Description**
FPGA_V5_FTDI_DATA[0]	1	J12	IO_L7P_A5_D21_1
FPGA_V5_FTDI_DATA[7]	1	J15	IO_L3N_A12_D28_1
FPGA_V5_FTDI_RDN	1	J22	IO_L2P_A15_D31_1
FPGA_DP_CTRL_GPIO[0]	1	K12	IO_L9N_CC_A0_D16_1
FPGA_DP_CTRL_GPIO[1]	1	K13	IO_L9P_CC_A1_D17_1
FPGA_V5_FTDI_DATA[3]	1	K14	IO_L5N_A8_D24_1
FPGA_V5_FTDI_SI_WU	1	K16	IO_L3P_A13_D29_1
FPGA_V5_FTDI_WRN	1	K21	IO_L2N_A14_D30_1
FPGA_V5_FTDI_DATA[1]	1	K22	IO_L6N_A6_D22_1
FPGA_V5_FTDI_DATA[2]	1	K23	IO_L6P_A7_D23_1
FPGA_V5_FTDI_DATA[4]	1	L14	IO_L5P_A9_D25_1
FPGA_V5_FTDI_PWRENN	1	L15	IO_L1P_A17_1
FPGA_V5_FTDI_RSTOUTN	1	L16	IO_L1N_A16_1
FPGA_V5_FTDI_RXFN	1	L20	IO_L0N_A18_1
FPGA_V5_FTDI_TXEN	1	L21	IO_L0P_A19_1
Bank 2: 20 Pins			
Bank Voltage: +3.3V			
P3V3D_V5	2	AH21	VCCO_2
P3V3D_V5	2	AM19	VCCO_2
FPGA_LA_DATA[7]	2	AE12	IO_L0N_CC_RS0_2
FPGA_LA_CLK	2	AE13	IO_L0P_CC_RS1_2
FPGA_LA_DATA[0]	2	AE14	IO_L4P_FCS_B_2
No Connect	2	AE16	IO_L6N_D6_2
V5_FS2	2	AE17	IO_L8N_D2_FS2_2
V5_FS1	2	AE19	IO_L9P_D1_FS1_2
V5_FS0	2	AD19	IO_L9N_D0_FS0_2
FPGA_V5_PUSHBUTTON[0]	2	AD20	IO_L7N_D4_2
FPGA_V5_PUSHBUTTON[1]	2	AE21	IO_L7P_D5_2
FPGA_LA_DATA[2]	2	AE22	IO_L3P_A21_2
FPGA_LA_DATA[1]	2	AE23	IO_L3N_A20_2
FPGA_LA_DATA[4]	2	AF13	IO_L2P_A23_2
No Connect	2	AF14	IO_L4N_VREF_FOE_B_MOSI_2
No Connect	2	AF15	IO_L6P_D7_2
No Connect	2	AF16	IO_L8P_D3_2
No Connect	2	AF20	IO_L5P_FWE_B_2
No Connect	2	AF21	IO_L5N_CSO_B_2
FPGA_LA_DATA[6]	2	AF23	IO_L1P_CC_A25_2
FPGA_LA_DATA[3]	2	AG12	IO_L2N_A22_2
FPGA_LA_DATA[5]	2	AG23	IO_L1N_CC_A24_2
Bank 3: 20 Pins			
Bank Voltage: +3.3V			
P3V3D_V5	3	D23	VCCO_3
P3V3D_V5	3	E20	VCCO_3
FPGA_BANK3_VRN	3	G15	IO_L2P_GC_VRN_3
FPGA_BANK3_VRP	3	G16	IO_L2N_GC_VRP_3
FPGA_V5_SD_BUSY_LED	3	H13	IO_L8N_GC_3
FPGA_DP_CTRL_SCK	3	H14	IO_L6P_GC_3
FPGA_V5_SD_RXD	3	H15	IO_L6N_GC_3
FPGA_V5_RS232_RTS	3	H17	IO_L0P_CC_GC_3
FPGA_V5_RS232_RX	3	H18	IO_L0N_CC_GC_3
			Continued on Next Page...

Virtex-5 SX50T (XC5VSX50T-3FFG1136C) FPGA Pin Out			
Signal Name	**Bank**	**Pin**	**Description**
No Connect	3	H19	IO_L9P_GC_3
No Connect	3	H20	IO_L9N_GC_3
FPGA_V5_SD_CARD_DETECT	3	J14	IO_L8P_GC_3
FPGA_DP_CTRL_MOSI	3	J16	IO_L4P_GC_3
FPGA_DP_CTRL_SRQN	3	J17	IO_L4N_GC_VREF_3
FPGA_DP_CTRL_MISO	3	J19	IO_L3N_GC_3
FPGA_V5_SD_TXD	3	J20	IO_L7P_GC_3
FPGA_V5_SD_CLK	3	J21	IO_L7N_GC_3
FPGA_V5_RS232_TX	3	K17	IO_L1P_CC_GC_3
FPGA_DP_CTRL_ADDR_CSN	3	K18	IO_L3P_GC_3
FPGA_BOARD_RSTN	3	K19	IO_L5N_GC_3
FPGA_V5_RS232_CTS	3	L18	IO_L1N_CC_GC_3
FPGA_DP_CTRL_RSTN	3	L19	IO_L5P_GC_3
Bank 4: 20 Pins			
Bank Voltage: +2.5V			
P2V5D_V5	4	AG14	VCCO_4
P2V5D_V5	4	AL12	VCCO_4
FPGA_TRIG_OUT_N	4	AE18	IO_L8N_CC_GC_4
FPGA_TRIG_OUT_P	4	AF18	IO_L8P_CC_GC_4
FPGA_DEBUG_LEDS[0]	4	AF19	IO_L6N_GC_4
FPGA_DSP_CLKIN_N	4	AG13	IO_L1N_GC_D12_4
FPGA_DEBUG_LEDS[2]	4	AG15	IO_L5N_GC_4
FPGA_TRIG_IN_N	4	AG16	IO_L7N_GC_VRP_4
FPGA_AUX_IN_N	4	AG17	IO_L9N_CC_GC_4
FPGA_DEBUG_LEDS[1]	4	AG18	IO_L6P_GC_4
FPGA_CLK100MHZ_N	4	AG20	IO_L4N_GC_VREF_4
FPGA_CLK100MHZ_P	4	AG21	IO_L4P_GC_4
FPGA_ASAP_CLKIN_P	4	AG22	IO_L0P_GC_D15_4
FPGA_DSP_CLKIN_P	4	AH12	IO_L1P_GC_D13_4
FPGA_SDRAM_CLK_N	4	AH13	IO_L3N_GC_D8_4
FPGA_SDRAM_CLK_P	4	AH14	IO_L3P_GC_D9_4
FPGA_DEBUG_LEDS[3]	4	AH15	IO_L5P_GC_4
FPGA_TRIG_IN_P	4	AH17	IO_L7P_GC_VRN_4
FPGA_AUX_IN_P	4	AH18	IO_L9P_CC_GC_4
FPGA_SRAM_CLK_N	4	AH19	IO_L2N_GC_D10_4
FPGA_SRAM_CLK_P	4	AH20	IO_L2P_GC_D11_4
FPGA_ASAP_CLKIN_N	4	AH22	IO_L0N_GC_D14_4
Bank 5: 40 Pins			
Bank Voltage: +3.3V			
P3V3D_V5	5	B19	VCCO_5
P3V3D_V5	5	C16	VCCO_5
P3V3D_V5	5	F17	VCCO_5
NOPAD			
Bank 6: 40 Pins			
Bank Voltage: +2.5V			
P3V3D_V5	6	AJ18	VCCO_6
P3V3D_V5	6	AK15	VCCO_6
P3V3D_V5	6	AN16	VCCO_6
NOPAD			
Continued on Next Page...			

Virtex-5 SX50T (XC5VSX50T-3FFG1136C) FPGA Pin Out			
Signal Name	**Bank**	**Pin**	**Description**
Bank 11: 40 Pins			
Bank Voltage: +1.8V			
P1V8D_V5	11	R30	VCCO_11
P1V8D_V5	11	T27	VCCO_11
P1V8D_V5	11	V31	VCCO_11
FPGA_DDR2_SDRAM_DQ[55]	11	A33	IO_L0N_11
FPGA_DDR2_SDRAM_DQ[50]	11	B32	IO_L0P_11
FPGA_DDR2_SDRAM_DQS[6]	11	B33	IO_L1P_11
FPGA_DDR2_SDRAM_DQ[54]	11	C32	IO_L2P_11
FPGA_DDR2_SDRAM_DQSN_NC[6]	11	C33	IO_L1N_11
FPGA_DDR2_SDRAM_DQ[51]	11	C34	IO_L3P_11
FPGA_DDR2_SDRAM_DQ[49]	11	D32	IO_L2N_11
FPGA_DDR2_SDRAM_DM[6]	11	D34	IO_L3N_11
FPGA_DDR2_SDRAM_DQ[58]	11	E32	IO_L6P_11
FPGA_DDR2_SDRAM_DQ[59]	11	E33	IO_L6N_11
FPGA_DDR2_SDRAM_DQ[63]	11	E34	IO_L5N_11
FPGA_DDR2_SDRAM_DM[7]	11	F33	IO_L5P_11
FPGA_DDR2_SDRAM_DQ[62]	11	F34	IO_L7N_11
FPGA_DDR2_SDRAM_DQ[53]	11	G32	IO_L4P_11
FPGA_DDR2_SDRAM_DQ[57]	11	G33	IO_L7P_11
P0V9D_MEM_VREF	11	H32	IO_L4N_VREF_11
FPGA_DDR2_SDRAM_DQ[52]	11	H33	IO_L8N_CC_11
FPGA_DDR2_SDRAM_DQS[7]	11	H34	IO_L9P_CC_11
FPGA_DDR2_SDRAM_DQ[48]	11	J32	IO_L8P_CC_11
FPGA_DDR2_SDRAM_DQSN_NC[7]	11	J34	IO_L9N_CC_11
FPGA_DDR2_SDRAM_A[6]	11	K32	IO_L11N_CC_SM14N_11
FPGA_DDR2_SDRAM_A[2]	11	K33	IO_L11P_CC_SM14P_11
FPGA_DDR2_SDRAM_A[1]	11	K34	IO_L10N_CC_SM15N_11
FPGA_DDR2_SDRAM_DQ[61]	11	L33	IO_L13P_11
FPGA_DDR2_SDRAM_A[4]	11	L34	IO_L10P_CC_SM15P_11
FPGA_DDR2_SDRAM_DQ[60]	11	M32	IO_L13N_11
FPGA_BANK11_VRP	11	M33	IO_L12N_VRP_11
FPGA_DDR2_SDRAM_A[7]	11	N32	IO_L15N_SM13N_11
FPGA_BANK11_VRN	11	N33	IO_L12P_VRN_11
P0V9D_MEM_VREF	11	N34	IO_L14N_VREF_11
FPGA_DDR2_SDRAM_A[11]	11	P32	IO_L15P_SM13P_11
FPGA_DDR2_SDRAM_DQ[56]	11	P34	IO_L14P_11
FPGA_DDR2_SDRAM_A[9]	11	R32	IO_L17N_SM11N_11
FPGA_DDR2_SDRAM_A[3]	11	R33	IO_L17P_SM11P_11
FPGA_DDR2_SDRAM_A[0]	11	R34	IO_L16N_SM12N_11
FPGA_DDR2_SDRAM_A[8]	11	T33	IO_L16P_SM12P_11
FPGA_DDR2_SDRAM_A[5]	11	T34	IO_L18N_SM10N_11
FPGA_DDR2_SDRAM_BA[1]	11	U31	IO_L19N_SM9N_11
FPGA_DDR2_SDRAM_BA[2]	11	U32	IO_L19P_SM9P_11
FPGA_DDR2_SDRAM_A[12]	11	U33	IO_L18P_SM10P_11
Bank 12: 40 Pins			
Bank Voltage: +2.5V			
P2V5D_V5	12	M9	VCCO_12
P2V5D_V5	12	N6	VCCO_12
P2V5D_V5	12	T7	VCCO_12
			Continued on Next Page...

Virtex-5 SX50T (XC5VSX50T-3FFG1136C) FPGA Pin Out			
Signal Name	**Bank**	**Pin**	**Description**
FPGA_ASAP1_DATA_OUT[1]	12	E6	IO_L19P_12
FPGA_ASAP1_DATA_OUT[0]	12	E7	IO_L19N_12
FPGA_ASAP1_DATA_OUT[9]	12	F5	IO_L15P_12
FPGA_ASAP1_DATA_OUT[8]	12	F6	IO_L15N_12
FPGA_ASAP1_DATA_OUT[12]	12	G5	IO_L13N_12
FPGA_ASAP1_DATA_OUT[5]	12	G6	IO_L17P_12
FPGA_ASAP1_DATA_OUT[4]	12	G7	IO_L17N_12
FPGA_ASAP1_DATA_OUT[13]	12	H5	IO_L13P_12
FPGA_ASAP1_DATA_OUT[15]	12	H7	IO_L11P_CC_12
FPGA_ASAP1_REQ_IN	12	J5	IO_L8N_CC_12
FPGA_ASAP1_CLK_IN	12	J6	IO_L8P_CC_12
FPGA_ASAP1_DATA_OUT[14]	12	J7	IO_L11N_CC_12
FPGA_ASAP1_DATA_IN[2]	12	K6	IO_L6N_12
FPGA_ASAP1_DATA_IN[3]	12	K7	IO_L6P_12
FPGA_ASAP1_DATA_IN[7]	12	L4	IO_L4P_12
FPGA_ASAP1_DATA_IN[6]	12	L5	IO_L4N_VREF_12
FPGA_ASAP1_DATA_IN[10]	12	L6	IO_L2N_12
FPGA_ASAP1_DATA_IN[14]	12	M5	IO_L0N_12
FPGA_ASAP1_DATA_IN[15]	12	M6	IO_L0P_12
FPGA_ASAP1_DATA_IN[11]	12	M7	IO_L2P_12
FPGA_ASAP1_DATA_IN[9]	12	N5	IO_L3P_12
FPGA_ASAP1_DATA_IN[12]	12	N7	IO_L1N_12
FPGA_ASAP1_DATA_IN[13]	12	N8	IO_L1P_12
FPGA_ASAP1_DATA_IN[8]	12	P5	IO_L3N_12
FPGA_ASAP1_DATA_IN[4]	12	P6	IO_L5N_12
FPGA_ASAP1_DATA_IN[5]	12	P7	IO_L5P_12
FPGA_BANK12_VRP	12	P9	IO_L12N_VRP_12
FPGA_ASAP1_DATA_OUT[10]	12	P10	IO_L14N_VREF_12
FPGA_ASAP1_DATA_IN[1]	12	R6	IO_L7P_12
FPGA_ASAP1_VLD_IN	12	R7	IO_L9P_CC_12
FPGA_ASAP1_REQ_OUT	12	R8	IO_L9N_CC_12
FPGA_BANK12_VRN	12	R9	IO_L12P_VRN_12
FPGA_ASAP1_DATA_OUT[11]	12	R11	IO_L14P_12
FPGA_ASAP1_DATA_IN[0]	12	T6	IO_L7N_12
FPGA_ASAP1_CLK_OUT	12	T8	IO_L10P_CC_12
FPGA_ASAP1_DATA_OUT[3]	12	T9	IO_L18P_12
FPGA_ASAP1_DATA_OUT[7]	12	T10	IO_L16P_12
FPGA_ASAP1_DATA_OUT[6]	12	T11	IO_L16N_12
FPGA_ASAP1_VLD_OUT	12	U7	IO_L10N_CC_12
FPGA_ASAP1_DATA_OUT[2]	12	U10	IO_L18N_12
Bank 13: 40 Pins			
Bank Voltage: +1.8V			
P1V8D_V5	13	AA32	VCCO_13
P1V8D_V5	13	AB29	VCCO_13
P1V8D_V5	13	W28	VCCO_13
FPGA_QDRII_SRAM_RDATA[12]	13	AA33	IO_L2N_SM6N_13
FPGA_QDRII_SRAM_RDATA[4]	13	AA34	IO_L3P_SM5P_13
FPGA_QDRII_SRAM_RDATA[13]	13	AB32	IO_L6N_SM3N_13
FPGA_QDRII_SRAM_RDATA[5]	13	AB33	IO_L7N_SM2N_13
FPGA_QDRII_SRAM_RDATA[7]	13	AC32	IO_L6P_SM3P_13
			Continued on Next Page...

Virtex-5 SX50T (XC5VSX50T-3FFG1136C) FPGA Pin Out			
Signal Name	**Bank**	**Pin**	**Description**
FPGA_QDRII_SRAM_RDATA[15]	13	AC33	IO_L7P_SM2P_13
FPGA_QDRII_SRAM_RDATA[14]	13	AC34	IO_L5P_SM4P_13
FPGA_QDRII_SRAM_RDATA[26]	13	AD32	IO_L11P_CC_13
FPGA_QDRII_SRAM_RDATA[6]	13	AD34	IO_L5N_SM4N_13
FPGA_QDRII_SRAM_RDATA[35]	13	AE32	IO_L11N_CC_13
FPGA_QDRII_SRAM_RDATA[8]	13	AE33	IO_L8N_CC_SM1N_13
FPGA_QDRII_SRAM_RDATA[16]	13	AE34	IO_L9N_CC_SM0N_13
FPGA_QDRII_SRAM_CQ_CLK_P	13	AF33	IO_L8P_CC_SM1P_13
FPGA_QDRII_SRAM_CQ_CLK_N	13	AF34	IO_L9P_CC_SM0P_13
FPGA_QDRII_SRAM_RDATA[25]	13	AG32	IO_L14P_13
FPGA_QDRII_SRAM_RDATA[34]	13	AG33	IO_L12P_VRN_13
P0V9D_MEM_VREF	13	AH32	IO_L14N_VREF_13
FPGA_QDRII_SRAM_RDATA[24]	13	AH33	IO_L12N_VRP_13
FPGA_QDRII_SRAM_RDATA[17]	13	AH34	IO_L10P_CC_13
FPGA_QDRII_SRAM_RDATA[33]	13	AJ32	IO_L15P_13
FPGA_QDRII_SRAM_RDATA[18]	13	AJ34	IO_L10N_CC_13
FPGA_QDRII_SRAM_RDATA[23]	13	AK32	IO_L15N_13
FPGA_QDRII_SRAM_RDATA[32]	13	AK33	IO_L13N_13
FPGA_QDRII_SRAM_RDATA[27]	13	AK34	IO_L13P_13
FPGA_QDRII_SRAM_RDATA[31]	13	AL33	IO_L16N_13
FPGA_QDRII_SRAM_RDATA[28]	13	AL34	IO_L16P_13
FPGA_QDRII_SRAM_RDATA[22]	13	AM32	IO_L17N_13
FPGA_QDRII_SRAM_RDATA[20]	13	AM33	IO_L17P_13
FPGA_QDRII_SRAM_RDATA[21]	13	AN32	IO_L19P_13
FPGA_QDRII_SRAM_RDATA[29]	13	AN33	IO_L18N_13
FPGA_QDRII_SRAM_RDATA[19]	13	AN34	IO_L18P_13
FPGA_QDRII_SRAM_RDATA[30]	13	AP32	IO_L19N_13
FPGA_QDRII_SRAM_RDATA[9]	13	V32	IO_L0P_SM8P_13
FPGA_QDRII_SRAM_RDATA[0]	13	V33	IO_L0N_SM8N_13
FPGA_QDRII_SRAM_RDATA[10]	13	V34	IO_L1N_SM7N_13
P0V9D_MEM_VREF	13	W32	IO_L4N_VREF_13
FPGA_QDRII_SRAM_RDATA[11]	13	W34	IO_L1P_SM7P_13
FPGA_QDRII_SRAM_RDATA[1]	13	Y32	IO_L4P_13
FPGA_QDRII_SRAM_RDATA[2]	13	Y33	IO_L2P_SM6P_13
FPGA_QDRII_SRAM_RDATA[3]	13	Y34	IO_L3N_SM5N_13
Bank 15: 40 Pins			
Bank Voltage: +1.8V			
P1V8D_V5	15	L32	VCCO_15
P1V8D_V5	15	M29	VCCO_15
P1V8D_V5	15	P33	VCCO_15
FPGA_DDR2_SDRAM_DQ[27]	15	E29	IO_L0P_15
FPGA_DDR2_SDRAM_DQ[31]	15	E31	IO_L3N_15
FPGA_DDR2_SDRAM_DQ[24]	15	F29	IO_L0N_15
FPGA_DDR2_SDRAM_DM[3]	15	F30	IO_L1N_15
FPGA_DDR2_SDRAM_DQ[25]	15	F31	IO_L3P_15
FPGA_DDR2_SDRAM_DQ[26]	15	G30	IO_L1P_15
FPGA_DDR2_SDRAM_DQSN_NC[4]	15	G31	IO_L5N_15
FPGA_DDR2_SDRAM_DQ[30]	15	H29	IO_L2P_15
FPGA_DDR2_SDRAM_DQS[4]	15	H30	IO_L5P_15
FPGA_DDR2_SDRAM_DQ[29]	15	J29	IO_L2N_15
			Continued on Next Page...

Virtex-5 SX50T (XC5VSX50T-3FFG1136C) FPGA Pin Out			
Signal Name	**Bank**	**Pin**	**Description**
FPGA_DDR2_SDRAM_DM[4]	15	J30	IO_L6P_15
FPGA_DDR2_SDRAM_DQ[36]	15	J31	IO_L6N_15
P0V9D_MEM_VREF	15	K29	IO_L4N_VREF_15
FPGA_DDR2_SDRAM_DQ[33]	15	K31	IO_L9P_CC_15
FPGA_DDR2_SDRAM_DQ[28]	15	L29	IO_L4P_15
FPGA_DDR2_SDRAM_DQ[34]	15	L30	IO_L7P_15
FPGA_DDR2_SDRAM_DQ[37]	15	L31	IO_L9N_CC_15
FPGA_DDR2_SDRAM_DQ[38]	15	M30	IO_L7N_15
FPGA_DDR2_SDRAM_CK_P[1]	15	M31	IO_L11P_CC_15
FPGA_DDR2_SDRAM_DQS[3]	15	N29	IO_L8P_CC_15
FPGA_DDR2_SDRAM_CK_N[1]	15	N30	IO_L11N_CC_15
FPGA_DDR2_SDRAM_DQSN_NC[3]	15	P29	IO_L8N_CC_15
FPGA_DDR2_SDRAM_DQ[44]	15	P30	IO_L10N_CC_15
FPGA_DDR2_SDRAM_DQ[45]	15	P31	IO_L10P_CC_15
FPGA_DDR2_SDRAM_DQ[46]	15	R26	IO_L17P_15
FPGA_DDR2_SDRAM_DQ[47]	15	R27	IO_L17N_15
FPGA_BANK15_VRN	15	R28	IO_L12P_VRN_15
FPGA_BANK15_VRP	15	R29	IO_L12N_VRP_15
FPGA_DDR2_SDRAM_DQ[32]	15	R31	IO_L13N_15
FPGA_DDR2_SDRAM_A[10]	15	T25	IO_L19N_15
FPGA_DDR2_SDRAM_DQ[43]	15	T26	IO_L18N_15
FPGA_DDR2_SDRAM_DM[5]	15	T28	IO_L15P_15
FPGA_DDR2_SDRAM_DQ[41]	15	T29	IO_L15N_15
P0V9D_MEM_VREF	15	T30	IO_L14N_VREF_15
FPGA_DDR2_SDRAM_DQ[39]	15	T31	IO_L13P_15
FPGA_DDR2_SDRAM_DQ[40]	15	U25	IO_L19P_15
FPGA_DDR2_SDRAM_DQ[42]	15	U26	IO_L18P_15
FPGA_DDR2_SDRAM_DQS[5]	15	U27	IO_L16P_15
FPGA_DDR2_SDRAM_DQSN_NC[5]	15	U28	IO_L16N_15
FPGA_DDR2_SDRAM_DQ[35]	15	U30	IO_L14P_15
Bank 17: 40 Pins			
Bank Voltage: +1.8V			
P1V8D_V5	17	AD33	VCCO_17
P1V8D_V5	17	AE30	VCCO_17
P1V8D_V5	17	AH31	VCCO_17
FPGA_QDRII_SRAM_WDATA[26]	17	AA29	IO_L11P_CC_17
FPGA_QDRII_SRAM_WDATA[18]	17	AA30	IO_L11N_CC_17
FPGA_QDRII_SRAM_WDATA[8]	17	AA31	IO_L9N_CC_17
FPGA_QDRII_SRAM_BWN[1]	17	AB30	IO_L10P_CC_17
FPGA_QDRII_SRAM_WDATA[16]	17	AB31	IO_L9P_CC_17
FPGA_QDRII_SRAM_WDATA[25]	17	AC29	IO_L13N_17
FPGA_QDRII_SRAM_WDATA[34]	17	AC30	IO_L10N_CC_17
FPGA_QDRII_SRAM_BWN[2]	17	AD29	IO_L15N_17
FPGA_QDRII_SRAM_WDATA[33]	17	AD30	IO_L13P_17
FPGA_QDRII_SRAM_WDATA[24]	17	AD31	IO_L12P_VRN_17
FPGA_QDRII_SRAM_WDATA[32]	17	AE29	IO_L15P_17
FPGA_QDRII_SRAM_WDATA[23]	17	AE31	IO_L12N_VRP_17
FPGA_QDRII_SRAM_WDATA[31]	17	AF29	IO_L17P_17
FPGA_QDRII_SRAM_WDATA[30]	17	AF30	IO_L17N_17
FPGA_QDRII_SRAM_WDATA[19]	17	AF31	IO_L14P_17
			Continued on Next Page...

Virtex-5 SX50T (XC5VSX50T-3FFG1136C) FPGA Pin Out			
Signal Name	**Bank**	**Pin**	**Description**
FPGA_QDRII_SRAM_WDATA[27]	17	AG30	IO_L19N_17
P0V9D_MEM_VREF	17	AG31	IO_L14N_VREF_17
FPGA_QDRII_SRAM_WDATA[22]	17	AH29	IO_L19P_17
FPGA_QDRII_SRAM_WDATA[21]	17	AH30	IO_L18N_17
FPGA_QDRII_SRAM_WDATA[29]	17	AJ30	IO_L18P_17
FPGA_QDRII_SRAM_WDATA[20]	17	AJ31	IO_L16P_17
FPGA_QDRII_SRAM_WDATA[28]	17	AK31	IO_L16N_17
FPGA_QDRII_SRAM_WDATA[13]	17	V24	IO_L0N_17
FPGA_QDRII_SRAM_WDATA[12]	17	V25	IO_L2P_17
FPGA_QDRII_SRAM_WDATA[9]	17	V27	IO_L5N_17
FPGA_QDRII_SRAM_BWN[0]	17	V28	IO_L5P_17
FPGA_QDRII_SRAM_WDATA[0]	17	V29	IO_L7N_17
FPGA_QDRII_SRAM_WDATA[14]	17	V30	IO_L4P_17
FPGA_QDRII_SRAM_WDATA[5]	17	W24	IO_L0P_17
FPGA_QDRII_SRAM_WDATA[4]	17	W25	IO_L2N_17
FPGA_QDRII_SRAM_WDATA[11]	17	W26	IO_L1N_17
FPGA_QDRII_SRAM_WDATA[10]	17	W27	IO_L3N_17
FPGA_QDRII_SRAM_WDATA[1]	17	W29	IO_L7P_17
P0V9D_MEM_VREF	17	W30	IO_L4N_VREF_17
FPGA_QDRII_SRAM_WDATA[6]	17	W31	IO_L6P_17
FPGA_QDRII_SRAM_WDATA[3]	17	Y26	IO_L1P_17
FPGA_QDRII_SRAM_WDATA[2]	17	Y27	IO_L3P_17
FPGA_QDRII_SRAM_WDATA[7]	17	Y28	IO_L8P_CC_17
FPGA_QDRII_SRAM_WDATA[17]	17	Y29	IO_L8N_CC_17
FPGA_QDRII_SRAM_WDATA[15]	17	Y31	IO_L6N_17
Bank 18: 40 Pins			
Bank Voltage: +2.5V			
P2V5D_V5	18	AB9	VCCO_18
P2V5D_V5	18	AC6	VCCO_18
P2V5D_V5	18	W8	VCCO_18
FPGA_DAC_DATA_P[13]	18	AA5	IO_L2P_18
FPGA_DAC_DATA_P[9]	18	AA6	IO_L6P_18
FPGA_DAC_DATA_N[13]	18	AB5	IO_L2N_18
FPGA_DAC_DATA_P[14]	18	AB6	IO_L1P_18
FPGA_DAC_DATA_N[14]	18	AB7	IO_L1N_18
FPGA_DAC_DATA_P[15]	18	AC4	IO_L0P_18
FPGA_DAC_DATA_N[15]	18	AC5	IO_L0N_18
FPGA_DAC_DATA_P[12]	18	AC7	IO_L3P_18
FPGA_DAC_DATA_P[10]	18	AD4	IO_L5P_18
FPGA_DAC_DATA_N[10]	18	AD5	IO_L5N_18
FPGA_DAC_DATA_P[8]	18	AD6	IO_L7P_18
FPGA_DAC_DATA_N[12]	18	AD7	IO_L3N_18
FPGA_DAC_DATA_N[8]	18	AE6	IO_L7N_18
FPGA_DAC_DATA_P[6]	18	AE7	IO_L9P_CC_18
FPGA_DAC_DATA_N[5]	18	AF5	IO_L10N_CC_18
FPGA_DAC_DATA_N[6]	18	AF6	IO_L9N_CC_18
FPGA_DAC_DATA_P[5]	18	AG5	IO_L10P_CC_18
FPGA_DAC_DATA_N[3]	18	AG6	IO_L12N_VRP_18
FPGA_DAC_DATA_N[1]	18	AG7	IO_L14N_VREF_18
FPGA_DAC_DATA_P[3]	18	AH5	IO_L12P_VRN_18
			Continued on Next Page...

Virtex-5 SX50T (XC5VSX50T-3FFG1136C) FPGA Pin Out			
Signal Name	**Bank**	**Pin**	**Description**
FPGA_DAC_DATA_P[1]	18	AH7	IO_L14P_18
FPGA_DAC_CLK_IN_N	18	AJ6	IO_L16N_18
FPGA_DAC_CLK_IN_P	18	AJ7	IO_L16P_18
No Connect	18	AK6	IO_L18N_18
No Connect	18	AK7	IO_L18P_18
FPGA_DAC_SYNC_N	18	U8	IO_L17N_18
FPGA_DAC_DATA_N[4]	18	V7	IO_L11N_CC_18
FPGA_DAC_SYNC_P	18	V8	IO_L17P_18
No Connect	18	V9	IO_L19N_18
No Connect	18	V10	IO_L19P_18
FPGA_DAC_DATA_P[7]	18	W6	IO_L8P_CC_18
FPGA_DAC_DATA_P[4]	18	W7	IO_L11P_CC_18
FPGA_DAC_DATA_N[0]	18	W9	IO_L15N_18
FPGA_DAC_DATA_P[0]	18	W10	IO_L15P_18
FPGA_DAC_DATA_N[2]	18	W11	IO_L13N_18
FPGA_DAC_DATA_N[7]	18	Y6	IO_L8N_CC_18
FPGA_DAC_DATA_N[9]	18	Y7	IO_L6N_18
FPGA_DAC_DATA_P[11]	18	Y8	IO_L4P_18
FPGA_DAC_DATA_N[11]	18	Y9	IO_L4N_VREF_18
FPGA_DAC_DATA_P[2]	18	Y11	IO_L13P_18
Bank 19: 40 Pins			
Bank Voltage: +1.8V			
P1V8D_V5	19	E30	VCCO_19
P1V8D_V5	19	H31	VCCO_19
P1V8D_V5	19	J28	VCCO_19
FPGA_DDR2_SDRAM_CK_P[0]	19	E26	IO_L11P_CC_19
FPGA_DDR2_SDRAM_CK_N[0]	19	E27	IO_L11N_CC_19
FPGA_DDR2_SDRAM_DQS[2]	19	E28	IO_L10P_CC_19
FPGA_DDR2_SDRAM_DQ[8]	19	F25	IO_L7P_19
FPGA_DDR2_SDRAM_DM[1]	19	F26	IO_L7N_19
FPGA_DDR2_SDRAM_DQSN_NC[2]	19	F28	IO_L10N_CC_19
FPGA_DDR2_SDRAM_DQ[14]	19	G25	IO_L5P_19
FPGA_DDR2_SDRAM_DQ[10]	19	G26	IO_L5N_19
FPGA_DDR2_SDRAM_DQS[0]	19	G27	IO_L8P_CC_19
FPGA_DDR2_SDRAM_DQSN_NC[1]	19	G28	IO_L9N_CC_19
FPGA_DDR2_SDRAM_DQ[11]	19	H24	IO_L6N_19
FPGA_DDR2_SDRAM_DQ[15]	19	H25	IO_L6P_19
FPGA_DDR2_SDRAM_DQSN_NC[0]	19	H27	IO_L8N_CC_19
FPGA_DDR2_SDRAM_DQS[1]	19	H28	IO_L9P_CC_19
FPGA_DDR2_SDRAM_DM[0]	19	J24	IO_L2P_19
FPGA_DDR2_SDRAM_DQ[0]	19	J25	IO_L2N_19
P0V9D_MEM_VREF	19	J26	IO_L4N_VREF_19
FPGA_DDR2_SDRAM_DQ[4]	19	J27	IO_L4P_19
FPGA_DDR2_SDRAM_DQ[1]	19	K24	IO_L0P_19
P0V9D_MEM_VREF	19	K26	IO_L14N_VREF_19
FPGA_DDR2_SDRAM_DQ[13]	19	K27	IO_L14P_19
FPGA_DDR2_SDRAM_DQ[12]	19	K28	IO_L13P_19
FPGA_DDR2_SDRAM_DQ[7]	19	L24	IO_L0N_19
FPGA_DDR2_SDRAM_DQ[6]	19	L25	IO_L1P_19
FPGA_DDR2_SDRAM_DQ[2]	19	L26	IO_L1N_19
			Continued on Next Page...

Virtex-5 SX50T (XC5VSX50T-3FFG1136C) FPGA Pin Out			
Signal Name	**Bank**	**Pin**	**Description**
FPGA_DDR2_SDRAM_DQ[9]	19	L28	IO_L13N_19
FPGA_DDR2_SDRAM_DQ[3]	19	M25	IO_L3P_19
FPGA_DDR2_SDRAM_DQ[5]	19	M26	IO_L3N_19
FPGA_BANK19_VRP	19	M27	IO_L12N_VRP_19
FPGA_DDR2_SDRAM_DM[2]	19	M28	IO_L15P_19
FPGA_DDR2_SDRAM_DQ[21]	19	N24	IO_L17P_19
FPGA_DDR2_SDRAM_DQ[17]	19	N25	IO_L18N_19
FPGA_BANK19_VRN	19	N27	IO_L12P_VRN_19
FPGA_DDR2_SDRAM_DQ[22]	19	N28	IO_L15N_19
FPGA_DDR2_SDRAM_DQ[18]	19	P24	IO_L17N_19
FPGA_DDR2_SDRAM_DQ[20]	19	P25	IO_L18P_19
FPGA_DDR2_SDRAM_DQ[19]	19	P26	IO_L16P_19
FPGA_DDR2_SDRAM_DQ[23]	19	P27	IO_L16N_19
FPGA_DDR2_SDRAM_DQ[16]	19	R24	IO_L19P_19
FPGA_DDR2_SDRAM_A[13]	19	T24	IO_L19N_19
Bank 20: 40 Pins			
Bank Voltage: +2.5V			
P2V5D_V5	20	E10	VCCO_20
P2V5D_V5	20	H11	VCCO_20
P2V5D_V5	20	J8	VCCO_20
FPGA_ASAP2_CLK_IN	20	A13	IO_L8P_CC_20
FPGA_ASAP2_REQ_IN	20	B12	IO_L8N_CC_20
FPGA_ASAP2_DATA_OUT[15]	20	B13	IO_L11P_CC_20
FPGA_ASAP2_DATA_IN[2]	20	C12	IO_L6N_20
FPGA_ASAP2_DATA_OUT[14]	20	C13	IO_L11N_CC_20
FPGA_ASAP2_DATA_IN[6]	20	D10	IO_L4N_VREF_20
FPGA_ASAP2_DATA_IN[7]	20	D11	IO_L4P_20
FPGA_ASAP2_DATA_IN[3]	20	D12	IO_L6P_20
FPGA_ASAP2_DATA_IN[14]	20	E8	IO_L0N_20
FPGA_ASAP2_DATA_IN[15]	20	E9	IO_L0P_20
FPGA_ASAP2_DATA_OUT[8]	20	E11	IO_L15N_20
FPGA_ASAP2_DATA_OUT[5]	20	E12	IO_L17P_20
FPGA_ASAP2_DATA_OUT[4]	20	E13	IO_L17N_20
FPGA_ASAP2_DATA_IN[12]	20	F8	IO_L1N_20
FPGA_ASAP2_DATA_IN[13]	20	F9	IO_L1P_20
FPGA_ASAP2_DATA_IN[11]	20	F10	IO_L2P_20
FPGA_ASAP2_DATA_OUT[9]	20	F11	IO_L15P_20
FPGA_ASAP2_DATA_OUT[1]	20	F13	IO_L19P_20
FPGA_ASAP2_DATA_IN[9]	20	G8	IO_L3P_20
FPGA_ASAP2_DATA_IN[10]	20	G10	IO_L2N_20
FPGA_ASAP2_DATA_OUT[13]	20	G11	IO_L13P_20
FPGA_ASAP2_DATA_OUT[12]	20	G12	IO_L13N_20
FPGA_ASAP2_DATA_OUT[0]	20	G13	IO_L19N_20
FPGA_ASAP2_DATA_IN[8]	20	H8	IO_L3N_20
FPGA_ASAP2_DATA_IN[0]	20	H9	IO_L7N_20
FPGA_ASAP2_DATA_IN[1]	20	H10	IO_L7P_20
FPGA_ASAP2_REQ_OUT	20	J9	IO_L9N_CC_20
FPGA_ASAP2_VLD_IN	20	J10	IO_L9P_CC_20
FPGA_ASAP2_DATA_IN[4]	20	J11	IO_L5N_20
FPGA_ASAP2_CLK_OUT	20	K8	IO_L10P_CC_20
			Continued on Next Page...

Virtex-5 SX50T (XC5VSX50T-3FFG1136C) FPGA Pin Out			
Signal Name	**Bank**	**Pin**	**Description**
FPGA_ASAP2_VLD_OUT	20	K9	IO_L10N_CC_20
FPGA_ASAP2_DATA_IN[5]	20	K11	IO_L5P_20
FPGA_ASAP2_DATA_OUT[10]	20	L8	IO_L14N_VREF_20
FPGA_ASAP2_DATA_OUT[6]	20	L9	IO_L16N_20
FPGA_BANK20_VRN	20	L10	IO_L12P_VRN_20
FPGA_BANK20_VRP	20	L11	IO_L12N_VRP_20
FPGA_ASAP2_DATA_OUT[11]	20	M8	IO_L14P_20
FPGA_ASAP2_DATA_OUT[7]	20	M10	IO_L16P_20
FPGA_ASAP2_DATA_OUT[2]	20	N9	IO_L18N_20
FPGA_ASAP2_DATA_OUT[3]	20	N10	IO_L18P_20
Bank 21: 40 Pins			
Bank Voltage: +1.8V			
P1V8D_V5	21	AJ28	VCCO_21
P1V8D_V5	21	AL32	VCCO_21
P1V8D_V5	21	AM29	VCCO_21
FPGA_QDRII_SRAM_BWN[3]	21	AA24	IO_L2N_21
FPGA_QDRII_SRAM_K_CLK_P	21	AA25	IO_L0P_21
FPGA_QDRII_SRAM_K_CLK_N	21	AA26	IO_L0N_21
FPGA_QDRII_SRAM_ADDR[4]	21	AA28	IO_L5N_21
FPGA_QDRII_SRAM_ADDR[17]	21	AB25	IO_L3P_21
FPGA_QDRII_SRAM_ADDR[1]	21	AB26	IO_L3N_21
FPGA_QDRII_SRAM_DUMMY_IN	21	AB27	IO_L1P_21
FPGA_QDRII_SRAM_ADDR[2]	21	AB28	IO_L5P_21
FPGA_DDR2_SDRAM_SN[0]	21	AC24	IO_L17N_21
FPGA_DDR2_SDRAM_SN[1]	21	AC25	IO_L17P_21
FPGA_QDRII_SRAM_DLL_OFFN	21	AC27	IO_L1N_21
FPGA_QDRII_SRAM_ADDR[0]	21	AC28	IO_L4P_21
FPGA_DDR2_SDRAM_CKE[1]	21	AD24	IO_L19P_21
FPGA_DDR2_SDRAM_ODT[0]	21	AD25	IO_L18N_21
FPGA_DDR2_SDRAM_ODT[1]	21	AD26	IO_L18P_21
P0V9D_MEM_VREF	21	AD27	IO_L4N_VREF_21
FPGA_DDR2_SDRAM_CKE[0]	21	AE24	IO_L19N_21
FPGA_DDR2_SDRAM_WEN	21	AE26	IO_L16N_21
FPGA_DDR2_SDRAM_CASN	21	AE27	IO_L16P_21
FPGA_QDRII_SRAM_ADDR[3]	21	AE28	IO_L7P_21
FPGA_QDRII_SRAM_ADDR[11]	21	AF24	IO_L13P_21
FPGA_DDR2_SDRAM_BA[0]	21	AF25	IO_L15P_21
FPGA_DDR2_SDRAM_RASN	21	AF26	IO_L15N_21
FPGA_QDRII_SRAM_ADDR[16]	21	AF28	IO_L7N_21
FPGA_QDRII_SRAM_WRN	21	AG25	IO_L13N_21
P0V9D_MEM_VREF	21	AG26	IO_L14N_VREF_21
FPGA_QDRII_SRAM_RDN	21	AG27	IO_L14P_21
FPGA_QDRII_SRAM_ADDR[12]	21	AG28	IO_L6P_21
FPGA_BANK21_VRP	21	AH25	IO_L12N_VRP_21
FPGA_QDRII_SRAM_ADDR[10]	21	AH27	IO_L11P_CC_21
FPGA_QDRII_SRAM_ADDR[8]	21	AH28	IO_L6N_21
FPGA_BANK21_VRN	21	AJ25	IO_L12P_VRN_21
FPGA_QDRII_SRAM_ADDR[15]	21	AJ26	IO_L11N_CC_21
FPGA_QDRII_SRAM_ADDR[7]	21	AJ27	IO_L8N_CC_21
FPGA_QDRII_SRAM_ADDR[13]	21	AJ29	IO_L9N_CC_21
			Continued on Next Page...

Virtex-5 SX50T (XC5VSX50T-3FFG1136C) FPGA Pin Out			
Signal Name	**Bank**	**Pin**	**Description**
FPGA_QDRII_SRAM_ADDR[6]	21	AK26	IO_L8P_CC_21
FPGA_QDRII_SRAM_ADDR[9]	21	AK27	IO_L10N_CC_21
FPGA_QDRII_SRAM_ADDR[14]	21	AK28	IO_L10P_CC_21
FPGA_QDRII_SRAM_ADDR[5]	21	AK29	IO_L9P_CC_21
FPGA_QDRII_SRAM_WDATA[35]	21	Y24	IO_L2P_21
Bank 22: 40 Pins			
Bank Voltage: +2.5V			
P2V5D_V5	22	AF7	VCCO_22
P2V5D_V5	22	AH11	VCCO_22
P2V5D_V5	22	AJ8	VCCO_22
FPGA_ADC_DATA_P[12]	22	AA8	IO_L3P_22
FPGA_ADC_DATA_N[12]	22	AA9	IO_L3N_22
FPGA_ADC_DATA_N[14]	22	AA10	IO_L1N_22
FPGA_ADC_DATA_N[10]	22	AB8	IO_L5N_22
FPGA_ADC_DATA_P[14]	22	AB10	IO_L1P_22
FPGA_ADC_DATA_P[10]	22	AC8	IO_L5P_22
FPGA_ADC_DATA_N[8]	22	AC9	IO_L7N_22
FPGA_ADC_DATA_P[8]	22	AC10	IO_L7P_22
FPGA_ADC_DATA_N[7]	22	AD9	IO_L9N_CC_22
FPGA_ADC_DATA_P[6]	22	AD10	IO_L10P_CC_22
FPGA_ADC_DATA_N[6]	22	AD11	IO_L10N_CC_22
FPGA_ADC_DATA_P[7]	22	AE8	IO_L9P_CC_22
FPGA_ADC_DATA_N[4]	22	AE9	IO_L12N_VRP_22
FPGA_ADC_DATA_N[0]	22	AE11	IO_L16N_22
FPGA_ADC_DATA_P[4]	22	AF8	IO_L12P_VRN_22
FPGA_ADC_DATA_P[2]	22	AF9	IO_L14P_22
FPGA_ADC_DATA_N[2]	22	AF10	IO_L14N_VREF_22
FPGA_ADC_DATA_P[0]	22	AF11	IO_L16P_22
No Connect	22	AG8	IO_L18P_22
No Connect	22	AG10	IO_L19P_22
No Connect	22	AG11	IO_L19N_22
No Connect	22	AH8	IO_L18N_22
FPGA_ADC_OVR_P	22	AH9	IO_L17P_22
FPGA_ADC_OVR_N	22	AH10	IO_L17N_22
FPGA_ADC_DATA_P[1]	22	AJ9	IO_L15P_22
FPGA_ADC_DATA_N[1]	22	AJ10	IO_L15N_22
FPGA_ADC_DATA_N[5]	22	AJ11	IO_L11N_CC_22
FPGA_ADC_DATA_P[3]	22	AK8	IO_L13P_22
FPGA_ADC_DATA_N[3]	22	AK9	IO_L13N_22
FPGA_ADC_DATA_P[5]	22	AK11	IO_L11P_CC_22
FPGA_ADC_DATA_RDY_N	22	AL10	IO_L8N_CC_22
FPGA_ADC_DATA_RDY_P	22	AL11	IO_L8P_CC_22
FPGA_ADC_DATA_N[9]	22	AM11	IO_L6N_22
FPGA_ADC_DATA_P[9]	22	AM12	IO_L6P_22
FPGA_ADC_DATA_N[13]	22	AM13	IO_L2N_22
FPGA_ADC_DATA_N[11]	22	AN12	IO_L4N_VREF_22
FPGA_ADC_DATA_P[13]	22	AN13	IO_L2P_22
FPGA_ADC_DATA_P[15]	22	AN14	IO_L0P_22
FPGA_ADC_DATA_P[11]	22	AP12	IO_L4P_22
FPGA_ADC_DATA_N[15]	22	AP14	IO_L0N_22
			Continued on Next Page...

Virtex-5 SX50T (XC5VSX50T-3FFG1136C) FPGA Pin Out			
Signal Name	**Bank**	**Pin**	**Description**
Bank 23: 40 Pins			
Bank Voltage: +3.3V			
P3V3D_V5	23	C26	VCCO_23
P3V3D_V5	23	F27	VCCO_23
P3V3D_V5	23	G24	VCCO_23
NOPAD			
Bank 25: 40 Pins			
Bank Voltage: +2.5V			
P2V5D_V5	25	AK25	VCCO_25
P2V5D_V5	25	AL22	VCCO_25
P2V5D_V5	25	AN26	VCCO_25
NOPAD			

Bibliography

[1] Memory interface generator user guide. http://www.xilinx.com/support/documentation/ip_documentation/ug086.pdf.

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