European LVDS Driver Development and ESCC Evaluation and Qualification

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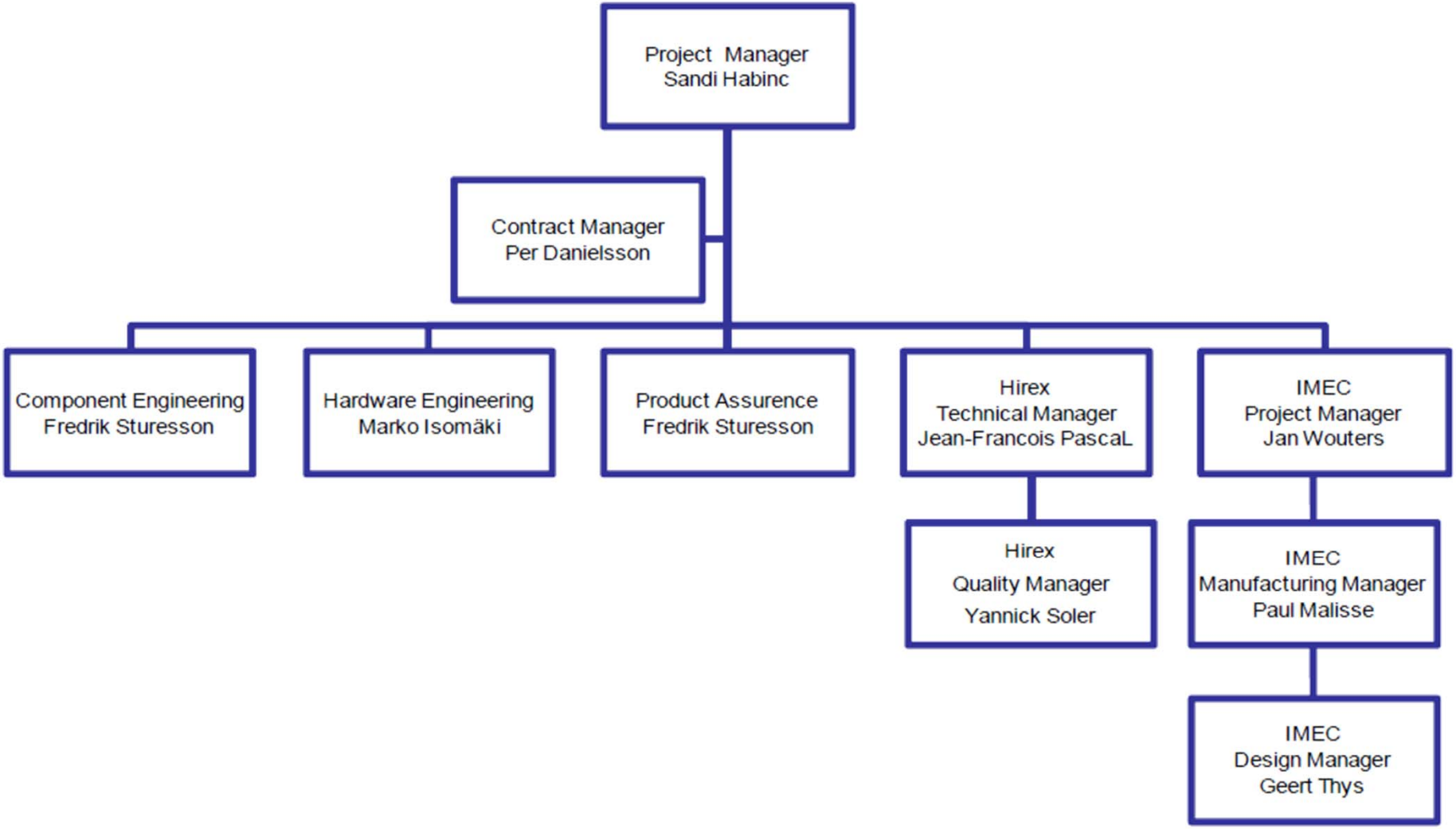
Quick introduction

- ESA Contract (ECI phase 3)
- 24 month development in three phases:
  - Definition and preliminary design
  - Design, prototype manufacture, test
  - ECSS qualification
- Development and ESCC Qualification os 2 LVDS ICs:
  - Dual Transceiver, 16 pin (type: National Semi. DS90LV049Q)
  - 4x4 Cross-Point Switch, 40 pin (type: Texas Instrument SN65LVDS125a)
- Based on technologies and companies with space heritage
  - Rad Hard CMOS
  - Hermetic sealed ceramic flat package
  - ESCC assembly and test

Consortium

- Aeroflex Gaiser
  - Requirement Definition
  - Package development
  - IC Assembly
  - System Validation
  - Evaluation board development and manufacturing
  - Radiation Testing
  - Product Documentation
  - ESCC Evaluation and Qualification
  - Commercialization of the product
- IMEC
  - IC Design and Verification
  - Management of Wafer production
- Hirex Engineering
  - Functional and Electrical validation testing
  - ESCC Evaluation testing and Screening testing
  - ESCC Qualification testing

Project team



Key features

- TIA/EIA-644 compliant LVDS inputs and outputs
- 3.3V single supply
- 3.3V LVTTL compatible input / output
- Up to 400 Mbps switching rates
- Tri-state output control

- Robust design, ESD, voltage tolerance, failsafe, coldsparing
- Radiation hard

Robustness (1/2)

- **ESD robustness**
  - **8 kV HBM ESD Level**
- **Overvoltage tolerant (transients)**
  - **Supply: -0.5V / 4.6V**
  - **LVTTL: -1V / +6V**
  - **LVDS: -5V / 6V**

Low risk of failure propagation at overvoltage, powered and un-powered.

Robustness (2/2)

- **Receiver Extended Common Mode Input**
  - **-4V / +5V**
- **Receiver with Active Failsafe Operation**
  - **High state at floating or shortened inputs**
- **Cold Spare outputs**
  - **For cold spare redundancy in multi-point systems**
- **5V tolerant TTL inputs**

Radiation

- **TID hard**
  - **> 300 krad(si)**
- **SEL immune**
  - **> 110 MeV-cm2/mg**
- **SEU/SET immune**
  - **> 80 MeV-cm2/mg**

by proven Rad Hard CMOS technology

Library extension for DARE 180 nm

- Receiver Extended Common Mode Input
- Receiver Failsafe Operation
- Cold Spare Functionality
- 8 kV HBM ESD Level

- Single Supply Capability
- Removal of External Resistor Requirement

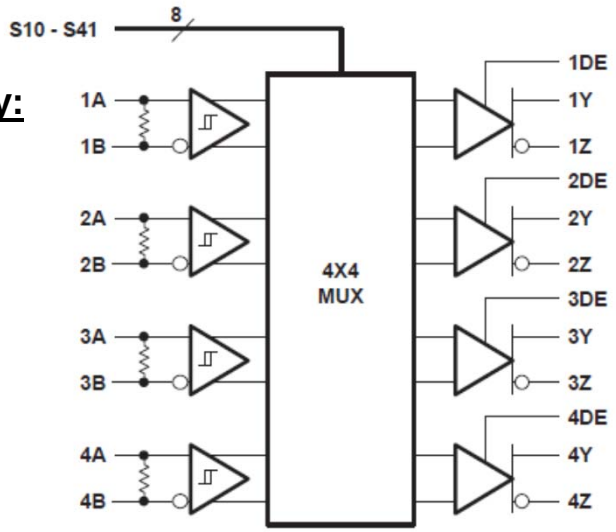
The LVDS IC devices

- **Dual Transceiver LVDS IC (pin compatible to DS90LV049Q) features the following pin types and counts (16 pins in total):**
  - **LVDS receiver pairs (+/-) 2 (2 pins each)**
  - **LVDS transmitter pairs (+/-) 2 (2 pins each)**
  - **LVTTL receiver output 2**
  - **LVTTL transmitter input 2**
  - **LVTTL enable (positive/negative) 2**
  - **Supply 2**

- **The 4x4 Cross-point Switch (pin compatible to SNLVDS125A) features the following pin types and counts (38 pins in total):**
  - **LVDS receiver pairs (+/-) 4 (2 pins each)**
  - **LVDS transmitter pairs (+/-) 4 (2 pins each)**
  - **LVTTL selectors 8**
  - **LVTTL enables 4**
  - **Supply 10**

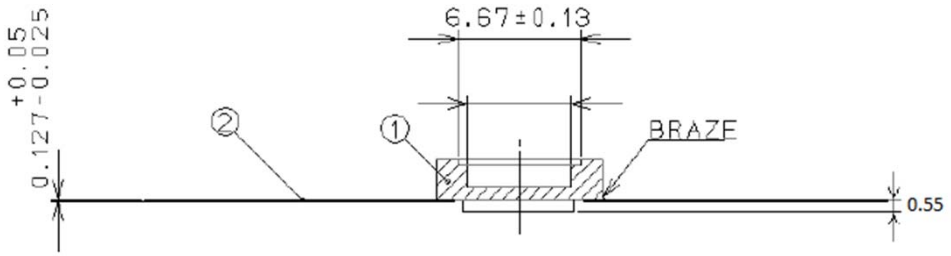
4x4 Cross-Point Switch (1/2)

- **Functionality and pin compability:**
  - **TI SN65LVDS125A**



NC	1	40	NC
S10	2	39	VCC
S11	3	38	GND
1A	4	37	1Y
1B	5	36	1Z
S20	6	35	1DE
S21	7	34	2Y
2A	8	33	2Z
2B	9	32	2DE
GND	10	31	GND
VCC	11	30	VCC
GND	12	29	GND
3A	13	28	3Y
3B	14	27	3Z
S30	15	26	3DE
S31	16	25	4Y
4A	17	24	4Z
4B	18	23	4DE
S40	19	22	GND
S41	20	21	VCC

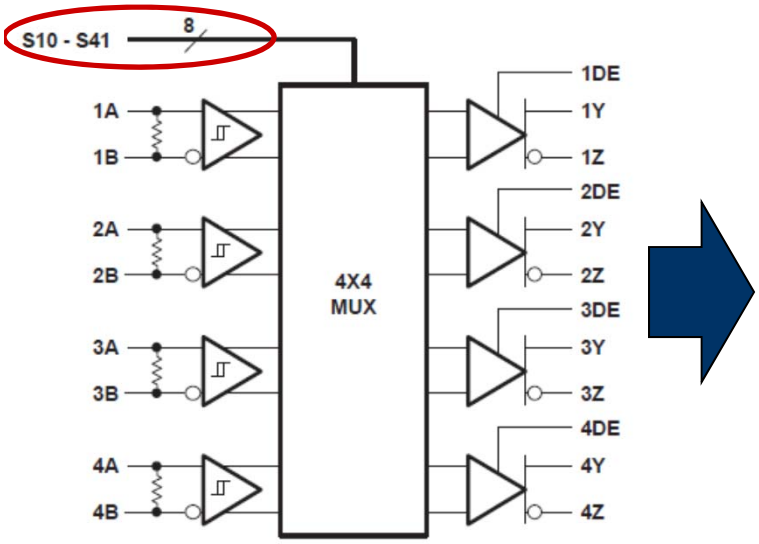
- **Ceramic flat package (baseline):**
  - **40 leads bottom brazed**
  - **1.27 mm pitch**
  - **26.7 mm x 9.0 mm x 2.5 mm**

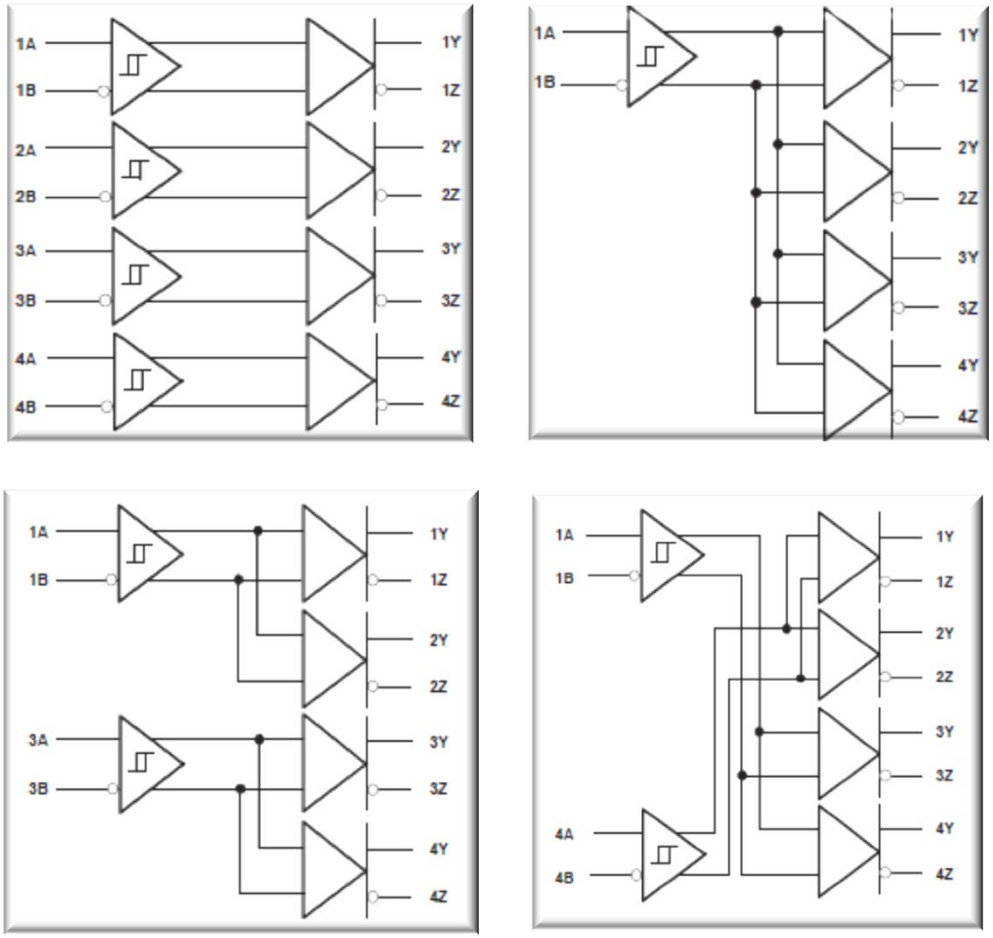


4x4 Cross-Point Switch (2/2)

Configuration Examples:

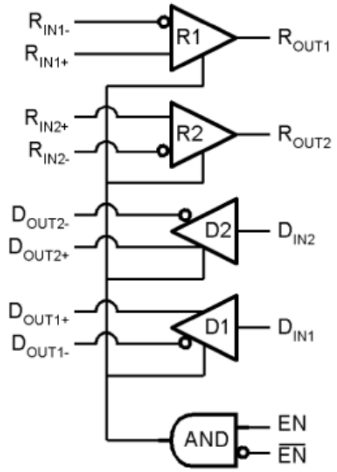
– **Selection with S10-S41**

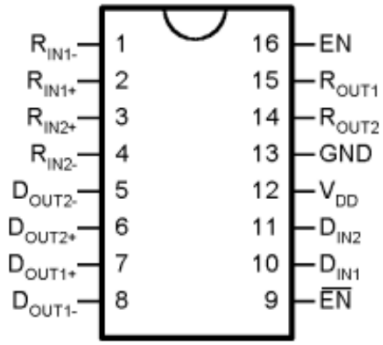


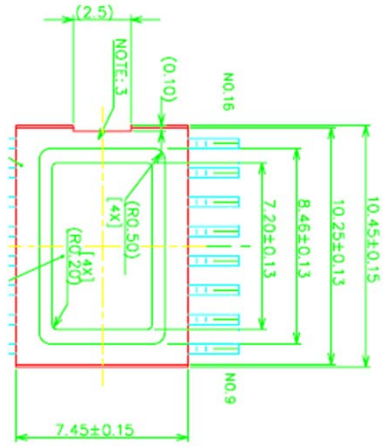


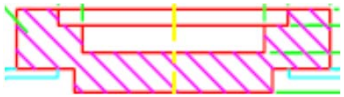
Dual LVDS Transceiver

- **Functionality and pin compability:**
  - **NSC DS90LV049Q**
  - **Ideal for Space Wire:**
    "one channel, one package"



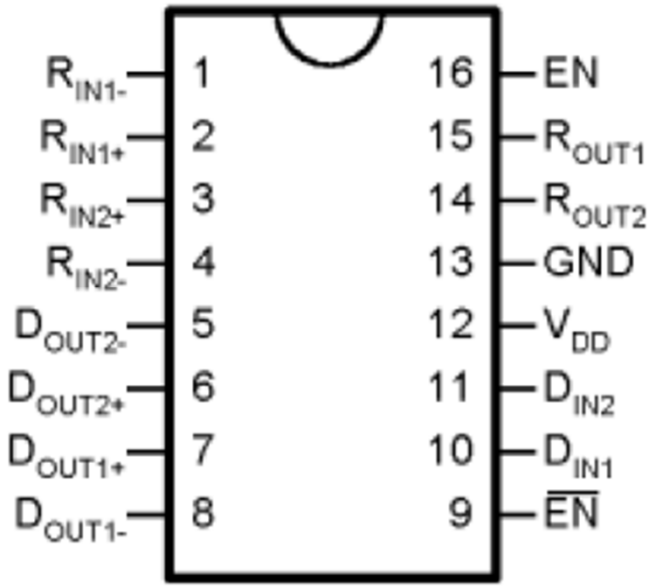


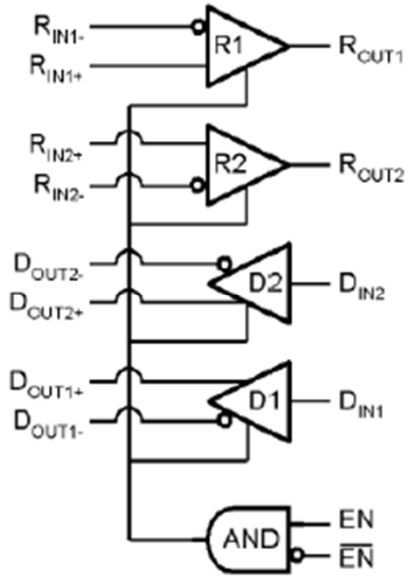




- **Ceramic flat package (baseline):**
  - **16 leads bottom brazed**
  - **1.27 mm pitch**
  - **10.5 mm x 7.5 mm x 2.2 mm**

Feedback: Dual Transceiver

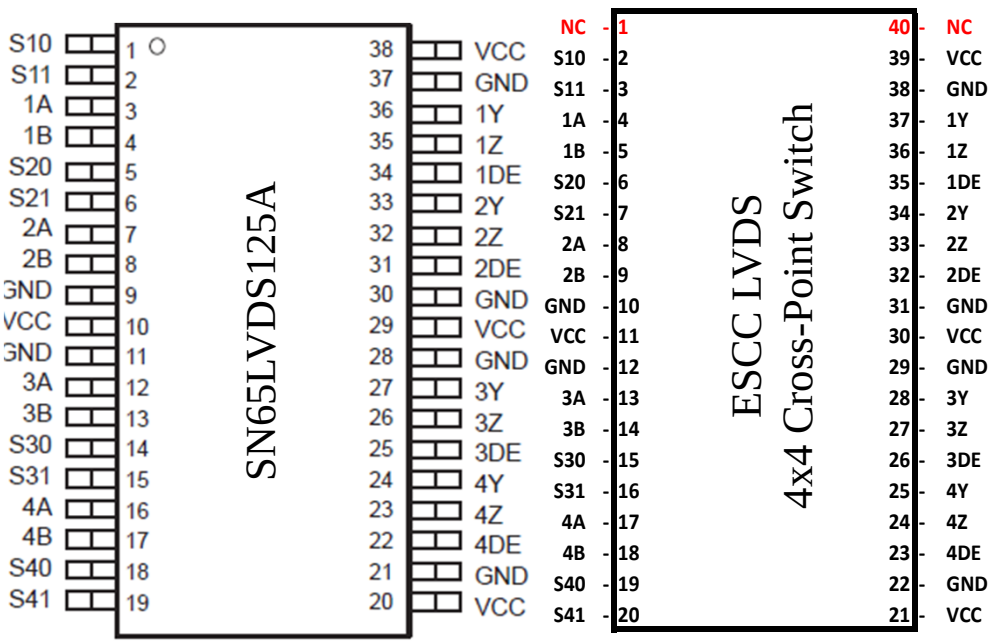


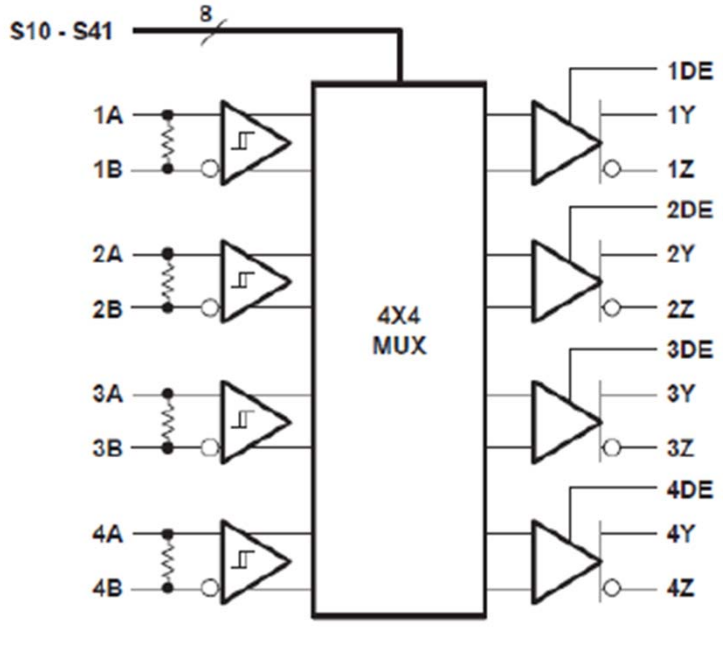


- By removing one of the enable pins this pin can be used as a mode pin:
  - Default enable value: Dual Transceiver
  - Not the default enable value: 2x2 Cross-point Switch
    - Use the two LVTTL inputs Din1 and Din2 as selectors
    - Use the two LVVTL output pins Rout1 and Rout2 for debug

Feedback: 4x4 Cross-point Switch

	SNLVDS125A	UT54LVDM288	UT54LVDM328	DS90LV049Q & UT54LVDM055		UT54LVDS031	UT54LVDS032	Custom
	Single 4x4 crosspoint	Quad 2x2 crosspoint	Octal repeater	Dual Rx & Tx		Quad Tx	Quad Rx	Redundant Rx & Tx
	Single	Dual	Quad	Dual	Quad	Quad	Quad	Dual
Signal / Mode	"00"	"00"	"01"	"10"	"10"	"10"	"10"	"11"
LVDS TX	8	8	8	4	8	8		8
LVDS RX	8	8	8	4	8		8	8
LVTTL DATA IN				2	4	4		2
LVTTL DATA OUT				2	4		4	2
ENABLE	4	4	4 (not 1)	2	4	4 (not 1+1)	4 (not 1+1)	4
SELECT	8	4						1
GND	6	6	6	6	6	6	6	6
VCC	4	4	4	4	4	4	4	4





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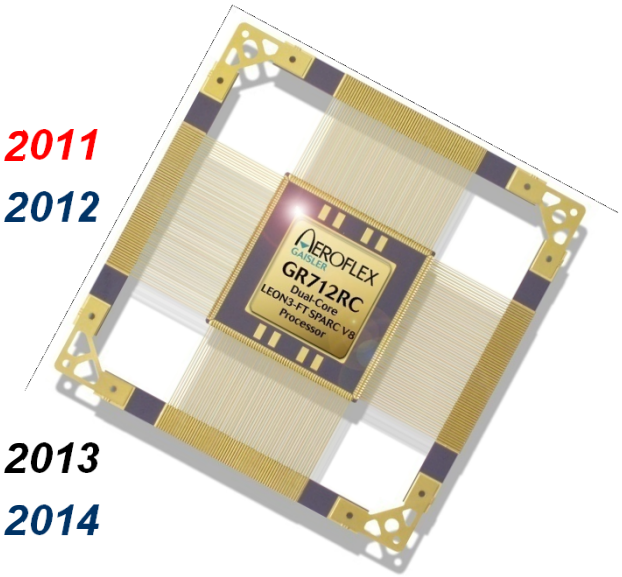
Schedule

- **August 2012**
  - **Specification / datasheet**
- **August 2013**
  - **Prototypes available**
  - **Prototype boards available**
- **April 2014**
  - **ESCC qualification och ESCC QPL**

Aeroflex Gaisler and space components

- **GR712RC, Dual Core LEON3FT processor**
  - **240 pin CQFP**
  - **Prototypes** — ***Q2 2011***
  - **MIL-STD-883 space flow** — ***Q4 2012***



- **SpaceWire Router**
  - **256 pin CQFP**
  - **Prototypes** — ***Q2 2013***
  - **ESCC 9000** — ***Q4 2014***

- **LVDS components**
  - **16 pin FP & 40 pin FP**
  - **Prototyper** — ***Q3 2013***
  - **ESCC qualification** — ***Q2 2014***

Contact information

- **IP cores information:**

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- **Board information:**

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- **Software and tools information:**

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