Genesys Logic, Inc.

GL835

USB 2.0 SD 3.0/MMC
Card Reader Controller

Datasheet

Revision 1.03
Dec. 07, 2017

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Revision History

Revision	Date	Description
0.90	11/29/2016	Preliminary release
0.91	01/10/2017	Modify Table 3.1 - GL835 Pin List/Descriptions
1.00	01/18/2017	1. Modify CH2 Features 2. Modify Table 3.1 - GL835 Pin List/Descriptions
1.01	04/25/2017	Update CH3.2 Pin List/Descriptions
1.02	11/14/2017	Modify CH3.2 Pin List/Descriptions
1.03	12/07/2017	Modify CH3.2 Pin List/Descriptions

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CHAPTER 1 GENERAL DESCRIPTION

GL835 is a crystal-less USB 2.0 to Single LUN SD3.0 (UHS-I/SDR-50)/MMC Memory Card Reader controller.

It supports USB 2.0 high-speed transmission to Secure Digital™ (SD), SDHC, miniSD, microSD (T-Flash), MultiMediaCard™ (MMC), RS-MMC, MMCmicro and MMCmobile on one chip. It also supports huge density memory cards (up to 2TB), such as SDXC and Memory Stick XC. As a single chip solution for USB 2.0 flash card reader, the GL835 complies with Universal Serial Bus specification rev. 2.0, USB Storage Class specification ver.1.0, and SD/MMC card interface specification.

The GL835 integrates a high speed 8051 microprocessor and a high efficiency hardware engine for the best data transfer performance between USB and flash card interfaces. Its' pin assignment design fits to card sockets to provide easier PCB layout. Inside the chip, it integrates 3.3V to 1.8V regulators and power MOSFETs and it enables the function of on-chip clock source (OCCS) which means no external 12MHz XTAL is needed and that effectively reduces the total BOM cost.

CHAPTER 2 FEATURES

- USB specification compliance
  - Comply with 480Mbps Universal Serial Bus specification rev. 2.0
  - Comply with USB Storage Class specification rev. 1.0
  - Support one device address and up to four endpoints:

    Control (0)/ Bulk Read (1)/ Bulk Write (2)
- Integrated USB building blocks
  - USB2.0 transceiver macro (PHY), USB controller, Build-in power-on reset (POR)
- Embedded 8051 micro-controller
  - Embedded mask ROM and internal SRAM
- Secure Digital™ (SD)
  - Support SD specification v1.0 / v1.1 / v2.0/ SDHC (Up to 32GB)
  - Support SD specification v3.0 UHS-I: SDR25/SDR50
  - Support 1.8V/3.3V switch signal pads
  - Support SDXC (Up to 2TB)
- ※ Optional: MultiMediaCard™ (MMC)
  - Support MMC specification v3.x / v4.0 / v4.1 / v4.2.
  - x1 / x4 bit data bus
- On chip clock source (OCCS) to eliminate the use of one 12MHz crystal from board
- Support 3.3V power input
- On-Chip 3.3V to 1.8V regulators
- Provide Over-Current protection mechanism for safety power supply
- On-Chip power MOSFETs for supplying flash media card power
- Support Power Saving mode/ Selective suspend driver for better power management.
- Support Spread Spectrum Clock enabled by vendor driver for SD to reduce EMI effect
- Support Remote Wakeup by default
- Support SD CPRM
- Support Intel Power Optimizer
- Support Microsoft InstantGo
- Support RTD3
- Package available in 24 pin QFN (4x4 mm)

CHAPTER 3 PIN ASSIGNMENT

3.1 QFN 24 Pinout

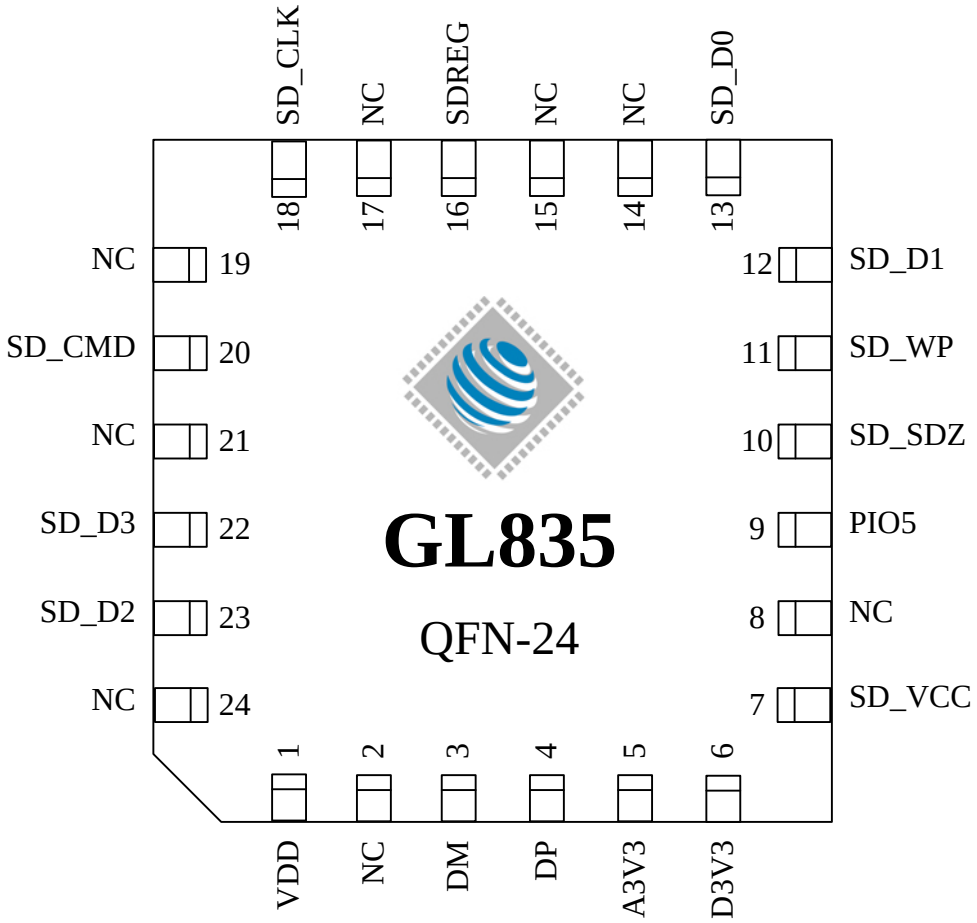


Figure 3.1 - 24 Pin QFN Pin out Diagram

3.2 Pin List/Descriptions

Table 3.1 - GL835 Pin List/Descriptions

Pin name	QFN24	Type	Description
VDD	1	P	1.8V core power, the power source of this pin comes from the internal regulator and no need of external 1.8V power input
NC	2	-	Not connect
DM	3	A	USB D-
DP	4	A	USB D+
A3V3	5	P	AVDD33
D3V3	6	P	DVDD33
SD_VCC	7	P	SD card power 400mA
NC	8	-	Not connect
PIO5	9	I, PU	Power-saving mode/Normal mode NC: Power-saving mode GND: Normal mode
SD_CDZ	10	I, PU	SD card detect 0: Card insert 1: No card
SD_WP	11	B, PU	SD write protect 0: write enable 1: write protection
SD_D1	12	B, PU	SD_DATA1
SD_D0	13	B, PU	SD_DATA0
NC	14	-	Not connect
NC	15	-	Not connect
SDREG	16	P	Internal regulator for SD card. An external capacitor should be connected
NC	17	-	Not connect
SD_CLK	18	O	SD clock
NC	19	-	Not connect
SD_CMD	20	B, PU	SD command
NC	21	-	Not connect
SD_D3	22	B, PU	SD_DATA3
SD_D2	23	B, PU	SD_DATA2
NC	24	-	Not connect

Notation:

Type	**O**	Output
	I	Input
	B	Bi-directional
	pu	Internal pull-up when input
	pd	Internal pull-down when input
	P	Power / Ground
	A	Analog

CHAPTER 4 BLOCK DIAGRAM

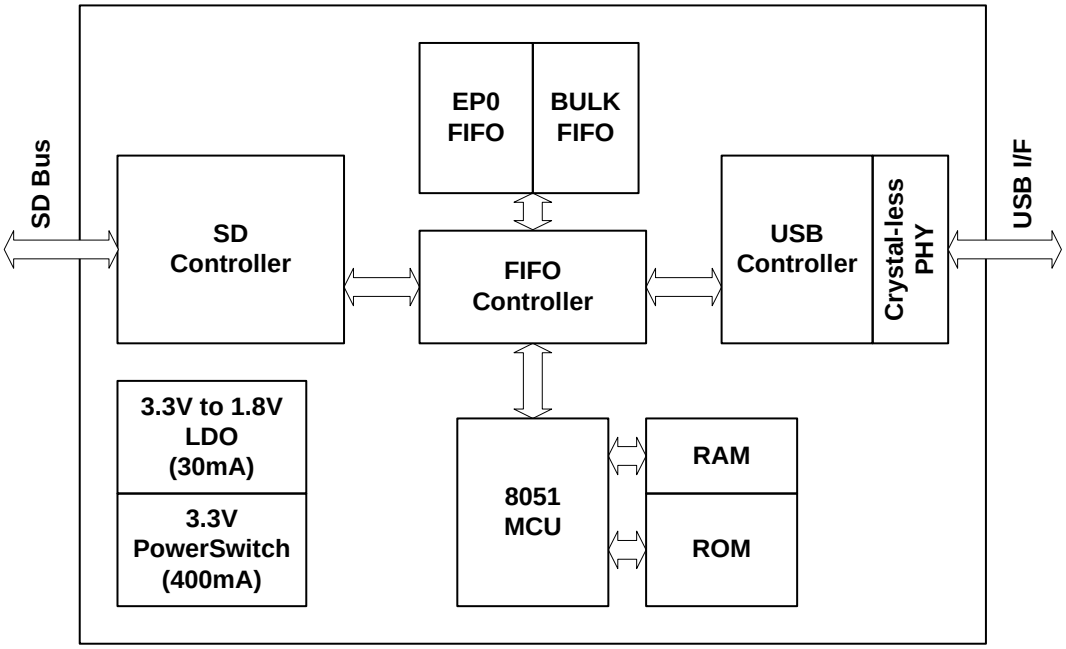


Figure 4.1 - Functional Block Diagram

4.1 Crystal-less PHY

The USB 2.0 Transceiver Macrocell is the analog circuitry that handles the low level USB protocol and signaling, and shifts the clock domain of the data from the USB 2.0 rate to one that is compatible with the general logic. On chip clock source and no need of 12MHz Crystal Clock input.

4.2 USB Controller

The Serial Interface Engine, which contains the USB PID and address recognition logic, and other sequencing and state machine logic to handle USB packets and transactions.

4.3 EPFIFO

Endpoint FIFO includes Control FIFO (FIFO0) and Bulk In/Out FIFO

- **Control FIFO** FIFO of control endpoint 0. It is 64-byte FIFO and used for endpoint 0 data transfer.
- **Bulk In/Out FIFO** It can be in the TX mode or RX mode:
  1. It contains ping-pong FIFO (512 bytes each bank) for transmit/receive data continuously.
  2. It can be directly accessed by micro-control

4.4 MCU

8051 micro-controller inside.

- **8051 Core** Compliant with Intel 8051 high speed micro-controller
- **ROM** FW code on ROM
- **SRAM** Internal RAM area for MCU access

4.5 SD controller

- Memory card host controller includes SD engine and DMA engine

4.6 Regulator and Power Switch

- **3.3V to 1.8V LDO** Core logic power source
- **3.3V power switch** SD card power source

CHAPTER 5 ELECTRICAL CHARACTERISTICS

5.1 Temperature Conditions

Table 5.1 - Temperature Conditions

Parameter	Value
Storage Temperature	-65°C to +150 °C
Operating Temperature	0°C to +70 °C

5.2 Operating Conditions

Table 5.2 - Operating Conditions

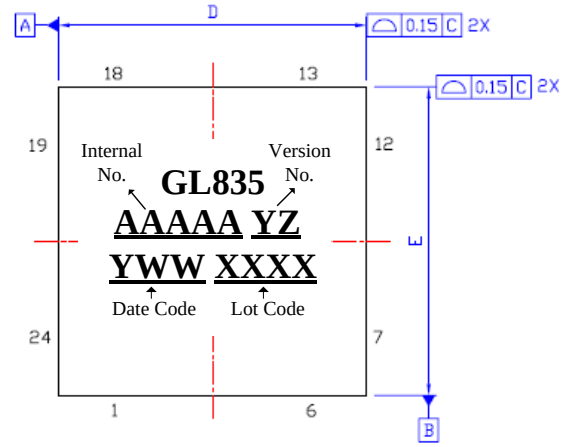
Parameter	Value
Supply Voltage	+3.135V to +3.465V
Ground Voltage	0V

5.3 DC Characteristics

Table 5.3 - DC Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	3.3V source	3.135	-	3.465	V
V_{IH}	Input High Voltage		2.0	-		V
V_{IL}	Input Low Voltage			-	0.4	V
I_I	Input Leakage current	$0 < V_{IN} < V_{CC}$	-10	-	10	µA
V_{OH}	Output High Voltage		2.8	-	-	V
V_{OL}	Output Low Voltage		-	-	0.4	V
I_{OH}	Output Current High		-	8	-	mA
I_{OL}	Output Current Low		-	8	-	mA
C_{IN}	Input Pin Capacitance		-	5	-	pF
I_{SUSP}	Suspend current	1.5K external pull-up included	-	-	276	µA
I_{CC}	Supply current	Connect to USB with 8051 operating	-	-	70	mA
*I_{NORMAL}	Idle current		-	41.8	-	mA

CHAPTER 6 PACKAGE DIMENSION



SYMBOL	DIMENSION MM (MIL)		
	MIN.	NOM.	MAX.
A	0.70 (27.6)	0.75 (29.5)	0.80 (31.5)
A1	---	0.02 (0.8)	0.05 (2.0)
A3	0.203 (8.0) REF		
b	0.18 (7.1)	0.25 (9.8)	0.30 (11.8)
D	4.00 (157.4) BSC		
D2	1.90 (74.8)	2.40 (94.5)	2.85 (112.2)
E	4.00 (157.4) BSC		
E2	1.90 (74.8)	2.40 (94.5)	2.85 (112.2)
e	0.50 (19.7) BSC		
L	0.30 (11.8)	0.40 (15.7)	0.50 (19.7)

NOTE: 1. REFER TO JEDEC STD. MO-220
2. ALL DIMENSIONS IN MILLIMETERS.

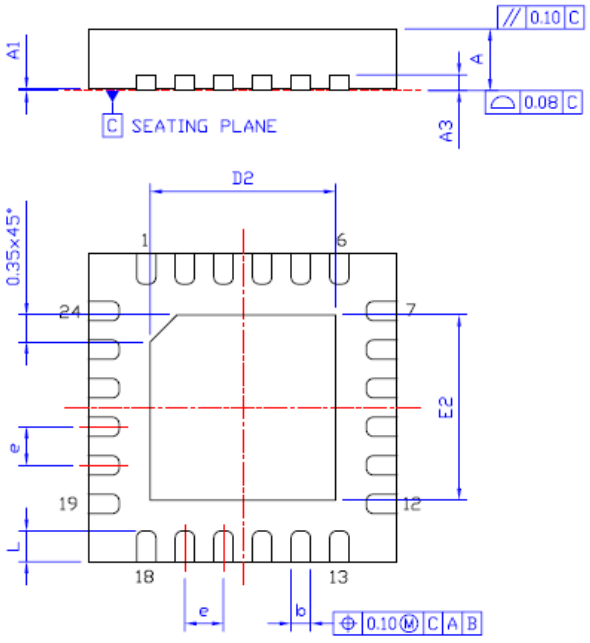


Figure 6.1 - QFN 24 Pin Package

CHAPTER 7 ORDERING INFORMATION

Table 7.1 - Ordering Information

Part Number	Package	Green/Wire Material	Version	Status
GL835-OGY03	QFN 24	Green Package + CU Wire	03	MP