

WILLIAM PETERS
RM02/03/05 Handbook
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## INTRODUCTION

The purpose of this handbook is to provide the Field Service Engineer with often used or good to know information. It also puts register bit definitions, module information, adjustment procedures, documentation, and other miscellaneous information into one package.

A smaller disk reference guide in a three or six ring binder is to be developed for publication soon. Separate sections will be developed for different disks such as the RM series disks and the RP04/05/06.

Your comments and ideas are welcome. Please review this copy as it will be the foundation for the printed version. Is it too much? Is it too little? Have you found any technical errors or typos?

It is not the purpose of this book to provide step by step troubleshooting. It is rather to provide a time-saving reference resource which hopeffully will aid the engineer in solving the problem.

Please address your comments to:
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DTN 223-4391

| $\begin{aligned} & \text { RMCS1 } \\ & (776700) 00 \end{aligned}$ | SC | TRE | MCPE | 0 | DVA | PSEL | A17 | A16 | RDY | IE | F4 | F3 | F2 | F1 | FO | GO |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |

BITS 00-05 Drive function field bits $01-05$ determine what function the drive will perform. Bit 00 is the GO bit and must be set in conjunction with the function bits before the drive will execute any command. The GO bit is cleared on completion of a command or by an error during the command.

## FUNCTION CODES <br> OPERATION

01
05
07
11
13
15
17
21
23
31
51
53
61
63
71
73

No operation
Seek command
Recalibrate
Drive clear
Port release Offset command Return to centerline Read-in preset Pack acknowledge Search command Write check data Write check header and data Write data Write header and data Read data Read header and data

Any other value in this field will set the illegal function bit (ILF) in RMERI.

BIT 06 Interupt enable. When set by the program, this will generate an interupt upon completion of a command or when an error is encountered.

BIT 07 Indicates the controller is ready to accept a new command.

BIT 08
BIT 09
BIT 10

BIT 11
Drive Available. Used in dual port configurations to indicate that the drive is currently available to this controller.

BIT 12 Not used.
BIT 13 Mass control parity error. Set when the RH controller detects a parity error on the massbus control lines. This bit would be set as the result of a remote register read in which bad parity was detected. If bad parity occurs during a write to a remote register, the PAR bit in RMER1 would be set.

BIT 14 Transfer error. Set by DLT, WCE, UPE, NED, NEM, MXF, PGE, MDPE, Or a drive error during a data transfer.

BIT 15 Special condition. Set by TRE or ATTN or Control Parity Error.

RMWC (776702) RH

| $W C$ | $W C$ | $W C$ | $W C$ | $W C$ | $W C$ | $W C$ | $W C$ | $W C$ | $W C$ | $W C$ | $W C$ | $W C$ | $W C$ | $W C$ | $W C$ |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |

## R/W

BITS 00-15 Contains the two's compliment of the number of words to be transfered to or from the drive over the syncronous data bus.

| RMBA |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| :--- | :--- | :--- | :--- | :--- | :--- | :--- | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| ( 776704 ) RH | BA | BA | BA | BA | BA | BA | BA | BA | BA | BA | BA | BA | BA | BA | BA | BA |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |  |

BITS 00-15 Contains the memory address to which the next transfer will start at. It is incremented by two and does not transfer to odd boundaries. Bit 00 is always read as a zero.

| RMDA |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| :--- | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| ( 776706 ) 05 | 0 | 0 | 0 | TA | TA | TA | TA | TA | 0 | 0 | 0 | SA | SA | SA | SA | SA |

BITS 00-04 Sector address. Set to the sector desired and increments at the end of each sector transfered.

BITS 08-12 Track address. Set to the desired track and is incremented by the sector address overflow. Note that bits ll-12 are not used by RM02/03.

RMCS2
(776710)RH

| DLT | WCE | UPE | NED | NEM | PGE | MXF | MDPE | OR | IR | CLR | PAT | BAI | U2 | U1 | UO |
| :--- | :--- | :--- | :--- | :--- | :--- | :--- | :--- | :--- | :--- | :--- | :--- | :--- | :--- | :--- | :--- |

BITS 00-02 Select a drive on the massbus, 0-7.
BIT 03 Bus Address Increment Inhibit. When set disables the Bus Address register from incrementing on a data transfer.

Page 2

BIT 04

BIT 05

BIT 06

BIT 07

BIT 08

BIT 09

BIT 10

BIT 11

BIT 12

BIT 13

BIT 14

Parity Test. When set, the controller generates even parity on both the control bus and the data bus. When clear, the controller normally generates odd parity. Note that when this bit is set it only checks for even parity recieved on the data bus.

Clear. Setting this bit will initialize the RH controller plus all the drives on the massbus.

Input Ready. Serves as a status bit to the program to inform it when the RH data buffer is ready to accept another word. If an attempt to write the data buffer is made before the Input Ready bit comes up, it will result in a data late error.

Output Ready. Indicates that the RH data buffer has a word of data latched in the output. An attempt to read the data buffer before Output Ready comes up will result in a data late error.

Massbus Data Parity Error. Set when the controller detects bad parity on the syncronous data bus. As with MCPE errors, the bit PAR in RMERI will set if the parity error occured during a write to the drive.

Missed Transfer. Will set if a drive fails to initiate a command for any reason. For instance if you issue a command with an error set. On a data command, missed transfer will be set if the drive does not respond within 250 ms .

Program error. This will be set if the programmer neglects to check for ready before issueing a command to the RH. Set by any command while the RH is busy.

Non-existant memory. Set when the controller does not get a response from main memory during a DMA cycle. On 11 systems indicates that memory did not respond to the RMBA by asserting MSYN within 10 uS. When this error occurs the PMBA will contain the bad address plus 2.

Non-existant drive. Set when the drive selected does not respond (assert TRA) within l.5 uS after the controller asserts DEM.

Unibus Parity Error. Set when a parity error is detected on a Write or a Write Check command. The feature is disabled when performing 18 bit transfers.

Write Check Error. When set indicates that the word read from the disk does not match the corresponding word in main memory. The RMBA will contain the address plus two of the failing word in memory and the RMDB will contain the failing word from the disk.

BIT 15 Data Late. Set when the controller is unable to accept a word during a read or a write-check or is unable to supply a word on a write operation at the time the drive demands it. This error indicates a severely overloaded bus. This bit can also be set by improper reading of the data buffer by the program.


BIT 00 Offset mode. Set when an offset command is issued to the drive. When set and a read command is recieved by the drive, the offset is performed prior to the read. Offset in the RM series drives is always done in a single step one way or the other. You cannot offset in multiple steps as in a RP04,5,\&6.

BITS 01-05
BIT 06

BIT 07

BIT 08

BIT 09

BIT 10

Spares. Reserved for future expansion.
Volume Valid. This bit is used to insure that the same disk pack is mounted on the drive as the last time the program used it. Volume Valid is cleared by the assertion of MOL. Therefore, any momentary loss of power, any unsafe condition, or drive address plug change will cause loss of VV. This will crash a software system by causing a fatal mount error.

Drive Ready. Set when ever the drive is ready to accept a new command. Clears immediately on reciept of a command. Setting of this bit indicates normal command termination. If an error is encountered, it will remain reset and the appropriate error bit will set.

Drive Present. Always set as long as there is power to the RM Adapter.

Programmable. Indicates that the drive is selected to operate in the dual port mode.

Last Block Transferred. This bit is set when the last addressable block on the disk pack has been transfered. Cleared by writing a new disk address into the RM desired cylinder register or track address register. This bit is used to prevent a spiral read on the pack from wrapping around to cylinder 0 . An attempt to read or write with this bit set will result in an AOE.

BIT 11 Write Locked. Set when the manual write protect switch on the drive is depressed or when MOL is not asserted. The drive will not accept any write commands in this state.

BIT 12 Medium on Line. Indicates that the drive has succeded in loading heads and is on cylinder. Any change in power status or if heads are unloaded, the MOL will reset. Dropping MOL will set ATA.

BIT 13 Positioning in Progress. Set only during the execution of positioning commands until the heads are settled over the correct cylinder. If PIP was set as a result of a direct positioning command such as SEEK, ATA will be asserted at the completion. ATA would not be asserted at the completion of positioning caused by implied seeks.

BIT 14
Error. This is a composite of any error bit in the RMERI or RMER2 registers.

BIT 15
Attention. This bit will set on any error if GO bit is set, at the completion of a command or if GO bit reset, at the occurance of the error. It will also set anytime MOL changes state. Cleared by Drive Clear or by writing a one into the bit in the ATA summary register.

| RMER1 <br> $(776714) 02$ DCK |
| :--- |

BIT 00 Illegal Function. Set by loading an invalid code into the function field of RMCSl (with GO and no previous errors). ILF is a class B error.

BIT 01 Illegal Register. Set by trying to read or write a massbus register whose number is greater than 17 octal. ILR is a class A error.

BIT 02
Register Modification Refused. Set when trying to write into any register except RMAS or RMMRI while the GO bit is active. RMR is a class A error.

Parity Error. Set by the drive detecting a parity error on information sent to it by the controller. If the parity error is on the Massbus control lines, the PAR bit sets and is classified as a class A error. If the parity error is detected on the data bus, then DPE of RMER2 will set also. This condition is a class B error.

Format Error. Set to indicate that bit 12 of the sector header does not agree with bit 12 of the RMOF register. This generally indicates that a pack formatted in 18 bit mode has been installed on 16 bit machine or vice versa. This bit will be inhibited if bit 10 of RMOF (HCI) is set and will always be invalid if bit 08 of RMERI (HCRC) is set. FER is a class A error during a Read header and data command and is a class $B$ error during all other commands.

Write Clock Fail. Set by the drive if it does not recieve write clock from the controller within l.6uS after asserting sync clock on a write or write header command. WCF is a class $B$ error.

ECC Hard Error. Indicates that the ECC logic was unable to correct the error. An ECC hard error is defined as an error burst greater than 11 bits in length. ECH is a class B error.

Header Compare Error. The first word of the header read does not match the RMDC (cylinder address) or the second word of the header does not match the contents of the RMDA (sector and track address). This is a positioning error as the drive did not go to the address specified by the controller. The meaning of this bit is not valid if HCRC is set. HCE is a class A error during a read header command and a class $B$ error during all others.

Header CRC error. Set if the CRC word generated by reading the header did not compare with the CRC word that was written in the header at the time the disk was formatted. $H C R C$ is a class $A$ error during a read header and data command and is a class B error during all others.

Address overflow error. Set when the controller requests a data tranfer to a block beyond the disk addresses which are possible. Note that when AOE is set, the contents of RMDA will increment at EBL time even though the command was terminated. AOE is a class $B$ error.

Invalid Address Error. Set when an invalid cylinder address, track address, or sector address are used in trying to perform a read or write or seek or search command. This differs from AOE in the respect that AOE is an overflow from the last sector of the last track of the last cylinder of the pack during a data command. IAE is a class B error.

Write Lock Error. Set if a write command is issued to a write protected drive. WLE is a class B error.

BIT 12 Drive Timing Error. Set when a sector pulse is detected during sector compare time. This usually is the result of installing an unformatted pack. Any time the SYNC byte of a sector is not detected a drive timing error could result. DTE is a class B error.

BIT 13 Operation Incomplete. Set primarily by three conditions: Drive does not respond to a command on the tag bus within 300 ns (Does not drop +On Cylinder) with a Seek command. Drive does not find a sector within three revolutions of the disk with a search command. Or; The massbus run signal is not asserted within 20 mS after the GO bit is set. OPI is a class $B$ error.

BIT 14
Unsafe. A condition exists which prevents the normal operation of the drive, such as low AC power. See RMER2.

BIT 15 Data Check Error. Set if after reading the entire data field, bits ll-3l are non-zero. DCK is a class A error if ECI of RMOF is set and it is a class $B$ error if ECI of RMOF is cleared.

RMAS
(776716) 04

| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | ATA | ATA | ATA | ATA | ATA | ATA | ATA | ATA |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |

BITS 00-07 Indicate which drives attention conditions exist on. Bit 00 equals drive zero, bit 07 equals drive seven. Clear by writing a one into the appropriate bit position.
RMLA

$(776720) 07$ | 0 | 0 | 0 | 0 | 0 | SC | SC | SC | SC | SC |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| 16 | 8 | 4 | 2 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |

BITS 00-05 SPARES
BITS 06-09 Sector count lines. Indicates the current sector that the heads are positioned over.

BITS 10-15 SPARES

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| RMDB |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| :--- | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| ( 776722 ) RH | DB | DB | DB | DB | DB | DB | DB | DB | DB | DB | DB | DB | DB | DB | DB | DB |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |  |

BITS 00-15 RM Data Buffer. When reading this register, the contents of the RH OBUF will be displayed. When writing this register, the data will go into the RH IBUF and will move toward the OBUF as the silo emptys.

RMMR1

(776724) 03 | $O C C$ | R/G | EBL | REX | ESRC | PLFS | ECRC | PDA | PHA | CONT | WC | EECC | WD | LS | LST | DMD |
| :--- | :--- | :--- | :--- | :--- | :--- | :--- | :--- | :--- | :--- | :--- | :--- | :--- | :--- | :--- | :--- |
| R |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| DBCK | DBEM | DEBL | MSEN | MCLK | MRD | MUR | MOC | MSER | MDF | MS | DTG | MWP | MI | MSC | DMD |

Bit assignments for RMMRI Read-Only portion:

| BIT | 00 | Diagnostic Mode. Set to put RM Adapter in to the maintenance and diagnostic mode. |
| :---: | :---: | :---: |
| BIT | 01 | Last Sector / Track. Used to fake the condition of a last sector on a track and force the cylinder address to increment as in a mid-transfer seek. |
| BIT | 02 | Last Sector. Used to fake the last sector of a track in order to increment heads as in a spiral read. |
| BIT | 03 | Write Data. Imitates the serial write data normally fed to the disk. Depending on when it is read, it can emulate the output of the data register, the ECC generator, or the CRC generator. |
| BIT | 04 | Enable ECC Out. This bit is only set during write operations when the ECC pattern is being written. |
| BIT | 05 | Prom Strobe. One complete prom cycle requires 16 bit clocks and controls the generation of read and write timing in the RMA. Produced by the Servo clock except during a read when it is a function of the read clock. |
| BIT | 06 | Continue. Set at the end of EBL if the run line is still active, the controller continues to perform the data transfer as long as this bit is active. |
| BIT | 07 | Header Area. This bit is generated by the data sequencer to indicate that the header has been found. It is set by the header sync byte and cleared by the header CRC area. |
| BIT | 08 | Data Area. Same as above except set by the data sync byte and cleared by the last word in a sector. |

Enable CRC Out. During a write operation this bit is set by the data sequencer to enable the CRC to be written following the data field.

Looking for Sync. Set during the sector gap to indicate that the sequencer is looking for the sync byte for the next sector. During this time the word clock is inhibited to the data sequencer.

Enable Search. This indicates that the search logic is enabled and is looking for rotational postion. When sector compare comes up, this bit will reset and the data sequencer will be activated.

Exception. This reflects the status of the Mass Exception line.

END OF BLOCK. Set by the adapter to indicate that the last block of data has been transfered.

Run and GO. Set when the massbus run line is active and the GO bit is set.

Occupied. Set when the syncronous data bus is involved in a valid transfer. Cleared on the trailing edge of GO.

Bit assignments for RMMRI write-only portion:
Diagnostic Mode. Sets the RM Adapter in maintenance mode and completely isolates the drive from the adapter.

Sector Compare. Simulates the function of the sector compare logic.

Index Pulse. Simulates the function of the drive index pulse. Used primarily to check out the format logic.

Write Protect. Allows the diagnostic to verify the write protect logic.

NOT USED.
Sector Pulse. Simulates the drives sector pulse to clock logic in the sector compare circuits.

Drive Fault. Used by the diagnostic to simulate the drive fault signal.

Seek Error. Fakes a seek error to occur from the disk drive.

| BIT 08 |  | On Cylinder. Simulates the on cylinder signal in the disk drive. |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| BIT 09 |  | Unit Ready. Set by the diagnostic to indicate that the pack is spun up and ready. |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| BIT 10 |  | Read Data. disk drive |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| BIT 1] |  | Maintenance Clock. Used to control the data flow through the adapter in maintenance mode. When used with read gate asserted, simulates read clock. If used with write gate asserted, simulates servo clock. |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| BIT 12 |  | Search Time-out Disable. Inhibits the search time-out if the sector is not found within two revolutions to give the diagnostic functions time to operate. |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| BIT 13 |  | Diagnostic EBL. Allows the diagnostic to step through the command sequencer states without completeing an entire command. EBL is the signal which can terminate. |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| BIT 14 |  | D. Clk. En.. Allows the programmer to debug the control sequencer by single stepping the system clock. |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| BIT 15 |  | Debug Clock. This is the bit the programmer would toggle to simulate the system clock if bit 14 were set. |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  | 15 | 14 | 13 | 12 | 11 | 10 | 09 | 08 | 07 | 06 | 05 | 04 | 03 | 02 | 01 | 00 |
| $\begin{aligned} & \text { RMDT } \\ & (776726) 06 \end{aligned}$ | 0 | 0 | MOH <br> 1 | 0 D | DRO | 0 | 0 | DT | DT | DT 6 | DT | DT 4 | DT 3 | DT 2 | DT 1 | DT 0 |
| BITS 00- | 8 | Drive Type Register |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| BIT 11 |  | Drive Request Required. If set indicates a dual port drive. |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| BIT 13 |  | Moving Head. Since all RM series drives are moving head devices, this bit is hard-wired in the RMA. |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| $\begin{aligned} & \text { RMSN } \\ & (776730) 10 \end{aligned}$ | SN 8000 | SN | (1) ${ }^{\text {SN }}$ 2000 | $\begin{gathered} \text { SN } \\ 1000 \end{gathered}$ | SN <br> 800 | SN 400 | SN 200 | $\begin{aligned} & \hline \text { SN } \\ & 100 \end{aligned}$ | SN | SN 40 | SN 20 | SN | SN 8 | SN 4 | SN 2 | SN 1 |

BITS 00-15 This is the RM serial number register.

RMOF
(776732) 11

| 0 | 0 | 0 | FMT <br> 16 | $E C I$ | $H C I$ | 0 | 0 | OFF <br> DIR | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| :--- | :--- | :--- | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |

RN

BITS 00-06, Not used, always zero.
BIT 07 Offset Direction. When set, the offset direction is toward the spindle. When reset, the offset direction is away from the spindle. This bit is valid if the Offset Mode bit is set by loading an offset command into RMCSI.

BITS 08-09 Not used, always zero.
BIT 10 Header Compare Inhibit. This bit allows the hardware to read a pack in which the header is bad or invalid. Setting this bit disables bits 07,08 of the RMERI register. This is a useful tool in troubleshooting positioning errors. It is recommended that you reset this bit before trying to do a write.

BIT 11 Error Correction Inhibit. This allows the drive to read the disk in spite of a data check error because it disables the normal ECC check that is done at the end of the data field. Used by the diagnostic to troubleshoot ECC and data errors.

BIT 12
Format. When set, selects 16 bit word length in the format of the pack. Reset, equals 18 bit length. If this bit does not agree with the format bit written in the header, the format error bit in RMERl will set on a data transfer command.

BITS 13-15 Not used, always zero.

| RMDC <br> $(776734)$ 12 | 0 | 0 | 0 | 0 | 0 | 0 | $D C$ | $D C$ | $D C$ | $D C$ | $D C$ | $D C$ | $D C$ | $D C$ | $D C$ | $D C$ |
| :--- | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |

BITS 00-09 Desired Cylinder Address Register. Bit 00 is the least significant bit and bit 09 is the most significant bit. Loading this register with a value larger than the maximum cylinder address possible will result in an invalid address error in RMERI.

RMHR
(776736) 13

| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| :--- | :--- | :--- | :--- | :--- | :--- | :--- | :--- | :--- | :--- | :--- | :--- | :--- | :--- | :--- | :--- |

The holding register is used by the diagnostic and has no drive function. It shadows any other valid register and holds a two's complement of it's data.

RMMR2 (776740) 14

| $R Q A$ | ROB | TAG | TEST | CIC | CIH | BB | BB | BB | BB | BB | BB | BB | BB | BB | BB |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |

BITS 00-09 Tag Bus Bits. These read-only bits reflect the state of the tag bus which runs between the RMA and the RM02/03/05/80 logic panel. This bus has three functions depending on which 'tag' line is asserted. The table below describes the possible functions associated with each bit.

| BUS BIT | CYLINDER TAG | HEAD TAG | CONTROL TAG |
| :--- | :---: | :---: | :--- |
| BB 00 | 1 | 1 | Write gate |
| BB 01 | 2 | 2 | Read gate |
| BB 02 | 4 | 4 | Servo offset plus |
| BB 03 | 8 | 8 | Servo offset minus |
| BB 04 | 16 | 16 | Not used |
| BB 05 | 32 | Not used | Not used |
| BB 06 | 64 | Not used | Return to Zero |
| BB 07 | 128 | Not used | Not used |
| BB 08 | 256 | Not used | Not used |
| BB 09 | 512 | Not used | Not used |

BIT 10 Control or Head Select. This bit is used to indicate the type of function that the bus bits are currently used for. If set, the tag is either control or head select. If reset, this means the tag is for cylinder address select. Read-only.

BIT 11 Control or Cylinder Select. This bit is used to indicate the type of function that the bus bits are currently used for. If set, the tag is either control or cylinder select. If reset, this means the tag is for head select. Read-only.
NOTE: It should be obvious that if both bits 10 and 11 are set, then the function must be control select. However, they deemed it necessary to designate bit 13 as the control select indicator. The reason for this is because only one function should be selected at a time. So if you see more than one tag line active at the same time, then one of them must be hung.

BIT 13 Control Tag. Indicates the status of the control select tag line. (See description under bits 10 and 11).

BIT 14 Request $B$. Indicates that a request has been recieved from port B. Read-only.

BIT 15 Request $A$. Indicates that a request has been recieved from port A. Read-only.

RMER2
(776742) 15

| BSE | SKI | OPE | IVC | LSC | LBC | 0 | 0 | DVC | 0 | 0 | 0 | DPE | 0 | 0 | 0 |
| :--- | :--- | :--- | :--- | :--- | :--- | :--- | :--- | :--- | :--- | :--- | :--- | :--- | :--- | :--- | :--- |

BITS 00-02 Not used, always zero.
BIT 03 Data Parity Error. When set, indicates that a parity error has occurred on the syncronous data bus during a data transfer. (That even parity was detected.) DPE also causes PAR in RMERI to set. DPE is a class B error.

BITS 04-06 Not used, always zero.
BIT 07
Device check. Set by the drive as an indication of low AC power or multiple head select failure. DVC is a class B error.

BITS 08-09 Not used, always zero.
BIT 10 Loss of bit clock. Set if no transition of the bit clock (derived from the servo and read clocks) occurs for more than 400 nS . LBC is a class B error.

BIT 11

BIT 12

BIT 13

BIT 14

Loss of system clock. The system clock referred to is the RMA clock which strobes the micro prom sequencer. This bit will be set if the prom states do not change and therefore the clock is dead. LSC is a class B error.

Invalid Command. Set when a command is recieved while Volume Valid or Drive Ready are not set. IVC is a class $B$ error.

Operator plug error. Set when the logical address plug has been removed from the drive. If the plug is removed during a data transfer, it is a class B error. If removed any other time, it is a class A error

Seek Incomplete. Sets if the drive is unable to complete a seek within 500 mS or if the heads move into the inner or outer guard band. In either case, the position of the heads cannot be determined, so you must issue a recalibrate command to get the heads back to zero.

BIT 15
Bad Sector Error. If in checking bits 14 and 15 of the first header word, the drive finds a zero in either, this bit will be set to indicate that this sector has been flagged bad. This is a class B error which will cause termination of a read command after the CRC has been read. This will be a class A error in the case where a read header and data are performed.

RMEC1
(776744) 16

| 0 | 0 | 0 | $P$ | $P$ | $P$ | $P$ | $P$ | $P$ | $P$ | $P$ | $P$ | $P$ | $P$ | $P$ | $P$ |
| :--- | :--- | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :--- | :--- |

BITS 00-12 ECC Position Register. This register gives the binary position of the correctable error burst within the data field just read. A correctable error burst is one in which the total length of the burst in error is not greater than 11 bits. Any errors that occur more than ll bits apart cannot be corrected. This register points to the first bit in error out of a data field 16 bits long by 256.

NOTE:
When a correctable data check occurs, the sector in error has already been transfered to memory. It is the software system which must correct the error in memory. To do this, the software takes the value in the position register and calculates the position of the burst in memory. Then it takes the value from the ECC pattern register and uses it to calculate which bits must be corrected.

RMEC2
(776746) 17

| 0 | 0 | 0 | 0 | 0 | PAT | PAT | PAT | PAT | PAT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |


| PAT | PAT |
| :---: | :---: |
| 6 | 5 |


| PAT | PAT | PAT | PAT |
| :---: | :---: | :---: | :---: |
| 4 | 3 | 2 | 1 |

BITS 00-10 ECC Pattern Register. Contains the actual error burst pattern detected by the ECC logic. Any or all of these 11 bits may be in error so long as there are no errors greater than ll bits.

RMBAE (776750) RH


R/W

BITS 00-05 Bus Address Extension. These extra six address bits would be used by the RH70 to develop the full 22 bit addressing of the PDP $11 / 70$ memory bus.

RMCS3
(776752) RH

| $A P E$ | DPE <br> $H I$ | DPE <br> LO | WCE <br> HI | WCE <br> LO | DBL | 0 | 0 | 0 | IE | 0 | 0 | IPCK | IPCK | IPCK | IPCK |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |

R/W

BITS 00-03 Invert parity check. Setting these bits will cause the parity to be inverted on the associated byte. IPCK $00=$ Byte 00; IPCK $01=$ Byte 01; IPCK 02 = Byte 02 IPCK 03 = Byte 03.

BITS 04-05 Not used.
BIT 06 Interrupt Enable. This bit shadows the interrupt enable bit in RMCSl. They are one and the same. The only difference with this one is that it will allow you to enable interupts on the RH without writing a drive register. (Remember that to set the interupt bit on RMCSI, you will initiate a write to the drive since the function bits are in the same register.)

BITS 07-09 Not used.
BIT 10 Double word. Read-only. Indicates that the data transfer in progress is 32 bits wide. On the PDP 11/70 the RH will transfer two words only if the desired data is on an even boundary in memory. If the data is on an odd boundary or the word count equals one, the RH will transfer 16 bits.

BIT 11

BIT 12

BIT 13

BIT 14

NOTE:

BIT 15

Write check error Even word. When the data word in the RH OBUF (from the disk) did not compare with the word in memory, this bit will set. WCE causes the RHDB to latch the failing word from the disk.

Write check error Odd word. Same as bit ll except error occurred in the odd (Hi) word.

Data Parity Error Even Word. If set, the even word in memory had a data parity error. This condition is checked on a write or a write-check operation.

Data Parity Error Odd Word. Same as bit 13 except odd word.

With either bits 13 or 14 set, the bit UPE will set in RMCS2. Don't forget to concantonate the RMBAE with the RMBA to get the physical address. If the double word bit was set in this register, subtract 4 from the RMBA. If the double bit is not set, subtract 2. This will give you the address of the bad word in memory.

Address Parity Error. If set, an address parity error was detected on the 22 bit address bus. The procedure for finding the bad address is the same as explained in the note above. APE also sets UPE in RMCS2.

VAX-11/780 RMO5 Register summary
RMCS1

| ${ }^{\text {R }} 15$ | 14 | 13 |  | 111 |  | 89 |  | 107 | 06 | 05 |  |  | 02 | 01 | $\infty$ | $\begin{aligned} & \text { BASE } \\ & \text { HFX) } \end{aligned}$ |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| SC | TRE | MCPE | $\emptyset$ | DVA | PSEL |  |  | RDY | IE | F4 | F3 | F2 | FI | F® | G® | 00 |
| RMDS |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ATA | ERR | PIP | MOL | WRL | LBT |  |  | DRY | VV | $\varnothing$ | $\varnothing$ | $\emptyset$ | $\emptyset$ | $\emptyset$ | OM | 04 |
| RMER1 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| DCK | Uns | OPI | DTE | WLE | IAE |  |  | HCE | ECH | Wer | FER | PAR | RMR | ILR | ILF | 08 |
| RMMR1 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  | R-G | EBL | REX | ESBC | Ples | ECRC | RDA | PHA | Cont | wc | EECC | wo | LS | LSIT | DMD |  |
| RMAS |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| $\varnothing$ | $\sigma$ | $\varnothing$ | ø | $\emptyset$ | $\varnothing$ | $\emptyset$ | $\checkmark$ | $\begin{gathered} \text { ATA } \\ 7 \\ \hline \end{gathered}$ | $\begin{gathered} \mathrm{ATAA}^{2} \\ \hline \end{gathered}$ | $\begin{gathered} \text { ATA } \\ 5 \\ \hline \end{gathered}$ | $\begin{gathered} \text { ATA } \\ 4 \end{gathered}$ | $\begin{array}{\|c\|c\|} \hline \text { ATA } \\ \hline \end{array}$ | $\begin{array}{\|c\|} \hline \text { ATA } \\ \hline \end{array}$ | $\begin{gathered} \text { ATA } \\ 1 \end{gathered}$ | $\begin{gathered} \text { ATA } \\ \triangle \\ \hline \end{gathered}$ | 10 |
| RMDA |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| $\varnothing$ | $\varnothing$ | $\varnothing$ | $\begin{array}{\|c\|} \hline \text { TA* } \\ 16 \\ \hline \end{array}$ | $\begin{gathered} \text { TA* } \\ 8 \\ \hline \end{gathered}$ |  | $\begin{array}{\|c} T A \\ 2 \end{array}$ | $\begin{gathered} T A \\ 1 \end{gathered}$ | $\varnothing$ | $\emptyset$ | $\varnothing$ | SA <br> 16 | $\begin{array}{\|c\|} \hline \text { SA } \\ \hline \end{array}$ | $\begin{array}{r} \mathrm{SA} \\ 4 \\ \hline \end{array}$ | $\begin{gathered} \hline 5 A \\ 2 \end{gathered}$ | SA | 14 |
| RMDT |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| $\bigcirc$ | $\varnothing$ | MOH | $\varnothing$ | DRQ | $\varnothing$ | $\varnothing$ | $\begin{array}{\|c} \hline 07 \\ 8 \\ \hline \end{array}$ | $\begin{aligned} & \hline 07 \\ & 7 \\ & \hline \end{aligned}$ | $\begin{array}{\|c\|} \hline D T \\ 6 \\ \hline \end{array}$ | $\begin{array}{\|c\|} \hline 07 \\ 5 \\ \hline \end{array}$ | $\begin{aligned} & \hline{ }^{\prime} \\ & 4 \\ & \hline \end{aligned}$ | $\begin{array}{\|l\|} \hline 0 T \\ 3 \\ \hline \end{array}$ | $\begin{array}{\|c\|} \hline D T \\ 2 \\ \hline \end{array}$ | $\begin{array}{\|c\|c\|c} \hline 0 T \\ \hline \end{array}$ | $\begin{array}{\|l\|} \hline D_{1} \\ \hline \end{array}$ | 18 |
| RMLA |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| $\varnothing$ | $\varnothing$ | 0 | $\varnothing$ | $\triangle$ |  | SC | $\begin{array}{\|c} \hline \mathrm{sc} \\ 4 \end{array}$ | $\begin{array}{\|c\|} \hline s c \\ 2 \\ \hline \end{array}$ | $\begin{array}{\|c} 5 \mathrm{SC} \\ \hline \end{array}$ | $\varnothing$ | $\varnothing$ | $\varnothing$ | $\emptyset$ | $\emptyset$ | $\emptyset$ | 1C |
| RMSN |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  | $\begin{gathered} S N \\ 0 \times 000 \\ \hline 20 \end{gathered}$ | $\begin{aligned} & \hline S N \\ & 2000 \\ & \hline \end{aligned}$ | $\begin{aligned} & \text { SN } \\ & 1000 \\ & \hline \end{aligned}$ | $\begin{aligned} & \text { SN } \\ & 800 \\ & \hline \end{aligned}$ |  |  | SN | $\begin{array}{r} \mathrm{SN} \\ \mathrm{BO} \\ \hline \end{array}$ | [SN <br> 40 | SN <br> 20 | $\begin{aligned} & \hline \mathrm{SN} \\ & 10 \\ & \hline \end{aligned}$ | SN | $\begin{array}{c\|} \hline \text { SN } \\ 4 \\ \hline \end{array}$ | $\begin{gathered} \hline \text { SN } \\ 2 \\ \hline \end{gathered}$ | $\begin{gathered} \hline S N \\ 1 \\ \hline \end{gathered}$ | 20 |
| RMOF |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| $\varnothing$ | $\varnothing$ | $\varnothing$ | $\begin{gathered} F M T \\ 16 \end{gathered}$ | ECI | HCI | $\varnothing$ | $\varnothing$ | $\begin{array}{\|c\|c\|} \hline \text { OFF } \\ \text { DIR } \end{array}$ | $\varnothing$ | $\varnothing$ | $\varnothing$ | $\varnothing$ | $\varnothing$ | $\emptyset$ | $\varnothing$ | 24 |
| RMDC |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| $\varnothing$ | $\varnothing$ | $\varnothing$ | $\varnothing$ | $\varnothing$ | 0 | $\begin{array}{\|c\|} \hline D C \\ 512 \\ \hline \end{array}$ | $\begin{array}{\|l\|} \hline \mathrm{DC} \\ 256 \\ \hline \end{array}$ | $\begin{array}{\|c\|} \hline 10 \\ 128 \\ \hline \end{array}$ | $\begin{array}{\|l\|} \hline 0 C \\ 64 \end{array}$ | $\begin{array}{\|l\|} \hline 00 \\ 32 \\ \hline \end{array}$ | $\begin{aligned} & \hline 0 \\ & 16 \\ & \hline \end{aligned}$ | $\begin{array}{\|c\|} \hline 00 \\ B \\ \hline \end{array}$ | $\begin{array}{\|c\|} \hline 0 \mathrm{C} \\ \hline \end{array}$ | $\begin{array}{\|l\|} \hline 0 \\ 2 \\ \hline \end{array}$ | $\begin{gathered} \hline 0 C \\ 1 \\ \hline \end{gathered}$ | 28 |
| RMHR |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| 0 | $\varnothing$ | $\varnothing$ | $\emptyset$ | $\emptyset$ | Ø | $\emptyset$ | $\varnothing$ | $\varnothing$ | $\varnothing$ | $\varnothing$ | $\varnothing$ | $\varnothing$ | $\emptyset$ | $\varnothing$ | $\emptyset$ | 2 C |
| RMMR2 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| $\begin{gathered} \text { REGG } \\ A \end{gathered}$ | $\begin{array}{\|c} \hline \text { REQ } \\ \mathrm{B} \\ \hline \end{array}$ | TAG | $\begin{array}{\|c\|} \hline \text { TEST } \\ \text { BITT } \\ \hline \end{array}$ | CIC | CIH | $\begin{array}{\|c\|} \hline 88 \\ 9 \end{array}$ | $\begin{array}{\|c\|} \hline 8 B \\ 8 \\ \hline \end{array}$ | $\begin{aligned} & \hline 88 \\ & \hline \end{aligned}$ | $\begin{array}{\|c\|} \hline B 8 \\ 6 \end{array}$ | $\begin{array}{\|c\|} \hline 8 B \\ \hline \end{array}$ | $\begin{aligned} & \hline 8 B \\ & 4 \\ & \hline \end{aligned}$ | $\begin{array}{\|c} \hline 88 \\ 3 \end{array}$ | $\begin{gathered} 86 \\ 28 \\ 2 \end{gathered}$ | $\begin{array}{\|c\|} \hline \mathrm{BB} \\ 1 \end{array}$ | $\begin{array}{\|l\|} \hline 8 B \\ \hline \end{array}$ | 30 |
| RMER2 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| $\emptyset$ | SkI | OPE | IVC | LSC | LBS | $\varnothing$ | $\emptyset$ | DVC | $\varnothing$ | 0 | $\emptyset$ | DPE | $\varnothing$ | $\varnothing$ | $\varnothing$ | 34 |
| RMEC1 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| $\varnothing$ | $\varnothing$ | $\emptyset$ | $9$ | $\begin{aligned} & 2948 \\ & 2084 \\ & \hline \end{aligned}$ | $\left.\right\|_{\|c\|} ^{p} 1624$ | $p_{12}$ | $\begin{array}{\|l\|} \hline{ }^{9} 56 \\ \hline \end{array}$ | $\begin{array}{\|c\|} \hline P \\ \hline 128 \\ \hline \end{array}$ | $\begin{array}{\|c\|} \hline 9 \\ \hline \\ \hline \end{array}$ | $\begin{array}{\|l\|} \hline p \\ \hline 22 \\ \hline \end{array}$ | $\begin{aligned} & \hline p \\ & 16 \end{aligned}$ | P | P | $\begin{array}{\|l\|} \hline p \\ 2 \\ \hline \end{array}$ | P | 38 |
| RMEC2 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| $\varnothing$ | $\emptyset$ | $\varnothing$ | $\varnothing$ | $\varnothing$ | [ PAT | $\left\lvert\, \begin{aligned} & \text { PAT } \\ & 10 \end{aligned}\right.$ | PAT | $\begin{array}{\|c} \hline \text { PAT } \\ \hline \end{array}$ | $\begin{array}{\|l\|} \hline \text { PAT } \\ \hline \end{array}$ | $\begin{gathered} \text { PATT } \\ 6 \\ \hline \end{gathered}$ | $\begin{array}{\|c\|} \hline \text { PAT } \\ 5 \\ \hline \end{array}$ | $\begin{gathered} P R T \\ 4 \end{gathered}$ | $\begin{array}{\|c\|} \hline \text { PAT } \\ \hline \end{array}$ | $\begin{array}{\|c\|} \hline \text { PAT } \\ 2 \end{array}$ | $\begin{gathered} \text { PAT } \\ 1 \end{gathered}$ | 3 C |

VAX 11/780 MBA DEVICE REGISTER ADDRESS CALCULATIONS


MBA REGISTER ADDRESS OFFSETS


Page 17



Data written into the SBI byte counter is copied into the Massbus byte counter. (2's complement of number of bytes to transfer.)


Page 19
(Front View)


RMA Module compatability charts

| MODULE | RM02/03 | RM80 | RM05 |
| :---: | :---: | :---: | :---: |
| M7684 | $C S=R$ | yes | yes |
| $\begin{aligned} & \text { M7685 } \\ & \text { M7685-YA } \\ & \text { M8685 } \end{aligned}$ | $\begin{aligned} & \text { CS = C } \\ & \text { yes } \\ & \text { yes } \end{aligned}$ | $\begin{aligned} & \text { no } \\ & \text { no } \\ & \text { yes } \end{aligned}$ | $\begin{aligned} & \text { no } \\ & \text { CS }=\mathrm{D} \\ & \mathrm{CS}=\mathrm{B} \end{aligned}$ |
| $\begin{aligned} & \text { M7686 } \\ & \text { ** M7686-YA } \end{aligned}$ | $\begin{aligned} & \text { CS = J } \\ & \text { yes } \end{aligned}$ | $\begin{aligned} & \text { yes } \\ & \text { yes } \end{aligned}$ | $\begin{aligned} & \text { no } \\ & \text { yes } \end{aligned}$ |
| M7687 | CS $=C$ | yes | yes |
| M5922 | $C S=E$ | yes | yes |
| M5923 | $C S=E$ | yes | yes |
| 70-13398 <br> Back Plane | $\begin{aligned} & \text { WL }=\mathrm{C} \\ & \text { WT }=\mathrm{D} \end{aligned}$ | $\begin{aligned} & W L=D \\ & W T=E \end{aligned}$ | $\begin{aligned} & W L=D \\ & W T=E \end{aligned}$ |

** If DUAL PORT Switches are located in the slot on the front door M7686-YA must be used.

## RM Adapter Backplane Revision Level:

The following changes have been made to the RM02/03 backplane to make it RM02/03/05/80 compatible.

- For the RM05:

ADD BP 3600 RPM L.................A06K2 to B05P2
For the RM80:


With all 5 wires added, the 'WL' is at a REV 'D' and the 'WT' is at a REV 'E'. This makes the 70-13398 Backplane RMO2/03/05/80 compatible.

In addition to this, the RM80 requires a special jumper on slot 06 of the RMA backplane grounding C06Dl to C06C2. This changes the cylinder address scheme and must be removed for all other drives.

| Coble | Pin* |  | Polerity | Deviramion | Cable | Pin |  | Pobarity | Desteration | Coble | Pr |  | Polarity | Deverantion |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $\begin{gathered} \text { Massuus } \\ \text { Cubte } \end{gathered}$ | A | 1 | - | MASS DOO | $\underset{\substack{\text { Masbus } \\ \text { Cible } \\ \hline}}{ }$ | A | 1 | - | MASS D06 | Massbus Cable C | A | 1 | - | MAsS D12 |
|  | ${ }^{\text {c }}$ | $\frac{1}{3}$ | + | MASS DOI |  | $\stackrel{\text { c }}{ }$ | $\frac{1}{3}$ | $\pm$ | MASSD07 |  | B | 3 | $\pm$ | MASS D13 |
|  |  | 4 |  |  |  | - | 4 | - |  |  | ${ }_{\text {D }}$ | ${ }^{3}$ | - | Mass dia |
|  | E | 6 | + | MASS D02 |  | $\underset{\text { E }}{ }$ | 5 | + | MASS D08 |  | E | 5 | - | MASS D14 |
|  | ${ }^{\text {H }}$ | 7 | + | MASS D03 |  | - | 7 | + | MASS D09 |  | H | $\frac{8}{7}$ | + | MASS DIS |
|  | ${ }^{\text {j }}$ | 8 | - | MASS D04 |  | , | 8 | $\square$ | MASS DIO |  | $\frac{1}{k}$ | 8 |  | MASSDI6 |
|  | $\underline{L}$ | 10 | $+$ |  |  | L | 10 | + |  |  | ${ }_{L}$ | 10 | + | MASS D16 |
|  | N | 111 | + | MASS DOS |  | $\stackrel{\text { M }}{ }$ | 11 | $\pm$ | MASS DII |  | $\stackrel{M}{M}$ | 11 | + | MASS D17 |
|  | P | ${ }_{14}^{13}$ | + | Mass ${ }^{\text {coo }}$ |  | P | $1{ }_{14}^{13}$ | + | MASSCO6 |  | P | 13 | - | MASS DPA |
|  | $\stackrel{1}{s}$ | 15 | + | MASSCOI |  | s | 15 | + | MASSC07 |  | R | 14 | $\pm$ |  |
|  |  | 16 |  |  |  | T | 16 |  |  |  | S | 16 | + | MASSC12 |
|  | U | 18 | + | MASS C02 |  | V | 18 | + | MAss C08 |  | v | 17 | - | MASS C13 |
|  | w | 19 | + | MASS CO3 |  | W | 19 | + | MASS C09 |  | w | 19 | + | MASSC14 |
|  |  |  |  | Masscas |  |  |  |  | ${ }^{\text {mascio }}$ |  | X | 20 | - |  |
|  | 2 | 22 | $+$ | masscou |  | 2 | 22 | + | Masscio |  | z | ${ }_{22}^{21}$ | - | MASSCIS |
|  | ${ }_{\text {A }}^{\text {A }}$ | ${ }_{24}^{23}$ | $\pm$ | MAss cos |  | ${ }_{\text {A }}^{\text {A }}$ | ${ }_{24}^{23}$ | + | MASS ${ }^{\text {C1I }}$ |  | ${ }^{\text {Af }}$ | ${ }^{23}$ | + | MASS CPA |
|  | cr | $2{ }^{25}$ | - | MASS SCLK |  | c | 25 | - | MASS EXC |  | B8 | 24 | - | mass occ |
|  | DD | 26 |  |  |  | DD | 26 | + |  |  | DD | 26 | + |  |
|  | EEf <br> fF | ${ }_{28}^{27}$ | $\pm$ | MASS RS3 |  | 皆 | ${ }_{28}^{27}$ | $\pm$ | MASS RSO |  | EE | 27 | + | MASS DSO |
|  | ${ }_{\text {H }}$ | ${ }_{30}^{29}$ | $\pm$ | MASS ATTN |  | ${ }^{\mathrm{HH}}$ | $\begin{aligned} & \frac{20}{29} \\ & 30 \end{aligned}$ | $\pm$ | MASS EbL |  | H | ${ }^{28}$ | + | MASS TRA |
|  | KK | ${ }^{31}$ | - | MASS RSA |  | ${ }^{\text {KK }}$ | 31 | - | MASS RSI |  | K | 30 |  |  |
|  | L | 32 | $+$ |  |  | $\underline{L}$ | 32 | + |  |  | 4 | 32 | + | MASS DSI |
|  | MM | ${ }_{34}^{33}$ | + | MASS CTOD |  | ${ }_{\text {M }} \mathrm{M}$ | ${ }_{34}^{33}$ | - | MASS RS2 |  | MM | ${ }^{33}$ | - | Mass ds2 |
|  | ${ }_{\text {PP }}^{\text {Pp }}$ | ${ }^{35}$ | $\pm$ | MASS WCLK |  | ${ }_{\text {PP }}$ | ${ }^{35}$ | + | MASS INIT |  | Pp | $3{ }^{34}$ | + | MASS DEM |
|  | RR |  | + | MASS RUN |  | RR | ${ }^{36}$ | $\div$ | MASS SPT |  | RR | 36 | - |  |
|  | TT | 38 | . |  |  | TT | 38 | - |  |  | TT | ${ }_{38}$ | + | MASS SP2 |
|  | W | 39 |  | SPARE |  | W | 39 |  | SPARE |  | U | 39 | H | MASS FAIL |
|  | w | 40 |  | GND | , |  | 40 |  | GND |  |  | 40 |  | GND |
| Cable A Cable B Cable |  |  |  |  |  |  |  |  |  |  |  |  |  |  |


| CD KIT | DESCRIPTION | RM03 DEC \# | BK5B5 \# | RM02 DEC \# | BK8A1 \# |
| :---: | :---: | :---: | :---: | :---: | :---: |
| 03 | Fuse 2A 250V | 29-22872 | 95647602 | same |  |
| 03 | Fuse 6A 250V | 29-22873 | 95647605 | same |  |
| 03 | Fuse 8A 250V | 29-23587 | 95647606 | same |  |
| -- | Magnet Assy | 29-22874 | 47200700 | same |  |
| 03 | HRVV RXer | 29-22875 | 54147709 | same |  |
| * 03 | ASGV Speed detect | 29-23117 | 54152505 | same * (note | 29-22876/6SGV obsolete) |
| 03 | ASHV (BSHV) Power Sup $\pm 5 \mathrm{v}$ | 29-22877 | 54152901 (902) | same | (fuse change only) |
| 03 | 5SJV (ASJV) Power Sup $\pm 42 \mathrm{v}$ | 29-22878 | 54153300 (301) | same | (fuse \& bleader res. change) |
| 03 | 5SKV Power Supply $\pm 20 \mathrm{v}$ | 29-22879 | 54153700 | same |  |
| 03 | JTVV TXer (as HTVV) | 29-22880 | 54167710 | same |  |
| 03/02 | HFRV (JFRV) Fine Servo | 29-22881 | 54226113 | 29-23112 | 54226114 |
| - 03 | EKFV Fault Reg | 29-22882 | 54262105 | same |  |
| 03 | FLPV Servo Control | 29-22883 | 54275307 | same |  |
| (1) 03 | JLQV D/A Converter | 29-22884 | 54275710 | same |  |
| ~ 03/02 | HLRV (LLRV) Data Latch | 29-22885 | 54276108 | 29-23113 | 54276113 |
| N 03/02 | CLSV (BLSV) Write PLO | 29-22886 | 54276503 | 29-23111 | 54276502 |
| 03/02 | ELTV (NLTV) A-Cont/Sect | 29-22887 | 54276906 | 79-23116 | 54276914 |
| 03 | ELUV A-Cont 2 | 29-22838 | 54277306 | same |  |
| 03 | MLVV A-Cont 1 | 29-22889 | 54277713 | same |  |
| 03 | FLWV Diff Generator | 29-22890 | 54278107 | same |  |
| 03 | ELXV NRZ to MFM | 29-22891 | 54278505 | 29-23115 | 54278509 *See attached Tech-Tip. |
| 03/02 | BLZV (CLZV) Read PLO | 29-22892 | 54279303 | 29-23114 | 54279304 |
| -- | Meter Hour 60 HZ | 29-22893 | 94313800 | same |  |
| 03 | FZQN Servo PreAmp | 29-22894 | 73485311 | same |  |
| 03/02 | R/W Head Lower | 29-22895 | 75010102 | 29-23109 | 75010302 |
| 03/02 | R/W Head Upper | 29-22896 | 75010103 | 29-23107 | 75010303 |
| 03/02 | R/W Head Servo | 29-22897 | 75010105 | 29-23108 | 75010305 |
| 03/02 | NZ.JN (SZJN) HD Sel/Amp | 29-22898 | 75061715 | 29-23119 | 75061719 |
| 03/02 | EZKN (DZKN) WR Driver | -29-22899 | 75062107 | 29-23118 | 75062106 |
| -- | Spindle Assy | 29-22900 | 75074714 | 29-23373 | 75074703 |
| 03 | B1ower Assy 60 Hz | 29-22901 | 75240304 | same |  |

RM02/RM03 DEC to CDC Part \#'s cont



[^0]Voltage and Frequency Dependent Components

|  | $\begin{array}{ll}\text { RM03 } & 3600 \mathrm{RPM}=\mathrm{BK} 5 \mathrm{BXX} \\ \text { RM02 } & 2400 \mathrm{RPM}=\mathrm{BK} 8 \mathrm{AXX}\end{array}$ | BK5B5G(120V/60HZ) | BK5B5H ( $240 \mathrm{~V} / 50 \mathrm{HZ}$ ) | BK8AlA (120V/60HZ) | BK8AlB (240V/50HZ) |
| :---: | :---: | :---: | :---: | :---: | :---: |
|  | VARISTOR CDC \# | NONE | 94395600 | NONE | 94395600 |
|  |  | - | - | - | - |
|  | BLOWER ASSEMBLY | 75240304 | 75240305 | 75240304 | 75340305 |
|  |  | 29-22901 | 29-22902 | 29-22901 | 29-22902 |
|  | SOLID STATE SWITCH | 94371305/76427404 | 94376501/76427406 | 94371305/76427404 | 94376501/76427406 |
|  | RUN/START TRIAC | 29-22929 | 29-23313 | 29-22929 | 29-23313 |
|  | HOUR METER | 94313800 | 94313807 | 94313800 | 94313807 |
|  |  | 29-22893 | 29-22924 | 29-22893 | 29-22924 |
|  | TRANSFORMER | 76840400 | 76846800 | 76840400 | 76846800 |
|  |  | 29-22907 | 29-22908 | 29-22907 | 29-22908 |
| $\begin{aligned} & \text { T0} \\ & 00 \\ & 0 \\ & 0 \end{aligned}$ | P.S. CIRCUIT BREAKER | 92696065 | 92696079 | 92696065 | 92696079 |
|  |  | 29-22917 | 29-22918 | 29-22917 | 29-22918 |
|  | MAIN CIRCUIT BREAKER | 94245217 | 94245205 | 94245217 | 94245205 |
| N |  | 29-22922 | 29-22921 | 29-22922 | 29-22921 |
|  | DRIVE BELT | 92314113 | 92314119 | 92314099 | 92314115 |
|  |  | 29-22915 | 29-22916 | 29-23110 | 29-23120 |
|  | DRIVE MOTOR KIT | 47204303 | 47204310 | 47204301 | 47204309 |
|  |  | 29-22911 | 29-22912 | 29-23121 | 29-23122 |
|  | CAP DRIVE MOTOR** | 94255116 | 94255120 SC-27 UP | 94255112 | 94255120 SC-27 UP |
|  |  | 29-22923 | 29-22937 | 29-23137 | 29-22937 |
|  | POWER CABLE | 75259410 | 75259409 | 75259410 | 75259409 |
|  |  | - | - | - | - |
|  | METER MOUNTING PLATE | 75256100 | 75256102 | 75256100 | 75256102 |
|  |  | - | - | - | - |
|  | **CAP DRIVE MOTOR | SC-15 thru SC-19 | $240 \mathrm{~V} / 50 \mathrm{HZ}=94255$ | 09 |  |
|  |  | SC-20 thru SC-26 | $240 \mathrm{~V} / 50 \mathrm{HZ}=94255$ | 01 = DEC \# 29-2358 |  |

> RM05 Branch Spares Kit $(60 \mathrm{~Hz})$
> A2-W0336-10

| SPARES KIT \# | A2-S005l-0 |
| :---: | :---: |
| SPARES KIT \#2 | . A2-S0052-0 |
| SPINDLE ASSEMBLY | 29-23559 |
| ACTIVATOR ASSEMB | 29-23572 |
| BIIOWER ASSEMBLY | 29-23573 |
| DRIVE MOTOR | 29-23574 |
| DATA PACK | 30-17107-00 |
| CE PACK. | 30-17108-00 |

RMA Spares Kit
A2-W0335-10

H7740 POWER SUPPLY..........................................
15 VOLT REGULATOR........................................54-11086

> A2-S0051-0 RM05 Spares Kit \#l

| Vendor PN | DEC PN | Description | Qty. | Unique |
| :---: | :---: | :---: | :---: | :---: |
| 75183604 | 29-23540 | Comp.Assy. Type AzCN | 1 | RM05 |
| 77427502 | 29-23543 | Comp.Assy. Type AYFN | 1 | RM05 |
| 54122900 | 29-23554 | Card Read Amp 4PHV | 1 | RM05 |
| 54123301 | 29-23555 | Card Write Driver 5PJV | 1 | RM05 |
| 54123700 | 29-23556 | Card R/W Control 4PKV | 1 | RM05 |
| 54135308 | 29-23557 | Card Diff \& Head FQPV | 1 | RM05 |
| 54262501 | 29-23558 | Card Access Cont. AKGV | 1 | RM05 |
| 54296505 | 29-23553 | Card Analog Servo DMSV | 1 | RM05 |
| 75054500 | 29-23566 | Card Reg. 5V | 1 | RM05 |
| 75208502 | 29-23568 | Card Serial Head BXGN | 1 | RM05 |
| 75243202 | 29-23569 | Card Servo 5ZGN | 1 | RM05 |
| 54277721 | 29-23577 | Card Access RLVV | 1 | RM05 |
| 54147709 | 29-22875 | Card Channel 1 HRVV | 1 | RM03/5 |
| 54167710 | 29-22880 | Card Channel 2 JTVV | 1 | RM03/5 |
| 54226113 | 29-22881 | Card Fine Servo HFRV | , | RM03/5 |
| 54262105 | 29-22882 | Card Fault EKRV | 1 | RM03/5 |
| 54276108 | 29-22885 | Card Data Latch HLRV | 1 | RM03/5 |
| 54276503 | 29-22886 | Card Write Clock CLSV | 1 | RM03/5 |
| 54276906 | 29-22887 | Card Access Cont ELTV | 1 | RM03/5 |
| 54278107 | 29-22890 | Card Difference FLWV | 1 | RM03/5 |
| 54278505 | 29-22891 | Card NRZ to MFM ELXV | 1 | RM03/5 |
| 54279303 | 29-22892 | Card Read PLO BLZV | 1 | RM03/5 |
| 73385311 | 29-22894 | Card Track Servo FZQN | 1 | RM03/5 |
| 54109701 | 29-22933 | Card Extender | 1 | RM03/5 |

RM05 Absolute Filter 29-23591 Purge all date codes from June l, 1981 to October 3l, 1981 from shelf stock and drives. See Tech Tip at end of Handbook.

A2-s0052-00 RM05 Spares Kit \#2

| Vendor PN | DEC PN | Description | Qty. | Unique |
| :---: | :---: | :---: | :---: | :---: |
| 77427100 | 29-23541 | Comp. Assm. | 1 | RM05 |
| 75010400 | 29-23656 | Head Arm Assm. | 10 | RM05 |
| 75010401 | 29-23657 | Head Arm Assm. | 9 | RM05 |
| 75010409 | 29-23658 | Head Arm Assm. Servo | 1 | RM05 |
| 92314087 | 29-23575 | Belt 60 Hz | 1 | RM05 |
| 92314093 | 29-23584 | Belt 50 Hz | 1 | RM05 |
| 12218425 | 29-13212 | Tool Screwdriver | 1 | RM05 |
| 12263205 | 29-20906 | Tool Torque Wrench | 1 | RM05 |
| 75018400 | 29-22934 | Tool Carriage/Spindle | 1 | RM05 |
| 75018803 | 29-22935 | Tool Head Adj. | 1 | RM05 |
| 87016701 | 29-22936 | Tool Screwdriver |  | RM05 |
| 76422501 | 29-22904 | Cont. Pan. Switch Assm |  | RM03/5 |
|  | A2-W0335-10 | RMA Controller Kit RMO | 3/5 |  |
|  | M5922 | RMA Transciever A | 1 |  |
|  | M5923 | RMA Transciever B | 1 |  |
|  | M7684 | Control Sequencer | 1 |  |
|  | M7685 | Data Sequencer | 1 |  |
|  | M7686 | Control Interface | 1 |  |
|  | M7687 | Drive Data Interface | 1 |  |

RM05 POWER SUPPLY PART NUMBERS

Vendor PN
94376500
94371302
94371301
94355401
76804200
76804000
47317900
50242705
95686701
75183604
77427100
94378200
77427502
92696031
94268303
92696023
92696001
94268308
94245209
94268315
94245211
94313808

Description
Solid State Switch AC 15 Amp
Solid State Switch AC 30 Amp
Solid State Switch AC 15 Amp
Filter Low Leakage
Transformer Ferro 60 Hz
Transformer Ferro 50 Hz
Transformer Assm. $\quad 50 / 60 \mathrm{~Hz}$
Rectifier Bridge
Capacitor 660 VAC
Comp. Assm. Power Amp. Type AZCN
Comp. Assm.Capacitor Board Type 5YEN
Contactor 24 V DC Power
Comp. Assm. Relay Board AYFN
Circuit Breaker . 5 Amp
Circuit Breaker 2 Amp 50 VDC
Circuit Breaker 5 Amp
Circuit Breaker 8 Amp
Circuit Breaker 7 Amp 50 VDC
Circuit Breaker Drive Motor
Circuit Breaker . 375 Amp 250 VAC
Circuit Breaker AC Main Power
Hour Meter 60 Hz

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RSL
Part
Number Description
$B C 06 Y-Y B$
H7440
H766A
H766B
M5922
M6923
M7684
M7686-YA
M7687
M8685
1Ø-16924-0 0
10-17217-00
12-09403-02
12-10719-03
12-11714-00
12-12635-03
12-12635-04
12-12691-00
12-12691-01
12-12691-02
12-12691-0 3
12-12691-94
12-12691-05
12-12691-06
12-12691-07
12-12714-00
12-12714-01
12-12714-02
12-12714-30
12-12714-31
12-12716-Øø
12-14011-00
12-16817-00
12-16870-00
12-17072-00
29-23187-00
54-11086-0 0
54-13596-00
54-13641-00
54-14012-00
70-14038-00
70-14039-00
70-16215-00
70-16225-00
70-16230-00
18 ft. shielded, massbus cable Adapter $+5 v$ regulator
.Power supply, $120 \mathrm{v} / 60 \mathrm{~Hz}$ Power supply, $220 \mathrm{v} / 50 \mathrm{~Hz}$ MASSBUS transceiver A
MASSBUS transceiver $B$
Control sequencer module
Control interface module
Drive interface module
Data sequencer module
Motor start cap, $115 \mathrm{v} . / 60 \mathrm{~Hz}$
Motor start cap, $220 \mathrm{v} . / 50 \mathrm{~Hz}$
Fan, 117 CFM, ball bearing
Fan, 117 VAC, ball bearing
MBA Fan, ll5v., ball bearing
Belt, 60 Hz
Belt, 50 Hz
ID cap ( $0 /$ READY)
ID cap (1/READY)
ID cap (2/READY)
ID cap (3/READY)
ID cap (4/READY)
ID cap (5/READY)
ID cap (6/READY)
ID cap (7/READY)
Switch cap (RUN/STOP)
Switch cap (WRIT PROT)
Switch cap (FAULT)
Switch cap (STAT 1)
Switch cap (STAT 2)
Lamp wedge, 6.3v
Microswitch (lPSA)
Optical switch (speed sensor)
HDA thermal switch
Gas spring
Spares case
MBA, $15 v$ regulator
Read/Write module
Control panel module
Microprocessor module (DCL)
26 - Pin Cable
60 - Pin Cable
Brush ground assembly
Head disk assembly (HDA)
Wing pivot assembly

RSL CON'T

| 70-16723-ø0 | $115 \mathrm{v} / 60 \mathrm{~Hz}$ motor brake as |
| :---: | :---: |
| 70-16723-01 | $220 \mathrm{v} / 50 \mathrm{~Hz}$ motor brake assy |
| 70-16724-0ø | Actuator assembly (BTRM) |
| 70-16732-00 | Logic D.C. power cable |
| 70-16733-00 | Logic A.C. harness assembly |
| -70-16735-00 | Servo preamp cable assembly |
| -70-16737-0. | 40 conductor data cable (person) |
| 70-16737-01 | 40 conductor data cable (servo) |
| 70-16738-00 | 20 conductor data cable (person) |
| 70-16738-01 | $2 \emptyset$ conductor data cable (R/W) |
| -70-16739-00 | $5 \emptyset$ conductor read/write cable |
| 70-16740-00 | Control panel cable assembly |
| 70-16742-60 | Shock mount assembly |
| 70-16975-00 | Personality module/stiffer |
| 70-16976-00 | Servo module/stiffner |
| -70-16978-00 | 26 conductor I/O cable (top half cable) |
| -70-16979-00 | 60 conductor I/O cable (top half cable) |
| 70-16980-00 | Belt tension SW assembly |
| 70-17335-60 | Line cord assembly $115 \mathrm{v} / 60 \mathrm{~Hz}$ |
| 70-17335-01 | Line cord assembly $220 \mathrm{~V} / 50 \mathrm{~Hz}$ |
| 74-22440-0日 | Motor tension spring |
| 74-22816-00 | Foam Air filter (front bezel) |

ARL
Part
Number
54-13596
54-14012
70-16225
70-16975
70-16976
H766A
H766B
M5922
M5923
M7684
M8685
M7686-YA
H7440
Description
Read/write module
Microprocessor module
HDA
Personality/stiffener
Servo/stiffener
Power supply - 60 Hz
Power supply - 50 Hz
MASSBUS transceiver A
MASSBUS transceiver $B$
Control sequencer
Data sequencer
Control interface
$+5 v$ regulator

RM80 Adder Branch Spares Kit - 50 Hz - EUR (A2-W0445-11)
Same as US Area Kits with the following exception:
H766-B Power Supply at 746.24 vs H766-A
RM8日 Generic Branch Spares Kit - 60HZ - USA (A2-Wø444-10)

| Part | Description | Std. |
| :--- | :--- | :--- |
| Number | Cost |  |


| 12-12635-03 | Belt, 60 Hz | 1 | 2.19 |
| :---: | :---: | :---: | :---: |
| 12-14011-00 | Microswitch | 1 | 1.01 |
| 12-16817-00 | Speed Sensor | 1 | 8.38 |
| 29-23187-00 | Spares Case | 1 | 61.75 |
| 54-13596-00 | Read/write module | 1 | 92.18 |
| 70-16215-00 | Brush ground assemblies | 2 | 23 |
| 70-16225-00 | HDA | 1 | 3,127.62 |
| 70-16723-00 | Motor brake assembly | 1 | 161.68 |
| 70-16976-00 | Servo/stiffener | 1 | 260.39 |
| 74-22440-ø0 | Motor tension springs | 2 | . 11 |
| 74-22816-00 | Air filters | 2 | 1.00 |

RM80 Generic Branch Spares Kit - 50HZ - EUR (A2-W0444-11)
Same as US Area Kits with following exceptions:

```
12-12635-04 Belt, 50 HZ at $3.83 vs 12-12635-03
70-16723-01 Motor Break Assembly at $168.83 vs 70-16723-00
```

| RM80 Adder Branch Spares Kit -60 HZ | - USA $-(A 2-W 0445-10)$ |  |
| :--- | :---: | :---: | :---: |
| Part |  |  |
| Number $\quad$ Description | Qty | Cost |


| H766-A | Power Supply | 1 | 745.74 |
| :--- | :--- | :--- | ---: |
| $12-12691-\emptyset \emptyset$ | ID Cap ( $/$ Ready) | 5 | .70 |
| $12-12691-\emptyset 1$ | ID Cap (1/Ready) | 5 | .92 |
| $12-12691-\emptyset 2$ | ID Cap (2/Ready) | 5 | .93 |
| $12-12691-\emptyset 3$ | ID Cap (3/Ready) | 5 | .88 |
| $12-12691-\emptyset 4$ | ID Cap (4/Ready) | 5 | .93 |
| $12-12691-\emptyset 5$ | ID Cap (5/Ready) | 5 | .93 |
| $12-12691-\emptyset 6$ | ID Cap (6/Ready) | 5 | .69 |
| $12-12691-\emptyset 7$ | ID Cap (7/Ready) | 5 | .69 |
| $54-13641-\emptyset \emptyset$ | Control panel assy | 1 | 45.15 |
| $54-14 \emptyset 12-\emptyset \emptyset$ | Microprocessor module | 1 | 261.55 |
| $7 \emptyset-16975-\emptyset \emptyset$ | Personality/stiffener | 1 | 124.11 |
|  |  |  | $\$ 1,183.22$ |





> "A" CABLE

BY: Greg Ekholm

| +Unit Select Tag | 52 | (+Plug Valid) |
| :---: | :---: | :---: |
| $\bigcirc$ - Unit Select Tag | 22 | (-Plug Valid) |
| $(\rightarrow)+U n i t$ Select Bit 0 | 53 | (+Select Add 1) |
| ( $\rightarrow$-Unit Select Bit 0 | 23 | (-Select Add 1) |
| $\rightarrow$ +Unit Select Bit 1 | 54 | (+Select Add 2) |
| -Unit Select Bit 1 | 24 | (-Select Add 2) |
| ( + Unit Select Bit 2 | 56 | (+Select Add 4) |
| $(\rightarrow)$-Unit Select Bit 2 | 26 | (-Select Add 4) |
| +Unit Select Bit 3 | 57 | (+Sector Cnt 1) |
| $\rightarrow-$ Unit Select Bit 3 | 27 | (-Sector Cnt 1) |
| +Tag 1 | 31 |  |
| -Tag 1 | 1 |  |
| +Tag 2 | 32 |  |
| -Tag 2 | 2 |  |
| +Tag 3 | 33 |  |
| -Tag 3 | 3 |  |
| +Bit 0 | 34 |  |
| -Bit 0 | 4 |  |
| +Bit 1 | 35 |  |
| -Bit 1 | 5 |  |
| +Bit 2 | 36 |  |
| -Bit 2 | 6 |  |
| +Bit 3 | 37 |  |
| -Bit 3 | 7 |  |
| +Bit 4 | 38 |  |
| -Bit 4 | 8 |  |
| +Bit 5 | 39 |  |
| -Bit 5 | 9 |  |
| +Bit 6 | 40 |  |
| -Bit 6 | 10 |  |
| +Bit 7 | 41 |  |
| -Bit 7 | 11 |  |
| +Bit 8 | 42 |  |
| -Bit 8 | 12 |  |
| +Bit 9 | 43 |  |
| -Bit 9 | 13 |  |
| topen Cable Detect | 44 | (+Sector Cnt 2) |
| -Open Cable Detect | 14 | (-Sector Cnt 2) |
| +Index | 48 |  |
| - Index | 18 |  |
| +Sector | 55 |  |
| -Sector | 25 |  |
| +Fault | 45 |  |
| -Fault | 15 |  |
| +Seek Error | 46 |  |
| -Seek Error | 16 |  |
| +On Cylinder | 47 |  |
| -On Cylinder | 17 |  |
| +Unit Ready | 49 |  |
| -Unit Ready | 19 |  |
| +Address Mark | 50 | (+Sector Cnt 4) |
| -Address Mark | 20 | (-Sector Cnt 4) |
| +Write Protect | 58 |  |
| -Write Protect | 28 |  |
| - Power Sequence Hold | 59 |  |
| -Sequence Pick In | 29 |  |
| SPARE | 51 | (+Sector Cnt 8) |
| SPARE | 21 | (-Sector Cnt 8) |
| SPARE | 60 | (+Sector Cnt 16) |
| SPARE | 30 | (-Sector Cnt 16) |

＂B＂CABLE

|  | Ground | 1 |  |  |
| :---: | :---: | :---: | :---: | :---: |
|  | －Servo Clock | 2 |  |  |
|  | ＋Servo Clock | 14 |  |  |
|  | Ground | 15 |  |  |
|  | －Read Data | 3 |  |  |
|  | ＋Read Data | 16 |  |  |
|  | Ground | 4 |  |  |
|  | －Read Clock | 5 |  |  |
|  | ＋Read Clock | 17 |  |  |
|  | Ground | 18 |  |  |
|  | －Write Clock | 6 |  |  |
|  | ＋Write Clock | 19 |  |  |
|  | Ground | 7 |  |  |
|  | －Write Data | 8 |  | H |
|  | ＋Write Data | 20 |  | 合 |
| $\underset{~}{\text { 品 }}$ | Ground | 21 |  |  |
| 句 | －Unit Selected | 22 | （－Sector 30＋32） | 是 |
| O | ＋Unit Selected | 9 | （＋Sector 30＋32） |  |
| 3 | －Seek End | 10 | （－Start Enable） |  |
| 0 | ＋Seek End | 23 | （＋Start Enable） |  |
|  | Ground | 11 |  |  |
|  | Spare | 12 |  |  |
|  | （ Spare | 24 |  |  |
|  | （ $\rightarrow$ Ground | 25 |  |  |
|  | Spare | 13 | （＋Initialize） |  |
|  | Spare | 26 | （－Initialize） |  |

SMD INTERFACE（ DEC＂MBA＂LINES）

BY：Greg Ekholm

```
RM80 HDA Assembly
(Bottom View)
```




Operator Control panel Fault Display Codes


The indicator state will be the same as it was before the FAULT switch was pushed.


RM02/03/05/80 Documentation
RM02/03 Documentation

| RM02 Disk Drive Technical Manual - Volume I | (EK-1RM02-TM)* |
| :--- | :--- |
| RM02 Disk Drive Technical Manual - Volume II (RM02 Print Set) | (EK-2RM02-TM) |
| RM03 Disk Drive Technical Manual - Volume I | (EK-1RM03-TM)* |
| RM03 Disk Drive Technical Manual - Volume II (RM03 Print Set) | (EK-2RM03-TM) |
| RM02/03 Disk Subsystem User's Guide | (EK-RM03-UG) |
| RM02/03 Adapter Technical Description Manual | (EK-RM023-TD)* |
| RM02 Disk Subsystem Illustrated Parts Breakdown | (EK-RM02-IP)* |
| RM03 Disk Subsystem Illustrated Parts Breakdown | (EK-RM03-IP)* |
| RM02 Field Maintenance Customer Print Set (Adapter Print Set) | (MP-00456) |
| RM03 Field Maintenance Customer Print Set (Adapter Print Set) | (MP-00350) |

*These documents are also available on microfiche. Order as EP-XXXXX-XX.


Title
RM8ø Disk Drive Technical Description Manual
RM8ø Pocket Service Guide
RM8ø Disk Drive User's Guide
RM8ø Disk Drive Illustrated Parts Breakdown
RM8ø Disk Drive Field Service Maintenance Print set

RM8ø Disk Drive Service Manual
RM8ø Disk Drive Technical Manual
RM Adapter Technical Description Manual

## Supporting Documentation for RH70 \& RH780

| EK-RWPø4-MM | RWP@4 Disk Subsystem Maintenance Manual |
| :---: | :---: |
| EY-D3038-SP | RH11/RH70 MASSBUSS Controllers Self-Paced Course |
| EK-RH780-TD | RH780 Technical Description Manual |
| EK-DS780-UG | VAX $11 / 780$ Diagnostic System User's Guide |

## RM02/03/05/80 Documentation

Title
RMO5 Disk Drive User's Guide (Ships with the drive)
RMO5 Disk Drive Service Manual
RM05 Disk Drive Maintenance Print Set
(Ships with the drive.)
BK7BlE/F Disk Drive Maintenance Print Set
RM05 Disk Drive Illustrated Parts Breakdown
Dec Part Number
EK-ORM05-UG EP-ORMO5-SV * MP-01075 ER-BK7BI-MP EP-0016A-IP * BK7BlE/F Disk Drive Illustrated Parts Breakdown ER-BK7Bl-IP BK7BlE/F Disk Drive Technical Description ER-BK7Bl-TD * RM Massbus Adapter Technical Description EK-RMADA-TD *
*Available on micro-fiche, order as EP-XXXXX-XX except the RM05 IPB which is EP-ORM05-IP.

With the introduction of the $50 \mathrm{~Hz} \mathrm{RMO5} \mathrm{and} \mathrm{the} \mathrm{new} \mathrm{power}$ supplies, some of the above documentation may be changed or added to.

## RM02/03 Specifications

| Specification | Limit |  |
| :---: | :---: | :---: |
| Seek Time | RM03 | RM02 |
| Maximum seek (822 cylinders) | 55 ms | 55 ms |
| One cylinder seek (maximum) | 6 ms | 6 ms |
| Average seek | 30 ms | 30 ms |
| Seek to the same cylinder | $37.5 \mu \mathrm{~s}$ | $37.5 \mu \mathrm{~s}$ |
| Latency |  |  |
| Speed | $3600 \mathrm{rev} / \mathrm{min}$ | $2400 \mathrm{rev} / \mathrm{min}$ |
| Maximum latency | 17.3 ms | 25.9 ms |
| Average latency | 8.33 ms | 12.5 ms |
| Start/Stop time |  |  |
| Start (maximum) | 35 s | 25 s |
| Start (typical) | 25 s | 15 s |
| Stop (with power) (maximum) | 35 s | 20 s |
| Stop (with power) (typical) | 25 s | 10 s |
| Stop (without power) | 120 s | 60 s |
| Heads |  |  |
| Servo head | 1 | 1 |
| Read/write heads | 5 | 5 |
| Data Rates |  |  |
| Bit cell time | 103.3 ns | 155.0 ns |
| Word rate (16-bit) | $1.65 \mu \mathrm{~s}$ | 2.48 ¢ ${ }^{\text {s }}$ |
| Word rate (18-bit) | $1.86 \mu \mathrm{~s}$ | $2.79 \mu \mathrm{~s}$ |
| Bit rate | 9.677 MHz | 6.45 MHz |
| No. of Addressable Registers in RM02/03 Adapter | 16 | 16 |
| Error Detection/Correction | 32-bit ECC/sector | 32-bit ECC/sector |
| Time for Correction | 4.47 ms , maximum | 5.96 ms , maximum |
| Environmental LimitsTemperature |  |  |
|  |  |  |
| Operating | $15.0^{\circ}$ to $32.2^{\circ} \mathrm{C}(5$ of $6.7^{\circ} \mathrm{C}\left(12^{\circ} \mathrm{F}\right)$ | F) with a maximum gradient |
| Non-operating | $-40^{\circ}$ to $66^{\circ} \mathrm{C}\left(-40^{\circ}\right.$ of $14^{\circ} \mathrm{C}\left(25^{\circ} \mathrm{F}\right) \mathrm{p}$ | F) with a maximum gradient |

RM02/03 Specifications (Cont)

| Specification | Limit |  |
| :---: | :---: | :---: |
| Relative humidity |  |  |
| Operating | 20 to 80 percent (providing there is no condensation) |  |
| Non-operating | 5 to 95 percent (providing there is no condensation) |  |
| Altitude |  |  |
| Operating | $305 \mathrm{~m}(1000 \mathrm{ft})$ below sea level to $2000 \mathrm{~m}(6500 \mathrm{ft})$ above sea level. |  |
| Non-operating | $305 \mathrm{~m}(1000 \mathrm{ft})$ below sea level to $4572 \mathrm{~m}(15,000 \mathrm{ft})$ above sea level. |  |
| Electrical | RM03 | RM02 |
| Voltages available (single-phase) | $\begin{aligned} & 100 \mathrm{Vac}+10,-10 ; 60 \mathrm{~Hz} \\ & 120 \mathrm{Vac}+8,-18 ; 60 \mathrm{~Hz} \\ & 240 \mathrm{Vac}+17,-27 ; 50 \mathrm{~Hz} \end{aligned}$ | $\begin{aligned} & 100 \mathrm{Vac}+10,-10 ; 60 \mathrm{~Hz} \\ & 120 \mathrm{Vac}+8,-18 ; 60 \mathrm{~Hz} \\ & 240 \mathrm{Vac}+17,-27 ; 50 \mathrm{~Hz} \end{aligned}$ |
| Start current for: |  |  |
| $100 \mathrm{Vac}, 60 \mathrm{~Hz}$ | 33 Arms , maximum | TBS |
| $120 \mathrm{Vac}, 60 \mathrm{~Hz}$ | 30 A rms , maximum | TBS |
| $240 \mathrm{Vac}, 50 \mathrm{~Hz}$ | 22 Arms , maximum | TBS |
| $100 \mathrm{Vac}, 50 \mathrm{~Hz}$ | 33 A rms, maximum | TBS |
| Line current |  |  |
| Disk and carriage in motion | Total | Total |
| $100 \mathrm{Vac}, 60 \mathrm{~Hz}$ | 11 A rms | TBS |
| $120 \mathrm{Vac}, 60 \mathrm{~Hz}$ | 11 Arms | TBS |
| $240 \mathrm{Vac}, 50 \mathrm{~Hz}$ | 7 Arms | TBS |
| $100 \mathrm{Vac}, 50 \mathrm{~Hz}$ | 14 A rms | TBS |
| In standby mode |  |  |
| $100 \mathrm{Vac}, 60 \mathrm{~Hz}$ | 4.5 A rms | TBS |
| 120 Vac, 60 Hz | 4.5 A rms | TBS |
| $240 \mathrm{Vac}, 50 \mathrm{~Hz}$ | 3.5 A rms | TBS |
| $100 \mathrm{Vac}, 50 \mathrm{~Hz}$ | 7 A rms | TBS |
| Line Cord Length | $213.4 \mathrm{~cm}(7 \mathrm{ft})$ | 213.4 cm (7 ft) |
|  |  |  |
| $100 \mathrm{~V} / 60 \mathrm{~Hz}$ | NEMA 5-15 P | NEMA 5-15 P |
| $120 \mathrm{~V} / 60 \mathrm{~Hz}$ | NEMA 5-15 P | NEMA 5-15 P |
| $240 \mathrm{~V} / 50 \mathrm{~Hz}$ | NEMA 6-15 P | NEMA 6-15 P |
| $100 \mathrm{~V} / 50 \mathrm{~Hz}$ | NEMA 5-15 P | NEMA 5-15 P |
| Disk Cartridge Type | RM03P | RM03P |

Table 1-8 RM03P Disk Pack Specifications

| Specification | Limits |
| :---: | :---: |
| Type | 9877 disk pack |
| Disk Diameter | 35.56 cm (14 in) |
| Number of Disks | 5 (the upper and lower disks are not used for recording) |
| Number of Recording Surfaces | $5 \mathrm{read} / \mathrm{write}$ and 1 read-only servo surface |
| Cylinders per Disk Pack | 823 |
| Total Number of Tracks | 4115 per disk pack |
| Tracks per Cylinder | 5 |
| Bad Sector File | Cylinder 822, track 4 |
| Environmental Requirements Temperature range (operating) | $10^{\circ}$ to $57^{\circ} \mathrm{C}\left(50^{\circ}\right.$ to $\left.135^{\circ} \mathrm{F}\right)$; temperature change rate not to exceed $0.1^{\circ} \mathrm{C}\left(0.2^{\circ} \mathrm{F}\right)$ per minute. |
| Temperature range (non-operating) | $-40^{\circ}$ to $65^{\circ} \mathrm{C}\left(-40^{\circ}\right.$ to $\left.150^{\circ} \mathrm{F}\right)$; temperature change rate not to exceed $14^{\circ} \mathrm{C}\left(25^{\circ} \mathrm{F}\right)$ per hour. |
| Relative Humidity <br> Operating and non-operating | 8 to 80 percent |
| Wet Bulb Reading Operating Non-operating | $25^{\circ} \mathrm{C}\left(78^{\circ} \mathrm{F}\right)$, maximum $30^{\circ} \mathrm{C}\left(85^{\circ} \mathrm{F}\right)$, maximum |
| Altitude Operating Non-operating | Mean sea level to $3050 \mathrm{~m}(10,000 \mathrm{ft})$ <br> Mean sea level to $12,190 \mathrm{~m}(40,000 \mathrm{ft})$ |
| Stray magnetic fields Operating and non-operating | Not to exceed 50 oersteds |

## RM02/RM03 OPTIONS

The RM02/03 options are specified, according to their power requirements and their number of access ports. Table 1-9 shows what options are currently available.

RM02/03 Options

| RM02/03 Single-Port Options |  |
| :--- | :---: |
| RM02-AA or RM03-AA | $120 \mathrm{~V} / 60 \mathrm{~Hz}$ |
| RM02-AD or RM03-AD | $240 \mathrm{~V} / 50 \mathrm{~Hz}$ |
| RM02-AE or RM03-AE | $100 \mathrm{~V} / 60 \mathrm{~Hz}$ |
| RM02-AF or RM03-AF | $100 \mathrm{~V} / 50 \mathrm{~Hz}$ |
| RM02/03 Dual-Port Options |  |
| RM02-BA or RM03-BA |  |
| RM02-BD or RM03-BD | $120 \mathrm{~V} / 60 \mathrm{~Hz}$ |
| RMo2-BE or RM03-BE | $240 \mathrm{~V} / 50 \mathrm{~Hz}$ |
| RM02-BF or RM03-BF | $100 \mathrm{~V} / 60 \mathrm{~Hz}$ |

NOTE
A single-port drive is field-upgradable to dual-port capabilities.

RM03P Pack Capacity Allocation

| Data Word Format | 18-Bit Format | 16-Bit Format |
| :--- | :--- | :--- |
| No. of Sectors/ <br> Data Track | 30 sectors | 32 sectors |
| Bits/Sector | 5,376 bits/sector | 4,864 bits/sector |
| Total Formatted Capacity <br> (See Note 1.) | $663,667,200$ bits/pack | $640,491,520$ bits/pack |
| Formatted Data <br> (See Note 2.) | $568,857,600$ data <br> bits $/$ pack | $539,361,280$ data <br> Total Number of Words <br> (See Note 3.) |

## NOTES

1. (Bits/sector) $\times($ sectors $/$ track) $\times(5$ tracks/cylinder) $\times(823$ cylinders/pack) $=$ Bits/pack
2. (Bits/data word) $\times$ ( 256 words $/$ sector $) \times$ (sectors $/$ track $) \times(5$ tracks $/$ cylinder $) \times(823$ cylinders/pack) $=$ Formatted data word bits/pack
3. (Formatted data word bits) $\div$ (bits/word) $=$ Words/pack

## DRIVE SPECIFICATIONS

The RM05 Disk Drive must operate in a Class A computer room environment. Performance, power, environmental, and physical specifications for the drive are listed in Table 1-6. The specifications for the disk pack are provided in Table 1-7.

RM05 Specifications

| Characteristic | Specification |
| :--- | :--- |
| Seek time |  |
| Maximum seek (822 cylinder) | 55 ms |
| One cylinder seek (maximum) | 6 ms |
| Average seek | 30 ms |
| Seek to the same cylinder | $4 \mu \mathrm{~s}$ |
| Latency |  |
| Speed | $3600 \mathrm{r} / \mathrm{min}$ |
| Maximum latency | 17.3 ms |
| Average latency | 8.33 ms |
| Start/stop time |  |
| Start (maximum) | 35 s |
| Start (typical) | 25 s |
| Stop (with power) (maximum) | 35 s |
| Stop (with power) (typical) | 25 s |
| Stop (without power) | 120 s |
|  |  |
| Heads |  |
| Servo head | 1 |
| Read/write heads | 19 |
| Data rates |  |
| Bit cell time |  |
| Word rate | 103.3 ns |
| Number of addressable | $1.65 \mu \mathrm{~s}$ |
| registers in RM05 adapter |  |
| Error detection/correction | 16 |
| Time for error correction | 4.47 ms, maximum |

## RM05 Specifications (Cont)

| Characteristic | Specification |
| :---: | :---: |
| Environmental limits |  |
| Temperature |  |
| Operating: | $15.0^{\circ}$ to $32.2^{\circ} \mathrm{C}\left(59^{\circ}\right.$ to $\left.90^{\circ} \mathrm{F}\right)$ with a maximum gradient of $6.7^{\circ}$ $\mathrm{C}\left(12^{\circ} \mathrm{F}\right)$ per hour. |
| Non-operating: | $-40^{\circ}$ to $70.0^{\circ} \mathrm{C}\left(-40^{\circ}\right.$ to $158^{\circ}$ <br> F) with a maximum gradient of $20^{\circ} \mathrm{C}\left(36^{\circ} \mathrm{F}\right)$ per hour. |
| Relative humidity |  |
| Operating: | 20 to 80 percent (providing there is no condensation) |
| Non-operating: | 5 to 95 percent (providing there is no condensation) |
| Altitude |  |
| Operating: | $305 \mathrm{~m}(1000 \mathrm{ft})$ below sea level to $2000 \mathrm{~m}(6500 \mathrm{ft})$ above sea level |
| Non-operating: | $305 \mathrm{~m}(1000 \mathrm{ft})$ below sea level to $4572 \mathrm{~m}(15,000 \mathrm{ft})$ above sea level |
| Electrical |  |
| Voltages available (Drive) | $\begin{aligned} & 208 \mathrm{~V}(+14.6,-29.0), 60 \mathrm{~Hz} \\ & 230 \mathrm{~V}(+14.5,-32.0), 60 \mathrm{~Hz} \\ & 220 \mathrm{~V}(+15.0,-25.0), 50 \mathrm{~Hz} \\ & 240 \mathrm{~V}(+17.0,-27.0), 50 \mathrm{~Hz} \end{aligned}$ |
| Voltages available (Adapter) | $\begin{aligned} & 120 \mathrm{~V}(+8.0,-8.0), 60 \mathrm{~Hz} \\ & 220 \mathrm{~V}(+15.0,-25.0), 50 \mathrm{~Hz} \\ & 240 \mathrm{~V}(+17.0,-27.0), 50 \mathrm{~Hz} \end{aligned}$ |
| Start current | $208 \mathrm{Vac}, 60 \mathrm{~Hz}$ @ 39.0 A rms max $230 \mathrm{Vac}, 60 \mathrm{~Hz}$ @ 40.0 A rms max $220 \mathrm{Vac}, 50 \mathrm{~Hz}$ @ 40.0 A rms max $240 \mathrm{Vac}, 50 \mathrm{~Hz}$ @ 41.0 A rms max |

## RM05 Specifications (Cont)

| Characteristic | Specification |
| :---: | :---: |
| Line current |  |
| Disk and carriage in motion | $208 \mathrm{Vac}, 60 \mathrm{~Hz}$ @ 8.0 A rms max $230 \mathrm{Vac}, 60 \mathrm{~Hz} @ 7.2 \mathrm{~A}$ rms max $220 \mathrm{Vac}, 50 \mathrm{~Hz}$ @ 9.5 A rms max $240 \mathrm{Vac}, 50 \mathrm{~Hz}$ @ 8.7 A rms max |
| Disk not in motion | $208 \mathrm{Vac}, 60 \mathrm{~Hz}$ @ 2.0 A rms max $230 \mathrm{Vac}, 60 \mathrm{~Hz}$ @ 1.8 A rms max $220 \mathrm{Vac}, 50 \mathrm{~Hz} @ 2.5 \mathrm{~A}$ rms max $240 \mathrm{Vac}, 50 \mathrm{~Hz} @ 2.3 \mathrm{~A}$ rms max |
| Adapter | $120 \mathrm{Vac}, 60 \mathrm{~Hz} @ 2.1 \mathrm{~A}$ rms max $220 \mathrm{Vac}, 50 \mathrm{~Hz}$ @ 1.3 A rms max $240 \mathrm{Vac}, 50 \mathrm{~Hz}$ @ 1.4 A rms max |
| Line cord length | 366 cm ( 12 ft ) |
| Disk cartridge type | RM05P |
| Weight |  |
| RM05 drive and cabinet | 249 kg (550 lbs) |
| Adapter cabinet With one adapter With two adapters | $54 \mathrm{~kg}(120 \mathrm{lbs})$ <br> 91 kg (200 lbs) <br> $127 \mathrm{~kg}(280 \mathrm{lbs})$ |
| AC plug types |  |
| RM05 drive 120 volt 60 Hz 208 volt 50 Hz | NEMA L6-20P <br> Not shipped |
| Adapter <br> 120 volt 60 Hz <br> 208 volt 50 Hz | NEMA 5-15P <br> NEMA 6-15P |

RM05P Disk Pack Specifications

| Characteristic | Specification |
| :--- | :--- |
| Disk Diameter | $35.56 \mathrm{~cm}(14 \mathrm{in})$ |
| Number of disks | 12 (the upper and lower disks |
|  | are not used for recording) |


| Characteristic | Specification |
| :---: | :---: |
| Number of recording surfaces | $19 \mathrm{read} / \mathrm{write}$ and one read-only servo surface |
| Cylinders per disk pack | 823 |
| Total number of tracks | 15,637 per disk pack |
| Tracks per cylinder | 19 |
| Tracks per inch | 384 |
| Bad sector file | Cylinder 822, track 18 |
| Environmental requirements |  |
| Temperature range |  |
| Operating: | $10^{\circ}$ to $57^{\circ} \mathrm{C}\left(50^{\circ}\right.$ to $\left.135^{\circ} \mathrm{F}\right)$; temperature change rate not to exceed $0.1^{\circ} \mathrm{C}\left(0.2^{\circ} \mathrm{F}\right)$ per minute |
| Non-operating: | $-40^{\circ}$ to $65^{\circ} \mathrm{C}\left(-40^{\circ}\right.$ to $\left.150^{\circ} \mathrm{F}\right)$; temperature change rate not to exceed $14^{\circ} \mathrm{C}\left(25^{\circ} \mathrm{F}\right)$ per hour |
| Relative humidity |  |
| Operating and non-operating: | 8 to 80 percent |
| Wet bulb reading |  |
| Operating: | $25^{\circ} \mathrm{C}\left(78^{\circ} \mathrm{F}\right)$, maximum |
| Non-operating: | $30^{\circ} \mathrm{C}\left(85^{\circ} \mathrm{F}\right)$, maximum |
| Altitude |  |
| Operating: | Sea level to $3,050 \mathrm{~m}(10,000$ ft) |
| Non-operating: | Sea level to $12,190 \mathrm{~m}(40,000$ ft) |
| Stray magnetic fields |  |
| Operating and non-operating: | Not to exceed 50 oersteds |

Drive Power Consumption Requirements

| Input <br> Voltage | Unit <br> Status | Line <br> Current |  | Consumption * <br> Kw |  |
| :--- | :--- | :--- | :--- | :--- | :--- |
| $208 \mathrm{VT}, 60 \mathrm{~Hz}$ | Disks and | 8.0 A | 1.20 | 4200 | Power <br> Factor |
| $230 \mathrm{~V}, 60 \mathrm{~Hz}$ | carriage | 7.2 A | 1.20 | 4200 | .70 |
| $220 \mathrm{~V}, 50 \mathrm{~Hz}$ | in motion | 9.5 A | 1.30 | 4200 | .70 |
| $240 \mathrm{~V}, 50 \mathrm{~Hz}$ |  | 8.7 A | 1.30 | 4200 | .70 |
|  |  |  |  |  |  |
| $208 \mathrm{~V}, 60 \mathrm{~Hz}$ | Disks not | 2.0 A | 0.40 | 1400 | .90 |
| $230 \mathrm{~V}, 60 \mathrm{~Hz}$ | in motion | 1.8 A | 0.40 | 1400 | .90 |
| $220 \mathrm{~V}, 50 \mathrm{~Hz}$ |  | 2.5 A | 0.50 | 1750 | .90 |
| $240 \mathrm{~V}, 50 \mathrm{~Hz}$ |  | 2.3 A | 0.50 | 1750 | .90 |

*These are maximum values.

## SECTION TWO

RM02/03/05 Checks
And Adjustments
1.) Remove $A C$ power from the drive, diconnect the $A$ and $B$ cables running to the drive. Connect the $A$ and $B$ cables from the FTU to the drive. See figure 1.
2.) Install the HFSV card in the drive's logic chassis at location A02. See figure 2.
3.) Install the head alignment cable between the drive's logic backplane and the jack on the $R / W$ module as specified in figure 3.
4.) Connect the test leads between the HFSV card and the null meter on the FTU panel. Observe polarity. See figure 2.
5.) Set switches on FTU as indicated in figure 4.
6.) Apply AC power to the drive.
7.) Turn on the FTU.
8.) Install CE pack, write protect the drive.
9.) Connect the oscilloscope to head alignment card test point $Y$.
10.) Make drive under test ready.

NOTE
In order to ensure accuracy during head alignment, it is important that the drive, CE pack, and FTU be at normal operating temperature. This requires that all three be connected and allowed to run for at least 60 minutes. If a second drive is to be aligned, then the stabilization period need only be 15 minutes for each additional drive.
11.) When the drive is up to speed and the ready light on the FIU panel is lit, momentarily actuate the initialize switch, the RTZ switch, and the reset switch on the FTU panel.
12.) Perform continuous seeks between cylinders $240_{10}$ and $245_{10}$ for 30 seconds minimum. This allows head gimbal springs to settle to a normal operating level.
a. Set the cylinder address to $240_{10}$ on the FTU. (Switches $16,32,64,128$ ON)
b. Set access mode switch to direct.
c. Momentarily depress the start switch.
d. Set the cylinder address to $245.10(1,4,16,32,64,128$ ON)
e. Set the access mode switch to continuous.
f. Actuate start. The drive will perform continuous seeks between cylinders $240_{10}$ and 245 .10
13.) Stop seeks and command a direct seek to cylinder 245.10
a. Actuate the RTZ switch, then the reset switch on the FTU panel.
b. Set the cylinder address to 245 .10
c. Set the access mode to direct.
d. Actuate start. The drive will seek to cylinder 245.10
14.) On the head alignment card in A02, set the $S / R W$ switch to the 'S' position. Set X. $1 / \mathrm{Xl}$ switch to $X .1$. See figure 2. NOTE
When calculating head offset, if both $P$ and $N$ readings are less than 100 mV , set $\mathrm{X} .1 / \mathrm{Xl}$ switch on the head alignment card to Xl position. Return switch to the X.l position before going on to the next head.
15.) Change the polarity of the alignment signal to the null meter with $P / N$ switch. Record both the positive and the negative readings obtained. Use the following formula to calculate head offset: $(P)-(N)=$ OFFSET. Example: $P=+30 \mathrm{mV}$ and $N=-40 \mathrm{mV}$. The offset therefore equals 70 mV . Servo offset must be less than $\pm 30 \mathrm{mV}$. If not, you have a problem in the servo system.
17.) On the head alignment card in slot A02, set the $S / R W$ switch to RW.
18.) Select head 0. Calculate and record offset.
19.) Repeat previous step for all remaining heads.
20.) If calculated offset for any head exceeded 100 mV then proceed to the Head Alignment.

NOTE
Any time you have to align the servo track or have heads which are severely out of alignment, you must back up the customer's data pack for the drive.

## HEAD ALIGNMENT

1.) Stop the drive and turn off the AC breaker.
2.) Remove the head connector support bracket'from the headarm connector.
3.) Loosen head mounting screw for any head that exceeded the offset specification. Retighten each loosened screw to a torque of 6 in.lbs. See figure 6 .
4.) Do steps 11 thru 13 of the head check procedure. WARNING
Install alignment track locking pin into the align track hole. See figure 6. Failure to do so could cause personal injury. Any attempt to retract the heads with the locking pin installed will blow a 6A 250 V fuse in the -42 Volt power supply. If this happens, you must manually unload the heads off of the CE pack before powering down the drive.
5.) GND backplane cylinder A2B09-03B (-On Cylinder) to prevent nuisance errors.
6.) Adjust head for balanced dibit pattern. See figure 7.
7.) Using the FTU meter, adjust the head until the minimum amount of offset is obtained. If the offset cannot be brought to less than 100 mV , you are probably at the end of travel on this head and will have to reposition the servo head. Any change in the servo head will require a complete alignment of all heads.
8.) While changeing the $P / N$ switch, continue to adjust the head until calculated offset is less than 100 mV .
9.) Set the switch on the head alignment card to the Xl position.
10.) Adjust the head to the smallest possible offset obtainable.
11.) On head alignment card, set the $\mathrm{X} .1 / \mathrm{Xl}$ to the X .1 position.
12.) Repeat steps 5 thru 9 for all heads to be aligned.
13.) Remove locking pin and jumper on backplane.
14.) Unload heads.
15.) Torque head mounting screws to $12 \pm 1 / 2$ in.lbs.
16.) Do a head alignment check to see that all heads are within specifications.

| Pin $60-$ Black |  |
| :--- | :--- |
| Pin 30 - Orange |  |
| Pin 31 - Black |  |
| Pin 01 - Brown |  |
| 31 | A CABLE |



CARD CAGE FROM REAR
Figure 1 - Tester Cable Connection

Figure 2
Head Alignment Card


Page 3


Equipment needed:
By:Greg Ekholm
RMO2/03 CE pack
3 Scope probes with grounds
Scope with . 5 us per division or better
4 " jumper wire to be used on CDC backplane pins Standard tools (screwdrivers, etc.)
RMO2/03 FTU (Field Test Unit)
Use this chart or something similar to track your measurements on each drive and keep it for future reference.

| DRIVE SERIAL \# DRIVE SERIES C $\overline{O D E}$ HOUR METER READING |  | CE PACK SERIAL \# DATE OF TEST |  |  |
| :---: | :---: | :---: | :---: | :---: |
|  |  |  |  |  |
|  |  | CUSTOMER |  |  |
| HEAD | Cylinder 10 | Cylinder 200 | Cylinder 300 | Carriage Way |
| 0 | uSec | usec | uSec | _uSec |
| 1 | usec | uSec | _usec | _uSec |
| 2 | $\sim^{\text {uSec }}$ | usec | _usec | $\ldots \ldots$ _uSec |
| 3 | _uSec | _usec | _usec | _usec |
| 4 | usec | usec | usec | uSec |
| Head Scatter |  |  |  |  |
|  |  |  |  |  |

1.) Connect the FTU to the 9762 drive under test. (RM02/03)
2.) Load a CE pack on the drive and start the drive. Be sure to write protect the drive. NOTE: this starts the stabilization period.
3.) Set up the scope as follows:

| NAME | PROBE | CARD | TEST POINT | CROSS-REF. |
| :--- | :--- | :---: | :---: | :---: |
|  |  |  |  |  |
| -RAW DATA | CH\#1 | A3A02 | F | 263 |
| +RAW DATA | CH\#2 | A3A02 | G | 263 |
| INDEX | EXT TRIG | A2B08 | C |  |
|  |  |  |  |  |
|  | Test point ${ }^{\prime} Z^{\prime}$ | $=$ GND on A3A02 and A3A03 cards |  |  |
|  | A2B08 |  | $=$ Access control and Index decode. |  |
|  | A3A02 |  | $=$ HD select and Read amplifier. |  |

Volts per division
Time per division
Sweep
Channel \#2
Coupling
Trigger
. 5 Volts (. 05 V with 10:1 probe)
.5 uSec
Add
Invert
AC
External Positive
4.) Set up the tester as follows: Write Inhibit Access Mode Wrt-Rd Select HD Select

On
Direct
Read
Manual
5.) Thermal stabilization should be at least 15 minutes. Do a direct seek to cylinder 10.10
6.) GND the 'READ ENABLE' line at A2A04 pin 13B on the backplane. Test points $A$ and $Z$ are GND and also pins 1A and 34A.
NOTE: Remove the jumper before you seek or you will get a fault.
7.) Position the INDEX pulse at time ' 0 ' and select HD '0' via the tester.
Record your readings and sequence thru the remaining heads, recording your readings each time.
8.) Remove the GND applied in step 6 and do a direct seek to cylinder 200.10(Switches 128, 64, 8 ON)
9.) Reapply the GND as in step 6 and sequence thru all the heads again, recording the readings as in step 7.
10.) Remove the GND as in step 8 and do a direct seek to cylinder 300.10(Switches 256,32,8,4 ON) NOTE: Do not try to seek beyond cylinder 330.10
11.) Reapply the GND as in step 6 and sequence thru all the heads again, recording the readings as in step 7.

YOUR READINGS SHOULD LOOK SOMETHING LIKE THIS:

| HEAD | CYL 1010 | CYL 200 $0_{10}$ | CYL 30010 | $\Delta$ Carriage Way |
| :---: | :---: | :---: | :---: | :---: |
| 0 | 3.7 usec | 3.6 usec | 3.5 uSec | -. 2 usec |
| 1 | 2.4 | 2.2 | 2.1 | -. 3 usec |
| 2 | 2.5 | 2.2 | 2.0 | -. 5 usec |
| 3 | 3.9 | 4.0 | 4.1 | +. 2 usec |
| 4 | 3.4 | 3.3 | 3.3 | -. 1 usec |
| $\triangle$ HEAD |  |  |  |  |
| SCATTER | 3.9 | 4.0 | 4.1 | -. 5 |
|  | -2.4 | -2.2 | -2.0 | +. 2 |
|  | 1.5 | 1.8 | 2.1 | . 7 |

12.) The present tolerances as defined by CDC for INDEX to BURST is:
$4 \pm 4$ uSec for the 3600 RPM RM03
$6 \pm 6$ uSec for the 2400 RPM RM02
This would give you a head scatter tolerance of 8 usec on the RM03. This can be checked by taking the largest and the smallest number from each of the cylinders and

- subtracting the smaller from the larger. This number must not exceed 8 .

Any carriage not meeting this INDEX to BURST may have the following:
1.) A spindle alignment problem.
2.) Ahead skewed to one side caused by one of the following:
a. Head seating problem to the carriage.
b. Head assembled wrong at the factory.
c. The carriage and coil head mounting surface being out of tolerance.
3.) An upper to lower rail alignment problem.


INDEX PULSE ALIGNED WITH ORDINATE

1. Check $\pm 5$ volt P.S. with $D V M$ (repeat $D V M$ ) while doing $0-32$ cylinder seeks
2.. Back Plane ECO (70-13398-5-04) (FO5C1 to F05C2)
2. w2 cut out of terminator/swapped
3. RM plugged into wall outlet dedicated 15A ckt (not 861)
4. Spindle ground cleaning
5. M7687 Bd plugged in good/straight
6. 2 drive system - plug MBA 0 to drive 1 and MBA 1 to drive 0
7. A2A04 fault latch card ( Tech Tip )
8. A port out $=$ input, $A$ port in $=$ output
9. Recheck $\pm 5$ volt power supply (RM02/3 Tech Tip \#2)
10. Solder on Fast Tabs on Logic chassis (9762)
11. Velocity gain adjustment
12. MBA - Run diskless 1 and diskless 2 9762 - Run tester on drive
13. Loose connections on any cable? Servo pre amp, logic cage, Berg Connectors or wires in Berg Connectors
14. "P"-clock? - Run extended drive test for seek timing
15. OPI's/seek incompletes/etc - check freeness of carriage and coil assy - clean rails
16. Header compare errors - recoverable on 2nd attempt - M7684 \#12 Rev-CS-P
17. $A$ and $B$ cable $180^{\circ}$ swap
18. Flex backplane MBA and 9762
19. Grds between MBA's/drives/CPU cabinet
20. W"1" Jumps on M7684 and M7685 Bds.
21. LCG Site? - Check jumper on MBA backplane E6El to E6C2. Must be in on 2020 sites. (BP144 ENBH)

Several articles and memos have been written about Data Lates on RMø2/ø3. It is generally known that systems with RLø1's, RLø2's, RKø6's, RKø7's, RM02's and RMø3's and combinations of these devices have the possibilities of having data lates. Listed below are some of the Sales Updates articles $I$ could find on the subject.

Sales Update Vol. 9 Number 8 Page 9
Vol. 9 Number 18 Page 15
Vol. 9 Number 18 page T12
vol. 11 Number 1 Page 3
As always, Sales Update articles are "Company Confidential" and therefore I have not reprinted them here.

Some of the best solutions to Data Lates are detailed as follows:

1. On PDP11/7Ø's - Cache must be turned on.
2. MJll-B core memory interleaved will be better than non-interleaved core memory.
3. RLll controller Rev "L" or "M" reduced data lates over Rev "D" boards.
4. MJll controller have been shown to vary data lates between the same rev boards.
5. The version of DECXIl used affects data lates.
6. Buffer size used under DECXIl effects the frequency of data lates larger buffer = more data lates.
7. MOS memory interleaved has fewer data lates than core interleaved memory.
8. UNIBUS configuration is important and should be checked if data lates occur.






NOTES

+5 Volt and -5 Volt Adjustments
1.) Useing the FTU or hand toggle, command continuous seeks between cylinders 000 and 128.
2.) Connect positive voltmeter lead to A2JD94-04A on logic backplane. Connect negative lead to GND on the regulator card.
3.) Adjust +5 (Rl7) to measure +5.1 Volts (+0.05 V).
4.) Connect negative voltmeter lead to A2JD $\overline{9} 4-01 \mathrm{~A}$ on logic backplane. Connect positive lead to GND on the regulator card.
5.) Adjust -5 (R3) to measure -5.1 Volts ( $\pm 0.05 \mathrm{~V}$ ).

Head Alignment Procedure
1.) Install head alignment card in logic rack A2. Connect FTU and meter leads.
2.) Mount CE pack on drive and allow it to thermally stabilize. CDC recommends that the pack be spinning with heads loaded for at least 60 minutes.

If the CE pack has just been removed from another drive which had been running for 60 minutes and the drive you are installing it on has been running for 60 minutes, then the recommended stabilization period is 15 minutes.
3.) Read the RM05 head alignment flow chart. Perform The servo head offset check.
3A.) Set the alignment card Servo/Read-Write switch to the Servo position. Set $\mathrm{X} .1 / \mathrm{Xl}$ to the Xl position.
3B.) Command continuous seeks between cylinders $360_{8}$ and $365_{8}$ for 30 seconds. Command a direct seek to cylinder 004.8
3C.) Compare dibit pattern with example in this book. Toggle the Positive/Negative switch and record readings in both positions. Meter readings to the right of zero are positive and readings to the left of zero are negative. The positive value minus the negative value equals the amount off offset. Or...(P) - (N) = OFFSET.
3D.) If the amount of offset is outside the $\pm 60 \mathrm{mV}$ range, there exists a problem in the sē̄vo system.
3E.) Next, command a direct seek to cylinder 005.8 Repeat steps 3C and 3D. Add offset readings from cylinders 0048 and $005 . \theta$ This sum should range between +75 mV and -75 mV . If it doesn't, you have a problem in the servo system.


BALANCED DIBIT PATTERN

## OSCILLOSCOPE SETTINGS

CHI- 2 volts/div. CH2- Not Used

> Time Base A- 2uS /div. B- Not Used

Triggering INTERNAL POSITIVE

```
CHl- Connected to
    Dibits Test point
    Y on alignment
    card.
```

4.) Command a direct seek to cylinder $753_{8}$ Install carriage locking pin into alignment hole.
5.) Set $S / R W$ switch to the RW position. Calculate the offset of all read-write heads by the same method used in step 3C. If all offsets fall within the +150 mV range then the alignment is within spec.
6.) Āny head that is greater than the +150 mV range is mis-aligned. If any head is $+30 \overline{\mathrm{~m} V}$ offset, then back up the data pack"for this $\overline{d r i v e}$ before continuing to the head alignment. Remove alignment pin from drive.


Page 20

These two notes appear in the CDC Service Manual for the RM05 and are well worth memorizing before you attempt a head alignment.

If the heads perform an unscheduled retract and the START and FAULT lights are both off, immediately turn off the $+20 Y$ breaker. You have dropped +5 Volts and run the risk of burning up the voice coil. Only after you've thus diabled the DC power supply should you check to see if the power-down resulted from a failure on the AC line. The blower will still be on if the AC power is OK.

Caution \#2: Should an emergency retract occur with the locking pin in the alignment track lock hole, the following may occur.
1.) Blown fuse
2.) Tripped DC circui.t breaker
3.) Blown power amplifier transistors
4.) Any of the above = Unretracted heads on a stationary CE pack.

Head Alignment Continued...
7.) If heads 16,17 , or 18 require adjustment, move the servo preamp cover before proceeding. (At this point the drive should be stopped.)
8.) Loosen screws on the heads to be adjusted and torque them to $4+1 / 2$ lbf-in.
9.) Start the drive and command a direct seek to cylinder 753.8

NOTE
Force exerted during head alignment can move the heads from the alignment cylinder to an adjacent cylinder, resulting in an improper alignment. Prevent this by connecting a jumper from A07-11A (seek error) to ground. Be sure to remove the jumper before commanding another seek.

If you use this jumper, remember to put the jumper on the signal end while the power is off. Then, when the drive is powered up and on cylinder, place the other end of the jumper to ground.
10.) Using the FTU, select the head to be aligned. To prevent personal injury, place the locking pin in the alignment track lock hole. Remember to remove it before commanding another seek.
ll.) Install head alignment tool so that the tool pin engages the hole in the head-arm alignment slot. Observe the oscilloscope and adjust head to obtain a balanced dibit pattern.
12.) Observe the null meter and adjust the head until the offset is less than +75 mV . If head cannot be brought into alignmen $\bar{t}$, you may have to recenter the servo head. Any adjustment of the servo head will require realignment of all data heads.
13.) Remove carriage locking pin and also the jumper from A07-11A. Spin down the drive.
14.) Final torque all the heads to $12+1 / 2$ lbf-in.
15.) Spin up drive and check to see thāt all heads adjusted are within specifications. Readjust those which are outside of the $\pm 150 \mathrm{mV}$ limits.

When head alignment is complete, perform all servo checks.
SERVO SYSTEM CHECKS AND ADJUSTMENTS

The servo system adjustments are interactive and must be performed in sequence to be valid. The servo system flow chart shows the order in which they must be performed.

1.) COARSE POSITION GAIN. Prepare the drive for use with the FTU.
2.) Command continuous seeks between $000_{8}$ and 1466.8
3.) Connect oscilloscope CHl to A07-03A (+On Cylinder).
4.) External Trigger scope to A07-07A (-Forward Seek).
5.) Observe display. If distance between on cylinder pulses is not between 50 to 54 ms , adjust top potentiometer on card A20 to meet this spec.
1.) INTEGRATOR GAIN ADJUSTMENT. Command continuous seeks between cylinders 0008 and 200.8 Set up scope as indicated in drawing on the next page. Adjust the scope until the two sloped curves are displayed as in the drawing.
2.) You want to examine closely the second to last discontinuity. This will require some fiddling with the scope in order to lock this portion of the wave.
3.) Adjust the bottom pot on the $A 20$ board until the wave is correct.


## INTEGRATOR GAIN WAVEFORM

1.) FINE VELOCITY GAIN. Command a read in conjunction with a continuous seek between cylinders 0008 and 001.8
2.) Connect and adjust scope as indicated by the drawing on the next page.
3.) The top wave form in the drawing is an overshoot condition which is not desirable. Adjust the middle pot on the A20 module to as nearly as possible resemble the ideal waveform. Best operation is attained with it adjusted slightly toward the under shoot waveform which can be seen in the final waveform.
4.) Command a sequential seek between cylinders $000_{8}$ to 14668in conjunction with a read.
5.) Note that the displayed waveform should look similar to the Final Check waveform. If any overshoot exists greater than 0.5 Volts, adjust the middle pot on card A20 until the specification is met.


INITIAL FINE VELOCITY GAIN

## OSCILLOSCOPE SETTINGS

LOGIC GND TO SCOPE GND

```
VOLTS / DIV
\(\mathrm{CH} \mathrm{I}-0.5 \mathrm{~V} / \mathrm{CM}\)
CH2-NOT USED
```

TIME / DIV
A- O.1MS/CM
B-NOT USED
triggering
A-EXT, A07-30A (-SEEK)
A- EXT, USED
PROBE CONNECTIONS
CHI TO A19-TPC (+FINE POSITION ANALOG)
CH2 - NOT USED


FINAL FINE VELOCITY GAIN

1.) Connect the drive to the FTU and command a 1010 bit pattern write to the disk.
2.) Check each test point from the block diagram above against the waveforms on the next few pages. Scope set-ups are included with each drawing.

OSCILLOSCOPE SETTINGS
LOGIC GND TO SCOPE GND
VOLTS / DIV
$\mathrm{CH}-0.2 \mathrm{~V} / \mathrm{CM}$
CH2-0.2V/CM
TIME / OIV
A- $2 \mathrm{MS} / \mathrm{CM}$
B-0.05 S/CM
triggering
A- +EXT, A06-TPC (INDEX)
B-INT
PROBE CONNECTIONS ( $10 \times$ PROBES)
CHI TO Al3-TPE (NRZ DATA)
CH 2 TO A13-TPB (WRT STROBE)
NOTE: SET TO DISPLAY MODE TO ALT AND TRIGGER MODE TO CH 1 ONLY. ALSO SET HORIZONTAL DISPLAY TO B (DELAYED SWEEP)


LOGIC GND TO SCOPE GND

> VOLTS / DIV
> CH $1-0.2 \mathrm{~V} / \mathrm{CM}$
> CH $2-0.2 \mathrm{~V} / \mathrm{CM}$

TIME / DIV
A-2MS/CM
B-0.05 $\mu \mathrm{S} / \mathrm{CM}$
TRIGGERING
A- +EXT, A06-TPC (+INDEX)
B-INT

PROBE CONNECTIONS (10X PROBES)
CHI TO A13-TPE (NRZ DATA)
CH 2 TO EO2-TPU


RM05 Write Driver Input
OSCILLOSCOPE SETTINGS
LOGIC GND TO SCOPE GND

```
VOLTS / DIV
    CHI-0.2V/CM
    CH2-0.2V/CM
```

TIME / DIV
A-2MS.CM
B-0.05 $\mu \mathrm{S} / \mathrm{CM}$
triggering
$A-+E X T, A 06-T P C(+I N D E X)$
E- -INT
PROBE CONNECTIONS (10X PROBES)
CHI TO A13-TPE (NRZ DATA)
CH 2 TO EO2-TPT

NOTE: SET DISPLAY MODE TO ALT AND TRIGGER MODE TO CH 1 ONLY. ALSO SET HORIZONTAL DISPLAY TO B (DELAYED SWEEP)


RM05 Write Driver Output

1.) Connect drive to FTU. Command a write data, pattern 1010.
2.) Command drive to read pattern l0l0. Verify that all waveforms are consistent with those shown on next few pages. Scope setups are included with the waveforms.

RM05 Analog Read Data Waveform
LOGG GND TO SCOPE GND
VOLTS / DIV
CHI-0.1v/CM
CH2-0.1V/CM
time/av
A- $2 \mathrm{MS} / \mathrm{CM}$
A- -0.05 Cl
$\mathrm{s} / \mathrm{CM}$
trigeering
A- EXT, A06-TPC (+INDEX)

-     - INT

PROBE CONNECTIONS (10X PROBES)
CHI TO A14-088 (-ANALOG DATA)
CH2 TO A14-078 (+ANALOG DATA)
NOTE: SET DISPLAY MODE TO ADD AND INVERT ONE CHANNEL. ALSO SET HORIZONTAL DISPLAY TO B (DELAYED SWEEP)


LOGIC GND TO SCOPE GND

```
VOLTS / DIV
    \(\mathrm{CH} \mathrm{I}-0.1 \mathrm{~V} / \mathrm{CM}\)
    \(\mathrm{CH} 2-0.1 \mathrm{~V} / \mathrm{CM}\)
```

TIME / DIV
A- $2 \mathrm{MS} / \mathrm{CM}$
B-0.05S/CM
TRIGGERING
A- +EXT, AOG-TPC (+INDEX)
B- -INT
PROBE CONNECTIONS (10X PROBES)
CHI TO A14-03B (+RD DATA)
CH 2 TO A14-04B (-RD DATA)

```
NOTE: SET DISPLAY MODE TO ADD AND INVERT ON CHANNEL. ALSO SET HORIZONTAL DISPLAY TO B (DELAYED SWEEP)
```



RM05 Data Latch Output Waveform
READ CLOCK CHECKS...
Use same setup as above except move CHl probe to Al5-24B. Move CH2 probe to Al5-23B. Observe that the displayed signal has a frequency of 4.84 Mhz .

NOTE: SET OISPLAY MODE TO ALT AND TRIGGER MODE TO CH 1 ONLY. OSCILLOSCOPE SETTINGS ALSO SET HORIZONTAL DISPLAY TO B (DELAYED SWEEP)

LOGIC GND TO SCOPE GND


```
VOLTS/DIV
    CH:-0.2V/CM
    CH2-0.2V/CM
TIME / DIV
    A-2MS/CM
    B-0.05\muS/CM
trigeering
    A--EXT, A15-12B (-READ GATE)
    B--INT
PROBE CONNECTIONS (10X PROBES)
    CH I TO A15-27B
    CH2TO A15-26B
```

RM05 Read Data to Read Clock Timing

## RM05 Head Amplitude Check

This procedure will verify that the amplitude of the signal off of the $R / W$ head is sufficient to allow reliable processing of data.

Amplitude is inversely proportional to the frequency of recording data. Therefore, the highest amplitude will be observed when reading all ones. The lowest amplitude will be observed when reading alternating ones and zeros.
1.) Connect drive to FTU. Command drive to seek to cylinder 1466.8 Command drive to write all ones on each head of that cylinder.
2.) Connect External trigger (negative) to A06-TPC (Index). Connect CH1 to E03-TPB. Connect CH2 to E03-TPC and set display mode to ADD and invert one channel. Set Volt/div and Time/div as required.
3.) Command drive to read all ones and step through each head in turn. The minimum level should be 130 mV peak to peak.
4.) Command drive to seek to cylinder $001_{g}$ and write a 1010 pattern on all heads.
5.) Command drive to read. Step through each head in turn and verify that the amplitude of each is a maximum of 1100 mV .

Index Timing Check.
1.) Connect CH1 to A06-TPC (+Index). Trigger internal positive.
2.) Observe that the Index is a logic one for 2.5 ( $\pm 0.3$ ) usec.
3.) Observe that the time between pulses is approximately 16.7 mS .

Speed Sensor Output Check
1.) Connect CH to Al7-17A. Trigger internal positive.
2.) Observe amplitude on scope. Signal should have positive and negative amplitudes of at least 600 mV . If not, the speed sensor gap may be misadjusted.

## SERVO AMPLITUDE CHECK

## NOTE: SET DISPLAY MODE TO ADD AND INVERT ONE CHANNEL



OSCILLOSCOPE SETTINGS

## LOGIC GND TO SCOPE GND

```
vOLTS/DIV
    CHI-0.5V/CM
    CH2-0.5V/CM
time / div
    A-1\muS CM
    B-NOT USED
triggering
A- INTERNAL NEGATIVE
B-NOT USED
```

PROBE CONNECTIONS
CHITO A18-25B (-DIBITS)
CH 2 TO A18-23B ( + DIBITS )

OSCILLOSCOPE SETTINGS
LOGIC GND TO SCOPE GND

```
VOLTS /DIV
    CH1-0.1V/CM (READ SCALE AS 100MV)
    CH2-NOT USED
time / div
    A-2MS/CM
    B - NOT USED
trigcering (POSITIVE/EXTERNAL)
    A-INDEX
    B-NOT USED
PROBE CONNECTIONS
    CHI TO A19-TPC (FINE POS ANALOG)
    CH2 - NOT USED
NOTES:
1. MORE THAN NORMAL RUNOUT RESULTS IN THE WAVEFORM HAVING A 60 Hz SINUSOIDAL COMPONENT AS SHOWN ON WAVEFORM A. AS AMOUNT OF RUNOUT INCREASES, THE PEAK TO PEAK AMPLITUDE OF THE 60 Hz COMPONENT INCREASES.
2. NORMAL RUNOUT IS SHOWN ON WAVEFORM B. IN THIS CASE, THE AMPLITUDE OF THE 60 Hz SINUSOIDAL COMPONENT IS LESS THAN GOOMV PEAK TO PEAK.
```


## RMO5 TRACK FOLLOWING CHECK

Inability to stay on track may be due to excessive pack or spindle assembly runout. It may also be due to drifting or 'hunting' servo circuits or bad AGC action. Inability of the heads to follow the track may cause read errors or occasionally cause the drive to lose on Cylinder.
1.) Connect the drive to the FTU. Connect the scope as indicated above. (Index is A06-TPC).
2.) Command a direct seek to cylinder 620.8 Observe the display using the above for reference. If the 60 Hz component is greater than 400 mV , then excessive runout exists.
3.) If runout exists, note the phase relationship of the 60 Hz component.
4.) Stop the drive. Note the position of the pack on the spindle and remove the pack. Replace the pack 90 degrees ( $1 / 4$ turn) from where it was. Start the drive and command a direct seek to cylinder 620.8
5.) Compare phase relationships with the signal now displayed and the one obtained earlier.
a. If the phase relationship of both waveforms are the same, then runout is due to the disk pack or a servo fault. b. If phase relationship has changed, then the runout is due to the spindle or again a servo fault.

OSCILLOSCOPE SETTINGS


LOGIC GND TO SCOPE GND

```
VOLTS / DIV
    CH I-5V/CM
    CH2-NOT USED
TIME / DIV
    A-5MS/CM
    B-NOT USED
triggering
    A-NEG EXT, A07-07A (-FWD SEEK)
    B-NOT USED
PROBE CONNECTIONS
    CHI TO A2O-TPB
    CH2 - NOT USED
```

D to A Output Check
The D to A converter produces some maximum value and steps down as each track is crossed. It should produce 0 V when on cylinder. The above waveform was taken doing continuous seeks between cylinders $000_{8}$ and 200.8

Cylinder Pulse Blanking Delay Check
Command continuous seeks between cylinders $000_{6}$ and 003.8 Connect CHl to A07-30B (+ Cylinder Pulse Blanking). Trigger positive internal. Observe that the Cylinder Pulse Blanking delay is a one for $950( \pm 50)$ usec.

Cylinder Pulse One Shot Check
Make same preparations as Cylinder pulse blanking check except connect CHl to A07-22A (+Cylinder Pulses). Observe that the cylinder pulse is a one for $10( \pm 2.5) \mathrm{usec}$.

OSCILLOSCOPE SETTINGS
Cylinder Pulse Switching Level Check
LOGIC GND TO SCOPE GND
time / div
A- 2 MS/CM
B-NOT USED
PROBE CONNECTIONS
CHI TO A18-09 B (+TRACK SERVO SIGNAL)
CH2 - NOT USED
VOLTS / DIV
CHI-. $5 \mathrm{~V} / \mathrm{CM}$
VOLTS / DIV
CHI-. $1 \mathrm{~V} / \mathrm{CM}$
CH2-NOT USED
triggering
A- POS EXT. A18-08B (+CYL DET B)
B-NOT USED

## Cylinder Pulse Switching Level Check

The waveform on the preceding page was taken under the following conditions:

Drive connected to FTU. Command sequential seeks between cylinders $000_{8}$ and $1466_{8}$ (forward). The other two waveforms are below this text.

OSCILLOSCOPE SETTINGS


Fine Enable Switching Level
Connect the drive to FTU and command continuous seeks between cylinders 0008 and 001.8 Compare display with drawing below.

NOTE: SET DISPLAY MODE TO CHOP.


## OSCILLOSCOPE SETTINGS

LOGIC GND TO SCOPE GND
volts/div
CHI-5V/CM
CH 2-0.5V/CM
time / oiv
A-O.5MS/CM

-     - NOT USED
triggering
A-EXT NEG, A20-12A (-FWD SEEK)
B- NOT USED
PROBE CONNECTIONS
CHITO A20-10A (-FINE ENABLE)
CH 2 TO A20-TPG (+INTEGRATED VEL)

NOTES


## FIELD CHANGE ORDER

| DIV. | f.c.o. no | REV. |
| :---: | :---: | :---: |
| PL A | $5 \because 20$ |  |
| , PAGE 20 |  |  |

INSTALLATION PROCEDURE CONTD
ADD:


LEVEL
1
2
2
2
C. ON THE COMPQNENT SIDE OF THE LOGIC BOARD, SOLDER THE SILICON DIODE \{24553500\} BETWEEN PINS $6 \&$ lL OF CHIP LOCATION FQ4. INSURE THE NEGATIVE OR CATHODE END OF THE DIODE IS ATTACHED TO PIN b. IF IN DOUBT AS TO UHICH END IS NEGATIVE OR THE CATHODE, CHECK WITH VIM TO VERIFY CORRECT POLARITY. $\frac{12}{4}$ CATHODE
D. CLOSE FTU AND CONNECT TO A qb. OPERATE DRIVE AND FTU CHECKING THE FTU'S ABILITY TO SELECT ALL HEADS ON THE 97bb.
E. LOG FLO ON UNIT FLO LOG.
F. UPDATE MAINTENANCE MANUAL DIAGRAMS WITH PAGES 4,5 AND b. UPDATE MAINTENANCE MANUAL WIRE LIST.
b. PARTS \& SPECIAL TOOLS:

FOO KIT NUMBER $\{89053768\}$ SEE ASSEMBLY PARTS LIST
7. AVAILABILITY: KITS DUE BEGINNING APRIL ll.1.1980

Remove 3 screws From Cohfonent side of FTU LocK. Lower PC DOARD Down to power
8. REMOVED PARTS: N/A
१. ATTACHED DOCUMENTS: N/A

Surat of hinged bottom. SEE NEXT PAGE FOR WIREWRAP TIDE DIAGRAM.





|  |  | FIELD SERVICE TECHNICAL MANUAL |  |  |  |  | Option or Designator |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | $12 \mathrm{BH} \quad \square$ | $16 \mathrm{Bi1}$ [ ${ }^{\text {d }}$ | $18 \mathrm{Btt} \square$ | 36 Bit | $\square$ |  | RM05 |  |
| lith RM05 HEAD CRASHES |  |  |  |  | Tech Tip <br> Number RMO5-TT- |  |  |  |  |
|  |  |  | F.S. Oition Maynard |  | Date 2-28-81 |  |  | Revision | A |
| Processor Applicability |  |  | Mgr./Su; . |  | Date |  |  | Cross Reference |  |
|  |  |  | Approval: |  | Date |  |  |  |  |

Due to the very low flying height of the heads and the critical characteristics of the RM05 packs, it is recommended that if a head crash is experienced, you should replace all the heads in the drive. There is no way you can determine with the unaided eye whether or not the remaining heads are good or not. This requires a microscope and a thorough knowledge of head construction.

In the event of a crash, the following steps should be taken:
1.) Because the RM05 uses a perforated shroud assembly, you must disassemble the shroud and clean the deck area very thoroughly. Some repeat crashes have been attributed to contamination left in the drive from the original crash.
2.) Take no chances. Replace every head when reassembling the drive. Visually inspect each head for signs of improper assembly or contamination before installing.
3.) Inspect the positioner and magnet for metal particles. BE THOROUGH IN EVERY RESPECT.
4.) When drive is reassembled, allow the drive to purge for a minimum of 30 minutes. Visually inspect the shroud area before installing a new scratch pack.
5.) When the pack has spun up for a few minutes and things look stable, you can then procede with the head alignment procedures.

Here are some important points to remember:
CDC does not recommend head or media cleaning on the 9766.
The tolerances involved are much more critical than the RPO6 or similar drives.

M: COGFFIDENTIAL



| Page 1 | Pace Revision | Pul品 |  |
| :--- | :--- | :--- | :--- |




Due to the 'Burnished media' technology used on these packs, the normal pack cleaning procedures tend to leave a residue on the platter surfaces. The media requires a special power wash cycle to insure that all the residue is removed. Again, only a keen eye trained to recognize a media defect can spot a problem by inspecting a pack. CDC recommends a program of media inspection at certain intervals but will not recommend any cleaning. Therefore a clean enviornment and proper storage of media to prevent pack contamination is strongly suggested.

If you have not done so already, purge all RM05 drives of any absolute filter assemblies with a date code of June l, 1980 to October 31, 1980. These assemblies have been found to be a source of contamination. Epoxy used in the contruction of the filter is in some cases chipping off and entering the air flow. The date code is found stamped on a yellow sticker attached to the filter. The part number for the absolute filter is 29-23591.

The maintainability group for the RM05 needs to have more complete reporting of RM05 head crashes. It has been found that some RM05 calls, especially if they are repeat crashes, have been reported on LARS against systems. This makes accurate performance statistics difficult at best. The last page of this Tech-Tip is a reporting format which should be used in every instance of a RM05 head crash until further notice. Send the completed form to: Bill Peters, Corporate Field Support Group, PK3-2 /Kll. We will appreciate your assistance in this very much.

Until the head crash problem has been resolved, we recommend that all branches have their RM05 CE and scratch packs inspected at least once a month by an outside company. This is necessary to eliminate the possibility that our test packs may be a source of contamination.
I): C CONFIDENTIAL

This decument is proprietary "Digital Equipment Culf:nitin and is intended for use by its Field Service Orgatization only. F', rinformation on writing or ungroving a Tech Tip, see Administration Toch Tin Number 2.


|  | FIELD SERVICE TECHNICAL MANUAL |  |  |  |  |  | Option or Designator |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  | $12 \mathrm{Bil} \quad \square$ | $16 \mathrm{Bit} \times$ | $18 \mathrm{Bit} \square$ | 36 Rit |  |  | RM05 |
| RM05 HEAD CRASHES (Continued) |  |  |  |  |  | Tech Tip Number RM05-TT- |  |
| \%H,n Bill Peters |  | F.S. Office | Maynard | Date | 2-28 | -81 | Revision A |
| Processor Applicabilit. |  | Mgr./Sup. |  | Date |  |  | Cross.Reterence |
| $\therefore \quad 11 \mid$ VAX |  | Approval: |  | Date |  |  |  |

PLEASE USE THIS FORM TO DOCUMENT RMO5 HEAD CRASHES FOR MAINTAINABILITY ENGINEERING IN COLORADO.
*********************************************************************

Branch Office Cost Center $\qquad$
Customer Name $\qquad$ LARS Log \# $\qquad$
RM05 Serial \# $\qquad$ Pack Serial \# $\qquad$
Date of failure $\qquad$ Date of installation $\qquad$
Hour Meter reading $\qquad$ Suspected cause $\qquad$

Site Enviornment $\qquad$
$\qquad$
Name of Engineer $\qquad$ Tele. $\qquad$
Additional comments: $\qquad$
$\qquad$
$\qquad$
SEND TO:
Bill Peters
Corporate Field Support Group
129 Parker Street PK3-2 /Kll Maynard, Mass.
Paye 3

Pas Revision ! ar : M Dat!


| Title RM05 Power and Ground ing Requirements |  | Tech Tip <br> Number |  |  |  |
| :--- | :--- | :--- | :--- | :--- | :--- |
| Author Bill Peters | F.S. Office Maynard | Date 1-6-81 | Revision |  |  |
| Processor Applicability | Mgr./Sup. | Date | Cross Reference |  |  |
| All | $\|x\|$ |  |  | Approval: | Date |

Due to the non-standard wiring scheme used on the RMO5 disk drive, care must be taken to assure proper ground integrity. The drive connects to a NEMA 6R which is rated at 240 V single phase and is normally used to connect an $861-\mathrm{B}$. RMO5's require 208 V phase to phase connection plus ground. On several sites, AC Neutral has been found to be connected where ground should be on the NEMA 6R. This causes system ground to be connected to AC Neutral through the chassis of the drive. Correct wiring is shown below.

1 Three-phase


A discrepancy exists between the RMO2/03 cookbook and the CDC vendor manuals regarding the NRZ to MFM converter (LXV) module. For a RM03, order DEC \# 29-22891 vendor \# 54278505. This is the ELXV module.

For a RMO2, order DEC \# 29-23115 vendor \# 54278509. This is a GLXV module.

The two are not completely cross compatible.
$\square$



## FIELD SERVICE TECHNICAL MANUAL

SUMMARY

This summary is current to Speed Bulletin \#164, February 2, 1981. It was originally intended that $I$ should attach all known TechTips to the back of the handbook as an appendix. The size of the resulting document prohibited that from happening. Use this summary to do your own research. I cannot stress enough the importance of regularly scanning the contents of each Speed Bulletin as they are released. Invest a few minutes of your time while you're near a fiche reader and save yourself an hour when you're on site without one.

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Three additional Tech Tips are attached to the back of the book. IMPORTANT.... RM05 Head Crashes.


[^0]:    these 5 parts make up the larger diam. hinge pins and obsoletes

