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digital INTEROFFICE MEMORANDUM

DATE: August 25, 1969

SUBJECT: STRUCTURAL (COMPUTER COMPONENTS) EXTENSION OF PDP-11 TO LARGER MODELS

TO: Roger Cady FROM: Gordon Bell

CC: N. Mazzarese
J. Jones
W. Hindle
G. Butler
B. Delagi
T. Johnson
D. Alusic

The enclosed memo discusses how the PDP-11 computer structure can be extended for larger computer configurations. The specific structures discussed are:

1. Multiple port memories
2. Multiple Unibus structures
3. Multiprocessor structures
4. Controls (eg. disks) used with multiple Unibus structures
5. Wider Unibusses (32 or 48 bits), and bus-to-bus couplers.
6. Bus repeaters for adding more devices (and device isolation).

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digital INTEROFFICE MEMORANDUM

DATE: August 29, 1969

SUBJECT: EXTENSIONS TO THE PDP-11 FOR FUTURE MODELS

TO: Nick Mazzarese
Roger Cady

FROM: Gordon Bell

cc: T. Johnson
W. Hindle
H. Spencer
D. Alusic
G. Butler
J. Jones
J. Bell

This memo discusses the instruction set. It is based on our discussions, misc. memos, and the large group discussion held in April 1969. It is a first pass design to comments, not quite the final spec.

The assumption of this memo is:

1. We shall have downward binary object compatibility of machines if possible. Failing that, we shall have downward binary object compatibility for a large subset of the instruction set. Failing binary subset compatibility, we shall have downward symbolic compatibility. Failing to meet any of the above three objectives, we pledge to not build a machine. Furthermore, we will discourage any attempts of any present or proposed product lines who propose a machine which is incompatible with subsets of 8, 10, 11, 12, 14 and 15 instruction sets. This memo is therefore predicated on:

DOWNWARD BINARY OBJECT COMPATIBILITY

We have outlined features for machines without specific references to which model numbers would contain various features we propose. The proposed changes would only involve recoding Module 4, the floating point interpretter (about 100 instructions), not the complete packaging. The proposed format would run about the same speed as the present interpretter.

Model	Bits	Definition	Optional Features
30	16	as previously defined	
40	16	has multiply, divide, shifts, repeat instructions	multiple port memories, and multiple bus structures for increasing performance of information transfers (multiple processors are not precluded)
45	16	40, with hardware program mapping	
50	16	45, with hardwired or microprogrammed processor for floating point	
60	32 or 48	paging, floating point, 32 bit memory-processor bus	multiple ports and multiple busses.
70	32 or 48	60 + segmentation	

The main extension is for 48 bit floating point data and 32 bit fixed data. We propose that the 48 bit floating point is used which is identical to the programmed floating point (i.e. a 16 bit exponent and 32 bit fraction). We might alternatively have 8 bit exponents, and 40 bit fractions - the software would emulate only 32 bits. Using this format, 32 bit fixed point data would also be necessary to take care of mixed mode data (although 16 bit integers could be used for Fortran) at the April meeting, the consensus favored this as opposed to carrying the data type information with the data ala Burroughs B-5000. The group also rejected an integer based (als JOSS) floating point. Instruction Set: Additions for floating and double length fixed point. Double precision floating point might eventually be provided with a 64 bit mantissa.

Providing floating point implies that there have to be operations and registers to hold 48 bit data. The scheme we propose is to add eight 48 bit registers, (whose last 32 bits are the fixed

point registers). Althought it was felt that 8 register was a small number, as experienced by the PDP-10, the present 6 general registers and SP give 15. Also, unlike PDP-10, the 11 stack can be used easily when overflow occurs. In fact, in a language like Algol, the registers may not be used at all, except by the function subroutines (the proposed PDP-10 Algol does this). On the other hand, the IBM System 360 has only 4 floating point registers. Also, there are times when the 11 can operate among memory without requiring AC's. Because there are no mapping between registers and memory, it does seem worthwhile to allow two of the registers to map into the 16 bit registers. The following notation might be confusing, so use Figure 1 for an alternative. That is, we now have the array:

R [0:7] ⟨15:0⟩[1]

SP ⟨15:0⟩, and PC ⟨15:0⟩

where mapping: SP ⟨15:0⟩ := R [6] ⟨15:0⟩

and PC ⟨15:0⟩ := R [7] ⟨15:0⟩ occur

We add floating array: F [0:7] ⟨47:0⟩

and double array: D [0:7] ⟨31:0⟩

where mapping: D [0:7] ⟨31:0⟩ := F [0:7] ⟨47:16⟩

(i.e. D [0:7] ⟨15:0⟩ is the exponent part)

we also map: F [0:1] ⟨47:0⟩ := R [0:5] ⟨15:0⟩

That is, the first two floating and fixed registers are also the same as the 16 bit fixed registers.

[1] [ ] delimits array range; ⟨ ⟩ delimits register bit range; A :=B means A and B are the same, and for every occurrence of the name A, substitute the name B.

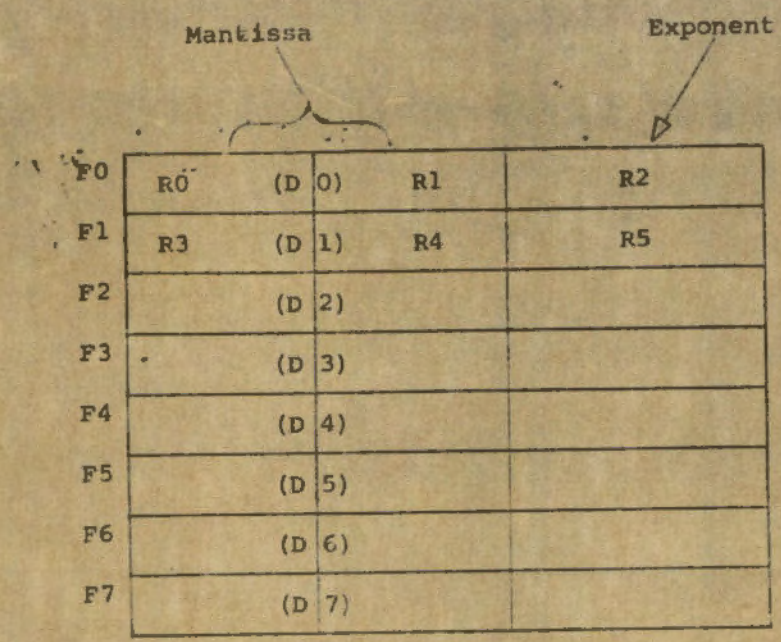


Figure 1

PROPOSED PROCESSOR STATE

Mapping of proposed PDP-11 floating point word length register/R, double length registers/D, and floating point register/F.

The following schemes for registers were considered and rejected:

1. Provide no additional registers and map the 48 bit registers into the present AC's. This would give only 2 floating or 3 double precision registers. Also, it would take away the 16 bit integer registers at a rapid rate. Such a scheme would necessitate, by convention, the use of a stack for all operations - thereby slowing down floating point significantly.

2. Providing many, say 16, floating point registers will only be marginally better than providing 8. Unless the software takes advantage of them all, it might be added cost with no gain.

Looking at one example will show our reasoning; more examples need to be examined before settling on a firm proposal.

I. Case of A B + C, where A, B and C are floating point. Add Takes 1 us (microsecond) and there are (fast) hardware registers.

	16 bit, lus memory	32 bit, lus memory	48 bit, lus memory
FMOV C, F1	2 + 3*	1 + 2	1 + 1
FAD B, F1	2 + 3 + 1	1 + 2 + 1	1 + 1 + 1
FMOV F1, A	2 + 3	1 + 2	0 + 1
	16	10	6 time

II. Case of A B + C where there are no AC's and we must use a stack (assumes read-pause write addition)

FMOV C, -(SP)	2 + 3 + 3	1 + 2 + 2	1 + 1 + 1
FAD B, @ SP	2 + 3 +(3+2)+1	1 + 2 + 3 + 1	1 + 1 + 1
FJOV (SP) +, A	2 + 3 + 3	1 + 2 + 2	0 + 1 + 1
	27	17	8 time

III. Case of A B + C, (32 bit double precision, multiple AC's)

DMOV C, D1	2 + 2	1 + 1	1 + 1 1/2 (odd boundaries)
DADD B, D1	2 + 2 + 1	1 + 1 + 1	1 + 1 1/2 + 1
DMOV D1, A	2 + 2	1 + 1	0 + 1 1/2
	13	7	7 1/2 time

IV. Case of A B + C 32 bit fixed and stack.

DMOV C, -(SP)	2 + 2 + 2	1 + 1 + 1	1 + 1 1/2 + 1 1/2
DADD B,@SP	2 + 2 + 2 + 1	1 + 1 + 1 + 1	1 + 1 1/2 + 1 1/2+ 1
DMOV (SP)+,A	2 + 2 + 2	1 + 1 + 1	0 + 1 1/2 + 1 1/2
	19	10	12 time

To conclude anything from this is difficult until we have a better idea of costs. However it does say that we always get any improvement using registers (as opposed to memory stacks), and unless the incremental price of registers is high, then it pays.

*Instruction + data fetch + execution

Let's assume that we have a $50K selling price, 16 bit computer with no registers. Add eight - 48 bit registers may add $5,000 to the selling price. To make a 32 bit memory and processor may add $15,000 and to make 48 bit memory and processor will add $30,000 . (Note that the price per bit of memory should be constant, thought the memory control is more costly. The PDP-8 and PDP-10 memories bear this out.)

Therefore the cost/performance ratios for the above costs and reciprocal program times are:

FLTPIJI

I	55/(1/16) = 890	70/(1/10) = 700	86/(1/6) = 510
II	50/(1/27) = 1350	65/(1/17) = 1100	80/(1/8) = 640
III	55/(1/13) = 720	70(1/7) = 490	85/(1/7.5) = 640
IV	50/(1/19) = 950	65/(1/10) = 650	80/(1/12) = 960

Conclusions about registers

Even though these are based on very crude guesses it seems like we can safely conclude that registers are worthwhile. Second, that for floating point, we might do well to consider a 48-bit machine. Also, eventually we might consider a 64-bit long floating point format, if a 32-bit processor is built, since it has about the same performance as the 48-bit data case (i.e. always requiring two memory accesses). (Right now, we favor the 32-bit processor at the high end.

Specifying the Operations (Op codes)

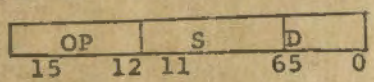
The main problem is specifying additional operation codes, while maintaining downward binary compatibility. We are suggesting there be an extended instruction mode which when entered, extended instructions would be interpretted by the processor in a different way. Two instructions in the present instruction set would be added:

1. Enter floating point mode/EFM

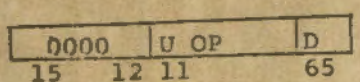
2. Enter floating point mode, but only to interpret one instruction/ EFM1.

This approach, at worse case requires all op codes to be 32 bits long, rather than 16, but at best, allows a long sequence of floating point instructions to be interpretted, efficiently. We would say the computer could always make this efficient, but it is probably fairly messy to do, since it means the computer has to do all the subscript calculating before doint the actual floating point arithmetic. Note, a small machine would trap EFM, and EFM1 instructions. Of course, the major disadvantage to the scheme is that DDT has to know the mode before it can give a mnemonic. Since PDP-11 instructions for arithmetic expression evaluation may be an average of 32 bits long, the worst case is an increase in 50%.

The new instruction set would have the following format:



BINARY OPS

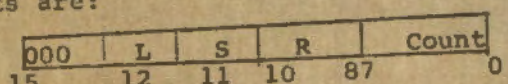


UNARY OPS

OP code	Mnemonic	Binary op action
0010	FADD	floating add
0101	FSUB	" substract
0111	FMUL	" multiply
0100	FDIV	" divide
0011	FCMP	" compare
0001	FMOV	" move
1010	DADD	double add
1101	DSUB	" substract
1111	DMUL	" multiply
1100	DDIV	" divide
1011	DCMP	" compare
1001	DMOV	" move

UOP	Mnemonic	Binary OP action
01	FNEG	floating negate
02	FTST	" test
41_8	DNEG	double negate
42_8	DTST	" test
03_8	FX	take floating and make fixed word
43_8	FXD	" " " " double word
04_8	FL	take fixed word and make word floating
44_8	FLD	" double " " make floating
00_8	EW	Enter word mode interpretation (returns to normal instruction)

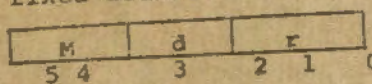
The shifts are:



LS	Mnemonic	
00	DASH	Double resigter arithmetic shift
01	DLSH	Double register logical shift
10	FASH	Floating (triple) arithmetic shift
11	FLSH	Floating (triple) logical shift

Source - Destination Interpretation

The meaning of S (or D) would change slightly for floating and fixed double.



M	d	Data	
		R^1 (r)	direct to register, where R^1 is either D or F
00	0		
00	1	M (R(r))	indirect to word register to pick up a floating or double word.
01	0		direct or indirect via stack double or floating word.
01	1		
10	0		
10	1		immediate a double or floating word follows
11	0		indexed via word register R plus the M(PC)
11	1		

G. BELL

INTEROFFICE MEMORANDUM

DATE October 3, 1966

SUBJECT Loan of a Tape Recorder.

TO Win Hindle

FROM Gordon Bell

CC: K. Olsen
S. Olsen

At one time, Ken bought a bunch (~6), very low cost cartridge tape recorders for the DEC booths. Could I borrow 1, immediately? I haven't gotten a paper tape reader for the PDP-8 yet, and want to interface the recorder to the PDP-8, as a real low cost, reasonable storage I/O unit.

dec INTEROFFICE MEMORANDUM

DATE October 5, 1966

SUBJECT Your Memo to Win Hindle dated October 3rd

TO Gordon Bell
cc: Win Hindle
Stan Olsen

FROM Ken Olsen

I was fascinated by your idea of making a cheap tape transport for your computer. I don't like the idea of loaning the tape transports which we have here because they are too poorly made to be used in this type application. However, the automobile type tape playback machines seem to work quite well and are reliable. I suggest that you look into this approach. They sell them for between $60 and $80 each and the cartridges seem to be better.

There are two types of cartridges, and the first step would be to look at which cartridge type is best. The mechanism would then probably have to be reviewed because you'll undoubtedly want to have a reversing mechanism. The number of tracks you use will probably be another decision. I believe these cartridges now use 8 tracks of quarter inch tape and you may want to buy a special head with 7 or 8 tracks on it.

If you look in the Electronic Engineers Master, you will see several tape head manufacturers listed who have tape heads that would have several channels and they have variations on the heads that can be used for digital. You may want to have a single channel and mechanically switch it to select the different tracks.

Let me know what your thoughts are. We may be willing to contribute some parts to this, and maybe some rework time in our shops, with the hope that we may get a new product out of it.

Ken

ecc

dec INTEROFFICE MEMORANDUM

DATE October 14, 1966

SUBJECT Tape Transport

TO Gordon Bell

FROM Ken Olsen

I have been thinking a little more about your cheap, cheap tape transport. I looked over some of the automobile type recorders and feel they are an awfully lot better than the Cousins machine we have. However, both of these use one spool of tape on which they wind the tape and withdraw it from the center. The result is a continouos loop, and you will have the advantage that they can be uni-directional without vacuum columns, etc. It does mean, though, that you're not going to go back and look at something without going through the whole real of tape.

I've ordered some other cartridges like the Wollensak cartridge which has two separate reels.

Ken

jeb

digital equipment corporation

MAYNARD, MASSACHUSETTS

(617) 897-8821 TWX 710-347-0212

February 28, 1967

Mr. C. Gordon Bell
553 Briar Cliff Road
Pittsburgh, Pennsylvania

Hi Gordon,

I have sent an analogue recorder head to a friend of mine in the head business. He is going to rebuild it into a Digital type head. I will forward the head to you after the gap width has been corrected.

The problem of the isolated pulse at low density and low speed calls for a different type of slicing rectifier and peak detector. I will have one designed ready for your trial in approximately 30 days.

To bring you up to date, I have investigated several recorders with unsatisfactory results so far. My brother has been away on an extended service trip so I haven't been able to get together with him yet, but I will in the near future.

In conclusion, new ideas on peripherals here make your idea far more attractive than it was at the time of the meeting with the Product Line Managers.

Campus Humor for Today

A friend of mine got all D's during the semester and a C on the final. The dean of men who taught the course gave him a final grade of F. The first day of class second semester, my friend walked into the classroom - straight to the dean, and planted a luscious kiss on the top of his bald head and said, "I don't mind getting screwed but I like a little loving along with it." After which he promptly lift the room.

Sincerely,

Roland Boisvert

Roland Boisvert
Electrical Engineer

RB/crh

G Bell

INTEROFFICE MEMORANDUM

DATE March 24, 1967

SUBJECT Small Tape for PDP-8I, 8, 8S

TO Ken Olsen

FROM Gordon Bell

Please Circulate: Nick Mazzarese
Stan Olsen
Roland Boisvert

Enclosed are some tape recorders similar to the one I've been suggesting for the Small Computers.

With a File System on Tape Cartridges, a small computer can overcome the file problem for program library and user programs. This kind of system would become the significant component in the Small Machines and should enhance its marketing appeal.

I would like to urge DEC to make it a standard peripheral, included on all 8I's, together with the software necessary for its utilization.

INTEROFFICE MEMORANDUM

DATE December 27, 1966

SUBJECT Serial Digital Magnetic Tape Unit Project - DECtape

TO K. H. Olsen

FROM Gordon Bell

CC: R. Boisvert
S. Olsen
H. Mann
N. Mazzarese
W. Hindle

Summary

I want to propose the above project, and have a project accounting number assigned to it. I would like someone within DEC to take it as a project, because it seems to be a very marketable device. Presently, I have a graduate student working on it here, and in a couple of months we should have enough data to show feasability of the system. I would like to use the DEC number to draw parts (on loan) for the project so that CIT Purchasing/DEC Order processing can be avoided.

Basic Operation

To use a standard ¼" cartridge audio tape of either 2 reel or 1 reel type, together with a DEC or other single capstan tape deck.

The data would only be written on a single track at a time, and timing would be self-synchronous in the same manner as the Teletype system. The selection of a trade would be under program control, and hopefully electronic, thus one track might be used to generate all sorts of main timing data, for fancy formats.

The data format would be a function of the program and since it is fundamentally Teletype format, the additional hardware needed in present systems for 1 unit would be:

3-F/F - Track Selection
1-F/F - Teletype/Tape Select
1-F/F - Write, on if TTY
1-F/F - Go/Stop
1-F/F - Beginning of tape mark
1-Reader, associate peak detector, etc.
1-Writer

1-Additional clock to time the tape
1-IOT card
1-Read in gates to check status of modes, and the flag
6-Misc. cards

The above system would share the teletype logic.

If electronic switching were possible between the heads, the system would perform about as well as present DECtape, but is capable of Remote, or Dataphone operation since serial data is transmitted.

Market Possibilities

1. Annihilate Paper Tape from 8, 8s entirely. Library would be on DECtape.

2. Use this in place of paper tape on 9, 10 low ends.

3. Provide possibility for a peripheral device which could be marketed separately for remote users who want their own data. (I think this could ultimately be an immense market, although I suspect not DEC's.) For example, Teletype, could include this gadget instead of paper tape, for high speed transmission. (If a dual speed system were possible, this would have more appeal.)

Storage Capacities/Data Rates

Assuming 400 bits/inch, 10"/sec, or 4000 bits/sec data rate we get:

Tape loops length	data on 1 track	data on 8 tracks	loop time (max. access)
100"	40,000	320,000	10 sec
1000"	400,000	3,200,000	100 sec

digital INTEROFFICE MEMORANDUM

DATE: May 1, 1967

SUBJECT: ANOTHER VERSION OF DECTAPE II

TO: Roland Boisvert
cc: /Gordon Bell

FROM: Ken Olsen

Here is another idea for a real cheap version of DECtape. The goal is to make it as inexpensive as possible. We want to accomplish this by making all compromises which can be made to significantly lower the cost. The most significant compromise is to have all the information flow serially. This not only makes the transport less critical, but, above all, makes the control very simple.

By eliminating the amount of tape, we can make a dramatic simplification over the capstan-driven one you have discussed. If we have 18 channels of information, as compared to the DECtape 3 channels, we would need 1/6 the length of tape to store the information. When we put 1/6 less tape on the reel, we can then drive the reels from a synchronous motor and we should be well within plus or minus 5% of speed control. This then eliminates the need for a capstan.

I would mount the tape reels on shafts very much like the LINC tape is mounted. On each of these I would put a clutch which would be driven by one synchronous motor. These clutches would drag during their off position. This then would allow us to keep the same configuration that we now use for DECtape.

Another variation that might work would be to drive one of the capstans with a Slo-Syn motor and the other with a torque motor. A torque motor would always supply tension in one direction and all the driving would be done by the Slo-Syn motor.

Gordon Bell feels that this operation has to be serial, and would like to have one labeling track. There may be a single information head which gets mechanically positioned between tracks, but there has to be a separate head for the labeling track which is electronically switched to and from the serial track. The serial channel looks at the labeling track until the right data block is found and then it is switched to the data head. In this way we can get by with one serial channel.

We should identify all of the questions involved in this transport and systematically go through and answer them. One of them is the tape path and guides. It would be nice to use the same ones we're using in present DECtape, but maybe we want to reconsider whether or not we want the oxide against the guides.

Density and speed, of course, are simple questions to be answered, along with width of tracks and number of tracks.

With a labeling track, there should then be no need for end of tape sensing because the computer can always look for that. It is not at all serious if we run off the end of the tape anyway. If we desire, we can put a strong leader on the supply reel that can take the torque of the system in the same way that the Grundig dictating machine does.

The control for this serial unit might be so simple that it could fit on the side of the 19 inch panel which now holds logic of the TU55.

Ken Olsen

ecc

digital INTEROFFICE MEMORANDUM

DATE: August 1, 1967

SUBJECT: TAPE PLAYER FOR PDP-8

TO: Gordon Bell
cc: Dick Best
Nick Mazzarese
Mike Ford
Bob Cesari

FROM: Ken Olsen

- 8ch.
- speed

I bought a new Ford, and splurged by having a tape player installed. This machine is really great. It is rugged, apparently reliable, and exceedingly convenient to use. I am asking our patent lawyer to look into what is involved in using this for instrumentation use.

Will you let me know how you would use one of these in a PDP-8. My thoughts are to put 8 blocks of 1,000 words on each track. The tape would run through a complete length of tape, read off the addressed block, and then stop when it gets to the end of the tape. One tape would then have 64 blocks, and it would probably take about half a minute to go through a whole tape.

I am going to talk to Dick Best about redundant recording systems that should be cheaper and more efficient than the audio recordings.

Ken

(EAI - Tape - Tape A-D.

ecc

Bob Jane re
Ed. Bryant
Pgh T.S.S. Co.

DIGITAL INTEROFFICE MEMORANDUM

DATE: August 7, 1967

SUBJECT: TAPE TRANSPORT FOR SMALL COMPUTER FILES

TO: Ken Olsen
cc: Nick Mazzarese
Dick Best

FROM: Gordon Bell

I'm glad to hear that there is finally going to be someone (an engineer and a programmer) assigned at DEC to work on the cheap transport for small computers. We could undoubtedly do it here, if we had a large grant, an awfully lot of time, and a carefully worded statement to render it useless; i.e., we do fundamental research. I hope that it can be made ready for the PDP-8/I. Let's obliterate paper tape from the universe! Here are some thoughts on the data organization of the tape and its use. I assume that a standard stereo, 8 channel (4 pair) audio unit will be used.

Organization of Basic Data On Tape

There are at least two basic data organizations: 1) direct or digital recording, and 2) audio (AM) recording. (See sketch.)

I don't care which method is used, except (today) I tend to favor number 2. This assumes that there is a basic one-character oriented control unit like either: 1) Teletype module for a synchronous or stop/start, or 2) 637-bit synchronous data phone connected to the computer. From the control unit then is connected a mode-in to connect it to tone modulation or frequency keeping. This in turn would connect directly to the tape recorder.

The reason I favor number 2 is that no modifications or circuits are necessary for connecting to the tape recorder. Also, using the audio system, present data phone hardware could be used which assumes a very noisy and unreliable channel between the mode-in and the recorder. The recorder can be placed anywhere. The information as such would be completely ASCII compatible with a parity and block sum check, and could be removed to a remote position if desirable. My feeling is that the ASCII control characters should be used to control the tape recorder by sending characters to: 1) position the head, 2) switch it on and off, 3) switch it from read to write, 4) unit number selection, and 5) just data.

In return, the tape recorder would send: 1) end of tape character interlaced with 2) just data.

Using the above scheme, either recording method would be okay. The layout of the data could be: 1) speed of $7\frac{1}{2}$ to 10 inches a second, 2) 8 tracks per lateral tape, 3) 60 seconds of recording or 480 seconds of data (30 seconds average access time), 4) 2400 bits per second serial data rate, 5) total storage would be 8-bit format, using ASCII, of which only 6 would be used as information:

$6 \times \frac{2400}{8}$ = 1800 useful bits per second, or

150 words per second, or
9,000 words per minute per track, or

72,000 words per 8 tracks (63,000 if only 7 tracks), or

865,000 useful bits per 60 seconds

6) density would be

2400 bits per second x 1 second per 10 inches, or
240 bits per inch

Using the above scheme at 2400 bits per second, a recorder channel band width of only 2400 h z with a signal to noise ratio of one would give adequate performance. As such, a recorder going at 3 3/4 inches per second would undoubtedly perform okay.

Use of Tape in Software Environment

Ideally, the tape would be almost compatible with DECtape; i.e., it must allow data to be replaced on a block-by-block basis. Blocks would be coded by a single track denoting the blocks, or a combination of information track together with several conductive strips to separate things into 1,000-word blocks. My feeling is that using one track which has been prerecorded with lots of padding characters (to accommodate for head switching time and speed variation), and time or block mark information, the head could be mechanically switched among head positions.

It would be desirable to use the software which is presently organized around DECtape. A desirable goal would be to use a 1 tape transport system (and that failing, go to 2 transports) which would provide for editing and compiling.

Some possible systems would be: 1) if the tape will allow inserts of data blocks, 2) if the tape can only be appended, 3) if only one block can be written on the tape (multiples could be written in 1K word blocks, for example) by putting multiple reflective or conductive markers, and 4) no inserts or appends. Note that 1 and 3 might be the same.

These yield:

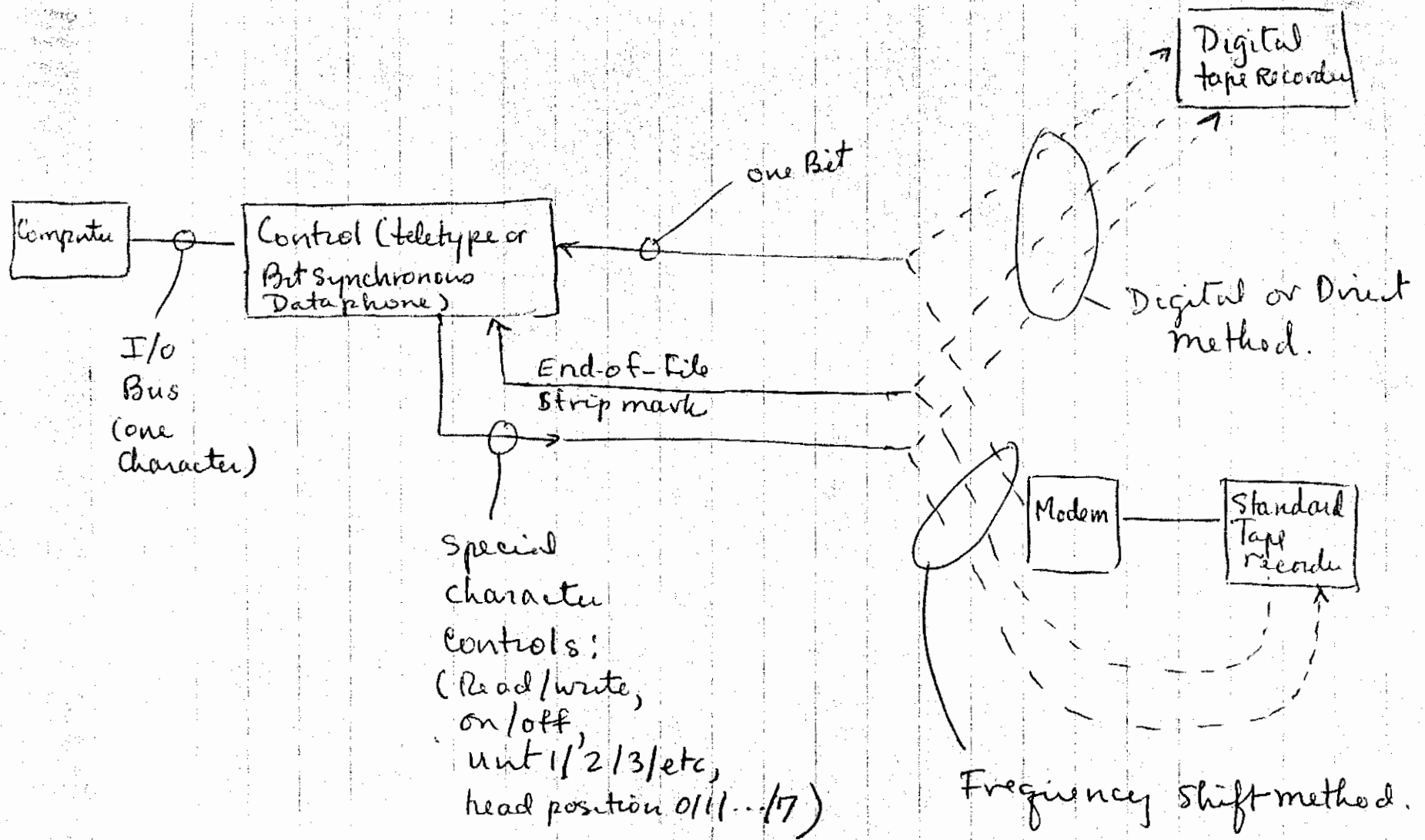
(For 1 and 3)
A system requiring only one transport and two transports if copies of programs are made. A file being edited could be read from one block on a tape and put back on another block on the same tape.

(For 2)
A system requiring two transports for editing. A partial string would be read into core and the position of the string marked. A partial string would be written, followed by blanks. On subsequent reads, more of the string would be read into core and the marker updated. On writing the appended output string, the output tape would first be read

and moved to the blanks, followed by the switching to write, to append the characters.

(For 4)
The tape would just be used for libraries.

C. Gordon Bell



Methods of Connecting Tape Recorders To Small Computers

CgB 7 Aug. 1967

digital INTEROFFICE MEMORANDUM

DATE: August 14, 1967

SUBJECT: CHEAP TRANSPORT

TO: Gordon Bell

FROM: Ken Olsen
(dictated from vacation in Maine)

I couldn't get going on the project last week because everyone is on vacation. We have made contact with a manufacturer and will buy equipment soon.

Ken

ecc

digital INTEROFFICE MEMORANDUM

DATE: April 24, 1969

SUBJECT: Is there Programming Morass? at DEC ?

TO: Operations Committee
Larry Portner

FROM: Gordon Bell

One of my many bosses, Alan Perlis says that we don't understand system programming the way we understand hardware design, hence we need something called computer engineering for the design of software. Perlis and other computer scientists say they also don't understand systems programming. (My explanation is based on the fact that programs have many more states than hardware; -- on the other hand hardware behaves with uncertainty.) This misunderstanding stems from the fact that locally each university computation center the computer scientists know best, doesn't know about systems programming, i.e., they have a local example to prove their argument. They know that MIT has had a great deal of problems building the system called MULTICS, and finally they point to IBM and say on one hand, IBM generally produces lousy software, and on the other hand, (TSS 360/67) it also fails. All of these attitudes are explainable, and therefore should not cloud the issue: Universities are not terribly business-like, and the fact that they can't run computation centers is not especially profound; they also have trouble with custodial services. MIT couldn't build MULTICS because everything they were doing was new and untried .. (forget about the fact that they had a GE computer). IBM had problems with their TSS for the same reason that MIT had trouble with MULTICS. The statement that "IBM has lousy software" may be a true one is the subject of this memo.

Ken says DEC knows what they are doing in software and can manage it; I believe this is only partially true. It is true that DEC is evolving to a software position (like IBM, and Honeywell) in that it can be thought of in terms of good business practices. Since DEC has come from a software position in which it didn't know what it was going to get, and it didn't quite know when it was going to get it, Ken (and I) have heaved a sigh of relief. We know about what we are going to get and we know about when we are going to get it. The differences between our attitudes is probably, that I don't think there is enough coming out, and that output has a low quality. To a large degree all that has been happening is a maturing. By adding manager types and expeditors who add overhead time, the certainty of output can be improved (though the flow can go to zero).

On the last week when I visited DEC I was forced into attacking the individual responsible for the PDP-11 software. In doing this I may have biased the company against him. I did not mean to do so, I'm very sorry, but the survival of that machine means a great deal to me (and perhaps the company, too). The individual was an ex-Honeywell employee, and I am somewhat afraid of them as being typical, professional programmers -- I doubt if DEC survives against them. IBM makes a genuine effort to understand the user's needs. The designers then try to build something, and for some reason, they never quite make what the user wanted .... normally this is because they generalize the hell out of it, and make it so ghastly slow as to be inoperable. (Programmers generally, don't know or worry about time.) For example, because Witcraft left, the TSS/8 may live by getting its slow, cancerous code removed. The problem is that Honeywell looks to IBM as to what to build, based on IBM's badly performing programs. Now, at DEC, we look to

Honeywell. IBM (and perhaps Honeywell) are both highly successful in their software from a business point of view. Namely, low quality, low performance,[1] high cost, but highly predictable in that their programmers emit trivia on schedule and ot exhorbitont costs. New programmers entering these environments are first beaten down so that their schedules are realistic, and they emit at a predictable rate -- because their bosses are afraid to commit them to anything.

The people in the product lines have mentioned that they are unhappy. The 110 programmers are not doing applications programming; but on the other hand the product lines are reluctant to rock the boat of "the programming morass" because the management problem is enormaus.

The relationship of the PDP-10 product line and software seems to be a very good one. Unfortunately, it doesn't seem achievable on any other product line. The reasons for this relationship are obvious:

1. Larry had better have strong allegiance to the PDP-10 just like I taught him. (His boss also runs the product line.)

2. The PDP-10 monitor programmers deserve and get respect in the product line; there is also mutual respect for the hardware people.

3. The hardware designers, are for the most part, equally capable systems programmers, and are not snowed by the 1 million reasons why software can't be built.

4. The product has been around awhile and people tend to know one another.

The reasons why the PDP-9 doesn't have average software is obvious:

1. The machine isn't that favored.

2. The more junior people train on it (for the 10?).

3. The hardware and marketing people of the product line aren't knowledgeable enough about the software, and they can be bluffed. Things that come out of the software, like the foreground-background (run-around) operating system, tend to be at best kludges, and when implemented by an inexperienced system's programmer, they are very buggy kludges. The Fortran IV compiler on the PDP-9 is just plain bad, stemming from not knowing the Fortran language, not knowing the PDP-9, not caring about doing something reasonable. I suspect that a really bad compiler could also have been built for the PDP-10, were it nat for cantankerous, hard to get along with, tranquilizer-taking H. Clark Frazier, who wanted the best compiler for the machine.

---

[1] The TSS 360/67 Assembler can take up to an hour for an assembly using disks. In a recent sales newsletter, a DEC programmer with a straight-face, said that a PDP-8 assembler takes 2 hours, and had been improved to take only 1 hour. These are fully up to IBM quality, but unthinkable to build. This particular problem occurs because PDP-8 system's programmers don't use the PDP-8, but use the PDP-10.

It is not my nature to fight for justice, windmills, or dinosaurs. I do believe in some changes -- occasionally because:

1. I have a PDP-8 and it merits better software.

2. I hate seeing the stress across the faces of the product lines.

3. The few good programmers (e.g. Leo Gossel) have expressed displeasure, and it takes about 5 - 10 Honeywell type programmers to make up for him.

4. The PDP-11 is a very nice machine with a lot of potential, and I will take several drastic steps ... like writing memos and calling people (i.e. lobbying) to see if it can't be saved from the systems programmers. So far there is some finger pointing on both sides. Fundamentally, systems programming is saying "We will design anything you want, just tell us what it is." They also suggest some of their old favorites like the foreground-background processing, sort-merge, Cobol, and an IBM overlay program far Fortran, not to mention that at least 32000 words are needed for all tasks. (Unlike PDP-8, core goes on tao easy with the PDP-11 and the Parkinsonian effect of filling all available core plus another 4000 words will have to be fought constantly.)

HELP

I'd like to see us:

1. Not to go back to the old unbusiness-like scheme where everyone is a designer, and anyone can over-commit themselves.

2. Move the software design to the product line. The software group would maintain technological expertise in compilers, assembling, etc. The planning of the hardware, the market and the software then are the group that takes the risk and has the profit. They have to live with their mistakes and do not have the large systems programming umbrella. The product line has the responsibility and knowledge for buying software it wants from the software groups. (Right now, the software groups can generally peddle anything it wants to the product line.) A product line has to be a combination of marketing, software and hardware --- no one group should dominate.

3. Create a product testing for software (quality control) outside the software group.

4. Writing engineering specifications and having engineering design reviews like other engineering. The software packages are often more complex than hardware, yet the specifications come out, after the manual, and there aren't software engineering design reviews.

5. Measure the software's performance. (Maybe as a wing outside software within quality control.) What happens now is like trying to sell modules without telling the user how big they are, how fast they go, and in many cases what they do.

6. Measure the programmers. The productivity of programmers vary by up to factors of 20, as measured by instructions per day (let alone correct ones). Find out why some programs work, and how much they cost to build. (Eventually piecework may be the answer---IBM has seriously considered this.)

7. Don't believe we know it all. We've removed the possibility of food poisoning by eating at HoJo's, surely there's a less drastic step.

8. Get and read the report:

SOFTWARE Engineering
NATO Science Committee
Garmisch Germany, 7-11 Oct. 1968

NATO Scientific Affairs Division
NATO
Brussels, 39, Belgium

bwf

digital INTEROFFICE MEMORANDUM

DATE: July 7, 1969

SUBJECT: COMPETITION WITH THE IBM 1130

TO: Gordon Bell FROM: Ken Olsen

Our marketing and sales people keep saying they never have competition with the IBM 1130 except for typesetting; however, there are thousands of these machines doing scientific calculations like the ones we would like to do with our machines. If you have any ideas as to why they sell so many and why our sales people feel they are no competition, I would like to hear what they are.

If the reason is that they have a large number of scientific software packages and we are never considered for these applications, it will be interesting to get a list of what their scientific applications are. We could then estimate the cost of getting most of them for the PDP-11 so we can take all the business. If IBM has the specifications published, it seems to me that we could make a good guess as to the cost of doing the packaging for ourselves.

I would also be interested in knowing what peripherals would be ideal or desirable on a PDP-11 to get all of this business.

Ken

ecc

digital INTEROFFICE MEMORANDUM

DATE: July 17, 1969

SUBJECT: IBM Selectirc Typewriter (one of KHO's things for me to do)

TO: Ken Olsen
cc: N. Mazzarese
W. Hindle
R. Savell
R. Collings

FROM: Gordon Bell

In the beginning, when DEC originated the idea of putting Model 28 Teletypes on a computer, we did so for cost and maintainance reasons, thereby arousing the ire of the serious programmer-user who liked the IBM electric typewriter. (The Model B as modified by Soroban was a serious competitor of the Flexowriter, and a real good vehicle to sell Field Service time.) With the alternative of a INVAC, Soroban, DURA, modified IBM Selectrics, Teletypes are great. Since DEC installed them on JOSS, IBM has improved them--until then they hadn't.

I believe the IBM Selectric is the best (feel, flexibility, and type quality) typewriter. Teletypes aren't typewriters--they don't feel, look, sound or smell like them. The Model 33 has a tinny feeling, the Model 35 though sounder has a mushy feeling, and the Model 37 is like a 35 but is slugish with regard to looking at its typed output. (Don Murphy has a scholarly paper which compares the 33, 35, and 37 from a user's phsychological viewpoint.)

I, therefore, believe there is presently only one reasonable console, the IBM 2741. (The PDP-10 group is even looking at them, thus we know they are around.) The 2741 rents for about the same price (or less) as the Teletype. The 2741 isn't an ideal console, but it isn't terrible (I have one, and I like it). The best console I have ever seen, is the DEC made JOSS console which Chuck Baker designed.

It isn't clear whether DEC can but typewriters from IBM, and put them in a console, but for certain applications either IBM will get the terminal business, or IBM will get the system. In order to persue the matter further, I would like to first, see who's interested in selling (and manufacturing) them at DEC. Second, let's see if money can be made on them, using a JOSS-console like approach, although repackaged to cut costs? Let's ask RAND how they perform?

digital INTEROFFICE MEMORANDUM

DATE: July 16, 1969

SUBJECT: Response to your memo - "Competition with the IBM 1130"

TO: Ken Olsen FROM: Gordon Bell

I can beleive that the DEC sales people do not feel we compete with the IBM 1130. The missing ingredients are:

1. Hardware (line printer, card reader, disk - although DEC tape may suffice).

2. Software - many special market packages. The feeling that there is a package to do anything the user might ever dream up.

3. A particular salesforce. IBM's salesmen are fundamentally smoother, more knowledgeable about software and less engineering oriented. DEC's salesmen are more versed in real time applications- there we compete with the 1800 favorably both on a price and services basis. With a few exceptions, I believe this is the image of our sales offices. I doubt if many of the salesmen are comfortable selling to non-engineers...Although I may be wrong.

What is the 1130?

On a cost performance ratio basis, the IBM 1130 is the best computer IBM has. It's program compatible with the IBM 1800, and took the place of the IBM 1620. For a school (high or junior college) or office (say civil engineering) it is a very good buy. It has

1. 8K - 16 bit word core.
2. Movinghead removeable disks.
3. Line printer.
4. Card reader (and perhaps punch).
5. Many nice software packages.
   a. Special language for engineering (eg. Continuous System Simulation Program/CSMP)-- written in Fortran, put into the DEC library by us at CMU, but no one is interested in announcing it.

b. Very special languages for Civil engineering, lens design, etc.

c. Special languages for social scientists (eg. statistical packages).

d. A Fortran IV much better in size and speed than the Fortran on PDP-9, even though the 9 is 2 times faster.

e. Ability to be a remote card reader, line printer and ship jobs to a central, larger 360.

f. Basic packages to make the computer be useful in limited business accounting situations.

What can be done:

1. The peripherals are important for this and other reasons...can't we buy a company or people to get some of these products?

2. Do a kind of advertising that tries to sell the image of vast DEC software like that of IBM (ie. there is a package or language to solve his problems).

3. Have a look at the various markets the 1130 serves, by looking at their software. Then go after the largest (or easiest to penetrate). Because of IBM's breadth they invariably lack depth, ie. that's why we win in typesetting. By picking some area (like high schools) we can probably win on depth (and cost). DEC now has the size and reputation to attack IBM markets and it shouldn't be too difficult.

digital INTEROFFICE MEMORANDUM

DATE: July 16, 1969

SUBJECT: Cheap Tape (one of KHO's things for me to do) - relation to new PDP-8 too

TO: Ken Olsen
cc: R. Lane
S. Olsen
N. Mazzarese
Jack Shields

FROM: Gordon Bell

In order to get some sense out of the parties involved, I propose we distribute some of the historical and pertinent data, then let us all get together and try to reach an understanding. We must have a meeting!

Last month I talked with Jim Milton who works for Bob Lane and his approach seems basically reasonable. The relevant memos I have are: GB: 10/3/66; KHO 10/5/66; 10/14/66, GB 12/27/66; 3/24/67, KHO 15/1/67, Roland Boisvert 5/5/67, KHO 8/1/67; 8/14/67; Lewis Illingworth 10/11/67; 12/12/67; 12/21/67. In addition in response to KHO 8/1/67, thereafter I wrote a fairly extensive memo on August 7, 1967, which described the use and helped prod the project into getting Lewis Illingworth.

Only three new events have transpired after Illingworth's departure. First, Jack Brown is making such a device and has loaned or sold one to Field Service. It's a SONY based device (not Cassette), but is essentially unmodified. His device only allows for one transport and is under complete manual control. Second, some small California based company, which was part of the Datamec crowd (Tom Tracy), has a company which sell 2-4 cassette tape recorders for a PDP-8. (Tenneco may also have one.)

Finally, DEC is again trying to make the device. I would like to hold a meeting on the subject, as soon as whoever is in charge of the project wants to hold it. The first part of the meeting should describe how the 2-3 existing systems work. My own thoughts haven't changed much on the subject basically - any sort of cheap transport is an order of magnitude better than paper tape. Also, the device doesn't have to be as good as we think.

digital INTEROFFICE MEMORANDUM

DATE: August 21, 1969

SUBJECT: Your Magnum Opus, August 7, 1969

TO: Larry Portner

FROM: Gordon Bell

cc: Steve Sobel
Win Hindle

Basically I concur. The valuable thing that doesn't seem to be automatic is measurement of how well the project is carried off with prediction; measurement of the thing -- namely for a compiler, the compiler should output its performance; predict the performance, e.g. floating point, and specify it, see how well it performs. Measure the projects in terms of development time, cost, size (as measured by instructions, language, and category--compiler, assembler, cpu maintenance, arithmetic, io maintenance, etc.) number of errors, document size. Begin to correlate projects variables, eg. size vs. cost to serve as a predictive guide.

To your New Project engineers, I think what you've got is fine; the only thing I think that's better is to hand out a real live example of a project history, with all the steps, all documentation, and a commentary. (Do 2, eg. a floating point page, and a monitor -Disk service.)

I still think the P.L. managers need software experts too, to protect themselves from your system.

bwf

digital INTEROFFICE MEMORANDUM

DATE: January 22, 1970

SUBJECT: Larger PDP-10's, the Low Price of PDP-10, Networks, Sales in Holland

TO: Bob Savell
Dave Cotton
Jim Bell
Larry Portner

FROM: Gordon Bell

DEPARTMENT:

cc: Operations Committee

Note: Please read this, it really isn't a put on.....I'm serious. I also think it will work. If it does, it's easily 50~to 100 million in sales. I stand firmly behind the standard party line: We've got to get out and sell small PDP-10's, ...more or less. The memo is predicated on this. This memo discusses the real problem of not having an expensive enough system, and proposal of how to get the price up.

Background

Dr. Nico Habermann just returned from Holland at Christmas time (death in family problem). He visited the DEC office in the Hague, and though it is a small sales office, was quite impressed with the salesman for Holland and Belgium. I trust Nico's appraisal, since he knows Europe, especially the universities.

Keeping up with the Jones's phenomena

Nico remarked that the DEC salesman was having trouble making a sale at UTEC in Holland, simply because one of the northern universities had just gotten a CDC6600--now all universities have to spend that much money. This is a well known attribute of people--let's accept it. Thus, when a user says he wants a 6600, it may often be for prestige. More often than not, he is willing to take something else if it can be shown to be as expensive and have as much prestige. He will readily buy it if it is different and he may even be willing to spend slightly less.

I therefore propose we put our heads together to see if we can come up with a $5,000,000 PDP-10. Remember that old proposal to DEC from CMU in May 1969---CMU figured out how to spend about $5M by buying a bunch of PDP-10's (≈ 6). In a university a bunch of computers is ideal because a number of users (and departments) are involved, thus a lot of tiny computers ($.8M) is better than one large one, say $4.8M, since each is autonomous.

What Would Be Offered

1. A collection of PDP-10's, PDP-11's, and PDP-8's, in some sort of nicely packaged deal arranged in a brochure.

2. Some interconnection software may be nice, although not necessary. Why not sell them on eventual interconnection. Sell a packaged deal that is based on independence. A simple network like our first stage is doable, since all it provides is file transfers among machines and remote user execution on another machine. Since we are already doing this on a single machine, and there doesn't seem to be any problems, then this facility could be safely offered.

Why Would You Buy One

1. Prestige, etc.

2. Face saving....here you can order a genuine $5,000,000 computer, but for practical reasons (budget) may only take delivery on the first $1,000,000 to $2,000,000 part.

3. It is part of the future. Several networks are being proposed and studied. A chance of working on current computer science research instead of taking an old system like the 6600.

Who's Going to Work on It

It just conceivably fits in with what Larry Portner and Jim Bell have been thinking about... however, due to the timeliness, I think we should try it on a few places, sort of semi-seriously, to see if they would buy it without any commitment on DEC's part.

bwf

digital INTEROFFICE MEMORANDUM

DATE: April 3, 1970

SUBJECT: Berkley Computer Corporation

TO: Win Hindle

FROM: Gordon Bell

cc: Alan Kotok
Dave Cotton
Jim Bell
Bob Savell
Larry Portner
Ken Olsen

DEPARTMENT:

Jesse Quatse visited us here yesterday to discuss the possibility of buying computing power from them in wholesale quantities. Jesse is Vice President in charge of engineering for BCC. You may recall that this is the company the group from UC/Berkley formed, and the same group that developed the 940. It includes: Butler Lampson, Peter Deutsch, Wayne Lichtenberger, and Mel Pirtle - President. They have a large number of Ph.D's in the group, so according to Ken, may be in real trouble. Their company has about 100 people now.

They are building a super computer to serve around 500 simultaneous on-line users. The structure is shown in the sketch below, along with several numbers. The machine was called the 6700 at Berkley, and Kotok has information on it. They say they will begin delivering computing power this summer, and they are in the process of putting all the components together now. They have run the monitor, simulated. They figure to come in at a price of about 1/2 of current service bureaus.

What's interesting about this:

1. It will be the largest in terms of number of simultaneous users, mainly due to a fast drum, getting rid of scheduler.

2. They have made very effective use of miroprogramming, because all 5 different type processors are made from the same structure.

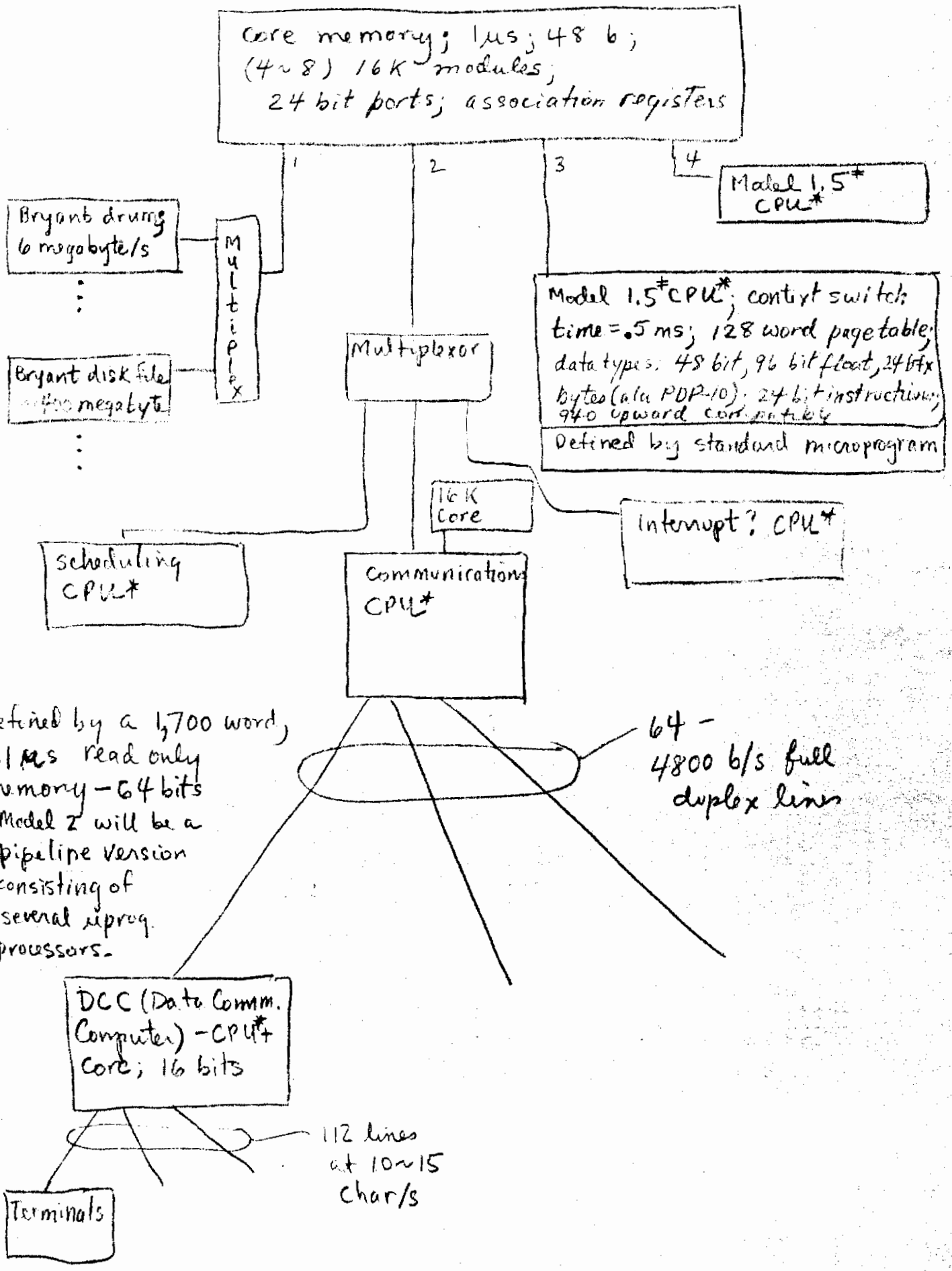
3. The system has probably been analyzed more than any other system because of their knowledge of the use of the 940.

4. It is a network.

5. This is the first time that a group has used actual data from a software operating system to design hardware - and their next software.

What does it mean to DEC? They don't intend to market this machine in its current version. However, they are thinking about a subsequent version which they would either sell, or make duplicate copies of to use in their wholesaling. The BBN system is easily capable as their system, I would guess -- the current evolutionary strategy for the 10I paging monitor isn't. The method of interfacing 11's to a 10 will give as many input lines. The drum is the key in most systems like this, a better drum will be necessary for 10I. Also, Strecker's work indicates the 10 is not optimum (according to inst/sec/$) until more CPU's are added.

bwf


Core memory; 1μs; 48 b;
(4~8) 16K modules;
24 bit ports; association registers
1
2
3
4
Model 1.5* CPU*
Bryant drum
6 megabyte/s
Multiplex
Bryant disk file
Multiplexor
Model 1.5* CPU*; context switch time = .5 ms; 128 word page table; data types: 48 bit, 96 bit float, 24 bit x bytes (a la PDP-10); 24 bit instructions; 940 upward compatible
Defined by standard microprogram
16K Core
Interrupt? CPU*
Scheduling CPU*
Communications CPU*
* Defined by a 1,700 word, 0.1 μs read only memory - 64 bits
* Model 2 will be a pipeline version consisting of several μprog. processors.
64 - 4800 b/s full duplex lines
DCC (Data Comm. Computer) - CPU* Core; 16 bits
112 lines at 10~15 char/s
Terminals

BCC System

Gordon Bell
August 7, 1970

LET'S BUILD SEVERAL THOUSAND COMPUTER TERMINALS SYSTEMATICALLY

Is there some unified way we can attack the computer terminal problem in a systematic way? Let's look at it my way. I've just spent the last few days being beaten on about having a particular terminal type, thus I've tried to build a method to generate all the terminals we must have. Let's agree to this (or a revised list) and then go after them. This list is given in an alternative generator diagram (Figure 1) and only about 13 of the more useful ones are shown. It is also given in a family tree structure (Figure 2). In this regard, let's not just have a few of them; let's get them all and also generate product by-products (like the IBM office tape-cassette writer/editor).

The approach is: packaging oriented--not just solve each problem as it comes; modular--you build with mechanical parts; and exhaustive--shows all we want/need. It also allows other terminal classes to be added when necessary, and it does a divying up of the computer-terminal market among the 8, 11 and 15.

The tree I have shown doesn't necessarily represent the final solution tree, but it does allow the problem and the policy solution to be shown in a simple way.[1]

Modules

The modules out of which these are developed (and we now have) are:

1. PDP-8/E (without cabinet)
2. PDP-11
3. 15" X-Y Scope
4. Short Vector Generator
5. Storage CRT
6. Paper Tape Reader/Paper Tape Punch
7. Calcomp Plotter

The modules we need (but are in process) are:

1. Typewriter Mechanism (7 and maybe 9 dot variety to handle higher quality print for letters).
2. Packaging Approach--so the whole thing looks like it was planned.
   a. Stand alone (capable of having computers or special logic in them).
   b. Computer Integrated.
   c. Table Top
   d. Portable Boxes.

Note: 1. As an alternative approach we can go the way the communications problem is being solved with three independent czars (who communicate a bit with each other) each after the same market with the 8, 11 and 15 and each telling the world why it should buy 8, 11 or 15 (check one) for their application, and each writing their own introductory literature designed to educate and tell the world what a modem is. A nice approach to maximize writer potential in engineers, enlarge the tech writing and publication staff, minimize corporate profit and ensure confusion in the field.

3. Scan--TV.
4. Large Scope.
5. Tape Cassette (DECtapette).
6. Microfiche/Microfilm Reader.

The modules we must develop are:

1. Software.
   a. Behave As Teletype.
   b. Behave As ARDS
2. Fast Character Generator
3. Fast Vector Generator.
4. Acoustic Coupler Modem

Figure 3 shows how some of the modules might look.

Module Stand Alone Considerations

Here we want terminals in various styles.

1. Most units will be stand alone floor mounts. Let's take the RAND JOSS console (circa 1964) designed by Alan Kotok and Chuck Baker as the ideal.

2. Computer Integrated--in some cases, we want a scheme to put scopes in consoles (a la PDP-12). In other cases (the high performance terminal) we want to put the PDP-8 or PDP-11 in the terminal.

3. Desk Top--special applications (e.g. ticket counters, desk tops, etc.) have to be considered too. Here the basic desk top unit should be able to be moved.

4. Portable--we want to hit all these small terminal manufacturers like Infotec, Datel, etc. who just take a crummy IBM selectric, add acoustic couplers and electronics and sell it. LET'S GO AFTER THE TYPEWRITER MARKET!!

Distribution:
Ken Olsen
Win Hindle
Nick Mazzarese
Stan Olsen
Ted Johnson
Pete Kaufmann
Joe St. Amour
Alan Kotok
Bob Savell
Andy Knowles
Bill Long
Len Halio

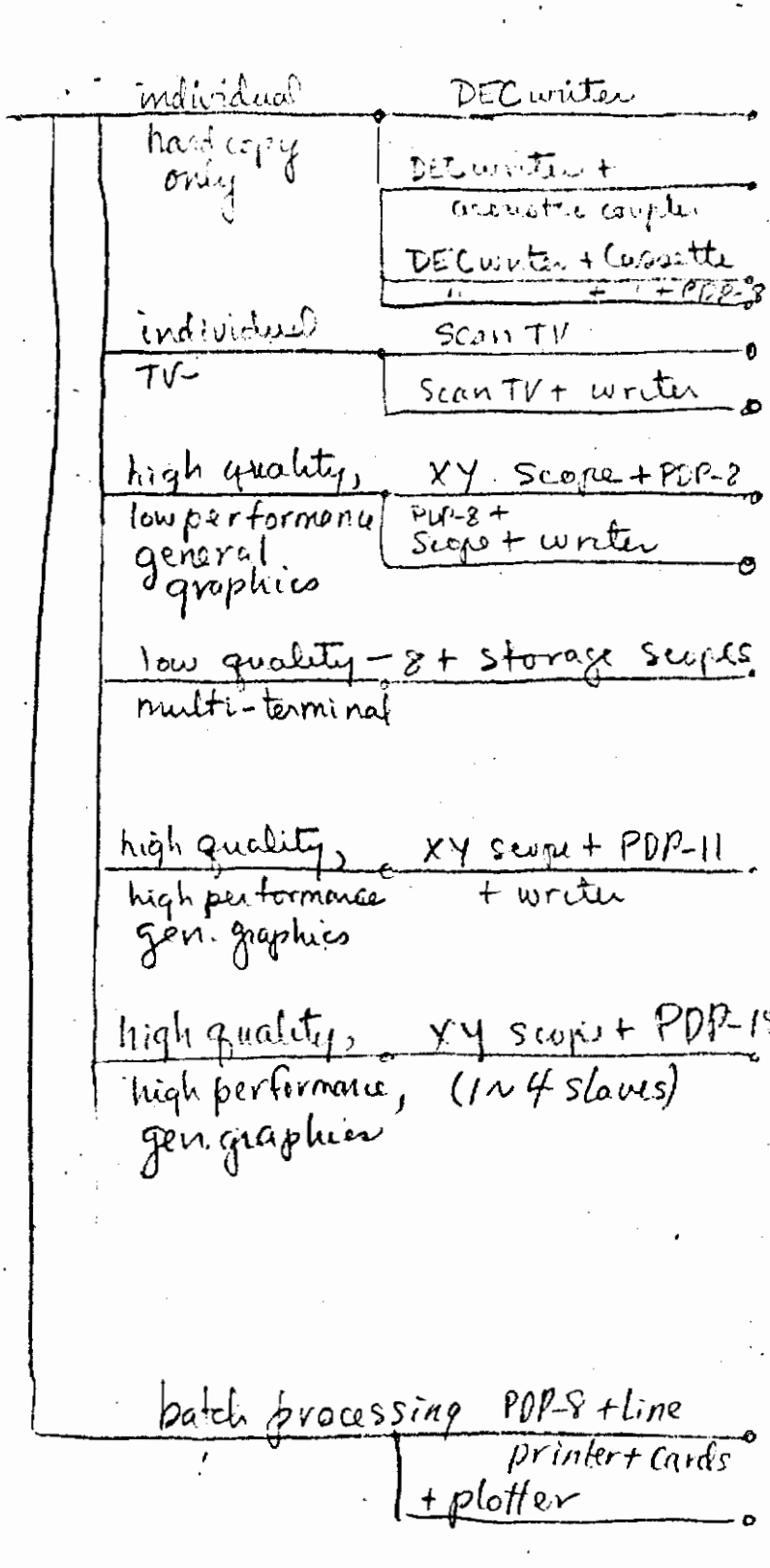
/kb

FIGURE 1

4 ENCASEMENT ALTERNATIVES	5 HARD COPY OUTPUT ALTERNATIVES	3 VIEW OUTPUT ALTERNATIVES	4 INPUT ALTERNATIVES
--Typewriter-Like Stand	--None	--None	--None
--Portable Case	--Plotter	--TV Scope	--Keyboard
--Desk Top	--DEC Writer	--XY Scope	--Tablet
--Within A Computer	--DEC Writer & Plotter		--Joystick
	--Camera		

7 FILE ALTERNATIVES	5 SOFTWARE PACKAGE ALTERNATIVES	4 COUPLER ALTERNATIVES	3 COMPUTER ATTACHMENT ALTERNATIVES
--None	--None--Uses Exist	--None	--Part Of Computer
--Paper Tape	--Teletype Replacement	--Direct	--8 Based
--DECtapette (or DECassette)	--ARDS Replacement	--Acoustic Modem	--11 Based
--DECtape	--XY Graphic Console	--High Speed Modem	
--Disks + Floppy	--IBM Cassette Secretary Terminal		
--Disk + DECtapette			
--Disk + DECtape			

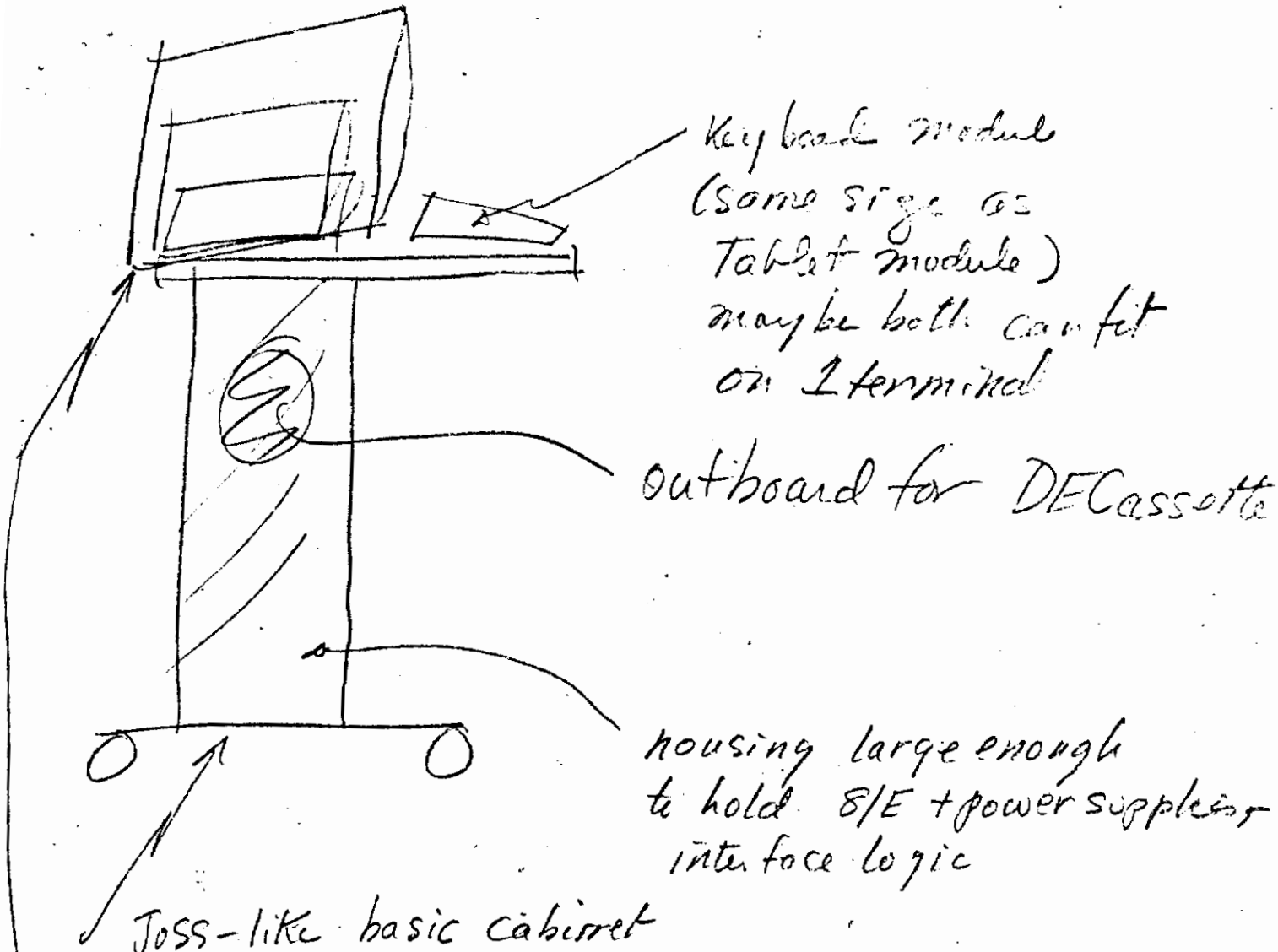
TERMINAL ALTERNATIVE GENERATION DIAGRAM
FOR
SEVERAL THOUSAND TERMINALS



	Subs Price	comments
individual DEC writer	1.0	TTY replacement (KSR)
hard copy only — DEC writer + acoustic coupler	2.0	IBM 2741 replacement
DEC writer + Cassette + " + PDP-8	2.5	TTY ASR replacement
	8	OFFICE Editor (a la IBM)
individual TV- Scan TV	1.5	TTY replacement
Scan TV + writer	2.2	" with hard copy in small space
high quality, low performance general graphics — XY Scope + PDP-8	7	ARDS replacement.
PDP-8 + Scope + writer	8	(used for PDP-10 console computer)
low quality - 8 + storage scopes multi-terminal	?	Do we need it? want it we have it. what about a good package?
high quality, high performance gen. graphics — XY scope + PDP-11 + writer	20	specialized software, can't we get this one
high quality, high performance, gen. graphics — XY scope + PDP-15 (1 ~ 4 slaves)	25	We are getting this one why?
batch processing PDP-8 + line printer + cards + plotter	20	PDP-10's doing this?
	25	

Fig. 2 Family tree of some of the more useful terminals which we might (and are being) generated

cgb - 3 Aug 1970

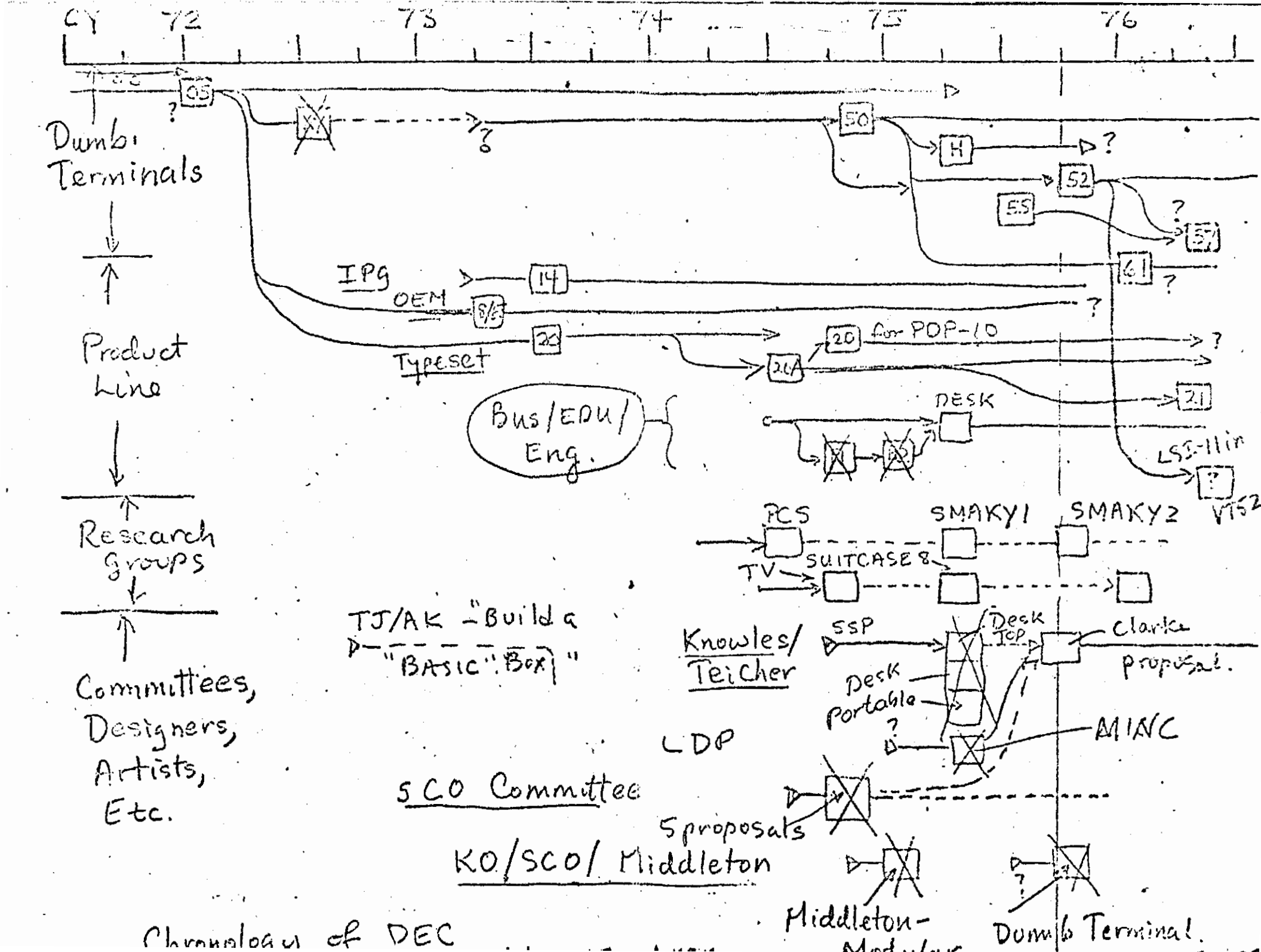


big enough for:

1. TV screen display; or
2. XY scope display?; or
3. DECwriter mechanism; or
4. " " " and TV screen
5. " " " and XY scope (hopefully

Fig. 3 Sketch of certain terminal modules

cg6. 3 Aug 1970



Chronology of DEC

digital INTEROFFICE MEMORANDUM

SUBJECT: COMPUTER NETWORKS

DATE: August 12, 1970

TO: Win Hindle
Bob Savell

FROM: Gordon Bell

cc: Larry Portner
Jim Bell
Nick Mazzarese
Andy Knowles

DEPARTMENT:

We simply must get organized on this issue!

In our last conversation on networks you gave Larry a push, who in turn gave Jim Bell a push. Jim responded with a memo (July 16, 1970) to Larry and I on Multi-Mini Timesharing.

Jim's memo discussed using mini's for the network. So far the IBM Research (1130's), Honeywell (H1648 = 3-516's) and potential Nova network appear to me as kludges. Little computers aren't worth a damn for computing because of their arithmetic capabilities. We can go the multi-mini route and I'm sure do it better but let's try to arrive at some sort of corporate plan. (Couple it into communication too.) We would build 1 or 2 internal networks to use. We have to have someone who really will push them. Such a person would look at:

1. The ARPA-like IMP structure for high speed message switching among computer. Don Alusic of 11 group has this one under control, I believe.
2. Use of TS/8-PDP-10. We'll have this one working soon at C.M.U., ship files; do job flow through 8 to 10.
3. PDP-10/PDP-10 communications. This is currently working at some of the ARPA installations We would go on to actually sell a multi-10 installation.
4. Remote entries to 10 for line printer, etc. and remote concentrators. Also, we would allow little computers (15,8) to get in for files, assembly, etc. We could probably pay for this internally at DEC by getting all the DECtapes off of all the remote computers, and by interconnecting the 10's.
5. Multi-11's. The switch structures proposed by Delagi allow simple networks to be formed easily with little software pain. These structures seem to be much more elegant than

the mini-nets being sold above. There is the added benefit of having an 11/40 to do arithmetic, and we have a good way of making

6. PDP-8/E as a terminal. Here we have to get a really nice scope, also a line printer-card reader combination. The IMLAC terminal is a great way to go - this couples up with a computer in the home market.

When can we get together to discuss networks?

/bfs

Copy 29

digital INTEROFFICE MEMORANDUM

1211

SUBJECT: GLAD YOU ASKED WHERE THE PDP-11 CAME FROM - DATE: August 12, 1970

TO: Ken Olsen FROM: Gordon Bell

cc: Nick Mazzarese DEPARTMENT:

- because it's close to my heart as an amateur computer historian and taxonomist. Basically, I like the British so I can probably show that everything came from them. It's too bad they don't have more manpower (or can't organize that they have) because they do have good ideas, but rarely do they come off - in a production sense. We had an undated,un-page-numbered, poorly written (41 pages) document by Computer Technology Limited on a computer called Modular One. I never really understood it very well; I'll talk about its influence below.

To get to the point, there are at least several reasonably nicely worked out ideas in the PDP-11. Let me give you my impression of where they came from.

The use of general registers (programmer view)
This ability makes the PDP-11 most interesting as a design. We use general registers for a number of things - more than in any other computer (I believe). This basic idea came from PDP-6/10. The idea of using general registers in the first place on PDP-6 was suggested by Peter Samson. I was influenced by the need for stacks(as in the Burroughs machines) so we made them very general (far more than IBM) in fact, SDS copied our use in Sigma 5, 7. IBM has contemplated using stacks in the 360 from time to time. The idea of general registers was first used (to my knowledge) on Pegasus - a vacuum tube machine (circa 1957). Christopher Strachey is apparently credited with the idea. I only knew of Pegasus in 1968 (when talking with a visiting professor at Carnegie from U.K.). I doubt if Peter knew Pegasus. I must also confess that the PDP-6 looks like a very nicely designed UNIVAC 1107, which was also around (if we had tried to find it, perhaps Peter saw it. All in all, the PDP-6/10 was, in retrospect appraisal, the best of the early general [illegible] lines until PDP-11. The PDP-11 influenced the [illegible] ch, to my way of thinking, would have been a better

general register computer than PDP-11 or 10. The reason I think the PDP-11 is a better general register machine than the PDP-10 is the way the registers are used to point to stacks. The PDP-11 use of general registers to control stacks occurred to me in 1966 when I first went to Carnegie. I discussed the matter of how a general register should point to a stack, and how one should be able to operate (arithmetically) on the stack, (not just load and store) with various people there. In particular, Harold McFarland and I discussed the idea, and I suggested how one should look at address calculation and unary/binary arithmetic/logical operation methodically. Harold put the whole thing together rather crudely, first at C.M.U., I believe.

I discouraged him from taking such an elaborate design to DEC, and to think 8-bit. Harold worked with John Cohen at DEC along very small machinery lines, but finally they ended up with a kludgy 16-bit design. Harold was transferred from under Cohen and refined the kludge for Roger Cady. Just prior to kludge building time, Harold resurrected the present PDP-11, though considerably refined, and persuaded Roger (and I) to look at it. The design of the current PDP-11 is essentially that one refined by lots of people and coding (only one or two individuals working on it would have made it better).

Modular One's Influence on General Registers

Modular One seems to be influenced by Pegasus. They do not use general registers for stacks (like the PDP-11) in the document I've seen! If they do then perhaps they changed and copied the idea from PDP-11. Their use is more extensive for software, because they point to files, segments, etc., they say. The manual looks like it was written by grand system designer types, but I would doubt that things ended up that way.

What you say to General Doriot

There are two important parts to computers: how a computer behaves, its instruction-set (or how people program it); and how the parts fit together in a structure.

From the instruction-set viewpoint:

The PDP-11 and the Modular One by Computer Technology look like they came from the same common ancestor - - namely the U.K. Pegasus (circa 1957). Since the idea is so fundamental (and simple) I suspect it was re-invented by UNIVAC (in the 1107), IBM (in the 360), and DEC (PDP-11). As we all know,

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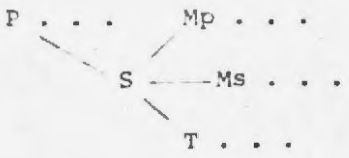
designers are poor readers and writers. It is clear that most later general register machines (e.g., Sigma 5, 6, 7) are based on the above machines. The PDP-11 was mostly influenced by PDP-6/10 and the extensions I talk about in detail, certainly not Pegasus, or Modular One which we didn't really know about.

From the structure standpoint:
PDP-11 has a structure called the Unibus (which I named and DEC copyrighted). It is:



which says that the components (primary core memory, Mp, and secondary memory, Ms, and terminals, T) communicate via a common switch, S. The U.K. computer and the PDP-11 both have such a logical structure. The U.K. computer has the above physical structure. The PDP-11 has a physical structure:

P	Mp. . .	Ms. . .	T. . .
S	S	S	S

In both cases, any component can communicate with any other. It is also the same as a telephone exchange with one trunk.

During PDP-6 development I attempted to use the PDP-11 scheme for a while, but Alan Kotok convinced me not to. Dick Best and I had long conversation about it one noon hour - and it may have been another mistake of the PDP-6. (Dick should have been working on the circuits that hour and I on the mechanical design). We rejected it in the PDP-6 because the discrete technology cost was too great, that is, a bus suitable for memory-processor dialogues was faster and more expensive than need be for processor-I/O control communication. In my book, I go into the matter of switching, and try to generate many of these structures (possibly some that most people have never thought about). I can truthfully say I knew about their switch. I saw it in their write-up. In fact, a main point of the book is switching and structure. The U.K. group did have this influence:
1. Made the PDP-11 group aware of the switching problem.
2. Gave the PDP-11 a name of master-slave for the Unibus, called it the Unibus. I was always against the name (particularly since we don't have masters and slaves . . . only slaves).

1217

3. Told us how not to have a central switch.
4. Showed me that at least on this matter the thoughts from the U.K. were relatively primitive.

The U.K. machine physical structure is based on the way we used to go out radially from a central hub as in a PDP-1. The CDC-160 convinced me to use busses. From PDP-5, 6 time on we have used them at DEC - though poorly as in the case of 5, 8, etc. As for the way the bus is controlled, we use a method that I believe comes from IBM.

Influence on the NOVA:
I think that NOVA was probably influenced by DEC most. The NOVA is a general register extension of the PDP-8. Their auto-index registers first appeared in PDP-4 (and later 5). The British give Data General too much credit. I doubt if any of those guys really read that much or could get hold of the relevant documents. I know Ed DeCastro couldn't read. Henry Burkhart, Dick Sogge, and Seligman probably do read - I doubt if they would ever admit being influenced in any way.

Epilogue:
Unlike histories, etc. made by real historians, this one has problems due to personal involvement. This one might be confirmed by Nick Mazzarese, Harold McFarland, Roger Cady, John Cohen, Alan Kotok et al. Hopefully to a first approximation it's ok. Hope it serves you!

/sfs

digital INTEROFFICE MEMORANDUM

SUBJECT: Competing with Computer Technology, Ltd. (CT) and University of Newcastle

DATE: August 28, 1970

TO: PDP-11 Coordinating Committee
Geoff Shingles (U.K. Office)

FROM: Gordon Bell

cc: Ken Olsen
Nick Mazzarese
Ted Johnson

DEPARTMENT:

I just spent several hours with Mr. Iann Barron, managing director of CT, at their Hemel Hempstead plant - thanks to Geoff Shingles. Mr. Barron has a background of both programming and engineering, with some work in operations research, so he is quite a reasonable competitor. He appears to be aggressive, likable, industrious and knowledgeable. He appears to have the right connections with the ministries (technology, etc.) and of the universities (Cambridge, a grad., Oxford, etc.). I hope we're dealing at these levels too.

In summary, I believe the modular one is going to be a significant competitor in Europe. I hope we'll get going on the manufacturing there. Several other things which might help are:

1. The tie-in with U. of Newcastle to do their experimentation using a PDP-11 multiprocessor structure. Here we have to take the idea of multiprocessing seriously -- get it out of special systems, and into a commitment.

2. More selling of universities in the U.K. -- getting some prestigious ones is important. Our PDP-11 paper helps here. Despite the fact that our sales people may not understand the paper, the university types do -- besides if you don't understand the paper, please get them a copy of my book (Computer Structures: Examples and Readings, Bell and Newell, McGraw Hill).

3. Competitive analysis. Can't we show the PDP-11 performs better?

4. Improved PDP-11's. -- Here Barron is wondering what we are to do. He sees the potential to extend the PDP-11. -- Modular one can get bigger, too, but not quite so nicely.

Modular One

The modular one is good, but not great, so please let's not use it as a goal, but rather a benchmark. With a little patience, we can make the PDP-11 almost great.

Instruction Set

Supposedly it was designed to compile and execute the AED language. A user program has three protected (and relocated) segments (execute-only, work space, and global work space for inter-process communication). Its instruction-set structure isn't bad, but according to the

three universities people I talked with, it has too many hardwired mechanisms, like the three segments -- and they aren't necessarily the right mechanism for all languages, and applications. I hope our segmentation scheme in the 11/40 is much better. All in all, their instruction set appears to be less than an 11/20; but with their crude segmentation scheme, one can write a reasonable monitor.

Structure

About the coupling of processors, memories, etc. to farm multi-computer and multi-processor structures: the modular one seems to be better than PDP-11, but it is also more expensive to implement. Since, I have constructed Modular one PMS figures from my memory, they may not be accurate. The modular one isn't as flexible as they might have you believe, because there ore lots of restrictions on numbers and types that communicate. Thus, when all the smoke clears, it looks like my general model of a computer which was around in 1966 (see book by Bell and Newell) of a computer which was around in 1966. If you look at the PMS figures of Modular ane, not their glib talk, and probably hidden restrictions, it has solved no problems. In fact, the cabling, for the rather exotic structures is a real mess (see figures).

Logic

Their technology is ECL, mounted on the same style lousy, pre-3rd generation, 2 sided boards, as PDP-11 uses. Their machine is quite fast, the polling of 8 ports into memory takes only 20 ns -- which is mighty impressive. Since their speeds are higher, and they have pretty bad transmission lines, signals and noise are probably equally poor in the two computers. Their interunit transmission lines are differential, thus, I suspect there's a better chance of getting the correct data transmitted between two units. I don't know whether they transmit parity, but if they don't, it's naiveté; the PDP-11 attitude (as expressed say by a field salesman) is one of a cavalier, and also unethical and stupid.

Cabinets

Their cabinetry is almost great in comparison by PDP-11 cabinet. The DEC cabinet hasn't changed in about 8 years (after the PDP-1 prototypes) except to get momentarily worse with PDP-7 for cooling, and incrementally better with PDP-9 and 10. The PDP-11 is pretty near the worst of DEC's cabinetry from a convenience-accessibility-cabling-coding viewpoint, so almost anything with a concept is good. The modular one uses about 16" wide x 32" tall x 16" deep frame. Like DEC, its power supply is on one side (a door) and its logic on the other. There is almost no waste space, and the modules are tested with extenders. There is no back panel wiring, only a large PC board for the connectors. The airflow pattern is U-shape, coming in over the top of the power supply, down to the $4 long, squirrel cage fan at the bottom of the cabinet, up through the modules. The modules are 2, 4 and 6 connectors long (about the same size as 5, 10 and 20" DEC modules.

Another interesting characteristic of their cabinet is that it is modular (up to 3 high although they only usually stack 2). There is space between cabinets for cables. This is needed because their wild configuration uses lots of cables. All in all, we would do well to copy their cabinets.

Software

They have some of the university types interested. Customers are adding facilities. A BCPL runs on the computer, and they are building a PL/360 - like language which will use assembler syntax with block-structure variables control. Strachey supposedly put up an operating system on it within 48 hours after it arrived. Strachey is using it for experimentation on kernel languages, etc.

Contacts with me and UK people

For my part, I've spent time at the University of Newcastle (with DEC people) and I think they want to use PDP-11's in their very reliable computer structure research. I possibly might have been useful at Cambridge and Oxford (and would have received valuable inputs). -- The next time I visit the U.K., I'll be more specific about who I want/or should see and arrange to see them. I'd like to have the U.K. office keep me directly informed about British machines - or should/can I get the information from Maynard? (If you tell me when Strachey is to be in the U. S. next, I'll go see him.)

At the Copenhagen conference, I also talked with:

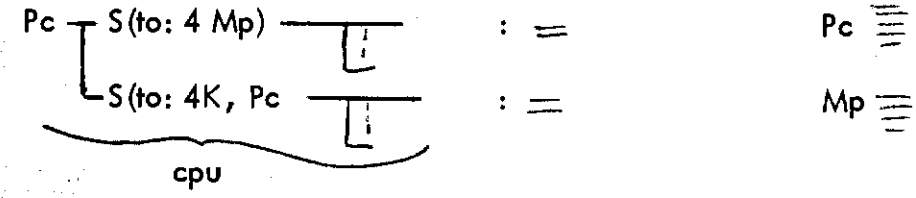
1. Dr. Spratt
   28 River Court, Chartham
   Canterbury, Kent,

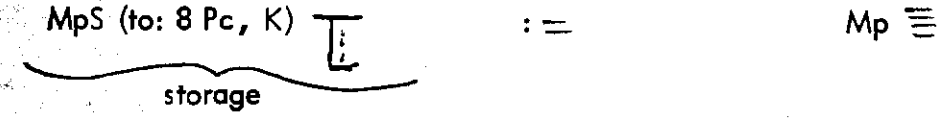
2. Dr. M.H. Rogers
   U. of Bristol

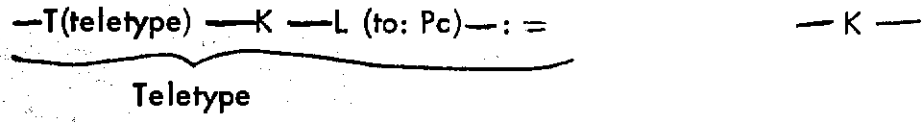
   Both were interested in PDP-11.

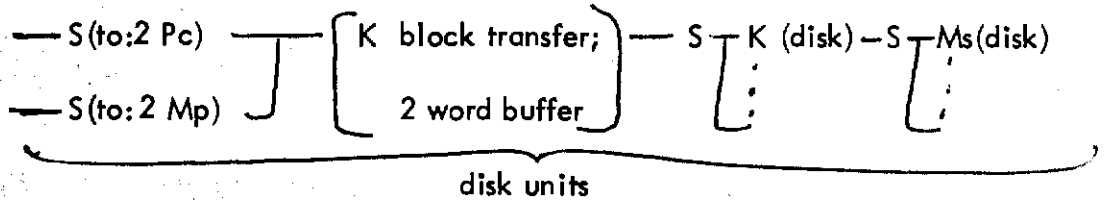
bwf

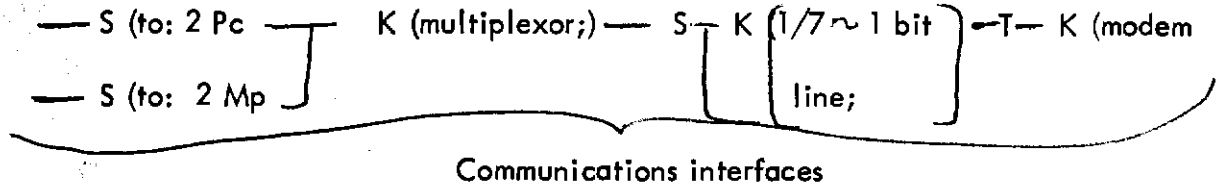
Some Modular One Structures



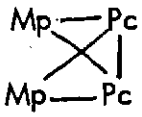








Some structures: C: = Mp— Pc — K (Teletype)— or



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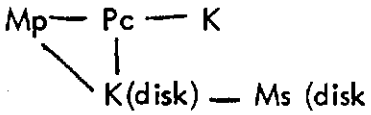

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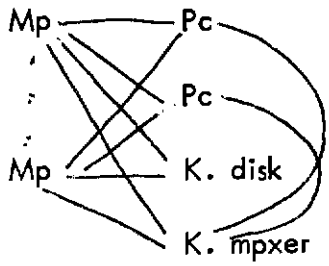


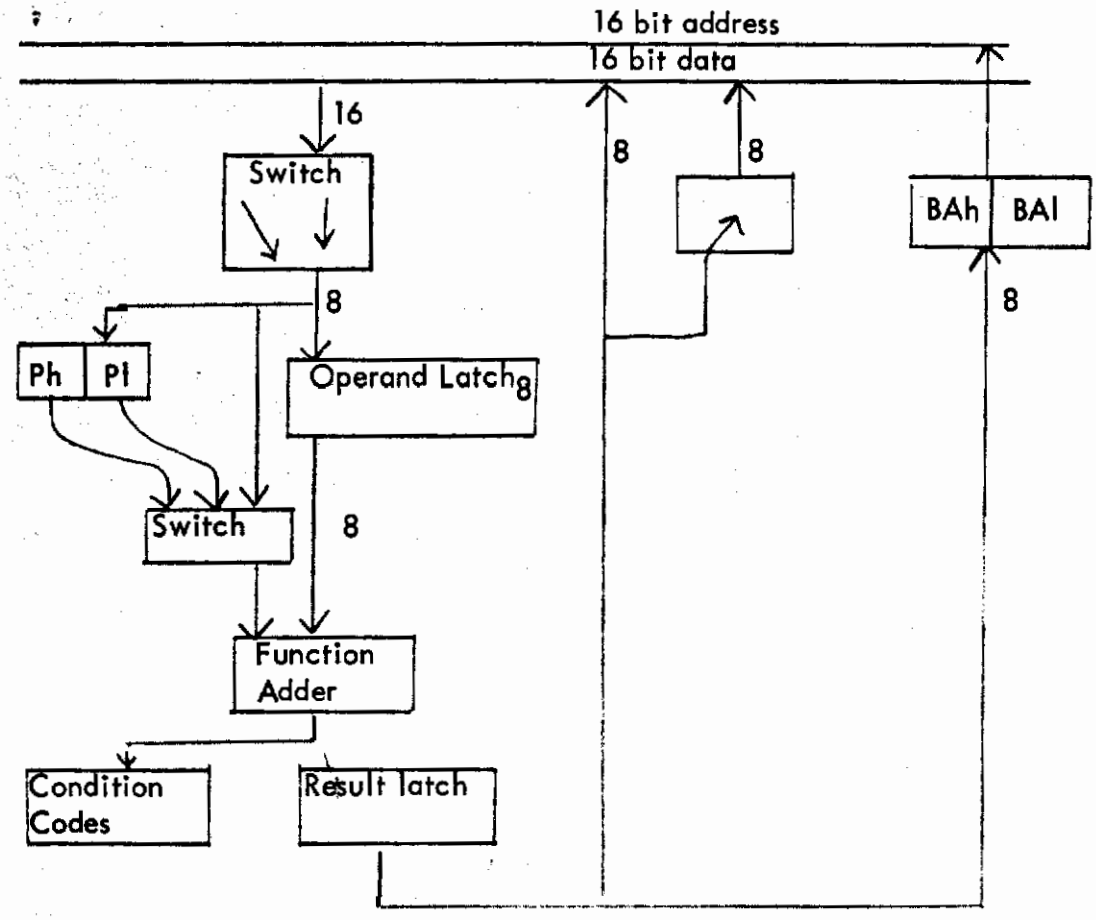
digital INTEROFFICE MEMORANDUM

SUBJECT: 8 Bit Processor Subset of PDP-11 DATE: December 18, 1970

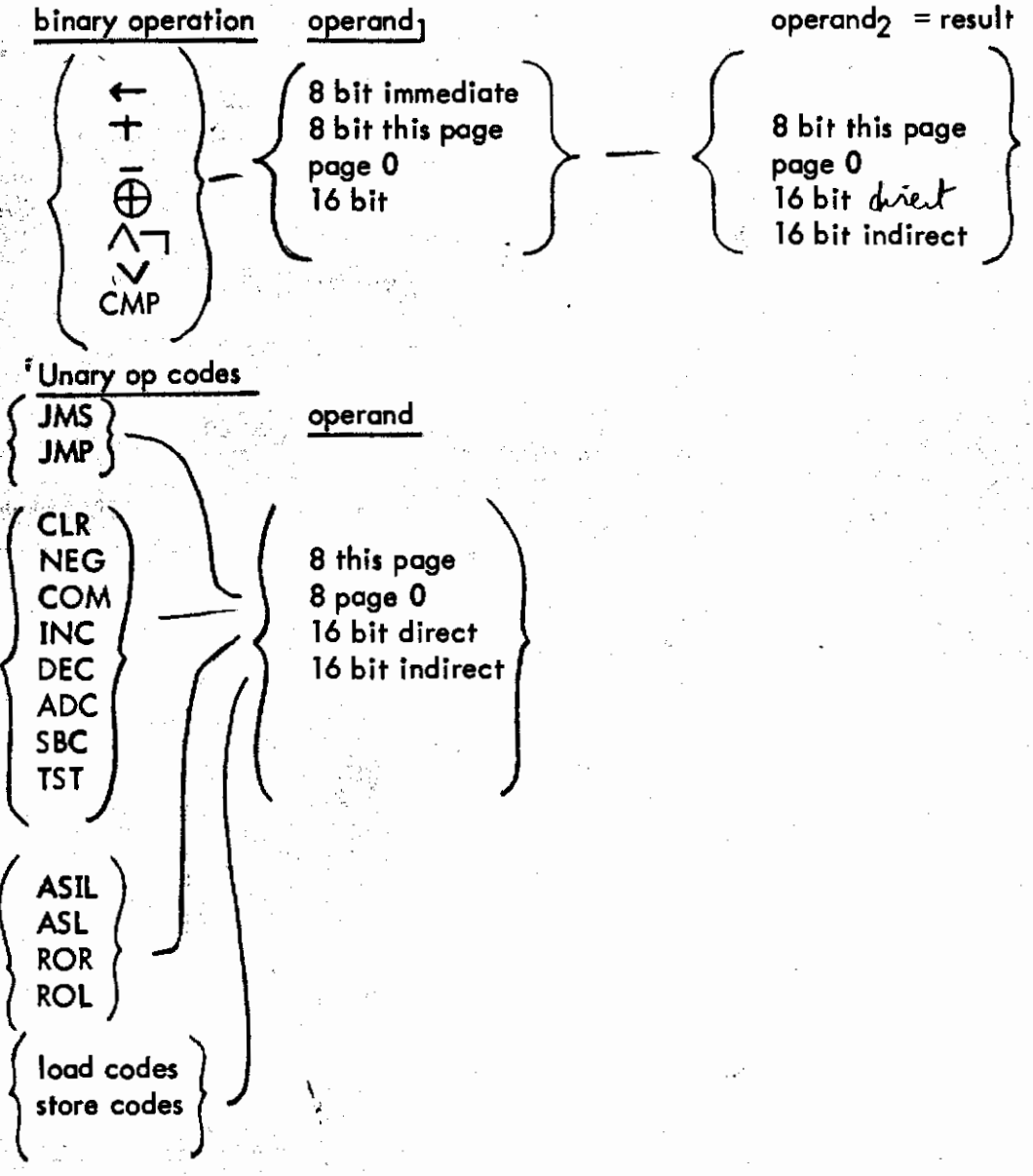
TO: Dave Chertkow FROM: Gordon Bell

Roger Cady
Jim O'Loughlin
Chuck Kamen DEPARTMENT:

Below is the register path for the above that we discussed on the phone. This basically has no registers - is 8 bit byte oriented.



This gives an 8 bit op code of roughly:



branch conditional

INTEROFFICE MEMORANDUM

SUBJECT: Graphical Tablet and Console

DATE: February 8, 1971

TO: Computer Strategy Committee

FROM: Gordon Bell

cc: Display Committee

DEPARTMENT:

Alan Kay of the Stanford Artificial Intelligence Project visited us the other day and discussed a very small terminal which he is building. It had an Owens-Illinois plasma panel with 64 dots/inch and a total of 512 x 512 (8 in. sq.). Aside from the built-in computer part of it, and the keyboard, the most interesting part was a graphical tablet which, though based on an old idea, now works. I saw a similar device operate a long time ago with conductive glass, but the glass wasn't good to write on or even enough. He uses surgical rubber conductive (used in operating room to carry off static charge) and stretches it across a square area as a tablet. Through diodes, he connects reference voltages in either the x or the y direction. You write on it with a conductive stylus and then pick up the voltage with an a to d. You get 9 bits of resolution in both x and y he claims. He also claims better resolution than the Sylvania tablet. The whole thing, excluding the a to d's, costs maybe $25. The rubber is about $5/sq. yard. He claims one can be built in the laboratory in an afternoon. I believe Len Halio can build and try it on the 15 graphics in less time. We are going to try one here, but it seems like a very nice device to have on the DEC machines instead of buying those expensive tablets. Roger, does it have any bearing as console keys for a PDP-11/05?

bwf Gordon Bell,
Len Halio,

5/24/71

Have we done anything about ~~dont~~ this suggestion? Sounds excellent if to seeing conductive glass operation. Rubber mfr. may not want to spec. the required conductivity tolerances.

John Holman

cc: (John Grason — you may copy if you want it. please return this, Gordon Bell.

digital INTEROFFICE MEMORANDUM

TO: Fred Gould
John Eggert

DATE: March 16, 1971

CC: Peter Williams, Bob VanNaarden, Al Walker, Dave Brown, Nick Mazzarese, Howie Painter, Andy Knowles, Ed Kramer, Stan Olsen, Lorrin Gale, Al Devault, Bill Long, Roger Cady

Mprogram.

FROM: Gordon Bell

SUBJECT: A computer on a Quad Board: The RTM Microprogrammed Control for Link Driver Trainer Bid

We talked about the above control and the Driver Training Car Controller problem. Friday afternoon I met with 8 - 11 people too, and it begins to be clear to me that we can attack the problems with RTMs and wipe out the computer in this case. We would also use this on the new Hycel controller. The basic methods I see for digital controllers are:

1. Sequential circuit machines - (conventional logical design) - no good because of complexity, design, inflexibility, etc.

2. Stored program computer for large problems - fine as long as cost is low.

3. RTM - hardwired controls (Kevoke, Kbranch, etc.).- cost too high for large systems, $5/control step.

4. RTM - good for small systems - hardwired control interpreter to first build a simple computer. Then use a stored program in a memory (Hycel approach). - likely to be too expensive because it first requires building o stored program computer.

5. A centralized, microprogrammed controller to directly evoke RTM register transfers. The final opplication control algorithm would be in the microprogrammed memory. The controller is fundomentally trivial - unlike one that might first be a PDP-8 interpreter, for exomple.

6. Combination of microprogramming and conventional programming (Firmware). The Interdato approach. A general purpose interpreter is put in the microprogrammed memory, along with special operations. Unlike, approach 5, instructions are stored in other memories and the control algorithm resides in a memory which is interpreted.

The basic structure of an RTM system for an application is shown in Figure 1. Thus in a conventional RTM design the box on left would just be a collection of the evoke, merge, and branch control modules (ot $5 per module).

All I'm proposing is to introduce a 1 quad board controller shown in Figure 2 to replace the distributed, hardwired control. Using this approach, the cost of the controller is only about $.10/step or a sales

price of say $.35/step - a cost factor decrease of about 30. Since the micro controller (Figure 2) has about 1 board it might sell for about $200 (plus memory). The crossover point when a read only approach pays would be about 40 control steps ($5 x 40).

The user would still flow chart in basic RTM form, and the step would not reside in the micro controller's memory. The readers may recognize it as being very much like a PDP-14.

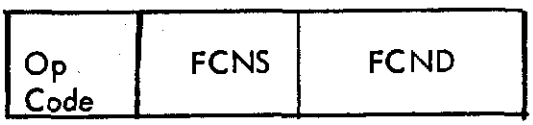
There are many approaches to the micro controller's instruction word layout - two are:

1. A wide word to evolve operations, select next micro instruction based on boolean inputs.

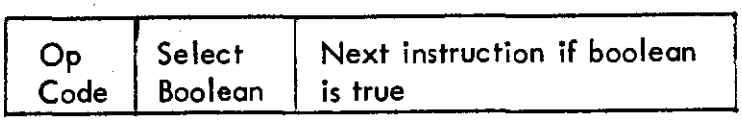
2. A very short word with bits to tell what kind of control step.

Using the second approach we could have these instructions:

Evoke instruction ≡ Evoke control



(Note: maybe only one evoke field is needed as we use now. The above has two fields for source and destination which might make use easier and cheaper.)



(branch if boolean is true)

If these two instructions are enough, we can have a 1 bit op code. Otherwise, two other instructions are very useful:

1. Load immediately part onto RTM data part (the bus). This is used to place constants into the data parts.

2. Some method of using subroutines:

   a. Have a few flags which can be set to encode the caller such that the subroutine knows where to return.

b. Use a 3-bit register and put in an 8-way branch instruction to encode the return.

c. Put 1 or 2 registers to save the MPC register so that nesting of subroutines is permitted. (This amounts to a stack which is just a few registers deep.)

d. Assume the load immediate instruction, then an instruction which loads MPC from the data part could be used for the return.

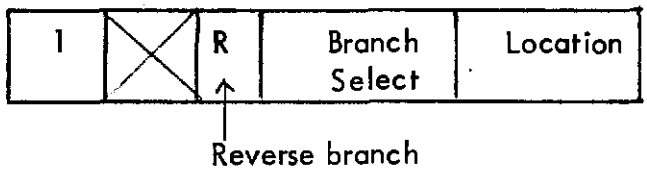
I prefer this last method for subroutines. Note, it has the advantage of not costing a register if it is not used. A normal transfer register would be used for it.

Also note that because of the intimate connection with the bus, K bus might be included in the micro-controller - for these type systems to save cost.

A reasonable word size might be 9 bits which would allow up to 512 step controls. This can easily be shrunk to 8 bits for up to 256 steps (shown below). The op code layout:

EVOKE

Load CONSTANT



Branch if boolean true, false

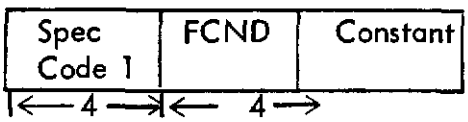
(Note: subroutine return is an evoke with MPC as an addressable destination)

The list price would be:

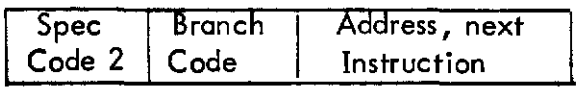
1	GPA	310	
1	K micro	250	
1	ROM (300 words)	100	(let them buy it)
1	R-W (64 w)	200	
	transfer and i/o interface registers	300	
		$1,160	

An 8 bit version (up to 256 steps):

Evoke



Load Constant



Branch if true

A 12 bit version is almost like PDP-14 -- but not quite since PDP-14 has skips (which usually requires a transfer in next location) transfers and evokes (without source and destination).

bwf

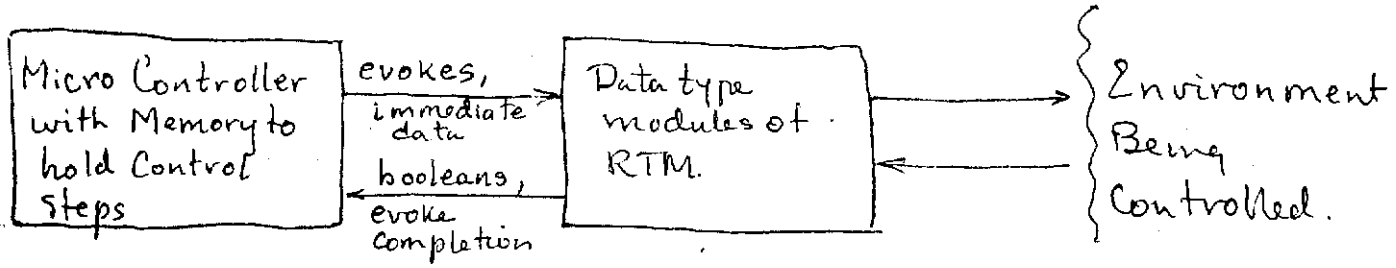
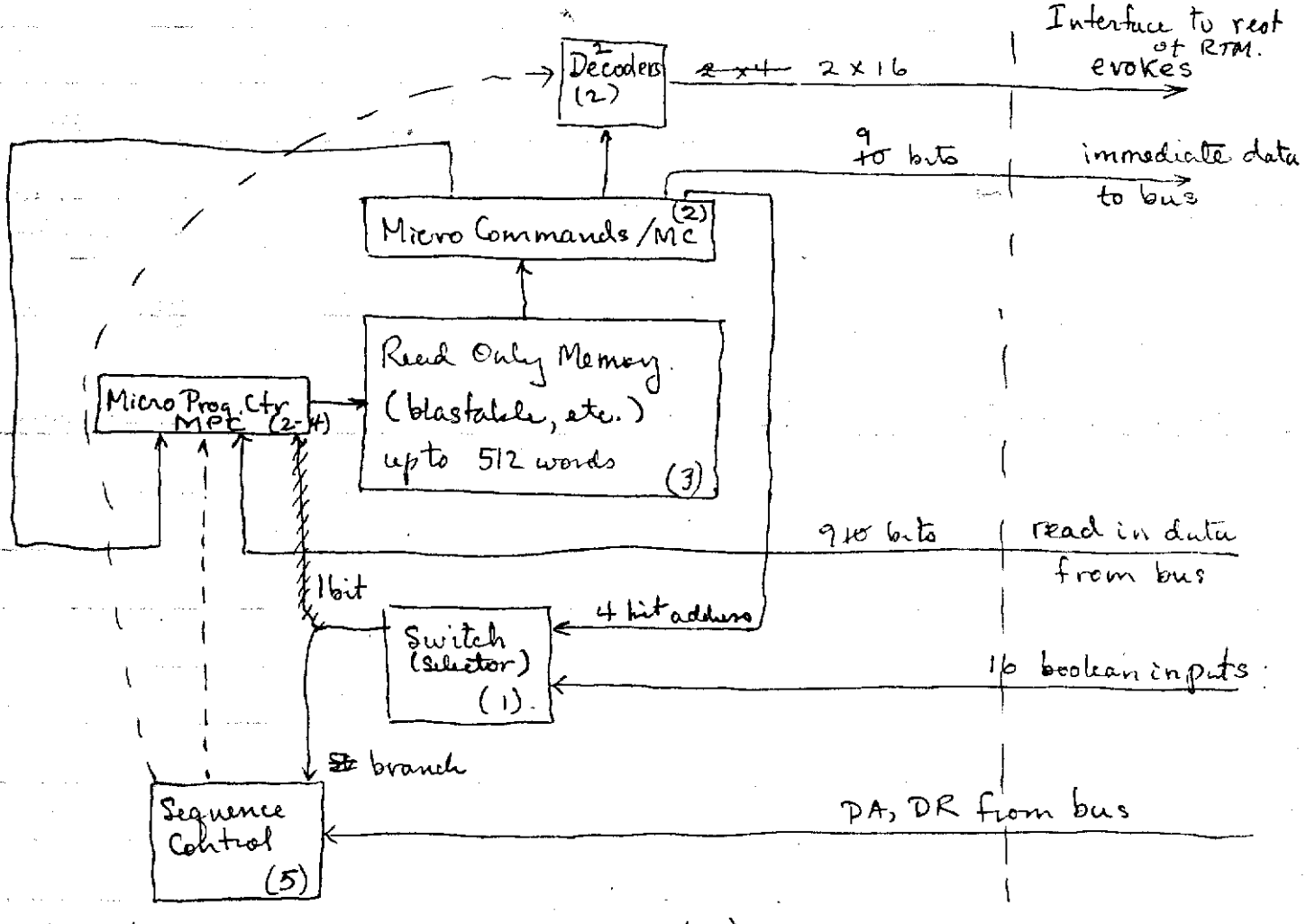


Fig. 1 RTM System with a Micro Controller (instead of Conventional, RTM distributed control).



(numbers indicated the IC count).

Fig. 2 Registers in Micro Controller (approx 20 IC's including read only memory.

CgB 14 Mar 70

INTEROFFICE MEMORANDUM

TO: Computer Strategy Committee
Grant Saviers
Jim Bell

DATE: December 21, 1971

FROM: Gordon Bell

DEPT:

SUBJ: New Fixed Head Disk

I've heard that a new, 3600 RPM fixed head disk is being designed. (This did not come through the minutes of the Computer Strategy minutes.) Why, when we are in our current position with regard to peripherals, do we take on an aeronautical engineering task that has in the past proven to be our nemesis? Aside from the difficulty of the task, aren't priorities for moving head disks more important? Forgetting these two basic reasons, why can't we get what is essentially the same effect for almost every application (except perhaps communications), by increasing the density (which is to be done anyway), or by changing the configuration to take multiple heads in parallel? Finally, if we're up against latency (e.g., in communications) then a hardware (or software) queuer has been and can be used to increase performance more than halving the latency. Again this is comparatively trivial.

Let's not take on engineering problems that we create.

bwf

original INTEROFFICE MEMORANDUM

TO: Roger Pyle
Computer Strategy Committee

DATE: February 25, 1972

FROM: Gordon Bell

cc: Ed Correll, Stan Olsen, Nick Mazzarese, Ted Johnson, Dave Brown, Len Halio

DEPT:

SUBJ: Possible Printer, Page Proof Printer, Typewriter, Using Incremental Techniques

Attached to this memo is a copy of output from a printing system we have been developing an the PDP-10 and a PDP-11. The actual printing is done with a program in the PDP-11 which controls an LDX (Long Distance Xerography) which Xerox gave to us. Apparently the LDX didn't make it as a product. The scanning is done in 5 milliseconds, and there are the equivalent of 1600 points across the 8 inches, and 200 scan lines per vertical inch. The paper moves at 1 inch/second. The interesting possibility is that it can also be used with graphics and has potential as a high quality line printer, multifont typewriter, and it would be useful to give quick looks for galley and page proofs in the printing industry. We have been inputing type fonts and now have a reasonably large library. We also have a system for manuscript preparation which includes final printing in this form. New character sets are input by drawing them on a scope (ARDS-type) by Video and by modifying an existing font. Almost every font has to be input separately although it can be derived from another and then cleaned up with the edit-drawing program.

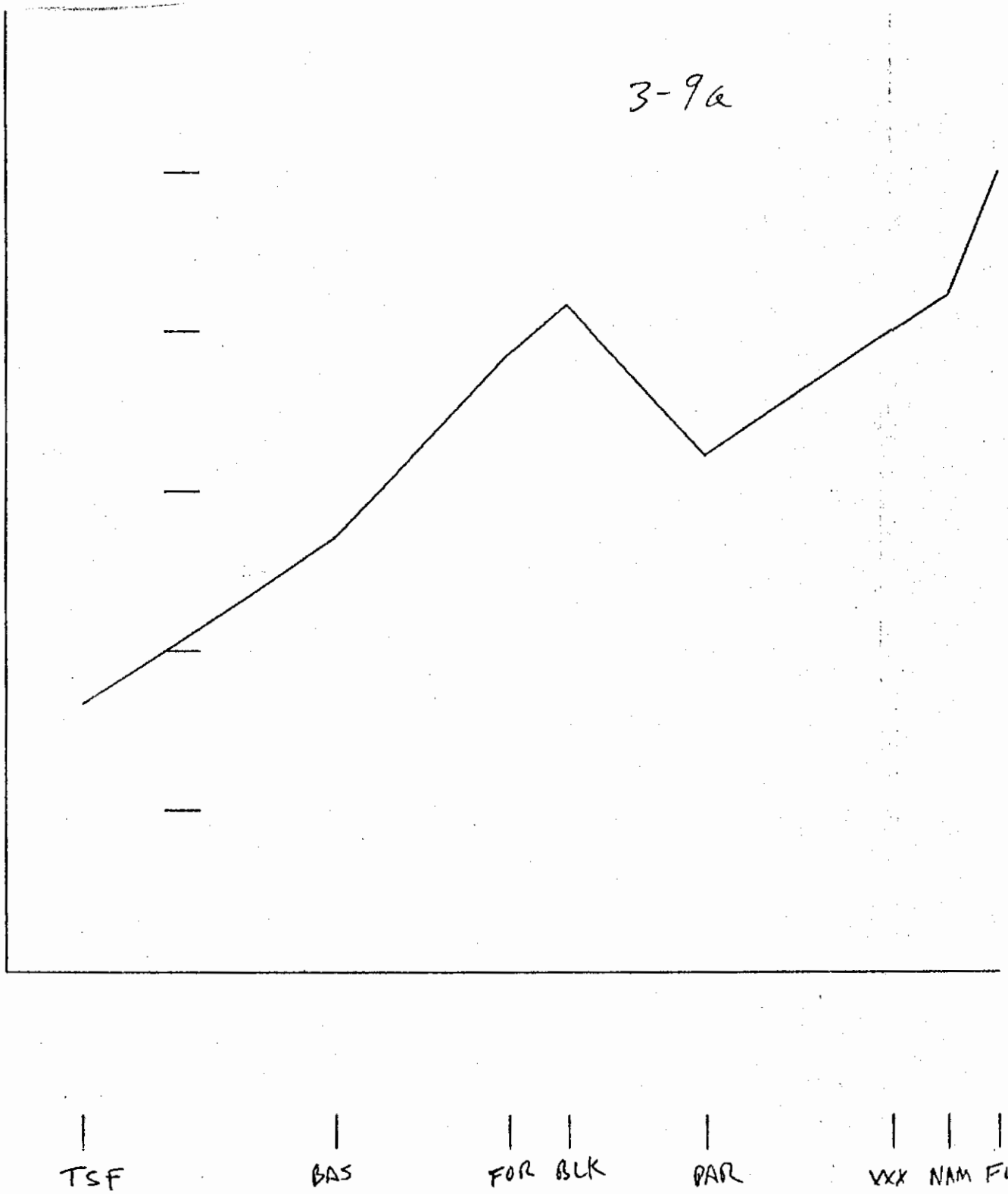
I understand we have a similar but cheap printer on a PDP-8/PDP-11 that could be used like this.

We (CMU) are planning a two-day session on future printing and display techniques for April.

bwf

Attachments

3-9a



00100
00200 Ash71a Ashcroft, E. and Manna, Z. The translation of go to
00300 programs to while programs. Memo AIM-138(CS-71-188),
00400 Stanford University January 1971.
00500
00600 Keywords and phrases: correctness, terminations.
00700
00800
00900 Ash71b Ashcroft, E. and Manna, Z. Formalization of properties of
01000 parallel programs. Memo AIM-118, Stanford University
01100 February 1971.
01200
01300 Keywords and phrases: correctness, terminations.
01400
01500
01600 Bac57 Backus, J. W., et.al and Balzer, R. M. The Fortran
01700 automatic coding system. Proceedings WJCC 11 (1957),
01800 188-198, 29-47, 535-544.
01900
02000 Keywords and phrases: structured programming.
02100
02200
02300 Bal69 Balzer, R. M. EXD: AMS--Extendable debugging and monitoring
02400 systems. Proceedings FJCC 1969, pp. 567-580.
02500
02600 Keywords and phrases: debugging.
02700
02800
02900 Bar70 Barley, J. and Sturgis, H. A formalism for translator
03000 interactions. CACM 13 #10 (October 1970), 607.
03100
03200 Keywords and phrases: exportability, mobility.
03300
03400
03500 Bern68 Bernstein, W. A. and Owens, J. T. Debugging in a
03600 time-sharing environment (PCS). Proceedings FJCC 1968, pp.
03700 7-14.
03800
03900 Keywords and phrases: debugging.
04000
04100
04200 Boh66 Bohm, C. and Jacopini, G. Flow diagrams, Turing machines
04300 and languages with only two formation rules. CACM (1966).
04400
04500 Keywords and phrases: correctness, terminations.
04600
04700
04800 Bra68 Brady, Paul T. Writing an online debugging program for the
04900 experienced user. CACM (June 1968), 423-427.
05000
05100 Keywords and phrases: debugging.
05200
05300
05400 Brat61 Bratman, H. An alternate for of the UNCOL diagram. CACM 4
05500 #3 (March 61), 142.

```
*       PRODUCTION LOADER AND INTERPRETER FOR ALGOL-LIKE LANGUAGES
*          COMMENCED 26 MAY 70
*          MARY SHAW
*
*       REFERENCE: EVANS, ARTHUR, AN ALGOL 60 COMPILER.
*          ANNUAL REVIEW IN AUTOMATIC PROGRAMMING, V. 4, 1964
*               EVANS DESCRIBES A COMPILER ORGANIZED IN THREE
*               SECTIONS.  THE FIRST (SUBSCAN OR SS) READS
*               SOURCE CARDS AND PERFORMS LEXICAL ANALYSIS.
*               THE SECOND (PHASE IOR PH1) INTERPRETS
*               FLOYD-EVANS PRODUCTIONS TO CONTROL SYNTACTIC
*               ANALYSIS AND GENERATE A POSTFIX REPRESENTATION
*               OF THE PROGRAM.  THE THIRD (PHASE II OR PH2)
*               PROCESSES THE OUTPUT OF PHASE I TO PERFORM
*               SEMANTIC ANALYSIS AND GENERATE CODE.  THE
*               PHASES ARE COMMONLY ARRANGED AS COROUTINES.
*
*    OPERATING INSTRUCTIONS
*       THIS PROGRAM LOADS AND INTERPRETS FLOYD-EVANS
*       PRODUCTIONS AS DESCRIBED BY EVANS.  TO RUN THE SYSTEM:
*     1. STORE THE PRODUCTIONS DEFINING THE LANGUAGE AND THE
*       PROGRAMS TO BE COMPILED ON A FILE AS DESCRIBED BELOW.
*       (PIP MAY BE USED TO CONCATENATE THE PROGRAM AND THE
*       LANGUAGE IF THEY ARE STORED SEPARATELY.)
*     2. EXECUTE THE MONITOR COMMAND
*            .R SNOBOL
*       WHEN SNOBOL RESPONDS WITH AN ASTERISK, ANSWER WITH THE
*       NAME OF THE FILE ON WHICH THIS PROGRAM IS STORED.
*       SAY, <NAME>.SNO
*     3. WAIT PATIENTLY WHILE THE PROGRAM LOADS.  WHEN
*       LOADING IS COMPLETE, THE PROGRAM WILL PROMPT
*          FULL TTY OUTPUT? RESPOND Y OR N
*          *** WHAT FILE CONTAINS THE LANGUAGE?
*          ***WHERE DOES PH1 OUTPUT GO?
*       WAITING AFTER EACH QUESTION FOR YOUR RESPONSE.  THE
*       FIRST QUESTION DETERMINES WHETHER THE OUTPUT FROM PHASE 1
*       WILL BE PRINTED ON THE TELETYPE.  THE SECOND AND THIRD
*       ASK, RESPECTIVELY, FOR THE INPUT AND OUTPUT FILES.
*     4. THE PROGRAM WILL LOAD THE LANGUAGE DEFINED ON THE
*       INPUT FILE AND PARSE THE PROGRAMS THAT FOLLOW THE
*       DEFINITION.  THE RESULTING POSTFIX (THE LEXEME STRING THAT
*       PHASE 1  WOULD PASS TO PHASE 2) AND PHASE 1 COST ANALYSIS
*       FOR EACH PROGRAM WILL BE DIRECTED TO THE OUTPUT FILE YOU
*       NAMED AT THE BEGINNING OF THE RUN.  CERTAIN OUTPUT WILL
*       ALSO BE GENERATED ON THE TELETYPE AND THE FILE <NAME>.LST
*       CORRESPONDING TO THE SOURCE FILE FOR THIS PROGRAM.
*     5. WHEN ALL PROGRAMS ON THE INPUT FILE HAVE BEEN PARSED,
*       SNOBOL WILL RETURN WITH AN ASTERISK.  YOU MAY NOW RUN
*       ANOTHER SNOBOL PROGRAM OR TYPE ^C TO RETURN TO MONITOR
*       CONTROL.
*
*    INPUT FORMAT
*          (REFER TO EXAMPLE THROUGHOUT)
*
*       ORGANIZATION OF THE FILE
*
*       EACH SECTION BEGINS WITH A HEADER CARD IDENTIFIED BY
*       '!!' IN COLUMNS 1 AND 2
*           !! PRODUCTIONS  OR  !! PRINT PRODUCTIONS; <TITLE>
*              <THE PRODUCTIONS>
*           !! HIERARCHIES
*              <THE HIERARCHIES>
*           !! METACLASSES
*              <THE METACLASSES>
*           !! RESERVED WORDS
*              <THE RESERVED WORDS>
*           !! PRINT TABLES   (ONLY IF DESIRED)
*           !! PROGRAM
*              <PROGRAM TO BE COMPILED>
*       IF THE FIRST CARD IS 'PRINT PRODUCTIONS' INSTEAD
*       OF 'PRODUCTIONS', THEN THE INPUT IS ECHOED ON THE
*       OUTPUT FILE AS IT IS READ.  THE OPTIONAL CARD
*       'PRINT TABLES' CAUSES A PRINTOUT OF THE LOADED
*       PRODUCTION TABLES, INTERPRETATION LIST, ETC.
*           !! PROGRAM
*              <PROGRAM TO BE COMPILED>
*                     ......
*           !! END
*
*    CARD FORMATS
*
*       PRODUCTIONS
*       NOTE: ALL FIELDS MUST BE LEFT-JUSTIFIED.
*           COL 1-4      LABEL
*           5            BLANK
*           6-9          FIFTH ELEMENT OF OLD STACK
*           10           BLANK
*           11-14        FOURTH ELEMENT OF OLD STACK
*           15           BLANK
*           16-19        THIRD ELEMENT OF OLD STACK
*           20           BLANK
*           21-24        SECOND ELEMENT OF OLD STACK
*           25           BLANK
*           26-29        TOP ELEMENT OF  OLD STACK
*           30           BLANK
*           31           !  (EXCLAMATION POINT)
*           32           :   IF A REPLACEMENT IS TO BE MADE IN THE EVENT
*                           OF A MATCH, OTHERWISE BLANK
*           33           BLANK
```

JMAX - 0 - (non-negative integer) Specifies the maximum number of bits the justifier is allowed to add to a line. If more than this number of bits are needed, then the line is left unjustified.

LOCKUP - NO - (YES, NO) Specifies whether or not core lockup should be used in real-time modes. Note that lockup cannot be used unless you are running under a project with the lockup priviledge.

MODE - TEXT - (TEXT, VECTOR, INKSET, OUTKSET,MIXED,IMAGE) Specifies how a file is to be handled. See below for a complete description of the different modes.

2.3 Modes

The following modes of operation determine how a user file is to be handled. The mode also determines how communication with the PDP-11 will be handled.

1. TEXT mode sends the current parameter settings for AKSET, BKSET, VERT.SPACING, LFTMAR, TOPMAR, BOTMAR, NLINES, CUT, and JWIDTH and JMAX if JUSTIFY is set to YES. Then text lines are sent from the specified file, line at a time, with or without line numbers as specified by LINENUMS.

   Once the parameters have been specified, the text mode deals only with text. It prints text lines (a string of characters terminated by LF) until an EOF character is seen (see escape conventions below). Null characters (octal code 0) are always ignored.

   The escape character is the rubout (octal code 177). The character following a rubout is interpretted as an escape code. The escape codes (in octal) along with their meanings are listed below.

Code	Meaning
0	End of file
1	Vertical spacing in next two characters
2	Left margin in next two characters
3	Top margin (2 characters)
4	Bottom margin (2 characters)
5	Number of text lines per page (2 characters)
6	Automatic cut
7	Manual cut

```
00100
00200
00300     AEAGE  EE
00400
00500
00600     BGG  EE
00700
00800
00900       EE
01000
01100
01200     E  EE
01300
01400
01500       AED
01600
01700
01800     DE  E  EE
01900
02000
02100     CE  E  EE
02200
02300
```

'n' th version. March 21

00100
00200
00300
00400
00500
00600
00700
00800
00900
01000
01100
01200
01300
01400
01500
01600
01700
01800
01900
02000
02100
02200
02300
02400
02500
02600
02700
02800

ATTOPROCESSOR

ASSEMBLY LANGUAGE

DOCUMENTATION

****

00100
00200
00300
00400
00500
00600
00700
00800
00900
01000
01100
01200
01300
01400
01500
01600
01700
01800 INTRO :
01900 -----
02000 ASSEMBLY LANGUAGE FOR THE ATTOPROCESSOR CAN BE
02100 CLASSIFIED IN ESSENTIALLY TWO SECTIONS, IT CONSISTS OF THE
02200 MACHINE OPS AND THE PSUEDO-OPS, AS ONE MAY READILY GUESS
02300 THE PSUEDO-OPS ARE THOSE THAT ARE OPS FOR THE ASSEMBLER
02400 AND DO NOT GENERATE CODE, THE MACHINE OPS RESULT IN
02500 GENERATION OF UNIQUE CODE, IF AND WHENEVER THE INSTRUCTION
02600 IS 'LEGAL' , (BY 'LEGAL' IS MEANT ONLY THE SYNTACTIC
02700 CORRECTNESS, IT DOES NOT MEAN A CHECK OF PROGRAM FLOW,
02800 ALTHOUGH AN ATTEMPT IS MADE TO CATCH AS MANY FLOW ERRORS
02900 AS EXIST IN THE SCOPE OF THE ASSEMBLER, FOR EXAMPLE, THE
03000 USER IS WARNED WHEN A DOUBLE WORD INSTRUCTION IS NOT
03100 FOLLOWED BY SOME STORAGE DECLARING INSTRUCTION; HOWEVER,
03200 IT IS NOT TREATED AS AN 'ERROR' ,),
03300

```
00100
00200   PSUEDO-OPS :
00300   ------ ---
00400   ORIGIN                                          ORG <NUM>
00500           THE ORIGIN STATEMENT IS USED TO SET
00600           PROGRAM LOCATION COUNTER TO THE
00700           VALUE SPECIFIED IN <NUM> . THIS
00800           NUMBER MUST LIE WITHIN 0 AND 377
00900           (OCTAL).
01000
01100   DEVICE DECLARATION                              <DVC NAME> = <NUM>
01200           USED FOR GIVING A NAME TO A DEVICE.
01300           ALL DEVICE NAMES MUST START WITH 'D'.
01400           THE <NUM> MUST LIE WITHIN 0 AND 37
01500           (OCTAL). USER MUST KEEP IN MIND THAT
01600           THE DEVICE NAME BINDING IS DONE
01700           DYNAMICALLY WITH RESPECT TO THE TEXT
01800           OF THE ASSEMBLY LANGUAGE PROGRAM.
01900
02000   TERMINATION                                     END
02100           USED TO TERMINATE THE ASSEMBLY.
02200
02300   MACHINE OPS:
02400   ------- ---
02500                   AGAIN IN THE MACINE OPS WE DISTINGUISH
02600   BETWEEN TWO CLASSES, ASSMBLER INSTRUCTIONS AND MACHINE
02700   INSTRUCTIONS , THE MACHINE INSTRUCTION IS
02800   TRANSLATED AS AN INSTRUCTION WHILE AN ASSEMBLER INSTRUCTION
02900   IS TRANSLATED AS DATA, OF COURSE, THANKS TO VON NUEMANN,
03000   AFTER THE TRANSLATION THERE IS NO DIFFERENCE BETWEEN THE
03100   TWO, FOR EXAMPLE, THE TEXT X←(0) IS TREATED AS A MACHINE
03200   INSTRUCTION AND THE CODE GENERATED IS 01000001, WHILE
03300   THE TEXT 'A IS TREATED AS AN ASSEMBLER INSTRUCTION ( IT
03400   MEANS AN ASCII CHARACTER "A" ) AND IS GIVEN ITS DATA FORM
03500   NAMELY, 01000001, CLEARLY, THERE IS NO WAY OF DISTINGUISHING
03600   BETWEEN THE TWO AFTER THE TRANSLATION.
03700
03800   ASSEMBLER INSTRUCTIONS :
03900   --------- ------------
04000   ASCII CHARACTER                                 '<SINGLE CHARACTER>
04100           ANY ASCII CHARACTER EXCEPT A
04200           BLANK AND A SEMICOLON.
04300
04400   BINARY STRING                                   "<BIN STRING>
04500           ANY BINARY STRING, THE VALUE OF
04600           THE NUMBER MUST BE LESS THAN
04700           400 (OCTAL).
04800
04900   ADDRESSING                                      ,<EXPR>
05000           ANY ADDRESS EXPRESSION IS
05100           PERMISSIBLE BUT IT MAY NOT
05200           INCLUDE MORE THAN ONE NON-
05300           PREDECLARED LABELS . ALL
05400           CONSTANTS MUST BE IN OCTAL,
05500           THE VALUE OF EXPRESSION MUST
05600           LIE WITHIN 0 AND 377 (OCTAL).
05700           <EXPR> MAY CONTAIN + AND - .
05800           * MAY BE USED TO DENOTE CURRENT
05900           VALUE OF PROGRAM COUNTER.
```

```
00100
00200   MACHINE INSTRUCTIONS :
00300   ------- ------------
00400           OF THE FOLLOWING, ALL BRANCHES AND
00500           THE  SUBROUTINE-CALL  INSTRUCTIONS
00600           ARE DOUBLE WORD INSTRUCTIONS,  THE
00700           SECOND  OF  THESE  WORDS  IS  THE
00800           OPERAND.
00900
01000
01100   MOVE                                          <REG1>←<REG2>
01200           <REG1>  IS  THE  DESTINATION,
01300           <REG2>  IS  THE  SOURCE,  ANY
01400           GENERAL  REGISTERS ,  IF  THE
01500           <REG>=M  THEN  THE  REFERENCE
01600           IS TO MEMORY LOCATION POINTED
01700           TO BY THE REGISTER A.
01800
01900   FUNCTION                                      Q←(<F(Q)>)
02000           Q  MAY  BE  ANY  OF W,X,Y,A,
02100           FOR <F(Q)> SEE THE SECTION.
02200           NOTE;  FOR  TWO-OP FUNCTIONS
02300           THE SECOND OP MUST BE R.
02400
02500   OUTPUT                                        <DVC NAME>←W
02600           THE REGISTER MUST BE W.
02700
02800   INPUT                                         W←<DVC NAME>
02900           AGAIN, THE REGISTER MUST BE W.
03000
03100   EVOKE                                         EV <DVC NAME>
03200           TO ISSUE EVOKE AND WAIT FOR
03300           DONE.
03400
03500   TEST AND BRANCH                               ↑ <DVC NAME>
03600           BRANCH IF THE FLAG OF THE
03700           DEVICE IS SET.
03800
03900   SUBROUTINE CALL                               CL
04000           CALL THE SUBROUTINE.
04100
04200   RETURN                                        RT
04300           RETURN FROM SUBROUTINE;
04400           TO ADDRESS SPECIFIED BY
04500           REGISTER S .
04600
04700   UNCONDITIONAL BRANCH                          ↑
04800           GOTO.
04900
05000   CONDITIONAL BRANCH                            <COND> ↑
05100           <COND> MAY BE :
05200            NZ  => BRANCH IF NON-ZERO,
05300             P  => BRANCH IF POSITIVE,
05400             N  => BRANCH IF NEGATIVE,
05500             C  => BRANCH IF CARRY,
05600             V  => BRANCH IF LAST INCR
05700                   INSTRUCTION  CAUSED
05800                   Ø RESULT.
```

```
00100
00200   MOVE LITERAL                                    <REG>←L
00300           TO MOVE NEXT MEMORY WORD TO
00400           REGISTER SPECIFIED;
00500
00600   INCREMENT                                       <REG>←<REG>+1
00700           INCREMENT THE REGISTER OR THE
00800           MEMORY LOCATION (IF <REG>=M),
00900           IF RESULT=0 THEN SET V FLAG,
01000
01100   COMPARE                                         <REG>←<REG>-R
01200           SUBTRACT R FROM <REG>,
01300           MODIFY C,N,Z FLAGS;
01400
01500   ********************************************************************
01600
01700   NOTE :  ALL EXCEPT THE 'END' INSTRUCTION, MUST BE
01800           TERMINATED BY A SEMICOLON,
01900
02000   LABELS :
02100           LABELS  MAY  APPEAR  ON ANY MACHINE OP,
02200           A LABEL MUST BE FOLLOWED BY A COLON(:),
02300
02400   COMMENTS :
02500           COMMENTS  MAY APPEAR AT THE END  OR
02600           AT THE BEGINNING OF AN INSTRUCTION,
02700           COMMENTS MUST BE ENCLOSED BY  "/" ,
02800           A COMMENT  NEED  NOT  BE TERMINATED
02900           BY  A  SEMICOLON,  IF  A  SEMICOLON
03000           FOLLOWS A COMMENT  THEN, IT RESULTS
03100           IN  BEING   TREATED   AS  AN  EMPTY
03200           INSTRUCTION,
03300
03400   EMPTY INSTRUCTION :
03500           AN EMPTY INSTRUCTION (NO TEXT , BUT
03600           A SEMICOLON  EXISTS ) IS  ASSEMBLED
03700           AS S←S;
03800
03900
```

```
00100
00200
00300
00400
00500
00600
00700
00800
00900
01000   SECTION-I
01100   -------
01200           FUNCTION OP : F(Q)
01300
01400           CODE    FUNCTION                SYNTAX
01500
01600           0000    ZERO                    0
01700           0001    FULL REG                377
01800           0010    ONE'S COMPLEMENT        -Q
01900           0011    AND                     Q&R
02000           0100    OR                      Q!R
02100           0101    EXCLUSIVE OR            Q#R
02200           0110    ROTATE LEFT             Q,C-
02300           0111    SHIFT LEFT              Q,C-0
02400           1000    INCREMENT               Q+1
02500           1001    DECREMENT               Q-1
02600           1010    ADD                     Q+R
02700           1011    SUBTRACT                Q-R
02800           1100    ADD C                   Q+C
02900           1101    SUB C                   Q-C
03000           1110    ADD R,C                 Q+R+C
03100           1111    SUB R,C                 Q-R-C
03200
03300           WHERE Q= A OR W OR X OR Y ,
03400
```

SECTION-II

THE MACHINE 'ATTOPROCESSOR' HAS 8-BIT 256-WORD MEMORY. IT HAS SEVEN GENERAL PURPOSE REGISTERS, THEY ARE : R, S, T, W, X, Y, A . ALL I/O TRANSFERS MUST BE CARRIED OUT THROUGH THE REGISTER W ; REGISTER R IS USED AS THE 'SECOND' OPERAND IN FUNCTION AND COMPARE TYPE INSTRUCTIONS . ALL THE MEMORY REFERENCES ARE INDIRECT, AND ARE CARRIED OUT THROUGH REGISTER A . THE CODES FOR THE REGISTERS ARE AS FOLLOWS :

REGISTER	CODE
MEMORY	000
S	001
R	010
T	011
W	100
X	101
Y	110
A	111

FOR FUNCTION TYPE INSTRUCTIONS, ONLY W,X,Y AND A QUALIFY FOR THE 'FIRST' OPERAND, THEIR CODE THEN BECOMES

REGISTER	CODE
W	00
X	01
Y	10
A	11

THE MACHINE CODE MAY BE SUMMARISED IN A TABLE AS :

NAME	CODE
MOVE	0 0 * * * - - -
FUNC	0 1 $ $ $ $ & &
OUTP	1 0 0 0 % % % %
INPT	1 0 0 1 % % % %
EVOK	1 0 1 % % % % %
TEST	1 1 0 % % % % %
BRAN	1 1 1 0 0 = = =
LTLD	1 1 1 0 1 * * *
INCR	1 1 1 1 0 * * *
CMPR	1 1 1 1 1 * * *

WHERE ,

```
00100
00200                   <* * *>       =>   DESTINATION,
00300                   <- - ->       =>   SOURCE,
00400                   <$ $ $ $>     =>   FUNCTION NUMBER,
00500                   <% % % % %>   =>   DEVICE NUMBER,
00600                   <& &>         =>   FUNCTION REGISTER,
00700                   <= = =>       =>   BRANCH CONDITIONS,
00800
00900           SOURCE OR DESTINATION REGISTER NUMBERS AS
01000           DESCRIBED EARLIER, SO ALSO FUNCTION REGISTERS,
01100           FUNCTION NUMBER AS IN <F(Q)>,
01200           CONDITIONS AS FOLLOWS :
01300
01400           000             SUBROUTINE RETURN
01500           001             SUBROUTINE CALL
01600           010             UNCONDITIONAL BRANCH
01700           011             BRANCH IF Z IS CLEAR (I.E. ON NONZERO)
01800           100             BRANCH ON POSITIVE
01900           101             BRANCH ON NEGATIVE
02000           110             BRANCH IF C IS SET
02100           111             BRANCH IF V IS SET
02200
02300
02400   **************************************************************
02500
```

```
00100
00200   SECTION-III
00300   -------
00400           EXAMPLE 1
00500
00600           SAMPLE PROGRAM THAT CALCULATES
00700           NUMBER  OF  ONES  IN  A  GIVEN
00800           MEMORY LOCATION,
00900           (NOTE ! THIS  PROGRAM  IS  NOT
01000           BY ANY MEANS THE BEST SOLUTION
01100           FOR THE PROBLEM , IT IS MERELY
01200           USED TO ILLUSTRATE THE KIND OF
01300           STATEMENTS  ONE  MAY WRITE FOR
01400           THIS MACHINE, )
01500
01600
01700           ORG 20;
01800           T←L;     ,0;
01900           W←T;     /W GETS ZERO/
02000           A←L;     ,S;
02100           Y←M;
02200           A←L;     ,S1;
02300   LOOP;   M←Y;
02400           R←L;     ,200;
02500           Y←(Y&R);
02600           R←W;     /R GETS ZERO/
02700           Y←Y-R;   /COMPARE WITH ZERO/
02800           NZ *;    ,L; /MULTIPLE STMTS/
02900                       /   ALLOWED    /
03000           *;       ,SKIP;
03100   L ;     T←T+1;
03200   SKIP;   Y←M;
03300           Y←(Y,C←0);
03400           Y←Y-R;
03500
03600           NZ *;    ,LOOP;
03700           RT;
03800           ORG 100;
03900   S ;     "10110110;
04000   S1 ;    ;
04100           END
04200
04300
04400   ********************************************************************
04500
```

```
00100
00200   PRINTOUT OF THE ASSEMBLER FOR THE EXAMPLE PROGRAM !
00300
00400   ***************************
00500   LINE  LC     CODE                    TEXT
00600   001,                                 ORG 20;
00700   002,  020  11101011                  T←L;     ,0;
00800   003,  021  00000000
00900   004,  022  00100011                  W←T;     /W GETS ZERO/
01000   005,  023  11101111                  A←L;     ,S;
01100   006,  024  01000000
01200   007,  025  00110000                  Y←M;
01300   008,  026  11101111                  A←L;     ,S1;
01400   009,  027  01000001
01500   010,  030  00000110      LOOP:       M←Y;
01600   011,  031  11101010                  R←L;     ,200;
01700   012,  032  10000000
01800   013,  033  01001110                  Y←(Y&R);
01900   014,  034  00010100                  R←W;     /R GETS ZERO/
02000   015,  035  11111110                  Y←Y-R;   /COMPARE WITH ZERO/
02100   016,  036  11100011                  NZ ↑;    ,L; /MULTIPLE STMTS/
02200   017,  037  00100010
02300   018,                                                 /   ALLOWED    /
02400   019,  040  11100010                  ↑;       ,SKIP;
02500   020,  041  00100011
02600   021,  042  11110011      L :         T←T+1;
02700   022,  043  00110000      SKIP:       Y←M;
02800   023,  044  01011110                  Y←(Y,C←0);
02900   024,  045  11111110                  Y←Y-R;
03000   025,
03100   026,  046  11100011                  NZ ↑;    ,LOOP;
03200   027,  047  00011000
03300   028,  050  11100000                  RT;
03400   029,                                 ORG 100;
03500   030,  100  10110110      S :         "10110110;
03600   031,  101  00001001      S1 :        ;
03700   032,                                 END
03800
03900
04000
04100   ********************************************************************
04200
04300
04400
04500           MORE SAMPLE PROGRAMS AND THEIR PRINTOUTS
04600           APPEAR IN THE FOLLOWING PAGES.
04700
04800
```

```
00100
00200
00300
00400
00500
00600              ORG 20;
00700              D1=12;
00800              D2=13;
00900              A=L;     ,100;
01000              X=M;
01100              X=(-X);
01200              X=X+1;
01300              M=X;
01400    LOOP:     W=D1;
01500              M=M+1;
01600              D2=W;
01700              NZ ↑; ,LOOP;
01800              RT;
01900              ORG 100;
02000              "00101011;
02100              END
02200
02300
02400    ****************
02500    LINE  LC      CODE                    TEXT
02600    001,                                  ORG 20;
02700    002,                                  D1=12;
02800    003,                                  D2=13;
02900    004,  020   11101111                  A=L;     ,100;
03000    005,  021   01000000
03100    006,  022   00101000                  X=M;
03200    007,  023   01001001                  X=(-X);
03300    008,  024   11110101                  X=X+1;
03400    009,  025   00000101                  M=X;
03500    010,  026   10011010      LOOP:       W=D1;
03600    011,  027   11110000                  M=M+1;
03700    012,  030   10001011                  D2=W;
03800    013,  031   11100011                  NZ ↑; ,LOOP;
03900    014,  032   00010110
04000    015,  033   11100000                  RT;
04100    016,                                  ORG 100;
04200    017,  100   00101011                  "00101011;
04300    018,                                  END
04400
04500
04600
04700
04800
```

```
00100
00200
00300
00400
00500
00600
00700           DTTY=10;
00800           DLPT=9;
00900           ORG 77;
01000           A←L; ,M;
01100           X←M;
01200           X←(-X);
01300           X←X+1;
01400           M←X;
01500   AROUND; W←DTTY;
01600           DLPT←W;
01700           M←M+1;
01800           NZ ↑; ,AROUND;
01900           RT;
02000           ORG 177;
02100   M ;     ;
02200           END
02300
02400
02500
02600   **WRONG OVC CODE,LINE NUMBER =  002,
02700   ********ILLEGAL REGISTER,SYNTAX ERROR,LINE NUMBER =  011,
02800   ******
02900   LINE  LC     CODE                TEXT
03000   001,                             DTTY=10;
03100   002,                             DLPT=9;
03200   003,                             ORG 77;
03300   004,  077  11101111              A←L; ,M;
03400   005,  100  01111111
03500   006,  101  00101000              X←M;
03600   007,  102  01001001              X←(-X);
03700   008,  103  11110101              X←X+1;
03800   009,  104  00000101              M←X;
03900   010,  105  10011000     AROUND;  W←DTTY;
04000   011,  106  ********              DLPT←W;
04100   012,  107  11110000              M←M+1;
04200   013,  110  11100011              NZ ↑; ,AROUND;
04300   014,  111  01000101
04400   015,  112  11100000              RT;
04500   016,                             ORG 177;
04600   017,  177  00001001     M ;      ;
04700   018,                             END
04800
04900
05000
05100           THE ERROR IN THIS PROGRAM IS NOT FATAL.
05200           THIS IS ILLUSTRATED ON THE NEXT PAGE.
05300
05400
```

```
00100
00200
00300
00400
00500
00600
00700              DTTY=10;
00800              DLPT=9;
00900              ORG 77;
01000              A←L; ,M;
01100              X←M;
01200              X←(-X);
01300              X←X+1;
01400              M←X;
01500              DLPT=11;
01600    AROUND:   W←DTTY;
01700              DLPT←W;
01800              M←M+1;
01900              NZ *; ,AROUND;
02000              RT;
02100              ORG 177;
02200    M :       ;
02300              END
02400
02500
02600
02700
02800    **WRONG DVC CODE,LINE NUMBER =  002,
02900    ***************
03000    LINE  LC      CODE                    TEXT
03100    001,                                  DTTY=10;
03200    002,                                  DLPT=9;
03300    003,                                  ORG 77;
03400    004,  077  11101111                   A←L; ,M;
03500    005,  100  01111111
03600    006,  101  00101000                   X←M;
03700    007,  102  01001001                   X←(-X);
03800    008,  103  11110101                   X←X+1;
03900    009,  104  00000101                   M←X;
04000    010,                                  DLPT=11;
04100    011,  105  10011000      AROUND:      W←DTTY;
04200    012,  106  10001001                   DLPT←W;
04300    013,  107  11110000                   M←M+1;
04400    014,  110  11100011                   NZ *; ,AROUND;
04500    015,  111  01000101
04600    016,  112  11100000                   RT;
04700    017,                                  ORG 177;
04800    018,  177  00001001      M :          ;
04900    019,                                  END
05000
05100
05200
05300
05400
05500
```

```
00100
00200
00300
00400
00500
00600
00700
00800
00900           DTTY=13;
01000           DLPT=15;
01100           A=L; ,M;
01200   M ;     ,20;
01300           RT;
01400           END
01500
01600
01700
01800   ***NO STARTING ADDRESS,
01900   PROBABLY MISSING ORG STMT,
02000
02100   LINE  LC     CODE                TEXT
02200   001,                             DTTY=13;
02300   002,                             DLPT=15;
02400   003,       00000000              A=L; ,M;
02500
02600
02700
02800
02900
03000
03100
03200
03300
```

```
00100
00200
00300
00400
00500           ORG 77;
00600           A←L;     ,L1;
00700           R←L;     ,200;
00800           X←M;
00900           X←(X&R);
01000           M←X;
01100           M←M+1;
01200           Y←M;
01300           Y←Y-R;
01400           N↑;      ,LOOP;
01500           RT;
01600           ORG 167;
01700           ;
01800           END
01900
02000
02100
02200   ************
02300   **UNDEFINED LABELS :
02400
02500           SYMBOL          LINE
02600           L1              003
02700           LOOP            013
02800
02900   LINE  LC     CODE               TEXT
03000   001.                            ORG 77;
03100   002.  077  11101111             A←L;     ,L1;
03200   003.  100  --------
03300   004.  101  11101010             R←L;     ,200;
03400   005.  102  10000000
03500   006.  103  00101000             X←M;
03600   007.  104  01001101             X←(X&R);
03700   008.  105  00000101             M←X;
03800   009.  106  11110000             M←M+1;
03900   010.  107  00110000             Y←M;
04000   011.  110  11111110             Y←Y-R;
04100   012.  111  11100101             N↑;      ,LOOP;
04200   013.  112  --------
04300   014.  113  11100000             RT;
04400   015.                            ORG 167;
04500   016.  167  00001001             ;
04600   017.                            END
04700
04800
04900
05000
```

digital INTEROFFICE MEMORANDUM

TO: Don White
Nick Mazzarese
Bill Long

DATE: March 27, 1972

FROM: Gordon Bell

cc: Larry Portner
Fred Gould
Win Hindle

DEPT:

SUBJECT: Attoprocessor Assembly Language

Having learned the hard way that it is difficult to bring a modern looking assembly language into DEC via the programming department, I asked one of my graduate students to design and write an assembler for the Attoprocessor. Since he has a fairly extensive programming background, it took about a month in his spare time. The program is written in Algol to run on the PDP-10. A manual for it is attached.

Thought for the second:

- to paraphrase -"The day you hire your first lawyer, is the day you have your first lawsuit."

"The day you hire your first programmer is the day you start a programming department to train programmer managers, to train programmer managers, to ....."

If Attoprocessor becomes a product, the project may need some programming. I would hope that the person who does this is fundomentally an engineer who doesn't mind writing assemblers, applications programs, diagnostics, etc. This approach seems to work in regard to the PDP-16; the engineers are equally comfortable with both circuits and programs.

bwf

Attachment

G. Bell

dec INTEROFFICE MEMORANDUM

DATE January 28, 1963

SUBJECT PDP-3

TO Ken Olsen

FROM Gordon Bell

cc: N. Anderson
D. Mann
N. Mazzarese

Beginning now, A. Kotok should be assigned full time to PDP-3.

The character of a machine influences our growth tremendously since day to day development decisions are always made around existing machines (eg. BBN system).

PDP-3 might be useful if it is: (I'm sure it could be placed in the same space as PDP-1)

1. Built to sell for under $200,000
2. 5 μsec cycle
3. Expandable (similar to BBN system)
4. Capable of running 704, 7040, 7044, 709, 7090, 7094 programs.
5. Built as if we intend to stay with it a while.
6. Entirely serial logic in the processor.
7. Complete systems approach:
   a) allow many memories
   b) allow many processors of various types.
   c) First processor might be very simple with complete trapping facilities to handle most every instruction, and provide only a very skeleton processor.
   d) Provide an encore (made with a faster parallel version).
8. Use new logic (If we have an extra 9 months for the project.)

INTEROFFICE MEMORANDUM

DATE February 21, 1963

SUBJECT New Computer Design Philosophy

TO Tom Stockebrand FROM Kenneth H. Olsen

A new computer is long overdue at DEC but we have not been in a position to build one because we have been so long in winding up the details from our present computers. However, now we do have the techniques and the time and the money for a new computer, I think we should go ahead and make one in a reasonably fast time schedule.

The proposal is to do all aspects of the computer design in parallel. This means that at the end of the time schedule whether it is four or six months, the job should be done. Then after a rest of a month or two we could if we wanted to go off and make another computer. Here is a list of the items which should be carried on in parallel:

Design and Build Central Processor
Write FORTRAN with Assembler and Simulator
Design and Build Tape Control Unit
Write All Manuals

We have never looked at competition before but I think as a result we have lost out because we don't know the points in which our machines are significantly better than others. I think that we should consider doing this parallel effort sub-contracting a survey out to someone like I.I.I. to compare our machine in detail with others.

Kenneth H. Olsen

INTEROFFICE MEMORANDUM

DATE February 21, 1963

SUBJECT Random Notes on New Computer

TO Tom Stockebrand

FROM Kenneth H. Olsen

We received a quote from Amphenol on a 36 pin connector for use in large system plug-in units but this will not work out well because it has to be thicker and therefore will not fit in our standard construction. Loren Prentice is now making a model of a double width plug-in unit which will have two 22 pin connectors on it which will make a total of 44. This looks like a reasonable approach to a large plug-in unit.

Gordon Bell suggests that we do all our register transfers through one common register. This is the way the MTC Computer worked originally. This would cut down the number of gates and they might end up using the very high speed transistor gates.

I asked Bob Savell to consider repackaging the reader, punch and typewriter control panels to make them less expensive. We might put much of it on a very small number of large plug-in units. We might also include the micro-tape logic in the same place.

I told Bob Savell to start working on the new punch timing control for PDP-1 but to plan to have it in the new computer.

Dit Morse feels that the teletype typewriter is a satisfactory typewriter for computer use. He of course would like a more extensive character set but a typewriter that works has a very definite advantage. I can't see that we'll have time to evaluate any other typewriter in time.

Loren Prentice has been working on a new design for the PDP-1 and PDP-4 console fronts. I suggested that they drop all work on that and work on the console front for the new computer. This one should include space for punch, reader, LINC and control panel.

Some people like the idea of having an extra register to store the contents of the accumulator when it is not being used. This would allow the accumulator to be used for index adding and other things. The extra register could then be used as a carry register which would allow very fast multiply. If this carry register is used as an accumulator buffer, the accumulator might then be used as the register which transfers information between registers. Several people have told me they would like to have a pointer register.

We have to decide whether we want indicators on all flip-flops or not. I have asked Jack Smith to estimate what it would cost to add an indicator.

It is a real chore to change cabinet design. Our present mounting panels hold 25 plug-in units and if we move the marginal checking panel, it will hold 26. It would therefore be convenient to keep the digit length of the machine 26 or less bits long.

file — PDP-3

dec INTEROFFICE MEMORANDUM

DATE February 22, 1963

SUBJECT New Computer Design

TO Ken Olsen

FROM Tom Stockebrand

My apologies for form and content of this memo, it is a rushed job. In particular it does not include enough evaluation of the competition nor enough filtering of the ideas presented. While I am on vacation, I will try to sketch out more of the machine design.

Commitments on delivery dates, price and so on should be to Ken Olsen and the company and not to customers.

This machine should be specifically designed to do the job as listed below superlatively well rather than to in any way "look like the competition" or be an answer for them.

This machine is to fill a vacuum we believe to exist at the present time in the computer market.

We must make no compromises in carrying out the ideas which are involved in its design. The implication of the above is that, as is usual with DEC effort, the ideas shall be limited to those which are eminently easy to do, general, straightforward extensions of the art..... In fact, "today's technology today." ------God.

The sources of the ideas presented in this note are indicated in an effort to provide "source data" while I'm gone. If the general ideas are agreed upon, future administration of the project will be vastly improved.

If we are to turn out machines regularly, we need some more official advanced development - that is answers to specific how-can-we-do-this-job questions. (Coax delays, micro-logic, serial, majority logic circuits, etc.)

THE IMPORTANT NOTIONS

It is time the Programmer was given real power in sub-routine writing ability so that no modifications of instructions are ordinarily necessary during program relocation.

Multi-programming, time sharing, fast break-in or what-you-will is necessary in the eyes of most users of our equipment and in fact necessary (though they don't know it) to many users who are comtemplating using our equipment.

Data words need to match today's data requirements in accuracy. The analog people are almost entirely concerned with 14 bit accuracy for what they call four significant digit precision.

Large memories are here. Index registers are here.

Some fair expansion of the machine should be planned for at the beginning though we understand that wholesale revisions of the machine are out of order.

The rest of this memo is a list of specifics pertaining to the generalities listed above.

Routine Relocation Power - The ability to operate routines wherever they may be located in memory after a dump from, say, the drum can be provided by the ability to (1) modify each memory reference by a constant while (2) checking that result against specified bounds and trapping to a particular memory location or executive program if the required location is outside of the bounded area. This feature can be achieved reasonably easily during the initial design of a machine by allowing the index adder, or its equivalent, to do the work. Dit says this feature would make programming "ten to a thousand times easier." Ed says that if you can use the arithmetic element more and memory less, you're way ahead and this feature would leap in that direction. (Dit, Shelley, Kotok, Ed and Ben.) This feature is considered by advanced type people to be crucial to the machine design.

Trapping - Trapping meaning to execute and instruction located at, for instance, the address indicated on the op code. This trapping would be done on non-used instructions or memory addresses outside of the bounds set by the executive routine in the relocation of power indicated above (Dit, Ben.)

Character Handling Power - The ability, in one form or another, to address characters stored in memory hopefully to deal with character strings in I/O transfers such as is done in the Lisp and Comet Programs. Dit, Ben and Ed are in favor of this, Ivan goes even further and says that bit addressing features are of great power. However, Len disagrees.

On Obsolescence - Trapping also allows optional expansion by do-it-now-with-program, later with wires. Also de-bugging and checking power is automatically incorporated. The machine should be built of modular parts of course like different memories and AE's and an extra bit or two should be assigned in the instruction word for future variations not thought of now when you absolutely have to have that bit!

Multi-Processing - Multi-Programming - First and foremost, a fast break - this means primarily no need for many accesses of a clean-up variety to store away stuff in preparation for operations in response to a break request. The most potent feature here seems to be an extra register in the AE to allow either exchanges with the AE for saving purposes, or as an address calculator (Dit) or as a multiply index by, or as an addend register, or as a carry register depending on your exact orientation. The second thing which would help this process out is probably a separate index adder though I believe a machine try should be made to use one adder for everything. Since it is reasonably certain that two groups of wide modules will be used, however, it is probably not unreasonable to suggest the index adder. In the future, that means perhaps with the development of another machine, separate program counters may be in order. For now, core program counters should certainly be enough if they are necessary. To hell with data gather. The idea here is to eliminate control problems from the channel and put them in the program where they belong.

Channels should be only high-speed data gathering devices. (Dit) System capability is an okay phrase. (Dit)

List Processing - This is a program technique which has general power which goes well together with our ideas of a processor with general power. It requires index registers and increment and decrement by more than one and, ideally, registers which can be packed with several addresses each (that is, word length equal to two times the address length.) However, I think a clever use of the relocation feature or of Dit's multiple indexing (1+ 2+ 4 scheme) will allow the shorter pack base address that this too short word machine will have. (Len) In general, this processing seems to be for the next machine though a small look into the future is probably in order. Similarly, floating point AE's will probably have to wait until the next machine or at the very best, be planned as a different kind of AE attachable to this memory.

Index Registers - These are clearly necessary. Dit feels that three register which could be added together in a micro-program fashion that is, any combination of the three according to MACRO programmed bits in the word, would be of more use than seven registers addressed directly by the same three bits though Kotok disagrees. I have no feelings. Whether the three could be added together and in fact the complete design of the index adder might depend crucially on the ability to build a simple circuit which would detect four out of seven to provide carry for carries. If this circuit were easily available I believe that five registers could be added together simultaneously and stored in a fifth and the sketch accompanying this memo shows the powerful use that could be made of this feature.

Addressable Registers - These would be very useful according to Len for much easy processing without complicated instruction and could perhaps be implemented to do the character addressing without using extra bits in the word by allowing certain kinds of character type transfers between registers. The most important addressable registers would perhaps be the in/out registers such as, for example, the scope buffer for use with the light pen -- especially if it were an incremental scope plus generator type. In this case too, the feature would allow sine, cosine and hyperbolic and parabolic function generation with no extra hardware. It would save on the IOT read-in bits but cost some address decoding.

Data Channel - Fast break SI, Data Channel SI, I/O Channel, no, - do it with program. (Dit)

Cute Instructions - Ben feels that load and deposit AC in push down list would be a useful instruction at least to the prospects of a clever turn of mind if not to real users. Instruction (Y+)AC)) ---- AC is reasonably necessary for multi-dimentional matrices when indexing is not readily available and would implement easier list processing. Ben likes an instruction called execute effective address however, Len doesn't go along with him. Dit makes the comment that we should avoid doing things in little pieces.

Word Length - There are two criterion for word length, one is the data word that will usually be of necessity, and the other one is the number of bits that you need in your instruction. For floating point work, 48 bits seems to be a minimum and for graceful manipulation of the text

this also seems like an appropriate word length. I do not believe that it is necessary to have precisely a multiple of six though this may be, in some cases, graceful for character processing. Many people would just love to have an extra bit or two to indicate whether this set of characters is to be considered in the list and for other marking purposes, ask Dit for example. I, myself, have run into this problem many times when programming character strings. Len will also agree I think. As far as the packaging limitations go, I agree that it is essential to keep the packaging the same which means no more than 25 units in a rack panel wide; notice that if the address portion is 16 or 17 bits, even, there are 8 bits left over in the mounting panel supporting the "short-word" AE in which to provide extensions of the full register portion of the AE. Since the floating point people need 48 bits and we can't possibly take this much of a jump in the present machinery, we should either leave them out of consideration or consider two-word data accesses floating point words. To this end, Dit suggests a single bit in the data words to tell whether the word is to be interpreted as floating point or not. This might be an example of the use of a spare bit location in the word for use when a floating point processor might become available. How about word lengths for ordinary users of fixed point type calculations? The competition seems to feel that 24 bits is a reasonable length however, I submit that in many practical cases 14 or so bits is a reasonable length based on my discussions with various analog and hybrid types. This is because 14 bits represents four decimal digits which is the current okay number in that industry, though there as here okay numbers do not necessarily represent the best in engineering philosophy or power. Analog people further state that they need higher data rates than we can get and if we are to capitalize on our parallel computing and data handling power in order to try to overcome some of the taint of the current serial flap, we should consider, I think, 28 bits minimum so as to be able to pack two 14 bit words per register and thus, double our data output rate to digital to analog converters and the like - also to scopes.

Now on to word length as determined by the instructions. Certainly 16 bits represents a reasonable address length to address 65 kilowords of memory. Everyone agrees that this would be a desirable number. 3 bits for index register seems about right and one bit for deferring. 6 bits seems like a minimum for op code, 1 bit for a programmed operator - primarily to catch up to the competition of SDS. I insist on one spare bit and many people who feel character addressing is important would want to use my spare bit plus two others to do the character addressing in those instructions where it matters, and leave it for instruction modifications where it does not matter. This would give a total of 28 or 30 bits depending how you look at it. If you really believe that there should be a multiple of six, then I would recommend a 30 bit machine. However, 28 bits I think is my current recommendation. Incidentally, if you allow 7 bit characters for 128 character set, which is quite a reasonable number, and a "step forward",then this even meets the criterion that 2 bits of character addressing is enough and comes out even. In any case we have room for 33 bits and 17 address bits in the two mounting panels which have double trays so this gives us three extra slots for odds and ends.
I STRONGLY RECOMMEND A 28 OR A 30 BIT WORD.

Concurrent Programming - In this area I am not an expert but Dit seems to feel that the FORTRAN four language, which looks like the ALGOL language is the language to use for all programming. I am not aware of the details of the character set required or like that.

He wants to do it all in ALGOL. I would have a good discussion with Dit on the subject. All agree that a full-time programmer should be working from the start of the project.

More Work - Very soon, more work should be done in the following areas before the design is completely hard.

1. A careful compilation and discussion of the competition's ideas and features, also of LINC and other semi-competitive machines.

2. Whether an analog input is a necessity - I believe it may be.

3. Whether serial methods of computation would give us any real advantage. It may be that in the shorter worded index adder, the multiple additions that will sometimes go on could be done very efficiently this way in the event that a majority logic circuit did not work out as a good idea. This would allow many additions in only the time to circulate one word plus N extra bit times. Furthermore, I am not sure of the best AE design. I am convinced that we should have one programmer (hopefully Lennie) working full time along with the design of this machine so that it is on cards or back panel wiring or like that right from the start. This, I think, will eliminate in the future bottle necks which we are certainly going to run into if we plan to turn out new type machines regularly.

Conclusions -

Relocation
Independence of AE and Memories
Trapping
Time Sharing or Multi-Processing or Addressable Register or Multi-Programming
Character Handling Power

I think a tentative example of the breakdown of parallel tasks in the developments of this machine would be somewhat as follows:

1. Programming with a good man such as Dit

2. Manual Design and Development along with the development of the machine with Stu Grover

3. AE design under Dit and Gordon

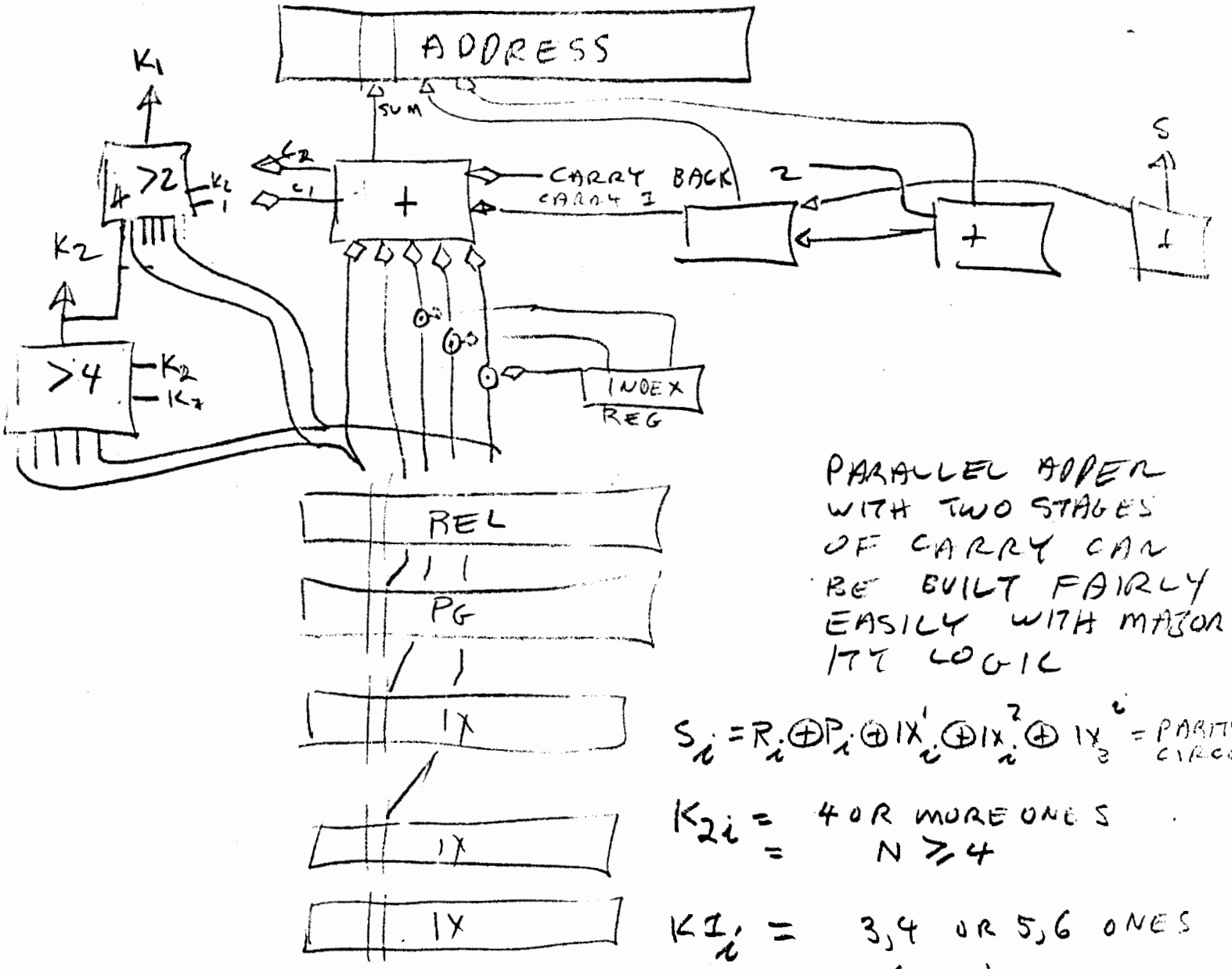
4. Machine design under Gordon and I

5. Programming toward aiding the design of the machine under Len

6. A small amount of research under Emile ar Russ Doane in the form of coaxial serial parallel conversion and multi-plexing and majority logic circuitry.

7. I/O development under Roland Boisvert or perhaps even better Mel Arsenault.

PG PARALLEL



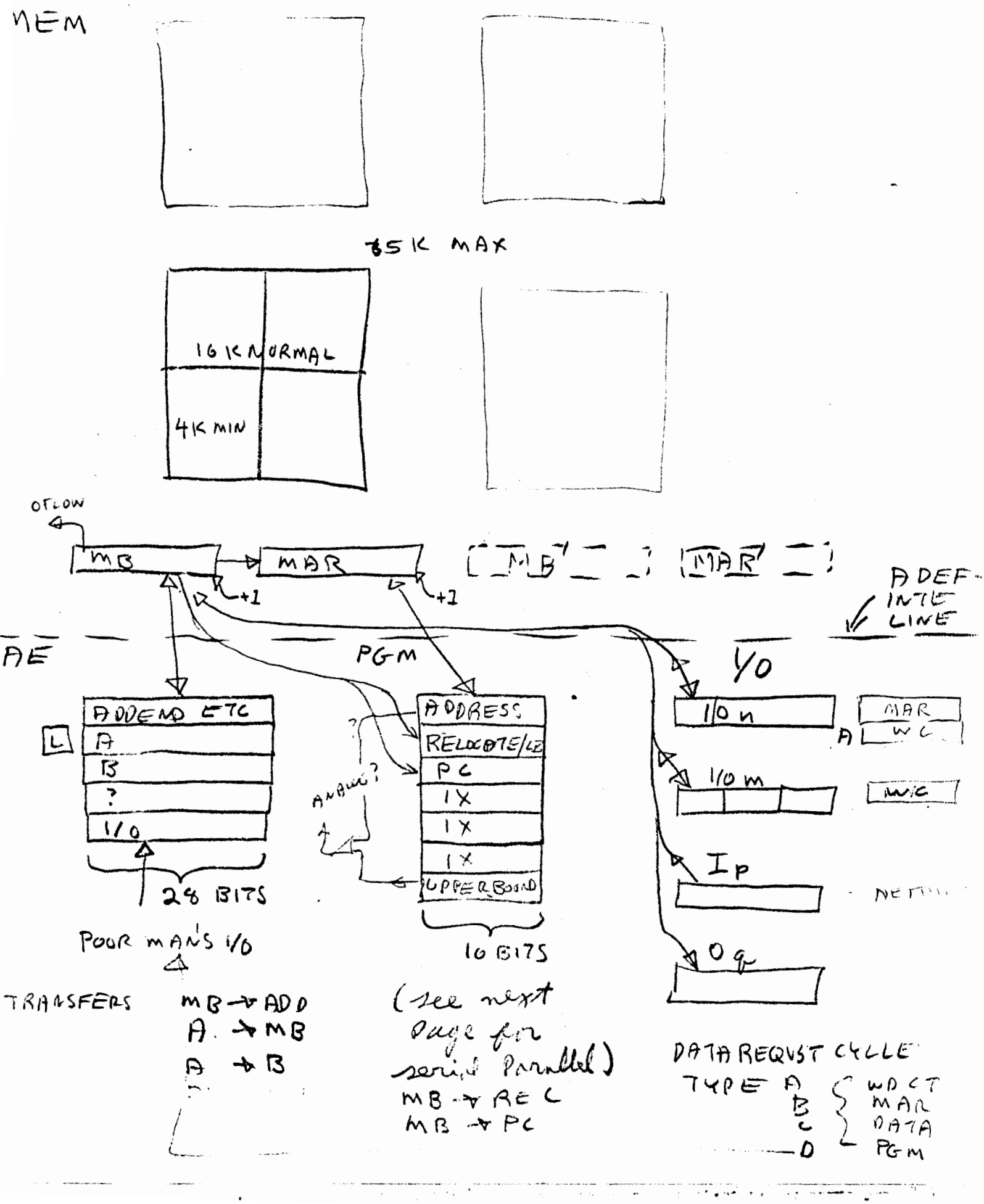
PARALLEL ADDER WITH TWO STAGES OF CARRY CAN BE BUILT FAIRLY EASILY WITH MAJOR ITT LOGIC

$S_i = R_i \oplus P_i \oplus 1X'_i \oplus 1X^2_i \oplus 1X^i_3$ = PARITY CIRCUIT

K_{2i} = 4 OR MORE ONES
= $N \geq 4$

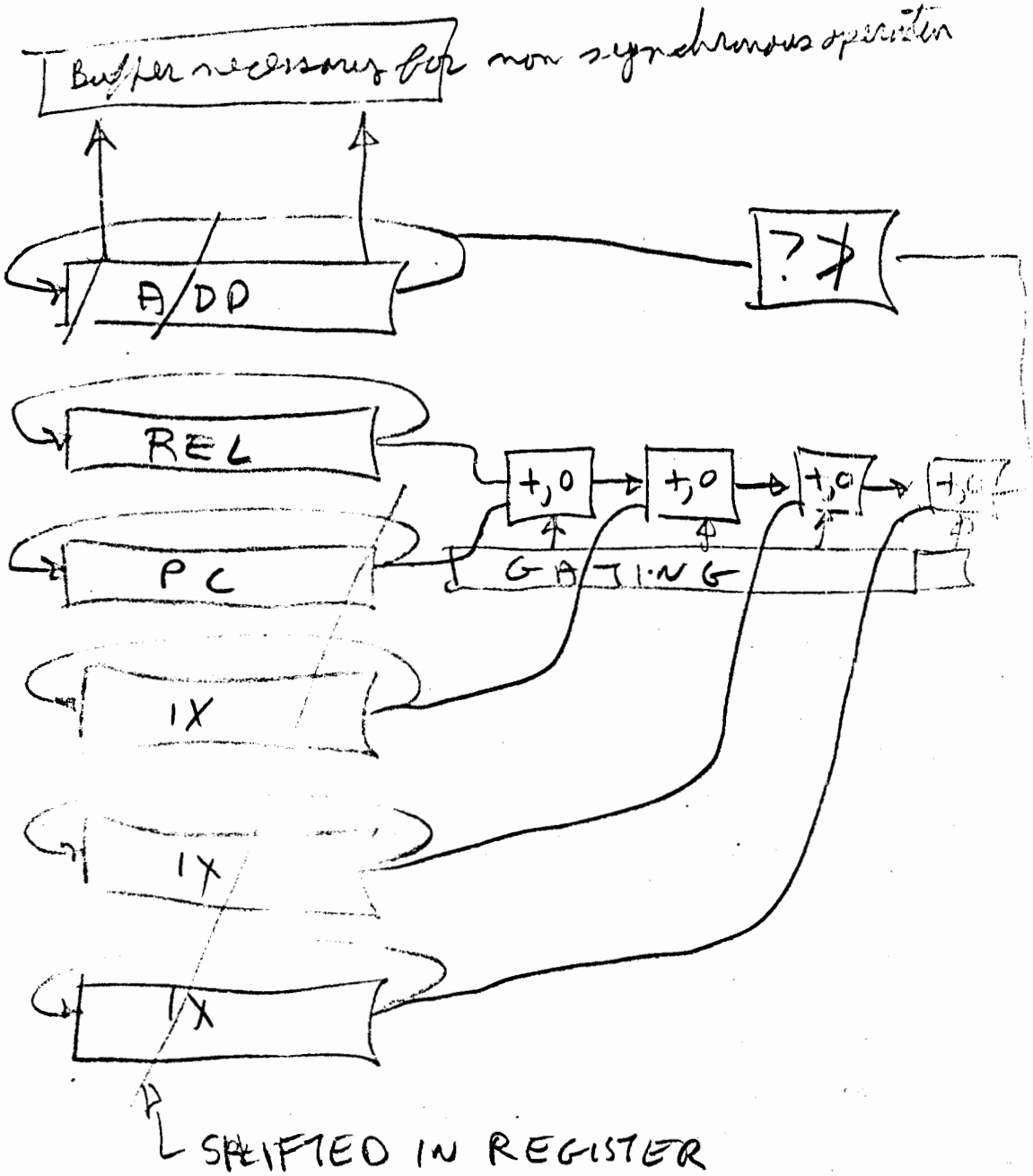
$K1_i$ = 3,4 OR 5,6 ONES
= $-\left(\frac{K_{2i}}{2}\right) + N \geq 3$

FLOW


MEM
65K MAX
16K NORMAL
4K MIN
OFLOW
MB
MAR
+1
+1
MB
MAR
A DEF
INTE
LINE
AE
PGM
I/O
ADDEND ETC
L
A
B
?
I/O
28 BITS
POOR MAN'S I/O
ADDRESS
RELOCATE/LE
PC
1X
1X
1X
UPPER BOUND
16 BITS
I/O n
MAR
WC
I/O m
WC
IP
OQ
TRANSFERS
MB → ADD
A → MB
A → B
(see next page for serial Parallel)
MB → REL C
MB → PC
DATA REQUST CYCLE
TYPE A WD CT
B MAR
C DATA
D PGM

MAXS NEXT MACHINE
DES = DIFFERENTIA EQN SOLVER

SERIAL



INTEROFFICE MEMORANDUM

DATE October 14, 1965

SUBJECT PRELIMINARY THOUGHTS ON A NEW COMPUTER LINE

TO N Mazzarese FROM E De Castro

I believe that we should start fairly soon to develop both hardware and software for a completely new line of small computers. Our current machines, because of their limited organization, have made it impossible for us to add features which cost very little and yet are standard equipment on most competitive machines. The following are some of the most predominant deficiencies in our line:

1. We are unable to offer our customers the ability to replace a small machine with a larger one as his requirements grow without asking him to undertake a complete reprogramming job.

2. We do not have a full line and therefore are precluded from a fair segment of the market.

3. We have yet to build a computer small enough and inexpensive enough to fully satisfy the OEM, educational and small laboratory markets.

4. We do not have compatible interfaces and therefore must develop and maintain different peripherals for each computer.

5. We do not have program compatibility and as new programming concepts evolve or new applications areas become interesting we must either duplicate our efforts or forego the competitive advantage on one machine or the other.

Completely replacing a computer line is certainly a large undertaking but we now have several advantages which we have not enjoyed during the recent past. These are as follows:

1. A large order backlog for standard products which can be produced with a minimum of engineering assistance.

2. A competitive line which with only minor modifications can probably be sold successfully for another year.

3. An adequate programming system which, although not fully competitive is complete enough so as not to detract seriously from sales in the short run.

4. Sufficient personnel in the small computer group capable in circuit design, system design and programming.

If we are going to avoid serious fluctuations in our production rate and still allow development to be done in a thorough and orderly manner we must start now to plan the products which will take over as PDP-7 and 8 phase out.

DESIGN OBJECTIVES

For a new computer line to be successful in the market it must meet several objectives some of which are in conflict and therefore compromises must be made. We must have a low cost basic configuration yet it must not be so inept that peripherals are prohibitively expensive or extremely unwieldy to attach. We must have machines that closely approach the accepted standards yet not so complex in organization that we are unable to sell at a price slightly below that of competition for a computer of equal memory speed and word length. We must do everything possible to get the most mileage out of our engineering and programming effort. To further this objective central processors must all have an identical interface so that one line of peripherals may be designed to connect to any processor. C.P. organization should be such that software may be transferred without change from one machine to another. In achieving this degree of compatibility we must not make it impossible for efficient programs to be written for each machine in the series although this does not mean that the most efficient program for one machine is necessarily optimum for another.

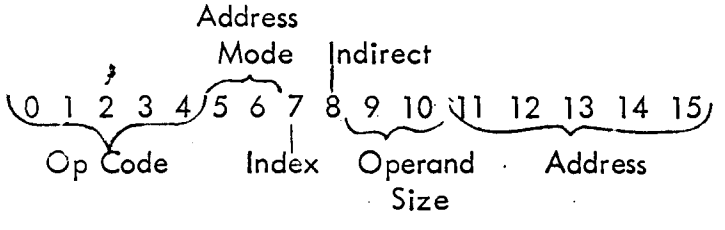
GENERAL CHARACTERISTICS

The line should consist of three computers having word lengths of 8, 16 and 32 bits respectively. Each machine will have a parallel memory and be capable of performing arithmetic and logical functions in parallel on operands equal to or smaller than the basic word length. In addition the two smaller machines will be able to perform 16 and 32 bit operations by processing operands in serial. For example, if the small machine were programmed to add two 32 bit numbers it would make 4 calls on memory to obtain operands and would add each 8 bit segment individually to the appropriate section of the accumulator using the same adding circuitry for each step. The 16 bit machine would require only two such steps. To achieve compatibility in the other direction the larger machines will be capable of dealing with words consisting of 1, 2 or 4 - 8 bit bytes. Thus the op code which causes the small machine to add a single word will be interpreted by the large machine as a command to add a single byte.

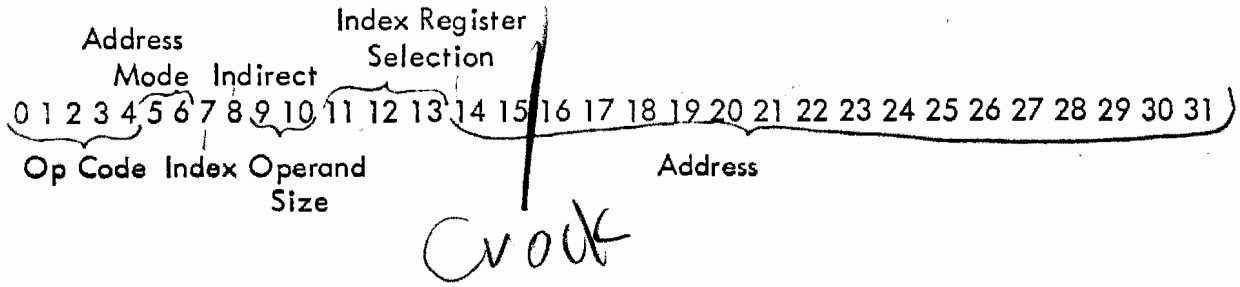
It is desirable to make the 32 bit machine capable of performing some instruction which will not be included in the repertoire of the smaller ones. To maintain compatibility all unused op codes will trap, i.e., cause the program to branch to a fixed location where a subroutine to simulate the non-existant instruction may be located. Some additional storage is thus required in the smaller machines to simulate these instructions.

INSTRUCTION FORMAT

All instructions are either 16 or 32 bits in length and are fetched from memory in 1, 2 or 4 cycles as required. The small machine must make at least 2 references to memory for each instruction while the large machine may have 2 instructions in a single word. The 16 bit memory reference instruction word format is as follows:



The 32 bit word format is:



"The OP Code portion" is used in the traditional sense and merely selects the instruction to be performed.

"The Address Mode" is decoded as follows:

0 = Immediate i.e. operand is contained in the next 2 bytes immediately following the instruction or in the same word on the 32 bit machine.

1 = Relative forward. Add the contents of the address portion to the current P.C. to obtain the address of the operand.

2 = Relative reverse. Subtract the contents of the address portion from the current P.C. to obtain the address of the operand.

3 = Full address. Fetch the next two bytes to obtain the address of the operand.

Modes 0, 1 and 2 specify 16 bit instructions whereas mode 3 specifies a 32 bit instruction.

"The Index bit" if a one indicates that the contents of the index register will be added to the address after any relative address calculation has been made.

"The Indirect bit" specifies deferred addressing in the usual sense. Multi level indirect addressing is possible. During a defer cycle the address mode, index and indirect bits of each word are obeyed.

"The Operand Size portion" indicates that the operand will be 8, 16 or 32 bits long.

"The Index Register selection bits" allow any one of 8 index registers to be specified in the full address mode. In any other address mode only index register 0 may be used.

"The Address portion" is used to select the first of the 1, 2 or 4 bytes which will be used as the operand. Thus in the 8 bit machine the address portion is equivalent to the memory address. In the 32 bit machine the least significant 2 bits are not used to address memory but rather are used as a byte pointer to select the desired portion of the word.

INSTRUCTION REPERTOIRE

The instruction set is designed to be complete but straightforward. Many of the instructions can be implemented at very small cost over and above the most basic useful set because they use existing gating and transfer paths. The following list represents a starting point and probably can be improved upon. Instructions are grouped by major function.

1. Memory Reference

   Arithmetic

   - Add to accumulator (#)
   - Add to memory
   - Subtract from accumulator
   - Multiply (optional)
   - Divide (optional)

   Logical

   - AND
   - Inclusive OR
   - Exclusive OR

   Store and Load

   - Load Accumulator
   - Store Accumulator
   - Store Zero in memory
   - Load MQ (optional)
   - Store MQ (optional)

   Index

   - Increment Memory and skip if 0
   - Decrement Memory and skip if 0

   Compare

   - Skip if same
   - Skip if different

Branching

Jump conditional #1

Jump conditional #2

Jump to subroutine

Jump and save P C in index register

In-Out

Transmit memory on IO bus

Transmit IO bus to memory

Test and jump

Miscellaneous

Execute

2. Augmented instructions

Shifts and Rotates

Logical Shift right (1 or 8 places)

Logical Shift left (1 or 8 places)

Arithmetic Shift right (1 or 8 places)

Rotate left (1 or 8 places)

Rotate right (1 or 8 places)

Long Shift right (optional)

Long Shift left (optional)

Normalize (optional)

Clears and Complements

Clear accumulator

Complement accumulator

Clear overflow

Complement overflow

Coun ting

Increment accumulator

Decrement accumulator

Miscellaneous

Halt

Read switches into accumulator

In-Out

Select device

Transmit AC on IO bus

Transmit IO bus to AC

Most of the instructions listed above are quite conventional. However the jump instructions require further explanation. Since the operand size portion has no meaning for these instructions it will be used to specify the condition for jumping. Conditions are decoded as follows:

Jump #1

0 = unconditional

1 = if AC = 0

2 = if AC $\neq$ 0

3 = if overflow = 1

Jump #2

0 = if AC is positive

1 = if AC is negative

2 = if overflow = 0

4 = not used

Test and Jump

0 = if device flag 0 is a 1

1 = if device flag 1 is a 1

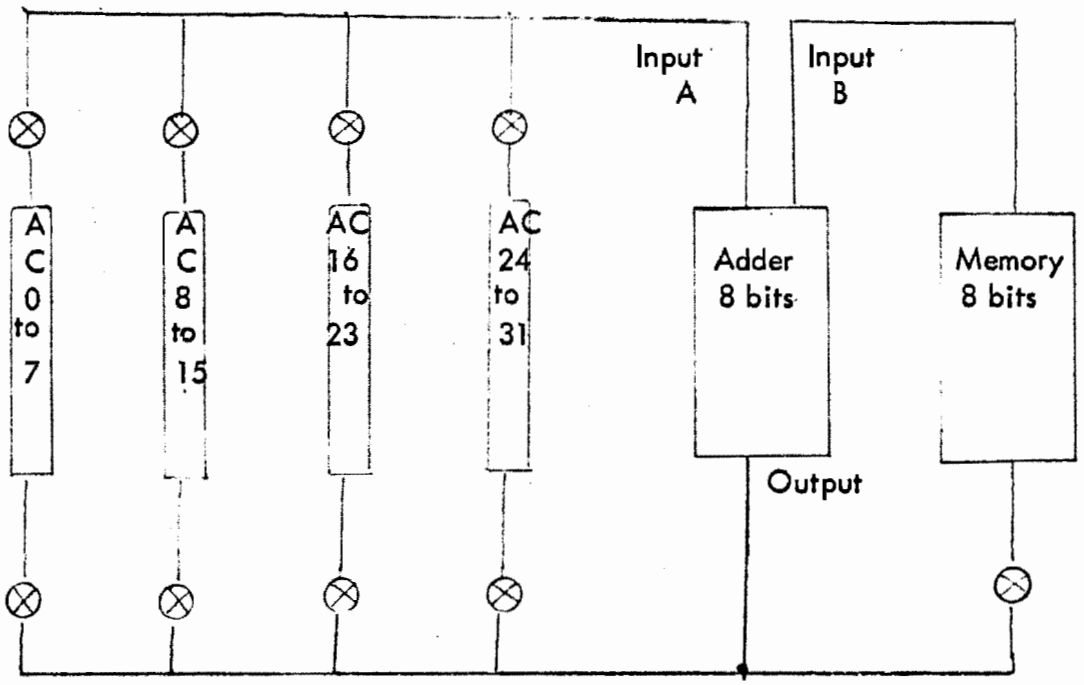
2 = if device flag 2 is a 1

3 = if device flag 3 is a 1

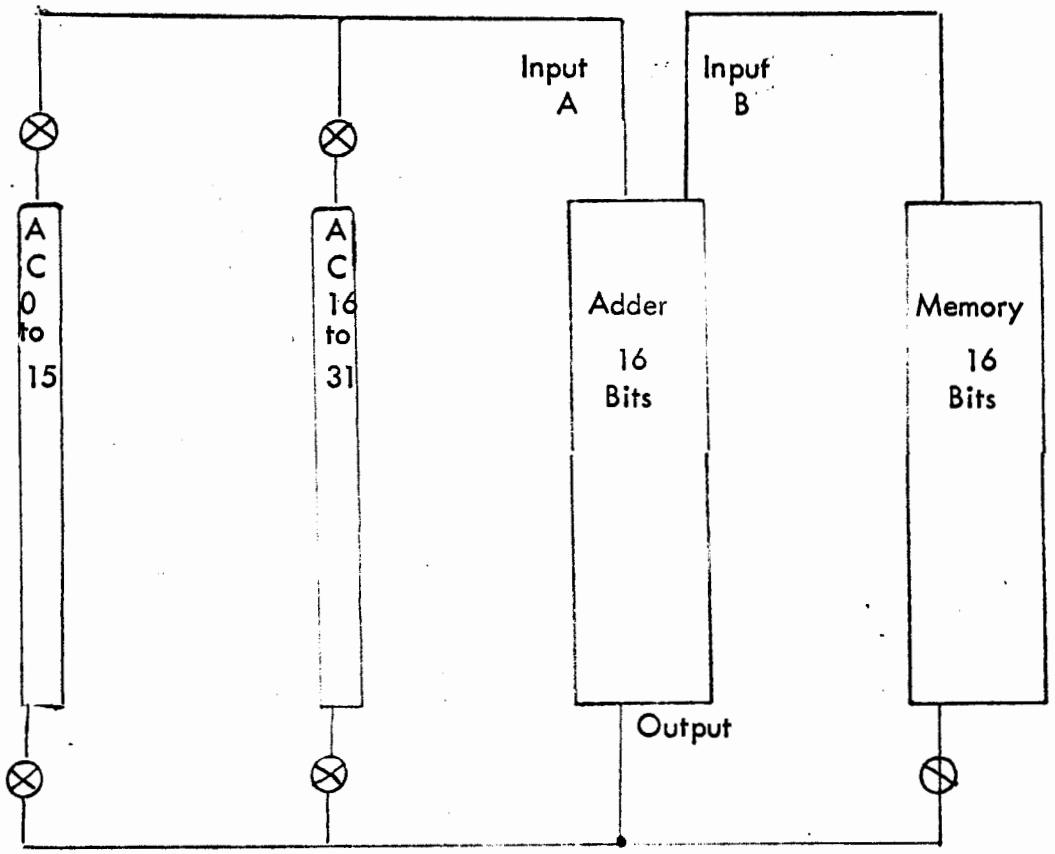
DATA HANDLING

Internal data is normally handled by moving it from memory to the accumulator where it is processed and then returned to memory. In all machines the accumulator is a full 32 bit register. However its organization and transfer paths differ. The block diagrams below illustrate the organization of each member of the family.

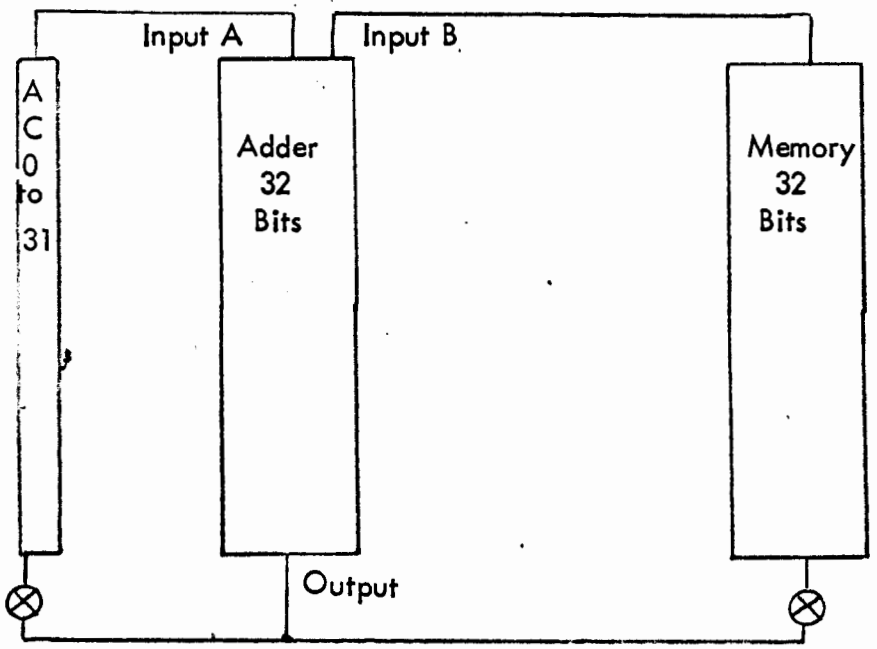
8 Bit Organization



16 Bit Organization



32 Bit Organization



It can be seen that in order to process a 32 bit number with an 8 bit machine, 4 passes must be made through the adder in serial. This of course takes 4 times as long but also substantially reduces the cost since all of the complex operations are done in the adder. The accumulator flip flops themselves are really quite simple and inexpensive. Carries out of any of the lower order portions of the accumulator will propagate into the next higher order part. Carries from the most signifi cant bit will set the overflow flip flop.

INDEX REGISTERS

Eight index registers are provided and are normally located in core memory. They may however be replaced by flip flop registers as an option. Each index register is 16 bits long including a sign bit. During an index cycle the sign bit will be obeyed, i.e., if it is negative the index register will be subtracted from the address. If it is positive it will be added. In addition if subtraction is specified and the index register is equal to 0 the next instruction will be skipped.

INPUT OUTPUT

All IO operations will be done on a bus system. Data transmission is normally accomplished as a 2 step operation. The first step is to load the selection register and the second is to transmit the data. The selection register is 8 bits long and its contents are transmitted to each device. Whenever a device recognizes its own code on the selection lines it will make a DC connection to the bus. Actual data transfers may be made with the accumulator using an augmented instruction or with memory using a memory reference instruction. If the transfer is with memory the instruction may be indexed and thus blocks of data may be conveniently transmitted or received. Either 1, 2 or 4 bytes will be transferred depending on the operand size portion of the instruction.

Device status may be tested by use of the test and jump instruction. This instruction will sample any one of 4 status lines on the IO bus. Since the selected device will have previously connected its status information to the bus the program may be branched in accordance with any of 4 different conditions from any of 256 devices.

ADVANTAGES

An organization along these lines gives us many advantages in return for a small amount of added complexity to maintain compatibility. The most important of these are as follows:

1. A 32 bit arithmetic capability. This will drastically reduce the amount of double and triple precision computations required and thus speed processing and reduce storage requirements.
2. A fairly powerful order code structure which will allow us to write programs to operate in smaller memories.
3. A more efficient method of handling data which allows easy character packing and does not require use of more memory than necessary for data of a given length.
4. A full line with the possibilityof replacing a small machine with a larger one as requirements change.
5. A fully compatible line of peripherals which may be transferred from one machine to the next if the processor is replaced. This will also reduce the engineering cost of peripheral equipment.
6. A fully compatible programming system. This will allow us to invest all of our programming effort in a single language and thus we will be able to develop better software at lower cost.
7. Reduced module costs since all machines will use the same circuits and thus volume will be much higher.

EDEC:ASJ

CC
K H Olsen, J Jones, R L Best,
G Bell, L Hantman

G. Bell

dec INTEROFFICE MEMORANDUM

DATE December 7, 1966

SUBJECT Proposal for the PDP-14X$_{GB}$ - Logical Structure of the 16 bit Processor.

TO K. Olsen, N. Mazzarese, W. Hindle, S. Olsen, S. Dinman, A. Kotok, L. Seligman, E. DeCastro, M. Ford, H. Burkhardt, J. Jones, L. Portner, T. Johnson, R. Lane

FROM Gordon Bell

Having attended a rather hectic, but stimulating meeting, at DEC on November 23, 1966, I decided to write down thoughts about the machine(s), generally. Those are included in the memo "New Machines Design Parameters". That memo deals with parameterizing the design, with attempts to list the goals. Having gone that far, I couldn't resist trying to specify a machine, and that's included.

The most important decisions in the machine(s), I believe, are:

1. Index Registers
1.a Are Index Registers, AC, MQ identical, general?
1.b Number of general registers?
2. Addressing Storage, how many modes? The desirable abilities are:

   a. Using a 32 bit instruction, directly address any work in memory, in connection with at least one index register. The instruction should be contiguous, so the assembler doesn't have to worry about building the 2nd half of it (with the address part) somewhere else nearby.

   b. Be able to transfer to a nearby address using a 16 bit instruction (nearby = -16±64 words).

   c. Pick up common 16 or 32 bit constants or data nearby for a common routine in a 16 bit instruction.

   d. Get at least a constant or immediate data of 2^5 for directly specifying shifts, selecting an I/O device, etc. in a 16 bit instruction.

e. Directly or indirectly address any of the general registers in a 16 bit instruction.

f. Address such that temporary data is stored in an "impure part" so that subroutines are all re-entrant.

g. Provide "immediate" data in a 32 bit instruction to avoid having assembler page difficulties.

3. Calling subroutines - can the subroutines be naturally re-entrant? Need they?

4. Extra codes/SYSPOP/UUOS/or Programmed Operators - Can these be implemented so that desirable order codes be implemented with little overhead in time, and interpretive programming provided for?

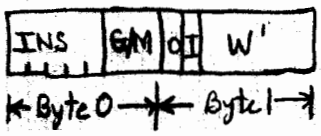
5. Address space - Is 2^{15} or 2^{16} large enough for foreseeable market?

6. Multiple users? Protection and Relocation Scheme.

7. Should page or relative addressing be used for short addresses?

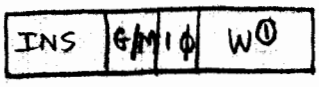
BASIC

INSTRUCTION LAYOUT PDP-14X$_{GB}$



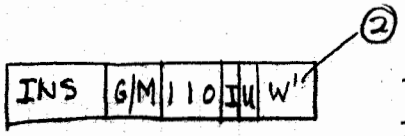
DIRECT OR INDIRECT USING THIS PAGE

I { DATA ← Memory (This Page + W)
  { DATA ← Memory (Memory (this page + W))



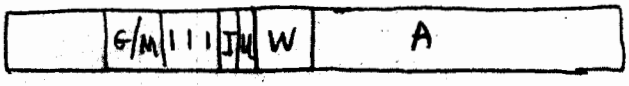
IMMEDIATE DATA

DATA ← W



DIRECT OR INDIRECT TO GENERAL REGISTER (W')

I { DATA ← Memory (W')
  { DATA ← Memory (memory (W'))



DIRECT OR INDIRECT, WITH INDEXING, TO SPECIFY DATA

I② { DATA ← Memory (A + General Register (W'))
   { DATA ← Memory (Memory (A + General Register (W')))

INS = INSTRUCTION PART

G/M = General REGISTER / MODE SELECTOR

I = INDIRECT BIT

W = WORD TO SPECIFY ADDRESS ON THIS PAGE OR DATA

U = UNUSED OR DIRECT DATA OR AUTO-INDEX BIT

W' = SHORT WORD TO SELECT A GENERAL REGISTER

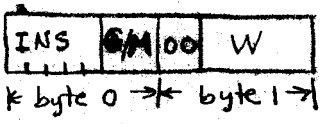
A = ADDRESS LENGTH DATA

① Preferrably sign extended ③ may or may not repeat indirect

② Memory (W') ≡ GR (W')

CGB 12/3/66

Expanded INSTRUCTION LAYOUT PDP-14X$_{GB}$



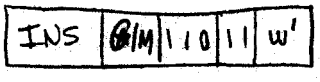
DATA ← Memory (THIS PAGE + W) – DIRECT TO PAGE

DATA ← Memory (Memory (This Page + W)) – INDIRECT TO PAGE

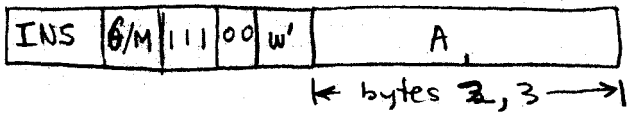
DATA ← W① – DIRECT DATA

DATA ← Memory (W') – DIRECT TO Registers (or memory)

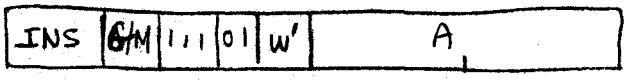
DATA ← Memory (memory (W')) – Indirect to registers (or memory)



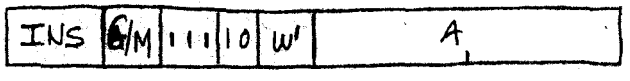
③

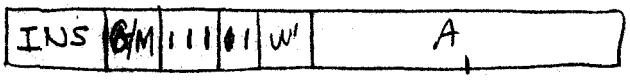


DATA ← Memory (A + General Register (W')) – Direct to memory, indexed.



Data ← Memory (Memory (A + Gen. Reg. (W'))) – Indirect to memory indexed④





③

① Preferably sign extended
② Memory (W') ≡ GR (W')
③ (Unused or Direct Data or Auto-index) bit
④ MAY OR MAY NOT Need Repeated indirect

LOGICAL MACHINE STATE

```
; General Registers
  Register Array General Registers [0:15, 0:7] ; General registers
; Program Counter
  REGISTER IDENTITY PROGRAM COUNTER [0:15]; General Register[0:15, Ø]
; MEMORY
  Register Array memory [0:15, 0:177777₈];

  Register array identity memory[0:15,Ø-7], general Registers[0:15, Ø-7]
; FLAGS
  BIT OVERFLOW FLAG ;  ARITHmetic OVERFLOW
  BIT CARRY FLAG;  IF SUM ≥ 2^16
  BIT ZERO FLAG ; IF NUMBER = 0
  BIT SIGN FLAG ; 1 IF NEGATIVE

  BIT INTERRUPT ON
  BIT INTERRUPT PROCESSING
```

Operations

1. TWO'S COMPLEMENT NUMBERS
2. FLAGS ABOVE MAY BE SET ON* INSTRUCTIONS AS A FUNCTION OF THE RESULTS

Instructions with a GR - Part, and Operands

LOAD ① GR(G) ← DATA

ADD* GR(G) ← GR(G) + DATA

SUBTRACT* GR(G) ← GR(G) − DATA

OR* GR(G) ← GR(G) ∨ DATA

AND* GR(G) ← GR(G) ∧ DATA

② XOR* GR(G) ← GR(G) ⊻ DATA

COMPARE* GR(G) − DATA

① MULTIPLY* GR(G), GR(G+1) ← GR(G) * DATA

① DIVIDE* GR(G), GR(G+1) ← GR(G), GR(G+1) / DATA

See key on next page

① ROTATE GR(G) ← f_1(Data, GR(G))

① SHIFT* GR(G) ← f_2(Data, GR(G))

③ ROTATE DOUBLE GR(G), GR(G+1) ← f_1'(DATA, GR(G), GR(G+1))

③ SHIFT DOUBLE GR(G), GR(G+1) ← f_2'(Data, GR(G), GR(G+1))

STORE DATA ← GR(G)

② LOAD STACK GR(G) ← GR(G)+1; Mem(GR(G)) ← DATA

② LOAD STACK, JUMP GR(G) ← GR(G)+1; Mem(GR(G)) ← PC
PC ← DATA

② STORE STACK DATA ← Mem(GR(G)); GR(G) ← GR(G)−1

② STORE STACK, RETURN PC ← Mem(GR(G)) + DATA;
GR(G) ← GR(G)−1

② CALL OPERATORS-TYPE1 GR(G) ← GR(G)+1;
Mem(GR(G)) ← PC;
GR(G) ← GR(G)+1;
Mem(GR(G)) ← DATA
PC ← OPCODE + FIXED LOCATION(G)

④ CALC OPERATORS-TYPE2 Mem(FIXED) ← PC
Mem(FIXED+1) ← DATA
PC ← FIXED + 2

each instruction is to a different location (fixed)

INSTRUCTIONS WITH A_n M (MODE) PART

JUMP (M = CONDITIONS OF FLAGS TO JUMP ON) (ϕ, -, flags)
IF f(M, FLAGS = 1) THEN PC ← DATA ELSE NULL.

③ EXECUTE (M = CONDITIONS OF FLAGS)
IF f(M, FLAGS = 1) THEN INSTRUCTION ← Memory (DATA)
ELSE NULL.

RESET Memory WITH AN M-MODIFIED ZERO
DATA ← f(M, ϕ) (yields 0, +1, -1,
RESET Memory WITH AN M- MODIFIED Memory
DATA* ← f(M, DATA)

M = 3 BIT: MICRO CODE

$1_{t=0}$ - COMPLEMENT
$1_{t=1}$ - +1
$1_{t=2}$ - COMPLEMENT

} yields: null, +1, -1, COMPLEMENT NEGATE

JUMP TO SUBROUTINE (M specifies: storage of FLAGS, INTERRUPT RESTORE

Memory (DATA) ← FLAGS ← Mode sel. ②
Memory (DATA+1) ← PC
PC ← DATA + 2

③ RESTORE FROM SUBROUTINE
M = RETURN WITH/WITHOUT FLAGS. ② - UN-NECESSARY UNLESS THE PREVIOUS INSTN IS FULLY IMPLEMENTED

IN/OUT M = 8 CONDITIONS LIKE PDP-10

W = DEVICE SELECT
Memory (PC+1) = DATA POINTER TO TRANSFER

KEY
* - sets FLAGS
① - OPTIONAL - (ROTATE/SHIFT WOULD THEN BE 1, OR 2 BITS)
② - DESIREABLE
③ - NICE
④ - MANDATORY - IF AVAILABLE, THEN ② and ③ COULD be sub-routines

cgs 12/13/63

G. Bell

INTEROFFICE MEMORANDUM

DATE February 6, 1967

SUBJECT Possibility of making many Peripherals at DEC with a Common Interface to all present and future computers.

TO

Ken Olsen
Nick Mazzarese
Win Hindle
Stan Olsen

FROM Gordon Bell

CC: A. Kotok
R. Savell

From time to time this has been considered, but has not been practical because the interface has been at the computer-peripheral control boundry. Also, because the designers want to optimize each system there is a tendency to design each control to tune a system. A common interface would benefit software design, as well as giving production flexibility, and minimizing system designs. I think that due to increased emphasis on remote terminals there is a trend (good one) to be able to remote any device, and as such the specialized interface will hopefully vanish from our universe. For example, IBM will shortly announce a card reader, card punch, line printer combination that connects to a standard Data phone.

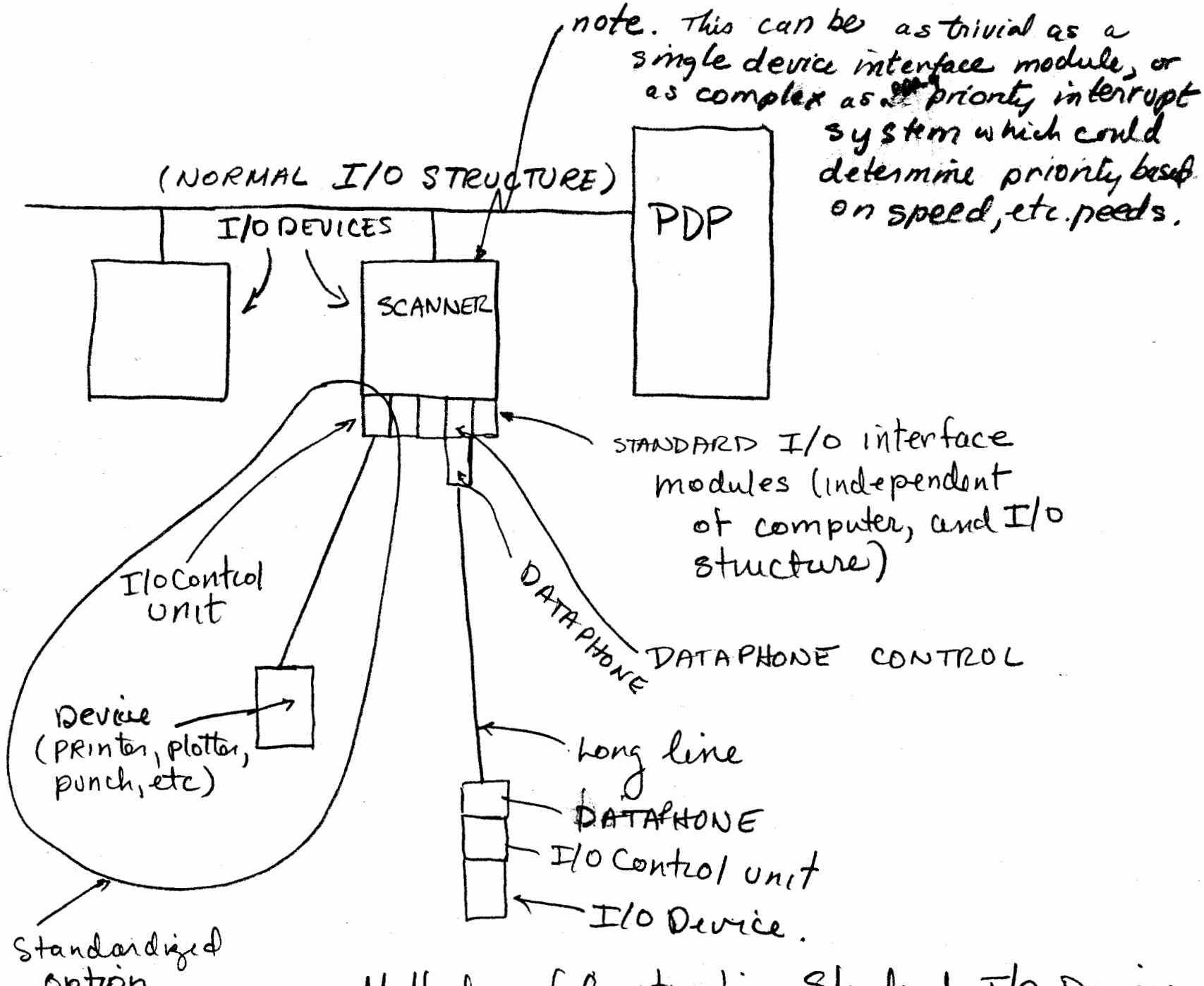
Therefore, I hope that since PDP-9,10, and 8I are in their pre-peripheral design phases, such an approach be studied as a means of having common I/O controllers across all computers and lines including new ones. Obviously, not all equipment fits the mold.

The equipment which looks most likely:

A-D-A
Paper Tape Readers & Punches
Card Readers and Punches
Printers
Plotters

Teletypes, Typewriters
Dataphones, and Phone Transmission stuff
slow displays
audio units
computer-to-computer buffers
relays, etc. (digital I/O)
Discs, Drums, mag. tape, DECtape, and Displays are undoubtedly too fast.

One possibility for such a system would be: (See attached sketch.)



Methods of Constructing Standard I/O Devices

cgb 1/25/67

digital INTEROFFICE MEMORANDUM

DATE: 26 February 1968

SUBJECT: Visit to DEC 15 February 1968

TO: J. A. Jones
Stan Olsen
Nick Mazzarese
Ed deCastro
Mike Ford
Win Hindle
Ken Olsen

FROM: Gordon Bell

After spending a day talking about computers, I'm reacting by trying to write down my version of what transpired. I hope others will do the same, as I felt a tremendous need to try to put things into a framework. Also, since Mike Ford asked me what machines to build, I wanted to write an answer.

To begin with, I'm sorry to hear that the X has been killed, since it potentially could have formed the basis for a compatible series. However, since it implied a large number of compromises in each group, it probably is not possible

Ultimately, it would have removed the 9 and 10 as product lines and no one likes to be part of a vanishing product line.

In Summary

My favorite suggestions (although I'd like some other points looked at) now are:

1. Form a product-planning group.

2. Patent the Homogeneous Read-Only plus Read-Write Memory (described below).

3. Don't build a 24-bit computer, fast. If you have to, you might look at the PDP-X, which has both 16 and 32-bit instructions for an average of 24-bits only it's better than most 24-bit computers.

4. Build an 8/I around larger boards and lower cost and better cabinet fabrication (see Data Machines/and Mike Ford's suggestions). Incorporating options for:

   a. Lower basic cost.
   b. Use of Read-Only Memory.
   c. Not moving the computer on slides, drawers, or books.

5. Build 10/I Develop 10/I Memory for use in 9/I, 10/I.

6. A nice, modular, vast 9:

   a. Very lost cost.
   b. Modular memory system a la X in upper models.
   c. Multi-processor at high end.
   d. Use Read-Only Memory (either internal or main) to increase speed of arithmetic, so that it competes with 24-bit computers.
   e. Add XR's and some scratch pad, a la Ed deCastro's large 16 X 32 bits (18 X 32) or (18 X 16).
   f. Make a processor for interpreting PDP-10 instructions and handling PDP-10 I/O devices using Read-Only Memory internally.

7. Build the 9-bit controller. As a stand-alone computer, and a controller to 9, and 10 devices.

8. Try to build special, total systems, based on software packages for existing machines (e.g. TS8; TS9; Administrative Terminal System-like thing (IBM's Multi-terminal editor);)

9. Do something to consolidate market planning across product lines.

10. Data Communications can still be yours, don't drop it!

Other Comments

Although my following arguments need to be based on cost/performance curves, I think our sales result from other factors, too: inertia, (IBM effect); lowest cost; and cost/performance.

The X group came up with some nice analytical relationships (e.g., instruction set utilization, performance of machines, checkout costs, etc.), especially when it was needed to back a decision. I would like to endorse their analysis and would hope the several machines that are being started could all be done on such underlying thoroughness. I'm suggesting a number of machines, and I'd really like to see cost/performance) memory size curves for each of them. I'm enclosing examples I did on the 360.

I'd like to put the following into a better framework then the linear list following, but think that's up to #1, below. The items are:

1. Set up a market-study group to try to consider the company as a whole, and have it connect with each product-marketing group. I would prefer to call and use the existing marketing groups for sales support, and sales, and information collection. Such a group would be more along the lines of product-planning group, doing market/cost analysis with a combination of design, production, and market inputs and would help guide product planning.

2. Try to increase the parts which are produced in common for all computers (for production, sales promotion, customer learning, and training reasons through some formal organizational body (maybe product planning)). (For example: parts of memories, peripherals, and peripheral controllers.) The structure of the 8, and 9 make it virtually idiotic not to have common controllers. The advent of the larger logic cards, then LSI, really necessitates this. Specifically Ed deCastro wound up with a 16 X 32 array, fast memory that could be used in the 9I+ and 10I. These parts include software (see 5 below). About a year ago (memo Feb 6, 1967), I suggested such a scheme for common peripherals, the arguments are still valid.

3. Start patent proceedings on the Homogeneous Read-Only, Read-Write Memory scheme, described below, which was developed on the 15 February meeting. It seems to be an effective way to get a nice local improvement in speed, in the case of simple processors like PDP-8, 9. I've looked at the PDP-8/I logic, and if you can wait long enough $\geq 1\frac{1}{2}$ years, I will make it go at .3 μsec/ read-only cycle, with only 15% more integrated circuits.

4. It is very difficult to measure the cost-benefit of another product in the line. I'm against any machine which is only incremental and does not try to better consolidate all DEC computers because I believe the cost of development and maintenance (especially software) is too high. For the same amount of development $'s, I believe system applications software has better payoff, i.e., a computer is converted to a particular device (a la typesetting, etc.).

5. Along the lines of 4, DEC could start collecting FORTRAN programs from places like SHARE, GUIDE, etc., which can be run on both the 9, and 10, and maybe 8. In fact, I think the generalized applications packages (e.g., a MATH-pak, or a STAT-pak, etc.) are the only reasons one would buy an IBM small 360 or 1130/1800 over DEC. This can be overcome by getting these packages into the DECUS library. A policy to use FORTRAN to code these packages seems like a good, long-range policy. Most such packages are available, free, now. (For example, all CALCOMP plotter programs exist in FORTRAN).

6. Investigate several design alternatives thoroughly. (The only implementation which traded-off cost for performance to come from DEC has been the PDP-8/S) I'd like for these to be investigated.

8/I-1 (lower cost using larger boards, and different bus structure to lower cost).

8/I-2 (lower cost-lower performance - possibly a serial version to run at 2 μsec/word or so)

8/I-3 (a rope memory control which allows some small set of core or flip-flop memory to be added along the lines of the homogeneous rope-core below).

8/I-4 (8/I-1+ 8/I-B).

9/I-1 (lower cost 9 - may or may not use rope control like the 9).

9/I-2 (fancier 9 structure with local MB and MA in a memory). The memory options would be based on some X designs and include:

(1) Memory box with connection or port to one processor with 4K, 8K or 16K.

(2) Memory box with connection or ports to two processors or a processor and controller with 4K, 8K, or 16K.

(3) Box to allow multiple (4-8) processors or controllers to connect to a memory port. The processor might use rope control.

9/I-3 (processor with a homogeneous read-only core structure in which Read-Only structure might include programmed floating point or FORTRAN operating system interpreter to speed up numerical calculations. This structure could do numerical work faster than a single 24-bit machine). The main memory structure would be along lines of 9/I-2 in which some modules would be rope.

9/I-4 (A fancier processor with rope control, along the lines of the 9, but a larger rope so that floating point and other common ops could be sped up.) Such a structure would also allow control functions, such as DECtape, Magtape, 680-like teletypes, high speed line concentrator, to be included.

This feature would be sold to customers for their use.

9/I-5 ≡ Mini-processor 10-2

A processor which would connect to 9/I-2 Memories, and PDP-10 I/O bus, and interpret only PDP-10 code (using rope memory). 16K X 18-bits would be minimum memory size. Use 10/10 + software.

9/I-6 ≡ Mini-processor 10-2

A processor which would connect to PDP-10 Memories, and PDP-10 I/O bus and be 18-bits wide, and interpret PDP-10 code. 16K X 18-bits would be minimum. Use 10/10 + software.

9/I-7 A multi-processor 9 (where multi ≥ 2), this should not only out perform a 24-bit computer, but should be cheaper, and more reliable.

9/I Increments

From a future product planning point of view, the 9 can be spruced up a bit, e. g.

(1) Three-core index registers.

(2) Replacement of first 16-core register to speed up operations using index registers temporary, and auto-index registers.

(3) Investigate if MIT's (Lee), and Harvard's PDP-9 time-sharing system is marketable.

(4) Incorporate Edinburg's PDP-7 MACRO Assembler in software.

(5) See why the PDP-9 FORTRAN is so bulky, and slow.

10/I — Integration of processor, compatible with 10. Integrate other components, attempt to use 9/I sub-components.

X-1 — Smaller scale version of X.

24 — Another computer.

9-bit computer — A smaller than PDP-8 computer which would be part of a series of weakly, compatible machines of our 9, 18, 36-bit series. This would stand alone as a minimum computer.

Also it would be specifically designed to serve as the <u>controller</u> for elaborate devices, or a group of devices which could be used on the 9 and 10, (also, 8 if desirable). It would be a front-end controller for communication lines for the 9 and 10 (scanning and buffering). This could be an important product, if it can be designed.

Note: This computer is along the lines of one we'd like built for here. I sent Mike Ford a copy of an 8-bit computer, along these lines which we thought could be built for $3K at Carnegie. I would like to remind people that the tasks which are done in 8-bit chunks, can be done nicely in a 9-bit computer. In fact, it may be a 'silly 1-bit longer'.

8-bit computer: Although this is also minimum, it doesn't look very good as a controller to an 18 or 36-bit machine. I've never felt that 8 is an especially good base, and base (2^9)'s has 100% more states than an 8-bit base.

7. Do something about Data Communications Market (product) planning, before it's too late! Although it still isn't too late, waiting another year before starting to plan may be. (See memos of about 1½ years back). This is just right for DEC as a market (especially with the new 9×10^6 bit disk). This includes both telegraph message switching, and display (text-keyboard) at 2400-bits/sec concentration. Respond positively, creatively, and correctly to ARPA's RFQ for their network switching computers. This job may take a PDP-9, and the present DEC organizational structure precludes thinking of the problem this way.

   Right now IBM has just announced an option to connect to the 360/25 to give 64 telegraph lines in and two high speed lines out in a concentrator and the price isn't awfully unreasonable, especially since they rent.

The proposed 24-bit machine

I think this machine isn't especially good as it's a compromise between a medium computer (16/18-bits) and a reasonably large one (32/36-bits). Although a 24-bit machine will out perform an 18-bit machine (for the same level of technology - i.e., memory speed) due to added index register and extra instructions. I don't give one (e.g., 910-920-like) more than a factor of 2 over a PDP-9 for the same memory speed, although one can build a 24-bit computer

that performs like a large computer (e.g. CDC 3200).

Mostly, I don't like the idea of another product which has no chance of bringing the other product's production, programming, or sales training any closer together. (I can show you a real mess at IBM prior to the 360 in which slightly better, non-computible products kept getting stuck in cost/performance, cost, or performance holes.)

I agree that thereis a significant hole between the 9 and 10. This hole can be filled with existing product parts rather than introduce another incompatible series. In both the 9 and 10, there exists the possibilities for a nice filler. There is a discussion of the 360 as an example of filling.

The issue of whether a multi-processor 9 is better than a mini-processor 10 (9/I-5 or 9/I-6) should be based on cost/performance comparing say space/time for FORTRAN in the two machines, peripheral costs, instruction set power, and the fact that 10 software is already pretty far advanced. (Such a machine would use a memory of 16K words). I dont believe that the PDP-10 group is capable of making such a design or evaluating thefeasability.

Again, I think $'s should be spent on support software instead of basic software like maintenance routines, compilers, etc. A three or four year extensive effort to get DEC to the level of the SDS 900 series. Also, I believe that if any present 24-bit manufacturers want to, they could wipe you out! On the other hand, with a dual processor 18-bit machine, you could make things rougher on them.

I looked at some sample SDS 900 series programs, and though admittedly not typical, in 100 instructions I counted, an 8-bit address was sufficient 75% of the time. This compares favorably with the statistics in the instructions measured by the X group. I don't believe the small address hack is a hack, but rather an efficient use of bits.

360 Lessons

Enclosed are some notes on a talk given by Fred Brooks, one of the IBM 360 designers at a talk at IBM Poughkeepsie. I have also enclosed my IBM 360 cost/performance graphs, as I believe this kind of analysis is necessary to find a filler between the 9 and 10. The issue of ROS and multi-processors can be seen from the 360. For example, the utilization of memory

$$= \frac{\text{number of memory cycles used}}{\text{number of memory cycles available}}$$

Model	Memory Utilization
30	.2
40	.4
44	.55
50	.5
65	.37 - .18
75	.54 - .27

This is low compared to the PDP-8,9 machines, but on the other hand, the complex 360 instructions do move. Their 1130 and 1800 are like .75. ROS causes part of the problem, but the complex instructions do too. The 10 would probably be pretty low too, due to floating point, and multiple memories (in fact, a 32K system would put it below .5).

I proposed a smaller set of 360 processor primitives which would give better cost/performance in the 360, and I think these also apply to the 9+, 10-, 24-bit issue. These are given below.

An Alternative Series of Processors to Cover the Range of Computing Power.

Graph 4 indicates that an alternative approach based on multiple Pc's is feasible. Suppose the following Pc's are chosen as primitives:

Model	Power
C(20)	1
C(30')	4
C(44)	30

Then by combining primitives, the performance values of the present computer line can be obtained, as shown below:

Model	Power	Pc Cost
C(20)	1	.00049
2-C(20)	2	.00098
C(30)	2	.00125
C(30')	4	.00125
C(40)	6	.00295
2-C(30')	8	.00250
C(50)	15	.011
4-C(30')	16	.005
C(44)	30	.004
2-C(44)	60	.008
C(65)	60	.022
C(75)	80	.0365
3-C(44)	90	.012
16-C(44)	480	.064
C(91)	500	.09

Note that in every case, the multiple Pc approach performs significantly better than the uni-processor, at a lower cost. (The multiple Pc interconnection cost with Mp, and the problem of breaking the task apart has been ignored.)

INTEROFFICE MEMORANDUM

PM 11-3

DATE: 1 April 1968

SUBJECT: Reexamination of 24-bits

TO:
Nick Mazzarese
Win Hindle
Ken Olsen
Ed DeCastro
Gordon Bell
Larry Portner

FROM:
John Cohen

I. Background

Since the demise of the PDP-X, a number of possibilities for new products have been discussed. One of these is a medium-scale 24-bit machine. Initial reaction was very negative - in fact, everyone I spoke to was against it. The feeling was that the market was tending away from existing 24-bit machines and no one was sure who would buy such a machine. However, further consideration, especially a technical comment by Ed DeCastro, make me want to bring the issue up again.

Ed points out that memory speeds are increasing faster than hardware speeds and that this trend is expected to continue over the next few years. The implication is that it will become more and more difficult to design the hardware to keep up with the memory. The simpler the addressing scheme and instruction set, the easier it is to achieve hardware speeds. An instruction length of 16 or fewer bits naturally leads to a complicated addressing scheme - along with the associated hardware complexity. A 24-bit machine can be simply and directly addressed - thus warranting its further consideration.

The next section reviews a number of technical and marketing considerations which seem to lead to 24-bits. Finally, section III contains a specific proposal to build a 24-bit product line.

II. Technical and Marketing Considerations

A. Objectives

After talking with many people, I tend to feel that there are three valid reasons for building a new computer line. In order of estimated importance, these are:

--bridge the "cost gap".

A PDP-10 typically sells for more than 175K, while a PDP-9 most often sells for 125K or less. There is a void between these two machines which should be filled. There is some question as to whether a big 9 or a small 10 could do this job effectively.

--Get better performance/cost.
New concepts of machine organization make it possible to produce a computer with better performance/cost than the PDP-9. Although performance/cost is not necessarily the thing that sells computers, an improvement would not hurt.

--Make programming easier and cheaper.
Without any question, one of the problems with our present small and medium scale computers is that they are difficult to program. Since we are likely to provide more applications software to our customers in future years, this can be a real difficulty. On a long term basis, we would save money with a more "programable" computer.

B. Hardware/Memory Speed

According to Ed DeCastro, the current trend is for hardware speed to increase more slowly than memory speed. From a cost/performance point of view, a computer is optimally designed when its memory speed is nearly balanced by its logic speed. This is seen to be true from the following reasoning - suppose a computer memory is much faster than the hardware. Then the memory could be replaced by a slower (and cheaper) memory without substantially changing the performance of the machine. A similar argument holds if the hardware is much faster than the memory. Henry Burkhardt points out that the Sigma 2 is mismatched in the sense that their hardware is considerably slower than the memory. They could replace the fast memory by a slower one without hurting the through-put capabilities.

The implication of the hardware/memory trend is that it will become more difficult, over the next few years, to design hardware to keep up with memory. The more complex an instruction set, the more this effect will be amplified. A 16-bit computer must naturally have complex effective address calculation. For example, on the PDP-X,a check first must be made to determine if an instruction is basic or extended. If it is basic, it must be further determined whether it is short or long form addressing. Then it must be determined if the addressing is immediate or memory reference. The point is that this type of scheme will become more expensive to implement as memory speeds increase.

This leads naturally to the consideration of 24-bits. First of all, I think any new machine we build should have a word length which is a multiple of 8. This is becoming fairly standard in the industry and people I talk to uniformally agree that it will help us sell systems which interface with other equipment. A 24-bit instruction allows direct memory referencing without paging (PDP-8) or relative addressing (PDP-X). Without question, this is a major hardware and software simplification. It makes a machine more easy to understand for all involved - engineers, programmers, salesmen and customers.

If the hardware speed/memory speed argument is correct, the manufacturers of 16-bit computers may be switching to 24-bits in the next 2-4 years. If we are not committed to 16-bits, there is no reason why we should not be the first to "switch" to 24.

C. The Waste of Memory Argument

Computers use one of two addressing techniques which could be called direct and non-direct. Many medium scale and large systems use the direct approach. Each instruction contains enough address bits to directly reference all of core memory. For example, the PDP-10 instructions have 18 bits to address a maximum of 256K. The advantages of such a scheme are that it is relatively easy to implement in hardware and that it is convenient for programming. However, many people say that it has the disadvantage of wasting instruction bits. The claim is that most memory references refer to locations which are relatively near the instruction. Thus, the claim is made that bits can be saved if addresses are given relative to the issuing instruction, or "local" to a memory page.

Two commonly used non-direct methods are the page scheme and the relative address scheme. For example, the PDP-8 memory is divided into 256 word pages. In each memory reference, the program must specify whether the effective address is in the current page or in a special, fixed page. If the address is in neither of these, then the reference must be made indirectly, using another word.

In the PDP-X, a "short form" was used if the effective address was located within 128 words of the instruction. If not, then another full 16-bit word was necessary to specify the address.

The proponents of the non-direct addressing schemes claim that 30 to 40 per cent of the bits in direct reference computers are wasted. The opposing view holds that paging and relative schemes make the computer inherently more complicated and cause programming to be more difficult and costly.

It is my personal feeling that the waste of memory argument is a "red herring". To be sure, certain programs can be coded in, say, 30% fewer bits in a non-direct computer. However, if the program is half data and half instructions, the savings is only 15%. In addition, there is no need to make relatively small programs even smaller if part of the computer memory isn't used. Therefore I believe that the 30% figure has to be discounted to a 10% savings. My feeling is that the advantages of this savings are more than out-weighed by the increased hardware complexity and software development difficulties.

D. How Many Registers?

If we do build a 24-bit machine, I feel that it should have one accumulator and one index register. This would be cheaper to implement and would make the programming easier. Minor disadvantages would be slightly larger

programs and the possibility of unfavorable comparisons on competitive checklists. An example of a computer with multiple accumulators and index registers is the PDP-10. I agree that the multiple registers give the capability of generating smaller and more efficient programs. However, I feel that the extra costs involved out-weight the advantages. Hardware development and maintenance is more expensive.

Possibly the best argument against multiple registers is in software development. In my experience, I have found that most programmers work better on machines which offer them only one method to perform a given function. If there is more than one method, they will spend much time and effort trying to optimize. The real objective in programming usually is to produce a program that works, rather than a program which works and is the fastest program possible and is the smallest program possible. This objective can be reached most easily on a simple computer with only one index register and one accumulator.

Unfortunately I don't have any solid figures to support the contentions made here, but I strongly suggest that a single index register and accumulator is to our advantage. It "forces" easy programming and makes the hardware easier to build and maintain. In addition, the nature of such a machine causes software systems to be more simply organized and thus easier to maintain.

E. The Use of Read Only Memory

There are basically two alternatives for internal computer structure - conventional orgainization and read-only memory control. The latter has the advantages of being flexible and cheaper for complex instruction sets. It has the disadvantage of being inherently slower than hardware. Computers built without ROM control tend to be faster, but inflexible in instruction set. However, if the instruction set is simple, conventional organization is cheaper than ROM control.

Since the discussion here is about a simple 24-bit machine, I think we are lead to the conclusion that read-only memory control should not be used.

III. A Recommendation

About a month ago, I suggested that DEC built both a 16 and a 32 bit computer. Because of the considerations above I'd recommend shelving the 16 and 32 ideas and focussing on 24. I think it promises the most immediate pay-off and will interfere least with existing product lines. Specifically I recommend:

A. 24-Bit Processor

We should build a 24-bit computer with direct memory addressing (no paging or relative addressing). There should be one accumulator and one index register (plus an additional register for multiply and divide operations).

The instruction set should be much simplier than the PDP-10 or PDP-X. An example of what I have in mind appears in the appendix.

The system should not be organized around time sharing. Multiply, Divide and Floating Point should be optional hardware. The computer should not be micro-programable via read-only memory.

B. 8-bit Peripheral Controller

We should also build a simple 8-bit micro-programable processor to be used primarily as a peripheral controller. It should be of intermediate internal complexity-more complex than the Interdata II, less complex than the PDP-X - about at the IBM 360/30 level. The machine would have a secondary use as an emulator for the 24-bit machine. It would probably sell at 1/3 the cost and run at 1/10 the speed. It could presumably be built before the 24-bit processor and could be used for software development for the larger machine.

C. Interfacing Standards

Computer Technology Limited has, in theory, a product line with exceedingly rigid interface standardization. I have the impression that we have never put in enough effort in this area and have had difficulties when trying to configure non-standard systems. Our engineers should look closely at the CTL Modular One and at functionally large macro-modules. Neither of these may be the answer to our interface standardization problems, but they should provide us with a starting point.

APPENDIX

This appendix is a description of a simple 24-bit instruction set. Input/output and interrupt instructions are not considered. From the point of view of software development, I would be extremely happy to work with such a machine.

The instruction format is:

where OP is a 6-bit op code (64 possibilities)
X is the index register specification
I is the indirect address specification
ADR is a 16-bit address (up to 64K 24-bit words)

Location 0 refers to the accumulator. Location one refers to the multiply/divide register, when the option is present. Location two is the subroutine linkage register and location three the index register (similar to the PDP-X). An undefined operation code causes the program counter plus one to be stored in location four and a branch to location five.

The instructions are:

LDA load accumulator
STA store accumulator
ADD add
SUB subtract
INC increment
NEG negate
COM complement
TST test
BRU branch unconditionally
BAL branck and link
BCT branch on carry true
BCF branch on carry false
BZT branch on zero true
BZF branch on zero false
BNT branch on negative true
BNF branch on negative false
CLR clear
AND and
ORA or
XOR exclusive or
SHF shift
BLM block move
CML compare logical
CMA compare arithmetic

LDC load character
STC store character
ICP increment character pointer
MUL multiply
DIV divide
LML logical multiply
LDV logical divide

LDA and STA load and store the accumulator. ADD and SUB add and subtract the effective word to the accumulator. INC adds one to the effective word. NEG and COM negate and complement the effective word, respectively.

There are three condition code flip-flops as in the PDP-X. One is carry or overflow, the second is zero result and the third negative result. TST sets these condition codes (except carry) based on the status of the effective word. BRU causes an unconditional branch to the effective address. BAL causes the program counter plus one to be stored in the subroutine linkage register and then a branch to the effective address.

BCT, BCF, BZT, BZF, BNT and BNF cause conditional branches on the condition code status.

CLR sets the effective word to zero. AND, ORA and XOR perform logical operations on the effective word and the accumulator, leaving the result in the accumulator. SHF shifts the accumulator as specified by the effective address. Zeros are shifted in from the right or left. No provision is made for shifting in one's or for rotating the accumulator.

BLM is a block move instruction, which can be an option. The effective address points to a three word block containing a destination address, a source address and the count. The number of words specified by the count is moved from the source address block to the destination address block. CML and CMA compare the accumulator to the effective word and set the condition codes appropriately. CML does a logical compare while CMA does an arithmetic compare.

Three instructions for character manipulation are included, possibly as an option. They operate on a character pointer with the following format:

where CT is zero, one or two indicating, the first, second, and third characters in the word.

ADR is the address of the word containing the referenced character.

For example, if CT is one and address is 1,000, the pointer refers to the second or middle character in memory location 1,000. The effective word of an LDC instruction must be a character pointer. The appropriate character is moved into the accumulator bits 16-23. Bit 0 through 15 of the

accumulator are set to zero. STC takes bits 16-23 of the accumulator and stores them as specified by the character pointer in the effective word. ICT increments the character pointer. If CT is zero or one, one is added to CT. If CT is greater than one, CT is set to zero and one is added to ADR.

The optional multiply/divide hardware has four instructions - arithmetic multiply and divide and logical multiply and divide.

ljh

digital INTEROFFICE MEMORANDUM

DATE: May 24, 1968

SUBJECT: PDP-10 COMPARABLE WITH SIGMA 5

TO: Gordon Bell FROM: Ken Olsen

SDS seems to have outsmarted us when they came out with their Sigma 5. They now have the lowest priced computer of this size, and are taking many orders away from our PDP-10.

What can we cut out of the PDP-10 to make a useful, low-priced computer?

Ken

February 26

...I'm glad you ask that question. On ~~April 2?~~ 1968 I wrote a number of possible solutions which came out of my visit on 15 February, and on 21 of February 1968 Seligman wrote a memo on PDP-9 which said roughly the same thing.

Namely, we say: The Sigma 5 came out because of the PDP-10 and is presumably selling better because of lower cost, or 32 bits or people not able to sell the 10 IO structure or the 10 IO structure may not be as good. The 10 people probably aren't interested in any compatibility with the 9, or are interested in a scaled down version of the 10. I expect future plans for the 10 to be more extensive in its ability to time share, with better (more exotic) program mapping to cut down on the monitor overhead.///... All of these take the machine up the price scale, but make it more useful or better for timesharing. I don't think the 10 designers are particularly interested in the problem...or maybe should they be? One thing that Seligman and I agree on in this regard, is that a very useful, PDP-10 compatible machine Processor could be made which is probably based on a Read Only Store to interpret the PDP-10 order code. It would be slow by 10 standards, but on the other hand could /it/ maybe exist for as little as 20-30 k$....and be only 1/4 as fast. Just integrating might help on the cost question.

In regard to the stuff taht John Cohen is doing we are obtaining very interesting results by coding various problems, and intend to find the best /of/ machines for various problem classes. /I/ I am asking John to add coding for the PDP-10 to see how it s fares, .. or am trying to find just what it is the large machine is good at. Several weeks ago, I started examining the possibility of connecting many of these computers together, to see if it helps the power problem, with the hopes of wiping out large machines for most problems, and it appears as if this may just be possible. Therefore, in the 8 bit machine, that sells for $1/$2k I want to put some escape mechanism so that it can exist in a high performance version with 32 or more bits, and floating point. As of now, the problem seems easy, but may not look so good as we get closer to the solution. So far the 8 bit (cough) $2k machine is better than and x, a 3, the 8, /all 16 bitters, and maybe the 10, no maybe we outht to look at a problem it doesn't do as well

cc

have Seligman circle it + this summ

SUBJ: POTENTIAL TO SHIP MORE BY ACCELERATING ENGINEERING PROJECTS

TO: Operations Committee

0964

FROM: OOD

December 6, 1974

General

1. Work on all projects that require sales and marketing support:

   A. The TC70 project needs analysis and measurement. Also analysis of RSX 11D/M and Comtex will probably enhance sales because of increased product knowledge.

   B. Benchmarks and product comparisons. We really need to organize this activity with PL's to avoid duplication.

   C. MTBF book on PDP-11.

2. Better analysis of the critical projects and elsewhere using staff and development resources now will assure these products will make it with low ECO's. These activities include: Potter (11A/05 PS), Best + Naelcke (PDP 14 I/O Modules, 32K sense, 11/A05 + 8/A PS, floppy RxW); 1 on 1 logic design reviews by persons in research and elsewhere (floppy, TS, COMM options, microprocessor); LSI groundlogical design; simulation to insure producibility--use on various high volume options (e.g. 11/A05).

3. Generally accelerate to the limit to manage: floppy, the small tape, large disk, 11/A, WD, and 11/OK

4. Networks. Real push and start selling components now for delivery prior to original June date.

5. IAS the timesharing system on 11/45 and 11/70. Will certainly compete with the HP3000.

6. Multiprogramming on RT using BASIC

7. Interprocessor High Speed Communications Link.

8. KL10. Can it use help?

9. VT50 copier.

10. A project that would get a quick writeable control store on 11/40. This would defuse the Microprogramming WCS on both the HP21MX and the DG Eclipse. We might not actually ship any until the OK, when all the smoke clears.

11. We should brainstorm to see if there is a trivial turnkey system which could be built to install immediately.

12. General expense reduction. Get a data base program to cut down on the tons of paper we distribute now throughout engineering!

SUBJ: POTENTIAL TO SHIP MORE BY ACCELERATING ENGINEERING PROJECTS

0964

TO: Operations Committee

FROM: OOD

December 6, 1974

General

1. Work on all projects that require sales and marketing support:

   A. The TC/D project needs analysis and measurement. Also analysis of RSX 11D/M and Comtex will probably enhance sales because of increased product knowledge.

   B. Benchmarks and product comparisons. We really need to organize this activity with PL's to avoid duplication.

   C. MTBF book on PDP-11.

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3. Generally accelerate to the limit to manage: Floppy, the small tape, large disk, 11/A, WD, and 11/DK

4. Networks. Real push and start selling components now for delivery prior to original June date.

5. IAS the timesharing system on 11/45 and 11/70. Will certainly compete with the HP3000.

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11. We should brainstorm to see if there is a trivial turnkey system which could be built to install immediately.

12. General expense reduction. Get a data base program to cut down on the tons of paper we distribute now throughout engineering.

13. Personnel and other support resources probably should be moved to liaison, support and communications roles.

OOOIMJK

December 6, 1974

R. J. Murray
Group Planning Manager
Valentine Holdings Limited
50-54 Clayton Road
Clayton North, Victoria 3168

Dear Mr. Murray:

We don't have a really good production system for ISP available. The CMU group is continuing to work on it however. Considerable design aids were made available for the PDP-16 modules for assembling hardware. These are not generally available now as the 16 isn't supported. They were written in BASIC, and converted blocks to a wire list.

Prof. Chu, at U. of Maryland, College Park, Maryland, has a system, CDL, which he might make available to you. You might contact him.

A copy of the Bell-Grason-Newell book is enclosed.

Sincerely,

Gordon Bell
Vice President, Engineering
Professor, Computer Science
Carnegie-Mellon University (on leave)

GB:mjk

Enclosure

DIGITAL EQUIPMENT CORPORATION, 146 MAIN STREET, MAYNARD, MASSACHUSETTS 01754
(617)897-5111 TWX: 710-347-0212 TELEX: 94-8457

0967

VALENTINE HOLDINGS LIMITED

50-54 CLAYTON ROAD, CLAYTON NORTH, VICTORIA 3168.
TELEPHONE: 544 0333 · CABLES: "VALENCARD" MELBOURNE
TELEX A.A.32762 AUSTRALIA

PUBLISHING

PRINTING

COMPUTER SERVICES

November 27, 1974.

Dr C Gordon Bell
c/- Digital Equipment Corporation
146 Main Street
MAYNARD. MASS. 01754. U.S.A.

Dear Dr. Bell:

We have a current project which is concerned with the design of some small special purpose computers, along the lines of the PDP-16 system.

Because you have originated techniques for the analysis of such designs using ISP, I would like to know from you whether it is possible for us to have access to ISP or some similar hardware modelling scheme you may be aware of. In particular, I would like to explore the possibility of having ISP made available to us locally.

As the only immediate alternative is develop our own modelling system, I would appreciate it if you would give me an answer as promptly as possible.

Yours faithfully,

R.J. MURRAY.
Group Planning Manager.

RJM/lc.

Dear

We don't have a really good production system for ISP available. The CMU group is continuing to work on it however. Considerable design aids were made available for the PDP-16 Modules for assembling hardware. There are ~~are~~ not generally available now as the 16 is not supported. They were written in BASIC, and converted ~~to~~ to blocks to arrive list.

Prof Chu at U of ~~Mary~~ Maryland, has a system, CDL which he might make available to you. You might contact him.

College Park, Maryland

Acquired the Bell - Sawyer Model 1 PDP 8 as attached

A copy of the

digital INTEROFFICE MEMORANDUM

TO: Circulation

DATE: December 11, 1974

0963

FROM: Gordon Bell

DEPT: OOD

EXT: 2236 LOC: ML12/A51

SUBJ: ATTACHED NATIONAL SCIENCE FOUNDATION PROPOSAL

I was given this proposal to review by the National Science Foundation. Note, they hope to use the 11/WD-on-a-board.

The work is interesting, because it addresses the problem of applying the microcomputer to small systems, which would have been done with analog techniques. If they get the grant, I believe we should try to sell them for sure to use our machines--particularly since the support is with an 11/35. This would give a user an extremely unique and powerful capability to apply the computer to problems, and it goes well beyond the low level tools we usually supply (e.g. Operating Systems, BASIC, and FORTRAN).

The proposal is worth reading, and this type of program is one that I believe we'll be seeing more of with smaller machines.

Circulate, date, and return:

Date

Jim Bell
Andy Knowles
Richie Lary
Bob Savell
Mark Sebern
Steve Teicher
Brad Vachon
Rob Vannaarden
Pete Van Roekens
Mel Woolsey

1086

TO: John Kulik

DATE: November 5, 1973

FROM: Gordon Bell GB

DEPT: Engineering 12-1

0969

EXT : 2236

SUBJ: MIKE DOREAU

Please arrange to give Mike Doreau a visitors-type badge which would allow him in the mill unescorted. He is a doctorate student from CMU and is writing his thesis on a subject here at DEC. Mike will be working with Lou Abel and will probably have some weekend work. He will be using the Thompson Street entrance.

Thank you.

GB:mjk

December 28, 1973

Please extend Mike Doreau's visitor's badge to the end of March.

Gordon Bell GBell mjk

5/30/74

John,

Please extend Mike Doreau's visitor badge until Dec. 31, 1974.

Gordon Bell Gordon Bell

12/13/74

John,

Please extend Mike Doreau's visitor badge until June 30, 1975.

Gordon Bell GBell

SUBJ: LA18Ø

DATE: 12-16-74
FROM: GORDON BELL

* *
PLEASESEND TO: FILE
* *

SUBJ: LA18Ø TO ENTER PRINTER BUSINESS

To: Ed Corell
Al Huefner
Andy Knowles

CC: Products Committee
Marketing Committee

Are we missing a tremendous opportunity by not pushing the LA18Ø faster and harder? Every competitive low end system I see has a Centronics on it (e.g, Singer, DEC, DG, etc.). Can we get this market away on the issues: of quality, reliability, price, service?

The interface to these systems is the same one we use? Is it an easy add-on or replacement business? All the printers out then are probably totally worn out now, and really costing the user or supplier vis a vis service.

What youse think? Can we get components and the product manager to make a proposal?

GB:mjk

SUBJ: MICROCOMPUTERS

DATE: 12-16-74
FROM: GORDON BELL

* *
PLEASESEND TO: FILE
* *

COMPANY CONFIDENTIAL

Subj: MICROCOMPUTERS--DATA NEEDED TO USE THEM INTERNALLY

To: Distribution

Rick and Mike did an excellent job of designing and benchmarking two terminal designs (PTS and VT51). The results are attached (I distributed this before). We need more data from them on the WD and Motorola chips. Rick Merrill has stated that the chip count using the 11/WD is 3X that of an 8080 based system for PCS. I want to see the design!

We are entering a computer market period where designs will be benchmarked by: chip count, cost, number of ROM/RAM bits, speed, apparent ease of hardware design by simple interface chips, clocks, etc., compatibility, and software (languages, host machines, and subprograms--ease of software design). Second sourceness is an issue. We have the benchmarks for bits/time for some small subprograms. We need to fill out the matrix of cost for say the above system--since it is a relatively large system, and add the Motorola 6800, 6700 (to be announced), and WD 3 chip and 1 chip set. This will give us some feeling as to where we (can) stand, and the direction for improvement.

For our own systems, e.g. VT51, it seems clear to me that the chip count probably isn't the constant on its success.

Our internal criteria:

1. Total cost--probably dominated by RAM/ROM. Clearly will be when the microprocessor people start shooting it out in the price war and cost=0.

   In VT and LA's the package and mechanics dominate.

2. Programming support--we have to limit ourselves to a single design and evolve it or evolve with it. These smart devices,

SUBJ: MICROCOMPUTERS

DATE: 12-16-74
FROM: GORDON BELL

e.g. VT51--appear to all be different in some way--a small programming problem.

Right now we're on a course to use WD externally, and we have chaos internally. We must have data to know why we can't use WD internally or what we have to do to use it? Can we better use their 1 chip processors, as it's bus compatible.

I've asked MOTOROLA to give us a real hard sell on microprocessors and their application. If they're really great, then we ought to turn on internally for various products. However, its clear to me they are our external competitor to boarded and boxed computers.

GB:mjk
Attachment

Distribution

Dick Clayton
Lorrin Gale
Andy Knowles
Mike Leis
Rick Merrill
Larry Portner
Bob Puffer
Tom Stockebrand
Steve Telcher
Rob VanNaarden

To: Clayton, Teicher, Eorell ✓

digital INTERCOFFICE MEMORANDUM

0973

TO: Gordon Bell
Tom Stockebrand
Ken Fine
John Buzynski
Chuck Kamann
Steve Teicher

DATE: December 5, 1974

FROM: Mike Leis/Rick Merrill

DEPT: A/N Display

EXT: 3406 LOC: 5-3

DEC 09 1974

SUBJ: PRESENT SIZE AND CHIP COUNT OF THE VT51 AND THE PCS

Attached are simplified block diagrams showing the chip per function of the VT51 and PCS.

Totaling the microprocessor, clock, equal size memory, UART, video and interfaces for cassettes, printer, and keyboard, the VT51 has 159 chips and the PCS has 185 chips. The VT51 has several other functions which bring its chip count to 186, and the PCS is not completely minimized.

The VT51 P.C. boards presently have 828 square inches or 4.4 square inches per chip, while the PCS may have 135 square inch of PC boards or .7 square inches per chip.

A study will follow later attempting to quantize the costs associated with the radically different densities. Also, we must investigate the cost differences between the VT50/51 style boards and the DEC standard boards.

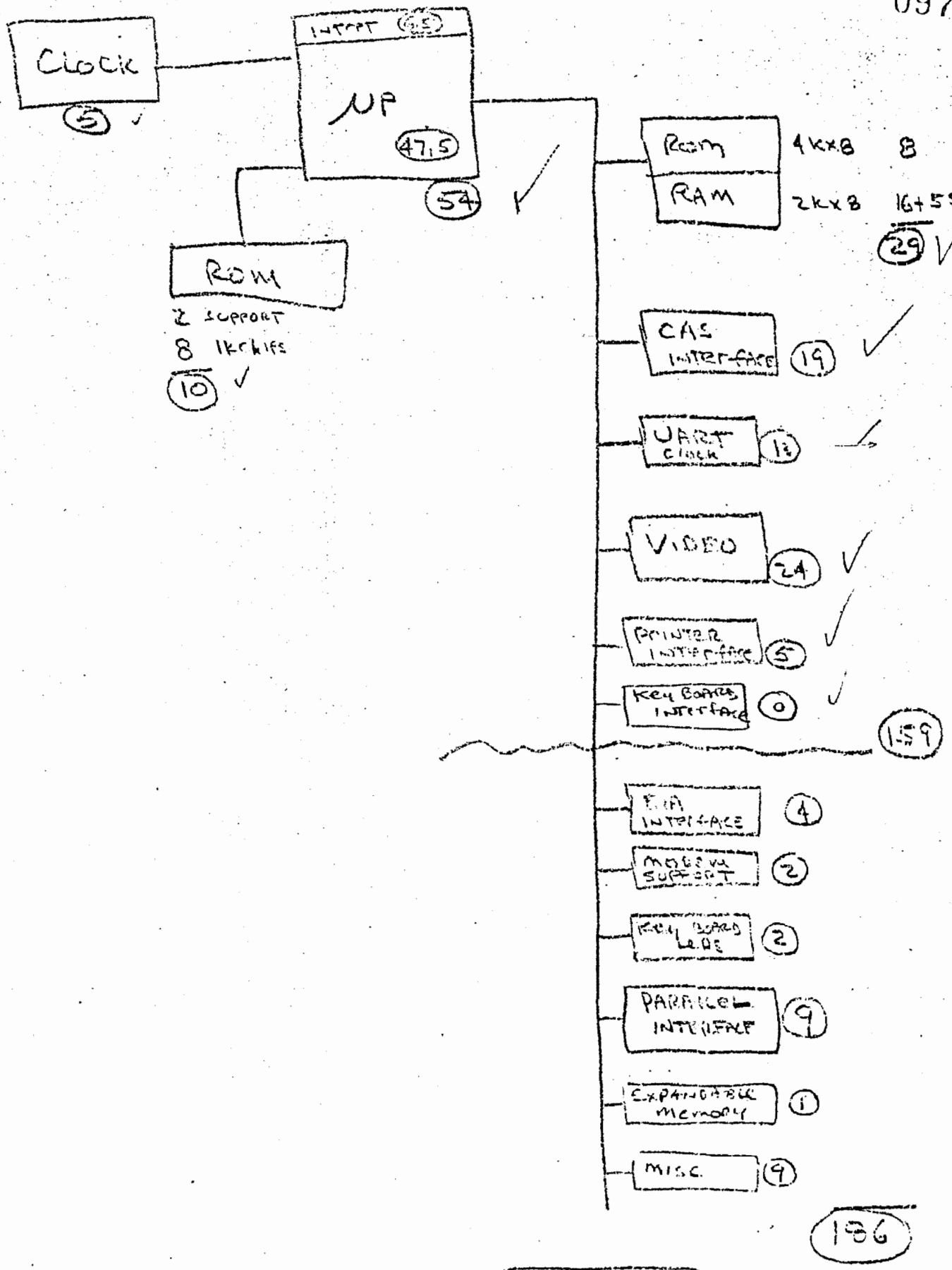
Rick What does the WD design look like, by comparison.

Also, the Motorola 6800 design?

G B

FM: Leis/Merrill

0974

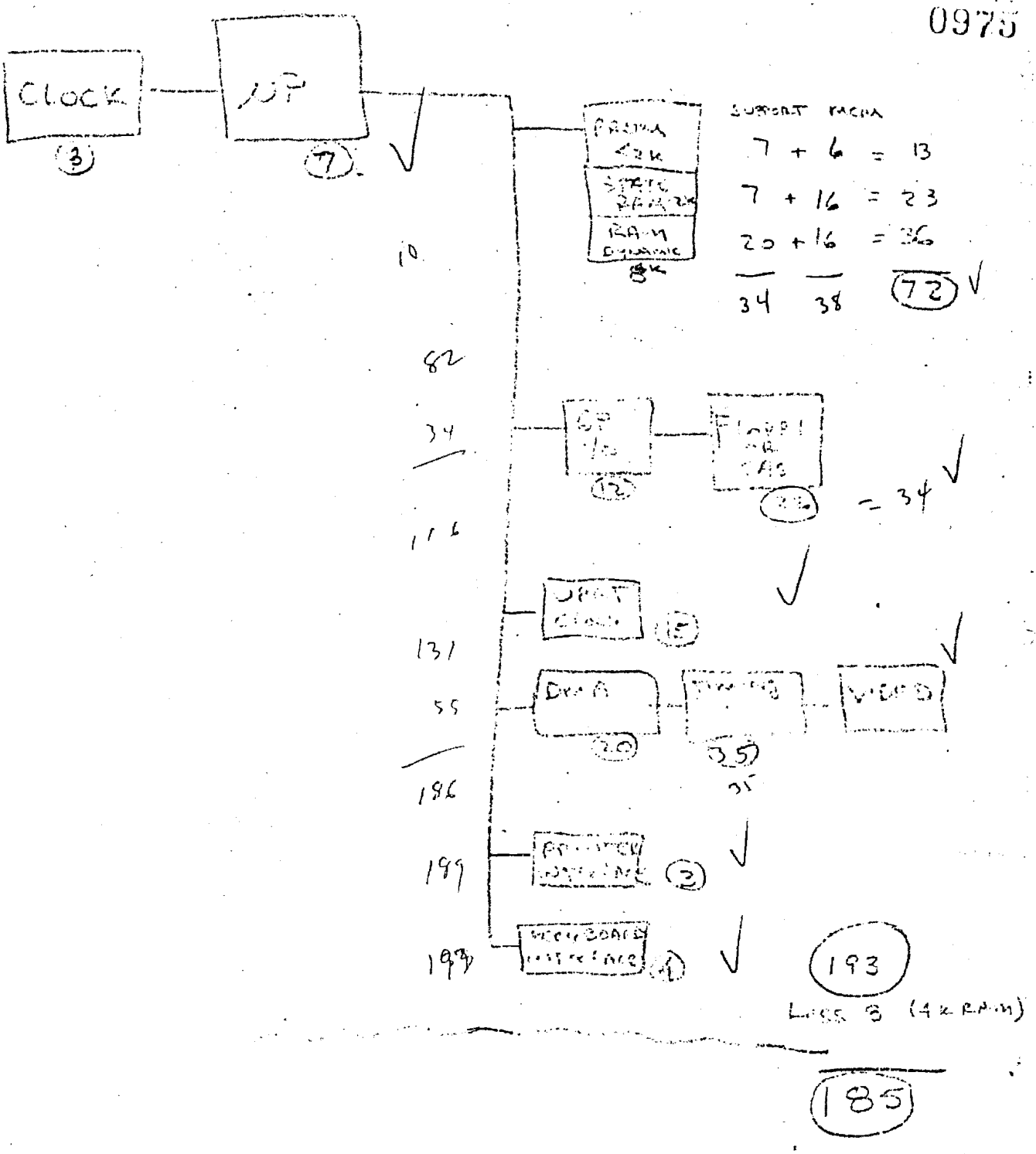


NOTE: ALL CHIPS CONSIDERED TO BE EQUAL SIZE.

VT51

Component	Prototype Computer System (8080)		VT51 0976 (Home-maid μP)	
clock and processor		10		59
microprogram memory - rom			2+8 (1K)	10
The - processor		10		6
static ram	7 + 16 (2K)	23	5+16(2K)	21
prom / rom	7 + 6 (2K)	13	8 (4K)	8
Dynamic ram.	20 + 16 (8K)	36		—
Total - $P+M_p$		82		98
Floppy or Cassette interface		34		19
UART to comm.		15		13
Video		55		24
Printer interface		3		5
Keyboard "		4		0
		193		159
Total.				
less Dynamic ram		36		
less display complexity		25		
adjusted Total.		132		159
EIA Interface				4
Modem Support				2
Keyboard LEDs				2
Parallel interface				9
Expandable Mem.				1
Misc				9
				186

GB
12/74


Clock
3
7
10
82
34
116
131
55
186
199
198
SUPPORT MACHA
7 + 6 = 13
7 + 16 = 23
20 + 16 = 36
34 38 72
= 34
193
185

PCS

December 17, 1974

W. Leighton Collins
Manager, Resident Fellow Program
American Society for Engineering Education
Suite 400
One Dupont Circle
Washington, D.C. 20036

Dear Mr. Collins:

I'm sorry, but we will not be able to participate this next year. Please try us the year after.

Sincerely,

Gordon Bell
Vice President
Office of Development

GB:mjk

DIGITAL EQUIPMENT CORPORATION, 146 MAIN STREET, MAYNARD, MASSACHUSETTS 01754
(617)897-5111 TWX: 710-347-0212 TELEX: 94-8457

(202) 293-7080

American Society for Engineering Education **suite 400**
one dupont circle, washington, d.c. 20036

0978

DEC 13 1974

December 9, 1974

Dear Mr. ~~—~~
Sorry, we will not participate this year. Please try us next year.

Mr. Gordon Bell
Vice President, Engineering
Digital Equipment Corporation
146 Main Street
Maynard, Massachusetts 01754

Dear Mr. Bell:

Your company is again invited to participate in the Resident Fellow Program of the American Society for Engineering Education. The Program is familiar to you but there are several changes this year that you should know about.

Most significant is the broadening of eligibility to give you a greater choice of the "kind of man" you want to employ. This has been accomplished by including faculties of engineering technology as well as of engineering, by removing the forty-year age limit and by eliminating the Ph.D. degree requirement. Major emphasis, of course, still is on giving the young faculty member an opportunity for experience in the decision making, problem solving and cost conscious world of the practice of the engineering profession--in industry, private practice or government. It also should be mentioned that the Program is now entirely self-supporting. According to plan, Ford Foundation funds are no longer available to defray any costs involved and the employer consequently pays ASEE $2,000 per Resident to defray administrative costs.

Participation in the Resident Fellow Program gives you an opportunity to employ a highly competent and motivated engineer, to improve college-industry relations, and to have an influence on the kind of education given to engineering students. The enclosed brochure gives the details. Please read it carefully and then inform me of your interests. Nominations are now being readied for screening and when the task is completed, I will send you, upon request, a brief resume of all candidates and a more detailed biographical sketch of those that seem particularly suited to your needs.

I hope you will respond favorably and I'll do my best to answer any questions you might have. If, perchance, you no longer are the individual to whom this letter should have been directed, please forward it and inform me of the individual's name and title.

Sincerely,

W. Leighton Collins

W. Leighton Collins
Manager, Resident Fellow Program

Enclosure

SUBJ: PDP-14

DATE: 12-17-74
FROM: GORDON BELL

* *
PLEASESEND TO: FILE
* *

SUBJ: PDP-14 PERFORMANCE AND FUTURE DIRECTION

To: OC
Don Chace
Bob Savell
Brad Vachon

The ROI on the PDP-14 from 70 to 74, and also for 75 as we are projecting, is 11% and 19.5%. The ROI is much less than we are expecting and getting. Our standard products including systems with combined hardware/software systems are anywhere from 25% to several hundred % on disks and memories. We spent $2.5M on it for engineering--less than the amount for our RSX series operating systems, which IPG successfully markets and always needs more capabilities in! My guess, if you can get the Field Service factored in, the results will be really abysmal.

GB:mjk

Attachment

ROI - PRESENT VALUE TABLE

0980

FACTOR	EXPENSES ACTUAL	EXPENSES PR VAL	REVENUES ACTUAL	REVENUES PR VAL
= 1.00000	= 1031.0	= 1031.0	= 0.0	= 0.0
= 0.95648	= 0.0	= 0.0	= 0.0	= 0.0
= 0.91486	= 0.0	= 0.0	= 629.0	= 575.5
= 0.87504	= 0.0	= 0.0	= 0.0	= 0.0
= 0.83696	= 1385.0	= 1159.2	= 0.0	= 0.0
= 0.80054	= 0.0	= 0.0	= 0.0	= 0.0
= 0.76570	= 0.0	= 0.0	= 1120.0	= 857.6
= 0.73237	= 0.0	= 0.0	= 0.0	= 0.0
= 0.70050	= 2167.0	= 1518.0	= 0.0	= 0.0
= 0.67002	= 0.0	= 0.0	= 0.0	= 0.0
= 0.64086	= 0.0	= 0.0	= 2571.0	= 1647.7
= 0.61297	= 0.0	= 0.0	= 0.0	= 0.0
= 0.58629	= 2741.0	= 1607.0	= 0.0	= 0.0
= 0.56078	= 0.0	= 0.0	= 0.0	= 0.0
= 0.53637	= 0.0	= 0.0	= 3142.0	= 1685.3
= 0.51303	= 0.0	= 0.0	= 0.0	= 0.0
= 0.49070	= 4127.0	= 2025.1	= 0.0	= 0.0
= 0.46925	= 0.0	= 0.0	= 0.0	= 0.0
= 0.44892	= 0.0	= 0.0	= 4865.0	= 2184.0
= 0.42936	= 0.0	= 0.0	= 0.0	= 0.0
= 0.41070	= 6470.0	= 2657.2	= 0.0	= 0.0
= 0.39282	= 0.0	= 0.0	= 0.0	= 0.0
= 0.37573	= 0.0	= 0.0	= 9119.0	= 3050.5
= 0.35938	= 0.0	= 0.0	= 0.0	= 0.0
	= 17921.0	= 9985.9	= 20446.0	= 9985.9

URN ON INVESTMENT = 19.5%

John Hughes
12/14/74

ROI - PRESENT VALUE TABLE

QTR	FACTOR	EXPENSES ACTUAL	EXPENSES PR VAL	REVENUES ACTUAL	REVENUES PR VAL
= 1	= 1.00000	= 1031.0	= 1031.0	= 0.0	= 0.0
= 2	= 0.97438	= 0.0	= 0.0	= 0.0	= 0.0
= 3	= 0.94941	= 0.0	= 0.0	= 629.0	= 597.2
= 4	= 0.92508	= 0.0	= 0.0	= 0.0	= 0.0
= 1	= 0.90137	= 1385.0	= 1248.4	= 0.0	= 0.0
= 2	= 0.87827	= 0.0	= 0.0	= 0.0	= 0.0
= 3	= 0.85577	= 0.0	= 0.0	= 1120.0	= 958.5
= 4	= 0.83384	= 0.0	= 0.0	= 0.0	= 0.0
= 1	= 0.81247	= 2167.0	= 1760.6	= 0.0	= 0.0
= 2	= 0.79165	= 0.0	= 0.0	= 0.0	= 0.0
= 3	= 0.77136	= 0.0	= 0.0	= 2571.0	= 1983.2
= 4	= 0.75160	= 0.0	= 0.0	= 0.0	= 0.0
= 1	= 0.73234	= 2741.0	= 2007.3	= 0.0	= 0.0
= 2	= 0.71357	= 0.0	= 0.0	= 0.0	= 0.0
= 3	= 0.69528	= 0.0	= 0.0	= 3142.0	= 2184.6
= 4	= 0.67747	= 0.0	= 0.0	= 0.0	= 0.0
= 1	= 0.66011	= 4127.0	= 2724.3	= 0.0	= 0.0
= 2	= 0.64319	= 0.0	= 0.0	= 0.0	= 0.0
= 3	= 0.62671	= 0.0	= 0.0	= 4865.0	= 3048.9
= 4	= 0.61065	= 0.0	= 0.0	= 0.0	= 0.0
		= 11451.0	= 8763.2	= 12327.0	= 8761.4

RETURN ON INVESTMENT = 11.0%

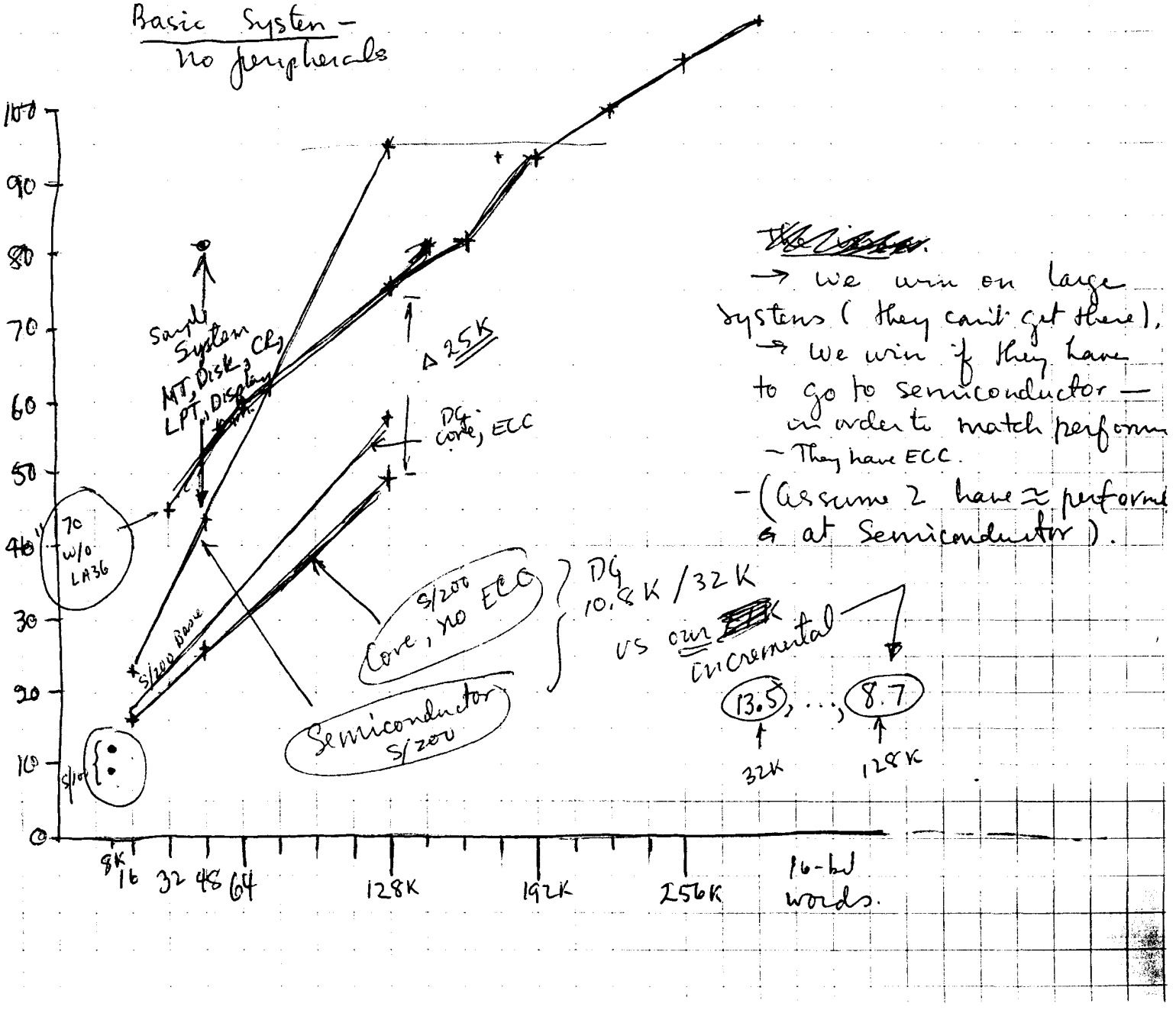
John Hughes
12/14/74

0982

Subject: Eclipse vs 11/20

To: Demmer, Clayton, McBride, Carnes, Fisher, Lemaire, Misaleh
~~MKT~~ MKT. Committee, Marcus, Long, Jacobs, Vachon, Kramer.

From: G Bell, 12/17/75



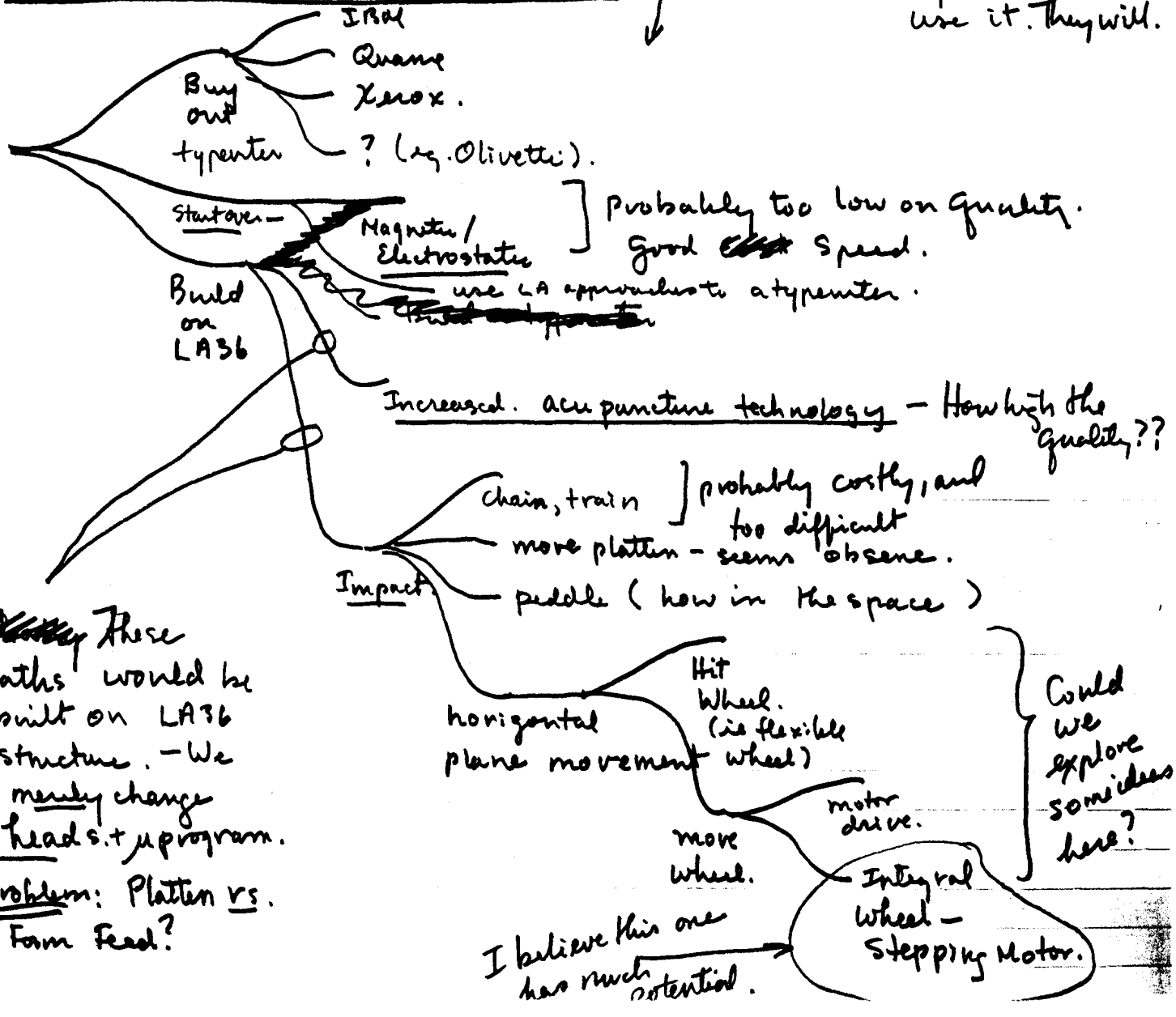
→ We win on large systems (they can't get there).
→ We win if they have to go to semiconductor — in order to match performance
– They have ECC.
– (Assume 2 have ≈ performance at Semiconductor).

Subject: High Quality Printing

To: Ed Cornell, Bob Putter, Al Hoffner. 15 Dec. 1974.
cc: K. Olsen, S Olsen, J. Gilmore Fm: gBell.

Within the next 2 years, there will be increased emphasis on getting a very high quality printer (ie typewriter). Let's outline how we're going to have the basis to make this decision. Stan (Jack Gilmore) is really pushing at word processing, for example. We could just wait for a clever typewriter co. (eg. Olivetti) to build a great, low cost typewriter — and use it. They will.

I see the space of alternatives:



These paths would be built on LA36 structure. — We merely change heads & μprogram.

Problem: Platten vs. Form Feed?

digital

December 17, 1974

Professor W. L. van der Poel
University of Technology of Delft,
Department of Mathematics
Julianalaan 132, Delft
The Netherlands

Dear Professor Van Der Poel:

I just received the letter of appointment for the editorship of the IFIPs Conference on Minicomputer Software. Please correct your files to read Dr. James R. Bell (DEC) and C. Gordon Bell (DEC and Carnegie-Mellon University)--coeditors. This is in accordance with my original agreement with Bill Wulf.

Jim will be attending the conference, and we will edit the proceedings together. It would be helpful if you could send ideas about what you expect of us as editors and deadlines. Also, I don't have a copy of the proceedings you edited, but would like a copy if you could send one, as it would be helpful as to standards (and I would like to read the material).

It would be helpful if you could put us in contact with the editor at the publisher, and indicate various dates, etc. I look forward to a successful conference and proceedings.

Sincerely,

Gordon Bell

Gordon Bell mjk
Vice President, Office of Development
Professor, Computer Science
Carnegie-Mellon University (on leave)

CGB:mjk

cc: Jim Bell
Bill Wulf
P. G. Hibbard

DIGITAL EQUIPMENT CORPORATION, 146 MAIN STREET, MAYNARD, MASSACHUSETTS 01754
(617)897-5111 TWX: 710-347-0212 TELEX: 94-8457

Copy to MJ

TWX 23763

0985

Dr. P. G. Hibbard

DEPARTMENT OF COMPUTATIONAL AND STATISTICAL SCIENCE
VICTORIA BUILDING BROWNLOW HILL
P.O. BOX 147 LIVERPOOL L69 3BX

TEL: 051 – 709 - 6022 EXT.

The University of Liverpool

and resend letters

PGH/JOC

26th November 1974

Professor C. G. Bell,
Department of Computer Science,
Carnegie-Mellon University,
Schenley Park,
Pittsburgh 15213,
U.S.A.

~~Please correct~~
Received Letter of 26 NOV.
Please correct
editorship to: ~~read~~:
Co-EDITORS: JAMES R. BELL AND Gordon Bell,

Dear Professor Bell,

On behalf of the Organising Committee of the Working Conference on Software for Minicomputers, may I thank you for accepting the editorship of the conference proceedings.

As you may know, the official IFIP publisher is North Holland, and I have written to Tom Steel, Chairman of IFIP Technical Committee 2, asking him to put you in touch with them. If you have any questions about this conference, please let me know, though questions specific to the editorship are best directed to Bill van der Poel, who edited the Trondheim Conference proceedings on Machine-Oriented Higher-Level Languages last year, and who is on the Organising Committee of this conference. His address is:

Professor W. L. van der Poel,
University of Technology of Delft,
Department of Mathematics,
Julianalaan 132,
Delft,
The Netherlands.

I enclose the circular which has just been sent to the invitees. I will be writing to the members of the organising committee shortly, and I will send you a copy of that letter. I will also send you copies of all future communications between organising committee members.

Yours sincerely,

Peter Hibbard

Digital Equip Corp

Re Digital Equip Corp Carnegie-Mellon U AND Digital Equip Corp

Dear

A schedule would be helpful.

~~Please send~~ ack other letter

JIM ~~JAMES~~ will be attending, I

IST

accordance with my original agreement with Bob Wolf.

Dear Professor Van Der Poel

I just received the letter-aeeepting- of appointment for the editorship of the IFIPs Conference on Minicomputer Software. Please correct your fils files to read, Dr James R Bell (and C Gordon Bell HJ James R Bell (DEC) and C Gordong Bell (DEC and Carnegie Mellon U). co-editors. James Jim will be attending the conference, and we will edit the proceedigns together. It would be helpful if you could send ideas about what you expedct of us as editors and deadlines. I g It w seems like the Also, I don't have a copy of the proceedings y-u edited, but would like to Could you send a copy ? as it would be helpful as to standards (and I would like to read the materil).

~~Also, what do~~

~~Also, I would like~~

It would be helpful if you could ~~tell us who contact the publisher~~ put us in contact with the editor at the publisher, and indicate various, dates, etc. I look forward to a successful conference and proceedings.

This is an

C.C: Wulf,
James Bell.
Hibbard.

OT
ITT 12 17 1538+
DIGITAL MAYN A
851627095";
UNIVERSITY LPL
DIGITAL MAYN A

0986

0078 1410 17-DEC 18081 1219 17-DEC
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23763
MSG NO NA10

TO: UNIVERSITY OF LIVERPOOL
     ATTN: DR. P.G. HIBBARD
     TELEX NO. 23763 LIVERPOOL ENGLAND

RECEIVED LETTER OF 26 NOVEMBER. PLEASE CORRECT EDITORSHIP
AND RESEND LETTERS TO:

CO-EDITORS

JAMES R BELL
DIGITAL EQUIPMENT CORPORATION

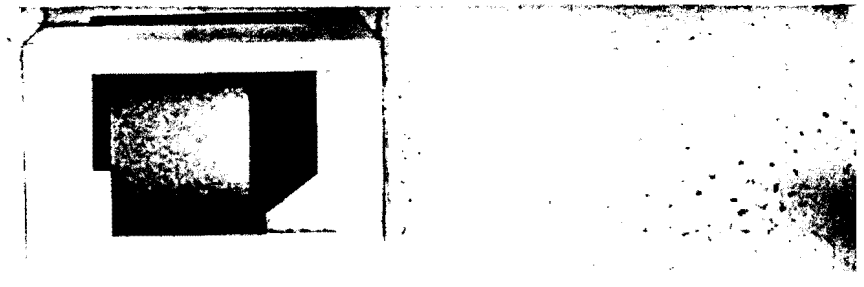
GORDON BELL
CARNAGIE MELLON UNIV AND DIGITAL EQUIPMENT CORPORATION.

JIM WILL BE ATTENDING. I WON'T AS I INDICATED TO BILL WOLF.
A SCHEDULE WOULD BE HELPFUL.

FROM: GORDON BELL - DIGITAL MAYNARD

REGARDS
JG
NNNN
+

UNIVERSITY LPL.....
12/17/74 1541EST 002.4



SUBJ: ARPA PROPOSAL

DATE: 12-19-74
FROM: GORDON BELL

* *
PLEASESEND TO: FILE
* *

SUBJ: A SECOND REQUEST FROM ARPA FOR RESEARCH ON 3 TOPICS

To: OOD
I got a call today from Craig Fields of ARPA, relative to a research proposal. They didn't like our draft proposal on the terminals, because it wasn't aligned with what they wanted. They would like any/all of the following before Jan 15.

1. A really good, scan-graphic display to be used as the front end to their office automation/data-base systems. It must be better than a GT40. It would drive a standard monitor, and possibly go to 1000 lines or color. They would like a bit memory map plus various generators to get the vectors and arbitrary characters. I hope Len Haile would put this proposal together (if interested), coordinating the various ideas and people (within Stocky's group and CSS). They would like to be able to get subsequent copies if we get anything interesting. They believe this would cost 100 to 110K.

2. Low cost PDP-10 with pager, and 1-megabit of memory and a swapper. They would pay about 250K for this research. This would be a single researcher's personal 10. Certainly double as a single breadboard.

3. High Speed IMP. They would like to get a commercial system similar to the one BBN developed for packet message switching. We would develop the hardware and software. Ideally, we would be able to get some assistance from BBN in the way of consulting etc.

I don't really know how this one should be handled. We have to have such a product eventually. Any ideas who would propose and run this?

The proposal format details can be answered by Gene Stubbs, ARPA business manager, who Tom Siekman should call to get the information on how to go about this and what the restrictions

SUBJ: ARPA PROPOSAL

DATE: 12-19-74
FROM: GORDON BELL

are.

The proposal format:

1. 1 page work statement--what we will do.

2. Details of the project, what avenues we intend to explore, milestones, approach, etc.

3. Budget

Jim Bell should probably coordinate this effort to present a consistent message. Call us if interested.

GB:mlk

cc: Jim Bell
Bruce Delagi
Len Hallo
Julius Marcus
Rick Merrill
Mark Sebern
Tom Stockebrand
Nat Telchholtz

digital INTEROFFICE MEMORANDUM

TO: John Leng

CC: Julius Marcus
Larry Portner
Nat Teichholtz

DATE: December 20, 1974

FROM: Gordon Bell

DEPT: OOD

EXT: 2236 LOC: ML12/A51

SUBJ: COMMUNICATIONS/NETWORKS

Regarding the communications/network systems products dilemma. Can we explore how DAS-10 might take on central development in this area? You have the most capability for products. How can you supply these to the corporation too?

How do we explore?

GB:mjk

SUBJ: LSI SEMINAR

DATE: 12-20-74
FROM: GORDON BELL

* *
PLEASESEND TO: FILE
* *

SUBJ:

To: Lorrin Gale
Tony Bryan
(and LSI GROUP)

cc: Dick Clayton
Bob Puffer

Since I'm habitually laudatory and supportive of your effort, let me take this special opportunity to state that I believe the LSI seminar came off really well. I hope the line users benefited from it as much as I did. The insights at all engineering levels into past, present, and future are essential to our future.

The book has much hard data and analytic methodology that I hope will filter into our standards and products. The model of what technology to use versus size, etc, for ROI is almost worth pushing to a standard program for engineering.

I hope you'll use the Engineering News to communicate some of the tidbits, and I look forward to book and quarterly updates.

GB:mjk

SUBJ: ARCHITECTURAL POSITION

DATE: 12-20-74
FROM: GORDON BELL

* *
PLEASESEND TO: FILE
* *

SUBJ:

COMPANY CONFIDENTIAL

To: Distribution

I had great hopes for the staff architectural position in terms of being able to provide focus, leadership alternatives, and perspective in terms of:

0. Structures which are competitive--we are currently in the corner looking at our navel, MODCOMP, now DG, and HP are beating us and already beat our new machines.

1. The necessary enhancements for a VAX at high end;

2. The VAX at low end.

3. The I/O mapping and context switching problem. Everyone has reasonable solutions now here--HP 21MX, MODCOMP and DG.

4. The basis for a 32-bit 11 so it could be compared with a 10, any other internal better alternatives, and most important-- the competition. The Rolls Royce benchmark certainly indicates a big hole in what we're doing. I want each one of us to understand why!

5. The ASCII console. All that's happened by having a standard, is that it licensed and suggested more ways to do things than a single engineering group would probably have done. The only 2 instances I know of Q and A both appear different to me.

Schedule of how we're going to get at some of the hard techincal competitors but failing that, get my expectations in line with what is happening or the advertising program to cover the deficiencies.

GB:mjk

SUBJ: ARCHITECTURAL POSITION

DATE: 12-20-74
FROM: GORDON BELL

Distribution

Jega Arulpragasam
Dick Clayton
Bruce Delagi
Bill Demmer
Robin Frith
Bill McBride
Dave Nelson
Bill Strecker
Steve Teicher

CC: Bob Armstrong (re 21MX)
Kaman and O'Loughlin (re DG + MODCOMP)

SUBJ: COMM CONTROLLER

DATE: 12-20-74
FROM: GORDON BELL

* *
PLEASESEND TO: FILE
* *

SUBJ: THE COMM CONTROLLER ON-A-BOARD AND THE CHIP-SET FOR HIGH PERFORMANCE CONTROLLERS.

To: Distribution

Regarding our discussions this last week, I understood:

1. Vince agreed to have a common microprogrammed controller board(s) for 2 new options. Even going from 2 to 1, I believe this is significantly understaffed in terms of experienced people to design, assemble, simulate, document, and build testers. I.e., it seems to me to be headed for disaster. (This board is more complex than many of our processors, and the currently assigned individual seems like the wrong person to do this.)

2. I don't know what's happening vis a vis controllers on PK06, etc.

3. LSI engineering is trying to define chips which can, in principle do communications controllers and disk controllers. They won't be ready at this time, and since they don't have a real product to go into now, it may not be useful anywhere!

4. LSI engineering has resources which can solve 1 and 2 now.

Since there's a proposal coming from LSI engineering soon, I hope some of these concerns (fears) will be addressed...i.e. educate me and tell me how great things are going to be.

GB:mjk

Distribution

Vince Bastiani
Lorrin Gale
John Hughes

SUBJ: COMM CONTROLLER

DATE: 12-20-74
FROM: GORDON BELL

CC: Dick Clayton
Julius Marcus
Bob Puffer
Grant Saviers

SUBJ: MINUTES/AGENDA FOR OOD

DATE: 12-20-74
FROM: GORDON BELL

* *
PLEASESEND TO: FILE
* *

SUBJ: OOD STAFF MEETING MINUTES--December 19, 1974

To: OOD
Brian Croxen
Julius Marcus
Henry Lemaire
Len Halio
Win Hindle
Bill Thompson

ACTION ITEMS ARE ***'d!

1. We discussed the extra hour plan. Each VP will distribute to their own managers.

2. *Budgets--problems in RS03/4 area, 11/55. Vince and Tom to come back with plans.

   Q2 data due beginning of second week in December. MIP will not be on Q2 results from plants. Thus the computer reports don't reflect the last month, but rather a float of one month.

   *Dick is trying to get this budget on for the year. It's currently projected to be 300K over. Dick will work his test equipment issue for 11/70 with Phil.

   Rules for testors: we are moving to have manufacturing pay for all testors beyond the prototype in peripherals as in CPU's and memories.

   *Phil will reissue the policy, call attention, and there will be inconsistencies until next year.

   *Memories will be 60K (MOS) and 130K (core) under for original budget, but over by 100K on new budget. Brian will come back with a plan for core.

SUBJ: MINUTES/AGENDA FOR 000 DATE: 12-20-74
FROM: GORDON BELL

Current estimated overrun: 100K core, 100K DECUS, displays 300K, COMM 50K+ and 100K+ for computers. Printer is somewhat over.

3. Plans for next year as/Lander is constant next year.

WE MUST SELL OUR BUDGET PLANS BETTER!!

4. Otis Courtney came and described the EEO audits which are forthcoming.

5. *We discussed the Marketing Committee/Products Committee merger possibility with Bill Thompson. Bill and Larry are going to propose a system of planning, marketing, product integration. 000 will attend on 1.

6. *PSG's--Bill Thompson will attempt to get an audit of the Marketing Committee and PL Managers.

7. Graphics (Hallo, Ashton, Kramer, Hindle)--by centralization, we hope to improve the visibility of graphics and hence increase the use, beginning FY76. This would focus on proper allocation and sales, relative to other products. The graphics group would stay in LDP.
*The graphics group will come back with a proposal.

ARPA--

1. *Graphics--Hallo will propose.
2. PDP-10--Bruce and Dick will study
3. IMP's--Gordon and Julius will study problem

*Gordon (and subsequently Jim Bell) will collect the data.

December 26 meeting agenda:
12:00 to 1:30
---

0. Bob Puffer--please assume the chairmanship.

1. Memories will come back re 100K overrun. Croxon, Lemaire

2. COMM budget review; displays probably will not be back.

3. Clayton will discuss his alternatives for meeting budget.

GB:mjk

December 28, 1974

Myron B. Gilbert
The Boylston, Apt. 8C
Prudential Center
Boston, Mass. 02199

Dear Mr. Gilbert:

I've sent your vitae to John Jones, who heads our Public Relations effort.

Sincerely,

Gordon Bell

Gordon Bell
Vice President
Office of Development

GB:mjk

cc: John Jones

DIGITAL EQUIPMENT CORPORATION, 146 MAIN STREET, MAYNARD, MASSACHUSETTS 01754
(617)897-5111 TWX: 710-347-0212 TELEX: 94-8457

0999

December 28, 1974

Mr. Wayne M. Roney, Jr.
c/o W. A. Swayze
4120 Auburn Drive
Royal Oak, Michigan 48072

Dear Mr. Roney:

Thanks for the interest in Digital; however, we aren't hiring at this time. Also, we in general are not searching for people with a highly theoretical and research background in physics.

Sincerely,

Gordon Bell

Gordon Bell
Vice President
Office of Development

GB:mjk

DIGITAL EQUIPMENT CORPORATION, 146 MAIN STREET, MAYNARD, MASSACHUSETTS 01754
(617)897-5111 TWX: 710-347-0212 TELEX: 94-8457

R E S U M É

WAYNE MASON RONEY, JUNIOR
Born: May 27, 1943
Married, one child

Education

University of Oregon (1961-1965) B.A. (Physics)
University of Wisconsin (1965-1966) M.A.(Physics)
University of Wisconsin (1966-1971) Ph.D.(Physics)

Thesis Title: 'Magnetic Moments of Excited States of Odd-A Nuclei'

Jobs

Teaching Assistant for first year physics lab/ discussion sections at the Univ. of Wis. (1965-66)
Research Assistant at the Univ. of Wisconsin (1966-71)
B.N.D.E. Fellow at the Univ. de São Paulo(1971-75)

Publications

G-factors of Core Excited States Near A=100
W.M.Roney, H.W.Kugel, G.M. Heestand, R.R. Borchers and Rafael Kalish in Nuclear Reactions Induced by Heavy Ions. Ed. by R. Bock and W.R. Hering (North-Holland Publishing Company Amsterdam 1970) p.419

IMPAC Measurements on Levels of ^{125}Te,
W.M. Roney and R.R. Borchers, in Hyperfine Interactions in Excited Nuclei. Ed. by G.Goldring and R. Kalish (Gordon and Breach Science Publishers 1971) Vol. 4, p.1182.

Time Dependent Angular Correlation Measurements of the First 2^+ State of ^{150}Sm Recoiling into Vacuum, T. Polga, W.M. Roney, H.W. Kugel and R.R. Borchers, in Hyperfine Interactions in Nuclei, Ed. by G. Goldring and R. Kalish (Gordon and Breach Science Publishers 1971) Vol. 3, p.961.

Gyromagnetic Ratios of Excited States in ^{123,125}Te . W.M. Roney, D.W. Gebbie and R.R. Borchers to be published in Nuclear Physics

Advanced Courses

Taught

'Hyperfine Interactions' A one semester graduate level course to give a general picture of the subject from the point of view of nuclear physics and with more emphasis on perturbed angular correlations.

'Statistical Methods for Physicists' A one semester course for seniors and graduate students. The main topics were Parameter Estimation ('Maximum Likely-hood' and 'Minimum Chi Squared'), Error Estimates including correlated parameters, and Prediction Analysis.

References

Robert R. Borchers (Major Adviser)
Physical Sciences Laboratory
P.O. Box 6
Stoughton, Wis. 53589

Oscar Sala
Instituto de Física
Universidade de São Paulo
C.P. 8219
São Paulo, S.P., Brazil

Trentino Polga
Instituto de Física
Universidade de São Paulo
C.P. 8219
São Paulo, S.P. Brazil

Position: I hold a fellowship sponsered by a governmental agency (Banco Nacional do Desenvolvimento Econômico) which requires that the recipients teach as well as do their research. However the Physics Institute treats my position as equal to their equivalent of assistant professor, and I am currently the major professor of one student.

Current Responsibilities: i) Chief of a group of 7 people working on general gamma-ray spectroscopy, and hyperfine interaction measured by perturbed gamma-ray angular correlations. (This item needs clarification since as far as I know my situation is rare. The Brazilian members of the group had never participated in the type of experiments that we are doing, and the other PhD in the group is overburdened with administration even by local standards. Thus I became responsible for nearly all phases of the experiments from making the vacuum in the chamber to analyzing the data) ii) Teaching a one semester course on hyperfine interactions, iii) Responsibility for the electronic modules of the accelerator and supervision of repairs of the beam transport system.

Previous Responsibilities and Projects (at the Univ. de São Paulo):

i) Initial testing of all the electronic modules for the laboratory, and some of the initial repairs due to a lack of personnel in the electronic shop at the time.

ii) Assistance for the National Electrostatic Corporation representatives during the initial installation and testing of the prototype Pelletron accelerator system. Primarily working with electrical and electronic components, but a reasonable share of the time spent on the preparation of the single stage injector (4U) and its ion source for the acceptance test.

iii) Implementation of computer programs for data analysis including: programs which I wrote for our specific needs, several general purpose programs for least square fits to linear and non-linear functions, and published programs e.g. the COULEX program of de Boer and Winther.

iv) Supervision and installation of the beam transport system between the NEC supplied equipment and the vacuum chamber of the angular correlation system. Design, and optical alignment of the detector supports.

Approximately 20 months after we had arrived I was asked to stay on at the institute. At that time the Pelletron had not passed the original acceptance test, however it seemed that the accelerator would function normally during the 2 years for which I agreed to stay on. This decision has not turned out well due to unforeseen problems which were aggravated by the level of Brazilian industrial development which is insufficient to support such an accelerator. In the 2 years since my decision, our group has had 4 useful days of machine time. Although we have succeeded in verifying the optical alignment of the system, it is doubtful that we can produce very much useful data in the short time remaining.

Note on Computer Programming Skills

Besides a thorough knowledge of Fortran G, I have had a course in assembly language programming (for the CDC 1600/3600 computers) which I presume would allow me to learn more easily how to program on small computers in lower level languages. In addition my knowledge of numerical analysis is approximately the level required in 1970 for a Masters degree in Computing at the University of Wisconsin.

December 28, 1974

Thomas H. Dunigan, Jr.
Department of Computer Science
University of North Carolina at Chapel Hill
New West Hall
Chapel Hill, North Carolina 27514

Dear Mr. Dunigan:

Sorry, we don't have anything in this area. Rockwell, Bell Northern Research, and Fairchild have built such devices and are prototyping them on PDP-]]'s. I believe you'd be better off getting the possibilities from the literature and provide insight into how they should be organized.

Sincerely,

Gordon Bell

Gordon Bell mjk
Vice President, Engineering
Professor, Computer Science
Carnegie-Mellon University (on leave)

GB:mjk

DIGITAL EQUIPMENT CORPORATION, 146 MAIN STREET, MAYNARD, MASSACHUSETTS 01754
(617)897-5111 TWX: 710-347-0212 TELEX: 94-8457

UNIVERSITY OF NORTH CAROLINA AT CHAPEL HILL

Department of Computer Science

December 17, 1974

DEC 2[illegible]
12-30

Professor Bell:

On one of your visits here to UNC, I spoke briefly with you about my doctoral research in the area of electronic mass memory system design. You indicated that DEC had a prototype device in operation. I believe the underlying technology was magnetic bubbles. If such information is not proprietary, I would like to know the device characteristics of DEC's bubble device -- access time, data rate, capacity, logical and physical organization. Since the main thrust of my research is in system design, I would also appreciate any insight that DEC may have gained into the efficient utilization of such a device.

Thank you.

Sincerely,

Tom Dunigan

Thomas H. Dunigan, Jr.

[illegible] Chapel Hill, [illegible] Carolina 27514 Telephone 919-933-5698

digital INTEROFFICE MEMORANDUM

TO: Distribution

DATE: December 20, 1974

FROM: Gordon Bell/Al Bertocchi

DEPT:

EXT: LOC:

SUBJ: COMPUTATIONAL SERVICES FACILITY RELOCATION

We are relocating the Computational Services Facility (CS-2) to Parker Street to improve the operating environment and obtain the benefits of a consolidated facility with Corporate EDP. Ron Rutledge will manage the CS-2 facility during the move and subsequent to the relocation. He will now be directly reporting to Herb McCauley, Corporate Manager Information Services; however, he will continue to be responsible to Phil Tays for administration of the Engineering budget and Computational Services for the remainder of FY-75.

Jack Wuenschel will continue to manage the DEC Data Center, reporting to Herb.

mjk

digital INTEROFFICE MEMORANDUM

TO: Ed Corell
Phil Laut
Bob Puffer
Andy.

DATE: December 20, 1974

FROM: Gordon Bell

DEPT: OOD

EXT: 2236 LOC: ML12/A51

SUBJ: LA180

Please put together a "CRASH" plan on the LA180.

How much.

When.

How many?

with Andy, d[illegible] mem.

Ken would like to review ROI on it.

GB:mjk

PS

Just received Andy's memo.

INTEROFFICE MEMORANDUM CONFIDENTIAL

digital COMPONENTS GROUP

1010

TO: Gordon Bell ✓
CC: Ed Corell
Al Huefner

DATE: December 18, 1974
FROM: Andy Knowles
DEPT: Components Group
EXT: 6777 LOC: MR2-2

cc Bob + Phil re memo.

SUBJ: LA180

Of course we are missing a tremendous opportunity by not pushing the LA180 harder and faster. Given the product at the projected cost and reliability, we could give Centronics a really bad time. They are ripe - every customer of theirs is unhappy, etc.

In our business model for FY76 we looked at the following possibilities:

	Shipments (Units) Q1	Q2	Q3	Q4	T	Total NOR	Bookings
Worst Case	0	0	0	0		0	0
Most Probable	0		150	530	680	1,156K	1,700
Optimistic			150	1000	1150	1,955K	2,720

Certainly we could push this up a quarter or two. In our #'s we assume no factory shipments prior to Q3 FY76. In FY77 we are forecasting 9000 units shipped with a resulting NOR of 13,500K$!

If one weighed, say, the TS03 vs the LA180 from any business standpoint, one would first spend his limited $ on the LA180.

P.S. Note these are COMPONENTS #'s. Given the product sooner the corporate projections could be:

	FY76 DCG	OTHER	TOTAL	FY77 DCG	OTHER	TOTAL
Units LA180	3500	1400	4900	9000	2000	11,000
NOR$	5,950K	3,220K	9170	13,500K	4,200	17,700
AVG PRICE	1,700	2,300	1870	1500	2100	1,610

We might project the market for LA180 like line printers to be 40,000+ in FY77. The way we are going we most likely will not come close to the FY76 or FY77 #'s unless someone takes this product seriously.

Circulate to Staff

digital INTEROFFICE MEMORANDUM

Please return F 1011

TO: John Fisher

DATE: July 18, 1974

FROM: Phil Laut

LA180

DEPT: Engineering

EXT: 4308 LOC: 12-1

SUBJ: Summary of Items Approved at the Products Committee July 9, 1974

Increase to Semi-conductor Memory Engineering Budget - Approved

Approval was granted to increase the Semi-Conductor Memory Engineering budget by $150,000 in FY75 from $512,000 to $662,000. The purpose of this increase was to allow purchase and testing of 4K memory chips from additional vendors. The $150,000 comes from the unallocated portion of the Central Engineering which was $448,000 and is $338,000 after this change.

LA180 Business Plan - Approved

The LA180 is a 180 character per second printer with:

First ship date: September, 1975
Manufacturing cost: $600
Development cost: $500,000

Sales of $49,000,000 (about 60% by the Components Group)

A copy of the business plan is attached.

/ale
att

digital INTEROFFICE MEMORANDUM

1012

TO: Product's Committee
Product Line Manager's Committee
Al Huefner
John Wolaver

DATE: September 4, 1974

FROM: Ed Corell

DEPT: Printer Engineering

EXT: 2991 LOC: 1-3

SUBJ: LA180 Money Problems

I feel a word of explanation is needed now to let everyone know what has taken place in the last two weeks on the development program for the LA180. For reference, we have obtained approval from the Product's Committee and showed a schedule that provided for first shipments from Westfield to Westminster in August 75.

My cost center has experienced budget overruns during July and August due to two reasons. First, we have some overspending occurring on the LA36 and second, drafting has provided us with 30% increase in rates since the beginning of the fiscal year. This is only significant, since that is where our project is at the present time.

I have stopped all drafting and layout work on the LA180 for the remainder of the first quarter. I expect this to result in a first shipment from Westfield date of November 75.

/sj

To: Gordon Bell cc Puffer Corell
This is dumb! dumb! dumb!
This is a top priority project. Something else should suffer below it in priority
How do we get at it. (Like I mean TOXY can suffer! etc)
Andy Knowles
9-12-74

SCHEDULE: LA180 Printer

BY Dan Belanger
DATE Oct. 17, 1974

SH. 1

	FY:75						FY76								
	Q3			Q4			Q1			Q2			Q3		
	J	F	M	A	M	J	J	A	S	O	N	D	J	F	M
LA180 Build							100	ϕ	200	200	350	500	400	500	800
Material Schedule				300				200	350	500	400	500	800	880	1090
Cumulative Build							100	100	300	500	850	1350	2150	2950	3950
Customer Ship													500	900	1200
Inventory (Build–Ship)							100	100	300	500	850	1350	1650	2050	2750
Module Schedule					50	75	125	200	375	525	500*	680*	1040*	1060*	1300*
Print Head Schedule						100	ϕ	200	200	350	500*	500*	680*	880*	1000*

*Includes 20% field spares

1013

INTEROFFICE MEMORANDUM **CONFIDENTIAL** DIGITAL COMPONENTS GROUP

AK

1014

TO Bill Chalmers

DATE December 16, 1974

FROM John Wolaver

DEPT Peripherals

EXT 6079 LOC MR2-2

SUBJ Report on DataPoint/ICC Milgo Trip to Test LA180 Market

I. Data Point

Data Point	Digital
Victor Poor - U.P. R+D	Ed Corell
John Walker - V.P. Eng.	Nick Notias
	John Wolaver

DataPoint presently is buying 1000 Centronics 101 165 cps line printers a year. They are yet another unsatisfied Centronics customer, claiming arrogance and unwillingness to correct deficiencies in printer. Datapoint keeps my record intact of never finding a satisfied Centronics customer.

DataPoint had hoped when they heard about our rumored printer, the LA36, that it was, in fact, a Centronics replacement. They would be interested in buying the LA180 if it were available today. The LA180 specifications meet their needs, and its projected pricing is acceptable.

A possible strategy to pursue with DataPoint would be to promote their idea of using the new and lower priced Centronics 500 Series on a limited basis for key accounts over the next 12 months. In the meantime, we keep them apprised of LA180 developments and get them an evaluation unit as soon as possible.

II. ICC Milgo

ICC Milgo	Digital
Ted Scarpa - Marketing	John Wolaver
Judd Gilberts - Software	Charlie Wycoff

ICC Milgo is building a one-plus product to sell against Teletype's Model 40. They estimate their need for LA180's could go as high as 10,000 over the next 3 years. A total of a not insignificant 3000 seems more likely.

Competitors here are Teletype, G.E. and Okidata. G.E.'s pricing appears too high to be competitive. Teletype in the 80 column mechanism and associated electronics with Teletype defined interface

configuration is quite attractive:

Model 40 P101B	$1340 list
	1073 maximum discount
132 Column Option	250 - 350 extra

Okidata, a CRT copier, with their $700 quantity price looks like to most likely near term buy for ICC Milgo. Essentially the price is right to help ease their cash flow problems. As a product, all indications are it is a very low duty cycle printer (10 minutes continuous printing before the head gets too hot to print.)

Our strategy could be to encourage ICC Milgo to use Okidata as an interim product. Then come back with a highly reliable, full feature printer, the LA180.

JW/njo
xc: E. Corell
~~A. Knowles~~
A. Michels
N. Notias
C. Wycoff

digital INTEROFFICE MEMORANDUM

TO: ED CORELL

DATE: December 9, 1974

1016

cc: Bob Puffer
Howard Reed
Art Williams
Dan Belanger
LA180 Distribution
Ed Savage

FROM: Paul McGaunn

DEPT: Peripheral Mfg.

EXT: 366 LOC: WF

SUBJ: LA180 MANUFACTURING RECOMMITMENT

Westfield Manufacturing based upon present economic conditions and the need to dedicate all efforts to insuring FY75 DEC success hereby notify you and all concerned that our LA180 schedule is extended 3 months.

This in effect changes initial build from July 75 to October 75. All other commitments move accordingly.

We will not hire the projected needs of twenty-two (22) additional people in FY75 for this project.

Comments.

Paul
PAUL

TO: LA180 DISTRIBUTION

1017

Paul McGaunn - Westfield

Ed Corell - MA 1-3

Rene Jodoin - MA 5-1

Ed Czerwinski- Westfield

Vahram Erdekian- MA 1-3

Art Granfors - MA 1-4

Jim Koskinen - Westfield

Fred Cortazzo- MA 1-4

Al Huefner - MA 1-3

Art Williams - MA 1-3

Dan Belanger - Westfield

John Chernick - MA 1-3

W. Owens - Westfield

John Eyres - Ireland

Don Call - MA 1-4

Tony Mongillo MA PK 3-2

SUBJ: FUNDS FOR RESEARCH DATE: 01-07-75
FROM: GORDON BELL

* *
PLEASESEND TO: FILE
* *

SUBJ: WHY I WOULD LIKE TO INCREASE OUR RESEARCH AND TO GET OUTSIDE FUNDS FOR RESEARCH--draft

To: Distribution

In the past we have been unable to establish a research program which yields products sufficiently in advance of the general market. In general, I believe we need to improve our ability to accumulate, filter, process, and utilize technology and techniques (ideas) in our products! The odds of scheduling a product which has significant innovation is extremely small. Similarly, our development is quite obvious, as development managers are reluctant to use more than 1 new idea/product and that by definition in our business is new circuits or higher magnetic recoding density.
Therefore, I want to know how the new ideas are going to be developed before we commit them to a scheduled product.

I am not unhappy with the research group, however; as they have been effective as: consultants, teachers, general problem solvers, product generators, recruiters; and about 25% of their time they work on research of the type I'd like to increase. Our problem-rich environment is terribly seductive to the very people we want to do research, because the development groups tend to operate behind schedule and sub-state-of-the art. There is intense pressure to move people from research into development as the development areas suffer (see appendix 1 for examples).

Summary

I want to go outside for research funding to:

0. indirectly build substantially better products;

1. increase the amount of spending in research;

2. get our research calibrated with the outside and move our researchers more into this community;

3. get better access to outside ideas and outside people;

4. enhance recruiting;

5. do more prototypes before we produce (having time is the only way to accomplish this);

6. work on larger, longer term research projects;

7. avoid the short term pressures the research group has now--teaching, problem solving, staffing crisis projects.

In doing this:

8. give up ideas gained through the research to the source funder (usually the government).

1. make public the research;

2. give up flexibility to move research people to solve crisis problems.

Pros and Cons on Letting the Development Groups Do Their Own Research

---

In the past, I've advocated doing a significant amount of advanced work in the respective development groups. This has been done in the disk area, and I'm not aware of whether it has been successful or not--I don't recall any techniques, prototypes, etc. that have come from the effort.

Having the research distributed in the groups should:

1. Ease the problem of moving from advanced development (ideas) to prototype.

2. Educate the development people by having them exposed to people who read the technical literature.

Similarly, the researchers are in contact with real problems, the market, and people who read the trade literature.

Having the research more central should:

SUBJ: FUNDS FOR RESEARCH DATE: 01-07-75
FROM: GORDON BELL

1. Achieve better systems concepts and integration and give researchers a broader view by not being confined to a single group.

2. Permit a variety of research to be carried out both central, decentral, and in various universities.

3. Provide better management, since a development group manages products and their production introduction.

Funding Research At Universities

In general, I'm for this, but it's an independent issue, except that it competes with getting more money for research internally. As we decide that a research area is important, we should look at it similar to the way we calculate ROI for products. If the cost, benefits, etc. are right, then we do the work in the appropriate place. My own bias is that unless the work is done jointly, the likelihood of impact is so small as to preclude our doing it outside.

Why Externally Funded Research?

Fundamentally, I don't believe we're spending enough money in this area, and I don't see how to extract more from our currently overcommitted development budget--the obvious answer to cut development back seems to be impractical for what we've sold to our PL customers.

In general, research is a business like product development; the product is knowledge written--communicated in reports and papers--but the most important product of the research is the knowledge in the researcher's head. This knowledge is the basis for subsequent development--and if the research is properly timed, starting over with a product in mind, should provide the best products. We can see how research so far has effected our own products--ARPA has the most (see below).

Therefore, the most valuable part of research is usually the training of people on a particular idea, such that the next time through the implementation will be "done right." We could take the view of simply recruiting people who have done a product outside; and when we build something, simply go locate them; but the DEC acclimatization (decompression) process may be so great as to make this infeasible--I can't think of any recent examples.

Since research is competitive, in going outside for funding

SUBJ: FUNDS FOR RESEARCH DATE: 01-07-75
FROM: GORDON BELL

we can callibrate our own research in a competitive environment.

I believe we must do several things to widen our scope for products--as we get larger, it seems more difficult for us to assimilate new ideasquickly: networks, multiprocessors, microprogramming, microcontrollers, processor-on-a-chip, structured programming, high level language programming, etc. Therefore, the only solution is to get the ideas, and assimilate them in advance of the need.

Also, in entering this competition, it can tend to focus us along the direction that other research is going at the time. This is double edged: we're all blundering along together or by being separate, we may stumble onto something really unconventional (and with high payoff).

In being a member of the conventional research community, I believe our access to ideas, literature, and people will increase. We have been most successful recruiting at Carnegie-Mellon and U. of Mass.--in both cases we have joint research.

By taking on research projects per se, with the associated commitments, I believe we will carry our research much further and deeper, than we currently do. The pressure (including mine) on the research group is on solving short term problems: staff a position, make a measurement, etc.--and we want to keep much of this pressure. It is possible that we have swung too far.

Criteria for Research Projects

We probably have to get much more formal in our funding of our own research--i.e. we have to decide on a cost-benefit basis what to do.

Some criteria:

1. Cost. The proposer, size of project, likelihood of success, input dollars.

2. The payoff. How big is the market area? Does it affect all new systems, one market, all programming? Try to quantify.

3. Need--especially timing.

Why ARPA?

I've personally been associated with this community for some

SUBJ: FUNDS FOR RESEARCH DATE: 01-07-75
FROM: GORDON BELL

time and believe it is involved in research which we eventually require in our products. I would like for others within DEC to be exposed more directly to this community. Either directly or indirectly they have provided us with: timesharing techniques; a modern timesharing system--TENEX, on which to base a new system; various programs and languages--e.g. ALGOL, APL, BLISS, LISP, MUMPS, SOS, TECO; several computer-aided-design programs; the basis for the KL10; knowledge about networks together with use to form our own more limited network strategy; ideas in building our own GT40-series graphics processors; a microprogrammed box for the 11/40; and multiprocessor research which I believe will influence subsequent products. By not having the right processors for the ARPA-net construction, we missed a great product opportunity for communications products. We'll eventually have to invent this.

Other ideas coming from this community include: the circuits which DEC initially used, DECtape, the LINC, and displays.

How Do We Justify the Research to ARPA (and to ourselves)?
(Or How Does ARPA Justify Research to a Corporation)

For ARPA, the justification of funding us is probably easier than for the National Science Foundation (NSF). NSF exists both as a body responsible for the education of scientists and for research, hence there is a conflict. ARPA (presumably) only cares about research, hence, the instrument is immaterial--be it a university (e.g. CMU, MIT, Stanford), non-profit research (e.g. RAND), research-for-hire, profit making (e.g. BBN, SRI or SDC) or research part of a corporation (e.g. IBM, Xerox, TI).
ARPA also cares about the transfer of technology from research into applications--i.e. they are rated on how their research is applied. Also, once successful, they want the products

to be available for other government users.
I'd like to justify the research on:

1. We are interested in research for the sake of ideas that will eventually impact the way we do computing--i.e. products. We want to transfer research to products quickly.

2. We have utilized much of the ARPA research in the past, would like to in the future, and believe the contractor relationship would enhance this.

3. We believe we have a unique collection of people, skills, facilities to do research--particularly in building.

hardware/software systems.

4. We have not had a strong research program, even though we have supported various ARPA ties (e.g. MIT, CMU) but would like to; and hence, need money. With this view, we never have enough money.

5. The techniques we would propose would benefit the public--e.g. better terminals, the 10, the network.

6. We are seeking support where there is a high research component, an education component, and which there is a relatively high risk. Otherwise a project would be in a development state.

7. The knowledge we obtain will be made public.

The Proprietary Nature of Research

Each outside source of funds has a different criteria for exposing the information gained in the research. In general, all sources require publication of the ideas and even working drawings, provided they are funded. In cases of patents, the government wants royalty-free access to the ideas if they are used in products purchased by the government.

Right now, I don't believe these requirements are unreasonable. The only problem might be the accounting and assignment of ideas to costs as a product goes from research to development.

MIGRATION OF PEOPLE (AND IDEAS) FOR RESEARCH TO MEET PRODUCT DEMANDS--APPENDIX 1

Historically people have left research to solve crisis development problems:

1. Brender--structured code, programming tools and implementation languages--FORTRAN compilers and FORTRAN-Plus.

2. Wecker--multiprocessors and networks--communications protocol, design and network architect.

3. Kaman--computer architecture and microprogramming--teaching of microprocessor design, computer design of 43, PDQ.

4. Levy--computer modules, microprogramming and small systems--manage timesharing system for PDP-11.

SUBJ: FUNDS FOR RESEARCH

DATE: 01-07-75
FROM: GORDON BELL

;onsulting is quite healthy if held to 1/2 time.

'here is pressure to solve day-to-day problems as an alternative ıethod to direct project funding.

.. Turner's work on programs to analyze performance has been viewed as line development. Even now, there is little work in the line development groups. Only recently have projects staffed this function.

:. Strecker has carried on performance analysis for cache, instruction streams, and architecture. A significant educational effort was involved in selling the cache concept.

:. Ken King is just formulating research in office automation. Certainly one alternative is to work on "word processing"--a development problem--the pressure will no doubt form.

urrent Research

he current projects could yield significant results if carried o completion.

. Poonen--structured programming and compiler parse table generator. Hopefully, this will lead to easy generation of language front ends and be tested on a limited PL/1.

. Eckhouse--operating systems. Hopefully this will lead to a multiprocessor system we sell. We're 1-2 years late in doing the work, because without it, we can never build the appropriate hardware.

. Sebern--low cost terminals, system and interconnected computers.

. Kaman--microprocessor design for peripherals was carried out, but has been abandoned for work on PDQ.

. ?--small systems research. Interface to Teicher's group.

B:mjk

ttachment

istribution

SUBJ: FUNDS FOR RESEARCH

DATE: 01-07-75
FROM: GORDON BELL

OD
lm Bell
en Olsen
om Siekman
teve Telcher

APPENDIX 2

Analogy Product Development Evaluation Criteria

Nearly every product we design is the most successful (e.g. profit, performance, reliability) the second time through--provided the same people do it! The first one is a prototype, the third one we usually goof because we get too sure and the people disappear. Alternatively, a product is successful if it utilizes advanced technology and the market is ready to understand and accept it. (5-8; 8/s-new; 8/I,L,8/E,F,M, 8/A 4, 7, 9, 15 new people each time; 5, KA10, KI10, KL10, KA was same performance as 6) however; each new processor was a significant new design effort requiring much invention; 11/20-11/40; 11/45--external technology; 11/05--not sure why it has been so successful--smallest member of 11 family?, good and reliable?--by these criteria the 11/04 should be really successful. The 11/PDQ should be all right because of third time through and new technology. The 11/WD will hopefully be a technology windfall similar to the 11/45 (let's hope).

For peripherals, the current papertape equipment is second time design. The LA30-36 seems better already; will the RK06 be significantly better than the 05? All our fixed head disks have trained new people, and have been relatively difficult--likewise the tapes. The VT50 should be a breakthrough over the VT05 because Russ Doane, and Stan Olsen were involved in the VT05. The TU55 was the most cost effective of the 555 and TU56. Another criterion determining a successful product is that it cannot appear to be an orphan--standing alone. The buyer wants to believe that it will be made forever and have program enhancements, service, parts, etc....always available.

January 6, 1975

Charles H. Frye
Northwest Regional Educational Laboratory
Lindsay Building
710 S.W. Second Avenue
Portland, Oregon 97204

Dear Mr. Frye:

I was interested to read the status of PLANIT. I would like to go about getting a tape of PLANIT to run on some of our in-house DEC-system 10's, so that we can evaluate it. In order that we can get on with this, could you please send some more information so that we could look into how it could be made available to our customers. Who has such a copy?

There are three areas of interest:

1. The DECsystem 10 product line (sales to marketing of the -10)--Floyd Benson.

2. The Education product lines (currently sales are only minis)--Bob Trocchi.

3. As a general product for our minis as a language--Al Brown.

I'm circulating the documents you sent, but I would like more information as to the size, language definition, the conversion process, what the library is at this time, and your projection of PLANIT's use.

Sincerely,

Gordon Bell
Vice President
Office of Development

GB:mjk

cc: Floyd Benson
Al Brown
Bob Trocchi

MS - Letter - out 1028

Northwest Regional Educational Laboratory
Lindsay Building · 710 S.W. Second Avenue
Portland, Oregon 97204 · Telephone (503) 224-3650

DEC 28 1974

December 23, 1974

Mr. Gordon Bell
Vice President
Office of Development
Digital Equipment Corporation
146 Main Street
Maynard, Massachusetts 01754

Dear Mr. Bell:

Enclosed is some information regarding PLANIT which I hope you will find useful.

Both the University of Indiana at Indianapolis and the University of Oregon at Eugene are very interested in making PLANIT run on the PDP-10. U of I has already invested some effort in that direction.

About four years ago I had some discussions with DEC people regarding the installation of PLANIT on the PDP-10 but nothing materialized at that time. The three included a vice president, a systems man, and a salesman. Of the three, I only remember the name of the salesman, Al Beal. If it is of interest, I think I can retrieve the names of the others--at least the vice president. The only conclusion at that time was that the installation of PLANIT on the PDP-10 would present no particular problem.

If I can be of further help, please let me know. A PLANIT Users Group exists with a newsletter (published quarterly) available from Dr. Lyle B. Smith, SLAC, P.O. Box 4349, Stanford, California 94305. The price is $6/year.

Sincerely,

Charles H. Frye

Charles H. Frye

Enc.

January 8, 1975

John Whitney
600 Erskine Drive
Pacific Palisades
California 90272
Dear Mr. Whitney:

I received your letter of December 26. I've looked at the picture and the information you sent to Bob Trocchi.

I have no trouble at being intrigued, and I would like you to send any more ideas and the direction you are pursuing right now with computer graphics. I am certainly interested in this area and have used computer scopes for about the last 15 years. In fact, I probably made the first computer maps, which were used for displaying information about city densities and characteristics.

Unfortunately, I don't believe we have the money for patronage that IBM has, so all we can probably offer you is encouragement and if perhaps things look interesting some equipment or at least time on equipment.

I'm glad that you are in contact with Ivan Sutherland, and since he is at RAND now, he probably can get you access to equipment that would be useful in this effort. Since you also are based around Cal. Tech., it is probably worth calling another friend of mine, who has been active in computer graphics there, Ed Fredkin, who's a visiting professor there now.

Each year we think computer graphics is going to be important as a product, but so far the applications are quite limited. I'll be happy if you send more information, and I am sending the information I have received so far to Bill McBride, who is becoming the manager for our computer graphics area.

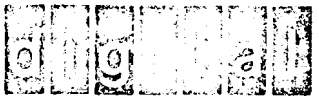
Sincerely,

Gordon Bell
Vice President
Office of Development

GB:mjk

cc: Bill McBride
Bob Trocchi

DIGITAL EQUIPMENT CORPORATION, 146 MAIN STREET, MAYNARD, MASSACHUSETTS 01754
(617)897-5111 TWX: 710-347-0212 TELEX: 94-8457



January 8, 1975

Mel Peisakoff
Director of Computing
University of California
Office of the President--Administration
2200 University Avenue
Berkeley, California 94720

Dear Prof. Peisakoff:

Keith Miles informed me that you had been made aware of a memo I wrote during your visit to DEC in September, and it was the cause of some embarrassment to you. The essence of the problem seems to be that the memo I wrote as a result of your visit was circulated to another of your colleagues, and I was apparently misquoted in the memo as being unhappy that you visited. To the contrary, I believe we had a very enjoyable visit, and as a result of the visit, I wrote a memo in which I tried to outline your position, especially relative to our own product direction. It has been circulated widely within the development and marketing organization, and received favorable comment. It is not clear that I quoted you accurately, however, as there is always that ambiguity in exchanging ideas like this. But as a result of the visit, and the memo, we have made a very large number of changes in our own product funding and direction, which I attribute to that point in time surrounding your visit.

I'm extremely unhappy that the memo got outside the DEC product development and product marketing organizations, and much sorrier that it got outside of DEC. Not because I was particularly embarrassed of what I said in the memo relative to you, but that the memo relatively clearly outlined a view of product strategy and our deficiencies in position that I would just as soon not be made public. In order that you can verify this, I have asked Keith Miles to show you his copy of the memo. (I know not where he got it) and ask that you read it on a confidential basis.

I would like to get your comments on it as to how accurate you feel I quoted you. Keith Miles was also concerned about the tone of the memo as he is responsible for a large part of UC. He intends that we are able to keep the current position with respect to sales in your campuses. It is certainly his intent that he do everything that we are able to do necessary to keep this position. Certainly I am available to help in anyway that I can, because I also would like to keep the same position with respect to sales there.

DIGITAL EQUIPMENT CORPORATION, 146 MAIN STREET, MAYNARD, MASSACHUSETTS 01754
(617)897-5111 TWX: 710-347-0212 TELEX: 94-8457

Apparently there was also a misunderstanding about how strongly you felt about the position of the DECsystem 10 in the computing picture at UC. I think it would be helpful if you would read the memo and comment as to how accurate I was in stating this position, because I perhaps overstated your position, but in a way it is almost irrelevant because this kind of thing is purely a matter of opinion and degree, and only time will tell.

All in all I certainly appreciated our meeting and I look forward to further interchange when I visit UC/Irvine as Professor Feldman has assured me that you will be present at their Tenth Birthday party, at which I will be a visitor.

If you have any inputs that you think would be helpful to us about the future of computing, I am always available to exchange ideas. From my standpoint, you caused no trouble within our organization, and I'm sorry about the foul-ups at your end.

Sincerely,

Gordon Bell
Vice President
Office of Development

GB:mjk

cc: Keith Miles

digital INTEROFFICE MEMORANDUM

TO: Distribution

DATE: January 14, 1975

FROM: Gordon Bell

DEPT: OOD

EXT: 2236 LOC: ML12/A51

SUBJ: ARPA MEETING ON INTELLIGENT TERMINALS

We are invited to attend a meeting with an ARPA group which is investigating the use of AI programs on small machines, and in essence makes them more available.

The two topics are:

1. Reduction in program size.

2. What software systems are needed to support the programming.

They would like someone knowledgeable in our Operating Systems so that the users aren't tempted to reinvent, or discount available systems.

I believe it would be worthwhile for Pete Van Roekens or Larry Wade to go.

Please get back to me so I can call back!
What you think!

GB:mjk

Distribution

Jim Bell
Larry Portner
Pete Van Roekens
Larry Wade

digital INTEROFFICE MEMORANDUM

TO: OOD

CC: Mark Abbett
Jim Cudmore
Dick Best

DATE: January 14, 1975

FROM: Gordon Bell

DEPT: OOD

EXT: 2236 LOC: ML12/A51

SUBJ: OOD STAFF MEETING MINUTES--January 9, 1975

1. John Cronkite presented the Product Manager's school.

2. Best and Amann--we are asking Jim Cudmore to come back in 8 weeks with a DEC Safety Standard. Ron Minezzi is presenting a first pass at Engineering Committee.

3. Ken described the organization vis a vis the Woods Meetings. The implications for us:

   A. It may be appropriate to have an interface to P/L's similar to their interface with manufacturing, finance, personnel (sales has a similar problem).

   B. We are moving to systems versus computer components (e.g. disk) PSG's for P/L interface. Computer component level will exist intra central engineering.

4. We approved Nat's plan to establish a Communications Review Board inside the software standards framework.

5. Gordon will call Leng and Marcus relative to the problem of planning and building communications systems.

6. The production interface. The 2x2--Bob will work on it specifically with Howard Reed and Jim Cudmore (if appropriate). The issue certainly needs cleaning up and a plan. Bob should report back on this.

7. Stocky came to ask for $20K-40K for a 12", integrated, low cost terminal with TPS (20K for terminal, 20K for TPS). Stocky will deliver a 1 page proposal on the subject.

GB:mjk

Future Items:

1. Hardware/Software Systems Plan — Portner/Clayton

digital INTEROFFICE MEMORANDUM

TO: Nat Teichholtz

DATE: January 15, 1975

FROM: Gordon Bell

DEPT: OOD

EXT: 2236 LOC: 12-1

SUBJ: NETWORK FUNDING

Nat, I had a talk with John Holman about the possibility of obtaining the funding for networks. John is certainly building networks all the time in Special Systems and is in fact implementing the standard DEC DDCMP protocols such that the things he builds wi-l in rpinciple be able to eventually talk to other things that are built from a network standpoint. As such John said he is willing to fund some of the standards in software activities.

I think this is excellent, and I think in fact by doing it that way we will all spend less for development and end up with networks--products that talk with other products.

Will you follow this up please?

GB:mjk

SUBJ: DDCMP STANDARD

DATE: 01-15-75
FROM: GORDON BELL

* *
PLEASESEND TO: FILE
* *

SUBJ: THE MAKING OF DDCMP INTO A STANDARD OUTSIDE OF DEC

I received a letter the other day from Hazeltine requesting a DDCMP spec, presumably so they could implement it on some of their equipment. I read that a reputable company, whose name I forget, is also intending to make DDCMP available as a product.

As I read our policy now on DDCMP, it is fundamentally that in the long run we believe SDLC will prevade as the industry standard for communication among machines. But in having such a standard defined defacto, by IBM, we inherently will be at their mercy from the point of view of changes, and understanding and any products that can use it for say connection to IBM machines will probably be inherently in the range of 1 to 2 years behind any published standards. This is because their simultaneous announcement of a product and standard will give them an inherent edge of 2 years-while we go about the understanding, the application of the understanding and the market education. I think we must understand that the low level protocol continues to be just more of the tip of the iceburg.

In essence the protocol is to the ANSCII character set as a command language is to the protocol and in having a protocol one can at least physically send messages, but then you engage in a mere matter of programming at either end of the terminal to support the various higher level commands that are transmitted using the protocol--e.g. transmit a file. Therefore, our policy on DDCMP is that we are in fact actively using it to implement products, simply because we almost understand it, and it can operate on today's hardware (as opposed to SDLC which requires special hardware). We can begin to focus on the higher levels with respect to machine to machine communication which we have been calling networking. We can get on with the applications.

In a sense we may have a built in market in taking this fairly

SUBJ: DDCMP STANDARD DATE: 01-15-75
FROM: GORDON BELL

evolutionary step in respect to DDCMP. Since it can run on existing equipment, we may have provided the industry with a standard that has long been searching for outside the really terrible 2780 standard that exists. In addition, DDCMP has the capability of running on either a synchronous or asynchronous communications lines. Therefore, we offer the computing and communications industry a significant standard, that is the ability to intercommunicate with existing equipment efficiently and error free, and get the benefits that normally we would attribute to standard languages, that is the ability to communicate.

I didn't see the issue this way until today--i.e. I thought we were just going off on a relatively independent trip. The way SDLC and DDCMP work are sufficiently close at the network command language level that once one has the system intercommunicating, transmitting jobs and files and tasks and things of that form, the switching over to another hardware (SDLC) and device driver set, doesn't appear to be a significant task, although it will be a traumatic and more difficult than we think. But we do have an edge on the problem since we do understand that this will probably eventually happen. Therefore, what I think we want to do is to:

> Eventually obtain the ability to use the SDLC protocol but to make the DDCMP a standard. Actively go through it through the ANSCII and/or CBEMA committees and some the associated headaches to provide the world with a way of interconnecting already existing hardware in a clean way.

I initially had asked Stu Wecker to put DDCMP into the ANSCII standard committees, simply as a tongue in cheek proposal to foil IBM, because I really didn't like the way they played around with the standards committee with respect to the standard and SDLC. Now I believe that DDCMP does have a role as a standard. Not in lieu of SDLC, but in parallel with SDLC until the world switches over--probably 3 years from now. What do you think?

GB:mjk

Distribution

Tom Hastings
Allen Kent
Tony Lauck
Stu Wecker

SUBJ: DDCMP STANDARD

DATE: 01-15-75
FROM: GORDON BELL

cc:

Marketing Committee
DDD
Vince Bastiani
John Gilbert
Frank Hassett
John Holman
Bill Klein
John Leng
Julius Marcus
Dave Stackpole
Nat Telchholtz

SUBJ: NOISY EQUIPMENT

DATE: 01-15-75
FROM: GORDON BELL

* *
PLEASESEND TO: FILE
* *

To: Distribution

Dick reminded me the other day how noisy our equipment is. I had independently been reminded a few days before as I walked into one of the programming areas and talked to some of the programmers and looked at the problem of baffling some of the equipment.

We subject our programmers to incredible hell. Can we begin to solve some of the problems internally, because I think we have to worry about the productivity. Also, this is cheap front-end money. With the noise levels one has in programming with the machines, there is just no way they can stand being around the machines that long. Therefore, what I would like to ask, is how can we look at some of the areas where the sound is particularly bad--building 3 and building 5--and work on reducing the sound level to ones that are normally fit for human consumption. If we learn anything by it, we can apply it and make it available to some special customers who would like a reasonable environment.

I think we have come a long way on terminals. Stockebrand is to really be congratulated on not having a fan, the LA36 is almost tolerable, and I think will eventually be when they get the right fans in there (I hope it is before I start using one--but since the outside demand is so high I will wait until we have some spares).

How can we get this noise design criteria under control? Should we go out and push OSHA to be unreasonable so we can meet it?

GB:mjk

Distribution

John Clarke

SUBJ: NOISY EQUIPMENT

DATE: 01-15-75
FROM: GORDON BELL

Dick clayton
Larry Nye
Dave Nevala
Larry Portner
Bob Puffer

January 15, 1975

Dr. Craig Fields
ARPA
1400 Wilson Boulevard
Arlington, Virginia 22209

Dear Dr. Fields:

Enclosed you will find an unsolicited proposal for a personal computer system capable of interpreting the PDP-10 instruction set.

I hope the proposal is in concert with your research program because we are quite excited about the possibility of such a personal computer. We believe that it is important to do as a research program because of its highly unorthodox nature...i.e. I feel that the feasibility of such a system will be very difficult to believe, and understand, without a prototype.

Also included is a research program on multiprocessor architectures for a modular communications system using our forthcoming large scale integrated circuit PDP-11.

I'm sorry we have not worked more closely with you in the exact definition of the project, but we certainly appreciated the interaction, guidance, and motivation you have given. We are quite receptive to changes. Please feel free to call me or Bruce Delagi, or Stuart Wecker at any time. My home phone is: 617-259-9144. We also are available to visit your office at any time.

Sincerely,

Gordon Bell

Gordon Bell
Vice President
Engineering

GB:mjk

DIGITAL EQUIPMENT CORPORATION, 146 MAIN STREET, MAYNARD, MASSACHUSETTS 01754
(617)897-5111 TWX: 710-347-0212 TELEX: 94-8457

digital INTEROFFICE MEMORANDUM

TO: Ed Corell

CC: Mark Sebern

DATE: January 15, 1975

FROM: Gordon Bell

DEPT: OOD

EXT: 2236 LOC: 12/1

SUBJ: LA36

Ed, is the LA36 for Mark on its way? I thought you were going to make one available to him. I want the front end work of terminals to proceed. This is extremely important to have this front end work done properly and the incremental price to pay here is peanuts. How are you going to get him one?

I make out the cost, if you steal one from Westfield, as $1000--- the incremental income that we would have made on the sale, and if he comes up with some product ideas, vis a vis enhancement, you've gained (particularly on the existing one) a whole product class of revenue. Thus, I look at it as a really cheap investment.

GB:mjk

digital INTEROFFICE MEMORANDUM

TO: Mark Sebern

DATE: January 20, 1975

FROM: Gordon Bell

DEPT: OOD

EXT: 2236 LOC: ML12/A51

SUBJ:

Some of the articles I looked at are the Scan Conversion algorithms for cell organized raster display--March 74 from the ACM, and an article of February 1974 by Jordan. There is an article in ELECTRONICS, February 7, 1974, by Thornhill and Cheek; and an article by Noll in March 71 on scan displays/computer graphics. Of course, April 1974 Proceedings of the IEEE was on computer graphics.

GB:mjk

SUBJ: COMPUTER CORPORATION OF AMERICA

DATE: 01-21-75
FROM: GORDON BELL

* *
PLEASESEND TO: FILE
* *

SUBJ: THE COMPUTER CORPORATION OF AMERICA (CCA)
MESSAGE SWITCHING SYSTEM

To: Don Alusic

Dr. Tom Marrill, President of CCA, called about some possibilities of our marketing his software on our PDP-11's--as a system. It works. He intends to market a service; hence, we should be compatible.

Don Alusic agreed to set up this meeting and I'd like to go with as many of you (cc: list) as possible.

Tom wants a 2+ phase approach:

1. Come, look at the system, get a rough idea of what it is and how it works--discuss whether we might be interested in going to part 2.

2. They would give a full-blown presentation at DEC to a wide audience.

GB:mjk

cc: John Fisher
George Friend
Ken King
Julius Marcus
Stan Olsen

SUBJ: LSI-11 MODULES DATE: 01-21-75
FROM: GORDON BELL

* *
PLEASESEND TO: FILE
* *

SUBJ: THE LSI-11 MODULES AND STEVE'S CONFERENCE

To: Dick Clayton
cc: Steve Teicher

I'm quite concerned that Steve's decision theory techniques are only applicable to projects outside Steve's group. Having lost in getting Steve to a common size for a power supply that could go in either an 8 or small 11 box and/or getting a common box for the 2 products, I at least understand Steve's art of non-negotiable demands. I hope the PS wasn't in the critical path for the 11/04, because these 2 counter-intuitive (to me) decisions certainly could have been costly in terms of NOR.

I'm also somewhat disturbed that the learning exercise I went through on packaging--and tried to present widely to engineers and much of DEC--wasn't taken seriously.

The drawer is clearly the worst packaging method that can be selected; and taking cables from the module handles places constraints on the packaging such that I don't believe a very good package can be designed--assuming one assigns arbitrary weighted values to an objective function consisting, for example, of cooling, cost, servicability, reliability, ...cableability. What is worse, a hastily designed box is now a constraint--we can't move because of limited development funds (we are in a crunch), and we have to meet arbitrary specs.

Steve is in the position of designing a new bus and mechanical structure for a computer that, I hope, will last many years. As such, there should be an attempt to do it right; and I would have thought it propitious to get feedback from internal users (P/L engineers and engineering managers--Bastiani, Savell,...) as well as through 1 or 2 marketing people--unless of course, we expect all the output to be OEM, or we expect a redo for each group. The problem with a single market outlet is that their forecasts may be wrong by up to a factor of

SUBJ: LSI-11 MODULES

DATE: 01-21-75
FROM: GORDON BELL

4 to infinity (on downside). I didn't see the very wide bus the modules use, and I think it may lose much of what the WD bus gains.

The other problem, while we want the OEM market (although it does turn down quickly and starts up slowly) we really do want advanced end user products, e.g, a lab spectrum analyzer, graphics, remote concentrator, remote controller for IPG, etc., that this gives. Here we'll make more money by having advanced products!

The Marketing Committee's decision to use a package scheme that appears to be poorly conceived was, I believe, irresponsible--violating the principle: if it don't work, don't announce it, and will put much more heat on Steve's already hot organization. As a party to previous packaging, PS, and backplane deals which have been oversold internally--I say let's clean up a few pending issues before committing totally beyond our resources to build a new package, power supply, bus, etc.

Please send me the spec and plan for Q-set and package, and then let's talk about a few of these issues

GB:mjk

SUBJ: MUSEUM PROTOTYPE IN MILL DATE: 01-22-75
FROM: GORDON BELL

* *
PLEASESEND TO: FILE
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SUBJ: MUSEUM POLICY AND MUSEUM PROTOTYPE IN MILL

To: Roy Gould
cc: Ken Olsen, Jim Bell

Since we are not going to do the museum for a while, I would like to take a section, since you are still continuing the funding on it, and put on various temporary exhibits in the lobbies of the mill and possibly in Parker Street.

Parker Street might even be more urgent because the people there don't know about computers. This would be a warm up for the full museum and it would test the output of the group that we have been funding.

I visited Bell Labs last week and they have a PDP-11/45 running there on their own operating system--UNIX, to manage all the displays in the front lobby, which is in fact about 25. The displays are the usual junk that one sees and would expect at a museum where a spectator pushes a button and sees some lights blink, or hear some talking.

If the museum is non profit, I think we can get a copy of their operating system and the various types of programs to do this. This is a really impressive system because it allows you to go in and program any kind of behavior quickly. I would like to urge that as a matter of principle, nothing in our museum be built that isn't computer controlled.

GB:mjk

cc: Jim Bell
Ken Olsen
Harold Trenouth

January 20, 1975

Prof. Robert Ashenhurst
University of Chicago
Chicago, Illinois 60637

Dear Bob:

Thank you for the hospitality extended to me in Chicago last Thursday. It was good to see your network activity first hand after reading about it. I was disappointed that you haven't a large user base yet, but these things always take a large effort. I believe the development of a special monitor will significantly detract from the network. Please let me urge you to consider one of our RSX series monitors, or the Bell Labs UNIX monitor, which, I believe, will accomplish the task.

Ed Kramer, who heads our Laboratory Data Products (LDP) Marketing group, is responsible for products in your environment. If there's some cooperative arrangement you'd like to propose for product development, it should be through him.

I believe it would be worthwhile to interact with our product development, because I'd like to know how you regard it. Similarly, you might find parts of interest--particularly in the protocol area. Nathan Teichholtz is our networks program manager; Stuart Wecker is the architect, and George Thissel is working on networks within the LDP marketplace.

Nat can send information on our DDCMP protocol, plus information of a general nature on our networks plans. Specific manuals aren't available yet, and they aren't ready for public disclosure. Therefore, the best way of communicating will probably be verbally, either through George, Stuart or Nathan. Since they're quite busy implementing, it isn't clear they could visit now, but it would, no doubt, be worth calling them to see if further interchange is worthwhile.

Again, thanks for the hospitality.

Sincerely,

Gordon Bell
Vice President, Office of Development
Professor, Computer Science
Carnegie-Mellon University (on leave)

GB:mjk

cc: Ed Kramer, Nat Teichholtz, George Thissell
Stu Wecker, Tom Schendorf (Chicago)

DIGITAL EQUIPMENT CORPORATION, 146 MAIN STREET, MAYNARD, MASSACHUSETTS 01754
(617)897-5111 TWX: 710-347-0212 TELEX: 94-8457

January 21, 1975

Dr. Mel Schwartz
Electrical Engineering and
Computer Sciences
2145 Sheridan Road
Evanston, Illinois 60201

Dear Mel:

Thank you for the hospitality extended to me at Northwestern and at the ACM talk on Thursday evening. I enjoyed visiting with you during the day and seeing the facilities at Northwestern.

Sincerely,

Gordon Bell
Vice President
Office of Development

GB:mjk

DIGITAL EQUIPMENT CORPORATION, 146 MAIN STREET, MAYNARD, MASSACHUSETTS 01754
(617)897-5111 TWX: 710-347-0212 TELEX: 94-8457

January 23, 1975

Dr. Craig Fields
ARPA
]400 Wilson Boulevard
Arlington, Virginia 22209

Dear Dr. Fields:

In our rush to get the proposal to you, we didn't stamp "proprietary" on it. Please consider the document as proprietary and disseminate only as far as you feel is necessary.

We prefer the proposal and product not be discussed at the ARPA contractors meeting on terminals.

Sincerely,

Gordon Bell

Gordon Bell
Vice President
Office of Development

GB:mjk

DIGITAL EQUIPMENT CORPORATION, 146 MAIN STREET, MAYNARD, MASSACHUSETTS 01754
(617)897-5111 TWX: 710-347-0212 TELEX: 94-8457

SUBJ: LA36ASR, VT51, AND DEC MICRO'S

DATE: 01-23-75
FROM: GORDON BELL

* *
PLEASESEND TO: FILE
* *

To: Ed Corell
Lorrin Gale
Tom Stockebrand

SUBJ: LA36ASR, VT51, AND DEC MICROPROCESSORS

I read with interest Jay Mackro's memo on ASR logic board: A STUDY OF SEVERAL METHODS OF IMPLEMENTATION OF 12/19/74.

Several conclusions*:

1. The cost for almost all the approaches are about the same except that the 11/WD is about 100-200 more, depending on the memory. (I wouldn't use 4K RAM--as the study showed.)

2. Special LSI in this area probably will only cost us by slowing a project down.

3. We probably have plenty of money if the 3 groups get together to pool their resources to produce 1 product, I.e., VT51, LA and LSI (2-3 people "studying").

4. From an ROI standpoint, using Teicher's stuff may get some products--whereas, there won't be money another way--hence, no ROI.

Can I ask Ed to take the leadership here in examining how we might produce the ASR and VT51 with 1 design within our current budget?

GB:mjk

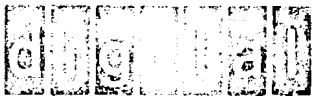
cc: OOD
Al Huefner
John Hughes
Mike Leis
Jay Mackro

SUBJ: LA36ASR, VT51, AND DEC MICRO'S

DATE: 01-23-75
FROM: GORDON BELL

Julius Marcus
Steve Telcher

*Aside from the fact that the memo should be an appendix to a table giving the results, and needs some conclusions, it seems to have the facts and indicates design understanding.



January 20, 1975

Dr. George L. Wied
Dept. of Obstetrics and Gynecology
University of Chicago
Chicago, Illinois 60637

Dear Dr. Wied:

It was a pleasure meeting you and discussing how we might be able to interact with you in the future as the pattern recognition system reaches production status. I looked over the reprints you gave me, and read "Objective Cell Image Analysis"; I'm sorry we didn't have the time to see a demonstration of your system.

I will discuss your application of multiple LSI-11's for pattern recognition, and how we might get involved in your subsequent stage of development with various DEC groups. My guess is that we probably wouldn't want to get involved in the direct marketing of such a system, but would prefer to sell modules to another manufacturer more closely tied to the medical supply field, or even build a special system for some other manufacturer. Since this is a basic marketing question, I'll defer the problem to Win Hindle and Andy Knowles.

The various marketing groups who might be interested in this application generally report to Win Hindle, who you know; they include: Original Equipment Manufacturer (OEM--Bill Long), Laboratory Data Products (LDP--Ed Kramer), Computer Special Systems (CSS--John Holman). LDP is, no doubt, where the interaction should be with for now. In addition, the DEC Components Group (DCG), headed by Andy Knowles, first market the basic boards for the LSI-11. Allen Michels, who you also know, manages the DCG marketing.

The Product Manager, who is in the engineering organization responsible for the product, is Steve Teicher.

Some information on the LSI-11, and a definition of the modules, is enclosed. I certainly dislike the notion of not using DEC computers in your system, which I believe is so important, and hope we can respond better now that we have a product that appears to be more suited to your application.

I enjoyed talking with you, and look forward to continued interaction.

Sincerely,

Gordon Bell

Gordon Bell
Vice President, Office of Development

GB:mjk

cc: Win Hindle, Andy Knowles, Ed Kramer, Bill Long, John Holman, Steve Teicher
Tom Schendorf (Chicago)

DIGITAL EQUIPMENT CORPORATION, 146 MAIN STREET, MAYNARD, MASSACHUSETTS 01754
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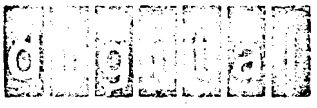


January 21, 1975

Prof. William Lennon
Electrical Engineering &
Computer Science
Northwestern University
2145 Sheridan Road
Evanston, Illinois 60201

Dear Bill:

Thank you for the hospitality extended to me at Northwestern and at the Chicago Chapter of the ACM during the talk on Thursday evening. I enjoyed talking with your students and seeing the laboratory network equipment. I'll be anxious to hear of the progress on the automated laboratory as it comes into existence.

I'm enclosing some articles and material on the LSI-11, which I hope will give you some idea of what it will be like. I would appreciate your keeping this material confidential until our announcement.

I hope that some of our people in the laboratory data products marketing group can visit you at some time, so as to compare notes about capabilities. Also, Nat Teichholtz is our head of network activities and is interested in these applications too. I would appreciate any written material you have on the network, including reports on protocols, equipment, bootstraps, user manuals, systems, etc.

I look forward to the photographs of the VT50 prototype in your lab and would appreciate any comments you have on it from users.

Again, thanks for the hospitality.

Sincerely,

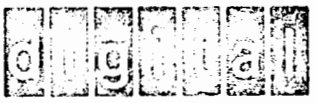
Gordon Bell
Vice President
Office of Development

GB:mjk

cc: Nat Teichholtz
Ed Kramer

Enc.

DIGITAL EQUIPMENT CORPORATION, 146 MAIN STREET, MAYNARD, MASSACHUSETTS 01754
(617)897-5111 TWX: 710-347-0212 TELEX: 94-8457



January 24, 1975

National Aeronautics
and Space Administration
John F. Kennedy Space Center
Florida 32899

Gentlemen:

After a very thorough review of your Request for Proposal 10-2-001-5 for Minicomputers and Peripherals for Checkout, Control and Monitor Subsystem of the Launch Processing System, Digital Equipment Corporation respectfully requests the opportunity to submit a late proposal in accordance with paragraph 7 on page 12 of your Request for Proposal.

The basis for this request is two-fold. First of all, an alternative technical solution is obviously possible since the benchmark data, in enclosure 1, that we are submitting with this letter indicates we more than satisfy the time constraints stated in your RFP, without the use of Writeable Control Store. Secondly, the specification is very explicit about the requirement for Writeable Control Store and Microprogrammable code features. Since you have placed such importance on these features and you would prefer "off-the-shelf" hardware, we request to submit an offering, in May 1975, based on a current new product development which both complies and exceeds the specifications, and satisfies the "off-the-shelf" desire.

Digital Equipment Corporation has consistently maintained a leadership role in the minicomputer field in both technology and total number of installations. We hope that our past successful performance coupled with our current new product developments will permit you to grant us a favorable decision on our request for a late proposal.

(continued)

If we can provide any further information, do not hesitate to contact me or Mr. James H. Kouarik and/or Mr. Daniel Murry of our Orlando Office, Telephone Number 305-851-4450. Thank you very much for your consideration.

Very truly yours,

Gordon Bell.

Gordon Bell
Vice-President
Office of Development

GB:sml

SUBJ: OOD STAFF MINUTES

DATE: 01-24-75
FROM: GORDON BELL

* *
PLEASESEND TO: FILE
* *

SUBJ: OOD STAFF MEETING MINUTES--1/23/75

To: OOD
CC: Mark Abbett, Ed Corell, Tom Stockebrand

1. A. Ed Corell and Tom Stockebrand will get together to work on the terminal plan.

   B. We will get Tom a decision on his request for budget over-run to maintain the group by February 1.

2. Becky Hawes introduced us to the Corporate Salary Planning process for 1975.

3. Mark will get back with expense visibility on the recruiting mechanism. The cost center pays for recruiting.

4. A. We will go to OC to ask for a policy to add people to spend according to budget.

   B. Larry asked for 5 hires: 3 are approved as a replacement. We recommend the other 2 to OC--Larry is under budget.

5. Gordon will get George Plowman to take over the Engineering Committee. (Notes on Eng. Co. Charter attached.)

6. We currently believe we aren't effectively communicating with Field Service and Production. We will talk with them once/quarter (Shields/Cudmore--St. Amour).

7. Core and MOS now meet the budget. Components is paying for core on 11/WD!

   A. 32K--progress in understanding ringing, better operating point, redressed lines. Two systems running at margin and room temperature. Report at schedule review on Wednesday, Feb. 15, looks good.

   B. MOSTEK--failure rates up on early devices at 70deg. C.

GB:mjk

digital INTEROFFICE MEMORANDUM

TO: Distribution

DATE: January 30, 1975

FROM: Gordon Bell

DEPT: OOD

EXT: 2236 LOC: ML12/A51

SUBJ: INTELLIGENT TYPEWRITER FOR DUMB PEOPLE (I.E. VOICELESS) TO USE FOR COMMUNICATION

The attached device is entering a hobby stage for me. A friend, Constantine Doxiadis, a planner and my wife's employer, has MS. His voice is gone, and he still wants to communicate, write and confer. I may get into doing the programming--another example of a small system.

I'm proposing to use an 8V, 8/A with floppies, mounted in a carrying case together with a keyboard and video monitors.

GB:mjk

Attachment — filed under inventions. Copy too light to film.

Distribution

Jim Bell
Ed Corell
John Clarke
Ed Kramer
Ken Olsen

digital INTEROFFICE MEMORANDUM

TO: Distribution

DATE: January 30, 1975

FROM: Gordon Bell GB

1058

DEPT: OOD

EXT: 2236 LOC: ML12/A51

SUBJ: RELATIVE COSTS ASSOCIATED WITH TERMINALS

	Cost/Yr (K$)	Cost ($)/Hr @ 2400 Hr.
Person	5, 10, 20, 40	2, 4, 8, 16
System	(12-25)/10=1.2~2.5	.5~1.
Terminal @ (4 yrs)	.25~.75	.1~.4
Service (assume 2400 MTBF)	.05	.02
Space	.050 - .100	.02 - .04
Power	.005~.01	.002~.004
Line charges	0~2.4	0~1.00
Paper	0~.1	0~.04

GB:mjk

Distribution
OOD
Ed Corell
Andy Knowles
Stan Olsen
Tom Stockebrand

cc: Ken Olsen

G. Bell
1/31/75

WHO'S DESIGNING/SELLING/USING PRODUCTS?

1059

P/L
- COMM
  - COMM
  - Telco
- PDP-10
  - Do?
  - DAS 10
- LDP-net
- IPG
- CSS
  - US
  - Europe--Germany

Central
- COMM Hdw
- COMM Soft.
- Net Soft.
- Net Prod. Mgmt.

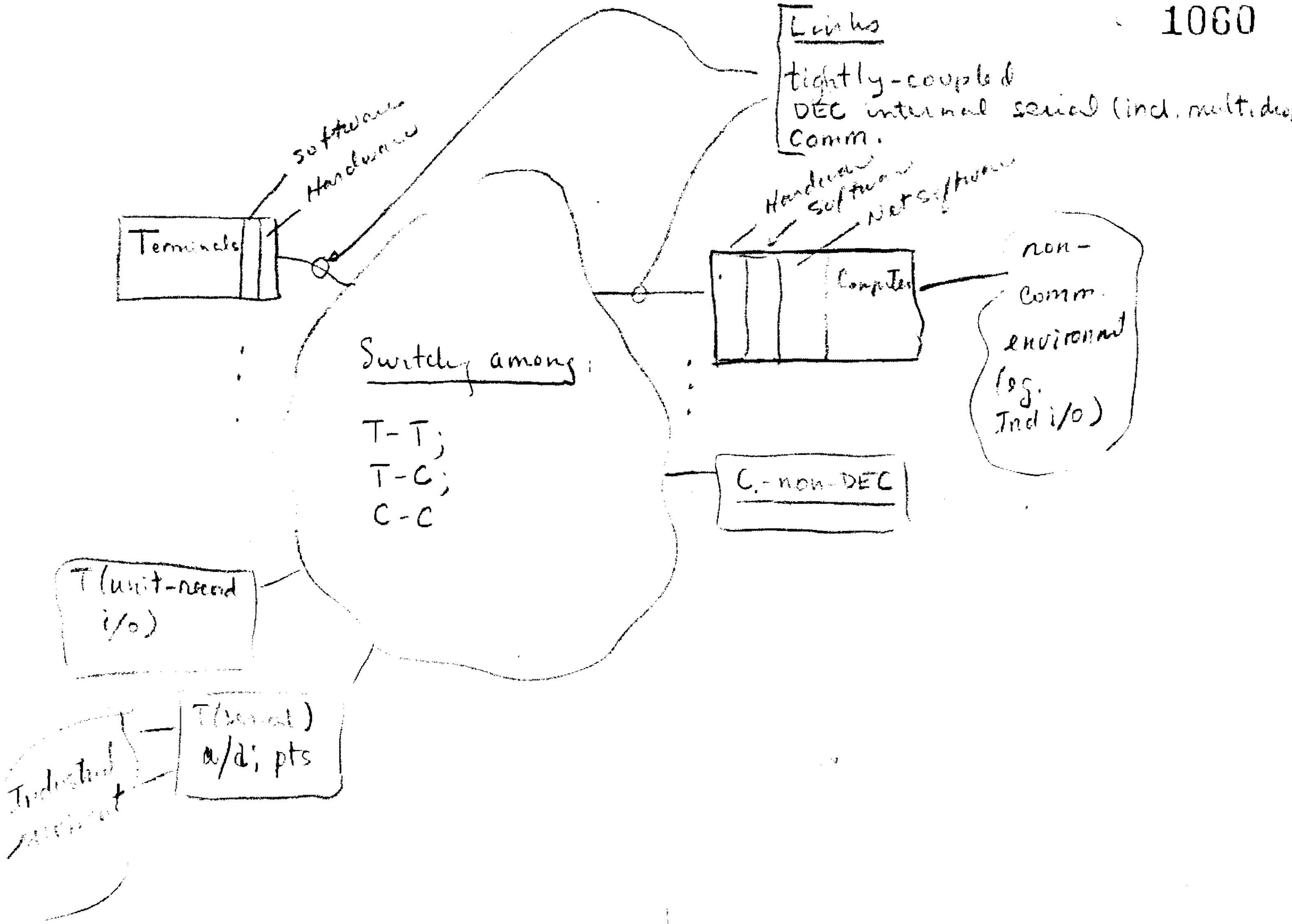
} Software

In house
- Eng.
  - CS/2
  - DA
- DECnet
- EDP--Maynard→ FS; WM→WM

Concerns

1. Product goodness (competitive $/perf; perf; reliability)
2. Future: LSI-11, dist. process, higher perf.; better T's.
3. Resources are spent--do all, incremental!
4. Non standard! Need adequate ones--must adhere to them } LDP-DAS
5. Lack of products: s/f; c-to-c; multiple 10; concentrators.
6. High support.

The Communications – Terminals – Network Domain



Thing	Standards
Hardware interfaces to Links (from C.)	tightly coupled DEC defined serial Comm
Terminals	20ma | EIA | multidrop. Terminal conventions
Software support	to Std. Op. Sys.
Sub systems (e.g. concentrators, RJE T's, s/f switch)	DDCMP.
Networks	NCL Software utilities Inter-process.
other	files command language. terminal modes. Languages.

GB 1/21/75

Who's Designing / Selling / Using Products?

P/L

Comm.

Comm

Telco

PDP-10

DO ?

DAS 10

LDP - net

IPC

CSS

US

Europe - Germany.

Central

Comm. Hdw

Comm soft.

Net Soft } Software

Net Prod. Mgmt }

In house.

Eng.

CS/2

DA

DECnet

LDP — Hayward → FS ; WH → WH

Concerns

1. Product goodness (competitive $/perf; perf; reliability)
2. Future; LSI-11, Dist. process, higher perf., better T's.
3. Resources: are spent — do all, incremental!
4. Non-standard! Need adequate ones — must adhere to them. (LDP-CSS)
5. Lack of products: s/f; C-to-C; multiple 10; Concentrators
6. High support
7. Nei

SUBJ: ALPHANUMERIC GROUP

DATE: 02-03-75
FROM: GORDON BELL

* *
PLEASESEND TO: FILE
* *

SUBJ: APPROVAL OF ALPHANUMERIC GROUP OVERRUN FOR 1 MONTH; REJECTION OF REQUESTS FOR LSI-11, LA 180

To: Operations Committee

From: Gordon Bell
Chairman, Products Committee

The Products Committee voted to not recommend the requested overrun for the VT51-, LA 180, LA36+, LSI-11, LSI-11 (core). Funding was approved for the next month for the alphanumeric group VT51 overrun to hold the group together. The Office of Development was requested to return to the Products Committee with a better recommendation.

The basis for the disapproval was:

1. The product lines are being held back next year and more products in this appear to only increase expense, not NOR.

2. The low end terminal strategy is certainly unclear as it relates to LA180, LA36 options and specials of all types especially, including ASR's, and VT51's.

3. The rapid build up of production capacity is occurring in a single plant and there is credibility that this is possible, especially in light of a new disk system which will be entering the same plant in the same time frame.

4. There is some scepticism on the part of product and product line managers as to whether terminal build up can occur with the rapidity forecast...especially since much of this will have to be on a specialized (learned) basis.

5. The build up shifts the resources away from the current center of the business and we have not reforecast spending and future NOR.

SUBJ: ALPHANUMERIC GROUP

DATE: 02-03-75
FROM: GORDON BELL

6. Examining the current product contribution and ROI for the LA180, VT50, and LA36, they are all below corporate average; hence, underpriced. The payoff is long, and in the case of VT50, the use of engineering resources is a factor of 3 too high. Future terminals are clearly going to suffer too.

For these reasons, we recommend that the overrun not be approved, except for the alphanumeric group and for the next month.

I believe a group composed of Puffer, Knowles, and Reed should look at the overall terminals plan in terms of the above considerations. Corell and Stockebrand have been working at the product part. Bell, Laut, and Frith will recompute the allocation of resources as a function of current and projected NOR. These forecasts (plans) are also needed before a plan occurs. (We would like the assistance of Curtis and Thompson.) Teicher and Tomasic have yet to establish a low end plan which is evolving rapidly, and appears to require much money, resources, etc.

GB:mik

cc: Products Committee
Ed Corell
Julius Marcus
Tom Stockebrand

SUBJ: DIALOGUE WITH JULIUS

DATE: 02-03-75
FROM: GORDON BELL

* *
PLEASESEND TO: FILE
* *

SUBJ: DISCUSSION WITH JULIUS ON OUR PRODUCTS

To: OOD
CC: Julius Marcus

I've been pressing quite hard for improving terminals and COMM products.

Julius has several important inputs on products which are under our direct control, which I hope we all understand and can establish some objectives to remedy.

1. The packaging and cabling is terribl. COMM exascerbates this by having lots of cables and odd-sized modules. (My feeling that we must stop the works-in-a-drawer designs unless we want out of COMM and IPG markets.

2. Diagnostics is nil. For Telco 370/158--MTBF is 2 months, MTTR is 2 hours. For 11/40--MTBF is 10 months, MTTR is 10 hours.

3. The 4 was a bad product idea (except for parity). It is unforecastable (unscheduled). The 8 is a worse idea. Marketing Committee rammed it down the PL managers throats.

I still would welcome having Julius at our staff meetings, but we must all have more dialogue with him.

GB:mk

digital

1065

February 4, 1975

D. B. Gillies
Professor of Computer Science
and Applied Mathematics
Computer Science Department
University of Illinois at Urbana-Champaign
Urbana, Illinois 61801

Dear Don:

Thanks for the documents on PASCAL I received in December. I was also anticipating more information on the later PASCAL and am curious as to how these tests are and when it will be available.

I had several people look at it, and although I think we may eventually be interested in it, I don't think we are right now. I would like to get your reaction as to what you think we might do with it as a product. Should we use it for implementing languages, operating systems, applications? Would users want it? When do you think there will be a standards effort?

George Poonan has been using PASCAL on the PDP-10 to write a language parse table generator, and he is looking at it for other applications. I still think we would like to get an object program somehow to fully evaluate. I still believe that if an object tape were available on some of our in house machines the interest might be increased. But without a way to look at it, there is not sufficient interest at this time.

I would like Al Brown to visit you in the future and discuss your views, and keep in touch as to how it might be useful. I believe it would be highly useful to our users community through DECUS. But since you are undoubtedly still interested in getting more support for it, then that avenue is probably out of the question. On the other hand, that would establish a need, and in the event that we wanted to make it a product, we would then work with you to establish a price.

I wish I could get more enthusiasm for the product internally, but I need your help somehow.

Sincerely,

Gordon Bell, Vice President
Office of Development

GB:mjk
cc: Al Brown, George Poonan

DIGITAL EQUIPMENT CORPORATION, 146 MAIN STREET, MAYNARD, MASSACHUSETTS 01754
(617)897-5111 TWX: 710-347-0212 TELEX: 94-8457

DEPARTMENT OF COMPUTER SCIENCE
UNIVERSITY OF ILLINOIS AT URBANA-CHAMPAIGN

1066

November 27, 1974

DEC 02 1974
12-5

Professor C. Gordon Bell
Vice President for Engineering
Digital Equipment Corporation
Maynard, Massachusetts 01754

Dear Gordon:

Enclosed please find two documents:

(1) a manual for the present (bootstrap) PASCAL-11,

(2) a sample of how it compiles code.

Since we are concerned only with clean code (not optimized) for such a provisional compiler, it should be read in that spirit. The final PASCAL (written in PASCAL) is coming up quite fast--we are going to test it on students next week and we expect to have it reasonably solid by December 20. I'll send a sample output as soon as possible. There will be some optimization at that time but much more in the first 10 weeks of 1975. Next semester it will be used for two courses--operating systems and compilers.

We don't use C ourselves so can't give you any first-hand information about it.

Sincerely,

D. B. Gillies
Professor of Computer Science
and Applied Mathematics

DBG:jw

Encl.

digital INTEROFFICE MEMORANDUM

1067

TO: Gordon Bell

CC: J. Bell
Al Brown

DATE: January 21, 1975

FROM: George Poonen

DEPT: R & D Group

EXT: 3537 LOC: 3-4

MJ get me Gillies letter & answer S

JAN 21 1975

SUBJ: PASCAL

This memo is in response to the letter sent by Professor Gillies regarding PASCAL. I have not seen any proposal by Professor Gillies and I have only evaluated the language implementation based on the documents sent by him.

A. First, how can DEC benefit?

1. As a systems programming language-
(for operating system and compiler development)
NO- The current implementation is not sufficient to warrant this. It makes no attempt at producing optimizing code. Possibly better code is forthcoming. On the other hand, as a language PASCAL is probably the cleanest and least error prone language existing today. PASCAL is more than adequate for writing compilers; however, it lacks adequate facilities for constructing operating systems. (Both Tony Hoare and Hansen are currently involved in extending PASCAL for this purpose.)

2. As an applications language-
(for application where a high degree of optimization is not required)

MAYBE- provided some of the basic constructs such as POINTERS and SETS are implemented. The current implementation has neither.

On the other hand, the language is not suitable for business applications because of lack of adequate I/O and data management facilities.

3. As an educational language-
MAYBE- many major universities and schools have adopted PASCAL as their standard. In fact, PASCAL is now available on all major manufacturers'machines. Provided the implementation is complete it would be attractive to some universities. On the other hand, it is not clear how big this market is today. The majority still teach FORTRAN, BASIC, PL/1, and COBOL.

4. As a language available through DECUS-
   YES- this appears to be the most suitable category under which DEC could acquire it. This has several advantages. Perhaps we could acquire their PASCAL when it is complete in exchange for some other piece of software.

B. The implementation of PASCAL by Professor Gillies-

1. The state of the compiler as documented in the recent letter (Dec. 1974) appears to be very similar to that existing about 6 months earlier when I visited him.

2. The implementation is reasonable; no attempt has been made to produce optimized code although the compiler does not produce really dumb code either. The paucity of examples shown preclude any real evaluation. (I can't understand why he cannot send us an object tape for an honest evaluation.) Optimization has been mentioned by Professor Gillies as not being an initial goal.

3. The implementation lacks the following basic constructs: POINTERS and SETS.

4. The run time system provided with the compiler appears to be fairly good. This is based on some of the facilities that I saw on my visit.

5. Dynamic records are not available since POINTERS are not available. This is a major weakness.

All in all it makes me very doubtful whether at this stage we should consider Gillies' PASCAL. As far as I can tell, there have been no substantial improvements since I saw it 6 months ago. (Documents for both are attached.) When a full implementation together with some optimization is available we should reevaluate this implementation. Hopefully he could send us a copy of the object code so that we can run it ourselves. Meanwhile, we may wish to consider concurrent PASCAL by Hansen which includes additional constructs for building operating systems. (However, this will not be available for at least another year.)

PASCAL as a language is about the cleanest language existing today. It embodies a number of innovations which make it less error prone than any other existing language. However, even PASCAL, simple as it is, may be too rich a language to introduce at DEC. A highly optimizable and, in fact, simplier subset of PASCAL could be considered as an alternative to assembly language for internal use but not as a product. Such a language will require about 6 months to implement. Until PASCAL becomes a standard (if it ever does) or attains the status of ALGOL, FORTRAN, etc., we should not consider it as a language for a product.

GP/bd

PASCAL/11 USER'S GUIDE

UNIVERSITY OF ILLINOIS, URBANA, ILLINOIS

1069

LANGUAGE AS OF

VERSION 4

20-NOV-74

NTRODUCTION

PASCAL/11 VERSION 4 IS AN IMPLEMENTATION ON THE PDP-11 OF HE PROGRAMMING LANGUAGE PASCAL. IT IS WRITTEN IN MACRO-11, AND IS ESIGNED TO BE A BOOTSTRAP COMPILER FOR THE NEXT VERSION TO BE RITTEN ENTIRELY IN ITSELF. IT IS ASSUMED THAT THE READER IS AMILIAR WITH THE LANGUAGE PASCAL AS DESCRIBED IN THE REVISED EPORT ON THE PROGRAMMING LANGUAGE PASCAL BY NIKLAUS WIRTH. THIS OCUMENT IS INTENDED TO DESCRIBE THE DIFFERENCES BETWEEN THE ANGUAGE SO DESCRIBED AND THE CURRENT IMPLEMENTATION, AND ALSO TO PECIFY SOME OF THE CONCEPTS NOT COMPLETELY DEFINED IN THE REPORT. S THIS IMPLEMENTATION IS MERELY A BOOTSTRAP, IT HAS NOT STRICTLY DHERED TO THE SPECIFICATIONS MENTIONED ABOVE. THE NEXT VERSION, S EXPECTED TO BE TOTALLY COMPATIBLE WITH OTHER IMPLEMENTATIONS F THE LANGUAGE. FURTHER, THIS DOCUMENT DESCRIBES THE VOCABULARY SED BY THE IMPLEMENTATION, AND THE CHARACTER SEQUENCES USED O REPRESENT VARIOUS PASCAL SYMBOLS. SINCE THE CHARACTER SET AT N INSTALLATION IS INDEPENDENT OF THE PROGRAM, IT IS EXPECTED HAT THE CHARACTER CONVENTIONS WILL BE THE SAME IN FUTURE MPLENTATIONS.

A ONE-PASS COMPILER WHICH PRODUCES AS ITS OUTPUT FILE A SET OF MACRO-CALLS, AND DEFINITIONS CONSTITUTES THE FIRST PHASE OF COMPILATION. THESE MACRO-CALLS, TOGETHER WITH A SET OF MACRO-DEFINITIONS, IS ASSEMBLED BY THE MACRO-11 ASSEMBLER TO PRODUCE AN OBJECT FILE. THE OBJECT FILE MAY BE LINKED TO A SET OF PASCAL RUN-TIME OBJECT FILES TO PRODUCE A STAND-ALONE PASCAL LOAD MODULE, OR IT MAY BE LINKED TO ITSELF TO PRODUCE A RE-ENTRANT, POSITION-INDEPENDENT MODULE (CALLED A CODE MODULE), WHICH CAN BE CALLED BY ANOTHER PASCAL PROGRAM. SINCE THE CODE MODULE IS A DOS FILE, THERE MUST EXIST A MECHANISM FOR FINDING THE NAME OF A PASCAL EXTERNAL PROCEDURE TO SUCH A FILE, AND THESE CONVENTIONS ARE DESCRIBED LATER.

IN ADDITION, THE FIRST PASS PRODUCES A LISTING OF THE SOURCE PROGRAM INCLUDING ERROR MESSAGES IF ANY. THE FIRST PASS ACCEPTS SPECIFICATIONS FOR INPUT AND OUTPUT DATASETS USING THE DOS COMMAND STRING INTERPRETER IN THE FOLLOWING FORM:

MACRO DATASET,LISTING DATASET<SOURCE DATASETS

COMPILER DIRECTIVES

COMMANDS TO THE COMPILER SUCH AS FORMAT CONTROL OR ERROR HANDLING DIRECTIVES, ARE NOT AN INTRINSIC PART OF THE LANGUAGE. THEY ARE SPECIFIED BY MEANS OF AN ESCAPE CHARACTER '$' OCCURRING AS THE FIRST CHARACTER ON A LINE. THIS CHARACTER IS NOT USED ANYWHERE ELSE IN A PASCAL PROGRAM (EXCEPT POSSIBLY INSIDE QUOTED STRINGS, WHICH MAY NOT CROSS LINE-BOUNDARIES) AND DENOTES THE START OF A COMPILER DIRECTIVE.
THE VALID $ COMMANDS AND THEIR MEANINGS ARE DESCRIBED BELOW:

$LIST	INCREMENT THE INTERNAL LIST COUNTER.
$NLIST	DECREMENT THE INTERNAL LIST COUNTER (UNLESS IT IS ZERO) IF THE COUNTER IS GREATER THAN 0 (IT IS INITIALLY 1) THEN THE SOURCE IS LISTED. IF A LINE OF SOURCE CONTAINS SYNTAX ERRORS, IT IS LISTED, REGARDLESS OF THE STATE OF THE LIST COUNTER. THESE OPTIONS PERMIT SELECTIVE SUPPRESSION OF THE LISTING.
$OCOMMENT	INCREMENT THE INTERNAL COUNTER OUTCOM.
$NCOMMENT	DECREMENT OUTCOM. IF OUTCOM (WHICH IS INITIALLY ZERO) BECOMES GREATER THAN ZERO, THE COMPILER PRODUCES DEBUG OUTPUT IN THE FORM OF COMMENTS CONTAINING THE SOURCE LINE PRECEDING THE CORRESPONDING MACRO-11 STATEMENTS GENERATED. THIS IS ESPECIALLY USEFUL FOR DE-BUGGING THE FIRST PASS.
$PAGE	CAUSE A FORM-FEED TO APPEAR IN THE LIST FILE (.LST) A NEW PAGE HEADER INCLUDING THE FIRST SIX CHARACTERS OF THE PROGRAM NAME, THE PAGE NUMBER AND VERSION NUMBER APPEAR AT THE TOP OF THE NEXT PAGE.
$IOLIM=<NUMBER>	SETS THE I/O LIMIT THIS IS A RUN-TIME PARAMETER DEFINING THE MAXIMUM NUMBER OF I/O REQUESTS THAT MAY BE MADE BY THE PROGRAM. NOTE THAT FOR A DISK FILE THIS NUMBER CORRESPONDS TO THE NUMBER OF BLOCKS IN THE FILE, WHILE FOR LP: IT CORRESPONDS TO THE NUMBER OF BUFFERS WRITTEN. THE DISK ACCESSES INVOLVED IN LOADING AN EXTERNAL PROCEDURE ARE COUNTED AS I/O REQUESTS. SETTING IT TO ZERO ($IOLIM=0) IS EQUIVALENT TO SETTING NO LIMIT.
$TIMELM=<NUMBER>	SETS THE TIME LIMIT IN SECONDS AS WITH $IOLIM, SETTING $TIMELM = 0 IMPLIES THERE IS NO LIMIT ON THE TIME THE PROGRAM MAY RUN.
$SYNTAX	INHIBITS CODE GENERATION AND EXECUTION, SO THAT ONLY THE SYNTAX OF A PROGRAM IS CHECKED. THIS REDUCES THE NUMBER OF DISK ACCESSES THE COMPILER NEEDS TO DO, AND THEREBY INCREASES THE COMPILE RATE. ONCE SET, THIS OPTION CANNOT BE TURNED OFF.
$ERRLIM=<NUMBER>	SETS THE INTERNAL COUNTER ERRLIM. IF THE NUMBER OF SYNTAX ERRORS FOUND EXCEEDS

EXECUTION STEP ARE SUPPRESSED.

>WARNLM=<NUMBER> SETS THE INTERNAL COUNTER WARNS.
IF AT ANY STAGE DURING THE FIRST PASS
THE NUMBER OF SYNTAX ERRORS FOUND EXCEEDS WARNS,
THEN THE COMPILER ABORTS COMPILATION IMMEDIATELY.

>STKSIZ=<NUMBER> DEFINES THE SIZE OF
THE RUN-TIME STACK. THE DEFAULT IS
1200. THIS IS THE AREA USED TO
ALLOCATE ALL NON-STRUCTURED
VARIABLES IN A PROGRAM.

REMARK

END

THIS IS USED TO ALLOW MULTI-LINE SEQUENCES OF DOCUMENTATION.
IT IS EQUIVALENT TO THE COMMENT CONVENTION DEFINED IN THE
REVISED REPORT, BUT IS RELATIVELY IMMUNE TO THE PROBLEM
OF MISSING COMMENT DELIMITERS.

CODE

END

THIS IS A MECHANISM TO PERMIT THE INSERTION
OF ASSEMBLY LANGUAGE STATEMENTS WITH A PASCAL PROGRAM.
ANY VARIABLE WHOSE SCOPE INCLUDES THE BLOCK
CONTAINING THE ASSEMBLY CODE MAY BE REFERENCED
WITHIN THAT ASSEMBLY CODE.
SINCE ALL VARIABLES IN PASCAL ARE
ADDRESSED OFF A REGISTER, (GLOBAL VARIABLES
OFF R5, LOCAL VARIABLES OFF R4), THE
PASCAL IDENTIFIER, IN ASSEMBLY LANGUAGE
ACTUALLY CORRESPONDS TO THE VALUE OF THE
OFFSET. THE COMPILER THUS GENERATES THE EQUATES
NECESSARY TO BE ABLE TO ACCESS THE
VARIABLES CORRECTLY.
THUS, THE FOLLOWING MAY BE TROUBLESOME:

```
PROGRAM DISPLAYR0;
        VAR R0:INT;
        PROC DISPLAY(VALUE:INT);
                BEGIN
$CODE
                MOV     VALUE(R4),R0
                HALT
$END
                END; "DISPLAY"
        BEGIN
        .
        .
        .
        END.
```

IN THE MOV INSTRUCTION SHOWN ABOVE, BOTH VALUE
AND R0 REPRESENT OFFSETS FROM THE RELEVANT DISPLAY
REGISTERS. FOR OBVIOUS REASONS, USE OF
$CODE BY ANYONE NOT FAMILIAR WITH PASCAL
INTERMEDIATE CODE IS TO BE DISCOURAGED.

HE FOLLOWING COMMANDS ARE USED TO DEFINE THE VARIABLES
OST, NOSUB, NODIM.
HESE VARIABLES ARE USED FOR CONDITIONAL ASSEMBLY.

EMANTICS:

OST=0 MEANS THAT STATEMENT NUMBERS ARE MONITORED AT RUN-TIME.
OST=1 MEANS THAT STATEMENT NUMBERS ARE NOT MONITORED.

/OSUB=0 ENABLES RUNTIME SUBSCRIPT CHECKING.
/OSUB=1 DISABLES RUNTIME SUBSCRIPT CHECKING, THEREBY SAVING CORE AND TIME
/ODIM=0 ENABLES DYNAMIC CHECKING OF ARRAY DIMENSIONS.
/ODIM=1 DISABLES RUNTIME CHECKING OF ARRAY DIMENSIONS.
OF COURSE, FOR A SINGLE PROGRAM THIS CAN BE DONE AT COMPILE
TIME. IT IS ONLY USEFUL FOR EXTERNAL PROCS WITH ARRAY
ARGUMENTS.

:COMMANDS:

:NOST SETS NOST TO 1.
:YOST SETS NOST TO 0.
:NSUB SETS NOSUB TO 1.
:YSUB SETS NOSUB TO 0.
:NDIM SETS NODIM TO 1.
:YDIM SETS NODIM TO 0.

:EFAULTS:

/OST=0
/ODIM=1
/OSUB=0

. LOWER CASE LETTERS ARE TRANSFORMED TO THE CORRESPONDING
PPER CASE LETTERS, IN THIS VERSION.

. THE FOLLOWING SPECIAL SYMBOLS HAVE THE DESIGNATED MEANINGS:

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!	SET UNION, LOGICAL OR.
&	SET INTERSECTION, LOGICAL AND.
\	NEGATION
\=	NOT EQUAL TO
<=	LESS THAN OR EQUAL TO
>=	GREATER THAN OR EQUAL TO
"	OPEN COMMENT
"	CLOSE COMMENT THERE IS NO AMBIGUITY ABOVE, SINCE A CLOSE COMMENT CAN OCCUR ONLY AFTER AN OPEN COMMENT
:=	ASSIGN
_	ASSIGN

. THE CHARACTER SET IS ASCII, WITH THE ASCII COLLATING SEQUENCE.

. ABBREVIATIONS:

INT	INTEGER
PROC	PROCEDURE
FUNC	FUNCTION

. THE RANGE OF VALUES FOR A VARIABLE OF TYPE INTEGER IS -32768..32767.

ECLARATIONS

. LABEL DECLARATIONS: ONLY LABELS THAT ARE USED IN TRANSFERS
UT OF PROCEDURES NEED BE DECLARED EXPLICITLY. THE AMBIGUITY
AUSED BY ENCOUNTERING A GOTO TO A LABEL WHICH HAS NOT YET BEEN
EFINED IN THE BLOCK, BUT HAS BEEN DECLARED IN THE SURROUNDING
LOCK (THAT IS, SHOULD THE GOTO BE INTERPRETED AS A BLOCK EXIT,
R A TRANSFER TO AN AS YET UNDEFINED LABEL WITHIN THE SAME BLOCK)
S HANDLED BY USING AN EXTRA RESERVED WORD, EXIT. THIS IS DESCRIBED
N MORE DETAIL IN THE NEXT SECTION. IN THE REVISED REPORT, THE
MBIGUITY IS HANDLED BY DECLARING ALL LABELS DEFINED IN A PROCEDURE,
ND THE NEXT VERSION SHOULD DO THE SAME.

. CONSTANT DEFINITIONS:
THE FOLLOWING FORMS ARE ALLOWED.

```
CONST
        X=65;
        X=+65;
        X=-65;
        X='A';          (SAME AS X=65;)
        X=+'A';         (SAME AS ABOVE)
        X=-'A';         (SAME AS X=-65;);
        Y=X;
        Y=+X;
        Y=-X;
        Z='ABCDEF'      (AN ARRAY CONSTANT)
```

THE FOLLOWING ARE NOT ALLOWED:

```
        X=-'ABCDEF';
        X=+'ABCDEF';
        X='ABCDEF';   Y=+X; OR Y=-X;
```

THE PREDEFINED CONSTANTS ARE EOL=10 (LINE-FEED),
FALSE=0, TRUE=1, NIL=0, AND ALFALENG=2.
THESE ARE ALL RESERVED WORDS AND MAY NOT BE
REDEFINED.

YPE DEFINITIONS:

. INTEGER IS A RESERVED WORD AND IS EQUIVALENT TO -32768..32767
CHAR IS A TYPE THAT CAN FIT IN ONE 8-BIT BYTE.
BOOLEAN = (FALSE,TRUE); ANY SUCH SCALAR TYPE DECLARATION
IMPLIES THAT CONSECUTIVE INTEGRAL VALUES, STARTING FROM ZERO,
ARE ASSIGNED TO SUCCESSIVE ELEMENTS OF THE DECLARATION,
AND THE TYPE IS DEFINED TO BE EQUIVALENT TO A SUBRANGE
TYPE 0..LASTELEMENT; THUS THE DECLARATION FOR BOOLEAN
IS THE SAME AS:

```
CONST
     FALSE=0;
     TRUE=1;
TYPE
     BOOLEAN=0..TRUE;
```

EAL (THAT IS FLOATING POINT) OPERATIONS HAVE NOT
EEN IMPLEMENTED AS THE HARDWARE FOR SUCH
NSTRUCTIONS DOES NOT EXIST ON OUR PDP-11.
INTEGER, CHAR, BOOLEAN, REAL ARE ALL RESERVED WORDS, AND MAY
NOT BE REDEFINED.

. GENERAL SCALAR TYPE DECLARATIONS ARE ALLOWED, AND ARE INTERPRETED
AS WITH BOOLEAN. THUS, COLOR=(RED,ORANGE,YELLOW); IS THE SAME AS

```
CONST
     RED=0;
     ORANGE=1;
```

```
TYPE
      COLOR=0..YELLOW;
```

NONE OF THE ELEMENTS OF A SCALAR TYPE DEFINITIONS MAY BE USED ELSEWHERE IN THEIR BLOCK EXCEPT AS DEFINED CONSTANT IDENTIFIERS.

SUBRANGE TYPES ARE PERMITTED USING ANY TWO NON-ARRAY CONSTANTS. THUS THE FOLLOWING ARE PERMITTED:


```
CONST
      LO=0;
      HI='Z';
      MINUSZ=-HI;
      TENBASE8=8;
      GREEN=3;
TYPE
      T1=LO..HI;
      T2=MINUSZ..HI;
      T3=MINUSZ..-5;
      COLOR=(RED,ORANGE,YELLOW);
      T4=RED..TENBASE8;
      COLOR2=RED..GREEN;
```

IF THE RANGE OF VALUES DEFINED BY A SIMPLE TYPE DECLARATION CAN BE STORED IN 8 BITS, THEN ALL VARIABLES OF THAT TYPE ARE STORED IN 1 BYTE. THIS IS ONLY FOR STORAGE PURPOSES, AND ALL CALCULATIONS ARE PERFORMED ON THEIR 16-BIT EQUIVALENTS. FOR THE PRESENT NO RANGE CHECKING IS DONE AT RUN-TIME. FOR EXAMPLE, A BOOLEAN VARIABLE MAY TAKE ON THE VALUE 2.

NO STRUCTURED TYPE IS ALLOWED IN A TYPE DEFINITION. ALL VARIABLES OF STRUCTURED TYPES, MUST BE DECLARED EXPLICITLY IN THE VARIABLE DECLARATION.

```
TYPE
      X=ARRAY[0..1] OF INT;
VAR
      A:X;
```

MUST BE WRITTEN AS

```
VAR
      A:ARRAY[0..1] OF INT;
```

3. VARIABLE DECLARATIONS

VARIABLES MUST BE ONE OF THE FOLLOWING TYPES:

A. SIMPLE TYPE, (WHICH MAY BE DEFINED EARLIER USING A TYPE IDENTIFIER)

B. FILE OF CHAR. 3 OPTIONS ARE AVAILABLE WITH A FILE DEFINITION, AND ARE SPECIFIED IN SQUARE BRACKETS AS SHOWN:
FILE[OPTION1,OPTION2,OPTION3] OF CHAR;
THE FIRST OPTION SPECIFIES IN/OUT/EXT CORRESPONDING TO THE DOS OPENI,OPENO,OPENE OPTIONS.
THE SECOND OPTION SPECIFIES ASCII/BINARY CORRESPONDING TO ASCII OR BINARY FILES.
THE THIRD OPTION SPECIFIES A DEVICE NAME.
ANY OR ALL OPTIONS MAY BE ABSENT, IN WHICH CASE THE DEFAULTS ARE FILE[IN,ASCII,SY] OF CHAR; WHERE SY IS THE NAME OF THE SYSTEM DEVICE (LIKE DF0).
THE ACTUAL NAME OF THE FILE MAY BE OBTAINED BY
NAME=FIRST 6 CHARACTERS OF PROGRAM NAME.
EXTENSION=FIRST 3 CHARACTERS OF FILE NAME.

C. RECORDS CAN HAVE ELEMENTS OF ONLY A SIMPLE TYPE, AND VARIANTS ARE NOT ALLOWED. FURTHERMORE, IDENTICAL FIELD NAMES IN TWO DIFFERENT RECORDS WHICH ARE DECLARED IN THE SAME BLOCK ARE NOT ALLOWED, UNLESS THE RECORDS ARE BE DECLARED IN THE SAME VARIABLE LIST.

D. SET AND POINTER TYPES ARE NOT IMPLEMENTED.

E. ARRAYS OF ARBITRARILY MANY DIMENSIONS ARE ALLOWED. HOWEVER, THE ARRAY TYPE CAN BE ONLY SCALAR, OR OF TYPE RECORD. SINCE AN ARRAY OF ARRAYS IS THE SAME AS A SINGLE ARRAY OF ONE HIGHER DIMENSION, THE FORMER HAS NOT BEEN IMPLEMENTED. THUS

```
VAR
        X:ARRAY[0..10] OF ARRAY[0..10] OF CHAR;
```

IS NOT PERMITTED, WHILE THE EQUIVALENT REPRESENTATION USING MULTIPLE DIMENSIONS SHOWN BELOW IS ALLOWED:

```
VAR
        X:ARRAY[0..10,0..10] OF CHAR;
```

PROCEDURE/FUNCTION DECLARATIONS

WITHIN DECLARATIONS OF PARAMETERS FOR PROCEDURES OR FUNCTIONS, THE FOLLOWING RULES APPLY.

A. VAR SPECIFIES A CALL-BY-REFERENCE.

B. THE DEFAULT IS CALL-BY-VALUE FOR SIMPLE VARIABLES AND CALL-BY-REFERENCE FOR STRUCTURED VARIABLES.

C. CALL-BY-VALUE FOR STRUCTURED VARIABLES HAS NOT BEEN IMPLEMENTED.

D. PROCEDURE AND FUNCTION PARAMETERS HAVE NOT BEEN IMPLEMENTED.

E. FOR ARRAY PARAMETERS, THE RANGE OF SUBSCRIPTS SPECIFIED BY THE FORMAL PARAMETER SPECIFICATION IS IGNORED, AND THE RANGE OF SUBSCRIPTS FOR THE CORRESPONDING ACTUAL PARAMETERS ARE USED. THUS, THE FORMAL DECLARATION SPECIFIES ONLY THE NUMBER OF SUBSCRIPTS OF THE ARRAY, AND ITS TYPE. IT IS THEREBY POSSIBLE, FOR EXAMPLE, TO WRITE PROCEDURES WHOSE PARAMETERS ARE STRINGS (=ARRAY OF CHAR) OF UNKNOWN LENGTH.

F. SIMIALRLY, THE OPTIONS SPECIFIED FOR AN ACTUAL FILE PARAMETER TAKE PRECEDENCE OVER THE OPTIONS SPECIFIED FOR THE CORRESPONDING FORMAL PARAMETER.

G. BOTH DECLARATIONS OF A FORWARD PROCEDURE/FUNCTION MUST HAVE AN IDENTICAL PARAMETER LIST.

'HE FOLLOWING OPERATIONS ARE NOT YET IMPLEMENTED.

A. NEW( )
B. SET OPERATIONS
C. THE FLOATING POINT FUNCTIONS SUCH AS SIN( ) OR ROUND( )

'HE FOLLOWING ARE EXTENSIONS/MODIFICATIONS:

A. TO DISTINGUISH BETWEEN JUMPS INSIDE A PROCEDURE AND EXITS TO OUTSIDE BLOCKS, A NEW STATEMENT 'EXIT <LABEL>' IS INTRODUCED.

B. CASE STATEMENTS CAN HAVE AN DEFAULT CLAUSE BY USING AN 'ELSE' WHERE A CASE LABEL SHOULD SYNTACTICALLY OCCUR.

C. FOR READ AND WRITE USING DECLARED FILES, THE SYNTAX IS 'READ <FILENAME> (LIST)' AND 'WRITE <FILENAME> (LIST)'.

D. WHILE WRITING A NUMBER TO A FILE OF CHAR, (A NUMBER MEANS AN EXPRESSION OF TYPE INTEGER, OR SUBRANGE THEREOF), A FIELD WIDTH MAY BE SPECIFIED BY PUTTING A ':<EXPRESSION OF SIMPLE TYPE>' AFTER THE EXPRESSION TO BE PRINTED. THE VALUE OF THE FIELD WIDTH SPECIFIER CAN BE USED TO CONTROL THE FOLLOWING:
   - LEADING ZEROS,
   - FIELD WIDTH SET TO MINIMUM POSSIBLE,
   - BASE 2, 8, 16 OR 10
   - TREAT THE NUMBER AS UNSIGNED.

   THE VALUES NEEDED TO SELECT ONE OR MORE OF THE ABOVE OPTIONS IS AVAILABLE IN EARLIER DOCUMENTATION.

F. MULTIPLE ASSIGNMENTS ARE ALLOWED IN AN EXPRESSION, AND ARE EVALUATED FROM RIGHT TO LEFT.

G. THE FOLLOWING FILE OPERATIONS ARE ALLOWED:
   - RESET (IN DOS CLOSE, OPEN FOR INPUT)
   - REWRITE (IN DOS DELETE, OPEN FOR OUTPUT)
   - CLOSE (CLOSE GIVES UP BUFFER SPACE)
   - EXTEND (IN DOS OPEN FOR EXTENSION)

DURING THE LAST QUARTER, THE BOOTSTRAP VERSION OF THE PASCAL COMPILER HAS BEEN COMPLETED, AND WORK IS PROGRESSING ON A COMPILER WRITTEN IN PASCAL ITSELF. THE NEW VERSION WILL INCLUDE THE ENTIRE DEFINED LANGUAGE PASCAL, TOGETHER WITH THE EXTENSIONS ALREADY PRESENT IN THE BOOTSTRAP VERSION, AND IS BEING DESIGNED SO AS TO MAKE FUTURE EXTENSIONS EXTREMELY EASY. THE INTENTION IS, IN PART, TO ALLOW EXPERIMENTATION WITH LANGUAGE CONSTRUCTS TO BE AS SIMPLE AS POSSIBLE.
ANOTHER DESIGN CONSTRAINT IS THAT THE CODE-GENERATION ROUTINES SHOULD BE EASILY CONVERTED TO GENERATE CODE FOR OTHER MACHINES, SUCH AS THE LOCKHEED SUE.

LANGUAGE AS IT EXISTED IN JULY 1974

THE BOOTSTRAP COMPILER HAS BEEN FROZEN AT ITS PRESENT LEVEL, SO THAT WORK CAN PROGRESS ON VERSION 2.
THE DIFFERENCES BETWEEN THE LANGUAGE ACCEPTED BY THE BOOTSTRAP VERSION AND THE LANGUAGE DEFINED IN THE PASCAL REPORT ARE AS FOLLOWS:

1082

1) VARIABLES OF TYPE SET ARE NOT CURRENTLY PERMITTED.
2) ONLY FILES OF TYPE CHAR MAY BE DECLARED. HOWEVER, A FILE MAY BE DECLARED AS A BINARY FILE, IN WHICH CASE IT MAY BE TREATED AS A FILE OF INTEGER.
3) RECORDS MAY NOT INCLUDE ARRAYS AS SUBFIELDS, AND A DECLARED TYPE MAY NOT INCLUDE AN ARRAY.
4) PROCEDURE/FUNCTION PARAMETERS ARE NOT YET IMPLEMENTED.
5) FUNCTIONS MAY RETURN ONLY SIMPLE VARIABLES.
6) THE GOTO STATEMENT HAS BEEN SUB-DIVIDED INTO TWO FORMS. THE FIRST ALLOWS BRANCHES WITHIN THE CURRENT BLOCK, AND IS INVOKED BY
   GOTO <LABEL>;
   THE SECOND ALLOWS ONLY BRANCHES OUT OF THE CURRENT BLOCK, TO A DECLARED LABEL, AND IS INVOKED BY
   EXIT <DECLARED-LABEL>;
   THIS MAKES PROGRAMS EASIER TO COMPREHEND, AND REMOVES SOME POSSIBLE AMBIGUITIES.
7) POINTER TYPES ARE NOT IMPLEMENTED.
8) PACKED ARRAYS ARE NOT EXPLICITLY IMPLEMENTED. HOWEVER, IF A VARIABLE'S VALUES FALL IN A SUB-RANGE OF -128..127, THE VARIABLE WILL BE STORED IN A BYTE, SO SOME PACKING IS DONE IMPLICITLY.
9) ARRAY AND RECORD PARAMETERS MAY NOT BE CALLED BY VALUE.
10) PROCEDURE AND FUNCTION PARAMETERS ARE NOT YET IMPLEMENTED, BUT IT IS EXPECTED THAT THEY WILL COME UP PRIOR TO VERSION 2 OF THE COMPILER.
11) THE TYPE 'REAL' IS EQUIVALENT TO INTEGER.
12) ANY PROCEDURE MAY BE DECLARED 'FORWARD'. THIS ALLOWS MUTUAL RECURSION OF PROCEDURES. THE PARAMETERS OF THE PROCEDURE MUST BE DECLARED AT THE FIRST DECLARATION OF THE PROCEDURE. IF A PROCEDURE IS DECLARED FORWARD AND NOT SUPPLIED, A RUNTIME ERROR IS CAUSED ON THE FIRST ATTEMPT TO EXECUTE IT.
13) A PROCEDURE MAY BE DECLARED EXTERNAL.
   THIS IMPLIES THAT THE BODY OF THE PROCEDURE IS RESIDENT ON DISK, AND SHOULD BE LOADED. THIS PERMITS COMPILATION OF PROGRAMS WHICH ARE TOO LARGE TO BE COMPILED AS A WHOLE. IT ALSO PERMITS A PROGRAM TO OVERLAY ITSELF IN A NATURAL MANNER. CURRENTLY, AN EXTERNAL PROCEDURE CAN ONLY COMMUNICATE WITH ITS CALLER THROUGH THE PARAMETERS ON THE PROGRAM STATEMENT.
   THE PROCEDURE QWERTYUIOP, DECLARED EXTERNAL, WILL BE SEARCHED FOR UNTIL THE TITLE OF QWERTY.COD, UNDER FIRSTLY THE CURRENT USER, AND SECONDLY [1,1]. THIS ALLOWS PUBLIC PROGRAM LIBRARIES TO BE SET UP.
   E.G.
   PROGRAM MAIN;

```
                I: INTEGER;
        PROCEDURE QWERTYUIOP(ASD: INTEGER; VAR FGH: INTEGER);
        EXTERNAL;
        BEGIN
                QWERTYUIOP(4, I);
                WRITE(I, EOL);
        END.
```



```
        IS A POSSIBLE MAIN PROGRAM.  IF THE PROGRAM

        PROGRAM Z(I: INT; VAR J: INT);
        BEGIN
                J←I*I;
        END.

        IS SUPPLIED ON DISK UNDER THE TITLE QWERTYUIOP.COD,
        THE OUTPUT WILL BE
           14
        NOTICE THAT THE PARAMETERS DECLARED SHOULD
        CORRESPOND, IN NUMBER, ORDER, AND TYPE, BUT
        THE NAMES PROVIDED NEED NOT AGREE.
```

14) THE CASE STATEMENT HAS BEEN EXTENDED TO ALLOW 'ELSE' AS A CASE SELECTOR. THE STATEMENT AFTER THE 'ELSE' IS EXECUTED IF THE CASE VARIABLE TAKES ON NONE OF THE VALUES OF THE OTHER CASE SELECTORS.

15) THE STATEMENT WRITE(X:0), WHERE X IS AN INTEGER, CAUSES X TO BE PRINTED WITH NO LEADING SPACES. THUS

```
        WRITE(Z:0, 4:0);
```

CAUSES OUTPUT

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FURTHER EXTENSIONS, TO PERMIT OCTAL AND HEXADECIMAL FORMATS ARE BEING CONSIDERED.

16) THE WRITE AND READ STATEMENTS HAVE BEEN EXTENDED TO ALLOW THEM TO APPLY TO AN ARBITRARY FILE. THE SYNTAX IS

```
        WRITE MYFILE(A, B, C);
```

17) THE FILE DECLARATION STATEMENT HAS BEEN EXTENDED. THE CURRENT SYNTAX IS

ZXC: FILE [<DIRECTION>, <FILETYPE>, <DEVICE>] OF CHAR;

THE EXTERNAL NAME OF THIS FILE WILL BE <PROGRAMNAME>.ZXC.

THE PARAMETERS TAKE ON THE VALUES

<DIRECTION> : CAN TAKE ON VALUES

- IN - THE FILE CAN ONLY BE USED FOR INPUT.
- OUT - THE FILE CAN ONLY BE USED FOR OUTPUT.
- EXT - THE FILE WILL BE OPENED EXTEND, IF IT EXISTS, AND OUTPUT, IF IT DOES NOT ALREADY EXIST.

<FILETYPE> : CAN TAKE VALUES

- ASCII - THE FILE IS A DOS ASCII FILE. ANY INTEGERS TRANSFERED TO/FROM IT WILL BE CONVERTED TO/FROM ASCII. THE DEFAULT FILES INPUT/OUTPUT ARE ASCII FILES
- BINARY- THE FILE IS A DOS BINARY FILE. IT ESSENTIALLY CONSISTS OF A BIT STREAM. READING/WRITING CHARS TRANSFERS A BYTE FROM/TO THE STREAM, WHILE READING/WRITING INTEGERS TRANSFERS TWO BYTES.

<DEVICE> : THIS FIELD CAN TAKE ON THE NAME OF ANY AVAILABLE DOS DEVICE. IF A NON-EXISTENT DEVICE IS SPECIFIED, A FATAL ERROR WILL BE CAUSED, AND THE PROGRAM TERMINATED.

18) THE STANDARD FUNCTIONS EXTEND(FILE) AND CLOSE(FILE) HAVE BEEN ADDED.

19) THE ASSIGNMENT OPERATOR MAY BE USED INSIDE AN EXPRESSION. THUS, A[I←I+1]←J←K←1; IS LEGAL.

20) A STRING IS TREATED AS A CONSTANT ARRAY, AND MAY BE PASSED AS A PARAMETER

A:ARRAY [0..20] OF CHAR;
A:='THIS IS A STRING';
IS A VALID STATEMENT.

22) THE READ/WRITE STATEMENTS HAVE BEEN EXTENDED TO ALLOW SPECIFICATION OF AN ARRAY ARGUMENT.

E.G. VAR A:ARRAY[0..79] OF CHAR; B:ARRAY[0..10] OF INT;
READ(A,B);
WILL READ 80 CHARACTERS FROM THE INPUT FILE INTO A, AND WILL READ THE NEXT 11 INTEGERS ON THE INPUT FILE INTO B. IF A CHARACTER ARRAY IS READ FROM AN ASCII FILE, THE READ IS TERMINATED BY AN EOL, OR BY THE END OF THE ARRAY, WHICHEVER OCCURS FIRST. WRITING A CHARACTER ARRAY ONTO AN ASCII FILE IS TERMINATED BY AN EOL, FF, VT OR ANY NEGATIVE CHARACTER.

23) IT IS POSSIBLE TO READ/WRITE TO/FROM AN ARRAY INSTEAD OF A FILE. AN ARRAY IS ASSUMED TO BE AN ASCII FILE.

THERE ARE SEVERAL ROUTINES IN THE RUNTIME PACKAGE FOR WHICH SUITABLE LANGUAGE CONSTRUCTS ARE NOT YET AVAILABLE. THESE INCLUDE

A) CORE ALLOCATION/DEALLOCATION PROCEDURES, IN READINESS FOR THE IMPLEMENTATION OF POINTERS.

B) A LOADER, CURRENTLY USED BY EXTERNAL PROCEDURES, AND BY OVERLAYS IN THE RUNTIME SYSTEM ITSELF. THERE WILL EVENTUALLY BE SOME TYPE OF CONSTRUCT TO PERMIT RUN-TIME CORRESPONDENCE BETWEEN A PROCEDURE AND A FILE.

C) A PROGRAM MAY START UP A PROCEDURE AS AN INDEPENDENT JOB, OR AS A DEPENDENT, ASYNCHRONOUS PROCESS. THIS IS ONE FORM OF ALLOWING MULTI-TASKING.

IN ADDITION TO THE WORK ON PASCAL, DEC'S MACRO ASSEMBLER HAS BEEN MODIFIED SO THAT THE PERMANENT SYMBOL TABLE MAY INCLUDE REGISTERS, CONSTANTS, AND PRE-DIGESTED MACROS. A PASCAL PROGRAM HAS BEEN WRITTEN TO TAKE A MACRO LIBRARY AS INPUT, AND PRODUCE AN OBJECT MODULE SUITABLE FOR LINKING TO MACRO.OBJ AS OUTPUT.

SUBJ: MILL ENVIRONMENT

DATE: 02-05-75
FROM: GORDON BELL

* *
PLEASESEND TO: FILE
* *

SUBJ: COMMENTS ON THE MILL ENVIRONMENT, WHERE DO WE GO NOW?

To: Distribution

The parts of the mill that have been worked on are really beginning to shape up and show some potential. I truly hope the energy we have expended trying to make it work is worthwhile. I think at this point it is worth thinking about how the scheme, system, work, etc. is going to be evaluated. The only complaint (a side from orange poles) has been from a manager who has not been involved and worries about the expenses. Therefore, the way to squelch this is to get a notion of the true expenses, and show what has been traded off...i.e. some sort of cost-benefit analysis. The tradeoffs appear to me:

0. We trade off general fix-up once to reduce mean time to move (to 4 hours according to Harold).

1. Electrical and telephone installation time versus lower cost of redoing the area next time around.

2. Non-permanent walls at lower costs, trades off specialized walls, and hence, the cost of moving and expanding (i.e. putting more people in a given area--which will be inevitable as we expand).

3. General trade off increased expenses for paints as a way of creating a more pleasant environment in which we hope people will perform better.

In some cases we do better both in costs and in performance. (In some sense, maybe the right way to handle the notion of moving is to perhaps put all the walls in the office supplies catalog, and let people order these supplies in the way way they order stationery and desks, tables--clearly the early bookcase/partition should be in this category.

SUBJ: MILL ENVIRONMENT DATE: 02-05-75
FROM: GORDON BELL

I think a lot of costs can be made lower by doing a better job of refabrication in the factory, e.g. in the electrical case. If your factory makes up the electrical outlets on pigtails, then the first operation is simply drilling the holes in the floors and putting the pigtails through. The electrician goes down below and runs the conduit among the boxes locating the boxes near the pigtails. There is only one operation on a floor, hence, no running back and forth between the floors. Also, it is probably worth getting the box out of the floor which will pick up dirt. The partitions, bookcase/desk housings and other things are all factory built and should be stocked.

It seems to me there are several things that we want to get formalized (ritualized) in regard to the business of living in the mill:

1. Lighting--I didn't realize how bad the tube problem was until I saw the thing at night, looked at it a bit, and then saw the contrast as we walked among the areas. I am really looking forward to Chris Ripman's entry in the "cover the lights sweepstakes." (He went over to PK3, and as a critical young architect, was pleasantly surprised with the overall place--very impressed with the cost, and only unhappy with the lights. Probably because that's his specialty.) I hope that he will come up with something more practical than the other 3 experiments.

   The other problem with the lighting, that bugs me a bit ecologically, is that it seems awfully expensive to have all those lights on all the time, especially with people not in the offices, and for those offices that like local lightings.

   We really could run a campaign in DIGITAL THIS WEEK on turning out lights. Also, we would offer to put a pull chain on the lights that people say they will turn off. At 150 watts/fixture and 4 cents per KWHR, it costs $.006 to run each light/hour. This amounts to about $15/year/light! For the mill it costs about $42/hour. But more locally, if a switch can be put in a fixture for say $4.00, then the payoff is about 700 hours, or if one saves 3 hrs/day, then it is about a year. The lifetime for bulbs is unaffected, and the only issue is whether the switches last long. As an experiment, it would probably be worthwhile in trying the switches in one of the new areas and put the whole thing on a recording watt/hour meter to see if in fact we do save anything over a period of several months. (This should be purely experi-

mental, as it may not work.)

Lighting should also reflect the "importance of the corridor"... going down to more than every fourth light in the lowest orders. In the cage stockrooms of building 3-5, there is too much lighting--a switch would do wonders--remember $15/year/light!

2. Air conditioning. The removal of walls certainly gets at the air circulation problem. When we repair or replace windows, we permit them to be opened, then we have a really big $ saving chance through lower cost air conditioning. In the case of building 12, it might be worth trying the idea my wife suggested, which was to put some barn-type ventilators, or even an exhaust fan, in the top so that during the marginal days we just use fans...a few days of non-air conditioning pays for installation costs. There are clearly many days where we could run without air conditioning if we could open the windows.

3. On the windows. Let's try 6 or so more experiments. I emotionally don't like getting rid of the ones we can see out, mainly because they are high enough that you can't see street activity. But I can't believe you get the openness effect of windows with the highly opaque ones. If/when we have to, we should try to stay with openers, as it relates to the air conditioning...which I want to try to have less of to save money. I also don't want to cover up windows with masonite. The 2 areas in 5-2 with/without are in stark, depressing contrast.

4. Floors. You're right, this is a problem. The issue to me is what is the tensil, shear, and dent strengths of the various materials? It is on these grounds that the various wood products: masonite, marine plywood, etc, compete with one another. I don't know the numbers. In general, if the floors are good enough, we probably ought to stay with what we have, and doing anything on other than an experimental basis will prove costly because we don't know now what to do. Thus, if a floor can be used at all--don't do anything with it until we know something that's better. Experiment only with really bad ones.

Antique houses often scrub down the floors and then apply linseed oil--beautiful color, not sticky, no nail resetting. The best solution is probably to do nothing, because the most awful looking floors are those which we repaired.

and the repair failed (e.g. tile, linoleum, panels painted grey, etc.).

5. Large isles. What can we put there? Picnic tables? Xerox machines in little cubby holes--how about files with rear ends out? Dead storage? Is it too late in 5-2 to use the space somehow? Safety is a problem no doubt.

6. Wall covering. Let's avoid covering up brick. This happened in an area or two already, and I'd like to avoid doing it because we pay $ to get what I believe is a worse solution.

7. Noise. This is a relatively bad, but difficult to deal with problem. I believe there are several things we want to do. Get the sound baffles for the various typewriters and teletypes into the standard DEC office catalog, so that it is painless to get them in the typewriters..especially those bloody teletypes.

   I believe it would be worth getting BBN back to see what is needed to help in some of the deadening. It will also include background white noise, music, etc. We should re-read their recommendations to see if there is insight we have missed.

   Probably the biggest noise reduction should come through the elimination or proper scheduling of various carts, and the rubber tiring of the carts. 5-2 is bad due to 5-3. We should walk around with a sound level meter; take some readings; and see just how far we are from a reasonable level; and where we would like to get to set some goals, and then try an area. The 3-5 conference room gets lots of noise from the computer room next door containing our noisy machines. Maybe just acoustic tile in the computer room + plugging holes would solve the problem. Also, what do the panels that Chris Ripman talked of look like?

8. Painting. Here we seem to have come the furthest. It is really a contrast to walk into an all grey area from the ones which have been painted. This has certainly rubbed off too, as evidenced by the recent painting in the software areas which hadn't occurred until this decoration was done. We may get to the point of having to really control expenses in redoing. However, I still believe in the notion that if you think about the design problem, it doesn't cost much more to do it right, and then you save

SUBJ: MILL ENVIRONMENT DATE: 02-05-75
FROM: GORDON BELL

by not having to redo the job. Also, the key is to stock a few basic paint colors to avoid the time and hassle of someone picking out paint for their offices. Standardize NOW--and get my permission to deviate. This will avoid the stuff that happened in Jim Bell's area with pastels. There is also a problem of control for super graphics--
Pat and one of the designers should control this for now.

10. THE JOHNS. These are almost all quite bad. Can they be spruced up using paint without doing anything drastic in terms of money? How much would it cost?

11. CIRCULATION PLAN. Can an analysis be made of the corridor system, and the noise coupling among floors. We screwed up in not putting production on the lower floors of 5. What is the width needed for a corridor for internal trucks? and the turning radius for corners? What is the width for heavy duty corridors through which furniture can easily be moved? What is the minimum width for internal access corridors in a group's own territory?

On major corridors which must be wide and cannot be cluttered there is some need for creating interesting relief. Super-graphics in paint on long walls is one solution. Another solution is to utilize from each group a large board that represents their product or "interest". This could be hung as a large display panel from the ceiling ala a "hanging." This "hanging" would identify the territory by which a person was passing. These "hangings" could either be ones that might first be used in a central display area--a lobby or museum--and then go to the "group." Or they could be developed by the group, produced according to a standard format and then be used as needed for special displays, shows, meetings, the front lobby etc. etc. I have the original artwork of some 11 parts that is useful this way.

Where do we go from here?

1. I'd like to get a notion of where we are relative to the various new moves. I've lost track of who's going where, and want to get the update, particularly in terms of whether I've given space to production that will be hard to get back. I don't want the corporate stockroom (unless John Trebendis tells me otherwise) to be in the mill. (My guess is that it's a dead storage for somebody operating under an alias.) Let's track them down and probably refuse them...they are not engineering!

SUBJ: MILL ENVIRONMENT DATE: 02-05-75
FROM: GORDON BELL

2. The library. With the activity level they have now, this should be a nice space, because we expect people to go in there and really work. Also, if we can eek out some more space for them, then a really quiet place would be nice when we have people who want to get away from their areas and write programs, or work.

3. Some displays for the lobby. I would like to warm up the museum in the mill using the junk I haveand probably displaying some of the new products there, too.If we can can get the prototypes. I am borrowing an 8 to make music at the New England Conservatory, and it could be used in the lobby for a month or so. Also, we might put a 10 terminal there for a demo to play games, program on, etc.

4. Cafeteria...Is it worth doing anything? Now that we have a reasonable conference room in 3-4, we may not have the big need for a large conference room it has served as. The cafeteria is awfully dreary, and a bit of paint and large graphics there would really help it. This would also hit a good cross section of employees who are not all enjoying rennovated areas--show we are doing something.

5. Central stores. Since you are the storekeeper, one can direct what happens by what's in stock. The things that would get stocked include the new and earlier wooden partitions. Hence, moving is something that can be almost ordered from office supplies. It would include both the old and new partitions, all the accessories for the partitions, sound deadeners for the typewriters, open office type blackboards and visual/sound baffles. If we come up with any other sound baffles, then this could be included too--possibly white noise sources also, and definitely the fixed paint!

6. Finishing our modular furniture. It looks like Plant Engineering has provided most of the accessories needed to complete the system. Let's tune them up, and put in the catalog...i.e. bookcases, tackboards, blackboards, hanging plant racks, the older bookcase/desk backboard, clamp-on lamps, acoustic-visual barriers, etc. The same goes for the supervisor areas (e.g. lidded offices, conference rooms). I'd like the schemes to be documented and purchasable by new movees. A set of before, after, after move in pictures would help movees ordering from the catalog.

7. Publicity--a small exhibition of before/after in the mill lobbies might be helpful, and get DEC interested in a better place

SUBJ: MILL ENVIRONMENT

DATE: 02-05-75
FROM: GORDON BELL

to work,

8. Publication. Pat might talk with a magazine re problems, and where we are. Are any of the designs worth describing outside?

GB:mjk

Distribution

Harold Trenouth
Ed Finn
Pat McCormick
Mary Jane Keeney

cc: Mark Abbett
Ken Olsen

digital

February 5, 1975

Ted Kehl
Department of Physiology
University of Washington
Seattle, Washington

Dear Professor Kehl:

Enclosed are manuals on the PDP-16/RTM system that Allen suggested I send to you.

The K(PCS) was used in the 16/M sub-minicomputer we built with the modules. Please let me know if you have trouble obtaining these parts. Our Components group (Logic Products) sells them and has more information. You might write or call Dwight Baker (DEC, Marlboro, Mass.) if you need more information.

Sincerely,

Gordon Bell

Gordon Bell
Vice President
Office of Development

GB:mjk

cc: Allen Newell, CMU

DIGITAL EQUIPMENT CORPORATION, 146 MAIN STREET, MAYNARD, MASSACHUSETTS 01754
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D I G I T A L INTEROFFICE MEMORANDUM

PAGE 1
SUBJ: P.LANGUAGES DATE: Ø4-14-75
FROM: GORDON BELL
EX: 2236
MS: ML12-1

TO: FILE

SUBJ: P.languages
LANGUAGES, THEIR STATE and INVESTMENT

To: Dist.

In order to get a better handle on our software investment, I feel we need to really assess the software we have on the 11, comparing it with the 1Ø, and other competitors. The 1Ø group did the attached; we need something as to size, investment, capabilities, etc. Each market, can then place a value on the software.

How can you come at this vis a vis our compatibility constraints?

GB:mik

Attachments

Distribution

Al Brown
Bruce Delagi
Larry Wade

cc: VAXC, John Leng

THE MYTH OF IBM APPLICATIONS SOFTWARE

IBM has a reputation of providing a lot of applications software, especially in the university environment. While there is a lot of software for the 360/370 series, most of it is not maintained by IBM, but by various Universities and other third parties.

The attached list describes software used at MIT's Information Processing Center. Note how little is IBM supported. Also, note that the IBM list includes two COBOL compilers, three FORTRAN compilers and three PL/1 compilers, but the STUDENT compilers: Assembler G, PL/C and WATFIV are all University products with NO IBM support.

Langua

COMPETITIVE

MI copy pages, 12, 13, 51.

~~(Ashley Grayson)~~

To: ~~HAXC~~ Lang, Wade, Bruce Delagi, Al Brown
cc: VAXC, Leng

Subject: P.Languages & Languages, Their State, ~~and~~ Investment, and

In order to get a better handle on our software investment, I feel we need to really assess the software we have on the 11, and ~~compare it~~ compare it with the 10, and other competitors. The 10 group did the attached; but we ~~really~~ need somethg as to size, investment, capabilities, etc. Each market, can then place a value on ~~it~~ the software.

- How can you come at this vis a vis our compatibility ~~strategy~~ to?

SOFTWARE	PRINCIPAL MAINTAINER	DEC-10 EQUIVALENT	MAINTAINER
MPSX	IBM	L.P.	Wooton Jeffries
ORTEP	None	ORTEP	None
PL/C	Cornell U.	None	None
PL/1-F	IBM	None	None
PL/1 Checkout	IBM	None	None
PL/1 Optimizer	IBM	None	None
P-STAT	Princeton U.	?	?
SIMSCRIPT	CAC, Inc	SIMULA	FOA
SLIP	None	LISP	Stanford U.
SNOBOL 4	Bell Labs	SITBOL	Stevens Institute
SPITBOL	Illinois Inst. of Technology	SITBOL	Stevens Institute
SPSS	U. of Chicago	SPSS	U. of Pittsburgh
WATFIV	U. of Waterloo	SITGO ?!	Stevens Institute

COMPETITIVE

Pascal

systems available on the DECsystem-10: SITBOL the Stevens' Institute interpreter and FASBOL a compiler available through DECUS. SITBOL on the 1040 runs about 2.7 times faster than Xerox SNOBOL on the SIGMA-9.

TEXT

TEXT is a feature by feature copy of IBM's ATS. It should be a plus for Xerox if the customer is commited to ATS but DECs editors such as TECO, SOS and VTED combined with RUNOFF provide a much more interactive system. Also DEC has TYPESET-10 and its friend ITPS which are much more powerful than TEXT. TEXT remember is oriented to IBM 2741 type terminals..nofill

Applications Software Checklist

A = available , D = DEC supported , X = Xerox supported U = under development

	Item	DECsystem-10	Xerox 560
	ALGOL-60	D	A
	ALGOL-68	U	
?	APL	D	X
RSTS	BASIC	D	X
	BAL (360/20,30)	A	
	BCPL	A	
	COBOL-68	D	X
	COGO	D	
	DYNAMO	A	
	FORTRAN	D	X
	fast FORTRAN	A	X
	GPSS	A	GPDS
	JOSS(AID)	A	
	JOVIAL	A	
	L*	A	
	LISP	A	A
	MATHLAB	A	
	NELIAC	A	
	OMNITAB	A	
?	PASCAL	A PL/1	
	POP-2	A	
	SIMULA-67	A	
	SL-1	CSSL(A)	X
	SNOBOL	A	A
	SNOBOL compiler	A	
	SPSS	A	
	1401 Simulator	A	X
	Pibol.	O	
	SAIL		

1328

INTEROFFICE MEMORANDUM

TO:	Lloyd Tucker	LOC/MAIL STOP PK3-2	
CC:	Dick Clayton	ML5/E71	
		DATE:	April 9, 1975
		FROM:	Gordon Bell
		DEPT:	OOD
		EXT:	2236
		LOC/MAIL STOP:	ML12/A16

DIGITAL EQUIP. CORP. RECEIVED APR 11 1975 ACCOUNTS PAYABLE

SUBJ: Signatory Authorization

Please enter signatory authorization as follows:

Cost Center	385	394
Location Code	MY	MY
Manager	R. Clayton	R. Clayton
Badge #	1590	1590
Advances	$500	$500
Business Expenses	$3,000	$3,000
Purchase Requisition (Expense)	$20,000	$20,000
Purchase Requisition (Capital)	$20,000	$20,000

The above 2 cost centers are in addition those he is already authorized for.

/ale

digital

April 16, 1975

Mr. William A. Wulf
Carnegie-Mellon University
Department of Computer Science
Schenley Park
Pittsburgh, Pennsylvania

Dear Bill:

Thanks a lot for the book. For now I've just thumbed through it. I'll be looking at it more carefully soon, as we are warming up for arguments for larger scale adoption of BLISS -- Larry Portner is pushing the fight this time, plus we have quite a lot of work (examples) in BLISS.

The type font looks good too. Hydra seems to be progressing nicely too; Sam's POE data points are significant. Is the coding versus time still linear?

Thanks,

Gordon Bell
Vice President, Engineering
Professor, Computer Science
Carnegie-Mellon University (on leave)

GB/mrg

DIGITAL EQUIPMENT CORPORATION, 146 MAIN STREET, MAYNARD, MASSACHUSETTS 01754
(617)897-5111 TWX: 710-347-0212 TELEX: 94-8457

Carnegie-Mellon University

Department of Computer Science
Schenley Park
Pittsburgh, Pennsylvania 15213
[412] 621-2600
[412] 683-7000

April 7, 1975

Hydra seems to be progressing nicely too; an significant. Sam's PDP-10 data points coding versus time

Is the coding still linear?

Mr. C. Gordon Bell
Digital Equipment Corporation
146 Main St.
Maynard, Mass. 01754

Dear Gordon:

Enclosed is a copy of a monograph which we just published on the Bliss/11 compiler implementation. It's not exactly a coffee table book, but we thought you might enjoy a copy.

Sincerely,

Bill

William A. Wulf

WAW/dmj
enc.

Dear Bill

~~I do like the type~~

Thanks a lot for the book. For now I've just thumbed through it. ~~Be~~ ~~I'll be looking at it~~ more carefully soon as we are warming up for arguments for larger scale adoption of BLISS — Larry Portner is pushing the ~~fight~~ fight this time, plus we have quite a lot of work (examples) in BLISS.

The type font look goods too.

Thanks
Gordon

digital

April 16, 1975

G. A. Michael
College of Engineering
University of California, Davis
P.O. Box 808
Livermore, California

Dear George:

Many thanks for the hospitality at LLL. I really enjoyed the interaction with the laboratory and the seminar.

The wine tasting was great, especially topped off with Heidi's dinner.

If possible, I'd like to get a copy of the video tape if it is any good. If you send one, I'll send a blank back or money. As a professor, I'd enjoy seeing Cray's tape too. I look forward to a return sometime.

I enjoyed the LLL graphs, but noticeably missing is a measure of MIPS, file storage, Kilo-core-seconds, printer output, teletypes, etc. which measures productivity, etc. If Sid has those, I'd be interested in having them.

Sincerely,

Gordon Bell
Vice President, Engineering
Professor, Computer Science
Carnegie-Mellon University (on leave)

GB/mrg

DIGITAL EQUIPMENT CORPORATION, 146 MAIN STREET, MAYNARD, MASSACHUSETTS 01754
(617)897-5111 TWX: 710-347-0212 TELEX: 94-8457

digital

March 11, 1975

1332

G. A. Michael
College of Engineering
University of California, Davis
P.O. Box 808
Livermore, California

Dear George:

I'll be able to spend all day at the Laboratory. I plan to arrive at 9:30 AM, as per plan I.

Sincerely,

Gordon Bell

Gordon Bell mjk
Vice President, Engineering
Professor, Computer Science
Carnegie-Mellon University (on leave)

GB:mjk

cc:

Dear George

Many thanks for the hospitality at LLL. I really enjoyed the interaction with the staff laboratory and the seminar.

The wine tasting was great, especially topped off along with Heidi's dinner.

If possible, I'd like to get a copy of the video tape if it is any good. If you send one, I'll send a blank back for mailing. Id enjoy having Gray's tape too. I'll forward to a return address.

DIGITAL EQUIPMENT CORPORATION, 146 MAIN STREET, MAYNARD, MASSACHUSETTS 01754
(617)897-5111 TWX: 710-347-0212 TELEX: 94-8457

UNIVERSITY OF CALIFORNIA, DAVIS

BERKELEY • DAVIS • IRVINE • LOS ANGELES • RIVERSIDE • SAN DIEGO • SAN FRANCISCO — SANTA BARBARA • SANTA CRUZ

COLLEGE OF ENGINEERING
DEPARTMENT OF APPLIED SCIENCE DAVIS-LIVERMORE

POST OFFICE BOX 808
LIVERMORE, CALIFORNIA

March 3, 1975

MAR 07 1975
3-10

Dr. Gordon Bell ML-12/A51
c/o Digital Equipment Corp.
146 Main Street
Maynard, Massachusetts 01754

Dear Gordon:

Many thanks for agreeing to take time to come here and give a seminar. Possible schedules for your visit are attached. We'll be prepared to adapt to any time constraints you may have.

After your talk - and again if you have time - we could adjourn to my place to "taste a few bottles of wine" and perhaps a snack or two.

On the question of parts from old LLL computers, I have advised Sid of your interest so I'm sure he'll want to discuss it with you.

A final comment for your amusement: Your talk is a very important component in a series of presentations given by acknowledged leading architects.

We got (through the kindness of Sid) Seymour Cray to talk about computer architecture. Next, you will view basically the same area - and I know - from a somewhat different point of view.

Later on Bob Noyce will come by and give a talk - so you see (ahem) three leaders in the industry will have commented on a very important field.

We got Seymour on videotape and I propose to do likewise for you - unless you object - don't worry about company private questions and so on - the tapes are not public and you will have editorial rights over them.

L mtg of 4/9
4/10 at LLL
4/11 Cosmos meet at SF airport

It would be helpful if you could let me know your preferences concerning the schedule so that I can set the appointment with Sid.

I'm really looking forward to your visit.

Sincerely,

George

G. A. Michael

GAM/njb
Enc.

POSSIBLE SCHEDULES

(April 10, 1975)

I) Arrive at the West Badge Office - A.M. (e.g. 9:30 am)

Computer Center Tour

10:30 Meet with S. Fernbach et al

11:45 Lunch

1:15 Meet with Computation Department Staff

2:30 Reserved for quiet time

A- 3:30 Give talk

4:45 - 5:00 Finish

5:00 + Possibly adjourn to wine tasting etc.

II) Arrive at the West Badge Office - P.M. (e.g. 1:00 pm)

1:00 Computer Center Tour

2:00 Meet with S. Fernbach et al

3:00 Quiet time

3:30 Go to IA

digital

February 17, 1975

Mr. George Michaels
Computation Group
Lawrence Livermore Laboratory
Livermore, California 94550

Dear George:

I'm glad you invited me to talk at LLL, and look forward to seeing the laboratory again. I hope I'll have time to see various facilities, and to interact with you about where you think computation is headed. I hope Dr. Fernbach will be available for some discussion. The abstract of a talk is enclosed, which gives a view of this.

I'm in the process of collecting parts from past computers, such that we might someday have a museum at DEC. Is there any chance of getting parts from some of the machines LLL has used and/or spawned--especially LARC, the CDC machines and Stretch?

Sincerely,

Gordon Bell
Vice President, Office of Development
Professor, Computer Science
Carnegie-Mellon University (on leave)

GB:mjk

Enclosure

DIGITAL EQUIPMENT CORPORATION, 146 MAIN STREET, MAYNARD, MASSACHUSETTS 01754
(617)897-5111 TWX: 710-347-0212 TELEX: 94-8457

digital INTEROFFICE MEMORANDUM

TO: Dick Devlin

CC: Win Hindle
John Leng
Nat Teichholtz

DATE: April 18, 1975

FROM: Gordon Bell

DEPT: OOD

EXT: 2236 LOC: ML12/A51

SUBJ: PDP-15 AND NETWORKS

Let me urge you to fund nets immediately.

Bob Schoenfeld (Rockefeller U.) suggested this, and he's absolutely right.

Since I don't understand your priorities, etc., I would place it at the top...above a faster CPU. This is the way to bring 15's back in the family, and show we're not deserting the users.

Networks were judged the hotest thing at DECUS--and I concur.

GB:mjk

D I G I T A L INTEROFFICE MEMORANDUM

SUBJ: NETWORKS ANNOUNCEMENTS

DATE: Ø4-22-75
FROM: GORDON BELL
EX: 2236
MS: ML12-1/A51

TO: FILE

To: Distribution

Congratulations on a successful announcement and demonstrations, for what I believe will be possibly our most significant product, Networks are not only a significant technical accomplishment, but are complex organizationally since they add one more dimension to our matrix organization.

Our users at DECUS clearly recognize it as truly significant too. The first level of documentation looks good.

It is also an interesting by-product that DDCMP is attracting attention (at NBS, BTL, and Canadian Bell) as the possible communication standard.

We've still got lots to do, including installations which will not be easy, but things are off to a good start.

GBimjk

Distribution

Dave Cutler
John Gilbert
Jose Garcia
R. L. Pitcher
Don Reinke
Frank Hassett
John Holmes
Stan Pearson
Nat Teichholtz
Pete Van Roekens
Stu Wecker
Mike Weinstein

cc: OC, PLM, Larry Portner

D I G I T A L INTEROFFICE MEMORANDUM

SUBJ: MINI-MACRO RUMORS
DATE: 04-22-75
FROM: GORDON BELL
EX: 2236
MS: ML12-1/A51

TO: FILE

SUBJ: RANDOM MINI-MICRO RUMORS AT ANNAPOLIS CONFERENCE, CLASSIC 8008 and MICROCOMPUTER LANGUAGE STANDARDIZATION: PL/M?

To: Distribution

One of the key developers of PL/M for the Intel 8080 is Prof. Gary Kildall, U.S. Naval Postgraduate School, Monterey, California. He is busily putting PL/M on other micros and the PDP-11. He stated that the semiconductor companies are really interested in standardizing on PL/M so that users can easily code, and get the functional isolation from specific computers. Also, the semis can sell systems without getting bogged down in the system programming morass that we have so carefully created. They are apparently meeting on the subject...with standardization semis in mind.

This is in stark contrast to our diehard position of programming in assembly language. The smart micro users are clearly moving to PL/M for higher level language systems programming. Thus, our software base can be small, compared to Intel's, if their user development base increases rapidly; and it can if they can keep the system understandable and increase productivity.

Kildall is transferring PL/M to the PDP-11. He wants to supply it to us, when available. He also wants to establish contact to get LSI-11, and to do benchmarks vis a vis other micros.

The irony of PL/M is that if it does get heavily used, it can be more hardwired, and in principle really compete with a very fast mini. Intel, I believe, is taking this position. Note, that the base machine can be changed a lot, without affecting the user--something we've not been able to do...or try until the current implementation of BLISS 10 which we hope to transfer to the 11.

CLASSIC 8080

Kildall also showed slides of interaction with his system using a 16K byte 8080, 2 floppies, and a CRT (note=CLASSIC 8). The

SUBJ: MINI-MACRO RUMORS DATE: 04-22-75
FROM: GORDON BELL

console commands he implemented were those of PDP-10 to get the 10 documentation, and also because he felt TOPS 10 is the best command language (note RT-11, and OS-8 are nearly identical). Question: Pat White, why are we trying to get another command language for IAS and VIROS (SNARK) when we have a good one already, and there is no reason to believe that command languages are better? to obsolete all monitors? to confuse user? as a technical challenge?

Again, this monitor is relatively simple as is OS-8 + RT11 (about 4-5K bytes) and written in PL/M. The cost of parts to him in unit quantities: $4000.

Altair 8080 and Low Cost Computing

The above, boxed and hit form machine which sells in the $400-$800 range is apparently selling like hot cakes. (They have 3000 orders.)

Roy Moffa/Steve Teicher: Is the LSI-11 bus such that we can sell 8080's, Motorola, LSI-11, etc, CPU's, and go after the module/box/options business like the initial charter?

GBimjk

Distribution

Bob Bean
Jim Bell
Al Brown
John Clarke
Andy Knowles
Carmen Mastropieri
Keith Miles--California
Roy Moffa
George Plowman
George Poonen
Larry Portner
Mark Sebern
Charlie Spector
Mike Soler
Steve Teicher
Pete Van Roekens
Larry Wade
Pete White
Mel Woolsey
cc: Ken Olsen

D I G I T A L INTEROFFICE MEMORANDUM

SUBJ: MICROPROCESSORS
DATE: 04-22-75
FROM: GORDON BELL
EX: 2236
MS: ML12-1/A51

TO: FILE

SUBJ: MICROPROCESSORS--WILL WE MAKE IT?

To: Distribution

I believe we might get together on the above topic for a free-form discussion. Frankly, I'm concerned.

Some concerns (no particular order):

1. We're locked into LSI-11 and backup--a relatively expensive microprocessor.

2. We don't yet have LSI-11, while others are delivering other machines. They are now working on next generation (I²L, bipolar)?

3. We could "package" all/any microprocessor--to achieve lowest price.

4. A high level programming language PL/M just may evolve to be the standard--not a machine language.

5. The semiconductor computer people look much brighter to me vis a vis higher level languages, multiprocessors, and working hardware systems problems.

6. CLASSIC 11 (?) at a low price is doable--note, a customer built one for $4K in unit quantities, yet our goals are only $3K--about the cost of a CLASSIC 8.

7. Should we try to become substantially or totally independent of CPU by using higher level languages for systems programming?

8. There are several possible CLASSIC 11's: Andy and Steve's, Len Hallo's, Bob Lane's, and Tom's. Who's doing what?

9. We're fooling around designing our own special micro-controller instead of something we sell.

10. A small company starts up and gets orders for 3000 Intel 8080's in a boxed configuration

SUBJ: MICROPROCESSORS

DATE: 04-22-75
FROM: GORDON BELL

Are there any real issues here, or do I just not understand the "plan"?

Can a few of us get together to discuss this low end?

GBimjk

Distribution

Andy Knowles, Steve Teicher
cc: John Clarke, Dick Clayton, Lorrin Gale, Henry Lemaire, Ken Olsen, Larry Portner, Bob Puffer

D I G I T A L INTEROFFICE MEMORANDUM

SUBJ: MAGNETIC BUBBLE MEMORY

DATE: 04-22-75
FROM: GORDON BELL
EXT: 2236
MS: ML12-1/A51

TO: FILE

To: Jim Hogan

I believe the magnetic bubble memory has promise, but question whether the University of York can advance what seems to me to be fundamentally a materials/production problem. They should proceed however. I would encourage them to work on the organization with respect to how it would be used in a computer. Their proposal was clearly a replacement to a fixed head disk, and as such was too expensive. Also, their costs in Fig. 1 look totally wrong; I believe they should do some more checking vis a vis trade magazines, etc. The performance needs to be much higher in order to get it into the memory hierarchy.

Regarding your questions; my opinion:

1. No.

2. No. It's even in trouble with respect to semiconductors. It has to be at least a factor of 2 lower in price and no worse than 100 in performance...

3. No. This is ridiculous for a university to worry about. They can simply look at projected costs of semiconductors and disks--the competitors they are trying to displace.

4. It is probably better at higher end. The mini really doesn't need it that much.

5. Disks have improved in density at about 40%/year. Their costs are too high initially, grow relatively the same, hence won't catch disks. (Actually, they probably will, but by a more radical price and performance improvement.)

6. I don't understand their model for projection of performance. If the bubble density is totally locked to magnetic recording density, then there may be a problem of the bubble really ever replacing a disk.

I certainly appreciate the thought going into this research, and would enjoy keeping in touch with it. I've sent copies of

SUBJ: MAGNETIC BUBBLE MEMORY DATE: 04-22-75
FROM: GORDON BELL

your query to others working in this area. If they disagree with my comments, they're free to write.

GBimjk

cc: Brian Croxen, Grant Saviers, Mark Sebern

Mr (Bulmer) Circulate (copy if you wish), and Ken

cc: Sawers, Crossen, Scherr

1345

MEMORANDUM TO: GORDON BELL
VICE PRESIDENT ENGINEERING

FROM: JIM HOGAN - LEEDS UK

RE: UNIVERSITY OF YORK
BUBBLE MEMORY RESEARCH PROJECT

G Bell 4/29 1975

Thank you for your telex NA28 asking for details of the Bubble Memory Research Project being conducted at the University of York.

At the stage currently reached two objectives are being pursued:-

1. Assessment of production costs.

2. Assessment of probable demand, taking into account the affect of the appearance of bubble memories in the market place on conventional disc devices.

Apparently plenty of information is available to meet the first objective. We have been approached for our views to help meet the second.

A copy of the paper describing the project is enclosed. The specific questions put to us are as follows:-

1. A bubble memory controller is simpler and less expensive than an equivalent capacity disc controller. Would $500 per 2 million bits appear excessive or reasonable? No.
$\frac{\$500}{2\times10^6} = \$.000250$ /bit
250×10^{-6}
2. Does the module described appear to offer an attractive alternative to present discs and those likely to be available in two/three years time? It is expensive and slow & appears to be in trouble via a via semiconductor mag.
3. Can we attempt a forecast of likely demand, worldwide, in the U.S.A., Europe, U.K.? no — I wouldn't worry about this now.
4. The module was designed with mini computers in mind. Does it appear to have potential for data processing in other areas? It is probably more effective on large machines where more staging is required.
5. Conventional discs will be the main competitors of bubble memories. Since the development costs of discs will by now have been written-off, how much might disc prices be expected to fall in the face of serious bubble memory competition? (e.g. 10%? 20%? 50%?) — Disks decline, at about 20% + 40% / year.
6. Bubble memory module capacity of the type described is projected to increase by factor of 2 over two years and by a factor of 10-50 of slower designs over five years.

Same as disks — Are there differences in densities, or are they locked together via size of domain wall?

/contd

Access times are projected as decreasing by a factor of 5-10 over three years. good .

Can we comment on how these possibilities are likely to affect demand for conventional memories, particularly discs.

Any assistance you can give on these points, without encroachment unduly into your timetable, would be greatly appreciated.

Yours,

Jim Hogan

BUBBLE MEMORY MODULE - DATA SUMMARY

Capacity	- 2, 4, or 6M bits.
Physical Size	- 13.5cm by 5.5cm by 2.0cm.
Natural Word Size	- 8, 16, 32 bit.
Access Time to Any Word	- 5.12 to 6.40 milliseconds.
Transfer Per Cycle	- 8k bits.
Transfer Rate	- 3.2M bits/sec.
Production Cost	- $2000 approximately.
Production Cost to M Bit Controller	- $500 approximately.

$\frac{\$2500.}{2}$

$\$.001250$ /bit

Several modules might be connected to a suitable controller; switching time between modules would be approximately 10 microseconds.

attachment too-light to film.
filed under - M. bubbles

digital

D I G I T A L INTEROFFICE MEMORANDUM

SUBJ: SYSTEMS, ETC.
DATE: 04-22-75
FROM: GORDON BELL
EX: 2236
MS: ML12-1/A51

TO: FILE

CONFIDENTIAL--DO NOT REPRODUCE

SUBJ: SYSTEMS, STANDARDS, ARCHITECTURE, ETC.

To: Distribution

I've been recommending UNIX on larger 11's for a large buyer interested in a range of machines, who had to justify total cost, not purchase cost. IBM might be a first choice, or MODCOMP-IBM or Interdata-IBM also are possibly in the running. I believe we are in the business of building and rebuilding low end tools, and will never get around to good languages and applications because we operate at very low levels.

It is very clear to me that, in extending UNIX 11, we have to have tighter control of specs, and some notion of "top-down" planning.

Some things that bother me:

0. The hardware among machines and options is pretty incompatible!

1. We have moved to a substantially more incompatible position over the last 2 years (see attached memo).

2. there is even incompatibility vis a vis RSX's.

3. The BASIC's (our specialty) are incompatible.

4. We go off an invent a command language (incompatible with all past CL's), which now no one wants. (Thank goodness--because we have a pretty good one in RT/OS/TOPS.

5. The compatible systems: RT11, OS8, and TOPS 10 are all incompatible.

6. Even TECO is different across machines.

7. R EDIT (see 5) brings in 3 radically different editors.

SUBJ: SYSTEMS, ETC. DATE: 04-22-75
FROM: GORDON BELL

8. PIP is different.

9. Networks had (are having) many problems in implementation, due to notion of adhering to specs.

10. I was promised some compatibility. I see some.

11. Etc. Etc.

We are not making effective use of our development $, because all systems are different, and have to be redone at a low level. Hence, we never get to pushing high level functions.

In the concern about 11VAX: software and the degree of compatibility are paramount. Now we have 4 or 5 independently evolved systems, each starting from ground level, and not growing very tall...because they don't build on each other.

We have to get together to discuss this, after 2 years of promises, concerns. I want a plan...or know why I can never get one.

GB:mjk
Distribution

Dick Angel
Al Brown
Dick Clayton
Pete Conklin
Bruce Delagi
Bill Demmer
Ed Fauvre
Clay Neal
George Plowman
Larry Portner
Nat Telchholtz
Pete Van Roekens
Larry Wade
Pat White
Mel Woolsey

D I G I T A L INTEROFFICE MEMORANDUM

SUBJ: RSX POSITION AT DECUS; IAS

DATE: Ø4-22-75
FROM: GORDON BELL
EX: 2236
MS: ML12-1/A51

TO: FILE

TO: Distribution

Apparently we looked like idiots at DECUS re our position of M versus D with rhetoric and an inconsistent party line from our product managers and development people. The D customers seem to feel we're pulling another DOS pull-out on them.

Can you send me a position on this? What happened at DECUS--your interpretations? Why not extend M upwards? All indications I get on D are bad--no understanding of why it performs poorly.

I get no good vibes on IAS--i.e. we're not using it especially internally. Already, we have committed cardinal sin "Ø"--announce before understand and use of a high technology product.

It would be useful if a few of us could get together to understand what's going on here. Let me know what the policy is and why the poor DECUS show.

Have software PSG's been abandoned?

GBimjk

Distribution

Dick Angel
Clay Neal
Larry Wade
Mel Woolsey

CC: Dave Cutler, Bernie LaCroute, John Leng, Larry Portner, Garth Wolfendale, Pete Van Roekens

digital INTEROFFICE MEMORANDUM

TO: Al Brown

CC: Mel Woolsey

DATE: April 28, 1975

FROM: Gordon Bell

DEPT: OOD

EXT: 2236 LOC: ML12/A51

SUBJ: PL/1 at PONTIAC MOTORS (GM)

Will you please call Mr. Elson Spangler, 313-857-1739.

He would like to give a formal input to us regarding PL/1, and possibly review our first spec.

They would also be worth visiting.

GB:mjk

SUBJ: LA181 VERSUS LA120 DATE: 04-28-75
FROM: GORDON BELL
EX: 2236
MS: ML12-1/A51

TO: FILE

TO: ED CORELL, AL HOEFFNER

CC: MARKETING COMMITTEE, DDD

I AM UNHAPPY ABOUT THE WAY WE DECIDED THE LA180 VERSUS THE LA120 (SERIAL). I VIEW IT AS A NON-DECISION. THE ONLY DAY I THOUGHT YOU MAY HAVE BEEN POSSIBLY RIGHT WAS WHEN ANDY EMITTED A WEAK SIGNAL THAT WE MIGHT WANT TO SELL LINE PRINTERS AS ADD ONS IN THE CENTRONICS MARKET. (THIS DIDN'T MATERIALIZE AS I'M AWARE.) THE CENTRONICS MARKET WILL MIGRATE TO SERIAL COMMUNICATIONS ANYWAY.

THE LA120 APPROACH:

0'. AN LA120 COVERS THE LA180 FUNCTION IN EVERY DIMENSION.

1'. IT RUNS SLOWER (ALTHOUGH WE COULD HAVE A BASTARD VERSION) AND HENCE HAS LONGER HEAD LIFE.

2'. IT IS A WAY TO IMPROVE THE MARGINS ON THE LA36 BY BEING DISPROPORTIONATELY HIGHER IN PRICE.

3'. IT WILL ALLOW PEOPLE BUYING THE LA120 A COMBINED LINE PRINTER/TERMINAL.

4'. IT PROVIDES A BETTER, MORE RELIABLE SYSTEM BY REDUCING THE UNIT UNIBUS LOADS AND HAVING A MORE ROBUST INTERFACE (SERIAL VERSUS PARALLEL). WE WANT TO GET ALL THE LOW SPEED PERIPHERALS OFF THE UNIBUS.

5'. IT ALLOWS OUR USERS TO GET MUCH MORE WORK DONE BY GIVING A LARGER NUMBER OF THEM HIGHER SPEED TERMINALS NOT A FEW CENTERED AROUND THE NOW, MORE UNRELIABLE COMPUTER.

6'. IT GIVES US SOME BIT OF UNIQUENESS IN THE TERMINALS MARKET, ASIDE FROM A LOW PRICE (THAT WE LOSE MONEY ON) BY HAVING SPEED. TERMINAL BUYERS WILL PROBABLY MIGRATE TO HIGHER QUALITY (AT SAME SPEED) OR SMALL SIZE OR QUIETNESS.

7'. A SUBSTANTIAL NUMBER OF OUR SYSTEM PRODUCTS ARE

SUBJ: LA130 VERSUS LA120 DATE: 04-28-75
FROM: GORDON BELL

MULTI-TERMINAL (I.E, RSTS, IAS, RSX, MUMPS, MULTI TERMINAL RT-11 F/B, ALL EDU SYSTEMS, TSS/8, AND TOPS 10, SNARK), HENCE, REQUIRE LOTS OF TERMINALS, A PRINTER GETS US A SALE, A SERIAL APPROACH SELLS MULTIPLES OF THESE; WHEREAS, A LINE PRINTER IS RESTRICTED TO LOCAL (HENCE 1 PER SYSTEM),

8. YOU WILL HAVE COMPETITORS FOR HIGHER SPEED QUITE SOON, IT FOCUSSES ON A TIDY SET OF TERMINALS, AND NOT FRAGMENTING US INTO A NEW THING, IT GETS RID OF THE LA180 (1 PRODUCT), THE LA120 IS INEVITABLE UNDER INCREASING TERMINAL SPEED COMPETITION (E.G, GE AND OTHERS USING ACUPUNCTURE PRINTERS),

THE ONLY REASONS I CAN FIND FOR DOING IT:

1. WE MUST HAVE DONE THE ENGINEERING ALREADY, AND IT MAY BE SLIGHTLY EASIER TO DO,

2. BY SOME WARPED VIEW, PEOPLE BELIEVE THAT AN RO VERSION IS DIFFERENT THAN A KSR,

3. IT WOULD IMPACT OUR SALES OF LA36,

UNDER THIS SCHEME THE LOW END USER WOULD NEED BOTH A LINE PRINTER AND AN LA36, INDEED, HE WILL PROBABLY ONLY USE THE LA36 IF HE'S THAT PRESSED FINANCIALLY (ACTUALLY, HE'LL PROBABLY GET A COMPETITOR HIGH SPEED TERMINAL),

THIS IS A CLASSIC CASE OF REALLY NOT DECIDING, BY BUMBLING ALONG ON WHAT I BELIEVE IS A BAD, DULL COURSE, IT WAS ONLY APPROVED BECAUSE PEOPLE WERE NOT REALLY GIVEN THE CHANCE TO DECIDE BECAUSE YOU PEOPLE DID NOT FRAME THE QUESTION,

CAN YOU PLEASE LOOK INTO THIS ALTERNATIVE, BECAUSE RIGHT NOW I BELIEVE WE ARE DOING IT WRONG, I ALSO BELIEVE THE MARKETING COMMITTEE MIGHT INSIST ON RETHINKING THIS ISSUE,

GB:MJK

D I G I T A L INTEROFFICE MEMORANDUM

SUBJ: THESIS TOPIC

DATE: 04-28-75
FROM: GORDON BELL
EXT: 2236
MS: ML12-1/A51

TO: FILE

SUBJ: HANDY THESIS TOPIC THAT WE NEED SOME WORK DONE ON

TO: DISTRIBUTION

I MET ONE OF DAN SIEWIOREK'S STUDENTS AT CMU ON FRIDAY, HE APPEARS TO BE A VERY BRIGHT ELECTRICAL ENGINEER WHO HAS A MASTER'S DEGREE AND IS ON LEAVE FROM LOS ALAMOS, WHERE HE WORKED FOR 3 YEARS IN VARIOUS PARTS OF COMPUTING AND IN SEMICONDUCTOR RESEARCH. THIS YEAR HE QUALIFIED FOR HIS PHD IN THE ELECTRICAL ENGINEERING DEPARTMENT AND IS VERY AGGRESSIVELY TRYING TO OBTAIN A PHD IN ONE MORE YEAR.

HE HAS TAKEN A LOT OF THE COMPUTER SCIENCE COURSES THIS LAST YEAR AND REALLY HAS NO MORE COURSE WORK. THEREFORE HE WANTS TO LOCK ONTO A PROBLEM AND TO COMPLETE HIS THESIS AS QUICKLY AS POSSIBLE. DO WE HAVE A HANDLY TOPIC FOR HIM?

HE IS GOING TO VISIT US WITHIN THE NEXT 2 OR 3 WEEKS. I BELIEVE HIS NAME IS BRANTLEY.

GB/HJK

DISTRIBUTION

JIM BELL, MARK SEBERN, BILL STRECKER, STEVE TEICHER

D I G I T A L INTEROFFICE MEMORANDUM

SUBJ: HARP

DATE: 04-28-75
FROM: GORDON BELL
EX: 2236
MS: ML12-1/A51

TO: FILE

SUBJ: HARP, A FAST PROCESSOR THAT ATTACHES TO THE UNIBUS FOR SIGNAL PROCESSING, ETC.

TO: ED KRAMER

THE SPEECH GROUP AT CARNEGIE-MELLON, HEADED BY RAJ REDDY, IS IN THE PROCESS OF BUILDING (NOW BEING SIMULATED) A HIGHLY SPECIALIZED PROCESSOR THAT ATTACHES TO THE UNIBUS. THEY HAVE BEEN USING AN SPS 41, BUT IT IS EXTREMELY DIFFICULT TO PROGRAM. THEIR PLAN IS TO MAKE IT IN A HIGHLY SPECIALIZED WAY, AND I HAVE SUGGESTED THEY MAKE IT IN SUCH A WAY THAT IT WOULD BE POSSIBLE FOR US TO PRODUCTIZE IF WE ARE INTERESTED, BY MAKING IT WITH OUR ECL RULES, AND BY MAKING IT ON HEX MODULES, ALA THE KL10.

THERE ARE ABOUT 400 ECL CHIPS INCLUDING 2K X 16 OF BIPOLAR AND 128 WORDS OF ECL MEMORY. IT IS PIPELINED WITH 3 STAGES TO GIVE AN EFFECTIVE INSTRUCTION TIME FOR STREAMED DATA OF 30NS. I HAVE LOOKED AT THE DESIGN FROM A CURSORY STANDPOINT, AND BASED ON THE KL10 SPEED, BELIEVE THEY CAN ACHIEVE THIS GOAL.

THE MACHINE ARCHITECTURE IS ATTACHED AND IS DESCRIBED IN ITS SEQUENTIAL (NON-PIPELINED FORM).

THEY ARE QUOTING SOME PRETTY FAST TIMES. I BELIEVE THAT A KL10 COULD BE MICROCODED TO GIVE FAIRLY IMPRESSIVE TIMES TOO, BECAUSE THE PROBLEM OF STREAMLING THE DATA IS DONE IMPLICITLY IN KL10; WHEREAS THIS MACHINE AND THE HOST 11 HAVE TO DO IT. ALL IN ALL, THEY ARE GOING TO BUILD IT, AND I HOPE THAT SOMEONE FROM DEC COULD INTERFACE WITH IT TO BENEFIT BOTH GROUPS.

I DON'T THINK IT TAKES A COMMITTMENT ON OUR PART, BUT I WOULD BELIEVE THAT SUCH A DEVICE MIGHT BE A WELCOME ADDITION FOR THE LABORATORY WHERE HIGH DATA RATES ARE INVOLVED, HENCE, I HOPE WE CAN FOLLOW IT, AND INTERACT WITH THEM. WHAT YOU THINK? WHO WOULD INTERACTION BE WITH?

GB:MJK

CC: GARY BUDIANSKY, ALAN KOTOK, JESSEE LIPCON, MARK SEBERN, ALLAN WALLACH

D I G I T A L INTEROFFICE MEMORANDUM

SUBJ: [illegible] MINUTES DATE: 04-28-75
FROM: DICK CLAYTON
EX: 3638
MS: ML5-2

TO: FILE

SUBJ: MINUTES OPD STAFF--4/24/75

Present: Bell, Clayton, Laut, Lemaire, Puffer

Guests: Abbett, Sims, Courtney, Siekman, Delagi, Gray, Wade, Cutler, Merrill, Nicoud

EEO: Sims, Courtney, Abbett

Topic was a discussion of the current status of Corporate EEO activity. The results of the OPD EEO audit and its relationship to realistic guidelines based on the local employment pool will be available from Mark in early May. John emphasized the need for forceful inclusion of EEO goals as part of the reward criteria for managers at all levels. The improved career mobility of all minorities (especially females) was presented as a major focus for the remainder of this year and most of next.

A skills inventory questionnaire will be executed for minorities and females by the end of the fiscal year.

STANDARDS: Gene Jordan

Gene and Jon presented an overview of the strategy for more formally including consideration of/and compliance with various international standards (mostly European). Gene will establish a staff oriented librarian of the various relevant international standards. The responsibility for design and testing will remain with the project (such as current UL and Canadian standards). It is expected that specific activities will have to be funded in Europe to understand the real standards and submit specific products for approval. These activities will be funded via a 07-xxxx project, managed by Gene and probably done by CSS in UK and Germany.

SAFETY: Ron Minezzi

Ron and Gene briefly discussed the need for a serious focus on product liability and safety issues in Europe. Ron will establish an activity (probably within Geneva Headquarters

SUBJ: [illegible] MINUTES DATE: 04-28-75
FROM: DICK CLAYTON

Field Service),

MIT COURSE ON MANAGEMENT OF R&D AND INNOVATION

Gordon presented a view that we need to focus more on creativity and prototypes; Bob provided some input on the probably course content based on his experience with some of the people, Bob is to learn some more about the exact course content and recommend specific participation (probably one or two senior development managers)

PATENTS

A presentation of 11/45 related patents was made to Dave Cutler, Bruce Delagi, Bob Gray, and Larry Wade,

TINY TERMINALS: Cloud

A presentation of a prototype KBD, microprocessor display, cassette terminal was made, It looked neat, the key question is how to infuse the various good concepts into many of our ongoing and future projects.

RC:mjh

D I G I T A L INTEROFFICE MEMORANDUM

SUBJ: DDD AGENDA DATE: 04-28-75
FROM: DICK CLAYTON
EX: 3638
MS: ML5-2

TO: FILE

SUBJ: DDD STAFF MEETING AGENDA--MAY 1, 1975

10:30	Responsibilities of DDD members (Ken's memo attached)	DDD
11:00	Job responsibility statements from DDD for Product Managers (Invite Hewett/Cronkite)	Clayton/Puffer/ Portner
11:30	LSI Engineering Goals, Resource allocation, Projects (Written material to be distributed)	Gale
12:15	Status report on 32 bit project	Ball

FUTURE AGENDA ITEMS

Date	Topic	Responsible
5/8	Jobs outline, goals, schedule 30 min	Portner
5/8	Department's white paper on testing Open discussion of software system, hardware, Field Service, Mfg, roles and potential changes in pressure on goals of various groups and the company 1 hour	DDD
5/8	Status of Corporate Packages (Written material ahead of time) 30 min	Puffer/Clayton
Q4	Production Communication	Cudmore/Smith
?	Communication Interface with hardware and software	Marcus et al
?	2x2 Reporting	Puffer
Jungle--Effective Systems; How do we do it?		DDD

digital

April 29, 1975

Peter Weiner
Head
Information Sciences Department
RAND
1700 Main Street
Santa Monica, California 90406

Dear Peter:

If you have any JOSS consoles, they'd be worthwile. A photo would suffice, or manual. I'd like to get manuals of Johnniac, JOSS 1, and JOSS (for PDP-6).

Photos of Johnniac would be fine. Photos of plug-ins and its construction will have to suffice. Where would I get a single plug-in?

Sincerely,

Gordon Bell

Gordon Bell mjk
Vice President, Office of Development

GB:mjk

DIGITAL EQUIPMENT CORPORATION, 146 MAIN STREET, MAYNARD, MASSACHUSETTS 01754
(617)897-5111 TWX: 710-347-0212 TELEX: 94-8457

1370

Rand
SANTA MONICA, CA. 90406

PETER WEINER
Head
Information Sciences Department

9 April 1975

APR 14 1975
C-32

Dr. Gordon Bell
Vice President
Office of Development
Digital Equipment Corporation
146 Main Street
Maynard, MA 01754

Dear Gordon:

I have asked around Rand about parts for your museum. Unfortunately, only photos of the JOHNNIAC remain. The only other item of possible interest would be the Rand-developed Keyboard used on the PDP-6 JOSS system.

Let me know what you need (i.e. how many photos, etc.) and I'll get all put together.

Sincerely,

Peter

PW:nc

Mr Peterson

If you have any JOSS consoles, they'd be worthwhile. A photo would suffice, or manual. I'd like to get manuals of Johnniac, Joss 1, and Joss (for PDP-6)

Photos of Johnniac would be fine. ~~If possible I'd like to get a plug-in~~. Photos of plugins and its construction will have to suffice. ~~Is there a way~~ When would I get a single plug-in?

D I G I T A L INTEROFFICE MEMORANDUM

SUBJ: PROF. NICOUD'S PAPERS DATE: 04-29-75
FROM: GORDON BELL
EX: 2236
MS: ML12-1/A51

TO: FILE

SUBJ: PROF. NICOUD'S PAPER REPRINTS

To: Distribution

I am transferring all of the file of papers I have from Prof. Nicoud to the library. Let me particularly recommend papers from him in the event that you were unable to see some of the demonstrations this last week on his hardware.

MICROPRERIPHERALS--In this paper he describes a bus structure for microcomputers that will take both the Intel 8080, the Fairchild F8, and the Motorola on the same bus; and he has a very interesting interconnection scheme which minimizes chip cost. In fact, in contrast, he has built a display system around the 8080 which uses one half the chips that our VT51 uses to accomplish exactly the same function (and these designs were done with exactly the same technologies).

HARDWARE CHARACTERISTICS OF MICROPROCESSORS--more on the interface system for microprocessors as previously described. Should we be looking at such a bus scheme so that we can simply use any random microprocessor and supply peripherals for it in a standardized way?

HARDWARE CHOICES FOR MICROPROCESSORS--an evaluation criteria for microprocessors.

HARDWARE STANDARDS FOR MICROPROCESSORS--another set of on the bus structure.

MODULAR LOGIC ELEMENTS--MICROPROCESSORS AND PERIPHERALS IMPROVE EFFICIENCY IN TEACHING AND DEVELOPMENT--describes a breadboard system for quickly interfacing to both minicomputers and to microprocessors.

COMMON INSTRUCTION MNEMONICS FOR MICROPROCESSORS--a scheme for easily cross assembling a number of machines. Note, that he is also considering PASCAL as a base language for converting across machines of different manufacturers. By the way, PLM is also being considered.

SUBJ: PROF. NICOUD'S PAPERS

DATE: 04-29-75
FROM: GORDON BELL

INCREMENTAL MOTION CONTROLS--application of synchronous motors to drive floppy disk. This is a paper by Jufer and Cassat in which they explore both stepping motors and regular induction motors for driving a floppy. They are compared using various criteria.

GB:mjk

Distribution

Jim Bell
Ed Corell
Mimi Cummings
Lorrin Gale
Len Hallo
Andy Knowles
Mike Lies
Rick Merrill
Roy Moffa
Bob Peyton
George Plowman
George Poonen
Bob Puffer
Mark Sebern
Mike Spier
Tom Stockebrand
Steve Teicher
Rob Vannaarden
Chuck Youse

D I G I T A L INTEROFFICE MEMORANDUM

SUBJ: LCC LANGUAGE

DATE: 04-29-75
FROM: GORDON BELL
EXT: 2236
MS: ML12-1/A51

TO: FILE

To: Distribution

I just picked up copies of a manual on LCC language that Allan Perlis put on me--360/67 a computer under TSS in 1970. There is both a reference manual and a users manual. Although the language doesn't have particularly unique features in it (it does have some that are not widely used, e.g. the automatic typing of variables as they are used), It does have other interesting properties, e.g. able to save the state of the system conveniently. For this, one pays a relatively high overhead price.

The manuals are in the library.

Bill Wulf's book, the design of an optimizing compiler by Elsevier, Computer Science Library, is also out. I have a copy, and will loan it, but it probably should be ordered for the library.

GBimjk
Distribution

Norma Abel
Ron Brender
Al Brown
Mimi Cummings
Jim Mills
George Plowman
John Xenakis

April 30, 1975

Dr. Craig Fields
ARPA
1400 Wilson Boulevard
Arlington, Virginia 22209

Dear Dr. Fields:

Enclosed please find the revised version of our proposal for a personal computer system capable of interpreting the PDP-10 instruction set.

As we discussed on the phone, Section 4.4 is now revised to say that Digital will provide ARPA with equipment rather than cash if we terminate.

We have also made some other changes. As we also discussed on the phone, Section 2.1 of the previous version referencing the virtual address space extension has been deleted. Similarly, Section 3.1.5.4 of the previous version relating to the multipoint serial bus controller has been deleted since our plans do not now include such a feature.

Section 3.1.5.5 has been revised to say that the majority, but not all, of the IC packages will be commercially available. We envision that some of these will be custom to Digital.

Some other changes have been made in Section 4.3. This section now also refers to confidential information which Digital may disclose. The paragraph providing ARPA license rights has been somewhat revised and is now more specific. We feel that these changes are reasonable and hope you concur.

I believe the proposal is now in order and we await your decision. Please feel free to call me or Bruce Delagi at any time if you have any questions. You have my home phone, and Bruce's is (617) 448-6548.

Sincerely,

/Gordon Bell
Vice President
Engineering

cmg
Enclosure

bcc: Bruce Delagi, Tom Siekman, Bob Walsh

digital INTEROFFICE MEMORANDUM

TO: OOD

CC: Ken Olsen

DATE: May 6, 1975

FROM: Gordon Bell

DEPT: OOD

EXT: 2236 LOC:ML12/A51

SUBJ: PRESENTATION OF OOD/PRODUCT MANAGEMENT TO DEC BOARD

Ken would like us to present the organization, its operation, and product management structure to the DEC Board on June 9.

While this date has been postponed for now, it should be sometime in the near future. The object is to use this forum to clarify our thinking as to how things work.

GB:mjk

digital INTEROFFICE MEMORANDUM

TO: George Bundy
Andy Knowles
Steve Teicher
Mike Titelbaum
Rob Van Naarden

DATE: May 2, 1975

FROM: Gordon Bell GB

DEPT: OOD

CC: Dick Clayton, Ken Olsen

EXT: 2236 LOC: ML12/A51

SUBJ: CONGRATULATIONS

Please accept my heartiest congratulations and thanks for the tremendous personal and group efforts on your part in delivering the LSI-11 to our first customer. This effort has been marked by fine engineering and extraordinary coordination within DEC and between us and Western Digital.

The LSI-11 is not only already a fine product to be used as a base for others, but it will be the basis of many other products for us.

All of the people who have worked on the project should truly be proud of a fine job. There's clearly more to do, but the progress so far has been great.

GB:mjk

digital INTEROFFICE MEMORANDUM

TO: Distribution

DATE: May 6, 1975

FROM: Gordon Bell

DEPT: OOD

EXT: 2236 LOC: ML12/A51

SUBJ: STRATEGY VIS A VIS SERIAL (MULTIDROP) + PROJECT SUDBURY

I believe that multidrop is going to happen through your perseverence. It looks good.

Will you please come and brief us on the Sudbury project, together with the direction you see our computer structures. I would like to get the bus into our computer planning for terminals and other systems.

The presentation should be when Julius can be present, and the purpose should be to inform us of the direction, together with a proposition as to how you believe other products should use it and when.

I concur with Andy, the interface to your module should be based on the LSI-11 (Q-bus).

GB:mjk

Distribution

Bill Avery
Vince Bastiani
Bob Savell
Tony Lauck

cc: OOD
Andy Knowles

D I G I T A L INTEROFFICE MEMORANDUM

1378

SUBJ: HAROLD STONE

DATE: 05-07-75
FROM: GORDON BELL
EX: 2236
MS: ML12-1/A51

TO: FILE

SUBJ: HAROLD STONE'S VISIT--May ~~15~~ 27, 1975

To: Jim Bell, Stu Wecker, Nat Telchholtz

oc: Andy Knowles

Prof. Harold Stone, U. of Mass is coming to talk with Andy and I on the 15th regarding the direction his committee of COSERS, an NSF task force to define Computer Hardware accomplishments and research. The goal of COSERS is to produce a document, like that for Physics In Perspective, outlines both Computer Science and Engineering. Harold's subcommittee deals with hardware.

I asked Harold to give a talk to us. He will, and I'll send the abstract when it arrives--it is on distributed computing (nets). He's bringing Prof. Walter Kohler and they'd like to meet with Stu and Nat. Please reserve the research conference room and some time to talk with them.

GBimjk

The Commonwealth of Massachusetts
University of Massachusetts
Amherst 01002

SCHOOL OF ENGINEERING
DEPARTMENT OF ELECTRICAL ENGINEERING

May 5, 1975

413-545-1971
545-2441

Dr. C. G. Bell
Vice President - Engineering
Digital Equipment Corporation
Maynard, Massachusetts 01754

Dear Gordon:

I am enclosing a copy of the abstract and title for the talk I will be giving on May 15, as I promised in our phone call last Friday. I am also enclosing for your information a copy of a proposal on the subject that was transmitted to NSF recently. I am completing a technical paper of the subject that may be ready in draft form by the time of the visit. I will be sure that you obtain a copy it then if it is ready, or eventually whenever it reaches a releasable stage.

Walt Kohler and I will plan to arrive in Maynard around noon, and plan to reach your office in time for the 12:20 meeting time. We are looking forward to the visit. Please let me know about any changes in time or place if you wish to make them in advance of the trip.

Sincerely,

Harold

Harold S. Stone
Professor, Electrical and
Computer Engineering

PLEASE POST!

To: Eng. Managers

1380

DATE: May 27, 1975
Place: Mill 3-4 Conference Room
Time: 3:30 PM

Multiprocessor Scheduling with the Max-flow Min-cut algorithm

by

Harold S. Stone

Abstract

In some multiprocessor computer systems under investigation, a modular program is executed with its modules distributed among several different computers. Some program modules are fixed in specific computers because they require resources unique to the computer in which they reside. Other modules are free to "float" from computer to computer during program execution. The goal of a scheduling algorithm is to assign the floating modules to specific processors during the course of computation so as to minimize computation time or some other cost measure associated with the assignment. We show how two-processor scheduling can be implemented efficiently with the aid of the Ford-Fulkerson max-flow-min-cut algorithm as modified by Edmonds and Karp.

D I G I T A L INTEROFFICE MEMORANDUM

SUBJ: THE % FOR ENGINEERING

DATE: 05-07-75
FROM: GORDON BELL
EX: 2236
MS: ML12-1/A51

TO: FILE

TO: OOD

We have a major problem in our engineering budgeting. Ken accuses us of managing by a constant % of NOR. He also states that this % should decline as we grow. He might be correct, although I doubt it;..we do use the 10% for all DEC engineering and 4.5% for our part as upper bounds.

In the case of semiconductors, we made a non-decision to get into it via the Worcester facility. Although I hope it will be the next-to-the-smartest thing we ever did (cores were probably first), I was convinced that it didn't matter when we talked about it at the particular Marketing Committee meeting.

I'm entirely baffled as to how we make these decisions on a rational basis. Unless we come up with an alternative, it will continue from the seat-of-the-pants.

I believe we can make everything, including transformers, and even the iron for transformers, but it clearly has to be based on % of NOR, % ROI, % PC, or our gut. Now it is personality driven, if anything. We must get better criteria, otherwise we could be getting the company in a lot of trouble vis a vis our investment for its products.

I'm mildly scared, because I don't understand. Let's get a method of analyzing this now.

Any ideas?

GB/mjk

D I G I T A L INTEROFFICE MEMORANDUM

1382

SUBJ: MEETING WITH JAKE

DATE: 05-07-75
FROM: GORDON BELL
EX: 2236
MS: ML12-1/A51

TO: FILE

SUBJ: MEETING ON MAY 2 WITH JAKE

TO: Larry Portner
CC: Irwin Jacobs

Jake and I met regarding his view about our software direction system. (The meeting had not been scheduled without you.) We should meet again soon, but I believe he has some valid concerns which we must consider.

1. The notion about design and product management which is distributed among operating systems groups (RSTS), language group, files (data management), and communications. Angel understands, but has a hard time communicating and controlling the various groups. (We're constructed this way to get standards, and skills), but the notion of a system complete with language may suffer with much better interface specs it can work (e.g. as in the 10).

2. He's going to be in trouble vis a vis RSTS. Last year, all that happened was some design and no extensions. It is old and will suffer, needing:

   A. New compiler to increase speed.

   B. More capabilities in data base.

   C. Operating system enhancements.

   D. COMM support for multidrop terminals (elsewhere too).

      BISYNC to IBM, and DECNET.

   We aren't spending any appreciable on extensions, and nothing happened last year.

3. The transition from 16 to 32 bits could take all software from 11 and make a real gap in time with no software.

4. Can we make DIBOL a standard instead of min-COBOL? I'll talk with Mike O'Connel about pursuing this with Grace Hopper.

5. TPM can be built from RSX and RSTS base. He prefers the RSTS base due to the progression of products. The TPM

SUBJ: MEETING WITH JAKE

DATE: 05-07-75
FROM: GORDON BELL

strategy is necessary--like crazy. For BUSINESS, it is more of an evolution over existing products to:

A. Better data base.

B. Interprocess communication so that a process can handle queues of terminals, messages, etc. in a pipelined fashion.

C. A single language.

Fundamentally, TPM is like timesharing, except that it is a single language, little or no programming (i.e. it is production), and has better interprocess communication.

6. COBOL will eventually be his language at high end.

Jake is not unhappy with possibility of UNICORN--in about $150K range. It has most of features for TPM (including DB, multi-terminals, interprocess communication).

There's a RSTS V7 meeting that we should buy into on May 7 and 8.

GB:mjk

D I G I T A L INTEROFFICE MEMORANDUM

SUBJ: STU WECKER

DATE: 05-07-75
FROM: GORDON BELL
EX: 2236
MS: ML12-1/A51

* *

TO: FILE

* *

SUBJ: STU'S MOVE BACK TO RESEARCH

To: Distribution

Although I believe Stu wants to get back to research, I'm terrified at not having a network architect. Please hold up this transfer until a replacement is found or the network products have been delivered through routing (approximately 1 year).

Stu has done a fine job in what's one of the most difficult jobs in the company; let's not blow it now by moving him and allowing the DEC mediocrity/anarchy to take over.

He must continue as an unreasonable architect, with some aspirations as to what networks are and can be.

GB:mjk

Distribution

Jim Bell
Larry Portner
George Plowman
Nat Telchholtz
Larry Wade
Stu Wecker

digital INTEROFFICE MEMORANDUM

TO: Distribution

DATE: May 7, 1975

FROM: Gordon Bell

DEPT: OOD

EXT: 2236 LOC: ML12/A51

SUBJ: PL/S--at IBM

Random rumor:

PL/S has been microcoded on a 360 and runs about 10 times faster for various Op. Sys. functions. Not surprising since PL/S is used for various Op.Sys. programming.

Supposedly, PL/S is used for all system programming.

PL/S machines run much more slowly for APL than hand-coded 360 code--somehow not explainable. PL/S has been effective (see report on it in IFIPS HLL seminar last year.

GB:mjk

Distribution

VAXC
Jim Bell
Ed Fauvre
George Plowman
George Poonen

digital INTEROFFICE MEMORANDUM

TO: Distribution

DATE: May 7, 1975

FROM: Gordon Bell

DEPT: OOD

EXT: 2236 LOC: ML12/A51

SUBJ: RANDOM RUMOR FROM A WEST COAST DESIGN GROUP

Some semiconductor company is busily building a PDP-11 for sale.

GB:mjk

Distribution

Dick Clayton
Bill Demmer
Lorrin Gale
Andy Knowles
Henry Lemaire
Steve Teicher
Mike Tomasic

digital

May 6, 1975

Al Phillips
President
Western Digital Corporation
19242 Red Hill Avenue
Box 2180
Newport Beach, California 92663

Dear Al:

Please accept my heartiest congratulations and thanks for the tremendous personal and group efforts on your part in delivering the LSI-11 to our first customer. This effort has been marked by fine engineering and extraordinary coordination within DEC and between us and Western Digital.

The LSI-11 is not only already a fine product to be used as a base for others, but it will be the basis of many other products for us.

All of the people who have worked on the project should truly be proud of a fine job. There's clearly more to do, but the progress so far has been great.

GB:mjk

Sincerely,

Gordon Bell
Vice President
Office of Development

DIGITAL EQUIPMENT CORPORATION, 146 MAIN STREET, MAYNARD, MASSACHUSETTS 01754
(617)897-5111 TWX: 710-347-0212 TELEX: 94-8457

digital

May 6, 1975

Donn C. Arrell
3200 So. Zuni Street
Englewood, CO 80110

Dear Mr. Arrell:

Your proposal came to me. I do not believe we have any interest in pursuing the use of your machine as a standard product, although it does sound interesting.

Sincerely,

Gordon Bell
Vice President
Office of Development

GB:mjk

cc: Steve Kallis w/ orig. letter.

DIGITAL EQUIPMENT CORPORATION, 146 MAIN STREET, MAYNARD, MASSACHUSETTS 01754
(617)897-5111 TWX: 710-347-0212 TELEX: 94-8457

D I G I T A L INTEROFFICE MEMORANDUM 1389

SUBJ: HP ANALYSIS

DATE: 05-08-75
FROM: GORDON BELL
EX: 2236
MS: ML12-1/A51

TO: FILE

SUBJ: GRANT'S HP DISC /15 ANALYSIS

To: Grant Saviers
CC: Bob Puffer

I agree (and hope), HP may have boxed themselves in.

They did do a good job for the material they started with.

Depending on the size of the logic design, do they have a better system than we have?

Clearly they thought about multiple drives and multiple CPU's, however, it looks like their approach could be expensive, unreliable (single control) and a bottleneck. Is it?

Our ability for multiple simultaneous transfers, redundant paths, and distributed control is good, especially if it's not too much more expensive. I believe such an approach can be, and can you explore what we need organizationally or whatever (e.g. should disks do all the handlers and diagnostics?). How can we get more aggressive in the product ideas relative to what the user sees vis a vis features (versus implied reliability, manufactureability, etc.) for disks?

GB/mjk

GB/mjk

D I G I T A L INTEROFFICE MEMORANDUM

SUBJ: LDP

DATE: 05-13-75
FROM: GORDON BELL
EX: 2236
MS: ML12-1/A51

TO: FILE

SUBJ: INTERACTION WITH LDP ON 8 MAY 1975

To: OOD

cc: Ed Kramer, John Fisher

Ed Kramer, Gus Ashton, George Thissell and Al Wallack met with Larry, Bill Demmer, Larry Wade, George Plowman, and I.

Ed gave a capsule of FY76.

DEV. $M		SALES	
Graphics	.65	RT-11	660+50%
A/D	.2	MUMPS	60
MUMP	.18	Gammall	50
Small System			
Videographics	.8	RSX11M	200
		RSX11D	30
Fast Floating pt.	.15	OS/8	300
	2.4		3 - 3.5
Support Costs			
About	.5	Units	
		11/10	650
		40	360
		45	175
		8	250
		Terminals	3000

SUBJ: LDP

DATE: 05-13-75
FROM: GORDON BELL

The big concerns regarding interaction with Engineering now that PC has gone:

1. How are all the PSG's reviewed individually and in toto? (Our line people...who we review individually.)

2. How does a PSG report on plans to PLMC and MC?

3. How can the PL products be reviewed as they were by PC?

I said we have to propose the process in lieu of PC, etc. and in light of MC responsibility.

Ed had questions on the Engineering allocation (Phil).

Ed proposes some form of products clearinghouse simply to keep all informed of potential products (e.g. the Quame printer for word processing).

LDP wants their proposal entered as an alternative in the CLASSIC 11 packaging.

GB/mjk

digital

May 13, 1975

Hector E. French
9 Davidson Road
Wakefield, Mass. 01880

Dear Mr. French:

Mr. Olsen handed me information on your adder. Please send the complete file including the algebra, so that I can evaluate whether we might proceed further.

Please be a little more specific in terms of quantities for speed, time, and other applications beside addition.

Sincerely,

Gordon Bell

Gordon Bell mjk
Vice President
Office of Development

GB:mjk

cc: Ken Olsen

DIGITAL EQUIPMENT CORPORATION, 146 MAIN STREET, MAYNARD, MASSACHUSETTS 01754
(617)897-5111 TWX: 710-347-0212 TELEX: 94-8457

Marilyn -
Please make copy of orig ltr and keep and send along also.

→ G. Bell (1)

APR 29 1975

1393

HECTOR E. FRENCH
9 Davidson Road
WAKEFIELD, MASS. 01880

April 22, 1975

MAY 01 1975
K-170

Mr. Kenneth H. Olsen, Pres.

Digital Equipment Corp.

Maynard, Mass., 01754

Dear Mr. Olsen:

Thank you for your reply of April 10 concerning my digital adder. I can understand your manufacturing requirements, and I thank you for your consideration.

You may recall that sometime last fall our mutual friend Nate Hubley forwarded to you a description of an alternate algebra I had worked out. I'd like to enclose, on a non-confidential basis, some further information for your review.

The value of this algebra to your company would lie in the economics of designing and manufacturing a mini-computer having complex magnitude capabilities, and possibly also within conventional equipment.

I would be glad to discuss this in greater detail at your convenience.

Yours truly,

Hector E. French

Hector E. French

Peggy Can I have the info?

Thanks

This is whole shebang - (last of paper)

Ken gave you this back in Dec. 74 - Didn't have a copy -

April 10, 1975

COPY

Mr. Hector French
9 Davidson Road
Wakefield, Massachusetts 01880

Dear Mr. French:

I thank you for your note on the digital adder.

A number of years ago we spent a great deal of time designing, inventing and improving adders. When parts were expensive this was worthwhile and people wrote books and spent a lot of time developing the theory of adders.

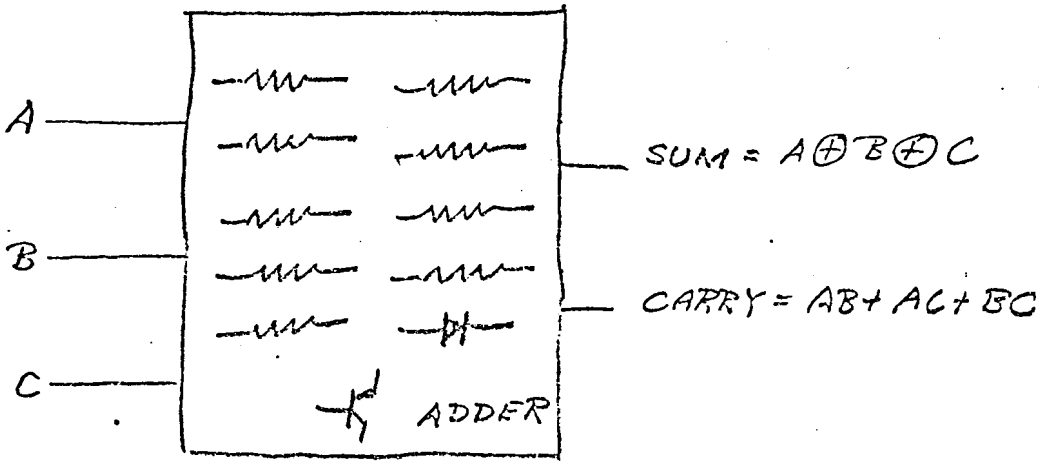
However, lately we buy most of our adders as large scale integrated circuits, and parts are so inexpensive that if there is some improvement in the economy it will not make much difference. As a result, we do not build adders anymore and have little interest in them except from an academic point of view.

Thank you again for your letter.

Sincerely yours,

KHO:mg

MINIMUM-ELEMENT ADDER



9 RESISTORS

1 DIODE

1 TRANSISTOR

Above information is supplied on a non-confidential basis.

Hector E. French

Hector E French

HECTOR E. FRENCH
9 Davidson Road
WAKEFIELD, MASS. 01880

April 7, 1975

Mr. Kenneth Olsen

Weston Road

Lincoln, Mass., 01773

Dear Mr. Olsen:

Our mutual friend Nate Hubley has suggested that you might be interested in the material enclosed. He has earlier given you a similar body of information on a completely different item, you may recall.

I'm enclosing, on a non-confidential basis, with no obligation expressed or implied, some information on a digital adder I've worked out. This adder requires only a minimum number of elements. All elements are non-critical, and the circuit is well-suited to solid-state manufacture.

If you are interested, with a view toward employment, I would be glad to demonstrate my working model on a non-confidential basis at your convenience.

Yours truly,

Hector E. French

Hector E. French

999

WUI NY TELUS 123 1547 05/12+
DIGITAL MAYN A

PPYQ 1540 12-MAY 13958 1517 12-MAY
MP30 FORN

DIGITAL EQUIPMENT CORPORATION
146 MAIN STREET
MAYNARD, MASS

LT

COLONEL RAO
BHARAT ELECTRONICS LTD.
JALAHALLI P.O.
BANGALOR, INDIA

I RECEIVED YOUR MAY 2 LETTER. PRAVIN GHANDI, INDIA, AND HECTOR BUENO, DEC MAYNARD, WILL WORK OUT SCHEDULE WITH YOU. PLEASE CONTACT HECTOR UPON YOUR ARRIVAL OR TWX INFORMATION AHEAD.

FROM: GORDON BELL - DIGITAL MAYNARD

END
NNNN

+
WUI TELUS NYK

DIGITAL MAYN A

digital INTEROFFICE MEMORANDUM

TO: OOD

DATE: February 17, 1975

FROM: Gordon Bell

DEPT: OOD

EXT: 2236 LOC: ML12/A51

SUBJ: OOD STAFF AGENDA--FEBRUARY 20, 1975

12:30 Lunch	Production Communications	Cudmore
2:00	Packaging Rules (material enclosed)	
3:00	Need for a "Systems" Engineering Handbook (Bob Gray memo attached.)	
3:15	Getting money for component engineering (material enclosed)	Best/Amann
3:30	Strategy/Budget Sequence Preliminary discussion on handle the Woods Meeting	
4:30	Perception of Product Manager function-- outline for workshop presentation	Cronkite

GB:mjk

- -

FUTURE AGENDA ITEMS

Date	Topic	Responsible
3/13	Field Service communications	Shields
3/13	DEC Safety Standard	Cudmore/Minezzi
3/13	Analysis of Product Manager's Workshop	Abbett/Cronkite
?	Hardware/Software Systems Plan	Portner/Clayton
?	2x2 report	Puffer
Q4	Production Communications	Cudmore/Smith

C2D + cc Ken STAFF Mfg. talk with me on this - I'm agreeing that we should get a prot. What you think? Gordon.

Jack, Denmer

PACKAGING RULES

1. Largest basic PC building block in a hex by 15" module.
2. Double sided PC boards.
3. Automatic insertion of components.
4. Standard digital interconnection schemes.
5. Present 18 mil cores - 3 wire stack.
6. Standard available integrated circuits.
7. Standard backpanel connector.

C1338

this one?
11/70
11/85
10
Somehow on PDC?

Internal Proposal R Wood 3/1/75

MECHANICAL FORM FACTOR

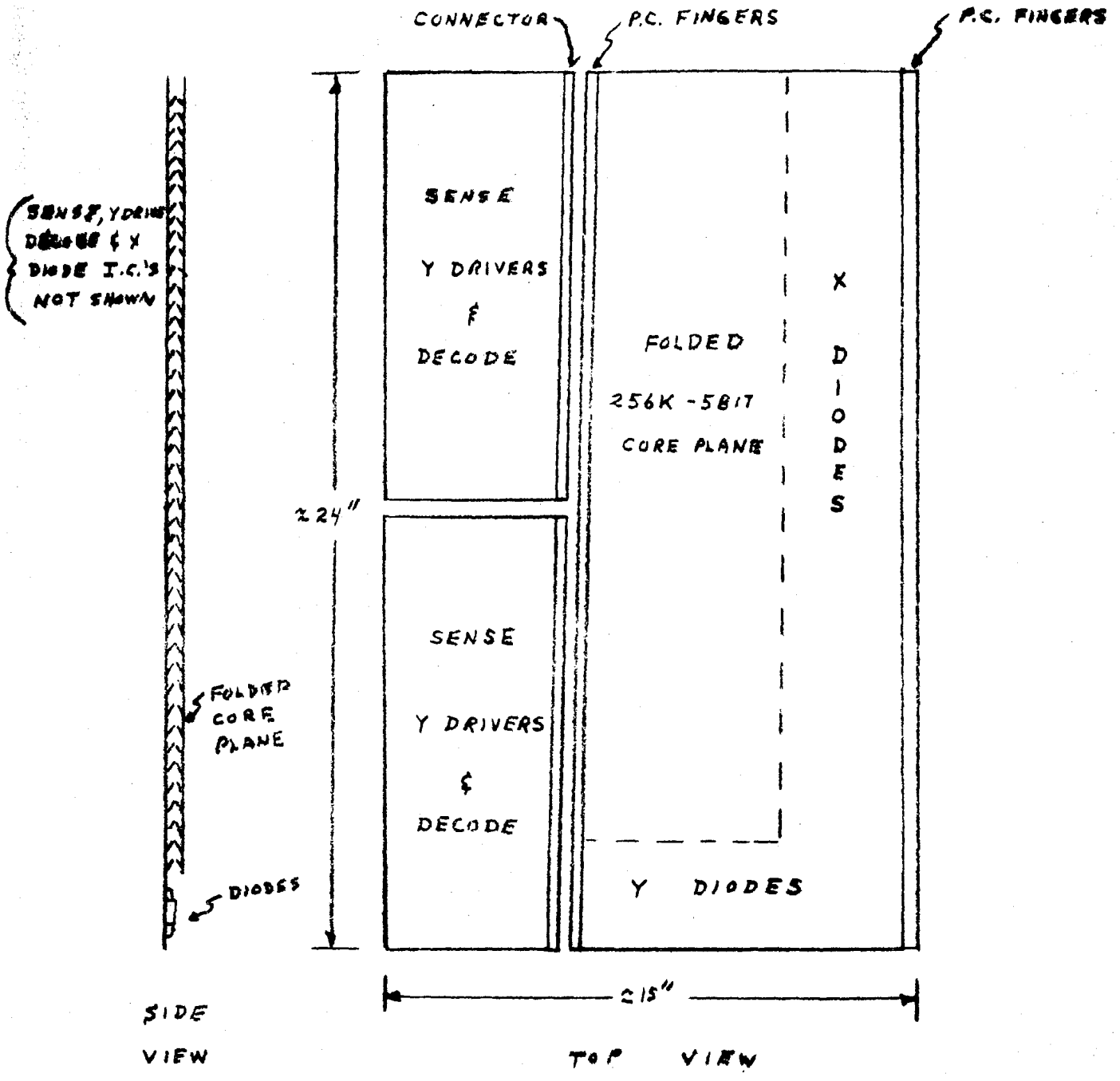
	FORM FACTOR 1 15" x 24" (4,980,736 Bits)			FORM FACTOR 2 15" x 15" (2,490,368 Bits)		
Memory Size	256K-19	128K-38	64K-76	128K-19	64K-38	32K-76
Cost - $	3150.	3375.	3650.	1975.	2175.	2400.
- ¢/Bit	.063	.068	.073	.078	.087	.096
% Increase	-	6.8	15.9	24.2	38.1	52.1
*Power Standby	120	140	175	80	100	135
(Watts) Operational	280	400	630	240	360	590
Performance Cycle	600	600	600	600	600	600
(Nanoseconds) Access	1600	1600	1600	1600	1600	1600
**MTBF System	11,000	10,800	10,600	15,200	15,000	14,800
(Hrs.) X Drive	30,000	30,000	30,000	56,300	56,300	56,300

*Voltages +20, +5, -5 : +20 Volts will be temperature compensated.

**Calculated taking average Mil Std 217A & EMI's Experience.

STACK BOARD - 256 K - 5 BITS

C1399

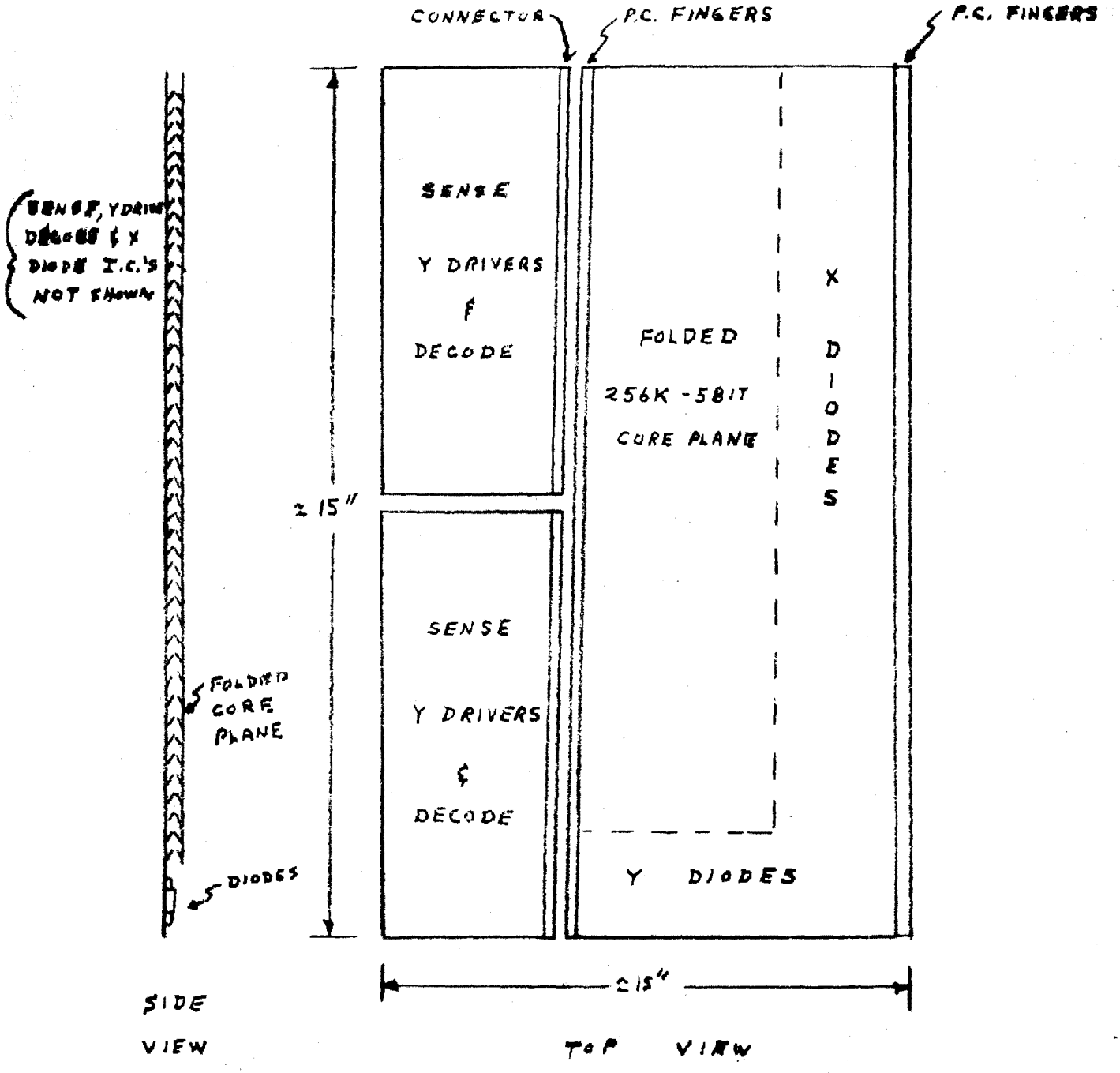


TENTATIVE CONCEPTUAL DESIGN
USEING FORM FACTOR 1

R.D.N - 1/29/75

STACK BOARD - 128 K - 5 BITS

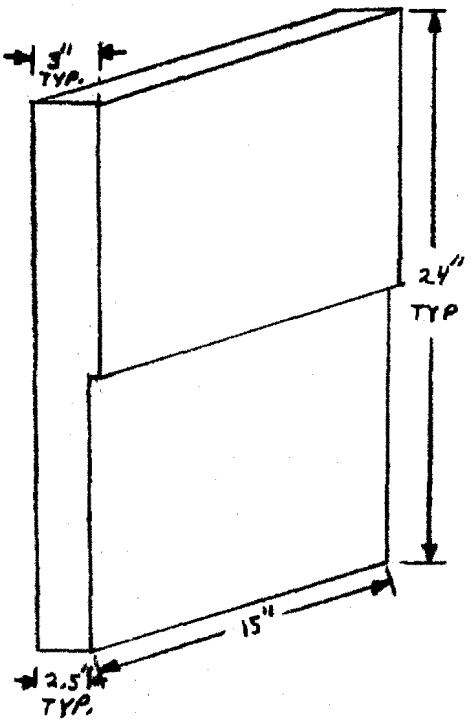
C1400



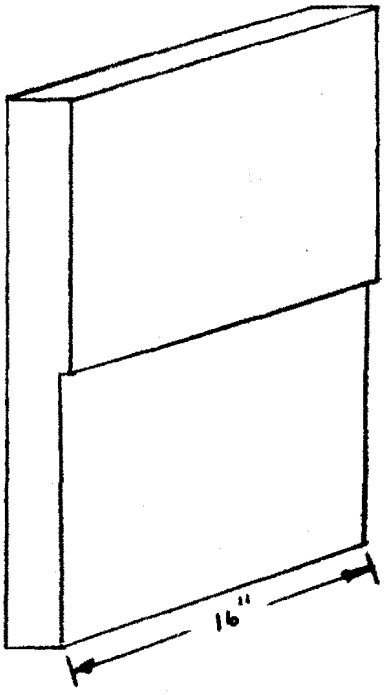
TENTATIVE CONCEPTUAL DESIGN
USEING FORM FACTOR 2

R.D.N - 1/29/75

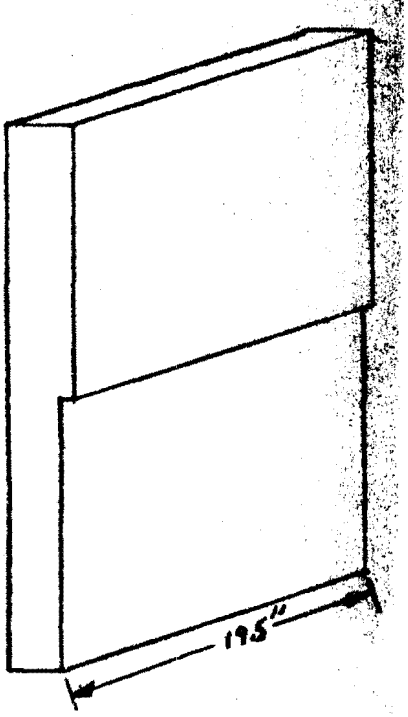
PACKAGE VOLUME



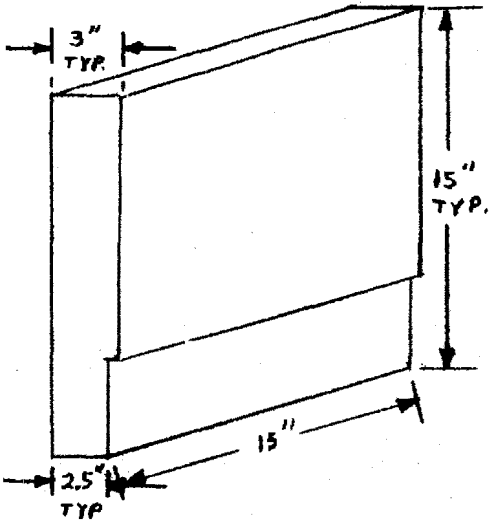
256K - 19 BITS



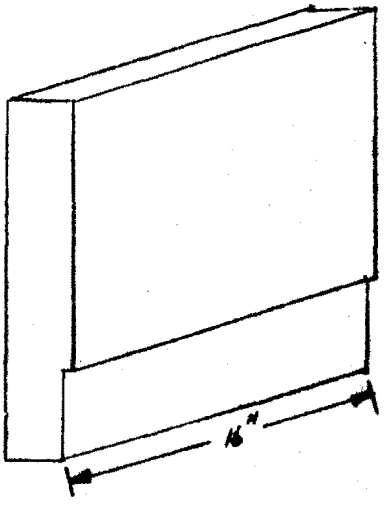
128K - 38 BITS



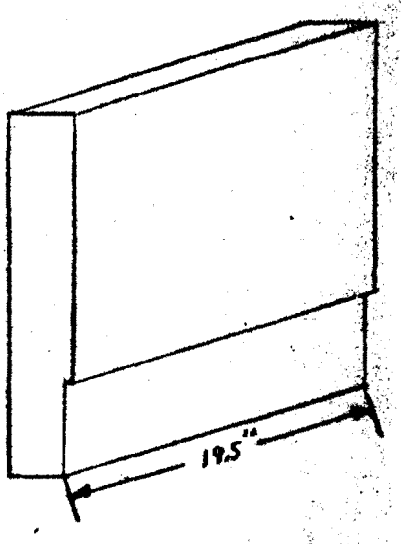
64K - 76 BITS



128 K - 19 BITS



64K - 38 BITS



32K - 76 BITS

R.S.H - 11/28/75

COMPANY CONFIDENTIAL

Gordon Bell

DIGITAL EQUIPMENT CORP.

digital INTEROFFICE MEMORANDUM

For staff mtg. discussion and resolution! cc.

TO: Gordon Bell

DATE: January 31, 1975 1402

CC: See Dist. List Below GB

FROM: Bob Gray

DEPT: 11 Engineering

Good parts: Larry + Dick

EXT: 3444 LOC: ML/E54

SUBJ: NEED FOR A "SYSTEMS" ENGINEERING HANDBOOK

The present "Project Leader's Notebook" and "Engineering Handbook" are magnificent pieces of work and offer real help and needed guidance.

One aspect of the present "Project Leader's Notebook," however, bothers me a great deal. It opens with the premise:

> "... we have been increasing our emphasis on the total system concept."

Yet, in no place could I find any mechanism or mention of coordinating software with hardware. Hardware is mentioned only as something to "get time on to debug!"

These "walls" must come down if we are to succeed! The next issue of the "Project Leader's Notebook" should have a section on hardware that parallels that of section 3.1 in the "Engineering Handbook."

An even better solution might be to merge these two documents into a single volume that deals with the system aspects as well as the purely software and purely hardware aspects of projects!

Dist. List:

Ken Olsen
Dick Clayton
Larry Portner
Bob Puffer
Stan Olsen
John Fisher
Bill Thompson
Bill Demmer
Jega Arulpragasam
11 Strategy Committee
Dick Best

digital INTEROFFICE MEMORANDUM

TO: DISTRIBUTION

DATE: JANUARY 15, 1975 1403

FROM: DICK AMANN RA

DEPT: COMPONENT ENGR.

EXT: 2008 LOC: 6B-3

SUBJ: HOW COMPONENT ENGINEERING (CC320) WILL HELP YOU CONTROL YOUR COST CENTER AND PROJECT BUDGETS

Some time ago, I sent a note to you asking whether or not you would budget Component Engineering for Q3 and Q4. Since you have replied negatively, or not replied at all, Component Engineering will take the following steps over the next six months to help keep your cost center budget accurate.

1. We will not accept any requests for work from personnel in your Cost Center.

2. We will make sure that nobody in your Cost Center introduces a new part into Digital IF IT REQUIRES SUBSTANTIAL WORK ON OUR PART.

There will be a minimum of exceptions to these above two rules. In fact, about the only exception I can think of is the following:

1. If somebody in your Cost Center requests a minimal (1 or 2 hours) amount of service on our part, or wishes to bring in a component that requires less than 2 hours of work on our part, then we will try, insofar as our resources allow it, to honor the request.

However, any activity requested of our department by personnel in your department that requires more than 1 or 2 hours of work will be refused.

Component Engineering will do its best to try to help you keep your Cost center Budget balanced.

I hope you'll understand our inability to honor requests on the part of personnel in your Cost Center for work during the next six months.

PRODUCT LINES AND PERSONNEL NOT FUNDING COMPONENT ENGINEERING

PRIMARY CONTACT	PERSONNEL	PRODUCT LINES
Grant Saviers	John Reed Walter Dunham Demétrios Lignos Chao Chi Nott Venugopal Norm Fields Win Seargent	Disk
Bob Peyton		Tape
Ed Correl	Ed Steltzer Chuck Bickhoff Peter Heller	LA 36
Tom Stockebrand	Russ Doane Dick Pucci Mike Morgenstern John Bucyzinski Mike Lies	
~~John Leng~~	~~Jim Provident~~ ~~Ron Melanson~~ ~~Sultan Zia~~ ~~Bill Walter~~ ~~Dave Thomas~~	← "10 land" will be budgetting cc 320
Brad Vachon	Bob Savelle Lenny Dionne Al Ricketts Akavia Kaniel Art Savelle Gerry Gagnon ~~Jim Melvin~~	← Jim will be budgetting cc 320

1404

PRODUCT LINES AND PERSONNEL NOT FUNDING COMPONENT ENGINEERING

PRIMARY CONTACT	PERSONNEL	PRODUCT LINES
Gordon Bell	Carl Noelcke Dick Best	98 - Applied Engineering
Jack Shields	Tom Kennedy Fred Dahl	94 - Field Service
Paul Rey	J. Drew B. Hazen F. Loya Dave Veinot	14PL98 Power Supply
Lorin Gale	Charles Valliant Ed Anton Mike Carriefello	
John Clarke	Dave Brown John Kirk Bob Reagan Paul Gardner Al DeLuca	95PL18 Central 8
~~Vince Bastiani~~		~~70PL20 Communications~~ ← Vince will be budgetting ca 320
Brian Croxon	Brian Taylor	16PL98 Memory Systems
Richard Morris	Don Smelser Cliff Granger Bill Choates Dick Manion Bob Price	18PL98 Core Memory
Bill Demmer	Al Ryder John Misialek Bob Kirk Sas Durvasula Dave Potter Steve Rothman Jega Arulpragasm Bob Gray John Levy	Dick Gonzales Ralph Platz Don Vonada

digital INTEROFFICE MEMORANDUM

TO: OOD

DATE: March 13, 1975

FROM: Gordon Bell

DEPT: OOD

EXT: 2236 LOC: ML12/A51

SUBJ: OOD STAFF AGENDA REVISION--Thursday, March 13

12:00 Lunch	New Members on M&E Stock Option Package	Puffer Abbett
12:15	Product Accounting Status	Laut
1:00	Design of Products and how it effects us in the marketplace	Carl Kooyoomjian Ray Michle
1:30	A. CBEMA representative B. SDC outside hires C. Component Eng. Money	OOD Kostetsky Best/Amann

GB:mjk

Postponed:

Misc. topics (Abbett)
Analysis of PM workshop (Abbett, Cronkite)

25BGr373-075

digital INTEROFFICE MEMORANDUM

FEB 14 1975

TO: Bob Puffer

DATE: 13 February 1975

CC: Andy Knowles Ralph Platz
Gordon Bell
Bill Demmer
Dick Clayton
Jega Arulpragasam

FROM: Bob Gray

DEPT: 11 Engineering

EXT: 3444 LOC: ML5/E54

SUBJ: RESULTS OF FIRST CBEMA MINI COMPUTER INTERFACING STANDARDS MEETING

The ANSI(CBEMA) Mini-Computer-Task-Force (X3T91) decided at the initial 10-11 February 1975 meeting to attempt to CREATE STANDARDS FOR MINI-COMPUTER PERIPHERAL INTERFACES. (The interface between a device and its controller). It was deemed unfeasible to standardize CPU bus interfaces.

It seemed to me that it would be in DEC's interest to influence these standards by having a permanent member of the task force. I do not feel I can or should be that representative. First, the task will occupy 10-25% of the representative's time. Secondly, my responsibility is mainly in CPU's, not peripherals.

I suggest we have a permanent representative from your organization with an alternate from Ralph Platz's group. (Andy Knowles' organization might be a reasonable place to look for a rep. also!)

The next meeting is April 3-4. Our rep has a considerable amount of work to do, to prepare for this! I have notes on the first meeting and can explain the expectations.

Could you please name someone from your group for this task?

Attached is the summary of the Feb. 11-12 meeting as will be forwarded to the main X3T9 committee by the Task Group's acting chairman.

/ecm
Attach.

(Copy of Summary, written by Bill McClain, X3T91 Acting Chairman.)

Appendix A 1408

X3T91-13-75

To: X3T9 Committee

The Task Group on Minicomputer Interface Standards has established for its efforts two main objectives:

1. Interchangeability of peripherals and minicomputers
2. Interconnection of minicomputers to large computers.

The Task Group has directed its attention initially to Item 1. Item 2 will be explored later.

The Task Group has decided that it is both reasonable and feasible to apply an interface standard between the controller and device electronics of the peripherals. As a start, the Group has defined two general families of interfaces (designated as Type I and Type II) and differentiated by their functional, electrical, and mechanical characteristics. The two groups are:

Type I	Type II
a. Line Printers	a. Disks
b. Card Reader/Punch	b. Cassette Tapes
c. Paper Tape Reader/Punch	c. Modems
d. Magnetic Tape	d. Terminals (alphameric)
e. Digitizers	e. Others
f. Plotters	
g. Serial Printers	
h. Terminals (graphics)	
i. Computers	
j. Memories (bulk)	
k. Others	

It is expected that the Type I group may be divided into two or more groups. It is considered feasible to provide interchangeability and compatibility within a type, but interchangeability across types cannot be assured. The Task Group's goal is to provide electrical and mechanical specifications that will cover each type and functional specifications unique to members of each type. Consideration will also be given to the operational specifications.

As a beginning several factors will be considered by the Task Group:

1. De Facto and proposed standards
2. Applicability of RS232C and SP1162,1163
3. Trends generated as the result of applications of microprocessors and intelligent devices.
4. Costs and economics.

The basic needs in this area of standardization is for total compatibility - both hardware and software, however, if hardware

is compatible this would be a step forward. This would permit:

1. Second sources (or more)
2. Reduce the time limitation of purchase, permitting more consideration of service and design.
3. Possible off-the-shelf items or components.

Standardization will not impact differences in products nor will it inhibit the functional capabilities of the system if the device and application are independent.

The Program of Work established follows:

I. Type I and II Interfaces

a. Detailed scope and objectives
   1. Parameters of Interfaces (4-75)
   2. Device characteristics - classification (similarities and differences) (6-75)
   3. Review present standards (defined and de facto) (4-75, 6-75)

b. Definitions of Standards families (8-75)

II. Type I Interface

a. Specifications - start (10-75), complete (2-76)
b. Review for similarities and merge if possible (4-76)
c. Final proposals for standard(s) (6-76)

III. Type II Interface

a. Specifications
b. Review for similarities and merge if possible
c. Final proposal(s) for standard(s)

digital INTEROFFICE MEMORANDUM

TO: OOD

DATE: March 17, 1975

cc: Vince Bastiani
Henry Lemaire
Julius Marcus
Mark Abbett
John Cronkite

FROM: Gordon Bell

DEPT: OOD

EXT: 2236 LOC: ML12/A51

SUBJ: OOD STAFF MEETING AGENDA--March 20, 1975

NOTE: LARRY PORTNER'S CONFERENCE ROOM; NO LUNCH

1:00	Strategy Position	Bastiani/Marcus
2:00	Strategy Position	Lemaire/Croxon
3:00	SDC outside hires	Kostetsky
3:10	Other strategy positions:	
	LA, Disks, Tape	Puffer
	VT's	Laut
	Systems	Clayton
	Software	Portner
4:00	Analysis of PM workshop	Cronkite/Abbett

Future Agenda Items

Date	Topic	Responsible
3/27	Field Service Communications	Shields
3/27	Responsibility for design, fabrication, and testing at the systems level	Clayton/Smith/Cudmore
3/27	Woods rehearsal	OOD
?	Hardware/Software Systems Plan	Portner/Clayton
?	2x2 report	Puffer
Q4	Production Communications	Cudmore/Smith
4/3	DEC Safety Standard	Cudmore/Minezzi

Note: STAFF MEETINGS WILL CONTINUE TO BE HELD ON THURSDAY FROM 12:30 to 5:00 unless otherwise noted.

digital

April 16, 1975

John Grason
Computer Science Department
Carnegie-Mellon University
Pittsburgh, Pennsylvania 15213

Dear John:

The sales on Designing Computers and Digital Systems last year were:

Books sold	601 x $.23 =	$138.23
Free books	3378 x $.02 =	67.52
Total		$205.79

Please find enclosed a check for $205.79.

Sincerely,

C. Gordon Bell
Vice President, Office of Development
Professor, Computer Science
Carnegie-Mellon University (on leave)

CGB:mjk

Enclosure

DIGITAL EQUIPMENT CORPORATION, 146 MAIN STREET, MAYNARD, MASSACHUSETTS 01754
(617)897-5111 TWX: 710-347-0212 TELEX: 94-8457

digital

April 16, 1975

Dr. Allen Newell
Computer Science Department
Carnegie-Mellon University
Pittsburgh, Pennsylvania 15213

Dear Allen:

The sales on Designing Computers and Digital Systems last year were:

Books sold	601 x $.23 =	$138.23
Free books	3378 x $.02 =	67.52
Total		$205.79

Please find enclosed a check for $205.79.

Sincerely,

C. Gordon Bell
Vice President, Office of Development
Professor, Computer Science
Carnegie-Mellon University (on leave)

CGB:mjk

Enclosure

DIGITAL EQUIPMENT CORPORATION, 146 MAIN STREET, MAYNARD, MASSACHUSETTS 01754
(617)897-5111 TWX: 710-347-0212 TELEX: 94-8457

To: Lloyd Tucker

DIGITAL EQUIPMENT CORPORATION

1113

VOUCHER

Payable To:

Name: See below

Address: _____

_____

Amount: $469.40 Date 4/14/75

Description: Royalties on Digital Press book "Designing Computers and Digital Systems" in calendar year 1974.

Badge	Cost Center	Account	Act. O E	1	2	3
80	371	7381	E	98	7207	

Order Rec'd.	Price OK	Payment OK	Check No.

Please write checks as follows:

John Grason (CMU) $205.79

Allen Newell (CMU) $205.79

Gordon Bell (DEC) $ 57.82

$469.40

☐ Mail Check

☒ Check To Originator

Gordon Bell ML12/A16

DEC 1-1028

digital

INTEROFFICE MEMORANDUM

TO: Gordon Bell LOC/MAIL STOP ML12/A51

DATE: April 11, 1975
FROM: Phil Laut
DEPT: Engineering
EXT: 4308
LOC/MAIL STOP: ML12/A16

file

SUBJ: Digital Press (Payments of Royalties to Authors for Calendar Year 1974)
"Designing Computers and Digital Systems"

	1974		
Source of Books	Northboro	Maynard	Total
# Free	3368	10	3378
# Sold	495	106	601

Payments Due:

Payee	Calculation	Total Payment
Gordon Bell	Free books 3378 x $.01 =	$ 33.78
	Books Sold 601 x $.04 =	24.04
		$ 57.82
Allen Newell & John Grason	Free Books 3378 x $.02	$ 67.56
	Books Sold 601 x $.23	138.23
		$205.79 each

Total royalties calendar '74 = $469.40

Income from book sales = 601 x $3.95 = $2373.95

Last year, you sent a $100.00 honorarium to Dr. Dan Srewrorek for his contribution to the book. Do you want to do that again?

A little history for you to look at:

Calendar Year	1972	1973	1974	Cumulative
Free Books	1480	1102	3378	5960
Books Sold	718	2942	601	4261
Total Books	2198	4044	3979	10221
Income from Book Sales	$2836.10	$11620.90	$2373.95	$16830.95
Royalties to:				
Gordon Bell	$ 43.52	$ 128.70	$ 57.82	$ 230.04
John Grason	194.74	698.70	205.79	1099.23
Allen Newell	194.74	698.70	205.79	1099.23
Sub-total Royalties	$ 433.00	$1526.10	$ 469.40	$2428.50
Honorarium		$ 100.00	?	
Total Expense	$ 433.00	$1626.10	?	?

To: Demmer + Jeggy + Gray (+ return)

Can any of this go in PDQ?

C1415

D I G I T A L INTEROFFICE MEMORANDUM

PAGE 1
SUBJ: 11 PROGRAMMED I/O
DATE: Ø4-ØØ-75
FROM: GORDON BELL
EX: 2236
MS: ML12-1/A51

TO: FILE

SUBJ: PIo*--vs(KIo+Pc)* BRIEF NOTE ON 11 PROGRAMMED I/O AND CHANGES IN PDP-11 ISP FOR BETTER I/O TRANSMISSION

To: VAXC, Chuck Kaman, Jim O'Loughlin

I have long been against PIo's (i.e. channels in the IBM venacular) because:

Ø. Historically, the IBM 709, 7090 provided them in a really maximally costly way.

1. They add logical, and physical complexity, without much payoff (low duty factor). Their real function is to pass information, without change,

2. As a somewhat intelligent device, they require more coorfination from a higher level intelligent processor, Pc, than either another Pc or a lesser device.

3. Another processor which has to be programmed, diagnosed, and stocked.

4. Programs have to be written for it, dynamically, by Pc.

5. In the limit, 1 memory cycle is required to transfer data, for high speed devices, the NPR is used, and achieves this limit.

6. Even in the case of IBM channels, an interrupt/block transfer to Pc is often required since the Pc executes a program to plan the transfers,

7. I/O computers organized in the fashion of the 6600, and networks are the real answer to I/O by doing significant data reduction and preprocessing,

Most of the things PIo's can do well, a Pc can do substantially better (e.g. optimize disk blocks in order of arrival time). When a Pc is used this way, and runs out of capacity, we simply add a second Pc of the same type,

I do believe we should have more powerful I/O instructions

Robin + Lauchbaum working on a proposal for block/block for VAX that would be suitable for PDQ.

GB

D I G I T A L INTEROFFICE MEMORANDUM

SUBJ: 11 PROGRAMMED I/O

DATE: 04-08-75
FROM: GORDON BELL
EX: 2236
MS: ML12-1/A51

In our Pc, to assist in transferring and manipulating data from the I/O world. This includes:

1. More rapid response to interrupts to transfer blocks (vectors) between the Mp (via Pc) and an I/O controller, Kio.

2. Actually processing information on the fly for certain tasks. For example, in communications tasks, it is appropriate to take in a character, translate it, put it in a queue, and evoking a process (interrupt) in the Pc, if necessary.

The performance gain, attributable to channels, can be obtained by:

1. Giving commands rapidly to a simple device controller, Kio.

2. Double buffering a second command in Kio.

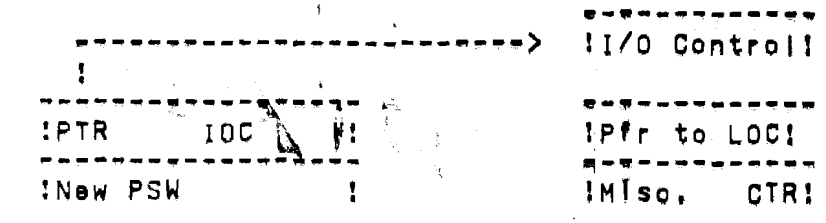
CURRENT INTERRUPT PROCESSING IN Pc

Responding to an interrupt, and transferring a word takes:

Save PC, PSW	4
MOVE IO, LOC	5
ADC LOC	3
DEC CTR	3
BR	1
RTI	3
Total	19 Memory Cycles

ADDING BLOCK TRANSMISSION

By placing a control block for block transfers, in the trap vector locations, we get:



D I G I T A L INTEROFFICE MEMORANDUM

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DATE: 04-08-75
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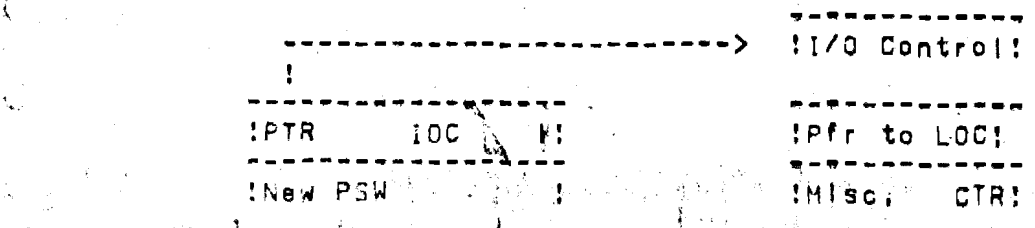


D I G I T A L INTEROFFICE MEMORANDUM

SUBJ: 11 PROGRAMMED I/O

DATE: Ø4-Ø8-75
FROM: GORDON BELL
EX: 2236
MS: ML12-1/A51

This takes 6 memory cycles per word transferred.

USE OF BLOCK TRANSMISSION IN MICROCODED MACHINES USING CURRENT PROGRAMMED Kio's.

The 11A4Ø can implement the instruction directly and achieve the 3X speed up.

For the PDQ, the variables can be moved into its WCS, and in principle, achieve a speed of 2 memory cycles with current programmed controllers (Kio)--another factor of 3. Note, that in this case, since the PC doesn't move, there is no need to fool with the stack, etc.

Summary of changes:

Current controllers via programming	19
Additional block transfer instruction for current controllers	6
Microcode caching of data for block transfer instructions using current controllers	2
Best case--NPR controllers	1

well, µP time becomes sig. here

IMPROVING THE RESPONSE TIME FOR HIGH SPEED CONTROLLERS

A second problem, getting commands to an NPR-controller, Kio fast, can be solved in a similar way. Although in principle, it could be handled by double buffering in the controller.

In this case, a block of instructions are sent to the controller at interrupt level. This could be accomplished in several ways, including a block transfer instruction. Most likely, this instruction should be executed at a high priority level, and an interrupt caused to a lower level, signifying command completion. This needs to be worked out based on our current K's.

*Pc--central processor; Pio--I/O processor (IBMese=channel)-- a device which executes commands (instructions) from a stored program the Pio is interpretting; Kio--io controller--simple device to execute 1 instruction at a time.

GB:mjk

digital INTEROFFICE MEMORANDUM

TO: OOD

CC: Mark Abbett

DATE: April 1, 1975

FROM: Gordon Bell

DEPT: OOD

EXT: 2236 LOC: ML12/A51

SUBJ: OOD STAFF MEETING AGENDA--April 3, 1975

12:30 Lunch	Format/purpose of OOD staff meetings	OOD
1:30	Yellow Book--a monster?	OOD
2:15	Standard Microsystems Proposal	Bastiani
2:45	LA36 RFI report (material attached)	OOD
3:15	Development Managers Committee Meetings (material attached)	OOD
3:30	Operating Systems (material attached)	OOD
4:00	Organization--Displays, LSI Eng. & Simulation	OOD
4:30	Budget Status & Schedule	Laut

FUTURE AGENDA ITEMS

Date	Topic	Responsible
4/24	EEO Position	John Sims
4/24	DEC Safety Standard	Mondani/Minezzi
4/24	Presentation of Patents (Delagi, Gray, Wade, Cutler, Siekman)	Siekman
4/24	Presentation of Eng. Mgrs. Seminar Design	Cronkite/Abbett
4/24	Job responsibility statements from OOD members for PM	Cronkite/Abbett
5/1	Engineering process	Best
Q4	Production Communications	Smith/Cudmore
?	2x2 Report	Puffer

digital

cc. Staff Mtg. #1124

INTEROFFICE MEMORANDUM

TO: Gordon Bell — LOC/MAIL STOP ML12/A51
Dick Clayton — ML5/E71
Phil Laut — ML12/A16
Larry Portner — ML12/A62

DATE: March 20, 1975
FROM: Bob Puffer
DEPT: Hardware Development
EXT: 2863
LOC/MAIL STOP: ML1/E38

MAR 21 1975

SUBJ: Yellow Book (For Staff Meeting Discussion)

This morning I read the February Yellow Book. I'd encourage you to do the same. Gentlemen, we've created a monster.

I had only glanced through the December and January copies, reassuring myself that I'd already read most of it anyway. In fact, besides the reports from my group, I do get many of the other reports directly (I'm not sure why) so that it is the second time through for at least one-third of what's there. But the real reason I'd been less than thorough in December and January is that the book is so thick and so intimidating and so full of (to me) meaningless detail that I can't cope with it. I'm not sure who can - certainly not the Marketing Committee or the Product Line Managers.

I propose one person (the new Al Sharon, whoever he is) be assigned to go through the book, reformat the index, eliminate the junk mail, and end up with a book 1/3 the size that is an overview rather than the infinite details of alphabet-soup projects.

Some points to consider: (1) How come Dick and Larry don't write monthly reports? Should I bother or are the next level reports all that's needed?

(2) There are 20 pages of Field Service component failure and inventory data starting at 3.1.5. This is useless to me and I can't believe anyone reads it. Who is it for?

(3) Some of the indexed authors never submit reports. Bill Hogan has never (to my knowledge) submitted a report, Tom Stockebrand hasn't had one since December, other areas are spotty at best.

(4) The software report at 9.1.1 is an untitled and unauthored list of neat mnemonics that I can't possibly decode. I can't even figure out what computers some of this stuff is for.

(5) The 34 pages of EDP gobbledygook starting at 12.0 has got to go. Did you realize we were planning to spend $62,340 on "HRSDB"? I didn't either, but I'm sure glad I know now!

(6) A monthly report should never exceed two or three pages. Ralph Platz uses CS2 to unfair advantage and generates 10 pages; George Plowman weighs in at 13 pages; and Jim Bell manages 12 pages on research! Good grief! Do even their bosses have the patience to read this?

Let's agree to stop this ecologically unsound production and return to something useful.

rml

Dick Clayton for OOD agenda. C1420

digital INTEROFFICE MEMORANDUM

TO: Ken Olsen

CC: Gordon Bell
Julius Marcus

DATE: 25 MAR 75

FROM: Vince Bastiani VB MAR 27 1975

DEPT: DECcomm Engineering

EXT: 3292 LOC: ML5-3/E43

SUBJ: STANDARD MICROSYSTEMS PROPOSAL

The enclosed proposal describes a joint venture between Standard Microsystems and Digital Equipment to develop an LSI chip usable for synchronous communications interfaces.

This chip would be extremely useful to us, as it would replace over 50 discrete IC's and would be usable in two or three project currently under design or being contemplated. Hwever, since the chip basically defines a serial synchronous communications function which is of use to anyone doing serial synchronous communication, I feel that to achieve an eventual lower cost part, the chip should be developed as a standard product. This should result in eventually having multiple sources and hence, a lower cost could be achieved in the long term. The disadvantage, of course, is that we are providing SMC with some of the expertise to build the chip.

It was my understanding that you had some concern over an identical situation regarding the UART, where we essentially provided some specification expertise as to what the chip should do. I would like to know your comments about pursuing the matter in regard to this particular chip.

/bt

SMC Microsystems Corporation
35 Marcus Boulevard
Hauppauge, New York 11787
(516) 231-5151

To: Gordon Bell 1431

We intend to pursue

Vince

Please check this OK?
with Dick Clayton & Peter

March 14, 1975

Gerald Gollub
vice president marketing
(516) 273-3100
TWX 510-227-8898

MAR 24 1975

Digital Equipment Corporation
146 Main Street
Maynard, Massachusetts 01754

Attention: Mr. V. Bastiani

Subject: SDLC Proposal

Gordon
OOD

Vince Bastiani

Staff mtg. Review with the Serial Multi-Drop Prod. Mgr.

Dear Mr. Bastiani:

SMC Microsystems Corporation would like to propose a joint venture between SMC and DEC for the purpose of producing a MOS/LSI SDLC communication device. SMC will supply the MOS/LSI design and manufacturing expertise and DEC will supply the SDLC product support. (Bill Avery?)

No OK

DEC/SMC will jointly generate an overall specification including: TTL schematics, timing diagrams, and overall circuit functionality. At a minimum SMC will produce a device acceptable to DEC which may also include some features based on SMC's product market survey.

It is understood that DEC and SMC have mutually committed to support each others requirements; in this regard DEC will commit to solely support SMC in its development efforts and SMC will commit to give DEC requirements (both design and production) highest pricrities within SMC.

Based on an initial market survey there appear to be three general areas of concern:

1. When does the market need an SDLC device
2. Will IBM change the CRC character
3. Will IBM change the SDLC format, ie. 7 bit data word, 6 bit data word, etc.

In all of these areas we are prepared to accept DEC's guidance.

In order to begin this venture an understanding of the business considerations is required. We at SMC need a firm commitment for a minimum of 2,500 pieces to be procured within the first year after prototype delivery. In addition, an agreed to production price must be established.

SMC is prepared to offer DEC a price of $32.00 for the first 2,500 pieces with a projected price of $15.00 to $20.00 thereafter.

We at SMC are prepared to undertake the design of the SDLC chip within 3-4 weeks after signing an agreement with DEC. Initial prototypes can be expected within 6 to 7 months, with production quantities to follow within 4 weeks.

Used in IPL, DUP11 (SDLC interface)
and Newer Serial Buses!

Summary

1. SMC is prepared to commit to a price and schedule for an MOS/LSI device for SDLC.

2. SMC needs to have a firm commitment from DEC which represents DEC's first year requirements.

It is SMC's desire to initiate and develop long-term relationships with select customers which we believe is best achieved by providing a competitive edge, both technically and price-wise in the market-place. We are confident in our ability to materially contribute to the satisfaction of this need. We appreciate the opportunity to provide this letter proposal and welcome an opportunity to discuss any or all elements in further detail at your convenience.

Very truly yours,

Gerald Gollub

Gerald Gollub

GG/cb

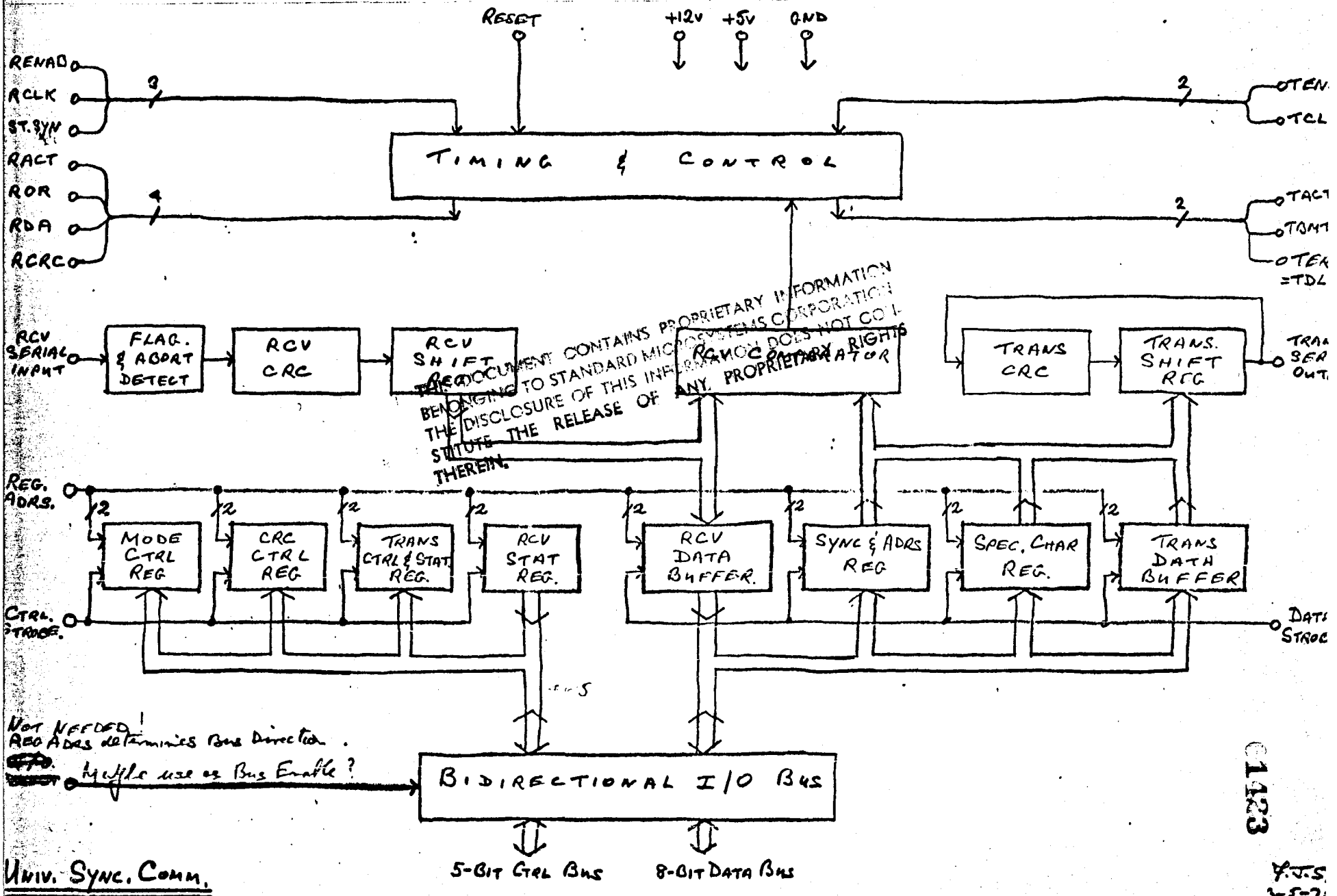
cc: D. Lutzick - J & J
F. Zereski - DEC

SDLC / BISYNC SEL
SEC ADRS MODE
FULL / HALF DUP
LOOP-AROUND

CRCC16 / CCITT SEL
CRC INH
—
—

TSOM
TEOM
—
TERR ?

RSOM
REOM
RSPCH
RERR



UNIV. SYNC. COMM.

Y.T.S.
3-5-7

G. Copy → Hardware Engineering Mgrs | FYI Hood Gray Jim O'L

Bob, let's identify sources for establishing European, Canadian and Japanese requirements. Jim: evaluate and let us know if we can meet them. Dave MAR 25 1975

INTEROFFICE MEMORANDUM

SUBJECT LA36 RFI Report DATE March 10th, 1975

TO Al Huefner ML 1-3,E26 FROM Dave Chertkow

c.c.: Gordon Bell ML 12-1,A51
Bob Puffer ML 1-3.E38
Horst Kuhn Munich

1424

Attached, (on Al's copy only) is the report covering LA36 RF1.

The conclusions are that the LA36, in its present form does not meet German requirements and therefore will not be granted a general license for sale in Germany.

Gordon, as we discussed during my last Maynard trip, meeting European standards is becoming very critical to the continued acceptance of our products. I still feel that there is little sensitivity on the part of Engineering to help us overcome these problems through consideration of European requirements during initial design.

I would appreciate your comments.

Regards.

to: Gordon Bell
Dick Clayton
Bill Demmer

How much longer is it viable for each Product Manager to be in his/her own in these matters? Could we please have some central help.

Bob Gray

1125

digital INTEROFFICE MEMORANDUM

Larry t | Bob + Dick + Mark + Staff Mtg

TO: Distribution DATE: February 26, 1975

FEB 27 1975

FROM: George W. Plowman

DEPT: Diagnostic Engineering

EXT: 3329 LOC: ML21/E20

SUBJ: DEVELOPMENT MANAGERS COMMITTEE MEETING - FEBRUARY 19, 1975 MEETING MINUTES

Those in attendance at the subject meeting were:

Pete Conklin*
Ed Fauvre*
Jack Mileski*
George Plowman*
Ed Wright (Guest)
Pat White (Guest)

Is such a structure worth having? Should much of this be done at your staff Mtgs, alone, & Eng. Committee, Special Mtgs (ala Worcester), etc. I.e. is there an economy of scale here? Gordon.

Absent were: Hank Spencer
Bill Slack*
Pete van Roekens*

Project Plans and Specifications

The responsibility for developing drafts for Project Plans, Functional Specifications and program Design Specifications were accepted as follows:

Project Plans - P. Conklin - Draft due 3/17
Functional Specifications - P. van Roekens - Draft due 3/17
Program Design Specifications - J. Mileski - Draft due 3/17

or does Larry's Committee just fill a much-needed gap?

Inputs relative to the above documents should be given to the responsible individuals by 2/28 for their review and consideration. It is desirable that the drafts for Project Plans and Functional Specifications be distributed one week prior to the March 19th committee meeting, so that any issues of concern can be discussed and resolved at that meeting.

Mechanics of the Product Development Process

In keeping with the goals outlined at Larry Portner's February Woods Meeting, it is the intent of the committee to have the basics of the development process defined and implemented by June 30th. In order to achieve this date, we will concentrate on a phased implementation of the development process wherever possible. The methodology that we are going to follow will be to work within the framework of the "total" development process model. Specific emphasis however, will be placed on those processes that relate specifically to the development activities, with the intent of further defining the model and incorporating other aspects of the total process itself as they become defined.

In order to bring the model of the development process into focus, the committee Chairman is responsible for generating a Cursory Project Plan and Ed Fauvre and

* Committee Members

Pete Conklin acting in the capacity of co-architects will generate a Concepts Overview. Preliminary drafts of these documents are due in two weeks. Following the creation and review of the above, it is our intent to develop Functional and Design Specifications and further delineate the additional phases required to make the process operational. Jack Mileski accepted the responsibility to provide the reliability/human factor relationships concerned with how we "sell" and implement the program as well as a follow up post-mortum on the results.

Management Policies and Procedures Manual

The introductory memo that Jack Mileski is drafting for Larry Portner's review was discussed. It was suggested that Jack place some added emphasis on short and long range implications to the company as additional support for the need for these policies. In all other respects, the committee accepted the memo. Jack will redraft the memo and submit it to Larry Portner for review.

The committee discussed the mechanics and how the policy manual would be controlled, and the requirements for conveying general information to the user of the manual relative to how policies may be added or changed. All members agreed that something would have to be drafted and included in the manual to solve this problem.

Jack Mileski expressed some concern about introducing the manual prior to having a clear concept of the "total" development process. This was discussed at length, but felt to be less consequential than holding back the release of the manual. It may be possible to provide a concepts overview for inclusion with the initial distribution of the manual, which is presently planned to be done no later than the end of March. The inclusion of this in the initial release will depend on the progress made by Ed Fauvre and Pete Conklin in defining the development process.

International Conference on Reliable Software

Larry Wade had circulated the notice of the above subject conference recommending that several people within the software development organization attend. The committee agreed that Jack Mileski and Ed Fauvre could, subject to Larry Portner's approval, attend the conference on behalf of the development groups and would be responsible for aggressively exposing the information gathered to the entire organization. Jack Mileski suggested that we might also combine the trip with some recruiting since Xerox is located in the immediate area.

Policy/Standard Reviews

The committee discussed the method for handling policies or standards at the committee meeting and decided that any policy or standard seeking ratification from the committee must be in the hands of the committee members at least one committee meeting prior to the meeting scheduled for the ratification of that policy or standard. This will insure that an adequate amount of time is provided for review.

Next Meeting

The next Development Managers Committee meeting will be held on Wednesday, March 5th in my office at 21-4. The agenda for this meeting is as follows:

Review Final Format of Specification Control Policy - 15 minutes

Final Review of Development Review Policy	- 15 minutes
Draft Review of Software Schedule Review Policy	- 30 minutes
Discussion of Development Process Model	- 1 hour
Cursory Plan and Concepts Overview	

rd

Distribution:
Gordon Bell
Jim Bell
Peter Christy
Pete Conklin
Ed Fauvre
Oleh Kostetsky
Jack Mileski
Dave Palmer
Larry Portner
Bill Slack
Hank Spencer
Pat Spratt
Nate Teichholtz
Pete van Roekens
Larry Wade
Pat White
Mel Woolsey
Ed Wright

SUBJECT: Software Engineering Development Managers Committee Minutes

STATUS AS OF: FEBRUARY 19, 1975

ISSUES	RESPONSIBLE PARTY(S)	DUE DATE	ISSUES/COMMENTS
Management Policies			
Code Reviews	P. van Roekens	Jan.1,'75	Not to be issued as general policy
Development Reviews	G. Plowman	" " "	Policy rewritten in release format - complete
Schedule Review	P. Conklin	" " "	Drafts undergoing review
Specification Control	E. Fauvre	" " "	Being rewritten in release format
Software Compatibility	B. Slack	Schedule Due Jan.1, '75	Being addressed by Software Compatibility Committee B. Slack - Chairman
Cataloging and Administration of Management Policies	G. Plowman	Feb.1,'75	Organization and format resolved - Initial release planned by 3/31/75
Project Management System			
Definition of Terms and Plan for Implementation	B. McNerney	OPEN	Effort ongoing. Schedule for next review not established.
Supervisor/Project Leader Training	J. Murphy	Jan.22,'75	To agree on Plan and assign responsibility for implementation. Modules 1 and 2 to be ready in March.
Guidelines for:			
Project Plans	P. Conklin	3/17 DRAFT	
Functional Specs	P. van Roekens	3/17 "	
Design Specs	J. Mileski	3/31 "	
Job Descriptions			
Managers	Jim Murphy		Individual comments are due to Murphy
Supervisors	" "		
Future Agenda Topics:			
Productivity and Process Technology			
Structured Programming			
Reusable Code			
Use of Bliss			
Project Notebook			
Performance Review			
Technical Training Plan			
Development Process Model	G. Plowman	MAR. 3,'75	Cursory Project Plan
	Conklin/Fauvre	MAR. 3,'75	Concepts Overview

SUBJ: OPERATING SYSTEMS

DATE: 03-04-75
FROM: GORDON BELL

* *
PLEASESEND TO: FILE
* *

SUBJ: OPERATING SYSTEMS

TO: LARRY PORTNER

CC: DOD

I believe we've really a disaster in the works vis a vis the mushiness of existing operating systems (and computers?).

At the high end GPTSS (which already seems too late):

1. RSTS (or TOPS 11)
2. IAS
3. RSX with swapping and scheduling (in progress)
4. RT with multi programming.
5. 11/85

At the low end:

1. RSX-11/M
2. RSX-11/S
3. RT-11

With the price of 5K of memory moving to be about $100 (also the price of a cheap service call), I have trouble understanding the low end, low core request for 2 operating systems which have identical functional capability. (Say we sell 10,000--that's only 1 million savings to handle manuals, training, support, standards, etc. etc.)

The next disaster in process could quite easily be using the PDQ WCS to enhance FORTRAN on RT11 to get a bigger memory in lieu of using a larger address space which we have to define.

I believe the two PM's involved here have to come at this from a business viewpoint. The development costs and incremental memory costs are the trivial costs, the rest will kill us.

SUBJ: OPERATING SYSTEMS

DATE: 03-04-75
FROM: GORDON BELL

Let's discuss this at staff meeting so that the review of these quite black and white hot issues can be looked at.

Unlike the CPU strategy that requires explicit tool up dollars in production and we kill; operating systems get us in subtle ways. Have we ever not released software that was done?? (Remember the work we have on DOS, and how we're unable to sell new hardware to these users unless we continue massive support?) We really can NEVER drop an operating system once it gets in the field.

Larry, please position the primate on your posterior.

GB:mlk

data general INTEROFFICE MEMORANDUM

TO: OOD

DATE: April 10, 1975

FROM: Dick Clayton

DEPT: OOD

EXT: 3638 LOC: ML5-2

SUBJ: OOD STAFF MEETING AGENDA--April 10, 1975

12:30 Lunch	CDLC Chip Analysis	Bastiani
1:15	Set on date and outline of Jungle meeting (late April). Topic: Help Dick & Larry set systems orientation and better integration of hardware/software development.	OOD
1:45	How can OOD best use Ed Schein?	OOD
2:15	Gordon's assignment of tasks to other OOD members.	OOD
2:30	End	

FUTURE AGENDA ITEMS

Date	Topic	Responsible
4/24	EEO Position	John Sims
4/24	DEC Safety Standard	Mondani/Minezzi
4/24	Presentation of Patents (Delagi, Gray, Wade, Cutler, Siekman)	Siekman
4/24	Presentation of Eng. Mgrs. Seminar Design	Cronkite/Abbett
5/1	Job responsibility statements from OOD members for PM	Cronkite/Abbett
5/1	Engineering process	Best
5/1	Corporate Package	Clayton/Puffer
Q4	Production Communications	Smith/Cudmore
?	2x2 Report	Puffer
Jungle	Effective Systems: How do we do it?	OOD

D I G I T A L INTEROFFICE MEMORANDUM C1432

PAGE 1

SUBJ: MY DUTIES DURING 11VAX WORK

DATE: Ø4-Ø8-75
FROM: GORDON BELL
EX: 2236
MS: ML12-1/A51

TO: FILE

To: Ken Olsen

During this period which I hope will last only until June 1, I would like to distribute my activities as follows:

Operations Committee: Larry will attend as rotating member, I will try to attend sections of meetings on OOD relevant issues.

Salary Review: I'll attend, but would like to leave early.

Woods: attend as needed--work on alts as needed

Manufacturing Engineering: Bob chairs and represents. I'd like to drop out for now. OOD should decide whether we add another member.

Eng. Committee: drop out completely for now.

Staff meetings: Dick will be the secretary, and in my absence, also run the meetings.

Marketing Committee guest: someone from OOD as needed. I found it very useful to attend during the reviews leading to budget due to product/market overlap. (I would like to continue this on ad hoc basis when 11VAX settles down.)

Products Committee: R. Puffer, Chairman

PSG Review Meetings: not attend

Packaging: Is it really yours (and Bob's and Dick's and every P/L which has to do their own because the standard is poor)? Dick and Bob should really have a plan by 5/1/75 to significantly improve packaging.

Interface to CONN: Dick, Larry and Julius. The integrated plan should be presented to OOD by 5/1,

Interface to displays: Tom is now reporting to Bob. I will

SUBJ: MY DUTIES DURING 11VAX WORK

DATE: Ø4-Ø8-75
FROM: GORDON BELL
EX: 2236
MS: ML12-1/A51

keep involved only to the extent needed to insure VT5Ø++ has 24 lines and lower case. Also, the VT51 should slip to the rumored extent it has, otherwise it becomes non-useful. The terminals strategy is thoroughly on Bob (for products), Andy (for components marketing) and Marketing Committee (for end user). It must be restated and reviewed in light of budget.

Mail: Intend to read and react less,

GB:mjk

CC: OOD, Bill Demmer, Bill Thompson, John Fisher

What is Husting up to.

DIGITAL INTEROFFICE MEMORANDUM

SUBJ: OOD AGENDA

DATE: 04-23-75
FROM: DICK CLAYTON
EXT: 3638
MS: ML5-2/E71

TO: ~~FILE~~ Clayton

SUBJ: OOD STAFF MEETING AGENDA--APRIL 24, 1975

10:30	EEO Position (Information)	John Sims
11:00	DEC Safety Standard Information (Is it coming together)	Mondani/Minezzi
11:30	Responsibilities of OOD members (Ken's memo attached)	OOD
12:00	What can we learn about Engineering Mgt? (MIT course material attached)	Bell
12:15 Lunch	Presentation of Patents--Delagi Gray, Wade Cutler	Slakman

10 30

FUTURE AGENDA ITEMS

Date	Topic	Responsible
~~5/1~~ 11:00	Job responsibility statements from OOD for Product Managers (Invite Abbett/Cronkite) 30 min.	Clayton/Puffer/ Portner
5/1 11 30	LSI Engineering Goals, Resource allocation, Projects (written material distributed by 4/28/75) 45 min.	Gale 2045
5/1 12 15	Status report on 32 bit project 15 min;	Bell
5/8	Woods outline, goals, schedule 30 min;	Portner
5/8	Depeyrot's white paper on testing; Open discussion of software, system, hardware, Field Service, Mfg, roles and potential changes in pressure on	OOD

10 30

SUBJ: OOD AGENDA

DATE: 04-23-75
FROM: DICK CLAYTON

goals of various groups and the company. 1 hour

5/8 Status of Corporate Packages — Puffer/Clayton
30 min (written material ahead of time)

Q4 Production Communication — Cudmore/Smith

RC1mJk

? Communication Interface with Hardware and software — Marous et al

? 2x2 Reporting — Puffer

Jungle--Effective Systems: How do we do it? — OOD

DIGITAL INTEROFFICE MEMORANDUM

SUBJ: OOD AGENDA

DATE: 04-28-75
FROM: DICK CLAYTON
EX: 3639
MS: ML5-2

TO: FILE

SUBJ: OOD STAFF MEETING AGENDA--MAY 1, 1975

12:30	Responsibilities of OOD members (Ken's memo attached)	OOD
11:[illegible]	Job responsibility statements from OOD for Product Managers (invite Abbett/Cronkite)	Clayton/Puffer/ Portner
11:[illegible]	LSI Engineering Goals, Resource allocation, Projects (Written material to be distributed)	Gale
12:1[illegible]	Status report on 32 bit project	Bell

FUTURE AGENDA ITEMS

Date	Topic	Responsible
5/[illegible]	Goals outline, goals, schedule 30 min	Portner
5/[illegible]	Segoyrait's white paper on testing Open discussion of software system, hardware, Field Service, Mfg, roles and potential changes in pressure on goals of various groups and the company 1 hour	OOD
5/[illegible]	Status of Corporate Packages (Written material ahead of time) 30 min	Puffer/Clayton
Q4	Production Communication	Cudmore/Smith
?	Communication Interface with hardware and software	Marcus et al
?	2x2 Reporting	Puffer
Jungle--Effective Systems: How do we do it?		OOD

DIGITAL

INTEROFFICE MEMORANDUM

1437

		LOC/MAIL STOP
TO.	Dick Clayton	ML5-2/E71
Cc:	Bob Puffer	ML1-3/E38
	Larry Portner	ML12-2/A62
	Henry Lemaire	ML1-5/E64
	Gordon Bell	ML12-1/A51

DATE. April 15, 1975
FROM. Ken Olsen
DEPT. Administration
EXT. 2300
LOC/MAIL STOP. ML12-1/A50

SUBJ. RESPONSIBILITIES OF OOD MEMBERS

I will not be able to make the meeting of your committee on April 24 but I would like you to list the responsibilities of the OOD members.

Instead of discussing Gordon Bell's responsibility and what we expect of the top man, I would like to turn the discussion around. I would like to have you write down what the responsibilities are for each of the members of the committee and then afterward make a list of what is left over for Gordon Bell.

/ma

digital INTEROFFICE MEMORANDUM

1438

TO: Henry Lemaire

DATE: 4/16/75

FROM: Lorrin Gale

DEPT: Micro Products

EXT: 2045 LOC: ML1/E61

SUBJ: DEPARTMENT PLANNING/APPROVAL STRATEGY

This is the game plan I'd like to follow to ensure that we move as quickly as possible, yet operate within corporate policies, in control and low risk/exposure.

1. Your review enclosed, I'll coach so you understand enough.

2. We must get basic approval - determine inside versus outside hires.

3. Complete project sheets, quartize and CC allocate.

4. Do our internal CC worksheets, manpower (cap. - equipment done and turned in already).

5. Hold broader review with OOD, system engineering who are going to use us, key Worcester, test, etc. - maybe 30 people - give out copies of planning book.

6. In addition, we have to immediately resolve the following issues which affect the FY76 budget.

    1. Process technology contract with Signetics.
    2. Second hand source funding committments.
    3. Q4, 1 hiring for reqs. already approved.
    4. WD second source.
    5. LA36/180 proposal.

Lorrin

/trl

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C1439

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B. Second hand money

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(b) almost - projects not approved but funds set aside

(c) wish list - no approval, no money

B. Description, costs

C. Coalescing activities into projects and responsibility

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A. Schedule

B. Outside versus inside

C. Job descriptions

VI. DEPARTMENT BUDGETS

A. Capital

B. Cost center worksheet (includes labor)

C. Project sheets

digital INTEROFFICE MEMORANDUM

TO: Henry Lemaire
CC: Roger Bedard
Joe Chenail
OOD

DATE: 4/17/75

FROM: Lorrin Gale

DEPT: Micro Products

EXT: 2045 LOC: ML1/E61

SUBJ: DEPARTMENT PLANS FY76

1. We have a set of projects and costs which range between 780 and 1,312. Source funding has been identified as follows:

From Central	780
"Second Source"	532
	1.312

2. From past experience, it has been proved unwise to count "too heavily" on second hand allocated funds from the system engineering groups and thus, I state our plans in terms of a "range" at this time.

3. Project/activity costs are listed on attached sheets starting with first priority items and ending with the"wish list". First priority items are solidly funded through Central Engineering and not suprisingly, maintains this department at its current manpower level.

4. As usual, we have many more "things" we would like to do than money available permits. Nevertheless, should the economy improve, we have included the wish list.

5. To support the 1.31M budget, we will have to increase the manpower in the department from 20 to 37 people. Present corporate outside hiring policies will have to be reviewed for this unique situation before we bother to fine-tune the numbers any further.

6. On a more positive note, DEC semi-activity is increasing by leaps and bounds. I'm pleased with upper management support, tolerance, and even patience. Corporate wide semi-design/manufacturing expenses will exceed 25M annual rate by FY79. We are on the right track and it's now a question of maximizing the payoff for these present and future semi investments.

7. To put our growth in perspective, last year we received from Central Engineering 726K to set-up the department and start 3 chips. We didn't receive any money from the benefactors of these chips, namely the system engineering groups. This year we are planning on an 780K subsistence level funded by central, but, our real product development funds will be coming from the systems engineering groups. Thus, our department expansion of up to 75 percent will be the direct result of our ability to "sell" our services to other groups.

8. In general, semiconductor talent we acquire is not transferable. Thus, it is with extreme caution I hire professionals based on non-central engineering funding. I've found that so-called "second hand" money can disappear in an instant. To stabilize this scene, I'm insisting on a few rules:

   (a) Money remains in place for 12 months.

   (b) If a project is cancelled, funding continues at a reduced level, but, sufficient to support my people in the project until they can be reassigned to other projects.

   (c) New chip starts require three to six months to put in place new people, contracts, etc.

9. Next year I intend to strengthen our ties with the semi-industry by setting up additional technology contracts beyond our present Signetics arrangement. In general, these contracts tend to (a) force communication (b) reduce the risks of totally screwing up a specific chip, and (c) allow more accurate scheduling. We will possibly set-up contracts covering:

   (a) LS process technology

   (b) I^2L circuit design and layout

   (c) MOS circuit design and layout

   (d) CAD

10. I'm not too concerned about being able to get semiconductor information as a result of our Worcester announcement. We will be shut-off proportionately to our ability to be self-sufficient and capable. The halfway point is out at least three years.

/trl

C1442

DEC BIPOLAR CUSTOM DEVELOPMENT

SCHEDULE - APRIL 23, 1975

	FY 75	76	77	78	79	TOTAL
CHIP DESIGN STARTS	2	7	10	14	19	52
UNIT VOLUME (K UNITS)	5	47	343	962	1,547	2,939
PURCHASE COSTS	2	350	2,021	4,685	6,553	13,614
COMPONENT SAVINGS	Ø	355	1,904	4,999	7.710	14,948
DEVELOPMENT						
(a) Central	700	780	936	1,123	1,348	4,887
(b) System	Ø	532	798	1,197	1,796	4,323

NOTES:

1. Includes LS and I^2L products.
2. 1977, 1978, and 1979 chip definitions have not been finalized. Their volume and sales for period considered are 630K and $2.7M respectively.
3. Presume sales are generated and start one year after "chip design start".
4. Sales mean "purchase price totals" from all sources.
5. DEC fiscal year runs July 1 to June 30.

/trl

FUNDING SOURCES

I. FROM CENTRAL			
A. February Woods Meeting	- Simulation	300	
	- LSI and Worcester	1,200	
			1,500
B. Second Wood's Meeting	- rev. #1		
P. Laut memo 3/26/75	- Simulation	280	
	- LSI	500	
	- Worcester	1,630	
			2,410
II. FROM P.L.'s AND SYSTEMS DEVELOPMENT			
A. LSI-11 project worksheet S. Teicher 3/13/75 rev. 3 - Q chips		217	
B. LSI-11 MOS circuit analysis		20	
C. Communications	- SDLC	20	
	- Multi-drop	50	
D. IPG	- SDLC	20	
E. Semi-memory engineering	- MOS Circuit Analysis	20	
F. Unicorn		65	
G. Test Engineering		120	
			532
			2,942
III. SUMMARY			
A. Semi-manufacturing		1,630	
B. Engineering		1,312	
			2,942

IV.

As of 4/16/75 we do not have written confirmation of source funding for B through G of section II which totals 315K.

- we do not intend to commit resources, establish vendor contracts, hire people or in any way, create an obligation for these activities without confirmation.

/trl

FY76 MICRO PRODUCTS ACTIVITY LIST

-FIRM-
APPROVED - MONEY AVAILABLE

1.	R.	Unicorn	65
2.	R.	Unibus	20
3.	R.	Signetics interchange	80
4.	B.	Sage II Support	135
8.	R.	Worcester Support	20
9.	B.	Applicon Support	18
10.	R.	Technology Planning	50
11.	J.	Undefined CHips	90
12.A	J.	Q Chips I	117
13.A	J.	MSC I	95
17.	R.	SDLC	40
18.	R.	Multi-drop	50
			780

-ALMOST-
NOT APPROVED - MONEY AVAILABLE

5.	J.	Applications Support	30
7.	R.	I^2L Design Study	30
12.B	J.	Q Chips II	100
13.B	J.	MSC II	100
15.	B.	Logic Schematics	18
16.	B.	Interconnect Vertifier	27
19.	B.	Circuit Analysis	36
20.	B.	Link to Sync.	9
21.	B.	Runoff + Plot	35
22.	B.	Signetics Phone Link	9
23.	B.	Fault Simulation/Test	120
24.	B.	UDDT	18
		SUB-TOTAL	532

1,312

-WISH LIST-
NOT APPROVED - NO MONEY

6.	R.	MOS Interchange	50
14.	R.	LS Family	50
25.	J.	Video Chips	70
26.	J.	Industrial 8 bit CMOS	20
27.	R.	WDC 2nd Source	80
29.	R.	Lectures and Consult Fees	30
30.	R.	Hybrid Assembly	30
31.	J.	LA36/180	70
32.	B.	Sage/LSS	18
33.	R.	Second Outside Bipolar House 1/2 year	30
34.	R.	CDI, EFL Investigation cost could be covered in Technology Planning	

digital INTEROFFICE MEMORANDUM

TO: Lorrin Gale

DATE: 4/9/75

FROM: Rony Elia-Shaoul (1446

DEPT: Micro Products

EXT: 2102 **LOC:** ML1/E61

SUBJ: FY76 BUDGET

1. UNICORN PROJECT ($65K)

   This cost includes second source vendor ($25K), $15K material at Signetics, $25K labor at DEC. Refer to my budget on that.

2. UNIBUS PROJECT ($20K)

   This cost includes $8K for second iterarion materials at Signetics and $12K labor at DEC.

3. I^2L DESIGN ($30K)

   This covers about one engineer full-time to track the I^2L design at Signetics and other vendors and actually, work on DEC design @ Q3. This design can be the multidrop chip.

4. SIGNETICS INTERCHANGE ($80K)

   Covers Martins Skele at Signetics full-time plus travel ($60K) and $20K for I^2L interchange.

5. WORCESTER SUPPORT ($20K)

   This covers a circuit engineer full-time starting Q3 to provide a liason between engineering in Maynard and manufacturing at Worcester to second source the Unicorn, Unibus, and Q chips.

6. TECHNOLOGY PLANNING ($50K)

   This covers 3/4 of Tony's time to bring into DEC the latest information of the Technology a product issue. ($30K). Also, includes $10K to cover material cost of two test chips I^2L and EFL? And, $10K to cover one time Hybrid assembly costs for two to three chips.

/trl
Attachment

digital INTEROFFICE MEMORANDUM

TO: Lorrin Gale

DATE: 4/10/75

FROM: Bob Kusik

1447

DEPT: LSD

EXT: 3744 **LOC:** ML1/E61

SUBJ: FY76 PROJECTS

Next years projects can be grouped into four areas; SAGE II (logic simulation), graphic processing (Applicon), circuit analysis, and simulation/testing. This memo describes these projects at a functional objective level, their costs, and funding sources.

SAGE II

SAGE II will be completed during Q1 FY76. By the fall, we will have a responsibility to train and support the user community. The addition of UDDT (an interactive debugging facility for microprograms) will extend the utility of SAGE II significantly.

GRAPHIC PROCESSING

Today we use the Applicon as a graphics editing system for mask layout. Next year, we will extend the capabilities of the system for creating logic and circuit schematics and their machine readable wire lists, and the standard cell library data base. This will enable us to link the system to SAGE II and SINC (circuit analysis system). More significant, however, will be our ability to analyze the metal layers which interconnect cells (transistor or logic) and compare the networks to the circuit or logic schematics.

We will also continue to support the growing user community. A second editing station is anticipated, and a phone link will be established to the West Coast to facilitate the interchange of design data bases. The Applicon system will be married to RUNOFF so that we can intermix figures with text and output composit documents on the Versatec.

CIRCUIT ANALYSIS

We will bring in house a MOS circuit analysis system (we have SINC for LS bipolar). In addition, we will develop an understanding of circuit modeling so that we can evaluate new models as they come along and anticipate limitations of the systems which we use.

SIMULATION/TESTING

SAGE II has been developed as a validation tool for design engineers. It is capable of performing fault insertion, but it is slow, clumsy, and it models with unnecessary detail. The execution guts of SAGE II will be augmented with a new data structure,

basic scheduler, and a collection of simple function models optimized to the test related tasks of fault insertion, fault dictionary generation, and test sequence coverage measurement.

FY76 PROJECT COSTS

SAGE II	$153K
Graphic Processing	$107K
Circuit Analysis	$ 45K
Simulation/Testing	$120K
	$425K

LSI CAD (CC 377) FY76 FUNDING SOURCES

Central	$280
Memory Eng.	$ 20
LSI-11	$ 20
Test Engineering	$120
	$440K

/trl

digital INTEROFFICE MEMORANDUM

TO: Lorrin Gale

DATE: April 4, 1975

FROM: John Hughes

DEPT: Micro Products

EXT: 6453 LOC: MLI/E61

SUBJ: PROJECT AND ACTIVITY DESCRIPTIONS

Here are the project and activity descriptions that you requested to go along with our budget.

Q Chip Project

We will be developing a series of support chips for the 11Q05 (LSI-11) system. These support chips are aimed mainly at reducing the size and cost of frequently repeated interface functions. We are already working on three chips in the group, they are:

- An interrupt chip
- An address latch and protocol chip
- An 8 bit slice digital I/O chip

During fiscal 1976 we expect to start production on at least 4 chips and the well end of the design phase of 2 more.

Micro Sequence Control (MSC)

The MSC project is aimed at developing a standard microprocessor for implementing peripheral control. During FY76 a large portion of the project will be to implement a peripheral prototyping system that will make the microprocessor easier and faster to use. We will also be developing the micro sequence control chip, which provides all of the sequencing and memory control for the microprocessor that we have designed. We expect to design and implement a number of other chips during FY77 for the peripheral microprocessor system.

SDLC Project

We are working with DECCOM engineering to specify a chip to handle the SDLC synchronous communications protocol. We expect that work will be started on this project during FY75 but there will be a lot of follow-up during FY76. The majority of the development activity will occur up at the vendors because there is a severe time constraint on developing this chip, and also because low power Schottky (the technology that we are presently working with) is not suitable for this application.

Serial Bus (Multidrop)

We are going to develop a proprietary serial bus, message protocol chip that will operate in conjunction with the SDLC communications protocol. DECCOM engineering will be doing the design and specification for the chip. Our present plans are to implement it in I^2L technology.

Application Support Activity

During FY76 we would like to add one logic design engineer to the group, who will work with other engineering groups in the company to partition and specify chips for new peripheral and processor designs. He will as well, look into a number of existing designs with a view to specifying chips that can be phased into production for cost reduction purposes. The application support activity is aimed at specifying product specific chips rather than general purpose chips.

Video Chip

We have done some work already to specify a video frequency source chip that would be used to provide timing signals for all of the various video requirements (i.e. horizontal sync, vertical fly-back, video blanking, etc.). We may develop this chip as a custom or a standard. If it is to be developed as a standard we will specify the logic and release the design to a number of suitable vendors. The A/N group may have difficulty funding this chip during FY76.

Industrial CMOS 8 Bit Slice Digital I/O

We have had preliminary discussions with the IPG group about developing a CMOS 8 bit slice digital I/O chip, to be used in industrial I/O equipment. CMOS is being specified because of its low power and high noise immunity. The design of the chip would be similar in concept to the one which we are proposing for the 11Q05.

LA36/LA180 Chip Set

We have started discussions with the printer group regarding the development of a set of chips to perform all of the control functions and some linear drive functions on the LA36 and LA180. If activity proceeds according to plan, a large portion of the development will occur in FY75. During FY76 we will will be coordinating with the vendors and we will handle the testing of prototype chips and setting up of an incoming inspection program.

Unknown Chips (contingency)

Some funding should be set aside in FY76 to cover the development of chips that are not yet being considered and are not being budgeted by other engineering groups. I feel that the contingency should be in the range of 50K to 75K and it should be used mainly for outside vendor expenses.

RESPONSIBILITY BY PROJECT

RONY ELIA-SHAOUL:

Unibus	20	
Unicorn	65	
SDLC	40	
Multi-drop	50	
LSI Support:		
- Signetics Interchange	80	
- Applications Support	30	
- I^2L Design Study	30	
- Worcester Support	20	
- Technology Planning	50	
- Undefined Chips	90	
		475

JOHN HUGHES:

Q Chips	217	
MSC	195	
		412

BOB KUSIK:

Sage II	135	
- UDDT	18	
Applicon Support	18	
- Logic Schematics	18	
- Interconnect Vertifier	27	
- Runoff + Plot	35	
- Signetics Phone	9	
Circuit Analysis	36	
- Link to Sync.	9	
Fault Simulation/test	120	
		425

1.312

D I G I T A L INTEROFFICE MEMORANDUM

SUBJ: OOD STAFF MINUTES

DATE: 05-06-75
FROM: DICK CLAYTON
EX: 3638
MS: ML5-2/E71

TO: FILE

SUBJ: MINUTES OOD STAFF, MAY 1, 1975

Present: Gordon Bell, Dick Clayton, Phil Laut, Henry Lemaire, Julius Marcus, Bob Puffer

Guests: Mark Abbett, Lorrin Gale, John Cronkite, Bill Demmer

1. Larry presented a Jungle meeting agenda. It was agreeable and the time will be picked to get Ed Shein.

2. Responsibilities of OOD members. While the responsibilities of the OOD members within their own specific groups seems reasonably clear and controlled, it was agreed that we need to work the various intergroup issues. The drawing attached summed it up.

   It was agreed that we must work the intergroup conflicts and joint planning and execution of the areas of real overlap. The Jungle meeting should help. Some areas of overlap are: systems management, writeable control store, small terminal support, small system, networks, communication support, etc.

3. Operations Committee Woods Meeting (Gordon) Products Committee is shut down (OODshould most likely propose a substitute).

   The OC discussed some small systems and the microprocessor strategy.

4. Product Management Process. Larry and Dick distributed memos addressing product management within their organizations. It was agreed that Product Management is real and here. Larry, Bob, and Dick all agreed that the Product Manager speaks for everyone on committments.

5. LSI Engineering (Lorrin Gale) Lorrin Gale described his current staffing and budget plans. The project details are yet to be decided. Generally, the activities support custom low power Schottkey LSI devices using the Signetics process.

SUBJ: DDD STAFF MINUTES

DATE: 05-06-75

FROM: DICK CLAYTON

Also supported is some second source Western Digital work, pushing design engineering to use microprocess technology, and helping others with outside custom projects. Finally, there is a close tie-in with the the Worcester facility.

6. 32 bits A brief overview of the present directions and goals was done by Bill Demmer and Gordon Bell.

RC/mjk

D I G I T A L INTEROFFICE MEMORANDUM

SUBJ: OOD AGENDA

DATE: 05-06-75
FROM: DICK CLAYTON
EX: 3638
MS: ML5-2/E71

TO: FILE

C1454

SUBJ: OOD STAFF MEETING AGENDA--MAY 8, 1975

10:30	Jungle outline, Agenda	Larry Portner
11:00	Depeyrot's White Paper Open discussion	OOD
12:00	Conference participation proposal	Bob Puffer
12:05	MIT Course Report	Bob Puffer
12:15	Tardiness (See attached)	OOD
12:25	Open Agenda Items	
12:30	End	

FUTURE AGENDA ITEMS

Date	Topic	Responsible
5/15	Status of Corporate Packages (written material ahead of time) 30 min.	Puffer/Clayton
5/15	Patent presentation (Len Hughes)	
5/15	Development Strategy for EMI/ESD/RFI Protection of Cabinets (See attached)	Nevala/Nye
5/22	IPG Sudbury Project Report Goals & Interaction with Central Development	Savell/et al
June Jungle:	What is proper level of development expense (vertical integration, more software, fewer products etc.) (double-bill)--Review 32 vs. 36 bit decision and/or process	OOD

SUBJ: DDD AGENDA

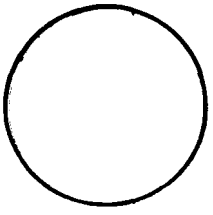
DATE: 05-06-75
FROM: DICK CLAYTON

C1155

Q4	Production Communication	Cudmore/Smith
?	Communication Interface with HW/SW	Marcus et al
?	2X2 Reporting	Puffer
?	Tiny Terminals	?
?	Small LSI-11 System	Clayton/Puffer

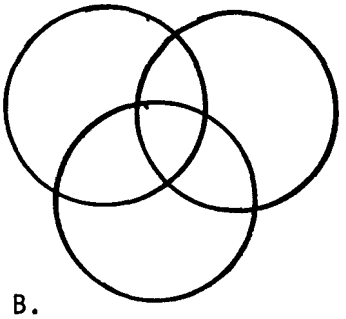
RC:mjk

Attachment--OOD MINUTES, May 1, 1975



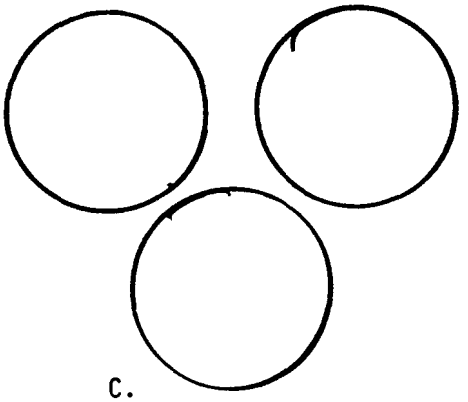
A. Desired integrated goals & plans

One story.



B. Reality of life.

Significant interaction.



C. Some time tendency today.

3 independent operations.

RC
5/6/75

Attachment 2 - OOD AGENDA, May 8

5/15	Mill Space--what is the most effective allocation in terms of group interaction.	OOD
	Larry (Ed Wright) will present a proposal to cover software engineering needs.	ED Wright
	30 min	

digital INTEROFFICE MEMORANDUM

TO: Distribution

For Staff Mtg

DATE: April 29, 1975

APR 30 1975

FROM: Dave Nevala/Larry Nye

DEPT: Mechanical Engineering

EXT: 2244/ 6744 LOC: ML1/E29

SUBJ: DEVELOPMENT STRATEGY FOR EMI/ESD/RFI PROTECTION OF CABINETS

In view of recent customer problems and European standards on EMI, we would like to make the following proposals relative to how we design future peripherals and the new standard cabinet.

1. All undesirable energies/fields shall be transparent to the system, to the extent their presence will, at worst, be seen only as "soft" errors.

2. With the view that operator accessed peripherals cannot be covered with iron, all peripherals should filter out any disturbances which could get into the processor, memories, etc., and cause system failures.

3. All processors, logic, etc., will have the capability of being shielded by external skins or internal bulkheads separating them from the peripherals.

4. All cables not enclosed in the shielded portion of the cabinet shall have the capability of being filtered or shielded to meet proposed EMI/ESD/RFI standards.

We would appreciate any comments or questions on the above proposals. I.e., should the RK06 design try to achieve this goal?

Distribution

Bob Puffer
Dick Clayton
Gordon Bell
Phil Tays
Don Vonada
Peter Boers

COMPANY CONFIDENTIAL

digital

INTEROFFICE MEMORANDUM

OOD/Mark Abbett
LOC/MAIL STOP

TO. OPERATIONS COMMITTEE

DATE. 17 April 1975
FROM. John Fisher
DEPT. Administration
EXT. 4515
LOC/MAIL STOP. ML12-1/A50

Urgent

SUBJ. Tardiness. For Staff Mtg!

Attached is a one week survey of possible late arrivals and early departures at Parker Street and in the Mill. When almost 50% of the Parker Street workforce comes in after 8:15a.m., we may have a problem which requires your attention. Ken has asked that we discuss the subject at the next OC meeting.

Please meet with [illegible]

Ken's edict: How are we going to measure it?

1. No grousing until tardiness is under control!
2. We have to show that efficiency is the reason to get more people. How?

Average Daily Arrivals/Departures W/E 4/4/75

	8:15/8:30	8:30/8:45	8:45/9:00	TOTAL	4:15/4:30	4:30/4:45	4:45/4:55	TOTAL
PK#3								
Population 1,629								
People	379	213	114	706	69	104	147	320
% of total	23%	13%	7%	43%	4%	6%	9%	19%
MILL								
Population 2,790								
People	335	152	89	576	39	105	88	232
% of total	12%	5%	3%	20%	2%	4%	3%	9%

0941

digital INTEROFFICE MEMORANDUM

TO: Distribution

For Staff Mtg

DATE: April 29, 1975

APR 30 1975

FROM: Dave Nevala/Larry Nye

DEPT: Mechanical Engineering

EXT: 2244/ 6744 LOC: ML1/E29

SUBJ: DEVELOPMENT STRATEGY FOR EMI/ESD/RFI PROTECTION OF CABINETS

In view of recent customer problems and European standards on EMI, we would like to make the following proposals relative to how we design future peripherals and the new standard cabinet.

1. All undesirable energies/fields shall be transparent to the system, to the extent their presence will, at worst, be seen only as "soft" errors.

2. With the view that operator accessed peripherals cannot be covered with iron, all peripherals should filter out any disturbances which could get into the processor, memories, etc., and cause system failures.

3. All processors, logic, etc., will have the capability of being shielded by external skins or internal bulkheads separating them from the peripherals.

4. All cables not enclosed in the shielded portion of the cabinet shall have the capability of being filtered or shielded to meet proposed EMI/ESD/RFI standards.

We would appreciate any comments or questions on the above proposals. I.e., should the RK06 design try to achieve this goal?

Distribution

Bob Puffer
Dick Clayton
Gordon Bell
Phil Tays
Don Vonada
Peter Boers

C1462

COMPANY CONFIDENTIAL

digital

INTEROFFICE MEMORANDUM

TO. OPERATIONS COMMITTEE

OOD/Mark Abbett
LOC/MAIL STOP

DATE. 17 April 1975
FROM. John Fisher
DEPT. Administration
EXT. 4515
LOC/MAIL STOP. ML12-1/A50

SUBJ. Tardiness.

Urgent

For Staff Mtg !!

Attached is a one week survey of possible late arrivals and early departures at Parker Street and in the Mill. When almost 50% of the Parker Street workforce comes in after 8:15a.m., we may have a problem which requires your attention. Ken has asked that we discuss the subject at the next OC meeting.

Please meet with your mgrs. re this

Ken's edict: How are we going to measure this?

1. No growth until tardiness is under control!
2. We have to show that efficiency is increased to get more people How?

Mary Jane Keeney 12/1 A-51

cc: Gordon Bell 12/1 A-51
Dick Clayton 5/2 E-7
Bruce Delagi 5/5 E-71

May 2, 1975
Tom Siekman
Legal
4422
PK3/F17

Patent award for Len Hughes

A patent award plaque for Len Hughes which we discussed is attached. Dick has suggested that the plaque be given to Len at one of Gordon's staff meetings.

A copy of Len's patent has been placed in the box along with the award plaque.

The patent covers the 11/45 floating point operation. I do not think that I need to be there for the presentation, but if anyone would like me to go, I will be glad to.

If anyone has any questions, please let me know.

TCS:cmg

digital INTEROFFICE MEMORANDUM

TO: OOD

CC: Mark Abbett

DATE: May 13, 1975

FROM: Dick Clayton

DEPT: OOD

EXT: 3638 LOC: ML5-2

SUBJ: MINUTES OF OOD STAFF MEETING--5/8/75

Present: G. Bell, R. Clayton, H. Lemaire, J. Marcus, R. Puffer
Guests: M. Abbett, J. Cudmore, M. Depeyrot, D. O'Connor

1. Jungle Meeting

Based on Ed Shein's availability, the date is June 12/13 (Larry Portner to work out with Ed). The material as generally outlined in Larry's April 28 memo will prevail. On May 29, we will refine the topic list in light of then current environment.

2. Manufacturing/Development Interfaces

We had a rather wide ranging discussion about a number of topics raised in Depeyrot's "white paper". Jim indicated the first priority from the Manufacturing viewpoint was effective and timely feedback between the various boxes (plants or functions) in the manufacturing process.

It was agreed that Jim Cudmore and Dick Clayton would set up a one day review of Manufacturing and Product strategy between OOD and the senior Mfg. staff for identification of some 10 or so goals for improvement. These would be specific finite goals that would be high payoff and leadership in nature. The goals would be based on the best expectations of products and their interrelationships with the manufacturing plant strategies.

3. Conference Approval Procedures

Bob's proposal was accepted and it is believed John Fisher will be contacted by Bob for the purpose of another 'green sheet".

4. MIT course--deferred to 5/15.

5. Tardiness

It was generally believed most of the mill people are working more than 40 hours/week. It is also obvious that 8:15 has become a bit sloppy. We all are going to work the time issue through our managers, but there are no company wide formal actions at this time.

RC:mjk

digital INTEROFFICE MEMORANDUM

TO: OOD

CC: Mark Abbett

DATE: May 13, 1975

FROM: Dick Clayton

DEPT: OOD

EXT: 3638 LOC: ML5-2

SUBJ: OOD STAFF AGENDA--5/15/75

10:30	MIT Course	Bob Puffer
10:40	Packaging Strategy (who does what)	Puffer/Clayton
11:00	Development Strategy for EMI/ESD/RFI	Nevala/Nye
11:30	Marketing Committee Interactions	Portner/Clayton
11:45	Budget Status	Phil Laut
12:00	Future Staff Agenda Topics	OOD
12:20	Len Hughes Patent	OOD
12:30	End	

- -

Future Agenda

Date	Topic		Responsible
5/22	IPG Switching Project Report Goals and Interaction with Central Development	45 min.	Savell et al
5/22	Small Computer Systems, How will it come together	20 min.	Clayton/Puffer
5/22	32 bit update (general)	20 min	Bell/Demmer
5/22	32 bit software update	20 min	Portner/Wade

Future Jungle--what is proper level of development expense (vertical integration, more software, fewer products, etc.) [July?]

RC:mjk

D I G I T A L INTEROFFICE MEMORANDUM

PAGE 1

SUBJ: OOD STAFF AGENDA 5/29/75 & MINUTES DATE: 05-27-75
FROM: DICK CLAYTON
EX: 3638
MS: ML5-2

TO: OOD XXX

10:30 Corporate Package Proposal — Larry Nye

11:00 IPG Sudbury Project & Multidrop goals and interaction with Central Development — Savell/Bastiani/

11:45 SDLC chip — Marcus/Lemaire Bastiani

12:00 Engineering Plan for Word Processing — Gilmore/Kalin

FUTURE TOPICS

Date	Item	Responsible
6/19	VT51 Software	Portner/Puffer
6/19	LSI-11 Product Plan	Teicher
6/19	Report on meeting with Mfg. Mgt.	Clayton
6/19	OOD Mgt. Employees Development Program(s)	Abbett
6/19	Computer Resource Consolidation	Rutledge
6/19	Yellow Book Revision	Laut
6/19	Secretarial Utilization by Managers	Abbett
6/19	WPI Master Degree Program	Bob Hall/Abbett

Future Jungle--What are proper levels of development expense in light of vertical integration, more software, fewer products, etc.

7/? MSC Proposal — Hughes/Lemaire

SUBJ: OOD STAFF AGENDA 5/29/75 & MINUTES DATE: 05-27-75
FROM: DICK CLAYTON

MINUTES OOD STAFF MEETING 5/22/75

Present: Bell, Clayton, Laut, Portner, Puffer
Guests: Abbett, Gale

1. Hiring up to 5 people for LSI design. Subject to agreement between Lorrin & Phil that the money really is in the budget, the five were approved.

2. Dick Clayton talked about the Small Packaged Systems Proposal. John Clark is expected to pull this together. It is expected a prototype will be selected and funded by a federation of product lines and the engineering group. A PSG will probably be formed. Bob and Dick agreed that some of the focus for Nicoud-type terminals will drift toward this project management, although Tom Stockebrand will reclaim people management. This is a soft area for all to work out over the coming months.

3. 32 bits--specifications for hardware architecture is still to be done 6-2. A decision is expected to exist during mid to late June. The software plan will be the next big step. A plan for conversion of some of the current software will exist about 6-2, but it will be some time later for the "new" operating system.

4. There will be a two hour presentation of product P&L type data during the Thursday, June 5 Woods meeting. Phil will do a 20-30 minute overview; and we will present LA30/36, one disk, RSX11-D, 11/05, and 11/45 + 11/70.

MAY 14 1975

digital INTEROFFICE MEMORANDUM

1468

TO: OOD
Julius Marcus
CC: Frank Zereski
Dan Hamel

DATE: May 12,1975

FROM: Vince Bastiani VB

DEPT: DECcomm Engineering

EXT: 3292 LOC: ML5/E43

SUBJ: SDLC CHIP

We have reached a tentative agreement with two vendors to have the SDLC Chip produced as a standard product. This approach was taken since it is felt that the long term advantage of lower chip cost would be realized if an industry standard part could be obtained. The basics of the agreement are outlined below and are identical for each vendor (with the exception of price).

1. Firm commitment to purchase 2500 pieces after acceptance of prototype with term of 12 months with option to extend to 18 months. Price is twenty-eight dollars with SMC and $24.50 with Signetics.

2. Firm release for 500 pieces must be issued after acceptance of prototypes.

3. Each vendor cannot announce details of part (Pinout and timing) until two months after delivery of 300 pieces to DEC or two months have elapsed whichever is greater. This gives us some competitive edge.

NOTE: Signetic wishes to have restrictions removed for all when one vendor has satisfied three above. This is the only issue left hanging and must be resolved with SMC.

4. DEC is free to issue Spec. to others at any time, and DEC has ultimate design jurisdiction.

5. An Escrow account will be established in case of SMC to insure that in event SMC goes bankrupt we will have access to all work done on Chip.

6. If vendor does not deliver acceptable part after two iteration of the prototype DEC has right to cancel.

Each agreement is funded with a firm purchase order (no front end money). DEC will be responsible for coordinating Spec. Non declosure agreement will be signed to try and protect whatever design information we give them.

These two agreements should be finalized within two to three weeks (Dan Hamel of Purchasing) is working out the details. Dan did a very good job at both negotiation sessions providing us with, I feel, a very good agreement.

Our commitment now is to have Frank produce a very detailed Spec. by June first to get each vendor started.

D I G I T A L INTEROFFICE MEMORANDUM

PAGE 1

SUBJ: OOD STAFF AGENDA 5/22/75 & MINUTES
DATE: 05-21-75
FROM: DICK CLAYTON
EX: 3638
MS: ML5-2

TO: FILE

10:30	Small systems, how will it come together.	Clayton/Puffer
10:45	Hiring people for LSI-11 Second source project.	Gale
11:00	32 bit update (10 min each)	
	Architecture	Bell
	Software	Portner
	Hardware	Clayton
11:30	SDLC chip	Marcus/Lemaire
12:00	June Woods--2 hour product presentation	Bell/Laut/et al

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FUTURE TOPICS

Date	Item	Responsible
5/29	IPG Sudbury Project Goals and Interaction with Central Development	Savell/Bastiani
6/4	VT51 Software	Portner/Puffer
6/11	LSI-11 Product Plan	Teicher
6/19	Report on meeting with Mfs. Mgt.	Clayton
?	OOD Mgt. Development Program(s)	Abbett
?	Computer Resource Consolidation	Rutledge

Future Jungle--What are proper levels of development expense in light of vertical integration, more software, fewer products, etc.

7/?	MSC Proposal	Hughes/Lemaire

SUBJ: ODD STAFF AGENDA 5/22/75 & MINUTES DATE: 05-21-75
FROM: DICK CLAYTON

MINUTES: ODD STAFF MEETING OF 5/15/75

1. MIT COURSE

Bob reported the course now contains significant new material applicable to industry. Bob and Dick will identify one candidate each. After they take the course we will review its potential as a special given for a few days to a broader group of DEC managers.

2. PACKAGING RESPONSIBILITIES

Bob outlined the role of the groups now under Phil Tays. Bob said these include responsibility for corporate wide connectors, packages, process related issues, and industrial design. These are done both as corporate standards or guidelines as well as specific contracted services for individual projects (especially by groups too small to have dedicated packaging talent). Generally it seems that about half the full time DEC people working on packaging related issues are collected in Phil Tay's central group. This seems a good balance.

3. EMI-RFI

Dave and Peter outlined system design and packaging considerations that must be made if our systems are to be insensitive to static discharge and relatively emission free (such as meeting German VDE requirements).

Dick Clayton agreed to form a group with the responsibility of stating our system design goals with respect to EMI-RFI across our products for the next few years.

4. MARKETING COMMITTEE INTERACTION

Larry & Dick discussed an ongoing conversation with the Marketing Committee focused on the role of systems managers, what they should do, who they might be.

5. BUDGET STATUS

Phil reported that the present estimates show about $175K moving from Q3 FY75 to Q4 FY75. The half remains the same.

Q1 FY76 still looks high by about $300K. Henry expected

SUBJ: OOD STAFF AGENDA 5/22/75 & MINUTES DATE: 05-21-75
FROM: DICK CLAYTON

he could pick up $50K-$75K in the memory area. We are going to seriously attempt to collectively get the rest of the money.

6. PATENT TO LEN HUGHES

Len was formally presented a patent for work on the 11/45 floating point unit.

RC:mjk

digital

May 21, 1975

Dr. Angel Jordan
Computer Science Department
Carnegie-Mellon University
Schenley Park
Pittsburgh, Pennsylvania 15213

Dear Angel:

I am authorizing a four (4) month extension to DEC support of Mike Doreau's work at Carnegie-Mellon.

Payments will be $375.00 per month as before.

Sincerely,

Gordon Bell
Vice President, Office of Development
Professor, Computer Science
Carnegie-Mellon University (on leave)

GB:mjk

Attachments: Payment schedule 6/3/74
Payment schedule 5/20/75

cc: Phil Laut--for payment
Luther Abel
Mike Doreau

DIGITAL EQUIPMENT CORPORATION, 146 MAIN STREET, MAYNARD, MASSACHUSETTS 01754
(617)897-5111 TWX: 710-347-0212 TELEX: 94-8457

FM PHIL LAUT
TO LLOYD TUCKER
CC GORDON Bell

1473

JUL 01 1974

June 3, 1974

Dr. Angel Jordan
Computer Science Department
Carnegie-Mellon University
Schenley Park
Pittsburgh, Pennsylvania 15213

Dear Angel:

In accordance with your letter of May 23, 1974, I am authorizing payment for Mike Doreau's support at DEC to work on his PhD. for the period March 1, 1974, to June 1, 1975. The amount includes:

Monthly support at $375 for 15 months	$5625
Registration at CMU during 1974-75 at 1/4 time	725
Total	$6350

The check will be sent to you as soon as possible and Mike should begin to receive this support.

There has been tentative agreement of a committee of myself, Professors Grason and Siewiorek, that Mike has a possible and acceptable thesis topic.

Sincerely,

Gordon Bell

Gordon Bell mjk
Vice President, Engineering
Professor, Computer Science
Carnegie-Mellon University

98-DS057
CC 371

GB:mjk

cc: Phil Laut--for payment
Luther Abel
Mike Doreau

C1474

PAYMENT SCHEDULE

Payment for months of:	Payment date	Amount
March, April, May, June, 1974	7/25/74	$1500
July, 1974	8/25/74	375
August, 1974 + CMU Registration 1/4 time at $725	9/25/74	1100
September, 1974	10/25/74	375
October, 1974	11/25/74	375
November, 1974	12/25/74	375
December, 1974	1/25/75	375
January, 1975	2/25/75	375
February, 1975	3/25/75	375
March, 1975	4/25/75	375
April, 1975	5/25/75	375
May, 1975	6/25/75	375
		$6350

PHIL LAUT 6/3/74

PAYMENT SCHEDULE

Payment for months of:	Payment date	Amount
June, 1975	7/25/75	$375
July, 1975	8/25/75	375
August, 1975	9/25/75	375
September, 1975	10/25/75	375
		$1500

Phil Laut
5/20/75

DIGITAL EQUIPMENT CORPORATION 1476

VOUCHER

Payable To:

Name: Carnegie-Mellon University

Address: c/o Dr. Angel Jordan, Computer Science Department

Carnegie-Mellon University, Schenley Park, Pittsburgh, Pa. 15213

Amount: $1500.00 Date 5/20/75

Description: Extension of Mike Doreau's Fellowship per Gordon Bell's letter of May 20, 1975.

Badge	Cost Center	Account	Act. O E	1	2	3
80	371	07381	E	98	05057	

Order Rec'd.	Price OK	Payment OK	Check No.

[XX] Mail Check Please follow payment schedule attached.

[ ] Check To Originator

DEC 1-1028

D I G I T A L INTEROFFICE MEMORANDUM C1477

SUBJ: INTERNAL EDITORS
DATE: 05-28-75
FROM: GORDON BELL
EX: 2236
MS: ML12-1/A51

TO: FILE

SUBJ: STANDARDIZATION OF INTERNAL EDITORS FOR THE PREPARATION OF MEMOS, MANUALS, etc.

To: Distribution

Finally, we are beginning to use our machines internally extensively for the preparation of memos, technical specifications, manuals, etc. and distribution of TWX and mail. I've heard that we have to retype documents in machine readable files because of poor inter-editor standards. There are a number of standards that might help us:

1. Programs that have the same name (e.g. TECO, RUNOFF) should behave the same on all systems.

2. Text files might be interchangeable so that text can be prepared on nearly any terminal and editor and then post processed (e.g. hyphenated and justified), and typeset by other processors. This take more standardization so that the typesetters use it.

3. There are several typesetting machines and these have different input.

4. The terminals (e.g. Diablo, VT52, LA36) all have idiosyncrasies.

5. New terminals such as the VT20 and VT51 provide substantially more processing of the files at the terminals. By making poor decisions, we can actually increase the load on CPU's by using these terminals...instead of decreasing it as intended.

6. There are extensive programs of different classes for all different systems, and these simply have to be enumerated so that people can fully use them. (I DON'T WANT MUCH MORE SOFTWARE WRITTEN TO USE INTERNALLY!) We seem to have more programs than people can use.

   A. Text editors
   B. Hyphenation, justification, pagination, etc.
   C. Memo and microfilm filing control.

SUBJ: INTERNAL EDITORS DATE: 05-28-75
FROM: GORDON BELL

D. Memo distribution and mailing.
E. Typeset machine control.
F. etc.

7. We are going into the business of developing even more programs for "word processing" for the unknowledgeable user. (For now, I prefer to educate our internal users...the increased capability looks worth the effort.) Mary Jane has brought together 20 secretaries in a training course, and there's a waiting list for another.

8. There is actually some knowledge about human engineering of these things, and there doesn't seem to be much sharing of this knowledge.

Since there are no external standards, as in the case of languages (e.g. COBOL, even BASIC, and FORTRAN), we might have an internal activity to get the standards we need in the above area.

How and shall we attack this? Is there anyone responsible for these utilities or do they just grow forever? For now, I'd be somewhat happy with a catalog.

GB:mjk (e.g. the tab key generated an extra line, as you can see, when queued to the line printer; however, it tabs normally without the line feed when typed on an LA36.)

now fixed

Distribution

Pete Conklin	Jim Milton
Ken Fine	Stan Olsen
George Friend	George Plowman
Bob Gafford	Larry Portner
Jack Gilmore	Ron Rutledge
M.J. Keeney	Pete Van Boekens
Roy Lightfoot	Ed Vrablick
Bob Maguire	Pat White
Arnie Goldfein	Bob Klein
Bill Kiesewetter	Bob Lane

cc: OOD

D I G I T A L INTEROFFICE MEMORANDUM

SUBJ: RUMOR OF THE MONTH

DATE: 05-19-75
FROM: GORDON BELL
EX: 2236
MS: ML12/A51

* *
TO: FILE
* *

SUBJ: INCOMPATIBILITY RUMOR OF THE MONTH?

To: Dist.

Say it isn't so.

Say that the binary files that RT FORTRAN and FORTPAN IV+ produce running under the same operating system (e.g. RSX-11/D) are not different?

GB:mjk

Distribution

Bob Bean
Ron Brender
George Plowman
Pete Van Roekens

cc: Larry Portner

digital INTEROFFICE MEMORANDUM

TO: Operations Committee

DATE: June 26, 1975

FROM: Gordon Bell GB

DEPT: Engineering

EXT: 4308 LOC: ML12/A16

SUBJ: Request for Approval for Outside Hires

I would like approval to start looking for the following outside hires now.

1. Five (5) LSI Design Engineers in Lorrin Gale's LSI Engineering Group. (All are additions.)

2. Two Applications Programmers to work on EPLS in the EDP group in my area. (One addition and one replacement.)

3. One Applications Programmer to work in the Software Distribution Center. (Addition.)

All of these hires fit within our FY76 budget.

The engineers in the LSI group are required for continuation of semiconductor efforts in Maynard and Worcester.

The programmers to work on EPLS are needed to complete the consolidation of our information concerning products in a single, easily maintainable data base.

The programmer in the Software Distribution Center is required to continue the improvement in productivity that has been achieved this year.

/ale
att

digital

INTEROFFICE MEMORANDUM

TO: Arnie Goldfein LOC/MAIL STOP

DATE: 24 June 75
FROM: Oleh Kostetsky
DEPT: SDC
EXT: 3704
LOC/MAIL STOP: ML11/E52

SUBJ: Justification for Additional EDP Personnel for SDC

See attached 5 Year Spending Plan for the SDC. Our Plans include a reduction in Non-Material Cost per Unit of production from .998 in FY'75 to .881 in FY'80.

(This metric is derived from dividing expected non-material costs by our productivity measure. The productivity measure is derived by multiplying expected production of a type of activity (e.g. MAGtape copying) by our current non-material standard cost for doing same.)

This represents a 12% cost savings in the face of an expected 7 1/2% inflation rate.

In order to achieve this result we must invest heavily in automation.

With everything done by hand until FY'75 and with explosive growth, the SDC is fertile ground for EDP automation.

/sf
attachment

SDC 5 YEAR SPENDING PLAN

	ACTUAL					PLANNED				
	FY'71	FY'72	FY'73	FY'74	FY'75	FY'76	FY'77	FY'78	FY'79	FY'80
Coporate N.O.R. (Millions)	146.8	187.6	265.5	422.3	505.0	675.0	1028.0	1367.0	1700.0	2000.0
SDC ($1000):										
Materials ($1000)	159.4	223.7	316.1	526.8	1139.0	1679.0	2946.0	4082.0	5100.0	6000.0
Labor, OT, Fringe ($1000)	189.4	233.6	382.1	653.0	973.6	1373.1	2008.6	2642.8	3287.1	4027.4
Other:										
Space	31.2	37.5	59.7	88.4	236.7	326.0	484.0	684.0	902.0	1124.8
Travel	0.2	0.4	0.2	4.8	11.3	22.0	32.0	44.0	60.0	80.0
Equipment	31.2	22.9	20.8	28.0	36.8	76.0	144.0	255.2	336.8	419.6
Telephone	3.4	7.5	12.1	22.9	34.5	55.4	88.8	122.4	161.6	201.6
Freight	*	*	3.4	2.4	9.2	15.2	24.2	34.0	44.7	56.2
Field Service	*	*	*	41.2	35.7	62.8	119.0	210.8	278.3	346.5
Computer	*	*	*	0.4	18.3	46.9	114.3	204.0	269.2	335.6
EDP	*	*	*	*	43.9	140.0	160.0	186.8	213.2	240.4
Shipping	*	*	*	*	41.2	0.0	0.0	0.0	0.0	0.0
Consultants	0.0	0.0	0.0	0.0	19.9	4.0	8.0	8.0	8.0	8.0
S.E. Tax	*	*	*	*	116.6	160.5	240.4	327.4	405.5	480.0
Copying Program Development	*	*	*	*	26.1	40.0	40.0	40.0	40.0	40.0
Miscellaneous	0.5	1.3	3.1	2.8	6.3	9.6	15.4	21.6	28.4	35.2
Total Other ($1000)	66.5	69.5	99.2	191.1	636.6	958.4	1470.1	2138.2	2747.7	3367.9
Total Non-Material Expenses ($1000)	255.7	303.1	481.3	844.1	1610.2	2331.5	3478.7	4781.0	6034.8	7395.3
Total SDC Expenses ($1000)	415.1	526.8	797.4	1370.9	2749.2	4010.5	6424.7	8863.0	11134.8	13395.3
Manual Print Costs ($1000)	N/A	N/A	N/A	N/A	1872.7	2685.0	4679.1	6284.6	7510.7	8378.5
Total SDC Responsibility ($1000)	-	-	-	-	4621.9	6695.5	11103.8	15147.6	18645.5	21773.8
Ave # of People		37	59	84	106	141	191	232	266	302
Workload (100 Units)	374.0	519.7	771.3	1064.7	1612.8	2314.0	3630.2	5104.4	6733.4	8393.4
Non-Material Cost Per Unit of Production					.998	1.008	.958	.937	.896	.881
WORKLOAD ÷ People	—	14.1	13.1	12.7	15.2	16.4	19.0	22.0	25.3	27.8

*=Not charged to SDC in this period

C1506

digital

INTEROFFICE MEMORANDUM

		LOC/MAIL STOP
TO:	Lloyd Tucker	PK3-2
	Cindy Donovan	PK3-2
	Andy Dufresne	ML5/P66
	Mimi Cummings	ML5/A20
CC:	Phil Laut	ML12/A16

DATE: June 23, 1975
FROM: Gordon Bell
DEPT: Engineering
EXT: 4308
LOC/MAIL STOP: ML12/A51

JUN 26 1975

SUBJ: Signature Authorization

Phil Laut is authorized to sign purchase requisitions in amounts not to exceed $500.00 for cost center #322.

/ale

digital

INTEROFFICE MEMORANDUM

TO: Bob Passerello

LOC/MAIL STOP

CC: Pat McCormick
Harold Trenouth

DATE: 27 June 1975
FROM: Gordon Bell
DEPT: Office of Development
EXT: 2236
LOC/MAIL STOP: ML 12-1

SUBJ: PEOPLE DENSITIES

Could you do some quick (rough) calculations on People densities in the new areas - Spector, Clarke, Gale, Software Diagnostics - Johnston, 12-1, Purchasing, Software Distribution Center versus various 5-5 Engineering groups, Hardware/Software, Delagi (3-5), Peripherals (1-3), Production (1-4)? Have we lost density? Is it in just some groups?

GB
mam

D I G I T A L INTEROFFICE MEMORANDUM

PAGE 1

SUBJ: HARDWARE/SOFTWARE EVALUATION
DATE: 06-27-75
FROM: GORDON BELL
EX: 2236
MS: ML12-1/A51

TO: FILE

SUBJ: METHODOLOGY OF EVALUATING HARDWARE-MICROPROGRAM-PROGRAM (SOFTWARE) TRADEOFFS IN VAX ARCHITECTURE--DRAFT

To: VAXA

We are facing an increasing number of tradeoffs of the above type, and we should state a clear policy (if we can). This document is a start at this. Some relevant goals and implications:

G3 = compatibility across a range.

I4.3 All machines will implement all op codes by some technique.

*I4.3.1 Op codes which are unimplemented in some machines require a clean, consistent method to permit software execution of the op code.

*I4.3.2 For various market places, we may emphasize different operations (e.g. no floating point, decimal, decimal floating versus binary floating), hence, there may be a rather dynamic implementation of op codes within a single model.

*I4.3.3 Due to cost-effective goal, there may be opcodes which are not cost-effective for microcode under any conditions, but appear in ISP. These codes will be infrequently executed, costly in microcode to implement, but will nevertheless still be worthwhile in the ISP even though they are only occasionally executed (e.g. Quad Divide, sin). Therefore, we must assume that even in high end implementations, some op codes are best implemented in software!

Speed and Cost Basis

The basic cost and speed (time) ground rules:

1. Generally ROM (microcode) costs versus RAM (software

code) costs will be highly variable as a function of the implementation.

2. The speed ratio of ROM to RAM is highly variable for various implementations.

3. There is also the possibility of executing microcode which resides in main memory.

For example, for LSI-11:

A. We assume 2 LSI-11 micros = 1-11 instructions. Since they are about the same length, then twice as many bits are required for a micro.

B. 10K bits cost $25, or .25 cents/bit and RAM currently costs about $8 for 4K. Thus the two have identical costs, but a given program costs 2X as much in microcode.

C. A micro instruction is executed in about 1 1/2 cycles or .5 micro sec., whereas a PDP-11 instruction on LSI-11 takes 5-7 microsec. But it takes twice as many micro instructions to be equivalent to a PDP-11 instruction. Therefore, a 2 microinstructions take 1 microsecond. Thus, a microprogram executes 5-7X faster in microcode.

In our implementations, let's assume for now (but I would like some hard #'s fedback to me from O'Loughlin, Kaman, Rothman, Armstrong, Dickhut):

1. A factor of 5-10 in speed for microcode in micro memory.

2. ROM cost=RAM cost, but 2-4 times the number of bits are required; hence, 2-4 times the cost for microcode versus macrocode.

3. A factor of 2 slow down for microcode stored in main memory; and a factor of 2-4 increase in cost over macrocode. Hence, there is no incentive for most implementations to do this.

How Do We Use This?

For cost reasons, we should move all of the ISP machine definition to 11 code instead of microcode. This clearly argues for a clean interface to tradeoff between the two. Note, as we are implementing 2 ISP's, the arguments are especially strong to do this.

There are three kinds of program versus microprogram substitutions that occur:

0. Tradeoff to win phony benchmarks--no significant use.

1. Tradeoff to get speed. This tells whether something should be in microcode versus macrocode. It also indicates whether something should be an op code to reduce I-stream over a subroutine. A typical example is placing floating point instructions in microcode.

2. Tradeoff to get space in the object program, permits deciding whether an op code should be in ISP or not (i.e. just treated as a closed subroutine, or a sequence of instructions-open subroutine). An example is a call, return instruction.

3. In doing the analysis, we must assume that a bit in micro memory can be traded for a bit in macromemory.

Microcode versus Macrocode Tradeoff

This analysis is carried out by looking at the instruction execution frequency, and determining whether the incremental gain in performance is worth the increase in cost.

Assume:

1. dp = gain in performance by moving from macro to microcode. The max is a factor of 5-10, but has to be multiplied by frequency of use in actual use.

2. dc = price increase due to microcode. normally only a few dollars.

3. Let's assume all new features are to behave at least as well as Grosch's law, ie:

$$p = k \times C^2$$

and

$$k = p/C^2$$

therefore a gain in performance has to follow

$$dp/dc \geq 2 \times k \times C$$

substituting k,

$$dp/dc \geq (2Xp)/C$$

and rearranging

$$dp/p \geq 2X(dc/C)$$

Or simply, the relative gain in performance has to exceed the relative gain in cost by at least a factor of 2.

Now test for floating point, assuming a C=$5,000; dc=$10, dp=2, and p=1 (i.e. performance just doubles with microcode due to execution frequencies applying:

2/1>> 2X10/5000

or

2>>.004

Let's apply the test to a complex instruction: assume it is executed each 500 milliseconds, and each time it is executed 1 millisecond is saved. Also assume dc=$10 and C=$5,000. Note, that

dp/p = .002
2Xdc/c = .004

therefore .002>.004, and by this criteria, the instruction is marginally worthwhile.

Now compare this with a software implementation that is a factor of 5 slower, and 2 cheaper:

dp/p = .0004
2Xdc/c = .002

thus since dp/p is less than 2Xdc/c, the feature should be placed in microcode, and not in software.

(Space Tradeoff) Extra Instructions in ISP to Reduce the I-Stream

By trading off microcode or macrocode we can add instructions to the ISP. We must, however, truly save the instructions.

Generally, the arguments are to add instructions, as long as we can safely identify the use of an instruction.

For example, let's assume a complex address mode costs 40 micro word bytes or 20 macroword bytes to implement. Assume that each subroutine saves 1 byte by using the instruction. Therefore, all we need is to guarantee a memory with 20 to 40 subroutines. Whether the instruction is in micro or macro code is purely a function of the number of calls.

GB:mik [EVALSF]

C1512

digital

INTEROFFICE MEMORANDUM

TO: John Kulik

LOC/MAIL STOP

DATE: June 27, 1975
FROM: Gordon Bell
DEPT: 00D
EXT: 2236
LOC/MAIL STOP: ML12/A51

SPDL

SUBJ: MIKE DOREAU

Please extend Mike Doreau's visitor badge until December 31, 1975. Mike uses the red entrance at Bldg. 21, if you would please inform the guard.

Thanks

GB:mjk

C1513

digital

INTEROFFICE MEMORANDUM

LOC/MAIL STOP

TO: Ron Rutledge
Herb McCauley

CC: Jack Shields
Al Bertocci
Larry Portner
John Leng

SUBJ:

DATE: 30 June 1975
FROM: Gordon Bell
DEPT: Office of Development
EXT: 2236
LOC/MAIL STOP: ML12-1/A51

RELIABILITY OF CS/2 AFTER MOVE

I've watched several of my co-workers trying to use CS/2 these last few months since the move. It is clear to me that the system is in significant trouble from a reliability standpoint. I've just measured several days of 15 min MTBF time, but don't have any real data.

You guys obviously need field service and/or IO Engineering help and must be too bashful to ask for it. I want to formally ask for this help. This is costing us a lot in productivity. What can be done?

GB:mam

digital

INTEROFFICE MEMORANDUM

LOC/MAIL STOP

TO: Tom Siekman
Ed Schwartz
CC: Ken Olsen
Phil Laut
Mark Abbett
Harold Trenouth

DATE: 30 June 1975
FROM: Gordon Bell
DEPT: Office of Development
EXT: 2236
LOC/MAIL STOP: ML12-1/A51

SUBJ: THE IDEA OF DESIGNING AND PUTTING EXTERNAL SWITCHES ON PIN-TYPE FLOURESCENT BULBS WITH NO INSTALLATION

I've talked with several of you over the last two weeks regarding the above idea. As an idea it is somewhat like Ken's wallpaper remover story.*

I have an idea for an invention, several possible implementations, and believe this has great product potential. In this case, the idea is the invention, since the implementations are straightforward.

It is, of course, totally useless as a DEC product, and I'm only mildly interested in pursuing it as a designer. I do intend to see that it comes to fruition as a product. Before I proceed, I would like:

1. A decision as to whether the patent belongs to DEC.

2. If it belongs to me, then I'll proceed in its development, probably by getting a competent engineer to bread-board it.

3. If it belongs to DEC, then I'll use our facilities, engineering consulting, and proceed to get it designed, patented, and get it an agent to sell to a manufacturer.

Please give me a formal statement on this, since I'd like to proceed very rapidly. We need about 5000 of them right now for the mill.

* The inventor, talking to his friend said,"I have this great idea for a wallpaper remover. You simply put it on the wall, and the wallpaper comes off and the wall is cleaned." The friend asked, "What is it?", and the inventor replied, "Don't ask me. That's your problem, since I thought of the idea."

GB:mam

D I G I T A L INTEROFFICE MEMORANDUM

SUBJ: WPST

DATE: Ø6-24-75
FROM: GORDON BELL
EX: 2236
MS: ML12-1/A51

* *
TO: FILE
* *

SUBJ: WPST--WORD PROCESSING, STORAGE AND TRANSMISSION

To: Distribution

The Word Processing product looks like a winner, and I believe it will be successful. As people talk about Office Automation, I look at WPST as being the highest payoff because it eliminates much trivia while providing better functions (e.g. filing). Here is another way to come at various aspects of WP; it is somewhat more unorthodox.

In the long term, this later approach is inevitable, and WP must lead to WPST for every local environment (e.g. DEC) with capabilities to interconnect environments (i.e. electronic mail).

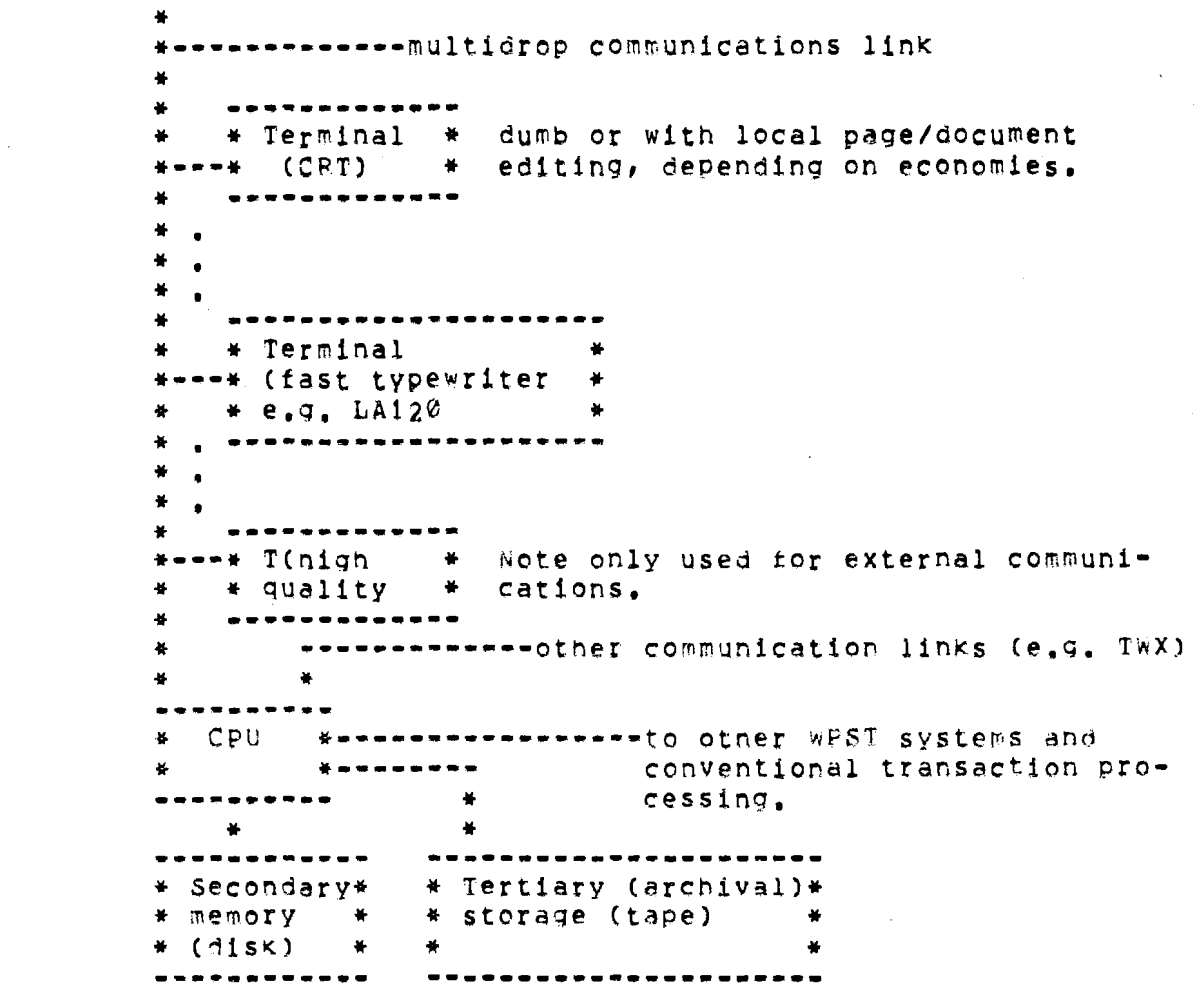
WPST can also be looked at as an extension of our local DECnet message switching to include message (document) editing, and the long term storage and retrieval of documents.

I hope we can puruse this second approach for internal use along the lines suggested by Computer Corporation of America; Friend/Copp; and Alusic/Marcus.

What is WPST?

With WPST, a conventional WP front end is assumed, and the host Word Processor is used to hold all documents including the archives in a central fasnion (though it need not be a single system). Multi WPST's would be interconnected.

Physically it is just:



SUBJ: WPST

DATE: 06-24-75
FROM: GORDON BELL

The system carries out the following functions:

1. Conventional text (document) preparation either via a central, shared program using a dumb terminal or locally on a smarter, buffered terminal (e.g. VT51). The text resides in a file(s) on the system.

2. Since the system also has distribution list files, the documents are inherently ready to send...or can be assumed to be sent.

3. Transmission of the documents can be carried out in several ways:

   A. The document is automatically printed as in DECnet.

   B. The reader is notified of messages. The reader peruses his mail via a CRT and deletes his reference to them, or states he wants the document filed in his own filing system, or prints it. Provided he hasn't deleted the document he can retrieve it again.

4. Subsequently, a reader can retrieve any document he has asked to have in his file system. Note, only 1 copy of the document is stored in this system--unlike any system based on paper, microfilm, etc.

Why is such a System Inevitable?

Basically, this system has to evolve within the next 10 years because all costs (especially technology) are conspiring to force it. It also provides more capability at less money.

1. People costs are growing at 6-10%/year. I.e. people are pricing themselves out of the market.

2. Disk storage costs are decreasing at 41%/year. communications costs for local phones, etc., are relatively constant. Terminal costs are decreasing at 25%/year while taking on more functionality.

3. the cost of paper, and xeroxing is increasing. file cabinets, mail carts, etc. are also increasing. Such a system is printed on a terminal at .01 versus .05 for a page of Xerox paper.

   the key components which it addresses are:

A. correcting the document (a factor of 2-4 cheaper) than with typing.

B. Manually Xeroxing, collating and posting the documents.

C. Transmission (mail)--there aren't people for this.

D. Opening
E. Filing--note this saves filing...and for documents with multiple receivers who file, really big savings result Filing is the really expensive part of sending memos.

F. For users who type, documents can be entered directly without secretarial help.

4. The quality and service is increaibly increased.

A. Documents are transmitted immediately.

B. Documents can really be retrieved, as opposed to our current systems. Ideas can be saved, and need not be re-invented.

C. Documents can be justified, hyphenated, etc. making for better readability. Typing is easier.

5. Telephone traffic can be decreased while significantly increasing communication. Short messages (questions and answers) can be transmitted without the need to synchronize on the phone.

6. A retrieval record of transaction can exist.

Which part of an Organization Will Buy it?

Normally, I would be skeptical of such a system because it has to be sold to the dull, bureaucratic heartland of an organization. However, in this case the payoff is so high, even the slowest manager can understand the payoff. Fortunately, we have no problems in these areas in terms of internal use.

Since it could represent a significant switch in the workforce it might be resisted by a clerical staff. There are 3 places who might have to approve such a system. Probably all 3 have to buy in:

1. Message switching/communications--the George Friend/Murray Copp of an organization.

2. Office Services--the part which buys typewriters, Xerox machines, file cabinets, and provides for duplicating and mail service--Frank Kalwell.

3. EDP--maybe it's treated as a computer.

4. Personnel--certainly affected.

Our Use

Clearly DEC is the ideal environment because:

1. We have a sharp, aggressive administrative function which analyzes, is cost-effective oriented, and can make it work.

2. We have a significant start via:

   A. DECnet for nearly the same function--it can be viewed as an extension. Terminals and organiztion are already in place. The group wants to do it.

   B. EDP which uses terminals interactively.

   C. Mary Jane's course--we have a large number of secretaries who are already using our 10's for this purpose.

   D. Orientation to computers.

3. DEC is growing, if there are major shifts in working, we can accommodate them in growth.

How Many Ways Can WP (i.e. Office Automation) be Solved and Which Way Is Likely to Win?

It is possible that our foray into WP may be unsuccessful. Fortunately it is a sideline, (a piece of ala carte software), but it will be valuable to learning about the market.

It certainly is questionable whether when people find their DS310 being used full time as a WP, they won't look for cheaper solutions. However, for the casual WP use it is a bargain. It also will work on a shared basis by getting the price down.

The competition:

1. Won't there just be stand-alone systems that use the same

components we have minus the desk, computer, etc. by the time we come on the market?

2. Really low cost smart typewriters (even IBM has something that gets one a substantial portion of the way to our system. The real question is whether typewriter manufacturers (e.g. Olivetti) will get it together and join the 20th century. I'm curious as to whether there's a plug on the new Selectric to allow it to be communicated with electrically.

3. Larger, shared systems such as we assume Xerox may be working on.

4. Other manufacturers--particularly Xerox that could build and market the system.

5. The telephone company could provide this via Teletype 40's, and local systems, probably prohibited, however.

6. IBM is moving toward a communications orientation for its computer structures. With this model, terminals and the ability to arbitrarily interconnect them to computers and to interconnect computers become the central focus. Computers are de-emphasized, and merely reside at nodes to carry out various functions (e.g. WP, or WPS, or storage).

7. Inherently, this is so big, obvious and inevitable that everyone (including ATT and the government) will be in trying to build, control and get their share. It is so important that it is not given in the market surveys...a sure sign of success.

SUBJ: WPST

DATE: 06-24-75
FROM: GORDON BELL

OUR CAPBILITIES VERSUS POSSIBLE COMPETITORS

	IBM	XEROX	DEC	OTHER (e.g. Honeywell, Burroughs
Basic hardware	X	X?	X	?
Large Disk	X	no	buyout	?
Comm. Hdw	X	?	X	?
Volume Terminals				
High quality	X	X	buyout	no
CRT	X	?	X	probably
Fast hardcopy	X?	?	X	not yet
Suitable (RSX-M) type monitor	X	?	X	?
Service	X	?	?	X
Sales	X	X	?	X

SUBJ: WPST

DATE: 06-24-75
FROM: GORDON BELL

What I'd like

CCA wants us to work with them in the installation and trial use of such a system. I'd like this to go in as a DECnet follow on, and with help from Ken King to assist in the specs and work on the analysis.

We (DECnet, King and I) ought to start coming at the cost-effectiveness issue. My back of the envelope analysis says that it takes 1 month payoff within DEC in terms of secretarial time, Xeroxing, mailing, filing, etc.; but it needs a traffic study, cost analysis, etc.

A critical issue with this form of WP, is that it be understood in a real, live environment. I believe we have that environment, and could operate such a system a year or two, and gain the understanding before taking it to market.

What you think?

GB:mjk

Distribution

Marketing Committee	Irwin Jacobs
OOD	Ken King
Don Alusic	Herb McCauley
Jim Bell	Ron Rutledge
Al Bertocchi	Tom Stockebrand
Murray Copp	Nat Teichholtz
George Friend	Stu Wecker
Jack Gilmore	

cc: Ken Olsen

June 26, 1975

Professor B. Shackel
Director: NATO ASI on MCI
Department of Human Sciences
University of Technology
Loughborough Leicestershire
England

Dear Professor Shackel:

Thank you for your letter requesting funding of the NATO Advanced Study Institute. We believe this is important, but do not have funds to support it now.

It is possible that DEC UK might have support funds, and I would encourage you to contact them through your local DEC customer sales engineer; but in view of the late date, I would be concerned that they too, are in a financial bind.

Sincerely,

Gordon Bell
Vice President
Office of Development

GB:mjk

cc: Geoff Shingles
Bill McBride

DIGITAL EQUIPMENT CORPORATION, 146 MAIN STREET, MAYNARD, MASSACHUSETTS 01754
(617)897-5111 TWX: 710-347-0212 TELEX: 94-8457

TWX ~~DEC Read~~ : I have answered

University of Technology

LOUGHBOROUGH LEICESTERSHIRE Telex 34319 Telephone 0509 63171

DEPARTMENT OF HUMAN SCIENCES

Professor B. SHACKEL Head of Department

1574

11 June 1975

The Technical Director,
Digital Equipment Corporation,
146 Main Street,
Maynard,
Massachusetts,
U.S.A.

NO. JUN 16 1975

Dear Sir,

I attach herewith an information sheet giving details of the NATO Advanced Study Institute which I am organising in Portugal at the end of August/beginning of September this year. I thought you might be interested to know of the very satisfactory progress in our arrangements.

We already have received 60 applications to attend the Institute, and there are still between 30 and 40 enquirers who have received forms but not yet replied. There seems every reason to expect a very full attendance, and my only regret is that we do not have enough funds to give more support to all the prospective participants who clearly merit an award. We have decided to spread the funds as far as possible by expecting all students to find partial support from elsewhere; therefore we have established a basic award to cover accommodation costs for all those students whom we can support, with an additional award towards part only of the travel costs for relatively few students who are unlikely to be able to get much support from other sources and whose travel costs are particularly high. Nevertheless, the indications are that we shall have a very full attendance.

The detailed arrangements with our lecturers are progressing well. 10 have positively confirmed their attendance, and I am expecting to hear positively from 2 more shortly. 2 have said that they cannot now attend, and I have invited 2 very appropriate replacements.

As you will appreciate, travel costs have escalated sharply in the last year or so. We have a considerable number of applicants both from the U.S.A. and from various parts of Europe somewhat distant from Portugal. As a result, some excellent students may not be able to participate in the Institute simply because they cannot get £100 help towards travel costs. By the way, I should emphasize that these students are all graduates of two or three years' standing, and many participants in this Institute have a Ph.D. and are even Assistant or Associate Professors.

In order to help towards the success of this Institute, I am wondering whether your Company would be willing to make a modest donation to the Institute funds so as to sponsor the travel costs of some participants. I would of course expect to make due acknowledgement by name (but not by financial amount) to your organisation appropriately in the conference record etc. I am writing to the four manufacturers of large computer systems and to four manufacturers of ranges of mini-computers seeking support of this nature.

I am sure that you will see the relevance of this Institute for the continued successful growth of the computer industry, as it moves into an era of less usage by specialists and more usage by non-specialists. I am hoping that your Company could see its way to assisting the Institute with a donation of between £500 and £1,000. If, as I hope, each Company is willing to assist us, then may I assure you that any surplus from the whole Institute programme will be set into a fund to sponsor further activities in the field of man-computer interaction. We have already proposed, as you see from the enclosed papers, the establishment of an international study group.

I look forward to hearing from you and to learning that your Company can assist us.

Yours faithfully,

Professor B. Shackel
Director: NATO ASI on MCI

Dear Dr Custom
Sally Engineering, but
in view of the
late date, I would
be concerned
that they for
we in a financial bind -

Dear
Thank you for your

Dear
Thank you for your letter regarding funding of
Fh _____. We believe this is important, but
do not have funds to support it now. Generally
~~we cannot fund~~

Professor Shackel is away and apologises for being unable to sign this letter.

It is possible that DEC UK might
have support funds; could I encourage you to contact them
through your

~~Our policy is to~~

cc: D.E.C. Reading, U.K.

Kindly

June 24, 1975

Frederick A. White
Professor and Industrial Liaison Scientist
Department of Nuclear Engineering
Rensselaer Polytechnic Institute
Troy, New York 12181

Dear Prof. White:

Thanks for your letter in regard to a possible liaison.

1. Adjunct Professors

   As a professor of Computer Science and Electrical Engineering at Carnegie-Mellon University, I believe this is difficult for the distance involved. If you have someone in mind at DEC, I would encourage you both to propose this.

2. Industrial-University Research

   Fine. What research would you propose here? Can you give us your programs, machines and research in Computer Science and Electrical Engineering to give us an idea of some possibilities.

3. The Dynamics of American Research

   Sure, let's talk if you can spare the time. Attached is a copy of a letter I sent to Dr. Stever of NSF with some examples.

In general, I believe points 1. and 2. are hard, since they should be discussed after we have a communications link at a technical level. Also, we have substantial interactions with several universities, which need to be improved. I'm skeptical of spreading ourselves thinner, but if your faculty has a link and the interest, these problems could be overcome.

Since I'm now only peripherally envolved in research now, it is more appropriate that you interface with Jim Bell, who heads our R&D group.

Look forward to hearing from you.

Sincerely,

Gordon Bell
Vice President, Engineering
Professor, Computer Science
Carnegie-Mellon University (on leave)

GB:mjk
cc: Jim Bell

DIGITAL EQUIPMENT CORPORATION, 146 MAIN STREET, MAYNARD, MASSACHUSETTS 01754
(617)897-5111 TWX: 710-347-0212 TELEX: 94-8457

D I G I T A L INTEROFFICE MEMORANDUM

SUBJ: M, D, AND IAS

DATE: 06-23-75
FROM: GORDON BELL
EX: 2236
MS: ML12-1/A51

TO: FILE

SUBJ: M, D, and IAS--THE ISSUES...on the table to resolve.

To: Larry Portner

I feel awfully uncomfortable on our choices, policy, fundins, etc. Don't you?

The whole thins is counter-intuitive:

1. Market--the market responds to M favorably, and wants more. Do we know somethins they don't?

2. Profit--sales of M are hisher and the product is profitable, as opposed to many software products which aren't. Normally we fund what's makins the money.

3. Manasement--there are manasement problems in D and IAS.

4. Product--technically M seems cleaner. Is D at the unstable breakins point?

5. Future--I don't believe we want D converted to VAX

The only reason to extend D is IAS. Is there another way to set functionality of IAS on M? MIAS?

Perhaps Phil could be useful here as an outsider in reviewins the software plan from these various aspects.

Let's come at this one.

[Should this be sent to: Wade, Laut, Plowman, Neal, Cutler, and Levy?]

GB:mJk

D I G I T A L INTEROFFICE MEMORANDUM C1528

SUBJ: VAXA STATUS

DATE: 06-23-75
FROM: GORDON BELL
EX: 2236
MS: ML12-1/A51

* *
TO: FILE
* *

SUBJ: VAXA STATUS--for June 24-25 Planning Meeting

To: Distribution

Architecture (Medium-level definition)

This definition should be of a form sufficient to build from, although many tiny issues will have to be resolved.

Addressing: complete proposal which satisfies goals but doesn't feel right; final pass recommendation due 18 July.

Instruction-set: complete final pass by 27 June including I/O, condition codes, call-return, and string (first pass only).

Process-structure: Complete.

I/O instructions: will be in Instruction-set.

Architectural evaluation: in preparation due with ISP (see ISP evaluation and tuning below).

Architecture (Detailed definition specification)

We intend to write a detailed specification which has a text description consisting of the various mechanisms (e.g. instructions), their rationale and goals, and rejected alternatives. The specification also includes an ISP language definition to precisely define the machine.

This description can be pared to provide the machine reference manual.

Requires: Strecker, Hastings, Rodgers, Bell and Dickman. (A really good technical writer might be useful)

Completion: about 2 months.

ISP Evaluation and Tuning (Benchmarks)

SUBJ: VAXA STATUS

DATE: 06-23-75
FROM: GORDON BELL

This will proceed concurrent with the detailed definition specification. The purpose is to ascertain how well we meet various code quality and ease of generation goals (e.g. the static and dynamic code size is a factor of 2 better than FORTRAN IV+ produces) with less processing. The goals are being specified now in detail (Rodgers and Bell). Marty Jacks and Jack Burness will carry out the first evaluations. We need someone to benchmark us against competition: HP3000, MODCOMP, DG, and Interdata. Could get this done outside, but prefer not.

Language Specification Contracts

We intend to have each language group write a contract (specification) for: code generation, run time environment and operating system, and structure of translator mechanism as it uses the ISP. Thus, for COBOL, FORTRAN, BASIC, PL/1, and the Implementation Language we can evaluate the ISP.

Operating System Architecture

The Operating System is an extension of the basic machine architecture to provide certain run time environments. There has been no work yet in this area, except to define the hardware generally to accommodate various style operating systems.

We are long overdue in the establishment of goals, constraints and assignment of tasks, etc. We must have a principal architect.

GB:mjk

Distribution

John Buckley
Peter Conklin
DaveCutler
Bruce Delagi
Bill Demmer
Roger Gourd
Len Hughes
George Plowman
Steve Rothman
Larry Wade

cc: VAXA

D I G I T A L INTEROFFICE MEMORANDUM

SUBJ: LANGUAGE TRANSPORTABILITY
DATE: 06-19-75
FROM: GORDON BELL
EX: 2236
MS: ML12-1/A51

TO: FILE

SUBJ: 10 BASIC TRANSPORTABILITY TO 11

To: Distribution

I've heard a lot of examples, problems, and possibility of writing interpreters, compilers (and other software) on a given computer system, and then transporting the language to another system. At one point, we were considering such a system for 10 BASIC to be transported to the 11, written in BLISS.

With another computer to program for, it seems highly desirable that we develop techniques of this sort so that languages (for example) can be made available on various systems without totally rewriting them.

Are we doing anything of this sort on the 10 for eventual 11 use?

How (can) one build a program of this sort? (E.g., the Design Automation group hand compiles 11 BLISS for the 15). Do you just make rules to accomplish this?

What languages (e.g. COBOL) are more machine independent?

When can we try an experiment of this form, so as to move more into a production mode? Can you people discuss this, and then meet with me and explain the position?

GB:mjk

Norma Abel
Pete Conklin
Ron Hamm
Jim Mills
George Plowman
Larry Portner
Larry Wade

D I G I T A L INTEROFFICE MEMORANDUM

PAGE 1

SUBJ: OOD GOALS

DATE: 06-19-75
FROM: GORDON BELL
EX: 2236
MS: ML12/A51

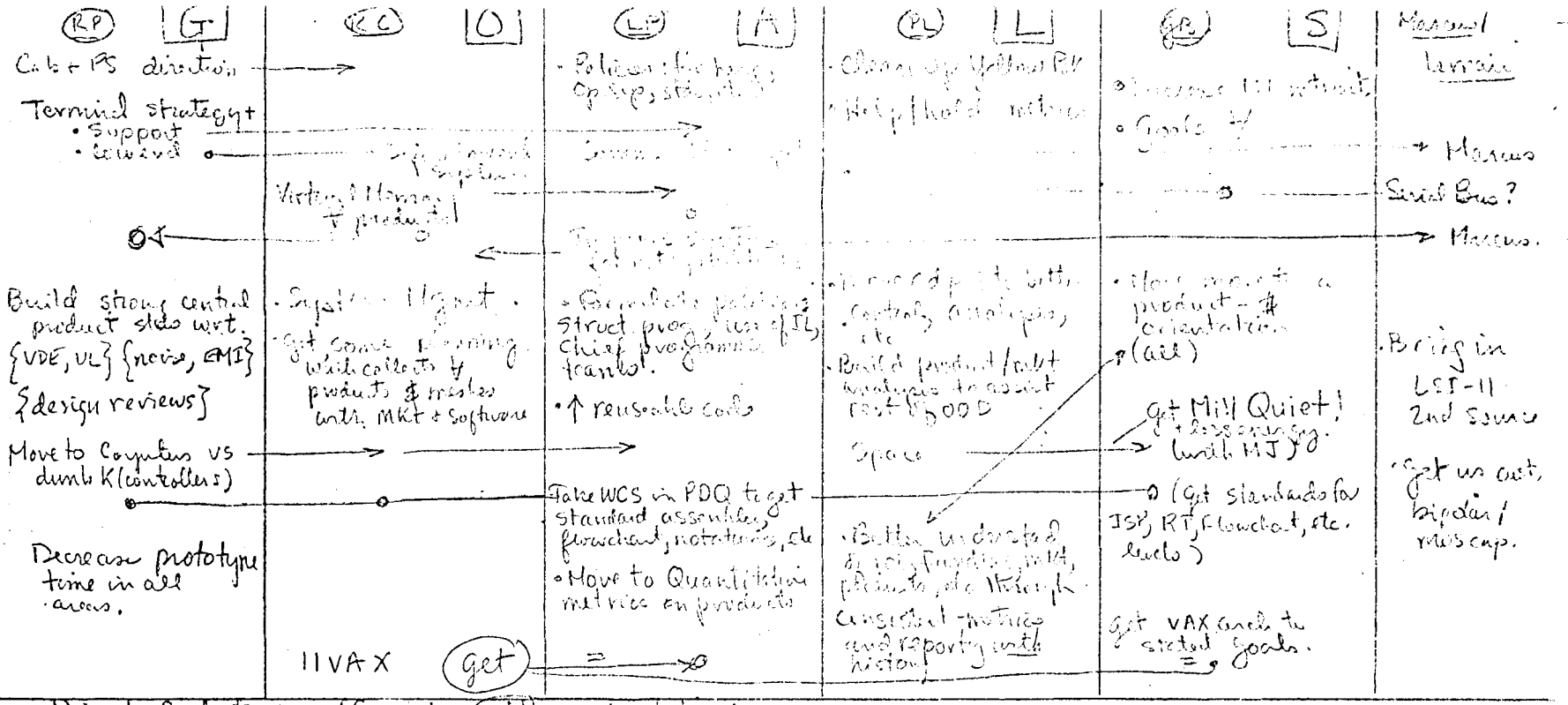
TO: OOD ML

To: OOD

Having spent 2 days in the pleasant surroundings of Dick's cottage and listened to us all try to transmit our hangups, I feel it's necessary for us to set at both joint and individual goals. It also is clear to me that you each have incredible power to get things done. As individuals, I'm sure we all believe in Bob's policy to try and segment things so that we can all proceed with our jobs in as nearly an independent fashion as possible, but there are great interdependencies.

In Oct. 74, I attempted to put down areas we needed goals and policies (not the detailed goals or their implementation). An update of this which is just a first pass (is attached). I'd like some feedback of these areas, and then I'd like to re-organize them for general discussion along products, people, process, planning, paper (control) lines...or some other way to get at them in a clean, orthogonal way. Also, please send me the current goals you're operating under (e.g. Larry's reattached). It's mandatory that this get on 1 sheet of paper (no spec on size) such that joint goals are identified along with responsibility, and most important the priority.

What you think?



- Drive to product-payoff orientation (all)
- Educate OOD wrt each group: structure, goals, philosophy, control metrics
- Fix Product Approval process + document
- Team - as needed (like Physail)
- Establish architectural direction to assist individual groups.
- Know Position of products { } { } phases:
  Clear delineation of funds for study, proposal, design/tool, produce (support), Rejuvinate.
  Policy: Each group must have ± activity in each category.
- Establish Productivity measures for groups
  Joint evaluation of direct reports + clean up engineering levels)
- Joint mtgs on State-of- engineering, products, technology, people, etc
- Quality: form metrics, in new design
- ↑Systems focus: mgmt more direct, fund clearly in 2 dimensions
- Work standards especially to reduce cost, increase interconnectability, ease learning, disc/prod
- Generally increase # of prototypes, which
- Get PDP-11's in use within OOD.

Increase interact with MC/PL's
Services + Mfg
including lower noise (EMI, d's)

OZD Possible Goals? 15/76 GB June 15, 75

Control (PL)	Peripherals (RF)	Systems/Software (KC)	Software (LP)	Technical Staff (GL)
• Formulate M/Reg better • Build total eval. System for M/B. (Rankall prod/proj) • Get EDP strategy / goals (also Soft.) • Streamline reports (use our C's)	• Paperpunch media • Cabinet/[illegible] • Strategy in smartT (LA36+) 000451	• Interrupts • Multi-tp • Virtual Memory in all machines (-3) • Single K (controller) → Controller support • Smarter K. →	• Language Advances • "OS" • Networks • [illegible]	
	• EMI, VDE, IIL, etc. process • Field integrate; easy configuration. • Speed D/R, proto process • Mgrs, develop.	• build more ideas	• Improve throughput • Decr Soft. dept. • More mini-applic. • [illegible] • Front. prog. standards • Qual. [illegible] reliable users	
• Co-ordinate people, #, space, plans. • Streamline processes, reports, etc.	(All) • Develop / integrate to get overall comp. system strategy (Including C in hand, tools, profs) • Know position ∀ Products ⇒ Move farther (esp. disks) • Work together better • Better documentation on □²D, PM, Eng. etc. processes • Hard C. Sys. Courses • more technical education • Grow Mgrs. • Get schools PM, Eng. Mgr			
• Get contract: KO, @²D; • Eng. Committee operate better •	(GB) • Space process.			

C1533

Possible 1974-1975 Goals for O²D GB Oct. 12, 1974.

OBJECTIVE	RESPONSIBILITY
Specific	
. Clarification of roles and responsibilities of the various management and technical levels - for example, do we use consulting programmers properly? Who develops implementation strategies? Who is responsible for absorption of new product technology?	G. Plowman/L. Wa
3.3 Improve Recognition and Participation for Key Software Development Personnel	
General	All
. Build a high level team with increased visibility to the company so they be recognized, and who with increased visibility of the company, can operate from the broadest possible perspective.	
Specific	
. Prepare and maintain a menu of likely candidates for both Research and Advanced Development projects.	J. Bell
. Cycle at least 2 superior technical people each year from the research group into the Software Development activity.	J. Bell
. Cycle at least 2 superior technical people each year from the development activity into the Research group.	G. Plowman/ E. Fauvre
. Participation in the "Advanced Development" activity.	G. Plowman
. Aggressive joint planning with the Product Management Group.	G. Plowman
. Development of a competent and visible management and technical staff in the applications area.	E. Fauvre
. Aggressive exposure to the Product Lines, Marketing Committee, OOD, etc., to help bring focus on growing applications activities in the corporation.	E. Fauvre

4. OTHER OBJECTIVES

OBJECTIVE	RESPONSIBILITY
4.1 Improve Services to our Internal and External Customers	
PRODUCT MANAGEMENT	
Specific	
. Publish overall software business strategy guidelines for use of Product Managers and Product LIne Managers (use output from Ted Johnson's Committee).	M. Woolsey
. Prepare business plans consistent to the Business Strategy guidelines, but above all with a sensitivity to our marketing requirements.	M. Woolsey
. Continue to tighten ties with Software Services.	M. Woolsey
HARDWARE ADMINISTRATION	
. Long term plan for supporting needs of software organization.	E. Fauvre
. Increased service to the software developers, at decreasing cost to the corporation.	E. Fauvre
. Proposal on development utilization alternatives.	E. Fauvre
SDC	
. Automation of order picking - order processing	O. Kostetsky
. Maximum of 1 week turnaround to customer orders.	O. Kostetsky
. Regional SDC's where economically or politically appropriate, or where service required. Maximum of one week turnaround to customers.	O. Kostetsky
. Priority system for field orders, including an "instan ship" option.	O. Kostetsky
. Periodic (twice a year) evaluation of kit contents, costs, effectiveness.	O. Kostetsky

OBJECTIVE	RESPONSIBILITY
2.4.3 General	
. Strengthen and formalize the inputs to planning and development.	
Specific	
. Have all new product starts approved by Products Committee.	M. Woolsey/L.Wa
. Formalize the PSG process; meet at fixed frequency with clear agenda and intentions; formalize inputs from participating groups, and prepare formal quarterly reports of product requirements to the Planning and Development groups.	M. Woolsey
2.5 Develop a Clear Uniform Process for Maintenance and Field Support	
2.5.1 General	
. Clarify our software maintenance process in support of new corporate software warranty.	M. Woolsey
. Establish an "E.C.O." process for software.	G. Plowman
Specific	
. Short term - analysis and proposal of the "Support Monster" problem.	J. Mileski
PEOPLE/ORGANIZATION OBJECTIVES	
Improve Organizational Depth	
3.1.1 Specific	
. Implement the Advanced Development function by end of Q1, including at least 2 participants from the development organization.	J. Bell
. Hire at least 4 technically superior individuals each year.	J. Bell
. Provide an effective Departmental Planning function to plan and implement the resource (human, financial, hardware, space) and organizational (structure, methodology) requirements in support of Software Engineering goals.	L. Wade

OBJECTIVE	RESPONSIBILITY
Specific	
. Develop effective Software Product Plans in support of Central Engineering and DEC-10.	L. Wade
. Formalize the PSG process; meet at fixed frequency with clear agenda and intentions; formalize inputs from participating groups, and prepare formal quarterly reports of product requirements to the Planning Group.	M. Woolsey
. Implement aggressive joing planning with the Product Management Group.	G. Plowman
. Clearly document a statement of diagnostic trends in the industry, and long term plans for DEC diagnostics.	E. Fauvre
*. Short term - Develop and establish as a corporate posture a simple, salable and achievable maintenance and support policy for our products (in lieu of "Warranty" statement").	G. Plowman/ H. Spencer/ M. Woolsey
. Establish a competitive analysis activity able to evaluate current competitive products, and predict competitive moves.	M. Woolsey
. Substantial upgrade in the line management structure.	G. Plowman E. Fauvre
. Availability of skilled applications developers in each of the applications areas of major interest to the corporation.	E. Fauvre
. Staffed and operational high level consulting role in Reliability Engineering applying a documented philosophy and methodology for setting Quality and Reliability goals, and designing, testing and implementing these goals.	J. Mileski
3. Increase Emphasis on Individual Responsibility and Accountability	
3.2.1 General	
. Products debugged by the developers - neither field test nor Q.A. audit should be able to find more than a few infrequent bugs, and no catastrophic failures.	G. Plowman/ E. Fauvre

*High Priority

OBJECTIVE	RESPONSIBILITY
. Operational new development policies by June.	G. Plowman
. Perform comprehensive review of plans at the detailed technical level for rigid adherence to specification, standards, quality and reliability goals, and spec discipline.	G. Plowman/ E. Fauvre/ J. Mileski
Specific	
. Jointly, with Development and Planning Groups, devise and implement a system (the War Room) for tracking and displaying the plans, resources, commitments, and changes to the plan.	M. Woolsey
. Periodically, with the development manager, review development activities for conformance to the plan, and issue a report on the "state of development".	M. Woolsey

2.3 Upgrade the Development Technology/Methodology

2.3.1 General

. Rapidly develop a development methodology, including higher level languages, debugging and design tools and methods, appropriate machine access, with automated bookkeeping and librarian type aids.	
. Model and simulate new software.	
. Build in performance analysis tools.	
Specific	
. Thru Research, bring in at least 2 new products or process technological improvements each year.	J. Bell
. Develop and disseminate an applications technology with emphasis on methods and utilization of resources.	E. Fauvre
. Aggressively install mechanisms and procedures to aid in the execution and management of programming projects.	G. Plowman
. Better methods for module test program generation; growth in this area (manufacturing support) seems unreasonably high.	E. Fauvre
. A documented philosophy and methodology for setting Quality and Reliability goals, and designing, testing and implementing these goals.	J. Mileski

OBJECTIVE	RESPONSIBILITY
2.3.2 General	
. All non-operating system development done in higher level languages.	E. Fauvre/ G. Plowman
*. Short term - commitment to and plan for use of BLISS - develop list of criteria for use of BLISS on any specific project.	G. Plowman
Specific	
. 90% of all applications work done in high level language.	E. Fauvre
. Significant portion of all diagnostics done in high level language. (Manager to supply definition of significance).	E. Fauvre
. Aggressive support for high level language (BLISS) development facility.	E. Fauvre
2.4 Improve the Planning Process	
2.4.1 General	
. Definition and integration of the Systems Architect role.	L. Wade
Specific	
. Develop a Systems Architecture function in order to achieve system-wide product cohesiveness, positioning, compatibility, efficiency and ease of implementation.	L. Wade
2.4.2 General	
. Continuously reduce product support costs on a per-product basis. This includes all aspects of support, such as internal maintenance, field support, SDC costs for updates, etc.	
. No new product development without a long-range plan, covering new releases, updates, new versions, etc. Question - can we ever complete a product?	
. Clear, effective maintenance and support plans - how will we support our products in the field?	

*High Priority

OBJECTIVE	RESPONSIBILITY
Specific	
. Have totally transportable device drivers.	G. Plowman/ E. Fauvre
. Develop Software Product Plans for each Software Product Family, including clear product positioning, time phasing and competitive goals.	M. Woolsey/L. Wad
. Integrate the Software Product Family Plans for consistency across families.	M. Woolsey/L. Wad
*. Short term - clarify compatibility goals (10-11, INTRA 11, 11/85, 11/70-32) and develop compatibility plan.	G. Plowman/L. Wad M. Woolsey
. Management support of standards activity and implementation plan for current and emerging standards.	G. Plowman
. Development of uniform standards for applications quality, reliability, documentation, etc.	E. Fauvre
5. Simplify the Product Offering	
1.5.1 General	
. Minimization of product set thru standard interfaces, modular implementation, etc. Guidelines in the foreseeable future - there should not be more than 2 implementations of any language processor or major utility.	G. Plowman/ M. Woolsey
. Decreased emphasis on ultra small core systems; core is getting cheaper, software is more complex.	G. Plowman/ M. Woolsey
Specific	
. Phase out old versions/multiple versions of products.	M. Woolsey
. Better organization of documentation set.	O. Kostetsky
. Share all language and utility manuals; write them once, and change only the cover.	O. Kostetsky
. Fewer pages in the manual set, with higher information content.	O. Kostetsky
. Maximum of 3 distribution mediums.	O. Kostetsky
. Continuous reduction of per system software kit costs.	O. Kostetsky

*High Priority.

2. PROCESS OBJECTIVES

OBJECTIVE	RESPONSIBILITY
2.1 Install Software Engineering Process	
2.1.1 General	
. Perform no development without a plan.	All
Specific	
. SYSTEMS - FIRST AND FOREMOST - NO DEVELOPMENT FOR 32 BIT SYSTEM WITHOUT TOTAL LONG TERM DEVELOPMENT PLAN, INCLUDING CONVENTIONS, TECHNIQUES, SPECIFIED SOFTWARE SYSTEM ARCHITECTURE TOOLS PLAN, SUPPORT, DISTRIBUTION, AND MAINTENANCE PLAN, ETC.	G. Plowman
. DIAGNOSTICS - NO DEVELOPMENT OF 32-BIT SYSTEM WITHOUT CLEAR, DOCUMENTED OVERALL DIAGNOSTIC STRATEGY.	E. Fauvre
*. Short term - documented development plans for FY76.	G. Plowman/L. Wad
. Each new product should specifically address hardware/software tradeoffs. Should we implement it in ROM? or WCS? Should the error recovery be hardware or software? What are application requirements that have hardware/software implications? Such as context switching, character handling, and memory management?	G. Plowman/ M. Woolsey
2.2 Improve Ability to Manage to the Plans	
2.2.1 General	
. Have a clear statement of product goals at the component, subsystem, and system level.	G. Plowman
. Install a process for maintaining the development plan, tracking and controlling changes to the plan, including changes in goals, scope, content, technique, schedule or budget.	G. Plowman/ E. Fauvre
. 80% of the projects must meeting schedule and budget, and do it without redefining the content, or changing the goals - too many of our commitments end up being met in the "next release".	G. Plowman/ E. Fauvre
*. Completion, installation and maintenance of a useful Software Engineering Policies and Procedures Manual.	G. Plowman

*High Priority

OBJECTIVE	RESPONSIBILITY
. Clear attention in the diagnostic strategy and plans to support the highly leveraged areas, such as Field Service.	E. Fauvre
1.3.2 General	
. Achieve a meaningful integration of hardware and software planning and development, so that we can profitably address the tradeoff opportunities between the two disciplines.	L. Wade M. Woolsey G. Plowman
. Each new product should specifically address hardware/software tradeoffs. - Should we implement it in ROM? or WCS? Should the error recovery be hardware or software? What are application requirements that have hardware/ software implications? Such as context switching, character handling, and memory management?	
Specific	
. Install scheme for tracking and controlling hardware support commitments.	G. Plowman
1.3.3 General	
. Strong applications orientation in all of our products. Each new development should specify several planned applications areas and specifically address the issue of these applications support requirements.	M. Woolsey G. Plowman E. Fauvre
Specific	
. Establish and maintain a clearing house of all applications development planned or underway in the corporation.	E. Fauvre
. Formal consulting/planning role to provide an "applications requirements" input to new systems software.	E. Fauvre
. Aggressive participation in new "small systems" development.	G. Plowman E. Fauvre
1.4. Establish a Software Product Continuum from Low End 11 through High End 10	
1.4.1 General	
. Have absolute upward compatibility through the entire product set.	
. Intensify concentration on standards to achieve compatibility goals.	G. Plowman

OBJECTIVE	RESPONSIBILITY
. 100% accuracy of examples in present and future manuals.	O. Kostetsky
. Zero defects program in the SDC shipped kits.	O. Kostetsky
1.2.2 General	
. Development and implementation of an overall RAS concept for our products.	J. Mileski
Specific	
. Overall RAS program for DEC software (and systems).	J. Mileski
. Useful statement of RAS goals for DEC products and a measurement and feedback system.	J. Mileski
. Documented RAS goals for all diagnostic products and supportive diagnostic plans.	E. Fauvre
1.3 Improve the Product Contents	
1.3.1 General	
*. Documented technical strategies available and updated at the component, subsystem and system level. How are we going to make our products?	G. Plowman
Specific	
. Hold quarterly "State of the Technology" presentations for interested audiences.	J. Bell
. Thru Research, bring in at least 2 new products or process technological improvements each year.	J. Bell
. Develop effective Software Product Strategies in support of Central Engineering and DEC-10.	L. Wade/M. Wools
. Maintain consistency between the product strategy and the product plans.	M. Woolsey
. NO DEVELOPMENT OF 32-BIT SYSTEM WITHOUT CLEAR, DOCUMENTED OVERALL DIAGNOSTIC STRATEGY.	E. Fauvre

*High Priority

OBJECTIVES

01535

1. Product Objectives

   1.1 Gain Market leadership; position

   1.2 Achieve higher product quality image

   1.3 Improve the product contents

   1.4 Establish a product continuum from low end 11 thru high end 10

   1.5 Simplify the product offering.

2. Process Objectives

   2.1 Install a Software Engineering process which operates to plans

   2.2 Improve ability to manage to the plans

   2.3 Upgrade the development technology/methodology

   2.4 Improve the planning process

   2.5 Develop a clear uniform process for maintenance and field support.

3. People/Organization Objectives

   3.1 Improve the organization's depth

   3.2 Increase the emphasis on individual responsibility and accountability

   3.3 Improve recognition and participation.

4. Other Objectives

   4.1 Improve services to our internal and external customers.

PRODUCT OBJECTIVES

OBJECTIVE	RESPONSIBILITY
.1 Gain Market Leadership Position	
1.1.1 General	
. Product superiority in most of the products most of the time. Development should always occupy a dominent product position in its marketplaces - this doesn't mean we can (or have to) be best in all aspects of every market, but it does mean that we must have at least one leadership product in every major segment of each of our markets. If we can't afford to occupy a leadership position, perhaps we are in the wrong markets.	
Specific	
. Establish and understand the competitive environment for all software products, and demonstrate this understanding in the Business Plans, "family" plans and in pricing approval presentation.	M. Woolsey
. Develop semi-annual report on our competitive posture in software and systems.	M. Woolsey
.2 Achieve Higher Product Quality Image	
1.2.1 General	
. Have the highest quality software in the industry - "if you buy it from DEC, it will work!"	
Specific	
. Installation of a Q.A. policy and procedure for centrally and non-centrally developed software.	J. Mileski
. Implementation of a field test policy and procedure.	J. Mileski
. Staffed and operational independent Quality Audit activity.	J. Mileski
. Higher communication quality in our manuals - test them by having the writers trade manuals with the recipient using the documentation to use the system.	O. Kostetsky
. Better print quality, particularly of examples.	O. Kostetsky

To: OOD Fm: GB 15 Jun 76

INTEROFFICE MEMORANDUM

TO:

DATE: ?

FROM: ?

C1534

DEPT:

SUBJ: Software Development - Goals and Objectives - 1976

useful for OOD group

The enclosed set of goals and objectives are put together in hierarchical form from the top down and represent the beginning step in a management by objectives program for 1976.

Directly behind the cover you will find the goals, the objectives in the same four catagories as the goals (Product, Process, People, Other), and following that several pages of further expansion of the objectives with both general and specific task assignments by department, the accomplishment of which is mandatory.

The intent now is to have each group manager generate a response to these objectives (the general objectives, tasks, and those specific to his departments) which contain his two-year plan for accomplishing the objective, how it will be measured, and when it or it's parts will be completed. These plans will then be integrated, reported against monthly, by the group, and managed to from the Vice Presidential level.

The basic understanding here must be that goals and subgoals are long term goals which cannot be accomplsihed overnight, somewhat overlap each other, require a measurable plan, and the tecmwork of each member of Software Development toward our common ends.

Everyone should address each general objective with a plan for it's accomplishment and measurement. If there is a specific objective also listed by name then this specific should be addressed and incorporated into the plan with completion dates and measurements.

Your plan is due to me by

This-type document might sure be useful to us. However, is a document like this for OOD

1 The collection of your documents (I only have two)?

2 Something we build, as a prelude to doing 1? GBell

GOALS

External Goal:

To establish Software Engineering as a significant, visible, contributory growth vehicle for the corporation which permits flexibility of market selection and maximizes hardware and system sales.

Internal Goals:

Because it is through

1. the integrity and contents of the product we provide
2. our ability to implement and efficiently operate the process for better product creation
3. the quality, depth, and efficiency of our human resources that operate the process of Software Development.
4. the strength of our reputation

that our goals will be attained; the internal goals are in 4 parts.

1. Product Goal:

   To continuously make available products of higher quality and performance which allow the corporation to occupy a dominant position in it's present and future end-user market places.

2. Process Goal:

   To ensure the timely completion of product development to the appropriate plan in keeping with the customer and corporate expectation of cost and performance, through a disciplined engineering process.

3. People Goal:

   Maximize the performance of our human resource by having the required technical/managerial depth and providing an environment for their personal achievement, advancement, and recognition.

4. Other Goal:

   Strengthen total corporate operations through the services provided to both internal and external customers.

01547

0156 1445 17-JUN 20541 1445 17-JUN
MP30 LPTR GENB

ZCZC
GG
MSG NO NA14

TO: MARC BASSIN - GENEVA

PLEASE TALK DIRECTLY WITH PROF. MICOUD REGARDING LSI-11
ADVISTING SHIPMENTS, DELIVERY, STATUS AND THE SERIOUSNESS
OF HIS VIEWS.

FROM: GORDON BELL - MAYNARD

REGARDS
JG
NNNN

C1548

D I G I T A L INTEROFFICE MEMORANDUM

SUBJ: OOD STAFF AGENDA 6/19/75 DATE: 06-18-75
FROM: DICK CLAYTON
EX: 3638
MS: ML5-2

TO: OOD ML12-1

10:30 Review this week's asenda and settle on future topics.

10:45 From the Cape:

Pick tenative date for Jungle.
Decide on cross group presentation.
When should we focus on new PC.

11:15	Proposed policy on magazine subscriptions	Portner
11:20	Approval policy	Laut
11:30	Employee Development	Abbett
12:00 Lunch	WPI Masters Degree Program Proposal	Hall/Abbett

FUTURE TOPICS

DATE	ITEM		RESPONSIBLE
6/26	Personnel Goals for FY76		Abbett
6/26	Computer Resource Consolidation		Rutledge
7/3	Yellow book revision plan	45 min.	Laut
7/3	VT51 Software		Portner/Puffer
7/3	Computer Packaging State		Nye
7/?	MSC Proposal		Hughes/Lemaire
7/?	Secretarial Utilization		Abbett
7/?	STACK		Croxon
7/?	ECO/Rev Level Control		
7/?	Field Integration		Jack Smith
7/?	Q BUS		Cady
7/?	Packet Switching Capability		Alusic
7/?	Multidrop development for LA36		Marcus
7/?	LA36 cost reduction		Huefner

Future Jungle--What are proper levels of development expense in the light of vertical integration, more software, fewer products, etc.

SUBJ: OOD STAFF AGENDA 6/19/75

DATE: 06-18-75
FROM: DICK CLAYTON

C1549

Attendance (all here except):

6/26 Clayton (Japan)
7/3 Puffer (Vac), Portner (Vac?)
7/10
7/17
7/24
7/31

digital

INTEROFFICE MEMORANDUM

TO: OOD LOC/MAIL STOP

DATE: June 17, 1975
FROM: Mark Abbett
DEPT: Central Development Personnel
EXT: 2633
LOC/MAIL STOP: ML12/A11

SUBJ: EMPLOYEE DEVELOPMENT

PURPOSE

This memo is intended to pull together my thoughts on the subject of Employee Development within Central Engineering. What is it? Why is it needed? What would be a reasonable program and how might it be implemented? Please consider the points made and I will be discussing this subject further at the 6/19 Staff Meeting.

BACKGROUND/PROBLEM STATEMENT

- An article appeared recently in the Harvard Business Review entitled"Accelerating Obsolescence of Older Engineers". The study was done by Paul Thompson of the Harvard Business School and talked about an efficiency rating which correlated an engineers ability to contribute to the time since his date of graduation. With no formal program of continued development, an engineer would be expected to reach a plateau nine to fifteen years after graduation and then his technical knowledge and contribution would start declining. On the other hand, with a formal development program, the technical life expectancy of an individual contributor would be doubled. Within Central Engineering, with new technologies being developed each year, engineering obsolescence is a priority concern.

- Educational Training at DEC is decentralized, uncoordinated, and in many cases, highly political. Look at the number of training programs and organizations that are scattered throughout the company; Del Lippert, Field Service, Mert Kenniston, Manufacturing, Charles Dyer, Software, Nick Pappas, Software Support, Jean Lougee, Clerical and Craig Zamzow, Sales Training to name a few. It seems to me there is a lack of consistency in the types of in-house training given and whether or not they meet the employee's and corporations needs.

- In starting a program of performance reviews, it is important that a section be devoted to an employee development plan. This plan should help to eliminate weaknesses and build on strengths. Right now, we have no resource book similar to the Management Training Manual that managers and Personnel Representatives can refer to in identifying programs that would be for the employee's personal development.

- o There does not seem to be a reasonable balance of our company resources between management development and employee development. Based on the time, effort, and programs available, I would guess that the split is 90%/10%.

- o There is only a small percent of employees who take the initiative to continue their development. During second semester, we had but 9.1% of our employees participate in the company Tuition Refund Program. Unless managers encourage the need for continuing development, this percent will not improve.

PROPOSAL

Phase I To Be Implemented During Q1

An immediate need is to summarize, in one brochure, the existing programs available at DEC for employee development. Jim Murphy has tackled this project for the Software Engineering organization and a similar manual should be developed addressing the available training for Hardware Engineers. These documents should be completed as soon as possible and ideally should be distributed to Personnel Representatives and line managers during the corporate Performance Review Workshop. The workshop seems to me to be an ideal time to discuss the relationships between performance appraisal, plan and development and how this document may be used as a resource.

Relative to Programmers and Engineers at DEC, I feel the manuals should include:

Section I	Relevant WPI and BU on campus courses with information on course content and objectives, eligibility and administrative information.
Section II	Other university programs at Lowell Tech., Northeastern, University of Massachusetts, etc.
Section III	Books, magazines, and cassettes available in our technical library with a short description of each.
Section IV	A summary of all in-house DEC training programs.
Section V	Planned special seminars and workshops with information on course outline and objectives.

Phase II To Be Implemented During Q2

Generally, during this phase, we should address the issues of how do we better identify the training needs of our employees and then influence the different training resources to better meet those needs. During Phase II, I would like to see OOD's support and guidance in forming a committee made up of Central Engineering Consulting Programmers and Engineers with a broad charter and responsibility for the technical excellence of our Engineering Organization. Jim Bell might be an excellent person to "chair" this committee whose charter would initially include:

1. Techniques for better publicizing existing programs to increase enrollment. This is needed as the company must actively compete with Adult Education, Company and Community Recreation Programs, Television, Movies, etc. for our employees free time.

2. What are the immediate or short term needs of development engineers at DEC. In response to this, identification of non-credit 5 day programs on microprocessors, T squared L logic, LSI technology, etc. could be put on by local universities or vendors to meet our needs.

3. Long Term Planning would include evaluating existing programs and recommending appropriate changes. This would include working with BU and WPI to assist in improving existing courses and designing additional ones more related to our needs. The same relationship should exist between the committee and Educational Services, the Library, and other local universities.

4. To administer the present fellowship program with Carnegie Mellon. This should be expanded to include not only Software but Hardware Engineers within our total organization.

Phase III To Be Implemented During Q3

Expand the program possibly with a defined budget. The Employee Development Committee would tackle projects such as:

1. Planning and implementation of a three day Woods Meeting for individual contributors.

2. Expanding the Carnegie Mellon program to include other universities in a broader range of studies for periods up to one academic year.

3. During this phase, the committee should probably start looking at philosophical questions such as should DEC commit to a certain percent of company time for employee development? I believe that IBM's Research and Development Center in Poughkeepsie insists that their development engineers spend 20% of company time in continuing educational programs.

4. Finally, this phase should also include the expansion of employee development into areas of technical hourly employees.

SUMMARY

Central Engineering has the most to gain by actively addressing this issue. This is an area where we should lead and set the standard for the rest of the corporation. I strongly feel that this is an important area to address and am willing to commit Personnel resources to work on projects such as the development of the Employee Training Manual to make this program sail.

I need from you:

1. Top down support within your organization to aggressively address the issue of Employee Development.

2. To support the formation of the Employee Development Committee and help in defining it's charter.

3. Some level of commitment and encouragement as to where we want to be a year from now.

4. A small level of funding so that this committee can make decisions on scholarship programs, Woods Meetings, etc.

clg

digital INTEROFFICE MEMORANDUM

TO: ALL COST CENTER MANAGERS

DATE: December 6, 1974

FROM: Finance and Administration Committee

DEPT:

EXT: 5311 LOC: PK 3-2

SUBJ: MAGAZINE AND NEWSPAPER SUBSCRIPTIONS

The Finance and Administration Committee has requested that all Cost Center Managers be made aware of Digital's position with respect to the purchase of magazines and newspapers.

The Company will not pay for any subscriptions to magazines or newspapers, such as Wall Street Journal, Business Week, Time, Electronic News, etc., except in very limited special situations. ~~These exceptions~~ must be approved by a Vice President.

The practice is that all magazine and newspaper requisitions must be processed through the Library in Maynard.

Subscriptions to general interest magazines previously purchased for lobby and reception areas will no longer be approved. It is suggested that product material and publications put out by Digital be used in those areas.

As a reminder, all professional society memberships and dues are also processed through the Library according to the details of Policy 4,21 in the Personnel Policies and Procedures Manual.

jam

digital

INTEROFFICE MEMORANDUM

TO: Distribution

LOC/MAIL STOP

©1555

DATE: May 20, 1975
FROM: Renate Baptiste
DEPT: Library
EXT: 3824
LOC/MAIL STOP: ML 5-4/A20

SUBJ: MAGAZINE AND NEWSPAPER SUBSCRIPTIONS

The attached quotation* lists the magazines and newspapers to which you subscribed in April 1974. Their expiration date is July 1, 1975.
Rather than wait for the July ordering period, we are sending this quotation to you for your approval now.
If we do not receive your quotation by May 27, 1975 your subscription will not be renewed.

To renew a subscription

1. Have both your cost center manager and vice-president sign the quotation.
2. Check the mailing address to be sure it is correct.
3. Return the quotation to the Library (A20) by May 27, 1975.
4. Please attach all renewal notices for subscriptions listed on quotation.

To cancel a subscription

1. Cross out the item on the quotation.
2. Return the quotation to the Library by May 27, 1975

To add a subscription

1. List the title on the quotation
2. Have both your cost center Manager and vice-president sign the quotation.
3. Return the quotation to the Library (A20) by May 27, 1975.

You will have another opportunity to place subscriptions in July.
If you have any questions, please call.

*Please note this is not an invoice.

June 18, 1975

Dr. Ronald Moskowitz
Ferrofluidics Corporation
144 Middlesex Turnpike
Burlington, Massachusetts 01803

Dear Dr. Moskowitz:

Your ferrofluidics reports are interesting. I've sent them on to Mr. Grant Saviers, who heads our disk group. He should contact you if there is some need in the disk area and/or other electromechanical equipment.

Sincerely,

Gordon Bell

Gordon Bell
Vice President
Office of Development

GB:mjk

cc: Grant Saviers

DIGITAL EQUIPMENT CORPORATION, 146 MAIN STREET, MAYNARD, MASSACHUSETTS 01754
(617)897-5111 TWX: 710-347-0212 TELEX: 94-8457

SUBJ: AGENDA/MINUTES--OOD

DATE: 06-24-75
FROM: DICK CLAYTON

MINUTES OOD STAFF 6/19/75

1. Future Agenda Topics

Dick will write memo to change group to look at more use of in house PDP-11 computer utilities.

Bob Puffer suggests the 6-25 Woods meeting on Packaging should be used for OOD focus on this topic.

Mark Abbett will work with Bob and Larry to do the Polly & Becky show for their managers of secretaries.

There was general agreement with Brian Croxon's proposal on STACK.

We reaffirmed the packet switching issue is squarely in the domain of Julius.

2. July OOD Jungle Meeting (Bob Puffer, Chairman)

We agreed to a one day (plus evening before) meeting at Larry's cottage. The topic is to be OOD and individual group goals. It was generally believed the goals are a relatively short issue. We want to focus on the priorities of actions implied by the goals.

3. The approval policy being proposed by Central Finance was discussed with Bob and Phil, noting a number of holes. We agreed that within OOD we aren't usually being pressed to liberalize approvals to the degree the proposed rules tend to imply.

4. Mark Abbett proposed a more formal and aggressive approach to technical employee development. The focus is on technical courses of many types. Mark will proceed with the plan and has the support of OOD.

5. Prof. Hall came in to discuss low enrollment in the on-site WPI Graduate EE program. It was obvious we are not getting to the potential students with a strong message. Bob and Dick will focus on the program via their staff meetings. Mark will insure we get material sent to the eligible engineers.

RC:mjk

SUBJ: IMpLEMENTATION LANGUAGE DATE: 06-17-75
FROM: GORDON BELL
EX: 2236
MS: ML12-1/A51

TO: FILE

SUBJ: IMPLEMENTATION LANGUAGE STRATEGY QUESTIONS

To: Distribution

Overall, I believe this report was very carefully done and hopefully represents the right direction. The alternative plans and costs seem particularly nicely done. It represents a great change in our attitudes from over 3 years ago, and I'm sad that it takes so long...particularly to adopt a structured assembly language. As a matter of policy, can you look into assuming hand PASCAL-to-SAL compilation so that we start (now!) to go this way?

I do have some questions that probably need to be answered before proceeding full blast with PASCAL-SAL, as opposed to BLISS-SAL.

Did you (or why did you) place high priority on portability? Doesn't this mean that our systems can be carried easily to an HP3000 or any other vendor quickly and provide a path for companies that don't have much (e.g. MODCOMP and INTERDATA)?

With such strong emphasis on machine independence, would we be better to make a PASCAL machine? Did you assume execution to be distributed like:

1. In the Operating System and utilities (20-40%).

2. As a compiler to write system and other applications (0 to 20%).

3. Other compilers (up to 1/2 of user time in some environments <25%).

4. Application run time compiled or interpretive code (25% to 50%)--what are you assuming are to be run in PASCAL?

Is PASCAL so high level that the machine doesn't matter--why not APL?

For that matter, what were the rankings you used for the

criteria? Why do we want another language in the field to sell? Do we make money now on languages?

In this case you have a well-defined alternative (i.e. BLISS) against which you're comparing a well-defined name PASCAL together with lots of ambiguous additions. When you get through, is it possible that your PASCAL language will bear the same relationship to worth as the RSTS language has to BASIC? In making these changes to have it be an IL is it possible you come nearly full circle to re-invent BLISS? Is it PASCAL+?

I really felt cheated in not being able to understand your decision. While we're only mid-way in the 11VAX design, we spend much effort in formulating goals and constraints and then measuring alternatives against these to select a particular design. Only the goals and constraints have been published, but I can show you some of the backup. But you should get some idea in looking at it as to why we're where we are.

What I really feel has to be done now to make our implementers feel comfortable is to put down a fairly complete list of criteria (say 10 groups with 10 items/group) that an implementation language must do (e.g. sense and set i/o words). I really don't understand the needs here of an IL and in comparing PASCAL and BLISS, I would rather program in PASCAL, but I don't write any systems programs, nor care about size, runtime, or data structures. With the error predicates for routines, could you eliminate so much of the type checking that PASCAL has (size and run time)? Hence, does one care that PASCAL checks? Don't you want it not to in production? It's hard for me to imagine that a language designed for gp student use has much relationship to a production, machine-oriented IL? Could you be more specific in quantifying the algorithms types that IL's deal with so as to get a better handle on the needs? As the developer of a set of modules (RTM's alias PDP-16), which were ideal for teaching and prototype building, they turned out to be unused in production environment (cost and speed were the issues...not design time). All your positive quotes from academicians in support of PASCAL tended to scare me about PASCAL as an IL. Don't you think there is a risk here?

Very often these languages (and machines) are hard to quantify and what usually clenches matters are benchmarks. Since we have so much BLISS code, I'd like to see some PASCAL code for comparison. What does it look like? How do you express a certain type of activity. Can you select, say 6, typical benchmarks and compare them? E.g., can it handle our

11VAX page table structures where bits are packed in every which way with pointers, etc.? Will Dave Cutler use it for the Operating System?

By stating your goals and constraints, it gets you really deep into the extensions of PASCAL. You (I or anybody) can then place our own weightings on these criteria and the others (e.g. $, time, training) such that its obvious why you chose PASCAL. Right now as a pure, simple, manager, my weightings tend to be on $ and short-term; thus BLISS might have been my choice, given only the data in your recommendation. When can I see some benchmarks, IL criteria, and weightings?

GB:mjk

Distribution

Ed Fauvre
Bill Slack

cc:

VAXA	Rick Grove	Bill Schauweker
Jim Bell	Glenn Lupton	Mike Spier
Bert Bruce	Jim Mills	Larry Wade
Dick Clayton	George Poonen	Peter Christy
Bill Demmer	Larry Portner	Dave Cutler

D I G I T A L INTEROFFICE MEMORANDUM C1561

SUBJ: A QUIET TERMINAL

DATE: 06-17-75
FROM: GORDON BELL
EX: 2236
MS: ML12-1/A51

* *

TO: FILE

* *

To: Joe Bitto
Ed Coreil

Please accept my heartiest thanks for getting the LA36 to the point where it is useable by normal mortals with regular hearing capability by reducing its noise level to below typewriter level. It's refreshing to now have an example (benchmark) for future designs.

I'm really anxious to get the APL version in order and trade-in my LA30.

GB:mjk

cc: Dick Clayton, Al Huefner, Andy Knowles, Ken Olsen, Bob Puffer
Ed Stelzer

D I G I T A L INTEROFFICE MEMORANDUM

C1564

PAGE 1

SUBJ: PDP-11 USE

DATE: 06-03-75
FROM: GORDON BELL
EX: 2236
MS: ML12-1/A51

TO: FILE

To: Distribution

With increased emphasis on future 11 development oriented toward the types of activities we do in engineering, i.e. computation, text processing, laboratory automation, data processing, I believe we (engineering) should make significantly more use of the PDP-11. Currently we use 10's for most of these activities. It appears this falls in your area(s).

Can you get together and propose how this might be done? Who's to do it?

Some of the questions I have about such an organization:

1. How will you network it, so that we can still access 10's for large jobs, and the specialized languages (e.g. ALGOL, APL, COBOL, some simulation languages, statistical packages)?

2. Should we use large ones centralized, or should we use 40-class and distribute them physically along the lines HP is advocating?

3. What would they do? Clearly all text processing, small engineering computation, some DBM, COBOL, all 11 programming development (they do now).

4. What operating system(s) will be useable?--RSX-11/D-IAS, MIAS (RSX-11/M version), RSTS, MUMPS, RT-11 for laboratory-type.

GB:mjk

Distribution

Leo Bennett
Don Crowther
Arnie Goldfein
Ron Rutledge
Phil Tays

cc: OOD, MC, John Leng

SUBJ: SPACE PLANNING REQUESTS

DATE: 06-03-75
FROM: GORDON BELL
EX: 2236
MS: ML12-1/A51

TO: FILE

To: Dick Clayton
Larry Portner

cc: OOD, Ed Wright

I've been holding up space planning requests by Ed Wright for 1 larger computer room + 1 large building for programming until you come up with the "systems" plan. While I don't know what you'll decide, I've developed some biasses (especially since my VAXA group is largely from programming):

1. Programmers are bright, and have a lot to offer the traditional hardware developers who only worry about processors and low level controllers. The system manager will be responsible for support of devices up to a standard, internal operating system interface--diagnostics and handler. Thus, these programmers should cohabit the space with hardware engineers.

2. Delagi has suggested (and started to demonstrate) that combining total systems development together is quite effective. His "team" is really Gourd, Hughes, a marketer, plus an architect. They have produced the best system results I've seen at DEC to date.

3. Ed has proposed a single, central computer room. I'd prefer to have several large rooms: 1-1 (for DA 10's), 3-5 and 5-5 which are located for open use and jam packed with machines. These would be associated with certain systems groups and there might be one for central groups e.g. languages (why can't the programmers have quiet, low power video terminals (VT52) with copier in their offices?) The purpose would be to make use convenient, close and quiet. Where possible, since power is decreasing, let's put small machines in offices (e.g. LSI-11).

4. The groups that might be co-located (note--no organizational changes):

   A. LSI-11 + RT + diagnostics for Q-bus.

SUBJ: SPACE PLANNING REQUESTS

DATE: 06-03-75
FROM: GORDON BELL

B. 11VAX high end + diagnostics + operating system design.

C. PDQ/11/70 would include RSX's.

D. 11/04; B05 would only include diagnostics and any other support to get them to run existing Operating Systems for their markets..largely iron.

E. PDP-8 would be fully integrated.

F. Communications + peripherals (tape, disk, printer) would be responsible for device level driver interface + diagnostics. This is mandatory as we evolve toward much smarter peripherals with programs in them.

G. Terminals (LA + VT) must have software help!

H. All applications would live with their respective PL's.

I. Manufacturing programming would be with their counter-part.

J. RSTS and languages would be central (Bldg. 3?).

K. Planning and general management would locate on 12-3.

L. Tools, plus common techniques, research, Bldg. 3.

What youse think? When or should we get at this?

GB:mjk

01567

digital

June 3, 1975

Bill Broadley
Computer Science Department
Carnegie-Mellon University
Pittsburgh, Pennsylvania 15213

Dear Bill:

I've been talking with Prof. Siewiorek regarding your manufacturing of the CMU-DEC microstore for the 11/40. NRL would like to obtain several of these, and since I feel their work is so important, it is imperative that the microstore be available to them.

At this time we, DEC, have no plans for the manufacture of this unit. Therefore, I would like to encourage you to manufacture the microstore and offer it for sale to NRL. In the future, if we become interested in the manufacture of the microstore, I would like to get the documentation so that it could be built here. But, in general, this would not preclude your continued manufacture of the unit.

If there's anything I can do to help, please let me know. I hope NRL can get the unit as soon as possible.

Sincerely,

Gordon Bell

Gordon Bell
Vice President
Office of Development

GB:mjk

cc: John Mucci--DEC
Roy Van Duesen--DEC
Charles Eichenlaub--DEC
Dr. Y. S. Wu--NRL Code 5490, Navy Research Lab, Wash. DC 20375
John Holman--DEC

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C1568

digital

June 3, 1975

Robert A. Stratton
President
Stratton Associates
4234 Matilija Avenue
Sherman Oaks, California

Dear Bob:

Thanks for the interest in Brian Warner. Some of our people talked to him and didn't find a match. I'm sorry I didn't meet him since you regard him so highly.

If other people, who may be somewhat controversial, come here, I'd appreciate meeting them.

Sincerely,

Gordon Bell
Vice President
Office of Development

GB:mjk

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C1569

digital

June 3, 1975

Susan Huhn
Election Process Consultants
38 Ridgewood Avenue
Groton, Massachusetts 01450

Dear Ms. Huhn:

As a product developer, your product sounds interesting, unique and important. However, I'm not really involved with products that are so "end-user" oriented, as I'm just involved with the building of our basic computers.

Since we really aren't segmented yet into a market structure which includes government, per se, it's not clear who would be responsible for working with you. I'm sending your material to Mr. Bill Long, who is in charge of our Original Equipment Manufacturer (OEM) product lines. I would believe you should base your product around one of our computers. If you're interested in pursuing this, let me urge you to contact Bill.

Sincerely,

Gordon Bell
Vice President
Office of Development

GB:mjk

cc: Bill Long
Stan Olsen

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D I G I T A L INTEROFFICE MEMORANDUM C1570

PAGE 1

SUBJ: SERIAL TYPEWRITER DATE: 06-02-75
FROM: GORDON BELL
EX: 2236
MS: ML12/A51

TO: FILE

SUBJ: HIGH QUALITY TYPEWRITER FOR WORD PROCESSING SYSTEM SHOULD BE SERIAL

To: Distribution

I would hope you make a cursory examination of using a serial interface instead of the parallel one to pDP-8 by getting the design operating! I believe it gets you many advantages and with probably less cost. It would use the existing MPS modules (an Intel 8008); hence, there would be NO hardware to develop since the series already has parallel interfaces, COMM I/O, etc.

The advantages, as I see them:

1. Quicker development time. Mark & Roy, could you help here to show that it can be done in less than a week?

2. The terminal could go on other computers...we currently buy a fair number for internal use, and I'm sure our customers wouldn't mind being offered a higher quality printer someday.

3. It can do self test...a real benefit since the thing is probably going to break a lot.

4. Easier to have redundant and multiple ones.

5. Easy to remote.

6. I believe it provides a better system design by functionally partitioning the system.

7. It lightens load on 8A--although this may not be important.

8. Can use it off-line at same time data system 310 is doing something else.

9. We'll end up doing it anyway eventually, so let's do it right the first time.

GB:mjk

SUBJ: SERIAL TYPEWRITER

DATE: 06-02-75
FROM: GORDON BELL

Distribution

Ed Corell	Jack Gilmore	Dick Kalin
Roy Moffa	Mark Sebern	

cc: Bob Puffer

C1572

D I G I T A L INTEROFFICE MEMORANDUM

SUBJ: PMS STRUCTURE POLICY

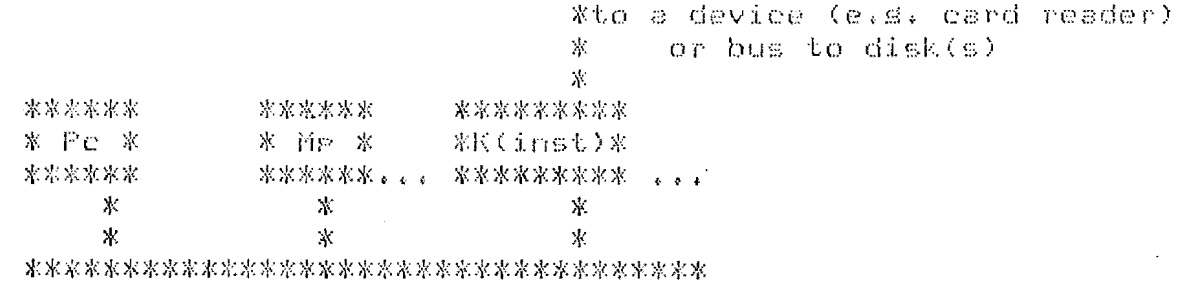
DATE: 06-02-75
FROM: GORDON BELL
EX: 2236
MS: ML12/A51

TO: DISTRIBUTION--VAXB XXX

SUBJ: INTER-PMS COMPONENT TRANSFERS ON DEC COMPUTERS:
RATIONALE, EVOLUTION AND RECOMMENDATION FOR A POLICY

This memo describes the philosophy that has been used for controlling the transmission of data among the various components within a computer (and especially at DEC). The method has remained relatively constant for about 15 years. As technology has changed recently to offer low cost, fast read only memories, it is time to update the position. We are to the point where nearly all controllers for larger devices can include their own computer which can interpret a program and have the capability of at least current device drivers. This memo will describe the past philosophy and posit what I believe is the right way to do in future systems. Recommendations will be given first, followed by the problem, and the alternatives that determine the solution framework.

Given the current, 1 central processor UNIBUS system with primary memory modules, and simple controllers, K's for devices; a controller K, may directly transfer data to Mp or it may interrupt Pc. Pc can communicate with K for data and/or control information.



Recommendations (the solution)

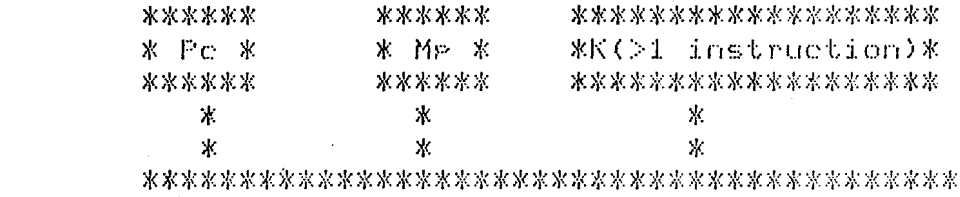
0. Define an IO process level interface which is at least as capable as current I/O drivers. Current hardware engineering would be responsible for developing systems and diagnostics to this level. Implementation would be by any of the techniques listed below ranging from totally programmed as with our current systems to separated IO computers with

SUBJ: PMS STRUCTURE POLICY

DATE: 06-02-75
FROM: GORDON BELL

their own microcode programs.

1. Adequate instruction buffering in K. We must add sufficient command buffering in each K, such that a device can operate at its full speed (subject to poor payoff from a cost/performance viewpoint).



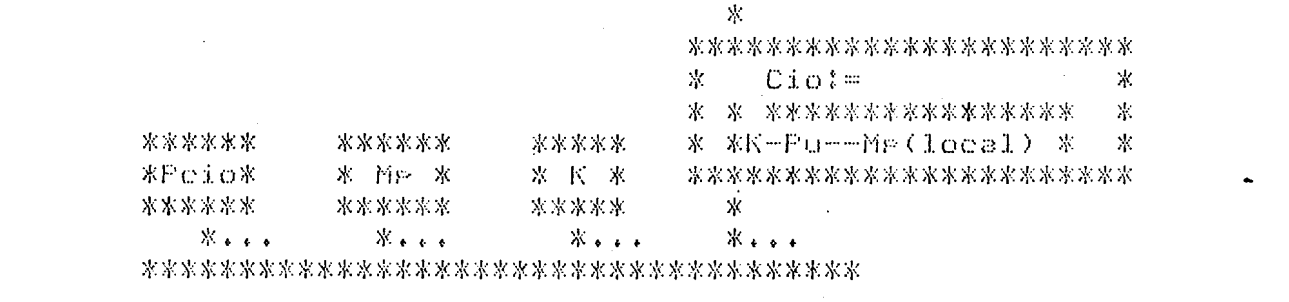
2. 1 instruction interrupt in Pc plus better I/O instructions--Pcio. We can, by a small change to current interrupt vectors, permit a single block-oriented data transfer instruction to be executed at interrupt time. The additional instructions we need are:

   A. Block I/O, Byte/Word, IO-device-address, Word-count and transfer-address. Input/Output a byte/word according to a control word which has a word-count and transfer address. At termination of block, cause a conventional interrupt.

   B. Decrement a word in memory and interrupt IO.

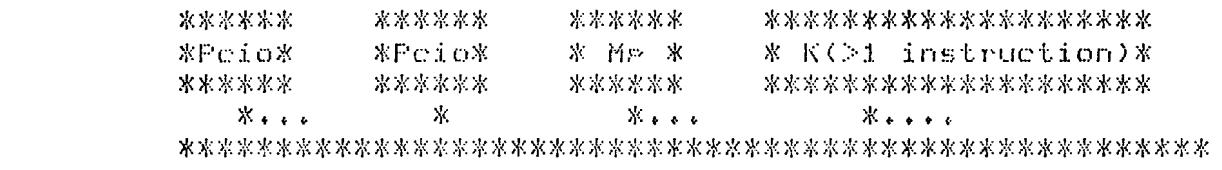
   C. Block I/O with character translation. The communications soup should specify the operation.r

3. Add a fully programmed microprocessor Pu with its local primary memory, Mp (local), which forms a small, fast stored program computer, Cio. Cio is connected to a control, K, or is part of a control K. With this scheme, IO processes will correspond to at least the current IO device driver level. In essence, Cio will operate on a data structure specifying a Job(s) to be done. The program in Cio is fixed. We are currently building controllers of this type for communications.



4. Examine the feasibility of using the small, Cio's, i.e. Demons, on the UNIBUS generally for specific control purposes (e.g. disk management, communications).

5. A multiple processor structure to increase reliability and performance.



Notice, the complexity is bounded; we have come full circle, once a Cio is formed. A Cio is precisely a second computer just like the starting point of the most primitive computer (i.e. K simple-Pc), but it is split apart for the sole purpose of I/O task management.

The Overall Problem

A computer consists of a number of PMS components and the design task is to interconnect them in a "cost/effective" way. This implies:

1. there is a physical structure that permits information to be transmitted among them. The UNIBUS is the most general way.

2. A process (program) in the computer system has to tell the various components that the transfer must take place... i.e. control.

3. According to good engineering principles, the system should be cost-effective:

   A. the cost of the transfer, in terms of the resources it uses, must be small.

   B. The overall system cost must be small. This can best be accomplished by leaving out components.

4. The overall throughput must be high, which in the case of I/O means greatest concurrency (parallelism).

5. The devices must operate at their own speed unless this cost does not increase the cost/effectiveness.

6. In some applications, it is important to have a minimal time between when an event is signalled until when a response is given by the program. (This also gives high throughput.) This, in effect, minimizes the interrupt response time.

Controls (K), processors (P), and computers (C)

A control (K) is the simplest form of finite state machine. It is given an input (1 or more instructions), it executes them and stops. In our systems, a control is given 1 instruction at a time by a processor (Pc), it executes the instruction (e.g. move a disk arm, print a character, transfer a block of data on Ms.disk to Mp).

A processor (Pc) picks up its own instructions from a list in a primary (program) memory (Mp). It has a program counter, which points to the instruction it is executing (or going to execute). The act of fetching and executing instructions is program interpretation. Thus to give a task to a processor to execute, requires giving it a program...i.e. specifying "how to do it."

A computer (C) is a Pc-Mp pair with a program(s). In the case of Cio, specifying a task requires giving Cio tabular information (data-structure) about the task...i.e. specifying "what to do", not "how to do it." The assumption is that a program in Cio "knows" about the data structure and knows how with not being told.

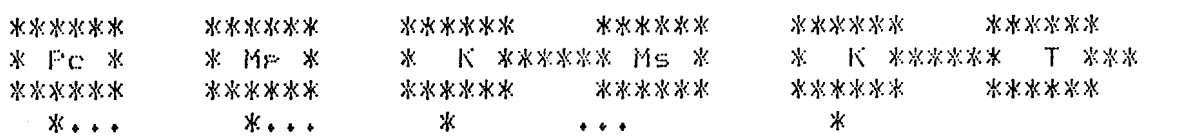
Pio and Cio are analogous to a procedure-oriented and a report generator-type program language (e.g. COBOL and RPG). In the former, tasks are specified by lists of instructions to carry out the task. The later accepts a template of the result (report) and then proceeds to achieve the goal by extracting the appropriate information from the data.

The Physical Structure Problem

The UNIBUS is the most general interconnection scheme to interconnect PMS components because it permits any device to communicate with any other. It is an obvious solution once the problem is formulated in its most general form.

The general structure is:

SUBJ: PMS STRUCTURE POLICY DATE: 06-02-75
FROM: GORDON BELL



There are several kinds of traffic which the UNIBUS (or any other bus structure) carries:

1. Central processors (Pc) to primary (program) memory (Mp)--in a stored program as the processes are being executed, each processor must access its program and data.

2. Primary memory (Mp) to secondary memory (ms), e.g. disk, via controller (K). In nearly all computers even beginning with Whirlwind, programs exceeded Mp size that Pc could execute from. It is necessary to move programs and/or data between secondary (backing) memory, Ms, and primary memory (Mp).

3. Non-memory transducers (T), e.g. typewriters, communicate with a program.

4. General control to cause transfers (2 and 3) and generally synchronize with them.

Historical Solutions to the Physical Structure and Control Problem in Terms of Processors

There has been an evolution in structure and in the way initiation and synchronization have taken place with Pc. This has been governed by technology, and has followed this path:

1. Very simple controllers (K's). With the processor stopping to help control each transfer. This also simplifies programming because everything is sequential.

2. Adding interrupts, and more complexity to each control (K) so that it could proceed in parallel with competitive interrupts were "invented" to synchronize completion with the processor without requiring Pc to wait or poll.

3. direct memory transmission (DMA-NPR) of information between Mp and Ms (or other device which require very high data rate transfers.

SUBJ: PMS STRUCTURE POLICY

DATE: 06-02-75
FROM: GORDON BELL

4. The addition of an io processor, Pio (IBMese=channel) which executes a stored program. Pio has instructions to initiate the controllers, and nominally spends its time passing data from the controller it initiates to Mp. at the completion of data block transmission, it fetches another instruction from its own program. I've been traditionally against this approach because:

A. It is most costly. (The initial channels on the IBM 7090 were really bad, because they were non-multiplexed; hence only 1 device (e.g. a 150 lin/min) printer could run at a time. The 360 selector channels are just as bad.

B. They add logical and physical complexity without much payoff. The controller is doing the real work, because of device idiosyncrasies, and all Pio does is buffer and pass data from a control to the memory...something that a buffer and wire will also do reliably and cheaply.

C. As a somewhat (not terribly) intelligent device, they require more communication because they are somewhat smarter than a dumb controller (notice the nice analogy with people). They must be told how to do a job.

D. Since a Pio has the same complexity as the central processor, one might as well use just the central processor. The central processor is the cheapest device in the system because it is already there, and the only time that Pc is expensive to use is when its at full load (i.e. there is no spare capacity).

However, when this happens, the nicest alternative is to merely add a second central processor to do the IO task (and any other tasks). Note the cost is no worse than in the case where we required both an arithmetic and IO processor.

E. There is system cost to have another component type which has to be stocked, diagnosed and programmed. The central processor has to have a program waiting for the IO processor, or has to compile one, or insert one in the Pio's table structure.

Note that when all the work has been done by the central processor, the only remaining work is actually handing the commands to the traditional, low level controller.

One should ask, why have a complex middle-man to which you hand commands, that merely hands commands off to someone else. Why not have Pc just hand commands to K when they're generated? It's clear to me since each small set of commands (a channel program) generates an interrupt back to the CPU, nothing has been gained since the Pc does the same (or slightly more work)...

5. The IO computer Cio. This has been used effectively by CDC in the 6600-7600 series, and we have done this to a certain extent in the PDP-10 and in large PDP-11's where a certain high level function is being performed by a totally separate program and complete process. The control activity is in Cio's memory, and it is told what to do--i.e. transfer a block, not how to do it (e.g. move arm + search + transfer + check).

6. Single instruction execution interrupt level. Improved instructions in Pc to handle IO transmission. This was done in the PDP-10 and in PDP-8 for communications I/O, such that instead of executing a program at interrupt time, a single instruction is executed. This slipped by in the initial implementation of the 11 and should be included at this time. Themost conventional use is to interrupt, and then execute a single Block Transfer In/Out instruction. The instruction transfers one word under control of a word count, and location pointer in memory. It has been used extensively byour competitors--the most notable has been Interdata, who added instructions to input characters from communications lines and perform translation, and store them in memory.

7. Specialized processors which interpret programs for a particular task. The GT40 is a good example of this. Because the instruction-rate is high, a complete processor is required. A typical instruction draws a character or line, or manipulates a list data structure defining the picture.

Evolution of Controllers (K)

While the above section discussed the evolution of the concept, and location of control, device controllers have varied considerably. Controller complexity has been influenced by technology, thus "control" can be distributed among hardware in a processor, a processor and a program, a specialized processor, or completely in an autonomous controller.

SUBJ: PMS STRUCTURE POLICY DATE: 06-02-75
FROM: GORDON BELL

Our controllers have evolved to the execution of single instruction (e.g. find a disk block, transfer a block from disk to a block in memory, output a character on a given LA36). I believe that controllers have and will evolve along the following lines:

1. K(simple). Simplest control where the CPU or a program handles most of the device control. In essence, all that K has are buffers to staticize information and convert signal levels according to the device's needs. Input converters sense the device's output and read them into another part of C.

2. K(instruction) Current controllers can execute a complete instruction on a data type that is known to the device being controlled (a character on the LA36, a line on a line printer, or a block on a disk or tape).

3. K(>-1 instruction) Current controllers but with sufficient command buffering (>1 instruction) such that the devices will operate continuously. We may have been minimizing controllers to the extent that system performance is degraded. For example, since a disk is usually the limiting component, and we use alternate blocks, the transfer rate is limited to be 1/2 the maximum, or conversely, the throughput is down by a factor of 2.

4. K's formed as K-Pu-Mp(local). This corresponds to at least the device driver level task. In this case, a special IO computer, is formed by a microprogrammed processor, Pu, which has a local primary read-only memory. In having a program, there are several possible uses of the increased complexity:

   A. The control program formerly in Pc-Mp or Pio-Mp can be located in Mp (local).

   B. K is told what to do, not hw to do it--it knows by interpretting its own program in Mp(local).

   C. The control program can diagnose the device.

   D. The control program can fetch a data structure (task) from Mp (global), and manage buffers, do error control, etc.

   E. More optimization of device control (e.g. disk transfers based on min. latency via a queue of jobs).

SUBJ: PMS STRUCTURE POLICY

DATE: 06-02-75
FROM: GORDON BELL

The dimensions of control choices evolves alons these lines for a controller (K) and the corresponding control in the processor (P).

*	K simple	*	* Pc (with embedded K)
*	K (instruction)	*	+ * Pc (interrupts + I/O programs)
*	K (>1 instruc)	*	* Pcio (1 instruction at interrupt)
*	K-Pu-Mp(local)	*	* Multi-Pcio
	(note equivalent		* Pio (e.s. channels0
	to K simple +		* P special
	Cio)		* Cio (separated computer with local Mp for I/O process control

GB:mjk [6/2/75]

C1581

digital

INTEROFFICE MEMORANDUM

LOC/MAIL STOP

TO: Jim Bell
OOD
Finance Committee

DATE: July 14, 1975
FROM: Gordon Bell
DEPT: OOD
EXT: 2236
LOC/MAIL STOP: ML12/A51

CC: John Fisher, Ken Olsen

SUBJ: HONORARIA--ATTACHED POLICY

The OOD is in the process of approving the following policy having to do with honoraria for talks. I just got a note from Ed Schwartz requesting officers and employees to list boards they're on, which presumably is covered in a policy somewhere.

Last year, I billed CMU for visiting and consulting CMU at $2,000 for joint DEC-CMU, CMU, and some profession-related projects. This year I made four trips and spent a total of approximately one hundred hours (2% of my professional time), much of which was on the phone and computer via the network. My intent was to turn this money over to DEC.

The problem: is my CMU affiliation like honoraria or a board fee? Are board fees turned over to the company?

There are clear cases where DEC doesn't get reimbursed, e.g., teaching classes after hours. Can F&A establish guidelines for everybody and rule on this by issuing the attached policy on some revised, appropriate form?

GB:mjk

Attachment

C1582

digital JUL 1975

INTEROFFICE MEMORANDUM

TO: Gordon Bell LOC/MAIL STOP ML12/A51

DATE: July 9, 1975
FROM: Jim Bell
DEPT: R & D Group
EXT: 2764
LOC/MAIL STOP: ML3-4/E41

SUBJ: Honoraria

Attached is the revised draft of the policy on Honoraria. Since there are still some open issues I will wait until I hear from you before proceeding further.

As we discussed on the phone the key open issues are:

1) should honoraria disbursements be centralized for better record keeping and control?

2) should incoming honoraria always be accepted, even from non-profit institutions, thereby serving

   a) as a control on the number of invitations,

   b) as a small source of income for the company, and

   c) as a counter balance to outgoing honoraria?

3) how do we distinguish between talks which DEC people give on their own (evenings, weekends, vacation days) and those talks given by DEC people as representatives of DEC.

JB/cw

C1583

digital

INTEROFFICE MEMORANDUM

TO. Hardware Engineering Managers
Software Engineering Managers
LOC/MAIL STOP

DATE. June 27, 1975
FROM. Jim Bell/Gordon Bell
DEPT. R & D Group
EXT. 2764
LOC/MAIL STOP. ML3-4/E41

SUBJ. Policy--Honoraria for Invited Speakers to Engineering Seminars

Background: The academic community has the custom of providing honoraria for invited talks when faculty members speak at other institutions.

DEC employees are offered honoraria for giving talks and participating in conferences at non-profit institutions, the government, and other companies.

Purpose: To establish a uniform policy within DEC with regard to giving and accepting honoraria.

Policy:

1) When a university faculty member is invited to give a seminar at DEC, it shall be customary to provide an honorarium in addition to expenses. The size of the standard honorarium shall be set by the Vice-President of Engineering; it is currently set at a maximum of $150.00, the exact amount to be based on the time and effort involved, and set by the person who issues the invitation.

2) When a DEC employee is offered an honorarium, the employee shall (a) decline it when offered by a university or other non-profit institution and (b) accept it on behalf of DEC otherwise.

3) The responsibility for enforcing this policy, providing outgoing honoraria, and accepting incoming honoraria shall rest with each cost center manager.

JB/GB/cw

C1584

0062 1302 30-JUL 36124 1300 30-JUL
MP30 LPTR RDGB
ZCZC
RD

MSG NO NA14

TO GEOFF SHINGLES READING ENGLAND

FOLLOWING IS A COPY OF THE LETTER I SENT TO PROFESSOR SHACKEL

"THANK YOU FOR YOUR LETTER REQUESTING FUNDING OF THE
NATO ADVANCED STUDY INSTITUTE. WE BELIEVE THIS IS IMPORTANT
BUT DO NOT HAVE FUNDS TO SUPPORT IT NOW.

IT IS POSSIBLE THAT DEC UK MIGHT HAVE SUPPORT FUNDS, AND I WOULD
ENCOURAGE YOU TO CONTACT THEM THROUGH YOUR LOCAL DEC CUSTOMER
SALE ENGINEER. BUT IN VIEW OF THE LATE DATE, I WOULD BE
CONCERNED THAT THEY TO ARE IN A FINANCIAL BIND.

REGARDS
CC GEOFF SHINGLES"

DEB

FROM GORDON BELL MAYNARD
NNNNN

D I G I T A L INTEROFFICE MEMORANDUM C1585

SUBJ: VAX ARCHITECTURE (HRDWR/SOFTWR)

DATE: 07-28-75
FROM: GORDON BELL
EX: 2236
MS: ML12/A51

TO: FILE

We have produced much documentation on the hardware architecture. Enough so that implementers can start to work so that we can interact with them. The software architecture is marked with great gobs of milling inactivity. The hardware architecture is described in terms of surrounding goals, constraints, and the technology environment for the 1975-1985 time scale. Most of the instruction set is completed and encoded, and the virtual addressing use and mechanism, though designed, is about 2 weeks away from description for review. We held our first corporate-wide (35 people for 3/4 day) design review (hearing).

So far, we appear to get a 1/3 reduction in code size and running time as compared with a comparable PDP-10 and 40% to 50% reduction over a PDP-11 for FORTRAN, while giving the user 29-bits of memory address space. While these measures are relatively spectacular for an Instruction-set, note that if we didn't build the machine, and used a PDP-10 instead, technology evolution would give us the same gain 2 years delayed.

As an architect, I'm helping provide the best 11 follow-on machine that is similar to an 11 so that a user recognizes it as such.

As a business person, I'm terrified at the amount we'll spend in getting a 3rd machine to support beyond 10 and 11--also the risk is enormous. The 11 software support is thin and this will further stress it.

As a user, I doubt if I'll turn in my PDP-10 account # for a a number of years. ALGOL, APL, BASIC+, COBOL, DBMS,...SIMULA plus lots of applications are most important to me and I don't see 8-bits versus 9-bits, or any OP-code at all except a language's. We're dead if I'm anywhere near a typical user who just wants to get work done and not bit hack.

As head of development, I see 4 years of sheer hell ahead for us all, and I expect super-human support.

GB:mjk

D I G I T A L INTEROFFICE MEMORANDUM

C1586

SUBJ: DG IN BUSINESS

DATE: 07-30-75
FROM: GORDON BELL
EX: 2236
MS: ML12-1/A51

TO: FILE

To: Irwin Jacobs, Larry Portner

CC: MC, OOD, John Fisher

We're getting strong signals that DG is:

1. Becoming aggressive in business market place--they have RPG.

2. Working on a full COBOL.

3. Working on a PL/1.

4. Working on a database language.

Do we have right strategy vis a vis our home brew languages: DIBOL, BASIC, and minimal COBOL?

GB:mjk

7/28/75

C1589

COMMENTARY ON YELLOW BOOK

From: G. Bell

In order to make the Yellow Book more meaninsful, I would like to emphasize the quarterly ones with EVERYONE reportins. In readins the report, I've commented on various pases, and if you have comments to me or ideas, please feed them back to the author.

BUDGET: We were only .6% ($172k) over budset. Good work in spendins control.

PROJECT SCHEDULES: The budset control and poor time estimates, caused poor performance in meetins schedules. However, more major products are soins into production this year than ever before, comins up from last year's low. The performance of projects reported on the calender and sections 6 and 7:

MONTHS LATE
(CUM %)

Project Group	?	-1	0	1	2	3	4-6	7-9	10-12	>12
Calender	2	1 (3)	6 (24)	3 (34)	3 (44)	4 (58)	2 (65)	4 (79)	1 (84)	5 (100)
Sect. 6 (Hrdw.)	103	2 (7)	11 (45)	1 (48)	6 (69)	5 (86)	4 (100)			
Sect. 7 (Sftw.)	40		18 (46)	1 (49)	8 (69)	3 (77)	6 (92)	2 (97)	1 (100)	

Note, the disparity of reportins in the 3 areas (unless the calender is atypical). While I am happy that we are settins the products done, the fact that half of them are about a quarter late, with some soins beyond a year, sure must cause product and product line manasers a lot of srief.

Section 6 and 7 charts desisned to slean summary information are really awful (with a few exceptions). We started out with a form for everybody that would allow others (includins me) to find out what the status of the project and budsets were. The budset numbers are continually revised upwards to reflect the newly required funds to complete, and the completion dates are mostly non existent. The most important soal: cost is missins in nearly all cases!. On the next quarterly Yellow Book, I would like to set this straishtened out so all can see what's soins on in a project asainst its initial commitments.

In seneral, our culture is really forsivins of project slippase and budset overrun...siven that we set the product and it is a sood product. It even isnores cost soal misses. A late, uncompetitive product is unacceptable. I don't want to chanse the way we schedule, because it is optimistic, but I do want us to understand and track it.

I don't know who's responsible here, but the pink book manufacturing costs are generally abysmal. There is negative learning in some areas (e.g., RS04) and only 5% in others. We really should flush many of these products. Hopefully, this is due to recession and not working at full capacity (and full urgency). Core is especially serious; and its demise is hastened. Especially since innovation as in 32K is so long in coming.

We have, however, moved into higher volumes for terminals (LA and VT) with 90% and a committed 85% (how's it actually?) learning. Now, if we can work the pricing, we might make some money.

Some projects are of concern to me:

1. RK06--I believe we're all available to help here. What is needed? This is a serious problem as it is pivotal to all systems. The controller cost, maintainability, and MASSBUS interface problem should be cranked into plans.

2. Serial bus versus LSI-11 bus--Wouldn't we be better off using this instead of going to another computer bus for all our low speed peripherals.

3. VAX--SEE Delagi/Bell reports.

4. Use of both special MOS computers (INTEL 8080, Motorola 6800, etc.) and support of microprogrammed controllers. Lorrin Gale to focus direction.

5. General architecture of more intelligent controllers--who to focus (see also 4)?

6. Terminals--a plethora of really difficult problems--smart versus dumb; multidrop and block mode of what flavor; how do we support in software--especially smarter (non-programmable) kind?

7. LSI-11--BUS, phase-in to standard systems, use in packaged systems, and unacceptable ROI. Since we feel it is a good product this should be easy to solve. Also note we really learned much about semiconductors (probably more than we wanted to).

8. Worcester--Now that it got into our budget, can we get a plan?

9. CAD/IDEA/Pc Layout--I'm frightened enough to totally trust the developers. All I hear about our service areas are the bad stories. Better measures are needed. The groups being served are so intimidated (their service could get worse) they won't talk.

10. VT5X-6X. Much misunderstanding about market with my colleagues (and PL's). Hopefully the sales take off and we won't have to know why.

11. Multitude of Operating Systems--With VAX, thin support will get thinner.

digital

C1591

24 July 1975

Drs. Samuel H. Fuller & Daniel P. Siewiorek
Department of Computer Science
Carnegie-Mellon University
Pittsburgh, PA 15213

Dear Drs. Fuller and Siewiorek:

The decision to continue DEC support of the Multi-Micro-Computer Project to its second stage (30 module configuration) will depend on a joint review of the project by CMU and DEC following the demonstration of the 10 module configuration. At that time, a new letter of agreement will specify how CMU and DEC will cooperate, although there is an understanding that if the 10 module configuration works well, both CMU and DEC are interested in developing the 30 module configuration. Details of the actual configuration will depend on a joint CMU/DEC evaluation of the initial 10 module system.

Because of the long development time, high cost and risk, discussions involving the support of the final stage of this project (100 module system) will not be started at this time.

Gordon Bell

Steve Teicher

DIGITAL EQUIPMENT CORPORATION, 146 MAIN STREET, MAYNARD, MASSACHUSETTS 01754
(617)897-5111 TWX: 710-347-0212 TELEX: 94-8457

01592

July 24, 1975

Mr. N. B. Hannay, Vice President
Research and Patents
Bell Telephone Laboratories
600 Mountain Avenue
Murray Hill, New Jersey 07974

Dear Mr. Hannay:

As you may know, Bell Telephone Laboratories has installed numerous Digital Equipment Corporation (DEC) computers at its various facilities. These machines are used in research within Research and Patents, area 10. Also, we have machines in other parts of the laboratory, particularly those which eventually end up in the operating companies.

DEC's Laboratory Data Products group is responsible for developing and supporting those computer hardware and software products that are most particular to research. Recently, we have increased our personnel assigned to the laboratories to include a Laboratory Data Products (LDP) sales representative.

In order to better serve your researchers, and to aid in determining the kinds of products they need, the LDP group would like to conduct a series of seminars dealing with computer applications. Edward Kramer, Product Line Manager for the LDP group, Jack Kay, LDP sales representative, and I would like to meet briefly with you and your divisional directors (individually or as a group) in order to discuss the possible interaction.

Although I'm not as involved in products development or use as I'd like to be, I have enjoyed interaction with BTL researchers, (especially H. S. MacDonald), and I particularly value this interaction to guide our product direction. The Digital Filter is entering this area of possible application now, and I would like some interaction about possible applications as a means of pushing us harder.

DIGITAL EQUIPMENT CORPORATION, 146 MAIN STREET, MAYNARD, MASSACHUSETTS 01754
(617)897-5111 TWX: 710-347-0212 TELEX: 94-8457

To: Mr. Hannay
-2-

From: Gordon Bell
July 24, 1975

If you believe this is worthwhile, please let me know and we can set up a meeting at Murray Hill.

Sincerely yours,

DIGITAL EQUIPMENT CORPORATION

Gordon Bell

C. Gordon Bell
Vice President
Office of Development

CGB:mjk

cc: S. J. Buchsbaum
A. M. Clogston
D. Gillette
R. C. Prim
W. P. Slichter
V. H. Wolontis

Jack Kay
Ed Kramer

C1594

July 23, 1975

David M. Taylor
939 Washington Street
Holliston, Mass. 01746

Dear Mr. Taylor:

I got your resume. The "objectives" will be more helpful to us.

Do you have anything written which represents your skills as an analytical engineer--such as a standard, or a task force report, etc., in which you are the principal author?

Sincerely,

Gordon Bell
Vice President
Office of Development

GB:mjk

DIGITAL EQUIPMENT CORPORATION, 146 MAIN STREET, MAYNARD, MASSACHUSETTS 01754
(617)897-5111 TWX: 710 347-0212 TELEX: 94-8457

D I G I T A L INTEROFFICE MEMORANDUM

SUBJ: CORPORATE AUDITORIUM

DATE: 07-23-75
FROM: GORDON BELL
EX: 2236
MS: ML12-1/A51

TO: FILE

TO: OWNER OF CORPORATE AUDITORIUM (CLASSROOM)

The tiny blackboard and screen share the same physical space, hence, can't be simultaneously used. The room is poor for televising.

There are no tables when coffee arrives (or for sales meetings coffee and doughnuts).

There is no overhead projector built in (why not?) and the audio visual group has no projectors for use, nor do the people come to work early enough to check them out for an 8:15 or 8:30 meeting. Sales Training saved us.

There is a high intensity noise source near it (cafeteria) that occasionally runs, inhibiting hearing in rear... although for us the acoustics are not too bad.

The parking facilities are good for 8:15 and 8:30 meetings since the PK3 people aren't using them; it does not help engineering morale to visit PK-3.

The tables and chairs are nice, especially the chair bottoms.. which is what we usually concentrate on.

We need a large, good conference room/auditorium in the mill.

GB:mjk

cc: Ted Johnson
John Jones
Ken Olsen
Harold Trenouth
Craig Zamzow

digital

INTEROFFICE MEMORANDUM

LOC/MAIL STOP

TO: Distribution

DATE: July 21, 1975
FROM: Gordon Bell
DEPT: OOD
EXT: 2236
LOC/MAIL STOP: ML12/A51

C1596

SUBJ: PORTABLE BLISS

Now that we are building a BASIC PLUS on the 10 and 11, what's the chance of writing it in portable BLISS? I assume the 11 will be written this way, and the 10 is already written this way? Clearly, some is different (such as the run time and the system interaces), but much is the same: editor, parser, common user documentation, etc.

GB:mjk

Distribution
Norma Abel
Ron Ham
Irwin Jacobs
John Leng
Jim Mills
George Plowman
Larry Portner
Jon Singer

July 21, 1975

Michael W. Rohrbach
International Marketing Services
38 Garden Road
Wellesley, Massachusetts 02181

Dear Mr. Rohrbach:

I really appreciate the effort you spent in writing down and focusing on interface problems with DEC and our various product deficiencies. I'm distributing the letter now to solicit responses in some of the problem areas you mentioned.

For the particular questions:

1. Please contact Bill Kiesewetter regarding the DEC System 10.

2. Since I too don't understand the precise structure of the Commercial Group (it's being reorganized), I suggest you start with Stan Olsen, who is Group Vice President in charge of Commercial, Communications and Typesetting Product Lines.

It's unclear specifically how we might interface better, but it probably has to be through the sales or a marketing group. For now, I believe you might contact Mort Ruderman as a next step. Again, thanks for your input.

Sincerely,

Gordon Bell
Vice President
Office of Development

GB:mjk

cc: Bill Kiesewetter
Stan Olsen
Mort Ruderman

DIGITAL EQUIPMENT CORPORATION, 146 MAIN STREET, MAYNARD, MASSACHUSETTS 01754
(617)897-5111 TWX: 710-347-0212 TELEX: 94-8457

To: Jacobs, Marcus, Portner, Schroeder, Johnson, Pedersen, Long, Long

INTERNATIONAL MARKETING SERVICES
38 GARDEN ROAD
WELLESLEY, MASSACHUSETTS 02181

01598

July 16, 1975

This guy came to see me by mistake. Some probs are mine, but bulk seems to be Marketing/sales etc

Dr. Gordon Bell
Vice President of Engineering
Digital Equipment Corporation
146 Main St.
Maynard, MA 01754

Subject: Review of meeting with Dr. Gordon Bell and Larry Portner on July 2, 1975

Purpose:

To review observations of an outsider on how DEC looks and to relate the challenge that DEC presents in dealing with its organization. To present specific first hand and second hand information as to the difficulty of obtaining a cohesive picture of DEC's posture in the business systems area as it relates to systems above the DIBOL business system. To review in brief the position of the competition on how they are marketing and how they are addressing the same market segment.

Database: For the past several months, I have attempted to determine whether there is an established position on the question of database. To my frustration I have not found out if there is a position, who has made that position known, and if the position is known, how the forces are going about evaluating databases. I am aware that there are several vendors attempting to convince DEC that theirs is the best, but I have not gotten a definitive statement, such as was given in our meeting, that DEC will wait for several companies to come up with DBM's that run on the PDP 11 and let them market these along with DEC.

Although I have little doubt that DEC can build their own DBM package, I am not at all convinced that you can afford to frustrate companies who are sincerely trying to gain your interest in their offering. You let them grind through the mill and then do not give them either an answer, opinion or a feeling as to what decisions you are making. I also feel that when companies such as Computer Corporation of America (whom I presented to DEC for their Model 204 database package and user language) spend six years developing their system before aggressively taking it to market, there might be good reason to buy a database design. This is particularly the case when such a supplier has been a long standing DEC OEM, supplies lots of software to the ARPA network, and is under contract to work in the DECOM product line development. DEC may in fact be sincerely interested. The point is that after lots of searching, I have not been led to the right person. Others with less tenacity have understandably given up.

HELP

I owe him a letter. Can you help? I believe he sincerely Kids Wants to work with us.

COBOL under DOS: This was the first of the projects which was to materialize into a potential market for my company. This is the activity through which I met Al Brown and Computer Power Ltd. For several months I was feeding information both ways trying to get underway a final agreement that would permit the marketing of COBOL under DOS by an independent company without the support of DEC. We were simply looking to provide COBOL to the existing DOS or one foreground, one background partition DEC processor. We even got to the point where DEC made an internal market study to make sure that DEC did not want to market that product themselves. It was our intention to resurrect the DOS/COBOL version in existence in Australia and market it in such a way that it would indeed be a subset to the RSX COBOL. The clients could later upgrade to DEC's own RSC COBOL. After working at this for over six months, the entire subject was suddenly closed off. Worse than that, Roger Allen left the States under the impression that everything had been cleared. He wrote me from Australia that all signals were go. It was only because I checked again with Al Brown that I found out that DEC Australia had turned the whole thing off. It was truly an education. Unfortunately a great deal of time and energy was spent for nothing.

As for the subject matter involved here, I believe that nothing could have been more perfect for DEC than to have an alternative to DEC's own COBOL available in the market. Since all the competition has COBOL running on systems much smaller than the minimum which will be required under RSX, I believe that there were opportunities that will now fall to competing hardware. We might also have seen systems houses who are building PDP 11 systems as RJE stations, target systems under DOS that would have later been moved up to RSX.

Operating systems versus languages: From the view presented by DEC to the general or special systems house in the commercial market, one is always left with some rather difficult alternatives. BASIC is an excellent language for use in interactive commercial systems. The problem to date is that in order to have BASIC, there has to be RSTS. However, there isn't an RSTS small enough to compete with a system programmed in BASIC on a number of competing minimainframes. COBOL is the next alternative, but there is no DOS COBOL that could be sold as a minimal system. Under RSX 11D COBOL is large enough to support at least ISAM files (if not a query language) and database. DEC's smaller system coming in at the lower end of the market using DIBOL requires a re-education of the prospect. The systems house working with DEC's DIBOL cannot compete (nor even survive) against a month-to-month rental RPG system that has the same application already bundled into the monthly rent. Therefore, a systems house has to have a very versatile set of personnel merely to cover the offering DEC has in the product line.

From a DEC corporate point of view, each marketing group has its own axe to grind and, therefore, little unification can be anticipated. I found this reflected in the attitude that headquarter people working with RSTS care little about COBOL and those in "business systems" are not at all sympathetic to things like BASIC for the commercial client.

Worse yet, the potential client is faced with different sales people covering different interests. When the systems house takes along a DEC sales person, it is never certain what will finally come out of the conversation. You might pick the salesman you think is the right one and find that in the middle of the conversation, he will say something like "COBOL is for universities".

Competition by DEC: A specific situation was brought to my attention in the retail trade. A systems organization has developed and has installed a number of DEC PDP 11's in this market segment. In calling on one major account, they now find that DEC is competing with them. The group competing against them is the DECOM group which is trying to show that they are able to do the whole thing including the retail application. The systems house has both the communication and the application all worked out and their system has been in operation for three years.

Maybe worse than that was the fact that DEC came to this same systems house to look at some special software and hardware interfaces that were built to handle asynchronous signals on synchronous channels. After the visit, DEC never came back with so much as an answer as to what they thought or what the interest was.

In a local case, a systems house had gotten to the point of defining a working system which the client considered acceptable. This system was to be written in BASIC. The client asked the systems house to call in a number of hardware vendors to make a bid on the hardware. Instruction had been given to the hardware vendor as to what system had been specified. DEC responded by bringing in another system house with a proposal for DIBOL. Admittedly they were not given much of a chance to present their case, since they were way off base. It did destroy the opportunity to have DEC as a vendor with this client.

Sell "FUTURES": There is not a question in my mind that DEC had a great deal more to offer to the commercial market than its major competitor. By merely advertising more and giving lip service to INFOS, for instance, DG has placed itself out front in getting leads from the systems houses. Technical people are turned on by it. Whatever the reason, the lack of a

stated position with regard to a complete system in the mid-range between DIBOL and the DEC 10 is hurting DEC. Thus, DEC may not get a chance to retrain these system organizations later on to recommend DEC, even when the direction DEC wishes to take is finally made public.

Application package: In a specific case there is a COBOL based application package for the Life Insurance field. The supplier of the application would like to work with DEC on making the conversion to DEC. A client has been located who does not have a machine at the present time. IBM is making a recommendation to go to an in-house 370/135. By combining the client and the software there is reason to think that the client can be won over. Where does one start working through the DEC organization to get something like this started?

Government request for bid: An opportunity exists for DEC to help write a spec for a complete system to be installed in a government facility. The person writing the spec is not an ally of IBM and is intrigued by the possibility of a large PDP 11 or small DEC 10 being specified. How would one go about securing the right person in DEC to start on that project?

Data dictionary vs. Database: Several weeks ago, I had an opportunity to present a new slant on database to DEC. The case I presented was that of offering a data dictionary facility first, so that DEC might buy time to work on resolving th question of database. Admittedly this would not only be a delaying tactic, but would make DEC unique in offering the most logical approach to database. Despite the fact that I took two months to set up a presentation, I asked myself why I had bothered. I presented a product and many reasons why we have had such success with it. I believe it was a compelling story as did a member of your Corporate Information Systems staff. Unfortunately it got nowhere. As it turns out, even Corporate Information Systems would like to have this facility for in-house use, and even they don't know how to get the project started.

And yet, when all is said and done, the "IRON" is shipping out and that does help pay for all of this. It is gratifying to hear from long-time DEC users that the "IRON" works well. It works so well that in a recent system bidding, we proposed an 8A and suggested to the client not to buy the maintenance contract. We suggested taking a couple of extra boards instead. Although this is less possible in the electromechanical units, it does demonstrate how well things do work out there. Your ability to provide service in almost as many places as IBM certainly is a major factor in why larger and stronger systems houses do prefer to go with DEC.

What I have highlighted in these notes may just point out to you that

your policies are indeed being carried out. If that is not the case, I would like to have the opportunity to review some of these items with Mr. Olson or others you may suggest so that they may have more complete background information. I would be most intrigued with the idea of working with DEC on some of these items in either a consulting role or as a contractor with the support of DEC. Since I spend most of my time selling software and systems to the commercial marketplace occupied by IBM, there are a number of strong opportunities into which I would like to draw DEC. I would, however, like to know that I can count on complete support before embarking on any of these projects.

Please let me know how I should proceed. For your information, I have also enclosed a brief write-up on the activities of my company should that be necessary as introductory material to those whom I might meet.

Very truly yours,

Michael M. Rohrbach

MMR:sj
Encl

July 21, 1975

Mr. Eric Marshall
Marshall Design International Ltd.
Haughdell House
Park Road
Banstead, Surrey, SM7 3EL
England

Dear Mr. Marshall:

Mr. Olsen asked me to respond to your request to visit DEC. You're welcome to talk with our people directly regarding possible consultation. However, we buy very little or no outside consulting in this area, and currently no consultation in the U.K., although we manufacture in Ireland. Our European design and engineering effort is special systems and programming.

I've given your letter to Dick Schneider and Dave Nevela, who have much of the design responsibility for our products.

Sincerely,

Gordon Bell
Vice President
Office of Development

GB:mjk

cc: Dave Nevela
Ken Olsen
Dick Schneider

DIGITAL EQUIPMENT CORPORATION, 146 MAIN STREET, MAYNARD, MASSACHUSETTS 01754
(617)897-5111 TWX: 710-347-0212 TELEX: 94-8457

Dick Schneider ~~the~~ and Dave Nevele who ~~when you for any del~~ have much of the design responsibility for our products.

cc Ken, Nevele, Schneider

1694

JUL 18 1975
K-177

Marshall Design International Ltd. *Haughdell House, Park Rd, Banstead, Surrey, SM7 3EL Tel Burgh Heath 58091*

Kenneth H. Olsen, Esq.,
Chief Executive,
Digital Equipment Corporation,
146 Main Street,
Maynard,
Maryland, 01754, U.S.A.

1st July, 1975.

~~Are~~ and currently no consultation in the U.K. although we manufacture in Ireland.

Our European design and engineering ~~effort~~ is specialised in special systems and programming

Dear Mr. Olsen,

I would like to introduce to you my Company - Marshall Design International Limited - one of Europe's largest and most successful design organisations.

We specialise in the styling of consumer and industrial products and we have earned our reputation by designing for such major Companies as I. T. T., Hoover, Philips, Black & Decker, Plessey, Shellmex & B. P., Thorn Electrical Industries and Citroen.

Some people may argue against new designs or new products during the present business recession. We disagree totally - now is the time to plan new products, redesign existing lines - be ready to increase your profits, expand your market share as soon as the economy picks up - as it will.

I shall be touring the U.S. during the next few months and would welcome a meeting with you.

Yours sincerely,

Eric Marshall

ERIC MARSHALL

Mr. Olsen asked me to respond to your request to ~~visit~~ visit DEC.

July 21, 1975

Dr. Michael J. McKeown
Chairman, Computer Development Committee
North Bend Medical Center, Inc.
1920 McPherson Avenue
North Bend, Oregon 97459

Dear Dr. McKeown:

I'm not in charge of this area of the company, which develops and markets products into the medical profession.

Since it is unclear to me just which group would develop and/or market such a system, I have turned the material over to Mr. William Thompson, Secretary of the Marketing Committee. Our Marketing Committee consists of four senior vice presidents, responsible for the development and marketing of special applications; and they can decide the next step.

The proposal looks interesting, and I'm glad you're considering DEC.

Sincerely,

Gordon Bell
Vice President
Office of Development

GB:mjk

cc: Bill Thompson (+ material)
MC

North Bend Medical Center, Inc.

Physicians and Surgeons

1920 McPHERSON AVENUE
NORTH BEND, OREGON 97459
(503) 756-4171

General Medicine
CARL L. ALBERTSON, M.D.
ROBERT CHIAPUZIO, M.D. P.C.
WILLIAM W. COX, M.D. P.C.
ERNST GEIZER, M.D.
CHARLES H. LINDSAY, M.D.
ELMO W. PETERSON, M.D.
GAYLE R. WILSON, M.D.

Surgery
PHILIP J. KEIZER, M.D.
WILLIAM H. MASSEY, M.D.

Internal Medicine
RICHARD L. WEST, M.D.
DAVID R. WHITE, M.D.
DAVID S. GELKE, M.D.
PHYLLIS J. BROWN, M.D.

Pediatrics
WILLIAM P. KEAN, M.D.
JAMES F. MEANS, M.D.

Obstetrics and Gynecology
MICHAEL J. McKEOWN, M.D. P.C.
RALPH E. WHITING, M.D.

Administrative Manager
GARY L. MILLER

JUL 18 1975
7-19

July 14, 1975

Gordon Bell, Ph.D.
Vice President, Office of Development
Digital Equipment Corporation
146 Main Street
Maynard, Massachusetts 01754

Dear Doctor Bell:

We are asking you to consider a proposal for an automated business management system for medical clinics. The increasing complexity of this business will soon require such tools to run efficiently. Dr. George Wied of the University of Chicago has reviewed this proposal and suggested we write to you.

We have developed these specifications after considerable study. The current version utilized the resources of Boeing Computer Systems for publication.

We believe there are three unique management tools in this system which will give it increasing usefulness in the medical clinic business.

First, it enables the patient to have an accurate, up to the minute bill and statement of account at the end of any patient encounter/visit. Our experience with a manual approach to this concept supports our belief that this significantly increases immediate collection percentage and decreases age of accounts receivable. A group our size can thereby realize a significant improvement in cash position. Automation of this concept makes it even more cost effective.

Second, the detailed management information available facilitates timely management decisions. Negotiations with third party payers can be much more productive for the medical clinic if its management has the supporting statistics that our proposed system produces about billing and receipts on accounts. Effective negotiations in this area are becoming a matter of economic survival for medical clinics.

Third, the payment allocation system allows a unique distribution of income such that individual doctor income is clearly

identifiable. This allows a cooperative corporation approach to the business with individual doctors utilizing professional corporations, HR 10 plans, etc. This conglomeration of individual retirement plans and not one unified plan with all employees covered has significant tax and estate planning advantages which are of increasing interest to more sophisticated group medical practices.

We realize that some details of this specification are unique to North Bend Medical Center, Inc., but we would consider more generally applicable procedures if the costs of development were to be shared.

Thank you for considering this proposal. We would hope that cooperative development of a business system would be possible.

Cordially,

M. J. McKeown, M.D.

Michael J. McKeown, M.D.
Chairman, Computer Development Committee

MJM mks
encl

C1606

CURRICULUM VITAE

Michael J. McKeown, M.D.

SOCIAL SECURITY NO.: 544-40-6953

DATE OF BIRTH: December 13, 1935

PLACE OF BIRTH: Portland, Oregon

CITIZENSHIP: American

EARLY SCHOOLING: Coos Bay, Oregon, Marshfield Senior High School, 1950-1954

COLLEGES AND DEGREES: Dartmouth College, 1958 - B.A.
Harvard Medical School, 1961 - M.D.
Diplomate American Board of Obstetrics & Gynecology, 1969

PRESENT POSITIONS:

Assistant Clinical Professor of Obstetrics and Gynecology, University of Oregon Medical School.

Clinical Professor of Biomedical Technology, Southwestern Oregon Community College.

PREVIOUS POSITIONS:

Intern, The University of Chicago Clinics and Hospitals, 1961-1962.

United States Navy Medical Corps, 1962-1964.

Resident, the Chicago Lying-in Hospital, 1964-1967.

Teaching Assistant in Mathematical Biology, 320, 321, The University of Chicago, October, 1966.

Chief Resident and Instructor, Department of Obstetrics and Gynecology, The University of Chicago School of Medicine, 1967-1968.

Instructor in the Department of Obstetrics and Gynecology of the Pritzker School of Medicine of The University of Chicago, July 1, 1968 to April 1, 1970.

Consultant, Obstetrics & Gynecology, Chicago Board of Health, 1970-1972.

Assistant Professor in the Department of Obstetrics and Gynecology of the Pritzker School of Medicine of The University of Chicago, April 1, 1970 to July 1, 1972.

SOCIETIES:

Fellow of the American College of Obstetrics and Gynecology

Fellow of the American College of Surgeons

American Fertility Society

American Public Health Association

The Institute of Electrical and Electronics Engineers, Inc.

Association for Computing Machines, Inc.

American Statistical Association

Association for the Advancement of Medical Instrumentation

American Institute for Ultrasound in Medicine

Society for Computers in Medicine

American Association for the Advancement of Science

New York Academy of Sciences

American Federation for Clinical Research

International Scientific Society

Association for Health Records

Fellow of the Royal Society of Health

Royal Society of Medicine

National Association for State Information Systems

American Academy of Political and Social Sciences

BIBLIOGRAPHY

PAPERS:

1. McKeown, M. J., Davis, M. E., and O'Kieffe, J. D.: FETAL ELECTROCARDIOGRAPHY: A Valuable Adjunct to Prenatal Management. Postgrad Med. 40:482, 1966.

2. McKeown, M. J., Burks, J. L.: MESENTERIC CYSTS: A Diagnostic Conundrum. Northwest Medicine 65:748, 1966.

3. Davis, M. E., McKeown, M. J.: The Management of Fetal Distress. Obst. and Gynec. Survey 22:549, 1967.

4. McKeown, M. J., Hesseltine, H. C.: VULVAL CARCINOMA: Philosophy of Treatment. Postgrad Med. 41:204, 1967.

5. McKeown, M. J., Bush, R., and Domizi, D.: A Computer System for the Monitoring of Intensive Care Obstetric Patients. Lying-in J. Reprod. Med. 1.275, 1968.

6. Davis, M. E., McKeown, M. J.: Complete Cesarean Hysterectomy in Perspective. J. Reprod. Med. II C1:13-19, January, 1969.

7. Burks, J. L., Bush, R., and McKeown, M. J.: A Computer Based Obstetric Information System. Lying-in J. Reprod. Med., August, 1969.

BOOKS:

1. Hamilton, Jr., L.A., McKeown, M. J.: Biochemical and Electronic Monitoring of the Fetus. Obstetrics and Gynecology Annual, 1973, Appleton Century Crofts, pp. 105-166.

PROCEEDINGS:

1. Bush, R., Domizi, D., Lee, R., and McKeown, M. J.: THE PDP-8/I AS A SATELLITE COMPUTER FOR BIO-MEDICAL APPLICATIONS (Systems Software). DECUS Fall Symposium, 1968.

2. McKeown, M. J., Domizi, D. B.: Computer Enhancement of Obstetric Intensive Care. San Diego, California, San Diego Biomedical Symposium, April, 1970.

3. McKeown, M. J., Domizi, D.: The Intelligent Obstetric Monitoring System. Society for Gynecologic Investigation, March, 1972.

4. Kneler, E., McKeown, M. J.: Experience with Computerized Predictive Scoring of High Risk Obstetric Patients. Society for Gynecologic Investigation, March, 1972.

5. McKeown, M. J., Schorum, S.: A Revolutionary Technique for Ultrasound Imaging. Society for Gynecologic Investigation, March, 1972.

6. McKeown, M.J.: A New Technique of Ultrasound Imaging. American Federation for Clinical Research, May, 1972.

digital

INTEROFFICE MEMORANDUM

LOC/MAIL STOP

TO: Dave Nelson
Grant Saviers

DATE: July 21, 1975
FROM: Gordon Bell
DEPT: OOD
EXT: 2236
LOC/MAIL STOP: ML12/A51

SUBJ: I/O

You guys were going to meet and discuss I/O channels, I/O processors and I/O computers. What's happening? Dave, you were going to propose a uniform message-oriented interface for VAX.

Our disk controllers are sadly lacking in technology/capability/ etc. Please send me a simple (understandable) version of RK06 controller for comment and starting point.

GB:mjk

C1610

digital

INTEROFFICE MEMORANDUM

TO: Ron Brender LOC/MAIL STOP

DATE: July 21, 1975
FROM: Gordon Bell
DEPT: 00D
EXT: 2236
LOC/MAIL STOP: ML12/A51

SUBJ:

Why isn't the WCS assembler written in BLISS? Don't you have many of utilities, interfaces, etc. from FORTRAN?

digital

INTEROFFICE MEMORANDUM

LOC/MAIL STOP

TO: Dave Cutler
Ed Fauvre
Roger Gourd

CC: Larry Portner

DATE: July 21, 1975
FROM: Gordon Bell
DEPT: 00D
EXT: 2236
LOC/MAIL STOP: ML12/A51

SUBJ: MACRO-VAX

Do I correctly assume that the new MACRO-VAX will be written in BLISS?

```
SMERGE(#447);
        EXECUTE(XTEQLOP     ,SYS156,USR131,USR222);
        EXECUTE(XTEQLOP     ,SYS212,USR131,USR223);
        EXECUTE(XTOROP      ,SYS144,SYS156,SYS212);
BRANCH(SYS144,PLIT(#450,#453));
SETLABEL(#453);
        EXECUTE(XTCALLOP    ,USR173,USR173,NIL);
        EXECUTE(XTMOVEOP    ,USR040,USR104,NIL);
        EXECUTE(XTCALLOP    ,USR142,USR142,NIL);
        EXECUTE(XTMOVEOP    ,USR105,USR041,NIL);
DIVERGE(PLIT(#463,#464,#465,#466));
SETLABEL(#463);
        EXECUTE(XTMOVEOP    ,USR023,USR165,NIL);
JOIN(#462);
SETLABEL(#464);
        EXECUTE(XTMOVEOP    ,USR031,USR165,NIL);
JOIN(#462);
SETLABEL(#465);
        EXECUTE(XTCALLOP    ,USR175,USR175,NIL);
JOIN(#462);
SETLABEL(#466);
        EXECUTE(XTCALLOP    ,USR202,USR202,NIL);
PMERGE(#462);
SMERGE(#450);
        EXECUTE(XTNOOP      ,USR221,NIL,NIL);
JOIN(#363);
SMERGE(#467);
        EXECUTE(XTEQLOP     ,SYS156,USR131,USR225);
        EXECUTE(XTEQLOP     ,SYS212,USR131,USR226);
        EXECUTE(XTOROP      ,SYS144,SYS156,SYS212);
BRANCH(SYS144,PLIT(#470,#473));
SETLABEL(#473);
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        EXECUTE(XTMOVEOP    ,USR040,USR104,NIL);
        EXECUTE(XTCALLOP    ,USR142,USR142,NIL);
        EXECUTE(XTADDOP     ,USR105,USR041,USR023);
        EXECUTE(XTANDOP     ,SYS144,USR106,USR157);
        EXECUTE(XTRSHFT0OP  ,SYS144,SYS144,USR160);
BRANCH(SYS144,PLIT(#505,#517));
SETLABEL(#505);
DIVERGE(PLIT(#507,#513));
SETLABEL(#507);
        EXECUTE(XTANDOP     ,SYS144,USR105,USR201);
        EXECUTE(XTEQLOP     ,SYS156,SYS144,USR165);
        EXECUTE(XTEQLOP     ,SYS212,USR023,USR154);
        EXECUTE(XTANDOP     ,SYS144,SYS156,SYS212);
BRANCH(SYS144,PLIT(#511,#512));
SETLABEL(#511);
        EXECUTE(XTMOVEOP    ,USR023,USR154,NIL);
JOIN(#510);
SETLABEL(#512);
        EXECUTE(XTMOVEOP    ,USR023,USR165,NIL);
SMERGE(#510);
JOIN(#506);
SETLABEL(#513);
        EXECUTE(XTANDOP     ,SYS144,USR105,USR201);
        EXECUTE(XTEQLOP     ,SYS156,SYS144,USR157);
        EXECUTE(XTEQLOP     ,SYS212,USR023,USR154);
        EXECUTE(XTANDOP     ,SYS144,SYS156,SYS212);
BRANCH(SYS144,PLIT(#515,#516));
SETLABEL(#515);
        EXECUTE(XTMOVEOP    ,USR031,USR165,NIL);
JOIN(#514);
```

D I G I T A L INTEROFFICE MEMORANDUM

SUBJ: PDP-11 REFERENCE MANUAL

DATE: 07-17-75
FROM: GORDON BELL
EX: 2236
MS: ML12-1/A51

* *
TO: FILE
* *

SUBJ: AVAILABILITY OF BILL ENGLISH (AUTHOR OF 10 REFERENCE AND MAINTENANCE MANUALS AND DG MANUALS)

To: Distribution

How about a really good PDP-11 Reference Manual? Don't we really need one? He's currently working for Savell on some IPG stuff.

Anyone want to talk with him?

He performs well to schedules and with fixed price (assuming there is a penalty clause).

GB:mjk

Distribution

Janice Carnes
Dick Clayton
Bruce Delagi
Bill Demmer
Steve Teicher
Mike Tomasic

cc: Bob Savell

digital

INTEROFFICE MEMORANDUM

TO: Distribution

LOC/MAIL STOP

DATE: July 14, 1975
FROM: Gordon Bell GB
DEPT: 00D
EXT: 2236
LOC/MAIL STOP: ML12/A51

SUBJ: HODGE & TAYLOR--CONSULTANTS

These guys keep calling me about consulting for us. They used to work at GA. They have the attached ECL design which they'll describe for 2K and give design documents for $10K to evaluate for manufacturing. (Rights are ?$.)

They have sold rights to this design--which they say can be manufactured for $200, CA and/or GA and Interdata. They say that Interdata is impressed that it can do the 7/16 in the same time.

They've consulted widely throughout the mini industry with everyone except DG and HP, thus I don't want to educate them. Also they say they're behind the Fortran speed-ups of Varian.

The interesting thing, they claim the ECL microprocessor can be built in one chip.

GB:mjk

Distribution
Bob Armstrong
Dick Clayton
Bill Demmer
Chuck Kaman
Steve Rothman
Steve Teicher

What do you think? Should someone drop by to talk with them?

Copy to Bell, Hedge, Feiler, Forbes, Roma

Winston W. Hodge, Lawrence E. Taylor, & Associates Clayton,

CONSULTANTS TO MANAGEMENT C1616

Minicomputer & Microprocessor Design
Computer & Communication Systems Design
Program Management
Market Analysis & Planning
High Technology Business Planning

Winston W. Hodge
2603 Hillcrest Avenue
Orange, California 92667

Lawrence E. Taylor
18612 Minuet Lane
Anaheim, California 92807

April 1, 1975

APR 04 1975

To: Gordon Bell
Vice President, Engineering
Digital Equipment Corporation
146 Main
Maynard, Massachusetts 01754

From: Win Hodge (714) 637-6556

Subject: Follow-up On 56 I.C. Emulator With No LSI

Reference: March 12, 1975 Correspondence

Dear Gordon:

Attached is a brief product summary of our emulator, as described in our referenced correspondence to you.

We are experiencing interest on this coast from two mini-computer houses, as evidenced by the fact that we are under contract to make preliminary disclosure and do a partial micro-coding of two target processors.

We have, however, retained the ownership of our emulator so that we may present it elsewhere, maintaining only applications micro-code and special interfaces as confidential and proprietary to these customers.

If your interest continues, we would still be most anxious to have a June-July-August technical summer engagement with you.

Sincerely,

Win Hodge

W. Hodge

Attachment

Shall we invite in OK, OK — for review? Sure, why not?

Gordon

Chuck

APR 14 1975

It's worth a day. (I hope!)

HODGE, TAYLOR, & ASSOCIATES LOW COST EMULATOR

Summary of Features:

General Registers - Dual-ported, 64 registers, expandable to 256

Register Addressing Modes - Implicit, explicit, stack

Control Store - 64 words by 24 bits, expandable to 16K X 24

Micro-instruction Cycle Time - 60 ns.

Simultaneous Control Functions Per Micro-instruction - 1 to 20

Number of I. C.'s - 56

Estimated Shop Cost - Under $250

CPU's That Can Be Emulated:

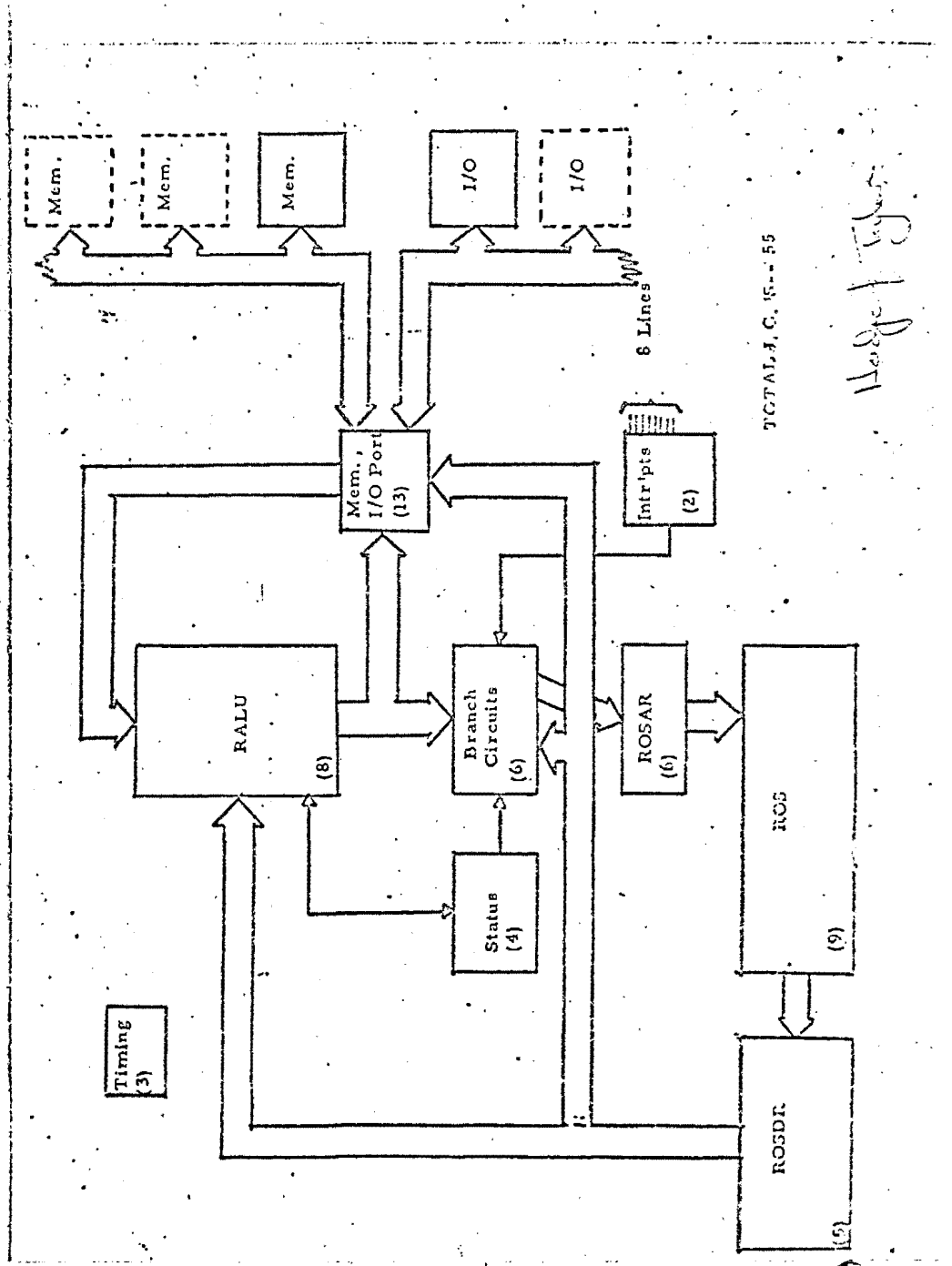
DEC	PDP-11	MICRODATA	800/1600
DEC	PDP-8	HP	2100
GA	SPC-16	IBM	System/3
INTERDATA	7/16	IBM	System/32
DG	Nova 2	IBM	System 360's (low end)
VDM	620-i	IBM	System 370's (low end)

Peripheral Controllers That Can Be Emulated:

Magnetic Tape	Card Readers and Punches
Fixed Head Disks	Tape Readers and Punches
Moving Head Disks	High Speed Line Printers
Floppy Disks	CRT Terminals
Plotters	Communications Controllers and Multiplexor

Computer Interfaces:

Most Popular Mini-computers
IBM 360/370 Channels



C1647

C1618

digital

INTEROFFICE MEMORANDUM

LOC/MAIL STOP

TO: Jim Bell
OOD
Finance Committee

DATE: July 14, 1975
FROM: Gordon Bell
DEPT: OOD
EXT: 2236
LOC/MAIL STOP: ML12/A51

CC: John Fisher, Ken Olsen

SUBJ: HONORARIA--ATTACHED POLICY

The OOD is in the process of approving the following policy having to do with honoraria for talks. I just got a note from Ed Schwartz requesting officers and employees to list boards they're on, which presumably is covered in a policy somewhere.

Last year, I billed CMU for visiting and consulting CMU at $2,000 for joint DEC-CMU, CMU, and some profession-related projects. This year I made four trips and spent a total of approximately one hundred hours (2% of my professional time), much of which was on the phone and computer via the network. My intent was to turn this money over to DEC.

The problem: is my CMU affiliation like honoraria or a board fee? Are board fees turned over to the company?

There are clear cases where DEC doesn't get reimbursed, e.g., teaching classes after hours. Can F&A establish guidelines for everybody and rule on this by issuing the attached policy on some revised, appropriate form?

GB:mjk

Attachment

digital JUL - 1975

INTEROFFICE MEMORANDUM

TO. Gordon Bell LOC/MAIL STOP ML12/A51

DATE. July 9, 1975
FROM. Jim Bell
DEPT. R & D Group
EXT. 2764
LOC/MAIL STOP. ML3-4/E41

SUBJ. Honoraria

Attached is the revised draft of the policy on Honoraria. Since there are still some open issues I will wait until I hear from you before proceeding further.

As we discussed on the phone the key open issues are:

1) should honoraria disbursements be centralized for better record keeping and control?

2) should incoming honoraria always be accepted, even from non-profit institutions, thereby serving

   a) as a control on the number of invitations,

   b) as a small source of income for the company, and

   c) as a counter balance to outgoing honoraria?

3) how do we distinguish between talks which DEC people give on their own (evenings, weekends, vacation days) and those talks given by DEC people as representatives of DEC.

JB/cw

digital

INTEROFFICE MEMORANDUM

TO. Hardware Engineering Managers LOC/MAIL STOP
Software Engineering Managers

DATE. June 27, 1975
FROM. Jim Bell/Gordon Bell
DEPT. R & D Group
EXT. 2764
LOC/MAIL STOP. ML3-4/E41

SUBJ. Policy--Honoraria for Invited Speakers to Engineering Seminars

Background: The academic community has the custom of providing honoraria for invited talks when faculty members speak at other institutions.

DEC employees are offered honoraria for giving talks and participating in conferences at non-profit institutions, the government, and other companies.

Purpose: To establish a uniform policy within DEC with regard to giving and accepting honoraria.

Policy:

1) When a university faculty member is invited to give a seminar at DEC, it shall be customary to provide an honorarium in addition to expenses. The size of the standard honorarium shall be set by the Vice-President of Engineering; it is currently set at a maximum of $150.00, the exact amount to be based on the time and effort involved, and set by the person who issues the invitation.

2) When a DEC employee is offered an honorarium, the employee shall (a) decline it when offered by a university or other non-profit institution and (b) accept it on behalf of DEC otherwise.

3) The responsibility for enforcing this policy, providing outgoing honoraria, and accepting incoming honoraria shall rest with each cost center manager.

JB/GB/cw

READY FOR INPUT
MMC1 RDCB

01620

TO: GEOFF FINCH SALES SUPPORT DEPT READING ENGLAND

FROM: GORDON BELL ML12-1 A51

1. YES - THOUGH NOT STRICTLY AN ARRAY PROCESSOR, BUT A MULTIPROCESSOR.

2. YES, PROF. WULF, 412-[illegible], CMU, COMPUTER SCIENCE DEPT.,
PITTSBURGH, PA. 15213.

MESSAGE ACCEPTED 00826 0959 01-JUL
MMC1 RDCB

READY FOR INPUT

TIMEOUT

01621

0016 1141 27-JUN 35410 1111 27-JUN
RDGB MR11

JUN 30 1975

JUN 27 11 44 AM '75

27TH JUNE 1975 REA/MB 7MAY
TWX NO 0071

127

TO: GORDON BELL [redacted] A.51
FM: GEOFF FINCH SALES SUPPORT DEPT — Reading-Eng.

FRANK BOOTY OF 'COMPUTER WEEKLY' IS WRITING AN ARTICLE ON ASSOCIATIVE OR ARRAY PROCESSING. HE HAS THE FOLLOWING QUESTIONS:-

TO!

1. DOES CARNIGEY MELLON UNIVERSITY, ARRAY PROCESSING PROJECT USE PDP11'S?

2. IF SO, (AND IT WOULD BE IN DEC'S INTEREST) CAN HE HAVE NAME AND ADDRESS AND PHONE NUMBER OF CONTACT THERE?

1. Yes — though not strictly an array processor but a multiprocessor

2 yes, Prof. Wulf, 412-621-2600, CMU, Comp. Sci Dept. Pittsburgh, PA 15213

READY FOR INPUT
MMC1 FORN

01622

TO: JEAN DANIEL M/NICAUD
LABORATOIRE DE CALCULATRICES DIGITALES
16, CH. DE BELLERIVE
CH-1007 LAUSANNE
TELEX 24478

FROM: GORDON BELL MAYNARD ML12-1 A51

WOULD PREFER YOU NOT CONSULT ON DISPLAY CONTROL. CONTRACT IN PROCESS.

MESSAGE ACCEPTED 06027 0900 07-JUL
MMC1 FORN

READY FOR INPUT

TIMEOY

C1623

CRASTRE 24473F
IRS 1715 *
22593X DEC CH

PROP PQPQ 07-JUL 06027 0900 07-JUL

MMC1 FQPN

TO: JEAN DANIEL M/NICAUD
LABORATOIRE DE CALCULATRICES DIGITALES
15, CH. DE BELLERIVE
CH-1007 LAUSANNE
TELEX 24478

FROM: GORDON BELL MAYNARD ML10-1 A51

WOULD PREFER YOU NOT CONSULT ON DISPLAY CONTROL. CONTRACT IN PROCESS

.

NNNN

CRASTRE 24473F

I would appreciate if you could send me more information on the Educational Centre (such things as the type of courses currently being offered, if any software development is done at the centre, etc.) and provide an indication whether or not such an UN-supported visit would be possible from DEC's standpoint.

Betty and I certainly enjoyed our evening with you when you were in Irvine in March and hope that we get to see you again soon.
All the best to Gwynn and the kids.

Sincerely,

Peter

Peter Freeman,
UN Visiting Expert,
and
Asst. Prof., University of California, Irvine

P.S. We just learned that our recommendation to the UN in New York that they buy an 11/70 for the center here was approved! So, this fellowship would be very valuable!

TO: Gordon Bell.

AUG 11 1975

Brad discussed this with me and unfortunately we do not feel that we can for this fellow to work in IPG at this point in time; mainly because we do not have in place the personnel to help him and get him familiarized with our equipment and systems. This was a great opportunity that we have to pass.

Bernie Lamoute

08/08/75

C1646

Copy to Brad Vachon + Peter

JUL 3 1975

International Computer Education Centre

United Nations Development Programme

Office of the Project Manager

Brad

Could you house such an individual for 6 months + lead him in Plan? What about work in Power Monitor Group to do application? GB

Call + find out!

Mr. C. Gordon Bell,
Vice President of Engineering
Digital Equipment Corporation,
146 Main Street,
Maynard,
Massachusetts 01754,
U.S.A.

25th June, 1975

Dear Gordon,

My stay here in Budapest is turning out to be quite interesting and productive. I am primarily helping with the design of a small time-sharing system, but am also working with people here at the Centre on a number of topics.

One of the things that the UN project does is to send staff members from the Centre abroad for study, ranging from a few weeks up to six months. I am writing to you to find out if it is possible to arrange a fellowship for one of the staff members here with the DEC Education Centre.

The particular person interested in this type of fellowship with DEC wants to learn more about DEC equipment and systems from the standpoint of teaching about them. Further, he would like to participate in some sort of programming or development activity so that he could obtain some hands-on-experience on PDP 11's. (In particular, he is interested in process control.) While I realise such work may not be done directly at the Educational Centre, I thought perhaps some sort of arrangement with a DEC user in the vicinity of the Educational Centre could be worked out.

In short, if it still looks appropriate after learning more about the Education Centre, he would like to come there for six months, take some courses, perhaps help teach some, observe others, and do some programming. If some of the programming is on a process-control application, that would be ideal.

The individual involved has a good command of English and is an engineering graduate of the Technical University of Budapest. He has 4 or 5 years teaching experience here with the Centre and programming experience on a number of different machines. I can personally vouch for his competence.

At this stage we basically only need feasibility information. Since the UN would support the individual and pay for his travel and local expenses, what we need to know is a) whether such a "work-study" arrangement would be possible from DEC's point of view and b) whether the Education Centre would be the right place.

Bernie

How about Wademo? - Or some Windlers etc.

?

End

I owe a letter.

I would appreciate if you could send me more information on the Educational Centre (such things as the type of courses currently being offered, if any software development is done at the centre, etc.) and provide an indication whether or not such an UN-supported visit would be possible from DEC's standpoint.

Betty and I certainly enjoyed our evening with you when you were in Irvine in March and hope that we get to see you again soon.
All the best to Gwynn and the kids.

Sincerely,

Peter

Peter Freeman,
UN Visiting Expert,
and
Asst. Prof., University of California, Irvine

P.S. We just learned that our recommendation to the UN in New York that they buy an 11/70 for the center here was approved! So, this follow-up would be very valuable!

01648

digital

August 6, 1975

Mr. Sandler
Atomic Energy of Canada Ltd.
Chalk River, Ontario
Canada

Dear Mr. Sandler:

Regarding your question about why we did not put form feed in the basic LA36 design, we drew the line at features just above form feed and tabs. The design and cost goals were such that we wished to replace the Teletype Model 33 on our equipment and provide significantly greater reliability, at minimal cost. At this time, we are a ways off in the cost, but the reliability has turned out beyond design expectations (2000 hours MTBF). The reliability and increased speed really brings the cost down for the user.

We have put in these features in a kit which is now just being announced. The reasoning was that we should have the lowest cost for the greatest number of users in the basic package; the more cost/performance oriented users such as yourself, who truly understand that more performance and function improves productivity, will buy them. It is continually distressing to find that many users buy on cost alone (i.e. the purchasing agent mentality); hence, we must market to them. I continually argue for more functionality, but we have to be careful of being uncompetitive. I believe that over the next few years the cost of these options will decrease, and there won't be the hassle about their availability in the standard package.

Thank you for your input. As an LA30 user, I believe you'll be pleasantly surprised with the LA36 (with option package).

Sincerely,

Gordon Bell
Vice President, Office of Development

GB:mjk
Attachment
cc: Dave Whiteside
Ed Corell - Mgr., Printer Engineering
Andy Knowles - Vice President, Components

DIGITAL EQUIPMENT CORPORATION, 146 MAIN STREET, MAYNARD, MASSACHUSETTS 01754
(617)897-5111 TWX: 710-347-0212 TELEX: 94-8457

digital

August 6, 1975

Real L'Archevesque
Atomic Energy of Canada Ltd.
Chalk River, Ontario
Canada

Dear Mr. L'Archevesque:

It was thoroughly enjoyable to spend the day at Chalk River last Wednesday. Since it has been about a dozen years since visiting there, it is nice to see the activities that have been going on in the application of the computers you helped design.

The discussion of the network activities were especially vigorous, and I sincerely hope that we can interact with the laboratory in providing equipment, observing use and collaborating on the research. I think it would be worthwhile to begin to have some discussion with our network and communications people when you are further along in the decision process. Since I concur with your approach to use CATV, it would also be helpful to get this view exposed to our internal people. Also, I hope you'll get in contact with Eric Manning at Waterloo, who is also working in this area.

Again, thank you for the invitation to speak, visit, and I look forward to continued interaction over the years.

Sincerely,

Gordon Bell
Vice President, Office of Development

GB:mjk

cc: Jim Bell - DEC, Mgr. of Research and Development
Nat Teichholtz - DEC, Mgr. of Computer Network Development
Stu Wecker - Network Architect

DIGITAL EQUIPMENT CORPORATION, 146 MAIN STREET, MAYNARD, MASSACHUSETTS 01754
(617)897-5111 TWX: 710-347-0212 TELEX: 94-8457

Computing
Services
Office
University of Illinois
at Urbana-Champaign
Urbana, Illinois 61801

C1651

AUG 15 1975

August 8, 1975

Dr. Gordon Bell
Digital Equipment Corporation
146 Main Street
Maynard, Massachusetts 01754

Dear Dr. Bell:

This is just a note to inquire about the computer museum and whether or not the material arrived concerning Illiac I, II, III.

We have been out of contact with each other for a few months and I didn't know whether or not you needed other items.

Sincerely,

Clifford E. Carter
Assistant Director
of Engineering

CEC:dkw

Dear — Cliff

to ~~Harry Yeats~~ inform you that we believe we have everything you wanted. I

The ~~Illiac~~ Illiac I storage tube Tubes and amplifiers, ILLIAC II Switch and core, and ILLIAC III modules are displayed

01650

digital

August 18, 1975

Mr. Clifford E. Carter
Assistant Director of Engineering
Computing Services Office
University of Illinois
at Urbana-Champaign
Urbana, Illinois 61801

Dear Mr. Carter:

Sorry, I didn't get around to informing you about the material. I believe we have everything you sent.

The Illiac I storage tubes and amplifiers, Illiac II switch and core, and Illiac III modules are displayed in the DEC Mill Lobby now.

I also recorded a 9 minute talk on computers and we used photos of the parts in it. The talk is going into service next week.

Thank you for the manuals and parts.

Sincerely,

DIGITAL EQUIPMENT CORPORATION

Gordon Bell

Gordon Bell mjh
Vice-President
Research and Development

GB:as

C1652

August 18, 1975

Mr. Charles E. Letteer, Jr.
Manager, Computer Systems
Data Systems Department
Armstrong Cork Company
Lancaster, Pennsylvania 17604

Dear Mr. Letteer:

If you will send more information on the proposal, I'll send it around for internal review.

Thanks for your letter of August 7, 1975.

Sincerely,

DIGITAL EQUIPMENT CORPORATION

Gordon Bell

Gordon Bell mlh
Vice-President
Research and Development

GB:as

DIGITAL EQUIPMENT CORPORATION, 146 MAIN STREET, MAYNARD, MASSACHUSETTS 01754
(617)897 5111 TWX: 710-347-0212 TELEX: 94-8457

C1653

AUG 13 1975

Armstrong
CORK COMPANY

AREA CODE 717 | TELEPHONE 397-0611

LANCASTER, PA. 17604

August 7, 1975

Dear Chuck,
If you send more information on the proposal, I'll send it around for internal review. Thanks for your letter of Aug. 7.
Sincerely,

Dr. C. Gordon Bell
Vice-President, Research and Development
Digital Equipment Corporation
Parker Street
Maynard, MA 01784

Dear Dr. Bell:

I have been working with Dr. David Freeman for the past several months in defining a thesis topic for my Masters Degree in Computer and Information Science at the University of Pennsylvania. We have narrowed the search to a single proposed topic that includes a hardware/software design using a DECsystem-10 and a PDP-11 that are installed in Armstrong's Research and Development Center. Dr. Freeman asked that I write to you outlining my plans and request any comments that you feel are appropriate, including any similar work that you might be familiar with.

My topic would involve a detailed description of the hardware and software to be used in implementing a multitasking laboratory automation system using a shared memory DECsystem-10/PDP-11. This work differs from that done at other locations (i.e. CERN) in that various experiments would be multitasked on the PDP-11 rather than having the PDP-11 dedicated to a single type of experiment. Under the proposed system, experimenters would develop their programs on the DECsystem-10 using Fortran, thus taking advantage of the full range of 10 capabilities (i.e. text editor, optimizing compiler, etc.). Compiled programs would execute on the DECsystem-10, and, by use of all CALL statements fully control the experiments through the PDP-11. The DEC supplied DMA-10 hardware facility is an integral part of the system functions.

When operational, the system would relieve the experimenter from learning the intricacies of machine language or the necessity of finding a programmer who is knowledgeable and available. The person most familiar with the experiment would usually be the one to write the code. It will also be easier to add new experiments and change existing programs while minimizing the impact of such changes on other running experiments. The programmer will be able to handle functions, such as digital input and output, in a way that is similar to his control over other I/O type devices. Manipulation of the data will be in a high level language familiar to many of the people involved in experimental work at our facility.

I realize that this is a brief description of a somewhat complicated task. However, I wanted to get your initial reactions without boring you with too much of the wrong detail. I am willing to provide whatever additional detail or explanation that you would require.

I appreciate your taking time from a busy schedule to handle this request and look forward to your comments. Correspondence can be sent to me in care of the address shown at the top of this letter.

Sincerely yours,

Charles E. Letteer, Jr.
Manager, Computer Systems
Data Systems Department

MLG

AUG 22 1975 01655

D I G I T A L INTEROFFICE MEMORANDUM

PAGE 1

SUBJ: PHILIPPINES/INDONESIA DATE: 08-18-75
FROM: GWEN BELL
EX: 2237
MS: LINCOLN

TO: FILE

To: Ted Johnson
Ron Smart

Subj: DEC IN THE PHILIPPINES AND INDONESIA

As we discussed when you were at our house, I would try to explore appropriate contacts when I was on my UN missions.

INDONESIA

In early August, I was one of 5 UN consultants at an Indonesian meeting of Ministers--government officials, academics, and private consultants--discussing the spatial components of the next five year plan and toward their plan for 2000. As you may well know, the Indonesian oil company has an 11; it is also used by a firm of engineers--P.T. Widya Pertiwi Engineering, whose President, Ariono Abdulkadir, attended the meeting. Ariono (everyone goes by their first names in Indonesia) got his PhD in Mechanical Engineering from Kentucky several years ago, and started this firm last August. It now has 170 people. He cannot understand why DEC is not in Indonesia; he is very bright; teaches one day a week at the Bandung Institute of Technology--Indonesia's premier school; works extraordinarily hard; and is a super person as well as a true believer (in DEC).

Independently in Bandung, I met Harijono Djojodihardjo, who is Director, Computer Science Division and Computer Centre, Bandung Institute of Technology; and Head, Aerospace Technology Center, The Indonesian National Institute of Aeronautics and Space. He has a recent MsMe, and Sc.D. in Mech. Eng. from MIT. He works part time in addition for Ariono, (who I think is brighter and certainly more of an entrepreneur). Anyway, these are your two contacts in Indonesia. The Bandung Institute of Technology has an old 401 and needs a new machine. This is the place where all the bright young men go who stay in the country and don't go abroad; or this is where they come first for a technical undergraduate degree before going abroad.

Ariono is having one of the people in his firm write a paper which he will send to me, evaluating the computer market

SUBJ: PHILIPPINES/INDONESIA DATE: 08-18-75
FROM: GWEN BELL

in Indonesia. It is a very exciting place; full of resources; developing a cadre of bright young men who are returning; and clearly has potential.

I have said that someone from DEC would probably also be in contact with Ariono, and secondly with Harijono. The addresses are:

Ariono Abdukadir,
President P. T. Widya Pertiwi Engineering,
Romol Pos 3316, Jakarta, Indonesia

Harijono Djojodihardjo
Lapan
Jl. Pemuda Persil No. 1
Jakarta Timur Indonesia

Philippines

Jose Benitez, Senior vice President, Development Academy of the Philippines, was one of the other UN experts at the meeting. He has said that the Academy is considering an 11. He has direct access to President Marcos, and the Development Academy is more or less a supra-cabinet task force organization. He will be at the UN the first week of Sept, and will probably come to Boston on the 2nd or 3rd. I will let you know just barely before, and also hope you could come here and have dinner with him.

[Hopefully, someone will contact these people on a junket. Gordon]

BARRY FERRANTI ASSOCIATES PTY. LIMITED

16 HUNTER STREET. SYDNEY. N.S.W.. AUSTRALIA. 2000. PHONES | 231-2026
P.O. BOX H101. AUSTRALIA SQUARE. SYDNEY. N.S.W.. 2000. | 960-2674

C1658

AUG 15 1975

BFA/BZF

8 August, 1975.

When you arrive US Contact Craig to Schedule a day.

Mr. Gordon Bell,
Chief Engineer,
Digital Equipment Corporation,
Maynard, Mass. 01754,
U.S.A.

We're all pretty busy but would like to understand your talk.

Dear Gordon,

Overseas Visit - August, September, October 1975

I do hope it will be possible for us to meet during my

AUG 22 1975

C1657

TTTT
WUI NY TELUS 119 0827 08/18*
DIGITAL MAYN A
948457
DIGITAL EQUIPMENT CORPORATION
PARKER STREET
MAYNARD, MASS

LT

FERRANTI ASSOCIATES
16 HUNTER ST
SYDNEY NSW, AUSTRALIA 2000

ATTN: BARRY DE FERRANTI

CRAIG MUDGE, RON SMART, AND I WILL BE IN MAYNARD WHEN YOU ARRIVE IN THE UNITED STATES. PLEASE CONTACT CRAIG TO SCHEDULE A DAY. WE ARE ALL PRETTY BUSY BUT WOULD LIKE TO UNDERSTAND YOUR TALK.

FROM: GORDON BELL - DIGITAL MAYNARD

END
+
WUI TELUS NYK

It will be good to catch up Ken Smart and other old friends.
I will probably be visiting UK during mid Sept or to 26.
Could I get together with you, Bob Neal and Greg Mudge?

Yours sincerely,

Barry Z. de Ferranti

Barry Z. de Ferranti

PS Think you would find the work we have done on Echelon of interest. Quite exciting. Have to be discreet about it.

01660

digital

August 6, 1975

Robert H. Vonderohe
Project Manager
University of Chicago
Institute for Computer Research
5640 Ellis Avenue
Chicago, Illinois 60637

Dear Dr. Vonderohe:

Thank you for sending the Christopher proposal of June 11, 1975, on building a PL/1 for the PDP-11. We have been reviewing it extensively internally for the last 2 months.

We are not interested in proceeding with the compiler at this time. A combination of cost, administration, and language definition issues have gone into this decision.

Thank you for the proposal.

Sincerely,

Gordon Bell
Vice President
Office of Development

GB:mjk

DIGITAL EQUIPMENT CORPORATION, 146 MAIN STREET, MAYNARD, MASSACHUSETTS 01754
(617)897-5111 TWX: 710-347-0212 TELEX: 94-8457

D I G I T A L INTEROFFICE MEMORANDUM

PAGE 1

SUBJ: VAXB MEETING AGENDA--8/12/75

DATE: 08-07-75
FROM: GORDON BELL
EX: 2236
MS: ML12-1/A51

* *

TO: MJ FORBES ML12-1/A51

* *

Place: ML3-4 CENTRAL MILL CONFERENCE ROOM
Time: 8:30

8:30-10	VA Mechanism	Hastings
10-10:30	Field/Bits	Rodgers
10:30-11:30	Call/Return	Hastings/Conklin
11:30-12	Status of 75 Design Review Problems	Rodgers

VAXA--DOCUMENTATION FOR VAXB (By 5:00, Aug. 8)

- Status of 75 Design Review Problems	Rodgers
- Call/Return, Field/Bits (handwritten)	Strecker
- VA Mechanism (whatever is ready by Friday evening)	Hastings

---

VAXA SCHEDULE WEEK OF 11 AUGUST

- Strecker - out	
- Compatibility/subsetability Design	with Lipman, Stewart, Delagi, Gourd
- Process Structure/Interrupts/Traps Design	with Lipman/ Stewart

GB:mjk

D I G I T A L INTEROFFICE MEMORANDUM

SUBJ: CHIEF ENGINEER

DATE: 08-07-75
FROM: GORDON BELL
EX: 2236
MS: ML12-1/A51

TO: -BELOW

SUBJ: CHIEF ENGINEER JOB DESCRIPTION THOUGHTS (STAFF POSITION)

To: Mark Abbett, Dick Best, Dick Clayton, Bob Puffer

Overall:

1. Has significant depth* in 2 areas:

   A. Device level (technology e.g., semiconductor, disk, core)
   B. Circuit level
   C. Logic level
   D. Architecture level including networks
   E. Programming
   F. Applications (1 area)

   (Recognized as "near the top" technically.)

2. Knowledge of entire field (breadth)

3. Understanding of business (breadth)

*"Recognized" contributions, talks, patents, papers.

Activities

1. Depth

   A. Solves problems, as needed--in depth 1/2 time
   B. Finds problems.
   C. Recommends strategy--related to "depth areas".
   D. Introduces new technology/techniques to DEC.

2. Breadth

   A. Helps formulate strategy.
   B. Helps with people development (determines/leads?)
   C. Outside spokesman

- customer visits
- talks (internal/external)
- papers

D. Guides Engineering Committee

3. Fire Fighting

GB:mjk

DIGITAL INTEROFFICE MEMORANDUM

SUBJ: TED STROLLO

DATE: 08-06-75
FROM: GORDON BELL
EX: 2236
MS: ML12-1/A51

TO: FILE

To: Distribution

Ted Strollo from BBN called again about coming to work here. So we have anything yet? He's quite good, and oriented to development of both hardware and software. He knows much about COMM.

Mark, will you coordinate this and give his resume to any interested party?

GB:mjk

Distribution

Mark Abbett
Jim Bell
Dick Clayton
Bill Demmer
Alan Kotok
Julius Marcus
George Plowman
Harry Portner
Pat Teichholtz
Mike Tobasic
Fred Wilhelm

)IGITAL INTEROFFICE MEMORANDUM 01665

PAGE 1

'UBJ: OMSI APL

DATE: 08-06-75
FROM: GORDON BELL
EX: 2236
MS: ML12-1/A51

* *

'O: FILE

* *

'o: Distribution

'm ecstatic that we are getting the APL on the -11...
articularly in view of the abortive behavior in the languages
roduct management area...for what I hope will be the last time.
PL is truly one of the triumphs in modern language design, and
believe it will be a significant product over the years.
'lassic 11 will certainly require it.

he deal bothers me somewhat, though not very much, because
e can't lose that much, and we might even make something.
he point is, maybe we could have made more. My initial
ntent was to let OMSI do the front work in development marketing
nd support, and that we could observe it as a marketing
xperiment. By placing options to buy at various times and
arious prices, we could later make APL as a tested product,
hen we had the right hardware (e.g. Classic 11), and when the
arket developed. Somehow, I don't see adding more software
o our catalog, since we make no money on nearly all software,
nd this one could be high support. (Not many software support
eople speak APL.)

yield to the marketing strategists here in that we have chosen
orrectly (I'm happy that we have the product), and I look
orward to seeing the business plan, which George has agreed to
rovide.

would believe this is a nice one for George and Larry (as
roduct Manager-Maynard) to present to the Marketing Committee
n a formal basis as it begins to focus on issues of pricing nad
upport.

B:mjk

istribution:
---
ave Brown
runo Durr
on Hardy
d Kramer
ill Long

UBJ: OMSI APL

DATE: 08-06-75
FROM: GORDON BELL

arry Portner
harlie Spector
eorge Thissell

c: Marketing Committee, OOD

SUBJ: REGARDING YOUR MEMO ON THE MUSEUM

DATE: 08-06-75
FROM: GORDON BELL
EX: 2236
MS: ML12-1/A51

* *
TO: FILE
* *

To: Don Mallinson

I was really happy with your memo. It looks like a good workable plan to proceed with. My 9 minute logic talk and the ML12-1 exhibit is about a week from completion, and the deadline is for the Board of Directors meeting on 18 August--so we can try it out on them.

We'll go ahead and give you text and some photos with the written version of the talk so that a little leaflet can be made available.

The Whirlwind module has been delivered to you in Marlboro and can be taken to the WESCON show. It would be great to take the 1K core to WESCON. The PDP-8 (Mill lobby) with music programs and VI05 has also been delivered to Marlboro for you to try out.

Can another panel be started?

GB:mjk

cc: Mimi Cummings, Andy Knowles, Ken Olsen

D I G I T A L INTEROFFICE MEMORANDUM

SUBJ: RELIABILITY/QC BROCHURE

DATE: 08-06-75
FROM: GORDON BELL
EX: 2236
MS: ML12-1/A51

TO: DISTRIBUTION

SUBJ: RELIABILITY AND QC BROCHURE--HOW MUCH TO DO A QUALITY JOB?

Distribution: Dick Clayton, Tom Coleman, Carl Noelcke

I read the draft because I was asked to give a talk on the reliability of our products at a customer site. They have perceived that the quality has fallen over the PDP-8, and I tried to assure them it hadn't. Has it? Can your brochure say? In preparing the talk, I first came at it from the things that have been happening the last year to improve quality, and then I read your brochure. Although I got some of the details to help the talk, I found it to be pretty superficial, and didn't learn very much.

The talk turned out to be acceptable to them as not many of the 250 or so walked out, even though it was the 2nd hour they listened to me; and I prepared it between 5 and 7:30 am on the plane to Ottawa. Anyway, the whole business is a multi-stage pipelined process shown in the sketch. Information and materials flow between the stages. You could really orient your paper this way, and then carry each chapter down to more detail (boxes). There are things (activities) that all groups engage in to make reliable products.

The basic theme I used was that we are producing more reliable products because we actually understand how the manufacturing system works, and how a design theoretically works. I gave some of the numbers on the RK05 improvement program, and that we really didn't react soon enough. Some of the things that make it work also include the Product Management function which is measured on the profitability through warranty, and include engineering changes for production. This really affects quality. Also, our plant managers are measured on both quantity and quality.

Bring the user in too--he should be demanding, and he should do the things we suggest to have reliability such as using redundant parts. He should demand that we tell him how well something will work before he buys. Your brochure doesn't help him understand or face this!

My impressions were on a very quick reading:

SUBJ: RELIABILITY/QC BROCHURE DATE: 08-06-75
FROM: GORDON BELL

Impressions

1. Not a very good, top-down structured approach to presentation.

2. Page 16 few #'s, e.g., seventeen ball bearing fans. Lots? Little? Are sleave bearings better? What is the importance? Will it work with 16? How often does a fan kill you? The chart is unconvincing. Do we run IC's hotter?

3. Lots of little bullets (i.e. 1 liners) with no real depth.

4. Can you put in the DEC Standard which relates to Design Reviews?

5. There are numerous new standards and tests introduced this year to increase reliability. State them.

6. Why not put in a case study--RK05 or LA36 or VT50 with real #'s? Compare LA36 with well known alternative.

7. Theme should be--there is a "science" to making things reliable. It is based on knowledge (information). In all areas, we first design--based on principles, and then test to verify that the original design (hypothesis) is correct.

8. You didn't have micro positioning for disks.

9. Self testing on 11/04 and 11/34.

10. The best part is the one not there...our serial consoles get rid of the lights and switches plus offer possible use remotely.

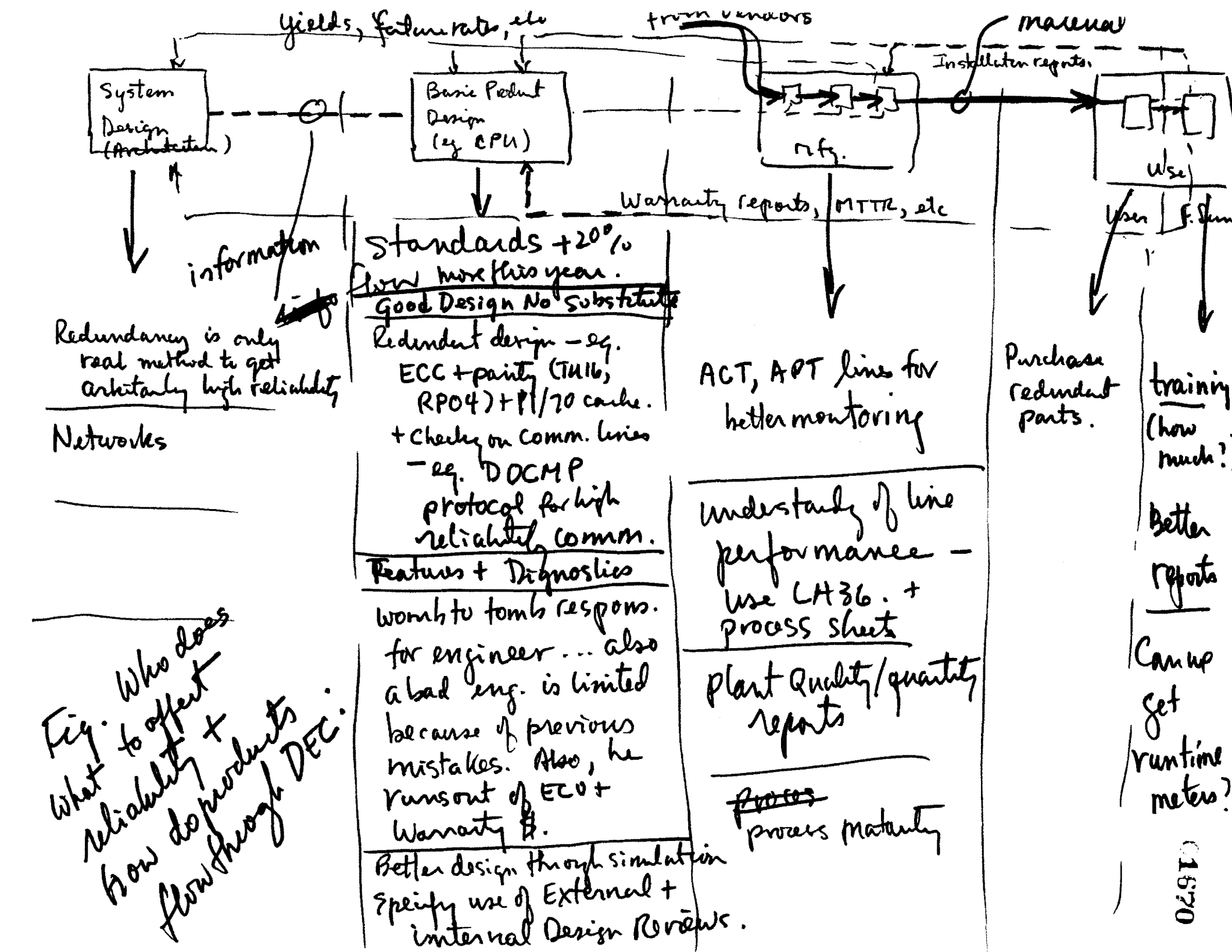
11. Simulation is used extensively on LSI-11: circuits, gate, resister-transfer, and systems.

12. MTBF indicator will come from parts list to help understand design maturity + field data.

13. Our people are better vis a vis their engineering backgrounds to understand the process statistical issues--i.e., education is important too.

14. We use our own computers in the design, construction and test. If you know what we do relative to say some of the other test equipment, that might be worthwhile. We were first to have computer testor for modules and for memories!

GB:mjk


Yields, failure rates, etc
from vendors
material
Installation reports
System Design (Architecture)
Basic Product Design (eg CPU)
mfg.
use
Warranty reports, MTTR, etc
information
Standards +20% flow more this year.
Good Design No Substitute
Redundancy is only real method to get arbitrarily high reliability
Redundant design – eg. ECC + parity (TU16, RP04) + P1/70 cache. + Checks on comm. lines – eg. DOCMP protocol for high reliability comm.
ACT, APT lines for better monitoring
Purchase redundant parts.
training (how much?)
Networks
Features + Diagnostics
Understandg of line performance – use LH36. + process sheets
Better reports
womb to tomb respons. for engineer ... also a bad eng. is limited because of previous mistakes. Also, he runsout of ECO + Warranty $.
plant Quality/quantity reports
Can we get runtime meters?
Process maturity
Better design through simulation
Specify use of External + internal Design Reviews.
Fig: Who does what to effect reliability + how do products flow through DEC.
1670

```
175   4    100   0  272   0      0 SETNCC
176   3      0   0    0   0      0 0,200
177   3      0   0    0   0      0 0,7
200   4    100   0  276   0      0 SETVCC
201   3      0   0    0   0      0 0,177777
202   4    100   0  310   0      0 SETZCC
203   4    100   0  322   0      0 SIGNEX
204   3      0   0    0   0      0 0,177400
205   4    100   0  332   0      0 BRANCH
206   4    100   0  360   0      0 EXEC
207   4    100   0  364   0      0 CLR.B
210   3      0   0    0   0      0 0,50
211   3      0   0    0   0      0 0,1050
212  10   1001   0    0   0      0 SYFLAG
213   4    100   0  400   0      0 COM.B
214   3      0   0    0   0      0 0,51
215   3      0   0    0   0      0 0,1051
216   4    100   0  424   0      0 INC.B
217   3      0   0    0   0      0 0,52
220   3      0   0    0   0      0 0,1052
221   4    100   0  447   0      0 TST.B
222   3      0   0    0   0      0 0,57
223   3      0   0    0   0      0 0,1057
224   4    100   0  467   0      0 ADC.B
225   3      0   0    0   0      0 0,55
226   3      0   0    0   0      0 0,1055
227   4    100   0  537   0      0 MOV.B
230   3      0   0    0   0      0 0,11
231   4    100   0  562   0      0 ADD
232   7   1001   0    0   0      0 SYTEMP
233   3      0   0    0   0      0 0,200000
234   3      0   0    0   0      0 0,20
235   4    100   0  613   0      0 CMP.B
236   3      0   0    0   0      0 0,12
237   3      0   0    0   0      0 0,400
240   4    100   0  651   0      0 ROR.B
241   3      0   0    0   0      0 0,600
242   3      0   0    0   0      0 0,10600
243   3      0   0    0   0      0 0,777
244   3      0   0    0   0      0 777777,777000
245   4    100   0  714   0      0 BPL
246   4    100   0  721   0      0 BLE
247   4    100   0  726   0      0 BNE
```

August 6, 1975

E. A. Weiss
Sun Services Corporation
240 Radnor-Chester Road
St. Davids, Pennsylvania 19087

Dear Eric:

I'm sorry I can't respond at this time due to time pressure. Right now I'm reluctant to delegate this to people who would do a good job since they are currently under similar pressures. I'm circulating the request however.

Sincerely,

Gordon Bell
Vice President
Office of Development

GB:mjk

DIGITAL EQUIPMENT CORPORATION, 146 MAIN STREET, MAYNARD, MASSACHUSETTS 01754
(617)897-5111 TWX: 710-347-0212 TELEX: 94-8457

Circulate J Bell, Sebern, Dyer, 01680

SUNOCO

SUN SERVICES CORPORATION 240 RADNOR-CHESTER ROAD, ST. DAVIDS, PENNSYLVANIA 19087 (215) 977-1600

Robert B. Anderson
President

JUL 15 1975

July 8, 1975

Dr. Gordon Bell
Digital Equipment Corporation
146 Main Street
Maynard, MA 01752

Dear Gordon:

Although the letter soliciting questions for the ACM Self-Assessment Test is directed to authors of books that deal with programming skills and techniques, I also sent copies to major figures in the industry who I thought would be willing to send questions which deal with the fundamentals of computing. You are in my category of "major figures."

I would like to have several questions which you think illuminate fundamental and important parts of the subject of computing, but failing that, perhaps you would be willing to designate a surrogate at DEC to do this for you.

I have now sent out about half the solicitations for questions and do not know what kind of response I will get. Consequently, I am anxious about the outcome and would appreciate some encouragement from my friends in the form of test questions.

Very truly yours,

Eric

E. A. Weiss

EAW/mv 1/7

Eric
I'm sorry I can't respond at this time

due to time
Right now I'm
pressure also
reluctant to put this
this to people
on to what Harris is
delegate
& relatively unmotivated

who would
do a good
job for them
anonymously under
some

Yours are welcome
to respond —
but no pressure from
me.

SUBJ: AGENDA/MINUTES OOD

DATE: 08-27-75

FROM: DICK CLAYTON

COMPANY CONFIDENTIAL

SUBJ: MILITARY COMPUTER STRATEGY

The August 11 memo to Operations committee (attached) stands. Since that time, we have continued with Rolm and Raytheon. My present belif is that we will have the opportunity to reach agreement with both Rolm and Raytheon within the next 6-8 weeks. They will be sufficiently willing and we will perceive adequate market such that there is a sound basis for proceeding with one (or possibly both) of them.

RC:mjk

Attachment

digital

INTEROFFICE MEMORANDUM

TO: Operations Committee LOC/MAIL STOP

cc: Military List

DATE: August 11, 1975
FROM: Dick Clayton
DEPT: Computer Systems Development
EXT: 3638
LOC/MAIL STOP: ML5/E71

SUBJ: STATUS OF MILITARIZED PDP-11

Background:

There seems to exist a market for $10 - $20 million per year of relatively standardized, militarized, PDP-11 compatible computers. The existence of one or more militarized PDP-11's would have some positive impact on at least several million dollars of current commercially oriented DEC business.

All this is part of a several hundred million dollars annual military business in Computer Systems and Custom Software dominated by IBM, UNIVAC, CDC, Raytheon, Rolm, Bunker Ramo and others. There seems to exist a significant push toward more standardization of product by the Airforce and Navy (especially mini & micro).

Current Activity:

We have casually invited proposals from several suppliers. We have a proposal from Rolm, a significant interest and apparent internal activity at Raytheon, and an internal proposal being done by Bunker Ramo.

All seem interested in PDQ level products. I believe the present seriousness of the activity is: Rolm, Raytheon, followed a distance by Bunker Ramo, in that order.

Recommendations:

- Do not build ~~an~~ a product ourselves
- Do not plan on being a significant marketing channel
- Push Raytheon for their proposal
- Work on Rolm to modify their proposal from DG & DEC to DEC only (over 3 yrs.). Soften the exclusivity of Rolm after a given period of time.
- Leave door open for DEC to market limited volumes of the product via an OEM arrangement.
- Leave door open for us to manufacture after 4 years.

#1202

INTEROFFICE MEMORANDUM

01686

TO: Gordon Bell
Larry Portner
Dick Clayton
Phil Laut
C-Irene Leary

DATE: August 20, 1975
FROM: Bob Puffer
DEPT: Hardware Development
EXT: 2863
LOC/MAIL STOP: ML1/E38

SUBJ: Increased FY76 Funding

I request $740K in increased funding as follows:

PRINTERS

	Q1	Q2	Q3	Q4	FY76
Approved	441	462	460	467	1830
Proposed	541	542	468	467	2018
Change	100	80	8	0	188

The above $188K is the remainder of the $250K appropriation approved for Q3 and Q4 last year. It could not be fully expended in FY75 because approval came too late in Q3.

The money is to complete the LA36 options and LA180. The alternative is to be over budget in Q1 but catch up in Q2 and Q3 by delaying high volume production for two months on these products.

DISKS

	Q1	Q2	Q3	Q4	FY76
Approved	943	964	990	1059	3956
Proposed	952	1006	1089	1119	4166
Change	9	42	99	60	210

Of the above, $160K funds RK06 Design Maturity Testing of 12 units which was not originally budgeted (a mistake). It also provides for necessary additional RK06 tooling. An additional $150K over plan for tooling will be amortized against product cost.

Alternatives are to keep the RK06 funded by reducing the number of design maturity test units and delay the RK07 project until FY77 or slip the RSL by two months.

The other $50K will allow us to maintain a Q2 FY77 first shipment for the RK06 Massbus interface. Although the project was stopped one month ago, the response to the cancellation suggests we will have to restart it. Without added funding it will be a Q3 ship.

D I G I T A L INTEROFFICE MEMORANDUM 01688

PAGE 1
SUBJ: AGENDA/MINUTES OOD DATE: 08-27-75
FROM: DICK CLAYTON
EX: 3638
MS: ML5-2

* *
TO: FILE
* *

To: OOD

SUBJ: OOD STAFF AGENDA--8/28/75

10:30	Review Minutes	All
10:35	Review Agenda--current/future	All
10:45	Discussion of COMM Stratesies	Bastiani et al
	A. What is COMM stratesy?	
	B. Is Corporate Processor really understood and funded?	
	C. What is thousht/status of serial bus?	
	D. What should happen to IOP processor?	
	E. Is there an SDLC chip fundins problem?	
11:40	How do we set a serial bus?	Avery/Bastiani
12:00	Is DEC System 20 sroup doins the risht thins in chansins from core to MOS	Lemaire/Lens/ Fasequist
12:30	Military computer status	Clayton
12:40	End	

SUBJ: AGENDA/MINUTES OOD

DATE: 08-27-75
FROM: DICK CLAYTON

01689

FUTURE AGENDA ITEMS

9/4/75	Product Mgrs. dinner meetings.	Portner et al
9/4/75	Assignment of Best/Noelcke	Puffer/Clayton
9/4/75	Product Mgrs. review (45 min)	
	Job Descriptions	Abbett
	Green Sheet	Portner/Clayton
	Overall organization perception	All
9/4/75	Business Plan Review Procedure	Laut
9/4/75	Review of the role of OOD staff sec. (and rotation)	All
9/4/75	QCMS Defect Reporting system	Smith/Pecore
9/11/75	OOD-Marketing Committee interface	Laut/All
9/11/75	Sales Meeting participation	All
	Who is covering which ones?	
	What message do we have?	
	Is action on new product control necessary?	
9/11/75	What is the status of PDQ project and what have we learned?	Demmer/Clayton
9/18/75	What is the three year serial bus strategy (15 min.)	Clayton/Bastiani
9/18/75	Approval of OOD Space Guidelines (30 min.)	Laut
Sept.	Report on in-house PDP-11 usage.	Computer Resources Committee
Sept.	Is there a field Integration Plan yet?	Smith/Shields/ Clayton/Puffer
Sept.	Honoraria Policy	Bell
10/9	Is there a formal action plan that allows follow up on field oriented product safety problems?	Shields/Minezzi
Oct.	Block Mode Strategy Resolution	Marcus/Portner
?	Is action on ECO control called for at this time.	Marcus
?	What is happening to make systems a reality in the way we do business.	Clayton

---

Expected attendance at next 3 weeks OOD meetings:

GB	LP	BP	DC	PL	MA	JM	HL
--	--	--	--	--	--	--	--

SUBJ: AGENDA/MINUTES OOD

DATE: 08-27-75
FROM: DICK CLAYTON

8/28		X	X	X	X	X	X	X
9/04	X	X	X	X	X	X	X	X
9/11	X	X	X	X	X	X	X	X

RC:mJk

Attachments

HELP!

INTEROFFICE MEMORANDUM

C1691

		LOC/MAIL STOP		
TO:	Julius Marcus + OOD	PK3-1/M10	DATE:	9 JUL 75
	~~Roger Gady~~	PK3-1/M29	FROM:	Vince Bastiani
	~~Don Alusic~~	PK3-1/M10	DEPT.	DECcomm Eng.
	Tony Lauck	PK3-1/M10	EXT.	3292
	Nate Teichholtz	ML12-2/A62	LOC/MAIL STOP:	ML5-3/E43
CC:	~~Bill Ross~~	PK3-1/F27		

Bill Arey; ~~Stan Frisbie~~

SUBJ: CENTRAL COMM PROJECTS

Listed in the attachment is the schedule for centrally supported projects in FY76. The projects have been divided into:

A.	Support	Overhead projects needed to support equipment and propose new projects.
B.	Software	Money allocated to provide software drivers for COMM devices.
C.	Current Hardware Projects	Those projects which are on-going.
D.	Future Hardware	Those projects to be started in this fiscal year.

The future projects are ranked in order of priority and represent the product manager's thinking, after discussion with various product lines (Telco, DECcomm, Business, LDP). The total priority list is shown in enclosure 2 with the funding limit line shown. The priority ranking takes into account the COMM I&P processor approach described in my 10 JUN 75 memo, as this appears to be the most viable approach to cutting down the number of Comm options and also provides both cost effective low and high throughput capability.

Note that the serial bus has fallen below the level of funding line. This is a result of adding in the two interfaces required for the LSI-11, which will provide a more immediate payoff than dollars spent on the serial bus. The serial bus, I still believe to be a longer term necessity and should be pursued by someone (Industrial or processor people). However, the only way I could continue this effort would be with additional E20 funds over the 952 allocated.

Money being spent for software drivers has been divided up by Nate Teichholtz and is part of the overall Network software budget. This money in part, will provide RSX11-D and RSX11-M

I'd sure like a different allocation. The LSI-11 came out of the blue. I think we have a plan under DUST. Another plan would be to keep the Serial Bus alive. I want to discuss this at OOD staff. The Serial Bus is dead by this group.

8112-

INTEROFFICE MEMORANDUM

1692

TO: Gordon Bell

CC: OOD
Vince Bastiani
Tony Lauck
Don Alusic

DATE: August 4, 1975
FROM: Julius Marcus
DEPT: Communications Products
EXT: 3191
LOC/MAIL STOP: PK3-1/M10

SUBJ: Communications Engineering Goals

1100

Product

Minimize comm hardware and software investment consistent with

a) single machine comm I/O support

b) front end and networking capability needs

i.e., exploit

generality of I/O,

front end concepts,

DECnet.

Organizational issues

Get backup to Vince in his group

Get "systems" knowledge applied to comm I/O specifications and planning

Assure better software/hardware planning for the comm functions since clearly both disciplines are involved.

mr

TO: GORDON BELL
DICK CLAYTON
JULIUS MARCUS
VINCE BASTIANI

The budget that Vince has submitted supports the goals outlined here.

As a separate issue, I'm worried that MULTIDROP will drop through the cracks. There is no mention of it here or in Vince's Budget. Vince has suggested that it be picked up by Dick's group or IPG.

I suggest we discuss at staff meeting

Phil dant 8/11/75

digital

INTER-OFFICE MEMORANDUM

LOC/MAIL STOP

TO: Vince Bastiani
CC: Bob Puffer
Andy Knowles
Gordon Bell
Don Alusic

DATE: May 28, 1975 01694
FROM: Julius Marcus
DEPT: Communications Products
EXT: 3191
LOC/MAIL STOP: PK3-1/M10

SUBJ:

cc NAT + Peter for Staff Dick

Vince, please find out what is going on with Multidrop development for the LA36's and write a broadly dispersed paper on what hardware and software is needed to use this product on DEC systems. I am under the impression that there is a Multidrop option recently priced on the LA36 which was developed by the Central Development Group. I'm also under the suspicion that some work of this type is being done by Logic Products.

Use Tony to make comments on software issues to state the minimal support necessary to support the LA36's in this environment.

I am concerned that we look disconnected within the Corporation (literally).

Bell Stall

mr

7/25

DIGITAL

OOD Staff

INTEROFFICE MEMORANDUM

TO:		LOC/MAIL STOP
	G. Bell	ML12/A51
	C. Ball	PK3/S20
	D. Clayton	ML5/E71
	J. Cudmore	ML1/E30
	G. Mondani	ML1/E30
	B. Puffer	ML1/E38
	J. Shields	PK3/A58

DATE: 21 July 1975
FROM: Ron Minezzi
DEPT: Product Safety
EXT: 3122
LOC/MAIL STOP: ML1/E30

01695

SUBJ: RESOLVING PRODUCT SAFETY PROBLEMS

One area of extreme concern in the resolution of product safety problems is the actual implementation of corrective action. Past experience with such incidents, as the Bell Labs fire, has shown that we need a well formulated program that will allow us to implement field retrofit changes quickly and in such a manner that we would have documented proof of such implementations.

I feel that such a program must start with a plan and time table for procuring parts and materials and any special manufacturing functions that are necessary.

EXAMPLE

Materials

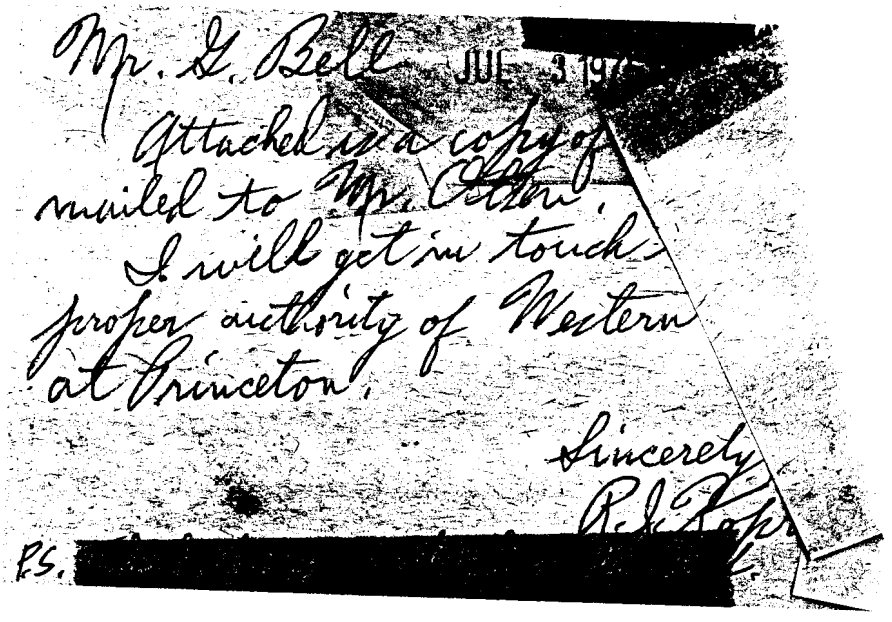
List of parts and materials	Method of Procurement	Person Responsible	Date to be Received

Manufacturing

Functions to be performed	Instructions Required	Person Responsible	Place of Manufacture	QC checks needed	Date of Completic

Consideration should also be given to stockroom requirements. Other considerations of materials is how do we select who handles it? Should it be one group in every case, or should we use who ever is available.

The second part of the problem is how do we notify our own people? (We will have the means of notifying customers thru mail before FY75). Past experience has shown that there is no positive and efficient method of notifying field service that they must take corrective action. Should we develop a special code system for letting everyone know that a problem requires special handling? Could we use the present A.I.D.'s system to communicate directly to field offices with a mandatory answer required by a predetermined time.


Mr. L. Bell JUL 3 19[redacted]

Attached is a copy of [redacted]
mailed to Mr. Colton.
I will get in touch
proper authority of Western
at Princeton.

Sincerely
R. L. Kap[redacted]

P.S. [redacted]

digital

INTEROFFICE MEMORANDUM

TO: OOD
LOC/MAIL STOP

CC: Mark Abbett

DATE: July 29, 1975
FROM: Mary Jane Forbes
DEPT: OOD
EXT: 2237
LOC/MAIL STOP: ML12/A51

SUBJ: JUNGLE MEETING--JULY 30, 31, 1975 (Larry's place*)

July 30

6:00 PM Dinner - Open discussion for agenda of next day.

July 31 Goals, space, etc.--to be determined night before.

*Note: Bring sleeping bag if possible.

GOALS

External Goal:

To establish Software Engineering as a significant, visible, contributory growth vehicle for the corporation which permits flexibility of market selection and maximizes hardware and system sales.

Internal Goals:

Because it is through

1. the integrity and contents of the product we provide
2. our ability to implement and efficiently operate the process for better product creation
3. the quality, depth, and efficiency of our human resources that operate the process of Software Development
4. the strength of our reputation

that our goals will be attained; the internal goals are in 4 parts.

1. Product Goal:

   To continuously make available products of higher quality and performance which allow the corporation to occupy a dominant position in it's present and future end-user market places.

2. Process Goal:

   To ensure the timely completion of product development to the appropriate plan in keeping with the customer and corporate expectation of cost and performance, through a disciplined engineering process.

3. People Goal:

   Maximize the performance of our human resource by having the required technical/managerial depth and providing an environment for their personal achievement, advancement, and recognition.

4. Other Goal:

   Strengthen total corporate operations through the services provided to both internal and external customers.

OBJECTIVES

01707

1. Product Objectives

   1.1 Gain Market leadership; position

   1.2 Achieve higher product quality image

   1.3 Improve the product contents

   1.4 Establish a product continuum from low end 11 thru high end 10

   1.5 Simplify the product offering.

2. Process Objectives

   2.1 Install a Software Engineering process which operates to plans

   2.2 Improve ability to manage to the plans

   2.3 Upgrade the development technology/methodology

   2.4 Improve the planning process

   2.5 Develop a clear uniform process for maintenance and field support.

3. People/Organization Objectives

   3.1 Improve the organization's depth

   3.2 Increase the emphasis on individual responsibility and accountability

   3.3 Improve recognition and participation.

4. Other Objectives

   4.1 Improve services to our internal and external customers.

PRODUCT OBJECTIVES

OBJECTIVE	RESPONSIBILITY
1.1 Gain Market Leadership Position	
1.1.1 General	
. Product superiority in most of the products most of the time. Development should always occupy a dominent product position in its marketplaces - this doesn't mean we can (or have to) be best in all aspects of every market, but it does mean that we must have at least one leadership product in every major segment of each of our markets. If we can't afford to occupy a leadership position, perhaps we are in the wrong markets.	
Specific	
. Establish and understand the competitive environment for all software products, and demonstrate this understanding in the Business Plans, "family" plans and in pricing approval presentation.	✓M. Woolsey
. Develop semi-annual report on our competitive posture in software and systems.	✓M. Woolsey
1.2 Achieve Higher Product Quality Image	
1.2.1 General	
. Have the highest quality software in the industry - "if you buy it from DEC, it will work!"	
Specific	
. Installation of a Q.A. policy and procedure for centrally and non-centrally developed software.	✓ J. Mileski
. Implementation of a field test policy and procedure.	✓ J. Mileski
. Staffed and operational independent Quality Audit activity.	✓ J. Mileski
. Higher communication quality in our manuals - test them by having the writers trade manuals with the recipient using the documentation to use the system.	✓ O. Kostetsky
. Better print quality, particularly of examples.	✓O. Kostetsky

OBJECTIVE	RESPONSIBILITY
. 100% accuracy of examples in present and future manuals.	✓ O. Kostetsky
. Zero defects program in the SDC shipped kits.	✓ O. Kostetsky
1.2.2 General	
. Development and implementation of an overall RAS concept for our products.	✓ J. Mileski
Specific	
. Overall RAS program for DEC software (and systems).	✓ J. Mileski
. Useful statement of RAS goals for DEC products and a measurement and feedback system.	✓ J. Mileski
. Documented RAS goals for all diagnostic products and supportive diagnostic plans.	✓ E. Fauvre
1.3 Improve the Product Contents	
1.3.1 General	
*. Documented technical strategies available and updated at the component, subsystem and system level. How are we going to make our products?	✓ G. Plowman
Specific	
. Hold quarterly "State of the Technology" presentations for interested audiences.	✓ J. Bell
. Thru Research, bring in at least 2 new products or process technological improvements each year.	✓ J. Bell
. Develop effective Software Product Strategies in support of Central Engineering and DEC-10.	✓ L. Wade/M. Woolsey
. Maintain consistency between the product strategy and the product plans.	✓ M. Woolsey
. NO DEVELOPMENT OF 32-BIT SYSTEM WITHOUT CLEAR, DOCUMENTED OVERALL DIAGNOSTIC STRATEGY.	✓ E. Fauvre

*High Priority

OBJECTIVE	RESPONSIBILITY
. Clear attention in the diagnostic strategy and plans to support the highly leveraged areas, such as Field Service.	✓E. Fauvre
1.3.2 General	
. Achieve a meaningful integration of hardware and software planning and development, so that we can profitably address the tradeoff opportunities between the two disciplines.	✓L. Wade ✓M. Woolsey ✓G. Plowman
. Each new product should specifically address hardware/software tradeoffs. - Should we implement it in ROM? or WCS? Should the error recovery be hardware or software? What are application requirements that have hardware/ software implications? Such as context switching, character handling, and memory management?	✓ LW
Specific	
. Install scheme for tracking and controlling hardware support commitments.	✓G. Plowman
1.3.3 General	
. Strong applications orientation in a ll of our products. Each new development should specify several planned applications areas and specifically address the issue of these applications support requirements.	✓M. Woolsey ✓G. Plowman ✓E. Fauvre
Specific	
. Establish and maintain a clearing house of all applications development planned or underway in the corporation.	✓E. Fauvre
. Formal consulting/planning role to provide an "applications requirements" input to new systems software.	✓E. Fauvre
. Aggressive participation in new "small systems" development.	✓G. Plowman ✓E. Fauvre
.4. Establish a Software Product Continuum from Low End 11 through High End 10	
1.4.1 General	
. Have absolute upward compatibility through the entire product set.	
. Intensify concentration on standards to achieve compatibility goals.	✓G. Plowman

OBJECTIVE	RESPONSIBILITY
Specific	
. Have totally transportable device drivers.	G. Plowman/ E. Fauvre
. Develop Software Product Plans for each Software Product Family, including clear product positioning, time phasing and competitive goals.	M. Woolsey/L. Wad
. Integrate the Software Product Family Plans for consistency across families.	M. Woolsey/L. Wad
*. Short term - clarify compatibility goals (10-11, INTRA 11, 11/85, 11/70-32) and develop compatibility plan.	G. Plowman/L. Wad M. Woolsey
. Management support of standards activity and implementation plan for current and emerging standards.	G. Plowman
. Development of uniform standards for applications quality, reliability, documentation, etc.	E. Fauvre
1.5. Simplify the Product Offering	
1.5.1 General	
. Minimization of product set thru standard interfaces, modular implementation, etc. Guidelines in the foreseeable future - there should not be more than 2 implementations of any language processor or major utility.	G. Plowman/ M. Woolsey
. Decreased emphasis on ultra small core systems; core is getting cheaper, software is more complex.	G. Plowman/ M. Woolsey
Specific	
. Phase out old versions/multiple versions of products.	M. Woolsey
. Better organization of documentation set.	O. Kostetsky
. Share all language and utility manuals; write them once, and change only the cover.	O. Kostetsky
. Fewer pages in the manual set, with higher information content.	O. Kostetsky
. Maximum of 3 distribution mediums.	O. Kostetsky
. Continuous reduction of per system software kit costs.	O. Kostetsky

*High Priority

2. PROCESS OBJECTIVES	RESPONSIBILITY
OBJECTIVE	
2.1 Install Software Engineering Process	
2.1.1 General	
. Perform no development without a plan.	All ✓✓✓✓✓✓
Specific	
. SYSTEMS - FIRST AND FOREMOST - NO DEVELOPMENT FOR 32 BIT SYSTEM WITHOUT TOTAL LONG TERM DEVELOPMENT PLAN, INCLUDING CONVENTIONS, TECHNIQUES, SPECIFIED SOFTWARE SYSTEM ARCHITECTURE TOOLS PLAN, SUPPORT, DISTRIBUTION, AND MAINTENANCE PLAN, ETC.	✓G. Plowman
. DIAGNOSTICS - NO DEVELOPMENT OF 32-BIT SYSTEM WITHOUT CLEAR, DOCUMENTED OVERALL DIAGNOSTIC STRATEGY.	✓E. Fauvre
*. Short term - documented development plans for FY76.	✓G. Plowman/L. Wade
. Each new product should specifically address hardware/software tradeoffs. Should we implement it in ROM? or WCS? Should the error recovery be hardware or software? What are application requirements that have hardware/software implications? Such as context switching, character handling, and memory management?	✓G. Plowman/ ✓M. Woolsey
2.2 Improve Ability to Manage to the Plans	
2.2.1 General	
. Have a clear statement of product goals at the component, subsystem, and system level.	✓G. Plowman
. Install a process for maintaining the development plan, tracking and controlling changes to the plan, including changes in goals, scope, content, technique, schedule or budget.	✓G. Plowman/ ✓E. Fauvre
. 80% of the projects must meeting schedule and budget, and do it without redefining the content, or changing the goals - too many of our commitments end up being met in the "next release".	✓G. Plowman/ ✓E. Fauvre
*. Completion, installation and maintenance of a useful Software Engineering Policies and Procedures Manual.	✓G. Plowman

*High Priority

OBJECTIVE	RESPONSIBILITY
. Operational new development policies by June.	✓G. Plowman
. Perform comprehensive review of plans at the detailed technical level for rigid adherence to specification, standards, quality and reliability goals, and spec discipline.	✓G. Plowman/ ✓E. Fauvre/ ✓J. Mileski
Specific	
. Jointly, with Development and Planning Groups, devise and implement a system (the War Room) for tracking and displaying the plans, resources, commitments, and changes to the plan.	✓M. Woolsey
. Periodically, with the development manager, review development activities for conformance to the plan, and issue a report on the "state of development".	✓M. Woolsey
2.3 Upgrade the Development Technology/Methodology	
2.3.1 General	
. Rapidly develop a development methodology, including higher level languages, debugging and design tools and methods, appropriate machine access, with automated bookkeeping and librarian type aids.	
. Model and simulate new software.	
. Build in performance analysis tools.	
Specific	
. Thru Research, bring in at least 2 new products or process technological improvements each year.	✓J. Bell
. Develop and disseminate an applications technology with emphasis on methods and utilization of resources.	✓E. Fauvre
. Develop and disseminate a 3 year technology for diagnostics.	✓E. Fauvre
. Aggressively install mechanisms and procedures to aid in the execution and management of programming projects.	✓G. Plowman
. Better methods for module test program generation; growth in this area (manufacturing support) seems unreasonably high.	✓E. Fauvre
. A documented philosophy and methodology for setting Quality and Reliability goals, and designing, testing and implementing these goals	✓J. Mileski

OBJECTIVE	RESPONSIBILITY
2.3.2 General	
. All non-operating system development done in higher level languages.	✓ E. Fauvre/ ✓ G. Plowman
*. Short term - commitment to and plan for use of BLISS - develop list of criteria for use of BLISS on any specific project.	✓ G. Plowman
Specific	
. 90% of all applications work done in high level language.	✓ E. Fauvre
. Significant portion of all diagnostics done in high level language. (Manager to supply definition of significance).	✓ E. Fauvre
. Aggressive support for high level language (BLISS) development facility.	✓ E. Fauvre
2.4 Improve the Planning Process	
2.4.1 General	
. Definition and integration of the Systems Architect role.	✓ L. Wade
Specific	
. Develop a Systems Architecture function in order to achieve system-wide product cohesiveness, positioning, compatibility, efficiency and ease of implementation.	✓ L. Wade
2.4.2 General	
. Continuously reduce product support costs on a per-product basis. This includes all aspects of support, such as internal maintenance, field support, SDC costs for updates, etc.	
. No new product development without a long-range plan, covering new releases, updates, new versions, etc. Question - can we ever complete a product?	
. Clear, effective maintenance and support plans - how will we support our products in the field?	

*High Priority

OBJECTIVE	RESPONSIBILITY
2.4.3 General	
. Strengthen and formalize the inputs to planning and development.	
Specific	
. Have all new product starts approved by Products Committee.	✓ M. Woolsey/L. Wade
. Formalize the PSG process; meet at fixed frequency with clear agenda and intentions; formalize inputs from participating groups, and prepare formal quarterly reports of product requirements to the Planning and Development groups.	✓ M. Woolsey
2.5 Develop a Clear Uniform Process for Maintenance and Field Support	
2.5.1 General	
. Clarify our software maintenance process in support of new corporate software warranty.	✓ M. Woolsey
. Establish an "E.C.O." process for software.	✓ G. Plowman
Specific	
. Short term - analysis and proposal of the "Support Monster" problem.	✓ J. Mileski
PEOPLE/ORGANIZATION OBJECTIVES	
Improve Organizational Depth	
3.1.1 Specific	
. Implement the Advanced Development function by end of Q1, including at least 2 participants from the development organization.	✓ J. Bell
. Hire at least 4 technically superior individuals each year.	✓ J. Bell
. Provide an effective Departmental Planning function to plan and implement the resource (human, financial, hardware, space) and organizational (structure, methodology) requirements in support of Software Engineering goals.	✓ L. Wade

OBJECTIVE	RESPONSIBILITY
Specific	
. Develop effective Software Product Plans in support of Central Engineering and DEC-10.	✓ L. Wade
. Formalize the PSG process; meet at fixed frequency with clear agenda and intentions; formalize inputs from participating groups, and prepare formal quarterly reports of product requirements to the Planning Group.	✓ M. Woolsey
. Implement aggressive joing planning with the Product Management Group.	✓ G. Plowman
. Clearly document a statement of diagnostic trends in the industry, and long term plans for DEC diagnostics.	✓ E. Fauvre
*. Short term - Develop and establish as a corporate posture a simple, salable and achievable maintenance and support policy for our products (in lieu of "Warranty" statement").	✓ G. Plowman/ H. Spencer/ ✓ M. Woolsey
. Establish a competitive analysis activity able to evaluate current competitive products, and predict competitive moves.	✓ M. Woolsey
. Substantial upgrade in the line management structure.	✓ G. Plowman ✓ E. Fauvre
. Availability of skilled applications developers in each of the applications areas of major interest to the corporation.	✓ E. Fauvre
. Staffed and operational high level consulting role in Reliability Engineering applying a documented philosophy and methodology for setting Quality and Reliability goals, and designing, testing and implementing these goals.	✓ J. Mileski
3. Increase Emphasis on Individual Responsibility and Accountability	
3.2.1 General	
. Products debugged by the developers - neither field test nor Q.A. audit should be able to find more than a few infrequent bugs, and no catastrophic failures.	✓ G. Plowman/ ✓ E. Fauvre

*High Priority

OBJECTIVE	RESPONSIBILITY
Specific	
. Clarification of roles and responsibilities of the various management and technical levels - for example, do we use consulting programmers properly? Who develops implementation strategies? Who is responsible for absorption of new product technology?	✓G. Plowman/L. Wad
3.3 Improve Recognition and Participation for Key Software Development Personnel	
General	All ✓✓✓✓✓✓✓
. Build a high level team with increased visibility to the company so they be recognized, and who with increased visibility of the company, can operate from the broadest possible perspective.	
Specific	
. Prepare and maintain a menu of likely candidates for both Research and Advanced Development projects.	✓J. Bell
. Cycle at least 2 superior technical people each year from the research group into the Software Development activity.	✓J. Bell
. Cycle at least 2 superior technical people each year from the development activity into the Research group.	✓G. Plowman/ ✓E. Fauvre
. Participation in the "Advanced Development" activity.	✓G. Plowman
. Aggressive joint planning with the Product Management Group.	✓G. Plowman
. Development of a competent and visible management and technical staff in the applications area.	✓E. Fauvre
. Aggressive exposure to the Product Lines, Marketing Committee, OOD, etc., to help bring focus on growing applications activities in the corporation.	✓E. Fauvre

. OTHER OBJECTIVES

OBJECTIVE	RESPONSIBILITY
4.1 Improve Services to our Internal and External Customers	
PRODUCT MANAGEMENT	
Specific	
. Publish overall software business strategy guidelines for use of Product Managers and Product LIne Managers (use output from Ted Johnson's Committee).	✓ M. Woolsey
. Prepare business plans consistent to the Business Strategy guidelines, but above all with a sensitivity to our marketing requirements.	✓ M. Woolsey
. Continue to tighten ties with Software Services.	✓ M. Woolsey
HARDWARE ADMINISTRATION	
. Long term plan for supporting needs of software organization.	✓ E. Fauvre
. Increased service to the software developers, at decreasing cost to the corporation.	✓ E. Fauvre
. Proposal on development utilization alternatives.	✓ E. Fauvre
SDC	
. Automation of order picking - order processing	✓ O. Kostetsky
. Maximum of 1 week turnaround to customer orders.	✓ O. Kostetsky
. Regional SDC's where economically or politically appropriate, or where service required. Maximum of one week turnaround to customers.	✓ O. Kostetsky
. Priority system for field orders, including an "instan ship" option.	✓ O. Kostetsky
. Periodic (twice a year) evaluation of kit contents, costs, effectiveness.	✓ O. Kostetsky

Control (PL)	Peripherals (RP)	Systems/Arch (RC)	Software (LP)	Technical Staff (RLB)
• Formulate M/Buy better • Build total eval. system for M/B. (Rank all prod/proj) • Get EDP strategy / goals (also Soft.) • Streamline reports (use our C's)	• Implements work • Cabinet/PS strategy • Strategy in SmartT (LA36+) 000451	Integrate • multiple • Virtual Memory in all machines (78)	Language + Interpreter • Time sharing • TSS II • Network • Utils (files, info, long) • PL/1 ?	
		• Single K (controller) →	• Controller support	
		• Smarter K. →		
	• EMI, VDE, UL, etc. process .Field integrate, easy configuration. • Speed D/A, proto process • Mgrs, develop.	• build more ideas	• Improve t. response • Desc Soft. dept • Move more to applic. • HLL • Struct. prog. + shared code • Quality, reliable, useable	

(all)

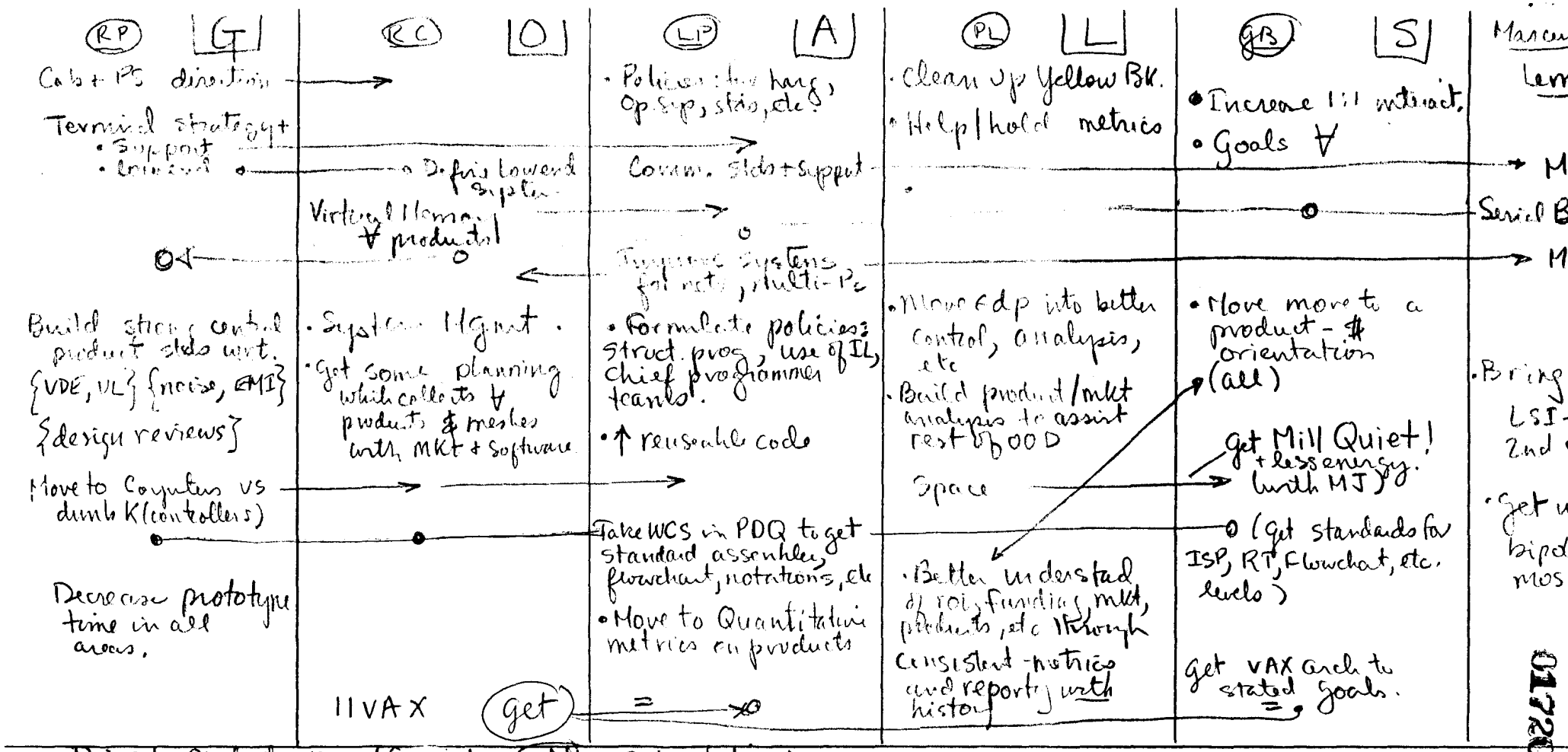
- Co-ordinate people, #, space, plans.
- Streamline processes, reports, etc.
- Develop / interact to get overall corp. system strategy (Including C in hand, table, desk)
- Know position ∀ Products ⊃ Move farther (esp. disks)
- Work together better
- Better documentation on O²D, PM, Eng. etc. processes.
- Hand C. Sys. Course
- more technical education
- Grow Mgrs.
- Get schools PM, Eng. Mgr.

(GB)

- Get Contract: KO, O²D;
- space process.
- Eng. Committee operate better
-

01719
1975
release

Possible 1974-1975 Goals for O²D — GB — Oct. 12, 1974.



- Drive to product-payoff orientation. (all)
- Educate OOD wrt each group: structure, goals, philosophy, control metrics
- Fix Product Approval process + document OOD Handbook
- Team - as needed (use Physnil) • Establish Architectural direction to assist individual gro
- Know Position ∀ products } { ∀ phases: Placement. • Clean up staff Mtgs.
  Clear delineation of funds for: study, proposal, design/tool, produce (support), Rejuvi
  Policy: Each group must have ∀ activity in each category.
- Establish productivity measures ∀ groups
  Joint evaluation of direct reports + clean up engineering levels.)
- Joint mtgs on state-of- engineering, products, technology, people, etc
- Quality: form metrics, in new design stds as # vs tradeoff
- ↑Systems focus: mgmt more direct, fund clearly in 2 dimensions
- Work standards especially to reduce costs, increase interconnectability, ease learning, dec
- Generally increase # of prototypes, while moving farther out
- Get ~ PDP-11's in use within OOD.

• Increase interact with MC
services + MH
includy lower noise (EM

02D Possible Goals? 75/76 GB Jun

01721

INTEROFFICE MEMORANDUM

TO:	Mark Abbett	ML12-1	DATE:	July 25, 1975		
	Gordon Bell	ML12/A51				
	Dick Clayton	ML5/E71	FROM:	Phil Laut		
	Henry Lemaire	ML1-2				
	Julius Marcus	PK3/M10	DEPT:	Engineering		
	Larry Portner	ML12/A62				
	Bob Puffer	ML1/E38	EXT:	4308	LOC:	ML12/A16
CC:	Bob Lander	PK3/F33				

SUBJ: FY76 Goals for Engineering Finance

The purpose of this note is to lay out my goals for discussion at the Jungle Meeting next week. It is a minor rewrite of my goals statement to Gordon and Bob Lander in May (#6 has been added).

Goals of Controller's Organization	Goals of Engineering Finance
1. Improve management decision through financial resources.	
A. Accelerated closing	Meet closing related deadlines
B. Measurements utilization.	Product Accounting (Statements distributed not more than 30 days following the end of the quarter by Nov. 1975.)
C. Utilization of PROFIT System	Continue to work with Finance EDP people to allow implementation of analytical tools designed for Product Accounting into GROMAR/PROFIT.
D. Improved forecasting techniques	Continue to work with Corporate Planning Group to allow pricing and costing of Product Line Forecasts
E. Improve profit planning	
2. Improve financial control system	
A. Accounting procedure manuals	Continue to improve documentation on engineering accounting and budgeting policies as needed
3. Improve corporate asset control/utilization/management	Considerable progress has already been made in controlling employee receivables and rotation inventory. FY76 goal is to understand current use and future needs for DEC-manufactured computers in Engineering.

Goals of Controller's Organization	Goals of Engineering Finance
4. Emphasize functional relationships within:	
A. Decentralized organization	Improve communication with Mfg. Finance
B. Establish and meet EEO goals	
5. Continue to build the Controller's organization	
A. Recruiting, training and development of personnel	Three major thrusts here. Intend to: 1) Increase the amount of reading done by the people in my group (me included) 2) Improve as needed, the clarity of writing done by people in my group. 3) Continue and expand the number of people going to school
6.	Co-ordinate Business Plans. This means encourage and prod product managers to do them, assist in the process, analyze them separately and in the aggregate. Observe, collect data and report on business and technical trends within the Company and in the rest of the industry.

/ale

INDIVIDUAL GOALS

LSI

1. Develop a realistic direction or strategy for LSI in the company. This will be accomplished by bringing together the thoughts of three functions:

   a. the systems user (the customer ex - LSI-11 disks, LA-36, etc.

   b. systems and circuit design (L. Gale)

   c. processing (J. Chenail, Worcester)

2. Define the particular devices which should be designed and LSI'd in the next three years. This is really a more specific definition of the strategy goal. It will demand an intense communication and understanding between the four groups.... systems user, systems designer, circuit designer, and process engineer.

3. Develop Worcester into a "going" processing operation of approximately 300 wafer starts/week by year end using both MOS and bipolar technologies. The processes will have manufacturing-level controls so as to be a state of readiness to manufacture high-volume, standard devices (ex - 4K RAMS) when the need is evident.

4. Bring the Engineering (Gale) and Manufacturing (Chenail) groups into an effective working team. This is always an important issue but absolutely indispensable in the semi world.

MEMORY

1. Engineering

   - All new memories 16K and under designed with MOS (4K RAM's).

   - Move deeper into total utilization of semi-memories (MOS, bipolar, CCD's).

- Start exploratory work on 16K MOS RAM.

- Use core for large systems - 32K, 64K, 2½D.

2. Product Management

- Develop this function beyond new product strategy, including a plan of developing an effective warning system and action plan to possibly modify product line forecasts. This will be accomplished by pooling data from memory groups, product manager, central planning, and Westminster.

- Phase out core memories and introduce semi memories in a controlled way. We neither want to "fall off the cliff" as cores drop off nor drag out cores when the market dictates that we should be using semi technology.

- Influence memory pricing strategy through Marketing Committee.

3. General

"Let go" of the memory operation so that in fact Cosgrove and Croxon together have 95% control of the business including issues which cut across organizational lines. This includes schedules, inventories, costs, but not systems engineering programs. These are the responsibility of Croxon only.

INTEROFFICE MEMORANDUM

TO: OOD LOC/MAIL STOP

cc: Henry Lemaire
Julius Marcus

DATE: July 25, 1975
FROM: Mark Abbett
DEPT: Central Engineering Personnel
EXT: 2633
LOC/MAIL STOP: ML12/A11

SUBJ: CENTRAL ENGINEERING PERSONNEL GOALS FOR FY '76

The following is a set of goals for Central Engineering Personnel to be discussed further at the July 30th Woods Meeting.

MANAGEMENT/EMPLOYEE DEVELOPMENT

Goals for Supervisor Training

- Core Workshops to continue for next six months with four modules including one on problem solving. All Central Engineering Supervisors to attend this program.
  Responsibility: John Cronkite Completion Date: 1/1/76

- Ken Trend to run two two-day Interviewing Skills Workshop for Central Engineering this Fall. Leo will participate in one, co-train the second, and be prepared to train future sessions.
  Responsibility: John Cronkite Completion Date: 11/15/75

- A one day workshop is to be designed for Supervisors on Techniques for Conducting a Performance Appraisal and Plan.
  Responsibility: John Cronkite Completion Date: 11/75

Goals For Management Training

- Run Engineering Managers Seminar again for the next level of management.
  Responsibility: John Cronkite and Ed Schein to train
  Completion Date:

- Have all managers attend a one day workshop on Techniques for Conducting Performance Appraisals and Plans.
  Responsibility: John Cronkite Completion Date: 11/75

Goals For Central Engineering Personnel Department Training

- An experimental Workshop will be run for the staff on Career Planning (What are factors that employees should consider in choosing a career)
  Responsibility: John Cronkite Completion Date: 4/76

Goals for Employee Development During FY '76

- o Selling of OOD in support of this effort.
  Responsibility: Mark Completion Date: 7/1/76

- o Development of a manual summarizing existing training for Central Engineering employees. This is to be distributed to managers and supervisors as part of our Performance Appraisal Workshop.
  Responsibility: Mark Completion Date: 10/1/75

- o The formation of a committee of individual contributors with the responsibility for administering a program of Employee Development for Central Engineering.
  Responsibility: Mark Completion Date: 6/76

Agreed Upon Guidelines for Relationship Between Management Development and Personnel Reps for Workshops

Workshop	Identification of Training Need	Design	Training	Follow Up
Corporate	Mgmt. Dev.	Mgmt. Dev.	Mgmt. Dev.	Reps
Central Eng.	Reps	Mgmt. Dev.	Reps	Reps

John Cronkite's Consulting Goals

A broad guideline for John relative to working consulting issues is that he designs programs to:

- o Resolve conlficts and problems with Central Engineering and other major organizations (i.e., 2 X 2, Engineering Managers)

- o Design programs to address issues and resolve conflicts between Vice Presidential organizations within Central Engineering (i.e., Product Management and Systems Management Workshops)

- o Act as consultant to Reps in resolving conflict issues within their individual organizations

EMPLOYMENT

- o The development of a comprehensive Manpower Plan for Central Engineering in conjunction with the Financial Reps. This plan is to include:

  a. Affirmative Action Plan
  b. January College Recruiting Plan

c. Co-op Hires
d. Minority and Female Training Programs
e. Plans for promotions and transfers
Responsibility: Leo Completion Date: 7/15/75

- Increase in minority and female applicants against committed Affirmative Action slots.

  a. A female and minority Employee Referral Program.
  Responsibility: Leo Completion Date: 2/15/76

  b. Better relationship with Minority Recruiting. This will include the invitation to Gas Riley whenever job spec meetings take place with managers.
  Responsibility: Leo Completion Date: 6/30/75

- Work relationship between the Personnel Recruiter and Personnel Representative as to further clarification of responsibilities.
  Responsibility: Leo Start Date: 10/1/75

- Hire a professional Recruiter and define the role of employment to include out placement, internal searches, reallocation of employees and career counseling when employees desire transfers to other organizations.
  Responsibility: Leo Completion Date: 11/1/75

- Monthly reports to be completed by the last working day of each month and sent to the Central Engineering Personnel staff and line management are to include:

  1. A Requisition Report of all full time internal and external openings for Central Engineering

  2. The top five Central Engineering openings and status of each

  3. An Affirmative Action Report to include how many committed openings, offers, and hires.
  Responsibility: Leo Start Date: 7/1/75

- With key individual searches (Level 11 jobs and above) and management openings, whether they be handled by an outside agency or Central Engineering Employment, an agreement be written up and bi-monthly status reports be sent to the managers, next higher level of management and Personnel Representatives.
  Responsibility: Leo Start Date: 7/1/75

COMPENSATION

- o Design and present a training session for managers dealing with Compensation philosophy. This session should include:

  a. The philosophy behind "Pay for Performance"
  b. The concept of frequecy of increases (how and when to use)
  c. The Exemption Questionnaire and a discussion of government requirements for qualifying as an exempt employee

  Responsibility: Jim McCarthy and Reps Completion Date:

- o Design and present a training session for all employees on DEC's Compensation Program. This training should include:

  a. What is a salary range?
  b. How does performance relate to salary range quartiles?
  c. What factor does cost of living play in the adjustment of salary ranges from year to year?
  d. How does job evaluation work and what factors are looked at in deciding the "worth" of a position?
  e. An explanation of the full process of performance and salary reviews at DEC.

  Responsibility: Jim McCarthy and Reps Completion Date:

- o A monthly report on Cost Center Manager's variance between salary plan and actual increases. This report should include a detailed analysis of each Vice Presidential organization and identification of problem areas.
  Responsibility: Jim McCarthy Start Date: 7/75

To start anticipating problems rather than reacting and fire fighting. This will be accomplished by our imput to compensation proposals through our Rep., Jim McCarthy, support of these proposals to our top management and Compensation's education of us to effectively implement these programs. Specifically:

- o During FY '76, Jim McCarthy and his Compensation Group will regularly attend Central Engineering's staff meetings to inform and involve us in all proposals. The goal is that our imputs be considered in these proposals and that we help sell these to our top management.
  Responsibility: Jim McCarthy and Mark Start Date: 6/27/75

- o Before any major compensation programs are implemented within Central Engineering, i.e., Phase I Salary Planning, AAIM Job Slotting, Stock Option Recommendation, etc., an educational program will be presented by Compensation to our Personnel Reps to ensure there is adequate knowledge in implementing the program.
  Responsibility: Jim McCarthy Start Date: Immediate

AFFIRMATIVE ACTION GOALS

- To have Managers complete an Affirmative Action Plan in conjunction with a manpower plan for each cost center for FY '76. This plan should include committed minority and female slots, training programs, co-op positions, transfers and promotions.
  Responsibility: Leo - Coordination, Reps - Implementation Completion Date: 7/15/75

- To set up a tracking system where managers quarterly receive a report of where they stand with relation to their Affirmative Action plans and commitments.
  Responsibility: Otis Courtney Start Date: 10/1/75

- To increase the number of minority and female applicants. The implementation and responsibility for this goal is covered under the Employment Section.

- To get a top management commitment and involvement in EEO through specific programs:

  1. Through quarterly reports on cost centers status versus their Affirmative Action plan, get Vice Presidents to come down hard on managers who are not obtaining their committed goals. This should be partially reflected in salary reviews and stock option recommendations.

  2. To budget a sum of money to be administered by OOD to support EEO programs beneficial to all of Central Engineering.

  Responsibility: Mark and OOD Completion Date: 10/1/75

- To develop two training programs to upgrade the skills of present minority and female DEC employees. A tentative plan would be to run another Tech Training Program and start a program for retraining employees to qualify for entry level Diagnostic Programming positions.
  Responsibility: Reps Completion Date: 3/76

- To complete the Employee Profiles and to use them as a resource for identifying promotable Affirmative Action candidates.
  Responsibility: Leo Completion Date: 2/76

EMPLOYEE RELATIONS GOALS

- Work with Vice Presidents and Managers to educate and prepare them for Personnel's effort in the area of Employee Relations over the next fiscal year.
  Responsibility: Reps Completion Date: 7/75

- o Employee Relations is management's responsibility and not Personnel's. With this perspective, our effort will be to develop specific programs to give managers more tools in order to develop an effective Employee Relations Program. Specific tools are:

  1. Available Technical Training for employees

  2. An awareness workshop on better secretary utilization

  3. A workshop on career counseling and alternative career paths for Central Engineering employees

  4. Other programs?

  Responsibility: Reps Start Date: 7/1/75

- o A program and training for managers on how to conduct Performance Appraisals and plans. Our goal is that every employee in Central Engineering have a performance evaluation every six months.
  Responsibility: Reps Start Date: 10/1/75

- o To develop one and possibly two social events for employees of Central Engineering. One program might be an open house for families of DEC employees and another possibly being a group sports activity such as a Red Sox baseball game.
  Responsibility: Theresa Start Date: 3/76

- o With the completion of the Employee Profile, to set up a mechanism for reviewing Central Engineering employees for all potential promotional and career path opportunities.
  Responsibility: Leo Start Date: 10/75

- o In areas of high hourly employee population (SDC and Engineering Services) to conduct an attitude survey with all employees. This will be an excellent opportunity for new Personnel Representatives to meet with the organization they're supporting.
  Responsibility: Reps Completion Date: Q2

ADMINISTRATION GOALS

- o To set up a policy for paperwork contained in an employee's Personnel File and set up all Central Engineering files accordingly.
  Responsibility: Policy: Theresa Completion Date: 1/76
  Implementation: PSA's

- o To complete a Secretarial Reference Book for use by all secretaries supporting technical organizations in Manufacturing and Engineering.
  Responsibility: Theresa Completion Date: 5/76

- Training for PSA's and Secretaries. The PSA's should visit John Hancock to get better insight into the mechanics of claims processing. With the decentralization of PSA's, Secretaries should be cross-trained so that they are qualified to cover the organization during times of vacation and absenteeism.
  Responsibility: Theresa Completion Date: 12/75

- To improve Central Engineering's New Employee Orientation. Areas to be looked at are:

  1. A film on DEC to give employees a better understanding of the products and business we're in.

  2. Clerical Training - To make new secretaries aware of forms, procedures, and DEC organization through a training program on their first day.

  Responsibility: Theresa Start Date: 8/75

clg

01732

INTEROFFICE MEMORANDUM

LOC/MAIL STOP

TO: Gordon Bell ✓
Bob Puffer
Henry Lemaire
Larry Portner
Julius Marcus
Phil Laut

DATE: July 29, 1975
FROM: Dick Clayton
DEPT: Computer Systems Development
EXT: 3638
LOC/MAIL STOP: ML5/E71

SUBJ: For OOD Woods - 7/31/75

Goals (For Major Focus in FY 76)

01733

I Product

- Understand where we build and sell systems vs components and strongly drive market, production, and development*
- Achieve realistic configuration rules
- Do fewer products better (increased risk & payoff)
- Get PDQ to market
- Get LSI to market & build solid successful family
- Successful 32 bit systems

II Process

- Integration of Product Management for Family Plans
- Evolution of System Management and focus* (implications across all development and market)
- Successful implementation of 32 bit management system across OOD*
- Focus on Reliability (Design and Process maturity, MTBF, etc.)
- Clarify Market Services role
- Strengthen PDP-11 & 32 bit Family forces (Platz, etc.)

III People

- Raise level and recognition of Product Managers*
- Bring in more bright college graduates
- Add 3 Product Managers-caliber of Steve, Bruce and Malcolm
- Raise technical training level
- Focus 70% of hardware engineers on minimum software skills (at least serious user)

IV Other

- Establish product specific competitive analysis
- 80% of Engineering Supervisors and above travel at least 3 weeks/year including one week in front of customers
- 70% of principle engineers & above travel 2 weeks/year including 4 days in front of customers
- Raise direct Product Line Eng. to 10% of total at least
- Build team strength and experience
- Execute cross group assignments for at least 10 people of supervisor or principle engineer level or above

*I believe these are also OOD wide goals.

September 3, 1975

Wes Graham, Director
Computer Systems Group
University of Waterloo
Waterloo, Ontario, Canada
N2L 3G1

Dear Wes:

I read the status report of WATFOR and WATBOL.

Can you send me brochures and/or material on them. Are they too restrictive (200 statements) to be useful? How are sales? How does WATBOL compare with our COBOL? How can the sales of these be improved?

Sincerely,

Gordon Bell
Vice President
Office of Development

GB:mjk

cc: Al Brown
Larry Portner

01735

Dept of
U of Waterloo
Waterloo, Ontario, Canada
N2L 3G1

Letter to Wes Graham at Waterloo

AUG 22 1975

August 15, 1975.

Dear Wes

I read the status report of the Waterloo WATFOR and WATBOL. Can you send me brochures and/or material on them. Are they too small restrictive (200 statements) to be useful? How are sales? How does WATBOL compare with our Cobol?

Mr. A. Brown
PK 31M12
OEM Group
Digital Equipment Corporation
146 Main Street,
Maynard, Mass 01754.

Dear Al:

It has been some time since we have reported to Digital Equipment Corporation about the status of our compilers for the PDP-11 series of computers.

We thought that you might be interested in the current developments, our plans for distribution and our plans for the next few months.

Attached to this letter are reports on WATFOR-11 and its extension WATFOR-11S and WATBOL-11 our new COBOL compiler.

If you have any questions about any of the details of the compilers or our distribution procedures, please do not hesitate to contact me.

Yours sincerely,

D.D. Cowan

DDC:cd

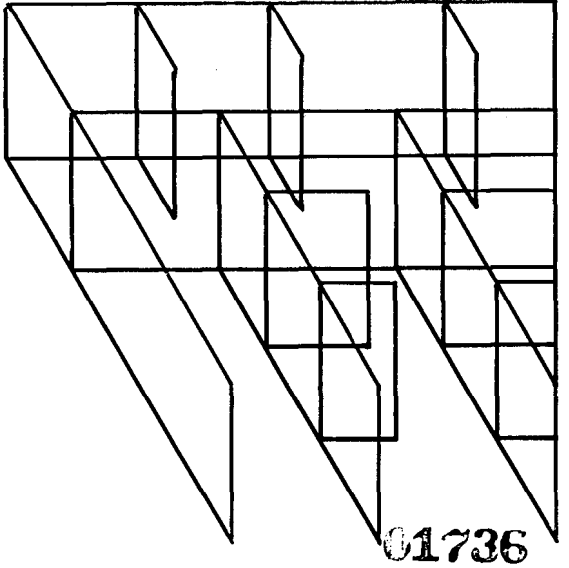
c.c. Mr. Gordon Bell.

cc: A Brown
L Porter
D Hardy

How can the Sales of these be improved?

WATFAC
Box 803
Waterloo, Ontario

*Waterloo Foundation
for the Advancement
of Computing*



01736

August 15, 1975.

PROGRESS REPORT

WATFOR-11 and WATFOR-11S.

WATFOR-11 has been completed and available for distribution since January 1, 1975. The compiler implements ANSI standard FORTRAN IV with format free I/O and other extensions. It compiles at very high speed with excellent error diagnostics.

WATFOR-11S is a version of WATFOR-11 which includes extra language features for structured programming. It contains the following constructs:

IF THEN ELSE,

WHILE DO,

and DO CASE,

as well as several other similar features. FORTRAN programs which run under the DEC FORTRAN IV compiler should also run under WATFOR-11 and WATFOR-11S and produce the same results.

Both the WATFOR-11 and WATFOR-11S compilers are available to be run under the RSX-11D and RSX-11M operating systems and will soon be available (Fall 1975) under the RT-11 operating system. The compilers use 24K of memory for the smallest configuration. Using this size of memory the compiler can accept about a 200 statement FORTRAN program. Of course the number of statements is highly dependent on the size of arrays. The compiler can be expanded to use a larger amount of memory and hence improve its performance both in terms of speed and size of program handled.

Specific details about these two compilers and the distribution package are attached to this report.

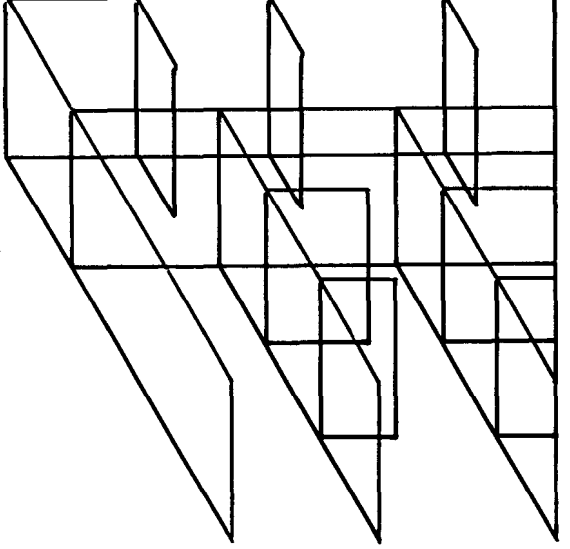
The distribution of the compiler is being handled in a straightforward manner - Upon receipt of a request, a distribution package is mailed to the potential user. The user completes the various forms and the contracts and returns them to WATFAC. WATFAC then copies WATFOR-11 onto DECTAPE or RK05 disk and sends the compiler to the user. The compiler is distributed as a number of object decks which can be combined to form a task by the receiving

installation. The object decks include WATFOR-11 compile-time and execution-time routines, additional object decks to create WATFOR-11S (if requested), built-in FORTRAN functions and the run-time support routines for formatted input-output. These last two items are part of the Digital Equipment Corporation FORTRAN Object Time System Version 4. By including the last two object decks our compiler is independent of various versions of the operating systems under which it is implemented.

The WATFOR-11 compiler is leased on an annual basis and at present costs $600 per year. The additional features for WATFOR-11S cost $100 annually.

WATFAC
Box 803
Waterloo, Ontario

*Waterloo Foundation
for the Advancement
of Computing*



August 15, 1975.

01738

PROGRESS REPORT

WATBOL-11

WATBOL-11 is a load-and-go batch COBOL compiler which is modelled after WATFOR-11. This compiler is designed for an environment where large numbers of small file-processing programs (i.e. educational institutions) are to be processed. WATBOL-11 compiles and executes batches of COBOL programs at speeds probably exceeding the speed of a 1000 line-a-minute printer or 1000 card-a-minute reader. Excellent diagnostic messages are issued to assist the programmer in detecting errors at both compile and execution time. The compiler is designed to be a minimum ANSI standard COBOL compiler with many extra language features. It appears to accept a richer version of COBOL then DEC's COBOL-11. Programs which run under DEC COBOL-11 should also run under WATBOL-11 and produce the same results.

The compiler is not quite complete although it presently will compile and execute a large number of COBOL test programs which exercise most of the language features.

We expect the WATBOL-11 compiler to be available for distribution on or before January 1, 1976. Initially it will be available under the RSX 11-D and RSX-11M operating system. It is expected that the compiler will require about 24K of memory for the smallest configuration and will accept at least a 200 statement COBOL program. Of course the number of statements is highly dependent on the size of tables and the number of files used. The compiler memory requirements can be expanded and as a consequence improve the performance in terms of both speed and size of program. A monitor is also being implemented which will allow a mixed job stream of WATFOR-11 and WATBOL-11 programs to be executed.

The distribution package for WATBOL-11 is not yet available. It is planned to distribute WATBOL-11 as a set of object decks on either DECTAPE or RK05 disk. These decks are then built into a task by the receiving installation. The object decks will include

WATBOL-11 compile-time and execution-time routines and the conversion, comparison and arithmetic run-time support routines. These last three items are from the Digital Equipment Corporation COBOL object time system. By including them the compiler is independent of the various versions of the operating systems under which it is implemented.

The WATBOL-11 compiler will be leased on an annual basis. Although the lease fee has not yet been decided we expect it will cost about the same as WATFOR-11.

digital INTEROFFICE MEMORANDUM

TO: Distribution

DATE: September 8, 1975

FROM: Gordon Bell

DEPT: OOD

EXT: 2236 LOC: ML12/A51

SUBJ: ASR CAPABILITY--WHAT IS IT?

I'd like to know how ASR's are used.

Do users keep the tapes? How long? Is the tape just a kludgy way to do editing? To get more throughput through a line? To pay less charges?

What I'm driving at is--why can't we build in page editry with say 4 to 8K bytes of RAM storage to hold the page and serve 90% of the ASR market? (This would solve the TWX and internal DEC network problems for example.)

GB:mjk

Distribution

Ed Corell
George Friend
Al Huefner
Andy Knowles
Roy Moffa
Bob Puffer
Mark Sebern
Tom Stockebrand
John Wolaver
Mike Wurster

digital INTEROFFICE MEMORANDUM

TO: Ron Ham
Pete Van Roekens

CC: Larry Portner

DATE: September 8, 1975

FROM: Gordon Bell

DEPT: OOD

EXT: 2236 LOC: ML12-1

SUBJ: DMS/11

Is DMS/11--a Data Base Management System for the PDP-11 by R. Hochsprung, as presented at the Fall 1973 DECUS--useful to our DMS/11 planning?

GB:mjk

01742

digital INTEROFFICE MEMORANDUM

TO: Steve Teicher

CC: Dick Clayton
Rob Van Naarden

DATE: September 9, 1975

FROM: Gordon Bell

DEPT: OOD

EXT: 2236 LOC: ML12/A51

SUBJ:

What are you thinking vis a vis a WCS and user ROM microprogramming?

GB:mjf

D I G I T A L INTEROFFICE MEMORANDUM

01743

PAGE 1

SUBJ: DATE CHANGE--LARRY ROBERT'S VISIT

DATE: 09-09-75
FROM: GORDON BELL
EX: 2236
MS: ML12-1/A51

TO: FILE

CHANGE IN MEETING NOTICE

To: Distribution

Larry Roberts, President of Telenet, will now visit us on October 24--many of you were going to be out of the country on October 1.

October 24, 1975
Time: 10:00 AM until 3:00 PM
My office

Purpose: to convince us that an interface to Telenet is an important and profitable product.

There are three areas of interest that I believe are being attend to already:

1. 10 interface via DAS10.
2. Communications products.
3. Standard networks or other products (e.g. RSTS).

Please arrange to have a spokesman from one of these areas in attendance (e.g. Pearson, Alusic, Teichholtz).

I will attend:---

I will represent:---

GB:mjf

Distribution

Don Alusic	Stan Olsen
Bob Klein	Stan Pearson
Irwin Jacobs	Nat Teichholtz
John Leng	Larry Wade
Julius Marcus	Stu Wecker

D·I G I T A L INTEROFFICE MEMORANDUM 01744

PAGE 1

SUBJ: MEETING NOTICE--10/2, LASER-SCAN LI DATE: 09-09-75
FROM: GORDON BELL
EX: 2236
MS: ML12-1/A51

* *
TO: FILE
* *

MEETING NOTICE

To: Distribution

Mr. Street, Laser-scan Limited, will be visiting us on October 2. The attached letter will explain his visit and more information will be coming.

Pending Mr. street's confirmation, the meeting will be held:

Date: October 2, 1975
Time: 1:00PM
Place: My office

I will attend:---

I can't make it:---

GB:mjf

Distribution

Leo Bennett
Ed Corell
Len Halio
Bill McBride
Mark Sebern
Tom Stockebrand--host
Phil Tays
Ed Vrablick

01745

LASER-SCAN LIMITED
Registered in England No. 966312
VAT No 213 8605 79

Tel: 0223-69872/4
Telex: 817346

Cambridge Science Park, Milton Road, CAMBRIDGE CB4 4BH, ENGLAND

AUG 28 1975
8-36

13th August 1975.

Professor C.G. Bell,
(V.P. Engineering),
Digital Equipment Corporation,
Maynard,
Mass. 01754, U.S.A.

Dear Professor Bell,

I hope you are well. You may remember that some time ago we met when you visited the Computer Laboratory in Cambridge, and saw the HRD-1 as it then was. At the time you were quite interested in this equipment for your own purposes, but unfortunately, we were too late for particular provision which had just been made to obtain micro-film equipment.

As I shall be in your area during late September, I would very much welcome the opportunity of visiting your establishment and discussing with you some of the possibilities for our Company and its equipment as they now stand.

The earliest date on which I could visit you would be Friday, 26th September, but preferably it would be during the following week, say between October 1st and 6th.

I do hope you can give me two alternative dates at either end of this period, which would suit you.

Yours sincerely,

Graham Street

G.S.B. Street
Director.

G. BELL
PAGE FARM RD.
LINCOLN, MASS. 01773

Visitors
Seborn
Stody
Bennet
Krablik
Holic
McBride
Tays
Torell

01746

TT
VOB NOT E
LASERSCAN CAMDG
00002 DEC CH
KZ

PPRR 1321 09-SEP 25371 1319 PDASLP
MP3C FORN

ZCZC
817346 - ENGLAND
MSG NO NA31

TO: G H STREET - DIRECTOR
LASER-SCAN LTD.
CAMBRIDGE SCIENCE PARK
CAMBRIDGE , ENGLAND
TELEX NO. 817346

I RESERVED TIME ON OCTOBER 2, 1975, AT 1:00 P.M. PLEASE LET ME KNOW THE AREAS YOU WOULD LIKE TO DISCUSS SO I CAN ALERT SOME OF OUR PEOPLE. ALSO, PLEASE SEND PRODUCT UPDATE INFORMATION.

FROM: GORDON BELL - DIGITAL EQUIPMENT CORPORATION
MAYNARD, MASS, U .S.A

REGARDS
J
NNNN
NNNN

D
LASERSCAN CAMDG

digital INTEROFFICE MEMORANDUM

TO: Distribution

CC: OOD

DATE: September 12, 1975

FROM: Gordon Bell

DEPT: OOD

EXT: 2236 LOC: ML12/A51

SUBJ: DDCMP, et al STANDARDS

In talking with Adm. Haak, who buys and installs computers for the Navy, his group strongly suggested we nominate DDCMP and the network protocols as standards to ANSI and CBEMA.

What can we do here? What do you think? Nat, will you come forth with a proposal or statement?

GB:mjf

Distribution

Larry Portner
Nat Teichholtz
Larry Wade
Stu Wecker
Pat White

digital INTEROFFICE MEMORANDUM

TO: Ron Ham
Larry Portner
Pete Van Roekens
Larry Wade

DATE: September 12, 1975

FROM: Gordon Bell

DEPT: OOD

EXT: 2236 LOC: ML12/A51

SUBJ: PROGRAM CONVERSION

In visiting US Navy people, they were concerned about conversions of programs from IBM and Honeywell. There's a major problem when DBMS-type systems are used, since these contribute to incompatibility.

Can we: What's the thinking here?

GB:mjk

digital INTEROFFICE MEMORANDUM

TO: Distribution

DATE: September 12, 1975

FROM: Gordon Bell

DEPT: OOD

EXT: 2236 LOC: ML12/A51

SUBJ: INTERESTING PERSPECTIVE ON OP.SYS.MODS

In talking with people from the Navy, they stated they forced a vendor who had benchmarked a system and given a certain performance, to give free hardware when the Op.Sys. had been enlarged and the performance decreased.

GB:mjk

Distribution

Pete Conklin
Dave Cutler
Roger Gourd
John Levy
Larry Portner
Larry Wade
Pete Van Roekens

digital INTEROFFICE MEMORANDUM

TO: Jim Bell
Mark Sebern
Stu Wecker

DATE: September 12, 1975

FROM: Gordon Bell

CC: Andy Knowles

DEPT: OOD

EXT: 2236 LOC:ML12/A51

SUBJ: CONSULTING WITH UMASS VIA HAROLD STONE

Since Harold Stone consults for HP, we should be careful with our own interaction with him. Are we going to, or do we want to build a relationship with him?

GB:mjk

digital INTEROFFICE MEMORANDUM

TO: Distribution

DATE: September 12, 1975

FROM: Gordon Bell

DEPT: OOD

EXT: 2236 LOC: ML12/A51

SUBJ: LASER PRINTERS

HP has taken licenses with Canon and Spectra Physics (?) for their printers. The copies are pretty. IBM is apparently working like crazy too on this.

I believe these all require a dry photographic process. What have we thought about here?

Should we get together to see what is known? Wouldn't Polaroid be the ideal company to work with?

GB:mjk

Distribution
Jim Bell
Ed Corell
Bob Puffer
Ken Olsen
Mark Sebern

D I G I T A L INTEROFFICE MEMORANDUM

SUBJ: DEC HANDBOOKS
DATE: 09-17-75
FROM: GORDON BELL
EX: 2236
MS: ML12/A51

TO: FILE

To: Distribution

SUBJ: PRICES AND STRUCTURE OF OUR HANDBOOKS

I keep getting promises from my friends in academia who teach the PDP-11 to stop buying it because the manuals are numerous and expensive.

Dan Siewiorek, Professor of CS at CMU, wrote a book to explain the PDP-11 (and data structures), but recently called me when the price to students go to be $14 ($4.50 for processor handbook and $9.50 for CAPS).

If the costs are indeed this high, can we give universities the plates to reprint them? Are we modular at the wrong level? Will new language and command standards help make the fabrication, etc. easier? Aren't we better off being less modular here? Is microfiche a possibility?

Is this just a problem in our small EDU market? Are there other quantity users?----------
Who's responsible for manual structure planning and pricing?----------

I view that this was only solved once in the old PDP-8 handbook that had everything. Now we've blown it there.

GB:mjf

Distribution

Dick Clayton	Ed Kramer
Dick Eckhouse	Ken Olsen
Bob Gafford	Larry Portner
Win Hindle	Charlie Spector
John Jones	Larry Wade
Olen Kostetsky	Gerry Witmore

SUBJ: EDITORS

DATE: 09-17-75
FROM: GORDON BELL
EX: 2236
MS: ML12-1/A51

TO: FILE

To: Distribution

Subj: ANOTHER ------ EDITOR, NUTS

At the VAX meeting today I heard that there's to be another editor for VAX, with different syntax, etc. Please, please, please don't give us another editor! What I see for the hard-copy editors:

0. TECO--most compatible among 8, 10, 11 (don't know about 15). Is strongly liked and disliked. Not useful for novice. Probably will get on VAX due to the strong likes. Turns out to be useful for certain kinds of users.

1. BASIC editor as part of languae.

2. EDIT evolving to SOS--10 and now on 11. Line #'s proven as an editor in a variety of user environments.

3. RSX 15 and 11 Editor--not line # oriented. Seems OK.

4. Editor in BASIC by Ken King

5. CCA Editor to be used in message switching/WPST system being installed at DEC.

6. ? for 8

7. VT61 Editor

8. Proposed (HELP) new editor

The tube editors:

0. All of the above.

1. VTED on the 10.

2. VT21 editor for typesetting.

3. New word processing editor.

SUBJ: EDITORS

DATE: 09-17-75
FROM: GORDON BELL

01760

To my knowledge, there's only been 1 study on the subject of performance for editors. Ken King has a copy of the results, but it looked roughly:

1. For text input, nothing matters

2. for editing the tube is best by X2--point to the stuff rather than describe where it is.

3. for string edits, TECO gets about 30% over others due to terseness--etc.

4. The string editors, SOS, QED, the multics editor are all about the same for corrections.

Also, there's a problem for doing text typesetting in a coherent, formatted way.

Where are we going here? Can I see a plan/statement of problem? Who's driving it? Given that we're understaffed by 30% in languages, why are we looking at a new editor?

It would also be nice to have a standard syntax for the editors we have that are implemented across machines and systems: the SOS, TECO, VTED, NEW-edit? What's happening on this?

GB:mjf

Distribution

Peter Conklin
Jack Gilmore
Ron Ham
Tom Hastings
Ken King
Larry Portner
Pat White

D I G I T A L INTEROFFICE MEMORANDUM 01761

SUBJ: AGENDA/MINUTES OOD

DATE: 09-04-75
FROM: DICK CLAYTON
EX: 3638
MS: ML5-2

TO: -OOD

SUBJ: OOD STAFF AGENDA--9/4/75

10:30	Review Minutes	
10:35	Review asenda	
10:40	Product Line Msr. Dinner Meetings	Portner
11:00	Business Plan Review Procedure	Laut
11:30	Product Managers Review	
	Job description	Abbett
	Green Sheet	Portner/Clayton
	Overall organization perception	All
12:15	Assignment of Best/Noelcke	Puffer/Clayton
12:30	Role of OOD Secretary (rotation)	All

FUTURE AGENDA ITEMS

When do we want to finalize capital & operating budgets?

9/11	OOD-MKT Committee interface	(40 min.)	
9/11	Sales meetings (especially Spain)	(10 min.)	Clayton
9/11	Status of microprocessor project	(15 min.)	John Hughes
9/11	What is our affirmative action status and what problems are key for next 12 months	(30 min.)	Abbett
9/11	What is PDQ status and what have we learned?	(15 min.)	Demmer
9/18	What is the purpose, form, and content of the upcoming MIT lecture series?	(30 min.)	Puffer/ Cronkite
9/18	What is 3 year serial bus strategy?	(20 min.)	Bastiani/ Clayton

SUBJ: AGENDA/MINUTES OOD

DATE: 09-04-75
FROM: DICK CLAYTON

9/18	What is resolution of DEC 20 memory strategy	(20 min.)	Lens/ Lemaire
9/18	OOD space guidelines	(60 min.)	out 9/25
9/25	Report on in house 2 year PDP-11 usage strategy.		Computer Resource Co.
9/25	QCMS defect reporting system		Smith/Pecore
Sept.	Is there a field integration plan yet?		Smith/Shields/ RC/RP
Sept.	Honoraria Policy		Bell
10/9	Is there a formal action plan that allows follow up on field oriented product safety problems?		Shields/ Minezzi
Oct.	Block mode strategy resolution		Marcus/Portner
?	Is action on ECO control called for at this time?		Marcus
?	What is happening to make systems a reality in the way we do business?		Clayton

Expected attendance at OOD meetings:

	GB	LP	RP	RC	PL	MA	JM	HL
9/04	X	X	X	X	X	X	out	X
9/11	out	~~out~~	X	X	X	X	X	X
9/18	X	X	out	X	X	X	X	out
9/25	X	X	X	X	X	X	X	X
10/2	X	X	X	?	?	X	?	X
10/9	X	X	X	X	X	X	X	X
10/16	X	?	X	X	X	X	out	X
10/23	X	X	X	?	X	X	X	X
10/30	X	X	X	X	X	X	X	X

Sept 11, 1975

01770

KEY MANAGEMENT ISSUES

(OC. Agenda)

Terminal Strategy **	Knowles/Puffer	Decided, managers needed
Discount Policy	Johnson/Michels	In process
Software Business Strategy	Johnson/Portner	In process
? Memory Strategy	Johnson	Partially decided
Competition with OEM	Hindle/Long	Awaiting write-up
Low Cost Selling Strategy	MC	In process
Transaction Processing	Portner	In process
IAS	Portner	Open
Marketing Function *	MC	Stalled
Mil Spec 11	Clayton/Buckley	Dick owes alternatives
Low end printer	Stockebrand/ Correll	September 1
Low end CRT **	Gale, Halio, Sebern	Open
Product Line/Field Org. *	OC	October Woods
Red Book Update	Bell	Open
Commercial Product Strategy	S. Olsen	Open
~~?~~ Combined 11/70, VAX & 2040 Strategy (MKt. - assigned to Levy / Hindle / Carnes)	OC	Open

9/16

****

FUTURE AGENDA ITEMS

Catalog GMO Review	Knowles	March 76
Mid & Large Operating System Strategy	Bell	Open
DEC Tablet	Johnson	Open
Industrial OC Concerns	Vachon	Open
Central Vs. PL Software Dev.	Portner	Open
MC/OOD Interface	Laut/Thompson	Open
Company Chaplin/Shrink	Burke	Future Woods Topic
Organization-how to avoid 15 layers	All	Future Woods Topic
Benefits Overview	Bornstein	September
Test of Space Assumptions	Crouse/Thompson	Open
High Potential People & Quarterly Letter Items	Burke	November Woods (with interim discussions)
Info Sent to Field	All	September 22

3/12

digital

INTEROFFICE MEMORANDUM

01771

TO: Gordon Bell

DATE: September 10, 1975
FROM: John Fisher
DEPT: Administration
EXT: 4515
LOC/MAIL STOP: ML 12/1 A-50

SUBJ: MID & LARGE OPERATING SYSTEM STRATEGY

SEP 11 1975

At the Woods Meeting we held at Stan's home you agreed to return to the OC with a strategy for holding together Mid and Large Operating Systems Strategy. I continue to carry this as a future agenda item for the OC and I sense that there are many people, including Marcus, Portner, Clayton, etc. who feel it needs to be resolved. Where should be go from here?

SUBJ: INTERACTION OF OOD AND MARKETING COMMITTEE (Phil / Bill) — Aug 26

I am still waiting for your writeup of how the OOD and MC should play together in making Corporate Product/Market decisions. This was requested by the OC some months ago and I believe it is of significant importance that we should consider its publication as a "Green Sheet". Today, I don't think anyone in DEC could explain clearly and simply how we decide on designing and introducing a new product.

SUBJ: CHEAP CRT (~~Stan~~ Bob / Dick) — Aug 26

At the last Woods Meeting there was consensus of the pressing need for a cheap CRT. Gale, Halio and Sebern were going to set up a special study group to make this happen. Also, at the 8/25 OC meeting, Puffer explained that he is looking for a new Product Manager to drive this. Andy is looking for a strong Marketing Manager to define a winning market strategy. Apparently there is much confusion about where we are going and the study group which you promised to set up has never materialized. You will recall Ken's feeling that genius was necessary to pick a unique product strategy, and I think everyone was hoping that this might come out of the Gale/Halio/Sebern team.

Should we continue to push for this?

DIGITAL

INTEROFFICE MEMORANDUM

01772

TO: Gordon Bell ML12-1/A51
John Fisher ML12-1/A50

DATE: September 4, 1975
FROM: Ken Olsen
DEPT: Administration
EXT: 2300
LOC/MAIL STOP: ML12-1/A50

SUBJ: REVIEW OF 32 BIT MACHINE

In addition to the periodic general reviews of all major projects with the Operations Committee, I think we should spend a half hour or one hour on specific projects.

I think it is time that we spend a half hour on a casual review of the 32 bit computer. Will you schedule a review of this soon?

I think this should be without slides, flip charts, or formal presentation, but should be just a casual review of what has been going on. In general terms, we should know how long it will take, what impact it will make, whether it will wipe out the PDP-10 or will the PDP-10 wipe it out, or whether the two can live compatibly forever. We are particularly interested in how compatible it is with the PDP-11 software.

It seems to me that our original goal was to make this machine, 1) compatible with the 11, and 2) accomplish all the wonderful things that new design makes possible. It will be good to review how we have deviated further from this goal and what we have gained by this deviation.

/ma

01773

September 3, 1975

Professor James Snyder
Computer Science Department
University of Illinois
Urbana, Illinois 61801

Dear Dr. Snyder:

We sadly regret the death of Professor Don Gillies of your department--a pioneer computer scientist, who has been active throughout the life of computing. His students (here) remember him as really bright and inspiring. I enjoyed the interaction with him on his Pascal language work.

It is therefore with mixed feelings that I enclose a check for five thousand dollars ($5000) on behalf of Digital Equipment Corporation to be used for an annual commemorative lecture series. However, we feel in this small way he can be remembered and computer science learning can partially continue in his name.

As the details of the series become firm and operates, we would like to follow it.

Sincerely,

Gordon Bell

Gordon Bell
Vice President
Office of Development

GB:mjk
cc: David Kuck
Enclosure

DIGITAL EQUIPMENT CORPORATION, 146 MAIN STREET, MAYNARD, MASSACHUSETTS 01754
(617)897-5111 TWX: 710-347-0212 TELEX: 94-8457

D I G I T A L INTEROFFICE MEMORANDUM 01774

PAGE 1

SUBJ: FPLA'S FINALLY DATE: 09-23-75
FROM: GORDON BELL
EX: 2236
MS: ML12/A51

* *
TO: FILE
* *

To: Distribution F/U 9/30

It just occurred to me that these devices which are now being introduced offer an interesting alternative to what would have been random logic on PCB's. They offer lots of interesting alternatives to conventional ROM's too.

Is anyone thinking about some of the uses?

Who can carry out an analysis to see if it works as a means of affecting testability, stocking, PCB area reduction?

Could we get a seminar here to expose and recommend?
Who should do it?

GB:mik

Distribution

Engineering Managers
Bob Armstrong
Michael Depevrot

D I G I T A L INTEROFFICE MEMORANDUM 01775

PAGE 1

SUBJ: DATA BASE/5100 DATE: 09-25-75
FROM: GORDON BELL
EX: 2236
MS: ML12/A51

* *
TO: FILE
* *

Subj: ALL THOSE TINY DATA BASE PROBLEMS CAN BE DONE ON A 5100

To: Distribution

The IBM hardware language, and interface, is ideal to tackle all those tiny, turnkey data-base applications that there are millions of:

1. Pharmacy record control
2. Doctor's office
3. Dentist's office
4. Simple tax form filling out.
5. Automobile pricing, financing, etc.
6. DEC field office inventory, computer configuring.

How will they go about doing applications and selling it? Will distributors spring up? People who sell fixed applications programs?

GB:mjk

Distribution

Operations Committee
Product Line Managers
Jerry Todd

[redacted]

[redacted]

01777

Janice Carnes
Dick Clayton
Bill Demmer
Bob Kirk
Clay Neal
Al Ryder
Bill Strecker

[redacted]

D I G I T A L INTEROFFICE MEMORANDUM

SUBJ: ROM MICROCODE

DATE: 10-01-75
FROM: GORDON BELL
EX: 2236
MS: ML12/A51

* *
TO: FILE
* *

Subj: INCREASING SIZE OF ROM MICROCODE ON PDP-11'S VERSUS TIME

To: Distribution F/U 10/10

It's clear we've really (in retrospect) missed opportunities to easily mid-life kick all our processors as bipolar ROMS have gone from 1K to 2K. Now when they go to 4K (1 to 2 years) can we easily retrofit, to get double the microcode in the same board space without retooling, etc?

Lloyd Dickman is putting the VAX string stuff in 11/03. Are these candidates for 45, and 70 (which don't yet have the new 2K ROMS)?

Are there other operations to help these machines now?

Should we conscientiously plan this on new designs...it's only an extra bit in micro PC?

Please comment.

GB:mjf

Distribution

Bob Armstrong
Jega Arulpragasam
Dick Clayton
Ed Corell
Bill Demmer
Lloyd Dickman
Duane Dickhut
Len Hughes
Chuck Kaman
Bob Kirk
Jim O'Loughlin
Steve Rothman
Al Ryder
Bob Stewart
Tom Stockebrand
Steve Teicher
Mike Tomasic

01786

digital INTEROFFICE MEMORANDUM

TO: OPERATIONS COMMITTEE

DATE: September 22, 1975

FROM: Gordon Bell

DEPT: OOD

EXT: 2236 LOC: ML12/A51

SUBJ: IBM 5100

Attached are the handouts submitted for the Operations Committee meeting today regarding the above subject.

GB:mjk

GB 21 Sept 1975

Wants

0. Who's doing compet. Eval. – 5100?

C1787

1. Hardware-level

VT5X + Table top Cab (AK) now → VT5X Repackage ↑ J.C. integrated tube } Integrated + new VT5X

OR

OR

VT5X → VT5X Repackage (dumb)?
Table Top Cab (AK) → Complete module package. } Modular

- Tube sizes.
- 1 Floppy vs 2 in basic pkg. gets size down.

2. Software-level.

- Evaluate 5100
- Move to clean up / simply RT interface

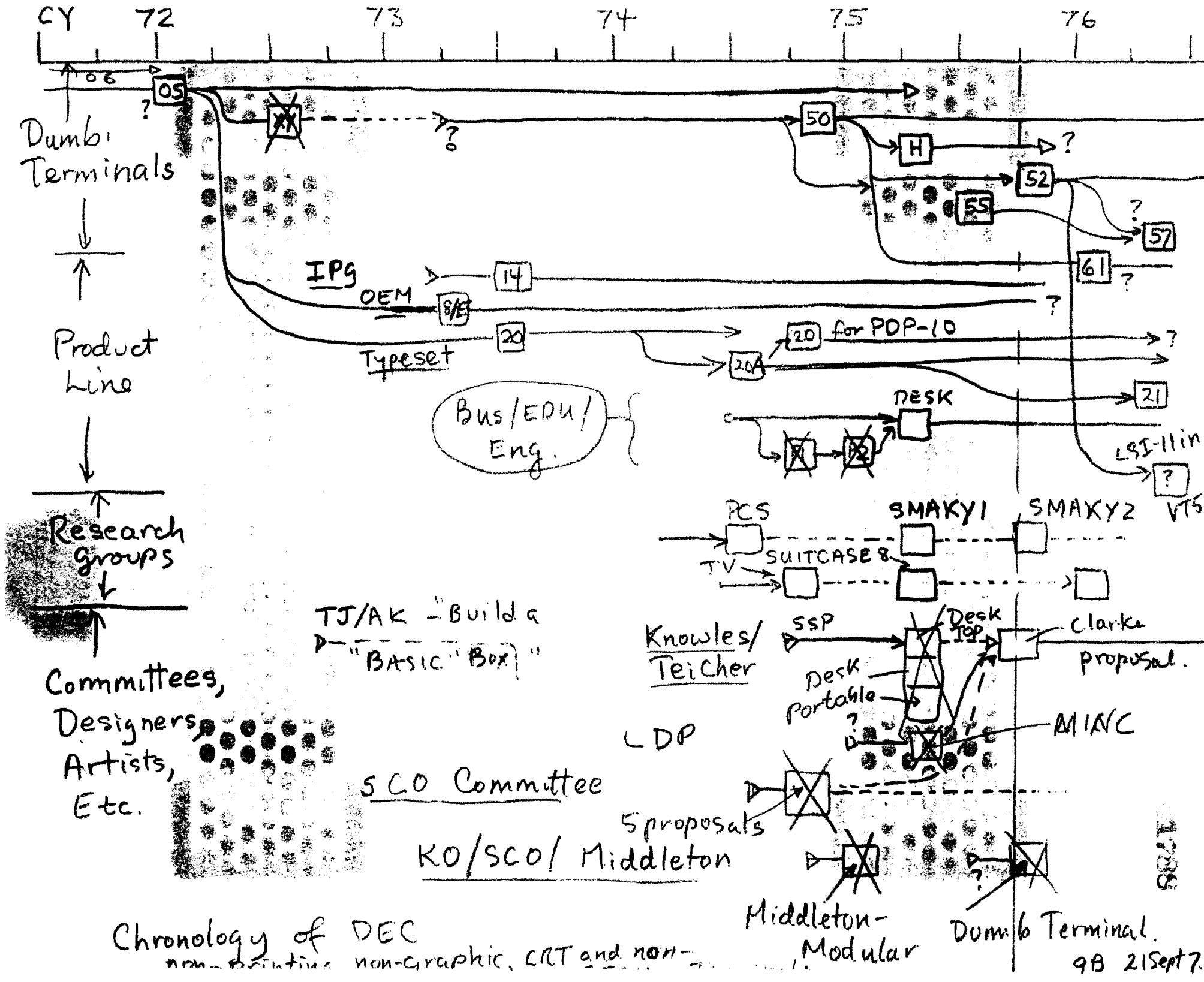
3. Applications

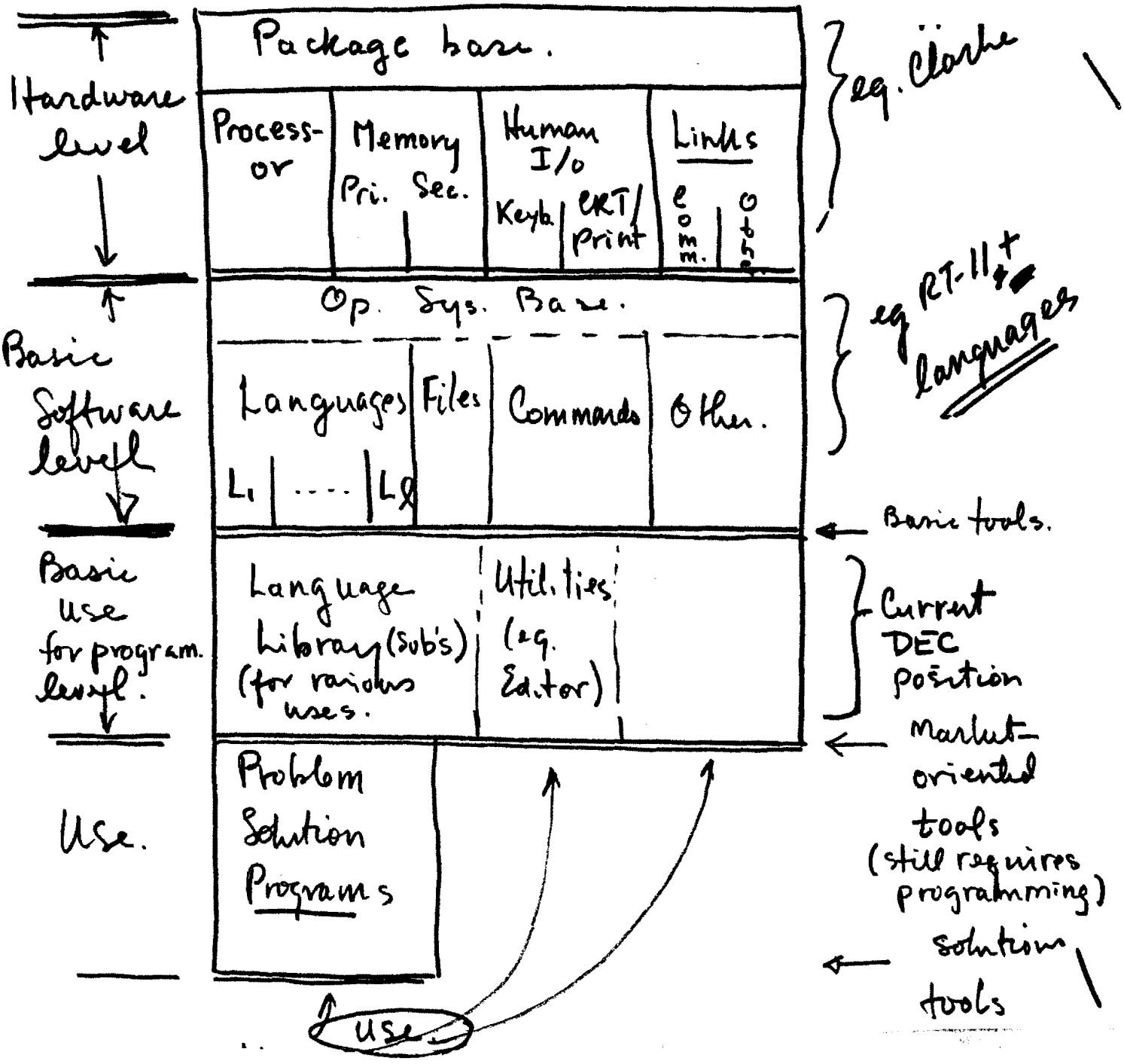
- Concerted / co-ordinated effort.

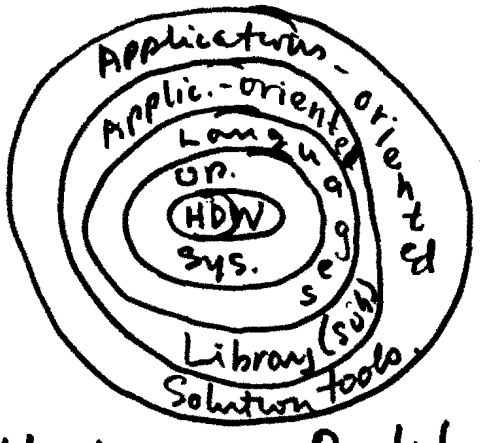
4. [redacted] Specific

VT61 vs (VT52+LSI-11)

5. Program MGMT


CY
72
73
74
75
76
06
05
?
Dumb Terminals
Product Line
Research Groups
Committees, Designers, Artists, Etc.
XX
?
50
H
?
52
55
?
57
61
?
IPG
OEM
14
8/E
?
Typeset
20
20A
20 for PDP-10
?
?
Bus/EDU/ Eng.
DESK
21
LSI-11in
?
VTS
PCS
SMAKY1
SMAKY2
TV
SUITCASE 8
TJ/AK - Build a "BASIC" Box
Knowles/ Teicher
SSP
Desk Top
Clarke proposal.
Desk Portable
?
MINC
LDP
SCO Committee
5 proposals
KO/SCO/ Middleton
Middleton-
Modular
Dumb Terminal.
Chronology of DEC
non-graphic, CRT and non-
9B 21Sept7





Levels of Machines - Partitioning

gB 21 Sept 197

	IBM 5100		DEC
Price		<	Does it matter?
Package	Portable; a bit big to move. Too big to move if programming (i.e. extra tape, printer).	>	Movable in small area. Can't be moved by programmers Small floppy makes ≡ possible in >2 years.
Service	?	>	Possibility exists for "user" replacement of modules.
Desk-top size	Still big.		VT5X is big; LA36 is fine. Modular or smaller CRT would get us a lot.
CRT graphics	Small No upper case?	= < << <<	Good sized. Could help us vis a vis word processing. VT57 would give plotting Clarke's is extensive
Hard copy	Printer 60#	< =	Copier + printer Bigger for printer
Keyboard	Overlays may help	=	
Processor + Performance	? (Could be a very fast 16-bitter, i.e. 6 micro-s/16-bits discussed)	=	PDP-11 (enhancements for F.P. + strings would help)
COMM interface	2741 This could give a way to other i/o	<	We have more--not clear about support.
Other i/o	Not announced. Clearly not needed.	<<	We have lots.
Processor features	? ?	<< <<	Interrupts permit real time i/o and; multiprogramming (for multi-terminals)
Primary Mem. RAM ROM	 Up to 65K bytes (in 2K chips) ≥65K bytes?	 = >	 65K bytes This could give us trouble!
Secondary Mem.	Tape Slow--90 sec. worst case.	<< —	Floppy We could get a user throughput of > 10~20% ∴Showing high productivity Enables Virtual Memory (potentially)

APL	YES (CLAIMS 4X SPEED UP OVER COBOL FOR BUS.)	>	? AT OMSI
BASIC	YES	>	NOT CLEAR HOW OURS STACKS UP? LIBRARY?
COBOL	--		COULD PROBABLY GET
DIBOL	--	<	YES--HOW WELL DO THE 90% OF THE WORLD'S) PROGRAMMER'S (COBOL) TAKE TO IT?
MINI-COBOL	--	>	ARE GETTING. DO WE WANT IT?
EDITOR	?		
FOCAL		<	GOOD APPLICATION LIBRARY
FORTRAN		<	WORLD'S SECOND MOST POPULAR LANGUAGE.
MACRO			YES...BUT FOR WHAT CLASS OF APPLICATIONS
PASCAL			YES--COULD GET
RPG			YES
AS A TERMINAL	2741		WE COULD

GB
9/22/75

HUMAN INTERFACE	SMALL CRT, REGULAR KEYBOARD WITH SPEC. FUNCTIONS	TYPEWRITTEN COMMANDS WILL PROBABLY BEAT IBM APPROACH. FLOPPY HELPS RESPONSE A GREAT DEAL!
MANUALS		> WE HAVE NONE FOR NOVICE.
POTENTIAL APPLICATIONS	GREAT; BUT SOMEWHAT LIMITED BY TAPE AND POSSIBLE LACK OF LOWER CASE. APL WILL RAISE LEVEL OF COMPUTING	> PORTABLE AND APPLICATIONS
	?	< REAL TIME MULTIPROGRAMMING.
	?	< MULTI-TERMINAL
	KEYPUNCH REPLACE	≈

GB
9/22/75

Bill Munson
18 Sept 1975

01793

IBM 5100 RESPONSE

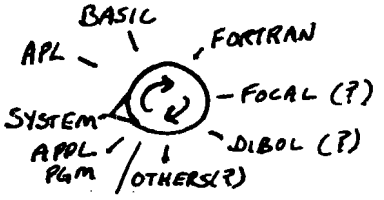
Re: Operating System (ie. RT-11), Languages and Human Interface

1. System Startup

   A. Operation

   - Thumbwheel selection of language or root system or application program on media, i.e.,

note extensive languages



Editing (ie word processing)

   - Depress BOOTSTRAP
   - Selection sets bits on bus accessible to bootstrap which loads requested module (or error halt)
   - Machine now set to environment selected
   - ? Allow chaining to another environment, or require re-boot? may allow some options depending on floppy space and/or other configuration parameters.
   - ? Automatic setting of keyboard interpreter to language/system selected? (i.e., APL keyboard, function keys?)

   B. Cost/Schedule

   - Should be fairly trivial, straightforward modifications (S/W guess on H/W); 1 month

2. User Command Language

   A. Description

   - Current RT-11 unacceptable
   - Need English language, straightforward set
   - Could be function keys, or keyboard entry
   - Might permit access to RT-11 if user-selected at bootstrap
   - Key point - no new knowledge required to understand commands
   - Proposed set:

```
COPY  { A to B                    }     CATALOG     floppy
      { Floppy 1 to Floppy 2      }     INITIALIZE  floppy
                                        LIST        file ON { screen  }
MAKE  file                                              { printer }
RUN   file
DELETE file
```

- Editing performed within language processor and/or separate editor program (thumbwheel select?)

B. Cost/Schedule

- Currently planned RT-11 development (44K) to support ICLS subset targeted for summer 1976 release; could bootstrap off that effort; 3-6 months.

3. File Structure

A. Description

- RT-11: contiguous, for fast access; other organizations not necessary due to lack of large on-line storage capacity.

- File allocation mechanisms might be altered slightly to lessen load on novice user; system overrides provided for more sophisticated type.

B. Cost/Schedule

- Trivial; 1 month.

4. Error Diagnosis/Reporting

A. Description

- Must be English language messages (possible message + number to look up).

- Fixed reaction to H/W - system errors anticipated (e.g., power fail, memory parity, unreadable block on floppy).

- Possible "on-line diagnostics" as part of system floppy - automatically loaded and run at bootstrap (or optional), or loaded and run in response to error.

B. Cost/Schedule

- Small ⟶ significant depending on capability selected; may have payoff in support cost control; 1-6 months.

5. Root Operating System

A. Description

- RT-11 Single Job with additional interfaces to avoid user access to system capabilities (or perhaps available on direct request).

- More/different system functions resident (depending on memory available) to provide correct performance mix (see below).

- Prefer rewritten, new root O/S with "zero-defect" goal-achievable due to reduced complexity/functionality.

- Eventual goal of ROM-ing, and optioning subset functionality.

- Integrated communications? with RT-11 F/B?

B. Cost/Schedule

- Trivial → 1 man year for new product; 1-12 months

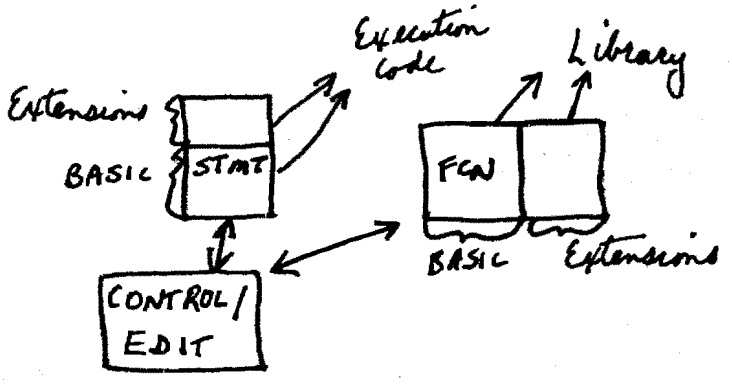
6. Languages

A. BASIC

- Use BASIC/RT-11 (or "common kernel" with O/S interface) need to specialize to configuration, revise error messages.
- BASIC/RT-11 - incremental compiler with "desk calculator" mode; has optional string capability (need 16K); supports CALL, overlays, chaining, sequential and virtual memory files; supports display processor (16K).

Unique

- Proposed "ROM BASIC" would provide table-driven interpreter with extendability via



- Used for "immediate mode" and program development.
- Cost/Schedule: Small → 1-2 man years; 2-16 months.

B. FORTRAN

- Use F4/RT-11.
- F4/RT-11: runs on 8K (16K for string handling subroutines); produces object code directly (threaded - going to in-line integer summer 1976); supports display processor (16K); math and statistical library of functions available.

Basis for quick appl. programs

- Need to specialize to configuration and revise error messages.
- Cost/Schedule: Small; 1-2 months
- Used for program development.

C. FOCAL (extensive user base / library)

- Use FOCAL/RT-11.
- FOCAL/RT-11: based on FOCAL/PTS with support of RT-11 file structure; double precision (16K).

- Need to specialize to configuration and revise error messages.
- Used for: "immediate mode" and some program development.
- Cost/Schedule: Small; 1-2 months

D. DIBOL (How well it known? How easy to pick-up if a COBOL programmer?)

- From COS-350 system.
- Need to separate language processor from system, and review COS-350 text editor, sort/merge, linker, PIP, librarian, and FILEX in context of alternative O/S functions; may want to lift entire system and review user interface for possible modification at this level; also restrict F/B capability, multi-user capability?
- Used for program development.
- Cost/Schedule: Small ⟶ ?; 2-? months.

E. APL

- From OMSI (OEM/LDP/ECP/EPG buy-out).
- OMSI/RT-11: will support APL as well as standard keyboard; DECsystem-10 compatible; double precision; memory overhead and implementation techniques unknown; EIS/FIS might be good ⟶ very desirable ⟶ required (?).
- Used for: primarily interactive (due to power of language) with some limited program development.
- Cost/Schedule: probably small (runs under RT-11); 1/1/76 RT-11 version available to DEC.

F. Mini-COBOL

- Not needed if DIBOL?
- Necessary for Federal Government?

G. RPG

- Desirable due to large user community of experience.
- Parameterized execution of fixed program cycle fits system concept nicely.
- Would provide super competitor to very small System/3 and 360/20 systems.
- Why didn't IBM provide? Too much impact on installed base? Will it be coming soon?
- Used for: program execution (≈ program development)
- Cost/Schedule: unknown

H. PASCAL, PL1, ALGOL, etc.

- Too limited to justify investment? Handle via DECUS?

7. Utilities

A. SORT/MERGE

- Useful in commercial environment, but RT-11 file structure and lack of large capacity on-line storage minimizes.

B. Editor

- BASIC, APL, FOCAL, RPG - no (part of language processor); other languages require one; might separate system products around this sort of function.

C. FILEX/PIP

- May need some capability for floppy media interchange among systems from other vendors (and other-than RT-11 DEC systems)

D. Linker

- Only for versions of this product sold to computer-familiar customers; too much new knowledge for new users.

E. Librarian

- Not for this product.

F. On-line Debugging

- May need some capability in selected products (i.e., only for certain languages).

G. System Patching

- Not for end user, only by DEC persons (on service call)? tied to support questions.

H. Prompting/"Help" Files

- Desirable ⟶ necessary; also depends on documentation available.

8. Documentation

A. Description

- System tutorials, example-oriented.
- Language tutorials and/or reference? language-specific; potential costly investment.
- System Managers Guide: high level, for multi-purpose system; also for product promotion.
- System internals for software support and sophisticated users.
- Self-study, Programmed Instruction Text.
- TV ~~Ed~~ tape

B. Cost/Schedule: varies.

note this material should be substantially system + paper based for programmed learning

9. Performance Parameters

A. APL, BASIC, FOCAL - must "feel" fast; perhaps micro-code extensions or EIS/FIS to achieve (or offer 2 versions - one normal, one speed-up).

B. Program development - lengthened compile times acceptable (not frequent operation); lengthened link times acceptable; editing should "feel" responsive and quick for sections of program displayed, but longer access times to source segments OK.

C. Program loading - lengthened load times OK; run-time execution is the measure.

D. File access - floppy access times acceptable for the anticipated file sizes.

E. System startup - from system integrity point-of-view, would prefer mini-diagnostic test before finishing boot, but time to load system and initiate activity may be important (IBM probably "instantaneous").

F. Memory usage - will vary with language used, but probably aim for larger system overheads to increase responsiveness; user programs may displace much, if not all of basic system, retaining only sequencing, chaining, and re-start type functions; memory context will probably change more completely than in typical RT-11 single job systems; ROM-potential needs looking at (fixed-purpose machines?).

From: Peter Christy
9/19/75

Subj: IBM 5100 Response Applications Package

01739

Motivation:

This study is motivated by the IBM introduction of the Model 5100 desktop computer. The primary motivation for this product may be marketplace penetration -- making sure that the first computer in a shop is an IBM computer, thus making further selling much easier. This would indicate that IBM recognizes substantial growth in the low to mid range computer markets in the future. Whereas the 5100 does not seem to represent dangerous competition per se, if the marketing strategy of "first entry" is correct, IBM could be seriously impacting our future selling situations, which is a real problem.

If we are to meet this challenge head on we need primarily to develop reasonable packaged Problem Solver products -- the major thrust of this section -- and to develop marketing and selling techniques suitable to this marketplace. Our hardware components are competitive (e.g. RX01--11/03--VT52). Any minor differences in the human usability of the RT-based system versus the 5100 are not highly significant because the vast majority of the use of such a product will be problem solution and not program generation. A product based on floppy disk rather than tape will permit verbose CRT dialogue during problem solution, and this is perhaps the optimal human interface.

Problem Solving versus Process Implementation

In terms of understanding a response to the 5100 it is useful to think of the 5100 and System/32 as representing entries into two areas of low-end computing with very different requirements. The System /32 represents competition directly against the traditional minicomputer. The /32 is used to support business activity and is programmed to conform to the particular needs of the customer. Digital has chosen to stay out of the real end-user market here, since this market is characterized by an extensive service relationship which we are not yet ready to address. IBM has chosen to support the end-user market and does this by producing generic application packages for very specific market areas. The applications represent extensive planning and research into the given market.

The 5100 represents an entry into a quite different market characterized by problem solving. This market is certainly better established than the /32 market, and is characterized by less expensive solution of the traditional computational problems -- engineering calculations, numerical analysis, etc. The markets are very different because the end user in the Problem Solver market is quite familiar with calculation and knows the problem area in detail, whereas the /32 customer may be terrified by computers and actually quite ignorant of the problem area

having left much of it to an accountant traditionally. Therefore, whereas the end-user /32 market is necessarily characterized by a service relationship, the 5100 type of market can be sold on a low sales cost, low service basis by providing complete solutions to the traditional Problem Solving areas. This kind of product is what this discussion addresses, not the /32 type of product.

Complete Product Offerings:

Having a complete product offering may be a critical part of selling computer systems into this low-end market. By a complete product offering we mean to suggest a complex calculator/minicomputer and an application package suitable for a given market segment -- BioStat, Statistics, Electrical Engineering, Fiscal, Mathematical, etc.

A complete product would include the machine, very easy to use complete application programs, documentation of program operation and basic introduction to the problem area including cross-reference to standard texts and presentations. The marketplace significance of complete product offerings is the ability of a general salesman being able to sell into, for example, an engineering firm either by a brochure detailing the programs available, or at least by a demonstration period during which the prospect is given access to the machine and standard application materials. The key point is not requiring detailed understanding of customer operations or extensive customer education as part of the selling effort. The product should sell itself and the customer should be able to teach himself the use of the product with essentially no sales time or cost.

Product Relationships and Customer Migration:

This is a facinating problem. It is reasonable to consider this a dead-end kind of product in many ways. The greatest customer "migration" will be due to the Digital sales and service contact and the natural desire for the customer to continue on this friendly and fruitful relationship when he wants to expand his use of computers. The fact that the average entry-level customer will want to increase his use of computers can be taken for granted, since computer technology clearly has substantial price/performance improvement left for the next decade. But beginning from a 5100 type of product, it is likely that the growth in computing will not be a simple, continuous process.

The 5100 type of product has substantial bounds of usability. For example, if such a product is being used for statistics the pain and agony of entering mountains of data will be a very real limitation. If we assume that many of these machines will be sold into offices or labs or organizations that have bigger computers, then the calculator solution must be more convenient than the big machine solution. The orientation should

be on suitably small problems for which large scale data entry is not a major problem. In the case of statistical analysis this would include problems with a reasonably small sample space for which the problem was functional interpolation, but not the formation of statistics on large data sets. Ideal examples of suitable problems are reasonably complex functional calculation for which basic parameters are input and the result calculated (filter design in electronics is a good example).

A Plan of Attack:

Competing in this arena has two major components, assuming for the moment that our hardware offering suffices: (1) creating a suitable product (2) understanding and implementing the marketing and selling of the product. The remainder of this discussion addesses only the first component.

The Product Concept:

The product consists of four parts:

1. The Hardware System

2. An Operating System/High-Level Language Software-supported Execution Environment

3. "Problem Solver" Application Packages (written in the HLL of the execution environment)

4. Documentation (product, marketing and sales support)

The execution environment could be very like the user-environment of todays RT systems.

Step One: Target a Half-Dozen Product Packages

Since all of the major advanced calculator products have chosen packages with a great deal of commonality, the easiest method is to take the obvious intersection of these offerings. This would include:

1. Elementary Statistics

2. BioStatistics

3. Elementary Mathematics

4. Advanced Mathematics

5. Business and Financial

The detailed composition of these packages could be easily determined from sales literature for the IBM 5100, HP9830, HP-65

and Wang calculators.

Step Two: Develop the Product Packages

Each package has two components:

1. The subject programs

2. The documentation

The programs should be easy to construct since all of the algorithms are well known, documented and understood. Although it might be possible to utilize existing library versions of these programs, it is unlikely that these would be adequate basic prducts. It will be important that the functioning and construction of each basic product be carefully verified by Digital specialists before we present it to the customer, and it is important that the human interface to the programs be both made uniform and made professional (for example, existing programs tend to have cryptic, nasty or obscene diagnostic messages).

The programs should be constructed such that the actual computation is partitioned from the interactive control of the Problem Solver. That is, to many customers the product would be used as a Digital provided Problem Solver: the computer would be powered on, the customer would enter RUN GAUSS, and the Digital-provided Guassian Statistics Problem Solver program would lead the customer thru a specification dialogue and then solve the given problem.

However, if the calculation subroutines are neatly partitioned from the interactive control segment, and if the subroutines are written such that addition of code to utilize the subroutines is a well-defined problem (some BASIC implementations pose serious naming problems among shared subroutines) then some customers will use the provided subroutines and add customized calculations or interactions.

The documentation for each Problem Solver product would consist of the following portions:

1. Introduction and Cross-Reference

2. Explanation of Use

3. Brief Description of Calculation Used

4. Listing of Program

The introduction and cross-reference would introduce the problem area briefly (one page) and would reference standard text material giving further discussion of the subject matter.

The explanation of use would relate the standard terminology in the problem area to the terminology and use of the Problem Solver program, and note any major limitations or exceptions to the operation of the program.

The brief description of the calcuation used would be a concise summary of the numerical techniques used, with an emphasis on known limitations or optimizations of the method (for example, consider integration methods).

The listing of the program would be for the customer who intended to modify the program, or was just curious. With a printer option the program could be listed by the computer in the OS facilities. In the manual it could either be presented in a highly reduced format (like the CACM algorithms perhaps) or be included as a microfiche presentation in an end-pocket of the manual.

The Existing DECUS Libraries:

The existing libraries should be a marketable item. The HP-65 user's library is a simple example. HP offers a library subscription (for a fee) which buys an updated catalog of offerings, and then for a further fee HP sells copies of the library item. The documentation method is straight reproduction of documentation on an HP created standard form. Supposedly HP requires that library offerings conform to some degree of documentation standization. In any case, our experience with DECUS should be convertible to a very attractive adjunct to the basic product.

Marketing the Product:

Although the subject is not addressed here, it is clear that the marketing of such products is an integral part of the problem. It is an area for which there is not an obvious model of success within Digital. If one can extrapolate from the HP experience, it would seem that techniques like directed mass mailings may be an important part of product success. A detailed marketing plan should certainly be in place at the time that serious product development is begun.

	IBM	CLASSIC	ANDY	STOCKY	CLARKE
• DEFINITION	PORTABLE SINGLE USER	DESK SINGLE USER	2 BOXES (1)VT52 (2)1103 + FLOPPY	2 BOXES (1)-LSI11 (2) FLOPPY	PORTABLE SINGLE USER COMPUTER
• SIZE	8X17.5 X24	30 x 48 X 30	(1)14 X21 X 28 (2)14 X 19 X 17	(1)14 X 21 X 28 (2)26 X 12 X 19	16 X 22 X 21
• WEIGHT	50 LBS.	450 LBS.	(1)50 LBS. (2)75 LBS.	(1)50 LBS. (2)75 LBS.	60 LBS.
• DISPLAY					
SIZE	5"	12"	12"	12"	12"
CHARACTERS	64/32	80	80	80	80
LINES	16	12	24	24	24
INV. VIDEO	YES	NO	NO	NO	YES
MONITOR JACK	YES	NO	NO	NO	YES
GRAPHICS	NO	NO	NO	NO	OPTIONAL
• KEYBOARD					
TYPEWRITER	YES	YES	YES	YES	YES
OTHER	NUM/APL	NUMERIC	NUMERIC	NUMERIC	NUMERIC
CURSOR CTRL	YES	YES	YES	YES	YES
FUNCTIONS	CMND. MODE	NO	NO	NO	OPTIONAL REMOTABLE
• BULK STORAGE					
TYPE	CARTRIDGE	FLOPPY	FLOPPY	FLOPPY	FLOPPY
BYTES	204K	512K	512K	512K	512K
SPEED	40 IPS	400 MS ACCESS	400 MS ACCESS	400 MS ACCESS	400 MS ACCESS
READ/WRITE	2850/950 CPS	1250/1250	1250/1250	1250/1250	1250/1250
• I/O	HARD COPY CARTRIDGE	6 OPTIONS	3 Q BUS DOUBLES	3 Q BUS DOUBLES	3 Q BUS QUADS
• PROCESSOR	INVISIBLE	8A	LSI-11	LSI-11	LSI-11
• MEMORY					
BYTES					
RAM	16 TO 64K		8 TO 56K	8 TO 56K	8 TO 56K
ROM	YES		YES	YES	YES
CORE		32K WORDS	YES	NO	YES
• PROGRAMMING					
MACHINE CODE	NO	YES	YES	YES	YES
HIGHER LEVEL	BASIC/APL	8 SOFTWARE	11 SOFTWARE	11 SOFTWARE	11 SOFTWARE
• INSTALLATION	USER	USER	USER	USER	USER
• MFG. COST	$1800 EST.		(1)$700 (2)$1716	(1)$1511 (2)$785	
FY'77		$3200	$2416	$2296	$2100
• DELIVERY	NOW	5/75	2/76	6/76	12/76
• DEVELOPMENT COST		DONE	(2)80K	(1)180K (2)130K	FY'76 750K FY'77 450K

ASSUMPTIONS FOR MFG. COST FY'77 :- 12K BOARD, IN HOUSE FLOPPY, 16K BASE SYSTEM

JOHN CLARKE 9-19-75

01805

• DEFINITION	VT61 SMART TERMINAL EDITING FEATURES PORTABLE	VT52+LS111 INTELLIGENT USER PROGRAMMABLE PORTABLE
• SIZE	14 X 21 X 28	14 X 21 X 28
• WEIGHT	50 LBS	50 LBS
• DISPLAY		
SIZE	12 "	12 "
CHARACTERS	80	80
LINES	24	24
UPPER/LOWER	YES	YES
INVERTED VIDEO	YES	NO
DATA	ONE SCREEN	FIVE SCREENS
FIELDS	PROTECTED	PROTECTED
• KEYBOARD		
TYPEWRITER	YES	YES
NUMERIC PAD	YES	YES
CURSOR CONTROL	YES	YES
EXTRA FUNCTIONS	YES	YES
• MEMORY	2 K	56 K
• PROGRAMMING	UNIQUE MICROCODE	11 SOFTWARE
• MFG. COST	$850	$1200 8 K BYTES
• DELIVERY	2/76	6/76
• DEVELOPMENT COST	200K/QTR. IN BUDGET	FY'76 $180 K
• PROTOCOL		
HOST MOD. NEEDED	YES	NO
ARPA NET. COMPATIBLE	NO	YES
USER PROGRAMMABLE	NO	YES
DDCMP COMPATIBLE	YES	YES
SPLIT SCREEN	NO	YES

T. CLARKE

D I G I T A L INTEROFFICE MEMORANDUM

SUBJ: FIBER OPTICS

DATE: 10-01-75
FROM: GORDON BELL
EX: 2236
MS: ML12-1/A51

TO: FILE

Subj: FIBER OPTICS, OPTICAL ISOLATORS AND US

To: Distribution

There were at least 4 mentions of Fiber Optics, etc. in Electronics, September 18, 1975; and it was not a special issue on the subject. My view is that if Electronics, or another of the popular trade press knows about something, then it's not very long till we see a rash of products (e.g. IBM and HP). Even the low risk components cause a problem (e.g. low power Schottky TTL).

although we seem to have a strong unwritten policy to wait for competitors to produce with a new technology before we look at it, this may be worth bending the policy.

I'd like your comment on the following:

Do you believe this is our development policy?----------

Should it be?----------

Is this an idea worth looking at for our computers?--------
How does it rank with some of the work done in your own group in importance?----------

Who's responsible to watch, recommend and/or initiate work in this area?

Eng. Committee--, Eng. Mgrs.--, Engineers--,
Operations Committee--, Office of Development--,
VP of Engineering--, Consulting Engineers--,
individual groups that might use it--, Research Group--,
component suppliers--, components engineering--,
Chief Engineer--, other--.

Should we have a group who does nothing other than look at new technology such that it can be applied when mature?

[illegible] operational amplifier, the CA3130 C-MOS/bipolar op amp is especially suited for this application because of its field-effect-transistor input, full voltage output swing, and low cost.

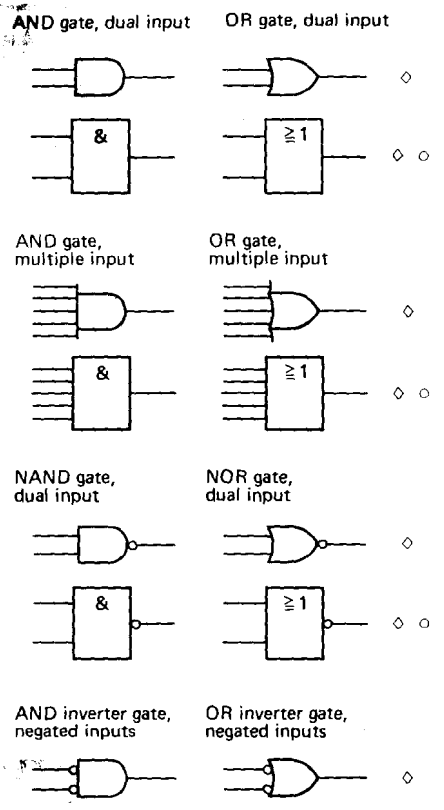
Programable current ranges are obtained by inserting one or more CD4051 C-MOS analog multiplexers in series with resistors of selected values, as shown in Fig. 2. The CD4051 multiplexer has internal level-shift circuitry to accommodate different logic families.

For the higher current ranges (R_{OUT} less than 10 kilohms), it may be necessary to take the on resistance of the switches into account by adjusting the combined resistance of the switch and resistor to yield accurate currents. If V_{IN} is less than ±0.5 V, the op-amp input-offset voltages should be nulled. □

Designer's casebook is a regular feature in Electronics. We invite readers to submit original and unpublished circuit ideas and solutions to design problems. Explain briefly but thoroughly the circuit's operating principle and purpose. We'll pay $50 for each item published.

Graphic symbols clarified

A number of readers were apparently confused by the gates section of two-state logic devices in the "Graphic Symbols for Electronics Diagrams," April 3, 1975. To clear up this confusion, the gates section has been modified and reproduced here. It can be clipped out and placed over the origi-



	IBM	CLASSIC	ADDY	STOCKY	CLARKE
• DEFINITION	PORTABLE SINGLE USER	DESK SINGLE USER	2 BOXES (1)VT52 (2)1103 + FLOPPY	2 BOXES (1)-LSI11 (2) FLOPPY	PORTABLE SINGLE USER COMPUTER
• SIZE	8X17.5 X24	30 X 48 X 30	(1)14 X21 X 28 (2)14 X 19 X 17	(1)14 X 21 X 28 (2)26 X 12 X 19	16 X 22 X 21
• WEIGHT	50 LBS.	450 LBS.	(1)50 LBS. (2)75 LBS.	(1)50 LBS. (2)75 LBS.	60 LBS.
• DISPLAY					
SIZE	5"	12"	12"	12"	12"
CHARACTERS	64/32	80	80	80	80
LINES	16	12	24	24	24
INV. VIDEO	YES	NO	NO	NO	YES
MONITOR JACK	YES	NO	NO	NO	YES
GRAPHICS	NO	NO	NO	NO	OPTIONAL
• KEYBOARD					
TYPEWRITER	YES	YES	YES	YES	YES
OTHER	NUM/APL	NUMERIC	NUMERIC	NUMERIC	NUMERIC
CURSOR CTRL	YES	YES	YES	YES	YES
FUNCTIONS	CMND. MODE	NO	NO	NO	OPTIONAL REMOTABLE
• BULK STORAGE					
TYPE	CARTRIDGE	FLOPPY	FLOPPY	FLOPPY	FLOPPY
BYTES	204K	512K	512K	512K	512K
SPEED	40 IPS	400 MS ACCESS	400 MS ACCESS	400 MS ACCESS	400 MS ACCESS
READ/WRITE	2850/950 CPS	125071250	125071250	125071250	125071250
• I/O	HARD COPY CARTRIDGE	6 OMNIBUS OPTIONS	3 Q BUS DOUBLES	3 Q BUS DOUBLES	3 Q BUS QUADS
• PROCESSOR	INVISIBLE	8A	LSI-11	LSI-11	LSI-11
• MEMORY					
BYTES					
RAM	16 TO 64K		8 TO 56K	8 TO 56K	8 TO 56K
ROM	YES		YES	YES	YES
CORE		32K WORDS	YES	NO	YES
• PROGRAMMING					
MACHINE CODE	NO	YES	YES	YES	YES
HIGHER LEVEL	BASIC/APL	8 SOFTWARE	11 SOFTWARE	11 SOFTWARE	11 SOFTWARE
• INSTALLATION	USER	USER	USER	USER	USER
• MFG. COST	$1800 EST.		(1)$700 (2)$1716	(1)$1511 (2)$785	
FY'77		$3200	$2416	$2296	$2100
• DELIVERY	NOW	5/75	2/76	6/76	12/76
• DEVELOPMENT COST		DONE	(2)80K	(1)180K (2)130K	FY'76 750K FY'77 450K

ASSUMPTIONS FOR MFG. COST FY'77 :- 12K BOARD, IN HOUSE FLOPPY, 16K BASE SYSTEM

JOHN CLARKE 9-19-75

01805

• DEFINITION	VT61 SMART TERMINAL EDITING FEATURES PORTABLE	VT52+LSI11 INTELLIGENT USER PROGRAMMABLE PORTABLE
• SIZE	14 X 21 X 28	14 X 21 X 28
• WEIGHT	50 LBS	50 LBS
• DISPLAY		
SIZE	12 "	12 "
CHARACTERS	80	80
LINES	24	24
UPPER/LOWER	YES	YES
INVERTED VIDEO	YES	NO
DATA	ONE SCREEN	FIVE SCREENS
FIELDS	PROTECTED	PROTECTED
• KEYBOARD		
TYPEWRITER	YES	YES
NUMERIC PAD	YES	YES
CURSOR CONTROL	YES	YES
EXTRA FUNCTIONS	YES	YES
• MEMORY	2 K	56 K
• PROGRAMMING	UNIQUE MICROCODE	11 SOFTWARE
• MFG. COST	$850	$1200 8 K BYTES
• DELIVERY	2/76	6/76
• DEVELOPMENT COST	200K/QTR. IN BUDGET	FY'76 $180 K
• PROTOCOL		
HOST MOD. NEEDED	YES	NO
ARPA NET. COMPATIBLE	NO	YES
USER PROGRAMMABLE	NO	YES
DDCMP COMPATIBLE	YES	YES
SPLIT SCREEN	NO	YES

J. CLARKE
9/17/75

October 2, 1975

D. J. Horton
Trans-Canada Telephone System
P.O. Box 365
Station A
Ottawa, Canada K1n 8v3

Dear Mr. Horton:

Thank you for the invitation to Ken Olsen to submit a paper to ICCC-76. We have several activities in computer communications: DECNET--methods for interconnecting our computers; and the Communication Product Line, which markets computers for communication.

I have sent a copy of the call to Nat Teichholtz, heading the network activity, and to Julius Marcus, Vice President of the Data Communication Product Line. I'm sure if they have any new results to report, they'll respond.

Clearly people from here will attend, if you get the kind of papers you're soliciting. Good luck on the conference.

Sincerely,

Gordon Bell

Gordon Bell
Vice President, Engineering

GB:mjf

DIGITAL EQUIPMENT CORPORATION, 146 MAIN STREET, MAYNARD, MASSACHUSETTS 01754
(617)897-5111 TWX: 710 347 0212 TELEX: 94-8457

ADVANCEMENT THROUGH RESOURCE SHARING

SEP 16 1975

01807

third international conference on computer communication

p.o.box 365
station a
ottawa, canada
k1n 8v3

September 10, 1975

Mr. K. Olsen,
President,
Digital Equipment Corp.,
146 Main St.,
Maynard, Mass. 01754

Dear Mr. Olsen:

As Conference Governor of ICCC-76, to be held in Toronto August 3-6, 1976, it is my pleasure to enclose a copy of the first publicity action on this conference, namely the Call for Papers.

The document covers the intent of the conference, but there are a couple of points I would like to emphasize.

1) A major objective of ICCC-76 is to have a truly international conference, which is one reason it is being held in the week following the Olympic Games. We hope that many people will take the opportunity to visit Canada for the Games and will travel to Toronto (one hour by plane, five hours by train from Montreal) for the conference.

2) We hope to have a relatively senior representation at this conference. We are aiming at an attendance of about 1000 delegates and we believe that the most important objective is that the conference should be an opportunity for people at the decision making level in all facets of computer communications to get together.

As you are aware, there is now a proliferation of such conferences, and, since it is impossible to attend them all, many have become less successful in recent years.

We would like to ensure that ICCC-76, and future ICCC conferences, will become a biennial opportunity for reunion.

3) A major objective for this conference is that it should be multi-disciplinary. Much attention has been given over the last few years to technical aspects of computer communications. Conferences on the social aspects have tended to be held quite separately. We want to see some of the social effects of computer communications highlighted at ICCC-76. While we will be particularly focussing on the fields of medicine and law, the social implications of electronic fund transfer is another area that will undoubtedly gain much attention.

As a senior official of an important organization in the Computer Communications field, your help would be valuable to us in ensuring that we have the best possible conference and I would particularly welcome any thoughts or ideas you or your people might have.

I look forward to hearing from you.

Yours very sincerely,

Encl.

Good luck on the Conference. Hope if you get the kind of papers you're solicitty.

Dear. to Ken Olsen

Thank you for the invitation to submit a paper to ICCC-76. We have several activities in Computer Communications: ~~Netw~~ DECNET — ~~a method~~ methods for interconnecting our computers; and a Communications Product line which markets computer ~~in the~~ for communication. I have sent a copy of the call to Nate Tenhoff ~~who heads~~ the network activity ~~and~~ to Julius Marcus, ~~head of~~ Vice President of the Data Communications product line. I'm sure if they have any new results to report, they'll respond. Clearly people from here will attend

01810

SUBJ: FIBER OPTICS

Other comments----------

GB:mjf
Attachment

Distribution

Engineering Managers
Consulting Engineers
Engineering Committee
Research Group

Around the world

BPO to test fiber-optic telephone transmission P53

Field trials begin soon for two types of fiber-optic telephone links the[y] Post Office has developed and successfully tested in the laboratory. [H]ever, much development and engineering work is still needed to ensu[re] links' reliability and maintainability before they become part of the phone network. The fiber-optics must also prove to be more econo[mical] than conventional coaxial cable.

A system intended for medium-length hops operates at 8.48 megabits/ second, and a system for long-distance trunks operates at 139.264 M[b/s] which, for convenience, is rounded off to 140 Mb/s. Both systems are c[om]posed of the light source, coupler, optical fiber, another coupler, the ph[oto] diode to convert the light to electrical signals, and the associated amp[lifier] and processing circuitry. To minimize transmission losses at the cri[tical] connecting points, the BPO researchers have designed a screwable c[ou]pler using aspheric optical plastic lenses to cut down distortion. The cou[pler] pler actually is two half-couplers, each with lenses 5 and 7 millimeters in diameter that [illegible] for a precise [illegible]

Where fiber optics can be used

Sure, fiber optics is a coming technology, offering low-loss wideband optical transmission in small spaces, but is it here yet? See for yourself—the National Technical Information Service has compiled **a bibliography of Government-sponsored work on fiber-optic materials and applications through May 1975.** The 147 abstracts include studies on display systems, communications and TV equipment, transmission lines, imaging devices, recording systems, measuring instruments, and integrated optical circuits. The report, entitled "Fiber Optics," is available in either hard copy or microfiche for $25 from National Technical Information Service, 5285 Port Royal Rd., Springfield, Va. 22161. Ask for NTIS/PS-75/420. **—Laurence Altman**

114

Bell plans test of fiber-optic phone system . . .

Fiber-optic telephone transmission will move closer to reality at the end of the year when Bell Laboratories starts a field trial of a system near Atlanta. **Significantly, production-type equipment will be used in a real operating environment.**

The transmission medium will be cables containing a large number of fibers, from both Bell and Corning, with a single fiber per channel of information. Also significant will be the repeater spacing: five to six miles rather than the easily attainable two or three, meaning repeaters could be taken out of manholes and placed in central offices. And though Bell won't comment, it is believed to have ready for production an advanced repeater with a "quick-connect" design.

P25

. . . as GTE sets field trials of optical trunks

At about the same time that Bell conducts its tests, GTE Corp., the nation's No. 2 telephone company, will start a field trial of its own "practical" fiber-optic system. The test will take place, using existing links, at an operating GTE facility, probably on the West Coast. Thus, the system, which will use an electronic/optical interface, appears to be the first big step **toward replacing T-carrier interoffice trunking with the much higher capacity fiber-optic system.**

According to E. Bryan Carne, director of electronic technology at GTE Labs, the fibers used in the trial will have a loss of 5 decibels per kilometer so that runs of 15,000 feet between repeaters are possible. By comparison, repe[illegible]ced every 6,000 ft.

D I G I T A L INTEROFFICE MEMORANDUM

SUBJ: SOFTWARE PRODUCT MODELS

DATE: 10-02-75
FROM: GORDON BELL
EX: 2236
MS: ML12/A51

TO: SOFTWARE DEVELOPMENT MANAGERS --

SUBJ: PROPER NAMES FOR SOFTWARE PRODUCT MODELS AND REVISIONS TO THEM

To: Distribution F/U 10/10

In listening to several PM's and the field hassle we create through revisions to software products, and changes in policy, it became clear to me why this occurs:

1. We build what are fundamentally different software product models by adding new user features and do not give them different names that are apparent to us and our users.

2. We do not clearly distinguish between ECO's and new features revisions. All are versions, and through these can be deduced, they are not advertised as such.

This leads to:

1. A feeling that a product will go on, be added to, and last forever without any bound.

2. No way to clearly talk about which version various systems will run on.

3. No way to ever change a policy, since our literature is not time (death) dated. As a result, our customers really don't know what's going on, can't distinguish among models and ECO's, etc.

4. Potentially explosive situation contractually when we do benchmarks on an early system, deliver a later version with more features (and larger size), and end up with less performance than initially promised. (Note, the Navy has actually gotten new hardware from a vendor who did this.)

PROPOSED SOLUTION

1. A system is never called without a model number. For example, like processor hardware, RT-11 is actually a series of operating systems and should always be identified

as such, i.e. no RT-11, only the RT-11 series...just like the PDP-11.

2. Each specific version (not an ECO) which has new features is identified by name in its literature title, or purhcase order name, and order number by its name and Model #. I would propose it could be either:

   A. Roman numeral mark #'s, e.g. RT-11/I, ..., RT-11/IV.

   B. Strict model # e.g. RT-11/1, ..., RT-11/4.

3. New versions would breed new literature and policies, prices, phase out, etc. plans could be managed. ECO's to models would be used as we do them now and have order #'s, e.g. RT-11/1.2. Normally, the ECO version would not be important, but it would be used to manage our warranty policy (whatever it might be).

Can we start this now and stop the confusion of giving a single name to what is basically a set of entities? What you think?

GB:mjf

Distribution

Software Product Managers
OOD
PLM
Software Managers
Dave Stone
Dick Best

D I G I T A L INTEROFFICE MEMORANDUM

SUBJ: OUTSIDE DESIGNED COMPUTER

DATE: 10-06-75
FROM: GORDON BELL
EX: 2236
MS: ML12/A51

TO: OPERATIONS COMMITTEE XX

SubJ: DECISION OF AN OUTSIDE DESIGNED COMPUTER FOR OUR PRODUCTS

CONFIDENTIAL

Engineering is recommending that it use the Motorola 6800 as the base of terminals, floppy controllers, etc. It's selection as a poor, second technical choice is due entirely to our perception of Intel as our dominant competitor.

The Winner

Motorla (AMI-second source)--small MOS division ($30M), technology not under control and weak technologists, poor past management structure, high investment in microprocessor could jeopardize future. This is almost a lose/lose situation: as a weakling, we'll have poorer products because of them; if they get strong--they'll be our competitor.

Why the alternatives were rejected:

1. Signetics--late with poor product; we have good working relationship with them; no interest in components to use part in low end microcomputer market.

2. Fairchild--product too small for future applications. Poor working relationship.

3. Intel--clear technology, programming, product and market leader by 2+ years. We would learn much, and if a close relationship, we would teach them more about systems, although it looks like they don't have much to learn. A competitor at systems and board level.

Concerns for LSI-11 Product Management and Microcomputer Marketing

1. Although we see Intel as our significant competitor at the board level now, this appears unrealistic: we lose money selling at this level; Intel (and others) have much

SUBJ: OUTSIDE DESIGNED COMPUTER DATE: 10-06-75
FROM: GORDON BELL

room to reduce prices in what is a seller's market

2. The board level may require memory chip manufacture, and already requires new parts, options, etc. 01815

3. We face little deliverable competition now except Intel... Motorola, et al will be inevitably. I don't see us as competitive at this level.

4. The LSI-11 is beginning to absorb significant resources in engineering for LSI chips, communications options, peripherals, cabinets to give us a cost reduction in the conventional systems business. This may just take away from other sales with lower NOR and high engineering costs. Alternatives, I hope we can make products heretofor unavailable (i.e. smaller).

5. We have no ROI/PC model of this investment. It's significant, and the Product Management/Marketing has effectively sold it internally as a great product. I think (hope) it is too. We all want to believe but a bigger picture, with some depth, would help.

GB:mjf

cc: Steve Teicher, Rob VanNaarden

GB
9/24/75

MICROPROCESSOR SELECTION ALTERNATIVES AND CRITERIA

	INTEL	SIGNETICS	MOTOROLA	FAIRCHILD
Mgmt.	Best managed.	Not clear about Philips commitment. Team is new.	Real problems; groups are spread out geographically. Team is new. MOS is only $30M	N o joint trust; too egocentric; top dog fight (rumored).
Inter-face	We interface well there; and will learn from their 2+year lead. They'll learn boxes from us.	Best technical interface.	Can probably work. We'll teach them programming, testing, etc.	Poor
Tech-nology	Best and improving technology.	Process looks good--Philips could help them.	Not clear whether they have it.	Not clear--should be OK.
Cost	Lowest cost by $10.	Next lowest cost (maybe phony)	OK	Low chip count--should be cheap.
Prod-ducts	Best product array. We will need their new, high and low end for new products.	Marginal--taking some chance.	OK for now, though there are some problems.	OK--not really powerful enough for other applications.
Support	Very good.	We'd have to do it.	Programming poor--we'll redo.	OK
Other (Market)	#1 competitor--their costs are low enough to support lower prices.	We could do parts, tell them what to build, do support software; and enter main microprocessor market.	Our order is relatively small to their plan. It will give them more credibility...and they will eventually compete.	
	Our volume is small; won't affect things. Will use our order to compete against us--to the naive customer.	This could help even out the sides: Intel #1, Motorola trying for #2.	They're doing BASIC to compile at systems.	
Eng. negatives	LSI-11 + Comp. Eng. don't want them.	Component group believes they're backward.	GB negative.	

D I G I T A L INTEROFFICE MEMORANDUM

SUBJ: AADS - WHO'S GOING TO INTERFACE WIT DATE: 10-06-75
FROM: GORDON BELL
EX: 2236
MS: ML12-1/A51

* *

TO: FILE

* *

Subject: AADS - WHO's GOING TO INTERFACE WITH THE SELECTION COMMITTEE?

To: Distribution

As I hope you're aware, a group from DOD, especially NRL (W. R. Smith and Y.S. Wu 202-767-2518) is in the process of selecting a commercial computer for all the services. Supposedly they will then ask to license it.

The 11,360 DG Eclipse, Interdata, and Burroughs B6700 are the architectures being evaluated. The 11 is fairing poorly. The pivotal issues: 16 vs 32 and addressing; spare opcode space; software; and military versions.

Prof. Dan Sieworiek, CMU (412-621-2600)) is head of the sub-committee studying and proposing the 11. They need help from us in answering some of the above questions.

Their schedule:

Report from sub-committees	Nov 15
Meet	Dec 1
Selection criteria ready	Jan 1
2 or 3 machines selected	Feb/March
Recommendations	July

The results of a call to Smith:

1. W. S. Wu and W. R. Smith want to meet with us about the patents and software licensing. They will come here for a 2+hr. meeting. They'll describe the program and time table. It should be scheduled by either Bob or Roy in the Washington office.

2. We need tomake a general statement about 11 evolution in the future vis a bis above problem. This can now be done in a letter to Sieworiek which I can

SUBJ: AADS - WHO'S GOING TO INTERFACE WIT DATE: 10-06-75
FROM: GORDON BELL

write.

3. Someone has to be the interface there and here. I want out.

4. They're trying to sort out how they handle proprietary data, given we want to say more about our plans.

GB/lp

Distribution: John Buckley, Dick Clayton, Bob Huberfield, Malcom Johnston, Julius Marcus, Ed Schwartz, Roy Van Dusen.

01820

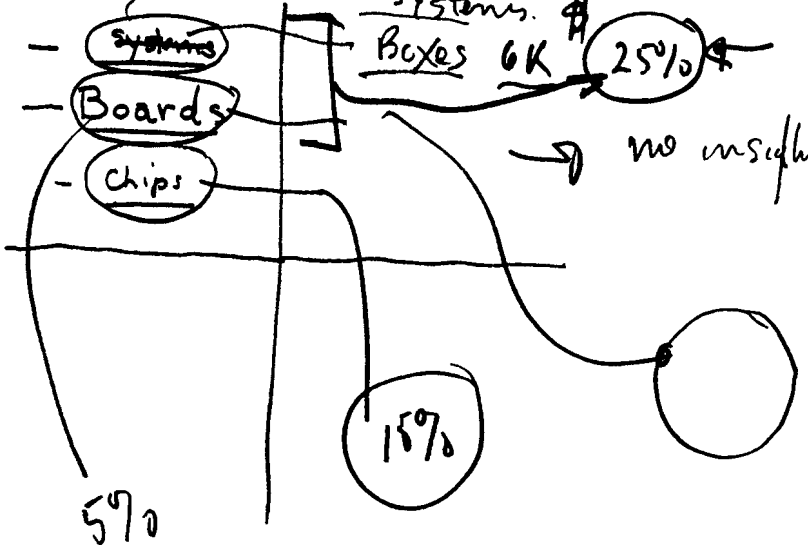
digital INTEROFFICE MEMORANDUM

TO: John Chambers
cc: Bob Poff
Mark Ahlert

DATE:
FROM: gBell
DEPT:
EXT: LOC:

SUBJ: Attendance of R+D Mgmt Seminars by K. Olsen

I've got a tentative commitment from Ken to attend. Will you contact Peggy to schedule him at first meeting and send a copy of the ~~Matrix~~ Schedule / topics?



→ no insight to sell to End user.

D I G I T A L INTEROFFICE MEMORANDUM

01821

PAGE 1

SUBJ: MULTIPROCESSORS

DATE: 10-02-75
FROM: GORDON BELL
EX: 2236
MS: ML12/A51

* *

TO: FILE

* *

To: Distribution F/U 10/10

As per my discussion with Mike and Roger, I would like several of us (e.g. GB, BD, Eckhouse, VAXA-rep, and Len Hughes) to meet with you regarding multiprocessors. Bruce is putting the multiprocessor banner selling responsibility on me. We would present some some arguments, problems, etc. and then get your input and reaction. This would be a warm-up for a more general presentation.

GB:mjf

Distribution

Roger Cady
Don Alusic
Julius Marcus
Mike Mensh

cc: Al Avery, Dick Clayton, Dick Eckhouse, Bruce Delagi, Len Hughes, Larry Portner, VAXA, Ulf Fagerquist

D I G I T A L INTEROFFICE MEMORANDUM

SUBJ: C. EXPERIMENTER MARKET

DATE: 10-02-75
FROM: GORDON BELL
EX: 2236
MS: ML12/A51

TO: FILE

Subj: THE COMPUTER EXPERIMENTER MARKET...A BEGINNING OF THE COMPUTER-IN-A-HOME (see attached interchange)

To: Distribution

Mark Sebern has been corresponding with a number of these people, and there is now a club, Byte, which interchanges information.

Since we subsidized another L.I. high school student, there has been more than the usual set of requests. This previous sale was OK, but there is still a problem with maintenance--the board mailer would solve most problems for them.

Clearly, no single PL can handle this now, although Logic Products looks close. Now, if DEC goes with Heathkit, this might be the right approach. The novice and experimenter (and many others--I suspect) seem to want:

1. Manuals to understand (they'll pay for these alone).

2. Low prices via catalog...no salespersons!

3. Modules where they can do as much as they have money for.

4. Ability to trade-off make-vs-buy (ala Heathkit).

5. Some mechanism to exchange programs and communicate with other users.

6. Ability to get mailer service. Currently ALTAIR is optimum for them. My "party line" is given in the letter.

GB:mjf

Attachment

Distribution

Bill Hogan

SUBJ: C. EXPERIMENTER MARKET

DATE: 10-02-75
FROM: GORDON BELL

Ted Johnson
Andy Knowles
Bob Lane
Alice Peters
Bob Reed
Mark Sebern
Charlie Spector

cc: Ken Olsen

October 1, 1975

01826

George A. Cacioppo, Jr.
238 Martha Avenue
East Patchogue, New York 11772

Dear George:

It was good to talk with you about the problem of setting your own computer. As I see it, we may not have computers at the price you want to pay, since our prices are predicated on certain market, sales, service and software support prices and policies.

I'm enclosing a catalog of our Logic Products product line, which has the MPS (8008) and the PDP-8/A modules. Both of these schemes might allow you to build at the rate you want. There is also a problem of service which you clearly have to address. I'd hope the MPS service arrangements and policy would work the way you want it to. I'd be interested in your reaction to this scheme versus the ALTAIR. Also, I'd like you to write just what you'd expect from a company that sells you a computer. I.e., do you want salespeople to call, software service, maintenance, software interchange, etc. Also, how much would you pay for this?

As I indicated on the phone, I hope you will move immediately (at least by the second semester), to a university with a strong Electrical Engineering/Computer Engineering department (Carnegie-Mellon is my preference, but some of the NY State universities are clearly fine). With your background and understanding of computers, your strong academic background, and Regent's Scholarship, the incremental approach you're taking to your education will be time-consuming and produce a poor product. The university should provide your machines to teach you for now, and I don't believe you should have enough spare time to do the building.

Sorry we can't help you for now, but I'll keep my eye open for a machine that we might sell you in a non-subsidizing, business basis.

Sincerely,

DIGITAL EQUIPMENT CORPORATION

Gordon Bell

Gordon Bell (mfl)
Vice President, Engineering
Professor, Computer Science
Carnegie-Mellon University (on leave)

GBell:jf

9/19

Gordon

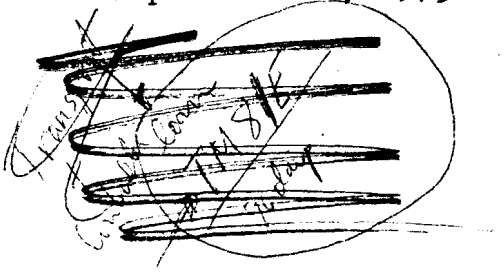
I've turned him down - gently, I hope. You should have received copy of my letter already. Original returned for your files -

Eric Rohmer

01827

George A. Cacioppo, Jr.
238 Martha Avenue
East Patchogue, N.Y. 11772

September 16, 1975



Gordon Bell
Vice-President
Digital Equipment Corp.
146 Maynard Street
Maynard, Mass. 01754

Dear Sir:

Perhaps Alice Peters did not understand my letter regarding my obtaining a PDP/8 computer. My application is not strictly software development.

I am a student of computer science and electrical technology my first priority is to obtain a PDP/8 for my work. I want it to be proggrammed by DIGITAL in Basic, and hopefully, Macro. I am not out to develop new software.

What I request is a helping hand from the company that I "plug" all of the time. I have worked in a timesharing environment for four years. If I do say so myself I have learned as much as possible at a remote site. Now having graduated from Long Island's high school system, I have been cut off from all the facilities their PDP-10 offers. I need to continue with what I have been doing.

I would like to obtain a desk top machine with a teletype which would be enough to suit my purposes for now. This would finally give me a hands on environment where I could learn even more about DEC machines. I hope someday to share my knowledge with others who would not be so fortunate as to have their own computer. I must admit that at this time my purposes are purely in my own interest. So that I may work further.

I can only emphasize that I have been cut off simply because I have graduated. I am willing to pay for the machine if I have to. I will even revert to buying a used machine if I must. I ask your help, whatever the case. If there is any way you can help me to obtain a PDP-8 so I won't be left hanging with knowledge I can't use, please contact me. I need someone's help, that is why I write to you. In the hope that you may be able to help me.

Yours Sincerely,

George A. Cacioppo Jr.

P.S. I am sorry to take up your time, but I hope you will understand how devoted I am to my work. Thank You.

AUG 22 1975

01829

George A. Cacioppo, Jr.
238 Martha Avenue
East Patchogue, N.Y.
11772
(516) 286-2091

Gordon Bell
Vice-President
Digital Equipment Corp.
146 Main street
Maynard, Mass.
01754

Dear Sir;

I am writing to you for some help. I have been a computer student for four years at Bellport Senior High School. I learned most of my programming abilities on the computer of LIRICS timesharing located in Dix Hills. The computer was a dec-system PDP-10. I was the president of their student user group for the 1973-1974 school year. You can find my name on your mailing list, or last years as having requested all the PDP-8 manuals Decsystem could supply me with, which they did.

My purpose in writing to you is that I would like to obtain a PDP-8/e (or if neccesary PDP-8/m). for my personal use in designing software for a timesharing system for a PDP-8. I am currently enrolled at SUNY of N.Y. at Farmingdale for Electrical Technology. At the completion of this course I hope to have completed the neccesary software and hardware work to begin opening a general timesharing and/or Data Processing company hereon the Island.

My problem is the availability of funds for my work. I cannot possibly afford to buy a PDP-8 out of my own funds. Is there an program that Dec has whereby a cost reduction can be made in return for my research efforts? I can assure that Dec would at least receive advertising from this venture as several of my teachers and a group of students from my PDP-10 work will be helping me to design the system.

Could there perhaps be grants from the government that would defer my cost of buying a PDP-8? After leaving college I hope to buy the additional hardware neccesary to support a multi-user environment. This means that the original computer will become a base for the system.

I have been interested in computers since a very young age, I am very well versed in assembly language(Macro) for the PDP-10. I find that I cannot give you any more reasons for helping me except that I have been working for years hoping to end up working with computers as a profession. I can assure that Dec will have all rights to the work that I(we) produce.

If there is some way in which you can help us we would probably need:

PDP-8 processor (8/e prefferred because of expandability, or 8/m

4 to 8 k of memory

one teletype w/interface

Macro-8 assembler (for ease in programming, examples)

Basic-8 (for simple programming, for demonstrations, instructing beginners, and perhaps usable for a source of income e.g. teaching students BASIC)

And any other equipment you deem neccesary (the Macro-8 assembler is optional, but would save our effort because of out prior experience.)

Thank You for reading my inquiry, I hope to have supplied with all the information necessary. I am not just anyone who wants to get a computer inexpensively, I am someone who loves DEC-system computers and would like to make his lifes work of operating one. Please feel free to call at any time of the day or night if you need more information.

Yours Sincerely,

George A. Cacioppo, Jr.

George A. Cacioppo, Jr

D I G I T A L INTEROFFICE MEMORANDUM

01830

PAGE 1

SUBJ: ASR CAPABILITY

DATE: 10-07-75
FROM: GORDON BELL
EX: 2236
MS: ML12-1/A51

* *

TO: FILE

* *

Subject: RE ASR CAPABILITY - WHAT IS IT AND HUEFNER/WOLAVER RESPONSES

To: Distribution

It looks like we're somewhat on the track to get some of the ASR capability:

1. LA36 with buffering (which I hope gets simulated now on Mark Sebern's machine before wiring down).

2. LA36 with Moffa - ASR Unit

3. VT5X with Moffa - ASR Unit

It's just occurred to me that we already have a nifty product which solves all the applications which are like DECNET. IT IS:

The VT61 with Copier!!

It has:

1. Editing capability

2. A buffer to store reasonable sized messages for computation

3. Ability to be pulled and transmit

4. Hard copy

Why can't we replace some of the TTY ASR's internally (i.e. all of George Friend's DECNET)?

How to test it??

GB/lp

Distribution:

[redacted]
Ed Correll
Alan Dziejma
Ken Fine
George Friend
Al Huefner
Andy Knowles
Roy Moffa
Bob Puffer
Mark Sebern
Tom Stockebrand
John Wolaver
Mike Wurster

[redacted]

SUBJ: JAPANESE COMPUTER MARKETING STRATEG DATE: 10-07-75
FROM: GORDON BELL
EX: 2236
MS: ML12-1/A51

TO: FILE

CONFIDENTIAL

To: Distribution

Subject: THE JAPANESE COMPUTER MARKETING STRATEGY:
\THE OLD ORIENTAL INTERCHANGEABLE AMMUNITION TRICK

Since the Japanese re-designed the Chinese Abacus for cheaper producibility and easier use, calling it the Soroban; they have been improving other devices. Now with computers there is a clear continuation of the trend. Some examples:

1. IBM ECL technology
   Amdahl (and Motorola) => Fujitsu

2. (Amdahl 470 = Fujitsu M-series) is an upward program compatible with the 360/370.

3. Intel 8080 is a subset of new Nippon part being marketed now.

4. Motorola 6800 is a subset of new Futitsu parts just being built.

The strategy is clear: Remember the Chinese (?) 7.6 mm guns that were upward compatible with the 8 mm guns? Computers are the same...once a user buys into the "improvents" he is locked in.

GB/lp

Distribution: OC, PLM, Ron Smart, OOD

D I G I T A L INTEROFFICE MEMORANDUM 01832

SUBJ: MICROPROCESSOR DESIGN

DATE: 10-07-75
FROM: GORDON BELL
EX: 2236
MS: ML12-1/A51

* *

TO: FILE

* *

To: Demitrios Lignus/Duane Dickhut

Subject: ANOTHER MICROPROCESSOR DESIGN ALTERNATIVE FOR RK06/RSL

Larry Hodges is sending me a proposal for the design of a small (37 standard dips), fast (80ns), 4-bit-slice oriented microprocessor that he believes will interpret 11 ISP competitively (at 11/40 speed). It includes ROM, but not Unibus interface.

Steve is permitting Duane to interact with them to consult on the Unibus design and the ISP. In turn, we get their basic logical design...on a non-proprietary basis.
I don't believe it's what we want or need for a processor, but I hope it can be used to start to get us into a positive position wrt disks and their controllers. Duane, in turn, will interact with the disk group which I would hope now has at least one experienced processor designer. Someone in the disk group (or any other group that might take the design responsibility of the controller) must work with Duane for the evaluation. The purpose of this:

1. Get a disk control based on a microprocessor we wouldn't have designed.

2. Get additional, real live thinking on the controller design problem, instead of the mass of content-free design specs and minutes meetings that currently eminate.

Since he consults with Varian, CA, and GA it is imperative that he really not visit here and have much interaction with us. I especially don't want to tell them that it is a disk controller! (I don't believe the Tayler/Hodges group (6 of them) are particularly deep, but they are very clever logicians).

I will send the proposal when it arrives.

GB/lp

CC: Bob Kirk, OOD, Grant Saviers, Steve Teicher, Bob Armstrong

D I G I T A L INTEROFFICE MEMORANDUM

01833

PAGE 1

SUBJ: RE MEMO ON 2K ROMS

DATE: 10-07-75
FROM: GORDON BELL
EX: 2236
MS: ML12-1/A51

* *
TO: FILE
* *

To: Distribution

Subject: RE MEMO OF 10-1-75 on 2K ROMs

What's the story? Fairchild delivered their first 8K Bipolar ROMS in June and I have 4K Proms. Why are we fooling around with 2K ROMS in new products?

I believe we should get on the stick and start a strategy to enhance the 11 vis a vis more complex instructions: string, i/o, loop control. These instructions could be in the same format as VAX, permitting a convergence to VAX in 2 years.

They clearly give us a big mid-life kicker boost!

Who's going to pull this together? Lloyd, what's the list?

Let's discuss in Dick's staff meeting in a week or so!

GB/lp

Attachment

Distribution

Bob Armstrong
Jega Arulpragasam
Dick Clayton
Ed Corell
Bill Demmer
Lloyd Dickman
Duane Dickhut
Len Hughes
Malcolm Johnston
Chuck Kaman
Bob Kirk

[redacted]

Jim O'Loughlin
Steve Rothman
Al Ryder
Bob Stewart
Tom Stockebrand
Steve Teicher
Mike Tomasic

Attachment

[redacted]

D I G I T A L INTEROFFICE MEMORANDUM

SUBJ: ROM MICROCODE

DATE: 10-01-75
FROM: GORDON BELL
EX: 2236
MS: ML12/A51

* *

TO: FILE

* *

Subj: INCREASING SIZE OF ROM MICROCODE ON PDP-11'S VERSUS TIME

To: Distribution F/U 10/10

It's clear we've really (in retrospect) missed opportunities to easily mid-life kick all our processors as bipolar ROMS have gone from 1K to 2K. Now when they go to 4K (1 to 2 years) can we easily retrofit, to get double the microcode in the same board space without retooling, etc?

Lloyd Dickman is putting the VAX string stuff in 11/03. Are these candidates for 45, and 70 (which don't yet have the new 2K ROMS)?

Are there other operations to help these machines now?

Should we conscientiously plan this on new designs...it's only an extra bit in micro PC?

Please comment.

GB:mjf

Distribution

Bob Armstrong
Jega Arulpragasam
Dick Clayton
Ed Corell
Bill Demmer
Lloyd Dickman
Duane Dickhut
Len Hughes
Chuck Kaman
Bob Kirk
Jim O'Loughlin
Steve Rothman
Al Ryder
Bob Stewart
Tom Stockebrand
Steve Teicher
Mike Tomasic

F/U 10/15

01835

digital INTEROFFICE MEMORANDUM

TO: Ron Kanne PK3-2/F34
Herb McCauley PK3-2/F34

DATE: October 10, 1975

FROM: Gordon Bell

DEPT: OOD

EXT: 2236 LOC: ML12/1-A51

SUBJ: OFFICE AUTOMATION

Where's the minutes of our meeting re word processing/office automation with the numbers, etc?

What's the chance of getting the software prep people decent terminals with UC/LC (e.g. LA36 or VT52)? How can they prepare documents efficiently, cheaply, etc. on ASR33's?

01037

October 13, 1975

M. J. Sullivan
Spec. Comm. Programs
IBM
Arkmont, New York 10504

Dear Mr. Sullivan:

It was nice talking with you last week regarding the equipment which we need for our company technology exhibits. We intend to use the parts now with various technology exhibits, and eventually to have a museum, where they might be on permanent display. The parts will not be connected; hence, need not be functional.

The parts I would like:

Memory technology: read-only memory assemblies from 360/30 (capacitor), and other 1 or 2 models (e.g. 360/50 inductor)..
IC read-write memory from a 370 model. MOS ROM IC (48K bits) from IBM 5100.

Disks: large platter (only) from original RAMAC, IBM 1311 (basis of current series), and flexible (floppy) mechanism with a floppy.

Logic technology:
CPC or 60X relay assembly plus plug-board
704 flip-flop assembly.
360-SLT on a card (several cards) with a mother board and cable to show interconnects on gate.
370 IC package to compare with SLT (2 cards)

Typewriter I/O: 1050 and/or 2741.

Complete early relay calculator (e.g. CPC)

I appreciate your help.

Sincerely,

Gordon Bell
Vice President
Office of Development

GB:mjf

DIGITAL EQUIPMENT CORPORATION, 146 MAIN STREET, MAYNARD, MASSACHUSETTS 01754
(617)897-5111 TWX: 710 347 0212 TELEX: 94 8457

D I G I T A L INTEROFFICE MEMORANDUM

PAGE 1

SUBJ: COPIER-BASED PRODUCT

DATE: 10-14-75
FROM: GORDON BELL
EX: 2236
MS: ML12/A51

TO: FILE

SUBJ: COPIER-BASED PRODUCT WITH VIDEO INPUT

To: Distribution F/U 10/24

Is there a use for our copier which takes standard video input, and converts this to a picture?

It is low cost...and I hope good.

1. Since the IBM 5100 has video output, it could connect to it directly.

2. Also, we could "add-on" to all the terminals which have video output. (E.g. Beehive, HP2640, Tektronix graphics, Conrace, Monitors whatever their use.)

3. This may also be the right way to connect the copier to the new packaged systems.

4. For the new VT52, it is a clean way to get the copier.

Is it unique?----------

Would anyone want one?----------

Should we make up such a self-contained gadget?----------

How much?--------

How long?--------

GB:mjf

Distribution

Jim Bell	Rick Merrill
Ed Corell	Ken Olsen
Ken Fine	Bob Puffer
Len Halio	Mark Sebern
Al Huefner	Tom Stockebrand
Andy Knowles	Al Wallack
Bill McBride	John Wolaver

D I G I T A L INTEROFFICE MEMORANDUM

SUBJ: LSI-11

DATE: 10-14-75
FROM: GORDON BELL
EX: 2236
MS: ML12/A51

TO: FILE

SUBJ: DEBUGGING LSI-11 PROGRAMS

To: Distribution

Sam Fuller at CMU has a very nice multi-user interactive program for controlling a cadre of LSI-11's via multiple high speed lines (9600 baud). They use a particular monitor, but I'd believe RSTS or RT11 and BASIC would be a reasonable environment.

Conventional terminals control, etc., info to the LSI-11's. In this way, we end up with a better programming environment.

I'll send the manual for their system when it arrives.

This came out of their research in LSI-11 computer modules and the problem of coordinating and controlling them. Such a system would be ideal for a lab-teaching environment involving multiple machines.

GB:mjf

Distribution

Bob Bean	Charlie Spector
Duane Dickhut	Steve Teicher
Andy Knowles	Nat Teichholtz
Ed Kramer	Rob Vannaarden
Roy Moffa	Stu Wecker
	Al Wallack

D I G I T A L INTEROFFICE MEMORANDUM 01840

PAGE 1

SUBJ: PM STAFF MEETINGS

DATE: 10-14-75
FROM: GORDON BELL
EX: 2236
MS: ML12/A51

* *
TO: FILE
* *

SUBJ: RE YOUR PM STAFF MEETINGS

To: Malcom Johnston

The several issues which feel hot to me (and I'd like to attend):

Z. Why are there no software PM's in these meetings?

A. 5100 - Sebern/Christy. Hallo should probably be the person asked to report on this. Also, he should NOT come alone. I believe we want segmentation of problems into the hierarchy of levels in my memo, i.e.:

1. Packaging/hardware--Clarke (& Teicher)
2. Operating System + file RT-11--Munson
3. Languages--Ham (+Thissell for APL)
4. Applications subprogram--actually Fauvre to pull it together; but also each P/L.
5. Customer pre-programmed packages--particular P/L's.
6. Sales interface/Service/Software support

We have a 5100 in house (my office now). Hallo is coordinating its evaluation vis a vis: documentation, human interface, APL and BASIC performance (I want #'s before we talk about it).

Rumour from Al Perlis, Professor at CMU-now Yale (who says it's the greatest invention yet): two teams were sent to do the design. The winner used the 370/145 package (about 40K bytes(with emulator-assist and the gadget also interprets the 370. The loser started from scratch. If this is true, watch out. A mini 370 in a small box...which according to our proposal to ARPA for a PDP-10 like it, is perfectly reasonable and natural. From our analysis so far it ain't true; it's merely an 8080-type design.

B. How can we use new larger ROMS, PROMS to enhance 11's?

This may be a can of worms. My view is that many features of VAX can be put into 11's now such that we see a gradual merging of VAX and 11/PDQ-45-70 -> VAX. The possible primitives:

SUBJ: PM STAFF MEETINGS DATE: 10-14-75
FROM: GORDON BELL

1. Strings.

2. Fast context switching (e.g. take stuff in M and wire it in).

3. VAX loop control is really good.

4. Possibly field/bit/32-bit operations.

These are quite well defined ala VAX, and must be identical!

C. Address extension of 11. Note, the 2 attached memos with time estimates. Neal/Hassett are going off to explore what we could do here by getting a few people to explore how. My hunch:

   0. Stay away from I/D.

   1. Extend M/D-based primitives ala Cutler's suggestion; not clear we have to extend program-size space. Extend RT ala Bruce Leavitt.

   2. Wire-in (microprogram) these into PDQ-45-70 to get reasonable times (i.e. 2 microseconds). Youse may recall this scheme in the original segmentation proposal. Note, this would permit competition with the rumoured DG machine. Also, it would probably defuse the large VA problem by providing access to large arrays. It would run very respectably.

D. General architecture control problem.

Who looks out for the 11? (Note, a group went off April 1 and got vaxcinated with a new machine...while I think they succeeded in defining an architecture which is by far the best I've ever seen, truly love, and intend to see that we build, we do have a transition time where competitors can come at us pretty hard.)

GB:mjf

Attachment

cc: Dick Clayton
Bruce Delagi
Bill Demmer
Bruce Leavitt
Clay Neal
Larry Portner
Al Ryder

digital INTEROFFICE MEMORANDUM

TO: Gordon Bell

DATE: October 6, 1975

FROM: Dave Cutler D.N.C.

DEPT: Advanced 11 Engineering

EXT: 5670 LOC: ML3-5/E35

SUBJ: EXTENDING VA SIZE

RE: Your memo of 1-October-1975

OCT 07 1975

There is a way to modify both RSX-11M/D (without impairing memory protection) so that users could change the address space and thereby get access to large arrays. The technique was suggested by Cutler in October, 1971, by Christy in the spring of 1975, by Lev in the summer of 1975, and implemented by XDS on the 940 timesharing system about seven years ago! I do not know why it was never accepted, perhaps because it required explicit management by the user.

The technique is very simple. The operating system basically implements three primitives:

1. Create segment (name, length).

2. Delete segment (name).

3. Remap segment (name, virtual address, access).

As a user executes, he creates segments (which may be of variable length and require more than one KT register to map) and remaps to them at will. He thus can effectively have a very large address space. The remap time would be on the order of 300 to 400 μs; and therefore, the assumption, that once remapped to a segment, a user program will execute considerably longer before again remapping.

The implementation time? A mere six man months (a SWAG, of course).

/s

cc: Ron Brender
Janice Carnes
Dick Clayton
Peter Christy
Bill Demmer
Ron Ham
John Levy
Al Ryder
Pete van Roekens

digital

INTEROFFICE MEMORANDUM

TO: OOD Staff

cc: Stan Olsen
Bill Demmer

DATE: September 26, 1975
FROM: Larry Portner
DEPT: Software Development
EXT: 2471
LOC/MAIL STOP: ML12/A62

SUBJ: OOD Agenda - October 2, 1975
Larry Portner, Chairman/Secretary

10:30	Review Minutes Review Agenda		
10:35	Budget Review	All	(60 mins.)
11:35	OOD/Marketing Committee Interface	All	(40 mins.)
12:15	OOD Space Guidelines	P. Laut	(15 mins.)

FUTURE AGENDA ITEMS

- Management Development. (J. Cronkite/M. Abbett) 10/9
- Sales Meetings. (D. Clayton) 10/9
- Low Power Schottky help. (V. Bastiani/OOD) 10/9
- Honoraria Policy. (G. Bell) 10/9
- What is Resolution of DEC-20 Memory Strategy? (J. Leng/H. Lemaire) 10/16
- Commercial/OOD Interface. (S. Olsen) 10/23
- GM. (T. Johnson)
- Report on In-House 2-Year PDP-11 Usage Strategy. (Computer Resource Co.)
- QCMS Defect Reporting System. (J. Smith/M. Pecore)
- Is There a Field Integration Plan Yet? (J. Smith/J. Shields/D. Clayton/B. Puffer)
- Is There a Formal Action Plan that Allows Follow-up on Field Oriented Product Safety Problems? (J. Shields/R. Minezzi)
- Block Model Strategy Resolution. (J. Marcus/L. Portner)
- Is Action on ECO Control Called for at This Time? (J. Marcus)
- What is Happening to Make Systems a Reality in the Way we do Business? (D. Clayton)
- What is 3 Year Serial Bus Strategy? (V. Bastiani/D. Clayton)
- Bubble Memories

Expected attendance at OOD Meetings:

	GB	LP	RP	RC	PL	MA	JM	HL
10/2	X	X	X	out	X	X	out	X
10/9	X	X	X	X	X	X	X	X
10/16	X	X	X	X	X	X	out	X
10/23	X	X	X	?	X	X	X	X
10/30	X	X	X	X	X	X	X	X

digital INTEROFFICE MEMORANDUM

TO: Gordon Bell ✓

CC: Ron Brender, Janice Carnes, Dick Clayton, Dave Cutler, Pete van Roekens, Ron Ham, John Levy, Al Ryder, Bill Demmer

DATE: October 8, 1975

FROM: Bruce Leavitt

DEPT: 8/11 Software Development

EXT: 5465 LOC: ML5-5/E40

SUBJ: Extending VA Size

OCT 10 1975

RE: Your memo of October 1, 1975, same subject

FORTRAN IV version 2 will support large virtual arrays (32,767 elements), as planned.

Time frame: about 9-12 months

Systems: Direct access I/O VAs on all FORTRAN IV systems (RSX/IAS, RSTS/E, RT-11);

KT-11 VAs on RT-11 only.

If RSX-11M/D can provide fast (.3ms) remap facilities for non-privileged tasks, we will plan support.

*FORTRAN IV KT-11 VAs have been implemented under RT-11; we are currently debugging and testing performance.

/nw

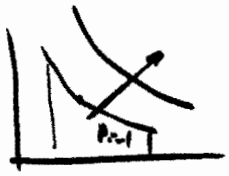
9

Note to Schein, Ed Roberts.

①

Drive → I.Q. → Industry (drive)

$P = E \times I$



---

② Characterize Skills Inventory

a. ⟹ Self improve
b. ⟹ location of gen
c. ⟹ project gen
d. ⟹ Corp.

Theory / model of info. flow.
- comm + teachg across discom
- Multiplicity.

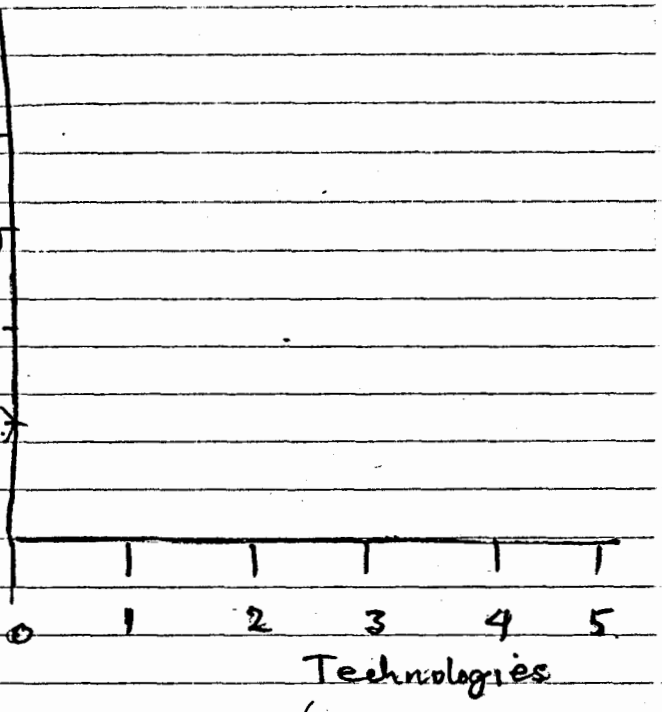
7. Recog. top few in disciplin
6. pushed s-of-art, most likely has patents
5. has done s-of-art dev.
4. accept (sole) member of project team in this area
3. took a course, knows, could be trained (OK if
2. reads Sci Am art
1. Can listen to convers. + detects a few words
0. Knows nothing.

To: OOD cc: Shel Davis

Subject: Characterizing Ourselves in Mgmt - Technology Space

Re: Jungle Mtg. Mgmt. 21 May 78.

Span → / # people ↓	3	4	5	6	...	9	Levels
depth ↑	364	1365	3906	9331		66430	5
	121	341	781	1,555		7,381	4
	40	85	156	259		820	3 (area)
↓	13	21	31	43		91	2 Σproj
	4	5	6	7		10	1 (proj.)
	1	1	1	1		1	0



Competence

0 – can't spell the area

$$T = \sum_{T=i}^{T=n} \text{Competence}_i$$

½ – understands an area, could bone up and enter an area.

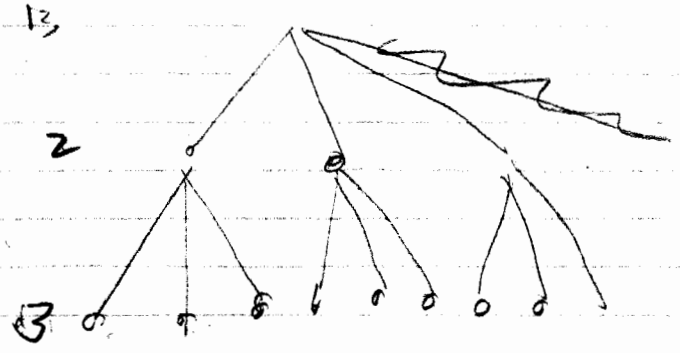
1 – average member of group works in an area.

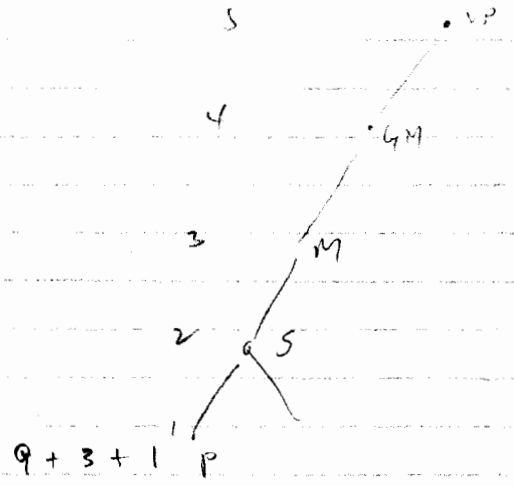
1½ – above average in area

2 – authority in the area (1-2 top in company)

2½ – imagine 1-10 persons in world.

d = 13,





$$\sum_{d=0}^{d=2} s^d + s^{d-1} + 3^2$$

$$T = \sum_{d=0}^{d=2} s^d + s^d$$

$$T = \frac{s^d - 1}{s - 1}$$

$$\frac{17 - 1}{2} = \frac{16}{2} = 8$$

$$\eta_l = \frac{s^{d-1}}{(s^d - 1)/(s-1)}$$

$$\eta_{l-1} = \frac{s^{d-1} + s^{d-2}}{(s^d - 1)/(s-1)} = \frac{s^{d-2}(s+1)}{(s^d - 1)/(s-1)}$$

$$\approx \frac{8^{6-2}(8+1)}{(8^6 - 1)(7)}$$

Gordon

GB0001/33

digital interoffice memorandum

Subject: Our Market/Product-Positioning/Growth Dilemma

To: Marketing Committee
OOD

Date: 3/19/79
From: Gordon Bell
Dept: OOD
Loc: ML12-1/A51 Ext: 223-2236

Right now we must be especially concerned about the large 3+ decade price range of systems required in our many, varied (applications) markets. Consider the following viewpoints.

We've got to lose market share which in turn usually means higher costs overall, and possibly lower profits because:

a. DEC future growth at 26%/year is lower than the past 36%/year growth (see Fig. 1).

b. The technology improvements continue to open up a new low end at an increasing rate. Note the range increase as shown in Fig. 2, and the range factor, ignoring the terminals and 10/20 is plotted in Fig. 1. Prices of low end systems decline at 10% to 20% per year, limited only by the mass storage capability whether it be ram, bubbles, tape, floppy, etc.

c. Over most of our market price range (i.e., applications) the market growth rate is constant or increasing.

d. Our market and sales strength seems to be (ordered) in the following price bands:

   i. 100K-250K (11/70, 2020, 780)
   ii. 40K-100K (11/34)
   iii. 1K-2.5K (terminals)
   iv. >400K [both bands 250-625-1.6] (36-bit)
   v. 16K-40K (low end 11/34 box and OEM RL based, plus Datasystems)
   vi. 6.25K-16K (PDT, WP)
   vii. 2.5-6.25 - almost non-existent, except for hardware-only components; small PDT's are here and the new WPS should be

e. Note, the market share, base and growth is highly diverse over our range of interest, as shown in Fig. 3.

f. It's impossible to grow enough to keep market share in all these price areas. Therefore, we should understand the ultimate

deleterious effect. By contrast, see Fig. 1, all our competitors (except IBM - who has divisions) seem to be in a narrower range, growing faster and are more profitable.

At last IBM has noticed us and is descending over the price-performance space like a bunch of locusts whose population is growing exponentially. For some time it's clear we've been exempt from IBM competition as they used to have really crappy products in this space. Now they're interested in the same growth, system size, and computing style we see.

a. The useful (i.e., 148-class with 0.5 Mbyte memory) 360/370 has come into the under 250K, mini market. Figures 3, 4, and 5 show how this series has stopped at the price boundary as more software is added and larger memories have been needed. Now even IBM can't fill all these primary memories with operating system and the cost has broken through with the lower cost/byte memory. Also, with the latest announcements, they have for the first time, machines that are competitive with the 10/20.

b. They have a mini with the Series 1 positioning at the 04/34 (one of our key strenths). The new enhancements get the price down to broaden its coverage into the 03. They may go after chips here, too. They'd really be smart to get an independent semi-house to make chips available.

c. The System 38 is targeted at the 11/70 class machine, our highest revenue earner.

d. The 8100 is targeted both at the 34 and 70 to do the system's off loading that many of our minis are sold for.

e. They're building user personal computers in the 5100.

Costs to engineer systems of a given price are increasing with time from several perspectives as can be seen in Figure 6. (I'll verify these costs later.) The cost of the minimal mini is rising from the situation in 1972 where it was built from standard MSI components.

a. IBM and semiconductor technology opportunities are raising the ante at the higher ends by using gate arrays to build higher performance, more cost effective (lower cost) systems. These cost proportionally more because:

   i. Special gate arrays are required, increasing the number of circuit types.

   ii. The machine is higher speed by more parallelism and is therefore more complex.

   iii. More RAMP features are required.

   iv. Mid life extensions should be built in to protect and extend the investment.

b. Intel and semiconductor technology opportunities are raising the ante at the low end because we must have DEC ISP chips for small systems. Gordon Moore has observed that the number of man-months/chip to design a chip is doubling every 2.7 years. These chips aren't taking advantage of maximum densities, either.

c. Our product size, system structure and diverse markets engender almost unbounded commitments (see the typical situation for the Large Systems' area shown in Fig. 7). The total number of products announced, is approximately the product of:

base hardware x
special front-end, back end hardware x
operating systems x
network options x
applications and data base hardware and software options x
any CSS products

i. There are many base hardware systems, tending to include other special hardware each of which has to be tested in a combinatorial fashion.

ii. Depending on the system size and the dedicatedness (versus general purposeness), we seem to take on a lifetime system enhancement-support commitment (see attachment for large). For example, only recently have we been able to decommit TOPS 10 enhancements on KA10's.

d. We have multiple families, all of which our customers expect, to be evolved and their ranges expanded forever! This means that whatever problem we think exists above, it is actually 4 x worse. Or ignoring ranges that have only one product in them 2-3 x worse than first glance.

<u>There are several reasons to focus on <250K systems</u>.

a. With the newly announced Federal Channel standard, the price line is 250K to define a mainframe. The 780 is excluded.

b. Various government groups can purchase computers under 250-300K without OMB approval.

c. For many large organizations, a selling price under $250K doesn't require the authorizations that a $500K purchase requires.

d. IBM isn't as strong here <u>now</u> as they seem to be headed for.

<u>DEC's ability to introduct new products is actually more limited and more expensive</u> than we think because all products tend to be marketed through all groups.

The expanding 3+ decades range of products presents a problem

---

because:

a. Field Service, Software Support, Sales and Manufacturing are faced with much of the product introduction complexity and costs (paralleling development cost) that engineering faces.

b. Although we design many products, the introduction cycle and ability to absorb is clearly one limit.

c. With the high rate of growth and turnover in all groups, including sales. For example, it's impossible to believe that no matter how we segment, a salesman is being asked to cover and leave too wide a range.

d. It feels like we need the much better segmentation according to size, because costs over the whole P and L vary greatly by size! In engineering I'm attempting to have much clearer segmentation through funds firewalling and organizational segmentation! (I feel we need the same in the other organizations.)

GB:ljp

Attachments

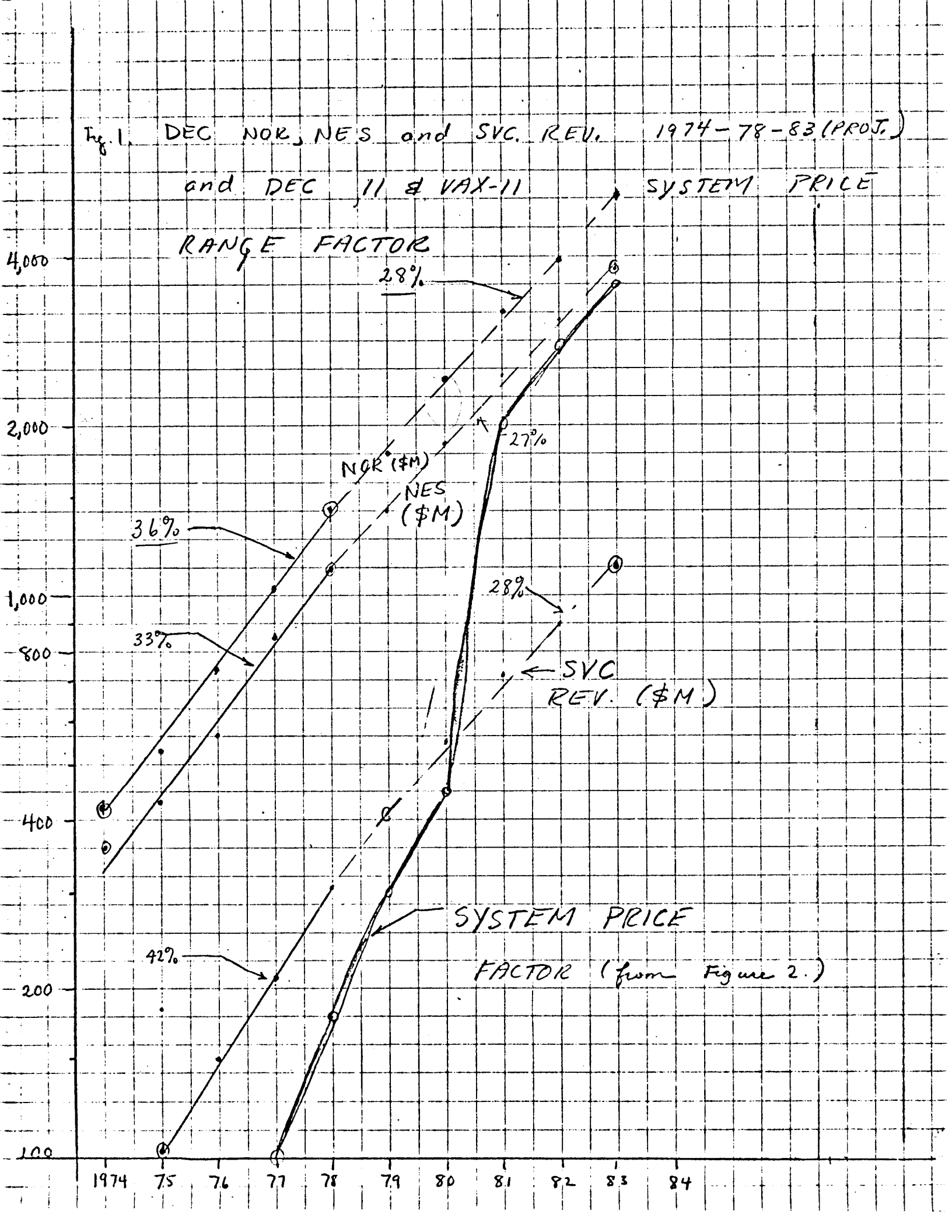
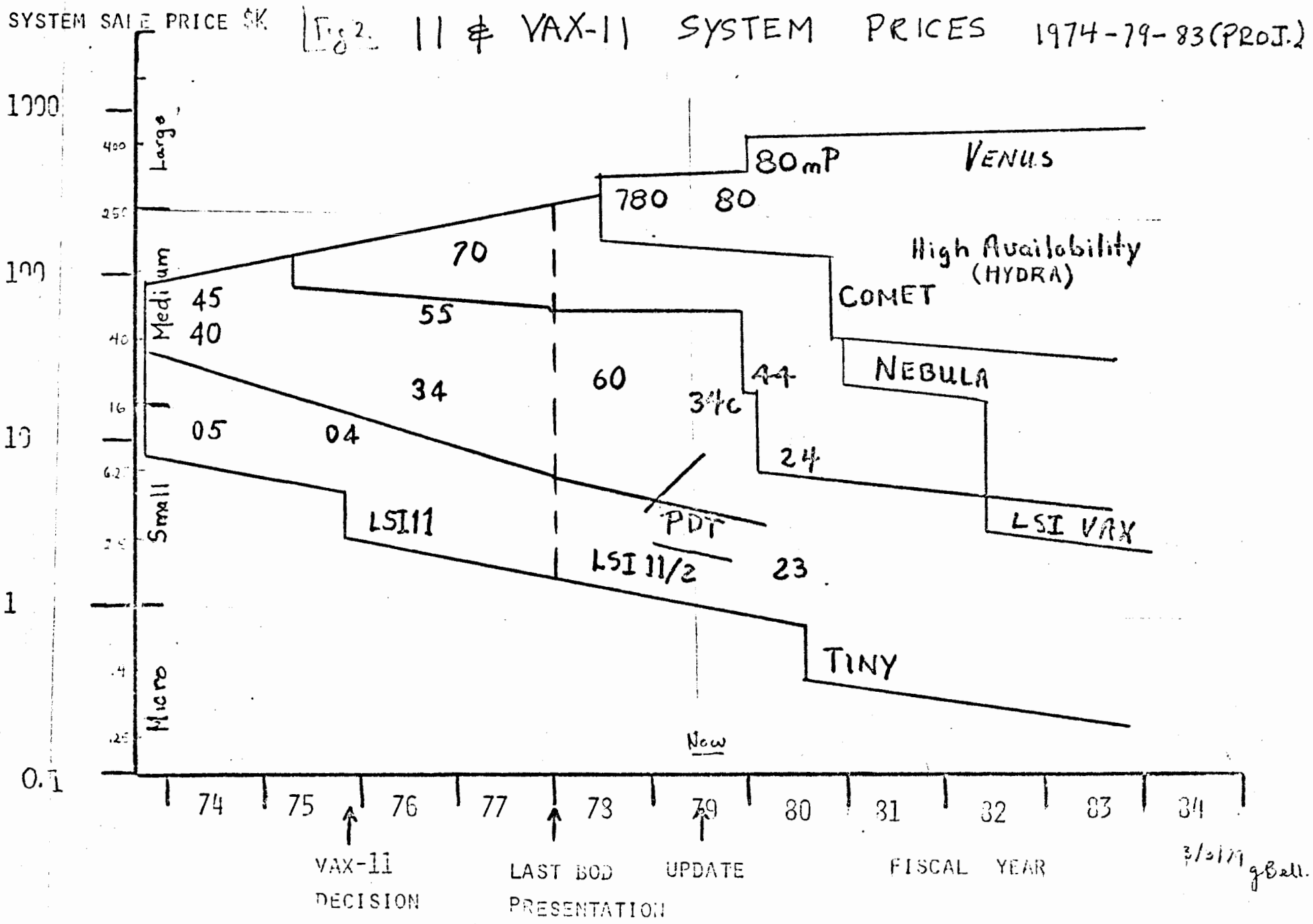


Fig. 1 DEC NOR, NES and SVC. REV. 1974-78-83 (PROJ.)
and DEC 11 & VAX-11
SYSTEM PRICE
RANGE FACTOR
28%
27%
NOR ($M)
NES ($M)
36%
33%
28%
SVC REV. ($M)
SYSTEM PRICE
42%
FACTOR (from Figure 2.)
4,000
2,000
1,000
800
400
200
100
1974
75
76
77
78
79
80
81
82
83
84


SYSTEM SALE PRICE $K
Fig 2. 11 & VAX-11 SYSTEM PRICES 1974-79-83 (PROJ.)
1000
100
10
1
0.1
Large
Medium
Small
Micro
400
250
40
16
4
.25
80mP
VENUS
780
80
70
High Availability
(HYDRA)
COMET
45
40
55
NEBULA
34
60
44
34c
05
04
24
LSI VAX
PDT
LSI11
LSI 11/2
23
TINY
Now
74
75
76
77
78
79
80
81
82
83
84
VAX-11
DECISION
LAST BOD
PRESENTATION
UPDATE
FISCAL YEAR
3/1/79 gBell.

Competitors' Products, Market Share, Market Size.

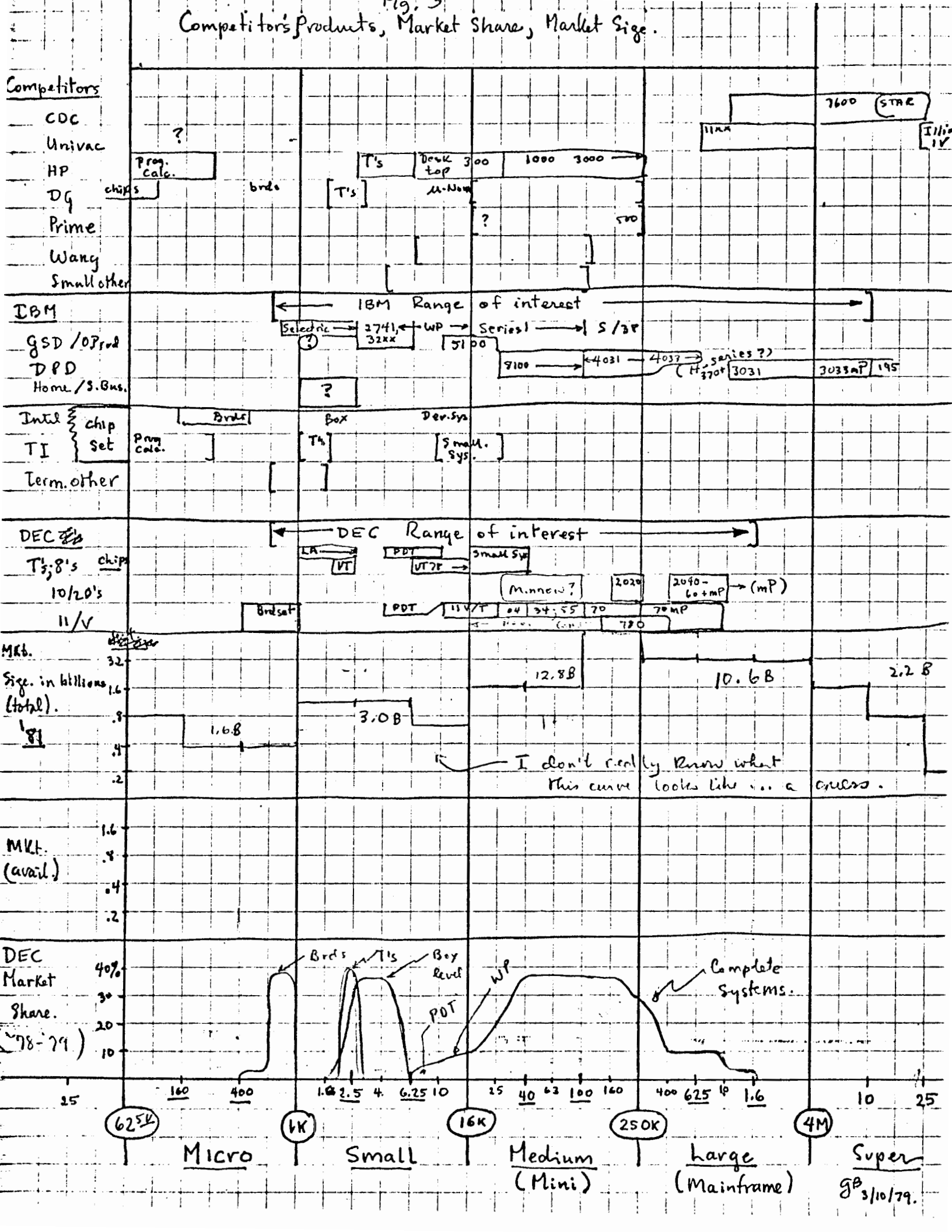


Fig. 4 DEC Introductions versus time. (Ship date)

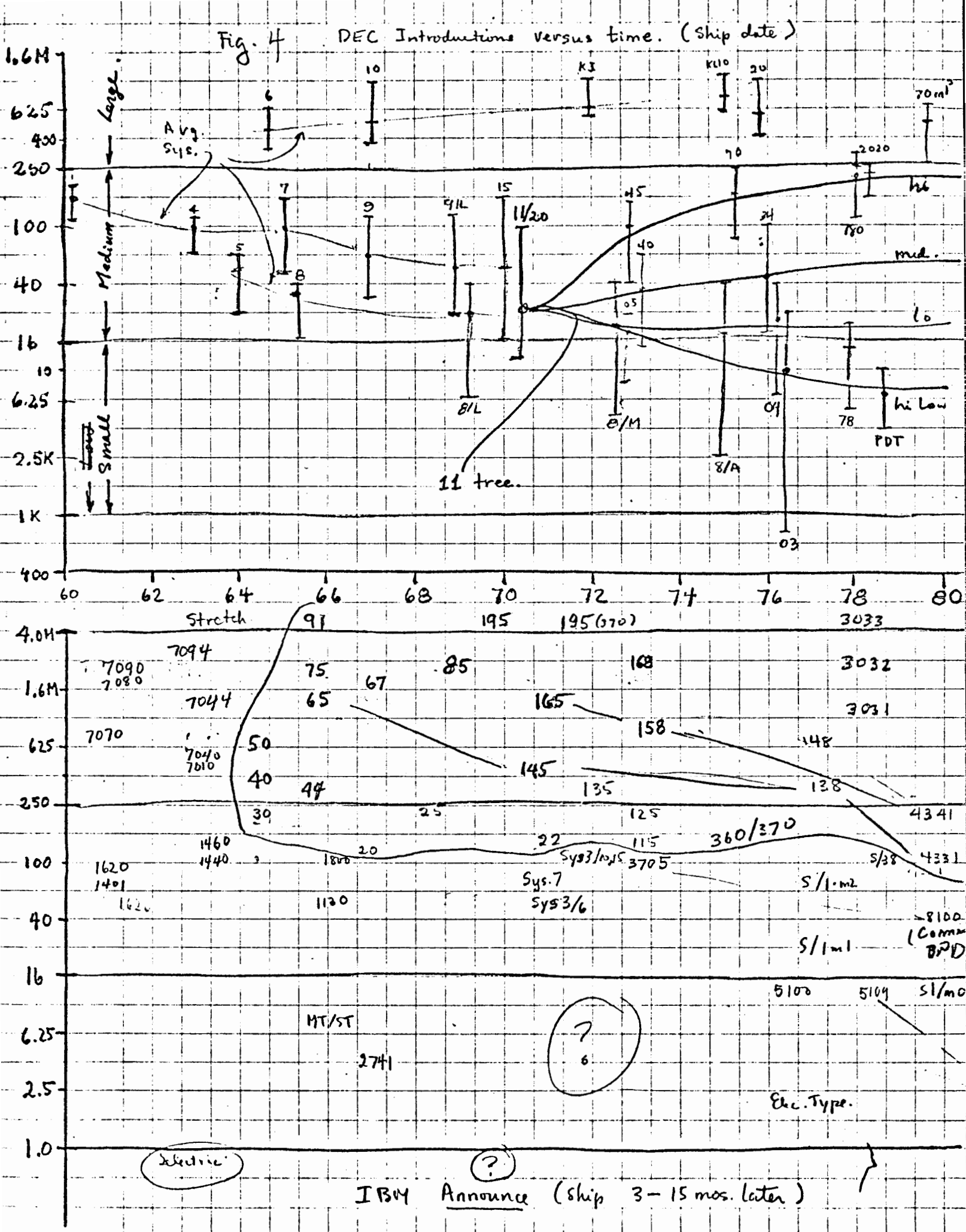
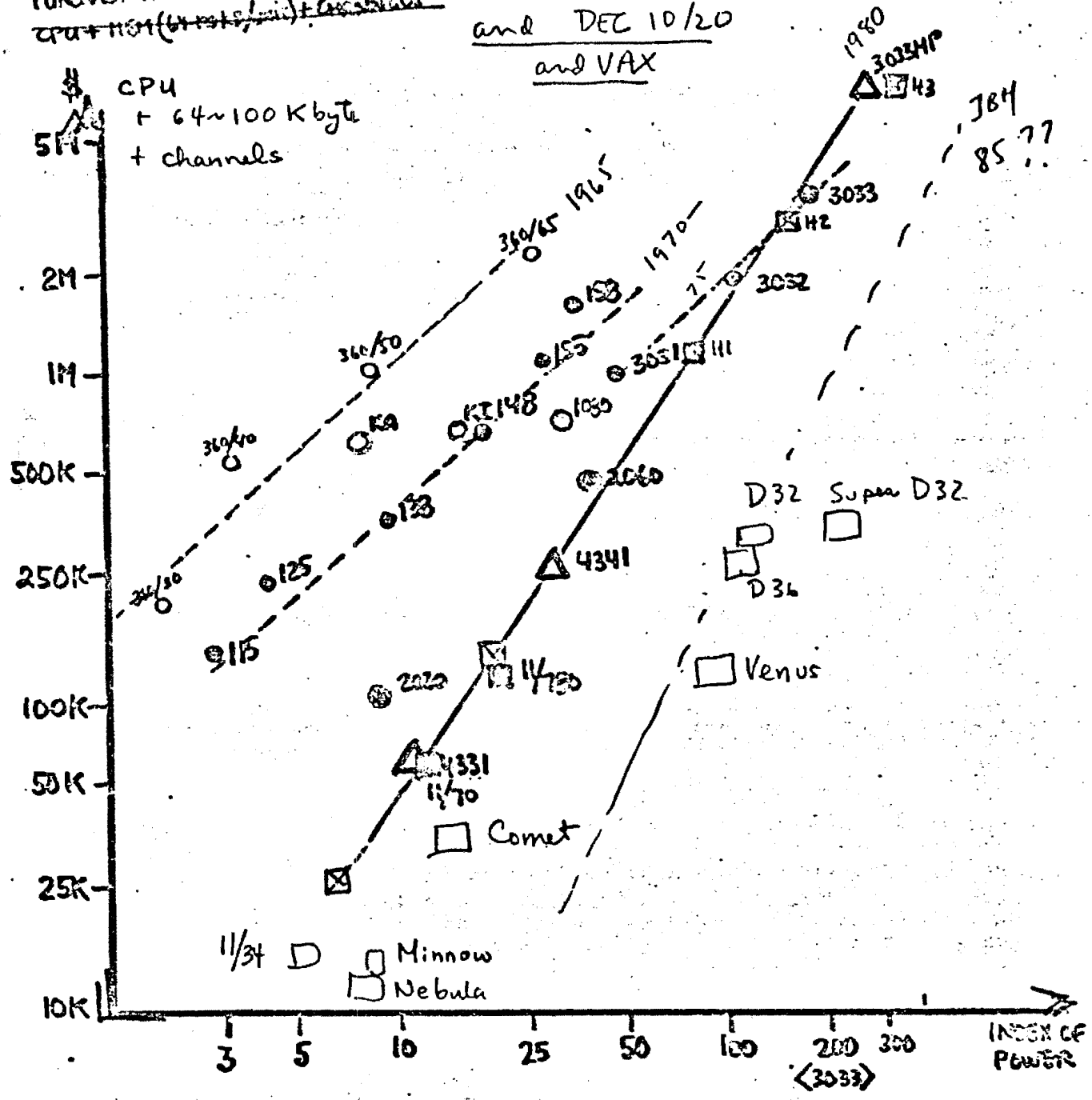
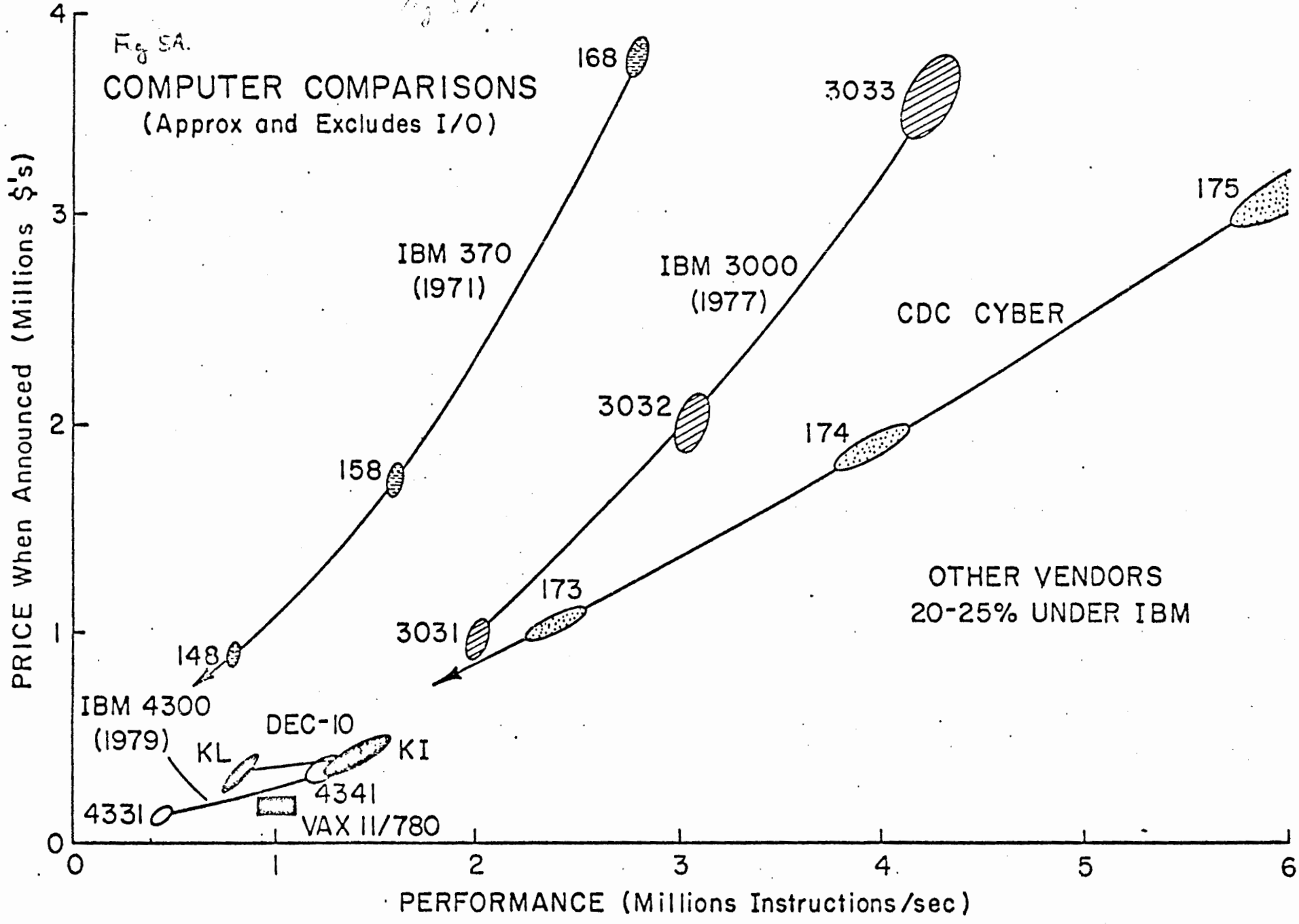


Fig. 5 Price versus Performance of IBM 360/370 and DEC 10/20 and VAX



Ulf Fagerquist
3/79

Copy to Gordon



FEB. 79

Est.* Development Cost versus System Size for various times

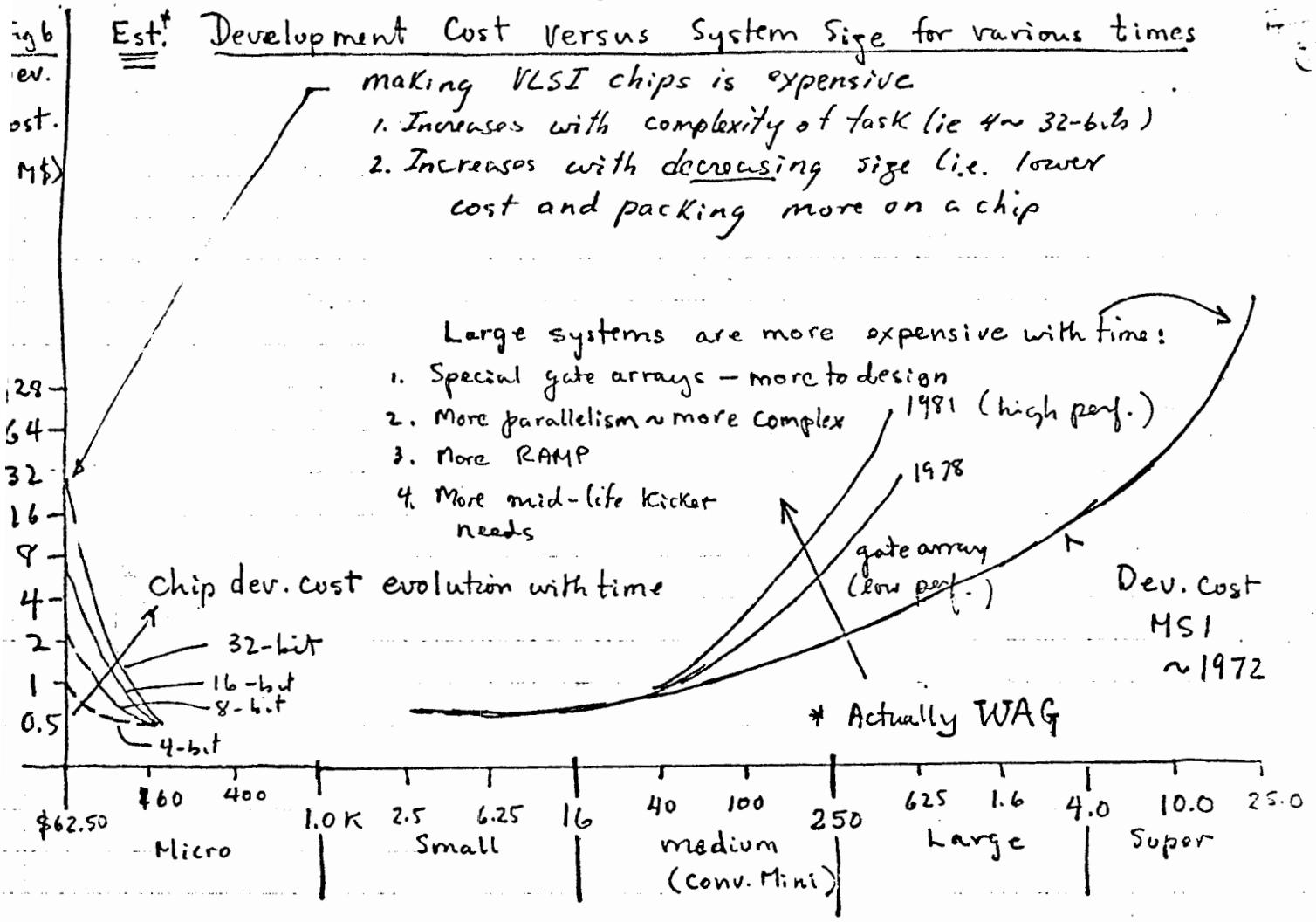
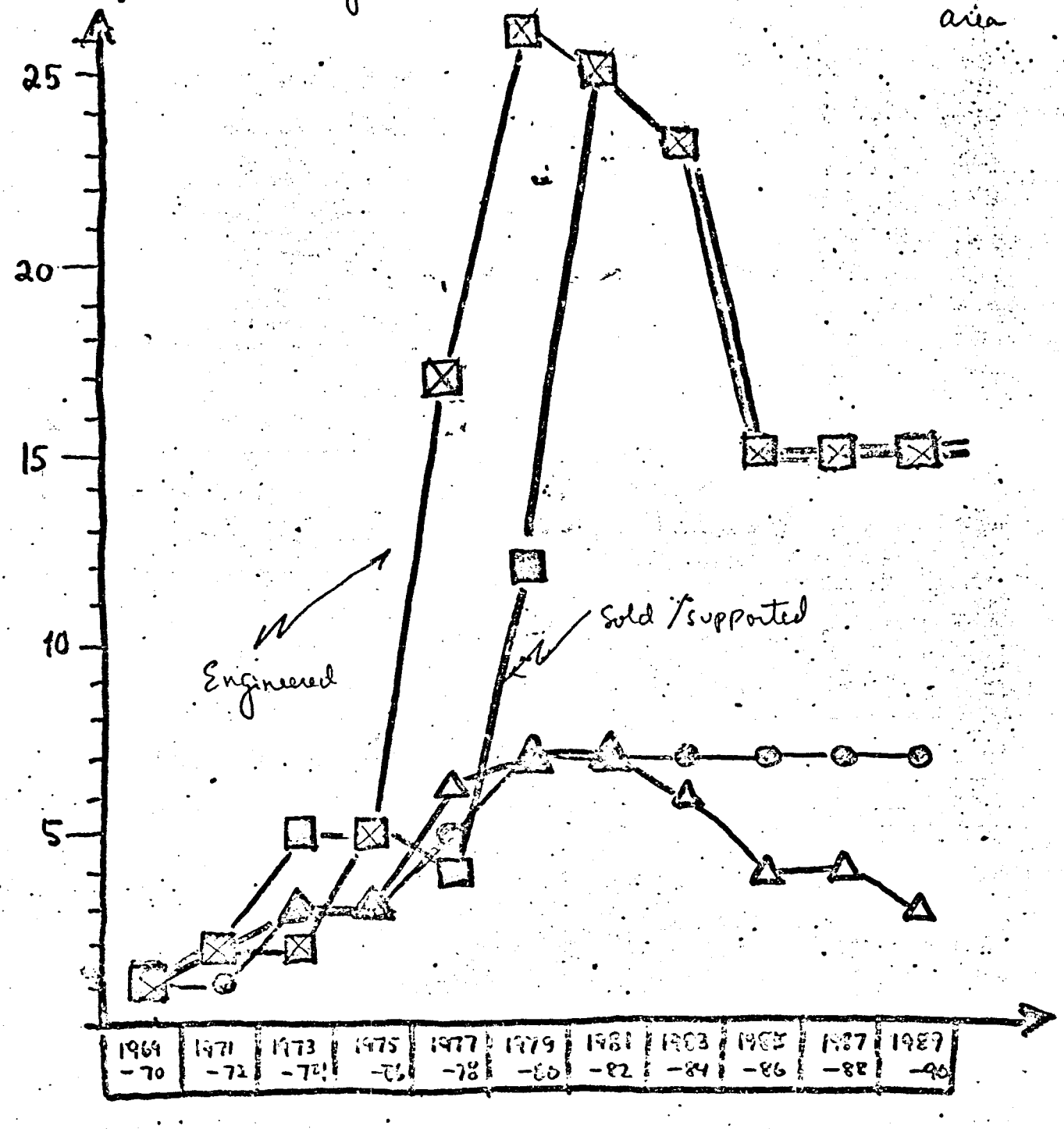


Fig. 7.

NUMBER OF... Systems to be tested/supported in 36 bit area



△ = HARDWARE SUBSYSTEMS supported

○ = SOFTWARE SUBSYSTEMS "

□ = COMBINATIONS SOLD (SEEN OUTSIDE ENGINEERING)

⊠ = COMBINATIONS MANAGED BY ENGINEERING

D I G I T A L INTEROFFICE MEMORANDUM

DIST:

Dick Clayton	ML12-2/E71	Jim Cudmore	ML1-5/E30
Bill Demmer	TW/D19	Ulf Fagerquist	MR1-2/E78
Bill Hanson	ML1-4/P11	Win Hindle	ML10-2/A53
Bill Johnson	ML3-5/H33	Ted Johnson	PK3-2/A55
John Kevill	ML3-6/E94	Andy Knowles	ML10-2/A52
John Leng	MR1-1/F35	Bill Long	ML10-2/A57
Julius Marcus	MK2/C37	John Meyer	ML12-1/A11
Ken Olsen	ML10-2/A50	Stan Olsen	MK1-2/A57
Larry Portner	ML12-3/A62	Bob Puffer	ML12-2/E38
Jack Shields	PK3-2/A58	Bill Thompson	PK3-2/C12

Gordon

Digital Interoffice Memo

Subject Gene Amdahl's Enjoyable Talk Last Week at NATO Summer School

To Distribution

Date 20 SEP 76
From Gordon Bell
Dept OOD
Loc . ML12-1 Ext . 2236

F/U 9/29

He was director of ACS IBM Menlo Park California 1966-1969 and left because he could not build a large profitable 360 I didn't find out how much of Amdanl Corporation's development was done at IBM, or how much time he spent fund raising there but he appears to be highly ethical

The decision to leave IBM was based on his inability to get policy changes that would permit large machines to be built The two he discussed were 1. The uniform allocation of overhead such that large machines could be made profitably and 2 Poor performance internal component purchases were forced.

He claimed the high end expenses (i e 370/168) were less than the 158 by a significant amount because the customers were sophisticated and self-sufficient Indeed this group put the "independents" in business. The policy supports mid-range thrust. In fact, the support for a 145 is higher since the customers don't know what they're doing. The range is shown in the attached figure. Can we try this representation for our sales? It matches the distribution for corporations NOR.

The components supplier within IBM/Essex Junction?) was not performing acceptably to support large machines in fact it was a marginal supplier of the 168. The System Managers had to "pay" and couldn't go outside.

Amdahl Corporation is predicated on these two policies plus the changing ratio of the processor to cover a wider range!. He doesn't see how IBM can make high end machines, nor why it would want to put him out of business. His machine provides a high end blanket for the 370. I believe he also will push multiprocessors to "extend" his range in the same way as the 168 and thereby pick up more of the high end tail in much the same way a lower price ratio for the CPU tends to "widen" the range He is also working on other products.

His support (console) machine is a NOVA and he's invited me to come present the PDP-11 to them and see the factory/machines in Sunnyvale

---

Who wants to go visit with me?

Do you believe his strategy is viable?

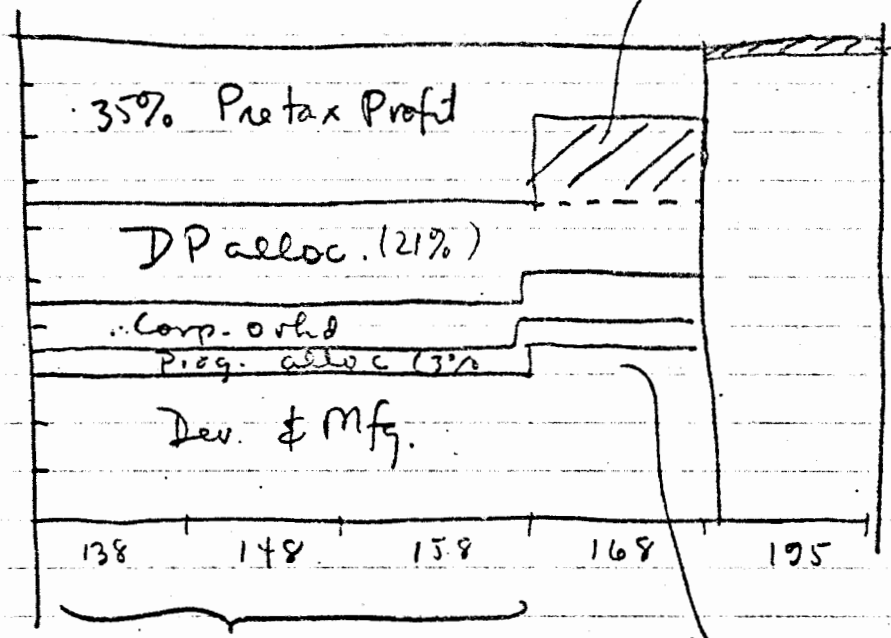
GB ljp

Attachment

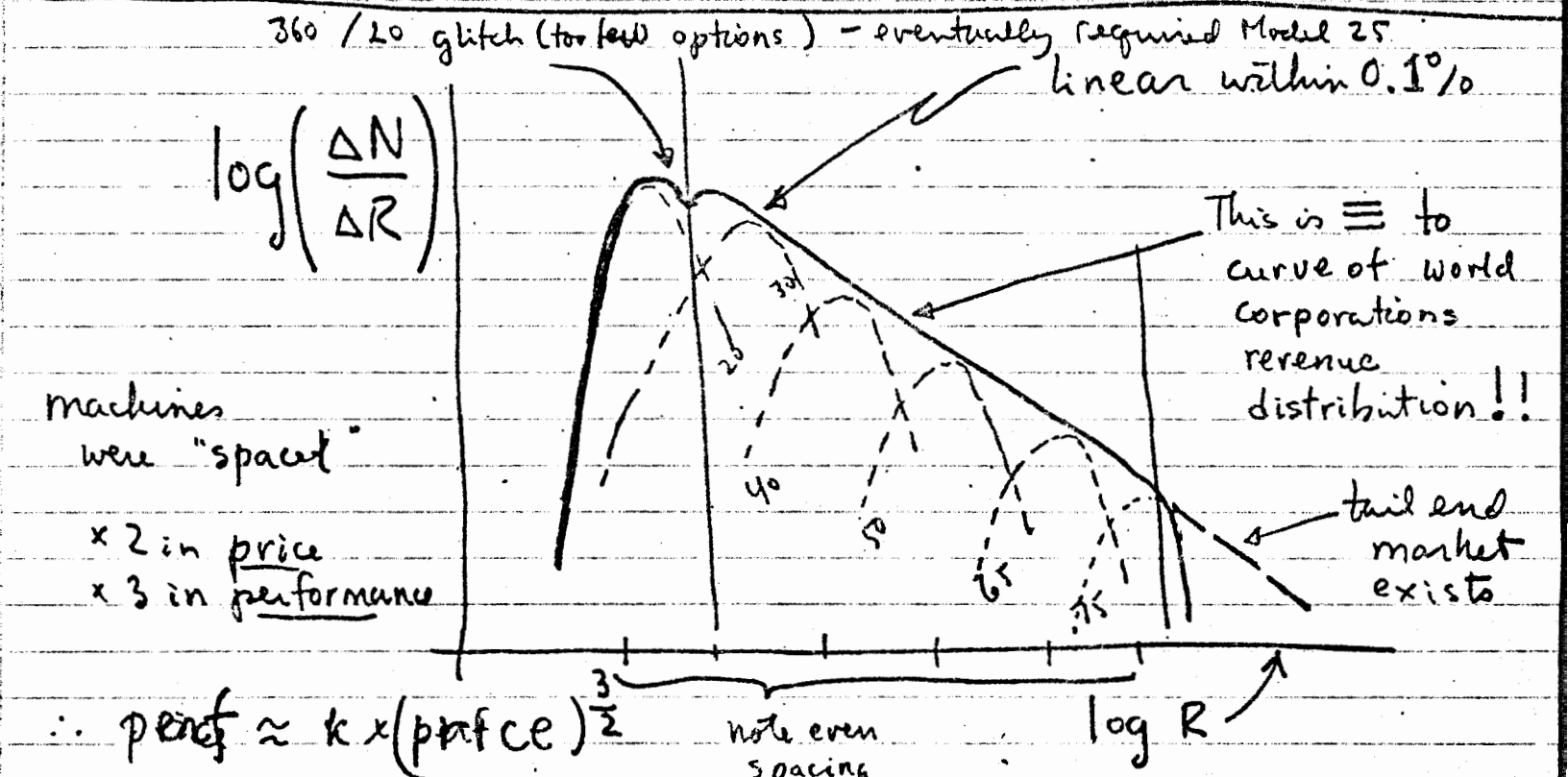
Distribution

Marketing Committee
Janice Carnes
Bill Demmer
Bill Kiesewetter
Julius Marcus
Jerry Todd
OOD
Bruce Delagi
Jake Jacobs
John Leng
Larry Tashbook
Mike Tomasic

Dist. of IBM's Profit within 370.



# Machines	?	?	5000	900	19



$\therefore$ perf $\approx k \times (\text{price})^{\frac{3}{2}}$

$\frac{d(\text{perf})}{d(\text{price})} \propto \frac{3}{2}$

method of "measuring" revenue / price for IBM

D I G I T A L INTEROFFICE MEMORANDUM

DIST

Dick Clayton	ML5-2/E71	Ulf Fagerquist	MR1-2/E78
Arnie Goldfein	ML12-1/A16	Win Hindle	ML5-2/A53
Ted Johnson	PK3-2/A55	Andy Knowles	MR2-2/A52
Henry Lemaire	ML1-4/A97	Julius Marcus	PK3-1/M29
Stan Olsen	PK3-1/A57	Larry Portner	ML12-3/A62
Bob Puffer	ML1-3/E38	Bill Thompson	ML12-1
Janice Carnes	ML5-2/E71	Bruce Delagi	ML12-1
Bill Demmer	ML3-5/E35	Jake Jacobs	PK3-1/M33
Bill Kiesewetter	MR1-1/M76	John Leng	MR1-1/F35
Julius Marcus	PK3-1/M10	Larry Tashbook	PK3-1/M33
Jerry Todd	PK3-2/S14	Mike Tomasic	ML21-1/E81

Gordon

Digital **Interoffice Memo**

Subject: The 10 and 11 As Seen By A Smart Buyer

To: OOD, OPC, PLM
Janice Carnes Al Crawford
Bill Demmer Steve Teicher
Mike Tomasic Pete Van Roekens

Date: 20 JAN 77
From: Gordon Bell
Dept: OOD
Loc.: ML12-1 Ext.: 2236

Pete Warter, Department Head at the University of Delaware and former high level engineer at Xerox, came to us (as a buyer) with the following view:

System	No.Users	Price(K$)	Mp.size	Flexibility	Job Size (32-b/w)	Capital Cost/ User (K$)
11/03	1	10-15M	28K (16b)	medium	8-16K 32-64	10-15K
11/34 (11/60?)	15	80	96K (16b)	low (BASIC)	8-16K	5
11/70	25 (35?)	150 200	184K (16b)	high (UNIX)	16K 64	6 5.6
2040	25	450	256K	high	128K 512	18
2050	35	650	384K 1/3	high	256K 1024	18.5

His premise:

0. The 11/70 and 2050 perform about the same except the 11 is faster due to being tailored and having less address bits. One pays for this.

1. Buy both 11/70 and 2050, but work to get most jobs onto 11/70 (where it's the cheapest) because it's significantly more cost effective.

2. Only 1 parameter matters to a vast # of users (besides the software investment)...that's job size!

3. The generality of 20 really costs and probably isn't worth it versus Unix.

Note how easy it is to separate the computers:

1. 11/70 for best cost/performance (by factor of 3!)

2. 20 for languages and large computational jobs

When can we understand products as users do?

GB:ljp

D I G I T A L INTEROFFICE MEMORANDUM

DIST:

Janice Carnes	ML3-3/E71	Al Crawford	PK3-2/A56
Bill Demmer	ML3-5/E35	Steve Teicher	ML5-2/E93
Mike Tomasic	ML3-3/E71	Pete VanRoekens	ML3-3/E71
Jim Bell	ML3-4/E41		
Al Bertocchi	PK3-2/A56	Bill Chalmers	MR2-2/M67
Dick Clayton	ML3-3/E71	Bruno Durr	PK3-1/S44
Ulf Fagerquist	MR1-2/E78	John Fisher	PK3-2/A93
Jack Gilmore	NT	Arnie Goldfein	ML12-2/A16
Win Hindle	ML5-2/A53	John Holman	PK1/P84
Irwin Jacobs	PK3-1/M33	Ted Johnson	PK3-2/A55
Pete Kaufmann	ML1-4/A54	Dave Knoll	ML1-4/P69
Andy Knowles	MR2-2/A52	Ed Kramer	MR2-4/M16
Bob Lander	PK3-2/F33	Bob Lane	PK3-1/M45
Henry Lemaire	ML1-4/A97	John Leng	MR1-1/F35
Bill Long	PK3-1/A60	Julius Marcus	PK3-1/M29
John Meyer	ML12-1/A11	Al Michels	PK3-2/S14
Gerry Moore	PK3-2/A55	Ken Olsen	ML12-1/A50
Stan Olsen	PK3-1/A57	Stan Pearson	ML12-3/E13
JC Peterschmitt	GE	Larry Portner	ML12-3/A62
Bob Puffer	ML1-3/E38	Jack Shields	PK3-2/A58
Jack Smith	ML1-4/P14	Charlie Spector	ML5-2/M40
Bill Thompson	ML12-1	Gerry Witmore	ML5-2/M40

D I G I T A L INTEROFFICE MEMORANDUM -->FILE COPY

SUBJ: SEGMENTING THE MARKET

DATE: 13-Jan-76
FROM: GORDON BELL
EX: 2236
MS: ML12-1/A51

To: Janice Carnes, Tom Campbell F/U 1/19

Could I have the short version message that the salespersons and customers use to determine when to buy a 2040 vs 11/70(RSTS) vs 11/70(IAS) vs 11/70(RSX-11D-M)?

I would sure favor a rather simple multi-dimensional space approach where the buyer or seller could look things up in a table and see a clear picture of the choices. I can't believe the thing is much bigger than a single sheet of paper with the 4 systems across the top and about 20 or so dimensions going down the side.

Alternatively why can't we just use a standard Datapro and/or Auerbach listing for each machine?

The dimensions that seem relevant to me are:

1. Price/terminal and price range. Something that gives the curves for a single system.

2. Availability and delivery

3. Overall simple hardware measures: precision of floating point, memory and job array size limits, and speed that is relatively simple to characterize...e.g., the Gibson mix.

4. Any built-in data-types to give the buyer the feeling as to how much COBOL or a scientific language is emphasized.

5. Single operating system characteristics/features: scheduler (e.g., pie-slice); performance monitoring, accounting; file system...including back-up; device support

6. DBMS characteristics: speed, size, etc.

7. For each main language, a rough idea of what to expect...and whether it is provided at all. Program and array size limits. In the case of Fortran, whetstones/sec characterizes speed. The implementation of the language as a compiler, interpreter, together with any additional debugging tools should be noted. A note of special features (suserset) and subset is also needed.

8. Listing of exotic and/or non-standard languages.

9. A listing of the kinds of applications programs available

SUBJ: SEGMENTING THE MARKET

DATE: 13-Jan-76
FROM: GORDON BELL

internally and externally so the user will get some idea of scope and size of library. These would be listed by applications domain (e.g., EE-ECAP). This is probably the most important dimension. A simple listing of lines of programming (EE-100K, CAI-25K, etc.) would clearly give an idea of machine's use.

GB:lp

CC: Dick Clayton, Bill Demmer, Arny Goldfein, Bill Kiesewetter, Phil Laut, John Leng, Clay Neal, Larry Portner

I G I T A L INTEROFFICE MEMORANDUM TO -->JANICE CARNES

SUBJ: SEGMENTING THE MARKET

DATE: 13-Jan-76
FROM: GORDON BELL
EX: 2236
MS: ML12-1/A51

From
To: Janice Carnes, Tom Campbell F/U 1/19

Could I have the short version message that the salespersons and customers use to determine when to buy a 2040 vs 11/70(RSTS) vs 11/70(IAS) vs 11/70(RSX-11D-M)?

JAN 16 1976

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5. Single operating system characteristics/features: scheduler (e.g., time-slice); performance monitoring, accounting; file system...including back-up; device support

6. DBMS characteristics: speed, size, etc.

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8. Listing of exotic and/or non-standard languages.

9. A listing of the kinds of applications programs available

Tom & I are putting together a "Selling Against the HP3000" Guide that will contain exactly that information. We will send you a draft as soons one is finished.

Janice

Gordon

Digital Interoffice Memo

2 Copy + att.

Subject: How Big Is the cpu Family? ~~1 copy to Craig~~

To: OOD
Paul Bauer
Ed Corell
Howard Fineman
Ken Olsen
Steve Teicher

M/C
Janice Carnes
Bruce Delagi
John Levy
Grant Saviers
Mike Tomasic

Date: 5 JAN 77
From: Gordon Bell
Dept: OOD
Loc.: ML12-1 Ext.: 2236

This is a suggestion for a presentation to the board presenting our cpu, disk, printer, etc. families in terms of ranges.

Ken has been suggesting we either cut machines or explain why there are so many. Since I can't bear to part with members of the family, I was able to rationalize that we have the right number of machines...as compared with IBM. (And with what I think users need.) Ironically, I took IBM to task in 1970 for having too many models...(7 or 11). I proposed only three by using multiprocessors.

The 04/34 and 45/55 pairs are considered as 1 machine each. The LA36/180/120 is similar. This is a significant innovation in design technology and it may be the best way to approach designs in other areas (e.g., tapes, disks, some software). In this way we get 2 products with 1 effort and set of plans!

IBM's strategy on the 360 was to have a factor of:

-- X 2 gap in price to separate the models
X 3 gap in performance

$3/2$

This means perf = k X cost

See Bell/Newell p587 for analysis/data (attached)

Note
Models 20 - 91 Price (mins) 1:105
Price (avgs) 1:65
Price (min-min to max of max) 1:125?

20 - 91 Perf 1:300 (probably high)

Models 20, 25*, 30, 40, 44*, 50, 65, 75, 85*, 91, 95**

* later or ** special model

7 or 10 (or 11) models depending how you count

$125 = 1.99$ <--- original plan

$125 = 1.6^{10}$ <--- what got sold (neglecting #95)

$65 = 1.36^{?}$ = 300 <--- should be 2 for Grosch's law to hold

---

Note we do a better job now than IBM did on 360! Current 11's

	Range	Issues Range	Original 20
1.	03	10-20	11/20 - (20-50K)
	04	20-30	
	34	40-80	
	45	45-75	
	55	60-100	
	70	90-250	

$1.7^{6} = \frac{250}{10}$

or

$2.25^{4} = 25$

6 machines
or
4 machines if we count 04/34 and 45/55 as one. The PDQ will replace 45/55.

2. Factor of 2 in price is probably all a single machine can do.

Therefore $25^{3/2} = 125$ performance factor we should have. We get 70 for plain Fortran...but probably more when it's floppy vs. RP06.

3. Can't do all designs at one time! (This causes more models, less separation.) In essence there always has to be phasing blips.

4. Must treat 8, 10, 11 as **separate**, possible competitive, product lines - like Chevy, Olds, Cadillac. Each have a range and a set of customers that move across the range.

5. Engineering resources = f(range, volume, # systems).

6. Our planning is more complex because we may sell at 2 or 3 levels of integration (i.e., chips, boards, box, box + software).

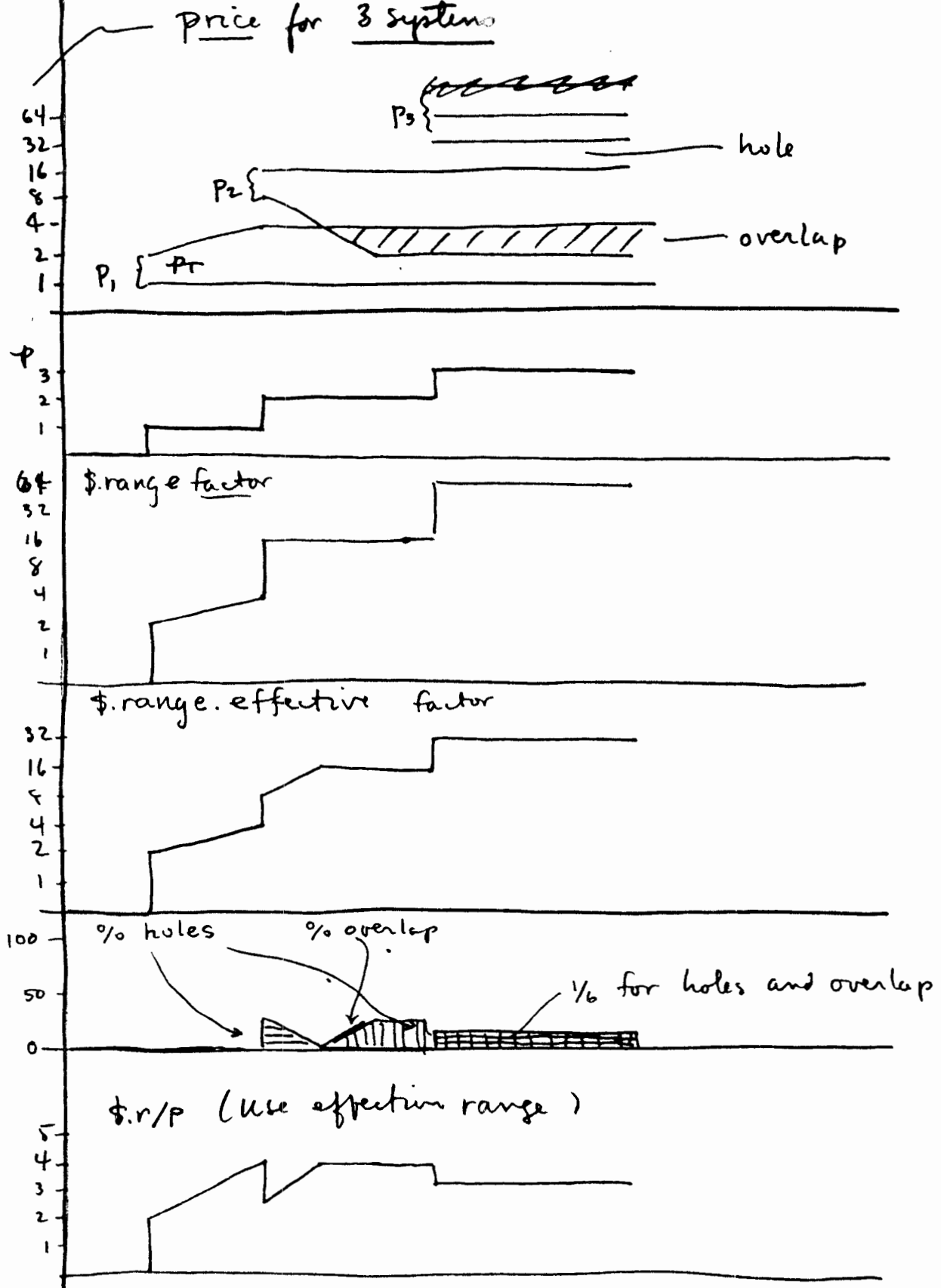
The attached metrics are ones I'd like to use for measuring range(t) for all products - disks, cpu's, printers, etc. We can measure each family and all the machines. Note, we can get >100% overlap.

$.range - from lowest price to highest price includes holes

p - # of processors or units in catalog

$.range.effective - subtracts holes (e.g., 11-10 gap) in range to get an effective coverage

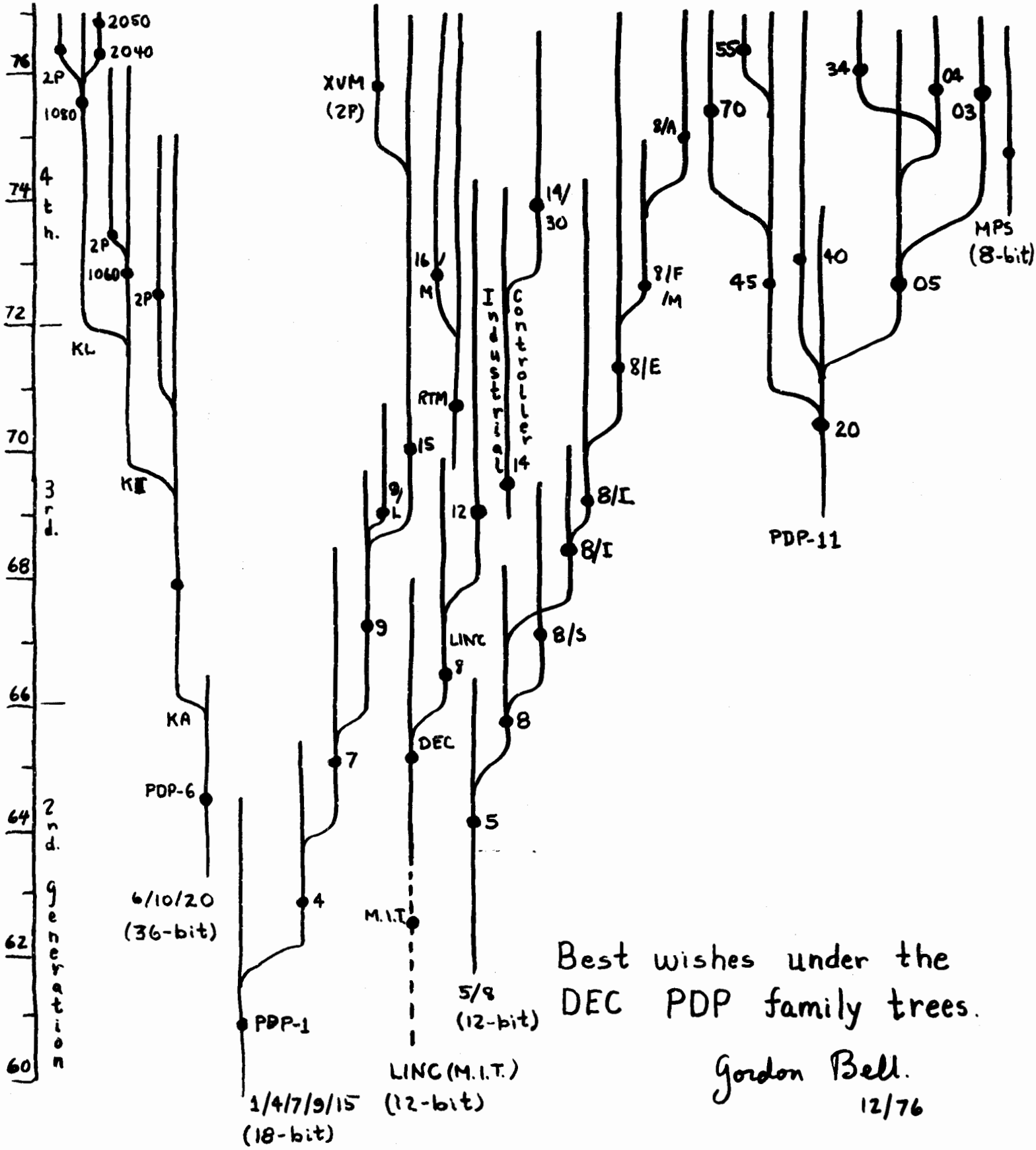
$.r/p = $.range 1/p



GB 1/2/77

digital
DIGITAL EQUIPMENT GMBH

DATUM:

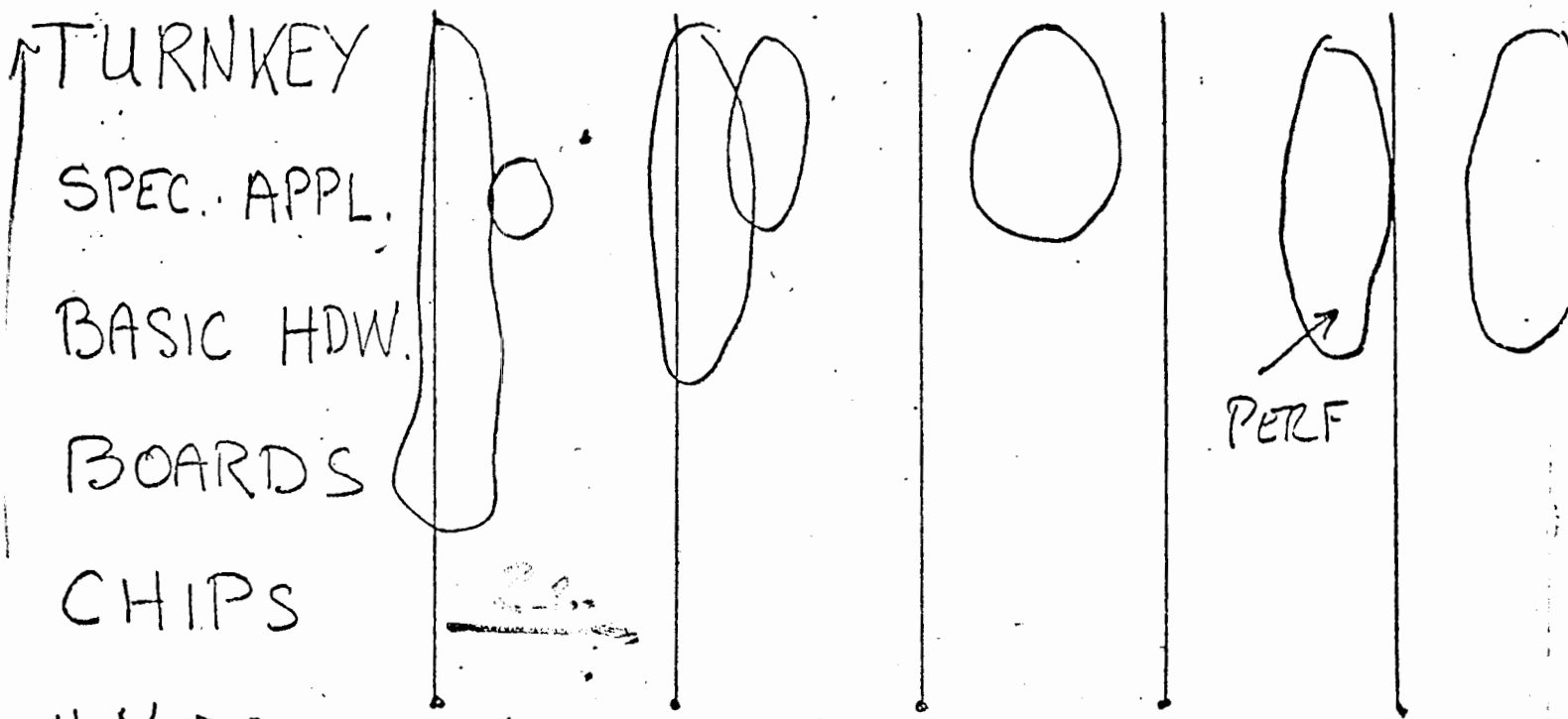


Best wishes under the DEC PDP family trees.

Gordon Bell.
12/76

Gen. Purp →

1



11 MODELS: 03 / 04 / 05 / 34 / 40 / 45 / 70

PRICE	.6-10	2-20	10-50	30-150	50-250
PERF. (Basic)	1	2	4	10	20
Perf. (Sci)	3	1	5	40	70
Perf ~ Price^2	1	4	25	225	625
Perf ~ Price$^{\frac{1}{2}}$	1	2	5	15	25

Mem. Size : (1) 4K - 28Kw ... -128Kw (32) (256) 1Mw

4.248
2.814

D I G I T A L INTEROFFICE MEMORANDUM

DIST:

Paul Bauer	ML1-3/E38	Janice Carnes	ML3-3/E71
Ed Corell	ML1-3/E62	Bruce Delagi	ML12-1/F41
Howard Fineman	ML5-5/E67	John Levy	ML3-4/E41
Ken Olsen	ML12-1/A50	Grant Saviers	ML1-3/E58
Steve Teicher	ML1-2/E65	Mike Tomasic	ML21-1/E81
Jim Bell	ML3-4/E41	Dick Clayton	ML3-3/E71
Ulf Fagerquist	MR1-2/E78	Arnie Goldfein	ML12-2/A16
Win Hindle	ML5-2/A53	Ted Johnson	PK3-2/A55
Andy Knowles	MR2-2/A52	Henry Lemaire	ML1-4/A97
Julius Marcus	PK3-1/M29	John Meyer	ML12-1/A11
Stan Olsen	PK3-1/A57	Stan Pearson	ML12-3/E13
Larry Portner	ML12-3/A62	Bob Puffer	ML1-3/E38
Bill Thompson	ML12-1		

Gordon

Digital Interoffice Memo

Subject Small-System Curve (Trends)

To: Distribution

Date: 9 SEP 76
From Gordon Bell
Dept: OOD
Loc ML12-12 Ext. 2236

The sketch (market size versus degree of participation for various priced systems) is attached which I drew at the Small Systems Woods If we built an analytical model of this, it might show that we look into an infinite market, and all we see is our ability to supply the market within our growth limits...this is what I'd hope a central planning group might someday do and/or understand. Note this sort of model might help understand why we are not getting smaller priced systems and why our installed base is only increasing linearly not exponential (as it had in the past!)

In the following figures, I postulate that the market matures by penetrating the levels of integration. That is, since we sell at a constant or increasing price (i.e constant salesman's yield in number of systems), we must offer more by increasing the product depth. In nearly all markets we watch it materialize in sophistication (while ignoring the lower level upstarts from below in the case of microprocessors, calculators, and programmable desk calculators)...and these products are the high volume products In general, the whole computer market (or an evolutionary subset) evolves:

1. Machine language (only the knowledgeable).

2. High level language.

3. Specialization to the language (eg. BEEF - Business Enriched Fortran.

4. COBOL/DIBOL.

5. Basic applications packages.

6. Production method for applications--eg. IBM's IAPs.

7. Turnkey applications (very high volume).

Also, a sketch (Fg. 2) is given which relates the maturity of a particular application market for various sizes. If a product is a constant price, then it's just learning (and new software = new product).

Finally, a sketch comparing two markets is given in Figure 3.

I believe we are doing an abysmal job in operating in the right points in the following three dimensional product space:

1. Market applications dimension = market maturity time.

2. System price for the market (too high or too low).

3. Level-of-integration or degree-of-participation (i.e. we're not deep enough in the right markets with right sized products).

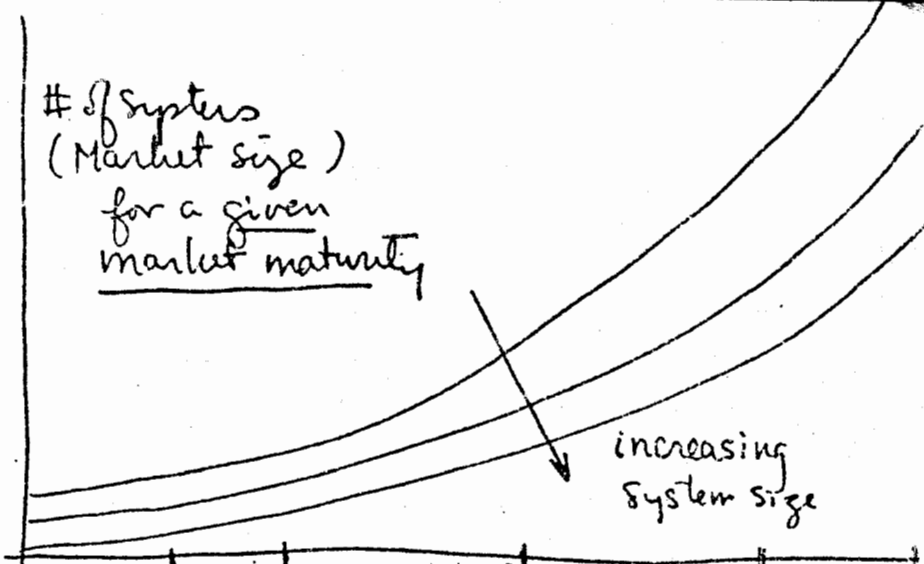
In lieu of any central market understanding, I assume you and I are responsible for reporting on where we are in this space, and how well we achieve it...together with the consequence of resource allocations. Figure 4 shows how we can begin to plot products in terms of markets level-of-integration, and system size...now all we need are numbers and a way to analyze and optimize it.

GB:ljp

Attachments

Fig. 1 Market Size vs Degree of Participation for various priced Systems.

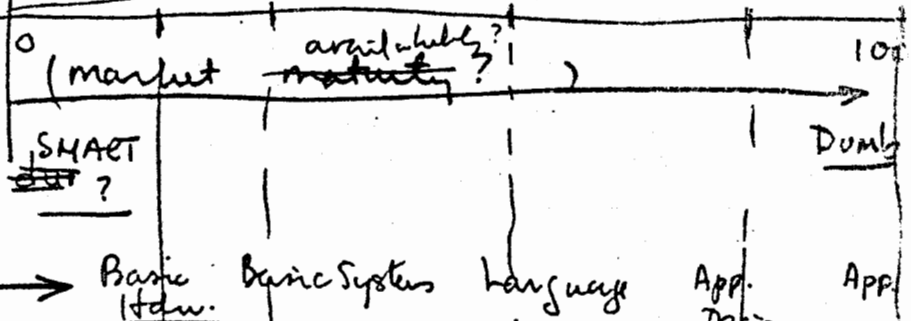
(Assumes constant maturity across an application)

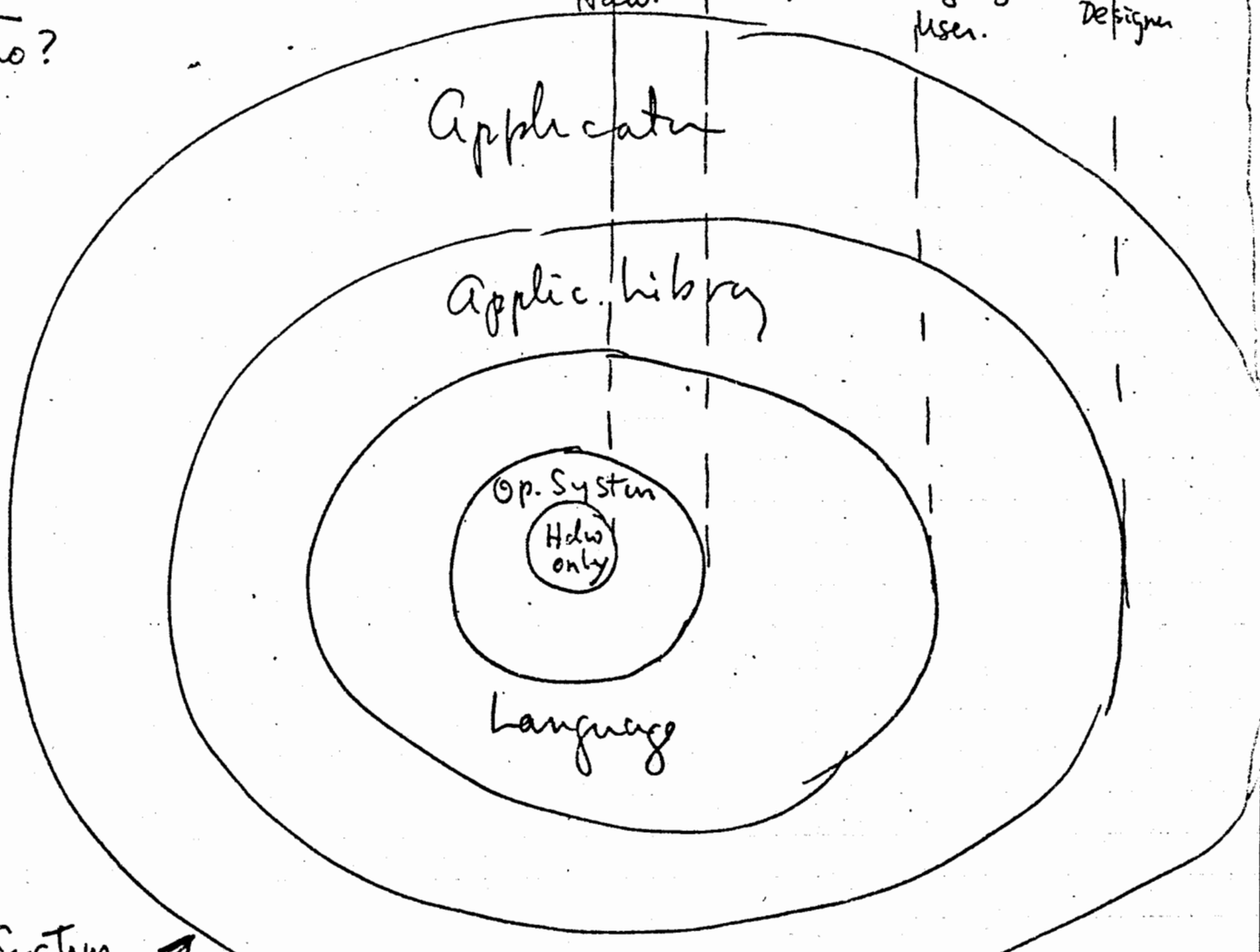


Degree of our participation to solve problem

Sophistication in Computing

User — Who?



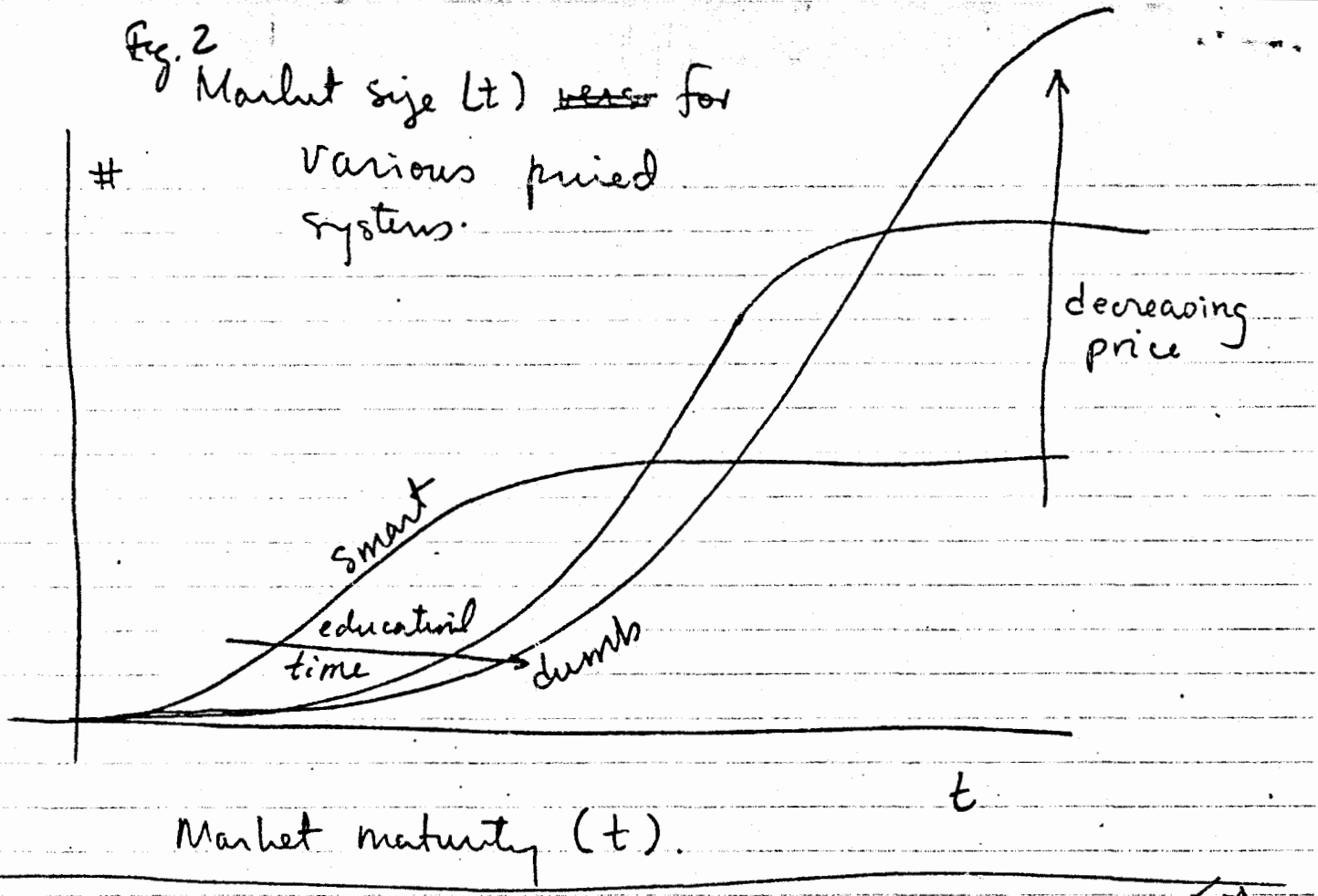


The System (Level-of-integration)

GB
6 Sept 76.

Fig. 2

Market size (t) ~~vers~~ for various priced systems.



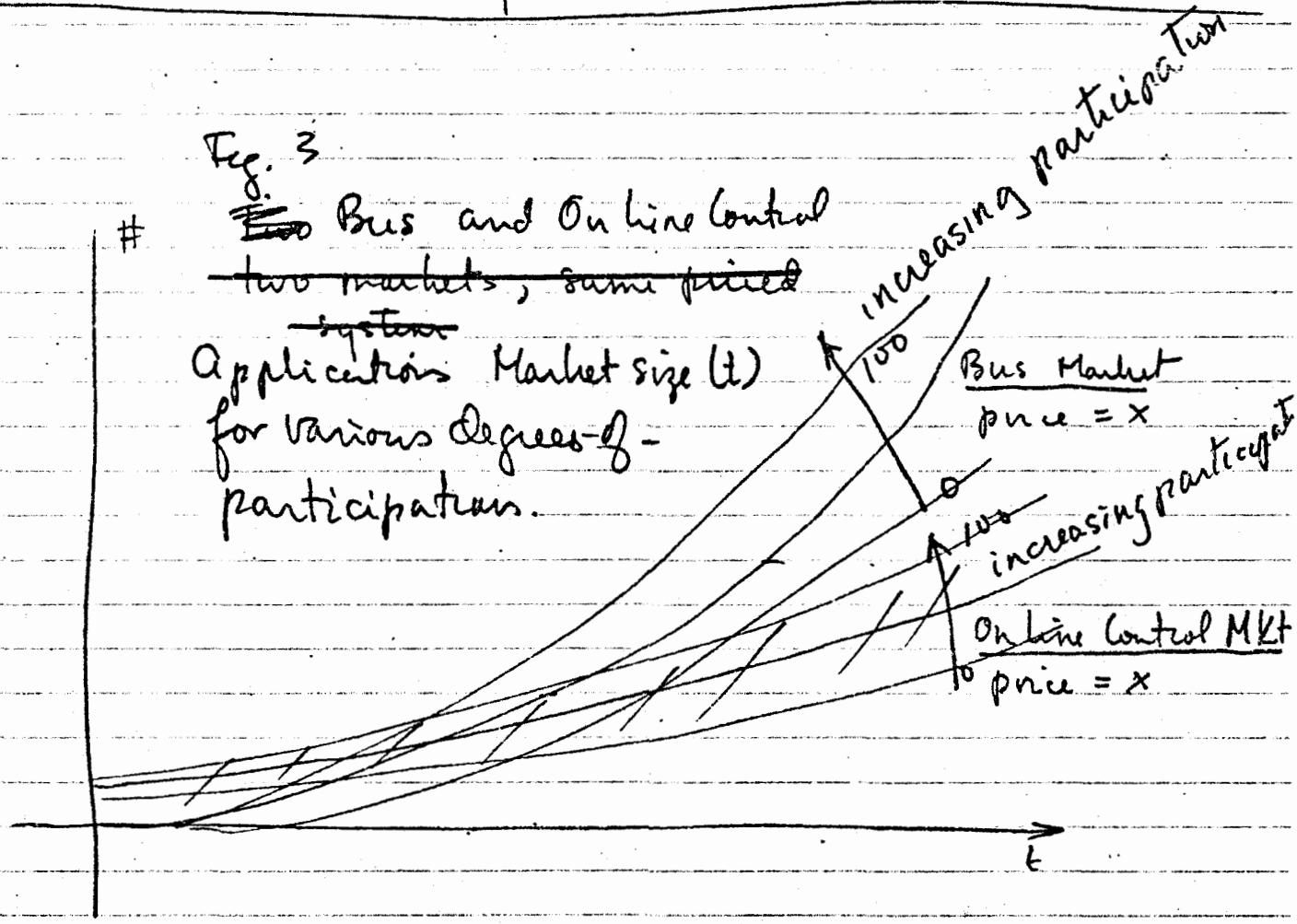
Market maturity (t).

Fig. 3

~~Exo~~ Bus and On line Control

~~two markets, same priced systems~~

Applications Market size (t) for various degrees-of-participation.



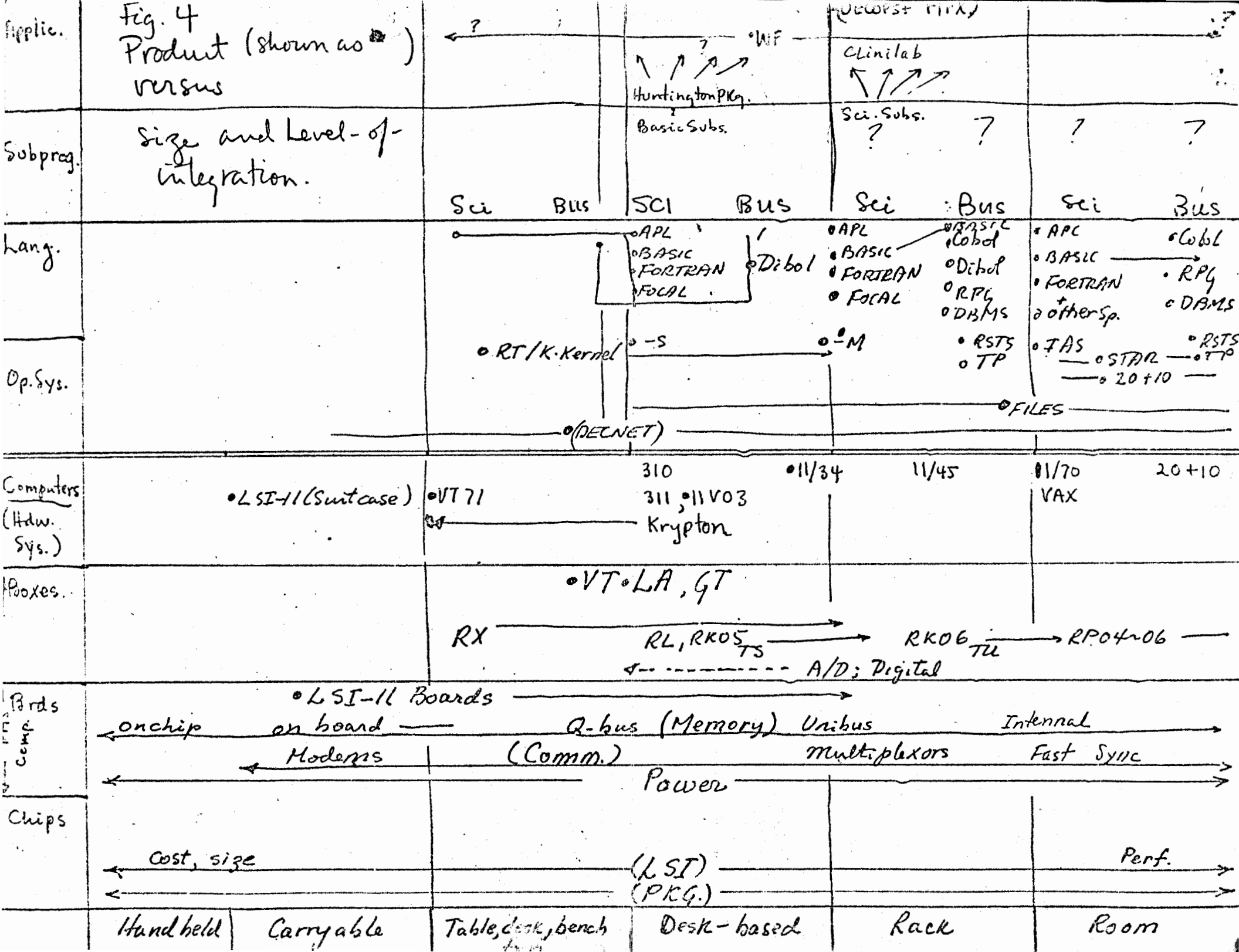


Fig. 4
Product (shown as •) versus
Size and Level-of-integration.
Applic.
Subprog.
Lang.
Op.Sys.
Computers (Hdw. Sys.)
Boxes
Brds
Chips
Sci
Bus
SCI
Bus
Sci
Bus
Sci
Bus
?
•WF
Huntington Pkg.
Basic Subs.
Clinilab
Sci. Subs.
? ? ? ?
•APL
•BASIC
•FORTRAN
•FOCAL
•Dibol
•Cobol
•RPG
•DBMS
•other Sp.
•RT/K-Kernel
-S
-M
•RSTS
•TP
•IAS
•STAR
•20+10
•RSTS
•TPO
•FILES
•(DECNET)
•LSI-11 (Suitcase)
•VT71
310
311, •11V03
Krypton
•11/34
11/45
11/70
VAX
20+10
•VT•LA, GT
RX
RL, RK05 TS
RK06 TU
RP04-06
A/D; Digital
•LSI-11 Boards
onchip
on board
Q-bus (Memory)
Unibus
Internal
Modems
(Comm.)
Multiplexors
Fast Sync
Power
Cost, size
(LSI)
(PKG.)
Perf.
Hand held
Carryable
Table, desk, bench
Desk-based
Rack
Room

D I G I T A L INTEROFFICE MEMORANDUM

****

****

DIST	Dick Clayton	ML5-2/E71	Win Hindle	ML5-2/A53
	Kal Hubler	WA	Irwin Jacobs	PK3-1/M33
	Ted Johnson	PK3-2/A55	Andy Knowles	MR2-2/A52
	Ken Olsen	ML12-1/A50	Stan Olsen	PK3-1/A57
	Ed Schein	MIT	Charlie Spector	ML5-2/M17
	Ron Spinek	ML12-1/F41	Bill Thompson	ML12-1/F41
	Jerry Todd	PK3-2/S14		
CC:	Ed Fauvre	ML21-4/E20	Bill Munson	ML12-2/E13
	Steve Teicher	ML1-2/E65	Ulf Fagerquist	MR1-2/E78
	Henry Lemaire	ML1-4/A97	Julius Marcus	PK3-1/M29
	Larry Portner	ML12-3/A62	Bob Puffer	ML1-3/E38

Digital Interoffice Memo

Subject: Calculator Prices (t) and Other Hand Held and Desk Top Things/P/M's

To: Distribution

Date 8 SEP 76
From: Gordon Bell
Dept OOD
Loc.: HL12-1 Ext.: 2236

Excuse my poor knowledge of history. Note the trends:

1. Various price ranges for various base type products and users.

2. Build constant functionality and reduce price fall out of semiconductor density increase.

3. Build improved functionality at constant price fall out of semiconductor density increase.

4 TI's strategy of better products at 1/2 HP's prices! Look out HP!

5. The scientific calculators have better libraries than computer companies. We have no competition with the business and statistics library.

6. By 1980 hand-held functionality will surpass many of our current products.

7. They will chew away at the need for computers to do calculations on small, data bases.

8. Some of the old calculator companies are still around (eg. SCM, Marchant, Olivetti, Monroe, Remington, Burroughs) although they are essentially dead just because they have old sales and service outlets, other products (which are vulnerable too), and a few non-competitive products which their old name can carry...until the distribution (sales and service) is shaken out. Their demise is clear, given a TI.

9. We can last longer if we die because we have EDP, big (useless?) data bases and programmer users (and the DECUS parties to go to) and a whole cult to keep us alive even though we're not needed.

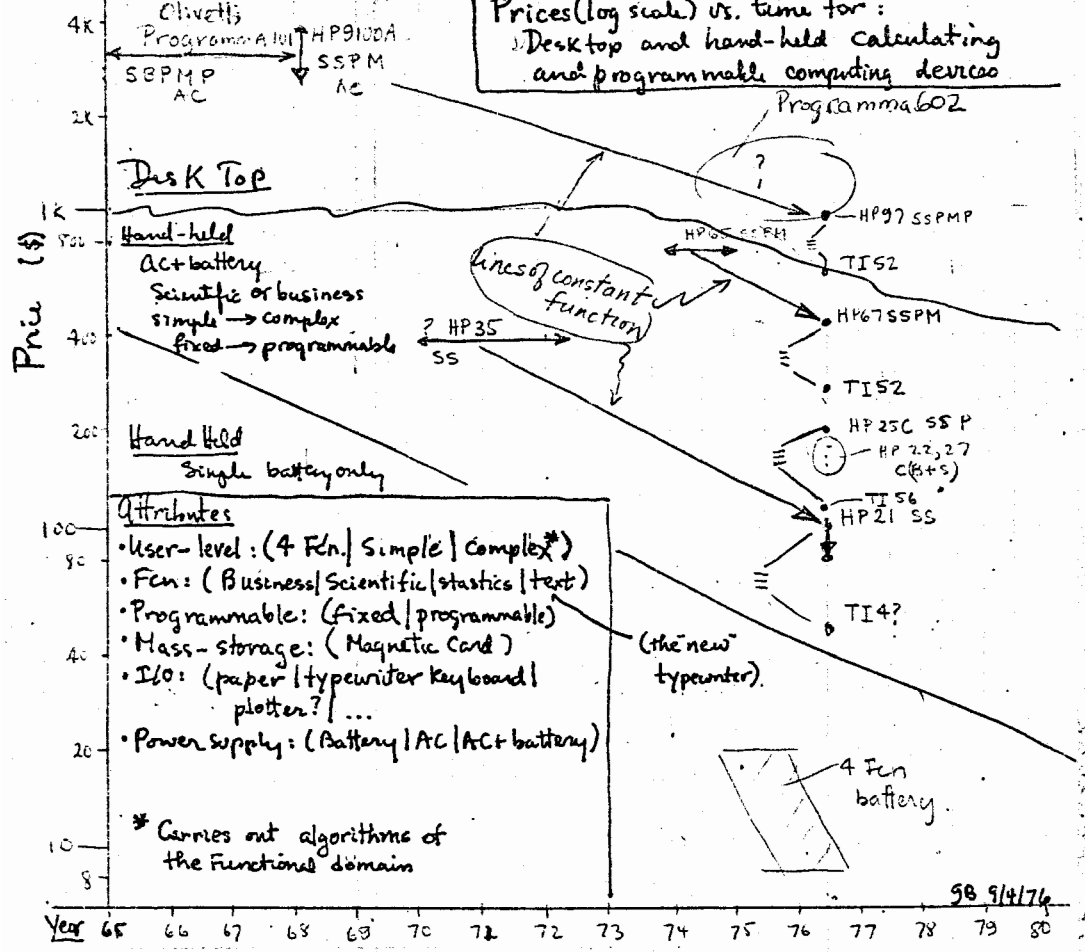
---

10. The low cost electronic typewriter with storage (circa 1978-) will chew up the projected, emerging high end word processing market since the volume is high for individual single user-based things...versus the Ferraris we handcraft. (Note IBM's the Cadillac.)

11 Calculator companies "progress" and introduce faster due to high programming content which uses increased ROM and RAM density

GB:ljp

Attachments (8)



ing instructions. Five flags can be set, cleared, or tested from the keyboard or within a program. You also get 10 user-defined keys.

Direct or indirect access to *all* data memories. Store numbers directly in *any* memory register. Or, store a number in a data memory specified by *any* other register (indirect addressing). Add, subtract, multiply, divide directly within all registers. Exchange display with memory.

Edit and debug. Move through a program a step at a time. Forward or backward. Insert. Delete. Or write over steps. List and trace your programs on the PC-100 printer.

Basic Library of 22 programs included. Put them to work right away: math, statistics, finance, electrical engineering, and others. You also get a 96-page Basic Library manual. Each prerecorded program card is supported with sample problems, user instructions and program listings.

Develop, write and record your own programs.

Programming is just logical thinking. You can do it. Using the programming manual with the handy coding form and user instruction tablet, you'll be writing programs in just a few hours. More than likely you won't be able to write optimum programs straight-off. Programs which run the fastest and use the fewest steps. However, you can begin writing programs that work. Press LRN to store each keystroke. Press it again and the SR-52 has learned your program. It's ready to RUN. Record your program on a blank magnetic card, and make it part of your personal library to use again and again. As your programming knowledge develops, you'll discover how this skill magnifies your professional capability. Better decisions will be as near as your SR-52.

Share programs with your colleagues through PPX-52.

There may be times when you need a complex specialty program. But you'd like the convenience of having a ready-made program that's not a bother to obtain. This is where TI's Professional Program Exchange (PPX) can be of enormous help. Here's how it works:

As a member you'll be able to turn to the section of your PPX-52 Catalog that serves your discipline. With hundreds of user-submitted programs available, there's a good chance the one you need is there. Order it, and put it to work on receipt.

What you get is a program developed, tested and submitted by one of your professional peers. Likewise, when you develop programs you may submit them for possible inclusion in the Exchange for others to use.

PPX-52 is for SR-52 owners who want to increase their professional contribution and efficiency. The annual membership fee of $15 entitles you to a Catalog, updates, and a subscription to the PPX-52 newsletter. Plus, your choice of three programs. Order more programs as you need them—$3.00 each.

Or, run prerecorded programs from TI's Libraries.

Optional libraries for the SR-52 go further and do more. Because of the 10 user-defined keys, 20 data memories and 224 program steps. So more steps and functions can be put on a card.

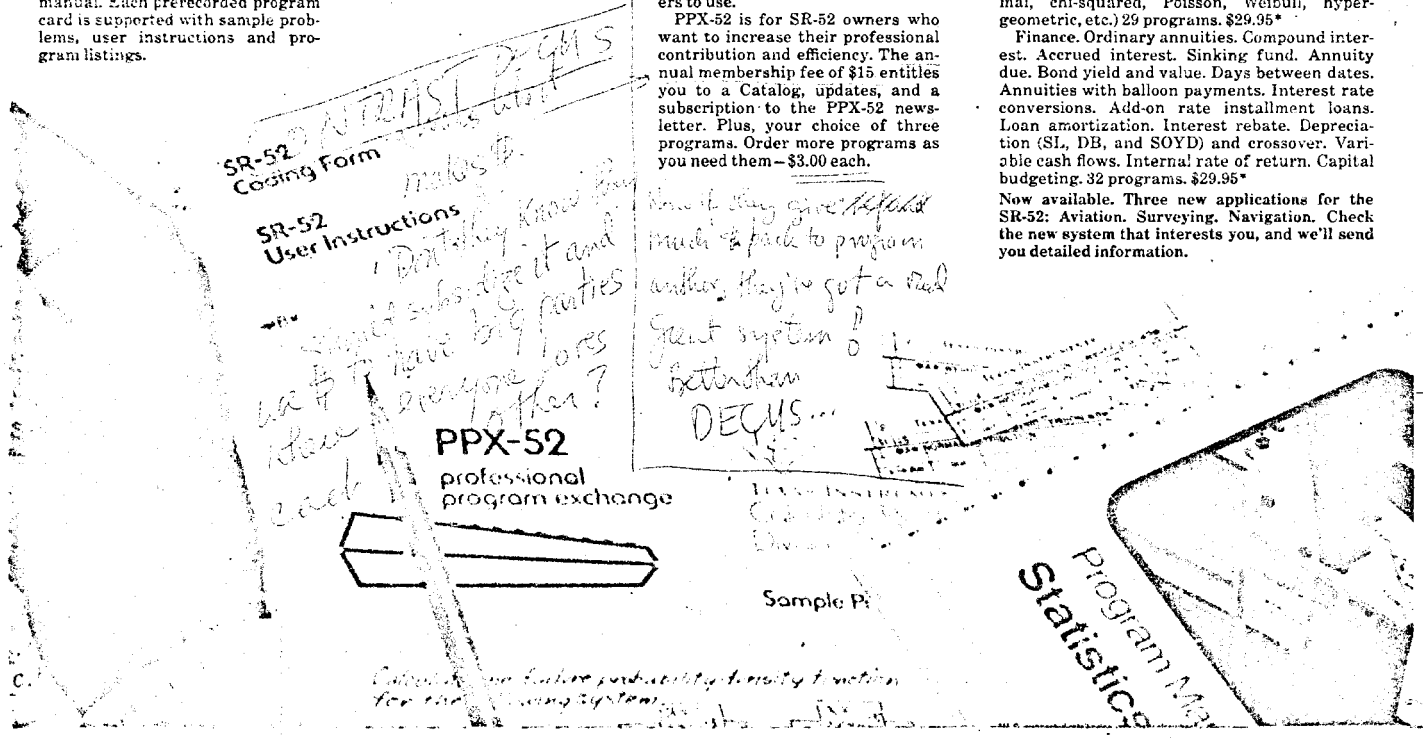
Math. Hyperbolic functions. Quadratic and cubic equations. Simultaneous equations. Interpolation. Numerical integration. Differential equations. Matrix operations. Base conversions. Triangle solutions. Complex functions. 34 program cards. $29.95*

Electrical Engineering. Active filters. Resonant circuits. T-π networks and transformations. Transmission lines. Phase-locked loops. Transistor amplifiers. Fourier series. Coils. Power transformers. Controlled rectifier and power supply circuits. 25 programs. $29.95*

Statistics. Means, moments, standard deviations. Random numbers. Permutations and combinations. t-statistics. Analysis of variance. Regression analysis (linear, power curve, exponential, logarithmic, quadratic). Multiple regression. Histograms. 12 distributions (normal, chi-squared, Poisson, Weibull, hypergeometric, etc.) 29 programs. $29.95*

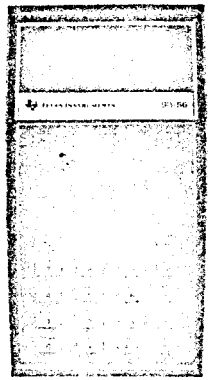
Finance. Ordinary annuities. Compound interest. Accrued interest. Sinking fund. Annuity due. Bond yield and value. Days between dates. Annuities with balloon payments. Interest rate conversions. Add-on rate installment loans. Loan amortization. Interest rebate. Depreciation (SL, DB, and SOYD) and crossover. Variable cash flows. Internal rate of return. Capital budgeting. 32 programs. $29.95*

Now available. Three new applications for the SR-52: Aviation. Surveying. Navigation. Check the new system that interests you, and we'll send you detailed information.



SR-56 new low price $109.95*

74-preprogrammed operations. Incredible calculating power, 10 memories and computer-like programmability in 100 steps.



A powerful slide rule calculator that also does double-duty as an economical, powerful key-programmable with: 100 programming steps. Eight-register stack (handles up to seven pending operations). Nine levels of parentheses. And 10 data memories.

Branches like a computer. Capable of direct addressing, which includes: Go to. Reset. Subroutine (4 levels). Plus six conditional branches.

Unique independent test register. Compare the value in the display with a value in the t-register—without interfering with calculations in progress. Or, use it as an extra memory.

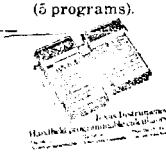
10 memories for your tough problems. Store and recall data. Add, subtract, multiply, or divide within a memory register without affecting the calculation in progress.

Unique pause key works two ways. Using this key in a program displays any step you designate for a ½-second. Hold the key down and you'll see the result of every step in the program for ½-second.

Easy editing. Single-step and back-step keys let you sequence through program memory to examine what you've done. If you pressed a key incorrectly, you can go back and write over it.

An applications library, too. A 192-page collection of programs. All pre-written. Select a program. Follow the listing (putting in your own data, of course). And you'll immediately begin using your SR-56's computing power to solve your own problems. • Math (10 programs) • Statistics (12 programs) • Finance (11 programs) • Electrical Engineering (11 programs) • Navigation (7 programs) • Miscellaneous and games (5 programs).

Circle reader service number 200



Get our new 16-page brochure that delves deeply into the features of the SR-52, SR-56 and PC-100. Also get a free prerecorded program and instructions so you can try an SR-52 at your TI retailer.

Texas Instruments Incorporated
P.O. Box 5012 M/S 598
Dallas, Texas 75222

Check one. Send me free:
- ☑ EE program card
- ☐ Statistics program card
- ☐ Finance program card

Send me more information:
- ☐ Navigation System
- ☐ Aviation System
- ☐ Surveying System
- ☑ PPX-52

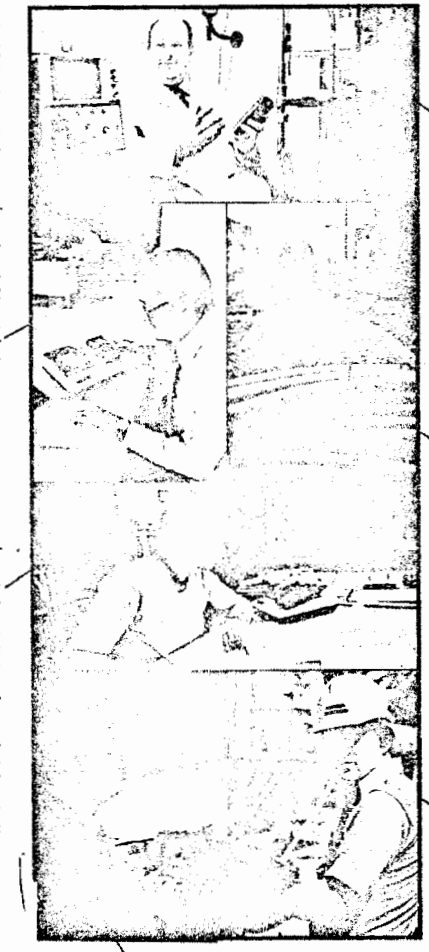
Name Gordon Bell
Title Prof Eng
Company DEC
Address
City Maynard State MA Zip 01754

4

When professionals need decisions, programmables deliver. Anywhere. Anytime.

"The SR-52 saves me time in designing attenuators—pi pads, T-pads, H-pads, etc. I key in the impedance and amount of loss and, in seconds, the SR-52 tells me what resistors to use. Without a calculator, it might take hours to optimize these values. The SR-52 is very easy to program—it works very naturally. It's cheaper, of course, than using a time shared system. It's also quicker and more convenient—not having to go to a terminal and access the big computer. And many things—formula translations, for example—are just easier to do on the SR-52."
M. H. Kindermann
Engineering Staff
Supervisor
AT&T Long Lines
Kansas City

"I'm using the SR-52 to handle long calculations in determining optimum locations in a warehousing system. I need lots of data storage — plus I can copy the magnetic cards and send them to our clients for use on their SR-52. We're also working on an energy model — a huge computer program with thousands of calculations. Here, I'm using the SR-52 for pre-processing and post-processing data to get it in a more usable form — to get my data out faster. The SR-52 is very powerful — and convenient. It's always available. I can take it anywhere."
Marleen Mandt
Operations Researcher
Stanford Research
Institute
Menlo Park



"We had a program we ran twice a week on time shared computer. It involved entering stock prices, option exercise prices—60 option prices. We had chronic difficulty getting a clean, accurate run because wrong quotations crept in. We'd lose time locating each error. I got the idea we could do it faster with an SR-52 and a PC-100 printer—screening each entry. I wrote the program myself. It worked beautifully. It's a big dollar savings. My secretary usually runs the program now."
Biddie W.
Worthington, Jr.
Securities Account
Executive
Wertheim & Co., Inc.
New York City

"Inserting a lens in the eye, usually at the time of a cataract extraction, has become an important surgical technique. The lens must be precise. This is where my SR-52 has proven invaluable. First the length of the eye is measured by ultrasound. Then I incorporate this and other data into formulas which I've developed and programmed on the SR-52. Of course, I share my programs with my colleagues. And, my approach is an integral part of my lectures."
Richard D.
Binkhorst, M.D.
Ophthalmic Surgeon
New York City

"Calculating a gas pipeline network for 200 homes under construction takes hours of tedious work. I developed a program for my SR-52. It makes all the necessary iterations—and gives me pressures and flow rates. Now I do in less than two hours the same work that used to take 10."
Carlos de León
Consulting Engineer
Diseño Ingenieria y
Tecnica en Gas, S.A.
Mexico City

"I wrote a program which I use in designing overhead bridge cranes. It calculates the moment and the maximum deflection on the beams that carry the trolley. I plug in the section's modulus and moment of inertia. Then the bending stresses and deflection are calculated for me. I wrote another program that I use in designing column footings. A programmable gives me the capability to analyze several setups very rapidly and come up with a good solution."
Joel Waldbieser
Civil Engineer
Waldbieser Engineering
Terra Haute

5

TI's unique Algebraic Operating System makes the calculator part of the solution. Not part of the problem.

With the introduction of the SR-50 slide rule calculator a few years ago, Texas Instruments had a choice: algebraic entry or Reverse Polish Notation (RPN). TI chose algebraic entry because it's the most natural and easiest to use. Now, with the new programmable calculators, TI takes another major step forward in power and ease of use—the unique Algebraic Operating System.

AOS is more than just algebraic entry. It's a full algebraic hierarchy coupled with multiple levels of parentheses. This means more pending operations, as well as easy left-to-right entry of expressions—both numbers *and* functions.

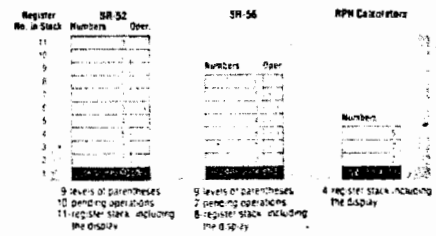
Pending operations let you compute complex equations directly. For example, a seemingly simple calculation like this:

$$1 + 3 \times \left[4 + \frac{5}{\left(7 - \frac{2}{9}\right)} \right] = ?$$

contains six pending operations as it's written. A TI calculator with full AOS easily handles it just as it's stated, left-to-right. You don't have to rearrange the equation, or remember what's in the stack as with RPN.

Here's how AOS stacks up.

AOS remembers both numbers and operations, so you key in your equation left-to-right. RPN only remembers numbers, so you have to remember operations and the order.



A calculator with full AOS remembers both the numbers and functions in its register stack. And performs them according to algebraic hierarchy. As more operations become pending, the stack fills up (see diagram). Finally, when the equals key is pressed, the operations in the register stack are performed to give you the correct answer (15.21311475). Automatically.

Compare the SR-52 & SR-56 with other programmables in their class.

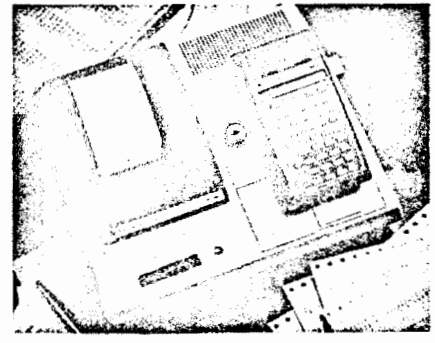
Operating characteristics	SR-56	SR-52
Logic System	AOS	AOS
Maximum number of pending operations	7	10
Parentheses levels	9	9
Memories	10	22
Store & recall	●	●
Clear memory	●	●
Sum/Subt to Memory	●	●
Mult/Div to Memory	●	●
Exchange display with memory	●	●
Additional special memories	1	38
Indirect memory addressing	—	●
Exchange x with t	●	—
Fixed decimal option	●	●
Calculating digits	12	12
Angular mode Deg/Rad	●	●
Grad angular mode	●	—
Digits displayed (mantissa + exponent)	10 + 2	10 + 2

Calculating characteristics	SR-56	SR-52
Log, ln, e^x	●	●
10^x, $\sqrt{x}$	●	●*
x^y, $\sqrt[x]{y}$	●	●
$1/x$, π	●	●
x^2	●	●
$\sqrt{y}$	●	●
$x!$	●*	●
Int X (integer part)	●	●*
Fractional part	●	●*
Trig functions & inverses	●	●
Hyperbolic functions & inverses	●*	●*
Deg/min/sec to decimal deg & inverse	●*	●
Deg to Rad conversion & inverse	●*	●
Polar to rectangular conversion & inverse	●	●
Mean, variance & standard deviation	●	●*

*Programmable functions

Programming capability	SR-56	SR-52
Editing steps	100	224
Multiple entry	●	●
Keystroke-level program capture	—	●
Decimal point programming (DPP)	—	●
User-defined keys	—	10
Possible steps	—	224
Absolute addressing	●	●
Subroutine levels	1	2
Program flags	—	5
Decrement & skip on zero (loop)	●	●
Conditional branching instructions	5	30
Unconditional branching	—	7
Indirect branching	—	●
Editing: Step, Back-step	●	●
Insert, delete	—	●
NOP	●	—
Single step execution	●	●
Pause	●	—

PC-100 printer. Turns an SR-52 or SR-56 into a quiet, high-speed printing calculator. $295*



Imagine the convenience of getting a hard copy printout of: Data. Intermediate results. Answers. Imagine the efficiency of listing an entire program at the push of a key. Or, printing the calculator's entire data memory contents with a simple program. And now imagine seeing every step of your program as it's executed—both the number and the function. Imagine no more. TI's exclusive PC-100 printer is here.

*U.S. suggested retail price, may vary elsewhere.

Be sure and send coupon to get your 16 page brochure and free preprogrammed magnetic card

Circle reader service number 200

TEXAS INSTRUMENTS
INCORPORATED

Printed in U.S.A.
03543

Hewlett-Packard announces two powerful breakthroughs in fully programmable portable calculators.

Two important breakthroughs distinguish Hewlett-Packard's newest personal-sized calculators.

Breakthrough Number One: Power.

The HP-67 and HP-97 are the most powerful personal calculators Hewlett-Packard ever built. Both can handle programs up to 224 steps. But there's a lot more to program capacity than just the number of steps available.

Example: All prefix functions and operations are merged—conserving steps—allowing you to store two or three keystrokes as a single program instruction.

Also, for the first time ever in a battery-powered calculator, you can directly record the contents of all 26 data storage registers on a separate magnetic card for easy reloading later. The result: Another substantial saving in program steps since constants and other numerical data don't have to be incorporated in your program.

And while we're still on the subject of power here are a few more of the programming features built into the remarkable HP-67 and HP-97:

- 3 Levels of Subroutines
- 10 User Definable Functions
- 10 Conditional/Decision Functions
- 4 Flags
- 3 Types of Addressing
  - Label Addressing
  - Relative Addressing
  - Indirect Addressing

But there's more to the HP-67 and HP-97 than raw power. There's ease of use.

Breakthrough Number Two: Ease of Use.

With the HP-67 and HP-97, a "smart" card reader *automatically* records the display mode, angular mode setting and flag status separately from your program so you never have to waste program steps for these "housekeeping" chores. What's more, it also prompts you—via a "Crd" display—when there's additional information on the card that must be loaded into the machine. Moreover, it's virtually impossible to improperly load programs or data from the cards.

In addition, the "smart" card reader enables you to automatically expand the capacity of either calculator beyond 224 steps. Here's how: At the appropriate point in your program—and under program control—the card reader can automatically turn on and read another card. This new card can be used to load either selected portions of program memory or selected data registers.

For ease of editing, the line number and all keycodes of every instruction are displayed. You can insert, delete or change functions at any point in your program. And, you can check or execute your programs step-by-step in order to locate programming errors.

Still another reason the HP-67 and HP-97 are so easy to use: RPN logic and four-register automatic-memory-stack. This means you can forget about parenthesis keys and tackle complicated programs with confidence.

Your Choice of Models. Pick the One That Suits You Best.

The HP-67 and HP-97 are identical in both versatility and capability. All programs written and recorded on the HP-67 can be loaded and run on the HP-97 (and vice-versa).

The HP-67 gives you shirt-pocket portability. The battery-powered HP-97 gives you attaché-case compactness plus a quiet, built-in thermal printer.

Programming, debugging and editing are so much faster and easier with a printer, you'll wonder how you ever got along without one. The printer provides hard copy not only of routine calculations but also of programs, listed by stepnumber, key mnemonic and keycode. Or you can TRACE a running program and have the stepnumber, function, and result printed for each step as it is executed. And you can also list the contents of the automatic memory stack or the contents of the data storage registers. With a clear record of your programs or data, you don't have to remember what you've done and what remains to be done.

More than three times the program capacity of the HP-65.

Hewlett-Packard analyzed 34 comparable Application Pac programs for both the new HP-67/97 and the industry's classic programmable, the HP-65†. These programs included a broad spectrum of disciplines: Electrical engineering, mathematics, statistics, and finance.

The results of this analysis indicate that the HP-67/97 offer over three times the program capacity (actually 3.4 times) and yet they have only twice as many program steps (224 vs 100). This is because the HP-67/97 are more efficient—in every case the HP-67/97 required fewer program steps to accomplish the same task (the overall ratio was 1:1.5).

As you can see, you can't judge a calculator's programming power solely by the number of program steps available—you must also evaluate program efficiency, that is, how many program steps it takes to solve a problem.

†Hewlett-Packard's HP-65 programmable calculator.

An Unparalleled Program of Product/Owner Support.

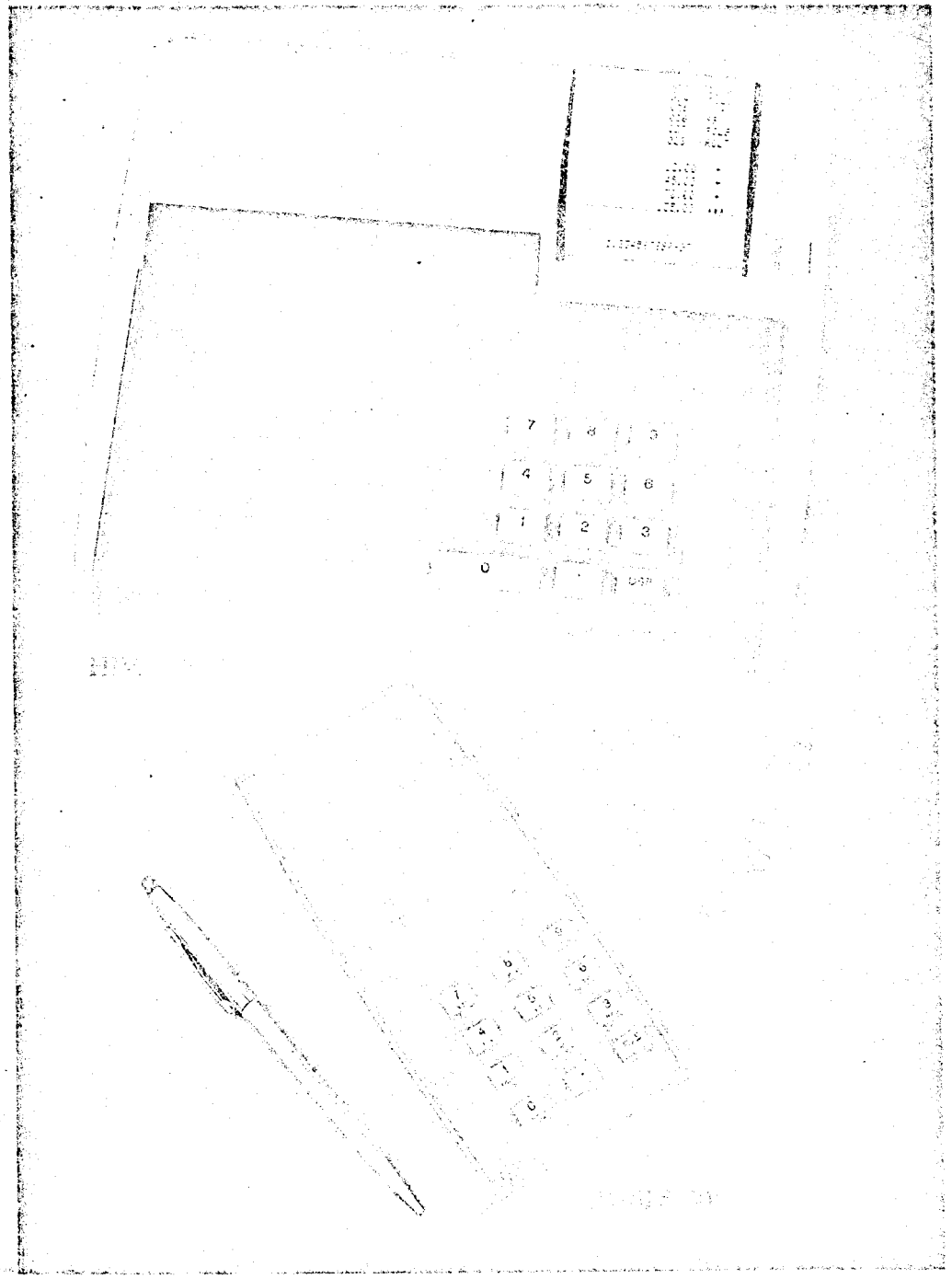
With either the $450* HP-67 or the $750* HP-97 you get all of the following: A detailed Owner's Handbook and Programming Guide, Standard Application Pac (with 15 programs of broad appeal), and a free one-year subscription to a Newsletter that provides programming assistance and keeps you informed about new Application Pacs.

Optional Application Pacs of up to 24 prerecorded programs are available in a variety of disciplines such as statistics, mathematics, finance, electrical engineering, surveying, mechanical engineering, and medicine. In addition, Hewlett-Packard maintains a User's Library** of programs contributed by owners.

If you would like additional information about the HP-67 or HP-97—including the name of a nearby dealer, simply call 800-538-7922 (in Calif. 800-662-9862) toll-free, or send in the coupon.

HEWLETT hp PACKARD

Sales and service from 172 offices in 65 countries.
Dept. 2144G, 19310 Pruneridge Avenue, Cupertino, CA 95014



Circle

Gordon
+ orig!

Digital Interoffice Memo

Subject: World Model of Computing Based on Amount of File Memory

To: Distribution

Date: 30 NOV 76
From: Gordon Bell
Dept: OOD
Loc.: ML12-1 Ext.: 2236

F/U 12/14

The attached graph is a guess, note no scales on distribution, as to how problems are structured based on memory data base sizes. Note, by coupling this with an earlier price model where cpu primary memory size determines the function (or amount of multiprogramming (and a memory hierarchiey model)), these two graphs could be used to impute the potential market size for all systems.

What's your estimate for shape of curves?

What are they centered about? Use? Technology?

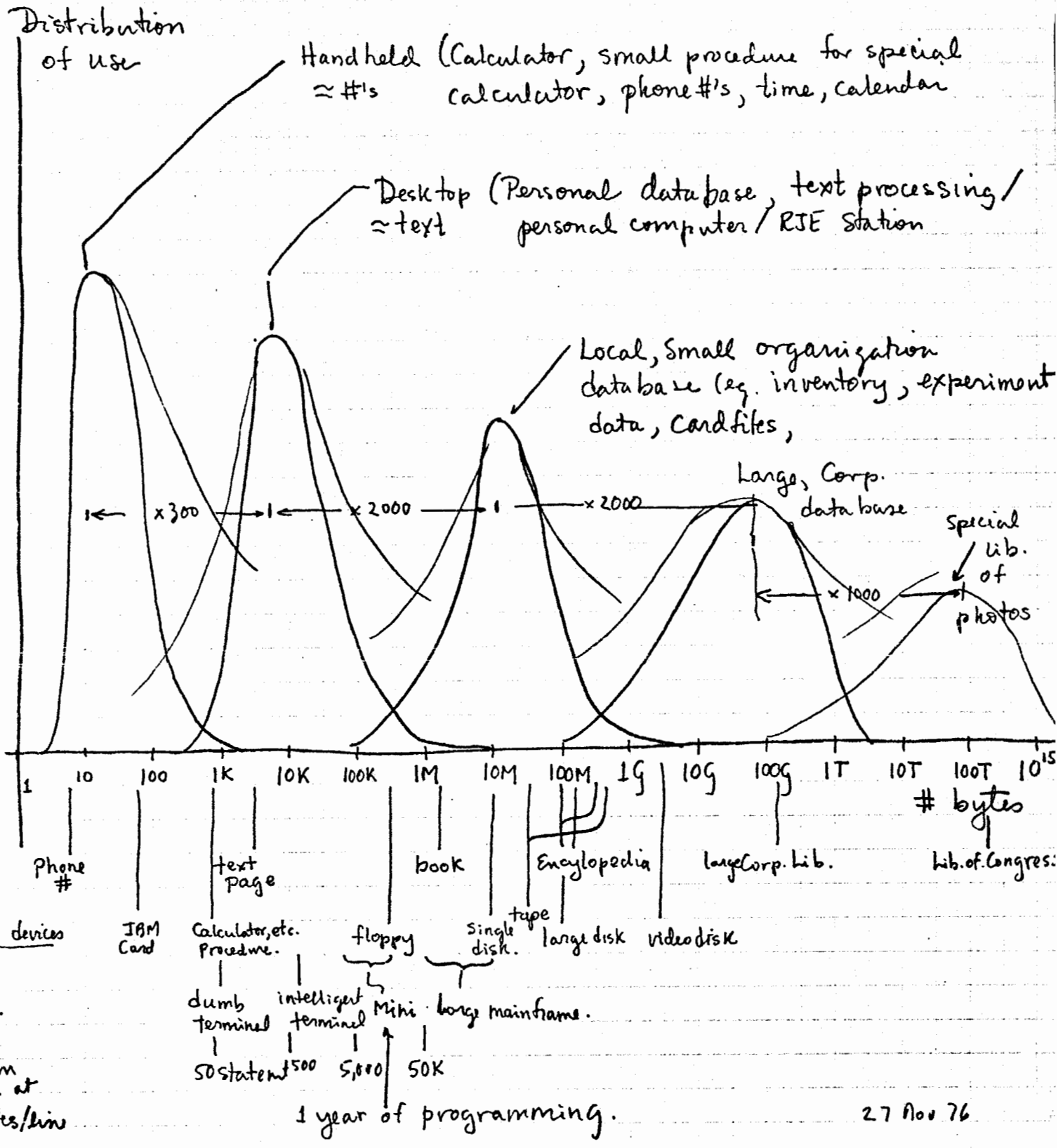
GB:ljp

Attachment

Distribution

OOD	Jim Bell
Brian Croxon	Mike Gutman
Stan Pearson	Bob Peyton
Grant Saviers	Bill Strecker
Steve Teicher	Mel Woolsey

Fig. — Distribution of use for various memory sizes.



27 Nov 76

digital

INTEROFFICE MEMORANDUM

TO: Gordon Bell

DATE: December 2, 1976
FROM: Steve Teicher
DEPT: Small Systems Product Development
EXT: 3175
LOC/MAIL STOP: ML1-2/E65

Gordon Bell

DEC 0 3 1976

SUBJ: DISTRIBUTION OF MEMORY SIZES

On first blush I would think that about 500K bytes of on-line storage would be a higher peak than the rest. My reasoning is that a lot of small businesses should be similar to the re-estate problem, which I guess would be served by a floppy for each town and the number of listings per town would be under 1000 at 500 bytes/listing.

This is really an interesting problem. A few years back several of us tried to figure out which operating systems would be used by which media. I think we concluded that DOS-11 wouldn't work on floppies because the code taken by the system programs exeeded two drives. Now we are sophisticated enough to begin thinking of applications as you suggest. I would begin by looking at the amount of on-line data plus sort space that we need to operate some small business units. We might look at the memory size needed to store the annual reports financial data for typical portfolios or several months of cost center reports. We may also want to try getting some people to keep logs about their data accesses for some sample interval.

/nj

Digital Interoffice Memo

Subject: Understanding the "Total DEC (and other)" Marketplace

To: Marketing Committee
Bruce Delagi
Jerry Todd

CC: OOD, Ken Olsen

Date: 30 NOV 76
From: Gordon Bell
Dept: OOD
Loc.: ML12-1 Ext.: 2236

F/U 12/14

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This section is on the distribution channel. Four figures (attached) might be of use to help specify the structure of the marketplace, and then begin to get measurements on the product flow. I feel we must ultimately understand this flow and the associated implicit model to use as an investment strategy.

The figures are:

1. Basic pieces of hardware taking on entirely different machine characteristics by various operating systems. One or more applications are added to match the ultimate single or multiple use in an organization.

2. & 3. At each level-of-integration and also for application installation/train and service (including applications) DEC, a 3rd party, or the ultimate user can be the supplier. Also multiple 3rd parties can participate. To really track, understand we must know something about the channel...i.e., what is ultimate use?

4. Shows data (hypothetical) for what the various groups do/supply. This particular data and the consequential understanding might be the basis of our market investment strategy. The particular plot should be done for: size
product lines

5. Shows market size (availability) with level-of-integration.

Overall, shouldn't we try to get a more proprietary position with a basic applications library such that we, franchise as OEMs or end users can get to the applications quicker?

GB:ljp

Attachments

GORDON, APPLICATIONS FROM CENTRAL FUNDS IMPLY A. CLEAR MARKET TARGETS
B. SOME AGREEMENT AMONG P.L.S SO THAT WE CAN SPEND CENTRAL FUNDS ON SPECIFIC APPLICATIONS (RIGHT NOW WE ARE ONLY SPENDING FOR APPLICATIONS TOOLS) &P.

D I G I T A L INTEROFFICE MEMORANDUM

DIST:				
	Bruce Delagi	ML12-1/F41	Ken Olsen	ML12-1/A50
	Jerry Todd	PK3-2/S14		
	Dick Clayton	ML5-2/E71	Ulf Fagerquist	MR1-2/E78
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	Bill Thompson	ML12-1		

Gordon Bell

DEC 02 1976

Digital Interoffice Memo

NOV 30 1976

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To: Marketing Committee
Bruce Delagi
Jerry Todd

CC: OOD, Ken Olsen

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DEC 1 - 1976

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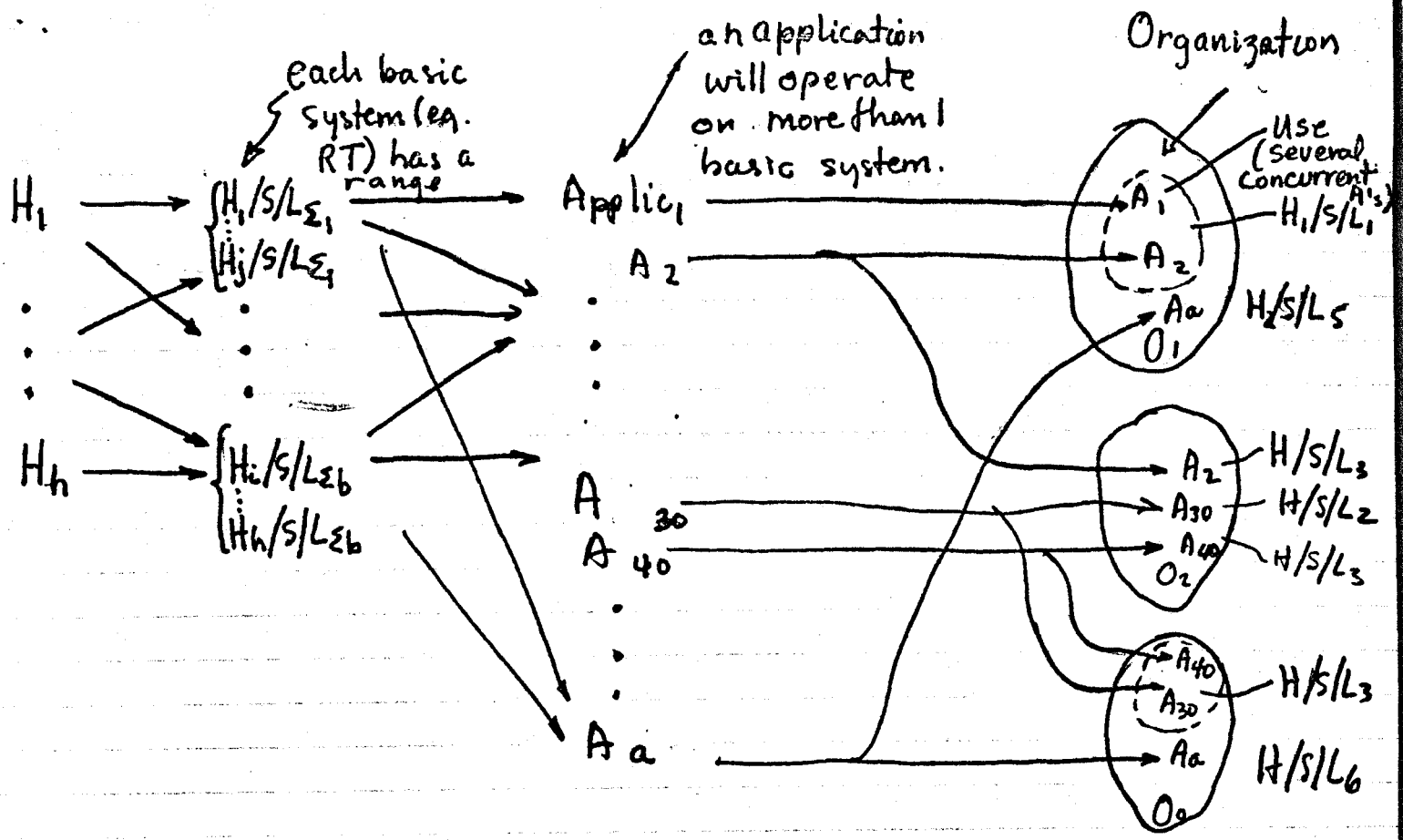


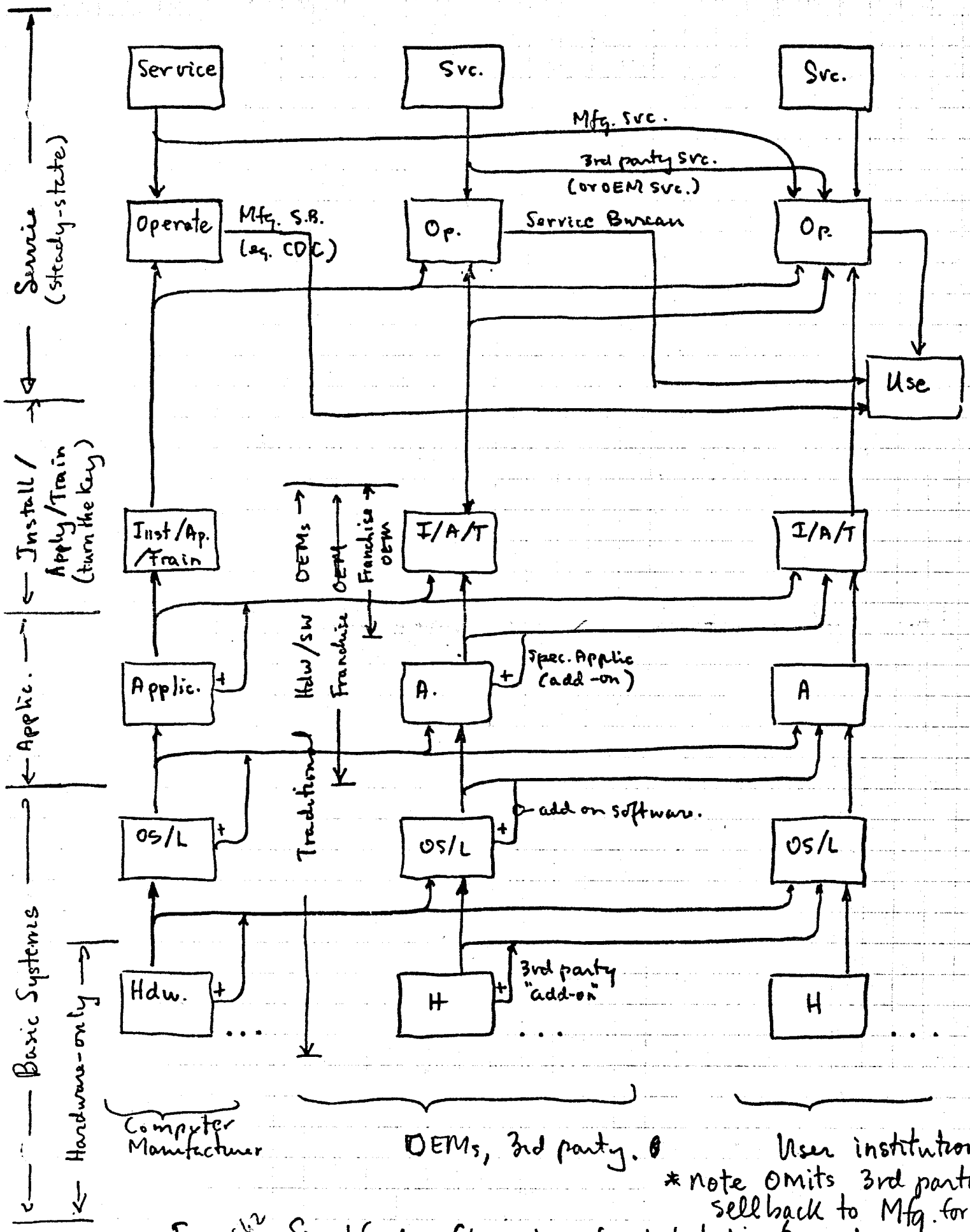
Number of distinct systems

$$\leq h \times b \times \left(\frac{h}{a}\right).$$

where

h = no. of unique hardware system models
b = no. of basic operating system × {language} systems.
a = no. of application programs
n = no. of concurrent applications which operate on a given system.

Fig. Not The network (simplified) of basic hardware / operating system / language / applications systems flowing to various organizations for use.



* note OMits 3rd party sellback to Mfg. for resale

Fig. 6.2 ~~Simplified~~ Channels of distribution & and service for computer systems (simplified)

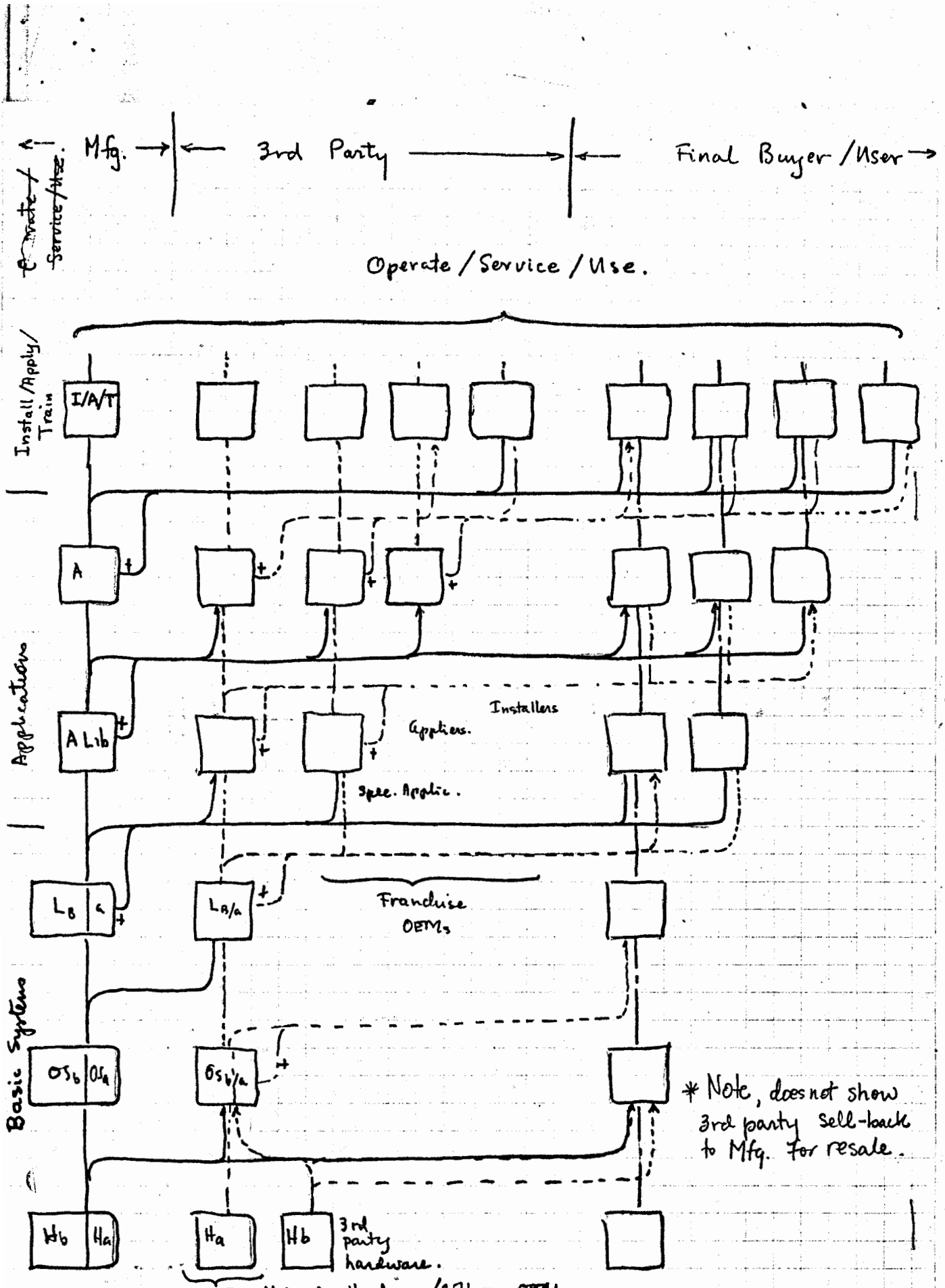


Fig 1 Channels of distribution for complete system

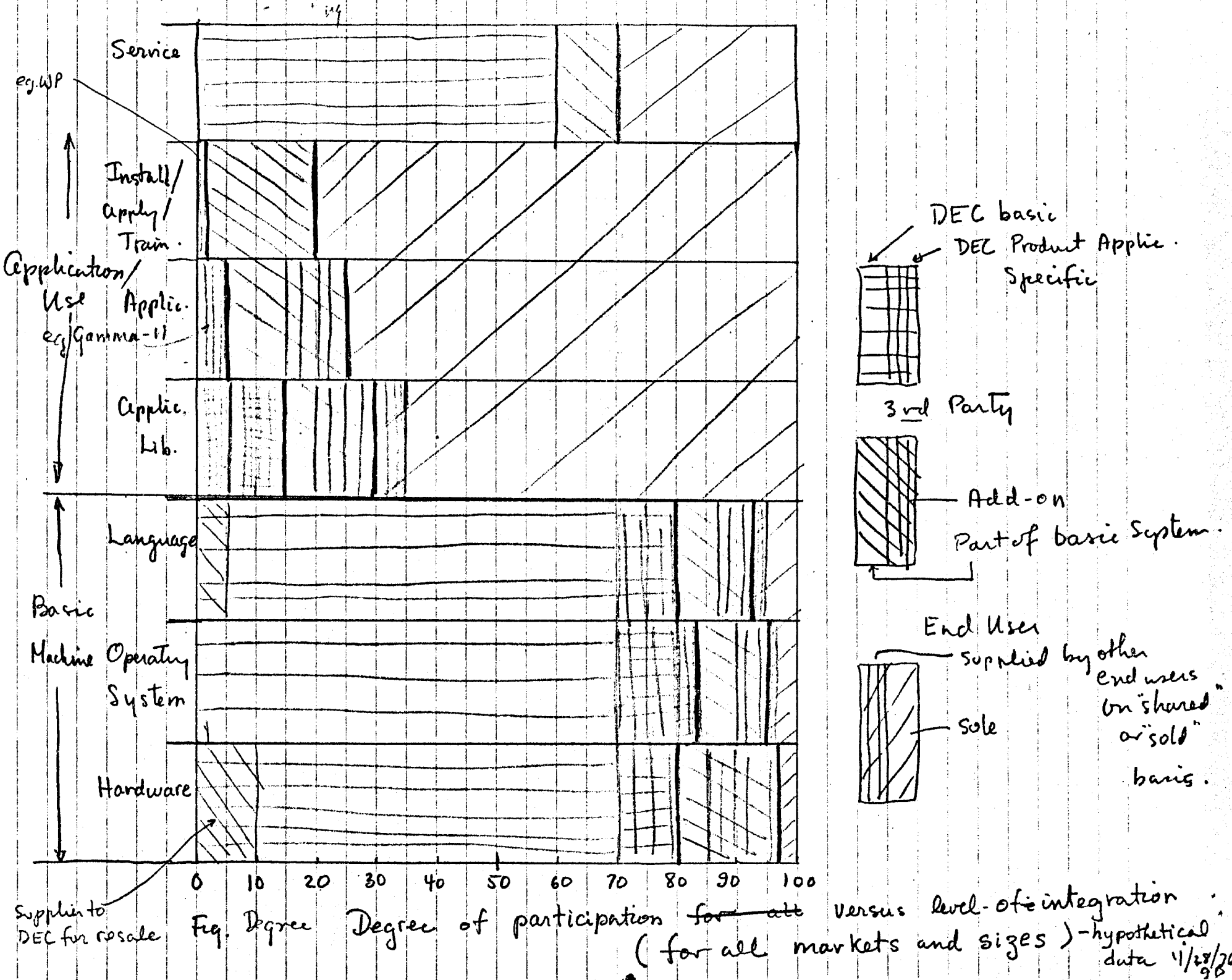


Fig. Degree Degree of participation ~~for all~~ versus level-of-integration (for all markets and sizes) - hypothetical data 1/28/76

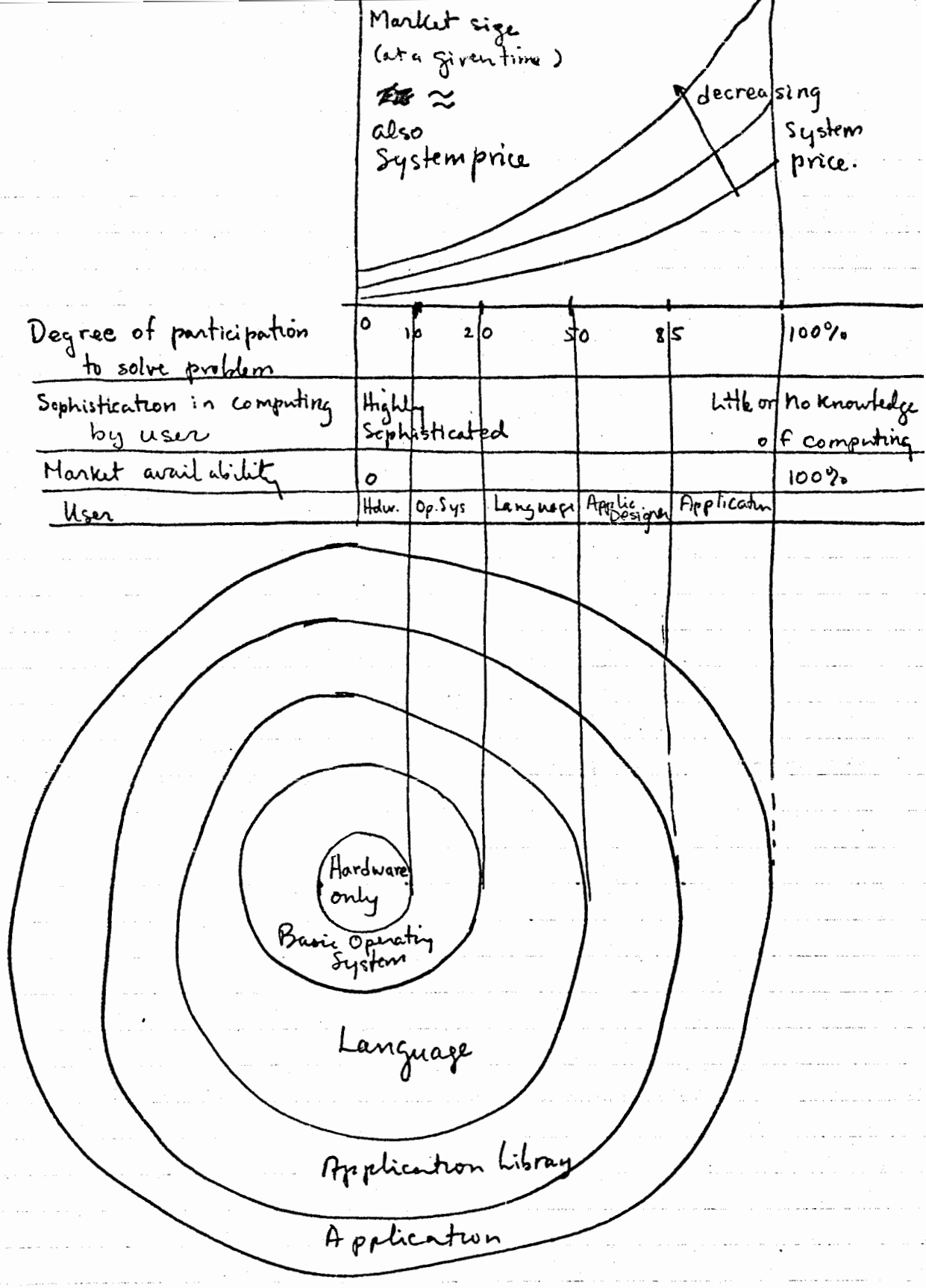


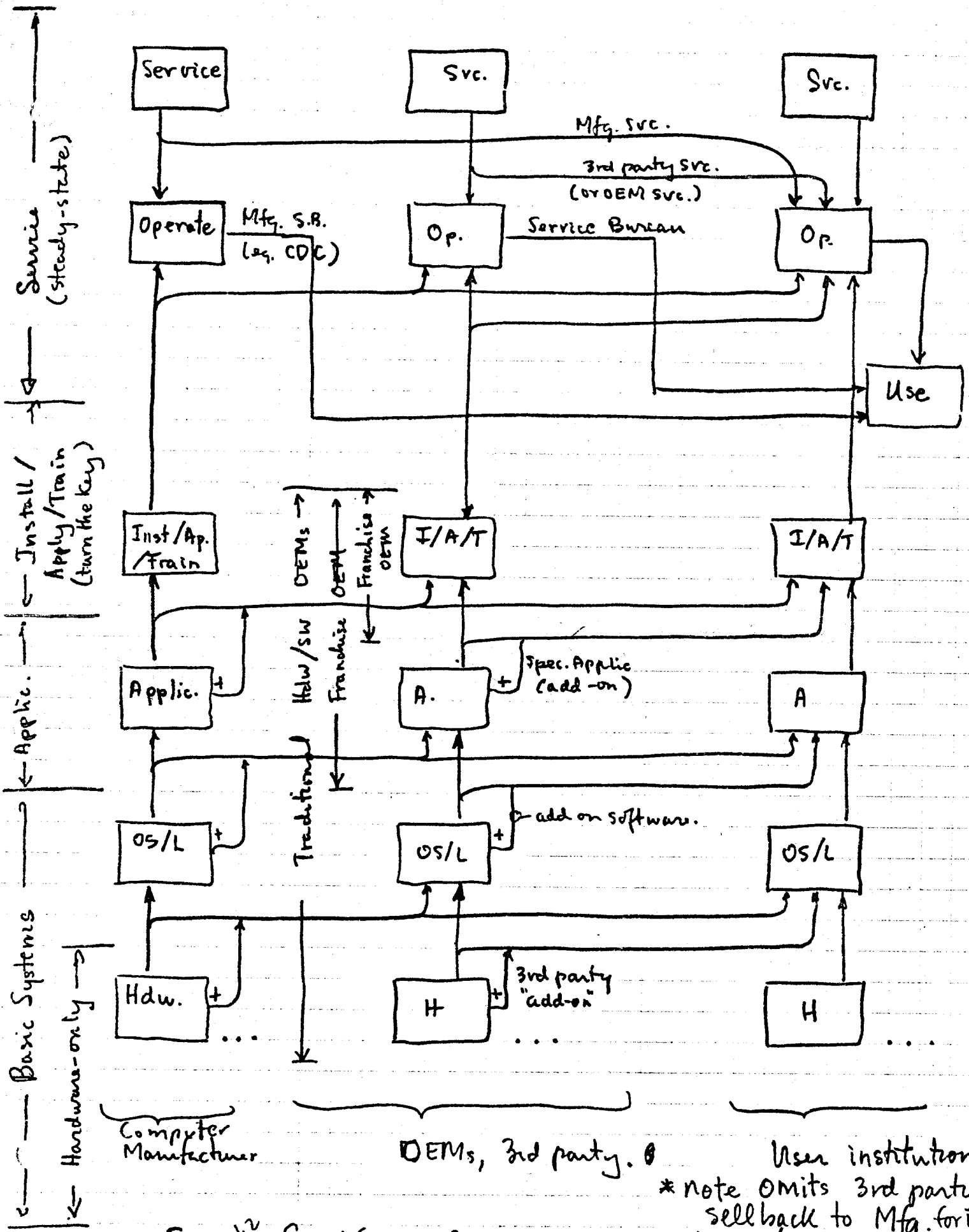
Fig. M1 Market size versus degree of participation (≈ level-of-integration) to solve problem.

Sndr –

(some) levels of integration

- we train unsophisticated users in use of our soln to their problem
- we solve "problem"
- we provide complete environment in which problem is solved — (our customer states problem in terms of application)
- we provide ~~operating system~~ computer system environment in which problem is solved (Customer states ~~desired~~ problem in & our terms [redacted])
- we configure hardware system that probably is useful in solving problem
- we provide a parts catalog of things that fit together most of the time – namely to our standards
- we provide parts to externally defined standards

Bruce



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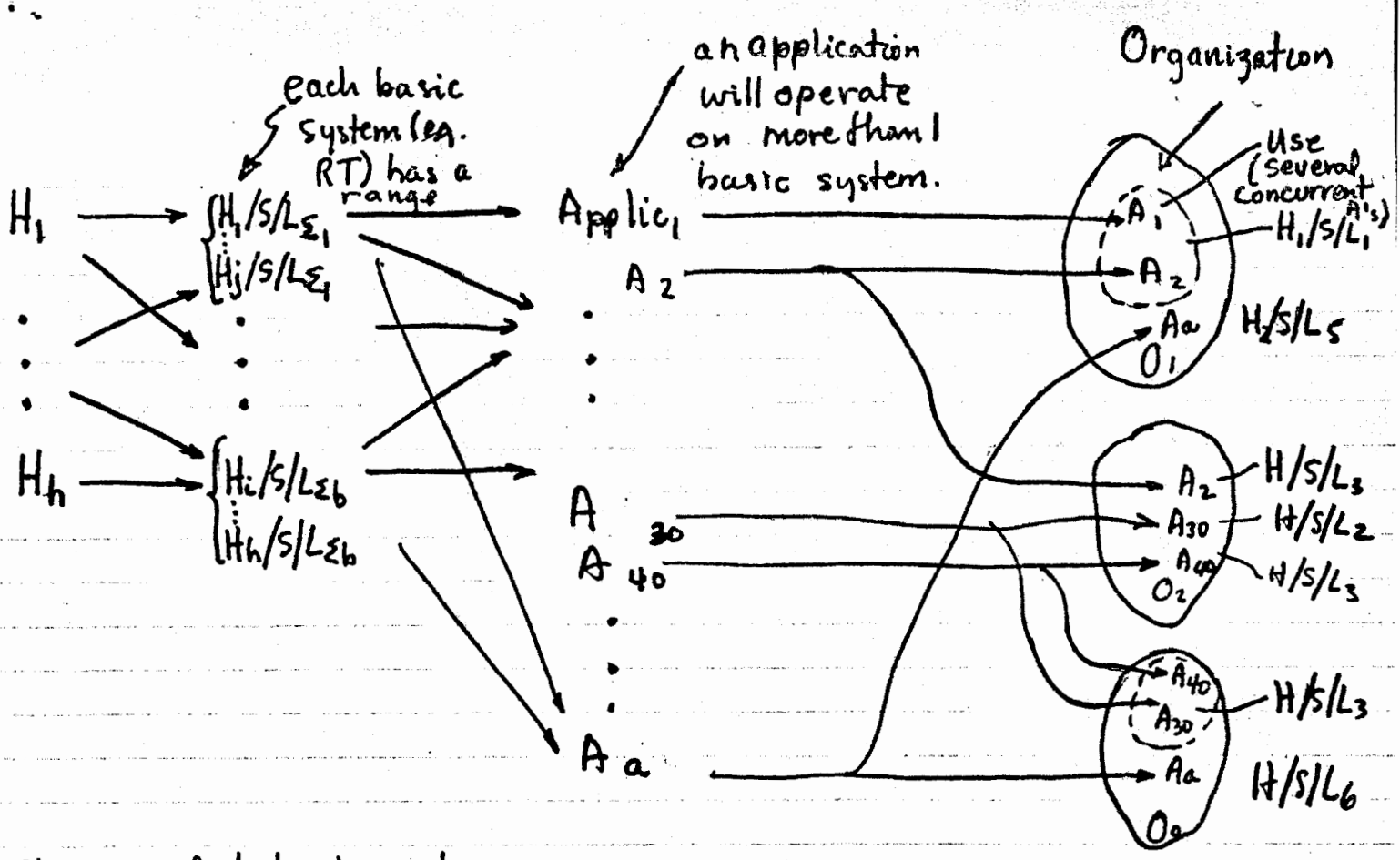

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If I have lots of application programs & only 1 application running concurrently, I have

where

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NOV 29 1976

Digital Interoffice Memo

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To: Marketing Committee
Bruce Delagi
Jerry Todd

CC: OOD, Ken Olsen

Date: 30 NOV 76
From: Gordon Bell
Dept: OOD
Loc.: ML12-1 Ext.: 2236

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GB:ljp

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+---------------+
! d i g i t a l !
+---------------+

INTEROFFICE MEMO

SUBJ: SHOULD WE PUSH THE 11 AGAINST THE 8086 AS THE 1980s STANDARD COMPUTER?

Date: 1/31/78
From: Gordon Bell
TO: Distribution
Dept: OOD
MS: ML12-1 Ext: 2236

We must focus now to understand the alternatives surrounding how deeply we push the 11 as the standard, 1 chip computer for the 80's using FONZ and/or T-11. It is the single most important corporate decision we have to make in the next six months. In one year a decision will most likely be too late.

It seems there are only a few alternatives, none of which are pleasant:

1. We do nothing--this is the most likely because we have to make a decision against our easy course. Following this is essentially alternative 3. I don't want us to defacto give up like this without thinking through the scenarios.

2. We make the 11 ISP (increasingly broader subsets) available for the industry standard computer architecture of the 80's just as it <u>has been</u> for the 70's as a mini. <u>(This gives buyers an incentive to move up to the larger DEC machines -- which we now market.)</u>

   A. We try to supply the world with chips (with/without second sourcing).

   B. We get the semiconductor vendors to (help) design and supply the world with 11 chips. Maybe we never need design another 11 LSI processor.

3. We give up the 11 as a standard, if it becomes too expensive for us to maintain as a vanity ISP (about 1980) then we'll buy the standard computer--the 8086 and re-implement our software (making small changes).

4. We introduce a new DEC architecture for thelow end. This confuses the marketplace (and probably us as well) and <u>may</u> defer establishment of the standard. This is analogous to the IBM Series 1 decision.

<u>Semiconductor Standards</u>

The semiconductor industry and its user community always rallies around standards with second sources. Only a few of the possible technology alternatives are ever chosen, e.g.: technology (TTL and MOS but not DTL, ECL, SOS, IIL). If we observe the 8-bit market it is 60% 8080, 30% 6800 and 5% Fairchild (but for more specialized markets). This means all vendors supply 8080's, there are programming tools supplied by many and others build programming languages, and applications for them. The 8080 customer base dwarfs ours with over one million machines. The 8080 took two years to attain standardization based on its predecessor which also took two years.

Intel has a good standard architecture in the 8086 that rivals the 11 and in its present form can be sold around the 11 because it has adequate address space.

Within a year or so after the recent 8086 announcement and ships there will be adequate enhancements to compete totally across the board with 11's. Their customers and designers will force it. These enhancements will be: better memory protection for multiprogramming, floating point for the scientific and control markets, and better instructions for commercial data processing (although the 8086 isn't too bad now). This inevitability is based on the way all computers have evolved for every generation from von Neumann to the PDP-1, and includes the 8, 10, and 11 plus all of IBM's computers!

Implications of a good standard

The threat of the market is not Intel, but the standard and the surrounding marketplace it creates to compete with us for OEMs, our systems houses and end user applications area. No matter what manufacturing capacity we have, we can't supply all this market; and the chips and standards will be the rallying point.

Users who want to integrate backwards will do it with the standard (lowest cost). This market has shown that it doesn't understand software investment, hence will mainly be driven by manufacturing cost. Wang, Sycor, NCR, Olivetti, and Univac are typical users (and in some cases our customers), but our former customers (e.g., Tektronix, GR) may ultimately desert us because they want the lower cost of forward integration.

Any attempt to hold back the standard by supplying any large part of the computer market with some board level or box level product is probably naive. Computers are and will go underground and be more specialized in packages we don't understand. Any attempt to dominate with a high complexity item (as opposed to a dumb terminal) in such a high volume market will be like building a dam with our finger.

Us

The value added in central processors will continue to decrease in all sized systems as the mix continues to evolve toward storage, terminals, and software capabilities (including those implied by "distributed processing"). Our OEM's primarily interested in cost reduction of (their) existing function will wane in their interest in us and go to the industry standard instruction set as the software becomes available. When they upgrade capability from this base, they will do so on the industry standard with which they have experience. The base we will hold will be those primarily interested in increasing capabilities of their current offering. We will hold these customers to the extent we demonstrate dominant capabilities in storage systems and distributed processing. The competitive marketplace will set costs, and the cummulative effort on the industry standard architecture will set the software and its quality.

Giving up the 11

Since we spend roughly 1/4 of our engineering budget to maintain the 11 as a

vanity standard (something we have but the world can't have), we may have to give it up to move more to a market focus. We may pay too much premium of having to develop all the chips, write all the software and do all the applications. And we don't (nor does any company!) have a big enough base to compete with all the companies the 8086 will spawn generating hardware and software!

Selling the 11 as Chips

It's hard to predict what the scenario would be if we sell or license the 11 as the standard. For one thing, competition by hardware suppliers at the basic tools level we currently sell at would increase. All the logic hackers could make systems and compete with our FA&T and the end user PLs that sell low level tools. We would survive to the extent we sold the most cost-effective storage and network capabilities or the most highly valued services. On the other hand, competitors will take the lower cost standard...the 8086 and drive the market in that direction anyway. If we didn't follow, we'd be increasingly irrelevant.

For end user P/Ls selling applications who control the software there would be no change.

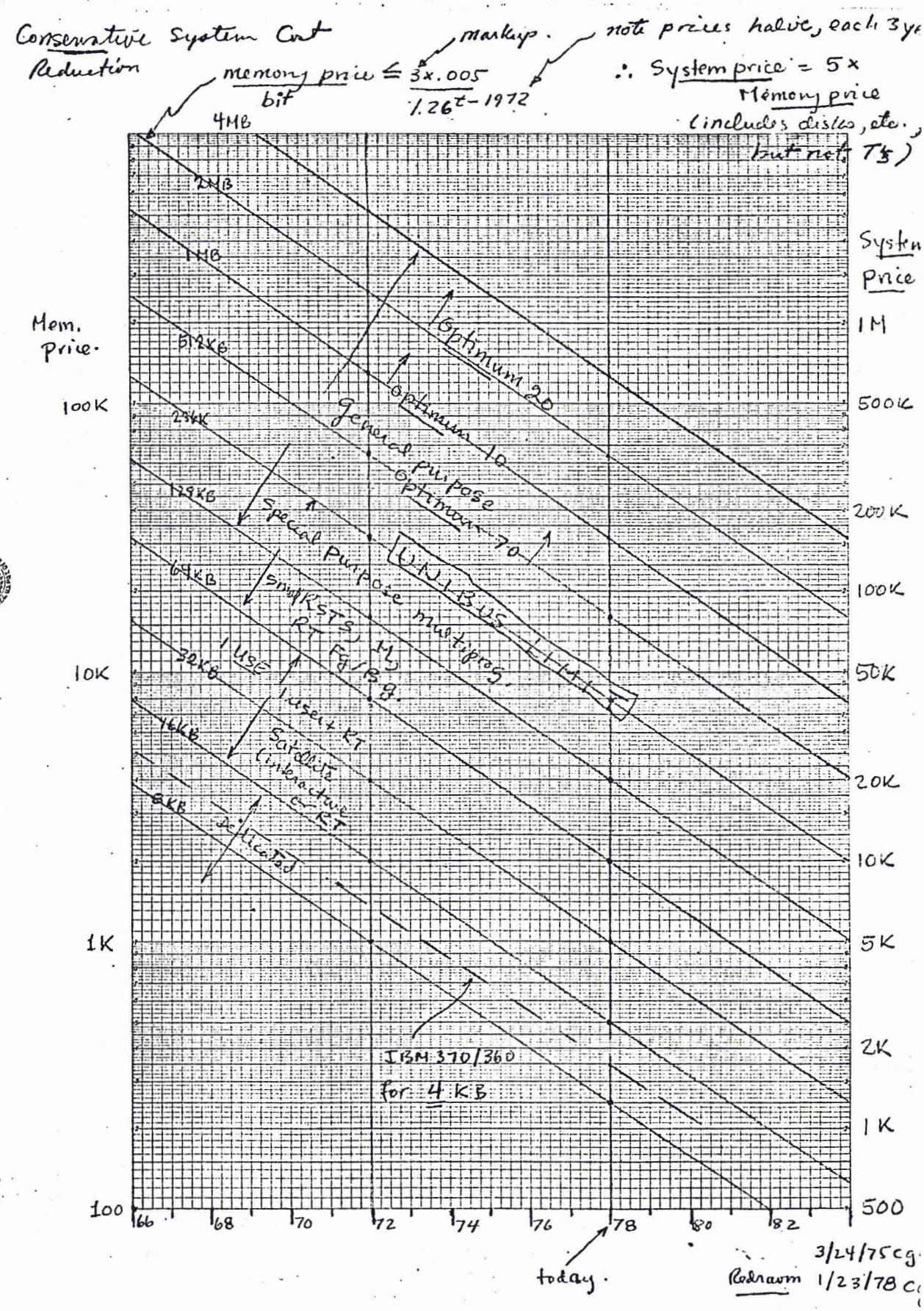
In summary, the alternatives

	11 standard	8086 standard
machine quality	better now, weak in addressing, series of increments from basic set already mostly developed.	can evolve quickly to scientific and commercial
basic software	mainly DEC based, but also standard UNIX, could be set on software standards we have spent the last 8 years	will have 1 system from Intel, remainder from industry--probably will evolve software standards over time.
user software	large base	phenomenal growth rate, given 0 cost hardware
business effect to DEC	wide scale availability of low cost 11 products placing competition on OEM. Our control will be software and peripheral interface standards. The true end user application will be uneffected.	wide scale availability of 8086-based systems to compete with us
	We will be involved and can sell 11 systems, applications, software, and DEC (services).	We will be ignored.
	As we wish, we can develop	

end user applications off
of our experience and that
of others.

GB:mjf

Distribution
OOD
Operations Committee
Marketing Committee
Base Systems Pot
George Beason
Buzz Brooks
Henry Crouse
Bruce Delagi
Lorrin Gale
Len Hughes
Glen Leedy
John MacKeen
Art Masicott
Roy Moffa
Steve Teicher



NOTES ON THE FORMATION OF DATA GENERAL

THOUGHTS PRIOR TO RETURN TO DEC IN JUNE 1972

I have the whole set of 23 memos on the original PDP-X, 16-bit machines. I wrote a strong letter of recommendation of the X to Stan Olsen on October 19, 1967 with copies to John Jones, Larry Seligman, Ed DeCastro, and Henry Burkhardt while I was at Carnegie. Ed and Henry visited me there to get my endorsement, and I gave it to them. I felt that a 16-bit machine was essential and inevitable in order to replace the 8, 9 and eventually 10.

└ LINC-8

I watched at a distance the manouvering of the various individuals about building the X. It wasn't clear who was in charge: Stan, Nick or John Jones? Larry Seligman sold the complexity of the X as being more difficult than the 10, which no doubt ensured its demise. Larry wanted to build it using microprogramming because of his experience with the 9. (This would have been a fine decision, although a bit tough in the 67 timescale. I was happy to go with the long term and more exotic architecture, even though it was clearly costly over something like an 8 or the 16-bit 8 (HP2100). The addressing was fine at that stage even though it would have required a tweak to get to 32 bits eventually.)

I was VERY unhappy that the X didn't get built because there was no alternative, and simply saw it as a typical managment fiasco of miscommunication: the big shouter/router/mixmaster, his brother trying to carry out orders, John Jones trying to be an executive like the General told him, and Ed (who played it close to the vest and wouldn't or couldn't communicate).

The development of the 11 was simply horrible given NO leadership. John Cohen, a programmer? / mathematician had been placed in charge with a rag-tag crew including Harold McFarland doing the design. The Unibus emerged from this, based on the notions I transmitted to Harold at CMU. They fooled around on an awful machine, the Desk Calculator Machine (DCM), which was clothed in secrecy so the DG guys wouldn't find out. People were leaving to go to DG then. DCM was awful. I told Cohen to work from benchmarks. He did, and DCM won them all... unfortunately you couldn't write a compiler for the machine.

Ultimately, Roger Cady was placed in charge and we redid the design at CMU one weekend along the lines of a machine that Harold had in his drawer. It used the general register concepts pretty much along the lines of what I developed in Bell and Newell and I had worked out with Harold at CMU. The key was the stack for procedure calls and interrupts.

The second round of 11's were tenuous at best: the 05, 40 and 45. I worked with O'Laughlin on the 40, Bob Armstrong did the 05 and Bruce Delagi, Len Hughes, Dick Clayton, and Ad Van de Goor worked on the 45. Another machine, the K, an 18 bitter surfaced under Jerry Butler's wing that Ad wanted to do. I ultimately wrote the definitive memo to kill it (K=KILL), because the concept of a range was somthing I pushed

at this point it being with Nick even though the 18-bitters and the X used to be there under Sfuzz. Not This mess

since the inception of the 11. Ad did work on the 11 memory management, and ultimately this got botched from what was proposed at CMU by Wulf and Parnas. The scheme was roughly equivalent to the Intel 8086 extensions. Compatiblity was played fairly delicately in doing the 5, in inorder to bring the rest of the company into the community of the 11. The 10 was a seperate world!

Clayton played a critical role in doing this along with Andy

With the final array of loosely compatible 11's, 05/40/45 I was happy to return in 72 for several reasons: I felt DEC must go to LSI and get a processor on a chip (the 4004 was emerging, and the future was clear to me!); the 11 had been botched and would have to be extended again; and I wanted to get back to real versus academic engineering. It was simply too frustrating trying to influence DEC at a distance!

KO'S SIDE ON MY RETURN
Pat J. Greene's notebook, which he turned over to Ken describes the business plan and thoughts behind the company. I was surprised to see the notebook that showed that DG and the X were being designed concurrently. Ken stated that Adler had threatened to counter-sue if DEC sued for dissertion. Ken also stated that Pat had gotten cold feet and as a result couldn't bear to leave DEC... even though he did at somepoint?,

DISCUSSION WITH GENERAL DORIOT AND DOROTHY ROWE July 17, 1983
They were very uncomplementary about the crew who formed DG, especially Fred Adler who visited The General. He feared that Fred might have had made a recording of their visit. The purpose of the visit was to warn DEC NOT to sue them. He clearly questioned Henry's integrity.

DISCUSSION WITH HENRY BURKHARDT July 29, 1983
Ed and Henry worked on the formation of DG during the time when the X was being designed. Henry said they didn't work on the machine both because of the legal reasons and because the parts were changing rapidly then and they should wait till the last minute before selecting the parts and doing the architecture around them. This also was a good idea because Ed had been burned on the negative logic DCD gates which should have been made compatible with positive IC logic, not the negative logic that was carried over from the original DEC logic. I too had argued this with Ken to no avail! The ultimate cost to DEC and its customers were MILLIONS because the ultimate switch cost so much more.

Henry claimed it wasn't a particularly good place to work at the time because they 6/10 folks dominated the scene intellectually even though the 8 was bringing in 125% of the profit. The X crew wasn't making friends because they mangaged to threaten every group including the 10... note that history says they were right. Kotok was making life miserable for them. Also there was product disarray with FOUR families: 4/5/LINC-8/6. A unified architecture was clearly needed, but there was no support for it. The X team had aligned with Nick Mazaresse who'd given them his support, but this was ultimately moved to report to Stan and then given the ultimate insult... reporting to John Jones. Henry spoke no kind words about John, who had risen to

fame by marketing pulse height analysis packaged systems to the physics market in the hey day of high energy physics. John was known as the repackager of other's ideas and was quick to let everyone know he was a student of The General's. No one wanted to work for John. Note that a few years ago John wanted to write the history of DEC... I think to exonerate himself as critical to its success (eg the pulse height business or his part in the DG business). Did the Bell Labs business start disappearing when John took it over?

Ultimately, Ed suggested that the X not be built because it had no support from its management. They were given no resources to do the design except some inexperienced tech by the name of Butler, who was clearly not up to building a computer. The crew (Ed, Henry, Sogge, Larry) and weren't given an assignment. (They probably did some interesting work on board size and memory designs during this time cause DG did go to a radically large board which could hold a cpu or a memory?)

As the DG plans progressed, Henry evoked a revolt to remove Pat as the president and stated that Ed had better be the president because he (HB) was too young. Pat was simply a loser. This explains the notebook coming to DEC.

The critical parts turned out to be the 4 x 16 bit ram, and the 4-bit ALU from TI, permitting a minimal mahcine to be built around the 4-bit nibble. Henry did the basic architecture so that it could have software written for it. At one point Henry said they thought of not having Index Registers, but luckily didn't because of the difficulty of calling procedures and addressing arrays. The Eclipse added the essentials of procedure calls, which were costing 40% of the runtime.

Henry said the machine and software were trivial, given his training at DEC. The assembler, loader, operating system, and editor (teco subset) came over from the 10!

Richman was a salesman for Fairchild? and looked into parts plus supplied the names of venture capitalists and Fred Adler.

Sogge was ok as head of engineering, but ultimately left because he simply couldnt' / wouldn't communicate. Dick estabished the semi operation. He wouldn't say anything, and finally left to do some focussed things: invested in bonds one year, built tennis clubs one year. He lives in South Saulitto.

Henry left DG after burnout in 76? when he worked 14 hours/day and weekends for several years to save the company. He took over manufacturing, while being the chief financial officer, head of programming including mis, diagnostics, and swe. After regaining control in light of rising inventories and lack of output, he told Ed he wanted to leave. He did so in 9 months after getting the right folks to take over for him. After a year, he asked about returning, but Ed was indifferent so he stayed away and eventually left the bod.

I told Henry that I returned to do VAX, having let the folks botch the

extensions to the 11 (remember you can only make one extension to a GOOD machine before it becomes a kludge.) Henry said they were all concerned then because they thought they could beat DEC as they knew it without me. I clearly agree with Henry because I don't think DEC would have gone into VLSI, VAX, "the Environment", gate arrays, QDM, QIA, PC's, Trilogy, etc. without me (see the DECworld July 83).

I asked Henry whether they would have left DEC, had the X proceeded. He answered: "you know what turns engineers on... we would have never left".

GB'S THOUGHTS
The Soul of A New Machine pretty much typified what I thought was DG (and DEC)... basically a pretty manipulative environment with NO real right to actually pull the design off! DG was lucky to actually get the machine to work, given the strictly opportunistic management!

I gave no credence to DG at anytime. I knew the people and felt I had an adequate model of how they thought about engineering, computers and management oriented to short term opportunities. Ken and Ed were pretty much alike in their orientation, alhtough I gave the edge to Ken in terms of thinking about the future... now 7/31/83 Sun I'd pretty much toss a coin about which one I'd take for the long term. DG was still a thorn in 72, but I never paid any attention to them, instead concentrating on building an organization and the technology that would make DEC number 2.

Queue of jobs...

- I/O sub bit processing
  Bit

Display processor —

memory size

Microprogram implementation - have pref... available to ... shell

Think out whole system -- mapping

- multiprocessor (synchronous)
- multicomputer

PDP-X

Description

Communication processor
a job dri... stick.

revision date

5/1/67

5/12/67

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- 5.1 Concise definition of instructions

PDP-X is a modern, very high performance, third generation computer family designed for the small computer market. Upward and downward program compatibility permits easy system growth and enhances application programming. Standard IO and Memory interfaces are used for all processor models and all perhipheral devices. The architecture lends itself to fourth generation hardware implementation and the development of multiprocessor systems.

The system architecture of the PDP-X computer family is described below. In addition to specifying the organization of the entire family, details of a particular implementation have been included. The major design objective has been significantly increaded performance in order to meet increasingly more sophisticated user demands.

1.1 The performance of current products

Although there is no magic formula into which parameters of vastly different machines may be substituted to achieve an absolute measure of performance, the relative performance of past and current DEC small computer central processors may be estimated since their architectures are so closely related. Factors relating to word length, order code, memory speed possible, etc., have been evaluated and are given in figure 1. PDP-6/10 has been somewhat arbitrarily estimated to be an order magnitude more powerful than PDP-7/9. System performance dependence upon available software and optional perhipherals has been specifically omitted. Note that the PDP-8I ~~does~~ does not appear, its performance is identical to that of the PDP-8; 9+ and 1+ represent versions which include optional multiply/divide and priority interrupt hardware.

The PDP-X, designed to be, initially, a replacement for the PDP-9, has a minimum performance at least equal to the 9+ and possibly several times better. This performance extends upwards with the addition of processor options. Other implementations of the same architecture span markets currently held by PDP-8 and the currently nonexistant 24 bit machine. Selling prices as a criterion for the machine would shift the set of curves for PDP-X left. The PDP-9 replacement has approximately the same amount of hardware and based upon estimates of integrated circuit costs derived from PDP-8I, its manufacturing cost should be half PDP-9. Similarly, the very smallest model, running with a slow memory, should cost less to manufacture than the PDP-8S.

The performance/price ratio of PDP-X to PDP-9 is, conservatively, 3 to 1. Verification of this ratio is difficult without more cost estimation and a considerable programming test. Perhaps the best measure will be the relative performance and size of the Fortran IV compiled programs and the effort required to write the compiler itself. — True. — What are the indications so far?

1.2 Models

Three basic models are worth singling out of the possible implementations. As shown in figure 1, they cover a performance range from PDP-8 to smaller versions of PDP-10 and may be aimed at, respectively, the PDP-8, PDP-9, and a currently non extant 24 bit processor. The two larger models would compare in performance to the SDS Sigma 2 and Sigma 5.

The smallest processor, the PDP-X / 14, has only the basic instruction set implemented and all its registers are located in main core memory; a typical ADD instruction takes 4 memory cycles at less than a microsecond each. The longer word length, lower price, and superior instruction set make this machine superior to the -8. The processor may also be implemented using an even less expensive memory system to achieve the minimum cost true's complement computer. Expansion to a system with hardware general registers is not possible since the flow chart must differ to optimize each processor.

The medium processor, PDP-X / 16, implements its registers in a fast memory array and is provided with an expanded instruction set. Additional instructions as well as a number of interrupt channels with corresponding general register sets may be optionally installed. As in / 14 the memory width is 16 bits but some double word instructions are implemented.

The largest processor, PDP-X / 32, is an expanded version of the above. Although the word length is still 16 bits, many double word instructions, including floating point, are implemented and the basic memory width is 32 bits to speed instruction processing. The economics of building this machine, especially for markets which do little if any serious arithmetic computation, needs careful scrutiny.

1.3 Design goals

a. Advanced concepts- The system architecture should make superior use of currently available and anticipated technology. In particular, program core storage requirements must be reduced to minimize the relatively expensive memory's contribution to total system cost and the architecture should be amenable to the use of internal scratch pad memories, gate arrays, and other forms of large scale integration.

b. Implementations- The architecture should be implementable in several processor models whose price and performance span the entire small computer market and include a model small enough to use as part of an IO device controller or selector channel. Smooth evolution and reimplementation should be possible over the next several years as the architecture leads to many new models.

c. Software- Although major hardware improvements are possible, even more significant gains can be achieved through further development of software systems. The hardware necessary for dynamic memory allocation/protection, privileged instruction traps, and other features of complex software systems must be imbedded into the basic design. A true real-time compiler, especially one that permits dynamic memory assignment, seems a necessity. There are many special application packages that would make the system far more useful in many new market areas.

d. Standard interfaces- Standard memory and IO interfaces must be shared by all processor models, memories, and perhipherals in order to unify the set of options and to facilitate field expansion of systems.

e. Goals of the implementations- To the normal goal of lowest possible manufactureing costs for any model may be added the requirement of automated production and production test facilities. System selling prices should be reduced by making it possible to produce useful results using less of the more powerful hardware and software.

f. Specific IO goals- Control signals available at the IO interface should permit channel control of all basic perhipherals; device hardware requirements should be minimized, any special timing, for example, should be done in the processor IO logic; the system should respond extremely rapidly to interrupts, even those requiring the full processor computational ability; communication with devices physically far from the processor should be possible; the IO bus should be mechanically simple.

g. Specific processor goals- the order code should be as concisely organized as possible, placing as few arbitrary restriction on the program as possible; a single instruction should be able to directly address anywhere in memory as well as call upon an immediate operand; the most common instructions must be available in compressed form to conserve memory requirements; recursive, reëntrant, and pure code should be possible.

h. The system architecture should in no way limit system expansion as a multiprocessor. Future implementations should include a dynamically restructureable multiprocessor which exhibits fail soft features.

i. Multi computer organization.

1.4 Design Decisions

a The basic word length has been choosen to be 16 rather than 18 bits in order to maintain compatibility with the majority of the newer computers, especially IBM. The byte and character are 8 bits long; a double word consists of 4 bytes; a floating point word, with hexadecimal radix, contains either 4 or 8 data bytes.

b The word, 16 bits of data, has been choosen to be the basic addressable unit although instructions are available which reference bits, bytes, words, doublewords, etc. as data. Doubleword instructions need not fall on doubleword boundaries although double data words must.

c The basic structure contains multiple accumulators/index registers. The general register structure simplifies the order code and proves greater programming power over more conventional single accumulator organizations. The floating point registers, more of a programming convention than hardware feature on the two smaller processors, are distinct from the general registers.

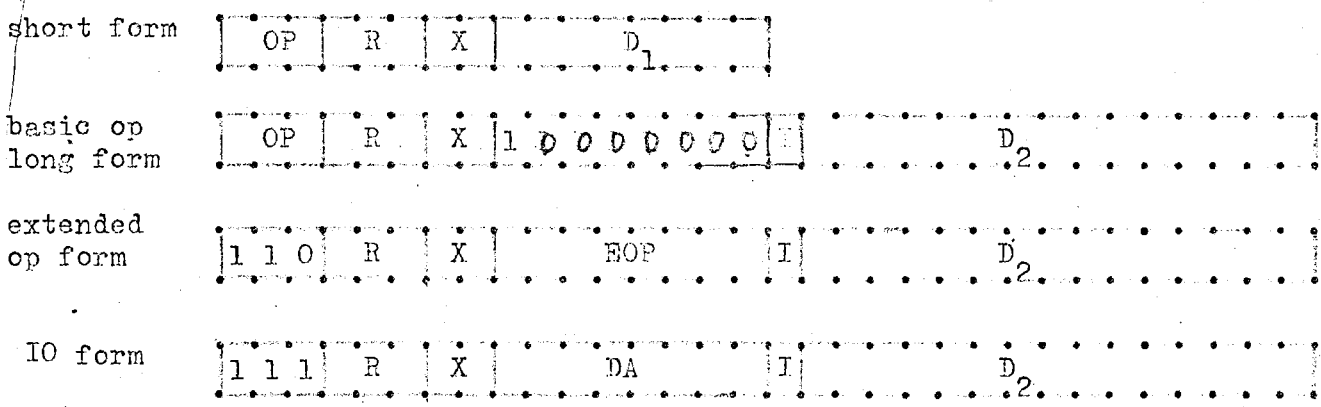
d No base registers are used in addressing, instructions are capable of addressing relatively, indexed, and to page 0 in the short format. A long format permits direct specification of any word anywhere in the entire memory system. The most common instructions are available in short form, all are available in long form.

e The basic unit of IO data is the byte. This unit is natural for paper tape perhipherals, the most common types, as well as the teletype. The bus organization permits the transmission of a full word whenever necessary.

f A priority interrupt system which permits direct device recognition is provided as standard. Separate register sets for the interrupt levels are provided to maximize IO bandwidth.

g A standardized, unified IO structure common to all processors permits both program controlled and channel controlled transfers over the same bus with a minimum of device hardware.

2.1 Instruction Format



mnem	bits	definition
OP	3	basic operation code specifying major instruction class
R	3	general register specification or sub function selection for non accumulator reference instructions
X	2	index register and address mode selector
D_1	8	short form address and immediate operand
D_2	15	long form address
I	1	indirect addressing specification
EOP	8	extended operation code specifying instruction
DA	8	IO device address and bus selection

2.2 Instructions

Instructions may be divided into 2 groups , basic and extended. The basic instructions appear in all models and may either be in long or short format. Extended instructions are implemented in some models, they trap when executed in machines for which no hardware has been provided; all extended instructions are long format only. Instruction class is determined by the 3 Op Code bits (0,1,2) of the instruction word. EOP (extended) instructions are characterized by a 110 pattern in the Op Code and the specific operation in the D_1 bits.

/14	/16	/32
All basic instructions are implemented; the EOP class is uniformly trapped.	All basic and some EOP instructions, the remainder of the EOP class trap.	All EOP and basic class instructions, some EOP class are, by convention, still trapped

Instructions may also be classified by the type of operand they effect. These include:

arithmetic	signed words
logical	unsigned words
floating	floating point double/quadruple words
branch	address pointers
IO	IO system

class	OP	mnem	definition
load	0	L	load selected register (R) from memory; condition code remains unchanged
store	1	ST	store selected register (R) into memory; condition code remains unchanged
and	2	N	and selected register (R) with memory, place result in selected register; condition code 0 remains unchanged 1 set if negative result 2 cleared if zero result, set otherwise
add	3	A	add contents of selected register (R) to memory following the rules of two's complement arithmetic, place result in selected register; condition code bits are first cleared and then set as follows: 0 set if carry out of bit 0 1 set if negative result 2 cleared if zero result, set otherwise
branch	4		general conditional branch and subroutine linkage instruction; R bits specify particular operation. When R=7 the program counter, updated to point to the instruction following the branch, is saved in general register 2. The condition code remains unchanged for all branch instructions.

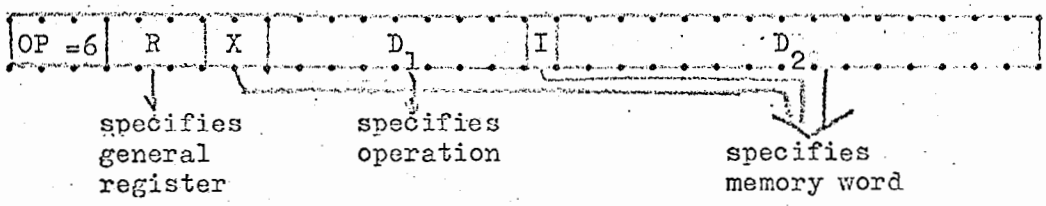
	R	condition
BCZ	0	branch if condition code bit 0 set
BM	1	1
BN	2	2
B	3	unconditional branch
BNC	4	branch if condition code bit 0 not set
BP	5	1
BZ	6	2
BAL	7	branch and link

class	OP	mnem	definition
modify	5		general memory modification instruction, R bits specify particular operation. Condition code bit 0 is changed only by the two shift instructions (R=4,5). Condition code bits are set as follows for all modify instructions: bit 1 set if negative result, cleared if positive bit 2 cleared if zero result, set otherwise

R	mnem	operation
0	T	no operation but condition code is set to reflect state of the memory word
1	C	logical complement, the memory word is complemented on a bit by bit basis
2	I	increment, one is added to the sepcified memory location
3	CI	arithmetic complement (two's), complement then increment, negate
4	SR	shift right, the memory word and condition code bit 0 are rotated together as a 17 bit register one place to the right, loading condition code bit 0 from bit 15
5	SL	shift left, the memory word and condition code bit 0 are rotated left together as a 17 bit register, loading condition code bit 0 from bit 0 of the memory word
6	SB	swap bytes, the left and right bytes of the memory word are interchanged
7	CL	clear, the memory word is set to all zeros

class	OP	mnem	definition
EOP	6		extended operation code class; forced long format; D_1 bits specify particular operation to be performed by selecting an entry point into a read only memory routine. The effect on the condition code is determined by the particular operation performed.

EOP class instruction doubleword



If the operation specified has not been implemented in the machine a trap occurs as follows:

location 8_{10} receives the updated program counter
9 EOP instruction
10 effective address
11 contains the entry point into the EOP handler. This word is loaded into the program counter

Since D_1 codes 0 through 31_{10} are never implemented in the machine hardware, some 32_{10} programmed operators are available.

Extended Operation Codes

The opcode is located in D.1. The first 64 of these (codes 000 - 077) are reserved for monitor calls, Fortran operating system calls, etc.

Below is a list of the first sixteen (20) of the implemented instructions.

OP	mnem	definition ptr. incmt
100	LDC	Load Character. The content of the effective address is used as a character pointer to locate an 8-bit byte. This byte is loaded into the right half of the specified R-register. The left half is cleared. The addressed memory word is left unchanged.
101	STC	Store Character. The content of the effective address is used as a character pointer. The right half of the specified R-register is stored at the indicated character position. The other half of the addressed word is unaltered. The content of R remains unchanged.
102	MUL	Multiply. The content of the effective address is multiplied by the content of the specified R-register. The high order result is stored in the specified R-register and the low-order result is stored in the next odd R-location. If R already is odd, the low order result is stored in the specified R-location. C(EFA) x C(R) → C(R), C(R+1). The arguments are treated as 16-bit logical data. The result is a 32-bit logical double word.
103	MULS	Multiply Signed. This operation is the same as MUL except that the arguments are treated as signed 2's complement data. The result is a signed 2's complement double word.

(Note: Both MUL and MULS leave CC0 unchanged. CC2 is set if the double word result is non-zero, otherwise it is cleared. CC1 is set if bit 0 of the high-order result is one, otherwise it is

OP	mnem	definition

104 DIV — Divide. The logical double word located by the R-field is divided by the logical word located by the effective address. The result is stored in the double word located by R.

C(R), C(R+1) ÷ C(EFA) → C(R) remainder
C(R+1) quotient

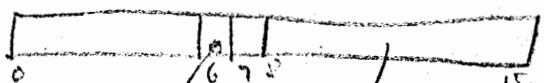
(note: if R is odd, this is an integer divide)

105 DVS — Divide Signed. This operation is the same as DIV except that the arguments are treated as signed 2's complement data. The remainder and quotient are stored with the correct sign such that the identity:
dividend = divisor × quotient + remainder
holds. (Note: CC0 is left undisturbed and CC1, CC2 are set according to the quotient).

106 SUB — Subtract. The content of the effective address is subtracted from the content of the specified R-register. The result is placed in the specified R-register. The content of the effective address remains unchanged.

C(R) - C(EFA) → C(R)
(Note: The condition code bits 0, 1, 2 are set as in ADD).

107 SHFT — Shift. The content of R is shifted as indicated by the content of the effective address.



Signed shift count
> 0 : left
< 0 : right
0 : no shift

Shift mode
00 - rotate
01 - rotate with CC0
10 - arithmetic shift
11 - logical shift

The result shall - byte of the content of the effective address is used as a signed step count. A positive value indicates a left shift. A negative value indicates a right shift. Bits 6,7 of the effective word indicate the type of shift to be performed:

00 rotate - bits leaving one end enter at the other end.

01 rotate with CCϕ - bits leaving one end enter condition code bit ϕ. CCϕ enters at the other end.

10 arithmetic shift - perform two's complement multiplication by powers of two. The sign is unchanged. When going to the right, the sign is shifted into bit 1. Ones or zeros leaving bit 15 are lost. The arithmetic error bit is set if, during shifting, the sign bit and bit 1 became unequal

11 logical shift - bits leaving one end are lost and zeros enter the other end.

Condition code bit ϕ is undisturbed except for rotate with CCϕ. CC bits 1 and 2 are set according to the result.

LOGICAL COMPARE AND MODIFY (opcodes 110-113)

Bits of an R-field word that are masked by bits of a memory word may be tested and/or modified to determine a conditional branch. The bits to be tested and/or modified are selected by ones in the content of the effective address. Condition code bit 2 is cleared if all of the selected bits of the R-field word are zero; otherwise it is set to a one. Condition code bit 1 is set to a one if bit ϕ is selected and bit ϕ of the R-field word is a one; otherwise it is cleared. The selected bits of the R-field word are then modified or not depending upon the operation being performed.

110 TSTN Test. Test the content of the R-field word with the content of the effective address. Set condition code bits 1 and 2 according to the result.

111 TST Z Test and Zero selected bits. Test the content of the R-field word with the content of the effective address. Set condition code bits 1 and 2 according to the result. Clear selected bits in the R-field word (ie, for every one in the content of the effective address, clear the corresponding bit in the R-field word).

112 TSTO Test and set selected bits to Ones. Test the content of the R-field word with the content of the effective address. Set condition code bits 1 and 2 according to the result. Set selected bits in the R-field word (ie, for every one in the content of the effective address, set the corresponding bit in the R-field word). This performs the logical function inclusive or.

113 TSTC Test and Complement selected bits. Test the content of the R-field word with the content of the effective address. Set condition code bits 1 and 2 according to the result. Complement selected bits in the R-field word (ie, for every one in the content of the effective address, complement the corresponding bit in the R-field word). This performs the logical function exclusive or.

114 LCMP Logical Compare. Compare the content of the R-field word with the content of the effective address both treated as unsigned logical words. Set condition code bits 1 and 2 according to the result.

115 ACMP Arithmetic Compare. Compare the content of the R-field word with the content of the effective address both treated as signed arithmetic words. Set condition code bits 1 and 2 according to the result.

116 PUSH-DOWN class. The R field of the instruction is decoded to determine the function to be performed. In the following mapped location 12 is the push-down pointer which always points to the last item placed on the push-down list. Location 13 is the push-down counter. It is incremented each time an item is placed on the push-down list and is decremented each time an item is removed from the push-down list. A carry out of bit 0 indicates a push-down error.

Mnem	R	Definition
PUSH	0	Push. The content of the effective address is placed in the next location of the push-down list.
PUSHB	1	Push and Branch. The program counter is placed in the next location of the push-down list. The effective address replaces the program counter.
PUSHBL	2	Push, Branch and Link. The subroutine linkage register is placed in the next location of the push-down list. The program counter is placed in the subroutine linkage register. The program counter is placed in the next location of the push-down list. The effective address replaces the program counter.
———	3	Unused
POP	4	Pop. The last word placed on the push-down list is removed to the content of the effective address.
POPB	5	POP and Branch. The sum of the effective address and the last word placed on the push-down list replaces the program counter. This is the return

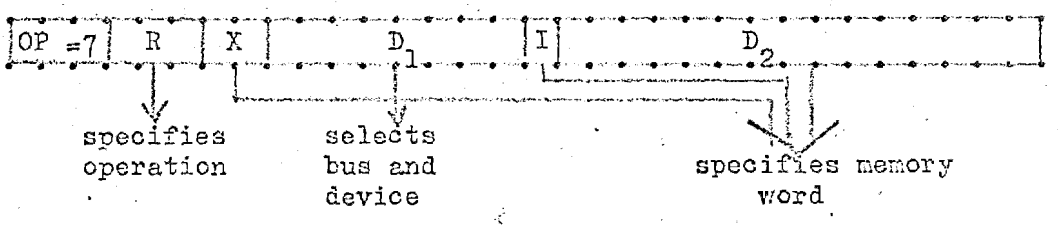
pair for PUSHBL.

POPBL	6.	Pop, Branch and Link. The sum of the effective address and the last word placed on the push-down list replaces the program counter. The last word placed on the push-down list is then placed in the secondary linkage register. This is the return pair for PUSHBL.
—	7	Unused

class	OP	mnem	definition
IO	7		input/output instruction class; R bits specify particular operation; forced long format. D_1 is taken to specify the device, the lower order 6 bits select a device code, the high order 2 bits select one of 4 possible IO busses. Condition code bit 0 is unchanged. Condition code bit 1 is set on the read status (IOS) instruction if no device responds and on the command (IOC) instruction if the command is unacceptable. Bit 2 is cleared if the data byte or word resulting from the operation is identically zero, it is set otherwise. This has particular meaning in the IO test status (IOT) instruction. A byte is normally transmitted to the device from the right half of the effective address, some devices will automatically take the second byte also.

	R	operation
IOR	0	read device data word into selected memory word
IOS	1	read device status into selected memory word
	2	unassigned
	3	unassigned
IOW	4	write device data word from selected selected memory word
IOC	5	command, write device status from selected memory word
IOT	6	test status, the device status and the selected memory word are ANDed, a non zero result sets condition code bit 1
	7	unassigned

IO class instruction doubleword



Read instructions to a device that can write only or write instructions to a device that can only read will result in no data transfer.

2.3 General registers

Each level of priotiry contains a set of 16 general registers, 8 of which may be used by the program as accumulators, index registers, etc. The program status word (PSW) occupies registers 0 and 1. These registers occupy page 0 words 0 to 7 in the memory space as well as the R bits in the instruction, hence register to register instructions are possible. The registers may be stored, loaded, added into, etc. depending on the operation code of the particular instruction used. The second group of 8 registers contain the trap locations for unimplemented EOP instructions and the push down words. These may be modified or read as memory words but are not explicitly referenced as accumulators.

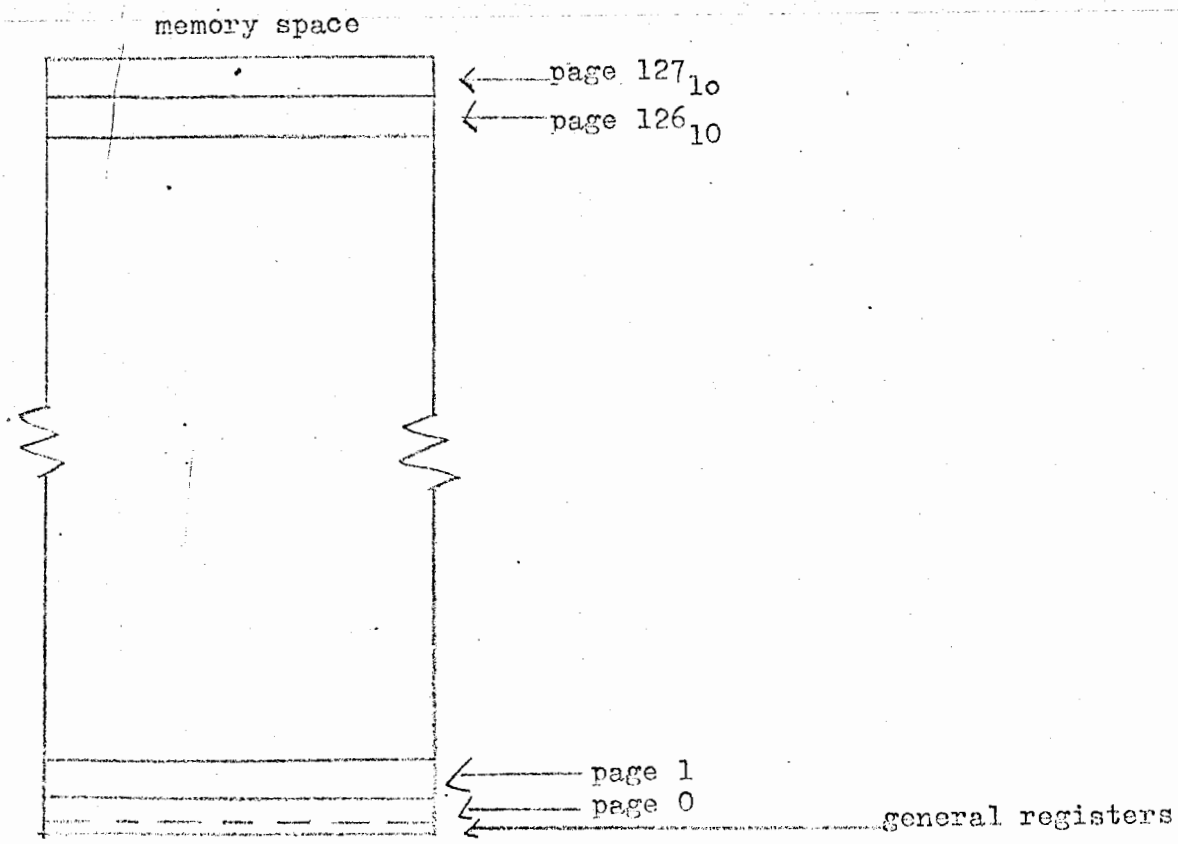
register	use
0 R_0	status word, contains condition code, etc.
1 R_1	status word, contains program counter (PC)
2 R_2	accumulator, subroutine linkage register, or secondary index
3 R_3	accumulator or main index register — ?
4 R_4	accumulator
5 R_5	"
6 R_6	"
7 R_7	"
8	EOP, receives the updated program counter
9	EOP, " instruction itself
10	EOP, " effective address
11	EOP, contains the entry point into the ECP handler, loaded into PC
12	contains the push down pointer
13	" " " " counter
14	reserved for use by processor
15	reserved for use by processor

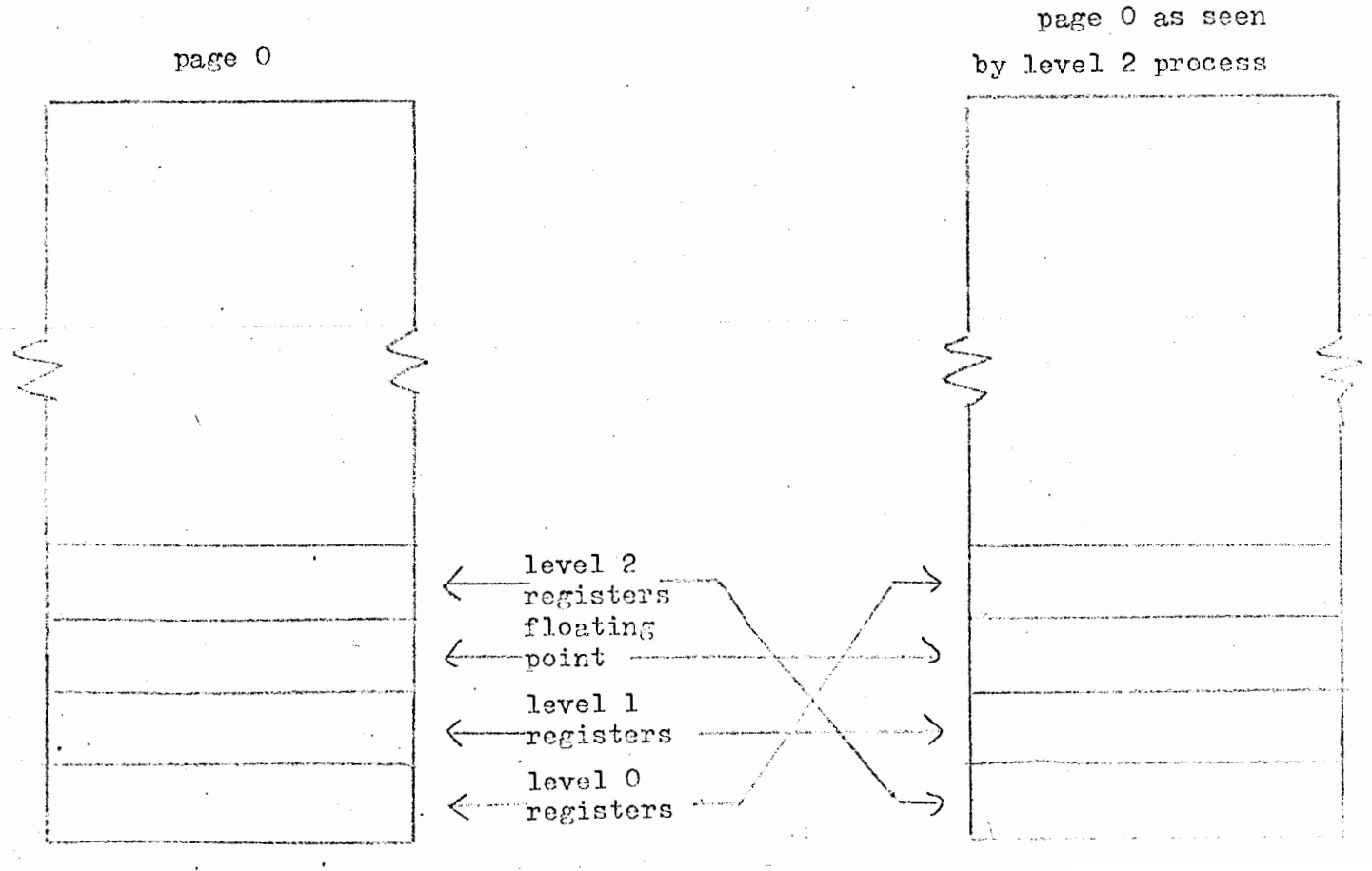
For each level of machine priority, both background and IO, there exists a set of general registers; in addition, the hardware insures that the applicable set is available at apparent locations $0\text{-}15_{10}$ in memory address space. Thus, the general registers need not be stored and restored during interrupts.

The lowest (background) priority level contains floating point registers. These registers are not available for use on the higher priority levels unless they are explicitly stored and restored under program control. Each of the 4 floating point registers is 64 bits (4 words) long, permitting multiple precision floating point instructions. In all floating operations the R bits of the instructions specify these registers, only the low order 2 bits of R are used.

The set of general registers map onto the main memory space in page 0. The figure on the left shows the entire memory space; the figure on the right is an exploded view of physical memory. Apparent memory is the memory space as seen by the running process; this differs from physical memory in the location of its general registers as is shown for a priority level 2 process in the bottom figure.

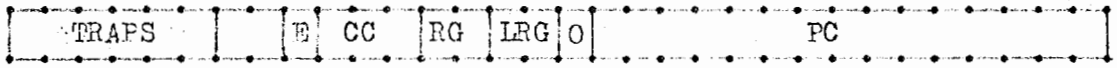
model	levels
14	2, core
16	2 minimum hardware, 4 maximum
32	4 hardware


memory space
page 127_{10}
page 126_{10}
page 1
page 0
general registers


page 0
page 0 as seen
by level 2 process
level 2
registers
floating
point
level 1
registers
level 0
registers

2.4 Program Status Word

The collection of bits that constitute the state of the processor between instructions are called, collectively, the Program Status Word (PSW). This state word occupies the doubleword at memory locations 0 and 1 of the active process, corresponding to general registers R_0 and R_1.



bit(s)	definition
0	arithmetic (add, divide, floating, etc.) enabled if bit 8 = 1
1	machine check (processor or memory error)
2	nonexistant memory (reference to an address not in the memory system or to a protected area)
3	nonexistant instruction (attempt to use an instruction for which no such hardware has been provided)
4	priveleged instruction (attempt to execute a system instruction while in user mode)
5	read only violation (attempt to write into a write protected memory area)
6-7	unused
8	arithmetic trap enable
9	condition code bit 0
10	condition code bit 1
11	condition code bit 2
12-13	priority of active process (current register group)
14-15	priority of interrupted process (last register group)
16	unused, always 0
17-31	program counter of active process

2.5 Addressing

Addresses are generated by either long or short format instructions. In either case, the processor forms a 15 bit effective address (EFA) which it sends to the memory system. The left byte (high order 7 bits) of the address is called the page, the right byte is called the line; there are 128 pages of 256 words each directly addressable.

The available addressing modes are :

direct (no indexing) to any word in memory ,

relative ($\pm$ 127_{10} words from the instruction);

immediate (the next word is the operand,

linked (the subroutine linkage register is used to pick up arguments or make returns),

indexed. The short displacement (D_1) is taken to be a two's complement negative number whose sign is to be extended. Long format addresses are specified whenever $D_1=128_{10}$ or the instruction implicitly forces this format (all IO and extended op code instructions).

Addressing table

X	short	long	description
0	D_1	D_2	direct
1	$\pm D_1+PC$	PC+1	relative/immediate
2	$\pm D_1+R_2$	D_2+R_2	linked
3	$\pm D_1+R_3$	D_2+R_3	indexed

The basic addressable unit is the word (two bytes, 16 bits), although certain instructions do reference bytes or doublewords. Words in storage are consecutively numbered starting with 0. The 15 bit address field accomodates a maximum of 32,768 words. When only a part of the maximum storage capacity is available in a given installation, the available storage is contiguously addressable from 0. A nonexistant memory trap occurs when any operand is located beyond the installed capacity. The invalid address is recognized when the data is accessed and a program interruption occurs.

2.7 Priority (Interrupt) Structure

The interrupt system is designed to handle 4 levels of priority including the main program (at the lowest level). The interrupt due to an internal source (trap) or external source causes the new, appropriate set of general registers to be used in place of the previously operating set. Hence, no time is lost before the interrupt service program can begin. Priorities of service are fully nested; high priority requests interrput low priority processes but even lower ones are delayed. Linkage between the interrupted process and the interrupt process is performed by the LRG bits of the program status word (PSW). These bits receive the priority number of the interrupted process; the priority of the currently active process is contained in a 2 bit register, the register group (RG) register. Priorities are assigned as follows:

Level (RG=)	use
0	main program
1	traps, lowest hardware device level
2	device hardware level
3	highest hardware device level

When an interrupt occurs, the LRG bits of the new PSW are loaded from the RG register. The RG register is then set to the new priority level. Subsequent instructions will come from the interrupt process PC and register set. The interrupt is cleared with a debreak IO instruction which loads the RG register from the LRG bits of the current PSW. Subsequent instructions will be from the originally interrupted process.

3.1 Devices and controllers

The hardware involved in IO operation is logically divided into 4 parts: IO section, IO bus, controller, and device. The IO section and bus are described in detail below. Controllers and devices are generally different for each type of IO media; from the programming point of view most controller functions merge with IO device functions.

In all cases, the controller function is to provide the locical and buffering capabilities necessary to operate the associated IO device. Each controller functions only with the IO device for which it is designed, but each controller has standard signal connections with regard to the IO bus. The teletype device (keyboard, printer), for example, connects to the IO bus through teletype controller logic (single character data buffering and interrupt logic). The detailed meaning of the command/status bits read under program control through the IO section from controller type to type but the general format remains unchanged.

3.2 Modes of data transfer

There are 3 basically different modes of data transfer available in the IO system: program controlled, multiplexor channel, and selector channel. All three use the standard IO bus interface; the third, optionally implemented, provides an additional physical bus interface and additional control logic at the processor end. Maximum data transfer rate of each mode varies with processor model, the program controlled rate is lowest and the selector channel rate highest. In all cases transfer sequences are initiated by IO instructions issued to the appropriate controller, rather than to the channel.

Program controlled transfer, while slowest, provides the greatest flexibility. Data may be modified, limit checked, or otherwise monitored as it is inputted and special control sequences required by special purpose or custom designed IO equipment may be generated. For the slower devices, especailly paper tape or teletype, direct program control of IO leads to simpler programming.

Multiplexor channels are provided in the basic processors. When a device requires channel servicing, the state of the processor is dumped, the device serviced, and the state of the processor restored. The program never realizes that the transfer took place except that it has been subjected to a short delay. The multiplexor channel is capable of sustaining concurrent IO operations with several devices. Bytes of data are interleaved together and routed to or from the selected IO devices and to or from the desired locations in main storage. The channel's single data path is time shared by the concurrently operating devices.

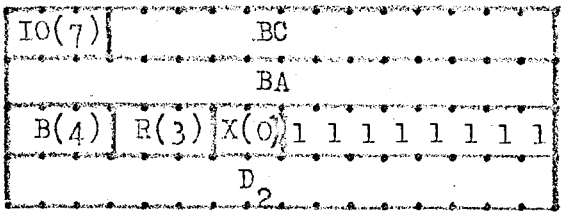
Selector channels are capable of operating only one device at a time, however they permit extremely high data rates, over a million bytes per second is possible. Devices such as disc files operate only with seclector channels, other devices operate in all data transfer modes. As with the multiplexor channel, the selector channel is invisible to the programmer; all instructions are directed at the device rather than the channel. Devices requiring special hardware features in the IO system, such as signal averaging, normally would add a selector channel with appropriate ROS control

3.3 Operation of the multiplexor channel and interrupt

A device signals that it needs attention by requesting service at the priority level that has been assigned to the device. Devices operating on the multiplexor channel require attention for every byte (word) of information transferred; devices under program control require attention whenever they complete a specified operation. When the priority of the active process drops below the priority of the request, the interruption occurs. The state of the old process is stored in its general register set (R_0 and R_1 contain the processor state) and a new general register set is switched in. The priority of the old process is saved in the LRG bits of the new status word. Processor hardware then requests the device to transmit its address (6 bits); the address is or'ed into bit positions 8 through 15 of a word with bit position 7 set to 1 and all other positions 0. This address, called the interrupt address, lies somewhere on page 1.

Subsequent operation depends on the word found at the interrupt address. Any instruction class other than IO is executed, such an instruction is normally a branch to an IO service routine for program controlled transfer operation. An IO class instruction signifies that the device is under multiplexor channel control. A byte (word) of data is read from (written to) the device and packed into memory (unpacked from memory). The byte address pointer and byte counter are updated. If the byte counter went to zero indicating that the last byte (word) has been transferred or the device indicated an unusual condition, the instruction following the IO class instruction is also executed. This is normally a branch to an IO service routine that re-initializes the device and channel for subsequent operations. If no unusual condition was detected and the byte counter did not overflow, the device continues operating and will reinterrupt with the next data byte.

The format of the words starting at the interrupt address for multiplexor channel operation are given below. The double word at that address for program controlled transfer is a simple single or doubleword branch instruction. Branch instructions are normally unconditional, direct.



BC stands for byte counter and maintains a count of data bytes as they are transferred to and from the device. Prior to each transfer BC is incremented to determine whether or not this is the last byte. When initializing a device for multiplexor channel operation, the programmer must load BC with the two's complement of the number of bytes to be transferred. At the end of channel operation, the entire word at the interrupt address will be set to zero. Exceptional conditions which cause termination before the specified number of bytes is read leave the word non zero.

BA stands for byte address and maintains the address of the data byte next tobe transferred to and from memory. Prior to each transfer BA is incremented to form the byte address of the data byte. This byte address is shifted right before use to form a word address, the end bit determines which half of the word the data byte will be loaded into. A 1 indicates the left byte, a zero the right byte. When the program initializes the channel it must load BA with the byte address of the first byte to transferred.

Unless the word executed at interrupt address (or interrupt address + 2 when reached during channel operation) is a branch class, control immediately returns to the interrupted process. The priority level is restored from the LRC bits and the processor continues with the old program counter, status, and general registers.

3.4 IO BUS

The connection between the processor and the IO device control units is called the IO Bus. The interface consists of signal lines that connect the control units to the processor; except for the signal used to establish selection, all communications lines to and from the processor are common to all control units. At any one instant, however, only one control unit may be logically connected to the processor. The logical connection is maintained from the time it is first established by the processor until it is broken by the processor. The rise and fall of all signals transmitted over the interface are controlled by interlocked responses. This interlocking removes the dependence of the interface on circuit speed and bus length, making it applicable to a wide variety of circuits and data rates.

32 signals comprise the bus including 16 control signals and 16 data signals. Half of the signals transmit to the processor, the other half recieve from it. The Select Out signal is retransmitted by each device, as is Select In.

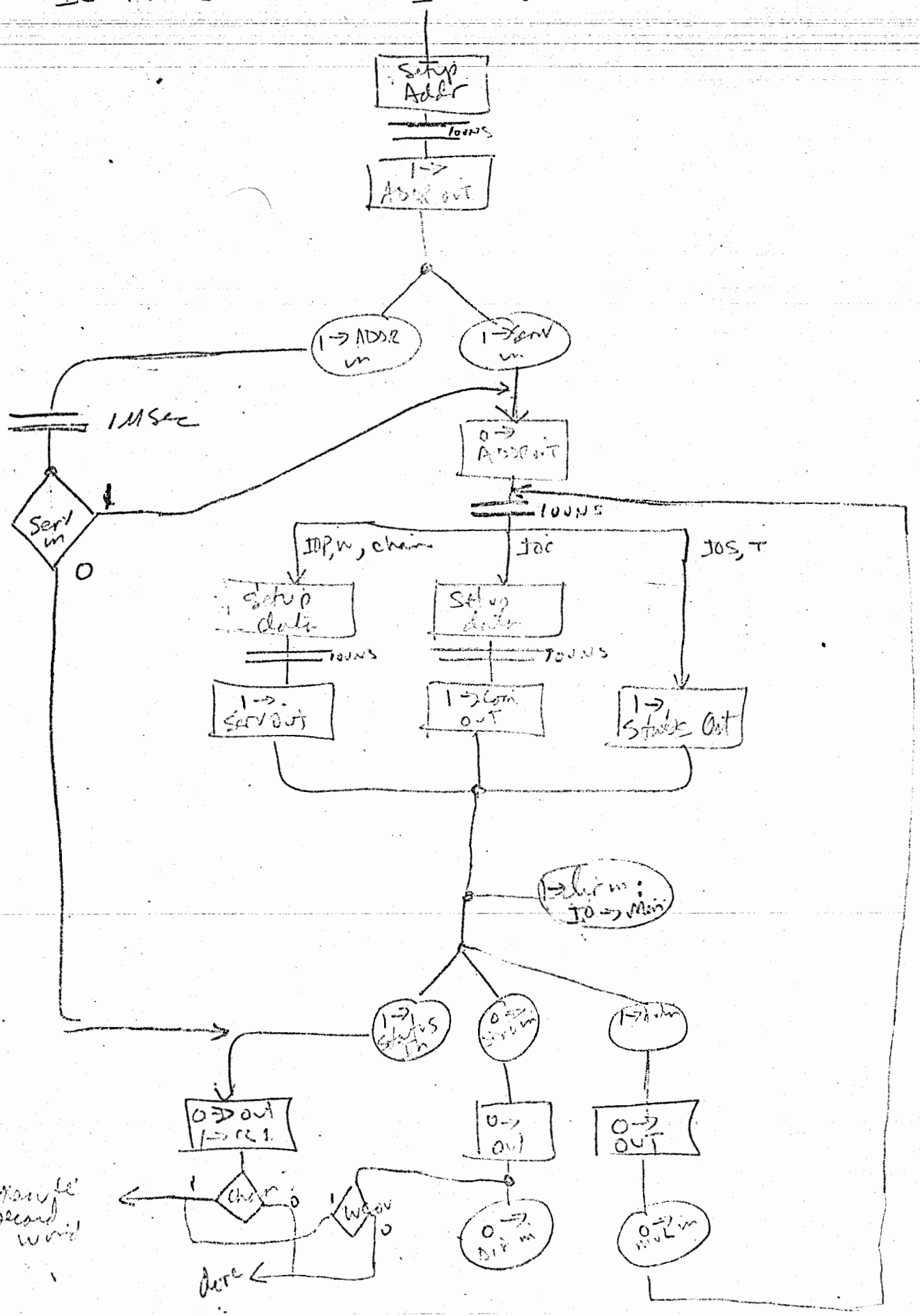
Line (direction)		function
Address	In	echo on Address Out, used to detect nonextant device; response to Select Out
Address	Out	selection code is on data lines, respond with Service In and become selected
Command	Out	command is on data lines, respond with Service In if acceptable; else, respond with Status In
Data 0	Out	data lines from processor to device controllers, also includes command specification and address
⋮		
Data 7	Out	
Data 0	In	data lines from device controller to processor, also includes status and address
⋮		
Data 7	In	
Direction	In	additional response to Service Out for to computer data transfer
Multiple	In	response to service out when additional byte is required
Operational	Out	system reset when down
Request 1	In	request to processor for attention at each of 3 priority levels (1 lowest, 3 highest)
⋮		
Request 3	In	
Service	In	drops as response to most Out signals, rises as response to Address In
Service	Out	accept or transmit data on data lines, respond by dropping Service In or raising Multiple In
Status	In	response to Command Out if unacceptable command
Status	Out	processor request for controller status, respond by sending status and raising Direction In
Select 1	Out	processor request for address from requesting device at the same priority leve. Select Out is propagated by those devices not requesting, blocked by the first device requesting, respond with Address In, send address on data lines
⋮		
Select 3	Out	

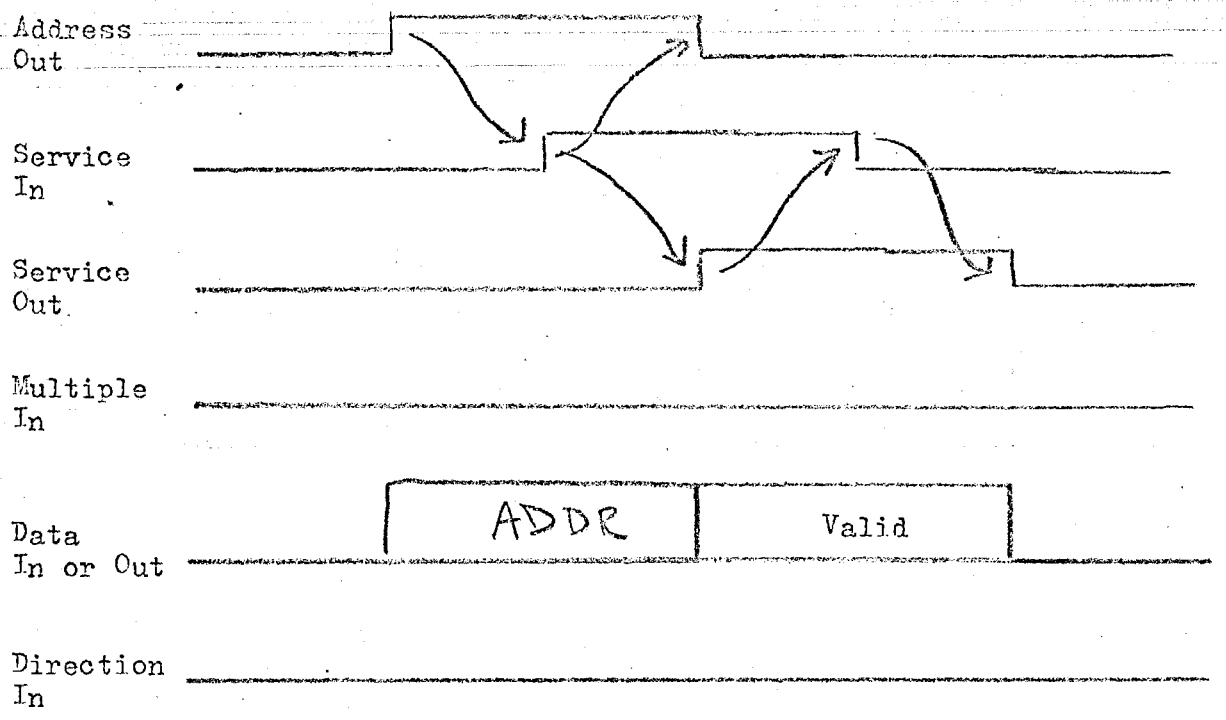
3.5 Bus flow diagrams

The following diagrams indicate signal timing relationships on the bus for various forms of transfer. Note that the only difference between read and write is the status of the Direction In bus line, that line solely determines the direction of transfer. Devices capable of both reading and writing have a status bit which determines the direction and use of the corresponding Direction In bus signal.

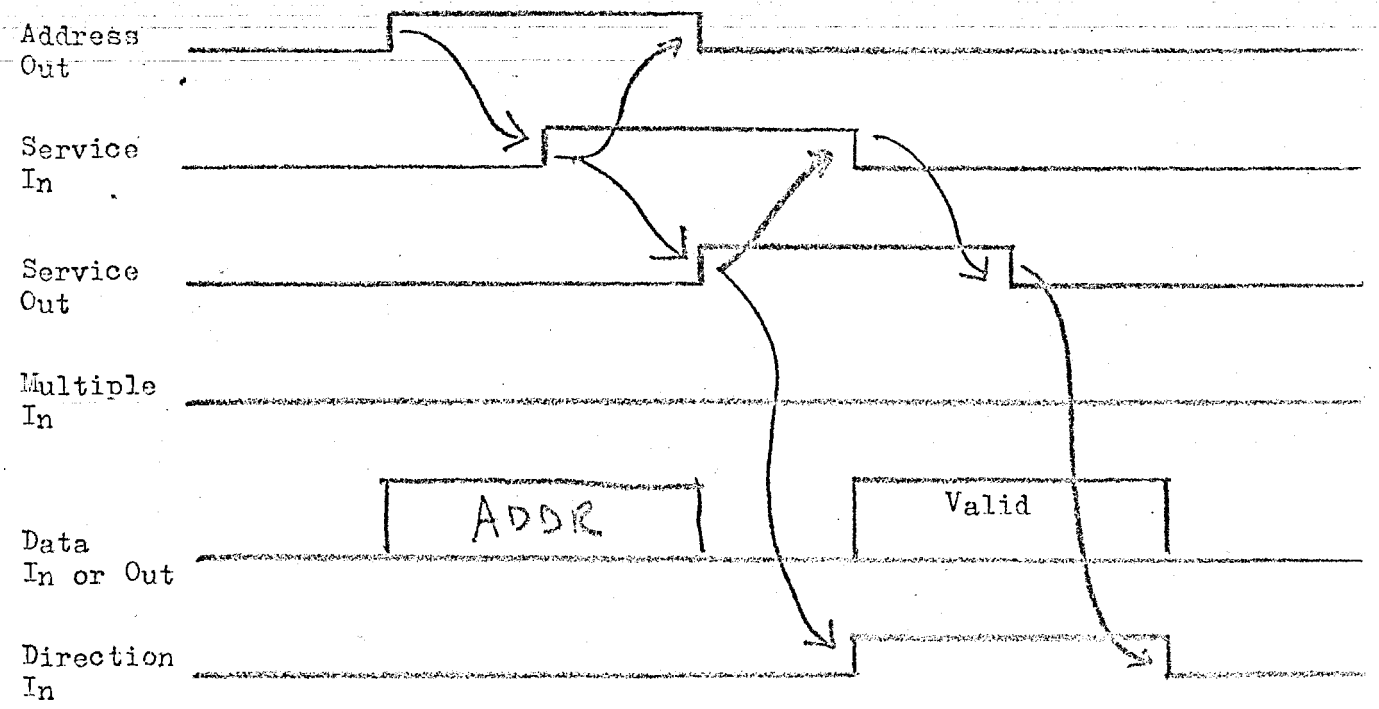
IO FLOW

IO inst

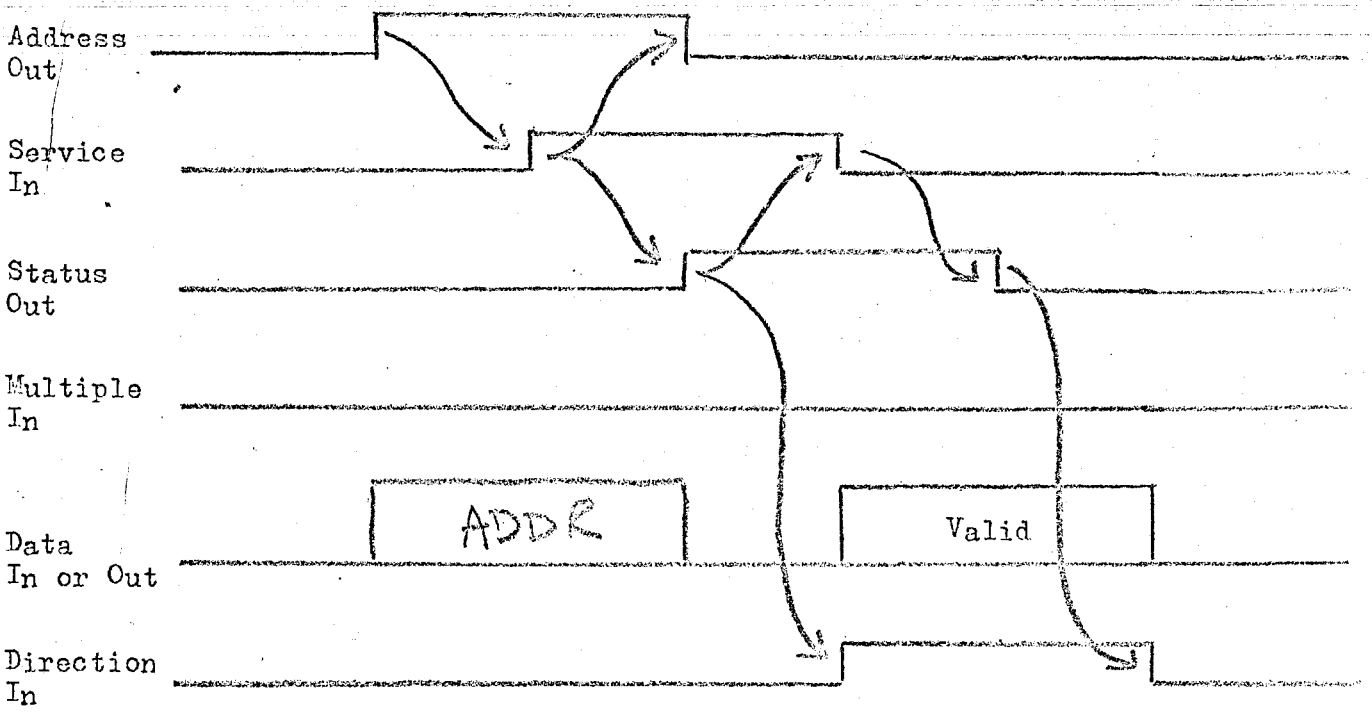




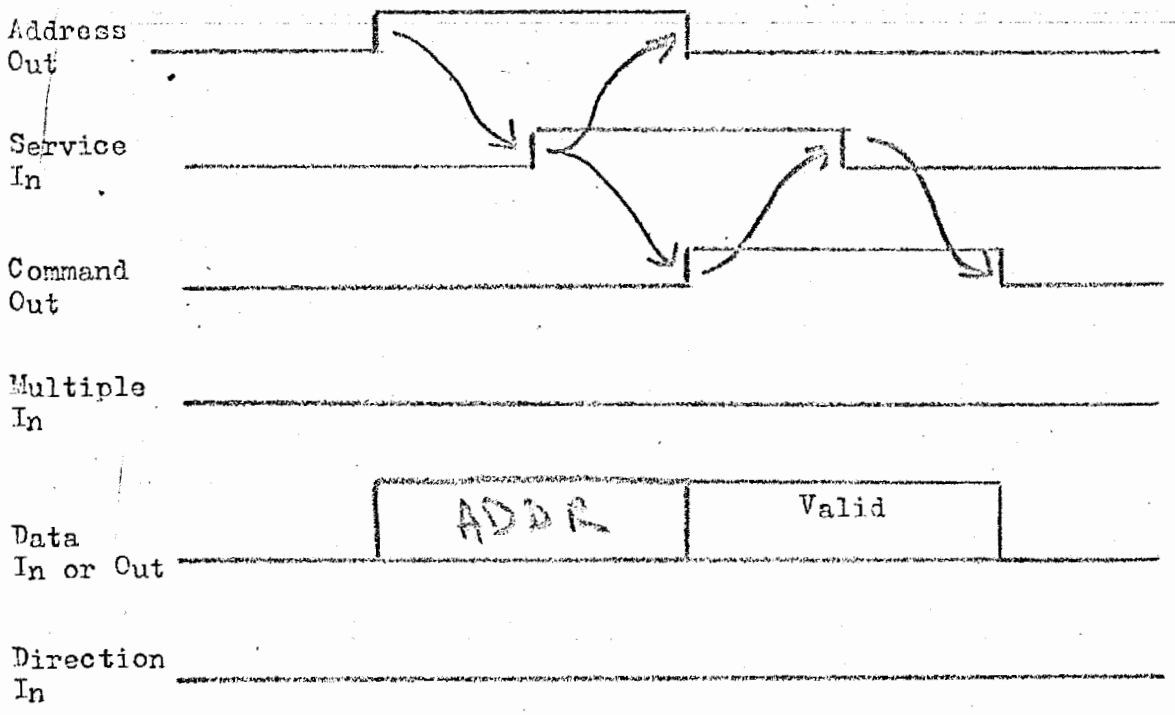
IOW Command operation sequence



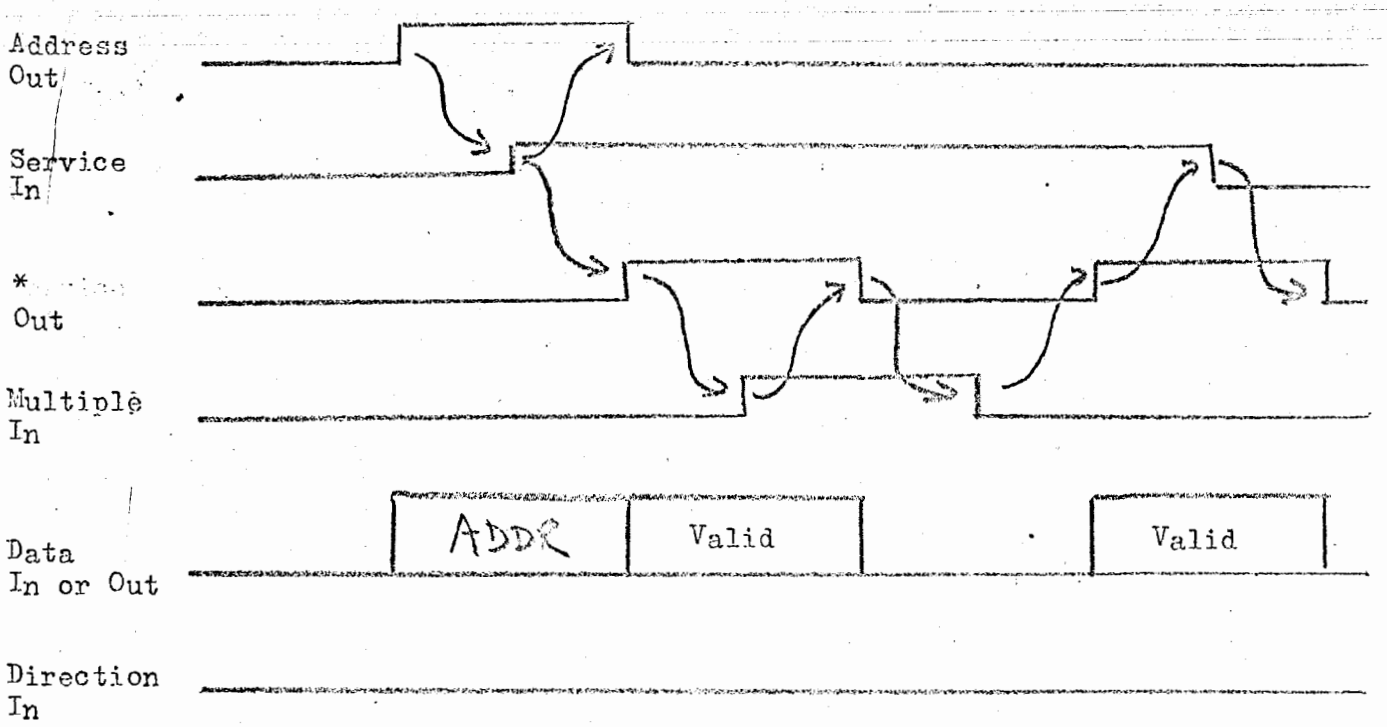
IOR Command operation sequence



IOT, IOS Command operation sequence

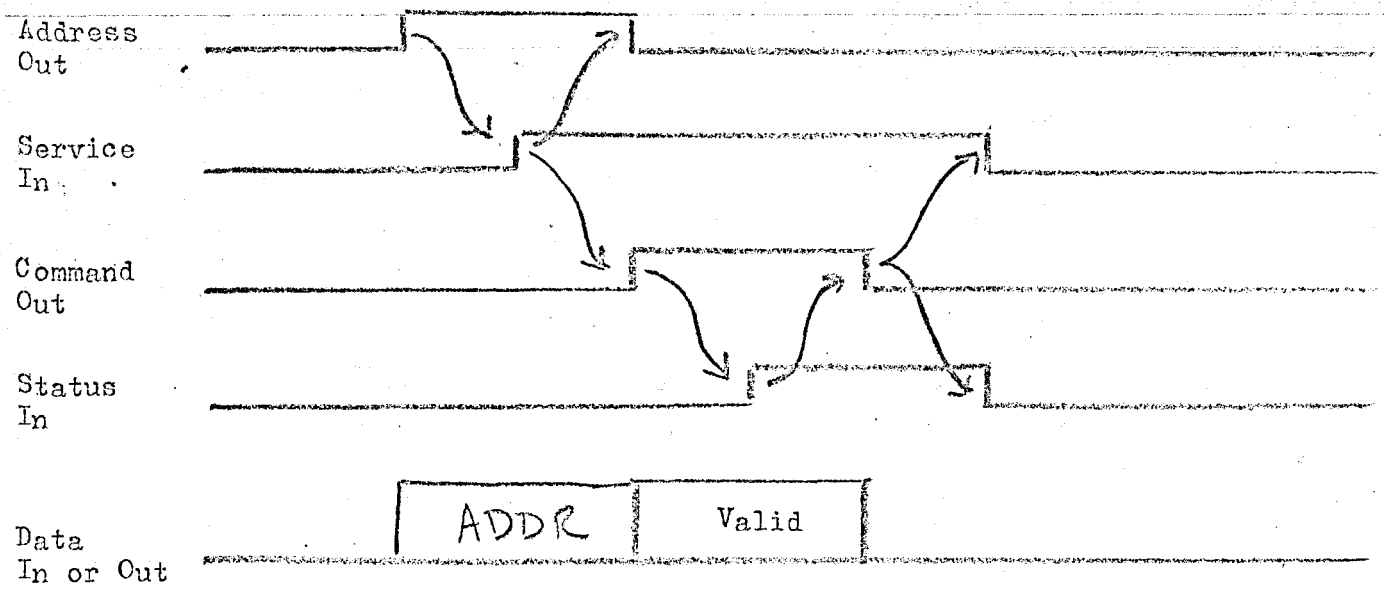


IOC Command operation sequence

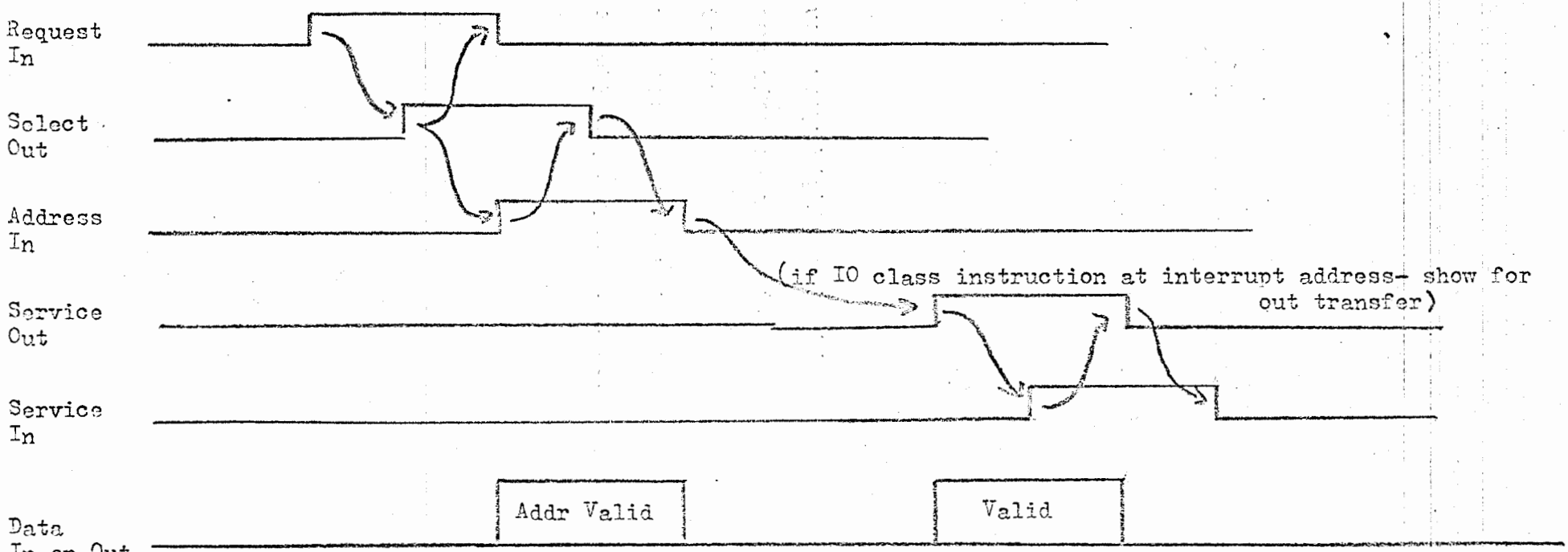


* Service, Command, Status

Multiple Byte transfer



Illegal Command operation sequence



Response to interrupt

1.0 Introduction

This document proposes a high speed, serial IO bus system in which 2 coaxial cables emanate in the processor and thread their way through all IO devices. The bus is broken (terminated, received, and retransmitted) in each device to establish priorities and to permit long lines without degrading the performance of physically close devices. All signal flow is syncronized to code blocks originating in the processor. The following are the major properties of the system:

1. Simple cabling - two single, simple coaxial cables with standard connectors are used.
2. High performance circuitry - since only 1 receiver and 2 transmitters are required at each device, it is economical to use very highly reliable, very high performance circuitry.
3. Information is transmitted in code blocks much as they are by teletype.
4. IO devices require a serial to parallel conversion buffer, some very high speed control logic, and the analog circuitry used in the receivers and transmitters. Much of this logic would be required in any bus system.
5. Multibus - since the bus itself is simple, devices may easily be interfaced to several. The intent is, partially, to facilitate expansion to multiprocessor systems without expensive crossbar switching systems.

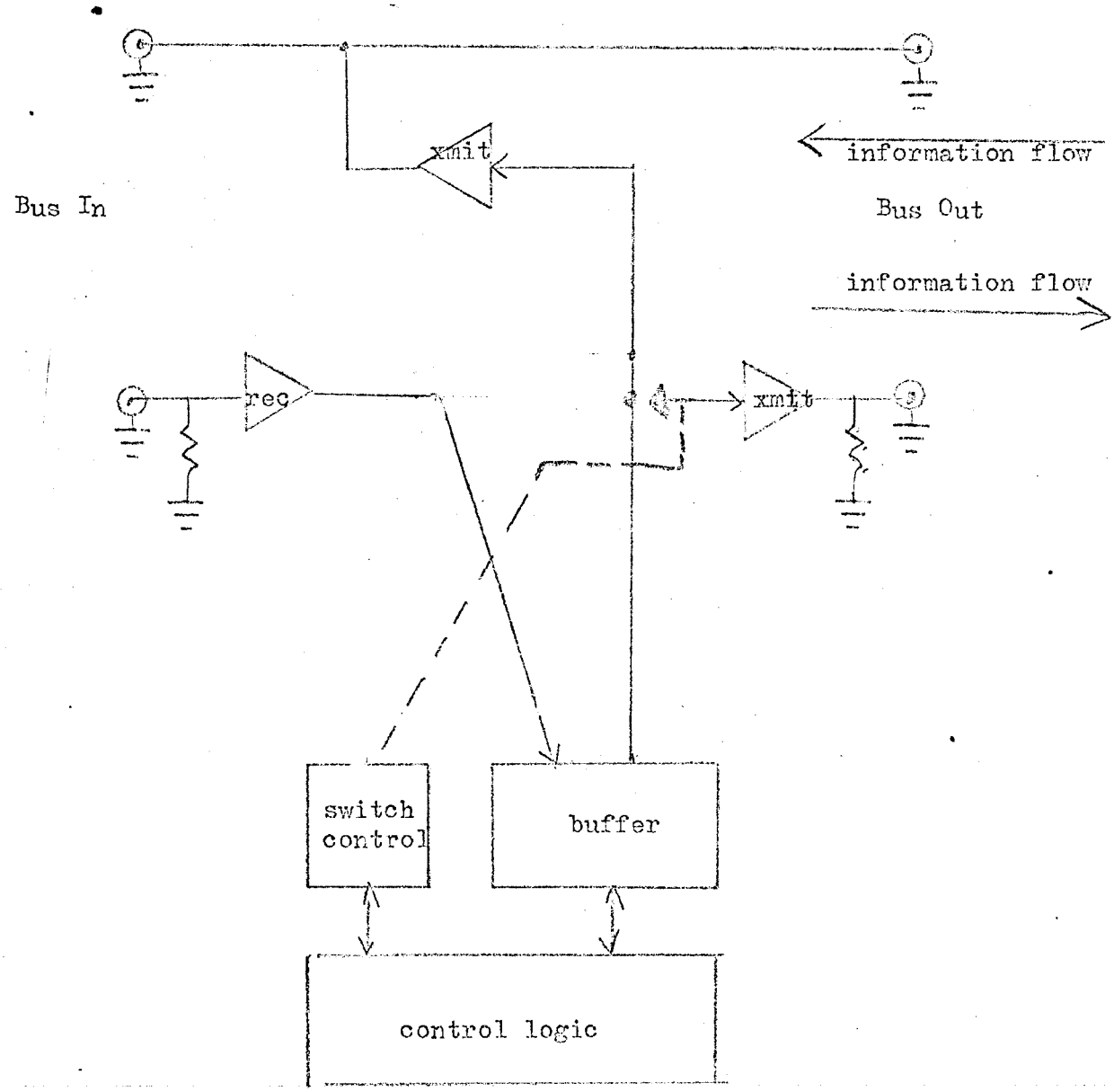
With a 50ns bit rate on the bus, a code block would require 0.8 usec for transmission. Round trip time through 20

devices and a total of 100' of cable yields a basic half cycle of 5 usec for the far devices and about 1 usec for the close ones. These are rates comparable to PDP-9.

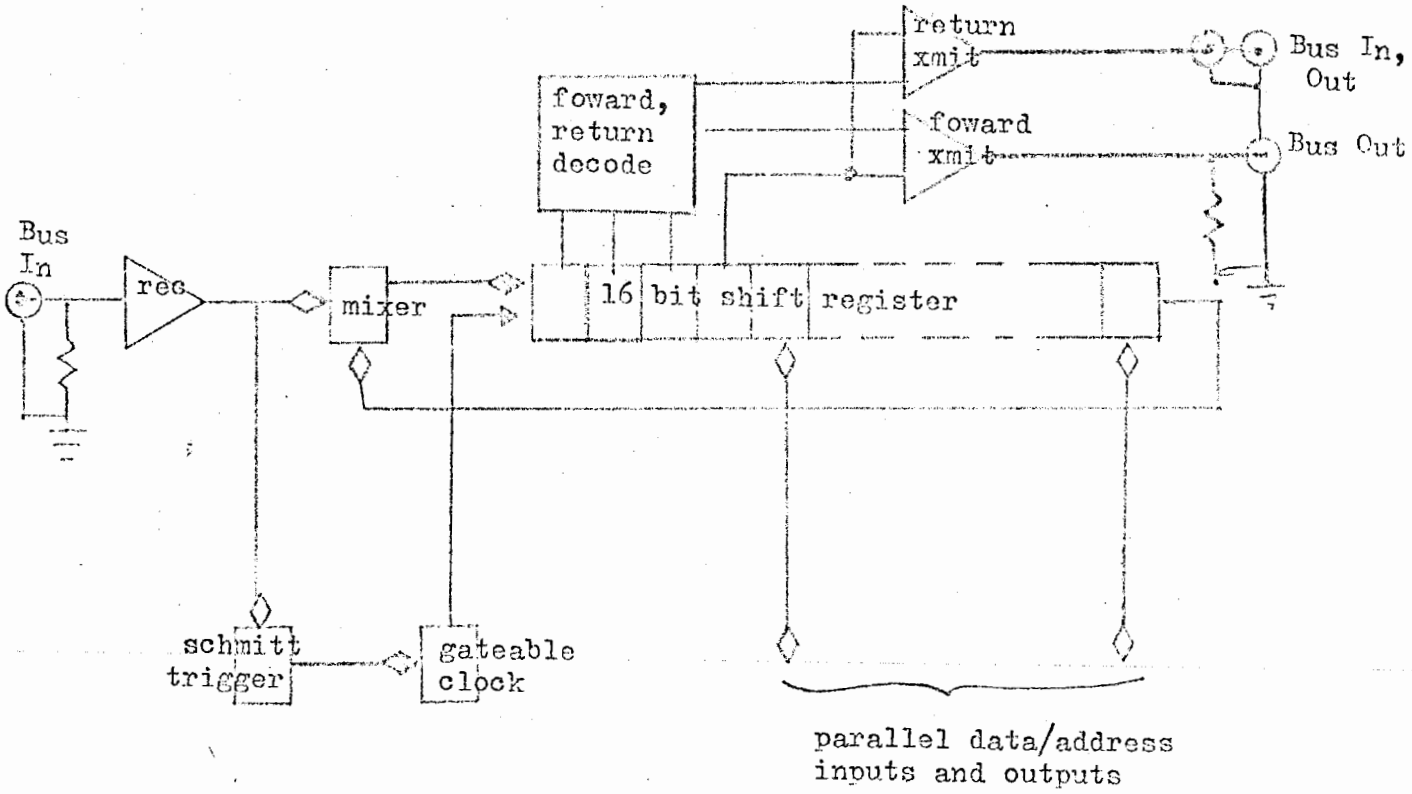
block length	.8
device delay 20x0.2	4.0
cable delay 100x0.002	.2
	5.0 usec

2.0 Basic device Hardware

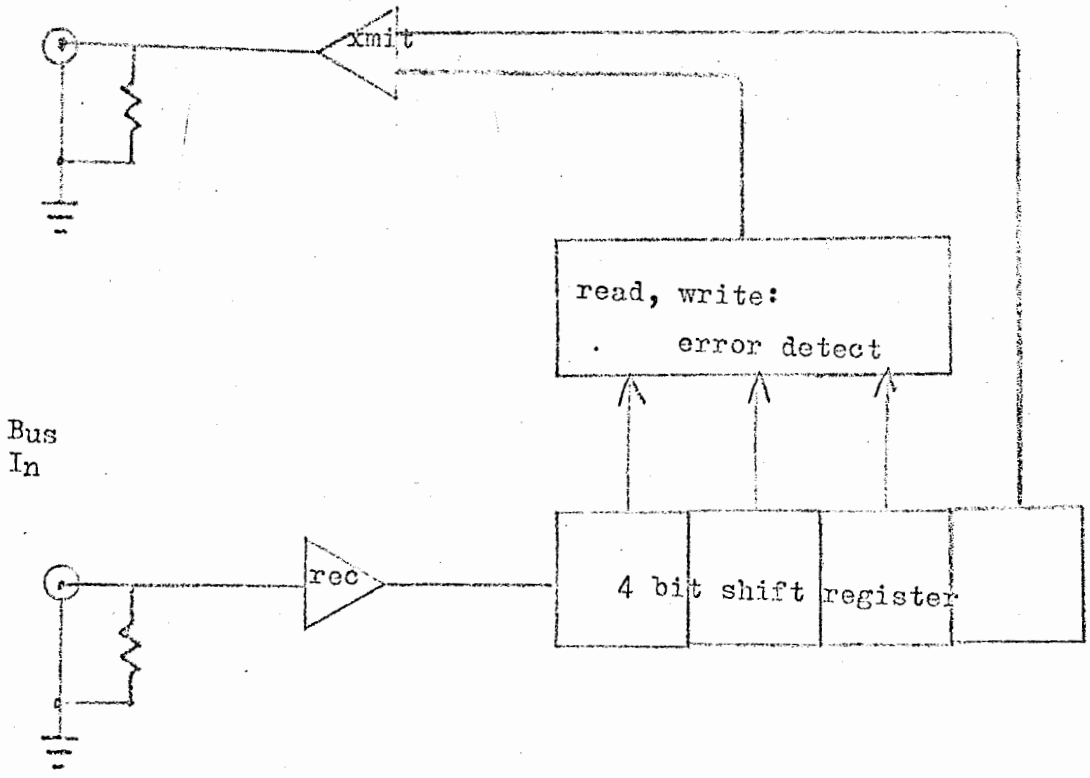
2.1 Block Diagram



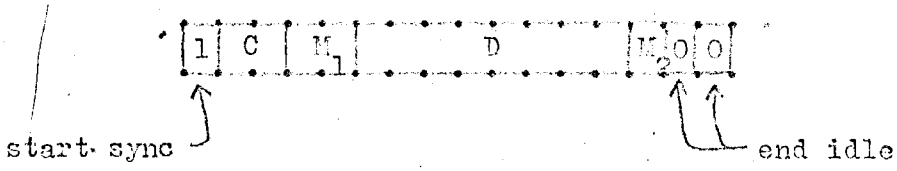
2.2 Control circuit details



2.3 Terminator



3.0 Code Format



C command type

M_1M_2 command mode

D data or address

3.1 Command types

0 Select - address follows, become selected if address match

1 Scan - processor looking for interrupt, send address

2 Read - selected device to send data

3 Write - selected device to accept data

3.2 Command mode

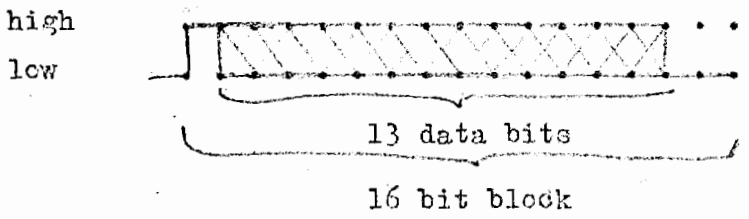
Mode is used as additional control information during read or write operations. Distinction is made between read/write status vs data, additional bytes, illegal commands, etc.

3.3 Data

Data bits transmit a byte of information or an address. On write operations they are supplied by the processor; on read they are inserted by the device.

4.o Bus signal electrical properties

The bus signal consists of a group of code bits spaced at 50ns intervals. The high state indicates a "1", the low state a "0". Rise and fall times are on the order of 10 ns.

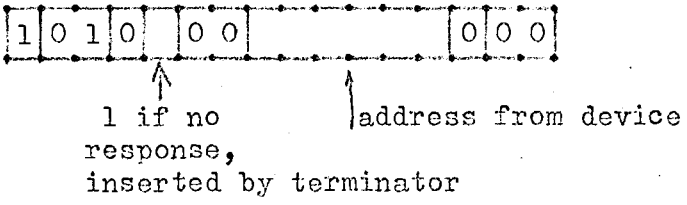


5.0 Basic operation

Devices receive a bit stream from the adjacent device, phase their internal clock to the start bit at the begining of the stream, and generally retransmit the stream to the next device after approximately 4 bits of delay time. Decoding the bit stream on Bus In may, however, result in a very different operation. In responding to a read command, for example, the selected device modifies the command string, appending its data bits, and sends it back along the second bus but does not foward it.

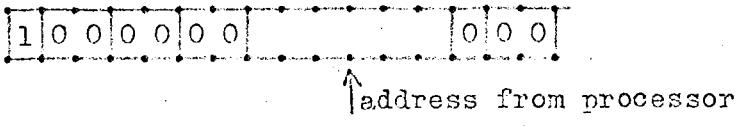
5.1 Scan operation

Whenever the computer interrupt system is on, the processor periodically issues scan sequences. When received by a requesting device, the sequence is modified to include the address of the requesting device and is transmitted back to the processor; it is not fowarded. The device address is mapped by the processor into an interrput address and the interrupt is processed. Scan sequence frequency is determined by bus length. The end of bus terminator returns the unacknowledged scan sequence. Internal request syscronization in each device is accomplished at the begining of each block.



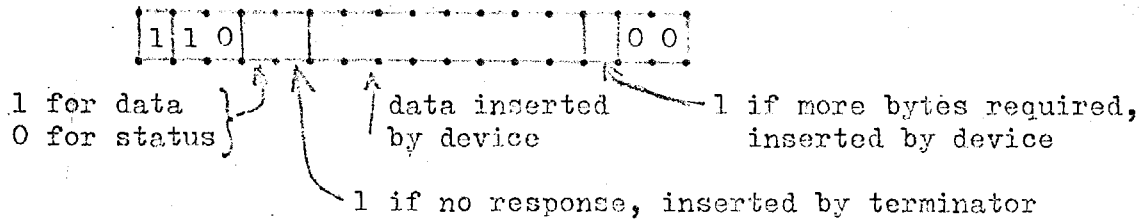
5.2 Selection Block

A selection block comprises the first part of a read or write operation. An address is transmitted to all devices, one of which responds to address match by setting an internal select flip flop. The sequence itself is retransmitted by each device to the next.



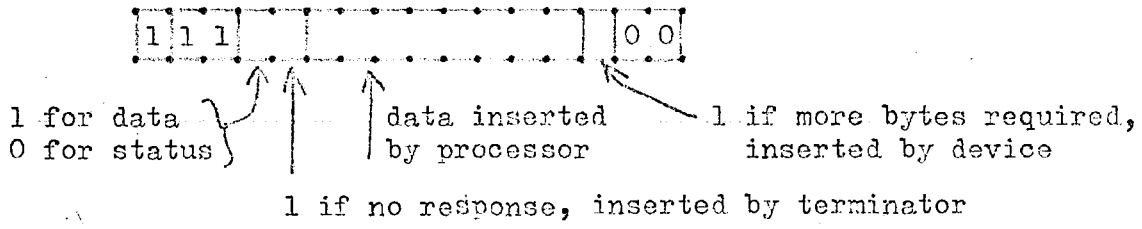
5.3 Read

A read block is initiated by the processor when it transmits a dummy data word. All non selected devices merely re-transmit forward the incoming sequence, the selected device does not forward the block, rather it inserts its byte to be read, necessary control information, etc. and returns it to the processor. If no device has been selected, the terminator will retransmit the block with an error indication.



5.4 Write

A write data or write status (command) operation begins with a selection block. The processor then transmits a write block which contains the data byte. The block is not forwarded but is retransmitted to the processor with any necessary control information. As in read, if no device has been selected, the terminator will retransmit the block with an error indicator.



PDP-X MEMORANDUM INDEX

digital INTEROFFICE MEMORANDUM

DATE: December 11, 1969

SUBJECT: **A Congeries on the Computer-in-the-home Market**

TO: **Operations Committee** FROM: **Gordon Bell**

cc: Jim **Bell**
Ad van de Goor
Larry Portner

This memo was triggered by a number of things, and the result will be semi-structural ramblings. The triggering events were:

1. **A discussion with Nick on it -- and a suggestion to jot down thoughts.**

2. **Seeing a DDP-316 computer being exploited by Neiman-Marcus for in the kitchen. (It doesn't do anything much, and if anyone of you has ever used a computer with only a Teletype for loading programs, you'll know it's useless.) Thus we'll do it right-er.**

3. **A lot of work at CMU on networks. Our present one is not way out enough to influence it, but I have students who are beginning to think about it. Thus, if you connect a computer to another iarger computer, you gain a lot.**

4. **I currently have a computer terminal in my home, and can't imagine not having one! Everyone says that you want large central machines -- I say no, why make the telephone company bigger (let's make IBM bigger). Organization theory works against the large central one.**

5. **The price trend. (The price is that of a car or 1/5~1/10 of a house.)**

6. **Looking at the computer-in-the-car market.**

7. I've **thought a lot about it; like all questionable ideas there comes a time to expose them.**

8. **Seeing the news releases on someone in Connecticut that bought an 8 for home.**

9. **They can conceivably be useful (in the Headstart sense) for teaching children.**

10. It **is a market of 50,000,000 +.**

11. It's **inevitable, so let's start now to get a headstart on the market.**

12. **I'm dedicated to bringing computers to the masses.**

What would it Do?

1. Teach (children)

   a. My 9 year old wrote an arithmetic program to teach the 6 year old addition and himself multiplication. (My 9 year old while thoroughly enjoyable has only a slightly above average IQ.)

   b. The 6 year old uses it as a desk calculator.

   c. The 9 year old learns about algorithms and is just getting the idea of a program. Aspires to write a tic-tat-toe playing program; only knows JOSS and Perlis's LCC. Prefers LCC because of language richness.

   d. Both children are learning to type.

   e. There are many "canned" teaching programs that can be useful. (arithmetic, spelling, word recognition .)

   f. In upper grades it could be useful for mathematics.

   g. Learn new computer and natural languages.

2. Self-improvement for adults

   a. Learn Programming. My wife is a typical PhD in the Social Sciences, and unlike her students who she can force to take computer programming courses, she learns at home. Other wives can learn programming and algorithms. This creates a source for programmers because the machine teaches programming. Life often becomes tolerable for people once they understand that a good model for most systems they encounter is a small (finite-state) machine. In short, things are pretty predictable.

   b. Learn new programming languages. I was recently forced into really learning LISP (I was teaching it) and it would have been impossible for me without a computer.

   c. Learn new skills. The use would be a typical teaching machine. These include foreign language, vocabulary, typing, accounting, mathematics, etc. These programs might be used in conjunction with a text.

   d. Correspondence courses.

   e. Learn typing.

3. The small home-based self-employed business. (This is a market unto itseif, and a fair dinkum product line in the DEC product line sense would be wise to start here because it's really sure fire.) This market includes doctors (who are inherently gadget-addicts and can afford to be), lawyers, etc. The computer is an expense, and with a minute amount of effort we can come up with tasks it can do to pay for itself. The following tasks are generally beyond the mental scope of the average professional (e.g. doctor).

a. Keep appointments

b. Write, bi ls

c. Keep inventory

d. Do taxes

e. Balance checkbook

f. Order processing

g. Letter filing

3A. DEC Salesmen. The kinds of tasks would be similar to 3 above. In addition a machine could take in the DEC daily expense sheets and produce the weekly voucher. Since this accounting system was designed to maximize the time spent by DEC secretaries, maybe we don't want to use a computer. On the other hand we could probably put the secretaries to work on something more useful like counting the supporting beams in the mill or something.

4. Play Games

a. Entertainment for simple games (e.g., my kids occasionally get me into a friendly game of monopoly. This is bad because I hate monopoly, and second, I can't play without winning.) Simple games like rummy, monopoly, etc. could be played in the teaching mode.

b. Teaching complex games - This is a bit far fetched for a small computer (e.g. my children use the Greenblatt chess program on the PDP-10, to improve their game.)

c. Poker - For the poker player, he can sharpen up.

d. Footbal l games, etc. The whole game market.

4A. Musical Instrument

5. Quantitative Analysis

a. Bookkeeping/budget/cash flow. (My wife took this problem as a vehicle to teach herself programming.) She wrote a program in which one enters monthly expenditures in about 20 categories and the program holds the data. It can be retrieved, summed over months, plotted (as bar graph) cash flow calculated, etc. She may incorporate checkbook control too. As a by-product, the data is all set to be used to make out the income taxes.

b. Income tax figuring . A good program would know the ways to help cut the tax for the user.

c. Stock portfolio analysis. For those who need it, such a program could be written.

d. Insurance - checking. (Get rid of those guys who sell insurance.)

e. Food buying. The user could give constraints, and a linear program could optimize the diet (e.g. so many turnips, pork, milk, etc.) and then proceed to plan menus. This program might need updating every 6 months for food costs. Food lists in terms of storing recipes and quantities - especially for parties.

f. Time analysis. For those concerned that they waste time, an analysis program could help them.

6. Filing/ Editing

a. Use for mailing list at Xmas time, print your own Xmas card labels.
b. Keeping phone numbers, addresses.
c. Keeping files of all collecting hobbies: stamps, shells, slides, etc.
d. Keeping personal library file
e. Keeping bibliographies
f. Doing indexes for books.
g. Holding and typing letters.
h. Memos, papers
i. Books (try one out with DEC tech writers)
j. Personalized letters to your Senator, Congressman, Governor, President, etc.

7. A Calendar

a. Anniversaries, birthdays
b. Appointments
c. Automatic reminders (baking, pick up children, etc.)

d. Day-to-day appointments.

e. Medical records - when children should be vaccinated and for what.

f. Remind me to put up storm windows, flush water softner, clean furnace filters, etc.

8. Control (These are a bit way out)

a. Furnace, air conditioning, climate control (many loops in a plant control sense). Close windows when it rains.

b. Burglar alarm - Sense inputs, call police, make sure doors are locked at night.

c. Run dishwasher or other device which have relatively complex time sequences.

d. Provide a control system for a constant-temperature-constant pressure water system (shower)

e. Control lights.

f. Private musak controlling with own choice.

9. Future

a. Play complex games - e.g. chess

b. Print ietters in the home. I would like to eliminate the post office, because it's getting senile. Also if we can have that money for a network, the network is more feasible.

c. Shopping in the home (from cable TV)

d. Print newspapers, too.

e. Order books, magazines, etc.

f. Scan periodical for keeping informed as to what to read.

What Would the Computer Look Like?

At least initially, I think the computer should be a fairly straightforward small computer. Eventually there should be scopes, but since the LINC's have never had hard copy, maybe you can get away with just scopes. It would have a keyboard, and probably hardcopy output. As an added bonus, an electric typewriter is a nice thing to have around the house. (preferably a Selectric) You might give the computer an extra connection to the phone line, so that when it got into trouble, it could call up the nearest large time-sharing computer to get help. (When it's trying to get most vitamins for the lowest cost in a diet.) Also , it seems absolutely necessary to have some form of low cost, but rather painless input media for new programs. The Cassette

cartridge looks great to me for this. Thus, we can visualize having something like a program of the month club to which the subscribers belong. It would not be a kitchen computer, ala Honeywell/Nieman-Marcus -- but a "family room" game room, study computer.

What Would the Software Look Like ?

For the kinds of programs we have been talking about I would strongly recommend that most programs be applications programs. In the cases where the user is learning about programming, it should be at a fairly high level.

In order to get lots of programs written, because variety will sell the deal, and also since some users would also write applications programs, the systems should be written at a very high level. I think FOCAL is almost at a high enough level, provided it has better string facilities, and the ability to work with files. On the bookkeeping program my wife wrote, it is only a page of code, and it has lots of string manipulation embedded in it. In the case of dedicated machines, and for the tasks we are talking about, the language can be very, very slow (interpretive) as long as it is powerful.

How to Proceed

There seems to be several ways one could proceed, all of which say we should spend sometime thinking a bit more before we act.

1. Just agree to spend some time thinking about the configurations, and then go on to write some of the basic software, and then distribute a number of computers to see how they would be used. Some machines could be either loaned or purchased by DEC employees, e.g. salesmen, engineers, programmers, technical writers. (I'm not volunteering yet).

2. Carry the idea forward a bit, get an approach, and then get a software company to get in bed and then try to peddle it. The software company really makes out in this deal, because it is sold like a record of the month club. (That's also appropriate to the people generating the software, because there could be glossy record-cover-like covers. Just picture for a minute a glossy photograph of Harris Hyman and his nimble coding pencil, as author of a Parcheesi program .)

3, I'd like to get somebody to work with me on this . . .

Now _____

Soon _____

Later _____

Never _____

(Check one.)

bwf

To: Ken Olsen and the Board of Directors
CC: Ed Kramer, Jack Shields, Jack Smith and Win Hindle

I would like to strongly recommend that we buy an interest in Trilogy for the following reasons:

1. We can build several, significant VAX products that offer a factor of 2 to 8 increase in performance times the machines we are introducing in the next two years. We have NO technology in house or in development that approaches this; we know of no technology that rivals this at IBM or in Japan.

   Nearly all of our customers require significantly more computing power, and the application of very large scale, high priced computing technology to minicomputers constitutes a major breakthrough in the design of minicomputers.

2. High performance, minicomputer-priced computers, coupled with our ability to interconnect machines would hold American Bell and other customers who may leave DEC for IBM. Just the announcement of our agreement may keep customers.

3. Minicomputers built with this mainframe technology will have an order of magnitude higher reliability, and as such, some may NEVER fail. Service cost, which constitutes half the total system cost is reduced a factor of two. Service is by simple replacement at the user's convenience.

4. The technology as a whole is a breakthrough, and forms the basis of both direct descendant technology and other systems:
   a. Their Computer Aided Design is the best we've seen. With it, designer productivity is an order of magnitude better than with our most advanced systems.
   b. Their mainframe design techniques are useful in minicomputers. We have already learned much from the Amdahls.
   c. The packaging and semiconductor technologies are state of the art, yet conservative, and extendable to another generation and probably lower cost machines. These technologies are coupled to the critical manufacturing processes development.
   d. The method for achieving reliability and obtaining higher yields through redundancy is truly unique, and a breakthrough. It goes directly to the ultimate goal of building a computer that will never fail. The current state of the art only permits the diagnosis of faults.

5. The technology is being developed by Gene Amdahl, who has built great high speed computers for the last 30 years.

6. We have able designers who want to start now.

Indeed, the only reason NOT to go with Trilogy is one of risk. We believe the risk is manageable, the people are the best, and our entry will increase their likelihood of success by additional resources and a different view.

We have the opportunity to participate in a breakthrough. Let's go.

Gordon Bell
19 June 1983

GENE M. AMDAHL, AGE 60

CHAIRMAN OF THE BOARD OF DIRECTORS, TRILOGY SYSTEMS

- PRIOR TO 1970, MANAGER OF ARCHITECTURE FOR THE IBM SYSTEM/360 AND DIRECTOR OF IBM'S ADVANCED SYSTEMS LABORATORY.
- LEFT IBM WHEN IBM DISCONTINUED DEVELOPMENT OF LARGE COMPUTERS.
- 1970 - FOUNDED AMDAHL CORPORATION TO DEVELOP POWERFUL COMPUTERS USING IBM SOFTWARE.
- 1975 - AMDAHL CORPORATION INTRODUCED ITS 470 COMPUTER LINE AND FOUNDED THE "PLUG-COMPATIBLE" INDUSTRY.
- 1976 - REVENUES AT AHDAHL WERE $93M, AND EARNINGS PER SHARE WERE $1.21.
- 1978 - REVENUES WERE $321M, EARNINGS PER SHARE OF $2.86. STOCK VALUE HAD INCREASED FROM $12 TO $71.
- IN THE COURSE OF FINANCING DEVELOPMENT OF AMDAHL CORPORATION'S PRODUCTS, FUJITSU LTD. AND HEIZER CORPORATION ACQUIRED LARGE BLOCKS OF STOCK. CURRENTLY THESE CORPORATIONS HOLD 33% AND 23% RESPECTIVELY. GENE AMDAHL'S EQUITY OWNERSHIP DROPPED TO ABOUT 5%.
- 1979 - LEFT AHDAHL CORPORATION. AMDAHL CORP. EARNINGS DROPPED TO $1.02 PER SHARE, REVENUES DROPPED TO $300M.
- SINCE 1979, AMDAHL CORP. EARNINGS HAVE BEEN NO HIGHER THAN $1.31 PER SHARE. REVENUES INCREASED TO $462M BY 1982.
- 1980 - TRILOGY FORMED.

FOUNDRY

OUR NEED:

LOW COST OF SUPPLY

THEIR GOALS

SECOND SOURCE OF SUPPLY

SELL LARGE CHIPS TO OTHER COMPANIES

TRILOGY/DIGITAL FOUNDRY PROPOSAL
STATEMENT OF DIRECTION

- TRILOGY WILL BUILD, STAFF, AND RUN A 10,000 WAFER START/MONTH MANUFACTURING FACILITY
- DIGITAL WILL FINANCE BUILDING, EQUIPMENT, AND STARTUP COSTS ($60M)
- TRILOGY WILL REPAY CAPITAL COSTS OVER 5 YEARS BEGINNING WHEN PRODUCTION BEGINS

- MODULE COST = ACTUAL COST + 25%
- DIGITAL'S CAPACITY = 6000 WAFER STARTS/MONTH

RISKS

- FORECASTING FLEXIBILITY
- MANUFACTURING YIELDS

ANOTHER APPROACH

ALTERNATIVE:

DIGITAL BUILD ITS OWN FAB FACILITY

REASONS NOT PREFERRED:

- DIGITAL DOES NOT HAVE A WEALTH OF BIPOLAR EXPERIENCE
- DIGITAL SEMICONDUCTOR EFFORT FOCUSED ON LOW COST TECHNOLOGIES
- EASIER FOR TRILOGY TO ATTRACT SEMICONDUCTOR PROFESSIONALS
- TRILOGY WILL HAVE FASTER YEILD ATTAINMENT

BACKUP

SLIDES

HIGH END STRATEGY

- A UNIQUE OPPORTUNITY

  TO HAVE A LEADERSHIP PRODUCT SET IN THE HIGH END VAX MARKETPLACE

- WE ARE ASKING FOR

  BOARD OF DIRECTORS SUPPORT OF PROPOSED STRATEGY

CURRENT TECHNOLOGY STRATEGY

- EVOLUTION OF VENUS SEMICONDUCTOR TECHNOLOGY
- DEVELOP NEW LIQUID COOLED PACKAGE

TRILOGY TECHNOLOGY STRATEGY

UNIQUE NEW CONCEPT:

- VERY LARGE CHIPS
- VERY HI DENSITY PACKAGE
- VERY HI RELIABILITY

To: Ken Olsen
CC: Ed Kramer, Jack Shields, Jack Smith and Win Hindle

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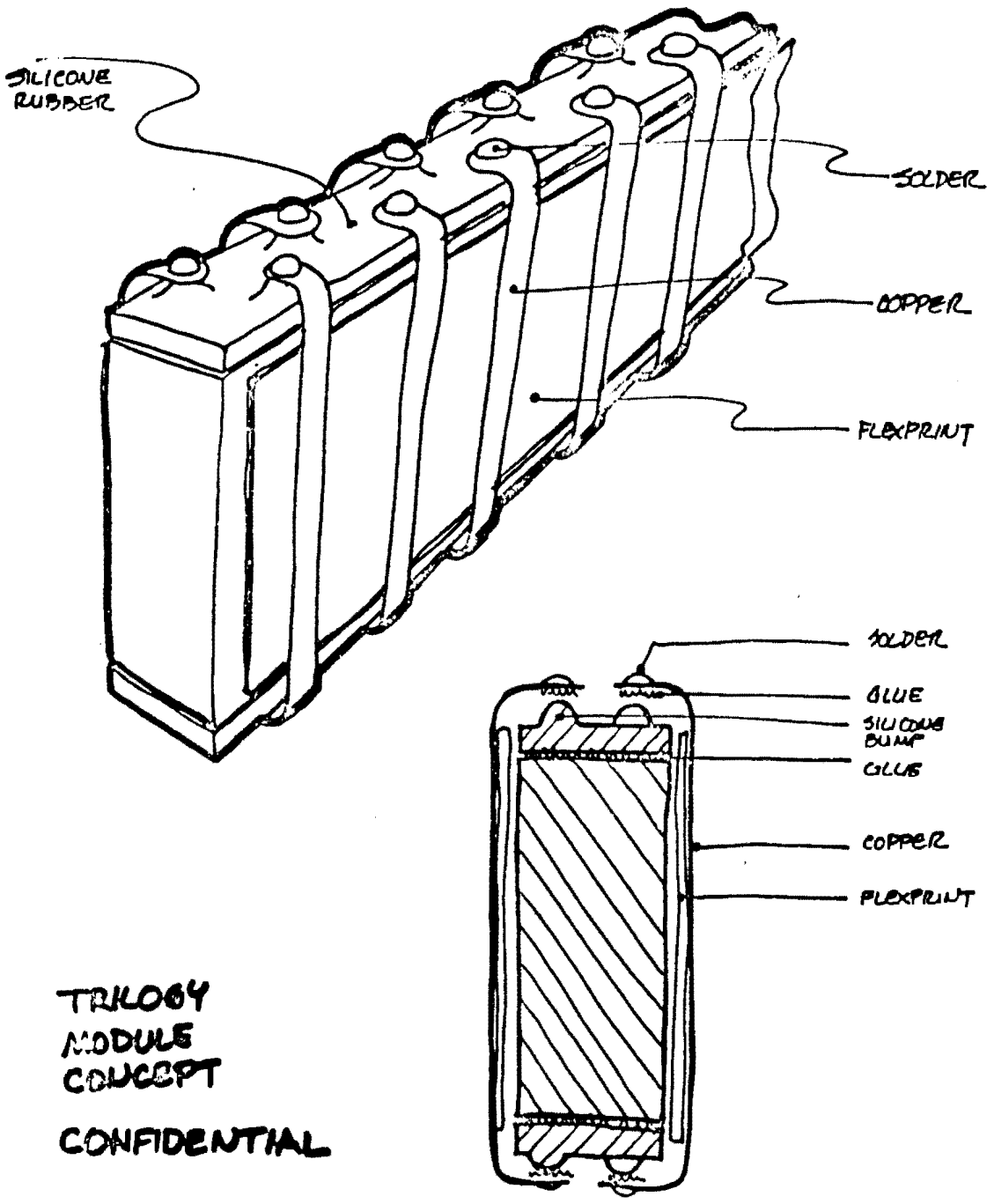


TRILOGY
MODULE
CONCEPT

CONFIDENTIAL

	CURRENT STRATEGY		PROPOSED STRATEGY	
	SYSTEM A	SYSTEM B	TRILOGY 1	TRILOGY 2
PERFORMANCE (X780)	*8	*15	12	25

*TARGET TECHNOLOGY NOT YET DEFINED

	CURRENT STRATEGY		PROPOSED STRATEGY	
	SYSTEM A	SYSTEM B	TRILOGY 1	TRILOGY 2
PERFORMANCE (X780)	*8	*15	12	25
NUMBER OF MODULES/WAFERS	**8**	**16**	**6**	**15**

*TARGET TECHNOLOGY NOT YET DEFINED

	CURRENT STRATEGY		PROPOSED STRATEGY	
	SYSTEM A	SYSTEM B	TRILOGY 1	TRILOGY 2
PERFORMANCE (X780)	*8	*15	12	25
NUMBER OF MODULES/WAFERS	8	16	6	15
PRODUCT COST (CPU - K$)	40	75	45	100

*TARGET TECHNOLOGY NOT YET DEFINED

	CURRENT STRATEGY		PROPOSED STRATEGY	
	SYSTEM A	SYSTEM B	TRILOGY 1	TRILOGY 2
PERFORMANCE (X780)	*8	*15	12	25
NUMBER OF MODULES/WAFERS	8	16	6	15
PRODUCT COST (CPU - K$)	40	75	45	100
FIRST SHIP	**FY87**	**FY87**	**FY87**	**FY87**

*TARGET TECHNOLOGY NOT YET DEFINED

FINANCIAL SUMMARY

	CURRENT STRATEGY	PROPOSED STRATEGY
DEVELOPMENT COSTS (FY84-FY91)	$150.0M	$128.0M
FOUNDRY COSTS		60.0M
TECHNOLOGY PURCHASE		26.0M
SIZE OF MARKET (FY87-FY90)		
250K-625K PRICE RANGE	$10.1B - 15.9B	$10.1B - 15.9B
625K-1.6M PRICE RANGE	$ 5.0B - 6.3B	$ 5.0B - 6.3B
MARKET SHARE (FY87-FY90)		
250K - 1.6M PRICE RANGE	10 - 11%	10 - 16%
UNITS SHIPPED RANGE OF	11000 - 17000	14000 - 20000
FY87 TO FY92 ANALYSIS BASED UPON	15000	16000
REVENUE		
FY87 TO FY92	$ 6.5B	$ 8.0B
PRESENT VALUE CASH FLOWS @ 40%	($ 5.0M)	$25.0M
OPERATING PROFIT BEFORE TAX	$ 2.0B 28% OF NOR	$ 3.0B 34% OF NOR

ANALYSIS ASSUMES SALES PRICE OF STOCK IN 1992 IS SAME AS PURCHASE PRICE IN 1983. IF TRILOGY IS SUCCESSFUL, THE STOCK OFFERS A PROFIT POTENTIAL

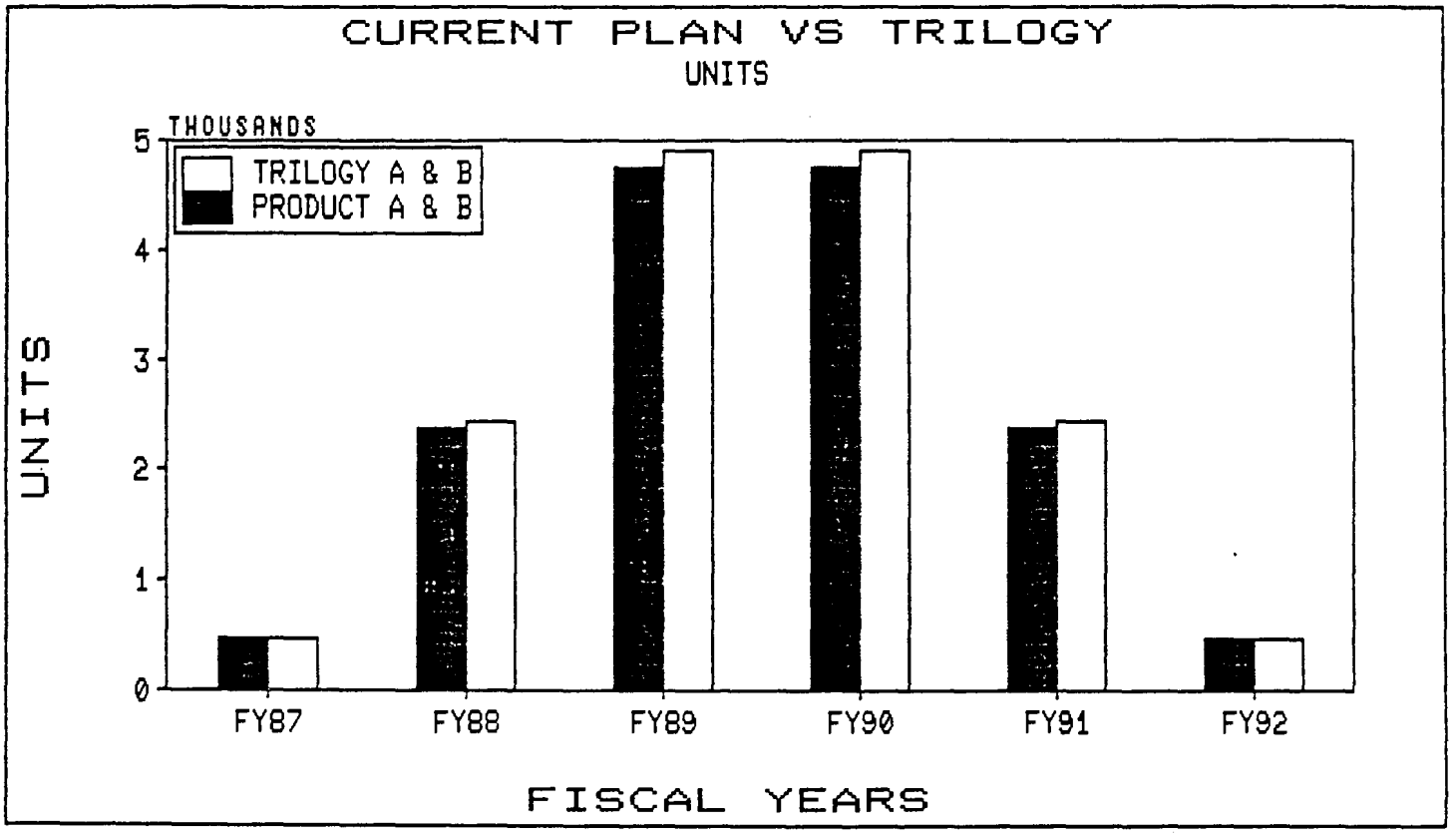
ENGINEERING COSTS

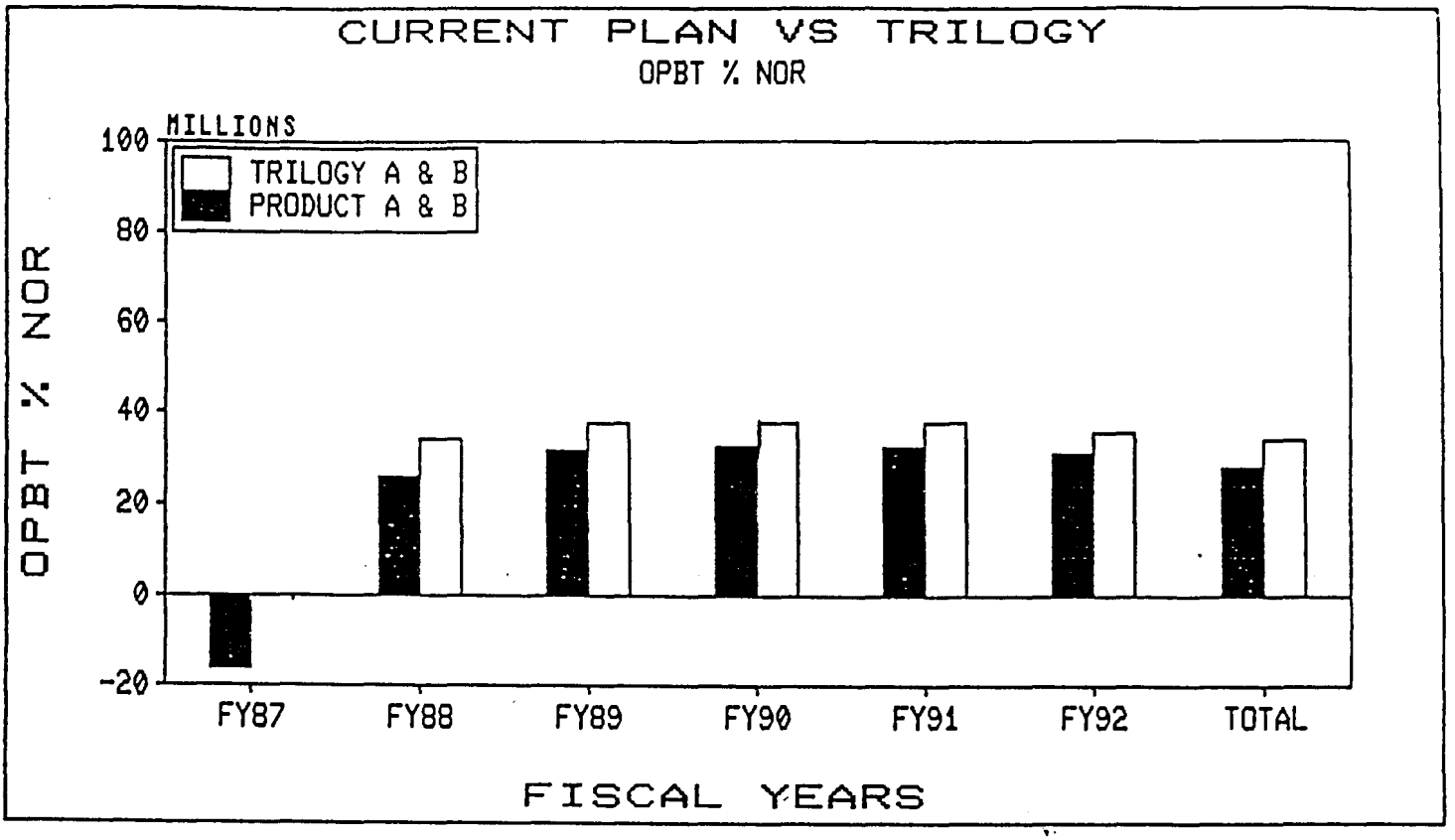
$M

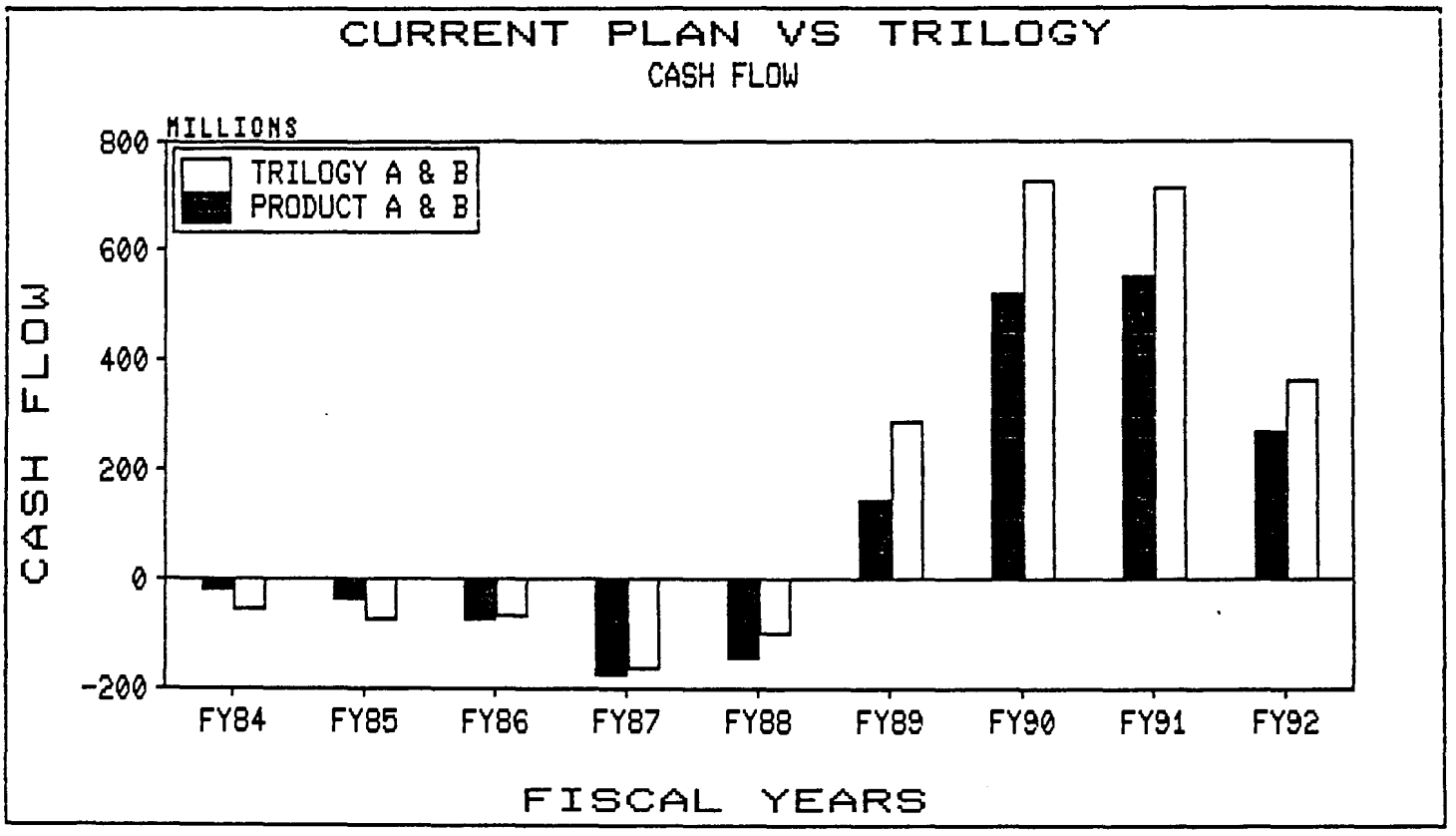
	CURRENT STRATEGY	PROPOSED STRATEGY*
FY1984	9	14
FY1985	23	27
FY1986	36	36
FY1987	29	27
FY1988	23	13
FY1989	17	6
FY1990	9	3
FY1991	4	2
TOTAL	150	128

*CAD ASSUMPTIONS BASED UPON TRILOGY'S PLANNING METRICS

ENGINEERING COSTS REPRESENT CPU DEVELOPMENT AND SYSTEM TEST.


CURRENT PLAN VS TRILOGY
UNITS
THOUSANDS
TRILOGY A & B
PRODUCT A & B
UNITS
5
4
3
2
1
0
FY87
FY88
FY89
FY90
FY91
FY92
FISCAL YEARS


CURRENT PLAN VS TRILOGY
OPBT % NOR
MILLIONS
100
80
60
40
20
0
-20
TRILOGY A & B
PRODUCT A & B
OPBT % NOR
FY87
FY88
FY89
FY90
FY91
FY92
TOTAL
FISCAL YEARS


CURRENT PLAN VS TRILOGY
CASH FLOW
MILLIONS
800
600
400
200
0
-200
TRILOGY A & B
PRODUCT A & B
CASH FLOW
FY84
FY85
FY86
FY87
FY88
FY89
FY90
FY91
FY92
FISCAL YEARS

TRILOGY FINANCING

EQUITY AND INCOME TO DATE:

1980	LIMITED PARTNERSHIP	$55.0M
1980	SALE OF STOCK	$1.5M
1981	SALE OF STOCK	$26.7M
1982	SALE OF STOCK	$23.8M
TO DATE INTEREST EARNED ON CAPITAL		$15.0M

OTHER FINANCING

IRISH GRANTS AND FINANCING TO BE RECEIVED	$18.0M
RENTAL OF CUPERTINO FACILITY	$20.0M
NET EQUIMENT LEASES AND LOANS	$27M
TOTAL EQUITY, INCOME AND FINANCING	$187.0M

TRILOGY'S CASH NEEDS
TO COMPLETE THE PROJECT

CASH NEEDS	$ MILLION
CASH AVAILABLE AS OF OCTOBER 1, 1983	0
CASH FLOW PRIOR TO FIST SHIPMENT (MARCH 1, 1985)	
1983 (LAST 3 MONTHS)	10
1984 (12 MONTHS)	70
1985 (FIRST 2 MONTHS)	15
	95
POST-FIRST SHIP WORKING CAPITAL - UNTIL BREAKEVEN	35
PROJECTED NEEDS	**130**

CASH SOURCE (TRILOGY PLAN)	
SPERRY	42
ADDITIONAL FINANCING FROM CURRENT INVESTORS	16
DIGITAL	26
PUBLIC OFFERING	80 - 100
SOURCES	**164 - 184**

EXCESS FUND TO COVER UNEXPECTED NEEDS	**34 - 54**

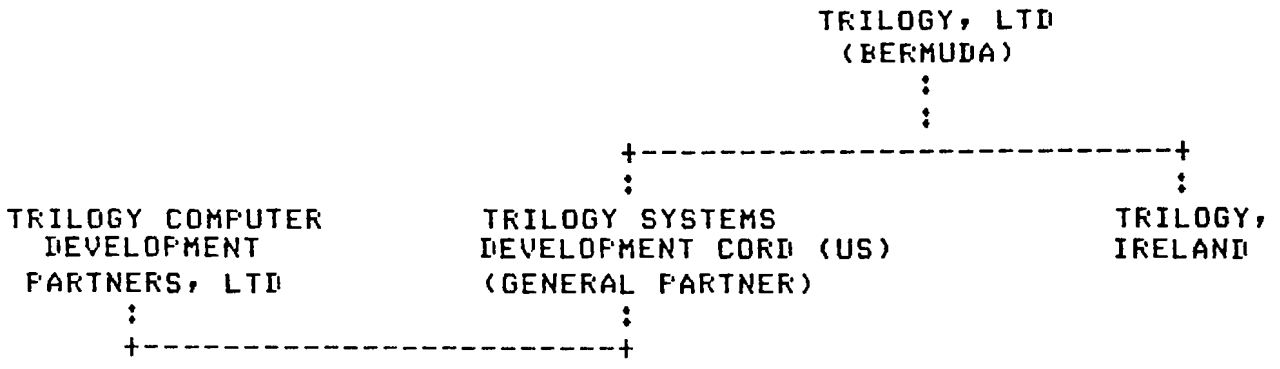
INVESTOR EQUITY

(000,000'S OMITTED)

	$	SHARES	%*
AS OF 6/27/83			
PRINCIPALS & OPTIONS	0	18.9	36.1
CII - HONEYWELL - BULL	13	2.3	4.4
BANK OF AMERICA	10	2.0	3.8
IVORY - SIME	10	2.0	3.8
DEVELOPMENT CAPT CORP	5	.8	1.5
AETNA	3	.5	1.0
OTHERS	11	1.7	3.3
IDA COMMITMENT @ $5.00	0	.2	.4
	52	28.4	54.3
SPERRY	40	5.0	9.6
	92	33.4	63.9
ADDITIONAL 1983			
DIGITAL	24	3.0	5.7
OTHER	16	2.0	3.8
STOCK BUYOUT OF R&D PARTNERSHIP	0	6.9	13.2
PUBLIC OFFERING	100	7.0	13.4
	232	52.3	100

* % ARE BASED UPON ANTICIPATED NUMBER OF SHARES OUTSTANDING AFTER THE PUBLIC OFFERING

Trilogy Structure



- Trilogy, Ltd - Bermudian parent company. Owns exculsive option to acquire technology and product from Trilogy Computer Development Partners Ltd. (The Partnership).
- Trilogy Systems Development Corporation - U.S. subsidiary of Trilogy Ltd. will perform research, for a fee, for The Partnership.
- Trilogy, Ireland - Irish subidiary of Trilogy, Ltd. which will purchase U.S. made "big chips" and perform systems integration. The company has an Irish tax exemption through 1990.
- Trilogy Computer Development Partners, Ltd. - Trilogy Systems is the general partner with some 4,600 limited partners. The Partnership was brokered by Merrill Lynch & Co.. The Partnership has contracted with Trilogy Systems for research and development.

RELATIONSHIP BETWEEN THE PARTNERSHIP AND THE TRILOGY GROUP

I. TRILOGY SYSTEMS RECEIVES:

- o REIMBURSEMENT OF RESEARCH AND DEVELOPMENT COSTS. CAPITAL COSTS ARE BORNE BY TRILOGY SYSTEMS.
- o MAXIMUM FUNDING - $55M.

II. THE PARTNERSHIP RECEIVES:

- o EXCLUSIVE WORLD-WIDE RIGHT TO USE THE TECHNOLOGY DEVELOPED BY TRILOGY SYSTEMS.

III. TRILOGY LTD. RECEIVES:

- o AN OPTION TO REACQUIRE ALL RIGHTS IN THE TECHNOLOGY GRANTED TO THE PARTNERSHIP.
- o COST OF OPTION EXERCISE.
  - ROYALTIES OF 7 7/9% OF REVENUE TO $111,111,111 REACHED. LESS AFTER THAT

    OR
  - LUMP-SUM OF GREATER OF $222,222,222 LESS ROYALTIES PAID OR $111,111,111 CASH.
  - PARTNERSHIP MAY ELECT TO RECEIVE 6,944,444 SHARES OF TRILOGY COMMON STOCK IN LIEU OF A CASH LUMP-SUM PAYMENT.

GENE M. AMDAHL, age 59

Chairman of the Board of Directors, Trilogy Systems and Storage Technology.

- Prior to 1970, Dr. Amdahl was employed by IBM as Manager of Architecture for the IBM System/360 and Director of IBM's Advanced Systems Laboratory.
- Left IBM when IBM discontinued development of large computers.
- 1970 - Founded Amdahl Corporation to develop more powerful computers than IBM high end equipment, but using IBM software and operating systems.
- 1975 - Amdahl Corporation introduced its 470 computer line and founded the "plug-compatible" industry.
- 1976 - Revenues at Amdahl were $93 M, and earnings per share were $1.21.
- 1978 - Revenues were $321 M, earnings per share of $2.86. Stock value had increased from $12 to $71.
- In the course of financing development of Amdahl Corporation's products, Fujitsu Ltd. and Heizu Corporation acquired large blocks of stock. Currently these corporations hold 33% and 23% respectively. Gene Amdahl's equity ownership dropped to about 5%.
- 1979 - Left Amdahl Corporation. Amdahl Corp. earnings dropped to $1.02 per share, revenues dropped to $300 M.
- Since 1979, Amdahl Corp. earnings have been no higher than $1.31 per share. Revenues increased to $462 M by 1982.
- 1980 - Trilogy formed.

D I G I T A L H I G H
E N D V A X
S I R A I E G Y

PRESENTATION TO BOARD
OF DIRECTORS

JUNE 27, 1983

THE TRILOGY OPPORTUNITY

- OPPORTUNITY TO HAVE LEADERSHIP PRODUCTS AT THE HIGH END OF THE VAX FAMILY IN THE 1986-90 TIMEFRAME.

- OPPORTUNITY TO EXPLOIT FUTURE ENHANCEMENTS TO THIS UNIQUE TECHNOLOGY TO MAINTAIN VAX LEADERSHIP IN THE HIGH END INTO THE 1990'S.

- OPPORTUNITY TO EXPLORE THE USE OF THE TECHNOLOGY IN OTHER SYSTEMS ARCHITECTURES AND APPLICATIONS.

- OPPORTUNITY TO LEARN TECHNIQUES FOR THE DESIGN OF HIGH PERFORMANCE SYSTEMS.

- OPPORTUNITY TO LEARN TECHNIQUES FOR THE DESIGN OF HIGHLY RELIABLE SYSTEMS.

- OPPORTUNITY TO BEGIN INSTANT USE OF AN ESTABLISHED DESIGN PROCESS.

- OPPORTUNITY TO CONSIDER WAFER SCALE INTEGRATION CONCEPTS IN OTHER SEMICONDUCTOR TECHNOLOGIES.

THE DOWNSIDE

NOMINAL WORST CASE -- BASED UPON OUR TECHNICAL ASSESSMENT

INITIAL INVESTMENT - $26M

WORSE CASE DELAY TO TECHNICAL DEV - 1 YEAR

EFFECT: DELAY DIGITAL PRODUCT DEVELOPMENT 6 MONTHS
TRILOGY MIGHT REQUIRE $10-20M

IMPACT: SMALL IMPACT ON OVERALL NEW BUSINESS PLAN

ABSOLUTE WORST CASE

WE CONCLUDE IN 18 MONTHS THE TECHNOLOGY IS NOT MANUFACTURABLE.

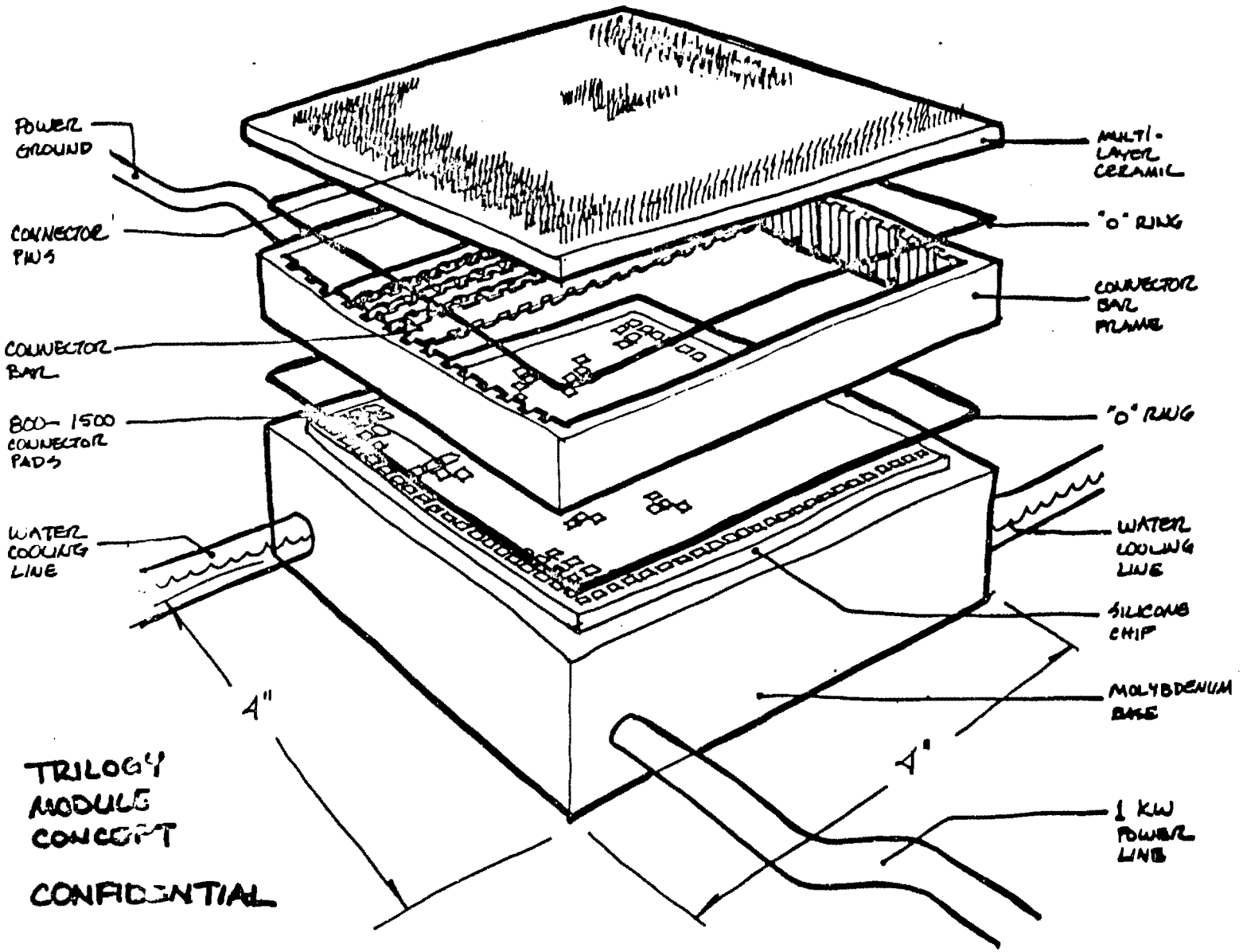
EFFECT: DELAYS DIGITAL'S CURRENT STRATEGY BY ONE YEAR

IMPACT: SIGNIFICANT IMPACT ON OUR CURRENT BUSINESS PLAN

RISK SUMMARY

- THE TRILOGY TECHNOLOGY IS A MAJOR TECHNICAL BREAKTHROUGH WITH $100M OF DEVELOPMENT ALREADY INVESTED IN IT AND WITH A FINITE RISK OF FAILURE.

- THE DIGITAL ALTERNATIVE IS A SMALLER EVOLUTIONARY STEP THAT HAS HAD RELATIVELY LITTLE EFFORT APPLIED TO IT, AND WILL LIMIT THE UPPER RANGE OF SYSTEMS DIGITAL CAN OFFER. IT SHOULD HAVE A LOWER TECHNICAL RISK AND HIGHER TIME TO MARKET RISK.


POWER GROUND
CONNECTOR PINS
CONNECTOR BAR
800–1500 CONNECTOR PADS
WATER COOLING LINE
4"
4"
MULTI-LAYER CERAMIC
"O" RING
CONNECTOR BAR FRAME
"O" RING
WATER COOLING LINE
SILICONE CHIP
MOLYBDENUM BASE
1 KW POWER LINE
TRILOGY MODULE CONCEPT
CONFIDENTIAL

	CURRENT STRATEGY		PROPOSED STRATEGY		
	SYSTEM A	SYSTEM B	TRILOGY 1	TRILOGY 2	
	4-5				
PERFORMANCE (X780)	*8	*15	12	25	32
NUMBER OF MODULES/WAFERS	8	16	6	15	
	(25-40)				
PRODUCT COST (CPU - K$)	40	75	45	100	
FIRST SHIP	FY87	FY87	FY87	FY87	
MARKET POSITION	**COMPETITIVE**		**LEADERSHIP**		

*TARGET TECHNOLOGY NOT YET DEFINED

THE OVERALL COMPETITIVE PICTURE

TECHNICAL BASE	POTENTIAL COMPETITOR	ASSESSMENT RELATIVE TO TRIL VAX
THERMAL CONDUCTION	IBM	GREATER NO OF INTERCONNECTS REQ'D
TRILOGY TECHNOLOGY	SPERRY, HONEYWELL	SYS ARCH NOT COMPETITIVE
OTHER TECHNOLOGY	HP, PRIME, SEL	NOT ABLE TO ACHIEVE EQUIV PERF
TRILOGY TECHNOLOGY	TRILOGY	CURRENT FOCUS AT VERY HIGH END

NET ASSESSMENT: TRILOGY TECHNOLOGY VAXs WILL BE LEADERSHIP PRODUCTS

THE PROPOSAL

EQUITY INVESTMENT IN TRILOGY

3 * MILLION SHARES @ $8.00	=	$24,000,00

CASH

$2,000,000 LICENSE FEE FOR RIGHT TO TECHNOLOGY	=	$2,000,000
		$26,000,000

* DIGITAL HAS THE OPPORTUNITY TO BUY UP TO 5M SHARES

WHAT DIGITAL GETS

- RIGHTS TO THE TRILOGY TECHNOLOGY

- ACCESS TO HIGH PERFORMANCE COMPUTER DESIGN AND IMPLEMENTATION METHODOLOGY

- A TECHNOLOGY THAT CAN SUPPORT FUTURE HIGHER PERFORMANCE DESIGNS WITH OPPORTUNITY TO RECEIVE IMPROVEMENTS MADE TO THE TECHNOLOGY ITSELF

- RIGHTS TO THE TRILOGY DEVELOPMENT, TESTING, AND MANUFACTURING PROCESSES

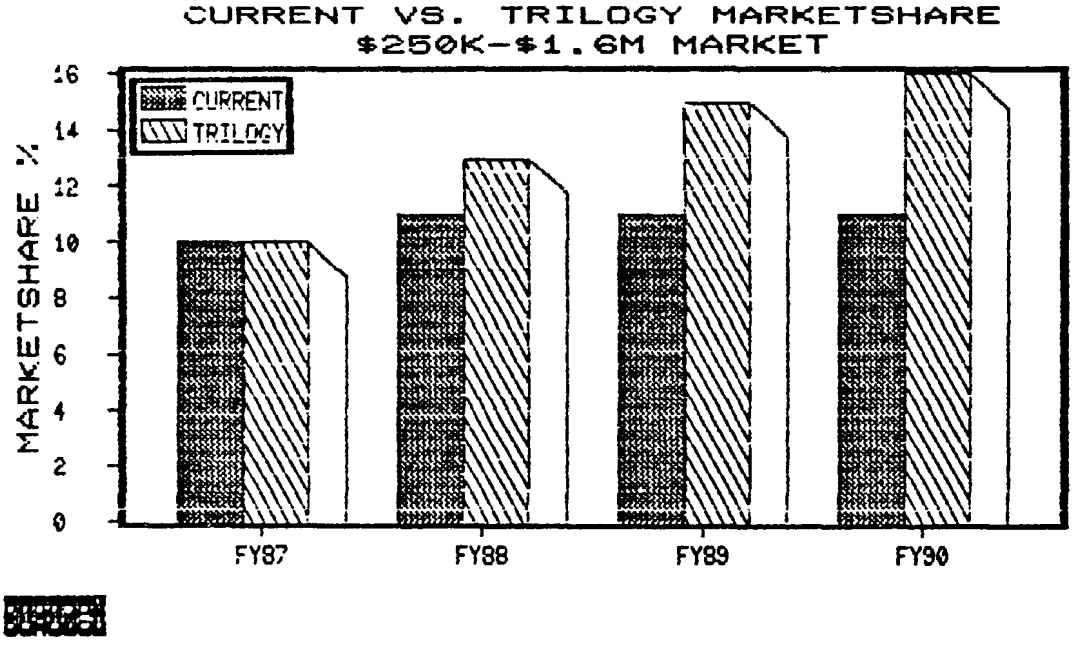
- A SOURCE OF SUPPLY OR SUPPORT TO ESTABLISH ONE

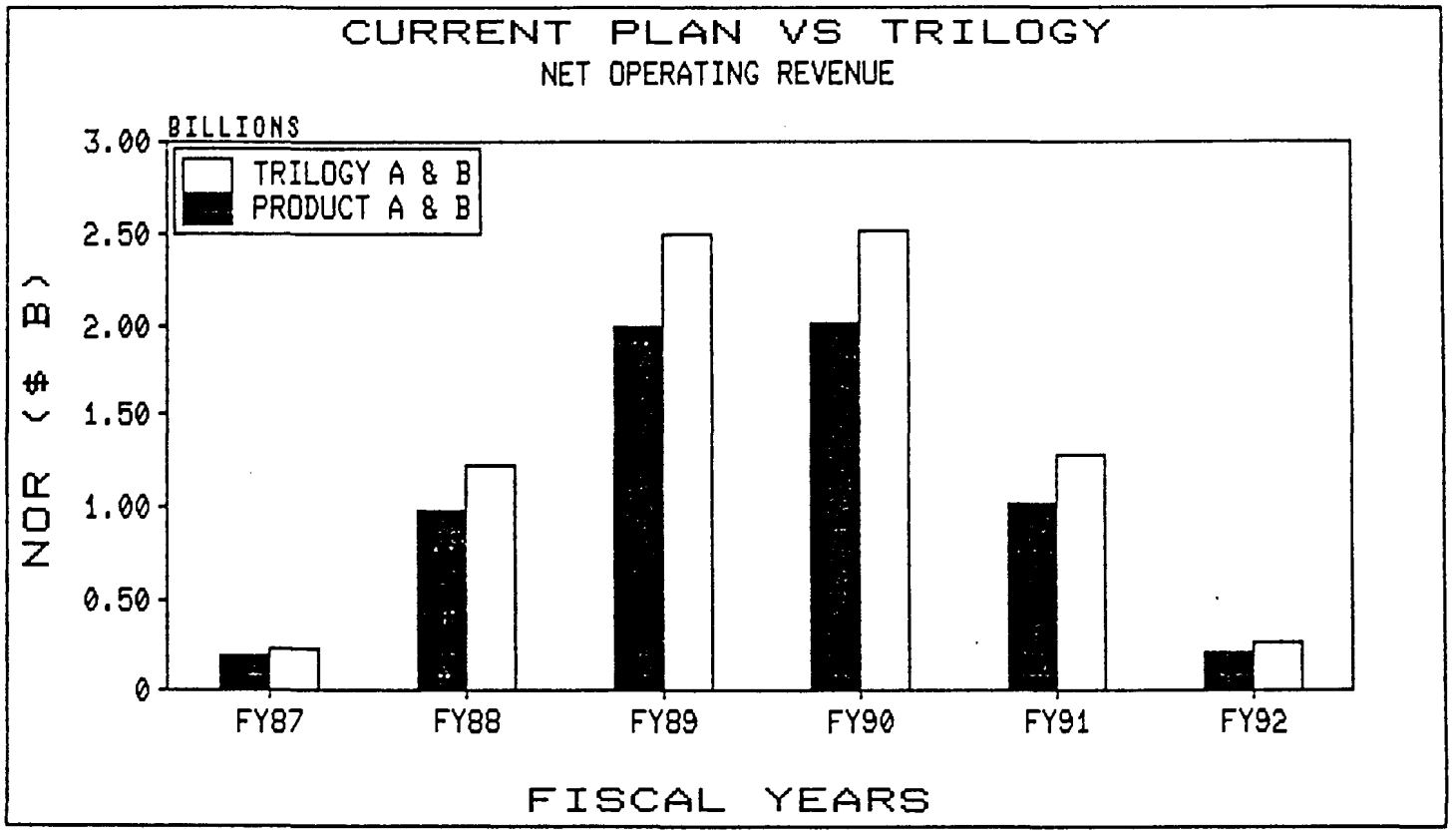
- EQUITY INVESTMENT

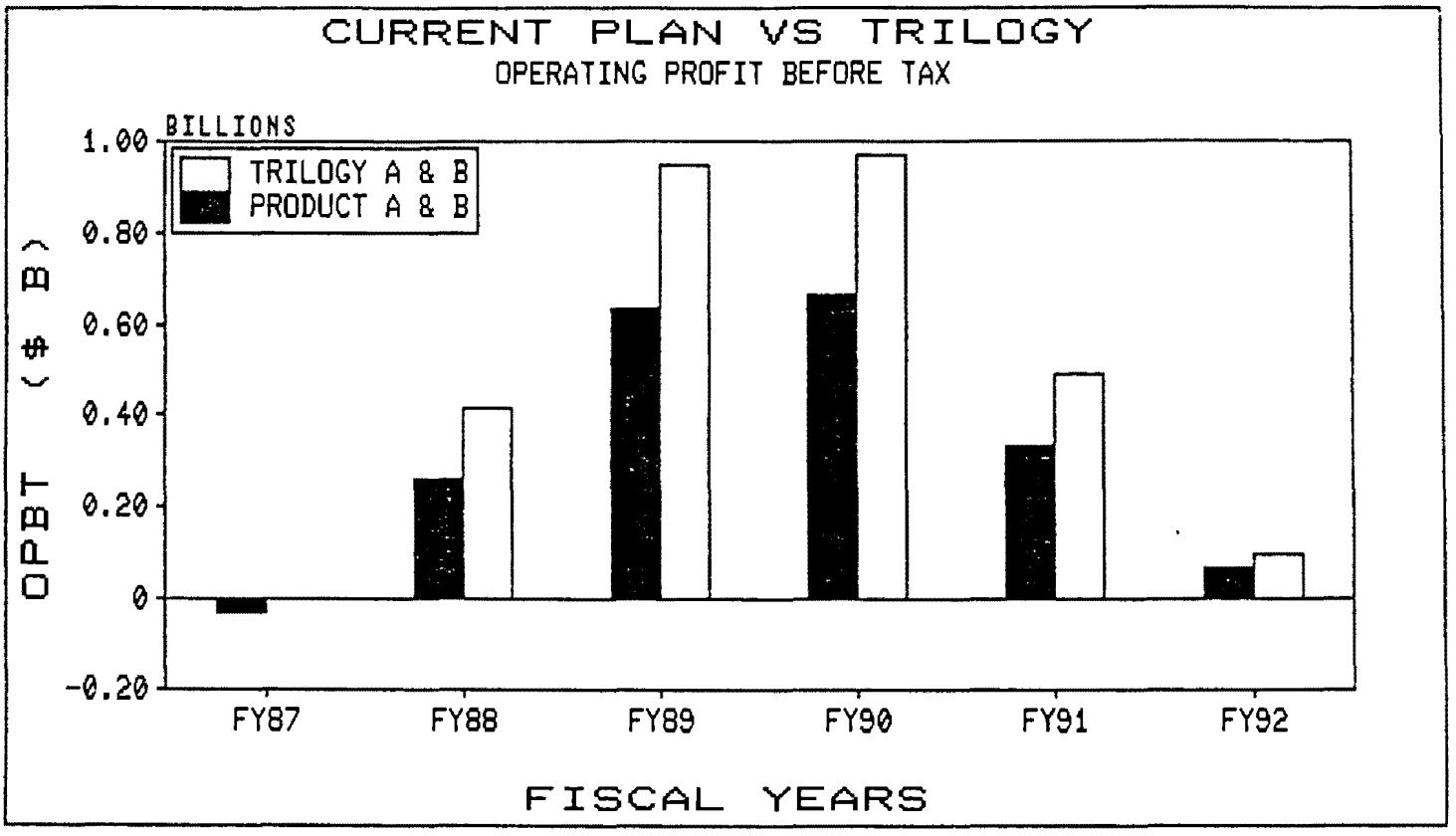
    8% INITIALLY

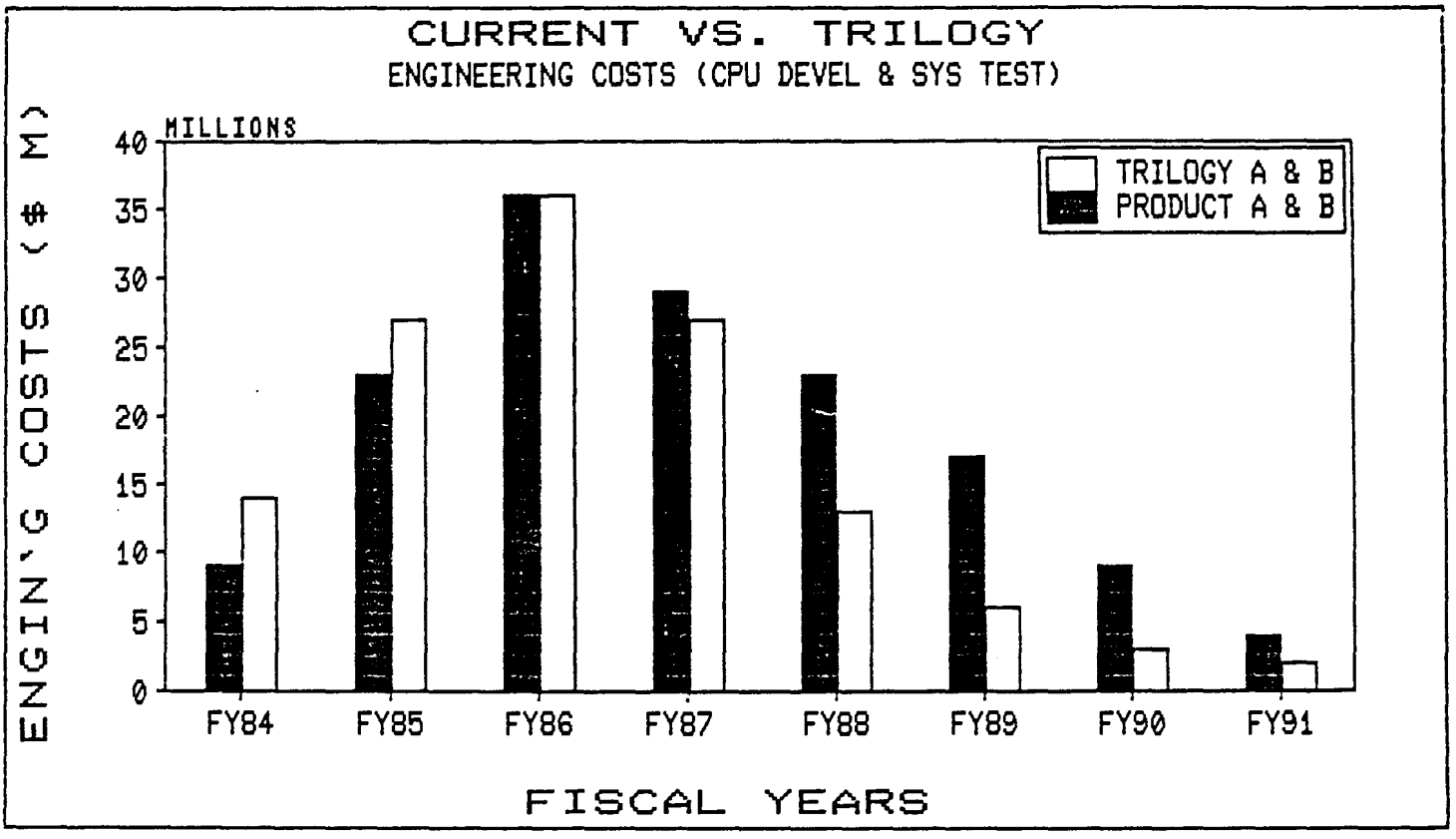
    6% AT PUBLIC OFFERING TIME

- POSITION ON BOARD OF DIRECTORS


CURRENT VS. TRILOGY MARKETSHARE
$250K-$1.6M MARKET
CURRENT
TRILOGY
MARKETSHARE %
0
2
4
6
8
10
12
14
16
FY87
FY88
FY89
FY90


CURRENT PLAN VS TRILOGY
NET OPERATING REVENUE
BILLIONS
3.00
2.50
2.00
1.50
1.00
0.50
0
NOR ($ B)
TRILOGY A & B
PRODUCT A & B
FY87
FY88
FY89
FY90
FY91
FY92
FISCAL YEARS


CURRENT PLAN VS TRILOGY
OPERATING PROFIT BEFORE TAX
BILLIONS
TRILOGY A & B
PRODUCT A & B
OPBT ($ B)
1.00
0.80
0.60
0.40
0.20
0
-0.20
FY87
FY88
FY89
FY90
FY91
FY92
FISCAL YEARS


CURRENT VS. TRILOGY
ENGINEERING COSTS (CPU DEVEL & SYS TEST)
ENGIN'G COSTS ($ M)
MILLIONS
40
35
30
25
20
15
10
5
0
TRILOGY A & B
PRODUCT A & B
FY84
FY85
FY86
FY87
FY88
FY89
FY90
FY91
FISCAL YEARS

SUMMARY OF BENEFITS

COMPETITION

- BE LEADER IN HIGH END TECHNICAL MARKET

BUSINESS

- IMPROVED RETURN ON INVESTMENT
- HIGHER PROFIT MARGINS
- REDUCED TIME TO MARKET RISK
- SECOND GENERATION FOLLOW-ON PRODUCTS

TECHNOLOGY

- WAFER SCALE INTEGRATION DENSITY
- METHODOLOGY FOR COMPLEX DESIGNS
- POTENTIAL FOR NEW LEVELS OF RELIABILITY

DIGITAL CAN LEAD IN FUTURE HIGH END MARKET

Send to Gordon Bell

Gordon - surprised to hear Wednesday that you didn't know we have a large system mfg. organization - this should make your day! Charlie Bradshaw is Ulf's mfg. twin and they are even colocated! You'll like Charlie, he is an effective manager and has the right motivations. See first few pages for flavor.

Dave Knoll
9/12/80

gBell

COPY #: 1 NAME: Gordon Bell

C O M P A N Y C O N F I D E N T I A L
D O N O T C O P Y

d i g i t a l

interoffice
memorandum

SUBJ: PERSONAL COMPUTERS AND THEIR IMPACT ON THE PRODUCT STRATEGY

TO: OOD
OC
Dave Cutler
Dick Hustvedt
Duane Dickhut
Bob Glorioso

Date: 11/10/80 Mon
From: Gordon Bell
Dept: OOD
MS: ML12-1/A51 Ext: 223-2236
EMS: @CORE

Alan Kotok	Bernie Lacroute	Larry Samberg
Tony Lauck	Jesse Lipcon	Tomas Lofgren
Maurice Wilkes	Mark Bramhall	Avram Miller
Pete Hurley	Peter Lipman	Richy Lary
Mike Riggle	Dave Rodgers	Henk Schalke
Scott Davis	Ollie Stone	Bill Strecker
Steve Teicher	Tom McIntyre	Bob Travis

CC:

Joe Carchidi	Bob Daley	Bruce Delagi
Frank Hassett	Bill Heffner	Stan Pearson
Bill Picott	George Plowman	John Rose
Dick Snyder	Gil Steil	Bruce Stewart

We are building a Personal Computer to be used both in the existing PC marketplace, and with our own systems. This discussion shows why we can not ignore PC's by first showing how they have evolved within the total computing context, together with how, by networking them, they compare with our conventional shared sytems.

Specific recommendations are made so as to align with the 1979 Product Strategy, followed by a more detailed background, and rationale.

The middle section describes a set of segmentation dimensions so we can tell the difference between a 1K Radio Shack TRS80 I, and a 40K Single User VAX. The dimensions are: price; the overall Galactic (Digital) Architecture which describes all our products and how they interconnect; the base machine as seen by applications programs; various applications programs that various different users use; the various users and the applications programs they are likely to use; and finally a product availability segment.

The final section lists various questions we need to answer in setting our direction.

EVOLUTION SUMMARY

In the beginning, we had standalone, but shared computers, as an individual went to the computer and operated it alone. This quickly evolved into batch mode because computers were so expensive and had to be run efficiently. We developed Timesharing Systems (TSSs) so that everyone could "apparently" have their own computer. We also made minis so everyone could have their own computer (eg. LINC) ... and then we put timesharing on the larger minis (eg. TSS8, evolving to RSTS) to get the cost per terminal down. This era covers 1965 to 1990.

In 1977, with microprocessors, low cost ram, and small floppies, the Personal Computer (PC) entered the scene as an alternative to some TSS; by simply adding a terminal emulation program, a PC could operate as a dumb terminal (with some nice file access capability like the old Teletype ASR 33). WPS78 is a good example of a PC doing word processing (WP) and behaving as a terminal emulator. PC's with terminal emulators will be a short lived phenomena, covering only 1975 to 1985, because there is pressure to have PC Networks in order to minimize shared facilities. PC's with terminal emulation will have home use!

PC Networks must form both for economic and sharing reasons. Local area networks, like Ethernet, are necessary to effectively support them. PC Networks will be the dominant structure of the 80's! Figure Evolve shows the evolution from Timesharing Systems to Personal Computers with dumb terminal emulation programs to PC Clusters (and networks of clusters) PC Networks. If we dissect the structure of a TSS, we find it is composed of components that in principle can be broken apart and allocated to individual computers when forming a completely distributed PC cluster. A cluster is organized around the "distributed server" concept, where one or more processes reside on distinct processors and communicate with one another using a message passing mechanism via a fast, serial link. The components include: file service, print service (print queue), communications and network service. The scheduling and accounting programs, and of course, the jobs that exist for each person are distributed on the "person server" machines (i.e. the PCs ... which indeed must be capable of operating stand alone!). As we distribute the various processes, there are pros and cons which will be described below.

WHAT TSS, PC AND PCC/PCN PROVIDE

What	Timeshared System	Personal Computer	PC Cluster/Net
proc	highest peak	lo-med, guaranteed	= PC
prog	high peak	small to large	= PC
filing	large	small, guaranteed	= PC and TSS
comm.	network	term. emulation	= PC and TSS
CRT	slow response	fast response	= PC
	evolve from Teltyp	screen oriented	= PC
cost	fixed, can go to lowest/terminal	lowest entry	f(no. of PCs)
secure	shared, public acs	totally private	contained/TSS
pros	explicit costs, shared programs big jobs	low entry cost "owned" by indiv. security	ability to expand shared facilities

cons	shared poor response for terminals higher entry security	very limited, but increasing	limited proc/prog. shared facilities

IDEAL DISTRIBUTED SERVER SYSTEMS

As an ideal, one would simply take an existing system such as RSTS, and rewrite it such that each person's job is placed in his own personal computer; the appropriate server computers would also be added. With this structure, a user's investment in data and in programs to access that data is preserved and a given user can buy either a PCC to execute RSTS, or he could buy a single computer RSTS system like today. A file server in the personal computer would permit access either within his own machine, or at the central server, or possibly within other individual machines (perhaps via the central file server). As a further ideal, servers could run equally well on any one of our current systems (eg. VMS, RSTS, 10, 20) as a cluster, with the additional capability of being able to access other systems anywhere in the network in a transparent fashion. Such a system is well beyond our present ability to construct, but having the goal of preserving data and programs together with tools to move from a TSS to a PCC and then a PCN environment is necessary.

Alternatively, since we have a goal to evolve our machine use to VMS within the next 5 years, we should take the PC as an opportunity to begin this migration by making PC-11 and PCC-11 a subset of VAX. This would mean that programs written for the 11 environment would run on VAX. Also, the files would be upward compatible with VAX. Furthermore, we must establish a PC-VAX, and PCC-VAX environment.

PRODUCT STRATEGY UPDATE FOR PERSONAL COMPUTERS

In January 1979, we adopted the Corporate Product Strategy of evolving our systems to VAX by 1985, while building additional hardware to operate TOPS 10/20. 11 systems are to be developed in the product space where low cost VAX systems can not yet be built. Terminals and small systems were to be converged and built on 11's. Given the strategy, I believe it means:

minimize future investment in current 11 systems
concentrate on co-existence/migration tools for RSTS, M/M+
build minimal follow on 11 cabinet systems, since our future low end VAX covers systems of 23 size with RL's
aggressively build PC-11 that can operate stand alone, as a terminal emulator, or in a cluster environment. It would provide an environment compatible with a VAX subset.
(explore alternative of a PCC-11 fully compatible with RSTS or 11M for a user's program and data)
establish a clearly defined VAX environment to envelope the

existing TSS-VAX, TSS-VAX (Clustered), PC-VAX, and PCC-VAX (distributed server).

build, ship, and test a SUVAX to establish PC-VAX and PCC-VAX

aggressively go for PC-VAX with a <2.5K cost (system with high resolution scope and mass storage)

This strategy is aimed at establishing the 11 in the personal computer in the form of PC's, PCC's and PCN's compatible with the long term. Do it FAST and go for VAX in the long term. Build to maintain products at a constant price per terminal and provide increasing functionality.

DETAILED BACKGROUND

The opening statement of the August 1979 CMU Research Proposal for Personal Computers was "Timesharing is dead, to be replaced by networks of Personal Computers in the 80's". Research groups have built and are building Personal Computer (PC) Networks (PCNs) using PCs costing 20K-50K and interconnected by high speed links like the Ethernet. Xerox Research PARC, the developer of the "distributed server" architecture is the archetype of this environment with several hundred Alto personal computers and service facilities (eg. File Servers, Printer Servers, Network Server for interconnection to outside computers, and a Tenex Computation Server) interconnected over 3 Ethernet segments of several kilometers. The Datapoint computer system is built using the "distributed server" structure. Apple is likely to introduce Apple-net in 1981 to interconnect their PC's, forming Personal Computer Networks (PCN's). Wang and other WPSs are organized around a co-axial ring, using file and printer servers, and distributing the processing in the terminal computer, forming a limited, single cluster, PCC. (It's stretching the definition a bit to call these PCC's, cause they can not stand alone.)

PC's, PCC's, and PCN's all form alternatives to our small, medium and large timesharing systems (TSS's) for various reasons, and therefore, we have no choice of ignoring them! Figure Cstyle shows my guess at how the computing style (batch, shared, RJE, personal, PCC, PCN) has evolved and will evolve from 1950-1990. Given that a terminal has video, keyboard, power supply, control logic in the form of a microprocessor, a package constrained by the video and keyboard, it is only slightly more expensive to increment the primary memory and add a secondary memory to get a complete computer capable of standing alone and acting as a terminal emulator. Also, tasks like editing require great amount of computing power and very fast interrupt response time. It should also be noted that this kind of response is virtually impossible to deliver in very large systems, and gets even worse in modern very large computers. (There is some evidence to show that the cache miss rate goes up as the square of the processor speed. Also, the access time of large disks is not improving as rapidly as processing speed can.)

As an example of a terminal evolving into a PC, GIGI has a ROM which gives it Microsoft BASIC capability, although we provide no secondary memory for programs... our customers probably will. Therefore the forces to make every terminal evolve into a personal computer are: constant overhead of the terminal, high cost of people sitting at the terminals (eg. 20K- 150K/year) relative to the terminal, lower primary memory cost, need for much more processing at the terminal, the introduction of the small floppy and now the small Winchester that can be packaged in the terminal. Given that we sell a lot of dumb terminals, it is important for us to evolve them this way.

Just as there have been forces to establish the PC as an alternative to the dumb terminal using a terminal emulator program, the forces will continue to replace all the functions that the Timeshared System provides by clustering the PC's and by having shared facilities. The Ethernet (NI) hardware supports this evolution. As we simply cluster the PCs, communication and file access among the machines is provided as long as all the computers are ALL turned on. This requirement leads back to asking for some shared facilities, in addition to the communications link. Sharing occurs for only two reasons: it is drastically cheaper or that it is necessary for communications. High performance or high quality printers, communications facilities, and large filing systems are examples of economic sharing; a filing system and communications link are examples of communications sharing.

SEGMENTATION DIMENSIONS

PC's will be described using these segmentation dimensions:

- Price (correlated with size)
- The Galactic Architecture PMS Structure
- Base Machine (PMS structure, O/S, Files and Languages)
- Applications Machines (Layered SW Components)
- Users
- Time (actually product availability)

PRICE

Our system price bands are ideal for our product planning because it will force us to not over populate the product space. Note that each product should be positioned a factor of 2.5 apart, such that 3 ranges cover a factor of 16. With PCCs it is possible to cover a much wider range by adding more identical components because the entry cost is reduced! The price bands and products:

.4K- 1K	Radio Shack PC's
1K-2.5K	Small Computing Terminal 65Kbytes (with/without floppy) Simple network, and Printing servers
2.5-6.5K	Large Computing Terminal 256K and 5Mbytes
6.5-16K	File Server and line printer (copier) servers
16K-40K	SUVAX

Note that an RL02-based 11/23 with 8 terminals sells for about 50K, giving a price of 6.25K, which is the price of the large CT.

SUVAX now costs 12K with Nebula, disks and high resolution scope, but PC-VAX should be aimed at 2.5K to replace 11's (which by then may be directed to cost under 1K! Note, there are a large number of competitive machines entering this arena. All have high resolution scopes and are aimed at the professional. The competitors:

Zenith, being designed by MIT (5K-50K) and with deliveries in March and volume next year;

Three Rivers Perq, being designed with CMU, 20K-50K, 3 delivered and lots operating, based on a very fast, microprogrammed machine;

Appolo, Spector's company being designed by Bill Poduska, formerly VP of Eng. at Prime and developer of the Prime Systems and using the 68000;

Big Apple, Wayne Rosing et al targetting the Office, using 68000, most likely;

Convergent Technology, Al Michaels, et al, mostly Ben Wegreit a very bright researcher from Xerox Research Parc. They've announced and are building it solely as an OEM using the Intel boards and the Multibus. A great way to track Intel the closest and minimize hardware development costs;

BBN Jerricho- ?

THE GALACTIC ARCHITECTURE PMS STRUCTURE

GA- Galactic Architecture- The entire collection of computers we are building including the interconnection to form a single network using an NI at a single site. It includes the range of systems over all user environments. Figure GAE shows the evolution of the total computing environment over thes next few years. The following components form GA:

TSS- Timesharing Systems- Systems with >1 dumb terminal, evolving to have intelligent (programmable) terminals to increase cost effectiveness and throughput, evolving PC's connect to it. TSSs exist both for departmental and group level sharing. Our users run 11 systems: Tops-10, Tops-20, VMS, RSTS, 11M, 11M+, IAS, DSM and WPS 200; and Unix-11 and Unix-VAX.

TSS Clusters- A collection of VMS or VMS and Tops 20 System running at a single site and interconnected using a high speed NI, called CI. A seperate disk server holds files.

PC- Personal Computers- Systems with ONLY 1 terminal and which can operate in a complete stand alone fashion. Mass storage evolving from floppies to hard disk. Future diminishing dependence on virtual terminal access to TSS's for files and computation. A PC would typically not be directly connected to NI, but would connect to a TSS, a concentrator, or be part of a PCC. RT11 and MINC are

current examples.

PCC- Personal Computer Clusters = Distributed Server Systems- Set of PCs and specialzed servers (eg. files, comm. and printing) interconnected via high speed link of 1 - 10 mbits / sec and may be confined to a very local area (eg. 100 meter radius). Each PC is a "person server" and contains one or more processes to serve a person. The kernel server O/S in each physical server accesses both internal and external servers. Each PCC can be thought of as equivalent to a TSS. Most likely a "person server" would only have service capabilities for the individual using it.

PCN- PC Networks- PCCs which are part of the overall network and are interconnected via NI.

Concentrators- A computer connected either directly to a TSS or to NI and with ability to interface dumb or intelligent terminals to the NI.

Gateways- Real time computer for converting international and computer company protocols to the DEC network environment.

Real Time Computers- Real time I/O would be either connected directly to a given computer, or would come into the network via special "front end" machines. RSX-11M.

NI- Ethernet- The interconnect we intend to use during the 80's to interconnect many of the components we are building, to form a Galactic Architecture. Capability of spanning 2.5Km in .5Km segments. Must have same protocol as LNI, the local network interconnect, used to interconnect a PCC.

BASE MACHINE (PMS STRUCTURE, O/S, FILES AND LANGUAGES) FOR APPLICATIONS MACHINES CONSTRUCTION

Given that we currently support at least 12 user machine environments, it is difficult to think of how we can evolve to a homogeneous VMS environment in the future. Nevertheless, we must have a constraint such that programs and data are made to be compatible with this homogeneous environment over time. In doing the PCC, it has to be made compatible with either an existing system so that users can chose between a TSS and a distributed system, or it has to be subset compatible with the VAX environment. This means that a program and its data written for PC-11, or PCC-11 would run on: PC-VAX, TSS-VAX, or PCC-VAX.

The problem of determining the user environment is similar to that we face in having the TOPS 10 and TOPS 20 environment coexist with VMS. However, there is one major difference, VMS is established and the constraint is to build a system that is sub-set compatible with it in terms of the languages, files and

user interface. We still have to resolve the compatibility with RSTS and M/M+ and VMS. Also, whether we want to build a distributed RSTS and M/M+ systems on PCC-11.

We probably need to support the following languages:
BASIC- Compatible with BASIC+2 (RSTS base)
BASIC- Compatible with Microsoft BASIC to run std. PC software
DIBOL- For COEM environments
COBOL- For emerging business applications
Fortran- For technical market and specific applications
Pascal- Education and technical market until ADA arrives
VISICALC- Two dimension calculator and language

APPLICATIONS MACHINES (LAYERED SW COMPONENTS)

Word Processing
Telephone Management
Datatrieve for personal databases
Terminal emulation for dumb, intelligent, forms entry, tp terms.
including Tektronix emulation
Graphics calculator including VISICALC (VMS educational SW)
Entertainment programs

Languages for build it yourself applications (as above)

Commercial specific:
Standard small business set (payroll, A/P, A/R, Gen. Ledger, etc)
Parameterized software

Technical market specific:
COGO, Stress, Project Control System

School administration

USERS

Here, we take the basic applications components and package them as a set of components for specific, identifable users:

Office worker
Office worker with forms entry
Technical person (engineer, scientists, statistician, bus. analy)
Small Businessperson
Home management

MACHINE AVAILABILITY (TIME SCALES)

In order to start getting results in entering this market, it is important to start aggressively marketing the products we CURRENTLY have. Therefore, we should segment our thinking into the following time scales.

Next Two Years

We have to move the following products:
PDT 150, using LA34's, VT100's, VT125's and possibly GIGI to get graphics
VT278 which will also be available with RL02's!

This can be a very good opportunity to learn about channels of distribution and packaging collections of applications to address an identifyable set of users.

Two-Four Years
Introduce PC, followed by PCC with Network support
Aggressively cost reduce to go for mass market!(?)

Four Years
Introduce PC-VAX and PCC-VAX

QUESTIONS TO BE RESOLVED

What program environment should PC-11 and PCC-11 provide? (VAX-subset, RSTS, M/M+, UNIX, something else)

Is it possible to generally distribute any system like this easily?

Can the protocols on the LNI be those of the NI?

Can we evolve servers to run on any machine? Is this a technique to evolve into compatibility with homogeneous computing environment?

Can we make a PC-11 standalone, and a compatible PCC that are cost-effecitive?

How large do the PC's have to be to run the various systems? (Eg. file server, person server) Do we force floppies or do we downline load on LNI using a ROM boot?

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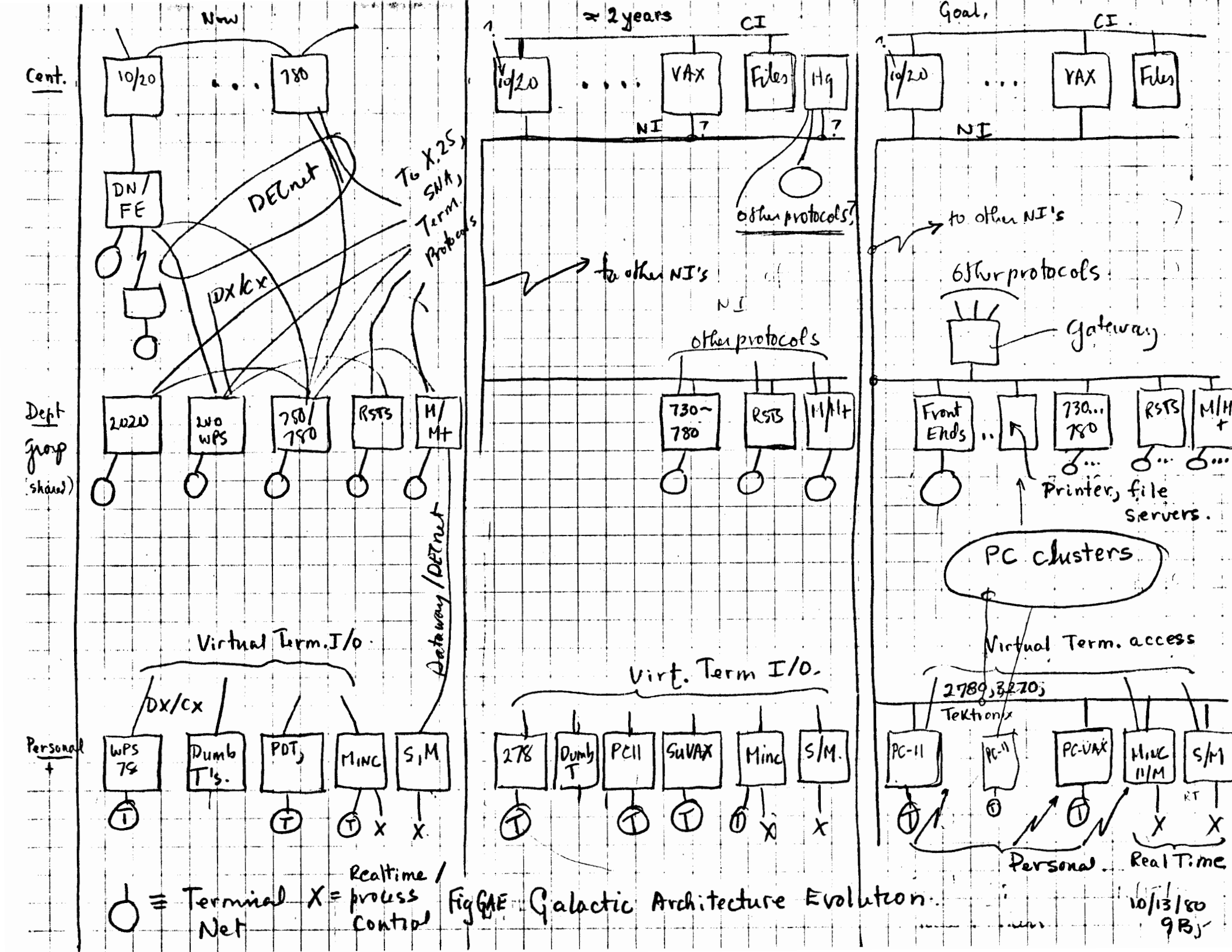

Fig 6AE Galactic Architecture Evolution

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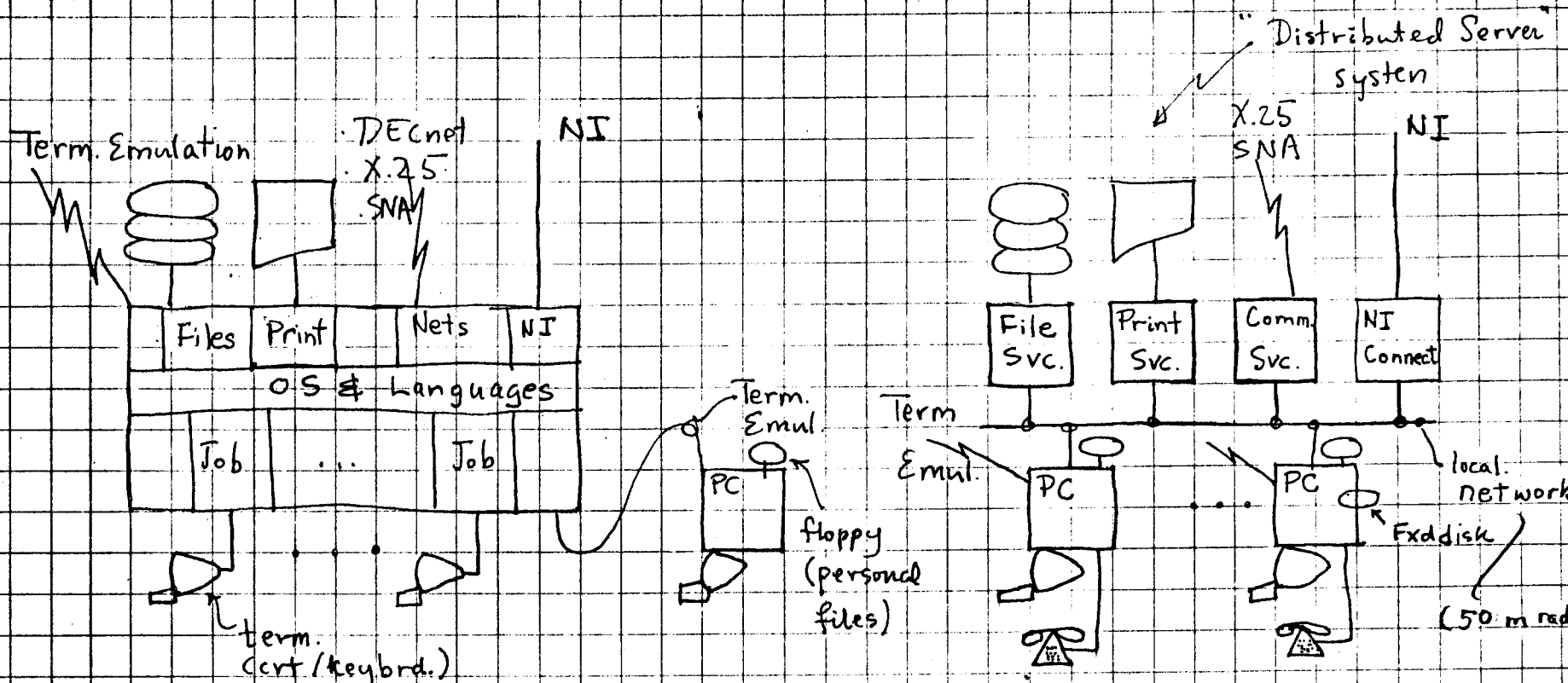


Timeshared Systems of the 70's ('65-'85) (eg. RSTS, WPS, 11/M, VMS)

• Personal Computers (with Term. emul.). (+eg. WPS, RT, Apple) (1978-'85)

• Personal Computer Clusters & Networks of the 80's (>1981) (eg. DRSTS, D-VMS, D-11/M)

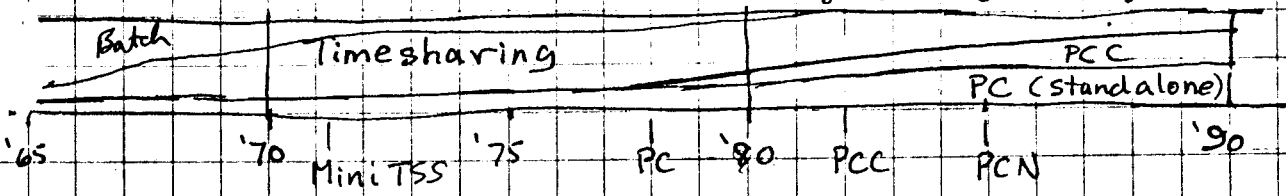
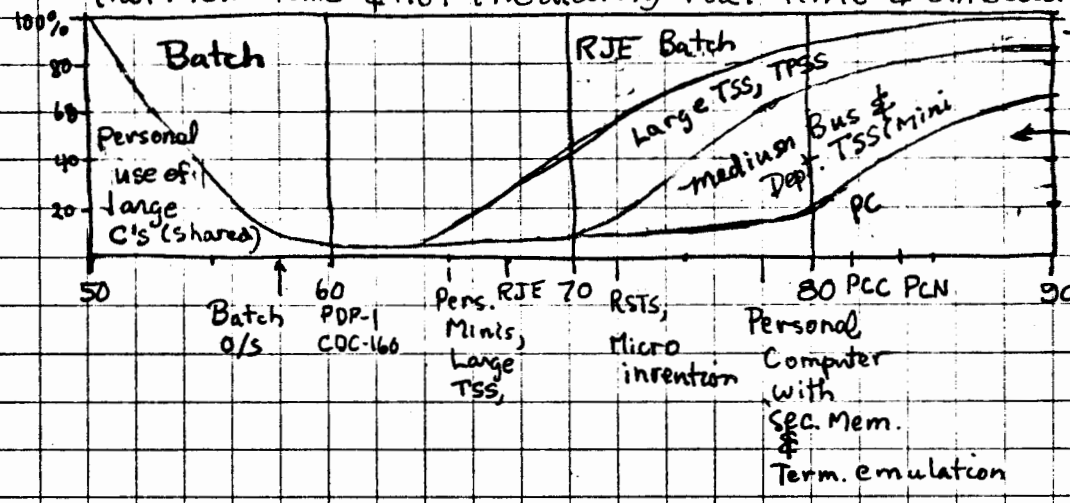


Fig. Evolve Evolution from timesharing to Personal Computer Cluste

gB 11/9/80

Fig. Cstyle. Computing style of use vs. time (G Bell Wag).
(not incl. home & not including real time & embedded computers)



— Large orgs. only

← Personal Computers:
- standalone
- term. emul.
- clusters
- networked

(for small bus; clusters for med. bus. & nets for large orgs.)

GB 11/9/80

C O M P A N Y C O N F I D E N T I A L
D O N O T C O P Y

SUBJ: PERSONAL COMPUTERS AND THE PRODUCT STRATEGY (DRAFT)

TO: ENG STAFF
Avram Miller, ML5-2/T53
Bruce Stewart, MK1-2/E06

Date: 2/10/81
From: Gordon Bell
Dept: OOD
MS: ML12-1/A51 Ext: 223-2236
EMS: @CORE

BACKGROUND

We are building a Personal Computer to be used both in the existing PC marketplace AND as a key part of the computing environment we are supplying. This discussion argues why we must build first-rate PC's by first showing how they have evolved, and how, by networking them into PC Clusters (PCC) and PC Networks (PCN's), they compare and compete with our conventional, shared sytems. Perhaps 100K of the PC's sold in 1980 are as alternatives to say 5K departmental timeshared systems with 100K dumb terminals we could have sold!

A set of dimensions segment the difference between a $1K Radio Shack TRS80 I, and a $40K Single User VAX. The dimensions are: price; our homogeneous computing environment (architecture) which describes all our products and how they interconnect; the base machine as seen by applications programs; and applications program set for various users.

Specific recommendations are made so as to align with the 1979 Product Strategy, followed by a more detailed background, and rationale.

THE PERSONAL COMPUTER AS AN ALTERNATIVE TO TIMESHARING

The opening statement of the August 1979 CMU Research Proposal for Personal Computers was "Timesharing is dead, to be replaced by networks of Personal Computers in the 80's". Research groups have built and are building Personal Computer (PC) Networks (PCNs) using PCs costing 20K-50K and interconnected by high speed links like the Ethernet. Xerox Research PARC, the developer of the "distributed server" architecture is the archetype of this environment with several hundred Alto personal computers and service facilities (eg. File Servers, Printer Servers, Network Server for interconnection to outside computers, and a Tenex Computation and File Server) interconnected over 3 Ethernet segments of several kilometers. The Datapoint computer system is built using the "distributed server" structure. Apple is likely to introduce Apple-net in 1981 to interconnect their PC's, forming Personal Computer Networks (PCN's). Wang and other WPSs are organized around a co-axial ring, using file and printer servers, and distributing the processing in the terminal computer, forming a limited, single cluster, PCC. It's stretching the definition a bit to call these PCC's, cause no PC can stand alone.

It's essential to note that a PC is not just a tiny computer with a serial link to a dumb terminal (glass teletype). This was only time in the initial implementations. New PC's must have the ability to save and restore a complete screen, and to be able to use a screen to help the user more similar to the TV games. This very high speed communication will dictate a whole different O/S philosophy for screen management.

PROPOSED (DETAILED) PC PRODUCT STRATEGY

The Corporate Product Strategy (1/79) outlines evolving our systems to VAX by 1985, while building 11 systems in the product space where low cost VAX systems can not yet be built (i.e. single user, less Mp:512Kby than Ms:10Mbyte system). Terminals and single user, small systems are built on 11's. The strategy continues to hold as being our strength against competitors. This imples:

- minimize future investment in current multi-terminal 11 systems i.e.
  - concentrate on co-existence/migration tools for RSTS, M/M+ to VMS
  - build the fewest possible follow on 11 cabinet systems, since our future low end VAX covers larger hard disk systems
  - aggressively build PC-11 for three environments:
    - support of our conventional OS's on the PC-11 hardware for existing users
    - supporting the PC industry - standard software terminal emulator
    - as part of the DEC architecture which starts standalone and evolves to a cluster. This system is compatible with a VAX subset for files and programs. This implies a different lower level interface and to be successful, the terminal interface must evolve beyond the "glass teletype" which is used on our system.
  - establish a VAX environment for PC's (including servers) to ervelope the PC-11, PC-VAX (i.e. SUVAX) and ultimate PC-VAX based on Scorpio
  - build, ship, and test a SUVAX to establish PC-VAX and PCC-VAX and to begin to acquire the application that only VAX can support
  - aggressively schedule PC-VAX with a <2.5K cost (system with high resolution scope and mass storage) by 1985

This strategy is aimed at establishing the 11 in the personal computer in the form of PC's, PCC's and PCN's compatible with the long term VAX architecture and PC-VAX by 1985 based on Scorpio.

PC'S ARE A NEW COMPUTER GENERATION

PC's, PCC's, and PCN's all form alternatives to our small, medium and large timesharing systems (TSS's) for various reasons, and therefore, we have no choice of ignoring them! Figure Cstyle shows a guess at how the computing style (batch, shared, RJE, personal, PCC, PCN) has evolved and will evolve from 1950-1990.

Given that a terminal has video, keyboard, power supply, control logic in the form of a microprocessor, a package constrained by the video and keyboard, it is only slightly more expensive to increment the primary memory and add a secondary memory to get a complete computer capable of standing alone and acting as a terminal emulator.

As an example of a terminal evolving into a PC, GIGI has a ROM which gives it Microsoft BASIC capability, although we provide no secondary memory for programs...our customers probably will. Therefore the forces to make every terminal evolve into a personal computer are:

- constant overhead of the terminal;

- high cost of people sitting at the terminals (eg. 20K- 150K/year) relative to the terminal;
- lower primary memory cost;
- need for much more processing at the terminal;
- the introduction of the small floppy and now
- the small Winchester that can be packaged in the terminal.

Given that we sell a lot of dumb terminals, it is important for us to evolve them this way.

Tasks like editing require great amount of computing power and very fast interrupt response time. It should also be noted that this kind of response is virtually impossible to deliver in very large systems, and gets even worse in very large computers. There is some evidence to show that the cache miss rate goes up as the square of the processor speed. Also, the access time of large disks is not improving as rapidly as processing speed.

Just as there have been forces to establish the PC as an alternative to the dumb terminal using a terminal emulator program, the forces will continue to replace all the functions that the Timeshared System provides by clustering the PC's and by having shared facilities using Ethernet. As we simply cluster the PCs, communication and file access among the machines is provided as long as all the computers are ALL turned on. This requirement leads back to asking for some shared facilities, in addition to the communications link. Sharing occurs for two reasons: it is drastically cheaper or that it is necessary for communications. High performance or high quality printers, communications facilities, and large filing systems are examples of economic sharing; a filing system and communications link are examples of communications sharing.

EVOLUTION FROM TSS TO PC CLUSTERS AND NETWORKS

DEC developed Timesharing Systems (TSSs) so that everyone could "apparently" have their own computer which could be operated in an interactive, not batch fashion. We also built single user minis so everyone could have their own computer (eg. LINC) as the first truly interactive, personal computers ... and then we put timesharing on the larger minis (eg. TSS8, evolving to RSTS) to get the cost per terminal down. This era covers 1965 to 1980. 1980-1990 is likely to be a transition from the shared system to powerful PC's!

In 1977, with good microprocessors, low cost ram, and small floppies, the Personal Computer (PC) entered the scene as an alternative to some TSS. By simply adding a terminal emulation program, a PC could operate as a dumb terminal (with some nice file access capability like the old Teletype ASR 33) and still be connected to a TSS, YET THE COST IS NOT MUCH MORE THAN A DUMB TERMINAL. WPS78 is a good example of a PC doing word processing (WP) and behaving as a terminal emulator. PC's that only standalone and use terminal emulators will be a short lived phenomena, covering only 1975 to 1985, because there is pressure to have PC Networks in order to minimize shared facilities. This is analogous to the growth limiting departmental minis have placed on central mainframes. However, it is possible that PC's with terminal emulators could strengthen central mainframe computing and decrease departmental minis. PC's with terminal emulation and access to central systems will have wide scale home use!

PC Networks will form for economic pressure and sharing needs. Local area networks, like Ethernet permit their formation. Thus, by proper design it appears that one can cover a much wider dynamic product range using this

approach as compared to our TSS approach. Figure Evolve shows the evolution from Timesharing Systems to Personal Computers with dumb terminal emulation programs to PC Clusters and finally to networks of clusters; PC Networks.

A TSS is composed of components that in principle can be broken apart and assigned to individual computers when forming a distributed PC cluster. A cluster is organized around the "distributed server" concept, where one or more computers reside on distinct processors and communicate with one another using a message passing mechanism via the fast, serial local area network link. The components include: the local area network link, the basic "person server", file service, print service (print queue), communications and network service. The scheduling and accounting programs, and of course, the jobs that exist for each person are distributed on the "person server" machines (i.e. the PCs ... which indeed must be capable of operating standalone!).

TABLE: WHAT TSS, PC'S AND PC CLUSTERS OR NETWORKS PROVIDE

What	Timeshared System	Personal Computer	PC Cluster/ Net
processing	highest peak	lo-med, guaranteed	= PC
programs size	very high peak	small to medium	= PC
filing	large	small, guaranteed (+ off line)	= PC and TSS
communication	network	term. emulation	= PC and TSS
CRT	slow response "glass Teletype"	fast response, screen oriented	= PC = PC
cost	fixed, can go to lowest$/terminal	lowest entry	f(no. of PCs)
secure	shared, public access	totally private	contained/TSS
pros	explicit costs, shared programs big jobs	low entry cost "owned" by indiv. security software publishing = low cost	ability to expand shared facilities
cons	shared poor response for terminals higher entry security	limited capibility, but increasing	limited proc/prog. shared facilities

SEGMENTATION DIMENSIONS

PC's can be segmentated along these dimensions:
- Price (correlated with size);
- The Homogeneous Computing Environment Architecture;
- Base Machine (PMS structure, O/S, Files and Languages);
- Applications Machines (Layered SW Components);
- Users;

PRICE

The system price bands are guidelines for our product planning because it helps us avoid over-populating the product space. Each product should be positioned a factor of 2.5 apart, such that 3 ranges cover a factor of 16. With PCCs it is possible to cover a much wider product range by adding more identical components because the entry cost is reduced! One takes full advantage of learning curves by minimizing products. The price bands and products:

.4K- 1K	Radio Shack PC's
1K-2.5K	Small Computing Terminal 65Kbytes (with/without floppy) Simple network, and Printing servers
2.5-6.5K	Large Computing Terminal 256K and 5Mbytes disk
6.5-16K	File Server and line printer (copier) servers
16K-40K	SUVAX

Note that an RL02-based 11/23 with 8 terminals sells for about 50K, giving a price of 6.25K, which is the price of the large CT. Thus, PC's not only start cheaper, they can be less costly for all but the largest TSS. No wonder universities are buying them in droves as an alternative to large TSS's.

SUVAX now costs 12K with Nebula, disks and high resolution scope, but PC-VAX should be aimed at 2.5K to replace 11's (which by then may be directed to cost under 1K!

COMPETIVE MACHINES

There are a large number of competitive machines entering this arena. All have high resolution, highly interactive scopes and are aimed at the professional. None resemble the interaction we provide between a TSS and a dumb terminal using a 9.6Kbaud link.

They are:
- Zenith, being designed by MIT (5K-50K) and with deliveries in March and volume next year;
- Three Rivers Perq, being designed with CMU, 20K-50K, 3 delivered and lots operating, based on a very fast, microprogrammed machine;
- Appolo, Spector's company being designed by Bill Poduska, formerly VP of Eng. at Prime and developer of the Prime Systems and using the 68000;
- Apple IV, Wayne Rosing et al for the Office, using 68000
- Convergent Technology, Al Michaels, et al, mostly Ben Wegreit a very bright researcher from Xerox Research Parc. They've announced and are building it solely as an OEM using the Intel boards and the Multibus. A great way to track Intel the closest and minimize hardware development costs;
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THE HOMOGENEOUS COMPUTING ENVIRONMENT ARCHITECTURE (COMPONENTS)

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- Fortran- For technical market and specific applications
- Pascal- Education and technical market until ADA arrives
- VISICALC- Two dimension calculator and language

(some of these enviorrments could be supported by simply executing one of the 11s O/S's.)

APPLICATIONS MACHINES (LAYERED SW COMPONENTS)

Word Processing
Telephone Management
Datatrieve for personal databases (Rolladex cards)
Terminal emulation for dumb, intelligent, forms entry, tp terminals. including Tektronix emulation
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Entertainment programs

Languages for build it yourself applications (as above)

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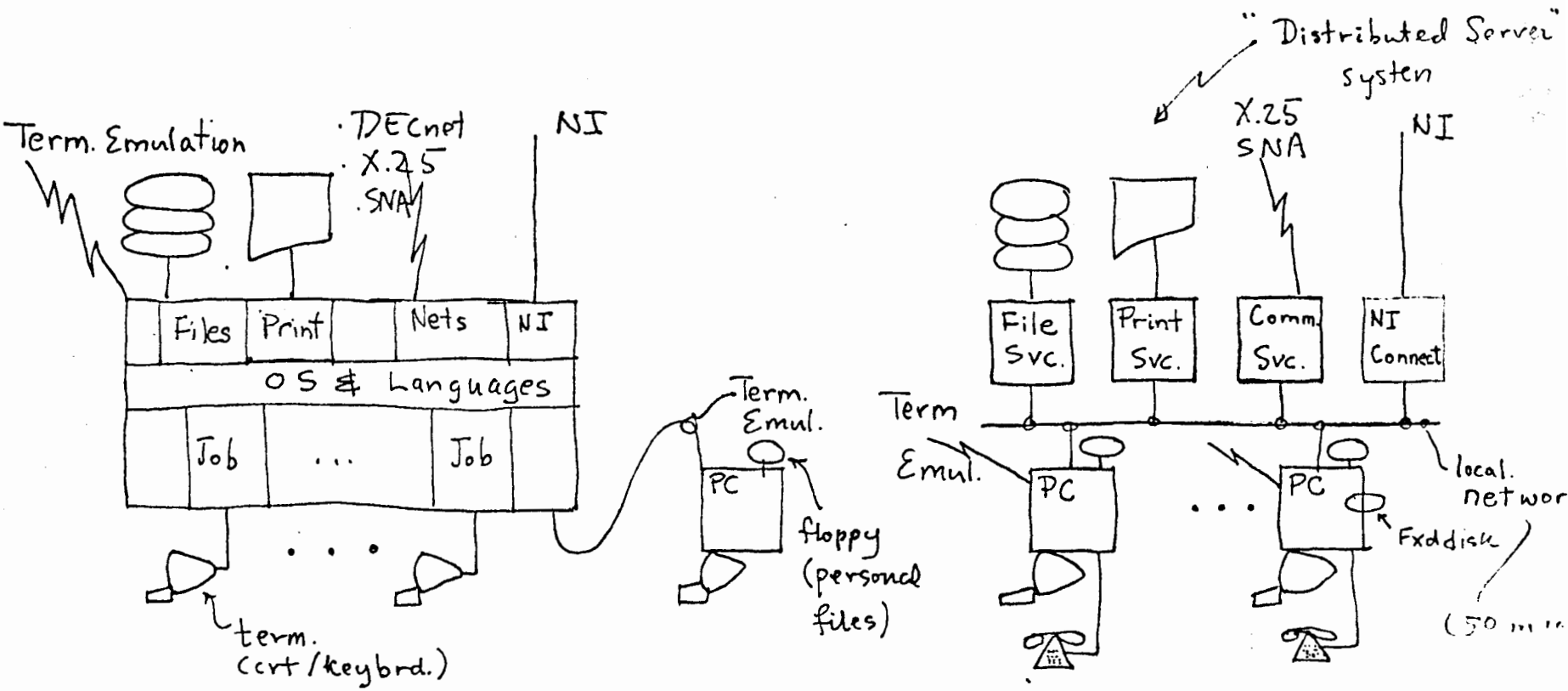
Office worker
Office worker with forms entry
Technical person (engineer, scientists, statistician, bus. analy)
Small Businesspersor
Home management



Timeshared Systems of the 70's ('65-'85) (eg. RSTS, WPS, II/M, VMS)

Personal Computers (with Term. emul.). (-eg. WPS, RT, Apple) (1978-85)

Personal Computer Clusters & Networks of the 80's (>1981) (eg. DRSTS, D-VMS, D-II/M)

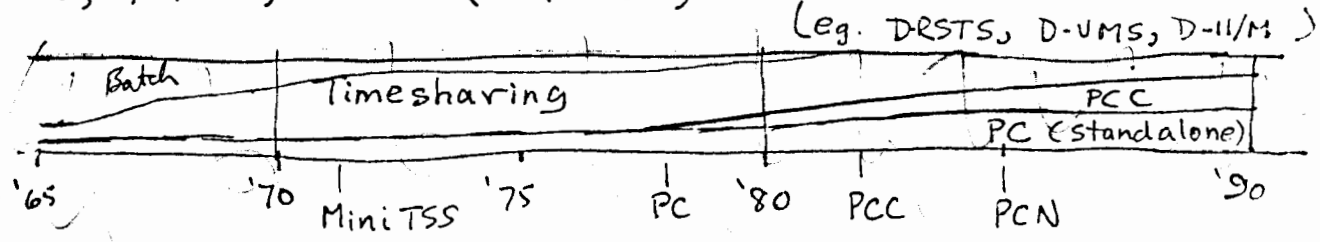


Fig. Evolve Evolution from timesharing to Personal Computer Cluste

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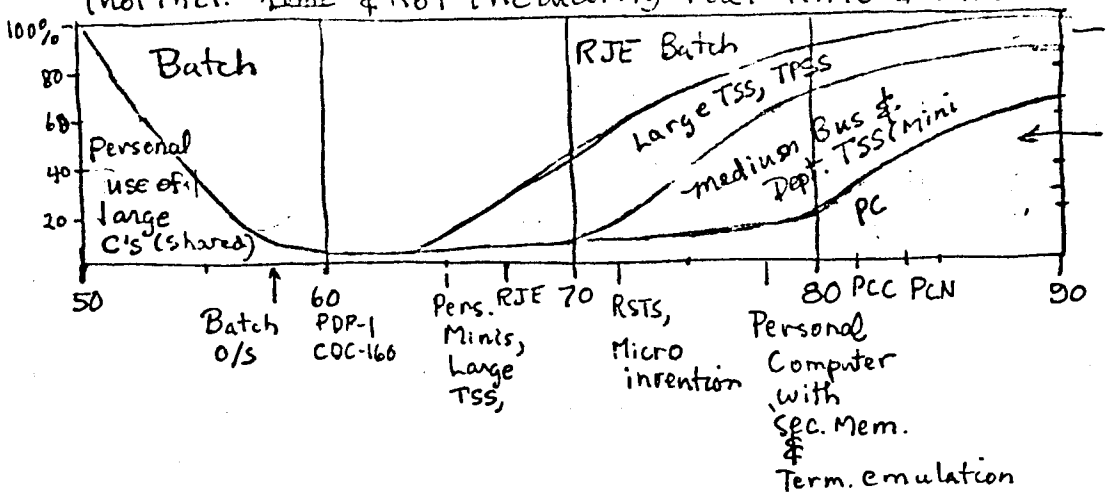


— Large orgs. only

Personal Computers:
- standalone
- term. emul.
- clusters
- networked

(for small bus; clusters for med. bus. & nets for larg orgs.)

GB 11/9/81

Acoustics · 1

COMPANY CONFIDENTIAL

Preliminary Draft for Commment by Digital Engineering Community

Spec among groups

HEURISTICS AND COMMENTS FOR BUILDING GREAT PRODUCTS

Gordon Bell, Vice President, Engineering

Product goodness is somewhat like pornography, it can't fully be described, but we're told people know it when they see it. If we can agree on heuristics about product goodness and how to achieve it - then we're clearly ahead. Five sets of dimensions for building great products need be attended to (roughly in order of importance):

- a responsible, productive and creative engineering group;
- product and design metrics (competitiveness);
- design goals and constraints;
- product evolution, revolution and death; and
- the ability to get the product built and sold.

ENGINEERING GROUP

As a company managed primarily by engineers, groups are encouraged to form and design products. With this right, are responsibilities.

The Team must have:

- a chief designer/chief programmer to formulate and lead the resolution of the problems encountered in the design; No matter how large the project, it must be lead from a "single head". We often make two errors in leadership: having no clear technical leader/problem resolver, and abdicating to a committee.

  Committees do not do design! They are never held responsible, nor are they rewarded or punished. Committees can review.

- management who understand the product space and who has engineered successful products; The two most important jobs are:
  - making sure that everyone knows their job; and
  - setting and reviewing work on a timely basis, ie. MBO.
- team skills and resources to implement the proposal so that we adhere to the cardinal rule of Digital, "He Who Proposes, Does"; A plan must include the chief designer, team, project organization and resources (eg. computers). Supporting skills and disciplines are essential in the respective product areas, eg. ergonometrics, acoustics, radiation, microprogramming, data bases, security, reliability.
- an understanding of the design, design production (eg. CAD) processes, and manufacturing processes; Learning curves apply to all processes! The organization must be staffed with people who understand the product, the design process (CAD and management discipline) and the production introduction process. One or two out of three isn't enough.

Behaviorally, the team must:

- do it right the first time: Being correct has the highest payoff everywhere: timeliness, quality, lack of rework, and mfg. cost.
- execute the project in a timely fashion: Virtually ALL of our projects are late because we start too late, don't get it done on time because some critical invention is required, take too long to get it introduced, etc. For the very long, very late projects, the failure is lack of planning, tools and organization. Finally, people burn out. This suggests we:
  - limit projects to two years by a small team. We often make an aggressive business plan, then hire the team. They then find out they have neither tools nor technology to do the project.
  - not predicate a project on scheduling inventions in the design, process and CAD areas. If we can't see how to do the work in 2 years, then let's not start the project! This means the product must be cut down to fit the tools, people and process. Advanced developement is to insure that we can do development.
- have a written design methodology that includes: all design processes in the form of manuals, design conventions, conflict resolution, criteria for task completion, PERT structure, etc.;
- be open and have external reviews, and clearly written product descriptions for inspection: For new product areas, we require breadboards in addition to the above heuristics. When the product gestation time equals the generation time, a full advanced development effort is the only way to be successful.
- start small, be reviewed and grow on its demonstrated success;
- learn, in order to handle the increase in complexity that comes with technology. Until there's a formal sabbatical program, individuals would do well to consider taking the equivalent of a semester of technical courses each 10 years.

PRODUCT METRICS KNOWLEDGE includes:

- products for which there'll be no competitor;
- all product cost metrics (cost, cost of ownership, cost to operate and use);
- all product performance and cost/performance metrics; These are the goodness measures of a product and tell how easily it will be to sell, and if we have improved. Cost and performance is measured against a state-of-the-art line represented by the first shipment of a more advanced product. Alternatively, when there's no direct comparison, the time goodness is determined from the day the product could have shipped. For example, because of parts availability, Nebula and CT could have shipped two and three years ago based on component availability.
- reasons why the product will succeed against present and likely future competition; sure success in the market is to introduce a needed function (eg. 32-bit address) by which all other products have to be measured.
- major competitor products by cost, performance and functionality; This should cover the past and future five years.
- leading edge, innovative, small company products;
- productivity, quality and design process metrics for projects.

DESIGN GOALS AND CONSTRAINTS

Design constraints are generally set as various kinds of standards. These are useful because they limit the choice of often trivial design decisions, and let us deal with important free choices, the goals. Goals are vitally important because they target our uniqueness.

Poor "mind-set" standards can create poor products, even though they may have made sense at one time. The historical English measures is a good case in point. Currently, the 19" rack and the metal boxes Digital makes to fit in them, and then ship on pallets to customers, act as constraints on building cost-effective PDP-11 Systems. This historical "mind set" standard often impedes the ability to produce products that meet the 20% per year cost decline curve.

- Goals and constraints must be written down and updated from the day the project starts. Virtually every product failure and period of product floundering is a result of no clear goals and constraints since everyone has a different idea of the product.
- A product can only have a few goals and constraints. The ranking is usually: it must work and have improved cost of ownership, be the shortest time to market, highest performance and lowest cost.

We must adhere to standards which we either follow or set!

- If a standard exists, follow it or change it for all! We lost the IEEE Floating Point format. It is likely we will eventually have to support it.
- If a standard is forming go all out to set it. When formed, then follow it. We didn't make DDCMP a standard. When HDLC came, we didn't use it. The result: expensive, low performance products.

Standards can be grouped into four distinct sets:

- DEC Engineering Standards; These cover most physical structures and design practice for producibility, and assimilate critical external standards, such as UL, VDE, and FCC.
- professional society, industry and area information processing standards, from EIA, CBEMA, ECMA, ANSI, ISO etc. such as Cobol '74, Codasyl, IEEE 488;
- defacto industry wide information processing and communication standards such as IBM SNA, Visicalc;
- standards implied by the architecture of existing DEC products to insure our customer software investments are preserved include:
    - architecture of computers, terminals, mass store and communications links; Our current ISP's include 8, 11's, 10/20, VAX, 8048, 8080, 8086, 68000; VT52, VT100, keyboards, Regis; MCP; HDLC, C1, N1, S1.
    - physical interconnect busses for computers and for interconnecting them CT, Q, U, N1, C1, etc. These insure that future system products can evolve from component and computer options between generations.
    - operating system interface file commands, command language, human interface, calling sequence, screen/form management, keyboard, etc.

- Products must be designed for easy translation into in any natural language since we are an international company.
- All products must have be customer installable and maintainable.
- Portability is an important goal. Personal computers must be portable! We must achieve this for all systems ASAP!

WHEN TO CREATE, WHEN TO EVOLVE AND WHEN TO STOP PRODUCTS

Engineering is responsible for designing evolutionary products in our markets AND for producing products that are natural to our tradition of supplying the most interactive, cost-effective computing. If a new product such as personal computing emerges and we do not have a product, engineering has failed, independent of being asked for it!

Given all the constraints, can we ever create a new product, or is everything just an evolutionary extension of the past? If revolutionary do we know or care where product ideas come from? The important aspect about product ideas is:

- Ideas must exist to have products! If we don't have ideas to redefine or extend a market, then we should not build a product.

It is hard to determine whether something is an evolution or just an extension. The critically successful products are likely to occur the second time around. Some examples: PDP 6,KA10,KI10,KL10,2060; Tops 10,Tenex,TOPS20; PDP5,8,8S,81/L,8E/F/M; OS8-RT11; 11/20,40,34,44; RSX-A... M, M+; TSS-8,RSTS; various versions of Fortran, Cobol and Basic follow this; LA30,36,120; VT05,50/52,100, 101 etc.; RK05,RL01/2.

- A product tree MUST be maintained by each engineering group showing roots, gestation time and life.

Goodness and Greatness

All products whether they be revolutionary, creating a new base, or evolutionary, should:

- be elegant and high quality: Russ Doane's working definition is: "every feature contributes two benefits", like a double pun. Quality means no excess. Elegant, high quality designs, do double duty with a minimum use of resources. Quality is also the absence of errors, by being right the first time so that it doesn't have to be inspected or redone.
- offer at least a factor of two in terms of cost-effectiveness over a current product; We have classic failures because a CPU cost has been minimized, only to find the total system cost has barely changed 10% and the total cost to the customer is only 5% lower! If each product is unique then we will have funds to build good products.
- be based on an idea which will offer an attribute or set of attributes that no existing products have; For example, the goals and constraints for VAX included factor of two algorithm encoding and also offering ability to write a single program in multiple languages. VT100 got distinction by offering 132 columns and smooth scrolling.
- build in generality, and extensibility: Historically we have not

been sufficiently able to predict how applications will evolve, hence generality and extensibility allow us and our customers to deal with changing needs. Extendable products also permit mid-life kickers to products. We have built several dead end products with the intent of lower product cost, only to find that no one wants the particular collection of options. In reality, even the $200 calculators offer a family of modular printer and mass storage options. For example, our 1-bit PDP-14 had no arithmetic ability, nor could it be a general purpose computer. As customers used it, ad hoc extensions were needed to count, compare, etc. and it finally evolved into a really poor, general purpose digital computer.

- be a complete system, not piece parts; The total system is what the user sees. A word processing system for example includes: memory, keyboard, tube, modems, cpu, documentation including how to unpack it, the programs, table (if there is one, if not then the method of using at the customer table), and shipping boxes.
- be a great system because the components are great; We should not depend on system markups and software functionality to cover poor components and high overhead.
- if we don't make it, buy it; We must carefully decide what components to make versus buy. It is very hard for an organization to be competitive without competing in the marketplace, hence unless we sell it, we should buy it.

Product Evolution

A product family evolution is described on page 10 of Computer Engineering along the paths of lower cost, and relatively constant performance; constant cost and higher performance; and higher cost and performance. In looking at our successful evolutions:

- lower cost products require additional functionality too; A lower cost product, with constant performance or constant function is risky because a new customer base and new way of marketing may be required. Some other company may, however, be successful with the concept. The PDP-8, based on new technology, was radically more successful than its higher priced predecessor, the PDP-5, because it was 2/3 the price and 6 times more performance. The PDP-8/S was a failure at 2/3 the price and 15 less performance than the PDP-8. There are similar stories about the LA 34, VT50/52 and PDT as replacement products.
- constant cost, higher performance products are likely to be the most useful; Economics of use, the marketing channel and customer base are already established and a more powerful system such as the LA120 will allow higher productivity (see Computer Engineering for the understanding and economics). In the 11's there was a successful evolution: 20, 40, 34 anChied 44. Not the 60. The 11/70 was probably our greatest success; it was billed as a mid-life kicker to the 11/45-55.

Revolutionary New Product Bases

- A new product base, such as a new ISP, physical interconnection, Operating System, approach to building Office Products, must

start a family tree from which significant evolution can occur. The investment for a point product is so high that the product is very likely not to payoff. In every case where we have successful evolutionary products, the successors are more successful than the first member of the family. Point products with no follow-on will probably fail all roi tests.

Product Termination

- A product evolution is likely to need termination after successive implementations, because new concepts in use have obsoleted its underlying structure. All structures decay with evolution, and the trick is to identify the last member of a family, such as the 132 column card, and then not build it. This holds for physical components, processors, terminals, mass storage, operating systems, languages and applications. Some of the signs of product obsolescence:
  - It has been extended at least once, and future extensions render it virtually unintelligible.
  - Better products using other bases are available.

SELLING AND BUILDING THE PRODUCT

"Buy in" of the product can come at any time. However, if all the other rules are adhered to, there is no guarantee that it will be promoted, or that customers will find out about it and buy it. Some rules about selling it:

- it has to be producible and work, AND be useful to software; This, although seemingly trivial rule, is often overlooked when explaining why a product is good or not. If it is a piece of hardware that requires software to support it, the hardware must be available to the programmers who must support it. Software engineers approach new hardware with much caution! The often ask: is it significant? is it needed? why isn't it compatible with the past? If a hardware is viewed with distrust by software engineers it may be met with the same distrust by customers!
- a business plan with orders and marketing plans from several marketing persons and groups needs to be in place; Just as it is unwise to depend on a single opinion in engineering for design and review, it is even more important that several different groups are intending to sell the product. Individual marketers are just as fallible as unchecked engineers. This rule can and must be violated for revolutionary products!
- never build a product for a single customer, although a particular customer may be used as an archetype user; predicating a product on one sale is the one sure way to fail! Paraphrasing a remark by former GM executive Charles Wilson: if it's good for General Motors, it may only be good for GM.
- it must be done in a timely fashion according to the committed schedule, price and functions as previously described;
- it must be understandable and easy to use. The small size, complete hardware books were the DEC trademark that established the minicomputer. We must revive these such that a particular user never need access more than one. Simplicity must be the

rule for our documentation.

What heuristics are missing? What heuristics do you disagree with?

What heuristics could be removed? reordered?

Could I please have your feedback before this becomes a final draft?

3/15/82 Mon 8:47
GB3.S2.5

DESIGN GOALS AND CONSTRAINTS

- GOALS AND CONSTRAINTS MUST BE WRITTEN DOWN AND UPDATED FROM THE DAY THE PROJECT STARTS.

- A PRODUCT CAN ONLY HAVE A FEW GOALS AND CONSTRAINTS. THE RANKING IS USUALLY: IT MUST WORK AND HAVE IMPROVED COST OF OWNERSHIP, BE THE SHORTEST TIME TO MARKET, HIGHEST PERFORMANCE AND LOWEST COST.

- IF A STANDARD EXISTS, FOLLOW IT OR CHANGE IT FOR ALL!

- IF A STANDARD IS FORMING GO ALL OUT TO SET IT.

- PRODUCTS MUST BE DESIGNED FOR EASY TRANSLATION INTO IN ANY NATURAL LANGUAGE SINCE WE ARE AN INTERNATIONAL COMPANY.

- ALL PRODUCTS MUST HAVE BE CUSTOMER INSTALLABLE AND MAINTAINABLE.

- PORTABILITY IS AN IMPORTANT GOAL.

ELEGANCE: WHAT IS IT?

RUSS DOANE: "EVERY FEATURE CONTRIBUTES TWO BENEFITS"

RH DICTIONARY: "GRACEFULLY REFINED, DIGNIFIED, OF HIGH QUALITY"

QUALITY = LACK OF EXCESS (ESPECIALLY ERRORS)

ELEGANT DESIGN IS THE USE OF A PART TO PERFORM MANY FUNCTIONS.

ARCHITECTS SAY: "LESS IS MORE."

SOME EXAMPLES: THE STORED PROGRAM COMPUTER (USE OF MEMORY), THE GENERAL REGISTERS, THE UNIBUS, PASCAL, APL.

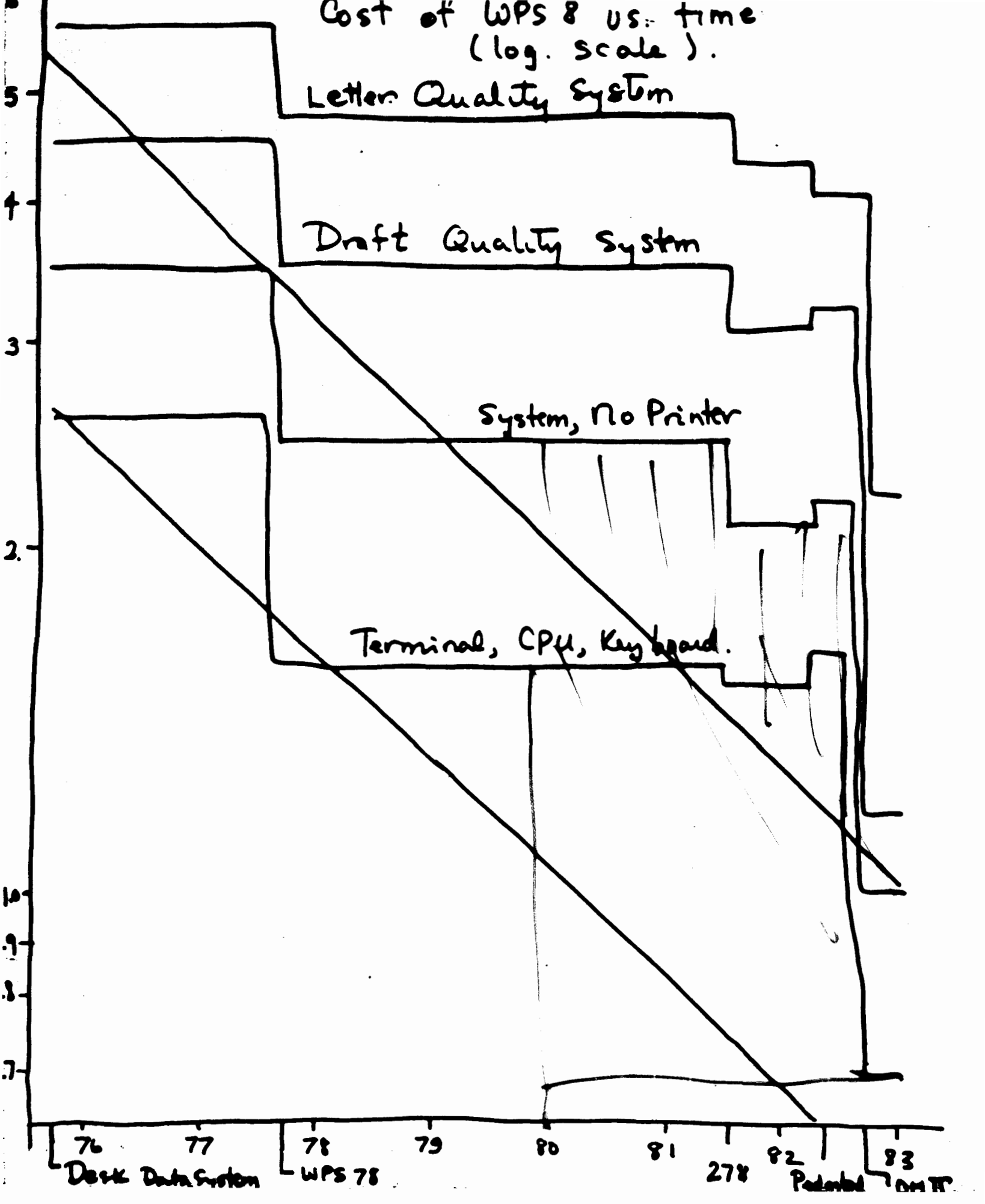
SEVERAL PIONEERS: "LEAVE A FEATURE OUT THAT CAN BE DONE ANOTHER WAY."

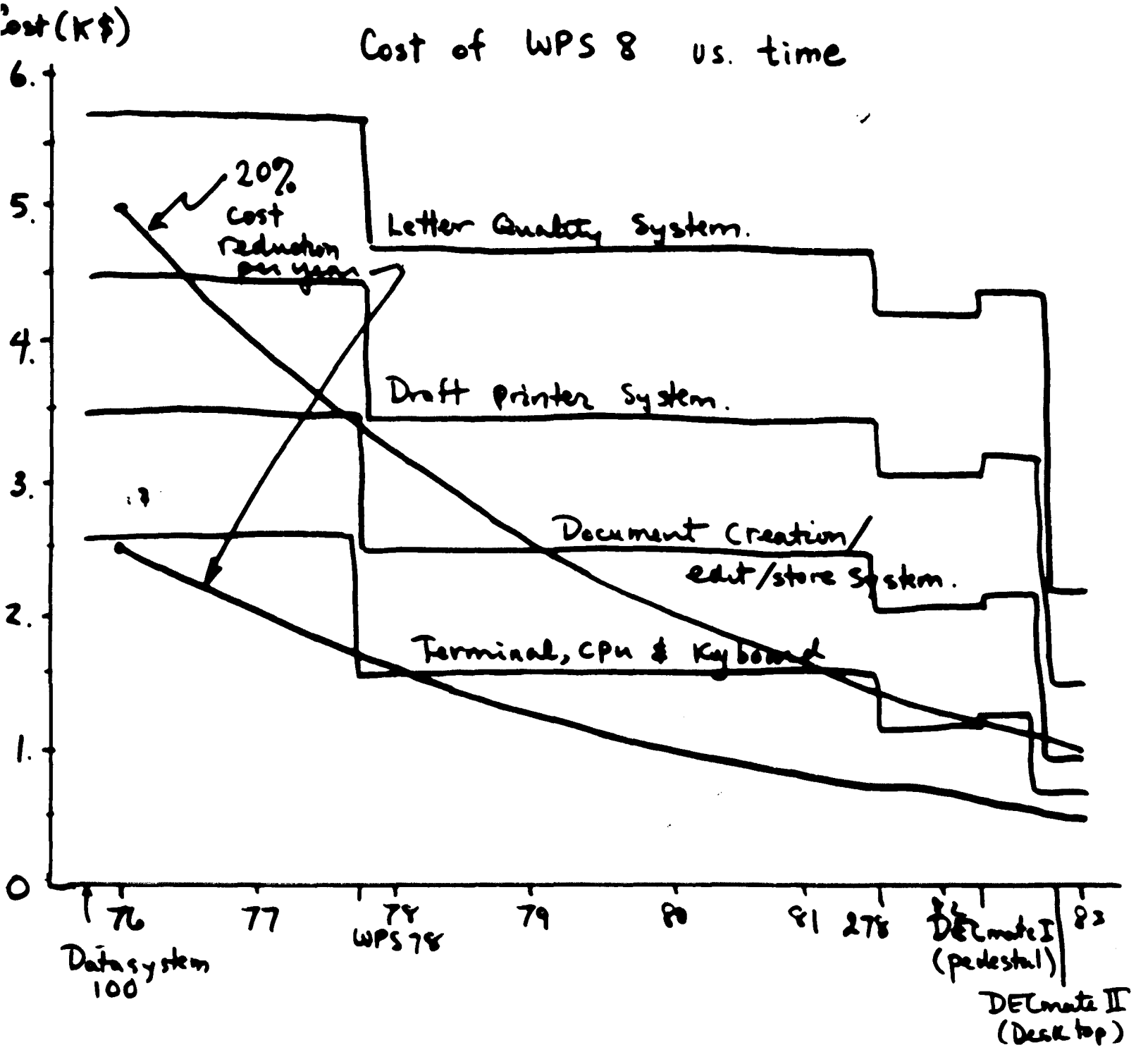
IT CAN SOMETIMES CONFLICT WITH OTHER GOALS LIKE ORTHOGONALITY.

BUT TOO MUCH ELEGANCE IS TRICKERY.

Great Systems are Built On Quiet Corp.

System	DEC 100	WPS 78	WPS 278	DECmate I	DECmate II
Package	desk	stand	stand	pedestal	table top
What	8/A	CPU in	6102+video	6120+video	-
	VT52	VT52 base	VT100 box	VT100 box	monitor
	RX01	RX01	RX02	RX02	RX50+6120
When	9/75	9/77	6/81	3/82	9/82
Performance	1	.3	.75	.75	1
base cost	3.5	2.5	2.1	2.2	1.0
base+dp	4.5	3.5	3.06	3.2	1.5
base+lqp	5.7	4.7	4.26	4.4	2.2
CPU only+crt	2.6	1.6	1.2	1.3	.7
floppies	.9	.9	.9	.9	.3
cost/perf	3.5	8.3	2.8	2.9	1.0
cost/perf@					
20% on 3.5	3.5	2.2	.9		.72


Cost of WPS 8 vs. time
(log. scale).
Letter Quality System
Draft Quality System
System, No Printer
Terminal, CPU, Keyboard.
5
4
3
2.
1.0
.9
.8
.7
76
77
78
79
80
81
82
83
Desk Data System
WPS 78
278
Personal


Cost (K$)
Cost of WPS 8 vs. time
6.
5.
4.
3.
2.
1.
0
20% cost reduction per year
Letter Quality System.
Draft printer System.
Document Creation/ edit/store System.
Terminal, CPU & Keyboard
76
77
78
WPS 78
79
80
81
278
DECmate I (pedestal)
83
DECmate II (Desk top)
Datasystem 100

WHEN TO CREATE, WHEN TO EVOLVE AND WHEN TO STOP PRODUCTS

- IDEAS MUST EXIST TO HAVE PRODUCTS! IF WE DON'T HAVE IDEAS TO REDEFINE OR EXTEND A MARKET, THEN WE SHOULD NOT BUILD A PRODUCT.

* - A PRODUCT TREE MUST BE MAINTAINED BY EACH ENGINEERING GROUP SHOWING ROOTS, GESTATION TIME AND LIFE.

GOODNESS AND GREATNESS = NO CRAPPY PRODUCTS

* - BE ELEGANT AND HIGH QUALITY;

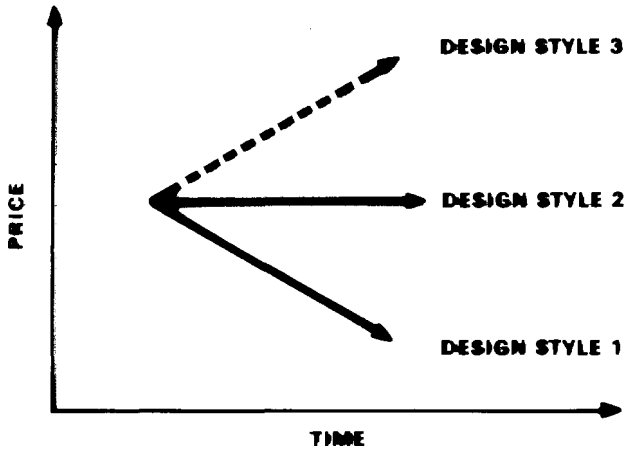
- OFFER AT LEAST A FACTOR OF TWO COST-EFFECTIVENESS OVER A CURRENT PRODUCT;

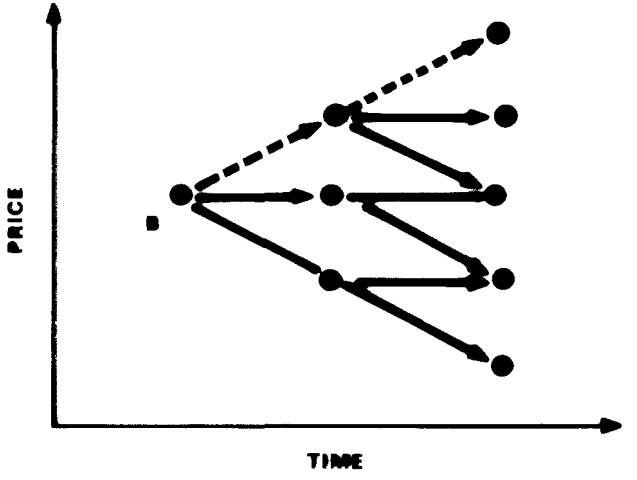
- BE BASED ON AN IDEA WHICH WILL OFFER AN ATTRIBUTE OR SET OF ATTRIBUTES THAT NO EXISTING PRODUCTS HAVE;

- BUILD IN GENERALITY, AND EXTENSIBILITY;

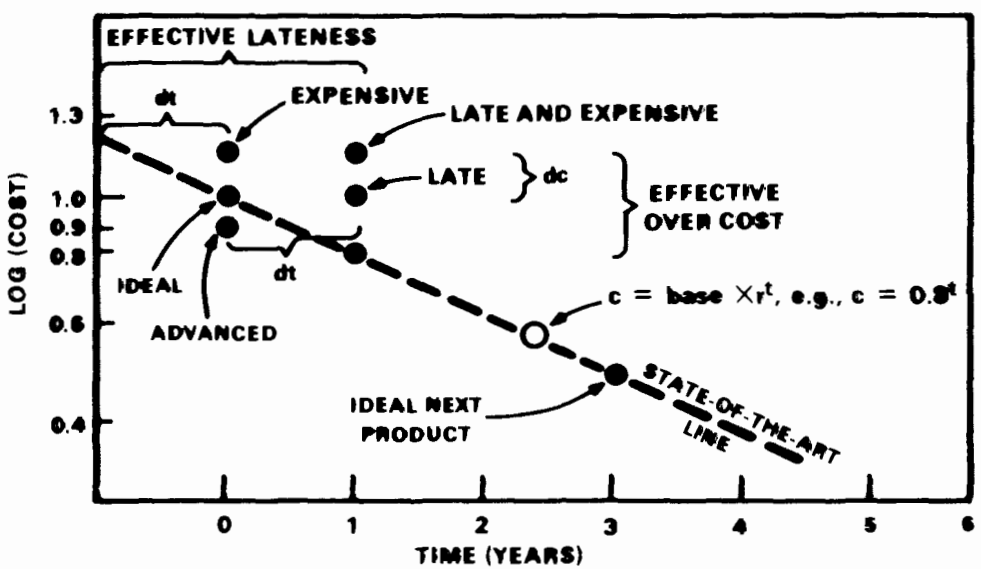
* - BE A COMPLETE SYSTEM, NOT PIECE PARTS;
- BE A GREAT SYSTEM BECAUSE THE COMPONENTS ARE GREAT;

- IF WE DON'T MAKE IT, BUY IT;


DESIGN STYLE 3
DESIGN STYLE 2
DESIGN STYLE 1
PRICE
TIME


PRICE
TIME

1- FIG. 9,10


EFFECTIVE LATENESS
dt
EXPENSIVE
LATE AND EXPENSIVE
LATE
dc
EFFECTIVE OVER COST
IDEAL
ADVANCED
dt
c = base ×r^t, e.g., c = 0.8^t
IDEAL NEXT PRODUCT
STATE-OF-THE-ART LINE
LOG (COST)
1.3
1.0
0.9
0.8
0.6
0.4
0
1
2
3
4
5
6
TIME (YEARS)

2 - FIG. 25

Product Evolution

- Lower cost products require additional functionality too;
- Constant cost, higher performance products are likely to be the most useful;

Revolutionary New Product Bases

- A new product base, must start a family tree from which significant evolution can occur.

Product Termination

- A product evolution is likely to need termination after successive implementations, because new concepts in use have obsoleted its underlying structure.

PRODUCTS THAT HAVE NOT MET EXPECTATIONS

PDP-8/S

VT8/E (REUTERS), VT14 (FOR PDP-14, + PDP-14)

VT30 ETC. (CSS)

VT15, GT40, GT60, MEGATEK BUYOUT (ENG P/L)

VSV11 (LDP AND CSS)

VT20, 21, 61T, 71, 171 (TYPESETTING P/L)

LA36/BSR, LA36/TU60, LA120/TU58 (ATT)

MINC, MINI-MINC (LDP P/L) — but profitable.

PDT 110, 130 150 (SPECIALIZED CUSTOMER)

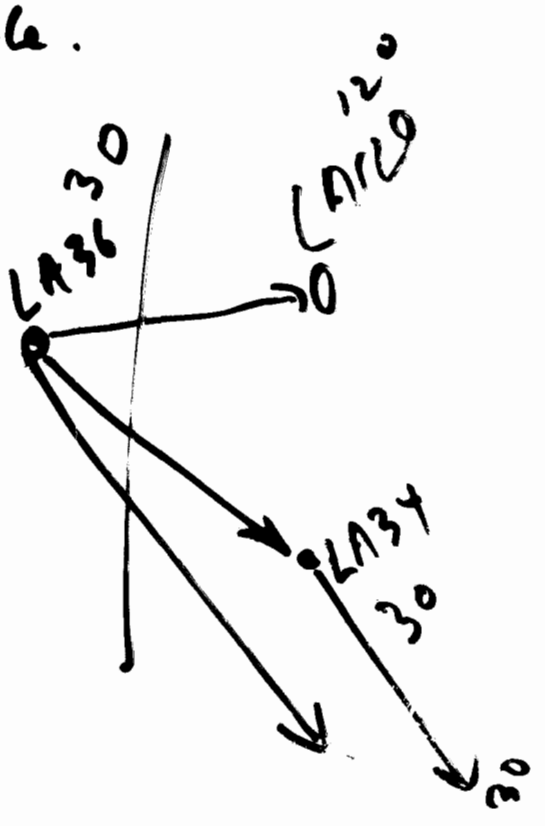
GIGI (EDU P/L)

VT103 (TPG)

11/60, DS315, 11/23

LA34 → LA120

WS100, WPS78, WPS 278, DECMATE I? (WPS P/L)



PITFALLS OF LOW END PRODUCTS

- Customer specialized
- Specialized market not doable with GP Terminal or System
- Done on a limited budget. Just enough spending to lose.
- Marketing Demands It. Engineering Designs It.
- Poor engineering leadership to provide the right solution
- Poor solution compared to competition
- Inadequate product support in marketing or engineering

SELLING AND BUILDING THE PRODUCT

- IT HAS TO BE PRODUCIBLE AND WORK, AND BE USEFUL TO SOFTWARE;

- A BUSINESS PLAN WITH ORDERS AND MARKETING PLANS FROM SEVERAL MARKETING PERSONS AND GROUPS NEEDS TO BE IN PLACE;

- NEVER BUILD A PRODUCT FOR A SINGLE CUSTOMER,

- IT MUST BE DONE IN A TIMELY FASHION ACCORDING TO THE COMMITTED SCHEDULE, PRICE AND FUNCTIONS;

- IT MUST BE UNDERSTANDABLE AND EASY TO USE.

MAR 11 1982

DESIGN for the 80's

ENGINEERING DESIGNER LECTURE SERIES

TOPIC: THE HEURISTICS IN BUILDING GREAT PRODUCTS: PAST AND PRESENT

SPEAKER: C. GORDON BELL

GORDON IS THE VICE PRESIDENT OF ENGINEERING AND FOR MORE THAN TWENTY YEARS HAS BEEN A LEADER IN THE DEFINITION AND DESIGN OF MANY OF DIGITAL'S PRODUCTS.

TOPIC: THE APPLICATION OF SOFTWARE ENGINEERING TECHNIQUES TO HARDWARE DESIGN

SPEAKER: EARL C. VAN HORN

EARL IS AN EXPERIENCED DESIGNER AND PROGRAMMER OF SOFTWARE SYSTEMS, WITH ADDITIONAL BACKGROUND IN COMPUTER HARDWARE DESIGN, MODELING, AND SYSTEM ARCHITECTURE. SINCE JOINING DIGITAL'S CORPORATE RESEARCH GROUP IN 1976, HE HAS WORKED ON THEORETICAL AND PRACTICAL ASPECTS OF SYSTEM DESIGN METHODOLOGY. HE WAS PROJECT LEADER FOR ADVANCED DEVELOPMENT OF THE DEC/CMS PROGRAMMING LIBRARY SYSTEM. CURRENTLY HE IS MODELING A PORTION OF A NEW CPU.

EARL RECEIVED HIS PH.D. IN ELECTRICAL ENGINEERING FROM M.I.T., WHERE HE WORKED ON OPERATING SYSTEM AND VIRTUAL MEMORY CONCEPTS AND ON DETERMINISTIC PARALLEL PROCESSING.

TIME: 1:30 P.M.

DATE/PLACE:

MARCH 19, 1982 - FUNCTION ROOM ML5-4
MARCH 26, 1982 - DEC 10/20 CONF. RM. MR1-2
MARCH 30, 1982 - BABBAGE AUDITORIUM ZK

Leadership !

NOV 19 1981

****
* d i g i t a l *
****

INTEROFFICE MEMORANDUM

TO: GORDON BELL

DATE: 16 NOVEMBER 1981
FROM: RON CADIEUX
DEPT: ADV MFG TECH
EXT: 223-7189
LOC/MAIL STOP: ML1-5/T55
NO: #13/1.42

SUBJECT: PARTICIPATION IN DESIGN FOR THE 80'S LECTURE SERIES

Thank you for agreeing to present a lecture on "Heuristics In Building Great Products: Past And Present" as a part of the "Design for the 80's Lecture Series." Three hours have been allocated for this lecture and Earl Van Horn's, please allow at least a 15 minute question and answer period.

Your lecture is scheduled for presentation as follows:

DATE	TIME	PURPOSE	LOCATION
TBD	TBD	Dry Run	TBD
3/19/82	1:30	Presentation to Engineers in the Maynard area (this session will be video taped).	Function Rm. ML4-5
3/26/82	1:30	Presentation to Engineers in the Marlboro area.	DEC 10/20 Conf Rm MR1-2
3/30/82	1:30	Presentation to Engineers in the Tewksbury & southern N.H. area.	Babbage Aud. ZK

The attached guidance will provide you with more details on the purpose of this lecture series and in the procedures which have been established.

If you have any questions or need further assistance, please don't hesitate to call me or Barbara Hein at 223-3457.

Gordon,
your topic has already stirred a lot of interest & think we can expect a big turn out. If there is anything I can do to help give me a yell.

Ron

GUIDANCE TO LECTURERS

The purpose of the Design for the 8Ø's Lecture Series is to introduce our engineers and designers to a wide variety of topics of critical interest to them and the corporation as a whole. You are not expected to turn your audience into experts in the short two hours that has been alocated for this lecture. Rather your lecture should be designed to introduce your audience to the topic, make them aware of the importance of the subject to the corporation, and to motivate them to do more indepth study of this topic on their own. If you are successful in your presentation your audience will walk away with the following:

- a general knowledge of the subject including some of the basic principals involved.
- a knowledge of what's going on around central engineering in relation to this topic and who to call for help.
- a feeling that this is important to them and the corporation and that they should learn more about it.

This lecture provides an excellent opportunity for you to transmit "lessons learned" from one part of Central Engineering to other parts. You are therefore encouraged to add examples of problems and their solution from your experience with this topic at DEC. In the fast moving world of computer technology, we can not afford to reinvent the wheel or to go chasing down a rat hole that someone else has already explored.

HELP

To assist you in the preparation of your lecture we have arranged for the services of Ray Slesinski from Sales Training. Ray is an instructor in the Effective Presentations Course which is offered by Sales Training. He has developed a check list to help you in preparing your presentation and will be available to help you in any way possible. If you wish he can arrange for you to video tape your lecture during a practice session so that you can review and critique your presentation on your own. Ray will be contacting you shortly, if your have any questions in the interum he can be reached at DTN 264-7432.

DRY RUN

A requirement has been established for this lecture series that each lecture must be dry run before a selected panel before it is presented to the general audience. The purpose of this dry run is to ensure the effectiveness of the lectures being presented to our engineers and designers. The dry run panel will be composed of one or more members of the engineering staff, several technical experts and Ray Slesinski from Sales Training.

VIDEO TAPING

Your first lecture before a live audience will be video taped and made available to the entire Digital engineering community through the Corporate Library. This is being done because we feel that the topic you are presenting is of vital interest to the engineering community as a whole and we don't want people to miss out on it simply because they were unable to attend one of your live lectures.

HAND OUTS

There is no need for you to prepare and distribute multiple copies of your presentation. Simply provide one clean copy of your presentation to Barbara Hein at the time of your first lecture. She will see to it that the handout is duplicated and distributed to all attendees. It is suggested that you also prepare a bibliography of additional readings on your topic for us to distribute to all attendees after the lecture.

The lecture you will be presenting may reach several hundred of our key engineers and designers during the live presentations and may well be viewed by 500 to 1,000 more via the video tape you are preparing. We feel that this is a unique opportunity for you to reach a large segment of Digital's engineering community with your message. --- Good Luck! and thanks for agreeing to present this lecture.

Circ Eng. Staff V Jean

MAR 3 1 1981

+---------------+
| d i g i t a l | INTEROFFICE MEMORANDUM
+---------------+

TO: Gordon Bell ML12-1/A51

CC: Dave Brown ML1-3/E58
Jack Knott ML1-3/E63

DATE: 26 Mar 81
FROM: Paul Kinzelman
DEPT: Tape Engineering
EXT: 3-2473
LOC: ML1-3 E63

SUBJ: RESPONSE TO YOUR PRODUCT STRATEGY MEMO

I recently saw a copy of your memo dated 5-MAR-81 entitled: "Winning, Great Products: A Constraint on our Product Strategy." I would like to reply to your memo.

First of all, your memo sounds great. I am sure we would all love to design only winning products. I understand that from your point of view, all products should be super. I am obviously not going to defend "crappy" products, but I think that placing the blame and responsibility purely on engineering is too simplistic.

I would like to use as an example the TS04/TS-11 project, with which I have been associated from almost the beginning to the end. My responsibility was to write most and to support all of the microcode and tools used during the project. I think this project is quite revealing because the TS-11 also wound up a year or two late and very over budget.

The TS11 was supposed to be a very cheap, reliable, and easy to fix drive. The way to make the drive cheap to fix and the boards easy to debug is to have a lot of small boards. However only one logic engineer on the project had any experience running fast busses among many boards. His previous company set up a special group to breadboard the physical machine with board connectors and special circuitry to evaluate the quality of the machine layout. We didn't have the expertise and we didn't have the money or time to do this evaluation, so we made some educated and some not so educated guesses. Hindsight shows us we went after an impossible goal: fast busses going thru many connectors and non-multi-layer cheap boards. We didn't know we couldn't do it until we tried.

Rule

The result was that we were thrown out of DMT due to flaky errors, etc. For the next two years, the project was in panic mode. An engineer can't design well in panic mode. The thought is "how little can I change to get the thing thru DMT?" In developing a project, the engineer should be thinking, "What would I like to see if I were to use the box?" In the end, we probably spent as much money as we would have spent if we had taken the time to do the research at the beginning of the project. My positive suggestion is to take the time to investigate a new approach

before committing a project to that approach. Be willing to acknowledge that a project using a new approach may have to be scrapped or have goals reevaluated.

Another thing that plagued the TS11 project was the amount of plus 1's. As I understand from those that were there, you added in a few of your own. Plus 1's almost always increase the time to do a project even over the time the project would have taken if the plus 1's were specified at the beginning of the project.

The result of the TS11 project is a drive that is medium priced with a maintenance that is quite a bit cheaper than any other drive on the market. Unfortunately, the thing is single density. Also, there are newer and greater tape technologies. We can't expect TS11's to sell that well, coming out 8 years after IBM has come out with the next technology (GCR).

Because the TS11 contract cost is so much less than the contract cost of competing drives, the sales people should be selling the TS11 by emphasizing this advantage. Since most people go on field service contract, the over-all 5 year cost might be quite a bit cheaper than any competitor. I hear reports that the sales force is trying to sell the TS11 on base price alone. And so the TS11 doesn't sell well, and engineering gets another black eye.

Another point is that DEC only goes into a technology, GCR for instance, years after several other companies have achieved a high level of excellence in the specialty. DEC's forte is quality computing for a low price. We wait until others have a technique down pat and then we try to do the same task with newer devices for less money. But these other companies have spent a lot of money developing these technologies and that's why their products are expensive. When we jump into new technologies, we must develop expertise. Developing this expertise costs money. The funding and schedule is appropriate for a group that has the expertise and must merely churn out another drive or whatever. And so we are chastised for missing the schedule because the new technology contains some surprises.

Even doing buy-outs does not solve the problem. Take the TU77 and TU78 as an example. At the time, Pertec was the only reliable company that had a useable drive, although the drive had many problems. By the time other companies had come out with a similar drive, we were committed to staying with Pertec. If we could have afforded the time and money, we could have gotten a better drive a couple of years later. The TU77 has been a real problem in the field and the TU78 is basically the same drive. Several people here have spent a lot of time helping Pertec fix their drive. Again these people have been operating in panic mode. And when these people find a problem, they must then convince Pertec to fix the drive. We couldn't afford the time to switch to a better drive so we spent the same time helping Pertec for free.

I have observed that most marketing input (when it's there) comes

based upon marketing's opinion and possibly analysis of the competition. Marketing is supposed to provide market information, not competitor information. I don't need marketing to order and read manuals from the competition. I need analyses of what the marketplace needs. A case in point comes from terminal engineering who never did find any customer capable of testing a half-duplex feature that marketing said was a "gotta have."

As to Andy (Knowles?) not buying into the CT project, where was he when the engineers were sitting down and specifying what the CT would do? Now, I don't know the details, but he should show an interest in the project at the start, when his input is useful. He, too, should take some responsibility for the project being the best the engineers can do. We engineers need help in specifying what to design. We don't need inside buyers who only come in at the end and say they don't quite like a product.

Years ago, the TOPS-20 engineers asked the marketing people for input and got nothing. When the project's first release was done, a marketing person came up and said that he didn't quite like TOPS-20. Where was he during the design?

As an engineer, I would like nothing better than for marketing people, or anybody else for that matter, to come to me during the beginning of a project and help specify what the project should look like.

The result of all this is that the engineer and the engineering manager become the scapegoats. We in the engineering department need support from the marketing area. Too often, the engineering department is left to specify the product because of the lack of marketing input until it's too late. We don't have the money, budget, or schedule flexibility to adjust to marketing's input when the input comes too little and too late.

Engineering must not be blamed for changing expectations during the course of a long project. Let's realize that it's nobody's fault, work to change the product, and allow more time and money for the project. Don't allow the project development to fall into panic mode.

We must also be willing to spend the money to develop expertise in a chosen field. Somehow, most DEC products end up being done in panic mode. I believe you cannot develop any expertise while in panic mode. The solution to developing expertise is to develop a product out of panic mode by spending the money at the beginning to do the project right.

Heuristics

V

+---------------+
! d i g i t a l ! I N T E R O F F I C E M E M O R A N D U M
+---------------+

TO: Gordon Bell ML12-1/T51

DATE: 21 Apr 81
FROM: Paul Winzelman PNW
DEPT: Tape Engineering
EXT: 3-2473
LOC: ML1-3 B63
DECNET: STORS::KTWZELMAN

SUBJ: RESPONSE TO YOUR HEURISTICS MEMO

I read over your memo several times and have a few comments and suggestions.

The overall tone I get from your memo is that the engineer is responsible not only for designing the product but also for knowing what specs the the project should have to best fit the market. I think marketing should take much of the responsibility for the specification of the project due to market constraints. I never talk to salesmen in the field and so I don't know what the field wants. I need to be able to depend on marketing for this information and for critical input based on the market. Marketing should get involved with projects a lot more than I have seen or heard them get involved in the past. I believe that this lack of marketing input to be the most critical problem we engineers have.

Once the market has been identified and the necessary specs generated, the engineer should have a lot of flexibility as to the specific implementation. I think that a good philosophy for an engineer to follow when designing a procuce is "What would I like to see in the product if I had to use it when I'm done?" I think that approach creates a much greater personal commitment to excellence of implementation.

You specify the need for reviews in several places. I think in addition, the marketing people who specified the product and the product lines who are going to buy the product should come over and actually see and use the breadboard. Hands on experience is always better and more meaningful than reading a dry spec. I think that this approach would reduce problems along the lines noted in your last memo concerning Andy not liking the CT project. I think communication and constructive criticism would increase. We need a working dialog with people knowledgeable about what the marketplace needs.

Concerning the rule, "he Who Proposes, Does," do you mean that if one proposes something, he must have on hand all the expertise to do the project? I thought you couldn't get funding or people for a project until you got a budget approved. Expertise is expensive and not always immediately available. If something is worth

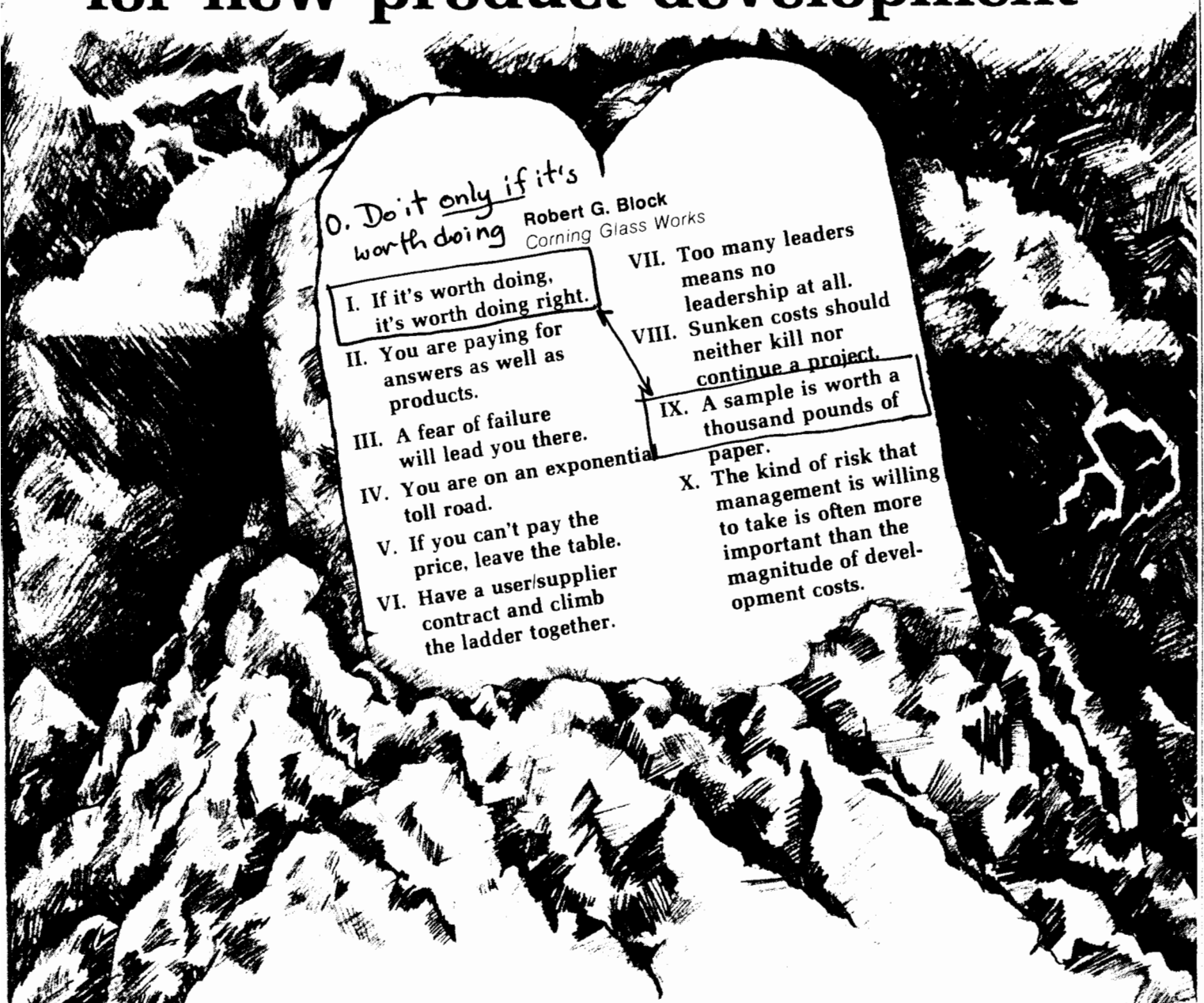
doing, expertise might have to be brought in after approval.

You write a lot about evolution and not building lower cost products without increasing functionality. I think we should divide the computer world into two product lines, those that must be highly compatible with the outside world (large tapes, for instance) and those that need not be compatible with the outside world (disks and terminals, for instance). All of what you said holds true for non compatible products, but do they hold true for compatible products? Most of the cost of a tape drive is in the area of circuitry that maintains compatibility. Most of the industry in tapes are just IBM watchers. We can build in more diagnostics, etc., but the basic drive must be IBM compatible. Since we are so constrained, could not a valid reason for another tape drive be that the price is low? I believe that the LCGCP project is only around because of price.

OC, PEG / Eng. Staff. + net Fyi. Gordon (courtesy of? who sent it to me)
Something for our conference room walls, if there's any room left.

Less wasted time and effort, better communications, a more productive development process, and happier people with a better attitude can result from following the . . .

ten commandments for new product development



Robert G. Block
Corning Glass Works

THE PRIME RESPONSIBILITY of today's Corporate Manager is to set that course which best insures the future health and survival of his business. There can be no doubt, then, that New Product decisions are some of the most important the manager must make. The New Product Development Process also presents him with his greatest challenge because it is: surrounded by many market and technical unknowns, not well understood and difficult to quantify, where success is the sweetest and failure the most bitter, and an area with a high potential for "gut" recommendations and subsequent decisions.

Without the luxury of solid information, the manager must rely on both his experience and *common sense* in new product de-

cisions. The "Ten Commandments" presented here provide a checklist for cutting to the quick on key issues and bringing to the surface the strengths and weaknesses in a new product portfolio. They apply equally well when viewed from a strategy/marketing, technical, or manufacturing standpoint at almost any organizational level.

0. Do it only if it's worth doing.

I. If it's worth doing, it's worth doing right

Doing product development right means:

- Assuring that each project has the proper resources to enhance its probability of success. The converse of this rule also holds: "If you can't do it right, it's not worth doing at all." Resource allocation must limit the number of projects such that they are all done well, rather than having too many done poorly.
- Reviewing projects periodically to ensure that resources, as applied to projects in the portfolio, are justified and that the portfolio balance is maintained when any projects are added or deleted.
- Establishing project stages with technical and marketing milestones as prerequisites for proceeding to the next stage.
- Allowing sufficient time to do a thoro marketing and technical job.
- Putting decisions regarding the development process at the organizational levels with "grass roots" technical and marketing understanding.
- Qualifying *all* products by in-use testing before introduction.

Doing things the right way will not guarantee technical and market success for the product concept. However, it does insure that the proper emphasis on the development provides both a good chance of success and the *answers* that are required for periodic decisions in development.

II. You are paying for answers as well as products

Think about how many times you have heard the following questions regarding new products:

- When can we have it?
- What are our chances of having it?
- Can the competition do it?
- What is our business strategy assuming we have the new product?
- What is our business strategy if we can't have the new product?

If you have heard or asked these questions, you know that the answers are sometimes as critical as the existence of the new product. In fact, a NO GO on a particular approach can, and often does, start the project and/or business off in a more fruitful direction. It is critical that new product developments be structured as decision trees with key GO/NO GO criteria.

If one accepts the fact that answers are sometimes as important as the products themselves, the prospect of failure can be organizationally accommodated and considerable wasted effort avoided.

III. A fear of failure will lead you there

The possibility of failure to develop a product must be recognized and its consequences accepted up front. Recognition of when it's time to call it quits can save much time and money. Questions concerning what can go wrong are as important as positive ones; they uncover potential "stoppers" for the development of the product, Furthermore, if there is an organizational atmosphere where failure is feared, the risks necessary to achieve success will not be taken.

The greatest failure in R&D is the unwarranted spending that can occur when funds are expended without having the proper technical and marketing foundation.

IV. You are on an exponential toll road

The development of a product can be broken into five stages with each being the foundation for the next:

- *Basic research.* The kind of technical knowledge building that occurs in broad scientific studies. Market needs are not specific during this stage.
- *Applied research.* Demonstration of the technical feasibility of a phenomenon. The market need is apparent and specific. An invention may be required.
- *Exploratory development/prototyping.* Demonstration of the commercial feasibility of a known technical phenomenon. A general product specification to meet a specific market need exists.
- *Manufacturing Development.* Demonstration of a manufacturing process capability regarding specifications and cost.
- *Production.* Manufacture of the product in volume.

As one proceeds up the scale, the probability of success increases and costs to achieve a given objective or product attribute grow exponentially. A good approximation is that $1 of new product change in research represents $10 in applied research, $100 in exploratory development, $1,000 in manufacturing development and $10,000 for a retrofit of production. This lesson has been learned by many, most notably the Department of Defense in their "total systems acquisition" concept of the 1960's with its concommitant cost overruns. It's no

wonder that resistance to change grows rapidly as a development proceeds.

Projects should be reviewed at each stage of their development to determine what changes in their probability of success have occurred and the ante required to provide good odds for subsequent project stages.

V. If you can't pay the price, leave the table

Product development is an educated gamble and requires the best marketing and technical judgment of the players. As the development process moves forward, fact replaces opinion and the odds improve. From a business standpoint, the total R&D program represents an investment portfolio of varying risks and payoffs.

The matrix diagrammed on this page represents the field to be played. Logically, one should always play above and to the left of the matrix diagonal. However, this in turn requires that enough money be laid down to assure odds consistent with expected payoff.

VI. Have a user/supplier contract and climb the ladder together

As stated earlier, each project should have marketing and technical milestones as prerequisites for subsequent stages.

Marketing, as the user, owes the R&D organization a product specification and well founded market estimates to insure that technical efforts will not be wasted. If R&D accepts the challenge to develop the product, it owes Marketing an honest appraisal of the probability of technical success and a willingness to flag critical events. As the development process moves through the various stages described under the Fourth Commandment, the level of precision requires of both parties becomes much more stringent.

New products have a tendency to gather crowds. They are not only exciting, but generally have a significant impact on business strategy. Care must be taken to avoid the free-for-all that can occur if responsibility and authority are not properly defined.

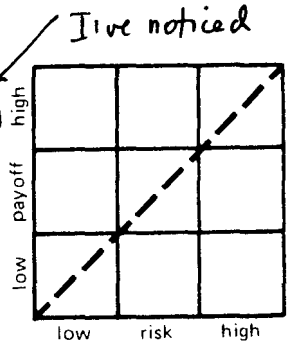
VII. Too many leaders means no leadership at all

Many kinds of organizational behavior can be observed at one time or another wherever new products are developed:

- High level management has a great deal of interest.
- Everyone wants in on the act when the odds look good.
- When things look bad, a program can become orphaned and many politicians emerge pointing fingers.
- Everyone has his own sandbox and doesn't like others to step in it.
- Decisions tend to move up the organization when the going gets tough.

It is critical that responsibility and authority are delegated equally to the proper organizational level. For large projects, do yourself a favor and appoint *one* person with over-all responsibility *and* authority. For smaller projects, one technical leader from R&D and one commercial leader with clearly defined authorities can be more appropriate.

Project leaders should be chosen from the ranks of those who continually look forward, not those who walk thru life peering over their shoulders. There are enough historians and beancounters who will give the project leader information about the past whether he wants it or not.



Risk and payoff *of R&D projects can be considered in matrix form. Logically, all projects should be to left and above diagonal.*

VIII. Sunken costs should neither kill nor continue a project

When someone says; "We have spent $1,000,000 on this project and must make it a success," or "We have spent $1,000,000 on this project and can't afford a penny more," think carefully about what he really means. In the first case, he generally is talking about a project to which he is emotionally attached and/or one that has a high "political ROI" in the organization. In the second case, look carefully to see if he has one or more eyes in the back of his head.

Money spent has already been taken by the croupier. The key question is, "Where are we, and what resources will it take to get to the goal?"

Each project, regardless of resources consumed, should be ranked/prioritized periodically versus all others in the portfolio to insure that any spending changes are justified by strategic importance, probability of success, and/or efficient use of resources.

Costs for R&D, as any costs, are both direct and indirect. One of the most expensive unmeasured costs is the extra, and sometimes unnecessary, effort consumed by premature paperwork and schedules.

IX. A sample is worth ten thousand pounds of paper

A working model of a product or technical phenomenon is worth many times the paperwork and meetings surrounding it. Certainly, good record keeping in the form of laboratory notebooks and technical reports is necessary to analyze where you've been and to provide documentation for filing patents. Additionally, marketing investigations and specifications must be documented. Periodically scheduled reviews, as far apart as possible, are necessary for good and continuing communications, as well as for decision inputs.

The unnecessary efforts that can be eliminated generally fall into one of the following categories:

- "Number crunching" exercises.
- Posterior-covering memos and other sandbags.
- Scheduling of inventions.
- Reviews that lead to meetings that lead to reviews...

In only one area can documentation be *lacking* before an invention is made: when the product concept involves those kinds of risks that can have sweeping strategic and/or legal ramifications.

X. The kind of risk is often more important than costs

The kinds of risk that can threaten the survival of a business go far beyond development price tags. Some of these far-reaching risks and their potential consequences are as follows:

- *Decisions not to fund improvement of "bread and butter" products.* You can bet the competion is out to do you one better. To underestimate him opens the door to your market.
- *Forward integration.* Successful or not, you will lose some or all of your customer base.
- *Backward integration.* You will most likely dry up your current source of supply, with the benefit accuring to your current competition.
- *Product safety and liability.* A failure to meet *expected* consumer safety requirements can precipitate a product recall that can all but put you out of business.
- *Product integrity.* Putting out products that do not measure up to your organization's reputation can ruin years of effort.

Risks in any one of these categories should be documented thoroly and understood *"up-front"* all the way to the top. If this is not done, at best, a lot of money and time may be spent on products that never go out the door. At worst, you could lose the business. ■

THE AUTHOR

Robert G. Block is manager of market development, Sunglass Products Dept. of Corning Glass Works. Earlier, he was a research physicist with the Air Force. He has an MS in ceramics from MIT, an MBA from the Univ. of Dayton

JAN 28 1982

5.20

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* D I G I T A L *
****

INTEROFFICE MEMORANDUM

TO: Distribution

DATE: 26 Jan. 82
FROM: MIKE GUTMAN
DEPT: PSD
EXT: 223-5285
LOC/MAIL STOP: ML12-2/E71

CC: Jack Smith Gordon Bell
Larry Portner Cathy Klinck

SUBJECT: PRODUCT EXCELLENCE - WHAT DOES IT MEAN TO ENGINEERS

Thanks for a very stimulating dicussion. I've tried to capture all your thoughts below - please continue to input additional thoughts as they evolve.

1. What?

A. Figure out what you want to do and do it fast.
B. Functionality for the $

1. More functionality, same cost.
2. Constant functionality, lower cost.

C. Can it be serviced?
D. Can it be sold internationally?
E. Is it easy to program?
F. Balance between cost, performance and time to market.
G. Easy to understand product?
H. Easy to fix product?
I. Product excellence is seen in our architecture, software and field service.
J. Technology - means risk! Means new tools! Means being willing to do projects which might fail. Environment doesn't support risk taking. On budget + on time = winner.
K. No new parts because the hassle to bring them is is too high. How to fix?
L. Change rewards for taking risks.

1. If you hatch a turkey, you shouldn't be killed.
2. Our review system doesn't mention risk. Why?
3. Risk management should be at multiple levels.

M. Software - who will generate it? Will it be in silicon?

2. How?

A. Establish the spec, be firm, but flexible.
B. Lots of resoures at DEC, know where to look.
C. Tools are very important - simulation.
D. Need to understand how we build our products.

E. Need to permit a team to bring together a wide variety of different disciplines to make excellent products. Involve people earlier. Helps time to market.
F. We keep information to ourselves too long. (Skate in closet). Engrs want to be sure before they tell anyone.
G. Are we late to market because of too much buy in?
H. Technology moving rapidly - need to decide and move - don't revisit and reverse very much.
I. Need a radical rethinking of the way DEC does its (internal) business.
J. Need to get rid of a-la-carte to reduce the options we need to document and support - go to automatic configuration.

3. Who?

A. Sense of pride, do I feel good about product?
B. Who wants it? Know someting about customer.
C. We should talk to people - DECUS.
D. Should keep engineers on projects long enough to fix the problems.
E. Do we expect engineers to know too much today?
F. Who tells us what to design? No one - we're on our own.
G. Need to "tell" marketing people what's good.
H. Do we tell marketing people enough about what we're doing, so they understand the tradeoffs and don't yank us around?
I. Who was our competition (HP, DG, IBM, Prime, Semiconductor vendors, Apple). Our future competition will be semiconductor manufacturers and Japanese.

4. When?

A. Cost has to be right when product appears.
B. Time to market being hurt by relatively inflexible manufacturing organization.

/df

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HEURISTICS FOR BUILDING GREAT PRODUCTS
(DRAFT FOR COMMENT)

FIVE SETS OF DIMENSIONS FOR BUILDING GREAT PRODUCTS NEED BE ATTENDED TO (ROUGHLY IN ORDER OF IMPORTANCE):

- A RESPONSIBLE, PRODUCTIVE AND CREATIVE ENGINEERING GROUP;

- PRODUCT AND DESIGN METRICS (COMPETITIVENESS);

- DESIGN GOALS AND CONSTRAINTS;

- PRODUCT EVOLUTION, REVOLUTION AND DEATH; AND

- THE ABILITY TO GET THE PRODUCT BUILT AND SOLD.

ENGINEERING GROUP

THE TEAM MUST HAVE:

- A CHIEF DESIGNER/CHIEF PROGRAMMER TO FORMULATE AND LEAD;

  NO COMMITTEES AS DESIGNERS

- MANAGEMENT WHO UNDERSTAND THE PRODUCT SPACE AND WHO HAS ENGINEERED SUCCESSFUL PRODUCTS; THE TWO MOST IMPORTANT JOBS ARE:

  - MAKING SURE THAT EVERYONE KNOWS THEIR JOB; AND

  - ESTABLISHING AND REVIEWING WORK ON A TIMELY BASIS, I.E. MBO.

- TEAM SKILLS AND RESOURCES TO IMPLEMENT THE PROPOSAL SO THAT WE ADHERE TO THE CARDINAL RULE OF DIGITAL, "HE WHO PROPOSES, DOES";

- AN UNDERSTANDING OF THE DESIGN, DESIGN PRODUCTION (EG. CAD) PROCESSES, AND MANUFACTURING PROCESSES.

BEHAVIORALLY, THE TEAM MUST:

- DO IT RIGHT THE FIRST TIME;

- EXECUTE THE PROJECT IN A TIMELY FASHION;
  - LIMIT PROJECTS TO LESS THAN TWO YEARS BY A SMALL TEAM.
  - NOT PREDICATE A PROJECT ON SCHEDULING INVENTIONS IN THE DESIGN, PROCESS AND CAD AREAS.

- HAVE A WRITTEN DESIGN METHODOLOGY;

- BE OPEN AND HAVE EXTERNAL REVIEWS, AND CLEARLY WRITTEN PRODUCT DESCRIPTIONS FOR INSPECTION;

- START SMALL, BE REVIEWED AND GROW ON ITS DEMONSTRATED SUCCESS;

- LEARN, IN ORDER TO HANDLE THE INCREASE IN COMPLEXITY

PRODUCT METRICS KNOWLEDGE INCLUDES:

- PRODUCTS FOR WHICH THERE'LL BE NO COMPETITOR;
- ALL PRODUCT COST METRICS;
- ALL PRODUCT PERFORMANCE AND COST/PERFORMANCE METRICS;
- REASONS WHY THE PRODUCT WILL SUCCEED;
- MAJOR COMPETITOR PRODUCTS BY COST, PERFORMANCE AND FUNCTIONALITY;
- LEADING EDGE, INNOVATIVE, SMALL COMPANY PRODUCTS;
- PRODUCTIVITY, QUALITY AND DESIGN PROCESS METRICS FOR PROJECTS

DESIGN GOALS AND CONSTRAINTS

- GOALS AND CONSTRAINTS MUST BE WRITTEN DOWN AND UPDATED FROM THE DAY THE PROJECT STARTS.

- A PRODUCT CAN ONLY HAVE A FEW GOALS AND CONSTRAINTS. THE RANKING IS USUALLY: IT MUST WORK AND HAVE IMPROVED COST OF OWNERSHIP, BE THE SHORTEST TIME TO MARKET, HIGHEST PERFORMANCE AND LOWEST COST.

- IF A STANDARD EXISTS, FOLLOW IT OR CHANGE IT FOR ALL!

- IF A STANDARD IS FORMING GO ALL OUT TO SET IT.

- PRODUCTS MUST BE DESIGNED FOR EASY TRANSLATION INTO IN ANY NATURAL LANGUAGE SINCE WE ARE AN INTERNATIONAL COMPANY.

- ALL PRODUCTS MUST HAVE BE CUSTOMER INSTALLABLE AND MAINTAINABLE.

- PORTABILITY IS AN IMPORTANT GOAL.

WHEN TO CREATE, WHEN TO EVOLVE AND WHEN TO STOP PRODUCTS

- IDEAS MUST EXIST TO HAVE PRODUCTS! IF WE DON'T HAVE IDEAS TO REDEFINE OR EXTEND A MARKET, THEN WE SHOULD NOT BUILD A PRODUCT.

- A PRODUCT TREE MUST BE MAINTAINED BY EACH ENGINEERING GROUP SHOWING ROOTS, GESTATION TIME AND LIFE.

GOODNESS AND GREATNESS = NO CRAPPY PRODUCTS

- BE ELEGANT AND HIGH QUALITY;
- OFFER AT LEAST A FACTOR OF TWO COST-EFFECTIVENESS OVER A CURRENT PRODUCT;
- BE BASED ON AN IDEA WHICH WILL OFFER AN ATTRIBUTE OR SET OF ATTRIBUTES THAT NO EXISTING PRODUCTS HAVE;
- BUILD IN GENERALITY, AND EXTENSIBILITY;
- BE A COMPLETE SYSTEM, NOT PIECE PARTS;
- BE A GREAT SYSTEM BECAUSE THE COMPONENTS ARE GREAT;
- IF WE DON'T MAKE IT, BUY IT;

ELEGANCE: WHAT IS IT?

Russ Doane: "every feature contributes two benefits"

RH dictionary: "gracefully refined, dignified, of high quality"

guality = lack of excess (especially errors)

Elegant design is the use of a part to perform many functions.

Architects say: "Less is more."

Some examples: the stored program computer (use of memory), the general registers, the Unibus, Pascal, APL.

Several pioneers: "Leave a feature out that can be done another way."

It can sometimes conflict with other goals like orthogonality.

But too much elegance is trickery.

Product Evolution

- LOWER COST PRODUCTS REQUIRE ADDITIONAL FUNCTIONALITY TOO;
- CONSTANT COST, HIGHER PERFORMANCE PRODUCTS ARE LIKELY TO BE THE MOST USEFUL;

Revolutionary New Product Bases

- A NEW PRODUCT BASE, MUST START A FAMILY TREE FROM WHICH SIGNIFICANT EVOLUTION CAN OCCUR.

Product Termination

- A PRODUCT EVOLUTION IS LIKELY TO NEED TERMINATION AFTER SUCCESSIVE IMPLEMENTATIONS, BECAUSE NEW CONCEPTS IN USE HAVE OBSOLETED ITS UNDERLYING STRUCTURE.

SELLING AND BUILDING THE PRODUCT

- IT HAS TO BE PRODUCIBLE AND WORK, AND BE USEFUL TO SOFTWARE;

- A BUSINESS PLAN WITH ORDERS AND MARKETING PLANS FROM SEVERAL MARKETING PERSONS AND GROUPS NEEDS TO BE IN PLACE;

- NEVER BUILD A PRODUCT FOR A SINGLE CUSTOMER,

- IT MUST BE DONE IN A TIMELY FASHION ACCORDING TO THE COMMITTED SCHEDULE, PRICE AND FUNCTIONS;

- IT MUST BE UNDERSTANDABLE AND EASY TO USE.

PRODUCTS THAT HAVE NOT MET EXPECTATIONS

PDP-8/S

VT8/E (REUTERS), VT14 (FOR PDP-14

VT30 ETC. (CSS)

VT15, GT40, GT60, MEGATEK BUYOUT (ENG P/L)

VSV11 (LDP AND CSS)

VT20, 21, 61T, 71, 171 (TYPESETTING P/L)

LA36/BSR, LA36/TU60, LA120/Tu58 (ATT)

MINC, MINI-MINC (LDP P/L)

PDT 110, 130 150 (SPECIALIZED CUSTOMER)

GIGI (EDU P/L)

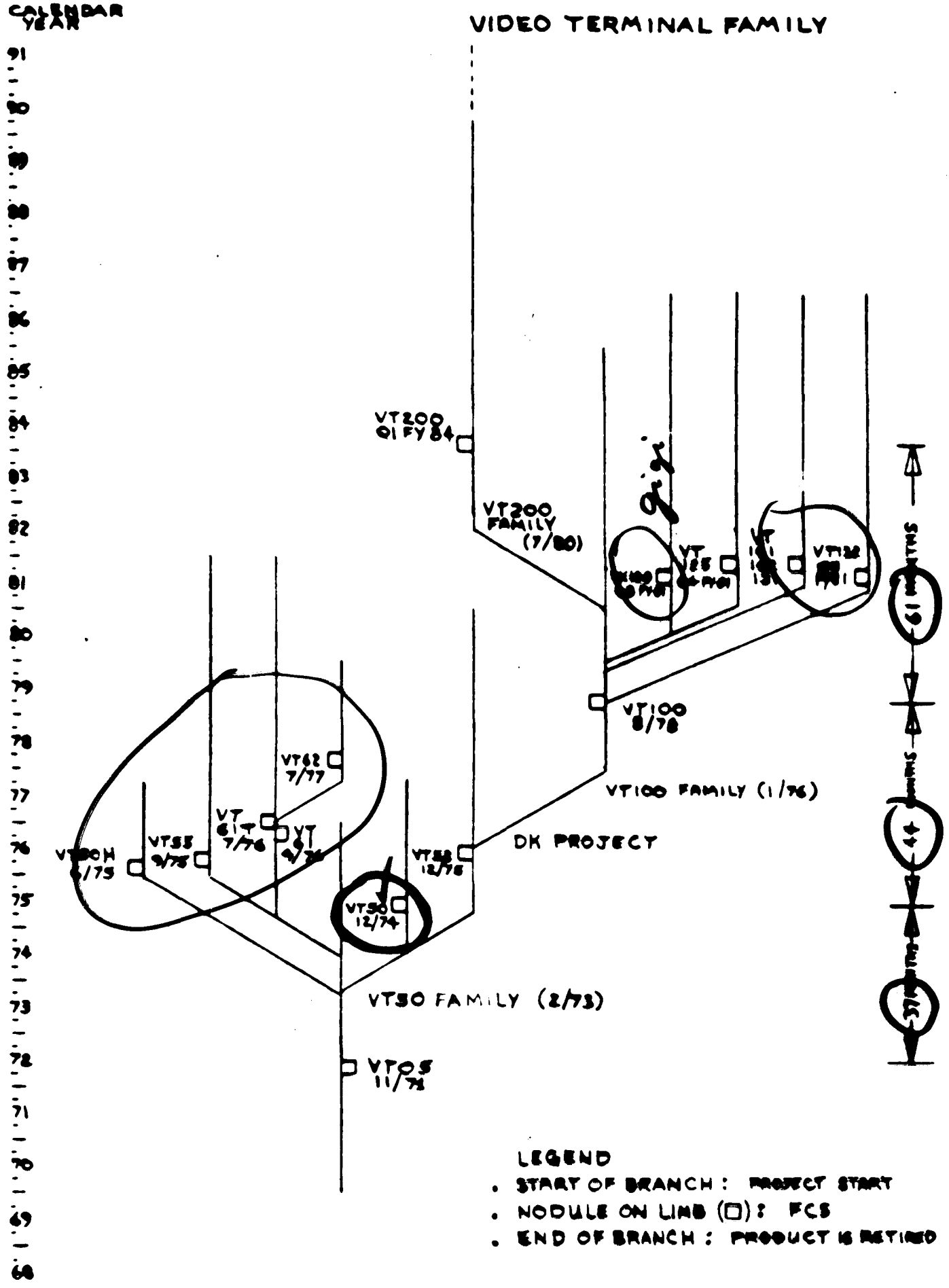
VT103 (TPG)

11/60, DS315, 11/23

LA34

WS100, WPS78, WPS 278, DECMATE I? (WPS P/L)

COMPANY CONFIDENTIAL



LEGEND

- START OF BRANCH : PROJECT START
- NODULE ON LIMB (□) : FCS
- END OF BRANCH : PRODUCT IS RETIRED

JCOX 8/80

PITFALLS OF LOW END PRODUCTS

- CUSTOMER SPECIALIZED
- SPECIALIZED MARKET NOT DOABLE WITH GP TERMINAL OR SYSTEM
- DONE ON A LIMITED BUDGET. JUST ENOUGH SPENDING TO LOSE.
- MARKETING DEMANDS IT. ENGINEERING DESIGNS IT.
- POOR ENGINEERING LEADERSHIP TO PROVIDE THE RIGHT SOLUTION
- POOR SOLUTION COMPARED TO COMPETITION
- INADEQUATE PRODUCT SUPPORT IN MARKETING OR ENGINEERIN

HOW CAN WE REDUCE THE TIME TO INTRODUCE PRODUCTS?

By doing quality engineering... NO REWORK in the Testing Phases

Getting the Quick Turn Around Process to a Week
Prints to correctly build module

Mid-life kickers and multiple implementations per design

WHAT IS QUALITY DESIGN?

Functional Specification in a working, design language

Quality Design

Checking of the Design by Design Walk-through (Code Walk through)

Simulate and verify the design. Prepare test data

Build it and verify that it works as designed

COHEN'S ELEMENTS OF SOFTWARE QUALITY

PACKAGING

INSTALLABILITY

EASE OF USE

RELIABILITY

PERFORMANCE

FEATURES

SERVICE TO USERS

MAINTAINABILITY

MAINTAINENCE

COMPATIBILITY

EVOLVABILITY

TIMELINESS

... ALL OF THE ABOVE

WHAT IS A DESIGN METHODOLOGY?

PROCESS CHARACTERIZATION

DESIGN STEPS, TIMES, LEARNING, SCHEDULING

DESIGN REPRESENTATION

[PHYSICAL,FUNCTIONAL] X [LEVELS] X
[AMOUNT AND KIND OF DETAIL]

CONVENTIONS (FOR NAMES) AND RULES FOR CREATING THE DESIGN

WHAT ABOUT A MODERN DESIGN SYSTEM

ONE DATABASE THAT HAS ALL SIGNALS, BOXES AND THEIR DEFINITIONS

HIERARCHIAL, WITH TOOLS TO CONSTANTLY CHECK ALL ASSERTIONS...

NO FEEDING FORWARD OF DESIGN THROUGH A SERIES OF PROGRAMS

INTERACTIVE

SIMULATION AND VERIFICATION ARE ESSENTIAL

What was learned from Robin (VT18X).

PROJECT MANAGEMENT

time-to-market = 8 mos

- o RECOGNIZE THAT TIME, NOT MONEY, IS THE ENEMY:
  - TIME IS THE RESOURCE TO BE CONSERVED
  - MONEY IS USED FOR MAKING TRADE-OFFS

- o FIRM UP AND GET COMMITMENT TO THE PRODUCT SPEC/BUSINESS PLAN, HAVE CUT-OFF DATES, STICK TO THEM - NO SURPRISES!
  - IF YOU HAVE TO CHANGE, MAKE SURE THE BENEFIT IS GREAT ENOUGH FIRST TO JUSTIFY EVEN DETERMINING WHAT THE COST MIGHT BE

- o USE GOOD PROJECT MANAGEMENT

- o REVIEW PROGRESS - MEASURE IN DAYS/WEEKS FROM THE TARGETED END DATE.

Robin

PROJECT MANAGEMENT (CONT'D)

0 USE GOOD PROJECT MANAGEMENT

- GIVE ONE PERSON YOU TRUST CLEAR OWNERSHIP
  - PROJECT/BUSINESS - GENERALIST
- STAFF X-FUNCTIONALLY WITH GOOD, DEDICATED PEOPLE
- PUT THEM PHYSICALLY CLOSE TOGETHER
- GET CORPORATE BACKING
- CREATE A STRONG TEAM FOCUS
- PLAN THOROUGHLY - DESIGN IN PARALLELISM
- MAKE SURE YOU HAVE ENOUGH MONEY
- DON'T CHANGE THE SPECIFICATION
- STAY AWAY WHILE THE WORK IS GOING ON
- HAVE A CLEAR, QUICK, "BUBBLE-UP" DECISION-MAKING PROCESS IN PLACE
- REVIEW PROGRESS, MEASURE IN DAYS/WEEKS FROM END DATE
- FOCUS ON TIME AS THE ENEMY
  - "HOW CAN WE MAKE THE DATE?"

    NOT
  - "WHY WE ARE GOING TO SLIP."
- SET A CLEARLY DEFINED/FIXED PRIMARY PRODUCT/PROJECT GOALS - UNDERSTAND AND MAKE SECONDARY GOAL TRADE-OFFS AGAINST THEM.
- SET FIXED EXTERNAL (PUBLIC) PROJECT TARGET DATES TO FORCE PRODUCT/PROJECT CLOSURE.

Robin

DESIGN VERIFY/TEST PROCESS

- o DEFINE/EXPLAIN THE DVT/DMT/PMT SO THAT EVERYBODY KNOWS WHAT IS GOING ON, WHAT TO EXPECT, AND WHEN

- o TREAT DESIGN TESTING AS AN INDEPENDENT "DO" PROCESS (NOT AN OVERHEAD FUNCTION)
  - PLAN IT RIGHT/DESIGN IN PARALLISM
  - PROVIDE ENOUGH MONEY/PEOPLE TO DO THE JOB
  - MAINTAIN A HIGH VISIBILITY ON WHERE WE ARE - WHAT'S NEXT - WHEN
  - APPLY SERIOUS MANAGEMENT TECHNIQUES TO IT

- o HAVE A TEST SPEC - TEST ONLY TO IT, NOT BEYOND IT

- o PUSH PROBLEMS TOWARD BEGINNING WHERE THEY ARE CHEAP TO FIX
  - FOCUS ON DVT (HARDWARE/FIRMWARE/SOFTWARE)

- o ONLY ENTER DMT/PMT WHEN YOU ARE 90% CERTAIN OF PASSING

- o PROVIDE A CLEAR "RECOVERY" PROCESS TO CORRECT PROBLEMS THAT ARE DISCOVERED

- o UNDERSTAND HOW THE MACHINE WORKS - UNDERSTAND WHAT IS OK - WHAT STILL NEEDS TO BE TESTED

Robin

DESIGN SERVICES/PROTOTYPE BUILD PROCESS

- o Start with a breadboard
- o MAKE MISTAKES ON PAPER - NOT IN HARDWARE
  - USE SIMULATION TOOLS - HARDWARE/FIRMWARE
  - USE DESIGN REVIEWS → Design Walk-through
  - ASSURE PRODUCIBILITY
  - AVOID RE-LAYOUT CYCLES
- o ALLOW SPACE IN THE DESIGN FOR FLEXIBILITY - DON'T UNNECESSARILY PACK TOO MUCH ON ONE BOARD/IN ONE ROM
- o KEEP DOCUMENTATION CLEAN AND UP-TO-DATE
- o SUBMIT "CLEAN/COMPLETE" DESIGNS TO P.C. LAYOUT
  - USE DESIGN CHANGE CUT-OFF DATES
  - STAY AWAY
- o GET THE SERVICE GROUPS ON THE NEW PRODUCTS TEAM
- o CONTINUE THE LITTLETON TURNAROUND IMPROVEMENTS
- o ANTICIPATE TECHNOLOGICAL CHANGE WITH NEW CAD TOOLS

MANUFACTURING

- o HAVE A STRONG CENTRAL TERMINALS NEW PRODUCT GROUP TO SERVE AS THE MKT/ENG/C.S. INTERFACE FOR THE PLANTS
  - GET MISSIONS/ROLES/RESPONSIBILITIES CLEAR
  - WHO'S DRIVER/OWNER AND WHO'S SUPPORT, WHEN
- o BE RESPONSIVE - USE SENIOR MANUFACTURING PEOPLE THE PLANTS TRUST TO ANSWER QUESTIONS/MAKE DECISIONS QUICKLY

VENUS: WHAT WENT WRONG?

CHIEF DESIGNER:	0,1,2,3,4?
MANAGEMENT:	3 LEVELS; DISCONNECTED FROM PROJECT; LACK OF RIGHT REVIEWS; FOCUS ON PROCESS, NOT PRODUCT
TEAM:	CONTRACT PRECEEDED TEAM; ORGANIZATION MUDDY
UNDERSTANDING:	POOR ON HOW TO DESIGN; CAD OK: MFG. VERY GOOD
TIMELINESS:	PROJECT ALWAYS 27 MONTHS AWAY; PLAN DIDN'T SUPPORT THE SCHEDULE
DESIGN METHODOLOGY:	WORD OF MOUTH, TOO MUCH PAPER, DESIGN TO SCHEDULE, BUILD A BREADBOARD THEN REDESIGN IT!
REVIEWS:	INADEQUATE; MISALIGNED GOALS
LEARNING:	INADEQUATE KNOWLEDGE ON HOW TO DESIGN, COMPLEXITY MANAGEMENT, AND SCHEDULING
PRODUCT METRICS:	FINE
GOALS:	MUDDY... NOW IT'S TIME TO MARKET
CUSTOMER INSTALL:	FINE
ELEGANCE & QUALITY:	TOO MANY IDEAS (AND PEOPLE)

VENUS: NOW

CHIEF DESIGNER:	ALAN KOTOK
MANAGEMENT:	BOB GLORIOSO, PRIMARY FOCUS IS ON PROJECT
TEAM:	HIERARCHY
DESIGN METHODOLOGY:	PROCESSES WRITTEN; HIERARCHY OF SPECS; QUALITY-BASED DESIGN VS. SCHEDULE BASED; DESIGN WILL WORK BEFORE ITS BUILT; DESIGN PROCESS MODEL
UNDERSTANDING:	INCREASING; COURSES ON COMPLEXITY AND SW
REVIEWS:	A HIERARCHY; MONTHLY WITH MILESTONES
GOALS:	WORKS; TIME TO MARKET; PERFORMANCE; COST

WHAT IS A DESIGN METHODOLOGY?

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00 BURT DECGRAM ACCEPTED S 2131 O 58 21-MAR-82 14:41:27

****
* d i g i t a l *
****

TO: DIANA MAYER

DATE: SUN 21 MAR 1982 2:40 PM EST
FROM: GORDON BELL
DEPT: ENG STAFF
EXT: 223-2236
LOC/MAIL STOP: ML12-1/A51

SUBJECT: RE: DESIGN LECTURE SERIES

Please send me the relevant section. I must confess that in putting the phase review into such an awesome book (it has lots of blank space) versus the thinest possible book and tightest possible set of words, it has chased me away from reading it.

Also, I think otherlook at this and say we've lost a lot by trying to get everyone to paint by the numbers. This virtually assures that a product project is very big, just to fill out the plethora of forms.

For the critical first part, I like reading only a few pages of spec to find out why the product is going to be good. If it doesn't pop out in the summary, then quite likely we have a problem.

Also, if we put more focus on preliminary work, which may also get the engineers to engineer versus filling out the forms, then the transition to phase 1 might best be a working breadboard instead of loads of paper.

****
* d i g i t a l *
****

TO: *GORDON BELL

DATE: SUN 21 MAR 1982 1:25 PM EST
FROM: DIANA MAYER
DEPT: CENTRAL ENGIN OPER
EXT: 223-7612
LOC/MAIL STOP: ML3-5/T47

SUBJECT: DESIGN LECTURE SERIES

RE: DESIGN LECTURE SERIES MARCH 18 on Engineering Project Mgmt:

1) INSPIRATIONAL: Listening to a brilliantly conceived and executed discourse on the structure of technological change and managerial misconceptions of the process, I reflected that we hadn't heard Professor Bell since Stratton V. How can we get you to address the troops a bit more often...no one else can bring together so much current theory (Deming, etc) and apply it to current problems as well as you do.

2) TIMELINESS: I am currently struggling to define functional and design specifications. Standard "assessment guides" for these specs were not available for the Phase Review Process Notebook accompanying DEC STD 028 recently issued by Picariello. You mentioned these documents in the lecture. Could you send over to Charlie's office any source materials or references or insights on these specifications? You might want to check the "milestone descriptions" in the notebook to see if they agree with your concepts. We can revise them if they do not.

Regards, and thank you for providing much food for thought on Engineering Management in the 80's at DEC. Diana

21-MAR-82 13:27:14 S 2070 EMML

EMML MESSAGE ID: 5157958020

****
* d i g i t a l *
****

TO: *GORDON BELL

DATE: MON 22 MAR 1982 10:38 AM EST
FROM: GEORGE THISSELL
DEPT: CSE PLN'G & OPERAT'NS
EXT: 223-7698
LOC/MAIL STOP: ML12-3/A62

SUBJECT: COMMENTS RE GREAT PRODUCTS HEURISTICS

If I may, a couple of sussested additional heuristics and a sussested chanse:

-Though a development project's a project, software is not the same as hardware; for example software doesn't die and is much harder to replace once it has users who like it - witness RSTS and RT-11.

-By definition "sreat people" have done somethins sreat - corrollaries are that potential needs a chance to prove itself; and there are no winners from a losins product.

-On ps 1 under ". manasement who....", I'd add a third most important job:

.makins sure it's a successful product

(otherwise why does he need a successful backsround ?)

Resards

22-MAR-82 10:38:50 S 4591 EMML

EMML MESSAGE ID: 5158058145

****
* d i g i t a l *
****

TO: *GORDON BELL

cc: FRANK GRIMALDI
HENK SCHALKE
WILL THOMPSON

DATE: TUE 23 MAR 1982 5:29 PM EST
FROM: BOB LOTZ
DEPT: PDT
EXT: 223-5774
LOC/MAIL STOP: ML8-3/T13

SUBJECT: FEEDBACK ON YOUR DRAFT TALK, "HEURISTICS ..."

23.3(1)

PAG#: 641

Per your request on page 7 for comments, I would like to suggest some or all of the following bullets under your existing topic headings as indicated:

MANAGEMENT WHO UNDERSTAND THE PRODUCT SPACE ...

- Team leader needs to be alert as to how 80s are different from 70s.
- For example, regulations and office workers will force acoustically noisy products out of the office.
- Therefore, yesterdays acoustical performance won't suffice tomorrow.

LOWER COST PRODUCTS REQUIRE ADDITIONAL FUNCTIONALITY TOO:

- Constant noise level/decreasing cost curve -- probably wrong.

CONSTANT COST, HIGHER PERFORMANCE PRODUCTS ARE LIKELY TO BE MOST USEFUL

- Where office compatibility is a consideration, improve acoustical performance with each new or "mid-lifed" product.

BL/NY .

23-MAR-82 17:31:12 S 18983 EMML

EMML MESSAGE ID: 5158159058

APR 1 1982

TO:

==========
D I G I T A L
==========

I N T E R O F F I C E M E M O R A N D U M

TO: Gordon Bell

DATE: 30 March 1982
FROM: Geoffrey Feldman
DEPT: VENUS
EXT: 231-6259
MAIL STOP: MR1-2/E78

SUBJ: Heuristics and great products

Dear Mr. Bell,

I enjoyed your talk last Friday. Here are some of my thoughts regarding it.

If those that propose, do then, doers should be proposers. They have met the key requirement. If workers should demand(propose) good management they should be able to manage(do) themselves. Out of this falls the conclusion that workers should be self managing.

In fact in this thing which we call matrix management that is essentialy the case. The problems come when the parameters of that self management are not understood. When engineers in other companys ask me what it is like to work here, I have a very succinct answer. "DEC is a nice place to work, you can do almost anything you want consistent with the companys goals." "The bad news is that everyone else is doing what they want, sometimes it is to you."

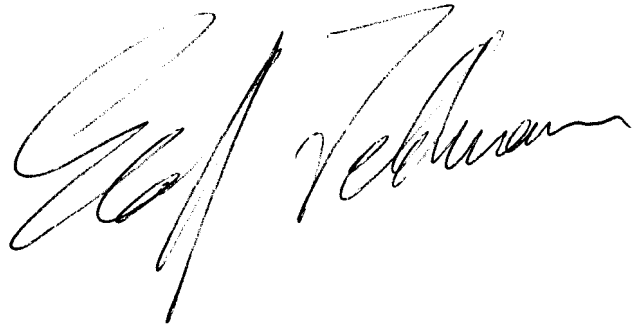
I often find cases where two groups are, with the very best intentions, pursuing opposing goals. Both groups believe they are making the most money they can for Digital. Often they could make more if their goals were more in synch. People need to take a more global view of their role within the company. Some examples of this are 20 DECnet/VMS DECnet, GIGI/the VT125, ED services/Engineering groups.

Function relative to your group since this is the easiest way to think. However, always check your actions against the question, "Is the agregate affect with other groups the best for the company?"

Do not form such an emotional commitment to your design that you execute it when it simply should be put to death. Also many projects become so loaded with features trying to serve many masters that they never work. Do not design past capacity to execute (in both senses). Know when a design is really two designs. Keep it simple. TRAX would have been wonderful had it been simple. Instead it broke the capacity of the 16 bit architecture to support complex software. ADE was a nice idea Unfortunately it was obsolete before it was finished. That should have been the end of it. Now it is an 'In house' product and will be a burden for years to come.

Some of the above were touched on in your talk, but I feel could have been more explicit. The issues of conflicting goals and not forming emotional attachments that cloud judgement are the hardest for individuals to manage. We are often skewered by such primal instincts as territorial imperative and an overly maternal (/paternal, parental?) attitude toward our ideas. We must remember that in nature mothers eat their young in the common good.

[memo name: HEURAnSw]



DIGITAL

INTEROFFICE MEMORANDUM

POST

TO: STAN PEARSON

CC: OOD
Software Product Managers
Julius Marcus
Jane Ward
Marty Hoffmann

DATE: 18 JUNE 76
FROM: NATHAN TEICHHOLTZ
DEPT: NETWORKS
EXT: 2533
LOC/MAIL STOP: ML12-3/A62

SUBJ: THE NEW PRODUCT DISASTER PHENOMENON

Most of the money we spend on product development actually goes to re-engineer or enhance existing products, but every once in a while we actually succeed in introducing a 'new product', i.e., one which includes a substantial set of new features not previously found together on a given class of systems. With few exceptions (at least in the software area) we end up regretting at least a few of the initial sales of such new products. This memo explores how and why we get ourselves into this situation and possible alternatives to lessen the pain for future product introductions (DCOPS, DBMS, TPS, ...). The memo was motivated by the DECNET problems we've had at Deering-Milliken, but the problem transcends DECNET, and has been a characteristic of DEC software introductions at least as long as I have been observing them.

Symptoms of a new product disaster

The new product disaster usually has the following visible characteristics:

1. Occurs within first 6 months of FCS (sometimes just prior to FCS).

2. Normally shows up as less than adequate performance (in terms of number of users, lines, response times, transactions per second, etc.).

3. Occasionally shows up as irremediable configuration problems (surpasses limits of virtual or physical address space, system bandwidth, etc.).

4. Usually requires some internal modifications to the internals of the product. Generally thought to be minor at pre-sales time, they inevitably are not. CSS, PL90 and/or the customer may plan to implement changes. Almost always requires bailing out by product developers.

5. Usually involves big systems with lots of 'potential follow-on business'; often major customer.

6. Usually involves agressive salesperson who 'knows DEC' and has hooks into the Development organization.

7. Usually has extensive product-line pre-sales involvement, with some assistance and review from development.

8. Usually shows up at least once per product in the Texas District (comprising Texas, Oklahoma, and Louisiana).

Any situation characterized by four or more of the above symptoms either is or is ripe for a disaster. (Letters to Ken, threats, A/R problems, excessive support costs, etc.).

What causes these disasters to occur?

There are relatively simple forces at work that motivate each of the disaster symptoms. It's useful to understand them in order to understand how to prevent them. These forcing phenomena (correllated with the symptoms just described) are:

1.1 These sales are invariably made before FCS, often before field test. The actual limits of the product are not understood, so it's easy to oversell. (We use disasters like this to learn what the limits are.) During the pre-FCS period, all products are 'perfect'; they have no warts. They are infinitely expandable with infinite performance, require no core, store infinite data in almost no buffer space, and are easily modified, even with no internal documentation. The field and CSS can modify them without any training whatsoever.

1.2 It is depressing to note that on the one recent product (IAS) where we emphasized limitations in the introduction package, the field has been very slow to accept and promote the product. The implicit reasoning seems to be that if we admit to limits, the product must be a real dog, since the other products are billed as perfect, and yet do have limits.

1.3 The lack of field experience with the product hurts two ways. There are no 'sanity checks' on the fit between the product and the application. Once problems do arise, they are handled ineptly, further aggravating the customer.

1.4 During the introductory phase we usually cannot run benchmarks, so the customer never has the opportunity to trip over the limitations before he buys.

2.1 Historically, we have not specified the performance of our software products in any meaningful way. Thus, the customer who hasn't been able to run a benchmark, and has heard all these glowing things from everybody in DEC Sales, Product line, development) has expectations of infinite performance. In many cases, we don't even know how to specify performance (e.g., the original DECnet spec on line speeds versus the current one on throughputs and messages per second; the more meaningful parameters). In the hardware area we often 'blow' specs by ignoring environmental concerns that weren't considered, but are, in actuality, relevant (altitude, particulate matter, media vendor,...). We only learn what negative specs need to be included via the disaster process.

3.1 Historically, we have done a bad job of specifying the fixed and variable core sizes of our software products. Developers rarely recognize that when all options are included, all tables are set at their maximum sizes, and all buffers and file blocks are allocated, that their core size may exceed the maximum available to them. This turns out to be a limiting factor in every PDP-11

operating system. Most of these systems allocate resources dynamically, and the developers are rarely confronted with situations where their systems are so active that the resources actually run out.

4.1 The likelihood that there will be a perfect fit between the customers requirements and the capabilities of the first release of a product (which inevitably lacks certain functionality traded off for schedule purposes) is small. This is normally compensated for by the customer (or CSS or PL90) planning to write the missing device handler and integrate it into the system. Since there is usually no good information on how to do this for a new system, the likelihood of success is small. An attempt is made, it doesn't work, and assistance from Maynard development is requested. This is usually forthcoming under great protest, and leaves a bad taste in everybody's mouth.

5.1 Such disasters are almost always highly visible (at least within DEC) and carry big potential sales value (if we succeed in turning the situation around). We wouldn't have exposed ourselves to such a big risk unless the payoff was substantial. During the interval between the sale and the disaster, the product line, product manager and developers all refer to the situation as a glowing example of how great the product is. Thus, when it flops, it flops big!

6.1 Such disasters are usually sold by salesmen who know how to "work DEC". The more timid sales reps either don't know about the products too far in advance, or don't have the endurance to 'sell Maynard' on exposing itself to the inherent risks. These same reps also know whom to call when they need to be bailed out of the disaster, and can apply pressure to the product lines to help straighten things out.

7.1 It is rare that such a situation occurs without extensive presales involvement of the product line and development groups. The salesman usually tries to 'sell' the sale to the product line. The product line hates to turn away a large potential order, since it feels it is developing the product in question to attract just such business. The timing, performance, and features may be a little less than ideal, but eventually this is viewed as a reasonable business risk, given the potential for follow-on business. So they nervously acceed, hoping that development will point out any areas why the system cannot work.

7.2 Unfortunately, the developer should be the last person to ask for an objective statement on whether the 'system will do the job'. His ego involvement with the product is such that he will overlook even the most obvious reasons for instant failure; to do otherwise would be to admit limits in his product, and by implication, in his abilities. The competitive spirit that exists between various development groups contributes to this blindness; no way will the developer admit that his product can't hack it, but someone else's might.

With the advent of architects, the problem becomes even greater. The architect reviews the potential system in light of his architecture, rather than any specific implementation (with inherent limitations). While the abstract architecture might in fact accomodate the problem, rarely will the 'flawed' implementations be so adaptable.

7.3 As if the previous reasons for ignoring development reviews of the sale were not enough, it should also be realized that Developers rarely have enough time to seriously analyze the application and the stresses it will put on their system, and thus their conclusions are specious to begin with. The developer's priorities are usually first to develop. Sales support functions, such as finding the holes in system proposals, are in his mind a product line function, so he won't put much effort into the activity.

7.4 Thus we end up playing a deadly game of 'chicken'. The product line hopes development will block the sale, and development hopes the product line will, since both are really very scared that the thing won't work; but neither is willing to admit the fact. Sometimes the customer finally 'chickens out' and everybody breathes a sigh of relief; other times a competitor gets the business and everyone is both relieved and disappointed simultaneously. But sometimes, unfortunatley, the customer bites, and the seeds of the disaster take root.

8.1 I don't know why the Texas District spawns problems of this type, but they do abstract more than their share of disasters, specifically:

TSS/8 - Computer Applications
RSTS - C.O.E.D.D.
RSX-11D - Broyles & Broyles
DECNET - Chrysler; Computer Dimensions

The end results of new product disasters

There are two major consequences of new product disasters, and both are not necessarily bad. First, the entire organization learns where the product 'works' and where it doesn't, so we usually don't get burned by the same problem more than once. In effect, we determine the strengths and weaknesses of our products in an expost facto manner. Second, the organization 'turns off' from the product, and no longer sees it as the panacea it once was (even if it was only a virtual panacea). This 'off' period continues until a goodly number of happy reference sites are established to counteract the initial bad impressions. The conservatism induced during the 'off' period, coupled with the learning that occurs, allows Maynard and the field to develop realistic expectations for the product, so that when the product gradually gains acceptance, further disasters are infrequent.

Possible Strategies to avoid future disasters

First, consider whether we want to change the process. Products that survive the current initiation ritual are usually very successful once we learn where and how to sell them. The current mechanism provides information equivalent to or better than much a priori analysis of product capabilities and markets, and the lessons learned at such great pain are rarely forgotten. So we may wish to retain the current masochistic scheme.

We could attempt to spend more time early in the project understanding and specifying the products' behaviour, but to some extent we will never be able to avoid the customer who sees a novel way to use a system that will hit some unknown limit and provoke a disaster. Also, no matter what limits we do specify, someone will always come along who wants to go just a bit further. (Within 48 hours of the appearance of a limit of 4 front-ends on a RSTS/E system, a potential customer walked in who wanted 5.) Handling such situations invokes all the problems previously alluded to.

We could maintain a stricter veil of secrecy around new product developments, in the hopes of avoiding sales during that critical time before product limits are understood. But, we only learn about such limits now from previous disasters, so we might end up rejecting much good business, or not selling anything at all. Further, such a policy makes it difficult to locate field test sites, since the field organization would not know of the potential product. We would also lose much of the openness that characterizes our current customer dealings, and cause customers to be upset when some of them discover they developed at great expense some capability which appears in our new widget just as they 'got their last bug out'.

We could arbitrarily refuse, for some initial period, to sell a new product that was not going to be used totally within spec; i.e., no internal modifications by users would be allowed for the first year or so of product shipments. We could enforce this by restricting sources and listings initially. This too makes us appear non-responsive, and would be difficult to make stick. Getting CSS and/or PL90 involved in lieu of the customer doesn't solve the problem, since they typically have the same problems modifying things as would the user. It seems unlikely we could cause this policy to be accepted; in any event, our inability to specify fully and exactly what our systems can do (and can't do) means that some disasters are still likely to slip through.

We could selectively refuse potential disasters by putting someone with veto power in the sales approval loop for complex new products, probably in the product management area. Such a person would provide in-depth technical pre-sales support to product lines, and have a major say in whether a particular piece of business should be accepted. The principal metric for such a person would be the number of disasters he let through the system. Like a bank loan officer, we would be suspicious if no disasters got through such a filter (i.e., too conservative an approach), and we would get a new person if too many disasters got through. Such a person would have the skills, motivation, and objectivity to reject the bad and accept the good business.

cp

APR 5 1982

+---+---+---+---+---+---+---+
! d ! i ! g ! i ! t ! a ! l !
+---+---+---+---+---+---+---+

INTEROFFICE MEMO

To: Gordon Bell

cc: Don Wunschel - TW/F17
Steve Jenkins - TW/C04
Barry Poland - TW/F17

Date: 2 Apr 82
From: S.Duncan/J.Sarni
Dept: BSDE (VAX Diag)
Ext: 247-2225/247-2870
Loc/Mail Stop: TW/F17
Node: YODA

Subject: COMMENTS ON YOUR DRAFT 'HEURISTICS' PAPER

Steve Jenkins forwarded a draft of your paper "Heuristics and Comments for Building Great Products" to us. He said you were looking for feedback and invited us to send our comments to you.

As Diagnostic Engineers, our principal concern is delivering a product that satisfies the customers maintainability requirements. During the design phase, decisions are made to balance the initial product cost with the cost of ownership. In many cases the metrics needed for making these decisions are not well understood. Your paper does a fine job of explaining to a design team how to meet cost/performance goals. However, we believe more emphasis should be put on the maintainability goals.

You stated that an engineer must understand the design, the design production (CAD), and the manufacturing process. We believe he must also understand the maintenance process (diagnosability in the field). All four are required.

If the development team has an understanding of both the science and the importance of developing easily maintainable systems, we should be able to provide customer installable and maintainable computer systems.

Later in the paper (on top of Page 4) customer maintainability is listed as necessary in all new products. To avoid misunderstanding in this area, a definition of who that customer is would help engineering development groups to meet this goal. I think the customer installable/maintainable goal should specify simplicity and brevity of the installation/maintenance process such that new product developers understand the goal. If the goal is for sophisticated customers to perform the installation and maintenance then we have already achieved that goal.

3/31/82

GB ...

Some comments re: "Heuristics" ... etc. presentation:

- Working from the end ... SELLING & BUILDING THE PRODUCT section seems a rather weak, after-thought and could be incorporated into the other sections with less redundancy and more impact (After all, the main reason we BUILD products is to SELL them. All our sins and virtues as a Company come together at the point of sale ... or shortly thereafter when the customer tries to use the damn thing!!)

- ... Goodness & Greatness ... "be a great system not piece parts" ... This strikes me as a considerable understatement and deserves more "up-front" billing" --- i.e., I believe Engineering would be a very different place today if the focus were on building systems vs. products. It is the responsibility of management to maintain the interdependent, system-focus across the product groups. This addresses the way people work or behave and may belong in the ENGINEERING GROUP/TEAM section.

- One thing conspicuous by its absence is the PHASE REVIEW PROCESS. Aren't there any tips for maximizing it?

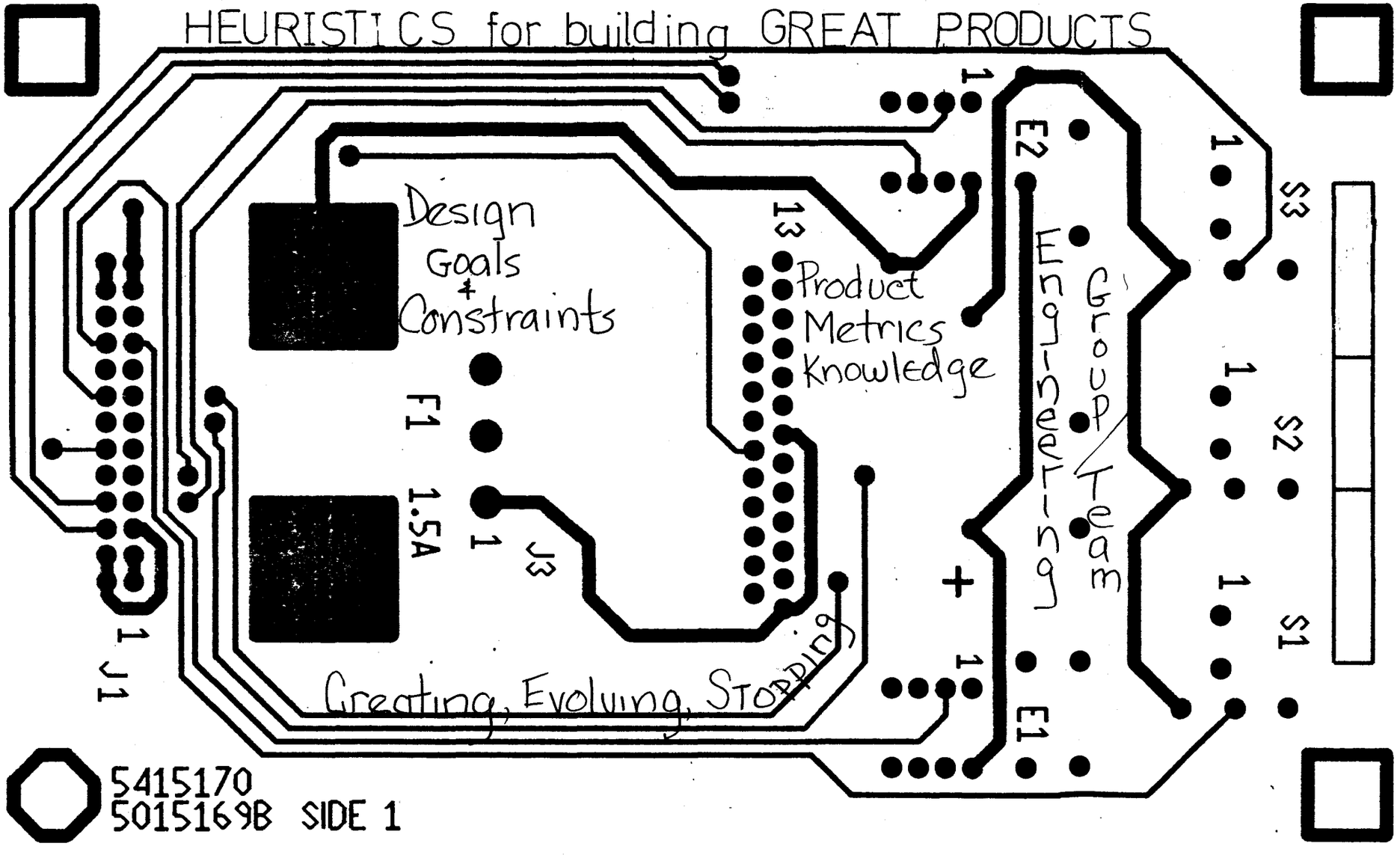
- Your PRESENTATION STYLE ... very animated, informal, and full of conviction: Ideal for this topic ... you're great to watch in action!

- "WORKERS DEMANDING GOOD MANAGERS ... " an excellent addition ... The function seems to have lost its sense of "bottoms-up" responsibility; lots of people seem to be colluding in the irresponsibility of those above them!

- As I said the other day ... the biggest challenge is to get these heuristics into the "hearts and minds of the countrymen"! If this is "RELIGION" how do people "GET IT"?! How do you make this the context in which all work is done? How about HEURISTICS INFORMATION MANAGER (H.I.M.?) (naah)

  ... A HEURISTICS INFORMATION PROGRAM (H.I.P.) (as in ... GET H.I.P.!!) I would work the main ideas into a visual format ... for a poster or one-page hand-out (see attached).

- MOST IMPORTANT: THE HEURISTICS CONCEPT HAS THE POTENTIAL OF BEING THE GLUE WHICH HOLDS THIS FRAGMENTED, UNFOCUSED, ILLUSION CALLED CENTRAL ENGINEERING TOGETHER!!!



JO BURT DECGRAM ACCEPTED S 2790 O 151 21-FEB-82 13:55:32

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* d i g i t a l *
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TO: KEN OLSEN

cc: see "CC" DISTRIBUTION

DATE: SAT 20 FEB 1982 1:40 PM EST
FROM: GORDON BELL
DEPT: ENG STAFF
EXT: 223-2236
LOC/MAIL STOP: ML12-1/A51

SUBJECT: THE BEST WAY TO GET A LOW COST VT100... A COUNTERPROPOSAL

There was a clear screwup when there wasn't a plan to get the low cost VT. Cathy and Bill should have gotten this issue to us.

PROPOSAL---I think we want to strive for excellence by:
1. Having Barry lead us in the CP/M and other products based around the z80 and 8086. Here, the competitor is the IBM PC and we need someone full time to concentrate on IBM. I believe Barry is up to the beat IBM task, but I don't think it's fair to ask him to beat both IBM and all the companies such as ATT who are going to be designing the product you should be dreaming of (it interfaces to a phone nicely).

2. Having the VT200 group go ahead as planned, I think they fundamentally are going to perform best by working on advanced video and relatively lower cost, higher performance products. I don't think they are oriented to building the very low cost products. Here, let's really review this again and why it can be done.

3. Chartering a NEW group to do very low cost follow on products. In Taiwan we have a motivated, creative engineering group that can take on this contained problem because the specification is well-defined. They have done first rate monitor work, and I'd like to see them go after this one.

HISTORICAL OBSERVATION ON PRODUCT DEFINITION FORCES:
IN ORDER TO GET A DRASTICALLY LOWER COST VERSION OF THE SAME PRODUCT, WE HAVE USUALLY HAD TO DO IT BY ESTABLISHING A NEW ENGINEERING, and sometimes a new marketing GROUP due to forces:
- marketing wants lost sales features
- marketing has an established channel and customer base, getting a new low cost product screws up the status quo... inventories, requires new customers, new applications, etc. (The small car.)
- engineering is safer and more challenging when providing a constant cost product with more performance and features (eg. 11 40,34,44,LA120,VT100
- engineering isn't interested unless there's a technology for it which also gets both lower cost and same performance (5,8,8/I, 7,15,LA36,LSI-11, VT125 follow on
- engineeing knows the greats are lower cost and more performance as in the PDP-8 and VT100. We all want to engineer greats!
- engineering is leary since every product we have built which lowers cost AND performance has been a loser (8S,VT50,LA34,PDT) It gets confused that we have to maintain the performance, and get drastically reduced cost! Losing performance too always

loses.

We've all seen the large yawn (and the departure of the engineering management) that greeted the VT101/131/etc. that were just a simple, neglisible cost reduction of the VT100. No marketing folks are to be found as part of this.

MANAGEMENT BACKGROUND:
We could tease Cathy and Barry to do a low cost VT. I like what I see in Cathy's lab and on her schedules. They have a dedicated group and are going to get us a great product quick.

Barry and his group are doing a fabulous job. The person I most admire in building computers, Seymour Cray, builds one machine at a time, with a group about the same size as Barry's. I'm tired of pushing our really good engineering groups to become mediocre by trying to do every possible product in a half assed way. Each one of these products requires careful engineering thought on a 24 hour a day basis for a period of 6-12 months. The groupp could probably rise to the size and can do anything that they want to, but I believe they are going to sacrifice the potential of CAT and what it should be! I'm sure Barry has all sorts of creative options like voice, Wini, IBM emulation, WPS, Wang emulation, and every conceivable software package. LET'S HAVE BARRY'S GROUP CREAM IBM IN THE PC MARKET WITH CAT. Somehow, i believe this is a full time job for a superb engineersing and marketing group that i see emersing. I hope barry is smart enough to take on this challenge by not getting involved with the tangential effort of making lcvt. Excellence only comes out of focus.

I really believe in small, focussed engineering groups because they out perform our large ones by an order of magnitude. THE ONLY REASON TO HAVE BIG ONES IS FOR THAT THE PROJECT WORK DEMANDS IT. Note too that virtually every time we take on these large projects, they are virtually impossible to manage effectively and get done on time. We simply don't know how to manage and motivate a large group over a long time. Every time a group gets really big, we get communications problems, bad morale due to low personal output, lack of product target, long schedules, and worst of all... a potential poor product.

Anyway, here's some food for thought in how we:
get lcvt
do engineering that's going to beat the Japanese
and organize

"CC" DISTRIBUTION:

BILL AVERY BARRY JAMES FOLSOM WALTER HANSTEIN
JACK SMITH

ATTACHED: MEMO;56

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* d i g i t a l *
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TO: BILL AVERY
GORDON BELL
BARRY JAMES FOLSOM

DATE: FRI 19 FEB 1982 10:30 AM EST
FROM: KEN OLSEN
DEPT: ADMINISTRATION
EXT: 223-2301
LOC/MAIL STOP: ML10-2/A50

SUBJECT: TERMINALS ENGINEERING GROUP TASK

I like the way the Display Terminal Group is organized now and I think Cathy is doing a good job. However, they are only interested in making a significant technical contribution with our products, and probably not interested in something that might be very important to the customers and the Company but with little technical contribution.

It seems to me last September when we charted out the products of the Corporation and the Heald Pond Woods, we concluded that what was necessary was an immediate and inexpensive replacement for the VT100. The Terminal Group has a better idea. They want to wait longer and make a VT100 with VT125 features, and they have another product which has VT100 features but is very, very inexpensive but a long way away. When you look at the needs of our customers and all those customers we do not have, and the financial needs of the Corporation, it was clear last September and probably is still even more clear, we need immediately a very inexpensive, very simple terminal that will just handle simple black and white data.

Maybe we should turn over to the Terminals Engineering group, this mundane unexciting task, and request that they make no technical contribution just do what the VT100 does - do it quickly and simply as possible, and only add a plug-in modem as a new feature.

Because this task is so well defined, they might be able to whip it out very quickly and fit it in a very, very small box.

The machine that the Terminals Group is doing is going to have VT125 features with the price of a VT100. That's not the measure. The measure is what is the least expensive VT100 we can make in the smallest amount of space, and in the quickest time to take care of those millions of applications which don't need any more features than the VT100 has.

Should we turn this over to the Terminals Product Line to do since they have less technical pride and are closer to the customers?

KHO/ep
KO1:S9.45

APR 8 1982

+----------+
! D I G I T A L !
+----------+

INTEROFFICE MEMORANDUM

DATE: APRIL 5,1982
FROM: MIKE ROBEY
DEPT: C.S. MAINT ENG.
EXT : 5067
LOC : MR1-1/S35
FILE:

SUBJECT: Your draft regarding "Building Great Products"

I have read your document, found it quite interesting and valuable, and offer the following comments:

1. RELIABILITY

I found the term reliability mentioned only once in the document and believe you have missed an opportunity to stress that this is a very significant aspect of a "Great Product". While it is possible that you are implying this under the guise of "working machine", "cost of ownership", or "performance" I really don't see the message. It is interesting that I have had a serious problem communicating with the hardware engineering community when the word performance is used. It always means "how fast" not "how often".

2. MAINTAINABILITY

Except for pushing the responsibility off to the customer I don't think you have owned up the the fact that this is currently a big contributor to DEC's costs and customer perceptions of poor quality. This will probably continue to be a challenge in the large computer system area. Once again, assuming that there is no perfectly reliable design, a "Great Product" must be capable of being restored to operation with a minimum amount of System down time and at a minimal service cost.

3. CUSTOMER INSTALLABLE/MAINTAINABLE/PORTABILITY

I am not convinced that large computer systems require any of these characteristics and might suggest that quality would be seriously impaired if we tried to force these ideas. There is no doubt that the customer is expected to be quite involved with both Installation and Maintenance of large systems, and we must design for this, but lets not oversimplify it by suggesting that they will have the resources and expertise to do it all themselves.

4. POOR "MIND-SET"

I think this is a good point to make and personally think that the

"one shoe" fits all idea in packaging is a negative contributor to optimizing reliability visavis thermal design. At day 1 someone says it will fit in this box. Then we determine the functionality and logic requirements and subsequently squeeze it all in. At every step our ability to improve reliability is impacted.

You must forgive me if I seem overly critical of the attention that you are giving to reliability (We all have our axes to grind). We are currently building the HSC5Ø and PLUTO for every reason in the world except for inherent product reliability. These products are far more unreliable that their historical functional counterparts and I have seen no aggressive reliability goals for either.

While there are lots of interesting things that we could do to increase reliability, it seems to me that our thermal design technology and parts procurement process (ie. higher quality parts) are in need of serious review.

In conclusion I'd like to make it clear that most of the content of your document will, in my estimation, improve our chances of building great products.

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DIGITAL
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TO: [redacted]

CC: Dick Albright, QI-1/B20
Don Metzger NR1-5/B98
Joe Chenail QI-1/B17

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INTEROFFICE MEMORANDUM
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DATE: 8-APR-82
FROM: Jack Arabian
DEPT: Adv. Test Tech.
EXT: 280-7234
LOC/MAIL STOP: QI-1/B20

SUBJECT: INPUTS TO GORDON BELL'S, DESIGN FOR THE '80's SEMINAR.

This is an input for your preliminary draft, entitled, "Heuristics and Comments For Building Products".

1. A design methodology should include not only design conventions but also, design for testability. As all projects should have open and external design reviews, these reviews should include manufacturability and testability considerations by participation of interested groups. It is just as important to be able to manufacture the product and test the product as it is to design and verify the product.

2. Individuals should consider the total educational process as a continuum. If one were to wait every 10 years to take a semester of technical courses, he would be way behind in the technology, especially in the computer business. Modern engineers should attend conferences and participate in the day to day data exchange programs which advance the state-of-the-art. Taking courses in an accredited university these days does little to advance the state of the art. The professors and the courses are already years behind the state-of-the-art.

3. "Product Metrics Knowledge" should include the cost to test the product.

4. Poor "Mind-set" standards can create poor products: this phrase is true, but the example of a 19 inch rack leaves some question in the minds of the design community. A 19 inch rack is a standard or convention which is used internationally and as stated previously, standards or conventions are good. Perhaps additional standards or conventions may be used, but the 19 inch rack should not be assailed as part of the poor mind set.

   An additional definition of quality can be stated as follows: "Quality means that it was conceived, designed and built with a little bit of love".

5. *On the subject of "Selling and Building the Product": Simplicity as a rule for our documentation is a good rule, a better rule is to require that documentation must exist. Documentation is needed not only for the commercial customer, but also for the test engineer who must verify its operation years after the product was designed. In other words, lets make documentation simple, but let us at least make it complete in order for the product to be tested and manufactured.*

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DIGITAL
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INTEROFFICE MEMORANDUM
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TO: Gordon Bell
Dick Albright
Joe Chenail
Don Metzger

Date: 8-APR-82
FROM: Ernst Ulrich
DEPT: ATT
EXT: 280-7237
LOC: QI-1/B20

E.U.

SUBJ: Inputs to "Heuristics and Comments for Building Products."

My views are based on my CAD background and CAD teams, and are not necessarily totally transferable to design team scenarios.

In CAD, and probably in other areas, DEC is still not giving enough attention to outside technical developments.

We should persuade our good "lone wolves" to work within small technical teams. The small team rather than the individual or the large team is a key ingredient for success in our kind of work. In CAD there are several excellent individualists (e.g. Armstrong, Elkind, Helliwell) who would probably be even more successful by working within a small team.

Key people, once on an important job, should not find it so promiscuously easy to abdicate their responsibility and find another job within DEC. The great DEC climate of individual freedom is probably the cause for this. We should find a balance between freedom and responsibility abdication.

Ideally, every design team should include expertise in CAD, simulation, and testing. Very few designers understand these disciplines. Let's train a few people to fill this vacuum.

There exist alternatives to going back to school for a year. I follow the technical literature and go to conferences. This may give me more up-to-date information than academic courses.

It is probably true that design is 90% evolution and at best 10% revolution. From this it follows that history, and probably fashion, play important roles in computer design.

On elegance and quality. SIMPLICITY and PRACTICALITY should be mentioned in the same breath. More on this below.

Technical people, I think, fall into two classes: Complexity lovers and simplicity lovers. The former are usually wrong and the latter usually right. Simplicity lovers tend to be practical and complexity lovers impractical. Management should find simplicity lovers and put one on each important project.

Strategic and tactical talent is unevenly available. Good strategists are rare, and a combination of strategic and tactical talent within one person is very rare. The system, however, tends to push good tacticians into the role of strategist, at which they usually fail. Recognition of this problem is half the solution.

Money isn't enough. The industry has spent huge sums on CAD and has received relatively little in return. The successes have usually been achieved by very small teams of strong individuals, and by teams having a good mixture of strategic and tactical talent. I think this is universally applicable.

NOV 30 1982

To: Operations Committee 11/29/82 background attached
Ken asked that we all learn from our problems with ROBIN. Here are Art Campbell's views on the lessons learned
Please share this with anyone you believe can also learn.

* * * * * * * * *
* d i g i t a l *
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INTEROFFICE MEMORANDUM

TO: Win Hindle
Andy Knowles

NOV 15

DATE: 15 November 1982
FROM: Art Campbell
DEPT: Terminals Product Group
EXT: 278-4038
MAILSTOP: UP1-4

Win

Copy: Technical Comps Staff

Note: There is also an Internal Audit Report if you want more detail

SUBJ: Lessons Learned on Robin

The following is my summary of the key lessons we learned on the Robin Program, per our discussion:

1. Market Analysis and Sizing

We overestimated the market size for Robin. Robin was targeted as a personal computer upgrade to a VT100. Due to the very rapid growth of the personal computer market, we projected that at least 10% to 20% of the VT100 users would want a personal computer. We did not attempt to confirm that percentage with formal studies.

We have recently completed a formal survey of 200 VT100 users in a wide cross section of companies. That data suggests that the upgrade market is approximately 5% of the installed base.

Lesson - Don't shortcut the market analysis and sizing studies, even when the conclusions seem obvious.

2. Pricing and Competitive Positioning

Because we were targeting Robin as an upgrade option to an existing VT100 user, we were concerned only with the upgrade price. It did not worry us that the price of a VT100 plus the upgrade was very high. After all, this was not Digital's mainline personal computer, that was yet to be announced.

In retrospect, we we too impressed with minor features of our product versus the competition. We priced the upgrade kit at $2400 ($2650 with CPM), when you could buy an entire personal computer from Xerox for $2995.

Part of the reason we set the price that high was our determination to breakeven in FY'82. The project was proposed after profit budgets were final. We were being pressured to present a plan which paid it's own way in FY'82, or not be allowed to implement it. We believed we could get $2400 for our product. We believed we could breakeven with only six months of shipments. We were wrong.

Lesson - Don't overestimate the value which the market will pay for product features, especially if you are a late entrant into a market. Also, don't let budgeting pressures cause you to make pricing decisions that make you uncompetitive. Don't commit suicide in the financial plan.

3. Unique Product Status

Robin was a unique product to the Terminals Product Group. We did this to get it to market as soon as possible (without having to lobby with all other product groups), and to get all the revenue into TPG so that the sales would repay our development expenses as fast as possible. However, the price paid for unique products in terms of a lack of support in the entire sales and marketing organization, is too high for the benefits achieved.

Lesson - Product line unique products are losers. Although the process may be slower, and the allocations of revenues versus expenses unfair, we have to have corporate products that are understood and supported by everyone in order to win.

4. Market Window

When Robin was proposed, we targeted an FCS date of January 1982. The PC Family announcement was then targeted for September 1982. We planned on a nine month window in the market before DEC's big gun products in the space were announced.

We missed our January ship target. We were not able to ship Robin until March (still only eight months from proposal to FCS). In addition, the PC Family announcement was pulled in to May. Thus, the market window reduced from nine months to three months.

We did not reposition Robin at the time of the May announcement because we believed it was not necessary at that time. We were wrong. We should have repriced and positioned Robin in May and made it an integral part of our PC Family announcement.

Lesson - Be prepared for dramatic changes in the competitive environment with contingency plans already thought through. Be able to react swiftly through prior planning.

5. Resource Limitations

The entire Robin program, both in engineering and marketing, was implemented with a small resource team. When the decision to pull-in the announcement of the PC Family to May was made, the Robin team was reassigned to that higher pirority program. We lost

emphasis on Robin in both engineering and marketing. We fell below critical mass. We were worried about it, but believed we could do "everything" by just working even harder. We should have been more vocal about our concerns and forced a different allocation of resources so that both Robin and the May announcement could have been adequately supported.

Lesson - Raise to the highest levels the visibility of resource limitations that affect a project's ability to succeed, even if problems don't become visible until after the fact.

6. Product Quality

Robin uses a standard, high volume floppy disc drive for disc storage. It is built by Shugart. Although they have delivered more than one million of these drives, there is an inherent problem in the design regarding media seating. If the spindle is not spinning when a floppy is inserted, there is a high likelihood that it will not center properly on the spindle, and thus it cannot be read by the system. The user has to reinsert the floppy until it seats properly.

We were aware of this problem by January 1982. Since it was an industry situation common to PC users we decided to ship Robin as is. That was a mistake. The users perceived the Robin system as poor quality due to this seating problem.

We put the product on engineering hold after the first 90 days of shipments to ECO our design to solve the problem. (We now spin the spindles continously when in CPM mode.) We were on hold throughout Q1 FY'83 while implementing this ECO.

Lesson - If the user perceives that a product has a quality problem, you're dead. Never ship a product that the user will perceive as poor quality, without a timely solution in hand and visible to the customer.

/p

APR 8 1982

Russ Doane AdvMfgTech ML1-5/T55 223-6707 DIGITALmemo 4/5/82

to Gordon Bell

KEEPING GOOD PEOPLE
(a reaction to your Spit Brook talk)

Your personal warmth is one of the things that helps keep good engineers at DEC, in combination with your technical appreciation. Neither your love alone without the technical appreciation, nor the technical appreciation alone without the love could do what you do.

That's why Dave Cain singled you out in his departure memo as the one signer of the VAX success poster who had personally communicated your appreciation of him. That meant a lot to Dave.

It meant a lot to me to get a warm note from you about my "Introduction to the MOS Design Style...". And honorable mention in your "heuristics..." draft (elegance=pun).

It means a lot to any design team to have Gordon Bell speak of the things they did well as public examples to be emulated. To get Honorable Mention in your publications. To be praised in the marginal notes you write when responding to memos.

Being in the audience at your Spit Brook "Design for the '80s" talk, it occurred to me that you sometimes choose a style that waters down the contribution you make in this area. Namely: focussing more on failures than on successes.

Negative focus is part of engineering. We're here to solve PROBLEMS. That's how we think of ourselves.

But OPPORTUNITY is what brings people together. At Spit Brook your heaviest theme was what went wrong with Venus. I believe the same lessons could be extracted, though with greater effort, from what went right in successful projects. As you did with Robin.

And the audience can leave with an attractive vision: what I WANT my project to look like.

From my perspective, there is enough put-down and macho around DEC to impact productivity and make feet itchy. People love you and try to emulate you. I wish you'd more often use positive examples and publicly analyze successes.

HEURISTICS FOR BUILDING GREAT PRODUCTS
(DRAFT FOR COMMENT)

FIVE SETS OF DIMENSIONS FOR BUILDING GREAT PRODUCTS NEED BE ATTENDED TO (ROUGHLY IN ORDER OF IMPORTANCE):

- A RESPONSIBLE, PRODUCTIVE AND CREATIVE ENGINEERING GROUP;

- PRODUCT AND DESIGN METRICS (COMPETITIVENESS);

- DESIGN GOALS AND CONSTRAINTS;

- {Process} PRODUCT EVOLUTION, REVOLUTION AND DEATH; AND

- THE ABILITY TO GET THE PRODUCT BUILT AND SOLD.

ENGINEERING GROUP

THE TEAM MUST HAVE:

- A CHIEF DESIGNER/CHIEF PROGRAMMER TO FORMULATE AND LEAD;

  NO COMMITTEES AS DESIGNERS

- MANAGEMENT WHO UNDERSTAND THE PRODUCT SPACE AND WHO HAS ENGINEERED SUCCESSFUL PRODUCTS; THE TWO MOST IMPORTANT JOBS ARE:

  - MAKING SURE THAT EVERYONE KNOWS THEIR JOB; AND

  - ESTABLISHING AND REVIEWING WORK ON A TIMELY BASIS, I.E. MBO.

* → Workers must start demanding good management.

- TEAM SKILLS AND RESOURCES TO IMPLEMENT THE PROPOSAL SO THAT WE ADHERE TO THE CARDINAL RULE OF DIGITAL, "HE WHO PROPOSES, DOES";

- AN UNDERSTANDING OF THE DESIGN, DESIGN PRODUCTION (EG. CAD) PROCESSES, AND MANUFACTURING PROCESSES.

"EVERYONE IN SEG/CAD HAS A RIGHT TO BE WELL MANAGED"

Arnie Goldfein

YOU HAVE THE RIGHT TO:

- HAVE A JOB THAT CHALLENGES YOU TO THE LIMITS OF YOUR PROFESSIONAL ABILITY
- KNOW WHAT YOUR MANAGEMENT THINKS YOU SHOULD BE DOING
- KNOW HOW YOUR WORK RELATES TO DIGITAL'S BUSINESS AND YOUR ORGANIZATION'S PLANS
- KNOW WHAT YOUR MANAGEMENT THINKS OF YOU AND YOUR WORK
- HAVE ENOUGH RESOURCES TO DO YOUR JOB
- HAVE AS MUCH OPPORTUNITY FOR JOB-RELATED PERSONAL GROWTH AND LEARNING AS YOU CAN SUCCESSFULLY HANDLE
- BE COMPETITIVELY REWARDED FOR YOUR WORK
- HAVE A CLEAR UNDERSTANDING OF YOUR CAREER OPTIONS AND PATH

(NOTE: THE MANAGEMENT "RITUALS" OF O & KR AND REGULAR ONE--ON-ONE'S GUARANTEE THAT YOU CAN GET CALIBRATED AS FREQUENTLY AS YOU NEED.)

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DIGITAL
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INTEROFFICE MEMORANDUM

TO: SEG/CAD Users

DATE: 11 January 82
FROM: Army Goldfein
DEPT: SEG/CAD
EXT: 225-4926
M/S: ML2-2/J13
DECNET: ELSIE::GOLDFEIN

SUBJECT: SEG/CAD, Objectives and Key Results
Q2 FY82, Rev. 0

I. Increase speed, reliability, maintainability of the CHAS custom-MOS integrated design system, while extending it's functionality to include schematic entry (DECDRAW), RTL simulation (DECSIM), and graphic output from circuit simulation (SPICE).

A. Publish a revised CHAS architecture document. (2/20) /

B. Publish performance analysis study of CHAS Version 2. (1/31) /

C. Release CHAS Version 2.1 with bug fixes and some performance improvements. (1/20)

D. Implement architectural changes to CHAS data base, menu-actor interface, and actor dispatching in CHAS Version 3. (3/20 field test) /

E. Publish CHAS Version 3 interface specifications that detail the CHAS/DECDRAW, CHAS/DECSIM, and CHAS/GRAPES interfaces. (2/20) /

F. Release CHAS Version 3 field test on CHIPS and SHORTY. (3/20) /

II. Provide MOS design engineers with a production quality MOS schematics drawing system (DECDRAW). The delivered tool should meet the users requirements for scheduling and function.

A. Install and demonstrate DECDRAW Version 1.0 on CHIPS, SHORTY and NANCEY. (2/15) /

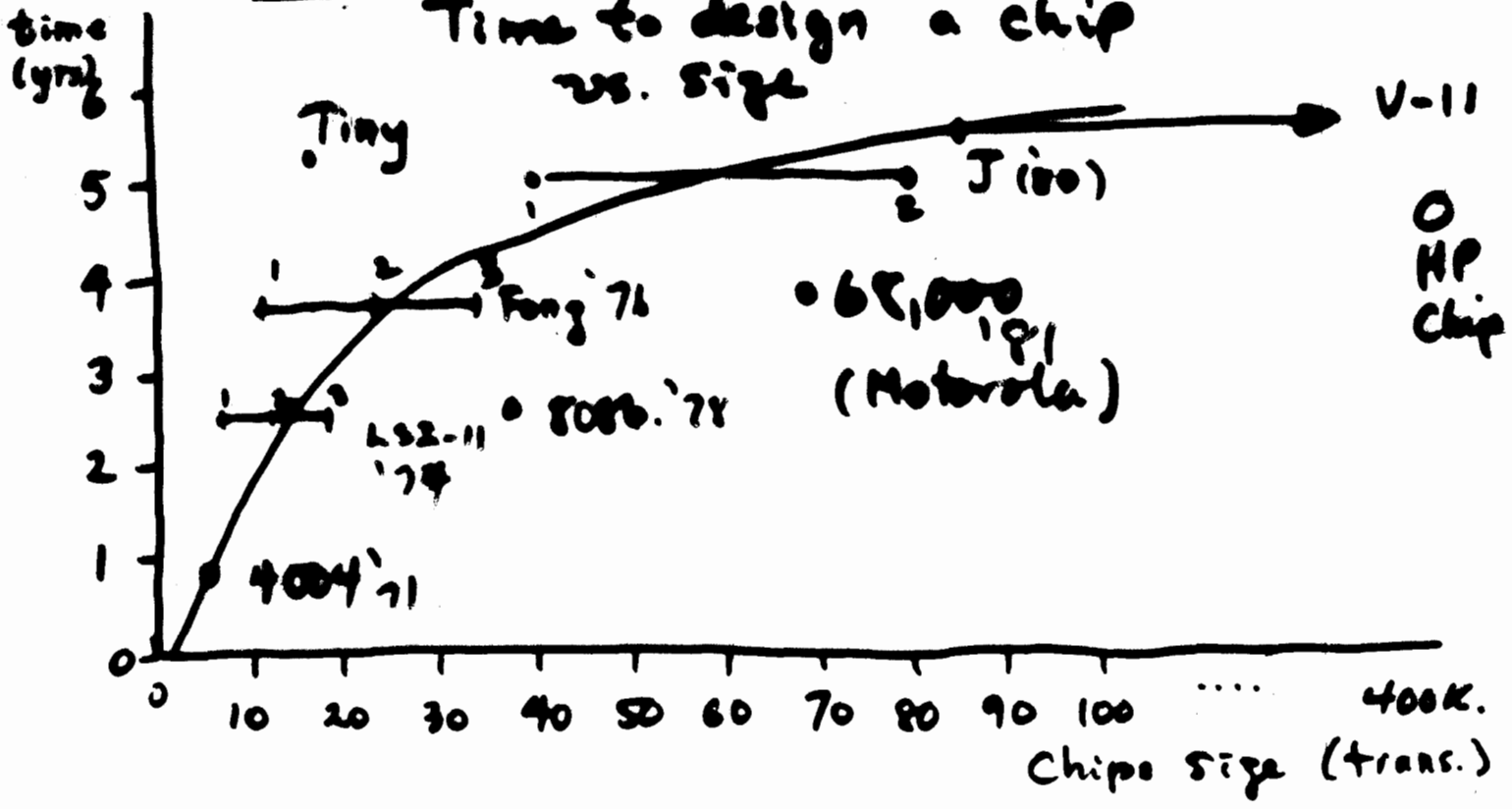
B. Install and demonstrate DECDRAW Version 2.0 on CHIPS, SHORTY and NANCEY. (4/1) /

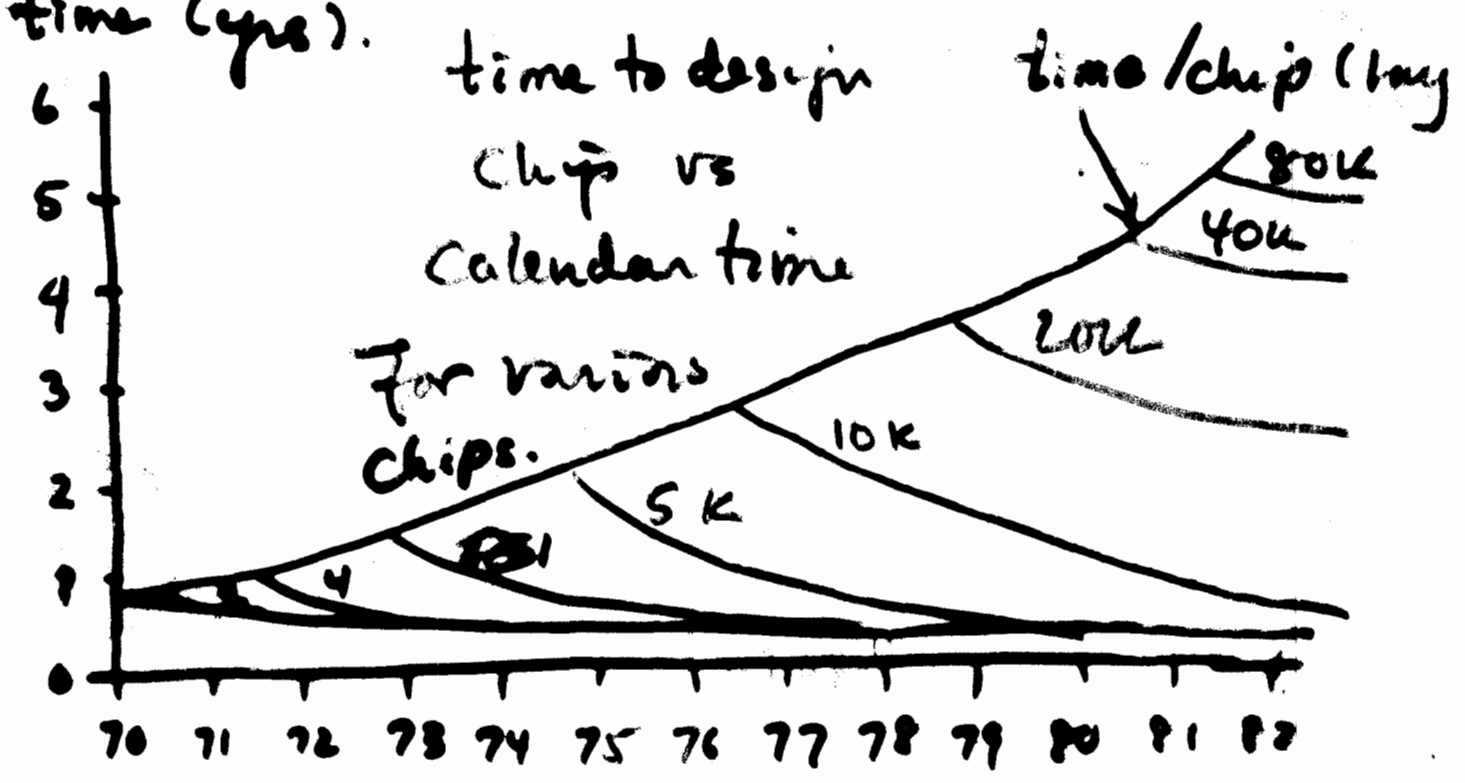
SEG/CAD Objectives and Key Results
Q2 FY82, Rev. 0

KEY RESULTS

Key Results			Orig. Date	1/18 1	1/25 2	2/1 3	2/8 4	2/15 5	2/22 6	3/1 7
		CMAS								
I.	A.	Architectural Docu.	2/20	2/20	2/20	2/20	2/20	2/20	(2/26)	(3/3)
	B.	Performance Analysis	1/31	1/31	1/31	(2/2)	{2/3}			
	C.	V2.1 Release	1/20	(1/22)	{1/22}					
	D.	Version 3 Field Test	3/20	3/20	3/20	3/20	3/20	3/20	3/20	(4/26)
	E.	Version 3 Interface Specs	2/20	2/20	2/20	2/20	2/20	2/20	(2/26)	(3/3)
	F.	Version 3 Field Test	3/20	3/20	3/20	3/20	3/20	3/20	3/20	(4/26)
		DECDRAW								
II.	A.	Install V1.0 on CHIPS	2/15	2/15	2/15	2/15	2/15	2/15	(2/15)	(2/15)
	B.	Install V2.0 on CHIPS	4/1	4/1	4/1	4/1	4/1	4/1	4/1	4/1
		DECSIM								
III.	A.	V1.0 Release	2/3	2/3	2/3	2/3	{2/3}			
	B.	Publish MOS Spec	2/26	2/26	2/26	2/26	2/26	(3/12)	(3/12)	(3/12)
	C.	Fault Sim. Func. Spec.	3/15	3/15	3/15	3/15	3/15	3/15	3/15	3/15
	D.	Test current Fault Sim.	3/30	3/30	3/30	3/30	3/30	3/30	3/30	3/30
		Auto Layout								
IV.	A.	Publish TAT008	1/31	{1/12}						
	B.	Publish TAT020	3/31	3/31	3/31	3/31	(4/23)	(4/23)	(4/23)	(4/23)
	C.	Production System Plan	2/28	2/28	2/28	2/28	2/28	2/28	2/28	(3/15)
	D.	FINCUT into IDEAS	3/26	3/26	3/26	3/26	3/26	drop		
		Layout Verification								
V.	A.	ZMOS/NCA Rules File	2/1	2/1	2/1	(2/15)	(2/15)	{2/15}		
	B.	ZMOS/GDS2 Rules File	2/15	2/15	2/15	2/15	(2/17)	(2/17)	(2/17)	(2/17)
	C.	MOSAIC Rules File	2/1	2/1	{2/1}					
	D.	Release ERC	2/7	2/7	2/7	(2/15)	{2/15}			
	E.	Release NCC	2/15	2/15	2/15	2/15	2/15	(2/19)	{2/22}	
	F.	IV Functional Spec	2/1	2/1	(2/8)	(2/8)	2/15	{2/12}		
	G.	HDRC Design Spec	3/15	3/15	3/15	3/15	3/15	3/15	3/15	3/15
		Circuit & Technology Simulation								
VI.	A.	Release SPICE with MOS4	1/18	(2/22)	(2/22)	(2/22)	(2/22)	(2/22)	{2/22}	
	B.	Release SPICE with MOS5	2/15	(3/1)	(3/1)	(3/1)	(3/1)	(3/1)	(3/1)	(3/8)
	C.	Release SPICE with MOS6	3/15	(4/1)	(4/1)	(4/1)	(4/1)	(4/1)	(4/1)	(4/1)
VII.	A.	Publish SUPREM supt. plan	2/22	2/22	2/22	2/22	2/22	2/22	(3/1)	{3/1}
	B.	MINIMOS Compile on 11/780	3/15	3/15	3/15	3/15	3/15	3/15	3/15	3/15
	C.	Run MINIMOS test case	4/5	4/5	4/5	4/5	4/5	4/5	4/5	4/5

Timeliness


Time to design a chip vs. Size
time (yrs)
Tiny
V-11
J (80)
HP Chip
Fong '78
8086. '78
(Motorola)
LSI-11 '78
4004 '71
0 10 20 30 40 50 60 70 80 90 100 .... 400K.
Chips Size (trans.)


time (yrs).
time to design Chip vs Calendar time for various chips.
time/chip (low
80K
40K
20K
10K
5K
4
70 71 72 73 74 75 76 77 78 79 80 81 82

WHAT IS A DESIGN METHODOLOGY?

PROCESS CHARACTERIZATION

DESIGN STEPS, TIMES, LEARNING, SCHEDULING

DESIGN REPRESENTATION

[PHYSICAL,FUNCTIONAL] X [LEVELS] X
[AMOUNT AND KIND OF DETAIL]

CONVENTIONS (FOR NAMES) AND RULES FOR CREATING THE DESIGN

WHAT ABOUT A MODERN DESIGN SYSTEM

ONE DATABASE THAT HAS ALL SIGNALS, BOXES AND THEIR DEFINITIONS

HIERARCHIAL, WITH TOOLS TO CONSTANTLY CHECK ALL ASSERTIONS...

NO FEEDING FORWARD OF DESIGN THROUGH A SERIES OF PROGRAMS

INTERACTIVE

SIMULATION AND VERIFICATION ARE ESSENTIAL

HOW CAN WE REDUCE THE TIME TO INTRODUCE PRODUCTS?

BY DOING QUALITY ENGINEERING... NO REWORK IN THE TESTING PHASES

GETTING THE QUICK TURN AROUND PROCESS TO A WEEK
(PRINTS TO CORRECTLY BUILT MODULE)

MID-LIFE KICKERS AND MULTIPLE IMPLEMENTATIONS PER DESIGN → Less work

---

WHAT IS QUALITY DESIGN?

FUNCTIONAL SPECIFICATION IN A WORKING, DESIGN LANGUAGE

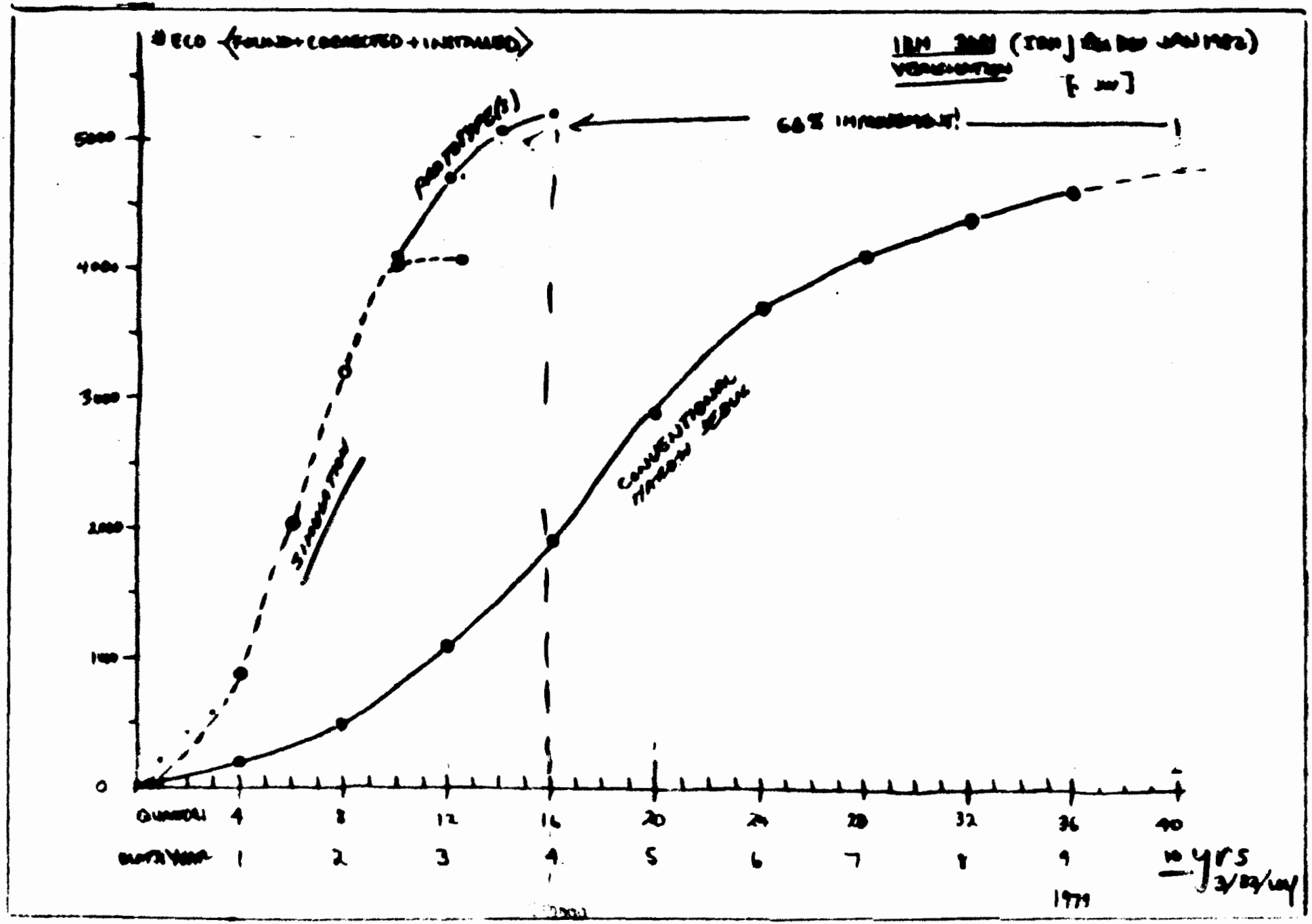
Detailed
QUALITY DESIGN

CHECKING OF THE DESIGN BY DESIGN WALK-THROUGH (CODE WALK THROUGH)

SIMULATE AND VERIFY THE DESIGN. PREPARE TEST DATA

BUILD IT AND VERIFY THAT IT WORKS AS DESIGNED

IBM 3081


5000
4000
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4
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12
16
20
24
28
32
36
40
1
2
3
4
5
6
7
8
9
10 yrs
1979

VENUS: NOW

CHIEF DESIGNER:	ALAN KOTOK
MANAGEMENT:	BOB GLORIOSO, PRIMARY FOCUS IS ON PROJECT
TEAM:	HIERARCHY
DESIGN METHODOLOGY:	PROCESSES WRITTEN; HIERARCHY OF SPECS; QUALITY-BASED DESIGN VS. SCHEDULE BASED; DESIGN WILL WORK BEFORE ITS BUILT; DESIGN PROCESS MODEL
UNDERSTANDING:	INCREASING; COURSES ON COMPLEXITY AND SW ?
REVIEWS:	A HIERARCHY; MONTHLY WITH MILESTONES
GOALS:	WORKS; TIME TO MARKET; PERFORMANCE; COST

Basics

VENUS: WHAT WENT WRONG?

CHIEF DESIGNER:	0,1,2,3,4?
MANAGEMENT:	3 LEVELS; DISCONNECTED FROM PROJECT; LACK OF RIGHT REVIEWS; FOCUS ON PROCESS, NOT PRODUCT
TEAM:	CONTRACT PRECEEDED TEAM; ORGANIZATION MUDDY
UNDERSTANDING:	POOR ON HOW TO DESIGN; CAD OK: MFG. VERY GOOD
TIMELINESS:	PROJECT ALWAYS 27 MONTHS AWAY; PLAN DIDN'T SUPPORT THE SCHEDULE
DESIGN METHODOLOGY:	WORD OF MOUTH, TOO MUCH PAPER, DESIGN TO SCHEDULE, BUILD A BREADBOARD THEN REDESIGN IT!
REVIEWS:	INADEQUATE; MISALIGNED GOALS
LEARNING:	INADEQUATE KNOWLEDGE ON HOW TO DESIGN, COMPLEXITY MANAGEMENT, AND SCHEDULING
PRODUCT METRICS:	FINE
GOALS:	MUDDY... NOW IT'S TIME TO MARKET
CUSTOMER INSTALL:	FINE
ELEGANCE & QUALITY:	TOO MANY IDEAS (AND PEOPLE)

Basics What was learned from Robin (VT18x)

PROJECT MANAGEMENT

time-to-market = 8 mos

- o RECOGNIZE THAT TIME, NOT MONEY, IS THE ENEMY:
  - TIME IS THE RESOURCE TO BE CONSERVED
  - MONEY IS USED FOR MAKING TRADE-OFFS
- o FIRM UP AND GET COMMITMENT TO THE PRODUCT SPEC/BUSINESS PLAN, HAVE CUT-OFF DATES, STICK TO THEM - NO SURPRISES!
  - IF YOU HAVE TO CHANGE, MAKE SURE THE BENEFIT IS GREAT ENOUGH FIRST TO JUSTIFY EVEN DETERMINING WHAT THE COST MIGHT BE
- o USE GOOD PROJECT MANAGEMENT
- o REVIEW PROGRESS - MEASURE IN DAYS/WEEKS FROM THE TARGETED END DATE.

Robin

PROJECT MANAGEMENT (CONT'D)

- USE GOOD PROJECT MANAGEMENT
  - GIVE ONE PERSON YOU TRUST CLEAR OWNERSHIP
    - PROJECT/BUSINESS - GENERALIST
  - STAFF X-FUNCTIONALLY WITH GOOD, DEDICATED PEOPLE
  - PUT THEM PHYSICALLY CLOSE TOGETHER
  - GET CORPORATE BACKING
  - CREATE A STRONG TEAM FOCUS
  - PLAN THOROUGHLY - DESIGN IN PARALLELISM,
  - MAKE SURE YOU HAVE ENOUGH MONEY
  - DON'T CHANGE THE SPECIFICATION
  - STAY AWAY WHILE THE WORK IS GOING ON
  - HAVE A CLEAR, QUICK, "BUBBLE-UP" DECISION-MAKING PROCESS IN PLACE
  - REVIEW PROGRESS, MEASURE IN DAYS/WEEKS FROM END DATE
  - FOCUS ON TIME AS THE ENEMY
    - "HOW CAN WE MAKE THE DATE?"

      NOT

    - "WHY WE ARE GOING TO SLIP."
  - SET A CLEARLY DEFINED/FIXED PRIMARY PRODUCT/PROJECT GOALS - UNDERSTAND AND MAKE SECONDARY GOAL TRADE-OFFS AGAINST THEM.
  - SET FIXED EXTERNAL (PUBLIC) PROJECT TARGET DATES TO FORCE PRODUCT/PROJECT CLOSURE.

Robin

DESIGN VERIFY/TEST PROCESS

- o DEFINE/EXPLAIN THE DVT/DMT/PMT SO THAT EVERYBODY KNOWS WHAT IS GOING ON, WHAT TO EXPECT, AND WHEN

- o TREAT DESIGN TESTING AS AN INDEPENDENT "DO" PROCESS (NOT AN OVERHEAD FUNCTION)
  - PLAN IT RIGHT/DESIGN IN PARALLISM
  - PROVIDE ENOUGH MONEY/PEOPLE TO DO THE JOB
  - MAINTAIN A HIGH VISIBILITY ON WHERE WE ARE - WHAT'S NEXT - WHEN
  - APPLY SERIOUS MANAGEMENT TECHNIQUES TO IT

- o HAVE A TEST SPEC - TEST ONLY TO IT, NOT BEYOND IT

- o PUSH PROBLEMS TOWARD BEGINNING WHERE THEY ARE CHEAP TO FIX
  - FOCUS ON DVT (HARDWARE/FIRMWARE/SOFTWARE)

- o ONLY ENTER DMT/PMT WHEN YOU ARE 90% CERTAIN OF PASSING

- o PROVIDE A CLEAR "RECOVERY" PROCESS TO CORRECT PROBLEMS THAT ARE DISCOVERED

- o UNDERSTAND HOW THE MACHINE WORKS - UNDERSTAND WHAT IS OK - WHAT STILL NEEDS TO BE TESTED

Robin

DESIGN SERVICES/PROTOTYPE BUILD PROCESS

- o Start with a breadboard
- o MAKE MISTAKES ON PAPER - NOT IN HARDWARE
  - USE SIMULATION TOOLS - HARDWARE/FIRMWARE
  - USE DESIGN REVIEWS → Design Walk-through
  - ASSURE PRODUCIBILITY
  - AVOID RE-LAYOUT CYCLES
- o ALLOW SPACE IN THE DESIGN FOR FLEXIBILITY - DON'T UNNECESSARILY PACK TOO MUCH ON ONE BOARD/IN ONE ROM
- o KEEP DOCUMENTATION CLEAN AND UP-TO-DATE
- o SUBMIT "CLEAN/COMPLETE" DESIGNS TO P.C. LAYOUT
  - USE DESIGN CHANGE CUT-OFF DATES
  - STAY AWAY
- o GET THE SERVICE GROUPS ON THE NEW PRODUCTS TEAM
- o CONTINUE THE LITTLETON TURNAROUND IMPROVEMENTS
- o ANTICIPATE TECHNOLOGICAL CHANGE WITH NEW CAD TOOLS

MANUFACTURING

- HAVE A STRONG CENTRAL TERMINALS NEW PRODUCT GROUP TO SERVE AS THE MKT/ENG/C.S. INTERFACE FOR THE PLANTS
  - GET MISSIONS/ROLES/RESPONSIBILITIES CLEAR
  - WHO'S DRIVER/OWNER AND WHO'S SUPPORT, WHEN
- BE RESPONSIVE - USE SENIOR MANUFACTURING PEOPLE THE PLANTS TRUST TO ANSWER QUESTIONS/MAKE DECISIONS QUICKLY

BEHAVIORALLY, THE TEAM MUST:

- DO IT RIGHT THE FIRST TIME;

  Quality means absence of errors!

* - EXECUTE THE PROJECT IN A TIMELY FASHION;

  - LIMIT PROJECTS TO LESS THAN TWO YEARS BY A SMALL TEAM.

  - NOT PREDICATE A PROJECT ON SCHEDULING INVENTIONS IN THE DESIGN, PROCESS AND CAD AREAS.

    Stay in A/D until a project can be scheduled.

\# - HAVE A WRITTEN DESIGN METHODOLOGY;

  - BE OPEN AND HAVE EXTERNAL REVIEWS, AND CLEARLY WRITTEN PRODUCT DESCRIPTIONS FOR INSPECTION;

  - START SMALL, BE REVIEWED AND GROW ON ITS DEMONSTRATED SUCCESS;

  - LEARN, IN ORDER TO HANDLE THE INCREASE IN COMPLEXITY

    || How many courses have you taken or taught?

* Venus Example ⇒ > 6 years

* Robin Example ⇒ ≈ 6 months.

COHEN'S ELEMENTS OF SOFTWARE QUALITY

PACKAGING

INSTALLABILITY

EASE OF USE

RELIABILITY

PERFORMANCE

FEATURES

SERVICE TO USERS

MAINTAINABILITY

MAINTAINENCE

COMPATIBILITY

EVOLVABILITY

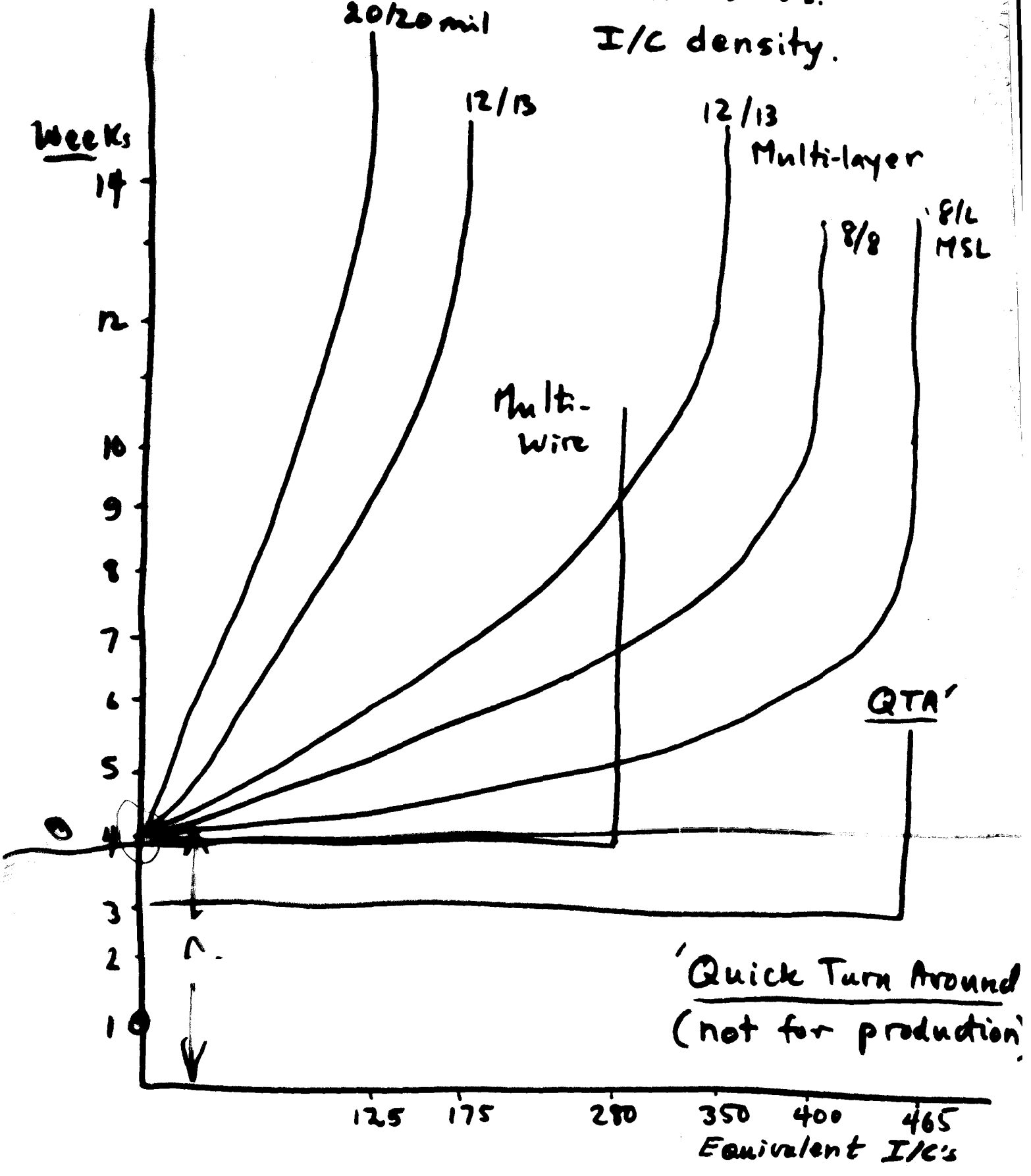
TIMELINESS

... ALL OF THE ABOVE

PRODUCT METRICS KNOWLEDGE INCLUDES:

- PRODUCTS FOR WHICH THERE'LL BE NO COMPETITOR;
- ALL PRODUCT COST METRICS;
- ALL PRODUCT PERFORMANCE AND COST/PERFORMANCE METRICS;
- REASONS WHY THE PRODUCT WILL SUCCEED;
- MAJOR COMPETITOR PRODUCTS BY COST, PERFORMANCE AND FUNCTIONALITY;
- LEADING EDGE, INNOVATIVE, SMALL COMPANY PRODUCTS;
- PRODUCTIVITY, QUALITY AND DESIGN PROCESS METRICS FOR PROJECTS

Design Process Metrics



Gordon Bell
April, 1974

WHY DO WE NEED HARDWARE DESCRIPTION LANGUAGES?

In writing the book, COMPUTER STRUCTURES, Allen Newell, and I used 2 notations to describe and analyze computers, PMS, a 2-dimensional representation, is for the block diagram, physical structure (processors, memories, switches, terminals, links), with extensions for lower level structures such as logical diagrams. ISP (for Instruction Set Processor) describes the instruction set precisely.

The notations have been used in several other ways;

0. The ISP descriptions in the above book, have been hand translated to programming languages for simulation.

1. Michael Knudsen built a program PMS for use in computer structures design; the system computes reliability and performance parameters. Extensions will compare machines and test valid computer configurations.

2. Mario Barbacci built a programm which accepts ISP and carries out various design activities for a specific set of register transfer level modules.

3. ISP has been extended for register transfer systems (hardwired and microprogrammed control structures), design although its need is unclear.

4. ISP was used to describe the DEC PDP-11 in its design phase, and in the programming manual. Since this description is supplementary to the conventional text description, users of the manual have not damned the description, nor are we overrun with letters of praise. Through lack of support, descriptions of future DEC computers will probably be more conventional--with no formal descriptions--simply to save trees and cost.

5. A set of Register Transfer Modules, called RTM's (PDP 16), were built by DEC. PMS was used for describing structure, while a flowchart form of ISP was used for control. Here we needed and use description languages, including software for processing the designs (including simulation).

All of the above uses (except 3) stem from need.

I believe there is little need for the conventional 1-dimensional hardware description languages typified by the plethora of

register transfer languages. These seem to come from the need to invent a language and write a simulator. I have seen little actual use, even the texts that posit and promote these language inventions give no real (not toy) machine designs. For logical design, block diagram symbols for the elements (gates, flip-flops, etc.) and the corresponding logic diagrams are better than a 1-dimensional text (eg, Boolean Algebra) or a description language to conceptualize designs. The diagrams are sometimes converted to a 1-dimensional form for logic simulation, but the register transfer language is unsuitable for describing the logic and doing the design. For register transfer descriptions, flowcharts (again 2 dimensions) are usually preferred for showing hardwired and microprogrammed control flow. Again, these flow diagrams are compressed into 1 dimensional text to assemble microprograms into binary words, and occasionally for simulation. When the conversion from flowchart form occurs, it is easy enough to use or modify a conventional assembler; and for simulation, a conventional software register transfer language such as ALGOL, BASIC, FORTRAN, or PL/1 is adequate (and preferred because it's better known and such a program executes substantially faster.

If the 1-dimensional, register transfer language is not for the logical designer, the machine designer, microprogrammer, or system software writer who uses a simulation of a machine, then who is it for? Students, who should know that systems can be represented in various ways? Why can't they use a programming register transfer language (eg, Fortran)? Until graphic displays are more universal, these languages will fall short of the block diagrams and flow charts currently in use.

There is need for machine representation for design and checking aids, automatic compiler, and systems program writers, comparing, designing, and configuring machines; but these have not been in the domain of the typical hardware description language designer.

A NEED FOR HARDWARE DESCRIPTION LANGUAGES?

I believe there is little need for any more conventional hardware description languages typified by the plethora of register transfer languages. These seem to come from the need to invent a language and write a simulator. The problems addressed by these languages have been adequately addressed by existing languages. Also, they are still at too low a level to address the problems that are met in real design. I have seen little actual use, even the texts that posit and promote these language inventions give no real (not toy) machine designs.

Taking the concept of a language in a broader sense, a graphical representation or "graphical language" has proven to be more useful than a conventional programming printed (or text) language. For logical design, block diagram symbols for the elements (gates, flip-flops, etc.) and the corresponding logic diagrams are better than a text (e.g. Boolean Algebra) or a description language to conceptualize designs. Similarly, the flowchart remains the tool of most hardware designers. This has yet to be incorporated in a formal way within hardware description languages.

Finally, conventional software register transfer language such as ALGOL, APL, BASIC, FORTRAN, or PL/1 are generally adequate because they are better known, available, and execute substantially faster. With these languages, a system designer can (at last) think in terms of hardware-software tradeoffs. However, such languges may have to be extended to express concurrency, time delays, and other hardware constructions.

There is also a need for machine representation for design and checking aids, automatic compiler, and systems program writers, comparing, designing, and configuring machines; but these have not been in the domain of the typical hardware description language designer.

There is a need for work leading to better hardware description languages; but until the work is done, there are many languages available to use.

Gordon Bell
October 14, 1974