



- 1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
- 2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
- 3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

REV	ECN	DESCRIPTION OF REVISION	CK APPD
<REV>	<ECN>	<ECO_DESCRIPTION>	<ECODATE>

# J44 MLB-4GB SCHEMATIC

## 08/20/2013

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# ALIASES RESOLVED

Schematic / PCB #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
051-0052	1	SCHEM,MLB-4GB,J44	SCH	CRITICAL	
820-3536	1	PCBF,MLB-4GB,J44	PCB	CRITICAL	

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Apple Inc.		DRAWING NUMBER	SIZE
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		REVISION	
		<E4LABEL>	
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BOM Groups

BOM GROUP	BOM OPTIONS
J44_COMMON	ALTERNATE , COMMON , J44_COMMON1 , J44_COMMON2 , J44_COMMON3 , J44_COMMON4 , J44_PROGPARTS
J44_COMMON1	TBTHV:P15V, SKIP_5V3V3:AUDIBLE, SPI:DUAL_IO
J44_COMMON2	EDP, EDP_LS_CAP, CAMERA_3V3:S0, CAM_WAKE:NO, CAM_XTAL:NO, MEM_ODT:PU, VCORE_FETS
J44_COMMON3	XDP, LPCPLUS, BKLT:PROD, CPUTHRM:ALRT, LOADRC:NO, OTHERRC:NO, DDRRC:NO, TBTRC:NO, BMONRC:NO
J44_PROGPARTS	SMC_PROG:PVT, BOOTROM:PVT, TBTRM:PVT, TPAD_PSOC:PROG
ENGISNS	LOADISNS, OTHERISNS, DDRISNS, TBTISNS, BMONISNS

Programmables (All Builds)

TBT

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
341S3918	1	EPROM,FALCON RIDGE (V13.7) J44	U2890	CRITICAL	TBTROM:PVT

SMC

341S3922	1	IC,SMC-B1,EXT(V2.16F39),PVT,J44	U5000	CRITICAL	SMC_PROG:PVT
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Module Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
337S4596	1	HSWULT,SR18A,PRQ,CO,2.4,28W,2+3,3M,BGA	U0500	CRITICAL	CPU_HSW:2.4G
337S4597	1	HSWULT,SR189,PRQ,CO,2.6,28W,2+3,3M,BGA	U0500	CRITICAL	CPU_HSW:2.6G
337S4598	1	HSWULT,SR188,PRQ,CO,2.8,28W,2+3,4M,BGA	U0500	CRITICAL	CPU_HSW:2.8G
338S1247	1	IC,TBT,FR-4C,A0,PRQ,CIO,SR1JC,FCBGA288	U2800	CRITICAL	
338S1186	1	IC,BCML5700A2,S2 PCIE CAMERA PROCESSOR	U3900	CRITICAL	
376S1194	2	MOSFET,N-CH,30V,15.3A,12M,8P 3.3X3.3 DFN	Q7310,Q7320	CRITICAL	VCORE_FET:VSHY
376S1193	2	MOSFET,N-CH,30V,22A,6.0M,8P 3.3X3.3 DFN	Q7311,Q7321	CRITICAL	VCORE_FET:VSHY
376S0964	2	MOSFET,N-CH,25V,30A,9.6M,8P 3.3X3.3 DFN	Q7310,Q7320	CRITICAL	VCORE_FET:REN
376S1104	2	MOSFET,N-CH,25V,30A,6.1M,8P 3.3X3.3 DFN	Q7311,Q7321	CRITICAL	VCORE_FET:REN

EFI ROM

341S3924	1	IC,EFI ROM (V0116),PVT,J44	U6100	CRITICAL	BOOTROM:PVT
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PSOC

341S3862	1	IC,TRKPD/KYBD PSOC,CU ONLY(V224) J44	U4801	CRITICAL	TPAD_PSOC:PROG
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Alternate Parts

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
376S1053	376S0604		ALL	Diodes alt to Fairchild
128S0311	128S0329		ALL	NEC alt to Sanyo
138S0739	138S0706		ALL	Samsung alt to Murata
197S0481	197S0480		ALL	Epson alt to NDK
152S0461	152S1645		ALL	Cyntec alt to Vishay
376S1080	376S0820		ALL	Diodes alt to On Semi
155S0667	155S0583		ALL	Panasonic alt to TDK
138S0725	138S0724		ALL	Samsung alt to Murata
376S1032	376S0855		ALL	Toshiba alt for Diodes Dual
376S1129	376S0855		ALL	NXP Alt for Diodes Dual
376S1089	376S1128		ALL	NXP Alt for Diodes Single
353S3452	353S1286		ALL	Maxim alt to Microchip
376S1180	376S0761		ALL	Renesas alt to Vishay
128S0364	128S0264		ALL	Sanyo 2nd Factory alt
107S0254	107S0241		ALL	Cyntec alt to TFT
138S0843	138S0674		ALL	Samsung alt to Murata (BKLT)
138S0803	138S0639		ALL	Samsung alt to Murata (BKLT)
138S0846	138S0811		ALL	Samsung alt to Murata (BKLT)
197S0542	197S0544		ALL	NDK alt to TXC
197S0545	197S0544		ALL	Epson alt to TXC
152S1876	152S1804		ALL	TDK alt to Toko
107S0255	107S0240		ALL	Cyntec alt to TFT
107S0250	107S0248		ALL	Cyntec alt to TFT
127S0164	127S0162		ALL	Rohm alt to Vishay
353S4070	353S4069		ALL	Pericom alt to TI DP Mux U9750
353S4068	353S4069		ALL	NXP alt to TI DP Mux U9750
353S3814	353S3812		ALL	TI alt to NXP
311S0649	311S0541		ALL	ONsemi alt to Toshiba
128S0436	128S0392		ALL	Kemet alt to Sanyo

SYMC MASTER:J44 SYMC DATE:08/20/2013

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**BOM Configuration**

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BOM Variants

BOM NUMBER	BOM NAME	BOM OPTIONS
685-0054	COMMON,MLB-4GB,J44	J44_COMMON
985-0053	DEV,MLB-4GB,J44	XDP_CONN
639-4878	PCBA,MLB-4GB,2.4G,4GB-HYNIX,J44	BASE_BOM,CPU_HSW:2.4G,RAM_4G_HYNIX_H,CAMDRAM:HYNIX_H
639-4879	PCBA,MLB-4GB,2.4G,4GB-ELPIDA,J44	BASE_BOM,CPU_HSW:2.4G,RAM_4G-ELPIDA,CAMDRAM:ELPIDA
639-4880	PCBA,MLB-4GB,2.4G,4GB-MICRON,J44	BASE_BOM,CPU_HSW:2.4G,RAM_4G-MICRON,CAMDRAM:MICRON
639-5272	PCBA,MLB-4GB,2.6G,4GB-HYNIX,J44	BASE_BOM,CPU_HSW:2.6G,RAM_4G_HYNIX_H,CAMDRAM:HYNIX_H
639-5273	PCBA,MLB-4GB,2.6G,4GB-ELPIDA,J44	BASE_BOM,CPU_HSW:2.6G,RAM_4G-ELPIDA,CAMDRAM:ELPIDA
639-5274	PCBA,MLB-4GB,2.6G,4GB-MICRON,J44	BASE_BOM,CPU_HSW:2.6G,RAM_4G-MICRON,CAMDRAM:MICRON
639-5275	PCBA,MLB-4GB,2.8G,4GB-HYNIX,J44	BASE_BOM,CPU_HSW:2.8G,RAM_4G_HYNIX_H,CAMDRAM:HYNIX_H
639-5276	PCBA,MLB-4GB,2.8G,4GB-ELPIDA,J44	BASE_BOM,CPU_HSW:2.8G,RAM_4G-ELPIDA,CAMDRAM:ELPIDA
639-5277	PCBA,MLB-4GB,2.8G,4GB-MICRON,J44	BASE_BOM,CPU_HSW:2.8G,RAM_4G-MICRON,CAMDRAM:MICRON
685-0074	VCORE,FET,VSHY,J44	VCORE_FET:VSHY
685-0075	VCORE,FET,REN,J44	VCORE_FET:REN

DEVELOPMENT/BASE BOM

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
685-0054	1	J44 MLB COMMON BOM	BASE	CRITICAL	BASE_BOM
985-0053	1	J44 MLB DEVEL BOM	DEVEL	CRITICAL	DEVEL_BOM

SUB-BOMS

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
685-0074	1	VCORE,FET,VSHY,J44	VCOREFETS	CRITICAL	VCORE_FETS

Alternate Parts

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
685-0075	685-0074		ALL	RENDSAS ALT TO VSHY

DRAM PARTS

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
333S0704	8	1C,SDRAM,4GBIT,256MX16,DDR3-1600,P,DIE,96FBGA	U4000	CRITICAL	4G-ELPIDA
333S0700	8	1C,SDRAM,4GBIT,256MX16,DDR3-1600,HUMA,96FBGA	U4000	CRITICAL	4G_HYNIX_H
333S0698	8	1C,SDRAM,4GBIT,256MX16,DDR3-1600,REV E,96FBGA	U4000	CRITICAL	4G-MICRON
333S0715	8	1C,SDRAM,4GBIT,256MX16,DDR3-1866,P,DIE,96FBGA	U4000	CRITICAL	4G-ELPIDA_1866
333S0717	8	1C,SDRAM,4GBIT,256MX16,DDR3-1866,HUMA,96FBGA	U4000	CRITICAL	4G_HYNIX_H_1866
333S0720	8	1C,SDRAM,4GBIT,256MX16,DDR3-1866,REV E,96FBGA	U4000	CRITICAL	4G-MICRON_1866

DRAM SPD Straps

BOM GROUP	BOM OPTIONS
RAM_4G-ELPIDA	4G-ELPIDA, RAMCFG3:L, RAMCFG2:L, RAMCFG1:L, RAMCFG0:L, PPDDR:1V35
RAM_4G-HYNIX_H	4G-HYNIX_H, RAMCFG3:L, RAMCFG2:L, RAMCFG1:L, RAMCFG0:H, PPDDR:1V35
RAM_4G-MICRON	4G-MICRON, RAMCFG3:L, RAMCFG2:L, RAMCFG1:H, RAMCFG0:L, PPDDR:1V35
RAM_4G-ELPIDA_1866	4G-ELPIDA_1866, RAMCFG3:L, RAMCFG2:L, RAMCFG1:L, RAMCFG0:L, PPDDR:1V5
RAM_4G-HYNIX_H_1866	4G-HYNIX_H_1866, RAMCFG3:L, RAMCFG2:L, RAMCFG1:L, RAMCFG0:H, PPDDR:1V5
RAM_4G-MICRON_1866	4G-MICRON_1866, RAMCFG3:L, RAMCFG2:L, RAMCFG1:H, RAMCFG0:L, PPDDR:1V5

NOTE: 1866 PARTS BEING STRAPPED TO RUN AT 1600

13" MBP VARIABLE BOM GROUPS

BOM GROUP	BOM OPTIONS
J44_COMMON4	SMCBOARDID:8

DRAM SPD Straps

BOM GROUP	BOM OPTIONS
CAMDRAM:HYNIX_H	CAMDRAM_TYPE:HYNIX_H
CAMDRAM:ELPIDA	CAMDRAM_TYPE:ELPIDA
CAMDRAM:MICRON	CAMDRAM_TYPE:MICRON

DRAM Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
333S0700	1	1C,SDRAM,4GBIT,DDR3L-1600,HUMA,96B FBGA	U4000	CRITICAL	CAMDRAM_TYPE:HYNIX_H
333S0704	1	1C,SDRAM,4GBIT,DDR3L-1600,DIE P,96B FBGA	U4000	CRITICAL	CAMDRAM_TYPE:ELPIDA
333S0698	1	1C,SDRAM,4GBIT,DDR3L-1600,REV E,96B FBGA	U4000	CRITICAL	CAMDRAM_TYPE:MICRON

SYNC MASTER=J44 SYNC DATE=01/03/2013

**BOM Configuration**

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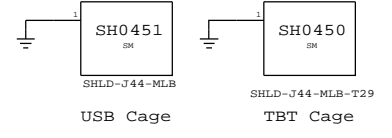
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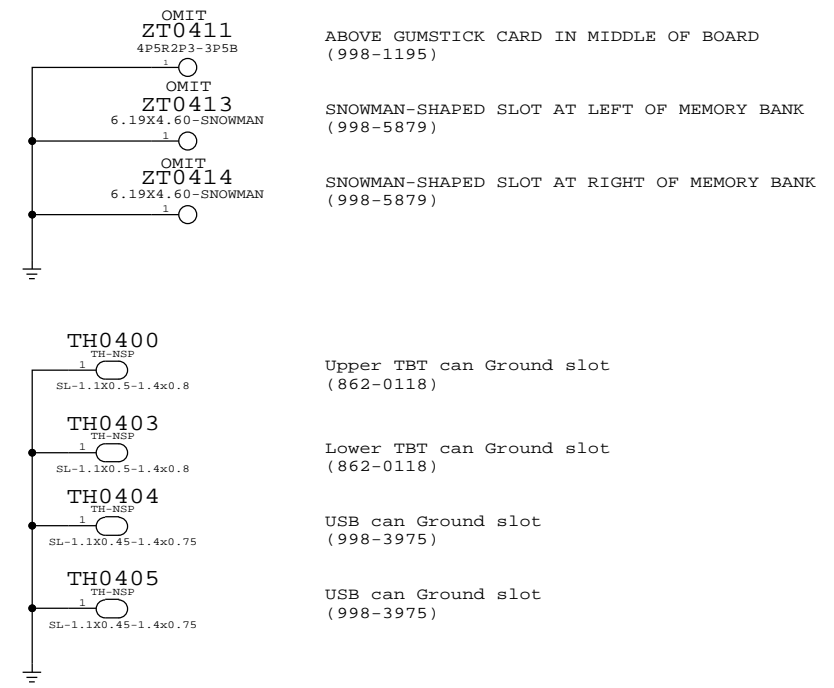


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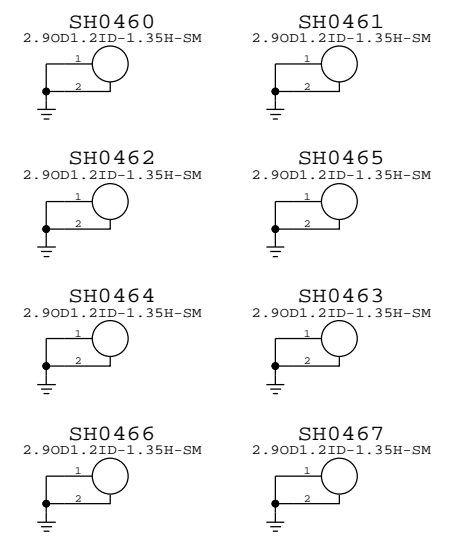
### Shield Cans



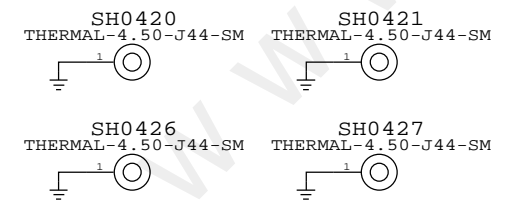
### Mounting Holes & Slots



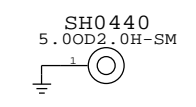
### Rubber Mount Standoffs (860-1448)



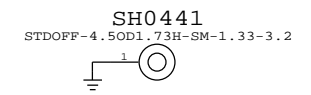
### THERMAL MODULE STANDOFF (860-1645)



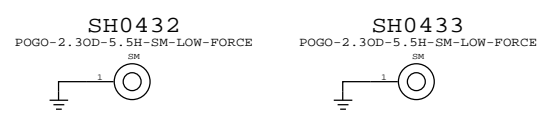
### SSD STANDOFF (806-5375)



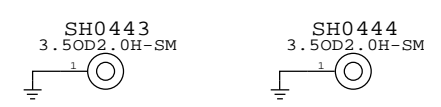
### FAN STANDOFF (806-5376)



### POGO PINS (870-2451)



### RIO FLEX BRACKET BOSSES (860-2354)

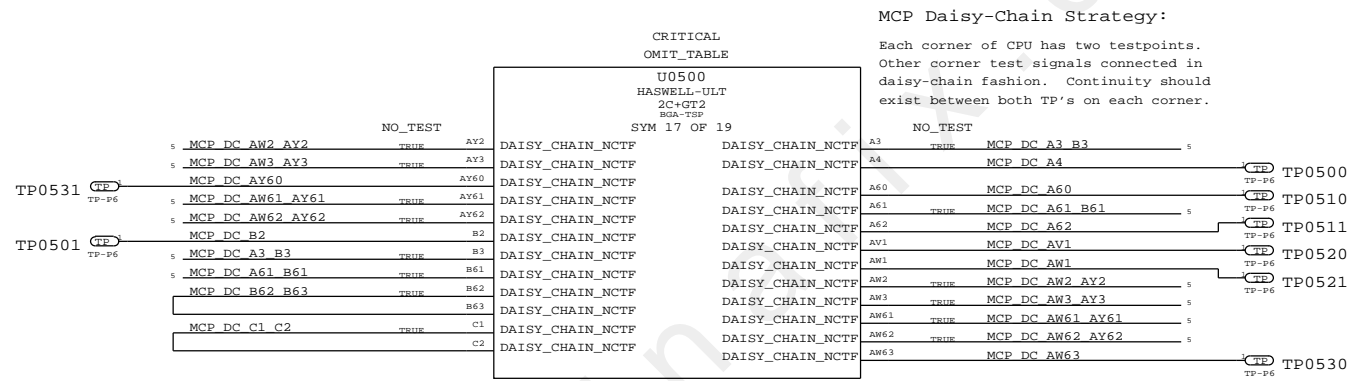
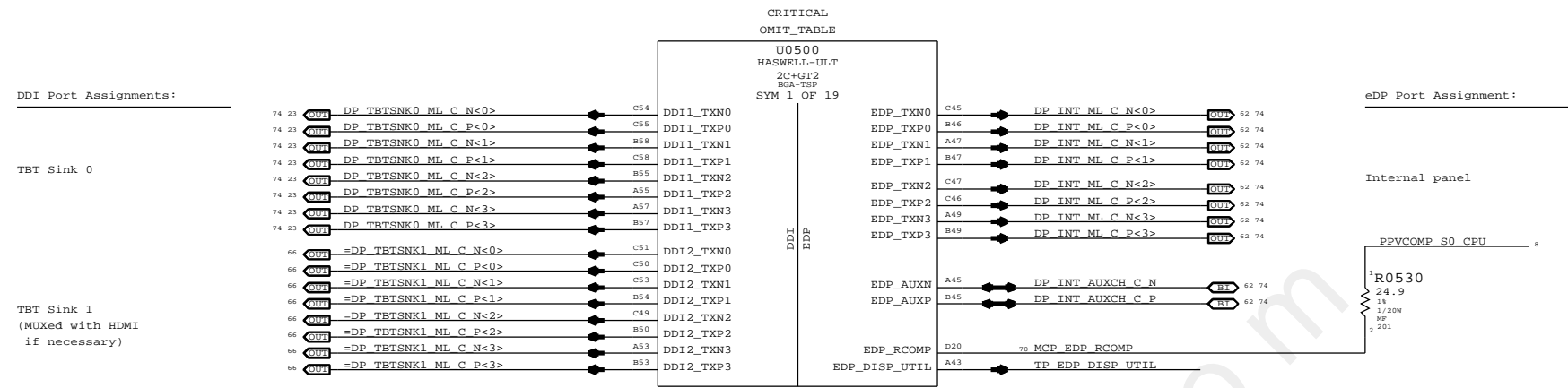


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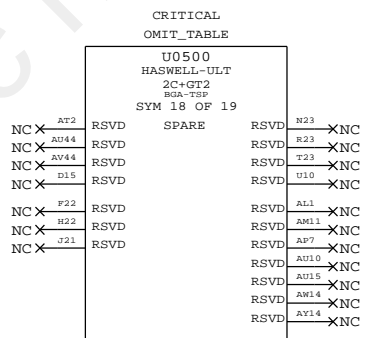
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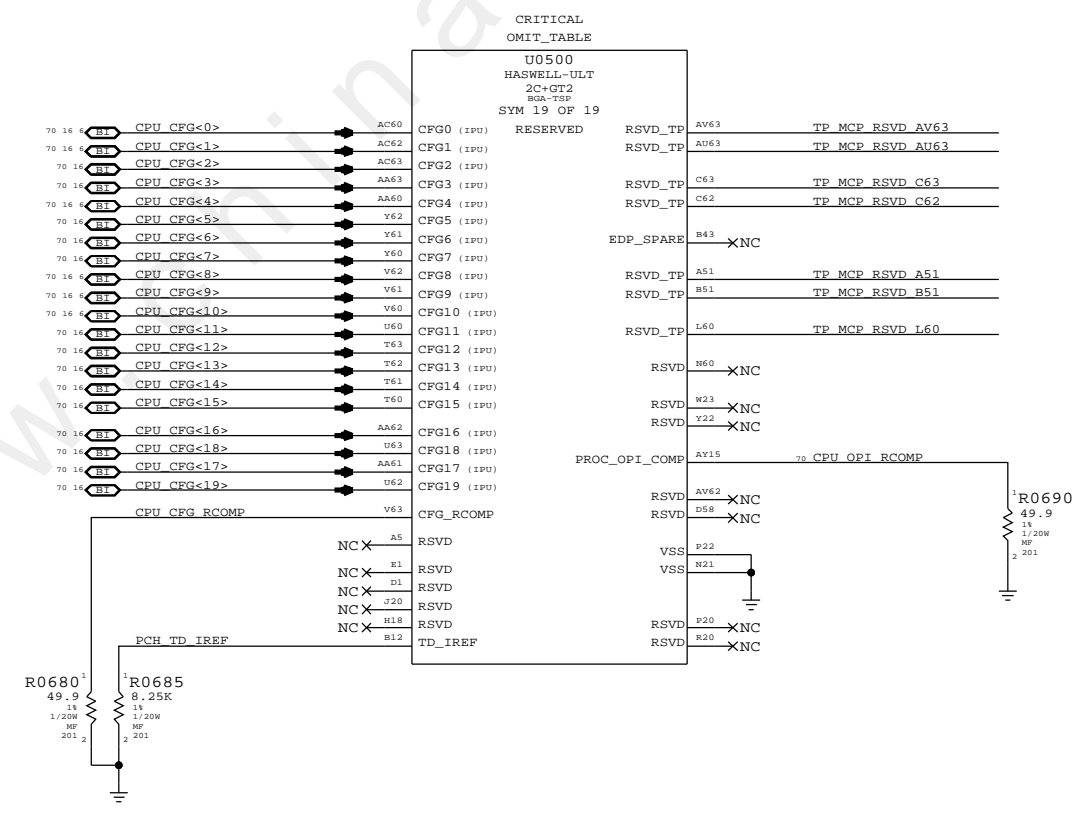
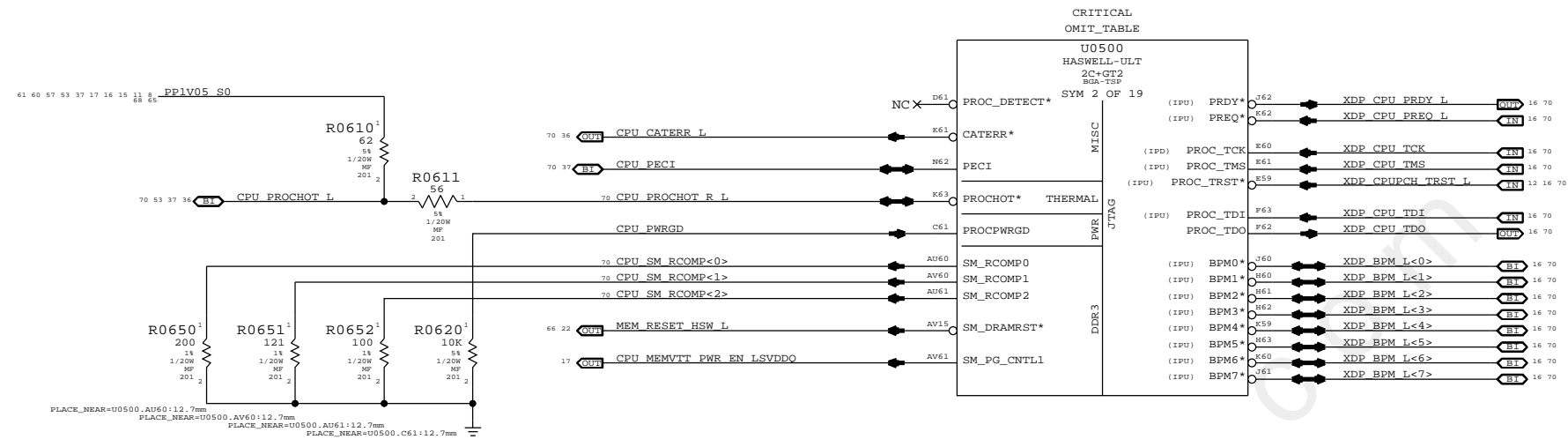


MCP Daisy-Chain Strategy:

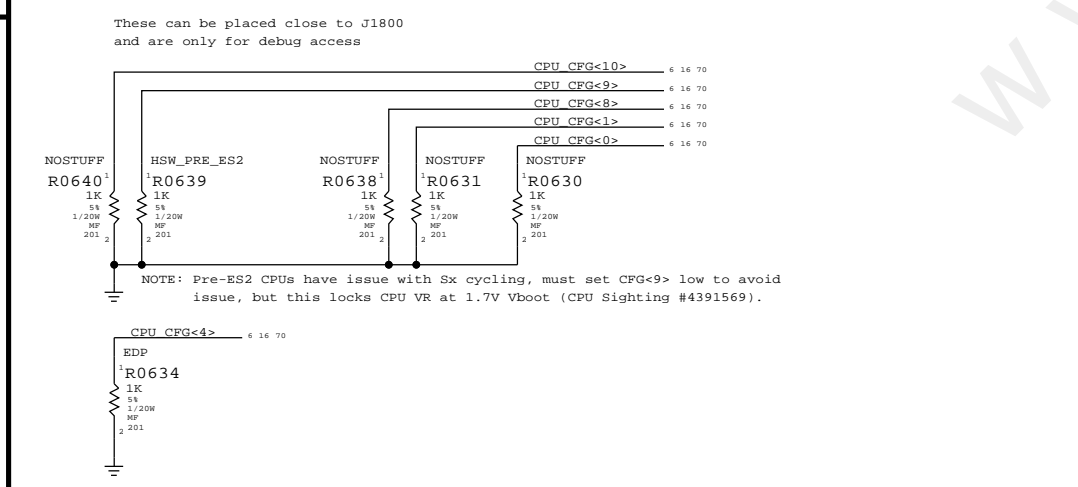
Each corner of CPU has two testpoints. Other corner test signals connected in daisy-chain fashion. Continuity should exist between both TP's on each corner.



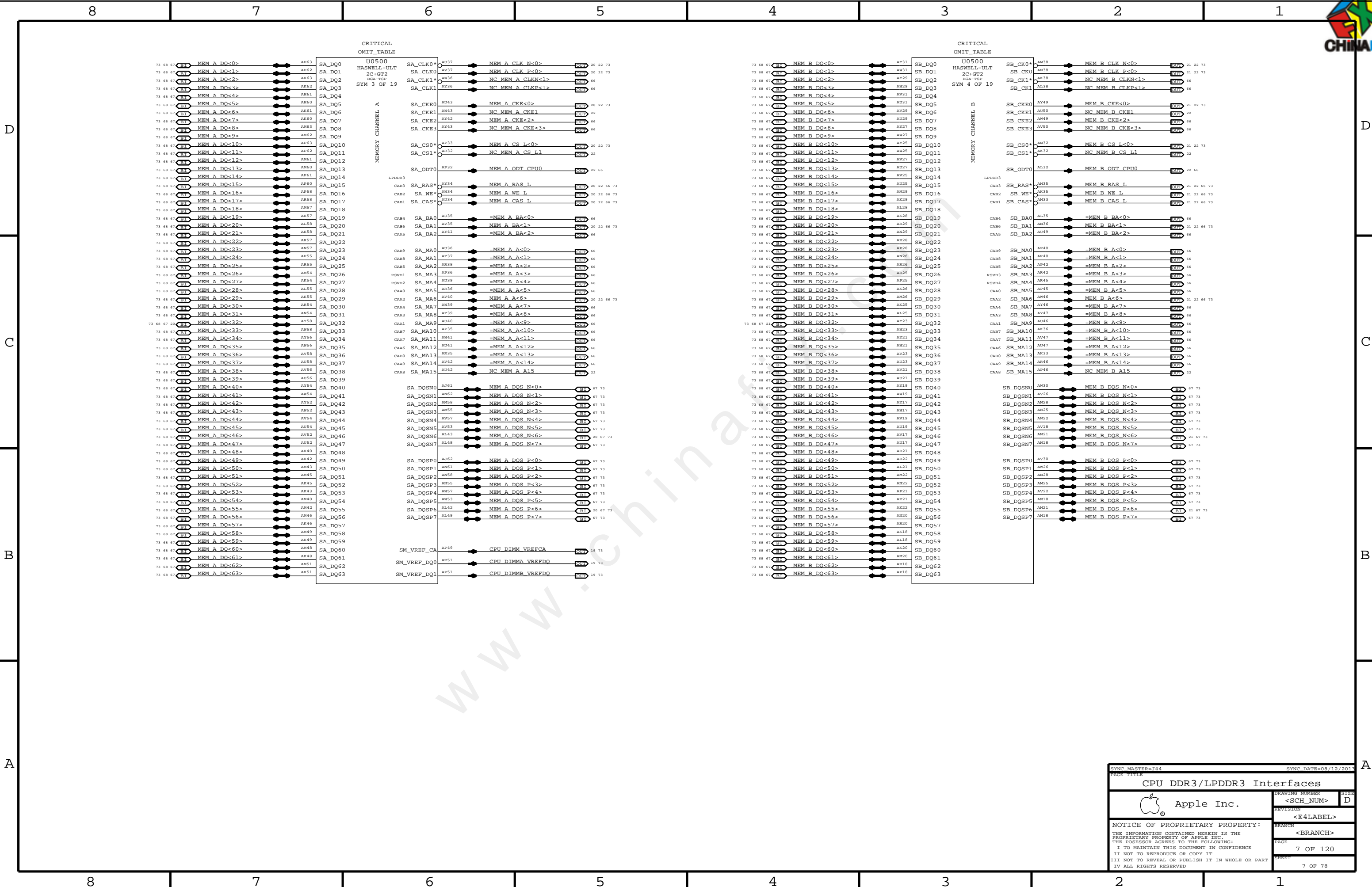
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CFG<10>:SAFE MODE BOOT 1 = NORMAL OPERATION 0 = POWER FEATURES NOT ACTIVE  
 CFG<9> :NO SVID-CAPABLE VR 1 = VR SUPPORTS SVID 0 = VR DOES NOT SUPPORT SVID  
 CFG<8> :ALLOW NOA ON LOCKED UNITS 1 = NORMAL OPERATION 0 = NOA ALWAYS UNLOCKED  
 CFG<4> :EDP ENABLE/DISABLE 1 = DISABLED 0 = ENABLED  
 CFG<1> :PCH-LESS MODE 1 = NORMAL OPERATION 0 = PCH-LESS MODE  
 CFG<0> :RESET SEQUENCE STALL 1 = NORMAL OPERATION 0 = STALL AFTER PCU PLL LOCK



SYNC MASTER=144		SYNC DATE=08/12/2013	
PAGE TITLE			
<b>CPU Misc/JTAG/CFG/RSVD</b>			
Apple Inc.		DRAWING NUMBER	SIZE
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		BRANCH	<E4LABEL>
		PAGE	<BRANCH>
		SHEET	6 OF 120
			6 OF 78



CRITICAL OMIT\_TABLE

CRITICAL OMIT\_TABLE

U0500  
HASWELL-ULT  
2C+GT2  
BGA-TSFP  
SYM 3 OF 19

U0500  
HASWELL-ULT  
2C+GT2  
BGA-TSFP  
SYM 4 OF 19

MEMORY CHANNEL A

MEMORY CHANNEL B

LPDDR3

LPDDR3

SYNC MASTER=144		SYNC DATE=08/12/2013	
PAGE TITLE			
CPU DDR3/LPDDR3 Interfaces			
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7 OF 120		7 OF 78	

HSW-ULT current estimates from Haswell Mobile ULT Processor EDS vol 1, doc #502406, v0.9.  
 LPT-LP current estimates from Lynx Point-LP PCH EDS, doc #503118, v1.0.  
 Note [1] current numbers from clarification email, from Srini, dated 9/10/2012 2:11pm.

D

D

C

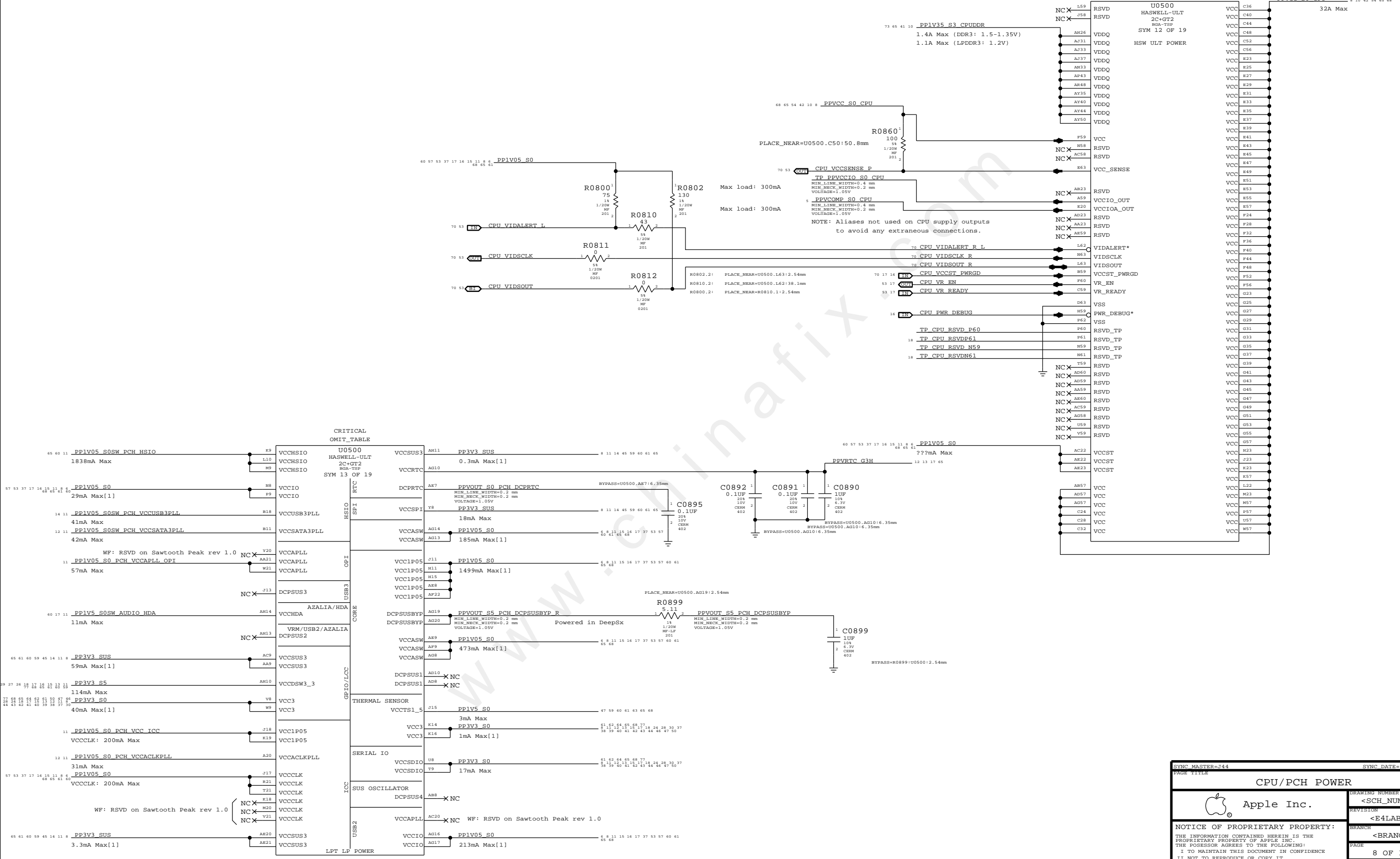
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B

B

A

A

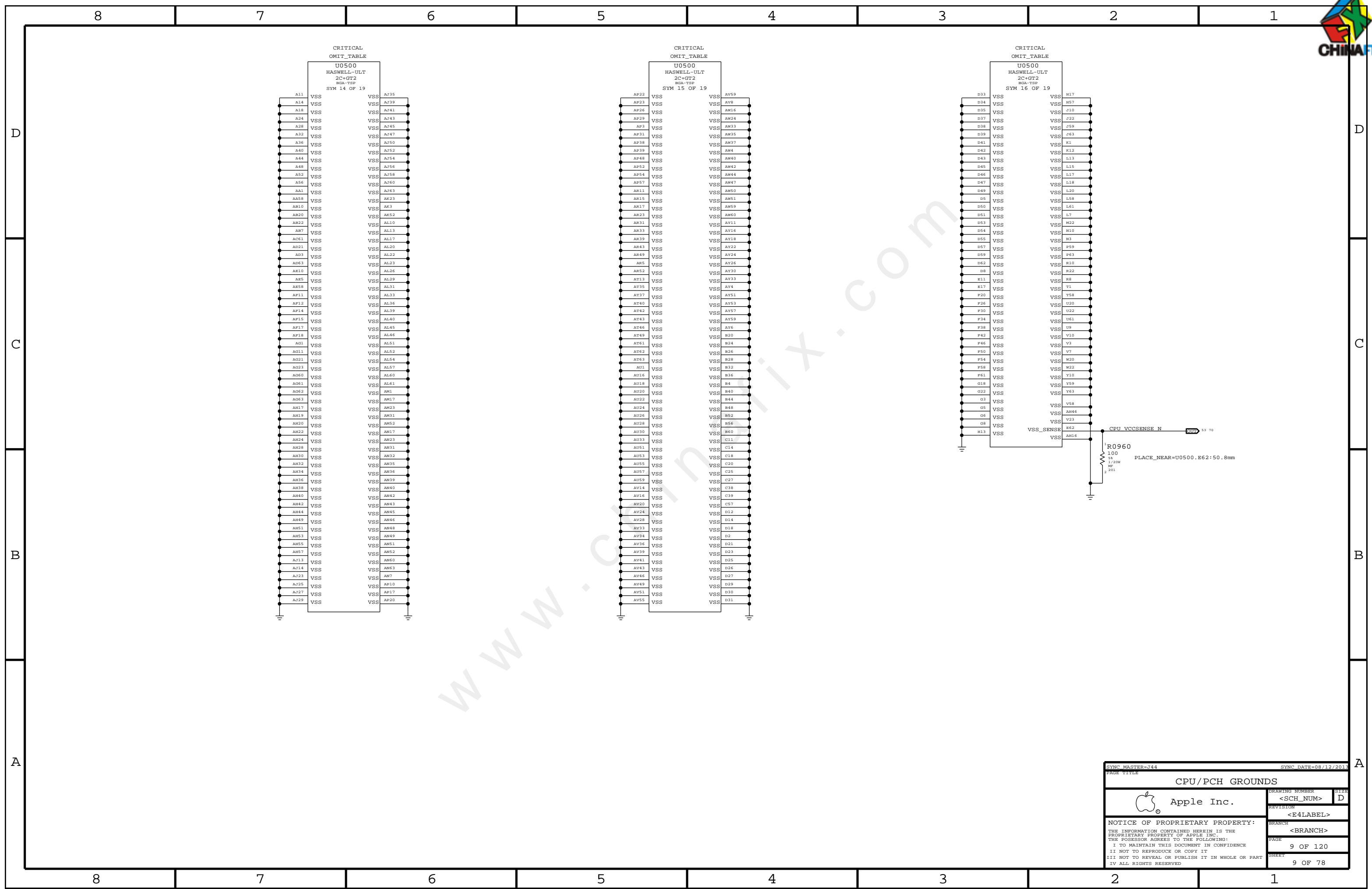


CRITICAL OMIT_TABLE		PPVCC S0 CPU	
U0500	HASWELL-ULT	VCC36	32A Max
2C+GT2	2C+GT2	VCC40	
BGA-TSP	BGA-TSP	VCC44	
SYM 12 OF 19	HSW ULT POWER	VCC48	
		VCC52	
		VCC56	
		VCC60	
		VCC64	
		VCC68	
		VCC72	
		VCC76	
		VCC80	
		VCC84	
		VCC88	
		VCC92	
		VCC96	
		VCC100	
		VCC104	
		VCC108	
		VCC112	
		VCC116	
		VCC120	
		VCC124	
		VCC128	
		VCC132	
		VCC136	
		VCC140	
		VCC144	
		VCC148	
		VCC152	
		VCC156	
		VCC160	
		VCC164	
		VCC168	
		VCC172	
		VCC176	
		VCC180	
		VCC184	
		VCC188	
		VCC192	
		VCC196	
		VCC200	
		VCC204	
		VCC208	
		VCC212	
		VCC216	
		VCC220	
		VCC224	
		VCC228	
		VCC232	
		VCC236	
		VCC240	
		VCC244	
		VCC248	
		VCC252	
		VCC256	
		VCC260	
		VCC264	
		VCC268	
		VCC272	
		VCC276	
		VCC280	
		VCC284	
		VCC288	
		VCC292	
		VCC296	
		VCC300	
		VCC304	
		VCC308	
		VCC312	
		VCC316	
		VCC320	
		VCC324	
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		VCC332	
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		VCC340	
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		VCC396	
		VCC400	
		VCC404	
		VCC408	
		VCC412	
		VCC416	
		VCC420	
		VCC424	
		VCC428	
		VCC432	
		VCC436	
		VCC440	
		VCC444	
		VCC448	
		VCC452	
		VCC456	
		VCC460	
		VCC464	
		VCC468	
		VCC472	
		VCC476	
		VCC480	
		VCC484	
		VCC488	
		VCC492	
		VCC496	
		VCC500	

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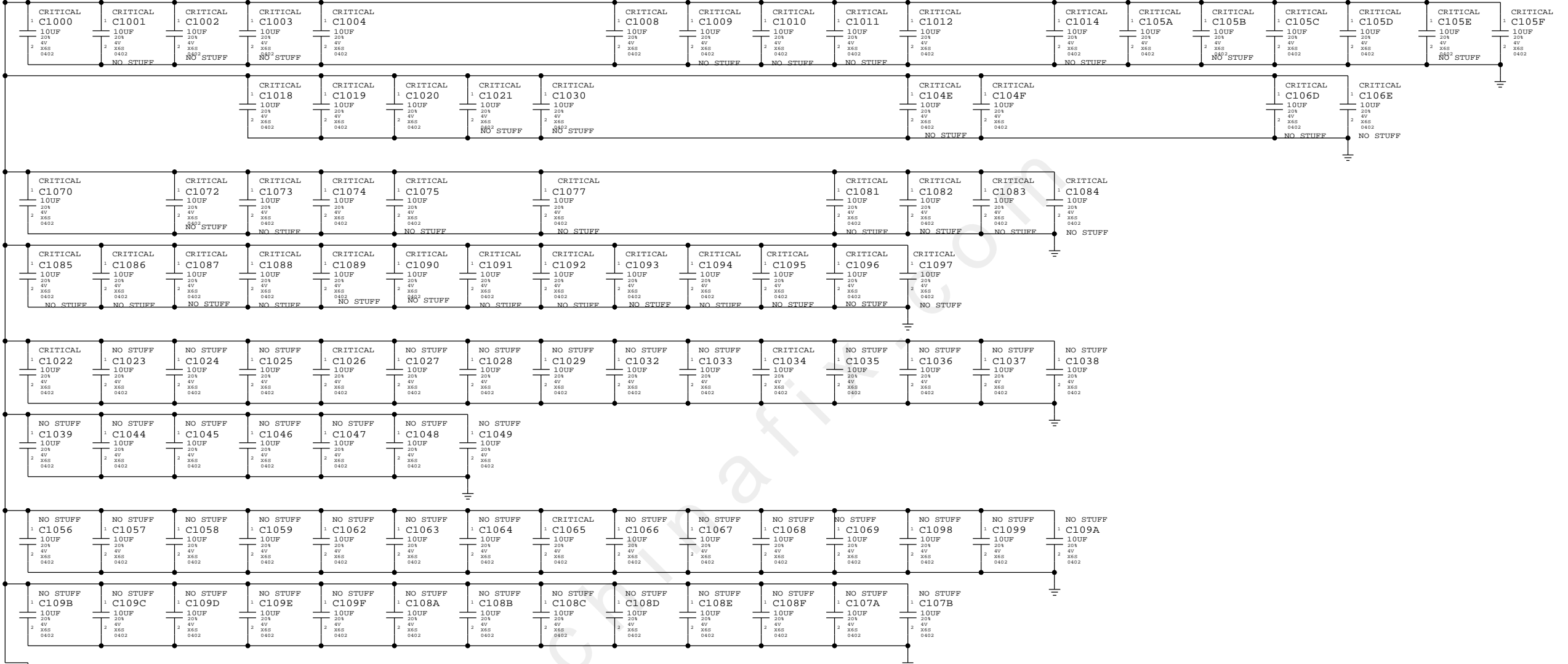
8 7 6 5 4 3 2 1

All Intel recommendations from Intel doc #603160 Shark Bay Ultrabook Platform Power Delivery Design Guide Rev 0.9 unless stated otherwise

### CPU VCC Decoupling

Intel recommendation (Table 5-1): 23x 22uF 0805 stuff, 7x 22uF 0805 nostuff  
Apple implementation : 18x 22uF 0603 stuff, 80x 22uF 0603 nostuff

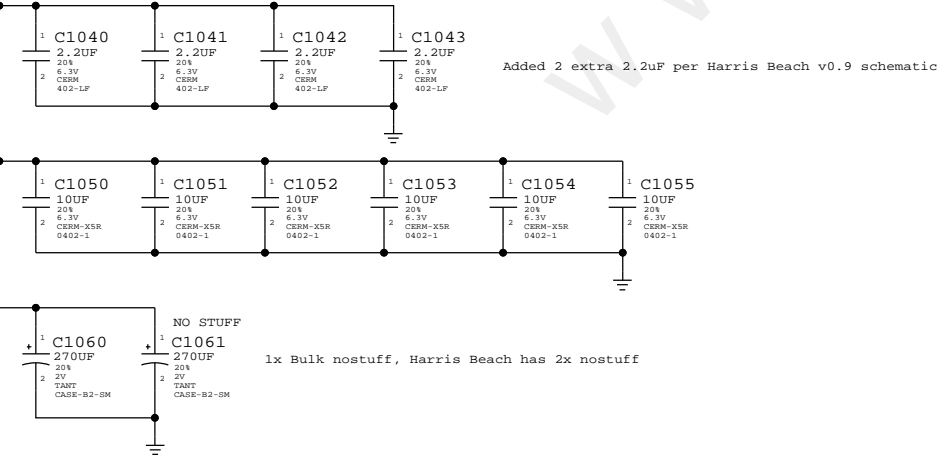
68 65 54 42 8\_PPVCC\_S0\_CPU



### CPU VDDQ DECOUPLING

Intel recommendation (Table 5-4): 2x 2.2uF 0402, 6x 10uF 0603  
Apple implementation : 2x 2.2uF 0402, 6x 10uF 0402

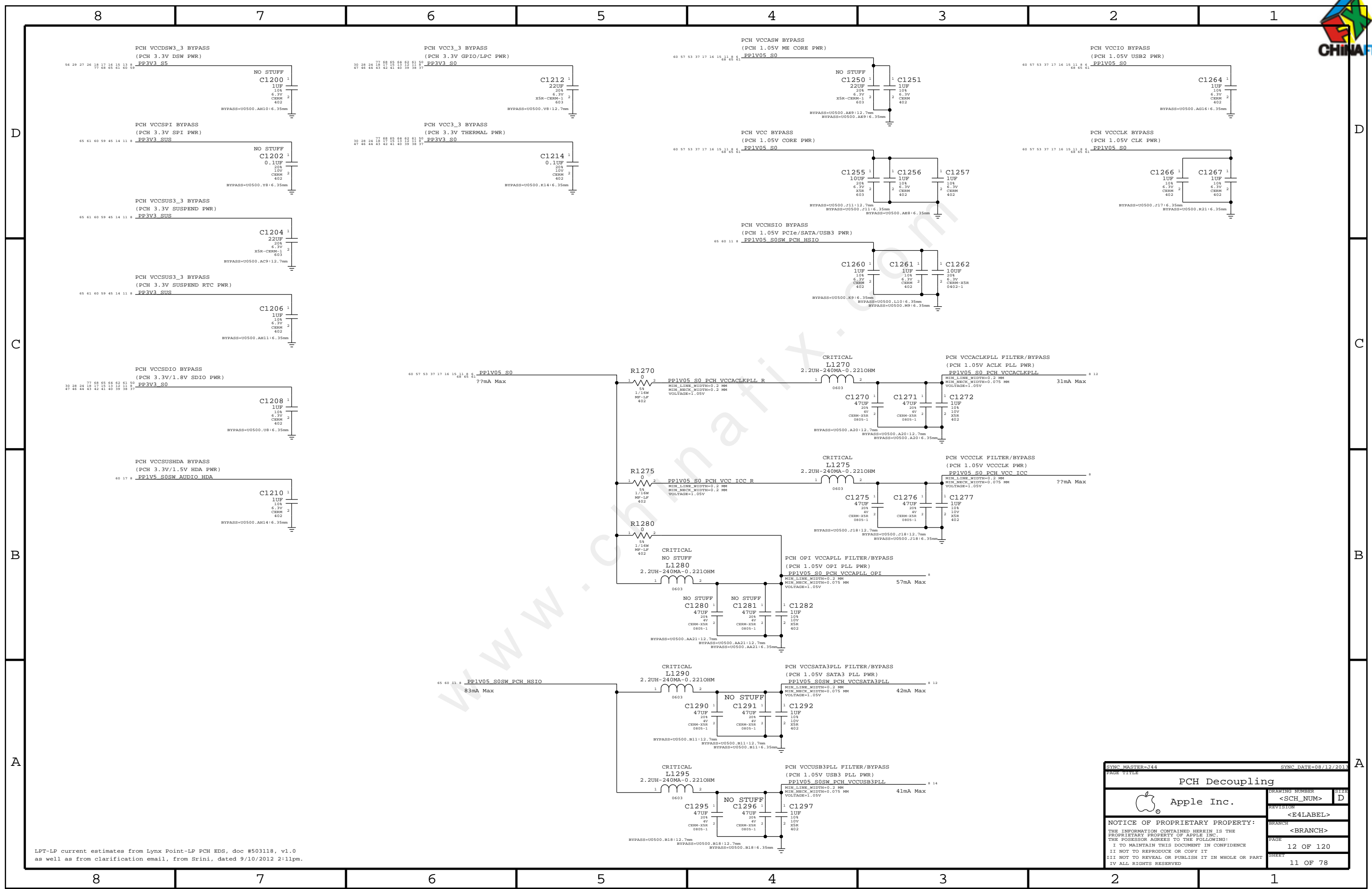
73 65 41 8\_PP1V35\_S3\_CPUDDR



## CPU VCC Decoupling

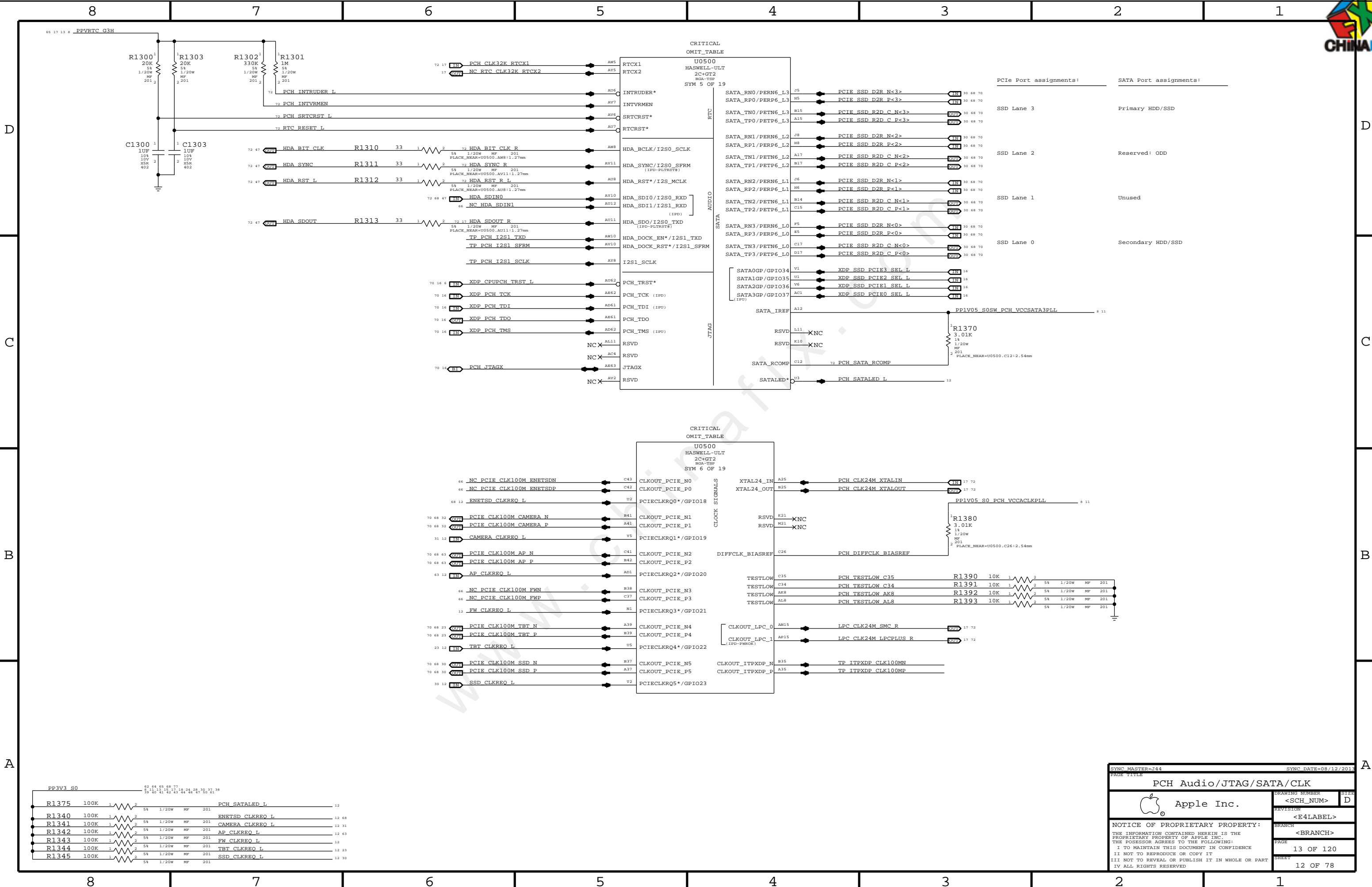
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CPU Decoupling			
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8 7 6 5 4 3 2 1

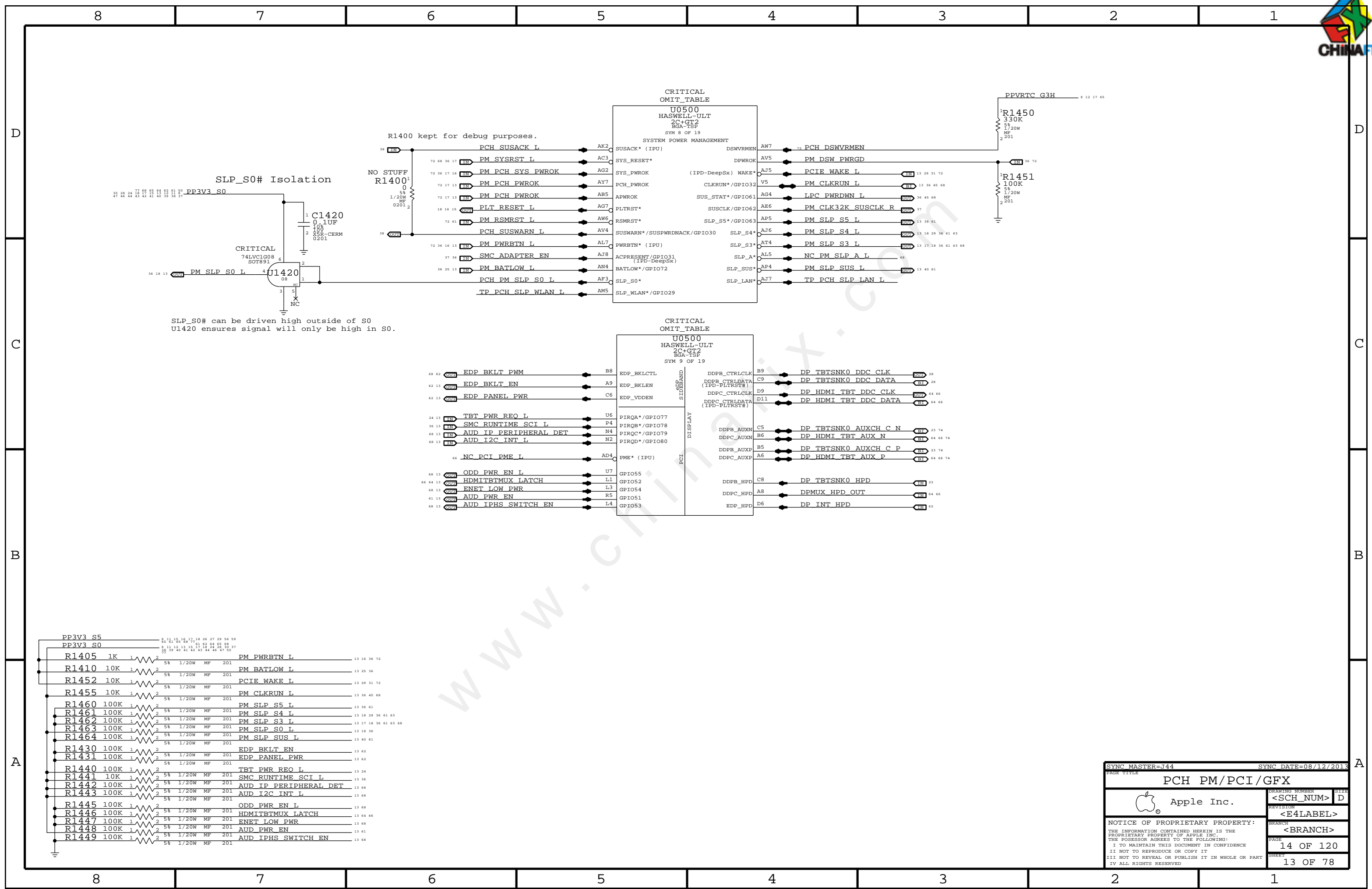


LPT-LP current estimates from Lynx Point-LP PCH EDS, doc #503118, v1.0 as well as from clarification email, from Srini, dated 9/10/2012 2:11pm.

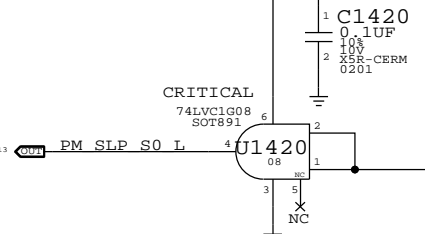
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PAGE TITLE			
PCH Audio/JTAG/SATA/CLK			
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**SLP\_S0# Isolation**



SLP\_S0# can be driven high outside of S0  
U1420 ensures signal will only be high in S0.

**CRITICAL OMIT\_TABLE**

U0500 HASWELL-ULT  
2C+GT2 BGA-TSP  
SYM 8 OF 19

SYSTEM POWER MANAGEMENT

AK2	SUSACK* (IPU)	DSWVRMEN	AW7	PCH_DSWVRMEN
AC3	SYS_RESET*	DPWRK	AV5	PM_DSW_PWRGD
AG2	SYS_PWROK (IPD-DeepSx) WAKE*		AJ5	PCIE_WAKE_L
AY7	PCH_PWROK	CLKRUN*/GPIO32	V5	PM_CLKRUN_L
AB5	APWRK	SUS_STAT*/GPIO61	AG4	LPC_PWRDWN_L
AG7	PLTRST*	SUSCLK*/GPIO62	AE6	PM_CLK32K_SUSCLK_R
AW6	RSMRST*	SLP_S5*/GPIO63	AP5	PM_SLP_S5_L
AV4	SUSWRN*/SUSPWRDNACK*/GPIO30	SLP_S4*	AJ6	PM_SLP_S4_L
AL7	PWRBTN* (IPU)	SLP_S3*	AT4	PM_SLP_S3_L
AJ8	ACPRESENT*/GPIO31 (IPD-DeepSx)	SLP_A*	AL5	NC_PM_SLP_A_L
AN4	BATLOW*/GPIO72	SLP_SUS*	AP4	PM_SLP_SUS_L
AF2	SLP_S0*	SLP_LAN*	AJ7	TP_PCH_SLP_LAN_L
AM5	SLP_WLAN*/GPIO29			

**CRITICAL OMIT\_TABLE**

U0500 HASWELL-ULT  
2C+GT2 BGA-TSP  
SYM 9 OF 19

B8	EDP_BKLT_PWM	EDP_BKLTCTL	B9	DP_TBTSNK0_DDC_CLK	28
A9	EDP_BKLT_EN	EDP_BKLEN	C9	DP_TBTSNK0_DDC_DATA	28
C6	EDP_PANEL_PWR	EDP_VDDEN	D9	DP_HDMI_TBT_DDC_CLK	64 66
U6	TBT_PWR_REQ_L	PIRQA*/GPIO77	D11	DP_HDMI_TBT_DDC_DATA	64 66
P4	SMC_RUNTIME_SCI_L	PIRQB*/GPIO78	C5	DP_TBTSNK0_AUXCH_C_N	23 74
N4	AUD_IP_PERIPHERAL_DET	PIRQC*/GPIO79	B6	DP_HDMI_TBT_AUX_N	64 66 74
N2	AUD_I2C_INT_L	PIRQD*/GPIO80	B5	DP_TBTSNK0_AUXCH_C_P	23 74
AD4	NC_PCI_PME_L	PME* (IPU)	A6	DP_HDMI_TBT_AUX_P	64 66 74
U7	ODD_PWR_EN_L	GPIO55	C8	DP_TBTSNK0_HPD	23
L1	HDMITBTMUX_LATCH	GPIO52	A8	DPMUX_HPD_OUT	64 66
L3	ENET_LOW_PWR	GPIO54	D6	DP_INT_HPD	62
R5	AUD_PWR_EN	GPIO51			
L4	AUD_IPHS_SWITCH_EN	GPIO53			

PP3V3 S5	1	5%	1/20W	MF	201	PM_PWRBTN_L	13 16 36 72
PP3V3 S0	1	5%	1/20W	MF	201	PM_BATLOW_L	13 25 36
R1405 1K	1	5%	1/20W	MF	201	PCIE_WAKE_L	13 29 31 72
R1410 10K	1	5%	1/20W	MF	201	PM_CLKRUN_L	13 36 45 68
R1452 10K	1	5%	1/20W	MF	201	PM_SLP_S5_L	13 36 61
R1455 10K	1	5%	1/20W	MF	201	PM_SLP_S4_L	13 18 29 36 61 63
R1460 100K	1	5%	1/20W	MF	201	PM_SLP_S3_L	13 17 18 36 61 63 68
R1461 100K	1	5%	1/20W	MF	201	PM_SLP_S0_L	13 18 36
R1462 100K	1	5%	1/20W	MF	201	PM_SLP_SUS_L	13 40 61
R1463 100K	1	5%	1/20W	MF	201	EDP_BKLT_EN	13 62
R1464 100K	1	5%	1/20W	MF	201	EDP_PANEL_PWR	13 62
R1430 100K	1	5%	1/20W	MF	201	TBT_PWR_REQ_L	13 24
R1440 100K	1	5%	1/20W	MF	201	SMC_RUNTIME_SCI_L	13 36
R1441 10K	1	5%	1/20W	MF	201	AUD_IP_PERIPHERAL_DET	13 68
R1442 100K	1	5%	1/20W	MF	201	AUD_I2C_INT_L	13 68
R1443 100K	1	5%	1/20W	MF	201	ODD_PWR_EN_L	13 68
R1444 100K	1	5%	1/20W	MF	201	HDMITBTMUX_LATCH	13 64 66
R1445 100K	1	5%	1/20W	MF	201	ENET_LOW_PWR	13 68
R1446 100K	1	5%	1/20W	MF	201	AUD_PWR_EN	13 61
R1447 100K	1	5%	1/20W	MF	201	AUD_IPHS_SWITCH_EN	13 61
R1448 100K	1	5%	1/20W	MF	201		
R1449 100K	1	5%	1/20W	MF	201		

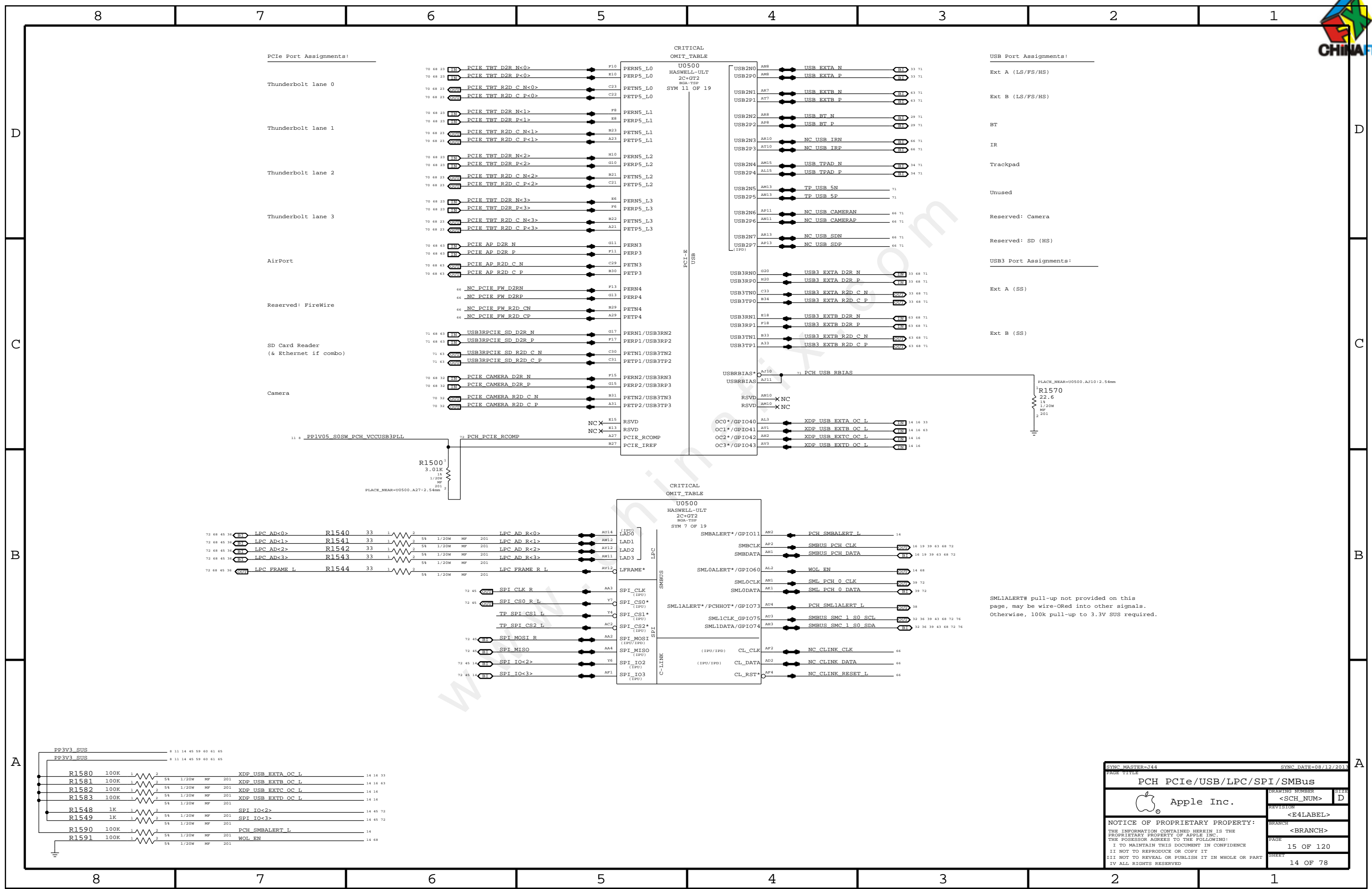
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**PCH PM/PCI/GFX**

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PCIe Port Assignments:

Thunderbolt lane 0	PCIE TBT D2R N<0>	F10	PERN5_L0
Thunderbolt lane 0	PCIE TBT D2R P<0>	E10	PERP5_L0
Thunderbolt lane 1	PCIE TBT R2D C N<0>	C23	PETN5_L0
Thunderbolt lane 1	PCIE TBT R2D C P<0>	C22	PETP5_L0
Thunderbolt lane 2	PCIE TBT D2R N<1>	F8	PERN5_L1
Thunderbolt lane 2	PCIE TBT D2R P<1>	E8	PERP5_L1
Thunderbolt lane 2	PCIE TBT R2D C N<1>	B23	PETN5_L1
Thunderbolt lane 2	PCIE TBT R2D C P<1>	A23	PETP5_L1
Thunderbolt lane 3	PCIE TBT D2R N<2>	H10	PERN5_L2
Thunderbolt lane 3	PCIE TBT D2R P<2>	G10	PERP5_L2
Thunderbolt lane 3	PCIE TBT R2D C N<2>	B21	PETN5_L2
Thunderbolt lane 3	PCIE TBT R2D C P<2>	C21	PETP5_L2
AirPort	PCIE AP D2R N	G11	PERN3
AirPort	PCIE AP D2R P	F11	PERP3
AirPort	PCIE AP R2D C N	C29	PETN3
AirPort	PCIE AP R2D C P	B30	PETP3
Reserved: FireWire	NC PCIE FW D2RN	F13	PERN4
Reserved: FireWire	NC PCIE FW D2RP	G13	PERP4
Reserved: FireWire	NC PCIE FW R2D CN	B29	PETN4
Reserved: FireWire	NC PCIE FW R2D CP	A29	PETP4
SD Card Reader (& Ethernet if combo)	USB3RPCIE SD D2R N	G17	PERN1/USB3RN2
SD Card Reader (& Ethernet if combo)	USB3RPCIE SD D2R P	F17	PERP1/USB3RP2
SD Card Reader (& Ethernet if combo)	USB3RPCIE SD R2D C N	C10	PETN1/USB3TN2
SD Card Reader (& Ethernet if combo)	USB3RPCIE SD R2D C P	C11	PETP1/USB3TP2
Camera	PCIE CAMERA D2R N	F15	PERN2/USB3RN3
Camera	PCIE CAMERA D2R P	G15	PERP2/USB3RP3
Camera	PCIE CAMERA R2D C N	B31	PETN2/USB3TN3
Camera	PCIE CAMERA R2D C P	A31	PETP2/USB3TP3

CRITICAL OMIT\_TABLE

U0500 HASWELL-ULT 2C+GT2 BGA-TSP SYM 11 OF 19

PCIE USB

RSVD AM10 X NC

RSVD AM10 X NC

OC0\*/GPIO40 AL3 XDP USB\_EXT\_A\_OC\_L 14 16 33

OC1\*/GPIO41 AT1 XDP USB\_EXT\_B\_OC\_L 14 16 63

OC2\*/GPIO42 AH2 XDP USB\_EXT\_C\_OC\_L 14 16

OC3\*/GPIO43 AV3 XDP USB\_EXT\_D\_OC\_L 14 16

USB Port Assignments:

USB2N0	AM8	USB_EXT_A_N	63 71
USB2P0	AM8	USB_EXT_A_P	63 71
USB2N1	AR7	USB_EXT_B_N	63 71
USB2P1	AT7	USB_EXT_B_P	63 71
USB2N2	AM9	USB_BT_N	29 71
USB2P2	AP9	USB_BT_P	29 71
USB2N3	AR10	NC USB_IRN	66 71
USB2P3	AT10	NC USB_IRP	66 71
USB2N4	AM15	USB_TPAD_N	34 71
USB2P4	AL15	USB_TPAD_P	34 71
USB2N5	AM13	TP_USB_5N	71
USB2P5	AM13	TP_USB_5P	71
USB2N6	AP11	NC_USB_CAMERAN	66 71
USB2P6	AM11	NC_USB_CAMERAP	66 71
USB2N7	AR13	NC_USB_SDN	66 71
USB2P7	AP13	NC_USB_SDP	66 71
USB3RN0	G20	USB3_EXT_A_D2R_N	33 68 71
USB3RP0	H20	USB3_EXT_A_D2R_P	33 68 71
USB3TN0	C33	USB3_EXT_A_R2D_C_N	33 68 71
USB3TP0	B34	USB3_EXT_A_R2D_C_P	33 68 71
USB3RN1	E18	USB3_EXT_B_D2R_N	63 68 71
USB3RP1	F18	USB3_EXT_B_D2R_P	63 68 71
USB3TN1	B33	USB3_EXT_B_R2D_C_N	63 68 71
USB3TP1	A33	USB3_EXT_B_R2D_C_P	63 68 71

USB3 Port Assignments:

Ext A (SS)	USB3_EXT_A_D2R_N	33 68 71
Ext A (SS)	USB3_EXT_A_D2R_P	33 68 71
Ext A (SS)	USB3_EXT_A_R2D_C_N	33 68 71
Ext A (SS)	USB3_EXT_A_R2D_C_P	33 68 71
Ext B (SS)	USB3_EXT_B_D2R_N	63 68 71
Ext B (SS)	USB3_EXT_B_D2R_P	63 68 71
Ext B (SS)	USB3_EXT_B_R2D_C_N	63 68 71
Ext B (SS)	USB3_EXT_B_R2D_C_P	63 68 71

CRITICAL OMIT\_TABLE

U0500 HASWELL-ULT 2C+GT2 BGA-TSP SYM 7 OF 19

SMBALERT\*/GPIO11 AN2 PCH\_SMBALERT\_L 14

SMBCLK AP2 SMBUS\_PCH\_CLK 16 19 39 63 68 72

SMBDATA AH1 SMBUS\_PCH\_DATA 16 19 39 63 68 72

SML0ALERT\*/GPIO60 AL2 WOL\_EN 14 68

SML0CLK AN1 SML\_PCH\_0\_CLK 39 72

SML0DATA AK1 SML\_PCH\_0\_DATA 39 72

SML1ALERT\*/PCHHOT\*/GPIO73 AD4 PCH\_SML1ALERT\_L 68

SML1CLK\_GPIO75 AH3 SMBUS\_SMC\_1\_S0\_SCL 32 36 39 43 68 72 76

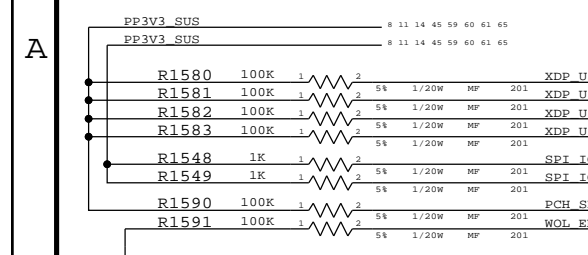
SML1DATA\_GPIO74 AH3 SMBUS\_SMC\_1\_S0\_SDA 32 36 39 43 68 72 76

(IPU/IPD) CL\_CLK AP2 NC\_CLINK\_CLK 66

(IPU/IPD) CL\_DATA AD2 NC\_CLINK\_DATA 66

(IPU) CL\_RST\* AP4 NC\_CLINK\_RESET\_L 66

SML1ALERT# pull-up not provided on this page, may be wire-ORed into other signals. Otherwise, 100k pull-up to 3.3V SUS required.



SYNC\_MASTER=144 SYNC\_DATE=08/12/2013

PAGE TITLE: PCH PCIe/USB/LPC/SPI/SMBus

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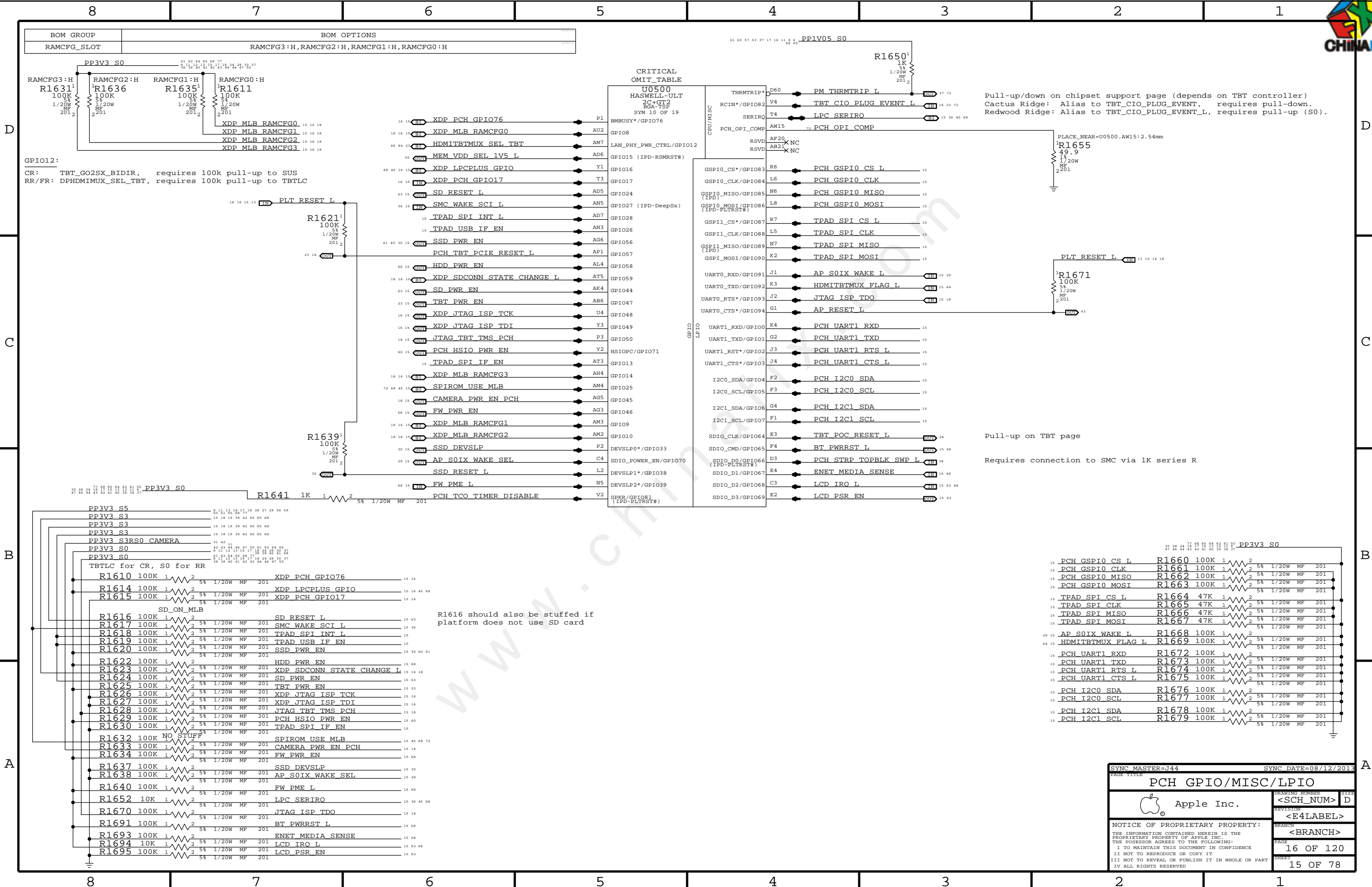
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BOM GROUP	BOM OPTIONS
RAMCFG_SLOT	RAMCFG3:H, RAMCFG2:H, RAMCFG1:H, RAMCFG0:H

GPIOL2:  
 CR: TBT\_GO2SX\_BIDIR, requires 100k pull-up to SUS  
 RR/FR: DPHDMIMUX\_SEL\_TBT, requires 100k pull-up to TBTLC

**CRITICAL OMIT TABLE**

U0500 HASWELL-ULT	GPIO	GPIO
2C+CT2 BGA-TSP SYM 10 OF 19	BMBUSY*/GPIO76	P1
	LAN_PHY_PWR_CTRL/GPIO12	AU2
	GPIO15 (IPD-RSMRST#)	AD6
	GPIO16	Y1
	GPIO17	T3
	GPIO24	AD5
	GPIO27 (IPD-DeepSx)	AN5
	GPIO28	AD7
	GPIO26	AN3
	GPIO56	AG6
	GPIO57	AP1
	GPIO58	AL4
	GPIO59	AT5
	GPIO44	AK4
	GPIO47	AB6
	GPIO48	U4
	GPIO49	Y3
	GPIO50	P3
	HSIOPC/GPIO71	Y2
	GPIO13	AT3
	GPIO14	AH4
	GPIO25	AM4
	GPIO45	AG5
	GPIO46	AG3
	GPIO9	AM3
	GPIO10	AM2
	DEVSLP0*/GPIO33	P2
	SDIO_POWER_EN/GPIO70	C4
	DEVSLP1*/GPIO38	L2
	DEVSLP2*/GPIO39	N5
	SPKR/GPIO81 (IPD-PLTRST#)	V2

Pull-up/down on chipset support page (depends on TBT controller)  
 Cactus Ridge: Alias to TBT\_CIO\_PLUGIN\_EVENT, requires pull-down.  
 Redwood Ridge: Alias to TBT\_CIO\_PLUGIN\_EVENT\_L, requires pull-up (S0).

Pull-up on TBT page  
 Requires connection to SMC via 1K series R

R1616 should also be stuffed if platform does not use SD card

SYNC MASTER=J44		SYNC DATE=08/12/2013	
PCH GPIO/MISC/LPIO			
Apple Inc.		DRAWING NUMBER	SIZE
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		REVISION	
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### Extra BPM Testpoints

- XDP\_BPM\_L<2> TP1802
- XDP\_BPM\_L<3> TP1803
- XDP\_BPM\_L<4> TP1804
- XDP\_BPM\_L<5> TP1805
- XDP\_BPM\_L<6> TP1806
- XDP\_BPM\_L<7> TP1807

### Merged (CPU/PCH) Micro2-XDP

NOTE: This is not the standard XDP pinout. Use with 921-0133 Adapter Flex to support chipset debug.

- XDP\_CPU\_TDO R1810 51 1
  - XDP\_CPU\_TCK R1813 51 2
- TDI and TMS are terminated in CPU.

D

D

C

C

B

B

A

A

### PCH XDP Signals

These signals do not connect to XDP connector in this architecture, only accessible via Top-Side Probe. Nets are listed here to show XDP associations and to make clear what restrictions exist on PCH GPIOs when Top-Side Probe is used for PCH debug.

#### PCH/XDP Signals

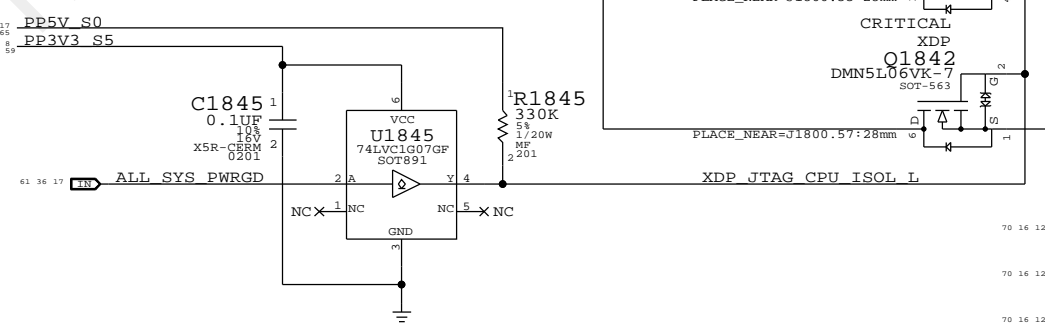
- XDP\_MLB\_RAMCFG0 TP1870
- XDP\_USB\_EXT\_A\_OC\_L MAKE\_BASE=TRUE
- XDP\_USB\_EXT\_B\_OC\_L MAKE\_BASE=TRUE
- XDP\_USB\_EXT\_C\_OC\_L TP1873
- XDP\_USB\_EXT\_D\_OC\_L TP1874
- XDP\_SDCONN\_STATE\_CHANGE\_L MAKE\_BASE=TRUE
- XDP\_MLB\_RAMCFG1 TP1876
- XDP\_MLB\_RAMCFG2 TP1877
- XDP\_MLB\_RAMCFG3 TP1878

#### Non-XDP Signals

- JTAG\_ISP\_TCK
- XDP\_SSD\_PCIE3\_SEL\_L R1881 1K
- XDP\_SSD\_PCIE2\_SEL\_L R1882 1K
- XDP\_SSD\_PCIE1\_SEL\_L R1883 1K
- XDP\_SSD\_PCIE0\_SEL\_L R1884 1K
- XDP\_LPCPLUS\_GPIO
- XDP\_PCH\_GPIO17 TP1886
- XDP\_PCH\_GPIO76 TP1887
- JTAG\_ISP\_TDI

Unused & MLB\_RAMCFGx GPIOs have TPs.  
 USB Overcurrents are aliased, do not cause USB OC# events during PCH debug.  
 SDCONN\_STATE\_CHANGE\_L is aliased, do not plug/unplug SD Cards during PCH debug.  
 JTAG\_ISP (non-TMS) nets are aliased, do not attempt bit-banged JTAG during PCH debug.  
 NOTE: Should force PCH GPIO47 high to ensure TBT router powered to avoid leakage/clamping of signals.  
 SSD\_PCIEx\_SEL\_L straps are connected via 1K to common net.  
 LPCPLUS\_GPIO is aliased, do not attempt use during PCH debug.

### CPU JTAG Isolation



- PCH\_JTAGX R1899 1K
- XDP\_PCH\_TDO R1890 51 2
- XDP\_PCH\_TDI R1891 51 2
- XDP\_PCH\_TMS R1892 51 2
- XDP\_PCH\_TCK R1896 51 2
- XDP\_CPURCH\_TRST R1897 51 2

SYNC MASTER=J44		SYNC DATE=08/12/2013	
<b>CPU/PCH Merged XDP</b>			
Apple Inc.		DRAWING NUMBER	SIZE
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# System RTC Power Source & 32kHz / 25MHz Clock Generator

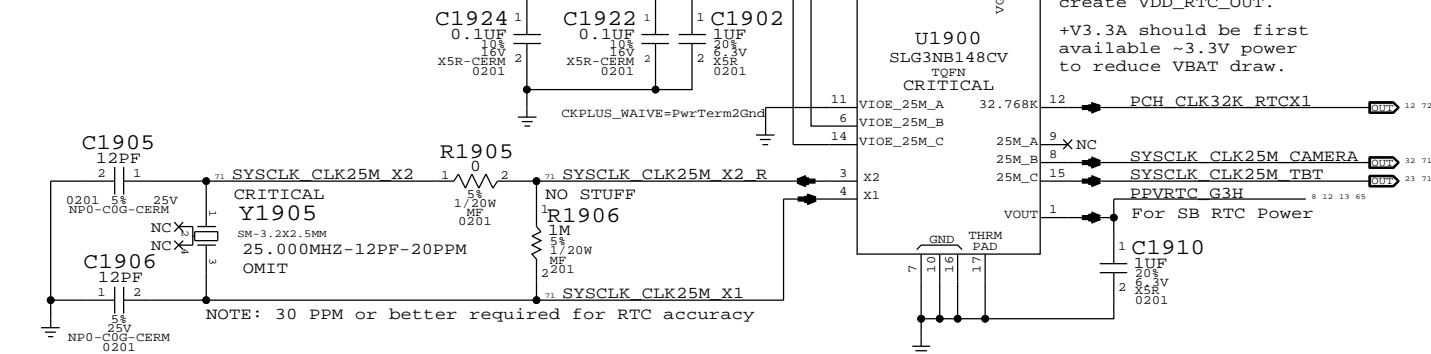
Chipset uses 24MHz crystal, GreenCLK kept to save 1x 25MHz crystal & 1x 32kHz crystal

This looks a little ugly to support new and old parts. With GreenCLK Rev C pin 5 must receive S5 power (Stuff R2042)

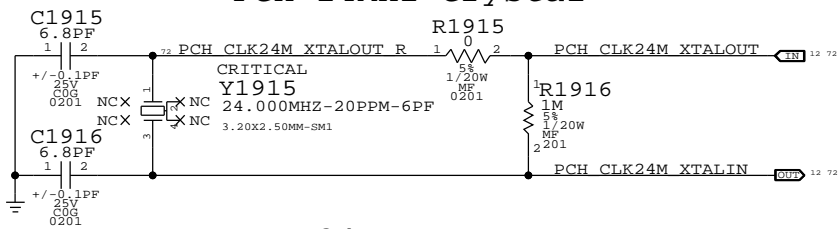
**PP3V42 G3H**  
Coin-Cell: VBAT (300-ohm & 10uF RC)  
No Coin-Cell: 3.42V G3Hot  
**PP3V3 S5**  
Coin-Cell & G3Hot: 3.42V G3Hot  
Coin-Cell & No G3Hot: 3.3V S5  
No Coin-Cell: 3.3V S5

GreenCLK 25MHz Power Must be powered if any VDDIO is powered.

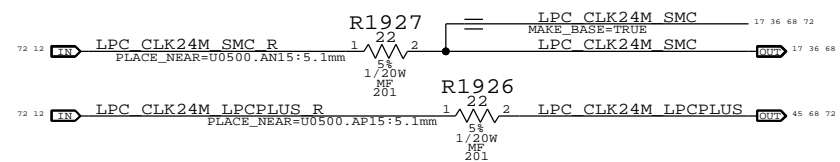
CAM XTAL Power  
TBT XTAL Power



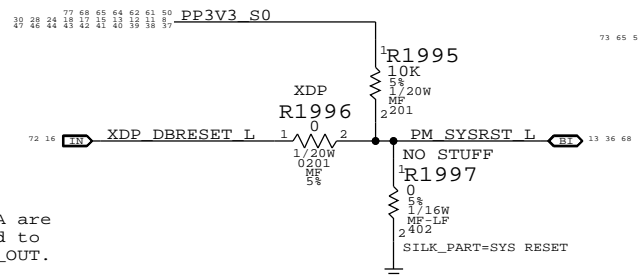
## PCH 24MHz Crystal



## PCH 24MHz Outputs

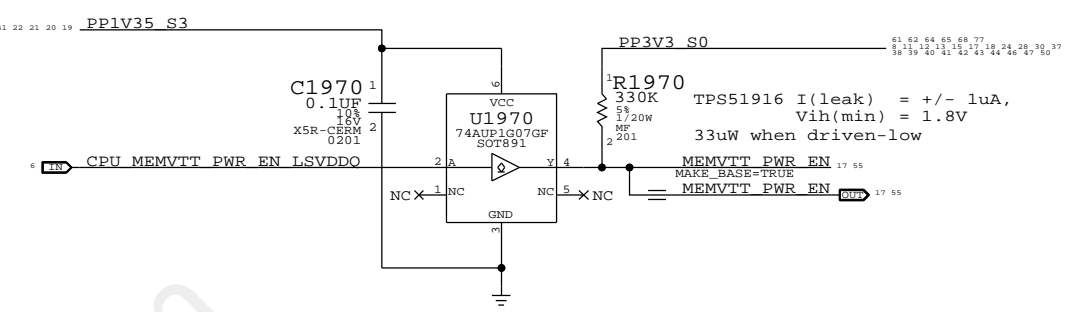


## PCH Reset Button

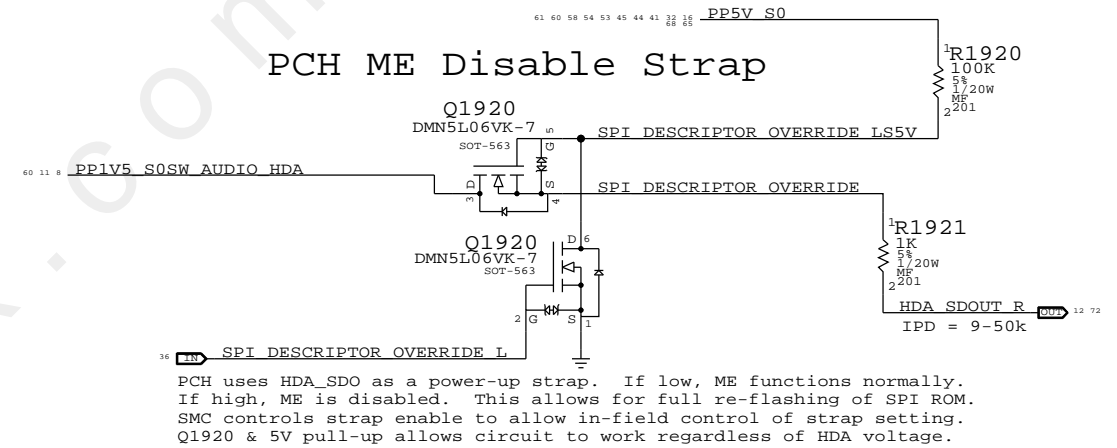


## Memory VTT Enable Level-Shifter

CPU output is on VDDQ rail (1.2V), TPS51916 has 1.8V Vih(min).

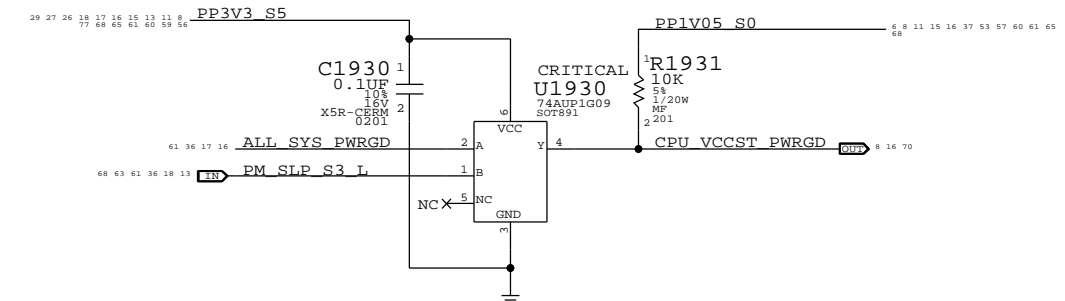


## PCH ME Disable Strap

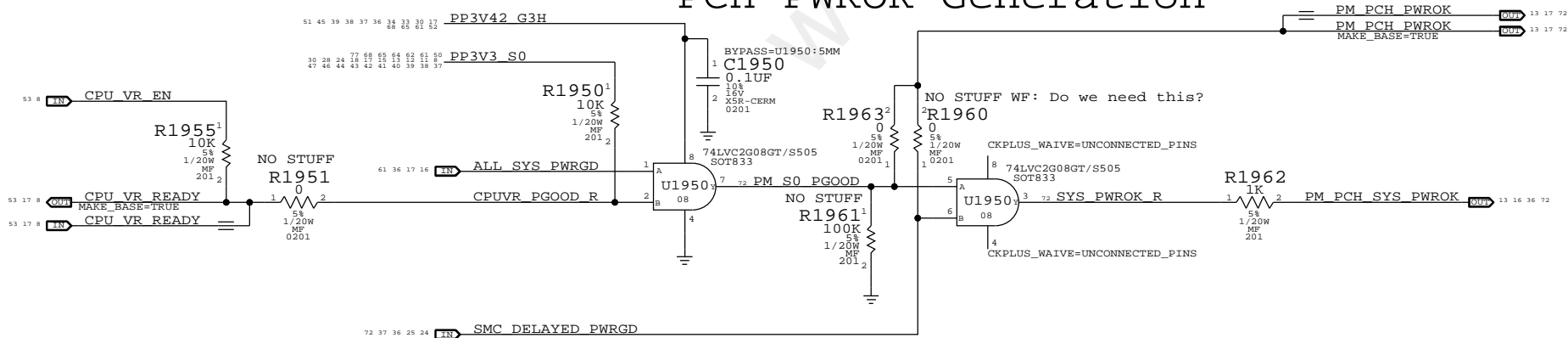


PCH uses HDA\_SDO as a power-up strap. If low, ME functions normally. If high, ME is disabled. This allows for full re-flashing of SPI ROM. SMC controls strap enable to allow in-field control of strap setting. Q1920 & 5V pull-up allows circuit to work regardless of HDA voltage.

## VCCST (1.05V S0) PWRGD



## PCH PWROK Generation



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
197S0480	1	XTAL, 25MHZ, 20PPM, 12PF, 3.2X2.5X.6MM, 85C	Y1905		

SYNC MASTER=J44 SYNC DATE=08/12/2013

**Chipset Support**

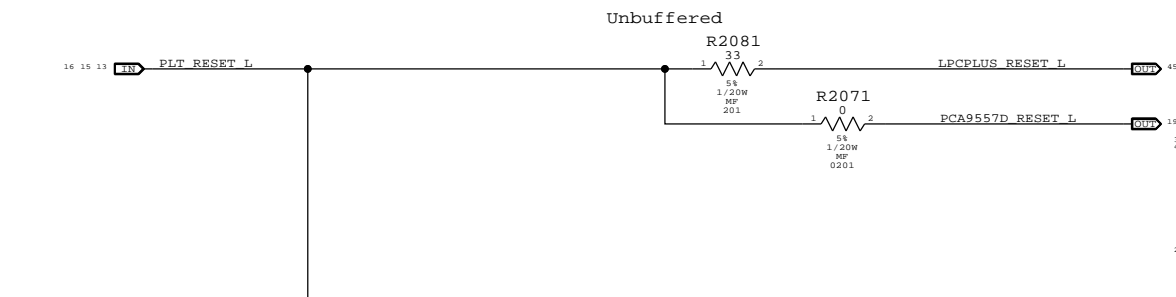
Apple Inc.

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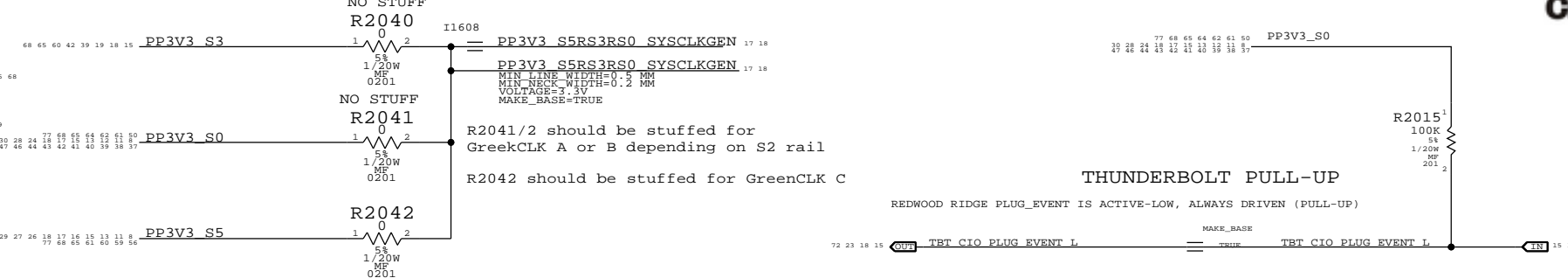
DRAWING NUMBER: <SCH\_NUM> D  
REVISION: <E4LABEL>  
BRANCH: <BRANCH>  
PAGE: 19 OF 120  
SHEET: 17 OF 78



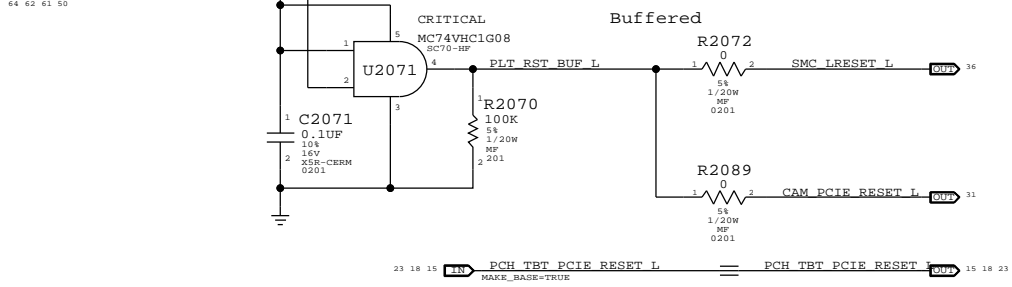
### Platform Reset Connections



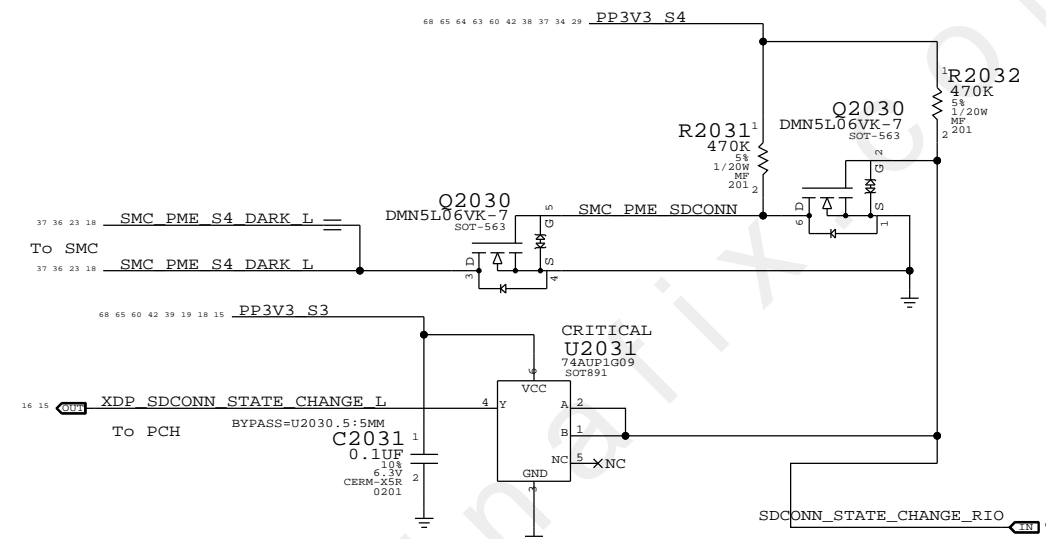
### GreenCLK 25MHz Power



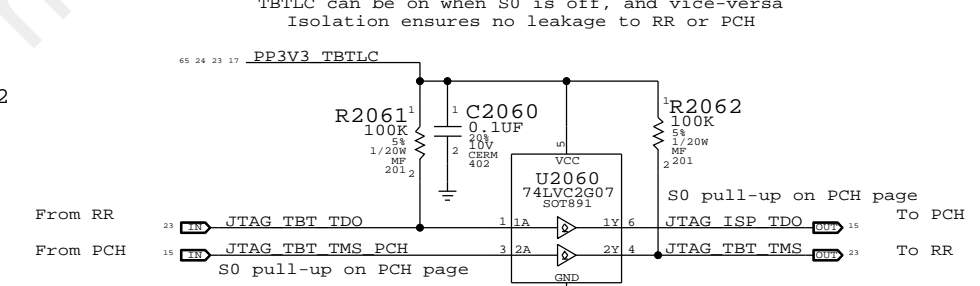
### Scrub for Layout Optimization



### SDCONN\_STATE\_CHANGE Isolation



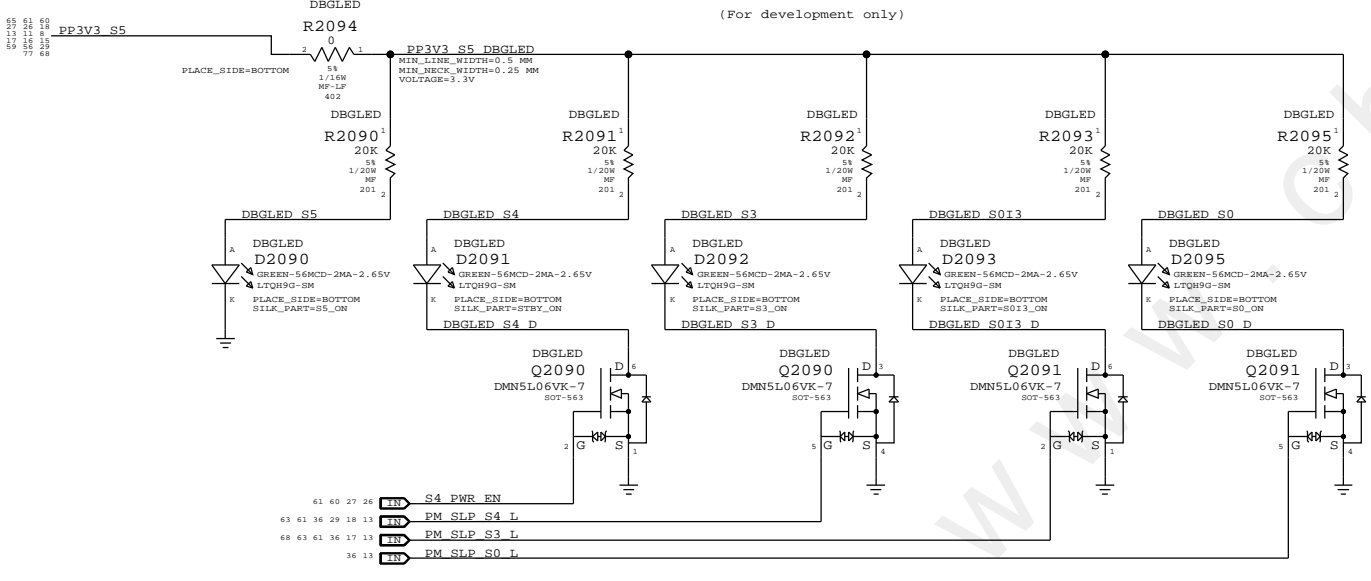
### Redwood Ridge JTAG Isolation



NOTE: Solution shown is for LPT-LP. Other PCH's may require isolation on TCK and TDI as well for PCH glitch-prevention.

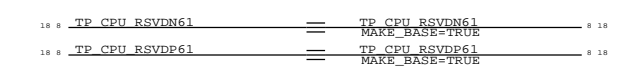
NOTE: This reference schematic assumes PCH JTAG GPIOs are only used for Thunderbolt. If other ASIC JTAG signals are wired into these GPIOs different isolation techniques will likely be necessary. Multi-router designs also require different circuitry.

### Power State Debug LEDs

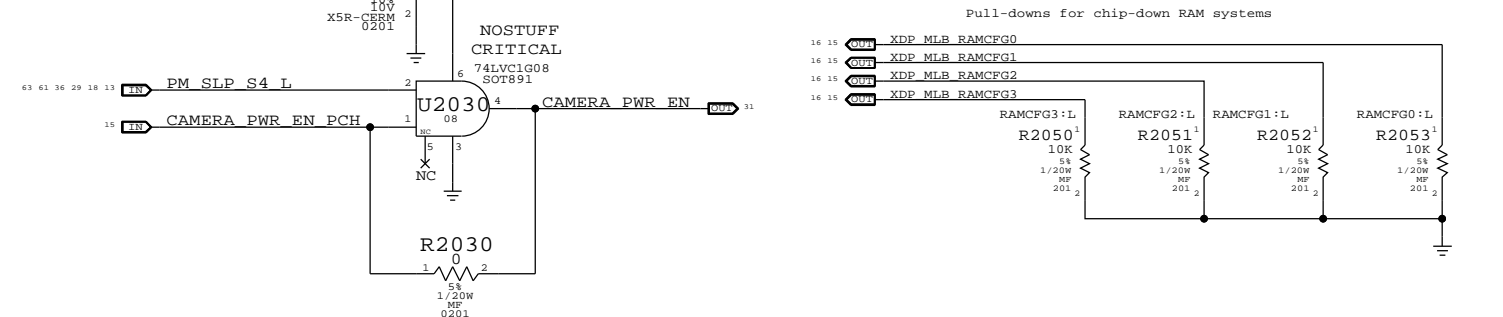


Pin N61 needs a TP for Power to perform iFDIM test

Renaming the pins N61 and P61 to remove automatic diffpari property



### RAM Configuration Straps



SYNC MASTER=144		SYNC DATE=08/12/2013	
Project Chipset Support			
Apple Inc.		DRAWING NUMBER	SIZE
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		REVISION	
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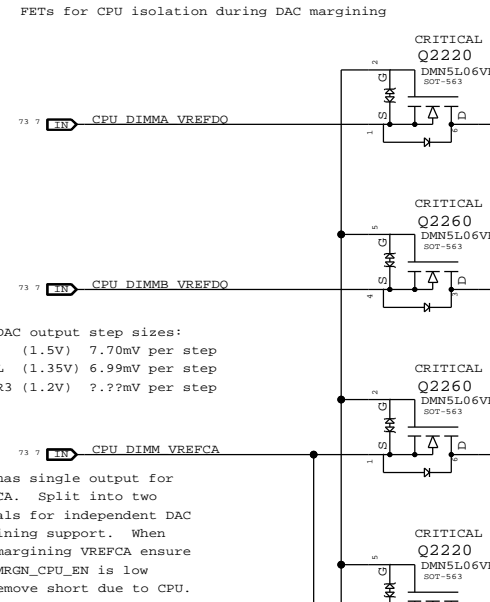
Page Notes

Power aliases required by this page:  
 - =PP3V3\_S3\_VREFMRGN  
 - =PPDDR\_S3\_MEMVREF

Signal aliases required by this page:  
 - =I2C\_VREFDACS\_SCL  
 - =I2C\_VREFDACS\_SDA  
 - =I2C\_PCA9557D\_SCL  
 - =I2C\_PCA9557D\_SDA

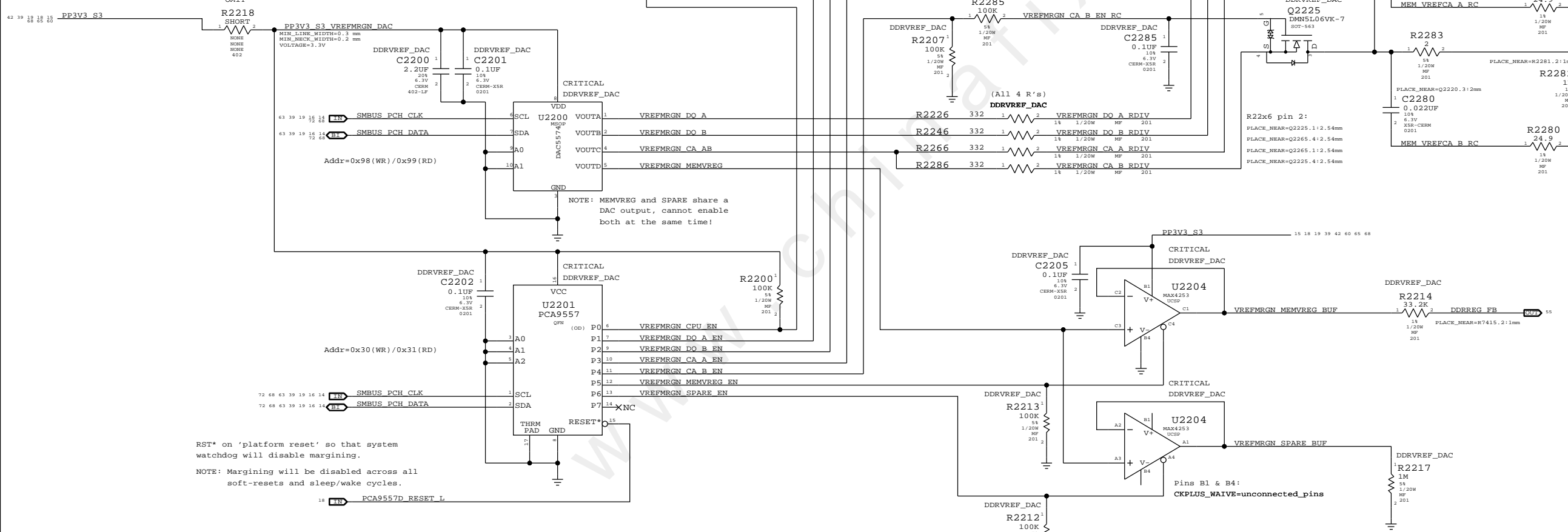
BOM options provided by this page:  
 - DDRVREF\_DAC - Stuffs DAC margining circuit.

CPU-Based Margining



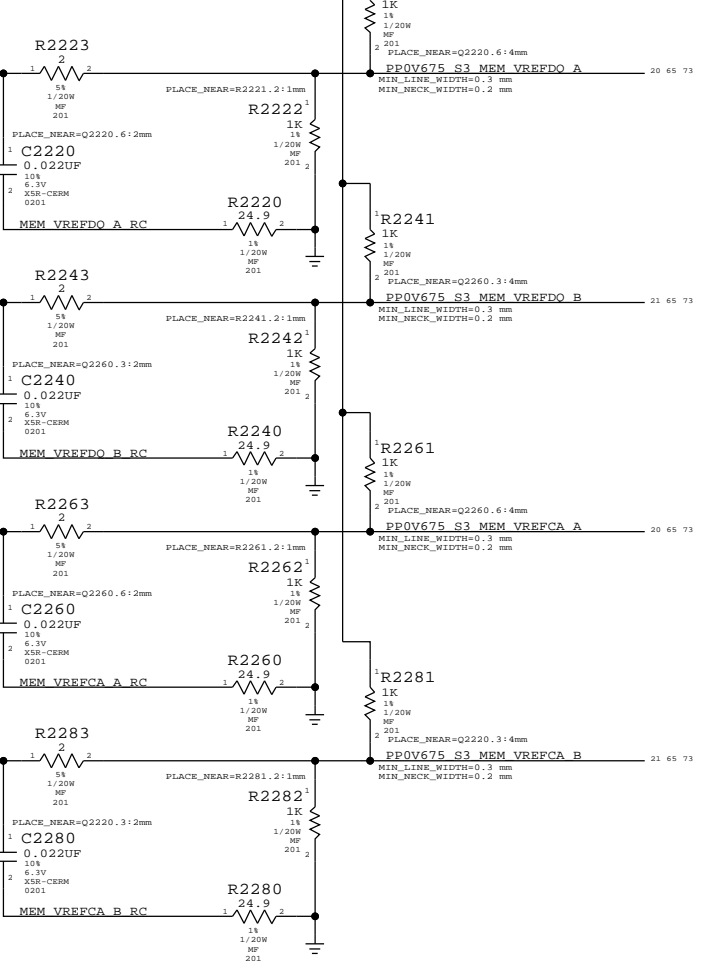
DAC-Based Margining

DAC sets voltage level, PCA9557 & FETs enable outputs and disables margining after platform reset.



VRef Dividers

Always used, regardless of margining option.



	MEM A VREF DQ	MEM B VREF DQ	MEM A VREF CA	MEM B VREF CA	MEM VREG
DAC Channel:	A	B	C	C	D
PCA9557D Pin:	1	2	3	4	5
Nominal value	LPDDR3 (1.2V)		DDR3L (1.35V)		LPDDR3 (1.2V)
Margining target:	0.300V - 0.900V (+/- 300mV)		0.337V - 1.013V (+/- 337.5mV)		0.800V - 1.600V (+/- 400mV)
DAC range:	0.000V - 1.199V (0x00 - 0x5D)		0.000V - 1.354V (0x00 - 0x69)		0.000V - 2.397V (0x00 - 0xBA)
Vref current:	+73uA - -73uA (- = sourced)		+82uA - -82uA (- = sourced)		+21uA - -21uA (- = sourced)
DAC step size:	6.36mV / step @ output		6.36mV / step @ output		4.28mV / step @ output

NOTE: LPDDR3 assumes TPS51916 supply with 28.7k/57.6k divider  
 DDR3L assumes TPS51916 supply with 19.6k/57.6k divider

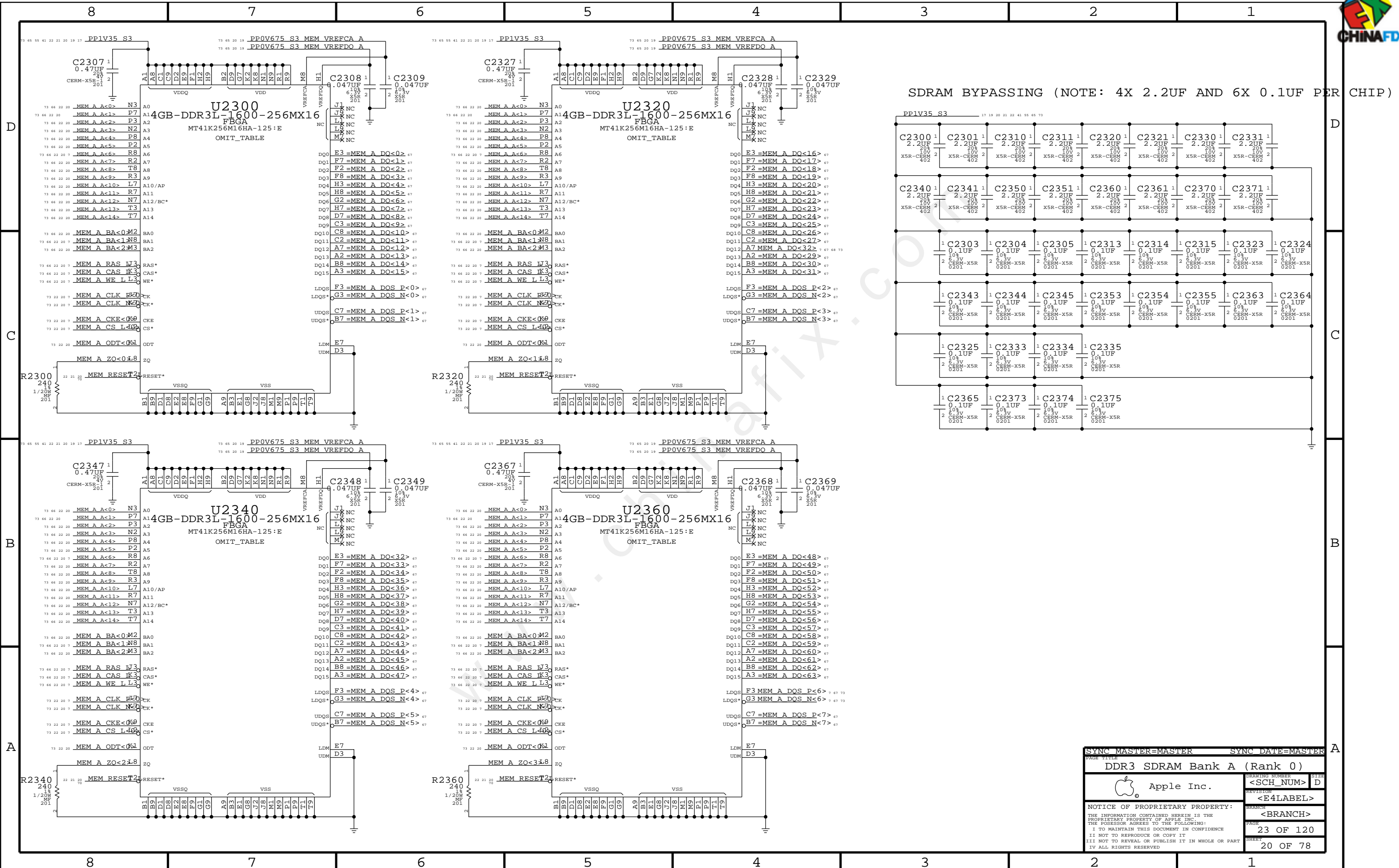
SYNC MASTER=144 SYNC DATE=08/12/2013

DDR3 VREF MARGINING

Apple Inc.

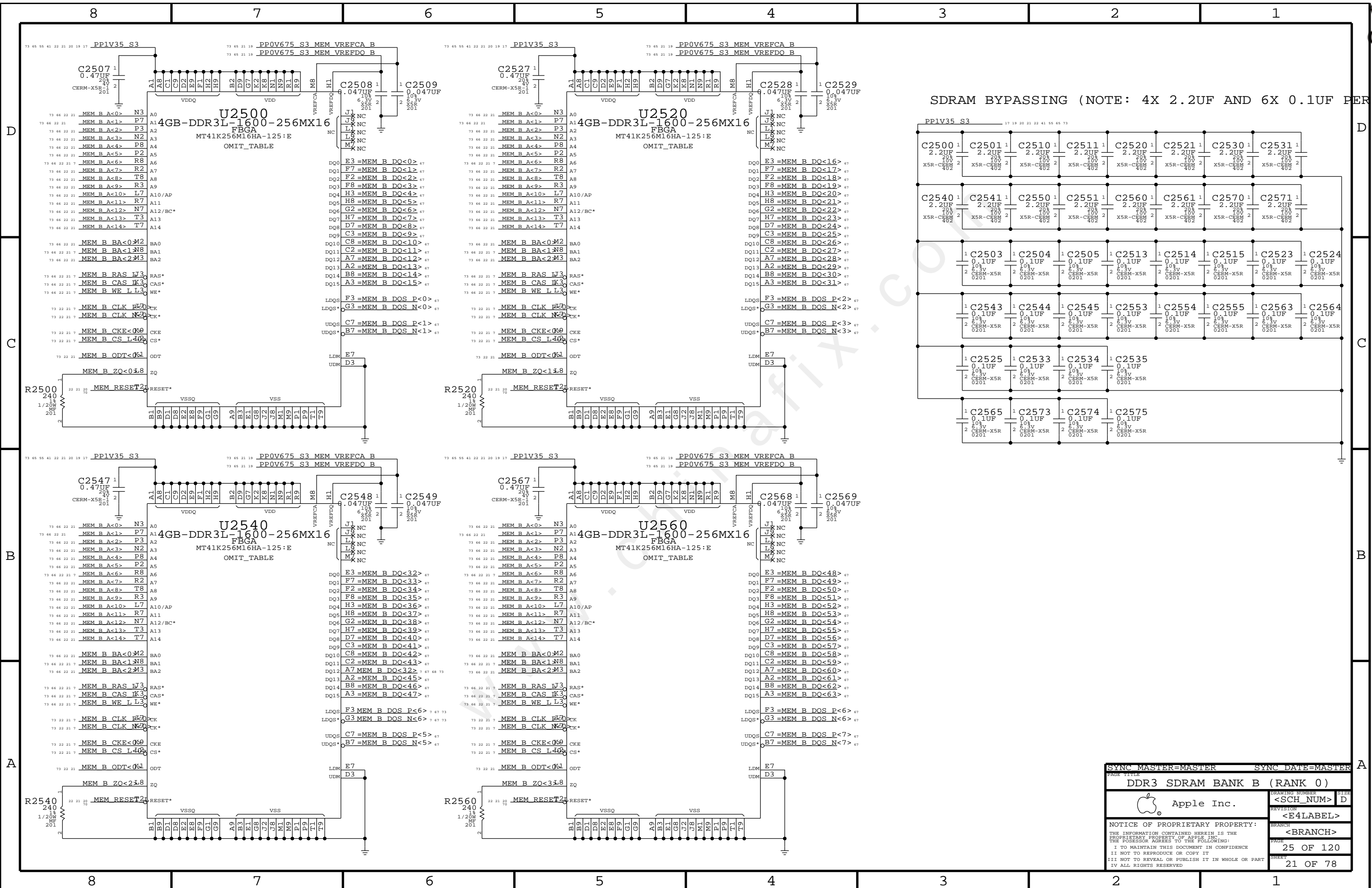
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 PAGE: 22 OF 120  
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SDRAM BYPASSING (NOTE: 4X 2.2UF AND 6X 0.1UF PER CHIP)

SYNC MASTER=MASTER		SYNC DATE=MASTER	
PAGE TITLE			
DDR3 SDRAM Bank A (Rank 0)			
DRAWING NUMBER		SIZE	
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REVISION		<E4LABEL>	
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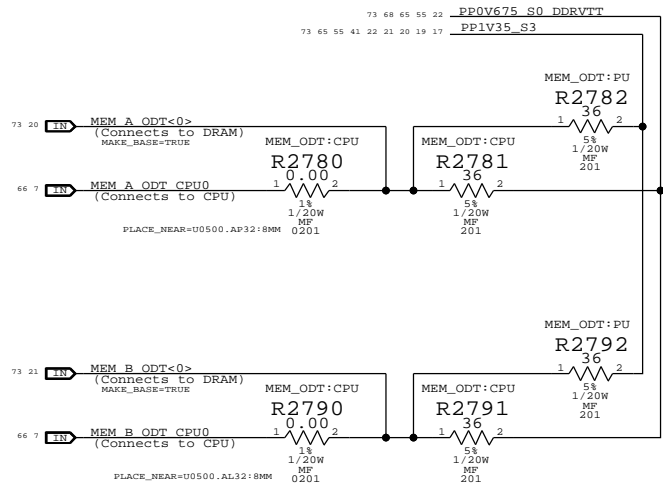
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PAGE TITLE			
DDR3 SDRAM BANK B (RANK 0)			
Apple Inc.		BRANCH NUMBER	SHEET
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		SHEET	21 OF 78



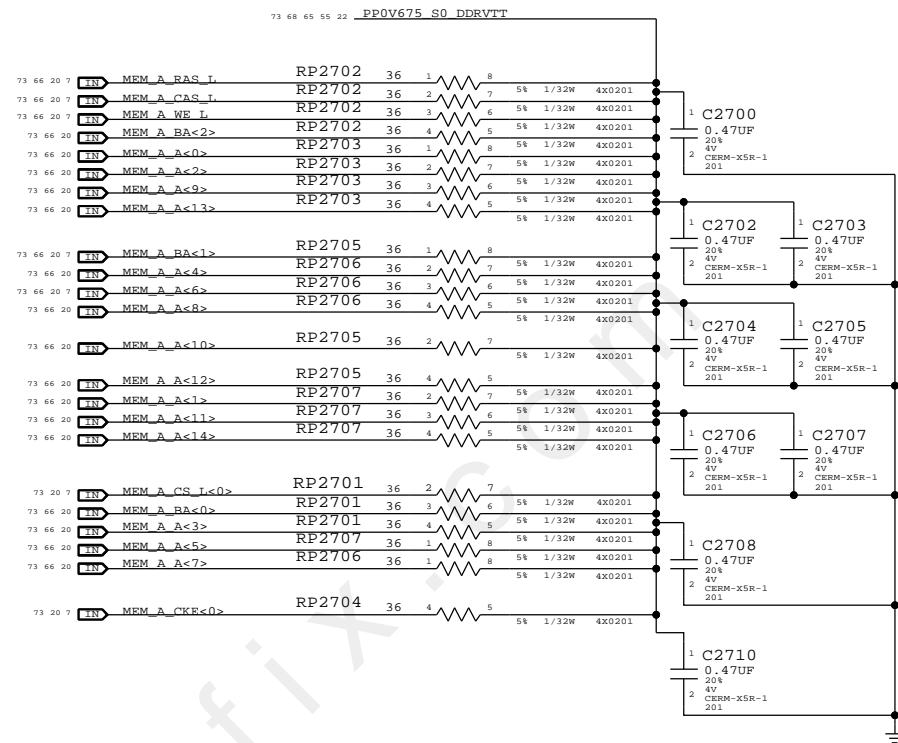
8 7 6 5 4 3 2 1

### Memory ODT Option

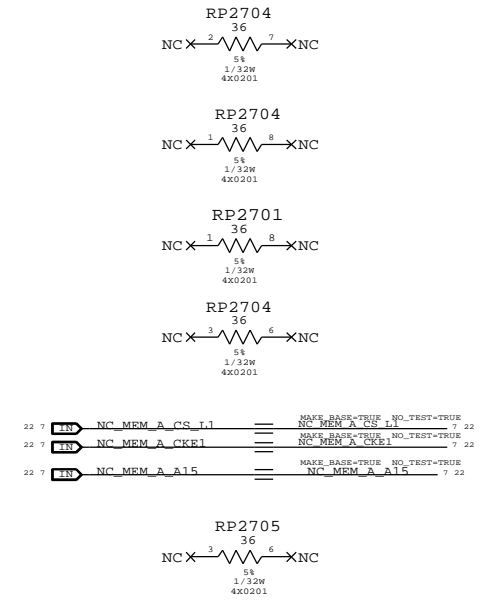
MEM\_ODT:CPU drives ODT from CPU, terminated to 0.675V VTT.  
MEM\_ODT:PU disconnect ODT from CPU, ODT pins on DRAM pulled up to 1.35V VDDQ.



### Memory CMD/CTL Termination - Channel A

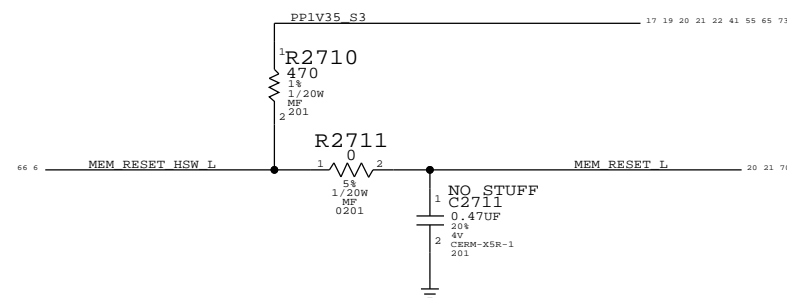


### MEMORY RPACK SPARES

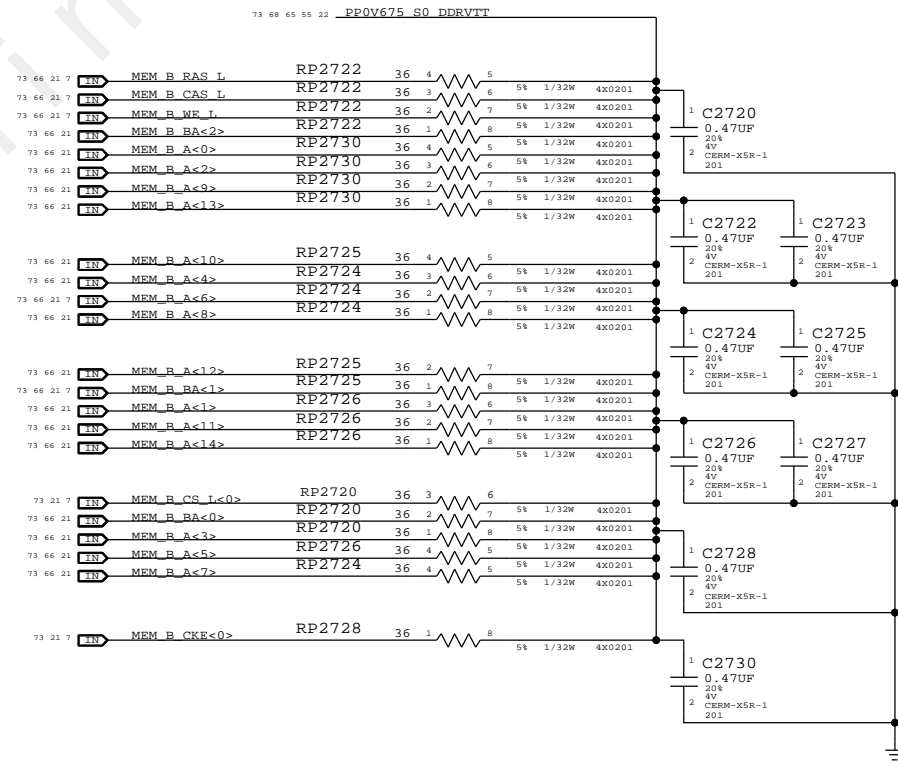


### Memory Reset Pull Up

Reset is an open drain in Haswell ULT and needs pull up

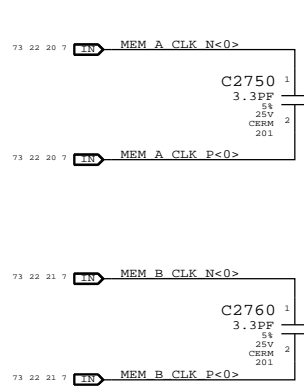


### Memory CMD/CTL Termination - Channel B



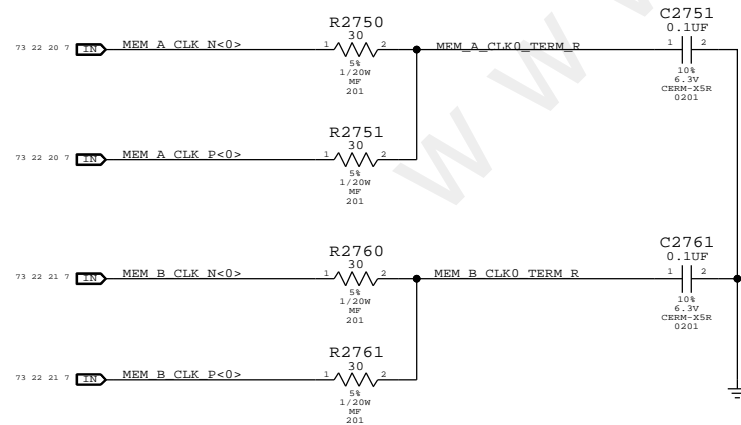
### Memory Clock Near-End Termination

Place Source C termination before first DRAM



### Memory Clock Far-End Termination

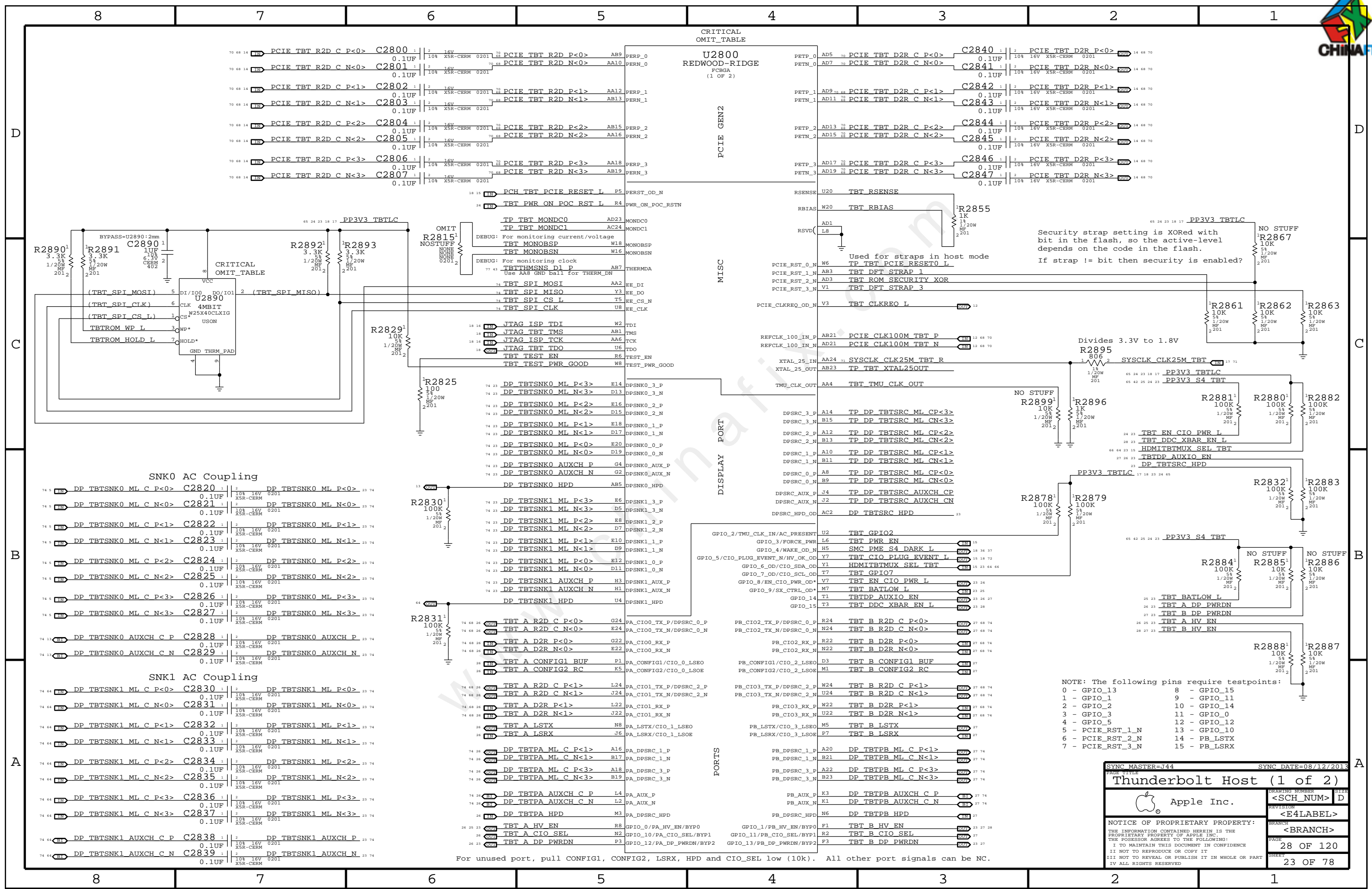
Place RC end termination after last DRAM



SYNC MASTER=J44 YONAS-4GB SYNC DATE=04/02/2013

DDR3 Termination		DRAWING NUMBER	SIZE
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		PAGE	27 OF 120
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8 7 6 5 4 3 2 1



Security strap setting is XORed with bit in the flash, so the active-level depends on the code in the flash.  
If strap != bit then security is enabled?

Divides 3.3V to 1.8V

- NOTE: The following pins require testpoints:
- |                  |              |
|------------------|--------------|
| 0 - GPIO_13      | 8 - GPIO_15  |
| 1 - GPIO_1       | 9 - GPIO_11  |
| 2 - GPIO_2       | 10 - GPIO_14 |
| 3 - GPIO_3       | 11 - GPIO_0  |
| 4 - GPIO_5       | 12 - GPIO_12 |
| 5 - PCIE_RST_1_N | 13 - GPIO_10 |
| 6 - PCIE_RST_2_N | 14 - PB_LSTX |
| 7 - PCIE_RST_3_N | 15 - PB_LSRX |

SYNC MASTER=J44 SYNC DATE=08/12/2013

Thunderbolt Host (1 of 2)

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DRAWING NUMBER: <SCH NUM> D

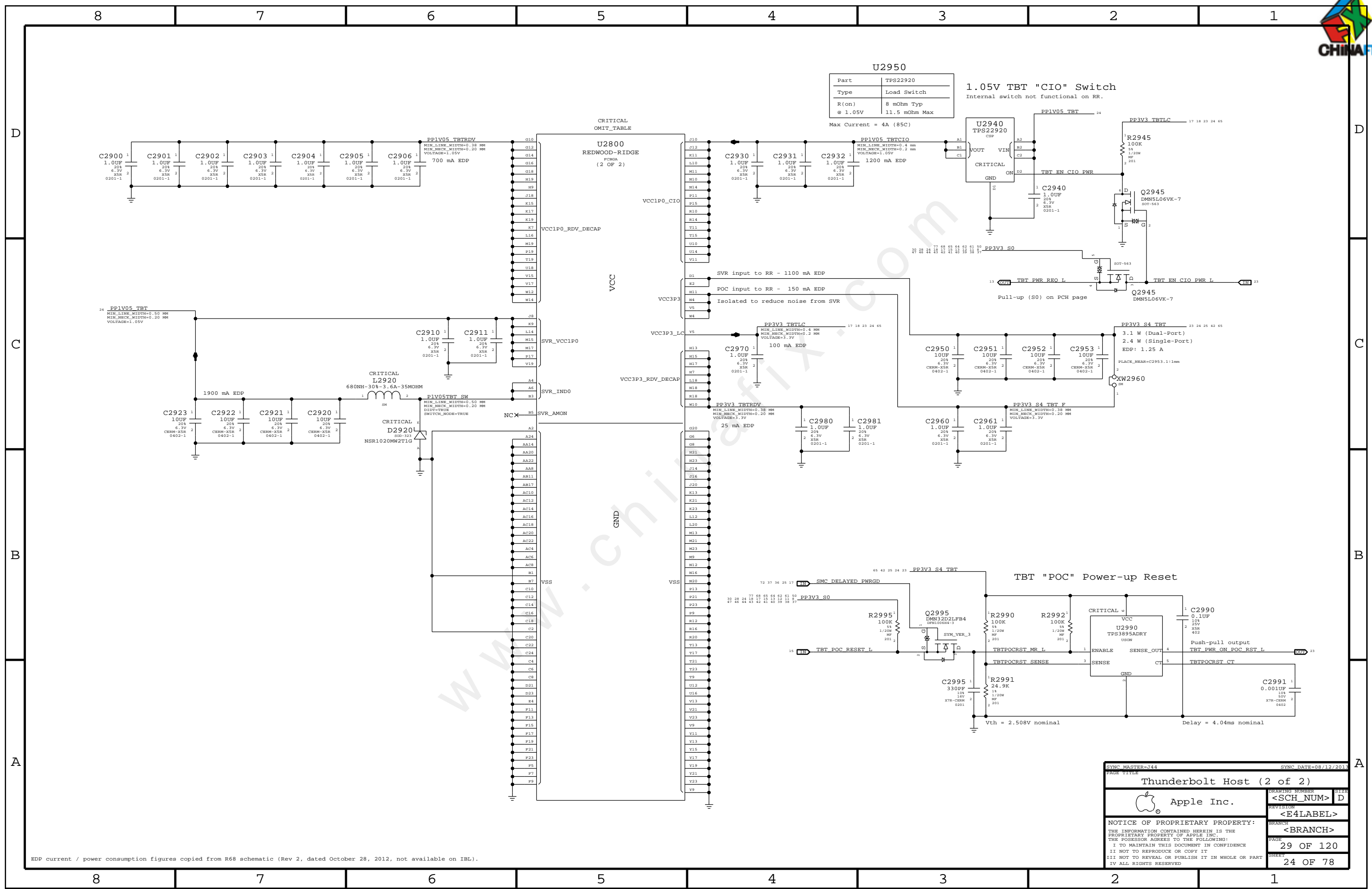
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For unused port, pull CONFIG1, CONFIG2, LSRX, HPD and CIO\_SEL low (10k). All other port signals can be NC.



U2950

Part	TPS22920
Type	Load Switch
R(on)	8 mOhm Typ
@ 1.05V	11.5 mOhm Max

Max Current = 4A (85C)

1.05V TBT "CIO" Switch  
Internal switch not functional on RR.

3.1 W (Dual-Port)  
2.4 W (Single-Port)  
EDP: 1.25 A  
PLACE\_NEAR=C2953.1:1mm

TBT "POC" Power-up Reset

SYNC MASTER=144		SYNC DATE=08/12/2013	
PAGE TITLE			
Thunderbolt Host (2 of 2)			
Apple Inc.		DRAWING NUMBER	SIZE
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EDP current / power consumption figures copied from R68 schematic (Rev 2, dated October 28, 2012, not available on IBL).



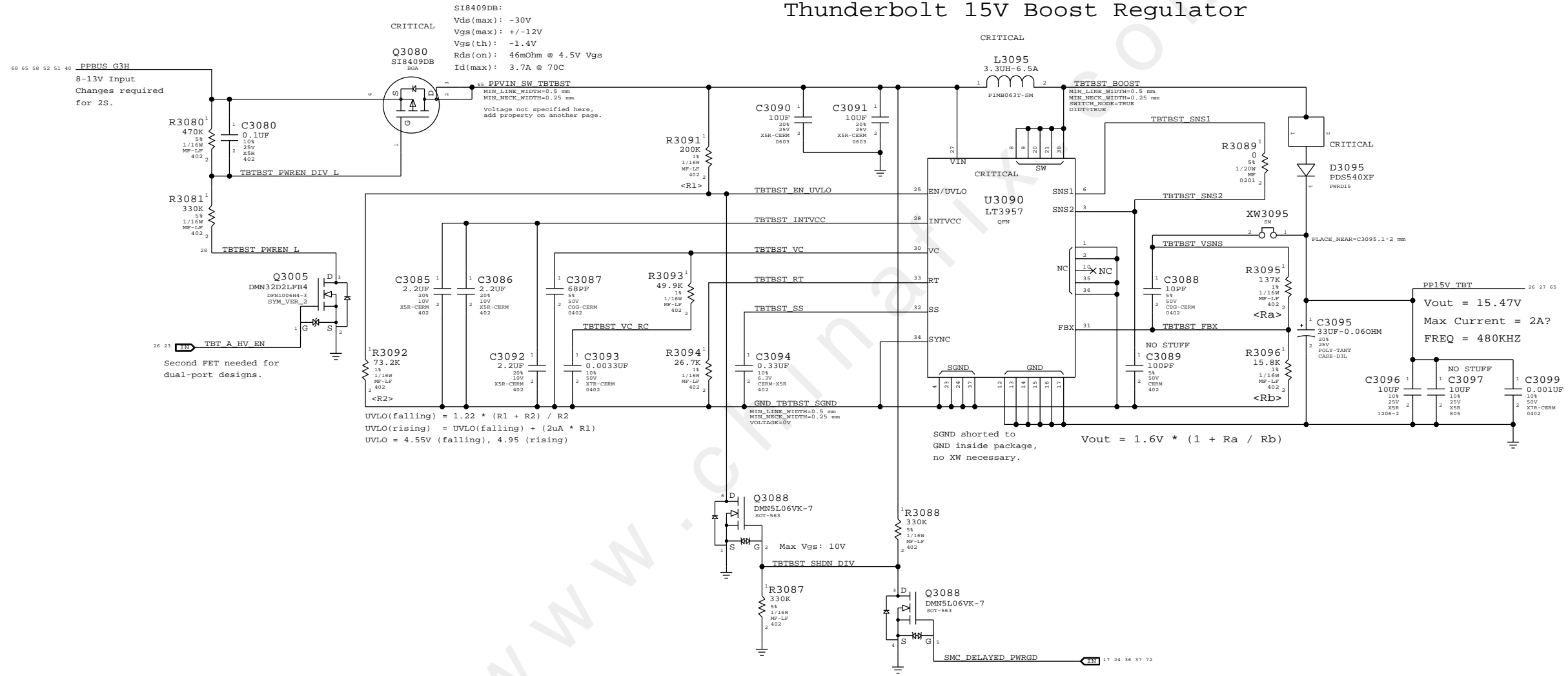
### Page Notes

Power aliases required by this page:  
 - =PPVIN\_SW\_TBTBST (8-13V Boost Input)  
 - =PP15V\_TBT\_REG (15V Boost Output)

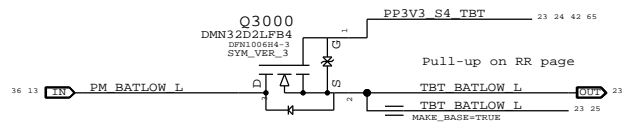
Signal aliases required by this page:  
 (NONE)

BOM options provided by this page:  
 (NONE)

## Thunderbolt 15V Boost Regulator



### BATLOW# Isolation

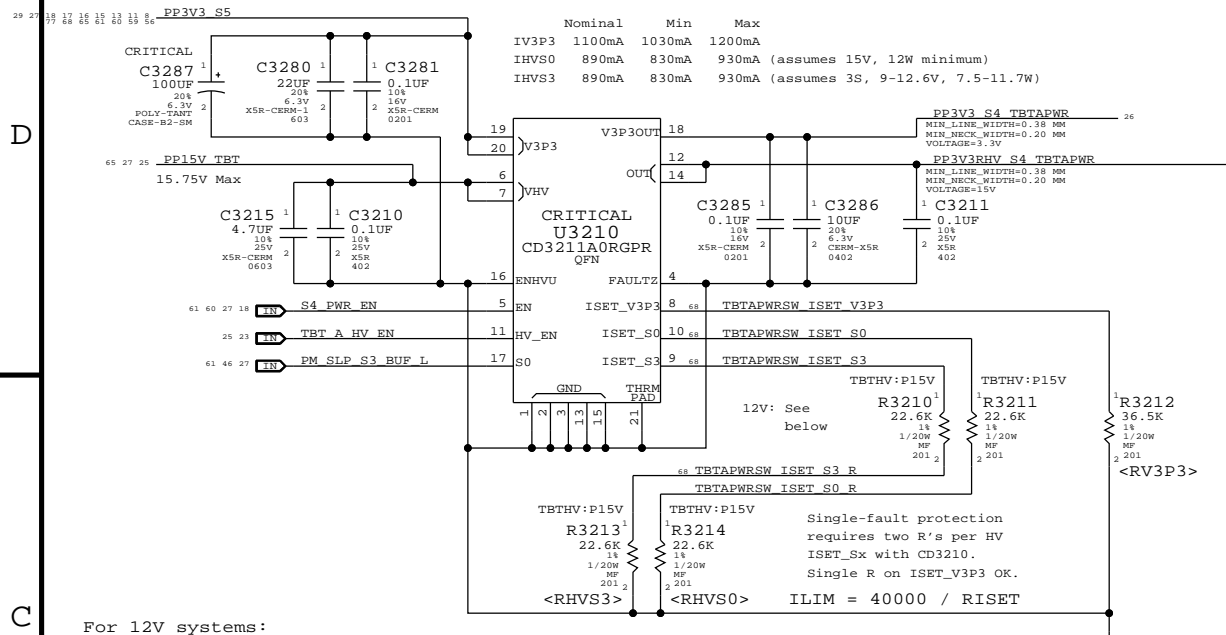


SYNC MASTER=144		SYNC DATE=08/12/2013	
Thunderbolt Mobile Support			
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### 3.3V/HV Power MUX

V3P3 must be S4 to support wake from Thunderbolt devices.

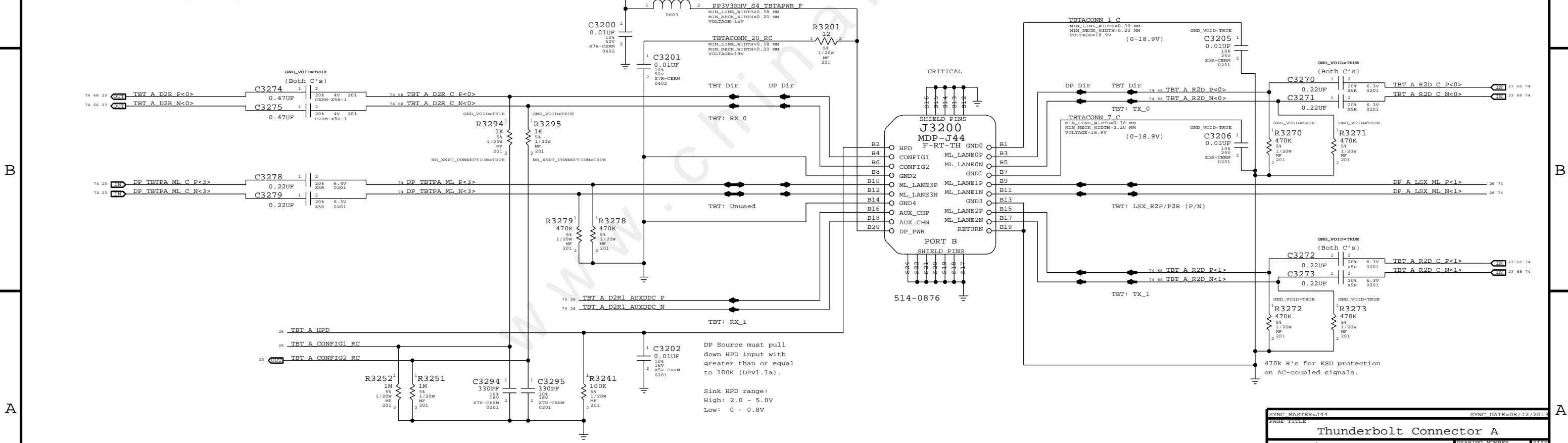


For 12V systems:

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
118S0145	2	RES_MTL FILM,1/20W,17.8K,1.0201,SMD,LF	R3210,R3213		TBTHV:P12V
118S0145	2	RES_MTL FILM,1/20W,17.8K,1.0201,SMD,LF	R3211,R3214		TBTHV:P12V

Nominal	Min	Max	
IHV50/S3	1120mA	1090mA	1170mA (12W minimum)

### Thunderbolt Connector A



SYNC MASTER=144 SYNC DATE=08/12/2013

**Thunderbolt Connector A**

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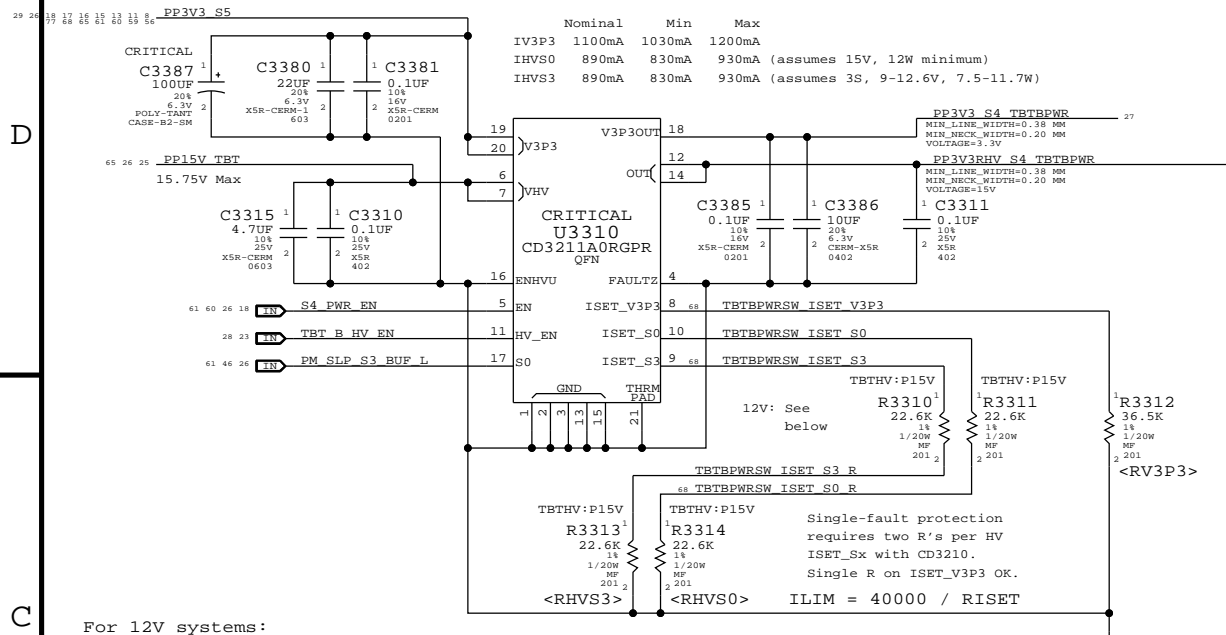
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### 3.3V/HV Power MUX

V3P3 must be S4 to support wake from Thunderbolt devices.

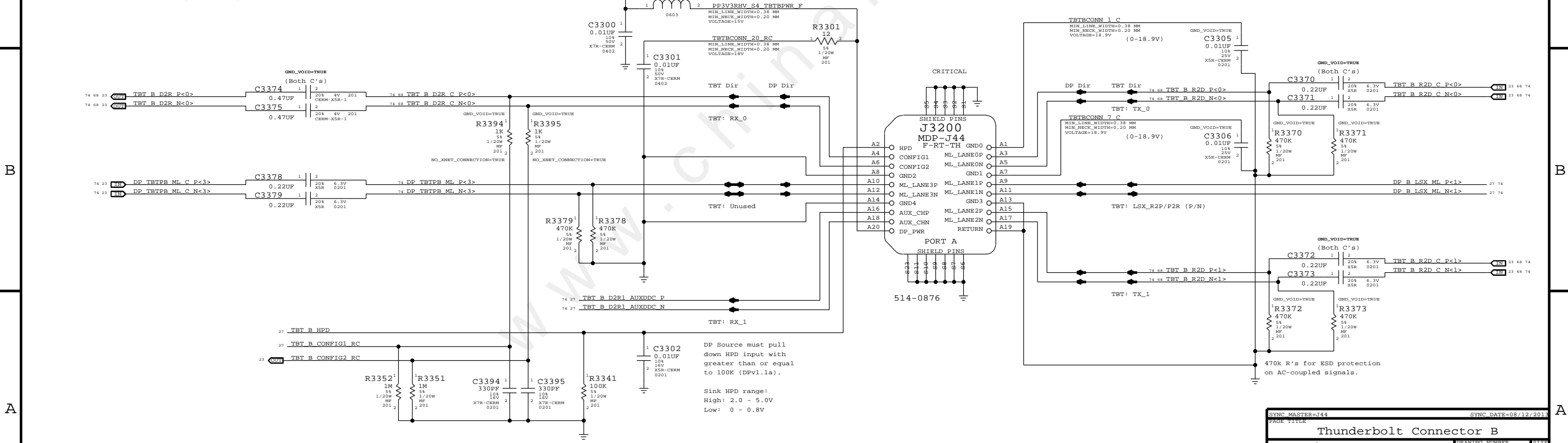


For 12V systems:

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
118S0145	2	RES_MTL_FILM,1/20W,17.8K,1.0201,SMD,LF	R3310,R3313		TBTHV:P12V
118S0145	2	RES_MTL_FILM,1/20W,17.8K,1.0201,SMD,LF	R3311,R3314		TBTHV:P12V

Nominal	Min	Max	
IHV50/S3	1120mA	1090mA	1170mA (12W minimum)

### Thunderbolt Connector B



DP Source must pull down HPD input with greater than or equal to 100K (DPv1.1a).

Sink HPD range:  
High: 2.0 - 5.0V  
Low: 0 - 0.8V

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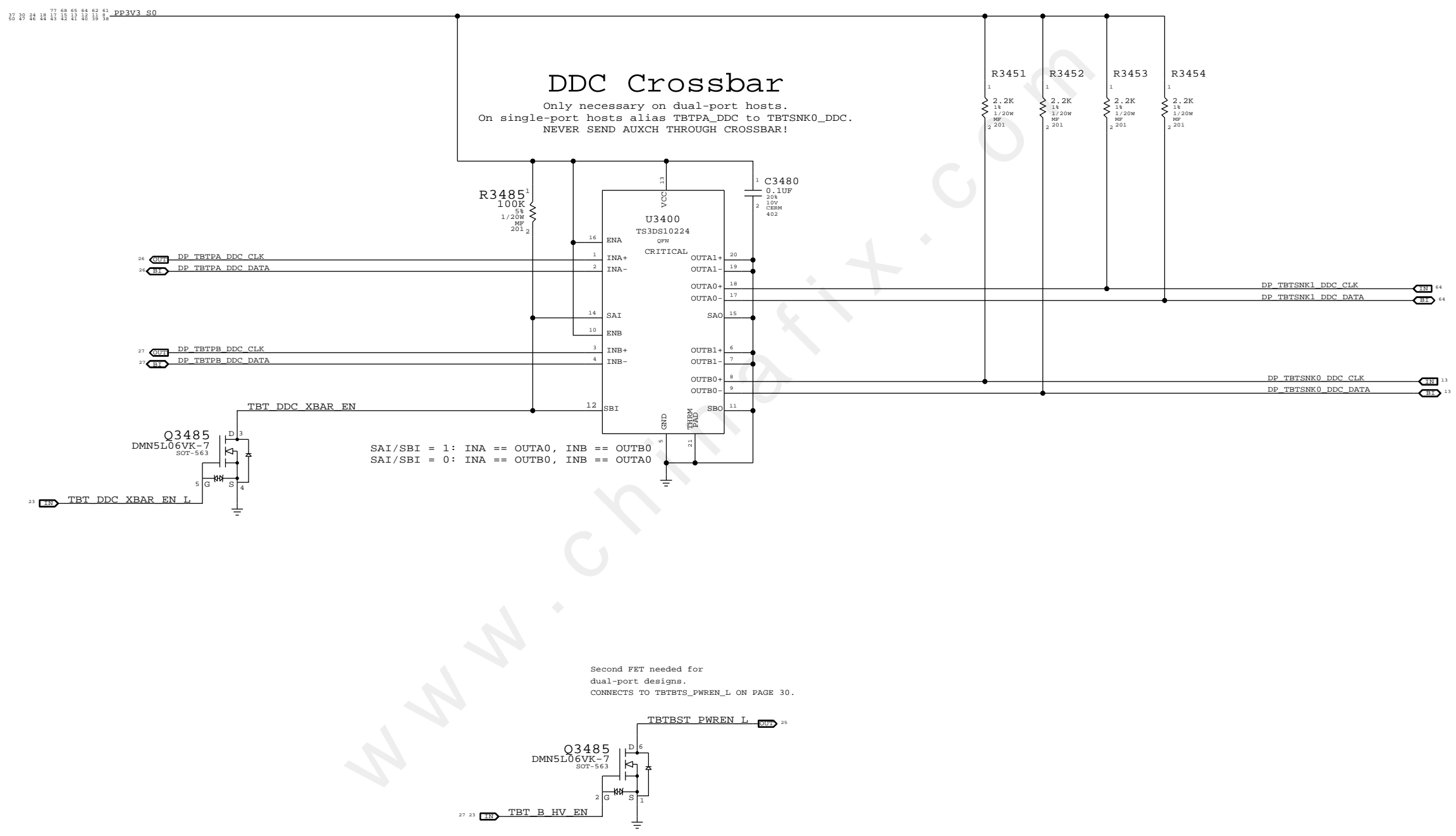
Thunderbolt Connector B

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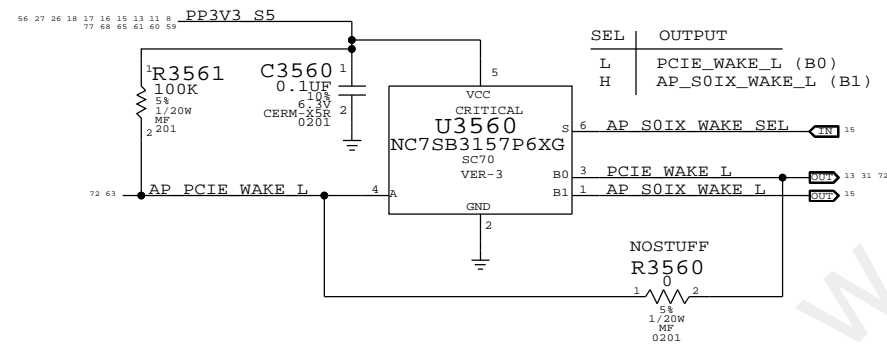
### DDC Pull-Ups

2.2k pull-ups are required by PCH to indicate active display interface.  
 DP++ spec violation, should remove!  
 NOTE: Only DDC\_DATA is sensed, so DDC\_CLK pull-ups are unstuffed.

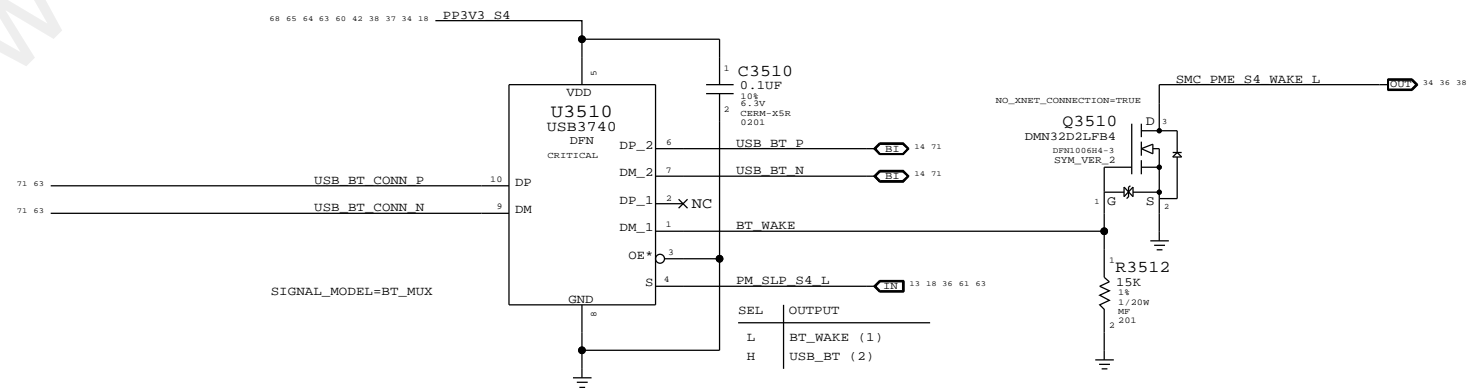


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DDC Crossbar			
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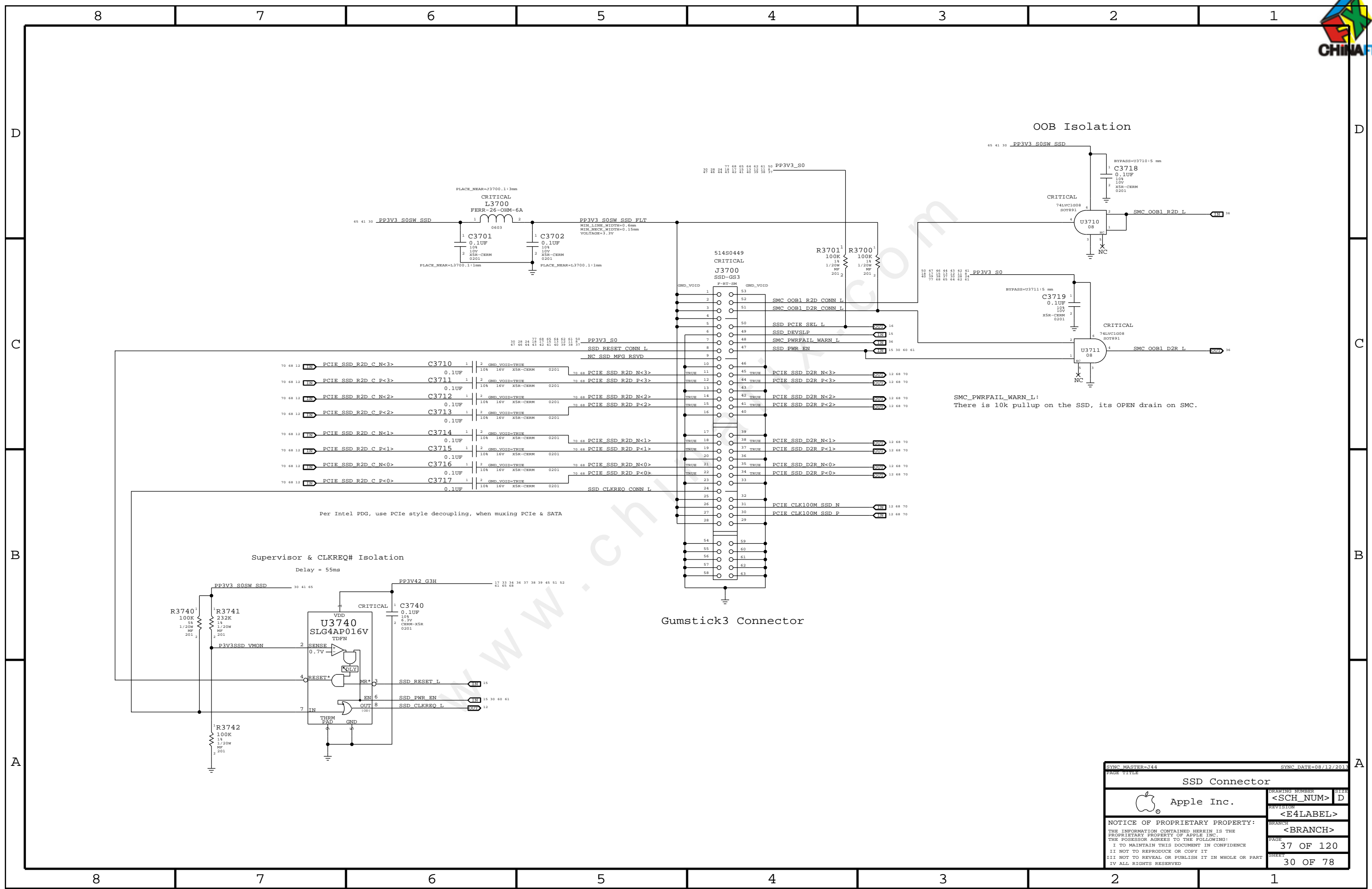
### PCIe Wake Muxing



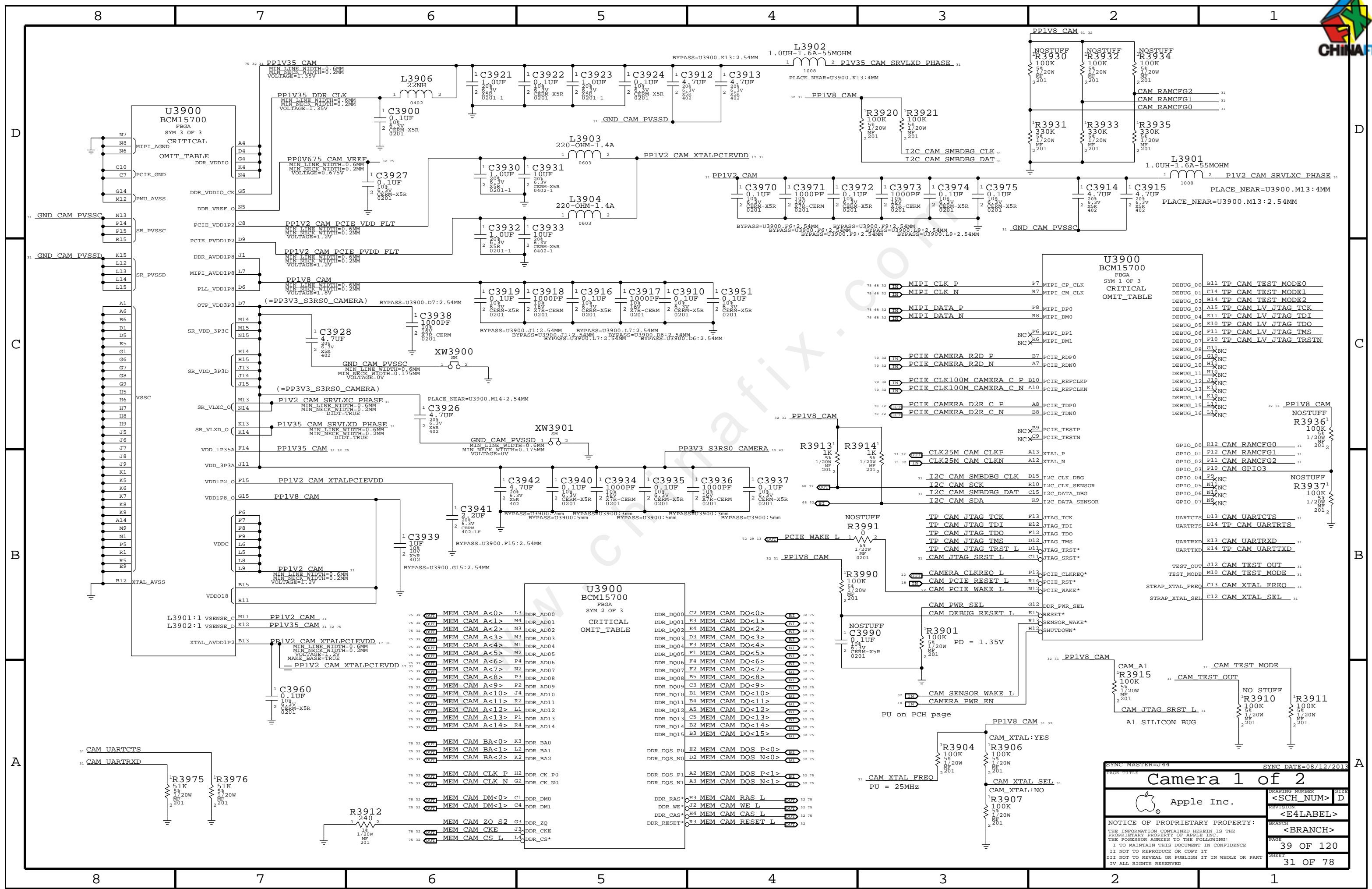
### BLUETOOTH



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<b>SSD Connector</b>			
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Camera 1 of 2

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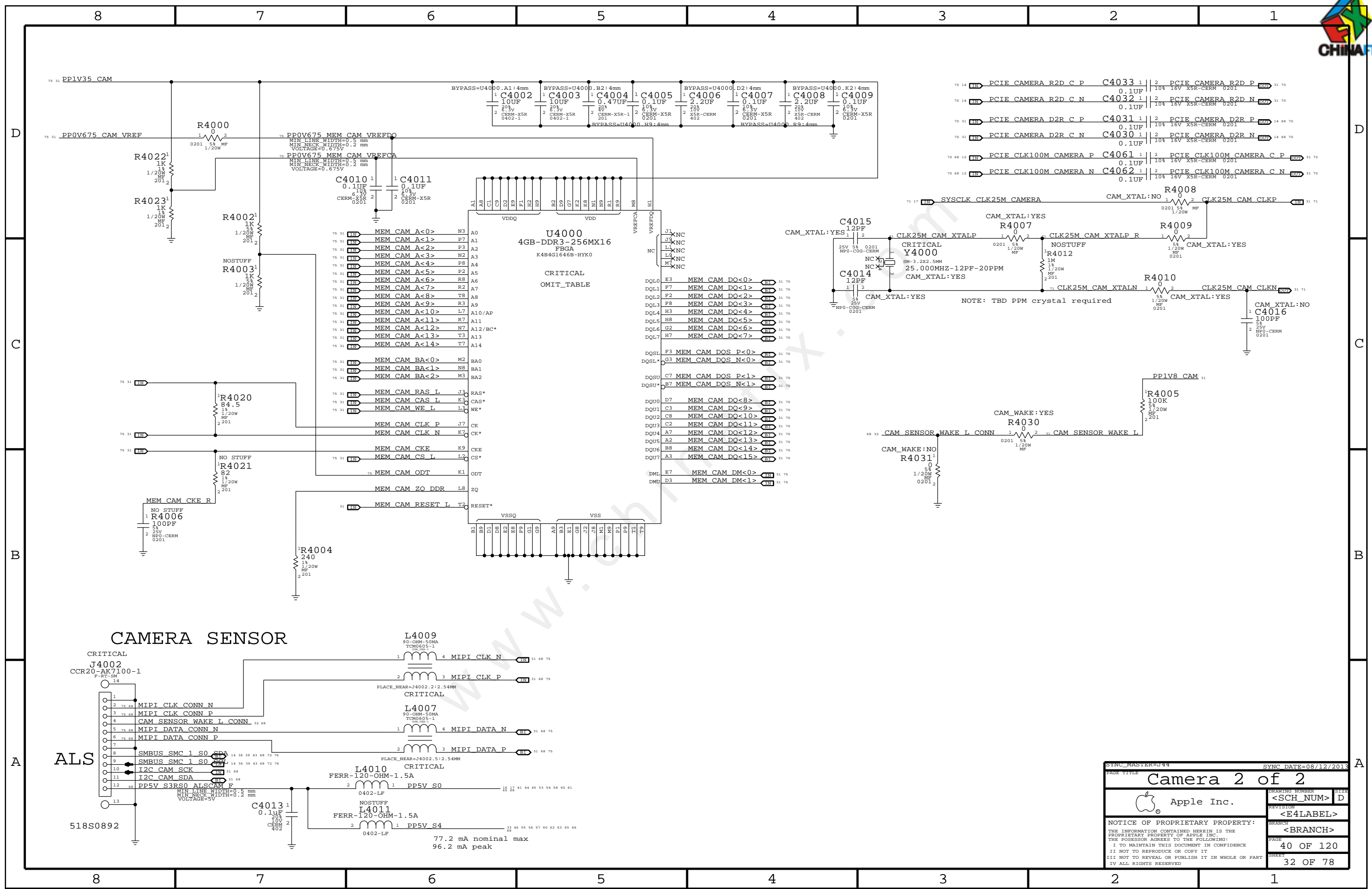
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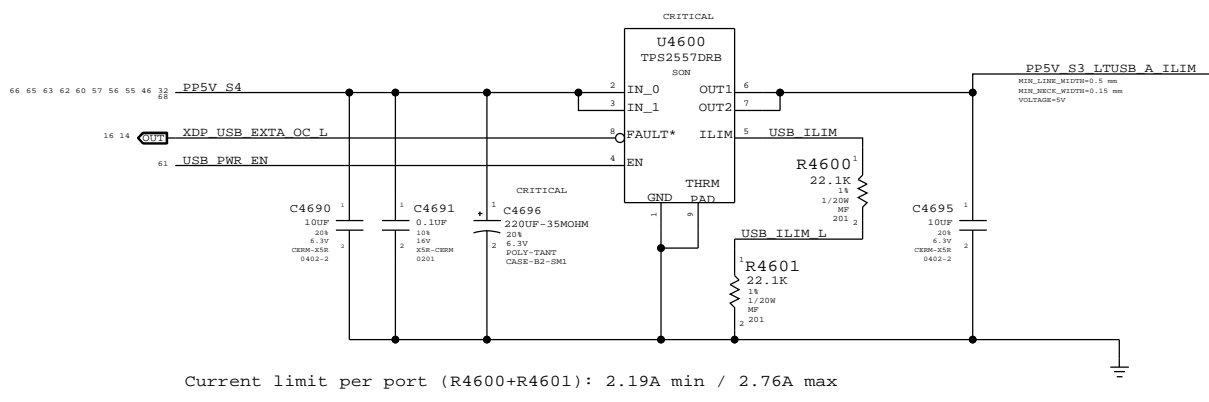


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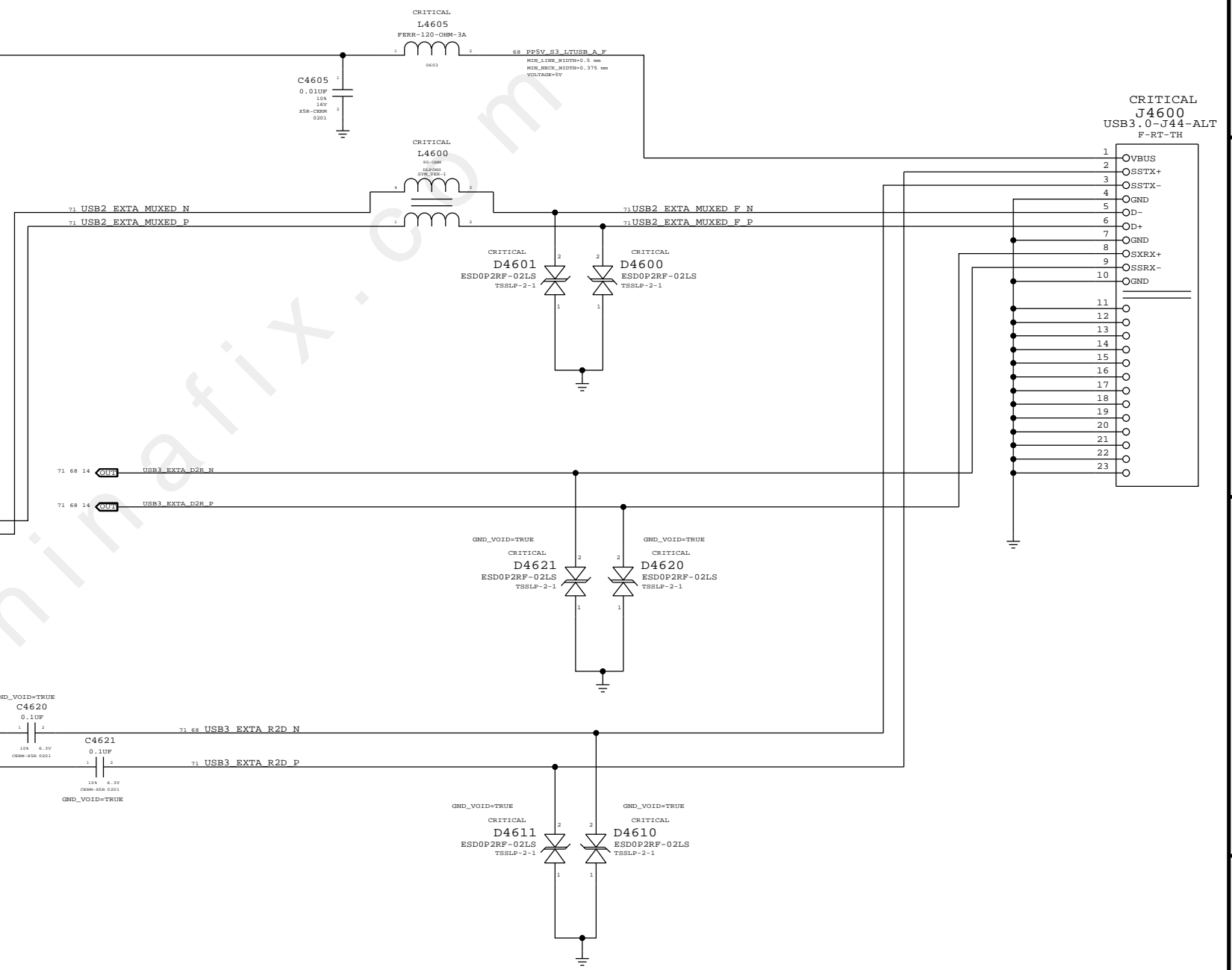
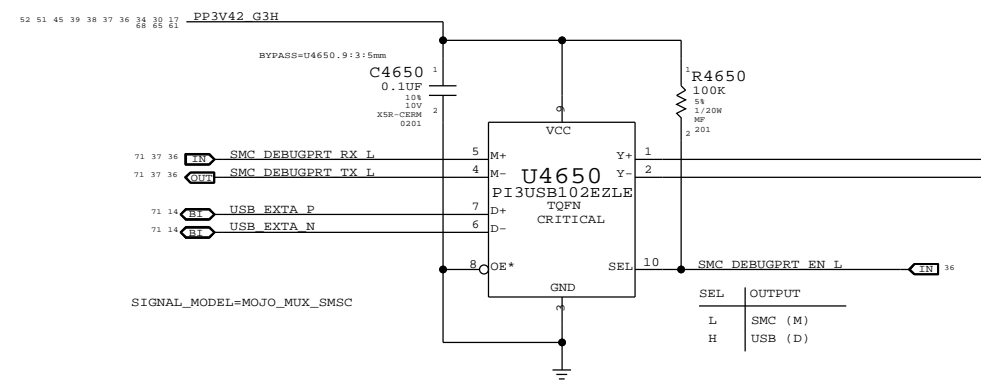
RIGHT USB PORT A

USB Port Power Switch



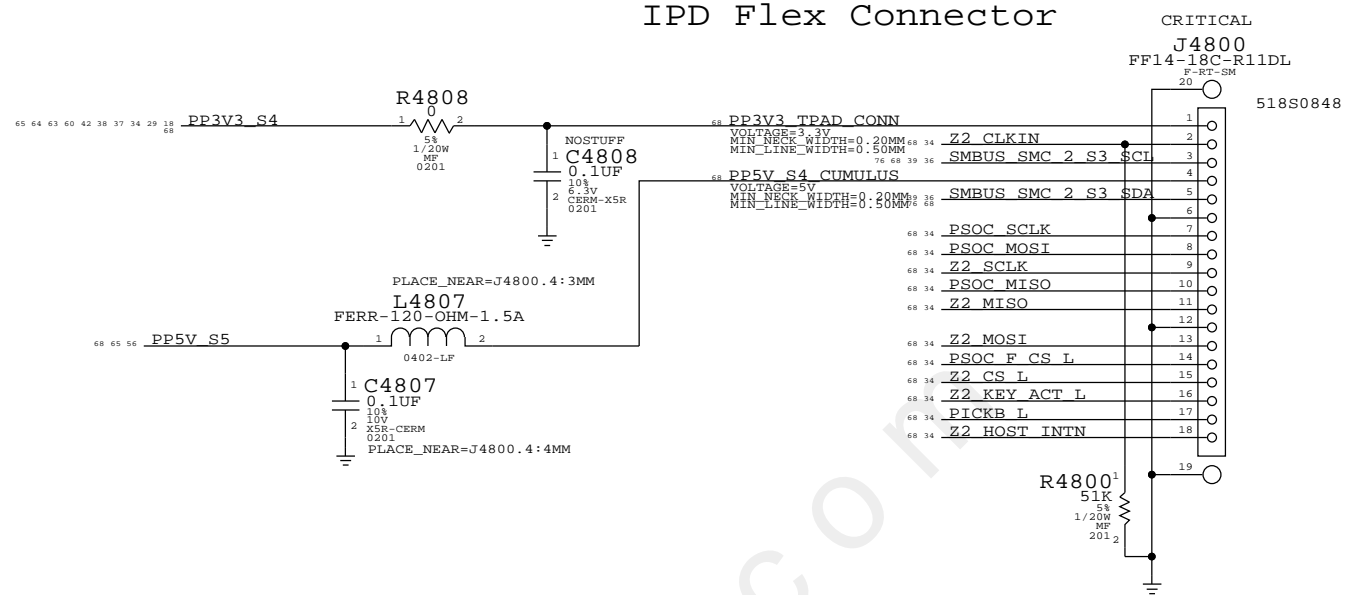
Mojo SMC Debug Mux

THE PI3USB102E CAN CLAMP VOLTAGE IN THE INTERNAL USB PINS

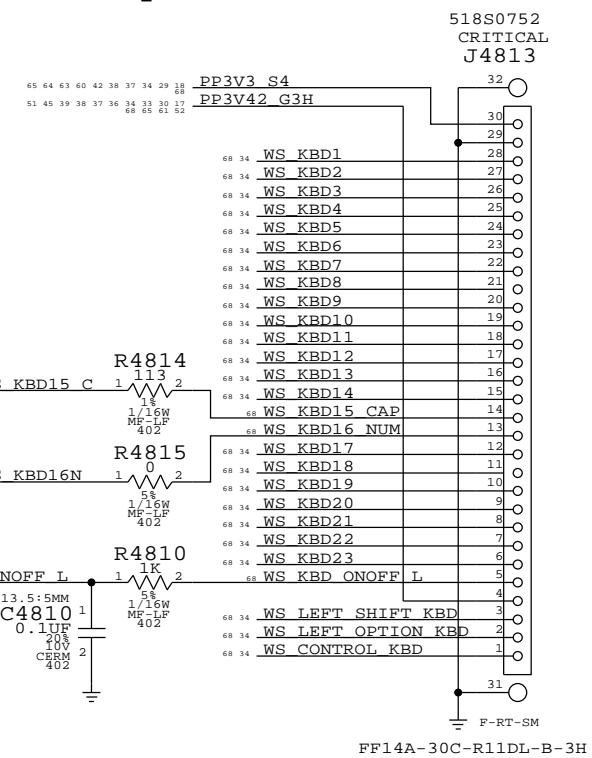


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### IPD Flex Connector

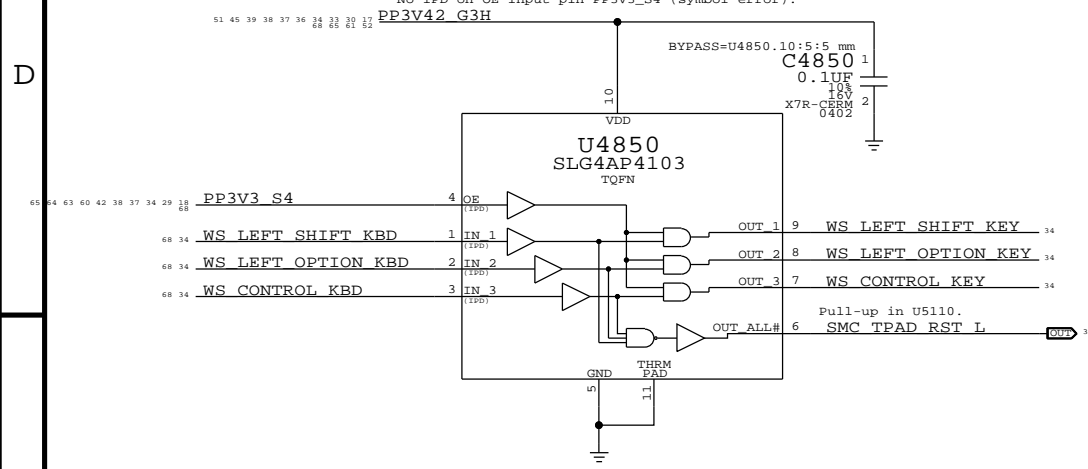


### Keyboard Connector



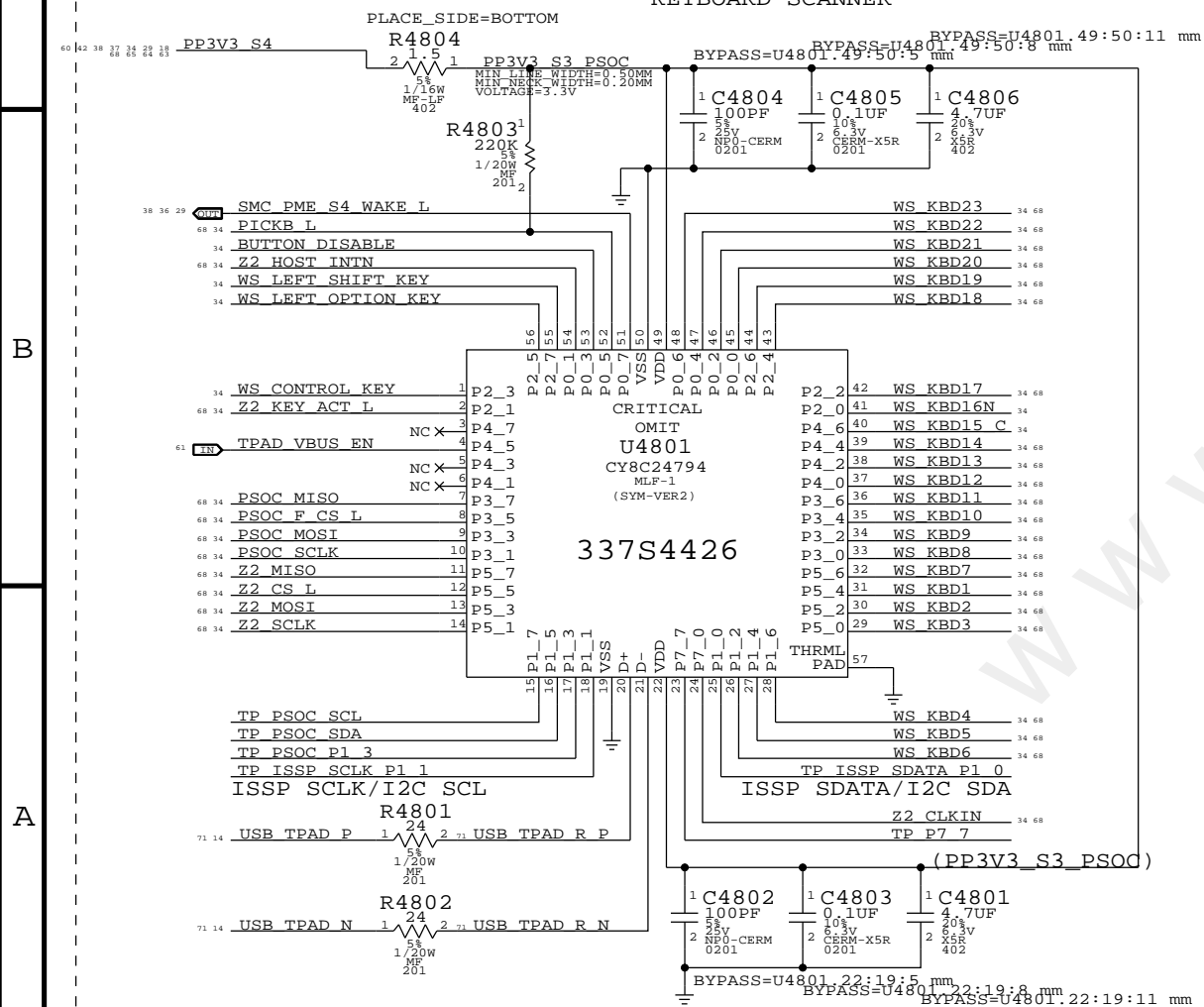
### SMC Manual Reset & Isolation

Left shift, option & control keys combined with power button cause SMC RESET# assertion.  
Keys ANDed with PSOC power to isolate when PSOC is not powered.  
No IPD on OE input pin PP3V3\_S4 (symbol error!).



### PSOC USB CONTROLLER

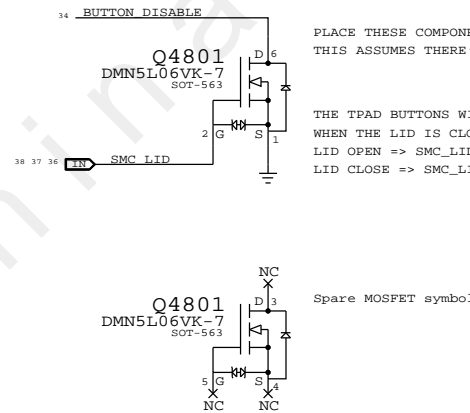
- USB INTERFACES TO MLB
- SPI HOST TO Z2
- TRACKPAD PICK BUTTONS
- KEYBOARD SCANNER



### TPAD Buttons Disable

PLACE THESE COMPONENTS CLOSE TO J4800  
THIS ASSUMES THERE'S A PP3V42\_G3H PULL UP ON MLB

THE TPAD BUTTONS WILL BE DISABLE WHEN THE LID IS CLOSED  
LID OPEN => SMC\_LID\_LC ~ 3.42V  
LID CLOSE => SMC\_LID\_LC < 0.50V



IC	PIN	NAME	CURRENT	R_SNS	V_SNS	POWER
TMP102	V+		100A	2.55 KOHM	0.255 V	0.255E-6 W
			800A		0.204 V	16.32E-6 W
			60MA (MAX)	10 OHM	0.6 V	36E-3 W
3V3 LDO	VDD		60MA (MAX)	0.2 OHM	0.012 V	0.72E-3 W
	VOUT		8MA (TYP)	1.5 OHM	0.012 V	96E-6 W
PSOC	VDD		14MA (MAX)		0.021 V	294E-6 W
	VIN		4MA (MAX)	4.7 OHM	0.0188 V	75.2E-6 W

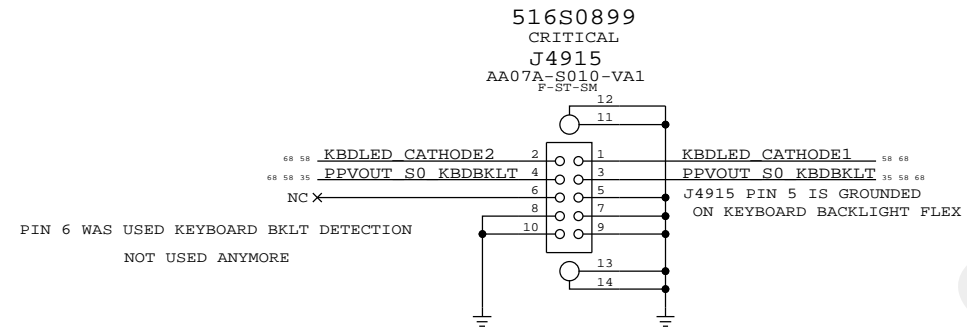
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PAGE TITLE: KEYBOARD/TRACKPAD (1 OF 2)

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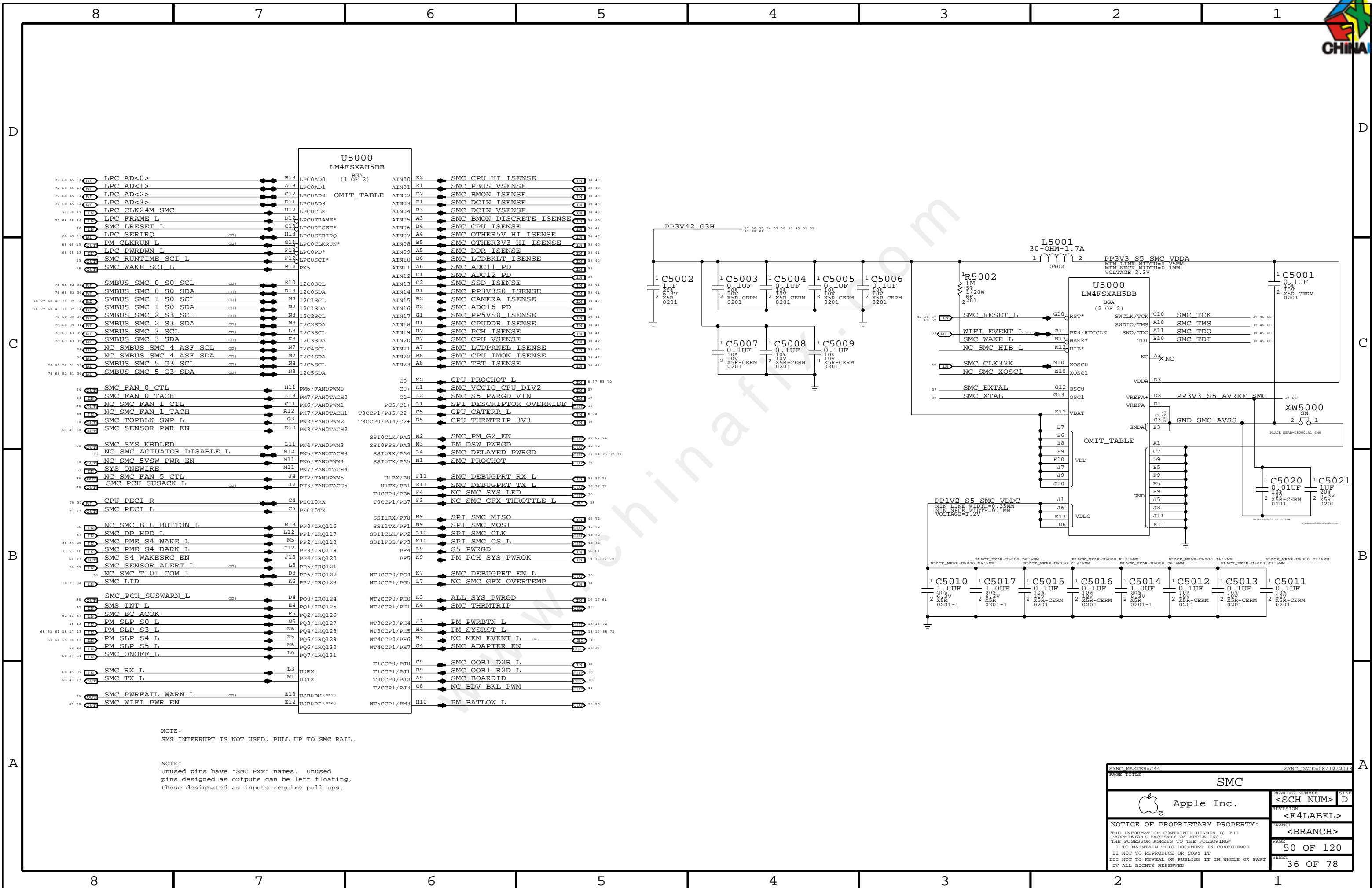
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### Keyboard Backlight Connector



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PAGE TITLE KEYBOARD/TRACKPAD (2 OF 2)			
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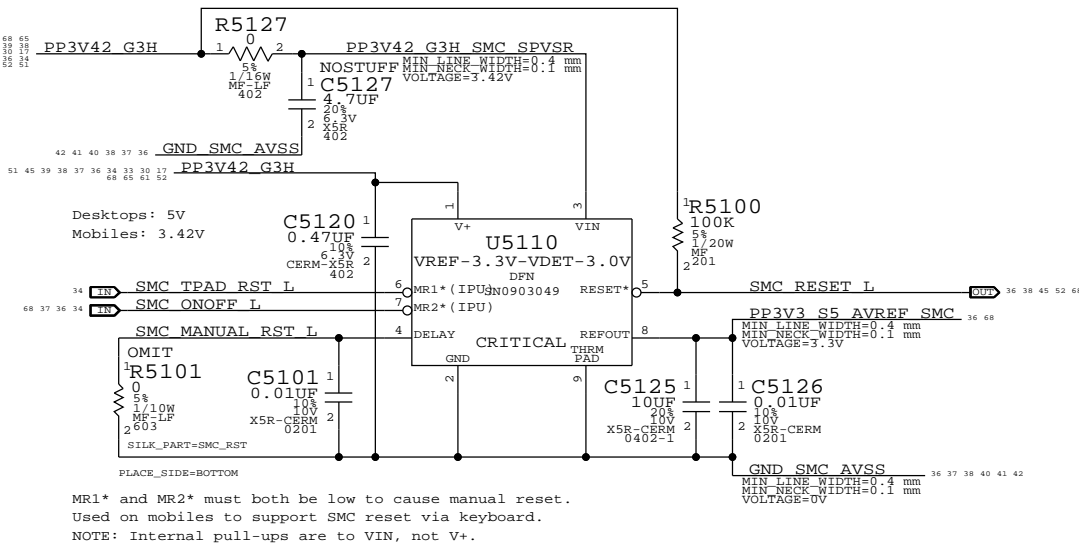
NOTE:  
SMS INTERRUPT IS NOT USED, PULL UP TO SMC RAIL.

NOTE:  
Unused pins have "SMC\_Pxx" names. Unused pins designed as outputs can be left floating, those designated as inputs require pull-ups.

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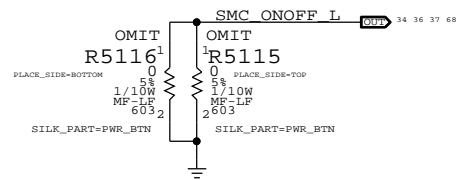


### SMC Reset "Button", Supervisor & AVREF Supply



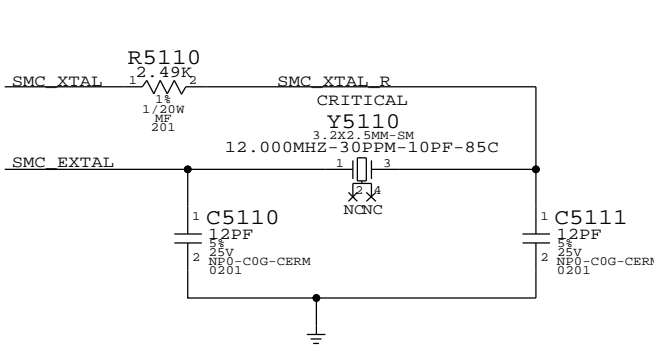
MR1\* and MR2\* must both be low to cause manual reset.  
Used on mobiles to support SMC reset via keyboard.  
NOTE: Internal pull-ups are to VIN, not V+.

### Debug Power "Buttons"

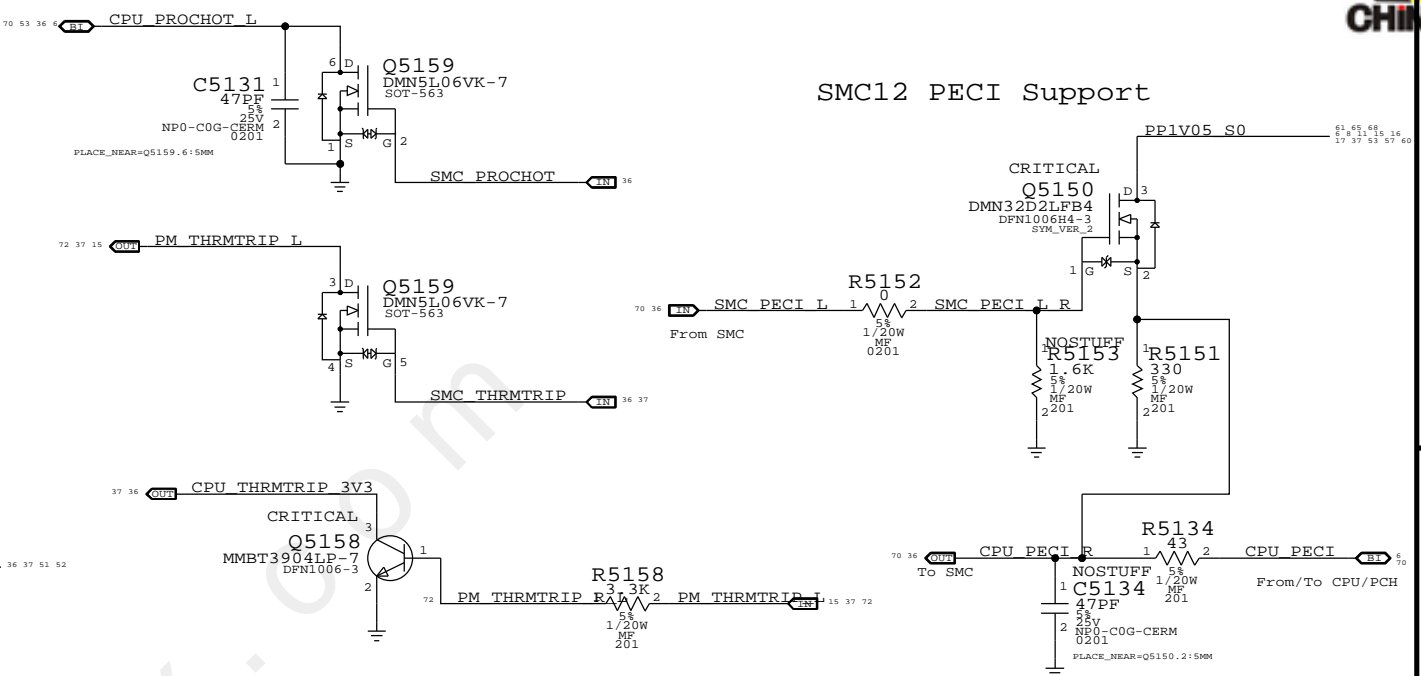


### SMC Crystal Circuit

SMC USB Clock require these crystal values: 5, 6, 8, 10, 12, 16, 18, 20, 24, 25 Mhz



### SMC12 PECI Support



SMC BC ACOK == SMC BC ACOK MAKE\_BASE=TRUE

SMC PME S4 DARK L == SMC PME S4 DARK L MAKE\_BASE=TRUE

PM CLK32K SUSCLK R1 == SMC CLK32K MAKE\_NEAR=10550\_A615\_1mm

51 45 39 38 37 36 34 33 30 17	PP3V42 G3H		
68 65 64 63 60 42 38 34 29 18	PP3V3 S4		
30 29 28 18 17 16 15 14 13 10 10 10 9 8	PP3V3 S0		
37 36 23 18	SMC PME S4 DARK L	R5167	100K 1 2 5% 1/20W MF 201
36	SMC DP HPD L	R5168	100K 1 2 5% 1/20W MF 201
68 37 36 34	SMC ONOFF L	R5170	10K 1 2 5% 1/20W MF 201
38 36	SMC SENSOR ALERT L	R5172	10K 1 2 5% 1/20W MF 201
38 36 34	SMC LID	R5171	100K 1 2 5% 1/20W MF 201
68 45 36	SMC TX L	R5173	10K 1 2 5% 1/20W MF 201
68 45 36	SMC RX L	R5174	100K 1 2 5% 1/20W MF 201
71 36 33	SMC DEBUGPRT TX L	R5175	20K 1 2 5% 1/20W MF 201
71 36 33	SMC DEBUGPRT RX L	R5176	20K 1 2 5% 1/20W MF 201
68 45 36	SMC TMS	R5177	10K 1 2 5% 1/20W MF 201
68 45 36	SMC TDO	R5178	10K 1 2 5% 1/20W MF 201
68 45 36	SMC TDI	R5179	10K 1 2 5% 1/20W MF 201
68 45 36	SMC TCK	R5180	10K 1 2 5% 1/20W MF 201
52 51 37 36	SMC BC ACOK	R5187	100K 1 2 5% 1/20W MF 201
36	SMC S5 PWRGD VIN	R5192	100K 1 2 5% 1/20W MF 201
36	SMS INT L	R5193	10K 1 2 5% 1/20W MF 201
37 36	CPU THRMTRIP 3V3	R5117	100K 1 2 5% 1/20W MF 201
68 45	SMC ROMBOOT		
61 56 36	SMC PM G2 EN	R5198	100K 1 2 5% 1/20W MF 201
36 13	SMC ADAPTER EN	R5185	10K 1 2 5% 1/20W MF 201
37 36	SMC THRMTRIP	R5186	10K 1 2 5% 1/20W MF 201
72 36 25 24 17	SMC DELAYED PWRGD	R5191	100K 1 2 5% 1/20W MF 201
61 36	SMC S4 WAKESRC EN	R5190	100K 1 2 5% 1/20W MF 201

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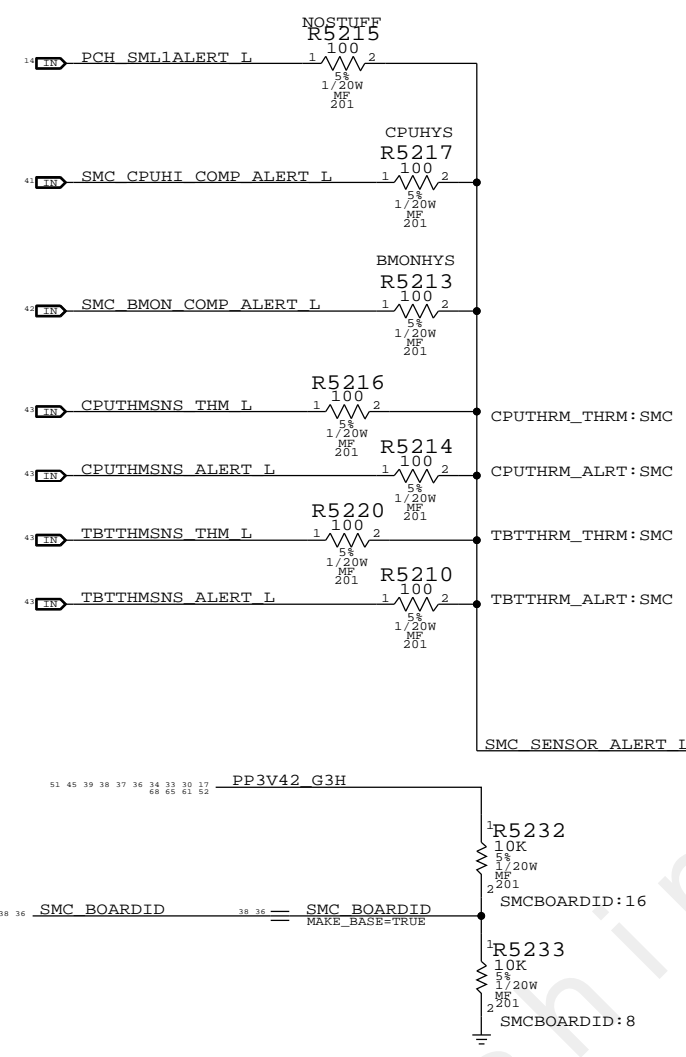


8 7 6 5 4 3 2 1

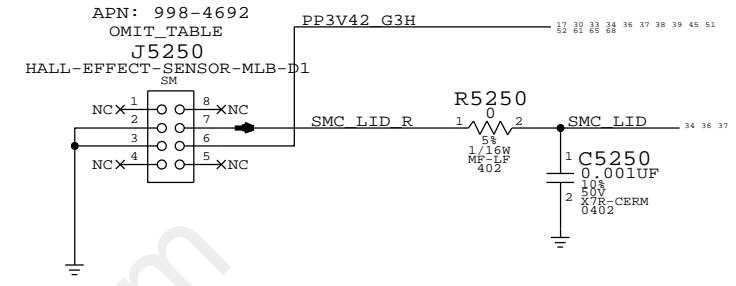
### SMC12 ADC Assignments

40 38 36	SMC CPU HI ISENSE	=	SMC CPU HI ISENSE	36 38 40
40 38 36	SMC PBUS VSENSE	=	SMC PBUS VSENSE	36 38 40
40 38 36	SMC BMON ISENSE	=	SMC BMON ISENSE	36 38 40
40 38 36	SMC DCIN ISENSE	=	SMC DCIN ISENSE	36 38 40
40 38 36	SMC DCIN VSENSE	=	SMC DCIN VSENSE	36 38 40
40 38 36	SMC BMON DISCRETE ISENSE	=	SMC BMON DISCRETE ISENSE	36 38 42
41 38 36	SMC CPU ISENSE	=	SMC CPU ISENSE	36 38 41
40 38 36	SMC OTHER5V HI ISENSE	=	SMC OTHER5V HI ISENSE	36 38 40
40 38 36	SMC OTHER3V3 HI ISENSE	=	SMC OTHER3V3 HI ISENSE	36 38 40
41 38 36	SMC DDR ISENSE	=	SMC DDR ISENSE	36 38 41
40 38 36	SMC LCDBKLT ISENSE	=	SMC LCDBKLT ISENSE	36 38 40
38 36	SMC ADC11 PD	=	SMC ADC11 PD	36 38
38 36	SMC ADC12 PD	=	SMC ADC12 PD	36 38
41 38 36	SMC SSD ISENSE	=	SMC SSD ISENSE	36 38 41
41 38 36	SMC PP3V3S0 ISENSE	=	SMC PP3V3S0 ISENSE	36 38 41
42 38 36	SMC CAMERA ISENSE	=	SMC CAMERA ISENSE	36 38 42
38 36	SMC ADC16 PD	=	SMC ADC16 PD	36 38
41 38 36	SMC PP5V50 ISENSE	=	SMC PP5V50 ISENSE	36 38 41
41 38 36	SMC CPUDDR ISENSE	=	SMC CPUDDR ISENSE	36 38 41
41 38 36	SMC PCH ISENSE	=	SMC PCH ISENSE	36 38 41
42 38 36	SMC CPU VSENSE	=	SMC CPU VSENSE	36 38 42
42 38 36	SMC LCDPANEL ISENSE	=	SMC LCDPANEL ISENSE	36 38 42
42 38 36	SMC CPU IMON ISENSE	=	SMC CPU IMON ISENSE	36 38 42
42 38 36	SMC TBT ISENSE	=	SMC TBT ISENSE	36 38 42

### Thermal Alerts



### Hall Effect Pads



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
677-0912	1	SUBASSY,PCBA HALL EFFECT,J44	J5250	CRITICAL	
639-4502 (J44 HALL EFFECT BOARD) REPORTS TO 677-0912					

Specify one of these BOM GROUPS.

BOM GROUP	BOM OPTIONS
CPUTHRM: BOTH	CPUTHRM_THRM: SMC, CPUTHRM_ALERT: SMC
CPUTHRM: THRM	CPUTHRM_THRM: SMC, CPUTHRM_ALERT: PU
CPUTHRM: ALERT	CPUTHRM_THRM: PU, CPUTHRM_ALERT: SMC
CPUTHRM: NONE	CPUTHRM_THRM: PU, CPUTHRM_ALERT: PU

Specify one of these BOM GROUPS.

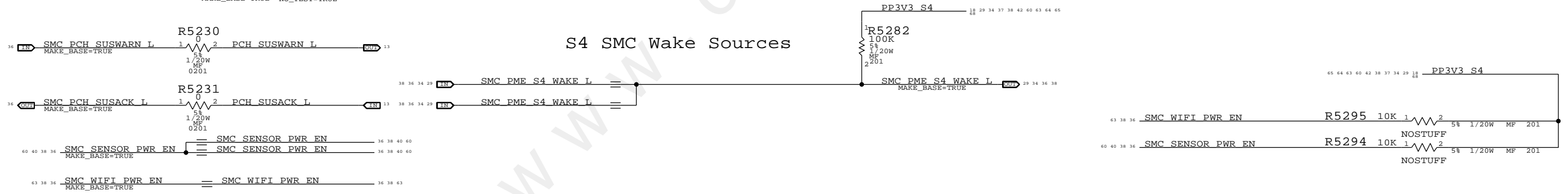
BOM GROUP	BOM OPTIONS
TBTHRM: BOTH	TBTHRM_THRM: SMC, TBTHRM_ALERT: SMC
TBTHRM: THRM	TBTHRM_THRM: SMC, TBTHRM_ALERT: PU
TBTHRM: ALERT	TBTHRM_THRM: PU, TBTHRM_ALERT: SMC
TBTHRM: NONE	TBTHRM_THRM: PU, TBTHRM_ALERT: PU
TBTHRM: GONE	

Requires EM1412-1 or EM1412-2 instead of EM1412-A, new APN needs to be created.

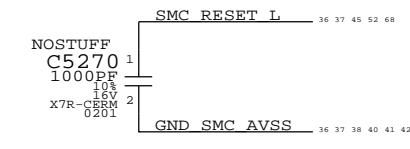
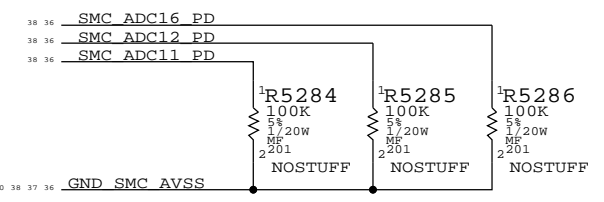
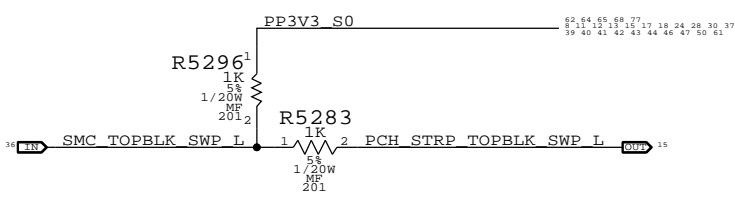
### SMC12 Pin Assignments

38 36	NC SMBUS SMC 4 ASF SCL	=	NC SMBUS SMC 4 ASF SCL	36 38
38 36	NC SMBUS SMC 4 ASF SDA	=	NC SMBUS SMC 4 ASF SDA	36 38
38 36	NC BDV BKL PWM	=	NC BDV BKL PWM	36 38
38 36	NC SMC SYS LED	=	NC SMC SYS LED	36 38
38 36	NC SMC GFX THROTTLE L	=	NC SMC GFX THROTTLE L	36 38
38 36	NC SMC GFX OVERTEMP	=	NC SMC GFX OVERTEMP	36 38
38 36	NC SMC FAN 1 CTL	=	NC SMC FAN 1 CTL	36 38
38 36	NC SMC FAN 1 TACH	=	NC SMC FAN 1 TACH	36 38
38 36	NC SMC 5VSW PWR EN	=	NC SMC 5VSW PWR EN	36 38
38 36	NC SMC FAN 5 CTL	=	NC SMC FAN 5 CTL	36 38
38 36	NC SMC BIL BUTTON L	=	NC SMC BIL BUTTON L	36 38
38 36	NC MEM EVENT L	=	NC MEM EVENT L	36 38
38 36	NC SMC T101 COM 1	=	NC SMC T101 COM 1	36 38
38 36	NC SMC ACTUATOR DISABLE L	=	NC SMC ACTUATOR DISABLE L	36 38

### S4 SMC Wake Sources

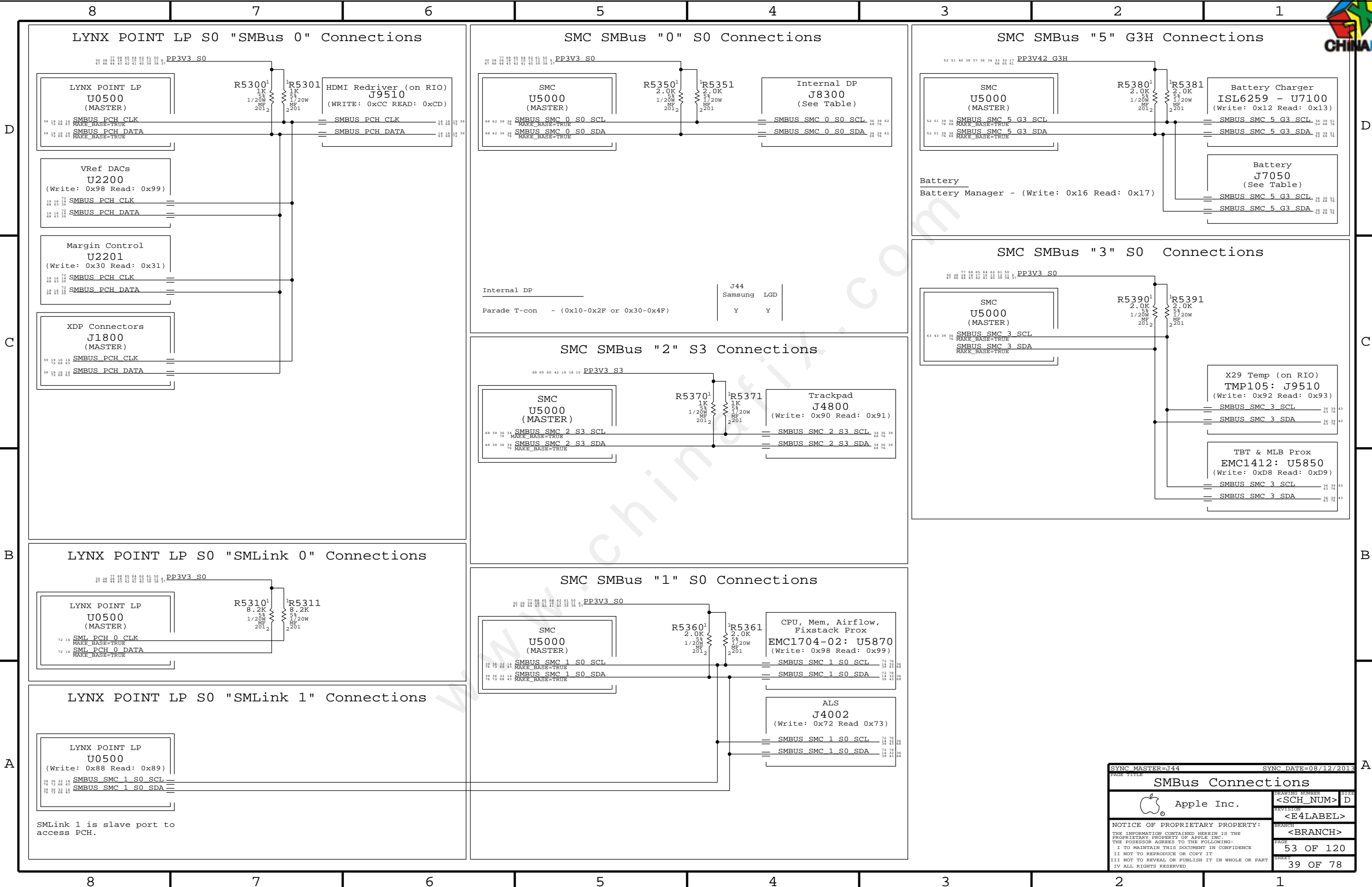


### Top Block Swap



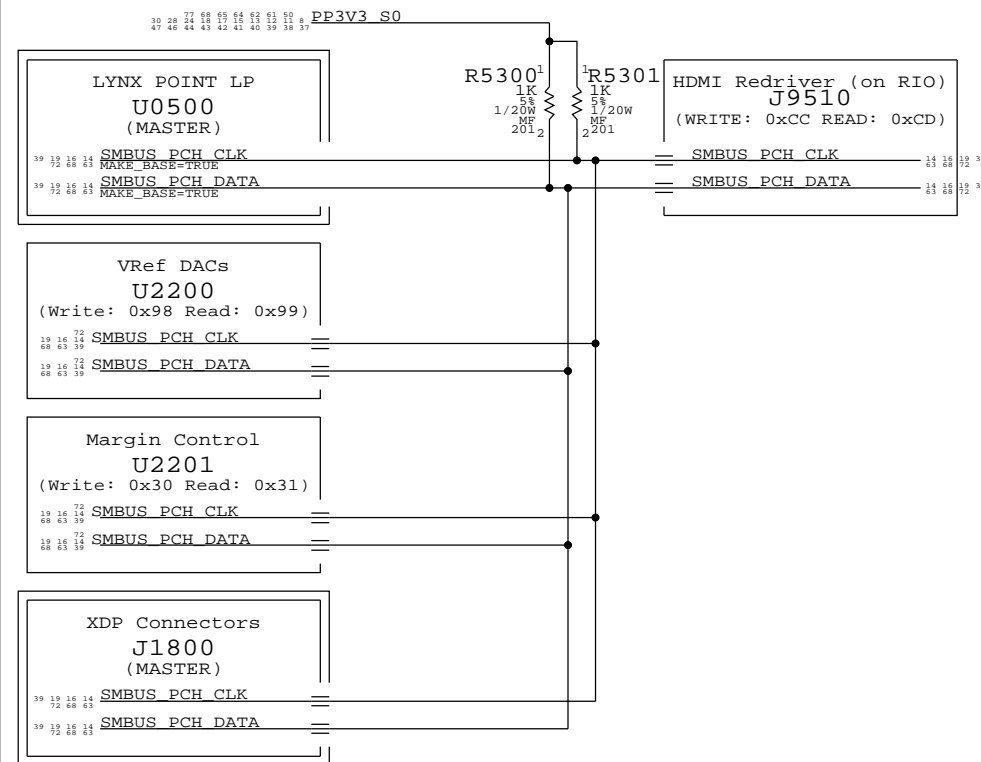
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8 7 6 5 4 3 2 1

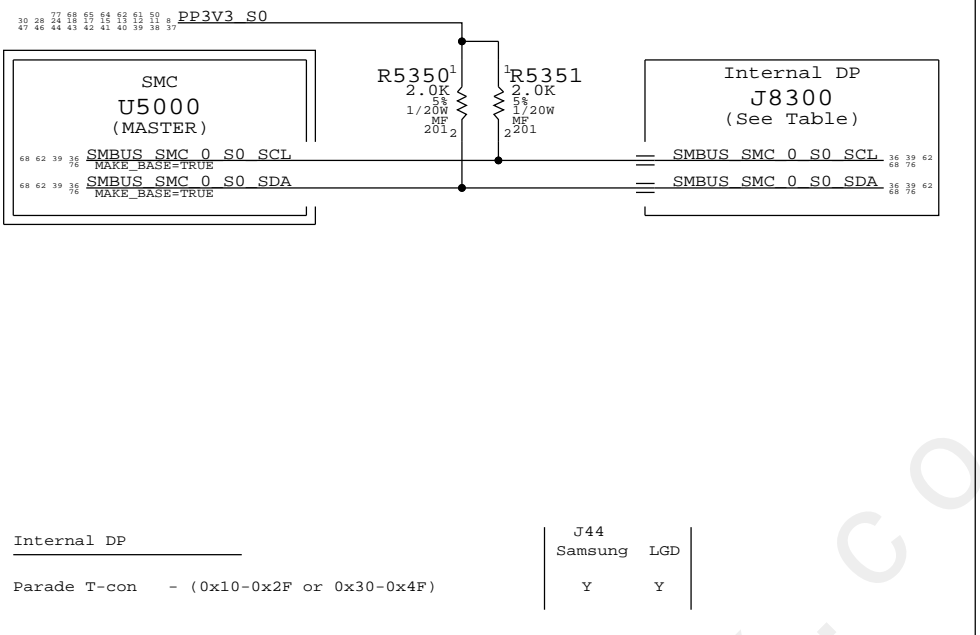


SYNC MASTER=J44		SYNC DATE=08/12/2013	
<b>SMBus Connections</b>			
Apple Inc.		DRAWING NUMBER	SIZE
		<SCH_NUM>	D
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		PAGE	53 OF 120
		SHEET	39 OF 78

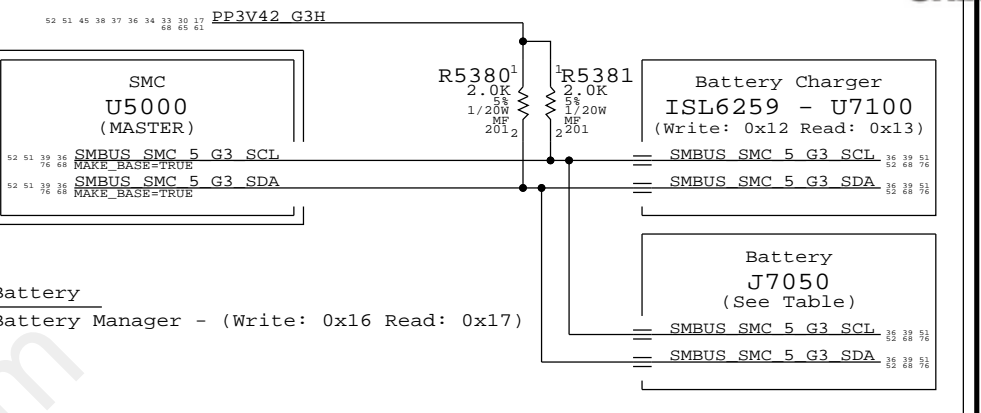
LYNX POINT LP S0 "SMBus 0" Connections



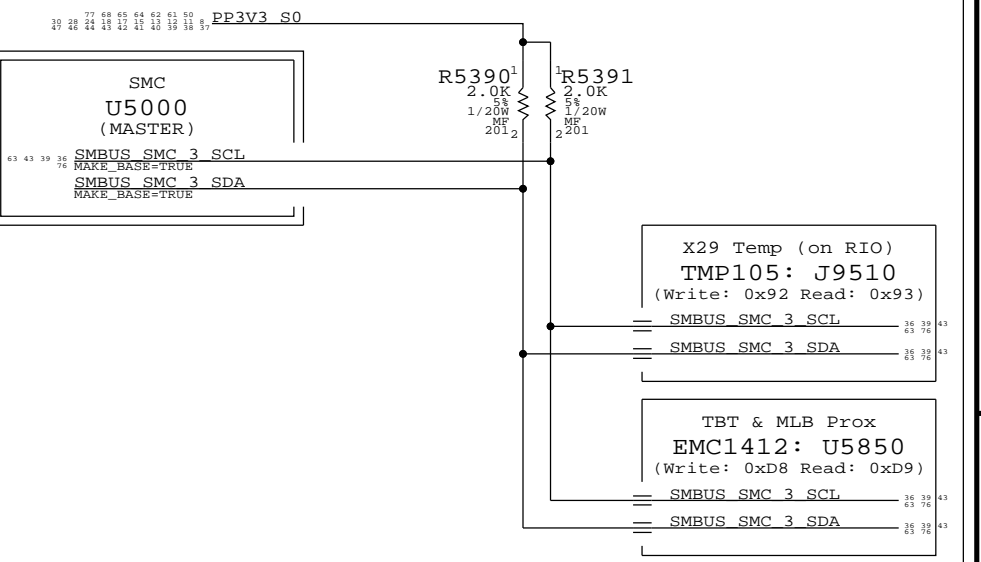
SMC SMBus "0" S0 Connections



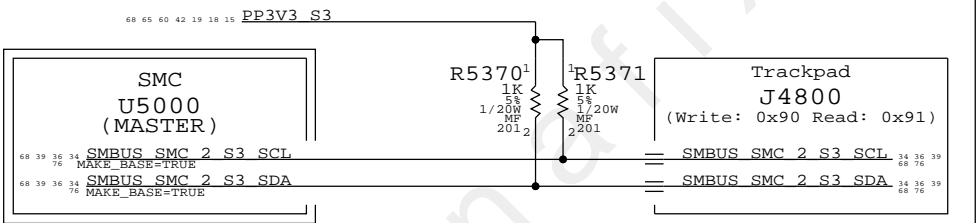
SMC SMBus "5" G3H Connections



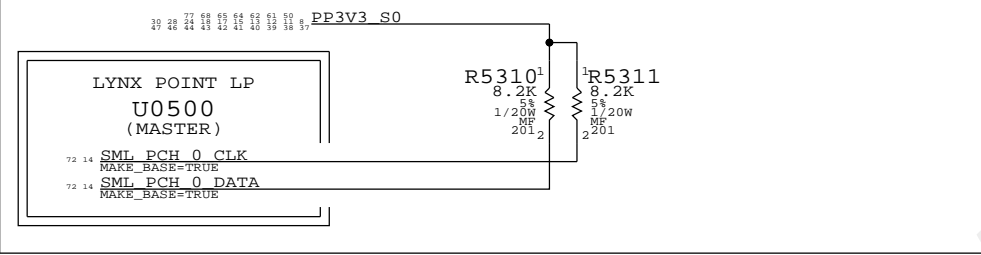
SMC SMBus "3" S0 Connections



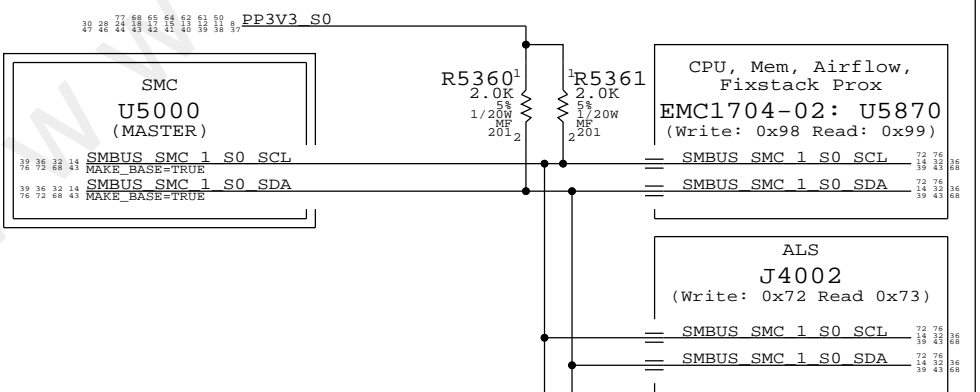
SMC SMBus "2" S3 Connections



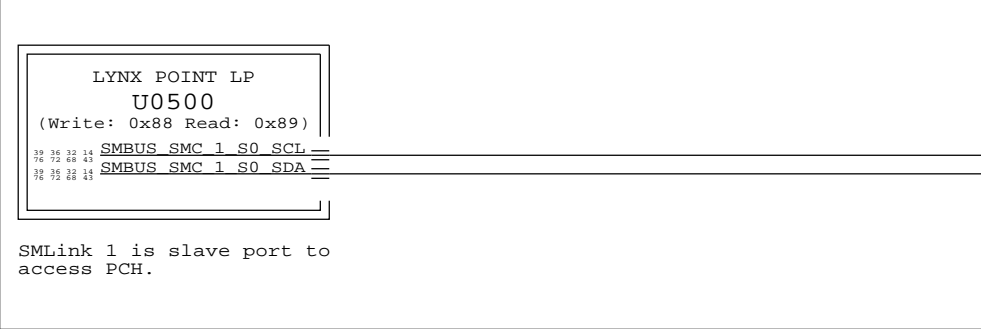
LYNX POINT LP S0 "SMLink 0" Connections



SMC SMBus "1" S0 Connections



LYNX POINT LP S0 "SMLink 1" Connections



D

C

B

A

D

C

B

A

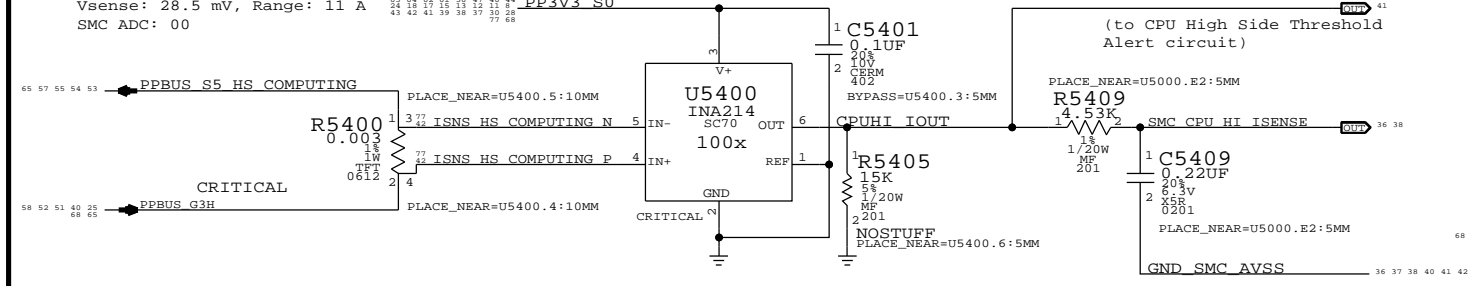
8 7 6 5 4 3 2 1

8 7 6 5 4 3 2 1



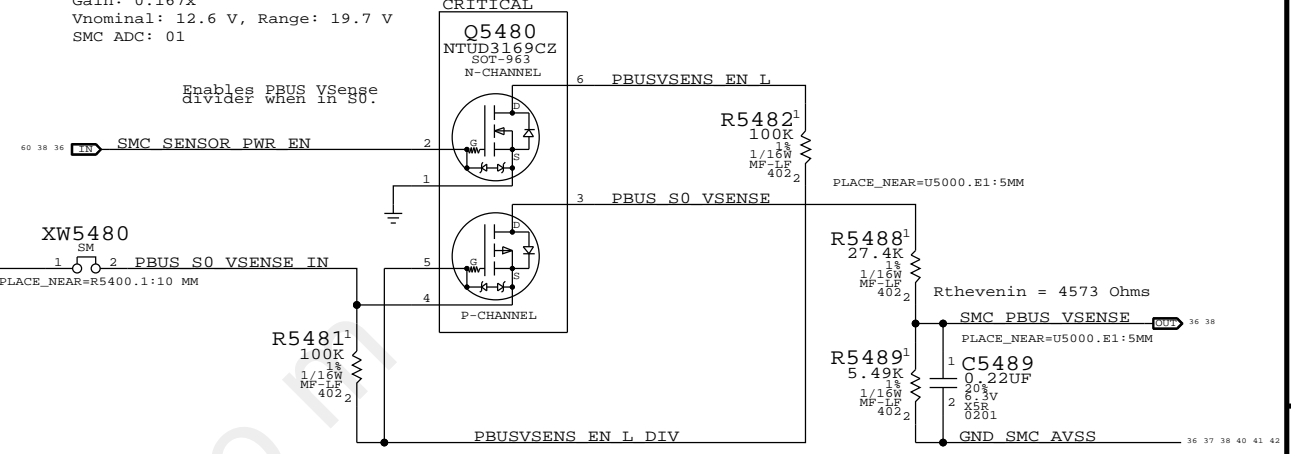
### CPU High Side Current Sense (IC0R)

Gain: 100x, EDP: 9.5 A  
 Rsense: 0.003 (R5400)  
 Vsense: 28.5 mV, Range: 11 A  
 SMC ADC: 00



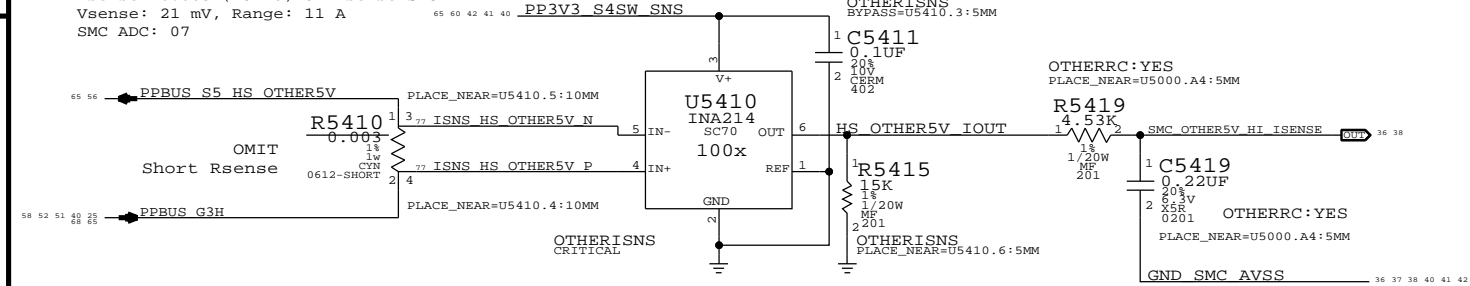
### PBUS Voltage Sense & Enable (VP0R)

Gain: 0.167x  
 Vnominal: 12.6 V, Range: 19.7 V  
 SMC ADC: 01



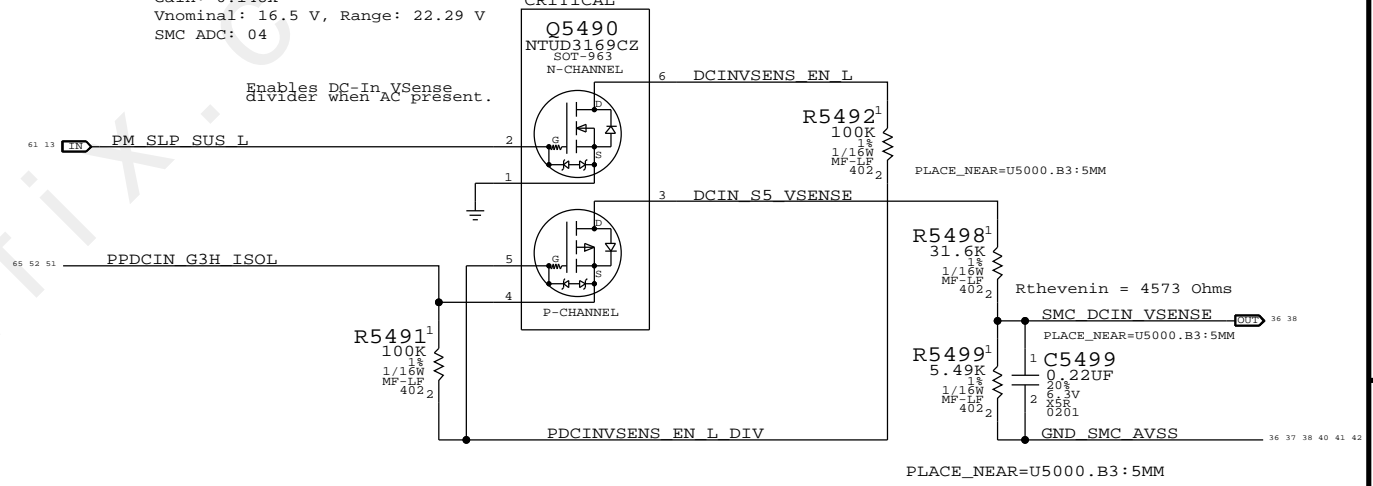
### OTHER 5V High Side Current Sense (IO5R)

Gain: 100x, EDP: 7 A  
 Rsense: 0.003 (R5410) or Rsense SHORT  
 Vsense: 21 mV, Range: 11 A  
 SMC ADC: 07



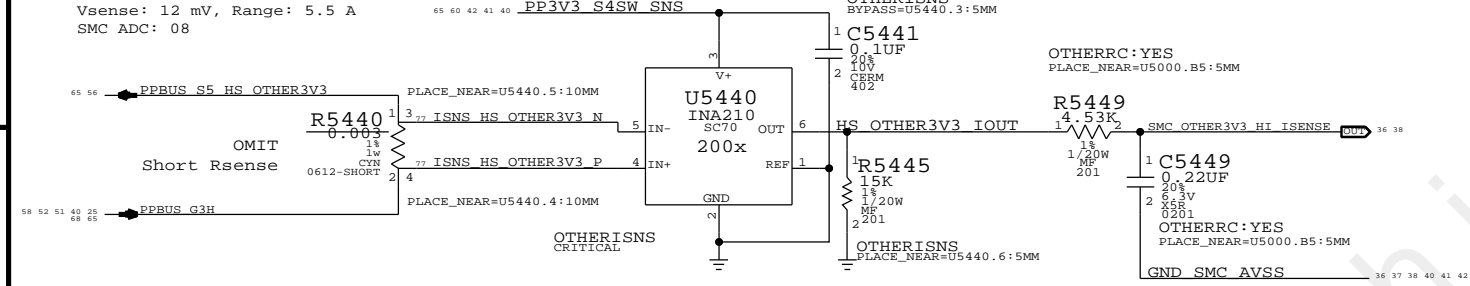
### DC In Voltage Sense & Enable (VD0R)

Gain: 0.148x  
 Vnominal: 16.5 V, Range: 22.29 V  
 SMC ADC: 04



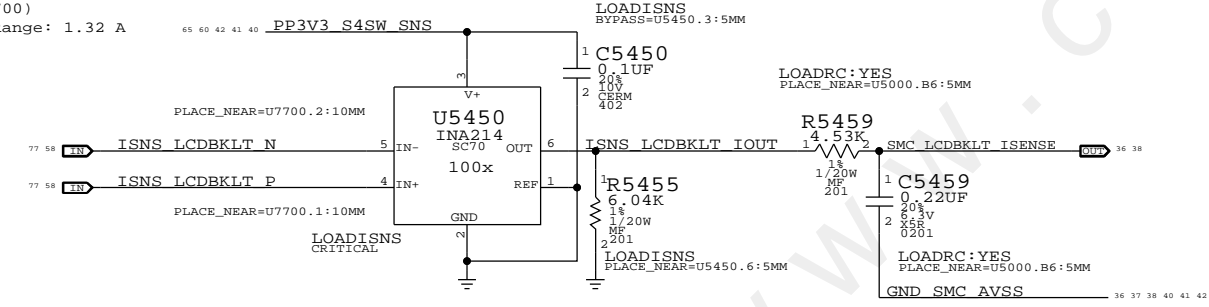
### OTHER 3.3V High Side Current Sense (IO3R)

Gain: 200x, EDP: 5 A  
 Rsense: 0.003 (R5440) or Rsense SHORT  
 Vsense: 12 mV, Range: 5.5 A  
 SMC ADC: 08



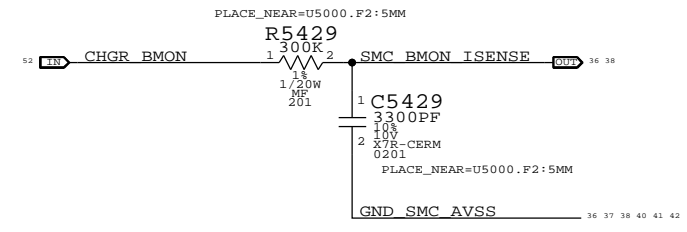
### LCD Backlight Current Sense (IBLC)

Gain: 100x, EDP: 0.9 A  
 Rsense: 0.025 (R7700)  
 Vsense: 22.5 mV, Range: 1.32 A  
 SMC AD: 10



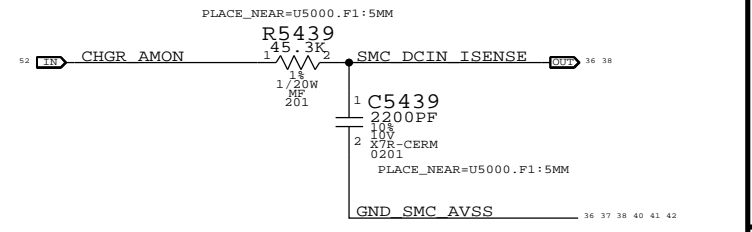
### Charger (BMON) Current Sense (IPBR)

Charger Gain: 36x, EDP: 8 A  
 Rsense: 0.005 (R7150)  
 SMC ADC: 02



### DC-IN (AMON) Current Sense (ID0R)

Charger Gain: 20x, EDP: 4.6 A  
 Rsense: 0.020 (R7120)  
 SMC ADC: 03



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
117S0008	1	RES,MTL,FLIM,100K,1/16W,0201,SMD,LF	C5419,C5449	CRITICAL	OTHERRC:NO
117S0008	1	RES,MTL,FLIM,100K,1/16W,0201,SMD,LF	C5459		LOADRC:NO

SYNC MASTER=J44 SYNC DATE=08/12/2013

**Power Sensors: High Side**

Apple Inc.

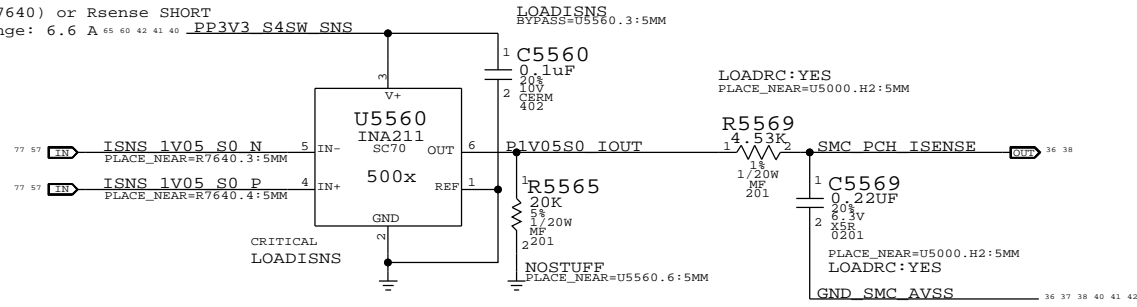
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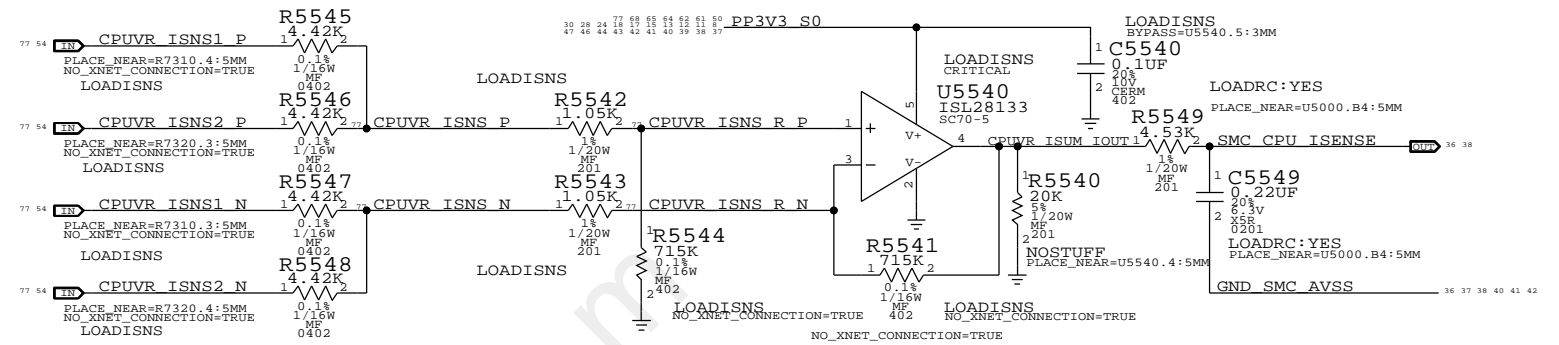
### PCH 1.05V Current Sense (IC1C)

Gain: 500x, EDP: 5 A  
 Rsense: 0.001 (R7640) or Rsense SHORT  
 Vsense: 5 mV, Range: 6.6 A  
 SMC ADC: 19



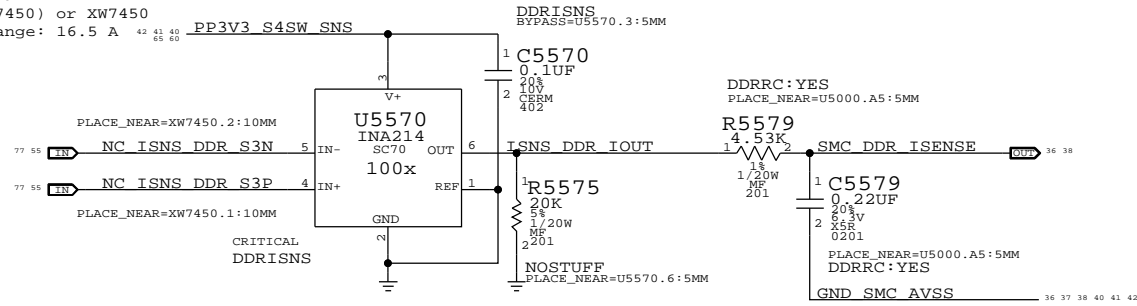
### CPU Fixed Current Sense (IC0C)

Gain: 219.33x, EDP: 40 A  
 Rsense: 2x of 0.00075 (R7310, R7320), Rsum: 0.000375  
 Vsense: 15 mV, Range: 40.12 A  
 SMC ADC: 06



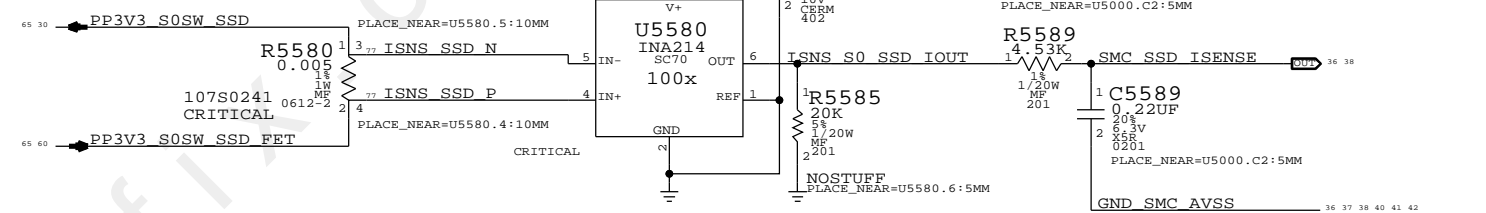
### DDR 1.35V S3 (CPU & Memory) Current Sense (IM0C)

Gain: 100x, EDP: 9 A  
 Rsense: 0.002 (R7450) or XW7450  
 Vsense: 21 mV, Range: 16.5 A  
 SMC ADC: 09



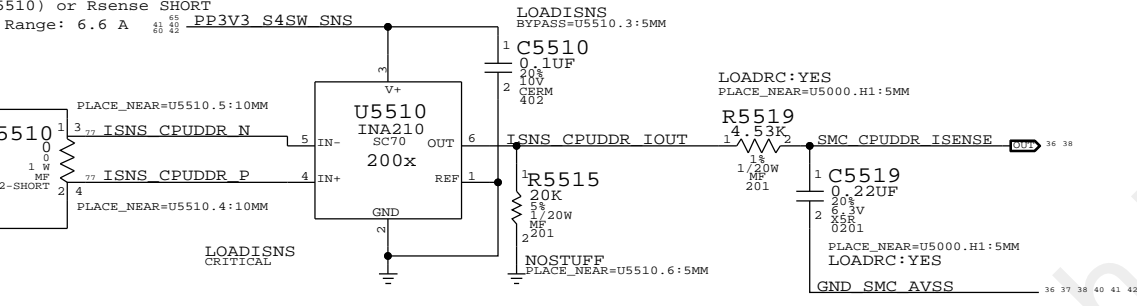
### SSD Current Sense (ISDC)

Gain: 100x, EDP: 5 A (16.5 W)  
 Rsense: 0.005 (R5580)  
 Vsense: 25 mV, Range: 6.6 A  
 SMC ADC: 13



### CPU DDR 1.35V S3 (CPU Only) Current Sense (IM1C)

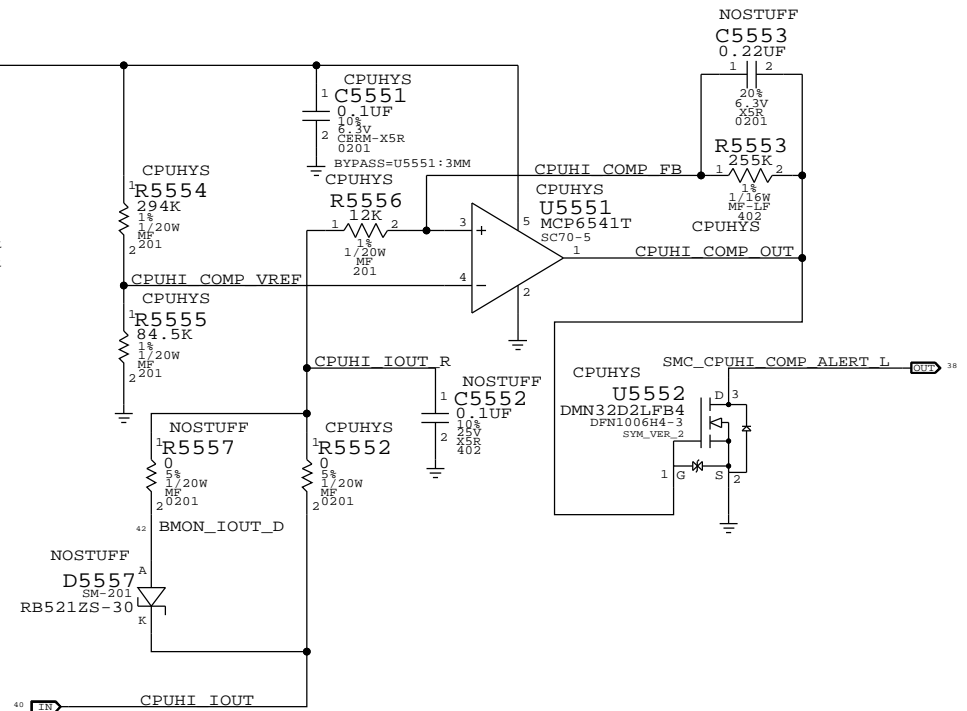
Gain: 200x, EDP: 2.5 A  
 Rsense: 0.005 (R5510) or Rsense SHORT  
 Vsense: 12.5 mV, Range: 6.6 A  
 SMC ADC: 18



### CPU High Side Current (IC0R) Threshold Alert

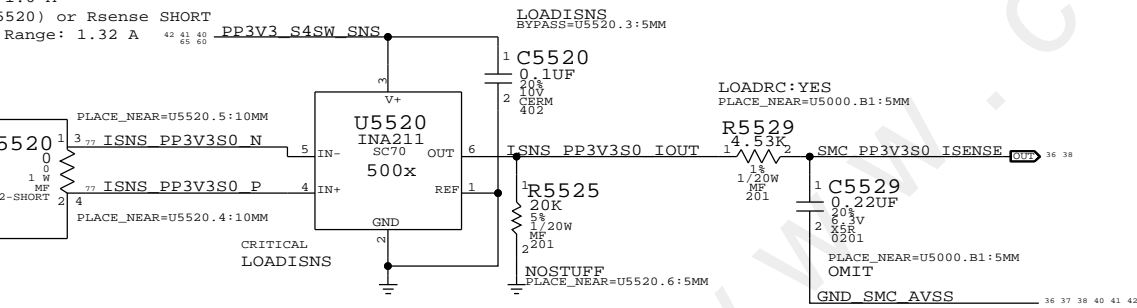
Gain: 100x  
 Rsense: 0.003 (R5400)

Trip Target on CPU High current: 2.5 A  
 Hysteresis Circuit:  
 Vref = 0.737 V  
 Vth = 0.616 V -> 2.054 A on CPU High current  
 Vtl = 0.771 V -> 2.571 A on CPU High current  
 Hysteresis Margin = 0.518 A



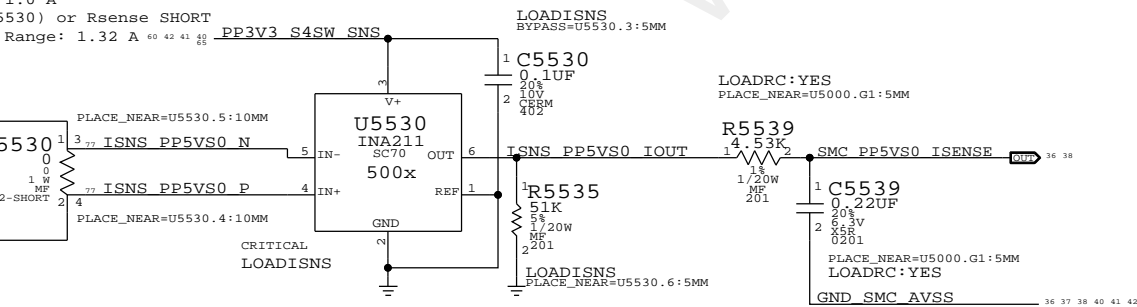
### 3.3V S0 Rail Current Sense (IR3C)

Gain: 500x, EDP: 1.0 A  
 Rsense: 0.005 (R5520) or Rsense SHORT  
 Vsense: 21.5 mV, Range: 1.32 A  
 SMC ADC: 14



### 5V S0 Rail Current Sense (IR5C)

Gain: 500x, EDP: 1.0 A  
 Rsense: 0.005 (R5530) or Rsense SHORT  
 Vsense: 23.5 mV, Range: 1.32 A  
 SMC ADC: 17



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
117S0008	2	RES,MTL,FLIM,100K,1/16W,0201,SMD,LF	C5569,C5519		LOADRC:NO
117S0008	3	RES,MTL,FLIM,100K,1/16W,0201,SMD,LF	C5529,C5539,C5549		LOADRC:NO
117S0008	1	RES,MTL,FLIM,100K,1/16W,0201,SMD,LF	C5579		DDRRC:NO

SYNC MASTER=J44 SYNC DATE=08/12/2013

**Power Sensors: Load Side**

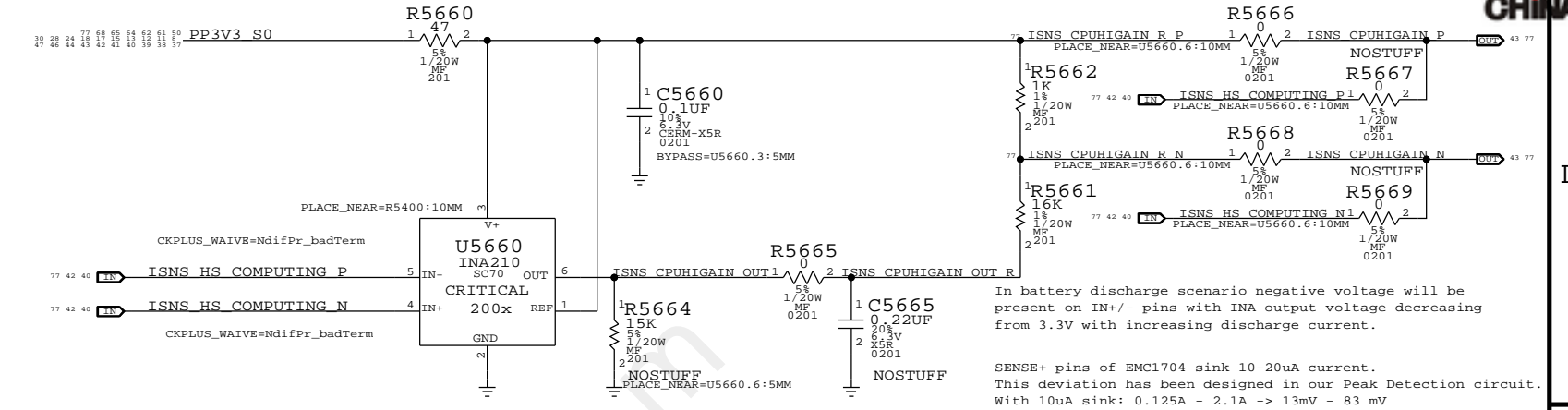
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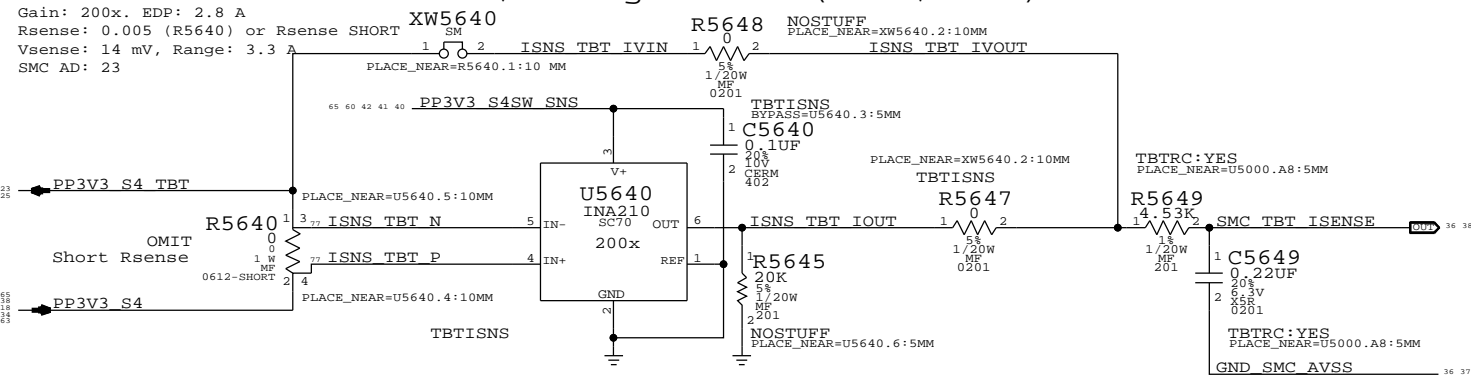
### CPU High Side (IC0R) Peak Detection Support



In battery discharge scenario negative voltage will be present on IN+/- pins with INA output voltage decreasing from 3.3V with increasing discharge current.

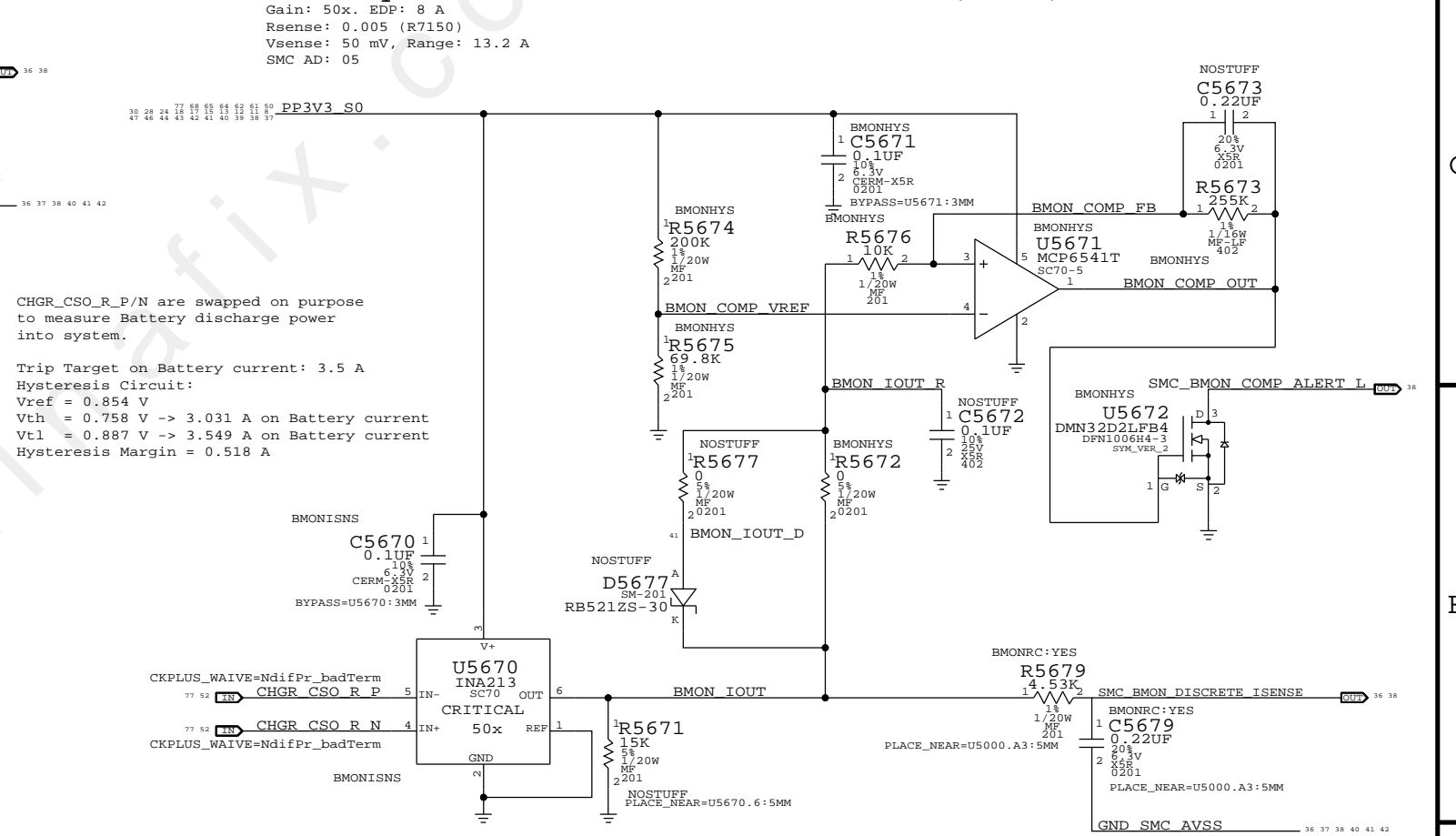
SENSE+ pins of EMC1704 sink 10-20uA current. This deviation has been designed in our Peak Detection circuit. With 10uA sink: 0.125A - 2.1A -> 13mV - 83 mV With 20uA sink: 0.125A - 2.1A -> 23mV - 92 mV

### Thunderbolt TBT Current/Voltage Sense (IHSC/VHSC)



Gain: 200x. EDP: 2.8 A  
Rsense: 0.005 (R5640) or Rsense SHORT  
Vsense: 14 mV, Range: 3.3 A  
SMC AD: 23

### Battery BMON Discrete Current Sense (IP0R) & Threshold Alert

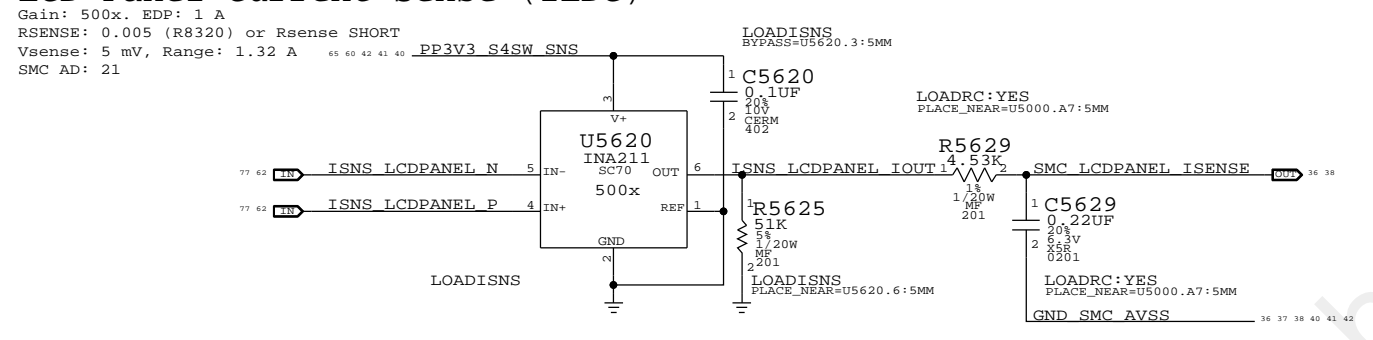


Gain: 50x. EDP: 8 A  
Rsense: 0.005 (R7150)  
Vsense: 50 mV, Range: 13.2 A  
SMC AD: 05

CHGR\_CS0\_R/P/N are swapped on purpose to measure Battery discharge power into system.

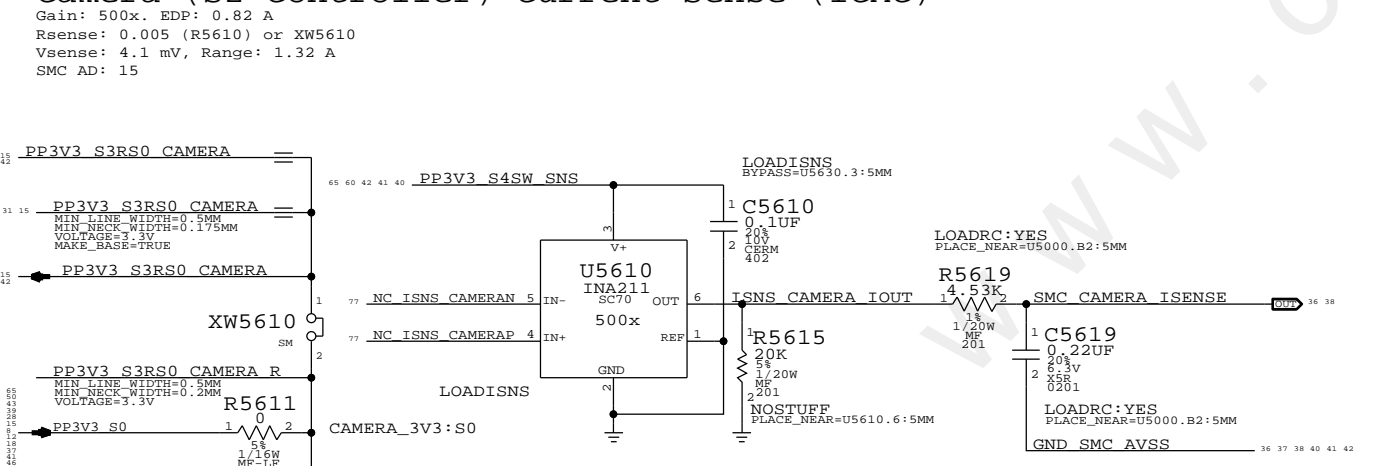
Trip Target on Battery current: 3.5 A  
Hysteresis Circuit:  
Vref = 0.854 V  
Vth = 0.758 V -> 3.031 A on Battery current  
Vtl = 0.887 V -> 3.549 A on Battery current  
Hysteresis Margin = 0.518 A

### LCD Panel Current Sense (ILDC)



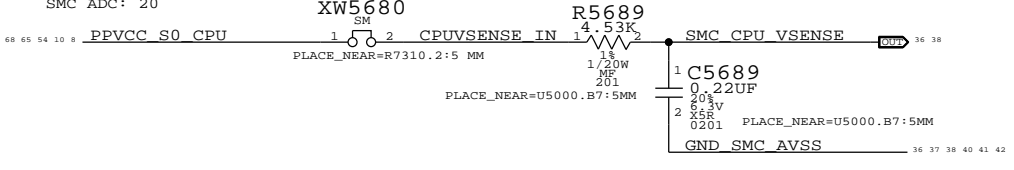
Gain: 500x. EDP: 1 A  
RSENSE: 0.005 (R8320) or Rsense SHORT  
Vsense: 5 mV, Range: 1.32 A  
SMC AD: 21

### Camera (S2 Controller) Current Sense (ICMC)



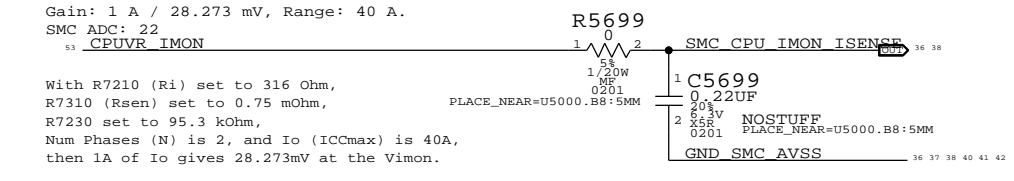
Gain: 500x. EDP: 0.82 A  
Rsense: 0.005 (R5610) or XW5610  
Vsense: 4.1 mV, Range: 1.32 A  
SMC AD: 15

### CPU Core Voltage Sense (VC0C)



SMC ADC: 20

### CPU Core IMON Current Sense (IC2C)



Gain: 1 A / 28.273 mV, Range: 40 A.  
SMC ADC: 22

With R7210 (Ri) set to 316 Ohm, R7310 (Rsen) set to 0.75 mOhm, R7230 set to 95.3 kOhm, Num Phases (N) is 2, and Io (ICmax) is 40A, then 1A of Io gives 28.273mV at the Vimon.

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
117S0008	4	RES,MTL FILM,100K,1/16W,0201,SMD,LF	C5619,C5629,C5649		
117S0008	1	RES,MTL FILM,100K,1/16W,0201,SMD,LF	C5679		

SYNC MASTER=144 SYNC DATE=08/12/2013

Power Sensors: Extended

Apple Inc.

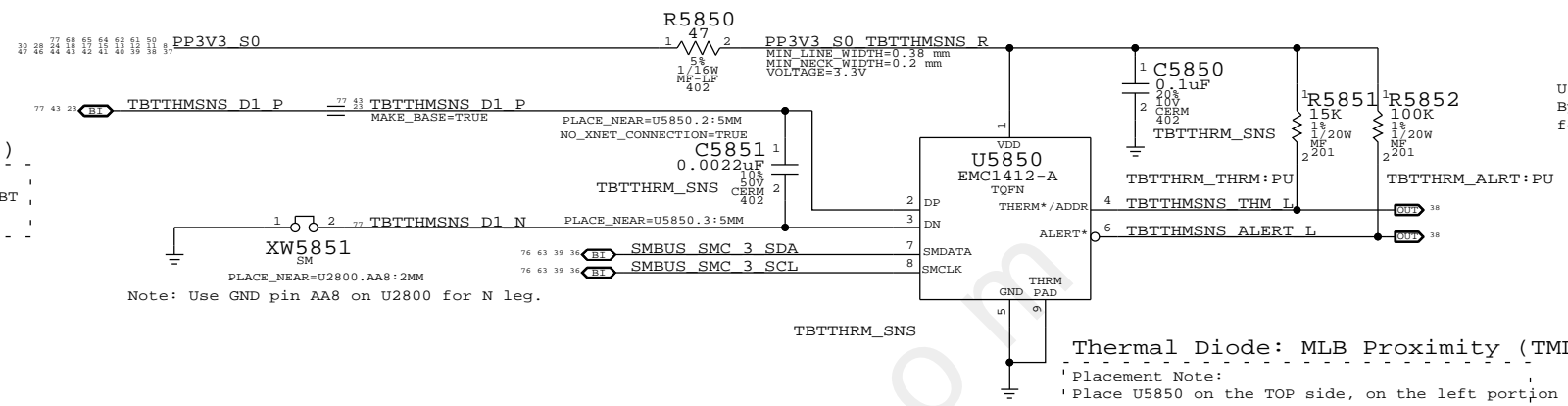
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### Thermal Sensor A: Thunderbolt Die, MLB Proximity

I2C Write: 0xD8, I2C Read: 0xD9

**Thermal Diode: TBT Die (THSP)**  
 Placement Note:  
 The P leg connects to THERMDA pin of the TBT chip, the N leg connect to pin AA8.



U5850 I2C Address:  
 By setting R5851 to 15k, I2C address for U5850 is 0xD8/0xD9.

**Thermal Diode: MLB Proximity (TMLB)**  
 Placement Note:  
 Place U5850 on the TOP side, on the left portion of the board, 1" to the right of USB connector.

### Thermal Sensor B & CPU High Peak Detection: CPU Proximity, Memory Proximity, Airflow, Fin Stack Proximity

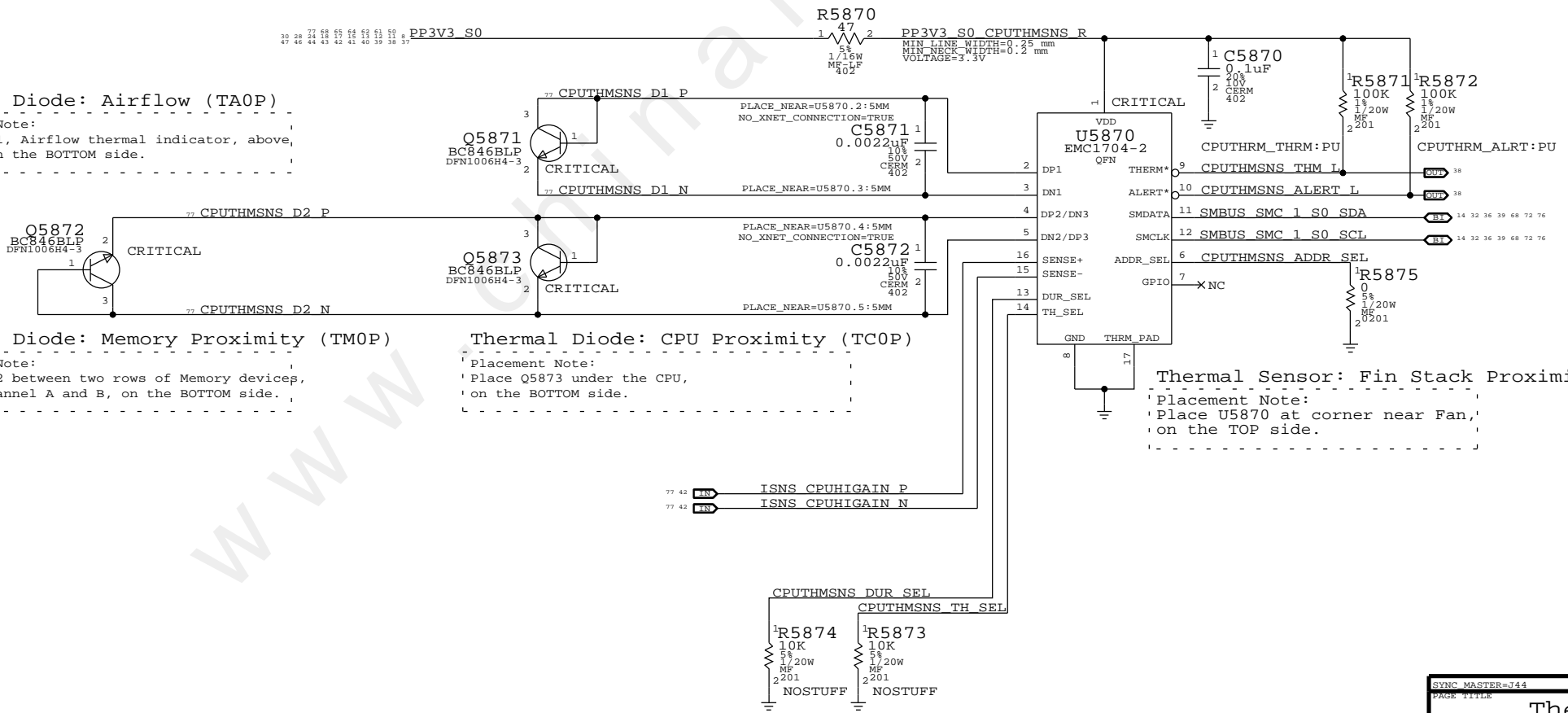
I2C Write: 0x98, I2C Read: 0x99

**Thermal Diode: Airflow (TA0P)**  
 Placement Note:  
 Place Q5871, Airflow thermal indicator, above the SSD, on the BOTTOM side.

**Thermal Diode: Memory Proximity (TM0P)**  
 Placement Note:  
 Place Q5872 between two rows of Memory devices, between channel A and B, on the BOTTOM side.

**Thermal Diode: CPU Proximity (TC0P)**  
 Placement Note:  
 Place Q5873 under the CPU, on the BOTTOM side.

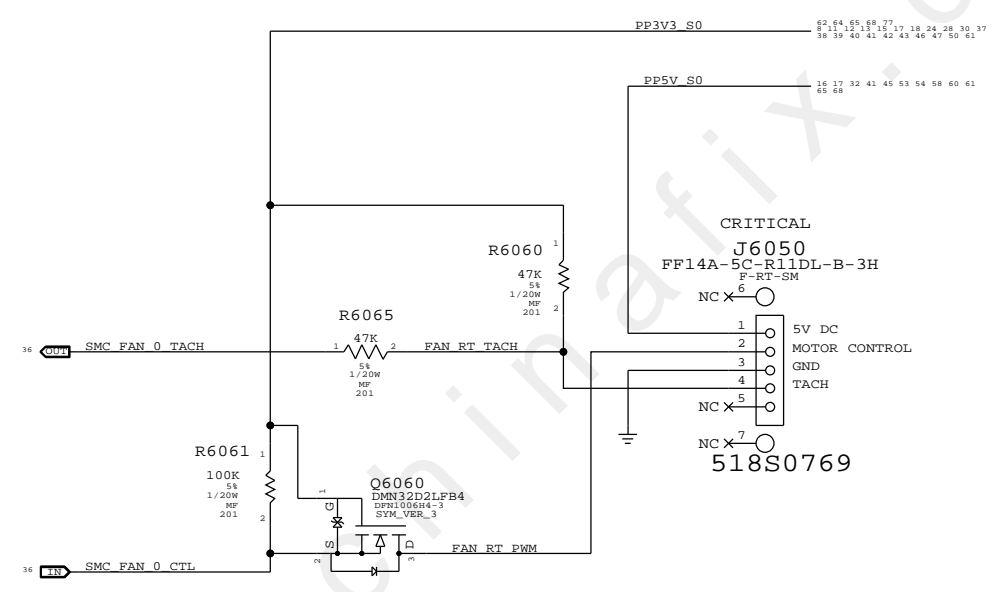
**Thermal Sensor: Fin Stack Proximity (Th1H)**  
 Placement Note:  
 Place U5870 at corner near Fan, on the TOP side.



SYNC MASTER=144		SYNC DATE=08/12/2013	
<b>Thermal Sensors</b>			
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# FAN CONNECTOR

KEEP THE 5 PIN CONNECTOR FROM D1

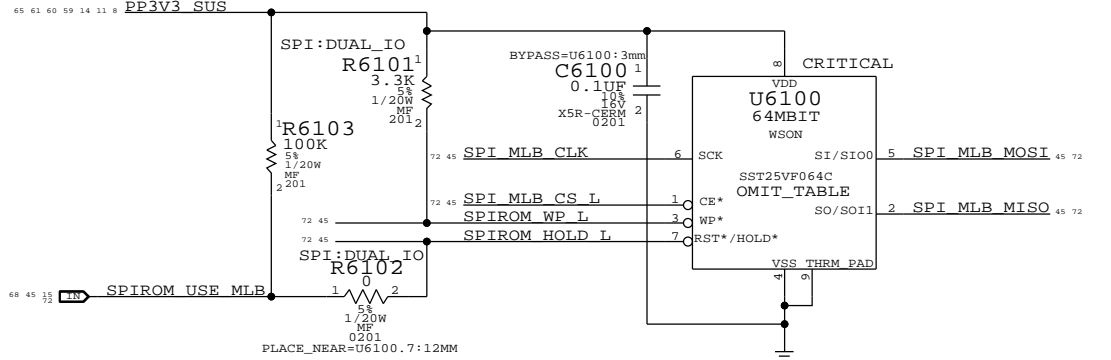


SYNC MASTER=144		SYNC DATE=08/12/2013	
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### SPI ROM

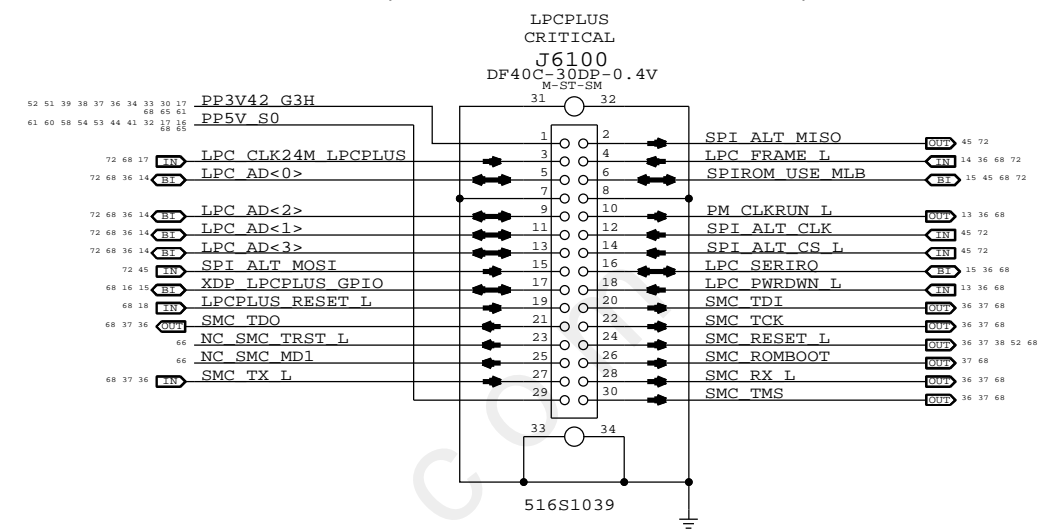
Dual-IO Mode (Mode 0 & 3) supported.  
 SPI Frequency: 50MHz for CPU, 20MHz for SMC.



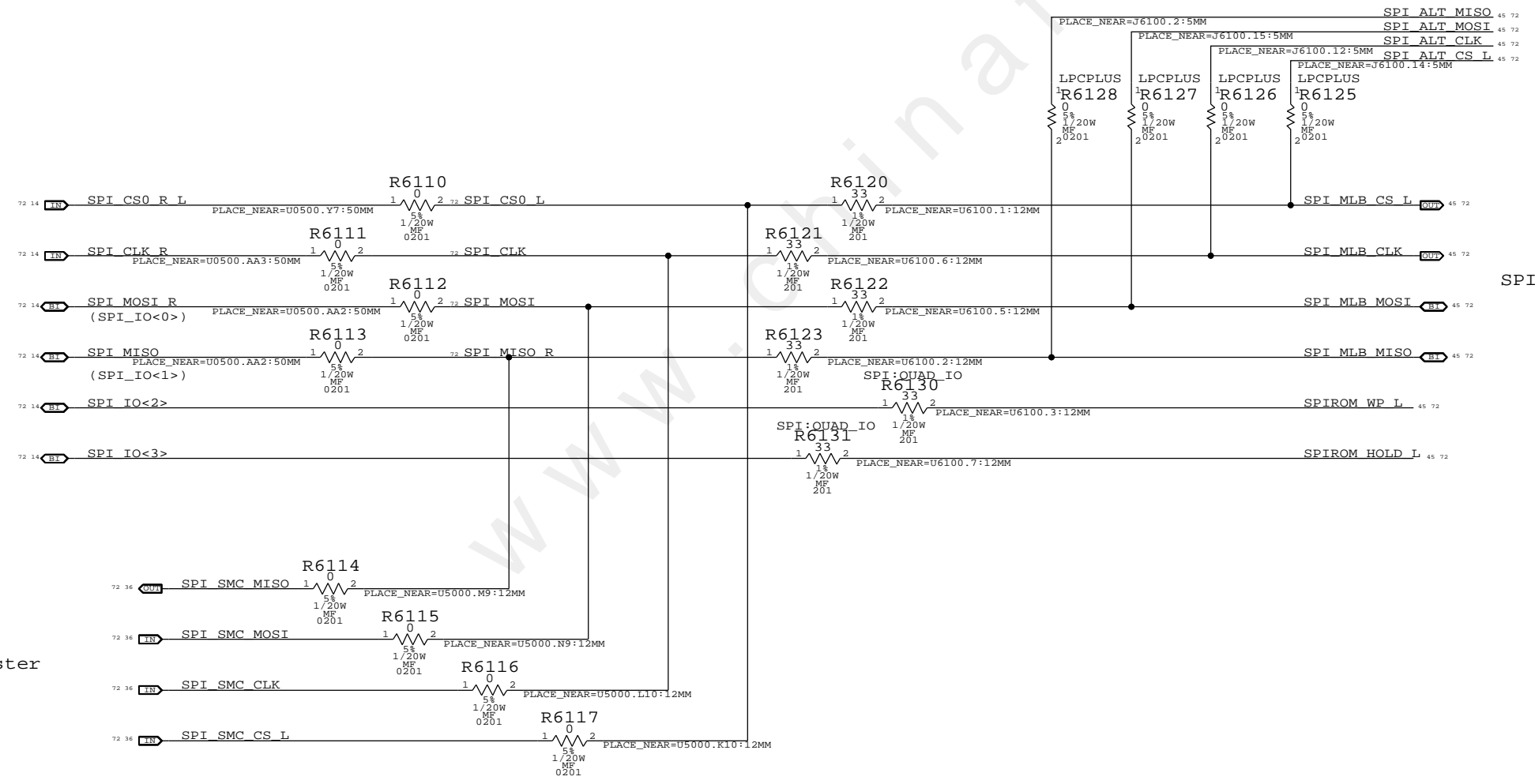
NOTE: If HOLD\* is asserted ROM will ignore SPI cycles in normal and Dual-IO modes.

NOTE: Not all ROM APNs currently used support Quad-IO. Also not compatible with Matt card ROM override. Quad-IO support is for experimentation only.

### LPC+SPI Connector (Matt Card Connector)



### SPI Bus Series Termination



Matt Card ROM Slave

SPI ROM Slave

CPU Master

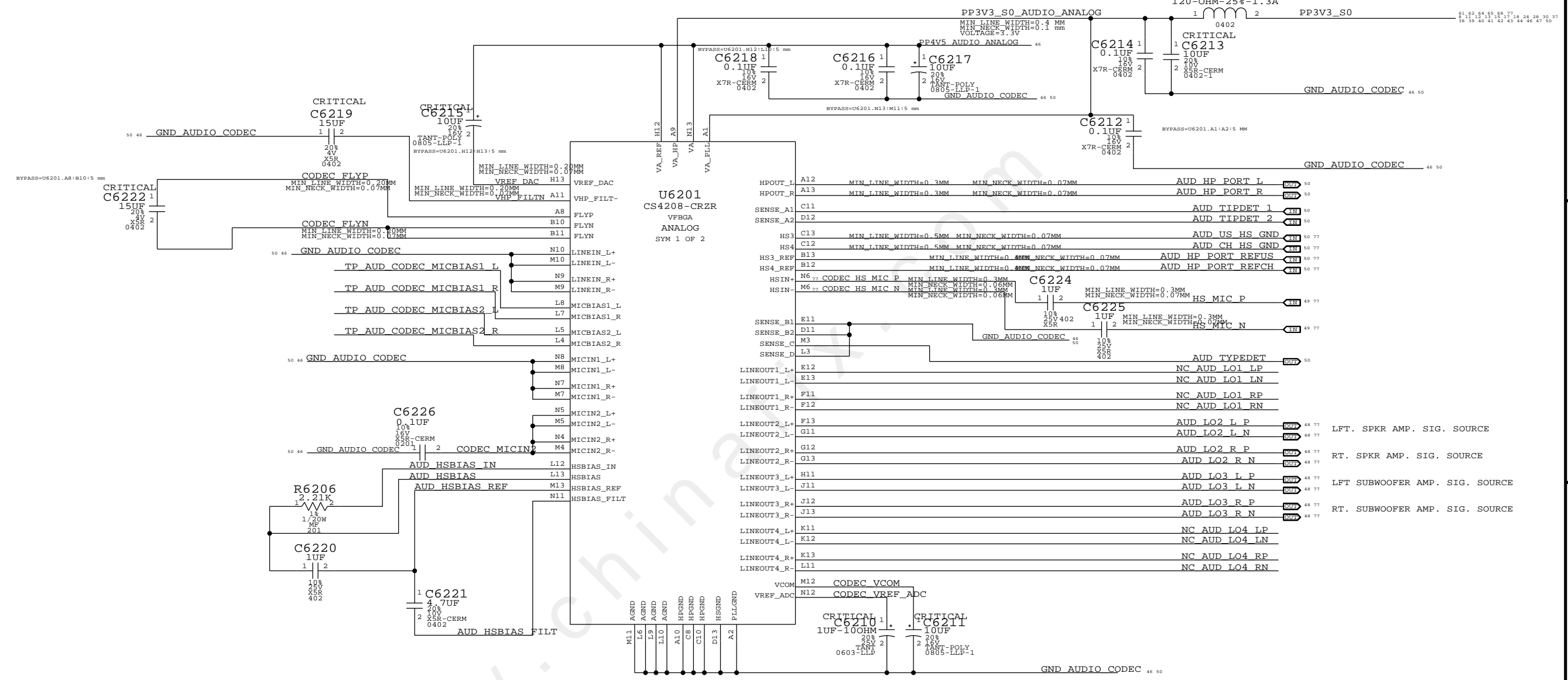
SMC12 Master

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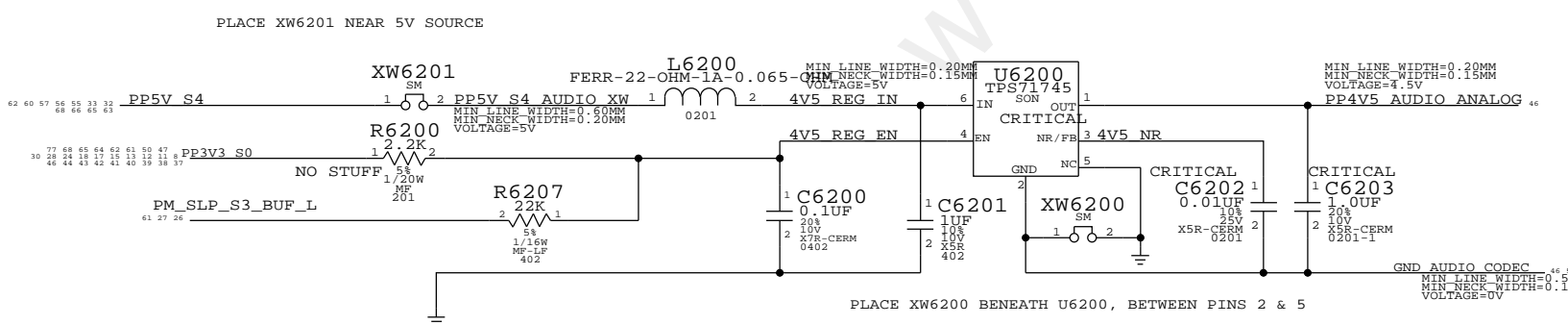
### AUDIO CODEC, ANALOG BLOCKS

APPLE P/N 353S4080



### 4.5V POWER SUPPLY FOR CODEC

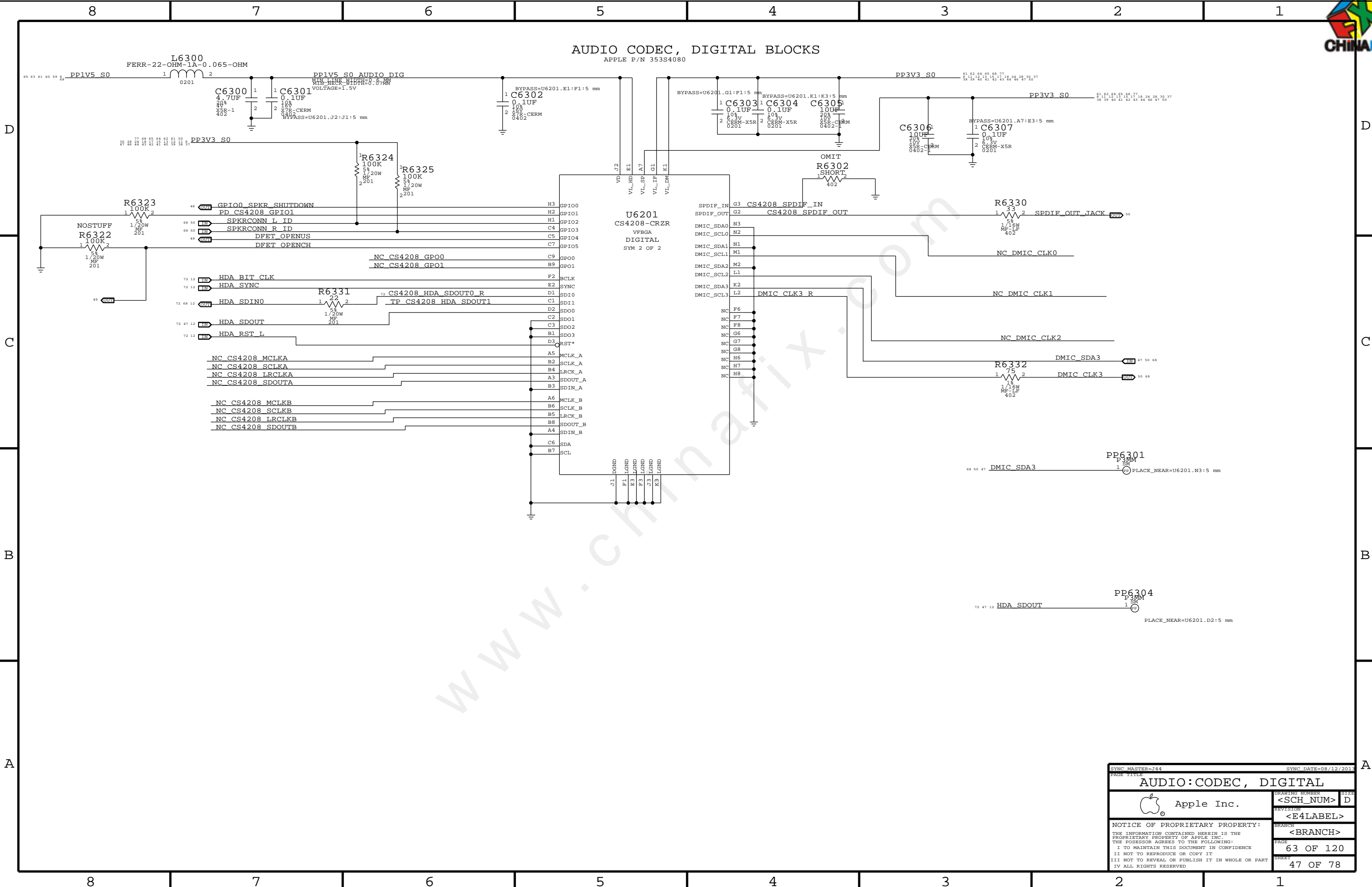
APPLE P/N 353S2456



SYNC MASTER=144		SYNC DATE=08/12/2013	
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AUDIO:CODEC, ANALOG		DRAWING NUMBER	SIZE
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AUDIO CODEC, DIGITAL BLOCKS  
APPLE P/N 353S4080



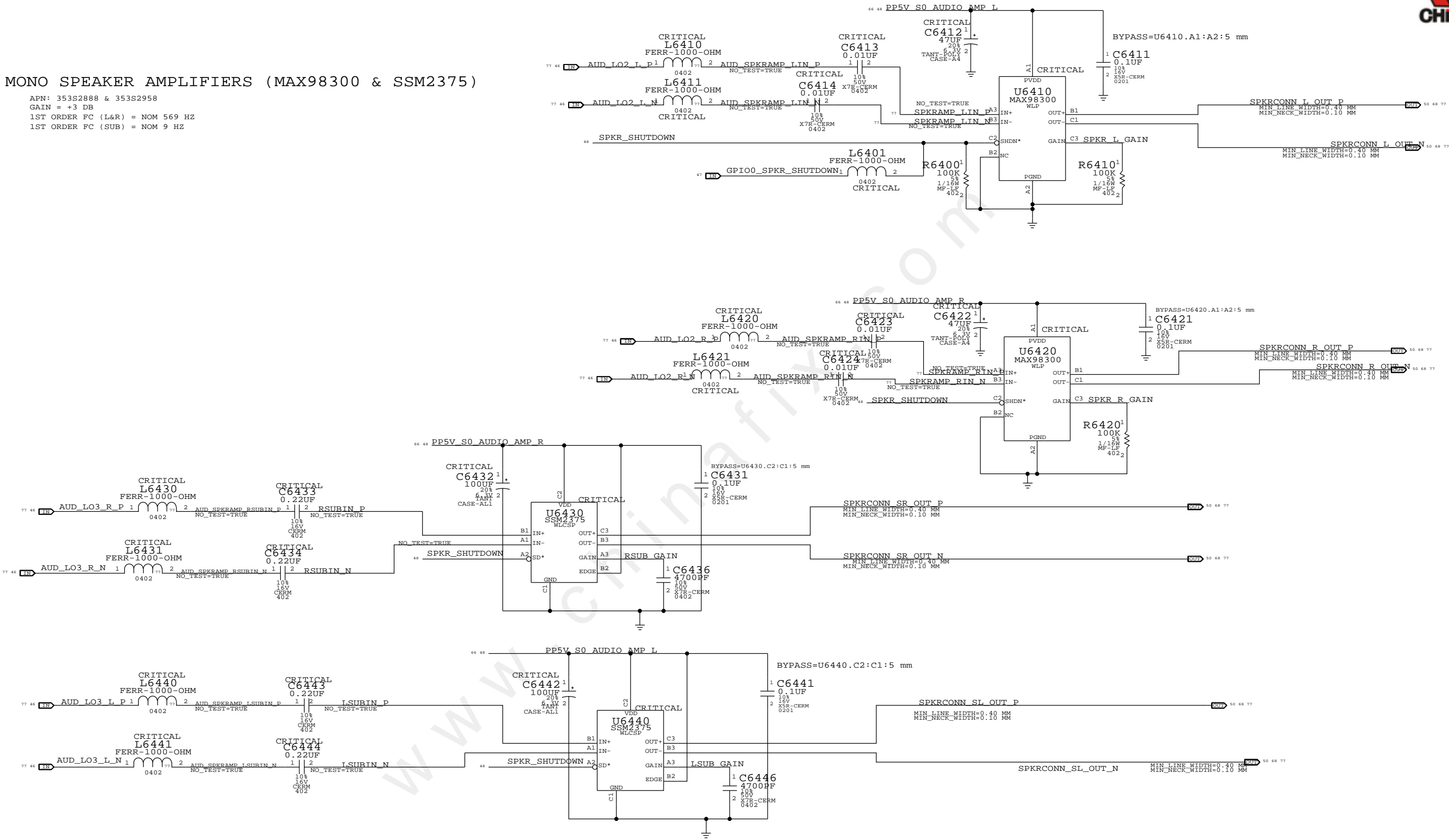
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8 7 6 5 4 3 2 1

### 4X MONO SPEAKER AMPLIFIERS (MAX98300 & SSM2375)

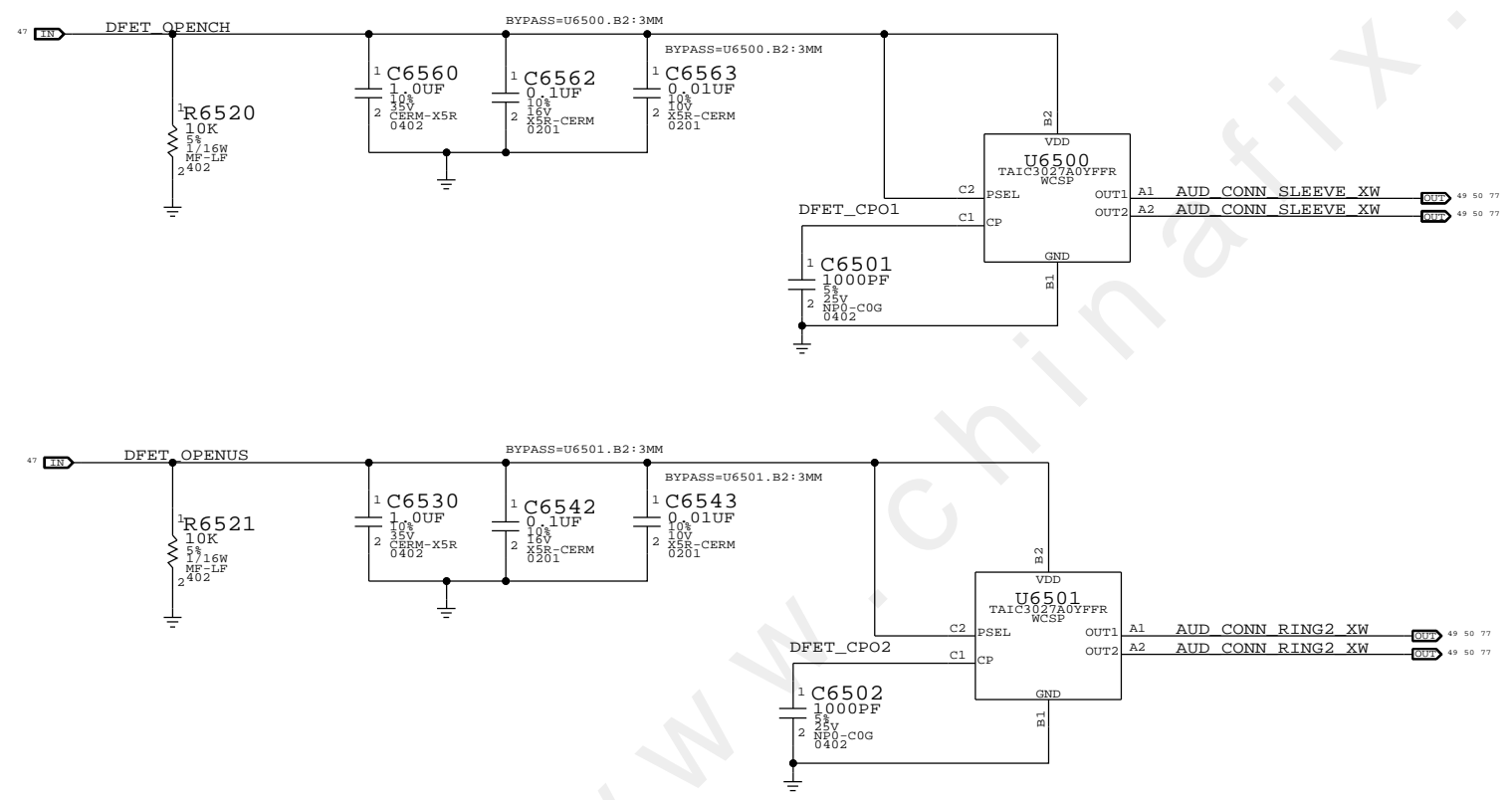
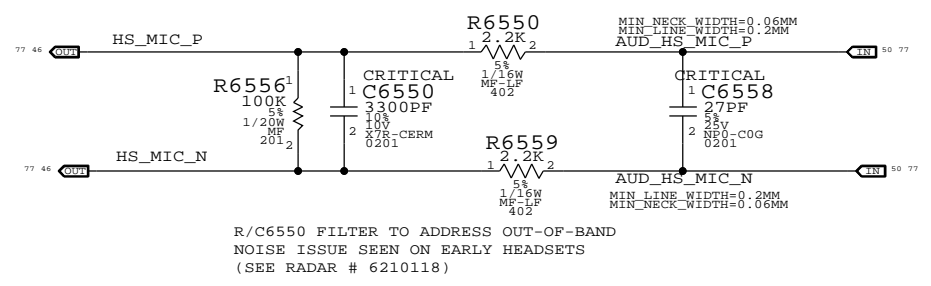
APN: 353S2888 & 353S2958  
GAIN = +3 DB  
1ST ORDER FC (L&R) = NOM 569 HZ  
1ST ORDER FC (SUB) = NOM 9 HZ



8 7 6 5 4 3 2 1

SYNC MASTER=144		SYNC DATE=08/12/2013	
PAGE TITLE			
<b>AUDIO: SPEAKER AMP</b>			
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		<BRANCH>	
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SYNC MASTER=144		SYNC DATE=08/12/2013	
<b>AUDIO: JACK</b>			
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		<E4LABEL>	
		BRANCH	<BRANCH>
		PAGE	65 OF 120
		SHEET	49 OF 78



### CODEC OUTPUT SIGNAL PATHS

FUNCTION	VOLUME	CONVERTER	PIN COMPLEX	MUTE CONTROL
HP/HS OUT	0X02 (2)	0X02 (2)	0X10 (16)	N/A
TWEETERS	0X03 (3)	0X03 (3)	0X12 (18)	CODEC GPIO0
SUB	0X04 (4)	0X04 (4)	0X13 (19)	CODEC GPIO0
SPDIF OUT	N/A	0X0E (14)	0X21 (33)	N/A

### CODEC INPUT SIGNAL PATHS

FUNCTION	CONVERTER	PIN COMPLEX	VREF
DMIC 1	0X09 (9)	0X1C (28)	3.3V
DMIC 2	0X09 (9)	0X1C (28)	3.3V
HEADSET MIC	0X07 (7)	0X18 (24)	2.7V

### OTHER CODEC GPIO LINES

LEFT SPEAKER ID	GPIO2 INPUT	HIGH = FG, LOW = MERRY
RIGHT SPEAKER ID	GPIO3 INPUT	HIGH = FG, LOW = MERRY
DFET CONTROL	GPIO4 OUTPUT	HIGH = DFETS OPEN

### SPEAKER CONNECTOR

HP=80HZ  
APN: 518S0672

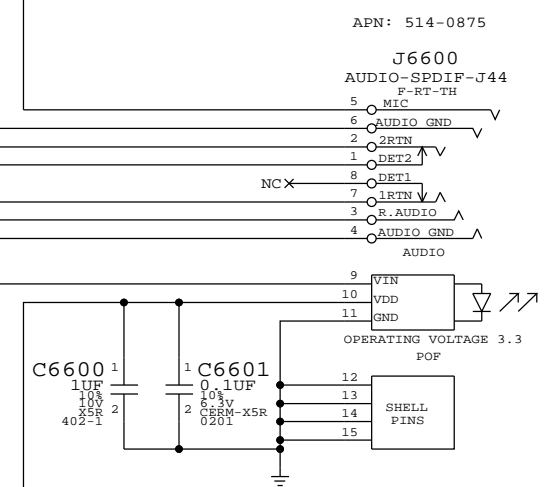
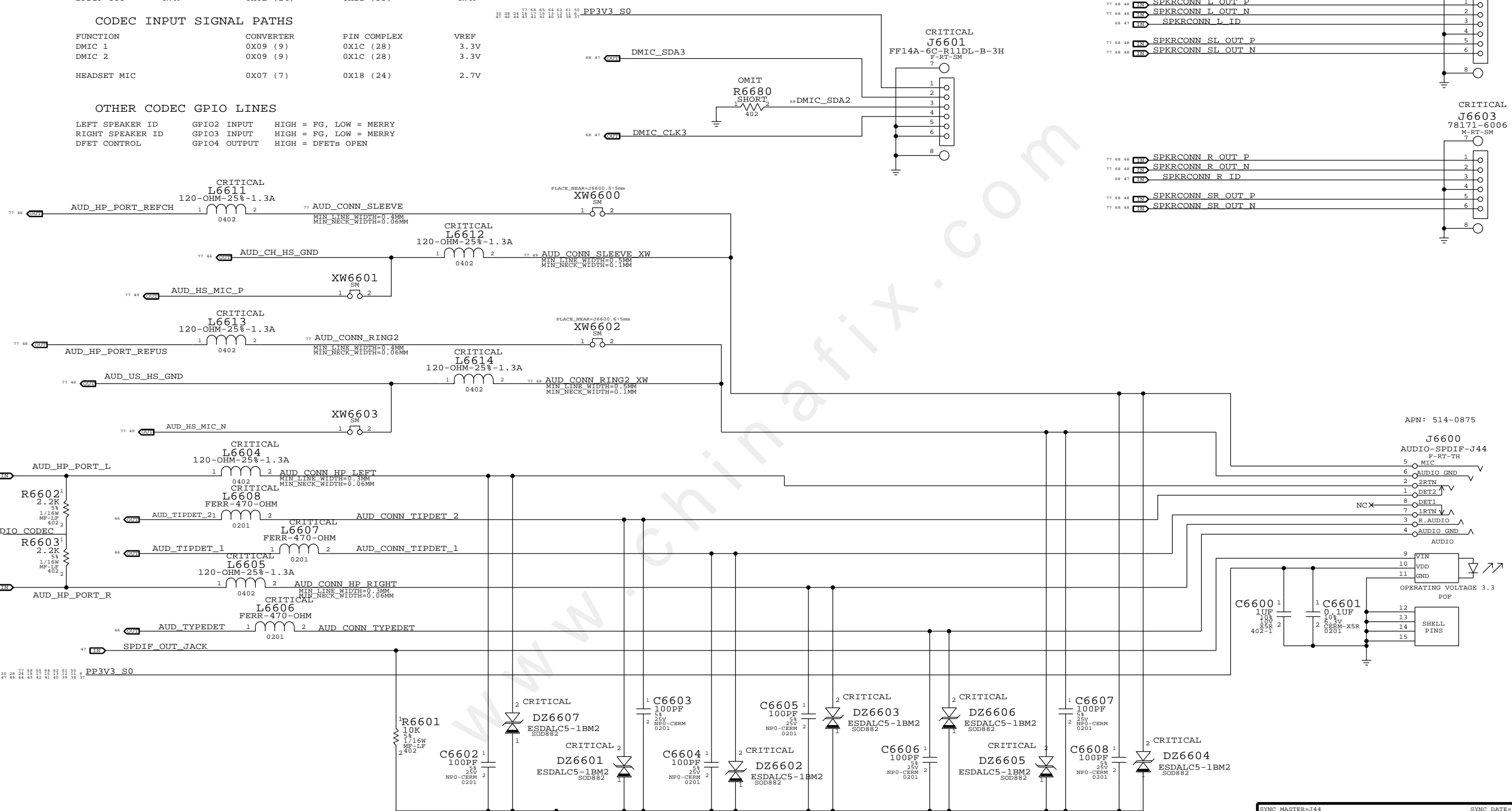
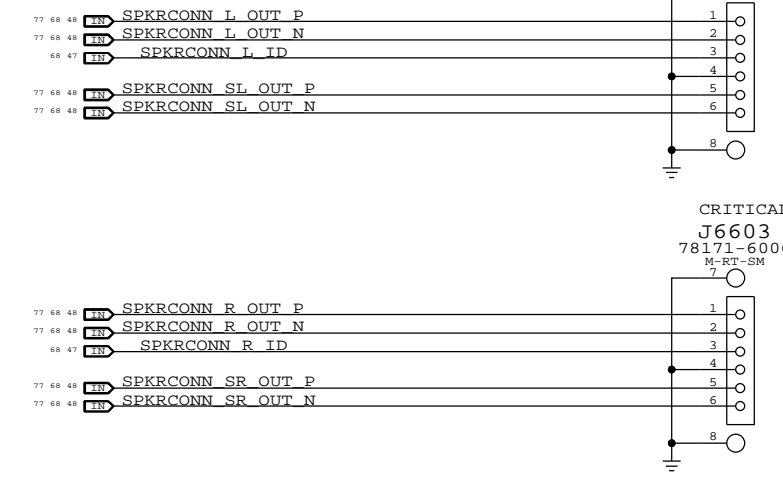
CRITICAL  
J6602  
78171-6006  
M-RT-SM

### 2-MIC CONNECTOR

APN: 518S0818

CRITICAL  
J6601  
FF14A-6C-R11DL-B-3H  
F-RT-SM

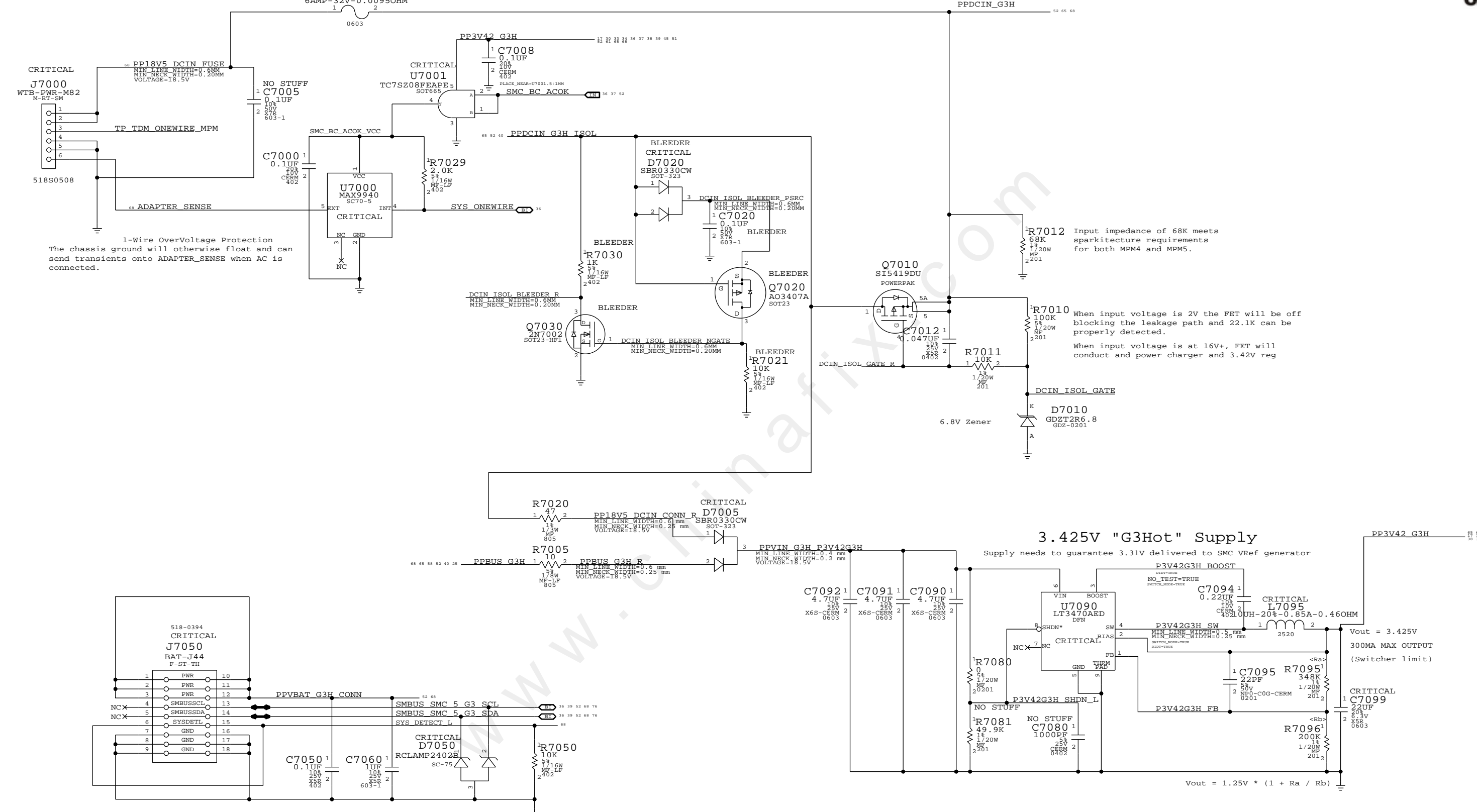
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J6603  
78171-6006  
M-RT-SM



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# MagSafe DC Power Jack



DC-In & Battery Connectors	
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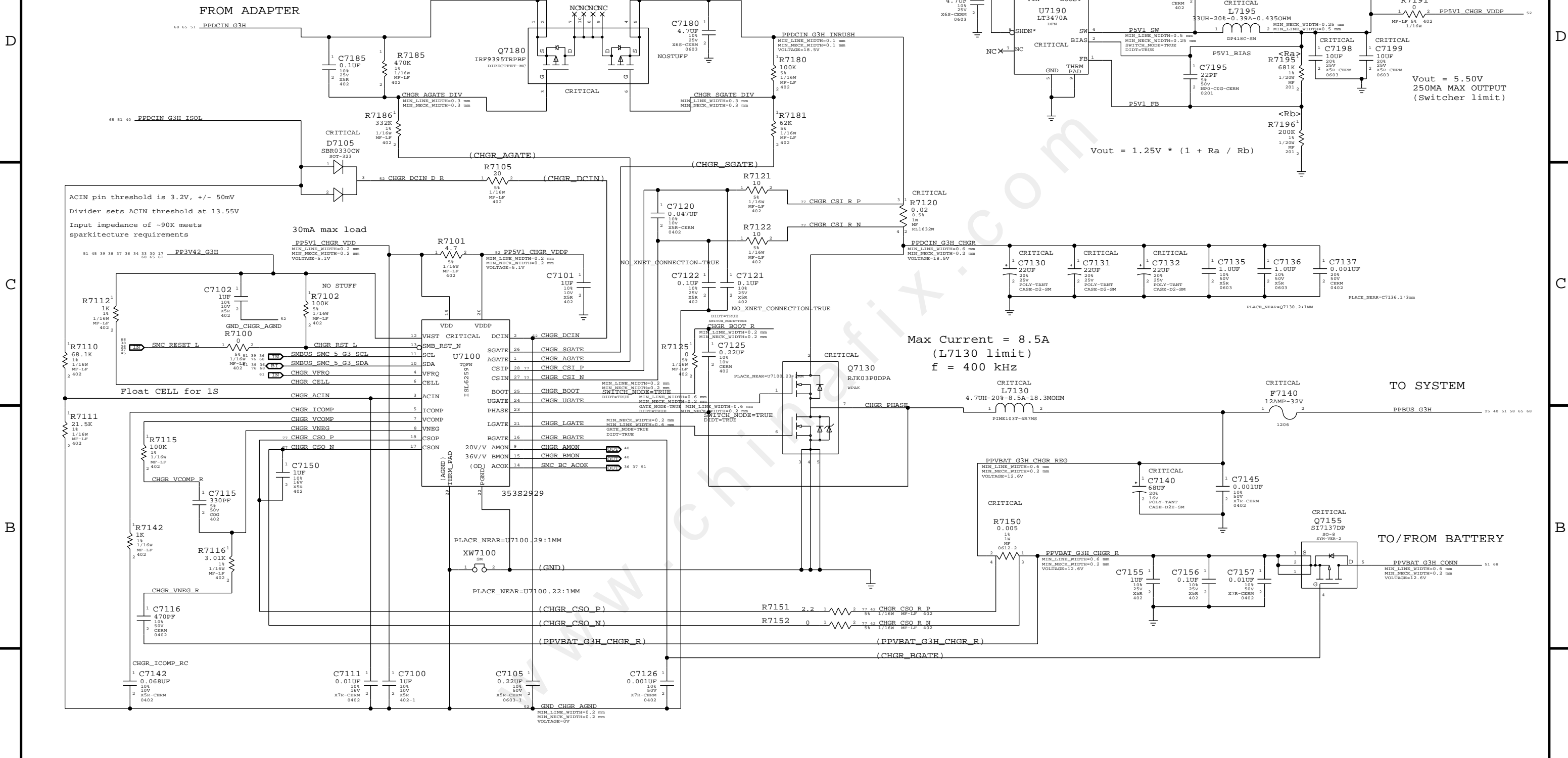


# Reverse-Current Protection

## Inrush Limiter

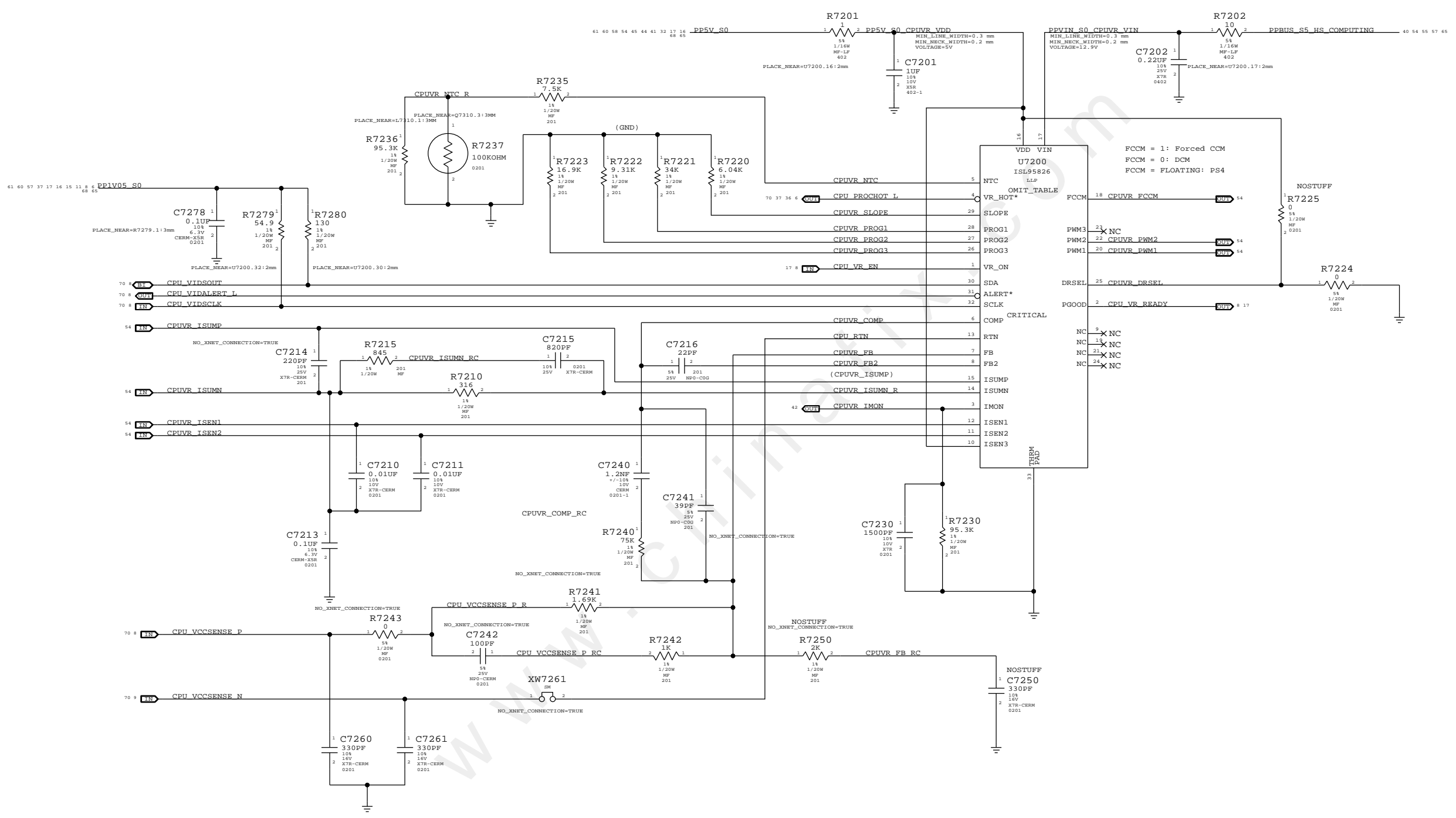
For Exp Lot6 spec

NOSTUFF

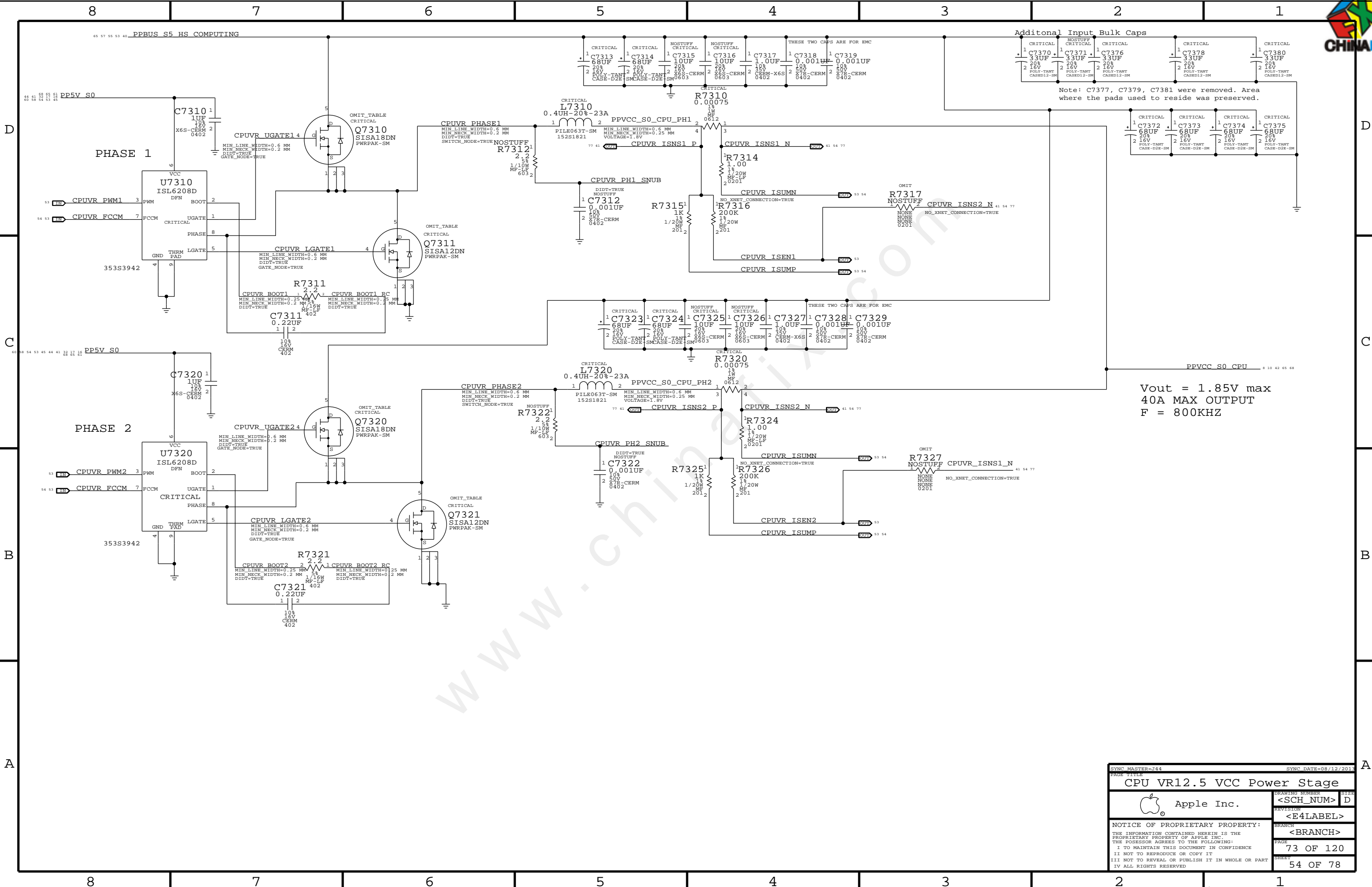


SYNC MASTER=144		SYNC DATE=08/12/2013	
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PBus Supply & Battery Charger			
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PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
353S4170	1	IC, ISL95826R6200, PWM, PGOOD, SCREEN, 32P, QFN	U7200	CRITICAL	



SYNC MASTER=144		SYNC DATE=08/12/2013	
CPU VR12.6 VCC Regulator IC			
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		<SCH_NUM>	D
		REVISION	<E4LABEL>
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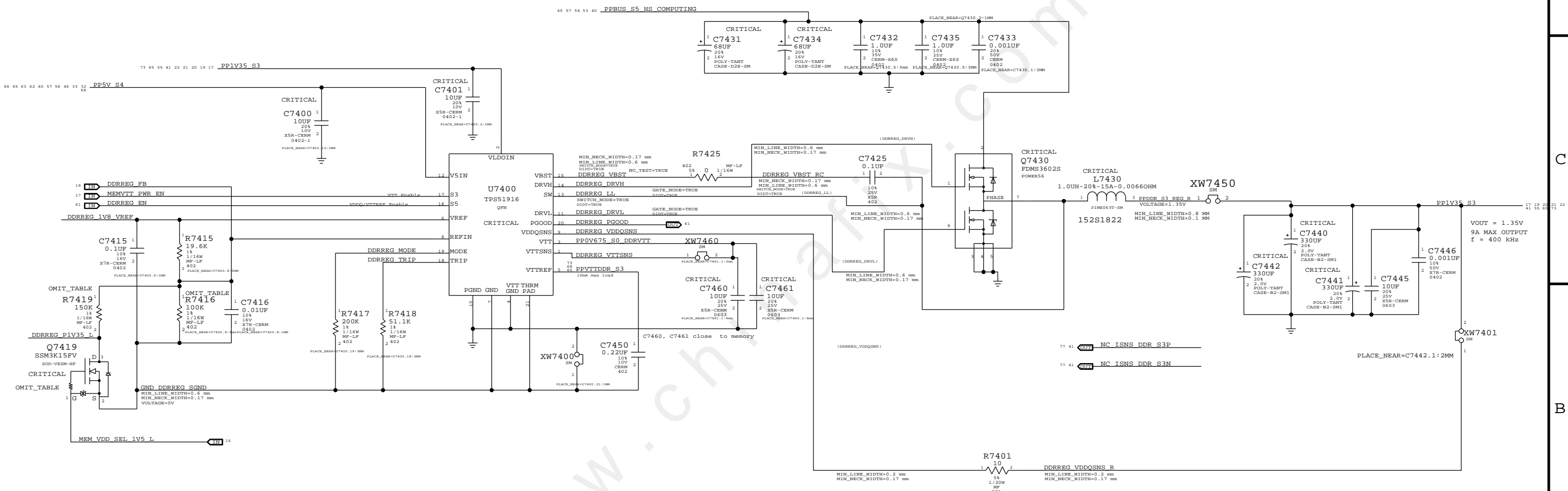
Additional Input Bulk Caps

Note: C7377, C7379, C7381 were removed. Area where the pads used to reside was preserved.

Vout = 1.85V max  
40A MAX OUTPUT  
F = 800KHZ

CPU VR12.5 VCC Power Stage	
Apple Inc.	DRAWING NUMBER: <SCH_NUM>
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### DDR3L (1V35 S3) REGULATOR



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
114S0411	1	RES,MTL FILM,1/16W,100K,1,0402,SMD,LF	R7416	CRITICAL	PPDDR:1V5
114S0391	1	RES,MTL FILM,1/16W,60.4K,1,0402,SMD,LF	R7416	CRITICAL	PPDDR:1V35
376S0612	1	MOSFET,N-CH,30V,100MA,7.00HM,SOT-723,HP	Q7419	CRITICAL	PPDDR:1V5
114S0428	1	RES, MTL FILM,1/16W,150k,0402,SMD,LF	R7419	CRITICAL	PPDDR:1V5

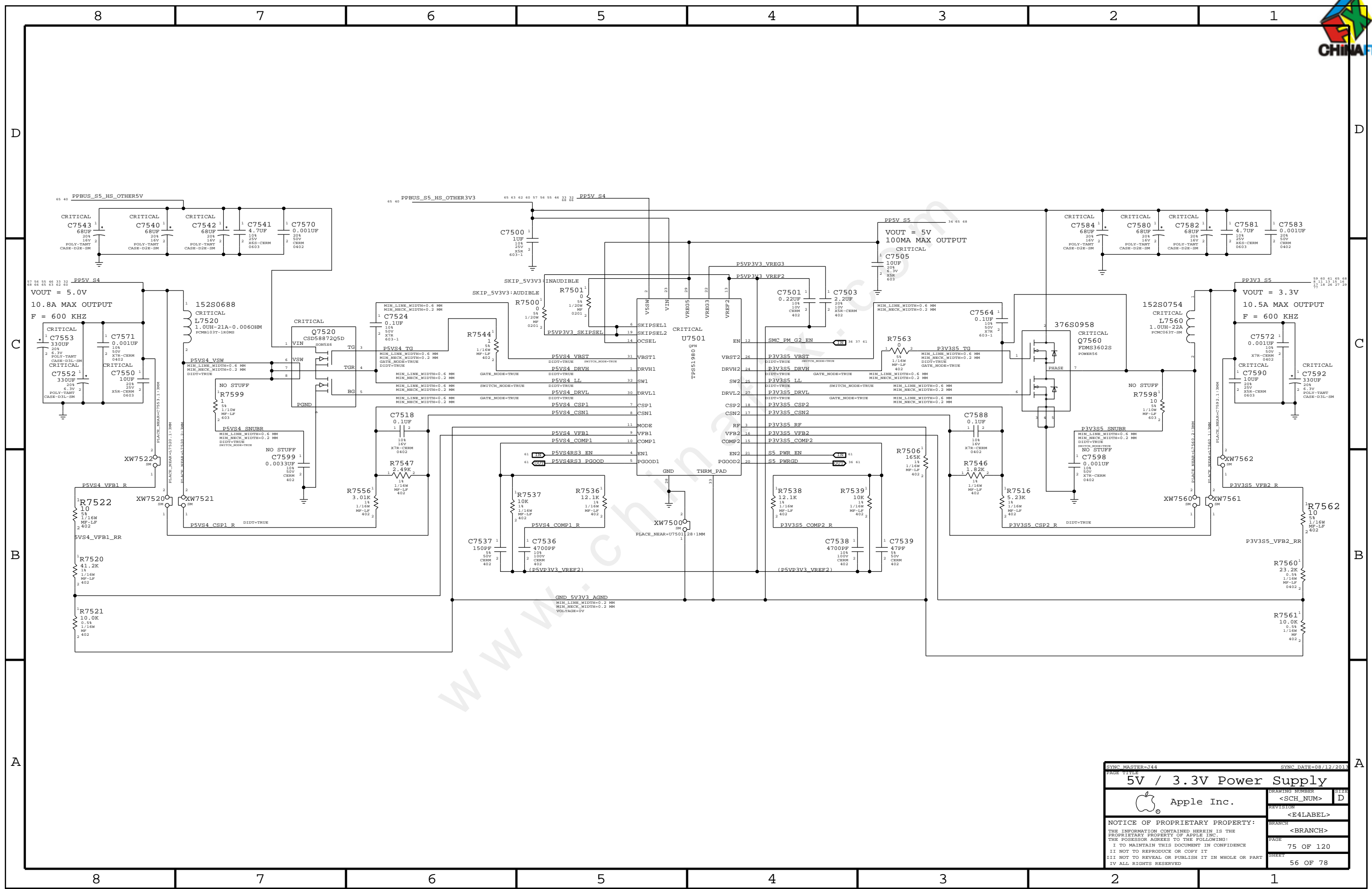
SYMC: WATERS-144 SYMC: DATE: 08/12/2015

1.35V DDR3 SUPPLY

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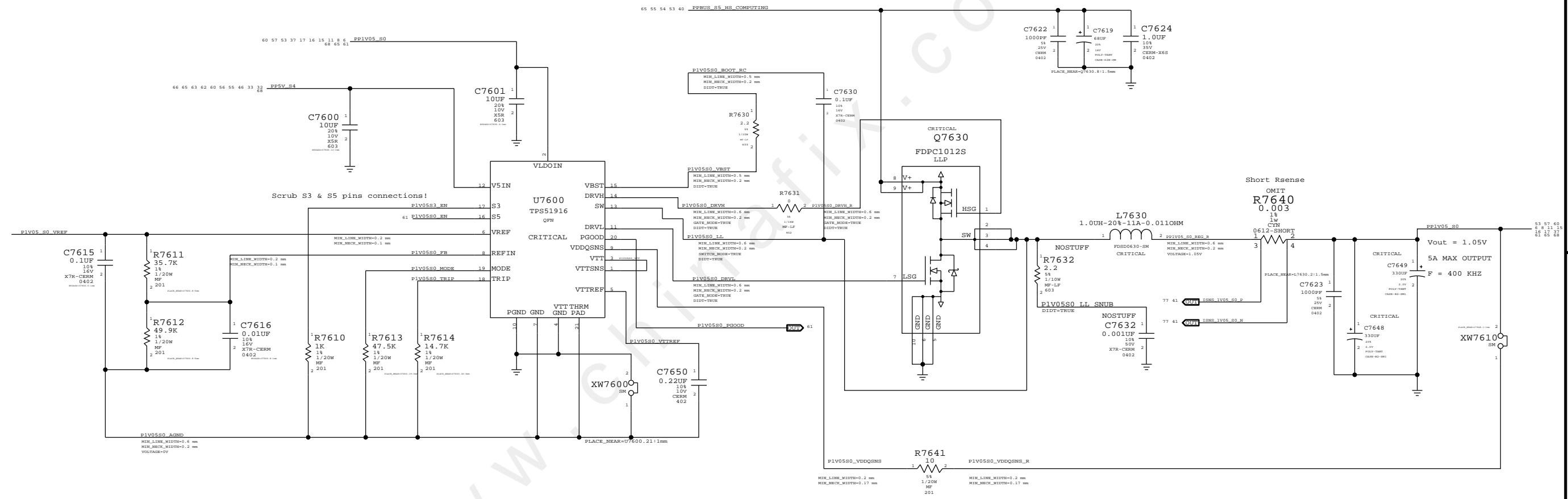
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5V / 3.3V Power Supply			
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### 1.05V S0 Regulator



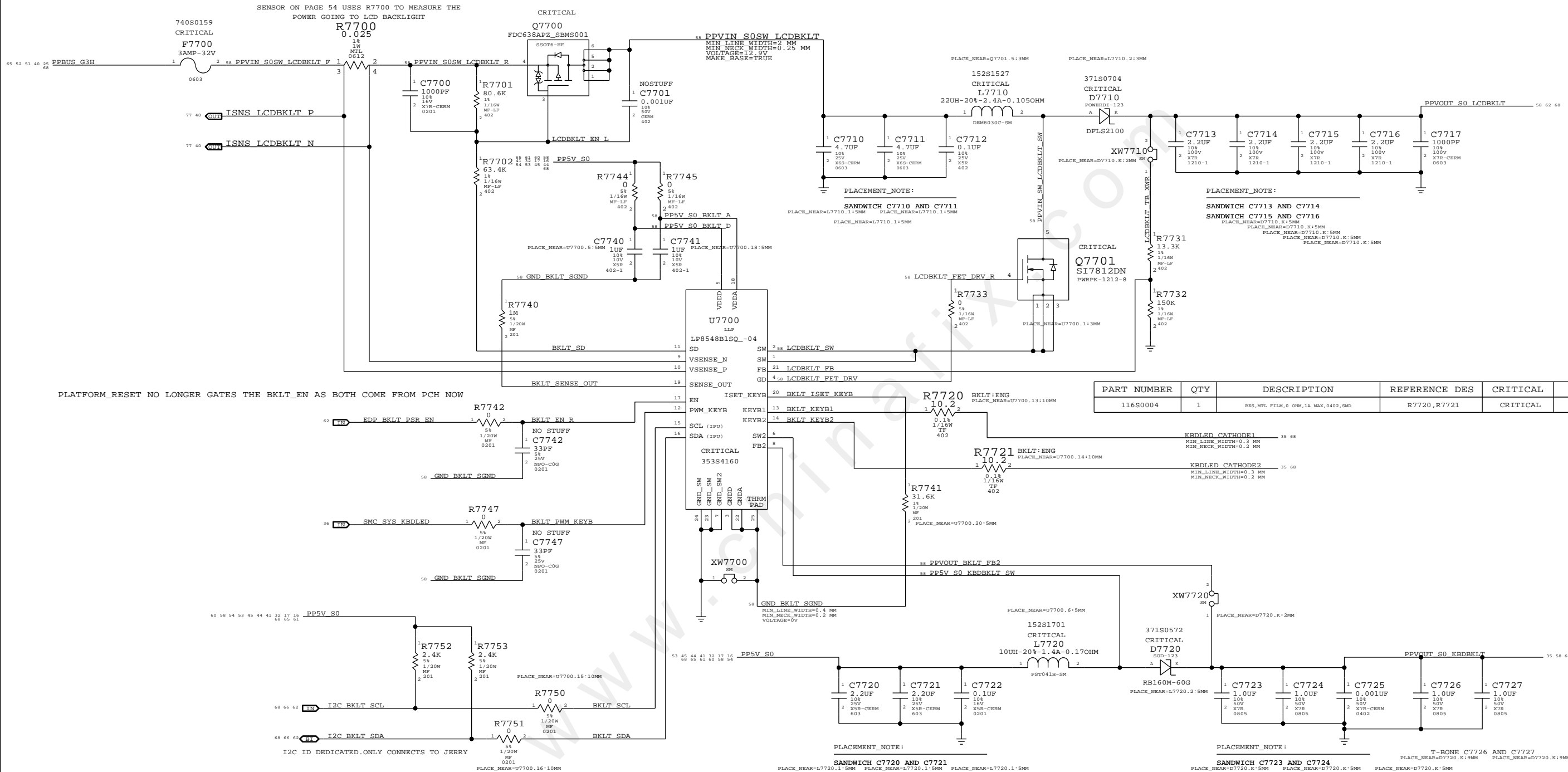
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Page Notes

Power aliases required by this page:  
 - =PPVIN\_S0SW\_LCDBKLT FET (9-12.6V LCD BACKLIGHT INPUT)  
 - =PP5V\_S0\_BKLT (5V BACKLIGHT DRIVER INPUT)  
 - =PP5V\_S0SW\_KBDLED (5V KEYBOARD BACKLIGHT INPUT)

BOM options provided by this page:  
 BKLT:ENG - Stuffs 10.2 ohm series R for engineering builds  
 BKLT:PROD - Stuffs 0 ohm series R for production

SENSOR ON PAGE 54 USES R7700 TO MEASURE THE POWER GOING TO LCD BACKLIGHT



PLATFORM\_RESET NO LONGER GATES THE BKLT\_EN AS BOTH COME FROM PCH NOW

PBUS LINE WIDTHS

LCD BKLT LINE WIDTHS

KBD BKLT LINE WIDTHS

PP5V\_S0\_BKLT\_A 58  
 MIN\_LINE\_WIDTH=2 MM  
 MIN\_NECK\_WIDTH=0.25 MM  
 VOLTAGE=5V

PP5V\_S0\_BKLT\_D 58  
 MIN\_LINE\_WIDTH=2 MM  
 MIN\_NECK\_WIDTH=0.25 MM  
 VOLTAGE=5V

PPVIN\_S0SW\_LCDBKLT\_F 58  
 MIN\_LINE\_WIDTH=2 MM  
 MIN\_NECK\_WIDTH=0.25 MM  
 VOLTAGE=12.9V

PPVIN\_S0SW\_LCDBKLT\_R 58  
 MIN\_LINE\_WIDTH=2 MM  
 MIN\_NECK\_WIDTH=0.25 MM  
 VOLTAGE=12.9V

PPVIN\_S0SW\_LCDBKLT\_FET 58  
 MIN\_LINE\_WIDTH=2 MM  
 MIN\_NECK\_WIDTH=0.25 MM  
 VOLTAGE=5V

PPVIN\_S0SW\_LCDBKLT 58  
 MIN\_LINE\_WIDTH=2 MM  
 MIN\_NECK\_WIDTH=0.25 MM  
 VOLTAGE=12.9V

LCDBKLT\_FET\_DRV\_R 58  
 MIN\_LINE\_WIDTH=2 MM  
 MIN\_NECK\_WIDTH=0.25 MM  
 VOLTAGE=5V  
 GATE\_MODE=TRUE  
 DIDD=TRUE

LCDBKLT\_FET\_DRV 58  
 MIN\_LINE\_WIDTH=2 MM  
 MIN\_NECK\_WIDTH=0.25 MM  
 VOLTAGE=5V  
 GATE\_MODE=TRUE  
 DIDD=TRUE

LCDBKLT\_SW 58  
 MIN\_LINE\_WIDTH=2 MM  
 MIN\_NECK\_WIDTH=0.25 MM  
 VOLTAGE=5V  
 SWITCH\_MODE=TRUE  
 DIDD=TRUE

PPVIN\_SW\_LCDBKLT\_SW 58  
 MIN\_LINE\_WIDTH=2 MM  
 MIN\_NECK\_WIDTH=0.25 MM  
 VOLTAGE=5V  
 SWITCH\_MODE=TRUE  
 DIDD=TRUE

PP5V\_S0\_LCDBKLT 58 62 68  
 MIN\_LINE\_WIDTH=0.5 MM  
 MIN\_NECK\_WIDTH=0.25 MM  
 VOLTAGE=5V

PP5V\_S0\_BKLT\_FB2 58  
 MIN\_LINE\_WIDTH=0.4 MM  
 MIN\_NECK\_WIDTH=0.25 MM  
 VOLTAGE=5V

PP5V\_S0\_KBDKLT\_SW 58  
 MIN\_LINE\_WIDTH=0.5 MM  
 MIN\_NECK\_WIDTH=0.25 MM  
 VOLTAGE=40V  
 SWITCH\_MODE=TRUE  
 DIDD=TRUE

PP5V\_S0\_KBDKLT 35 58 68  
 MIN\_LINE\_WIDTH=0.5 MM  
 MIN\_NECK\_WIDTH=0.25 MM  
 VOLTAGE=40V

PP5V\_S0\_BKLT\_FB2 58  
 MIN\_LINE\_WIDTH=0.4 MM  
 MIN\_NECK\_WIDTH=0.25 MM  
 VOLTAGE=40V

SYNC MASTER=144 SYNC DATE=08/12/2013

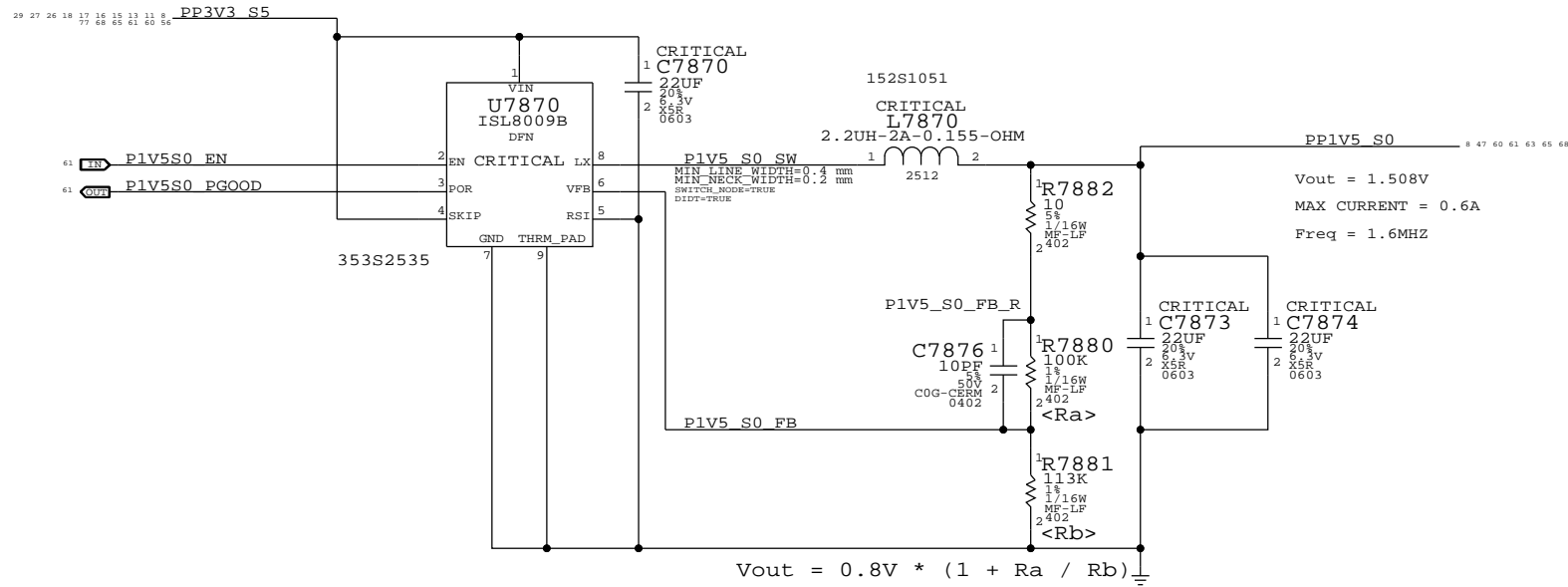
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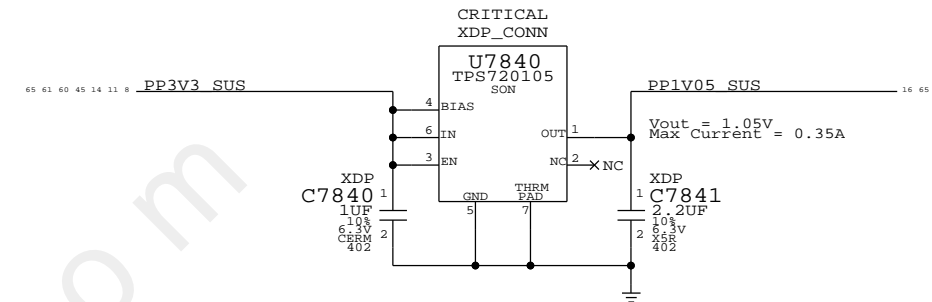
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### 1.5V S0 Switcher



### 1.05V SUS LDO

Cougar Point requires JTAG pull-ups to be powered at 1.05V when SUS suspend well is active. Pull-ups (3) must be 51 ohms to support XDP (not required in production). 70mA is required to support pull-ups. Alternative is strong voltage dividers (200/100) to 3.3V S5, which burns 100mW in all S-states.



www.chinafix.com

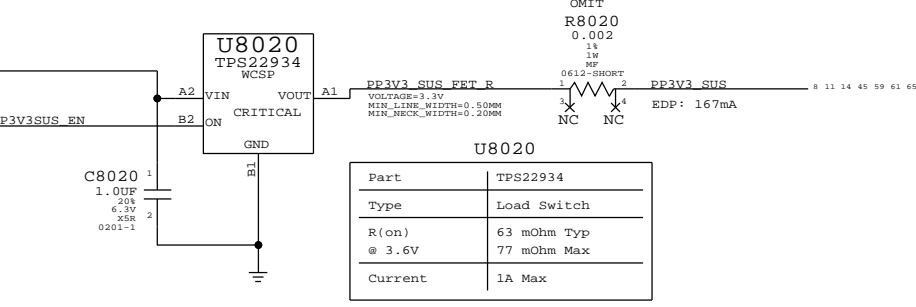
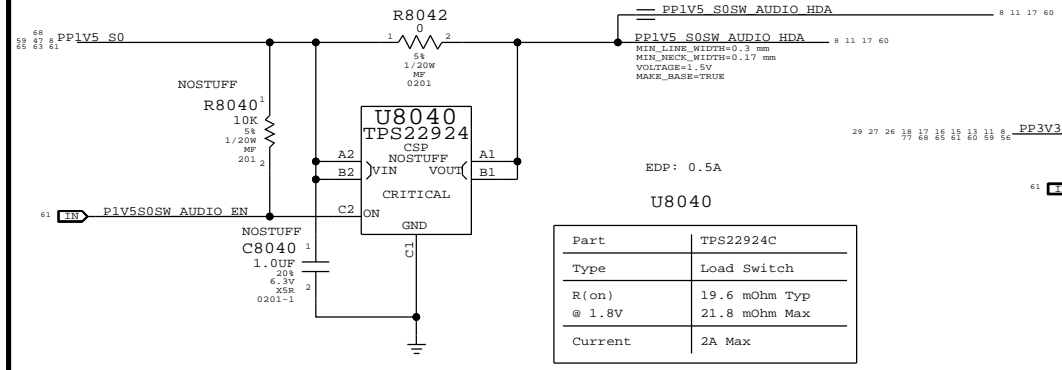
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Misc Power Supplies			
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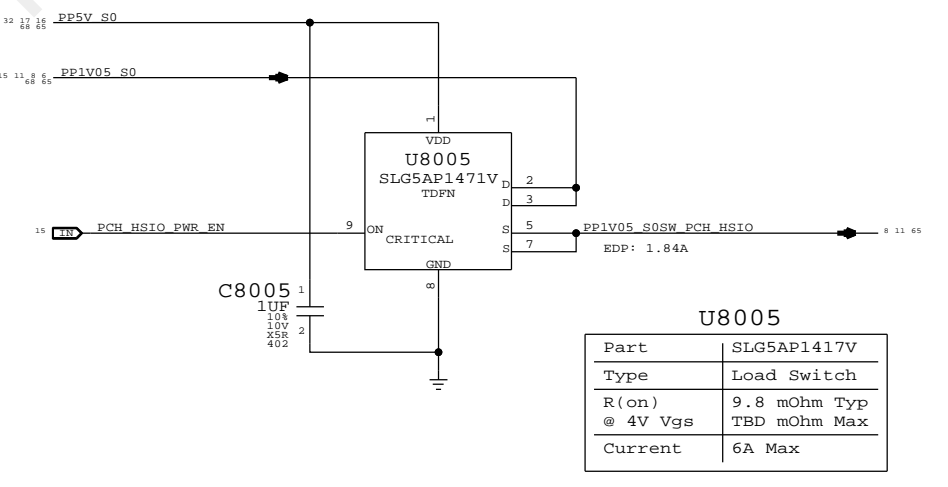
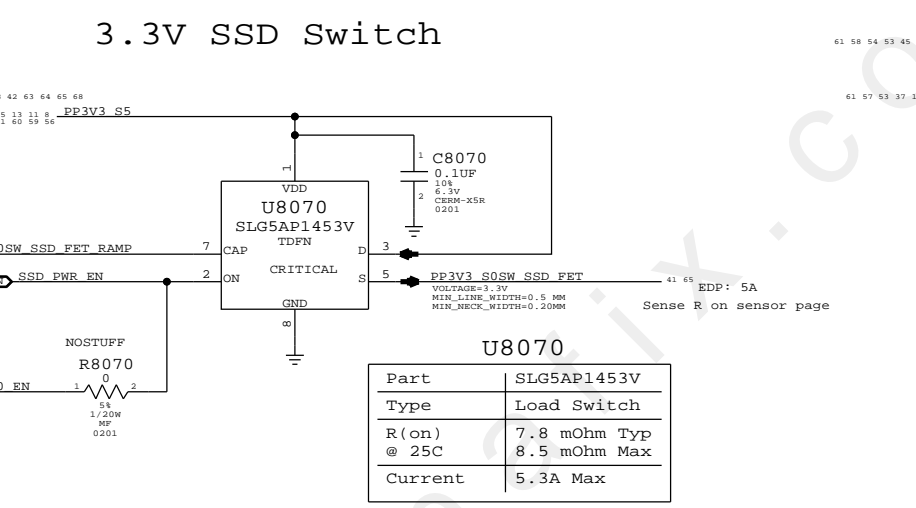
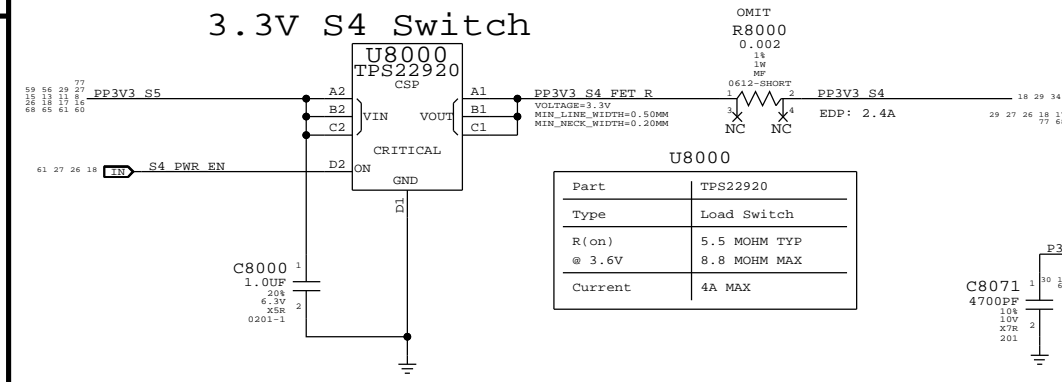
### 1.5V S0 Audio Switch (BYPASSED)

Loading specs per J41/43\_PowerBudget\_Riviera\_rev0.99e

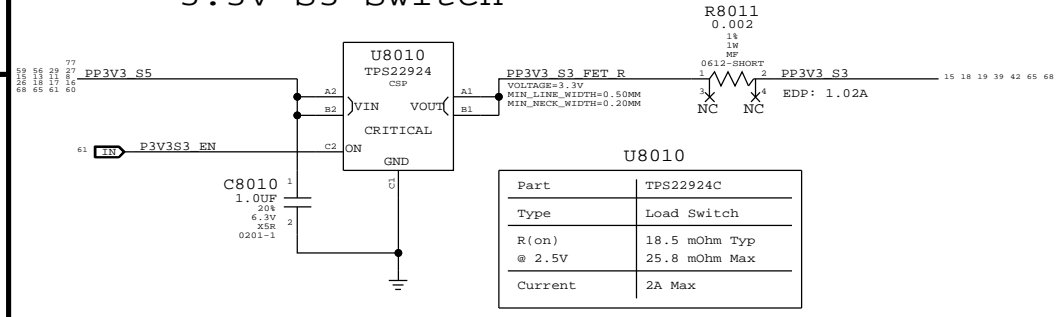
### 3.3V SUS Switch



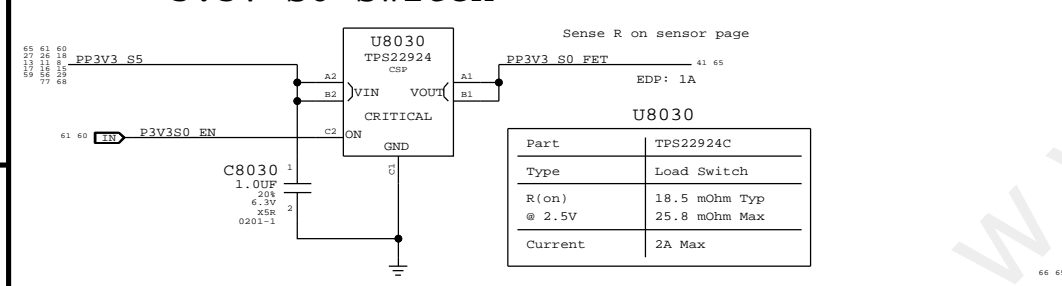
### 1.05V PCH HSIO Switch



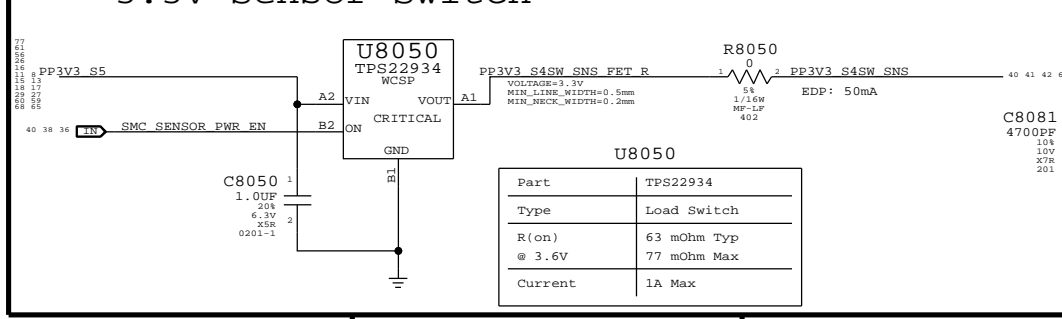
### 3.3V S3 Switch



### 3.3V S0 Switch

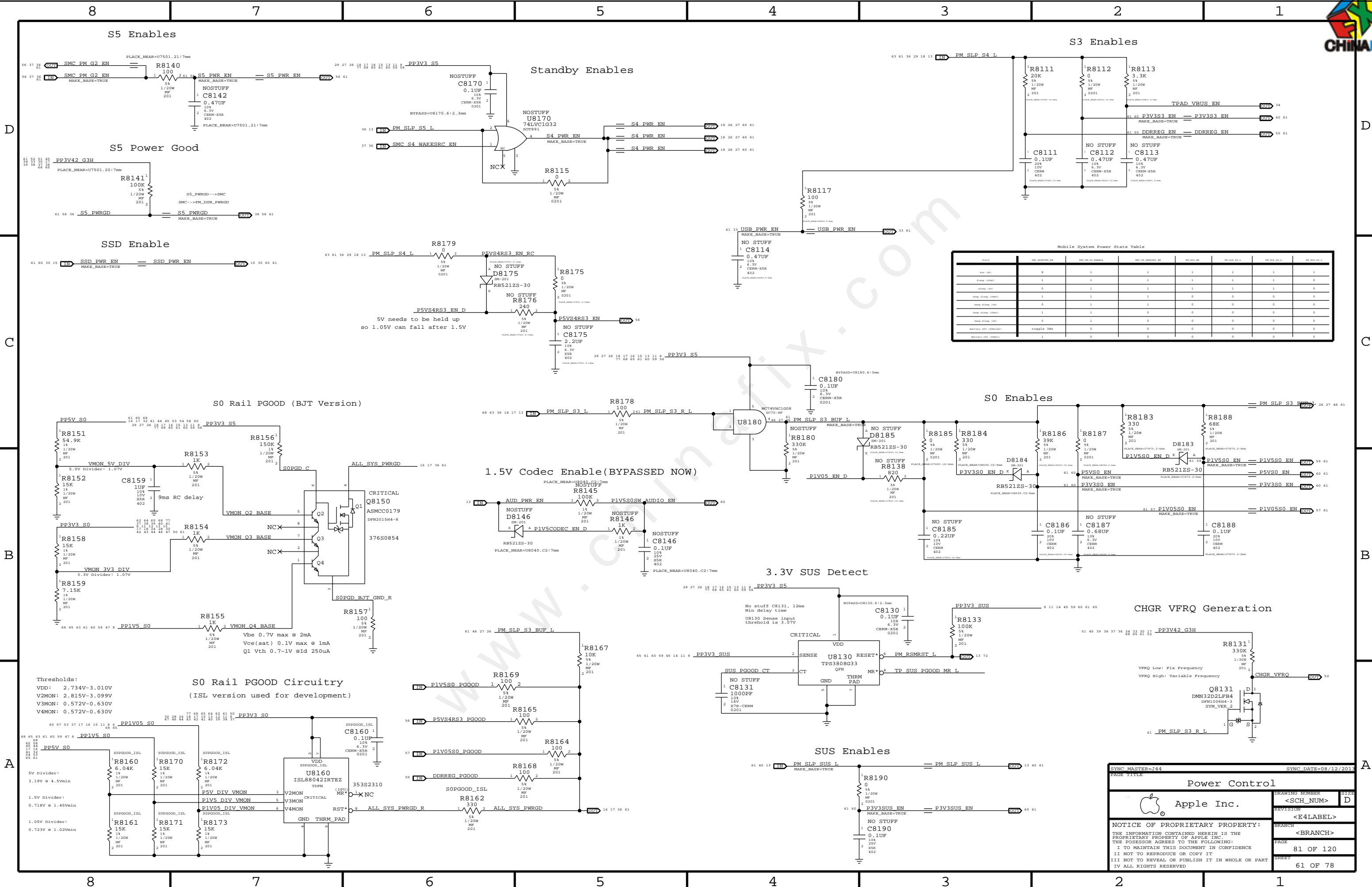


### 3.3V Sensor Switch



REMOVED THE ANALOG POWER GATE AS SLG5AP1471 SHOULD BE AVAILABLE BY THEN

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Power FETs	
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Mobile System Power State Table

State	PM_SLP_S4_L	PM_SLP_S3_L	PM_SLP_S3_R_L	PM_SLP_S3_BUF_L	PM_SLP_S3_BUF_R	PM_SLP_S3_R_R	PM_SLP_S3_L
Power Off	0	0	0	0	0	0	0
Standby (S4)	1	1	1	1	1	1	1
Standby (S3)	0	1	1	1	1	1	1
Deep Standby (S4)	1	1	1	0	0	0	0
Deep Standby (S3)	0	1	1	0	0	0	0
Deep Standby (S0)	1	1	1	0	0	0	0
Deep Standby (S1)	1	1	1	0	0	0	0
Deep Standby (S2)	1	1	1	0	0	0	0
Battery Off (Normal)	1	0	0	0	0	0	0
Battery Off (Critical)	1	0	0	0	0	0	0

Power Control

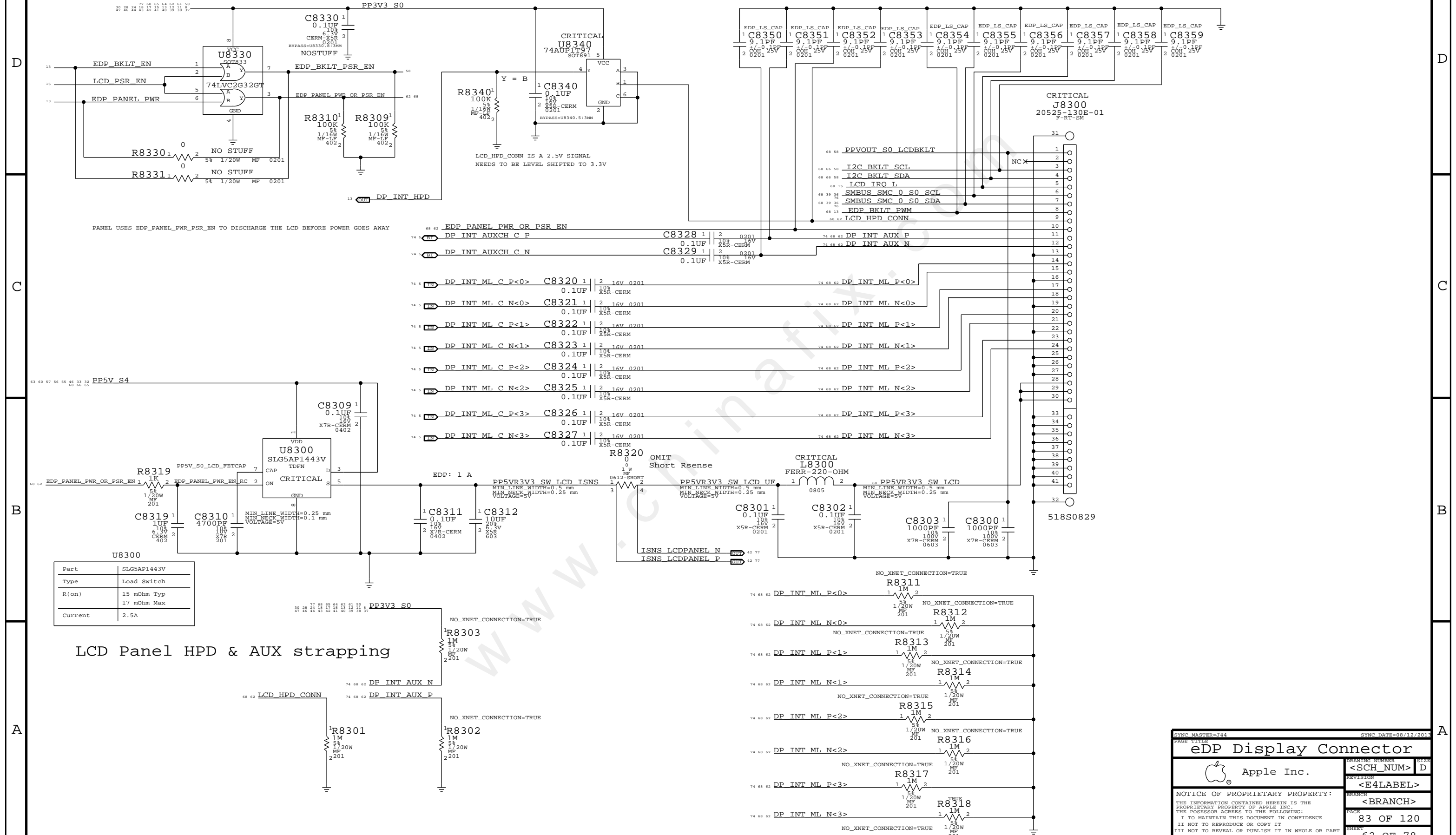
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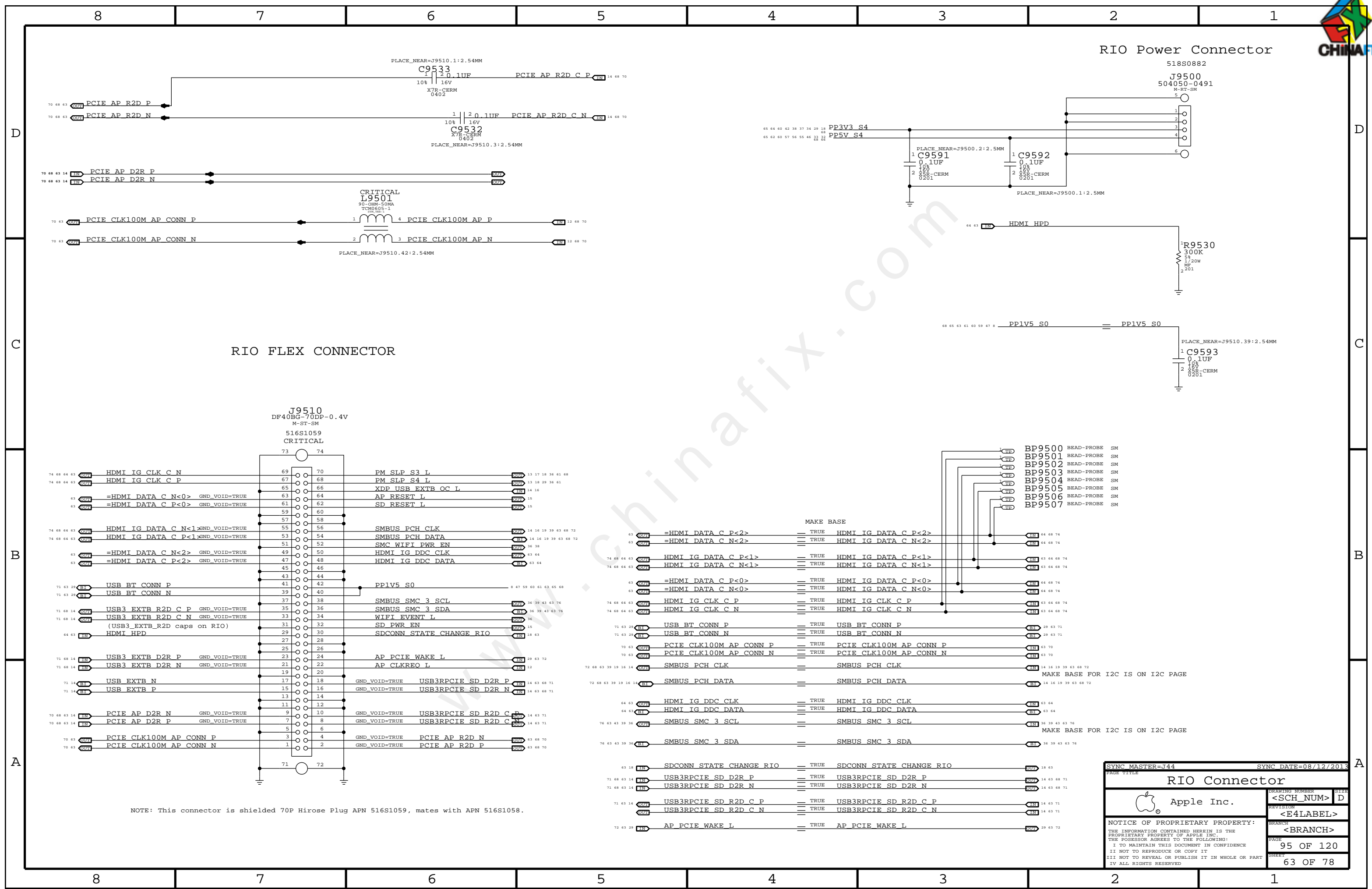
## LCD PANEL INTERFACE (eDP) NEEDS FINAL CHECK AGAINST UPDATE FOR NEW PANEL



Part	SLG5AP1443V
Type	Load Switch
R(on)	15 mOhm Typ 17 mOhm Max
Current	2.5A

### LCD Panel HPD & AUX strapping

SYNC MASTER=144		SYNC DATE=08/12/2013	
<b>eDP Display Connector</b>			
Apple Inc.		DRAWING NUMBER	SIZE
		<SCH_NUM>	D
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		PAGE	83 OF 120
		SHEET	62 OF 78



RIO FLEX CONNECTOR

RIO Power Connector

J9510  
DF40BG-70DP-0.4V  
M-ST-SM  
516S1059  
CRITICAL

74 68 64 63	HDMI IG CLK C N	69	70	PM SLP S3 L	13 17 18 36 61 68
74 68 64 63	HDMI IG CLK C P	67	68	PM SLP S4 L	13 18 29 36 61
63	=HDMI DATA C N<0> GND_VOID=TRUE	63	64	XDP USB EXTB OC L	14 16
63	=HDMI DATA C P<0> GND_VOID=TRUE	61	62	AP RESET L	15
		59	60	SD RESET L	15
		57	58		
74 68 64 63	HDMI IG DATA C N<1> GND_VOID=TRUE	55	56	SMBUS PCH CLK	14 16 19 39 63 68 72
74 68 64 63	HDMI IG DATA C P<1> GND_VOID=TRUE	53	54	SMBUS PCH DATA	14 16 19 39 63 68 72
		51	52	SMC WIFI PWR EN	36 38
63	=HDMI DATA C N<2> GND_VOID=TRUE	49	50	HDMI IG DDC CLK	63 64
63	=HDMI DATA C P<2> GND_VOID=TRUE	47	48	HDMI IG DDC DATA	63 64
		45	46		
		43	44		
71 63 21	USB BT CONN P	41	42	PPIV5 S0	8 47 59 60 61 63 65 68
71 63 21	USB BT CONN N	39	40		
		37	38	SMBUS SMC 3 SCL	36 39 43 63 76
71 68 14	USB3 EXTB R2D C P GND_VOID=TRUE	35	36	SMBUS SMC 3 SDA	36 39 43 63 76
71 68 14	USB3 EXTB R2D C N GND_VOID=TRUE	33	34	WIFI EVENT L	36
	(USB3_EXTB_R2D caps on RIO)	31	32	SD PWR EN	15
64 63	HDMI HPD	29	30	SDCONN STATE CHANGE RIO	18 63
		27	28		
		25	26		
71 68 14	USB3 EXTB D2R P GND_VOID=TRUE	23	24	AP PCIE WAKE L	29 63 72
71 68 14	USB3 EXTB D2R N GND_VOID=TRUE	21	22	AP CLKREQ L	12
		19	20		
71 14	USB EXTB N	17	18	GND_VOID=TRUE USB3RPCIE SD D2R P	14 63 68 71
71 14	USB EXTB P	15	16	GND_VOID=TRUE USB3RPCIE SD D2R N	14 63 68 71
		13	14		
		11	12		
70 68 63 14	PCIE AP D2R N GND_VOID=TRUE	9	10	GND_VOID=TRUE USB3RPCIE SD R2D C P	14 63 71
70 68 63 14	PCIE AP D2R P GND_VOID=TRUE	7	8	GND_VOID=TRUE USB3RPCIE SD R2D C N	14 63 71
		5	6		
70 63	PCIE CLK100M AP CONN P	3	4	GND_VOID=TRUE PCIE AP R2D N	63 68 70
70 63	PCIE CLK100M AP CONN N	1	2	GND_VOID=TRUE PCIE AP R2D P	63 68 70

63	=HDMI DATA C P<2>	TRUE	HDMI IG DATA C P<2>	64 68 74
63	=HDMI DATA C N<2>	TRUE	HDMI IG DATA C N<2>	64 68 74
74 68 64 63	HDMI IG DATA C P<1>	TRUE	HDMI IG DATA C P<1>	63 64 68 74
74 68 64 63	HDMI IG DATA C N<1>	TRUE	HDMI IG DATA C N<1>	63 64 68 74
63	=HDMI DATA C P<0>	TRUE	HDMI IG DATA C P<0>	64 68 74
63	=HDMI DATA C N<0>	TRUE	HDMI IG DATA C N<0>	64 68 74
74 68 64 63	HDMI IG CLK C P	TRUE	HDMI IG CLK C P	63 64 68 74
74 68 64 63	HDMI IG CLK C N	TRUE	HDMI IG CLK C N	63 64 68 74
71 63 21	USB BT CONN P	TRUE	USB BT CONN P	29 63 71
71 63 21	USB BT CONN N	TRUE	USB BT CONN N	29 63 71
70 63	PCIE CLK100M AP CONN P	TRUE	PCIE CLK100M AP CONN P	63 70
70 63	PCIE CLK100M AP CONN N	TRUE	PCIE CLK100M AP CONN N	63 70
72 68 63 39 16 14	SMBUS PCH CLK	TRUE	SMBUS PCH CLK	14 16 19 39 63 68 72
72 68 63 39 16 14	SMBUS PCH DATA	TRUE	SMBUS PCH DATA	14 16 19 39 63 68 72
64 63	HDMI IG DDC CLK	TRUE	HDMI IG DDC CLK	63 64
64 63	HDMI IG DDC DATA	TRUE	HDMI IG DDC DATA	63 64
76 63 43 39 36	SMBUS SMC 3 SCL	TRUE	SMBUS SMC 3 SCL	36 39 43 63 76
76 63 43 39 36	SMBUS SMC 3 SDA	TRUE	SMBUS SMC 3 SDA	36 39 43 63 76
63 18	SDCONN STATE CHANGE RIO	TRUE	SDCONN STATE CHANGE RIO	18 63
71 68 63 14	USB3RPCIE SD D2R P	TRUE	USB3RPCIE SD D2R P	14 63 68 71
71 68 63 14	USB3RPCIE SD D2R N	TRUE	USB3RPCIE SD D2R N	14 63 68 71
71 63 14	USB3RPCIE SD R2D C P	TRUE	USB3RPCIE SD R2D C P	14 63 71
71 63 14	USB3RPCIE SD R2D C N	TRUE	USB3RPCIE SD R2D C N	14 63 71
72 63 29	AP PCIE WAKE L	TRUE	AP PCIE WAKE L	29 63 72

NOTE: This connector is shielded 70P Hirose Plug APN 516S1059, mates with APN 516S1058.

SYNC MASTER=J44 SYNC DATE=08/12/2013

**RIO Connector**

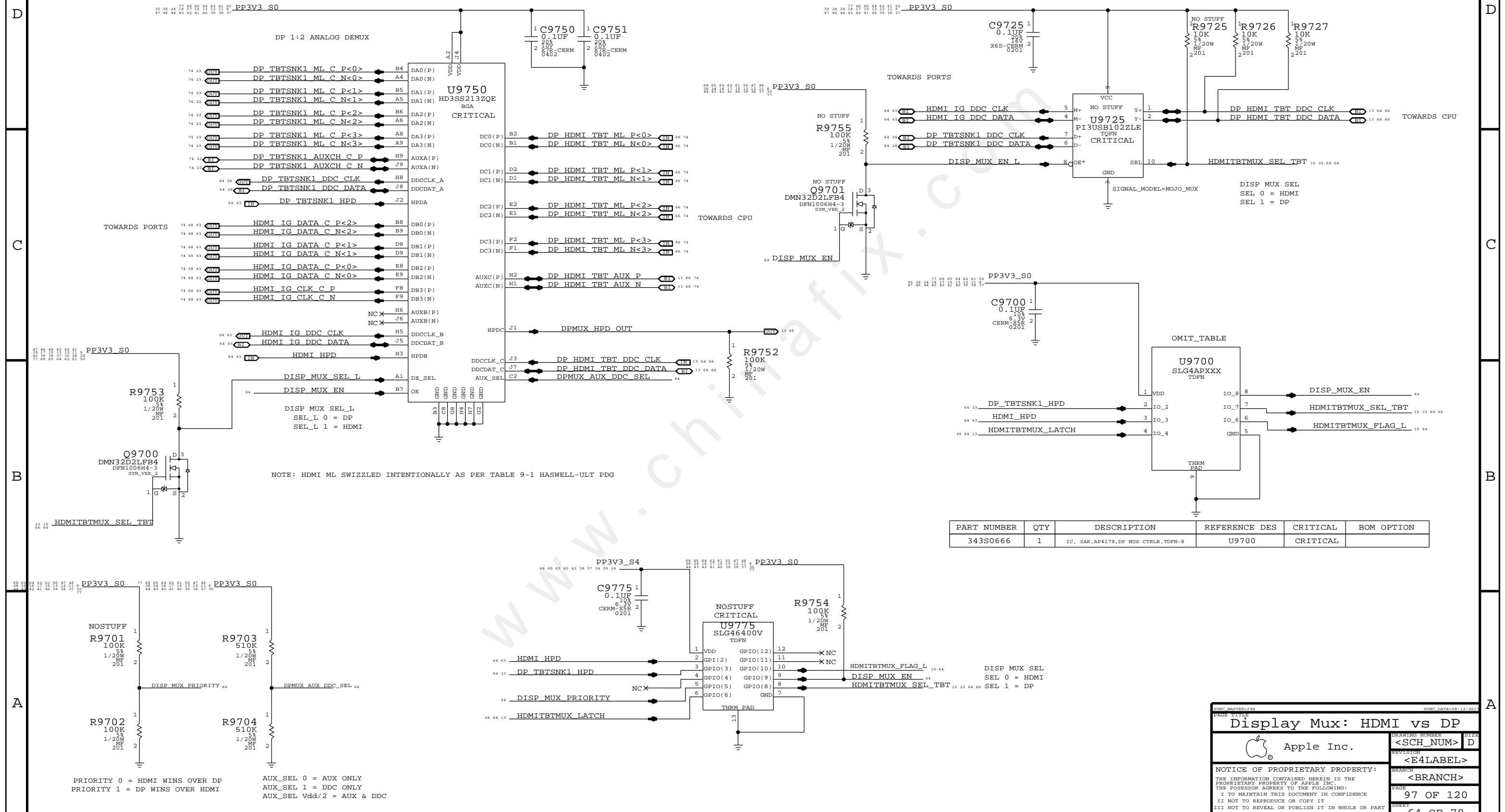
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DISPLAY MUX: DP OR HDMI



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
343S0666	1	IC, SAK,AP4179,DP MUX CTRLR,TDFN-8	U9700	CRITICAL	

Display Mux: HDMI vs DP

Apple Inc.

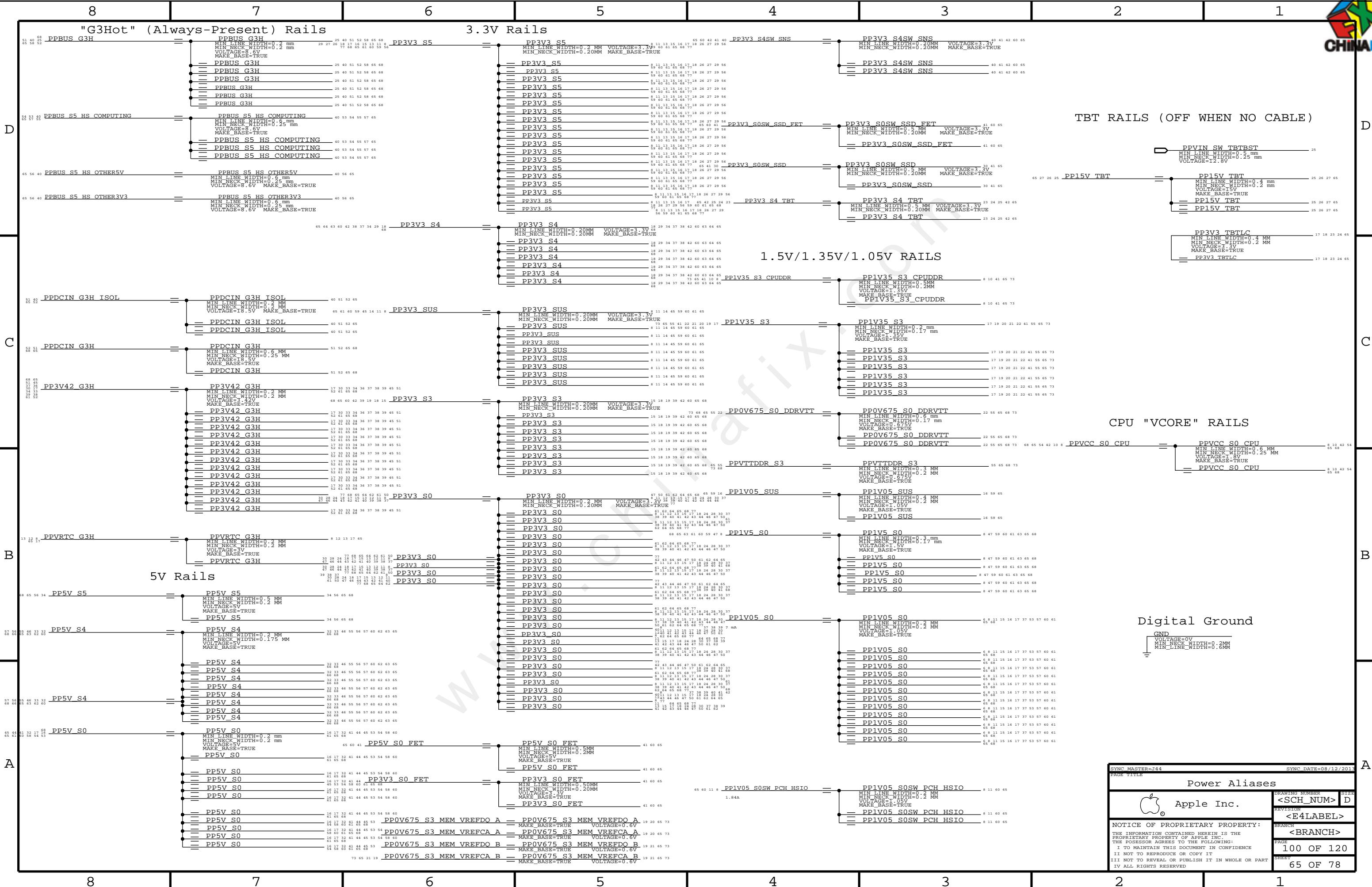
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PRIORITY 0 = HDMI WINS OVER DP  
 PRIORITY 1 = DP WINS OVER HDMI

AUX\_SEL 0 = AUX ONLY  
 AUX\_SEL 1 = DDC ONLY  
 AUX\_SEL Vdd/2 = AUX & DDC





TBT RAILS (OFF WHEN NO CABLE)

1.5V/1.35V/1.05V RAILS

CPU "Vcore" RAILS

Digital Ground

SYNC MASTER=144		SYNC DATE=08/12/2013	
PAGE TITLE		DRAWING NUMBER	
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8 7 6 5 4 3 2 1

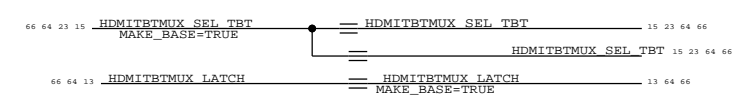
MEMORY ADDRESS/CTRL

HDMI VS TBT

MEM A A<0>	MEM A A<1>	MEM A A<2>	MEM A A<3>	MEM A A<4>	MEM A A<5>	MEM A A<6>	MEM A A<7>	MEM A A<8>	MEM A A<9>	MEM A A<10>	MEM A A<11>	MEM A A<12>	MEM A A<13>	MEM A A<14>
7	7	7	7	7	7	7	7	7	7	7	7	7	7	7
20	20	20	20	20	20	20	20	20	20	20	20	20	20	20
73	73	73	73	73	73	73	73	73	73	73	73	73	73	73

DP TBT SNK1 ML C P<0>	DP TBT SNK1 ML C N<0>	DP TBT SNK1 ML C P<1>	DP TBT SNK1 ML C N<1>	DP TBT SNK1 ML C P<2>	DP TBT SNK1 ML C N<2>	DP TBT SNK1 ML C P<3>	DP TBT SNK1 ML C N<3>	DP HDMI TBT AUX P	DP HDMI TBT AUX N	DP HDMI TBT DDC CLK	DP HDMI TBT DDC DATA	DPMUX HPD OUT
5	5	5	5	5	5	5	5	74	74	66	66	64
64	64	64	64	64	64	64	64	66	66	64	64	66
74	74	74	74	74	74	74	74	66	66	64	64	66

MEM B A<0>	MEM B A<1>	MEM B A<2>	MEM B A<3>	MEM B A<4>	MEM B A<5>	MEM B A<6>	MEM B A<7>	MEM B A<8>	MEM B A<9>	MEM B A<10>	MEM B A<11>	MEM B A<12>	MEM B A<13>	MEM B A<14>
7	7	7	7	7	7	7	7	7	7	7	7	7	7	7
21	21	21	21	21	21	21	21	21	21	21	21	21	21	21
22	22	22	22	22	22	22	22	22	22	22	22	22	22	22
73	73	73	73	73	73	73	73	73	73	73	73	73	73	73



EPD PANEL

I2C BKLT_SCL	I2C BKLT_SDA
68	68
66	66
62	62
58	58
66	66
62	62
58	58
66	66
62	62
58	58

MEM A ODT_CPU0	MEM A RAS_L	MEM A WE_L	MEM A CAS_L	MEM A BA<0>	MEM A BA<1>	MEM A BA<2>
66	66	66	66	66	66	66
22	22	22	22	22	22	22
7	7	7	7	7	7	7
22	22	22	22	22	22	22
66	66	66	66	66	66	66
20	20	20	20	20	20	20
73	73	73	73	73	73	73

UNUSED SIGNALS

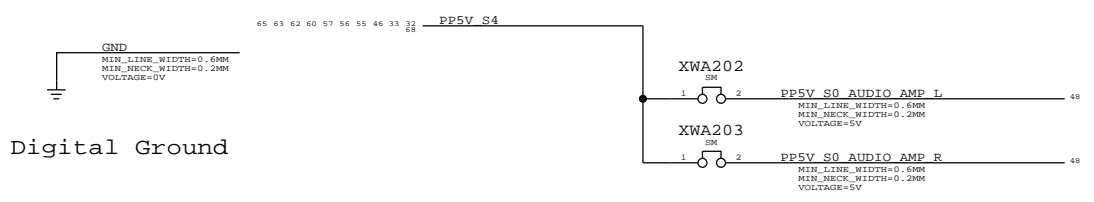
MEM B ODT_CPU0	MEM B RAS_L	MEM B WE_L	MEM B CAS_L	MEM B BA<0>	MEM B BA<1>	MEM B BA<2>
66	66	66	66	66	66	66
22	22	22	22	22	22	22
7	7	7	7	7	7	7
22	22	22	22	22	22	22
66	66	66	66	66	66	66
20	20	20	20	20	20	20
73	73	73	73	73	73	73

NC_PCIE_CLK100M_FWP	NC_PCIE_CLK100M_FWN	NC_PCIE_FW_D2RP	NC_PCIE_FW_D2RN	NC_PCIE_FW_R2D_CP	NC_PCIE_FW_R2D_CN	NC_PCIE_CLK100M_ENETSDP	NC_PCIE_CLK100M_ENETSDN	NC_USB_IRP	NC_USB_IRN	NC_USB_CAMERAP	NC_USB_CAMERAN	NC_USB_SDP	NC_USB_SDN	NC_HDA_SDIN1	NC_PCI_PME_L	NC_CLINK_CLK	NC_CLINK_DATA	NC_CLINK_RESET_L	
66	66	66	66	66	66	66	66	71	71	71	71	71	71	66	66	66	66	66	66
12	12	12	12	12	12	12	12	66	66	66	66	66	66	66	66	66	66	66	66
66	66	66	66	66	66	66	66	14	14	14	14	14	14	14	14	14	14	14	14
66	66	66	66	66	66	66	66	66	66	66	66	66	66	66	66	66	66	66	66
14	14	14	14	14	14	14	14	66	66	66	66	66	66	66	66	66	66	66	66
66	66	66	66	66	66	66	66	14	14	14	14	14	14	14	14	14	14	14	14
66	66	66	66	66	66	66	66	66	66	66	66	66	66	66	66	66	66	66	66
14	14	14	14	14	14	14	14	66	66	66	66	66	66	66	66	66	66	66	66

MEM_RESET_HSW_L
66
22
6
22
66

UNUSED MEMORY SIGNALS

NC_MEM_A_CLKN<1>	NC_MEM_A_CLKP<1>	MEM_A_CKE<2>	NC_MEM_A_CKE<3>	NC_MEM_B_CLKN<1>	NC_MEM_B_CLKP<1>	MEM_B_CKE<2>	NC_MEM_B_CKE<3>
66	66	66	66	66	66	66	66
7	7	7	7	7	7	7	7
22	22	22	22	22	22	22	22
66	66	66	66	66	66	66	66
20	20	20	20	20	20	20	20
73	73	73	73	73	73	73	73



SYNC MASTER=MASTER		SYNC DATE=MASTER	
Signal Aliases			
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8 7 6 5 4 3 2 1

D

D

Memory Bit/Byte Swizzle

C

C

B

B

A

A

MAKE\_BASE

73 68 7	TRUE	MEM A DQ<0>	==MEM A DQ<60>	20
73 68 7	TRUE	MEM A DQ<1>	==MEM A DQ<56>	20
73 68 7	TRUE	MEM A DQ<2>	==MEM A DQ<57>	20
73 68 7	TRUE	MEM A DQ<3>	==MEM A DQ<61>	20
73 68 7	TRUE	MEM A DQ<4>	==MEM A DQ<62>	20
73 68 7	TRUE	MEM A DQ<5>	==MEM A DQ<58>	20
73 68 7	TRUE	MEM A DQ<6>	==MEM A DQ<59>	20
73 68 7	TRUE	MEM A DQ<7>	==MEM A DQ<63>	20
73 68 7	TRUE	MEM A DQ<8>	==MEM A DQ<44>	20
73 68 7	TRUE	MEM A DQ<9>	==MEM A DQ<40>	20
73 68 7	TRUE	MEM A DQ<10>	==MEM A DQ<45>	20
73 68 7	TRUE	MEM A DQ<11>	==MEM A DQ<47>	20
73 68 7	TRUE	MEM A DQ<12>	==MEM A DQ<46>	20
73 68 7	TRUE	MEM A DQ<13>	==MEM A DQ<42>	20
73 68 7	TRUE	MEM A DQ<14>	==MEM A DQ<41>	20
73 68 7	TRUE	MEM A DQ<15>	==MEM A DQ<43>	20
73 68 7	TRUE	MEM A DQ<16>	==MEM A DQ<20>	20
73 68 7	TRUE	MEM A DQ<17>	==MEM A DQ<18>	20
73 68 7	TRUE	MEM A DQ<18>	==MEM A DQ<23>	20
73 68 7	TRUE	MEM A DQ<19>	==MEM A DQ<19>	20
73 68 7	TRUE	MEM A DQ<20>	==MEM A DQ<17>	20
73 68 7	TRUE	MEM A DQ<21>	==MEM A DQ<21>	20
73 68 7	TRUE	MEM A DQ<22>	==MEM A DQ<22>	20
73 68 7	TRUE	MEM A DQ<23>	==MEM A DQ<16>	20
73 68 7	TRUE	MEM A DQ<24>	==MEM A DQ<38>	20
73 68 7	TRUE	MEM A DQ<25>	==MEM A DQ<36>	20
73 68 7	TRUE	MEM A DQ<26>	==MEM A DQ<37>	20
73 68 7	TRUE	MEM A DQ<27>	==MEM A DQ<39>	20
73 68 7	TRUE	MEM A DQ<28>	==MEM A DQ<34>	20
73 68 7	TRUE	MEM A DQ<29>	==MEM A DQ<32>	20
73 68 7	TRUE	MEM A DQ<30>	==MEM A DQ<35>	20
73 68 7	TRUE	MEM A DQ<31>	==MEM A DQ<33>	20
73 68 7 20 7	TRUE	MEM A DQ<32>	==MEM A DQ<32>	7 20 67 68 73
73 68 7	TRUE	MEM A DQ<33>	==MEM A DQ<24>	20
73 68 7	TRUE	MEM A DQ<34>	==MEM A DQ<25>	20
73 68 7	TRUE	MEM A DQ<35>	==MEM A DQ<29>	20
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73 68 7	TRUE	MEM A DQ<37>	==MEM A DQ<26>	20
73 68 7	TRUE	MEM A DQ<38>	==MEM A DQ<31>	20
73 68 7	TRUE	MEM A DQ<39>	==MEM A DQ<27>	20
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73 68 7	TRUE	MEM A DQ<43>	==MEM A DQ<15>	20
73 68 7	TRUE	MEM A DQ<44>	==MEM A DQ<14>	20
73 68 7	TRUE	MEM A DQ<45>	==MEM A DQ<10>	20
73 68 7	TRUE	MEM A DQ<46>	==MEM A DQ<9>	20
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73 7	TRUE	MEM A DQS N<0>	==MEM A DQS N<7>	20
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73 7	TRUE	MEM A DQS N<1>	==MEM A DQS N<5>	20
73 7	TRUE	MEM A DQS P<2>	==MEM A DQS P<2>	20
73 7	TRUE	MEM A DQS N<2>	==MEM A DQS N<2>	20
73 7	TRUE	MEM A DQS P<3>	==MEM A DQS P<4>	20
73 7	TRUE	MEM A DQS N<3>	==MEM A DQS N<4>	20
73 7	TRUE	MEM A DQS P<4>	==MEM A DQS P<3>	20
73 7	TRUE	MEM A DQS N<4>	==MEM A DQS N<3>	20
73 7	TRUE	MEM A DQS P<5>	==MEM A DQS P<1>	20
73 7	TRUE	MEM A DQS N<5>	==MEM A DQS N<1>	20
73 67 20 7	TRUE	MEM A DQS P<6>	==MEM A DQS P<6>	7 20 67 73
73 67 20 7	TRUE	MEM A DQS N<6>	==MEM A DQS N<6>	7 20 67 73
73 7	TRUE	MEM A DQS P<7>	==MEM A DQS P<0>	20
73 7	TRUE	MEM A DQS N<7>	==MEM A DQS N<0>	20

MAKE\_BASE

73 68 7	TRUE	MEM B DQ<0>	==MEM B DQ<8>	21
73 68 7	TRUE	MEM B DQ<1>	==MEM B DQ<14>	21
73 68 7	TRUE	MEM B DQ<2>	==MEM B DQ<11>	21
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73 68 7	TRUE	MEM B DQ<15>	==MEM B DQ<31>	21
73 68 7	TRUE	MEM B DQ<16>	==MEM B DQ<5>	21
73 68 7	TRUE	MEM B DQ<17>	==MEM B DQ<1>	21
73 68 7	TRUE	MEM B DQ<18>	==MEM B DQ<6>	21
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73 68 7	TRUE	MEM B DQ<25>	==MEM B DQ<17>	21
73 68 7	TRUE	MEM B DQ<26>	==MEM B DQ<20>	21
73 68 7	TRUE	MEM B DQ<27>	==MEM B DQ<22>	21
73 68 7	TRUE	MEM B DQ<28>	==MEM B DQ<23>	21
73 68 7	TRUE	MEM B DQ<29>	==MEM B DQ<19>	21
73 68 7	TRUE	MEM B DQ<30>	==MEM B DQ<18>	21
73 68 7	TRUE	MEM B DQ<31>	==MEM B DQ<16>	21
73 68 7 21 7	TRUE	MEM B DQ<32>	==MEM B DQ<32>	7 21 67 68 73
73 68 7	TRUE	MEM B DQ<33>	==MEM B DQ<40>	21
73 68 7	TRUE	MEM B DQ<34>	==MEM B DQ<45>	21
73 68 7	TRUE	MEM B DQ<35>	==MEM B DQ<43>	21
73 68 7	TRUE	MEM B DQ<36>	==MEM B DQ<46>	21
73 68 7	TRUE	MEM B DQ<37>	==MEM B DQ<42>	21
73 68 7	TRUE	MEM B DQ<38>	==MEM B DQ<47>	21
73 68 7	TRUE	MEM B DQ<39>	==MEM B DQ<41>	21
73 68 7	TRUE	MEM B DQ<40>	==MEM B DQ<60>	21
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73 68 7	TRUE	MEM B DQ<50>	==MEM B DQ<32>	21
73 68 7	TRUE	MEM B DQ<51>	==MEM B DQ<33>	21
73 68 7	TRUE	MEM B DQ<52>	==MEM B DQ<35>	21
73 68 7	TRUE	MEM B DQ<53>	==MEM B DQ<36>	21
73 68 7	TRUE	MEM B DQ<54>	==MEM B DQ<34>	21
73 68 7	TRUE	MEM B DQ<55>	==MEM B DQ<39>	21
73 68 7	TRUE	MEM B DQ<56>	==MEM B DQ<51>	21
73 68 7	TRUE	MEM B DQ<57>	==MEM B DQ<53>	21
73 68 7	TRUE	MEM B DQ<58>	==MEM B DQ<48>	21
73 68 7	TRUE	MEM B DQ<59>	==MEM B DQ<55>	21
73 68 7	TRUE	MEM B DQ<60>	==MEM B DQ<50>	21
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73 68 7	TRUE	MEM B DQ<62>	==MEM B DQ<54>	21
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73 7	TRUE	MEM B DQS N<0>	==MEM B DQS N<1>	21
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73 7	TRUE	MEM B DQS N<1>	==MEM B DQS N<3>	21
73 7	TRUE	MEM B DQS P<2>	==MEM B DQS P<0>	21
73 7	TRUE	MEM B DQS N<2>	==MEM B DQS N<0>	21
73 7	TRUE	MEM B DQS P<3>	==MEM B DQS P<2>	21
73 7	TRUE	MEM B DQS N<3>	==MEM B DQS N<2>	21
73 7	TRUE	MEM B DQS P<4>	==MEM B DQS P<5>	21
73 7	TRUE	MEM B DQS N<4>	==MEM B DQS N<5>	21
73 7	TRUE	MEM B DQS P<5>	==MEM B DQS P<7>	21
73 7	TRUE	MEM B DQS N<5>	==MEM B DQS N<7>	21
73 67 21 7	TRUE	MEM B DQS P<6>	==MEM B DQS P<6>	7 21 67 73
73 67 21 7	TRUE	MEM B DQS N<6>	==MEM B DQS N<6>	7 21 67 73
73 7	TRUE	MEM B DQS P<7>	==MEM B DQS P<6>	21
73 7	TRUE	MEM B DQS N<7>	==MEM B DQS N<6>	21

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Memory Bit/Byte Swizzle

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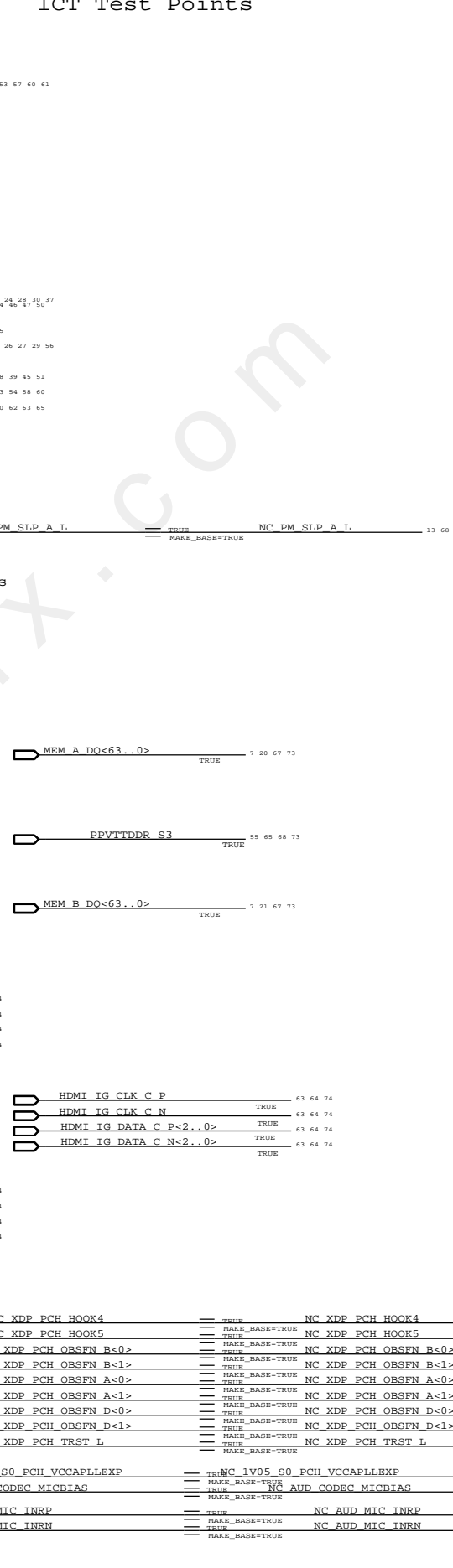
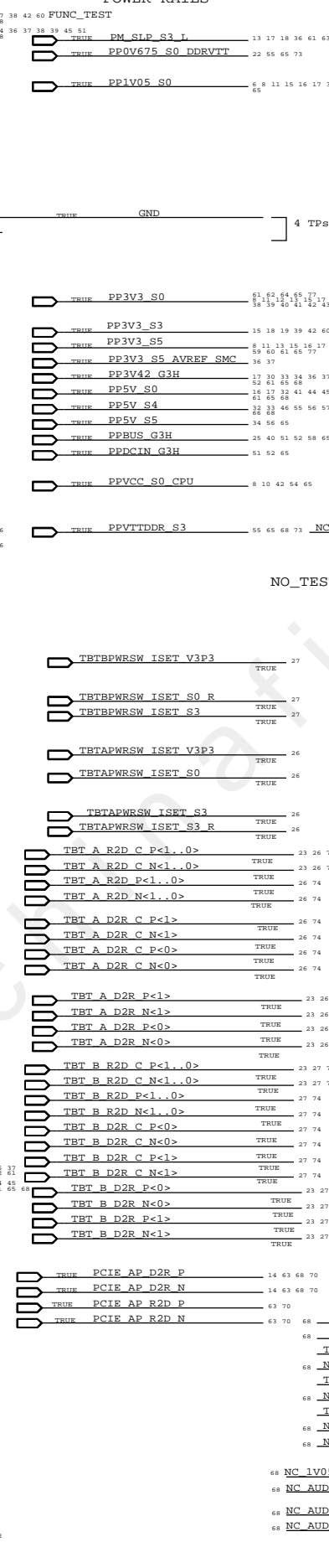
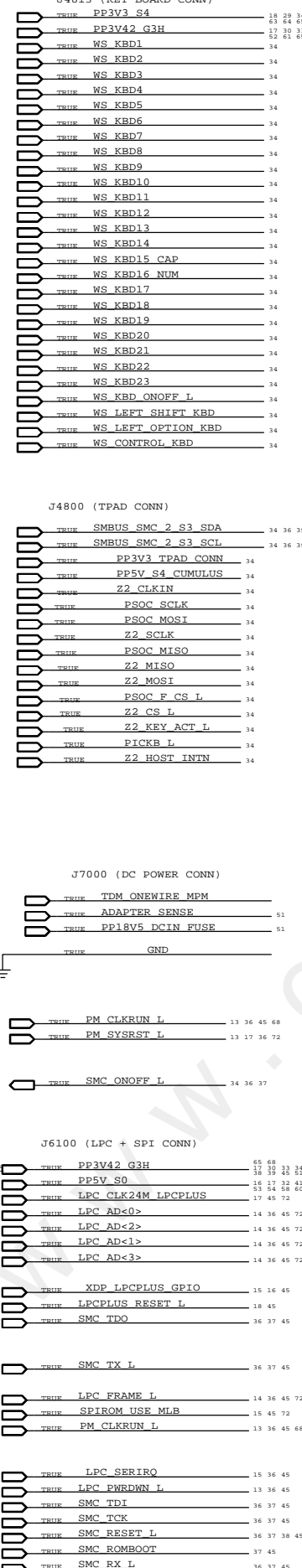
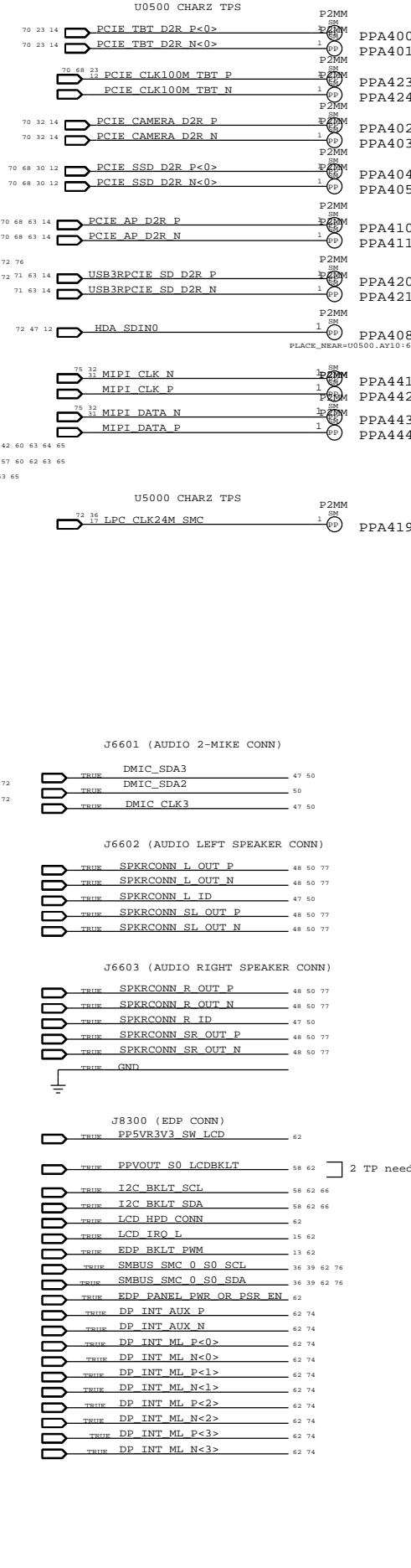
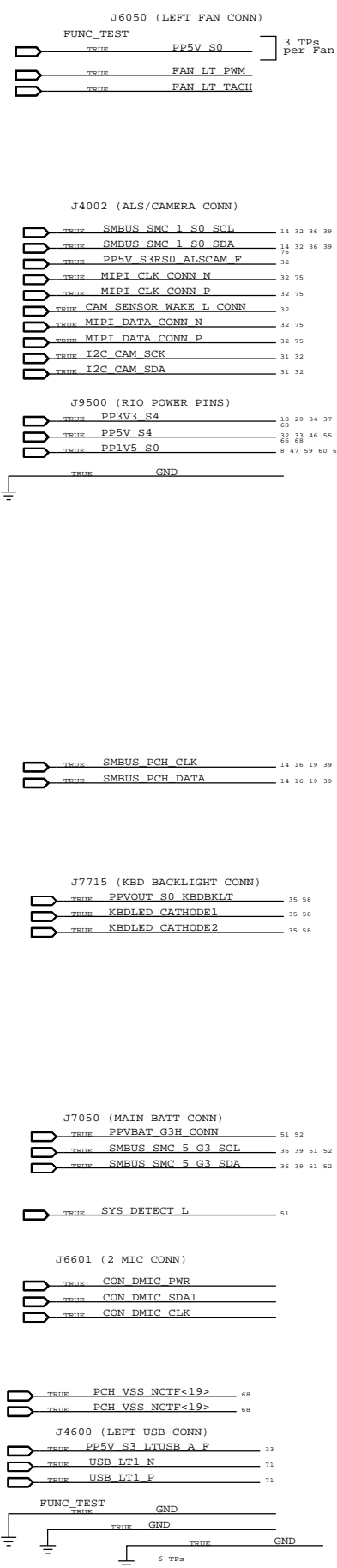
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Functional Test Points



Functional / ICT Test

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# J44 BOARD-SPECIFIC SPACING & PHYSICAL CONSTRAINTS

BOARD LAYERS			BOARD AREAS			BOARD UNITS (MIL OR MM)	ALLEGRO VERSION
TOP, ISL2, ISL3, ISL4, ISL5, ISL6, ISL7, ISL8, ISL9, ISL10, ISL11, BOTTOM			NO_TYPE, BGA, P65BGA, BGA_MEM			MM	16.5

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DEFAULT	*	Y	=45_OHM_SE	=45_OHM_SE	10 MM	0 MM	0 MM
STANDARD	*	Y	=DEFAULT	=DEFAULT	10 MM	=DEFAULT	=DEFAULT

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
50_OHM_SE	TOP, BOTTOM	Y	0.095 MM	0.095 MM			
50_OHM_SE	*	Y	0.066 MM	0.066 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
45_OHM_SE	TOP, BOTTOM	Y	0.116 MM	0.116 MM			
45_OHM_SE	*	Y	0.083 MM	0.083 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
40_OHM_SE	TOP, BOTTOM	Y	0.145 MM	0.095 MM			
40_OHM_SE	*	Y	0.102 MM	0.090 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
37_OHM_SE	TOP, BOTTOM	Y	0.165 MM	0.095 MM			
37_OHM_SE	*	Y	0.118 MM	0.090 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
27P4_OHM_SE	TOP, BOTTOM	Y	0.265 MM	0.095 MM			
27P4_OHM_SE	*	Y	0.186 MM	0.090 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
72_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
72_OHM_DIFF	ISL3, ISL4, ISL9, ISL10	Y	0.105 MM	0.105 MM		0.120 MM	0.120 MM
72_OHM_DIFF	ISL2, ISL11	Y	0.105 MM	0.105 MM		0.120 MM	0.120 MM
72_OHM_DIFF	TOP, BOTTOM	Y	0.146 MM	0.146 MM		0.120 MM	0.120 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
80_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
80_OHM_DIFF	ISL3, ISL4, ISL9, ISL10	Y	0.092 MM	0.092 MM		0.120 MM	0.120 MM
80_OHM_DIFF	ISL2, ISL11	Y	0.092 MM	0.092 MM		0.120 MM	0.120 MM
80_OHM_DIFF	TOP, BOTTOM	Y	0.125 MM	0.125 MM		0.155 MM	0.155 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
85_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
85_OHM_DIFF	ISL3, ISL4, ISL9, ISL10	Y	0.080 MM	0.080 MM		0.120 MM	0.120 MM
85_OHM_DIFF	ISL2, ISL11	Y	0.080 MM	0.080 MM		0.120 MM	0.120 MM
85_OHM_DIFF	TOP, BOTTOM	Y	0.105 MM	0.105 MM		0.125 MM	0.125 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
90_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
90_OHM_DIFF	ISL3, ISL4, ISL9, ISL10	Y	0.078 MM	0.078 MM		0.200 MM	0.200 MM
90_OHM_DIFF	ISL2, ISL11	Y	0.078 MM	0.078 MM		0.200 MM	0.200 MM
90_OHM_DIFF	TOP, BOTTOM	Y	0.101 MM	0.101 MM		0.180 MM	0.180 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
P65_BGA	*	Y	0.071MM	0.071MM		0.075MM	0.126MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1T01_DIFFPAIR	*	Y	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.1 MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
*	*	BGA	P072_SPACE
*	*	P65BGA	P075_SPACE

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DEFAULT	*	0.1 MM	?
STANDARD	*	=DEFAULT	?
P072_SPACE	*	0.071 MM	?
P075_SPACE	*	0.075 MM	?

### Stackup-Defined Spacing Rules

Note: Outer dielectric is 0.058 mm nominal,  
Inner dielectric is 0.053 mm nominal.

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1:1_SPACING	.	0.1 MM	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1x_DIELECTRIC	TOP, BOTTOM	0.058 MM	?
1x_DIELECTRIC	ISL3, ISL4, ISL9, ISL10	0.053 MM	?
1x_DIELECTRIC	ISL2, ISL11, ISL12, ISL13, ISL14	0.101 MM	?

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
*	P65BGA	P65_BGA

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CPU Signal Constraints

Table with 8 columns: PHYSICAL\_RULE\_SET, LAYER, ALLOW\_ROUTE\_ON\_LAYER?, MINIMUM LINE WIDTH, MINIMUM NECK WIDTH, MAXIMUM NECK LENGTH, DIFFPAIR PRIMARY GAP, DIFFPAIR NECK GAP. Rows include CPU\_45S and CPU\_27P4S.

Table with 4 columns: SPACING\_RULE\_SET, LAYER, LINE-TO-LINE SPACING, WEIGHT. Row includes CPU\_VCCSENSE.

Table with 7 columns: SPACING\_RULE\_SET, LAYER, LINE-TO-LINE SPACING, WEIGHT. Rows include CPU\_08MIL, CPU\_12MIL, CPU\_18MIL, CPU\_25MIL.

PCI Express Constraints

Table with 8 columns: PHYSICAL\_RULE\_SET, LAYER, ALLOW\_ROUTE\_ON\_LAYER?, MINIMUM LINE WIDTH, MINIMUM NECK WIDTH, MAXIMUM NECK LENGTH, DIFFPAIR PRIMARY GAP, DIFFPAIR NECK GAP. Rows include PCIE\_85D and CLK\_PCIE\_85D.

Table with 4 columns: SPACING\_RULE\_SET, LAYER, LINE-TO-LINE SPACING, WEIGHT. Rows include PCIE\_2SAME, PCIE\_TXRX, PCIE\_2OTHER, PCIE\_2CLK, PCIECLK\_2OTHER.

Table with 4 columns: NET\_SPACING\_TYPE1, NET\_SPACING\_TYPE2, AREA\_TYPE, SPACING\_RULE\_SET. Rows include PCIE\_\*, CLK\_PCIE, PCIE\_TX, PCIE\_RX.

CPU Signal Properties

Table with 4 columns: ELECTRICAL CONST SET, NET TYPE (PHYSICAL, SPACING), and signal names. Lists various CPU signals like XDP\_TCK0, CPU\_VCCST\_PWRGD, CPU\_PROCHOT, CPU\_CFG, CPU\_MEM\_RESET, CPU\_VCCSENSE.

PCI Express Properties

Table with 4 columns: ELECTRICAL CONST SET, NET TYPE (PHYSICAL, SPACING), and signal names. Lists various PCI Express signals like PCIE\_SSD\_D2R, PCIE\_TBT\_D2R, PCIE\_CAMERA\_D2R, PCIE\_CLK100M.

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### USB 2 Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCH_USB_RBIAS	*	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
USB_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT	SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	*	=4X_DIELECTRIC	?	USB	TOP,BOTTOM	=6X_DIELECTRIC	?
USB_RBIAS	*	=6X_DIELECTRIC	?	USB_RBIAS	TOP,BOTTOM	=10X_DIELECTRIC	?

### USB 3 Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
USB3_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT	SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB3_2SAME	*	=3X_DIELECTRIC	?	USB3_2SAME	TOP,BOTTOM	=4X_DIELECTRIC	?
USB3_TXRX	*	=6X_DIELECTRIC	?	USB3_TXRX	TOP,BOTTOM	=10X_DIELECTRIC	?
USB3_2OTHER	*	=4X_DIELECTRIC	?	USB3_2OTHER	TOP,BOTTOM	=6X_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
USB3_*	*	*	USB3_2OTHER
USB3_*	=SAME	*	USB3_2SAME
USB3_TX	*_RX	*	USB3_TXRX
USB3_RX	*_TX	*	USB3_TXRX

### System Clock Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_25M_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_25M	*	=5X_DIELECTRIC	?

### SATA Interface Constraints (Not Used)

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SATA_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF
SATA_45SE	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT	SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA_2SAME	*	=3X_DIELECTRIC	?	SATA_2SAME	TOP,BOTTOM	=4X_DIELECTRIC	?
SATA_TXRX	*	=6X_DIELECTRIC	?	SATA_TXRX	TOP,BOTTOM	=10X_DIELECTRIC	?
SATA_2OTHER	*	=4X_DIELECTRIC	?	SATA_2OTHER	TOP,BOTTOM	=6X_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
SATA_*	*	*	SATA_2OTHER
SATA_*	=SAME	*	SATA_2SAME
SATA_TX	*_RX	*	SATA_TXRX
SATA_RX	*_TX	*	SATA_TXRX

### USB Constraints

ELECTRICAL CONST SET	NET TYPE			
	PHYSICAL	SPACING		
USB_BT	USB_85D	USB	USB BT P	14 29
USB_BT	USB_85D	USB	USB BT N	14 29
USB_BT	USB_85D	USB	USB BT CONN P	29 63
USB_BT	USB_85D	USB	USB BT CONN N	29 63
USB_EXTA	USB_85D	USB	USB EXTA P	14 33
USB_EXTA	USB_85D	USB	USB EXTA N	14 33
DEFAULT	DEFAULT	DEFAULT	SMC DEBUGPRT RX L	33 36 37
DEFAULT	DEFAULT	DEFAULT	SMC DEBUGPRT TX L	33 36 37
USB_EXTA	USB_85D	USB	USB2 EXTA MUXED P	33
USB_EXTA	USB_85D	USB	USB2 EXTA MUXED N	33
USB_EXTA	USB_85D	USB	USB2 EXTA MUXED F P	33
USB_EXTA	USB_85D	USB	USB2 EXTA MUXED F N	33
USB_EXTA	USB_85D	USB	USB LT1 P	68
USB_EXTA	USB_85D	USB	USB LT1 N	68
USB_EXTB	USB_85D	USB	USB EXTB P	14 63
USB_EXTB	USB_85D	USB	USB EXTB N	14 63
USB_TPAD	USB_85D	USB	USB TPAD P	14 34
USB_TPAD	USB_85D	USB	USB TPAD N	14 34
USB_TPAD	USB_85D	USB	USB TPAD R P	34
USB_TPAD	USB_85D	USB	USB TPAD R N	34
USB3_EXTA_D2R	USB_85D	USB3_RX	USB3 EXTA D2R P	14 33 68
USB3_EXTA_D2R	USB_85D	USB3_RX	USB3 EXTA D2R N	14 33 68
USB3_EXTA_R2D	USB_85D	USB3_TX	USB3 EXTA R2D P	33
USB3_EXTA_R2D	USB_85D	USB3_TX	USB3 EXTA R2D N	33 68
USB3_EXTA_R2D	USB_85D	USB3_TX	USB3 EXTA R2D C P	14 33 68
USB3_EXTA_R2D	USB_85D	USB3_TX	USB3 EXTA R2D C N	14 33 68
USB3_EXTB_D2R	USB_85D	USB3_RX	USB3 EXTB D2R P	14 63 68
USB3_EXTB_D2R	USB_85D	USB3_RX	USB3 EXTB D2R N	14 63 68
USB3_EXTB_R2D	USB_85D	USB3_TX	USB3 EXTB R2D C P	14 63 68
USB3_EXTB_R2D	USB_85D	USB3_TX	USB3 EXTB R2D C N	14 63 68
USB3_SD_D2R	USB3_85D	USB3_RX	USB3RPCIE SD D2R P	14 63 68
USB3_SD_D2R	USB3_85D	USB3_RX	USB3RPCIE SD D2R N	14 63 68
USB3_SD_R2D	USB3_85D	USB3_TX	USB3RPCIE SD R2D C P	14 63
USB3_SD_R2D	USB3_85D	USB3_TX	USB3RPCIE SD R2D C N	14 63
USB_NC	USB_85D	USB	NC USB IRP	14 66
USB_NC	USB_85D	USB	NC USB IRN	14 66
USB_NC	USB_85D	USB	TP USB 5P	14
USB_NC	USB_85D	USB	TP USB 5N	14
USB_NC	USB_85D	USB	NC USB SDP	14 66
USB_NC	USB_85D	USB	NC USB SDN	14 66
USB_NC	USB_85D	USB	NC USB CAMERAP	14 66
USB_NC	USB_85D	USB	NC USB CAMERAN	14 66
PCH_USB_RBIAS	PCH_USB_RBIAS	USB_RBIAS	PCH USB RBIAS	14
SATA_85D	SATA_85D	SATA_RX	DUMMY SATA D2R P	
SATA_85D	SATA_85D	SATA_RX	DUMMY SATA D2R N	
SATA_85D	SATA_85D	SATA_TX	DUMMY SATA R2D P	
SATA_85D	SATA_85D	SATA_TX	DUMMY SATA R2D N	
SYSCLK_CLK25M	CLK_25M_45S	CLK_25M	SYSCLK CLK25M X1	17
SYSCLK_CLK25M	CLK_25M_45S	CLK_25M	SYSCLK CLK25M X2	17
SYSCLK_CLK25M	CLK_25M_45S	CLK_25M	SYSCLK CLK25M X2 R	17
SYSCLK_CLK25M_CAM	CLK_25M_45S	CLK_25M	SYSCLK CLK25M CAMERA	17 32
SYSCLK_CLK25M_CAM	CLK_25M_45S	CLK_25M	CLK25M CAM CLKP	31 32
SYSCLK_CLK25M_CAM	CLK_25M_45S	CLK_25M	CLK25M CAM XTALP R	32
SYSCLK_CLK25M_CAM	CLK_25M_45S	CLK_25M	CLK25M CAM XTALP	32
SYSCLK_CLK25M_CAM	CLK_25M_45S	CLK_25M	CLK25M CAM XTALN	32
SYSCLK_CLK25M_CAM	CLK_25M_45S	CLK_25M	CLK25M CAM CLKN	31 32
SYSCLK_CLK25M_TBT	CLK_25M_45S	CLK_25M	SYSCLK CLK25M TBT	17 23
SYSCLK_CLK25M_TBT	CLK_25M_45S	CLK_25M	SYSCLK CLK25M TBT R	23

Notes:  
This is here to keep the SATA rules.

SYNC MASTER=144		SYNC DATE=08/12/2013	
<b>USB Constraints</b>			
Apple Inc.	DRAWING NUMBER	SIZE	
	<SCH_NUM>	D	
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### LPC Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
LPC_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
CLK_LPC_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
LPC	*	6 MIL	?
CLK_LPC	*	8 MIL	?

### SMBus Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SMB_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SMB	*	=2x_DIELECTRIC	?

### HD Audio Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
HDA_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
HDA	*	=2x_DIELECTRIC	?

### SPI Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SPI_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SPI	*	8 MIL	?

### PCH Single Net Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCH_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
PCH_27P4S	*	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	7 MIL	7 MIL

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCH_12MIL	*	0.305 MM	?
PCH_15MIL	*	0.381 MM	?
PCH_18MIL	*	0.457 MM	?
PCH_20MIL	*	0.508 MM	?

### PCH Net Properties

ELECTRICAL CONST SET	NET TYPE		NET NAME	LENGTH
	PHYSICAL	SPACING		
LEC_AD	LEC_45S	LEC	LPC AD<3..0>	14 36 45 68
LEC_AD	LEC_45S	LEC	LPC FRAME L	14 36 45 68
LEC_CLK24M_SMC	CLK_LPC_45S	CLK_LPC	LPC CLK24M SMC R	12 17
LEC_CLK24M_SMC	CLK_LPC_45S	CLK_LPC	LPC CLK24M SMC	17 36 68
LEC_CLK24M_LPCPLUS	CLK_LPC_45S	CLK_LPC	LPC CLK24M LPCPLUS	17 45 68
LEC_CLK24M_LPCPLUS	CLK_LPC_45S	CLK_LPC	LPC CLK24M LPCPLUS R	12 17
SMBUS_PCH_CLK	SMB_45S	SMB	SMBUS PCH CLK	14 16 19 39 63 68
SMBUS_PCH_DATA	SMB_45S	SMB	SMBUS PCH DATA	14 16 19 39 63 68
SML_PCH_0_CLK	SMB_45S	SMB	SML PCH 0 CLK	14 39
SML_PCH_0_DATA	SMB_45S	SMB	SML PCH 0 DATA	14 39
SMBUS_SMC_1_S0_SCL	SMB_45S	SMB	SMBUS SMC 1 S0_SCL	14 12 36 39 63 68 76
SMBUS_SMC_1_S0_SDA	SMB_45S	SMB	SMBUS SMC 1 S0_SDA	14 12 36 39 63 68 76
HDA_BIT_CLK	HDA_45S	HDA	HDA BIT_CLK	12 47
HDA_BIT_CLK_R	HDA_45S	HDA	HDA BIT_CLK R	12
HDA_SYNC	HDA_45S	HDA	HDA SYNC	12 47
HDA_SYNC_R	HDA_45S	HDA	HDA SYNC R	12
HDA_RST	HDA_45S	HDA	HDA_RST R L	12
HDA_RST_L	HDA_45S	HDA	HDA_RST L	12 47
HDA_SDIN0	HDA_45S	HDA	HDA_SDIN0	12 47 68
CS4208_HDA_SDOUT0_R	HDA_45S	HDA	CS4208_HDA_SDOUT0 R	47
HDA_SDOUT	HDA_45S	HDA	HDA_SDOUT	12 47
HDA_SDOUT_R	HDA_45S	HDA	HDA_SDOUT R	12 17
SPI_ALT_CLK	SPT_45S	SPT	SPI ALT_CLK	45
SPI_CLK	SPT_45S	SPT	SPI_CLK	45
SPI_CLK_R	SPT_45S	SPT	SPI_CLK R	14 45
SPI_MLB_CLK	SPT_45S	SPT	SPI_MLB_CLK	45
SPI_SMC_CLK	SPT_45S	SPT	SPI_SMC_CLK	36 45
SPI_ALT_CS_L	SPT_45S	SPT	SPI_ALT_CS L	45
SPI_CS0_L	SPT_45S	SPT	SPI_CS0 L	45
SPI_CS0_R_L	SPT_45S	SPT	SPI_CS0 R L	14 45
SPI_MLB_CS_L	SPT_45S	SPT	SPI_MLB_CS L	45
SPI_SMC_CS_L	SPT_45S	SPT	SPI_SMC_CS L	36 45
SPI_ALT_MISO	SPT_45S	SPT	SPI_ALT_MISO	45
SPI_MISO	SPT_45S	SPT	SPI_MISO	14 45
SPI_MISO_R	SPT_45S	SPT	SPI_MISO R	45
SPI_MLB_MISO	SPT_45S	SPT	SPI_MLB_MISO	45
SPI_SMC_MISO	SPT_45S	SPT	SPI_SMC_MISO	36 45
SPI_ALT_MOSI	SPT_45S	SPT	SPI_ALT_MOSI	45
SPI_MOSI	SPT_45S	SPT	SPI_MOSI	45
SPI_MOSI_R	SPT_45S	SPT	SPI_MOSI R	14 45
SPI_MLB_MOSI	SPT_45S	SPT	SPI_MLB_MOSI	45
SPI_SMC_MOSI	SPT_45S	SPT	SPI_SMC_MOSI	36 45
SPI_IO<2>	SPT_45S	SPT	SPI_IO<2>	14 45
SPIROM_WP_L	SPT_45S	SPT	SPIROM_WP L	45
SPI_IO<3>	SPT_45S	SPT	SPI_IO<3>	14 45
SPIROM_HOLD_L	SPT_45S	SPT	SPIROM_HOLD L	45
SPIROM_USE_MLB	SPT_45S	SPT	SPIROM_USE_MLB	15 45 68
PCH_CLK32K_RTCX1	PCH_45S	PCH_15MTL	PCH_CLK32K_RTCX1	12 17
PCH_SRTCST_L	PCH_45S	PCH_15MTL	PCH_SRTCST L	12
RTC_RESET_L	PCH_45S	PCH_15MTL	RTC_RESET L	12
PM_THRMTRIP_L	PCH_45S	PCH_18MTL	PM_THRMTRIP L	15 37
PM_THRMTRIP_R_L	PCH_45S	PCH_18MTL	PM_THRMTRIP R L	37
PCH_INTRUDER_L	PCH_45S	PCH_15MTL	PCH_INTRUDER L	12
PCH_INTVRMEN	PCH_45S	PCH_15MTL	PCH_INTVRMEN	12
PCH_DSWVRMEN	PCH_45S	PCH_15MTL	PCH_DSWVRMEN	13
PM_RSMRST_L	PCH_45S	PCH_15MTL	PM_RSMRST L	13 61
PM_SYSRST_L	PCH_45S	PCH_15MTL	PM_SYSRST L	13 17 36 68
XDP_DBRESET_L	PCH_45S	PCH_15MTL	XDP_DBRESET L	16 17
PM_PCH_SYS_PWROK	PCH_45S	PCH_15MTL	PM_PCH_SYS_PWROK	13 16 17 36
XDP_SYS_PWROK	PCH_45S	PCH_15MTL	XDP_SYS_PWROK	16
SYS_PWROK_R	PCH_45S	PCH_15MTL	SYS_PWROK R	17
PM_PCH_PWROK	PCH_45S	PCH_15MTL	PM_PCH_PWROK	13 17
PM_S0_PGOOD	PCH_45S	PCH_15MTL	PM_S0_PGOOD	17
SMC_DELAYED_PWRGD	PCH_45S	PCH_15MTL	SMC_DELAYED_PWRGD	17 24 25 36 37
PM_DSW_PWRGD	PCH_45S	PCH_15MTL	PM_DSW_PWRGD	13 36
PM_PWRBTN_L	PCH_45S	PCH_15MTL	PM_PWRBTN L	13 16 36
XDP_CPU_PWRBTN_L	PCH_45S	PCH_15MTL	XDP_CPU_PWRBTN L	16
PCIE_WAKE_L	PCH_45S	PCH_15MTL	PCIE_WAKE L	13 29 31
AP_PCIE_WAKE_L	PCH_45S	PCH_15MTL	AP_PCIE_WAKE L	29 63
CAM_PCIE_WAKE_L	PCH_45S	PCH_15MTL	CAM_PCIE_WAKE L	31
TBT_CIO_PLUG_EVENT_L	PCH_45S	PCH_15MTL	TBT_CIO_PLUG_EVENT L	15 18 23
PCH_CLK24M_XTALIN	PCH_45S	PCH_20MTL	PCH_CLK24M_XTALIN	12 17
PCH_CLK24M_XTALOUT	PCH_45S	PCH_20MTL	PCH_CLK24M_XTALOUT	12 17
PCH_CLK24M_XTALOUT_R	PCH_45S	PCH_20MTL	PCH_CLK24M_XTALOUT R	17
PCH_PCIE_RCOMP	PCH_27P4S	PCH_12MTL	PCH_PCIE_RCOMP	14
PCH_OPI_COMP	PCH_27P4S	PCH_12MTL	PCH_OPI_COMP	15
PCH_SATA_RCOMP	PCH_27P4S	PCH_12MTL	PCH_SATA_RCOMP	12

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<b>PCH Constraints</b>			
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### Memory Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_40S	*	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=STANDARD	=STANDARD
MEM_72D	*	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF
MEM_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
MEM_80D	*	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF
MEM_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
MEM_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

### Spacing Rule Sets

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MEM_DATA2SELF	*	=2x_DIELECTRIC	?
MEM_DQS2OWNDATA	*	=2x_DIELECTRIC	?
MEM_CMD2CMD	*	=2x_DIELECTRIC	?
MEM_CMD2CTL	*	=2x_DIELECTRIC	?
MEM_CTL2CTL	*	=2x_DIELECTRIC	?
MEM_CLK2CLK	*	=4x_DIELECTRIC	?
MEM_2OTHERMEM	*	=4x_DIELECTRIC	?
MEM_2PWR	*	=2x_DIELECTRIC	?
MEM_2GND	*	=2x_DIELECTRIC	?
MEM_2OTHER	*	=6x_DIELECTRIC	?
MEM_CMD2CMD_BM	*	=2x_DIELECTRIC	?
MEM_CMD2CTL_BM	*	=2x_DIELECTRIC	?
MEM_CTL2CTL_BM	*	=2x_DIELECTRIC	?
MEM_12MIL	*	0.305 MM	?

### Memory Bus Spacing Group Assignments

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM*_DQBYTE*	*	*	MEM_2OTHER
MEM*_DQS*	*	*	MEM_2OTHER
MEM_CMD	*	*	MEM_2OTHER
MEM_CTL	*	*	MEM_2OTHER
MEM_CLK	*	*	MEM_2OTHER

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM*_DQBYTE*	=SAME	*	MEM_DATA2SELF

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CMD	MEM_CMD	*	MEM_CMD2CMD
MEM_CMD	MEM_CTL	*	MEM_CMD2CTL
MEM_CTL	MEM_CTL	*	MEM_CTL2CTL
MEM_CLK	MEM_CLK	*	MEM_CLK2CLK
MEM*	MEM*	*	MEM_2OTHERMEM
MEM_CMD	MEM_CMD	BGA_MEM	MEM_CMD2CMD_BM
MEM_CMD	MEM_CTL	BGA_MEM	MEM_CMD2CTL_BM
MEM_CTL	MEM_CTL	BGA_MEM	MEM_CTL2CTL_BM

### Haswell ULT Memory Down DDR3L 1x8 Length Matching

DDR3 Signal Group	Unit	Min Length	Max Length
CTLmax - CTLmin	mils	0	100
CTL to CLK	mils	CLK - 500	CLK + 500
CMDi to CMDj	mils	CMDj - 100	CMDj + 100
CMD to CLK	mils	CLK - 500	CLK + 500
(DQmax - DQmin) per byte	mils	0	250
(DQS - DQmax) per byte	mils	-100	150
DQS to DQS#	mils	-5	5
DQS to CLK (Rule 1)	mils	CLK - 6500	CLK + 500
Max(CLK-DQS) - Min(CLK-DQS)	mils	0	5500
CLK to CLK#	mils	-5	5

### Memory to Power Spacing

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_PWR	MEM_*	*	MEM_2PWR
MEM_PWR	*	*	DEFAULT

### Memory to GND Spacing

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
GND	MEM_*	*	MEM_2GND

### Memory Net Properties

ELECTRICAL CONST SET	NET TYPE		PROPERTY	VALUE
	PHYSICAL	SPACING		
MEM_A_CLK	MEM_72D	MEM_CLK	MEM A CLK P<0>	7 20 22
MEM_A_CLK	MEM_72D	MEM_CLK	MEM A CLK N<0>	7 20 22
MEM_A_CTL	MEM_40S	MEM_CTL	MEM A CKE<0>	7 20 22
MEM_A_CTL	MEM_40S	MEM_CTL	MEM A CS L<0>	7 20 22
MEM_A_ODT0	MEM_40S	MEM_CTL	MEM A ODT<0>	20 22
MEM_A_CMD	MEM_40S	MEM_CMD	MEM A A<15..0>	7 20 22 66
MEM_A_CMD	MEM_40S	MEM_CMD	MEM A BA<2..0>	7 20 22 66
MEM_A_CMD	MEM_40S	MEM_CMD	MEM A RAS L	7 20 22 66
MEM_A_CMD	MEM_40S	MEM_CMD	MEM A CAS L	7 20 22 66
MEM_A_CMD	MEM_40S	MEM_CMD	MEM A WE L	7 20 22 66
MEM_A_DQBYTE0	MEM_45S	MEM_A_DQBYTE_0	MEM A DQ<7..0>	7 67 68
MEM_A_DQBYTE1	MEM_45S	MEM_A_DQBYTE_1	MEM A DQ<15..8>	7 67 68
MEM_A_DQBYTE2	MEM_45S	MEM_A_DQBYTE_2	MEM A DQ<23..16>	7 67 68
MEM_A_DQBYTE3	MEM_45S	MEM_A_DQBYTE_3	MEM A DQ<31..24>	7 67 68
MEM_A_DQBYTE4	MEM_45S	MEM_A_DQBYTE_4	MEM A DQ<39..32>	7 20 67 68
MEM_A_DQBYTE5	MEM_45S	MEM_A_DQBYTE_5	MEM A DQ<47..40>	7 67 68
MEM_A_DQBYTE6	MEM_45S	MEM_A_DQBYTE_6	MEM A DQ<55..48>	7 67 68
MEM_A_DQBYTE7	MEM_45S	MEM_A_DQBYTE_7	MEM A DQ<63..56>	7 67 68
MEM_A_DQS0	MEM_80D	MEM_A_DQS_0	MEM A DQS P<0>	7 67
MEM_A_DQS0	MEM_80D	MEM_A_DQS_0	MEM A DQS N<0>	7 67
MEM_A_DQS1	MEM_80D	MEM_A_DQS_1	MEM A DQS P<1>	7 67
MEM_A_DQS1	MEM_80D	MEM_A_DQS_1	MEM A DQS N<1>	7 67
MEM_A_DQS2	MEM_80D	MEM_A_DQS_2	MEM A DQS P<2>	7 67
MEM_A_DQS2	MEM_80D	MEM_A_DQS_2	MEM A DQS N<2>	7 67
MEM_A_DQS3	MEM_80D	MEM_A_DQS_3	MEM A DQS P<3>	7 67
MEM_A_DQS3	MEM_80D	MEM_A_DQS_3	MEM A DQS N<3>	7 67
MEM_A_DQS4	MEM_80D	MEM_A_DQS_4	MEM A DQS P<4>	7 67
MEM_A_DQS4	MEM_80D	MEM_A_DQS_4	MEM A DQS N<4>	7 67
MEM_A_DQS5	MEM_80D	MEM_A_DQS_5	MEM A DQS P<5>	7 67
MEM_A_DQS5	MEM_80D	MEM_A_DQS_5	MEM A DQS N<5>	7 67
MEM_A_DQS6	MEM_80D	MEM_A_DQS_6	MEM A DQS P<6>	7 20 67
MEM_A_DQS6	MEM_80D	MEM_A_DQS_6	MEM A DQS N<6>	7 20 67
MEM_A_DQS7	MEM_80D	MEM_A_DQS_7	MEM A DQS P<7>	7 67
MEM_A_DQS7	MEM_80D	MEM_A_DQS_7	MEM A DQS N<7>	7 67
MEM_B_CLK	MEM_72D	MEM_CLK	MEM B CLK P<0>	7 21 22
MEM_B_CLK	MEM_72D	MEM_CLK	MEM B CLK N<0>	7 21 22
MEM_B_CTL	MEM_40S	MEM_CTL	MEM B CKE<0>	7 21 22
MEM_B_CTL	MEM_40S	MEM_CTL	MEM B CS L<0>	7 21 22
MEM_B_ODT0	MEM_40S	MEM_CTL	MEM B ODT<0>	21 22
MEM_B_CMD	MEM_40S	MEM_CMD	MEM B A<15..0>	7 21 22 66
MEM_B_CMD	MEM_40S	MEM_CMD	MEM B BA<2..0>	7 21 22 66
MEM_B_CMD	MEM_40S	MEM_CMD	MEM B RAS L	7 21 22 66
MEM_B_CMD	MEM_40S	MEM_CMD	MEM B CAS L	7 21 22 66
MEM_B_CMD	MEM_40S	MEM_CMD	MEM B WE L	7 21 22 66
MEM_B_DQBYTE0	MEM_45S	MEM_B_DQBYTE_0	MEM B DQ<7..0>	7 67 68
MEM_B_DQBYTE1	MEM_45S	MEM_B_DQBYTE_1	MEM B DQ<15..8>	7 67 68
MEM_B_DQBYTE2	MEM_45S	MEM_B_DQBYTE_2	MEM B DQ<23..16>	7 67 68
MEM_B_DQBYTE3	MEM_45S	MEM_B_DQBYTE_3	MEM B DQ<31..24>	7 67 68
MEM_B_DQBYTE4	MEM_45S	MEM_B_DQBYTE_4	MEM B DQ<39..32>	7 21 67 68
MEM_B_DQBYTE5	MEM_45S	MEM_B_DQBYTE_5	MEM B DQ<47..40>	7 67 68
MEM_B_DQBYTE6	MEM_45S	MEM_B_DQBYTE_6	MEM B DQ<55..48>	7 67 68
MEM_B_DQBYTE7	MEM_45S	MEM_B_DQBYTE_7	MEM B DQ<63..56>	7 67 68
MEM_B_DQS0	MEM_80D	MEM_B_DQS_0	MEM B DQS P<0>	7 67
MEM_B_DQS0	MEM_80D	MEM_B_DQS_0	MEM B DQS N<0>	7 67
MEM_B_DQS1	MEM_80D	MEM_B_DQS_1	MEM B DQS P<1>	7 67
MEM_B_DQS1	MEM_80D	MEM_B_DQS_1	MEM B DQS N<1>	7 67
MEM_B_DQS2	MEM_80D	MEM_B_DQS_2	MEM B DQS P<2>	7 67
MEM_B_DQS2	MEM_80D	MEM_B_DQS_2	MEM B DQS N<2>	7 67
MEM_B_DQS3	MEM_80D	MEM_B_DQS_3	MEM B DQS P<3>	7 67
MEM_B_DQS3	MEM_80D	MEM_B_DQS_3	MEM B DQS N<3>	7 67
MEM_B_DQS4	MEM_80D	MEM_B_DQS_4	MEM B DQS P<4>	7 67
MEM_B_DQS4	MEM_80D	MEM_B_DQS_4	MEM B DQS N<4>	7 67
MEM_B_DQS5	MEM_80D	MEM_B_DQS_5	MEM B DQS P<5>	7 67
MEM_B_DQS5	MEM_80D	MEM_B_DQS_5	MEM B DQS N<5>	7 67
MEM_B_DQS6	MEM_80D	MEM_B_DQS_6	MEM B DQS P<6>	7 21 67
MEM_B_DQS6	MEM_80D	MEM_B_DQS_6	MEM B DQS N<6>	7 21 67
MEM_B_DQS7	MEM_80D	MEM_B_DQS_7	MEM B DQS P<7>	7 67
MEM_B_DQS7	MEM_80D	MEM_B_DQS_7	MEM B DQS N<7>	7 67
MEM_PWR			PP1V35 S3	17 19 20 21 22 41 55 65
MEM_PWR			PP1V35 S3 CPUDDR	8 10 41 65
MEM_PWR			PP0V675 S0 DDRVTT	22 55 65 68
MEM_PWR			PPVTDDR S3	55 65 68
MEM_12MIL			CPU DIMMA VREFD0	7 19
MEM_12MIL			CPU DIMMA VREFD0 A ISOL	19
MEM_12MIL			CPU DIMMB VREFD0	7 19
MEM_12MIL			CPU DIMMB VREFD0 B ISOL	19
MEM_12MIL			CPU DIMM VREFCA	7 19
MEM_12MIL			CPU DIMM VREFCA A ISOL	19
MEM_12MIL			CPU DIMM VREFCA B ISOL	19
MEM_12MIL			PP0V675 S3 MEM VREFD0 A	19 20 65
MEM_12MIL			PP0V675 S3 MEM VREFD0 B	19 21 65
MEM_12MIL			PP0V675 S3 MEM VREFCA A	19 20 65
MEM_12MIL			PP0V675 S3 MEM VREFCA B	19 21 65

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Memory Constraints

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### Thunderbolt, DP, HDMI Constraints

#### Thunderbolt SPI Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
TBT_SPI_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
TBT_SPI	*	=2x_DIELECTRIC	?

#### Thunderbolt & DisplayPort Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
TBTDP_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
TBTDP_2SAME	*	=3x_DIELECTRIC	?
TBTDP_TXRX	*	=6x_DIELECTRIC	?
TBTDP_2OTHER	*	=4x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
TBTDP_2SAME	TOP,BOTTOM	=4x_DIELECTRIC	?
TBTDP_TXRX	TOP,BOTTOM	=10x_DIELECTRIC	?
TBTDP_2OTHER	TOP,BOTTOM	=6x_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
TBTDP_*	*	*	TBTDP_2OTHER
TBTDP_*	=SAME	*	TBTDP_2SAME
TBTDP_TX	*_RX	*	TBTDP_TXRX
TBTDP_RX	*_TX	*	TBTDP_TXRX

#### DisplayPort & HDMI Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DP_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF
HDMI_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DP_2SAME	*	=3x_DIELECTRIC	?
DP_2OTHER	*	=4x_DIELECTRIC	?
HDMICLK_2OTHER	*	=7x_DIELECTRIC	?
HDMICLK_2DPHDMI	*	=4x_DIELECTRIC	?
HDMIDATA_2SAME	*	=3x_DIELECTRIC	?
HDMIDATA_2OTHER	*	=4x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DP_2SAME	TOP,BOTTOM	=4x_DIELECTRIC	?
DP_2OTHER	TOP,BOTTOM	=6x_DIELECTRIC	?
HDMICLK_2OTHER	TOP,BOTTOM	=10x_DIELECTRIC	?
HDMICLK_2DPHDMI	TOP,BOTTOM	=6x_DIELECTRIC	?
HDMIDATA_2SAME	TOP,BOTTOM	=4x_DIELECTRIC	?
HDMIDATA_2OTHER	TOP,BOTTOM	=6x_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
HDMI_DATA	*	*	HDMIDATA_2OTHER
HDMI_DATA	=SAME	*	HDMIDATA_2SAME
HDMI_DATA	TBTDP_TX	*	HDMIDATA_2SAME
HDMI_DATA	TBTDP_RX	*	TBTDP_TXRX
HDMI_CLK	*	*	HDMICLK_2OTHER
HDMI_CLK	HDMI_DATA	*	HDMICLK_2DPHDMI
HDMI_CLK	DISPLAYPORT	*	HDMICLK_2DPHDMI
HDMI_CLK	TBTDP_TX	*	HDMICLK_2DPHDMI

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
DISPLAYPORT	*	*	DP_2OTHER
DISPLAYPORT	=SAME	*	DP_2SAME
DISPLAYPORT	HDMI_DATA	*	DP_2SAME
DISPLAYPORT	TBTDP_TX	*	DP_2SAME
DISPLAYPORT	TBTDP_RX	*	TBTDP_TXRX

DisplayPort/TMDS intra-pair matching should be 0.127mm. Inter-pair matching should be within 2.54cm. Max Length 241.3mm.  
 DisplayPort AUX CH intra-pair matching should be 0.127mm. Max length 330.2mm.  
 SOURCE: Calpella SFF DG Rev 1.5 (407364) and Family GPU DG-04202-001-v04.  
 MAX LENGTH OF DISPLAYPORT/TMDS TRACES: 13 INCHES.

ELECTRICAL CONST SET	NET TYPE		
	PHYSICAL	SPACING	
	DP_85D	DISPLAYPORT	DP TBTSRC ML C P<3..0>
	DP_85D	DISPLAYPORT	DP TBTSRC ML C N<3..0>
	DP_85D	DISPLAYPORT	DP TBTSRC AUXCH C P
	DP_85D	DISPLAYPORT	DP TBTSRC AUXCH C N
	TBT_SPI_45S	TBT_SPI	TBT SPI CLK
	TBT_SPI_45S	TBT_SPI	TBT SPI MOSI
	TBT_SPI_45S	TBT_SPI	TBT SPI MISO
	TBT_SPI_45S	TBT_SPI	TBT SPI CS L
	DP_85D	DISPLAYPORT	DP HDMI TBT ML P<3..0>
	DP_85D	DISPLAYPORT	DP HDMI TBT ML N<3..0>
	DP_85D	DISPLAYPORT	DP HDMI TBT AUX P
	DP_85D	DISPLAYPORT	DP HDMI TBT AUX N
	HDMI_85D	HDMI_CLK	HDMI IG CLK C P
	HDMI_85D	HDMI_CLK	HDMI IG CLK C N
	HDMI_85D	HDMI_DATA	HDMI IG DATA C P<2..0>
	HDMI_85D	HDMI_DATA	HDMI IG DATA C N<2..0>

Only used on hosts supporting Thunderbolt video-in

### Thunderbolt, DP, HDMI Net Properties

ELECTRICAL CONST SET	NET TYPE		
	PHYSICAL	SPACING	
	TBTDP_85D	TBTDP_TX	TBT A R2D C P<1..0>
	TBTDP_85D	TBTDP_TX	TBT A R2D C N<1..0>
	TBTDP_85D	TBTDP_TX	TBT A R2D P<1..0>
	TBTDP_85D	TBTDP_TX	TBT A R2D N<1..0>
	DP_85D	DISPLAYPORT	DP TBTPA ML C P<1>
	DP_85D	DISPLAYPORT	DP TBTPA ML C N<1>
	DP_85D	DISPLAYPORT	DP TBTPA ML P<1>
	DP_85D	DISPLAYPORT	DP TBTPA ML N<1>
	DP_85D	DISPLAYPORT	DP A LSX ML P<1>
	DP_85D	DISPLAYPORT	DP A LSX ML N<1>
	DP_85D	DISPLAYPORT	DP TBTPA ML C P<3>
	DP_85D	DISPLAYPORT	DP TBTPA ML C N<3>
	DP_85D	DISPLAYPORT	DP TBTPA ML P<3>
	DP_85D	DISPLAYPORT	DP TBTPA ML N<3>
	TBTDP_85D	TBTDP_RX	TBT A D2R C P<0>
	TBTDP_85D	TBTDP_RX	TBT A D2R C N<0>
	TBTDP_85D	TBTDP_RX	TBT A D2R P<0>
	TBTDP_85D	TBTDP_RX	TBT A D2R N<0>
	TBTDP_85D	TBTDP_RX	TBT A D2R C P<1>
	TBTDP_85D	TBTDP_RX	TBT A D2R C N<1>
	TBTDP_85D	TBTDP_RX	TBT A D2R P<1>
	TBTDP_85D	TBTDP_RX	TBT A D2R N<1>
	TBTDP_85D	TBTDP_RX	TBT A D2R1 AUXDDC P
	TBTDP_85D	TBTDP_RX	TBT A D2R1 AUXDDC N
	DP_85D	DISPLAYPORT	DP TBTPA AUXCH C P
	DP_85D	DISPLAYPORT	DP TBTPA AUXCH C N
	DP_85D	DISPLAYPORT	DP TBTPA AUXCH P
	DP_85D	DISPLAYPORT	DP TBTPA AUXCH N
	TBTDP_85D	TBTDP_TX	TBT B R2D C P<1..0>
	TBTDP_85D	TBTDP_TX	TBT B R2D C N<1..0>
	TBTDP_85D	TBTDP_TX	TBT B R2D P<1..0>
	TBTDP_85D	TBTDP_TX	TBT B R2D N<1..0>
	DP_85D	DISPLAYPORT	DP TBTPB ML C P<1>
	DP_85D	DISPLAYPORT	DP TBTPB ML C N<1>
	DP_85D	DISPLAYPORT	DP TBTPB ML P<1>
	DP_85D	DISPLAYPORT	DP TBTPB ML N<1>
	DP_85D	DISPLAYPORT	DP B LSX ML P<1>
	DP_85D	DISPLAYPORT	DP B LSX ML N<1>
	DP_85D	DISPLAYPORT	DP TBTPB ML C P<3>
	DP_85D	DISPLAYPORT	DP TBTPB ML C N<3>
	DP_85D	DISPLAYPORT	DP TBTPB ML P<3>
	DP_85D	DISPLAYPORT	DP TBTPB ML N<3>
	TBTDP_85D	TBTDP_RX	TBT B D2R C P<0>
	TBTDP_85D	TBTDP_RX	TBT B D2R C N<0>
	TBTDP_85D	TBTDP_RX	TBT B D2R P<0>
	TBTDP_85D	TBTDP_RX	TBT B D2R N<0>
	TBTDP_85D	TBTDP_RX	TBT B D2R C P<1>
	TBTDP_85D	TBTDP_RX	TBT B D2R C N<1>
	TBTDP_85D	TBTDP_RX	TBT B D2R P<1>
	TBTDP_85D	TBTDP_RX	TBT B D2R N<1>
	TBTDP_85D	TBTDP_RX	TBT B D2R1 AUXDDC P
	TBTDP_85D	TBTDP_RX	TBT B D2R1 AUXDDC N
	DP_85D	DISPLAYPORT	DP TBTPB AUXCH C P
	DP_85D	DISPLAYPORT	DP TBTPB AUXCH C N
	DP_85D	DISPLAYPORT	DP TBTPB AUXCH P
	DP_85D	DISPLAYPORT	DP TBTPB AUXCH N
	DP_85D	DISPLAYPORT	DP TBTSNK0 ML C P<3..0>
	DP_85D	DISPLAYPORT	DP TBTSNK0 ML C N<3..0>
	DP_85D	DISPLAYPORT	DP TBTSNK0 ML P<3..0>
	DP_85D	DISPLAYPORT	DP TBTSNK0 ML N<3..0>
	DP_85D	DISPLAYPORT	DP TBTSNK0 AUXCH C P
	DP_85D	DISPLAYPORT	DP TBTSNK0 AUXCH C N
	DP_85D	DISPLAYPORT	DP TBTSNK0 AUXCH P
	DP_85D	DISPLAYPORT	DP TBTSNK0 AUXCH N
	DP_85D	DISPLAYPORT	DP TBTSNK1 ML C P<3..0>
	DP_85D	DISPLAYPORT	DP TBTSNK1 ML C N<3..0>
	DP_85D	DISPLAYPORT	DP TBTSNK1 ML P<3..0>
	DP_85D	DISPLAYPORT	DP TBTSNK1 ML N<3..0>
	DP_85D	DISPLAYPORT	DP TBTSNK1 AUXCH C P
	DP_85D	DISPLAYPORT	DP TBTSNK1 AUXCH C N
	DP_85D	DISPLAYPORT	DP TBTSNK1 AUXCH P
	DP_85D	DISPLAYPORT	DP TBTSNK1 AUXCH N
	DP_85D	DISPLAYPORT	DP INT ML C P<3..0>
	DP_85D	DISPLAYPORT	DP INT ML C N<3..0>
	DP_85D	DISPLAYPORT	DP INT ML P<3..0>
	DP_85D	DISPLAYPORT	DP INT ML N<3..0>
	DP_85D	DISPLAYPORT	DP INT AUXCH C P
	DP_85D	DISPLAYPORT	DP INT AUXCH C N
	DP_85D	DISPLAYPORT	DP INT AUXCH P
	DP_85D	DISPLAYPORT	DP INT AUXCH N

Notes:  
 AUX and DDC was removed from DISPLAYPORT or TBTDP\_RX/TX because it's not high speed, and to save routing space.

Only used on dual-port hosts.

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### Camera Net Properties

ELECTRICAL CONST SET	NET TYPE			
	PHYSICAL	SPACING		
S2_MEM_CLK	S2_MEM_85D	S2_MEM_CLK	MEM CAM CLK P	31 32
S2_MEM_CLK	S2_MEM_85D	S2_MEM_CLK	MEM CAM CLK N	31 32
S2_MEM_CKE	S2_MEM_45S	S2_MEM_CTRL	MEM CAM CKE	31 32
S2_MEM_CS	S2_MEM_45S	S2_MEM_CTRL	MEM CAM CS L	31 32
S2_MEM_CMD	S2_MEM_45S	S2_MEM_CTRL	MEM CAM ODT	32
S2_MEM_CMD	S2_MEM_45S	S2_MEM_CTRL	MEM CAM CAS L	31 32
S2_MEM_CMD	S2_MEM_45S	S2_MEM_CTRL	MEM CAM RAS L	31 32
S2_MEM_CMD	S2_MEM_45S	S2_MEM_CMD	MEM CAM WE L	31 32
S2_MEM_CMD	S2_MEM_45S	S2_MEM_CMD	MEM CAM BA<0>	31 32
S2_MEM_CMD	S2_MEM_45S	S2_MEM_CMD	MEM CAM BA<1>	31 32
S2_MEM_CMD	S2_MEM_45S	S2_MEM_CMD	MEM CAM BA<2>	31 32
S2_MEM_DQS0	S2_MEM_85D	S2_MEM_DQS0	MEM CAM DQS P<0>	31 32
S2_MEM_DQS0	S2_MEM_85D	S2_MEM_DQS0	MEM CAM DQS N<0>	31 32
S2_MEM_DQS1	S2_MEM_85D	S2_MEM_DQS1	MEM CAM DQS P<1>	31 32
S2_MEM_DQS1	S2_MEM_85D	S2_MEM_DQS1	MEM CAM DQS N<1>	31 32
S2_MEM_DATA_0	S2_MEM_45S	S2_MEM_DATA0	MEM CAM DM<0>	31 32
S2_MEM_DATA_1	S2_MEM_45S	S2_MEM_DATA1	MEM CAM DM<1>	31 32
S2_MEM_A	S2_MEM_45S	S2_MEM_CMD	MEM CAM A<14..0>	31 32
S2_MEM_DATA_0	S2_MEM_45S	S2_MEM_DATA0	MEM CAM DO<7..0>	31 32
S2_MEM_DATA_1	S2_MEM_45S	S2_MEM_DATA1	MEM CAM DO<15..8>	31 32
MIPI_DATA_S2	MIPI_85D	MIPI_DATA	MIPI DATA P	31 32 68
MIPI_DATA_S2	MIPI_85D	MIPI_DATA	MIPI DATA N	31 32 68
MIPI_DATA_S2	MIPI_85D	MIPI_DATA	MIPI DATA CONN P	32 68
MIPI_DATA_S2	MIPI_85D	MIPI_DATA	MIPI DATA CONN N	32 68
MIPI_CLK_S2	MIPI_85D	CLK MIPI	MIPI CLK P	31 32 68
MIPI_CLK_S2	MIPI_85D	CLK MIPI	MIPI CLK N	31 32 68
MIPI_CLK_S2	MIPI_85D	CLK MIPI	MIPI CLK CONN P	32 68
MIPI_CLK_S2	MIPI_85D	CLK MIPI	MIPI CLK CONN N	32 68
S2_MEM_PWR			P1V35 CAM	31 32
S2_MEM_PWR			P0V675 CAM VREF	31 32
S2_MEM_PWR			P0V675 MEM CAM VREFCA	32
S2_MEM_PWR			P0V675 MEM CAM VREFDO	32

### MIPI Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MIPI_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MIPI_2OTHER	*	=4X_DIELECTRIC	?
MIPI_2CLK	*	=6X_DIELECTRIC	?
MIPICLK_2OTHER	*	=7X_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MIPI_2OTHER	TOP,BOTTOM	=6X_DIELECTRIC	?
MIPI_2CLK	TOP,BOTTOM	=8X_DIELECTRIC	?
MIPICLK_2OTHER	TOP,BOTTOM	=10X_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MIPI_DATA	*	*	MIPI_2OTHER
MIPI_DATA	CLK_MIPI	*	MIPI_2CLK
CLK_MIPI	*	*	MIPICLK_2OTHER

### Memory Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
S2_MEM_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
S2_MEM_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

### Spacing Rule Sets

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
S2_DATA2SELF	*	=2x_DIELECTRIC	?
S2_DQS2OWNDATA	*	=2x_DIELECTRIC	?
S2_CMD2CMD	*	=2x_DIELECTRIC	?
S2_CMD2CTRL	*	=2x_DIELECTRIC	?
S2_CTRL2CTRL	*	=2x_DIELECTRIC	?
S2_2OTHERMEM	*	=4x_DIELECTRIC	?
S2MEM_2PWR	*	=2x_DIELECTRIC	?
S2MEM_2GND	*	=2x_DIELECTRIC	?
S2MEM_2OTHER	*	=6x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
S2_DATA2SELF	TOP,BOTTOM	=4x_DIELECTRIC	?
S2_DQS2OWNDATA	TOP,BOTTOM	=4x_DIELECTRIC	?
S2_CMD2CMD	TOP,BOTTOM	=4x_DIELECTRIC	?
S2_CMD2CTRL	TOP,BOTTOM	=4x_DIELECTRIC	?
S2_CTRL2CTRL	TOP,BOTTOM	=4x_DIELECTRIC	?
S2_2OTHERMEM	TOP,BOTTOM	=6x_DIELECTRIC	?
S2MEM_2PWR	TOP,BOTTOM	=4x_DIELECTRIC	?
S2MEM_2GND	TOP,BOTTOM	=4x_DIELECTRIC	?
S2MEM_2OTHER	TOP,BOTTOM	=10x_DIELECTRIC	?

### Memory Bus Spacing Group Assignments

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
S2_MEM_DATA*	*	*	S2MEM_2OTHER
S2_MEM_DQS*	*	*	S2MEM_2OTHER
S2_MEM_CMD	*	*	S2MEM_2OTHER
S2_MEM_CTRL	*	*	S2MEM_2OTHER
S2_MEM_CLK	*	*	S2MEM_2OTHER
S2_MEM_DATA*	=SAME	*	S2_DATA2SELF
S2_MEM_CMD	S2_MEM_CMD	*	S2_CMD2CMD
S2_MEM_CMD	S2_MEM_CTRL	*	S2_CMD2CTRL
S2_MEM_CTRL	S2_MEM_CTRL	*	S2_CTRL2CTRL
S2_MEM_*	S2_MEM_*	*	S2_2OTHERMEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
S2_MEM_DQS1	S2_MEM_DATA1	*	S2_DQS2OWNDATA
S2_MEM_DQS0	S2_MEM_DATA0	*	S2_DQS2OWNDATA

### Memory to Power Spacing

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
S2_MEM_PWR	S2_MEM_*	*	S2MEM_2PWR
S2_MEM_PWR	*	*	DEFAULT

### Memory to GND Spacing

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
GND	S2_MEM_*	*	S2MEM_2GND

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<b>Camera Constraints</b>			
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		REVISION	
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### SMC SMBus & Charger Net Properties

ELECTRICAL CONST SET	NET TYPE			
	PHYSICAL	SPACING		
SMBUS_SMC_2	SMB_45S	SMB	SMBUS_SMC_2_S3_SCL	34 36 39 68
SMBUS_SMC_2	SMB_45S	SMB	SMBUS_SMC_2_S3_SDA	34 36 39 68
SMBUS_SMC_1	SMB_45S	SMB	SMBUS_SMC_1_S0_SCL	14 32 36 39 43 68 72
SMBUS_SMC_1	SMB_45S	SMB	SMBUS_SMC_1_S0_SDA	14 32 36 39 43 68 72
SMBUS_SMC_0	SMB_45S	SMB	SMBUS_SMC_0_S0_SCL	36 39 62 68
SMBUS_SMC_0	SMB_45S	SMB	SMBUS_SMC_0_S0_SDA	36 39 62 68
SMBUS_SMC_5	SMB_45S	SMB	SMBUS_SMC_5_G3_SCL	36 39 51 52 68
SMBUS_SMC_5	SMB_45S	SMB	SMBUS_SMC_5_G3_SDA	36 39 51 52 68
SMBUS_SMC_3	SMB_45S	SMB	SMBUS_SMC_3_SCL	36 39 43 63
SMBUS_SMC_3	SMB_45S	SMB	SMBUS_SMC_3_SDA	36 39 43 63

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SYNC MASTER=144		SYNC DATE=08/12/2013	
<b>SMC Constraints</b>			
	DRAWING NUMBER		SIZE
	<SCH_NUM>		D
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PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SENSE_45S	*	=1TO1_DIFFPAIR	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	0.1 MM	0.1 MM
THERM_45S	*	=1TO1_DIFFPAIR	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	0.1 MM	0.1 MM
DIG_AUDIO	*	=1TO1_DIFFPAIR	=1TO1_DIFFPAIR	=1TO1_DIFFPAIR	=1TO1_DIFFPAIR	0.1 MM	0.1 MM
ANL_AUDIO	*	=1TO1_DIFFPAIR	0.1 MM	0.1 MM	10 MM	0.1 MM	0.1 MM
ANL_AUDIO_WIDE	*	=1TO1_DIFFPAIR	0.3 MM	0.3 MM	10 MM	0.1 MM	0.1 MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SENSE	*	=2X_DIELECTRIC	?
THERM	*	=2X_DIELECTRIC	?
AUDIO	*	=2X_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND	*	=STANDARD	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND_P2MM	*	0.20 MM	1000
PWR_P2MM	*	0.20 MM	1000

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CPU_VCCSENSE	GND	*	GND_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLK_PCIE	GND	*	GND_P2MM
GND	PCIE_*	*	GND_P2MM
GND	SATA_*	*	GND_P2MM
USB	GND	*	GND_P2MM
CLK_PCIE	SB_POWER	*	PWR_P2MM
SB_POWER	SATA_*	*	PWR_P2MM
USB	SB_POWER	*	PWR_P2MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_45S	* OVERRIDE	OVERRIDE	OVERRIDE	0.070 MM OVERRIDE	100 MIL OVERRIDE	OVERRIDE	OVERRIDE
MEM_40S	* OVERRIDE	OVERRIDE	OVERRIDE	0.090 MM OVERRIDE	100 MIL OVERRIDE	OVERRIDE	OVERRIDE
MEM_72D	* OVERRIDE	OVERRIDE	OVERRIDE	0.090 MM OVERRIDE	100 MIL OVERRIDE	OVERRIDE	OVERRIDE
MEM_85D	* OVERRIDE	OVERRIDE	OVERRIDE	0.090 MM OVERRIDE	100 MIL OVERRIDE	OVERRIDE	OVERRIDE
PCIE_85D	* OVERRIDE	OVERRIDE	OVERRIDE	0.090 MM OVERRIDE	10 MM OVERRIDE	OVERRIDE	OVERRIDE
USB_85D	TOP			0.100 MM	500 MIL		
CPU_27P4S	BOTTOM			0.230 MM	100 MIL		
USB3_85D	TOP			0.100 MM	500 MIL		
USB3_85D	ISL10			0.075 MM			0.090 MM
DP_85D	ISL9			0.075 MM			0.090 MM
PCIE_85D	ISL10			0.075 MM			0.090 MM

### DDR3 Loaded Segment Constraint Relaxations

Alternate single ended and differential impedances between devices.

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
MEM_40S	BGA_MEM	MEM_45S
MEM_72D	BGA_MEM	MEM_85D

Allow 0.127 mm necks for >0.127 mm lines for ARD fanout.

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_72D	BOTTOM			0.127 MM	6.35 MM		
MEM_85D	TOP			0.100 MM	6.35 MM		

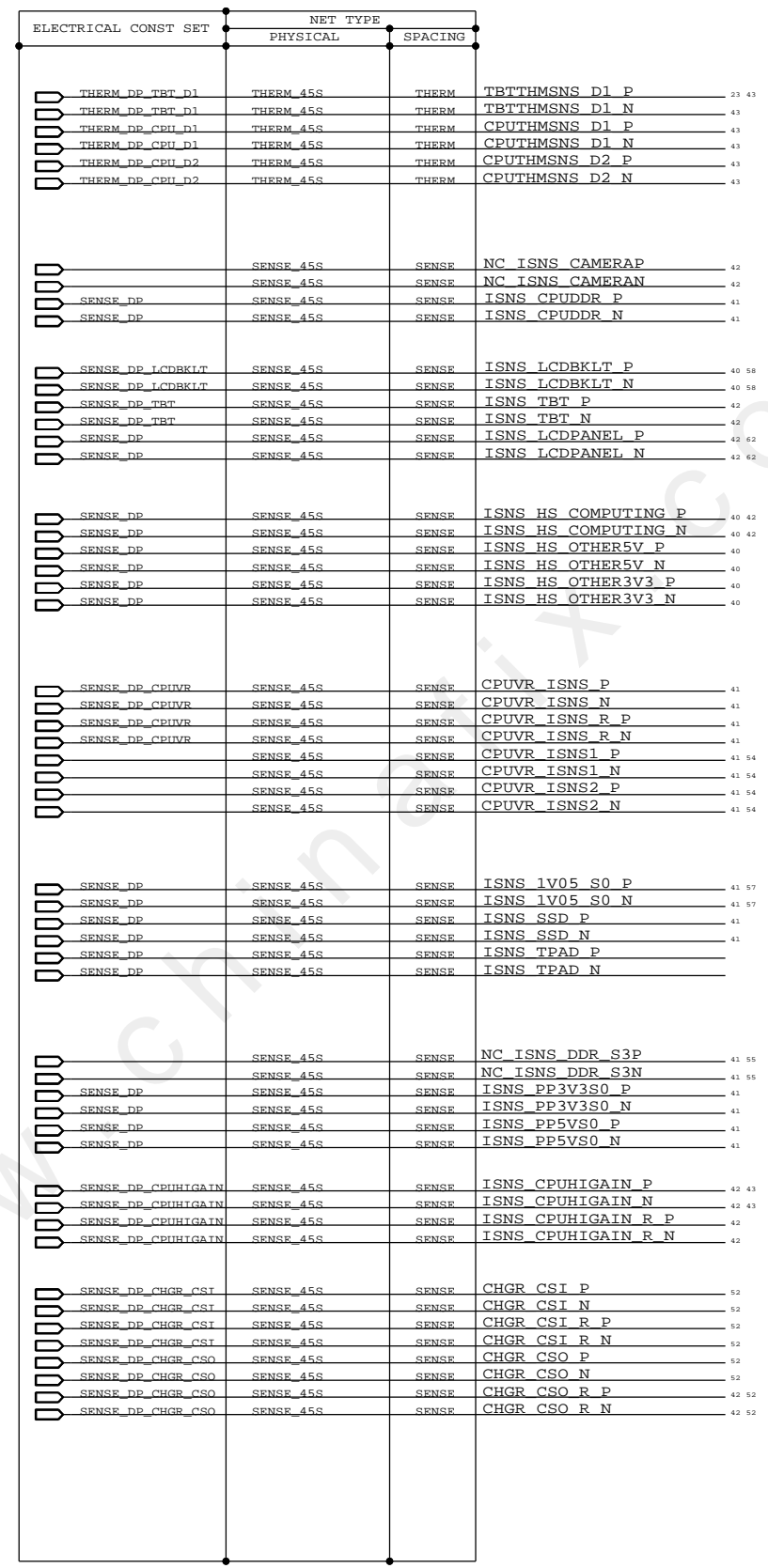
### DP, SATA, HDMI, PCIE CONSTRAINT RELAXATIONS

Alternate diffpair width/gap through BGA fanout areas (95-ohm diff)

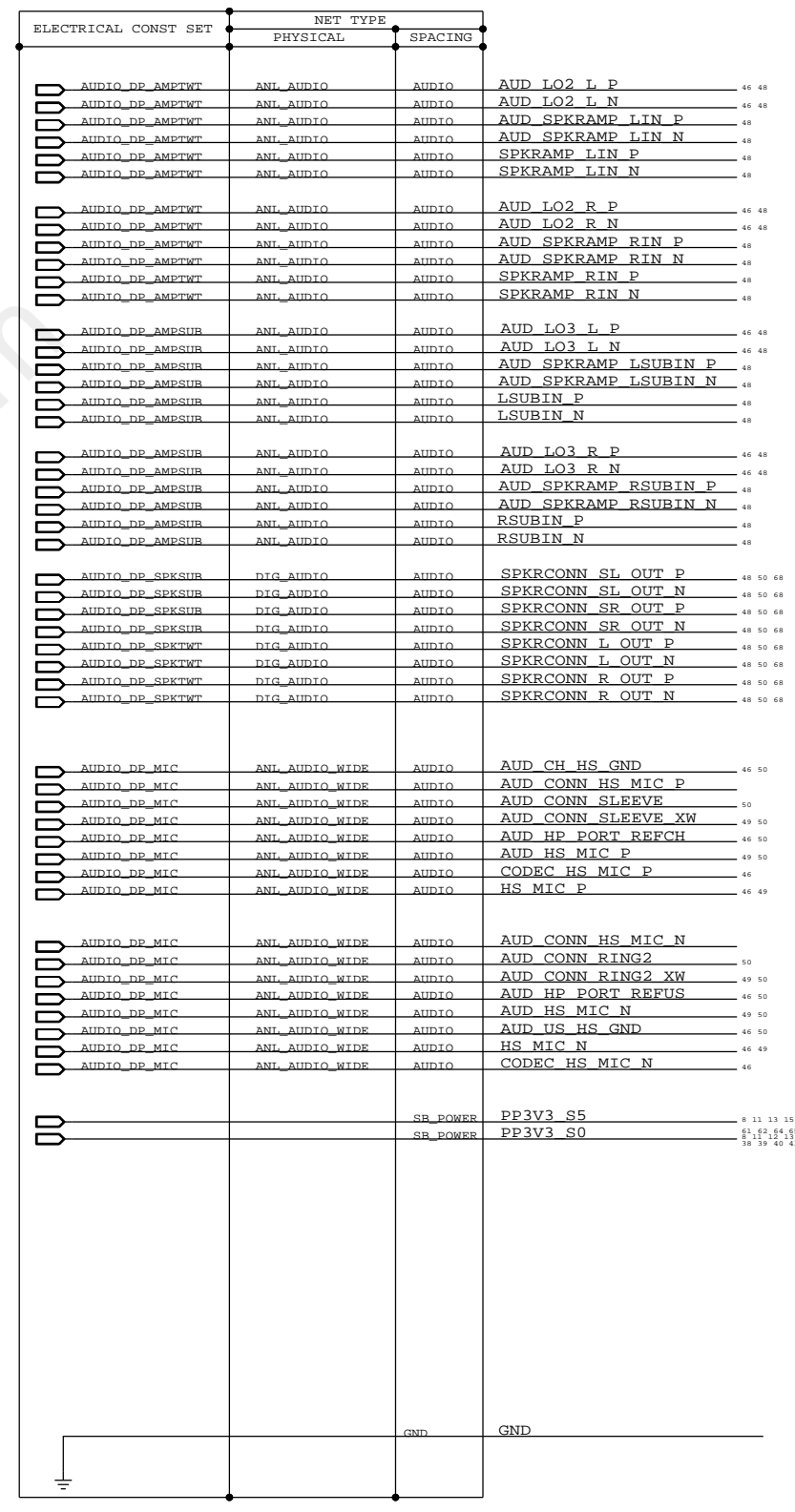
NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
DP_85D	BGA	P65_BGA
PCIE_85D	BGA	P65_BGA
CLK_PCIE_85D	BGA	P65_BGA
HDMI_85D	BGA	P65_BGA

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
SENSE_45S	*	SENSE_45S
THERM_45S	*	THERM_45S
DIG_AUDIO	*	DIG_AUDIO
ANL_AUDIO	*	ANL_AUDIO
1TO1_DIFFPAIR	*	1TO1_DIFFPAIR

### J44 Specific Net Properties



### J44 Specific Net Properties



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