

Genesis-1 Block Diagram

LGS-1 91.4RQ01.001

JULY. 18, 2011

PCB Layer Stackup

- L1:Component
- L2:GND
- L3:Signal 1
- L4:VCC
- L5:Signal 2
- L6:Signal 3
- L7:VCC
- L8:Signal 4
- L9:GND
- L10:Component

Battery Charger/Selector
BQ24760 75

INPUTS		OUTPUTS	
VINT20		CHARGER_OUT12	

System DC/DC
TPS51220ARSN 79

VINT20	VCC5M
	VCC3M

CPU DC/DC
VT1318M/VT1324S 80

VCC5M_OUT	VCCPCUCORE
-----------	------------

GMCH GFX CORE
VT1324S 81

VCC5M_OUT	VCCGFXCORE
-----------	------------

VCC1R5B
VT355FCX 86

VCC5M_OUT	VCC1R5B
-----------	---------

VCC0R675B
MAX1510 87

VCC1R35A
VT356FCX 88

VCC5M_OUT	VCC1R35A
VCC1R35A	VCC0R675B

VCC1R8B
BD9139 89

VCC5M_OUT	VCC1R8B
-----------	---------

VCC1R05AMT
VT356FCX 85

VCC5M_OUT	VCC1R05LAN
-----------	------------

VCC1R05B_VTT
VT356 84

VCC5M_OUT	VCC1R05B_VTT
-----------	--------------

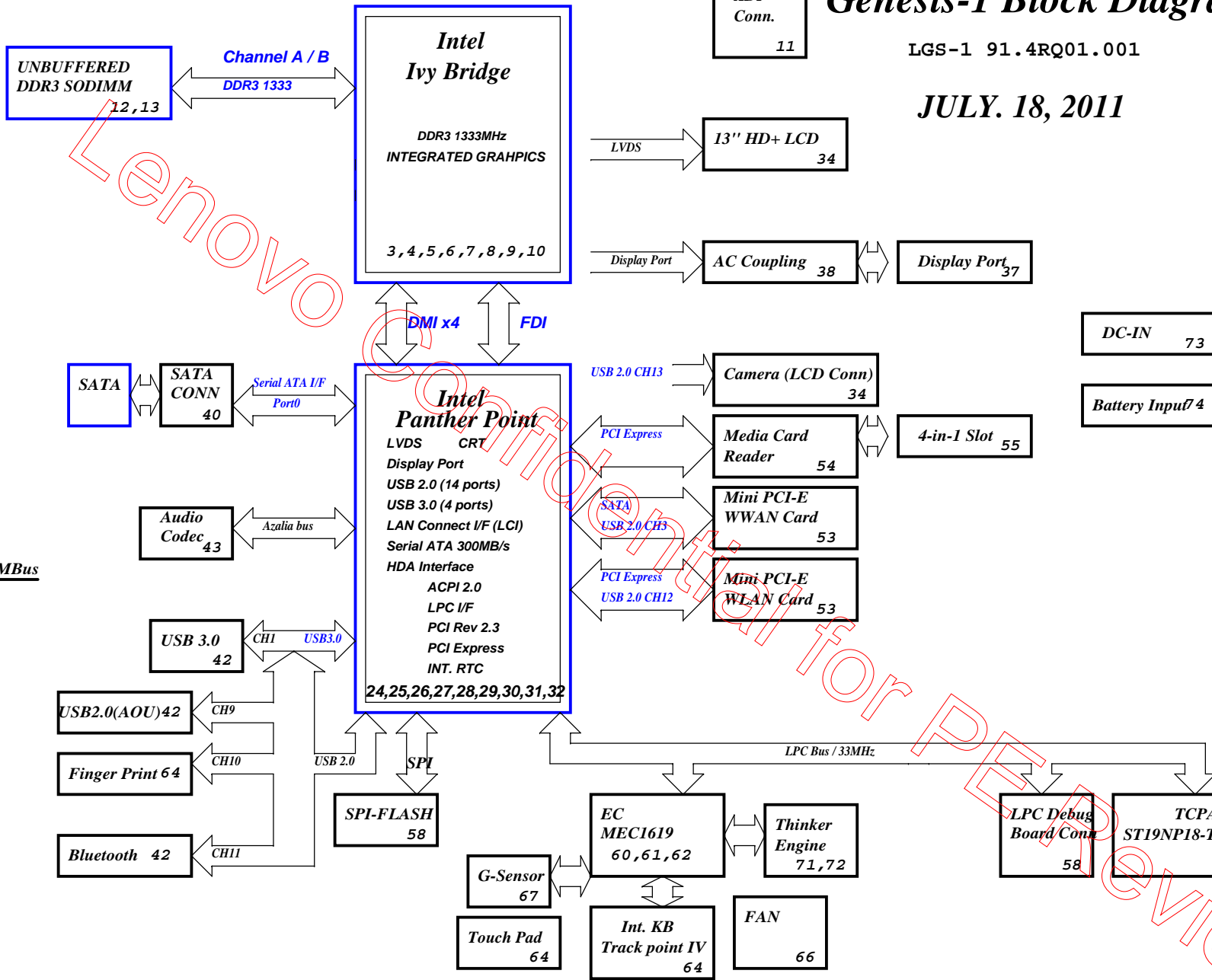
VCCSA
VT371 90

VCC5M_OUT	VCCSA
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<Core Design>

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Block Diagram		
File		
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RESISTOR

Symbol name	Value	Tolerance (J: 5%, F: 1%, D: 0.5%, B: 0.1 %)	Rating 0402=> 1/16W, 25V 0603 => 1/16W, 75V 0805 => 1/10W, 100V	Size 2=>0402, 3=>0603, 5=>0805, 6=>1206, 0=>1210

The naming rule is value + R + size + tolerance
 For the value, it can be read by the number before R (R means resistor)
 For the tolerance, it can be read from the last letter.
 For the rating, we don't show on the symbol name.
 For the size, R2=>0402, R3=>0603, R5=>0805,.....

CAPACITOR

Symbol name	Value	Tolerance (M: +/-20, K: +/-10, Z: +80/-20)	Rating	Size 2=>0402, 3=>0603, 5=>0805, 6=>1206, 0=>1210

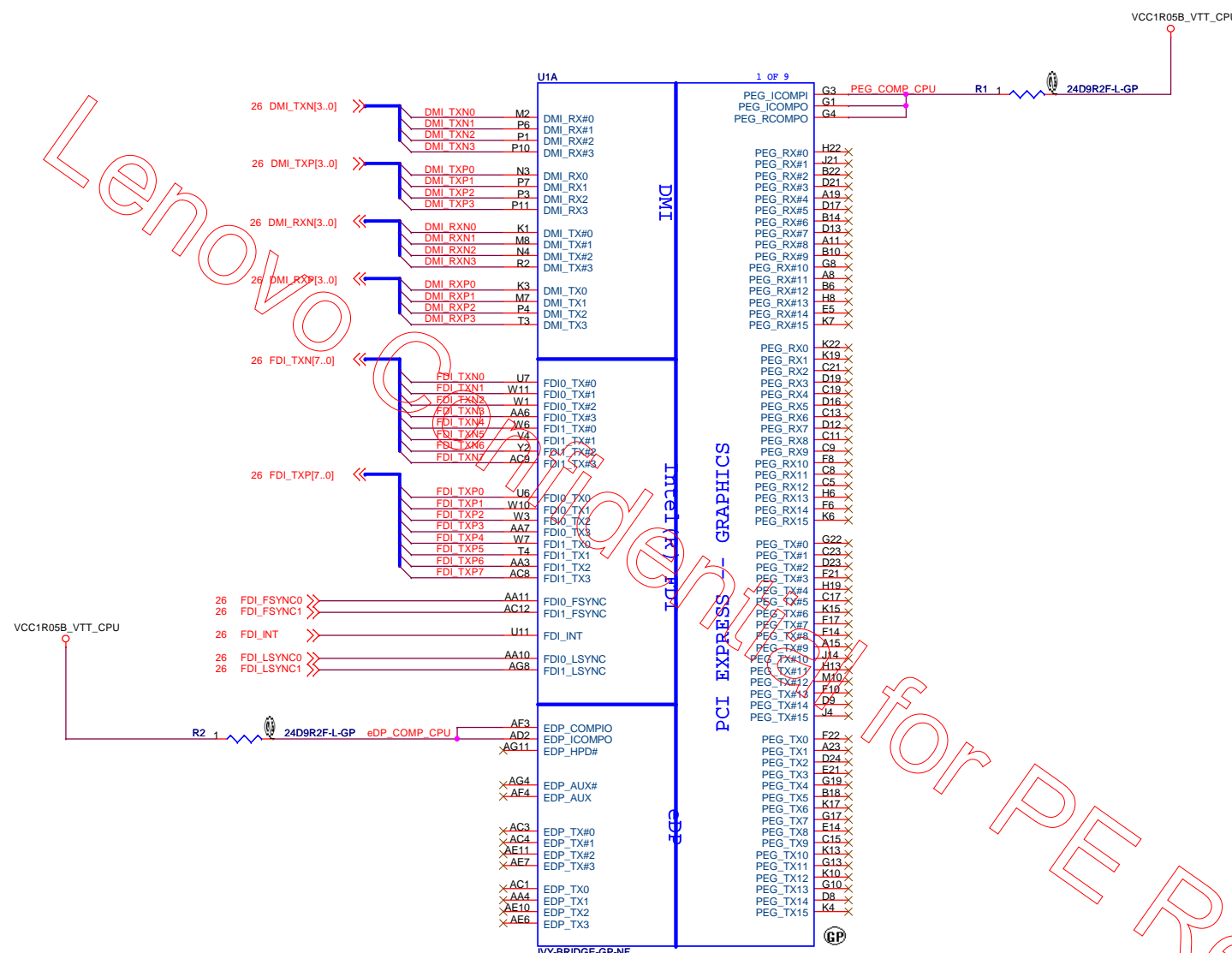
The naming rule is
 Capacitor type + value + rating + size + tolerance + material
 SCD1U10V2MX-1
 SC=> SMT Ceramic, TC=> POS cap or SP cap
 D1U => 0.1uF
 10V => the voltage rating is 10V
 2=> 0402, 3=>0603, 5=>0805
 M=>tolerance M, K, Z
 X=> X7R/X5R, Y=> Y5V
 -1 => symbol version, nonsense to EE characteristic

PLANAR_ID[3..0]

IBEXPEAK-M	39	38	48	49	Planar ID Version	Planar PCB Version
PLANAR_IDn	3	2	1	0	Genesis-1 initial	N/A
	0	0	0	0	Genesis-1 initial	N/A
	0	0	0	1	FVT	N/A
	0	0	1	0	SIT	SC
	0	0	1	1		
	0	1	0	0		
	0	1	0	1		
	0	1	1	0		
	0	1	1	1		
	1	0	0	0		
	1	0	0	1		
	1	0	1	0		

EC HISTORY

Stage	Date	EC No.	Page	Note



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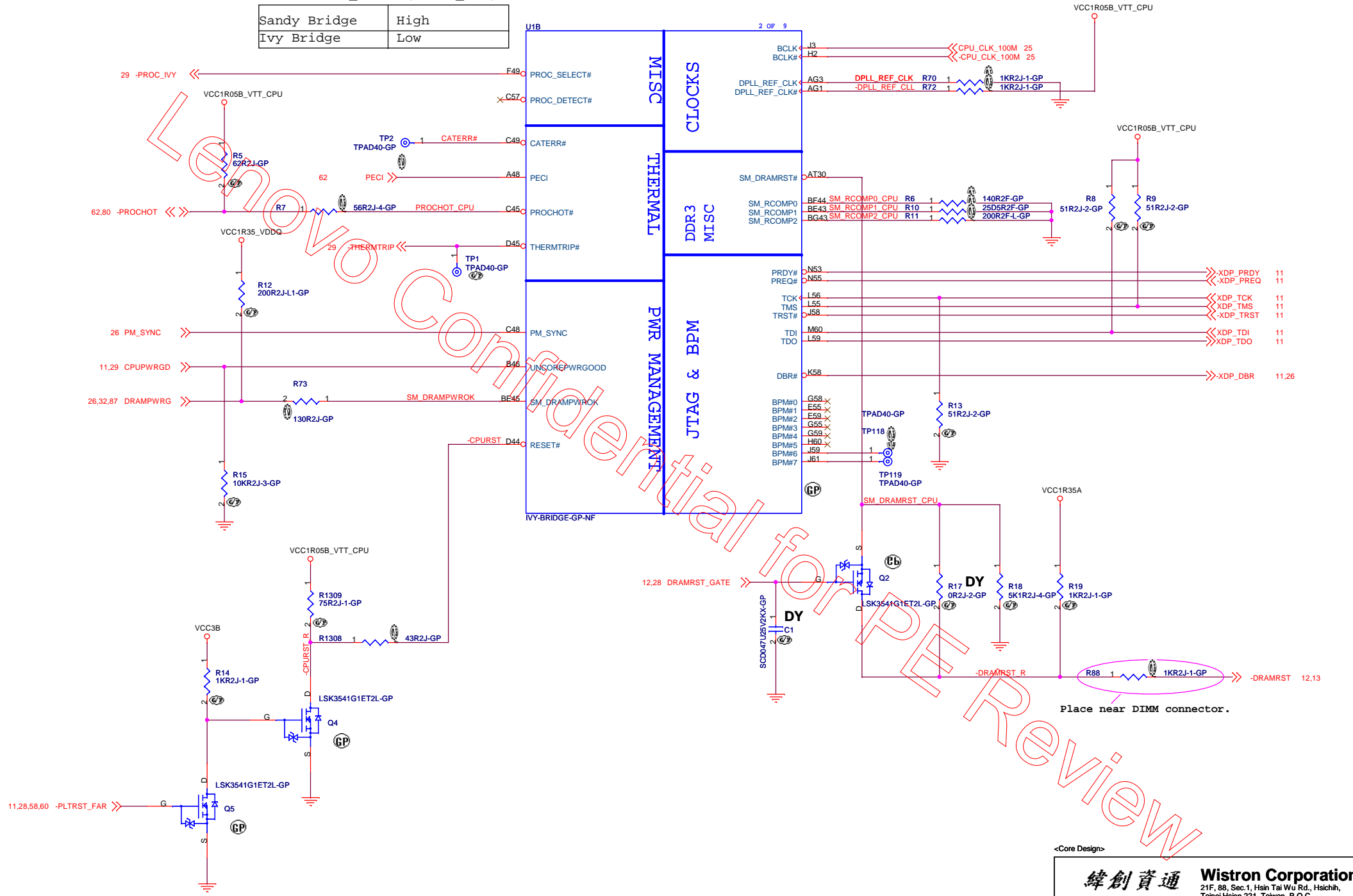
Intel(R) FDI

PCI EXPRESS - GRAPHICS

for PE Review

Table -PROC_SELECT(-PROC_IVY)

Sandy Bridge	High
Ivy Bridge	Low

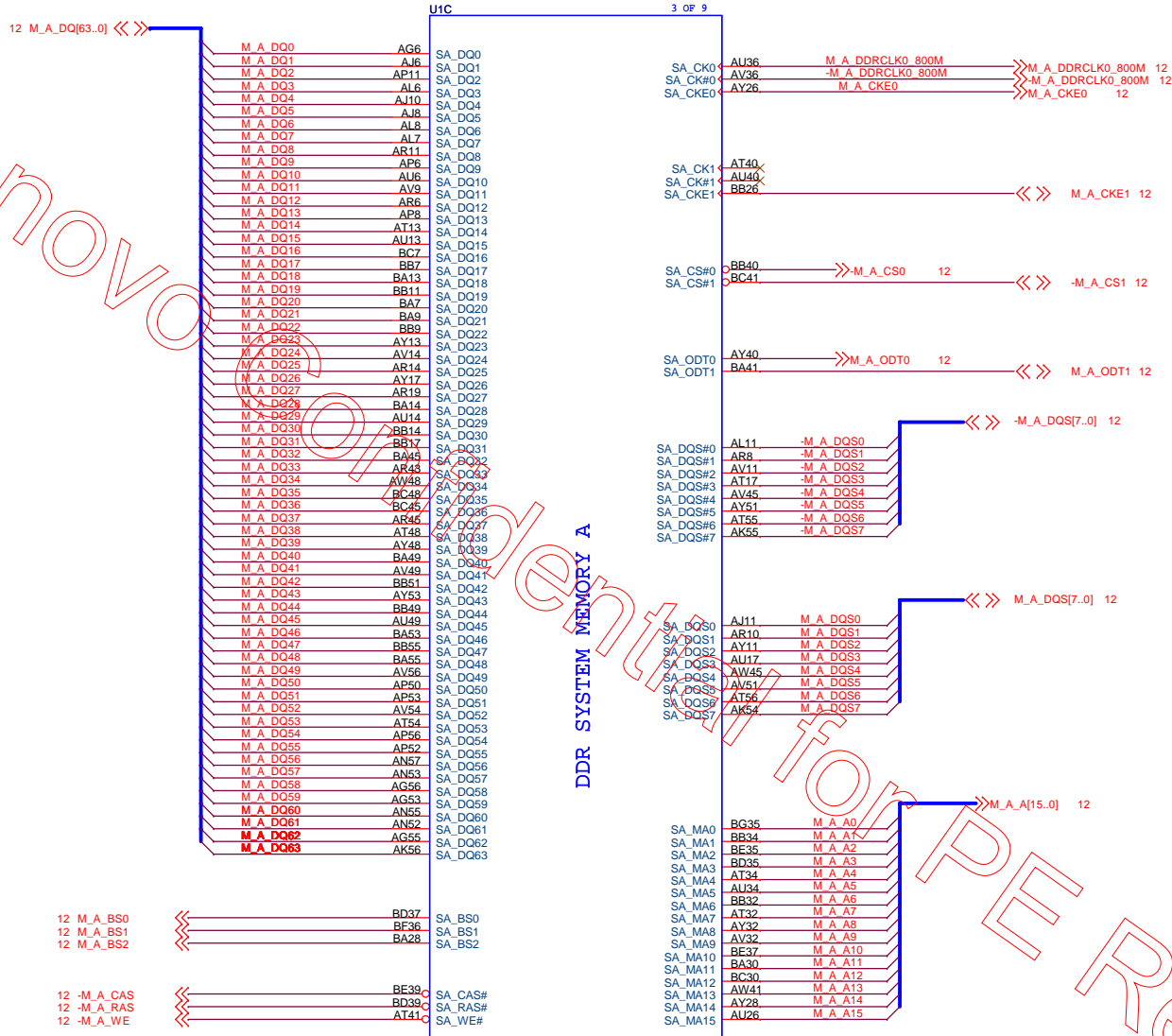


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Title CPU(2/8):CLK/MISC/JTAG	
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Place near DIMM connector.

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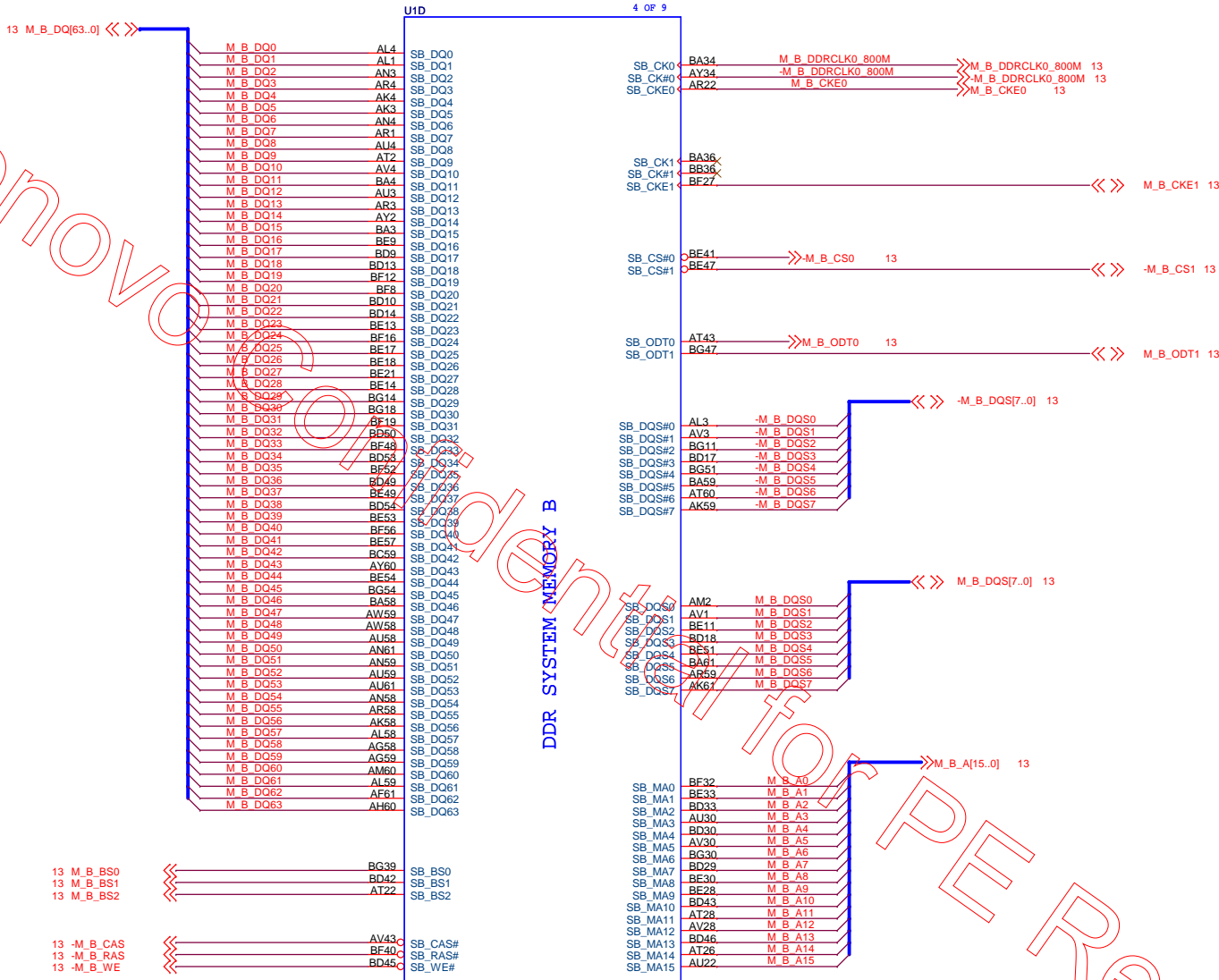


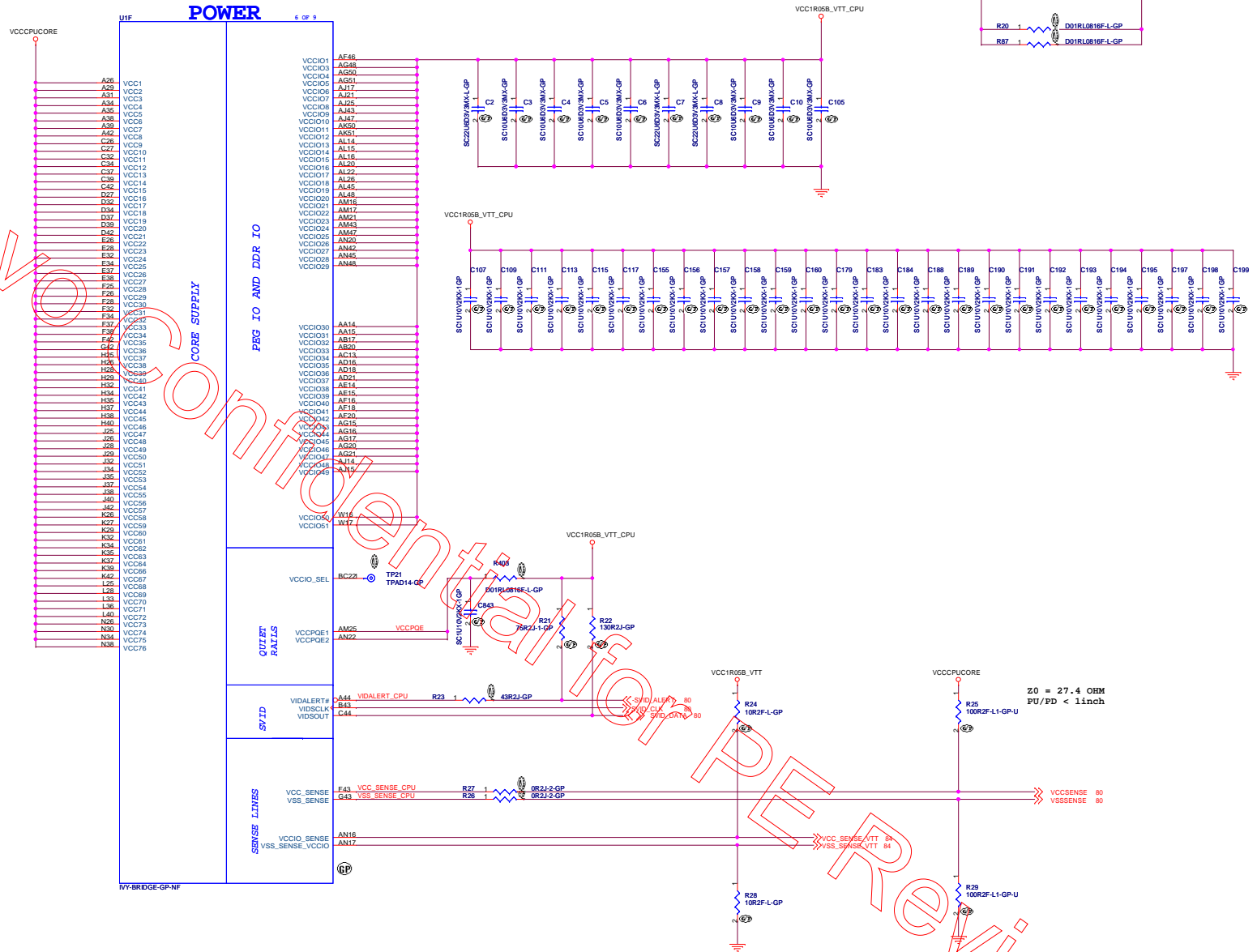
UIC 3 OF 9

IVY-BRIDGE-GP-NF



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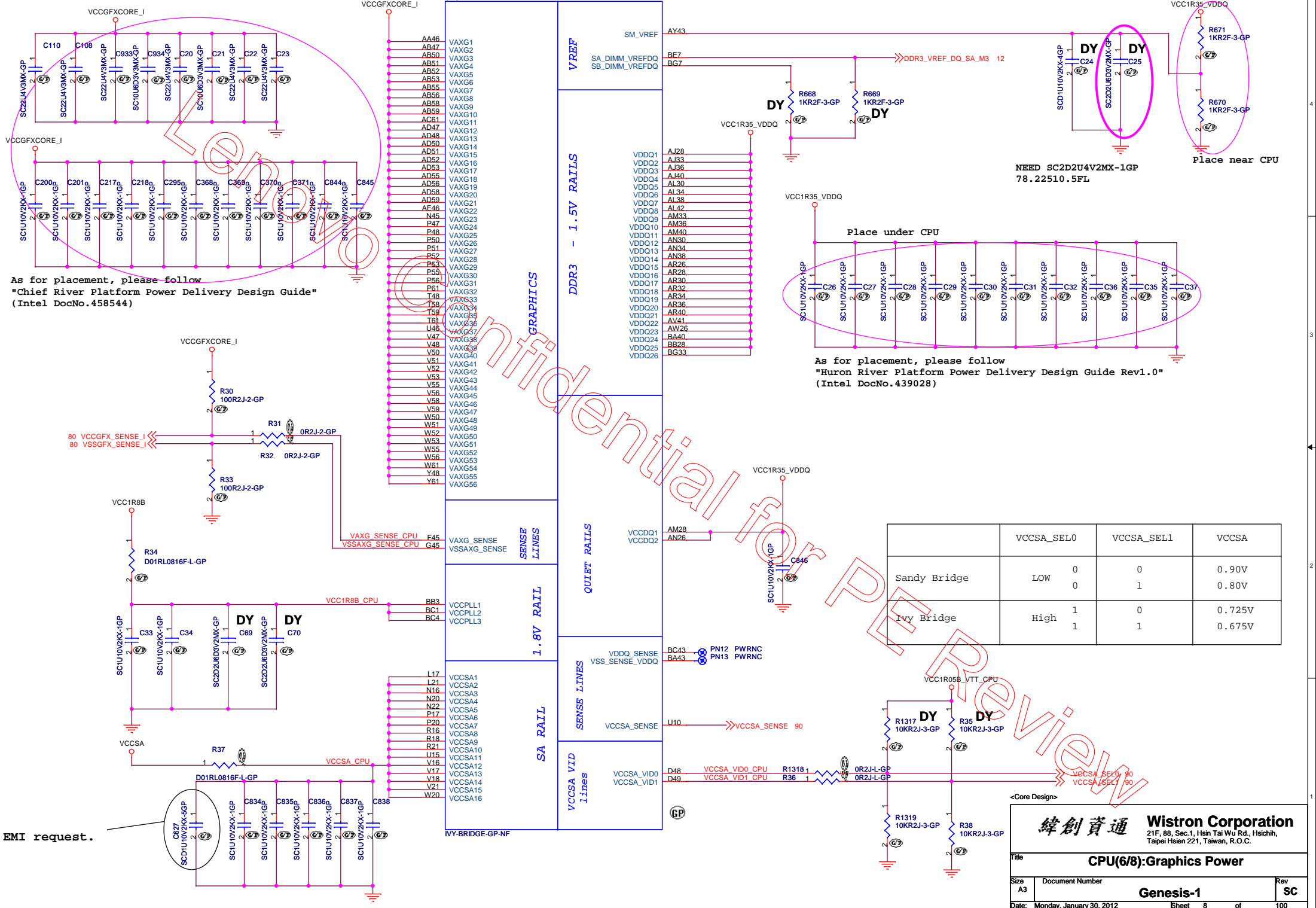




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Z0 = 27.4 OHM
 PU/PD < 1mch

POWER



As for placement, please follow
 "Chief River Platform Power Delivery Design Guide"
 (Intel DocNo.458544)

As for placement, please follow
 "Huron River Platform Power Delivery Design Guide Rev1.0"
 (Intel DocNo.439028)

EMI request.

Pin	Signal	Category
AA46	VAXG1	GRAPHICS
AB47	VAXG2	
AB50	VAXG3	
AB51	VAXG4	
AB52	VAXG5	
AB53	VAXG6	
AB55	VAXG6	
AB56	VAXG7	
AB58	VAXG8	
AB59	VAXG9	
AC61	VAXG10	
AD47	VAXG11	
AD48	VAXG12	
AD50	VAXG13	
AD51	VAXG14	
AD52	VAXG15	
AD53	VAXG16	
AD54	VAXG17	
AD56	VAXG18	
AD58	VAXG19	
AD59	VAXG21	
AE46	VAXG22	
N45	VAXG23	
P47	VAXG24	
P48	VAXG25	
P50	VAXG26	
P51	VAXG27	
P52	VAXG28	
P53	VAXG29	
P56	VAXG30	
P61	VAXG31	
T48	VAXG32	
T58	VAXG33	
T59	VAXG34	
T61	VAXG35	
U48	VAXG36	
V47	VAXG37	
V48	VAXG38	
V50	VAXG40	
V51	VAXG41	
V52	VAXG42	
V53	VAXG43	
V56	VAXG44	
V58	VAXG45	
V59	VAXG47	
W50	VAXG48	
W51	VAXG49	
W52	VAXG50	
W53	VAXG51	
W55	VAXG52	
W56	VAXG53	
W61	VAXG54	
Y48	VAXG55	
Y61	VAXG56	

	VCCSA_SEL0	VCCSA_SEL1	VCCSA
Sandy Bridge	LOW 0	0	0.90V
	0	1	0.80V
Ivy Bridge	High 1	0	0.725V
	1	1	0.675V

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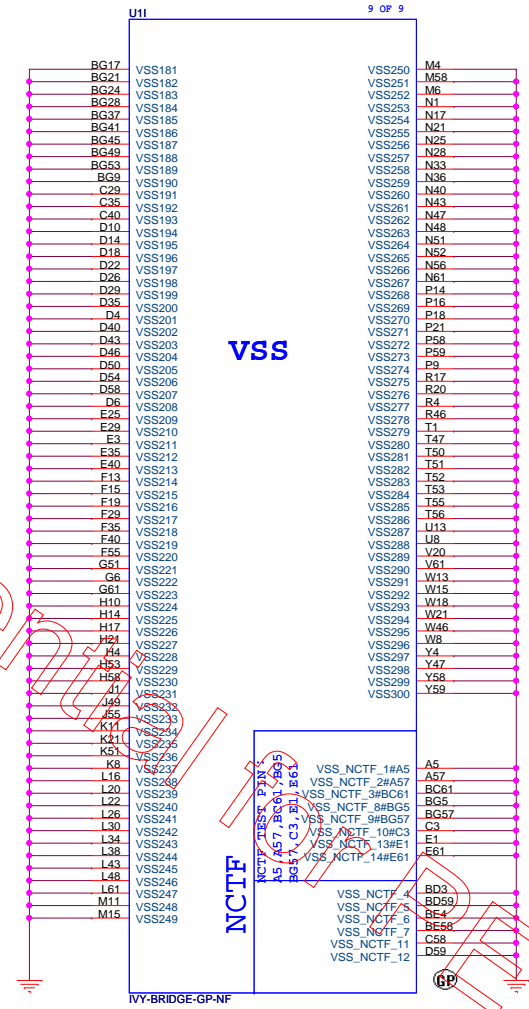
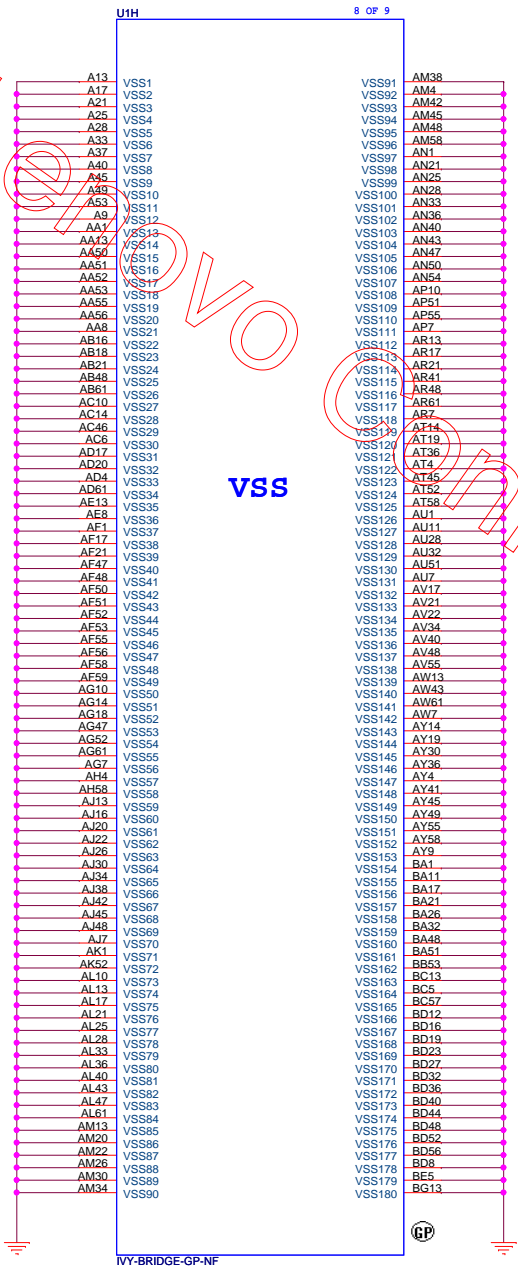
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Title: **CPU(6/8):Graphics Power**

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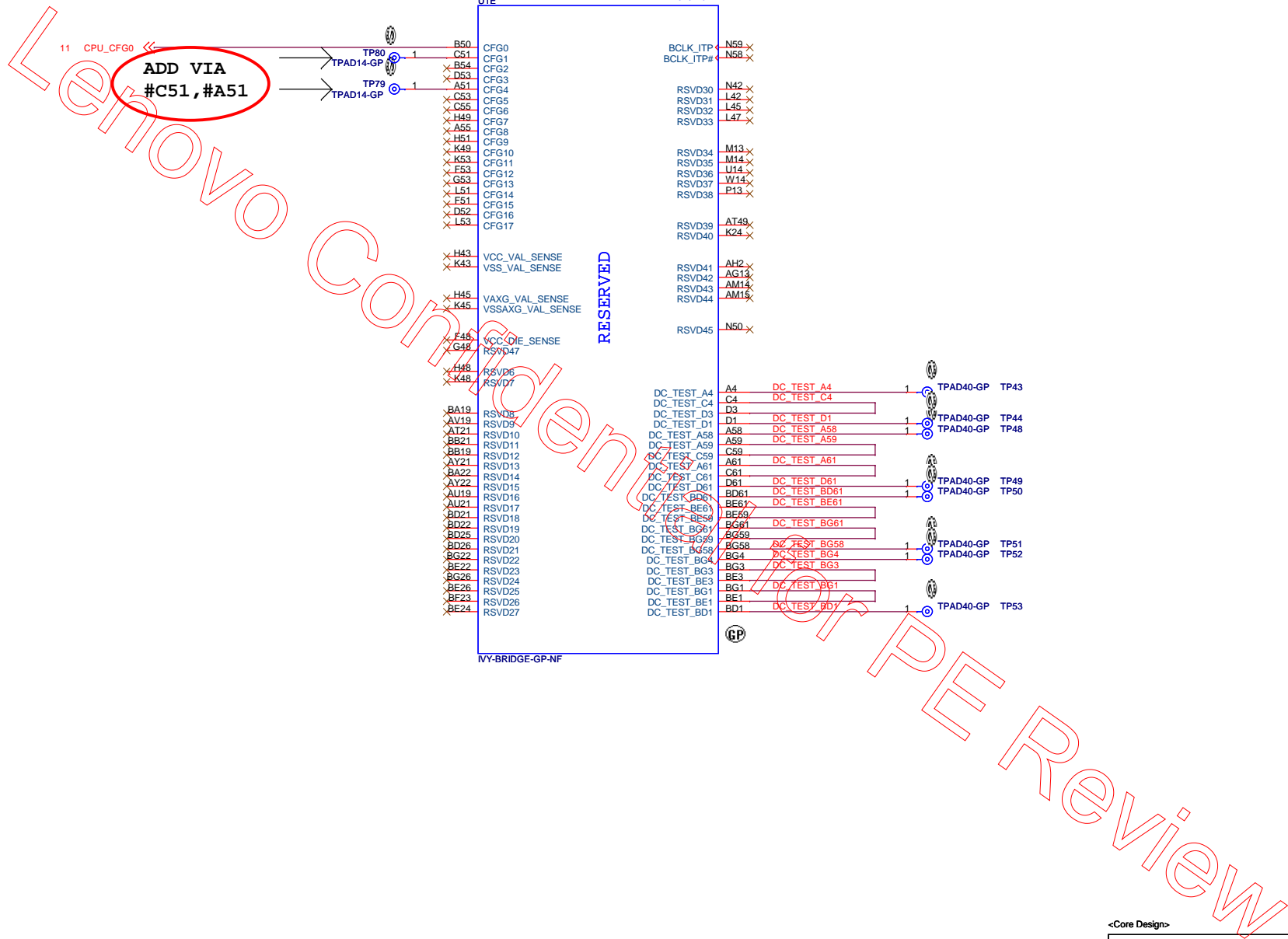
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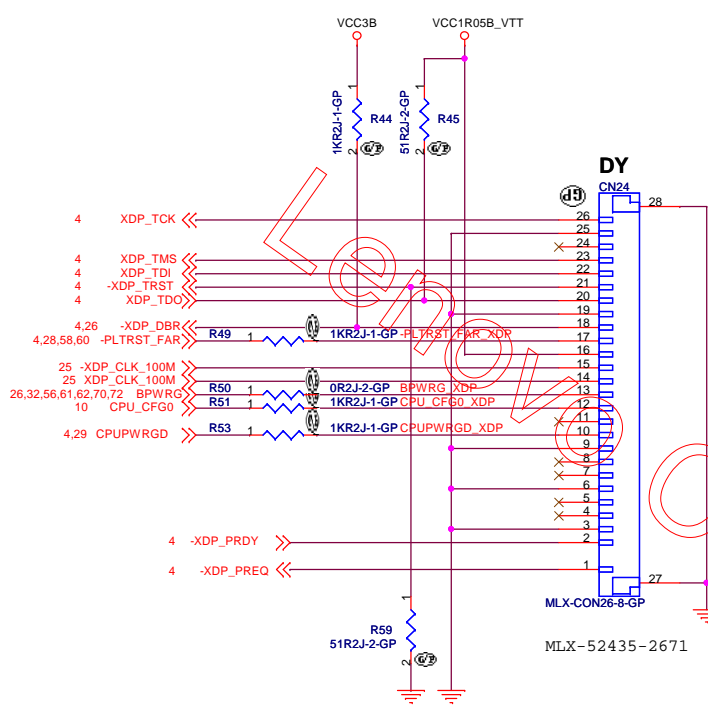
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Title **CPU(7/8):GND**

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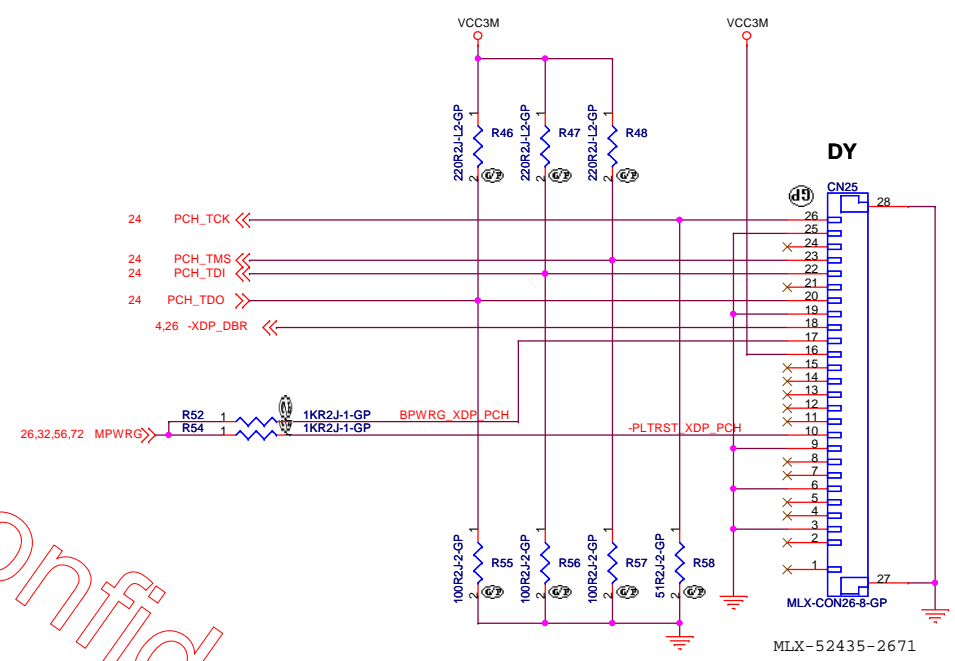


DEBUG Interface for Processor.

XDP1 NOTE:"ASM" FOR PDV/SDV ONLY

		ENABLE	DISABLE
TDO	R45	ASM	DY
TRST#	R59	ASM	ASM
DBRST#	R44	ASM	ASM
RESET#	R49	ASM	DY
CFG0	R51	ASM	DY
PWRGD	R53	ASM	DY
BPWRG	R50	ASM	DY
	CN24	ASM	DY

↑
PDV Logic



DEBUG Interface for PCH.

XDP2 NOTE:"ASM" FOR PDV/SDV ONLY

		ENABLE	DISABLE
TDO	R46	220	DY
	R55	100	DY
TMS	R48	220	DY
	R57	100	DY
TDI	R47	220	DY
	R56	100	DY
TCK	R58	51	51
MPWRG	R52	ASM	DY
	R54	ASM	DY
	CN25	ASM	DY

↑
PDV Logic

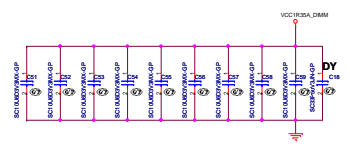
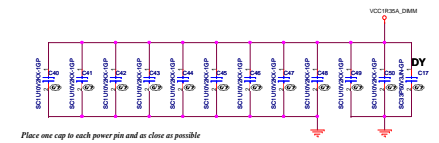
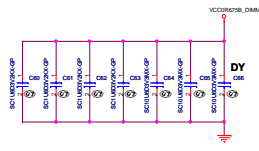
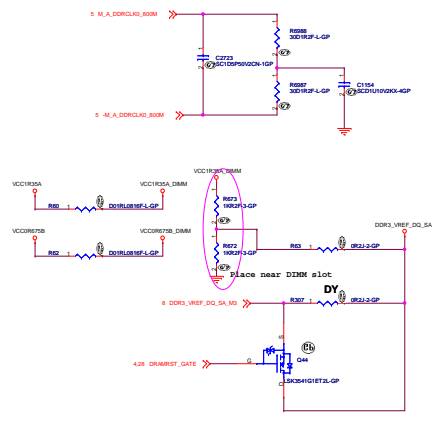
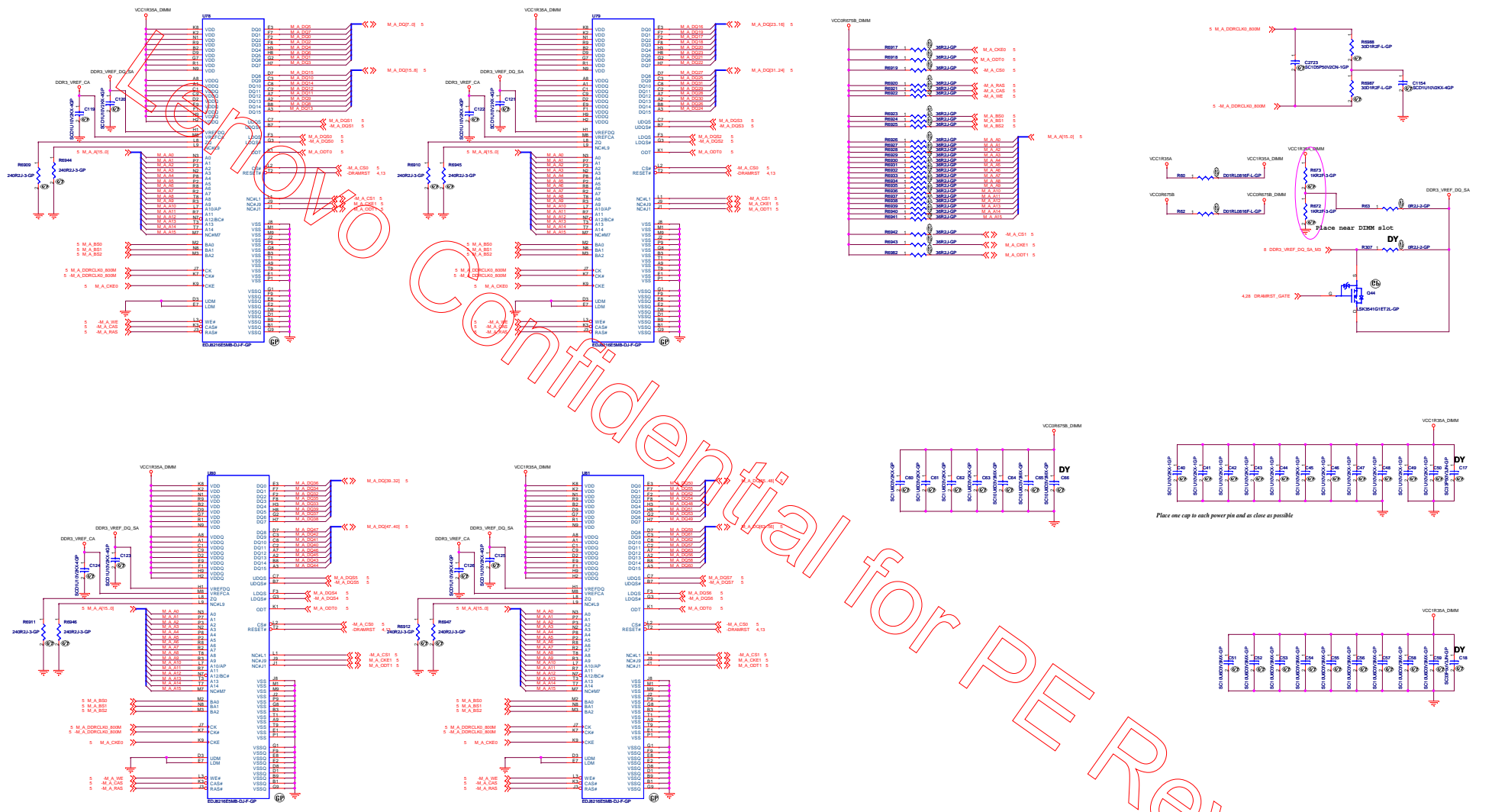
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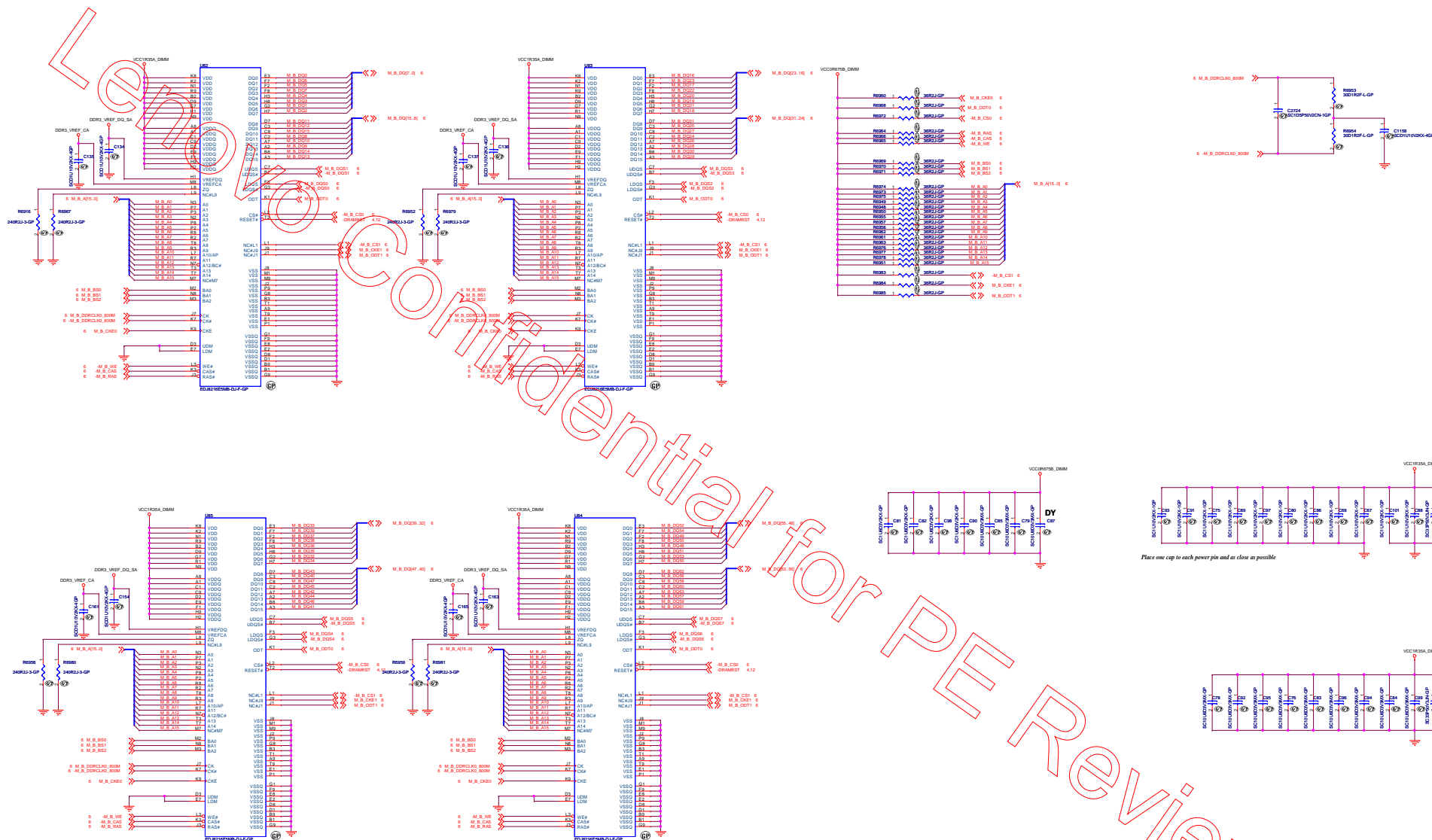
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Title: **XDP Connector**

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Place one cap to each power pin and as close as possible

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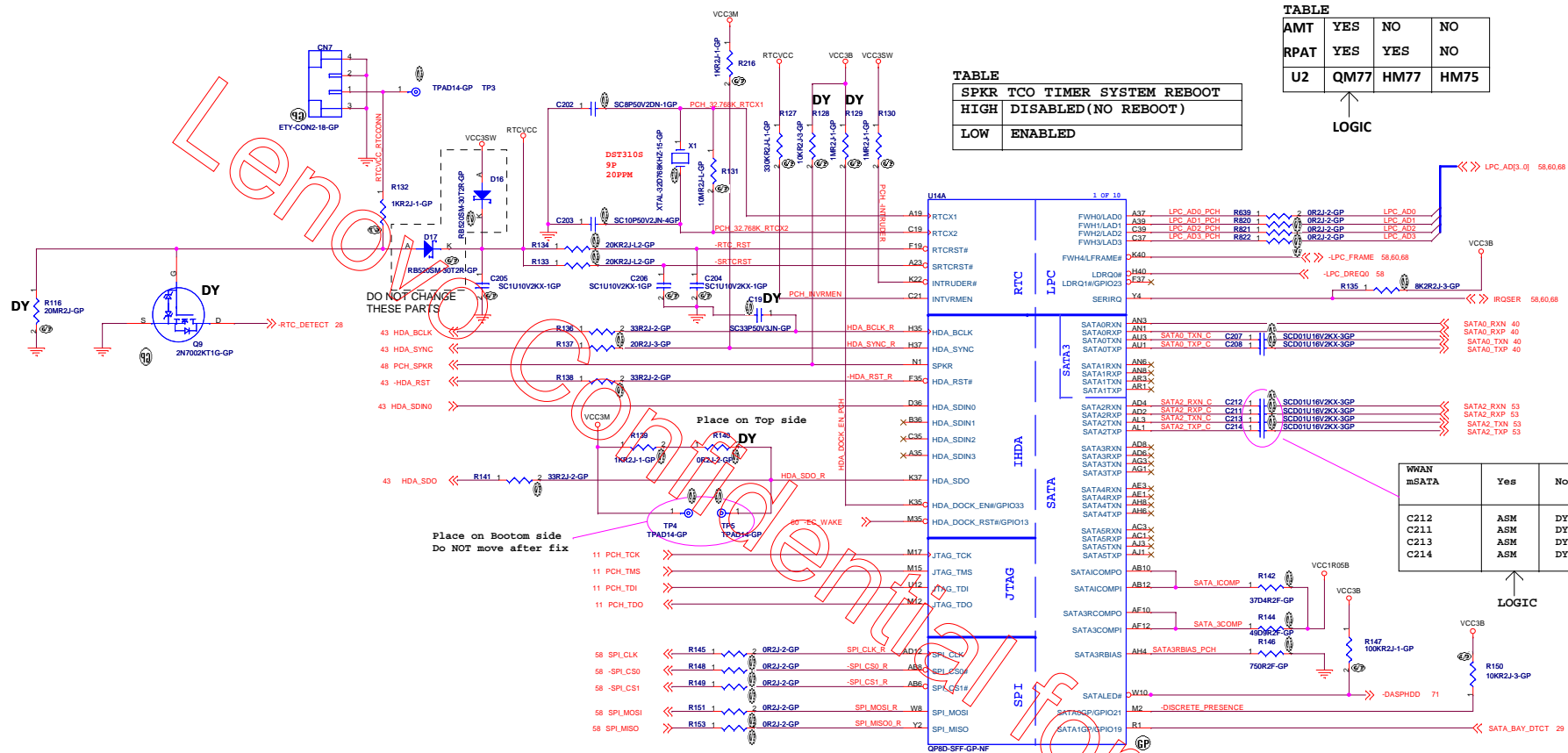
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TABLE

AMT	YES	NO	NO
RPAT	YES	YES	NO
U2	QM77	HM77	HM75

TABLE

SPKR	TCO	TIMER	SYSTEM	REBOOT
HIGH	DISABLED(NO REBOOT)			
LOW	ENABLED			

LOGIC

WWAN			
mSATA	Yes	No	
C212	ASM	DY	
C211	ASM	DY	
C213	ASM	DY	
C214	ASM	DY	

LOGIC

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54 PCIE_MCC_RXN
54 PCIE_MCC_RXP
54 PCIE_MCC_TXN
54 PCIE_MCC_TXP

53 PCIE_WLAN_RXN
53 PCIE_WLAN_RXP
53 PCIE_WLAN_TXN
53 PCIE_WLAN_TXP

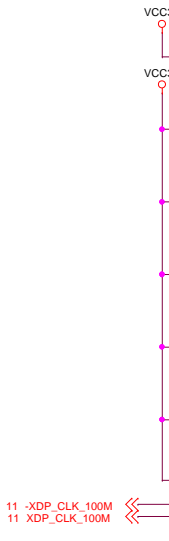
GPIO44	Size	Logic
0: Low	4Gb	← Logic
1: High	8Gb	

GPIO45	GPIO25	Supplier	Logic
0: Low	0: Low	Elpida	← Logic
1: High	1: High	Hynix	
0: Low	0: Low	Samsung	← Logic
1: High	1: High	Reserved	

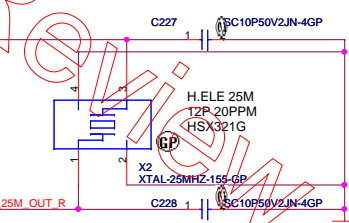
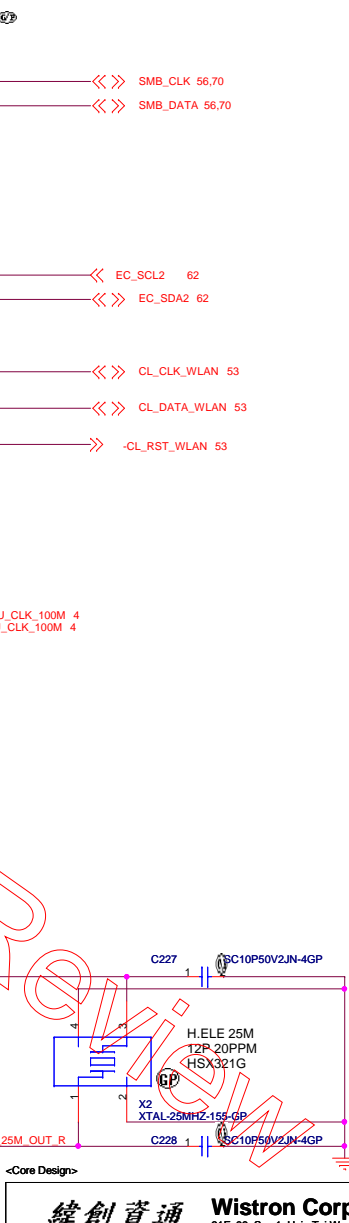
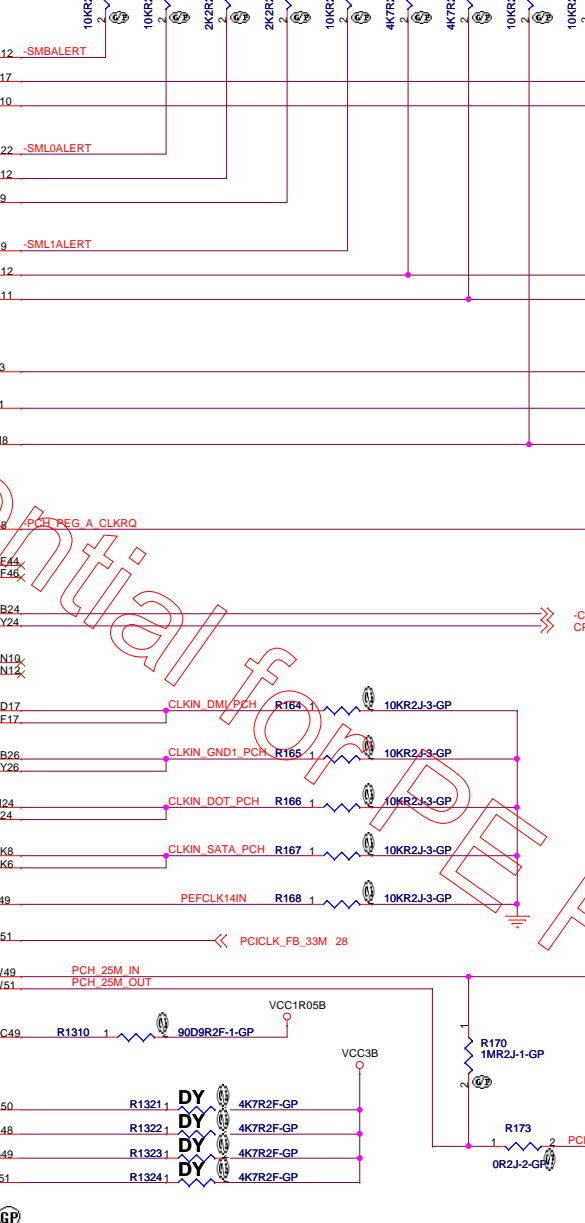
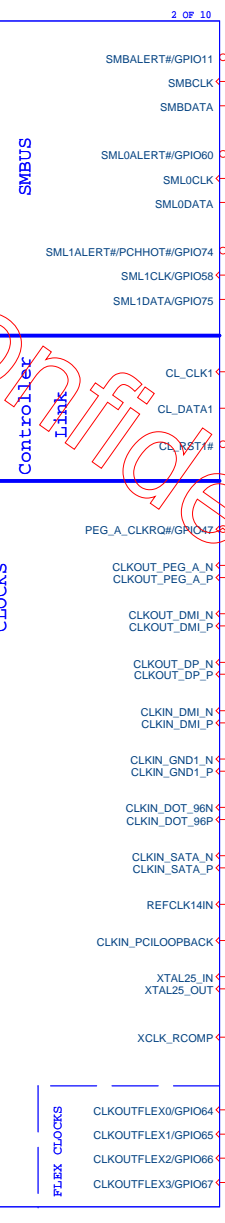
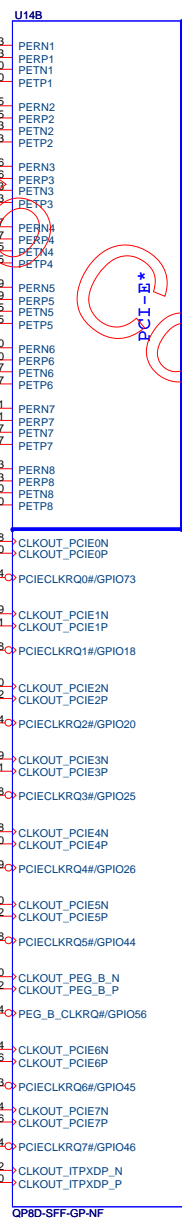
GPIO56	GPIO26	Revision	Logic
0: Low	0: Low	A:Initial	← Logic
1: High	1: High	B	
0: Low	0: Low	C	← Logic
1: High	1: High	D	

54 -PCIE_CLK_MCC
54 PCIE_CLK_MCC
54 -CLKREQ_MCC

53 -PCIE_CLK_WLAN
53 PCIE_CLK_WLAN
53 -CLKREQ_WLAN



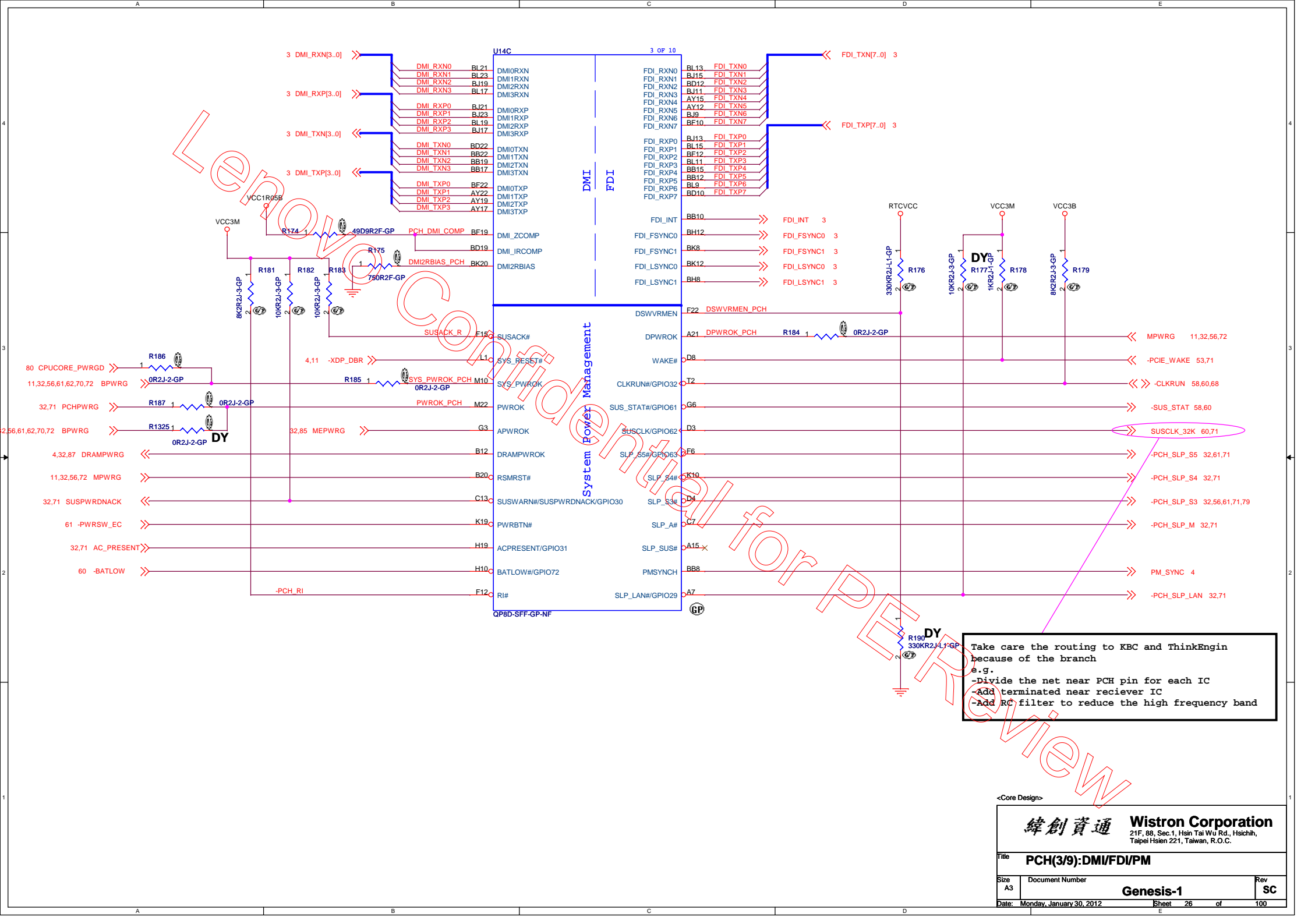
11 -XDP_CLK_100M
11 XDP_CLK_100M



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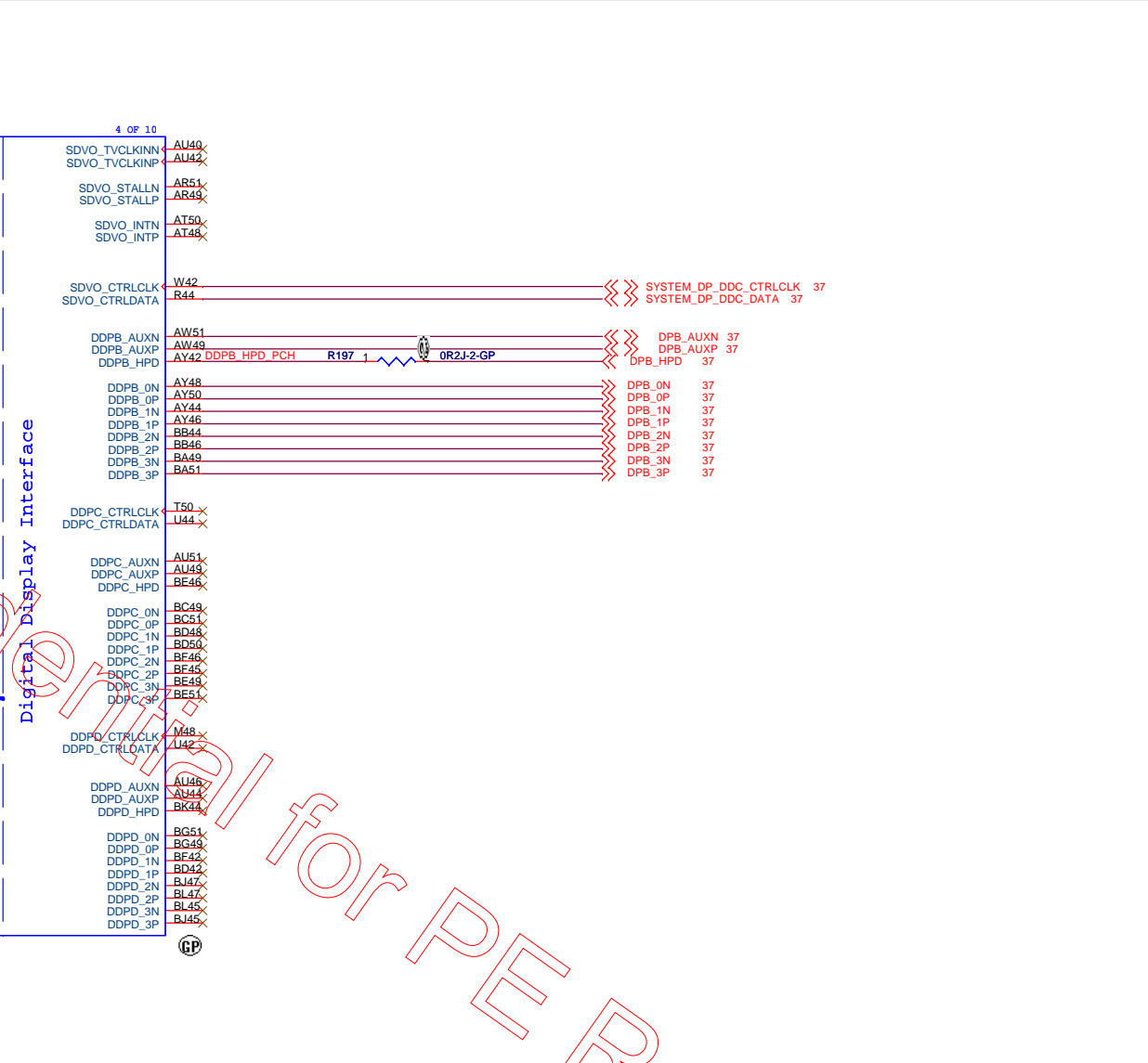
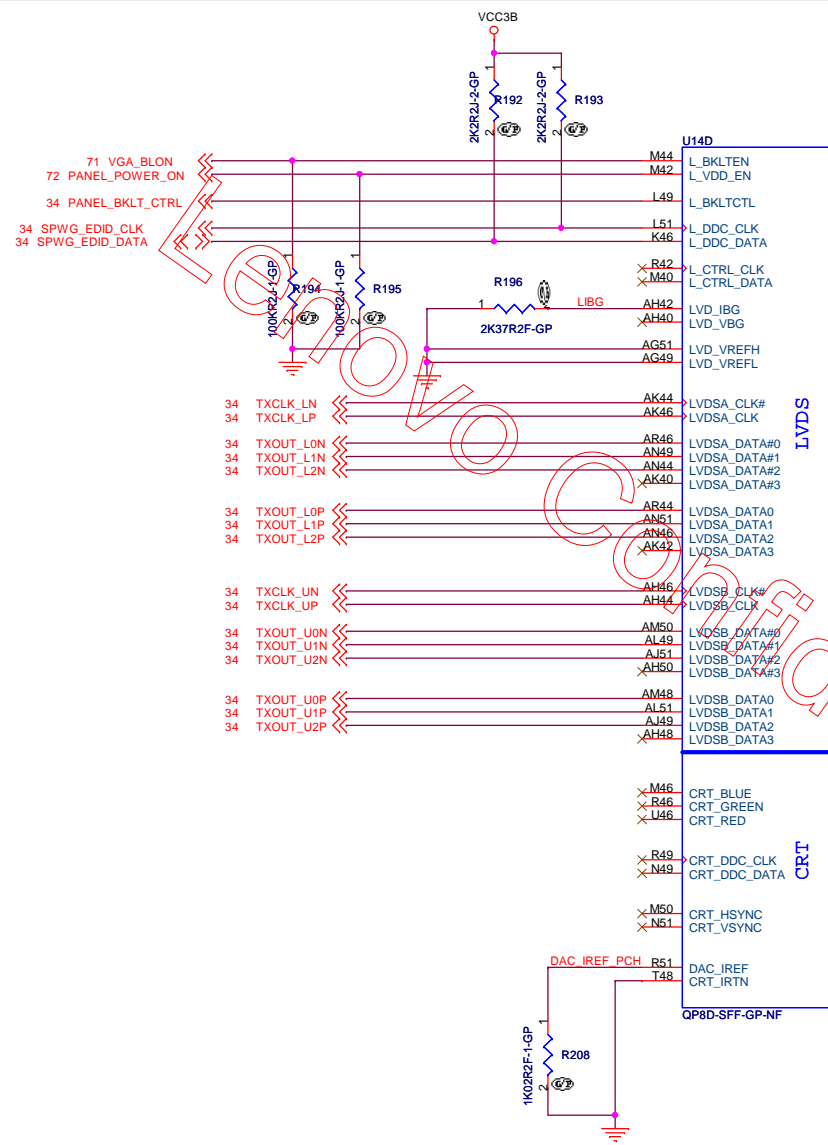
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Title		PCH(2/9):PCI-E/SMBUS/CLK	
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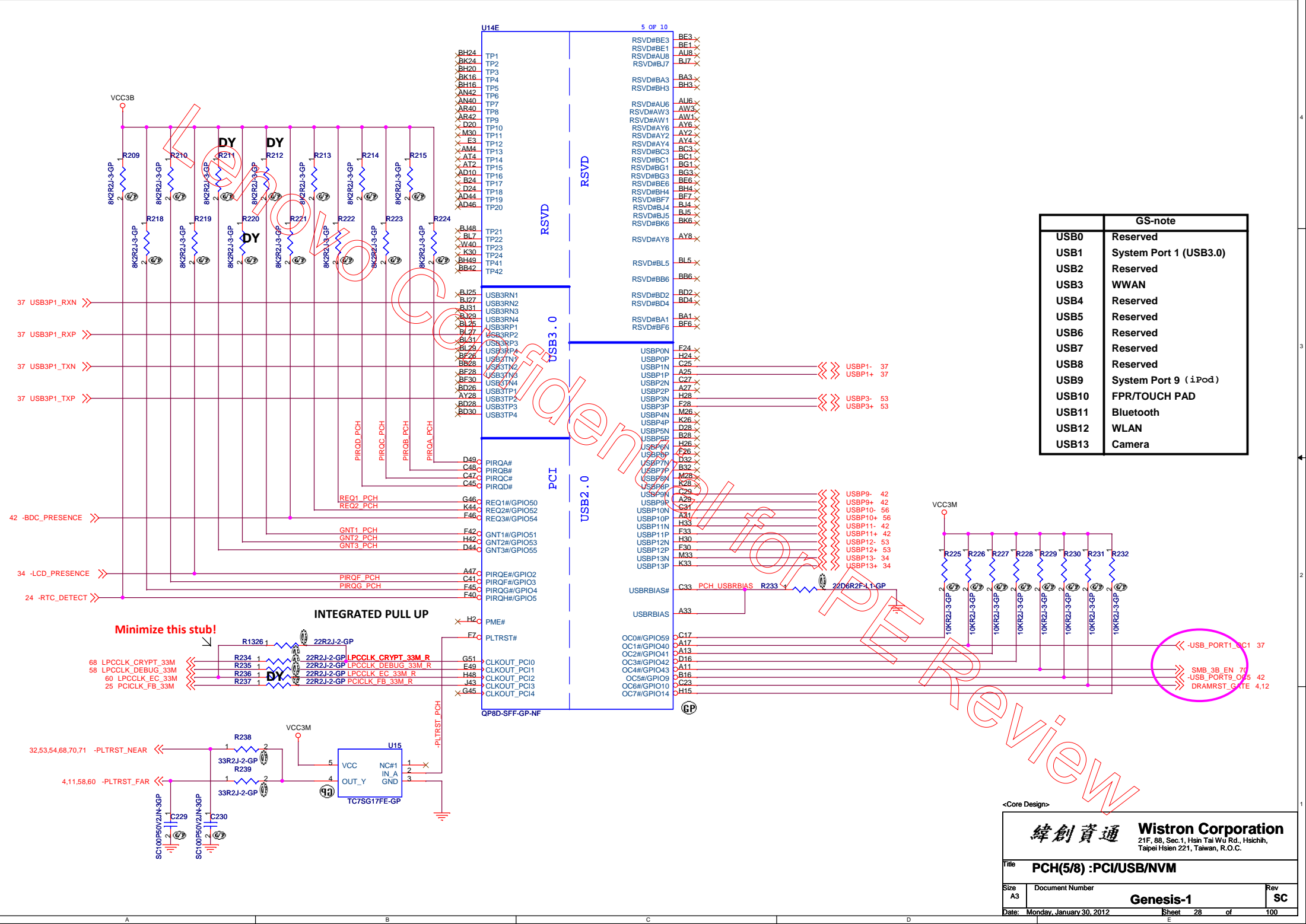


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Take care the routing to KBC and ThinkEngine because of the branch
 e.g.
 -Divide the net near PCH pin for each IC
 -Add terminated near receiver IC
 -Add RC filter to reduce the high frequency band



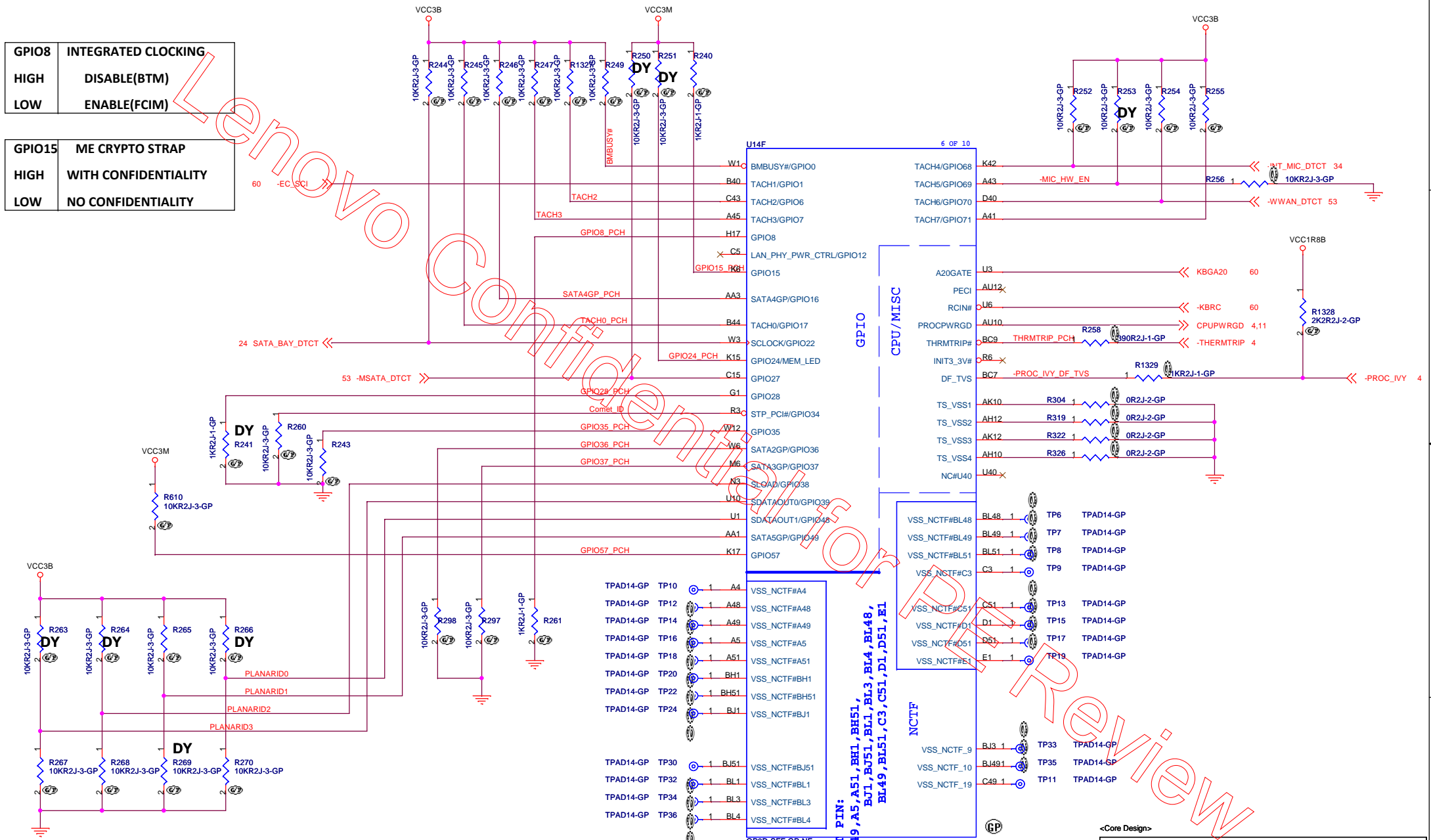
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GS-note	
USB0	Reserved
USB1	System Port 1 (USB3.0)
USB2	Reserved
USB3	WWAN
USB4	Reserved
USB5	Reserved
USB6	Reserved
USB7	Reserved
USB8	Reserved
USB9	System Port 9 (iPod)
USB10	FPR/TOUCH PAD
USB11	Bluetooth
USB12	WLAN
USB13	Camera

GPIO8	INTEGRATED CLOCKING
HIGH	DISABLE(BTM)
LOW	ENABLE(FCIM)

GPIO15	ME CRYPTO STRAP
HIGH	WITH CONFIDENTIALITY
LOW	NO CONFIDENTIALITY



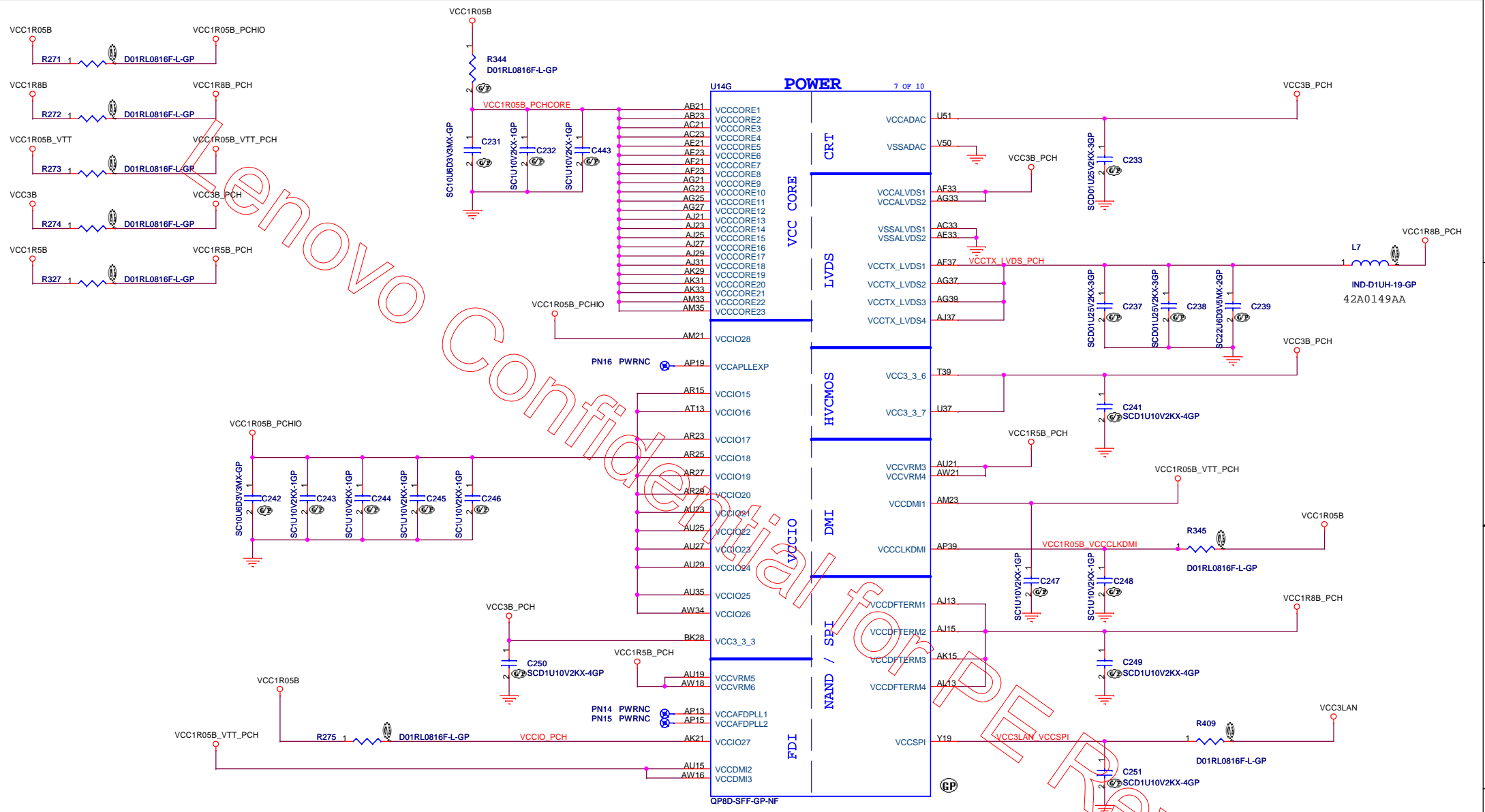
PLANAR ID: 0000 for Initial Assessment
 0001 for FVT
 0010 for SIT

NCTF TEST PIN:
 A4, A48, A49, A51, A55, A51, BH1, BH51, BJ1, BJ51, BL1, BL3, BL4, BL48, BL49, BL51, C3, C51, D1, D51, E1

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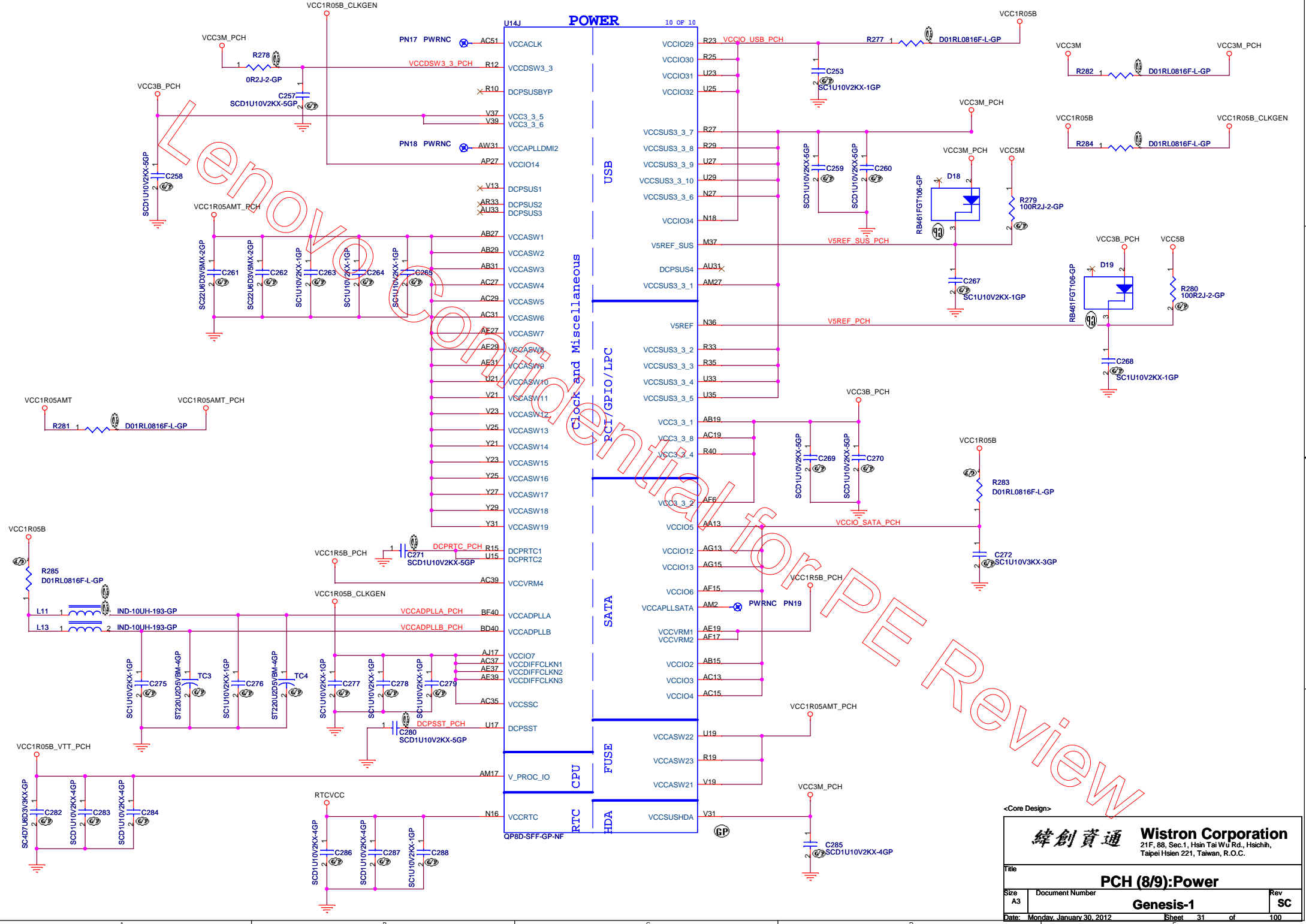
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Size	Document Number	Rev
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Title PCH(7/9):Power	
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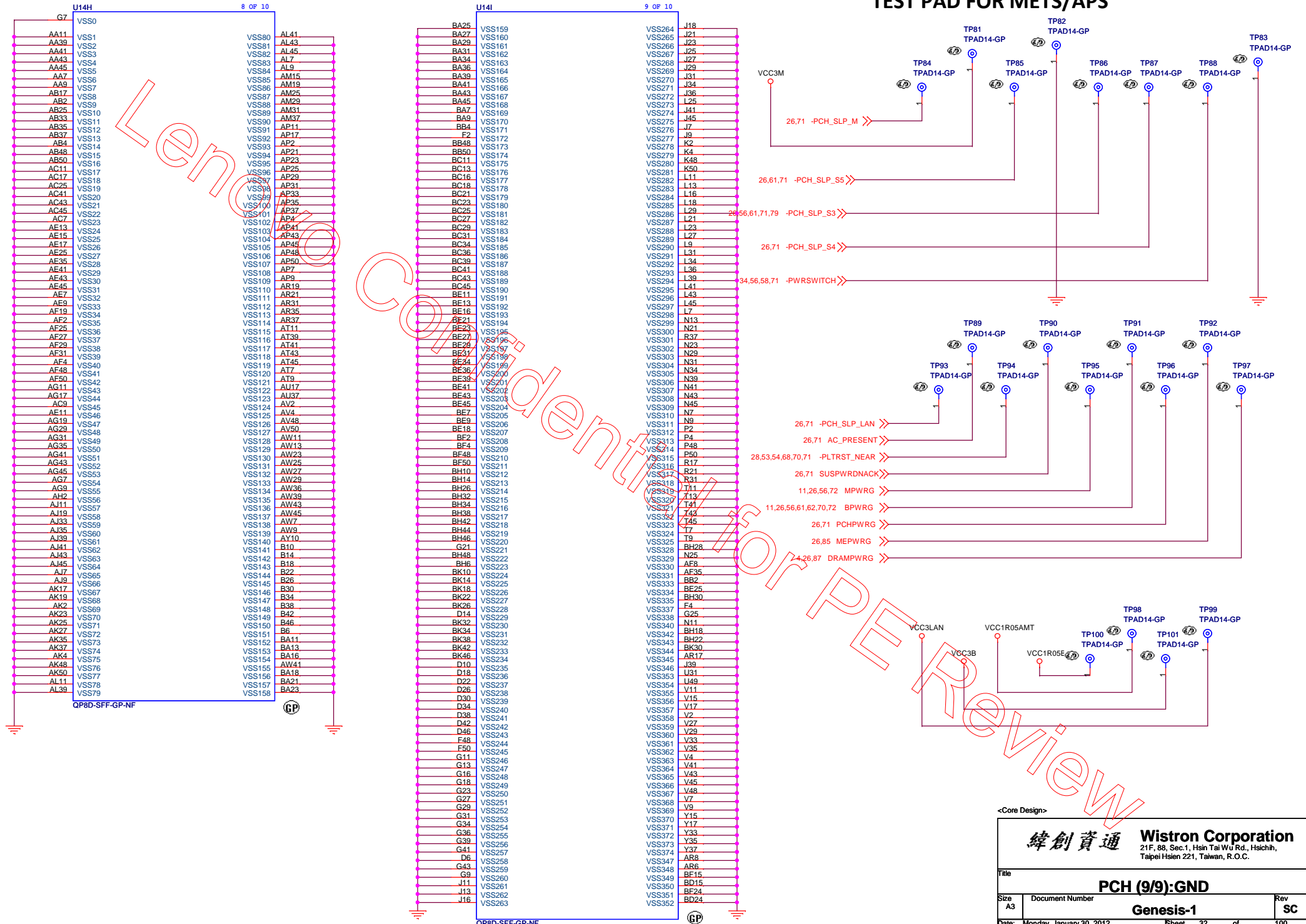


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Title		
PCH (8/9):Power		
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TEST PAD FOR METS/APS



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Title: **PCH (9/9):GND**

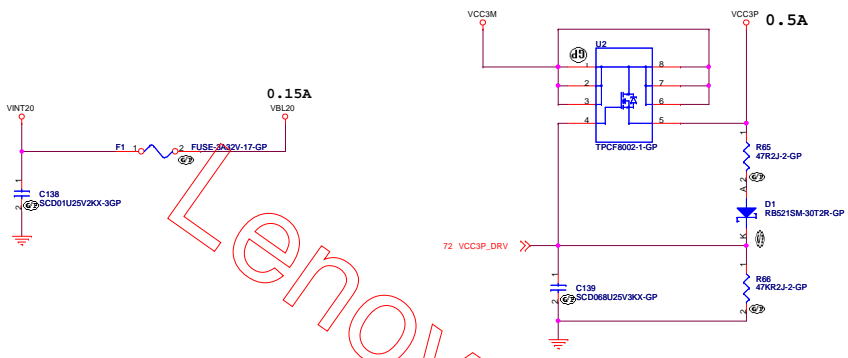
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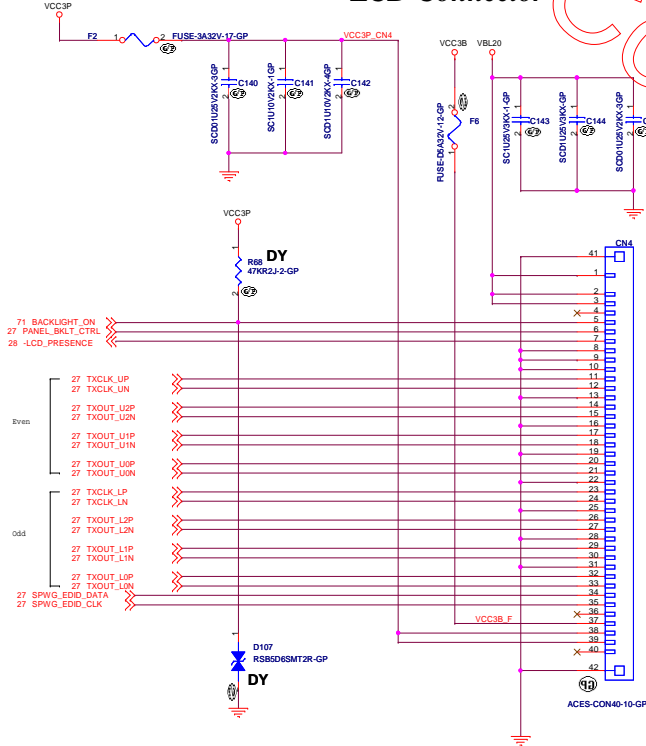
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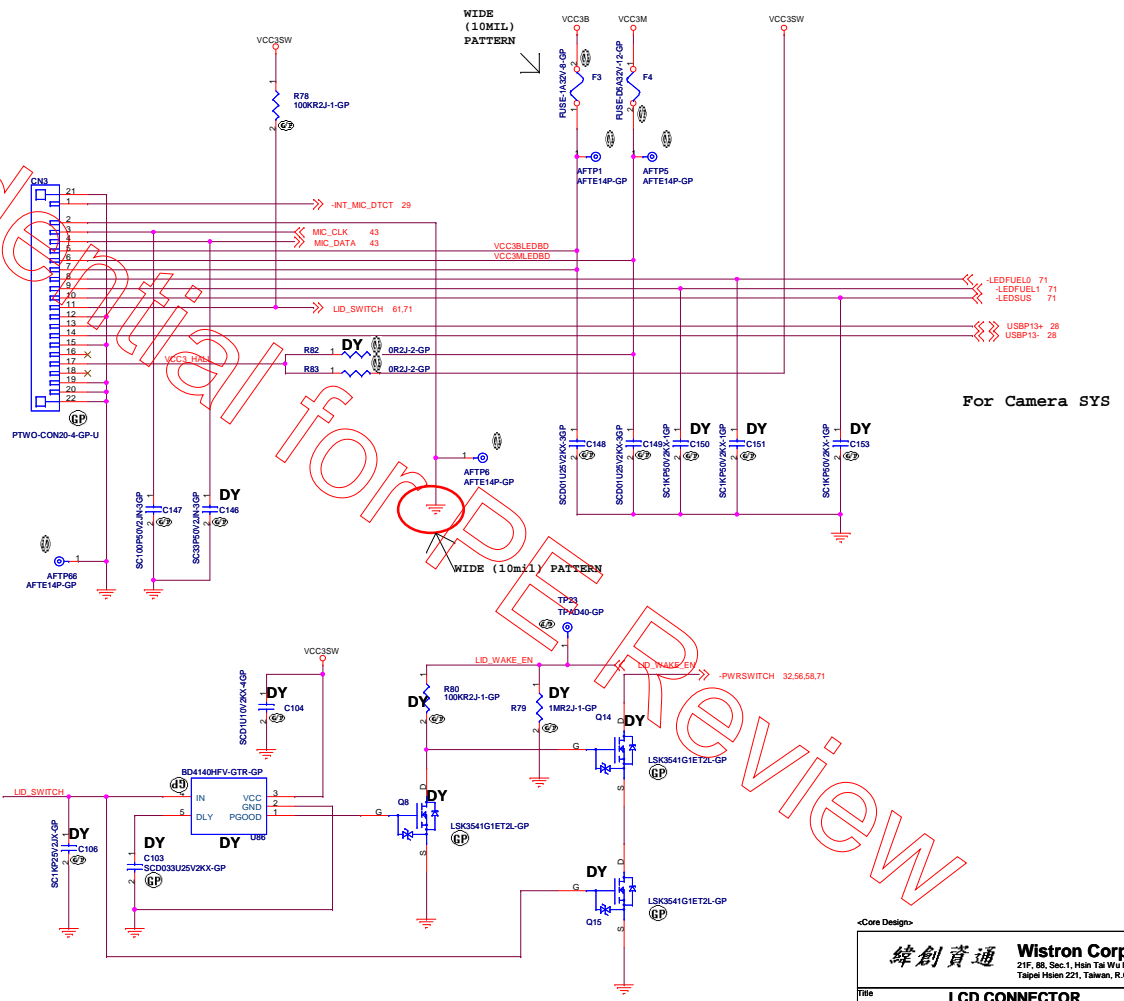
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Size	Document Number		Rev
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LCD Connector



PolySW



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A4	Genesis-1			SC	
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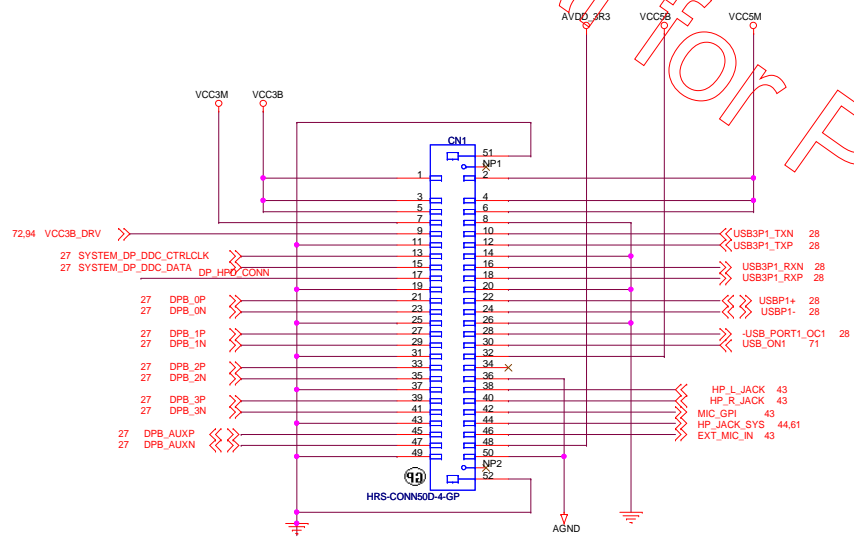
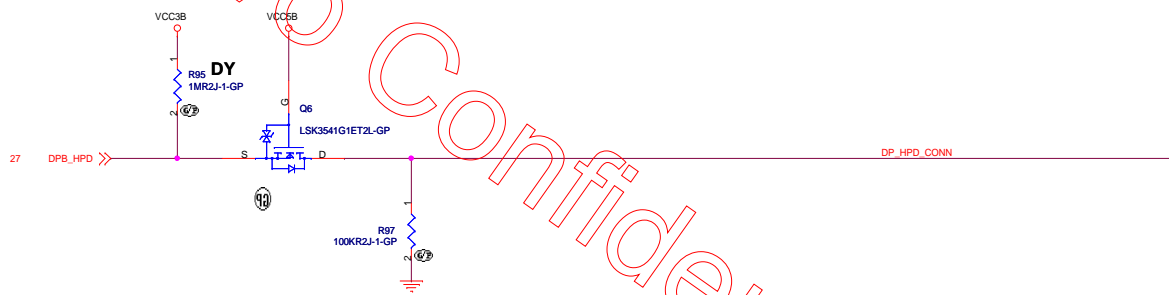
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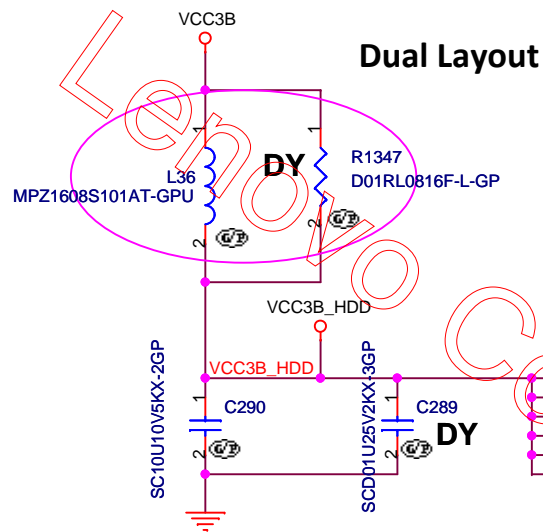
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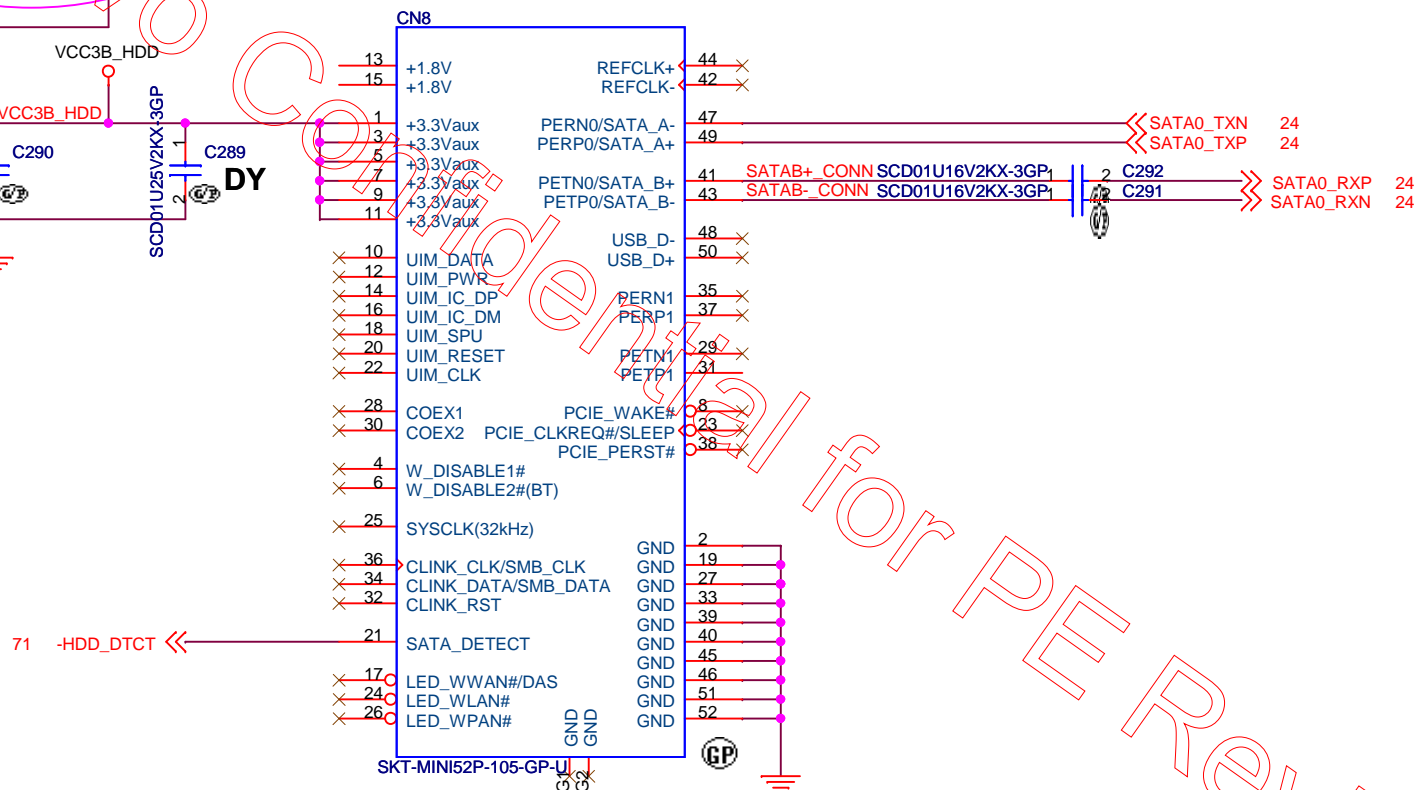
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Size	Document Number		Rev
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SATA CONN



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SATA Connector			
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Document Number

Genesis-1

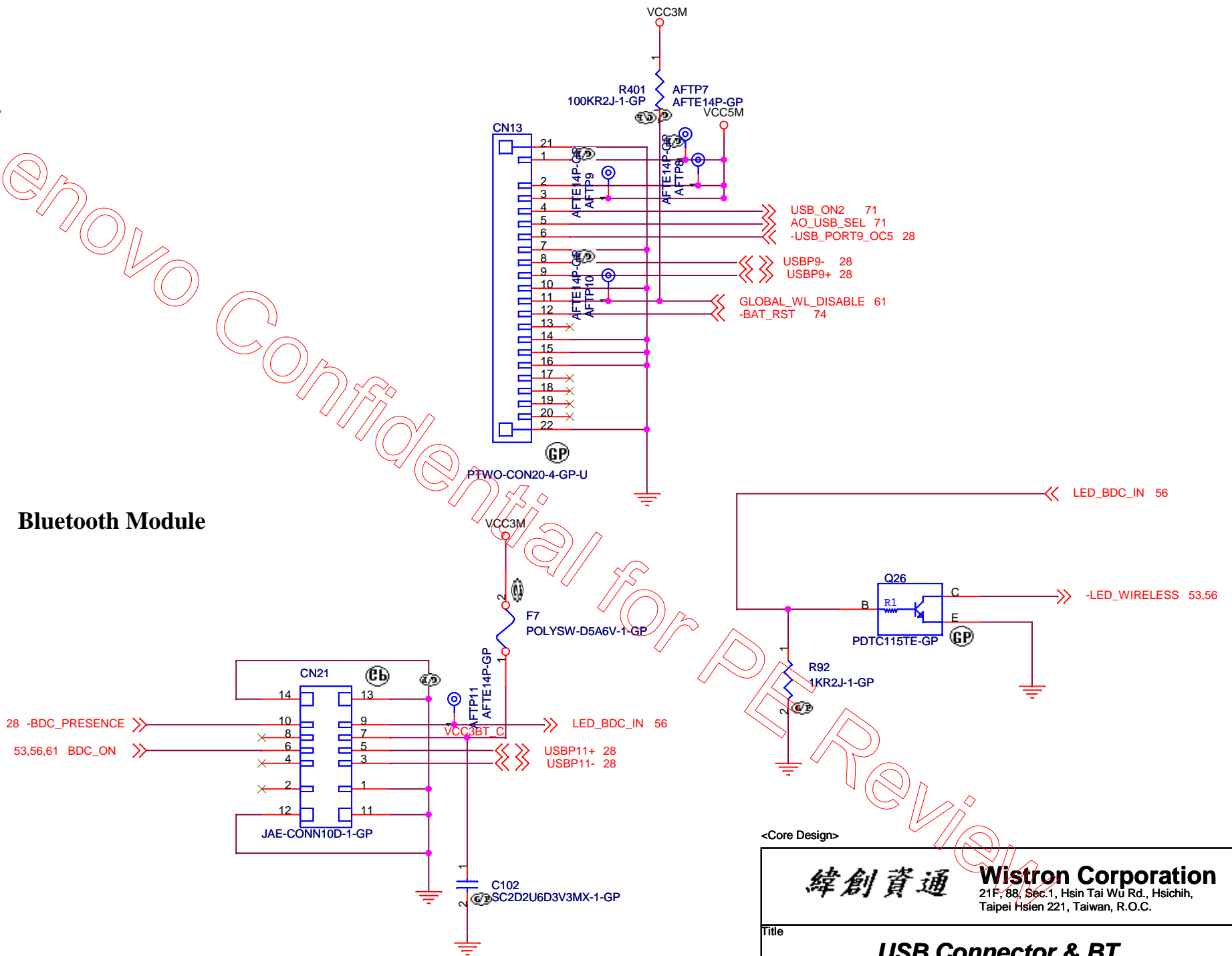
Rev
SC

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Bluetooth Module

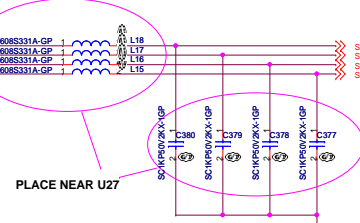
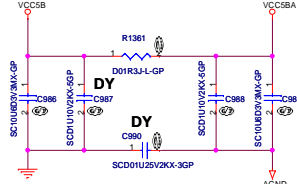
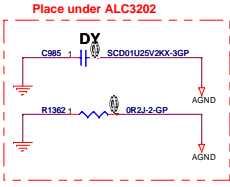
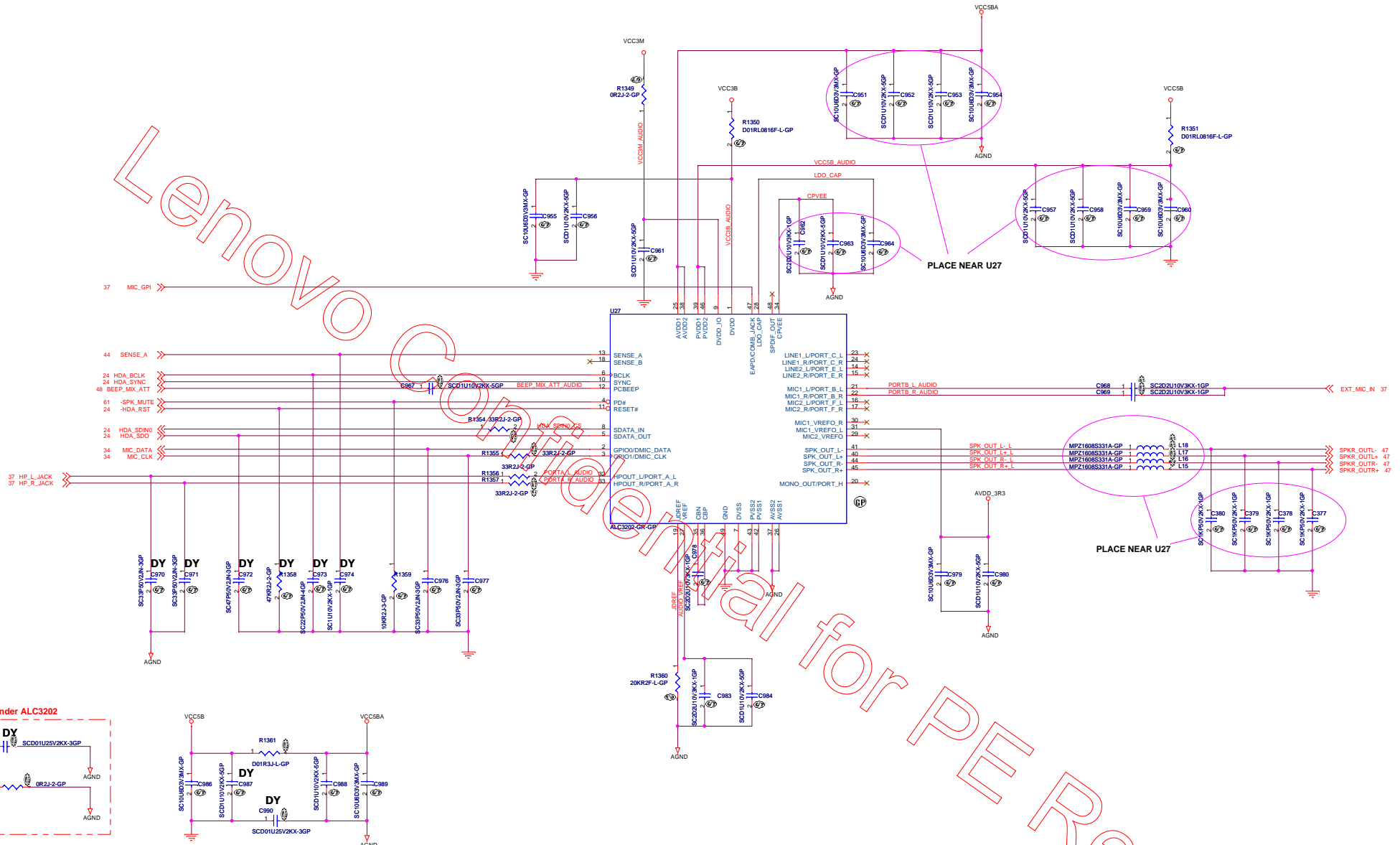


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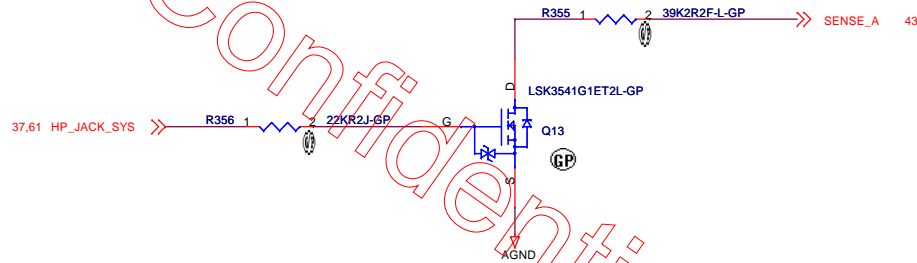
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USB Connector & BT		
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Title			
AUDIO JACK SENSE			
Size	Document Number	Rev	
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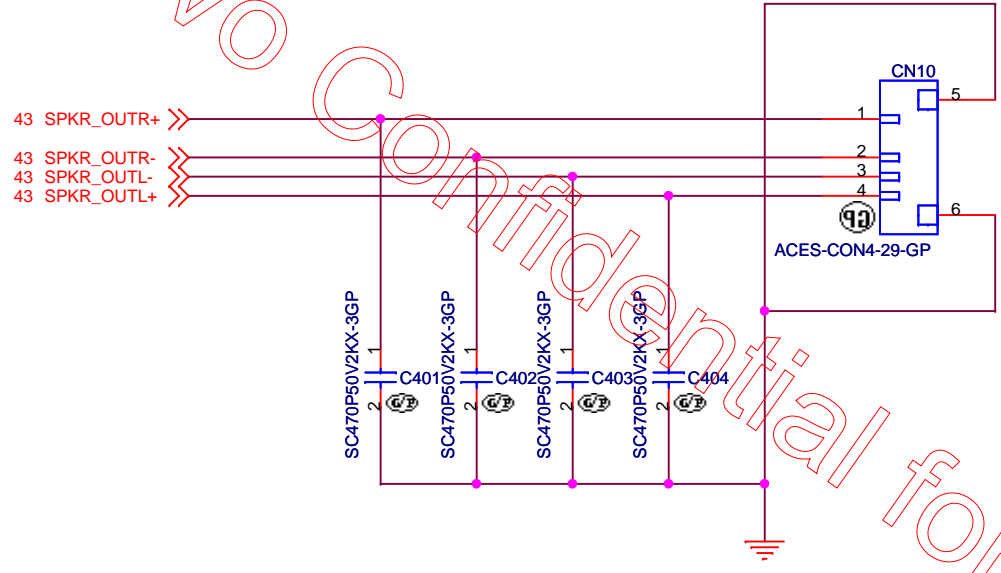
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21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

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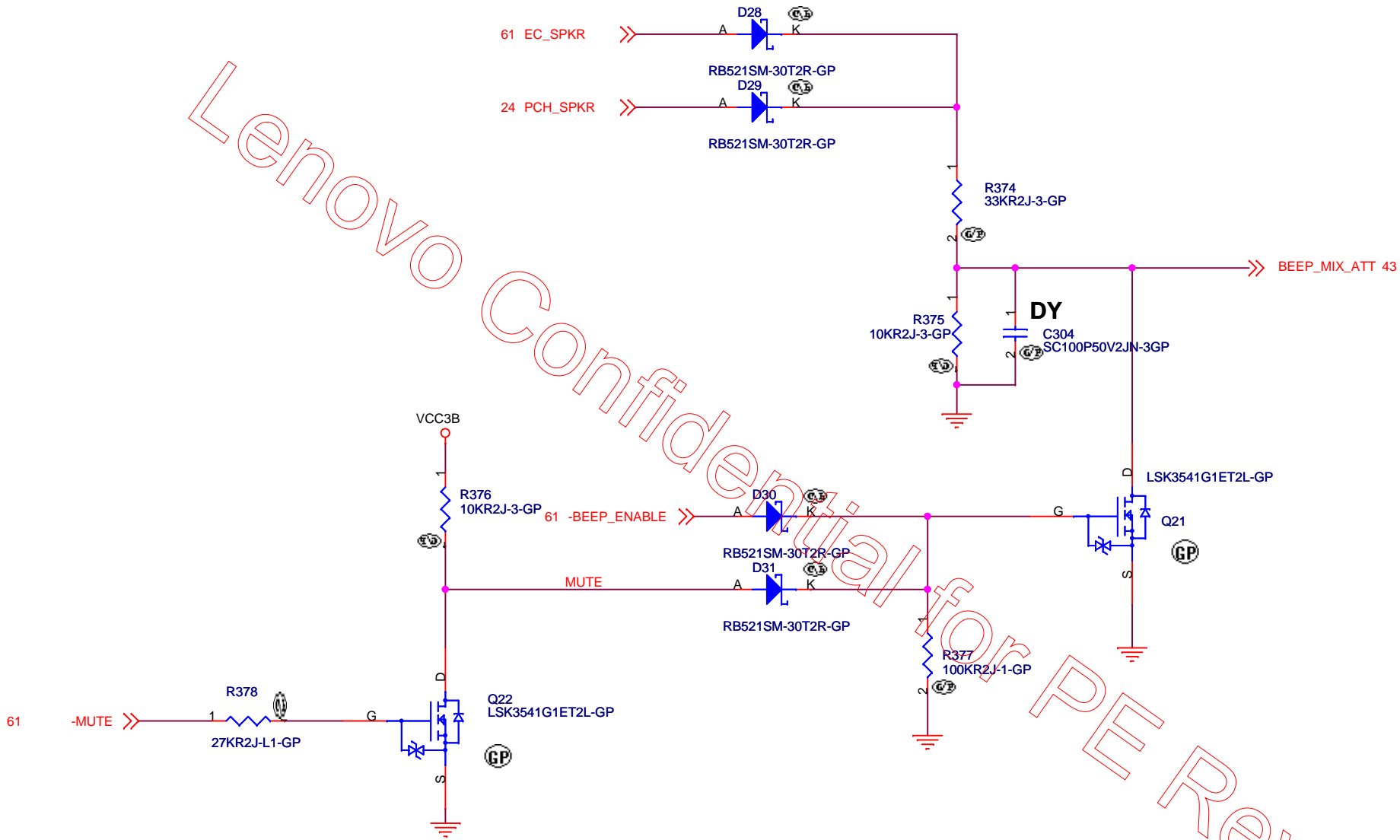
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Size A4	Document Number Genesis-1		Rev SC
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Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Size
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Document Number

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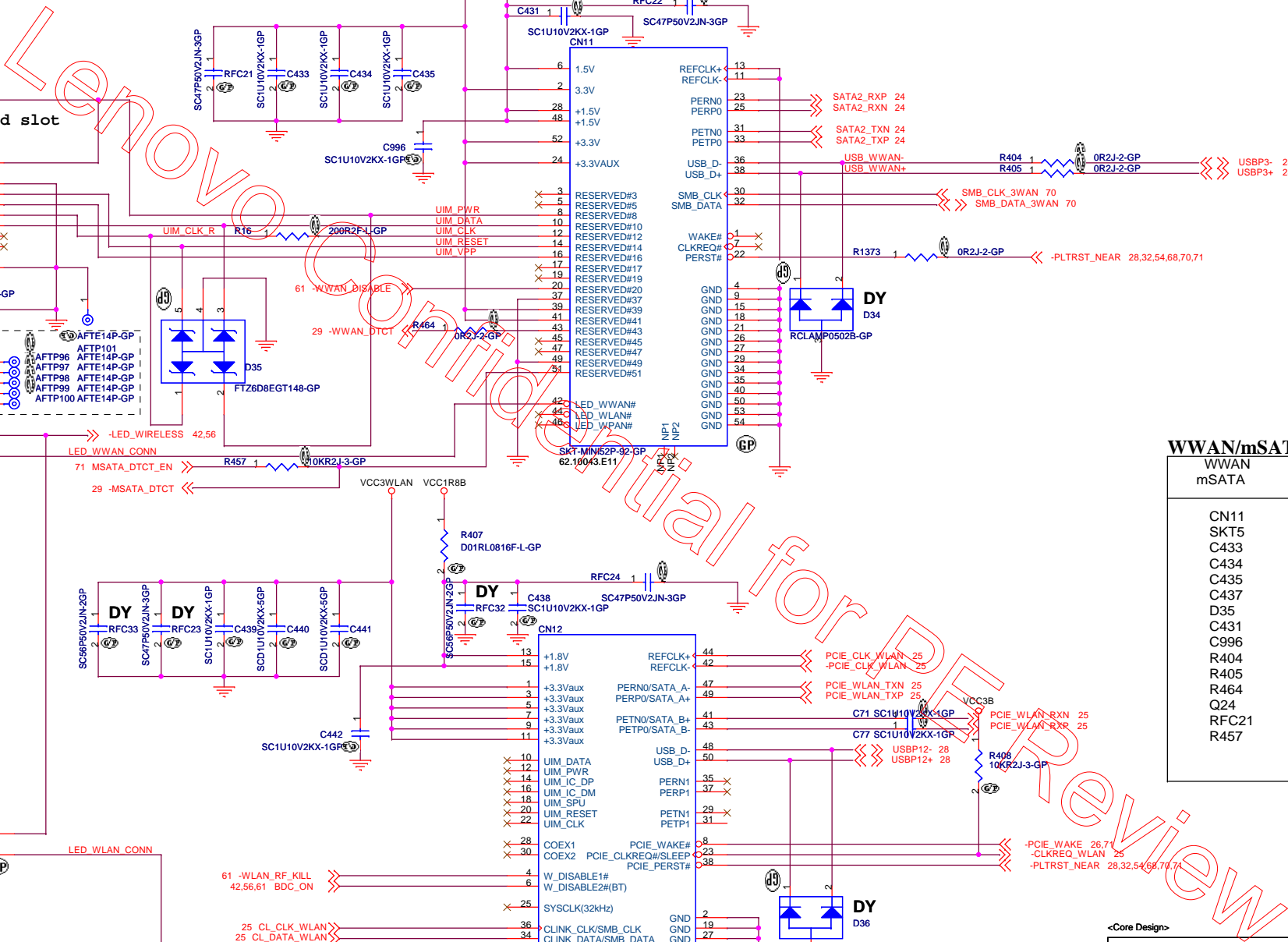
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WWAN/mSATA CONTROL TABLE

WWAN mSATA	YES	NO
CN11	ASM	DY
SKT5	ASM	DY
C433	ASM	DY
C434	ASM	DY
C435	ASM	DY
C437	ASM	DY
D35	ASM	DY
C431	ASM	DY
C996	ASM	DY
R404	ASM	DY
R405	ASM	DY
R464	ASM	DY
Q24	ASM	DY
RFC21	ASM	DY
R457	ASM	DY

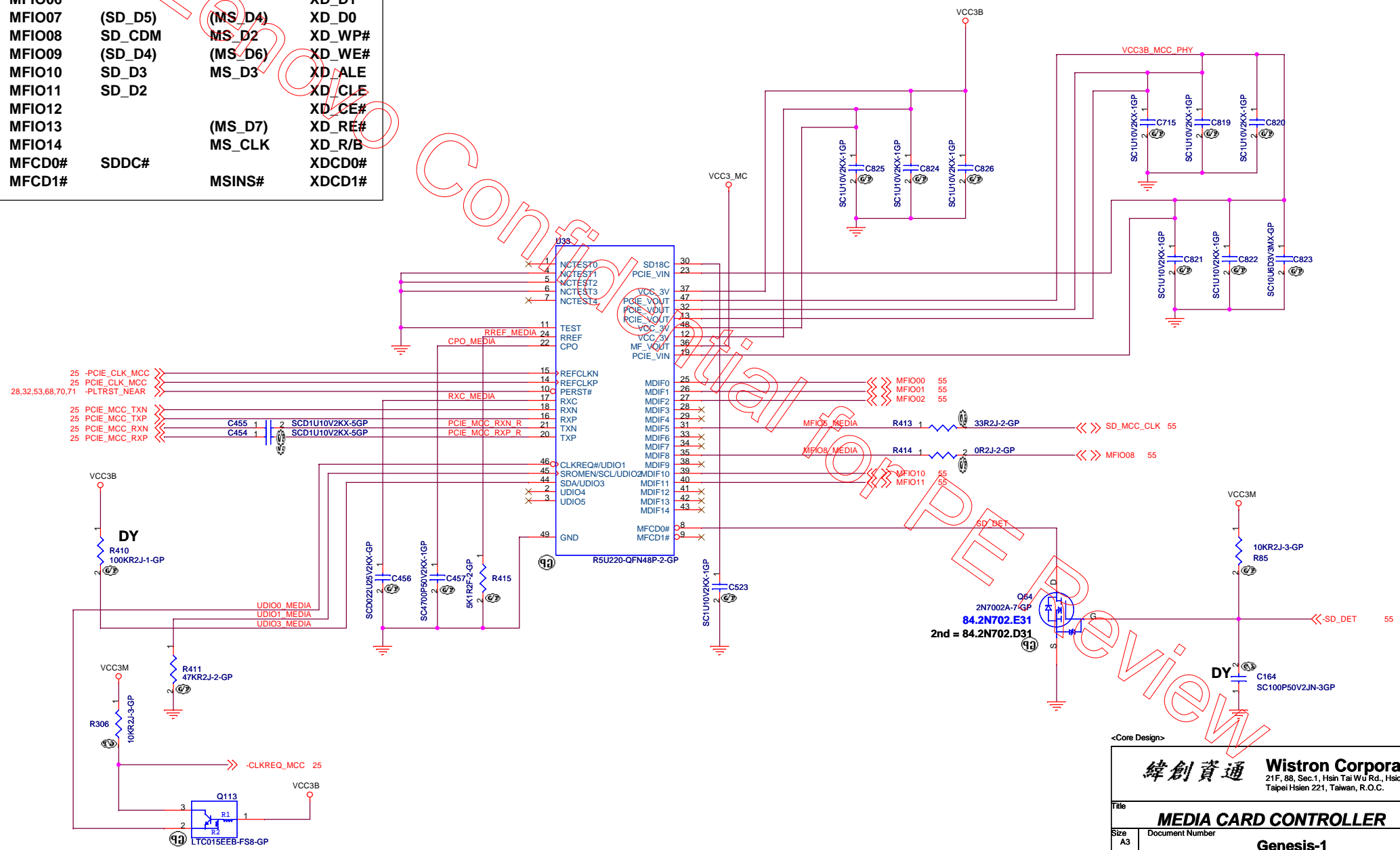
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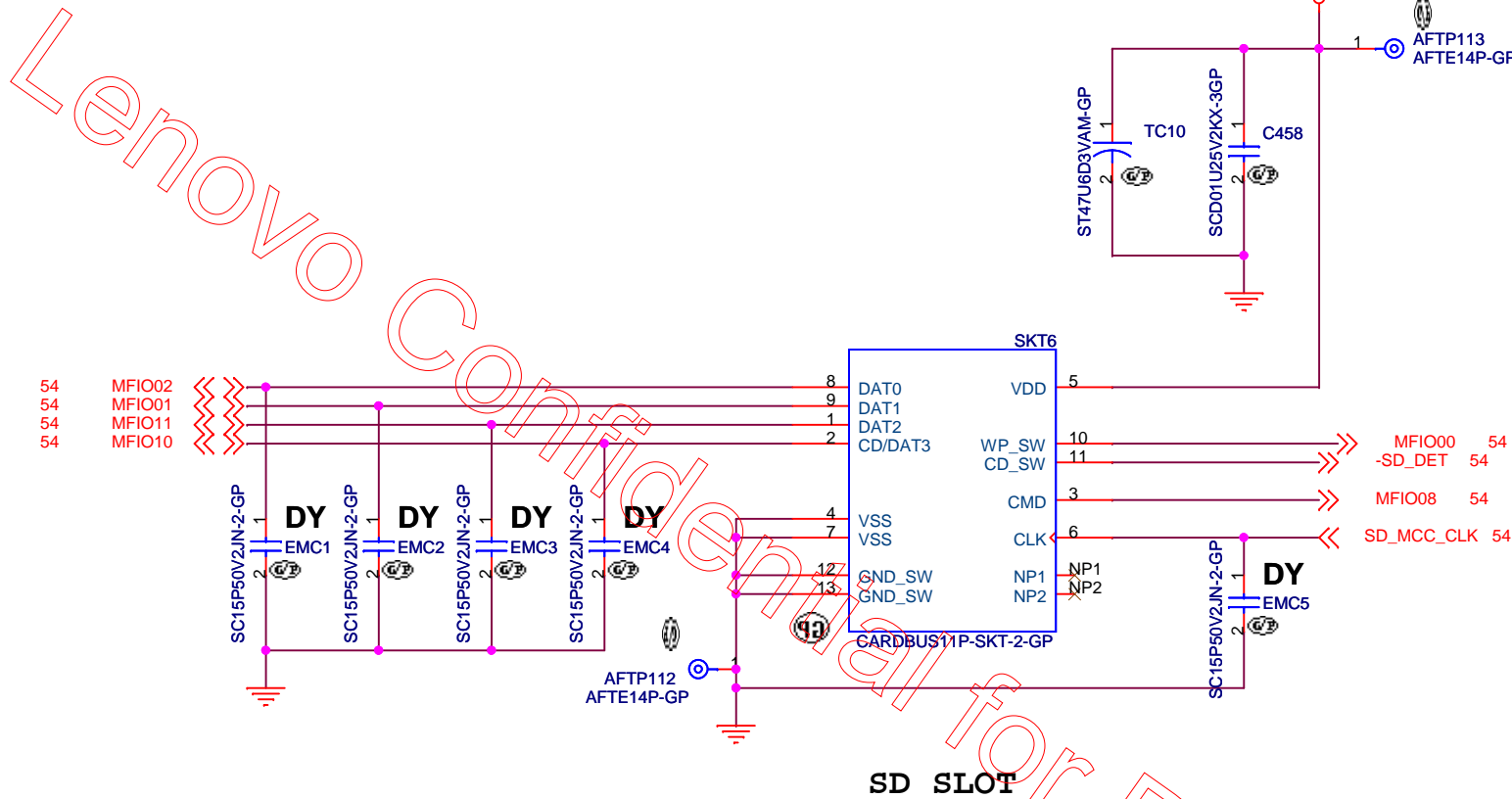
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 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih,
 Taipei Hsien 221, Taiwan, R.O.C.

Title: **MINI CARD SLOT**

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MEDIA I/F	SD/MMC	MEMORYSTICK	XD
MFIO00	SDWP#	MSBS	XD_D7
MFIO01	SD_D1		XD_D6
MFIO02	SD_D0	MS_D1	XD_D5
MFIO03	(SD_D7)		XD_D4
MFIO04	(SD_D6)	(MS_D5)	XD_D3
MFIO05	SD_CLK	MSD0	XD_D2
MFIO06			XD_D1
MFIO07	(SD_D5)	(MS_D4)	XD_D0
MFIO08	SD_CDM	MS_D2	XD_WP#
MFIO09	(SD_D4)	(MS_D6)	XD_WE#
MFIO10	SD_D3	MS_D3	XD_ALE
MFIO11	SD_D2		XD_CLE
MFIO12			XD_CE#
MFIO13		(MS_D7)	XD_RE#
MFIO14		MS_CLK	XD_R/B
MFCD0#	SDDC#		XDCD0#
MFCD1#		MSINS#	XDCD1#





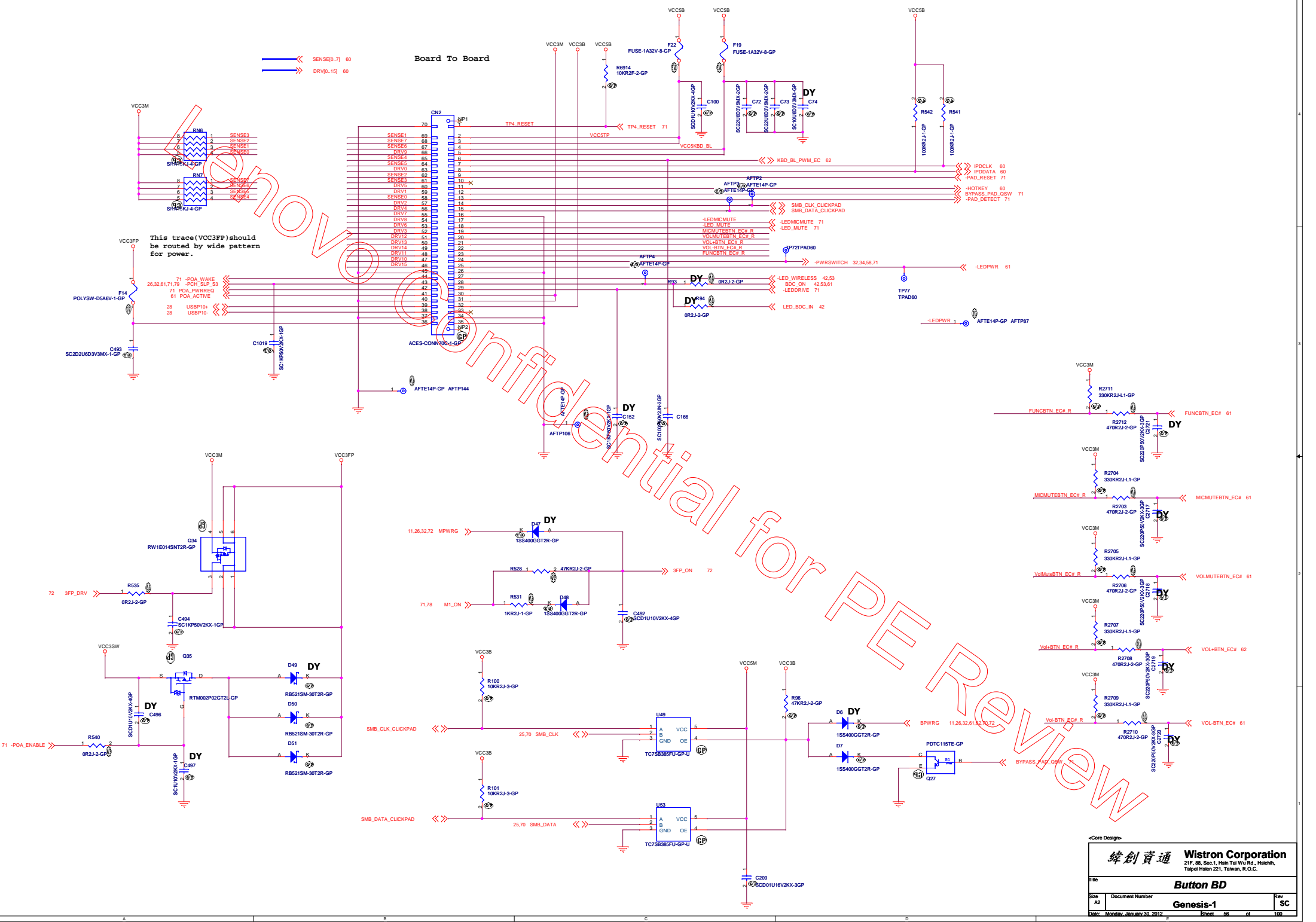
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緯創資通 **Wistron Corporation**
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Title **Media Card Slot**

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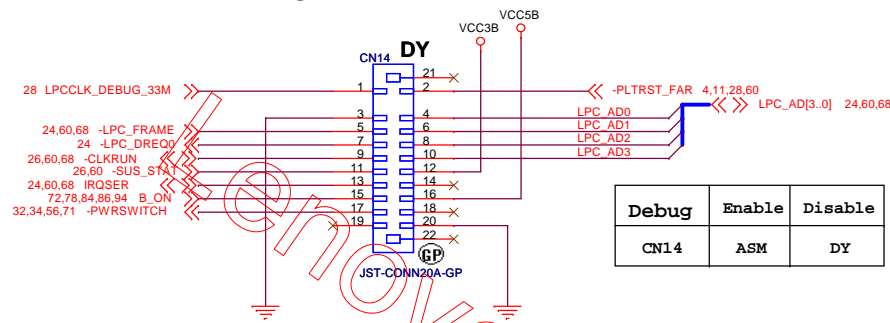
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Size A4	Document Number		Rev SC
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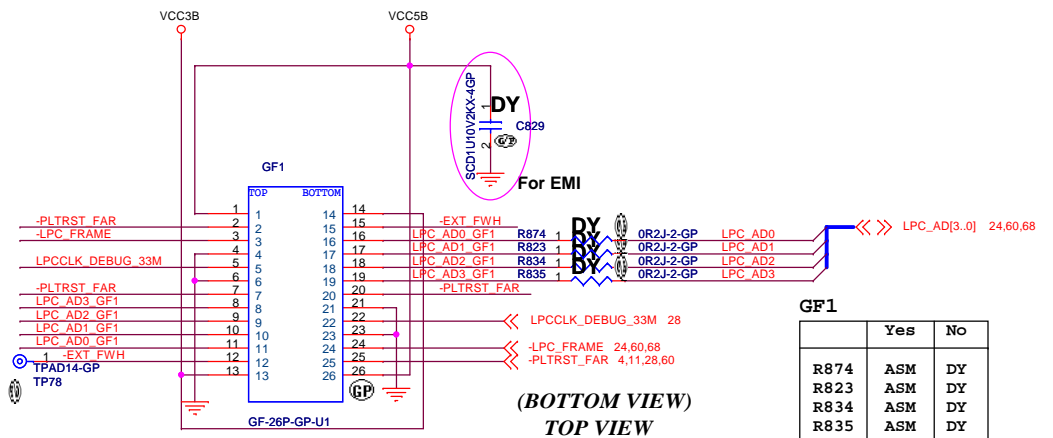
Golden Finger for Debug Board

Debug card connector



Debug	Enable	Disable
CN14	ASM	DY

Put "easy-to-access" place



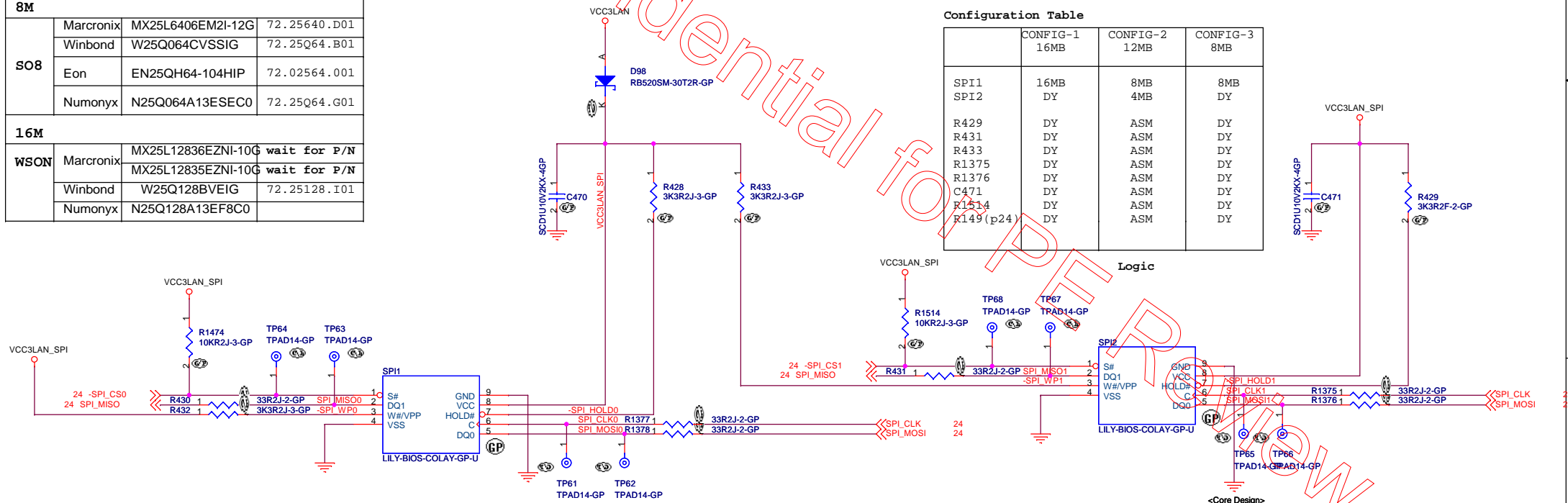
GF1	Yes	No
R874	ASM	DY
R823	ASM	DY
R834	ASM	DY
R835	ASM	DY
R235	ASM	DY

Logic

4M			
SO8	Marcronix	MX25L3206EM2I-12G	72.25320.C01
	Winbond	W25Q032BVSSIG	72.25Q32.A01
	Eon	EN25QH32-104HIP	72.02532.B01
Numonyx	N25Q032A13ESEC0	72.25Q32.C01	
8M			
SO8	Marcronix	MX25L6406EM2I-12G	72.25640.D01
	Winbond	W25Q064CVSSIG	72.25Q64.B01
	Eon	EN25QH64-104HIP	72.02564.001
	Numonyx	N25Q064A13ESEC0	72.25Q64.G01
16M			
WSO8	Marcronix	MX25L12836EZNI-10G	wait for P/N
	Marcronix	MX25L12835EZNI-10G	wait for P/N
	Winbond	W25Q128BVEIG	72.25128.I01
	Numonyx	N25Q128A13EF8C0	

Configuration Table

	CONFIG-1 16MB	CONFIG-2 12MB	CONFIG-3 8MB
SPI1	16MB	8MB	8MB
SPI2	DY	4MB	DY
R429	DY	ASM	DY
R431	DY	ASM	DY
R433	DY	ASM	DY
R1375	DY	ASM	DY
R1376	DY	ASM	DY
C471	DY	ASM	DY
R1514	DY	ASM	DY
R149 (p24)	DY	ASM	DY



SO8 and WSON8 are both supported!

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緯創資通 Wistron Corporation
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Title: **SPI&LPC debug card**

Size A3 Document Number: **Genesis-1** Rev **SC**

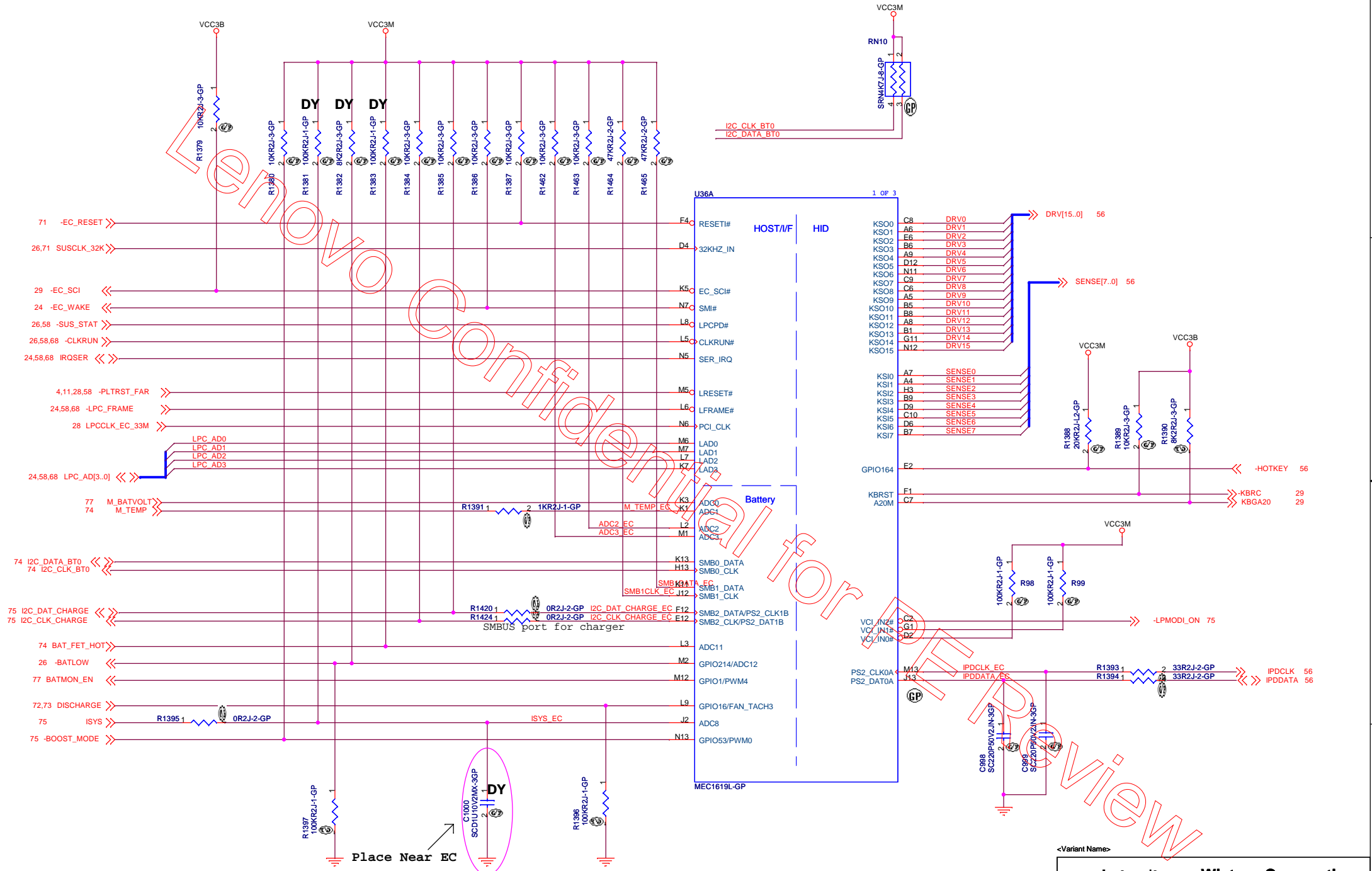
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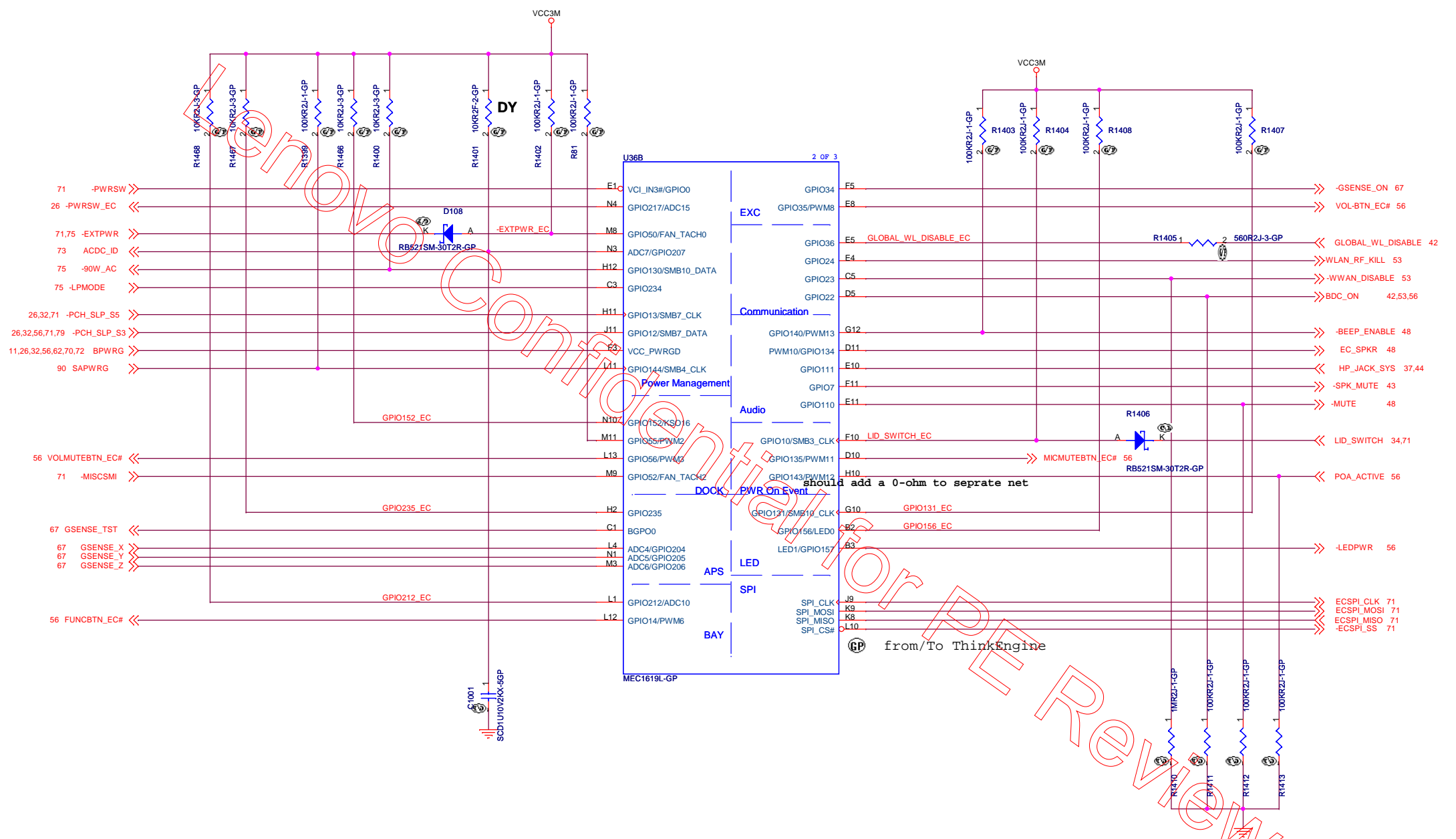
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Size A4	Document Number	Genesis-1	Rev SC
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Place Near EC

<Variant Name>

Wistron Corporation 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Embedded Controller (1/3)	
Title Size Date	Document Number Genesis-1 Sheet 60 of 100
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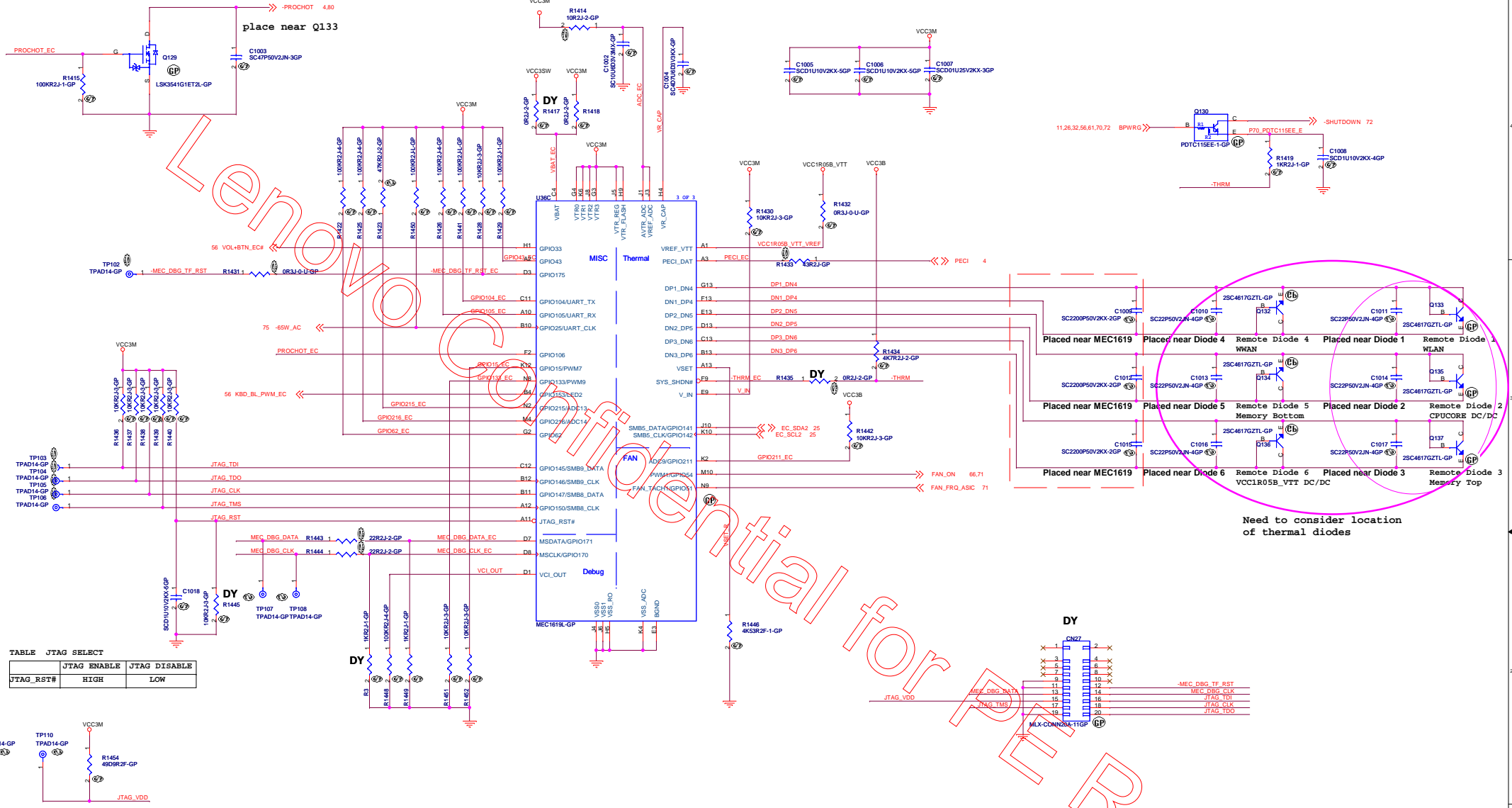


TABLE JTAG SELECT

JTAG_RST#	JTAG ENABLE	JTAG DISABLE
	HIGH	LOW

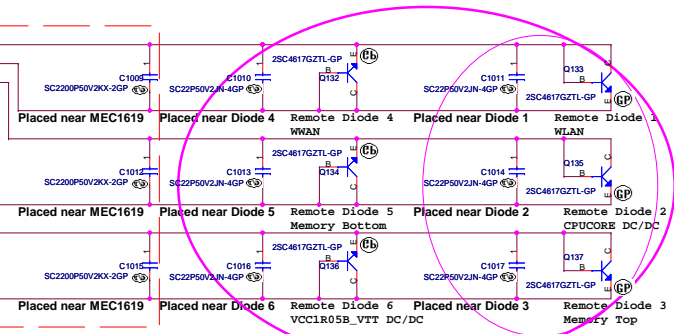
JTAG debug port

	Enable	Disable
R1440	ASM	DY
R1445	DY	ASM
R1454	ASM	DY



trace FIFO debug port

	Enable	Disable
R1443	ASM	DY
R1444	ASM	DY
R3	DY	ASM



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Size	Document Number	Rev	
Custom	Genesis-1	SC	
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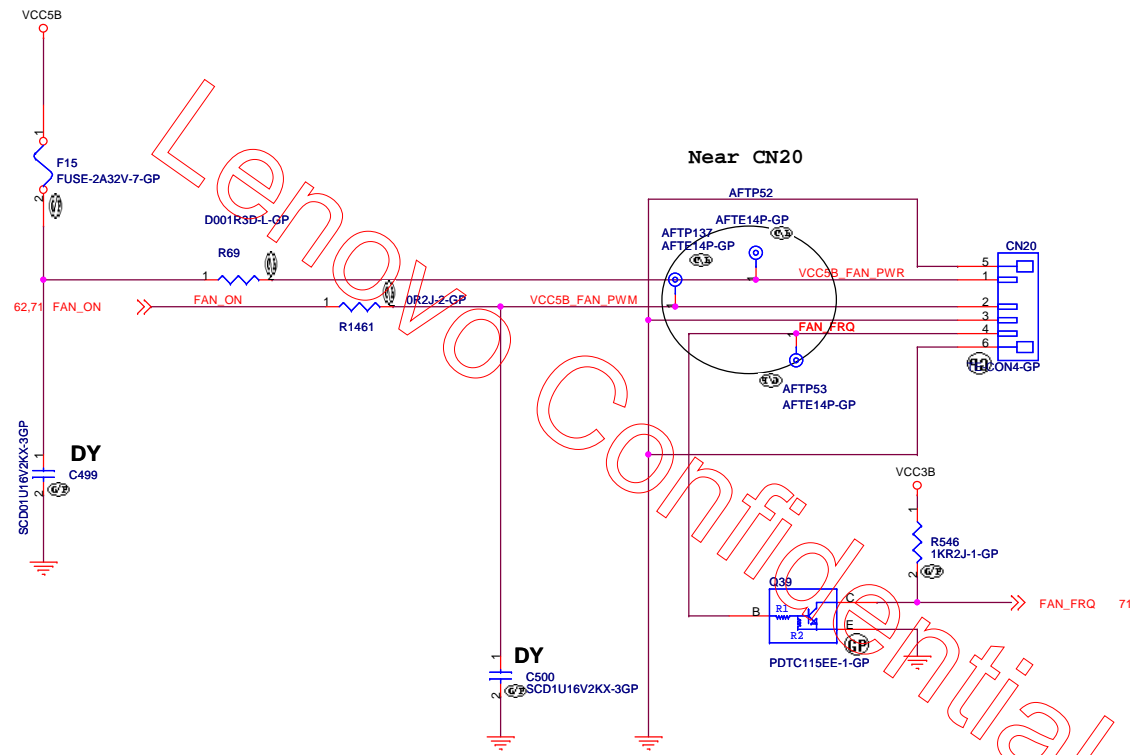
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Rev
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Date: Monday, January 30, 2012

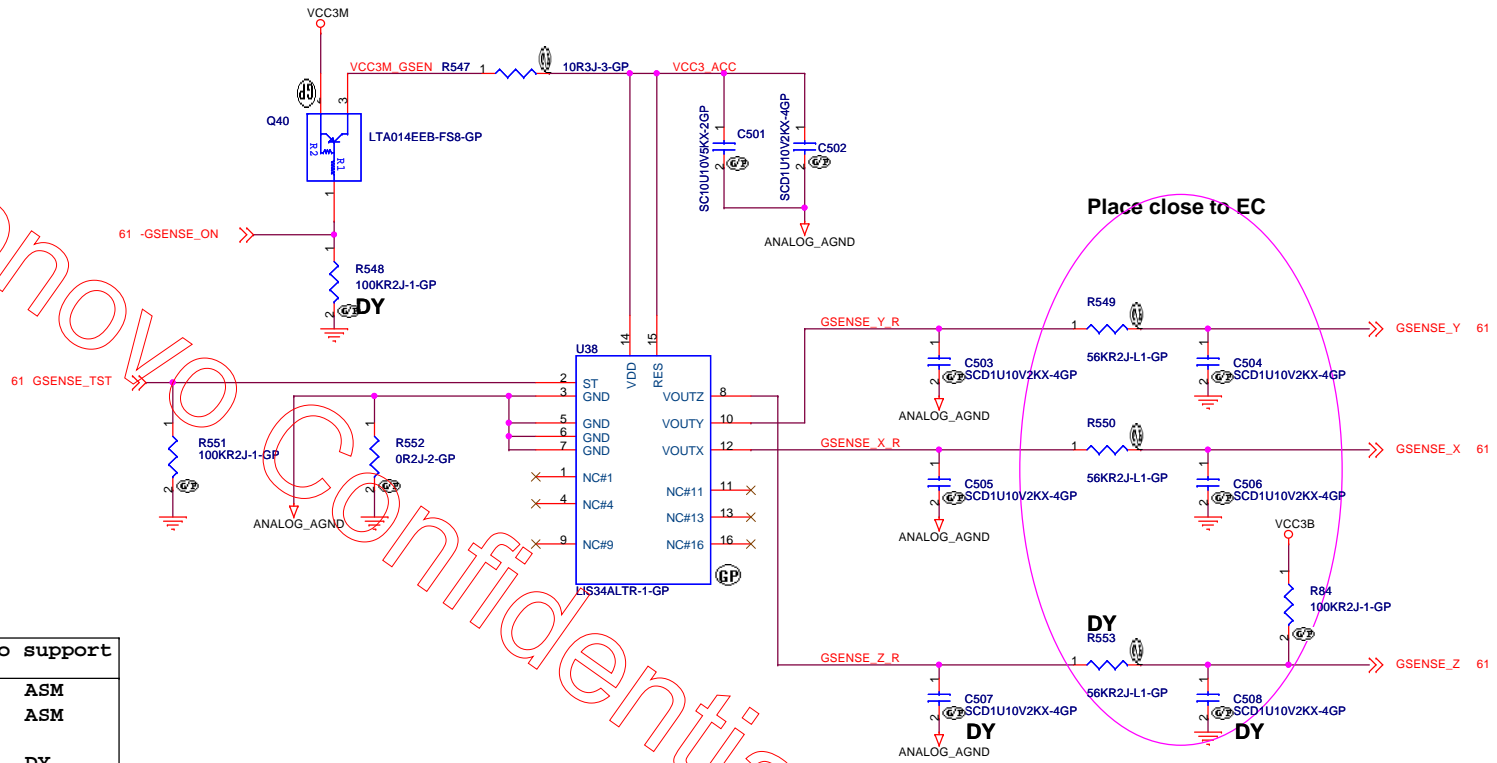
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 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	
FAN Control	
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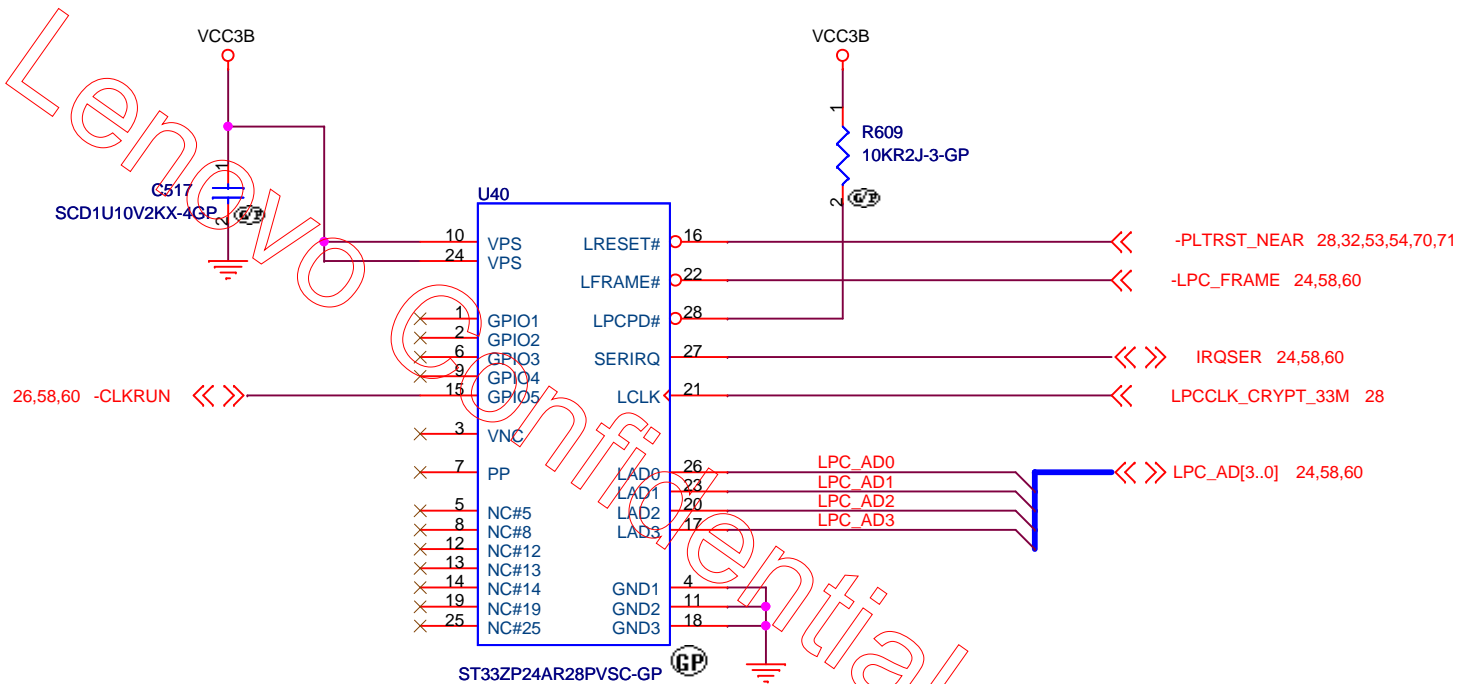
G-sensor	support	no support
R548	DY	ASM
R551	ASM	ASM
U38	ASM	DY
Q40	ASM	DY
R547	ASM	DY
C501	ASM	DY
C502	ASM	DY
R552	ASM	DY
C503	ASM	DY
R549	ASM	DY
C504	ASM	DY
C505	ASM	DY
R550	ASM	DY
C506	ASM	DY
C507	DY	DY
R553	DY	DY
C508	DY	DY
R84	ASM	ASM

U38

Primary	STMicro LIS34AL	41R0828AA
Second	Kionix KXTC8-2850	74.KXTC8.0BZ
Third		

Layout Comment :
 (1) Avoid routing under DCDC switching area.

Width = 6 mil & Spacing = 10 mil
 for three Output traces



	TPM P/N	Firmware
SDV / FVT	ST33ZP24AR28PVRC	1.2.C.0
SIT	ST33ZP24AR28PVSC	1.2.D.0

<Core Design>

 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
TPM	
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Document Number
Genesis-1

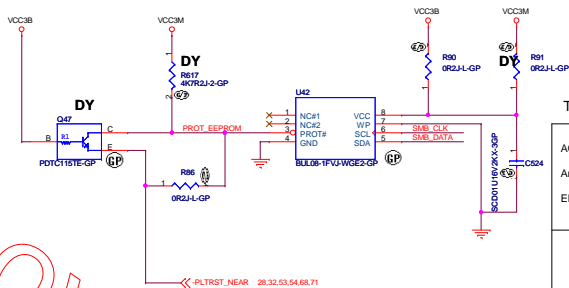
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EEPROM

EEPROM	U42	U36
U42	ASM	DY
C524	ASM	DY
Q47	ASM	DY
R617	ASM	DY

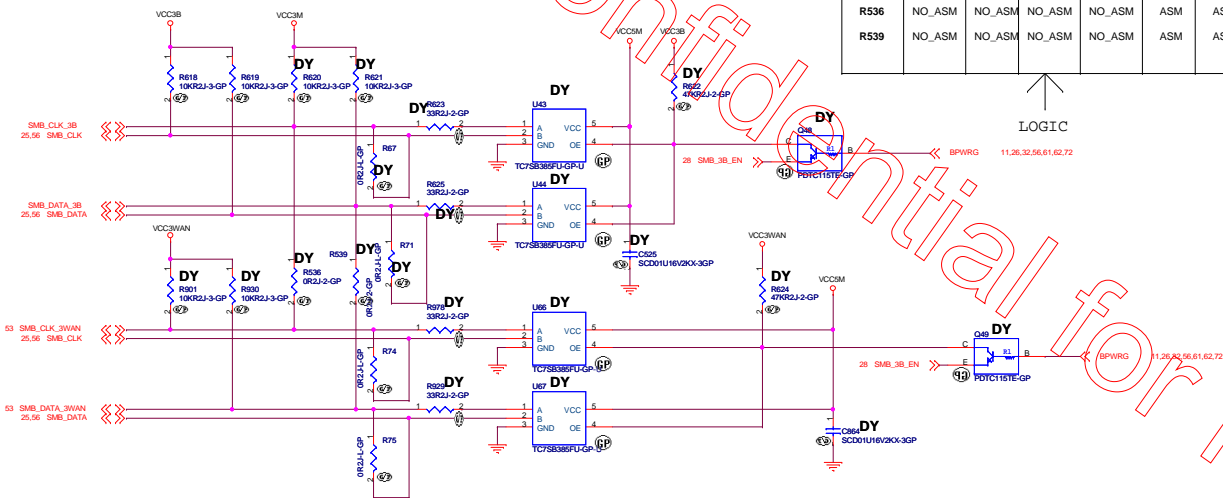


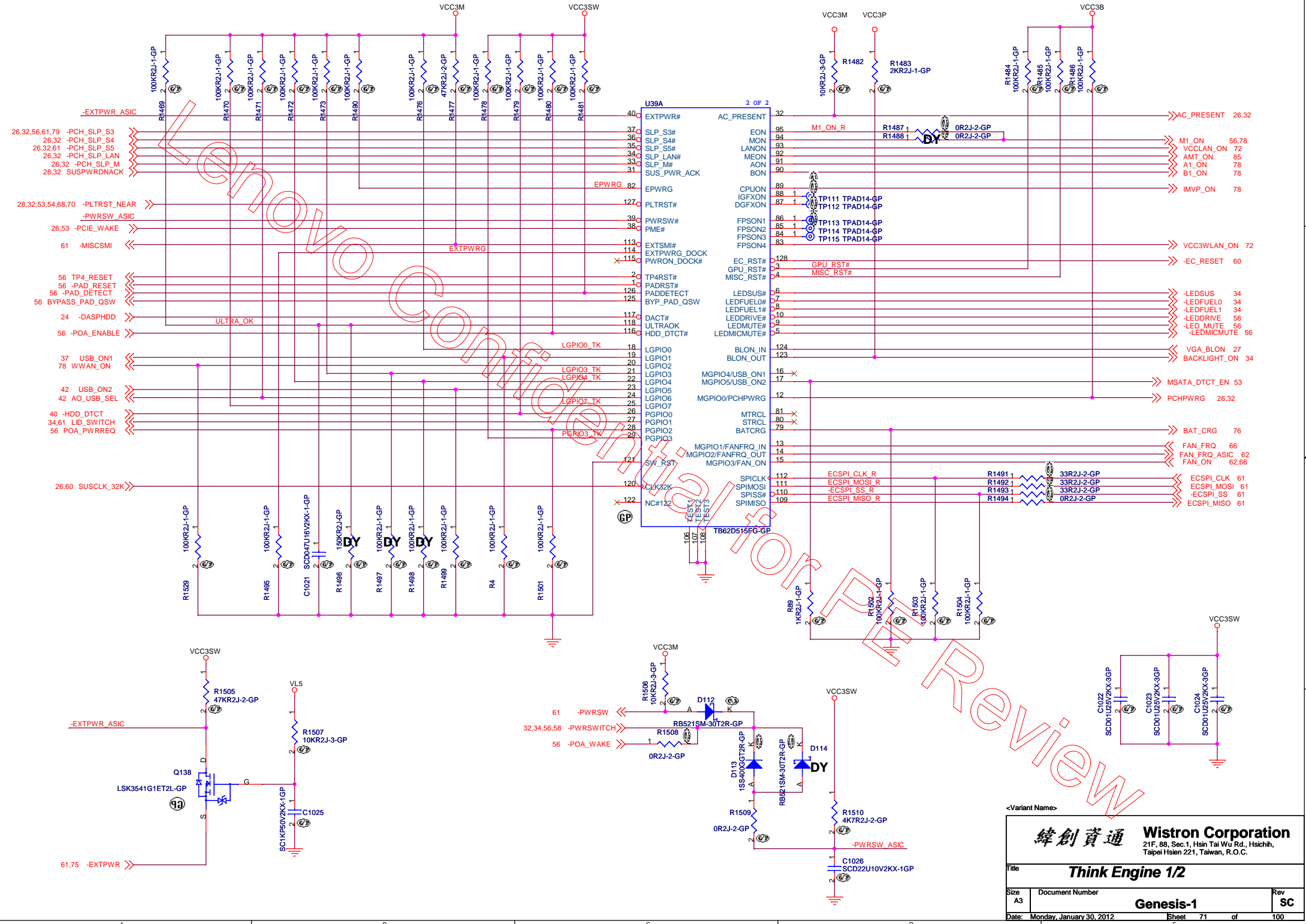
Vendor	U42	Part Number
1st	ROHM	BUL08-1FVJ-W 72.BUL08.AOQ
2nd	PHILIPS	FCA24S08ADP 72.24S08.AOQ
3rd	Sanyo	LE26CAPO8TT 72.26C08.00R

TABLE

AOAC	YES	YES	YES	YES	NO	NO	NO	NO
Anti Theft	YES	YES	NO	NO	YES	YES	NO	NO
EEPROM	U42	U36	U42	U36	U42	U36	U42	U36
U66	ASM	ASM	NO_ASM	NO_ASM	NO_ASM	NO_ASM	NO_ASM	NO_ASM
U67	ASM	ASM	NO_ASM	NO_ASM	NO_ASM	NO_ASM	NO_ASM	NO_ASM
C864	ASM	ASM	NO_ASM	NO_ASM	NO_ASM	NO_ASM	NO_ASM	NO_ASM
R978	ASM	ASM	NO_ASM	NO_ASM	NO_ASM	NO_ASM	NO_ASM	NO_ASM
R929	ASM	ASM	NO_ASM	NO_ASM	NO_ASM	NO_ASM	NO_ASM	NO_ASM
R901	ASM	ASM	NO_ASM	NO_ASM	NO_ASM	NO_ASM	NO_ASM	NO_ASM
R930	ASM	ASM	NO_ASM	NO_ASM	NO_ASM	NO_ASM	NO_ASM	NO_ASM
R624	ASM	ASM	NO_ASM	NO_ASM	NO_ASM	NO_ASM	NO_ASM	NO_ASM
Q49	ASM	NO_ASM	NO_ASM	NO_ASM	NO_ASM	NO_ASM	NO_ASM	NO_ASM
Q48	ASM	NO_ASM	ASM	NO_ASM	ASM	NO_ASM	ASM	NO_ASM
R536	NO_ASM	NO_ASM	NO_ASM	NO_ASM	ASM	ASM	NO_ASM	NO_ASM
R539	NO_ASM	NO_ASM	NO_ASM	NO_ASM	ASM	ASM	NO_ASM	NO_ASM

LOGIC



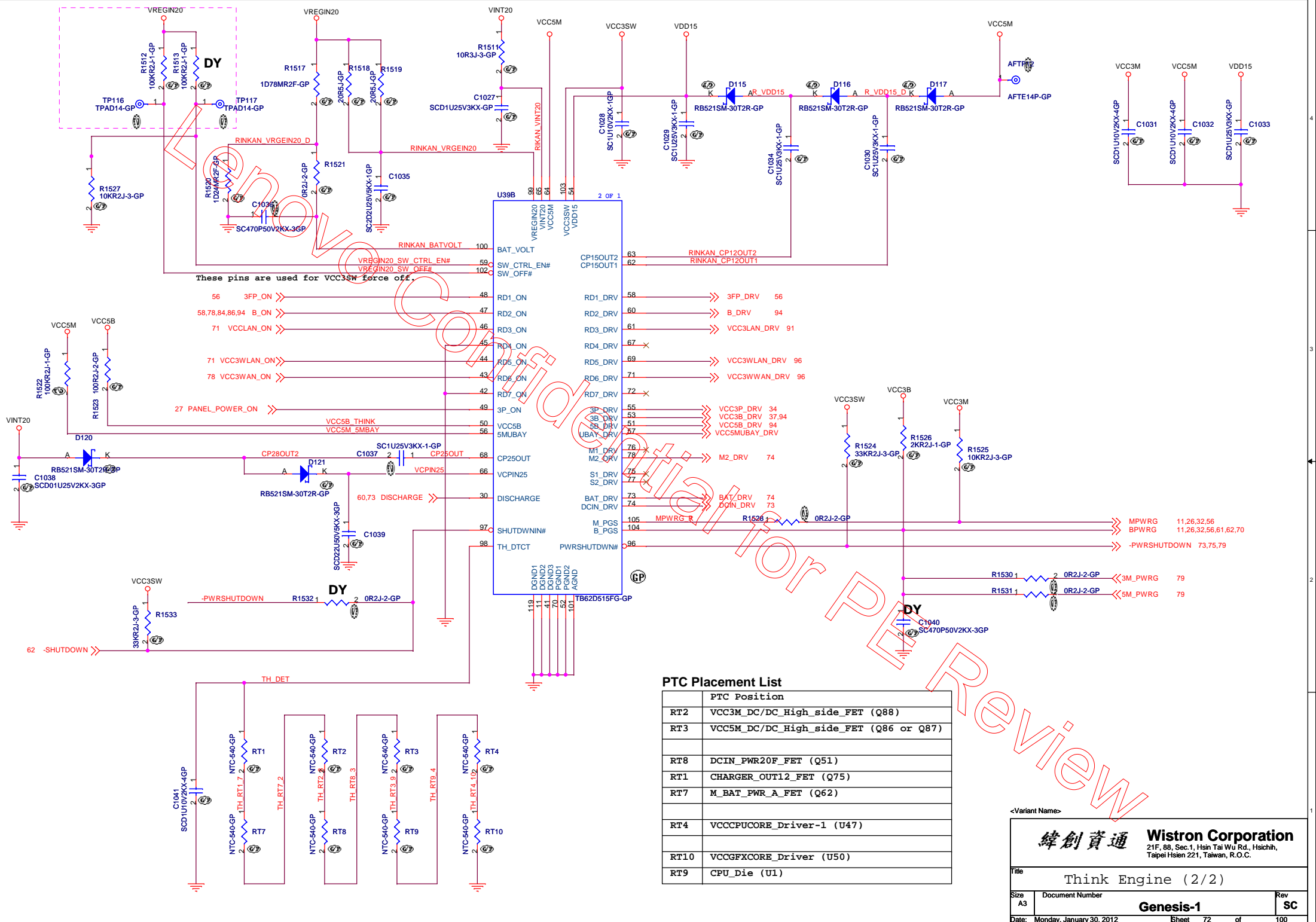


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Think Engine 1/2

Title	Think Engine 1/2	
Size	Document Number	Rev
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These pins are used for VCC3SW force off.

- 56 3FP_ON >>> RD1_ON 48 RD1_DRV 58 >>> 3FP_DRV 56
- 58,78,84,86,94 B_ON >>> RD2_ON 47 RD2_DRV 60 >>> B_DRV 94
- 71 VCCLAN_ON >>> RD3_ON 46 RD3_DRV 61 >>> VCC3LAN_DRV 91
- 71 VCC3WLAN_ON >>> RD4_ON 45 RD4_DRV 67 >>> VCC3WLAN_DRV 96
- 78 VCC3WAN_ON >>> RD5_ON 44 RD5_DRV 69 >>> VCC3WAN_DRV 96
- 27 PANEL_POWER_ON >>> RD6_ON 43 RD6_DRV 71 >>> VCC3WAN_DRV 96
- 3P_ON >>> RD7_ON 42 RD7_DRV 72 >>> VCC3WAN_DRV 96
- 3P_DRV 55 >>> VCC3P_DRV 34
- 3B_DRV 53 >>> VCC3B_DRV 37,94
- 5B_DRV 51 >>> VCC5B_DRV 94
- 5MUBAY 56 >>> VCC5MUBAY_DRV
- CP28OUT2 68 >>> M1_DRV 76 >>> M2_DRV 74
- CP25OUT 66 >>> M2_DRV 77
- 60,73 DISCHARGE >>> S1_DRV 75 >>> BAT_DRV 74
- DISCHARGE 30 >>> S2_DRV 74 >>> DCIN_DRV 74
- SHUTDWNIN# 97 >>> M_PG5 105 >>> MPWRG 11,26,32,56
- TH_DTCT 98 >>> B_PG5 104 >>> BPWRG 11,26,32,56,61,62,70
- TH_DET >>> PWRSHUTDOWN >>> -PWRSHUTDOWN 73,75,79
- TH_RT1 >>> 3M_PWRG 79
- TH_RT2 >>> 5M_PWRG 79

PTC Placement List

PTC	PTC Position
RT2	VCC3M_DC/DC_High_side_FET (Q88)
RT3	VCC5M_DC/DC_High_side_FET (Q86 or Q87)
RT8	DCIN_PWR20F_FET (Q51)
RT1	CHARGER_OUT12_FET (Q75)
RT7	M_BAT_PWR_A_FET (Q62)
RT4	VCCCPUCORE_Driver-1 (U47)
RT10	VCCGFXCORE_Driver (U50)
RT9	CPU_Die (U1)

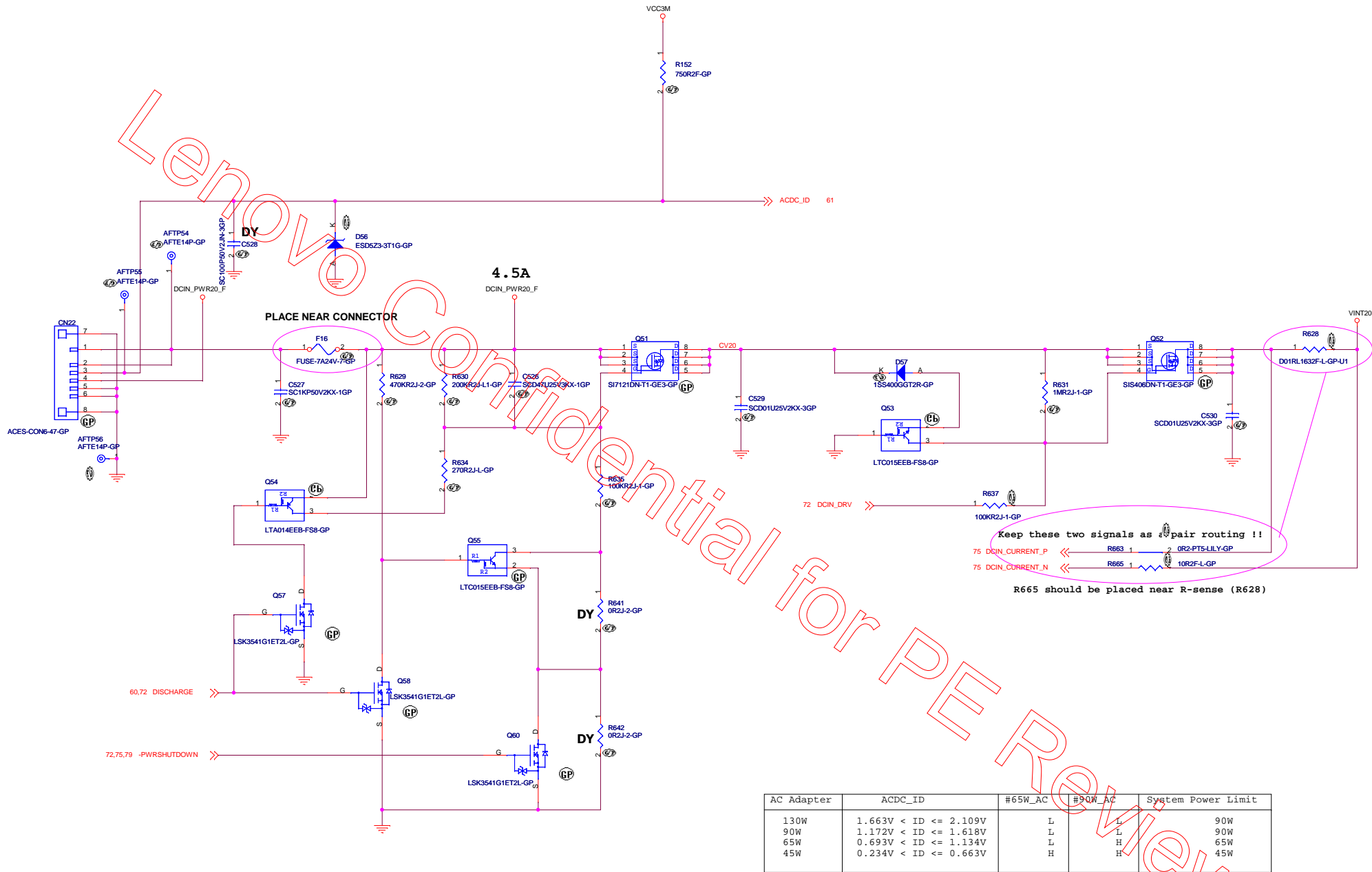
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緯創資通 Wistron Corporation
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Title: Think Engine (2/2)

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Keep these two signals as a pair routing !!
 75 DCIN_CURRENT_P << R663 1 2 OR2-PT5-LILY-GP
 75 DCIN_CURRENT_N << R665 1 10R2F-L-GP
 R665 should be placed near R-sense (R628)

AC Adapter	ACDC_ID	#65W_AC	#90W_AC	System Power Limit
130W	1.663V < ID <= 2.109V	L	L	90W
90W	1.172V < ID <= 1.618V	L	L	90W
65W	0.693V < ID <= 1.134V	L	H	65W
45W	0.234V < ID <= 0.663V	H	H	45W

PEAK SHIFT	YES	NO
R641	NO-ASM	ASM
R629	ASM	NO-ASM
Q58	ASM	NO-ASM
Q55	ASM	NO-ASM

Logic

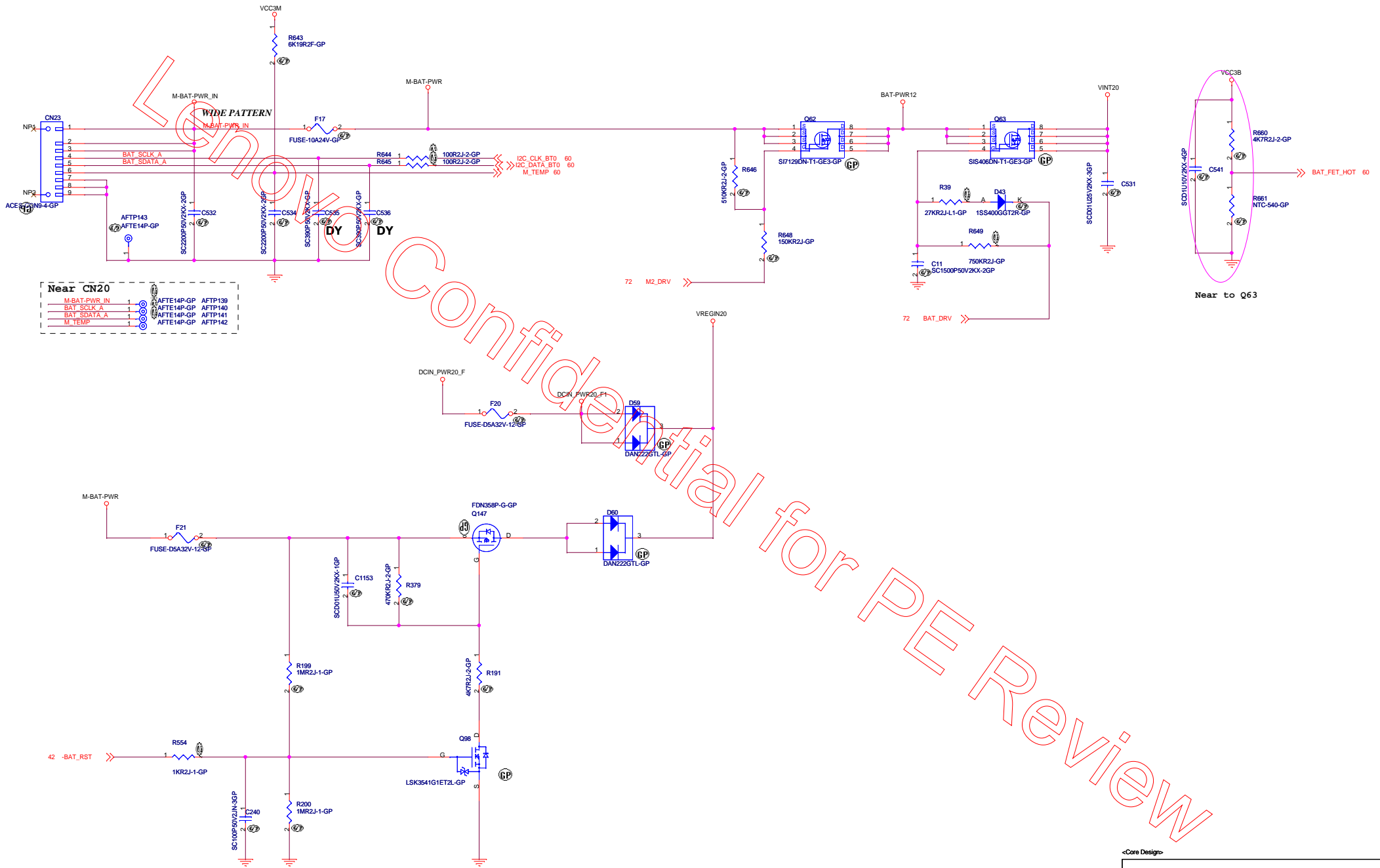
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緯創資通 Wistron Corporation
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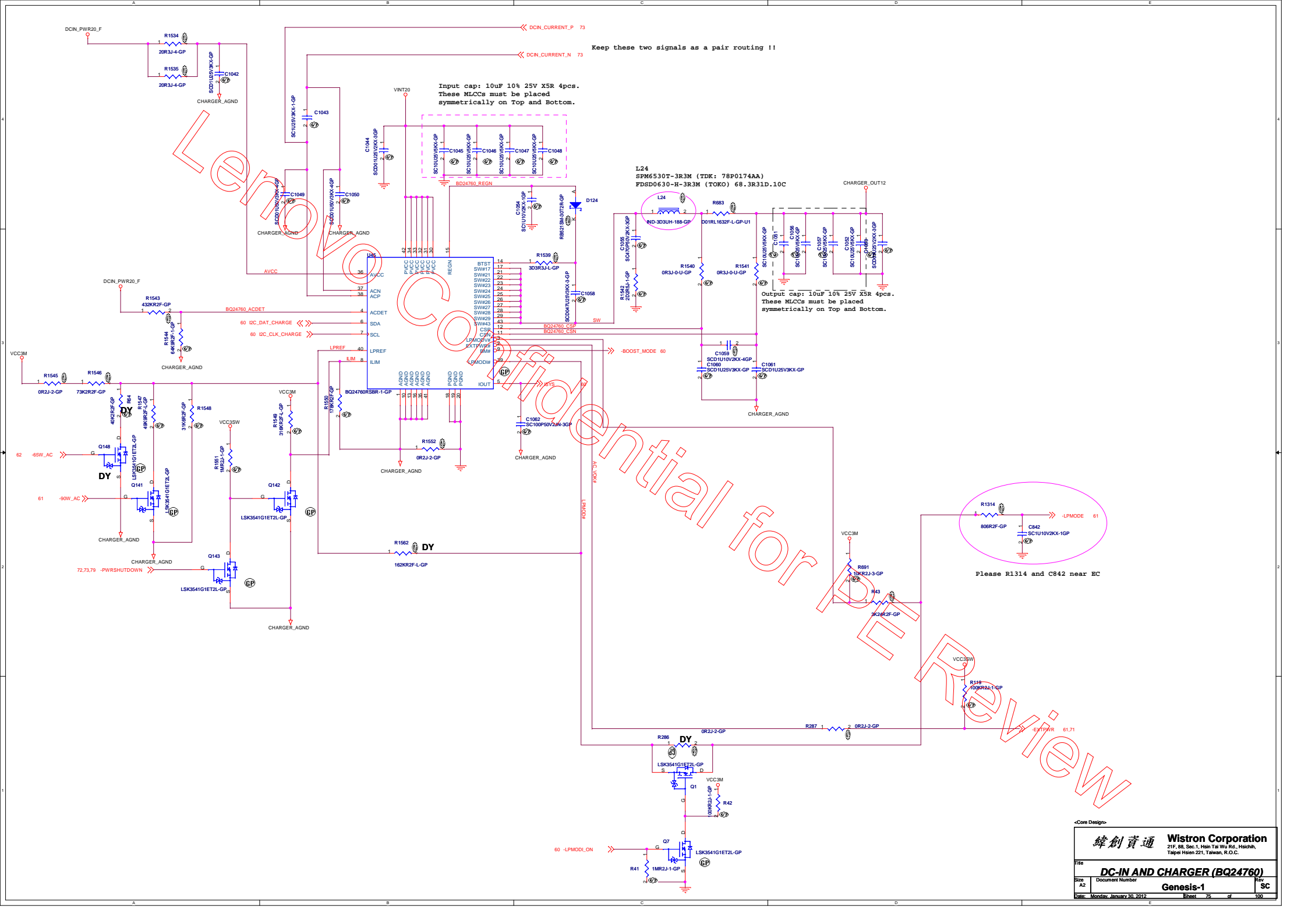
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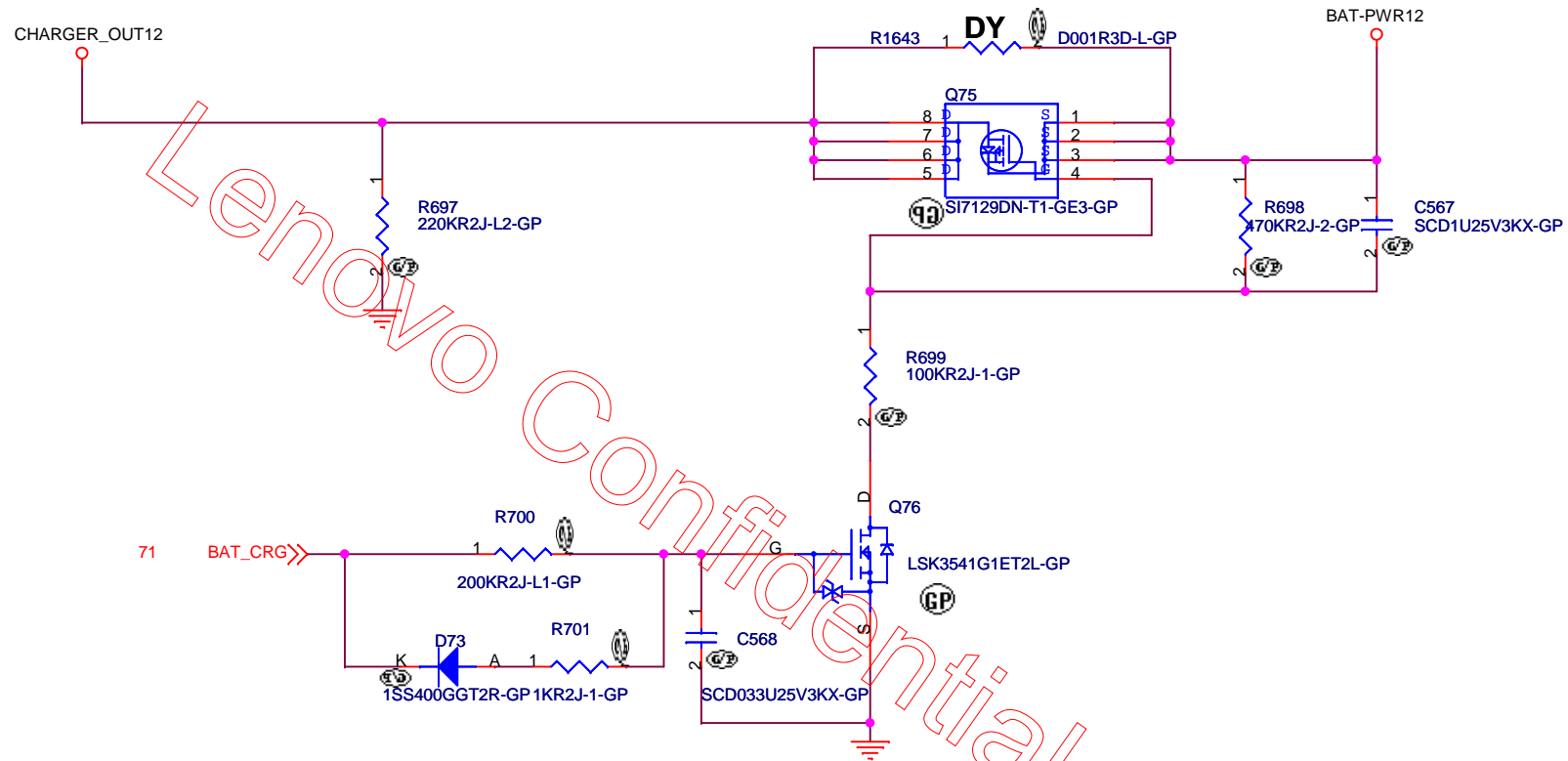
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Date: Monday, January 30, 2012 Sheet 73 of 100



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Title

CHARGER SELECT

Size
A4

Document Number

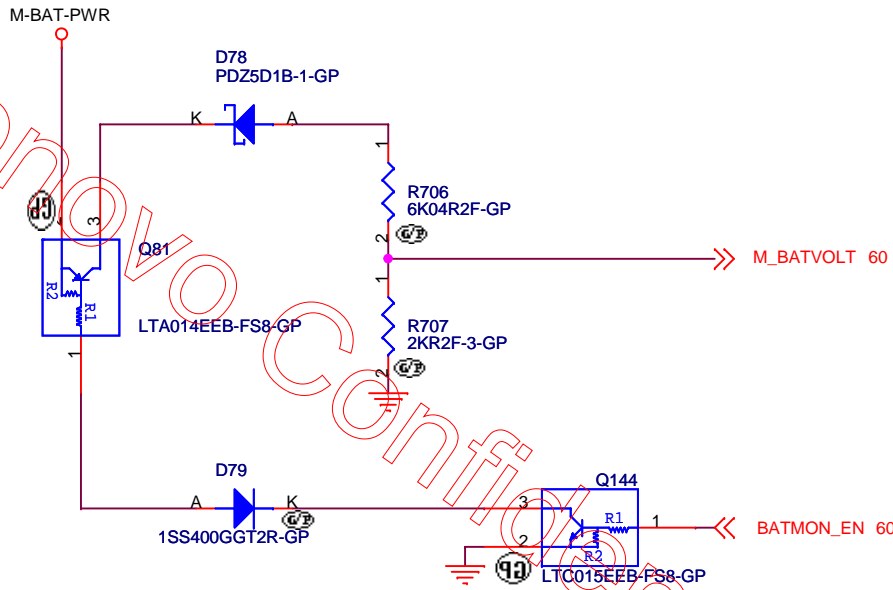
Genesis-1

Rev
SC

Date: Monday, January 30, 2012

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$$V_{OUT} = 0.249 (V_{BAT} - 5)$$



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Title

BATTERY MONITOR

Size
A4

Document Number

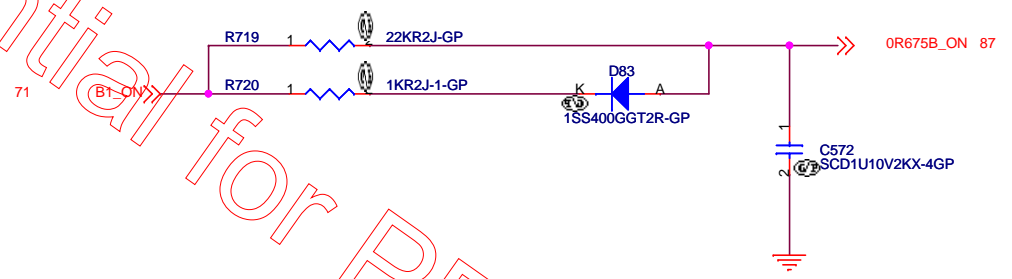
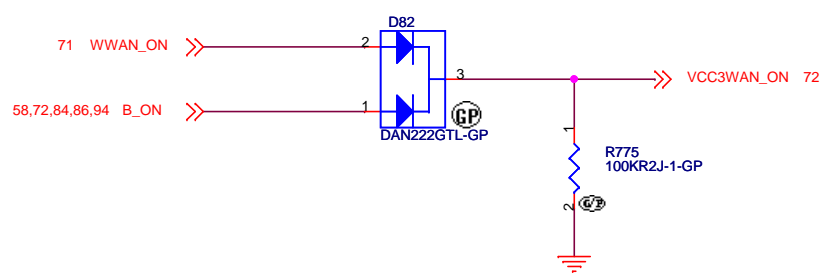
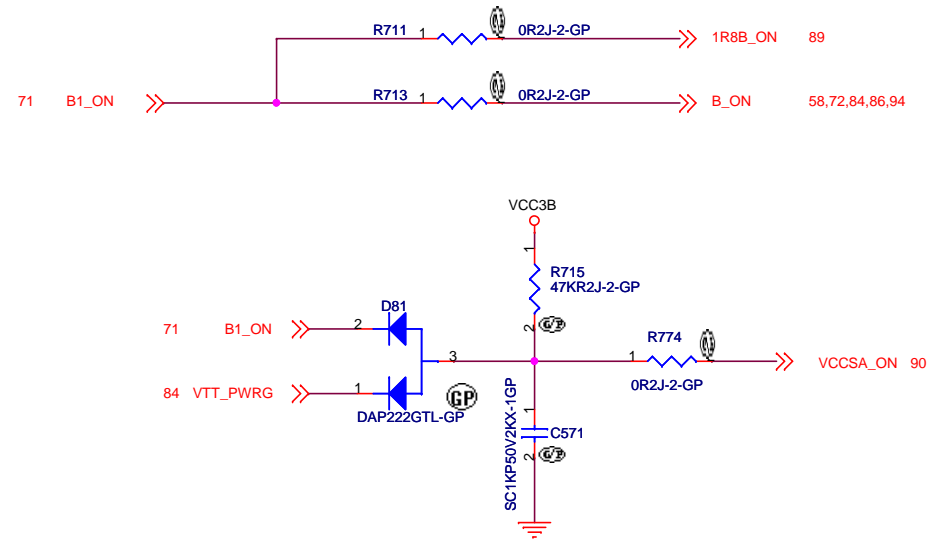
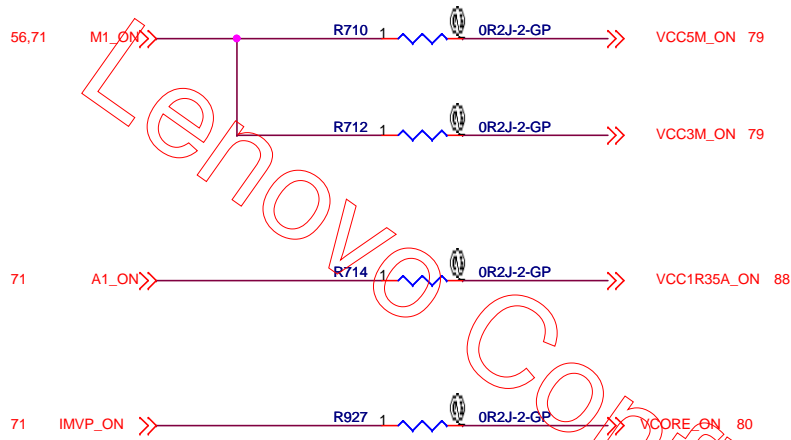
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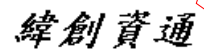
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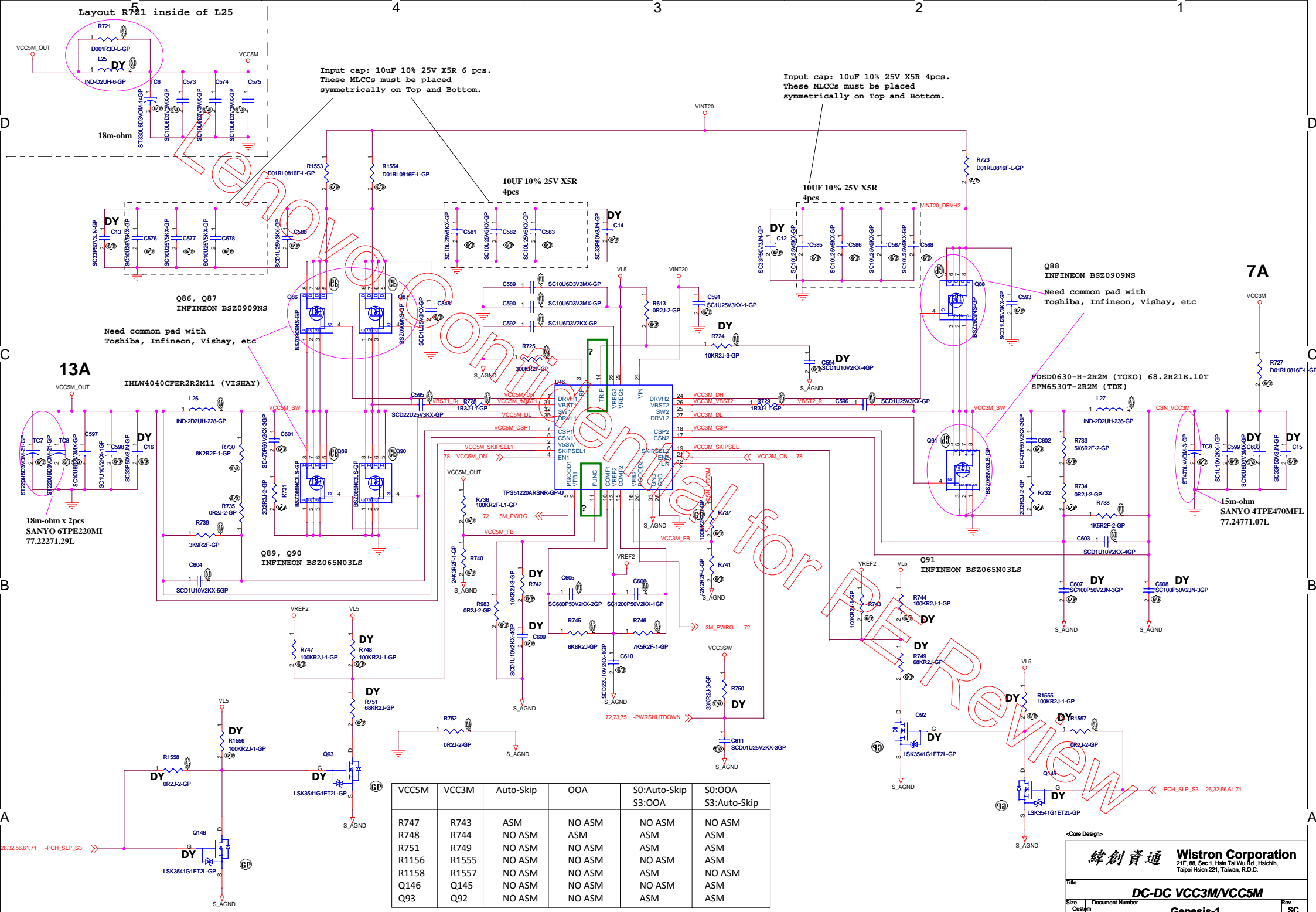


AOAC	YES	NO
D82	ASM	DY
R775	ASM	ASM
	100Kohm	0ohm

Logic

<Core Design>

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POWER SEQUENCE	
Genesis-1	
Title Size Custom	Document Number Rev SC
Date: Monday, January 30, 2012	Sheet 78 of 100



Input cap: 10uF 10% 25V X5R 6 pcs.
These MLCCs must be placed symmetrically on Top and Bottom.

Input cap: 10uF 10% 25V X5R 4pcs.
These MLCCs must be placed symmetrically on Top and Bottom.

Need common pad with
Toshiba, Infineon, Vishay, etc

Need common pad with
Toshiba, Infineon, Vishay, etc

18m-ohm x 2pcs
SANYO 6TPE220MI
77.22271.29L

15m-ohm
SANYO 4TPE470MFL
77.24771.07L

VCC5M	VCC3M	Auto-Skip	OOA	S0:Auto-Skip S3:OOA	S0:OOA S3:Auto-Skip
R747	R743	ASM	NO ASM	NO ASM	NO ASM
R748	R744	NO ASM	ASM	ASM	ASM
R751	R749	NO ASM	NO ASM	ASM	ASM
R1156	R1555	NO ASM	NO ASM	NO ASM	ASM
R1158	R1557	NO ASM	NO ASM	NO ASM	NO ASM
Q146	Q145	NO ASM	NO ASM	NO ASM	ASM
Q93	Q92	NO ASM	NO ASM	ASM	ASM

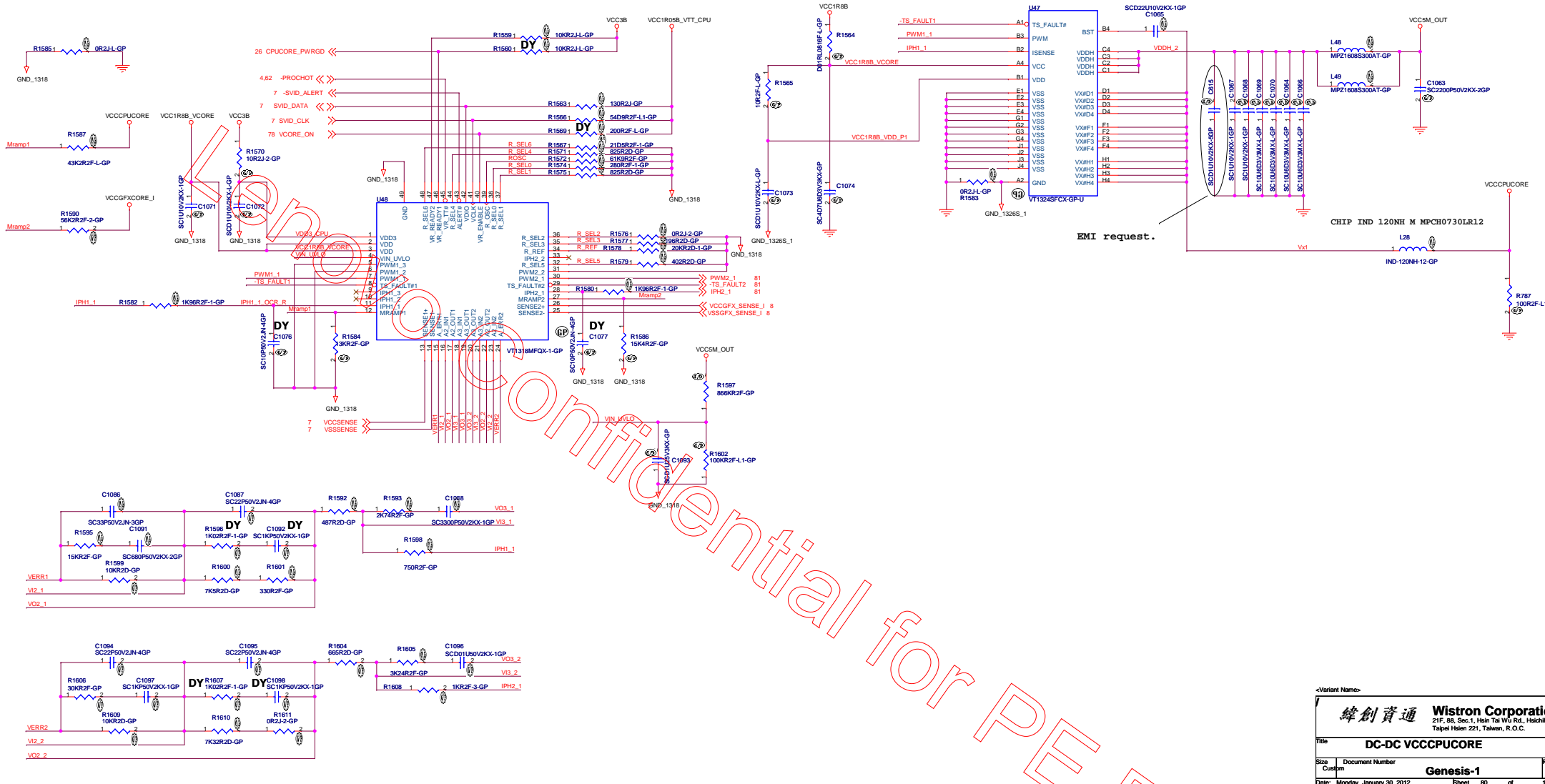
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緯創資通 Wistron Corporation
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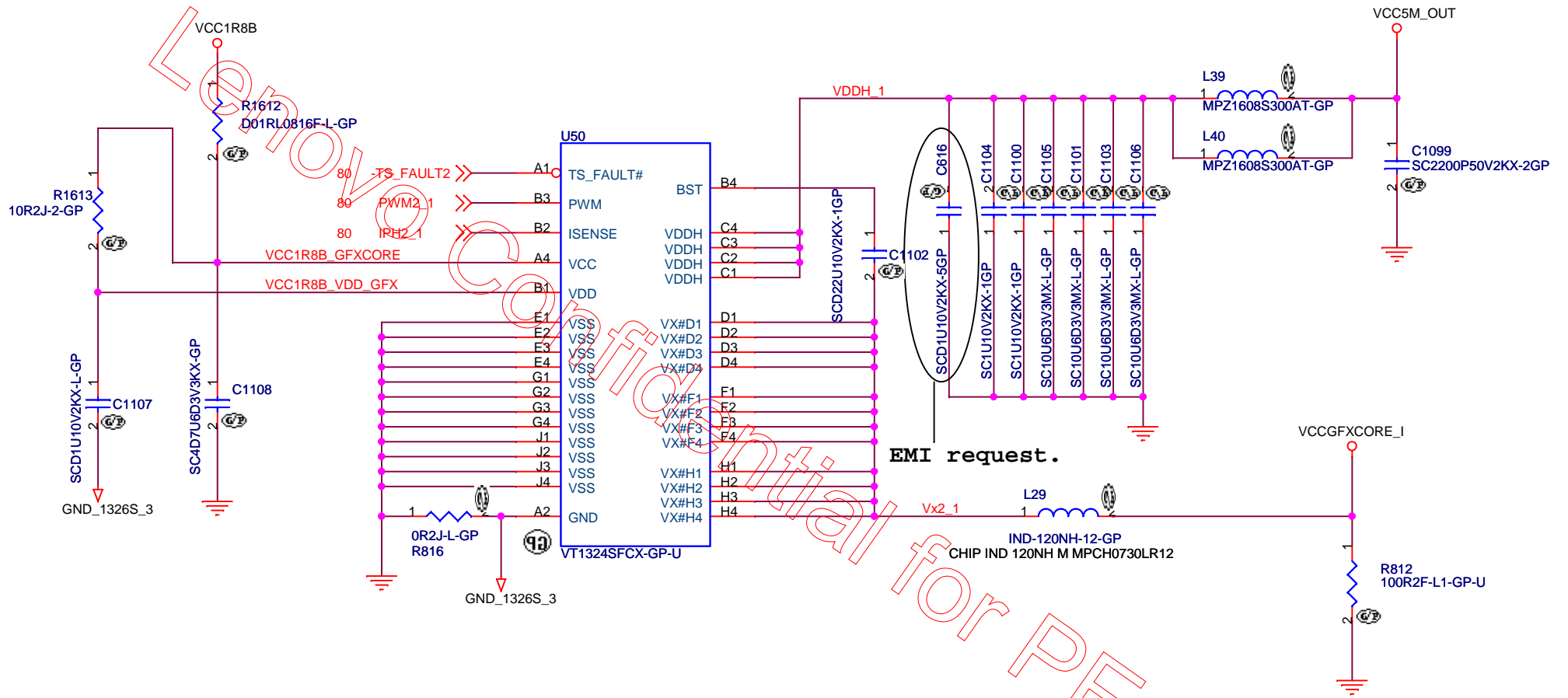
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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title: DC-DC VCCCPUCORE	
Size: Custom	Document Number: Genesis-1
Rev: SC	Rev: SC
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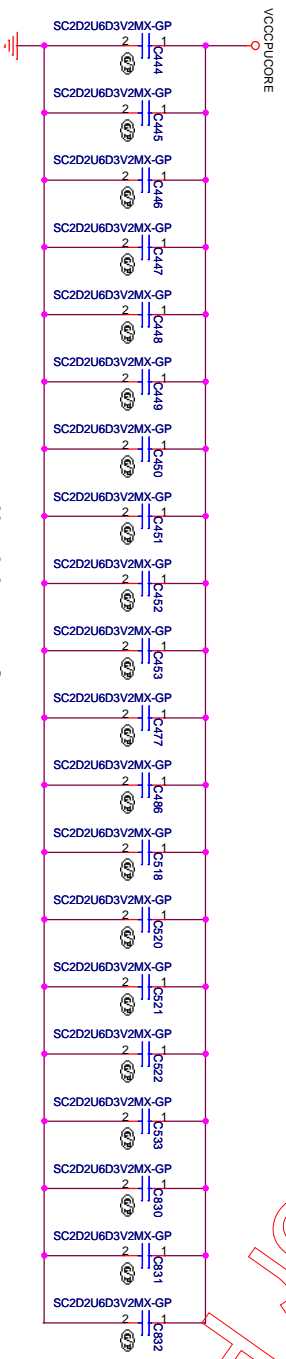
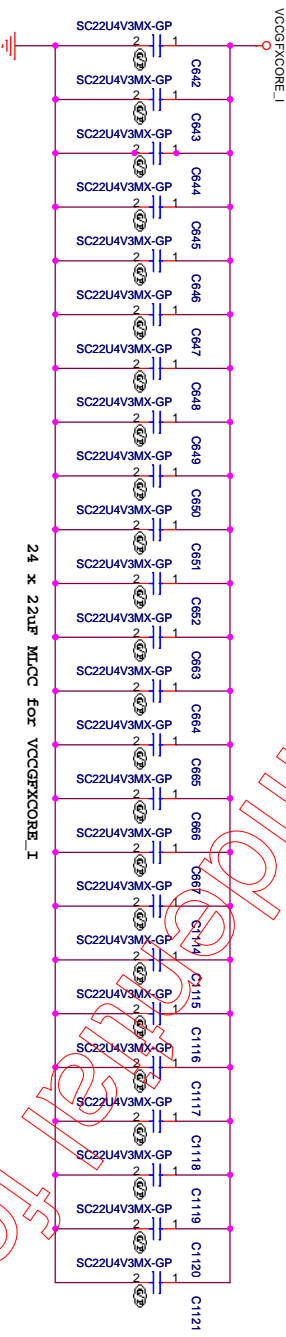
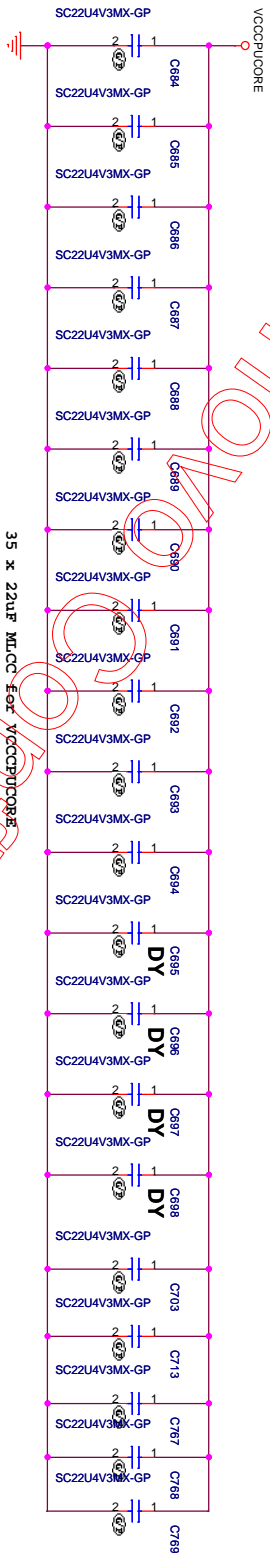
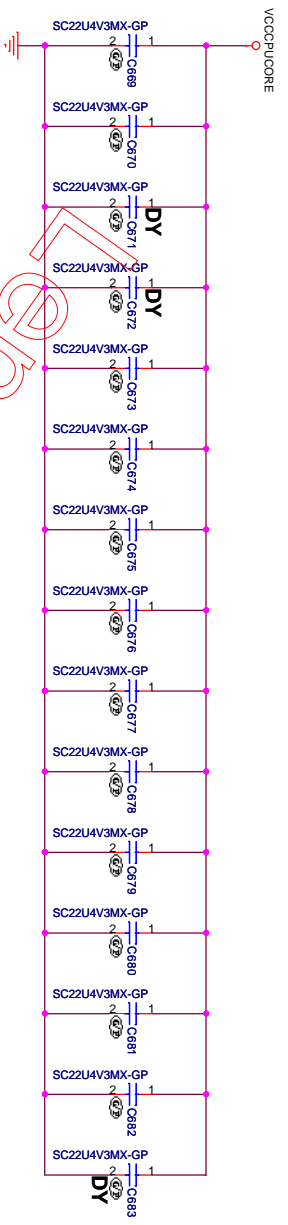
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 Taipei Hsien 221, Taiwan, R.O.C.

Title **VCCGFXCORE**

Size A4	Document Number Genesis-1	Rev SC
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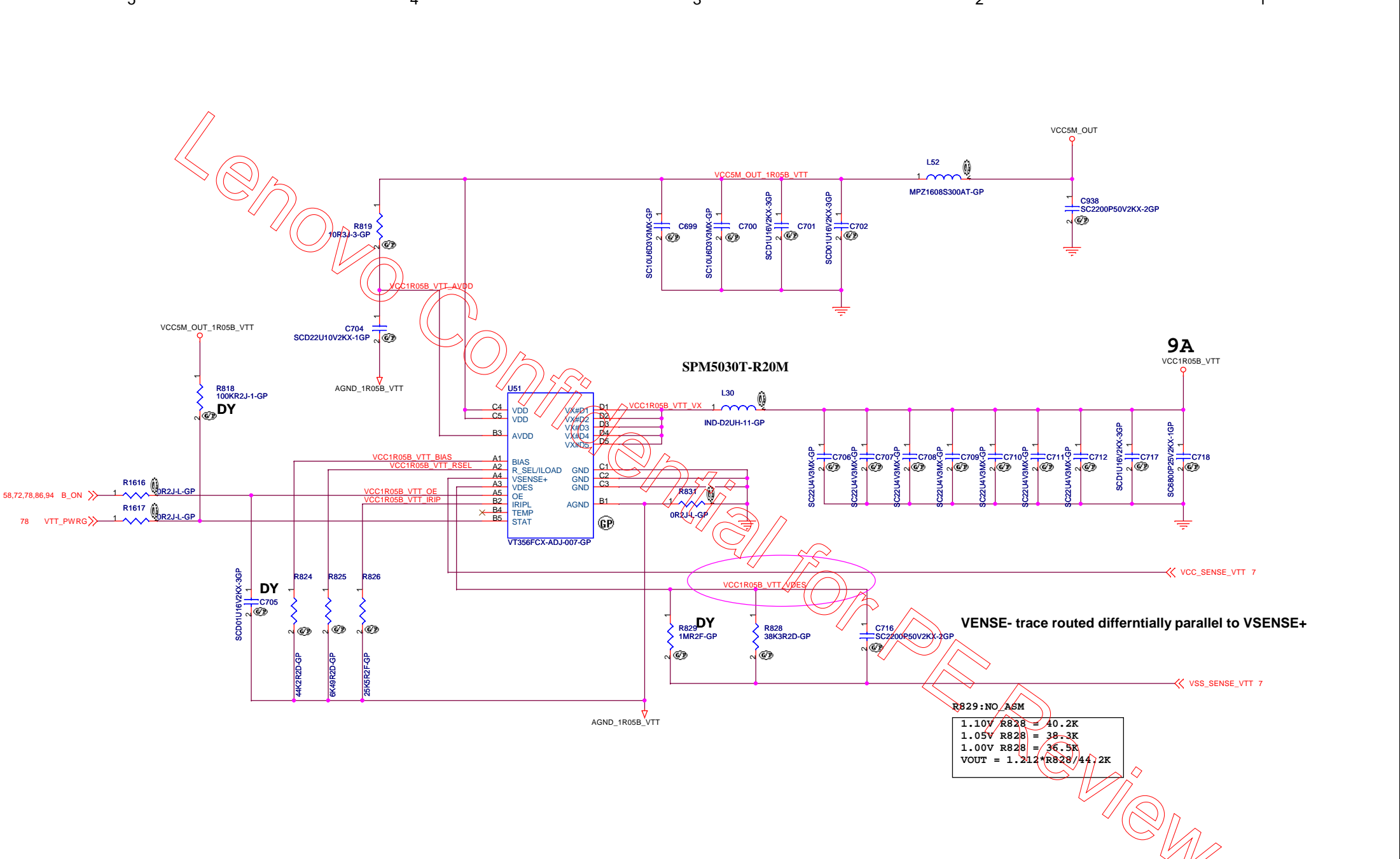
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Date		Monday, January 30, 2012	
Rev		SC	
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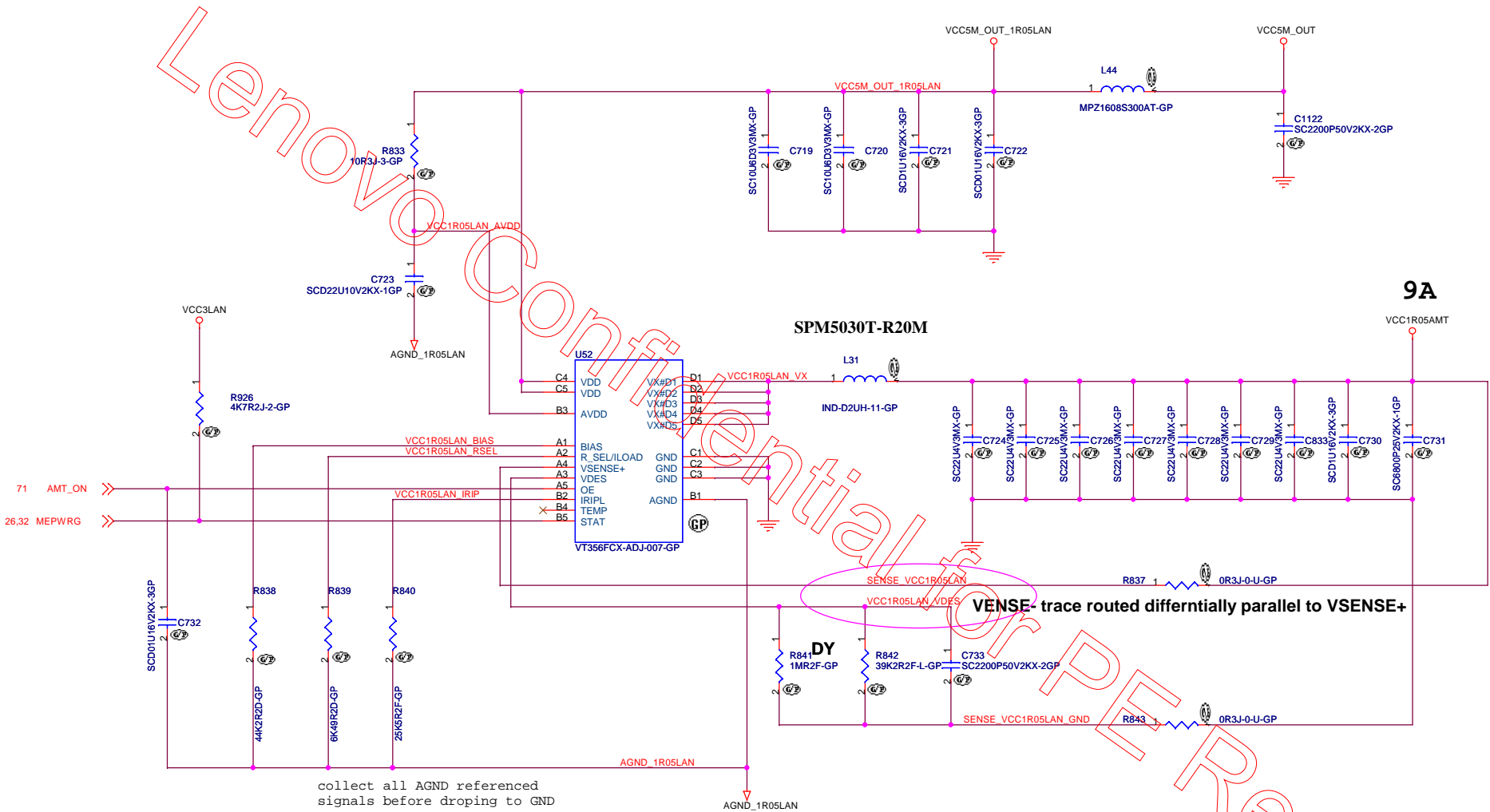
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R829: NO_ASM
 1.10V R828 = 40.2K
 1.05V R828 = 38.3K
 1.00V R828 = 36.5K
 $V_{OUT} = 1.212 * R828 / 44.2K$

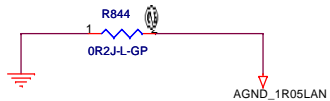
VENSE- trace routed differentially parallel to VSENSE+

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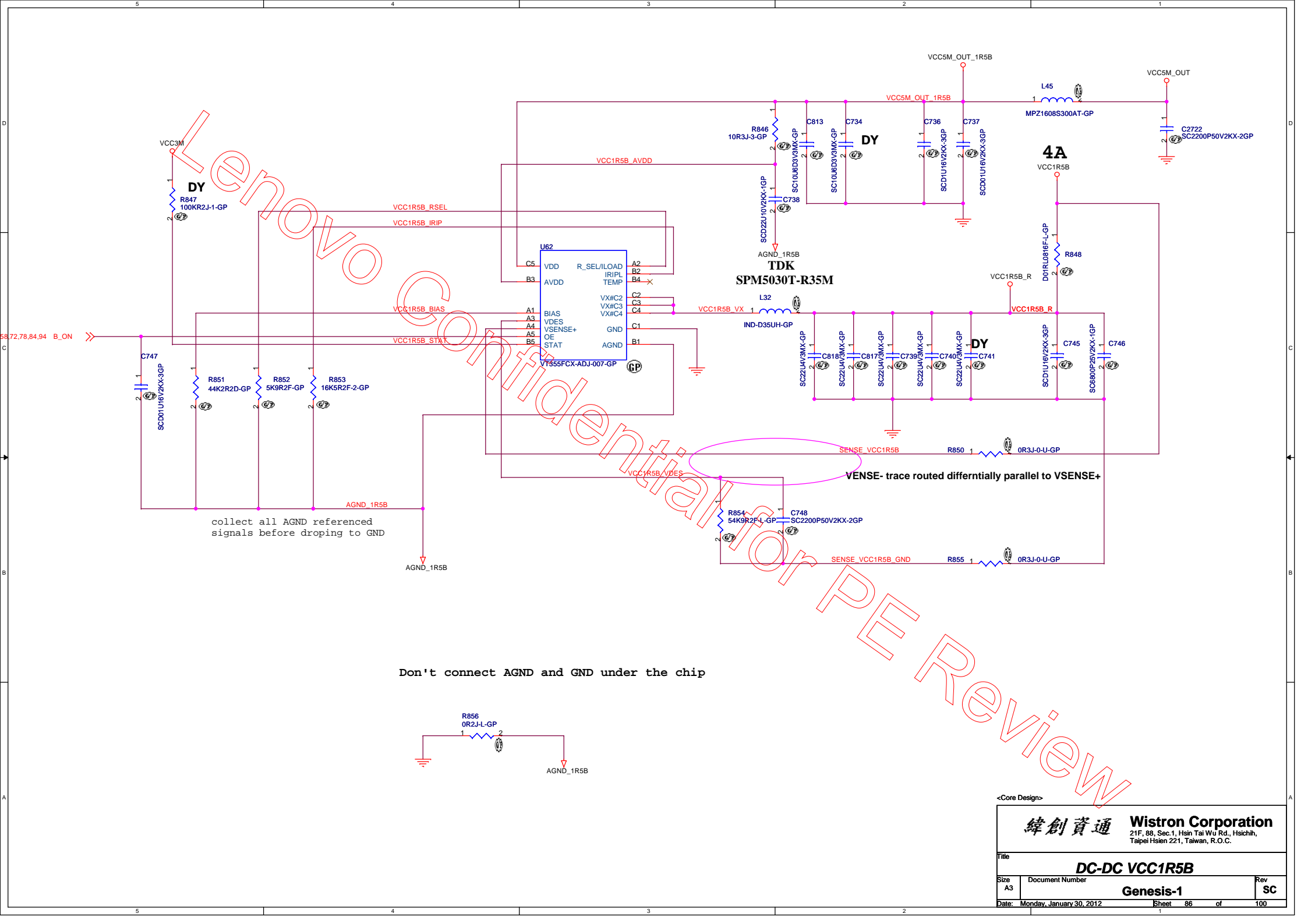
collect all AGND referenced signals before dropping to GND

Don't connect AGND and GND under the chip



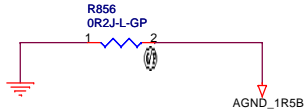
VENSE- trace routed differentially parallel to VSENSE+

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Title DC-DC VCC1R05AMT			
Size A3	Document Number Genesis-1		Rev SC
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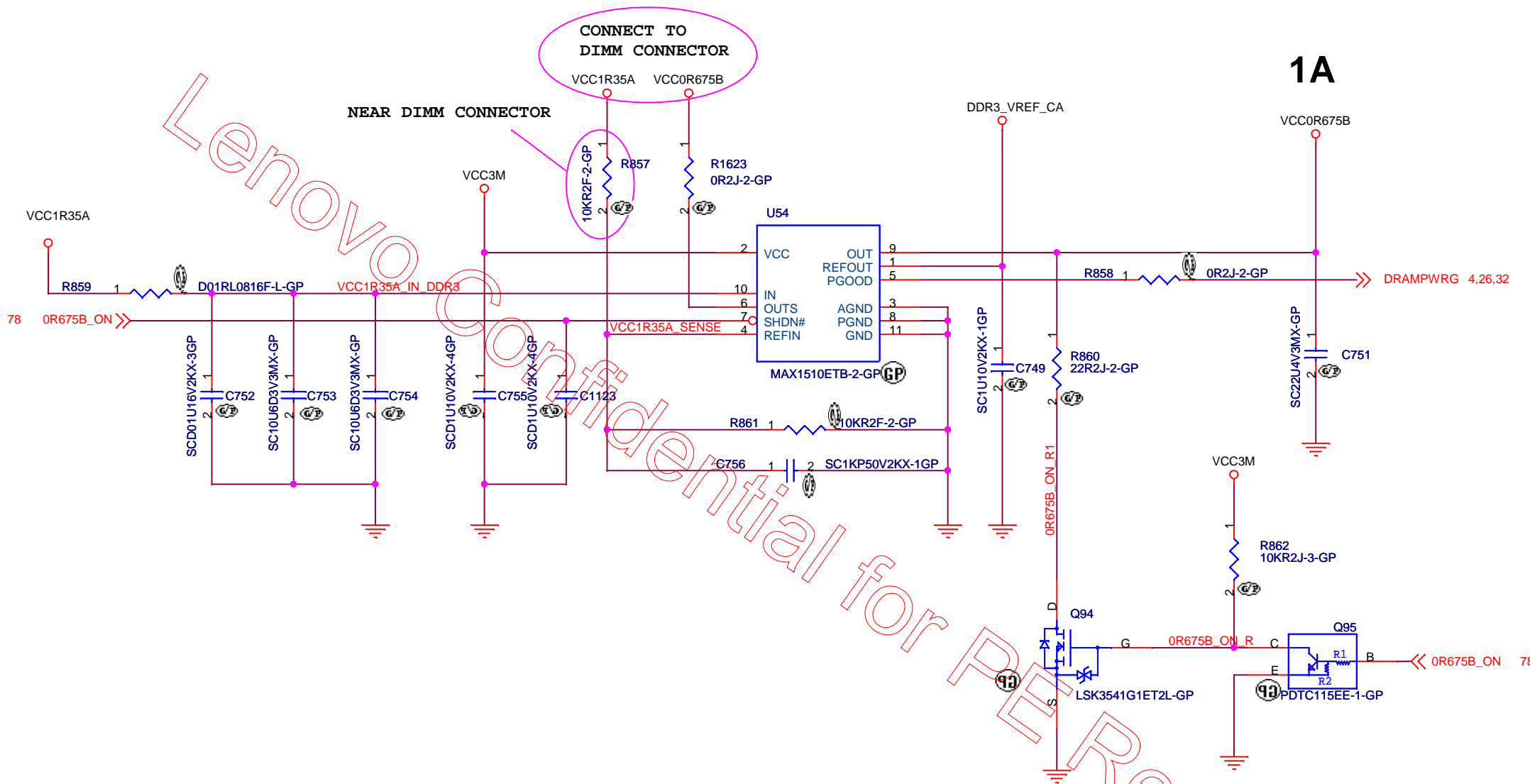


collect all AGND referenced signals before dropping to GND

Don't connect AGND and GND under the chip



VENSE- trace routed differentially parallel to VSENSE+



1A

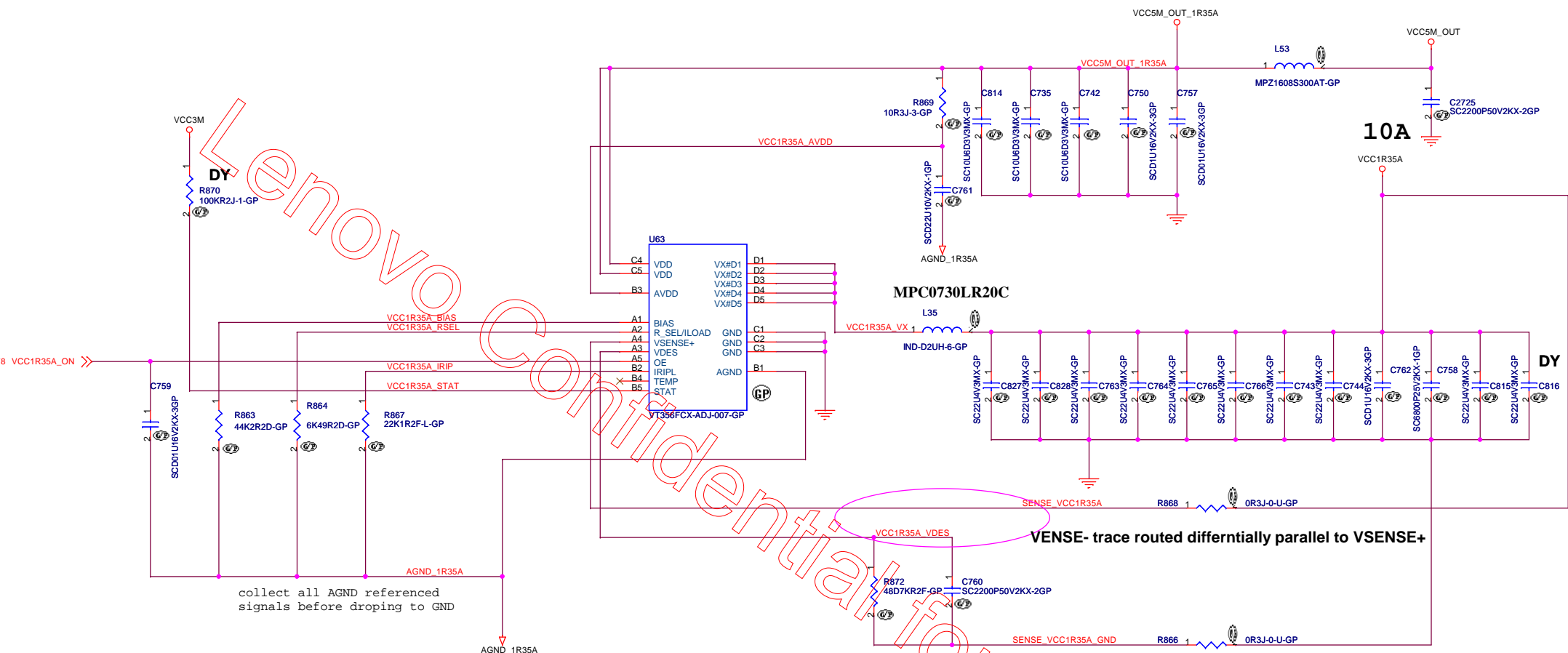
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緯創資通 **Wistron Corporation**
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 Taipei Hsien 221, Taiwan, R.O.C.

Title **DC-DC VCC0R675B**

Size A4	Document Number	Rev SC
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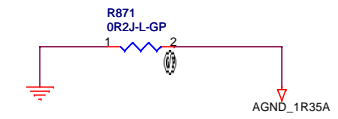
Genesis-1



collect all AGND referenced signals before dropping to GND

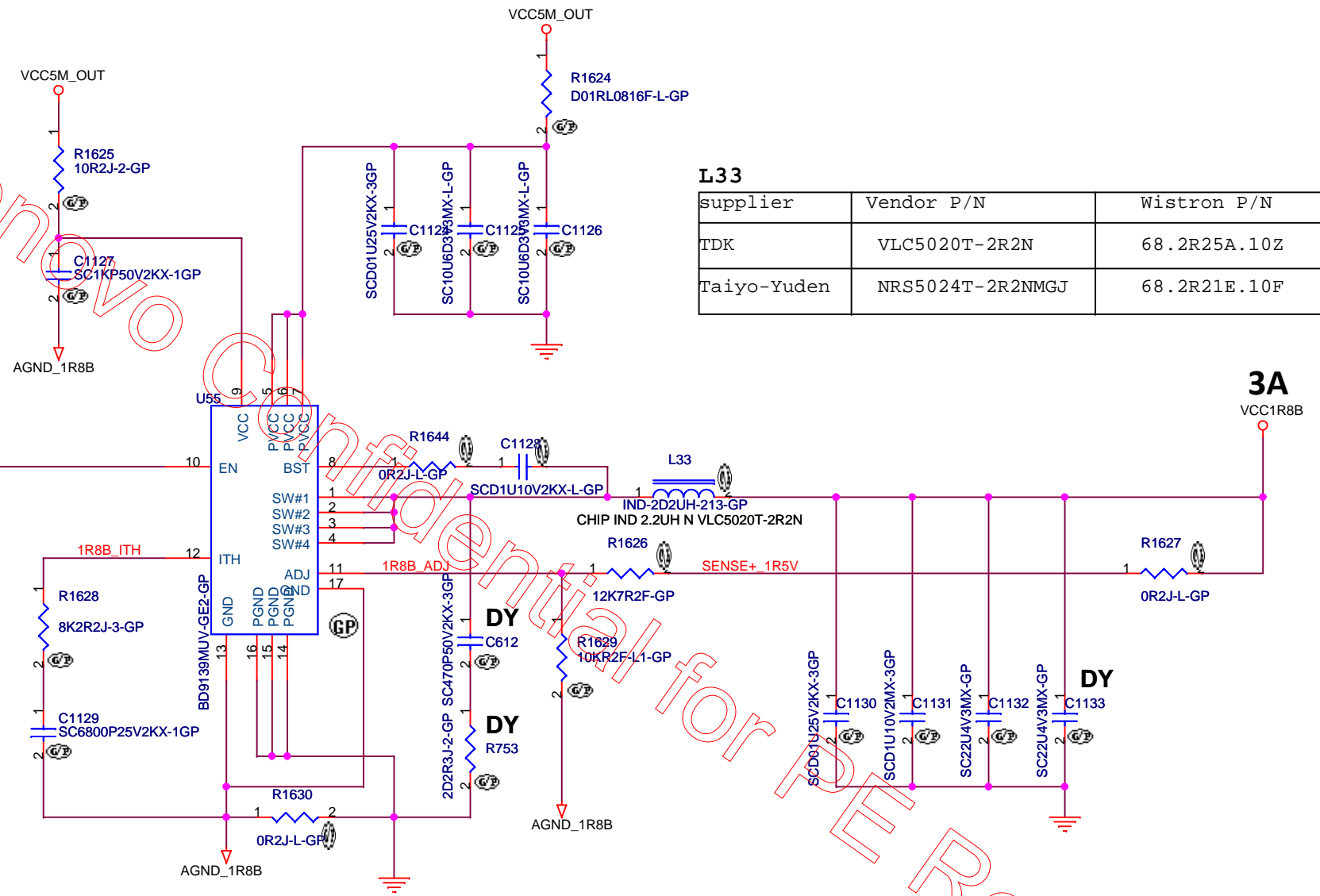
VENSE- trace routed differentially parallel to VSENSE+

Don't connect AGND and GND under the chip



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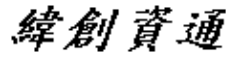
78 1R8B_ON



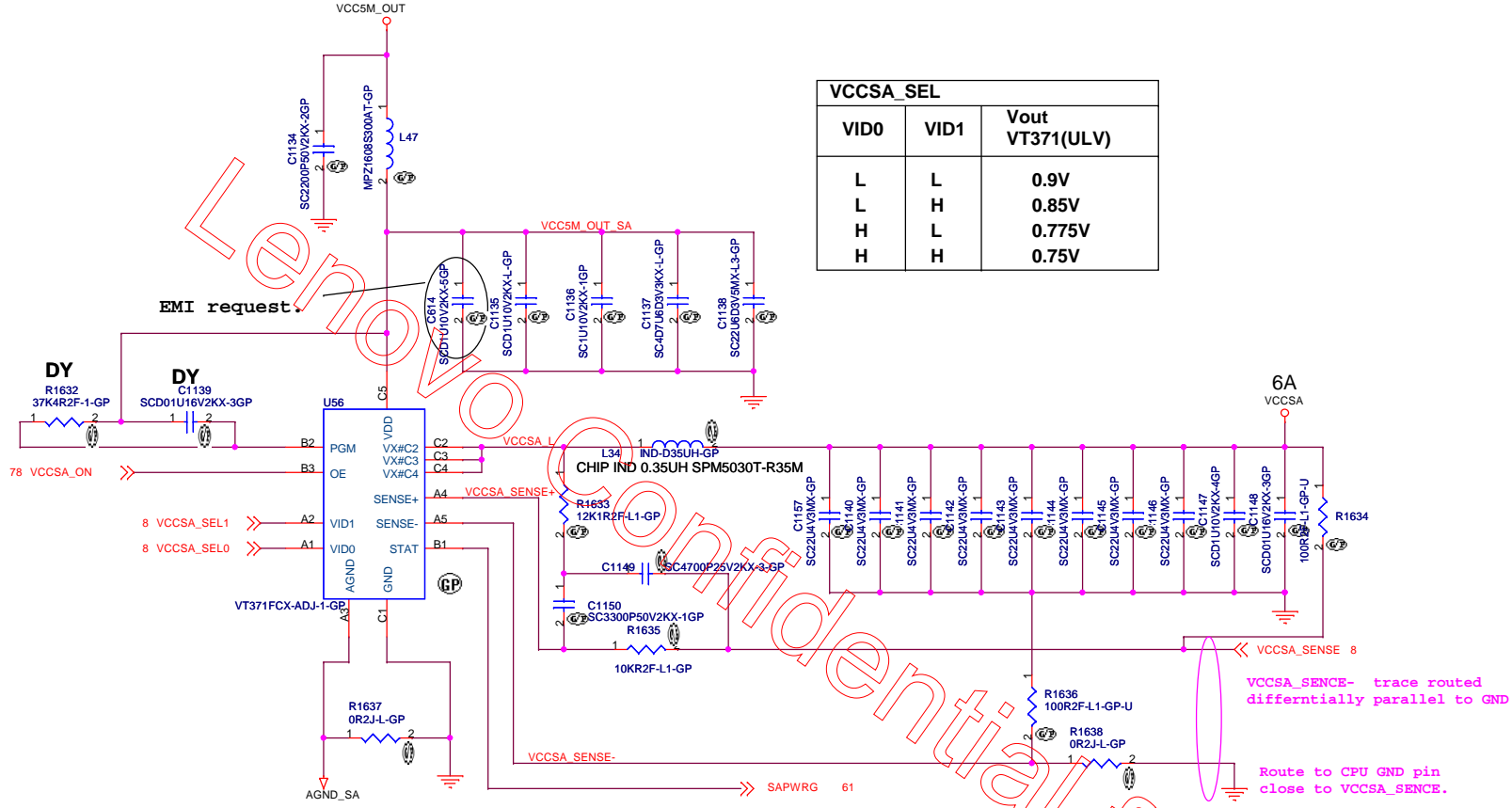
L33

supplier	Vendor P/N	Wistron P/N
TDK	VLC5020T-2R2N	68.2R25A.10Z
Taiyo-Yuden	NRS5024T-2R2NMGJ	68.2R21E.10F

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Title DC-DC VCC1R8B	Document Number Genesis-1
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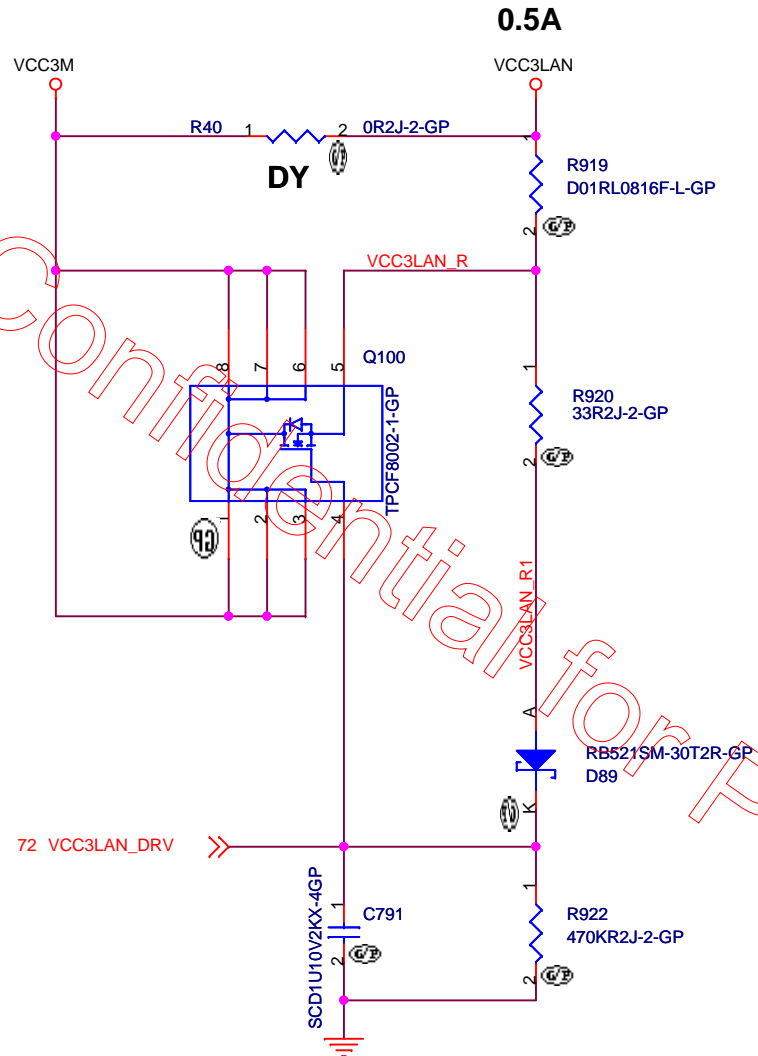
VCCSA_SEL		
VID0	VID1	Vout VT371(ULV)
L	L	0.9V
L	H	0.85V
H	L	0.775V
H	H	0.75V



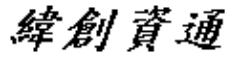
VCCSA_SENSE 8
 VCCSA_SENSE- trace routed differentially parallel to GND
 Route to CPU GND pin close to VCCSA_SENSE.

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Title **LOAD SW LAN**

Size A4	Document Number Genesis-1	Rev SC
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A4

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SC

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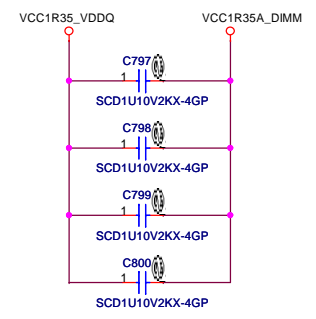
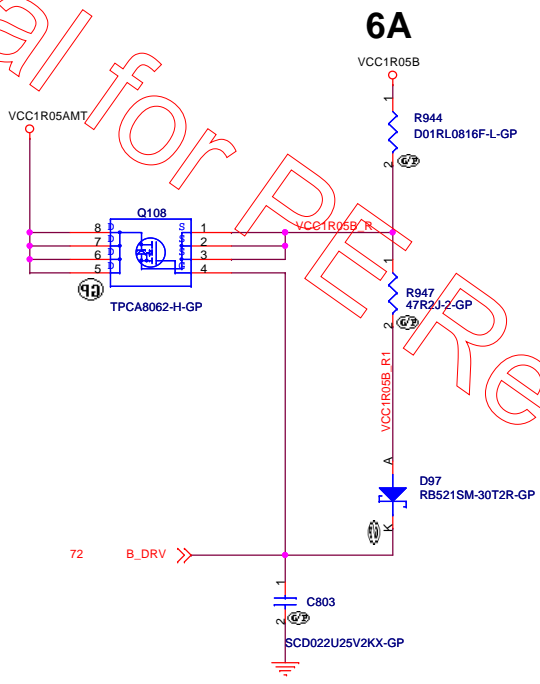
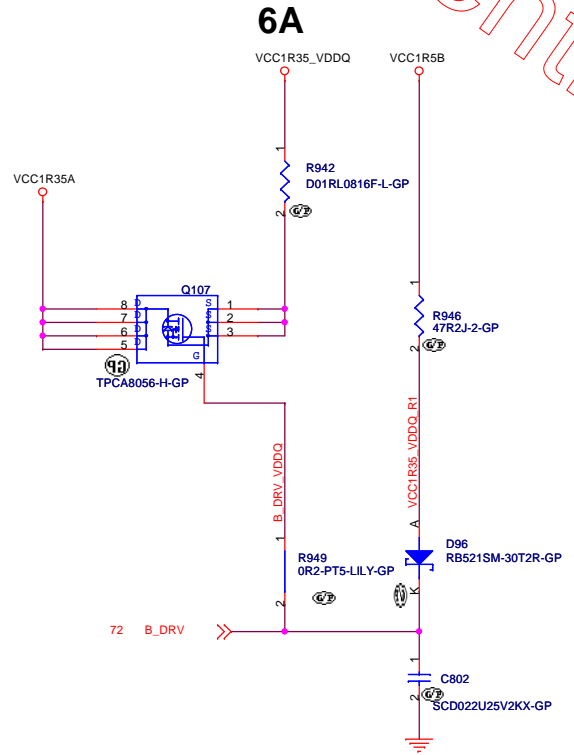
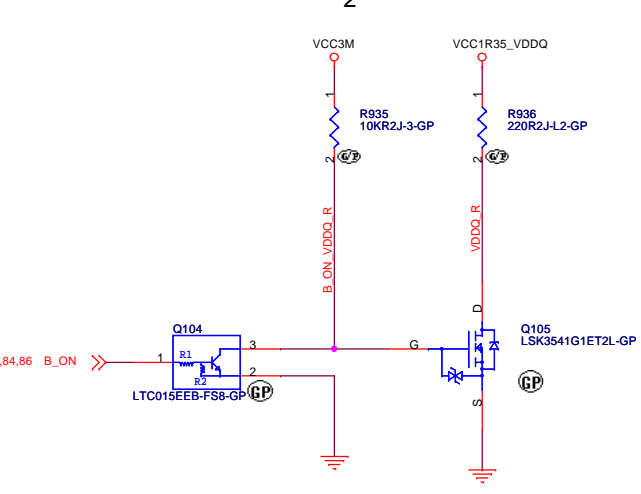
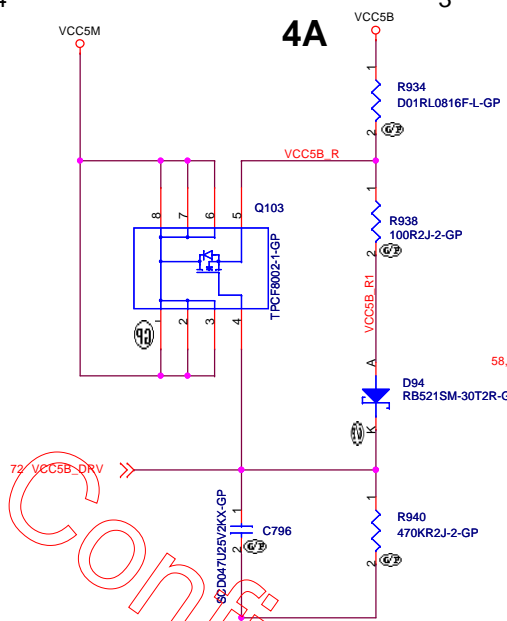
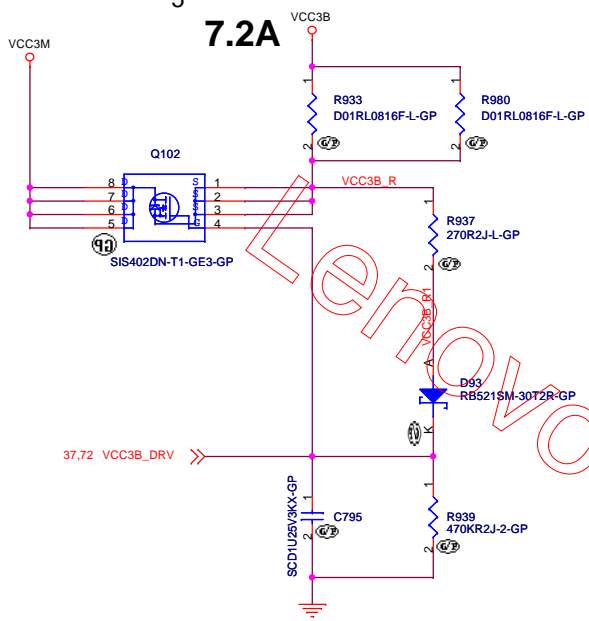
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Size A4	Document Number Genesis-1	Rev SC
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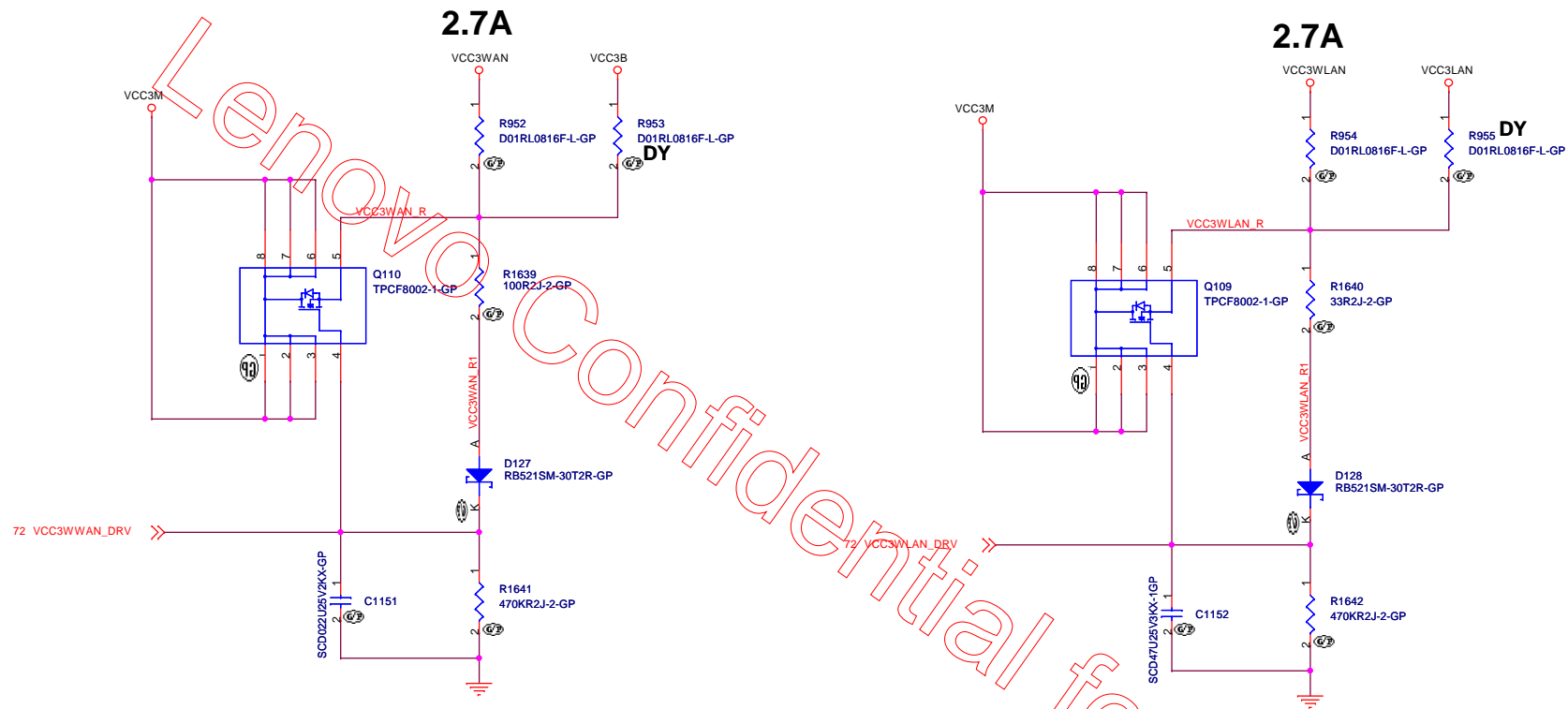
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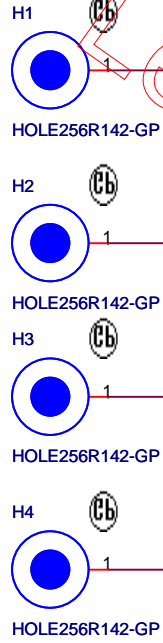
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R952	ASM	ASM
R953	DY	ASM
Q110	ASM	DY
R1639	ASM	DY
D127	ASM	DY
R1641	ASM	DY
C1151	ASM	DY

Logic

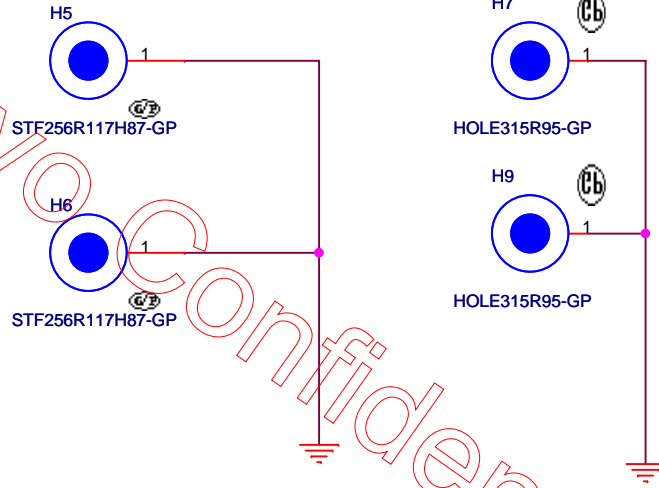
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LOAD SW WWAN & WLAN			
Title	Document Number		Rev
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A3			
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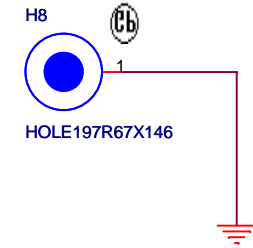
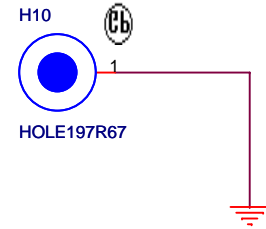
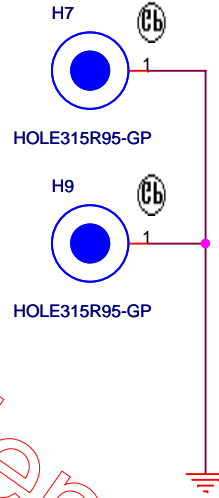
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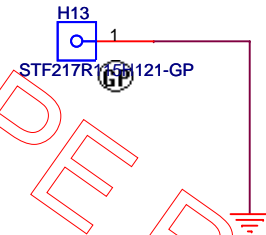
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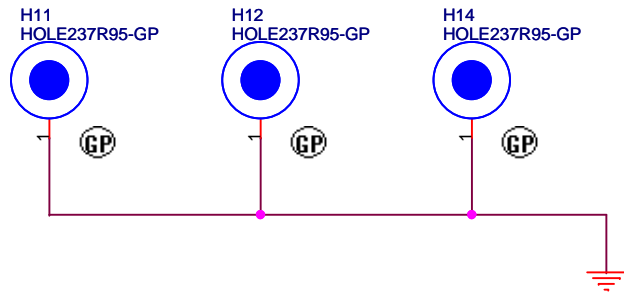
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34.4Y801.011



ZZ.00PAD.921



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Title
HOLES/GND/PADS

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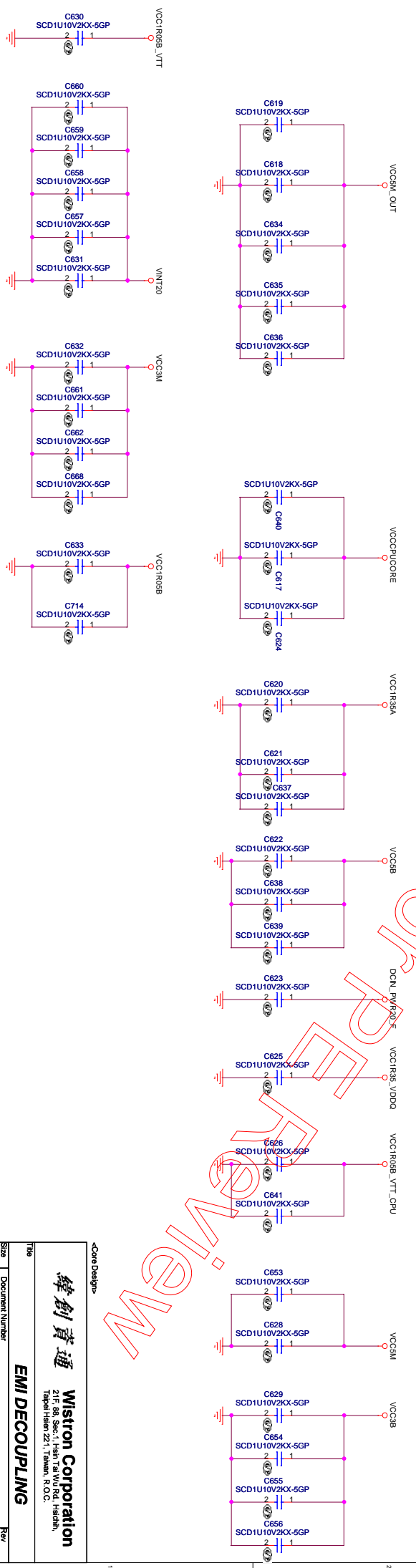
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Title		BLANK	
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RF decoupling caps

named as RFCxxxx

Long power trace EMI decoupling caps



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<Core Design>

緯創資通
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EMI DECOUPLING

Size	Document Number	Rev
Casepin		SC
Part#	Mandchuk-Ldman0V_30_2012	99 d 100

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Title

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Size
A3

Document Number

Genesis-1

Rev
SC

Date: Monday, January 30, 2012

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