User Manual

CG635
2.05 GHz Synthesized Clock Generator

Stanford Research Systems

Revision 1.3 (08/2010)

Certification

Stanford Research Systems certifies that this product met its published specifications at the time of shipment.

Warranty

This Stanford Research Systems product is warranted against defects in materials and workmanship for a period of one (1) year from the date of shipment.

Service

For warranty service or repair, this product must be returned to a Stanford Research Systems authorized service facility. Contact Stanford Research Systems or an authorized representative before returning this product for repair.

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Stanford Research Systems, Inc.
1290-C Reamwood Avenue
Sunnyvale, California 94089
Phone: (408) 744-9040
Fax: (408) 744-9049
www.thinkSRS.com

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Safety and Preparation for Use

Line Voltage

The CG635 operates from a 90 to 132 VAC or 175 to 264 VAC power source having a line frequency between 47 and 63 Hz. Power consumption is less than 80 VA total. In standby mode, power is turned off to the main board. However, power is maintained at all times to any optional timebases installed. Thus, a unit with an optional rubidium or ovenized quartz oscillator is expected to consume less than 25 VA and 15 VA of power, respectively, in standby mode.

Power Entry Module

A power entry module, labeled AC POWER on the back panel of the CG635, provides connection to the power source and to a protective ground.

Power Cord

The CG635 package includes a detachable, three-wire power cord for connection to the power source and protective ground.

The exposed metal parts of the box are connected to the power ground to protect against electrical shock. Always use an outlet which has a properly connected protective ground. Consult with an electrician if necessary.

Grounding

A chassis grounding lug is available on the back panel of the CG635. Connect a heavy duty ground wire, #12AWG or larger, from the chassis ground lug directly to a facility earth ground to provide additional protection against electrical shock.

BNC shields are connected to the chassis ground and the AC power source ground via the power cord. Do not apply any voltage to the shield.

Line Fuse

The line fuse is internal to the instrument and may not be serviced by the user.

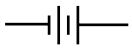
Operate Only with Covers in Place

To avoid personal injury, do not remove the product covers or panels. Do not operate the product without all covers and panels in place.

Serviceable Parts

The CG635 does not include any user serviceable parts inside. Refer service to a qualified technician.

Symbols you may Find on SRS Products

Symbol	Description
	Alternating current
	Caution - risk of electric shock
	Frame or chassis terminal
	Caution - refer to accompanying documents
	Earth (ground) terminal
	Battery
	Fuse
	On (supply)
	Off (supply)

Specifications

Frequency

Range	1 µHz to 2.05 GHz
Resolution	
f < 10 kHz	1 pHz
f ≥ 10 kHz	16 digits
Accuracy	$\Delta f < \pm (2\times10^{-19} + \text{timebase error}) \times f$
Settling time	<30 ms

Timebase (+20 °C to +30 °C ambient)

Stability	
Std. timebase	<5 ppm
Opt. 02 (OCXO)	<0.01 ppm
Opt. 03 (Rb)	<0.0001 ppm
Aging	
Std. timebase	<5 ppm/year
Opt. 02 (OCXO)	<0.2 ppm/year
Opt. 03 (Rb)	<0.0005 ppm/year
External Input	10 MHz ± 10 ppm, sine >0.5 V_{pp}, 1 kΩ impedance
Output	10 MHz, 1.41 V_{pp} sine (+7 dBm) into 50 Ω

Noise & Spurs

Phase noise (at 622.08 MHz)	
100 Hz offset	<–90 dBc/Hz
1 kHz offset	<–100 dBc/Hz
10 kHz offset	<–100 dBc/Hz
100 kHz offset	<–110 dBc/Hz
Phase noise vs. freq.	6 dB/oct. relative to 622.08 MHz
Spurious	<–70 dBc (within 50 kHz of carrier)

Jitter and Wander

Jitter (rms)	<1 ps (1 kHz to 5 MHz bandwidth)
Wander (p-p)	<20 ps (10 s persistence)

Time Modulation

Rear-panel input	BNC, DC coupled, 1 kΩ
Sensitivity	1 ns/V, ±5 %
Range	±5 ns
Bandwidth	DC to greater than 10 kHz

Phase

Range	±720°
Resolution	<20 ps
Maximum step size	±360°
Slew time (Δp > 0°)	<300 ms

Q and $\overline{Q}$ Outputs

Outputs	Front-panel BNC connectors
Frequency range	DC to 2.05 GHz
High level	$-2.00\ V \leq V_{HIGH} \leq +5.00\ V$
Amplitude	$200\ mV \leq V_{AMPL} \leq 1.00\ V$ ($V_{AMPL} \equiv V_{HIGH} - V_{LOW}$)
Level resolution	10 mV
Level error	<1 % + 10 mV
Transition time	<100 ps (20 % to 80 %)
Symmetry	<100 ps departure from nominal 50 %
Source impedance	50 Ω (±1 %)
Load impedance	50 Ω to ground on both outputs
Pre-programmed levels	+5.0 V PECL, +3.3 V PECL, LVDS, +7 dBm, ECL
Protection	Continuous to ground, momentary to $+5\ V_{DC}$

CMOS Output

Output	Front-panel BNC
Frequency range	DC to 250 MHz
Low level	$-1.00\ V \leq V_{LOW} \leq +1.00\ V$
Amplitude range	$500\ mV \leq V_{AMPL} \leq 6.00\ V$ ($V_{AMPL} \equiv V_{HIGH} - V_{LOW}$)
Level resolution	10 mV
Level error	<2 % of V_{AMPL} + 20 mV
Transition time	<1.0 ns (10 % to 90 %, with 12pF load at far end of 50 Ω cable)
Symmetry	<500 ps departure from nominal 50%
Source impedance	50 Ω (reverse terminates cable reflection)
Load impedance	Unterminated 50 Ω cable of any length
Attenuation (50 Ω load)	Output levels are divided by 2
Preprogrammed levels	$V_{LOW} = 0$; $V_{HIGH} = 1.2$, 1.8, 2.5, 3.3, or 5.0 V
Protection	Continuous to ground, momentary to $+5\ V_{DC}$

RS-485 Output

Output	Rear-panel RJ-45
Frequency range	DC to 105 MHz
Clock output	Pin 7 and pin 8 drive twisted pair
Transition time	<800 ps (20% to 80%)
Source impedance	100 Ω between pin 7 and pin 8
Load impedances	100 Ω between pin 7 and pin 8
Logic levels	$V_{LOW} = +0.9$ V, $V_{HIGH} = +2.2$ V
Recommended cable	Straight-through Category-6
Protection	Continuous to ground, momentary to $+5\ V_{DC}$

LVDS Output (EIA/TIA-644)

Output	Rear-panel RJ-45
Frequency range	DC to 2.05 GHz
Clock output	Pin 1 and pin 2 drive twisted pair
Transition time	<100 ps (20% to 80%)
Source impedance	100 Ω between pin 1 and pin 2
Load impedances	100 Ω between pin 1 and pin 2
Logic levels	V_{LOW} = +0.96 V, V_{HIGH} = +1.34 V
Recommended cable	Straight-through Category-6
Protection	Continuous to ground, momentary to +5 V

PRBS (Opt. 01) (EIA/TIA-644)

Frequency range	DC to 1.55 GHz
Level	LVDS on rear-panel SMA jacks
Outputs	PRBS, –PRBS, CLK & –CLK
PRBS generator	$x^7 + x^6 + 1$ for a length of $2^7 – 1$ bits
Transition time	<100 ps (20 % to 80 %)
Load impedance	50 Ω to ground on all outputs

Accessory Power (on rear-panel RJ-45 connector)

+5 VDC	Pin 3
–5 VDC	Pin 5
Ground return	Pin 4 and pin 6
Short circuit protection	Current limited to 375 mA
Polarity clamps	Diode clamps prevent polarity inversion (2 ADC max., 120 A non-rep.)

General

Computer interfaces	IEEE-488.2 and RS-232 standard. All instrument functions can be controlled through the computer interfaces.
Non-volatile memory	Ten sets of instrument configurations can be stored and recalled.
Line power	Universal input, 90 to 264 VAC, 47 Hz to 63 Hz
Standby power	<5 W (std. timebase) <15 W (opt. 02, OCXO timebase) <25 W (opt. 03, Rb timebase)
Operating power	<30 W (std. timebase) <40 W (opt. 02, OCXO timebase) <50 W (opt. 03, Rb timebase)
Dimensions	8.5” × 3.5” × 13” (WHD)
Weight	<9 lbs.
Warranty	One year parts and labor on defects in materials and workmanship

Optional Receiver Modules

General

Inputs	RJ-45. Connects to CG635 via standard Category-6 cable.
Outputs	Q / $\overline{Q}$ on SMA connectors
Dimensions	1 5/8" × 1" × 3" (WHD)

Models

Model	Levels	Source Impedance	Termination Impedance	Transition Time (max)	F_{max} (2)
CG640	+5 V CMOS	50 Ω	High Z	2.0 ns	105 MHz(1)
CG641	+3.3 V CMOS	50 Ω	High Z	800 ps	250 MHz
CG642	+2.5 V CMOS	50 Ω	High Z	800 ps	250 MHz
CG643	+5 V PECL	50 Ω	High Z	800 ps	250 MHz
CG644	+3.3 V PECL	50 Ω	50 Ω	100 ps	2.05 GHz
CG645	+2.5 V PECL	50 Ω	50 Ω	100 ps	2.05 GHz
CG646	+7 dBm RF	50 Ω	50 Ω	100 ps	2.05 GHz
CG647	CML/NIM	50 Ω	50 Ω	100 ps	2.05 GHz
CG648	NEG ECL	50 Ω	50 Ω	100 ps	2.05 GHz
CG649	LVDS	50 Ω	50 Ω	100 ps	2.05 GHz

Notes: (1) Output is set to logic '0' above F_{max}.

(2) Except for the CG640, all outputs continue to operate above F_{max} with reduced amplitude. Maximum operating frequency is also limited by the CAT-6 cable length. At 2 GHz, cable lengths up to 10 feet may be used. At 10 MHz, cable lengths of up to 200 feet may be used. See Figure 3 on page 11 for the maximum recommended cable lengths at other frequencies.

Quick Start Instructions

Step by Step Example

1. With the power button in the Standby position, connect the CG635 to a grounded outlet using the power cord provided.

2. Push in the power button to turn on the CG635. The CG635 will perform some start up tests and then recall the instruments' last known settings from non volatile memory.

3. Reset the CG635 to its default state by pressing sequentially the following 3 keys located in the ENTRY section of the front panel: 'SHIFT', '+/-', 'Hz'. This performs the INIT function which resets the instrument to its default settings.

   The INIT function will set the frequency to 10 MHz, set the phase to 0 degrees, set the output levels for Q and $\overline{Q}$ to LVDS, set the output levels for CMOS to 3.3 V, and select the frequency for display. The LVDS and +3.3 V LEDs in the OUTPUT LEVELS section of the front panel should be on. The FREQ LED in the DISPLAY section should be on. The seven segment display should show 10.000000000 and the MHz LED should be lit. This indicates that the frequency is 10 MHz.

4. Connect the CMOS output to an oscilloscope with a high impedance input to see that the output is indeed a 3.3 V square wave with a frequency of 10 MHz.

5. Adjust the frequency to 5 MHz by pressing the following keys sequentially: '5', 'MHz'. The display should change to 5.000000000 MHz. The oscilloscope should now display a 5 MHz square wave with amplitude 3.3 V.

6. Adjust the CMOS output up to 5.0 V by pressing the CMOS ▲ key in the OUTPUT LEVELS section of the front panel. The +3.3 V LED should turn off and the +5.0 V LED should turn on. The oscilloscope should now display a 5 MHz square wave with amplitude 5.0 V.

7. Press the 'CMOS HIGH' key in the DISPLAY section of the front panel. The CMOS HIGH LED should turn on and the seven segment display should show 5.00 VDC.

8. Adjust the CMOS output to 4.5 V by pressing the following keys sequentially in the ENTRY section of the front panel: '4', '.', '5', 'VOLT'. The seven segment display should now show 4.50 VDC. In the OUTPUT LEVELS section, the +5.0 V and VAR LEDs should be lit. This indicates that the current CMOS output voltage varies from, but is closest to the +5.0 V standard output level.

9. Press the CMOS ▼ key in the OUTPUT LEVELS section of the front panel. The CMOS output changes to the nearest standard level in the direction of the indicated key, which is 3.3 V in this case. The VAR LED should turn off, indicating that the current output is at a standard level.

10. Press the ‘FREQ’ key in the DISPLAY section to display the current frequency. The seven segment display should show 5.000000000 MHz.

11. Press the ‘STEP SIZE’ key in the MODIFY section of the front panel. The display should now show 1.000 Hz, and the STEP LED should be lit. This indicates that the current step size for frequency is 1.000 Hz.

12. Change the frequency step size to 1 kHz by pressing the following keys sequentially in the ENTRY section of the front panel: ‘1’, ‘kHz’. The display should now show 1.000000 kHz.

13. Switch back to the frequency display be pressing the ‘STEP SIZE’ key again. The STEP LED should turn off, and the display should show the current frequency of 5.000000000 MHz. The digit corresponding to 1 kHz should be blinking, indicating that frequency steps will change that digit by one.

14. Step the frequency up by 1 kHz by pressing the MODIFY ▲ key. The frequency should now display 5.001000000 MHz.

15. For more details about the operation of keys on the front panel, see the Front Panel Overview (page 2) in the Introduction.

16. For more details about a particular feature, see the chapter Operation (page 13).

Introduction

Feature Overview

The CG635 Synthesized Clock Generator provides precise, low-jitter digital clock signals for applications ranging from the development of digital circuits to the testing of communications networks.

The CG635 generates single ended and differential clocks from 1 µHz to 2.05 GHz with sub-picosecond jitter. Clock frequencies may be set with up to 1 pHz resolution and 16 significant digits. Front-panel outputs have continuously adjustable offsets and amplitudes, and may be set to standard logic levels including CMOS, PECL, ECL, and LVDS. A rear-panel output delivers clocks at RS-485 and LVDS over twisted pairs.

Several instrument features support more complex tasks. The phase of the outputs may be adjusted with nanodegree resolution at 2 Hz, and one-degree resolution at 2 GHz. The timing of clock edges may be modulated over ±5 ns by an external analog signal. An optional pseudo-random binary sequence (PRBS) generator (Opt. 01) provides clock and data outputs at LVDS levels for eye-pattern testing of serial data channels. Edge transition times are typically 80 ps.

The standard crystal oscillator timebase of the CG635 provides sufficient accuracy for many applications. An optional ovenized crystal oscillator (Opt. 02), or rubidium frequency standard (Opt. 03), may be added to improve frequency stability and reduce aging. The CG635 may also be locked to an external 10 MHz timebase.

The CG635 delivers a low spurious output signal—better than most commercial synthesizers. Phase noise for a 622.08 MHz carrier at 100 Hz offset is less than –80 dBc/Hz, and the spurious response is better than –70 dBc.

All instrument functions may be controlled from the front panel or via the GPIB (IEEE-488.2) or RS-232 interfaces. Up to ten complete instrument configurations can be stored in non-volatile memory and recalled at any time. A universal input AC power supply allows world-wide operation.

Several clock receiver modules are available which may be connected to the rear-panel RS-485/LVDS output via Category-6 cable. These accessories provide complementary high-speed transitions at standard logic levels on SMA connectors, and may be located at a substantial distance from the instrument. CMOS (+5 V, +3.3 V, and +2.5 V), PECL (+5 V, +3.3 V and +2.5 V), RF (+7 dBm), CML/NIM, ECL, and LVDS outputs are all available.

Front-Panel Overview

The front panel was designed to provide a simple, intuitive, user interface to all the CG635 features (see Figure 1). The power switch is located in the lower right corner of the front panel. Pushing the switch enables power to the instrument. Pushing the switch again places the instrument in stand-by mode, where power is enabled only to optionally installed timebases. Power to the main board is turned off in stand-by mode.

The front panel provides three output drivers for connecting the CG635 clock signals to user applications via standard BNC cables. The two upper outputs are complementary, high-speed, ECL compatible output drivers. The lower output is a CMOS output driver.

Keys on the front panel are divided into four sections to indicate their overall functionality: OUTPUT LEVELS, DISPLAY, ENTRY, and MODIFY. Keys in the OUTPUT LEVELS section modify the amplitude and offset of the clock signals provided by the front panel output drivers. Keys in the DISPLAY section control what is shown in the main display. The user can choose among six standard displays. Keys in the ENTRY section are used for changing the currently displayed item to a specific value. This section is also used to access secondary functions. Keys in the MODIFY section allow the user to increment the currently displayed item by configurable steps.

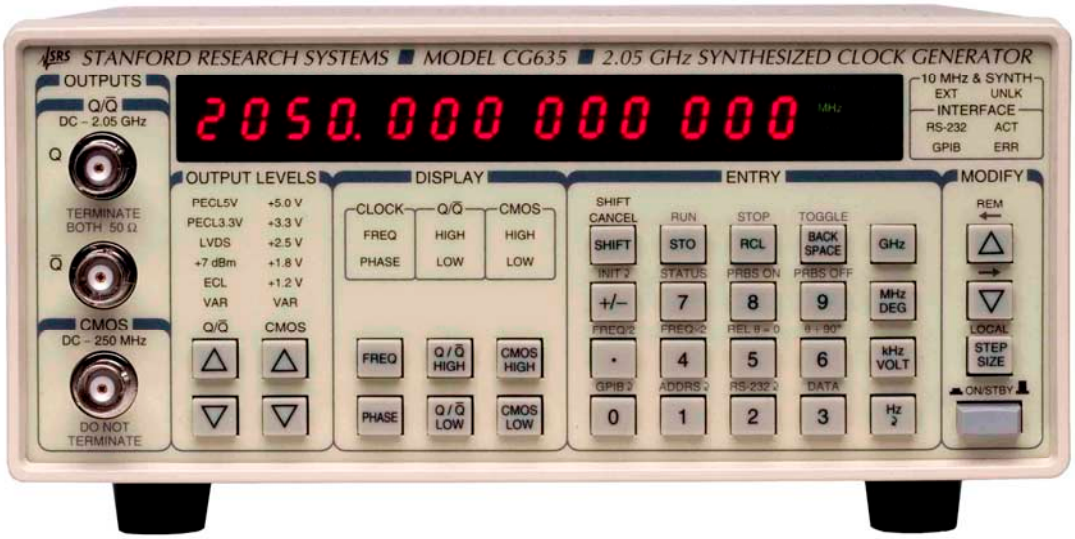


Figure 1: The CG635 Front Panel

Outputs

Q and $\bar{Q}$

The CG635 front panel includes three BNC outputs. The upper two outputs, labeled Q and $\bar{Q}$, are high-speed drivers that operate from DC to 2.05 GHZ. The outputs provide the user with fast, complementary voltages at the selected frequency, amplitude, and offset.

To operate at specification, BOTH outputs should be terminated into 50 Ω, even if only one output is used.

CMOS

The bottom output driver is a CMOS compatible driver that can operate from DC to 250 MHz. It drives the output at the selected frequency, amplitude and offset. At frequencies above 250 MHz, the CMOS driver will be turned off and forced to a low logic state. To operate at specification, the CMOS output driver should be terminated into a high impedance input and NOT terminated into 50 Ω.

Output Levels

Standard Levels

The CG635 provides a simple method for switching among five standard voltage levels for the Q / $\overline{Q}$ and CMOS outputs. The meaning of the five standard levels is summarized in Table 1 and Table 2 below:

Table 1: Q / $\overline{Q}$ Standard Output Levels

Label	Description	V_{HIGH} (V)	V_{LOW} (V)
PECL5V	ECL run on +5 VDC supply	4.00	3.20
PECL3.3V	ECL run on +3.3 VDC supply	2.30	1.50
LVDS	Low voltage differential signaling	1.43	1.07
+7 dBm	1 V_{pp} with 0.0 VDC offset	0.50	–0.50
ECL	ECL run on negative supply	–1.00	–1.80

Table 2: CMOS Standard Output Levels

Label	Description	V_{HIGH} (V)	V_{LOW} (V)
+5.0V	5 V CMOS	5.00	0.00
+3.3V	3.3 V CMOS	3.30	0.00
+2.5V	2.5 V CMOS	2.50	0.00
+1.8V	1.8 V CMOS	1.80	0.00
+1.2V	1.2 V CMOS	1.20	0.00

V_{HIGH} and V_{LOW} indicate the voltage driven by the Q / $\overline{Q}$ or CMOS outputs for the high and low logic levels.

LEDs in the OUTPUT LEVELS section indicate the standard level that is currently being driven on the output. Pressing the ▲ and ▼ keys in this section will move the standard output level up and down in the table, respectively.

Variable Levels

A sixth LED, labeled VAR, turns on when the current output levels do not correspond to any of the standard levels. In this case, the standard level LED indicates the standard level that is closest to the current level. Pressing the ▲ and ▼ keys when the VAR LED is on, forces the output to the closest standard output in the direction indicated by the key.

Display

The DISPLAY section allows the user to select which values are reported in the main front panel display. The LEDs in the display section indicate what is currently being displayed or edited. The meaning of the LEDs and keys are summarized in Table 3.

Table 3: DISPLAY Section Keys

Label	Value Shown in Main Display When Pressed
FREQ	Current frequency
PHASE	Current phase
Q / $\overline{Q}$ HIGH	Voltage for a Q / $\overline{Q}$ logic high state
Q / $\overline{Q}$ LOW	Voltage for a Q / $\overline{Q}$ logic low state
CMOS HIGH	Voltage for a CMOS logic high state
CMOS LOW	Voltage for a CMOS logic low state

The keys are used to change the main display to the indicated item. Pressing ‘FREQ’, for example, will cause the CG635 to display the current frequency. The FREQ LED will turn on, indicating that the current display is frequency.

Entry

Numeric Entry

The ENTRY section is used to modify the current settings of the CG635. In most cases, the currently displayed item can be changed by entering a new value with the numeric keys, and pressing an appropriate units key to complete the entry. For example, if the frequency is currently being displayed, pressing the keys ‘1’, ‘MHz’, sequentially will change the frequency to 1 MHz. Similarly, if the CMOS HIGH voltage is displayed, pressing the keys ‘2’, ‘.’, ‘1’, ‘VOLT’ will set the CMOS logic high voltage to 2.1 VDC.

Store and Recall Settings

The ‘STO’ and ‘RCL’ keys are for storing and recalling instrument settings, respectively. The instrument saves the frequency, phase, Q / $\overline{Q}$ and CMOS output levels, all the associated step sizes, the run/stop state, the PRBS state, and the current display. Up to ten different instrument settings may be stored in the locations 0 to 9. To save the current settings to location 5, press the keys ‘STO’, ‘5’, ‘Hz’, sequentially. To recall instrument settings from location 5, press the keys ‘RCL’, ‘5’, ‘Hz’ sequentially.

Secondary Functions

Many of the keys have secondary functions associated with them. The names of these functions are printed above the key. The ‘4’ key, for example, has FREQx2 above it. The meaning of the secondary functions is summarized in Table 4.

Table 4: Secondary Functions

Label	Function Description
RUN	Enables the output. Drives the output at the current frequency.
STOP	Stops the output. Forces the output to a logic low state.

TOGGLE	When stopped, toggles the logic state of the output
INIT	Resets the instrument to its default settings
STATUS	Displays instrument status
PRBS ON	If installed, turns on the pseudo-random binary generator
PRBS OFF	If installed, turns off the pseudo-random binary generator
FREQ/2	Divides the current frequency by 2 and displays frequency
FREQx2	Multiplies the current frequency by 2 and displays frequency
REL θ = 0	Defines the current phase to be 0 degrees and displays phase
θ + 90°	Increments the phase by 90 degrees and displays phase
GPIB	Enables the GPIB remote interface. Disables RS-232.
ADDRS	Displays / Sets the GPIB primary address for the CG635
RS-232	Enables the RS-232 remote interface. Disables GPIB.
DATA	Displays the most recent data received over the remote interface
←	Increases the current step size by the next exact factor of ten (Located in the MODIFY section.)
→	Decrease the current step size by the next exact factor of ten (Located in the MODIFY section.)

A more detailed description of each of the secondary functions is given in the Secondary Functions section of the Operation chapter (page 22).

The secondary functions can only be accessed when SHIFT mode is active, which is indicated by the SHIFT LED being turned on. The SHIFT mode can be toggled on and off by pressing the ‘SHIFT’ key. Therefore, to increase the frequency by a factor of four, you would press the ‘SHIFT’ key to activate SHIFT mode, and then press ‘4’ twice to execute FREQx2 twice. Pressing ‘SHIFT’ again toggles SHIFT mode off.

Most of the secondary functions will automatically toggle SHIFT mode off when executed. FREQ/2, FREQx2, θ + 90°, and TOGGLE are exceptions to this rule. This allows the user to easily sweep frequency or phase without having to continually reactivate SHIFT mode.

Secondary functions that have an arrow (↘) printed after them, such as INIT, GPIB, ADDRS, and RS-232, require that the user press the key ‘Hz’ to complete the action. For example, to initialize the instrument to its default settings, you would sequentially press ‘SHIFT’, ‘INIT’, ‘Hz’.

Cancel

The ‘SHIFT’ key also functions as a general purpose CANCEL key. Any numeric entry which has not been completed by pressing a units key, can be canceled by pressing the ‘SHIFT’ key. Because of the dual role played by the SHIFT key, the user may have to press ‘SHIFT’ twice to reactivate SHIFT mode. The first key press cancels the current action, and the second key press activates SHIFT mode.

Modify

Stepping Up and Down

The MODIFY section is used to step the currently displayed item up or down by a programmed amount. Each of the six standard display items listed in the DISPLAY section has a step size associated with it. Normally, pressing the MODIFY ▲ and ▼ keys causes the displayed item to increment and decrement, respectively, by the associated step size.

Step Size

The step size for the current standard display can be viewed by pressing the 'STEP SIZE' key. Pressing 'STEP SIZE' a second time toggles the view back to the standard display. When the step size is being viewed, the STEP LED in the main display will be turn on. To view the frequency step size, press 'FREQ', 'STEP SIZE', sequentially. Pressing 'FREQ' ensures that frequency is the current standard display. Pressing 'STEP SIZE' then toggles the main display to the step size associated with frequency.

The step size can be changed in a number of ways. If the current step size is being displayed, the user can modify the current step size in one of two ways. First, you can enter a new value with the numeric keys in the ENTRY section and complete the entry by pressing an appropriate units key. Second, you can increment and decrement the current step size by exact factors of ten by pressing the MODIFY ▲ and ▼ keys, respectively. For example, if the currently displayed frequency step size is 1.000 Hz, then the step size can be increased to 10.000 Hz by pressing MODIFY ▲ once.

The step size can also be changed, even when the current step size is not being displayed. This is accomplished by accessing the SHIFTED functions ← and → shown above the MODIFY ▲ and ▼ keys, respectively. For example, pressing 'SHIFT', MODIFY ▲, sequentially will increase the associated step size to the next exact factor of ten.

When the step size of a standard display item is an exact factor of ten, the corresponding digit in the main display will blink. This provides a convenient visual cue to let the user know which digit will change when the user presses the MODIFY ▲ and ▼ keys. For example, if the frequency step size is 1.000 Hz, and the displayed frequency is 123456.789 Hz, then the '6' will be blinking. Pressing the MODIFY ▲ key will step the frequency up 1 Hz to 123457.789 Hz.

Remote and Local Mode

The REM LED turns on when the CG635 is placed in remote mode by the GPIB bus. In this mode, all the front panel keys are disabled and the instrument can only be controlled via the GPIB bus. The user can return to normal, local mode by pressing the 'STEP SIZE' key once. The 'LOCAL' label above the key indicates the dual functionality of the 'STEP SIZE' key.

Clock Status and Interface Indicators

10 MHz & SYNTH

In the upper right portion of the front panel are two groups of LED indicators. The upper group is labeled 10 MHz & SYNTH. This contains the EXT and UNLK LEDs. The EXT LED indicates that the CG635 has detected an external 10 MHz reference at the 10 MHz input BNC on the rear panel of the CG635. The CG635 will lock its internal clock to this external reference.

The UNLK LED indicates that the output has not yet stabilized for some reason. This is usually due to a user request to change frequency or phase. Frequency changes can take roughly 30 ms to stabilize. A backward phase step of 360 degrees at 1 Hz can take as long as 1.5 s to complete. The UNLK LED may also indicate that the internal clock has not locked to the external reference.

INTERFACE

The lower group of LED indicators is labeled INTERFACE. These LEDs indicate the current status of RS-232 or GPIB remote programming interfaces. The RS-232 LED is on if the instrument is configured to accept commands over the RS-232 interface. Alternately, the GPIB LED is on if the instrument is configured to accept commands over the IEEE-488 port. When a character is received or sent over one of the interfaces, the ACT LED will flash. This is helpful when troubleshooting communications problems. If a command received over the remote interface fails to execute due to either a parsing error or an execution error, the ERR LED will flash.

Rear-Panel Overview

The rear panel provides connectors for AC power, GPIB/RS-232 computer interfaces, chassis ground, external timing references, clock edge timing modulation, additional clock outputs, and an optional, pseudo-random binary sequence generator (see Figure 2).

Figure 2: The CG635 Rear Panel

AC Power

The Power Entry Module is used to connect the CG635 to a power source through the power cord provided with the instrument. The center pin is connected to the CG635 chassis so that the entire box is grounded.

The source voltage requirements are: 90 to 132 VAC or 175 to 264 VAC, 47 to 63 Hz (80 VA total).

Connect the CG635 to a properly grounded outlet. Consult an electrician if necessary.

GPIB

The CG635 comes standard with a GPIB (IEEE-488) communications port for communications over a GPIB bus. The CG635 supports the IEEE-488.1 (1978) interface standard. It also supports the required common commands of the IEEE-488.2 (1987) standard.

Before attempting to communicate with the CG635 over the GPIB interface, the port must be enabled via the front panel. Do this by sequentially pressing the following keys located in the ENTRY section: ‘SHIFT’, ‘GPIB’, ‘Hz’. The GPIB address can be changed by pressing the keys ‘SHIFT’, ‘ADDRS’. Use the MODIFY ‘UP’ and ‘DOWN’ keys to select the desired address. Press ‘Hz’ to complete change.

A host computer interfaced to the CG635 can perform virtually any operation that is accessible from the front panel. Programming the CG635 is discussed in the CG635 Remote Programming chapter.

RS-232

The CG635 comes standard with an RS-232 communications port. The RS-232 interface connector is a standard 9 pin, type D, female connector configured as a DCE (transmit on pin 3, receive on pin 2). The communication parameters are fixed at: 9600 Baud, 8 Data bits, 1 Stop bit, No Parity, RTS/CTS Hardware Flow Control.

Before attempting to communicate with the CG635 over RS-232, the port must be enabled via the front panel. Do this by sequentially pressing the following keys located in the ENTRY section: 'SHIFT', 'RS-232', 'Hz'.

A host computer interfaced to the CG635 can perform virtually any operation that is accessible from the front panel. Programming the CG635 is discussed in the CG635 Remote Programming chapter.

Chassis Ground

Use this grounding lug to connect the CG635 chassis directly to facility ground

Timebase

10 MHz IN

The CG635 provides a 10 MHz BNC input for synchronizing its internal clock to an external 10 MHz reference. The external reference should provide greater than 0.5 V_{pp} into a 1 kΩ impedance. The CG635 will automatically detect the presence of an external 10 MHz reference and lock to it if possible. If the CG635 is unable to lock to the external reference, the front-panel UNLK LED will turn on and stay on until the CG635 either successfully locks to the external reference or the reference is removed.

10 MHz OUT

The CG635 provides a 10 MHz BNC output for synchronizing other instrumentation to the CG635's timebase.

T_{mod} Input

The CG635 clock edges can be modulated over ±5 ns by providing a modulation voltage to the T_{mod} BNC input. The input is calibrated to provide 1 ns of modulation for 1 volt of input swing. The input can accept voltages of ±5 V. Positive inputs advance the clock outputs, negative inputs retard the clock outputs.

The T_{mod} input can be very useful for characterizing a circuit's susceptibility to timing jitter.

Clock Output

The CG635 interfaces to a number of optional clock receiver modules which can be used to get a clock signal from the CG635 to where it is needed. The receiver modules regenerate the clock locally providing the user with clean, fast clock edges, even if the CG635 is several meters away. Receiver modules are available for generating most of the standard CMOS and ECL signal levels.

All modules provide both +CLK and –CLK with a source impedance of 50 Ω, and connect to the rear-panel RJ-45 connector using standard Category-6 cable. Table 5 summarizes the features of the optional receiver modules offered by SRS. The maximum frequency (F_{max}) listed in the table for each module is the maximum frequency at which the module operates at specification. With the exception of the CG640, the modules continue to operate above F_{max}, but with reduced amplitude.

Table 5: Optional Receiver Modules

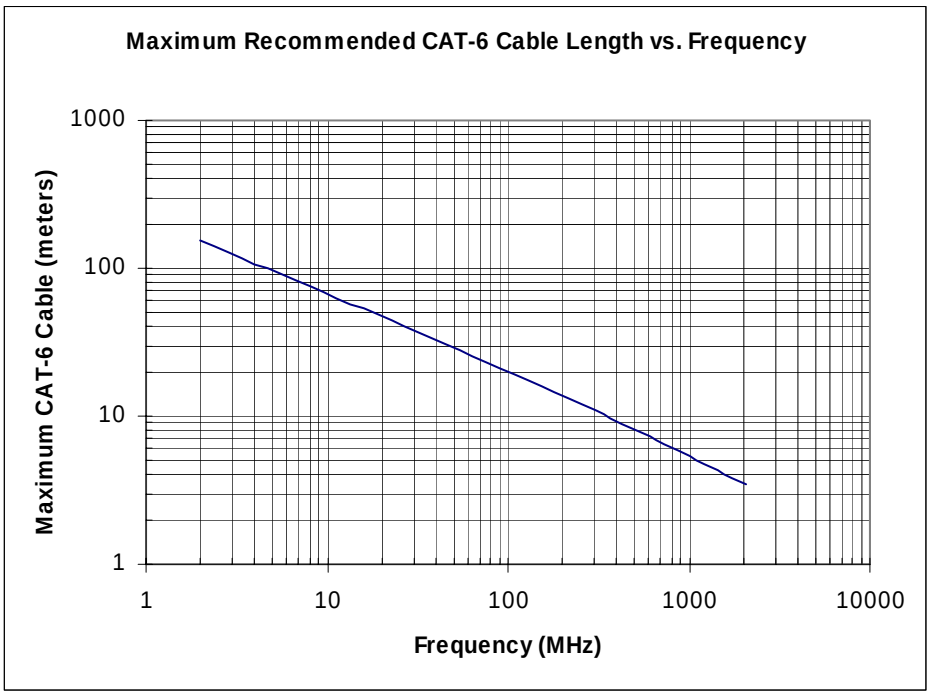
Model	Description	Termination Impedance	Transition Time(max)	F_{max} (2)
CG640	CMOS (+5 V_{cc})	High Z	2.0 ns	105 MHz (1)
CG641	CMOS (+3.3 V_{cc})	High Z	800 ps	250 MHz
CG642	CMOS (+2.5 V_{cc})	High Z	800 ps	250 MHz
CG643	PECL (+5 V_{cc})	High Z	800 ps	250 MHz
CG644	PECL (+3.3 V_{cc})	50 Ω	100 ps	2.05 GHz
CG645	PECL (+2.5 V_{cc})	50 Ω	100 ps	2.05 GHz
CG646	RF (+7 dBm)	50 Ω	100 ps	2.05 GHz
CG647	CML/NIM	50 Ω	100 ps	2.05 GHz
CG648	ECL	50 Ω	100 ps	2.05 GHz
CG649	LVDS	50 Ω	100 ps	2.05 GHz

Notes: (1) Output is set to logic '0' above F_{max}.
(2) Maximum operating frequency is limited by the CAT-6 cable length.

The maximum frequency may also be limited by the CAT-6 cable length. At 2 GHz, the cable may be up to 10 feet long. At 10 MHz, the cable may be up to 200 feet long. Figure 3 summarizes the limitation on maximum frequency due to cable length.

If clock regeneration is not needed, the user can interface directly to the clock signals provided on the various pins of the RJ-45 connector. The clock signals and pin assignments are printed on the rear panel of the CG635 in the CLOCK OUT section.

Figure 3: Maximum recommended CAT-6 cable length as a function frequency.



PRBS and Clock Option

An optional pseudo-random binary sequence generator for the CG635 is also available from SRS. If installed, both the PRBS data and the clock are output as LVDS levels on rear-panel SMA connectors.

A Pseudo-Random Binary Sequence (PRBS) generator is used for testing data transmission systems. A typical arrangement is to display an “eye pattern” on an oscilloscope by triggering the oscilloscope with the clock while displaying the (random) data after it passes through the data transmission system. An “open” eye pattern is necessary for reliable data transmission. The eye pattern “closes” from the left and right with jitter, and from the top and bottom with insufficient channel bandwidth, increasing the likelihood for transmission errors.

The most common way to create a PRBS generator is to use a linear shift-register, feeding the input of the shift-register with the exclusive OR of two (particular) data bits as they shift through the system. The CG635 uses a 7-bit ECL shift register that provides a pseudo-random bit sequence which repeats after $2^7 – 1 = 127$ clock cycles. The data bit stream is described by the polynomial $x^7 + x^6 + 1$. It satisfies many criteria to qualify as “random”; however, it does repeat itself (exactly) after 127 clock cycles. Another departure from randomness is that the longest string of “1’s” is seven in a row, while the longest string of “0’s” is six in a row.

Operation

Front-Panel User Interface

The previous chapter described the function of the front-panel keys based on their location on the front panel. This section provides guidelines for viewing and changing instrument parameters independent of their location on the front panel.

Power On

At power on, the CG635 performs a number of self tests to verify that various internal components are operating correctly. If any of the tests fail, the CG635 will briefly display "Failed" after the test. In such a case, consult the troubleshooting section later in this chapter before contacting SRS or an authorized representative to repair the unit.

After the self tests have completed, the CG635 will recall the latest known instrument settings from nonvolatile memory and be ready for use.

The CG635 continuously monitors front-panel key presses and will save the current instrument settings to nonvolatile memory after approximately ten seconds of inactivity. To prevent the nonvolatile memory from wearing out, however, the CG635 will not automatically save instrument settings that change due to commands executed over the remote interface. The remote commands *SAV and *RCL can be used to explicitly save instrument settings over the remote interface, if desired. See the CG635 Remote Programming chapter for more information about these commands.

The CG635 can be forced to boot up at factory default settings. This is accomplished by pressing and holding the 'BACK SPACE' key during power up, until the initialization is complete. All instrument parameters will be set back to their default values, including the enabled remote interface and the GPIB address. See the Default Factory Settings section later in this chapter for a listing of the default settings.

Displaying a Parameter

The CG635 has six main displays which are activated by pressing the keys in the DISPLAY section of the front panel. The function of each key is summarized in Table 6.

Table 6: DISPLAY Section Keys

Label	Value Shown in Main Display When Pressed
FREQ	Current frequency
PHASE	Current phase
Q / $\overline{Q}$ HIGH	Voltage for a Q / $\overline{Q}$ logic high state
Q / $\overline{Q}$ LOW	Voltage for a Q / $\overline{Q}$ logic low state
CMOS HIGH	Voltage for a CMOS logic high state
CMOS LOW	Voltage for a CMOS logic low state

Each of these parameters has an independent step size associated with it. When one of the six main displays is active, the associated step size for the parameter can be displayed by pressing the 'STEP SIZE' button in the MODIFY section of the front panel. Pressing the 'STEP SIZE' key again toggles the display back to the original parameter. When the step size for a parameter is displayed, the STEP LED in the main display will be highlighted.

For example, to display the frequency, press the 'FREQ' key. Now that frequency is displayed you can display the frequency step size by pressing the 'STEP SIZE' key. The STEP LED should be highlighted in the main display. Pressing 'STEP SIZE' once more toggles the display back to frequency. The STEP LED should now be off.

Changing a Parameter

To change a parameter, enter a new value using the numeric keys in the ENTRY section of the front panel, and complete the entry by pressing an appropriate units key. Generally speaking, only displayed parameters can be changed. For example, to change the frequency to 10 kHz, press the following keys sequentially: 'FREQ', '1', '0', 'kHz'. Pressing 'FREQ' selects it for display and editing. Pressing '1' initiates the parameter change. Pressing 'kHz' completes the numeric entry and sets the frequency to 10 kHz.

The same techniques can be used to change the step size of a parameter. The only difference is that the parameter step size must be displayed first, before entering a new value.

If the user enters extra digits beyond the allowed resolution of a parameter, the extra digits will be ignored. For example, the phase has a resolution of 1 degree at 1 GHz. Entering a step size of 2.5 degrees will result in the step size being truncated to 2 degrees.

Stepping a Parameter

The six main parameters can be stepped up and down by their associated step sizes by respectively pressing the ▲ and ▼ keys in the MODIFY section of the front panel. For example, if frequency is currently being displayed as 10.000000000 MHz, and the frequency step size is 1.000 Hz, then pressing MODIFY ▲ will change the frequency to 10.000001000 MHz. Pressing MODIFY ▼ will bring the frequency back to 10 MHz.

Step Sizes of Exact Factors of Ten

If a parameter's step size is an exact factor of ten, then the corresponding digit in the main display of the parameter will blink. This provides a visual cue to inform the user of the digit that will change when the parameter is stepped up or down. For example, if the frequency step size is 1.000 Hz, and the displayed frequency is 123456.789 Hz, then the '6' will be blinking. Pressing the MODIFY ▲ key will step the frequency up 1 Hz to 123457.789 Hz.

When a parameter step size is being displayed, the user can increase or decrease the step size to the nearest exact factor of ten by pressing the MODIFY ▲ and ▼ keys, respectively. For example, if the current frequency step size is being displayed as 1.000 Hz, then pressing MODIFY ▲ will increase to the step size to 10.000 Hz.

The same behavior can also be achieved even when the current step size is NOT being displayed. This is accomplished by accessing the SHIFTED functions ← and → shown above the MODIFY ▲ and ▼ keys, respectively. For example, if the frequency is being displayed as 123456.789 Hz, and the frequency step size is 1 Hz, then sequentially pressing 'SHIFT', MODIFY ▲ will increase the associated step size to 10 Hz. The '6' will stop blinking and the '5' will start blinking to indicate the new step size.

Changing Units

Frequency has the option of being displayed in units of GHz, MHz, kHz, or Hz. When the user enters a frequency using the front panel, the CG635 will display the frequency in the units used to complete the entry. For example, pressing the keys 'FREQ', '1', '0', 'kHz' sequentially, to change the frequency to 10 kHz, will cause the CG635 to display the result as 10.000000 kHz. The user can change the displayed units by pressing a different units key. Continuing with the previous example, if the user presses 'Hz', the CG635 will change the display to 10000.000 Hz.

Store and Recall Settings

The 'STO' and 'RCL' keys are for storing and recalling instrument settings, respectively. The instrument saves the frequency, phase, Q / $\overline{Q}$ and CMOS output levels, all the associated step sizes, the run/stop state, the PRBS state, and the current display. Up to ten different instrument settings may be stored in the locations 0 to 9. To save the current settings to location 5, for example, press the keys 'STO', '5', 'Hz' sequentially. To recall instrument settings from location 5, press the keys 'RCL', '5', 'Hz' sequentially. The user may also use the MODIFY ▲ and ▼ keys to select the desired location, rather than enter the location directly with the numeric keys. The CG635 will remember the last location used for store and recall. To reuse the remembered location, simply skip the numeric entry when storing or recalling settings. For example, to recall settings from the remembered location, the user should simply press 'RCL', 'Hz.'

Secondary Functions

Most of the keys in the ENTRY section of the front panel have secondary functions associated with them. The names of these functions are printed above the key. The '4' key, for example, has FREQx2 above it.

The secondary functions can only be accessed when SHIFT mode is active, which is indicated by the SHIFT LED being turned on. The SHIFT mode can be toggled on and off by pressing the 'SHIFT' key. Therefore, to increase the frequency by a factor of four, you would press the 'SHIFT' key to activate SHIFT mode, and then press '4' twice to execute FREQx2 twice. Pressing 'SHIFT' again toggles SHIFT mode off.

Most of the secondary functions will automatically toggle SHIFT mode off when executed. FREQ/2, FREQx2, θ + 90°, and TOGGLE are exceptions to this rule. This allows the user to easily sweep frequency or phase without having to continually reactivate SHIFT mode.

Secondary functions that have an arrow (↴) printed after them, such as INIT, GPIB, ADDRS, and RS-232, require that the user press the key 'Hz' to complete the action. For

example, to initialize the instrument to its default settings, you would press 'SHIFT', 'INIT', 'Hz' sequentially.

Detailed descriptions of each of the secondary functions can be found later in this chapter.

Q and $\overline{Q}$ Outputs

The Q and $\overline{Q}$ outputs on the front panel are high-speed, differential, ECL-compatible drivers that operate from DC to 2.05 GHz with a nominal 50 % duty cycle. The rise and fall times of these outputs are <100 ps. The outputs provide the user with fast, complementary voltages at the selected frequency, amplitude, and offset. To operate at specification, BOTH outputs should be terminated into 50 Ω, even if only one output is used.

The user can easily switch between five standard output voltage levels by pressing the Q / $\overline{Q}$ ▲ and ▼ keys in the OUTPUT LEVELS section of the front panel. When the Q / $\overline{Q}$ outputs are at a standard level, the appropriate standard level LED will be highlighted. The meaning of the five standard levels is summarized in Table 7.

Table 7: Q / $\overline{Q}$ Standard Output Levels

Label	Description	V_{HIGH} (V)	V_{LOW} (V)
PECL5V	ECL run on +5 VDC supply	4.00	3.20
PECL3.3V	ECL run on +3.3 VDC supply	2.30	1.50
LVDS	Low voltage differential signaling	1.43	1.07
+7 dBm	1 V_{pp} with 0.0 VDC offset	0.50	–0.50
ECL	ECL run on negative supply	–1.00	–1.80

V_{HIGH} and V_{LOW} indicate the voltage driven by the Q and $\overline{Q}$ outputs for the high and low logic levels, respectively.

Various ECL logic families have different logic thresholds that may vary with temperature. The ECL levels in the table above were chosen to lie between the levels for the 10 k and 100 k ECL logic families when operated at 25 ºC. The differences are small: at 25 ºC the typical V_{HIGH} for an ECL part run off a negative supply is -0.945 V (for the 10 k series) and –1.020 V (for the 100 k series), while V_{LOW} is –1.745 V (for the 10 k series) and –1.820 V (for the 100 k series). As seen in Table 7, the CG635 will provide a V_{HIGH} of –1.00 V and a V_{LOW} of –1.80 V.

The user also has the ability to set the Q / $\overline{Q}$ outputs to nonstandard levels. When the outputs differ from the standard levels, the Q / $\overline{Q}$ VAR LED in the OUTPUT LEVELS section will turn on. In this case, the highlighted standard LED indicates the standard level nearest the current output levels. Pressing the Q / $\overline{Q}$ ▲ and ▼ keys when the VAR LED is on will force the outputs to the nearest standard level in the direction indicated by the key.

The voltages for Q / $\overline{Q}$ high and low states can be viewed in the main display by pressing 'Q/$\overline{Q}$ HIGH' and 'Q/$\overline{Q}$ LOW' keys in the DISPLAY section of the front panel.

The Q / $\overline{Q}$ high and low voltages may be set to arbitrary values, or stepped up and down by configurable step sizes by following the instructions described in the Front-Panel User Interface section at the beginning of this chapter. However, the limits summarized in Table 8 apply.

Table 8: Limits for Q / $\overline{Q}$ High and Low Voltages

Parameter	Minimum	Maximum	Resolution
Q / $\overline{Q}$ HIGH (V_{HIGH})	–2.00 V	5.00 V	0.01 V
Q / $\overline{Q}$ LOW (V_{LOW})	–3.00 V	4.80 V	0.01 V
Q / $\overline{Q}$ Amplitude (V_{HIGH}–V_{LOW})	0.20 V	1.00 V	0.01 V

Beware that a +5 V output will dissipate ½ watt into the target system's 50 Ω termination.

If the user tries to enter a value that violates the V_{HIGH} or V_{LOW} limit, the CG635 will briefly display "Volt Error" and leave the current value unchanged. However, if the user tries to enter a value that is valid in terms of the limits on V_{HIGH} and V_{LOW}, but violates the amplitude limit, the CG635 will change both the requested voltage and its complement. The requested voltage will be set to the desired level, and the complementary voltage will be adjusted to satisfy the amplitude limits. The CG635 will briefly display "lo is N.NN" or "hi is N.NN" to indicate the new complementary voltage level. If $V_{HIGH} - V_{LOW}$ would be > 1.00 V, V_{LOW} will be set 1.00 V below V_{HIGH} or V_{HIGH} will be set 1.00 V above V_{LOW}. If $V_{HIGH} - V_{LOW}$ would be < 0.20 V, V_{LOW} will be set 0.20 V below V_{HIGH} or V_{HIGH} will be set 0.20 V above V_{LOW}.

For example, if the outputs are currently at LVDS levels, setting V_{HIGH} to 5.5 V will cause the CG635 to briefly display "Volt Error" and leave the outputs unchanged, because 5.5 V exceeds the upper limit for V_{HIGH}. On the other hand, setting V_{HIGH} to 5.0 V will cause the CG635 to briefly display "Lo is 4.00" and to set V_{HIGH} and V_{LOW} to 5.00 V and 4.00 V, respectively. V_{LOW} is adjusted in addition to V_{HIGH} in order to satisfy the amplitude limits.

CMOS Output

The CMOS output provides CMOS compatible voltages at a 50 % duty cycle. The transition times of this output are less than 1.0 ns (10% to 90%). It drives the output at the selected frequency, amplitude and offset for frequencies ranging from DC to 250 MHz. At frequencies above 250 MHz, the CMOS driver will be turned off and forced to a low logic state.

Despite its relatively high speed, the CMOS output should not be terminated with a 50 Ω load. Terminating the output will not harm the instrument but it will divide the output voltage levels in half. The CMOS output has a 50 Ω source impedance and so will reverse terminate pulses which are reflected back from the user's (unterminated) target system. For CMOS levels below 2.50 V, the user may wish to terminate the CMOS output with a 50 Ω load and set the output levels to twice that required by the user's target system. Doing so will somewhat improve the rise time and reduce reflected clocks edges on the output.

The user can easily switch between five standard output voltage levels by pressing the CMOS ▲ and ▼ keys in the OUTPUT LEVELS section of the front panel. When the CMOS output is at a standard level, the CG635 will highlight the appropriate standard level LED. The meaning of the five standard levels is summarized in the Table 9.

Table 9: CMOS Standard Output Levels

Label	Description	V_{HIGH} (V)	V_{LOW} (V)
+5.0V	5 V CMOS	5.00	0.00
+3.3V	3.3 V CMOS	3.30	0.00
+2.5V	2.5 V CMOS	2.50	0.00
+1.8V	1.8 V CMOS	1.80	0.00
+1.2V	1.2 V CMOS	1.20	0.00

V_{HIGH} and V_{LOW} indicate the voltage driven by the CMOS output for the high and low logic levels, respectively.

The user also has the ability to set the CMOS output to nonstandard levels. When the output differs from the standard levels, the CMOS VAR LED in the OUTPUT LEVELS section will turn on. In this case, the highlighted standard LED indicates the standard level nearest the current output level. Pressing the CMOS ▲ and ▼ keys when the VAR LED is on will force the outputs to the nearest standard level in the direction indicated by the key.

The voltages for CMOS high and low states can be viewed in the main display by pressing 'CMOS HIGH' and 'CMOS LOW' keys in the DISPLAY section of the front panel.

The CMOS high and low voltages may be set to arbitrary values, or stepped up and down by configurable step sizes by following the instructions described in the Front-Panel User Interface section at the beginning of this chapter. However, the limits summarized in Table 10 apply.

Table 10: Limits for CMOS High and Low Voltages

Parameter	Minimum	Maximum	Resolution
CMOS HIGH (V_{HIGH})	–0.50 V	6.00 V	0.01 V
CMOS LOW (V_{LOW})	–1.00 V	1.00 V	0.01 V
CMOS Amplitude(V_{HIGH}–V_{LOW})	0.50 V	6.00 V	0.01 V

If the user tries to enter a value that violates the V_{HIGH} or V_{LOW} limit, the CG635 will briefly display "Volt Error" and leave the current value unchanged. However, if the user tries to enter a value that is valid in terms of the limits on V_{HIGH} and V_{LOW}, but violates the amplitude limit, the CG635 will change both the requested voltage and its complement. The requested voltage will be set to the desired level, and the complementary voltage will be adjusted to satisfy the amplitude limits. The CG635 will briefly display "lo is N.NN" or "hi is N.NN" to indicate the new complementary voltage level. If $V_{HIGH} - V_{LOW}$ would be > 6.00 V, V_{LOW} will be set 6.00 V below V_{HIGH} or V_{HIGH} will be set 6.00 V above V_{LOW}. If $V_{HIGH} - V_{LOW}$ would be < 0.50 V, V_{LOW} will be set 0.50 V below V_{HIGH} or V_{HIGH} will be set 0.50 V above V_{LOW}.

For example, if the outputs are currently at +3.3 V CMOS levels, setting V_{HIGH} to 6.5 V will cause the CG635 to briefly display "Volt Error" and leave the outputs unchanged, because 6.5 V exceeds the upper limit for V_{HIGH}. On the other hand, setting V_{HIGH} to 0.25 V will cause the CG635 to briefly display "Lo is -0.25" and to set V_{HIGH} and V_{LOW} to 0.25 V and –0.25 V, respectively. V_{LOW} is adjusted in addition to V_{HIGH} in order to satisfy the amplitude limits.

Frequency

The CG635 can output frequencies in the range 1 µHz to 2.05 GHz with up to 1 pHz of resolution and 16 significant digits. The frequency may be set to arbitrary values, or stepped up and down by configurable step sizes by following the instructions described in the Front-Panel User Interface section at the beginning of this chapter. All sixteen significant digits can be entered via the front panel. If the user enters more than sixteen digits, the result will be truncated to sixteen digits. If the user enters an invalid frequency, the CG635 will briefly display "Freq Error" and leave the frequency unchanged.

While the frequency can be set to 16 significant digits, the CG635's main display is only 13 digits wide. For most users, this will not be a problem because the extra digits will usually be zero. Nevertheless, the user can view the extra significant digits by pressing and holding the 'FREQ' key down. After a brief delay, the CG635 will display all significant digits below 1 Hz. For example, if the frequency is 1234567890.123456 Hz, the CG635's main display for frequency will be 1234567890.123 Hz. If the user then presses and holds the 'FREQ' key down, the display will show 0.123456 Hz after a brief delay.

Similarly, the extra significant digits for the frequency step size can be viewed by first pressing 'FREQ', and then pressing and holding 'STEP SIZE' down.

The frequency resolution is limited by the available significant digits. For frequencies less than 10 kHz, the resolution is 1 pHz. Starting at 10 kHz, the resolution is reduced by a factor of ten for each decade of frequency from 10 kHz to 1 GHz where the resolution is 1 µHz.

The CG635 truncates both the frequency and the frequency step size to the available resolution when the frequency changes. Thus, if the current step size is 1 pHz, and the user changes the frequency to 1 GHz, the CG635 will also modify the frequency step size to be 1 µHz, which is the minimum valid step size for frequencies of 1 GHz.

Normally, when the user steps the frequency up and down by a small amount, the CG635 will seamlessly slew the output to the new frequency. If the user crosses an octave boundary, however, the CG635 will disable the output momentarily, forcing it low for about 10 ms before re-enabling it at the new frequency. The octave boundaries are a consequence of the fact that the CG635 generates all output frequencies by dividing down the output of an RF VCO that operates from 960 MHz to 2.05 GHz, which is a little more than one octave of tuning range.

An example should make the operation clear. When the frequency is 1.5 MHz, the divider is 1024, and the RF VCO operates at 1024×1.5 MHz = 1.536 GHz. Now, suppose you increase the frequency in steps of 0.1 MHz to 2.1 MHz. From 1.5 MHz to 2.0 MHz,

the divider remains at 1024 and the RF VCO increases in corresponding steps to 1024×2.0 MHz = 2.048 GHz. At 2.1 MHz, however, the CG635 crosses an octave boundary because the RF VCO does not have the range to provide 1024×2.1 MHz = 2.1504 GHz. Therefore, the CG635 changes the divider to 512 and slews the RF VCO back to 512×2.1 MHz = 1.0752 GHz.

The CG635 has fifty-one, overlapping octave bands. They are summarized in Table 11.

Table 11: CG635's Fifty-one, Overlapping Octave Bands

Band	Divider	Min Frequency (Hz)	Max Frequency (Hz)
0	1	960,000,000	2,050,000,000
1	2	480,000,000	1,024,000,000
2	4	240,000,000	512,000,000
3	8	120,000,000	256,000,000
4	16	60,000,000	128,000,000
5	32	30,000,000	64,000,000
6	64	15,000,000	32,000,000
7	128	7,500,000	16,000,000
8	256	3,750,000	8,000,000
9	512	1,875,000	4,000,000
10	1024	937,500	2,000,000
11	2048	468,750	1,000,000
…	…	…	…
49	2^{49}	0.000,001,705,302	0.000,003,637,978
50	2^{50}	0.000,000,852,651	0.000,001,818,989

When the user changes the frequency, the CG635 attempts to stay within the same octave. If an octave switch is required, however, and the frequency is in one of the first eleven bands, the CG635 will disable the output, forcing it low before changing the divider and slewing the RF VCO to the new frequency. When the VCO has settled at the new frequency, the output will be re-enabled in a “runtless” fashion. This is done to protect the user’s application from spurious clock pulses and frequencies as the dividers are changed.

For frequencies in bands eleven to fifty, the CG635 uses DDS technology to seamlessly change dividers. Since no spurious pulses are generated, the output is not disabled.

In addition to the normal methods of stepping frequency by the current step size, the user can also step the frequency by factors of two by accessing the secondary functions FREQ/2 and FREQx2.

Phase

The CG635 can adjust the phase of the output by up to 360° per step. The phase may be set to arbitrary values, or stepped up and down by configurable step sizes by following the instructions described in the Front-Panel User Interface section at the beginning of this chapter. If the user enters a phase that requires the output to adjust by more than 360°, the CG635 will briefly display “Step Error” and leave the phase unchanged.

The CG635 will integrate phase steps in the main display until the phase reaches ±720°, at which point it will wrap the phase back to 0°. For example, if the current phase is 700°, and the user steps the phase 90°, the CG635 will display 70°.

The phase resolution of the CG635 is frequency dependent and is summarized in Table 12.

Table 12: Phase Resolution versus Frequency

Frequency	Phase Resolution
200 MHz < f ≤ 2.05 GHz	1°
20 MHz < f ≤ 200 MHz	0.1°
2 MHz < f ≤ 20 MHz	0.01°
200 kHz < f ≤ 2 MHz	0.001°
20 kHz < f ≤ 200 kHz	0.0001°
2 kHz < f ≤ 20 kHz	0.00001°
200 Hz < f ≤ 2 kHz	0.000001°
20 Hz < f ≤ 200 Hz	0.0000001°
2 Hz < f ≤ 20 Hz	0.00000001°
1 µHz ≤ f ≤ 2 Hz	0.000000001°

If the user tries to enter a phase with more resolution than permitted, the CG635 will truncate the result to the appropriate resolution.

When the user changes frequency, the CG635 will automatically reset the phase to 0°, and truncate the phase step size to the resolution allowed at the new frequency. For example, let the current phase and phase step size be 123.456° and 0.0001°, respectively. If the user changes the frequency to 100 MHz, the CG635 will change the phase and phase step sizes to 0.0° and 0.1°.

The user can define the current phase to be zero degrees by accessing the secondary function REL θ = 0°. The secondary function, θ + 90°, is also available for advancing the phase by 90°.

For frequencies greater than or equal to 1 Hz, the CG635 adjusts phase by increasing or decreasing the frequency for a short interval of time to advance or retard the phase by the desired amount. This is the case even when the phase step is 360°. Advancing phase by 360° results in one extra cycle being inserted over the time period of the phase shift. Similarly, retarding phase by 360° results in one less cycle being inserted over the time period of the phase shift.

In most cases, phase shifts take less than 150 ms to complete. At low frequencies, however, backward phase shifts can take significantly longer. This is simply due to the fact that the frequency can not be shifted below 0 Hz. Therefore, a backwards phase shift of 360° at 1 Hz takes a minimum of one second to complete. Arming circuitry in the CG635 may add an additional 0.5 seconds to that time.

For frequencies less than 1 Hz, the CG635 does “instantaneous” phase shifts using DDS techniques. In contrast to phase shifts at frequencies above 1 Hz, a 360° phase shift at

frequencies less than 1 Hz is equivalent to doing nothing. Extra cycles are not inserted or deleted as part of the phase shift.

The current phase is stored as part of the instrument settings when the user stores and recalls settings. However, the current phase only has meaning at the current frequency. Therefore, the phase will only be recalled if the recall of settings does not alter the current frequency and does not result in a phase shift larger than 360°. Otherwise, the phase will be simply set to zero.

Secondary Functions

Most of the keys in the ENTRY section of the front panel have secondary functions associated with them. The names of these functions are printed above the key. The '4' key, for example, has FREQx2 above it.

To access these secondary functions, follow the instructions described in the Front-Panel User Interface section at the beginning of this chapter. Details about each of the functions follow.

RUN, STOP, TOGGLE

Normally, the CG635 drives the front-panel outputs with square waves at the selected frequency, phase, and amplitude settings. The STOP function causes the CG635 to disable oscillation and force the outputs to a logic low state. When the outputs are in the stopped state, the STOP LED will blink. Once outputs are stopped, the TOGGLE function can be used to toggle the state of the outputs. The RUN function restores the CG635 outputs to normal, running operation.

The run/stop state of the instrument is saved when instrument settings are saved.

INIT

The INIT function causes the CG635 to return to default settings. This function is not executed until the user presses 'Hz.' Table 15 itemizes the CG635 default settings. The remote interface, GPIB address, and power-on status clear are not affected by this command, however.

STATUS

The STATUS function displays a number of instrument parameters which characterize the current status of the CG635. The user can cycle through each of the parameters by pressing the MODIFY ▲ and ▼ keys. The meaning of each of the parameters is summarized in Table 13.

Table 13: Status Parameters

Label	Description
STATUS	CG635 serial poll status byte
SYNTH	Current lock state of CG635
ERRORS	Number of errors in the error buffer

R	RF synthesizer R parameter
N	RF synthesizer N parameter
D	Divider = 2^D
FT3	Bits 48-63 of the frequency tuning word
FT2	Bits 32-47 of the frequency tuning word
FT1	Bits 16-31 of the frequency tuning word
FT0	Bits 0-15 of the frequency tuning word
PRBS	PRBS on/off/disabled status (if installed)
RB	Rb stability (if installed)

The STATUS parameter displays the current value of the CG635 serial poll status byte. This is the same value that is returned by the *STB? command. See the CG635 Remote Programming chapter for information on how to interpret the status byte.

The SYNTH parameter displays the current lock status of CG635. The interpretation of each lock status bit is summarized in Table 14. The red UNLK LED will be on when any of these bits is set. If the SYNTH parameter is 3, for example, then the RF and 19 MHz PLLs are currently unlocked.

Table 14: Synthesizer Lock Status

Bit	Name	Meaning
0	RF_UNLOCK	RF PLL is unlocked.
1	19MHZ_UNLOCK	19 MHz PLL is unlocked
2	10MHZ_UNLOCK	10 MHz PLL is unlocked
3	RB_UNLOCK	Optional Rb oscillator is unlocked
4	OUTPUT_DISABLED	The output is disabled
5	PHASE_SHIFT	The output is scheduled to shift phase.
6	Reserved	
7	Reserved	

The interpretation of the SYNTH parameter is similar to that of the lock status register (LCKR? command). The difference is that the SYNTH parameter bits indicate the current state of each bit, while the lock status register bits indicate whether the bits have been set since the register was last read.

The ERRORS parameter displays the number of errors currently stored in the error buffer. The errors may be retrieved one by one over the remote interface by repeatedly sending the LERR? command. See the CG635 Remote Programming chapter for information about the meaning of errors returned by the LERR? command.

The parameters R, N, D define the current state of the RF synthesizer. They satisfy the equation,

$$f_{DDS} = \frac{2^D R}{N} f_{OUT},$$

where f_{DDS} is frequency being output by the DDS chip, and f_{OUT} is the current output frequency.

The parameters FT3, FT2, FT1, and FT0 define the current frequency tuning word for the DDS chip. They satisfy the equation,

$$f_{DDS} = \frac{FT3 \times 65536^3 + FT2 \times 65536^2 + FT1 \times 65536 + FT0}{2^{64}} \times (M \times 20\text{MHz}),$$

where M is the DDS clock multiplier which is normally set to 5. See the Circuit Description chapter for more information about the operation of the RF synthesizer and DDS chip.

PRBS ON/OFF

If the PRBS option is installed, the PRBS ON function enables the PRBS output, and the PRBS OFF disables it. The CG635 will briefly display 'PRBS on' or 'PRBS off', respectively, when the functions are accessed.

If the PRBS option is not installed, the CG635 will briefly display 'no PRBS.'

The PRBS on/off state is saved when instrument settings are saved. If PRBS is installed, the current status (on/off/disabled) of the PRBS can viewed via the STATUS function. A status of 'disabled' indicates that the PRBS is requested on but disabled because the current frequency is too high.

FREQ/2, FREQx2

The functions FREQ/2 and FREQx2 cause the CG635 to decrease or increase the current frequency by a factor of two. They also force the CG635 to display frequency.

REL θ = 0

This function defines the current phase to be zero degrees. It does not affect the output. It also forces the CG635 to display phase.

θ + 90°

This function advances the current phase by 90°. It also forces the CG635 to display phase.

GPIB

This function enables the GPIB remote interface and disables the RS-232 remote interface. The CG635 will briefly display 'Enabled' after enabling the interface. This function is not executed until the user presses 'Hz'. The GPIB LED in the INTERFACE section of the front panel will be on when GPIB is the selected interface.

ADDRS

This function sets the CG635's primary GPIB address. The user can enter an address using the numeric keys or the MODIFY ▲ and ▼ keys. The address is not set until the user presses the 'Hz' key. For example, to set the GPIB address to 23, press the keys 'SHIFT', 'ADDRS', '2', '3', 'Hz' sequentially. The CG635 will briefly display 'Changed' if the address changes.

The factory default GPIB address is 23.

RS-232

This function enables the RS-232 remote interface and disables the GPIB remote interface. The CG635 will briefly display 'Enabled' after enabling the interface. This function is not executed until the user presses 'Hz'. The RS-232 LED in the INTERFACE section of the front panel will be on when RS-232 is the selected interface. The communication parameters are fixed at: 9600 Baud rate, 8 Data bits, 1 Stop bit, No Parity, RTS/CTS Hardware Flow Control.

DATA

This function enables the user to see the most recent characters received by the CG635 over the remote interface. The characters are shown in hexadecimal format, with older characters appearing to the left and newer characters appearing to the right. The last character received is marked with the decimal point showing.

To move back and forth through the buffer, use the MODIFY ▲ and ▼ keys.

Factory Default Settings

The factory default settings are listed in Table 15. The CG635 may be forced to assume its factor default settings by power cycling the unit with the 'BACK SPACE' key depressed. The INIT secondary function and the *RST remote command reset all but the communication parameters back to factory default settings.

Table 15: Factory Default Settings

Parameter	Setting
Frequency	10 MHz
Frequency step size	1 Hz
Phase	0°
Phase step size	1°
Q / $\overline{Q}$ high	1.43 V (LVDS)
Q / $\overline{Q}$ high step size	0.1 V
Q / $\overline{Q}$ low	1.07 V (LVDS)
Q / $\overline{Q}$ low step size	0.1 V
CMOS high	3.3 V (+3.3 V CMOS)
CMOS high step size	0.1 V
CMOS low	0.0 V (+3.3 V CMOS)
CMOS low step size	0.1 V

PRBS	Off
Run/stop state	Running
Display	Frequency
Display on/off state	On
Enabled remote interface	RS-232
GPIB address	23
Power-on Status Clear (*PSC)	1

Troubleshooting

The CG635 does not include any user serviceable parts inside. The line fuse is internal to the instrument and may not be serviced by the user. In the event of instrument failure, refer service to a qualified technician.

The CG635 performs several instrument tests during startup. The tests are described in Table 16. In most cases the unit will have to be repaired by a qualified technician if the unit fails one of these tests.

Table 16: Power-On Self Tests

Test	Description	Test Fail Symptoms
ROM	ROM checksum	Flash memory is corrupted. Unit may behave unpredictably
1	24V Power	Power supply is not providing stable 24 volts.
2	19.44 MHz tuning	The crystal can't tune to ±100 ppm. The CG635 may not be able to lock at all frequencies.
3	19.40 MHz tuning	The crystal can't tune to ±100 ppm. The CG635 may not be able to lock at all frequencies.
4	RF VCO	The VCO can't tune from 960MHz to 2.05 GHz. The CG635 may not be able to lock at all frequencies.
5	CMOS output	The CG635 is unable to drive the front-panel CMOS output to the correct voltage. Check that the output is not connected to a voltage source.
6	Q / $\overline{Q}$ outputs	The CG635 is unable to drive the Q / $\overline{Q}$ outputs to the correct voltages. Check that the outputs are terminated into 50 Ω and not connected to a voltage source.
7	Clock symmetry	Output duty cycle is not 50 %. Output driver is likely damaged.
8	Option detection	Optional oscillator is installed, but not oscillating. The CG635 will use its internal oscillator.

Table 17 contains a list of troubleshooting tips for various symptoms which may occur in a normally functioning unit. Please consult this list before contacting SRS regarding a potential instrument failure.

Table 17: Troubleshooting Tips

Symptom	Resolution
STOP LED flashing and output not oscillating	Output is in stopped state. To put back into running state, sequentially press ‘SHIFT’, ‘RUN’
CMOS output not oscillating	The front-panel CMOS output is forced to a low state at frequencies above 250 MHz. Try setting the frequency below 250 MHz.
RS-485 output not oscillating	The rear panel RS-485 output is disabled above 105 MHz. Try setting the frequency below 105 MHz.
PRBS outputs not functioning	Make sure PRBS is enabled. Press ‘SHIFT’, ‘PRBS ON’ to enable. The PRBS is also disabled above 1.55 GHz. Try setting the frequency below 1.55 GHz.
UNLK LED flashes once a second	An optional rubidium oscillator is installed but it is not yet stable. Wait 10 minutes to give the rubidium time to warm up and stabilize.
No GPIB communication	Check that GPIB communication is enabled. Sequentially press ‘SHIFT’, ‘GPIB’, ‘Hz’. Also check that the GPIB address is set correctly. See the ADDRS secondary function.
No RS-232 communication	Check that RS-232 communication is enabled. Sequentially press ‘SHIFT’, ‘RS-232’, ‘Hz’. Also check that the communication parameters are set to 9600 baud, 8 bits, no parity, one stop bit and RTS/CTS hardware flow control. When connecting to a PC, make sure you are using a standard PC serial cable, not a “null-modem” cable.
Doesn’t respond to key presses and REM LED is on	The CG635 has been placed in remote mode by the GPIB bus. Press ‘STEP SIZE’ to put the CG635 back into local mode.
ERR LED flashes	The CG635 has received characters over the remote interface, but the command parser has determined that the command is invalid. Check the command syntax and make sure you are appending a command terminator.

CG635 Remote Programming

Introduction

The CG635 may be remotely programmed via the standard GPIB interface or the RS-232 serial interface. Any host computer interfaced to the CG635 can easily control and monitor the operation of the CG635.

GPIB

The CG635 comes with an IEEE 488 standard port for communicating over GPIB. The port is located on the rear panel of the CG635.

This interface is enabled via the front panel by pressing the keys 'SHIFT', 'GPIB', 'Hz'. The primary GPIB address of the instrument is also set via the front panel by pressing the keys 'SHIFT', 'ADDRS', MODIFY ▲ or ▼, 'Hz'. Valid GPIB addresses range from 0 to 30. Enabling the GPIB interface causes the RS-232 interface to be disabled. The GPIB LED in the INTERFACE section of the front panel will be on when GPIB is the selected interface.

The factory default GPIB address is 23.

RS-232

The CG635 comes standard with an RS-232 communications port. The port is located on the rear panel of the CG635.

The RS-232 interface connector is a standard 9 pin, type D, female connector configured as a DCE (transmit on pin 3, receive on pin 2). The communication parameters are fixed at: 9600 Baud rate, 8 Data bits, 1 Stop bit, No Parity, RTS/CTS Hardware Flow Control. This interface is enabled via the front panel by pressing the keys 'SHIFT', 'RS-232', 'Hz'. Enabling the RS-232 interface causes the GPIB interface to be disabled. The RS-232 LED in the INTERFACE section of the front panel will be on when RS-232 is the selected interface.

Front-Panel Indicators

To assist in programming, the CG635 has four front panel indicators located under the INTERFACE section: RS-232, GPIB, ACT, and ERR. The RS-232 LED is on when the CG635 is configured to accept commands over RS-232. The GPIB LED is on when the CG635 is configured to accept commands over GPIB. The ACT LED serves as an activity indicator that flashes every time a character is received or transmitted over one of the remote interfaces. The ERR LED will flash when a remote command fails to execute due to illegal syntax or invalid parameters.

Command Syntax

Communications with the CG635 is done with ASCII characters. All commands are 4-characters long and are case-insensitive. Standard IEEE-488.2 defined commands begin with the '*' character followed by three letters. CG635 specific commands are composed of four letters.

The four-letter mnemonic (shown in CAPS) in each command sequence specifies the command. The rest of the sequence consists of parameters.

Commands may take either *set* or *query* form, depending on whether the '?' character follows the mnemonic. *Set only* commands are listed without the '?', *query only* commands show the '?' after the mnemonic, and *optionally query* commands are marked with a '(?)'.

Parameters shown in { } and [ ] are not always required. Parameters in { } are required to set a value, and are omitted for queries. Parameters in [ ] are optional in both set and query commands. Parameters listed without any surrounding characters are always required.

Do NOT send () or {} or [] or spaces as part of the command.

The command buffer is limited to 255 bytes, with 25 byte buffers allocated to each of up to three parameters per command. If the command buffer overflows, both the input and output buffers will be flushed and reset. If a parameter buffer overflows, a command error will be generated and the offending command discarded.

Commands are terminated by either a semicolon, a <CR> (ASCII 13), or a <LF> (ASCII 10). If the communications interface is GPIB, then the terminating character may optionally be accompanied by an EOI signal. If the EOI accompanies a character other than a <LF>, a <LF> will be appended to the command to terminate it. Execution of the command does not begin until a command terminator is received.

Aside from communication errors, commands may fail due to either syntax or execution errors. Syntax errors can be detected by looking at bit 5 (CME) of the event status register (*ESR?). Execution errors can be detected by looking at bit 4 (EXE) of the event status register. In both cases, an error code, indicating the specific cause of the error, is appended to the error queue. The error queue may be queried with the LERR? command. Descriptions of all error codes can be found in the Error Codes section starting on page 43.

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Instrument Control Commands

CMOS(?) i,{j} **CMOS Output**

Set (query) the i^{th} component of the CMOS output {to j}.

The parameter i selects the CMOS component.

i	Value
0	CMOS low voltage
1	CMOS high voltage

Example

CMOS 1, 2.5<CR> Set CMOS high to 2.5 volts.
CMOS?0<CR> Query CMOS low voltage.

DISP(?){i} **Display**

Set (query) the current display value {to i}.

The parameter i selects the display type.

i	Display
0	Frequency
1	Phase
2	Q / $\overline{Q}$ high
3	Q / $\overline{Q}$ low
4	CMOS high
5	CMOS low
6	Frequency step
7	Phase step
8	Q / $\overline{Q}$ high step
9	Q / $\overline{Q}$ low step
10	CMOS high step
11	CMOS low step

The query form returns –1 if the current display does not correspond to one of the standard displays. This might occur, for example, if one of the status displays were active.

FREQ(?){i} **Frequency**

Set (query) the frequency {to i}.

PHAS(?){i} **Phase**

Set (query) the phase {to i}. Note that this command is executed as an overlapped operation. If necessary, use *OPC or *WAI to determine when the operation is complete.

PRBS(?){i} **Enable PRBS**

Set (query) the PRBS enabled state {to i}. If i is 0, PRBS is disabled. If i is 1, PRBS is enabled.

QOUT(?) i,{j} **Q / $\overline{Q}$ Output**

Set (query) the i^{th} component of the Q / $\overline{Q}$ output {to j}.

The parameter i selects the Q / $\overline{Q}$ component.

i	Value
0	Q / $\overline{Q}$ low voltage
1	Q / $\overline{Q}$ high voltage

Example

QOUT 1, 2.1<CR> Set Q / $\overline{Q}$ high voltage to 2.1 volts.
QOUT?0<CR> Query Q / $\overline{Q}$ low voltage.

RPHS **Relative Phase**

Define the current phase to be zero degrees. This command does not affect the output.

RUNS(?){i} **Running State**

Set (query) the running state of outputs {to i}. If i is 0, the outputs are in the stopped state. RUNS 0 stops the output and also sets stop level low. If i is 1, the output is not stopped.

SHDP(?){i} **Show Display**

Set (query) the current state of the display. If i is 0, the display is turned off. If i is 1, the display is turned on.

SLVL(?){i} **Stop Level**

Set (query) the level at the output in the stopped state {to i}. If i is 0, the stop level is low. If i is 1, the stop level is high. If i is set to 2, the stop level is toggled.

STDC(?){i} **Standard CMOS**

Set (query) the CMOS output {to i}.

The parameter i selects the standard level.

i	Standard CMOS Level
0	1.2 V standard CMOS
1	1.8 V standard CMOS
2	2.5 V standard CMOS
3	3.3 V standard CMOS
4	5.0 V standard CMOS

The query form returns –1 if the current levels do not correspond to one of the standard levels. This indicates that the VAR LED is on.

STDQ(?){i} **Standard Q / $\overline{Q}$**

Set (query) the Q / $\overline{Q}$ outputs {to i}.

The parameter i selects the standard level.

i	Standard Q / $\overline{Q}$ Level
0	ECL levels (–1.00/–1.80 V)
1	+7 dBm levels (+0.50/–0.50 V)
2	LVDS levels (1.43/1.07 V)
3	PECL 3.3 V levels (2.30/1.50 V)
4	PECL 5.0 V levels (4.00/3.20 V)

The query form returns 1 if the current levels do not correspond to one of the standard levels. This indicates that the VAR LED is on.

STPD i — **Step Down**

Step down the ith component.

The parameter i selects the component to step.

i	Value
0	Step the frequency
1	Step the phase
2	Step Q / $\overline{Q}$ high
3	Step Q / $\overline{Q}$ low
4	Step CMOS high
5	Step CMOS low

STPS(?) i,{j} — **Step Size**

Set (query) the i^{th} step size {to j}.

The parameter i selects the component.

i	Value
0	Frequency step size in Hz
1	Phase step size in degrees
2	Q / $\overline{Q}$ high step size in volts
3	Q / $\overline{Q}$ low step size in volts
4	CMOS high step size in volts
5	CMOS low step size in volts

Example

STPS 1,2.0<CR> Set the phase step size to 1 degree.
STPS?0<CR> Query the frequency step size.

STPU i — **Step Up**

Step up the ith component.

The parameter i selects the component to step.

i	Value
0	Step the frequency
1	Step the phase
2	Step Q / $\overline{Q}$ high
3	Step Q / $\overline{Q}$ low
4	Step CMOS high
5	Step CMOS low

TIMB? — **Timebase**

Query the current timebase for the CG635.

The returned value identifies the timebase.

Value	Meaning
0	Internal timebase
1	OCXO timebase
2	Rubidium timebase
3	External timebase

UNIT(?) i,{j} — **Units Display**

Set (query) the units for display value {to j}.

The parameter i selects the item.

i	Display Item
0	Frequency
1	Frequency Step

The parameter j selects the units.

j	Display
0	Hz
1	kHz
2	MHz
3	GHz

Interface Commands

***IDN?** — **Identification String**

Query the instrument identification string.

Example

*IDN?<CR> Returns a string similar to 'Stanford Research Systems,CG635,s/n004025,ver0.01'

***OPC(?)** — **Operation Complete**

The set form sets the OPC flag in the ESR register when all prior commands have completed. The query form returns '1' when all prior commands have completed, but does not affect the ESR register.

***RCL i** — **Recall Instrument Settings**

Recall instrument settings from location i. The parameter i may range from 0 to 10. Locations 0 to 9 are for arbitrary use. Location 10 is reserved for the instrument's current settings. This location is automatically updated 60 seconds after the user presses any key that modifies the current state of the instrument. The following settings are recalled:

1. Current frequency and frequency step size.
2. Current phase and phase step size.
3. Q / $\overline{Q}$ high and low levels and step sizes.
4. CMOS high and low levels and step sizes.
5. Current display selection.
6. PRBS on/off state
7. Run/stop state
8. Stop level

The display will be turned on when settings are recalled.

Example

*RCL 3<CR> Recall instruments settings from location 3.

***RST** — **Reset the Instrument**

Reset the instrument to default settings. This is equivalent to pressing the keys 'SHIFT', 'INIT', 'Hz' on the front panel. The factory default settings are listed in Table 15. . The remote interface, GPIB address, and power-on status clear are not affected by this command, however.

Example

*RST<CR> Resets the instrument to default settings

***SAV i** — **Save Instrument Settings**

Save instrument settings to location i. The parameter i may range from 0 to 10. Locations 0 to 9 are for arbitrary use. Location 10 is reserved for the instrument's current settings. This location is automatically updated ten seconds after the user presses any key that modifies the current state of the instrument. The following settings are saved:

1. Current frequency and frequency step size.
2. Current phase and phase step size.

3. Q / $\overline{Q}$ high and low levels and step sizes.
4. CMOS high and low levels and step sizes.
5. Current display selection.
6. PRBS on/off state
7. Run/stop state
8. Stop level

Example

*SAV 3<CR> Save current settings to location 3.

---

*TST? Self Test

Runs the instrument self test and returns 0 if successful and 72 (EXE_FAIL_SELF_TEST) if unsuccessful. If unsuccessful, the error buffer will include device dependent errors related to the parts of the self test that failed.

Example

*TST?<CR> Run the instrument self test and return the result.

---

*WAI Wait for Command Execution

The instrument will not process further commands until all prior commands including this one have completed.

Example

*WAI<CR> Wait for all prior commands to execute before continuing.

Status Reporting Commands

***CLS** — **Clear Status**

Clear Status immediately clears the ESR, CESR, LCKR, and INSR registers as well as the LERR error buffer.

***ESE(?){i}** — **Standard Event Status Enable**

Set (query) the standard event status enable register {to i}. Bits set in this register cause ESB in the serial poll status byte to be set when the corresponding bit is set in the standard event status register.

***ESR?** — **Standard Event Status Register**

Query the standard event status register. The value returned is a decimal value from 0 to 255. After executing a *ESR? query, the register is cleared. See the Status Byte Definitions section for a description of each of the bits.

Example

*ESR?<CR>	A return of '176' would indicate that PON, CME, and EXE are set.

***PSC(?){i}** — **Power-on Status Clear**

Set (query) the Power-on Status Clear flag {to i}. The Power-on Status Clear flag is stored in nonvolatile memory in the CG635, and thus, maintains its value through power-cycle events.

If the value of the flag is 0, then the Service Request Enable and Standard Event Status Enable Registers (*SRE, *ESE) are stored in non-volatile memory, and retain their values through power-cycle events. If the value of the flag is 1, then these two registers are cleared upon power-cycle.

Example

*PSC 1<CR>	Set the Power-on Status Clear to 1.
*PSC?<CR>	Returns the current value of Power-on Status Clear.

***SRE(?){i}** — **Service Request Enable**

Set (query) the Service Request Enable register {to i}. Bits set in this register cause the CG635 to generate a service request when the corresponding bit is set in the serial poll status register.

***STB?** — **Serial Poll Status Byte**

Query the standard IEEE 488.2 serial poll status byte. The value returned is a decimal value from 0 to 255. Reading this byte has no effect on its value. See the Status Byte Definitions section for a description of each of the bits.

Example

*STB?<CR>	A return of '114' would indicate that LCKB, MAV, ESB, and MSS are set. LCKB indicates that an enabled bit in LCKR is set. MAV indicates that a message is available in the output queue. ESB indicates that an enabled bit in ESR is set. MSS reflects the fact that at least one of the summary bits is set.

CESE(?){i} **Communication Error Status Enable**

Set (query) the communications error status enable register {to i}. Bits set in this register cause CESB in the serial poll status byte to be set when the corresponding bit is set in the communications error status register (CESR).

CESR? **Communication Error Status Register**

Query the communications error status register. The value returned is a decimal value from 0 to 255. After executing a CESR? query, the register is cleared. See the Status Byte Definitions section for a description of each of the bits.

Example

CESR?<CR> A return of '24' would indicate that OR and OVFL bits are set. OR indicates that a character was received over RS-232 before the microcontroller had time to process the previous character. OVFL indicates that the input buffer overflowed.

INSE(?){i} **Instrument Status Enable**

Set (query) the instrument status enable register {to i}. Bits set in this register cause INSB in the serial poll status byte to be set when the corresponding bit is set in the instrument status register (INSR).

INSR? **Instrument Status Register**

Query the instrument status register. The value returned is a decimal value from 0 to 255. After executing a INSR? query, the register is cleared. See the Status Byte Definitions section for a description of each of the bits.

Example

INSR?<CR> A return of '4' would indicate that an eeprom write failed.

LCKE(?){i} **PLL Lock Status Enable**

Set (query) the PLL lock status enable register {to i}. Bits set in this register cause LCKB in the serial poll status byte to be set when the corresponding bit is set in the PLL lock status register (LKCR).

LCKR? **PLL Lock Status Register**

Query the PLL lock status register. The value returned is a decimal value from 0 to 255. After executing a LCKR? query, the register is cleared. See the Status Byte Definitions section for a description of each of the bits.

Example

LCKR?<CR> A return of '3' would indicate that the RF PLL and the 19 MHz PLL have come unlocked.

LERR? **Last Error**

Query the last error in the error buffer. After executing a LERR? query, the returned error is removed from the error buffer. See the Error Codes section later in this chapter for a description of the possible error codes returned by LERR?. The error buffer has space to store up to 20 errors. If more than 19 errors occur without being queried, the 20th error will be 254 (Too Many Errors) indicating that errors were dropped.

Status Byte Definitions

The CG635 reports on its status by means of the serial poll status byte and four event status registers: the standard event status (*ESR), the communication error status (CESR), the PLL lock status (LCKR), and the instrument event status (INSR). These read-only registers record the occurrence of defined events inside the CG635. If the event occurs, the corresponding bit is set to one. Bits in the status registers are latched. Once an event bit is set, subsequent state changes do not clear the bit. Bits are cleared when the registers are queried, with a *ESR?, for example. The bits are also cleared with the clear status command, *CLS. The bits are not cleared, however, with an instrument reset (*RST) or a device clear.

Each of the CG635's four event status registers has an associated enable register. The enable registers control the reporting of events in the serial poll status byte (*STB). If a bit in the event status register is set and its corresponding bit in the enable register is set, then the summary bit in the serial poll status byte (*STB) will be set. The enable registers are readable and writable. Reading the enable registers or clearing the status registers does not clear the enable registers. Bits in the enable registers must be set or cleared explicitly. To set bits in the enable registers, write an integer value equal to the binary weighted sum of the bits you wish to set.

The serial poll status byte (*STB) also has an associated enable register called the service request enable register (*SRE). This register functions in a similar manner to the other enable registers, except that it controls the setting of the master summary bit (bit 6) of the serial poll status byte. It also controls whether the CG635 will issue a request for service on the GPIB bus.

Serial Poll Status Byte

Bit	Name	Meaning
0	INSB	An unmasked bit in the instrument status register (INSR) has been set.
1	LCKB	An unmasked bit in the PLL lock status register (LCKR) has been set.
2	CESB	An unmasked bit in the communications status register (CESR) has been set.
3	Reserved	
4	MAV	The interface output buffer is non-empty.
5	ESB	An unmasked bit in the standard event status register (*ESR) has been set.
6	MSS	Master summary bit. Indicates that the CG635 is requesting service because an unmasked bit in this register has been set.
7	Reserved	

The serial poll status byte may be queried with the *STB? command. The service request enable register (*SRE) may be used to control when the CG635 asserts the request-for-service line on the GPIB bus.

Standard Event Status Register

Bit	Name	Meaning
0	OPC	Operation complete. All previous commands have completed. See command *OPC.
1	Reserved	
2	QYE	Query error occurred.
3	DDE	Device dependent error.
4	EXE	Execution error. A command failed to execute correctly because a parameter was out of range.
5	CME	Command error. The parser detected a syntax error
6	Reserved	
7	PON	Power on. The CG635 has been power cycled.

The standard event status register may be queried with the *ESR? command. The standard event status enable register (*ESE) may be used to control the setting of the ESB summary bit in the serial poll status byte.

Communication Error Status Register

Bit	Name	Meaning
0	PE	Parity error. An RS-232 parity error was detected.
1	FE	Framing error. An RS-232 framing error was detected.
2	NF	Noise flag. An RS-232 character may have been received incorrectly due to noise on the line.
3	OR	Overrun error. An RS-232 character was received before the CG635 had time to process the previous character.
4	OVFL	The input buffer of the CG635 overflowed.
5	NL	The CG635 was addressed to talk under GPIB, but there were no listeners.
6	Reserved	
7	DCAS	Device clear active state. The CG635 received a device clear or selected device clear command.

The communication error status register may be queried with the CESR? command. The communication error status enable register (CESE) may be used to control the setting of the CESB summary bit in the serial poll status byte.

Instrument Status Register

Bit	Name	Meaning
0	EE_BDRY	Eeprom write occurred outside of eeprom.
1	EE_PROT	Eeprom write occurred in protected eeprom.
2	EE_VERF	Eeprom write failed to verify.
3	CMF_RESET	A clock-monitor-fail reset has occurred.
4	COP_RESET	A COP-timeout reset has occurred.
5	ILGL_RESET	An illegal-instruction reset has occurred.
6	RB_COMM	An installed rubidium oscillator failed to communicate.
7	Reserved	

The instrument status register may be queried with the INSR? command. The instrument status enable register (INSE) may be used to control the setting of the INSB summary bit in the serial poll status byte.

PLL Lock Status Register

Bit	Name	Meaning
0	RF_UNLOCK	The RF PLL has come unlocked.
1	19MHZ_UNLOCK	The 19 MHz PLL has come unlocked.
2	10MHZ_UNLOCK	The 10 MHz PLL has come unlocked.
3	RB_UNLOCK	The optional rubidium oscillator has come unlocked.
4	OUT_DISABLED	The output was disabled.
5	PHASE_SHIFT	The output has or is scheduled to shift phase.
6	Reserved	
7	Reserved	

The PLL lock status register may be queried with the LCKR? command. The PLL status enable register (LCKE) may be used to control the setting of the LCKB summary bit in the serial poll status byte.

Error Codes

The CG635 contains an error buffer that may store up to 20 error codes associated with errors encountered during power-on self tests, command parsing, or command execution. The errors in the buffer may be read one by one by executing successive LERR? commands. The meaning of each of the error codes is described below.

Execution Errors

0 **No Error**

No more errors left in the queue.

10 **Illegal Value**

A parameter was out of range.

20 **Frequency Error**

The frequency or frequency step size was illegal.

30 **Phase Error**

The phase step size was illegal.

31 **Phase Step Error**

The phase could not be set because it would have caused a phase step larger than 360°.

40 **Voltage Error**

The voltage could not be set because it was out of range.

51 **Q / $\overline{Q}$ Low Changed**

Q / $\overline{Q}$ high was set to the requested value, but Q / $\overline{Q}$ low was also changed in order to satisfy the Q / $\overline{Q}$ amplitude limits.

52 **Q / $\overline{Q}$ High Changed**

Q / $\overline{Q}$ low was set to the requested value, but Q / $\overline{Q}$ high was also changed in order to satisfy the Q / $\overline{Q}$ amplitude limits.

61 **CMOS Low Changed**

CMOS high was set to the requested value, but CMOS low was also changed in order to satisfy the CMOS amplitude limits.

62 **CMOS High Changed**

CMOS low was set to the requested value, but CMOS high was also changed in order to satisfy the CMOS amplitude limits.

71 **No PRBS**

PRBS could not be enabled because it's not installed.

72 **Failed Self Test**

The self test failed. The device dependent errors that caused the self test to fail will follow in the error buffer.

Query Errors

100 **Lost Data**

Data in the output buffer was lost. This occurs if the output buffer overflows, or if a communications error occurs and data in output buffer is discarded.

102 **No Listener**

This is a communications error that occurs if the CG635 is addressed to talk on the GPIB bus, but there are no listeners. The CG635 discards any pending output.

Parsing Errors

110 **Illegal Command**

The command syntax used was illegal. A command is normally a sequence of four letters, or a '*' followed by three letters.

111 **Undefined Command**

The specified command does not exist.

112 **Illegal Query**

The specified command does not permit queries

113 **Illegal Set**

The specified command can only be queried.

114 **Null Parameter**

The parser detected an empty parameter.

115 **Extra Parameters**

The parser detected more parameters than allowed by the command.

116 **Missing Parameters**

The parser detected missing parameters required by the command.

117 **Parameter Overflow**

The buffer for storing parameter values overflowed. This probably indicates a syntax error.

118 **Invalid Floating Point Number**

The parser expected a floating point number, but was unable to parse it.

120 **Invalid Integer**

The parser expected an integer, but was unable to parse it.

122 **Invalid Hexadecimal**

The parser expected hexadecimal characters, but was unable to parse them.

126 **Syntax Error**

The parser detected a syntax error in the command.

Device Dependent Errors

151 **Failed ROM Check**

The ROM checksum failed. The firmware code is likely corrupted.

152 **Failed 24 V Out of Range**

The CG635 24 V power is out of range.

153 **Failed 19.44 MHz Low Rail**

The 19.44 MHz crystal can not tune to low enough frequencies.

154 **Failed 19.44 MHz High Rail**

The 19.44 MHz crystal can not tune to high enough frequencies.

155 **Failed 19.40 MHz Low Rail**

The 19.40 MHz crystal can not tune to low enough frequencies.

156 **Failed 19.40 MHz High Rail**

The 19.40 MHz crystal can not tune to high enough frequencies.

157 **Failed RF at 2 GHz**

The RF VCO could not tune to 2 GHz.

158 **Failed RF at 1 GHz**

The RF VCO could not tune to 1 GHz.

159 **Failed CMOS Low Spec.**

The CMOS low output is out of specification.

160 **Failed CMOS High Spec.**

The CMOS high output is out of specification.

161 **Failed Q / $\overline{Q}$ Low Spec.**

The Q / $\overline{Q}$ low output is out of specification.

162 **Failed Q / $\overline{Q}$ High Spec.**

The Q / $\overline{Q}$ high output is out of specification.

163 **Failed Optional Timebase**

An installed optional timebase is not oscillating.

164 **Failed Clock Symmetry**

The clock output symmetry is out of specification

Other Errors

254 **Too Many Errors**

The error buffer is full. Subsequent errors have been dropped.

Performance Evaluation

Overview

The performance of a CG635 may be evaluated by running a series of tests designed to measure the accuracy of its inputs and outputs and comparing the results with their associated specifications. While the performance tests presented here are not as extensive as the tests performed at the factory, one can nevertheless have confidence that a unit that passes these tests is functioning properly and within specification.

The performance tests can be divided into three broad categories: output driver tests, frequency synthesis tests, and timebase calibration tests. The output driver tests are designed to test the integrity and accuracy of the front panel outputs by measuring the accuracy with which its levels are generated and the speed with which it transitions between levels. The frequency synthesis tests are designed to measure the stability of the frequency synthesis by measuring the phase noise and jitter at specified frequencies. Overall functionality is verified by measuring the frequency generation at various points in the spectrum from DC to 2.05 GHz. Lastly, the timebase calibration tests evaluate the accuracy and stability of the installed timebase.

Equipment Required

In addition to the CG635 under test, the following equipment will be required to carry out the performance tests:

- Agilent 34401A digital multimeter
- HP 54120A digitizing oscilloscope with HP 54121A four channel input module
- CG646 +7 dBm RF receiver module
- FS725 rubidium frequency standard
- HP 89440A spectrum analyzer
- SR620/SR625 time interval counter (SR625 needed to test to 2 GHz)

Equivalent equipment may be substituted as desired as long as they have similar or superior specifications. Standard SMA and BNC cables will be required to connect the test equipment to the CG635. Additionally accessories required include, 50 Ω terminators for the CG635's high frequency outputs and 20 dB DC to 18 GHz SMA attenuators for the HP 54121A inputs.

CG635 Self Test

The CG635 includes a self test that checks the functional operation of several internal components. If any of the tests fail, the CG635 will briefly display "Failed" after the test. The tests are described in Table 16. In most cases the unit will have to be repaired by a qualified technician if the unit fails one of these tests.

Table 18: Power-On Self Tests

Test	Description	Test Fail Symptoms
ROM	ROM checksum	Flash memory is corrupted. Unit may behave unpredictably
1	24V Power	Power supply is not providing stable 24 volts.
2	19.44 MHz tuning	The crystal can't tune to ±100 ppm. The CG635 may not be able to lock at all frequencies.
3	19.40 MHz tuning	The crystal can't tune to ±100 ppm. The CG635 may not be able to lock at all frequencies.
4	RF VCO	The VCO can't tune from 960MHz to 2.05 GHz. The CG635 may not be able to lock at all frequencies.
5	CMOS output	The CG635 is unable to drive the front-panel CMOS output to the correct voltage. Check that the output is not connected to a voltage source.
6	Q / $\overline{Q}$ outputs	The CG635 is unable to drive the Q/$\overline{Q}$ outputs to the correct voltages. Check that the outputs are terminated into 50 Ω and not connected to a voltage source.
7	Clock symmetry	Output duty cycle is not 50 %. Output driver may be damaged.
8	Option detection	Optional oscillator is installed, but not oscillating. The CG635 will use its internal oscillator.

The CG635 self test is automatically executed at power-on. It may also be executed by sending the command ***TST?** over the remote interface. If the unit passes it will return 0 over the remote interface. If it fails, it will return 72. Refer to the user guide for more information about communicating with the CG635 over a remote interface.

Output Level Tests

The output level tests are intended to test the accuracy and integrity of the CG635 output drivers. They test the accuracy of the DC voltage levels at each of the supported communication standards. They also test the speed with which transitions between levels occurs.

Q/$\overline{Q}$ Level Tests

The Q/$\overline{Q}$ ouput level tests require the setup shown in Figure 4.

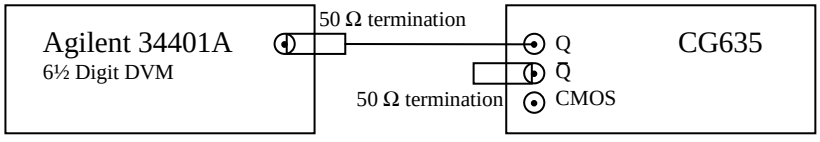

Figure 4: Q/$\overline{Q}$ output level test setup

The Q/$\overline{Q}$ outputs should be terminated into 50 Ω. The terminator connected to the Agilent DVM should be accurate to 1%. To test the Q output, configure the CG635 as follows:

1. Press 'SHIFT', 'INIT', 'Hz' to return the CG635 to default settings.

2. Press the Q/$\overline{Q}$ ▲ and ▼ buttons to select the communication standard under test.
3. Press 'SHIFT', 'STOP' to stop the clock outputs at a low level.
4. Record V_{low} as reported by the DVM.
5. Press 'SHIFT', 'TOGGLE', 'SHIFT' to toggle the clock outputs to a high level.
6. Record V_{high} as reported by the DVM.

The recorded values (V_{low}, V_{high}) should fall between the minimum and maximum values listed in Table 19 for each standard level.

Table 19: Minimum and Maximum allowed values for the Q/$\overline{Q}$ outputs

Output	Min. (Low, High) V	Measured (Low, High) V	Max. (Low, High) V
ECL	(–1.828, –1.020)		(–1.772, –0.980)
+7 dBm	(–0.515, 0.485)		(–0.485, 0.515)
LVDS	(1.049, 1.406)		(1.091, 1.454)
PECL 3.3V	(1.475, 2.267)		(1.525, 2.333)
PECL 5V	(3.158, 3.950)		(3.242, 4.050)

To test the $\overline{Q}$ output, configure the CG635 as in Figure 4, except swap the connections to Q and $\overline{Q}$. Repeat the steps above except record V_{high} in step 4 and record V_{low} in step 6.

CMOS Level Tests

The CMOS output level tests require the setup shown in Figure 5.

Figure 5: CMOS output level test setup

To test the CMOS output, configure the CG635 as follows:

1. Press 'SHIFT', 'INIT', 'Hz' to return the CG635 to default settings.
2. Press the CMOS ▲ and ▼ buttons to select the communication standard under test.
3. Press 'SHIFT', 'STOP' to stop the clock outputs at a low level.
4. Record V_{low} as reported by the DVM.
5. Press 'SHIFT', 'TOGGLE', 'SHIFT' to toggle the clock outputs to a high level.
6. Record V_{high} as reported by the DVM.

The recorded values (V_{low}, V_{high}) should fall between the minimum and maximum values listed in Table 20 for each standard level.

Table 20: Minimum and Maximum allowed values for the CMOS output

Output	Min. (Low, High) V	Measured (Low, High) V	Max. (Low, High) V
1.2 V	(–0.044, 1.156)		(0.044, 1.244)
1.8 V	(–0.056, 1.744)		(0.056, 1.856)
2.5 V	(–0.070, 2.430)		(0.070, 2.570)
3.3 V	(–0.086, 3.214)		(0.086, 3.386)
5.0 V	(–0.120, 4.880)		(0.120, 5.120)

Transition Time Measurements

The 20 % to 80 % output transition times of the CG635 are tested using the HP 54120A Digitizing Oscilloscope with HP 54121A four channel input module. Configure the setup as in Figure 6.

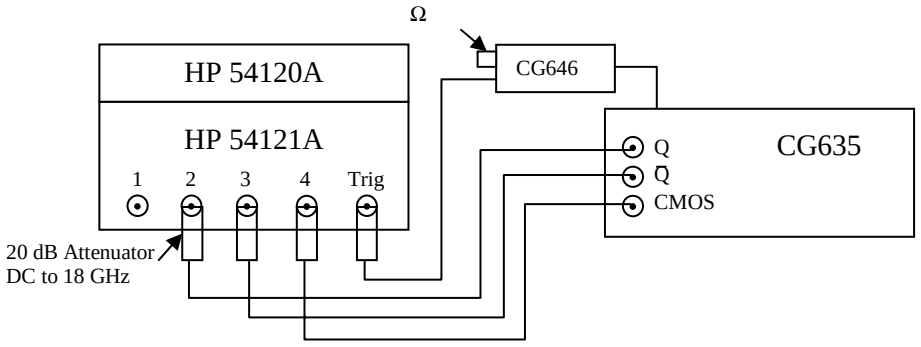

Figure 6: Transition time measurement setup

Connect 20 dB attenuators to the inputs of the HP 54121A. Use short, equal length SMA cables with SMA to BNC adaptors to connect the CG635 to the HP 54121A.

Setup the CG635 as follows:

1. Press ‘SHIFT’, ‘INIT’, ‘Hz’ to return the CG635 to default settings.
2. Press the Q/$\overline{Q}$ ▼ button to select +7 dBm output level for the Q/$\overline{Q}$ outputs
3. Press the CMOS ▲ button to select +5.0 V output levels for the CMOS output
4. Press ‘FREQ’, ‘2’, ‘0’, ‘0’, ‘MHz’ to set the frequency to 200 MHz.

The same CG635 configuration is used for both the Q/$\overline{Q}$ output timing measurements and the CMOS output timing measurements.

Q/$\overline{Q}$ Timing Measurements

For Q/$\overline{Q}$ timing measurements, configure the HP 54120A digitizing scope as in Table 21.

Table 21: HP 54120A digitizing scope setup for Q/$\overline{Q}$ timing

Parameter	Setting
Trigger	0.0V level, positive slope, HF sens. off, HF reject off
Trig. Slope	Positive
Volts/div	20 mV for channel 2 and 3
Offset	0.0 V for channel 2 and 3
Time/div	50 ps
Delay	Reference at center, value adjusted to center transition in the display
Display	Channels 2 and 3, averaged with count of 4
V Markers	Marker 1: –30 mV Marker 2: +30 mV
T Markers	Start Marker: adjusted to time where Q/$\overline{Q}$ waveform crosses V Marker 1 Stop Marker: adjusted to time where Q/$\overline{Q}$ waveform crosses V Marker 2

The scope delay will have to be adjusted manually until the transitions from the 200 MHz output are located. Once the delay is properly adjusted to center the transition on the display, the complementary transition can be readily obtained by adding 2.5 ns to the delay.

Measure the rise-time by adjusting the T Markers so that the Start Marker is located at the point where the waveform crosses V Marker 1 and the Stop Marker is located at the point where the waveform crosses V Marker 2. Record the Δt of the markers as the rise time of the given waveform.

Measure the fall-time by adjusting the T Markers so that the Start Marker is located at the point where the waveform crosses V Marker 2 and the Stop Marker is located at the point where the waveform crosses V Marker 1. Record the Δt of the markers as the fall time of the given waveform.

The rise-time of Q and the fall-time of $\overline{Q}$ can be measured at one delay setting. The rise-time of $\overline{Q}$ and the fall-time of Q can be measured at a reference delay that is 2.5 ns later.

The measured transition times should meet the specifications given in Table 22.

Table 22: Maximum allowed transition times for Q/$\overline{Q}$ outputs

Output	Meas. (Rising, Falling) ps	Max. (Rising, Falling) ps
Q		(100, 100)
$\overline{Q}$		(100, 100)

CMOS Timing Measurements

For the CMOS output timing measurements, configure the HP 54120A digitizing scope as in Table 23.

Table 23: HP 54120A digitizing scope setup for CMOS timing

Parameter	Setting
Trigger	0.0V level, positive slope, HF sens. off, HF reject off
Trig. Slope	Positive
Volts/div	50 mV for channel 4
Offset	125 mV for channel 4
Time/div	200 ps
Delay	Reference at center, value adjusted to center transition in the display
Display	Channel 4, averaged with count of 4
V Markers	Marker 1: 50 mV Marker 2: 200 mV
T Markers	Start Marker: adjusted to time where waveform crosses V Marker 1 Stop Marker: adjusted to time where waveform crosses V Marker 2

The scope delay will have to be adjusted manually until the rising edge of the CMOS output transition from the 200 MHz output is located. Once the delay is properly adjusted to center the transition on the display, the falling edge transition can be readily obtained by adding 2.5 ns to the delay.

Measure the rise-time by adjusting the T Markers so that the Start Marker is located at the point where the waveform crosses V Marker 1 and the Stop Marker is located at the point where the waveform crosses V Marker 2. Record the Δt of the markers as the rise-time of the given waveform.

Add 2.5ns to the reference delay to center the falling edge transition in the display. Measure the fall-time by adjusting the T Markers so that the Start Marker is located at the point where the waveform crosses V Marker 2 and the Stop Marker is located at the point where the waveform crosses V Marker 1. Record the Δt of the markers as the fall-time of the given waveform.

The measured transition times should meet the specifications given in Table 24.

Table 24: Maximum allowed transition times for CMOS output

Output	Meas. (Rising, Falling) ps	Max. (Rising, Falling) ps
CMOS		(1000, 1000)

Frequency Synthesis Tests

Basic functionality of the CG635 is verified by testing the generation of several specific frequencies from DC to 2 GHz. This ensures that all the dividers are working properly. Overall stability of the CG635 is tested by measuring the phase noise, jitter, and wander at a couple of specific frequencies. The test points ensure that both crystals used in the frequency generation are operating at specification. At the factory, we use a proprietary mixer and filter which allows us to measure the jitter directly with a voltmeter. Here we provide an alternative method which should provide equivalent results.

Functional Tests

Functional tests verify that basic frequency synthesis of the CG635 is operating correctly. This is accomplished by measuring the frequency of the CG635 at several specific frequencies from DC to 2 GHz. The SR620 time interval counter is used to measure the frequency output from the CG635. An SR625 is required to measure frequencies from 1 GHz to 2 GHz.

SR620/SR625 Configuration

Use the following procedure to set up the SR620/SR625:

1. With the power off hold down the 'CLR' button in the DISPLAY section and turn the power on. This resets the SR620 to default settings.
2. Press MODE ▼ button three times to switch the mode from TIME to FREQ.
3. Press the GATE/ARM ▲ button two times to switch the gate to 1 s.
4. Press the SAMPLE SIZE ▼ button three times to set the sample size to 1.
5. Press DISPLAY ▼ button five times to set the display to TRIG.
6. Adjust the channel A trigger knob until the trigger level displayed for channel A reads 0.00.
7. Press the DISPLAY ▲ button five times to set the display back to MEAN.
8. Press the channel A 'AC/DC' button once to switch to AC coupling
9. Press the channel A 'INPUT' button once to switch to 50 Ω termination.
10. For frequency measurements between 100 MHz and 1 GHz, press the channel A 'INPUT' button once more to switch to 50 Ω termination with UHF prescalers.

CG635 Configuration

Use the following procedure to configure the CG635 for frequency measurements:

1. Press 'SHIFT', 'INIT', 'Hz' to return the CG635 to default settings.
2. Press the Q/$\overline{Q}$ ▼ button to select +7 dBm output level for the Q/$\overline{Q}$ outputs.
3. For each frequency, use the number pad to enter in the desired frequency and complete the entry with the appropriate units button.

Frequencies 1.0 to 2.0 GHz

Measuring frequencies above 1.3 GHz with the SR620 requires the UHF divide by 10 prescalers that come with an SR625. Use the setup shown in Figure 7.

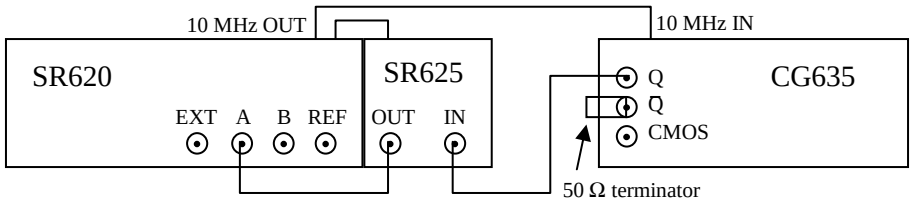

Figure 7: Setup for frequency measurements from 1.0 to 2.0 GHz.

The SR625 prescaler has a level adjustment knob. Adjust the level until the SR620 reports frequencies that are 1/10 of the set frequency. Set the frequency of the CG635 to

each value given in Table 25. Record the frequency measured by the SR620. The actual frequency is 10 times the reported frequency. Verify that the measured frequency is within the limits specified in Table 25.

Table 25: Test frequencies from 1.0 to 2.0 GHz

Set Freq. (GHz)	Min Freq. (Hz)	Measured Freq. (Hz)	Max Freq (Hz)
1.0	999,999,999.0		1,000,000,001.0
1.1	1,099,999,999.0		1,100,000,001.0
1.2	1,199,999,999.0		1,200,000,001.0
1.3	1,299,999,999.0		1,300,000,001.0
1.4	1,399,999,999.0		1,400,000,001.0
1.5	1,499,999,999.0		1,500,000,001.0
1.6	1,599,999,999.0		1,600,000,001.0
1.7	1,699,999,999.0		1,700,000,001.0
1.8	1,799,999,999.0		1,800,000,001.0
1.9	1,899,999,999.0		1,900,000,001.0
2.0	1,999,999,999.0		2,000,000,001.0

Frequencies 100 MHz to 1.0 GHz

The SR620 can measure frequencies below 1.0 GHz directly. Use the setup shown in Figure 8 for frequencies from 100MHz to 1.0 GHz. Configure the SR620 as described above. Make sure that the channel A input has the UHF prescaler activated.

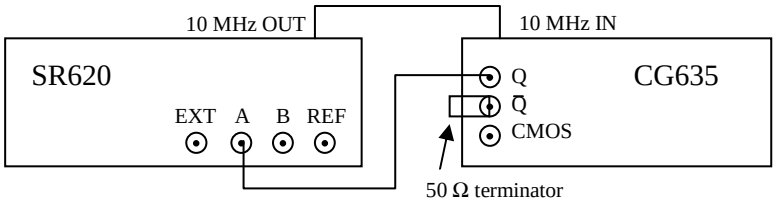

Figure 8: Setup for frequency measurements below 1.0 GHz.

Set the frequency of the CG635 to each value given in Table 26. Record the frequency measured by the SR620. Verify that the measured frequency is within the limits specified in Table 26.

Table 26: Test frequencies from 100 MHz to 1.0 GHz

Set Freq. (MHz)	Min Freq. (Hz)	Measured Freq. (Hz)	Max Freq (Hz)
100.0	99,999,999.0		100,000,001.0
200.0	199,999,999.0		200,000,001.0
300.0	299,999,999.0		300,000,001.0
400.0	399,999,999.0		400,000,001.0
500.0	499,999,999.0		500,000,001.0
600.0	599,999,999.0		600,000,001.0
700.0	699,999,999.0		700,000,001.0
800.0	799,999,999.0		800,000,001.0
900.0	899,999,999.0		900,000,001.0
1000.0	999,999,999.0		1,000,000,001.0

Frequencies Below 100 MHz

For frequencies below 100 MHz use the setup shown in Figure 8 again. Also use the same SR620 configuration except make sure the channel A UHF prescaler is not activated. Set the frequency of the CG635 to each value given in Table 27. Record the frequency measured by the SR620. Verify that the measured frequency is within the limits specified in Table 27.

Table 27: Test frequencies below 100 MHz

Set Freq. (MHz)	Min Freq. (Hz)	Measured Freq. (Hz)	Max Freq (Hz)
0.1	99,999.999		100,000.001
0.2	199,999.999		200,000.001
0.5	499,999.999		500,000.001
1.0	999,999.999		1,000,000.001
2.0	1,999,999.990		2,000,000.010
5.0	4,999,999.990		5,000,000.010
10.0	9,999,999.990		10,000,000.010
20.0	19,999,999.900		20,000,000.100
50.0	49,999,999.900		50,000,000.100
100.0	99,999,999.900		100,000,000.100

Time Modulation Test

The time modulation test verifies that the time modulation input on the rear panel of the CG635 is functioning properly. A voltage swing from –5 V to +5 V should modulate the phase of the output by 10 ns. Use the setup shown in Figure 9 to test the time modulation input.

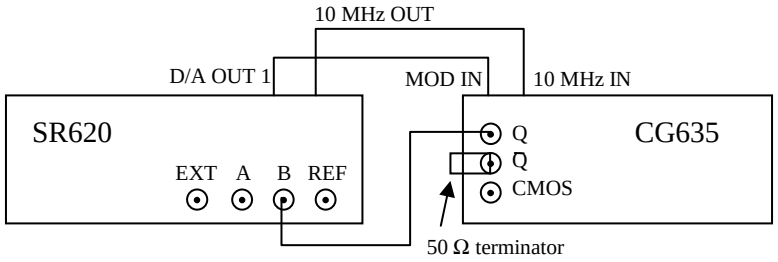

Figure 9: Setup for time modulation test.

CG635 Configuration

Use the following procedure to configure the CG635 for the time modulation test:

1. Press ‘SHIFT’, ‘INIT’, ‘Hz’ to return the CG635 to default settings.
2. Press the Q/$\bar{Q}$ ▼ button to select +7 dBm output level for the Q/$\bar{Q}$ outputs.

Time Modulation Test Procedure

Perform the following steps on the SR620 to test the time modulation input:

1. With the power off hold down the 'CLR' button in the DISPLAY section and turn the power on. This resets the SR620 to default settings.
2. Press SOURCE button two times to switch the start pulse to REF.
3. Press the SAMPLE SIZE ▲ button six times to set the sample size to 1000.
4. Press DISPLAY ▼ button five times to set the display to TRIG.
5. Adjust the channel B trigger knob until the trigger level displayed for channel B reads 0.00.
6. Press the DISPLAY ▲ button five times to set the display back to MEAN.
7. Press the channel B 'AC/DC' button once to switch to AC coupling
8. Press the channel B 'INPUT' button once to switch to 50 Ω termination.
9. Press 'SEL' in the CONFIG section until "SCN" is flashing
10. Press 'SET' in the CONFIG section until "DA Src chrt chrt" is displayed
11. Press SAMPLE SIZE ▼ once to change the display to "DA Src dac chrt". This configures the D/A output 1 to be sourced by the dac.
12. Press 'SET' in the CONFIG section once to display "DA 0.000 ---.---"
13. Press SAMPLE SIZE ▼ and ▲ to adjust the DAC voltage to –5.00 V.
14. Press DISPLAY ▲ to view the mean time interval.
15. Press 'SET' in the DISPLAY section to start showing relative measurements.
16. Press 'SET' in the CONFIG section until the display shows "DA –5.000 ---.---"
17. Press SAMPLE SIZE ▼ and ▲ to adjust the DAC voltage to +5.00 V.
18. Press DISPLAY ▲ to view the mean time interval.
19. Record the absolute value of the time interval as T_{mod}

T_{mod} should meet the specifications given in Table 28.

Table 28: Time Modulation Specification

Voltage Swing	Min Mod. (ns)	Measured Mod. (ns)	Max Mod. (ns)
10 V	9.5		10.5

Phase Noise Tests

When making phase noise measurements, it is critical that the reference clock have superior stability to that of the device under test. Use the setup shown in Figure 10 to measure phase noise and jitter. Note that since the CG635 is locked to the FS725, this setup will test the noise of the synthesizer alone, independent of the internal timebase.

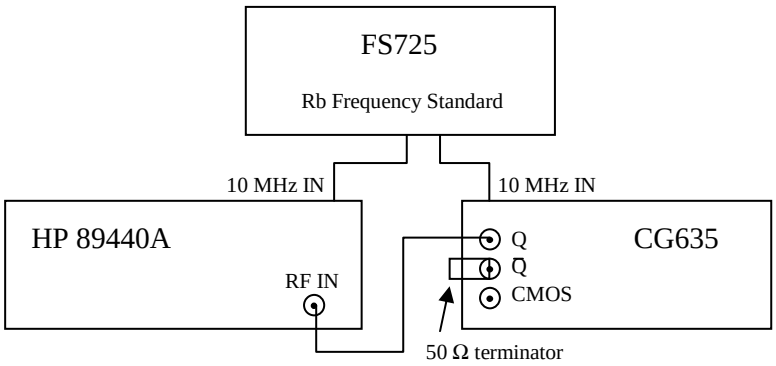

Figure 10: Setup for phase noise and jitter tests.

CG635 Configuration

Use the following procedure to configure the CG635 for the phase noise test:

1. Press 'SHIFT', 'INIT', 'Hz' to return the CG635 to default settings.
2. Press the Q/$\overline{Q}$ ▼ button to select +7 dBm output level for the Q/$\overline{Q}$ outputs.
3. Use the numeric key pads to enter the test frequency and press the appropriate units key to complete the entry.

HP 89440A Configuration

First press the 'Preset' key to force the unit to default settings. Then enter the settings detailed in Table 29.

Table 29: HP 89440A configuration for phase noise tests

Key	Menu	2nd Menu	Setting
Instrument Mode	Inst Mode		Demodulation
	Demodulation Setup	Ch1 Result	PM
		Auto carrier	On
		PM auto type	Phase
Range	Ch1 range		10 dBm
Measurement Data	Meas Data		PSD
Average	Average		On
	Num averages		100
Frequency	Center		622.08 MHz *
	Span		400 Hz *
Marker	Enter marker position		100 Hz *

The settings marked with a * will change at each test point as specified in Table 30 below.

Phase Noise Test Procedure

At each test point identified in Table 30, set the CG635 to the given frequency. Then set the HP 89440A to the given center frequency, span, and marker position. Record S(f) reported by the HP 89440A at the marker position in units of dBradrms^2/Hz. Calculate the phase noise from S(f) using the equation L(f) = S(f) – 3dB. For example, if the HP reports that the noise at 100Hz offset is –91 dBradrms^2/Hz, then S(100) = –91 dBradrms^2/Hz. L(100) = S(100) – 3dB = –94 dB$_c$/Hz. The measured phase noise should be lower than the maximum phase noise specified in Table 30.

Table 30: Phase noise measurements

Frequency	Span	Marker	S(f)	L(f) = S(f) – 3dB	Max L(f) (dBc/Hz)
622.08 MHz	400 Hz	100 Hz			–90
	4 kHz	1 kHz			–100
	40 kHz	10 kHz			–100
	400 kHz	100 kHz			–110
620.80 MHz	400 Hz	100 Hz			–90
	4 kHz	1 kHz			–100
	40 kHz	10 kHz			–100
	400 kHz	100 kHz			–110

Jitter Tests

The CG635's jitter can be inferred from its phase noise spectrum. Use the same setup shown in Figure 10 to measure jitter. Use the HP 89440A band power markers to measure the integrated rms noise of the spectrum. The CG635's jitter is specified in a bandwidth from 1 kHz to 5 MHz. The HP 89440A does not have adequate bandwidth to measure out to 5 MHz. However, the spectrum of the noise from the CG635 is flat from 1 MHz to 5 MHz. Therefore, the jitter can be approximated by assuming that the rms noise in the band from 1 MHz to 5 MHz is equal to 2 times the measured rms noise in the band from 1 MHz to 2 MHz.

At SRS we use a proprietary mixer and filter that automatically filters the output to the appropriate bandwidth and measures the rms jitter directly. The procedure given here, however, should give a reasonable approximation of the jitter.

HP 89440A Configuration

First press the 'Preset' key to force the unit to default settings. Then enter the settings detailed in Table 31.

Table 31: HP 89440A configuration for jitter tests

Key	Menu	2nd Menu	Setting
Instrument Mode	Inst Mode		Demodulation
	Demodulation Setup	Ch1 Result	PM
		Auto carrier	On
		PM auto type	Phase
Range	Ch1 range		10 dBm
Measurement Data	Meas Data		PSD
Average	Average		On
	Num averages		100
Frequency	Center		622.08 MHz *
	Span		4 MHz
Marker function	Band power markers	Band pwr mkr	On
		Units	Rms sqrt (pwr)
		Band width	1 MHz
		Band center	500 kHz *

The settings marked with a * will change depending on the frequency under test and the band being measured. Take measurements at the frequencies and bands given in Table 32. For band 0 to 1 MHz, set the band center to 500 kHz and record the measured noise as N_0. For band 1 to 2 MHz, set the band center to 1.5 MHz and record the noise as N_1.

Table 32: Jitter noise measurements

Frequency	0 to 1 MHz N_0	1 to 2 MHz N_1	Rms Noise N_T	Jitter (ps) N_J	Max Jitter (ps)
622.08 MHz					1
620.80 MHz					1

Calculate the rms noise, N_T, using the equation $N_T = (N_0^2 + 4N_1^2)^{1/2}$ Calculate the rms jitter, N_J, from the rms noise using the equation $N_J = N_T/2\pi F$, where F is the carrier frequency.

For example, if N_0 = 2.3 mradrms and N_1 = 0.66 mradrms and F = 620.80 MHz, then

$N_T = (2.3^2 + 4\times0.66^2)^{1/2} = 2.65$ mradrms

and

$N_J = 2.65\times10^{-3}/(2\times3.14\times620.80\times10^6) = 0.68$ ps.

The calculated jitter should be less than the maximum allowed jitter specified in Table 32.

Timebase Calibration

The accuracy of the internal timebase may be tested against a house reference if it is known that the house reference has a superior stability and accuracy than the timebase installed in the CG635. Use the setup shown in Figure 11 to test the accuracy of the timebase.

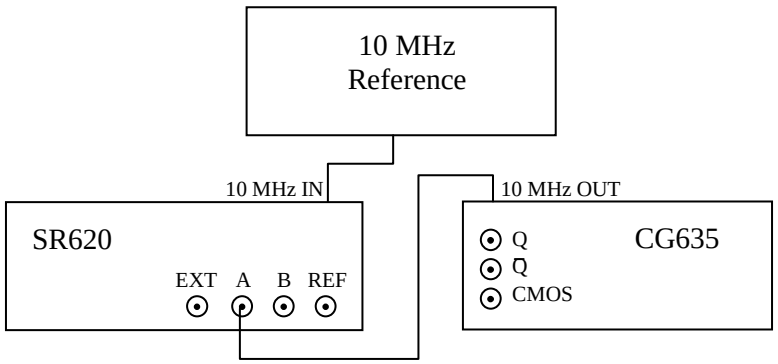

Figure 11: Setup for timebase calibration

The accuracy and stability of the CG635 timebase depends on the type of timebase installed. An optional timebase, if installed, can be identified on the rear panel of CG635 under the serial number as Option 2, OCXO timebase, or Option 3, Rubidium timebase.

If the standard timebase or OCXO is installed, an FS725 Rb frequency standard may be used as the 10 MHz reference. If a rubidium timebase is installed, a cesium based reference will be required as a reference.

SR620 Configuration

Use the following procedure to set up the SR620:

1. With the power off hold down the ‘CLR’ button in the DISPLAY section and turn the power on. This resets the SR620 to default settings.

2. Press ‘SEL’ in the CONFIG section until “CAL” is flashing
3. Press ‘SET’ in the CONFIG section until “cloc Source” is displayed
4. Press SCALE▲ in the SCOPE AND CHART section until “cloc Source rear” is displayed
5. Press MODE ▼ button until the selected mode is FREQ.
6. Press ‘SEL’ in the CONFIG section until “OUT” is flashing
7. Press ‘SET’ in the CONFIG section until “Gate Scale” is displayed
8. Press SCALE▲ in the SCOPE AND CHART section until 100 is displayed.
9. Press the DISPLAY ▲ to return to the normal display
10. Press the GATE/ARM ▲ button once to set the gate to 10 s
11. If a rubidium timebase is installed in the CG635, press the GATE/ARM ▲ button once more to set the gate to 100 s
12. Press the SAMPLE SIZE ▼ button three times to set the sample size to 1.
13. Turn the trigger level knob above the channel A input counter clockwise until AUTO is highlighted.
14. Press the channel A ‘INPUT’ button once to switch to 50 Ω termination.

Timebase Calibration Test

It is critical that the timebase be fully warmed up before measurements are taken. Allow at least 1 hour of warm-up for an OCXO or Rubidium timebase. Allow at least 30 minutes of warm-up for a standard timebase.

Record the timebase frequency reported by the SR620 and compare it to the stated one-year accuracy shown in Table X for the installed timebase.

Table 33: Timebase calibration test

Timebase	Min Freq. (Hz)	Measured Freq. (Hz)	Max Freq (Hz)
Standard	9,999,950.000,000		10,000,050.000,000
Opt 2: OCXO	9,999,998.000,000		10,000,002.000,000
Opt 3: Rubidium	9,999,999.995,000		10,000,000.005,000

Calibration

The CG635’s internal timebase may be calibrated using the measurements taken above if communication over a remote interface is enabled. The process is iterative. Send the query **TCAL?** to get the current value of the cal byte. If the measured frequency is low, this number should be increased, otherwise it should be decreased. Send a new value by sending the command **TCAL dddd**, where dddd is the new 4 digit cal byte. After sending the new cal byte, measure the frequency again and continue iterating until calibration is achieved to the desired accuracy.

Circuit Description

Overview

The CG635 Synthesized Clock Generator was designed with several goals in mind:

1. Generation of square wave clocks from 1 µHz to 2050 MHz
2. Very high frequency resolution for long-term phase stability
3. Very low phase noise
4. Low cost

The design benefits from several frequency synthesis techniques while avoiding the pitfalls of those same techniques. For example, the design uses direct digital synthesis (DDS) for unlimited frequency resolution while avoiding the high spurs associated with DDS. The design also employs dual-modulus synthesis without suffering from the high phase noise that often accompanies high resolution (i.e., close channel spacing) designs.

The CG635 was primarily designed to provide convenient clock sources for the testing and operation of digital circuits and systems. Clock frequencies of up to 2.05 GHz may be synthesized. However, the high accuracy, high resolution, and low phase noise of the synthesized clock source will recommend its use in more esoteric tasks such as signal heterodyning, bit error rate and network synchronization testing.

Accuracy

The frequency accuracy depends on the accuracy of the internal timebase. The standard timebase is a 20 MHz crystal oscillator which provides an aging of <5 ppm per year. The 20 MHz timebase may be phase locked to an optional internal timebase or to an external 10 MHz source. Option 2, an ovenized crystal oscillator, provides an aging of <0.2 ppm per year, while Option 3, a rubidium frequency standard, provides an aging of <0.0005 ppm per year.

Resolution

The frequency resolution of the CG635 is determined by the frequency resolution of the DDS frequency synthesizer used in the system. The CG635 uses a 48-bit DDS; however the frequency resolution is extended to 64 bits by frequency-shift keying (FSK) the least significant bit (LSB) of the DDS with a duty factor with 16 bits of resolution. With this, the fractional frequency resolution is about $1 : 3.58 \times 10^{18}$ providing an edge drift rate of about 4.4 ps/year relative to a source with infinite resolution.

Phase Noise

Phase noise pitfalls are carefully avoided. The phase noise is essentially the multiplied up (or divided down) phase noise of a fundamental mode, AT-cut crystal oscillator.

Typical results are –130 dBc/Hz at 1 kHz offset from a 10 MHz carrier, or –95 dBc/Hz at 1 kHz offset from a 622.08 MHz carrier.

Circuit Block Diagram

A block diagram of the frequency synthesizer for the CG636 Synthesized Clock Generator is shown on the first page of the schematic diagrams: CG_BLK_D. A description of this diagram follows.

Timebase

The timebase for the synthesizer is a 20 MHz VCXO. The circuit uses a 20 MHz, 3rd overtone, AT-cut crystal. The VCXO will be phase locked to an external 10 MHz reference if applied; otherwise, a digital-to-analog converter (DAC) provides an analog voltage to calibrate the 20 MHz timebase. The 20 MHz timebase is used as a frequency reference for the DDS which follows.

Reference Synthesizer

A 48-bit DDS uses the 20 MHz timebase as a reference to generate a frequency near (i.e., within ±100 ppm) either 19,400,000 Hz or 19,440,000 Hz. The output of the DDS synthesizer is used as a frequency reference for the RF synthesizer after being cleaned up by a phase locked VCXO. The DDS has a clock multiplier which increases the frequency sample clock by 5× to 100 MHz. The output frequency of the DDS is given by the equation,

$$f_{DDS} = \text{sample clock} \times FTW / 2^{64} = 100\ \text{MHz} \times FTW / 2^{64}$$

or

$$FTW = f_{DDS} \times 2^{64} / 100\ \text{MHz}$$

The frequency resolution of the DDS is extended to 64 bits by toggling between a 48-bit frequency tuning word (FTW) of k and k+1 with a duty factor that has 16 bits of resolution.

The output of the DDS is low-pass filtered and converted to a square wave by a high speed comparator. While the in-close phase noise of this reference is very good, there is a thick forest of spurious components in the broadband spectrum below –80 dBc. These spurs must be eliminated in order for the frequency reference to be useful for synthesizing an RF output.

Reference Synthesizer Clean-up

The frequency reference from the DDS is "cleaned-up" by one of two VCXOs. One of the VCXOs (either the 19,400,000 Hz VCXO or the 19,440,000 Hz VCXO) is selected (by a procedure to be detailed later) and loosely phase locked to the DDS output. The natural frequency of this PLL is only a few Hertz, and so the VCXO will not pass spurs more than a few Hertz away from the carrier. The VCXO can lock to input frequencies with a capture range of at least ±100 ppm (±1944 Hz). The output of the VCXO provides a spur-free reference frequency to the RF synthesizer which follows.

Time Modulation

The output from the selected VCXO is converted to a triangle ramp and applied to the input of a high speed comparator. The external "time modulation" input is applied to the other input of the comparator, allowing the external modulation source to linearly delay or advance the transitions at the output of the comparator. Since the RF synthesizer phase locks the RF VCO to the reference, the RF VCO timing will follow the modulation applied to the reference (up to the bandwidth of the RF PLL.)

RF Synthesizer

A dual-modulus RF frequency synthesizer is used to phase lock a 960-2050 MHz VCO to the cleaned-up DDS reference. The RF frequency synthesizer divides the DDS reference by a factor "R" ($1 \le R \le 16{,}383$), divides the VCO frequency by a factor "N" ($40 \le N \le 65591$ with the restriction that $N \neq 46$, 47 or 55…more on this quirky numerology later), and compares the divided frequencies with a phase/frequency detector. (The phase comparison frequency will be the DDS frequency / R.) The output of the phase/frequency detector operates a charge pump which in turn controls the frequency of the VCO to achieve phase lock.

For a low phase noise output, it is important that the R & N divisors be as small as possible; the instrument's output phase noise can be no better than the dividers' and phase detector's phase noise floor (typically –159 dBc/Hz at 1 MHz) multiplied up from the phase comparison frequency to the output frequency. (The output phase noise will suffer 20 dB phase noise degradation per decade of frequency between the phase comparison frequency and the output frequency.)

The R & N dividers are determined by enumeration, starting with R=1 and determining if there is an N value that will provide the desired output frequency from a reference of 19,400,000 Hz ± 100 ppm or 19,440,000 Hz ± 100 ppm. Computer enumeration shows that the average R value is 8 and no R value larger than 26 is required to synthesize any frequency. (The R values with two VCXOs are about four times lower than they would be with just one VCXO. The R values would be smaller if the tuning range of the VCXOs was larger.)

A low pass filter (with a bandwidth that is decreased as the R divider is increased) filters the dual modulus synthesizer's phase detector output. The output of the filter controls the VCO which can operate over the range of 960-2050 MHz.

Programmable Dividers and Clock Fan-out

A high speed (>2 GHz) digital divider is used to scale the 960-2050 MHz clock to lower frequencies. There are fifty-one, overlapping octave bands to span the frequency range between 1 µHz and 2.05 GHz. If a new output frequency is specified, the firmware will attempt to stay within the same octave band. If an octave switch is required, however, and the frequency is in one of the first eleven octave bands, the output will go to a low state until the VCO has settled, and then the output will be re-enabled in a "runtless" fashion.

Table 34: CG635's Fifty-one, Overlapping Octave Bands

Band	Divider	Min Frequency (Hz)	Max Frequency (Hz)
0	1	960,000,000	2,050,000,000
1	2	480,000,000	1,024,000,000
2	4	240,000,000	512,000,000
3	8	120,000,000	256,000,000
4	16	60,000,000	128,000,000
5	32	30,000,000	64,000,000
6	64	15,000,000	32,000,000
7	128	7,500,000	16,000,000
8	256	3,750,000	8,000,000
9	512	1,875,000	4,000,000
10	1024	937,500	2,000,000
11	2048	468,750	1,000,000
…	…	…	…
49	2^{49}	0.000,001,705,302	0.000,003,637,978
50	2^{50}	0.000,000,852,651	0.000,001,818,989

For frequencies in bands eleven to fifty, the CG635 uses DDS technology to seamlessly change dividers. Since no spurious pulses are generated, the output is not disabled.

Determining Register Values

Definitions

f_R = 20 MHz timebase reference (which can be locked to an external 10 MHz)

f_{DDS} = DDS synthesizer output frequency (±100 ppm of 19.40 MHz or 19.44 MHz)

f_{VCXO} = VCXO frequency (±100 ppm of 19.40 MHz or 19.44 MHz)

f_U = upper tuning limit of f_{VCXO} (100 ppm above f_M)

f_M = nominal f_{VCXO} frequency (19,400,000 Hz or 19,440,000 Hz)

f_L = lower tuning limit of f_{VCXO} (100 ppm below f_M)

f_C = phase detector comparison frequency

f_{VCO} = RF VCO frequency

f_O = output frequency

M = DDS clock multiplier (5×)

FTW = 64-bit DDS frequency tuning word

R = reference divider for dual modulus synthesizer. $1 \le R \le 16{,}383$

N = VCO divider for dual modulus synthesizer. $N = B \times P + A$ with $A \le B$ and $P=8$

D = output divider = 2^n where $0 \le n \le 50$

Calculations

Referring to the schematic diagram CG_BLK_C, the output frequency is given by:

$$f_O = [\{ f_R \times M \times FTW / 2^{64} \} \times N / R] / D$$

Where the term: $\{ f_R \times M \times FTW / 2^{64} \} = f_{DDS}$ which has the restriction that $f_L \le f_{DDS} \le f_U$ (so that the VCXO can lock to the DDS.)

Given the desired output frequency (f_O) the procedure to find all of the parameters (D, R, N and FTW) is:

1. Use Table 34 to determine the output divider, "D". If possible, stay within the current band (i.e., use the current value for D).
2. Compute the required RF VCO frequency: $f_{VCO} = f_O \times D$.
3. Find the lowest values for R & N (by enumeration, starting with R=1, and given that $f_{VCO} \approx f_M \times N / R$) so that the desired f_{VCO} can be generated consistent the restriction that $f_L \le f_{VCXO} \le f_U$ (This loop is carried out for f_M = 19,400,000 Hz and 19,440,000 Hz. The first iteration to satisfy the loop conditions determines which VCXO will be selected.)
    a. Start with R=1
    b. Compute the nearest $N = INT(0.5 + f_{VCO} \times R / f_M)$
    c. If N = 46, 47 or 55 (disallowed values) increment R and go to (b.)
    d. Compute the required $f_{VCXO} = f_{VCO} \times R / N$
    e. Test if the computed f_{VCXO} satisfies the condition $f_L \le f_{VCXO} \le f_U$
    f. If the test fails, increment R and go to (b.)
    g. Parse N into A & B registers: $B = INT(N/8)$ & $A = N - 8 \times B$

h. Compute the FTW for the DDS with 64+ bits of resolution (rounding to the nearest integer value): FTW = $f_O \times D \times R \times 2^{64} / (f_R \times M \times N)$

Example

A specific example: Synthesizer parameters to generate 750 MHz.

1. As 750 MHz lies between 480 MHz and 1024 MHz, using Table 1 we select an output divider D = 2.

2. We compute $f_{VCO} = f_O \times D = 1500$ MHz

3. Enumeration for R & N for f_M = 19,400,000 Hz is shown in the table below:

R (try)	Nearest N	Required VCXO(MHz)	VCXO tuning (ppm)
1	77	19.48051948	4150
2	155	19.35483871	–2328
3	232	19.39655172	–178
4	309	19.41747573	901
5	387	19.37984496	–1039
6	464	19.39655172	–178
7	541	19.40850277	438
8	619	19.38610662	–716
9	696	19.39655172	–178
10	773	19.40491591	253
11	851	19.38895417	–569
12	928	19.39655172	–178
13	1005	19.40298507	154
14	1082	19.40850277	438
15	1160	19.39655172	–178
16	1237	19.4017785	92

4. Enumeration for R & N for f_M = 19,440,000 Hz is shown in the table below:

R (try)	Nearest N	Required VCXO(MHz)	VCXO tuning (ppm)
1	77	19.48051948	2084
2	154	19.48051948	2084
3	231	19.48051948	2084
4	309	19.41747573	–1159
5	386	19.43005181	–512
6	463	19.43844492	–80

5. The first table shows that R=16 and N=1237 allows us to generate 750 MHz with the VCXO running 92 ppm above its nominal value.

6. The second table shows that R=6 and N=463 allows us to generate 750 MHz with the VCXO running 80 ppm below its nominal value.

7. The value from the second table is preferred, as the lower N value will provide a lower phase noise, and so the 19,440,000 Hz VXCO will be selected. The phase comparison frequency in the RF PLL will be about 3.23 MHz.

8. For N=463, N = 8 × B + A, so the B counter will be loaded with 57 and the A counter will be loaded with 7.

9. Finally, compute the DDS frequency tuning word:

$$FTW = f_O \times D \times R \times 2^{64} / (f_R \times M \times N)$$

$$= 750{,}000{,}000 \times 2 \times 6 \times 2^{64} / (20{,}000{,}000 \times 5 \times 463)$$

$$\approx 3.58 \times 10^{18}$$

The top 48-bits of the FTW are sent to the DDS synthesizer and the 16 LSBs are used to control the FSK PWM. The FTW may only be correct to ½ LSB. This quantization error leads to a frequency setting error of about ½ part in 3.58×10^{18}, which would cause a phase drift of about 4.4 ps/year relative to an ideal source.

Typical values for the R divider

A program was written to find R & N divider values for output frequencies in the top band (960-2050 MHz). R & N dividers for the 1,090,000 frequencies spaced by 10 kHz (10 ppm) were computed and statistics were complied. The following results were obtained with available VCXO frequencies of 19,400,000 Hz and 19,440,000 Hz (with a tuning range of ±100 ppm): $R_{min} = 1$, $R_{mean} = 8.02$ and $R_{max} = 26$. About 99.9% of the computed R dividers were ≤ 20. The maximum R value of 26 provides a phase comparison frequency of 747 kHz, where the phase noise floor of the dual modulus synthesizer is typically –159 dBc/Hz. If this comparison frequency is being used to generate an output frequency 1,000 × higher (i.e. at 747 MHz), one would expect an output phase noise of approximately –159+60 = –99 dBc/Hz.

Phase adjustment

The CG635 allows the phase of the output to be viewed and adjusted from the front panel or via the computer interface. Since the output edges are phase locked to the internal DDS edges, output edges will move by the same amount of *time* as the DDS edges. Therefore, the instrument can adjust the phase of its output by adjusting the timing of the DDS edges.

The user enters a phase change in *degrees* and the instrument computes a corresponding *time* change. For example, if the user requests a 90º phase change for an output at 622.08 MHz this corresponds to a time delay of:

$$\Delta T = (1/622.08 \times 10^6) \times (90^o / 360^o) \approx 401.877 \text{ ps}$$

So, delaying the DDS edges by 401.877 ps will cause a 90º phase shift of a 622.08 MHz output. In contrast, if the user requests a phase change of 360° for a 1 MHz output, the DDS edges would have to be moved by 1 µs.

While the DDS has the capability to do phase-shift-keying, it cannot adjust the phase of the output directly; instead, the edges of the DDS output will be moved by operating the DDS at a nearby frequency for a short period of time.

If the frequency tuning word (FTW) of the DDS is changed from its value by ΔFTW, and the DDS is operated at this new frequency for a time Δt_{pwm}, then the DDS edges will advance in time by:

$$\Delta T_{DDS} = (\Delta FTW/ FTW) \times \Delta t_{pwm}$$

There is an important restriction on the magnitude of ΔFTW/FTW: the DDS frequency change must not be so large as to cause the VCXO to come unlocked from the DDS. We will restrict ΔFTW/FTW to be less than ±10 ppm. This restriction requires a relatively *long* phase slew interval in order to achieve the desired time shift.

There is another restriction: we need to make sure that the quantization error on ΔT_{DDS} (due to the rounding in the calculation on the integer ΔFTW) does not significantly degrade the phase setting. Every cycle of the DDS (which occur at 100 MHz) may add up to ½ LSB of error to the 48-bit phase accumulator. This accumulating error degrades the accuracy with which we are setting the phase and so we must limit the number of times that the ½ LSB error sums into the phase. This restriction is accommodated by choosing a relatively *short* phase slew interval in order to limit the accumulated error.

Gratefully, there is an overlap between the *long* and the *short* restrictions on Δt_{pwm}. The Δt_{pwm} FSK pulse is generated by a single pulse from the microcontroller's PWM. The pulse generator uses a clock with a period of 25.6 µs (ECLK/128 or XTAL/256.) The pulse generator will be programmed to use 10 × D cycles of this clock to generate a Δt_{pwm} between 256 µs and 262,114 µs. (Recall D is the frequency synthesizer output divider and D=1, 2, 4…1024.)

Given this, we can look at two limiting cases: (1) the frequency de-tuning required to produce a phase step of 360° at 937.5 kHz (the largest phase step at the lowest frequency which is adjusted in this manner) and (2) the accumulated phase error for a phase step at 2.05 GHz given a ½ LSB error in the calculation of ΔFTW.

(1) The time delay required to phase shift 937.5 kHz by 360° is given by:

$$\Delta T_{DDS} = (1/937.5\times10^{3}) \approx 1.06666 \text{ µs (one period for 360°)}$$

At this frequency, the output divider D is 1024 and so Δt_{pwm} will be 262,114 µs. In order to slew by 1.06666 µs in an interval of 262,114 µs will require:

$$\Delta FTW/FTW = \Delta T_{DDS} / \Delta t_{pwm} = 1.06666 \text{ µs} / 262{,}114 \text{ µs} = 4.069476 \text{ ppm}$$

So we see that Δt_{pwm} is long enough to avoid having the VCXO come unlocked ($\Delta f \approx 4$ ppm), but not so long as to cause the user to grow impatient with the phase

change (0.26 s). Note that at the top of this frequency band (at 2 MHz) the required Δf for a 360° phase shift will be about 2 ppm.

(2) The accumulated phase error due to the rounding error in the computation of the integer ΔFTW at 2 GHz is equal to ½ LSB (max) × the number of DDS cycles during the phase slew. In the top octave, where D=1, the Δt_{pwm} will be 256 µs; hence, there are 100 MHz × 256 µs or 25,600 DDS cycles which can lead to a worst case phase error of 12,800 LSBs. This leads to a DDS output timing error of $12{,}800/2^{48}$ periods or 16.4 nanodegrees at 2 GHz, which is very small compared to the 1° display resolution.

This method of phase slewing is quite satisfactory for high output frequencies, but can take too long to execute at low frequencies. For example, a 360° phase shift at 1 Hz would require 200,000 s (more than two days!) to perform if the frequency offset is limited to 5 ppm. To overcome this restriction, output frequencies below 1 MHz are sourced by a CMOS divider whose output can be quickly phase shifted by the CPU. Phase shifts on outputs below 1 MHz can consist of two components: a small phase slew component (which, as detailed above, is always used from high frequency phase adjustments) and large phase jumps programmed into the CMOS divider.

Detailed Circuit Description

Note on reference designators: The hundreds digit of the reference designator indicates the schematic sheet number. For example, R200 is a resistor on Sheet 2 and U500 is an integrated circuit on Sheet 5.

Note on PECL logic: Most of the ECL logic used in this instrument is 100k series operated from a +3.3 VDC power supply. The "high" level is +2.28 VDC and the "low" level is +1.48 VDC, both of which follow the +3.3 VDC supply. An ECL output is customarily terminated with a 50 Ω resistor to a potential which is 2.0 V below the V_{cc} power (i.e., a 50 Ω resistor to +1.3 VDC.) Terminating both the Q & $\overline{Q}$ outputs on each device will reduce system noise and allows termination to a node connected to ground through the paralleled combination of a 50 Ω resistor and a 0.1 µF capacitor.

Timebase

Main Board, Schematic sheet "CG_MB1D"

The frequency reference for the CG635 Synthesized Clock Generator is a 20 MHz Colpitts oscillator. The oscillator's resonator (Y100) is a 3rd overtone AT-cut crystal designed to operate at 20 MHz with a 20 pF load. The load capacitance is the series combination of D100 (a dual varactor), C121 and C122 in parallel with L103. (The oscillator will not operate at the fundamental mode of the resonator as the parallel combination of C122 and L103 is inductive below 10.7 MHz.) Y100's load capacitance at 20 MHz is about 20 pF when the there is a reverse bias of 7 VDC across the dual varactor. The bias to the varactor is provided by either a calibration voltage from a 12-bit DAC or by a phase-lock loop (PLL) circuit if an external 10 MHz reference is applied or if an optional 10 MHz reference is installed.

The 20 MHz sine output from the oscillator is converted to TTL logic levels by U112, an AD8561 comparator. The 20 MHz square wave is used as the frequency reference for

the clock synthesizer. The 20 MHz is also divided down to 10 MHz by U113, a dual D-type flip-flop. One of the flip-flops, U113A, provides a 10 MHz clock for the microcontroller, for the GPIB interface controller, and a 10 MHz reference for phase-locking the 20 MHz timebase to a rear-panel 10 MHz input or to an optional 10 MHz reference oscillator (either an SC10 ovenized oscillator or a PRS10 rubidium frequency standard.) The differential outputs of the other flip-flop, U113B, drive a 10 MHz tank circuit (T101, 47 pF internal to T101, C126 & C127) and an output filter (C128, C129, C130 & L104) to provide a rear-panel 10 MHz sine wave output of 1.4 V_{pp} amplitude into a 50 Ω load via J101.

A rear-panel 10 MHz reference input is applied to a 10 MHz tank circuit (T100, 47 pF internal to T100 and in parallel with C101) via R100 and C100. The input impedance for frequencies much higher than 10 MHz is set by R100 (49.9 Ω) to provide a high return loss for high frequency noise. The tank operates as a 2:1 auto-transformer, reducing the amplitude of 10 MHz input by half and transforming the load (R101) by 4:1, so that the input impedance is about 1 kΩ at 10 MHz. The output of the tank is applied to U100, an AD8561 comparator. The comparator's inverting input is biased to +40 mV by R102 and R103 so that its non-inverting output is low in the absence of a user-applied 10 MHz reference input. When a 10 MHz signal is applied to the rear-panel timebase input, the comparator will generate a TTL square-wave. The low-pass filter (R107/C108) allows the microcontroller to measure the average value of this square wave via its A/D converter and so determine the presence of an external 10 MHz reference.

Another comparator (U102) is used to convert the 10 MHz sine wave from an optional internal timebase (either an SC10 ovenized oscillator or a PRS10 rubidium frequency standard) into TTL logic levels. The low-pass filter (R109/C109) allows the microcontroller to measure the average value of this square wave via its A/D converter and so determine the presence of an optional 10 MHz reference.

The microcontroller will phase lock the 20 MHz timebase to an external 10 MHz reference if one is supplied (by setting –EXT/OPT and DAC/-PLL low.) If no external reference is applied, but an optional reference is installed, the microcontroller will phase lock the 20 MHz timebase to the installed optional 10 MHz reference (by setting –EXT/OPT high and DAC/–PLL low.) If neither is present, the microcontroller will provide an analog voltage to the 20 MHz oscillator varactor via a 12-bit DAC to set the frequency of the 20 MHz timebase per the last calibration (by setting DAC/–PLL high.) The unused reference is gated "off" near the source (by U101 or U103) to avoid crosstalk between the references.

The PLL circuit consists of the phase/frequency detector (U106A, U106B and U107), a pre-filter (R111/C111 & R112/C112), and an integrating loop filter (U109A and surrounding R's and C's). The phase/frequency detector compares the phase of the selected reference (either external or optional) to the phase of the divided-by-two 20 MHz timebase. If the external (or optional) timebase leads in phase, then the output of the phase/frequency detector will cause the integrating loop filter to ramp upward, increasing voltage on the varactor (D100) and so increase the frequency of the 20 MHz timebase until it is brought in-phase with the selected reference.

Minimum pulse widths will be seen at the Q outputs of U106A/B when the PLL circuit achieves phase-lock. The pulse widths will be equal to the sum of the propagation delays through the OR gate (U107, 0.9-3.6 ns) and the flip-flops (U106, 1.0-5.4 ns). Meta-

stable resets are avoided by stretching the reset pulse with D101, C134 and R138. For propagation delay sums between 1.9 ns and 9 ns, and a period of 100 ns, the duty cycle of the 3.3 V pulse is between 1.9 % and 9.0 % leading to a voltage of 63 mV to 297 mV on the pre-filter outputs (10MHZ_LEAD and 10MHZ_LAG.) Hence the criteria for phase lock of the 20 MHz timebase to an external or optional frequency reference is that 10MHZ_LEAD and 10MHZ_LAG be between 50 mV and 350 mV and within 20 mV of each other.

If neither an external 10 MHz reference is applied nor an optional frequency reference is installed, the microcontroller will set DAC/-PLL "high", disabling the PLL and pre-charging the PLL integrator to 3.66 × CAL_20MHZ control voltage. When DAC/–PLL is "high", the analog switches (U108) disconnect the phase/frequency detector from the PLL integrator, ground the inverting input to the integrator, and apply a feedback signal to the non-inverting input of the integrator. The feedback signal is the difference between the output of the integrator divided by 11 and the filtered CAL_20MHZ signal divided by 3. The integrator output, pin 1 of U109A, will slew until the feedback signal is zero (i.e., to where the integrator output is equal to CAL_20MHZ ×11 / 3). Since CAL_20MHZ can be set between 0 and 4.095 VDC, the integrator output can be set from 0 to 15 VDC.

Using this approach, prior to applying the external 10 MHz reference, the PLL integrator will be pre-charged to the voltage for which the 20 MHz timebase was last calibrated. Also, the microcontroller can calibrate the 20 MHz timebase finding the value of CAL_20MHZ which provides the same voltage seen on 10MHZ_VC when the 20 MHz timebase is locked to an accurate external reference.

DDS and the 19.40/19.44 MHz Reference

Main Board, Schematic sheet "CG_MB2D"

Clock outputs from the CG635 are generated by dividing down the output of an RF synthesizer. The RF synthesizer operates between 950 MHz and 2050 MHz and is used without division to provide clock outputs in that range.

The RF synthesizer used in this instrument (see sheet "CG_MB3D") requires one of two low-noise reference frequencies: 19.40 MHz or 19.44 MHz. Both of these references need to be tuned over a range of ±100 ppm and need to be set with a resolution of $1{:}2^{64}$ (about $1{:}2\times10^{19}$).

The purpose of the circuitry on this page of schematics is to provide a low noise 19.40 MHz or 19.44 MHz reference for the RF synthesizer which is tunable over ±100 ppm with very high resolution.

Direct Digital Synthesis (DDS) allows the generation of the reference frequency with arbitrary precision. However, DDS synthesizers have a rich spur spectrum that makes them unsuitable for multiplication to high frequencies. This design uses a voltage controlled crystal oscillator (VCXO) phase locked to a DDS reference by a narrow bandwidth PLL to simultaneously achieve high frequency resolution and low spurious components. The low-noise VCXO is then frequency multiplied by the dual-modulus RF synthesizer to generate high frequency, low-noise clock outputs.

An integrated 48-bit DDS (U200) is used to generate tunable reference frequencies around 19.40 MHz or 19.44 MHz. The DDS provides complementary 12-bit current source outputs at a sampling rate of 100 MHz. The stair-stepped current sources are ac coupled by T200 and low-pass filtered by C213-C218 and L202-204. The sine-wave output of the low-pass filter is converted to a reference clock by the AD8561 comparator, U203. A 19.40 MHz or a 19.44 MHz VCXO will be phase locked to this signal with a narrow bandwidth. Doing so provides a spur-free reference of a VCXO with the arbitrarily high frequency precision of a DDS.

The B-Port of the microcontroller (see sheet "CG_MB5D") is used to read and write data to the DDS registers via the bidirectional level shifter U503. Address and read/write control bits for the DDS arrive via U502. The 20 MHz clock comes from the 20 MHz timebase on Sheet 1, and is multiplied by 5× by a clock multiplier in U200.

The DDS output frequency is controlled by the 48-bit Frequency Tuning Word (FTW) loaded in the DDS registers. The DDS has a Frequency Shift Key (FSK) input which allows the DDS to shift between two different FTWs. This feature is used to extend the frequency resolution of the 48-bit DDS by 16 bits to 64 bits in the following manner: Two 48-bit (FTWs) are loaded into the registers of U200, FTW and FTW+1. By applying a Pulse Width Modulated (PWM) signal (with 16 bits of duty cycle resolution) to the FSK input, the DDS can operate with any FTW (with 16 bits of resolution) between FTW and FTW+1. The frequency error associated with a ±1/2 LSB quantization error in the 16-bit duty cycle of the FSK will cause a clock output to time shift by 7 ps/year relative to an ideal source (which is considered to be negligible).

The two VCXOs, one at 19.40 MHz and the other at 19.44 MHz, operate continuously. When the user enters a new operating frequency, the microcontroller determines which VCXO will allow the RF synthesizer to generate the required RF frequency with the lowest divisors, consistent with the ±100 ppm tuning restriction of the VCXOs. The comparator for that VCXO is enabled and the selected VCXO will be phase-locked to the tunable DDS source.

The two VCXOs are nearly identical. The 19.40 MHz VCXO will be described here: The VCXO uses a Colpitts configuration consisting of Y200 with the series load consisting of capacitors C256, C242 and C243 and the dual varactor D200. The crystal is a fundamental mode, AT-cut, designed to operate with a parallel load 20 pF. The sine wave output of the VCXO is converted to TTL levels by U205, which is enabled when the logic signal ALT_REF is set high. (When ALT_REF is high, the comparator for the 19.44 MHz reference is latched.)

The symmetry of the selected VXCO reference is controlled by the integrator U204B which compares the filtered output of the selected reference to Vcc/2. If the duty cycle of the selected reference is low, the integrator output will ramp upward, increasing the bias at the inverting input to the comparators (U205 and U210), and so increase the duty cycle of the inverted outputs from the comparators.

The selected VCXO is phase locked to the DDS reference by a PLL which consists of the phase/frequency detector (U207A, U207B and U208), a pre-filter (R217/C247 & R218/C248), and an integrating loop filter (U204A and surrounding R's and C's). The phase/frequency detector compares the phase of the DDS to the phase of the selected VCXO. If the DDS leads in phase, then the output of the phase/frequency detector will

cause the integrating loop filter to ramp upward, increasing voltage on the varactor (D200 or D201) and so increase the frequency of the VCXO until it is brought in-phase with the DDS.

Minimum pulse widths will be seen at the Q outputs of U207A/B when the PLL circuit achieves phase-lock. The pulse widths will be equal to the sum of the propagation delays through the OR gate (U208, 0.9-3.6 ns) and the flip-flops (U207, 1.0-5.4 ns). For propagation delay sums between 1.9 ns and 9 ns, and a period of 51.5 ns, the duty cycle of the 3.3 V pulse is between 3.6 % and 17 % leading to a voltage of 118 mV to 561 mV on the pre-filter outputs (19MHZ_LEAD and 19MHZ_LAG.) Hence the criteria for phase lock of the VCXO to the DDS are that 19MHZ_LEAD and 19MHZ_LAG be between 100 mV and 600 mV and within 20 mV of each other. The PLL bandwidth is 20 Hz.

The varactor voltage can operate between 0 and +15 VDC to tune the VCXO over a range of about ±180 ppm. The frequency synthesizer design only requires a range of ±100 ppm; hence, the varactor voltage will not need to go to the rails. An attenuated and filtered version of the varactor voltage (19 MHZ_VC) may be read via the microcontroller's ADC to verify the tuning range of the VCXO.

Time Modulation

Main Board, Schematic sheet "CG_MB3D"

The CG635 has a rear panel time-modulation input (J300) which allows an analog voltage to modulate the timing of the clock outputs. This input is calibrated to have a sensitivity of 1 ns/V and a full-scale range of ±5 ns. The input is DC coupled and so may be used as a DC phase adjustment of the clock outputs. Broadband noise applied to this input will cause broadband output jitter (within the bandwidth of the RF PLL).

The selected 19 MHz VCXO is used as a frequency reference to the dual-modulus RF PLL synthesizer. Since the synthesizer phase locks its RF output to the reference input, time-modulation of the reference will time-modulate the clock outputs. The frequency reference is time modulated by converting the 19 MHz square wave from the output of U213 to a linear ramp on C302, applying the linear ramp and the time-modulation signal to the inputs of a fast comparator (U302), and using the output of the comparator as the frequency reference for the RF synthesizer (U307).

The linear ramp on C302 is created by equal opposing current sources which are alternately applied to C301 or C302 by the diode bridge (D300/D301). When the 19 MHz output from U301 is low, the current sourced by U300A via L300 and R304 is shunted to C301, causing C302 to ramp down. When the 19 MHz output from U301 is high, the current drawn by U300B via L301 and R305 is sourced by C301, causing C302 to ramp up. The positive current source (U300A) is controlled by the analog signal CAL_TMOD so as to calibrate the rear panel time-modulation input sensitivity. The negative current source (U300B) is configured to maintain the ramp on C302 so that it is symmetrical about ground.

The time modulation input (J300) is filtered, attenuated and limited by R308-312, C307, C308, and D302 before being applied to the comparator (U302). The input impedance of

the time modulation input is 1 kΩ for frequencies below 100 kHz, 50 Ω for frequencies above 1 MHz, and is bandwidth limited to 200 kHz.

RF Synthesizer

Main Board, Schematic sheet "CG_MB3D"

The RF synthesizer consists of a VCO (U310), a fast PECL comparator (U304B), a dual-modulus synthesizer (U307), and a charge-pump loop filter (U309 and various R's and C's). The VCO can be tuned over more than an octave (960-2050 MHz). The dual-modulus synthesizer has a very low noise floor (typically –159 dBc/Hz at a comparison frequency of 1 MHz). The low-noise loop filter has an adjustable proportional gain to minimize timing jitter as synthesizer parameters are changed.

Several measures are used to reduce the disturbance of the RF PLL by external sources of noise and interference: (1) the VCO is powered by a low noise op-amp whose output is 2.5 × the (filtered) 4.096 V reference, (2) SPI clock and data to the RF PLL (U307) are gated "off" by U306 unless U307 is the intended target of the data transfer, (3) a low-dropout linear regulator is used to power the dual-modulus synthesizer, and (4) the charge pump is powered by the +4.096 V reference.

Low clock jitter (which is close to, but not exactly the same as low phase noise) is an important design goal for the RF synthesizer. The dual-modulus synthesizer is a PLL that phase locks the VCO frequency (divided by an integer N) to the reference frequency (divided by an integer R). The VCO output frequency, f_{vco}, is therefore set by the choice of reference frequency, f_{ref}, and the R and N divisors: $f_{vco} = f_{ref} \times N / R$. The phase noise of the VCO output cannot be better than the "multiplied up" (i.e., degraded by 6 dB/octave or 20 dB/decade) phase noise floor of the synthesizer at the comparison frequency. For example, with a reference frequency of 19 MHz (as we have here) and an R divider of 19 (which is close to the worst case, as we shall see), the comparison frequency is 1 MHz, for which the synthesizer noise floor is typically –159 dBc/Hz. If we are generating an output frequency near 1 GHz, which is three decades above the 1 MHz comparison frequency, the best phase noise we can expect from the VCO is $–159 + 3 \times 20 = –99$ dBc/Hz. So a key goal here is to operate the dual-modulus synthesizer with small R divisors so as to keep the comparison frequency high to keep the phase noise low.

We also need to be able to generate all frequencies between 960 MHz and 2050 MHz with 16 digits of resolution. Large values of R and N would be required to achieve this high resolution if the reference frequency was not tunable. However, using just two reference frequencies (either 19.40 MHz or 19.44 MHz) that are tunable over a range of ±100 ppm we have the following remarkable results: (1) any frequency in the range of 960 MHz to 2050 MHz may be generated, (2) the average R divisor will be 8, (3) the largest R divisor will be 25, and (4) the prime factors of 19.44 MHz ($2^7 \times 3^5 \times 5^4$) are such that many canonical frequencies can be generated with an R divisor of 1.

The output of the RF synthesizer is a complementary pair of +3.3 V PECL levels (+RF_VCO and –RF_VCO) from U304B. These outputs have the following characteristics: (1) Vhigh = +2.34 V, (2) Vlow = +1.55 V, (3) t_{rise} = 175 ps, (4) t_{fall} = 140 ps, (5) $t_{jitter} < 1$ ps_{rms}, (6) f_{min} = 960 MHz, and (7) f_{max} = 2050 MHz.

ECL Dividers and Clock Multiplexer

Main Board, Schematic sheet "CG_MB4D"

The differential PECL clock from the RF synthesizer (+RF_VCO and –RF_VCO) is the "top octave" clock that may be set from 960 MHz to 2050 MHz with 16 digits of resolution. This clock is also used to clock ECL divider circuits that can divide the clock by 2, 4, 8, 16, 32 … 1024. The output from the ECL divider may also be further divided by U408, a programmable divider that has programmable phase jumps. An ECL 1:4 multiplexer (U404) is used to select one of four sources for output from the CG635: (1) the undivided "top octave" clock, (2) the "top octave" clock divided by 2 by U400, (3) the top octave clock divided by 4 × (256-ECL_DIV) where ECL_DIV is the 8-bit "LOAD" value to the programmable counter, U401, or (4) the top octave clock divided by 64 and further divided by a factor between 2^n where $5 \leq n \leq 30$ by U408. When the "top octave" is selected, U411 disables the ECL dividers to reduce sub-harmonic distortion. All clocks, both the inputs to and the outputs from the multiplexer U404, are differential +3.3 V PECL levels.

The ECL programmable divider was designed to operate to >1 GHz. The –TC output from U401 goes low on the terminal count (i.e. when the counter reaches 255) and will load the ECL_DIV value synchronously with the next clock. The –TC output is pipelined (to meet propagation delay constraints) and inverted by U402, a D-type flip-flop. The output of U402 is applied to the J&K inputs of the J/K flip-flop, U403. The J/K flip-flop will toggle states with a clock if the J&K inputs are both high, and will not change if the J&K inputs are both low. Therefore, the output of the J/K flip-flop is at a rate equal to the top octave clock divided by 4 × (256-ECL_DIV) = 4, 8, 12, 16, ..1024.

The ECL divider can be used to generate clock outputs as low as 960 MHz/1024 or 937.5 kHz. Output frequencies below 937.5 kHz are generated by the CMOS programmable divider (U408) which is clocked by the RF/64 via the TTL comparator U407.

For frequencies above 1 MHz, phase adjustments to the output are accomplished by running the DDS synthesizer off-frequency by a small amount (less than 5 ppm, as limited by the headroom available in the VCXO tuning characteristic) for an accurately controlled interval of time. The maximum phase step is limited to ±360°. At 1 MHz, the clock edges will have to move by 1 µs for a 360° step. Running off-frequency by 5 ppm for 200 ms will accomplish this phase step. At 1 GHz, a 360° step can be accomplished with a 0.05 ppm frequency offset for an interval of 20 ms. And so phase adjustments can be done quickly at frequencies above 1 MHz, even with a limited frequency offset. However at an output frequency of 1 Hz, a 360° step would require running off frequency by 5 ppm for 200,000 s (more than two days) which is clearly not acceptable. An alternate approach to phase stepping is used for output frequencies below 1 MHz to overcome this limitation. The programmable divider in U408 may be jumped ahead (or backward) by an integer number of clock cycles allowing large instantaneous phase jumps. High resolution phase steps at low output frequencies are accomplished by combining both methods (phase step in the CMOS divider and phase slew by running the DDS off-frequency for an accurately determined interval of time).

A differential clock fan-out driver (U405) is used to fan-out the selected clock to multiple destinations: to (1) the front panel Q&$\overline{Q}$ driver, (2) the front panel CMOS driver, (3) a low pass filter to allow the microcontroller's ADC to measure the top-octave symmetry, (4) rear panel LVDS and RS485 clock outputs, and (5) an optional pseudo-random binary sequence generator. The clock driver can select between two clock sources: when the bit –RUN/STOP is "low", the clock driver selects the CLK0 input which is the output of the 1:4 ECL multiplexer; when –RUN/STOP is "high", the clock driver selects the CLK1 input which is the STOP_LVL bit from the microcontroller. This allows the microcontroller to set the outputs high or low for "half-stepping" and for calibration purposes. The clock driver outputs are enabled when the –EN_OUT is low. The selected clock is enabled synchronously with its own falling edge, thereby eliminating runt pulses. (The synchronous enable will require the microcontroller to toggle the state of the STOP_LVL bit before it appears at the outputs, and will cause a one-cycle delay in the enabling of free-running clocks.)

The differential PECL clocks for the front panel outputs connect to the driver daughter board via J400. This connector also passes amplitude and offset control voltages and power supplies to the front panel output driver board.

Microcontroller

Main Board, Schematic sheet "CG_MB5D"

The microcontroller (U500) is a MC68HC912D60A. The important features used in this design include (1) 16-bit device with hardware math operations, (2) 60k bytes of flash ROM for program instructions, (3) 2k bytes of RAM for volatile storage, (4) 1k byte of EEPROM for calibration constants, (5) dual serial communication interfaces for two RS-232 channels, (6) serial peripheral interface for communications with system components, (6) 16-bit pulse width modulator for extending the resolution of the DDS via its FSK input, (7) sixteen channels of 10-bit A/D conversion for testing and calibration, (8) real-time interrupt generator, and (9) myriad I/O port bits for system integration.

Analog Inputs to the Microcontroller

There are 16 analog inputs to the microcontroller. The full-scale range is 0-4.096 VDC and the inputs are digitized with 10 bits of resolution (4.00 mV per bit). Details for each of the sixteen inputs are given below.

EXT_DET: Greater than 1.00 VDC indicates that an external 10 MHz reference has been applied to the rear panel input and so the 20 MHz timebase should be phase-locked to the external reference.

OPT_DET: Greater than 1.00 VDC indicates that an optional 10 MHz reference is installed and operating and so the 20 MHz timebase should be phase-locked to the optional timebase if an external reference is not present.

10MHZ_LEAD: Used to detect the phase-lock of the 20 MHz timebase to an external or an optional timebase. 10MHZ_LEAD is a voltage proportional to the amount by which the external reference or optional reference leads the 20 MHz timebase. The front-panel UNLOCK LED will be lit if the instrument is trying to lock the 20 MHz timebase

to either an external or an optional timebase and the 10MHZ_LEAD and 10MHZ_LAG are not between 50 mV and 350 mV or not within 20 mV of each other.

10MHZ_LAG: Used to detect the phase-lock of the 20 MHz timebase to an external or an optional timebase. 10MHZ_LAG is a voltage proportional to the amount by which the external reference or optional reference lags the 20 MHz timebase. The front-panel UNLOCK LED will be lit if the instrument is trying to lock the 20 MHz timebase to either an external or an optional timebase and the 10MHZ_LEAD and 10MHZ_LAG are not between 50 mV and 350 mV or not within 20 mV of each other.

10MHZ_VC: Scaled (by 0.285×) and filtered (with about 500 Hz bandwidth) version of the varactor voltage that controls the frequency of the 20 MHz VCXO timebase. The front-panel UNLOCK LED will be lit if the instrument is trying to lock the 20 MHz timebase to either an external or an optional timebase and the 10MHZ_VC is less than 0.25 V or greater than 3.75 V. (These thresholds may change.)

19MHZ_LEAD: Used to detect the phase-lock of the 19.4 MHz timebase to the DDS. 19MHZ_LEAD is a voltage proportional to the amount by which DDS leads the 19.4 MHz VCXO. The front panel UNLOCK LED will be lit if 19MHZ_LEAD and 19MHZ_LAG are not between 100 mV and 600 mV or not within 20 mV of each other.

19MHZ_LAG: Used to detect the phase-lock of the 19.4 MHz timebase to the DDS. 19MHZ_LAG is a voltage proportional to the amount by which DDS lags the 19.4 MHz VCXO. The front panel UNLOCK LED will be lit if 19MHZ_LEAD and 19MHZ_LAG are not between 100 mV and 600 mV or not within 20 mV of each other.

19MHZ_VC: Scaled (by 0.285×) and filtered (with about 500 Hz bandwidth) version of the varactor voltage that controls the frequency of the 19.4 MHz VCXO timebase. The front panel UNLOCK LED will be lit if 19MHZ_VC is less than 0.25 V or greater than 3.75 V. (These thresholds may change.)

10mV/C: Analog voltage proportion to the PCB temperature in °C. Scale factor is 10 mV/°C with zero intercept. (Example: 300 mV at 30°C)

RF_VC: Scaled (by 0.210×) and filtered (with about 50 Hz bandwidth) version of the varactor voltage that controls the frequency of the RF VCO. The front panel UNLOCK LED will be lit if RF_VC is less than 0.20 V or greater than 3.00 V. (These thresholds may change.)

+CLK_TST: Analog voltage equal to the average voltage (with 1 ms time constant) of the non-inverted PECL clock source. The signal is useful for measuring the duty cycle of the top octave clock signal when compared to –CLK_TST. The analog DAC voltage CAL_SYM will be adjusted to equalize +CLK_TST and –CLK_TST to assure 50/50 duty cycle in the top octave.

-CLK_TST: Analog voltage equal to the average voltage (with 1 ms time constant) of the inverted PECL clock source. The signal is useful for measuring the duty cycle of the top octave clock signal when compared to +CLK_TST. The analog DAC voltage CAL_SYM will be adjusted to equalize +CLK_TST and –CLK_TST to assure 50/50 duty cycle in the top octave.

+Q_TST: Offset, scaled and filtered (with 180 Hz bandwidth) version of the front panel Q output. Useful for testing and calibrating the amplitude and offset of the Q output provided that the user load is disconnected from the instrument. Transfer function: +Q_TST = 0.285 × (+Q_OUT + 4.096 V).

–Q_TST: Offset, scaled and filtered (with 180 Hz bandwidth) version of the front panel $\overline{Q}$ output. Useful for testing and calibrating the amplitude and offset of the $\overline{Q}$ output provided that the user load is disconnected from the instrument. Transfer function: –Q_TST = 0.285 × (–Q_OUT + 4.096 V).

CMOS_TST: Offset, scaled and filtered (with 140 Hz bandwidth) version of the front panel CMOS output. Useful for testing and calibrating the amplitude and offset of the CMOS output provided that the user load is disconnected from the instrument. Transfer function: CMOS_TST = 0.444 × CMOS_OUT + 0.455 V.

+24V_TST: Scaled and filtered (with 120 Hz bandwidth) version of the +24 V power supply. +24V_TST = 0.130 × +24 V (unswitched) power supply. The scaling network has a high impedance so as to source only 200 µA from the +24 V standby power supply when the instrument is turned "off".

RS-232 Interfaces

RTS_RS232: Request-to-Send input to CPU from the rear panel RS-232 interface.

RXD_RS232: Serial data input to CPU from the rear panel RS-232 interface.

RXD_RB: Serial data input to CPU from the optional rubidium timebase.

CTS_RS232: Clear-to-Send output from CPU to the rear panel RS-232 interface.

TXD_RS232: Serial data output from CPU to the rear panel RS-232 interface.

TXD_RB: Serial data output from CPU to the optional rubidium timebase.

Digital Inputs to Microcontroller

-DROPOUT: Status bit goes low to generate an –XIRQ (non-maskable interrupt request) when the unit is turned "off" or when the power is removed.

-GPIB: Status bit goes low to generate an –IRQ (maskable interrupt request) when the GPIB interface requires service.

10MHZ: 10 MHz square wave processor clock derived from the 20 MHz timebase.

KEY0-KEY4: Five key strobe lines. One of the five lines will go "high" when a front panel key is pressed during the column strobe period for that key. All five inputs have their active pull-downs enabled.

-DONE: This line goes low when the phase jump requested of U408 has been completed.

-RB_OPT: This line is pulled low when the optional rubidium timebase is installed. (The active pull-up for this port bit is enabled.)

-OCXO_OPT: This line is pulled low when the optional Oven Controlled Crystal Oscillator (OCXO) timebase is installed. (The active pull-up for this port bit is enabled.)

-PRBS_OPT: This line is pulled low when the optional PRBS generator is installed. (The active pull-up for this port bit is enabled.)

RF_LOCK: This line goes high when the RF synthesizer has achieved phase-lock to the 19 MHz reference.

Microcontroller Outputs

PORT_A: Data bus (8-bits) supplies data to nine octal latches. There is a corresponding port strobe for each of the nine latches (ex: -CS_LAMP or –CS_ODD or –CS_EVEN). Data is latched on the rising edge of the port strobe. Latches are operated from either +5 V or +3.3 V as required by the target.

-CS_GPIB_CTL: Port strobe for GPIB interface latch.

-CS_DDS_CTL: Port strobe for DDS interface latch.

-CS_DDS: Port strobe for DDS bi-directional (read or write) data transfer.

-CS_GPIB_CTL: Port strobe for GPIB interface latch.

-CS_STROBE: Port strobe for LED and KEY strobe line latch.

-CS_LAMP: Port strobe for lamp LEDs latch.

-CS_ODD: Port strobe odd-digit seven-segment LED display latch.

-CS_EVEN: Port strobe even-digit seven-segment LED display latch.

-CS_SYN: Chip select for dual-modulus synthesizer.

-CS_FLT: Port strobe for RF PLL bandwidth control (& misc) latch.

-CS_DIV: Port strobe for programmable ECL divider interface latch.

-CS_ECL: Port strobe for ECL logic control interface latch.

-CS_DAC: Port strobe for octal 12-bit DAC that supplies system analog voltages.

FSK_DDS: Pulse width modulated signal whose duty cycle is controlled with 16 bits of resolution to extend the resolution of the 48-bit DDS to 64 bits.

SDO: Synchronous serial data output for data transfer to octal DAC and dual-modulus synthesizer.

SCK: Serial clock output for synchronous data transfer to octal DAC and dual-modulus synthesizer.

DAC/–PLL: Controls the operation of the 20 MHz timebase. A high level allows the frequency to be controlled by the CAL_10MHZ DAC output. A low level will cause the 20 MHz timebase to be phase locked to either an external 10 MHz input or to an installed optional reference (rubidium or OCXO.)

–EXT/OPT: Controls which high-precision source (either the external 10 MHz or an internal OCXO or rubidium) is used as a frequency reference for the synthesizer. The bit –EXT/OPT is set low to select the external 10 MHz reference or set high to select the optional OCXO or rubidium.

EN_PRBS: This bit is used to enable the optional PRBS generator. When low, the PRBS shift register is loaded with all "ones". When set high, the PRBS generates a random binary sequence with a run-length of 127 bits.

Microcontroller Bi-directional Port

PORT_B: Port B is used as a bidirectional port for reading and writing data to the GPIB and DDS. Level translation and direction control between the microcontroller and the DDS is provided by U503. Data flow is controlled by the following: a data direction register in the microcontroller, –CE_GPIB (U501), –WR_GPIB (U501), DBIN_GPIB (U501), –WR_DDS (U502), –RD_DDS (U502) and –CS_DDS (U500).

Analog Control Voltages

An octal 12-bit DAC (U504) provides analog voltages for system control. The DAC outputs have 1 mV resolution between 0 V and 4.095 VDC. The functions of the eight control voltages are detailed here:

CAL_OPT: Used calibrate the frequency of an optional timebase (either rubidium or an OCXO.) Nominal: +2.048 VDC. Scaled to 0 V to +5 V (for ± 0.02 Hz on PRS10) and 0 V to +10 V (for ±2.5 Hz on SC10-24-1-J-J-J-J)

CAL_20MHZ: Used calibrate the frequency of the standard 20 MHz timebase (which is divided by two to provide the rear-panel 10 MHz timebase output.) This voltage controls the frequency of the timebase when no external reference is applied and no optional timebase is installed. Full-scale range is about ±20 ppm. Nominal: +2.048 VDC.

CAL_TMOD: Used to calibrate the sensitivity of the rear panel time modulation input to 1 ns/V. Nominal: +2.048 VDC. Full scale range is approximately ±20 %.

CAL_SYM: Used to calibrate the symmetry of the top octave output clock as indicated when the difference between +CLK_TST and –CLK_TST is zero. Increasing CAL_SYM will decrease +CLK_TST and increase –CLK_TST. The required value may be a function of frequency.

Q_AMPL: Controls the amplitude of the front panel Q & -Q outputs. The output amplitude, Q_{AMPL}, is given by: $Q_{AMPL} \approx 0.276 \times$ Q_AMPL.

Q_OFFS: Controls the high level offset of the front panel Q & -Q outputs. The output offset, Q_{OFFS}, is given by: $Q_{OFFS} \approx 1.834 \times Q\_OFFS - 2.150$ V.

CMOS_AMPL: Controls the amplitude of the front panel CMOS output. The output amplitude, $CMOS_{AMPL}$, is given by: $CMOS_{AMPL} \approx 1.648 \times CMOS\_AMPL$.

CMOS_OFFS: Controls the low level offset of the front panel CMOS output. The output offset, $CMOS_{OFFS}$, is given by: $CMOS_{OFFS} \approx 0.519 \times CMOS\_OFFS - 1.063$ V.

Microcontroller Output Latches

There are nine octal output latches to which the microcontroller writes data via the Port-A bus to control the instrument. There are:

U501: GPIB register address and control latch.

U502: DDS register address and control latch.

U506: Front panel seven-segment (odd digit) segment enable latch.

U507: Front panel seven-segment (even digit) segment enable latch.

U508: Front panel display and keypad strobe latch.

U509: Front panel LED lamp enable latch.

U510: RF reference and RF PLL bandwidth control latch and CMOS enable.

U511: Programmable ECL divider load value.

U512: Band select, output enable, PRBS enable, LVDS enable

Microcontroller Display and Keypad Scanning

Four of the octal latches (U506-U509) are used to refresh the front panel LED displays and scan the keypad for key presses. The front panel display and key pad scanning is controlled by seven strobe lines: STB0 to STB6. Each strobe line enables two seven-segment displays, up to six LED lamps and the scanning of up to six keys. The display refresh consists of eight periods of 1 ms duration; seven periods to refresh the entire display and scan the keypad and an eight period to intensify/blink one of the seven-segment display digits to show which digit would be affected by a step-up/step-down key press. The sequence of that operation is outlined here.

1. At the start of each 1 kHz real-time interrupt the microcontroller writes all zeros to U508 to disable all of the displays.

2. Data for the next strobe interval is loaded into the U506 (odd digit segments), U507 (even digit segments), and U509 (LED lamps.) Writing a “0” will turn “on” the corresponding segment or lamp, writing a “1” will turn it “off”.

3. A single “1” is written to U508 to enable a single strobe line.

4. Port-G is read to see if any keys have been pressed in the currently enabled strobe column. Port-G is configured with active pull-downs to return the KEY0-KEY5 to ground after the key is released.

5. The sequence terminates with a return from interrupt instruction.

NPN emitter followers (Q500-Q506) are used to provide the required strobe line current. PNP emitter followers (Q507-Q512) are used to provide the required lamp drive current. High efficiency seven-segment displays are driven directly by the octal latches and do not require emitter followers. Current in the seven segment displays is limited by N500 and N501 and current in the LED lamps is limited by N504-N506.

The front panel LED refresh could cause substantial interference at harmonics of 125 Hz due to the 8 ms refresh interval. A large power supply capacitor, C514, is used as a source for this large periodic current and the ground return path for the LED currents is isolated from the other circuit grounds. The capacitor is charged from the +5_digital supply via a L501.

A 10 ms one-shot, U505A, is used to disable the LED current drive if the microcontroller stops generating –CS_STROBE signals. This prevents damaging the LEDs (which are normally operated with a $1/8^{th}$ duty factor) should the microcontroller stop operating. The second half of U505 is used to generate a key-click sound when the MSB of U508 is set high.

Rear-Panel RJ-45 Outputs

Main Board, Schematic sheet "CG_MB6D"

The clock and ±5 VDC are made available on the rear-panel RJ-45 connector (J604). Both LDVS (pins 1 & 2) and RS-485 levels (pins 7 & 8) are available on the RJ-45 connector. The outputs are intended to drive unshielded twisted pair (UTP) CAT-6 cable with 100 Ω terminations on the clock lines. The ±5 VDC supplies may be used to power far-end line receivers. The current that may be drawn from these supplies is limited to 375 mA.

The RS-485 outputs are turned "off" above 105 MHz. The LVDS outputs operate up to 2.05 GHz. Internal PECL levels are translated to LVDS levels by the resistor networks R622-R625. These resistor networks also reverse terminate the LVDS source with the 100 Ω characteristic impedance of the UTP cable.

The PECL clock is also used to drive the differential inputs of the RS-485 line driver (U607), converting the clock to TTL levels. The open-emitter clock outputs from U605 will only be active when -EN_RS485 is low. When –EN_RS485 is high, the rear-panel RS-485 outputs will be turned "off".

An N-channel MOSFET (U612) provides +5 VDC on the RJ-45 connector. The MOSFET is turned "off" by U611A if the current seen in the shunt resistors (R617, R618 & R641) exceeds 375 mA. A co-packaged Schottky diode in U612 prevents the +5 VDC from being pulled below ground.

A P-channel MOSFET (U613) provides –5 VDC on the RJ-45 connector. The MOSFET is turned "off" by U611B if the current seen in the shunt resistors (R637, R638 & R642) exceeds 375 mA. A co-packaged Schottky diode in U613 prevents the –5 VDC from being pulled above ground.

RS-232 and GPIB Interfaces

Main Board, Schematic sheet "CG_MB6D"

The TXD and CTS outputs from the microcontroller are converted to RS-232 levels by U604. The received RS-232 signals, RXD and RTS, are converted to TTL levels for the microcontroller by U604. U604 also provides an RS-232 high level for the CD and DSR (carrier-detect and data-set-ready) lines on the RS-232 DB-9 connector (J603).

The GPIB interface (U601) is connected to the rear panel GPIB connector (J602) via the buffers U602 and U603. Data is read and written to U601 via the bi-directional Port-B. Other control lines for U601 come from U501. U601 indicates a need for service by asserting –GPIB (the –IRQ maskable interrupt request) to the microcontroller.

Power Supply Interface

Main Board, Schematic sheet "CG_MB6D"

The CG635 uses a universal input switching power supply in a separate enclosure to power the system. The power supply has a +24 V output which is "on" whenever the instrument has line voltage (whether or not the power switch is "on"). This power supply powers the optional timebase (an OCXO or rubidium) even while the instrument is "off". LED lamps on the main circuit board and in the modular power supply indicate the presence of the +24 V supply. DC to DC inverters, which provide ±15 V, ±5 V, and +3.3 V to power the instrument, are enabled when the –ENABLE pin on the modular power supply is pulled to ground by the front panel power button.

A dual comparator (U600) is wire-or'd to alert the microcontroller via –DROPOUT that the power switch has been turned "off" or that the +24 VDC main power supply is coming out of regulation. The –DROPOUT asserts an –XIRQ to the microcontroller which suspends operations until the +24 V recovers.

Front-Panel Output Drivers

To reduce the effect of circuit parasitics, components for the front-panel output drivers (Q / $\overline{Q}$ and CMOS) are located on a small circuit board directly behind the output BNCs. The PCB and BNC block are secured to the front panel by two screws which hold the connector block to the front panel. To remove the output drivers you must remove these two screws, and the four side-panel screws, and tilt the front panel forward. The output driver block may then be removed vertically.

A twenty-pin connector (J604 on the main PCB and J100 on the driver PCB) passes the clock signals, amplitude and offset control voltages and the power supplies from the main PCB to the driver PCB. The connectors are positioned so as to reduce the path length for the fast signals.

Front-Panel Q and $\overline{Q}$ Drivers

Driver Board, Schematic sheet "CG_DR1F"

The Q and $\overline{Q}$ outputs are high speed (DC-2.05 GHz with transitions times of <100 ps), low amplitude (0.2 V to 1.0 V), differential outputs designed to be terminated into 50 Ω loads. The outputs' high level can be as high as +5 VDC or as low as –2 VDC to be compatible with a variety of logic families (+5 V PECL, +3.3 V PECL, LVDS, RF, ECL, RSECL, etc.) If either the Q or $\overline{Q}$ output is used, both outputs should be terminated with 50 Ω to ground.

Each of the Q and $\overline{Q}$ outputs consist of two series 24.9 Ω resistors (to provide a source impedance of 50 Ω) connected to a programmable voltage source (U100). The programmable voltage source is set to twice the high level for the desired logic output. This voltage source must always source current to operate properly. In the case of negative output offsets it is necessary to load the voltage source, which is done by U107B and Q101.

A fast, differential, current sink provided by U105 (MAX3737) alternates between the Q and $\overline{Q}$ outputs under the control of the ±Q_DRV clock signals. An output is pulled low when current is drawn from that output by U105. The current source is programmed by the analog control voltage Q_AMPL. Increasing the current source increases the amplitude of the output clock signal.

The MAX3737 (U105) is a laser diode driver, and it is used in this application to provide an extremely fast current switch. The 3.3V part has a very limited output voltage compliance range, and so it is operated from two power supplies which track the outputs' high level. The ±Q_DRV clock signals which switch the fast current sink are AC coupled to U105 via C111 and C112, and the DC levels for these logic signals are maintained by the (slow) differential amplifiers U104A and U104B.

The MAX3737 has other features which are not used here but which need to be accommodated so as to avoid apparent "fault" conditions. The transistor Q100 imitates a laser diode's photo monitor by providing small current that increases with the MAX3737's bias current generator. U106 provides a reset to U105 in the case that a fault should occur.

The Q and $\overline{Q}$ output levels may be sampled by the microcontroller via the ±Q_TST outputs which are attenuated, offset and filtered versions of the Q and $\overline{Q}$ outputs. These test points allow the microcontroller to verify operation, check for user termination, and calibrate the output amplitudes and offsets of the Q and $\overline{Q}$ outputs.

Front-Panel CMOS Driver

Driver Board, Schematic sheet "CG_DR2F"

The front-panel CMOS driver is a high-level (up to 6 V), fast transition time (<1.0 ns), cable driver with a 50 Ω source impedance. The baseline for the output, which is normally at 0 VDC, may be offset by ±1.00 VDC. This output is normally not terminated with 50 Ω. Doing so will not damage the output, and will improve the

transition times, but terminating the output will reduce the output levels by a factor of two.

The CMOS output offset and amplitude are controlled by the analog signals CMOS_OFFS and CMOS_AMPL. The output is biased at the midpoint of the logic transition by U200. The output may be offset from the midpoint by the CMOS_OFFS signal, and the output is pulled above the midpoint (or pulled below it) by the outputs of the fast differential current sink, U203. The ±CMOS_DRV PECL level signals are terminated by R205 and R206 and drive the inputs to the fast current sink via the cascode transistors Q200 and Q201.

The amplitude of the current sink is controlled by CMOS_AMPL. U205A servos U203 to provide the correct current by comparing the output current to CMOS_AMPL. When the clock level is “0”, the OUT- output of U203 sinks current, drawing it from the cascode transistor U206, pulling the output low. When the clock level is “1”, the OUT+ output of U203 sinks current, drawing it from the cascode transistor U205. The collector current of Q205 is mirrored by the transistors Q203 and Q204, pulling the output high.

The CMOS output has a source impedance of 50 Ω, consisting of the parallel combination of R250-R252 in parallel with the series combination of R247-R249. The parallel combination of L200 and R253 match return pulses into the collector capacitance of Q204 and Q206, providing a high return loss at all frequencies.

Front-Panel Display and Keypad

Schematic sheet “CG_FP1B”

The front panel time-multiplexed display PCB has 13 digits, 34 lamps and 33 keys. There are seven strobe lines, each of which allows up to two digits and six lamps to be refreshed and up to six keys to be read during 1 ms intervals. An eighth time interval is use to intensify/blink one of the 13 digits to indicate which digit would be affected by a “modify up/down” key press. Details of the refresh operation are provided in the section “Microcontroller Display and Keypad Scanning.”

Power Supply

Schematic sheet “CG_PS1B”

The modular power supply for the CG635 is in a separate shielded case inside the instrument. The power supply consists of universal input, 60 W, +24 V, OEM switching power supply which is “on” whenever power is applied to the unit (whether or not the power switch is in the “on” position). This supply provides power to the optional timebase whenever the unit is connected to the mains and provides power to two DC-DC converters when the front panel power switch is pressed “on”.

One of the DC-DC converters is a switching power supply (U1) that operates at 260 kHz to provide up to 3 A at +3.3 VDC with an efficiency of about 90 %. The input to this

switcher is filtered by L2 and C2, to reduce crosstalk between the various supplies in the system. U1 controls the duty cycle with which it connects the filtered +24 VDC power supply to the input of L3 in order to regulate the output voltage to +3.3 VDC. The flyback diode, D9, turns “on” when U1 disconnects L3 from the +24 V supply. The output capacitor, C4, holds charge between switching cycles and the L4/C5 filter further reduces the ripple

The second DC-DC converter (U4) operates at 100 kHz to generate unregulated ±8 VDC and ±20 VDC. When enabled (by letting go of the soft-start node) the switching controller drives the gates of the power MOSFETs, Q1 and Q2, with (nearly) 50 % duty cycle square waves that are 180° out of phase. The MOSFETs drive the primaries of an ungapped transformer, whose center tap is at +24 VDC. Full wave rectifiers (D3-D10) drive the inputs to L/C filters (L5-L8 and C12, C15, C18 & C22). The outputs of these filters are conditioned by linear regulators to provide clean voltages to the instrument. Ordering diodes on the outputs, D11-D16, assure that load currents will not create polarity inversions on these power supply outputs.

The DC-DC converters are enabled by the power switch which pulls the –ENABLE line to ground. Doing so turns off the open collector outputs of U3 releasing the soft start input to U4 and the ON/-OFF input to U1.

Timebase Options

Schematic sheet “CG_TB1B”

There are two timebase options: an OCXO (SRS p/n SC-10-24-1-J-J-J-J) and a rubidium frequency standard (SRS p/n PRS10). The optional timebases are held by the same mechanical bracket and connected to the system using the same adapter PCB.

The adapter PCB schematic is quite simple: J1 is the connector to the OCXO option, J2 is the connector to the rubidium option, and J3 is the connector to the main PCB. The op amp U1 is used to scale the 0-4.095 VDC frequency calibration voltage (CAL_OPT) to 0-10 VDC for the OCXO or 0-5 VDC for the rubidium. The logic inverter, U2, is used to invert the logic levels for the RS-232 communication between the microcontroller on the main PCB and the PRS10 rubidium frequency standard.

Optional PRBS Generator

Schematic sheet “CG_PR1B”

A Pseudo-Random Binary Sequence (PRBS) generator is used for testing data transmission systems. A typical arrangement is to display an “eye pattern” on an oscilloscope by triggering the oscilloscope with the clock while displaying the (random) data after it passes through the data transmission system. An “open” eye pattern is necessary for reliable data transmission. The eye pattern “closes” from the left and right with jitter, and from the top and bottom with insufficient channel bandwidth, increasing the likelihood for transmission errors.

The most common way to create a PRBS generator is to use a linear shift-register, feeding the input of the shift-register with the exclusive-or of two (particular) data bits as they shift through the system. The CG635 uses a 7-bit ECL shift register that provides a

pseudo-random bit sequence which repeats after $2^7 - 1 = 127$ clock cycles. The data stream satisfies many criteria to qualify as "random", however it does repeat itself, exactly, after 127 clock cycles. Another departure from randomness is that the longest string of "1's" is seven in a row while the longest string of "0's" is six in a row.

The 7-bit PRBS generator consists of seven D-type flip-flops (U1-U7) and one exclusive-or gate (U8). All clocks and data are passed differentially for lowest noise and maximum speed. The exclusive-or of the 6^{th} and 7^{th} bits are feedback to the shift register input. The 7^{th} bit is used as the PRBS output (any bit would do) and it is buffered by U10.

The critical timing path, which determines the highest clock frequency for which the circuit will operate, is through the exclusive-or gate. The impact of the exclusive-or's propagation delay is reduced by phasing the clocks. Delaying the clock to U1 by 250 ps effectively removes 250 ps of the exclusive-or's 330 ps (worst case) propagation delay, thereby allowing the circuit to operate above 2 GHz. The clock is advanced by 50 ps in each successive stage so that the data meets the setup time for the un-delayed clock at U6. The technique effectively spreads out the exclusive-or's propagation delay over five stages allowing the circuit to operate at a much higher frequency.

The layout of this circuit on the PCB is critical to its operation. The seven flip-flops are arranged in a circle to minimize delays in the data path. Data propagates clockwise around the circle. The clock is arranged to propagate counterclockwise along a differential transmission line with a 20 Ω impedance.

A control bit from the microcontroller, EN_PRBS, is set high to enable the PRBS. Setting EN_PRBS low will force the input to U1 to be a "1". Seven additional clock cycles are required for the rear-panel PRBS output to go to "1" after EN_PRBS is set low. The PRBS output will stay high until 7 clock cycles after the EN_PRBS goes high again.

Both the PRBS data and the clock are output as LVDS levels on rear panel SMA connectors. The PRBS data is buffered by the U10 and converted to LVDS levels by R48-R53. The clock is buffered by the U11 and converted to LVDS levels by R54-R59. These resistor networks also reverse terminate the LVDS source with the 100 Ω characteristic impedance of the UTP cable.

Line Receiver Accessories

The rear-panel of the CG635 has an RJ-45 connector to provide clock signals at RS-485 and LVDS levels as well as ±5 VDC. A series of line receiver accessories are used to receive the clock signals over an unshielded, four-pair, CAT-6 cable and convert the clock to single-ended complementary logic outputs on SMA connectors. In addition to being a useful accessory, these devices demonstrate the use of the RJ-45 outputs.

Ten different clock receivers are available as accessories to provide complementary clock outputs on SMA connectors at standard logic levels. The SMA outputs are intended to drive 50 Ω coax cables terminated with 50 Ω loads to ground (with the exception of the CMOS and the +5 V PECL receivers, which are intended to drive unterminated 50 Ω coax cables.) The following types are available:

SRS Model	Logic output level
CG640	CMOS (+5.0 V_{cc})
CG641	CMOS (+3.3 V_{cc})
CG642	CMOS (+2.5 V_{cc})
CG643	PECL (+5.0 V_{cc}, V_{ee}=0)
CG644	PECL (+3.3 V_{cc}, V_{ee}=0)
CG645	PECL (+2.5 V_{cc}, V_{ee}=0)
CG646	RF (+7 dBm, ±0.5 V_{dc})
CG647	CML/NIM (0 V / -0.8 V)
CG648	ECL (V_{ee}<0, V_{cc}=0)
CG649	LVDS

The CG640 +5 V CMOS receiver uses the RS-485 clock; all of the other receivers use the LVDS clock. The maximum length of Category-6 cable that may be used with a receiver will depend on the clock frequency and the type of Category-6 cable that is used.

CG640 line receiver

Schematic sheet "CG_LR1B"

The CG640 line receiver converts the RS-485 differential clocks to complementary +5 V CMOS outputs on SMA connectors.

The RS-485 level clock is received on the 7-8 pair of the RJ-45 connector (J400). The differential signal is attenuated and terminated with 100 Ω by R101-R104. Undesired common mode signals are terminated by R105 and C100. The unused LVDS level clocks are terminated by R100. The RS-485 clock is converted to 3.3 V CMOS levels by U101, a dual LVDS to CMOS line receiver. One of the translators in U101 is connected in a non-inverting configuration while the other is connected in an inverting configuration.

The complementary outputs of U400 drive the inputs of the hex buffers, U102 and U103 (CDC329). The six outputs from the two buffers are wired together to drive the SMA output via a 50 Ω source impedance (R117-R122 or R123-R128). The 10.0 Ω resistors (R107, R108, R112 & R113) in series with the Vcc bypass capacitors (C105-C108) reduce output overshoot.

The outputs are intended to drive any length of un-terminated 50 Ω cable. The reflection from the unterminated end is reverse terminated by the output's 50 Ω impedance. The resistors in the ground leads of U102 & U103 allow the source impedance for logic "0" outputs to be matched to the source impedance of logic "1" outputs, allowing for a high return loss for both levels.Terminating the outputs will not damage the module, but doing so will reduce the amplitude of the outputs by a factor of 2×.

CG641 and CG642 line receivers

Schematic sheet "CG_LR2B"

The CG641 line receiver converts the LVDS differential clocks to complementary +3.3 V CMOS outputs on SMA connectors. The CG642 line receiver converts the LVDS differential clocks to complementary +2.5 V CMOS outputs on SMA connectors.

The LVDS level clock is received on the 1-2 pair of the RJ-45 connector, J200. The differential signal is terminated with 100 Ω by two resistor networks, N200 and N201. Undesired common mode signals are terminated by the same networks together with C207 and C208. The unused RS-485 level clocks on the 7-8 pair are terminated by R200. The LVDS clocks are converted to complementary 3.3 V CMOS levels by U201 and U202, which are dual LVDS line receivers.

The complementary outputs of U201 and U202 drive the SMA outputs via a resistor network. The resistor network provides a 50 Ω source impedance to reverse terminate reflected signal. The resistor network also provides attenuation in the CG642, which provides 2.5 V CMOS output levels.

The outputs are intended to drive any length of un-terminated 50 Ω cable. The reflection from the unterminated end is reverse terminated by the output's 50 Ω impedance. Terminating the outputs will not damage the module, but doing so will reduce the amplitude of the outputs by a factor of 2×.

CG643-CG645 line receivers

Schematic sheet "CG_LR3B"

The CG643-CG645 line receivers convert differential LVDS clocks to complementary PECL outputs on SMA connectors. These three line receivers use the same PCB and circuit design. The voltage source for the logic "1" level (U300) is set for a particular output logic level, as is the magnitude of the switched current which controls the amplitude of the logic transition.

The LVDS level clock is received on the 1-2 pair of the RJ-45 connector, J300. The differential signal is (primarily) terminated by R302 and R303. Undesired common mode signals are terminated by R304 and C323. The unused RS-485 level clocks are terminated by R300.

The LVDS clock input is AC coupled to an ECL line receiver, U303. The clocks' DC levels are summed with the AC levels by the (slow) differential amplifiers U302A and U302B. The output of the line receiver is passed to a laser diode driver, U304 a MAX3737, which provides fast (≈ 60 ps), switched, differential, programmable current sources to drive the SMA outputs.

The MAX3737 has other features which are not used here but which need to be accommodated so as to avoid apparent "fault" conditions. The transistor Q300 imitates a laser diode's photo monitor by providing small current that increases with the MAX3737's bias current generator. U305 provides a reset to U304 in the case that a fault should occur. The magnitude of the current switched by U304 is controlled by R308.

Both SMA outputs should be terminated with 50 Ω loads. (Except for the CG643, which provides +5 V PECL level outputs into unterminated 50 Ω cables.)

CG646 and CG647 line receivers

Schematic sheet "CG_LR4B"

The CG646-CG647 line receivers convert differential LVDS clocks to complementary RF, CML, or NIM outputs on SMA connectors. These two line receivers use the same PCB and circuit design. The voltage source for the logic "1" level is set for a particular output logic level, as is the magnitude of the switched current which controls the amplitude of the logic transition.

The LVDS level clock is received on the 1-2 pair of the RJ-45 connector, J400. The differential signal is (primarily) terminated by R425 and R426. Undesired common mode signals are terminated by R424 and C419. The unused RS-485 level clocks are terminated by R400.

The LVDS clock input is AC coupled to an ECL line receiver, U401. The clocks' DC levels are summed with the AC levels by the (slow) differential amplifiers U400A and U400B. The output of the line receiver is passed to a laser diode driver, U403 a MAX3737, which provides fast (≈ 60 ps), switched, differential, programmable current sources to drive the SMA outputs.

The MAX3737 has other features which are not used here but which need to be accommodated so as to avoid apparent "fault" conditions. The transistor Q400 imitates a laser diode's photo monitor by providing small current that increases with the MAX3737's bias current generator. U404 provides a reset to U403 in the case that a fault should occur. The magnitude of the current switched by U403 is controlled by R413.

Both SMA outputs should be terminated with 50 Ω loads.

CG648 line receiver

Schematic sheet "CG_LR5B"

The CG648 line receivers convert differential LVDS clocks to complementary negative ECL outputs on SMA connectors.

The LVDS level clock is received on the 1-2 pair of the RJ-45 connector, J500. The differential signal is (primarily) terminated by R502 and R503. Undesired common mode signals are terminated by R504 and C501. The unused RS-485 level clocks are terminated by R500.

The LVDS clock input is AC coupled to an ECL line receiver, U501. The clocks' DC levels are summed with the AC levels by the (slow) differential amplifiers U500A and U500B. The output of the line receiver is passed to a laser diode driver, U503 a MAX3737, which provides fast (≈ 60 ps), switched, differential, programmable current sources to drive the SMA outputs.

The MAX3737 has other features which are not used here but which need to be accommodated so as to avoid apparent "fault" conditions. The transistor Q500 imitates a laser diode's photo monitor by providing small current that increases with the MAX3737's bias current generator. U504 provides a reset to U503 in the case that a

fault should occur. The magnitude of the current switched by U503 is controlled by R510.

Both SMA outputs should be terminated with 50 Ω loads.

CG649 line receiver

Schematic sheet "CG_LR6B"

The CG649 line receiver reconstructs the LVDS differential clocks to provide complementary LVDS outputs on SMA connectors.

The LVDS level clock is received on the 1-2 pair of the RJ-45 connector, J600. The differential signal is (primarily) terminated by R602 and R603. Undesired common mode signals are terminated by R604 and C601. The unused RS-485 level clocks are terminated by R600.

The LVDS clock input is AC coupled to an ECL line receiver, U602. The clocks' DC levels are summed with the AC levels by the (slow) differential amplifiers U601A and U601B. The open emitter outputs of U602 are biased on and terminated by N601 and subsequently drive the inputs to U603. The PECL outputs of U603 are converted to LVDS levels by the resistor network R609-R614, which also provides a 50 Ω source impedance to drive the SMA outputs. Both U602 and U603 are powered by the low dropout regulator U600, which provides +3.3 V.

The SMA outputs are intended to drive 50 Ω loads to ground. Both outputs should be terminated. (Without a terminator, the open emitter outputs of U202 will be biased "off", and there will be no clock at the SMA output.)

Parts List

Motherboard Assembly

C 100	5-00387-552	1000P	Capacitor, Chip (SMT1206), 50V, 5%, NPO
C 101	5-00368-552	27P	Capacitor, Chip (SMT1206), 50V, 5%, NPO
C 102	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 103	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 104	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 105	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 106	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 107	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 108	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 109	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 110	5-00611-578	4.7U - 16V X5R	SMT Ceramic Cap, all sizes
C 111	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 112	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 113	5-00056-512	.1U	Cap, Stacked Metal Film 50V 5% -40/+85c
C 114	5-00387-552	1000P	Capacitor, Chip (SMT1206), 50V, 5%, NPO
C 115	5-00056-512	.1U	Cap, Stacked Metal Film 50V 5% -40/+85c
C 116	5-00387-552	1000P	Capacitor, Chip (SMT1206), 50V, 5%, NPO
C 117	5-00060-512	1.0U	Cap, Stacked Metal Film 50V 5% -40/+85c
C 118	5-00298-568	.01U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 119	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 120	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 121	5-00372-552	56P	Capacitor, Chip (SMT1206), 50V, 5%, NPO
C 122	5-00383-552	470P	Capacitor, Chip (SMT1206), 50V, 5%, NPO
C 123	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 124	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 125	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 126	5-00372-552	56P	Capacitor, Chip (SMT1206), 50V, 5%, NPO
C 127	5-00372-552	56P	Capacitor, Chip (SMT1206), 50V, 5%, NPO
C 128	5-00379-552	220P	Capacitor, Chip (SMT1206), 50V, 5%, NPO
C 129	5-00369-552	33P	Capacitor, Chip (SMT1206), 50V, 5%, NPO
C 130	5-00379-552	220P	Capacitor, Chip (SMT1206), 50V, 5%, NPO
C 131	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 132	5-00611-578	4.7U - 16V X5R	SMT Ceramic Cap, all sizes
C 133	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 134	5-00363-552	10P	Capacitor, Chip (SMT1206), 50V, 5%, NPO
C 135	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 136	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 137	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 138	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 200	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 201	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 202	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 203	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 204	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 205	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 206	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 207	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 208	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 209	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 210	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 211	5-00298-568	.01U	Cap, Ceramic 50V SMT (1206) +/-10% X7R

C 212	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 213	5-00368-552	27P	Capacitor, Chip (SMT1206), 50V, 5%, NPO
C 214	5-00368-552	27P	Capacitor, Chip (SMT1206), 50V, 5%, NPO
C 216	5-00368-552	27P	Capacitor, Chip (SMT1206), 50V, 5%, NPO
C 217	5-00368-552	27P	Capacitor, Chip (SMT1206), 50V, 5%, NPO
C 218	5-00363-552	10P	Capacitor, Chip (SMT1206), 50V, 5%, NPO
C 237	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 238	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 239	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 240	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 241	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 242	5-00371-552	47P	Capacitor, Chip (SMT1206), 50V, 5%, NPO
C 243	5-00379-552	220P	Capacitor, Chip (SMT1206), 50V, 5%, NPO
C 244	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 245	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 246	5-00611-578	4.7U - 16V X5R	SMT Ceramic Cap, all sizes
C 247	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 248	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 249	5-00623-554	1UF / 63V	Capacitor, Polypropylene, Radial
C 250	5-00623-554	1UF / 63V	Capacitor, Polypropylene, Radial
C 251	5-00387-552	1000P	Capacitor, Chip (SMT1206), 50V, 5%, NPO
C 252	5-00387-552	1000P	Capacitor, Chip (SMT1206), 50V, 5%, NPO
C 253	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 254	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 255	5-00611-578	4.7U - 16V X5R	SMT Ceramic Cap, all sizes
C 256	5-00387-552	1000P	Capacitor, Chip (SMT1206), 50V, 5%, NPO
C 257	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 258	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 259	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 260	5-00387-552	1000P	Capacitor, Chip (SMT1206), 50V, 5%, NPO
C 261	5-00371-552	47P	Capacitor, Chip (SMT1206), 50V, 5%, NPO
C 262	5-00379-552	220P	Capacitor, Chip (SMT1206), 50V, 5%, NPO
C 263	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 264	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 265	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 266	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 267	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 268	5-00363-552	10P	Capacitor, Chip (SMT1206), 50V, 5%, NPO
C 270	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 271	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 272	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 273	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 274	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 300	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 301	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 302	5-00371-552	47P	Capacitor, Chip (SMT1206), 50V, 5%, NPO
C 303	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 304	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 305	5-00375-552	100P	Capacitor, Chip (SMT1206), 50V, 5%, NPO
C 307	5-00298-568	.01U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 308	5-00393-552	3300P	Capacitor, Chip (SMT1206), 50V, 5%, NPO
C 310	5-00056-512	.1U	Cap, Stacked Metal Film 50V 5% -40/+85c
C 311	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 313	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 315	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 316	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 319	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 320	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 322	5-00611-578	4.7U - 16V X5R	SMT Ceramic Cap, all sizes
C 323	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 324	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 325	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R

C 326	5-00375-552	100P	Capacitor, Chip (SMT1206), 50V, 5%, NPO
C 327	5-00375-552	100P	Capacitor, Chip (SMT1206), 50V, 5%, NPO
C 328	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 329	5-00393-552	3300P	Capacitor, Chip (SMT1206), 50V, 5%, NPO
C 330	5-00059-512	.47U	Cap, Stacked Metal Film 50V 5% -40/+85c
C 331	5-00318-569	2.2U/T35	Cap, Tantalum, SMT (all case sizes)
C 332	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 333	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 334	5-00393-552	3300P	Capacitor, Chip (SMT1206), 50V, 5%, NPO
C 335	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 336	5-00318-569	2.2U/T35	Cap, Tantalum, SMT (all case sizes)
C 338	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 339	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 340	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 342	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 343	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 344	5-00298-568	.01U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 345	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 346	5-00611-578	4.7U - 16V X5R	SMT Ceramic Cap, all sizes
C 347	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 348	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 349	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 350	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 400	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 401	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 402	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 403	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 404	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 406	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 407	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 408	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 409	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 410	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 411	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 412	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 413	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 414	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 415	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 416	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 417	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 418	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 419	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 420	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 421	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 422	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 423	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 424	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 425	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 426	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 427	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 428	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 500	5-00318-569	2.2U/T35	Cap, Tantalum, SMT (all case sizes)
C 502	5-00060-512	1.0U	Cap, Stacked Metal Film 50V 5% -40/+85c
C 503	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 504	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 505	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 506	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 507	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 509	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 510	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 511	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 512	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R

C 513	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 514	5-00516-526	330U HIGH RIPPL	Capacitor, Electrolytic, 35V, 20%, Rad
C 515	5-00611-578	4.7U - 16V X5R	SMT Ceramic Cap, all sizes
C 516	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 517	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 518	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 519	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 520	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 521	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 522	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 523	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 600	5-00318-569	2.2U/T35	Cap, Tantalum, SMT (all case sizes)
C 601	5-00318-569	2.2U/T35	Cap, Tantalum, SMT (all case sizes)
C 602	5-00318-569	2.2U/T35	Cap, Tantalum, SMT (all case sizes)
C 603	5-00318-569	2.2U/T35	Cap, Tantalum, SMT (all case sizes)
C 604	5-00318-569	2.2U/T35	Cap, Tantalum, SMT (all case sizes)
C 605	5-00318-569	2.2U/T35	Cap, Tantalum, SMT (all case sizes)
C 606	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 607	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 608	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 609	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 610	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 611	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 612	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 613	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 614	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 615	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 616	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 617	5-00387-552	1000P	Capacitor, Chip (SMT1206), 50V, 5%, NPO
C 618	5-00318-569	2.2U/T35	Cap, Tantalum, SMT (all case sizes)
C 619	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 622	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 623	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 624	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 626	5-00387-552	1000P	Capacitor, Chip (SMT1206), 50V, 5%, NPO
C 627	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 628	5-00318-569	2.2U/T35	Cap, Tantalum, SMT (all case sizes)
C 629	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 630	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
D 100	3-00803-360	MMBV609	Integrated Circuit (Surface Mount Pkg)
D 101	3-00538-360	MMBD352L	Integrated Circuit (Surface Mount Pkg)
D 200	3-00803-360	MMBV609	Integrated Circuit (Surface Mount Pkg)
D 201	3-00803-360	MMBV609	Integrated Circuit (Surface Mount Pkg)
D 202	3-00538-360	MMBD352L	Integrated Circuit (Surface Mount Pkg)
D 203	3-00538-360	MMBD352L	Integrated Circuit (Surface Mount Pkg)
D 204	3-00538-360	MMBD352L	Integrated Circuit (Surface Mount Pkg)
D 300	3-00538-360	MMBD352L	Integrated Circuit (Surface Mount Pkg)
D 301	3-00538-360	MMBD352L	Integrated Circuit (Surface Mount Pkg)
D 302	3-00896-301	BAV99	Diode
D 600	3-00011-303	RED	LED, T1 Package
J 100	1-00579-120	227677-1	Connector, BNC
J 101	1-00579-120	227677-1	Connector, BNC
J 300	1-00579-120	227677-1	Connector, BNC
J 400	1-00558-131	HEADER10X2	Connector, Female
J 401	1-00551-131	2MM 10PIN	Connector, Female
J 500	1-00289-130	6 PIN DI TSW 07	Connector, Male
J 501	1-00038-130	40 PIN DIL	Connector, Male
J 600	1-00555-133	10M156(LONG)	Connector, Male, Right Angle
J 602	1-00160-162	IEEE488/STAND.	Connector, IEEE488, Standard, R/A, Femal
J 603	1-01031-160	DEKL-9SAT-E	Connector, D-Sub, Right Angle PC, Female
J 604	1-00518-100	RJ-45S	Connector, Misc.
L 102	6-00236-631	FR47	Ferrite bead, SMT

L 103	6-00650-609	.47UH - SMT	Inductor, Fixed, SMT
L 104	6-00651-609	.82UH - SMT	Inductor, Fixed, SMT
L 105	6-00236-631	FR47	Ferrite bead, SMT
L 106	6-00236-631	FR47	Ferrite bead, SMT
L 107	6-00236-631	FR47	Ferrite bead, SMT
L 200	6-00236-631	FR47	Ferrite bead, SMT
L 201	6-00236-631	FR47	Ferrite bead, SMT
L 202	6-00669-609	3.3UH - S1210	Inductor, Fixed, SMT
L 203	6-00670-609	3.9UH - S1210	Inductor, Fixed, SMT
L 204	6-00669-609	3.3UH - S1210	Inductor, Fixed, SMT
L 205	6-00236-631	FR47	Ferrite bead, SMT
L 206	6-00236-631	FR47	Ferrite bead, SMT
L 207	6-00236-631	FR47	Ferrite bead, SMT
L 210	6-00659-609	22UH -SMT	Inductor, Fixed, SMT
L 211	6-00659-609	22UH -SMT	Inductor, Fixed, SMT
L 212	6-00236-631	FR47	Ferrite bead, SMT
L 300	6-00659-609	22UH -SMT	Inductor, Fixed, SMT
L 301	6-00659-609	22UH -SMT	Inductor, Fixed, SMT
L 302	6-00236-631	FR47	Ferrite bead, SMT
L 303	6-00236-631	FR47	Ferrite bead, SMT
L 304	6-00236-631	FR47	Ferrite bead, SMT
L 305	6-00236-631	FR47	Ferrite bead, SMT
L 400	6-00236-631	FR47	Ferrite bead, SMT
L 401	6-00236-631	FR47	Ferrite bead, SMT
L 402	6-00236-631	FR47	Ferrite bead, SMT
L 500	6-00236-631	FR47	Ferrite bead, SMT
L 501	6-00647-601	47UH	Inductor
L 502	6-00236-631	FR47	Ferrite bead, SMT
L 600	6-00236-631	FR47	Ferrite bead, SMT
L 601	6-00236-631	FR47	Ferrite bead, SMT
L 602	6-00236-631	FR47	Ferrite bead, SMT
L 603	6-00236-631	FR47	Ferrite bead, SMT
L 604	6-00236-631	FR47	Ferrite bead, SMT
L 605	6-00236-631	FR47	Ferrite bead, SMT
L 606	6-00236-631	FR47	Ferrite bead, SMT
N 500	4-01716-463	270X4	Resistor network, SMT, Leadless
N 501	4-01716-463	270X4	Resistor network, SMT, Leadless
N 502	4-01716-463	270X4	Resistor network, SMT, Leadless
N 503	4-01716-463	270X4	Resistor network, SMT, Leadless
N 504	4-01715-463	15X4	Resistor network, SMT, Leadless
N 505	4-01715-463	15X4	Resistor network, SMT, Leadless
N 506	4-01715-463	15X4	Resistor network, SMT, Leadless
PC1	7-01582-701	CG635 MAIN BD	Printed Circuit Board
Q 100	3-00808-360	MMBT5179	Integrated Circuit (Surface Mount Pkg)
Q 201	3-00808-360	MMBT5179	Integrated Circuit (Surface Mount Pkg)
Q 202	3-00808-360	MMBT5179	Integrated Circuit (Surface Mount Pkg)
Q 400	3-01214-360	BFT92	Integrated Circuit (Surface Mount Pkg)
Q 500	3-01210-360	BC817	Integrated Circuit (Surface Mount Pkg)
Q 501	3-01210-360	BC817	Integrated Circuit (Surface Mount Pkg)
Q 502	3-01210-360	BC817	Integrated Circuit (Surface Mount Pkg)
Q 503	3-01210-360	BC817	Integrated Circuit (Surface Mount Pkg)
Q 504	3-01210-360	BC817	Integrated Circuit (Surface Mount Pkg)
Q 505	3-01210-360	BC817	Integrated Circuit (Surface Mount Pkg)
Q 506	3-01210-360	BC817	Integrated Circuit (Surface Mount Pkg)
Q 507	3-01209-360	BC807	Integrated Circuit (Surface Mount Pkg)
Q 508	3-01209-360	BC807	Integrated Circuit (Surface Mount Pkg)
Q 509	3-01209-360	BC807	Integrated Circuit (Surface Mount Pkg)
Q 510	3-01209-360	BC807	Integrated Circuit (Surface Mount Pkg)
Q 511	3-01209-360	BC807	Integrated Circuit (Surface Mount Pkg)
Q 512	3-01209-360	BC807	Integrated Circuit (Surface Mount Pkg)
Q 513	3-01210-360	BC817	Integrated Circuit (Surface Mount Pkg)
R 100	4-00992-462	49.9	Thin Film, 1%, 50 ppm, MELF Resistor

R 101	4-01059-462	249	Thin Film, 1%, 50 ppm, MELF Resistor
R 102	4-01184-462	4.99K	Thin Film, 1%, 50 ppm, MELF Resistor
R 103	4-00992-462	49.9	Thin Film, 1%, 50 ppm, MELF Resistor
R 104	4-00992-462	49.9	Thin Film, 1%, 50 ppm, MELF Resistor
R 105	4-01184-462	4.99K	Thin Film, 1%, 50 ppm, MELF Resistor
R 106	4-00992-462	49.9	Thin Film, 1%, 50 ppm, MELF Resistor
R 107	4-01503-461	10K	Thick Film, 5%, 200 ppm, Chip Resistor
R 108	4-01503-461	10K	Thick Film, 5%, 200 ppm, Chip Resistor
R 109	4-01503-461	10K	Thick Film, 5%, 200 ppm, Chip Resistor
R 110	4-01503-461	10K	Thick Film, 5%, 200 ppm, Chip Resistor
R 111	4-01059-462	249	Thin Film, 1%, 50 ppm, MELF Resistor
R 112	4-01059-462	249	Thin Film, 1%, 50 ppm, MELF Resistor
R 113	4-01155-462	2.49K	Thin Film, 1%, 50 ppm, MELF Resistor
R 114	4-01155-462	2.49K	Thin Film, 1%, 50 ppm, MELF Resistor
R 115	4-01251-462	24.9K	Thin Film, 1%, 50 ppm, MELF Resistor
R 116	4-01251-462	24.9K	Thin Film, 1%, 50 ppm, MELF Resistor
R 117	4-01309-462	100K	Thin Film, 1%, 50 ppm, MELF Resistor
R 118	4-01271-462	40.2K	Thin Film, 1%, 50 ppm, MELF Resistor
R 119	4-01405-462	1.00M	Thin Film, 1%, 50 ppm, MELF Resistor
R 120	4-01376-462	499K	Thin Film, 1%, 50 ppm, MELF Resistor
R 121	4-01251-462	24.9K	Thin Film, 1%, 50 ppm, MELF Resistor
R 122	4-01155-462	2.49K	Thin Film, 1%, 50 ppm, MELF Resistor
R 123	4-01280-462	49.9K	Thin Film, 1%, 50 ppm, MELF Resistor
R 124	4-01309-462	100K	Thin Film, 1%, 50 ppm, MELF Resistor
R 125	4-01309-462	100K	Thin Film, 1%, 50 ppm, MELF Resistor
R 126	4-01527-461	100K	Thick Film, 5%, 200 ppm, Chip Resistor
R 127	4-01163-462	3.01K	Thin Film, 1%, 50 ppm, MELF Resistor
R 128	4-01021-462	100	Thin Film, 1%, 50 ppm, MELF Resistor
R 129	4-00963-462	24.9	Thin Film, 1%, 50 ppm, MELF Resistor
R 130	4-01059-462	249	Thin Film, 1%, 50 ppm, MELF Resistor
R 131	4-01059-462	249	Thin Film, 1%, 50 ppm, MELF Resistor
R 132	4-01447-461	47	Thick Film, 5%, 200 ppm, Chip Resistor
R 134	4-01447-461	47	Thick Film, 5%, 200 ppm, Chip Resistor
R 136	4-01447-461	47	Thick Film, 5%, 200 ppm, Chip Resistor
R 138	4-01479-461	1.0K	Thick Film, 5%, 200 ppm, Chip Resistor
R 139	4-01280-462	49.9K	Thin Film, 1%, 50 ppm, MELF Resistor
R 140	4-01280-462	49.9K	Thin Film, 1%, 50 ppm, MELF Resistor
R 141	4-01251-462	24.9K	Thin Film, 1%, 50 ppm, MELF Resistor
R 142	4-00992-462	49.9	Thin Film, 1%, 50 ppm, MELF Resistor
R 143	4-01021-462	100	Thin Film, 1%, 50 ppm, MELF Resistor
R 144	4-01021-462	100	Thin Film, 1%, 50 ppm, MELF Resistor
R 200	4-01128-462	1.30K	Thin Film, 1%, 50 ppm, MELF Resistor
R 201	4-01050-462	200	Thin Film, 1%, 50 ppm, MELF Resistor
R 202	4-01050-462	200	Thin Film, 1%, 50 ppm, MELF Resistor
R 203	4-01175-462	4.02K	Thin Film, 1%, 50 ppm, MELF Resistor
R 205	4-01079-462	402	Thin Film, 1%, 50 ppm, MELF Resistor
R 207	4-01447-461	47	Thick Film, 5%, 200 ppm, Chip Resistor
R 208	4-01280-462	49.9K	Thin Film, 1%, 50 ppm, MELF Resistor
R 209	4-01309-462	100K	Thin Film, 1%, 50 ppm, MELF Resistor
R 210	4-01338-462	200K	Thin Film, 1%, 50 ppm, MELF Resistor
R 211	4-01527-461	100K	Thick Film, 5%, 200 ppm, Chip Resistor
R 212	4-01184-462	4.99K	Thin Film, 1%, 50 ppm, MELF Resistor
R 213	4-01021-462	100	Thin Film, 1%, 50 ppm, MELF Resistor
R 214	4-00963-462	24.9	Thin Film, 1%, 50 ppm, MELF Resistor
R 216	4-01447-461	47	Thick Film, 5%, 200 ppm, Chip Resistor
R 217	4-01155-462	2.49K	Thin Film, 1%, 50 ppm, MELF Resistor
R 218	4-01155-462	2.49K	Thin Film, 1%, 50 ppm, MELF Resistor
R 219	4-01021-462	100	Thin Film, 1%, 50 ppm, MELF Resistor
R 220	4-01021-462	100	Thin Film, 1%, 50 ppm, MELF Resistor
R 221	4-01309-462	100K	Thin Film, 1%, 50 ppm, MELF Resistor
R 222	4-01309-462	100K	Thin Film, 1%, 50 ppm, MELF Resistor
R 223	4-01213-462	10.0K	Thin Film, 1%, 50 ppm, MELF Resistor

R 224	4-01213-462	10.0K	Thin Film, 1%, 50 ppm, MELF Resistor
R 225	4-01021-462	100	Thin Film, 1%, 50 ppm, MELF Resistor
R 226	4-01021-462	100	Thin Film, 1%, 50 ppm, MELF Resistor
R 227	4-01309-462	100K	Thin Film, 1%, 50 ppm, MELF Resistor
R 228	4-01271-462	40.2K	Thin Film, 1%, 50 ppm, MELF Resistor
R 229	4-01503-461	10K	Thick Film, 5%, 200 ppm, Chip Resistor
R 230	4-01503-461	10K	Thick Film, 5%, 200 ppm, Chip Resistor
R 238	4-01479-461	1.0K	Thick Film, 5%, 200 ppm, Chip Resistor
R 239	4-01338-462	200K	Thin Film, 1%, 50 ppm, MELF Resistor
R 240	4-01280-462	49.9K	Thin Film, 1%, 50 ppm, MELF Resistor
R 241	4-01309-462	100K	Thin Film, 1%, 50 ppm, MELF Resistor
R 242	4-01527-461	100K	Thick Film, 5%, 200 ppm, Chip Resistor
R 243	4-00963-462	24.9	Thin Film, 1%, 50 ppm, MELF Resistor
R 244	4-01184-462	4.99K	Thin Film, 1%, 50 ppm, MELF Resistor
R 245	4-01021-462	100	Thin Film, 1%, 50 ppm, MELF Resistor
R 246	4-01184-462	4.99K	Thin Film, 1%, 50 ppm, MELF Resistor
R 247	4-00992-462	49.9	Thin Film, 1%, 50 ppm, MELF Resistor
R 248	4-01184-462	4.99K	Thin Film, 1%, 50 ppm, MELF Resistor
R 249	4-00992-462	49.9	Thin Film, 1%, 50 ppm, MELF Resistor
R 251	4-01447-461	47	Thick Film, 5%, 200 ppm, Chip Resistor
R 252	4-01309-462	100K	Thin Film, 1%, 50 ppm, MELF Resistor
R 253	4-01309-462	100K	Thin Film, 1%, 50 ppm, MELF Resistor
R 254	4-01280-462	49.9K	Thin Film, 1%, 50 ppm, MELF Resistor
R 255	4-01079-462	402	Thin Film, 1%, 50 ppm, MELF Resistor
R 256	4-01079-462	402	Thin Film, 1%, 50 ppm, MELF Resistor
R 300	4-01309-462	100K	Thin Film, 1%, 50 ppm, MELF Resistor
R 301	4-01309-462	100K	Thin Film, 1%, 50 ppm, MELF Resistor
R 302	4-01309-462	100K	Thin Film, 1%, 50 ppm, MELF Resistor
R 304	4-01117-462	1.00K	Thin Film, 1%, 50 ppm, MELF Resistor
R 305	4-01117-462	1.00K	Thin Film, 1%, 50 ppm, MELF Resistor
R 307	4-01309-462	100K	Thin Film, 1%, 50 ppm, MELF Resistor
R 308	4-00992-462	49.9	Thin Film, 1%, 50 ppm, MELF Resistor
R 309	4-01021-462	100	Thin Film, 1%, 50 ppm, MELF Resistor
R 311	4-01099-462	649	Thin Film, 1%, 50 ppm, MELF Resistor
R 312	4-01050-462	200	Thin Film, 1%, 50 ppm, MELF Resistor
R 316	4-01088-462	499	Thin Film, 1%, 50 ppm, MELF Resistor
R 317	4-01021-462	100	Thin Film, 1%, 50 ppm, MELF Resistor
R 318	4-01079-462	402	Thin Film, 1%, 50 ppm, MELF Resistor
R 319	4-01447-461	47	Thick Film, 5%, 200 ppm, Chip Resistor
R 320	4-01405-462	1.00M	Thin Film, 1%, 50 ppm, MELF Resistor
R 321	4-01038-462	150	Thin Film, 1%, 50 ppm, MELF Resistor
R 322	4-01021-462	100	Thin Film, 1%, 50 ppm, MELF Resistor
R 323	4-01230-462	15.0K	Thin Film, 1%, 50 ppm, MELF Resistor
R 324	4-01213-462	10.0K	Thin Film, 1%, 50 ppm, MELF Resistor
R 331	4-01527-461	100K	Thick Film, 5%, 200 ppm, Chip Resistor
R 332	4-01309-462	100K	Thin Film, 1%, 50 ppm, MELF Resistor
R 333	4-01309-462	100K	Thin Film, 1%, 50 ppm, MELF Resistor
R 336	4-01184-462	4.99K	Thin Film, 1%, 50 ppm, MELF Resistor
R 337	4-01021-462	100	Thin Film, 1%, 50 ppm, MELF Resistor
R 338	4-01021-462	100	Thin Film, 1%, 50 ppm, MELF Resistor
R 339	4-01213-462	10.0K	Thin Film, 1%, 50 ppm, MELF Resistor
R 340	4-01213-462	10.0K	Thin Film, 1%, 50 ppm, MELF Resistor
R 341	4-01137-462	1.62K	Thin Film, 1%, 50 ppm, MELF Resistor
R 342	4-01108-462	806	Thin Film, 1%, 50 ppm, MELF Resistor
R 343	4-01079-462	402	Thin Film, 1%, 50 ppm, MELF Resistor
R 344	4-01045-462	178	Thin Film, 1%, 50 ppm, MELF Resistor
R 345	4-01009-462	75.0	Thin Film, 1%, 50 ppm, MELF Resistor
R 346	4-01021-462	100	Thin Film, 1%, 50 ppm, MELF Resistor
R 347	4-01117-462	1.00K	Thin Film, 1%, 50 ppm, MELF Resistor
R 348	4-00992-462	49.9	Thin Film, 1%, 50 ppm, MELF Resistor
R 349	4-00992-462	49.9	Thin Film, 1%, 50 ppm, MELF Resistor
R 354	4-00963-462	24.9	Thin Film, 1%, 50 ppm, MELF Resistor

R 355	4-00963-462	24.9	Thin Film, 1%, 50 ppm, MELF Resistor
R 356	4-00992-462	49.9	Thin Film, 1%, 50 ppm, MELF Resistor
R 357	4-00992-462	49.9	Thin Film, 1%, 50 ppm, MELF Resistor
R 358	4-00992-462	49.9	Thin Film, 1%, 50 ppm, MELF Resistor
R 359	4-01326-462	150K	Thin Film, 1%, 50 ppm, MELF Resistor
R 360	4-01271-462	40.2K	Thin Film, 1%, 50 ppm, MELF Resistor
R 361	4-00963-462	24.9	Thin Film, 1%, 50 ppm, MELF Resistor
R 362	4-01213-462	10.0K	Thin Film, 1%, 50 ppm, MELF Resistor
R 363	4-01259-462	30.1K	Thin Film, 1%, 50 ppm, MELF Resistor
R 364	4-01213-462	10.0K	Thin Film, 1%, 50 ppm, MELF Resistor
R 365	4-01021-462	100	Thin Film, 1%, 50 ppm, MELF Resistor
R 366	4-01213-462	10.0K	Thin Film, 1%, 50 ppm, MELF Resistor
R 367	4-01117-462	1.00K	Thin Film, 1%, 50 ppm, MELF Resistor
R 368	4-01479-461	1.0K	Thick Film, 5%, 200 ppm, Chip Resistor
R 369	4-01479-461	1.0K	Thick Film, 5%, 200 ppm, Chip Resistor
R 370	4-01117-462	1.00K	Thin Film, 1%, 50 ppm, MELF Resistor
R 371	4-01117-462	1.00K	Thin Film, 1%, 50 ppm, MELF Resistor
R 372	4-01021-462	100	Thin Film, 1%, 50 ppm, MELF Resistor
R 400	4-01447-461	47	Thick Film, 5%, 200 ppm, Chip Resistor
R 401	4-01447-461	47	Thick Film, 5%, 200 ppm, Chip Resistor
R 402	4-01447-461	47	Thick Film, 5%, 200 ppm, Chip Resistor
R 403	4-00971-462	30.1	Thin Film, 1%, 50 ppm, MELF Resistor
R 404	4-00971-462	30.1	Thin Film, 1%, 50 ppm, MELF Resistor
R 405	4-01447-461	47	Thick Film, 5%, 200 ppm, Chip Resistor
R 406	4-01447-461	47	Thick Film, 5%, 200 ppm, Chip Resistor
R 407	4-01447-461	47	Thick Film, 5%, 200 ppm, Chip Resistor
R 408	4-01447-461	47	Thick Film, 5%, 200 ppm, Chip Resistor
R 409	4-01447-461	47	Thick Film, 5%, 200 ppm, Chip Resistor
R 410	4-01447-461	47	Thick Film, 5%, 200 ppm, Chip Resistor
R 411	4-01447-461	47	Thick Film, 5%, 200 ppm, Chip Resistor
R 412	4-01038-462	150	Thin Film, 1%, 50 ppm, MELF Resistor
R 413	4-01038-462	150	Thin Film, 1%, 50 ppm, MELF Resistor
R 414	4-01503-461	10K	Thick Film, 5%, 200 ppm, Chip Resistor
R 415	4-01503-461	10K	Thick Film, 5%, 200 ppm, Chip Resistor
R 417	4-01096-462	604	Thin Film, 1%, 50 ppm, MELF Resistor
R 418	4-01096-462	604	Thin Film, 1%, 50 ppm, MELF Resistor
R 419	4-01050-462	200	Thin Film, 1%, 50 ppm, MELF Resistor
R 420	4-01050-462	200	Thin Film, 1%, 50 ppm, MELF Resistor
R 421	4-01067-462	301	Thin Film, 1%, 50 ppm, MELF Resistor
R 422	4-01067-462	301	Thin Film, 1%, 50 ppm, MELF Resistor
R 431	4-01021-462	100	Thin Film, 1%, 50 ppm, MELF Resistor
R 432	4-01105-462	750	Thin Film, 1%, 50 ppm, MELF Resistor
R 433	4-01088-462	499	Thin Film, 1%, 50 ppm, MELF Resistor
R 434	4-00971-462	30.1	Thin Film, 1%, 50 ppm, MELF Resistor
R 500	4-01117-462	1.00K	Thin Film, 1%, 50 ppm, MELF Resistor
R 501	4-01309-462	100K	Thin Film, 1%, 50 ppm, MELF Resistor
R 502	4-01447-461	47	Thick Film, 5%, 200 ppm, Chip Resistor
R 503	4-01479-461	1.0K	Thick Film, 5%, 200 ppm, Chip Resistor
R 504	4-01309-462	100K	Thin Film, 1%, 50 ppm, MELF Resistor
R 506	4-01213-462	10.0K	Thin Film, 1%, 50 ppm, MELF Resistor
R 507	4-00925-462	10.0	Thin Film, 1%, 50 ppm, MELF Resistor
R 600	4-01503-461	10K	Thick Film, 5%, 200 ppm, Chip Resistor
R 601	4-01238-462	18.2K	Thin Film, 1%, 50 ppm, MELF Resistor
R 602	4-01175-462	4.02K	Thin Film, 1%, 50 ppm, MELF Resistor
R 603	4-01309-462	100K	Thin Film, 1%, 50 ppm, MELF Resistor
R 604	4-01230-462	15.0K	Thin Film, 1%, 50 ppm, MELF Resistor
R 605	4-01503-461	10K	Thick Film, 5%, 200 ppm, Chip Resistor
R 606	4-01479-461	1.0K	Thick Film, 5%, 200 ppm, Chip Resistor
R 607	4-01503-461	10K	Thick Film, 5%, 200 ppm, Chip Resistor
R 608	4-01503-461	10K	Thick Film, 5%, 200 ppm, Chip Resistor
R 609	4-01045-462	178	Thin Film, 1%, 50 ppm, MELF Resistor
R 610	4-01050-462	200	Thin Film, 1%, 50 ppm, MELF Resistor

R 611	4-00983-462	40.2	Thin Film, 1%, 50 ppm, MELF Resistor
R 612	4-00983-462	40.2	Thin Film, 1%, 50 ppm, MELF Resistor
R 616	4-01447-461	47	Thick Film, 5%, 200 ppm, Chip Resistor
R 617	4-01407-461	1.0	Thick Film, 5%, 200 ppm, Chip Resistor
R 618	4-01407-461	1.0	Thick Film, 5%, 200 ppm, Chip Resistor
R 619	4-01117-462	1.00K	Thin Film, 1%, 50 ppm, MELF Resistor
R 620	4-01271-462	40.2K	Thin Film, 1%, 50 ppm, MELF Resistor
R 622	4-00996-462	54.9	Thin Film, 1%, 50 ppm, MELF Resistor
R 623	4-00996-462	54.9	Thin Film, 1%, 50 ppm, MELF Resistor
R 624	4-01090-462	523	Thin Film, 1%, 50 ppm, MELF Resistor
R 625	4-01090-462	523	Thin Film, 1%, 50 ppm, MELF Resistor
R 626	4-01055-462	226	Thin Film, 1%, 50 ppm, MELF Resistor
R 627	4-01050-462	200	Thin Film, 1%, 50 ppm, MELF Resistor
R 634	4-01271-462	40.2K	Thin Film, 1%, 50 ppm, MELF Resistor
R 636	4-01117-462	1.00K	Thin Film, 1%, 50 ppm, MELF Resistor
R 637	4-01407-461	1.0	Thick Film, 5%, 200 ppm, Chip Resistor
R 638	4-01407-461	1.0	Thick Film, 5%, 200 ppm, Chip Resistor
R 639	4-01447-461	47	Thick Film, 5%, 200 ppm, Chip Resistor
R 640	4-01447-461	47	Thick Film, 5%, 200 ppm, Chip Resistor
R 641	4-01419-461	3.3	Thick Film, 5%, 200 ppm, Chip Resistor
R 642	4-01419-461	3.3	Thick Film, 5%, 200 ppm, Chip Resistor
SP500	6-00096-600	MINI	Misc. Components
SW600	2-00023-218	DPDT	Switch, Panel Mount, Power, Rocker
T 100	6-00195-610	10.7 MHZ	Transformer
T 101	6-00195-610	10.7 MHZ	Transformer
T 200	6-00671-610	TC1-1T	Transformer
U 100	3-00653-360	AD8561AR	Integrated Circuit (Surface Mount Pkg)
U 101	3-01269-360	74VHC1GT02	Integrated Circuit (Surface Mount Pkg)
U 102	3-00653-360	AD8561AR	Integrated Circuit (Surface Mount Pkg)
U 103	3-01249-360	74VHC1GT08	Integrated Circuit (Surface Mount Pkg)
U 104	3-01204-360	SN74LVC1G32DBVR	Integrated Circuit (Surface Mount Pkg)
U 105	3-01184-360	LP2985AIM5-3.3	Integrated Circuit (Surface Mount Pkg)
U 106	3-00978-360	74LVC74	Integrated Circuit (Surface Mount Pkg)
U 107	3-01204-360	SN74LVC1G32DBVR	Integrated Circuit (Surface Mount Pkg)
U 108	3-00643-360	DG211BDY	Integrated Circuit (Surface Mount Pkg)
U 109	3-00724-360	LF353	Integrated Circuit (Surface Mount Pkg)
U 110	3-01202-360	SN74LVC1G02DBVR	Integrated Circuit (Surface Mount Pkg)
U 111	3-00773-360	LM358	Integrated Circuit (Surface Mount Pkg)
U 112	3-00653-360	AD8561AR	Integrated Circuit (Surface Mount Pkg)
U 113	3-01271-360	74HCT74	Integrated Circuit (Surface Mount Pkg)
U 114	3-01269-360	74VHC1GT02	Integrated Circuit (Surface Mount Pkg)
U 200	3-01122-360	AD9852AST	Integrated Circuit (Surface Mount Pkg)
U 203	3-00653-360	AD8561AR	Integrated Circuit (Surface Mount Pkg)
U 204	3-00724-360	LF353	Integrated Circuit (Surface Mount Pkg)
U 205	3-00653-360	AD8561AR	Integrated Circuit (Surface Mount Pkg)
U 206	3-01184-360	LP2985AIM5-3.3	Integrated Circuit (Surface Mount Pkg)
U 207	3-00978-360	74LVC74	Integrated Circuit (Surface Mount Pkg)
U 208	3-01204-360	SN74LVC1G32DBVR	Integrated Circuit (Surface Mount Pkg)
U 210	3-00653-360	AD8561AR	Integrated Circuit (Surface Mount Pkg)
U 211	3-01204-360	SN74LVC1G32DBVR	Integrated Circuit (Surface Mount Pkg)
U 212	3-01269-360	74VHC1GT02	Integrated Circuit (Surface Mount Pkg)
U 213	3-01270-360	74VHC1GT32DTTI	Integrated Circuit (Surface Mount Pkg)
U 214	3-01249-360	74VHC1GT08	Integrated Circuit (Surface Mount Pkg)
U 215	3-00773-360	LM358	Integrated Circuit (Surface Mount Pkg)
U 216	3-00773-360	LM358	Integrated Circuit (Surface Mount Pkg)
U 300	3-00581-360	AD822	Integrated Circuit (Surface Mount Pkg)
U 301	3-01249-360	74VHC1GT08	Integrated Circuit (Surface Mount Pkg)
U 302	3-00653-360	AD8561AR	Integrated Circuit (Surface Mount Pkg)
U 303	3-00724-360	LF353	Integrated Circuit (Surface Mount Pkg)
U 304	3-01178-360	ADCMP567BCP	Integrated Circuit (Surface Mount Pkg)
U 305	3-01184-360	LP2985AIM5-3.3	Integrated Circuit (Surface Mount Pkg)
U 306	3-01201-360	74LVC157AD	Integrated Circuit (Surface Mount Pkg)

U 307	3-01179-360	ADF4106BRU	Integrated Circuit (Surface Mount Pkg)
U 308	3-01365-360	DG411DY	Integrated Circuit (Surface Mount Pkg)
U 309	3-01426-360	AD797AR	Integrated Circuit (Surface Mount Pkg)
U 310	6-00975-625	V585ME48	Voltage Controlled Crystal Oscillator
U 311	3-00773-360	LM358	Integrated Circuit (Surface Mount Pkg)
U 400	3-01195-360	MC100EP51D	Integrated Circuit (Surface Mount Pkg)
U 401	3-01189-360	MC100EP016AFA	Integrated Circuit (Surface Mount Pkg)
U 402	3-01195-360	MC100EP51D	Integrated Circuit (Surface Mount Pkg)
U 403	3-01194-360	MC100EP35D	Integrated Circuit (Surface Mount Pkg)
U 404	3-01197-360	MC100EP57DT	Integrated Circuit (Surface Mount Pkg)
U 405	3-01193-360	MC100EP14DT	Integrated Circuit (Surface Mount Pkg)
U 406	3-00751-360	74HC574	Integrated Circuit (Surface Mount Pkg)
U 407	3-01650-360	AD8611AR	Integrated Circuit (Surface Mount Pkg)
U 408	3-00421-340	F107563FN	Integrated Circuit (Thru-hole Pkg)
U 409	3-01382-360	74AC74	Integrated Circuit (Surface Mount Pkg)
U 410	3-01249-360	74VHC1GT08	Integrated Circuit (Surface Mount Pkg)
U 411	3-01202-360	SN74LVC1G02DBVR	Integrated Circuit (Surface Mount Pkg)
U 500	3-01198-360	MC912D60ACPV8	Integrated Circuit (Surface Mount Pkg)
U 501	3-00751-360	74HC574	Integrated Circuit (Surface Mount Pkg)
U 502	3-01206-360	74LVC574ADW	Integrated Circuit (Surface Mount Pkg)
U 503	3-01205-360	74LVC4245ADW	Integrated Circuit (Surface Mount Pkg)
U 504	3-01185-360	LTC2620CGN	Integrated Circuit (Surface Mount Pkg)
U 505	3-01467-360	74HC4538	Integrated Circuit (Surface Mount Pkg)
U 506	3-00751-360	74HC574	Integrated Circuit (Surface Mount Pkg)
U 507	3-00751-360	74HC574	Integrated Circuit (Surface Mount Pkg)
U 508	3-00751-360	74HC574	Integrated Circuit (Surface Mount Pkg)
U 509	3-00751-360	74HC574	Integrated Circuit (Surface Mount Pkg)
U 510	3-00751-360	74HC574	Integrated Circuit (Surface Mount Pkg)
U 511	3-01206-360	74LVC574ADW	Integrated Circuit (Surface Mount Pkg)
U 512	3-01206-360	74LVC574ADW	Integrated Circuit (Surface Mount Pkg)
U 513	3-01186-360	MAX6241BCSA	Integrated Circuit (Surface Mount Pkg)
U 514	3-00581-360	AD822	Integrated Circuit (Surface Mount Pkg)
U 515	3-00903-360	MAX6348UR44	Integrated Circuit (Surface Mount Pkg)
U 516	3-00775-360	LM45CIM3	Integrated Circuit (Surface Mount Pkg)
U 600	3-00728-360	LM393	Integrated Circuit (Surface Mount Pkg)
U 601	3-00914-360	NAT9914	Integrated Circuit (Surface Mount Pkg)
U 602	3-00915-360	75ALS160	Integrated Circuit (Surface Mount Pkg)
U 603	3-00916-360	75ALS161	Integrated Circuit (Surface Mount Pkg)
U 604	3-01468-360	MAX232ACSE	Integrated Circuit (Surface Mount Pkg)
U 605	3-01192-360	MC100EP11D	Integrated Circuit (Surface Mount Pkg)
U 607	3-01188-360	MAX9113ESA	Integrated Circuit (Surface Mount Pkg)
U 611	3-00773-360	LM358	Integrated Circuit (Surface Mount Pkg)
U 612	3-01181-360	IRF7353D2	Integrated Circuit (Surface Mount Pkg)
U 613	3-01180-360	IRF5803D2	Integrated Circuit (Surface Mount Pkg)
Y 100	6-00643-620	20,000,000HZ	Crystal
Y 200	6-00641-620	19,400,000HZ	Crystal
Y 201	6-00642-620	19,440,000HZ	Crystal
Z 0	0-00237-016	F1404	Power Button
Z 0	0-00517-000	BINDING POST	Hardware, Misc.

Output Driver Assembly

C 100	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 101	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 102	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 103	5-00611-578	4.7U - 16V X5R	SMT Ceramic Cap, all sizes
C 104	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 105	5-00611-578	4.7U - 16V X5R	SMT Ceramic Cap, all sizes
C 106	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 107	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 108	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R

C 109	5-00611-578	4.7U - 16V X5R	SMT Ceramic Cap, all sizes
C 110	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 111	5-00399-552	.01U	Capacitor, Chip (SMT1206), 50V, 5%, NPO
C 112	5-00399-552	.01U	Capacitor, Chip (SMT1206), 50V, 5%, NPO
C 113	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 114	5-00375-552	100P	Capacitor, Chip (SMT1206), 50V, 5%, NPO
C 115	5-00375-552	100P	Capacitor, Chip (SMT1206), 50V, 5%, NPO
C 116	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 117	5-00472-569	4.7U/T35	Cap, Tantalum, SMT (all case sizes)
C 118	5-00611-578	4.7U - 16V X5R	SMT Ceramic Cap, all sizes
C 119	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 120	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 121	5-00313-552	1P	Capacitor, Chip (SMT1206), 50V, 5%, NPO
C 122	5-00611-578	4.7U - 16V X5R	SMT Ceramic Cap, all sizes
C 123	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 124	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 125	5-00387-552	1000P	Capacitor, Chip (SMT1206), 50V, 5%, NPO
C 126	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 127	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 128	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 129	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 130	5-00375-552	100P	Capacitor, Chip (SMT1206), 50V, 5%, NPO
C 131	5-00387-552	1000P	Capacitor, Chip (SMT1206), 50V, 5%, NPO
C 132	5-00355-552	2.2P	Capacitor, Chip (SMT1206), 50V, 5%, NPO
C 133	5-00298-568	.01U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 200	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 201	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 202	5-00313-552	1P	Capacitor, Chip (SMT1206), 50V, 5%, NPO
C 203	5-00358-552	3.9P	Capacitor, Chip (SMT1206), 50V, 5%, NPO
C 204	5-00611-578	4.7U - 16V X5R	SMT Ceramic Cap, all sizes
C 205	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 206	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 207	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 208	5-00611-578	4.7U - 16V X5R	SMT Ceramic Cap, all sizes
C 209	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 210	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 211	5-00387-552	1000P	Capacitor, Chip (SMT1206), 50V, 5%, NPO
C 212	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 213	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 214	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 215	5-00611-578	4.7U - 16V X5R	SMT Ceramic Cap, all sizes
C 216	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 217	5-00611-578	4.7U - 16V X5R	SMT Ceramic Cap, all sizes
C 218	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 219	5-00358-552	3.9P	Capacitor, Chip (SMT1206), 50V, 5%, NPO
C 220	5-00375-552	100P	Capacitor, Chip (SMT1206), 50V, 5%, NPO
C 221	5-00375-552	100P	Capacitor, Chip (SMT1206), 50V, 5%, NPO
C 222	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 223	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 224	5-00472-569	4.7U/T35	Cap, Tantalum, SMT (all case sizes)
C 225	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 226	5-00387-552	1000P	Capacitor, Chip (SMT1206), 50V, 5%, NPO
C 227	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
D 200	3-00896-301	BAV99	Diode
J 100	1-00556-130	EDGE20	Connector, Male
J 101	1-00003-120	BNC	Connector, BNC
J 102	1-00003-120	BNC	Connector, BNC
J 200	1-00003-120	BNC	Connector, BNC
L 200	6-00265-609	.018UH - SMT	Inductor, Fixed, SMT
N 100	4-01644-463	10KX8D	Resistor network, SMT, Leadless
N 101	4-00906-463	100X4D	Resistor network, SMT, Leadless
N 102	4-00911-463	4.7KX4D	Resistor network, SMT, Leadless

N 200	4-00906-463	100X4D	Resistor network, SMT, Leadless
PC1	7-01583-701	SCG DRIVER PCB	Printed Circuit Board
Q 100	3-00580-360	MMBT3906LT1	Integrated Circuit (Surface Mount Pkg)
Q 101	3-00601-360	MMBT3904LT1	Integrated Circuit (Surface Mount Pkg)
Q 102	3-00601-360	MMBT3904LT1	Integrated Circuit (Surface Mount Pkg)
Q 103	3-00601-360	MMBT3904LT1	Integrated Circuit (Surface Mount Pkg)
Q 200	3-01214-360	BFT92	Integrated Circuit (Surface Mount Pkg)
Q 201	3-01214-360	BFT92	Integrated Circuit (Surface Mount Pkg)
Q 202	3-00580-360	MMBT3906LT1	Integrated Circuit (Surface Mount Pkg)
Q 203	3-01211-360	BFG31	Integrated Circuit (Surface Mount Pkg)
Q 204	3-01211-360	BFG31	Integrated Circuit (Surface Mount Pkg)
Q 205	3-01212-360	BFG541	Integrated Circuit (Surface Mount Pkg)
Q 206	3-01212-360	BFG541	Integrated Circuit (Surface Mount Pkg)
R 100	4-01213-462	10.0K	Thin Film, 1%, 50 ppm, MELF Resistor
R 101	4-01213-462	10.0K	Thin Film, 1%, 50 ppm, MELF Resistor
R 102	4-01195-462	6.49K	Thin Film, 1%, 50 ppm, MELF Resistor
R 103	4-01215-462	10.5K	Thin Film, 1%, 50 ppm, MELF Resistor
R 104	4-01059-462	249	Thin Film, 1%, 50 ppm, MELF Resistor
R 105	4-01059-462	249	Thin Film, 1%, 50 ppm, MELF Resistor
R 106	4-01213-462	10.0K	Thin Film, 1%, 50 ppm, MELF Resistor
R 107	4-01207-462	8.66K	Thin Film, 1%, 50 ppm, MELF Resistor
R 108	4-01216-462	10.7K	Thin Film, 1%, 50 ppm, MELF Resistor
R 109	4-01213-462	10.0K	Thin Film, 1%, 50 ppm, MELF Resistor
R 110	4-01029-462	121	Thin Film, 1%, 50 ppm, MELF Resistor
R 111	4-01029-462	121	Thin Film, 1%, 50 ppm, MELF Resistor
R 112	4-01117-462	1.00K	Thin Film, 1%, 50 ppm, MELF Resistor
R 113	4-00992-462	49.9	Thin Film, 1%, 50 ppm, MELF Resistor
R 114	4-00992-462	49.9	Thin Film, 1%, 50 ppm, MELF Resistor
R 115	4-00992-462	49.9	Thin Film, 1%, 50 ppm, MELF Resistor
R 116	4-01117-462	1.00K	Thin Film, 1%, 50 ppm, MELF Resistor
R 117	4-01117-462	1.00K	Thin Film, 1%, 50 ppm, MELF Resistor
R 118	4-01067-462	301	Thin Film, 1%, 50 ppm, MELF Resistor
R 119	4-01067-462	301	Thin Film, 1%, 50 ppm, MELF Resistor
R 120	4-01347-462	249K	Thin Film, 1%, 50 ppm, MELF Resistor
R 121	4-01213-462	10.0K	Thin Film, 1%, 50 ppm, MELF Resistor
R 122	4-01221-462	12.1K	Thin Film, 1%, 50 ppm, MELF Resistor
R 123	4-00992-462	49.9	Thin Film, 1%, 50 ppm, MELF Resistor
R 124	4-01734-454	24.9/.5W	Thick Film, 1%, 100ppm, Chip Res.(SMT)
R 125	4-01734-454	24.9/.5W	Thick Film, 1%, 100ppm, Chip Res.(SMT)
R 126	4-01734-454	24.9/.5W	Thick Film, 1%, 100ppm, Chip Res.(SMT)
R 127	4-01734-454	24.9/.5W	Thick Film, 1%, 100ppm, Chip Res.(SMT)
R 128	4-01213-462	10.0K	Thin Film, 1%, 50 ppm, MELF Resistor
R 129	4-01259-462	30.1K	Thin Film, 1%, 50 ppm, MELF Resistor
R 130	4-01059-462	249	Thin Film, 1%, 50 ppm, MELF Resistor
R 131	4-01259-462	30.1K	Thin Film, 1%, 50 ppm, MELF Resistor
R 132	4-01259-462	30.1K	Thin Film, 1%, 50 ppm, MELF Resistor
R 133	4-01259-462	30.1K	Thin Film, 1%, 50 ppm, MELF Resistor
R 134	4-01259-462	30.1K	Thin Film, 1%, 50 ppm, MELF Resistor
R 135	4-01242-462	20.0K	Thin Film, 1%, 50 ppm, MELF Resistor
R 136	4-01242-462	20.0K	Thin Film, 1%, 50 ppm, MELF Resistor
R 137	4-00992-462	49.9	Thin Film, 1%, 50 ppm, MELF Resistor
R 138	4-00992-462	49.9	Thin Film, 1%, 50 ppm, MELF Resistor
R 139	4-01009-462	75.0	Thin Film, 1%, 50 ppm, MELF Resistor
R 200	4-01201-462	7.50K	Thin Film, 1%, 50 ppm, MELF Resistor
R 201	4-01213-462	10.0K	Thin Film, 1%, 50 ppm, MELF Resistor
R 202	4-01201-462	7.50K	Thin Film, 1%, 50 ppm, MELF Resistor
R 203	4-01184-462	4.99K	Thin Film, 1%, 50 ppm, MELF Resistor
R 204	4-01201-462	7.50K	Thin Film, 1%, 50 ppm, MELF Resistor
R 205	4-00992-462	49.9	Thin Film, 1%, 50 ppm, MELF Resistor
R 206	4-00992-462	49.9	Thin Film, 1%, 50 ppm, MELF Resistor
R 207	4-01117-462	1.00K	Thin Film, 1%, 50 ppm, MELF Resistor
R 208	4-01021-462	100	Thin Film, 1%, 50 ppm, MELF Resistor

R 209	4-00992-462	49.9	Thin Film, 1%, 50 ppm, MELF Resistor
R 210	4-00992-462	49.9	Thin Film, 1%, 50 ppm, MELF Resistor
R 211	4-01009-462	75.0	Thin Film, 1%, 50 ppm, MELF Resistor
R 212	4-01192-462	6.04K	Thin Film, 1%, 50 ppm, MELF Resistor
R 213	4-01213-462	10.0K	Thin Film, 1%, 50 ppm, MELF Resistor
R 214	4-01242-462	20.0K	Thin Film, 1%, 50 ppm, MELF Resistor
R 215	4-01263-462	33.2K	Thin Film, 1%, 50 ppm, MELF Resistor
R 216	4-01117-462	1.00K	Thin Film, 1%, 50 ppm, MELF Resistor
R 217	4-01067-462	301	Thin Film, 1%, 50 ppm, MELF Resistor
R 218	4-01067-462	301	Thin Film, 1%, 50 ppm, MELF Resistor
R 219	4-01347-462	249K	Thin Film, 1%, 50 ppm, MELF Resistor
R 220	4-01213-462	10.0K	Thin Film, 1%, 50 ppm, MELF Resistor
R 221	4-01059-462	249	Thin Film, 1%, 50 ppm, MELF Resistor
R 222	4-01140-462	1.74K	Thin Film, 1%, 50 ppm, MELF Resistor
R 223	4-00992-462	49.9	Thin Film, 1%, 50 ppm, MELF Resistor
R 224	4-00992-462	49.9	Thin Film, 1%, 50 ppm, MELF Resistor
R 225	4-00992-462	49.9	Thin Film, 1%, 50 ppm, MELF Resistor
R 226	4-00992-462	49.9	Thin Film, 1%, 50 ppm, MELF Resistor
R 227	4-00992-462	49.9	Thin Film, 1%, 50 ppm, MELF Resistor
R 228	4-00971-462	30.1	Thin Film, 1%, 50 ppm, MELF Resistor
R 229	4-01407-461	1.0	Thick Film, 5%, 200 ppm, Chip Resistor
R 230	4-01407-461	1.0	Thick Film, 5%, 200 ppm, Chip Resistor
R 231	4-01407-461	1.0	Thick Film, 5%, 200 ppm, Chip Resistor
R 232	4-00992-462	49.9	Thin Film, 1%, 50 ppm, MELF Resistor
R 233	4-00954-462	20.0	Thin Film, 1%, 50 ppm, MELF Resistor
R 234	4-00971-462	30.1	Thin Film, 1%, 50 ppm, MELF Resistor
R 235	4-00971-462	30.1	Thin Film, 1%, 50 ppm, MELF Resistor
R 236	4-01059-462	249	Thin Film, 1%, 50 ppm, MELF Resistor
R 237	4-01213-462	10.0K	Thin Film, 1%, 50 ppm, MELF Resistor
R 238	4-00971-462	30.1	Thin Film, 1%, 50 ppm, MELF Resistor
R 239	4-00971-462	30.1	Thin Film, 1%, 50 ppm, MELF Resistor
R 240	4-01059-462	249	Thin Film, 1%, 50 ppm, MELF Resistor
R 241	4-01213-462	10.0K	Thin Film, 1%, 50 ppm, MELF Resistor
R 242	4-00971-462	30.1	Thin Film, 1%, 50 ppm, MELF Resistor
R 243	4-01213-462	10.0K	Thin Film, 1%, 50 ppm, MELF Resistor
R 244	4-01213-462	10.0K	Thin Film, 1%, 50 ppm, MELF Resistor
R 245	4-01292-462	66.5K	Thin Film, 1%, 50 ppm, MELF Resistor
R 246	4-01292-462	66.5K	Thin Film, 1%, 50 ppm, MELF Resistor
R 247	4-00992-462	49.9	Thin Film, 1%, 50 ppm, MELF Resistor
R 248	4-00992-462	49.9	Thin Film, 1%, 50 ppm, MELF Resistor
R 249	4-00992-462	49.9	Thin Film, 1%, 50 ppm, MELF Resistor
R 250	4-01055-462	226	Thin Film, 1%, 50 ppm, MELF Resistor
R 251	4-01055-462	226	Thin Film, 1%, 50 ppm, MELF Resistor
R 252	4-01055-462	226	Thin Film, 1%, 50 ppm, MELF Resistor
R 253	4-00992-462	49.9	Thin Film, 1%, 50 ppm, MELF Resistor
R 254	4-01251-462	24.9K	Thin Film, 1%, 50 ppm, MELF Resistor
R 255	4-01309-462	100K	Thin Film, 1%, 50 ppm, MELF Resistor
R 256	4-01251-462	24.9K	Thin Film, 1%, 50 ppm, MELF Resistor
R 257	6-00236-631	FR47	Ferrite bead, SMT
R 258	4-00925-462	10.0	Thin Film, 1%, 50 ppm, MELF Resistor
R 259	4-00925-462	10.0	Thin Film, 1%, 50 ppm, MELF Resistor
U 100	3-01281-360	LM317MDT	Integrated Circuit (Surface Mount Pkg)
U 101	3-00724-360	LF353	Integrated Circuit (Surface Mount Pkg)
U 102	3-01282-360	LM337KTP	Integrated Circuit (Surface Mount Pkg)
U 103	3-01184-360	LP2985AIM5-3.3	Integrated Circuit (Surface Mount Pkg)
U 104	3-00724-360	LF353	Integrated Circuit (Surface Mount Pkg)
U 105	3-01273-360	MAX3737ETJ	Integrated Circuit (Surface Mount Pkg)
U 106	3-01274-360	74LVC2G14DBVR	Integrated Circuit (Surface Mount Pkg)
U 107	3-00773-360	LM358	Integrated Circuit (Surface Mount Pkg)
U 200	3-00819-360	LM7171AIM	Integrated Circuit (Surface Mount Pkg)
U 201	3-01281-360	LM317MDT	Integrated Circuit (Surface Mount Pkg)
U 202	3-01184-360	LP2985AIM5-3.3	Integrated Circuit (Surface Mount Pkg)

U 203	3-01273-360	MAX3737ETJ	Integrated Circuit (Surface Mount Pkg)
U 204	3-01274-360	74LVC2G14DBVR	Integrated Circuit (Surface Mount Pkg)
U 205	3-00773-360	LM358	Integrated Circuit (Surface Mount Pkg)
Z 0	7-01615-721	CG635	Machined Part

Power Supply Assembly

C 1	5-00612-509	1000U	Capacitor, Electrolytic, 50V, 20%, Rad
C 2	5-00516-526	330U HIGH RIPPL	Capacitor, Electrolytic, 35V, 20%, Rad
C 3	5-00288-528	.01U	Cap, Mono. Ceramic, 50V, 10%, X7R RAD
C 4	5-00516-526	330U HIGH RIPPL	Capacitor, Electrolytic, 35V, 20%, Rad
C 5	5-00516-526	330U HIGH RIPPL	Capacitor, Electrolytic, 35V, 20%, Rad
C 6	5-00023-529	.1U	Cap, Monolythic Ceramic, 50V, 20%, Z5U
C 7	5-00288-528	.01U	Cap, Mono. Ceramic, 50V, 10%, X7R RAD
C 8	5-00023-529	.1U	Cap, Monolythic Ceramic, 50V, 20%, Z5U
C 9	5-00049-566	.001U	Cap, Polyester Film 50V 5% -40/+85c Rad
C 10	5-00612-509	1000U	Capacitor, Electrolytic, 50V, 20%, Rad
C 11	5-00143-536	1200P	Capacitor, Ceramic, 1000 VDCW
C 12	5-00516-526	330U HIGH RIPPL	Capacitor, Electrolytic, 35V, 20%, Rad
C 13	5-00102-517	4.7U	Capacitor, Tantalum, 35V, 20%, Rad
C 14	5-00143-536	1200P	Capacitor, Ceramic, 1000 VDCW
C 15	5-00516-526	330U HIGH RIPPL	Capacitor, Electrolytic, 35V, 20%, Rad
C 16	5-00102-517	4.7U	Capacitor, Tantalum, 35V, 20%, Rad
C 17	5-00143-536	1200P	Capacitor, Ceramic, 1000 VDCW
C 18	5-00516-526	330U HIGH RIPPL	Capacitor, Electrolytic, 35V, 20%, Rad
C 19	5-00102-517	4.7U	Capacitor, Tantalum, 35V, 20%, Rad
C 20	5-00102-517	4.7U	Capacitor, Tantalum, 35V, 20%, Rad
C 21	5-00143-536	1200P	Capacitor, Ceramic, 1000 VDCW
C 22	5-00516-526	330U HIGH RIPPL	Capacitor, Electrolytic, 35V, 20%, Rad
C 23	5-00102-517	4.7U	Capacitor, Tantalum, 35V, 20%, Rad
D 1	3-00226-301	1N5822	Diode
D 2	3-00226-301	1N5822	Diode
D 3	3-01208-301	MUR220	Diode
D 4	3-01208-301	MUR220	Diode
D 5	3-01208-301	MUR220	Diode
D 6	3-01208-301	MUR220	Diode
D 7	3-01208-301	MUR220	Diode
D 8	3-01208-301	MUR220	Diode
D 9	3-01208-301	MUR220	Diode
D 10	3-01208-301	MUR220	Diode
D 11	3-00516-301	1N5819	Diode
D 12	3-00516-301	1N5819	Diode
D 13	3-00516-301	1N5819	Diode
D 14	3-00516-301	1N5819	Diode
D 15	3-00516-301	1N5819	Diode
D 16	3-00516-301	1N5819	Diode
D 17	3-00011-303	RED	LED, T1 Package
J 1	1-00250-116	2 PIN, WHITE	Header, Amp, MTA-156
J 2	1-00554-150	HEADER10	Socket, THRU-HOLE
J 5	0-00176-031	4-40 X 1/4	Standoff
L 1	6-00646-601	10UH	Inductor
L 2	6-00647-601	47UH	Inductor
L 3	6-00648-601	54.81UH	Inductor
L 4	6-00646-601	10UH	Inductor
L 5	6-00647-601	47UH	Inductor
L 6	6-00647-601	47UH	Inductor
L 7	6-00646-601	10UH	Inductor
L 8	6-00646-601	10UH	Inductor
L 9	6-00646-601	10UH	Inductor
N 1	4-00244-421	10KX4	Res. Network, SIP, 1/4W,2% (Isolated)

PC1	7-01585-701	SCG P/S PCB	Printed Circuit Board
Q 1	3-00283-340	IRF530/IRF532	Integrated Circuit (Thru-hole Pkg)
Q 2	3-00283-340	IRF530/IRF532	Integrated Circuit (Thru-hole Pkg)
R 1	4-00138-407	10.0K	Resistor, Metal Film, 1/8W, 1%, 50PPM
R 2	4-00142-407	100K	Resistor, Metal Film, 1/8W, 1%, 50PPM
R 3	4-00347-407	7.50K	Resistor, Metal Film, 1/8W, 1%, 50PPM
R 4	4-00141-407	100	Resistor, Metal Film, 1/8W, 1%, 50PPM
R 5	4-00920-458	0.47/2W	Resistor, Metal Oxide
R 6	4-00920-458	0.47/2W	Resistor, Metal Oxide
R 7	4-00080-401	47	Resistor, Carbon Film, 1/4W, 5%
R 8	4-00080-401	47	Resistor, Carbon Film, 1/4W, 5%
T 1	6-00660-615	CG635 P/S	Power Supply
U 1	3-01182-360	LM2676T-3.3	Integrated Circuit (Surface Mount Pkg)
U 2	3-00114-329	7815	Voltage Reg., TO-220 (TAB) Package
U 3	3-00143-340	LM393	Integrated Circuit (Thru-hole Pkg)
U 4	3-00634-340	3525A	Integrated Circuit (Thru-hole Pkg)
U 5	3-00114-329	7815	Voltage Reg., TO-220 (TAB) Package
U 6	3-00120-329	7915	Voltage Reg., TO-220 (TAB) Package
U 7	3-00112-329	7805	Voltage Reg., TO-220 (TAB) Package
U 8	3-00112-329	7805	Voltage Reg., TO-220 (TAB) Package
U 9	3-00119-329	7905	Voltage Reg., TO-220 (TAB) Package
Z 0	0-00043-011	4-40 KEP	Nut, Kep
Z 0	0-00050-011	8-32 KEP	Nut, Kep
Z 0	0-00084-032	36154	Termination
Z 0	0-00177-002	6ESRM-3	Power Entry Hardware
Z 0	0-00185-021	6-32X3/8PP	Screw, Panhead Phillips
Z 0	0-00187-021	4-40X1/4PP	Screw, Panhead Phillips
Z 0	0-00210-020	4-40X5/16PF	Screw, Flathead Phillips
Z 0	0-00222-021	6-32X1/4PP	Screw, Panhead Phillips
Z 0	0-00231-043	1-32, #4 SHOULD	Washer, nylon
Z 0	0-00243-003	TO-220	Insulators
Z 0	0-00271-000	BUMPER	Hardware, Misc.
Z 0	0-00438-021	4-40X5/16PP	Screw, Panhead Phillips
Z 0	0-00469-070	40MM 12V	Fans, & Hardware
Z 0	0-00471-021	4-40X1"PP	Screw, Panhead Phillips
Z 0	0-00634-032	2-520184-2	Termination
Z 0	0-01011-050	18" BLK #18	Wire #18 UL1007 Stripped 3/8x3/8 No Tin
Z 0	0-01012-050	18" WHITE #18	Wire #18 UL1007 Stripped 3/8x3/8 No Tin
Z 0	0-01014-050	4"GREEN W/YELL	Wire #18 UL1007 Stripped 3/8x3/8 No Tin
Z 0	0-01098-055	4" #18 UL1007	Wire, Other
Z 0	0-01099-055	4" #18 UL1007	Wire, Other
Z 0	0-01100-055	4" #18 UL1007	Wire, Other
Z 0	0-01101-055	4" #18 UL1007	Wire, Other
Z 0	1-00120-113	3 PIN, 18AWG/OR	Connector, Amp, MTA-156
Z 0	1-00275-131	2 PIN DIF #18GA	Connector, Female
Z 0	1-00472-112	2 PIN, 24AWG/WH	Connector, Amp, MTA-100
Z 0	1-00473-114	2 PIN, WHITE	Header, Amp, MTA-100
Z 0	1-00496-113	6 POS 18GA ORNG	Connector, Amp, MTA-156
Z 0	6-00655-615	24V - 60W	Power Supply
Z 0	7-01612-720	CG635	Fabricated Part
Z 0	7-01613-720	CG635	Fabricated Part
Z 0	7-01656-720	CG635	Fabricated Part

Chassis and Front-Panel Assembly

D 1	3-00012-306	GREEN	LED, Rectangular
D 2	3-00885-306	YELLOW	LED, Rectangular
D 3	3-00012-306	GREEN	LED, Rectangular
D 4	3-00012-306	GREEN	LED, Rectangular
D 5	3-00012-306	GREEN	LED, Rectangular

D 6	3-00884-306	RED	LED, Rectangular
D 7	3-00012-306	GREEN	LED, Rectangular
D 8	3-00012-306	GREEN	LED, Rectangular
D 9	3-00012-306	GREEN	LED, Rectangular
D 10	3-00012-306	GREEN	LED, Rectangular
D 11	3-00012-306	GREEN	LED, Rectangular
D 12	3-00012-306	GREEN	LED, Rectangular
D 13	3-00012-306	GREEN	LED, Rectangular
D 14	3-00012-306	GREEN	LED, Rectangular
D 15	3-00012-306	GREEN	LED, Rectangular
D 16	3-00012-306	GREEN	LED, Rectangular
D 17	3-00012-306	GREEN	LED, Rectangular
D 18	3-00012-306	GREEN	LED, Rectangular
D 19	3-00012-306	GREEN	LED, Rectangular
D 20	3-00012-306	GREEN	LED, Rectangular
D 21	3-00012-306	GREEN	LED, Rectangular
D 22	3-00012-306	GREEN	LED, Rectangular
D 23	3-00012-306	GREEN	LED, Rectangular
D 24	3-00012-306	GREEN	LED, Rectangular
D 25	3-00012-306	GREEN	LED, Rectangular
D 26	3-00012-306	GREEN	LED, Rectangular
D 27	3-00012-306	GREEN	LED, Rectangular
D 28	3-00012-306	GREEN	LED, Rectangular
D 29	3-00012-306	GREEN	LED, Rectangular
D 30	3-00012-306	GREEN	LED, Rectangular
D 31	3-00012-306	GREEN	LED, Rectangular
D 32	3-00012-306	GREEN	LED, Rectangular
D 33	3-00012-306	GREEN	LED, Rectangular
D 34	3-00012-306	GREEN	LED, Rectangular
D 35	3-00004-301	1N4148	Diode
D 36	3-00004-301	1N4148	Diode
D 37	3-00004-301	1N4148	Diode
D 38	3-00004-301	1N4148	Diode
D 39	3-00004-301	1N4148	Diode
D 40	3-00004-301	1N4148	Diode
JP1	1-00661-130	5 PIN SI - TIN	Connector, Male
JP2	1-00661-130	5 PIN SI - TIN	Connector, Male
JP3	1-00661-130	5 PIN SI - TIN	Connector, Male
JP4	1-00661-130	5 PIN SI - TIN	Connector, Male
JP5	1-00661-130	5 PIN SI - TIN	Connector, Male
JP11	1-00052-171	40 COND	Cable Assembly, Ribbon
PC1	7-01584-701	SCG F/P PCB	Printed Circuit Board
U 1	3-00290-340	HDSP-A101	Integrated Circuit (Thru-hole Pkg)
U 2	3-00290-340	HDSP-A101	Integrated Circuit (Thru-hole Pkg)
U 3	3-00290-340	HDSP-A101	Integrated Circuit (Thru-hole Pkg)
U 4	3-00290-340	HDSP-A101	Integrated Circuit (Thru-hole Pkg)
U 5	3-00290-340	HDSP-A101	Integrated Circuit (Thru-hole Pkg)
U 6	3-00290-340	HDSP-A101	Integrated Circuit (Thru-hole Pkg)
U 7	3-00290-340	HDSP-A101	Integrated Circuit (Thru-hole Pkg)
U 8	3-00290-340	HDSP-A101	Integrated Circuit (Thru-hole Pkg)
U 9	3-00290-340	HDSP-A101	Integrated Circuit (Thru-hole Pkg)
U 10	3-00290-340	HDSP-A101	Integrated Circuit (Thru-hole Pkg)
U 11	3-00290-340	HDSP-A101	Integrated Circuit (Thru-hole Pkg)
U 12	3-00290-340	HDSP-A101	Integrated Circuit (Thru-hole Pkg)
U 13	3-00290-340	HDSP-A101	Integrated Circuit (Thru-hole Pkg)
Z 0	0-00048-011	6-32 KEP	Nut, Kep
Z 0	0-00079-031	4-40X3/16 M/F	Standoff
Z 0	0-00084-032	36154	Termination
Z 0	0-00150-026	4-40X1/4PF	Screw, Black, All Types
Z 0	0-00179-000	RIGHT FOOT	Hardware, Misc.
Z 0	0-00180-000	LEFT FOOT	Hardware, Misc.
Z 0	0-00181-020	6-32X1/4PF	Screw, Flathead Phillips

Z 0	0-00185-021	6-32X3/8PP	Screw, Panhead Phillips
Z 0	0-00187-021	4-40X1/4PP	Screw, Panhead Phillips
Z 0	0-00204-000	REAR FOOT	Hardware, Misc.
Z 0	0-00209-021	4-40X3/8PP	Screw, Panhead Phillips
Z 0	0-00248-026	10-32X3/8TRUSSP	Screw, Black, All Types
Z 0	0-00315-021	6-32X7/16 PP	Screw, Panhead Phillips
Z 0	0-00326-026	8-32X1/4PP	Screw, Black, All Types
Z 0	0-00371-026	4-40X3/16PF	Screw, Black, All Types
Z 0	0-00416-020	8-32X1/4PF	Screw, Flathead Phillips
Z 0	0-00438-021	4-40X5/16PP	Screw, Panhead Phillips
Z 0	0-00472-018	1-329631-2	Jam Nut
Z 0	0-00500-000	554808-1	Hardware, Misc.
Z 0	0-00501-042	1-329632-2	Washer, lock
Z 0	0-00893-026	8-32X3/8PF	Screw, Black, All Types
Z 0	7-00122-720	DG535-36	Fabricated Part
Z 0	7-00217-735	PS300-40	Injection Molded Plastic
Z 0	7-00259-720	SR560-28	Fabricated Part
Z 0	7-00260-720	SR560-27	Fabricated Part
Z 0	7-01594-709	CG635	Lexan Overlay
Z 0	7-01595-740	CG635	Keypad, Conductive Rubber
Z 0	7-01610-720	CG635	Fabricated Part
Z 0	7-01611-720	CG635	Fabricated Part
Z 0	7-01616-720	CG635	Fabricated Part

Option 1 Assembly

C 1	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 2	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 3	5-00528-568	2.2U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 4	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 5	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 6	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 7	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 8	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 9	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 10	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 11	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 12	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 13	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 14	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 15	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 16	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 17	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 18	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 19	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 20	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 21	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 22	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 23	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 24	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 25	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 26	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 27	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 28	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 29	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 30	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
J 2	1-00550-140	BULKHEAD JACK	SMA Connector
J 3	1-00550-140	BULKHEAD JACK	SMA Connector
J 4	1-00550-140	BULKHEAD JACK	SMA Connector
J 5	1-00550-140	BULKHEAD JACK	SMA Connector

J 6	1-00553-133	2MM 10POS	Connector, Male, Right Angle
J 7	1-00552-130	2MM 10POS	Connector, Male
L 2	6-00236-631	FR47	Ferrite bead, SMT
L 3	6-00236-631	FR47	Ferrite bead, SMT
PC1	7-01623-701	CG635 OPTION	Printed Circuit Board
Q 1	3-01214-360	BFT92	Integrated Circuit (Surface Mount Pkg)
R 1	4-01447-461	47	Thick Film, 5%, 200 ppm, Chip Resistor
R 2	4-01447-461	47	Thick Film, 5%, 200 ppm, Chip Resistor
R 3	4-01447-461	47	Thick Film, 5%, 200 ppm, Chip Resistor
R 4	4-00954-462	20.0	Thin Film, 1%, 50 ppm, MELF Resistor
R 5	4-00954-462	20.0	Thin Film, 1%, 50 ppm, MELF Resistor
R 6	4-00954-462	20.0	Thin Film, 1%, 50 ppm, MELF Resistor
R 7	4-01447-461	47	Thick Film, 5%, 200 ppm, Chip Resistor
R 8	4-01447-461	47	Thick Film, 5%, 200 ppm, Chip Resistor
R 9	4-01447-461	47	Thick Film, 5%, 200 ppm, Chip Resistor
R 10	4-01447-461	47	Thick Film, 5%, 200 ppm, Chip Resistor
R 11	4-01447-461	47	Thick Film, 5%, 200 ppm, Chip Resistor
R 12	4-01447-461	47	Thick Film, 5%, 200 ppm, Chip Resistor
R 13	4-01447-461	47	Thick Film, 5%, 200 ppm, Chip Resistor
R 14	4-01447-461	47	Thick Film, 5%, 200 ppm, Chip Resistor
R 15	4-01447-461	47	Thick Film, 5%, 200 ppm, Chip Resistor
R 16	4-01447-461	47	Thick Film, 5%, 200 ppm, Chip Resistor
R 17	4-01447-461	47	Thick Film, 5%, 200 ppm, Chip Resistor
R 18	4-01447-461	47	Thick Film, 5%, 200 ppm, Chip Resistor
R 19	4-01447-461	47	Thick Film, 5%, 200 ppm, Chip Resistor
R 20	4-01447-461	47	Thick Film, 5%, 200 ppm, Chip Resistor
R 21	4-01447-461	47	Thick Film, 5%, 200 ppm, Chip Resistor
R 22	4-01447-461	47	Thick Film, 5%, 200 ppm, Chip Resistor
R 23	4-01447-461	47	Thick Film, 5%, 200 ppm, Chip Resistor
R 24	4-01447-461	47	Thick Film, 5%, 200 ppm, Chip Resistor
R 25	4-01447-461	47	Thick Film, 5%, 200 ppm, Chip Resistor
R 26	4-01447-461	47	Thick Film, 5%, 200 ppm, Chip Resistor
R 27	4-01447-461	47	Thick Film, 5%, 200 ppm, Chip Resistor
R 28	4-01447-461	47	Thick Film, 5%, 200 ppm, Chip Resistor
R 29	4-01447-461	47	Thick Film, 5%, 200 ppm, Chip Resistor
R 30	4-01447-461	47	Thick Film, 5%, 200 ppm, Chip Resistor
R 31	4-01105-462	750	Thin Film, 1%, 50 ppm, MELF Resistor
R 32	4-01088-462	499	Thin Film, 1%, 50 ppm, MELF Resistor
R 33	4-00971-462	30.1	Thin Film, 1%, 50 ppm, MELF Resistor
R 42	4-01447-461	47	Thick Film, 5%, 200 ppm, Chip Resistor
R 43	4-01447-461	47	Thick Film, 5%, 200 ppm, Chip Resistor
R 44	4-01447-461	47	Thick Film, 5%, 200 ppm, Chip Resistor
R 45	4-01447-461	47	Thick Film, 5%, 200 ppm, Chip Resistor
R 46	4-01447-461	47	Thick Film, 5%, 200 ppm, Chip Resistor
R 47	4-01447-461	47	Thick Film, 5%, 200 ppm, Chip Resistor
R 48	4-01021-462	100	Thin Film, 1%, 50 ppm, MELF Resistor
R 49	4-01021-462	100	Thin Film, 1%, 50 ppm, MELF Resistor
R 50	4-01070-462	324	Thin Film, 1%, 50 ppm, MELF Resistor
R 51	4-01070-462	324	Thin Film, 1%, 50 ppm, MELF Resistor
R 52	4-01021-462	100	Thin Film, 1%, 50 ppm, MELF Resistor
R 53	4-01021-462	100	Thin Film, 1%, 50 ppm, MELF Resistor
R 54	4-01021-462	100	Thin Film, 1%, 50 ppm, MELF Resistor
R 55	4-01021-462	100	Thin Film, 1%, 50 ppm, MELF Resistor
R 56	4-01070-462	324	Thin Film, 1%, 50 ppm, MELF Resistor
R 57	4-01070-462	324	Thin Film, 1%, 50 ppm, MELF Resistor
R 58	4-01021-462	100	Thin Film, 1%, 50 ppm, MELF Resistor
R 59	4-01021-462	100	Thin Film, 1%, 50 ppm, MELF Resistor
U 1	3-01196-360	MC100EP52D	Integrated Circuit (Surface Mount Pkg)
U 2	3-01196-360	MC100EP52D	Integrated Circuit (Surface Mount Pkg)
U 3	3-01196-360	MC100EP52D	Integrated Circuit (Surface Mount Pkg)
U 4	3-01196-360	MC100EP52D	Integrated Circuit (Surface Mount Pkg)
U 5	3-01196-360	MC100EP52D	Integrated Circuit (Surface Mount Pkg)

U 6	3-01196-360	MC100EP52D	Integrated Circuit (Surface Mount Pkg)
U 7	3-01196-360	MC100EP52D	Integrated Circuit (Surface Mount Pkg)
U 8	3-01191-360	MC100EP08D	Integrated Circuit (Surface Mount Pkg)
U 9	3-01199-360	NB6L11D	Integrated Circuit (Surface Mount Pkg)
U 10	3-01200-360	NB6L16D	Integrated Circuit (Surface Mount Pkg)
U 11	3-01200-360	NB6L16D	Integrated Circuit (Surface Mount Pkg)
U 12	3-01199-360	NB6L11D	Integrated Circuit (Surface Mount Pkg)
Z 0	0-00187-021	4-40X1/4PP	Screw, Panhead Phillips
Z 0	7-01619-720		Fabricated Part

Option 2 Assembly

J 1	1-01078-150	SSW-107-01-S-S	Socket, THRU-HOLE
J 3	1-01058-131	09-52-3101	Connector, Female
PC1	7-01586-701	SCG TIMEBASE	Printed Circuit Board
R 1	4-00176-407	3.01K	Resistor, Metal Film, 1/8W, 1%, 50PPM
R 2	4-00158-407	2.00K	Resistor, Metal Film, 1/8W, 1%, 50PPM
R 3	4-00176-407	3.01K	Resistor, Metal Film, 1/8W, 1%, 50PPM
R 4	4-00148-407	12.1K	Resistor, Metal Film, 1/8W, 1%, 50PPM
U 1	3-00508-340	LM358	Integrated Circuit (Thru-hole Pkg)
Z 0	0-00048-011	6-32 KEP	Nut, Kep
Z 0	0-00096-041	#4 SPLIT	Washer, Split
Z 0	0-00241-021	4-40X3/16PP	Screw, Panhead Phillips
Z 0	0-01090-031	3403	Standoff
Z 0	1-01057-130	26-48-1101	Connector, Male
Z 0	6-00051-622	10 MHZ	Ovenized Crystal Oscillator
Z 0	7-01614-720	CG635	Fabricated Part

Option 3 Assembly

C 1	5-00023-529	.1U	Cap, Monolythic Ceramic, 50V, 20%, Z5U
J 2	1-00342-165	10 PIN STRAIGHT	Connector, D-Sub, Female
J 2A	1-00343-100	COAX CONTACT	Connector, Misc.
J 3	1-01058-131	09-52-3101	Connector, Female
PC1	7-01586-701	SCG TIMEBASE	Printed Circuit Board
R 1	4-00176-407	3.01K	Resistor, Metal Film, 1/8W, 1%, 50PPM
R 2	4-00158-407	2.00K	Resistor, Metal Film, 1/8W, 1%, 50PPM
R 3	4-00176-407	3.01K	Resistor, Metal Film, 1/8W, 1%, 50PPM
R 4	4-00148-407	12.1K	Resistor, Metal Film, 1/8W, 1%, 50PPM
U 1	3-00508-340	LM358	Integrated Circuit (Thru-hole Pkg)
U 2	3-00155-340	74HC04	Integrated Circuit (Thru-hole Pkg)
U 3	3-00116-325	78L05	Transistor, TO-92 Package
Z 0	0-00043-011	4-40 KEP	Nut, Kep
Z 0	0-00096-041	#4 SPLIT	Washer, Split
Z 0	0-00241-021	4-40X3/16PP	Screw, Panhead Phillips
Z 0	0-00781-031	4-40X1/4 M/F	Standoff
Z 0	1-01057-130	26-48-1101	Connector, Male
Z 0	6-00079-624	10 MHZ RUBIDIUM	Oscillator, Misc.
Z 0	7-01614-720	CG635	Fabricated Part

Schematics

CG635 Schematic Diagram List

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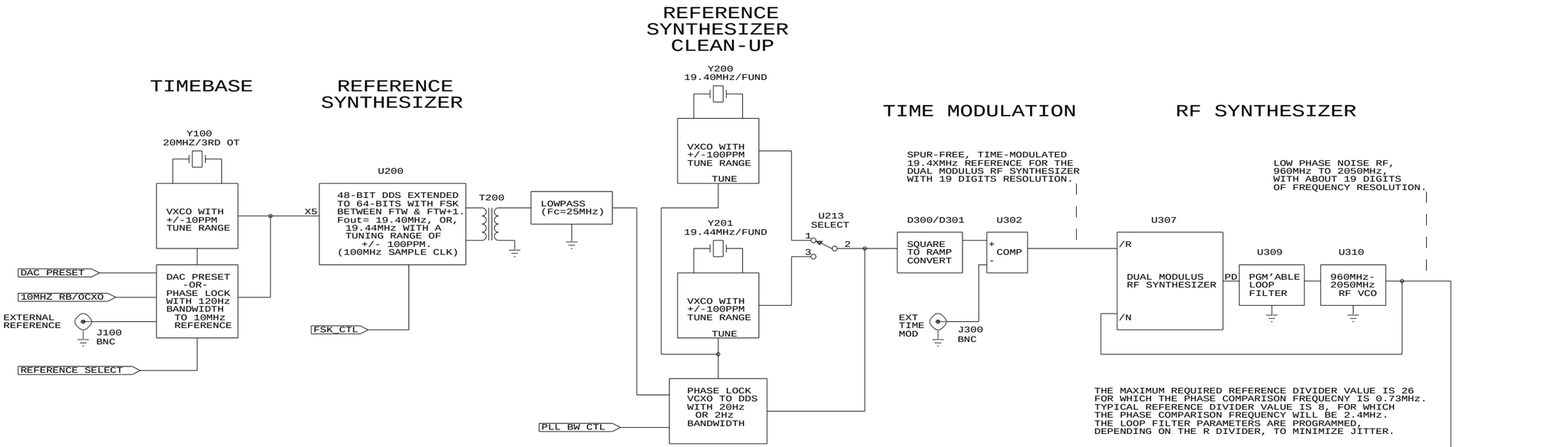
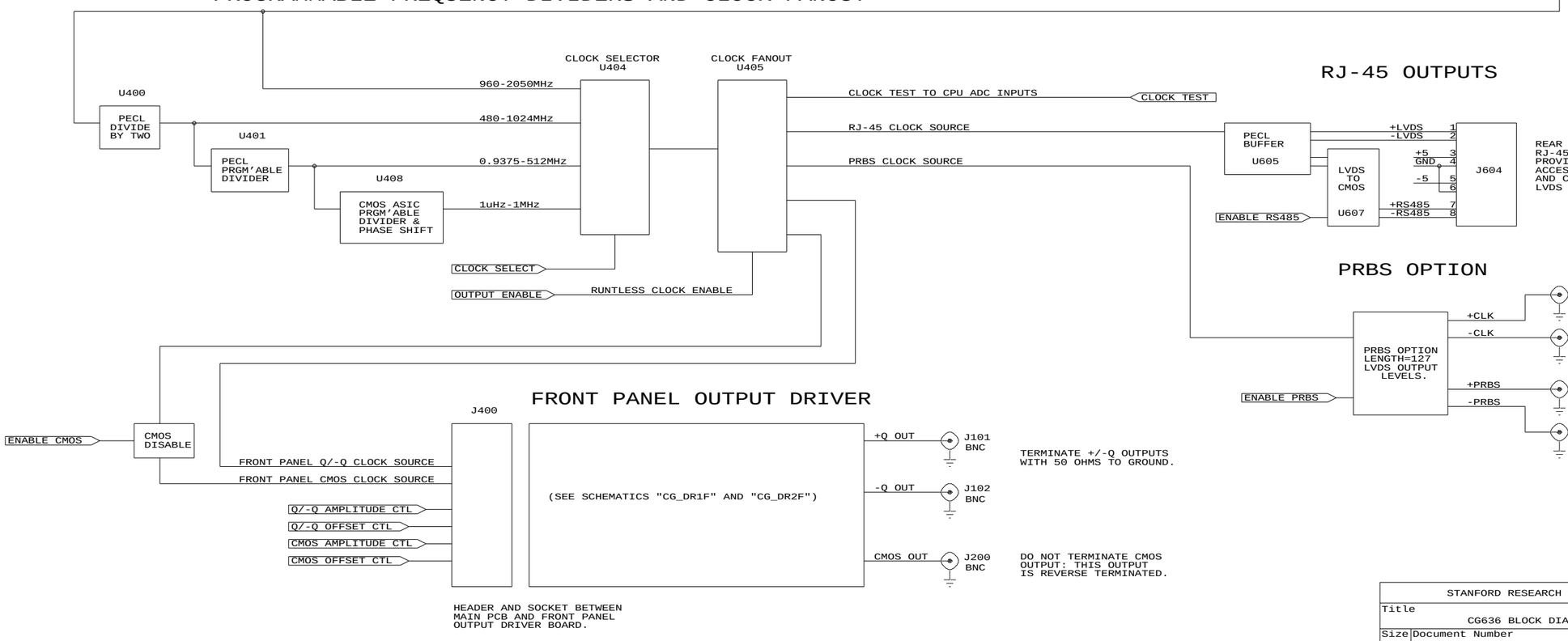
CG635 --- SYNTHESIZED CLOCK GENERATOR --- BLOCK DIAGRAM



PROGRAMMABLE FREQUENCY DIVIDERS AND CLOCK FANOUT



STANFORD RESEARCH SYSTEMS		
Title: CG636 BLOCK DIAGRAM		
Size: C	Document Number: GC_BLK_D	REV: D
Date: June 2, 2006	Sheet 1 of 1	

CAL_20MHZ
0-4.095VDC
TO CPU's ADC's
EXT_DET & OPT_DET "DETECTED" BY DC LEVEL OF >+1.0VDC
EXT_DET
R107
10K
C108
.1U
R108
10K
10MHZ_LEAD
EXTERNAL 10MHz INPUT.
INPUT IMPEDANCE IS
1000 OHMS AT 10MHz.
J100
BNC_RT
R100
49.9
C100
1000P
T100
TOKO7P
7:7:2 I.F. COIL AS
2:1 AUTOTRANSFORMER.
27PF TUNES COIL
DOWN TO 10.0MHz.
C101
27P
R101
249
+4.096V
R102
4.99K
R103
49.9
+5A
L105
BEAD
C102
.1U
C104
.1U
-5
R134
47
C103
.1U
U100
AD8561
U101
74VHC1GT02
U104
74LVC1G32
PLL LOOP FILTER CAN "HOLD"
AT 3.66 X (CAL_20MHZ) OR
LOCK 20MHz VCXO TO EXT/OPT.
LOOP BANDWIDTH = 120Hz
U105
LP2985AIM5-3.3
+5A
C110
4.7U
C133
.1U
+3.3PHASE
C132
4.7U
R119
1.00M
U109B
LF353
PRECHARGES INTEGRATOR
TO CAL_20MHZ x 11/3.
R120
499K
C117
1U-MF
T/H
R122
2.49K
+5A
+15
U108E
DG211
-15
U106A
74LVC74
R138
1K
D101
MMBD352
STRETCH
U107
74LVC1G32
C134
10P
U106B
74LVC74
R111
249
U108A
DG211
1 PLL/-DAC
U108D
DG211
DAC/-PLL
C111
.1U
C112
.1U
U108B
DG211
8 PLL/-DAC
U108C
DG211
DAC/-PLL
R112
249
R113
2.49K
C113
.1U-MF
R115
24.9K
C114
1000P
R121
24.9K
T/H
C136
.1U
R117
100K/1%
10MHZ_VC
U109A
LF353
R118
40.2K
C118
.01U
C137
.1U
C116
1000P
C115
.1U-MF
T/H
R116
24.9K
R114
2.49K
-EXT/OPT
DISABLE OPT COMP
W/EXT TIMEBASE.
+4.096V
R105
4.99K
+10MHZ_OPT
R106
49.9
+5A
L106
BEAD
U114
74VHC1GT02
C105
.1U
C107
.1U
R104
49.9
-5
R136
47
C106
.1U
U102
AD8561
U103
74VHC1GT08
PLL/-DAC
BRING 10MHZ OPTION
GROUND RETURN HERE ==>
PHASE DETECTOR AND PREFILTER.
Kphi IS APPROXIMATELY 0.52V/RAD.
"LOCKED" WHEN "LEAD" & "LAG" ARE BOTH ABOUT 0.15VDC.
R110
10K
10MHZ_LAG
OPT_DET
R109
10K
C109
.1U
DAC/-PLL
DAC/-PLL
+5A
U110
74LVC1G02
PLL/-DAC
<= 10MHZ FOR PHASE COMPARISON TO EXTERNAL OR OPTIONAL TIMEBASE
VCXO CAN BE PHASE LOCKED TO OPTIONAL INTERNAL OR EXTERNAL 10MHz REFERENCE
20MHz, 3rd OVERTONE, AT-CUT VCXO. Kv=300 r/s/v.
TUNING RANGE IS APPROXIMATELY +/-20ppm.
VARACTOR VOLTAGE EITHER FROM DAC OR PLL FILTER.
+15
C135
.1U
R127
3.01K
+4.096V
+4.096V
C119
.1U
R128
100/1%
U111A
LM358
R125
100K/1%
Y100
20MHz/3RD/20PF
Ic=2.0mA
Q100
MMBR5179LT1
C138
.1U
C120
.1U
R126
100K
C121
82P
R129
24.9
-15
R123
49.9K
2.73Vdc
R124
100K/1%
D100
MMBV609LT
Cvar = 28pF @ 7V
C122
470P
L103
.47UH
GLOBAL
POWER
+15
+5A
+5D
+3.3
GND
-5
-15
R139
49.9K
R140
49.9K
U111B
LM358
L107
BEAD
+5A
C123
.1U
R141
24.9K
R142
49.9
U112
AD8561
R143
100/1%
R144
100/1%
R132
47
-5
C124
.1U
20MHz/2 =>10MHz
L102
BEAD
+5A
+5FLT
C125
.1U
U113A
74HCT74
10MHZ CLOCK FOR MICROCONTROLLER
AND GPIB INTERFACE CONTROLLER.
10MHZ
C131
.1U
PUSH-PULL 10MHz OUTPUT DRIVER AND LOW-PASS FILTER
U113B
74HCT74
R130
249
7:7:2 TANK
ADJ FOR MAX
AMPLITUDE.
C126
56P
C127
56P
T101
TOKO7P
C129
33P
L104
.82UH
10MHz SINE WAVE
50 OHMS, +7dBm
J101
BNC_RT
C128
220P
C130
220P
R131
249
CAPS TUNE TANK
DOWN TO 10MHz
3rd DEGREE CAUER LPF
(40dB HARMONIC SUPPRESSION)
20MHZ
20MHZ FREQUENCY REFERENCE FOR DDS ===>
-20MHZ

STANFORD RESEARCH SYSTEMS		
Title: CG635 CLOCK GENERATOR: 10MHz TIMEBASES		
Size: C	Document Number: CG_MB1D	REV: D
Date: June 1, 2006	Sheet 1 of 6	

+3.3 C210 .1U L200 BEAD L201 BEAD C200 .1U C201 .1U C202 .1U C203 .1U C204 .1U C205 .1U C206 .1U C207 .1U C208 .1U C209 .1U

U200 AD9852

C211 .01U R200 1.30K

DDS_D0 DDS_D1 DDS_D2 DDS_D3 DDS_D4 DDS_D5 DDS_D6 DDS_D7 → D0 D1 D2 D3 D4 D5 D6 D7

DDS_A0 DDS_A1 DDS_A2 DDS_A3 DDS_A4 DDS_A5 → A0/SDIO A1/SDO A2/RST A3 A4 A5

-WR_DDS → WRB/SCLK
-RD_DDS → RDB/CSB
PAR/-SER

FSK KEYING
IO_UD
DIFF_EN
CLK
-CLK
RESET

PLL_FLT CTL_DAC CTL_DAC BYPASS DAC DAC RSET +VIN -VIN VOUT

LEVEL SHIFT FROM +5V.

U211 74LVC1G32

FSK_DDS UPD_DDS 20MHZ -20MHZ RST_DDS

R255 402 R256 402

C212 .1U

C213 27P C214 27P R201 200/1% R202 200/1%

T200 TC1-1T

7TH ORDER CHEBYSHEV LOWPASS FILTER (fc = 25MHz)

L202 3.3UH L203 3.9UH L204 3.3UH C216 27P C217 27P C218 10P R205 402

+5A L207 BEAD C237 .1U U203 AD8561 C238 .1U R207 47 -5

R203 4.02K Iset=10mA

DISABLE CONTROL DAC, AMPLITUDE MULTIPLIER, FAST VOLTAGE COMPARATOR, AND INVERSE SINC FUNCTION TO REDUCE POWER CONSUMPTION.

CLOCK MULTIPLIER: 5X FOR A SAMPLE CLOCK RATE OF 100MHz. fout=19,440,000Hz, +/-100ppm OR 19,400,000Hz, +/-100ppm.

GLOBAL POWER: +15 +5A +5D +3.3 GND -5 -15

+15 C239 .1U R212 4.99K Ic=2mA C240 .1U R213 100/1%

U216A LM358 R210 200K/1% Q202 MMBR5179LT1 C241 .1U C256 1000P C242 47P R214 24.9 C270 .1U Y200 19.40M C243 220P L210 22UH

R208 49.9K +4.096V R209 100K/1% R211 100K D200 MMBV609LT

ALT_REF

U212 74VHC1GT02 L205 BEAD C244 .1U U205 AD8561 R246 4.99K R247 49.9 C245 .1U R216 47 U216B LM358

+5A C246 4.7U C254 .1U U206 LP2985AIM5-3.3 (VIN OUT EN C GND) C255 4.7U

U207A 74LVC74 (PR VCC D Q CK Q CL GND)

R217 2.49K C247 .1U C248 .1U R218 2.49K

R238 1K L212 BEAD C268 10P C265 .1U

D202 MMBD352 U208 74LVC1G32 STRETCH

U207B 74LVC74

U213 74VHC1GT32

PHASE DETECTOR AND PREFILTER. Kphi IS APPROXIMATELY 0.52V/RAD.

19.44/19.40MHz VCXO ACTS AS A NARROW BAND FILTER TO STOP DDS SPURS.
NOMINAL VARACTOR VOLTAGE IS 7V WHERE TOTAL Cvar = 20pF.
TUNING RANGE IS APPROXIMATELY +/-170PPM AROUND 19,4X0,000Hz.
Kvco IS APPROXIMATELY 3000 RAD/S/V AROUND CENTER FREQUENCY.
MOTIONAL CAPACITANCE OF EACH CRYSTAL IS ABOUT 25fF IN HC49U CAN.
OPERATING FREQUENCY IS SELECTED TO MINIMIZE RF PLL DIVIDERS.
PRIME FACTORS: 19.44M = 2^7 X 3^5 X 5^4. 19.4M = 2^6 X 5^5 X 97.

PHASE LOCK 19.44MHz/19.40MHz VCXO TO DDS WITH NARROW BANDWIDTH.
LOCKED WHEN "LEAD" AND "LAG" ARE BOTH ABOUT 0.3V AND <20mV APART.

R229 10K 19MHZ_LEAD

D203 MMBD352 (100 OHMS) R219 10M U209A DG211 R221 100K/1% T/H C249 1U/PP R223 10.0K C251 1000P R225 100K/1% (100 OHMS) U209C DG211

+5A +15 U209E DG211

+15 C273 .1U U204A LF353

D204 MMBD352 (100 OHMS) R220 10M U209B DG211 R222 100K/1% C250 1U/PP T/H R224 10.0K R226 100K/1% (100 OHMS) U209D DG211 C274 .1U C252 1000P

R227 100K/1% 19MHZ_VC R228 40.2K C253 .1U

R230 10K 19MHZ_LAG 19MHZ

PLL LOOP FILTER B.W. = 2Hz or 20Hz (SEE NOTE BELOW)

NOTE: VCXO PLL BANDWIDTH HAS BEEN FIXED AT 20Hz BY REPLACING R219,R220,R225 & R226 WITH 100 OHMS AND OMITTING U209. (REV D)

LOW NOISE 19.44/19.40MHz FREQUENCY REFERENCE FOR RF SYNTHESIZER WITH NARROW BW LOCK TO DDS FREQUENCY. RANGE: +/-100PPM. RESOLUTION: 1:2^64.

+15 C257 .1U R244 4.99K C258 .1U R245 100/1% Ic=2mA

U215A LM358 R239 200K/1% Q201 MMBR5179LT1 C271 .1U C259 .1U C260 1000P C261 47P R243 24.9 C272 .1U Y201 19.44M C262 220P L211 22UH

R240 49.9K +4.096V R241 100K/1% R242 100K D201 MMBV609LT

U214 74VHC1GT08 L206 BEAD C263 .1U U210 AD8561 R248 4.99K R249 49.9 C264 .1U R251 47 U215B LM358

+5A R254 49.9K C266 .1U R252 100K/1% R253 100K/1% C267 .1U U204B LF353

SYMMETRY CONTROL

19MHz VCXO PLL BANDWIDTH CONTROL.

-FAST_19MHZ

STANFORD RESEARCH SYSTEMS		
Title: CLOCK GENERATOR: DDS & 19.40/19.44MHz VCXO		
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0 TO +4.095V FROM 12-BIT DAC.
CONTROLS CURRENT SOURCE FOR RAMP &
CALIBRATES T-MOD INPUT FOR 1NS/VOLT.

RAMP GENERATOR
FOR TIME MODULATION.
19MHz UP/DOWN RAMP
OF ABOUT 4 Vpp.

TIME MODULATION
INPUT (+/-5VDC)
SENS: 1nS/Vdc

NETWORK: DC/5,
-3dB AT 200kHz,
LIMITER AT +/-6V.

LIMITER
(+/-6V)

COMPARATOR GENERATES
TIME-MODULATED 19.4MHz
SQUARE WAVE REFERENCE.

+20V "REGULATOR" FOR RF PLL LOOP FILTER.
(POWERED BY +24_US. COMES UP WITH +15V)

LOW NOISE +10V "REGULATOR" FOR RF VCO.

GLOBAL POWER

LEVEL SHIFT &
NOISE BUFFER
("GT" REQUIRED)

960-2050MHz RF PLL WITH ADJUSTABLE LOOP FILTER.

960-2050MHz VCO
ABOUT +80MHz/V.
(13 GROUND PINS
ARE NOT SHOWN.)

SERIAL DATA IS
GATED "OFF" WHEN
NOT TARGETING
RF SYNTHESIZER.

TRISTATE CHARGE PUMP
WHEN CHANGING REGISTERS
TO REDUCE FREQ TRANSIENT.

R370 & R371 PIGGYBACK
ON C326 & C327.

STOP RF OUTPUT
WHEN V_TUNE
IS NEGATIVE.

TOP OCTAVE
CLOCK OUTPUT.

STANFORD RESEARCH SYSTEMS		
Title: CLOCK GENERATOR: TIME MODULATION & RF PLL.		
Size: C	Document Number: CG_MB3D	REV: D
Date: June 1, 2006	Sheet 3 of 6	

DIGITAL DIVIDER WITH ADJUSTABLE PHASE.
TRIGGER INPUT CAUSES PIRB TO BE USED
TO PHASE SHIFT BY INTEGER CLOCK PERIODS.

+5D
C421 C422 C423 C424
.1U .1U .1U .1U

U408
F107563FN
HI_SCOTT

A[0..7]
A[0..7]

-WR_ASIC

U406
74HC574
SET HIGH TO USE PIRB ONCE
EXTERNAL PIR SELECT CONTROL
-CLEAR 48-BIT ACCUMULATOR
-RESET AND INITIALIZE
-FORCE OUTPUT HIGH
-FORCE OUTPUT LOW
-ENABLE CLOCK

-CS_ASIC

L402
BEAD
+5A
C425 .1U
C428 .1U

GLOBAL POWER
+15
+5A
+5D
+3.3
GND
-5
-15

RF/64
U407
AD8611
U410
74VHC1GT08
R406 47
R407 47
R408 47
C410 .1U

DATA0 DATA1 DATA2 DATA3 DATA4 DATA5 DATA6 DATA7
HOST_RQ
HOST_WR
TRIG
CARRY
PIR_SEL
CLEAR
RESET
CLOCK
TEST0
TEST1
MA0 MA1 MA2 MA3 MA4 MA5 MA6 MA7 MA8 MA9 MA10 MA11 MA12 MA13 MA14 MA15
CSX0 CSX1 CSX2
WA0 WA1 WA2 WA3 WA4 WA5 WA6 WA7 WA8 WA9 WA10 WA11 WA12 WA13 WA14
SIGN
HOST_ACK
RUN
PIRA
OP_CLK
OP_FETCH
TRIGGERED
MIRROR

+5A
C426 .1U
PHASE HOP SYNCHRONIZER.
U409A
74AC74
GOES LOW WHEN DIGITAL PHASE ADJUST HAS COMPLETED.
-DONE

C427 .1U
OUTPUT CLOCK RESYNCHRONIZATION.
U409B
74AC74
OUTPUT DIVIDES CLK BY 2^N (N=1...48).
OPERATIONALLY, N RANGES FROM 5 TO 30
DIVIDING CLOCK BY 32 TO 1,073,741,824.
PHASE ADJUSTABLE TO ANY CLOCK BOUNDARY.

R417 604
R418 604
R419 200/1%
R420 200/1%
+3.3_MPX
+3.3
L401 BEAD
C411 .1U
C412 .1U
C413 .1U

DIV BY 4*(256-LOAD)
(4,8,12,16...1024)

L400
BEAD
+3.3
+3.3_CNT

+RF_VCO
-RF_VCO

DIVIDE BY 2
U400
MC100EP51
C400 .1U

U401
MC100EP016A
C401 .1U
C402 .1U
C403 .1U
C404 .1U

"LOAD"
ECL_DIV0
ECL_DIV1
ECL_DIV2
ECL_DIV3
ECL_DIV4
ECL_DIV5
ECL_DIV6
ECL_DIV7
P0 P1 P2 P3 P4 P5 P6 P7
Q0 Q1 Q2 Q3 Q4 Q5 Q6 Q7
PE TCLD CLK CLK CE MR
VBB COUT COUT TC
ECL_DIV_MR

C406 .1U
C409 .1U

U402
MC100EP51
U403
MC100EP35
"TC" LOW AT TERMINAL CNT. PIPELINE & INVERT -TC
TOGGLE ON -TC

R400 47
R401 47
R402 47
C407 .1U
R431 100/1%

DISABLE DIVIDERS IN TOP OCTAVE.
U411
74LVC1G02

PROGRAMMABLE DIVIDE BY 2*N.

UN-DIVIDED
DIVIDED BY 2
R403 30.1
R404 30.1
R405 47
C408 .1U

U404
MC100EP57
R421 301
R422 301
CLOCK SOURCE 4:1 MULTIPLEXER.

R409 47
R410 47
R411 47
C414 .1U

BAND_SEL0
BAND_SEL1
STOP_LVL
-RUN/STOP
-EN_OUT
EN_CMOS

CONTROLLED IMPEDANCE TEST SECTION
J402
SMA
R416
49.9

HEADER TO OPTIONAL PRBS GENERATOR.
J401
S2104
+5A
EN_PRBS
+3.3
+PRBS_DRV
-PRBS_DRV
+3.3
-5
C417 .1U
C418 .1U
C419 .1U
C420 .1U
-PRBS_OPT

CLOCK FANOUT WITH "RUNTLESS" ENABLE.
U405
MC100EP14
R414 10K
R415 10K
+CLK_TST
-CLK_TST
C415 .1U
C416 .1U
R412 150/1%
R413 150/1%
TO REAR PANEL TWISTED-PAIR OUTPUT DRIVERS.
+REAR_CLK
-REAR_CLK

SOURCES +24mA TO DISABLE CMOS OUTPUT.
+5A
R433 499
R434 30.1
R432 750/1%
Q400 BFT92

J400
HEADER20A
+4.096V
CMOS_AMPL
CMOS_OFFS
Q_AMPL
Q_OFFS
-CMOS_DRV
+CMOS_DRV
-Q_DRV
+Q_DRV
+15
+5A
-5
-15
+Q_TST
-Q_TST
CMOS_TST
HEADER TO FRONT PANEL BNC OUTPUT DRIVER PCB.

STANFORD RESEARCH SYSTEMS		
Title: CLOCK GENERATOR: ECL DIVIDE AND CLOCK FANOUT		
Size: C	Document Number: CG_MB4D	REV: D
Date: June 2, 2006	Sheet 4 of 6	

R500 1.00K
U513 MAX6241
R501 100K
U514A LF353
+15 .1U C522
+4.096V
C500 2.2U-35V
-5 .1U C523
U514B LF353
C502 1U-MF T/H
+5CPU (SOURCE)
C504 .1U
C505 .1U
C506 .1U
C507 .1U
L500 BEAD
R502 47
C503 .1U
C521 .1U
U516 LM45 10mV/C
EXT_DET
OPT_DET
10MHZ_LEAD
10MHZ_LAG
10MHZ_VC
19MHZ_LEAD
19MHZ_LAG
19MHZ_VC
RF_VC
+CLK_TST
-CLK_TST
+Q_TST
-Q_TST
CMOS_TST
+24V_TST
ANALOG TEST POINTS (4mV RESOLUTION)
-DROPOUT
-GPIB
R503 1K
+5CPU -RESET
U515 MAX6348UR44
BACKGROUND DEBUG
J500 +5CPU
HEAD3X2
C518 .1U
10MHZ
PORT G HAS PULLDOWNS.
-DONE
J506
U500 MC68HC912D60A
PORT H HAS PULL-UPS.
-RB_OPT
-OCXO_OPT
-PRBS_OPT
RF_LOCK
RE-PROGRAM
J507
J509
J510
PHUPD +5CPU
-CS_ASIC
-WR_ASIC
-CS_SYN
-CS_FLT
-CS_DIV
-CS_ECL
-CS_DAC
SDO SDI SCK SS
SYN_DATA
SYN_CLK
-CS_SYN
SPI INTERFACE FOR RF SYNTHESIZER.
C512 .1U
OCTAL 12-BIT DAC FOR CONTROL AND CALIBRAION.
U504 LTC2620
CAL_OPT
CAL_20MHZ
CAL_TMOD
CAL_SYM
Q_AMPL
Q_OFFS
CMOS_AMPL
CMOS_OFFS
R504 100K/1%
C513 .1U
U505A 74HC4538
-CS_STROBE
DISABLE LEDS IF CPU STOPS
-EN_LEDS
R506 10.0K
C520 .1U
U505B 74HC4538
S7 (KEY-CLICKS)
Q513 BC817
SP500 BUZZER
C514 330U/35V
R507 10.0
SINGLE POINT GROUND RETURN
LED_RTN
L501 47UH/1A
+5D +5_LEDS
GPIB CONTROL
C509 .1U
U501 74HC574
RS0_GPIB
RS1_GPIB
RS2_GPIB
-RST_GPIB
-CE_GPIB
-WR_GPIB
DBIN_GPIB
FOR GPIB
B[0..7]
DDS CONTROL
C510 .1U
U502 74LVC574
-RD_DDS
-WR_DDS
DDS_A5
DDS_A4
DDS_A3
DDS_A2
DDS_A1
DDS_A0
BI-DIRECTIONAL DATA FOR DDS.
C519 .1U
C511 .1U
U503 74LVC4245A
DDS_D7
DDS_D6
DDS_D5
DDS_D4
DDS_D3
DDS_D2
DDS_D1
DDS_D0
CTS_RS232
RTS_RS232
FSK_DDS
TXD_RS232
RXD_RS232
TXD_RB
RXD_RB
ODD-DIGITS
U506 74HC574
N500 270X4
N501 270X4
-CS_ODD
EVEN-DIGITS
U507 74HC574
N502 270X4
N503 270X4
-CS_EVEN
STROBES
U508 74HC574
N500 270X4
-CS_STROBE
STROBE 7 FOR KEYCLICK
LAMPS
U509 74HC574
-CS_LAMP
+5A
L502 BEAD
RF REFERENCE & PLL BANDWIDTH CONTROL.
C515 4.7U
U510 74HC574
PLL_FLT0
PLL_FLT1
PLL_FLT2
PLL_FLT3
-FAST 10MHZ
-EN_RS485
ALT_REF
EN_CMOS
-CS_FLT
OUTPUT DIVIDER PRESET.
NOTE ORDER:
C516 .1U
U511 74LVC574
ECL_DIV7
ECL_DIV6
ECL_DIV5
ECL_DIV4
ECL_DIV3
ECL_DIV2
ECL_DIV1
ECL_DIV0
-CS_DIV
OCTAVE SELECT & OUTPUT ENABLES.
C517 .1U
U512 74LVC574
UPD_DDS
RST_DDS
ECL_DIV_MR
STOP_LVL
-RUN/STOP
-EN_OUT
BAND_SEL1
BAND_SEL0
-CS_ECL
A[0..7]
BUS TO LOAD DDS ASIC REGISTERS
RIBBON CABLE TO FRONT PANEL DISPLAY AND KEYPAD SCAN.
J501 HEAD40
-Oa -Ob -Oc -Od -Oe -Of -Og -Odp
-Ea -Eb -Ec -Ed -Ee -Ef -Eg -Edp
STB0 STB1 STB2 STB3 STB4 STB5 STB6
-LAMP0 -LAMP1 -LAMP2 -LAMP3 -LAMP4 -LAMP5
KEY0 KEY1 KEY2 KEY3 KEY4 KEY5
S6 S5 S4 S3 S2 S1 S0
Q500 BC817
Q501 BC817
Q502 BC817
Q503 BC817
Q504 BC817
Q505 BC817
Q506 BC817
N504 15X4
N505 15X4
N506 15X4
Q507 BC807
Q508 BC807
Q509 BC807
Q510 BC807
Q511 BC807
Q512 BC807
-L0 -L1 -L2 -L3 -L4 -L5
GLOBAL POWER
+15 +5A +5D +3.3 GND -5 -15

STANFORD RESEARCH SYSTEMS		
Title: CLOCK GENERATOR: MICROCONTROLLER & I/O		
Size: C	Document Number: CG_MB5D	REV: D
Date: June 1, 2006	Sheet 5 of 6	

POWER SUPPLY INTERFACE AND CONNECTION TO OPTIONAL TIMEBASE.

GLOBAL POWER SUPPLIES FOR ALL MOTHERBOARD SCHEMATICS

HEADER FROM POWER SUPPLY MODULE.

J600 CONN10M156: +24_US, -ENABLE, +15, +5A, +5D, +3.3, -5, -15

+24_US +15 +5A +5D +3.3

C604 2.2U-35V, C605 2.2U-35V

C600 2.2U-35V, C601 2.2U-35V, C602 2.2U-35V, C603 2.2U-35V

-15 -5

CONNECTOR TO THE OPTIONAL TIMEBASE. USES EITHER SC-10 (SRS 10MHz/+24V OCXO, P/N SC-10-24-1-J-J-J-J) OR A PRS-10 RUBIDIUM. OPTIONAL TIMEBASES ARE "ON" DURING "STANDBY".

+24_TST = 0.130 X +24_US

+24V_TST

C606 .1U, R603 100K/1%, R604 15.0K

CAL_OPT, TXD_RB

J601 CONN10M156: RXD_RB, -OCXO_OPT, -RB_OPT, +10MHZ_OPT, (10MHZ RETURN)

R601 18.2K, +5D, R605 10K

R600 10K, D600 LED-RND, STAND-BY POWER WARNING

SW600A DPDT, SW600B DPDT — FRONT PANEL POWER SWITCH. (CLOSE=ON)

R602 4.02K, C607 .1U

U600 LM393

-DROPOUT

"-DROPOUT" XIRQ INTERRUPT TO MICROCONTROLLER WHEN "+24_US" DROPS BELOW +22VDC OR WHEN UNIT TURNED "OFF".

+4.096V +4.096V

REAR PANEL RS-485 & LVDS CLOCK OUTPUT DRIVERS

+5A, C616 .1U

R617 1.0, R618 1.0, R641 3.3

R619 1.00K, R620 40.2K

+15, C629 .1U, U611A LM358, -15, C630 .1U, C617 1000P

N-CHAN MOSFET & SCHOTTKY DIODE. U612 IRF7353

LIMIT +5VDC OUTPUT CURRENT TO 280mA.

C618 2.2U-35V

L603 BEAD

+3.3, L602 BEAD, +3.3_REAR

C619 .1U

LVDS CLOCK TO 2GHz

U605 MC100EP11: VCC, VEE, IN, IN, Q, Q, Q, Q

+REAR_CLK, -REAR_CLK

R639 47, R640 47, C622 .1U, R616 47

R622 54.9, R623 54.9

R624 523, R625 523, -5

C623 .1U, C624 .1U

L604 BEAD, J604 RJ-45S, L605 BEAD

U607 MAX9113ESA: I1, I1, I2, I2, VCC, O1, O2, VEE

R611 40.2, R612 40.2

RS-485 CLOCK TO 105MHz

R609 178, R610 200/1%

-EN_RS485

DISABLE RS485 ABOVE 105MHz

R626 226, R627 200/1%

L606 BEAD

R634 40.2K, C626 1000P

U613 IRF5803, U611B LM358

R636 1.00K

R637 1.0, R638 1.0, R642 3.3

P-CHAN MOSFET & SCHOTTKY DIODE.

C628 2.2U-35V

-5, C627 .1U

LIMIT -5VDC OUTPUT CURRENT TO 280mA.

GPIB INTERFACE

+5D, L600 BEAD, +5_GPIB

C608 .1U, C609 .1U, C610 .1U

U602 SN75ALS160DW, U603 SN75ALS161DW, U601 NAT9914BPL

B[0..7], B0, B1, B2, B3, B4, B5, B6, B7

-WR_GPIB, -WE_GPIB

DBIN_GPIB, DBIN

RS0_GPIB, RS1_GPIB, RS2_GPIB

-CE_GPIB

-RST_GPIB

10MHZ

J602 GPIB

R606 1K

-GPIB

RS-232 SERIAL INTERFACE.

+5D_L601, BEAD

C611 .1U, C612 .1U, C613 .1U, C614 .1U, C615 .1U

U604 MAX202

R607 10K, R608 10K

TXD_RS232, CTS_RS232

J603 DB9F318: CD, DSR, RX, RTS, TX, CTS, DTR, (NC), GND

RXD_RS232, RTS_RS232

MOUNTING HOLES (0.128" DIAMETER)

M1 HOLE4-40B, M2 HOLE4-40B, M3 HOLE4-40B, M4 HOLE4-40B

STANFORD RESEARCH SYSTEMS		
Title: CLOCK GENERATOR: REAR PANEL INTERFACES		
Size: C	Document Number: CG_MB6D	REV: D
Date: June 1, 2006	Sheet 6 of 6	

MEGAHERTZ KILOHERTZ HERTZ (.) MILLIHERTZ

U1 U2 U3 U4 U5 U6 U7 U8 U9 U10 U11 U12 U13

JP6 HED5: ST5, ST6, Oa, Ob

JP7 HED5: ST4, Oc, Od, Oe, Of

JP8 HED5: ST2, ST3, Og, Odp, Ea

JP9 HED5: ST1, Eb, Ec, Ed, Ee

JP10 HED5: ST0, Ef, Eg, Edp

FIVE CONNECTORS TO 13 DIGIT, SEVEN SEGMENT, DISPLAY DAUGHTER PCB.

JP1 HED5: STB5, STB6, -Oa, -Ob

JP2 HED5: STB4, -Oc, -Od, -Oe, -Of

JP3 HED5: STB2, STB3, -Og, -Odp, -Ea

JP4 HED5: STB1, -Eb, -Ec, -Ed, -Ee

JP5 HED5: STB0, -Ef, -Eg, -Edp

JP11 HEAD40

1	1	-Oa
2	2	-Ob
3	3	-Oc
4	4	-Od
5	5	-Oe
6	6	-Of
7	7	-Og
8	8	-Odp
9	9	
10	10	-Ea
11	11	-Eb
12	12	-Ec
13	13	-Ed
14	14	-Ee
15	15	-Ef
16	16	-Eg
17	17	-Edp
18	18	
19	19	
20	20	STB0
21	21	STB1
22	22	STB2
23	23	STB3
24	24	STB4
25	25	STB5
26	26	STB6
27	27	
28	28	-LAMP0
29	29	-LAMP1
30	30	-LAMP2
31	31	-LAMP3
32	32	-LAMP4
33	33	-LAMP5
34	34	
35	35	-KEY0
36	36	-KEY1
37	37	-KEY2
38	38	-KEY3
39	39	-KEY4
40	40	-KEY5

40 PIN RIBBON CABLE

STB6 STATUS INDICATORS

D1	EXT 10MHz	-LAMP0
D2	SYNTH UNLK	-LAMP1
D3	RS232	-LAMP2
D4	GPIB	-LAMP3
D5	ACTIVITY	-LAMP4
D6	ERROR	-LAMP5

LED, LED-YELLOW, LED, LED, LED, LED-RED

STB5 UNIT INDICATORS

D7	GHz	-LAMP0
D8	MHz	-LAMP1
D9	kHz	-LAMP2
D10	Hz	-LAMP3
D11	DEG	-LAMP4
D12	Vdc	-LAMP5

LED

STB4 Q/-Q LEVEL INDICATORS

D13	5VPECL	-LAMP0
D14	3.3VPECL	-LAMP1
D15	LVDS	-LAMP2
D16	+7dBm	-LAMP3
D17	ECL	-LAMP4
D18	VAR	-LAMP5

LED

STB3 CMOS LEVEL INDICATORS

D19	+5.0V	-LAMP0
D20	+3.3V	-LAMP1
D21	+2.5V	-LAMP2
D22	+1.8V	-LAMP3
D23	+1.2V	-LAMP4
D24	VAR	-LAMP5

LED

STB2 DISPLAYS

D25	FREQ	-LAMP0
D26	PHASE	-LAMP1
D27	Q HIGH	-LAMP2
D28	Q LOW	-LAMP3
D29	CMOS HIGH	-LAMP4
D30	CMOS LOW	-LAMP5

LED

STB1 OTHER DISPLAYS

D31	SHIFT	-LAMP0
D32	REM	-LAMP1
D33	STEP	-LAMP2
D34	STOP	-LAMP3

LED, LED-RED

D35 1N4148

SW1	Q/-Q UP	-KEY0
SW2	Q/-Q DOWN	-KEY1
SW3	SHIFT	-KEY2
SW4	+/-	-KEY3
SW5	(.)	-KEY4
SW6	0	-KEY5

KEY

D36 1N4148

SW7	CMOS UP	-KEY0
SW8	CMOS DOWN	-KEY1
SW9	STORE	-KEY2
SW10	7	-KEY3
SW11	4	-KEY4
SW12	1	-KEY5

KEY

D37 1N4148

SW13	FREQ	-KEY0
SW14	PHASE	-KEY1
SW15	RECALL	-KEY2
SW16	8	-KEY3
SW17	5	-KEY4
SW18	2	-KEY5

KEY

D38 1N4148

SW19	Q/-Q HIGH	-KEY0
SW20	Q/-Q LOW	-KEY1
SW21	BKSP	-KEY2
SW22	9	-KEY3
SW23	6	-KEY4
SW24	3	-KEY5

KEY

D39 1N4148

SW25	CMOS HIGH	-KEY0
SW26	CMOS LOW	-KEY1
SW27	GHz	-KEY2
SW28	MHz DEG	-KEY3
SW29	KHz VOLTS	-KEY4
SW30	Hz ENTER	-KEY5

KEY

D40 1N4148

SW31	MODIFY UP	-KEY0
SW32	MODIFY DOWN	-KEY1
SW33	STEP SIZE	-KEY2

KEY

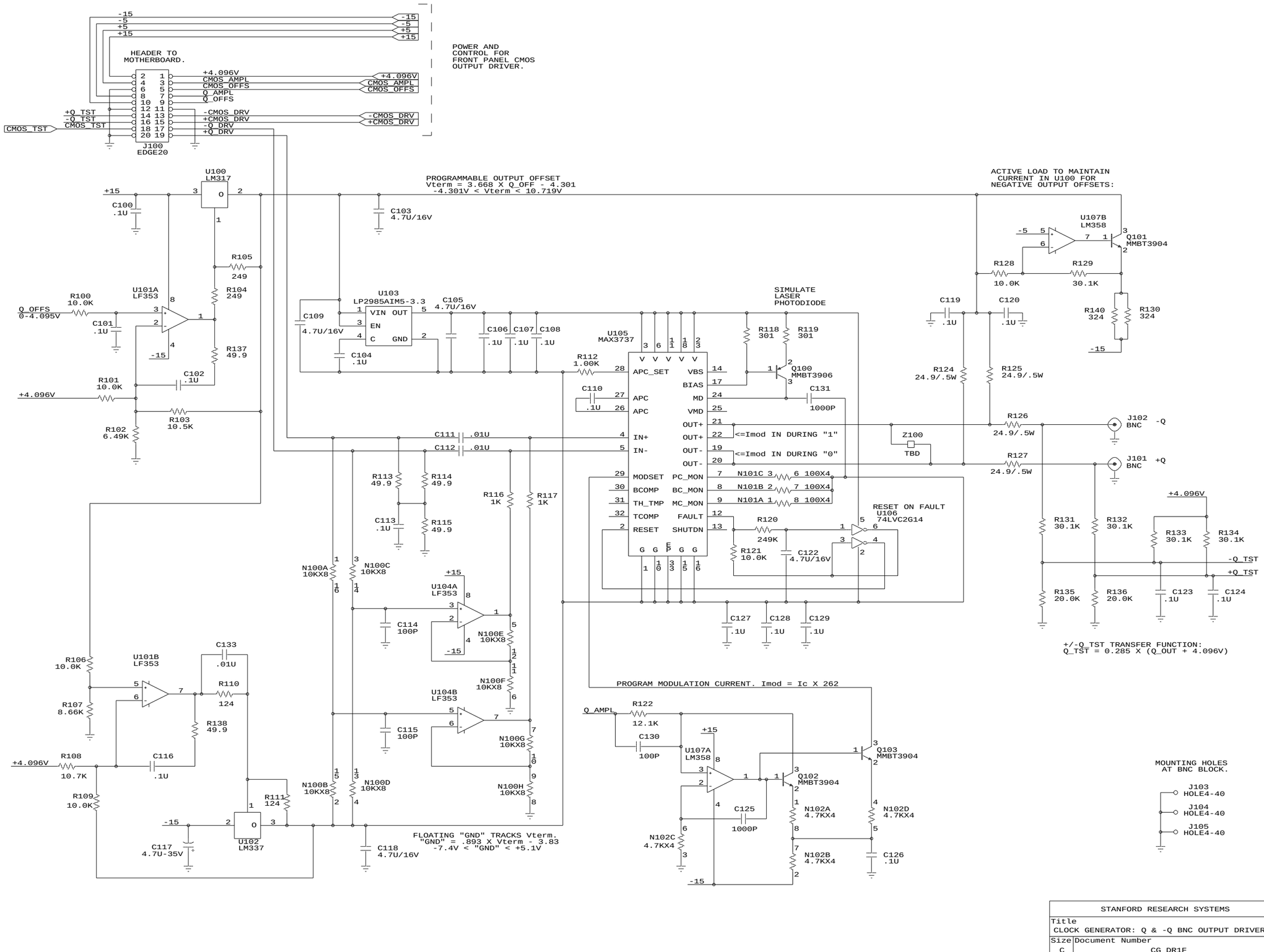
Display PCB for 13 Digits, 34 Lamps, and 33 Keys

STANFORD RESEARCH SYSTEMS

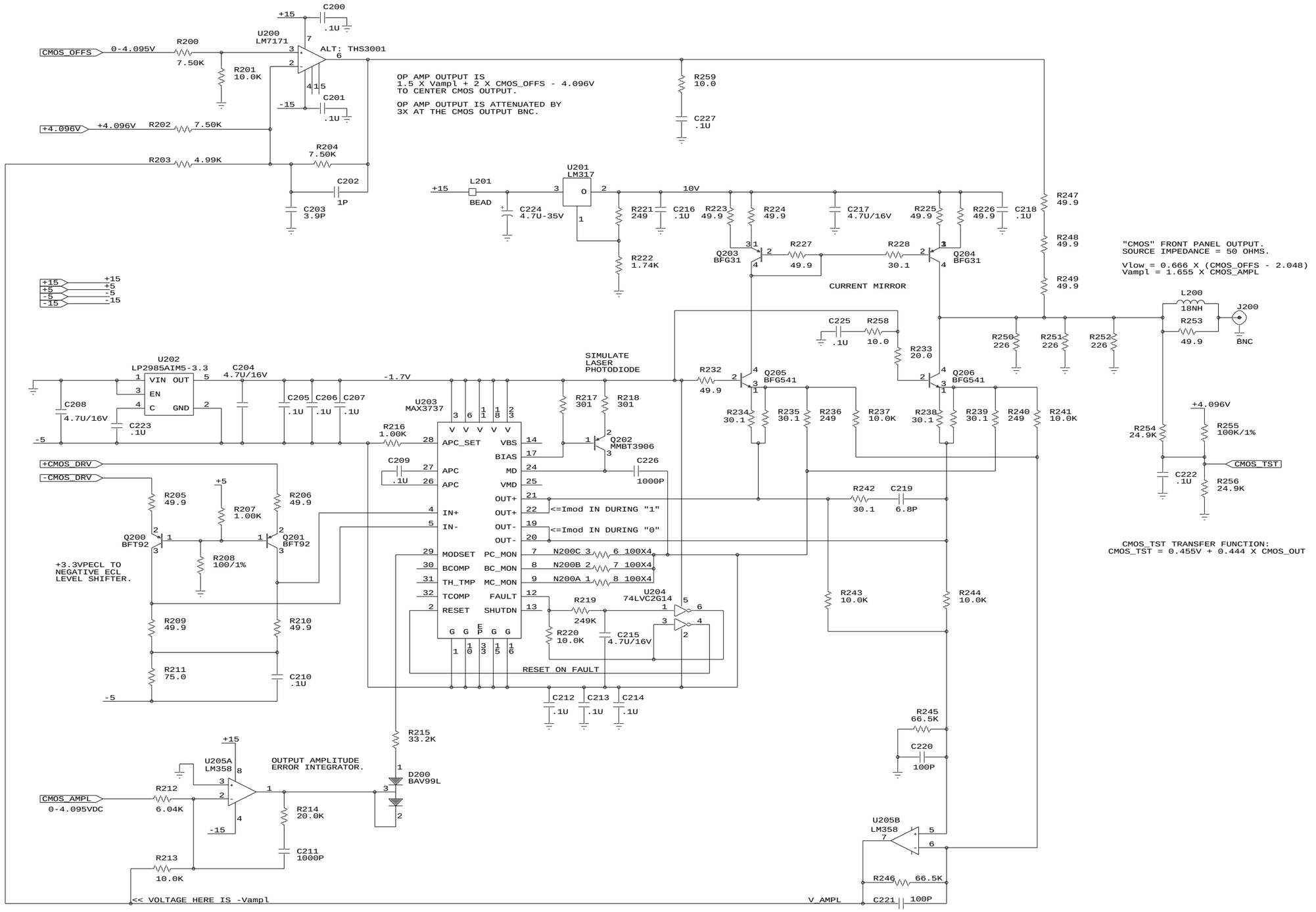
Title: CLOCK GENERATOR: FRONT PANEL KEYS AND LAMPS.

Size	Document Number	REV
C	CG_FP1B	B

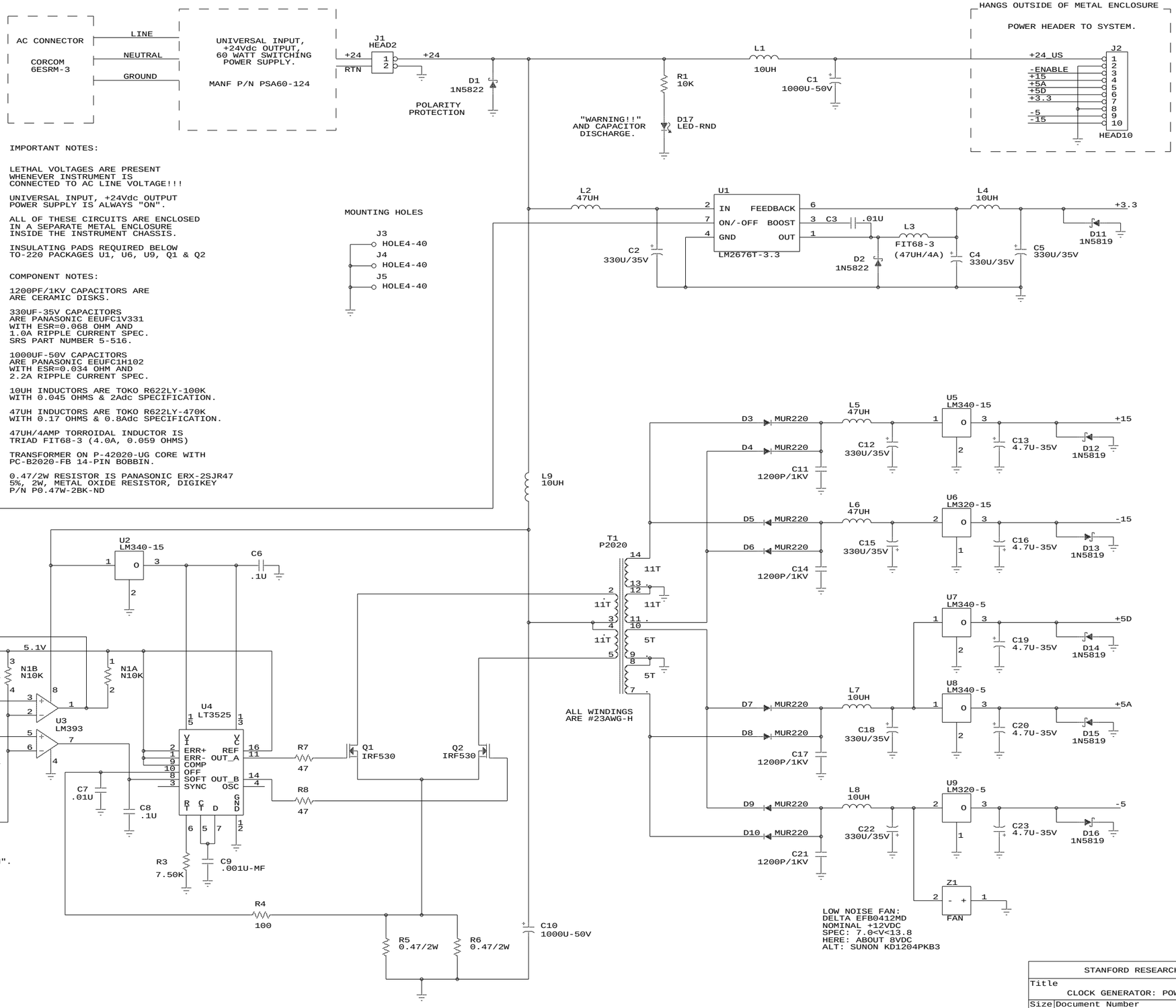
Date: February 11, 2005 Sheet 1 of 1



STANFORD RESEARCH SYSTEMS		
Title: CLOCK GENERATOR: Q & -Q BNC OUTPUT DRIVERS.		
Size: C	Document Number: CG_DR1F	REV: F
Date: September 29, 2005	Sheet 1 of 2	



STANFORD RESEARCH SYSTEMS		
Title: CLOCK GENERATOR: CMOS BNC OUTPUT DRIVER.		
Size: C	Document Number: CG_DR2F	REV: F
Date: September 29, 2005	Sheet 2 of 2	



STANFORD RESEARCH SYSTEMS		
Title: CLOCK GENERATOR: POWER SUPPLIES		
Size: C	Document Number: CG_PS1B	REV: B
Date: February 11, 2005	Sheet 1 of 1	

WIDTH Z(OHMS)
0.015" 48
0.029" 25
0.033" 20
(FR-4, e=4.3, t=0.008")
DELAY APPROX. 150PS/INCH

CONTROLLED IMPEDANCE TEST AREA
SMA_TST J8 8.0"x0.015" R60 49.9T

PHYSICALLY SHORT TRACES DUE TO CIRCULAR PCB LAYOUT.

USER TO TERMINATE BOTH OUTPUTS! (LVDS LEVELS)

+5A R32 499 R33 30.1
EN_PRBS R31 750/1% Q1 BFT92
SOURCES 24mA TO FORCE ALL 1'S.

+3.3 C23 .1U
U8 MC100EP08 (VCC A, AXB A, AXB B, VEE B)

U10 NB6L16 (INVERTER) NC VCC D Q D Q VBB VEE
+3.3 C24 .1U
+5A C29 .1U
R48 100 R49 100 J5 SMA -PRBS
R50 324 R51 324
R52 100 R53 100 J4 SMA PRBS

R28 47 R29 47 R30 47 C8 .1U
+3.3 C9 .1U

U1 MC100EP52 (D VCC, D Q, CLK Q, CLK VEE)
R7 47 R8 47 R9 47 C10 .1U
R4 20.0 R5 20.0 R6 20.0 C7 .1U

+3.3 C11 .1U
U2 MC100EP52
R10 47 R11 47 R12 47 C12 .1U

+3.3 C13 .1U
U3 MC100EP52
R13 47 R14 47 R15 47 C14 .1U

+3.3 C15 .1U
U4 MC100EP52
R16 47 R17 47 R18 47 C16 .1U

+3.3 C17 .1U
U5 MC100EP52
R19 47 R20 47 R21 47 C18 .1U

+3.3 C19 .1U
U6 MC100EP52
R22 47 R23 47 R24 47 C20 .1U

+3.3 C21 .1U
U7 MC100EP52
R25 47 R26 47 R27 47 C22 .1U

R42 47 R43 47 R44 47 C27 .1U

<==85PS DELAY==> <==85PS DELAY==> <==85PS DELAY==> <==85PS DELAY==> <==85PS DELAY==>

<===COUNTER-PROPAGATING 20 OHM DIFFERENTIAL CLOCK.

+3.3 C6 .1U
U9 NB6L11 (Q VCC, Q IN, Q IN, Q VEE)
20 OHM CLOCK DRIVER

"JUMPER" BOARD CONNECTS PRBS OPTION TO MOTHER BOARD.
J6 S2106
J7 S2105
PINS 4&7 USE POWER PLANE.
PINS 3&8 USE GND PLANE.
HOLE4-40 M2
HOLE4-40 M3

L2 BEAD +5A
C1 .1U C2 .1U
HOLE4-40 M1
L3 BEAD +3.3
C3 4.7U C4 .1U

J1 S2105
EN_PRBS
+PRBS_CLK
-PRBS_CLK
-5 (NOT USED)
PINS 3&8 ARE CIRCUIT GND.
PIN9 ACTS AS "-PRBS_OPT"

+3.3 C26 .1U
U12 NB6L11 (VCC Q, IN Q, IN Q, VEE Q)
R1 47 R2 47 R3 47 C5 .1U

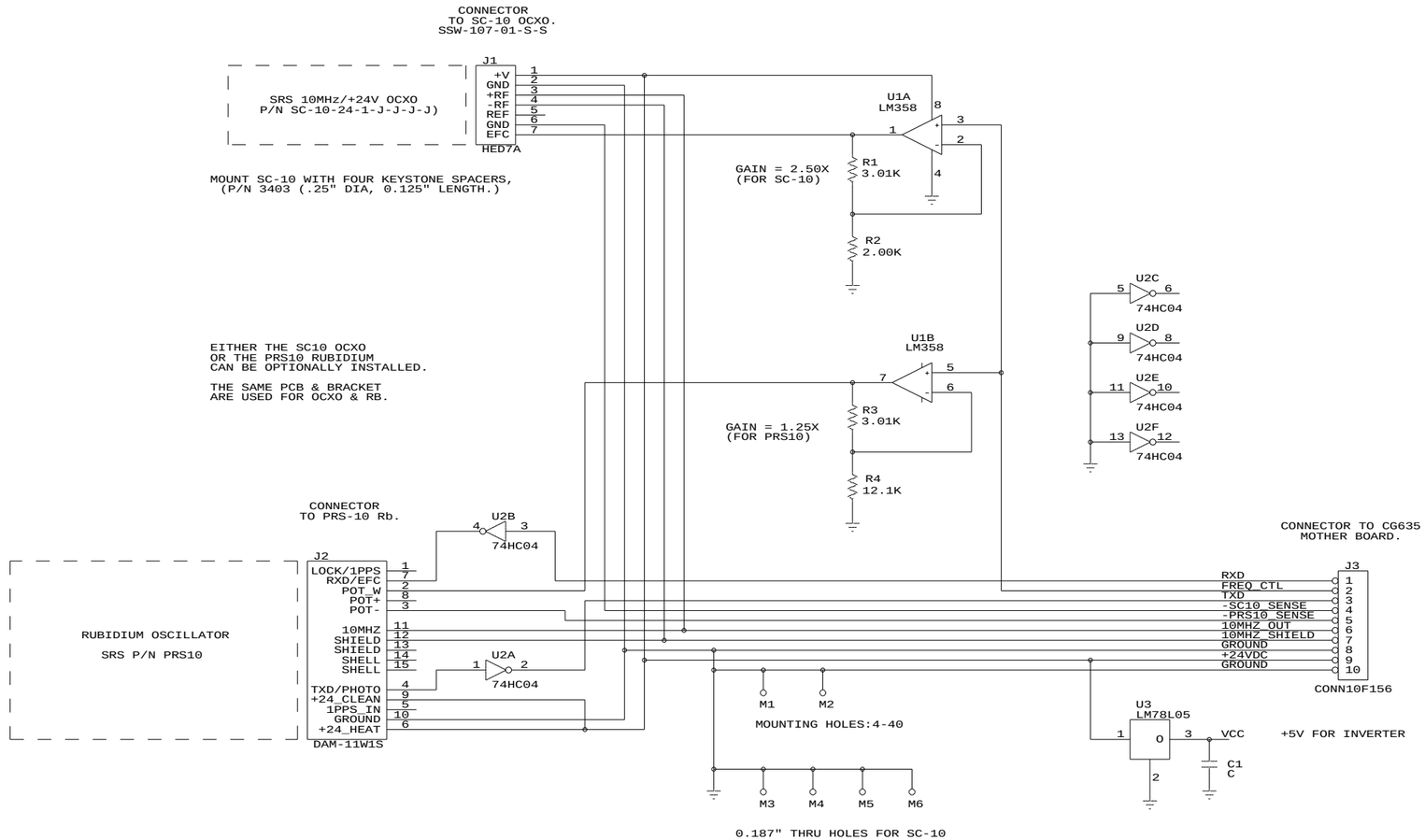
DELAY LINE SO THAT RISING EDGE OF CLOCK IS COINCIDENT WITH PRBS DATA TRANSITION.

U11 NB6L16 (INVERTER) NC VCC D Q D Q VBB VEE
+3.3 C25 .1U
+5A C30 .1U
R54 100 R55 100 J3 SMA -CLK
R56 324 R57 324
R58 100 R59 100 J2 SMA CLK

R45 47 R46 47 R47 47 C28 .1U

USER TO TERMINATE BOTH OUTPUTS! (LVDS LEVELS)

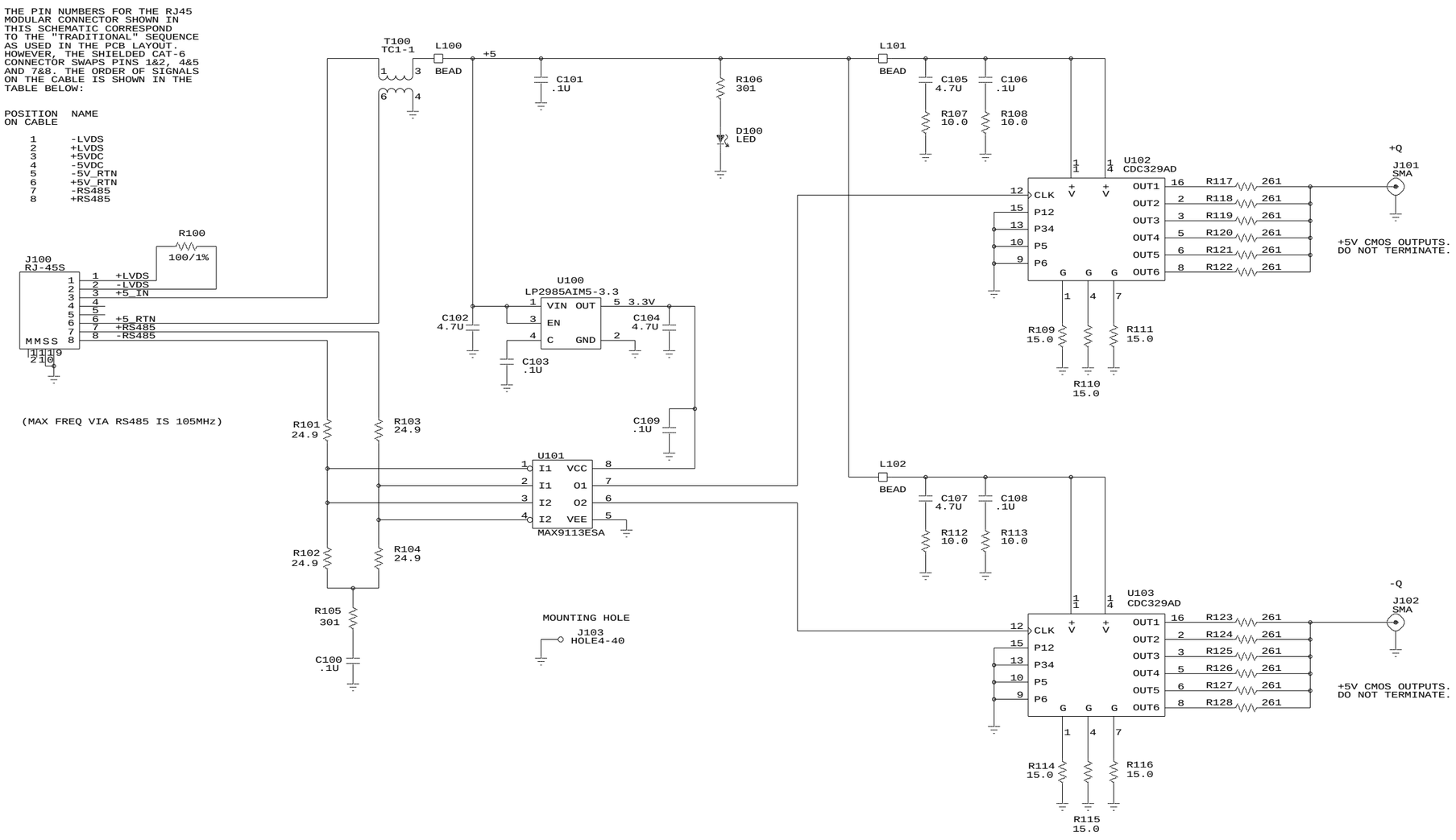
STANFORD RESEARCH SYSTEMS		
Title: CLOCK GENERATOR: PRBS OPTION		
Size: C	Document Number: CG_PR1B	REV: B
Date: March 22, 2005	Sheet 1 of 1	



STANFORD RESEARCH SYSTEMS		
Title: CLOCK GENERATOR: TIMEBASE OPTION ADAPTER		
Size: C	Document Number: CG_TB1B	REV: B
Date: February 15, 2005	Sheet 1 of 1	

THE PIN NUMBERS FOR THE RJ45 MODULAR CONNECTOR SHOWN IN THIS SCHEMATIC CORRESPOND TO THE "TRADITIONAL" SEQUENCE AS USED IN THE PCB LAYOUT. HOWEVER, THE SHIELDED CAT-6 CONNECTOR SWAPS PINS 1&2, 4&5 AND 7&8. THE ORDER OF SIGNALS ON THE CABLE IS SHOWN IN THE TABLE BELOW:

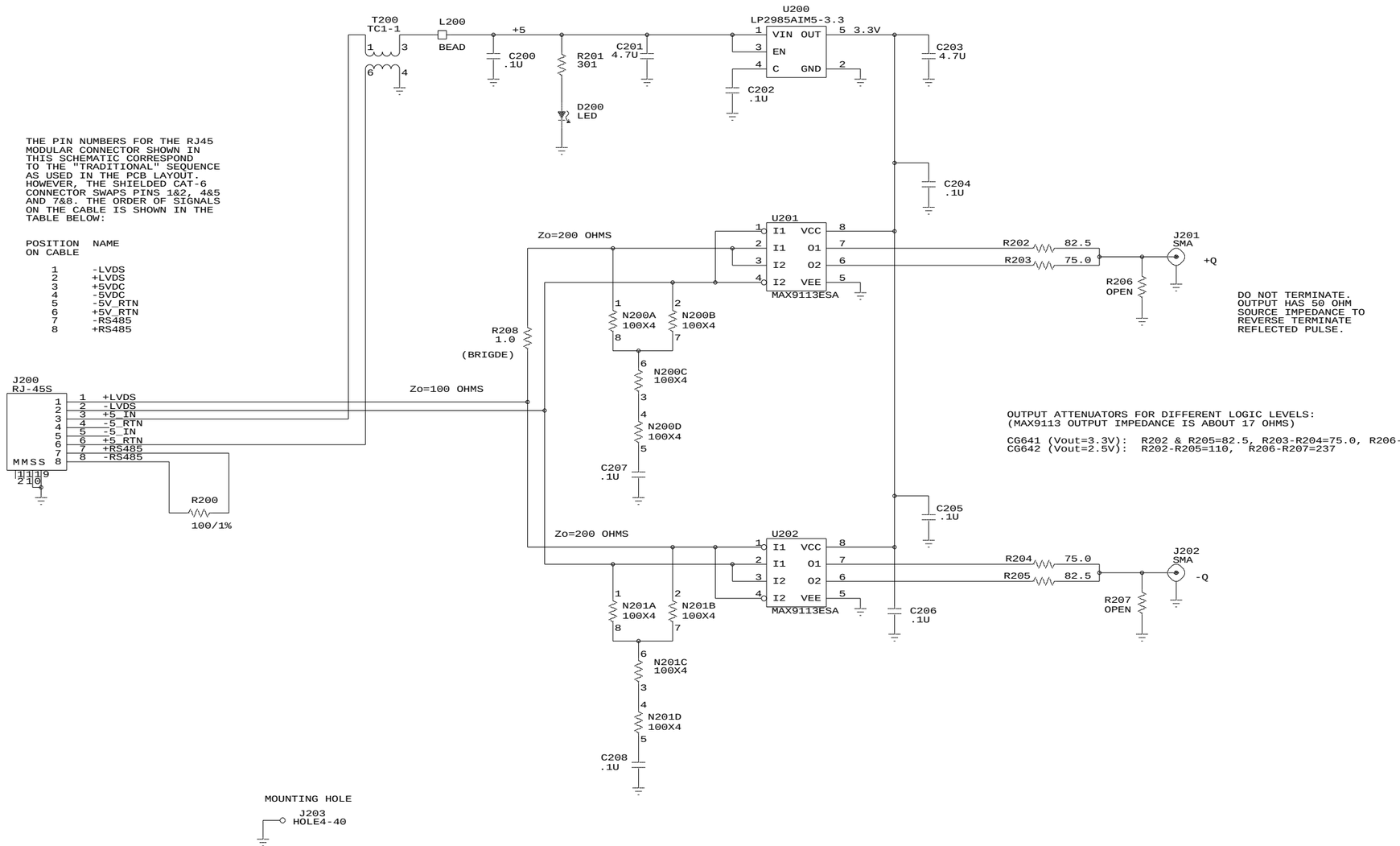
POSITION ON CABLE	NAME
1	-LVDS
2	+LVDS
3	+5VDC
4	-5VDC
5	-5V_RTN
6	+5V_RTN
7	-RS485
8	+RS485



STANFORD RESEARCH SYSTEMS		
Title: CG640: RS485 TO +5V CMOS LINE RECEIVER		
Size: C	Document Number: CG_LR1B	REV: B
Date: June 2, 2006	Sheet 1 of 6	

THE PIN NUMBERS FOR THE RJ45 MODULAR CONNECTOR SHOWN IN THIS SCHEMATIC CORRESPOND TO THE "TRADITIONAL" SEQUENCE AS USED IN THE PCB LAYOUT. HOWEVER, THE SHIELDED CAT-6 CONNECTOR SWAPS PINS 1&2, 4&5 AND 7&8. THE ORDER OF SIGNALS ON THE CABLE IS SHOWN IN THE TABLE BELOW:

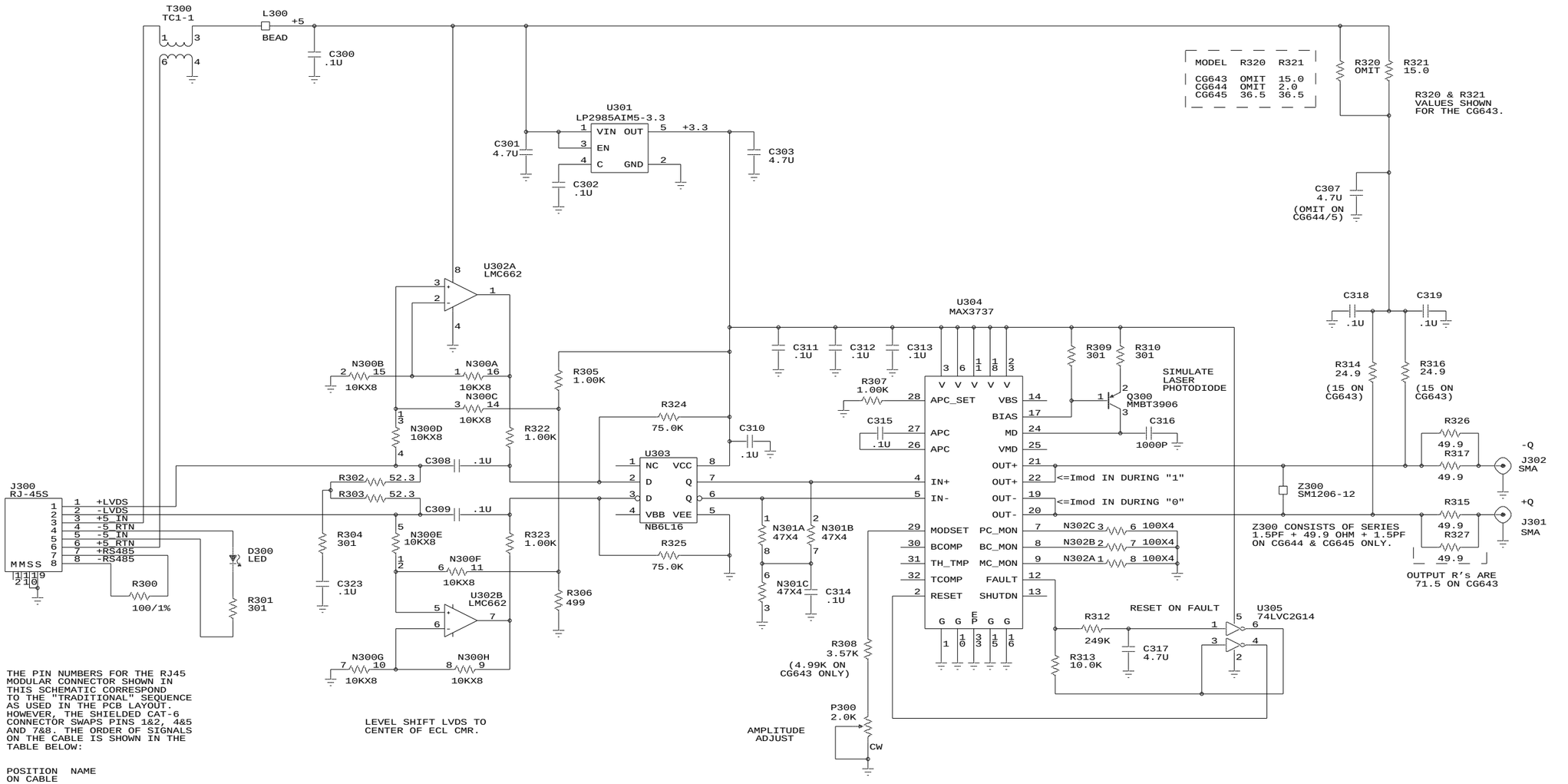
POSITION ON CABLE	NAME
1	-LVDS
2	+LVDS
3	+5VDC
4	-5VDC
5	-5V_RTN
6	+5V_RTN
7	-RS485
8	+RS485



STANFORD RESEARCH SYSTEMS		
Title: CG641/642: HIGH SPEED CMOS LINE RECEIVER		
Size: C	Document Number: CG_LR2B	REV: B
Date: June 2, 2006	Sheet 2 of 6	

OUTPUT LOGIC LEVELS PER MODEL NUMBER:

MODEL CG643, 5.0V PECL: OUTPUT TERM=OPEN, Vhigh=4.0V, Vlow=3.2V
MODEL CG644, 3.3V PECL: OUTPUT TERM=50 OHMS, Vhigh=2.3V, Vlow=1.5V
MODEL CG645, 2.5V PECL: OUTPUT TERM=50 OHMS, Vhigh=1.5V, Vlow=0.7V



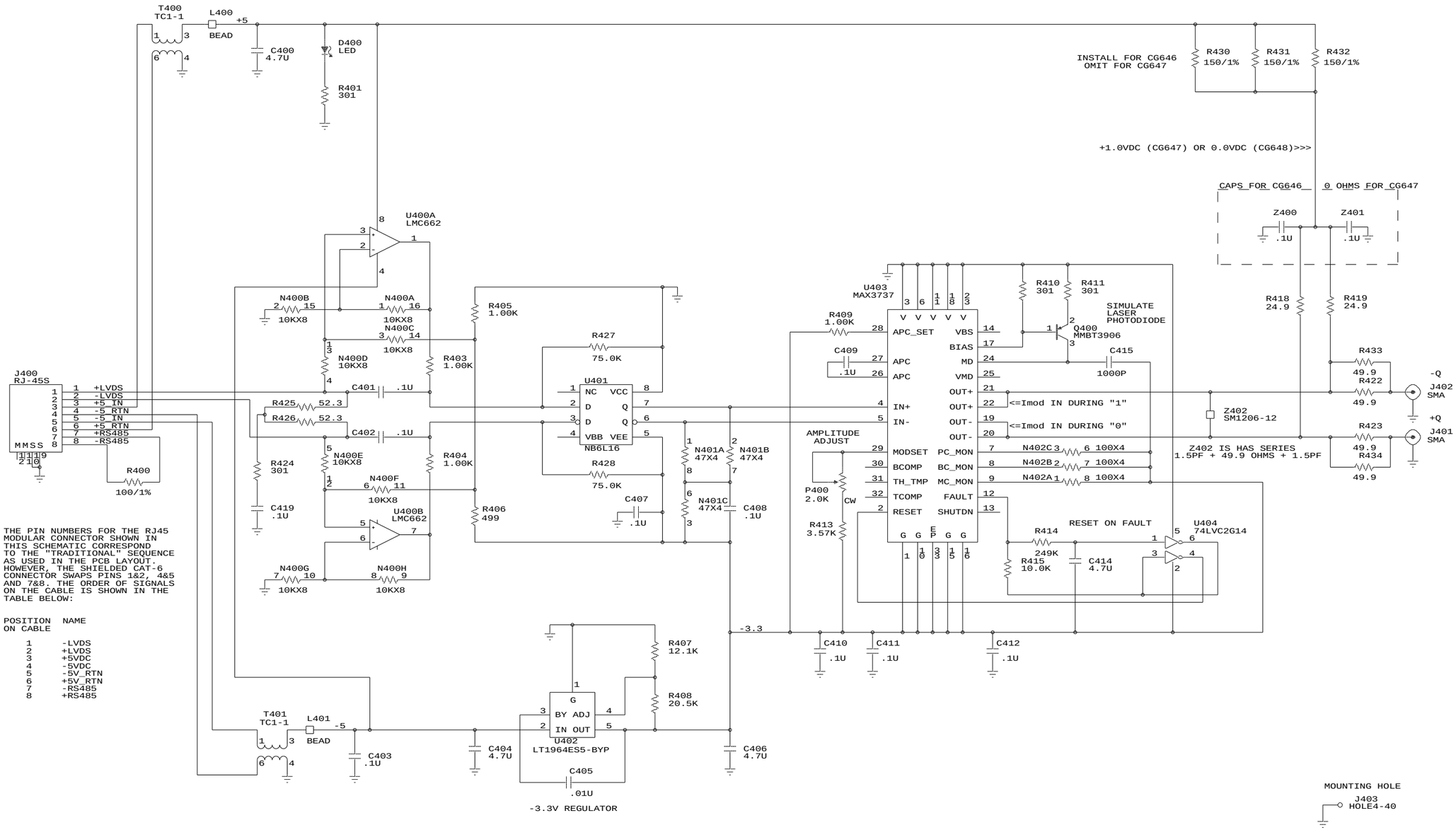
THE PIN NUMBERS FOR THE RJ45 MODULAR CONNECTOR SHOWN IN THIS SCHEMATIC CORRESPOND TO THE "TRADITIONAL" SEQUENCE AS USED IN THE PCB LAYOUT. HOWEVER, THE SHIELDED CAT-6 CONNECTOR SWAPS PINS 1&2, 4&5 AND 7&8. THE ORDER OF SIGNALS ON THE CABLE IS SHOWN IN THE TABLE BELOW:

POSITION ON CABLE	NAME
1	-LVDS
2	+LVDS
3	+5VDC
4	-5VDC
5	-5V_RTN
6	+5V_RTN
7	-RS485
8	+RS485

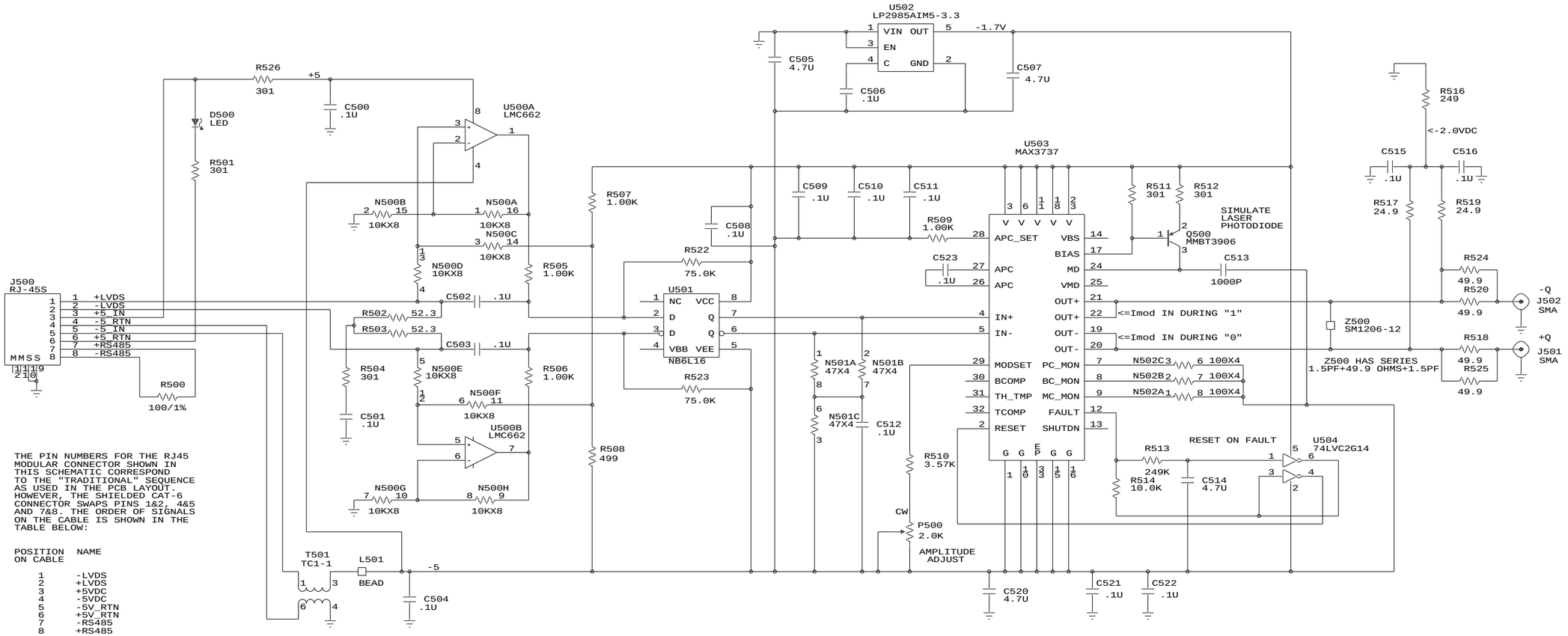
LEVEL SHIFT LVDS TO CENTER OF ECL CMR.

MOUNTING HOLE
J303
HOLE4-40

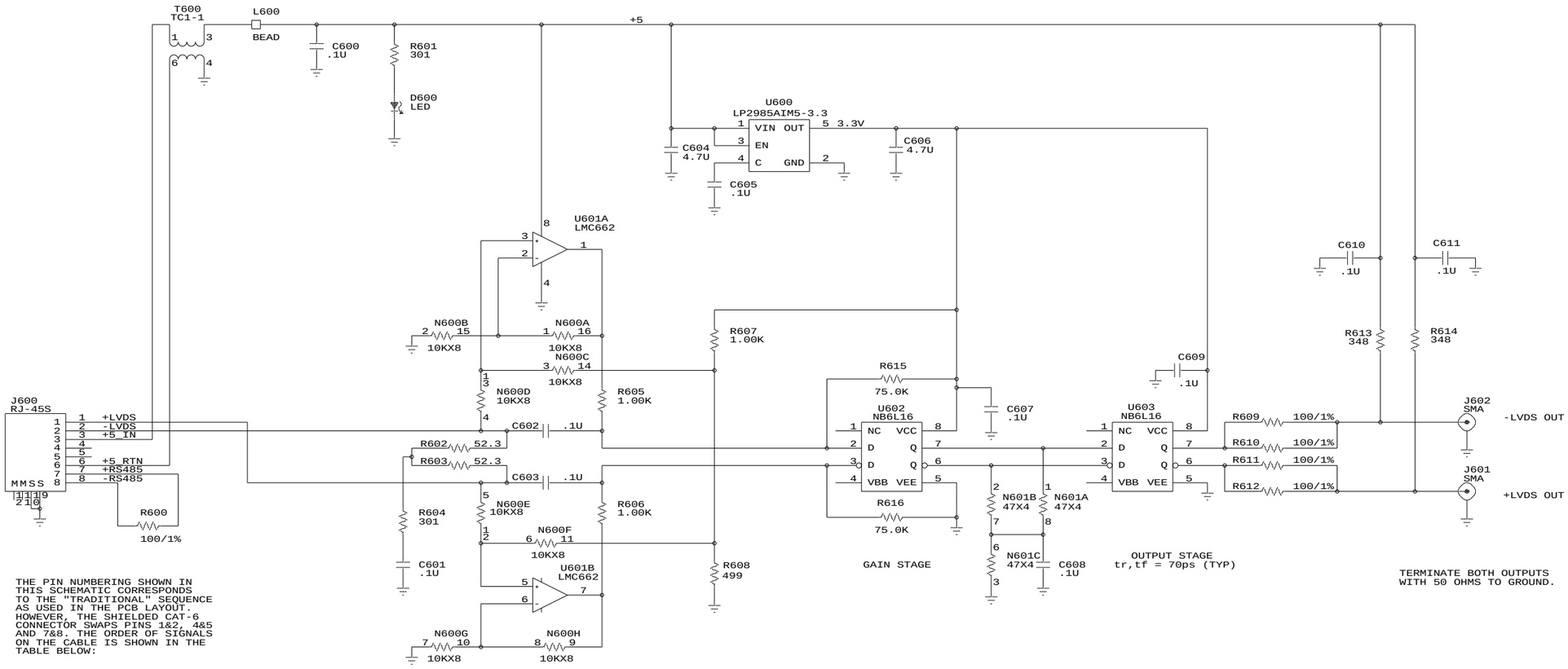
STANFORD RESEARCH SYSTEMS		
Title: CG643-CG645 PECL LINE RECEIVERS		
Size: C	Document Number: CG_LR3B	REV: B
Date: June 2, 2006	Sheet 3 of 6	



STANFORD RESEARCH SYSTEMS		
Title: CG646,CG647: RF & CML/NIM LINE RECEIVERS		
Size: C	Document Number: CG_LR4B	REV: B
Date: June 2, 2006	Sheet 4 of 6	



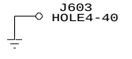
STANFORD RESEARCH SYSTEMS		
Title: CG648: NEG ECL LINE RECEIVERS		
Size: C	Document Number: CG_LR5B	REV: B
Date: June 2, 2006	Sheet 5 of 6	



THE PIN NUMBERING SHOWN IN THIS SCHEMATIC CORRESPONDS TO THE "TRADITIONAL" SEQUENCE AS USED IN THE PCB LAYOUT. HOWEVER, THE SHIELDED CAT-6 CONNECTOR SWAPS PINS 1&2, 4&5 AND 7&8. THE ORDER OF SIGNALS ON THE CABLE IS SHOWN IN THE TABLE BELOW:

POSITION ON CABLE	NAME
1	-LVDS
2	+LVDS
3	+5VDC
4	-5VDC
5	-5V_RTN
6	+5V_RTN
7	-RS485
8	+RS485

MOUNTING HOLE



STANFORD RESEARCH SYSTEMS		
Title: CG649: ULTRAFAST LVDS LINE RECEIVER		
Size: C	Document Number: CG_LR6B	REV: B
Date: June 2, 2006	Sheet 6 of 6	