Reference Voltage Buffer for a 12-bit 8 MS/s SAR ADC based on hybrid RC DAC in 0.13 μm CMOS

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***Abstract*—Fast settling, accurate reference voltage buffer (RVB) are one of the key blocks of a successive approximation register (SAR) ADC. This paper presents the design of buffer, targeted for a 12-bit, 8 MS/s SAR ADC architecture which employs a hybrid RC DAC, and is implemented in 0.13 μm CMOS. The design challenges associated with RVB, which is capable of driving a hybrid RC DAC : a popular architecture enabling area-efficient SAR architecture, is shown. The buffer operates from a 1.2V supply and consumes 760 μA current while occupying $1530\mu m^2$ of area. It is capable of settling to better than 12-bit accuracy within 3.9ns and has a total output noise of 87 μV. Post-layout simulations together with the entire SAR ADC shows a ENOB of 11.5 bits thus confirming that the proposed reference voltage buffer serves the targeted application.**

I. Introduction

SAR ADC has been a popular architecture choice for data-converter design because it scales well with lower CMOS technology node as well as is low power. It only consists of an input sampling network made of switches and a capacitive charge redistribution based DAC, which together with a comparator sequentially converts the analog input to digital code. There have been numerous publications in literature discussing SAR ADC design with emphasis on improving the power and area efficiency, making them a good candidate for fast, power-efficient solution for medium resolution ADCs. One of the key component that determines the overall performance of the SAR ADC is the reference buffer which drives the DAC used to measure the input signal against. Typically such a reference voltage to the ADC can be provided by a discrete voltage reference buffer IC. In comparison, implementing an on-chip reference buffer is beneficial because it saves area on the PCB, reduces system cost and consumes lower overall power.

In this work, we present design details of RVB targeted for a 12-bit 8 MS/s SAR ADC. The paper is organized as follows. Section II describes the motivation for choice of the RVB and provides details of load i.e. hybrid DAC array used in this particular SAR ADC and its impact on the RVB design. Section III provides the design details of the proposed reference voltage buffer operation. Section IV presents the key post-layout simulation results followed by conclusion.

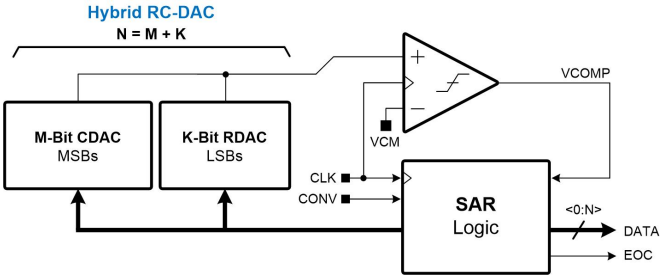

Fig. 1. Hybrid capacitor-resistor DAC for SAR ADC

II. Motivation for the reference voltage buffer

The speed bottleneck in high-speed SAR ADCs which require medium-to-high resolution (>8 bits) is determined by the settling time required by the DAC. SAR ADC of N-bit resolution requires N clock cycles to complete each conversion. In this work, we allocate 4 cycles for sampling the input, which translates to (N+4) cycles for overall conversion. For a 12-bit 8 MS/s, this translates to a ADC sample clock (f_{clk}) of 128 MHz. Therefore the buffer driving the DAC is expected to settle within $\frac{1}{2}$ LSB of 12-bit resolution in half-cycle of time period ($T_{per} = 7.8125$ ns). For a dynamic range of 0.8V, this translates to an error below 97 μV.

Traditionally off-chip reference drivers are employed in some applications. In the current system, the target application of the ADC is for a high-energy particle detector akin to an imager which consists of several ADC. Therefore integrated reference voltage buffers are essential. Besides it is seen that off-chip reference drivers are prone to ringing (much larger than LSB targeted) due to the associated bondwire inductance, which is in the order of few nH [1]. One way to overcome this is to ensure that the time instant of sampling is after the ringing is settled completely. This is challenging given the timing margin is decided by the overall throughput of the ADC and in most cases impossible. Alternative techniques such as using capacitors to absorb the transient ripple is not feasible as the required size is large. Therefore on-chip RVBs providing the three voltages (Vp,Vcm,Vn) to the SAR ADC is required.

Power dissipation and chip area of a SAR ADC is af-

fected by the design of the DAC. One strategy to reduce this is to lower the total capacitance used to implement the DAC. Hybrid DACs are useful for efficient realization over conventional capacitive DAC [2]. N-bit hybrid DAC consists of a K-bit voltage-scaling resistive array together with M-bit charge-redistribution capacitive array (N=M+K). For the first "M" conversions to determine the "M" most significant bits, the capacitive DAC is active followed by resistive DAC to determine the next "K" least significant bits. By using this technique, it can be seen that the overall capacitance of the DAC compared to the conventional capacitive DAC is reduced by 2^K. It should be noted that in the hybrid DAC structure, the total capacitance ($2^M \cdot C_{unit}$) should still satisfy the thermal noise (kT/C) requirement as well as the mismatch requirement. Fig. 1 shows a possible implementation of hybrid DAC based SAR ADC [**?**]. Such a DAC architecture poses additional requirement on the reference voltage buffer. Reference voltage buffer suffers from disturbance when capacitors are charged or discharged, as well as during the transition between different impedances ,in case of hybrid DAC based SAR architecture, during cycles of conversion.

The buffer should be able to drive both capacitive and resistive loads. The absolute reference voltage magnitude should not change between the two parts of the conversion i.e. during SAR conversion of M-bits which is capacitive loading and subsequent K-bits which is resistive loading (any offset constant or varying is detrimental to the ENOB of the ADC). On-chip NMOS Source follower [1] based reference buffer provides bandwidth to recover the voltage within a limited time but at the cost of a higher supply voltage and higher power consumption. In comparison flipped voltage follower (FVF) based buffer can operate at a lower power consumption. FVF is a popular architecture for driving loads since it offers a low output impedance compared to its common-drain amplifier as well as it can drive large load currents without disturbing the transconductance of the input MOS device. This ensures good stability across different load conditions.

Conventional FVF based reference buffer consists of two parts: the voltage control generator followed by the FVF output stage. Typically the output stage is replicated to provide the required drive capability at the load. This replica output stage is not applicable if the load impedance changes (for example between capacitance and resistance in case of hybrid DAC [**?**]). This implies that the load should be directly driven by the output stage, as well as it requires additional negative feedback to set the output voltage to ensure the voltage does not vary during the change of impedance type in the hybrid DAC load (explained in later section). This approach was chosen over other method such as using a replica feedback [3], which relies on symmetrical load to ensure the correct output voltage.

III. Reference Voltage Buffer Design

Fig. 2 shows the design of the proposed reference voltage buffer for driving the positive reference (1 V) of the SAR ADC ($Vrefp$). A complementary version is shown on the right which is used for negative reference($Vrefn$=0.2V) as well as

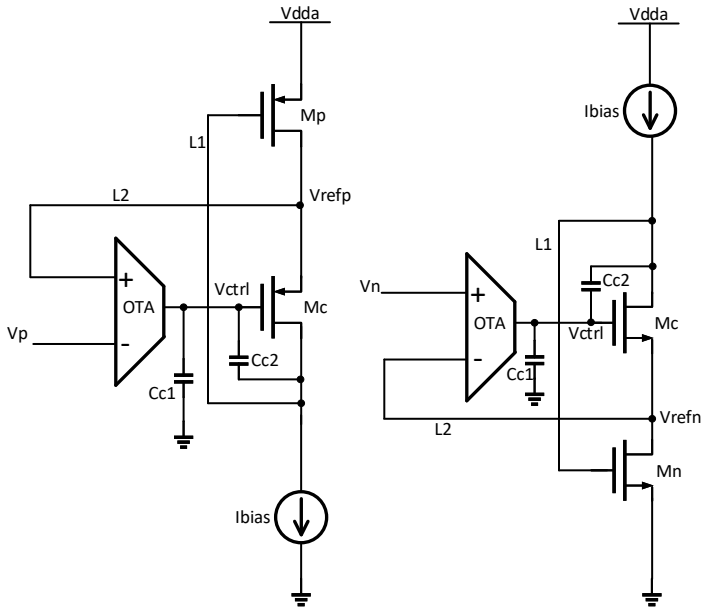

Fig. 2. Architecture of Reference Voltage Buffer (note : Identical node names used for representation only)

similar version for common-mode reference (Vcm=0.6V). It consists of the output stage (local shunt feedback loop shown by loop "L1") which comprises a flipped voltage follower (FVF) used to provide a low impedance node driving the $Vrefp$ and as will be seen later has a large bandwidth to support the high-speed settling. The minimum supply required for the FVF stage is given by:

$Vdd_{min} = 2 \cdot V_{dsat} + V_{thp}$

The biasing of Mc is implemented using another negative feedback loop (shown by loop "L2") comprising of an amplifier, which takes the input from a central bandgap reference.

In Fig. 2, Ibias is the main bias current of the output stage and is always constant through Mc irrespective of the load current requirement. Ibias (410) sets the transconductance (6.7mS) of the input device Mc. The local negative feedback controls the V_{gs} of Mp so as to be able to source current $Ibias + I_{load}$. When $Vrefp$ changes, the transistor Mc senses this at the drain and in turn controls the gate voltage of Mp, which controls the output current thus bringing the output voltage back to $Vrefp = Vp$.

Mc is operated in open-loop $Vrefp = V_{gMp} + V_{gsMc}$
V_{gsMc} = constant since the Ibias is fixed.

In order to keep $Vrefp$ constant, we need to ensure gate of Mc is constant across PVT. This is achieved by lower bandwidth feedback loop (indicated by loop "L2"). The OTA in negative feedback regulates the gate voltage of Mc such that: $Vrefp = Vp$

where Vp is derived from a central bandgap. The OTA in feedback is implemented as a folded-cascode stage with a transconductance of 2mS. Decoupling capacitor Cc1 (0.8pF) is placed at the gate of M1 so as to isolate any switching noise from coupling as a result of charge redistribution through gate-source capacitance of M1 during switching transients on

$Vrefp$, besides together with Cc2 (0.2pF) ensures the FVF stage is stable during cycles of SAR conversion. The load capacitor Cc1 also ensures the OTA is stable by establishing a dominant pole. The output impedance is given by eqn. (1), where gmc, roc are the transconductance and output resistance of Mc, while gmp is transconductance of Mp and A is the open-loop gain of the feedback OTA.

$$r_{out} = (gm_{Mp} * R_{op} * A * gm_{Mc})^{-1} \tag{1}$$

The open-loop gain of the FVF stage is given by:

$$A_{fvf} = -gm_{Mp} \cdot R_{ol} \tag{2}$$

where $R_{ol} = R_b||(g_{Mc} \cdot R_{oc}||R_{op})$

The poles associated with the FVF [4] are at X (non-dominant) and at Y (dominant) given by:

$$\omega_Y = \frac{1}{Cy \cdot Ry}$$
$$where: Ry = Rb||(gm_{Mp} \cdot gm_{Romp} \cdot Ro_{Mp} \cdot Ro_{Mc})$$
$$\omega_X = \frac{1}{Cx \cdot Rx}$$
$$where: Rx = \left[(1 + \frac{R_b}{R_{Mc}})/gm_{Mc}\right]||Ro_{Mp}$$

There is a zero formed by the load capacitance together with the switch-ON resistance of the capacitive DAC.

$$\omega_z = \frac{1}{R_{sw} \cdot C_{load}} \tag{3}$$

The load capacitance seen by the buffer is approximately 1.2 pF which is the MSB capacitance of the charge redistribution DAC through the switches of the SAR ADC. The settling time is within 3.9 ns to about 12 bit resolution. This translates to large bandwidth requirement of the FVF output stage.

The buffer needs to replenish the change in output voltage within the alloted time. This sets the slew rate as below and is provided by the Class-AB operation of the FVF.

$$\frac{\Delta Vref_{SAR}}{t_{slew}} = \frac{0.8}{0.25 \cdot 3.9 \cdot 10^{-9}} = \frac{I_{out}}{C_L} \tag{4}$$

For a load capacitance of 1.2pF, the minimum output current translates to:

$$I_{out} = 984\mu A \tag{5}$$

The negative voltage buffer ($Vrefn = 0.2V$) as well as common mode voltage buffer ($Vcm = 0.6V$) is implemented using similar architecture as shown in Fig. 2 but using the NMOS counterpart (M1,M2 are replaced by NMOS and Ibias is a sourcing). The specifications are similar for the $Vrefn$ buffer since it sees similar load as the $Vrefp$ buffer while the specification for common mode voltage buffer is different.

Vcm buffer sees a larger load of approximately 4.2 pF but also has 4 cycles to settle during the initial input signal sampling, but subsequently has same settling requirement ($1/2$ period of sample clk) during conversion cycles.

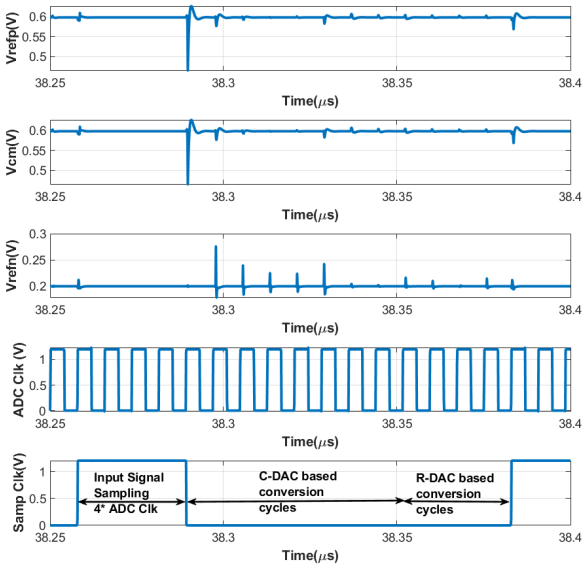

Fig. 3. Reference Buffer settling during SAR ADC conversion

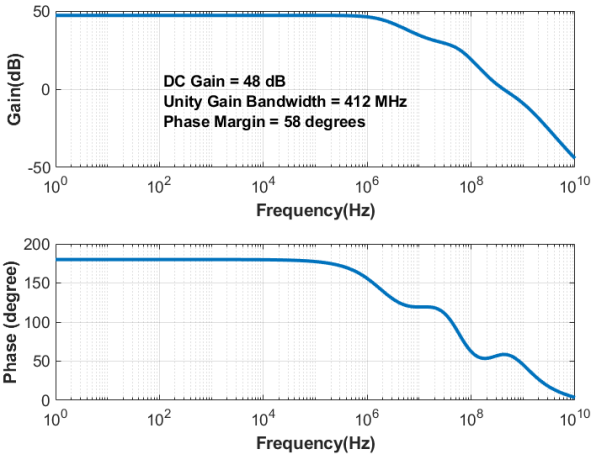

Fig. 4. Open loop Simulation of FVF loop

IV. Simulation Results

Transistor level simulations of the proposed reference voltage buffer shown in Fig. 2 were completed. As first step, the stability of the buffer was evaluated. The open-loop simulation was done by breaking the loop shown by "blue" wire and output node $Vref_{SAR}$ was loaded by switches together with the capacitance of 1.2pF. This represents the performance of the output FVF loop and has the larger bandwidth. Fig. 4 shows the gain and phase plot which shows a DC open-loop gain of 48 dB with unity gain bandwidth of 412 MHz while having phase margin of 58 degrees.

The other negative feedback loop (shown in "purple" wire) used to regulate the V_{ctrl} voltage to ensure the output is set

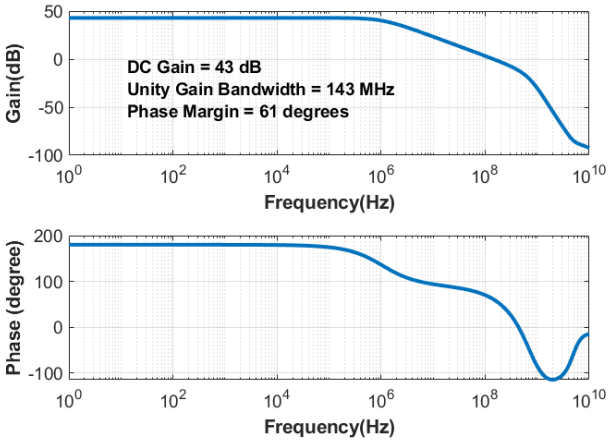

Fig. 5. Open loop Simulation of negative feedback loop

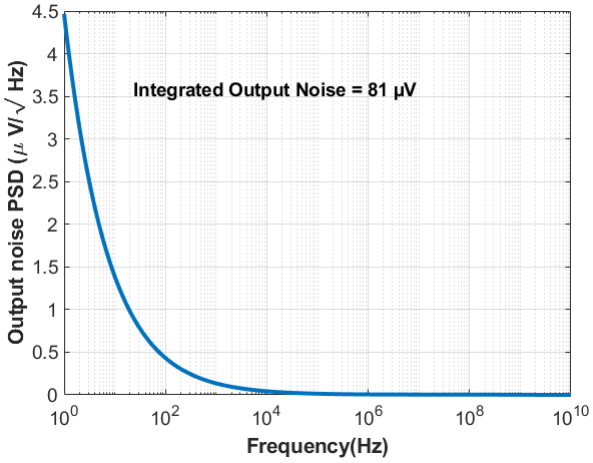

Fig. 6. Output Noise PSD of the reference voltage buffer

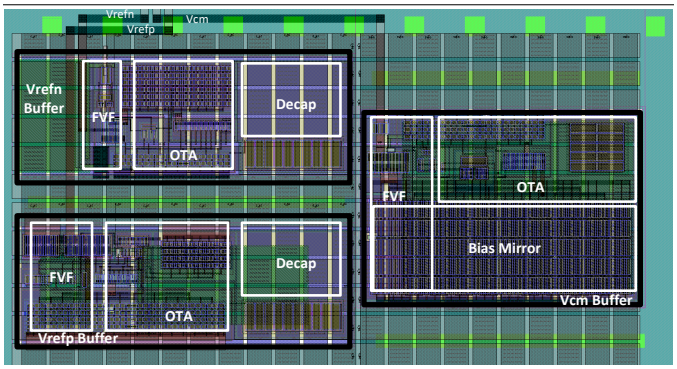

Fig. 7. Layout of the reference voltage buffer

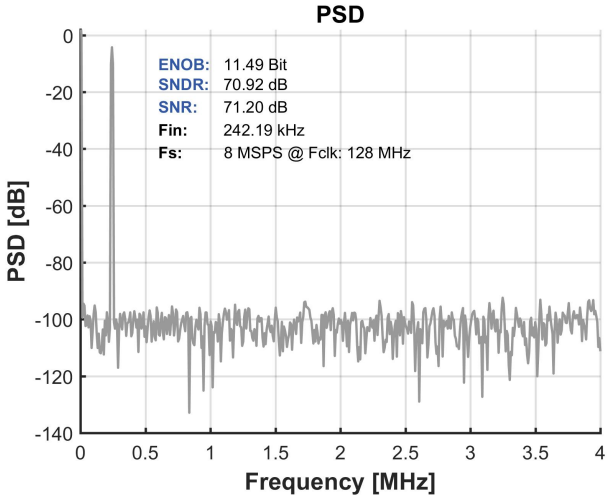

Fig. 8. Transient post-layout simulation of the buffers (Vrefp,Vcm,Vrefn) together with the SAR ADC

to $VrefSAR$ is broken to evaluate its stability. Fig. 5 shows the simulation results: DC open-loop gain of 43 dB with unity gain bandwidth of 143 MHz while having phase margin of 63 degrees. Fig. 7 shows the noise simulation of the reference voltage buffer.

Layout of the resulting reference voltage buffers (vrefp, vcm, vrefn) were completed and post-layout simulation done together with the complete SAR ADC. Vrefp and Vrefn occupy approximately $82\mu m \cdot 27\mu m$ while the common-mode buffer (Vcm) occupies $30\mu m \cdot 51\mu m$. Fig. 8 shows the spectrum for an input frequency of 242.19 kHz showing an ENOB of 11.5 bits.

V. Conclusion

Reference voltage buffers is an important part of a SAR ADC architecture and motivation for realizing them on-chip is presented. FVF based reference voltage buffer targeted for a 12-bit 8 MS/s SAR ADC based on hybrid RC DAC is presented. The reference voltage buffer is capable of driving capacitive and resistive loads. Design details of such a reference voltage buffer is presented together with related calculations. Finally simulation results of the stand-alone buffer show that it is stable and is capable of driving the targetted SAR ADC. Finally, we present the post-layout simulation results of all the three reference voltage buffers together with the SAR ADC thus highlighting that proposed design achieves the targeted ADC performance.

References

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