SiT6731EB Evaluation Board
User Manual

Contents

1   Introduction

The SiT6731EB evaluation board (EVB) is designed for use with SiTime's Emerald OCXOs in the 10-pin 9x7 mm package. It enables the evaluation of key functionalities of these OCXOs.

EVB Features

- SMA output for direct or buffered connection to measurement equipment
- Probing points for accurate waveform measurement
- Provision for I^{2}C control interface (connector)

SiTime typically ships the EVB with the OCXO mounted. The OCXO device should only be evaluated in its original soldered down state for best signal integrity and frequency stability. For best results the device should not be de-soldered and then re-soldered either manually or via reflow process.

2   I/O Descriptions

Table 1. SiT6731EB I/O

Connector designator	I/O	Description
P1	Power Supply and Sense	Four -pin connector (P1) for DC power supply and power sensing. **VDD is connected to Pin 1, GND – to Pin2 of P1.** **VDD sense is connected to Pin 4, GND – to Pin3 of P1.**
P2	Pin 1 access	Two-pin connector (P2) provides access to the pin 1 of the OCXO in OE mode. In OE mode, pin 1 can be left floating as there is an internal pull-up resistor.
P3	Frequency control via I^{2}C	A three-pin header (P3) provides access to I^{2}C (SDA, SCL) bus for DCOCXO configuration.
J1	Output	Oscillator output can be accessed in several ways: - Direct output through SMA connector - Buffered output through SMA connector - Oscilloscope probe at probing points - Direct output through LVCMOS-to-sinewave filter and SMA connector Please refer to the Section 3.1 for the details.
P4, P5	Service connectors	P4, P5 is reserved for SiTime internal use only.

3   EVB Usage Descriptions

3.1   EVB Configurations

SiT6731EB comes designed to support OCXO and DCOCXO devices.

Oscillator output can be accessed in several ways listed in Table 1. Table 2 describes components configuration to support all output configurations.

Table 2. Components configuration to support all output configurations

Output configuration	C3	R11	C5	R13	R14	R20	C8	R16	C9	R17	R12
Direct	DNP	DNP	0.1 uF/ 0 Ω	DNP	DNP	0 Ω	DNP	0 Ω	DNP	0 Ω	DNP
Direct + LVCMOS-to-sinewave filter**	DNP	DNP	Contact SiTime	DNP	DNP	Contact SiTime					DNP
Buffered output: LVCMOS Clipped Sine	DNP	DNP	0 Ω 0.1 uF	DNP 20 kΩ	DNP 20 kΩ	DNP	DNP	DNP	DNP	DNP	0 Ω
Probe: LVCMOS Clipped Sine	15 pF 10 pF*	DNP 10 kΩ*	DNP	DNP	DNP	DNP	DNP	DNP	DNP	DNP	DNP

* The value of the load capacitor C3 and load resistor R11 can be adjusted to match the load conditions in the target application. This enables the user to measure waveform characteristics under similar conditions as close to those on the target board as possible.

** LVCMOS-to-sinewave filter components values will depend on the carrier frequency of the device. Contact SiTime to get recommended nominals for filter components.

The test points for active probe are placed closely to the oscillator output for better signal integrity (see Figure A2).

Figure A1 in Appendix A shows the complete electrical schematic of SiT6731EB. Components labeled "DNP" are not assembled.

Shipment Configuration

SiT6731EB is shipped configured for buffered output allowing connecting it to the instrument input using 50 Ω coax cable. Details on the board assembly for shipment configuration can be found on the schematic (see Figure A1 in Appendix A). C5, R13 and R14 values would depend on the signaling type selected for the particular device configuration.

3.2 Waveform Capturing Using Active Probe

SiTime OCXO is a high-speed logic output device. It is critical that the proper logic and high frequency measurement techniques are used along with the high-quality active probe in order to ensure best measurement results.

SiTime recommends the following minimum equipment for proper clock waveform measurement

1) 4 GHz or higher active probe with capacitance <1 pF, such as a Keysight 1134B;
2) Oscilloscope with 4 GHz bandwidth or higher such as a Keysight DSA90604A.

A passive voltage probe should not be used as it adds a high capacitive load to the part and the long ground lead clip is not suitable for high frequency measurement applications. The inductance of the long ground lead coupled with the input capacitance of the probe results in a resonant circuit. The consequence of this resonance results in the distortion of the clock signal. Typical manifestations of this distortion include ringing, overshoot, and undershoot of the clock signal.

Eliminating such distortion requires a probe with the lowest input capacitance and a low inductance ground lead. In addition, SiTime OCXOs are typically configured for fast rise and fall times (2.5 ns or less) with 15 pF load. It is therefore critical that the probe tip ground be as short as possible, lowest inductance, and the return path for the ground be located as close as possible to the trace carrying the RF logic signal.

For waveform measurement, it's recommended to remove capacitor C5. Please refer to Figure A2 for test point locations on the SiT6731EB. If used, the soldering probe head is recommended use R11 resistor pads or solder it over it if it is needed. (Figure 1).
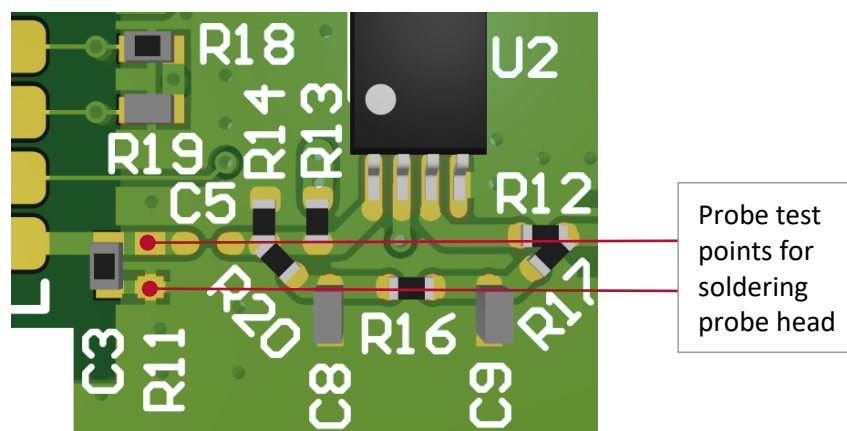

Figure 1: Recommended points for soldering probe head

More details on the SiTime recommendations on the oscillator's output probing can be found in AN10028.

3.3 Measuring Jitter and Phase Noise

For jitter and phase noise measurements, buffered output configuration is recommended. SiTime OCXO was not designed to drive 50 Ω load directly so buffer avoids excessive current draw from the device output. For minimal impact on the measurement LMK1C1104 low-additive jitter buffer is used on the board.

SMA connector is used to connect directly to the jitter measurement instrument, such as Time Interval Analyzer (TIA) or high-bandwidth real-time oscilloscope. Jitter measurement technique is described in SiTime AN10007.

The SMA can also be connected through 50 Ω coaxial cable to signal source analyzers or spectrum analyzers to measure phase noise. In such case the use of AC-coupling configuration is recommended because not all measurement instruments can accept DC voltage at their inputs.

3.4 Current Measurement

To measure the current consumption user, need to use ammeter/multi-meter in the power supply circuit. We recommend removing diode D1 to avoid measuring the additional current of the diode circuit. It is recommended to measure the voltage on DUT VDD and adjust for any drop on the DMM to ensure known VDD voltage on the device. VDD adjustment must be completed before every current measurement.

Appendix A
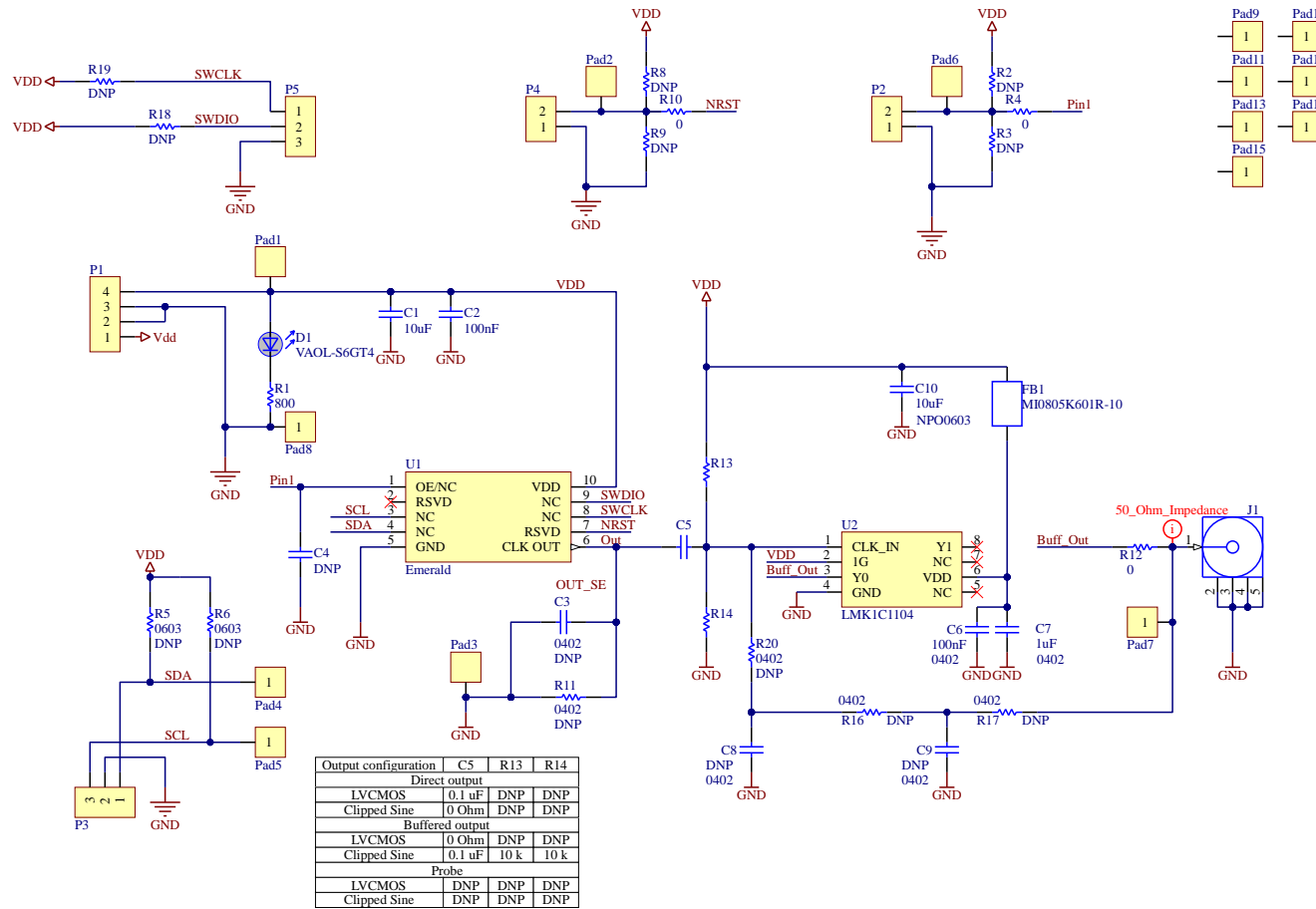
Figure A1. SiT6731EB EVB Electrical schematics

Output configuration	C5	R13	R14
Direct output			
LVCMOS	0.1 uF	DNP	DNP
Clipped Sine	0 Ohm	DNP	DNP
Buffered output			
LVCMOS	0 Ohm	DNP	DNP
Clipped Sine	0.1 uF	10 k	10 k
Probe			
LVCMOS	DNP	DNP	DNP
Clipped Sine	DNP	DNP	DNP

Table A1. Bill of Materials (BOM)

#	Reference Designators	Description	Qty	SMD component size	Value
1	C1, C10	Capacitor	2	0603	10uF
2	C2, C5, C6	Capacitor	3	0402	0.1uF
3	C3, C4, C8, C9	Capacitors	4	0402	DNP
4	C7	Capacitors	1	0402	1uF
5	D1	LED	1	0603	Green
6	J1	SMA connector	1	-	-
7	FB1	Ferrite Bead	1	0805	600 Ω @ 100 MHz
8	P1	4-pin header	1	-	-
9	P2, P4	2-pin header	2	-	-
10	P3, P5	3-pin connector	2	-	-
11	R1	Resistors	1	0603	800 Ω
12	R2, R3, R5, R6, R8, R9	Resistors	6	0603	DNP
13	R4, R10	Resistors	2	0603	0 Ω
14	R12	Resistor	1	0402	49.9 Ω
15	R13, R14	Resistor	2	0402	8.2 kΩ
16	R11, R16, R17, R18, R19, R20	Resistor	6	0402	DNP
17	U2	Buffer	1	TSSOP8-TI	LMK1C1104

Table A2. Connectors Digi-Key Part Number

Connectors	Digi-Key part number	Digi-Key part number for mating connector	Digi-Key part number for associated products
Power/ Power adjust	WM10159-ND	WM2002-ND	WM1114TR-ND
Pin 1 access	732-5335-ND	-	-
Pin 2 access	732-5335-ND	-	-
Frequency control via I²C	732-5336-ND	-	-
OUT	WM5534-ND	-	-
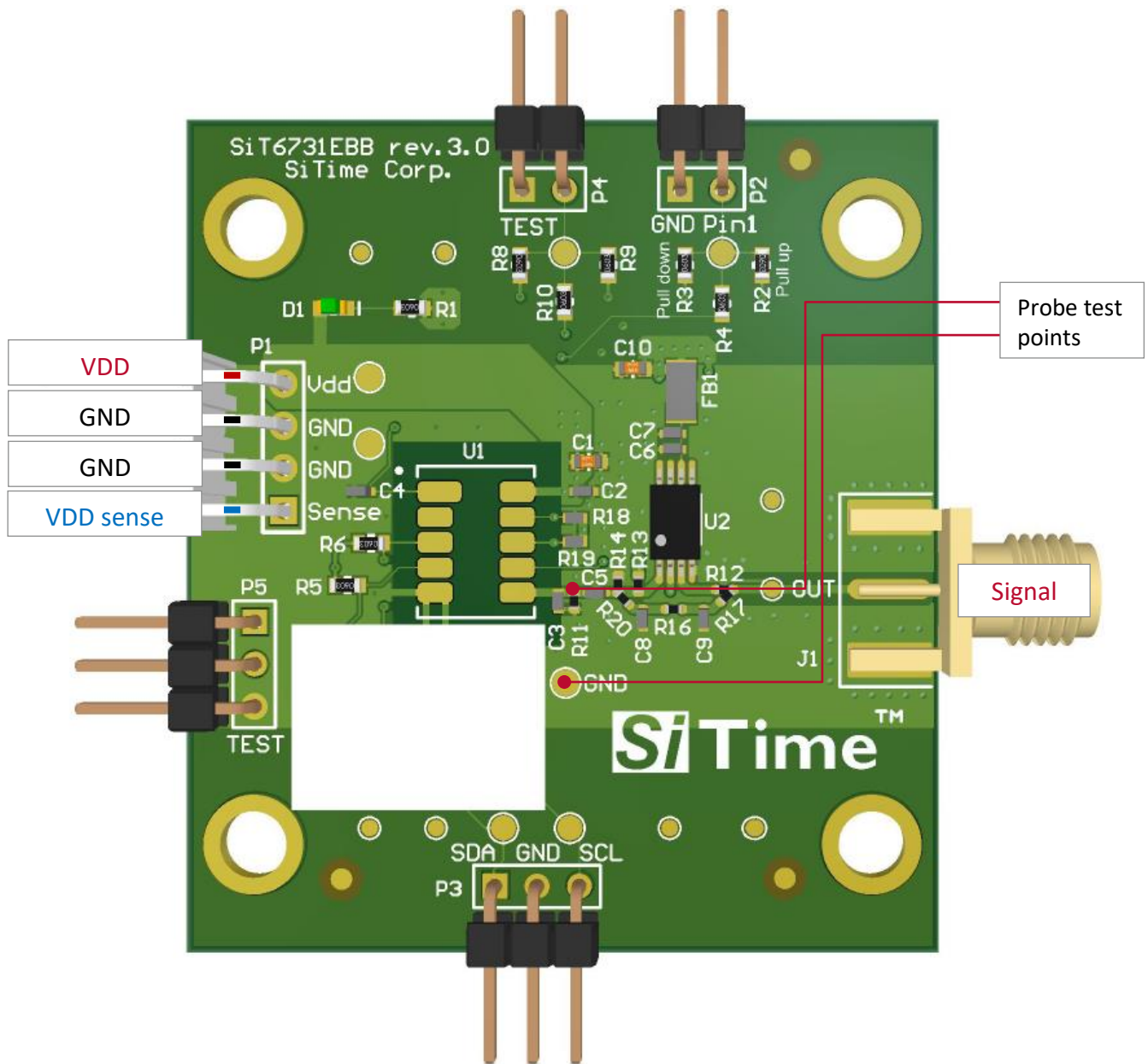
Figure A2. SiT6731EB EVB

Table 3: Revision History

Version	Release Date	Change Summary
1.0	12/13/2018	Original doc
2.0	05/31/2021	Changed according to next board revision
3.0	05/30/2022	Changed according to next board revision