6

A Switching Current-Source Oscillator

Ultra-low-power (ULP) transceivers underpin short-range communications for wireless Internet-of-Things (IoT) applications. However, their system lifetime is extremely limited by the transceiver power consumption and available battery technology. On the other hand, energy harvesting technologies typically deliver supply voltages that are much lower than the standard supply of CMOS circuits; e.g., on-chip solar cells can supply only 200–800 mV. Although boost converters can bring the level up to the required $\sim$1 V, their poor efficiency ($\leq$80%) wastes the harvested energy. Consequently, RF oscillators, as one of the transceiver's most power hungry circuitry, must be very power efficient and preferably operate directly at the energy harvester output. In this chapter, we analyze in depth design of an oscillator topology to address the aforementioned constraints without sacrificing manufacturability and phase purity.

6.1 Introduction

Ultra-low-power (ULP) radios underpin short-range communications for wireless Internet-of-Things (IoT). Since RF transmitters (TX) have consumed a significant portion, if not the majority, of the radio's power, the IoT system lifetime tends to be severely limited by the TX power consumption and available battery technology.

Figure 6.1 shows the system lifetime for various battery choices as a function of current consumption. State-of-the-art Bluetooth Low Energy (BLE) radios [1, 2] consume $\sim$7 mW and thus can *continuously* operate no more than 40 hours on an SR44 battery, which has a comparable dimension to the radio module. This directly causes inconvenient battery replacements at least every few months, which limits their attractiveness from the market

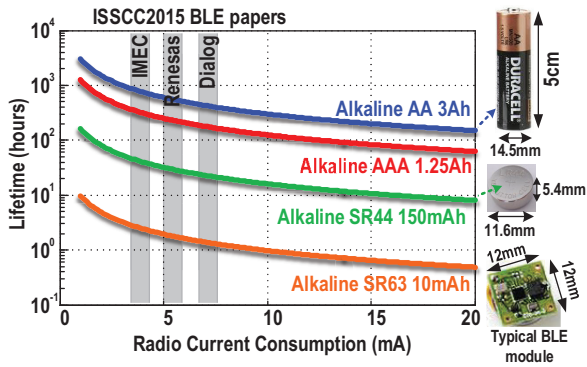

Figure 6.1 BLE system lifetime versus radio current consumption for various battery types.

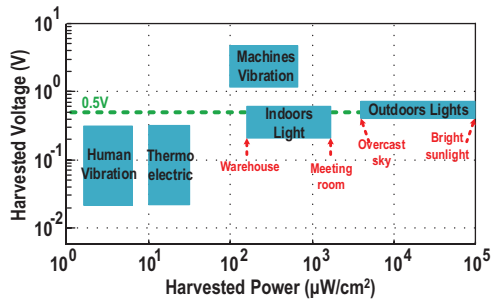

Figure 6.2 Delivered voltage and power density for various harvester types.

perspective. The lifetime can be easily increased by employing larger batteries, but that comes at a price of increased weight and dimensions and it is clearly against the miniaturization vision of IoT. This has motivated an intensive research leading to miniaturized transceivers with a high power efficiency [1–12].

Energy harvesting from a surrounding environment can enable and further spur the IoT applications by significantly extending their lifetime. The delivered voltage versus power density of different harvesting methodologies is depicted in Figure 6.2 [10, 13]. Solar cells offer the highest harvested power per area in both indoor and outdoor conditions. However, they provide lower voltages (0.25–0.75 V) than the expected deep-nanoscale CMOS supply of $\sim$1 V. Hence, boost converters are typically used to bring the supply level up to the required $\sim$1 V. As can be gathered from Table 6.1, the relatively poor efficiency ($\leq$80%) of boost converters wastes the harvested energy, thus worsening the system-level efficiency, in addition to increasing

Table 6.1 Performance summary of state-of-the-art boost converters

	[14] ISSCC'12	[15] ISSCC'14	[16] ISSCC'15
Technology	N/A	65 nm CMOS	0.18 μm CMOS
Input voltage range	0.1–2.9 V	0.15–0.5 V	0.45–3 V
Output voltage range	3 V	0.5–0.6 V	3.3 V
Efficiency @$V_{in} = 0.5$ V	$\leq 80\%$	$\leq 72.5\%$	$\leq 78.5\%$

the hardware complexity coupled with issues of switching ripples. Consequently, it would be highly desirable for the ULP transceivers to operate directly from the harvested voltage.

The rest of this chapter is dedicated to introduce and analyze a switching current-source oscillator [17, 18] which is optimized for 28-nm CMOS, can operate directly at the low voltage of harvesters, and reduces power and supply voltage without compromising the robustness of the oscillator start-up or loading its tank quality factor.

6.2 Oscillator Power Consumption Trade-offs

The oscillator phase noise (PN) requirements can be calculated by considering the toughest BLE blocking profile:

$$\mathcal{L}(\Delta\omega) = P_{signal} - P_{blocker} - SNR_{min} - 10log_{10}(BW). \tag{6.1}$$

The received packet error rate (PER) must be better than 30.8% while the wanted signal is just 3 dB above the reference sensitivity level of –70 dBm and in face of an in-band blocker of –40 dBm located at 3-MHz offset from the desired channel. Furthermore, the required signal-to-noise ratio (SNR) should be better than 15 dB to support such PER for a GFSK signal with a modulation index $m = 0.5$ [20]. By replacing the aforementioned values in (6.1), PN shall be better than –105 dBc/Hz at $\Delta\omega = 2\pi \cdot 3$ MHz. Hence, the PN requirements are quite trivial for IoT applications and can be easily met by LC oscillators as long as Barkhausen start-up criterion is satisfied over process, voltage, and temperature (PVT) variations.[1] Consequently, reducing oscillator power consumption, P_{DC}, is the ultimate goal in IoT applications.

[1] Ring oscillators can also satisfy such a relaxed phase noise requirement. However, they consume much higher power than LC oscillators at $f_0 \geq 1$ GHz [19].

The PN of any class of an RF oscillator (i.e., class-B) at an offset frequency $\Delta\omega$ from its resonating frequency ω_0 can be expressed as

$$\mathcal{L}(\Delta\omega) = 10\log_{10}\left(\frac{KT}{2\,Q_t^2\;\alpha_I\;\alpha_V\;P_{DC}}\cdot F\cdot\left(\frac{\omega_0}{\Delta\omega}\right)^2\right), \tag{6.2}$$

where K is the Boltzmann's constant; T is the absolute temperature; Q_t is the LC-tank quality factor; α_I is the current efficiency, defined as ratio of the fundamental current harmonic I_{ω_0} over the oscillator DC current I_{DC}; and α_V is the voltage efficiency, defined as a ratio of the single-ended oscillation amplitude, $V_{osc}/2$, over the supply voltage V_{DD} [21, 22]. Furthermore, F is the effective noise factor of the oscillator.

Equation (6.2) clearly demonstrates a trade-off between the oscillator's P_{DC} and PN. Furthermore, the oscillator's FoM normalizes the PN performance to the oscillation frequency and power consumption, yielding

$$FoM = 10\log_{10}\left(\frac{10^3 KT}{2\,Q_t^2\;\alpha_I\;\alpha_V}\cdot F\right). \tag{6.3}$$

The effective noise factor F is expressed by [23, 24]

$$F = \frac{R_{in}}{2KT}\cdot\sum_i\frac{1}{2\pi}\int_0^{2\pi}\overline{i_{n,i}^2(\phi)}\cdot\Gamma_i^2(\phi)\,d\phi, \tag{6.4}$$

where $\phi = \omega_0 t$, $\overline{i_{n,i}^2(\phi)}$ is the white current noise power density of the ith noise source and Γ_i is its relevant ISF function from the corresponding ith device noise [25]. Finally, R_{in} is an equivalent differential input parallel resistance of the tank's losses. The oscillator I_{DC} may be estimated by one of the following equations:

$$I_{DC} = \frac{I_{\omega_0}}{\alpha_I}\xrightarrow{I_{\omega_0}=\frac{V_{osc}}{R_{in}}} I_{DC} = \frac{V_{osc}}{R_{in}}\cdot\frac{1}{\alpha_I}\xrightarrow{V_{osc}=2\alpha_V V_{DD}} I_{DC} = \frac{2V_{DD}}{R_{in}}\cdot\frac{\alpha_V}{\alpha_I}. \tag{6.5}$$

As a result, the RF oscillator's P_{DC} is derived by

$$P_{DC} = \frac{V_{DD}^2}{R_{in}}\cdot\frac{\alpha_V}{\alpha_I}. \tag{6.6}$$

Equation (6.6) indicates that the minimum achievable P_{DC} can be expressed in terms of a set of *optimization* parameters, such as R_{in}, and

a set of *topology*-dependent parameters, such as minimum supply voltage ($V_{DD,min}$), current and voltage efficiencies.

Lower P_{DC} is typically achieved by scaling up $R_{in} = L_p\omega_0 Q_t$ simply via a large multi-turn inductor, as in [26]. For example, while maintaining a constant Q_t, doubling L_P would theoretically double R_{in}, which would reduce P_{DC} by half but at a cost of a 3-dB PN degradation. However, at some point, that trade-off stops due to a dramatic drop in the inductor's self-resonant frequency and Q-factor. Figure 6.3(a) shows the simulated Q-factor of several multi-turn inductors in 28-nm CMOS versus their inductance values. As the inductor enlarges, the magnetic and capacitive coupling to the low-resistivity substrate increases such that the tank Q-factor drops almost linearly with L_P. As can be gathered from Figure 6.3(b), this constraint sets an upper limit on maximum $R_{in} = L_p\omega_0 Q_t$, which is chiefly a function of the technology node. Note that the inductor's value is largely dependent on its physical dimensions, rather than on the technology. However, the tank Q-factor is a bit degraded in the most recent process nodes (i.e., 28 nm) mainly due to more stringent minimum metal density rules, closer separation between the top-metal and substrate, as well as thinner lower-level metals that are used in metal-oxide-metal (MoM) capacitors. As a consequence, it is expected that $R_{in(max)}$ slightly reduces by migrating to finer CMOS technologies.

Parasitic capacitance of inductor windings, gm-devices, switchable capacitors, and oscillator routings determines a minimum floor of the tank's capacitance, which appears to be ~250 fF at $f_0 = 4.8$ GHz. It puts another restriction on L_p and $R_{in(max)}$ to ~4.5 nH and ~1.3 $k\Omega$ and sets a lower limit on P_{DC} of each oscillator structure. Under this condition, the tank's Q-factor drops to $\leq$9. This explains the poor FoM of RF oscillators in modern BLE transceivers.

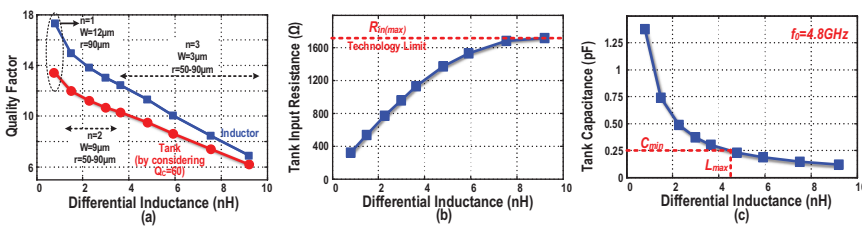

Figure 6.3 Dependency of various inductor parameters in 28-nm LP CMOS across inductance value: (a) inductor and tank Q-factor; (b) equivalent differential input resistance of the tank; and (c) required tank capacitance at 4.8-GHz resonance. Note that at this point the inductors are without dummy metal fills.

The topology-dependent parameters also play an important role in trying to reduce P_{DC}. Equation (6.6) favors structures that offer higher α_I or can sustain oscillation with smaller V_{DD} and α_V. On the other hand, $\alpha_V \cdot \alpha_I$ should be maximized to avoid any penalty on FoM [22, 27], as evident from (6.2). Consequently, to efficiently reduce P_{DC} without disproportionately worsening the FoM, it is desired to employ structures with a higher α_I and a lower minimum V_{DD}. To get a better insight, Figure 6.4 shows such effects for the traditional cross-coupled NMOS-only (OSC_N) and complementary push–pull (OSC_NP) structures [28, 29]. Due to the less stacking of transistors, the $V_{DD,min}$ of OSC_N can go 40% lower than that of OSC_NP. However, α_I of OSC_NP is doubled due to the switching of tank current direction every half period. Its oscillation swing, and thus α_V, is also 50% smaller. Hence, OSC_NP offers $\sim 3\times$ lower α_V/α_I. However, both structures demonstrate similar $\alpha_V \cdot \alpha_I$ product [30]. Consequently, each of them has its own set of advantages and drawbacks such that the minimum achievable P_{DC} and FoM is almost identical, as shown in Table 6.2. Note that applying a tail filtering technique to a class-B oscillator increases its α_V [22, 31], which is in line with the FoM optimization but against the P_{DC} reduction, as evident from (6.2) and (6.6). Furthermore, while maintaining the same R_{in}, a class-F_3 operation does not reduce P_{DC} of traditional oscillators since its minimum V_{DD}, α_V and α_I are identical to OSC_N (see Chapter 3).

A push–pull class-C oscillator appears as an excellent choice for ULP applications due to its largest α_I and smallest α_V [32], as per Table 6.2. However, it needs an additional complex biasing circuitry (e.g., an opamp)

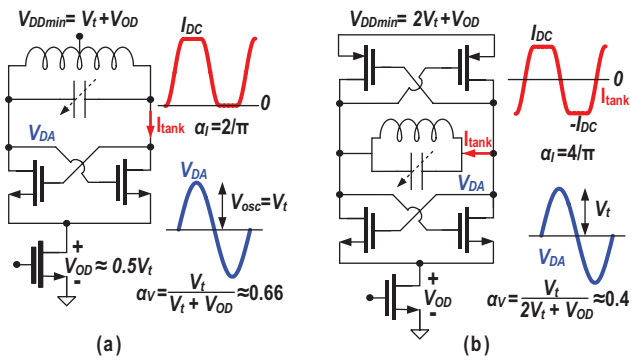

Figure 6.4 $V_{DD,min}$, α_I and α_V parameters for: (a) cross-coupled NMOS and (b) complementary push–pull oscillators.

Table 6.2 Minimum P_{DC} for different RF oscillator topologies

Topology	$V_{DD,min}$ †	α_V ‡	α_I *	P_{DCmin}	$\alpha_V.\alpha_I$
OSC_N	$V_t + V_{OD} \approx 1.5\ V_t$	0.66	2/π	4.66 V_t^2/R_{in}	0.42
OSC_{NP}	$2\ V_t + V_{OD} \approx 2.5\ V_t$	0.4	4/π	3.92 V_t^2/R_{in}	0.51
OSC_{NP} with tail filter	$2\ V_t + V_{OD} \approx 2.5\ V_t$	0.63	4/π	6.2 V_t^2/R_{in}	0.8
Class-C_{NP}	$2\ V_t + V_{OD} \approx 2.5\ V_t$	0.25	2	0.15 mW + 1.56 V_t^2/R_{in}	0.5
Class-D	$\approx\ V_t$	1.635	0.5	6.54 V_t^2/R_{in}	0.82
Class-F_3	$V_t + V_{OD} \approx 1.5\ V_t$	0.66	2/π	4.7 V_t^2/R_{in}	0.42
This work	$V_t + V_{OD} \approx 1.5\ V_t$	0.33	4/π	1.2 V_t^2/R_{in}	0.42

† by considering $V_{OD} = 0.5\ V_t$ for the current source.
‡ at the minimum V_{DD}.
* ideal value.

to guarantee the proper oscillator start-up and to keep the transistors in saturation during the on-state. There are also strong mutual trade-offs between the biasing circuit's P_{DC}, oscillator's amplitude stability and PN, much intensified in ULP applications where the tank capacitance tends to be smaller [33]. As a consequence, the biasing circuitry can end up consuming comparable power as the ULP oscillator itself. On the other hand, V_{DD} of class-D oscillators can go below a threshold voltage, V_t. However, due to hard switching of core transistors, its α_V and α_I are, respectively, higher and lower than other structures [34], as shown in Table 6.2. According to (6.6), this trend is against the P_{DC} reduction. Consequently, the current oscillator structures have issues with reaching simultaneous ultra-low power *and* voltage operation.

In this chapter, we disclose how to convert the fixed current source of the traditional NMOS topology into a structure with alternating current sources such that the tank current direction can change every half period. Consequently, the benefits of low supply of the OSC_N topology and higher α_I of OSC_{NP} structure are combined to reduce power consumption further than practically possible in the traditional oscillators.

6.3 Switching Current-Source Oscillator

Figure 6.5 shows an evolution towards the switching current-source oscillator. The OSC_N topology is chosen as a starting point due to its low V_{DD} capability. To reduce P_{DC} further, it is desired to switch the direction of the

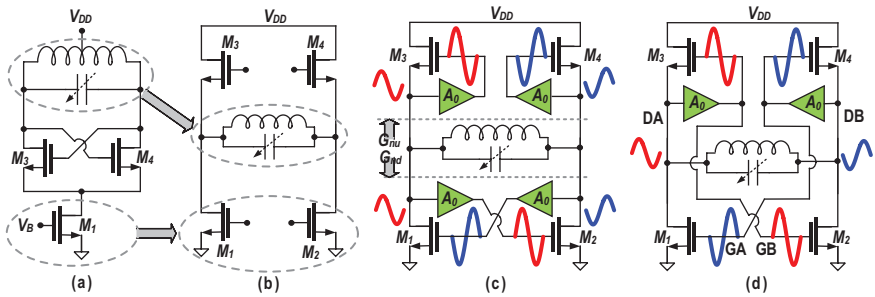

Figure 6.5 Evolution towards the switching current-source oscillator.

LC-tank current in each half period, which will double α_I. Consequently, we beneficially split the fixed current source M_1 in Figure 6.5(a) into two switchable current sources, M_1 and M_2, as suggested in Figure 6.5(b). This allows for the tank to be disconnected from the V_{DD} feed and be moved inbetween the upper and lower NMOS transistor pairs to give rise to an H-bridge configuration. In the next step, the passive voltage gain blocks, A_0, are added to the NMOS gates, as shown in Figure 6.5(c). Both upper and lower NMOS pairs should each independently demonstrate *synchronized* positive feedback to realize the switching of the tank current direction. The "master" positive feedback enforces the differential-mode operation and is realized by the lower-pair transistors configured in a conventional cross-coupled manner. Its negative conductance seen by the tank may be estimated by (see Section 6.4 for detailed calculations)

$$G_{down} = \frac{-A_0}{4} \cdot (g_{m1}(\phi) + g_{m2}(\phi)) \,. \tag{6.7}$$

On the other upper side, the differential-mode oscillation of the tank is reinforced by the $M_{3,4}$ devices which realize the second positive feedback.[2] The negative conductance seen by the tank into the upper pair can be calculated by (see Section 6.4 for detailed calculations)

$$G_{up} = G_{down} = \frac{-(A_0 - 1)}{4} \cdot (g_{m3}(\phi) + g_{m4}(\phi)) \,. \tag{6.8}$$

Equation (6.8) clearly indicates that the voltage gain block is necessary and A_0 must be safely larger than 1 to be able to present a negative conductance to the tank, thus enabling the H-bridge switching. By merging

[2]It should be noted that the "master/slave" view is mainly valid from a small-signal standpoint. Both are equally important when considering the large-signal switching operation.

the redundant voltage gain blocks, the disclosed switching current-source oscillator is shown in Figure 6.5(d). Note that the tank with an implicit voltage gain can be realized by using a capacitive divider, autotransformer, or step-up transformer, as illustrated in Figure 6.6. The transformer-based tank is chosen in this work due to its simplicity.

Figures 6.7 and 6.8 illustrate the novel oscillator schematic as well as waveforms and various operational regions of M_{1-4} transistors across the oscillation period. The two-port resonator consists of a step-up 1:2 transformer and tuning capacitors, C_1, C_2, at its primary and secondary windings.

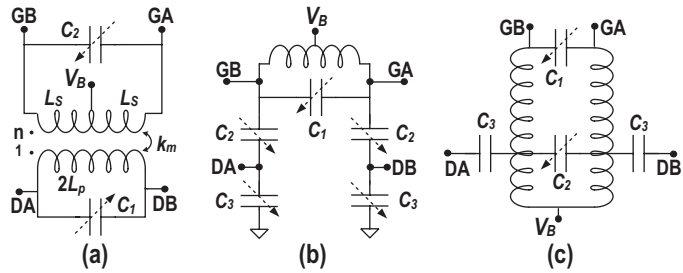

Figure 6.6 Various options of a tank providing voltage gain.

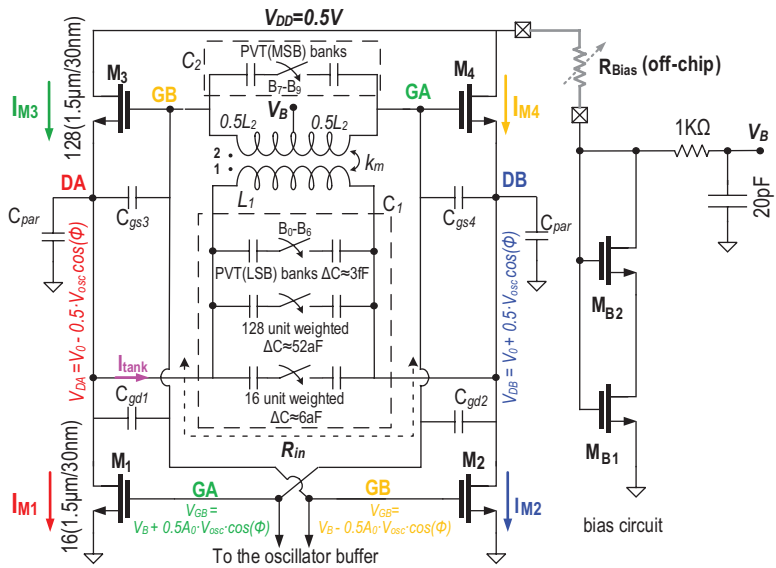

Figure 6.7 Schematic of the switching current-source oscillator.

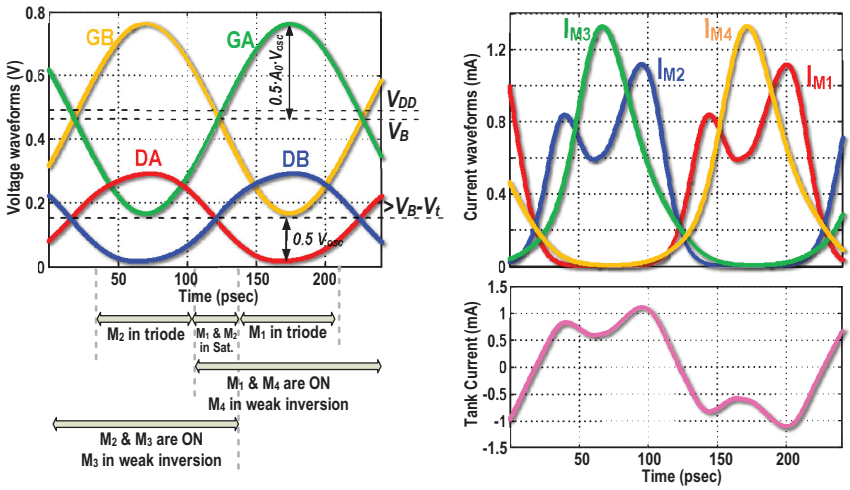

Figure 6.8 Waveforms and various operational regions of M_{1-4} transistors across the oscillation period.

The transistors $M_{1,2}$ set the oscillator's DC current, while the $M_{3,4}$ pair acts as a switching current source. Both $M_{1,2}$ and M_{3-4} pairs play an equally vital role of switching the tank current direction. As can be gathered from Figure 6.8, G_B oscillation voltage is high within the first half period. Hence, only M_2 and M_3 transistors are on and the current flows from left to right side of the tank. However, M_1 and M_4 are turned on for the second half period and the tank's current direction is reversed. Consequently, just like in the push–pull structure, the tank current flow is reversed every half period, thus doubling the oscillator's α_I to $4/\pi$.

The V_{DD} of the new oscillator can be as low as $V_{OD1} + V_{OD3} \approx V_t$, which is extremely small for an oscillator with a capability of switching the tank current direction. This makes it suitable for a direct connection to solar cells. Note that the oscillation swing cannot go further than $V_{OD1,2}$ at DA/DB nodes, which is chosen $\sim$150 mV to satisfy the system's phase noise requirement by a few dB margin. However, the maximum required voltage of the circuit is determined by the bias voltage V_B.

$$V_B \approx V_{OD1} + V_{gs3}. \tag{6.9}$$

Equation (6.9) implies that $M_{3,4}$ should work in weak inversion keeping $V_{gs3}<V_t$ to achieve lower $V_{DD,min}$. However, the transistor's cut-off frequency f_{max} drops dramatically in the subthreshold operation. Note that f_{max} should be at least $4\times$ higher than the operating frequency $f_0 = 4.8$ GHz

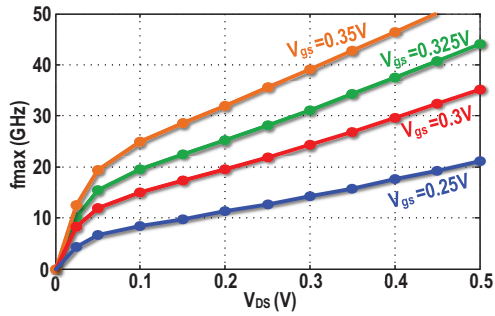

Figure 6.9 f_{max} of low-V_t 28 nm transistor versus V_{DS} for different V_{GS}.

to guarantee the oscillator start-up over PVT variations. This constraint limits $V_{gs3} \approx 0.32$ V for $V_{OD3} \approx 150$ mV, as can be gathered from Figure 6.9. Consequently, even by considering only the tougher V_B requirement, the new structure can operate at V_{DD} as low as 0.5 V, on par with OSC_N.

Such a low V_{DD} and oscillation swing can easily lead to start-up problems in the traditional structures. It will certainly increase power consumption, P_{buf}, of the following buffer, which would require more gain in order to provide a rail-to-rail swing at its output that is interpreted as a local oscillator (LO) clock. Fortunately, the transformer gain enhances the oscillation swing at $\text{M}_{1,2}$ gates to even beyond V_{DD}, guaranteeing the oscillator start-up and reduction of P_{buf}. Consequently, the oscillator buffer is connected to the secondary winding of the transformer in this design.

As can be gathered from Figure 6.8, the $\text{M}_{3,4}$ switching current-source transistors operate in a class-C manner as in a Colpitts oscillator, meaning that they deliver more or less narrow-and-tall current pulses. However, their non-zero conduction angle is quite wide, $\sim\pi$, due to the low overdrive voltage in the subthreshold operation. On the other hand, $\text{M}_{1,2}$ operate in a class-B manner like cross-coupled oscillators, meaning that they deliver square-shaped current pulses. Hence, the shapes of drain currents are quite different for the lower and upper pairs. However, their fundamental components demonstrate the same amplitude ($\alpha_I \approx 2/\pi$) and phase to realize the constructive oscillation voltage across the tank. The higher drain harmonics obviously show different characteristics. However, they are filtered out by the tank's selectivity characteristic. Note that the current through a transistor of the upper pair will have two paths to ground: through the corresponding transistor of the lower pair and through the single-ended capacitors. Consequently, the single-ended capacitors sink the higher current harmonics of $\text{M}_{3,4}$ transistors.

6.4 Thermal Noise Upconversion

To calculate a closed-form PN equation, the oscillator model is simplified in Figure 6.10. At the resonant frequency, the transformer-based tank can be modeled by an equivalent LC tank of elements L_{eq}, C_{eq}, and R_{in}.[3] On the other hand, M_{1-4} transistors with passive voltage gain of the transformer are decomposed into two nonlinear time-variant conductances. Note that the active elements in the circuit may add to the resonator loss, particularly at the extremes of large oscillation waveforms which may push transistors into their triode regions. Consequently, the nonlinearity is decomposed into two nonlinear resistances: one that is always positive, $G_{ds}(\phi)$, and one that is always negative, $G_n(\phi)$, where $\phi = \omega_0 t$. Further, to get a better insight, the effects of noise on the oscillator phase noise due to channel conductance ($\overline{i^2_{n,Gds}(\phi)} = 4KTG_{ds}(\phi)$) and transconductance gain ($\overline{i^2_{n,Gm}(\phi)}$) of M_{1-4} transistors are separately modeled in Figure 6.10. All circuit variables in this generic model will be obtained in the following sections.

6.4.1 Calculating the Effective Noise Due to Transconductance Gain of M_{1-4} Transistors ($\overline{i^2_{n,Gm}(\phi)}$)

It is clear that the lower pair is a voltage-biased circuit. Consequently, the noise sources of M_1 and M_2 are uncorrelated for the entire oscillation period. However, the situation is more complicated for the upper pair. For a short time around zero-crossings, both transistors of the upper pair work in the subthreshold region, while elsewhere one of them is off and the other device will be driven into saturation. In this situation, current through the upper NMOS transistor will have no path to ground other than through the corresponding

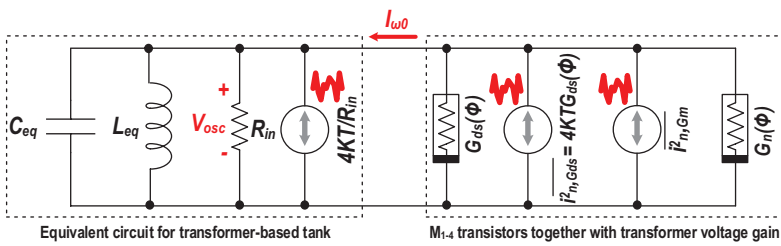

Figure 6.10 Generic noise circuit model of the disclosed oscillator.

[3]The interested reader is directed to [35] for accurate closed-form equations of L_{eq}, C_{eq}, and R_{in}.

NMOS transistor of the lower pair if there were no single-ended capacitance at the tank. This phenomenon creates a common-mode oscillation across the tank, which ensures that the drain currents of both lower and upper NMOS transistor are the same.

However, if the tank includes some single-ended capacitors connected to ground, the oscillator will behave very differently (we also use this single-ended capacitors to create a common-mode resonant frequency at the second harmonic of the fundamental frequency to reduce 1/f noise upconversion). Note that one cannot avoid the presence of single-ended capacitors in the tank due to drain–bulk and drain–source parasitic capacitance of lower-pair transistors, source–bulk and drain–source parasitic capacitance of upper pair transistors, and parasitic capacitance of the transformer's primary winding. In this situation, the current through transistors of upper pair will have two paths to the ground: through the corresponding NMOS transistor of the lower pair and through the single-ended capacitors. Consequently, single-ended capacitors suppress the common-mode oscillation voltage across the tank. In this instance, the upper pair is more appropriately viewed as a voltage-biased circuit. Consequently, noise sources due to transconductance gain of M_{1-4} transistors are absolutely uncorrelated.

By using the same approach as [36], we are going to replace all noise sources with an equivalent noise source across the tank. By writing KCL at DA and DB nodes, it is straightforward to show that the instantaneous equivalent current can be calculated by (see Figure 6.11)

$$\left.\begin{aligned} I_{eq} &= I_{M1} - I_{M3} \\ I_{eq} &= I_{M4} - I_{M2}, \end{aligned}\right\} \rightarrow I_{eq} = \frac{1}{2}((I_{M1} + I_{M4}) - (I_{M1} + I_{M4})) \rightarrow$$
$$I_{eq} = (I_{M1} - I_{M2}) + (I_{M3} - I_{M4}). \qquad (6.10)$$

As a consequence, the resulting differential noise current through the tank is

$$\overline{i^2_{n,Gm}(\phi)} = \frac{1}{4}\left(\overline{i^2_{n,gm1}(\phi)} + \overline{i^2_{n,gm2}(\phi)} + \overline{i^2_{n,gm3}(\phi)} + \overline{i^2_{n,gm4}(\phi)}\right) \rightarrow$$
$$\overline{i^2_{n,Gm}(\phi)} = KT\left(\gamma_1(g_{m1}(\phi) + g_{m2}(\phi)) + \gamma_3(g_{m3}(\phi) + g_{m4}(\phi))\right). \quad (6.11)$$

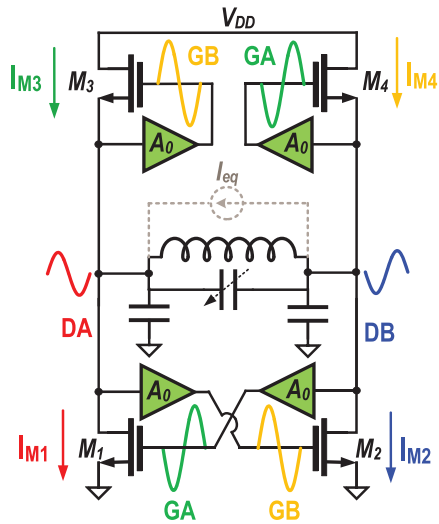

Figure 6.11 Simplified schematic of the switching current-source oscillator.

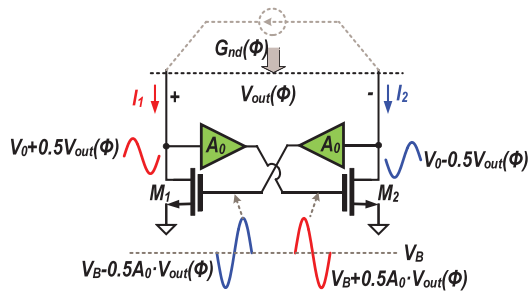

Figure 6.12 Simplified schematic of the lower pair of the oscillator.

6.4.2 Calculating the Negative Conductance of the Oscillator ($G_n(\phi)$)

The negative conductance of lower and upper pairs will be calculated separately in the following sections. The upper and lower negative conductances are in parallel. Hence, the total negative conductance is calculated by adding the negative conductance of lower and upper pairs.

The gate–source voltage of M_1 is calculated by (see Figure 6.12)

$$V_{GS1}(\phi) = V_B - \frac{A_0 V_{out}(\phi)}{2}. \tag{6.12}$$

As a result, the derivative of gate–source voltage of M_1 is calculated by

$$\frac{dV_{GS1}(\phi)}{d\phi} = -\frac{A_0}{2} \cdot \frac{dV_{out}(\phi)}{d\phi}. \tag{6.13}$$

The transconductance gain of M_1 transistor may be estimated by

$$g_{m1}(\phi) = \frac{dI_1(\phi)}{dV_{GS1}} = \frac{dI_1(\phi)/d\phi}{dV_{GS1}/d\phi} = \frac{dI_1(\phi)/d\phi}{\frac{-A_0}{2} dV_{out}/d\phi} = -\frac{2}{A_0} \cdot \frac{dI_1(\phi)}{dV_{out}(\phi)}. \tag{6.14}$$

We can rewrite Equation (6.14) as

$$\frac{dI_1(\phi)}{dV_{out}(\phi)} = -\frac{2}{A_0} \cdot g_{m1}(\phi). \tag{6.15}$$

On the other hand, the gate–source voltage of M_2 is calculated by

$$g_{m2}(\phi) = \frac{dI_2(\phi)}{dV_{GS2}} = \frac{dI_2(\phi)/d\phi}{dV_{GS2}/d\phi} = \frac{dI_2(\phi)/d\phi}{\frac{A_0}{2} dV_{out}/d\phi} = \frac{2}{A_0} \cdot \frac{dI_2(\phi)}{dV_{out}(\phi)}. \tag{6.16}$$

And again, we can rewrite Equation (6.16) as

$$\frac{dI_2(\phi)}{dV_{out}(\phi)} = \frac{2}{A_0} \cdot g_{m2}(\phi). \tag{6.17}$$

The effective negative conductance of lower pair,

$$G_{nd}(\phi) = \frac{dI_{eq2}(\phi)}{dV_{out}(\phi)} = \frac{1}{2} \cdot \frac{dI_1(\phi) - dI_2(\phi)}{dV_{out}(\phi)}. \tag{6.18}$$

By using (6.15) and (6.17), the above equation can be rewritten by

$$G_{nd}(\phi) = -\frac{1}{4} \cdot A_0 \cdot (g_{m1}(\phi) + g_{m2}(\phi)). \tag{6.19}$$

The same calculations can be done for M_3 and M_4.

The gate–source voltage of M_3 is calculated by (see Figure 6.13)

$$V_{GS3}(\phi) = V_B - V_0 + 0.5(A_0 - 1)V_{out}(\phi). \tag{6.20}$$

As a result, the derivative of gate–source voltage of M_3 is calculated by

$$\frac{dV_{GS3}(\phi)}{d\phi} = 0.5(A_0 - 1) \cdot \frac{dV_{out}(\phi)}{d\phi}. \tag{6.21}$$

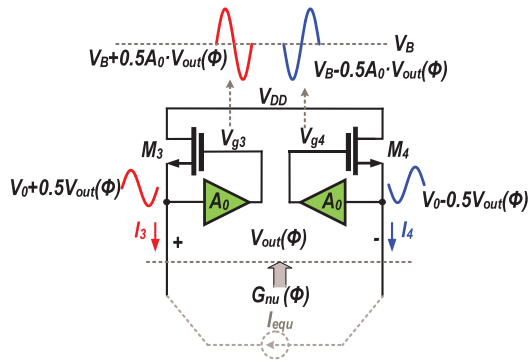

Figure 6.13 Simplified schematic of the upper pair of the oscillator.

The transconductance gain of M_3 transistor may be estimated by

$$g_{m3}(\phi) = \frac{dI_3(\phi)}{dV_{GS3}} = \frac{dI_3(\phi)/d\phi}{dV_{GS3}/d\phi} = \frac{dI_3(\phi)/d\phi}{0.5(A_0-1)\frac{dV_{out}}{d\phi}}$$
$$= \frac{2}{(A_0-1)} \cdot \frac{dI_3(\phi)}{dV_{out}(\phi)}. \tag{6.22}$$

We can rewrite the above equation by

$$\frac{dI_3(\phi)}{dV_{out}(\phi)} = \frac{A_0-1}{2} \cdot g_{m3}(\phi). \tag{6.23}$$

On the other hand, the gate–source voltage of M_4 is calculated by

$$V_{GS4}(\phi) = V_B - V_0 - \frac{(A_0-1)}{2} V_{out}(\phi). \tag{6.24}$$

As a result, the derivative of gate–source voltage of M_4 is calculated by

$$\frac{dV_{GS4}(\phi)}{d\phi} = \frac{(A_0-1)}{2} \cdot \frac{dV_{out}(\phi)}{d\phi}. \tag{6.25}$$

The transconductance gain of M_4 transistor then is estimated by

$$g_{m4}(\phi) = \frac{dI_4(\phi)}{dV_{GS4}} = \frac{dI_4(\phi)/d\phi}{dV_{GS4}/d\phi} = -\frac{dI_4(\phi)/d\phi}{0.5(A_0-1)\frac{dV_{out}}{d\phi}}$$
$$= -\frac{2}{(A_0-1)} \cdot \frac{dI_4(\phi)}{dV_{out}(\phi)}. \tag{6.26}$$

We can rewrite the above equation by

$$\frac{dI_4(\phi)}{dV_{out}(\phi)} = -\frac{A_0 - 1}{2} \cdot g_{m4}(\phi). \tag{6.27}$$

The negative conductance of upper pair

$$G_{nu}(\phi) = \frac{dI_{equ}(\phi)}{dV_{out}(\phi)} = \frac{1}{2} \cdot \frac{dI_4(\phi) - dI_3(\phi)}{dV_{out}(\phi)}. \tag{6.28}$$

By using (6.23) and (6.27), the above equation can be rewritten by

$$G_{nu}(\phi) = -\frac{1}{4} \cdot (A_0 - 1) \cdot (g_{m3}(\phi) + g_{m4}(\phi)). \tag{6.29}$$

The upper and lower negative conductance are in parallel. Hence, the total negative conductance is calculated by

$$\begin{aligned} G_n(\phi) &= G_{nd}(\phi) + G_{nu}(\phi) \\ &= \frac{1}{4} \cdot \left[A_0 \cdot (g_{m1}(\phi) + g_{m2}(\phi)) + (A_0 - 1) \cdot (g_{m3}(\phi) + g_{m4}(\phi))\right]. \end{aligned} \tag{6.30}$$

6.4.3 Calculating the Positive Conductance of the Oscillator ($G_{DS}(\phi)$)

The positive conductance of lower and upper pairs will be calculated separately in the following sections. The upper and lower positive conductance are in parallel. Hence, the total positive conductance is calculated by adding the positive conductance of lower and upper pairs.

The drain–source voltage of M_1 is calculated by (see Figure 6.12)

$$V_{ds1}(\phi) = V_0 + \frac{V_{out}(\phi)}{2}. \tag{6.31}$$

As a result, the derivative of drain–source voltage of M_1 is calculated by

$$\frac{dV_{ds1}(\phi)}{d\phi} = \frac{1}{2} \cdot \frac{dV_{out}(\phi)}{d\phi}. \tag{6.32}$$

The drain–source conductance of M_1 transistor may be estimated by

$$g_{ds1}(\phi) = \frac{dI_1(\phi)}{dV_{ds1}} = \frac{dI_1(\phi)/d\phi}{dV_{ds1}/d\phi} = -\frac{dI_1(\phi)/d\phi}{0.5\frac{dV_{out}}{d\phi}} = 2 \cdot \frac{dI_1(\phi)}{dV_{out}(\phi)}. \tag{6.33}$$

We can rewrite the above equation by

$$\frac{dI_1(\phi)}{dV_{out}(\phi)} = \frac{1}{2} \cdot g_{ds1}(\phi). \tag{6.34}$$

On the other hand, the drain–source voltage of M_2 is calculated by

$$V_{ds2}(\phi) = V_0 - \frac{V_{out}(\phi)}{2}. \tag{6.35}$$

As a result, the derivative of drain–source voltage of M_2 is calculated by

$$\frac{dV_{ds2}(\phi)}{d\phi} = -\frac{1}{2} \cdot \frac{dV_{out}(\phi)}{d\phi}. \tag{6.36}$$

The drain–source conductance gain of M_2 transistor may be estimated by

$$g_{ds2}(\phi) = \frac{dI_2(\phi)}{dV_{ds2}} = \frac{dI_2(\phi)/d\phi}{dV_{ds2}/d\phi} = -\frac{dI_2(\phi)/d\phi}{-0.5\frac{dV_{out}}{d\phi}} = -2 \cdot \frac{dI_2(\phi)}{dV_{out}(\phi)}. \tag{6.37}$$

We can rewrite the above equation as

$$\frac{dI_2(\phi)}{dV_{out}(\phi)} = -\frac{1}{2} \cdot g_{ds2}(\phi). \tag{6.38}$$

The positive conductance of lower pair then will be

$$G_{ds-down}(\phi) = \frac{1}{2} \cdot \frac{dI_1(\phi) - dI_2(\phi)}{dV_{out}(\phi)}. \tag{6.39}$$

Using (6.34) and (6.38), we can conclude:

$$G_{ds-down}(\phi) = \frac{1}{4} \left(g_{ds1}(\phi) + g_{ds2}(\phi) \right). \tag{6.40}$$

The drain–source voltage of M_3 is calculated by (see Figure 6.13)

$$V_{ds3}(\phi) = V_{DD} - V_0 - \frac{V_{out}(\phi)}{2}. \tag{6.41}$$

As a result,

$$\frac{dV_{ds3}(\phi)}{d\phi} = -\frac{1}{2} \cdot \frac{dV_{out}(\phi)}{d\phi}. \tag{6.42}$$

The drain–source conductance gain of M_3 transistor then is estimated by

$$g_{ds3}(\phi) = \frac{dI_3(\phi)}{dV_{ds3}} = \frac{dI_3(\phi)/d\phi}{dV_{ds3}/d\phi} = \frac{dI_3(\phi)/d\phi}{-0.5\frac{dV_{out}}{d\phi}} = -2 \cdot \frac{dI_3(\phi)}{dV_{out}(\phi)}. \quad (6.43)$$

We can rewrite the above equation as

$$\frac{dI_3(\phi)}{dV_{out}(\phi)} = -\frac{1}{2} \cdot g_{ds3}(\phi). \quad (6.44)$$

On the other hand, the drain–source voltage of M_4 is calculated by

$$V_{ds4}(\phi) = V_{DD} - V_0 + \frac{V_{out}(\phi)}{2}. \quad (6.45)$$

As a result,

$$\frac{dV_{ds4}(\phi)}{d\phi} = +\frac{1}{2} \cdot \frac{dV_{out}(\phi)}{d\phi} \quad (6.46)$$

and

$$g_{ds4}(\phi) = \frac{dI_4(\phi)}{dV_{ds4}} = \frac{dI_4(\phi)/d\phi}{dV_{ds43}/d\phi} = \frac{dI_4(\phi)/d\phi}{0.5\frac{dV_{out}}{d\phi}} = 2 \cdot \frac{dI_4(\phi)}{dV_{out}(\phi)}. \quad (6.47)$$

We can rewrite the above equation as

$$\frac{dI_4(\phi)}{dV_{out}(\phi)} = \frac{1}{2} \cdot g_{ds4}(\phi). \quad (6.48)$$

The positive conductance of upper pair then will be

$$G_{ds-up}(\phi) = \frac{1}{2} \cdot \frac{dI_4(\phi) - dI_3(\phi)}{dV_{out}(\phi)}. \quad (6.49)$$

Using (6.44) and (6.48), we can conclude

$$G_{ds-up}(\phi) = \frac{1}{4} \left(g_{ds3}(\phi) + g_{ds4}(\phi) \right). \quad (6.50)$$

The upper and lower positive conductance are in parallel. Hence, the total negative conductance is calculated by

$$G_{ds}(\phi) = G_{ds-up}(\phi) + G_{ds-down} = \frac{1}{4} \left[g_{ds1} + g_{ds2} + g_{ds3}(\phi) + g_{ds4}(\phi) \right]. \quad (6.51)$$

6.4.4 Satisfying Barkhausen Criterion

To sustain oscillation, the average power dissipated in the tank (R_{in}) and positive conductance of active devices ($G_{ds}(\phi)$) must equal the average power delivered by the negative conductance of nonlinearity ($G_n(\phi)$) [36]. Hence,

$$P_{R_{in}} + P_{G_{ds}} = -P_{G_n}. \tag{6.52}$$

Assuming $V_{out} = A_c cos(\omega_0 t)$, the average power dissipated in the tank can be calculated by

$$P_{R_{in}} = \frac{1}{T}\int_{-\frac{T}{2}}^{\frac{T}{2}} \frac{\left(A_c cos(\omega_0 t)\right)^2}{R_p} dt = \frac{A_c^2}{2R_p}. \tag{6.53}$$

The current drawn by the positive conductance of nonlinearity can be described as

$$\begin{aligned} I_{G_{ds}}(t) &= I_{G_{ds-DC}} + \int_{-\infty}^{t} d(I_{G_{ds}}(\tau))d\tau \\ &= I_{G_{ds-DC}} + \int_{-\infty}^{t} G_{ds}(\tau)d(V_{out}(\tau))d\tau \\ &= I_{G_{ds-DC}} - A_c\omega_0 \int_{-\infty}^{t} G_{ds}(\tau)\cdot sin(\omega_0\tau))d\tau \end{aligned} \tag{6.54}$$

and the average power dissipated by the positive conductance of the nonlinearity is

$$\begin{aligned} P_{G_{ds}}(t) &= \frac{1}{T}\int_{-T/2}^{T/2} V_{out}(t)\cdot I_{G_{DS}}(t)dt \\ &= \frac{1}{T}\int_{-T/2}^{T/2} A_c cos(\omega_0 t)\cdot \Bigg[I_{G_{DS-DC}} - A_c\omega_0 \\ &\quad \int_{-\infty}^{t} G_{ds}(\tau)\cdot sin(\omega_0\tau)\cdot d\tau\Bigg]\cdot dt \\ &= \frac{1}{T}\int_{-T/2}^{T/2} A_c cos(\omega_0 t)\cdot I_{G_{DS-DC}}\cdot dt \\ &= -\frac{A_c^2\omega_0}{T}\int_{-T/2}^{T/2} cos(\omega_0 t)\left[\int_{-\infty}^{t} G_{ds}(\tau)\cdot sin(\omega_0\tau)d\tau\right]\cdot dt. \end{aligned} \tag{6.55}$$

If we switch the order of the integrals, we may write

$$\begin{aligned} P_{G_{ds}}(t) &= -\frac{A_c^2\omega_0}{T}\int_{-\frac{T}{2}}^{\frac{T}{2}}\int_{\tau}^{\frac{T}{2}} G_{ds}(\tau)\cdot sin(\omega_0\tau)\cdot cos(\omega_0 t)\cdot dt\cdot d\tau \\ &= -\frac{A_c^2}{T}\int_{-\frac{T}{2}}^{\frac{T}{2}} G_{ds}(\tau)\cdot sin(\omega_0\tau)\cdot d\tau\cdot sin(\omega_0 t)|_{\tau}^{\frac{T}{2}} \\ &= +\frac{A_c^2}{T}\int_{-\frac{T}{2}}^{\frac{T}{2}} G_{ds}(\tau)\cdot (sin(\omega_0\tau))^2\cdot d\tau \\ &= +\frac{A_c^2}{T}\int_{-\frac{T}{2}}^{\frac{T}{2}} G_{ds}(\tau)\cdot (1-cos(2\omega_0\tau))\cdot d\tau. \end{aligned} \tag{6.56}$$

We know

$$G_{ds}[0] = \frac{1}{T}\int_{-T/2}^{T/2} G_{DS}(\tau)\cdot d\tau = \frac{1}{2\pi}\int_{-\pi}^{\pi} G_{DS}(\phi)\cdot d\phi \tag{6.57}$$

and

$$\begin{aligned} G_{ds}[2] &= \frac{1}{T}\int_{-T/2}^{T/2} G_{DS}(\tau)\cdot cos(2\omega_0\tau)\cdot d\tau \\ &= \frac{1}{2\pi}\int_{-\pi}^{\pi} G_{DS}(\phi)\cdot cos(2\phi)\cdot d\phi, \end{aligned} \tag{6.58}$$

where $G_{ds}[k]$ describes the Fourier series coefficients of the instantaneous positive conductance of nonlinearity $G_{ds}(t)$. By replacing (6.57) and (6.58) in (6.56)

$$P_{G_{ds}} = \frac{A_c^2}{2}\cdot (G_{DS}[0] - G_{DS}[2]). \tag{6.59}$$

We also define,

$$G_{DSEF} = G_{DS}[0] - G_{DS}[2]. \tag{6.60}$$

By replacing (6.60) in (6.59),

$$P_{G_{ds}} = \frac{A_c^2}{2}\cdot (G_{DSEF}). \tag{6.61}$$

Now let us calculate the average power delivered $G_n(\phi)$. The current drawn by the $G_n(\phi)$ can be described as

$$\begin{aligned} I_{G_n}(t) &= I_{G_{n-DC}} + \int_{-\infty}^{t} d(I_{G_n}(\tau))d\tau \\ &= I_{G_{n-DC}} + \int_{-\infty}^{t} G_n(\tau)d(V_{out}(\tau))d\tau \\ &= I_{G_{n-DC}} - A_c\omega_0 \int_{-\infty}^{t} G_n(\tau)\cdot sin(\omega_0\tau))d\tau. \end{aligned} \tag{6.62}$$

and the average power dissipated by the positive conductance of the nonlinearity is

$$\begin{aligned} P_{G_n}(t) &= \frac{1}{T}\int_{-T/2}^{T/2} V_{out}(t)\cdot I_{G_n}(t)dt \\ &= \frac{1}{T}\int_{-T/2}^{T/2} A_c cos(\omega_0 t)\cdot \Bigg[I_{G_{DS-DC}} \\ &\quad -A_c\omega_0 \int_{-\infty}^{t} G_n(\tau)\cdot sin(\omega_0\tau)\cdot d\tau\Bigg]\cdot dt \\ &= \frac{1}{T}\int_{-T/2}^{T/2} A_c cos(\omega_0 t)\cdot I_{G_{n-DC}}\cdot -\frac{A_c^2\omega_0}{T}\int_{-T/2}^{T/2} cos(\omega_0 t) \\ &\quad \Bigg[\int_{-\infty}^{t} G_n(\tau)\cdot sin(\omega_0\tau)d\tau\Bigg]\cdot dt. \end{aligned} \tag{6.63}$$

If we switch the order of the integrals, we may write

$$\begin{aligned} P_{G_n}(t) &= -\frac{A_c^2\omega_0}{T}\int_{-\frac{T}{2}}^{\frac{T}{2}}\int_{\tau}^{\frac{T}{2}} G_n(\tau)\cdot sin(\omega_0\tau)\cdot cos(\omega_0 t)\cdot dt\cdot d\tau \\ &= -\frac{A_c^2}{T}\int_{-\frac{T}{2}}^{\frac{T}{2}} G_n(\tau)\cdot sin(\omega_0\tau)\cdot d\tau\cdot sin(\omega_0 t)|_{\tau}^{\frac{T}{2}} \\ &= +\frac{A_c^2}{T}\int_{-\frac{T}{2}}^{\frac{T}{2}} G_n(\tau)\cdot (sin(\omega_0\tau))^2\cdot d\tau \\ &= +\frac{A_c^2}{T}\int_{-\frac{T}{2}}^{\frac{T}{2}} G_n(\tau)\cdot (1-cos(2\omega_0\tau))\cdot d\tau. \end{aligned} \tag{6.64}$$

Consequently,

$$P_{G_n} = \frac{A_c^2}{2}\cdot (G_{NSEF}). \tag{6.65}$$

To sustain oscillation, the average power dissipated in the tank (R_{in}) and positive conductance of active devices (G_{ds}) must equal the average power delivered by the negative conductance of nonlinearity (G_n). By replacing (6.53), (6.61) and (6.65) in (6.52),

$$\frac{A_c^2}{2R_{in}} + \frac{A_c^2}{2} \cdot (G_{DSEF}) = -\frac{A_c^2}{2} \cdot (G_{NEF}). \tag{6.66}$$

Consequently,

$$G_{NEF} = -\frac{1 + R_{in} \cdot G_{DSEF}}{R_{in}}. \tag{6.67}$$

On the other hand, the total effective negative conductance can be rewritten as sum of the effective negative conductance of lower and upper pairs

$$G_{NDEF} + G_{NUEF} = -\frac{1 + R_{in} \cdot G_{DSEF}}{R_{in}}. \tag{6.68}$$

Note that both upper and lower NMOS pairs should each individually demonstrate synchronized positive feedback to realize the switching of the tank current direction. Consequently, as with traditional complimentary oscillator, each pair should roughly compensate half of the oscillator losses.

$$G_{NDEF} = G_{NUEF} = -\frac{1}{2} \cdot \frac{1 + R_{in} \cdot G_{DSEF}}{R_{in}}. \tag{6.69}$$

On the other hand, G_{NDEF} and G_{NUEF} can be, respectively, calculated by

$$G_{NDEF} = -\frac{1}{4} \cdot A_0 \cdot [G_{M1EF} + G_{M2EF}] \tag{6.70}$$

and

$$G_{NUEF} = -\frac{1}{4} \cdot (A_0 - 1) \cdot [G_{M3EF} + G_{M4EF}]. \tag{6.71}$$

By merging (6.70), (6.71) and (6.69), we have

$$G_{M1EF} + G_{M2EF} = \frac{2}{(A_0)} \cdot \frac{1 + R_{in} \cdot G_{DSEF}}{R_{in}} \tag{6.72}$$

$$G_{M3EF} + G_{M4EF} = \frac{2}{(A_0 - 1)} \cdot \frac{1 + R_{in} \cdot G_{DSEF}}{R_{in}}. \tag{6.73}$$

Since the oscillator is a symmetric circuit, the effective transconductance of M_1 and M_2 (also, M_3 and M_4) are the same. Hence, we can rewrite the above equation by

$$G_{M1EF} = \frac{1}{(A_0)} \cdot \frac{1 + R_{in} \cdot G_{DSEF}}{R_{in}} \tag{6.74}$$

and

$$G_{M4EF} = \frac{1}{(A_0 - 1)} \cdot \frac{1 + R_{in} \cdot G_{DSEF}}{R_{in}}. \tag{6.75}$$

We will use (6.74) and (6.75) later for calculating a closed-form equation of this oscillator.

6.4.5 Phase Noise Equation

It is well known that the phase noise and FoM of any RF oscillator at an offset frequency ω_0 from its resonating frequency $\omega_0 = 2\pi f_0$ can be expressed by

$$L(\Delta\omega) = 10\log_{10}\left(\frac{KT}{2 \cdot Q_t^2 \cdot \alpha_I \cdot \alpha_V \cdot P_{DC}} \cdot \left(\frac{\omega_0}{\Delta\omega}\right)^2\right) \tag{6.76}$$

and,

$$FoM = 10\log_{10}\left(\frac{10^3 \cdot K \cdot T}{2 \cdot Q_t^2 \cdot \alpha_I \cdot \alpha_V} \cdot F\right), \tag{6.77}$$

where K is the Boltzmann's constant; T is the absolute temperature; Q_t is the LC-tank quality factor; α_I is the current efficiency, defined as ratio of the fundamental current harmonic I_{ω_0} over the oscillator DC current I_{DC}; and α_V is the voltage efficiency, defined as ratio of single-ended oscillation amplitude $V_{osc}/2$ over the supply voltage V_{DD}. F is the oscillator's effective noise factor and estimated by

$$F = \frac{R_{in}}{2KT} \cdot \sum_k \frac{1}{2\pi} \int_0^{2\pi} \overline{i_{n,k}^2(\phi)} \cdot \Gamma_k^2(\phi) d\phi. \tag{6.78}$$

Let us now calculate the contribution of the losses and active devices. The white current noise power density of the resistive loss of the oscillator is given by

$$\overline{i_{n,loss}^2(\phi)} = \overline{i_{n,tank}^2(\phi)} + \overline{i_{n,G_{ds}}^2(\phi)} = 4KT\left(\frac{1}{R_{in}} + G_{ds}(\phi)\right). \tag{6.79}$$

The relevant impulse sensitivity function of noise sources associated with a sinusoidal waveform oscillator, $V_{osc} \cdot \cos(\phi)$, may be estimated by $\Gamma = \sin(\phi)$ [25, 28]. By exploiting (6.4), the effective noise factor due to resistive losses of the oscillator becomes

$$\begin{aligned} F_{loss} &= \frac{R_{in}}{2KT} \cdot \frac{1}{2\pi} \int_0^{2\pi} \overline{i_{n,loss}^2(\phi)} \Gamma_{loss}^2(\phi) d\phi \\ &= \frac{R_{in}}{2KT} \cdot \frac{1}{2\pi} \int_0^{2\pi} 4KT \left(\frac{1}{R_{in}} + G_{ds}(\phi) \right) \cdot \sin^2(\phi) \cdot d\phi \\ &= \frac{1}{2\pi} \int_0^{2\pi} 2\sin^2(\phi) d\phi + R_{in} \left(\frac{1}{2\pi} \int_0^{2\pi} G_{ds}(\phi) \cdot d\phi \right. \\ &\quad \left. - \frac{1}{2\pi} \int_0^{2\pi} G_{ds}(\phi) \cdot \cos(2\phi) \cdot d\phi \right) \rightarrow F_{loss} \\ &= 1 + R_{in} \left(G_{DS}[0] - G_{DS}[2] \right) = 1 + R_{in} G_{DSEF}, \end{aligned} \tag{6.80}$$

where $G_{DS}[k]$ describes the kth Fourier coefficient of the instantaneous $G_{ds}(\phi)$. From (6.51) and since the oscillator is a symmetric circuit, $G_{DSEF} = \frac{1}{4} \cdot [G_{DSEF1} + G_{DSEF2} + G_{DSEF3} + G_{DSEF4}] = \frac{1}{2} \cdot [G_{DSEF1} + G_{DSEF4}]$. Consequently, we can rewrite (6.80) as

$$F_{loss} = 1 + \frac{R_{in}}{2} \left(G_{DS1EF} + G_{DS4EF} \right). \tag{6.81}$$

To get a better insight, different components of the above equation are graphically illustrated in Figure 6.14(a)–(c). The literature interprets $R_{in}G_{DSEF}$ term in (6.81) as the tank loading effect. In our design, M_1 and M_2 alternatively enter the triode region for part of the oscillation period and exhibit a large channel conductance. As shown in Figure 6.14(a), simulated $0.5R_{in}G_{DS1EF}$ can be as large as 0.6 for the lower-pair transistors. However, $M_{3,4}$ work only in saturation and demonstrate small channel conductance for their entire on-state operation, as evident from Figure 6.14(a). Hence, the simulated value of $0.5R_{in}G_{DS4EF}$ is as low as 0.15 for upper pair transistors. Note that both NMOS and PMOS pairs of the OSC_{NP} structure simultaneously enter the triode region for part of the oscillation period and load the tank from both sides. In this structure, however, only one side of the tank is connected to the AC ground when either M_1/M_2 is in triode while the other side sees high impedance. Hence, this structure at least preserves the charge of differential capacitors over the entire oscillation period. Consequently, compared to the traditional oscillators, the tank loading effect is somewhat reduced here.

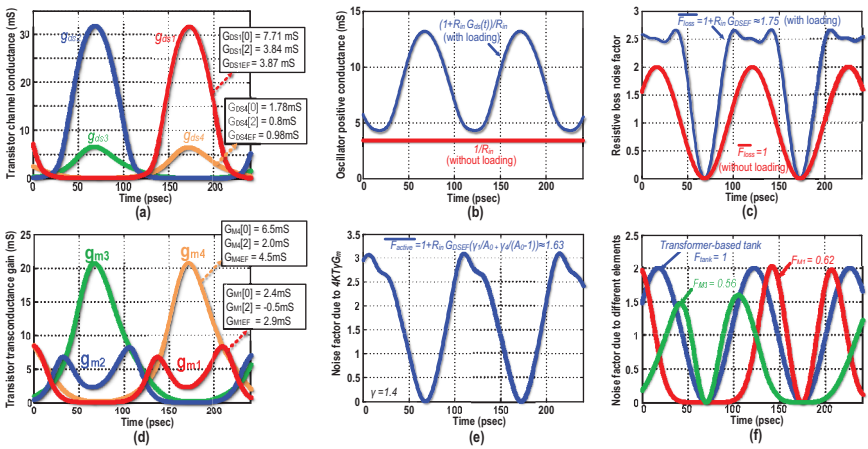

Figure 6.14 Circuit-to-phase-noise conversion across the oscillation period in the switching current-source oscillator. Simulated (a) channel conductance of M_{1-4}; (b) conductance due to resistive losses; (c) noise factor due to losses; (d) transconductance of M_{1-4}; (e) effective noise factor due to transconductance gain; (f) effective noise factors due to different oscillator's components.

The effective noise factor due to transconductance gain can be calculated by

$$F_{active} = \frac{R_{in}}{2KT} \cdot \frac{1}{2\pi} \int_0^{2\pi} \overline{i_{Gm}^2(\phi)} \Gamma_{Gm}^2(\phi) d\phi. \tag{6.82}$$

Replacing (6.11) in (6.82),

$$\begin{aligned} F_{active} &= \frac{R_{in}}{2KT} \cdot \frac{1}{2\pi} \int_0^{2\pi} KT \left(\gamma_1(g_{m1}(\phi) + g_{m2}(\phi)) + \gamma_3(g_{m3}(\phi) \right. \\ &\quad \left. + g_{m4}(\phi))\right) \cdot \sin^2(\phi) \cdot d\phi \\ &= \frac{R_{in}}{4\pi} \int_0^{2\pi} 2\sin^2(\phi) \left(\gamma_1(g_{m1}(\phi) + g_{m2}(\phi)) \right. \\ &\quad \left. + \gamma_3(g_{m3}(\phi) + g_{m4}(\phi))\right) \cdot \left(\frac{1}{2} - \frac{1}{2} cos(2\phi)\right) \\ &= \frac{R_{in}}{4} [\gamma_1(G_{M1}[0] - G_{M1}[2] + G_{M2}[0] - G_{M2}[2]) \\ &\quad + \gamma_4(G_{M4}[0] - G_{M4}[2] + G_{M4}[0] - G_{M4}[2])] \\ &= \frac{R_{in}}{4} [\gamma_1(G_{M1EF} + G_{M2EF}) + \gamma_4(G_{M3EF} + G_{M4EF})] \end{aligned} \tag{6.83}$$

By replacing (6.72) and (6.73) in (6.83),

$$F_{active} = (1 + R_{in}G_{DSEF}) \cdot \left(\frac{\gamma_1}{2A_0} + \frac{\gamma_4}{2(A_0 - 1)} \right). \tag{6.84}$$

To get a better insight, different components of the above equation are graphically illustrated in Figure 6.14(d–e).

As discussed in conjunction with Figure 6.5(c), the transformer's passive voltage gain, A_0, covers a significant part of the required loop gain of the lower positive feedback. Hence, the lower-pair transistors have to compensate only $1/(2A_0)$ of the circuit losses. For the upper positive feedback, however, A_0 covers a smaller part of the required loop gain. Consequently, the upper transistors should work harder and compensate $1/(2(A_0-1))$ of the oscillator loss. Consequently, as (6.84) indicates, the G_M noise contribution by the lower pair is smaller. However, its effect on F_{loss} is larger such that both pairs demonstrate more or less the same contribution to the oscillator PN (see Figure 6.14(f)). Finally, the total oscillator effective noise factor is given by

$$F = F_{loss} + F_{active} = (1 + R_{in}G_{DSEF}) \cdot \left(1 + \frac{\gamma_1}{2A_0} + \frac{\gamma_4}{2(A_0 - 1)} \right). \tag{6.85}$$

To obtain the oscillator phase noise, G_{DS1EF} and G_{DS4EF} should also be calculated or simulated. Since transistor size and oscillation waveforms are known, it is pretty straight-forward to calculate a closed-form equation for them. However, the final equation will be huge and these parameters are calculated numerically here.

When $M_{3,4}$ are not turned off, they work only in saturation and thus their channel conductance and G_{DS4EF} are negligible. However, as shown in the manuscript, precise simulations show that $\frac{R_{in}}{2} \cdot G_{DS4EF}$ can be as large as 0.15 even if the transistor works only in the saturation. It translates to 0.6 dB higher noise factor for this oscillator due to channel conductance noise of $M_{3,4}$ transistors. On the other hand, M_1 and M_2 alternatively enter the triode region for part of the oscillation period. Hence, their effective conductance G_{DS1EF} is larger. Simulations show that $\frac{R_{in}}{2} \cdot G_{DS1EF}$ is about 0.6 in this oscillator. We will also show later that the excess noise factor of NMOS

transistors is 1.4. The voltage gain is 2.16. By replacing those numbers in the nose factor equation, we have

$$F = (1 + 0.6 + 0.15) \cdot \left[1 + \left(\frac{1.4}{2 \cdot 2.15} + \frac{1.4}{2 \cdot 1.15}\right)\right] \approx 5.3\, dB \quad (6.86)$$

the noise factor is just 1.5 dB higher than the ideal value of $(1 + \gamma)$, despite the aforementioned practical issues of designing ulta-low voltage and power oscillators. The phase noise and FoM of this oscillator can be calculated by replacing (6.85) in (6.2).

6.5 1/f Noise Upconversion

Several techniques have been exploited to improve the oscillator's 1/f noise upconversion. First, dynamically switching the bias-setting devices $M_{1,2}$ will reduce their flicker noise, as also demonstrated in [37]. It also lowers a DC component of their effective impulse sensitivity function. Second, as discussed in Chapter 5, [38, 39], a second-order harmonic of the gm-devices' drain current flows into the capacitive part of the tank due to its lower impedance and creates asymmetric rise and fall times for the oscillation waveform. It directly increases a DC value of the oscillator ISF and thus its $1/f^3$ PN corner. This phenomenon can be alleviated by realizing an auxiliary resonance at $2\omega_0$ such that the second harmonic current flows into equivalent resistance of the tank in order to avoid disturbing the rise and fall time symmetry of the oscillation voltage. Since common-mode signals, such as a second harmonic of the drain current, cannot see the tuning capacitance at the transformer secondary winding [21], the auxiliary $2\omega_0$ can be realized without die area penalty and by adjusting the single-ended capacitance at the transformer primary winding [39].

The last source of the 1/f noise is M_{B1} in the biasing circuitry. By exploiting long channel device for biasing, its power consumption becomes negligible compared to the oscillator core while $M_{B1/B2}$ occupy larger area and thus generate lower 1/f noise. Consequently, based on aforementioned techniques, a lower $1/f^3$ PN corner is expected than in the traditional oscillators.

6.6 Optimizing Transformer-Based Tank

The transformer-based tank's input equivalent resistance, R_{in}, and voltage gain, A_0, should be maximized for the best system efficiency. Both optimization parameters are a strong function of $\zeta = L_2C_2/L_1C_1$ [35], as shown in

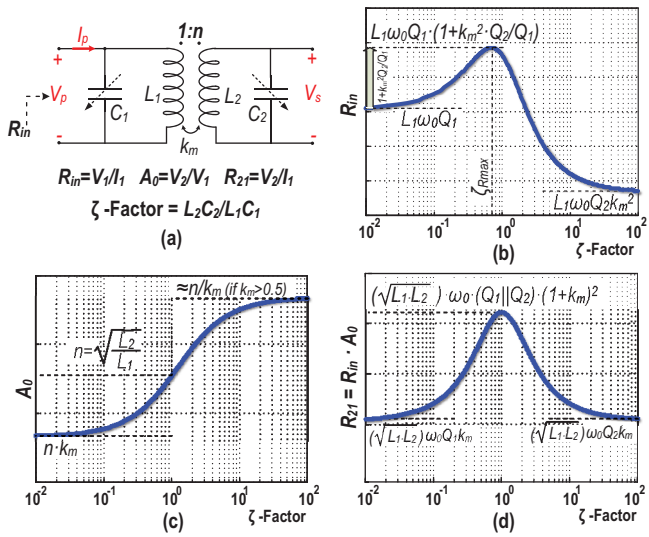

Figure 6.15 Transformer-based tank: (a) schematic; (b) input parallel resistance; (c) voltage gain; and (d) R_{21} versus ζ-factor.

Figure 6.15. R_{in} may be estimated by

$$R_{in} = L_1\omega_0 Q_1 \cdot \frac{\left(1-\left(\frac{\omega_0}{\omega_s}\right)^2(1-k_m^2)\right)\zeta}{-\left(\frac{\omega_0}{\omega_s}\right)^4\left(1+\frac{Q_1}{Q_2}\right)+\left(\frac{\omega_0}{\omega_s}\right)^2\left(1+\frac{Q_1}{Q_2}\zeta\right)}, \tag{6.87}$$

where $\omega_s^2 = 1/L_2C_2$, and Q_1 and Q_2 are, respectively, the Q-factors of the transformer's primary and secondary windings. It can be shown that R_{in} reaches its maximum when

$$\zeta_{Rmax} = \frac{Q_2}{Q_1}\cdot\left(\frac{Q_2}{Q_1+Q_2}\cdot k_m^2 + \frac{Q_1}{Q_1+Q_2}\right). \tag{6.88}$$

Note that the tank Q-factor is maximized at different $\zeta = Q_2/Q_1$ [24]. The maximum R_{in} is obtained by inserting (6.88) into (6.87)

$$R_{inmax} = L_1\omega_0 Q_1\cdot\left(1+k_m^2\cdot\frac{Q_2}{Q_1}\right). \tag{6.89}$$

Consequently, the transformer's coupling factor k_m enhances R_{in} by a factor of $\sim(1+k_m^2)$ at ζ_{Rmax}. For this reason, the switched-capacitor banks

are distributed between the transformer's primary and secondary to roughly satisfy (6.88). For $k_m \geq 0.5$, the voltage gain of the transformer-based tank may be estimated by

$$A_0 = \frac{2k_m n}{1 - \zeta + \sqrt{1 + \zeta^2 + \zeta(4k_m^2 - 2)}}. \tag{6.90}$$

As shown in Figure 6.15(c), A_0 increases with larger ζ. Note that larger R_{in} and A_0 are desired to reduce P_{DC} and P_{buf}, respectively. To consider both scenarios, trans-impedance $R_{21} = R_{in} \cdot A_0$ term is defined and depicted in Figure 6.15(d). R_{21} reaches its maximum at $\zeta = 1$ for $Q_1 \approx Q_2$, which is reasonable for monolithic transformers. We also define the maximum of R_{21} as the transformer FoM $= (Q_1 \| Q_2) \cdot (1 + k_m)^2 \cdot \sqrt{L_1 L_2} \cdot \omega_0$. Consequently, the transformer dimensions and winding spacing are chosen to maximize this term.

6.7 Experimental Results

The oscillator was prototyped in TSMC 40 nm 1P7M CMOS. The chip micrograph is shown in Figure 6.16(a). $M_{1,2}$ and $M_{3,4}$ transistors are minimum-length low-V_t devices with a width of 32 and 256 μm, respectively. The transformer's primary and secondary differential self-inductance is only 660 pH and 2 nH, respectively, with the coupling factor $k_m = 0.76$. Both

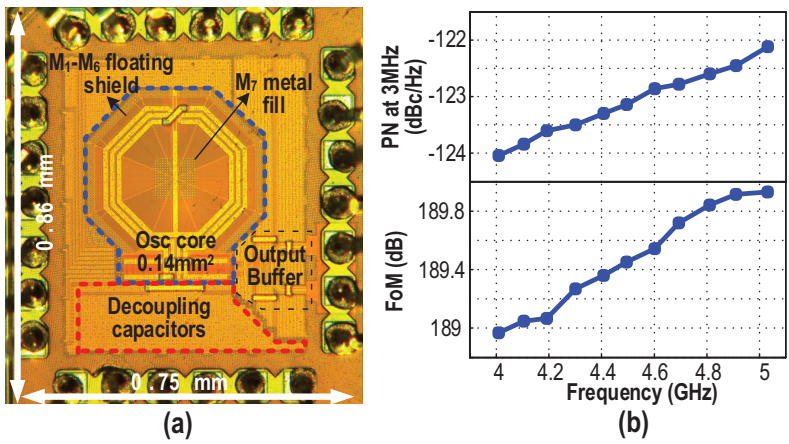

Figure 6.16 (a) Chip micrograph; (b) measured oscillator phase noise and FoM at 3-MHz offset frequency across the tuning range.

transformer's winding are realized with top ultra-thick metal (3.5 μm). However, the transformer includes a floating M1-to-M6 shield to comply with the strict metal density rules (>10%–20%) for manufacturability and also to alleviate the substrate loss. Note that the shield must be significantly thinner than the skin depth at the desired frequency to avoid any attenuation of the magnetic field. The skin depth of copper is ∼0.9 μm at 5 GHz. However, the thickness of M6 layer is 0.85 μm. Hence, adding M6 dummy metal reduces the transformer's magnetic field, inductance, and Q-factor, and thus R_{in} drops by 10%–20%. The simulated Q-factor is 12 and 16 for the primary and secondary windings, respectively.

Figure 6.17 shows the measured PN at the highest and lowest frequencies (f_{max}, f_{min}) with V_{DD} of 0.5 V and P_{DC} of 470 and 580 μW, respectively. Thanks to the switching current-source technique, 1/f^3 PN corner of the oscillator is relatively low and varies between 250 and 420 kHz

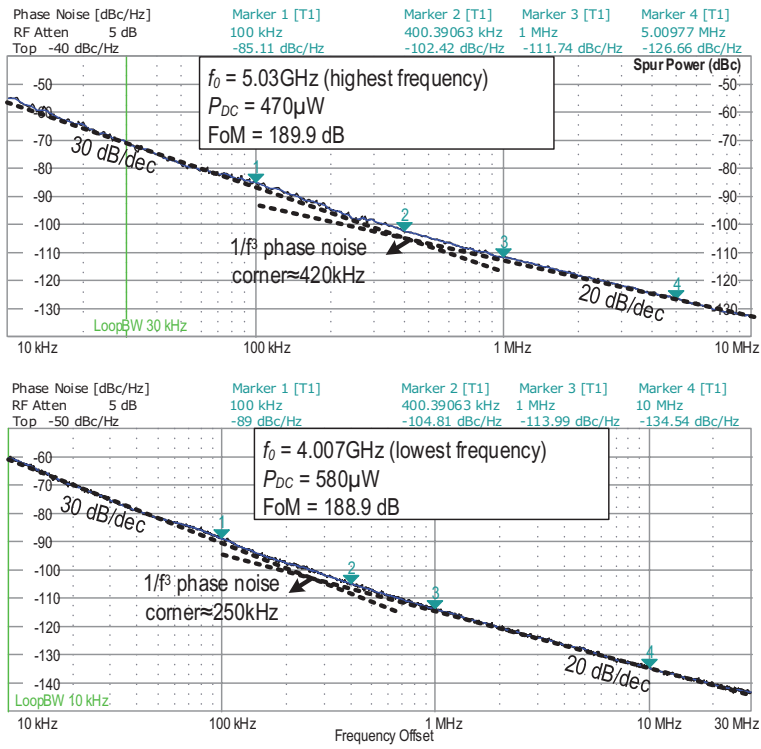

Figure 6.17 Measured phase noise of this oscillator.

Table 6.3 Comparison table of low power oscillators

	This Work	[40] JSSC'05	[23] JSSC'08	[41] ESS-CIRC'14†	[26] ISSCC'14
Technology	40 nm	0.18 μm	0.13 μm	28 nm	40 nm
V_{DD}	0.5 V	0.5 V	1 V	0.5 V	1 V
TR(%)	22.2	8.7	14	N/A	24.5
f_0(GHz)	4.8	3.8	4.9	2.35	2.44
PN (dBc/Hz)‡	−139	−143	−149.5	−125.8	−131.1
P_{DC} (mW)	0.48	0.57	1.4	0.38	0.4
FoM (dB)	189.8	193	195.5	187.5	183
FoM_T (dB)*	196.7	191.7	198.5	N/A	190.8
Freq pushing	17 MHz/V	273 MHz/V	N/A	N/A	N/A
Dummy fill	Yes	No	No	No	No
Area (mm^2)	0.14	0.23	0.11	0.2	0.15
Oscillator topology	Switching current source	TRX feedback	Class-C	Class-D	Traditional

†Including LDO. LDO also performs a start-up role.
‡At $\Delta f = 10$ MHz normalized to 2.4-GHz carrier.
*$\text{FOM}_\text{T} = |\text{PN}| + 20\log_{10}((f_0/\Delta f)(\text{TR}/10)) - 10\log_{10}(P_{DC}(\text{mW}))$.

across the tuning range (TR). The oscillator has a 22.2% TR, from 4 to 5 GHz. Figure 6.16(b) displays plots of phase noise and FoM across the TR. The FoM reaches maximum 189.9 dBc at f_{max} and varies ∼1 dB across the TR.

Table 6.3 summarizes the oscillator performance and compares it with relevant state-of-the-art for P_{DC}<2 mW and TR>8%. It is the only one with the all-layer dummy metal fills inside the LC tank for manufacturability. For the similar P_{DC} (400–600 μW), only the transformer-feedback VCO [40] shows better FoM but with a much larger area, lower TR, and extremely high frequency pushing. Class-C VCO [23] also shows better FoM but at a much higher P_{DC}. Furthermore, it needs additional complex biasing circuits (such as opamp) for proper operation, which can potentially limit its minimum V_{DD} and thus P_{DC}.

It might be interesting to point out that switching current source oscillator is already adapted in a fractional-N ADPLL for BLE [42], in a fully integrated BLE transmitter [18], and a BLE transiver [43].

6.8 Conclusion

A switching current-source oscillator has been described and analyzed, providing deep insights into beneficial circuit operation. It combines advantages of low supply voltage operation of the conventional NMOS cross-coupled oscillator with high current efficiency of the complementary push–pull oscillator to reduce the oscillator supply voltage and dissipated power without sacrificing its start-up robustness or loading tank's Q-factor. The 28-nm CMOS prototype exhibits 189.5 dBc/Hz FoM, with 22% tuning range, dissipating 0.5 mW from 0.5 V power supply, while complying with the process technology manufacturing rules.

References

[1] Y.-H. L., C. Bachmann, X. Wang, Y. Zhang, A. Ba, B. Busze, M. Ding, P. Harpe, G.-J. van Schaik, G. Selimis, H. Giesen, J. Gloudemans, A. Sbai, L. Huang, H. Kato, G. Dolmans, K. Philips, and H. de Groot, "A 3.7 mW-RX 4.4 mW-TX fully integrated Bluetooth Low-Energy/IEEE802.15.4/proprietary SoC with an ADPLL-based fast frequency offset compensation in 40 nm CMOS," *IEEE International Solid-State Circuits Conference Digest of Technical Papers (ISSCC)*, Feb. 2015, pp. 236–237.

[2] T. Sano, M. Mizokami, H. Matsui, K. Ueda, K. Shibata, K. Toyota, T. Saitou, H. Sato, K. Yahagi, and Y. Hayash, "A 6.3 mW BLE transceiver embedded RX image-rejection filter and TX harmonic-suppression filter reusing on-chip matching network," *IEEE International Solid-State Circuits Conference Digest of Technical Papers (ISSCC)*, Feb. 2015, pp. 240–241.

[3] Prummel, M. Papamichail, J. Willms, R. Todi, W. Aartsen, W. Kruiskamp, J. Haanstra, E. Opbroek, S. Rievers, P. Seesink, J. van Gorsel, and H. Woering, "A 10 mW Bluetooth Low-Energy Transceiver With On-Chip Matching," *IEEE J. Solid-State Circuits*, vol. 50, no. 12, pp. 3077–3088, Dec. 2015.

[4] A. Wong, M. Dawkins, G. Devita, N. Kasparidis, A. Katsiamis, O. King, F. Lauria, J. Schiff, and A. Burdett, "A 1V 5 mA multimode IEEE 802.15.6/Bluetooth low-energy WBAN transceiver for biotelemetry applications," *IEEE International Solid-State Circuits Conference Digest of Technical Papers (ISSCC)*, 2012, pp. 300–301.

[5] G. Devita, A. Wong, M. Dawkins, K. Glaros, U. Kiani, F. Lauria, V. Madaka, O. Omeni, J. Schiff, A. Vasudevan, L. Whitaker, S. Yu, and

A. Burdett, "A 5mW multi-standard Bluetooth LE/IEEE 802.15.6 SoC for WBAN applications," *Proceedings of European Solid-state Circuits Conference (ESSCIRC)*, 2014, pp. 283–286.

[6] J. Masuch and M. Delgado-Restituto, "A 1.1-mW-RX 81.4 dBm sensitivity CMOS transceiver for Bluetooth Low Energy," *IEEE Transactions on Microwave Theory and Techniques*, vol. 61, no. 4, pp. 1660–1673, Apr. 2013.

[7] "CC2640 SimpleLinkTM Bluetooth smart wireless MCU," in *Texas Instruments*, 2015, pp. 1–57. Available: http://www.ti.com/lit/ds/symlink/cc2640.pdf.

[8] F.-W. Kuo, M. Babaie, R. Chen, K. Yen, J.-Y. Chien, L. Cho, F. Kuo, C.-P. Jou, F.-L. Hsueh, and R. Staszewski, "A fully integrated 28 nm Bluetooth Low-Energy transmitter with 36% system efficiency at 3 dBm," *Proceedings of European Solid-state Circuits Conference (ESSCIRC)*, 2015, pp. 356–359.

[9] A. Selvakumar, M. Zargham, and A. Liscidini, "Sub-mW current re-use receiver front-end for wireless sensor network applications," *IEEE J. Solid-State Circuits*, vol. 50, no. 12, pp. 2965–2974, Dec. 2015.

[10] F. Zhang, Y. Miyahara, and B. P. Otis, "Design of a 300-mV 2.4-GHz receiver using transformer-coupled techniques," *IEEE J. Solid-State Circuits*, vol. 48, no. 12, pp. 3190–3205, Dec. 2013.

[11] C. Bachmann, M. Vidojkovic, X. Huang, M. Lont, Y.-H. Liu, M. Ding, B. Busze, J. Gloudemans, H. Giesen, A. Sbai, G.-J. van Schaik, N. Kiyani, K. Kanda, K. Oishi, S. Masui, K. Philips, and H. de Groot, "A 3.5 mW 315/400 MHz IEEE802.15.6/proprietary mode digitally-tunable radio SoC with integrated digital baseband and MAC processor in 40nm CMOS," *Proceedings of IEEE VLSI Circuits Symposium*, 2015, pp. 94–95.

[12] P. Whatmough, G. Smart, S. Das, Y. Andreopoulos, and D. Bull, "A 0.6 V All-Digital body-coupled wakeup transceiver for IoT applications," *Proceedings of IEEE VLSI Circuits Symposium*, 2015, pp. 98–99.

[13] S. Bandyopadhyay and A. P. Chandrakasan, "Platform architecture for solar, thermal, and vibration energy combining with MPPT and single inductor," *IEEE J. Solid-State Circuits*, vol. 47, no. 9, pp. 2199–2215, Sept. 2012.

[14] K. Kadirvel, Y. Ramadass, U. Lyles, J. Carpenter, V. Ivanov, V. McNeil, A. Chandrakasan, and B. Lum-Shue-Chan, "A 330 nA

energy harvesting charger with battery management for solar and thermoelectric energy harvesting," *IEEE International Solid-State Circuits Conference Digest of Technical Papers (ISSCC)*, 2012, pp. 106–108.

[15] J. Kim, P. K. T. Mok, and C. Kim, "A 0.15V-input energy-harvesting charge pump with switching body biasing and adaptive dead-time for efficiency improvement," *IEEE International Solid-State Circuits Conference Digest of Technical Papers (ISSCC)*, 2014, pp. 394–395.

[16] X. Liu and E. Sanchez-Sinencio, "A 0.45-to-3V reconfigurable charge-pump energy harvester with two-dimensional MPPT for Internet of Things," *IEEE International Solid-State Circuits Conference Digest of Technical Papers (ISSCC)*, 2015, pp. 370–371.

[17] M. Babaie, M. Shahmohammadi, and R. B. Staszewski, "A 0.5 V 0.5 mW switching current source oscillator," *Proceedings of IEEE Radio Frequency Integrated Circuits (RFIC) Symposium*, 2015, pp. 356–359.

[18] M. Babaie, F. W. Kuo, H. N. Ron Chen, L. C. Cho, C. P. Jou, F. L. Hsueh, Mina Shahmohammadi, and Robert Bogdan Staszewski, "A fully integrated Bluetooth Low-Energy transmitter in 28 nm CMOS with 36% system efficiency at 3 dBm" *IEEE J. Solid-State Circuits*, vol. 51, no. 7, pp. 1547–1565, Jul. 2016.

[19] A. A. Abidi, "Phase noise and jitter in CMOS ring oscillators," *IEEE Journal of Solid-State Circuits,* vol. 41, no. 8, pp. 1803–1816, Aug. 2006.

[20] "Bluetooth Specification Version 4.2," in *Bluetooth*, 2014. Available: http://www.bluetooth.com.

[21] M. Babaie and R. B. Staszewski, "An ultra-low phase noise class-F2 CMOS oscillator with 191 dBc/Hz FoM and long-term reliability," *IEEE J. Solid-State Circuits*, vol. 50, no. 3, pp. 679–692, Mar. 2015.

[22] M. Garampazzi, S. Dal Toso, A. Liscidini, D. Manstretta, P. Mendez, L. Romano, and R. Castello, "An Intuitive Analysis of Phase Noise Fundamental Limits Suitable for Benchmarking LC Oscillators," *IEEE J. Solid-State Circuits*, vol. 49, no. 3, pp. 635–645, Mar. 2014.

[23] A. Mazzanti and P. Andreani, "Class-C harmonic CMOS VCOs, with a general result on phase noise," *IEEE J. Solid-State Circuits*, vol. 43, no. 12, pp. 2716–2729, Dec. 2008.

[24] M. Babaie and R. B. Staszewski, "A class-F CMOS Oscillator," *IEEE J. Solid-State Circuits*, vol. 48, no. 12, pp. 3120–3133, Dec. 2013.

[25] A. Hajimiri and T. H. Lee, "A general theory of phase noise in electrical oscillators," *IEEE J. Solid-State Circuits*, vol. 33, no. 2, pp. 179–194, Feb. 1998.

[26] Y.-H. Chillara, B. Liu, A. Wang, M. Ba, M. Vidojkovic, K. Philips, H. de Groot, and R. Staszewski, "An 860μW 2.1-to-2.7 GHz all-digital PLL-based frequency modulator with a DTC-assisted snapshot TDC for WPAN (Bluetooth Smart and Zigbee) applications," *IEEE International Solid-State Circuits Conference Digest of Technical Papers (ISSCC)*, 2014, pp. 172–173.

[27] J. Bank, "A harmonic-oscillator design methodology based on describing functions," Ph.D. dissertation, Chalmers Univ. Technology, Göteborg, Sweden, 2006.

[28] P. Andreani, X. Wang, L. Vandi, and A. Fard, "A study of phase noise in Colpitts and LC-tank CMOS oscillators," *IEEE Journal of Solid-State Circuits*, vol. 40, no. 5, pp. 1107–1118, May 2005.

[29] P. Andreani and A. Fard, "More on the phase noise performance of CMOS differential pair LC-tank oscillators," *IEEE Journal of Solid-State Circuits*, vol. 41, no. 12, pp. 2703–2712, Dec. 2006.

[30] A. Liscidini, L. Fanori, P. Andreani, and R. Castello, "A 36 mW/9 mW power-scalable DCO in 55 nm CMOS for GSM/WCDMA frequency synthesizers," *IEEE International Solid-State Circuits Conference Digest of Technical Papers (ISSCC)*, 2012, pp. 348–349.

[31] M. Garampazzi, P. M. Mendes, N. Codega, D. Manstretta, and R. Castello, "Analysis and Design of a 195.6 dBc/Hz Peak FoM P-N Class-B Oscillator With Transformer-Based Tail Filtering," *IEEE Journal of Solid-State Circuits*, vol. 50, no. 7, pp. 1657–1668, Jul. 2015.

[32] A. Mazzanti and P. Andreani, "A push-pull class-C CMOS VCO," *IEEE Journal of Solid-State Circuits*, vol. 48, no. 3, pp. 724–732, Mar. 2013.

[33] L. Fanori and P. Andreani, "A high-swing complementary class-C VCO," *Proceedings of European Solid-state Circuits Conference (ESSCIRC)*, 2013, pp. 407–410.

[34] L. Fanori and P. Andreani, "Class-D CMOS oscillators," *IEEE Journal of Solid-State Circuits*, vol. 48, no. 12, pp. 3105–3119, Dec. 2013.

[35] A. Mazzanti and A. Bevilacqua, "On the phase noise performance of transformer-based CMOS differential-pair harmonic oscillators," *IEEE Transactions on Circuits and Systems I, Reg. Papers*, vol. 62, no. 9, pp. 2334–2341, Sept. 2015.

[36] D. Murphy, J. J. Rael, A. A. Abidi "Phase noise in LC oscillators: A phasor-based analysis of a general result and of loaded Q" *IEEE Transactions on Circuits and Systems I, Reg. Papers*, vol. 57, no. 6, pp. 1187–1203, Jun. 2010.

[37] E. Klumperink, S. Gierkink, A. van der Wel, and B. Nauta, "Reducing MOSFET 1/f noise and power consumption by switched biasing," *IEEE Journal of Solid-State Circuits*, vol. 35, no. 7, pp. 994–1001, Jul. 2000.

[38] M. Shahmohammadi, M. Babaie, and R. B. Staszewski, "A 1/f noise upconversion reduction technique applied to class-D and class-F oscillators," *IEEE International Solid-State Circuits Conference Digest of Technical Papers (ISSCC)*, 2015, pp. 444–445.

[39] M. Shahmohammadi, M. Babaie, and R. B. Staszewski, "A 1/f Noise upconversion reduction technique for voltage-biased RF CMOS oscillators," *IEEE Journal of Solid-State Circuits*, vol. 51, no. 11, pp. 2610–2624, Nov. 2016.

[40] K. Kwok and H. C. Luong, "Ultra-low-voltage high-performance CMOS VCOs using transformer feedback," *IEEE Journal of Solid-State Circuits*, vol. 40, no. 3, pp. 652–660, Mar. 2005.

[41] Y. Yoshihara, H. Majima, and R. Fujimoto, "A 0.171-mW, 2.4-GHz Class-D VCO with dynamic supply voltage control," *Proceedings of European Solid-state Circuits Conference (ESSCIRC)*, 2014, pp. 339–342.

[42] N. Pourmousavian, F.-W. Kuo, T. Siriburanon, M. Babaie, and R. B. Staszewski, "A 0.5-V 1.6-mW 2.4-GHz fractional-N all-digital PLL for Bluetooth LE with PVT-Insensitive TDC using switched-capacitor doubler in 28-nm CMOS," *IEEE Journal of Solid-State Circuits (JSSC),* vol. 53, no. 9, pp. 2572–2583, Sept. 2018.

[43] F.-W. Kuo, S. Binsfeld Ferreira, H.-N. R. Chen, L.-C. Cho, C.-P. Jou, F.-L. Hsueh, I. Madadi, M. Tohidian, M. Shahmohammadi, M. Babaie, and R. B. Staszewski, "A Bluetooth low-energy transceiver with 3.7-mW all–digital transmitter, 2.75-mW high-IF discrete-time receiver, and TX/RX switchable on-chip matching network," *IEEE Journal of Solid- State Circuits (JSSC),* vol. 52, no. 4, pp. 1144–1162, Apr. 2017.