ESF LOAD SEQUENCER

SOFTWARE VERIFICATION AND VALIDATION REPORT

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ESF LOAD SEQUENCER

SOFTWARE VERIFICATION AND VALIDATION REPORT

1. OBJECTIVE

The objective of the Software Verification and Validation Study is to verify that the software of the ESF Load Sequencer meets the requirements of the design specification, and that no sneak software paths (circuits) exist that would render the system inoperable. The ESF Load Sequencer is a module in the Balance of Plant (BOP) Engineered Safety Features Actuation System (ESFAS) supplied by General Atomic Company (GA) to the Palo Verde Nuclear Generating Station under Arizona Public Service Company Purchase Order 10407-13-JM-104 and Bechtel Power Corporation Specification 13-JM-104. This module controls loading of the station ESF bus and diesel generators under loss of power conditions or if an accident signal is present.

The purpose of this report is to outline the methods used to perform this study and to detail the findings of the study.

2. STUDY PROCEDURE AND RESULTS SUMMARY

The following steps were taken to perform the study:

a. Review of Bechtel Specification (13-JM-104). This specification was reviewed in detail to determine the functional requirements of the ESF Load Sequencer.

b. Review of General Atomic Operations and Maintenance Manual (E-115-760). This manual was reviewed to determine how the functional requirements had been implemented and in particular, which functions had been implemented in software. The major functions implemented in software are:

   i. Monitoring of accident signals and sequencing control of ESF bus loads.

   ii. Monitoring loss of power condition and generation of load shed signal and loss of power off delay.

   iii. Auto-testing of all ESFAS Modules including ESF Load Sequencer.

c. Review of Software Documentation (SK-1678). This documentation includes program listings and flowcharts for all software modules in the ESF Load Sequencer. The documentation was reviewed for completeness. In addition, each module was reviewed individually to determine that the flowcharts matched the program code, that the program code was properly documented and that the code as implemented performed the required functions.

d. Review of Performance Test Report (E-115-787) and Design Demonstration Test Report (E-160-972). The Performance Test demonstrates the functional performance of the ESFAS equipment. The Design Demonstration Test verifies that the design of the ESF Load Sequencer permits no credible common failure modes to exist in response to credible input perturbations and series of events. Both test reports were reviewed to determine whether the tests exercised all program paths within the software of the ESF Load Sequencer.

The results of this study show that the software of the ESF Load Sequencer meets the requirements of ESFAS Specification, 13-JM-104. Two minor anomalies were noted in the software, neither of which will cause a malfunction of the ESFAS equipment.

The first anomaly results from disabling interrupts during test of the bottom half of RAM memory. This causes an increase in the sampling interval of the contact debounce algorithm which in turn delays posting of an input change. Since the delay is of the order of 10 msec, there is no significant affect on the performance of the ESFAS system.

The second anomaly is in the load sequencer logic and can cause 2 msec pulses on certain relay outputs. The duration of these pulses is not sufficient to cause activation of any device.

3. SPECIFICATION REQUIREMENTS

The Bechtel Specification, 13-JM-104, defines the technical requirements for all aspects of the ESFAS system. The functions specific to the ESF Load Sequencer are defined in Section 4.5.14 of that specification. These functions are implemented in the ESF Load Sequencer software. In addition, this software also controls the auto-testing functions as specified in Section 4.5.13 and certain alarm contact outputs as specified in Section 4.5.16. The major requirements of the specification are:

a. Monitor undervoltage input from LOP/LS module. Upon detection of undervoltage condition generate a 1 second load shed pulse and activate loss of power signal. When undervoltage condition clears ensure that it remains in the cleared condition for 60 seconds before deactivating loss of power signal.

b. Monitor loss of power and accident signals. Upon detection of specific combinations of these inputs, initiate one of four loading sequences or modes (see specification attachment 4-1, sheet 8). Activate one contact per sequencer mode to indicate automatic sequencing in progress. Activate up to ten independent, time separated loading signals, adjustable in one second increments over a total time span of 60 seconds (for sequencer outputs and timing, see specification attachment 4-2, tables 8 and 9, respectively).

c. Automatically test the operation of the maximum possible portion of the ESFAS system. Upon detection of circuit malfunction, immediately initiate remote annunciator and indicate malfunction locally. This automatic testing, under normal or failure condition of the test features must not interfere with the normal operation of system or cause protective action.

4. SOFTWARE STRUCTURE

The software consists of a number of routines which operate in conjunction with each other to fulfill all functions of the system. These routines fall into four categories.

a. System Routines. These routines handle timer interrupts and input/output. They also control the execution of the other programs in the system.

b. Task Routines. These routines implement the major functions in the system, i.e., under voltage monitoring, mode detection/output sequencing and auto-testing.

c. Task Subroutines. These routines implement specific functions within the task routines.

d. Common Subroutines. These routines implement functions common to several tasks.

The software structure and hierarchy is shown in Figure 4-1. Appendix A contains a profile of each routine in the system. The profile lists the following information for each routine:

a. Category (e.g., system routine, task, etc.)

b. Function

c. Verification Study Data, including:

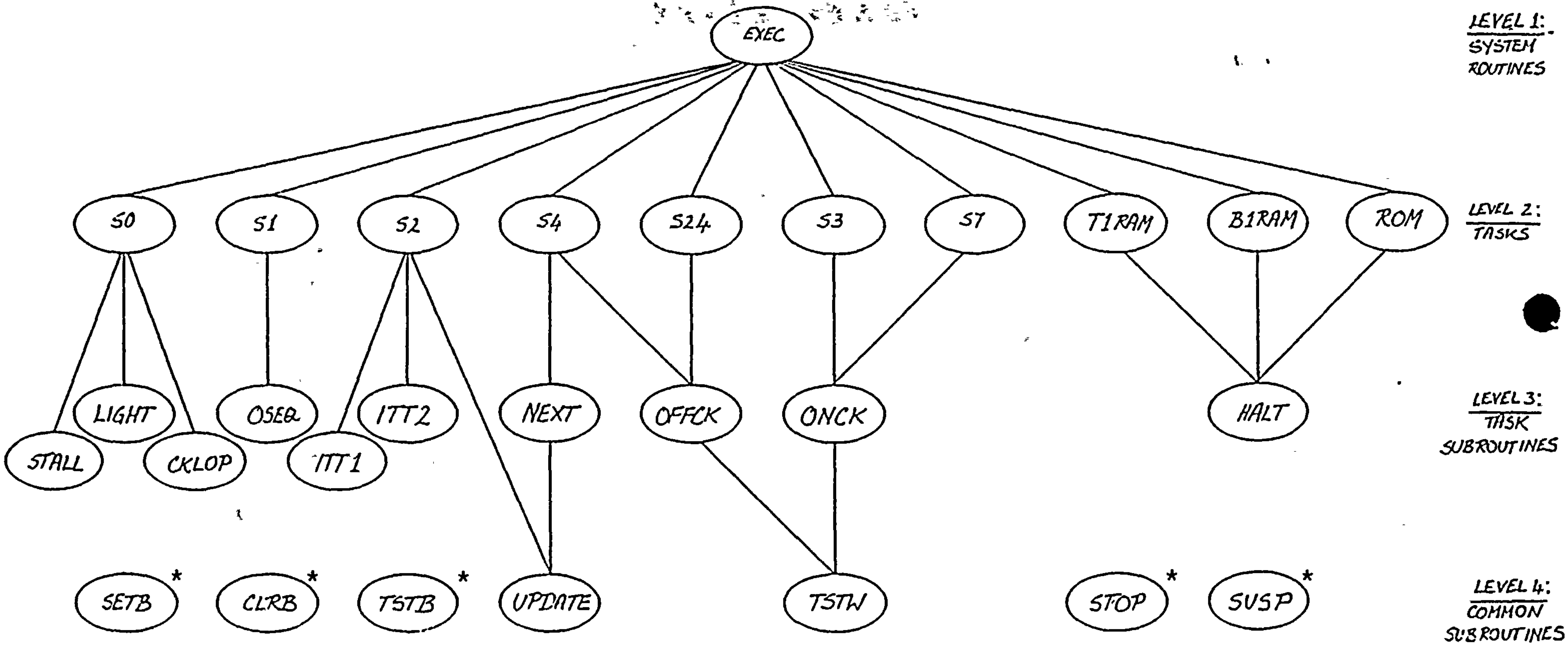
   i. accuracy and completeness of flowcharts

   ii. accuracy and completeness of program listing comments

   iii. specific design demonstration/performance tests which exercise the code

   iv. coding or design errors detected in the routine

   v. comments



* These common subroutines called by multiple tasks or task subroutines

Figure 4-1 Software Structure Chart

5. SYSTEM ROUTINES

To meet the functional requirements defined in section 3, the system must provide the following major features:

a. Accurate time base generator to control time-related functions e.g., input debouncing, load shed pulse duration, loss-of-power off delay and sequencing of loads onto the ESF bus.

b. Concurrent operation of several different functions e.g., undervoltage monitoring, mode determination/load sequencing and automatic testing.

These features are implemented in two system routines, the timer interrupt handler (RST75/RST65) and the executive program (EXEC). The overall design of these programs was validated and the detailed implementation of each feature was verified. Particular emphasis was placed on verification of the major features outlined above.

The system meets the time base generator requirements by implementation of two timer interrupts. The lower priority interrupt occurs every 2 msec, the higher priority interrupt occurs every 10 msec. The 2 msec interrupt routine reads all digital inputs and processes them through a debounce routine. The debounce algorithm is based on the 2 msec sampling time and ensures that the input has reached a steady state before reporting any change to the other software routines. The 10 msec interrupt routine sets a software flag for the executive program in addition to debouncing the inputs. The executive uses this 10 msec flag to allocate execution time to each of the concurrent functions and as a time base to schedule programs handling time-related functions.

The executive allocates 10 msec time slots for execution of the concurrent functions required in the system. Each concurrent function outlined in (b) above is designed as a separate program(s) (see Table 5-1). These programs, or tasks, run under control of the executive which allocates 10 msec time slots to each as required. Within the 10 msec time slot the task must execute to completion and return control to the executive. The system complies with this requirement; the execution time for each task is shown in Table 5-1.

Every 250 msec the executive allocates one 10 msec time slot to the task S0 which monitors the undervoltage condition and checks for a stall condition in the opposite train (redundant system). It also allocates one 10 msec time slot to the task S1 which detects changes in the sequencer mode and performs the bus load sequencing operation. The remaining twenty-three 10 msec time slots are allocated to autotesting tasks. The sequential time slot during which each task may be executed is shown in Table 5-1. Since the task S0 and S1

TABLE 5-1

Task Name	Function Performed	Executed during time-slot	Approximate execution time
S0	Check loss of power condition *Generate/check stall opposite train signal	0	1 msec
S1	Sequencer mode determination Sequencer output control	1	3 msec
S2	*Generate 10msec/50msec module test pulse	2	1 msec
S3	*Check 10 msec module test pulse on	3	1 msec
S4	*Check 10 msec module test pulse off	4	1 msec
S7	*Check 50 msec module test pulse on	7	1 msec
S24	*Check 50 msec module test pulse off	24	1 msec
T1RAM	*Test top half of RAM memory	2-24	7 msec
B1RAM	*Test bottom half of RAM memory	2-24	8 msec
ROM	*Test ROM memory	2-24	4 msec

* Auto testing functions

are executed every 25th time slot, they execute at 250 msec (1/4 sec) intervals. This synchronous execution permits the timed execution of functions at 1 sec intervals as required for load shed pulse, loss-of-power off delay and sequencing of loads onto the ESF bus. This inherent program timing is also used in the autotesting software to control the duration of test pulses to the other ESF modules.

The design was found to be valid and met the system requirements of the specification. No discrepancies were detected in the software implementation of the design.

6. UNDERVOLTAGE MONITORING

The design specification defines the following major requirements for the undervoltage monitoring function:

a. Monitor an input from LOP/LS module for undervoltage condition on the 4.16 kV ESF bus.

b. Upon occurrence of undervoltage condition, generate a one second load shed pulse and set loss of power condition.

c. If undervoltage condition clears and remains cleared for 60 sec, clear loss of power condition (off-delay).

These functions are implemented in subroutine CKLOP which is executed every 250 msec by the task S0. The overall design of the subroutine was validated and the detailed implementation of each feature was verified. Particular emphasis was placed on verification of the major features outlined above.

The program monitors the bus undervoltage input from the LOP/LS module. Upon detection of an undervoltage condition it activates the load shed output to the LOP/LS module and illuminates the loss of power indicator on the Load Sequencer module. Internally it indicates the loss of power condition by setting a software flag. The program uses the synchronous nature of the task (it executes every 250 msec) to control the duration of the load shed pulse. On the fourth execution of the program after the signal is activated, it is deactivated terminating the load shed pulse.

After generation of the load shed pulse, the system continues to monitor the undervoltage input. If the undervoltage clears and remains in the cleared state for 60 seconds, the loss of power indicator is extinguished and the loss of power software flag is cleared. Again, the synchronous nature of the task is used to determine this 60 sec off-delay. Should the undervoltage condition re-occur within the 60 sec off-delay period, the design of the software ensures that the 60 sec off-delay is terminated without resetting the loss of power indicator or flag. A new 60 sec off-delay is started when the undervoltage clears again. The design of the software also ensures that the load shed pulse occurs only once for each loss of power condition. The load shed pulse is generated when the undervoltage condition is first detected. No further load shed pulses are generated until the 60 sec off-delay completes although several undervoltage conditions may occur within this time interval.

The design was found to be valid and met the undervoltage monitoring requirement of the specification. No discrepancies were detected in the software implementation of the design.

7. ESF BUS LOAD SEQUENCING

The design specification defines the following major requirements for the ESF bus load sequencing function:

a. Monitor loss of power condition and accident signal inputs for specified combinations of these inputs.

b. Upon detection of any such combination, initiate/terminate load sequencing mode. The input combinations which cause mode transitions are defined in specification attachment 4-1, sheet 8.

c. Upon initiation of any mode, start bus loading sequence defined for that mode per specification attachment 4-2, table 9. Initiate contact closure to indicate currently active mode.

d. Sequence loads onto ESF bus at the specified time intervals for the active mode.

e. Upon termination of a sequencing mode, return all outputs to idle state (mode 0) and clear mode indication contact.

The mode determination function is implemented in task S1 which executes every 250 msec. The load sequencing function is implemented in the subroutine OSEQ. OSEQ is called by task S1 when the sequencer is in any mode other than mode 0. The overall design of these programs was validated and the detailed implementation of each feature was verified. Particular emphasis was placed on verification of the major features outlined above.

The task S1 checks initially for an active sequencing mode (modes 1-4). If such a mode is active, it verifies that the specified inputs are still in the required state. All inputs which are not specified for the mode are considered as "don't care" inputs and are ignored. If all specified inputs are still true, no mode change is required. If some inputs have changed state, the sequencer returns to the idle state (mode 0), the mode indication output is cleared and all sequencer output signals are returned to the mode 0 condition. The sequencer always returns to the idle state when conditions for the active sequencing mode are no longer true even though conditions may be correct for entry into another sequencing mode. The next execution of the task will cause the transition to the new mode.

If the sequencer is in the idle state (mode 0) upon entry to the task, the loss of power software flag and the accident signals are checked. If the state of these inputs matches the state specified for any of the sequencing modes 1-4, that mode is activated. Again, all inputs which are not specified for the mode are treated as "don't care" conditions. Upon

transition to the mode, the mode indication output is set and the sequencing timer is started.

Prior to exiting task S1, a check of the current sequencing mode is made. If the mode is not zero (output sequence active) the subroutine OSEQ is called. This routine handles the contact closure outputs and the time activation of these signals necessary to sequence the loads onto the ESF bus. Since the routine executes every 1/4 sec the time resolution is sufficiently accurate to meet the load sequencing requirements. The routine is table-driven in design; this means that all sequencing modes are handled by the same executable program code with variable parameters (e.g., output signal, activation time) stored in a table of each mode. All table entries were verified and found to be correct.

A design anomaly was found in the routine OSEQ. As with all digital outputs in the system, this routine sets/clears outputs in the output bit map. This output bit map is copied to the output ports every 2 msec by the timer interrupt routine. Certain actuation signals exist which change state twice during a sequencing mode e.g., Charging Pumps in mode 2. These require two entries in the mode table which specifies the parameters for OSEQ, one to activate the output, the other to deactivate the output. The design of the software is such that if, for example, the signal is activated at time 0 sec and deactivated at time 40 sec, every time the routine executes after the 40 sec time, the signal will first be set, then cleared in the output bit map. If an interrupt occurs while the bit is set, the bit is copied from the bit map to the output port. The bit will remain set until the next interrupt, 2 msec later, by which time OSEQ will have reset the bit. The probability of occurrence of this 2 msec pulse is small; in addition, the duration of the pulse is insufficient to cause actuation of the controlled device. This anomaly will cause no malfunction of the ESFAS system.

All other features of the design were found to be valid and met the requirements of the specification. No discrepancies were detected in the software implementation of the design.

8. AUTOTESTING

The design specification defines the following requirements for the autotesting function:

a. Test automatically and continually maximum possible portion of the ESFAS system.

b. Under normal or failure conditions of the testing system, ensure that it interferes in no way with the normal operation of the system.

c. Upon detection of circuit malfunction, initiate a remote annunciator and locally indicate malfunction.

d. Permit convenient interruption of autotesting at any time.

These functions are implemented in three categories; redundant system (opposite train) monitoring by task S0, ESFAS module testing by tasks S2, S3, S4, S7 and S24, and Load Sequencer testing by tasks T1RAM, B1RAM and ROM. The overall design of each test was validated and the detailed implementation of the testing features verified.

The task S0 monitors a square wave input with a 10 second period which is generated by the opposite train (redundant system). If a transition is not detected every 5 secs, an indicator on the Load Sequencer module is illuminated to indicate a stall. In addition, the stall opposite train annunciator is activated. The task S0 also generates a square wave output with a 10 second period which is monitored by the opposite train. This feature continually monitors the correct operation of each system.

The other testing features are executed only if the Manual/Auto switch is in the Auto position and only if the sequencer is in the idle state (mode 0). The executive routine monitors the Manual/Auto switch and prevents scheduling of the autotest tasks if it is in the Manual position. This meets the requirement to permit convenient interruption of autotesting at any time.

The system tests the other modules within the ESFAS system by generation of test pulses to those modules. The tasks S2, S3 and S4 working in conjunction with each other, generate and test responses to 10 msec test pulses. The tasks S2, S7 and S24 generate and test responses to 50 msec test pulses. The synchronous nature of task scheduling by the executive, permits generation of accurate pulse lengths. This test pulse software is table driven in the same manner as the output sequencer (OSEQ) routine. The test output, the expected module input and the expected test return are all defined within the parameter table for each module. To test

a module the output is set. At 10 msec (or 50 msec) later the state of the module inputs and the test return inputs are tested. If found in the correct state the test output is cleared. At 10 msec (or 170 msec) later the state of the module inputs and the test return inputs are again tested to ensure that they have returned to the cleared state. It should be noted that the program not only tests the correct response of the module input and test return which correspond to the activated test output, but it also tests all other module inputs and test returns to ensure that they do not respond. If an error is detected the test is terminated and the test indicator lamp on the module under test is flashed. The autotest suspend annunciator is also activated. These features satisfy the requirements specified in item (c) above.

Under normal autotesting conditions the task S0 checks for the presence of a real input, as opposed to a test output response. If a real input is found, autotesting is suspended and initiation of the new sequencer mode (if required) will be performed by task S1. Suspension of autotesting due to a real input or due to a module test failure, does not affect the mode determination or the load sequencing functions of the Load Sequencer in any way.

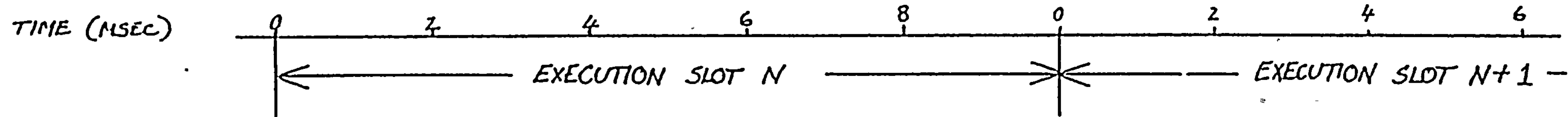
Autotesting of the Load Sequencer module itself is performed by the tasks T1RAM, B1RAM and ROM. These tasks test the top half of RAM memory, the bottom half of RAM memory and ROM memory, respectively. The RAM memory tests do a write/read/compare operation of all data patterns into all RAM memory locations. The ROM memory test does a checksum calculation/comparison operation on all ROM memory locations. If an error is detected in any of these tests, an error light pattern is flashed on the Load Sequencer module and all software functions are inhibited. It is not possible to continue system operation when an error is detected in one of the tests as failure of RAM or ROM can cause unpredictable operation of the system.

An anomaly was found in the design of task B1RAM. Inputs are sampled by the interrupt routine which normally executes at 2 msec intervals. Any input change is processed by a debounce algorithm which requires three consecutive sample values to determine the true debounced state. This results in a delay of up to 4 msec between the occurrence of the change and the reporting of it to the processing task.

Interrupts are disabled while testing the bottom half of RAM. This ensures that no data is changed during execution of the test which requires slightly in excess of 8 msec of the 10 msec exection slot assigned by the Executive. The inputs are sampled once prior to disabling of the interrupt, once upon reenabling of the interrupt and a third time at the end of the 10 ms execution time slot (see Figure 8-1). Assuming

this extended sample interval (8 msec) will still match the mechanical characteristics of the input contact, the delay between the occurrence of the change and the reporting of it to the processing task (i.e., time required for three consecutive samples of the input) has now increased to 10 msec. This is an increase of 150% in the reporting delay experienced with the 2 msec sample interval. It will have no significant affect on the operation of the Load Sequencer however; the undervoltage monitoring and sequencer mode determination functions are only performed once every 250 msec.

All other features of the design were found to be valid and met the requirements of the specification. No discrepancies were detected in the software implementation of the design.



NORMAL EXECUTION

BIRAM EXECUTION

Figure 8-1 Input sampling timing diagram

9. PERFORMANCE/DESIGN DEMONSTRATION TEST RESULTS

The results of the Performance Test Report (E-115-787) and the Design Demonstration Test Report (E-160-972) were reviewed to determine whether all program paths within the software had been exercised by these tests. Appendix A lists tests which exercised the logic of each program. In general, almost all program paths were tested. Exceptions are the failure paths for the RAM and ROM test programs, and the fatal error routine (HALT) to which they transfer control. These program paths are straightforward and perform their designed function.

All test results indicate that the design and implementation of the software fulfill the requirements of the design specification.

10. CONCLUSION

The results of this study show that the software of the ESF Load Sequencer meets all the requirements of the ESFAS Design Specification 13-JM-104. In addition, no sneak circuits or software paths exist that would render the system inoperable. The two anomalies which were noted, 2 msec pulses on sequencer output relays and variations in debounce timing of inputs, will cause no malfunction in the ESFAS equipment.

APPENDIX A

PROGRAM DATA

Program Name:	HALT
Category:	System Routine
Function:	Terminates system execution on fatal error. Displays flashing error code in lights of Load Sequencer module.
Flowchart:	Complete and correct
Source Code Comments:	Adequate
Exercised by:	This routine was not exercised by either the Design Demonstration Test or the Performance Test.
Design/Coding Errors:	None
Comments:	None

Program Name:	COLD
Category:	System Routine
Function:	Initializes software and hardware on system power up (cold start).
Flowchart:	Complete and correct
Source Code Comments:	Adequate
Exercised by:	Performance Test on start up (ELA 342-0062, Sheet 33 of 70)
Design/Coding Errors:	None
Comments:	None

Program Name:	RST75/RST65
Category:	System Routine
Function:	Processes timer interrupts. Reads inputs and stores debounced results in input bit map. Copies output bit map to output ports. Sets 10 msec interrupt flag for executive.
Flowchart:	Complete and correct
Source Code Comments:	Adequate
Exercised by:	Performance Test and Design Demonstration Test on each interrupt (every 2 msec).
Design/Coding Errors:	None
Comments:	None

Program Name:	DEBNC
Category:	System Routine
Function:	Debounces digital inputs. Called by system routine RST75/RST65.
Flowchart:	Complete and Correct
Source Code Comments:	Adequate
Exercised by:	Performance Test and Design Test on each interrupt (every 2 msec).
Design/Coding Errors:	None
Comments:	None

Program Name:	INIT
Category:	System Routine
Function:	Initializes I/O ports and timers. Called by system routine COLD.
Flowchart:	Complete and correct
Source Code Comments:	Adequate
Exercised by:	Performance Test on start up (ELA 342-0062 Sheet 33 of 70)
Design/Coding Errors:	None
Comments:	None

Program Name:	EXEC
Category:	System Routine
Function:	Controls execution of tasks within system.
Flowchart:	Complete and correct
Source Code Comments:	Adequate
Exercised by:	Autotest section of Performance Test (ELA 342-0062 Sheet 55 of 70).
Design/Coding Errors:	None
Comments:	None

Program Name:	SO
Category:	Task
Function:	Calls STALL to check for stall of opposite train (redundant system). Updates system running flag for this train. Calls CKLOP to monitor undervoltage condition. Checks for any real inputs to stop/resume autotesting.
Flowchart:	Complete and correct
Source Code Comments:	Adequate
Exercised by:	Stall/system running; tested by Performance Test (ELA 342-0062, Sheet 65 of 70). Undervoltage monitoring; tested by Design Demonstration Test (ELA 342-0063, Page 16 of 43, Test 1) Stop autotesting on real input; tested by Design Demonstration Test (ELA 342-0063, Page 22 of 43, Test 6) Resume autotesting on absence of real inputs tested by Design Demonstration Test (ELA 342-0063, Page 24/43, Test 8A/8B)
Design/Coding Errors:	None
Comments:	None

Program Name:	S1
Category:	Task
Function:	Monitors loss of power and accident signals to determine sequencing mode. Calls output sequencing (OSEQ) routine to sequence bus loads.
Flowchart:	Complete and correct.
Source Code Comments:	Accurate
Exercised by:	Mode transitions tested by Desing Demonstration Test (ELA 342-0063, Pages 22 and 23 of 43, Tests 6, 7A and 7B).
Design/Coding Errors:	None
Comments:	None

Program Name:	S2
Category:	Task
Function:	Activates test pulse for module autotesting.
Flowchart:	Complete and correct
Source Code Comments:	Adequate
Exercised by:	Performance Test (ELA 342-0062, Sheet 58 of 70).
Design/Coding Errors:	None
Comments:	None

Program Name:	S3
Category:	Task
Function:	Checks "on" condition of test return for 10 msec test pulse (module autotesting) and deactivate test pulse.
Flowchart:	Complete and correct
Source Code Comments:	Adequate
Exercised by:	Performance Test (ELA 343-0062, Sheet 58 of 70).
Design/Coding Errors:	None
Comments:	Task, S3, S4, S7 and S24 are all a part of the same source code module (TEST) and use a common error exit, TSTERR.

Program Name:	S4
Category:	Task
Function:	Check "off" condition of test return for 10 msec test pulse (module autotesting).
Flowchart:	Complete and corret
Source Code Comments:	Adequate
Exercised by:	Performance Test (ELA 34-0062, Sheet 58 of 70).
Design/Coding Errors:	None
Comments:	Part of source code module TEST.

Program Name:	S7
Category:	Task
Function:	Checks "on" condition of test return for 50 msec test pulse (module autotesting) and deactivate test pulse.
Flowchart:	Complete and correct
Source Code Comments:	Adequate
Exercised by:	Performance Test (ELA 342-0062, Shweet 58 of 70).
Design/Coding Errors:	None
Comments:	Part of source code module TEST.

Program Name:	S24
Category:	Task
Function:	Checks "off" condition of test return for 50 msec test pulse (module autotesting).
Flowchart:	Complete and correct
Source Code Comments:	Adequate
Exercised by:	Performance Test (ELA 342-0062, Sheet 58 of 70).
Design/Coding Errors;	None
Comments:	Part of source code module TEST.

Program Name:	T1RAM
Category:	Task
Function:	Tests the top half of RAM memory.
Flowchart:	Complete and correct.
Source Code Comments:	Adequate
Exercised by:	Autotest section of Performance Test (ELA 342-0062, Sheet 58 of 70). Failure condition not encountered during test, hence no testing of failure path.
Design/Coding Errors:	None
Comments:	None

Program Name:	B1RAM
Category:	Task
Function:	Tests the bottom half of RAM memory.
Flowchart:	Complete and correct
Source Code Comments:	Adequate
Exercised by:	Autotest section of Performance Test (ELA 642-0062, Sheet 58 of 70). Failure condition not encountered during test hence no testing of failure path.
Design/Coding Errors:	This test disables interrupt for approximately 8 msec. This affects the input debouncing algorithm and can delay updating of debounced inputs in input bit map. No coding errors.
Comments:	None

Program Name:	ROM
Category:	Task
Function:	Tests ROM memory
Flowchart:	Complete and correct
Source Code Comments:	Adequate
Exercised by;	Autotest section of Performance Test (ELA 642-0062, Sheet 58 of 70). Failure condition not encountered during test hence no testing of failure path.
Design/Coding Errors:	None
Comments:	None

Program Name:	STALL
Category:	Task Subroutine called by S0
Function:	Check for stall of opposite train (redundant system).
Flowchart:	Complete and correct
Source Code Comments:	Adequate
Exercised by:	Exercised continuously during testing. Stall condition simulated during Performance Test (ELA 342-0062, Sheet 65/70)
Design/Coding Errors:	None
Comments:	None

Program Name:	LIGHT
Category:	Task Subroutine called by S0
Function:	Toggles lights which have blink status set.
Flowchart:	Complete and Correct
Source Code Comments:	Minimal
Exercised by:	Performance Test failure simulation. (ELA 342-0062, Sheet 64 of 70).
Design/Coding Errors:	None
Comments:	None

Program Name:	CKLOP
Category:	Task Subroutine called by SO
Function:	Monitors undervoltage condition and generates load shed pulse and loss of power indication.
Flowchart:	Complete and correct
Source Code Comments:	Adequate
Exercised by:	All paths exercised by Design Demonstration Test (ELA 342-0063, Page 19 of 43, Test 4 and Page 18 of 43, Test 3).
Desig/Coding Errors:	None
Comments:	None

Program Name:	OSEQ
Category:	Task Subroutine called by S1
Function:	Controls time sequencing of loads onto ESF bus.
Flowchart:	Complete and correct
Source Code Comments:	Adequate
Exercised by:	Actuation response time measurements of Performance Test (ELA 342-0062, Sheet 40 of 70 to Sheet 44 of 70).
Design/Coding Errors:	Design can cause unwanted 2 msec pulses on signals which change state twice during bus loading sequence.
Comments:	None

Program Name:	ITT1/ITT2
Category:	Task Subroutine called by S2
Function:	Initializes parameters for 10msec/50msec pulse testing of module
Flowchart:	Complete and correct
Source Code Comments:	Adequate
Exercised by:	Autotest section of Performance Test (ELA 342-0062, Sheet 58 of 70).
Design/Code Errors:	None
Comments:	Flowcharts for these programs are included with programs for task S2.

Program name:	ONCK
Category:	Task Subroutine called by S3 and S7.
Function:	Checks "on" condition for specified input, "off" condition for all other inputs.
Flowchart:	Complete and correct
Source Code Comments:	Adequate
Exercised by:	Autotest section of Performance Test (ELA 342-0062, Sheet 58 of 70).
Design/Coding Errors:	None
Comments:	None

Program Name:	OFFCK
Category:	Task Subroutine called by S4 and S24
Function:	Check "off" condition for specified input.
Flowchart:	Complete and correct
Source Code Comments:	Adequate
Exercised by:	Autotest section of Performance Test (ELA342-0062, Sheet 58 f 70).
Design/Coding Errors:	None
Comments:	None

Program Name:	NEXT
Category:	Task Subroutine called by S2 and S24
Function:	Advances testing to next entry in parameter table used for 10msec/50msec pulse testing.
Flowchart:	Complete and correct
Source Code Comments:	Adequate
Exercised by:	Autotest section of Performance Test (ELA 342-0062, Sheet 58 of 70).
Design/Coding Errors:	None
Comments:	None

Program Name:	UPDATE
Category:	Common Subroutine
Function:	Updates test parameters for 10msec/50msec pulse test of module.
Flowchart:	Complete and correct
Source Code Comments:	Adequate
Exercised by:	Autotest section of Performance Test (ELA 3432-0062, Sheet 58 of 70).
Design/Coding Errors:	None
Comments:	None

Program Name:	TSTW
Category:	Common Subroutine
Function:	Compares byte (8 bits) with specified byte of input bit map.
Flowchart:	Complete and correct
Source Code Comments:	Minimal
Exercised by:	Autotesting section of Performance Test (ELA 342-0062, Sheet 58 of 70).
Design/Coding Errors:	None
Comments:	None

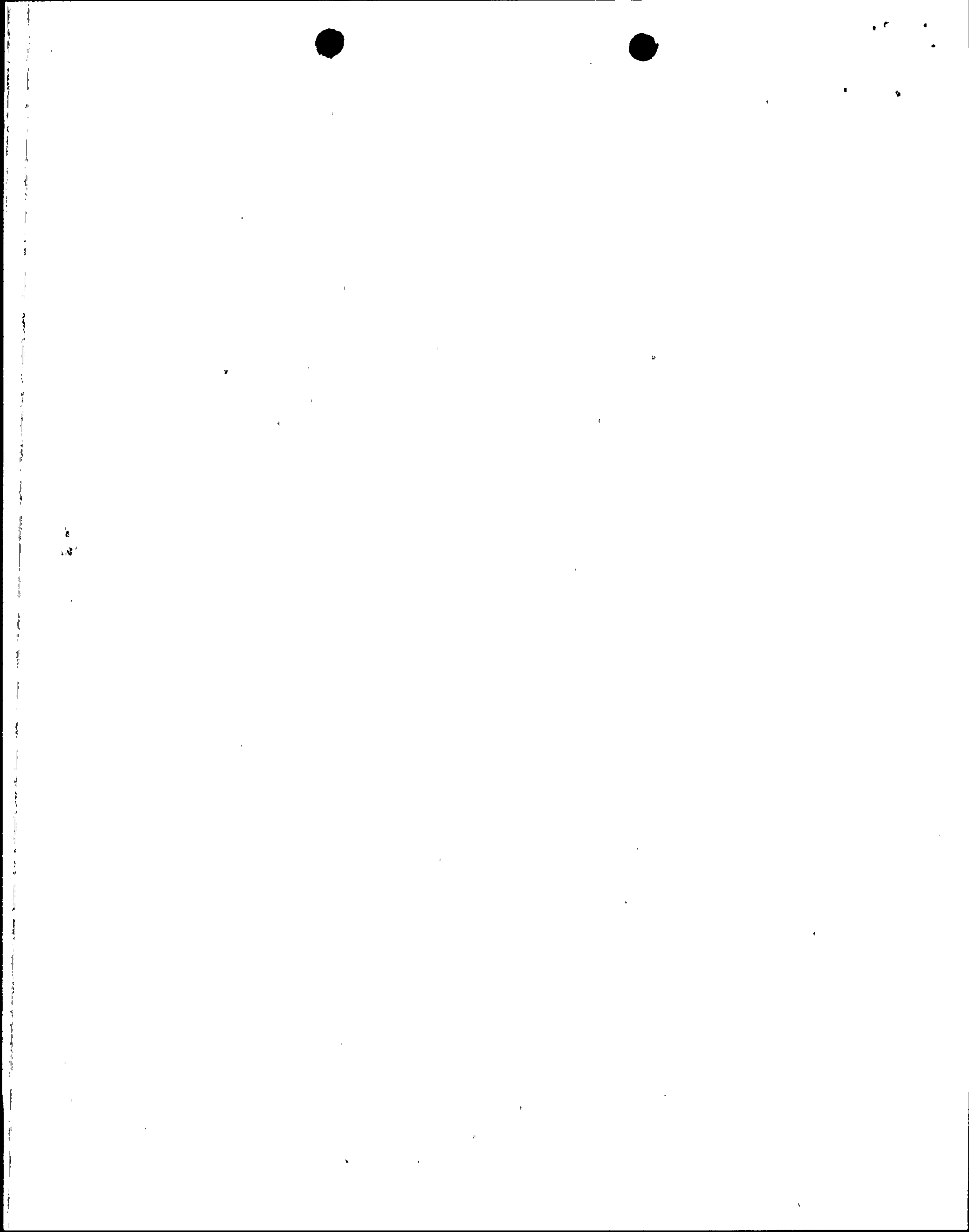
Program Name:	SETB
Category:	Common Subroutine
Function:	Sets bit corresponding to designated output in output bit map.
Flowchart:	Complete and correct
Source Code Comments:	Minimal
Exercised by:	Load shed pulse generation of Design Demonstration Test (ELA 342-0062, Page 19 of 43, Test 4).
Design/Coding Errors:	None
Comments:	None

Program Name:	CLRB
Category:	Common Subroutine
Function:	Clears bit corresponding to designated output in output bit map.
Flowchart:	Complete and correct
Source Code Comments:	Minimal
Exercised by:	Load Shed pulse generation of Design Demonstration Test (ELA 342-0062, Page 19 of 43, Test 4).
Design/Coding Errors:	None
Comments:	None

Program Name:	TSTB
Category:	Common Subroutine
Function:	Tests bit corresponding to designated input in input bit map.
Flowchart:	Complete and correct
Source Code Comments:	Minimal
Exercised by:	Load Shed pulse generation of Design Demonstration Test (ELA 342-0062, Page 19 of 43, Test 4).
Design/Coding Errors:	None
Comments:	None

Program Name:	SUSP
Category:	Common Subroutine
Function:	Calls STOP to terminate sequencing mode or autotesting, then sets system in autotesting suspended state.
Flowchart:	Complete and correct
Source Code Comments:	Adequate
Exercised by:	Autotest termination in Design Demonstration Test (ELA 342-0063, Page 24 of 43, Test 8A/8B).
Design/Coding Errors:	None
Comments:	None

Program Name:	STOP
Category:	Common Subroutine
Function:	Terminates sequencing mode or autotesting. Sets all outputs to idle state and turns off all lights except STOP.
Flowchart:	Complete and correct
Source Code Comments:	Adequate
Exercised by:	Mode 1 or mode 4 termination in Design Demonstration Test (ELA 342-0063, Page 24 of 43, Test 8A/8B).
Design/Coding Errors:	None
Comments:	None



BOP ESFAS CHANGE
Scope of Work

The following software modules have been changed to redefine the bit 7 of OBM+3 from the mode Ø indicator to the stall opposite train annunciator:

By searching the cross reference files for OBM+3 and A7:

1. EQUATE .SRC: Change 1 place for the redefinition of bit 7.
2. S1 .SRC: Remove code in 2 places where the mode Ø indicator was both set and reset.
3. STALL .SRC: Add code in 2 places to both set and reset the stall opposite train annunciator.
4. SUBS .SRC: Change code in STOP routine such that it will not set the mode Ø indicator bit.
5. In addition, add a date and revision module. (ID.SRC)
   Link this module last so that it will be in the second EPROM.

Put the following ASCII data in the date and revision module:

DATE   August 18, 1982

REVISION   PVLS.03

18-AUG-82

```
ASM80 :F1:EQUATE.SRC OBJECT(:F0:EQUATE.OBJ) DEBUG XREF MOD85 PRINT(:T0:)


ISIS-II 8080/8085 MACRO ASSEMBLER, V2.0        EQUATE   PAGE    1


  LOC  OBJ        SEQ        SOURCE STATEMENT

                    1         NAME    EQUATE
                    2 ;       TITLE   ('LOAD SEQUENCER - EQUATE FILE <18-AUG-82>')
                    3 ;
                    4 ;       DATE:             05-JAN-78
                    5 ;       PROGRAMMER:       S. P. SKOGLUND
                    6 ;
                    7 ;****************************************************
                    8 ;
                    9 ;
                   10 ;       THIS FILE CONTAINS THE SYSTEM EQUATES FOR
                   11 ;       THE LOAD SEQUENCER.
                   12 ;
                   13 ;****************************************************
                   14 ;
                   15         PUBLIC  PRT1CS,PRT1A,PRT1B,PRT1C,PRT1TL,PRT1TH
                   16         PUBLIC  PRT2CS,PRT2A,PRT2B,PRT2C,PRT2TL,PRT2TH
                   17         PUBLIC  PRT3A,PRT3B,PRT3C,PRT3CS
                   18         PUBLIC  PRT4A,PRT4B,PRT4C,PRT4CS
                   19         PUBLIC  FBEVAS,CREFAS,CRVIAS,SIAS,LOP,AFAS1,AFAS2,ALLIN
                   20         PUBLIC  TFBEVAS,TCREFAS,TCRVIAS,TCPIAS,TDGSS,TLOP
                   21         PUBLIC  LOP1,LOP60,AUTO,THOD,TDGR,TDGB
                   22         PUBLIC  CCRUN,DGBKR
                   23         PUBLIC  HFSI,LPSI,CREAHU,DGESS,FBEXAF,AF,CS,ECU
                   24         PUBLIC  ESP,ESSCHL,CHSP,DATCH,LC480,CEDNM,CCNTN,NORCHL
                   25         PUBLIC  L0,L1,L2,L3,L4,L5,L6,L7,L8,L9,L10,L11,L12,L13,L14,L15
                   26         PUBLIC  A0,A1,A2,A3,A4,A5,A6,A7
                   27         PUBLIC  R0,R1,R2,R3,R4,R5,R6,R7,R8,R9,R10,R11,R12,R13,R14,R15
                   28         PUBLIC  X4CCAA,X2AA,X2CC,TGSP
                   29 ;
                   30 ;******************************************************************
                   31 ;
                   32 ;
                   33 ;
                   34 ;       HARDWARE PORT ASSIGNMENTS
                   35 ;       -------------------------
                   36 ;
                   37 ;
                   38 ;       DEVICE 1
                   39 ;       --------
                   40 ;
 0010              41 PRT1CS  EQU     16      ;CONTROL/STATUS 1
 0011              42 PRT1A   EQU     17      ;INPUT PORT 1 'A'
 0012              43 PRT1B   EQU     18      ;INPUT PORT 1 'B'
 0013              44 PRT1C   EQU     19      ;INPUT PORT 1 'C'
 0014              45 PRT1TL  EQU     20      ;TIMER LSB 1
 0015              46 PRT1TH  EQU     21      ;TIMER MSB 1
                   47 ;
                   48 ;
                   49 ;       DEVICE 2
                   50 ;       --------
                   51 ;
 0018              52 PRT2CS  EQU     24      ;CONTROL/STATUS 2
```

```
LOC  OBJ        SEQ        SOURCE STATEMENT

0019               53 PRT2A   EQU     25      ;INPUT PORT 2 'A'
001A               54 PRT2B   EQU     26      ;INPUT PORT 2 'B'
001B               55 PRT2C   EQU     27      ;OUTPUT PORT 2 'C'
001C               56 PRT2TL  EQU     28      ;TIMER LSB 2
001D               57 PRT2TH  EQU     29      ;TIMER MSB 2
                   58 ;
                   59 ;
                   60 ;       DEVICE 3
                   61 ;       --------
                   62 ;
                   63 ;
0020               64 PRT3A   EQU     32      ;OUTPUT PORT 3 'A'
0021               65 PRT3B   EQU     33      ;OUTPUT PORT 3 'B'
0022               66 prt3c   equ     34      ;output port 3 'c'
0023               67 PRT3CS  EQU     35      ;CONTROL/STATUS 3
                   68 ;
                   69 ;
                   70 ;       DEVICE 4
                   71 ;       --------
                   72 ;
0028               73 prt4a   equ     40      ;output port 4 'a'
0029               74 prt4b   equ     41      ;output port 4 'b'
002A               75 prt4c   equ     42      ;output port 4 'c'
002B               76 PRT4CS  EQU     43      ;CONTROL/STATUS 4
                   77 ;
                   78 ;*****************************************************************
                   79 ;
                   80 ;
                   81 ;
                   82 ;       MODULE INPUT BIT DEFINITIONS
                   83 ;       ----------------------------
                   84 ;
0100               85 FBEVAS  EQU     0100H   ;FUEL BUILDING ESSENTIAL VENTILATION
0200               86 CREFAS  EQU     0200H   ;CONTROL ROOM ESSENTIAL FILTRATION
0400               87 CRVIAS  EQU     0400H   ;CONTROL ROOM VENTILATION ISOLATION
0800               88 SIAS    EQU     0800H   ;SAFETY INJECTION
1000               89 LOP     EQU     1000H   ;LOSS OF POWER
2000               90 AFAS1   EQU     2000H   ;AUXILIARY FEEDWATER - 1
4000               91 AFAS2   EQU     4000H   ;AUXILIARY FEEDWATER - 2
8000               92 DGRUN   EQU     8000H   ;DIESEL GENERATOR RUN INPUT
                   93 ;
6000               94 X2AA    EQU     AFAS1+AFAS2
0600               95 X2CC    EQU     CREFAS+CRVIAS
6600               96 X4CCAA  EQU     CREFAS+CRVIAS+AFAS1+AFAS2
FF00               97 ALLIN   EQU     FBEVAS+CREFAS+CRVIAS+SIAS+LOP+AFAS1+AFAS2+DGRUN
E700               98 TGRP    EQU     FBEVAS+CREFAS+CRVIAS+AFAS1+AFAS2+DGRUN
                   99 ;
                  100 ;
                  101 ;       TEST RETURN INPUT BIT DEFINITIONS
                  102 ;       ---------------------------------
                  103 ;
0101              104 TFBEVAS EQU     0101H   ;TEST RETURN (FUEL BLDG ESSENTIAL VENTILATION)
0201              105 TCREFAS EQU     0201H   ;TEST RETURN (CNTL ROOM ESSENTIAL FILTRATION)
0401              106 TCRVIAS EQU     0401H   ;TEST RETURN (CNTL ROOM VENTILATION ISOLATION)
0001              107 TSIAS   EQU     0001H   ;TEST RETURN ( ?????? )
```

```
LOC  OBJ         SEQ         SOURCE STATEMENT

1001             108 TDGSS   EQU     1001H   ;TEST RETURN (DIESEL GENERATOR START SIGNAL)
2001             109 TLOP    EQU     2001H   ;TEST RETURN (LOSS OF POWER)
4001             110 XXX     EQU     4001H   ;N/A
8001             111 DGBKR   EQU     8001H   ;DIESEL GENERATOR BREAKER INPUT (MODULE INPUT)
                 112 ;
                 113 ;       SWITCH INPUT BIT DEFINITIONS
                 114 ;       ---------------------------
                 115 ;
0102             116 AUTO    EQU     0102H   ;AUTO/MANUAL SWITCH (0=MAN,1=AUTO)
                 117 ;
                 118 ;       RELAY RETURN INPUT BIT DEFINITIONS
                 119 ;       ----------------------------------
                 120 ;
0103             121 HPSI    EQU     0103H   ;HIGH PRESSURE SAFETY INJECTION PUMP
0203             122 LPSI    EQU     0203H   ;LOW PRESSURE SAFETY INJECTION PUMP
0403             123 CREAHU  EQU     0403H   ;CONTROL ROOM ESSENTIAL AHU
0803             124 DGESF   EQU     0803H   ;DIESEL GENERATOR ESSENTIAL EXHAUST FAN
1003             125 FBEXAF  EQU     1003H   ;FUEL BUILDING ESSENTIAL EXHAUST FAN
2003             126 AF      EQU     2003H   ;AUXILIARY FEEDWATER PUMP
4003             127 CS      EQU     4003H   ;CONTAINMENT SPRAY PUMP
8003             128 ECW     EQU     8003H   ;ESSENTIAL COOLING WATER PUMP
0104             129 ESP     EQU     0104H   ;ESSENTIAL SPRAY POND PUMP
0204             130 ESSCHL  EQU     0204H   ;ESSENTIAL CHILLER
0404             131 CHGP    EQU     0404H   ;CHARGING PUMP PERMISSIVE
0804             132 BATCH   EQU     0804H   ;BATTERY CHARGER
1004             133 LC480   EQU     1004H   ;480 VOLT LOAD CENTER BREAKER
2004             134 CEDNM   EQU     2004H   ;CEDM NORMAL ACU PERMISSIVE
4004             135 CONTN   EQU     4004H   ;CONTAINMENT NORMAL ACU PERMISSIVE
8004             136 NORCHL  EQU     8004H   ;NORMAL CHILLER
                 137 ;
                 138 ;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;
                 139 ;
                 140 ;       LIGHT OUTPUT BIT DEFINITIONS
                 141 ;       ----------------------------
                 142 ;
0100             143 L0      EQU     0100H   ;FBEVAS (FUEL BUILDING ESSENTIAL VENTILATION)
0200             144 L1      EQU     0200H   ;CREFAS (CONTROL ROOM ESSENTIAL FILTRATION)
0400             145 L2      EQU     0400H   ;CPIAS (CONTAINMENT PURGE ISOLATION)
0800             146 L3      EQU     0800H   ;MODULE TEST
1000             147 L4      EQU     1000H   ;LOP/LS TST
2000             148 L5      EQU     2000H   ;AUTO TEST FAIL
4000             149 L6      EQU     4000H   ; ???
8000             150 L7      EQU     8000H   ; ???
0101             151 L8      EQU     0101H   ;CRVIAS (CONTROL ROOM VENTILATION ISOLATION)
0201             152 L9      EQU     0201H   ;DGSS SIAS (DIESEL GENERATOR START SIGNAL -
                 153 ;                                  SAFETY INJECTION ACTUATION SIGNAL)
0401             154 L10     EQU     0401H   ;DGSS LOP (LOSS OF POWER)
0801             155 L11     EQU     0801H   ;DGSS AFAS-1 (AUXILIARY FEEDWATER - 1)
1001             156 L12     EQU     1001H   ;DGSS AFAS-2 (AUXILIARY FEEDWATER - 2)
2001             157 L13     EQU     2001H   ;OTHER SYSTEM STALLED
4001             158 L14     EQU     4001H   ;[illegible]
8001             159 L15     EQU     8001H   ;[illegible] GENERATOR [illegible]
                 160 ;
                 161 ;       ANNUNCIATOR OUTPUT BIT DEFINITIONS
                 162 ;       ----------------------------------
```

```
LOC  OBJ        SEQ      SOURCE STATEMENT

                163 ;
0103            164 A0       EQU     0103H   ;MODE 1 ANNUNCIATOR
0203            165 A1       EQU     0203H   ;MODE 2 ANNUNCIATOR
0403            166 A2       EQU     0403H   ;MODE 3 ANNUNCIATOR
0803            167 A3       EQU     0803H   ;MODE 4 ANNUNCIATOR
1003            168 A4       EQU     1003H   ;LSP DRIVE
2003            169 A5       EQU     2003H   ;STOP INDICATOR
4003            170 A6       EQU     4003H   ;START INDICATOR
8003            171 A7       EQU     8003H   ;STALL OPPOSITE TRAIN ANNUNCIATOR
                172 ;
                173 ;        RELAY OUTPUT BIT DEFINITIONS
                174 ;        ----------------------------
                175 ;
0104            176 R0       EQU     0104H   ;HP SI
0204            177 R1       EQU     0204H   ;LP SI
0404            178 R2       EQU     0404H   ;CRE AMU
0804            179 R3       EQU     0804H   ;BG ESS (EXAFU)
1004            180 R4       EQU     1004H   ;FSE EXAFU
2004            181 R5       EQU     2004H   ;AF
4004            182 R6       EQU     4004H   ;CS
8004            183 R7       EQU     8004H   ;ECW
0105            184 R8       EQU     0105H   ;ESP
0205            185 R9       EQU     0205H   ;ESS CHL
0405            186 R10      EQU     0405H   ;CHG P
0805            187 R11      EQU     0805H   ;BAT CH
1005            188 R12      EQU     1005H   ;480 LC
2005            189 R13      EQU     2005H   ;CEDH NOR
4005            190 R14      EQU     4005H   ;CCNT NOR
8005            191 R15      EQU     8005H   ;NOR CHL
                192 ;
                193 ;
                194 ;
                195 ;        OUTPUT BIT DEFINITIONS
                196 ;        ----------------------
                197 ;
0106            198 TBGR     EQU     0106H   ;BG RUN TEST PULSE LINE
0206            199 TBGB     EQU     0206H   ;BG BREAKER TEST PULSE LINE
0406            200 LSP1     EQU     0406H   ;LSP 1 SEC PULSE
0806            201 LSP60    EQU     0806H   ;LSP 60 SEC OFF-DELAY OUTPUT
2006            202 TMOD     EQU     2006H   ;MODULE TEST PULSE LINE
                203 ;
                204 ;
                205          END

PUBLIC SYMBOLS
A0     A 0103   A1     A 0203   A2     A 0403   A3     A 0803   A4     A 1003   A5     A 2003   A6     A 4003
A7     A 8003   AF     A 2003   AFAB1  A 2000   AFAB2  A 4000   ALLAN  A FF00   AUTO   A 0102   BATCH  A 4004
CEDHN  A 2004   CHGP   A 0404   CCNTN  A 4004   CREAMU A 0103   [illegible] A 0200   [illegible] A 0200   CS     A 4003
[illegible] A 9001   [illegible] A 0203   [illegible] A 8000   ECW    A 8003   ESP    A 0104   ESSCHL A 0204   FBEVAS A 0100
[illegible] A 1003   [illegible] A 0103   L0     A 0100   L1     A 0200   L10    A 0401   L11    A 0801   L12    A 1001
L13    A 2001   L14    A 4001   L15    A 8001   L2     A [illegible]   L3     A [illegible]   L4     A [illegible]   L5     A [illegible]
L6     A 4000   L7     A [illegible]   L8     A [illegible]   L9     A [illegible]   [illegible] A 1004   LSP    A [illegible]   LSP1   A [illegible]
LSP60  A 0806   LSPI   A 0203   [illegible] A [illegible]   FTT1A  A [illegible]   FTT1B  A 0012   [illegible] A 0013   [illegible] A [illegible]
[illegible] A [illegible]   [illegible] A 0014   [illegible] A 0019   [illegible] A 001A   [illegible] A 001B   FRT2CS A 001C   [illegible] A 001D
FRT2TL A 001E   FPT3A  A 0020   FRT3B  A 0021   FPT3C  A 0022   FRT3CS A 0023   [illegible] A [illegible]   [illegible] A [illegible]
```

LOAD SEQUENCER - EQUATE FILE (18-AUG-82)

```
PRT4C  A 002A   PRT4CS A 002B   R0     A 0104   R1     A 0204   R10    A 0405   R11    A 0805   R12    A 1005
R13    A 2005   R14    A 4005   R15    A 8005   R2     A 0404   R3     A 0804   R4     A 1004   R5     A 2004
R6     A 4004   R7     A 8004   R8     A 0105   R9     A 0205   SIAS   A 0800   TCPIAS A 0801   TCREFA A 0201
TCRVIA A 0401   TDGB   A 0206   TDGR   A 0106   TDGSS  A 1001   TFEEVA A 0101   TGRP   A E700   TLOP   A 2001
THOD   A 2006   X2AA   A 6000   X2CC   A 0600   X4CCAA A 6600
```

EXTERNAL SYMBOLS

USER SYMBOLS

```
A0     A 0103   A1     A 0203   A2     A 0403   A3     A 0803   A4     A 1003   A5     A 2003   A6     A 4003
A7     A 8003   AF     A 2003   AFAS1  A 2000   AFAS2  A 4000   ALLIN  A FF00   AUTO   A 0102   BATCH  A 0804
CEDMN  A 2004   CHOP   A 0404   CONTN  A 4004   CREAHU A 0403   CREFAS A 0200   CRVIAS A 0400   CS     A 4003
DSSNP  A 8001   DSESS  A 0803   DSRUN  A 8000   ECW    A 8003   ESP    A 0104   ESSCHL A 0204   FDEVAS A 0100
FDEXAF A 1003   HPSI   A 0103   L0     A 0100   L1     A 0200   L10    A 0401   L11    A 0801   L12    A 1001
L13    A 2001   L14    A 4001   L15    A 8001   L2     A 0400   L3     A 0800   L4     A 1000   L5     A 2000
L6     A 4000   L7     A 8000   L8     A 0101   L9     A 0201   LC480  A 1004   LOP    A 1000   LOP1   A 0406
LOP60  A 0806   LPSI   A 0203   NORCHL A 8004   PRT1A  A 0011   PRT1B  A 0012   PRT1C  A 0013   PRT1CS A 0010
PRT1TH A 0015   PRT1TL A 0014   PRT2A  A 0019   PRT2B  A 001A   PRT2C  A 001B   PRT2CS A 0018   PRT2TH A 001D
PRT2TL A 001C   PRT3A  A 0020   PRT3B  A 0021   PRT3C  A 0022   PRT3CS A 0023   PRT4A  A 0028   PRT4B  A 0029
PRT4C  A 002A   PRT4CS A 002B   R0     A 0104   R1     A 0204   R10    A 0405   R11    A 0805   R12    A 1005
R13    A 2005   R14    A 4005   R15    A 8005   R2     A 0404   R3     A 0804   R4     A 1004   R5     A 2004
R6     A 4004   R7     A 8004   R8     A 0105   R9     A 0205   SIAS   A 0800   TCPIAS A 0801   TCREFA A 0201
TCRVIA A 0401   TDGB   A 0206   TDGR   A 0106   TDGSS  A 1001   TFEEVA A 0101   TGRP   A E700   TLOP   A 2001
THOD   A 2006   X2AA   A 6000   X2CC   A 0600   X4CCAA A 6600   XXX    A 4001
```

ASSEMBLY COMPLETE, NO ERRORS

A0	26	164#				
A1	26	165#				
A2	26	166#				
A3	26	167#				
A4	26	168#				
A5	26	169#				
A6	26	170#				
A7	26	171#				
AF	23	126#				
AFAB1	19	90#	94	96	97	98
AFAB2	19	91#	94	96	97	98
ALLIN	19	97#				
AUTO	21	115#				
BATCH	24	132#				
CBEMON	24	134#				
CHOP	24	131#				
CONTRL	24	135#				
CREAHD	23	123#				
CSEFAS	19	86#	95	96	97	98
CSVIAS	19	87#	95	96	97	98
CS	23	127#				
DSBMR	22	111#				
DSESS	23	124#				
DSRUN	22	92#	97	98		
ECM	23	125#				
EQUATE	1					
ESP	24	129#				
EISCNL	24	136#				
FEEVAS	19	85#	97	98		
FEEXAF	23	125#				
HFSI	23	121#				
L0	25	143#				
L1	25	144#				
L10	25	154#				
L11	25	155#				
L12	25	156#				
L13	25	157#				
L14	25	158#				
L15	25	159#				
L2	25	145#				
L3	25	146#				
L4	25	147#				
L5	25	148#				
L6	25	149#				
L7	25	150#				
L8	25	151#				
L9	25	152#				
LOAD0	24	133#				
LOP	19	97#	97			
LOP1	21	200#				
LOPA0	21	201#				
LFSI	23	122#				
MCFCNL	24	133#				
OPT1A	15	40#				
[illegible]	15	47#				
OPT1C	15	[illegible]				
OPT1CS	15	41#				

```
PRT1TH   15    44#
PRT1TL   15    45#
PRT2A    16    53#
PRT2B    16    54#
PRT2C    16    55#
PRT2CS   16    52#
PRT2TH   16    57#
PRT2TL   16    56#
PRT3A    17    64#
PRT3B    17    65#
PRT3C    17    66#
PRT3CS   17    67#
PRT4A    18    73#
PRT4B    18    74#
PRT4C    18    75#
PRT4CS   18    76#
R0       27   176#
R1       27   177#
R10      27   186#
R11      27   187#
R12      27   188#
R13      27   189#
R14      27   190#
R15      27   191#
R2       27   178#
R3       27   179#
R4       27   180#
R5       27   181#
R6       27   182#
R7       27   183#
R8       27   184#
R9       27   185#
SIAS     19    82#    97
TCPIAS   20   107#
TCREFA   20   105#
TCRVIA   20   106#
TDBS     21   199#
TDGR     21   192#
TDSBS    20   103#
TFREVA   20   104#
TGSP     20    92#
TLSP     20   109#
THOS     21   202#
XIAA     23    94#
XDDC     23    95#
X4CCAA   23    96#
XXX     110#

CROSS REFERENCE COMPLETE


DATE OF ASSEMBLY -
THURSDAY   AUGUST 19, 1982   *********
```

18-AUG-82

```
ASM80 :F1:S1.SRC OBJECT(:F0:S1.OBJ) DEBUG XREF MOD85 PRINT(:T0:)

ISIS-II 8080/8085 MACRO ASSEMBLER, V2.0        S1       PAGE    1

 LOC  OBJ         SEQ         SOURCE STATEMENT

                   1         NAME    S1
                   2 ;       TITLE   ('S1 - STATE 1 PROCESSOR <18-AUG-82>')
                   3 ;
                   4 ;
                   5 ;       DATE:           11-JAN-78
                   6 ;       PROGRAMMER:     S. P. SKOGLUND
                   7 ;
                   8 ;
                   9         PUBLIC  S1
                  10 ;
                  11         EXTRN   MODE,TYPE,MCNT,SUSP
                  12         EXTRN   SIAS,LOP,DGBKR
                  13         EXTRN   TGRP
                  14         EXTRN   SETB,TSTB,IBH,TERM,OSEQ,CLRB,STOP
                  15         EXTRN   A7,A3,A2,A1,A0
                  16         EXTRN   LOPFLG
                  17 ;
                  18 ;
                  19         CSEG
                  20 ;
                  21 ;
                  22 ;       STATE 1 PROCESSOR MODULE
                  23 ;       ------------------------
                  24 ;
                  25 ;       ENTER EVERY 250 MILLI-SECONDS.  PERFORMS THE FOLLOWING
                  26 ;
                  27 ;               1. CHECKS INPUTS FOR CHANGE OF STATE
                  28 ;                  AND SET MODE TO INPUT CONDITIONS.
                  29 ;
                  30 ;               2. IF NOT IN MODE 0, THEN RUN SEQUENCER.
                  31 ;
0000 3A0000   E   32 S1:     LDA     MODE    ;GET MODE
0003 B7           33         ORA     A       ;MODE 0 ?
0004 CA9A00   C   34         JZ      M0      ;YES, JUMP
0007 3D           35         DCR     A       ;MODE 1 ?
0008 CA7900   C   36         JZ      M1      ;YES, JUMP
000B 3D           37         DCR     A       ;MODE 2 ?
000C CA5700   C   38         JZ      M2      ;YES, JUMP
000F 3D           39         DCR     A       ;MODE 3 ?
0010 CA3E00   C   40         JZ      M3      ;YES, JUMP
                  41 ;
                  42 ;       EXIT MODE 4 CHECK ROUTINE
                  43 ;       -------------------------
                  44 ;
0013 010000   E   45         LXI     B,A3
0016 CD0000   E   46         CALL    SETB    ;TURN ON MODE 4 INDICATOR
0019 010000   E   47         LXI     B,SIAS
001C CD0000   E   48         CALL    TSTB    ;SAFETY INJECTION SIGNAL ON ?
001F [illegible] C 49        JNZ     RESET   ;YES, JUMP
0022 3A0000   E   50         LDA     LOPFLG
0025 B7           51         ORA     A       ;LOSS OF POWER SIGNAL ON ?
0026 [illegible] C 52        JNZ     RESET   ;YES, JUMP
```

```
LOC  OBJ         SEQ       SOURCE STATEMENT

0029 010000   E   53       LXI    B,TEMP
002C CD0000   E   54       CALL   TSTB    ;FEEVAS, CLEFAS, CRVIAS, AFAS1, AFAS2, LGRUN ON ?
002F CA8F00   C   55       JZ     RESET   ;JUMP IF NONE ON
0032 C3FE00   C   56       JMP    CHECK   ;OTHERWISE CHECK MODE
                  57 ;
                  58 ;       EXIT MODE 3 CHECK ROUTINE
                  59 ;       ------- -----------------
                  60 ;
0035 010000   E   61 M3:   LXI    B,A2
0038 CD0000   E   62       CALL   SETB    ;TURN ON MODE 3 INDICATOR
003B 010000   E   63       LXI    B,SIAS
003E CD0000   E   64       CALL   TSTB    ;SAFETY INJECTION SIGNAL ON ?
0041 C28F00   C   65       JNZ    RESET   ;YES, JUMP
0044 3A0000   E   66       LDA    LOPFLG
0047 B7           67       ORA    A       ;LOSS OF POWER CYCLE ON?
0048 CA8F00   C   68       JZ     RESET   ;NO, JUMP
004B 010000   E   69       LXI    B,DGBKR
004E CD0000   E   70       CALL   TSTB    ;DIESEL GENERATOR BREAKER SIGNAL ON ?
0051 CA8F00   C   71       JZ     RESET   ;NO, JUMP
0054 C3FE00   C   72       JMP    CHECK   ;OTHERWISE EXIT.
                  73 ;
                  74 ;       EXIT MODE 2 CHECK ROUTINE
                  75 ;       -------------------------
                  76 ;
0057 010000   E   77 M2:   LXI    B,A1
005A CD0000   E   78       CALL   SETB    ;TURN ON MODE 2 INDICATOR
005D 010000   E   79       LXI    B,SIAS
0060 CD0000   E   80       CALL   TSTB    ;SAFETY INJECTION SIGNAL ON ?
0063 CA8F00   C   81       JZ     RESET   ;NO, JUMP
0066 3A0000   E   82       LDA    LOPFLG
0069 B7           83       ORA    A       ;LOSS OF POWER CYCLE ON ?
006A CA8F00   C   84       JZ     RESET   ;NO, JUMP
006D 010000   E   85       LXI    B,DGBKR
0070 CD0000   E   86       CALL   TSTB    ;DIESEL GENERATOR BREAKER SIGNAL ON ?
0073 CA8F00   C   87       JZ     RESET   ;NO, JUMP
0076 C3FE00   C   88       JMP    CHECK   ;OTHERWISE EXIT
                  89 ;
                  90 ;       EXIT MODE 1 CHECK ROUTINE
                  91 ;       -------------------------
                  92 ;
0079 010000   E   93 M1:   LXI    B,A0
007C CD0000   E   94       CALL   SETB    ;TURN ON MODE 1 INDICATOR
007F 010000   E   95       LXI    B,SIAS
0082 CD0000   E   96       CALL   TSTB    ;SAFETY INJECTION SIGNAL ON ?
0085 CA8F00   C   97       JZ     RESET   ;NO, JUMP
0088 3A0000   E   98       LDA    LOPFLG
008B B7           99       ORA    A       ;LOSS OF POWER SIGNAL ON ?
008C CAFE00   C  100       JZ     CHECK   ;NO, JUMP
                 101 ;
                 102 ;       THIS SECTION WILL CHANGE BACK TO MODE 0
                 103 ;
008F CD0000   E  104 RESET: CALL  SETP    ;SET MODE TO 0 & RESET ALL OUTPUTS
0092 3E07        105       MVI    A,7
0094 320000   E  106       STA    TYPE    ;SET TYPE TO 7 (AUTO SUSPEND)
0097 C30000   E  107       JMP    TEMA
```

```
LOC  OBJ          SEQ        SOURCE STATEMENT

                  108 ;
                  109 ;      EXIT MODE 0 CHECK ROUTINE
                  110 ;      ------------------------
                  111 ;
009A 010000   E   112 MO1:   LXI    B,SIAS
009D CD0000   E   113        CALL   TSTB    ;SAFETY INJECTION SIGNAL ON ?
00A0 C20000   C   114        JNZ    MO6     ;YES, JUMP
                  115 ;
                  116 ;      ENTER MODE 3 OR 4 CHECK ROUTINE
                  117 ;      ------------------------------
                  118 ;
00A3 3A0000   E   119        LDA    LOPFLG
00A6 B7           120        ORA    A       ;LOSS OF POWER SIGNAL ON ?
00A7 C2BB00   C  -121        JNZ    MOD     ;YES, JUMP
                  122 ;
                  123 ;      ENTER MODE 4 CHECK ROUTINE
                  124 ;      -------------------------
                  125 ;
00AA 010000   E   126        LXI    B,TGRP
00AD CD0000   E   127        CALL   TSTB    ;FIRVAS, CREFAS, CRVIAS, AFAS1, AFAS2, DGRUN ON ?
00B0 CAFE00   C   128        JZ     CHECK   ;NO, JUMP
00B3 010000   E   129        LXI    B,A3
00B6 1604         130        MVI    D,4
00B8 C3E900   C   131        JMP    CHANGE  ;CHANGE TO MODE 4
                  132 ;
                  133 ;      ENTER MODE 3 CHECK ROUTINE
                  134 ;      -------------------------
                  135 ;
00BB 010000   E   136 MOD:   LXI    B,DGBKR
00BE CD0000   E   137        CALL   TSTB    ;DIESEL GENERATOR BREAKER ON ?
00C1 CAFE00   C   138        JZ     CHECK   ;NO, JUMP
00C4 010000   E   139        LXI    B,A2
00C7 1603         140        MVI    D,3
00C9 C3E900   C   141        JMP    CHANGE  ;CHANGE TO MODE 3
                  142 ;
                  143 ;      ENTER MODE 1 OR 2 CHECK ROUTINE
                  144 ;      ------------------------------
                  145 ;
00CC 3A0000   E   146 MO9:   LDA    LOPFLG
00CF B7           147        ORA    A       ;LOSS OF POWER SIGNAL ON ?
00D0 CAE400   C   148        JZ     MOJ     ;NO, JUMP
                  149 ;
                  150 ;      ENTER MODE 2 CHECK ROUTINE
                  151 ;      -------------------------
                  152 ;
00D3 010000   E   153        LXI    B,DGSNR
00D6 CD0000   E   154        CALL   TSTB    ;DIESEL GENERATOR [illegible] SIGNAL ON ?
00D9 CAFE00   C   155        JZ     CHECK   ;NO, JUMP
00DC 010000   E   156        LXI    B,A1
00DF 1602         157        MVI    D,2
00E1 C3E900   C   158        JMP    CHANGE  ;CHANGE TO MODE 2
                  159 ;
                  160 ;      ENTER MODE 1 CHECK ROUTINE
                  161 ;      -------------------------
                  162 ;
```

```
LOC  OBJ         SEQ         SOURCE STATEMENT

00E4 010000  E   163 MOJ:    LXI     B,A0
00E7 1601        164         MVI     D,1      ;CHANGE TO MODE 1
                 165 ;
                 166 ;       THIS SECTION WILL CHANGE THE MODE FROM 0 TO 'X'.
                 167 ;
00E9 CD0000  E   168 CHANGE: CALL    STOP     ;SET TO STOP (MANUAL) STATE
00EC 7A          169         MOV     A,D
00ED 320000  E   170         STA     MODE     ;SET MODE
00F0 CD0000  E   171         CALL    SETB     ;TURN ON MODE INDICATOR
00F3 3EFF        172         MVI     A,-1
00F5 320500  E   173         STA     IBM15    ;FUDGE UP INPUT MAP
00F8 210000      174         LXI     H,0
00FB 220000  E   175         SHLD    MCNT     ;RESET MASTER COUNTER
                 176 ;
                 177 ;
                 178 ;       COMMON EXIT
                 179 ;
00FE 3A0000  E   180 CHECK:  LDA     MODE
0101 B7          181         ORA     A        ;TEST MODE
0102 C40000  E   182         CNZ     OSEQ     ;CALL OUTPUT SEQUENCER IF NOT MODE 0
0105 C30000  E   183         JMP     TERM     ;AND TERMINATE STATE
                 184 ;
                 185 ;
                 186         END

PUBLIC SYMBOLS
S1     C 0000

EXTERNAL SYMBOLS
A0     E 0000  A1     E 0000  A2     E 0000  A3     E 0000  A7     E 0000  CLRB   E 0000  DBSKR  E 0000
IBM    E 0000  LSP    E 0000  LSPFLG E 0000  MCNT   E 0000  MODE   E 0000  OSEQ   E 0000  SETB   E 0000
SIAS   E 0000  STOP   E 0000  SUSP   E 0000  TERM   E 0000  TGRP   E 0000  TSTB   E 0000  TYPE   E 0000

USER SYMBOLS
A0     E 0000  A1     E 0000  A2     E 0000  A3     E 0000  A7     E 0000  CHANGE C 00E9  CHECK  C 00FE
CLRB   E 0000  DBSKR  E 0000  IBM    E 0000  LSP    E 0000  LSPFLG E 0000  M0     C 009A  MOD    C 00DB
MOD3   C 00CC  MOJ    C 00E4  M1     C 0077  M2     C 0057  M3     C 0075  MCNT   E 0000  MODE   E 0000
OSEQ   E 0000  RESET  C 00BF  S1     C 0000  SETB   E 0000  SIAS   E 0000  STOP   E 0000  SUSP   E 0000
TERM   E 0000  TGRP   E 0000  TSTB   E 0000  TYPE   E 0000

ASSEMBLY COMPLETE,  NO ERRORS
```

```
A0      15     93    163
A1      15     77    156
A2      15     61    139
A3      15     45    129
A7      15
CHANGE  131    141   158   159#
CHECK   56     72    88    100   128   138   155   180#
CLOR    14
IOSNR   12     69    85    136   153
ION     14     173
LOP     12
LOPFLG  16     50    66    82    98    119   146
M0      34     119#
MOD     121    136#
MOG     114    146#
MOJ     143    163#
M1      36     93#
M2      38     77#
M3      40     61#
MONT    11     175
MODE    11     32    170   180
OSEQ    14     182
RESET   49     52    55    65    68    71    81    84    87    97    104#
S1      1      9     32#
SETB    14     46    62    78    94    171
SIAS    12     47    63    79    95    112
STOP    14     168
SUSP    11     104
TERM    14     107   183
TORP    13     53    126
TSTB    14     48    54    64    70    80    86    96    113   127   137   154
TYPE    11     165

CROSS REFERENCE COMPLETE


DATE OF ASSEMBLY -
#########   AUGUST 19, 1982   #########
```

```
LOC  OBJ          SEQ        SOURCE STATEMENT

                   1          NAME    STALL
                   2 ;        TITLE   ('LOAD SEQUENCER - STALL DETECTION LOGIC <13-AUG-82>')
                   3 ;
                   4 ;        DATE:           11-JAN-78
                   5 ;        PROGRAMMER:     S. P. SKOGLUND
                   6 ;
                   7 ;
                   8 ;
                   9          PUBLIC  STALL
                  10 ;
                  11          EXTRN   SLF,TSTALL,SF,SLEV,L13,SETB,CLRB,A7
                  12 ;
                  13 ;
                  14          CSEG
                  15 ;
                  16 ;        STALL DETECTOR ROUTINE
                  17 ;        ----------------------
                  18 ;
0000 C5           19 STALL:   PUSH    B       ;SAVE REGISTERS
0001 D5           20          PUSH    D
0002 E5           21          PUSH    H
0003 110000   E   22          LXI     D,SLF   ;GET ADDRESS OF LOCK FLAG
0006 210000   E   23          LXI     H,TSTALL
0009 3A0000   E   24          LDA     SF      ;GET STALL STATE FLAG
000C B7           25          ORA     A       ;IS OTHER SYSTEM RUNNING ?
000D C22100   C   26          JNZ     ST10    ;YES, JUMP
                  27 ;
                  28 ;        THIS SECTION EXECUTED WHEN OTHER SYSTEM STALLED.
                  29 ;
0010 CD5E00   C   30          CALL    READCK  ;READ AND COMPARE INPUT
0013 CA5E00   C   31          JZ      ST50    ;JUMP IF SAME AS STORED
0016 320000   E   32          STA     SLEV    ;SAVE INPUT LEVEL
0019 3E01         33          MVI     A,1
001B 320000   E   34          STA     SF      ;CLEAR STALL STATE FLAG (SET RUNNING)
001E C33F00   C   35          JMP     ST20
                  36 ;
                  37 ;        THIS SECTION EXECUTED WHEN OTHER SYSTEM IS RUNNING.
                  38 ;
0021 1A           39 ST10:    LDAX    D       ;GET STALL LOCK FLAG
0022 B7           40          ORA     A       ;BEFORE LOCK WINDOW ?
0023 CA4700   C   41          JZ      ST30    ;YES, JUMP
                  42 ;
                  43 ;        AT WINDOW PROCESSOR
                  44 ;
0026 35           45          DCR     M       ;DECREMENT STALL TIMER
0027 CA5?00   C   46          JZ      ST40    ;JUMP IF EXPIRED (STALLED)
002A CD5E00   C   47          CALL    READCK  ;READ AND COMPARE INPUT
002D CA5A00   C   48          JZ      ST?0    ;JUMP IF SAME AS STORED
0030 320000   E   49          STA     SLEV    ;SAVE INPUT LEVEL
                  50 ;
                  51 ;        CYCLE COMPLETE, NOW RESET STALL LIGHT
                  52 ;
```

```
  LOC  OBJ         SEQ         SOURCE STATEMENT

  0033 010000   E   53           LXI    B,L13
  0036 CD0000   E   54           CALL   CLRB    ;TURN OFF STALL LIGHT (STALL OPP TRAIN)
  0039 010000   E   55           LXI    B,A7
  003C CD0000   E   56           CALL   CLRB    ;TURN OFF STALL OPPOSITE TRAIN ANNUNCIATOR
                    57 ;
  003F 3E00         58 ST20:     MVI    A,0
  0041 12           59           STAX   D       ;CLEAR LOOK FLAG
  0042 3610         60           MVI    M,16    ;SET TIMER TO 16 (4 SEC.)
  0044 C36A00   C   61           JMP    ST90
                    62 ;
                    63 ;         BEFORE WINDOW PROCESSOR
                    64 ;
  0047 35           65 ST30:     DCR    M       ;DECREMENT STALL TIMER
  0048 C26A00   C   66           JNZ    ST90    ;JUMP IF STALL RUNNING
  004B 3E01         67           MVI    A,1
  004D 12           68           STAX   D       ;SET LOOK FLAG
  004E 3608         69           MVI    M,8     ;SET TIMER TO 8
  0050 CD6E00   C   70           CALL   READCK  ;READ AND COMPARE INPUT
  0053 CA6A00   C   71           JZ     ST90    ;JUMP IF SAME AS STORED (EXIT)
  0056 320000   E   72           STA    SLEV    ;SAVE INPUT VALUE
  0059 3E00         73 ST40:     MVI    A,0
  005B 320000   E   74           STA    SF      ;SET STALL INDICATOR (NOT RUNNING)
  005E 010000   E   75 ST50:     LXI    B,L13
  0061 CD0000   E   76           CALL   SETB    ;ISSUE STALL ALARM (LIGHT)
  0064 010000   E   77           LXI    B,A7
  0067 CD0000   E   78           CALL   SETB    ;TURN ON STALL OPPOSITE TRAIN ANNUNCIATOR
                    79 ;
                    80 ;         COMMON EXIT
                    81 ;
  006A E1           82 ST90:     POP    H
  006B D1           83           POP    D
  006C C1           84           POP    B
  006D C9           85           RET
                    86 ;
                    87 ;
                    88 ;**************************************************
                    89 ;
                    90 ;
                    91 ;         READCK
                    92 ;
                    93 ;         READ INPUT AND COMPARE WITH STORED VALUE
                    94 ;
  006E E5           95 READCK:   PUSH   H
  006F 210000   E   96           LXI    H,SLEV
  0072 20           97           RIM             ;READ INPUT INTO BIT 7
  0073 E680         98           ANI    080H    ;STRIP OFF OTHER BITS
  0075 BE           99           CMP    M
  0076 E1          100           POP    H
  0077 C9          101           RET
                   102 ;
                   103           END

PUBLIC SYMBOLS
STALL  C 0000

EXTERNAL SYMBOLS
```

```
AP     E 0000   CLRB  E 0000   L13   E 0000   SETB  E 0000   SF    E 0000   SLEV  E 0000   SLF   E 0000
TSTALL E 0000

USER SYMBOLS
AP     E 0000   CLRB  E 0000   L13   E 0000   READCK C 004E  SETB  E 0000   SF    E 0000   SLEV  E 0000
SLF    E 0000   ST10  C 0031   ST20  C 003F   ST30  C 0047   ST40  C 0059   ST50  C 005E   ST70  C 006A
STALL  C 0000   TSTALL E 0000

ASSEMBLY COMPLETE,  NO ERRORS
```

```
57       11     55     77
CLRB     11     54     56
LIB      11     52     75
PEACCK   30     42     79     95#
SETB     11     76     78
SF       11     24     34     74
SLEV     11     32     49     72     96
SLF      11     22
ST10     26     39#
ST20     35     58#
ST30     41     65#
ST40     45     73#
ST50     31     75#
ST90     48     51     66     71     82#
STALL     1      9     19#
TSTALL   11     23

CROSS REFERENCE COMPLETE


DATE OF ASSEMBLY -
##########   AUGUST 19, 1982   ##########
```

18-AUG-82

```
ASM80 :F1:SUBS.SRC OBJECT(:F3:SUBS.OBJ) DEBUG XREF NOPAGING PRINT(:TO:)

ISIS-II 8080/8085 MACRO ASSEMBLER, V2.0        SUBS     PAGE    1

 LOC  OBJ        SEQ        SOURCE STATEMENT

                   1          NAME    SUBS
                   2 ;        TITLE   ('LOAD SEQUENCER - SYSTEM SUBROUTINES,<18-AUG-82>')
                   3 ;
                   4 ;        FILE NAME:      SUBS.SRC
                   5 ;
                   6 ;        DATE:           10-JAN-78
                   7 ;        PROGRAMMER:     S. P. SKOGLUND
                   8 ;
                   9 ;
                  10          EXTRN   OBM,IBM,BLINK,MODE,TYPE
                  11 ;
                  12 ;
                  13          PUBLIC  SETB,CLRB,TSTB,STL
                  14          PUBLIC  LIGHT,TSTW,SUSP,STOP
                  15 ;
                  16          CSEG
                  17 ;
                  18 ;*************************************************
                  19 ;
                  20 ;        SET BIT IN OUTPUT BIT MAP
                  21 ;
                  22 ;        UPON ENTRY:
                  23 ;                B-REG = BIT PATTERN
                  24 ;                C-REG = OFFSET INTO OBM (OUTPUT BIT MAP)
                  25 ;
 0000 C5          26 SETB:    PUSH    B       ;SAVE REGISTERS
 0001 E5          27          PUSH    H
 0002 210000   E  28          LXI     H,OBM
 0005 78          29          MOV     A,B
 0006 0600        30          MVI     B,0
 0008 09          31          DAD     B
 0009 B6          32          ORA     M       ;SET BIT IN OUTPUT TABLE
 000A 77          33          MOV     M,A
 000B E1          34          POP     H
 000C C1          35          POP     B
 000D C9          36          RET
                  37 ;
                  38 ;*************************************************
                  39 ;
                  40 ;        CLEAR BIT IN OUTPUT BIT MAP
                  41 ;
                  42 ;        UPON ENTRY:
                  43 ;                B-REG = BIT PATTERN
                  44 ;                C-REG = OFFSET INTO OBM (OUTPUT BIT MAP)
                  45 ;
 000E C5          46 CLRB:    PUSH    B       ;SAVE REGISTERS
 000F E5          47          PUSH    H
 0010 210000   E  48          LXI     H,OBM
 0013 78          49          MOV     A,B
 0014 2F          50          CMA
 0015 0600        51          MVI     B,0
 0017 09          52          DAD     B
```

```
  LOC  OBJ        SEQ        SOURCE STATEMENT

 0018 A6           53        ANA     M       ;CLEAR BIT IN OUTPUT BIT MAP
 0019 77           54        MOV     M,A
 001A E1           55        POP     H
 001B C1           56        POP     B
 001C C9           57        RET             ;RETURN
                   58 ;
                   59 ;**********************************************
                   60 ;
                   61 ;       TEST BIT IN INPUT BIT MAP
                   62 ;
                   63 ;       UPON ENTRY:
                   64 ;               B-REG = BIT PATTERN
                   65 ;               C-REG = OFFSET INTO IBM (INPUT BIT MAP)
                   66 ;
 001D C5           67 TSTB:  PUSH    B       ;SAVE REGISTERS
 001E E5           68        PUSH    H
 001F 210000   E   69        LXI     H,IBM
 0022 78           70        MOV     A,B
 0023 0600         71        MVI     B,0
 0025 09           72        DAD     B
 0026 A6           73        ANA     M       ;TEST BIT (SET STATUS)
 0027 E1           74        POP     H
 0028 C1           75        POP     B
 0029 C9           76        RET
                   77 ;
                   78 ;******************************************************************
                   79 ;
                   80 ;       TEST WORD (8 BITS) IN INPUT BIT MAP
                   81 ;
                   82 ;       UPON ENTRY:
                   83 ;               B-REG = BIT PATTERN
                   84 ;               C-REG = OFFSET INTO IBM (INPUT BIT MAP)
                   85 ;
 002A C5           86 TSTW:  PUSH    B
 002B E5           87        PUSH    H
 002C 210000   E   88        LXI     H,IBM
 002F 78           89        MOV     A,B
 0030 0600         90        MVI     B,0
 0032 09           91        DAD     B
 0033 BE           92        CMP     M
 0034 E1           93        POP     H
 0035 C1           94        POP     B
 0036 C9           95        RET
                   96 ;
                   97 ;**************************************************************************
                   98 ;
                   99 ;               ******NOTE*****  NOT CURRENTLY USED
                  100 ;
                  101 ;       SET TEST LAMPS ROUTINE
                  102 ;       ----------------------
                  103 ;
                  104 ;
                  105 ;       THIS ROUTINE WILL SET ALL THE OUTPUT TEST LAMPS INDICATED
                  106 ;       BY THE INPUT TEST SWITCHES (SEE TABLE.
                  107 ;
```

```
  LOC  OBJ          SEQ        SOURCE STATEMENT

                    108 ;                    INPUTS           OUTPUTS
                    109 ;                    ------           -------
                    110 ;                 OFFSET  BIT      OFFSET  BIT
                    111 ;        FBEVAS     0      01        0      01
                    112 ;        CREFAS     0      02        0      02
                    113 ;        CRVIAS     0      04        1      01
                    114 ;        SIAS       0      08        1      02
                    115 ;        LOP        0      10        1      04
                    116 ;        AFAS1      0      20        1      08
                    117 ;        AFAS2      0      40        1      10
                    118 ;        DGSUN      2      10        1      40
                    119 ;        DGBKR      2      20        1      80
                    120 ;
  0037 3A0000   E   121 STL:     LDA     IBM
                    122 ;        ANI     3
                    123 ;        MOV     C,A
                    124 ;        LDA     OBM
                    125 ;        ORA     C
                    126 ;        STA     OBM
                    127 ;        LDA     IBM
                    128 ;        ANI     7CH
                    129 ;        RRC
                    130 ;        RRC
                    131 ;        MOV     C,A
                    132 ;        LDA     IBM+2
                    133 ;        ANI     30H
                    134 ;        RLC
                    135 ;        RLC
                    136 ;        ORA     C
                    137 ;        MOV     C,A
                    138 ;        LDA     OBM+1
                    139 ;        ORA     C
                    140 ;        STA     OBM+1
  003A C9           141          RET
                    142 ;
                    143 ;*************************************************************************
                    144 ;
                    145 ;
                    146 ;        THIS ROUTINE WILL TOGGLE ALL THE LIGHTS WHICH
                    147 ;        HAVE THEIR BLINK STATUS BITS SET.
                    148 ;
  003B E5           149 LIGHT:   PUSH    H       ;SAVE REGISTERS
  003C 210000   E   150          LXI     H,OBM+0
  003F 3A0000   E   151          LDA     BLINK
  0042 AE           152          XRA     M
  0043 77           153          MOV     M,A
  0044 23           154          INX     H
  0045 3A0000   E   155          LDA     BLINK+1
  0048 AE           156          XRA     M
  0049 77           157          MOV     M,A
  004A 23           158          INX     H
  004B 3A0000   E   159          LDA     BLINK+2
  004E AE           160          XRA     M
  004F 77           161          MOV     M,A
  0050 E1           162          POP     H
```

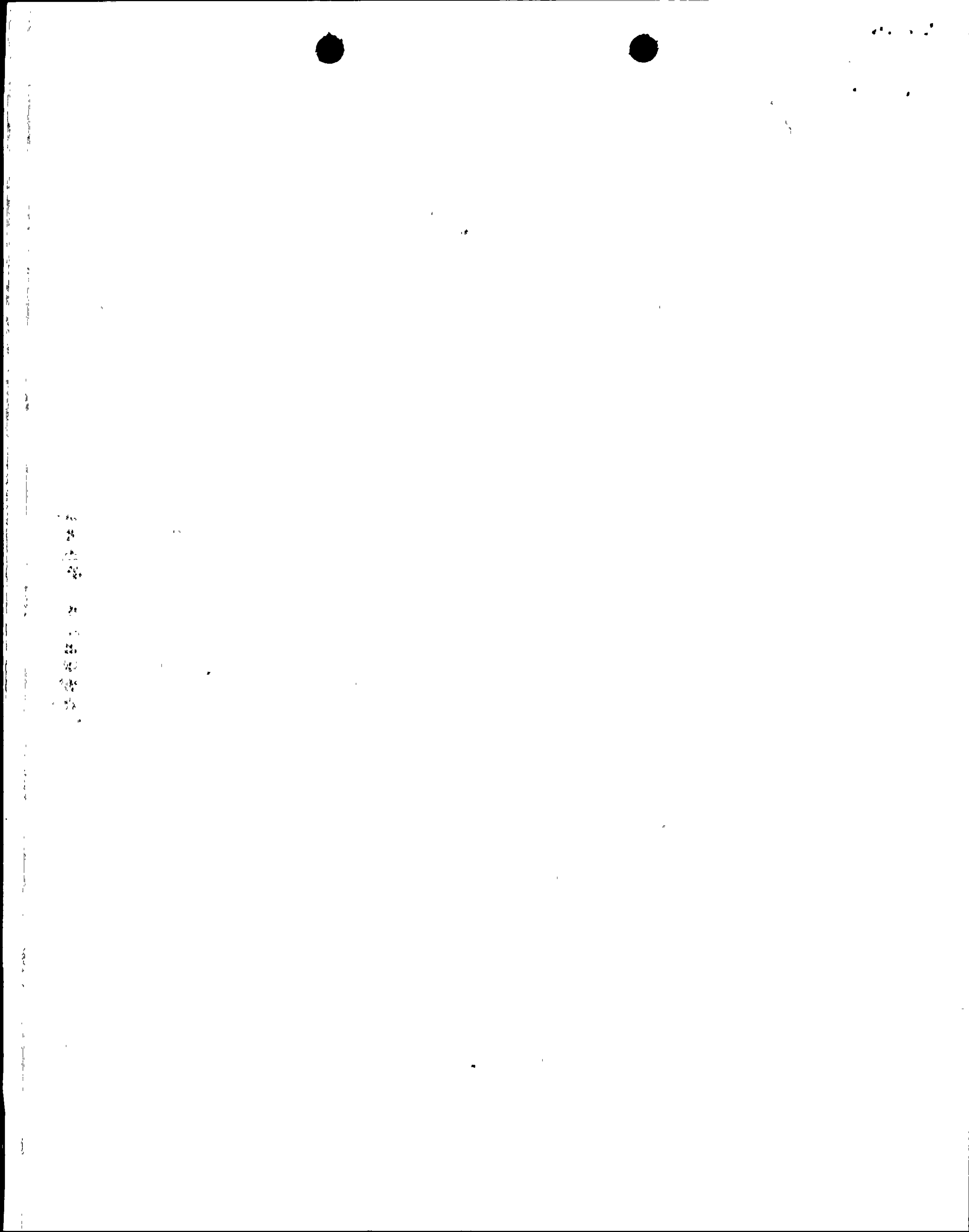
```
  LOC  OBJ          LINE        SOURCE STATEMENT

 0051 C9             163         RET
                     164 ;
                     165 ;**********************************************************************
                     166 ;
                     167 ;          SET TO AUTO SUSPEND STATE
                     168 ;          -------------------------
                     169 ;
                     170 ;          THIS ROUTINE WILL SET THE LOAD SEQUENCER TO THE AUTO
                     171 ;          SUSPEND STATE BY CALLING THE STOP ROUTINE AND THEN SETTING
                     172 ;          THE AUTO TEST SUSPEND ON AND THE TYPE TO 6.
                     173 ;
 0052 E5             174 SUSP:     PUSH    H
 0053 CD6200    C    175           CALL    STOP     ;SET TO STOP STATE
 0056 210000    E    176           LXI     H,OPM
 0059 3620           177           MVI     M,20H    ;SET AUTO TEST SUSPEND -> ON
 005B 3E06           178           MVI     A,6
 005D 320000    E    179           STA     TYPE     ;SET TYPE TO AUTO SUSPEND
 0060 E1             180           POP     H
 0061 C9             181           RET
                     182 ;
                     183 ;**********************************************************************
                     184 ;
                     185 ;
                     186 ;          SET TO STOP STATE
                     187 ;          -----------------
                     188 ;
                     189 ;          THIS ROUTINE DOES THE FOLLOWING:
                     190 ;
                     191 ;                   1. CLEARS ALL OUTPUTS
                     192 ;                   2. TEST LIGHT -> OFF
                     193 ;                   3. TEST PULSE -> OFF
                     194 ;                   4. MODULE ADDRESS SELECT LINES -> OFF
                     195 ;                   5. STOP INDICATOR -> ON
                     196 ;                   6. START INDICATOR -> OFF
                     197 ;                   7. MODE -> 0
                     198 ;                   8. TYPE -> 0
                     199 ;                   9. AUTO TEST SUSPEND -> OFF
                     200 ;
                     201 ;
 0062 E5             202 STOP:     PUSH    H
 0063 210000    E    203           LXI     H,OPM
 0066 3600           204           MVI     M,0      ; #0
 0068 23             205           INX     H
 0069 7E             206           MOV     A,M
 006A E620           207           ANI     20H      ;SAVE STALL OFF TRAIN BIT
 006C 77             208           MOV     M,A      ; #1
 006D 23             209           INX     H
 006E 3600           210           MVI     M,0      ; #2
 0070 23             211           INX     H
 [illegible] 7E      212           MOV     A,M
 [illegible]         213           ANI     [illegible]  ;SAVE STALL OFF TRAIN & [illegible]
 [illegible]         214           ORI     [illegible]  ; #3 [illegible]
 [illegible] 77      215           MOV     M,A
 0077 23             216           INX     H
 [illegible]         217           MVI     M,0      ; #4
```

```
  LOC  OBJ          SEQ        SOURCE STATEMENT

  007A 23            218        INX     H
  007B 3600          219        MVI     M,0     ; 45
  007D 23            220        INX     H
  007E 7E            221        MOV     A,M
  007F E61C          222        ANI     1CH     ;SAVE INTRP ACK & LCP BITS
  0081 77            223        MOV     M,A     ; 46
  0082 AF            224        XRA     A
  0083 320000     E  225        STA     MODE    ;SET MODE TO 0 (TESTING)
  0086 320000     E  226        STA     TYPE    ;SET TYPE TO 0 (STOP)
  0089 E1            227        POP     H
  008A C9            228        RET
                     229 ;
                     230        END

PUBLIC SYMBOLS
CLRB  C 00CE   LIGHT  C 003B   SETB  C 0000   STL    C 0037   STOP  C 0062   SUSP  C 0052   TSTB  C 001D
TSTW  C 002A

EXTERNAL SYMBOLS
BLINK  E 0000   IPM   E 0000   MODE  E 0000   OPM    E 0000   TYPE  E 0000

USER SYMBOLS
BLINK  E 0000   CLRB  C 00CE   IPM   E 0000   LIGHT  C 003B   MODE  E 0000   OPM   E 0000   SETB  C 0000
STL    C 0037   STOP  C 0062   SUSP  C 0052   TSTB   C 001D   TSTW  C 002A   TYPE  E 0000

ASSEMBLY COMPLETE,  NO ERRORS
```

```
[illegible]   10   151   [illegible]   159
[illegible]   13    46#
[illegible]   10    89    [illegible]   121
LIGHT   14   149#
MODE    16   225
OEM     10    28    48   150   176   205
SETP    13    26#
STL     13   120#
STOP    14   175   202#
SUBS     1
SUSP    14   174#
TSTB    13    57#
TSTW    14    86#
TYPE    10   179   226

CROSS REFERENCE COMPLETE


DATE OF ASSEMBLY -
##########   AUGUST 19, 1982   ##########
```

```
ASM80 :F1:ID.SRC OBJECT(:F0:ID.OBJ) DEBUG XREF NOPGS PRINT(:LO:)


ISIS-II 8080/8085 MACRO ASSEMBLER, V2.0          ID        PAGE    1


  LOC  OBJ          SEQ          SOURCE STATEMENT

                      1          NAME    ID
                      2 ;        TITLE   ('IDENTIFICATION MODULE')
                      3 ;
                      4 ;
                      5 ;        DATE:           18-AUG-82
                      6 ;        PROGRAMMER:     S. P. SKOGLUND
                      7 ;
                      8 ;**************************************
                      9 ;
                     10 ;        THIS MODULE CONTAINS THE DATE AND
                     11 ;        THE REVISION NUMBER WHICH WILL BE
                     12 ;        PUT INTO THE LAST EPROM.
                     13 ;
                     14 ;***************************************
                     15 ;
                     16 ;
                     17          CSEG
                     18 ;
                     19          PUBLIC  DATE,VERS
                     20 ;
  0000 41554755      21 DATE:   DB      'AUGUST 18, 1982     '
  0004 53542031
  0008 382C2031
  000C 39383220
  0010 20202020
                     22 ;
  0014 50564C53      23 VERS:   DB      'PVLS.03             '
  0018 2E303320
  001C 20202020
  0020 20202020
  0024 20202020
                     24 ;
                     25          END

PUBLIC SYMBOLS
DATE   C 0000    VERS   C 0014

EXTERNAL SYMBOLS


USER SYMBOLS
DATE   C 0000    VERS   C 0014

ASSEMBLY COMPLETE,  NO ERRORS
```

```
DATE    19    21#
X2       1
ZERO    19    23#

CROSS REFERENCE COMPLETE


DATE OF ASSEMBLY -
**********   AUGUST 19, 1982   **********
```



OPTICAL [illegible]LATOR VOLTAGE STANDOFF TEST JU[illegible]IFICATION AND PROCEDURE OUTLINE

The following constitutes a justification for the recommended procedure for testing the isolation capability of the optical isolator assembly (0342-7100) provided within the PVNGS BOP ESFAS equipment. Attachment A consists of annotated excerpts from Reliability Handbook MIL-HDBK-217C regarding discrete semiconductors, i.e. OPTO-Electronic Devices. Considering the opto-coupler type used (14 each of 4N38A devices) and environmental conditions expected within the equipment, the total MTBF for isolator assembly based upon the isolation standoff characteristic - this assumption is probably overly conservative because the MIL-HDBK-217C model includes all failure except degradation of output light from the light emitting elements - is 13.3 years. This result implies that each opto-isolator assembly (0342-7100) must be removed from its cabinet assembly location and bench tested for voltage isolation standoff capability per the procedure referenced below.

Reference information regarding light output degradation (CTR) is also supplied in Attachment B. Reference information concerning opto-coupler isolation parameter measurements and data sheets for the 4N38A optical isolator devices are provided in Attachment C.

Specification 13-JM-104, Section 4.4.5.2 requires that ..."Electrical isolation provided shall be capable of withstanding application of 1500 V RMS, 60 HZ potential for 60 seconds without degradation of isolation...". The procedure outlined below and performed once every 13.3 years during the plant life for the isolator assembly should verify the voltage isolation characteristic of the cross-train isolator assembly (0342-7100).

Because the isolator assembly is partitioned into two sections via the common input and output return lines (designed to minimize the number of terminals needed on the terminal blocks for circuit interface), two tests will be required to be performed on each assembly. The first test will verify isolator circuits 1 through 8 and 10 (see schematic 0342-7110), while the second test will check out isolator circuits 9 and 11 through 18. If a failure is detected in either test, common troubleshooting techniques may need to be used to locate the failed individual isolators within the applicable group. This additional trouble locating effort is forced by the common input return and output return printed circuit layout.

Figure 1 conceptually indicates the test approach and equipment setup for the voltage isolation standoff verification test.

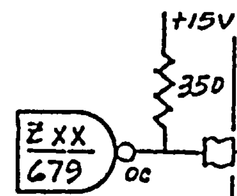
As a first step, the 0342-7100 isolator assembly must be removed from the applicable logic cabinet by carefully disconnecting the associated input and output wiring harness. Particular attention should be given to disturbing the lead dress as little as possible so as to minimize wiring reconnection errors.

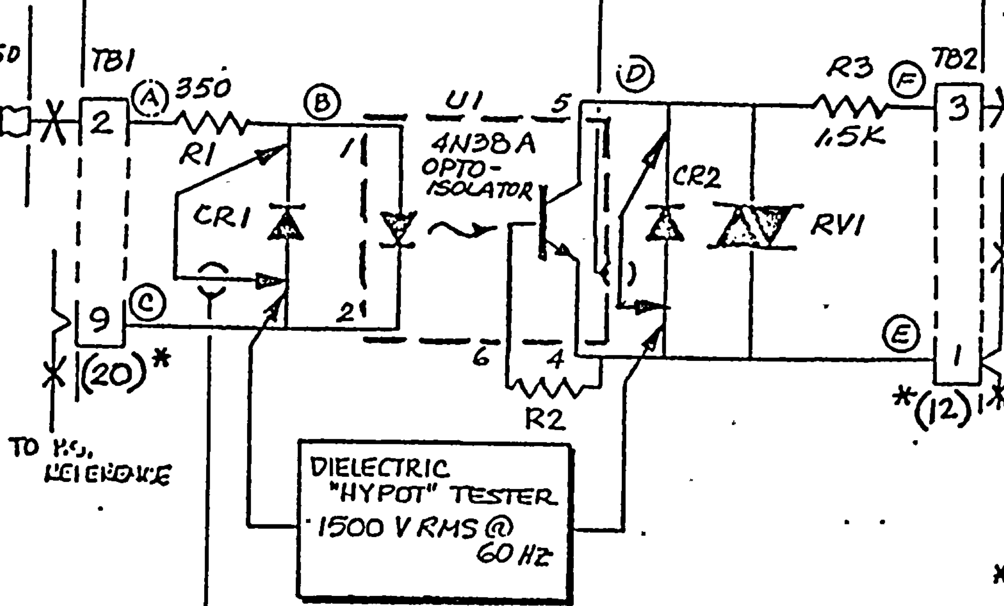
Secondly, a shorting jumper should be placed across each protection diode associated with both the input and output of each optical-coupler device. This jumper protects against damage to either the input led or the output transistor of the isolator from high capacitive charging currents impressed by high dv/dt's during the application of the test voltage.

Thirdly, a high voltage breakdown generator (GAC recommends the standard "AC Hypot Junior" unit manufactured by Associated Research, Inc., 8221 North Kimball Avenue, Skokie, Illinois, 60076, or equivalent.) is impressed across terminals TB1-9 and TB2-1, and checks are made for any breakdown with the test generator set to 1500 V RMS, 60 HZ output. This test voltage should be applied for 60 seconds minimum. The test generator must then be moved between terminals TB1-20 and TB2-12 and the same isolation breakdown check made.

After successful bench test completion, the test jumpers should be removed, the isolation assembly carefully re-installed in the logic cabinet, and wiring connection verified. After verification, normal manual test procedures should be conducted to verify that each cross train isolator circuit employed functions properly.

CAUTION:
REMOVE ISOLATOR ASSEMBLY FROM LOGIC CABINET FOR TEST.





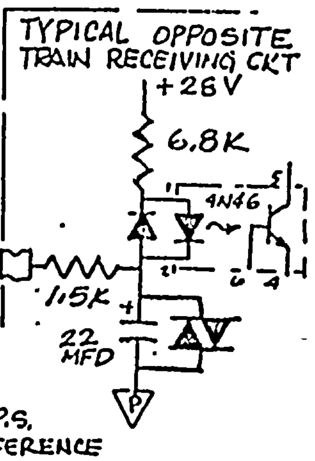


FIGURE 1

Isolator network schematic For IN-SITU Hypot testing to insure 1500 VAC isolation standoff characteristic.

* TEST 1 COVERS ISOLATOR CIRCUITS 1 THROUGH 8; 10 BY HYPOT TESTER BEING CONNECTED BETWEEN TERMINALS TB1-9 AND TB2-1.

TEST 2 COVERS ISOLATOR CIRCUITS 11 THROUGH 18; 9 BY HYPOT TESTER BEING CONNECTED BETWEEN TERMINALS TB1-20 AND TB2-12.

ATTACHMENT A
EXERPTS FROM: WITH RELIABILITY CALCULATION ANNOTATIONS.

2.2.10 Opto-electronic Semiconductor Devices, Group X.

SPECIFICATION	DESCRIPTION
MIL-S-19500	Light Emitting Diode (LED)
MIL-S-19500	Opto-electronic Coupler (Isolator)
None	LED Alpha-numeric Display

The part failure rate model, λ_p, is:

$$\lambda_p = \lambda_b \pi_C \pi_E \pi_Q \text{ failures}/10^6 \text{ hours}$$

$= (0.0034)(1.8)(1)(100) = 0.612$ FAILURES/10^6 HOURS FOR EACH 4N38A

where:

λ_b = base failure rate in failures/10^6 hrs., Table 2.2.10-4.
π_C = complexity factor, Table 2.2.10-3.
π_E = environmental factor, Table 2.2.10-1.
π_Q = quality factor, Table 2.2.10-2.

The above model includes all failures except degradation of output light from the light emitting elements.* For model background and guidance concerning light degradation, see Bibliography Item No. 49.

TABLE 2.2.10-1
π_E, ENVIRONMENTAL FACTOR
SEE PP. 2-3,4 FOR DEFINITION

Environment	π_E
G_B	1
S_F	1
G_F	2
A_{IT}	2.8
A_{IF}	5.6
N_S	4
G_M	4
N_U	5
A_{UT}	4.2
A_{UF}	8.4
M_L	10

TABLE 2.2.10-2
π_Q, QUALITY FACTOR

Quality Level	π_Q
JANTXV	1
JANTX	2
JAN	10
LOWER*	50
PLASTIC**	100

*-Applies to all hermetic packaged alpha-numeric displays and to NON-JAN hermetic packaged LED's and isolators.
**-Applies to all devices encapsulated with organic materials.

ASSUMING EQUAL PROBABILITY OF FAILURE FOR EACH USED ISOLATOR CIRCUIT, AND COMMC REFERENCES FOR EACH INP CIRCUIT AND EACH OUTPUT CIRCUIT; THE TOTAL ISOLATI FAILURE RATE IS:

$\lambda_T = \sum_{i=1}^{14} \lambda_{P_i} = 14(0.612)$ FAILU/10^6HR

$\lambda_T = 8.568$ FAILURE/10^6 HRS
OR
MTBF $= 1/\lambda_T = 116,713$ HRS $= 13.3$ YRS

* CURRENT TRANSFER RATIO (CTR), WHICH IS LIGHT OUTPUT DEPENDENT, ERODES ABOUT 30% WORSE CASE AFTER 30,000 HOURS (GE OPTO ELECTRONICS MANUAL, P.42, RE. OPTO ELECTRONIC COMPONENT RELIABILITY). THIS EROSION, FOR THE APPLICATION EMPLOYED WITHIN THE PVNGS BOP ESFAS EQUIPMENT, IS INSIGNIFICANT BECAUSE ISOLATORS REMAIN IN SATURATION EVE

TABLE 2.2.10-3
π_C, COMPLEXITY FACTOR

Device	π_C	Device	π_C
Single LED	1.0	Alpha-Numeric Displays*	
Single Isolators		1 character	2.8
Simple**	1.5	1 character w/logic chip	3.8
" w/1 trans.	1.8	2 character	4.0
" w/2 trans.	2.2	2 character w/logic chip	5.0
" w/lin. amp.	3.3	3 character	4.9
" w/lin. amp. & 1 trans.	3.6	3 character w/logic chip	5.9
" w/lin. amp. & 2 trans.	4.0	4 character	5.7
Dual Isolators		5 character	6.3
Simple**	2.3	6 character	6.9
" w/2 trans.	2.7	7 character	7.4
" w/4 trans.	3.3	8 character	8.0
" w/2 lin. amps.	5.0	9 character	8.5
" w/2 lin. amps. & 2 trans.	5.4	10 character	8.9
" w/2 lin. amps. & 4 trans.	6.0		

*-The number of characters in a display is the number of characters contained in a single sealed package. For example, a 4 character display comprising 4 separately packaged single characters mounted together would be 4-one character displays, not 1-four character display.

**-Simple isolator(s) contains only a light-emitting element(s) and a light detecting element(s).

TABLE 2.2.10-4
OPTO-ELECTRONIC SEMICONDUCTOR DEVICE
BASE FAILURE RATE, λ_b, IN FAILURES PER 10^6 HOURS

	* S (P_{op}/P_{max} or I_{op}/I_{max})									
T (°C)	.1	.2	.3	.4	.5	.6	.7	.8	.9	1.0
0	.0002	.0003	.0005	.0008	.0012	.0017	.0024	.0034	.0048	.0071
5	.0002	.0004	.0006	.0010	.0014	.0020	.0028	.0040	.0058	.0088
10	.0003	.0005	.0008	.0012	.0017	.0024	.0034	.0048	.0071	.0112
15	.0004	.0006	.0010	.0014	.0020	.0028	.0040	.0058	.0088	.0146
20	.0005	.0008	.0012	.0017	.0024	.0034	.0048	.0071	.0112	.0200
25	.0006	.0010	.0014	.0020	.0028	.0040	.0058	.0088	.0146	.0288
30	.0008	.0012	.0017	.0024	.0034	.0048	.0071	.0112	.0200	
35	.0010	.0014	.0020	.0028	.0040	.0058	.0088	.0146	.0288	
40	.0012	.0017	.0024	.0034	.0048	.0071	.0112	.0200		
45	.0014	.0020	.0028	.0040	.0058	.0088	.0146	.0288		
50	.0017	.0024	.0034	.0048	.0071	.0112	.0200			
55	.0020	.0028	.0040	.0058	.0088	.0146	.0288			
60	[illegible]	.0034	.0048	.0071	.0112	.0200				
65	.0028	.0040	.0058	.0088	.0146	.0288				
70	.0034	.0048	.0071	.0112	.0200					
75	.0040	.0058	.0088	.0146	.0288					
80	.0048	.0071	.0112	.0200						
85	.0058	.0088	.0146	.0288						
90	.0071	.0112	.0200							
95	.0088	.0146	.0288							
100	.0112	.0200								
105	.0146	.0288								
110	.0200									
115	.0288									

*-If derating information for isolators and displays is unavailable, assume S=.5, T_S=25°C, and:

T_{max} = 125°C for hermetic isolators,

T_{max} = 100°C for plastic isolators and for all displays.

See Section 2.2.11.2(7) & (9) for correction factor for S ratio and for the appropriate value of T to use with above table.

33. "Nichrome Resistor Properties and Reliability", RADC-TR-73-181, AD 765534.

34. "Dormancy & Power On-Off Cycling Effects on Electronic Equipment & Part Reliability", RADC-TR-73-248, AD 768619.

35. "Use of Warranties for Defense Avionic Equipment", RADC-TR-73-249, AD 769399/7.

36. "Reliability Acquisition Costs", RADC-TR-73-334, AD 916286L.

37. "Electrical Characterization of Complex Microcircuits", RADC-TR-73-373, AD 775740.

38. "Reliability Study of Polyimide/Glass Multilayer Boards", RADC-TR-73-400, AD 77194.

39. "Infrared Testing of Multilayer Boards", RADC-TR-74-88, AD 780550.

40. "Laser Reliability Prediction", RADC-TR-75-210, AD A016437.

41. "Reliability Model for Miniature Blower Motors Per MIL-B-23071B", RADC-TR-75-178, AD A013735.

42. "Reliability Investigation of the MSC 2010 Transistors", ECOM-0092-F-72, AD B000815L.

43. "Reliability Investigations of the MSC 1330A and MSC 1330B Microwave Power Transistors", AD 923318L.

44. "RCA TA8694 and TA8777 Microwave Power Transistor Reliability Investigation", AD A007587.

45. "Reliability Prediction for Microwave Transistors", RADC-TR-74-313, AD A003643.

46. "Reliability Study of Microwave Power Transistors, RADC-TR-75-18, AD A007788.

47. "RADC Nonelectronic Reliability Notebook, Revised", RADC-TR-75-22, AD A005657.

48. "Reliability/Design: Thermal Applications", MIL-HDBK-251, 19 January 1978.

49. "Development of Failure Rate Models for Semiconductor Optoelectronic Devices", FAA-RD-76-134, AD A029163.

50. "High Power Microwave Tube Reliability Study", FAA-RD-76-172, AD A033612.

$I_{Z(MAX)}$ = maximum rated zener current at T_S

C.F. = stress correction factor per (8) below

(4) Group VII Microwave Mixer Diodes

$$S = \frac{\text{Operating Spike Leakage (ergs)}}{\text{Rated Burnout Energy at 25 degrees C.}}$$

(5) Group VII Microwave Detector Diodes

$$S = \frac{P_{OP} \text{ (Operating Power Dissipation)}}{P_{MAX} \text{ (Rated Power at 25 degrees C.)}}$$

(6) Group VIII Varactor, Step Recover, and Tunnel Diodes.

$$S = \frac{P_{OP}}{P_{MAX}} \text{ (C.F.)}$$

where:

P_{OP} = actual power dissipated

P_{MAX} = maximum rated power at T_S

C.F. = stress correction factor per (8) below

(7) Group X Opto-electronic Semiconductor Devices.

$$S = \frac{I_{OP}}{I_{MAX}} \text{ (C.F.)} \quad \text{or } S = \frac{P_{OP}}{P_{MAX}} \text{ (C.F.)}$$

$$= \frac{20}{80}(0.75) = 0.1875$$

where:

I_{OP} = operating average forward current

I_{MAX} = maximum rated average forward current at T_S

P_{OP} = actual power dissipated

P_{MAX} = maximum rated power at T_S

C.F. = stress correction factor per (9) below.

(8) Stress Correction Factor (C.F.) and temperature corrections for Silicon Devices.

a. Devices with T_S = 25 degrees C & T_{MAX} = 175 degrees C to 200 degrees C.

$$C.F. = 1$$

b. Devices with T_S >25 degrees C & T_{MAX} = 175 degrees C to 200 degrees C.

$$C.F. = \frac{175 - T_S}{150}$$

c. Devices with T_S = 25 degrees C & T_{MAX} <175 degrees C.

$$C.F. = \frac{T_{MAX} - 25}{150}$$

and enter λ_b table with $T = T_A + (175 - T_{MAX})$

or $T = T_C + (175 - T_{MAX})$

d. Devices with T_S >25 degrees C & T_{MAX} <175 degrees C.

$$C.F. = \frac{T_{MAX} - T_S}{150}$$

and enter λ_b table with $T = T_A + (175 - T_{MAX})$

or $T = T_C + (175 - T_{MAX})$

(9) Stress Correction Factor (C.F.) and temperature correction for Opto-electronic Devices. For devices with $T_S \geq 25^oC$. or $T_{MAX} \leq 125^oC$., or both,

$$C.F. = \frac{T_{MAX} - T_S}{100} = \frac{100-25}{100} = 0.75$$

and enter λ_b table with $T = T_A + (125 - T_{MAX}) = 35 + (125-100) = 60$

or $T = T_C + (125 - T_{MAX})$

2.2.11 INSTRUCTIONS FOR USE OF SEMICONDUCTOR MODELS

2.2.11.1 Device Ratings

Transistors are normally rated at maximum power dissipation and diodes at maximum current permissible. Usually each device is given two temperature rating points:

1 T_{MAX} - Maximum permissible junction temperature.

2 T_S - Maximum ambient or case temperature at which 100 percent of the rated load can be dissipated without causing the specified maximum junction temperature to be exceeded. (Case temperatures are given primarily for power devices used on heat sinks.)

As the ambient or case temperature rises above the T_S value, the internal temperature rise (i.e., the power load) must be decreased so that the T_{MAX} is not exceeded. This is illustrated in Figure 2.2.11-1.

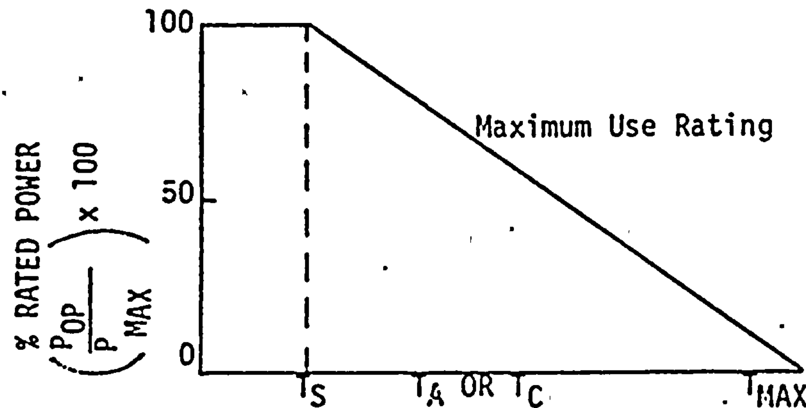


FIGURE 2.2.11-1. Conventional Derating Curve

Note:

T_S = temperature at which derating begins

T_{MAX} = maximum rated junction temperature

T_A = ambient temperature

T_C = case temperature

only to have the equipment production procedures damage the parts or introduce latent defects. Total equipment program descriptions as they might vary with different part quality mixes is beyond the scope of this Handbook. Reliability management and quality control procedures are described in other DOD standards and publications. Nevertheless, when a proposed equipment development is pushing the state-of-the-art and has a high reliability requirement necessitating high quality parts, the total equipment program should be given careful scrutiny and not just the parts quality. Otherwise, the low failure rates as predicted by the models for high quality parts will not be valid.

c. Use Environment.

All part reliability models include the effects of environmental stresses through the factor, π_E. The definitions of these environments are shown in Table 2-3. The π_E factor is quantified within each part failure rate model. These environments encompass the major areas of equipment use. Some equipment may experience more than one environment during its normal use, e.g., equipment in spacecraft. In such a case, the reliability analysis should be segmented, namely, missile launch (M_L) conditions during boost and return from orbit, and space flight (S_F) while in orbit.

TABLE 2-3
ENVIRONMENTAL SYMBOL IDENTIFICATION AND DESCRIPTION

ENVIRONMENT	π_E SYMBOL	NOMINAL ENVIRONMENTAL CONDITIONS
Ground, Benign	G_B	Nearly zero environmental stress with optimum engineering operation and maintenance.
Space, Flight	S_F	Earth orbital. Approaches Ground, Benign conditions without access for maintenance. Vehicle neither under powered flight nor in atmospheric re-entry.
Ground, Fixed	G_F	Conditions less than ideal to include installation in permanent racks with adequate cooling air, maintenance by military personnel and possible installation in unheated buildings.
Ground, Mobile	G_M	Conditions more severe than those for G_F, mostly for vibration and shock. Cooling air supply may also be more limited, and maintenance less uniform.

ENVIRONMENT	π_E SYMBOL	NOMINAL ENVIRONMENTAL CONDITIONS
Naval, Sheltered	N_S	Surface ship conditions similar to G_F but subject to occasional high shock and vibration.
Naval, Unsheltered	N_U	Nominal surface shipborne conditions but with repetitive high levels of shock and vibration.
Airborne, Inhabited, Transport	A_{IT}	Typical conditions in transport or bomber compartments occupied by aircrew without environmental extremes of pressure, temperature, shock and vibration, and installed on long mission aircraft such as transports and bombers.
Airborne, Inhabited Fighter	A_{IF}	Same as A_{IT} but installed on high performance aircraft such as fighters and intercepters.
Airborne, Uninhabited, Transport	A_{UT}	Bomb bay, equipment bay, tail, or wing installations where extreme pressure, vibration, and temperature cycling may be aggravated by contamination from oil, hydraulic fluid and engine exhaust. Installed on long mission aircraft such as transports and bombers.
Airborne, Uninhabited, Fighter	A_{UF}	Same as A_{UT} but installed on high performance aircraft such as fighters and intercepters.
Missile, Launch	M_L	Severe conditions of noise, vibration, and other environments related to missile launch, and space vehicle boost into orbit, vehicle re-entry and landing by parachute. Conditions may also apply to installation near main rocket engines during launch operations.

d. Part Failure Rate Models.

Part failure rate models for microelectronic parts are significantly different form those for other parts and are presented entirely in Section 2.1. Another type of model is used on most other parts; a typical example is the following one for discrete semiconductors:

SOLID STATE

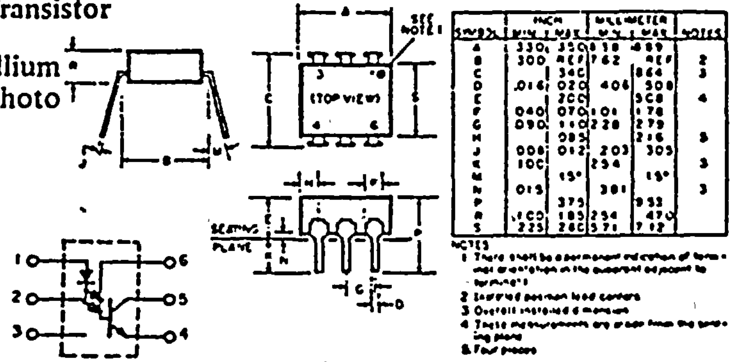
GENERAL ELECTRIC

OPTOELECTRONICS

Photon Coupled Isolator 4N38-4N38A

Ga As Infrared Emitting Diode & NPN Silicon Photo-Transistor

The General Electric 4N38 and 4N38A consist of a gallium arsenide infrared emitting diode coupled with a silicon photo transistor in a dual in-line package.



FEATURES:

- Fast switching speeds
- High DC current transfer ratio
- High isolation resistance
- 2500 volts isolation voltage
- I/O compatible with integrated circuits

†Indicates JEDEC registered values

absolute maximum ratings: (25°C) (unless otherwise specified)

†Storage Temperature -55 to 150°C. Operating Temperature -55 to 100°C. Lead Soldering Time (at 260°C) 10 seconds.

INFRARED EMITTING DIODE			PHOTO-TRANSISTOR		
†Power Dissipation	*150	milliwatts	†Power Dissipation	**150	milliwatts
†Forward Current (Continuous)	80	milliamps	†V_{CEO}	80	volts
†Forward Current (Peak) (Pulse width 300μsec, 2% duty cycle)	3	ampere	†V_{CBO}	80	volts
†Reverse Voltage	3	volts	†V_{ECO}	7	volts
			Collector Current (Continuous)	100	milliamps
*Derate 2.0 mW/°C above 25°C ambient.			**Derate 2.0 mW/°C above 25°C ambient.		

†Total device dissipation @ T_A = 25°C. P_D 250 mW. †Derate 3.3 mW/°C above 25°C ambient.

individual electrical characteristics (25°C)

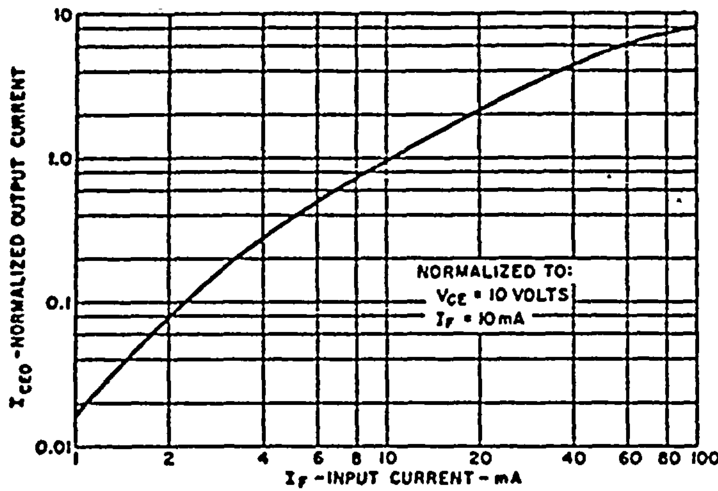
INFRARED EMITTING DIODE	TYP.	MAX.	UNITS
†Forward Voltage (I_F = 10mA)	1.2	1.5	volts
†Reverse Current (V_R = 3V)	–	100	microamps
Capacitance V = 0, f = 1 MHz	50	–	picofarads

PHOTO-TRANSISTOR	MIN.	TYP.	MAX.	UNITS
†Breakdown Voltage – $V_{(BR)CEO}$ (I_C = 1mA, I_F = 0)	80	–	–	volts
†Breakdown Voltage – $V_{(BR)CBO}$ (I_C = 1μA, I_F = 0)	80	–	–	volts
†Breakdown Voltage – $V_{(BR)ECO}$ (I_E = 100μA, I_F = 0)	7	–	–	volts
†Collector Dark Current – I_{CEO} (V_{CE} = 60V, I_F = 0)	–	–	50	nanoamps
†Collector Dark Current – I_{CBO} (V_{CE} = 60V, I_F = 0)	–	–	20	nanoamps

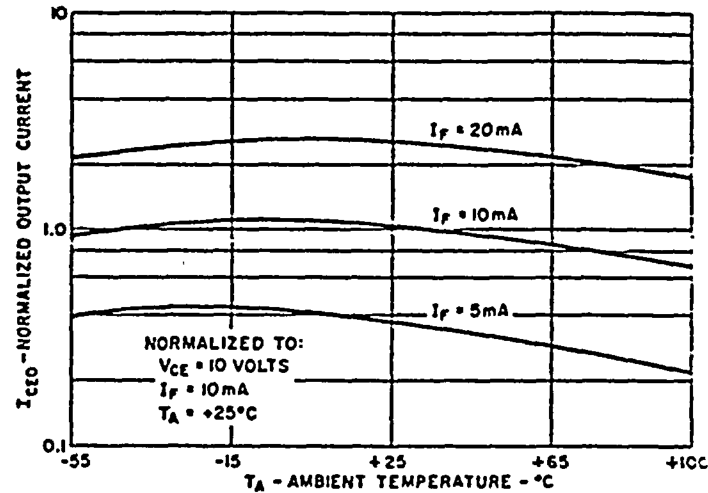
coupled electrical characteristics (25°C)

		MIN.	TYP.	MAX.	UNITS
†Isolation Voltage 60Hz with the input terminals (diode) shorted together and the output terminals (transistor) shorted together.	4N38	1500	–	–	volts (peak)
	4N38A	2500	–	–	volts (peak)
	4N38A	1775	–	–	volts (RMS) (1 sec.)
†Saturation Voltage – Collector – Emitter (I_F = 20mA, I_C = 4mA)		–	–	1.0	volts
Resistance – IRED to Photo-Transistor (@ 500 volts)		–	100	–	gigaohms
Capacitance – IRED to Photo-Transistor (@ 0 volts, f = 1 MHz)		–	1	–	picofarad
DC Current Transfer Ration (I_F = 10mA, V_{CE} = 10V)		10		–	%
Switching Speeds (V_{CE} = 10V, I_C = 2mA, R_L = 100Ω)					
Turn-On Time – t_{on}		–	5	–	microseconds
Turn-Off Time – t_{off}		–	5	–	microseconds

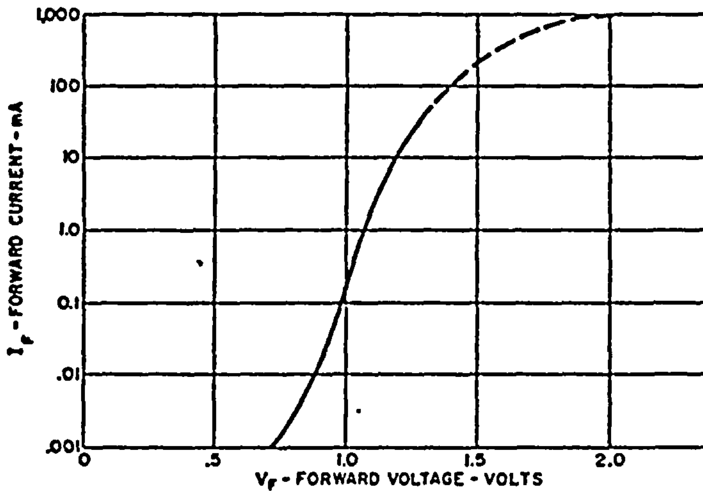
TYPICAL CHARACTERISTICS



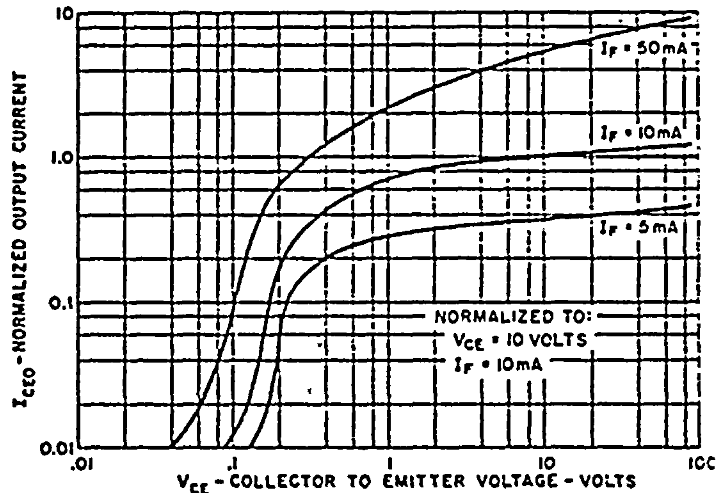
1. OUTPUT CURRENT VS INPUT CURRENT



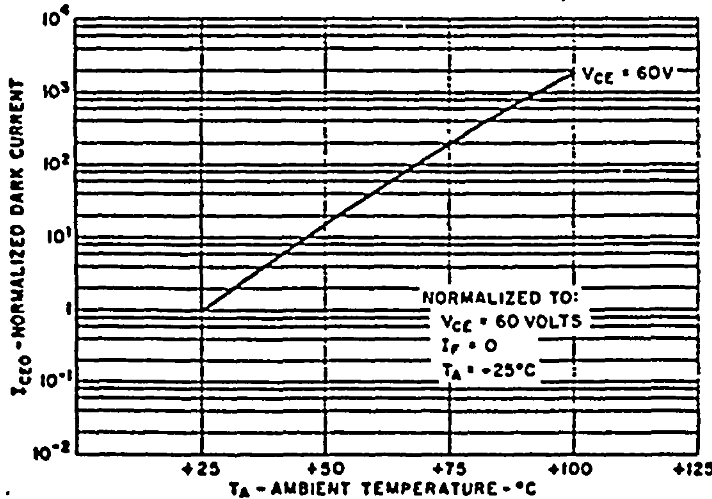
2. OUTPUT CURRENT VS TEMPERATURE



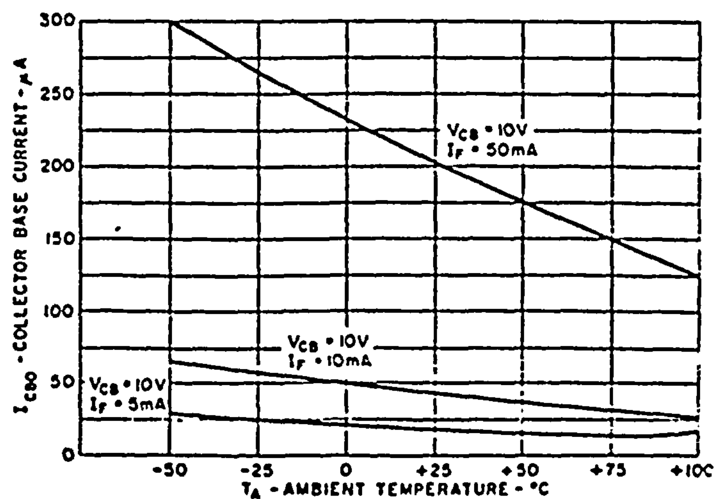
3. INPUT CHARACTERISTICS



4. OUTPUT CHARACTERISTICS



5. NORMALIZED DARK CURRENT VS TEMPERATURE



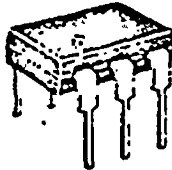
6. COLLECTOR BASE CURRENT VS TEMPERATURE

Optical Couplers/Isolators

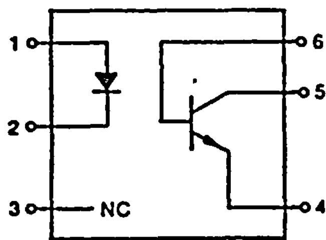
Couplers are designed to provide isolation protection from high-voltage transients, surge voltage, or low-level noise that would otherwise damage the input or generate erroneous information. They allow interfacing systems of different logic levels, different grounds, etc., that would otherwise be incompatible. Motorola couplers are tested and specified to an isolation voltage of 7500 Vac peak.

Motorola offers a wide array of standard devices with a wide range of specifications (including the first series of DIP transistors and Darlington couplers to achieve JEDEC registration: transistors — 4N25 thru 4N38, and Darlingtons — 4N29 thru 4N33). All Motorola couplers are UL Recognized with File Number E54915.

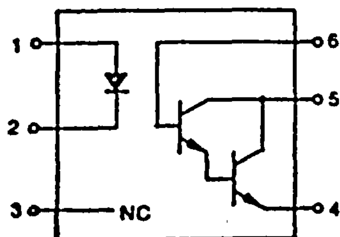
CASE 730A



The Transistor Coupler is probably the most popular form of isolator since it offers moderate speed (approximately 300 kHz), sensitivity and economy. In addition, the collector-base junction can be used as a photodiode to achieve higher speeds. The output in the diode mode is lower, requiring amplification for more usable output levels.



The Darlington Transistor Coupler is used when high transfer ratios and increased output current capability are needed. The speed, approximately 30 kHz, is slower than the transistor type but the transfer ratio can be as much as ten times as high as the single transistor type.



Transistor Output

Isolation Voltage is 7500 V (Min) on all devices. See notes.

Device Type	DC Current Transfer Ratio % Min	$V_{(BR)CEO}$ Volts Min
TIL112	2.0	20
TIL115	2.0	20
IL15	6.0	30
MCT26	6.0	30
TIL111	8.0	30
TIL114	8.0	30
IL12	10	20
MOC1006	10	30
4N27	10	30
4N28	10	30
H11A4	10	30
TIL124	10	30
TIL153	10	30
IL74	12.5	20
MOC1005	20	30
TIL125	20	30
TIL154	20	30
4N25	20	30
4N26	20	30
H11A2	20	30
H11A3	20	30
H11A520	20	30
IL1	20	30
MCT2	20	30
TIL116	20	30
4N38	20	80
H11A5	30	30
MCT271	45	30
H11A1	50	30
H11A550	50	30
TIL117	50	30
TIL126	50	30
TIL155	50	30
CNY17	62	70
MCT275	70	80
MCT272	75	30
MCT277	100	30
4N35	100	30
4N36	100	30
4N37	100	30
H11A5100	100	30
MCT273	125	30
MCT274	225	30

Darlington Output

Isolation Voltage is 7500 V (Min) on all devices. See notes.

Device Type	DC Current Transfer Ratio % Min	$V_{(BR)CEO}$ Volts Min
4N31	50	30
H11B3	100	25
4N29	100	30
4N30	100	30
MCA230	100	30
H11B255	100	55
MCA255	100	55
H11B2	200	25
MCA231	200	30
MOC119*	300	30
TIL119*	300	30
TIL113	300	30
MOC8030*	300	80
TIL127	300	30
TIL128*	300	30
TIL156	300	30
TIL157*	300	30
H11B1	500	25
4N32	500	30
4N33	500	30
MOC8020*	500	50
MOC8050*	500	80
MOC8021*	1000	50

* Pin 3 and Pin 6 are not connected

Notes:

1. Isolation Surge Voltage, V_{ISO}, is an internal device dielectric breakdown rating. For this test LED pins 1 and 2 are common and phototransistor pins 4, 5, and 6 are common.
2. All Motorola couplers are specified at 7500 Vac peak (5 seconds). This usually exceeds the originator's specification and JEDEC registered values.

ATTACHMENT B
EXCERPTS FROM: REGARDING CTR (LIGHT OUTPUT), DEGRADATION WITH OPERATING TIME

General Electric Optoelectronics Manual

By: W.H. Sahm

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SEMICONDUCTOR PRODUCTS DEPARTMENT

B. RELIABILITY PREDICTION OF CIRCUITS CONTAINING IRED's

Previously the IRED phenomena of light output decrease, as the time current flows through it, was mentioned. This presents a dilemma to the circuit designer attempting to provide adequate margins for bias values unless he can predict what minimum value of light output, from the IRED, he can expect at the end of the design life of his equipment. Based on the results of tests performed at G.E. and at customer's facilities (who were kind enough to furnish us test data and summaries) the G.E. Application Engineering Center has developed design guidelines to allow the prediction of the approximate worst case, end of life, IRED performance. The basis of the prediction is the observed behavior of the ratio of light output after operation to the initial value of light output. It also is based on the observation that all devices do not behave identically in this ratio in time, but that a distribution with identifiable tenth, fiftieth (median) and ninetieth percentile points exists at any time the ratio is calculated. Use of this tenth percentile ratio (90% of the devices are better than this) and the distribution of light output (or CTR for couplers) above the specified minimum value allows the product of specified minimum light output and tenth percentile ratio, predicted at end of life, to be used as a reasonable approximation of minimum

SUMMARY OF TESTS USED TO OBTAIN IRED DESIGN GUIDE LINES

I_{FS} \ T_A	25°C	40°C	55°C	70°C	80°C	100°C
3mA	20 1000 Hr. 3mA					
5mA	20 1000 Hr. 1, 5mA					
10mA	16 1000 Hr. 1, 10mA					
20mA	27 500, 1000 Hr. 1, 5, 10, 20mA				108 1000 Hr. 10mA	
25mA	20 1500 Hr. 10mA	20 1500 Hr. 10mA	20 1500 Hr. 10mA	60 1500 Hr. 10mA		
50mA		20 1500 Hr. 10mA		40 1500 Hr. 10mA		
60mA	20 1000 Hr. 1, 5, 10, 20, 60mA				163 1000, 3000, 5000 Hr. 10mA	
75mA				20 1500 Hr. 10mA		
100mA	79 1K, 15K, 30K Hr. 1, 10, 100mA					90 168, 1500 Hr. 1, 10, 100mA

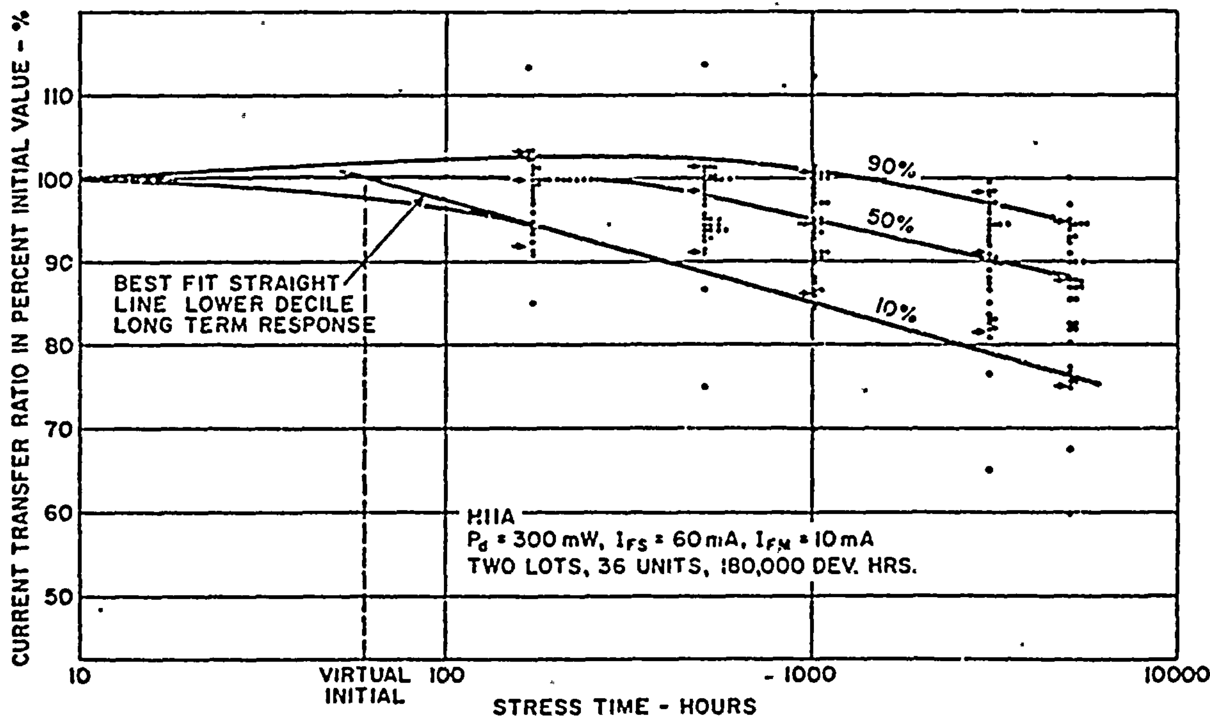
This chart represents about 2.0 million device hours of operation on 625 dual in-line optocouplers and 111 hermetic IRED's.

FORMAT OF DATA PRESENTATION:

SAMPLE SIZE TEST DURATION I_{FM} CURRENT

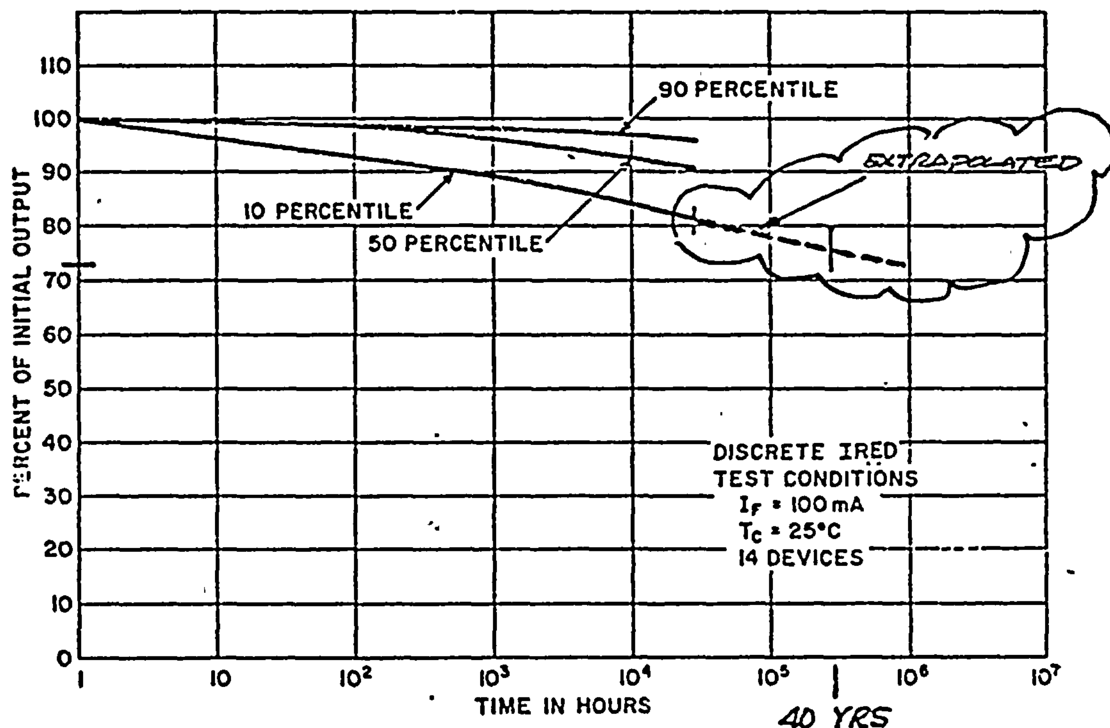
end of life value. Although this does not represent the worst possible case, no correlation can be found between initial light output and rate of decrease in light output, and so the percentage of devices expected to be less than the guideline derived number approaches zero. These guidelines, as can be noted, are based on fair sample sizes, although both larger samples than these and greater precision, higher resolution, measurements could provide better fits. To make the guideline development less obscure, the discussion will trace the steps followed in defining these design guidelines and, in the process, develop the guidelines.

When the percent of initial value of light output (or current transfer ratio in couplers) of an IRED on an operating life test, is plotted against the time the IRED has been operated, two phenomena become apparent. The long-term behavior is found to be a straight line when the ratio is plotted on a logarithmic time scale. The short-term behavior is found to have a much shallower slope, on the same plot, than the long-term behavior. This effect is illustrated by the fact that the long-term straight line can be extrapolated back towards zero and will usually intersect the initial value line at a time between 10 and 100 hours. These properties combine to allow the response to be described by a "virtual initial time" and the slope of the line passing through that time point. This had been recognized in other work. The problems with predicting response are the variety of test conditions at which both stress and measurement data have been taken, and the spread of data at the readout points. It was recognized that the fall in light output was accelerated by either stressing the IRED harder, i.e., at a higher current (I_{FS}) and/or temperature, or by monitoring the test results at lower current (I_{FM}) levels. Precise acceleration factors have yet to be determined due to lot-to-lot variability. Fortunately, circuit design purposes can be served by a less precise model, which only attempts to serve the requirements of circuit design. For this approach, as mentioned before, we pay attention to the lower decile of the distribution and its change in time.



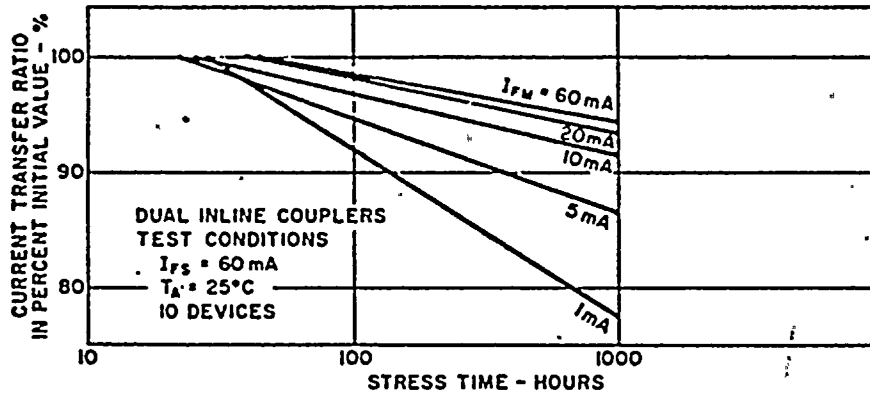
LIFE TEST RESULTS – ILLUSTRATING OBSERVED CHANGE IN IRED OUTPUT WITH OPERATING TIME

The question naturally arises of the applicability of this description to time periods beyond the one and five thousand hour times that the majority of the tests stopped at. Fortunately, tests have been completed on discrete IRED's for 30,000 hours. The results of these tests indicate that nothing unexpected happens at extremely long times, as can be seen above. This is reinforcing evidence indicating the superiority of the G.E. silicon doped, liquid phase epitaxially grown IRED. grown IRED.

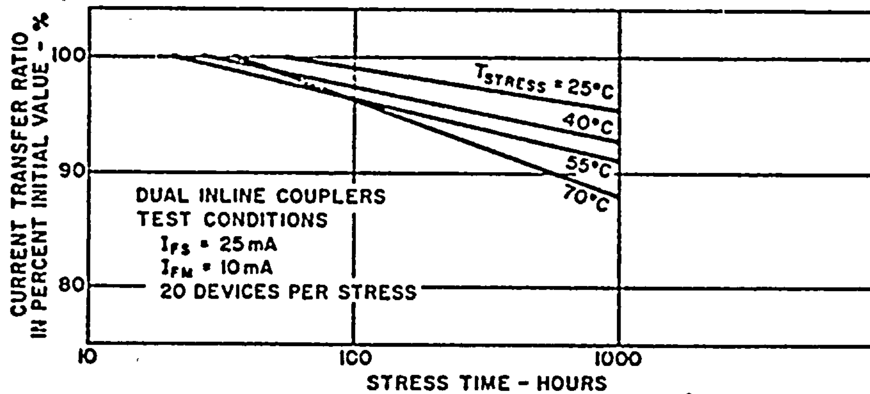


LONG-TERM IRED LIFE TEST RESULTS

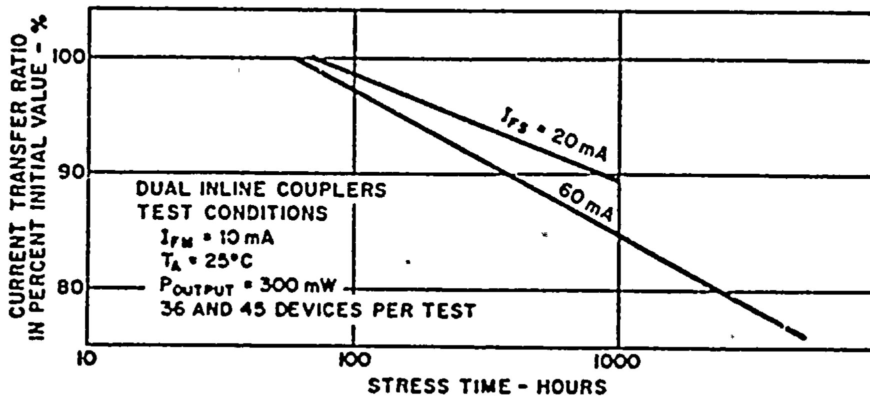
Plotting the response (best straight line) of various test conditions on a single graph, the acceleration due to raising stress current (I_{FS}) is easily seen. Higher temperatures during stress cause the same effect, and can be accomplished by raising the ambient or by self-heating (in a coupler by dissipating power in the output device). Lowering the current at which the IRED light output is monitored, (I_{FM}) also accelerates the phenomena, but in looking at many test results, it appears that the ratio of I_{FS}/I_{FM} is the key factor affecting the slope besides temperature.



EFFECT OF
MEASUREMENT CURRENT
ON SLOPE



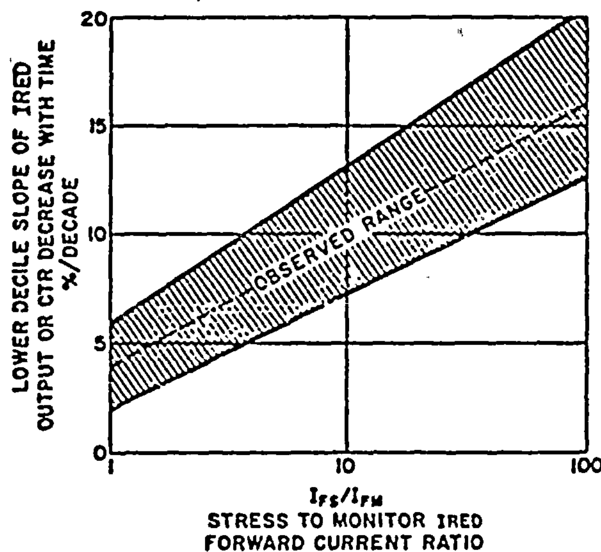
EFFECT OF
STRESS TEMPERATURE
ON SLOPE



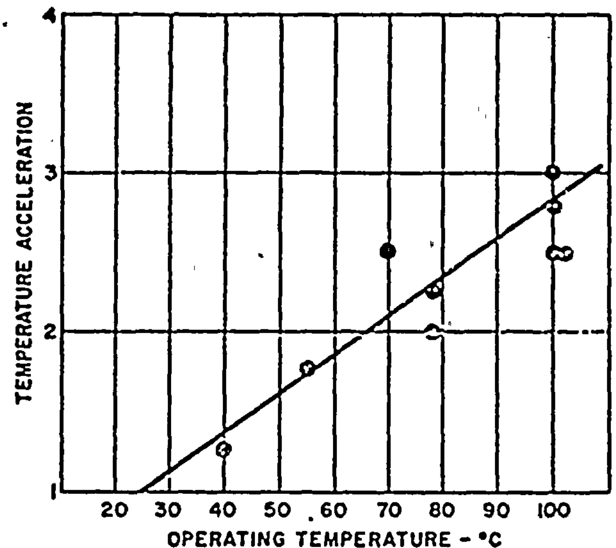
EFFECT OF
STRESS CURRENT
ON SLOPE

When the temperature effect is plotted as an acceleration vs. temperature, a fair straight line fit is found, as illustrated below. This temperature acceleration factor represents the ratios of the slopes of the lower decile lines of various temperature stresses. The fit is not perfect, but is good enough to be useful. It contains both discrete IRED data (LED55 series) and optocoupler data (H11 series) and appears to fit both equally.

With this, and the determination of the coupled thermal resistance in the optocoupler (i.e., the heating factor for the IRED from power dissipated in the output device), it was attempted to fit the I_{FS}/I_{FM} ratio into the model. After many attempts to find models which fit various phenomena better, and the generation of additional data to try to fill holes, it was decided that two factors contributed to the inability of defining a tight fit single line. These are lot-to-lot and sampling variability and the precision (and volume) of data required to find the slope at low I_{FS}/I_{FM} ratios and low temperatures. These factors cause the best model found to enclose a band of observed values, as can be seen.



Bias Current Effect



Temperature Effect

IRED OUTPUT VS. TIME SLOPE PREDICTION CURVES ASSUMING A VIRTUAL INITIAL TIME OF 50 HOURS

To use this data the circuit designer must define a desired lifetime, the degree of control he has on minimum and maximum values of I_F in any single socket, and the temperature environment to which the circuit is exposed.

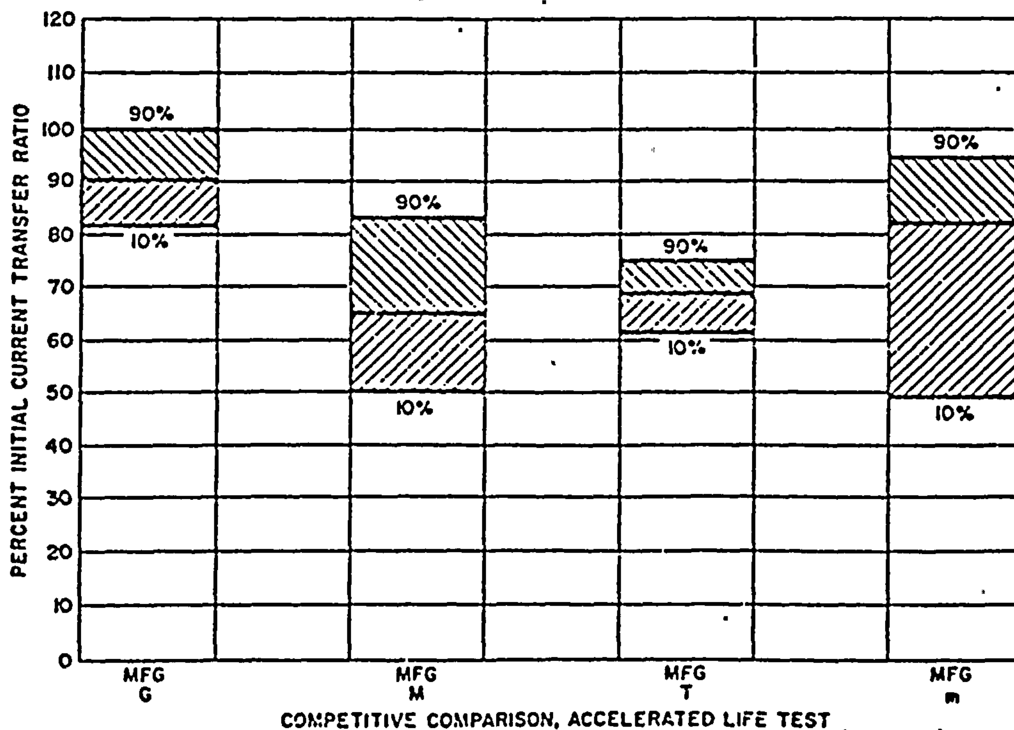
A simple example of the design procedure illustrates its use. Assume the need for an 4N35 which will provide 10 mA of output current at 5 Volts V_{CE} after 100,000 hours of 55°C operation. To find the IRED current needed to provide this, we need the minimum specified CTR of the 4N35, the estimated slope of the lower decile of light output vs. time and the temperature acceleration of that slope at 55°C. The 4N35 specification indicates a minimum CTR of 100%, that for I_F values of up to 20 mA the CTR is relatively constant and that at 55°C the CTR will be about 0.85 times its 25°C value $\left(\frac{\Delta CTR}{\Delta T}\right)$. The center of the range of slopes vs. I_{FS}/I_{FM} is conservatively chosen at a ratio of 1.3 and found to be 5% per decade (slope). This should provide a reasonably worst case approximation of both coupler performance and possible current variation

effects due to power supply and bias circuit drifts. The temperature acceleration factor curve indicates this slope will be increased by 1.75 times at 55°C (A_T), i.e., the slope will be 8.8%/ decade. The difference between 50 hours and 100,000 hours (t) is 3.3 decades (log 100,000 – log 50), so the expected lower decile will provide about 29% less light at 100,000 hours than initially. To provide the 10 mA output requirement, the IRED current must be raised by about 40% to compensate for light lessening with operation [i.e., $\frac{100}{100-29}$.] and this must be raised by 18% (i.e., 1/.85) to compensate temperature variation of CTR, yielding a minimum input current to the IRED of 16.6 mA, as compared to the 10 mA required initially at 25°C. The formula used in this example is:

$$I_F = \frac{100}{100 - [\text{slope} \times A_T \times \log(t/50)]} \times \frac{1}{\Delta CTR/\Delta T} \times \frac{I_C}{CTR}$$

where: A_T is the temperature acceleration for slope at the expected operating temperature,
CTR is the specified minimum current transfer ration,
$\Delta CTR/\Delta T$ is the change in CTR due to temperature,
I_C is the required output current,
I_F is the required IRED bias current,
Slope is the light output lessening per decade time, and
t is the circuit design life.

Note that for a one million hour life the required IRED current would only rise to 18.5 mA, as time has only increased by another decade! The estimate of the effect of operating time on the circuit has been almost as simple as the estimate of temperature effects.



COMPETITIVE COMPARISON, ACCELERATED LIFE TEST

ATTACHMENT C

EXCERPTS FROM: GENERAL ELECTRIC OPTOELECTRONICS MANUAL →
REFERENCING OPTOCOUPLER ISOLATION PARAMETER MEASUREMENT

non-light sensitive devices, except for the light sensitive parameters. Such techniques are described in the *General Electric Transistor Manual* and the *General Electric SCR Manual*, and will not be detailed here. The most common problem encountered is the leakage current measurement with the base open, as I_{CEO} is rarely measured on normal transistors, and understanding the need for considering dynamic effects and ambient light effects will solve the problem.* Dynamic effects must be considered, because the open base has no path but junction leakage to charge the junction capacitances. If the common high source impedance bias circuit for leakage current is used, the gain of the transistor multiplies the junction capacitance, of the collector base photodiode (≈ 25 pF), and provides a long stabilization time constant. Note the "double barreled" effect of source impedance in that it is the resistance in the RC time constant and also is the load resistor that determines voltage gain ($A_v \approx 1/hie \cdot R_L \cdot hFE$). These effects indicate I_{CEO} should be measured by application of the bias voltage from a low impedance supply until junction capacitances are charged (now determined by the base emitter diode impedance), which can take up to 100 msec, (with no external capacitances, switches, sockets, coaxial, etc. connected to the base) in a darlington. After junction capacitance is charged, the current measuring resistor is introduced to the circuit by removing the short across it. The charge balance at the base can be affected by the motion of conductive objects in the area, so best reproducibility will be obtained within an electrostatic shield. The electrostatic shield can also serve the purpose of shielding the detector from ambient light, the effects of which are obvious on a leakage current measurement.

Measurement of the light parameters of a phototransistor requires a light source of known intensity and spectral characteristics. Lamps with known spectral characteristics, i.e., calibrated standards, are available and, in conjunction with a thermo pile or calibrated photo cell and a solid mechanical positioning system, can be the basis of an opto measuring system. Some relatively simple systems based on the response of a silicon photo cell are available, but the assumption that all silicon devices have identical spectral response is implicit in their use for optical measurements. As different devices have different response curves, the absolute accuracy of these devices is impaired, although excellent comparative measurements can be made. Another method which has fair accuracy is the use of a calibrated detector, L9UX4 for the photo SCR's or L14H special for the phototransistors, to adjust the light source to the desired level. This will eliminate spectral problems as the calibrated device has an identical spectral response to the devices being measured. Accuracy will then depend on basic equipment accuracies, ambient control and mechanical position reproducibility.

Spectral response measurements require use of precision filters or a precision monochromator and a calibrated photo cell or thermo pile. As in the case of the IRED, it is recommended that these measurements be done by a laboratory specializing in optical measurements.

→ C. Optocoupler Measurements

The measurement of the individual devices in the optocoupler is identical to the measurement of a discrete diode and a discrete device of the type of detector being considered, and is covered previously. The measurement of isolation and transfer characteristics are not as obvious, and will be illustrated.

1. Isolation Parameters are always measured with the terminals of each device of the coupler shorted. This prevents the high capacitive charging currents, caused by the high dv/dt's applied during the measurement, from damaging either device. Safety precautions must be observed in these tests due to the very high voltages present!

a). Isolation voltage is measured as illustrated below. Normally the surge voltage capability is measured, and, unless the high voltage power supply has a fast shutdown (<0.5 μsec), the device under test will be destroyed if its isolation voltage capability is less than the high voltage supply

*see "Avoid I_{CEO} measurements", Hendriks.

** ALSO INCLUDED ARE DATA SHEETS FOR THE REFERENCED 4N38A OPTO-COUPLER DEVICES.

The design guideline, unfortunately, is only valid for the G.E. IRED's and DIP couplers. Life tests of competitive units at both maximum rating and accelerated test conditions indicate a wide variation of performance exists in the industry. The accelerated test results were duplicated by the maximum rating test results, indicating the same type of response in both the A_T and I_{FS}/I_{FM} curves. But the magnitude of shifts observed, especially the lower decile, are much greater, indicating much greater slopes, in percent per decade, of the light output vs. operating time graphs. This is illustrated in the plots comparing the life test results given above. To life cycle design with such devices would require derivation of a different model, based on a matrix of life tests. Based on extremely limited testing and some published information, it appears that at least two other manufacturers of IRED's and optocouplers can achieve light output performance with operation similar to the G.E. performance. Neither utilizes the glass dielectric in the coupler and no tests have been performed to allow comment on other reliability factors.

Degradation failure rates, to a desired criteria of percent initial light output, may be calculated from accelerated data to use condition response by use of the design guideline. The design guideline temperature acceleration and slope per decade factors may be used to calculate an equivalent number of test hours at use condition to the accelerated test. Note that early hour slope of light output vs. time is very shallow, and accelerated test results are not valid for operating times under 168 hours. The number of devices which decrease in light output to a value less than the desired criteria on the accelerated test is then used with the equivalent unit hours to estimate failure rate. While this is not strictly accurate, due to the distribution of change in light output, the following is a useful approximation:

$$t_x = 10^{\left[\left(\log \frac{t_o}{50}\right) \times \frac{A_{T1}}{A_{T2}} \times A_I + \log 50\right]}$$

where: A_I is the slope at stress conditions ÷ slope at use conditions,
A_{T1} is the temperature acceleration at stress conditions,
A_{T2} is the temperature acceleration at use conditions,
t_o is the stress test duration, and
t_x is the equivalent time at use conditions.

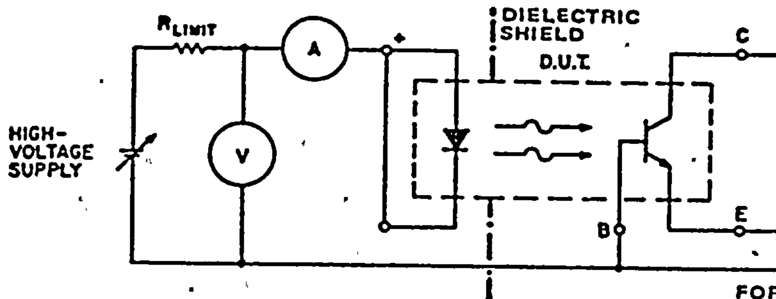
The reliability test summary degradation failure rates were calculated this way and provide an example.

The 100°C, 100 mA phototransistor accelerated operating life tests run for 168 hours (t_o). The temperature acceleration curve gives a $\frac{A_{T1}}{A_{T2}}$ ratio of the slope per decade at 100°C to the 55°C value of $\frac{2.83}{1.75}=1.62$. The middle line of the I_{FS}/I_{FM} curve gives a ratio of $\frac{10}{4}=2.5$ for the slopes of a 10 mA/10 mA I_{FS}/I_{FM} compared to the 100 mA/10 mA I_{FS}/I_{FM} the test was run at. The equivalent hours for this test at a 55°C use condition is:

$$t_x = 10^{\left[\left(\log \frac{168}{50}\right) \times (1.62) \times (2.5) + \log 50\right]}$$

$$= 6770 \text{ hours.}$$

Two units of the 325 tested failed a light output criteria of half the initial value, giving a 2/2,200,000 device hours observed failure rate, which at the 50% UCL is the 0.12% per thousand hour failure rate shown in the summary chart. This also illustrates that for the G.E. IRED and coupler, the decrease in light output should have a minimal effect on circuit failure rate in conservatively designed circuits.

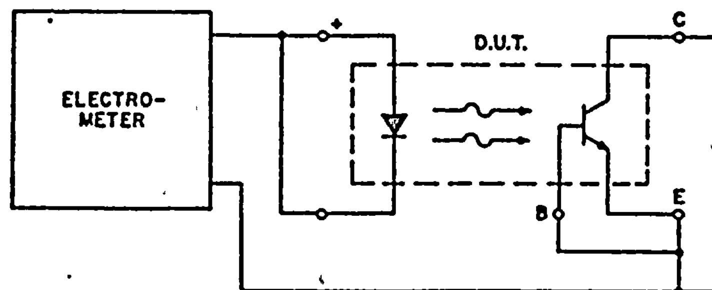


FOR VOLTAGES OVER 2500 Vrms, THE DIELECTRIC SHIELD IS RECOMMENDED TO ELIMINATE AIR GAP EFFECTS.

ISOLATION VOLTAGE TEST

is set at. Crowbar techniques may be used in lab set-ups to provide rapid turn-off and forestall the test being described as "destructive." Steady-state isolation voltage is usually specified as a fixed percentage of the measured surge capability, although limited life tests indicate this derating is not required for the G.E. glass dielectric isolation. Application Engineering believes conservative design practices are required in the use of isolation voltage ratings, due to the transients normally observed when line voltages are monitored and the catastrophic effects of a failure.

b). Isolation resistance is measured at voltages far below the surge isolation capability, and has less potential for damaging the device being tested. The test is illustrated schematically here,



MEASURING OF ISOLATION RESISTANCE

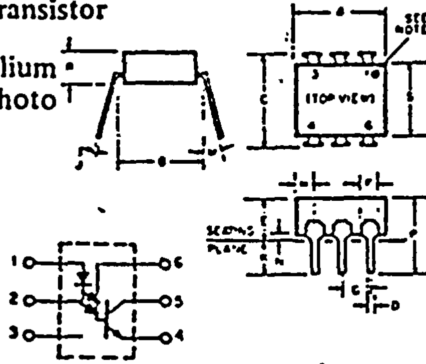
and requires the procedures normally used when measuring currents below a microampere.

c). Isolation capacitance is a straightforward capacitance measurement. The capacitance of couplers utilizing the G.E. patented glass dielectric process is quite independent of applied voltage

Photon Coupled Isolator 4N38-4N38A

Ga As Infrared Emitting Diode & NPN Silicon Photo-Transistor

The General Electric 4N38 and 4N38A consist of a gallium arsenide infrared emitting diode coupled with a silicon photo transistor in a dual in-line package.



FEATURES:

- Fast switching speeds
- High DC current transfer ratio
- High isolation resistance
- 2500 volts isolation voltage
- I/O compatible with integrated circuits

†Indicates JEDEC registered values

absolute maximum ratings: (25°C) (unless otherwise specified)

†Storage Temperature -55 to 150°C. Operating Temperature -55 to 100°C. Lead Soldering Time (at 260°C) 10 seconds.

INFRARED EMITTING DIODE		
†Power Dissipation	*150	milliwatts
†Forward Current (Continuous)	80	milliamps
†Forward Current (Peak) (Pulse width 300μsec, 2% duty cycle)	3	ampere
†Reverse Voltage	3	volts

*Derate 2.0 mW/°C above 25°C ambient.

PHOTO-TRANSISTOR		
†Power Dissipation	**150	milliwatts
†V_{CEO}	80	volts
†V_{CBO}	80	volts
†V_{ECO}	7	volts
Collector Current (Continuous)	100	milliamps

**Derate 2.0 mW/°C above 25°C ambient.

†Total device dissipation @ T_A = 25°C. P_D 250 mW.

†Derate 3.3 mW/°C above 25°C ambient.

individual electrical characteristics (25°C)

INFRARED EMITTING DIODE	TYP.	MAX.	UNITS
†Forward Voltage (I_F = 10mA)	1.2	1.5	volts
†Reverse Current (V_R = 3V)	–	100	microamps
Capacitance V = 0, f = 1 MHz	50	–	picofarads

PHOTO-TRANSISTOR	MIN.	TYP.	MAX.	UNITS
†Breakdown Voltage – $V_{(BR)CEO}$ (I_C = 1mA, I_F = 0)	80	–	–	volts
†Breakdown Voltage – $V_{(BR)CBO}$ (I_C = 1μA, I_F = 0)	80	–	–	volts
†Breakdown Voltage – $V_{(BR)ECO}$ (I_E = 100μA, I_F = 0)	7	–	–	volts
†Collector Dark Current – I_{CEO} (V_{CE} = 60V, I_F = 0)	–	–	50	nanoamps
†Collector Dark Current – I_{CBO} (V_{CE} = 60V, I_F = 0)	–	–	20	nanoamps

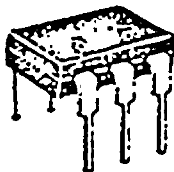
coupled electrical characteristics (25°C)

		MIN.	TYP.	MAX.	UNITS
†Isolation Voltage 60Hz with the input terminals (diode) shorted together and the output terminals (transistor) shorted together.	4N38	1500	–	–	volts (peak)
	4N38A	2500	–	–	volts (peak)
	4N38A	1775	–	–	volts (RMS) (1 sec.)
†Saturation Voltage – Collector – Emitter (I_F = 20mA, I_C = 4mA)		–	–	1.0	volts
Resistance – IRED to Photo-Transistor (@ 500 volts)		–	100	–	gigaohms
Capacitance – IRED to Photo-Transistor (@ 0 volts, f = 1 MHz)		–	1	–	picofarad
DC Current Transfer Ration (I_F = 10mA, V_{CE} = 10V)		10		–	%
Switching Speeds (V_{CE} = 10V, I_C = 2mA, R_L = 100Ω)					
Turn-On Time – t_{on}		–	5	–	microseconds
Turn-Off Time – t_{off}		–	5	–	microseconds

Optical Couplers/Isolators

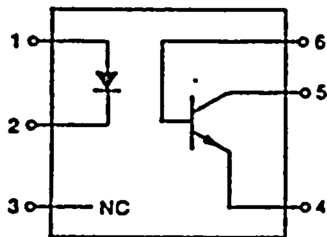
Couplers are designed to provide isolation protection from high-voltage transients, surge voltage, or low-level noise that would otherwise damage the input or generate erroneous information. They allow interfacing systems of different logic levels, different grounds, etc., that would otherwise be incompatible. Motorola couplers are tested and specified to an isolation voltage of 7500 Vac peak.

Motorola offers a wide array of standard devices with a wide range of specifications (including the first series of DIP transistors and Darlington couplers to achieve JEDEC registration: transistors — 4N25 thru 4N38, and Darlingtons — 4N29 thru 4N33). All Motorola couplers are UL Recognized with File Number E54915.

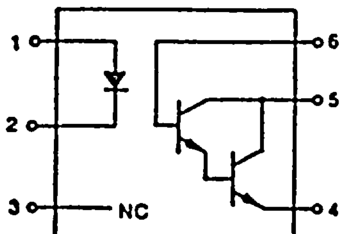


CASE 730A

The Transistor Coupler is probably the most popular form of isolator since it offers moderate speed (approximately 300 kHz), sensitivity and economy. In addition, the collector-base junction can be used as a photodiode to achieve higher speeds. The output in the diode mode is lower, requiring amplification for more usable output levels.



The Darlington Transistor Coupler is used when high transfer ratios and increased output current capability are needed. The speed, approximately 30 kHz, is slower than the transistor type but the transfer ratio can be as much as ten times as high as the single transistor type.



Transistor Output

Isolation Voltage is 7500 V (Min) on all devices. See notes.

Device Type	DC Current Transfer Ratio % Min	$V_{(BR)CEO}$ Volts Min
TIL112	2.0	20
TIL115	2.0	20
IL15	6.0	30
MCT26	6.0	30
TIL111	8.0	30
TIL114	8.0	30
IL12	10	20
MOC1006	10	30
4N27	10	30
4N28	10	30
H11A4	10	30
TIL124	10	30
TIL153	10	30
IL74	12.5	20
MOC1005	20	30
TIL125	20	30
TIL154	20	30
4N25	20	30
4N26	20	30
H11A2	20	30
H11A3	20	30
H11A520	20	30
IL1	20	30
MCT2	20	30
TIL116	20	30
4N38	20	80
H11A5	30	30
MCT271	45	30
H11A1	50	30
H11A550	50	30
TIL117	50	30
TIL126	50	30
TIL155	50	30
CNY17	62	70
MCT275	70	80
MCT272	75	30
MCT277	100	30
4N35	100	30
4N36	100	30
4N37	100	30
H11A5100	100	30
MCT273	125	30
MCT274	225	30

Darlington Output

Isolation Voltage is 7500 V (Min) on all devices. See notes.

Device Type	DC Current Transfer Ratio % Min	$V_{(BR)CEO}$ Volts Min
4N31	50	30
H11B3	100	25
4N29	100	30
4N30	100	30
MCA230	100	30
H11B255	100	55
MCA255	100	55
H11B2	200	25
MCA231	200	30
MOC119*	300	30
TIL119*	300	30
TIL113	300	30
MOC8030*	300	80
TIL127	300	30
TIL128*	300	30
TIL156	300	30
TIL157*	300	30
H11B1	500	25
4N32	500	30
4N33	500	30
MOC8020*	500	50
MOC8050*	500	80
MOC8021*	1000	50

* Pin 3 and Pin 6 are not connected

Notes:
1. Isolation Surge Voltage, V_{ISO}, is an internal device dielectric breakdown rating. For this test LED pins 1 and 2 are common and phototransistor pins 4, 5, and 6 are common.
2. All Motorola couplers are specified at 7500 Vac peak (5 seconds). This usually exceeds the originator's specification and JEDEC registered values.