Intel® Server System R2000LH2/T2 Product Family

Technical Product Specification

Revision 1.0

April 2013

Enterprise Platforms and Services Division

Revision History

Date	Revision Number	Modifications
June 2012	0.8	Updates to images and all sections
Nov 2012	0.95	Updates to images, environmental data,system boards,power supply section, IO Riser, GPGPU, Post Codes, and connector pinouts
April 2013	1.0	Updates to Power Supply section, POST Codes, and formatting

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1. Introduction

This Technical Product Specification (TPS) provides system level information for the Intel® Server System R2000LH2 and Intel® Server System R2000LT2 product families. The system level features of both these product families are common, however the server board integrated into them is different. The Intel® Server System R2000LH2 product family is integrated with an Intel® Server Board S4600LH2 and the Intel® Server System R2000LTH2 product family is integrated with the Intel® Server Board S4600LT2.

This document describes the functions and features of the integrated server system which includes the chassis layout, system boards, power subsystem, cooling subsystem, storage subsystem options, and available installable options. Server board specific details can be obtained by referencing the *Intel® Server Boards S4600LH2/T2 Product Specification*.

In addition, design-level information related to specific server board components or subsystems can be obtained by ordering External Product Specifications (EPS) or External Design Specifications (EDS) related to this server generation. EPS and EDS documents are made available under NDA with Intel and must be ordered through your local Intel representative. See the Reference Documents section for a complete list of available documents.

1.1 Chapter Outline

This document is divided into the following chapters:

- Chapter 1 – Introduction
- Chapter 2 – Product Family Overview
- Chapter 3 – Power Subsystem
- Chapter 4 – Thermal Management
- Chapter 5 – System Storage and Peripherals Drive Bay Overview
- Chapter 6 – Storage Controller Options Overview
- Chapter 7 – Front Control Panel and I/O Panel Overview
- Chapter 8 – Intel® Local Control Panel
- Chapter 9 – PCI Riser Card Support
- Chapter 10 – Additional System Boards
- Chapter 11 – Front Panel
- Chapter 12 – IO Module Support
- Chapter 13 –Intel® Intelligent Power Node Manager (NM)
- Appendix A – Integration and Usage Tips
- Appendix B – POST Code Diagnostic LED Decoder
- Appendix C – Post Code Errors
- Glossary
- Reference Documents

1.2 Server Board Use Disclaimer

Intel Corporation server boards support add-in peripherals and contain a number of high-density Very Large Scale Integration (VLSI) and power delivery components that need adequate airflow to cool. Intel ensures through its own chassis development and testing that when Intel® server building blocks are used together, the fully integrated system will meet the intended thermal requirements of these components. It is the responsibility of the system integrator who chooses not to use Intel developed server building blocks to consult vendor datasheets and operating parameters to determine the amount of airflow required for their specific application and environmental conditions. Intel Corporation cannot be held responsible if components fail or the server board does not operate correctly when used outside any of their published operating or non-operating limits.

2. Product Family Overview

This generation of Intel 2U server platforms offers a variety of system options to meet the varied configuration requirements of high-density high-performance computing environments. The Intel® Server System R2000LH2 and Intel® Server System R2000LT2 servers are comprised of several available 2U rack mount server systems that are integrated with either an Intel® Server Board S4600LH2 or Intel® Server Board S4600LT2.

This chapter provides a high-level overview of the system features and available options as supported in different platform SKUs within this server family. Greater detail for each major system component or feature is provided in the following chapters.

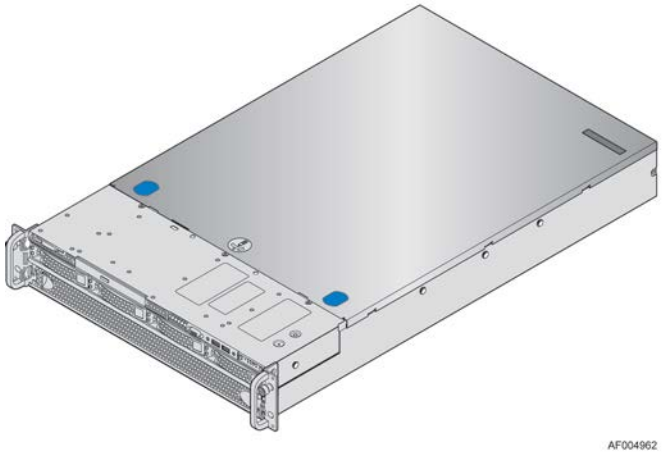


Figure 1. System Overview

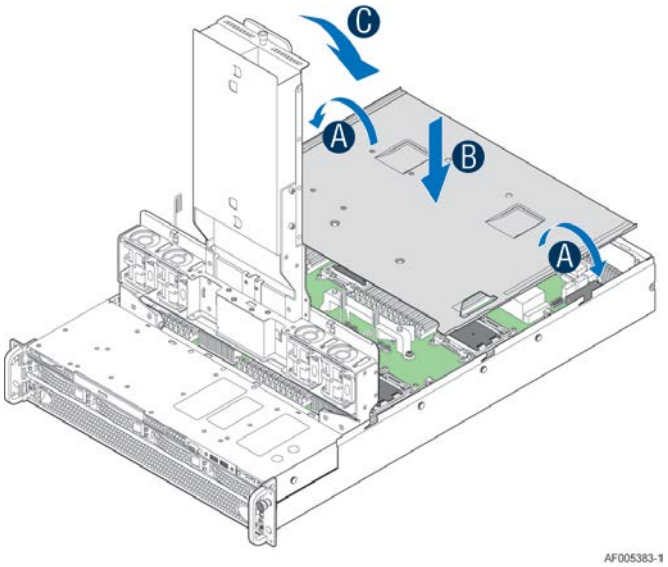


Figure 2. System Assembly

Note: Table 2 lists features common to both server product families. Features that are unique to one product family are identified by either denoting the server system name or the integrated server board name.

Table 1. Server System

Server System	Integrated Server Board
Intel® Server System R2000LH2	Intel® Server Board S4600LH2
Intel® Server System R2000LT2	Intel® Server Board S4600LT2

Table 2. System Feature Set

Feature	Description
Processor support	Support for up to four Intel® Xeon® processors E5-4600 product family with a Thermal Design Power (TDP) of up to 130 W
Memory	▪ 48 DIMM slots – 3 DIMMs / Channel – 4 memory channels per processor ▪ Unbuffered DDR3 (UDIMM), registered DDR3 (RDIMM), Load Reduced DDR3 (LRDIMM) ▪ Memory DDR3 data transfer rates of 800, 1066, 1333, and 1600 MT/s ▪ DDR3 standard I/O voltage of 1.5V and DDR3 Low Voltage of 1.35V
Chipset	Intel® C600-A chipset with support for optional Storage Option Select keys
External I/O connections	▪ DB-15 Video connector (Rear) ▪ RJ-45 Serial Port A connector ▪ **S4600LH2** Dual-port Network Interface supporting 10/100/1000Mbps ▪ **S4600LT2** Dual-port Network Interface supporting 100/1000/10000Mbps ▪ 6 USB 2.0 connectors (4 rear + 2 front)
Internal I/O connectors / headers	▪ One 2x5 pin connector providing front panel support for two USB ports ▪ One Type-A USB 2.0 connector ▪ One 2x15 pin SSI-EEB compliant front panel header ▪ One 2x7pin Front Panel Video connector ▪ One DH-10 Serial Port B connector
Optional I/O Module support	The following I/O modules utilize a single proprietary on-board connector. An installed I/O module can be supported in addition to standard on-board features and any add-in expansion cards. ▪ Quad port 1 GbE based on Intel® Ethernet Controller I350 – RMS25CB0080 ▪ Dual port 10GBase-T Ethernet module based on Intel® Ethernet Controller I350 ▪ Dual SFP+ port 10GbE module based on Intel® 82500 10 GbE controller ▪ Single Port FDR speed Infiniband* module with QSFP connector
System Fans	11 managed system fan headers
Riser Cards	Two riser card slots: ▪ Each riser card slot has a total of 48 PCIe lanes routed to them. ▪ Each riser card slot supports various Full Height Full Length (FHFL) and Full Height Half Length (FHHL) cards.
Video	▪ Integrated 2D Video Controller ▪ 16 MB DDR3 Memory
On-board storage controllers and	▪ One eUSB 2x5 pin connector to support 2mm low-profile eUSB solid state devices

Feature	Description
options	▪ Two 7-pin single port AHCI SATA connectors capable of supporting up to 6 GB/sec ▪ Two SCU 4-port mini-SAS connectors capable of supporting up to 3 GB/sec SAS/SATA ▪ Intel® RAID C600 Upgrade Key support providing optional expanded SATA/SAS RAID capabilities
Security	TPM Module AXXTPME5 (Accessory Option)
Server Management	▪ Integrated Baseboard Management Controller, IPMI 2.0 compliant ▪ Support for Intel® Server Management Software ▪ Intel® Remote Management Module 4 Lite – Accessory Option ▪ Intel® Remote Management Module 4 Management NIC – Accessory Option
Power Supply Options	▪ The server system can have up to two power supply modules installed, providing support for the following power configurations: 1+0, 1+1 Redundant Power, and 2+0 Combined Power ▪ Two power supply options: ▪ AC 1600W ▪ DC 1600W
Storage Bay Options	▪ 8x – 2.5” SATA/SAS Hot Swap Hard Drive Bays ▪ 4x – 3.5” SATA/SAS Hot Swap Hard Drive Bays ▪ 4x – 3.5” SATA/SAS Fixed Hard Drive Bays
Available Rack Mount Kit Options	▪ Tool-less rack mount premium rail kit – Intel Product Code – AXXPRAIL ▪ Value rack mount rail kit – Intel Product Code – AXXVRAIL ▪ Cable Management Arm – Intel Product Code – AXX1U2UCMA (*supported with AXXPRAIL only) ▪ 2-post fixed mount bracket kit – Intel Product Code – AXX2POSTBRCKT

2.1 Chassis Dimensions

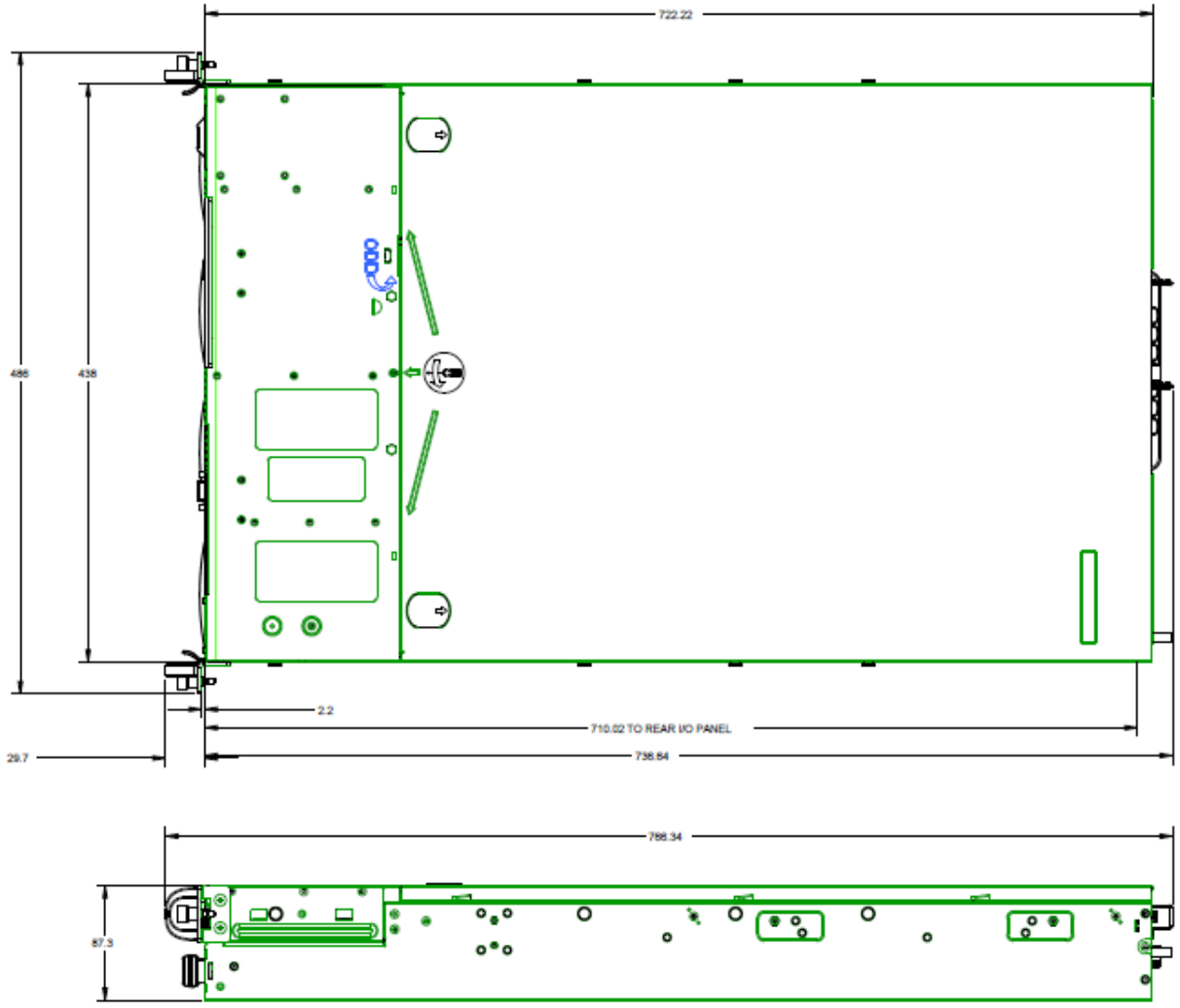


Figure 3. Chassis Dimensions

2.2 System Level Environmental Limits

The following table defines the system level operating and non-operating environmental limits.

Table 3. System Environmental Limits Summary

Parameter		Limits
Temperature		
	Operating	ASHRAE Class A2 – Continuous Operation. 10ºC to 35ºC [1] (50ºF to 95ºF) with the maximum rate of change not to exceed 10°C per hour
		ASHRAE Class A3 – Includes operation up to 40ºC for up to 900 hrs. per year
		ASHRAE Class A4 – Includes operation up to 45ºC for up to 90 hrs. per year
	Shipping	-40ºC to 70ºC (-40ºF to 158ºF)
Altitude		
	Operating	Support operation up to 3050m with ASHRAE class deratings
Humidity		
	Shipping	50% to 90%, non-condensing with a maximum wet bulb of 28°C (at temperatures from 25°C to 35°C)
Shock		
	Operating	Half sine, 2g, 11 mSec
	Unpackaged	Trapezoidal, 25 g, velocity change is based on packaged weight
	Packaged	Product Weight: ≥ 40 to < 80 Non-palletized Free Fall Height = 18 inches Palletized (single product) Free Fall Height = NA
Vibration		
	Unpackaged	5 Hz to 500 Hz 2.20 g RMS random
	Packaged	5 Hz to 500 Hz 1.09 g RMS random
AC-DC		
	Voltage	90 Hz to 132 V and 180 V to 264 V
	Frequency	47 Hz to 63 Hz
	Source Interrupt	No loss of data for power line drop-out of 12 mSec
	Surge Non-operating and operating	Unidirectional
	Line to earth Only	AC Leads 2.0 kV I/O Leads 1.0 kV DC Leads 0.5 kV
ESD		
	Air Discharged	12.0 kV
	Contact Discharge	8.0 kV
Acoustics Sound Power Measured		
	Power in Watts	<300 W ≥300 W ≥600 W ≥1000 W
	Servers/Rack Mount BA	7.0 7.0 7.0 7.0

Note:

1. Intel Corporation server boards contain a number of high-density VLSI and power delivery components that need adequate airflow to cool. Intel ensures through its own chassis development and testing that when Intel® server building blocks are used together, the fully integrated system will meet the intended thermal requirements of these components. It is the responsibility of the system integrator who chooses not to use Intel developed server building blocks to consult vendor datasheets and operating parameters to determine the amount of airflow required for their specific application and environmental conditions. Intel Corporation cannot be held responsible if components fail or the server board does not operate correctly when used outside any of its published operating or non-operating limits.

***Disclaimer Note**: Intel ensures the unpackaged server board and system meet the shock requirement mentioned above through its own chassis development and system configuration. It is the responsibility of the system integrator to determine the proper shock level of the board and system if the system integrator chooses different system configuration or different chassis. Intel Corporation cannot be held responsible, if components fail or the server board does not operate correctly when used outside any of its published operating or non-operating limits.*

See the *Intel® Server Board S4600LH2/T2 Power Budget and Thermal Configuration Guidelines Tool* for system configuration requirements and limitations.

2.3 System Features and Options Overview

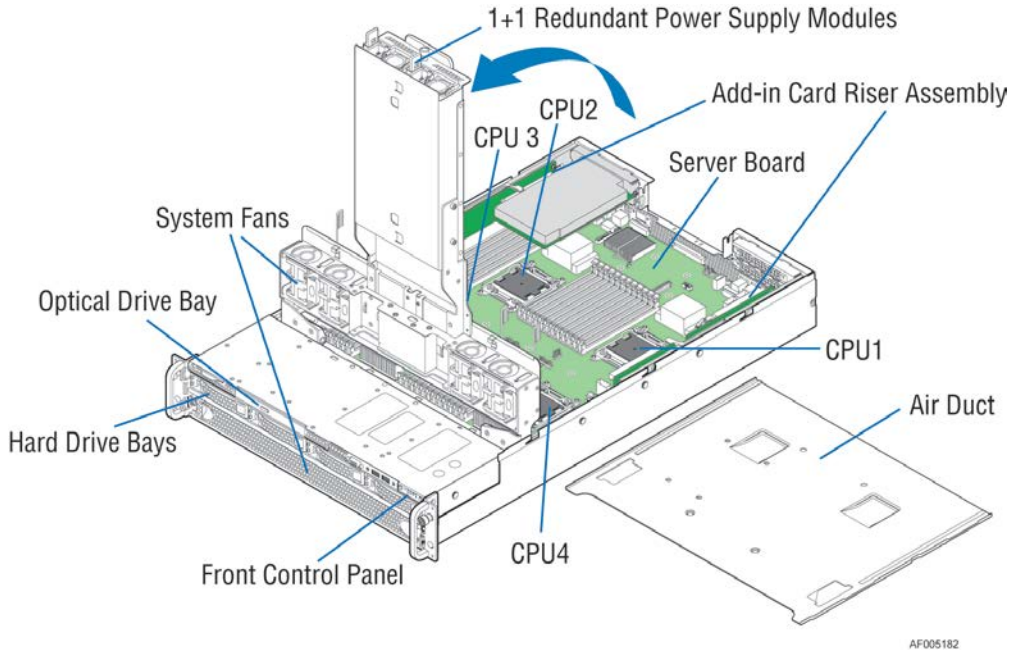


Figure 4. System Components Overview

2.3.1 Hot Swap Hard Drive Bay and Front Panel Options

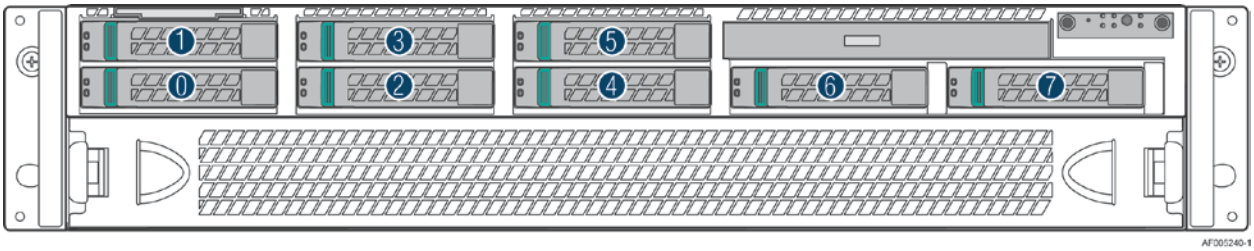


Figure 5. 2.5" Hot Swap Hard Drive Bay - 8 Drive Configuration

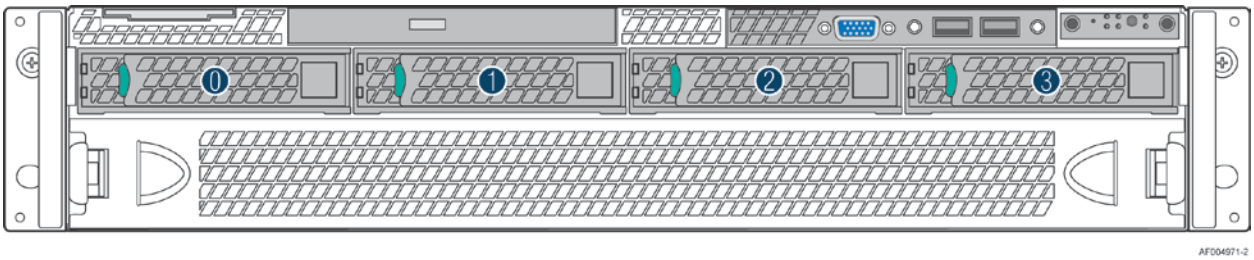


Figure 6. 3.5" Hotswap Hard Drive Bay - 4 Drive Configuration

2.3.2 Back Panel Features

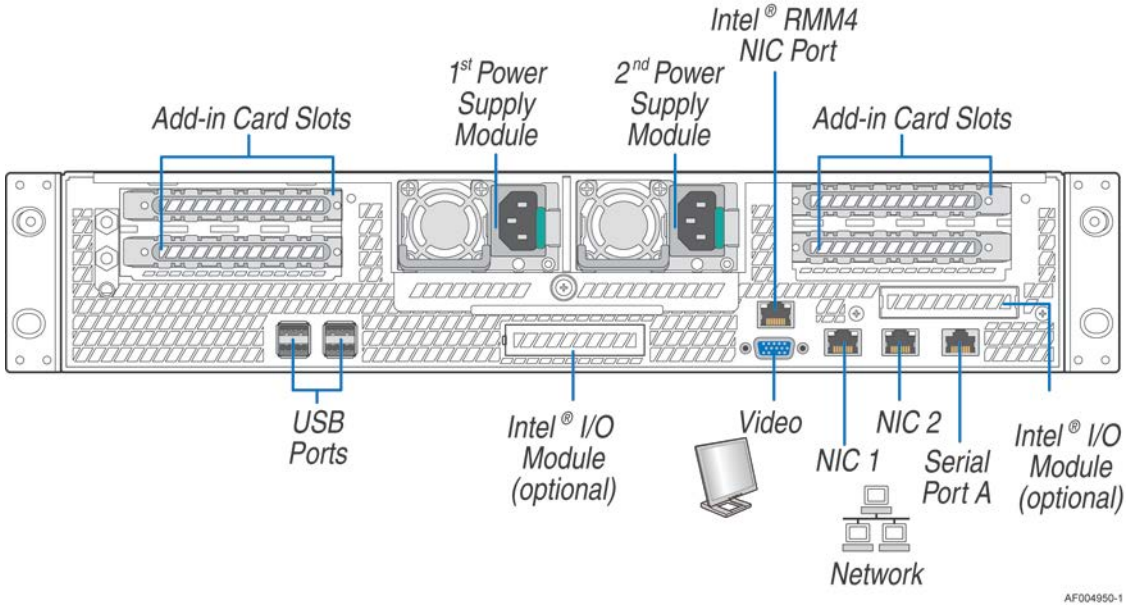


Figure 7. Back Panel Feature Identification

2.3.3 Front Control Panel Options

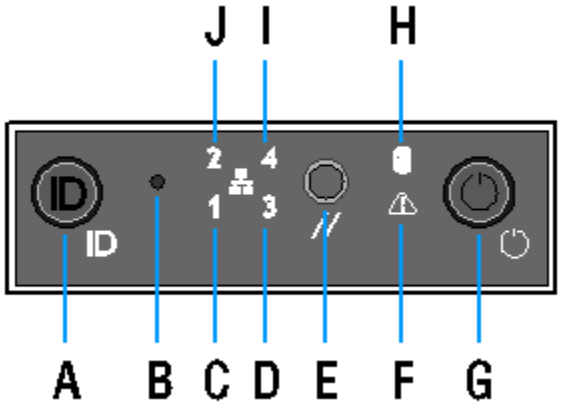


Figure 8. Front Control Panel Options

Table 4 Front Control Panel Options

Label	Description	Label	Description
A	System ID Button w/Integrated LED	F	System Status LED

Label	Description	Label	Description
B	NMI Button (recessed, tool required for use)	G	Power Button w/Integrated LED
C	NIC-1 Activity LED	H	Hard Drive Activity LED
D	Not used	I	Not used
E	System Cold Reset Button	J	NIC-2 Activity LED

2.4 Server Board Features Overview

The following illustration provides a general overview of the server board, identifying key feature and component locations. The majority of the items identified are common for the Intel® Server Board S4600LH2 and S4600LH2. The accompanying table identifies variations when present.

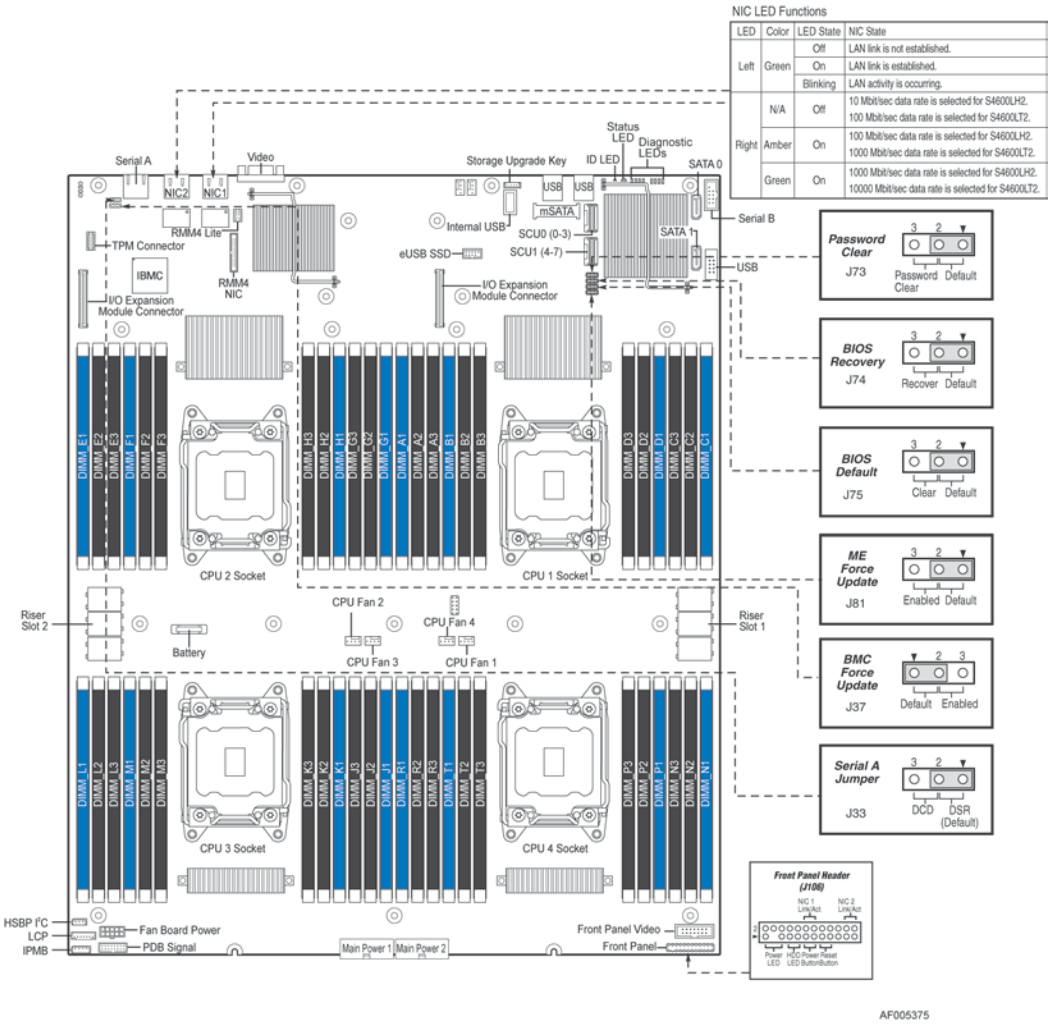


Figure 9. Intel® Server Board S4600LH2/LT2

2.5 Available Front Bezel Support

The optional front bezel is made of molded plastic and uses a snap-on design. When installed, its design allows for maximum airflow to maintain system cooling requirements. The bezel assembly includes snap-in options that can be used for customization.

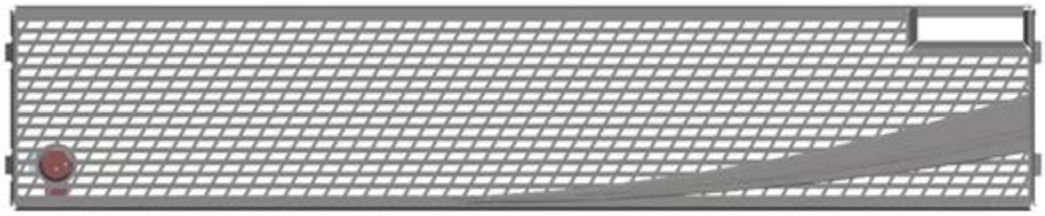


Figure 10. Optional Front Bezel (Intel Product Order Code – A2UBEZEL)

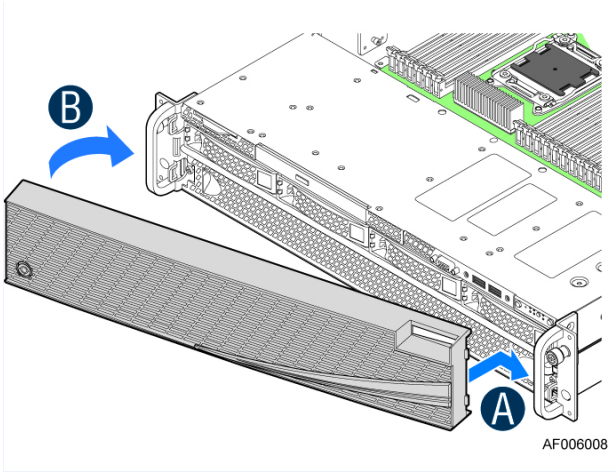


Figure 11. Installing the Front Bezel

2.6 Available Rack and Cabinet Mounting Kit Options

- Tool-less rack mount rail kit – Intel Product Code – AXXPRAIL
  - 2U compatible
  - 65 lbs. max support weight
  - Tool-less installation
  - Full extension from rack
  - Drop in system install
  - Optional cable management arm support
- Cable Management Arm – Intel Product Code – AXX1U2UCMA (*supported with AXXPRAIL only)
- 2-Post Fixed mount bracket kit – Intel Product Code – AXX2POSTBRCKT

3. Power Subsystem

This chapter provides a high level overview of the power management features and specification data for the power supply options available for this server product. Specification variations are identified for each supported power supply.

The server system can have up to two power supply modules installed, supporting the following power supply configurations: 1+0 (single power supply), 1+1 redundant power, and 2+0 combined power (non-redundant).The 1+1 redundant power and 2+0 combined power configurations are automatically configured depending on the total power draw of the system. If the total system power draw exceeds the power capacity of a single power supply module, the power from the second power supply module will be utilized. If this occurs, power redundancy will be lost. In a 2+0 power configuration, the total power available may be less than twice the rated power of the installed power supply modules due to the amount of heat produced with both supplies providing peak power. If system thermals exceed programmed limits, platform management will attempt to keep the system operational. See Closed Loop System Throttling (CLST) and Thermal Management for details.

There are two power supply options available for this server product: 1600W AC and 1600W DC.

Note: Mixing of AC and DC power supplies in the same system is unsupported.

The power supplies are modular, allowing for tool-less insertion and extraction from a bay in the back of the chassis. When inserted, the card edge connector of the power supply mates blindly to a matching slot connector on the server board.

In the event of a power supply failure, redundant 1+1 power supply configurations support hot-swap extraction and insertion.

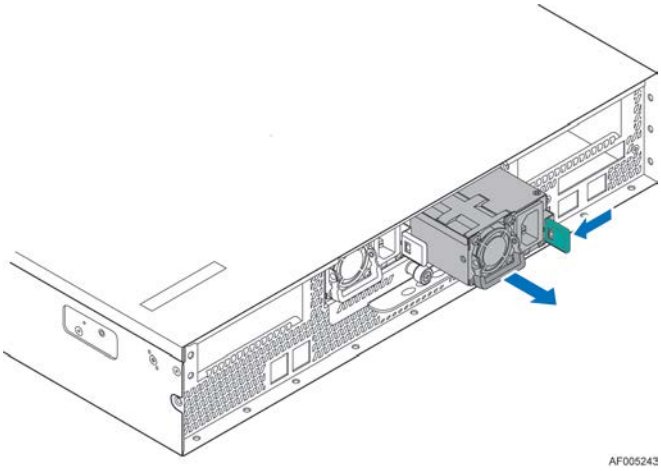


Figure 12. Power Supply

The AC input is auto-ranging and power factor corrected.

3.1 Mechanical Overview

The physical size of the power supply enclosure is 39/40mm x 74mm x 185mm. The power supply contains a single 40mm fan. The power supply has a card edge output that interfaces with a 2x25 card edge connector in the system. The AC plugs directly into the external face of the power supply.

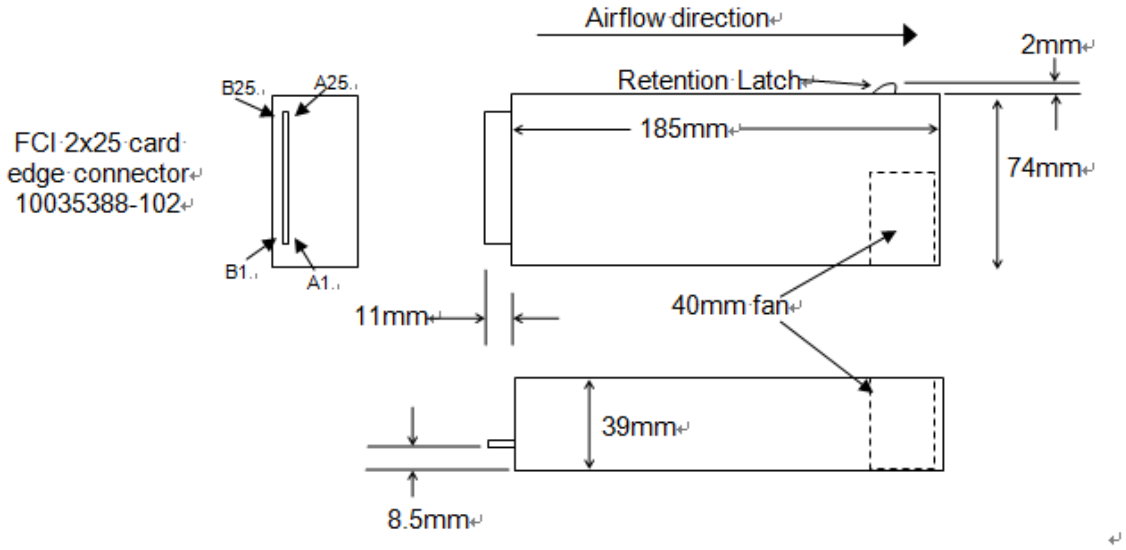


Figure 13. Power Supply Module Mechanical Drawing

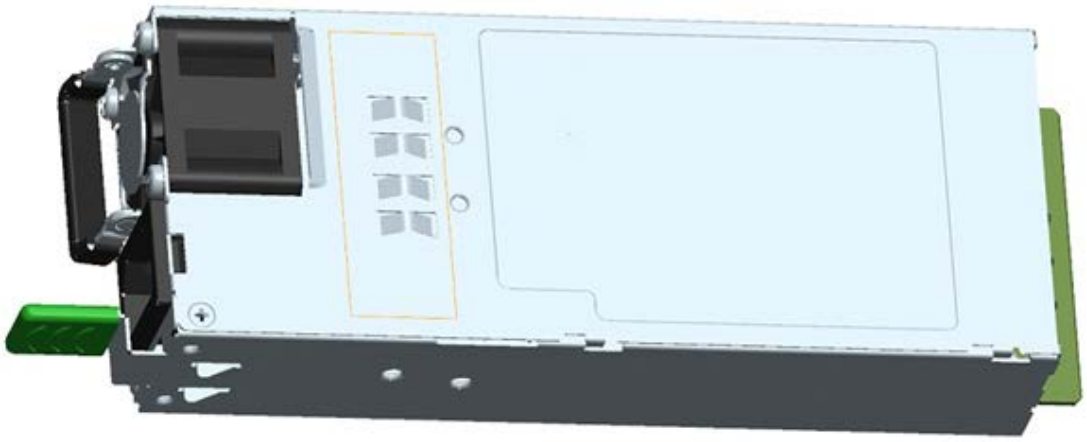


Figure 14. Power Supply Module

Figure 15. AC and DC Power Supplies – Connector View

3.2 Power Connectors

3.2.1 Power Supply Module Card Edge Connector

Each power supply module has a single 2x25 card edge output connection that plugs directly into a matching slot connector on the server board. The connector provides both power and communication signals to the server board. The following table defines the connector pin-out. The connector pin out in table applies to the 1600W (AC) and 1600W (DC) power supplies.

Note: Mixing of AC and DC power supplies in the same system is unsupported.

Table 5. Power Supply Module Output Power Connector Pin-out

Pin	Name	Pin	Name
A1	GND	B1	GND
A2	GND	B2	GND
A3	GND	B3	GND
A4	GND	B4	GND
A5	GND	B5	GND
A6	GND	B6	GND
A7	GND	B7	GND
A8	GND	B8	GND
A9	GND	B9	GND
A10	+12V	B10	+12V
A11	+12V	B11	+12V
A12	+12V	B12	+12V
A13	+12V	B13	+12V
A14	+12V	B14	+12V
A15	+12V	B15	+12V
A16	+12V	B16	+12V
A17	+12V	B17	+12V
A18	+12V	B18	+12V
A19	PMBus SDA	B19	A0 (SMBus address)
A20	PMBus SCL	B20	A1 (SMBus address)
A21	PSON	B21	12V stby
A22	SMBAlert#	B22	Cold Redundancy Bus
A23	Return Sense	B23	12V load share bus
A24	+12V remote Sense	B24	No Connect
A25	PWOK	B25	Compatibility Check pin*

3.3 Power Supply Module Efficiency

The following table provides the required minimum efficiency level at various loading conditions. These are provided at three different load levels: 100%, 50%, and 20%. Efficiency is tested over an AC input voltage range of 115 VAC to 220 VAC.

Table 6. 1600 Watt (AC) Power Supply Efficiency (Gold)

Loading	100% of maximum	50% of maximum	20% of maximum	10% of maximum
Minimum Efficiency	91%	94%	90%	82%

3.4 AC and DC Power Cord Specification Requirements

The AC and DC power cords used meet the specification requirements listed in the following tables and figures.

Table 7. AC Power Cord Specifications

Cable Type	SJT
Wire Size	16 AWG
Temperature Rating	105ºC
Amperage Rating	13 A
Voltage Rating	125 V

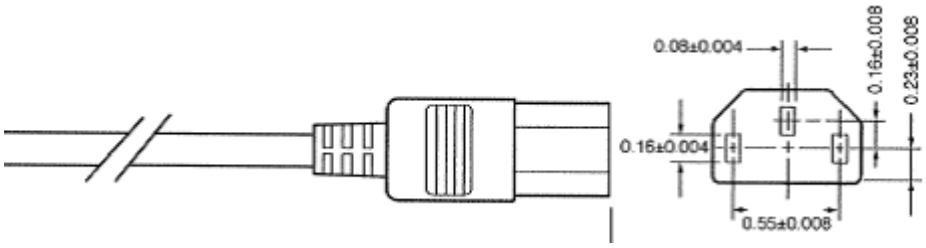


Figure 16. AC Power Cord

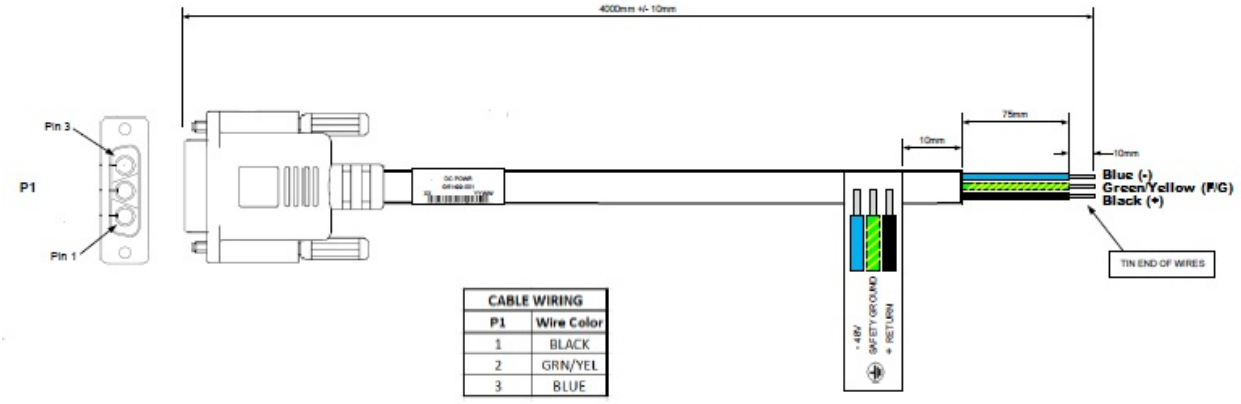


Figure 17. DC Power Cord

3.5 AC Input Specifications

3.5.1 Power Factor

The power supply meets the power factor requirements stated in the Energy Star Program Requirements for Computer Servers. These requirements are stated below.

Table 8. Power Factor

Output power	10% load	20% load	50% load	100% load
Power factor 1600w AC	> 0.80	> 0.90	> 0.90	> 0.95

Note: Tested at 230VAC, 50Hz and 60Hz and 115VAC, 60Hz

3.5.2 AC Input Voltage Specification

The power supply operates within all specified limits over the following input voltage range. Harmonic distortion of up to 10% of the rated line voltage does not cause the power supply to go out of specified limits. Application of an input voltage below 85VAC does not cause damage to the power supply, including a blown fuse.

Table 9. AC Input Voltage Range

Parameter	Min	Rated	Max	Start Up VAC	Power Off VAC
Voltage (110)	90 Vrms	100-127 Vrms	140 Vrms	85VAC +/- 4VAC	70VAC +/- 5VAC
Voltage (220)	180 Vrms	200-240 Vrms	264 Vrms		
Frequency	47 Hz	50/60	63 Hz		

Note:

1. Maximum input current at low input voltage range is measured at 90VAC, at max load.
2. Maximum input current at high input voltage range is measured at 180VAC, at max load.
3. This requirement is not to be used for determining agency input current markings.

3.5.3 AC Line Isolation Requirements

The power supply meets all safety agency requirements for dielectric strength. Transformers' isolation between primary and secondary windings complies with the 3000VAC (4242VDC) dielectric strength criteria. If the working voltage between primary and secondary dictates a higher dielectric strength test voltage, the highest test voltage will be used. In addition the insulation system complies with reinforced insulation per safety standard IEC 950. Separation between the primary and secondary circuits, and primary to ground circuits, complies with the IEC 950 spacing requirements.

3.5.4 AC Line Dropout/Holdup

An AC line dropout is defined to be when the AC input drops to 0VAC at any phase of the AC line for any length of time. During an AC dropout the power supply meets dynamic voltage regulation requirements. An AC line dropout of any duration does not cause tripping of control signals or protection circuits. If the AC dropout lasts longer than the holdup time, the power supply will recover and meet all turn on requirements. The power supply meets the AC dropout

requirement over rated AC voltages and frequencies. A dropout of the AC line for any duration does not cause damage to the power supply.

Table 10. AC Line Dropout/Holdup

Power Supply	Loading	Holdup Time
1600W AC	70%	10.0 msec

3.5.4.1 AC Line 12VSB Holdup

The 12VSB output voltage stays in regulation under its full load (static or dynamic) during an AC dropout of 70ms min (=12VSB holdup time) whether the power supply is in ON or OFF state (PSON asserted or de-asserted).

3.5.5 AC Line Fuse

The power supply has one line fused in the single line fuse on the line (Hot) wire of the AC input. The line fusing is acceptable for all safety agency requirements. The input fuse is a slow blow type. The AC inrush current does not cause the AC line fuse to blow under any conditions. All protection circuits in the power supply will not cause the AC fuse to blow unless a component in the power supply has failed. This includes DC output load short conditions.

3.5.6 AC Inrush

The AC line inrush current does not exceed 65A peak, for up to one-quarter of the AC cycle, after which, the input current is no more than the specified maximum input current. The peak inrush current is less than the ratings of its critical components (including input fuse, bulk rectifiers, and surge limiting device).

The power supply meets the inrush requirements for any rated AC voltage, during turn on at any phase of AC voltage, during a single cycle AC dropout condition as well as upon recovery after AC dropout of any duration, and over the specified temperature range (T_{op}).

3.5.7 AC Line Transient Specification

The AC line transient conditions are defined as sag and surge conditions. Sag conditions are also commonly referred to as brownout; these conditions are defined as the conditions when the AC line voltage drops below nominal voltage. Surge conditions are defined as the conditions when the AC line voltage rises above nominal voltage.

The power supply meets the requirements under the following AC line sag and surge conditions.

Table 11. AC Line Sag Transient Performance

AC Line Sag (10sec interval between each sagging)				
Duration	Sag	Operating AC Voltage	Line Frequency	Performance Criteria
0 to 1/2 AC cycle	95%	Nominal AC Voltage ranges	50/60 Hz	No loss of function or performance
> 1 AC cycle	> 30%	Nominal AC Voltage ranges	50/60 Hz	Loss of function acceptable, self-recoverable

Table 12. AC Line Surge Transient Performance

AC Line Surge				
Duration	Surge	Operating AC Voltage	Line Frequency	Performance Criteria
Continuous	10%	Nominal AC Voltages	50/60 Hz	No loss of function or performance
0 to 1/2 AC cycle	30%	Mid-point of nominal AC Voltages	50/60 Hz	No loss of function or performance

3.5.8 Susceptibility Requirements

The power supply meets the following electrical immunity requirements when connected to a cage with an external EMI filter that meets the criteria defined in the *SSI document EPS Power Supply Specification*. For further information on Intel standards, request a copy of the *Intel Environmental Standards Handbook*.

Table 13. Performance Criteria

Level	Description
A	The apparatus shall continue to operate as intended. No degradation of performance.
B	The apparatus shall continue to operate as intended. No degradation of performance beyond spec limits.
C	Temporary loss of function is allowed provided the function is self-recoverable or can be restored by the operation of the controls.

3.5.9 Electrostatic Discharge Susceptibility

The power supply complies with the limits defined in *EN 55024: 1998/A1: 2001/A2: 2003* using the IEC 61000-4-2: Edition 1.2: 2001-04 test standard and performance criteria B defined in *Annex B of CISPR 24*.

3.5.10 Fast Transient/Burst

The power supply complies with the limits defined in *EN55024: 1998/A1: 2001/A2: 2003* using the IEC 61000-4-4: Second edition: 2004-07 test standard and performance criteria B defined in *Annex B of CISPR 24*.

3.5.11 Radiated Immunity

The power supply complies with the limits defined in *EN55024: 1998/A1: 2001/A2: 2003* using the IEC 61000-4-3: Edition 2.1: 2002-09 test standard and performance criteria A defined in *Annex B of CISPR 24*.

3.5.12 Surge Immunity

The power supply is tested with the system for immunity to AC Unidirectional wave; 2kV line to ground and 1kV line to line, per *EN 55024: 1998/A1: 2001/A2: 2003*, *EN 61000-4-5: Edition 1.1:2001-04*.

The pass criteria include:

- No unsafe operation is allowed under any condition.
- All power supply output voltage levels to stay within proper spec levels.
- No change in operating state or loss of data during and after the test profile.
- No component damage under any condition.

The power supply complies with the limits defined in *EN55024: 1998/A1: 2001/A2: 2003* using the IEC 61000-4-5: Edition 1.1:2001-04 test standard and performance criteria B defined in *Annex B of CISPR 24*.

3.5.13 Power Recovery

The power supply recovers automatically after an AC power failure. AC power failure is defined to be any loss of AC power that exceeds the dropout criteria.

3.5.14 Voltage Interruptions

The power supply complies with the limits defined in *EN55024: 1998/A1: 2001/A2: 2003* using the IEC 61000-4-11: Second Edition: 2004-03 test standard and performance criteria C defined in *Annex B of CISPR 24*.

3.5.15 Protection Circuits

The protection circuits inside the power supply cause only the power supply's main outputs to shut down. If the power supply latches off due to a protection circuit tripping, an AC cycle OFF for 15 seconds and a PSON# cycle HIGH for one second reset the power supply.

3.5.16 Over-current Protection (OCP)

The power supply has current limit to prevent the outputs from exceeding the values shown in table below. If the current limits are exceeded, the power supply will shut down and latch off. The latch will be cleared by toggling the PSON# signal or by an AC power interruption. The power supply will not be damaged from repeated power cycling in this condition. 12VSB will be auto-recovered after removing OCP limit.

Table 14. Power Supply Over Current Protection

Power Supply	Output Voltage	Input voltage range	Over Current Limits
1600W AC	+12V	90 – 264VAC	180A min; 200A max
	12VSB	90 – 264VAC	4A min; 5A max

3.5.17 Over-voltage Protection (OVP)

The power supply over voltage protection is locally sensed. The power supply will shut down and latch off after an over voltage condition occurs. This latch will be cleared by toggling the PSON# signal or by an AC power interruption. The values are measured at the output of the power supply's connectors. The voltage will never exceed the maximum levels when measured at the power connectors of the power supply connector during any single point of fail. The voltage will never trip any lower than the minimum levels when measured at the power connector. 12VSB will be auto-recovered after removing OVP limit.

Table 15. Over Voltage Protection (OVP) Limits

Output Voltage	Min (V)	Max (V)
+12V	13.3	14.5
12VSB	13.3	14.5

3.5.18 Over-temperature Protection (OTP)

The power supply is protected against over temperature conditions caused by loss of fan cooling or excessive ambient temperature. In an OTP condition the PSU will shut down. When the power supply temperature drops to within specified limits, the power supply will restore power automatically, while the 12VSB remains always on. The OTP circuit has built-in margin so that the power supply will not oscillate on and off due to temperature recovering condition. The OTP trip level has a minimum of 4°C of ambient temperature margin.

3.6 1600W DC Power Supply Support

3.6.1 Power Supply Module Efficiency

The following table provides the required minimum efficiency level at various loading conditions. These are provided at three different load levels: 100%, 50%, and 20%. The input voltage is set to -53VDC during the test.

Table 16. 1600 Watt (DC) Power Supply Efficiency (Platinum)

Loading	100% of maximum	50% of maximum	20% of maximum	10% of maximum
Minimum Efficiency	88%	92%	88%	80%

3.6.2 DC Inlet Connector

The power supply has the -48VDC input fused. The fusing is acceptable for all safety agency requirements. The DC inrush current does not cause the fuse to blow under any conditions. No protection circuits in the power supply will cause the DC fuse to blow unless a component in the power supply has failed. This includes DC output load short conditions.

3.6.3 DC Input Voltage Specification

The power supply operates within all specified limits over the following input voltage range.

Table 17. 1600 Watt (DC) Power Supply Efficiency (Platinum)

Parameter	Minimum	Rated	Maximum	Maximum Input Current
DC Voltage	-38VDC	-48VDC/-60VDC	-75VDC	TBD

3.6.4 DC Holdup/Dropout Time

During a DC dropout of 0.2ms or less the power supply meets dynamic voltage regulation requirements for every rated load condition. A DC line dropout of 0.2ms or less does not cause tripping of control signals or protection circuits. Repeated every 10 seconds starting at the min input voltage DC line dropout does not damage the power supply under any specified load conditions. The PWOK signal does not go to a low state under these conditions. DC dropout transients in excess of 0.2 milliseconds may cause shutdown of the PS or out of regulation conditions, but do not damage the power supply. The power supply recovers and meets all turn on requirements for DC dropouts that last longer than 0.2ms. The power supply meets the DC dropout requirement over rated DC voltages and output loading conditions.

Table 18. DC Holdup/Dropout Time

Power Supply Wattage	Loading	Holdup Time
1600W	1200W (75%)	0.2 msec

3.6.5 DC Line Fuse

The power supply has the -48VDC input fused. The fusing is acceptable for all safety agency requirements. The DC inrush current does not cause the fuse to blow under any conditions. No protection circuits in the power supply will cause the DC fuse to blow unless a component in the power supply has failed. This includes DC output load short conditions.

3.6.6 DC Inrush

The maximum inrush current from power-on is limited to a level below the surge rating of the input line cable; input diodes, fuse, and EMI filter components. The inrush current does not exceed the I^2t curve shown in ETS 300 132-2 Equipment Engineering (EE); Power Supply Interface at the Input to Telecommunication Equipment; Part2: Operated by Direct Current (DC). To allow multiple power cycling events and DC line transient conditions, the maximum I^2t value does not exceed 20% of the fuse maximum rating. Repetitive ON/OFF cycling of the DC input line voltage does not damage the power supply or cause the input fuse to blow.

3.6.7 DC Line Surge Voltages (Line Transients)

The power supply demonstrates tolerance for transients in the input DC power line caused by switching or lightning. The power supply is primarily tested and complies with the requirements of EN61000-4-5: “Electrical Fast transients / Burst Requirements and Surge Immunity Requirements” for surge withstand capability. The test voltage surge levels are to be 500Vpk for each Line to Primary Earth Ground test (none required between the L1 and L2).

- **75VDC Line Transient Test**

  A standard line voltage momentary transient test is shown below. This test simulates a momentary voltage overshoot. This does not affect the operation of the PSU, and the output voltages remain in regulation.

  This test is conducted every 10 sec for 30 min (180 times total).

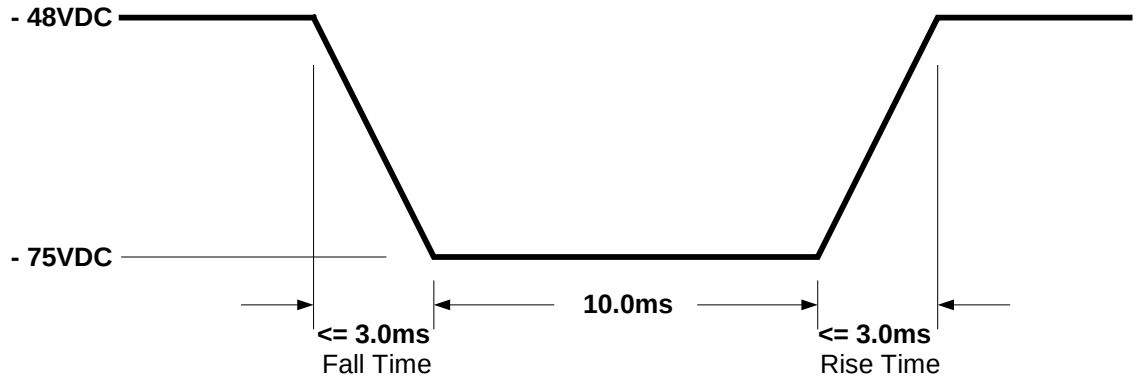


Figure 18. 75VDC Test

- **0V Line Transient Test**

  A standard line voltage momentary blackout test is shown below. This test simulates a momentary switch throw off-on. The power supply restarts, not latches.

  This test is conducted 3 times in 10 min intervals. Refer to document *TP76200MP Section 8.05-b*, page 14, for this transient test setup.

Practically a blackout of any duration does not damage the power supply in any way and not cause a latch off condition.

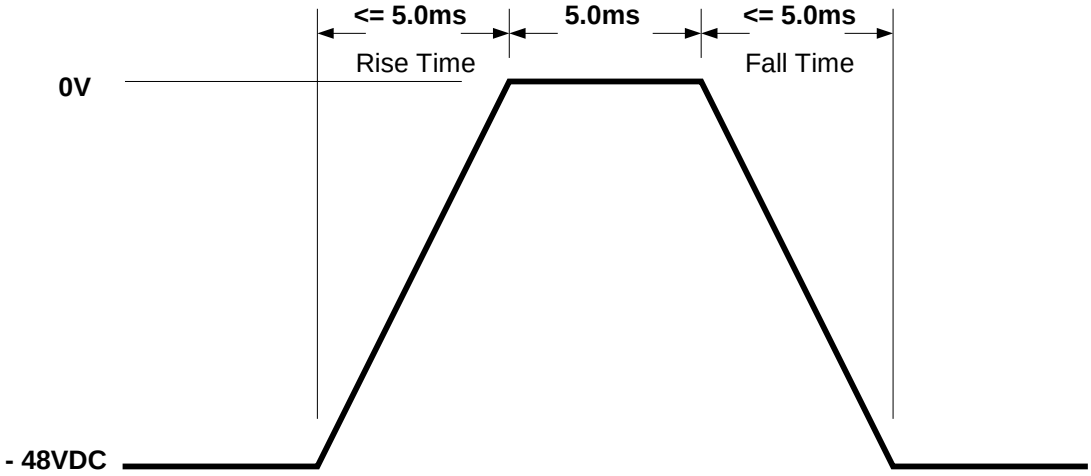


Figure 19. 0VDC Test

The power supply can also withstand the following transients.

Table 19. Line Voltage Transient Limits

Duration	Slope/Rate	Output	Performance Criteria
200µs max	-48V → -30V w/ +2V/µs	Rated DC Voltages	No loss of function or performance
	-30V → -48V w/ -2V/µs	Rated DC Voltages	No loss of function or performance

3.6.8 Residual Voltage Immunity in Standby Mode

The power supply is immune to any residual voltage placed on its outputs (typically a leakage voltage through the system from standby output) up to 500mV. There is neither additional heat generated, nor stressing of any internal components with this voltage applied to any individual or all outputs simultaneously. It also does not trip the protection circuits during turn on. The residual voltage at the power supply outputs for no load condition will not exceed 100mV when AC voltage is applied and the PSON# signal is de-asserted.

3.6.9 Protection Circuits

The protection circuits inside the power supply cause only the power supply's main outputs to shut down. If the power supply latches off due to a protection circuit tripping, a DC cycle OFF for 15sec and a PSON# cycle HIGH for 1sec will be able to reset the power supply.

3.6.9.1 Current Limit (OCP)

The power supply has current limit to prevent the outputs from exceeding the values shown in table below. If the current limits are exceeded, the power supply will shut down and latch off. The latch will be cleared by toggling the PSON# signal or by a DC power interruption. The

power supply will not be damaged from repeated power cycling in this condition. 12VSB will be auto-recovered after removing OCP limit.

Table 20. Over Current Protection

Output Voltage	Input Voltage Range	Over Current Limits
+12V	38 – 75VDC	168A min
12VSB	38 – 75VDC	3.6A min

3.6.9.2 Over Voltage Protection (OVP)

The power supply over voltage protection is locally sensed. The power supply will shut down and latch off after an over voltage condition occurs. This latch will be cleared by toggling the PSON# signal or by a DC power interruption. The values are measured at the output of the power supply's connectors. The voltage will never exceed the maximum levels when measured at the power connectors of the power supply connector during any single point of fail. The voltage will never trip any lower than the minimum levels when measured at the power connector. 12VSB will be auto-recovered after removing OVP limit.

Table 21. Over Voltage Protection Limits

Output Voltage	Min (V)	Max (V)
+12V	13.3	14.5
12VSB	13.3	14.5

3.6.10 Over Temperature Protection (OTP)

The power supply is protected against over temperature conditions caused by loss of fan cooling or excessive ambient temperature. In an OTP condition the PSU will shut down. When the power supply temperature drops to within specified limits, the power supply will restore power automatically, while the 12VSB remains always on. The OTP circuit has built-in margin so that the power supply will not oscillate on and off due to temperature recovering condition. The OTP trip level has a minimum of 4°C of ambient temperature margin.

3.7 Cold Redundancy Support

The power supplies that support cold redundancy can be enabled to go into a low-power state (that is, cold redundant state) in order to provide increased power usage efficiency when system loads are such that both power supplies are not needed. When the power subsystem is in Cold Redundant mode, only the needed power supply to support the best power delivery efficiency is ON. Any additional power supply, including the redundant power supply, is in Cold Standby state.

Each power supply has an additional signal that is dedicated to supporting Cold Redundancy, CR_BUS. This signal is a common bus between all power supplies in the system. CR_BUS is asserted when there is a fault in any power supply or the power supplies output voltage falls below the Vfault threshold. Asserting the CR_BUS signal causes all power supplies in Cold Standby state to power ON.

Enabling power supplies to maintain best efficiency is achieved by looking at the Load Share bus voltage and comparing it to a programmed voltage level via a PMBus command. Whenever there is no active power supply on the Cold Redundancy bus driving a HIGH level on the bus, all power supplies are ON no matter their defined Cold Redundant roll (active or Cold Standby). This guarantees that incorrect programming of the Cold Redundancy states of the power supply will never cause the power subsystem to shut down or become over loaded. The default state of the power subsystem is all power supplies ON. There needs to be at least one power supply in Cold Redundant Active state or Standard Redundant state to allow the Cold Standby state power supplies to go into Cold Standby state.

3.7.1 Powering on Cold Standby Supplies to Maintain Best Efficiency

The power supplies in Cold Standby state monitor the shared voltage level of the load share signal to sense when it needs to power on. Depending upon which position (1, 2, or 3) the system defines that power supply to be in the cold standby configuration, will slightly change the load share threshold that the power supply shall power on at.

Table 22. Example Load Share Threshold for Activating Supplies

	Enable Threshold for $V_{CR\_ON\_EN}$	Disable Threshold for $V_{CR\_ON\_DIS}$	CR_BUS De-asserted/Asserted States
Standard Redundancy	NA; Ignore dc/dc_ active# signal; power supply is always ON		OK = High Fault = Low
Cold Redundant Active	NA; Ignore dc/dc_ active# signal; power supply is always ON		OK = High Fault = Low
Cold Standby 1 (02h)	3.2V (40% of max)	3.2V x 0.5 x 0.9 = 1.44V	OK = Open Fault = Low
Cold Standby 2 (03h)	5.0V (62% of max)	5.0V x 0.67 x 0.9 = 3.01V	OK = Open Fault = Low
Cold Standby 3 (04h)	6.7V (84% of max)	6.7V x 0.75 x 0.9 = 4.52V	OK = Open Fault = Low

Notes:

Maximum load share voltage = 8.0V at 100% of rated output power

These are example load share bus thresholds; for a given power supply, these shall be customized to maintain the best efficiency curve for that specific model.

3.7.2 Powering on Cold Standby Supplies during a Fault or Over Current Condition

When an active power supply asserts its CR_BUS signal (pulling it low), all parallel power supplies in cold standby mode shall power on within 100 µsec.

3.7.3 BMC Requirements

The BMC uses the *Cold_Redundancy_Config* command to define or configure the power supply's roll in cold redundancy and to turn on/off cold redundancy.

The BMC shall schedule a rolling change for which PSU is the Active, Cold Stby1, Cold Stby 2, and Cold Stby 3 power supply. This allows for equal loading across power supply over their life.

Events that trigger a re-configuration of the power supplies using the *Cold_Redundancy_Config* command:

- AC power ON
- PSON power ON
- Power Supply Failure
- Power supply inserted into system

3.7.4 Power Supply Turn On Function

Powering on and off of the cold standby power supplies is only controlled by each PSU sensing the Vshare bus. Once a power supply turns on after crossing the enable threshold, it lowers its threshold to the disable threshold. The system defines the position of each power supply in the Cold Redundant operation. It will do this each time the system is powered on, a power supply fails, or a power supply is added to the system.

The system is relied upon to tell each power supply where it resides in the Cold Redundancy scheme.

3.8 Closed Loop System Throttling (CLST)

The server system supports Closed Loop System Throttling (CLST). CLST prevents the system from crashing if a power supply module is overloaded. If the system power reaches a pre-programmed power limit, CLST will throttle system memory and/or processors to reduce power. System performance will be impacted if this occurs. For more information about CLST implementation, refer to the *SmaRT & CLST Architecture on "Romley" Systems and Power Supplies Specification* (IBL Reference # 461024).

3.9 Smart Ride Through (SmaRT)

The server system supports Smart Ride Through Throttling (SmaRT). This feature increases the reliability for a system operating in a heavy power load condition, to remain operational during an AC line dropout event. See AC Line Dropout/Holdup for power supply hold up time requirements for AC Line dropout events.

When AC voltage is too low, a fast AC loss detection circuit inside each installed power supply asserts an SMBALERT# signal to initiate a throttle condition in the system. System throttling reduces the bandwidth to both system memory and CPUs, which in turn reduces the power load during the AC line drop out event.

3.10 Power Supply Status LED

There is a single bi-color LED to indicate power supply status. The LED operation is defined in the following table.

Table 23. LED Indicators

Power Supply Condition	LED State
Output ON and OK	GREEN
No AC power to all power supplies	OFF
AC present / Only 12VSB on (PS off) or PS in Cold redundant state	1Hz Blink GREEN
AC cord unplugged or AC power lost; with a second power supply in parallel still with AC input power	AMBER
Power supply warning events where the power supply continues to operate; high temp, high power, high current, slow fan	1Hz Blink Amber
Power supply critical event causing a shutdown; failure, OCP, OVP, Fan Fail	AMBER
Power supply FW updating	2Hz Blink GREEN

4. Thermal Management

The fully integrated system is designed to operate at external ambient temperatures of between 10ºC and 35ºC with limited excursion based operation up to 45ºC, which is outlined in *Figure 3. Chassis Dimensions*.

Working with integrated platform management, several features within the system are designed to move air in a front to back direction, through the system and over critical components in order to prevent them from overheating and allow the system to operate with best performance.

The Intel® Server System R2000LH2 and Intel® Server System R2000LT2 product family support short-term, excursion-based, operation up to 45°C (ASHRAE A4) with limited performance impact. The configuration requirements and limitations are described in the configuration matrix found in the *Intel® Server System R2000LH2LT2 Power Budget and Thermal Configuration Tool*, available at http://www.intel.com/support.

The installation and functionality of several system components are used to maintain system thermals. They include 11 managed 40x56mm a dual rotor hot swap system fans, one integrated 40mm fan for each installed power supply module, an air duct, populated hard drive carriers, and installed CPU heats sinks. The hard drive carriers can be populated with a hard drive or supplied drive blank. In addition, it may be necessary to have specific DIMM slots populated with DIMMs or supplied DIMM blanks.

4.1 Thermal Operation and Configuration Requirements

To keep the system operating within supported maximum thermal limits, the system meets the following operating and configuration guidelines:

- The system operating ambient is designed for sustained operation up to 35ºC (ASHRAE Class A2) with short term excursion based operation up to 45ºC (ASHRAE Class A4).
  - The system can operate up to 40ºC (ASHRAE Class A3) for up to 900 hours per year.
  - The system can operate up to 45ºC (ASHRAE Class A4) for up to 90 hours per year.
  - System performance may be impacted when operating within the extended operating temperature range.
  - There is no long term system reliability impact when operating at the extended temperature range within the approved limits.
- Specific configuration requirements and limitations are documented in the configuration matrix found in the *Intel® Server System R2000LH2LT2 Power Budget and Thermal Configuration Tool*, available at http://www.intel.com/support.
- The CPU-1 processor and CPU heat sink must be installed first. The CPU-2, CPU-3, and CPU-4 heat sinks must be installed at all times, with or without a processor installed.
- Memory Slot population requirements:

  NOTE: Specified memory slots can be populated with a DIMM or supplied DIMM Blank. Memory population rules apply when installing DIMMs.

  - **DIMM Population Rules on CPU-1** – Install DIMMs in order; Channels A, B, C, and D. Start with the first DIMM (Blue Slot) on each channel, then slot 2, and then slot 3. Only remove factory installed DIMM blanks when populating the slot with memory.
  - **DIMM Population on CPU-2** – Install DIMMs in order; Channels E, F, G, and H. Start with the first DIMM (Blue Slot) on each channel, then slot 2, and then slot 3. Only remove factory installed DIMM blanks when populating the slot with memory.
  - The following system configurations require that specific memory slots be populated at all times using either a DIMM or supplied DIMM Blank.
  - **DIMM Population Rules on CPU-3**– Install DIMMs in order; Channels J, K, L, and M. Start with the first DIMM (Blue Slot) on each channel, then slot 2, and then slot 3. Only remove factory installed DIMM blanks when populating the slot with memory.
  - **DIMM Population on CPU-4** – Install DIMMs in order; Channels N, P, R, and T. Start with the first DIMM (Blue Slot) on each channel, then slot 2, and then slot 3. Only remove factory installed DIMM blanks when populating the slot with memory.
- All hard drive bays must be populated. The hard drive carriers can be populated with a hard drive or supplied drive blank.
- With the system operating, the air duct must be installed at all times.
- In single power supply configurations, the second power supply bay must have the supplied filler blank installed at all times.
- The system must be configured with dual power supplies for the system to support fan redundancy.
- The system top-cover must be installed at all times when the system is in operation. The only exception to this requirement is to hot replace a failed system fan, in which case the top cover can be removed for no more than 3 minutes at a time.

4.2 Thermal Management Overview

In order to maintain the necessary airflow within the system, all of the previously listed components and top cover need to be properly installed. For best system performance, the external ambient temperature should remain below 35ºC and all system fans should be operational. The system is designed for fan redundancy. If a single system fan fails, integrated platform management will change the state of the System Status LED to flashing Green, report an error to the system event log, and automatically increase the fan speeds of all remaining system fans in order to maintain system temperatures below maximum thermal limits.

If system thermals continue to increase with the system fans operating at their maximum speed, platform management may begin to throttle bandwidth of either the memory subsystem or the processors or both, in order to keep components from overheating and keep the system operational. Throttling of these subsystems will continue until system thermals are reduced below preprogrammed limits.

If system thermals increase to a point beyond the maximum thermal limits, the system will shut down, the System Status LED will change to a solid Amber state, and the event will be logged to the system event log.

Note: Sensor data records (SDRs) for any given system configuration must be loaded by the system integrator for proper thermal management of the system. SDRs are loaded using the FRUSDR utility.

An intelligent Fan Speed Control (FSC) and thermal management technology (mechanism) is used to maintain comprehensive thermal protection, deliver the best system acoustics, and improve fan power efficiency. Options in <F2> BIOS Setup (**BIOS** > **Advanced** > **System Acoustic and Performance Configuration**) allow for parameter adjustments based on the actual system configuration and usage. Refer to the following sections for a description of each setting.

4.2.1 Set Throttling Mode

This option is used to select the desired memory thermal throttling mechanism. Available settings include [Auto], [DCLTT], [SCLTT] and [SOLTT].

- [Auto] – Factory Default Setting: BIOS automatically detects and identifies the appropriate thermal throttling mechanism based on DIMM type, airflow input, and DIMM sensor availability.
- [DCLTT] – Dynamic Closed Loop Thermal Throttling: For the SOD DIMM with system airflow input
- [SCLTT] – Static Close Loop Thermal Throttling: For the SOD DIMM without system airflow input
- [SOLTT] – Static Open Loop Thermal Throttling: For the DIMMs without sensor on DIMM (SOD)

4.2.2 Altitude

This option sets the proper altitude that the system will be used. Available settings include [300m or less], [301m-900m], [901m-1500m], and [Above 1500m].

Selecting an altitude range that is lower than the actual altitude the system will be operating at, can cause the fan control system to operate less efficiently, leading to higher system thermals and lower system performance. If the altitude range selected is higher than the actual altitude the system will be operating at, the fan control system may provide better cooling but with higher acoustics and higher fan power consumption. If the altitude is not known, selecting a higher altitude is recommended in order to provide sufficient cooling.

4.2.3 Set Fan Profile

This option sets the desired Fan Profile. Available settings include [Performance] and [Acoustic].

The Acoustic mode offers the best acoustic experience and appropriate cooling capability supporting the majority of the add-in cards used. Performance mode is designed to provide sufficient cooling capability covering all kinds of add-in cards on the market.

4.2.4 Fan PWM Offset

This option is reserved for manual adjustment to the minimum fan speed curves. The valid range is from [0 to 100] which stands for 0% to 100% PWM adding to the minimum fan speed. This feature is valid when Quiet Fan Idle Mode is at Enabled state. The default setting is [0].

4.2.5 Quiet Fan Idle Mode

This feature can be [Enabled] or [Disabled]. If enabled, the fans will either shift to a lower speed or stop when the aggregate sensor temperatures are satisfied, indicating the system is at ideal thermal/light loading conditions. When the aggregate sensor temperatures are not satisfied, the fans will shift back to normal control curves. If disabled, the fans will never shift to lower fan speed or stop, regardless of whether the aggregate sensor temperatures are satisfied or not. The default setting is [Disabled].

Note: The features above may or may not be in effect and depends on the actual thermal characteristics of the specified system.

4.2.6 Thermal Sensor Input for Fan Speed Control

The BMC uses various IPMI sensors as inputs to fan speed control. Some of the sensors are actual physical sensors and some are virtual sensors derived from calculations.

The following IPMI thermal sensors are used as input to fan speed control:

- Front Panel Temperature Sensor[1]
- Baseboard Temperature Sensor[2]
- CPU Margin Sensors[3, 5, 6]
- DIMM Thermal Margin Sensors[3, 5]
- Exit Air Temperature Sensor[1, 4, 8]
- PCH Temperature Sensor[4, 6]
- On-board Ethernet Controller Temperature Sensors[4, 6]
- Add-In Intel SAS/IO Module Temperature Sensors[4, 6]
- PSU Thermal Sensor[4, 9]
- CPU VR Temperature Sensors[4, 7]
- DIMM VR Temperature Sensors[4, 7]
- Integrated BMC Temperature Sensor[4, 7]
- Global Aggregate Thermal Margin Sensors[8]

Notes:

1. For fan speed control in Intel chassis
2. For fan speed control in 3rd party chassis
3. Temperature margin from throttling threshold
4. Absolute temperature
5. PECI value or margin value
6. On-die sensor
7. On-board sensor
8. Virtual sensor
9. Available only when PSU has PMBus

The following diagram illustrates the fan speed control structure.

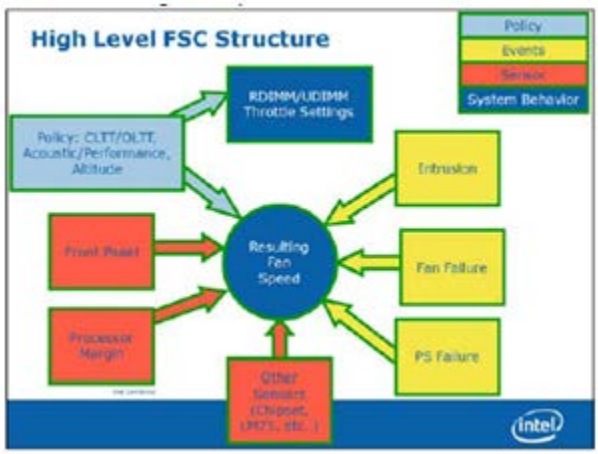


Figure 20. Fan Control Model

4.3 System Fans

Eleven system fans provide the primary airflow for the system. There are seven lower 40x56mm a dual rotor hot swap fans and four upper 40x56MM dual rotor hot swap fans. The system is designed for fan redundancy. If a single fan fails, the remaining system fans along with platform management will provide the necessary air flow and make other platform operating adjustments to maintain system thermals. Fan redundancy will be lost if more than one fan is in a failed state.

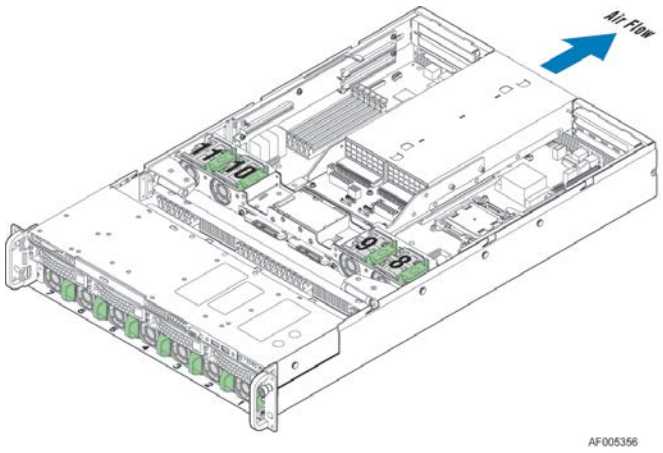


Figure 21. System Fan Identification

The system fan assembly is designed for ease of use and supports several features:

- Each fan is hot-swappable.
- Each fan is designed for tool-less insertion and extraction from the fan assembly. For instructions on installing or removing a fan module, see the *Intel® Server System R2000LH2/LT2 Service Guide*.
- Fan speed for each fan is controlled by integrated platform management as controlled by the integrated BMC on the server board. As system thermals fluctuate high and low, the integrated BMC firmware will increase and decrease the speeds to specific fans within the fan assembly to regulate system thermals.
- Each fan has a tachometer signal that allows the integrated BMC to monitor their status.
- Each fan has an integrated fault LED. Platform management illuminates the fault LED for the failing fan.

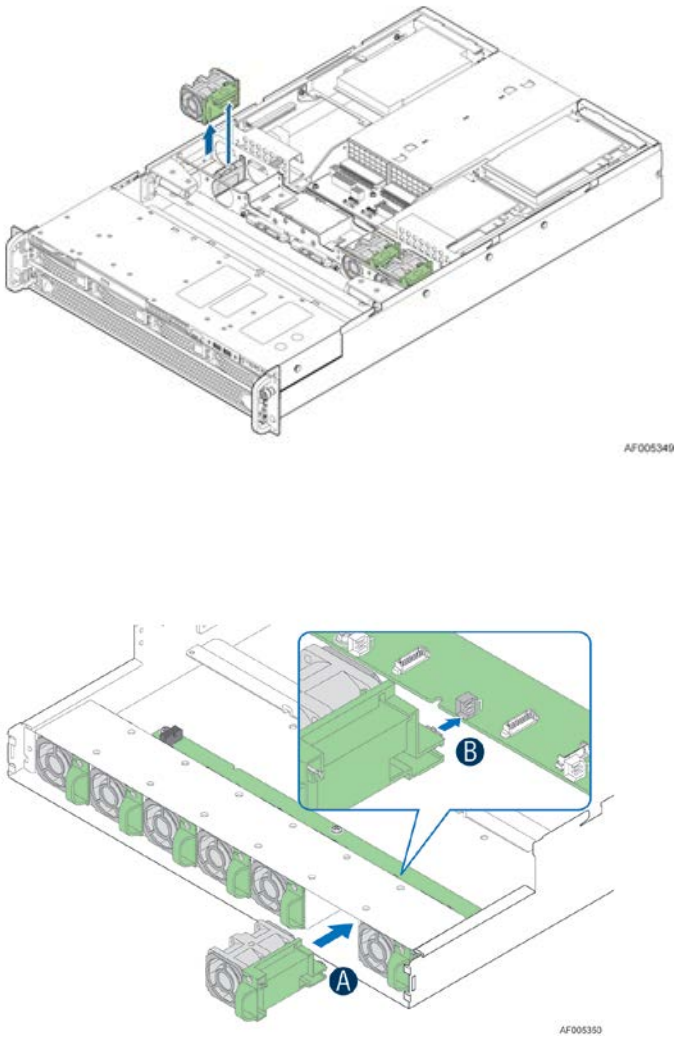


Figure 22. System Fan Assembly

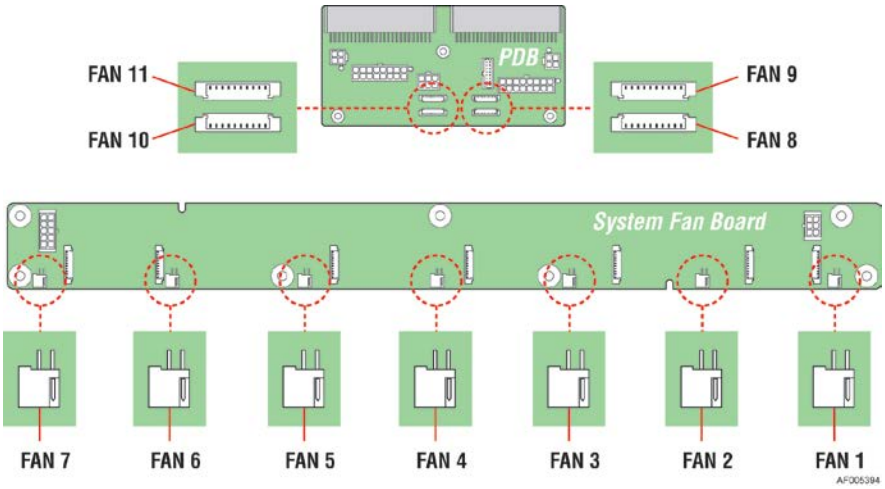


Figure 23. Upper and Lower System Fan Connections

4.3.1 Lower Fan Board

The lower fan board provides cooling for the lower half of the system. The Fan Board provides main 12V to lower seven 40x56mm dual rotor hot swap system fans. The board also provides the SMB interface for lower system fan monitoring and control, and provides power to the slim line DVD and 2x 2.5" SATA SSDs. Each fan has its own fan bracket which includes fan LED facing out of the front of the chassis. Additionally each fan has one PWM, two tachometer, one presence signal, 12V power, and ground. The board also provides SMB fan speed monitoring or control circuitry for seven 40mm dual rotor system fans (14 fan tachometers, 7 fan presence, and 7 fan fault LED signals).

Figure 24. Lower Fan Board

Table 24. Lower Fan Connector Pin-out

Pin #	Signal Description	Pin #	Signal Description
1	FAN_TACH_x_A	2	GND
3	FAN_TACH_x_B	4	FAN_FAULT_LED_x
5	FAN_PRESENT_x_N	6	FAN_PWM_y
7	P12V	8	Reserved

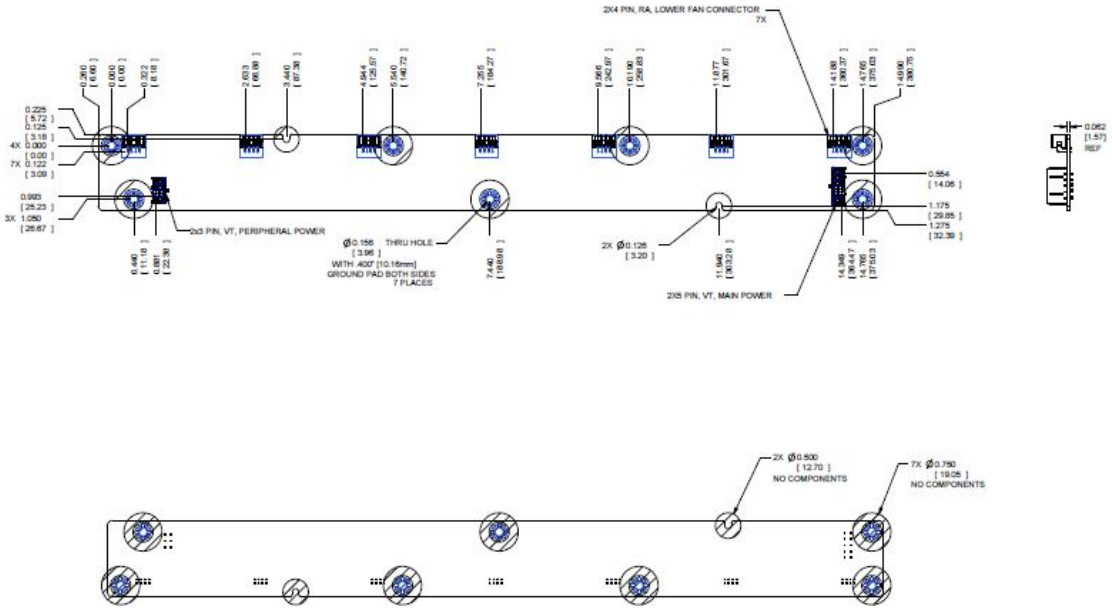


Figure 25. Lower Fan Board Dimensions

4.3.2 Upper Fans

The upper fans provide cooling for the upper half of the system. The upper fans derive power from and are connected to the Power Distribution Board (PDB). An SMBus fan monitoring device is also provided by the PDB.

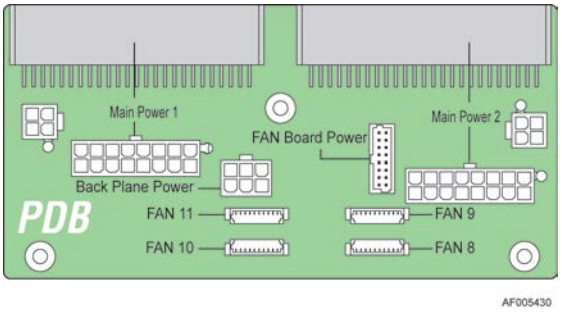


Figure 26. Upper Fans Connectors on PDB

Table 25. Upper Fan Connector Pin-out (Fans 8-11)

Pin #	Signal Description	Pin #	Signal Description
1	FAN_TACH_10_A	2	FAN_TACH_8_A
3	FAN_TACH_10_B	4	FAN_TACH_8_B
5	GND	6	GND
7	GND	8	GND

Pin #	Signal Description	Pin #	Signal Description
9	FAN_TACH_11_A	10	FAN_TACH_9_A
11	FAN_TACH_11_B	12	FAN_TACH_9_B
13	FAN_FAULT_LED_10	14	FAN_FAULT_LED_8
15	FAN_FAULT_LED_11	16	FAN_FAULT_LED_9
17	FAN_PRESENT_10	18	FAN_PRESENT_8
19	FAN_PRESENT_11	20	FAN_PRESENT_9
21	PWM_4	22	PWM_3
23	P12V	24	P12V2
25	P12V	26	P12V2

4.4 Power Supply Module Fan

Each installed power supply module includes one 40-mm fan. It is responsible for airflow through the power supply module. This fan is NOT managed by platform management. If this fan fails, the power supply will continue to operate until its internal temperature reaches an upper critical limit. The power supply will be protected against over temperature conditions caused by loss of fan cooling or excessive ambient temperature. In an over-temperature protection condition, the power supply module will shut down.

5. System Storage and Peripheral Drive Bays Overview

The Intel® Server System R2000LH2/LT2 product family supports many storage device options, including:

- Hot Swap 2.5” Hard Disk Drives
- Hot Swap 3.5” Hard Disk Drives
- SATA Optical Drive
- SATA Solid State Devices (SSDs)
- SATA DOMs
- Low Profile (2mm) eUSB Solid State Device (eUSB SSD)

Support for different storage and peripheral device options varies depending on the system SKU. This chapter provides an overview of each available option.

5.1 2.5” Hard Disk Drive Support

The server is available in 8 x 2.5” hard disk configurations illustrated below.

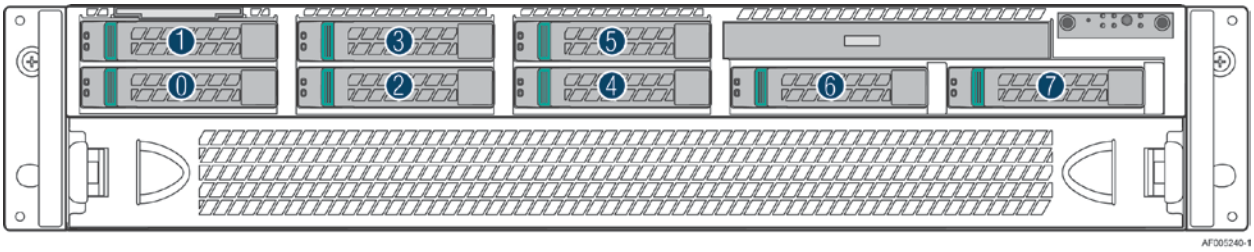


Figure 27. 8 x 2.5” Hard Drive Configuration

The drive bay can support either SATA or SAS hard disk drives. Mixing of drive types within the hard drive bay is not supported. Hard disk drive type is dependent on the type of host bus controller used, SATA only or SAS. Each 2.5” hard disk drive is mounted to a drive tray, allowing for hot swap extraction and insertion. Drive trays have a latching mechanism that is used to extract and insert drives from the chassis, and lock the tray in place.

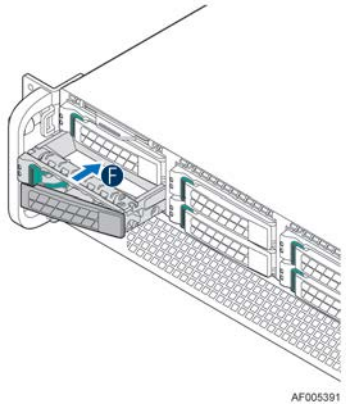


Figure 28. 2.5" Hard Disk Drive Assembly

Light pipes integrated into the drive tray assembly direct light emitted from Amber drive status and Green activity LEDs located next to each drive connector on the backplane, to the drive tray faceplate, making them visible from the front of the system.

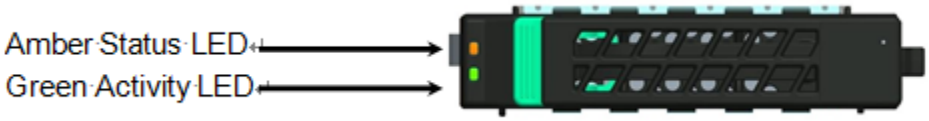


Figure 29. 2.5" Drive LEDs

Table 26. 2.5" Drive Status LED States

Amber	Off	No access and no fault
	Solid On	Hard Drive Fault has occurred
	Blink	RAID rebuild in progress (1 Hz), Identify (2 Hz)

Table 27. 2.5" Drive Activity LED States

	Condition	Drive Type	Behavior
Green	Power on with no drive activity	SAS	LED stays on
		SATA	LED stays off
	Power on with drive activity	SAS	LED blinks off when processing a command
		SATA	LED blinks on when processing a command
	Power on and drive spun down	SAS	LED stays off
		SATA	LED stays off
	Power on and drive spinning up	SAS	LED blinks
		SATA	LED stays off

5.1.1 2.5" Drive Hot-Swap Backplane Overview

The Hot-Swap SAS/SATA backplane serves as an interface between the mother board and the system drives. The following diagrams show the location for each connector found on the backplane. Each backplane is attached to the back of the drive bay assembly.

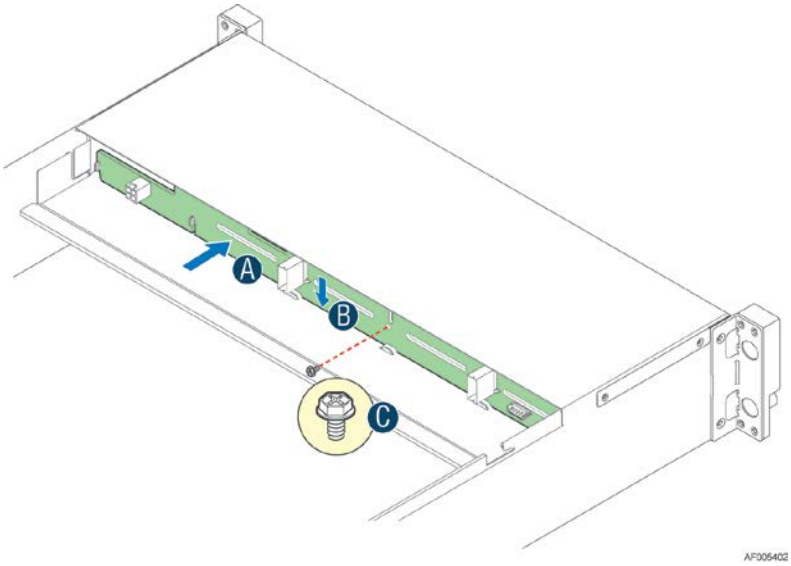


Figure 30. 2.5" Drive Hot-Swap Backplane Assembly

On the front side of each backplane are mounted eight hard disk drive hot swap interface connectors.

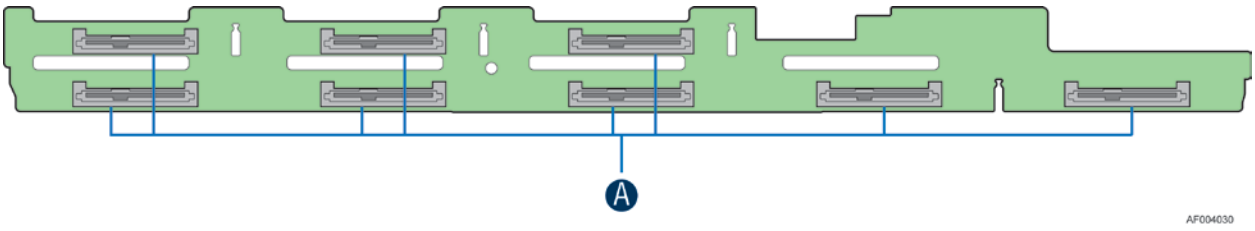


Figure 31. 2.5" Drive Hot-Swap Backplane – Front Side

On the back side of each backplane are several connectors. The following illustration identifies each.

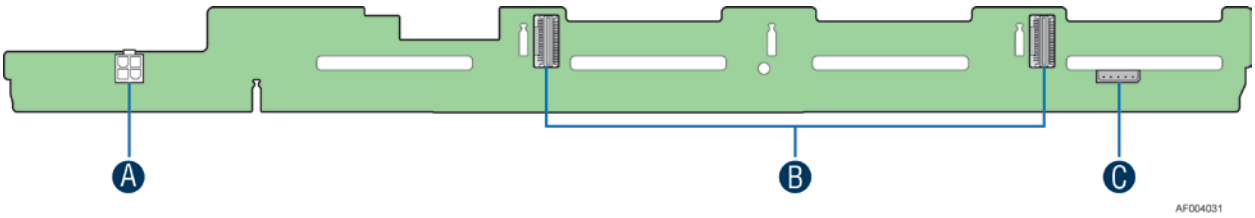


Figure 32. 2.5" Drive Hot-Swap Backplane – Back Side

Label	Description
A	Power connectors
B	4-port Mini-SAS cable connectors
C	I^2C connectors

5.2 3.5" Hard Disk Drive Support

The server is available in 4 x 3.5" hard disk configuration as illustrated below.

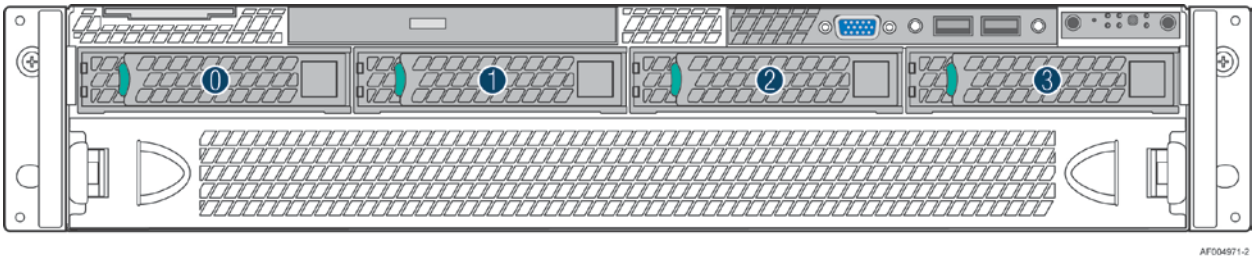


Figure 33. 4 x 3.5" Hard Drive Configuration

The drive bay can support either SATA or SAS hard disk drives. Mixing of drive types within the hard drive bay is not supported. Hard disk drive type is dependent on the type of host bus controller used, SATA only or SAS. Each 3.5" hard disk drive is mounted to a drive tray, allowing for hot swap extraction and insertion. Drive trays have a latching mechanism that is used to extract and insert drives from the chassis, and lock the tray in place.

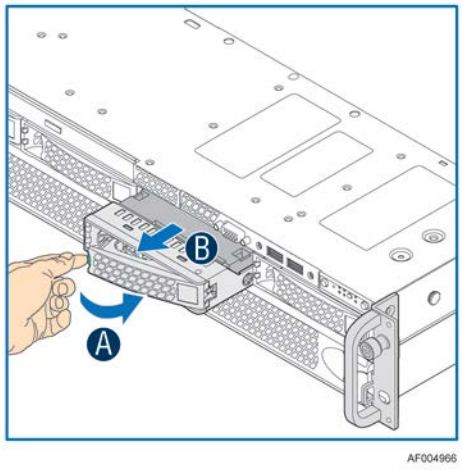


Figure 34. 3.5" Hard Disk Drive Assembly

Light pipes integrated into the drive tray assembly direct light emitted from Amber drive status and Green activity LEDs located next to each drive connector on the backplane, to the drive tray faceplate, making them visible from the front of the system.

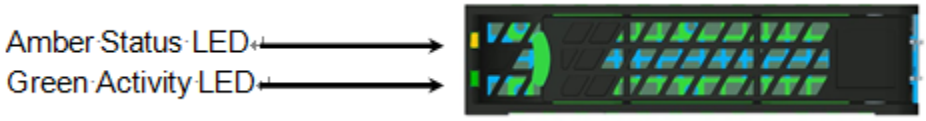


Figure 35. 3.5" Drive LEDs

Table 28. 3.5" Drive Status LED States

Amber	Off	No access and no fault
	Solid On	Hard Drive Fault has occurred
	Blink	RAID rebuild in progress (1 Hz), Identify (2 Hz)

Table 29. 3.5" Drive Activity LED States

	Condition	Drive Type	Behavior
Green	Power on with no drive activity	SAS	LED stays on
		SATA	LED stays off
	Power on with drive activity	SAS	LED blinks off when processing a command
		SATA	LED blinks on when processing a command
	Power on and drive spun down	SAS	LED stays off
		SATA	LED stays off
	Power on and drive spinning up	SAS	LED blinks
		SATA	LED stays off

5.2.1 3.5" Drive Hot-Swap Backplane Overview

The Hot-Swap SAS/SATA backplane serves as an interface between the mother board and the system drives. The following diagrams show the location for each connector found on the backplane. Each backplane is attached to the back of the drive bay assembly.

The backplanes mount to the back of the drive bay assembly.

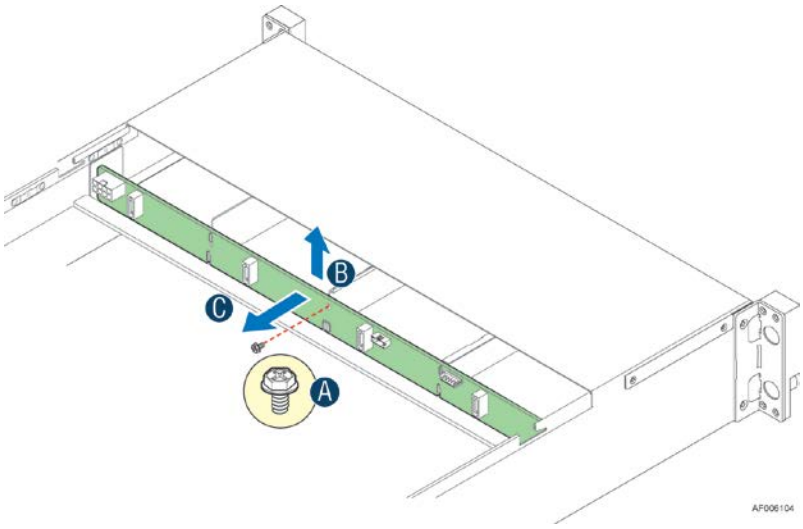


Figure 36. 3.5" Drive Hot-Swap Backplane Assembly

On the front side of the back plane are mounted four drive interface connectors.

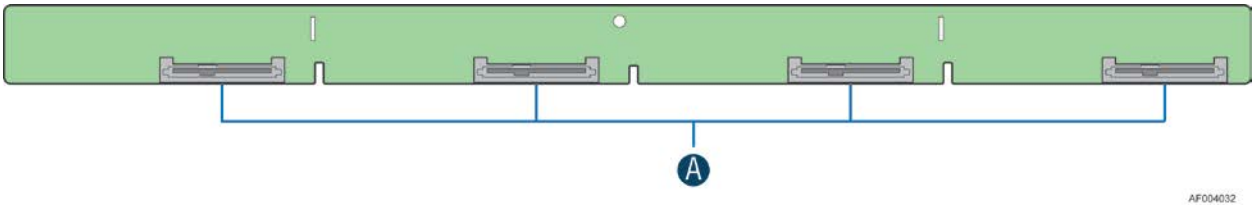


Figure 37. 3.5" Drive Hot-Swap Backplane – Front Side

Label	Description
A	Power connector

On the back side of each backplane are several connectors. The following illustration identifies each.

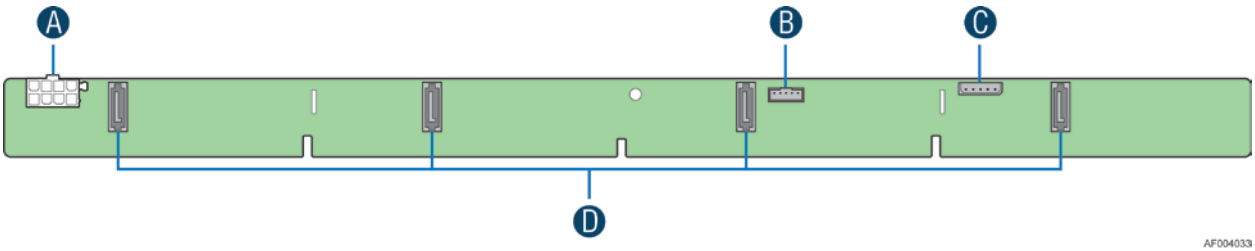


Figure 38. 3.5" Drive Hot-Swap Backplane – Back Side

Label	Description
A	Power connector
B	SGPIO connector
C	I^2C connector
C	SATA connectors

5.3 Optical Drive Support

Systems configured with four 3.5” hard drive bays or up to eight 2.5” hard drive bays also include support for an optical drive bay *A* as illustrated below.

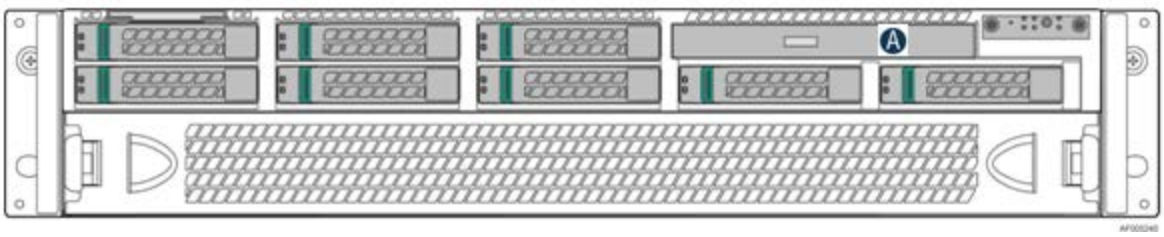


Figure 39. Optical Drive Support

The slimline optical drive carrier can be used with a single slimline optical drive. One slimline carrier is included with your server system; the optical drive must be purchased separately. The drive in the optical drive carrier is NOT hot-swappable. The system power must be turned off to insert or remove the slimline optical drive carrier. A 2x3 pin power connector on the server board labeled *ODD* is designed to provide power the SATA optical drive. The power cable is routed to the system fan board for power. The SATA cable routes along the right side of the chassis and is connected to SATA port 1 at the rear of the chassis.

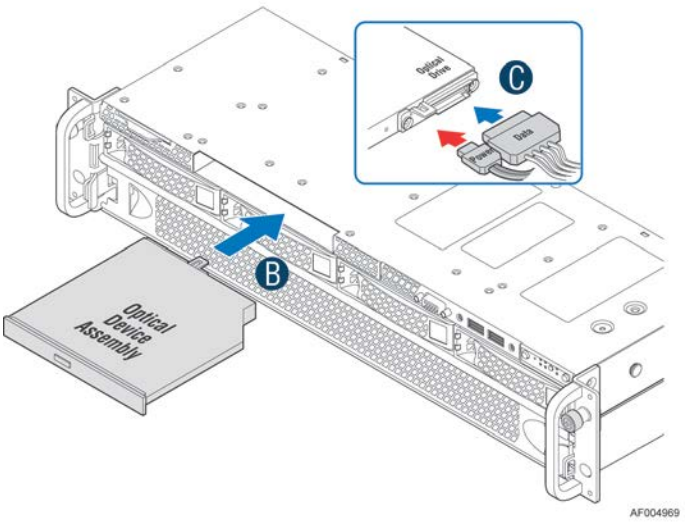


Figure 40. Optical Drive Assembly

5.4 Solid State Drive (SSD) Support

The system provides the option of supporting up to two internal fixed mount 2.5” Solid State Drives (SSD) to the top side of the system in front of the PDB.

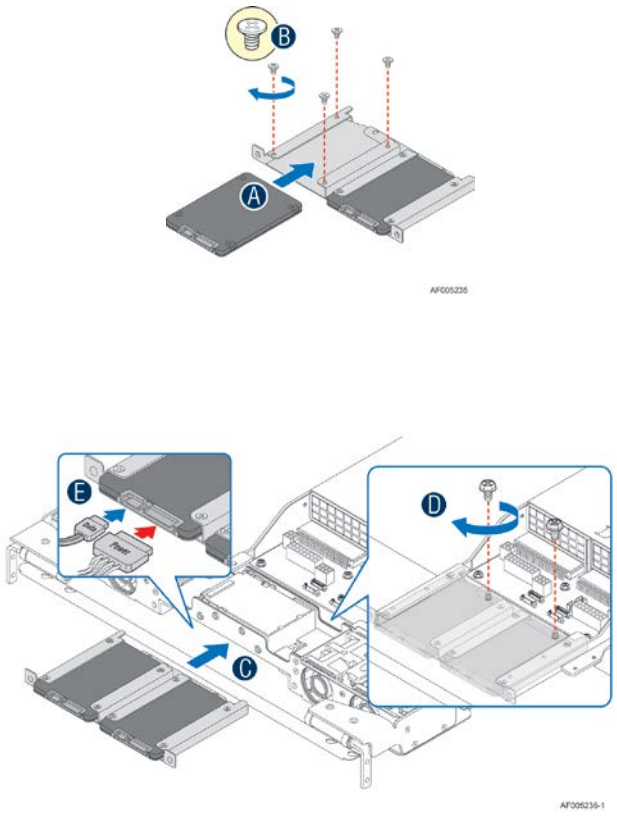
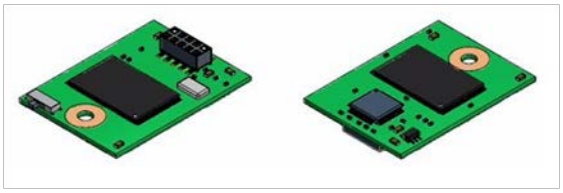


Figure 41. 2.5” Solid State Drive (SSD) Mounting Option

A 2x3 pin power connector on the server board labeled *ODD PWR* is designed to provide power to both SSDs or a single SSD and an optical drive. Using the supplied power harness, one power lead is routed to the optical drive bay, and two longer power leads are routed to the SSDs. When both SSDs are used, the SATA cables are routed to SATA Port 0 and SATA Port 1 at the right rear of the system. If an Optical Drive is used, only one SSD data and power is available.

5.5 Low Profile eUSB SSD Support

The system provides support for a low profile eUSB SSD storage device. A 2mm 2x5-pin connector labeled *eUSB SSD* near the rear I/O section of the server board is used to plug this small flash storage device into.



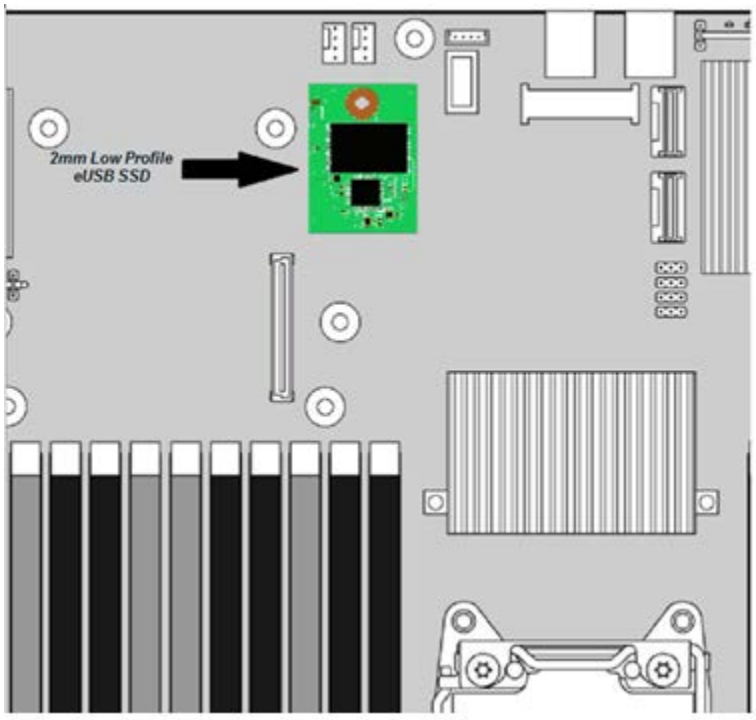


Figure 42. Low Profile eUSB SSD Support

eUSB features include:

- 2 wire small form factor Universal Serial Bus 2.0 (Hi-Speed USB) interface to host
- Read Speed up to 35 MB/s and write Speed up to 24 MB/s
- Capacity range from 256 MB to 32 GB
- Support USB Mass Storage Class requirements for Boot capability

5.6 SATA DOM Support

The system supports up to two vertical low profile Innodisk* SATA Disk-on-Module (DOM) devices.

Figure 43. InnoDisk* Low Profile SATA DOM

Each installed SATA DOM plugs directly into one of the 7-pin AHCI SATA ports on the server board, which provide both power and I/O signals.

6. Storage Controller Options Overview

The server platform supports many different embedded and add-in SATA/SAS controller and SAS Expander options to provide a large number of possible storage configurations. This chapter provides an overview of the different options available.

6.1 Embedded SATA/SAS Controller Support

Integrated on the server board is an Intel® C600-A chipset that provides embedded storage support via two integrated controllers: AHCI and SCU.

The standard server board (with no additional storage options installed) supports up to six SATA ports:

- Two single 6 Gb/sec SATA ports routed from the AHCI controller to two white 7-pin SATA ports labeled *SATA-0* and *SATA-1* on the server board. Embedded RAID levels 0 and 1 supported.
- Four 3 Gb/sec SATA ports routed from the SCU controller to the multi-port mini-SAS connector labeled *SCU_0 (0-3)*.

Note: The mini-SAS connector labeled "SCU_1 (4-7)" is NOT functional by default and is only enabled with the addition of an Intel® RAID C600 Upgrade Key option supporting 8 SAS/SATA ports.

With the addition of one of several available Intel® RAID C600 Upgrade Keys, the system is capable of supporting additional embedded SATA, SAS, and software RAID options. Upgrade keys install onto a 4-pin connector on the server board labeled *STOR_UPG_KEY*.

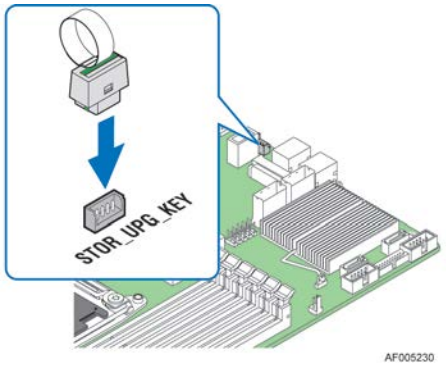


Figure 44. Embedded SATA/SAS Controller Support

The following table identifies available upgrade key options and their supported features.

Table 30. Intel® RAID C600 Upgrade Key Options

Intel® RAID C600 Upgrade Key Options (Intel Product Codes)	Key Color	Description
Default – No option key installed	N/A	4 Port SATA with Intel® ESRT RAID 0,1,10 and Intel® RSTe RAID 0,1,5,10
RKSATA4R5	Black	4 Port SATA with Intel® ESRT2 RAID 0,1, 5, 10 and Intel® RSTe RAID 0,1,5,10
RKSATA8	Blue	8 Port SATA with Intel® ESRT2 RAID 0,1, 10 and Intel® RSTe RAID 0,1,5,10
RKSATA8R5	White	8 Port SATA with Intel® ESRT2 RAID 0,1, 5, 10 and Intel® RSTe RAID 0,1,5,10
RKSAS4	Green	4 Port SAS with Intel® ESRT2 RAID 0,1, 10 and Intel® RSTe RAID 0,1,10
RKSAS4R5	Yellow	4 Port SAS with Intel® ESRT2 RAID 0,1, 5, 10 and Intel® RSTe RAID 0,1,10
RKSAS8	Orange	8 Port SAS with Intel® ESRT2 RAID 0,1, 10 and Intel® RSTe RAID 0,1,10
RKSAS8R5	Purple	8 Port SAS with Intel® ESRT2 RAID 0,1, 5, 10 and Intel® RSTe RAID 0,1,10

Additional information for the on-board RAID features and functionality can be found in the *Intel® RAID Software Users Guide* (Intel Document Number D29305-015).

6.2 Embedded Software RAID Support

The system supports two embedded software RAID options:

- Intel® Embedded Server RAID Technology 2 (ESRT2) based on LSI* MegaRAID SW RAID technology
- Intel® Rapid Storage Technology (RSTe)

Using the <F2> BIOS Setup Utility, accessed during system POST, options are available to enable/disable SW RAID, and select which embedded software RAID option to use.

6.2.1 Intel® Embedded Server RAID Technology 2 (ESRT2)

Features of the embedded software RAID option Intel® Embedded Server RAID Technology 2 (ESRT2) include the following:

- Based on LSI* MegaRAID Software Stack
- Software RAID with system providing memory and CPU utilization
- Supported RAID Levels – 0,1,5,10
  - 4 & 8 Port SATA RAID 5 support provided with appropriate Intel® RAID C600 Upgrade Key
  - 4 & 8 Port SAS RAID 5 support provided with appropriate Intel® RAID C600 Upgrade Key
- Maximum drive support = 8
- Open Source Compliance = Binary Driver (includes Partial Source files) or Open Source using MDRAID layer in Linux
- OS Support = Windows 7*, Windows 2008*, Windows 2003*, RHEL*, SLES, other Linux variants using partial source builds
- Utilities = Windows* GUI and CLI, Linux GUI and CLI, DOS CLI, and EFI CLI

6.2.2 Intel® Rapid Storage Technology (RSTe)

Features of the embedded software RAID option Intel® Rapid Storage Technology (RSTe) include the following:

- Software RAID with system providing memory and CPU utilization
- Supported RAID Levels – 0,1,5,10
  - 4 Port SATA RAID 5 available standard (no option key required)
  - 8 Port SATA RAID 5 support provided with appropriate Intel® RAID C600 Upgrade Key
  - No SAS RAID 5 support
- Maximum drive support = 32 (in arrays with 8 port SAS), 16 (in arrays with 4 port SAS), 128 (JBOD)
- Open Source Compliance = Yes (uses MDRAID)

- OS Support = Windows 7*, Windows 2008*, Windows 2003*, RHEL* 6.2 and later, SLES* 11 w/SP2 and later, VMWare 5.x.
- Utilities = Windows* GUI and CLI, Linux CLI, DOS CLI, and EFI CLI
- Uses Matrix Storage Manager for Windows
- MDRAID supported in Linux (Does not require a driver)

7. Front Control Panel and I/O Panel Overview

All system configurations include a Control Panel on the front of the system providing push button system controls and LED indicators for several system features. This chapter describes the features and functions of front panel options.

7.1 I/O Panel Features

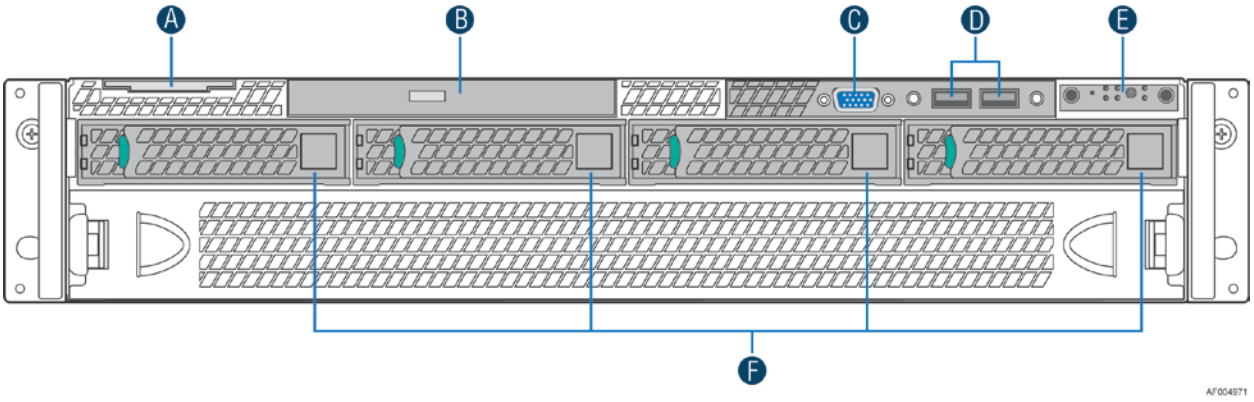


Figure 45. Front I/O Panel Features

Label	Description
A	Asset Tag
B	Slimline Optical Drive Bay
C	Video Port
D	USB Ports
E	Front Control Panel
F	Hard Disk Drive Bays

7.2 Control Panel Features

The system includes a control panel that provides push button system controls and LED indicators for several system features. Depending on the hard drive configuration, the front control panel may come in either of two formats; however, both provide the same functionality. This section provides a description for each front control panel feature.

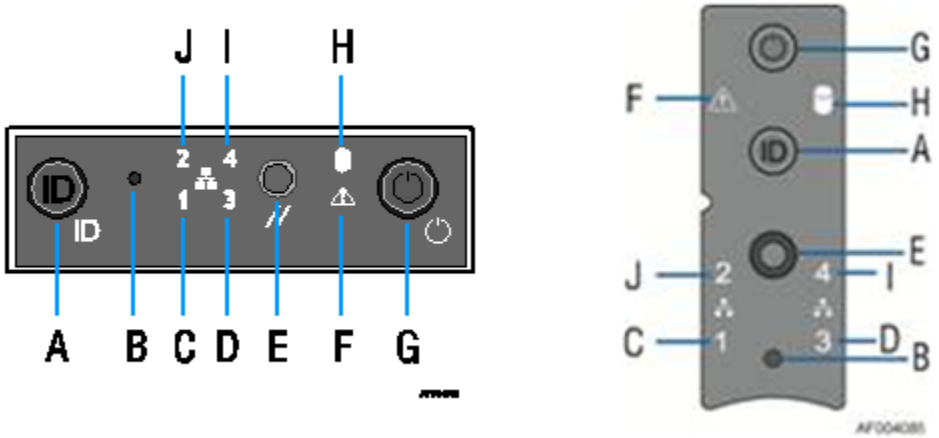


Figure 46. Front Control Panel Features

Label	Description	Label	Description
A	System ID Button w/Integrated LED	F	System Status LED
B	NMI Button (recessed, tool required for use)	G	Power / Sleep Button w/Integrated LED
C	NIC-1 Activity LED	H	Hard Drive Activity LED
D	Not Used	I	Not Used
E	System Cold Reset Button	J	NIC-2 Activity LED

- **A – System ID Button w/Integrated LED**: Toggles the integrated ID LED and the Blue server board ID LED on and off. The System ID LED is used to identify the system for maintenance when installed in a rack of similar server systems. The System ID LED can also be toggled on and off remotely using the IPMI *Chassis Identify* command which will cause the LED to blink for 15 seconds.
- **B – NMI Button**: When the NMI button is pressed, it puts the server in a halt state and issues a non-maskable interrupt (NMI). This can be useful when performing diagnostics for a given issue where a memory download is necessary to help determine the cause of the problem. To prevent an inadvertent system halt, the actual NMI button is located behind the Front Control Panel faceplate where it is only accessible with the use of a small tipped tool like a pin or paper clip.
- **C, D, I and J – Network Activity LEDs**: The Front Control Panel includes an activity LED indicator for each on-board Network Interface Controller (NIC). When a network link

is detected, the LED will turn on solid. The LED will blink once network activity occurs at a rate that is consistent with the amount of network activity that is occurring.

- **E – System Cold Reset Button**: When pressed, this button will reboot and re-initialize the system.
- **F – System Status LED**: The System Status LED is a bi-color (Green/Amber) indicator that shows the current health of the server system. The system provides two locations for this feature: one is located on the Front Control Panel, and the other is located on the back edge of the server board, viewable from the back of the system. Both LEDs are tied together and show the same state. The System Status LED states are driven by the on-board platform management subsystem. The following table provides a description of each supported LED state.

Table 31. System Status LED State Definitions

Color	State	Criticality	Description
Off	System is not operating	Not ready	1. System is powered off (AC and/or DC). 2. System is in EuP Lot6 Off Mode. 3. System is in S5 Soft-Off State. 4. System is in S4 Hibernate Sleep State.
Green	Solid on	Ok	Indicates that the System is running (in S0 State) and its status is 'Healthy'. The system is not exhibiting any errors. AC power is present and BMC has booted and manageability functionality is up and running.
Green	~1 Hz blink	Degraded - system is operating in a degraded state although still functional, or system is operating in a redundant state but with an impending failure warning	System degraded: Redundancy loss, such as power-supply or fan. Applies only if the associated platform sub-system has redundancy capabilities. Fan warning or failure when the number of fully operational fans is more than minimum number needed to cool the system. Non-critical threshold crossed – Temperature (including HSBP temp), voltage, input power to power supply, output current for main power rail from power supply and Processor Thermal Control (Therm Ctrl) sensors. Power supply predictive failure occurred while redundant power supply configuration was present. Unable to use all of the installed memory (one or more DIMMs failed/disabled but functional memory remains available) Correctable Errors over a threshold and migrating to a spare DIMM (memory sparing). This indicates that the user no longer has spared DIMMs indicating a redundancy lost condition. Corresponding DIMM LED lit. Uncorrectable memory error has occurred in memory Mirroring Mode, causing Loss of Redundancy. Correctable memory error threshold has been reached for a failing DDR3 DIMM when the system is operating in fully redundant RAS Mirroring Mode. Battery failure. BMC executing in uBoot. (Indicated by Chassis ID blinking at Blinking at 3Hz). System in degraded state (no manageability). BMC uBoot is running but has not transferred control to BMC Linux. Server will be in this state 6-8 seconds after BMC reset while it pulls the Linux image into flash BMC booting Linux. (Indicated by Chassis ID solid ON). System in degraded state (no manageability). Control has been passed

Color	State	Criticality	Description
			from BMC uBoot to BMC Linux itself. It will be in this state for ~10-~20 seconds. BMC Watchdog has reset the BMC. Power Unit sensor offset for configuration error is asserted. HDD HSC is off-line or degraded.
Amber	~1 Hz blink	Non-critical - System is operating in a degraded state with an impending failure warning, although still functioning	Non-fatal alarm – system is likely to fail: Critical threshold crossed – Voltage, temperature (including HSBP temp), input power to power supply, output current for main power rail from power supply and PROCHOT (Therm Ctrl) sensors. VRD Hot asserted. Minimum number of fans to cool the system not present or failed Hard drive fault Power Unit Redundancy sensor – Insufficient resources offset (indicates not enough power supplies present) In non-sparing and non-mirroring mode if the threshold of correctable errors is crossed within the window Correctable memory error threshold has been reached for a failing DDR3 DIMM when the system is operating in a non-redundant mode
Amber	Solid on	Critical, non-recoverable – System is halted	Fatal alarm – system has failed or shutdown: CPU CATERR signal asserted MSID mismatch detected (CATERR also asserts for this case). CPU 1 is missing CPU Thermal Trip No power good – power fault DIMM failure when there is only 1 DIMM present and hence no good memory present1. Runtime memory uncorrectable error in non-redundant mode. DIMM Thermal Trip or equivalent SSB Thermal Trip or equivalent CPU ERR2 signal asserted BMC\Video memory test failed. (Chassis ID shows blue/solid-on for this condition) Both uBoot BMC FW images are bad. (Chassis ID shows blue/solid-on for this condition) 240VA fault Fatal Error in processor initialization: Processor family not identical Processor model not identical Processor core/thread counts not identical Processor cache size not identical Unable to synchronize processor frequency Unable to synchronize QPI link frequency

- **G – Power/Sleep Button**: Toggles the system power on and off. This button also functions as a sleep button if enabled by an ACPI compliant operating system. Pressing this button will send a signal to the integrated BMC, which will either power on or power

off the system. The integrated LED is a single color (Green) and is capable of supporting different indicator states as defined in the following table.

Table 32. Power/Sleep LED Functional States

State	Power Mode	LED	Description
Power-off	Non-ACPI	Off	System power is off, and the BIOS has not initialized the chipset.
Power-on	Non-ACPI	On	System power is on.
S5	ACPI	Off	Mechanical is off, and the operating system has not saved any context to the hard disk.
S4	ACPI	Off	Mechanical is off. The operating system has saved context to the hard disk.
S3-S1	ACPI	Slow blink	DC power is still on. The operating system has saved context and gone into a level of low-power state.
S0	ACPI	Steady on	System and the operating system are up and running.

- **H – Drive Activity LED**: The drive activity LED on the front panel indicates drive activity from the on-board hard disk controllers. The server board also provides a header giving access to this LED for add-in controllers.

8. Intel® Local Control Panel

The Intel® Local Control Panel option (Intel Product Order Code – A1U2ULCP) utilizes a combination of control buttons and LCD display to provide system accessibility and monitoring.

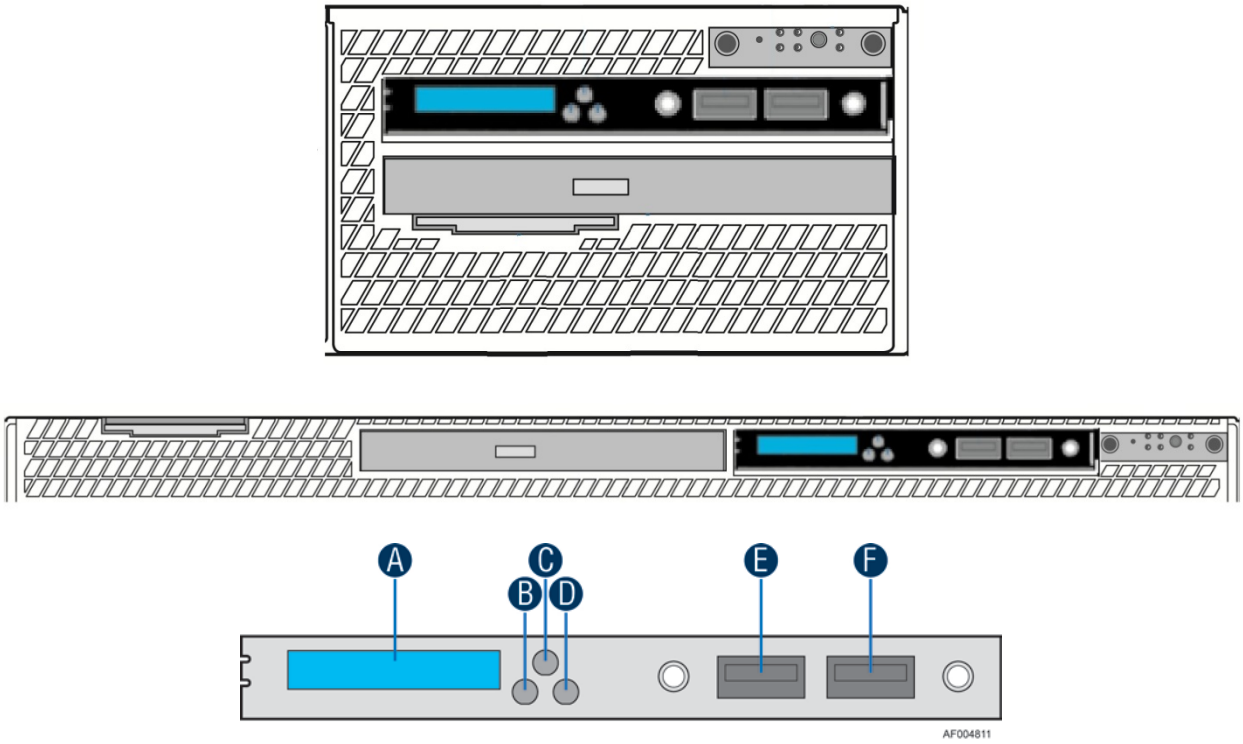


Figure 47. Intel® Local Control Panel Option

Label	Description	Functionality
A	LCD Display	One line 18 character display
B	Left Control Button	Moves the cursor backward one step or one character
C	Enter Button	Selects the menu item highlighted by the cursor
D	Right Control Button	Moves the cursor forward one step or one character
E	USB 2.0 Port	Connects external USB device
F	USB 2.0 Port	Connects external USB device

The LCD (Local Control Display) is a one line character display that resides on the front panel of the chassis. It can display a maximum of 18 characters at a time. This device also contains 3 buttons (Left, Right, and Enter). The user can select the content that needs to be displayed on the LCD screen by operating these buttons.

8.1 LCD Functionality

The LCD device provides the following features:

- Displays a banner when the system is healthy. The default banner is the server name.
- Displays active error messages when the system is not healthy.
- Provides basic server management configuration.
- Provides the ability to see asset information without having to open the chassis.

The LCD display is menu driven. Based on the user's selection, respective menu items are displayed. As soon as AC Power is applied to the system, the LCD panel displays faults detected while the system is on standby power prior to DC power on. If there are no faults, a banner is displayed. By default the banner is a text string which displays the Server Name. The Server Name is the value specified as the product name in the product FRU information in the BMC FRU. Users can set any of the parameters under the banner configuration menu as a banner string.

When the system's status is degraded, the corresponding active event will be displayed in place of the banner. During an error, the background color will be light amber in color. The LCD panel displays the event with the highest severity that is most recent and is currently active (for example, in an asserted state). For the case that there are multiple active events with the same severity, the most recent event will be displayed. The LCD panel returns to a light blue background when there are no longer any degraded, non-fatal, or fatal events active. The LCD panel shall operate in lock-step with the system status LED. For example, if the system is operating normally and an event occurs that results in the system status LED to blink green, the LCD will display the degraded event that triggered the systems status LED to blink.

Figure 48. LCP Background Color during Normal Operation

Figure 49. LCP Background Color during an Error

If the user presses any button after the system is powered on, the main menu will be displayed. The main menu contains **Evt**, **View**, and **Config** items. Based on the user's selection, respective sub menu items will be displayed. At any point of time, if there is no user intervention for more than 10 min, a default banner (if there is no active error event in the system) or an error event will be displayed.

The following sections discuss the individual menu items. In the following sections, it is assumed that no active event exists during the LCD display. If any event (fatal or non-fatal) occurs that degrades the system's performance, the color of the LCD background turns into light amber. Even though all the contents (full text) are shown in the example screen shots in the following sections, by default, only the first 18 characters are displayed when a particular menu item is selected. The remaining text can be viewed by using right or left buttons.

8.2 Main Menu

If the user presses any button, when the Banner/Error screen is displayed, the following main menu will get displayed. Using left and right scroll buttons, the curser can be moved under any one of the following four menu items.

Figure 50. LCP Main Menu

If the user selects menu item **^**, the LCD displays the previous screen, for example Banner/Error string. Selecting the menu item means, moving the cursor under that item using Left or Right buttons and pressing Enter button subsequently. In all the following sections (or for any screen shot), if the user presses Enter button, when the curser is under the symbol **^**, it takes to the previous screen. Selection of any of the menu items **Event**, **View**, or **Config**, leads the display to their corresponding screen shots and the details of these screen shots are given in the following sections.

8.3 Event Menu

In the **Event** menu, the LCD displays the following items. It displays all active error events in human readable text in chronological order. Informational events will not be displayed. There is no upper limit on the number of active events which can be displayed. The severity of the event will be indicated as either **Degraded**, **Non-Fatal**, or **Fatal**.

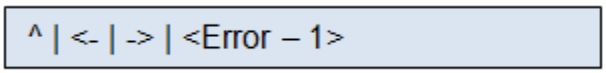


Figure 51. LCP Event Menu

The menu items **<-** and **->** are used to traverse among the events. Selection of the menu item **<-** displays the previous event and the item **->** displays the next event in human readable format. By default the first event after the last power on will be displayed. If there are no events after the last power on, the fourth field is empty on the LCD screen.

By default, each error event scrolls automatically so that the entire error message can be read without pressing either the left or right scroll buttons. To stop auto scrolling, cursor has to be brought under the event message and the Right button has to be pressed. Then the screen freezes. To start scrolling again Right button has to be pressed when the cursor is under the event message. So, when the cursor is under event message, the Right button decides whether to scroll or freeze the display of event message on the screen. When the cursor is under the event message, pressing Enter button displays the failing FRU (if any) in an easily human readable format for that error event. Pressing Enter button alternatively switches the display between error message and the failing FRU (if any) information of that error message alternatively. If there is no FRU device associated with that error, the Enter button has no effect when the cursor is under the error message. Left button moves the cursor under the previous token or menu item, for example **->**.

8.4 View Menu

The following screen is displayed when **View** is selected from the main menu.

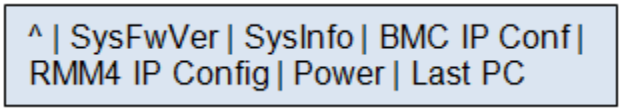


Figure 52. LCP View Menu

Based on the user's selection, details of the specific item will be displayed. The following sub sections explain the menu items above in detail.

8.4.1 System FW Version (SysFwVer)

Selection of the **SysFwVer** item in the **View** menu displays the current firmware versions of the system as shown below.

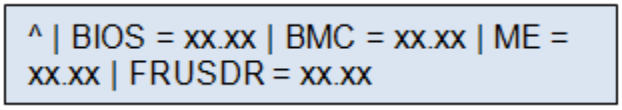


Figure 53. System Firmware Versions Menu

This is a leaf node and there is no further traversal below this menu. User can only go to the previous screen by selecting the item **^**. This applies to all the items of **View** menu.

8.4.2 System Information (SysInfo)

Selection of **SysInfo** item in the **View** menu displays the Server Name, Server Model, Server GUID, Asset Tag, and Custom String. It is also a leaf node. The blanks in the following display will be replaced by their values.

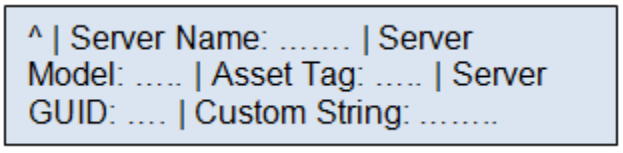


Figure 54. System Information Menu

Each field is explained as follows:

- Server Name: Value specified in the product name in the product FRU information in the main board BMC FRU.
- Server Model: Value specified in the product part number in the product FRU information in the main board BMC FRU.
- Asset tag: Value specified in the product asset tag in the product FRU information in the main board BMC FRU.
- Server GUID: System UUID stored by BIOS.
- Custom String: Custom string placed by the OEM end user.

8.4.3 BMC IP Configuration

Selection of **BMC IP Conf** item in the **View** menu displays the RMM4 IP configuration details. These details show whether the IP is configured using DHCP or Static, IP Address, Subnet Mask, and Gateway.

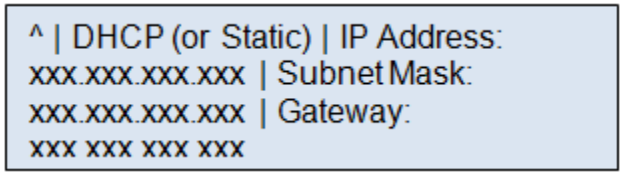


Figure 55. LCP – BMC IP Configuration

8.4.4 RMM4 IP Configuration

Selection of **RMM4 IP Conf** item in the **View** menu displays the BMC IP configuration details. These details show whether the IP is configured using DHCP or Static, IP Address, Subnet Mask, and Gateway.

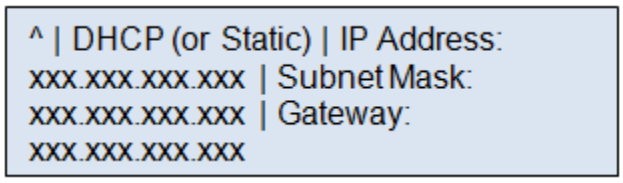


Figure 56. LCP – RMM4 IP Configuration

8.4.5 Power

Selection of **Power** item in the **View** menu displays the amount of AC power drawn by the system in Watts.

Figure 57. LCP – Power Consumed by the System Currently

8.4.6 Last Post Code (Last PC)

Selection of **Last PC** item in the **View** menu displays the last BIOS POST code in hexadecimal.

Figure 58. LCP – Last BIOS Post Code

8.5 Config Menu

If the user selects **Config** item in the main menu, the following options will be displayed to configure.

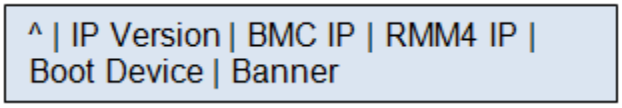


Figure 59. LCP – Configure Menu Items

The following subsections explain individual items of the configuration menu.

8.5.1 IP Version

If the user selects **IP Version** in the **Config** menu, the following options will be displayed. Based the user's selection, firmware will set the IP Version as either IPv4 or IPv6.

Figure 60. LCP – IP Version Configuration Screen

8.5.2 BMC IP

If the user selects **BMC IP** item in the **Config** menu, the following options will be displayed.

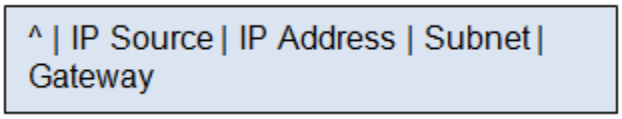


Figure 61. LCP – BMC IP Configuration Menu

Selection of the **IP Source** in the menu above leads to the following screen. Based on the user's selection in the following menu, the firmware sets the BMC IP source as either DHCP or Static.

Figure 62. LCP – BMC IP Source Configuration Menu

If the user selects DHCP or the existing IP source is DHCP, the other menu items such as IP Address, Subnet, and Gateway are not configurable. If the user selects Static or the existing setting is static for IP source, the user is allowed to change the other menu items and the screen shots look as follows.

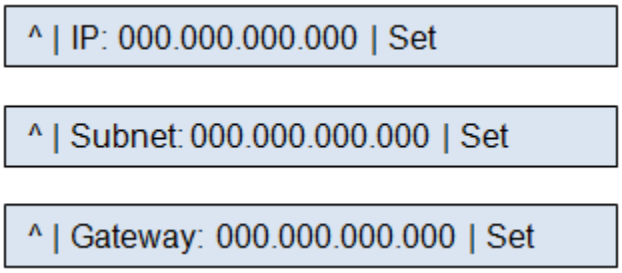


Figure 63. Screen shots for Configuring IP Address, Subnet Mask, and Gateway

By default the cursor will be under the symbol **^** and the IP address is displayed as 000.000.000.000. A Right button will take the cursor to the first position (first 0) of the IP address. When the cursor is under the second menu item, the functionality of Left, Right, and Enter buttons is different from the previous screens. The second token consists of twelve 0 s' separated by period (.) character in IP address format. The behaviors of these buttons are as follows when the cursor is under this item:

- Left and Right buttons inside the second menu item traverse among the 0 positions within the same item.
- If the cursor is under the last position inside the second menu item, a Right button will move the cursor to next item, that is, **Set**.
- If the cursor is under the first position inside the second menu item, a Left button moves the cursor to the previous item, that is, **^**.
- First Enter button at any **0** position makes that position to be selected to increase or decrease the value at that position. The values allowed are between and including 0 and 9.
- Any further Left or Right buttons will decrease or increase the value at that position.
- The second Enter button at that position makes the cursor to be ready for moving left or right. Any further Left or Right button moves the cursor to the previous or next position respectively.
- The Enter button is used to select a position at the first time and to leave the position at the second time.

The following state transition diagram explains the previous steps pictorially, while setting an IP address using the LCD device. After entering an IP address, the user has to select **Set** item to set the entered IP address to the corresponding parameter (IP Address, Subnet Mask, or Gateway).

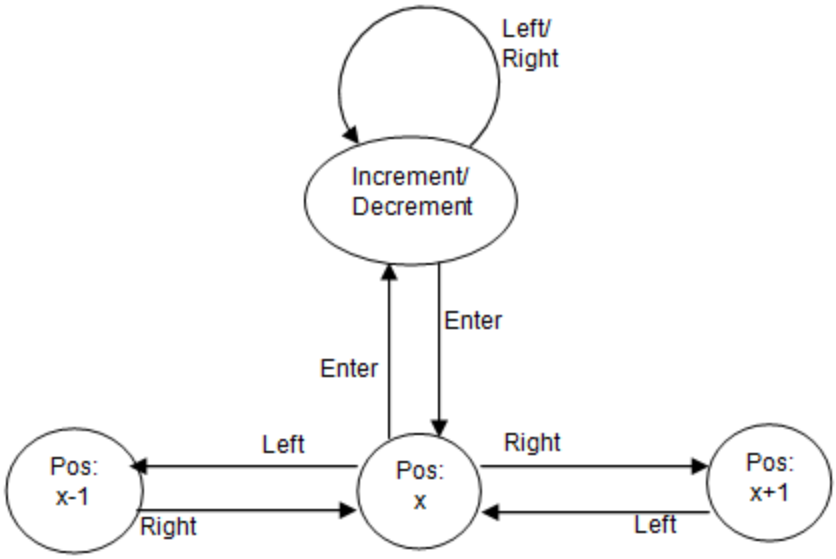


Figure 64. State Transition Diagram for Setting IP Address

8.5.3 RMM4 IP

The screen shots and the description of the previous section (for **BMC IP** menu) are also applicable for **RMM4 IP** configuration menu.

8.5.4 Boot Device

If the user selects **Boot Device** in the **Config** menu, the following options will be displayed. The selected item will be set as the next boot option and it will not be a permanent change.

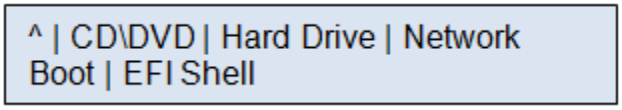


Figure 65. Boot Options Configuration Menu

8.5.5 Banner

When the user selects **Banner** in the **Config** menu, the following options will be displayed. The selected item will be set as banner and the same will be displayed from next banner screen onwards.

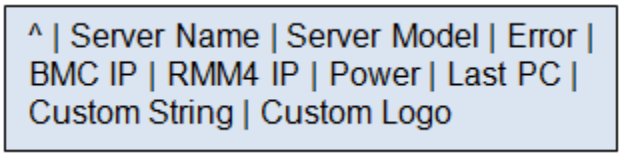


Figure 66. Banner Configuration Menu

Each menu item is explained as follows:

- Server Name: Displays the value specified in the product name in the product FRU information in the main board BMC FRU. The Server Name is the default banner.
- Server Model: Displays the value specified in the product part number in the product FRU information in the main board BMC FRU.
- Error: Displays the last active system event. The last active event may be degraded, non-critical, or critical only. It will not display an informational message. If the system is healthy then displays **System Health Ok**.
- BMC IP: Displays the IPv4 or IPv6 address of BMC IP. If the BMC IP address is not configured, nothing is displayed.
- RMM4 IP: Displays the IPv4 or IPv6 address of RMM4 dedicated LAN IP. If the RMM4 IP is not set or not present, nothing is displayed.
- Power: Displays the current system power consumption in watts. The power consumed will be refreshed every minute.
- Last PC: Displays last BIOS post code.
- Custom string: Displays a customizable text string. The custom text string is modifiable through BIOS setup.
- Custom Logo: Displays a customizable bitmap logo. The OEM customized logo is programmed by the OEM and maintained during subsequent firmware updates.

For additional information, see the *Intel® Local Control Panel for EPSD Platforms Based on the Intel® Xeon® Processor E5 -4600/2600/2400/1600/1400 Product Families Technical Product Specification*.

9. PCI Riser Card Support

The system includes two riser card slots on the server board. Available riser cards can be used in either slot. This chapter provides an overview of each available riser card and describes the server board features and architecture supporting them.

9.1 Riser Slot Overview

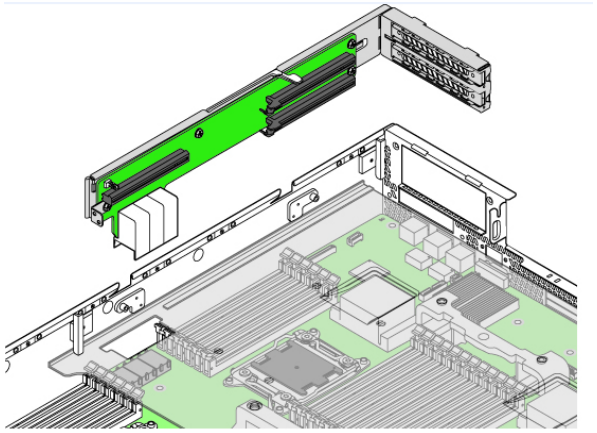
The server system supports two 3-slot riser cards identified by IO Riser 1 (Right) and IO Riser 2 (Left). The two 3- slot PCIe Risers each support up to x48 lanes of PCIe Gen3 through a custom interconnect (3 connector blocks at 120 pins per connector, 360pins total).The PCIe signals for each riser card slot are supported each by two installed processors.

Additional support:

- One double wide GPGPU or Graphics card per riser (up to 300W active supported, passive not supported)

  OR
- Two single wide GPGPU or Graphics cards per riser (up to 150W active supported; passive not supported)

  OR
- Two single wide full height, full length (FHFL) cards per riser (25W supported for each) OR
- Three single wide full height, half length (FHHL) cards per riser (one of these are internal only slots). Un-shadowed PCIe slots support 25W each and shadowed supports 10W each
- 3.3V VR for PCIe card power is located on the riser



AF004991-1

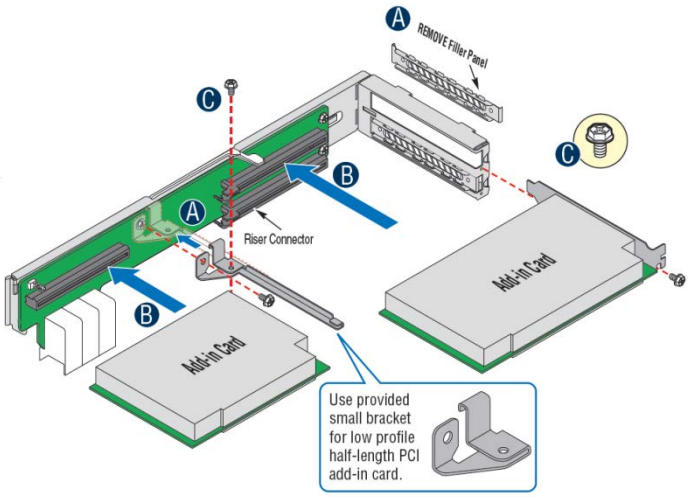


Figure 67. PCIe Risers and Add-in Cards

9.2 GPGPU Support on the PCIe Risers

9.2.1 GPGPU Power

The power to the GPGPUs is supplied via the PCIe Riser Slot and the Power Distribution Board. The 300w GPGPU power requirements are satisfied by:

- 75W from the PCIe connector
- 225W from the auxiliary connector on the Power Distribution Board (PDB)

The PDB auxiliary power connectors, J9 (Left) and J10 (Right), labeled *for GFX add-in card*, provide auxiliary power to GPGPU devices.

Table 33. GPGPU Aux Connector Pin-out (J9 and J10)

Pin #	Signal Description	Pin #	Signal Description
1	GROUND	13	P12V1/2
2	GROUND	14	P12V1/2

9.2.2 GPGPU Cable

The GPGPU cable uses the mini-Fit Jr HCS contact that is rated for 9.5A for a four circuit connector. Power delivery is 2 contacts * 9.5A * 12V = 240W. Since the cable needs to support 225W and the cable can support 228W, there is a 3W margin.

Note: The GPU power cable is not a productized component. Contact your Intel support representative for information on how to obtain the GPGPU power cables.

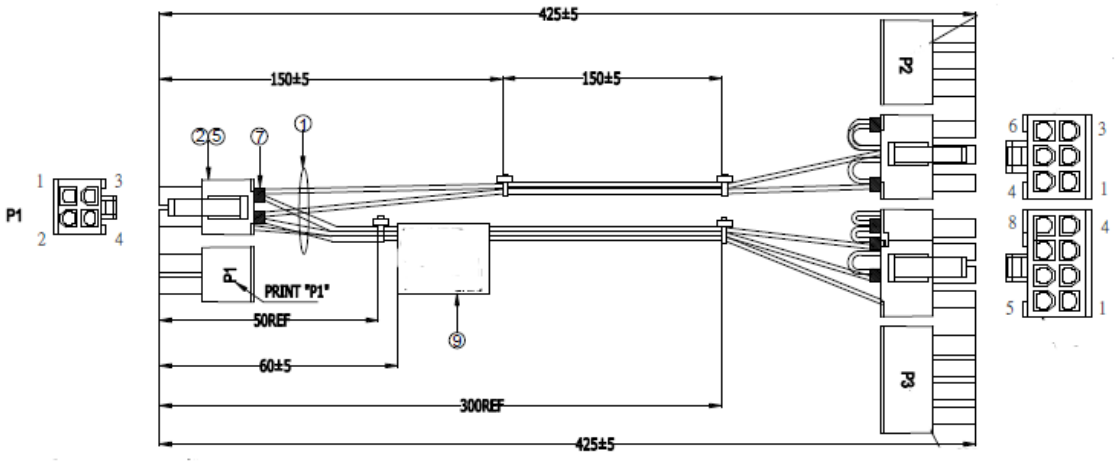


Figure 68. GPGPU Cable

9.3 Wattage Limitation of the PCI Loading

The following table summarizes the wattage limitation of the PCI loading.

Table 34. Wattage Limitation of PCIe Loading

VIN	Power Supply Configuration	Maximum PCI Loading
90 – 140VAC (AC low-Line)	1600W (1+1) Redundant Hot-swap Capable	260 W
	1600W (1+0 or 2+0) Non-Redundant	
180 – 264VAC (AC high-line)	1600W (1+1) Redundant Hot-swap Capable	450 W
	1600W (1+0 or 2+0) Non-Redundant	

9.4 Riser Slot Mapping

A total of 48 PCIe Gen3 signals are routed to each of the IO Risers. For IO Riser 1 (Right) there are 16 lanes from CPU 1 and 32 lanes from CPU 4. For IO Riser 2 (Left), there are 16 lanes from CPU 2 and 32 lanes from CPU 3.

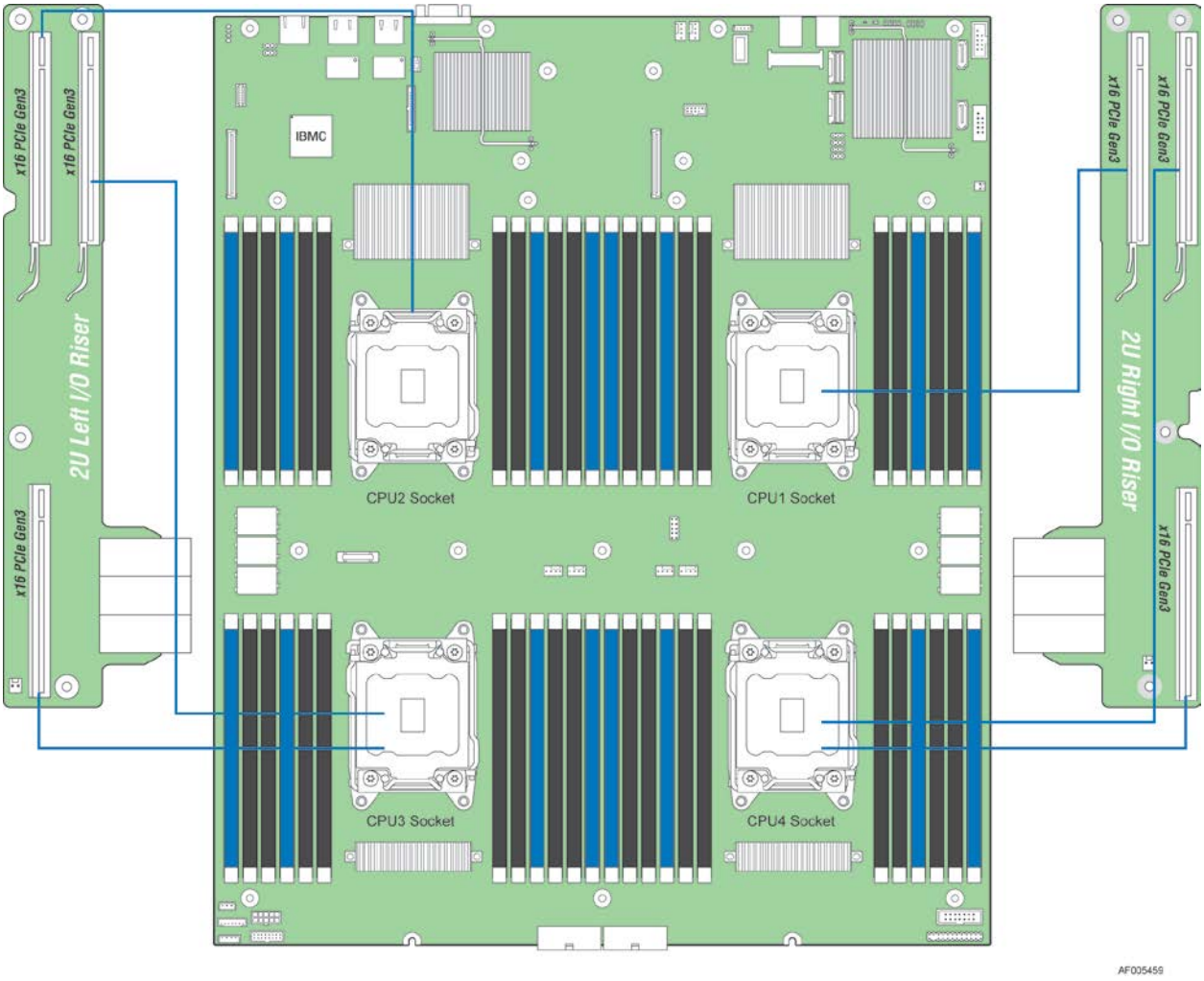


Figure 69. IO Riser CPU Mapping

9.5 Riser Card Drawing

The Right and Left Riser Card drawings are shown in scale 1500.

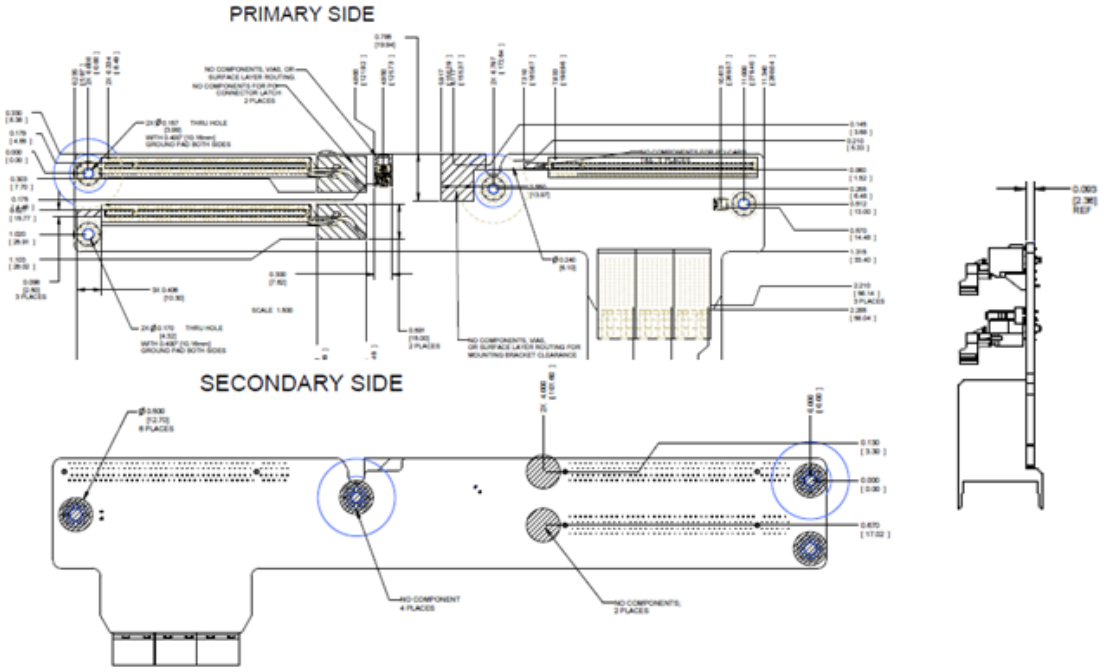


Figure 70. Right Riser Card Drawing

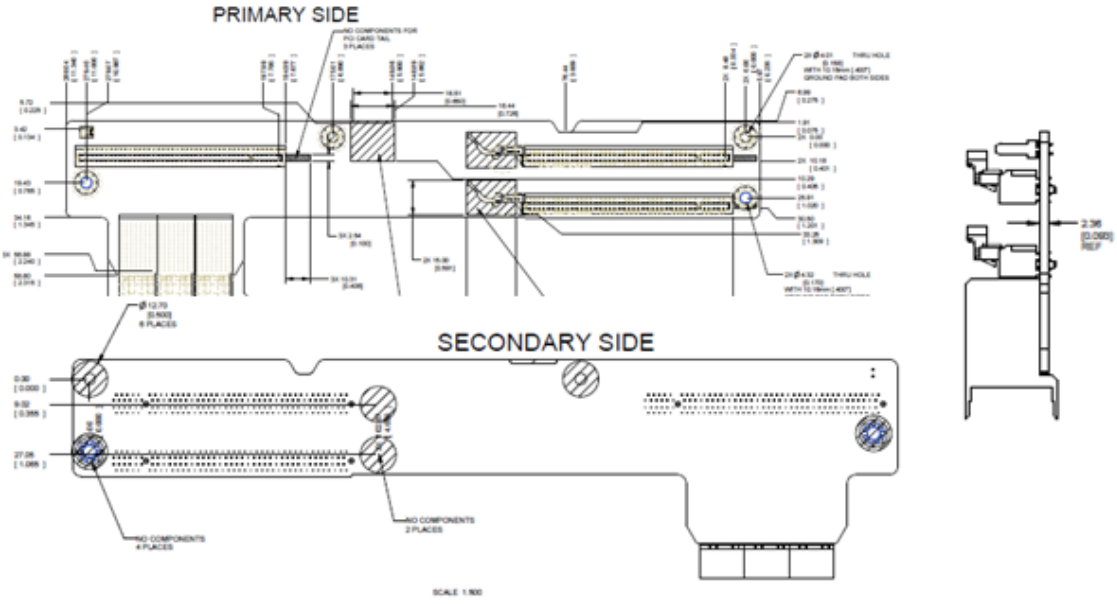


Figure 71. Left Riser Card Drawing

10. Additonal System Boards

This chapter provides additional information on other minor server boards in Intel® Server System R2000LH2/T2.

10.1 Power Distribution Board (PDB)

This specification defines the Power Distribution Board (PDB) for using in the Swan Peak chassis with the Lizard Head Pass motherboard. The PBD supports two 1600W AC or DC power supplies in a 2+0 non-redundant or 1+1 redundant configuration. The PDB has no electrical circuit. It only contains connectors and two pull-down resistors.

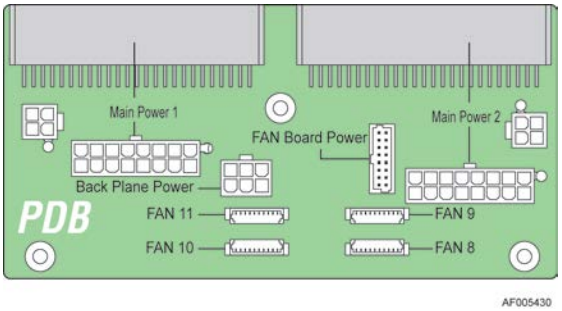


Figure 72. PDB

10.2 Setting the Power Supply Addressing for PMBus and FRU

The PDB has weak pull-down resistors (10K Ω) on the PSU SMBus addressing pins for A0 and A1.

10.3 12V Over Current Protection

The PDB has three 12V over current protection circuits. Two are limited to <100A to protect against catastrophic failures. They rely on the PSUs shutting down in <50msec (supported on the CRPS family of power supplies). One is a 240VA channel limited to < 20A for protection against safety energy hazards. Below is a summary of which components are on each 12V rail.

10.3.1 Over Current Protection Circuits

There are three over current protection circuits; two for high power rails and one for 240VA lower power protection. The PSON# signal will be de-asserted when over current limit is exceeded.

Table 35. Over Current Protection Circuits

Output Voltage	Min OCP Trip Limits	Max OCP Trip Limits	Min Trip Delay	Max Trip Delay
+12V1	80 A	100 A	1 msec	10 msec
+12V2	80 A	100 A	1 msec	10 msec
+12V3	18 A	20 A	1 msec	10 msec

10.4 Power Supply Keying

The power distribution board has no keying features for the power supply. The power supply keying is accomplished via the chassis sheet metal, not the PDB connector.

10.5 PDB Connectors

The power distribution board has no keying features for the power supplies. The power supply keying is accomplished via the chassis sheet metal, not the PDB connector.

10.5.1 Grounding

The ground of the pins of the PDB output connectors provides the power return path. The output connector ground pins are connected to safety ground (PDB enclosure).

10.5.2 Power Supply Card Edge Connectors

There are two (P8 and P9) power connectors connecting the power supplies to the PDB.

Table 36. Power Supply Card Edge Connector Pin-out P8 and P9

Pin #	Signal Description	Pin #	Signal Description
A1	GND	B1	GND
A2	GND	B2	GND
A3	GND	B3	GND
A4	GND	B4	GND
A5	GND	B5	GND
A6	GND	B6	GND
A7	GND	B7	GND
A8	GND	B8	GND
A9	GND	B9	GND
A10	+12V	B10	+12V
A11	+12V	B11	+12V
A12	+12V	B12	+12V
A13	+12V	B13	+12V
A14	+12V	B14	+12V
A15	+12V	B15	+12V
A16	+12V	B16	+12V
A17	+12V	B17	+12V
A18	+12V	B18	+12V
A19	PMBus SDA	B19	A0 (SMBus address)
A20	PMBus SCL	B20	A1 (SMBus address)
A21	PSON	B21	12V stby
A22	SMBAlert#	B22	Cold Redundancy Bus
A23	Return Sense	B23	12V load share bus
A24	+12V remote Sense	B24	No Connect
A25	PWOK	B25	Compatibility Check pin*

10.5.3 Motherboard Power Connectors

There are two power connectors (J8 and J6) connecting main power from the PDB to the motherboard.

Main power to the server board power is supplied via two power connectors, connecting main power from the PDB to the motherboard. Each connector is labeled as *J8* and *J6* on the PDB. The following tables provide the pin-out for both connectors.

Table 37. Main Power (J8) Connector Pin-out

Pin #	Signal Description	Pin #	Signal Description
1	GROUND	9	P12V1/2
2	GROUND	10	P12V1/2
3	GROUND	11	P12V1/2
4	GROUND	12	P12V1/2
5	GROUND	13	P12V1/2
6	GROUND	14	P12V1/2
7	GROUND	15	P12V1/2
8	GROUND	16	P12V1/2

Table 38. Main Power (J6) Connector Pin-out

Pin #	Signal Description	Pin #	Signal Description
1	GROUND	9	P12V1/2
2	GROUND	10	P12V1/2
3	GROUND	11	P12V1/2
4	GROUND	12	P12V1/2
5	GROUND	13	P12V1/2
6	GROUND	14	P12V1/2
7	GROUND	15	P12V1/2
8	GROUND	16	P12V1/2

10.5.4 Motherboard Signal from PDB

Power control signals are routed via connector J5. The connector provides signal and 12Vstby interface from the PDB to the motherboard. The 3.3Vstby and 3.3V pins are provided to allow 3.3V power to the fan monitoring circuit the PDB. The SMBus interface from the fan monitoring circuit is routed from the PDB to the motherboard through this connector.

Table 39. Power Control Signals Pin-out (J5)

Pin #	Signal Description	Pin #	Signal Description
1	P3V3_STBY	9	Return_Sense
2	P3V3	10	P12V_Remote_Sense
3	PMBUS_SCL	11	P12V_STBY
4	PMBUS_SDA	12	P12V_STBY
5	PSON#	13	P12V_STBY
6	PWOK	14	P12V_STBY
7	SMBAlert#	15	FAN_SCL
8	Reserved	16	FAN_SDA

10.5.5 GPGPU Power Connectors

PDB auxiliary power connectors, J9 (Left) and J10 (Right), labeled *for GFX add-in card*, provide auxiliary power to GPGPU devices.

Table 40. GPGPU Aux Connector Pin-out (J9 and J10)

Pin #	Signal Description	Pin #	Signal Description
1	GROUND	13	P12V1/2
2	GROUND	14	P12V1/2

10.5.6 Upper Fan Connector

The upper fans provide cooling for the upper half of the system. The upper fans derive power from and are connected to the Power Distribution Board (PDB). An SMBus fan monitoring device is also provided by the PDB.

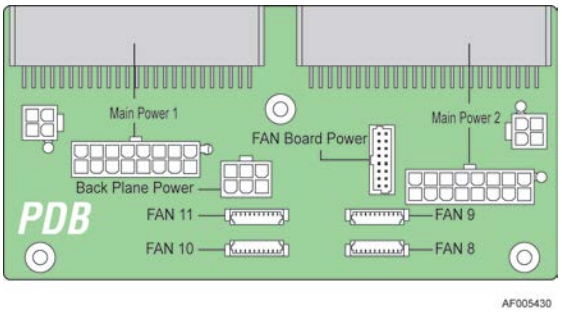


Figure 73. Upper Fans Connectors on PDB

Table 41. Upper Fan Connector Pin-out (Fans 8-11)

Pin #	Signal Description	Pin #	Signal Description
1	FAN_TACH_10_A	2	FAN_TACH_8_A
3	FAN_TACH_10_B	4	FAN_TACH_8_B
5	GND	6	GND
7	GND	8	GND
9	FAN_TACH_11_A	10	FAN_TACH_9_A
11	FAN_TACH_11_B	12	FAN_TACH_9_B
13	FAN_FAULT_LED_10	14	FAN_FAULT_LED_8
15	FAN_FAULT_LED_11	16	FAN_FAULT_LED_9
17	FAN_PRESENT_10	18	FAN_PRESENT_8
19	FAN_PRESENT_11	20	FAN_PRESENT_9
21	PWM_4	22	PWM_3
23	P12V	24	P12V2
25	P12V	26	P12V2

10.6 PDB Drawing

The PDB is 148mm wide x 74mm deep.

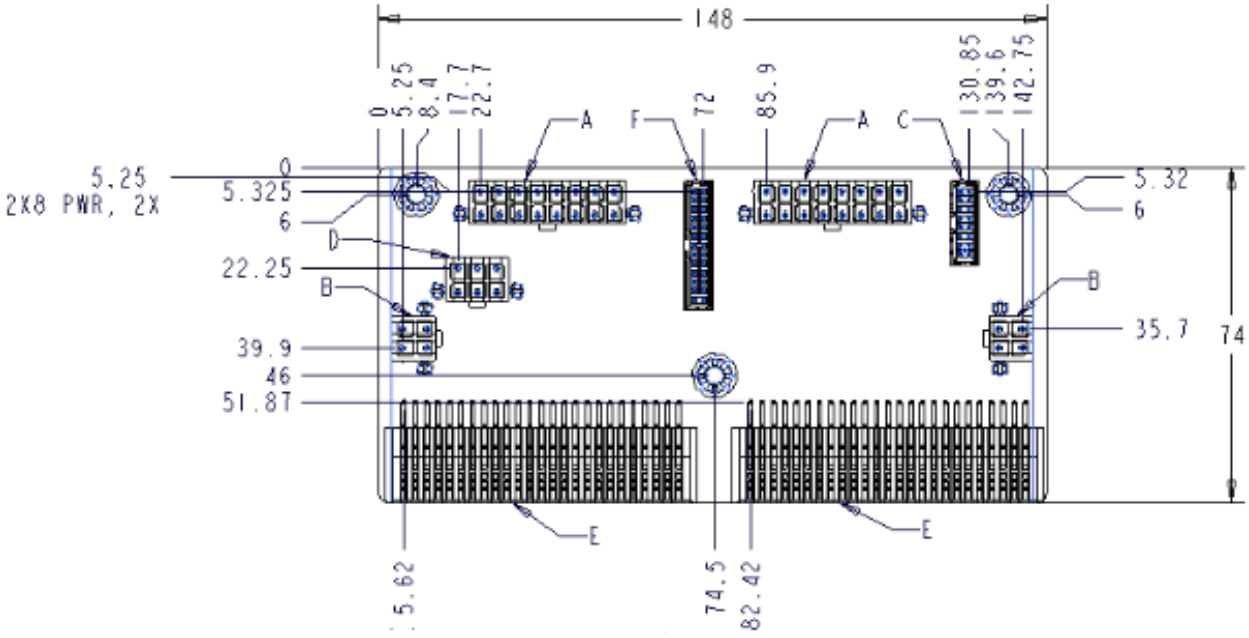


Figure 74. PDB Drawing

11. Front Panel

The common front panel feature set conforms to the industry standard SSI 2x12 connector specification, but includes an extension to this connector to support 3rd and 4th NIC Activity LEDs. The longer connector is a 2x15 right angle header, which includes missing pin locations at pins 25 & 26.

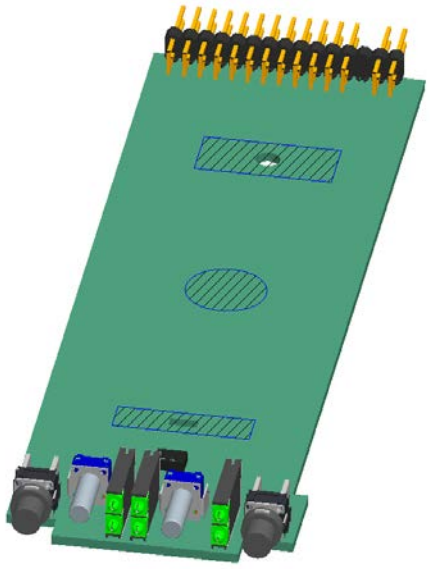


Figure 75. SSI Common Front Panel Board

While the front panel board uses a custom 2x15 connector, the baseboard simply adds a 2x2 connector in-line (and appropriately spaced) with the existing SSI 2x12 connector. Boards that support Quad LAN can populate the 2x2 connector, and boards that only support Dual LAN can depopulate the connector.

Table 42. SSI Front Panel Connector Pin-out (Baseboard)

Pin #	SSI Sig name	Pin #	SSI Sig name
1	SB3.3V	2	SB3.3V
3	Key	4	SB5V
5	Power LED Cathode	6	System ID LED Cathode
7	3.3V	8	System Fault LED Anode
9	HDD Activity LED Cathode	10	System Fault LED Cathode
11	Power Switch	12	NIC#1 Activity LED
13	GND (Power Switch)	14	NIC#1 Link LED
15	Reset Switch	16	I2C SDA
17	GND (Reset/ID/NMI Switch)	18	I2C SCL
19	System ID Switch	20	Chassis Intrusion
21	Pull Down	22	NIC#2 Activity LED
23	NMI to CPU Switch	24	NIC#2 Link LED

12. IO Module Support

In addition to the embedded I/O features of the server board, and those available with the addition of a PCIe add-in card, the server also provides concurrent support of an optionally installed I/O module.

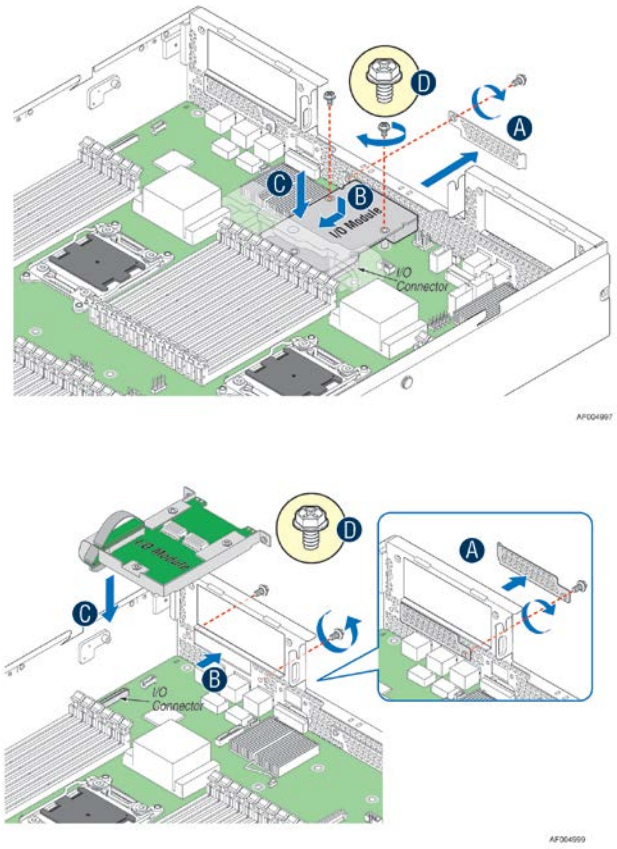


Figure 76. Mezzanine Support

The following table lists the Intel® I/O modules available for this server.

Table 43. Intel® I/O Modules

Product Code & IPN	Description
AXX10GBNIAIOM MM# 917905	Dual SFP+ port 10GbE IO Module based on Intel® 82599 10GbE Ethernet Controller
AXX10GBTWLIOM MM# 917907	Dual RJ45 Port, 10GBASE-T IO Module, based on Intel® I350 Ethernet chipset
AXX1FDRIBIOM MM# 918607	Single Port, FDR speed Infiniband module, with QSFP connector
AXX4P1GBPWLIOM MM# 917911	Quad Port 1GbE 1o Module based on Intel® Ethernet Controller I350

The system supports the Intel® Remote Management Module 4 (RMM4). Additional information for the RMM4 option can be found in the following documents: *Intel® Remote Management Module 4 Technical Product Specification* and the *Intel® Remote Management Module 4 and Integrated BMC Web Console Users Guide*.

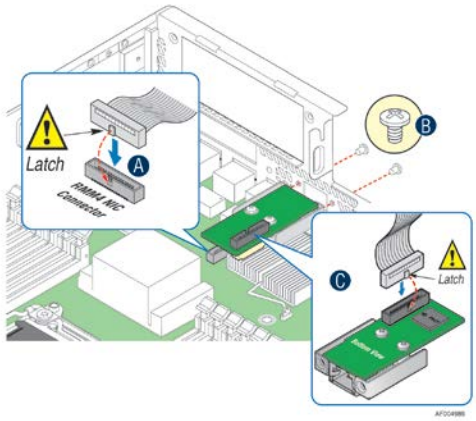


Figure 77. RMM4 Installation

13. Intel® Intelligent Power Node Manager (NM)

13.1 Overview

Power management deals with requirements to manage processor power consumption and manage power at the platform level to meet critical business needs. Node Manager (NM) is a platform resident technology that enforces power capping and thermal-triggered power capping policies for the platform. These policies are applied by exploiting subsystem knobs (such as processor P and T states) that can be used to control power consumption. NM enables data center power management by exposing an external interface to management software through which platform policies can be specified. It also implements specific data center power management usage models such as power limiting, and thermal monitoring. Refer to the *EPSD Platforms Based On Intel Xeon® Processor E5 4600/2600/2400/1600 Product Families BMC Core Firmware External Product Specification* for additional details.

The NM feature is implemented by a complementary architecture utilizing the ME, BMC, BIOS, and an ACPI-compliant OS. The ME provides the NM policy engine and power control/limiting functions (referred to as Node Manager or NM) while the BMC provides the external LAN link by which external management software can interact with the feature. The BIOS provides system power information utilized by the NM algorithms and also exports ASL code used by OSPM for negotiating processor P and T state changes for power limiting. PMBus-compliant power supplies provide the capability to monitoring input power consumption, which is necessary to support NM.

The NM architecture applicable to this generation of servers is defined by the *NPTM Architecture Specification v2.0*. NPTM is an evolving technology that is expected to continue to add new capabilities that will be defined in subsequent versions of the specification. The ME NM implements the NPTM policy engine and control/monitoring algorithms defined in the NPTM specification.

13.1.1 Hardware Requirements

NM is supported only on platforms that have the NM FW functionality loaded and enabled on the Management Engine (ME) in the SSB and that have a BMC present to support the external LAN interface to the ME. NM power limiting feature requires a means for the ME to monitor input power consumption for the platform. This capability is generally provided by means of PMBus-compliant power supplies although an alternative model using a simpler SMBus power monitoring device is possible (there is potential loss in accuracy and responsiveness using non-PMBus devices). The NM SmaRT/CLST feature does specifically require PMBus-compliant power supplies as well as additional hardware on the baseboard.

13.1.2 Features

NM provides feature support for policy management, monitoring and querying, alerts and notifications, and an external interface protocol. The policy management features implement specific IT goals that can be specified as policy directives for NM. Monitoring and querying features enable tracking of power consumption. Alerts and notifications provide the foundation for automation of power management in the data center management stack. The external interface specifies the protocols that must be supported in this version of NM.

13.1.3 Role of BMC in NM

This section summarizes the BMC role in the NM feature implementation.

13.1.3.1 External Communications Link

The BMC provides the access point for remote commands from external management SW and generates alerts to that SW. The ME plays the role of an IPMI satellite controller that communicates to the BMC over a secondary IPMB. There are mechanisms to forward commands to ME and send response back to originator. Similarly events generated by ME to the BMC (via IPMB) have to be sent by the BMC to the external SW over the LAN link. It is the responsibility of BMC to implement these mechanisms for communication with Node Manager (NM).

This section provides an overview of how the external communication link to ME works. Refer to the *Intel® Intelligent Power Node Manager 2.0 External Architecture Specification using IPMI* for details of this interface.

13.1.3.1.1 Command Passing via BMC

External SW wishing to communicate with the NM will send bridged IPMI commands to BMC. This will be in the form an IPMI packet encapsulated in another packet, following standard IPMI bridging as described in the *IPMI 2.0 Specification*. BMC forwards the encapsulated command to NM engine on the ME and returns the response to the sender.

Due to the fact that some of the NM commands have potential for performance limiting and system shut-down, the BMC FW enforces an administrator privilege for any commands bridged to the ME.

13.1.3.1.2 Alerting

Alerts may be sent from the NM in the ME to the external SW by one of two different methods depending on the nature of the alert.

Alerts that signify fault conditions that should be recorded in the system SEL will be sent to the BMC by the ME using the IPMI *Platform Event Message* command. The BMC deposits such events into the SEL. The external SW must configure the BMC's PEF and alerting features to send that event out as an IPMI LAN alert, directed to the SW application over the LAN link.

Alerts that provide useful notification to the external SW for NM management, but do not represent significant fault conditions that need to be put into the SEL, will be sent to the BMC using the IPMI *Alert Immediate* command. This requires that the external SW application provides the NM on the ME with the alert destination and alert string information needed to properly form and send the alert. The external SW must first properly configure the alert destination and string in the BMC LAN configuration using standard IPMI commands, then provide the associated selectors to the BMC using the *Set Node Manager Alert Destination* OEM command.

13.1.3.2 BIOS-BMC-ME Communication

Unlike the implementation in previous generation servers in which the BIOS and ME communicated through the BMC, this generation of platforms the BIOS communicates directly with the ME via PECI.

13.1.4 ME System Management Bus (SMBus) Interface

- The ME uses the SMLink0 on the SSB in multi-master mode as a dedicated bus for communication with the BMC using the IPMB protocol. The EPSD BMC FW considers this a secondary IPMB bus and runs at 400 kHz.
- The ME uses the SMLink1 on the SSB in multi-master mode bus for communication with PMBus devices in the power supplies for support of various NM-related features. This bus is shared with the BMC, which polls these PMBus power supplies for sensor monitoring purposes (for example, power supply status, input power, and so on). This bus runs at 100 KHz.
- The Management Engine has access to the Host SMBus.

13.1.5 PECI 3.0

The ME owns the PECI bus for all EPSD server implementations.

The ME uses SPI flash attached to the SSB to keep ME firmware code and configuration data. This flash device is also used by system BIOS.

13.1.6 PECI Proxy

The PECI proxy feature is included for all Westerlee FW configurations.

The general concept is that PECI Proxy provides access to PECI interface for BMCs that do not have direct PECI bus access.

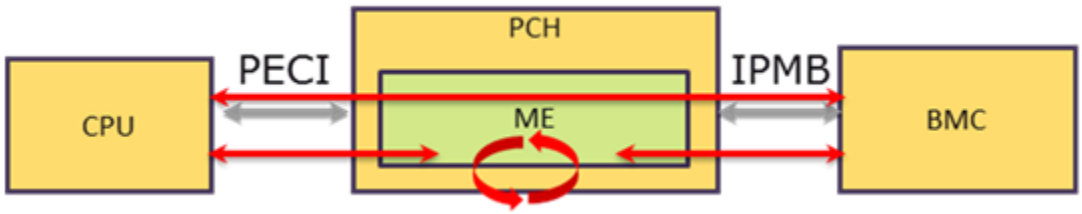


Figure 78. PECI Proxy

PECI Proxy support includes the following:

- Raw PECI: BMC can generate any PECI 3.0 network or link layer compatible transaction by encapsulation in OEM IPMI commands. PECI transaction return information is passed back to the BMC as an IPMI response. ME FW automatically retries PECI transactions that completed with completion code that indicates that the operation has started and that it has not completed yet.
- Support for aggregating multiple PECI requests/responses in a single OEM IPMI command.
- Special IPMI Sensors representing data available over PECI.
- Aggregated access to the CPU and memory temperature parameters over OEM IPMI commands.

- Read/write PCI configuration and Machine Check Register read access is provided via IPMI OEM commands.
- Support for configuration of filtering constant used by CPU to average CPU temperature readings.
- Read access to Icc TDC parameter of all CPUs on the platform over OEM IPMI extension command.

PECI Proxy functionality supports configurations up to 4 processors and up to 4 memory channels per processor socket.

13.1.7 ME Power and Firmware Startup

On EPSD server products, the ME is on standby power. The ME FW will begin its startup sequence at the same time that the BMC FW is booting. As the BMC FW is booting to a Linux kernel and the ME FW uses an RTOS, the ME FW will always complete its basic initialization before the BMC. The ME FW can be configured to send a notification message to the BMC. After this point, the ME FW is ready to process any command requests from the BMC.

In S0/S1 power states, all ME FW functionality is supported. Some features, such as power limiting, are not supported in S3/S4/S5 power states. Refer to ME FW documentation for details on what is not supported while in the S3/S4/S5 states.

13.1.8 ME Firmware Update

On EPSD server platforms, the ME FW uses a single operational image with a limited-functionality recovery image. In order to upgrade an operational image, a boot to recovery image must be performed. Unlike previous generation platforms, the ME FW does not support an IPMI update mechanism except for the case that the system is configured with a dual-ME (redundant) image. In order to conserve flash space, which the ME FW shares with BIOS, EPSD systems only support a single ME image. For this case, ME update is only supported by means of BIOS performing a direct update of the flash component. The recovery image only provides the basic functionality that is required to perform the update; therefore other ME FW features are not functional therefore when the update is in progress.

13.1.9 NM Discovery OEM SDR

A NM discovery OEM SDR must be loaded into the BMC's SDR repository if and only if the NM feature is supported on that product. This OEM SDR is used by management software to detect if NM is supported and to understand how to communicate with it.

Since PMBus compliant power supplies are required in order to support NM, the system will be probed when the SDRs are loaded into the BMC's SDR repository in order to determine whether or not the installed power supplies do in fact support PMBus. If the installed power supplies are not PMBus compliant, the NM discovery OEM SDR will not be loaded.

Refer to the *Intel® Intelligent Power Node Manager 2.0 External Architecture Specification using IPMI* for details of this interface.

13.1.9.1 ME-BMC Interactions

- BMC stores sensor data records for ME-owned sensors.

- BMC initializes ME-owned sensors based on SDRs.
- BMC receives platform event messages sent by the ME.
- BMC notifies ME of POST completion.
- BMC may be queried by the ME for inlet temperature readings.

13.1.10 SmaRT/CLST

The power supply optimization provided by SmaRT/CLST relies on a platform HW capability as well as ME FW support. When a PMBus-compliant power supply detects insufficient input voltage, an overcurrent condition, or an over-temperature condition, it will assert the SMBAlert# signal on the power supply SMBus (a.k.a. the PMBus). Through the use of external gates, this results in a momentary assertion of the PROCHOT# and MEMHOT# signals to the processors, thereby throttling the processors and memory. The ME FW also sees the SMBAlert# assertion, queries the power supplies to determine the condition causing the assertion, and applies an algorithm to either release or prolong the throttling, based on the situation.

System power control modes include:

- SmaRT: Low AC input voltage event; results in a onetime momentary throttle for each event to the maximum throttle state.
- Electrical Protection CLST: High output energy event; results in a throttling hiccup mode with fixed maximum throttle time and a fix throttle release ramp time.
- Thermal Protection CLST: High power supply thermal event; results in a throttling hiccup mode with fixed maximum throttle time and a fix throttle release ramp time.

When the SMBAlert# signal is asserted, the fans will be gated by HW for a short period (~100ms) to reduce overall power consumption. It is expected that the interruption to the fans will be of short enough duration to avoid false lower threshold crossings for the fan tach sensors; however, this may need to be comprehended by the fan monitoring FW if it does have this side-effect.

13.1.10.1 Dependencies on PMBus-compliant Power Supply Support

The SmaRT/CLST system feature depends on functionality present in the ME NM SKU. This feature requires power supplies that are compliant with the *PMBus Specification rev1.2*.

Appendix A: Integration and Usage Tip

This section provides a list of useful information that is unique to the Intel® Server System R2000LH2/LT2 Product Family and should be kept in mind while configuring your server system.

- Only the Intel® Xeon® processor E5-4600 product family is supported in this Intel server system. Previous generation Intel® Xeon® processors are not supported.
- For best system performance, follow memory population guidelines as specified in the *Intel® Server Board S4600LH2/S4600LT2 Technical Product Specification*.
- For best system performance, follow all thermal configuration guidelines as specified in this document.
- The CPU-1 processor and CPU heat sink must be installed first. The CPU-2, CPU-3, and CPU-4 heat sinks must be installed at all times, with or without a processor installed.
- The Mini-SAS connector labeled *SCU_1(4-7)* on the server board is only functional when an appropriate Intel® RAID C600 Upgrade Key is installed.
- Many integrated on-board SAS and RAID options are available by installing any of several available Intel® RAID C600 Upgrade Keys.
- The FRUSDR utility must be run after the hardware integration is complete in order to load the proper Sensor Data Records for the server chassis onto the server board.
- Make sure the latest system software is loaded on the server. This includes System BIOS, BMC Firmware, ME Firmware and FRUSDR. The latest system software can be downloaded from the Intel web site.

Appendix B: POST Code Diagnostic LED Decoder

As an aid to assist in troubleshooting a system hang that occurs during a system's Power-On Self-Test (POST) process, the server board includes a bank of eight POST Code Diagnostic LEDs on the back edge of the server board.

During the system boot process, Memory Reference Code (MRC) and System BIOS execute a number of memory initialization and platform configuration processes, each of which is assigned a specific hex POST code number. As each routine is started, the given POST code number is displayed to the POST Code Diagnostic LEDs on the back edge of the server board.

During a POST system hang, the displayed post code can be used to identify the last POST routine that was run prior to the error occurring, helping to isolate the possible cause of the hang condition.

Each POST code is represented by eight LEDs; four Green and four Amber. The POST codes are divided into two nibbles, an upper nibble and a lower nibble. The upper nibble bits are represented by Amber Diagnostic LEDs #4, #5, #6, and #7. The lower nibble bits are represented by Green Diagnostics LEDs #0, #1, #2, and #3. If the bit is set in the upper and lower nibbles, the corresponding LED is lit. If the bit is clear, the corresponding LED is off.

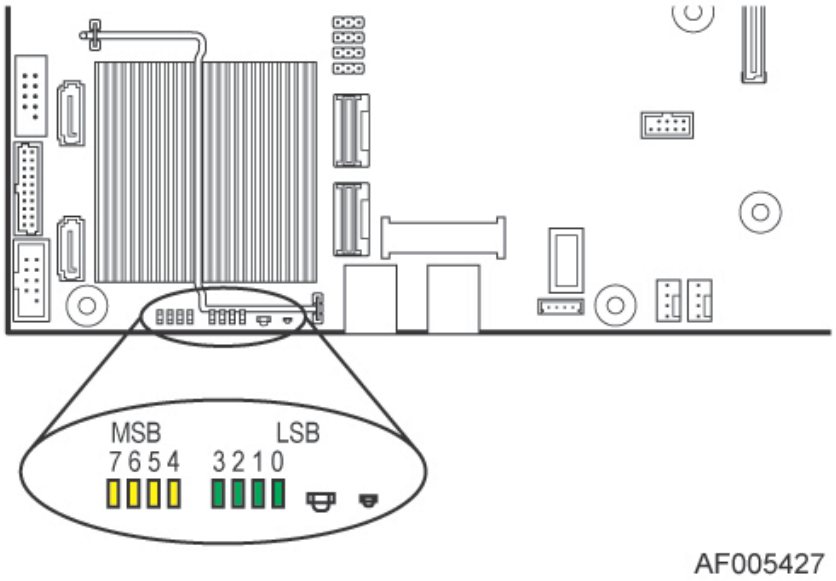


Figure 79. POST Diagnostic LED Location

In the following example, the BIOS sends a value of ACh to the diagnostic LED decoder. The LEDs are decoded as follows.

Table 44. POST Progress Code LED Example

LEDs	Upper Nibble AMBER LEDs				Lower Nibble GREEN LEDs			
	MSB							LSB
	LED #7	LED #6	LED #5	LED #4	LED #3	LED #2	LED #1	LED #0
	8h	4h	2h	1h	8h	4h	2h	1h
Status	ON	OFF	ON	OFF	ON	ON	OFF	OFF
Results	1	0	1	0	1	1	0	0
	Ah				Ch			

Upper nibble bits = 1010b = Ah; Lower nibble bits = 1100b = Ch; the two are concatenated as ACh

The following table provides a list of all POST progress codes..

Table 45. POST Progress Codes

Checkpoint	Diagnostic LED Decoder 1 = LED On, 0 = LED Off								Description
	Upper Nibble				Lower Nibble				
	MSB							LSB	
	8h	4h	2h	1h	8h	4h	2h	1h	
LED #	#7	#6	#5	#4	#3	#2	#1	#0	
SEC Phase									
01h	0	0	0	0	0	0	0	1	First POST code after CPU reset
02h	0	0	0	0	0	0	1	0	Microcode load begin
03h	0	0	0	0	0	0	1	1	CRAM initialization begin
04h	0	0	0	0	0	1	0	0	Pei Cache When Disabled
05h	0	0	0	0	0	1	0	1	SEC Core At Power On Begin.
06h	0	0	0	0	0	1	1	0	Early CPU initialization during Sec Phase.
07h	0	0	0	0	0	1	1	1	Early SB initialization during Sec Phase.
08h	0	0	0	0	1	0	0	0	Early NB initialization during Sec Phase.
09h	0	0	0	0	1	0	0	1	End Of Sec Phase.
0Eh	0	0	0	0	1	1	1	0	Microcode Not Found.
0Fh	0	0	0	0	1	1	1	1	Microcode Not Loaded.
PEI Phase									
10h	0	0	0	1	0	0	0	0	PEI Core
11h	0	0	0	1	0	0	0	1	CPU PEIM
15h	0	0	0	1	0	1	0	1	NB PEIM
19h	0	0	0	1	1	0	0	1	SB PEIM
MRC Process Codes – MRC Progress Code Sequence is executed									
PEI Phase continued…									
31h	0	0	1	1	0	0	0	1	Memory Installed
32h	0	0	1	1	0	0	1	0	CPU PEIM (Cpu Init)
33h	0	0	1	1	0	0	1	1	CPU PEIM (Cache Init)
34h	0	0	1	1	0	1	0	0	CPU PEIM (BSP Select)

Checkpoint	Diagnostic LED Decoder 1 = LED On, 0 = LED Off								Description
	Upper Nibble				Lower Nibble				
	MSB							LSB	
	8h	4h	2h	1h	8h	4h	2h	1h	
LED #	#7	#6	#5	#4	#3	#2	#1	#0	
35h	0	0	1	1	0	1	0	1	CPU PEIM (AP Init)
36h	0	0	1	1	0	1	1	0	CPU PEIM (CPU SMM Init)
4Fh	0	1	0	0	1	1	1	1	Dxe IPL started
DXE Phase									
60h	0	1	1	0	0	0	0	0	DXE Core started
61h	0	1	1	0	0	0	0	1	DXE NVRAM Init
62h	0	1	1	0	0	0	1	0	SB RUN Init
63h	0	1	1	0	0	0	1	1	Dxe CPU Init
68h	0	1	1	0	1	0	0	0	DXE PCI Host Bridge Init
69h	0	1	1	0	1	0	0	1	DXE NB Init
6Ah	0	1	1	0	1	0	1	0	DXE NB SMM Init
70h	0	1	1	1	0	0	0	0	DXE SB Init
71h	0	1	1	1	0	0	0	1	DXE SB SMM Init
72h	0	1	1	1	0	0	1	0	DXE SB devices Init
78h	0	1	1	1	1	0	0	0	DXE ACPI Init
79h	0	1	1	1	1	0	0	1	DXE CSM Init
90h	1	0	0	1	0	0	0	0	DXE BDS Started
91h	1	0	0	1	0	0	0	1	DXE BDS connect drivers
92h	1	0	0	1	0	0	1	0	DXE PCI Bus begin
93h	1	0	0	1	0	0	1	1	DXE PCI Bus HPC Init
94h	1	0	0	1	0	1	0	0	DXE PCI Bus enumeration
95h	1	0	0	1	0	1	0	1	DXE PCI Bus resource requested
96h	1	0	0	1	0	1	1	0	DXE PCI Bus assign resource
97h	1	0	0	1	0	1	1	1	DXE CON_OUT connect
98h	1	0	0	1	1	0	0	0	DXE CON_IN connect
99h	1	0	0	1	1	0	0	1	DXE SIO Init
9Ah	1	0	0	1	1	0	1	0	DXE USB start
9Bh	1	0	0	1	1	0	1	1	DXE USB reset
9Ch	1	0	0	1	1	1	0	0	DXE USB detect
9Dh	1	0	0	1	1	1	0	1	DXE USB enable
A1h	1	0	1	0	0	0	0	1	DXE IDE begin
A2h	1	0	1	0	0	0	1	0	DXE IDE reset
A3h	1	0	1	0	0	0	1	1	DXE IDE detect
A4h	1	0	1	0	0	1	0	0	DXE IDE enable
A5h	1	0	1	0	0	1	0	1	DXE SCSI begin
A6h	1	0	1	0	0	1	1	0	DXE SCSI reset
A7h	1	0	1	0	0	1	1	1	DXE SCSI detect
A8h	1	0	1	0	1	0	0	0	DXE SCSI enable
A9h	1	0	1	0	1	0	0	1	DXE verifying SETUP password
ABh	1	0	1	0	1	0	1	1	DXE SETUP start
ACh	1	0	1	0	1	1	0	0	DXE SETUP input wait

Checkpoint	Diagnostic LED Decoder 1 = LED On, 0 = LED Off								Description
	Upper Nibble				Lower Nibble				
	MSB							LSB	
	8h	4h	2h	1h	8h	4h	2h	1h	
LED #	#7	#6	#5	#4	#3	#2	#1	#0	
ADh	1	0	1	0	1	1	0	1	DXE Ready to Boot
AEh	1	0	1	0	1	1	1	0	DXE Legacy Boot
AFh	1	0	1	0	1	1	1	1	DXE Exit Boot Services
B0h	1	0	1	1	0	0	0	0	RT Set Virtual Address Map Begin
B1h	1	0	1	1	0	0	0	1	RT Set Virtual Address Map End
B2h	1	0	1	1	0	0	1	0	DXE Legacy Option ROM init
B3h	1	0	1	1	0	0	1	1	DXE Reset system
B4h	1	0	1	1	0	1	0	0	DXE USB Hot plug
B5h	1	0	1	1	0	1	0	1	DXE PCI BUS Hot plug
B6h	1	0	1	1	0	1	1	0	DXE NVRAM cleanup
B7h	1	0	1	1	0	1	1	1	DXE Configuration Reset
00h	0	0	0	0	0	0	0	0	INT19
S3 Resume									
E0h	1	1	0	1	0	0	0	0	S3 Resume PEIM (S3 started)
E1h	1	1	0	1	0	0	0	1	S3 Resume PEIM (S3 boot script)
E2h	1	1	0	1	0	0	1	0	S3 Resume PEIM (S3 Video Repost)
E3h	1	1	0	1	0	0	1	1	S3 Resume PEIM (S3 OS wake)
BIOS Recovery									
F0h	1	1	1	1	0	0	0	0	PEIM which detected forced Recovery condition
F1h	1	1	1	1	0	0	0	1	PEIM which detected User Recovery condition
F2h	1	1	1	1	0	0	1	0	Recovery PEIM (Recovery started)
F3h	1	1	1	1	0	0	1	1	Recovery PEIM (Capsule found)
F4h	1	1	1	1	0	1	0	0	Recovery PEIM (Capsule loaded)
F8h	1	1	1	1	1	0	0	0	Recovery PPI not found
F9h	1	1	1	1	1	0	0	1	Recovery Capsule not found
FAh	1	1	1	1	1	0	1	0	Invalid Recovery Capsule

POST Memory Initialization MRC Diagnostic Codes

There are two types of POST Diagnostic Codes displayed by the MRC during memory initialization; Progress Codes and Fatal Error Codes.

The MRC Progress Codes are displays to the Diagnostic LEDs that show the execution point in the MRC operational path at each step.

Table 46. MRC Progress Codes

Checkpoint	Diagnostic LED Decoder 1 = LED On, 0 = LED Off								Description
	Upper Nibble				Lower Nibble				
	MSB							LSB	
	8h	4h	2h	1h	8h	4h	2h	1h	
LED #	#7	#6	#5	#4	#3	#2	#1	#0	
MRC Progress Codes									
B0h	1	0	1	1	0	0	0	0	Detect DIMM population
B1h	1	0	1	1	0	0	0	1	Set DDR3 frequency
B2h	1	0	1	1	0	0	1	0	Gather remaining SPD data
B3h	1	0	1	1	0	0	1	1	Program registers on the memory controller level
B4h	1	0	1	1	0	1	0	0	Evaluate RAS modes and save rank information
B5h	1	0	1	1	0	1	0	1	Program registers on the channel level
B6h	1	0	1	1	0	1	1	0	Perform the JEDEC defined initialization sequence
B7h	1	0	1	1	0	1	1	1	Train DDR3 ranks
B8h	1	0	1	1	1	0	0	0	Initialize CLTT/OLTT
B9h	1	0	1	1	1	0	0	1	Hardware memory test and init
BAh	1	0	1	1	1	0	1	0	Execute software memory init
BBh	1	0	1	1	1	0	1	1	Program memory map and interleaving
BCh	1	0	1	1	1	1	0	0	Program RAS configuration
BFh	1	0	1	1	1	1	1	1	MRC is done

Memory Initialization at the beginning of POST includes multiple functions, including discovery, channel training, validation that the DIMM population is acceptable and functional, initialization of the IMC and other hardware settings, and initialization of applicable RAS configurations.

When a major memory initialization error occurs and prevents the system from booting with data integrity, a beep code is generated, the MRC will display a fatal error code on the diagnostic LEDs, and a system halt command is executed. Fatal MRC error halts do NOT change the state of the System Status LED, and they do NOT get logged as SEL events. The following table lists all MRC fatal errors that are displayed to the Diagnostic LEDs.

Table 47. MRC Fatal Error Codes

Checkpoint	Diagnostic LED Decoder								Description
	1 = LED On, 0 = LED Off								
	Upper Nibble				Lower Nibble				
	MSB							LSB	
	8h	4h	2h	1h	8h	4h	2h	1h	
LED	#7	#6	#5	#4	#3	#2	#1	#0	
MRC Fatal Error Codes									
E8h	1	1	1	0	1	0	0	0	No usable memory error 01h = No memory was detected from the SPD read, or invalid config that causes no operable memory. 02h = Memory DIMMs on all channels of all sockets are disabled due to hardware memtest error. 3h = No memory installed. All channels are disabled.
E9h	1	1	1	0	1	0	0	1	Memory is locked by Intel® Trusted Execution Technology and is inaccessible
EAh	1	1	1	0	1	0	1	0	DDR3 channel training error 01h = Error on read DQ/DQS (Data/Data Strobe) init 02h = Error on Receive Enable 3h = Error on Write Leveling 04h = Error on write DQ/DQS (Data/Data Strobe
EBh	1	1	1	0	1	0	1	1	Memory test failure 01h = Software memtest failure. 02h = Hardware memtest failed. 03h = Hardware Memtest failure in Lockstep Channel mode requiring a channel to be disabled. This is a fatal error which requires a reset and calling MRC with a different RAS mode to retry.
EDh	1	1	1	0	1	1	0	1	DIMM configuration population error 01h = Different DIMM types (UDIMM, RDIMM, LRDIMM) are detected installed in the system. 02h = Violation of DIMM population rules. 03h = The 3rd DIMM slot cannot be populated when QR DIMMs are installed. 04h = UDIMMs are not supported in the 3rd DIMM slot. 05h = Unsupported DIMM Voltage.
EFh	1	1	1	0	1	1	1	1	Indicates a CLTT table structure error

Appendix C: POST Code Errors

Most error conditions encountered during POST are reported using POST Error Codes. These codes represent specific failures, warnings, or are informational. POST Error Codes may be displayed in the Error Manager display screen, and are always logged to the System Event Log (SEL). Logged events are available to System Management applications, including Remote and Out of Band (OOB) management.

There are exception cases in early initialization where system resources are not adequately initialized for handling POST Error Code reporting. These cases are primarily Fatal Error conditions resulting from initialization of processors and memory, and they are handed by a Diagnostic LED display with a system halt.

The following table lists the supported POST Error Codes. Each error code is assigned an error type which determines the action the BIOS will take when the error is encountered. Error types include Minor, Major, and Fatal. The BIOS action for each is defined as follows:

- **Minor**: The error message is displayed on the screen or on the Error Manager screen, and an error is logged to the SEL. The system continues booting in a degraded state. The user may want to replace the erroneous unit. The POST Error Pause option setting in the BIOS setup does not have any effect on this error.
- **Major**: The error message is displayed on the Error Manager screen, and an error is logged to the SEL. The POST Error Pause option setting in the BIOS setup determines whether the system pauses to the Error Manager for this type of error so the user can take immediate corrective action or the system continues booting.

  Note that for 0048 “Password check failed”, the system halts, and then after the next reset/reboot will displays the error code on the Error Manager screen.
- **Fatal**: The system halts during post at a blank screen with the text “Unrecoverable fatal error found. System will not boot until the error is resolved” and “Press <**F2**> to enter setup” The POST Error Pause option setting in the BIOS setup does not have any effect with this class of error.

When the operator presses the **F2** key on the keyboard, the error message is displayed on the Error Manager screen, and an error is logged to the SEL with the error code. The system cannot boot unless the error is resolved. The user needs to replace the faulty part and restart the system.

NOTE: The POST error codes in the following table are common to all current generation Intel server platforms. Features present on a given server board/system will determine which of the listed error codes are supported.

Table 48. POST Error Messages and Handling

Error Code	Error Message	Response
0012	System RTC date/time not set	Major
0048	Password check failed	Major
0140	PCI component encountered a PERR error	Major
0141	PCI resource conflict	Major
0146	PCI out of resources error	Major
0191	Processor core/thread count mismatch detected	Fatal
0192	Processor cache size mismatch detected	Fatal
0194	Processor family mismatch detected	Fatal
0195	Processor Intel® QPI link frequencies unable to synchronize	Fatal
0196	Processor model mismatch detected	Fatal
0197	Processor frequencies unable to synchronize	Fatal
5220	BIOS Settings reset to default settings	Major
5221	Passwords cleared by jumper	Major
5224	Password clear jumper is Set	Major
8130	Processor 01 disabled	Major
8131	Processor 02 disabled	Major
8132	Processor 03 disabled	Major
8133	Processor 04 disabled	Major
8160	Processor 01 unable to apply microcode update	Major
8161	Processor 02 unable to apply microcode update	Major
8162	Processor 03 unable to apply microcode update	Major
8163	Processor 04 unable to apply microcode update	Major
8170	Processor 01 failed Self-Test (BIST)	Major
8171	Processor 02 failed Self-Test (BIST)	Major
8172	Processor 03 failed Self-Test (BIST)	Major
8173	Processor 04 failed Self-Test (BIST)	Major
8180	Processor 01 microcode update not found	Minor
8181	Processor 02 microcode update not found	Minor
8182	Processor 03 microcode update not found	Minor
8183	Processor 04 microcode update not found	Minor
8190	Watchdog timer failed on last boot	Major
8198	OS boot watchdog timer failure	Major
8300	Baseboard management controller failed self-test	Major
8305	Hot Swap Controller failure	Major
83A0	Management Engine (ME) failed Self-test	Major
83A1	Management Engine (ME) Failed to respond.	Major
84F2	Baseboard management controller failed to respond	Major
84F3	Baseboard management controller in update mode	Major
84F4	Sensor data record empty	Major
84FF	System event log full	Minor
8500	Memory component could not be configured in the selected RAS mode	Major
8501	DIMM Population Error	Major
8520	DIMM_A1 failed test/initialization	Major
8521	DIMM_A2 failed test/initialization	Major

Error Code	Error Message	Response
8522	DIMM_A3 failed test/initialization	Major
8523	DIMM_B1 failed test/initialization	Major
8524	DIMM_B2 failed test/initialization	Major
8525	DIMM_B3 failed test/initialization	Major
8526	DIMM_C1 failed test/initialization	Major
8527	DIMM_C2 failed test/initialization	Major
8528	DIMM_C3 failed test/initialization	Major
8529	DIMM_D1 failed test/initialization	Major
852A	DIMM_D2 failed test/initialization	Major
852B	DIMM_D3 failed test/initialization	Major
852C	DIMM_E1 failed test/initialization	Major
852D	DIMM_E2 failed test/initialization	Major
852E	DIMM_E3 failed test/initialization	Major
852F	DIMM_F1 failed test/initialization	Major
8530	DIMM_F2 failed test/initialization	Major
8531	DIMM_F3 failed test/initialization	Major
8532	DIMM_G1 failed test/initialization	Major
8533	DIMM_G2 failed test/initialization	Major
8534	DIMM_G3 failed test/initialization	Major
8535	DIMM_H1 failed test/initialization	Major
8536	DIMM_H2 failed test/initialization	Major
8537	DIMM_H3 failed test/initialization	Major
8538	DIMM_J1 failed test/initialization	Major
8539	DIMM_J2 failed test/initialization	Major
853A	DIMM_J3 failed test/initialization	Major
853B	DIMM_K1 failed test/initialization	Major
853C (Go to 853D)	DIMM_K2 failed test/initialization	Major
8540	DIMM_A1 disabled	Major
8541	DIMM_A2 disabled	Major
8542	DIMM_A3 disabled	Major
8543	DIMM_B1 disabled	Major
8544	DIMM_B2 disabled	Major
8545	DIMM_B3 disabled	Major
8546	DIMM_C1 disabled	Major
8547	DIMM_C2 disabled	Major
8548	DIMM_C3 disabled	Major
8549	DIMM_D1 disabled	Major
854A	DIMM_D2 disabled	Major
854B	DIMM_D3 disabled	Major
854C	DIMM_E1 disabled	Major
854D	DIMM_E2 disabled	Major
854E	DIMM_E3 disabled	Major
854F	DIMM_F1 disabled	Major
8550	DIMM_F2 disabled	Major

Error Code	Error Message	Response
8551	DIMM_F3 disabled	Major
8552	DIMM_G1 disabled	Major
8553	DIMM_G2 disabled	Major
8554	DIMM_G3 disabled	Major
8555	DIMM_H1 disabled	Major
8556	DIMM_H2 disabled	Major
8557	DIMM_H3 disabled	Major
8558	DIMM_J1 disabled	Major
8559	DIMM_J2 disabled	Major
855A	DIMM_J3 disabled	Major
855B	DIMM_K1 disabled	Major
855C (Go to 855D)	DIMM_K2 disabled	Major
8560	DIMM_A1 encountered a Serial Presence Detection (SPD) failure	Major
8561	DIMM_A2 encountered a Serial Presence Detection (SPD) failure	Major
8562	DIMM_A3 encountered a Serial Presence Detection (SPD) failure	Major
8563	DIMM_B1 encountered a Serial Presence Detection (SPD) failure	Major
8564	DIMM_B2 encountered a Serial Presence Detection (SPD) failure	Major
8565	DIMM_B3 encountered a Serial Presence Detection (SPD) failure	Major
8566	DIMM_C1 encountered a Serial Presence Detection (SPD) failure	Major
8567	DIMM_C2 encountered a Serial Presence Detection (SPD) failure	Major
8568	DIMM_C3 encountered a Serial Presence Detection (SPD) failure	Major
8569	DIMM_D1 encountered a Serial Presence Detection (SPD) failure	Major
856A	DIMM_D2 encountered a Serial Presence Detection (SPD) failure	Major
856B	DIMM_D3 encountered a Serial Presence Detection (SPD) failure	Major
856C	DIMM_E1 encountered a Serial Presence Detection (SPD) failure	Major
856D	DIMM_E2 encountered a Serial Presence Detection (SPD) failure	Major
856E	DIMM_E3 encountered a Serial Presence Detection (SPD) failure	Major
856F	DIMM_F1 encountered a Serial Presence Detection (SPD) failure	Major
8570	DIMM_F2 encountered a Serial Presence Detection (SPD) failure	Major
8571	DIMM_F3 encountered a Serial Presence Detection (SPD) failure	Major
8572	DIMM_G1 encountered a Serial Presence Detection (SPD) failure	Major
8573	DIMM_G2 encountered a Serial Presence Detection (SPD) failure	Major
8574	DIMM_G3 encountered a Serial Presence Detection (SPD) failure	Major
8575	DIMM_H1 encountered a Serial Presence Detection (SPD) failure	Major
8576	DIMM_H2 encountered a Serial Presence Detection (SPD) failure	Major
8577	DIMM_H3 encountered a Serial Presence Detection (SPD) failure	Major
8578	DIMM_J1 encountered a Serial Presence Detection (SPD) failure	Major
8579	DIMM_J2 encountered a Serial Presence Detection (SPD) failure	Major
857A	DIMM_J3 encountered a Serial Presence Detection (SPD) failure	Major
857B	DIMM_K1 encountered a Serial Presence Detection (SPD) failure	Major
857C (Go to 857D)	DIMM_K2 encountered a Serial Presence Detection (SPD) failure	Major
853D	DIMM_K3 failed test/initialization	Major

Error Code	Error Message	Response
853E	DIMM_L1 failed test/initialization	Major
853F	DIMM_L2 failed test/initialization	Major
85C0	DIMM_L3 failed test/initialization	Major
85C1	DIMM_M1 failed test/initialization	Major
85C2	DIMM_M2 failed test/initialization	Major
85C3	DIMM_M3 failed test/initialization	Major
85C4	DIMM_N1 failed test/initialization	Major
85C5	DIMM_N2 failed test/initialization	Major
85C6	DIMM_N3 failed test/initialization	Major
85C7	DIMM_P1 failed test/initialization	Major
85C8	DIMM_P2 failed test/initialization	Major
85C9	DIMM_P3 failed test/initialization	Major
85CA	DIMM_R1 failed test/initialization	Major
85CB	DIMM_R2 failed test/initialization	Major
85CC	DIMM_R3 failed test/initialization	Major
85CD	DIMM_T1 failed test/initialization	Major
85CE	DIMM_T2 failed test/initialization	Major
85CF	DIMM_T3 failed test/initialization	Major
855D	DIMM_K3 disabled	Major
855E	DIMM_L1 disabled	Major
855F	DIMM_L2 disabled	Major
85D0	DIMM_L3 disabled	Major
85D1	DIMM_M1 disabled	Major
85D2	DIMM_M2 disabled	Major
85D3	DIMM_M3 disabled	Major
85D4	DIMM_N1 disabled	Major
85D5	DIMM_N2 disabled	Major
85D6	DIMM_N3 disabled	Major
85D7	DIMM_P1 disabled	Major
85D8	DIMM_P2 disabled	Major
85D9	DIMM_P3 disabled	Major
85DA	DIMM_R1 disabled	Major
85DB	DIMM_R2 disabled	Major
85DC	DIMM_R3 disabled	Major
85DD	DIMM_T1 disabled	Major
85DE	DIMM_T2 disabled	Major
85DD	DIMM_T3 disabled	Major
857D	DIMM_K3 encountered a Serial Presence Detection (SPD) failure	Major
857E	DIMM_L1 encountered a Serial Presence Detection (SPD) failure	Major
857F	DIMM_L2 encountered a Serial Presence Detection (SPD) failure	Major
85E0	DIMM_L3 encountered a Serial Presence Detection (SPD) failure	Major
85E1	DIMM_M1 encountered a Serial Presence Detection (SPD) failure	Major
85E2	DIMM_M2 encountered a Serial Presence Detection (SPD) failure	Major
85E3	DIMM_M3 encountered a Serial Presence Detection (SPD) failure	Major
85E4	DIMM_N1 encountered a Serial Presence Detection (SPD) failure	Major

Error Code	Error Message	Response
85E5	DIMM_N2 encountered a Serial Presence Detection (SPD) failure	Major
85E6	DIMM_N3 encountered a Serial Presence Detection (SPD) failure	Major
85E7	DIMM_P1 encountered a Serial Presence Detection (SPD) failure	Major
85E8	DIMM_P2 encountered a Serial Presence Detection (SPD) failure	Major
85E9	DIMM_P3 encountered a Serial Presence Detection (SPD) failure	Major
85EA	DIMM_R1 encountered a Serial Presence Detection (SPD) failure	Major
85EB	DIMM_R2 encountered a Serial Presence Detection (SPD) failure	Major
85EC	DIMM_R3 encountered a Serial Presence Detection (SPD) failure	Major
85ED	DIMM_T1 encountered a Serial Presence Detection (SPD) failure	Major
85EE	DIMM_T2 encountered a Serial Presence Detection (SPD) failure	Major
85EF	DIMM_T3 encountered a Serial Presence Detection (SPD) failure	Major
8604	POST Reclaim of non-critical NVRAM variables	Minor
8605	BIOS Settings are corrupted	Major
8606	NVRAM variable space was corrupted and has been reinitialized	Major
92A3	Serial port component was not detected	Major
92A9	Serial port component encountered a resource conflict error	Major
A000	TPM device not detected.	Minor
A001	TPM device missing or not responding.	Minor
A002	TPM device failure.	Minor
A003	TPM device failed self-test.	Minor
A100	BIOS ACM Error	Major
A421	PCI component encountered a SERR error	Fatal
A5A0	PCI Express component encountered a PERR error	Minor
A5A1	PCI Express component encountered an SERR error	Fatal
A6A0	DXE Boot Service driver: Not enough memory available to shadow a Legacy Option ROM	Minor

POST Error Beep Codes

The following table lists the POST error beep codes. Prior to system video initialization, the BIOS uses these beep codes to inform users on error conditions. The beep code is followed by a user-visible code on the POST Progress LEDs. For complete details, refer to the *BIOS for EPSD Platforms based on Intel® Xeon® Processor E5 4600/2600/2400/1600 Product Families External Product Specification*, IBL Document ID #476637.

Table 49. POST Error Beep Codes

Beeps	Error Message	POST Progress Code	Description
1	USB device action	NA	Short beep sounded whenever a USB device is discovered in POST, or inserted or removed during runtime
1 long	Intel® TXT security violation	0xAE, 0xAF	System halted because Intel® Trusted Execution Technology detected a potential violation of system security.
3	Memory error	See Table 45 and Table 46	System halted because a fatal error related to the memory was detected.
2	BIOS Recovery started	NA	Recovery boot has been initiated
4	BIOS Recovery failure	NA	BIOS recovery has failed. This typically happens so quickly after recovery us initiated that it sounds like a 2-4 beep code.

The Integrated BMC may generate beep codes upon detection of failure conditions. Beep codes are sounded each time the problem is discovered, such as on each power-up attempt, but are not sounded continuously. Codes that are common across all Intel server boards and systems that use same generation chipset are listed in the following table. Each digit in the code is represented by a sequence of beeps whose count is equal to the digit. For complete details, refer to the *Intel® Server System Baseboard Management Controller Core External Product Specification*, IBL Document ID #474403.

Table 50. Integrated BMC Beep Codes

Code	Reason for Beep	Associated Sensors
1-5-2-1	No CPUs installed or first CPU socket is empty.	CPU1 socket is empty, or sockets are populated incorrectly. CPU1 must be populated before CPU2.
1-5-2-4	MSID Mismatch	MSID mismatch occurs if a processor is installed into a system board that has incompatible power capabilities.
1-5-4-2	Power fault	DC power unexpectedly lost (power good dropout) – Power unit sensors report power unit failure offset.
1-5-4-4	Power control fault (power good assertion timeout).	Power good assertion timeout – Power unit sensors report soft power control failure offset.
1-5-1-2	VR Watchdog Timer sensor assertion	VR controller DC power on sequence was not completed in time.
1-5-1-4	Power Supply Status	The system does not power on or unexpectedly powers off and a Power Supply Unit (PSU) is present that is an incompatible model with one or more other PSUs in the system.

Glossary

Term	Definition
ACPI	Advanced Configuration and Power Interface
AP	Application Processor
APIC	Advanced Programmable Interrupt Control
ARP	Address Resolution Protocal
ASIC	Application Specific Integrated Circuit
ASMI	Advanced Server Management Interface
BIOS	Basic Input/Output System
BIST	Built-In Self Test
BMC	Baseboard Management Controller
BPP	Bits per pixel
Bridge	Circuitry connecting one computer bus to another, allowing an agent on one to access the other
BSP	Bootstrap Processor
Byte	8-bit quantity
CBC	Chassis Bridge Controller (A microcontroller connected to one or more other CBCs, together they bridge the IPMB buses of multiple chassis.
CEK	Common Enabling Kit
CHAP	Challenge Handshake Authentication Protocol
CMOS	Complementary Metal-oxide-semiconductor In terms of this specification, this describes the PC-AT compatible region of battery-backed 128 bytes of memory, which normally resides on the server board.
DHCP	Dynamic Host Configuration Protocal
DPC	Direct Platform Control
EEPROM	Electrically Erasable Programmable Read-Only Memory
EHCI	Enhanced Host Controller Interface
EMP	Emergency Management Port
EPS	External Product Specification
ESB2	Enterprise South Bridge 2
FBD	Fully Buffered DIMM
F MB	Flexible Mother Board
FRB	Fault Resilient Booting
FRU	Field Replaceable Unit
FSB	Front Side Bus
GB	1024 MB
GPA	Guest Physical Address
GPIO	General Purpose I/O
GTL	Gunning Transceiver Logic
HPA	Host Physical Address
HSC	Hot-swap Controller
Hz	Hertz (1 cycle/second)
I^2C	Inter-Integrated Circuit Bus
IA	Intel® Architecture
IBF	Input Buffer

Term	Definition
ICH	I/O Controller Hub
ICMB	Intelligent Chassis Management Bus
IERR	Internal Error
IFB	I/O and Firmware Bridge
ILM	Independent Loading Mechanism
IMC	Integrated Memory Controller
INTR	Interrupt
I/OAT	I/O Acceleration Technology
IOH	I/O Hub
IP	Internet Protocol
IPMB	Intelligent Platform Management Bus
IPMI	Intelligent Platform Management Interface
IR	Infrared
ITP	In-Target Probe
KB	1024 bytes
KCS	Keyboard Controller Style
KVM	Keyboard, Video, Mouse
LAN	Local Area Network
LCD	Liquid Crystal Display
LDAP	Local Directory Authentication Protocol
LED	Light Emitting Diode
LPC	Low Pin Count
LUN	Logical Unit Number
MAC	Media Access Control
MB	1024 KB
MCH	Memory Controller Hub
MD2	Message Digest 2 – Hashing Algorithm
MD5	Message Digest 5 – Hashing Algorithm – Higher Security
ME	Management Engine
MMU	Memory Management Unit
ms	Milliseconds
MTTR	Memory Type Range Register
Mux	Multiplexor
NIC	Network Interface Controller
NMI	Nonmaskable Interrupt
OBF	Output Buffer
OEM	Original Equipment Manufacturer
Ohm	Unit of electrical resistance
OVP	Over-voltage Protection
PECI	Platform Environment Control Interface
PEF	Platform Event Filtering
PEP	Platform Event Paging
PIA	Platform Information Area (This feature configures the firmware for the platform hardware)
PLD	Programmable Logic Device

Term	Definition
PMI	Platform Management Interrupt
POST	Power-On Self Test
PSMI	Power Supply Management Interface
PWM	Pulse-Width Modulation
QPI	QuickPath Interconnect
RAM	Random Access Memory
RASUM	Reliability, Availability, Serviceability, Usability, and Manageability
RISC	Reduced Instruction Set Computing
RMII	Reduced Media-Independent Interface
ROM	Read Only Memory
RTC	Real-Time Clock (Component of ICH peripheral chip on the server board)
SDR	Sensor Data Record
SECC	Single Edge Connector Cartridge
SEEPROM	Serial Electrically Erasable Programmable Read-Only Memory
SEL	System Event Log
SIO	Server Input/Output
SMBUS	System Management BUS
SMI	Server Management Interrupt (SMI is the highest priority non-maskable interrupt)
SMM	Server Management Mode
SMS	Server Management Software
SNMP	Simple Network Management Protocol
SPS	Server Platform Services
SSE2	Streaming SIMD Extensions 2
SSE3	Streaming SIMD Extensions 3
SSE4	Streaming SIMD Extensions 4
TBD	To Be Determined
TDP	Thermal Design Power
TIM	Thermal Interface Material
UART	Universal Asynchronous Receiver/Transmitter
UDP	User Datagram Protocol
UHCI	Universal Host Controller Interface
URS	Unified Retention System
UTC	Universal time coordinare
VID	Voltage Identification
VRD	Voltage Regulator Down
VT	Virtualization Technology
Word	16-bit quantity
WS-MAN	Web Services for Management
ZIF	Zero Insertion Force

Reference Documents

See the following documents for additional information:

- *Intel® Server Boards S4600LH2/LT2 Technical Product Specification*
- *Intel® Server Boards S4600LH2/LT2 and Server Systems R2000LH2/LT2 Product Family Spares/Accessories List and Configuration Guide*
- *Intel® Server System R2000LH2/LT2 Service Guide*
- *Intel® Server System R2000LH2/LT2 Quick Installation Guide*
- *Intel® Server System R2000LH2/LT2 Quick Reference Label*
- *BIOS for EPSD Platforms Based on Intel® Xeon® Processor E5-4600/2600/2400/1600 Product Families External Product Specification*
- *EPSD Platforms Based On Intel® Xeon® Processor E5 4600/2600/2400/1600 Product Families BMC Core Firmware External Product Specification*
- *SmaRT & CLST Architecture on "Romley" Systems and Power Supplies Specification* (Doc Reference # 461024)
- *Intel® Remote Management Module 4 Technical Product Specification*
- *Intel® Remote Management Module 4 and Integrated BMC Web Console Users Guide*