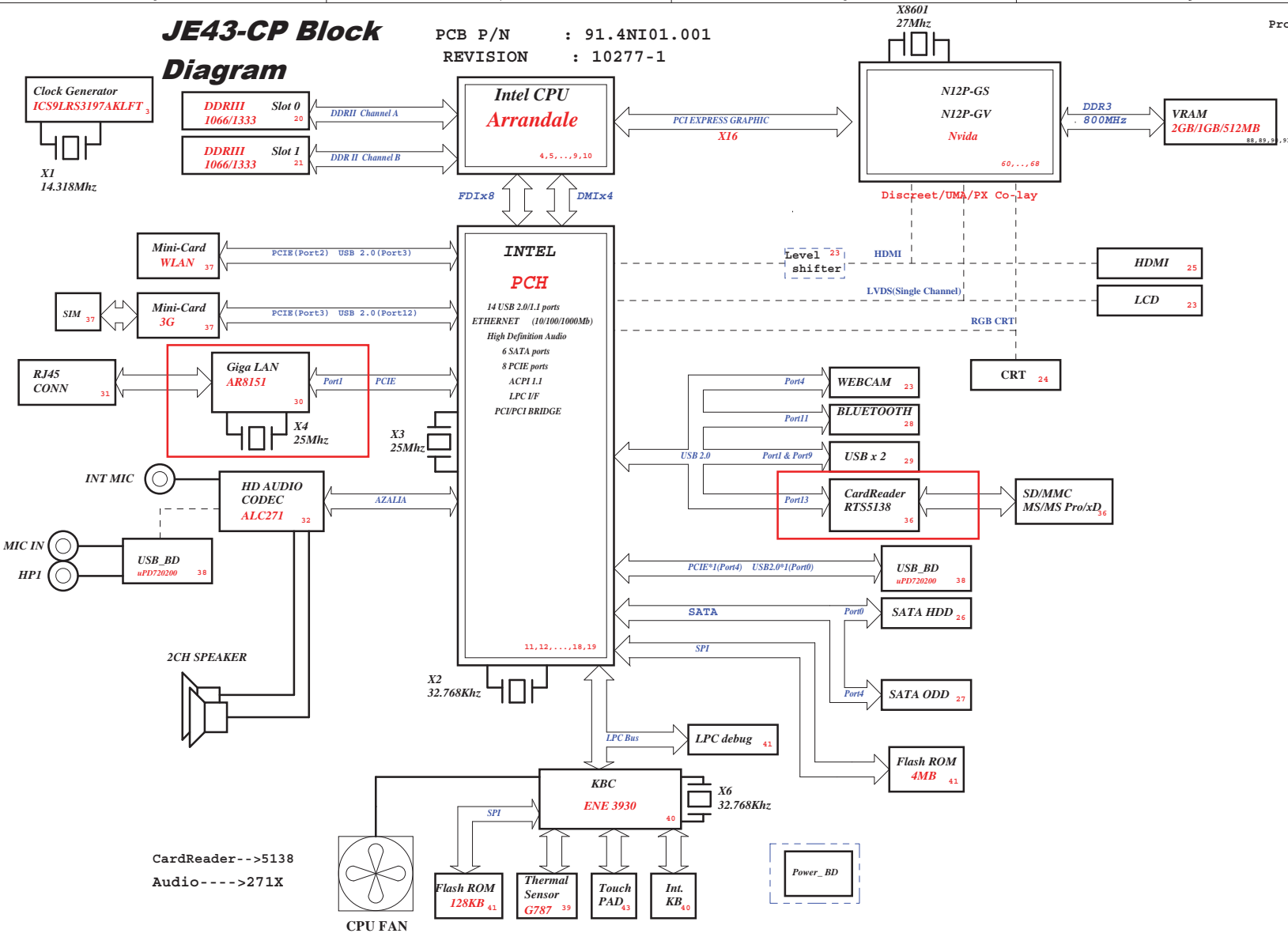


JE43-CP Block Diagram

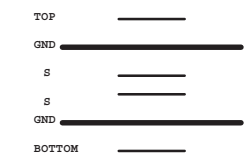
PCB P/N : 91.4NI01.001
 REVISION : 10277-1

Project code: 91.4NI01.001 (JE43-CP)



CPU DC/DC		ISL62881	54
INPUTS	OUTPUTS		
DCBATOUT	VCC_CORE		
SYSTEM DC/DC		RT8209E	50
INPUTS	OUTPUTS		
DCBATOUT	1D5V_VFT 1D5V_S0		
SYSTEM DC/DC		RT8209E	49
INPUTS	OUTPUTS		
DCBATOUT	5V_S5 3D3V_S5		
SYSTEM DC/DC		RT8209E	50
INPUTS	OUTPUTS		
DCBATOUT	1D5V_S3 0D75V_S0 DDR_VREP_S3		
SYSTEM DC/DC		ISL62881	54
INPUTS	OUTPUTS		
DCBATOUT	VCC GFXCORE_PWR		
VGA		RT8208B	55
INPUTS	OUTPUTS		
DCBATOUT	VGA_CORE		
TI CHARGER		BQ24745	53
INPUTS	OUTPUTS		
DCBATOUT	BT+		
SYSTEM DC/DC		RT9025	52
INPUTS	OUTPUTS		
3D3V_S0	1D8V_S0		
SYSTEM DC/DC		RT9025	56
INPUTS	OUTPUTS		
3D3V_VGA_S0	1D8V_VGA_S0		
Switches			
INPUTS	OUTPUTS		
1D5V_S3	1D5V_VGA_S0		
3D3V_S0	3D3V_VGA_S0		
1D05V_VTT	1V_VGA_S0		

PCB STACKUP



CardReader-->5138
 Audio---->271X

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PCH Strapping

Name	Schematics Notes
SPKR	Reboot option at power-up Default Mode: Internal weak Pull-down. No Reboot Mode with TCO Disabled: Connect to Vcc3_3 with 8.2-kΩ - 10-kΩ weak pull-up resistor.
INIT3_3V#	Weak internal pull-down. Do not pull high.
GNT3#/GPIO55	Default Mode: Internal pull-up. Low (0) = Top Block Swap Mode (Connect to ground with 4.7-kΩ weak pull-down resistor).
INTVRMEN	High (1) = Integrated VRM is enabled Low (0) = Integrated VRM is disabled
GNT0#, GNT1#	Default (SPI): Left both GNT0# and GNT1# floating. No pull up required. Boot from PCI: Connect GNT1# to ground with 1-kΩ pull-down resistor. Leave GNT0# Floating. Boot from LPC: Connect both GNT0# and GNT1# to ground with 1-kΩ pull-down resistor.
GNT2#/GPIO53	Default - Internal pull-up. Low (0) = Configures DMI for ESI compatible operation (for servers only. Not for mobile/desktops).
GPIO33	Default: Do not pull low. Disable MB in Manufacturing Mode: Connect to ground with 1-kΩ pull-down resistor.
SPI_MOSI	Enable iTPM: Connect to Vcc3_3 with 8.2-kΩ weak pull-up resistor Disable iTPM: Left floating, no pull-down required.
NV_ALE	Enable Danbury: Connect to Vcc3_3 with 8.2-kΩ weak pull-up resistor. Disable Danbury: Connect to ground with 4.7-kΩ weak pull-down resistor.
NC_CLE	Weak internal pull-up. Do not pull low.
HAD_DOCK_EN# /GPIO[33]	Low (0): Flash Descriptor Security will be overridden. High (1) : Flash Descriptor Security will be in effect.
HDA_SDO	Weak internal pull-down. Do not pull high.
HDA_SYNC	Weak internal pull-down. Do not pull high.
GPIO15	Weak internal pull-down. Do not pull high.
GPIO8	Weak internal pull-up. Do not pull low.
GPIO27	Default = Do not connect (floating) High(1) = Enables the internal VccVRM to have a clean supply for analog rails. No need to use on-board filter circuit. Low (0) = Disables the VccVRM. Need to use on-board filter circuits for analog rails.

Processor Strapping

Pin Name	Strap Description	Configuration (Default value for each bit is 1 unless specified otherwise)	Default Value
CFG[4]	Embedded DisplayPort Presence	1: Disabled - No Physical Display Port attached to Embedded DisplayPort. 0: Enabled - An external Display Port device is connected to the Embedded Display Port.	1
CFG[3]	PCI-Express Static Lane Reversal	1: Normal Operation. 0: Lane Numbers Reversed 15 -> 0, 14 -> 1, ...	1
CFG[0]	PCI-Express Configuration Select	1: Single PCI-Express Graphics 0: Bifurcation enabled	1
CFG[7]	Reserved - Temporarily used for early Clarksfield samples.	Clarksfield (only for early samples pre-ES1) - Connect to GND with 3.01K Ohm/5% resistor Note: Only temporary for early CFD samples (rPGA/BGA) [For details please refer to the WW33 MoW and sighting report]. For a common motherboard design (for AUB and CFD), the pull-down resistor should be used. Does not impact AUB functionality.	0

USB Table

Pair	Device
0	USB3
1	USB2
2	USB4
3	MINICARD1
4	WECAM
5	Touch Panel
6	NC
7	NC
8	NC
9	USB1 (HS)
10	Finger Print
11	Blue Tooth
12	MINIC2
13	Cardreader

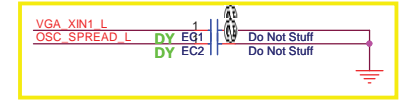
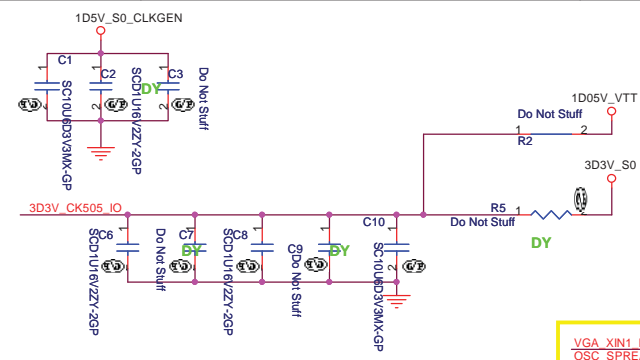
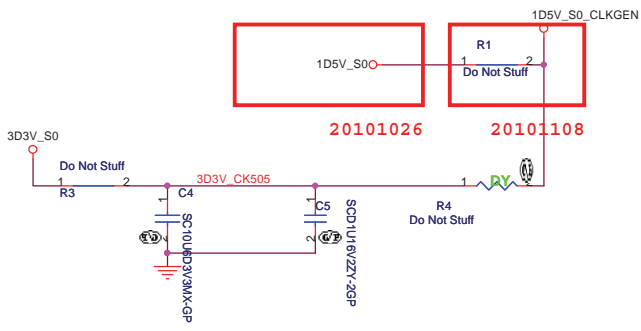
PCIE Routing

LANE1	LAN
LANE2	MiniCard1
LANE3	MiniCard2

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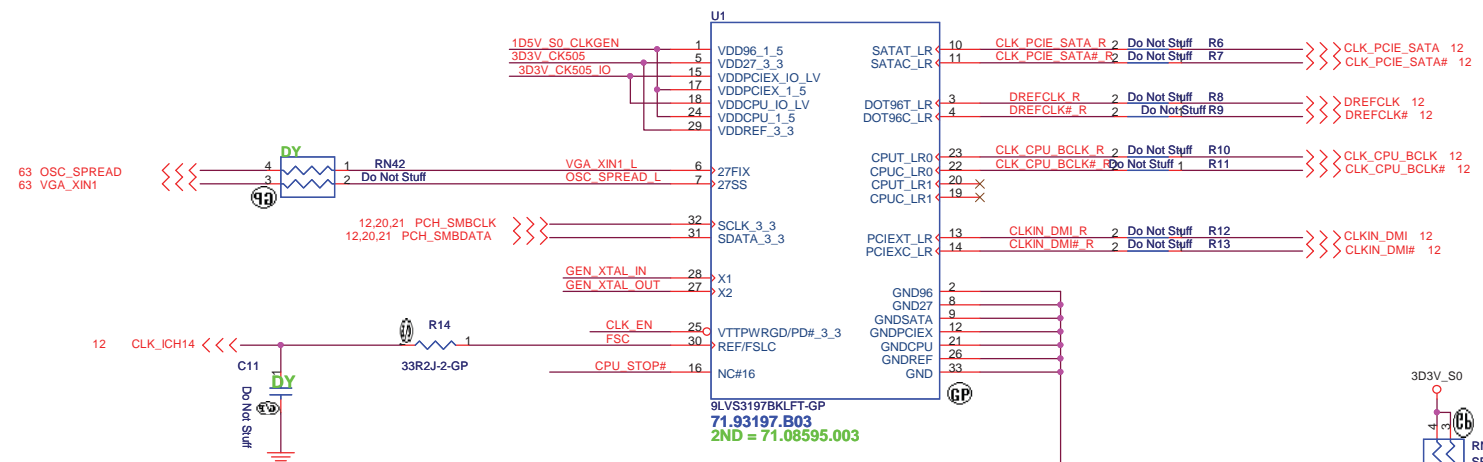
Hynix 1G 800M N11PGV SKU

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		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Table of Content			
Size A3	Document Number	Rev	
	JE43-CP	-1	
Date: Wednesday, November 24, 2010	Sheet 2	of	69

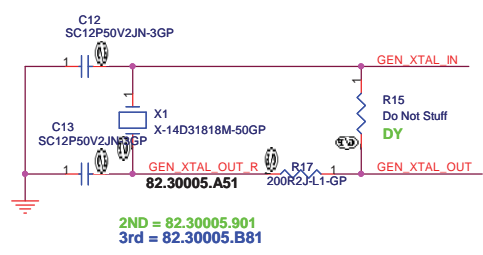


SA 0622 EMI

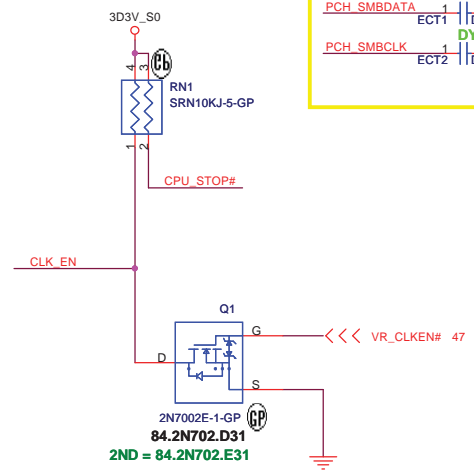
SA 0629 RF



FSC	0	1
SPEED	133MHz (Default)	100MHz



SB 0813 CL = 10pF
Freq tolerance : +/- 30 ppm

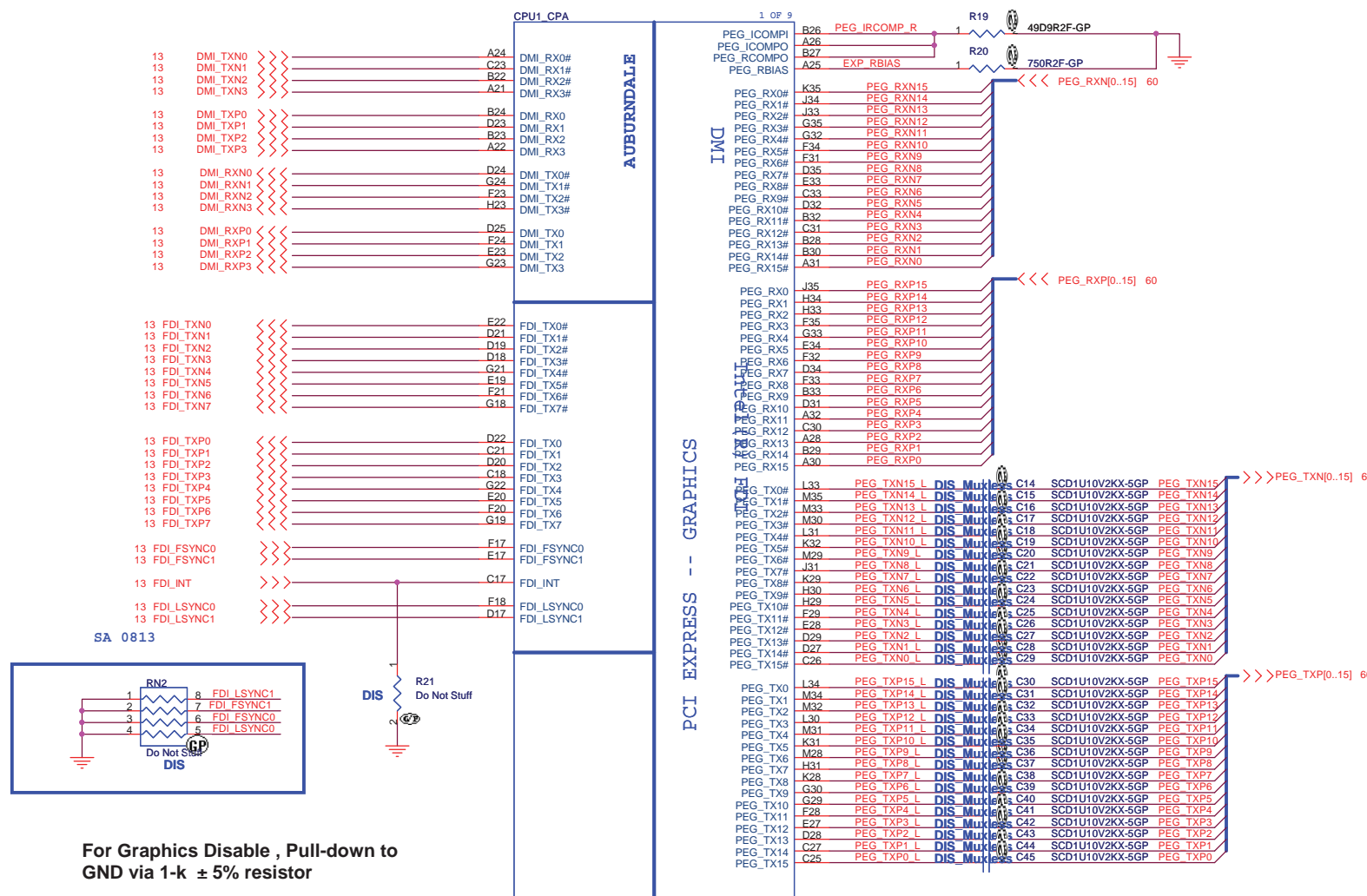


Hynix 1G 800M N11PGV SKU

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Title Clock Generator		
Size A3	Document Number JE43-CP	Rev -1
Date: Wednesday, November 24, 2010	Sheet 3	of 69

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For Graphics Disable , Pull-down to GND via 1-k ± 5% resistor

62.10055.321
 3RD = 62.10055.341
 4th = 62.10040.611
 2ND = 62.10053.561

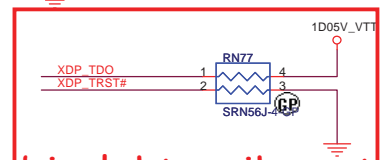
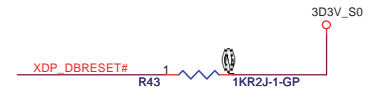
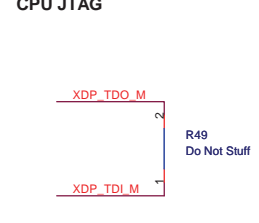
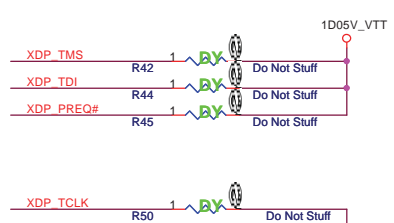
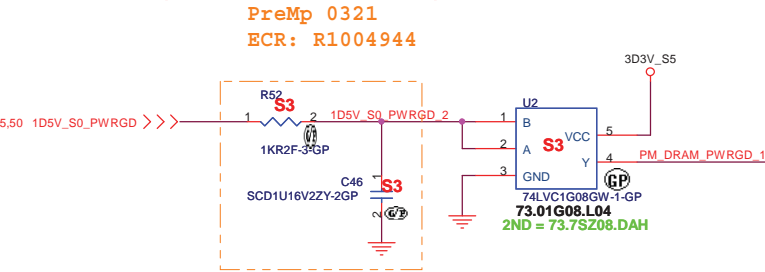
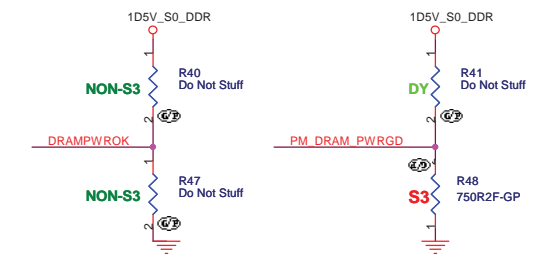
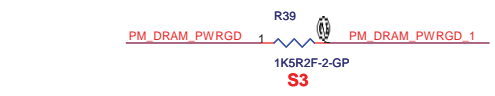
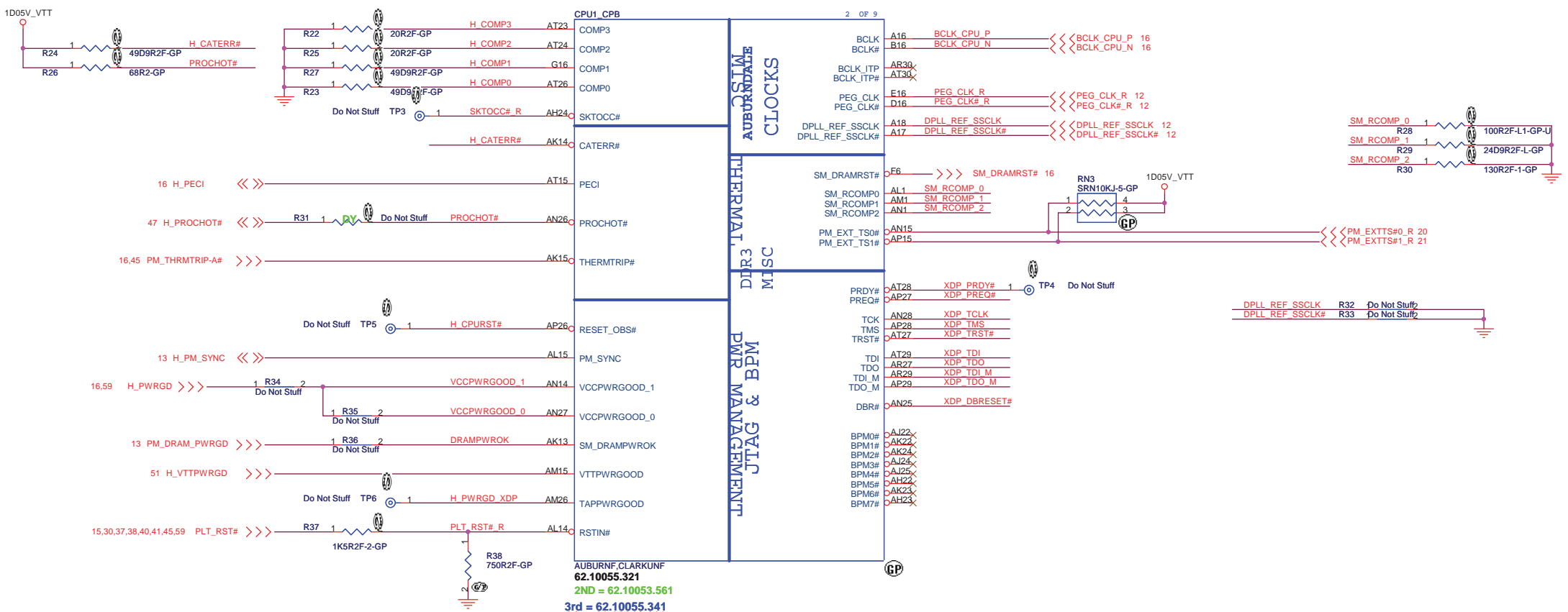
0113 -1
 del 3rd 62.10055.341 and 4th 62.10055.321
 3rd and 4th have been purged
 CE will confrim SQM if it can add BOM
 CE will release EC to add to BOM

lab stuff 2nd,3rd and 4 th in BOM
 Eng add 1st source(62.10040.611)
 Eng do not stuff 4 th in BOM
 because 4 th have been purge ,so stuff 1st in BOM
 but CE said, 4th need stuff in PD if not any

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Title: CPU (1/7)
 Size A3 Document Number JE43-CP Rev -1
 Date: Wednesday, November 24, 2010 Sheet 4 of 69



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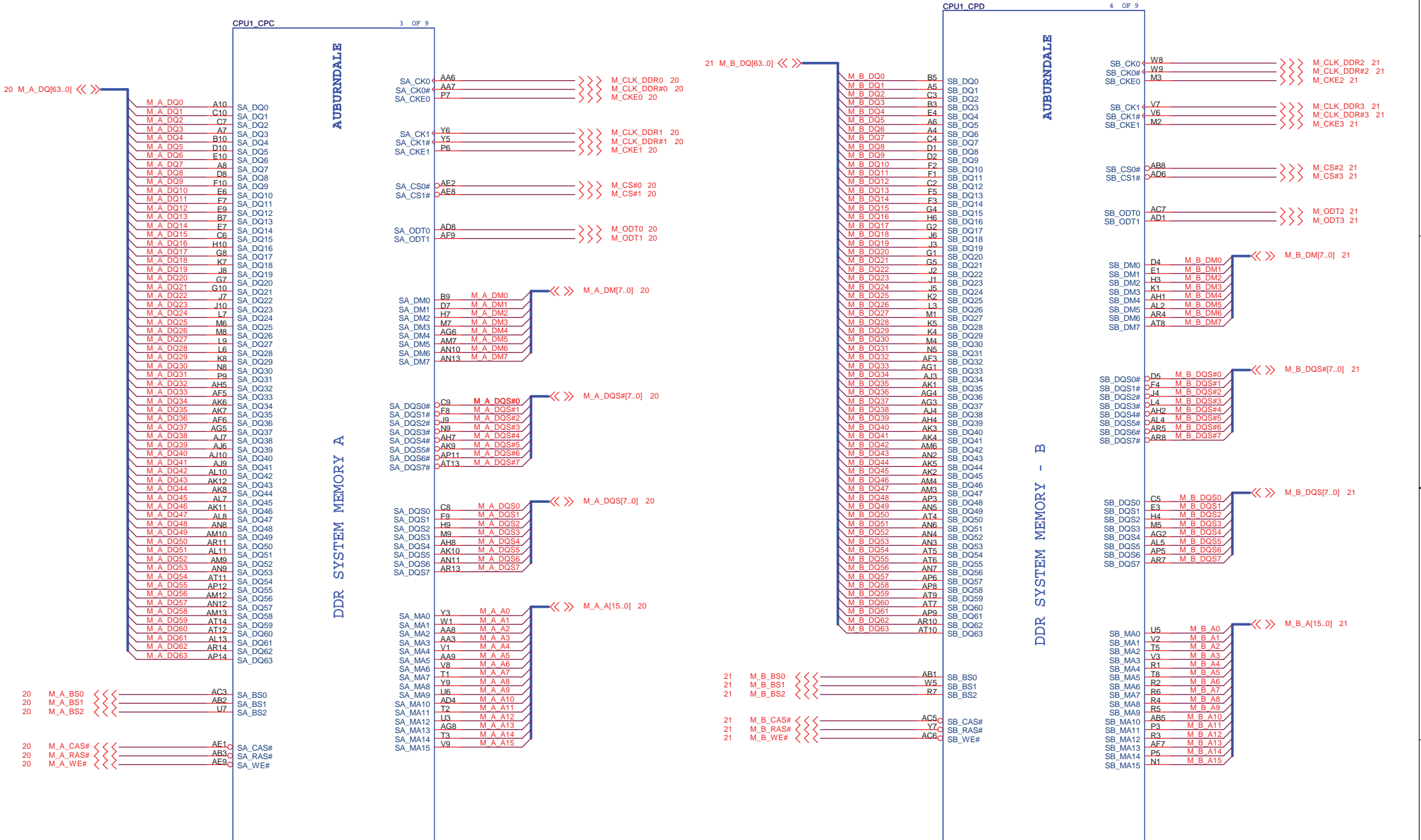
Hynix 1G 800M N11PGV SKU

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Title: **CPU (2/7)**

Size: A3 Document Number: **JE43-CP** Rev: **-1**

Date: Wednesday, November 24, 2010 Sheet 5 of 69



AUBURNF.CLARKUNF
62.10055.321

2ND = 62.10053.561
3rd = 62.10055.341
4th = 62.10040.611



AUBURNF.CLARKUNF
62.10055.321

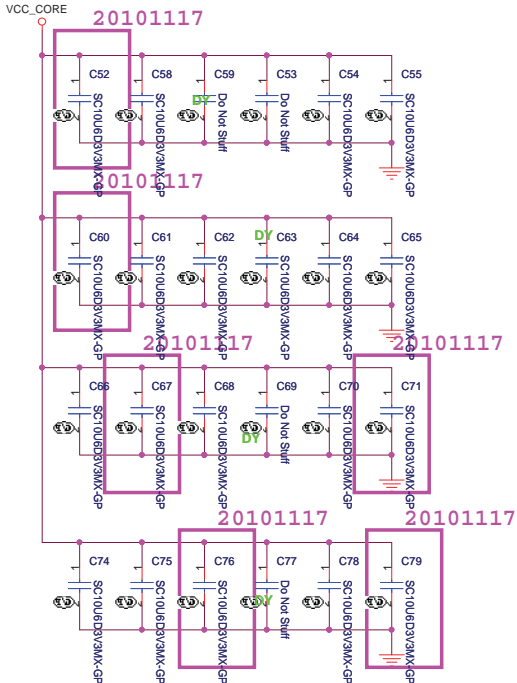
2ND = 62.10053.561
3rd = 62.10055.341
4th = 62.10040.611

Hynix 1G 800M GPV SKU

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Title CPU (3/7)		
Size A3	Document Number JE43-CP	Rev -1
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VCC_CORE
48A

PROCESSOR CORE POWER

- AG35 VCC
- AG34 VCC
- AG33 VCC
- AG32 VCC
- AG31 VCC
- AG30 VCC
- AG29 VCC
- AG28 VCC
- AG27 VCC
- AG26 VCC
- AF35 VCC
- AF34 VCC
- AF33 VCC
- AF32 VCC
- AF31 VCC
- AF30 VCC
- AF29 VCC
- AF28 VCC
- AF27 VCC
- AF26 VCC
- AD35 VCC
- AD34 VCC
- AD33 VCC
- AD32 VCC
- AD31 VCC
- AD30 VCC
- AD29 VCC
- AD28 VCC
- AD27 VCC
- AD26 VCC
- AC35 VCC
- AC34 VCC
- AC33 VCC
- AC32 VCC
- AC31 VCC
- AC30 VCC
- AC29 VCC
- AC28 VCC
- AC27 VCC
- AC26 VCC
- AA35 VCC
- AA34 VCC
- AA33 VCC
- AA32 VCC
- AA31 VCC
- AA30 VCC
- AA29 VCC
- AA28 VCC
- AA27 VCC
- AA26 VCC
- Y35 VCC
- Y34 VCC
- Y33 VCC
- Y32 VCC
- Y31 VCC
- Y30 VCC
- Y29 VCC
- Y28 VCC
- Y27 VCC
- Y26 VCC
- V35 VCC
- V34 VCC
- V33 VCC
- V32 VCC
- V31 VCC
- V30 VCC
- V29 VCC
- V28 VCC
- V27 VCC
- V26 VCC
- U35 VCC
- U34 VCC
- U33 VCC
- U32 VCC
- U31 VCC
- U30 VCC
- U29 VCC
- U28 VCC
- U27 VCC
- U26 VCC
- R35 VCC
- R34 VCC
- R33 VCC
- R32 VCC
- R31 VCC
- R30 VCC
- R29 VCC
- R28 VCC
- R27 VCC
- R26 VCC
- P35 VCC
- P34 VCC
- P33 VCC
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- P27 VCC
- P26 VCC

AUBURNDALE

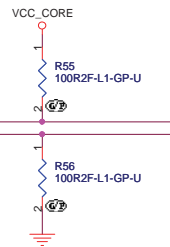
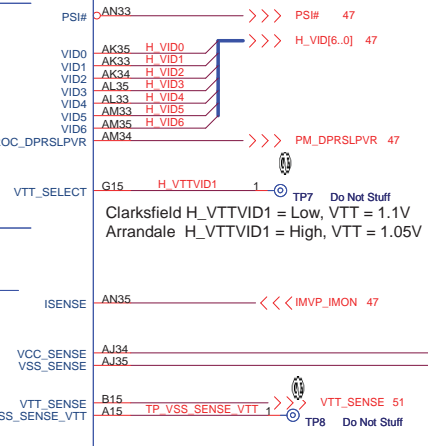
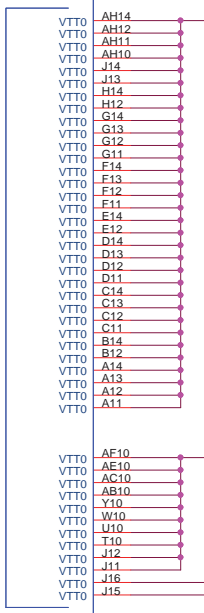
1.1V RAIL POWER

CPU CORE SUPPLY

POWER

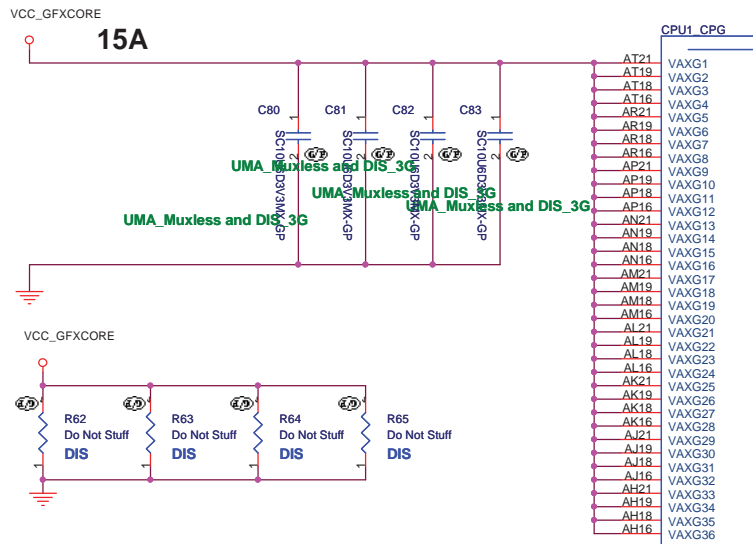
SPIN VIDS

SENSE LINES

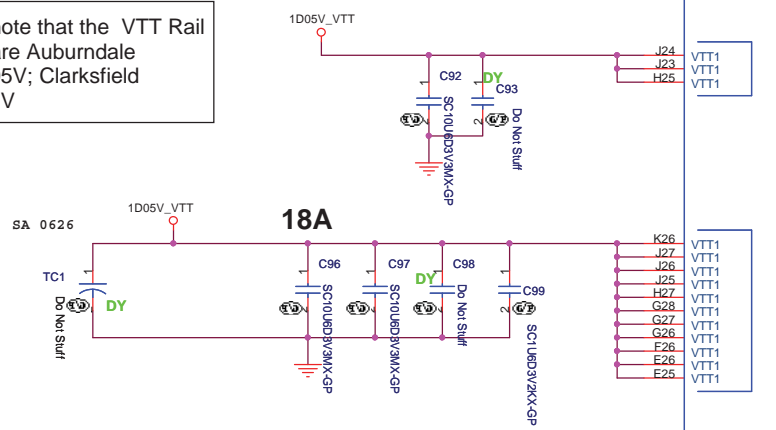


The decoupling capacitors, filter recommendations and sense resistors on the CPU/PCH Rails are specific to the CRB Implementation. Customers need to follow the recommendations in the Calpella Platform Design Guide.

Please note that the VTT Rail Values are Auburndale VTT=1.05V; Clarkfield VTT=1.1V

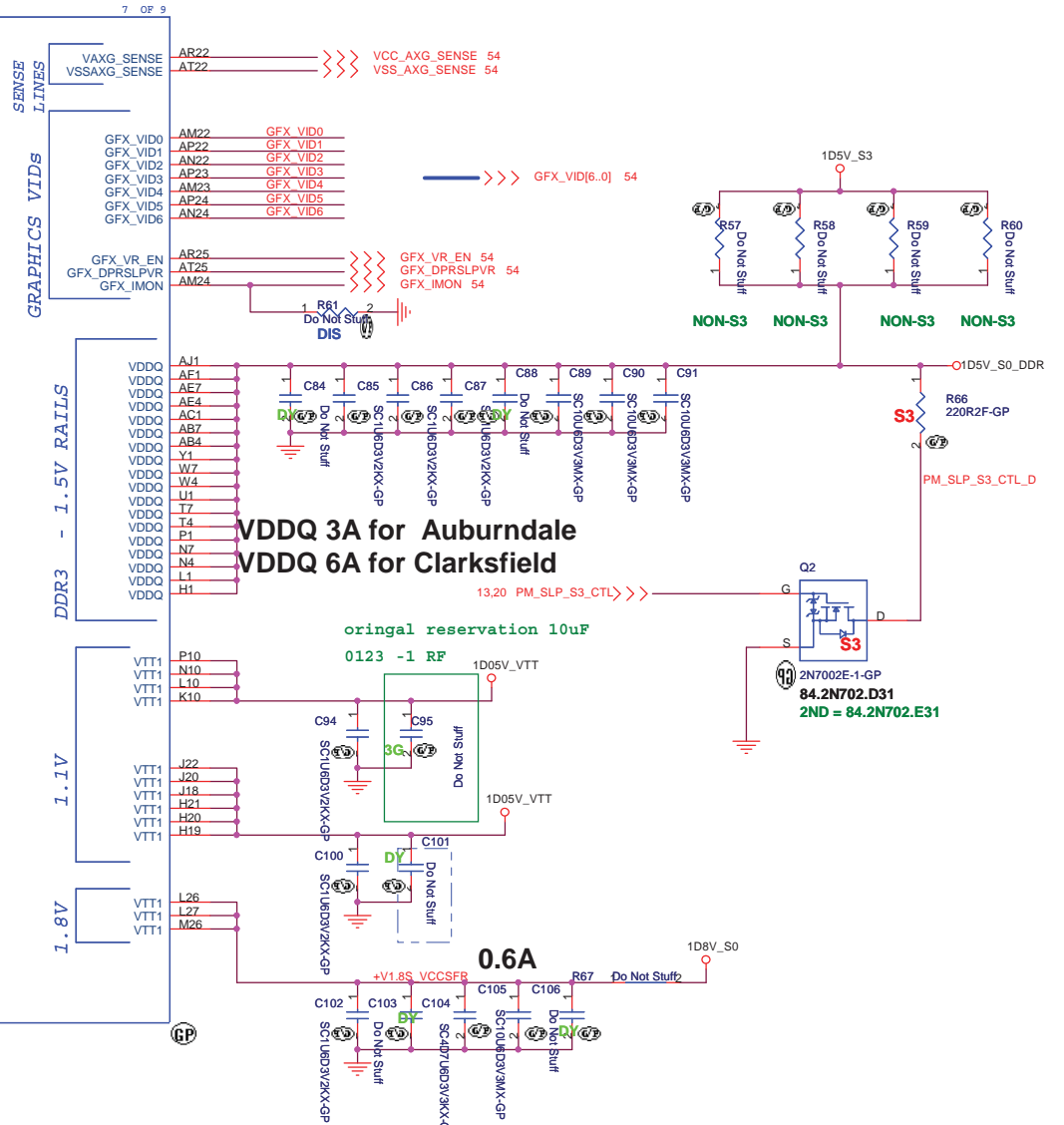


Please note that the VTT Rail Values are Auburndale VTT=1.05V; Clarksfield VTT=1.1V



AUBURNF,CLARKUNF
62.10055.321
 2ND = 62.10053.561
 3rd = 62.10055.341
 4th = 62.10040.611

GRAPHICS
POWER
PEG & DMI



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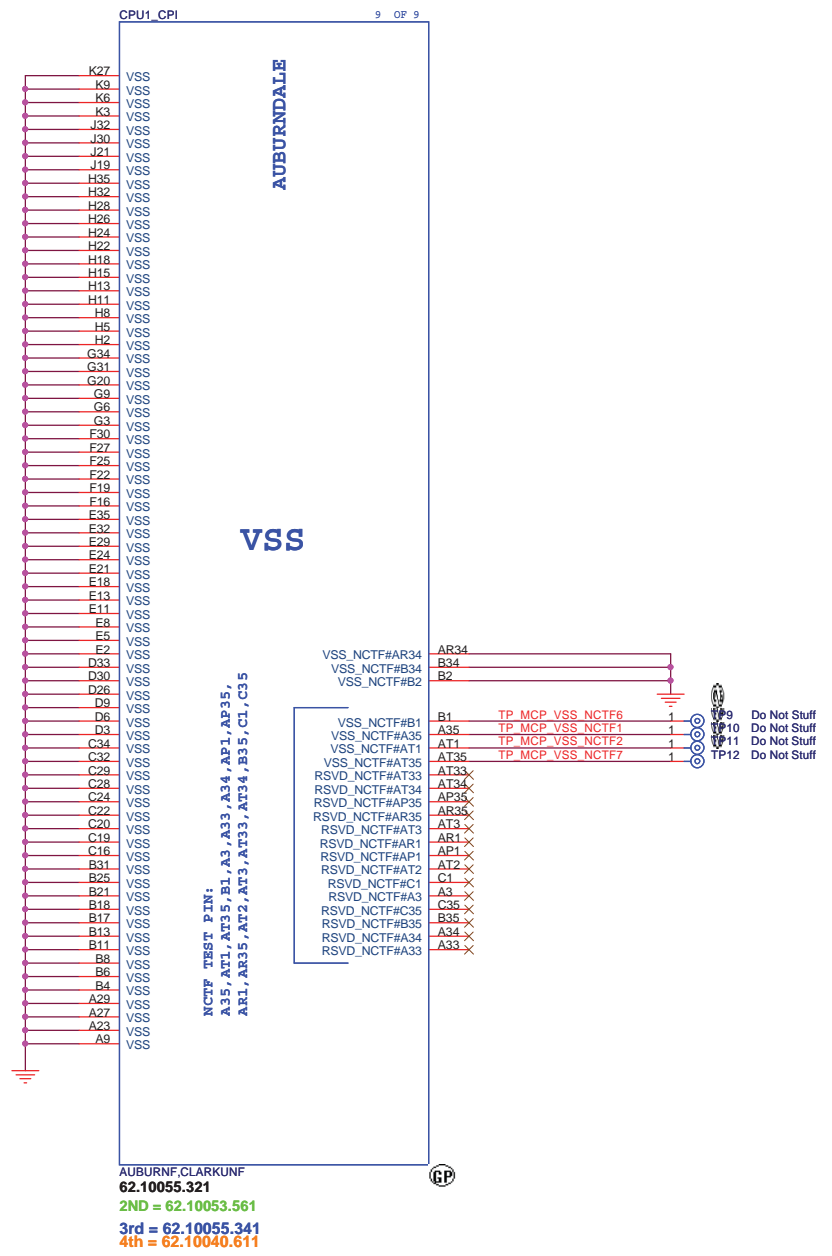
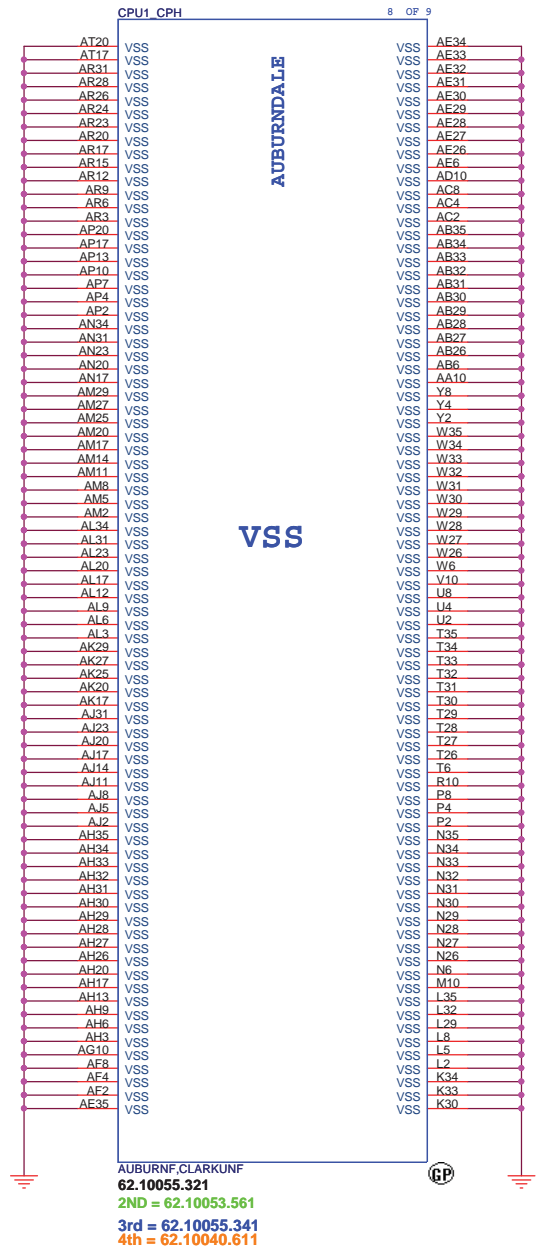
Hynix 1G 800M N11PGV SKU

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Title: **CPU (5/7)**

Size A3	Document Number JE43-CP	Rev -1
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Hynix 1G 800M N11PGV SKU

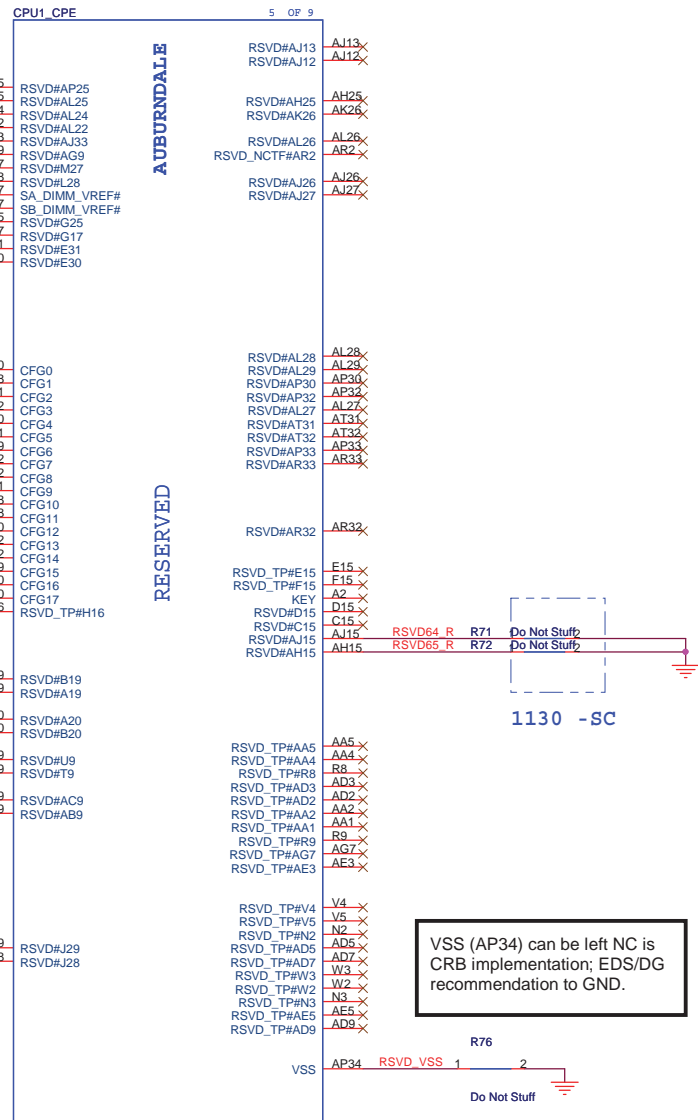
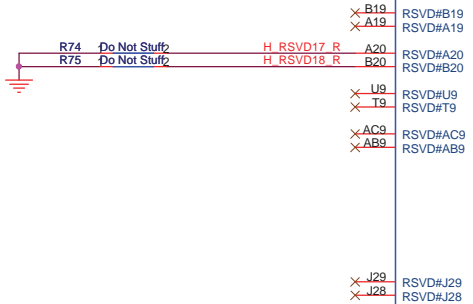
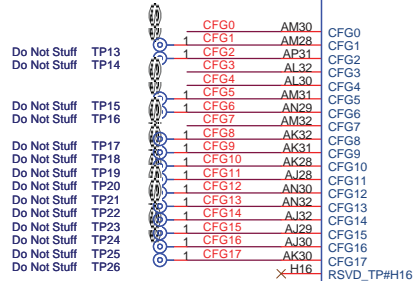
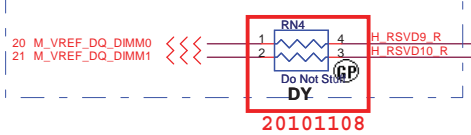
緯創資通 Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title CPU (6/7)

Size A3 Document Number JE43-CP Rev -1

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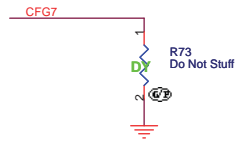
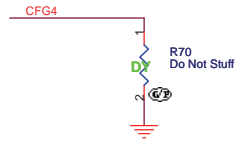
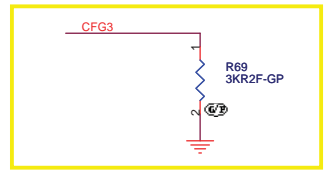
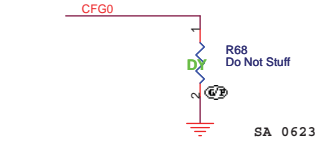
SO-DIMM VREFDQ (M3) Circuit for Clarkfield Processor



AUBURNF,CLARKUNF
62.10055.321
 2ND = 62.10053.561
 3rd = 62.10055.341
 4th = 62.10040.611

VSS (AP34) can be left NC is CRB implementation; EDS/DG recommendation to GND.

Processor Strapping



PCI-Express Configuration Select	
CFG0	1: Single PEG(Default) 0: Bifurcation enabled

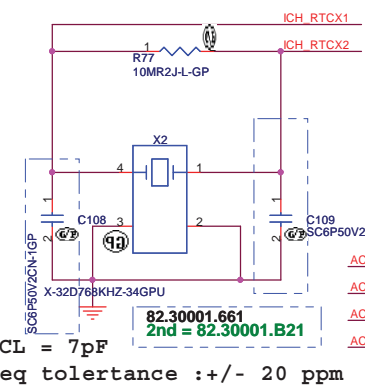
CFG3 - PCI-Express Static Lane Reversal	
CFG3	1 : Normal Operation(Default) 0 : Lane Numbers Reversed 15 -> 0, 14 -> 1, ...

CFG4 - Display Port Presence	
CFG4	1: Disabled; No Physical Display Port attached to Embedded Display Port (Default) 0: Enabled; An external Display Port device is connected to the Embedded Display Port

CFG7(Reserved) - Temporarily used for early Clarkfield samples.	
CFG7	Clarkfield (only for early samples pre-ES1) - Connect to GND with 3.01K Ohm/5% resistor. Note: Only temporary for early CFD sample (rPGA/BGA) [For details please refer to the WW33 MoW and sighting report]. For a common M/B design (for AUB and CFD), the pull-down resistor should be used. Does not impact AUB functionality.

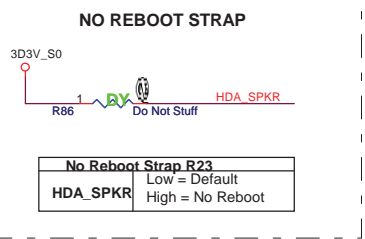
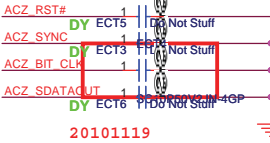
Hynix 1G 800M N11PGV SKU

緯創資通 Wistron Corporation	
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hstchih, Taipei Hsien 221, Taiwan, R.O.C.	
Title CPU (7/7)	
Size A3	Document Number JE43-CP
Date: Wednesday, November 24, 2010	Sheet 10 of 69
	Rev -1

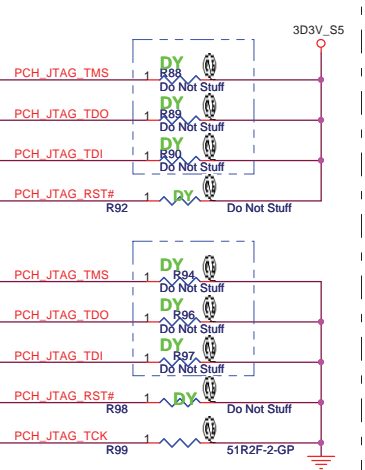


CL = 7pF
 Freq tolertance : +/- 20 ppm

- 32 HDA_CODEC_RST#
- 32 HDA_CODEC_SYNC
- 32 HDA_CODEC_BITCLK
- 32 HDA_CODEC_SDOUT

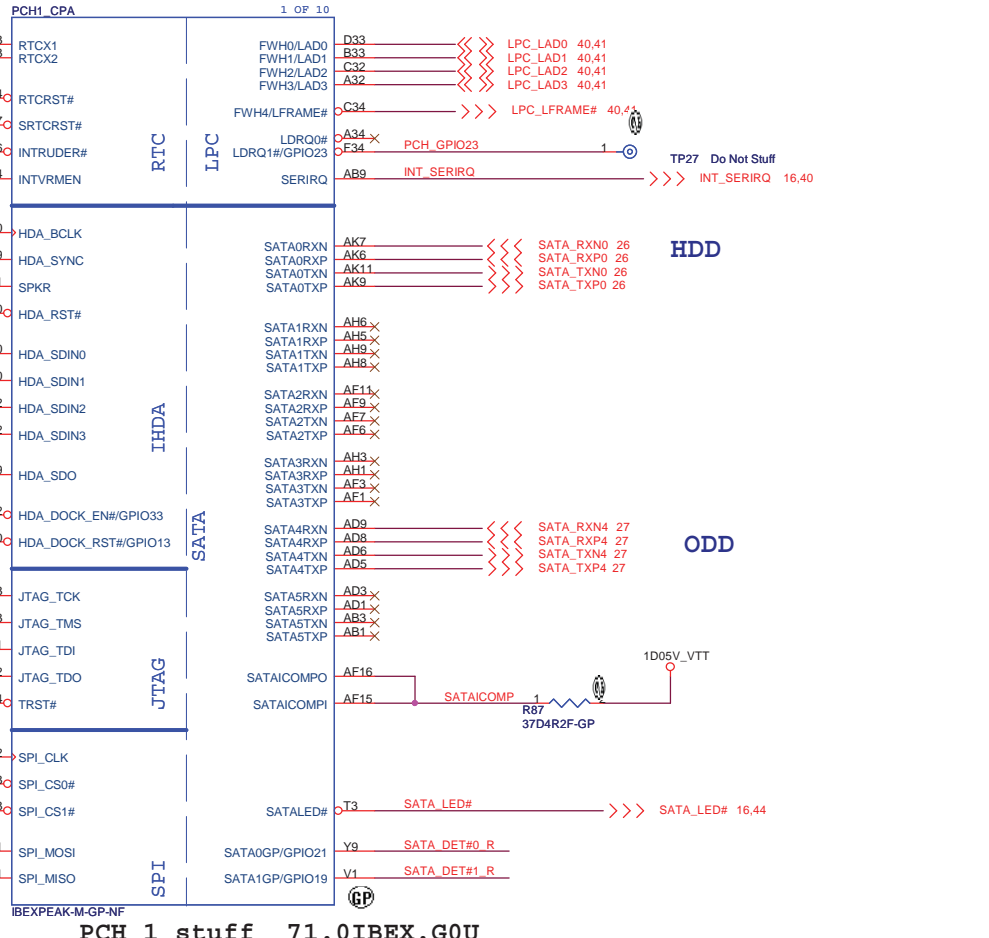
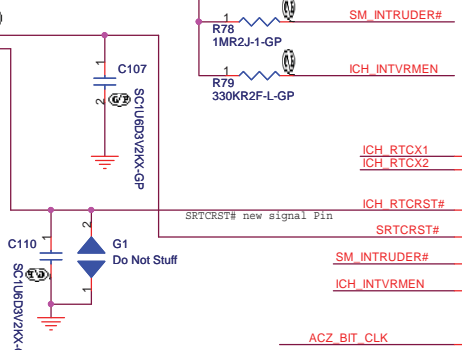


For after PCH stepping B3,have to DY,



When unused all JTAG pins may be NC

INTVRMEN- Integrated SUS 1.1V VRM Enable High - Enable internal VRs



integrated VccSus1_05,VccSus1_5,VccCL1_5		
INTVRMEN	High=Enable	Low=Disable
integrated VccLan1_05VccCL1_05		
LAN100_SLIP	High=Enable	Low=Disable

32 HDA_SPKR <<<

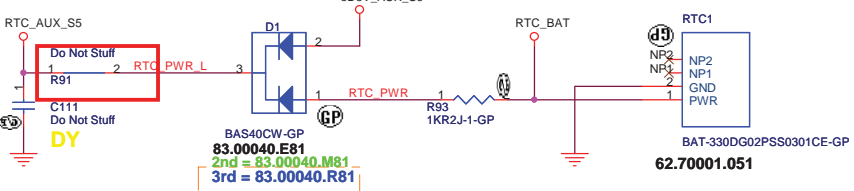
HDD

ODD

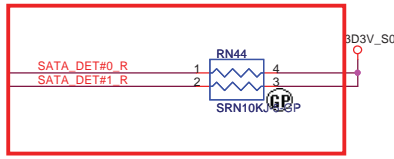
SPI_CS0#, SPI_MISO, SPI_MOSI, SPI_CLK:
 No series resistor required if routing length is 1.5"-6.5"

PCH Strapping

SPI_MOSI Enable iTPM: Connect to Vcc3_3 with 8.2-kΩ weak pull-up resistor. Disable iTPM: Left floating, no pull-down required



83.00040.Q81 is ROHS parts
 83.00040.R81 is Halogens free Part
 arrange qual in Eng SKU



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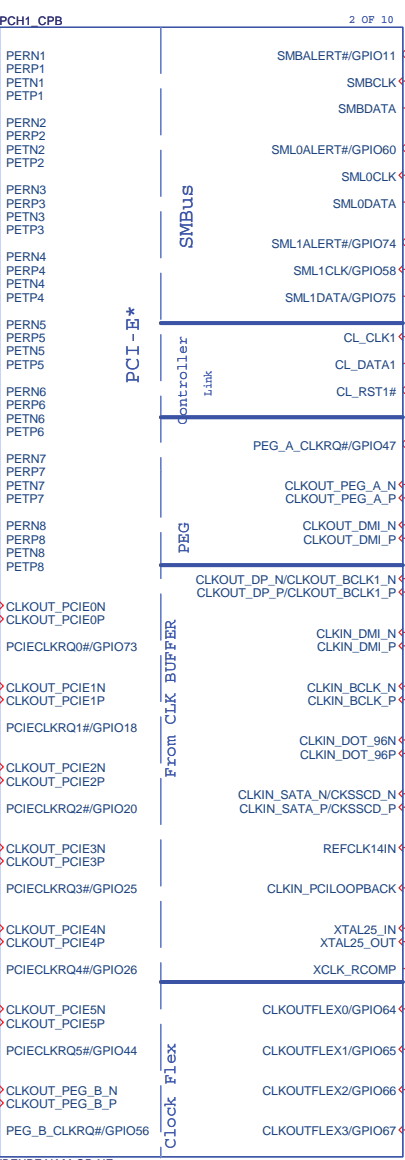
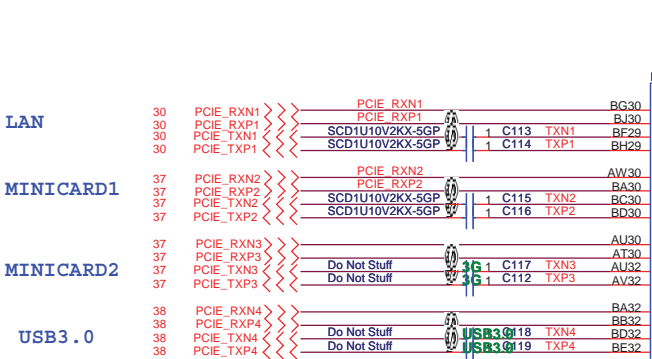
Hynix 1G 800M N11PGV SKU

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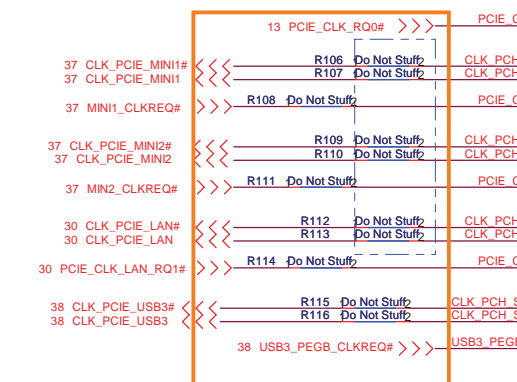
Title: PCH (1/9)

Size A3 Document Number JE43-CP Rev -1

Date: Wednesday, November 24, 2010 Sheet 11 of 69

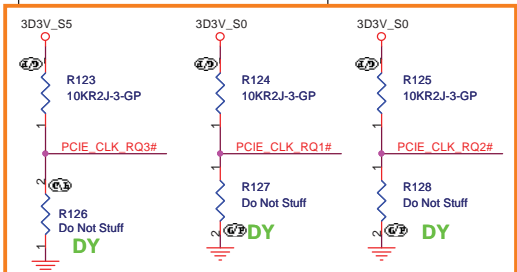


0721
1.R108 2.R111 3.R114
the three resistors should be moated



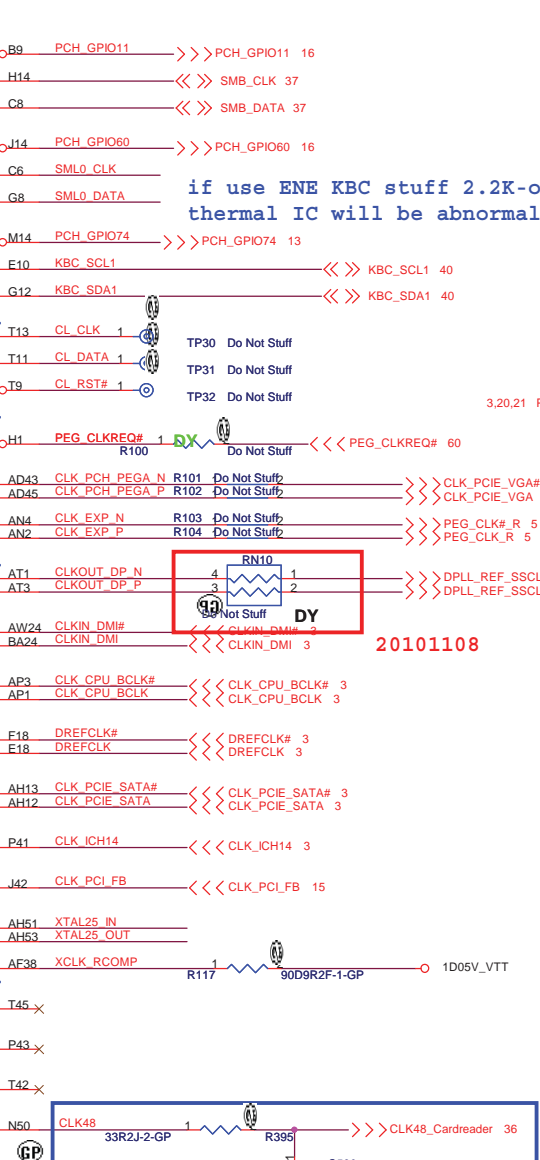
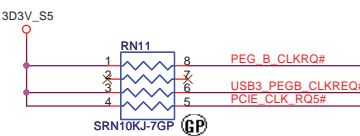
PCIECLKRQ{0,3,4,5,6,7}# should have a 10K pull-up to +3VALW.

PCIECLKRQ{1,2} should have a 10K pull-up to +1.05VS (But CRB is pull-up to +3VS).



20100920

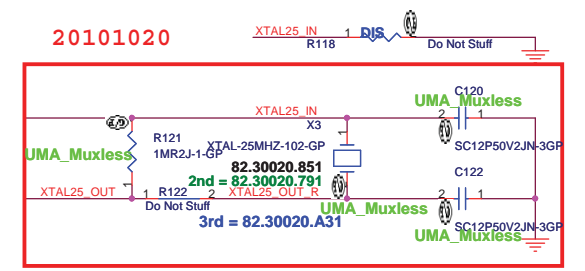
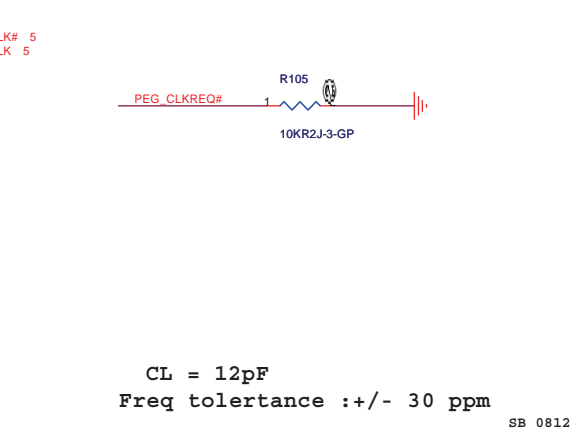
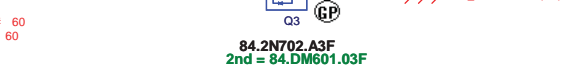
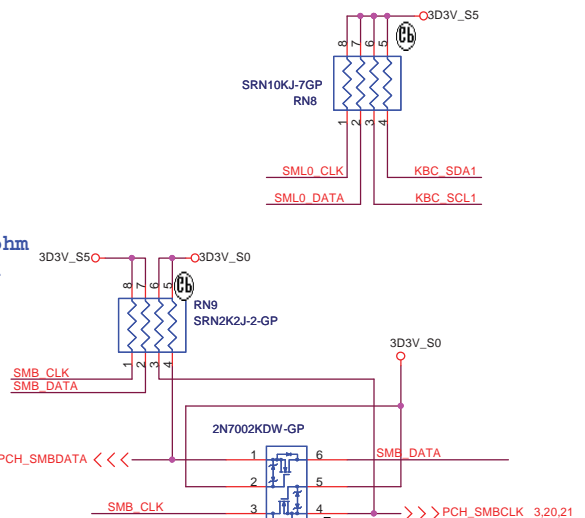
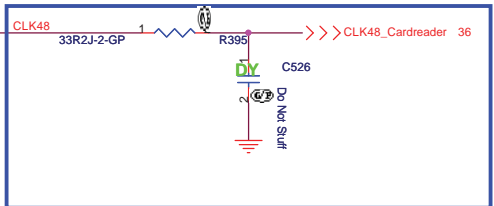
20100920



if use ENE KBC stuff 2.2K-ohm thermal IC will be abnormal



20101108



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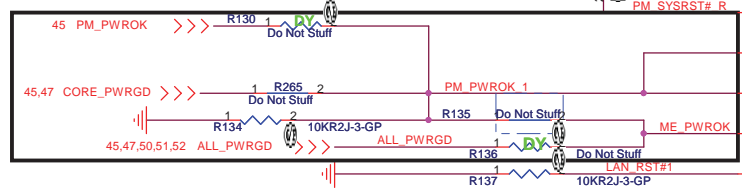
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Title: PCH (2/9)

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0804 SA
 1.cause of thermal sensor
 2.solution by JM31-CP

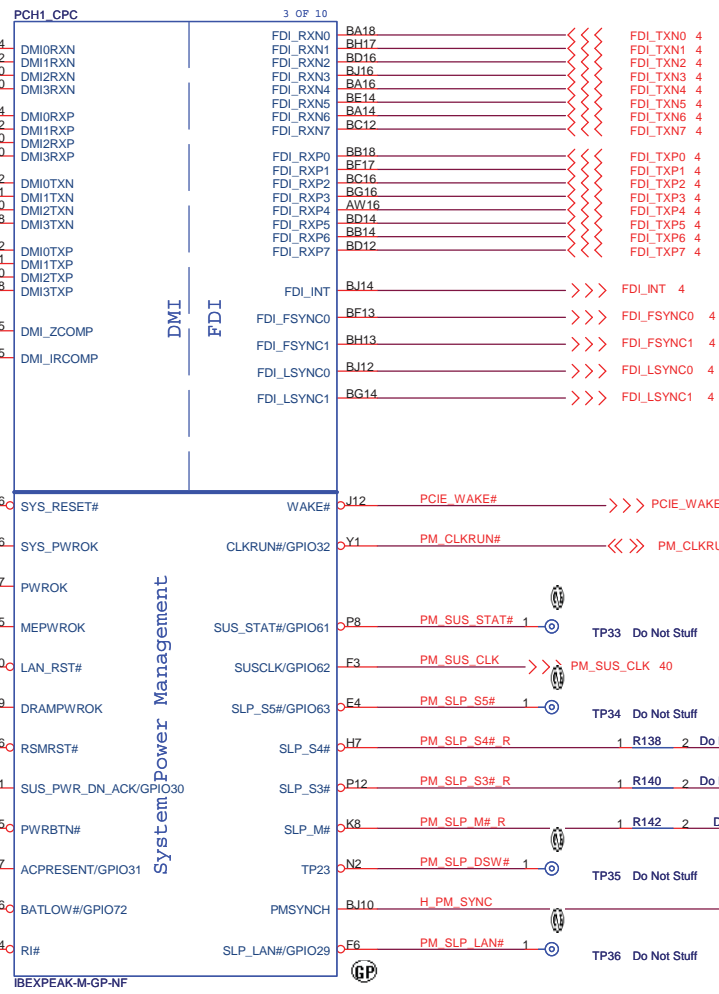
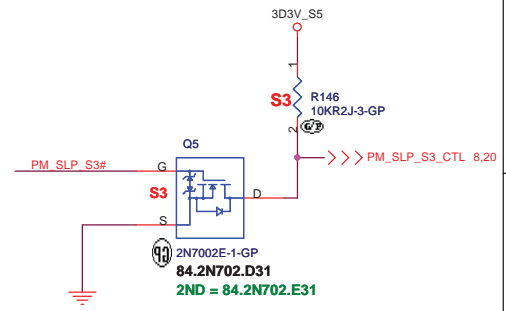
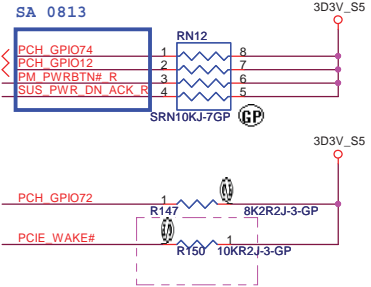
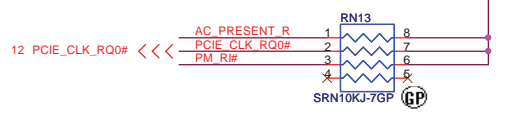
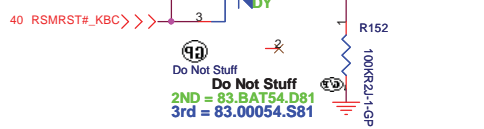
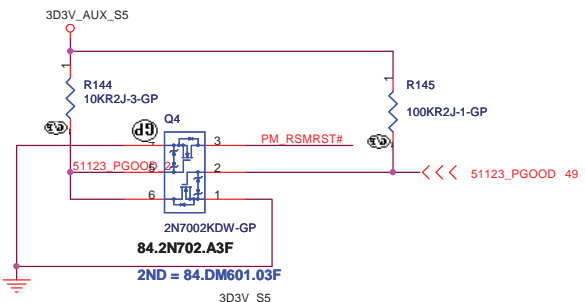


5 PM_DRAM_PWRGD <<< PM_DRAM_PWRGD

40 SUS_PWR_DN_ACK <<< 1 R139 2 Do Not Stuff SUS_PWR_DN_ACK R

40,59 PM_PWRBTN# >>> 1 R141 2 Do Not Stuff PM_PWRBTN# R

40 AC_PRESENT >>> 1 R143 2 Do Not Stuff AC_PRESENT R



change pull up 1K to 10K for Intel suggestion

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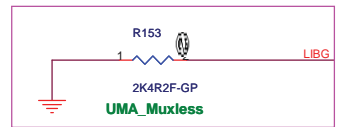
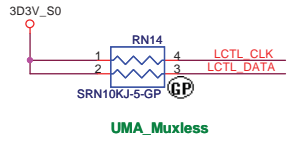
Hynix 1G 800M N11PGV SKU

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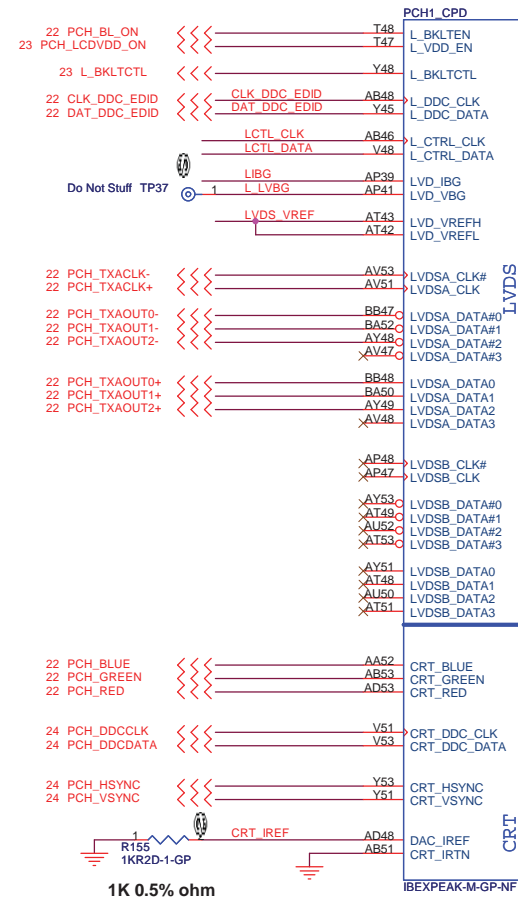
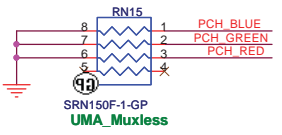
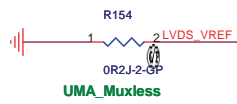
Title: **PCH (3/9)**

Size A3 Document Number: **JE43-CP** Rev: **-1**

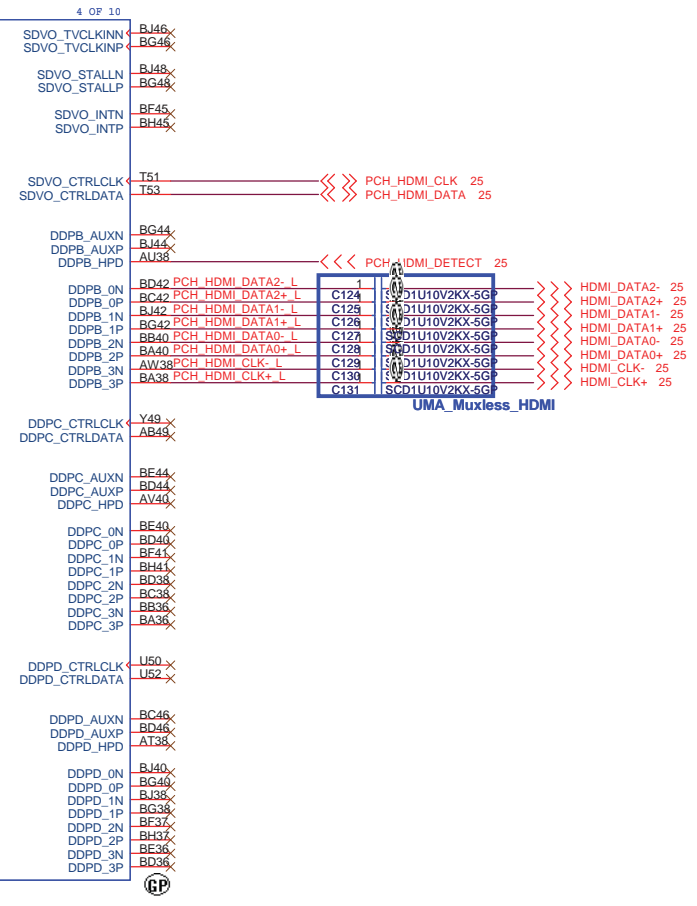
Date: Wednesday, November 24, 2010 Sheet 13 of 69



Muxless->64.23715.6DL,UMA-2.4K



Digital Display Interface



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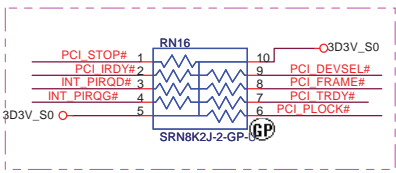
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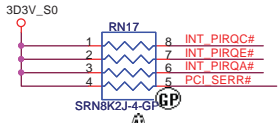
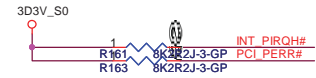
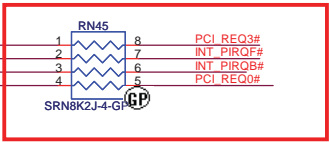
Title: PCH (4/9)

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These pins are left as NC, because the function is disable.



PCH strapping

BOOT BIOS Strap		
GNT#0	GNT#1	BOOT BIOS Location
0	0	LPC
1	0	Reserved
floating	0	PCI
floating	floating	SPI (Default)

PCI_GNT#1	Default (internal pull-up)
1	Default (internal pull-up)
0	Configures DMI for ESI compatible operation (Not for Mobile platform)

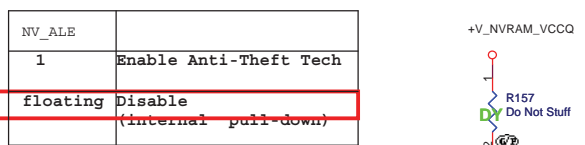
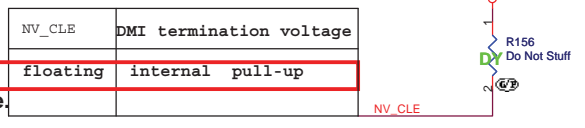
- 41 PCLK_FWH
- 12 CLK_PCI_FB
- 40 CLK_PCI_KBC



- H40 AD0
- N34 AD1
- C44 AD2
- A38 AD3
- C36 AD4
- J34 AD5
- A40 AD6
- D45 AD7
- E36 AD8
- H48 AD9
- E40 AD10
- C40 AD11
- M48 AD12
- M45 AD13
- F53 AD14
- M40 AD15
- M43 AD16
- J36 AD17
- K48 AD18
- F40 AD19
- C42 AD20
- K46 AD21
- M51 AD22
- J52 AD23
- K51 AD24
- L34 AD25
- F42 AD26
- J40 AD27
- G46 AD28
- F44 AD29
- M47 AD30
- H36 AD31
- J50 C/BE#0
- G42 C/BE#1
- H47 C/BE#2
- G34 C/BE#3
- G38 PIRQA#
- H51 PIRQB#
- B37 PIRQC#
- A44 PIRQD#
- F51 REQ0#
- A46 REQ1#
- E45 REQ2#
- M53 REQ3#
- F48 GNT0#
- K46 GNT1#
- F36 GNT2#
- H53 GNT3#
- B41 PIRQE#/GPIO2
- K53 PIRQF#/GPIO3
- A36 PIRQG#/GPIO4
- A48 PIRQH#/GPIO5
- K6 PCIRST#
- E44 SERR#
- E50 PERR#
- A42 PCI IRDY#
- H44 PCI DEVSEL#
- F46 PCI FRAME#
- C46 PCI PLOCK#
- D49 PCI STOP#
- C48 PCI TRDY#
- M7 ICH PME#
- D5 PCI PLTRST#
- N52 CLKOUT_PCIO
- P53 CLKOUT_PC1
- P46 CLKOUT_PC2
- P51 CLKOUT_PC3
- P48 CLKOUT_PC4

- AY9 NV_CEO#
- BD1 NV_CE#1
- AP15 NV_CE#2
- BD8 NV_CE#3
- AV9 NV_DQ#0
- BG8 NV_DQ#1
- AP7 NV_DQ#2
- AP6 NV_DQ#3
- AT6 NV_DQ#4
- BB1 NV_DQ#5
- AV6 NV_DQ#6
- BB3 NV_DQ#7
- BA4 NV_DQ#8
- BE4 NV_DQ#9
- BB6 NV_DQ#10
- BD6 NV_DQ#11
- BB7 NV_DQ#12
- BC8 NV_DQ#13
- B8 NV_DQ#14
- B6 NV_DQ#15
- BD3 NV_ALE
- AY6 NV_CLE
- AU2 NV_RCOMP
- AV7 NV_RB#
- AY8 NV_WR#0_RE#
- AY5 NV_WR#1_RE#
- AV11 NV_WE#_CK0
- BE5 NV_WE#_CK1
- H18 USBP#0
- J18 USBP#1
- A18 USBP#2
- C18 USBP#3
- M20 USBP#4
- F20 USBP#5
- J20 USBP#6
- L20 USBP#7
- F20 USBP#8
- L20 USBP#9
- F20 USBP#10
- C20 USBP#11
- M22 USBP#12
- N22 USBP#13
- B21 USBP#14
- D21 USBP#15
- H22 USBP#16
- J22 USBP#17
- E22 USBP#18
- F22 USBP#19
- C22 USBP#20
- G24 USBP#21
- H24 USBP#22
- L24 USBP#23
- M24 USBP#24
- A24 USBP#25
- C24 USBP#26
- B25 USBRBIAS#
- D25 USBRBIAS
- N16 USB_OC#0
- J16 USB_OC#1
- F16 USB_OC#2
- E16 USB_OC#3
- E14 USB_OC#4
- G16 USB_OC#5
- E12 USB_OC#6
- I15 USB_OC#7
- N16 USB_OC#0
- J16 USB_OC#1
- F16 USB_OC#2
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- G16 USB_OC#5
- E12 USB_OC#6
- I15 USB_OC#7

PCH strapping

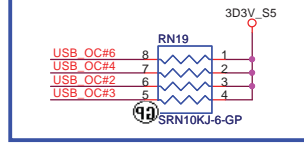
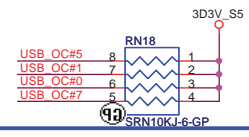


DMI Termination Voltage	
NV_CLE	Set to Vss when low. Set to Vcc when high.

USB

Pair	Device
0	I/O USB2.0
1	USB2.0
2	NC
3	MINICARD1 (WLAN)
4	WECAM
5	NC
6	NC
7	NC
8	3G SIM Card
9	USB 2.0
10	NC
11	Blue Tooth
12	MINIC2 (3G)
13	Cardreader

0806 SA for GPIO_table



SA 0813

PCH strapping

A16 swap override Strap/Top-Block Swap Override jumper	
PCI_GNT#3	Low = A16 swap override/Top-Block Swap Override enabled High = Default

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Title: **PCH (5/9)**

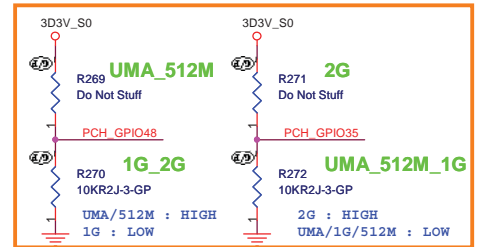
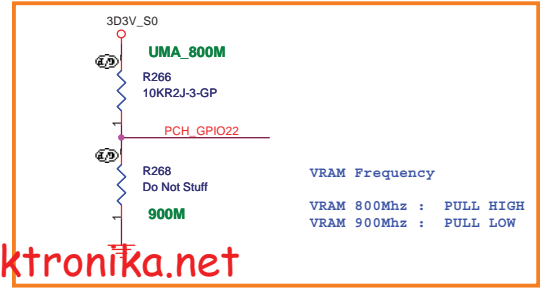
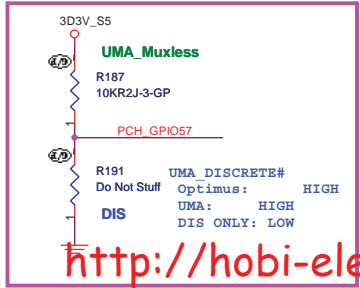
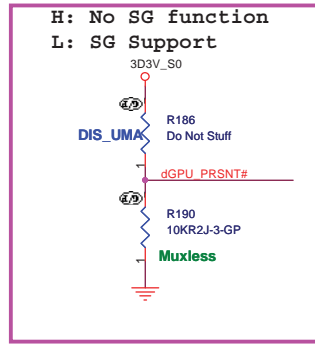
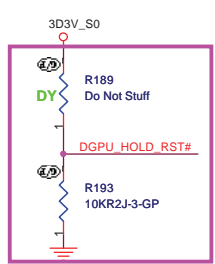
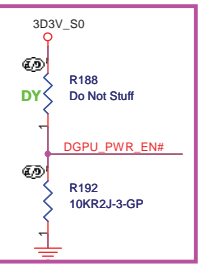
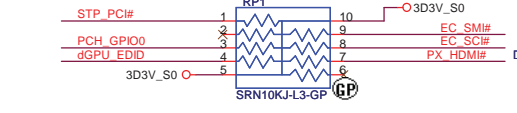
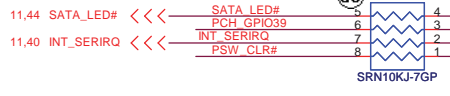
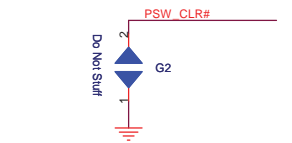
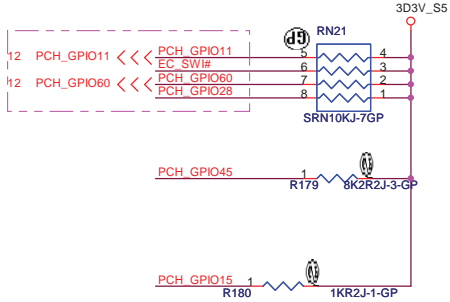
Size A3 | Document Number: **JE43-CP** | Rev: **-1**

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GPIO8 has a weak[20K] internal pull down.
No need to have external pull down/up.
GPIO8 pin set to high at reset.

GPIO15 has a weak[20K] internal pull down.
No need to have external pull up/down.
GPIO 15 pin is set to low at reset.
Low : ME Crypto TLS with no confidentiality
High : ME Crypto TLS with confidentiality

GPIO27 has a weak[20K] internal pull up.
To enable on-die PLL Voltage regulator,
should not place external pull down.

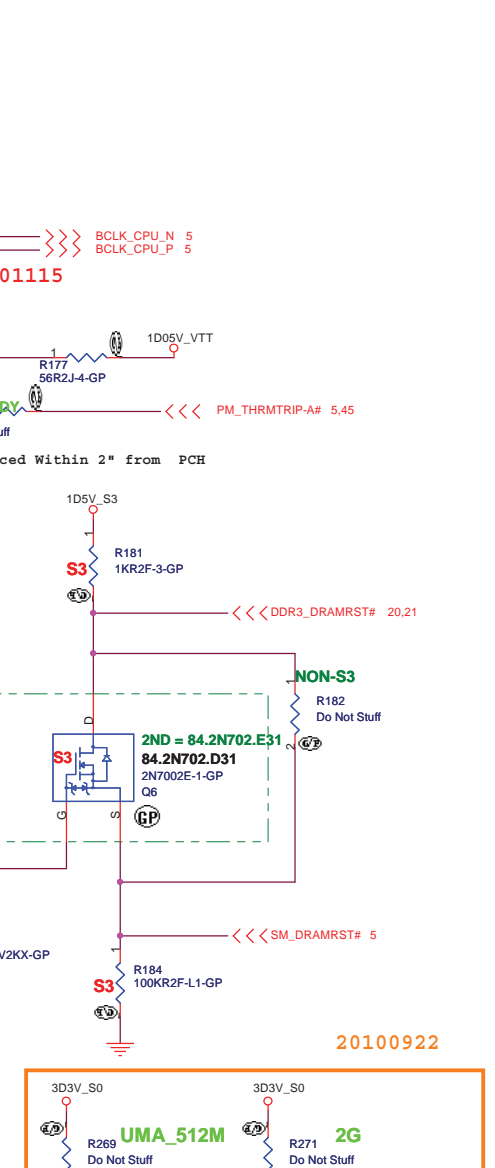


Signal	Pin	Function
PCH_GPIO0	Y3	BMBUSY#/GPIO0
EC_SMI#	C38	TACH1/GPIO1
25 PX_HDM#	D37	TACH2/GPIO6
EC_SCI#	J32	TACH3/GPIO7
40 EC_SWI#	F10	GPIO8
13 PCH_GPIO12	K9	LAN_PHY_PWR_CTRL/GPIO12
PCH_GPIO15	T7	GPIO15
60 DGPU_HOLD_RST#	AA2	SATA4GP/GPIO16
55,56 DGPU_PWROK	F38	TACH0/GPIO17
PCH_GPIO22	Y7	SCLOCK/GPIO22
1 PCH_GPIO24	H10	GPIO24
1 PCH_GPIO27	AB12	GPIO27
1 PCH_GPIO28	V13	GPIO28
STP_PCI#	M11	STP_PCI#/GPIO34
PCH_GPIO35	V6	SATACLKREQ#/GPIO35
56 DGPU_PWR_EN#	AB7	SATA2GP/GPIO36
dGPU_PRSENT#	AB13	SATA3GP/GPIO37
Do Not Stuff TP47	V3	SLOAD/GPIO38
PCH_GPIO39	P3	SDATAOUT0/GPIO39
PCH_GPIO45	H3	PCIECLKRQ6#/GPIO45
RST_GATE	F1	PCIECLKRQ7#/GPIO46
PCH_GPIO48	AB6	SDATAOUT1/GPIO48
PSW_CLR#	AA4	SATA5GP/GPIO49
PCH_GPIO57	F8	GPIO57
B4	B4	VSS_NCTF_8
B52	B52	VSS_NCTF_9
BH2	BH2	VSS_NCTF_16
BH52	BH52	VSS_NCTF_17
D2	D2	VSS_NCTF_28
A4	A4	VSS_NCTF#A4
A49	A49	VSS_NCTF#A49
A5	A5	VSS_NCTF#A5
A50	A50	VSS_NCTF#A50
A52	A52	VSS_NCTF#A52
A53	A53	VSS_NCTF#A53
B2	B2	VSS_NCTF#B2
B53	B53	VSS_NCTF#B53
BE1	BE1	VSS_NCTF#BE1
BE53	BE53	VSS_NCTF#BE53
BF1	BF1	VSS_NCTF#BF1
BF53	BF53	VSS_NCTF#BF53
BH1	BH1	VSS_NCTF#BH1
BH53	BH53	VSS_NCTF#BH53
BJ1	BJ1	VSS_NCTF#BJ1
BJ2	BJ2	VSS_NCTF#BJ2
BJ4	BJ4	VSS_NCTF#BJ4
BJ49	BJ49	VSS_NCTF#BJ49
BJ5	BJ5	VSS_NCTF#BJ5
BJ50	BJ50	VSS_NCTF#BJ50
BJ52	BJ52	VSS_NCTF#BJ52
BJ53	BJ53	VSS_NCTF#BJ53
D1	D1	VSS_NCTF#D1
D53	D53	VSS_NCTF#D53
E1	E1	VSS_NCTF#E1
E53	E53	VSS_NCTF#E53

Signal	Pin	Function
B4	B4	VSS_NCTF_8
B52	B52	VSS_NCTF_9
BH2	BH2	VSS_NCTF_16
BH52	BH52	VSS_NCTF_17
D2	D2	VSS_NCTF_28
A4	A4	VSS_NCTF#A4
A49	A49	VSS_NCTF#A49
A5	A5	VSS_NCTF#A5
A50	A50	VSS_NCTF#A50
A52	A52	VSS_NCTF#A52
A53	A53	VSS_NCTF#A53
B2	B2	VSS_NCTF#B2
B53	B53	VSS_NCTF#B53
BE1	BE1	VSS_NCTF#BE1
BE53	BE53	VSS_NCTF#BE53
BF1	BF1	VSS_NCTF#BF1
BF53	BF53	VSS_NCTF#BF53
BH1	BH1	VSS_NCTF#BH1
BH53	BH53	VSS_NCTF#BH53
BJ1	BJ1	VSS_NCTF#BJ1
BJ2	BJ2	VSS_NCTF#BJ2
BJ4	BJ4	VSS_NCTF#BJ4
BJ49	BJ49	VSS_NCTF#BJ49
BJ5	BJ5	VSS_NCTF#BJ5
BJ50	BJ50	VSS_NCTF#BJ50
BJ52	BJ52	VSS_NCTF#BJ52
BJ53	BJ53	VSS_NCTF#BJ53
D1	D1	VSS_NCTF#D1
D53	D53	VSS_NCTF#D53
E1	E1	VSS_NCTF#E1
E53	E53	VSS_NCTF#E53

Signal	Pin	Function
TP48	TP48	1 PCH TP95
TP49	TP49	1 PCH TP96
TP50	TP50	1 PCH TP97
TP51	TP51	1 PCH TP98

Signal	Pin	Function
CLKOUT_PCIE6N	AH45	
CLKOUT_PCIE6P	AH46	
TACH1/GPIO1		
TACH2/GPIO6		
TACH3/GPIO7		
GPIO8		
LAN_PHY_PWR_CTRL/GPIO12		
GPIO15		
SATA4GP/GPIO16		
TACH0/GPIO17		
SCLOCK/GPIO22		
GPIO24		
GPIO27		
GPIO28		
STP_PCI#/GPIO34		
SATACLKREQ#/GPIO35		
SATA2GP/GPIO36		
SATA3GP/GPIO37		
SLOAD/GPIO38		
SDATAOUT0/GPIO39		
PCIECLKRQ6#/GPIO45		
PCIECLKRQ7#/GPIO46		
SDATAOUT1/GPIO48		
SATA5GP/GPIO49		
GPIO57		
VSS_NCTF_8		
VSS_NCTF_9		
VSS_NCTF_16		
VSS_NCTF_17		
VSS_NCTF_28		
VSS_NCTF#A4		
VSS_NCTF#A49		
VSS_NCTF#A5		
VSS_NCTF#A50		
VSS_NCTF#A52		
VSS_NCTF#A53		
VSS_NCTF#B2		
VSS_NCTF#B53		
VSS_NCTF#BE1		
VSS_NCTF#BE53		
VSS_NCTF#BF1		
VSS_NCTF#BF53		
VSS_NCTF#BH1		
VSS_NCTF#BH53		
VSS_NCTF#BJ1		
VSS_NCTF#BJ2		
VSS_NCTF#BJ4		
VSS_NCTF#BJ49		
VSS_NCTF#BJ5		
VSS_NCTF#BJ50		
VSS_NCTF#BJ52		
VSS_NCTF#BJ53		
VSS_NCTF#D1		
VSS_NCTF#D53		
VSS_NCTF#E1		
VSS_NCTF#E53		



20100922

Hynix 1G 800M N11PGV SKU

R269	UMA_512M	Do Not Stuff	R271	2G	Do Not Stuff
R270	1G_2G	10KR2J-3-GP	R272	UMA_512M_1G	10KR2J-3-GP

UMA/512M : HIGH
1G : LOW

2G : HIGH
UMA/1G/512M : LOW

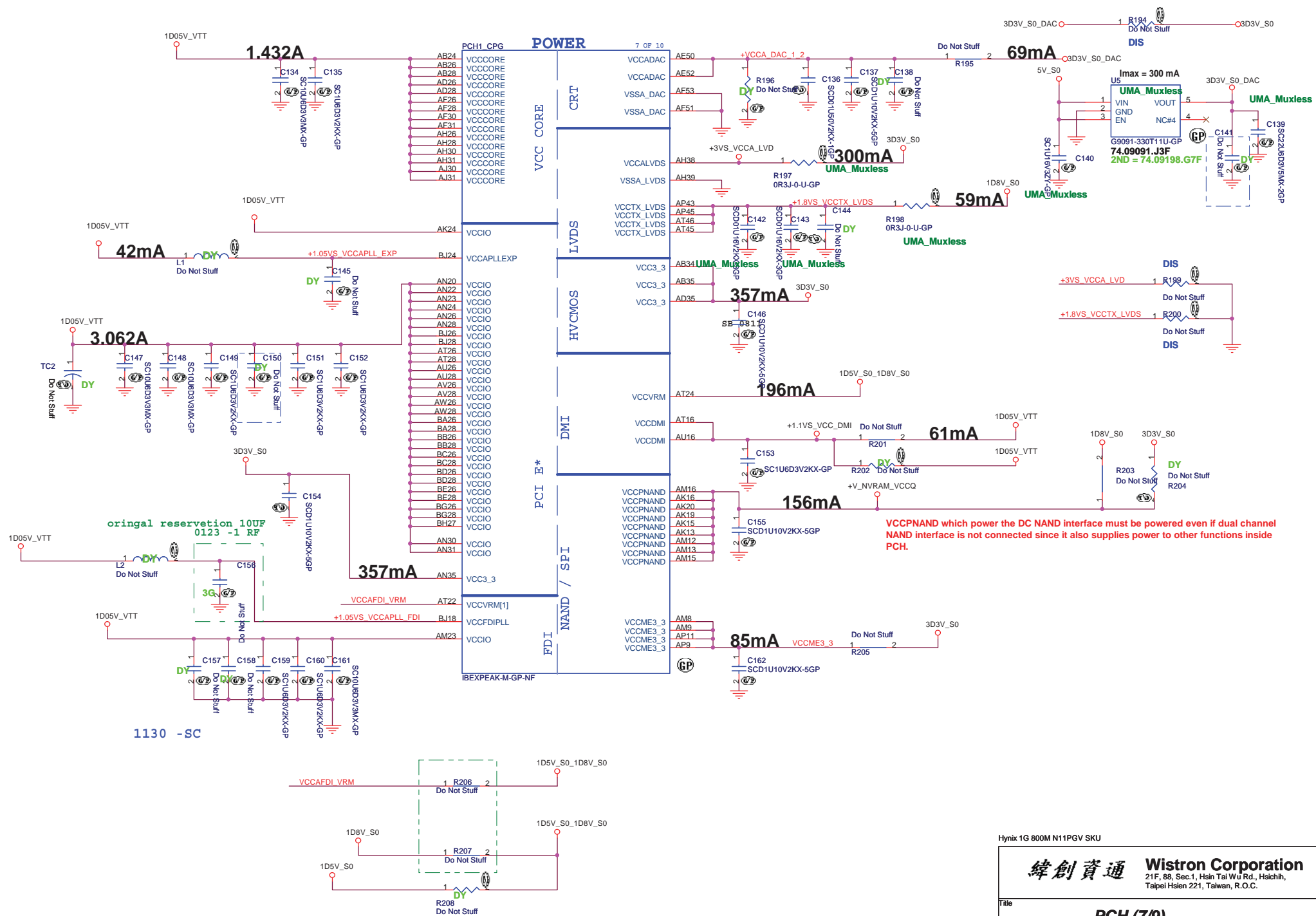
VRAM Frequency
VRAM 800Mhz : PULL HIGH
VRAM 900Mhz : PULL LOW

20100921

20101115

20100922

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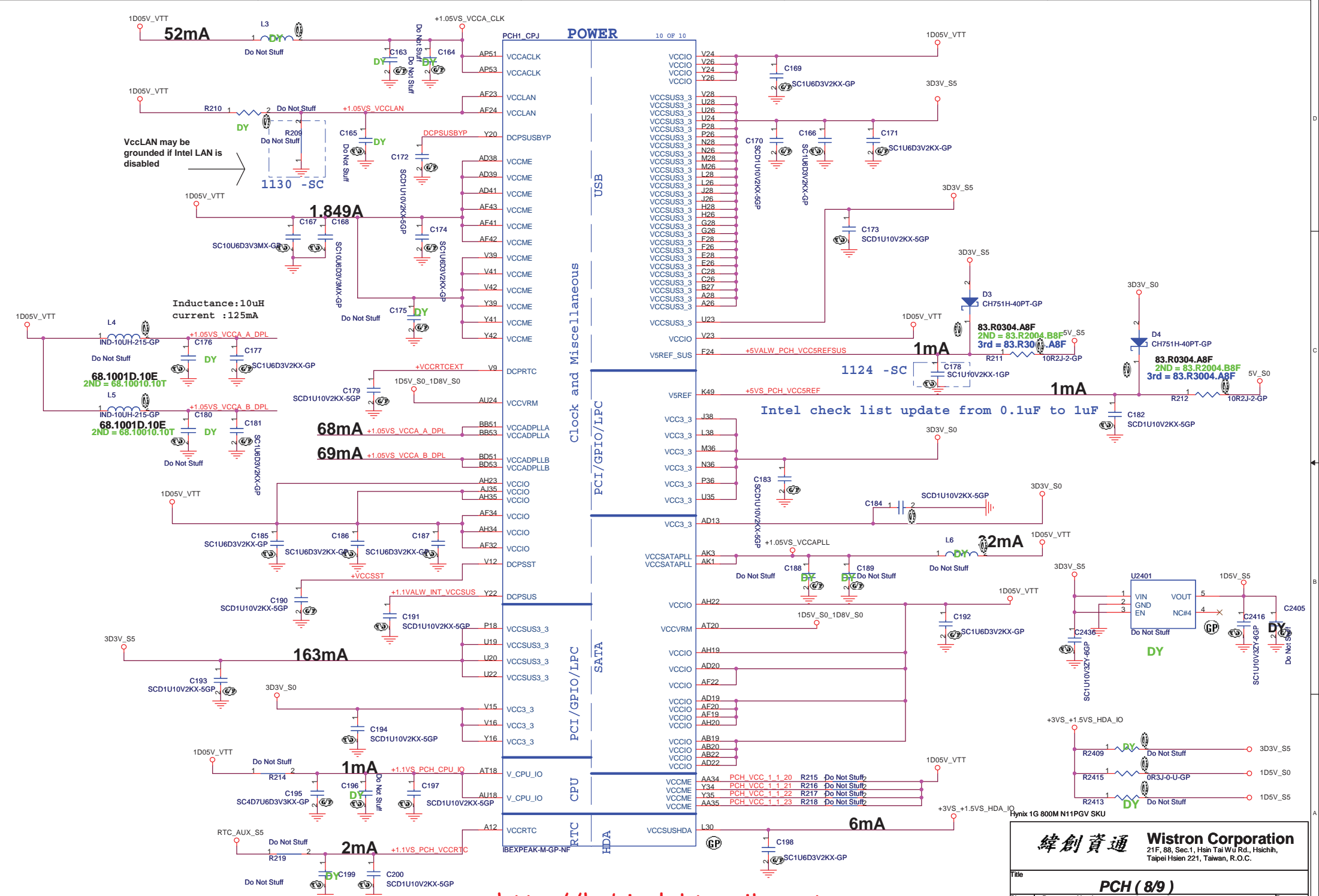


1130 -SC

<http://hobi-elektronika.net>

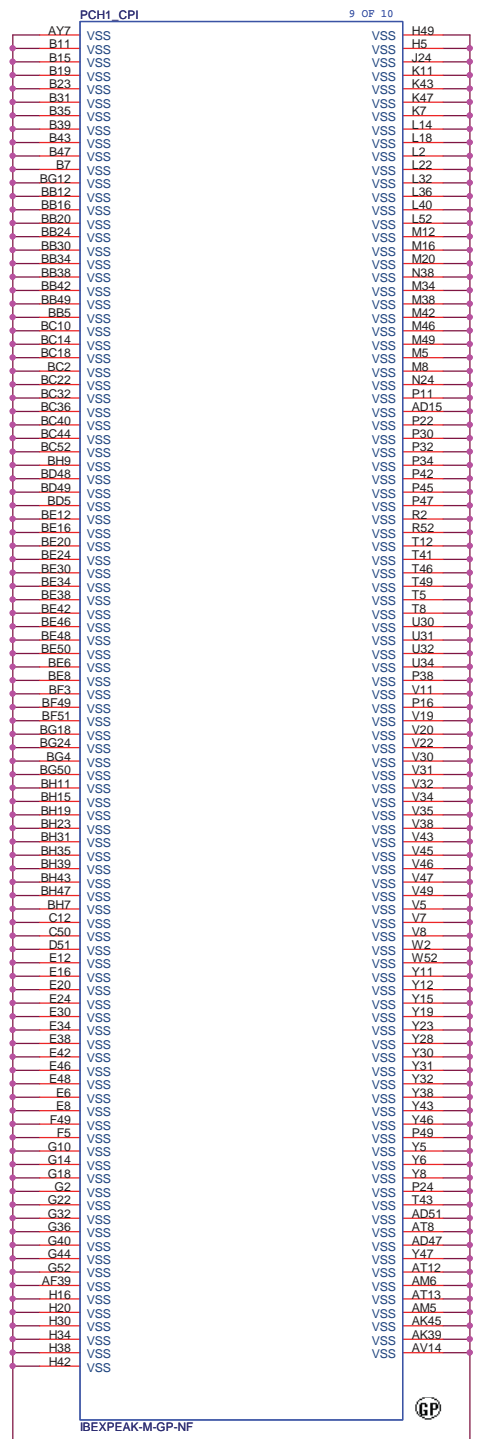
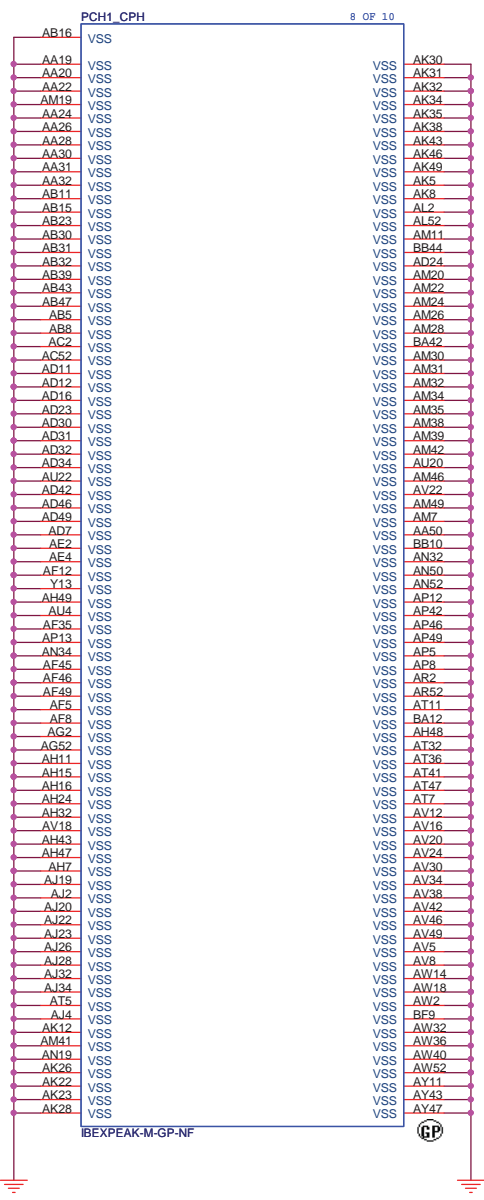
Hynix 1G 800M N11PGV SKU

緯創資通		Wistron Corporation	
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsin 221, Taiwan, R.O.C.			
Title		PCH (7/9)	
Size A3	Document Number	JE43-CP	
Date: Wednesday, November 24, 2010	Sheet 17	of	69



<http://hobi-elektronika.net>

 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title PCH (8/9)	
Size A3	Document Number JE43-CP
Date: Wednesday, November 24, 2010	Sheet 18 of 69
Rev -1	

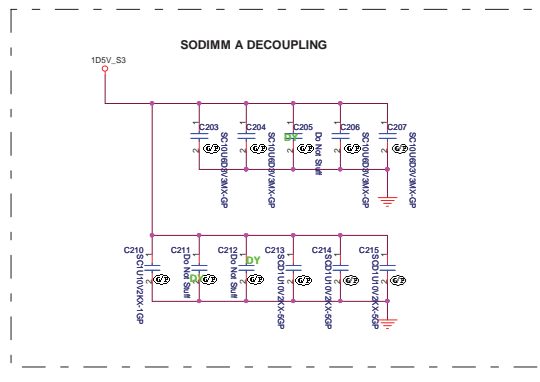
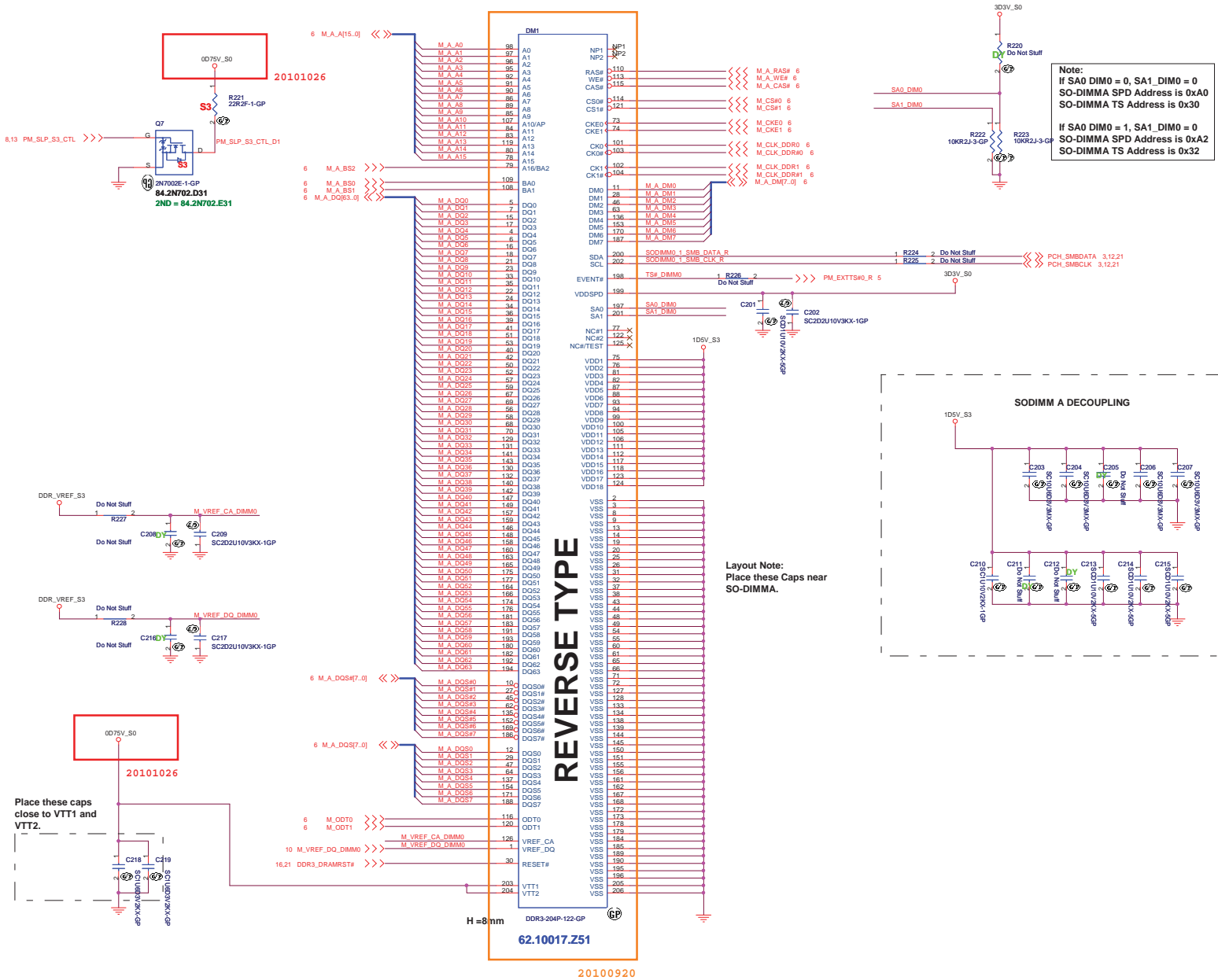


<http://hobi-elektronika.net>

Hynix 1G 800M N11PGV SKU

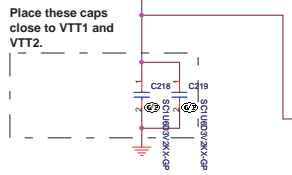
緯創資通 **Wistron Corporation**
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
 Taipei Hsien 221, Taiwan, R.O.C.

Title		
PCH (9/9)		
Size	Document Number	Rev
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Date:	Wednesday, November 24, 2010	Sheet 19 of 69



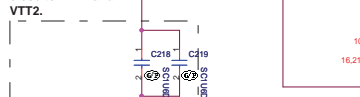
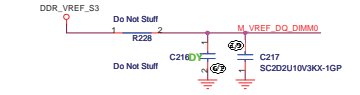
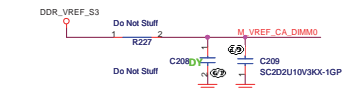
Layout Note:
Place these Caps near SO-DIMMA.

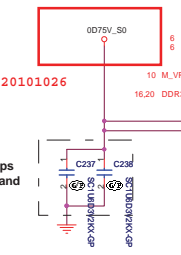
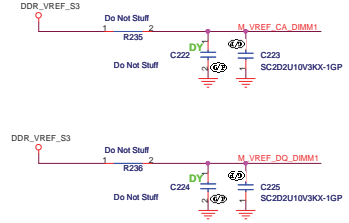
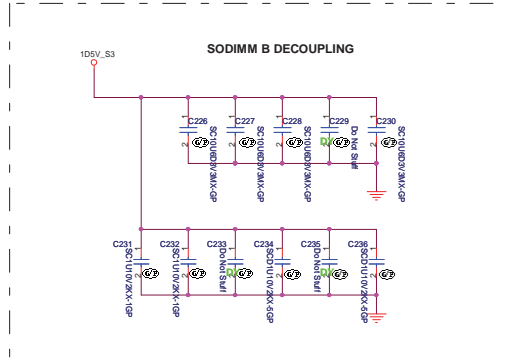
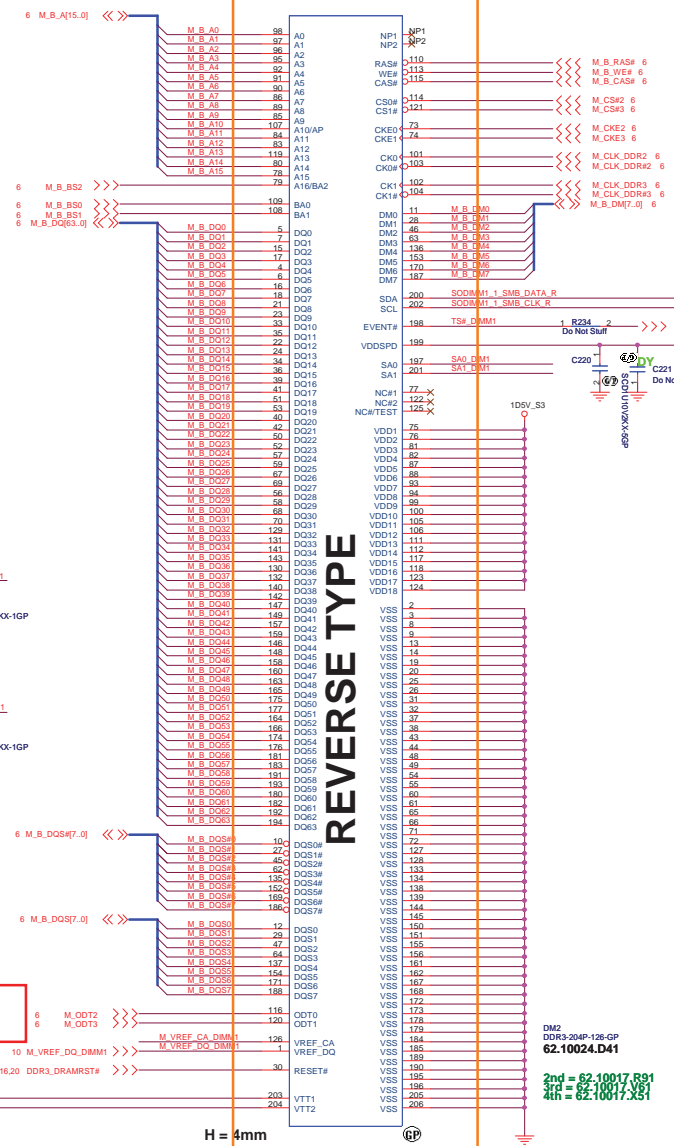
REVERSE TYPE



Place these caps close to VTT1 and VTT2.

8.13 PM_SLP_S3_CTL >>>





Place these caps close to VTT1 and VTT2.

Note:
SO-DIMMB SPD Address is 0xA4
SO-DIMMB TS Address is 0x34

SO-DIMMB is placed farther from the Processor than SO-DIMMA

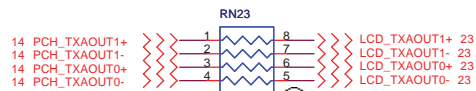
DM2
DDR3-204P-128 GB
62.10024.D41

2nd = 62-10017-R91
3rd = 62-10017-X91
4th = 62-10017-X91

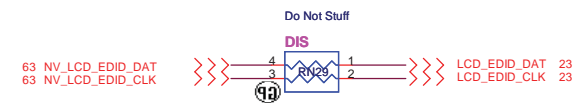
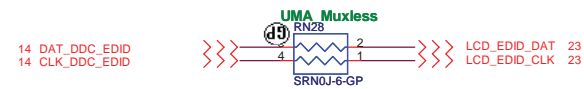
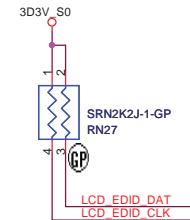
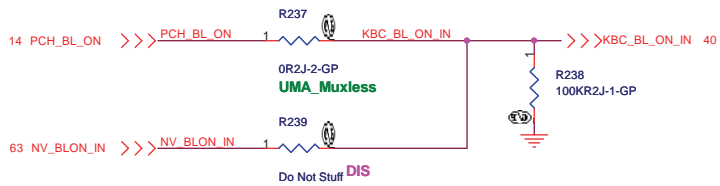
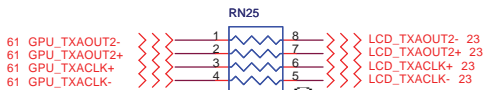
20100920

H = 4mm

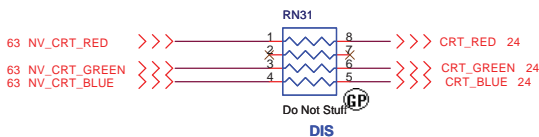
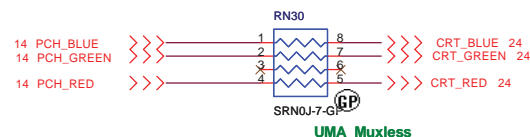
LCD



0807 SA CLK SWAP



CRT

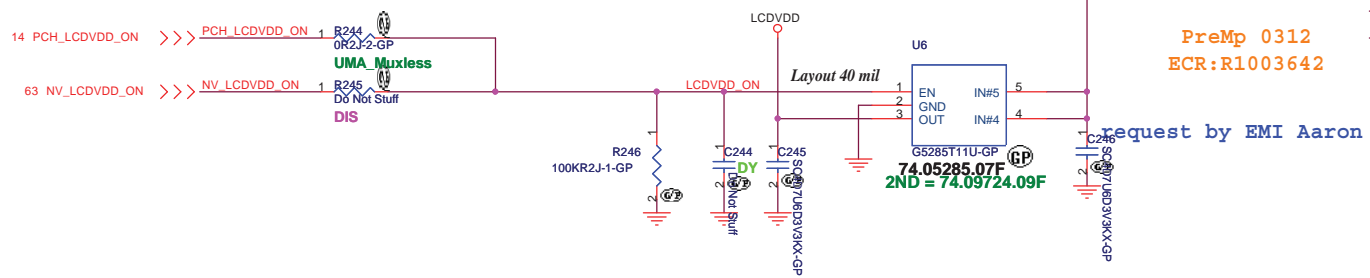
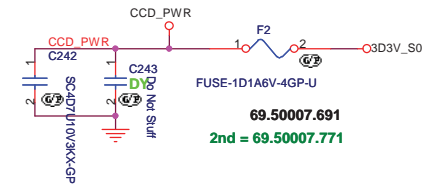
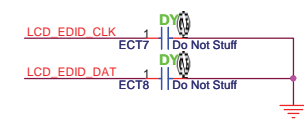
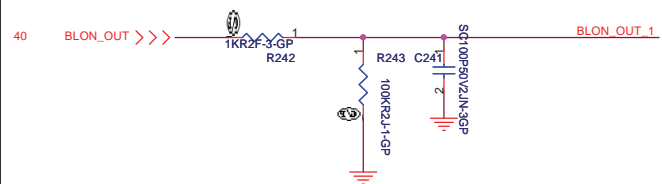
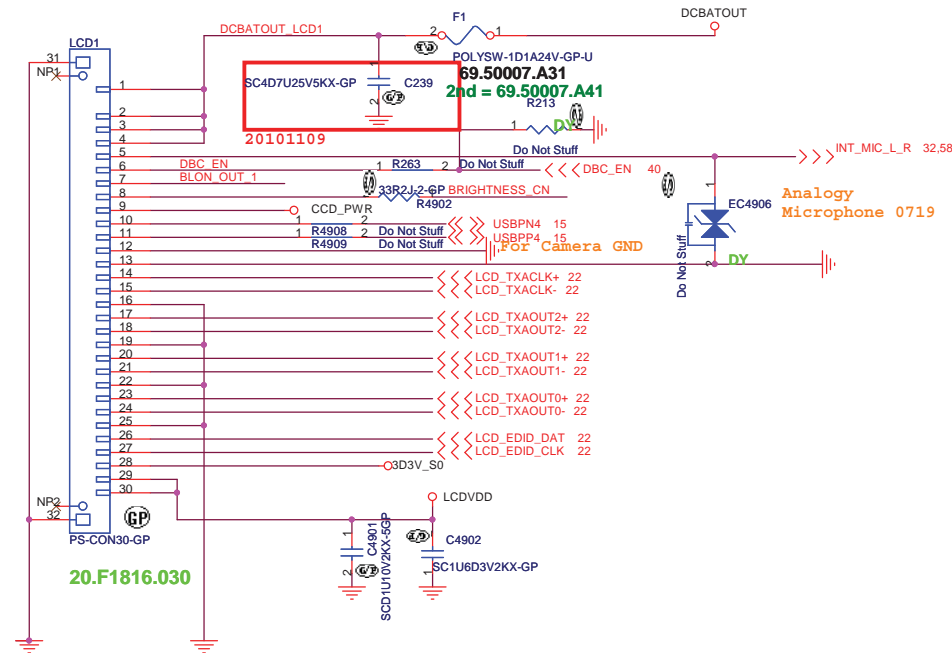


<http://hobi-elektronika.net>

Hynix 1G 800M N11PGV SKU

Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hstchih, Taipei Hsien 221, Taiwan, R.O.C.	
LCD CRT SWITCHABLE	
Title Size A3 Date: Wednesday, November 24, 2010	Document Number JE43-CP Sheet 22 of 69
Rev -1	Rev 69

LCD/INVERTER/CCD CONN LCD/CCD CONN



PreMp 0312
ECR:R1003642

request by EMI Aaron

<http://hobi-elektronika.net>

Hynix 1G 800M N11PGV SKU

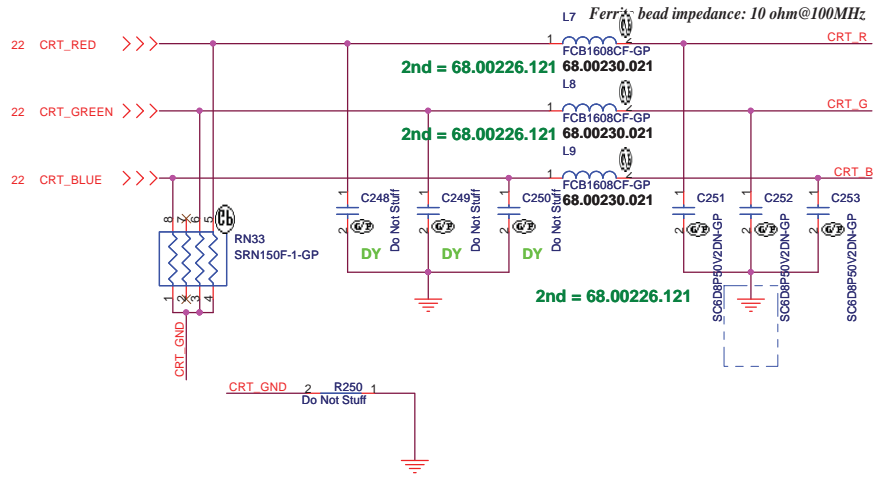
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **LCD CONN**

Size	Document Number	Rev
	JE43-CP	-1

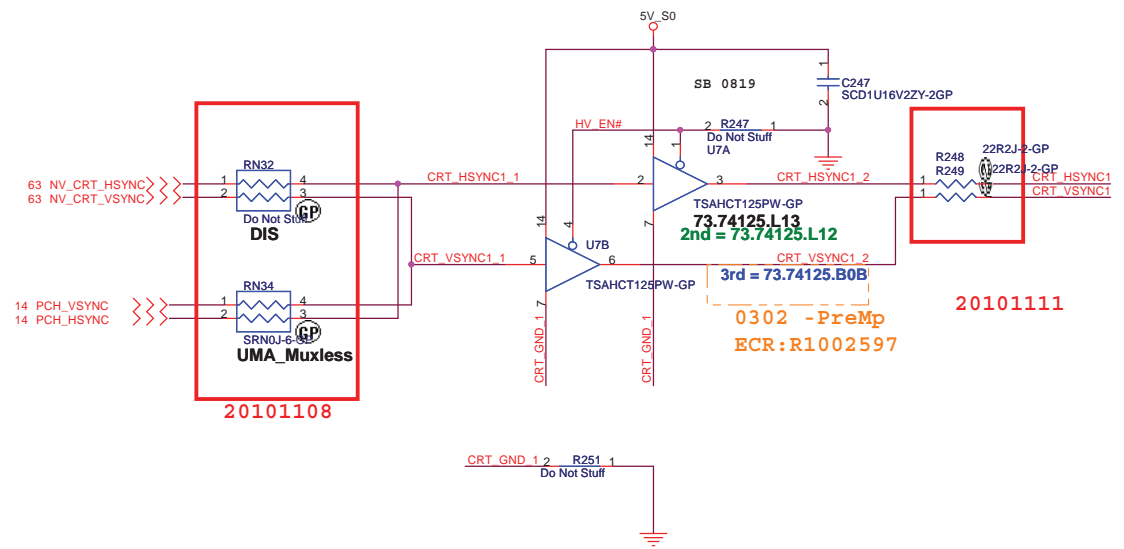
Date: Wednesday, November 24, 2010 Sheet 23 of 69

Layout Note:
Place these resistors close to the CRT-out connector

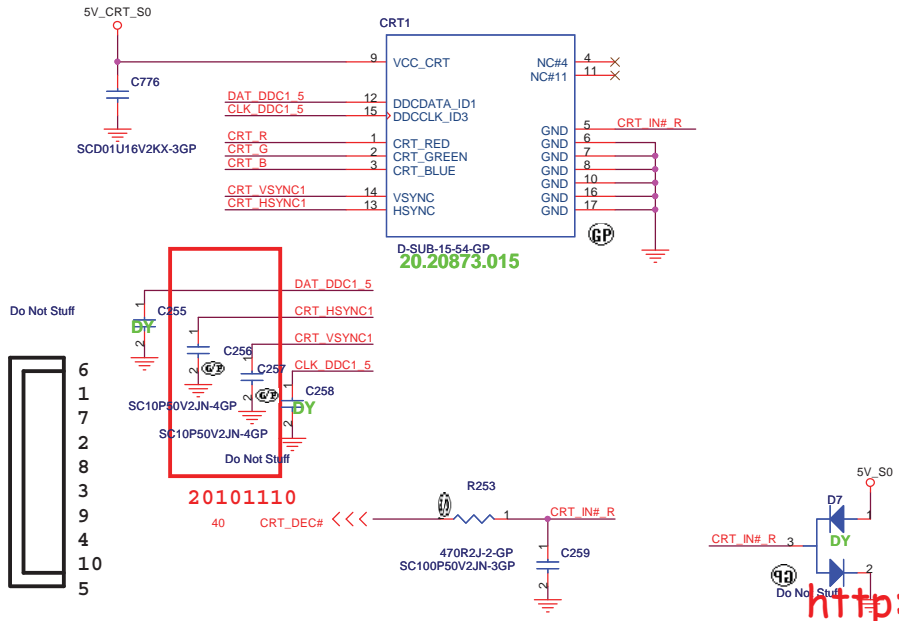


Layout Note:
* Must be a ground return path between this ground and the ground on the VGA connector.
Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN. RGB will hit 75 Ohm first, pi-filter, then CRT CONN.

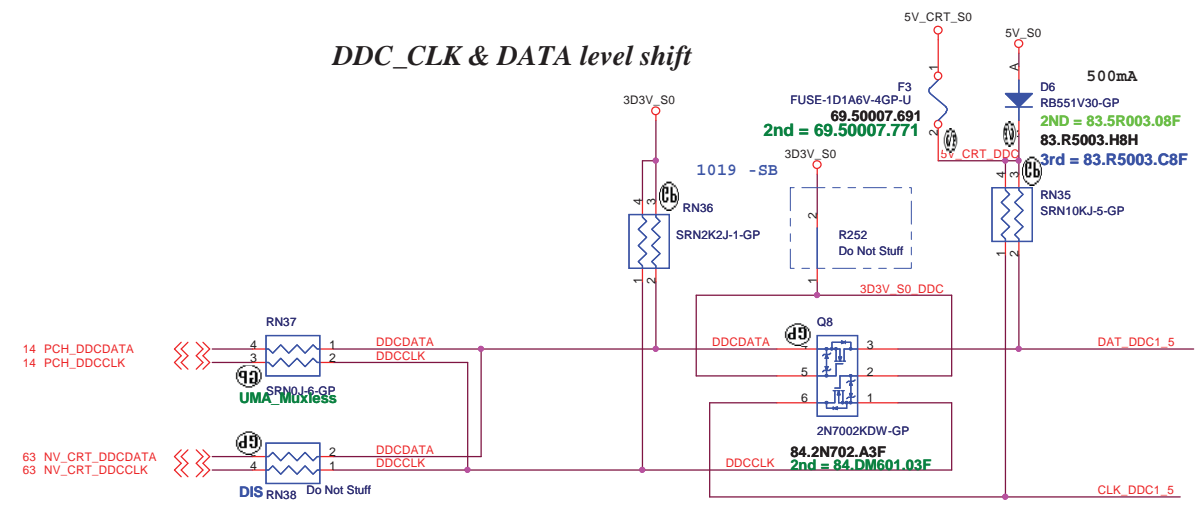
Hsync & Vsync level shift



CRT I/F & CONNECTOR



DDC_CLK & DATA level shift



Hynix 1G 800M N11PGV SKU

緯創資通 Wistron Corporation
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Title: **CRT CONN**

Size: Document Number: **JE43-CP** Rev: **-1**

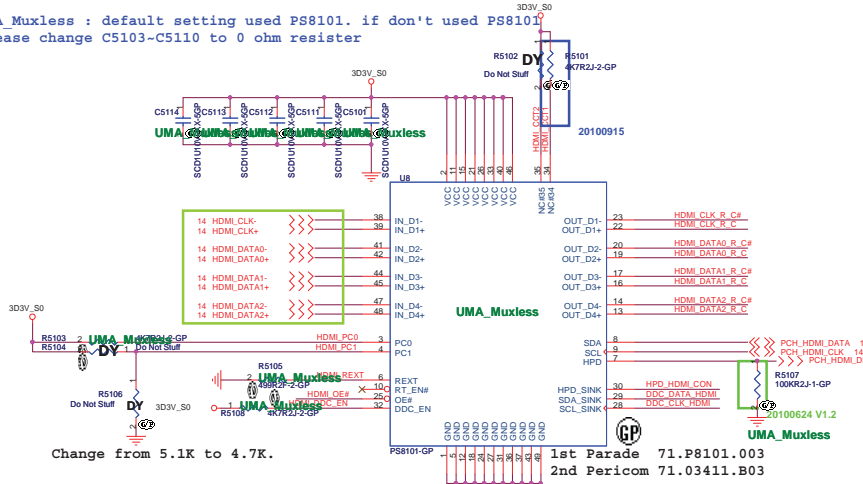
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HDMI Level Shifter & CONNECTOR

HDMI CONN

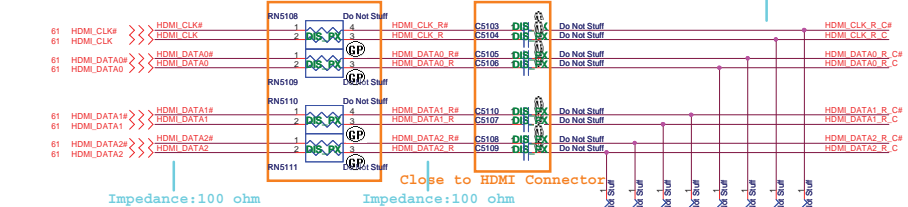
UMA Muxless : default setting used PS8101. if don't used PS8101
Please change C5103-C5110 to 0 ohm resistor



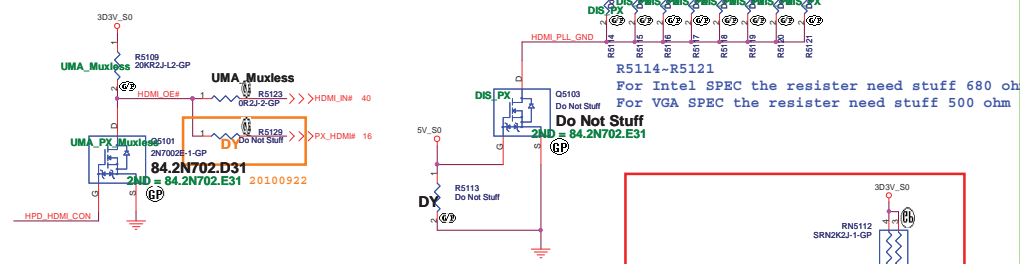
Change from 5.1K to 4.7K.

HDMI DISCRETE/ UMA Co-lay
Close to Level Shift

Impedance:100 ohm



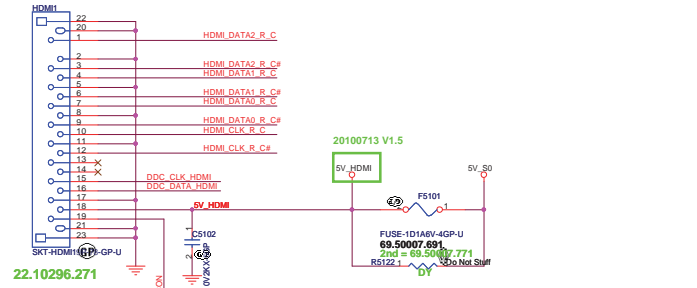
Close to HDMI Connector
Impedance:100 ohm



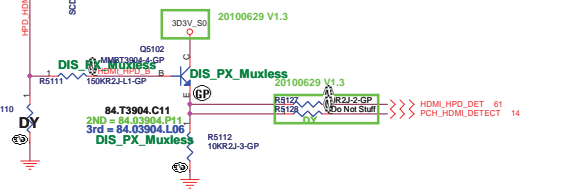
R5114-R5121
For Intel SPEC the resistor need stuff 680 ohm
For VGA SPEC the resistor need stuff 500 ohm



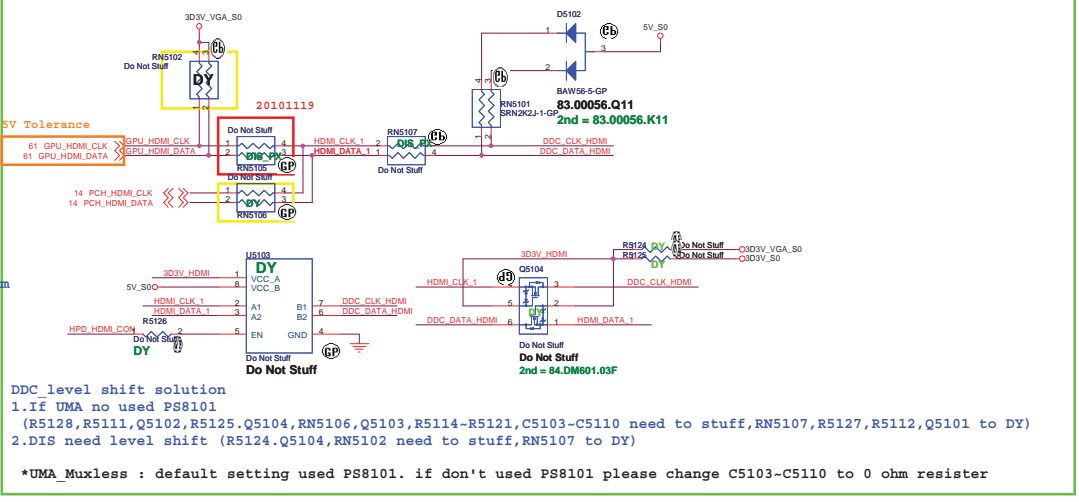
20101025



22.10296.271



20100629 V1.3

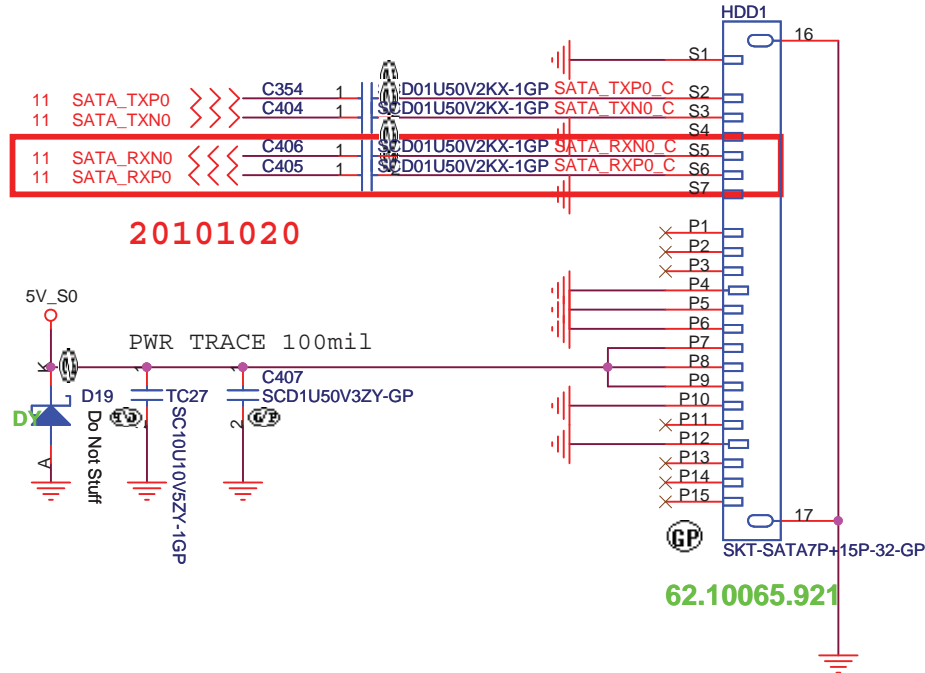


DDC level shift solution

1. If UMA no used PS8101 (R5128, R5111, Q5102, R5125, Q5106, Q5114-R5121, C5103-C5110 need to stuff, RNS107, R5127, R5112, Q5101 to DY)
2. DIS need level shift (R5124, Q5104, RNS102 need to stuff, RNS107 to DY)


*UMA Muxless : default setting used PS8101. if don't used PS8101 please change C5103-C5110 to 0 ohm resistor

SATA Connector

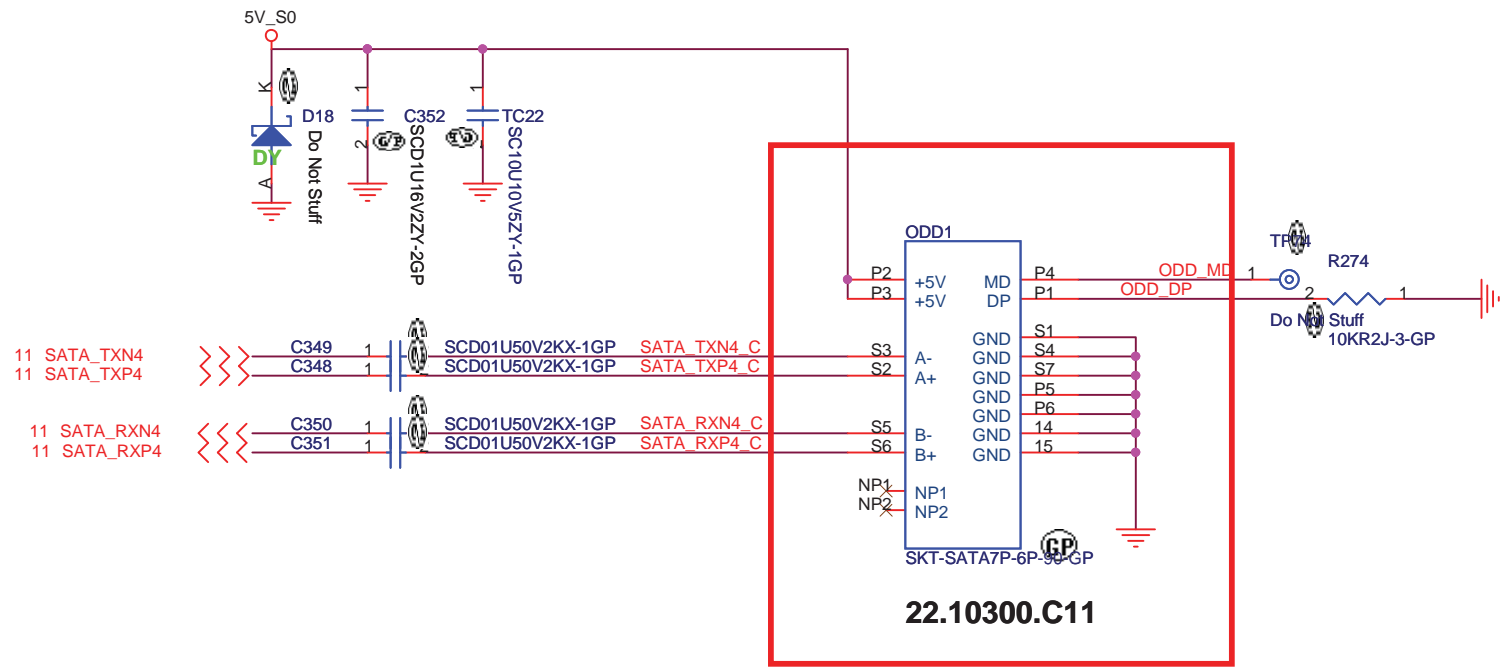


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Hynix 1G 800M N11PGV SKU

 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title HDD CONN	
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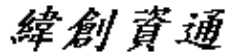
ODD Connector



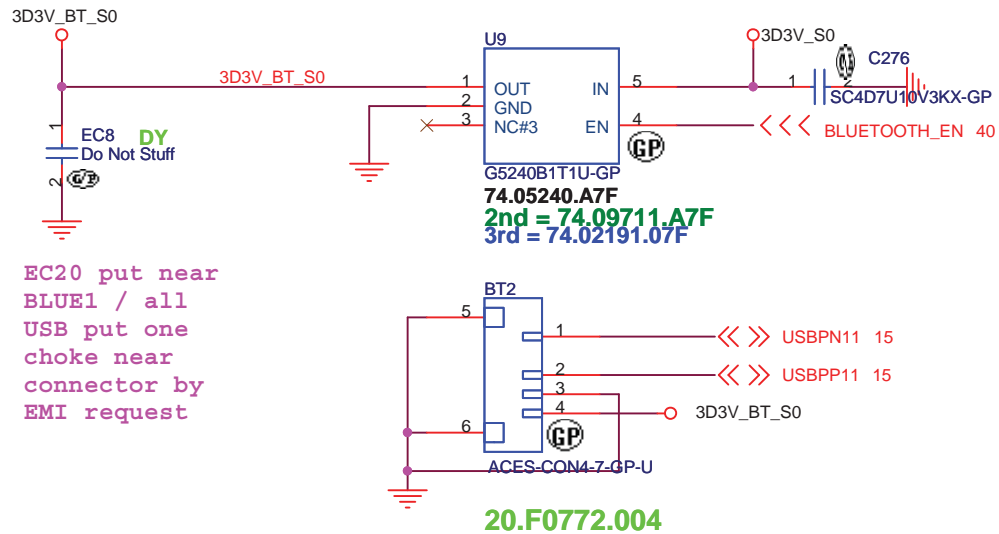
20101108

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Hynix 1G 800M N11PGV SKU

 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title ODD	
Size	Document Number
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27	69

BLUETOOTH MODULE



EC20 put near
BLUE1 / all
USB put one
choke near
connector by
EMI request

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Hynix 1G 800M N11PGV SKU

緯創資通

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

BLUETOOTH CONN

Size

Document Number

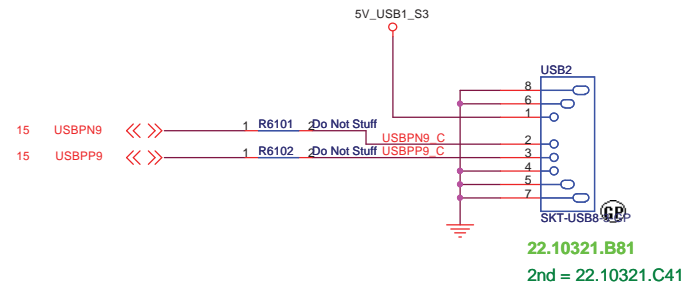
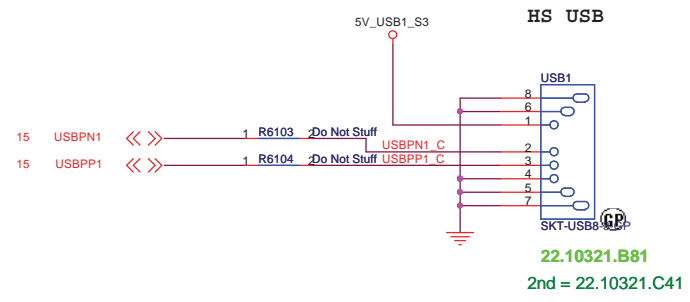
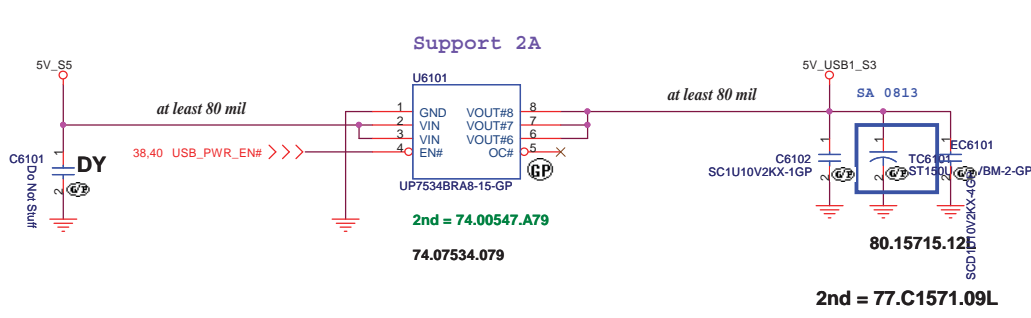
JE43-CP

Rev

-1

Date: Wednesday, November 24, 2010

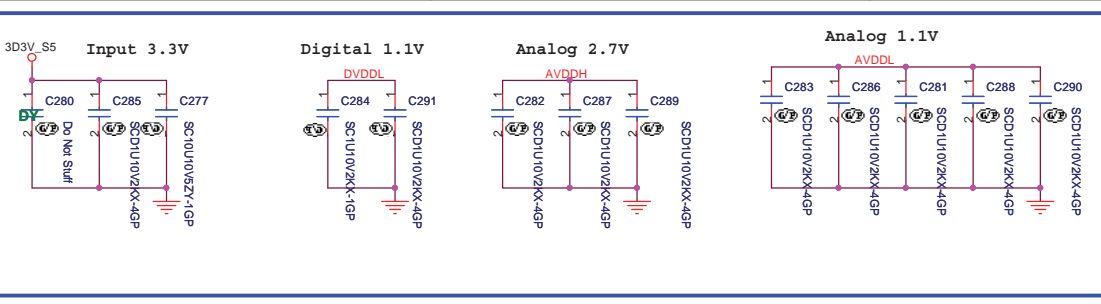
Sheet 28 of 69



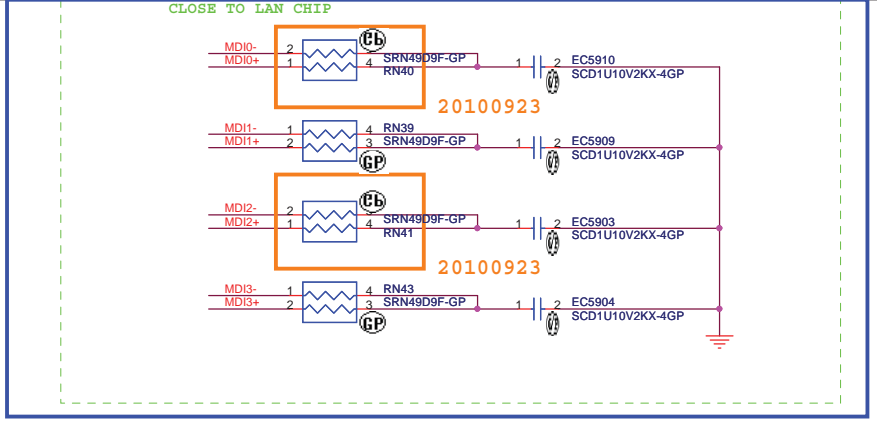
<http://hobi-elektronika.net>

Hynix 1G 800M N11PGV SKU

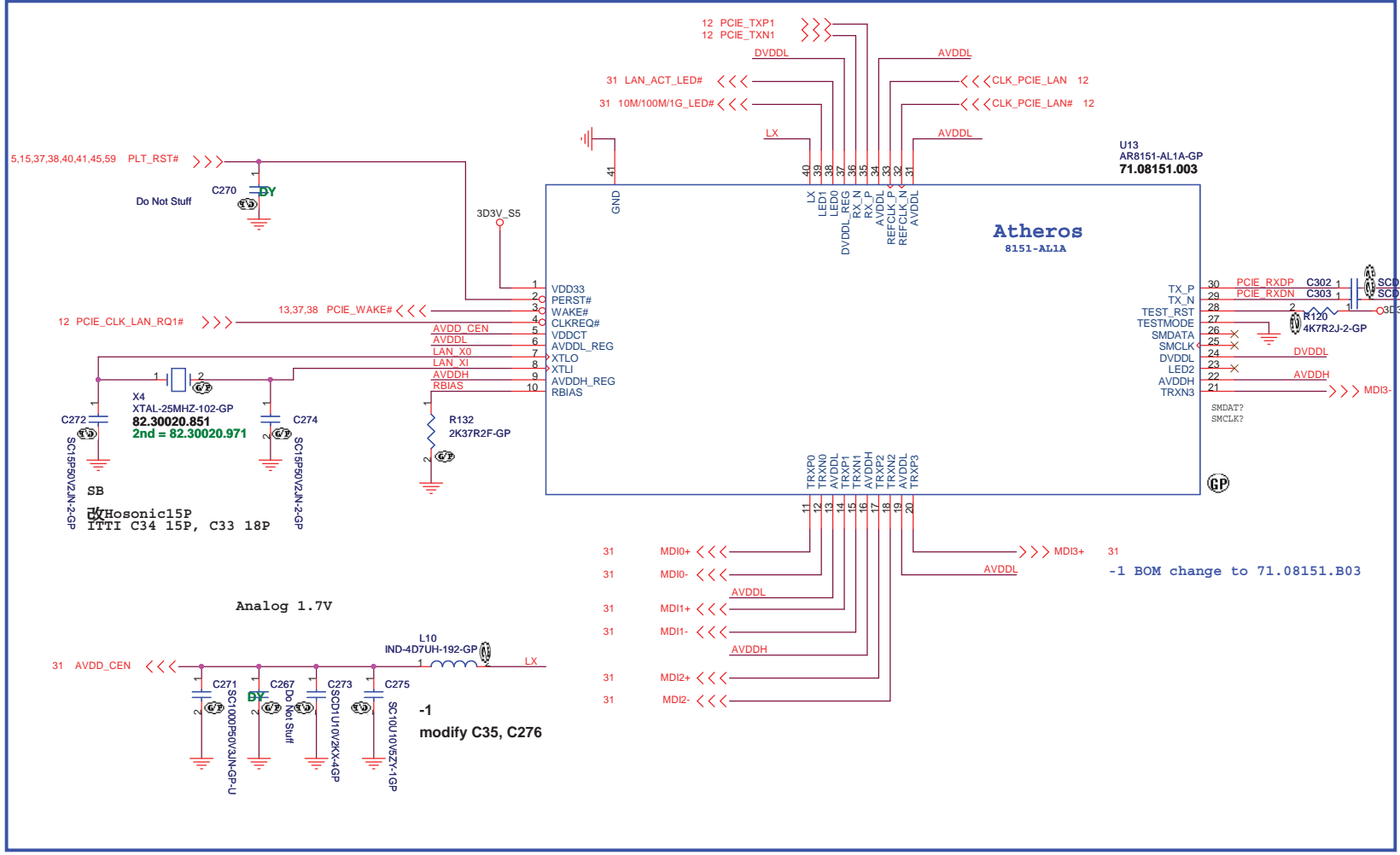
緯創資通		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
USB 2.0 CONN			
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Hynix 1G 800M N11PGV SKU

緯創資通 Wistron Corporation
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

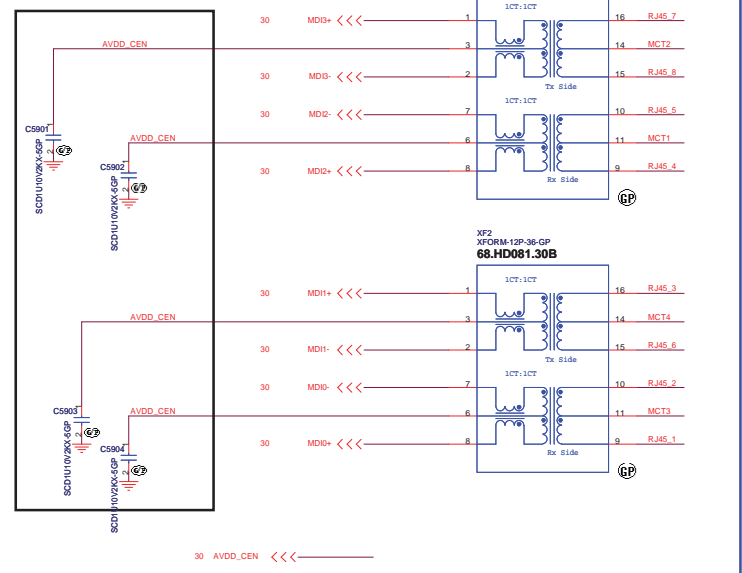
Title: **AR8151 chip**

Size A3 Document Number: **JE43-CP** Rev: **-1**

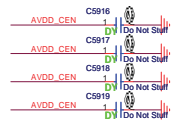
Date: Wednesday, November 24, 2010 Sheet 30 of 69

GIGA Lan Transformer

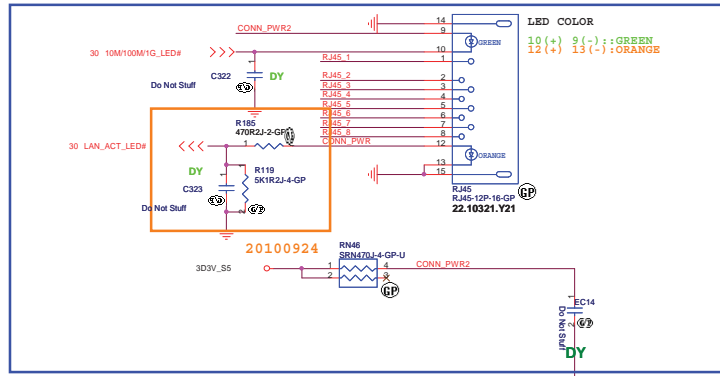
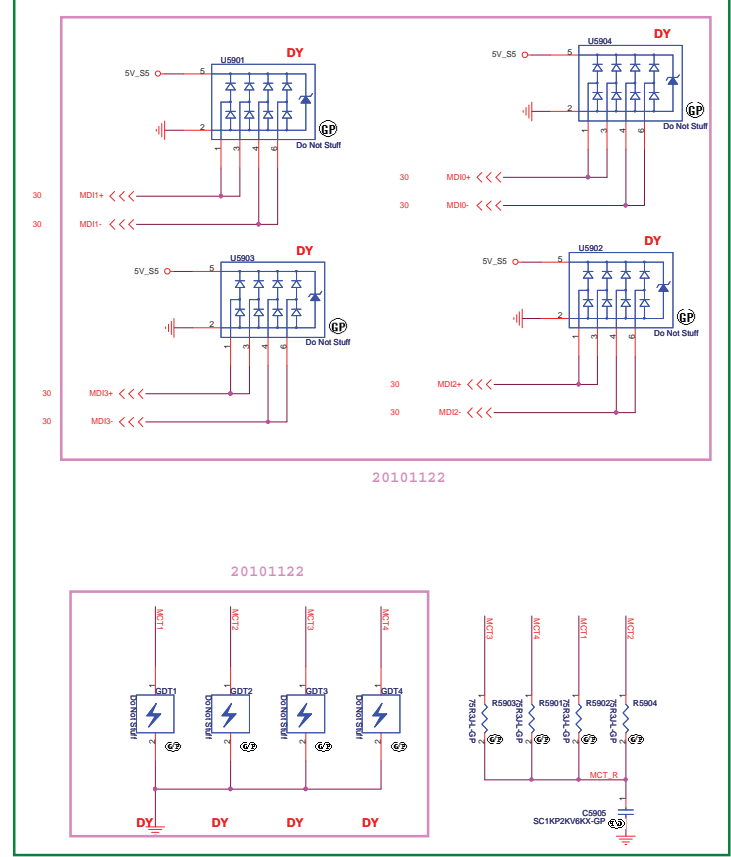
SSID = LOM



20100915

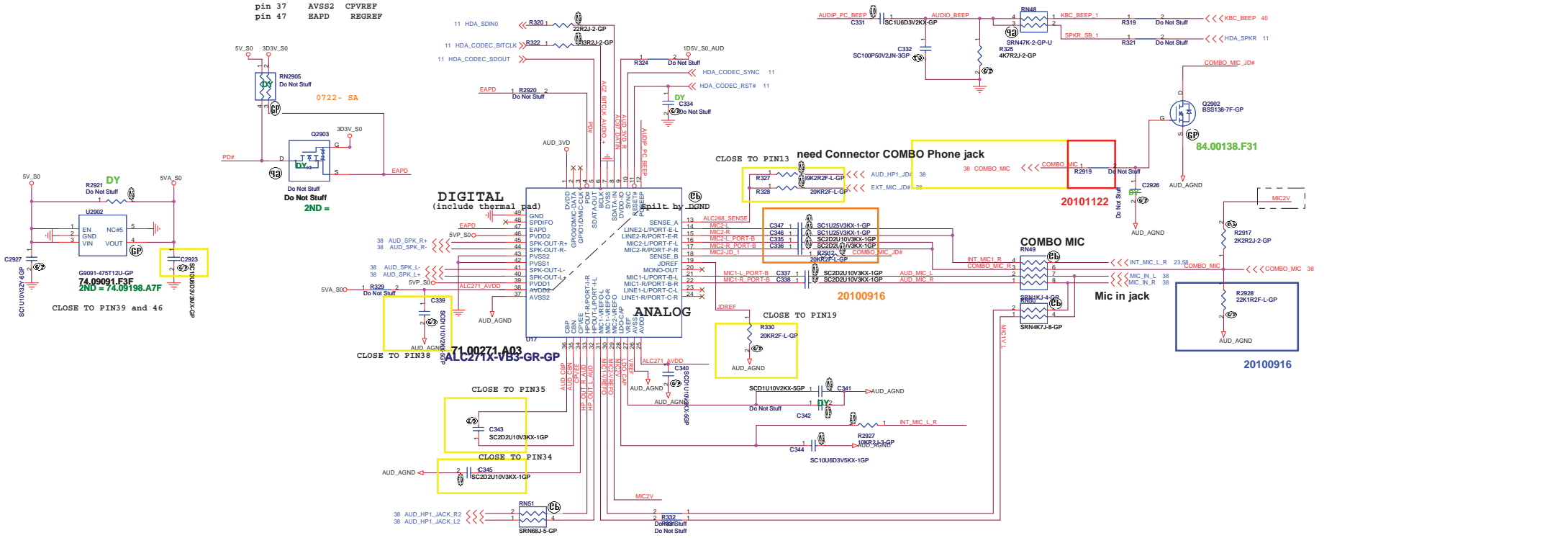
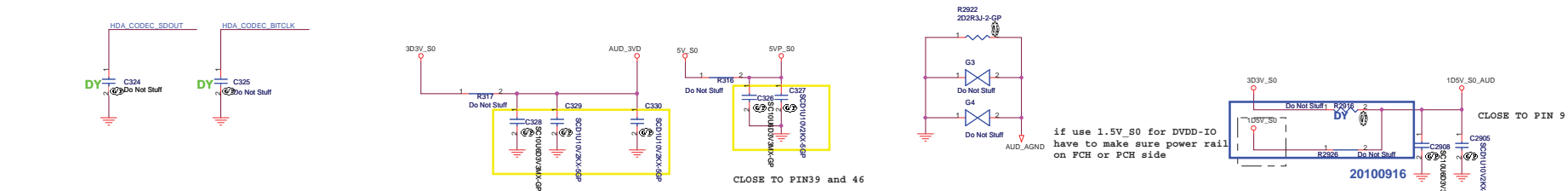


SB modify For EMI



20100915

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Hynix 1G 800M N11PGV SKU

緯創資通		Wistron Corporation	
		21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
File	AUDIO CODEC(ALC271)		
Size	Document Number		Rev
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Hynix 1G 800M N11PGV SKU

緯創資通		Wistron Corporation	
		<small>21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</small>	
Title			

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D

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A

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Hynix 1G 800M N11PGV SKU

緯創資通		Wistron Corporation	
		<small>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</small>	
Title			

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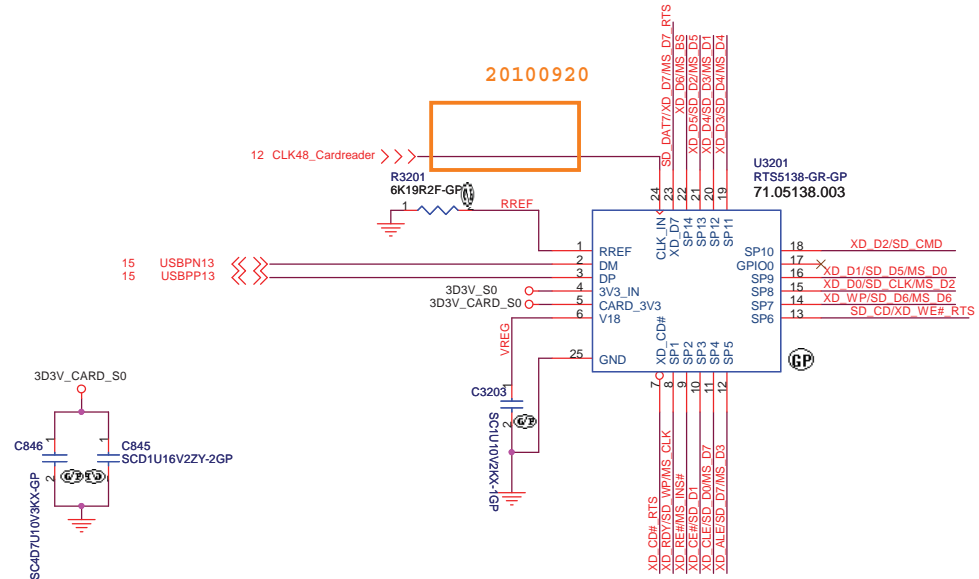
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<http://hobi-elektronika.net>

Hynix 1G 800M N11PGV SKU

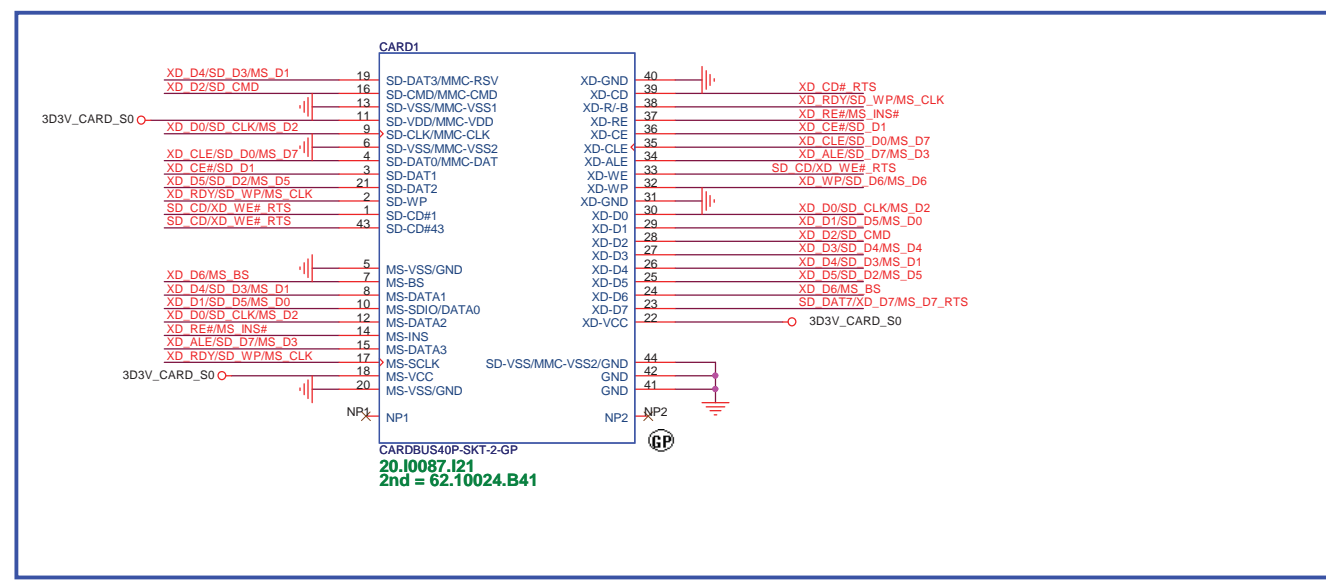
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<small>21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</small>		<small>21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</small>	
Title			
RTS5138 (CARD READER)			
Size	Document Number	Rev	Rev
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Date: Wednesday, November 24, 2010		Sheet 35	of 69

1

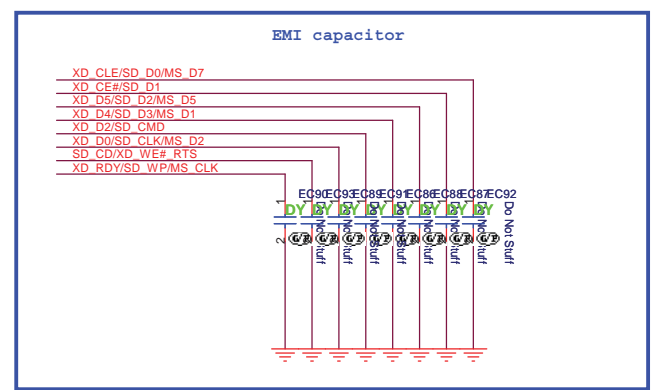


20100915

4 IN1 CARD-READER (SD/MS/MS PRO/XD)



20100915



20100915

<http://hobi-elektronika.net>

Hynix 1G 800M N11PGV SKU

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **Cardreader CONN**

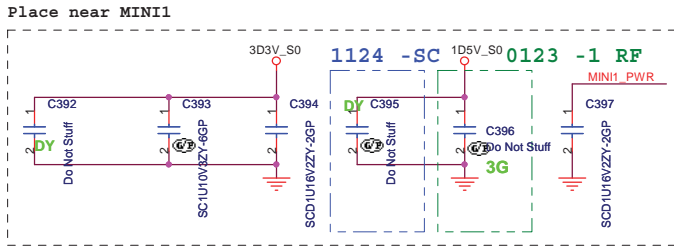
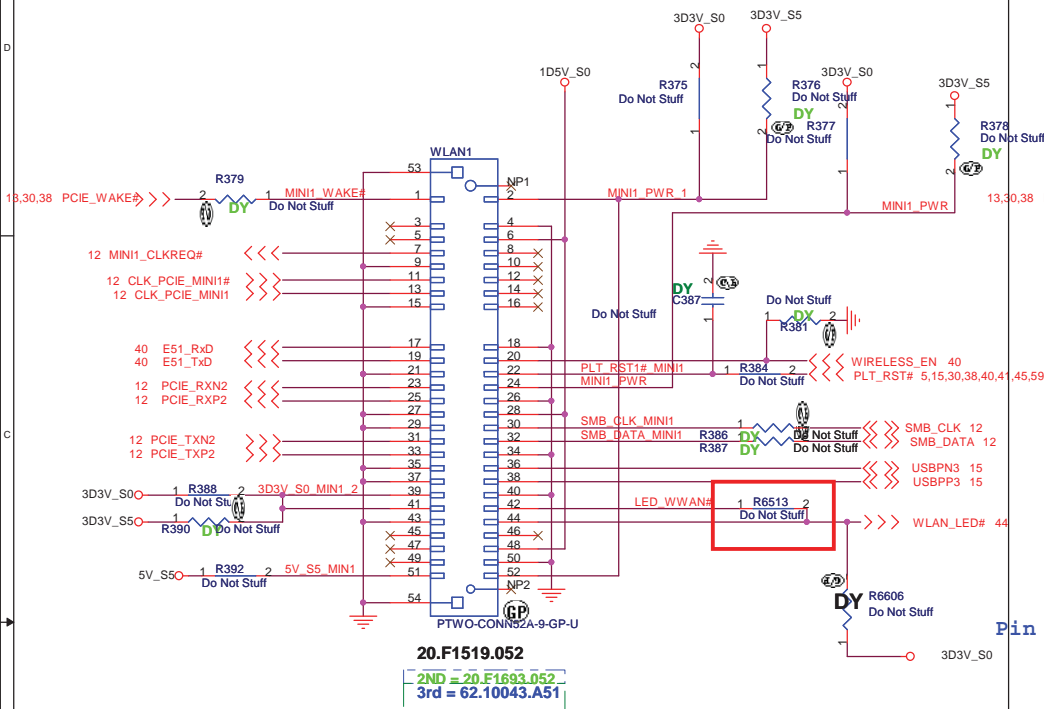
Size: JE43-CP -1

Document Number: _____

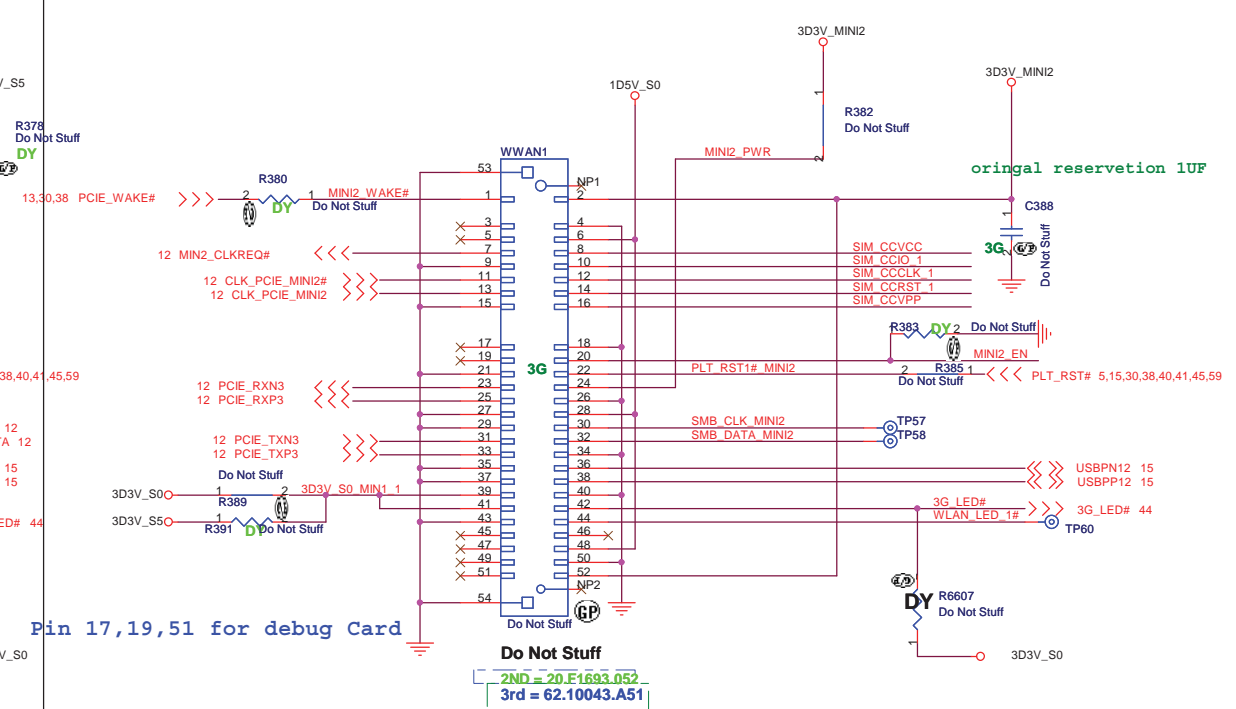
Date: Wednesday, November 24, 2010 Sheet: 36 of 69

Mini Card Connector(WLAN)

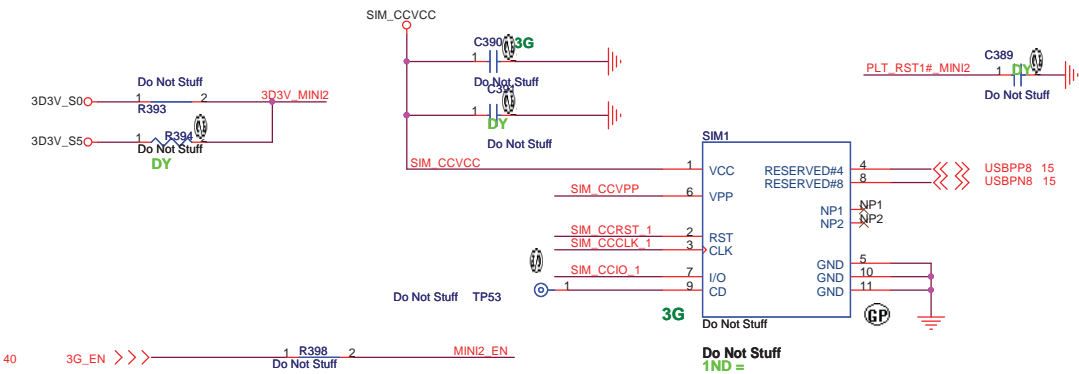
Support debug-card



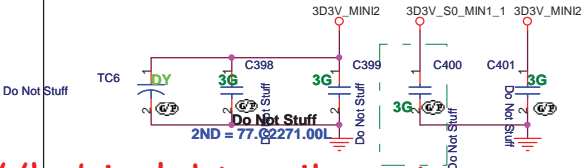
Mini Card Connector(Robson2 and 3G)



Pin 17,19,51 for debug Card



original reservation 10UF



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Hynix 1G 800M N11PGV SKU

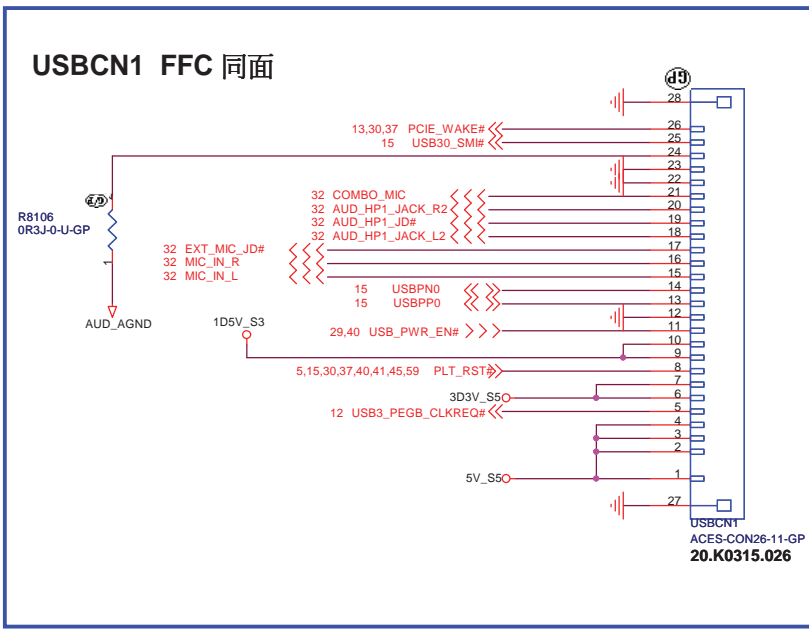
緯創資通 Wistron Corporation
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hstchih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **MINI CARD**

Size A3 Document Number: **JE43-CP** Rev: **-1**

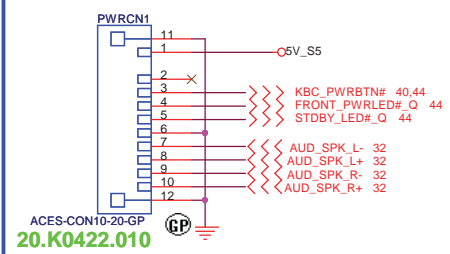
Date: Wednesday, November 24, 2010 Sheet 37 of 69

USBCN1 FFC 同面

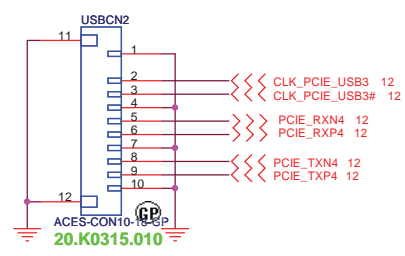


20100915

PWRCN1 FFC 異面



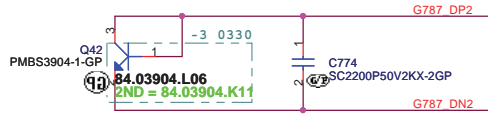
USBCN2 FFC 同面



<http://hobi-elektronika.net>

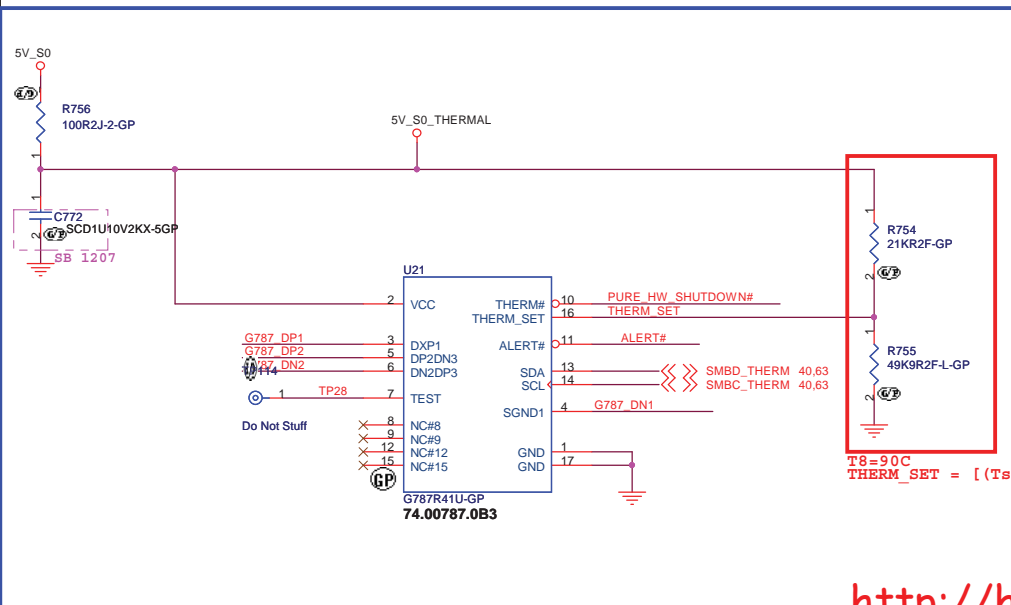
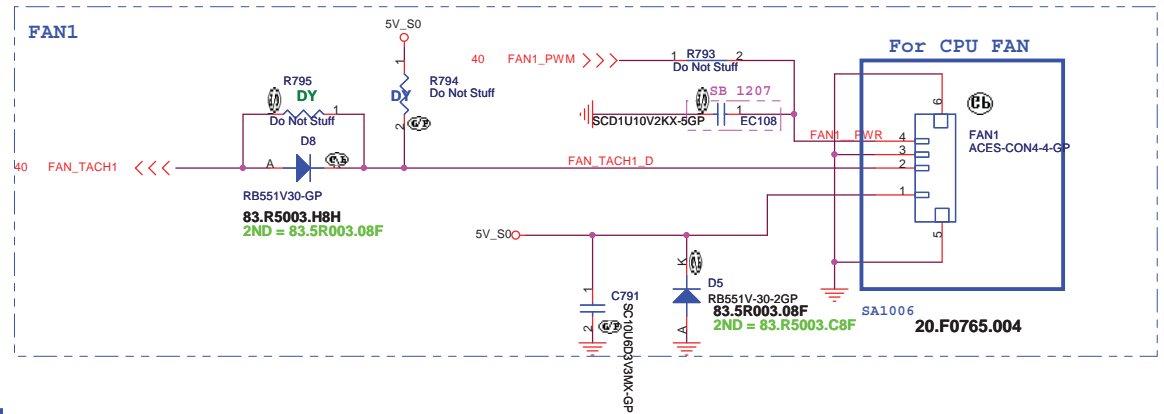
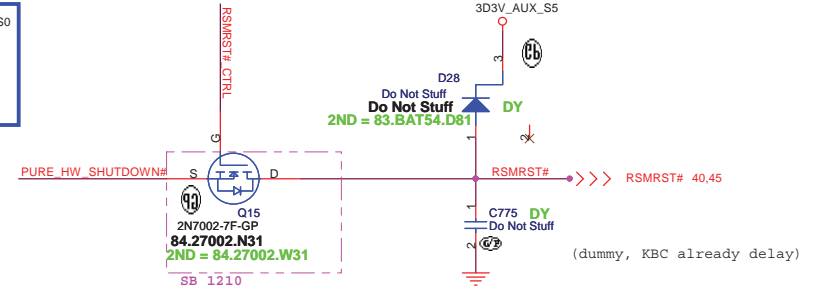
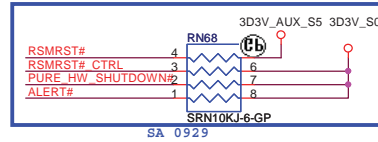
Hynix 1G 800M N11PGV SKU		
緯創資通		Wistron Corporation
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title: I/O Board		
Size: A3	Document Number: JE43-CP	Rev: -1
Date: Wednesday, November 24, 2010	Sheet: 38 of 69	

for T8 thermal diode



C82 & C561 CLOSE TO G787

for system thermal diode



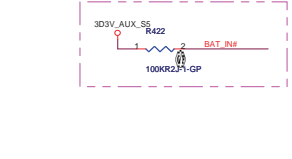
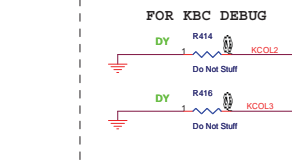
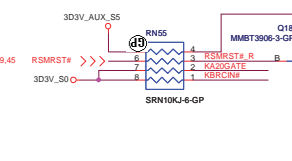
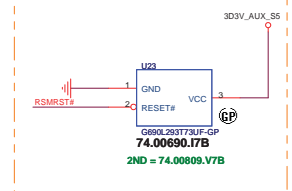
T8=90C
 $THERM_SET = [(T_{set}-72) \times 0.02+0.34] \times VCC$

<http://hobi-elektronika.net>

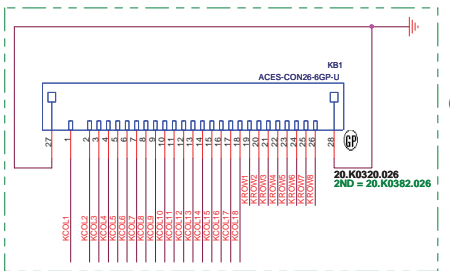
Hynix 1G 800M N11PGV SKU

緯創資通		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Thermal/Fan Connector			
Title	Document Number		Rev
	JE43-CP		-1
Date:	Wednesday, November 24, 2010	Sheet	39 of 69

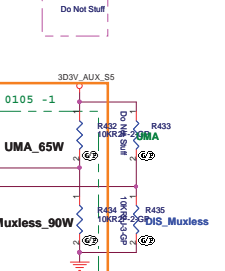
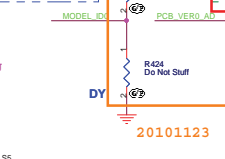
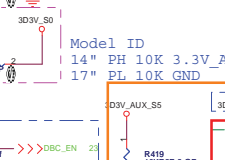
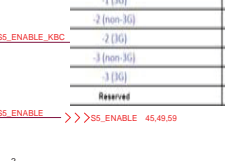
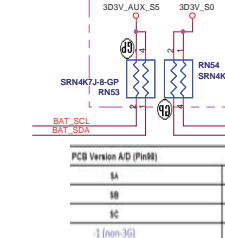
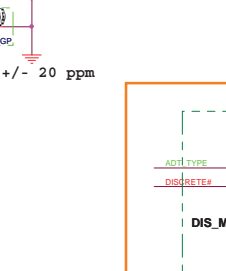
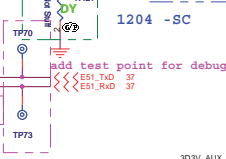
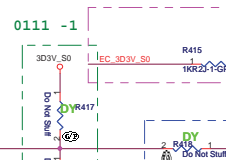
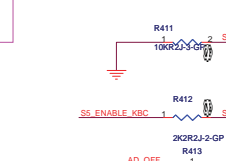
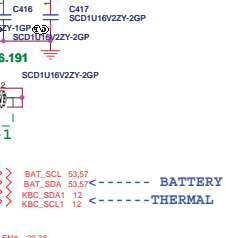
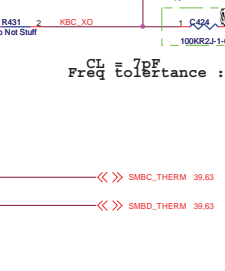
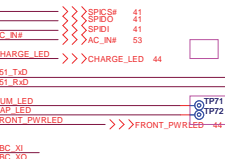
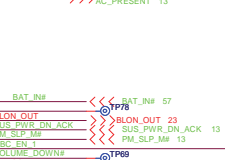
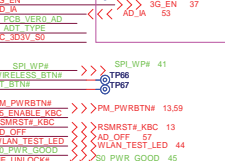
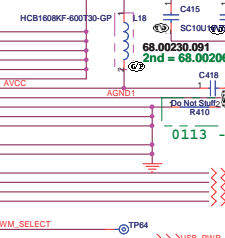
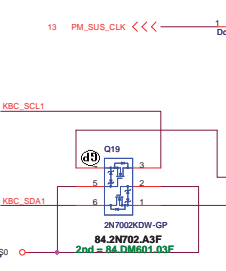
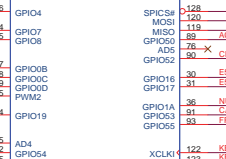
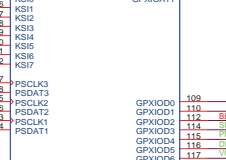
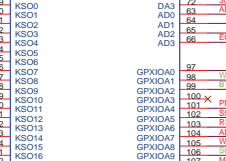
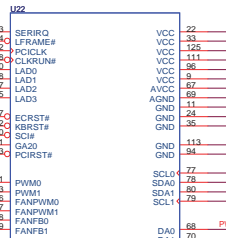
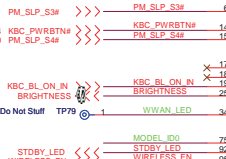
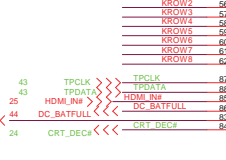
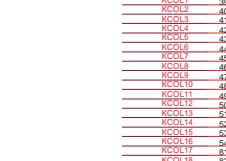
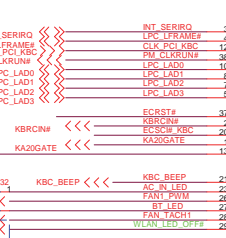
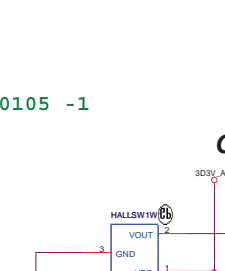
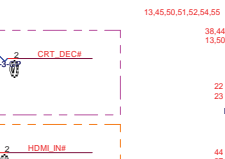
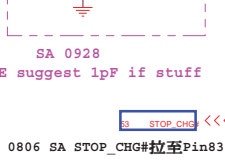
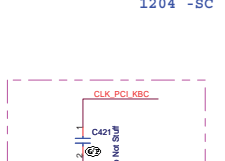
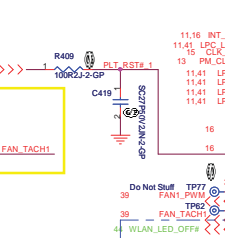
Prevent BIOS data loss solution
1019 -SB



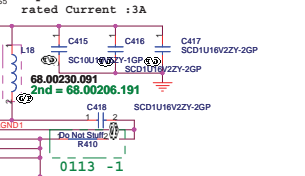
Internal Keyboard Connector



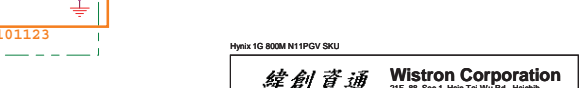
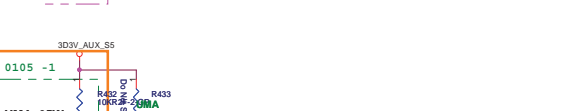
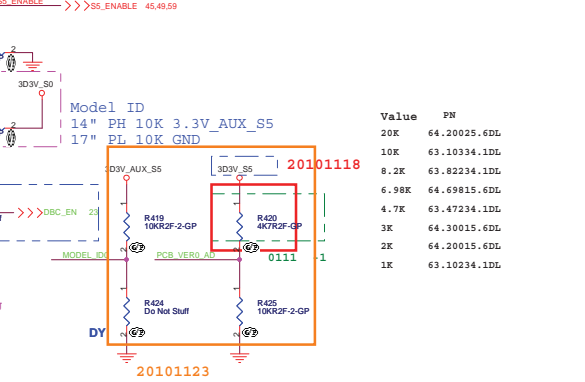
change connect to FPC (Same as Lab)
20.K0251.026 Pin 1 -> left side
20.K0320.026 Pin 1 -> right side (use in lab stage)
so swap net



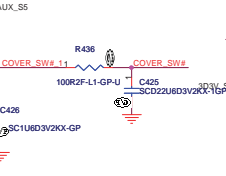
L16 -> 68.00082.011 is a obsoleted part
0930 -SA



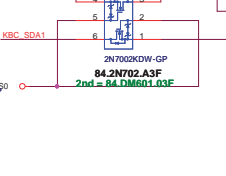
PCB Version AD (Pin#)	Full-Low Resistor	Full-High Resistor (10V, 15)	Voltage
1A	100K	100K	3.0V
1B	100K	100K	2.75V
1C	100K	100K	2.5V
1 (non-3G)	100K	100K	4.7K
1 [G]	100K	100K	1.3V
2 (non-3G)	100K	100K	1.94V
2 [G]	100K	100K	1.1V
3 (non-3G)	100K	100K	1.81V
3 [G]	100K	100K	0.9V
Reserved	100K	100K	1.0V



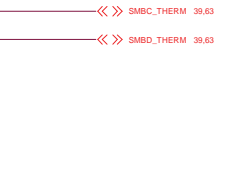
Cover Up Switch



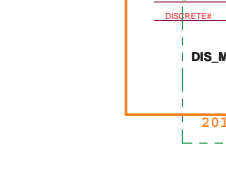
CL Freq tolerance +/- 20 ppm



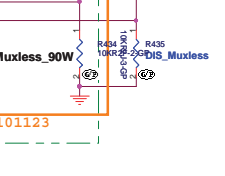
CL Freq tolerance +/- 20 ppm



CL Freq tolerance +/- 20 ppm



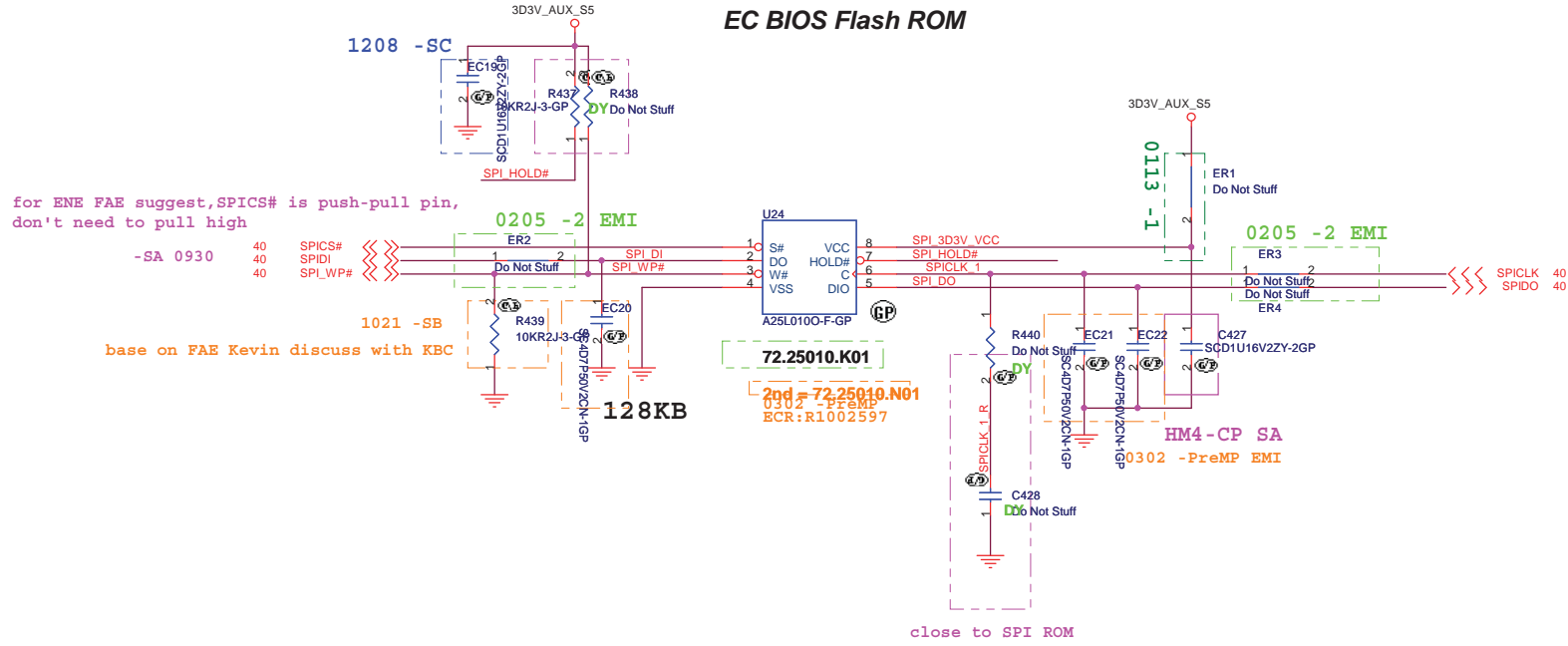
CL Freq tolerance +/- 20 ppm



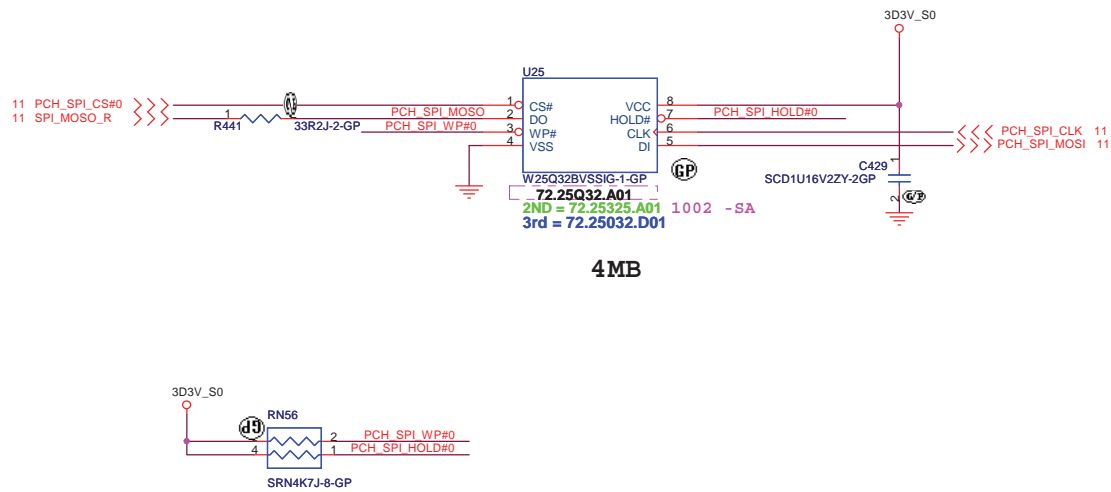
Hynix 1G 800M N11PG SKU

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsinchu, Taipei Hsin 211, Taiwan, R.O.C.

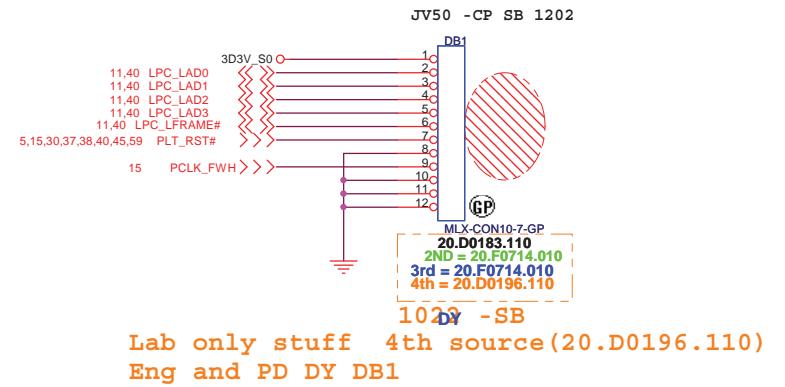
File: **KBC KB3930**
Size: Document Number: **JE43-CP** Rev: -1
Date: Wednesday, November 24, 2010 Sheet: 40 of 69



System BIOS Flash ROM



GOLDEN FINGER FOR DEBUG BOARD



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Hynix 1G 800M N11PGV SKU

緯創資通		Wistron Corporation	
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.			
Title BIOS			
Size	Document Number	Rev	
	JE43-CP	-1	
Date:	Wednesday, November 24, 2010	Sheet	41 of 69

5

4

3

2

1

D

D

C

C

B

B

A

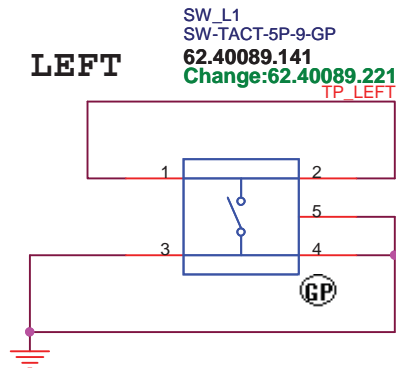
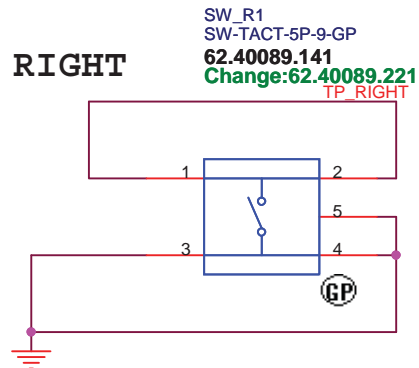
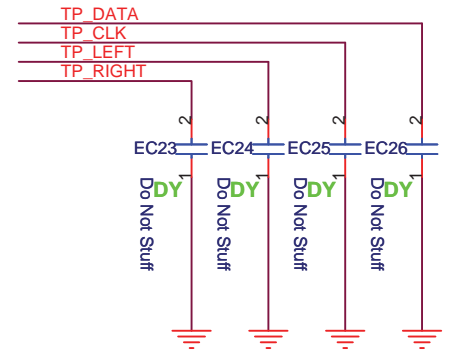
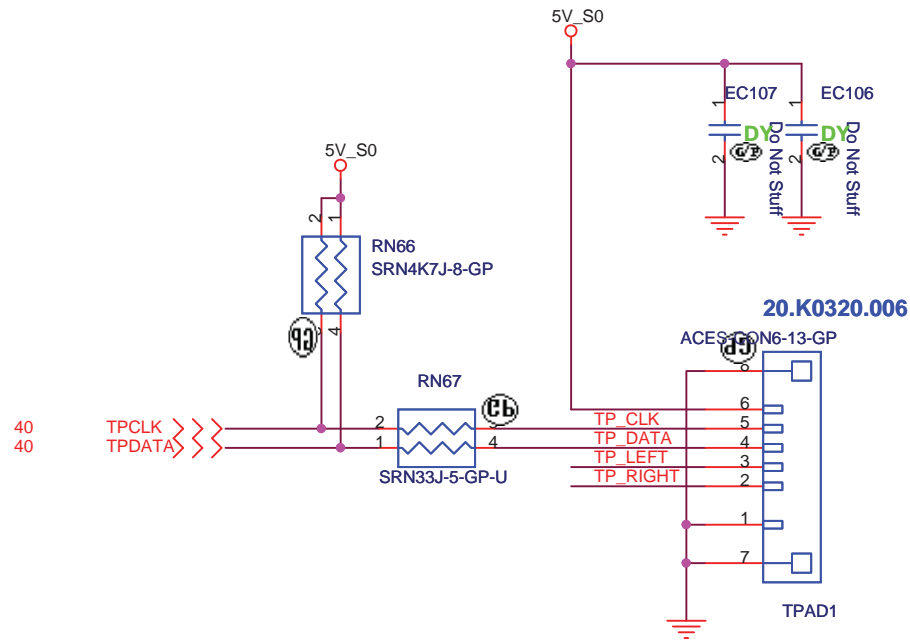
A

<http://hobi-elektronika.net>

Hynix 1G 800M N11PGV SKU

緯創資通		Wistron Corporation	
		<small>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</small>	
Title			

Size	Document Number	Rev	
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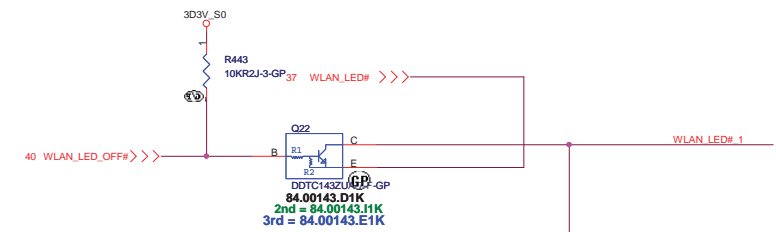
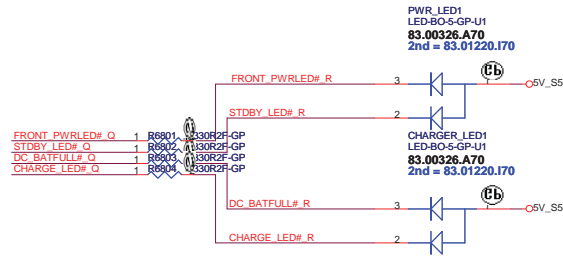
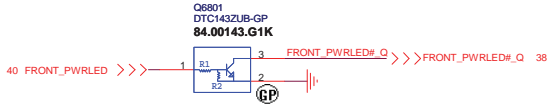
<http://hobi-elektronika.net>

Hynix 1G 800M N11PGV SKU

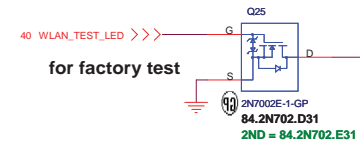
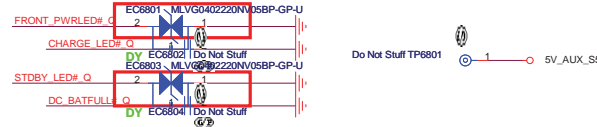
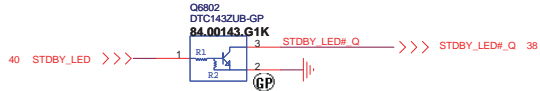
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title Touch PAD_FP CONN		
Size	Document Number	Rev
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Date: Wednesday, November 24, 2010	Sheet 43 of 69	

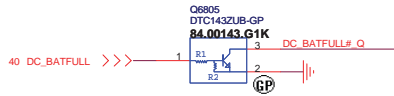
Power button LED



Power STDBY_LED



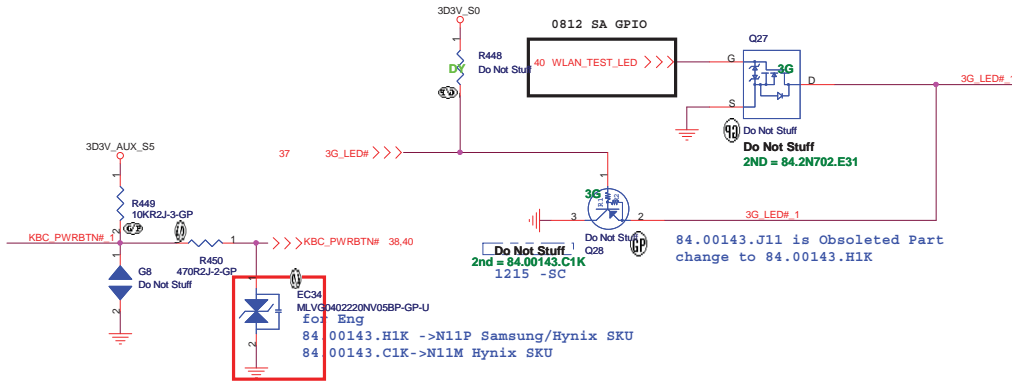
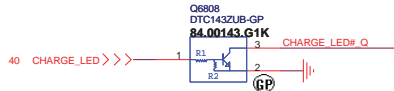
Battery LED2 (DC_BATFULL)



EC6801, EC6803, EC34 請幫忙上件 22p 5.5V 的 Varistor料號是 69.80024.011

For 2010 Acer Project, WLAN and 3G LED control by KBC

Battery LED1 (CHARGE)



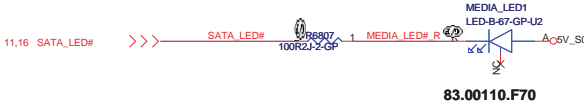
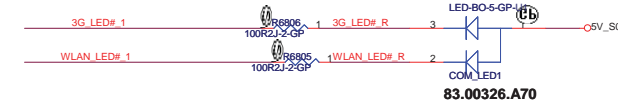
Eng stuff 20.K0491.010 Pin 1 ->right side
PD change to 20.K0228.010 Pin 1 -> right side
do not swap net

Pin 1	5V_S5	
Pin 2	FRONT_PWLED#_56_R	AC IN
Pin 3	5V_S0	
Pin 4	MEDIA_LED#_R	HDD
Pin 5	3G_LED#_R	3G
Pin 6	3D3V_S0	
Pin 7	WLAN_LED#_R	WLAN
Pin 8	KBC_PWRBTN#_1	Power button
Pin 9	FRONT_PWLED#_Q	Power LED
Pin 10	GND	

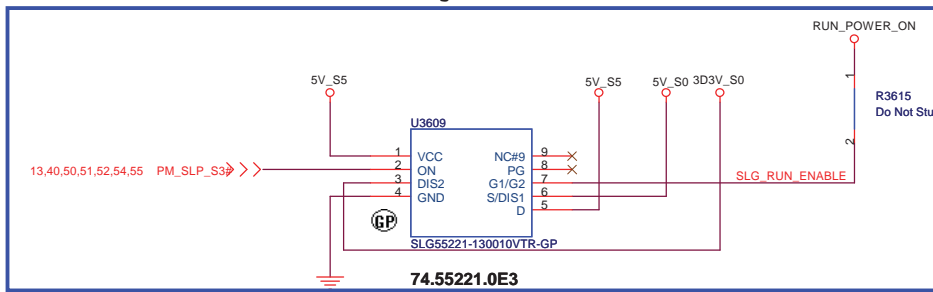
1208 -SC

	WLAN_LED_OFF#	WLAN_TEST_LED	WWAN_LED
WLAN ON Always on	L	H	L
WLAN ON (flash)	H	L	L
WWAN_ON	L	L	H
WLAN ON WWAN_ON	L	L	H

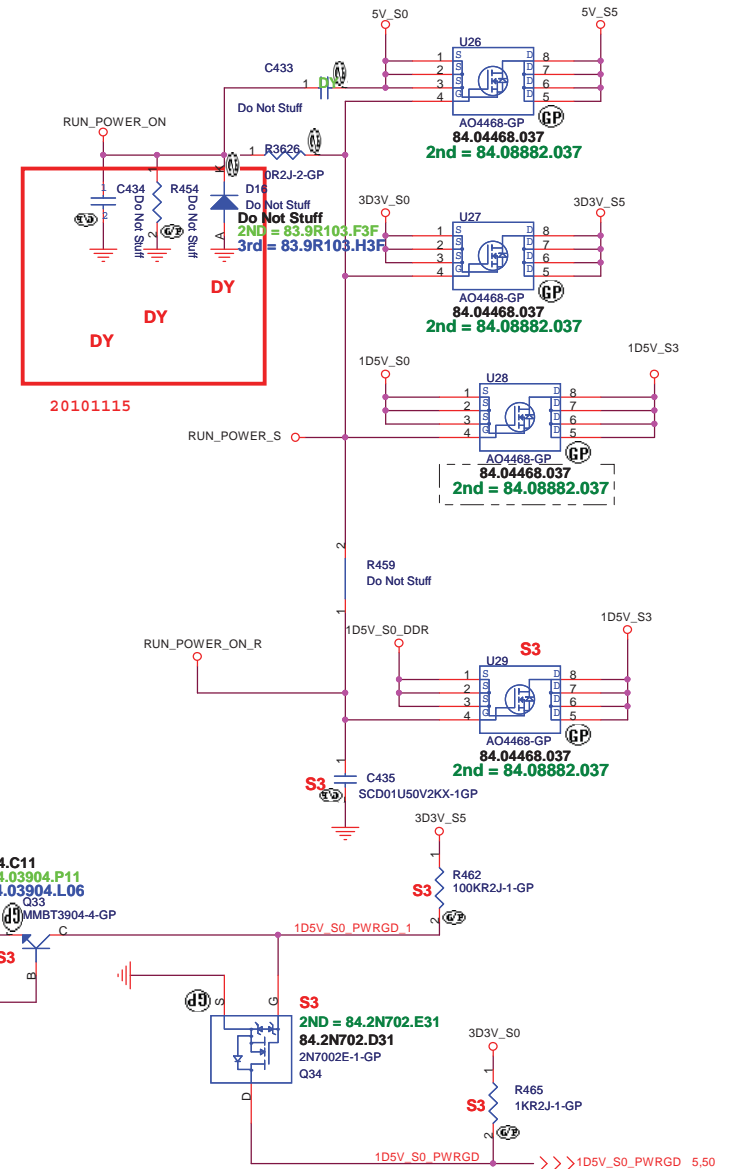
SATA HDD LED



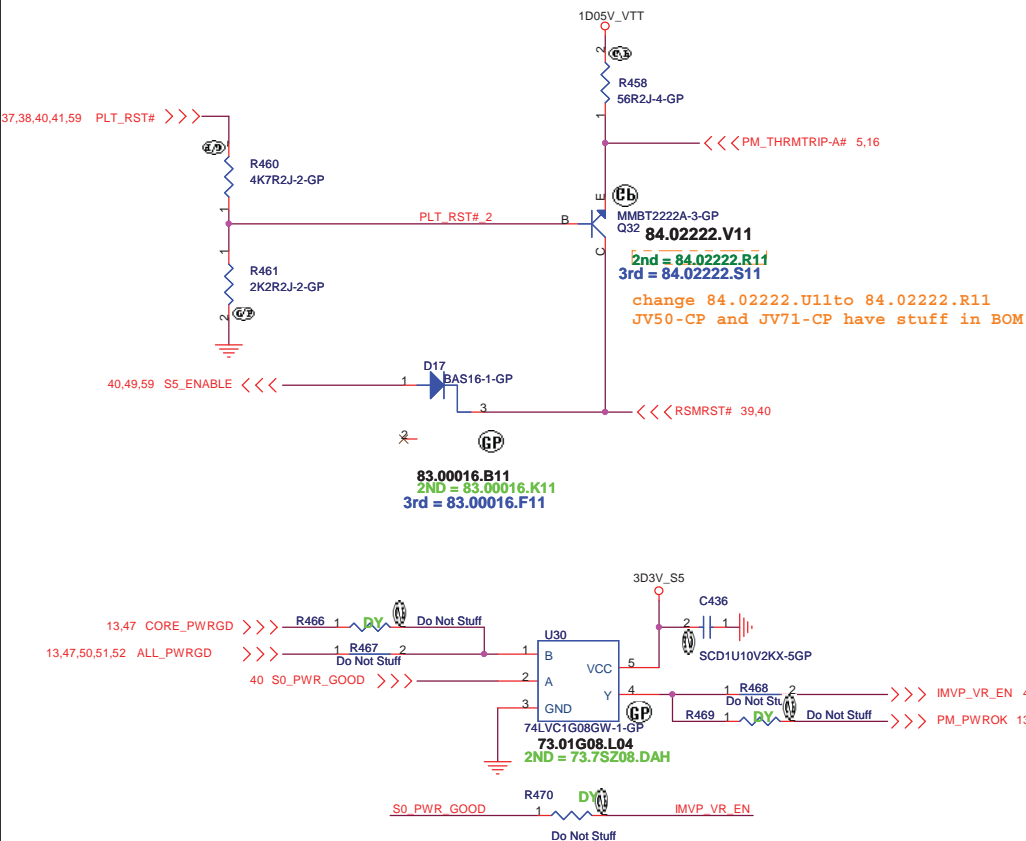
<http://hobi-elektronika.net>



Run Power



3D3V_AUX_S5
*Del Aux Power schematic,
 it is not necessary for reservation*



PM_SLP_S3#	1D5V_S0_DDR	1D5V_S0_PWRGD	0D75_S0
0	0	0	0
1	1	1	1

Hynix 1G 800M N11PGV SKU

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 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
 Taipei Hsien 221, Taiwan, R.O.C.

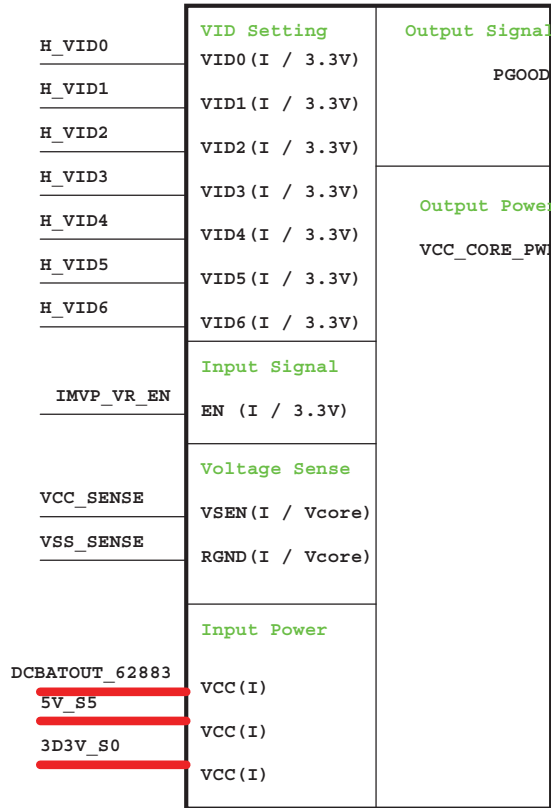
Title: **RUN POWER and 3D3V AUX S5**

Size: Document Number **JE43-CP** Rev -1

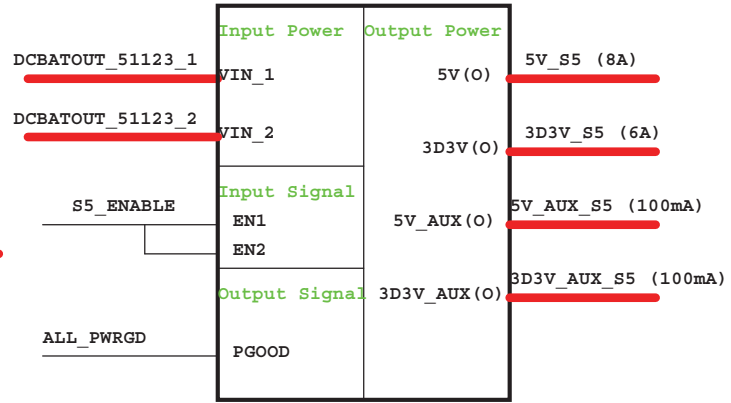
Date: Wednesday, November 24, 2010 Sheet 45 of 69

<http://hobi-elektronika.net>

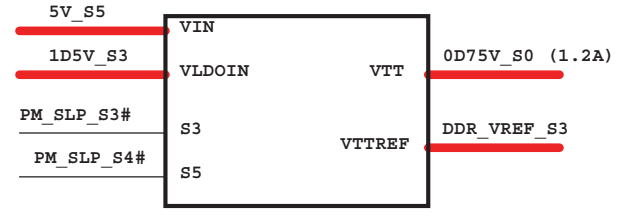
ISL62883 VCC_CORE



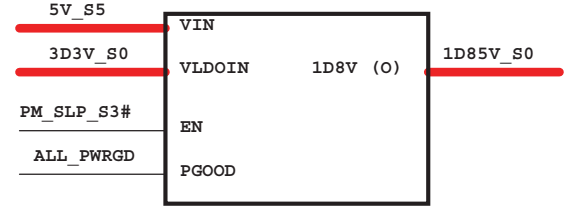
TPS51123 5V/3D3V



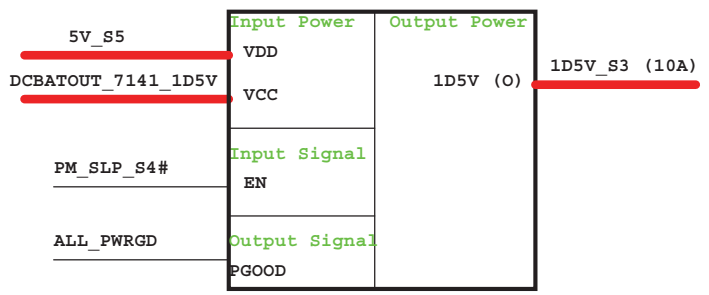
RT9026 0D75V_S0



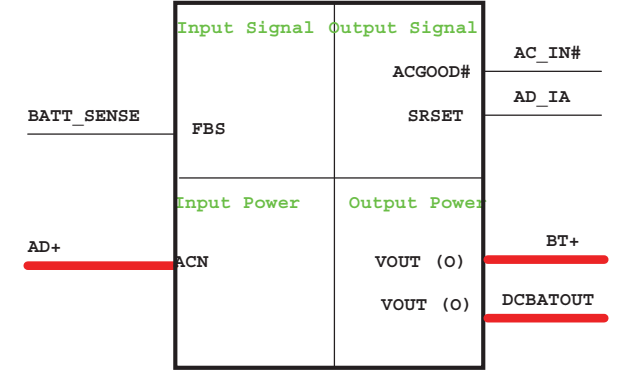
RT9025 1D8V



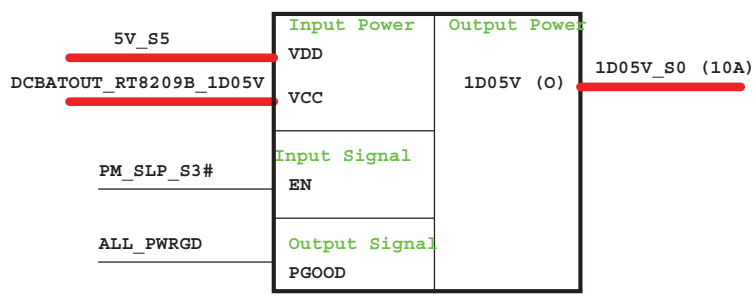
RT9025 1D5V



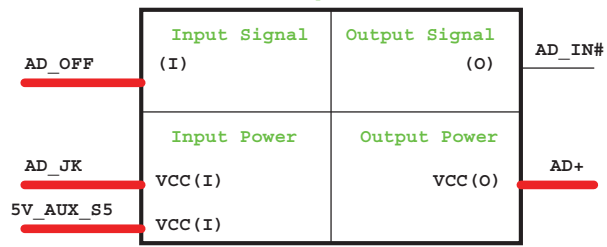
Charger BQ24745



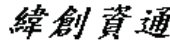
RT8209B 1D05V

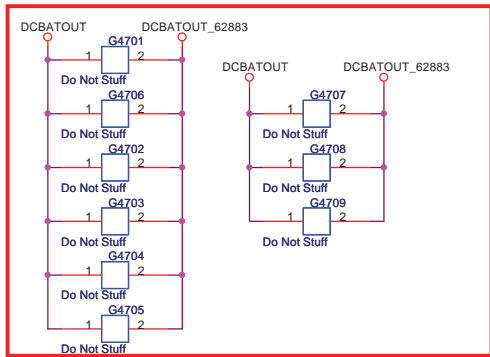


Adapter

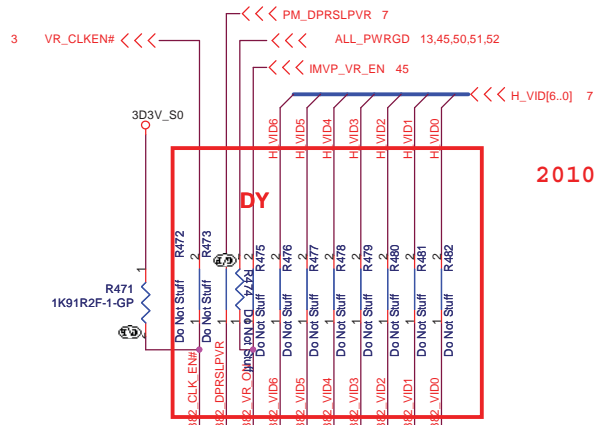


Hynix 1G 800M N11PGV SKU

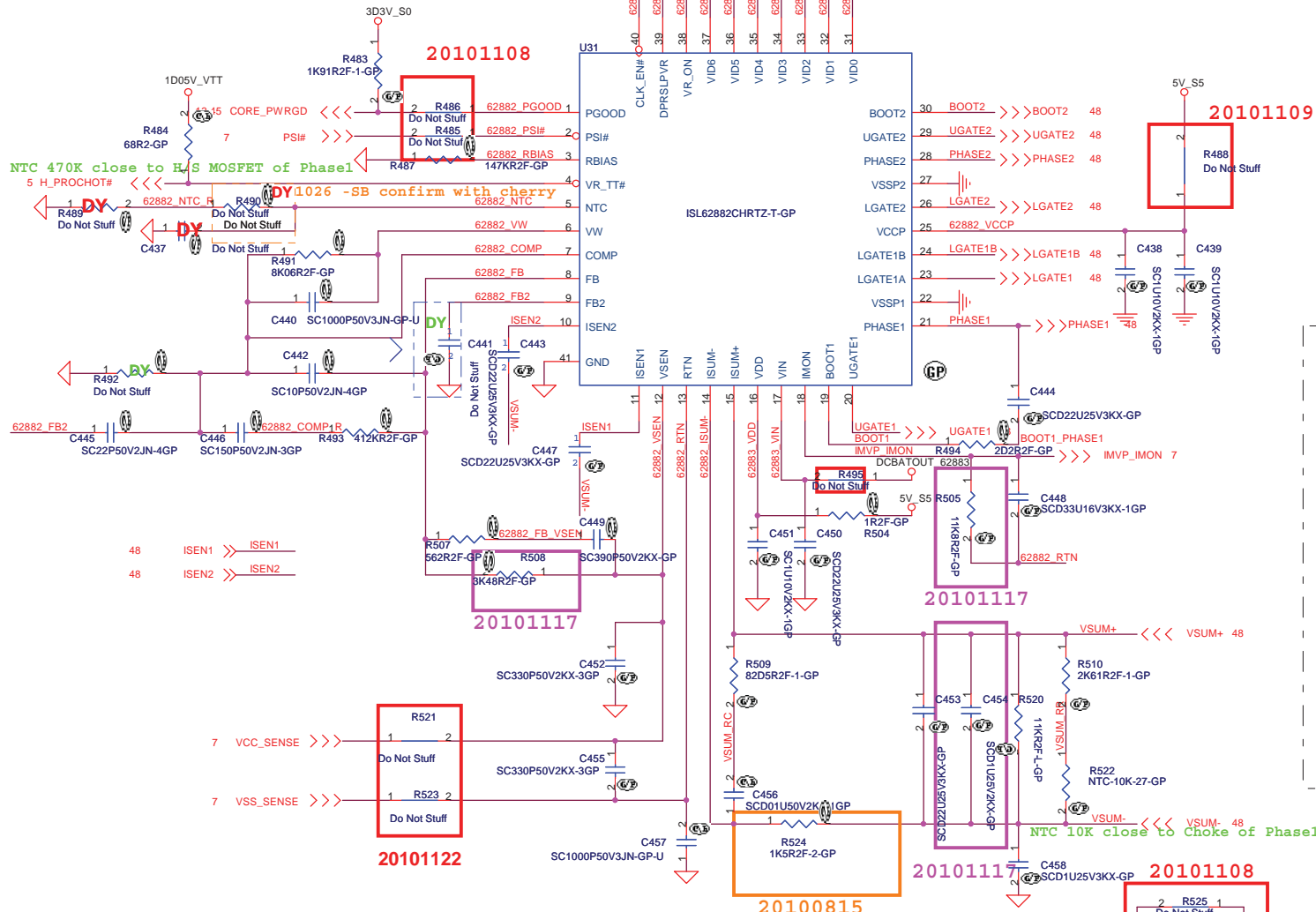
 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Power Block Diagram	
Size	Document Number
	JE43-CP
Date: Wednesday, November 24, 2010	Sheet 46 of 69



20100717



20101020



20101108

20101109

20101117

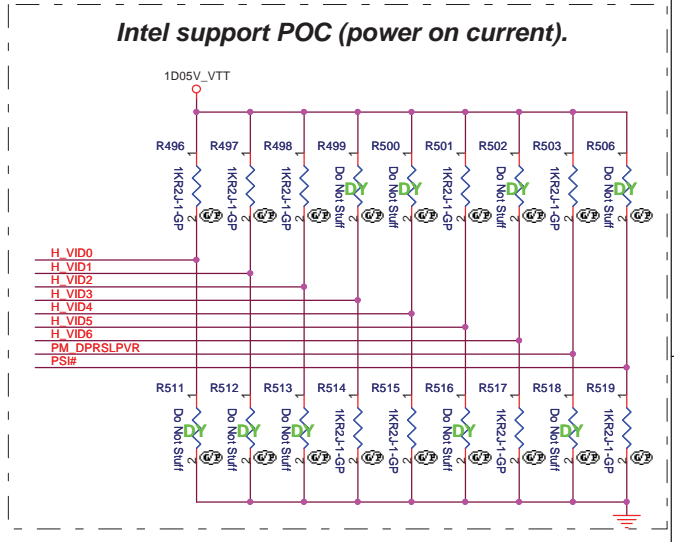
20101117

20101122

20100815

20101117

20101108



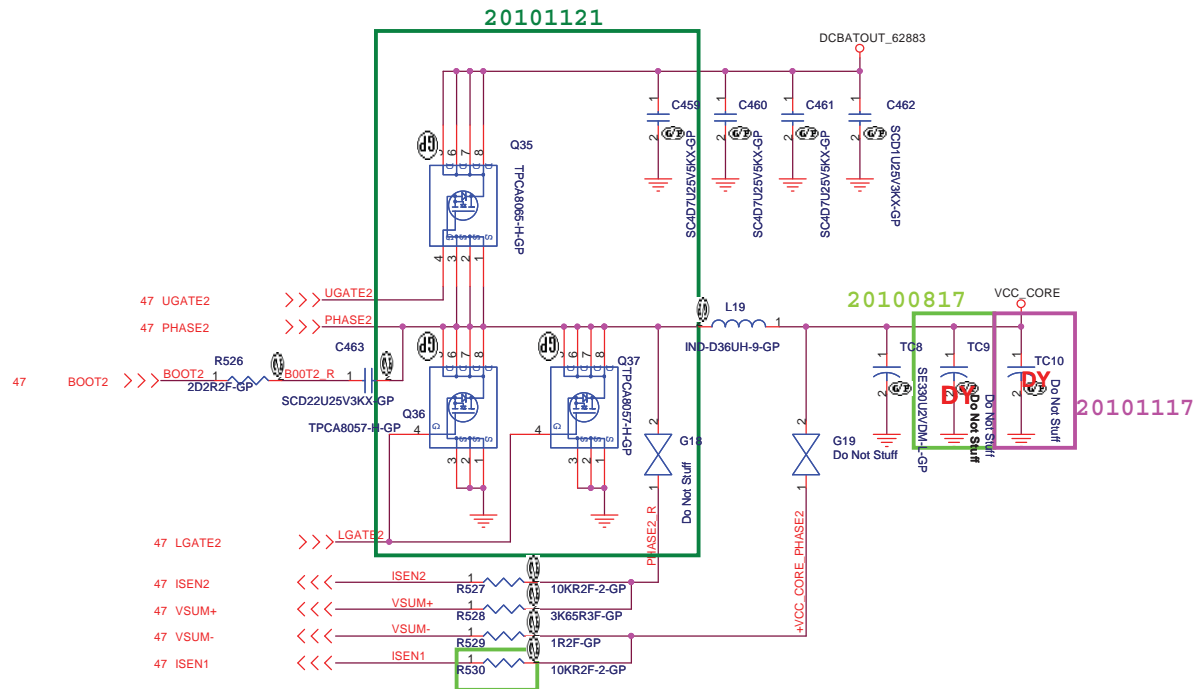
Intel support POC (power on current).

Hynix 1G 800M N11PGV SKU

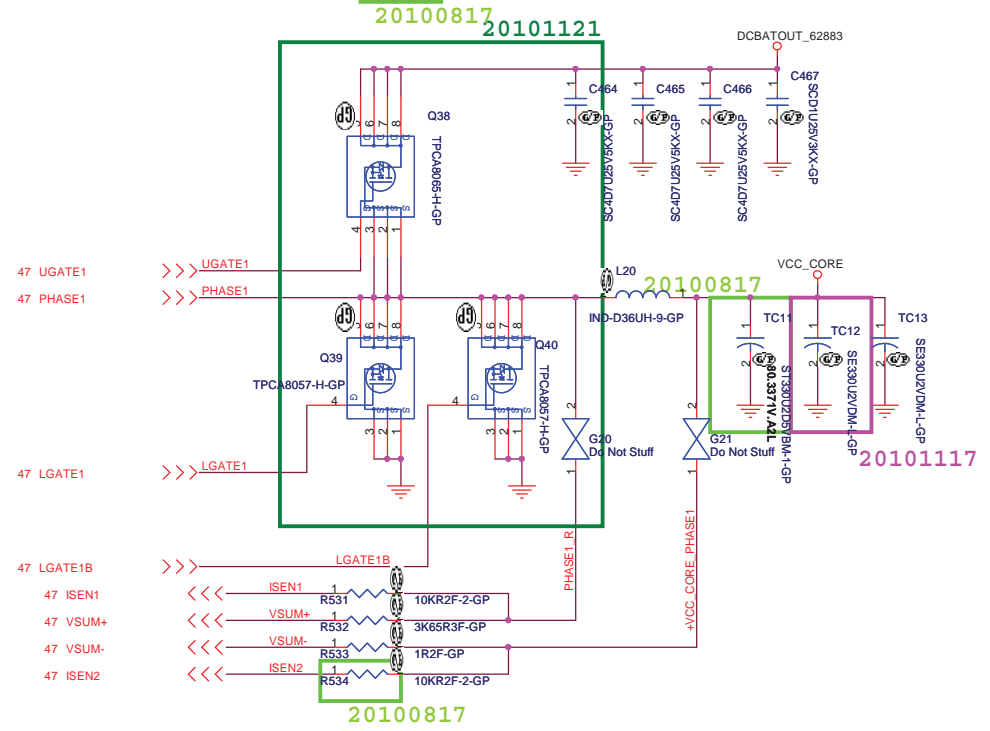
緯創資通 Wistron Corporation
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hstchih, Taipei Hsien 221, Taiwan, R.O.C.

Title		ISL62882 CPU CORE (1 / 2)	
Size	Document Number	Rev	
		JE43-CP	
Date:	Wednesday, November 24, 2010	Sheet	47 of 69

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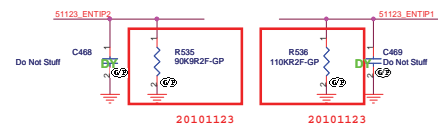
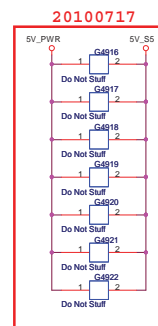
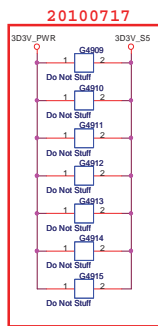
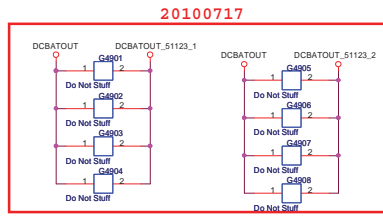
Vcc_core
Iomax=48A
OCP>72A



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Hynix 1G 800M N11PGV SKU

緯創資通		Wistron Corporation	
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Title			
ISL62882 CPU CORE (2 / 2)			
Size	Document Number		Rev
	JE43-CP		-1
Date:	Wednesday, November 24, 2010	Sheet	48 of 69



20100717
 68.3R31A.10V
 Mag, 6.86*6.74*3
 IND-3D3UH
 DCR=28-30mohm
 Irating=6A, Isat=13.5A

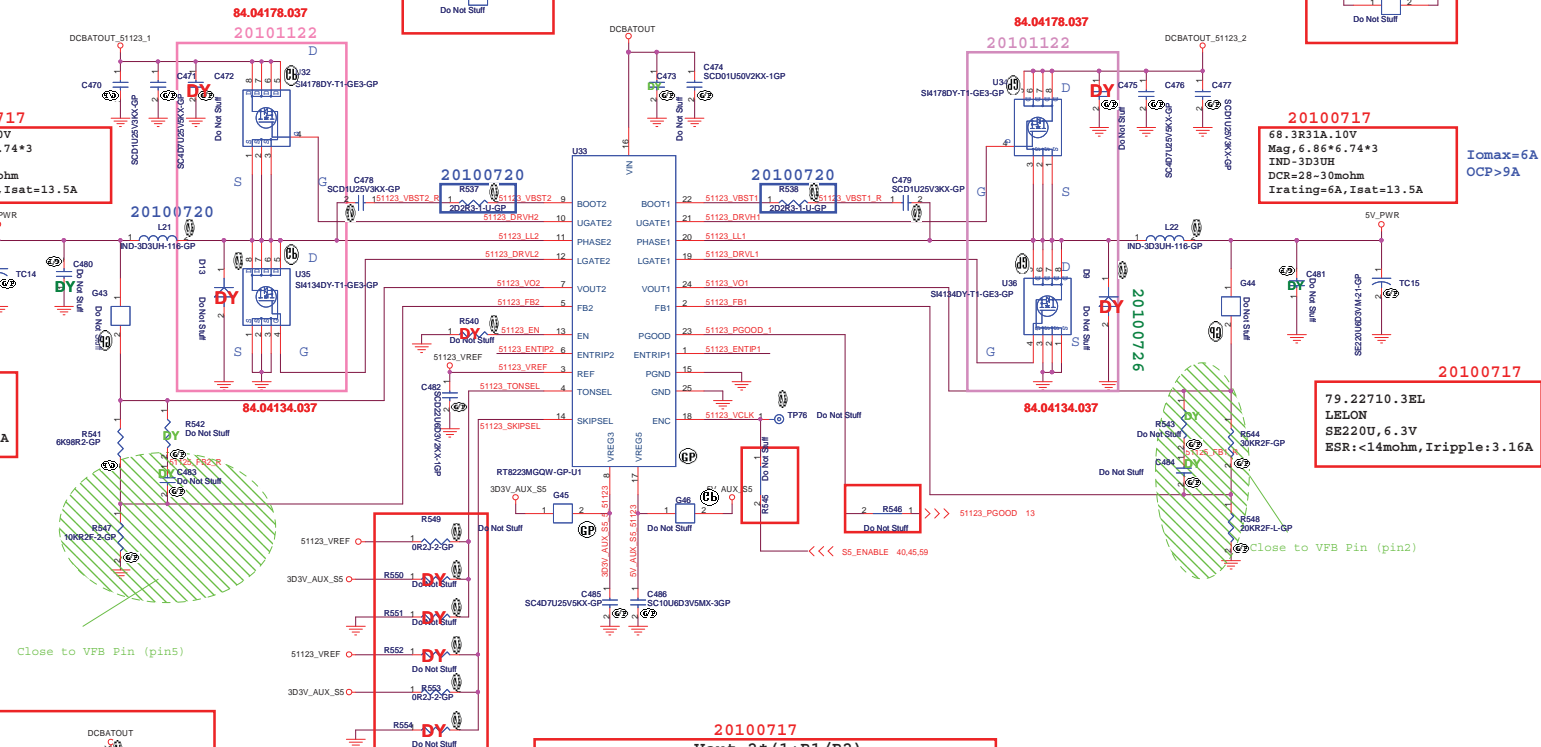
20100717
 68.3R31A.10V
 Mag, 6.86*6.74*3
 IND-3D3UH
 DCR=28-30mohm
 Irating=6A, Isat=13.5A

Iomax=5A
 OCP>7.5A

Iomax=6A
 OCP>9A

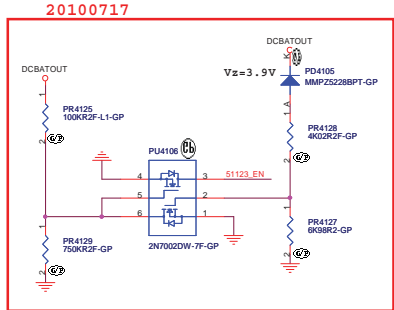
20100717
 79.22710.3EL
 LELON
 SE220U, 6.3V
 ESR:<14mohm, Iripple:3.16A

20100717
 79.22710.3EL
 LELON
 SE220U, 6.3V
 ESR:<14mohm, Iripple:3.16A

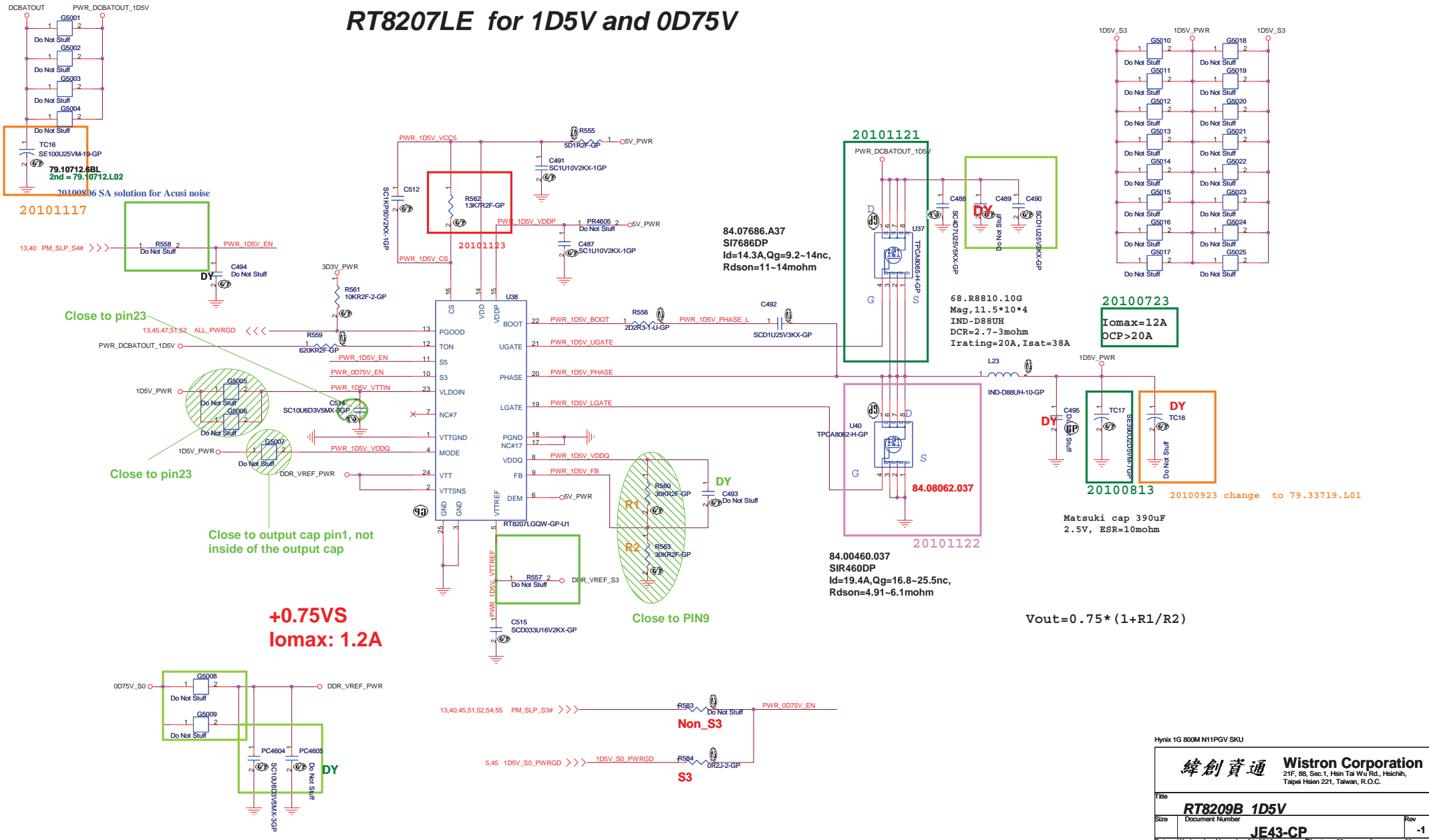


20100717
 $V_{out} = 2 * (1 + R1/R2)$

	GND	VREF	VREG3	VREG5
SKIPSEL	AUTOSKIP	PWM	00A AUTOSKIP	00A AUTOSKIP
TONSEL	200k/CH1 250k/CH2	245k/CH1 305k/CH2	300k/CH1 375k/CH2	365k/CH1 460k/CH2



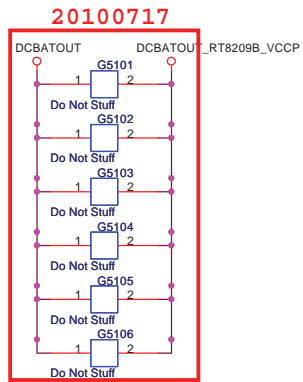
RT207LE for 1D5V and 0D75V



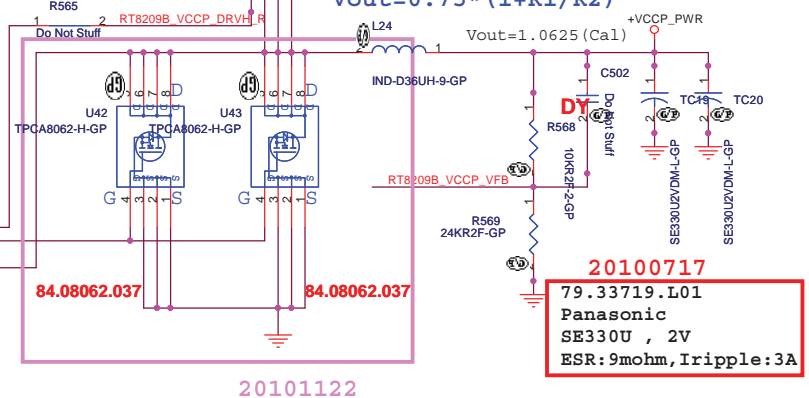
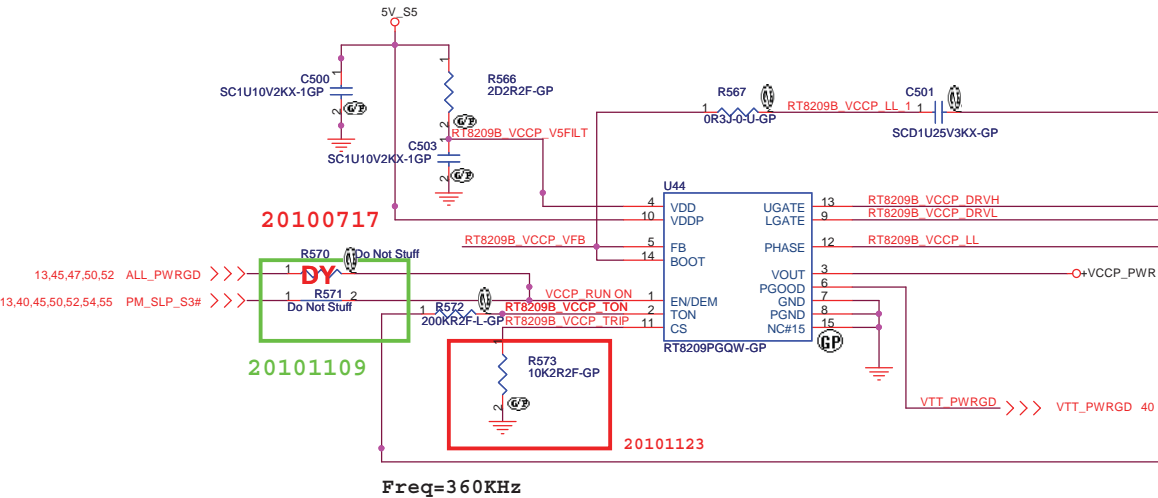
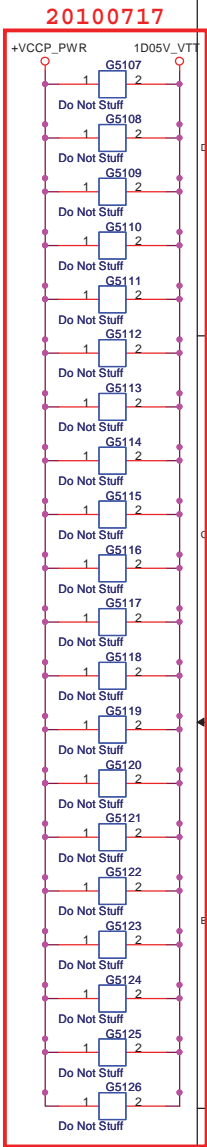
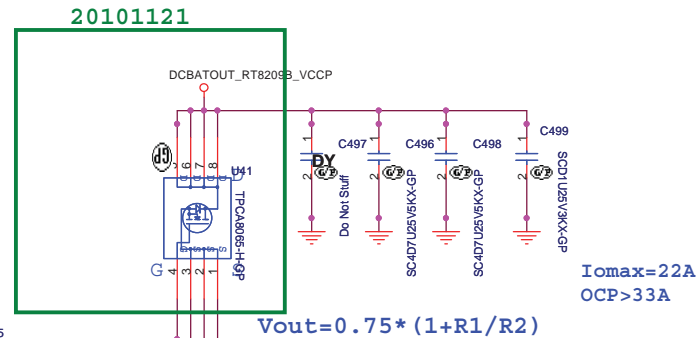
+0.75VS
Iomax: 1.2A

$$V_{out} = 0.75 * (1 + R1/R2)$$

Wistron Corporation		21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title: RT209B 1D5V			
Size: Document Number	JE43-CP		Rev: -1
Date: Wednesday, November 24, 2010	Sheet: 50	of: 69	



RT8209E for VCCP

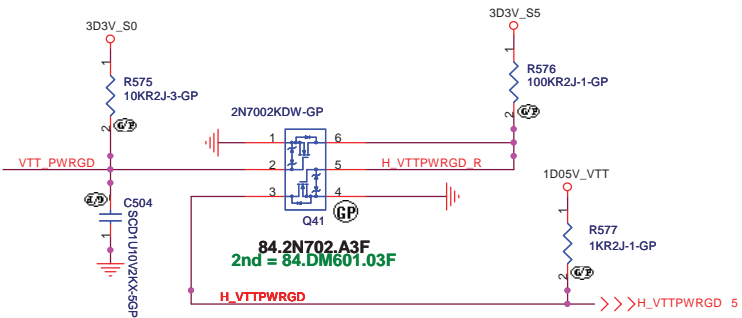


20100717
79.33719.L01
Panasonic
SE330U , 2V
ESR:9mohm, Iripple:3A

13,45,47,50,52 ALL_PWRGD >>>
13,40,45,50,52,54,55 PM_SLP_S3# >>>

VTT_PWRGD >>> VTT_PWRGD 40

because of 1.05V_S0 and 1.05V_VTT combin together
use PM_SLP_S3# Enable 1.05V power



RT8209B_VCCP_VFB 1 R574 Do Not Stuff >>> VTT_SENSE 7

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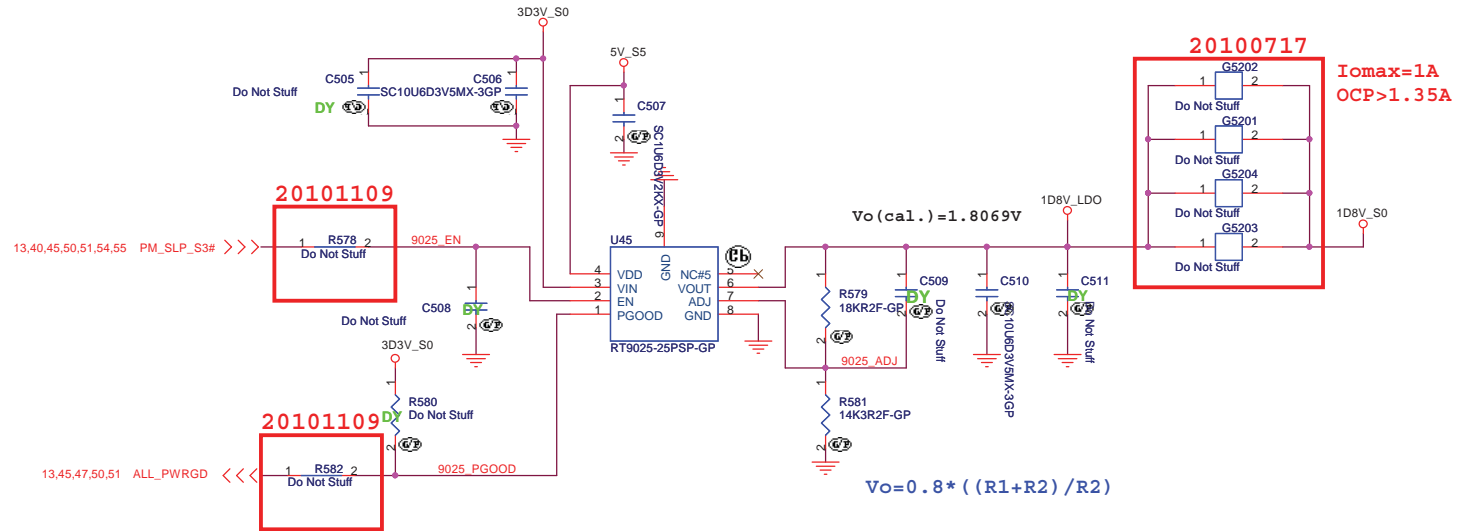
Hynix 1G 800M N11PGV SKU

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Taipei Hsien 221, Taiwan, R.O.C.

Title	RT8209B +VCCP	
Size	Document Number	Rev
		-1
Date:	Wednesday, November 24, 2010	Sheet 51 of 69

RT9025 for 1D8V_S0

20090915

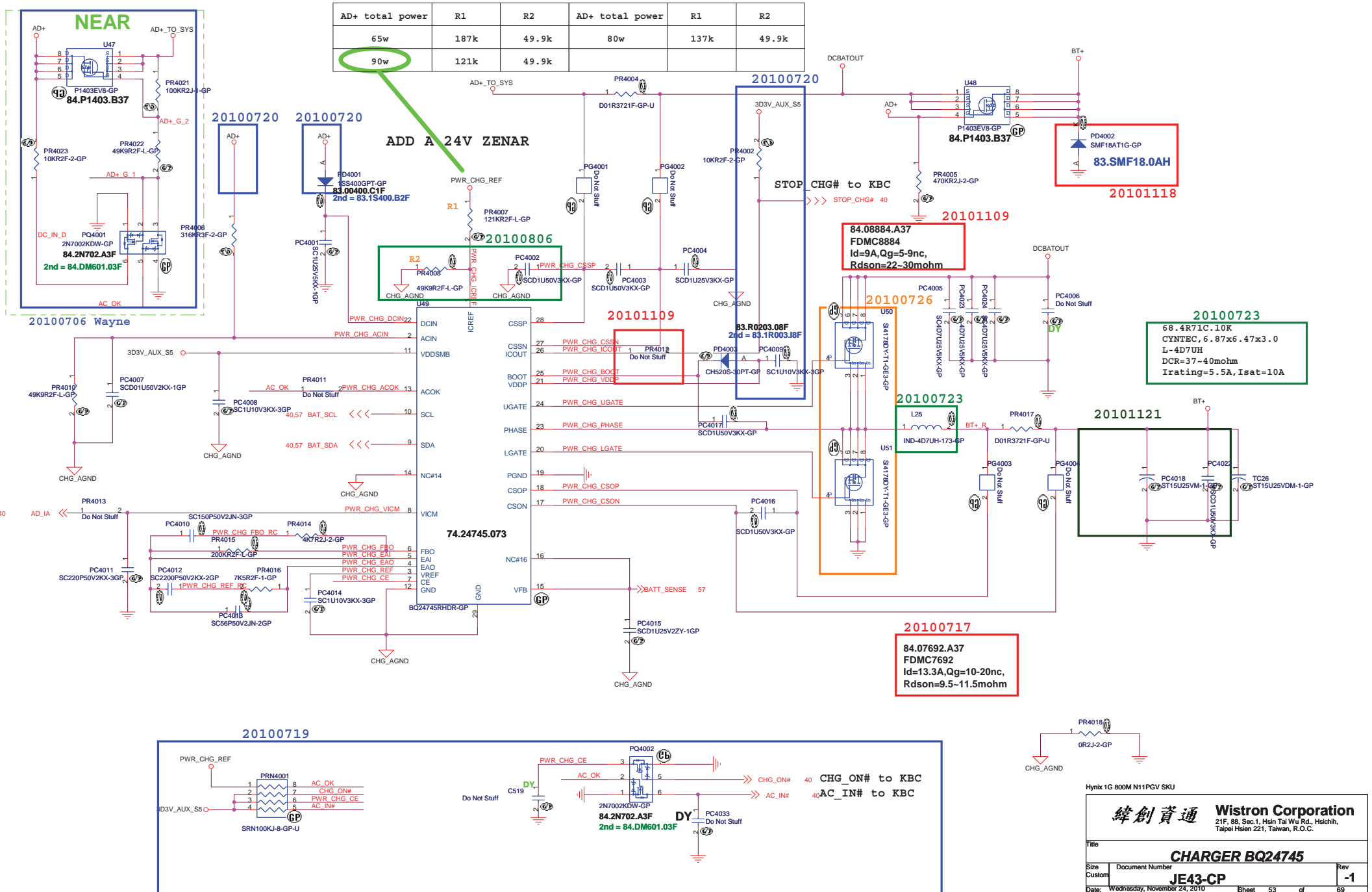


<http://hobi-elektronika.net>

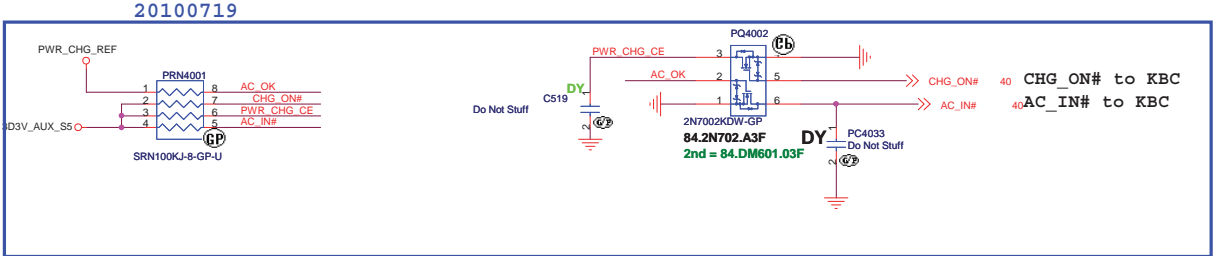
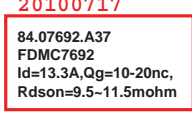
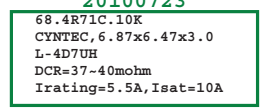
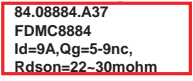
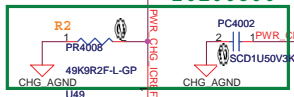
Hynix 1G 800M N11PGV SKU

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title		
RT9025 1D8V/RT9026 0D75		
Size	Document Number	Rev
		-1
Date: Wednesday, November 24, 2010		
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AD+ total power	R1	R2	AD+ total power	R1	R2
65w	187k	49.9k	80w	137k	49.9k
90w	121k	49.9k			



ADD A 24V ZENAR



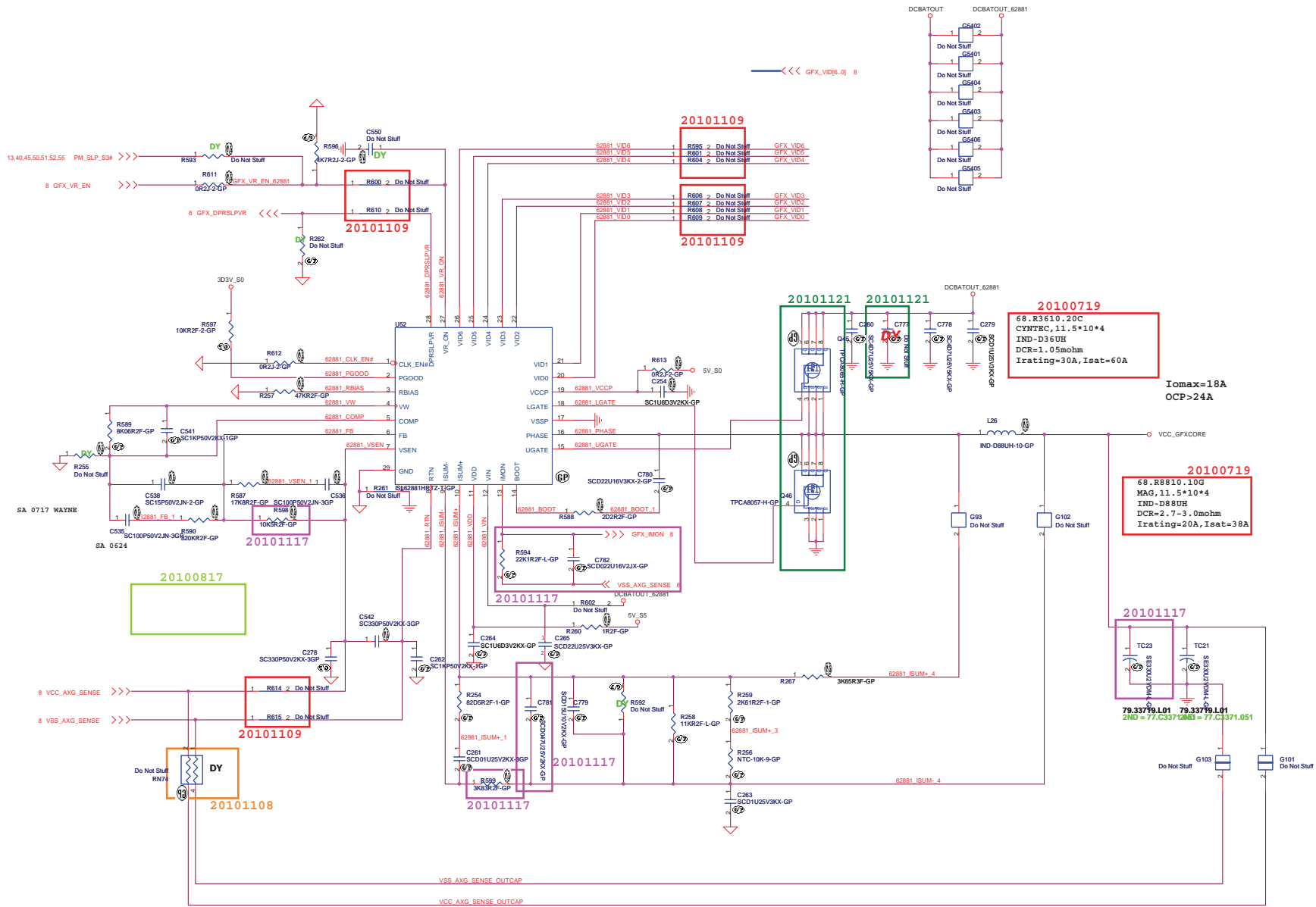
Hynix 1G 800M N11PGV SKU

緯創資通 Wistron Corporation
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

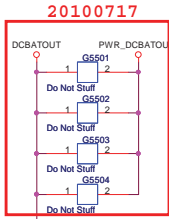
Title: **CHARGER BQ24745**

Size: Document Number **JE43-CP** Rev **-1**

Date: Wednesday, November 24, 2010 Sheet 53 of 69

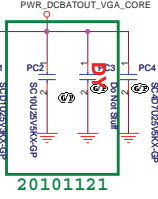
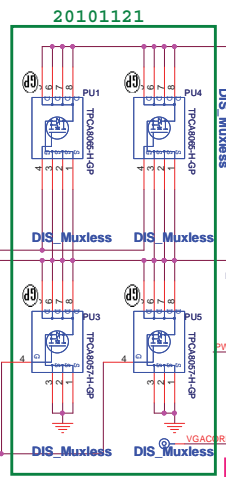
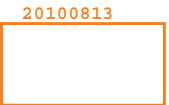


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SSID = PWR.Plane.Regulator_GFX

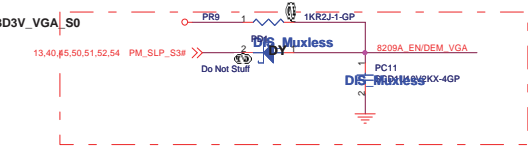
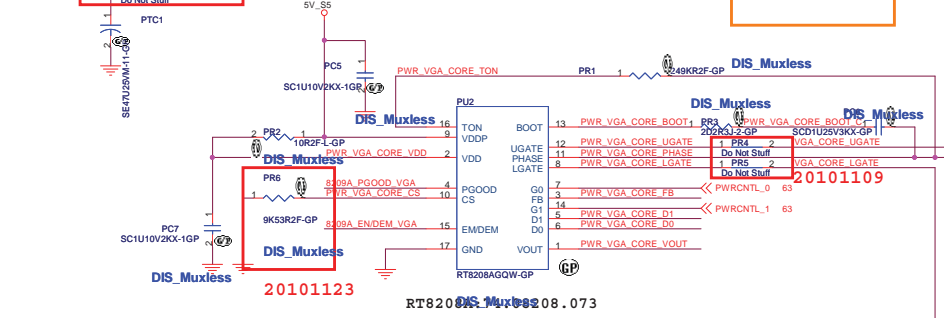
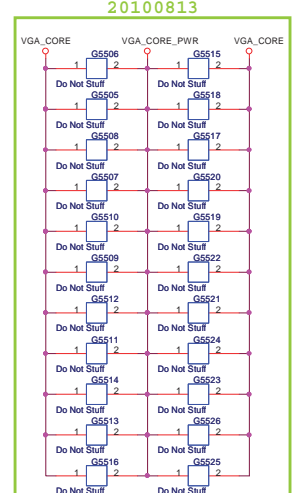
N12P-GV and N11P-GV, PR6換成9.1K
(part number: 64.91015.6DL), MOSFET 請用TPCA8065-H +TPCA8062-Hx2 上一下二



$V_{out} = 0.75V * (R1 + R2) / R2$

84.07686.A37
CYNTEC, 11.5*10*4
IND-D36UH
DCR=1.05mohm
Irating=30A, Isat=60A

Design Current = 21.94A
24.14A < OCP < 28.53A



N11P-GV

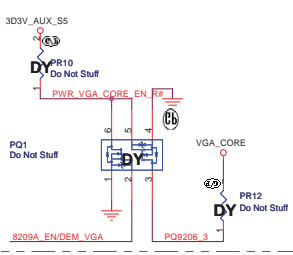
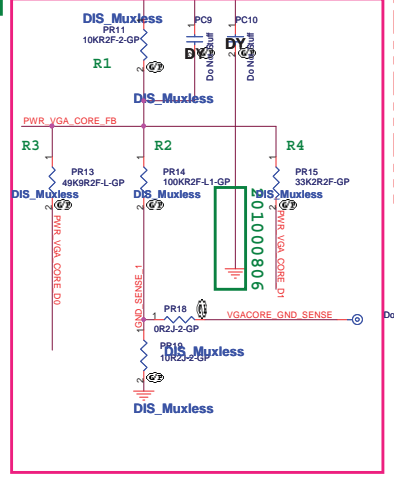
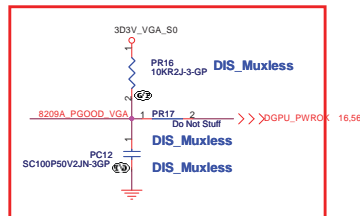
P-State	PWR_VGA_CORE_D1	PWR_VGA_CORE_D0	VGA_CORE_PWR
P8, P12	L	L	0.85V
P0 - HOT	L	H	0.90V
P0 - COLD	H	L	0.95V
	H	H	

I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
Inductor: 1.5UH PCMC104T-1R5MN Cyntec DCR:4.2mohm Isat =33Arms 68.1R510.10J
O/P cap: 330U 2V EEPFSX0D331ER 9mOhm 3Arms Panasonic/ 79.33719.L01
H/S: SI7686DP/ POWERPAK-8/11mOhm/14mOhm@4.5Vgs/ 84.07686.037
L/S: SiR460DP/ POWERPAK-8/ 4.9mOhm/6.1mohm@4.5Vgs/ 84.00460.037

Switching freq-->350KHz

Frequency setting

470K	-->165KHz
200K	-->323KHz
100K	-->500KHz



33.2K=64.33225.6DL
43K=64.43025.6DL
75K=64.75025.6DL
100K=64.10035.6DL
150K=64.15035.6DL

N12P_GS

P-State	PWR_VGA_CORE_D1	PWR_VGA_CORE_D0	VGA_CORE_PWR
P8, P12	L	L	0.825V
P0 - HOT	L	H	0.975V
P0 - COLD	H	L	1.05V
	H	H	

N12P_GV

P-State	PWR_VGA_CORE_D1	PWR_VGA_CORE_D0	VGA_CORE_PWR
P8, P12	L	L	0.85V
P0 - HOT	L	H	1.00V
P0 - COLD	H	L	1.02V
	H	H	

N12P GS: PR11=10K, PR14=100K, PR13=49.9K, PR15=33.2K
N12P GV: PR11=10K, PR14=75K, PR13=49.9K, PR15=43K
N11P GV: PR11=10K, PR14=75K, PR13=150K, PR15=75K

Hynix 1G 800M N11PGV SKU

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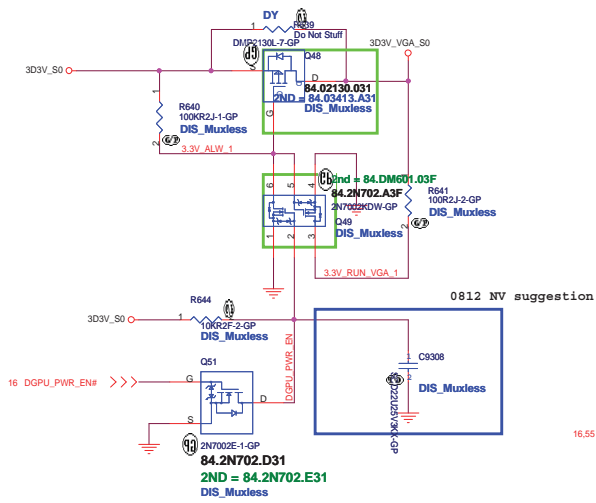
File: **RT8208B +VGA CORE**

Size: Document Number **JE43-CP** Rev: **-1**

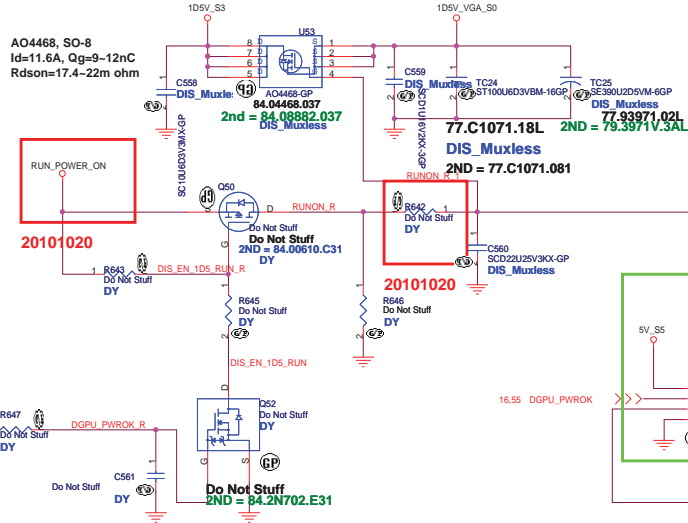
Date: Wednesday, November 24, 2010 Sheet 55 of 89

+3VS to 3.3V_DELAY Transfer

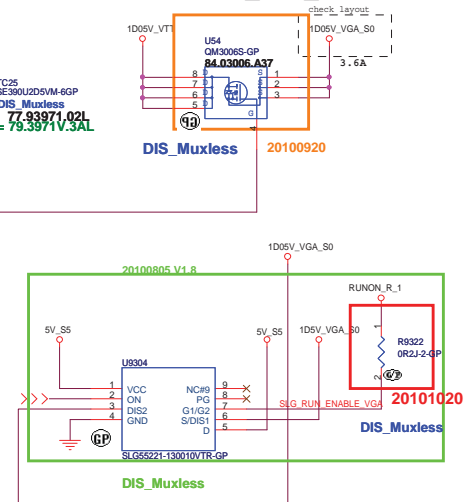
+3VS to 3.3V_DELAY Transfer



1D5V_VGA_S0

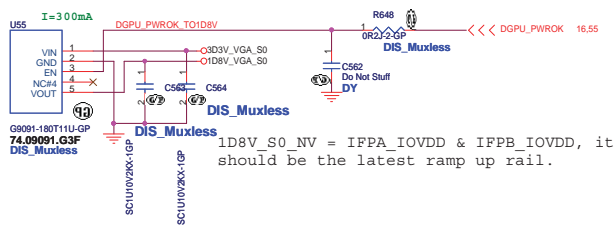


1.05V to 1.05V_VGA_S0 Transfer



RT9025 for 1D8V_VGA

+3VS to 1.8V Transfer



1D8V_S0_NV = IPPA_IOVDD & IPPB_IOVDD, it should be the latest ramp up rail.

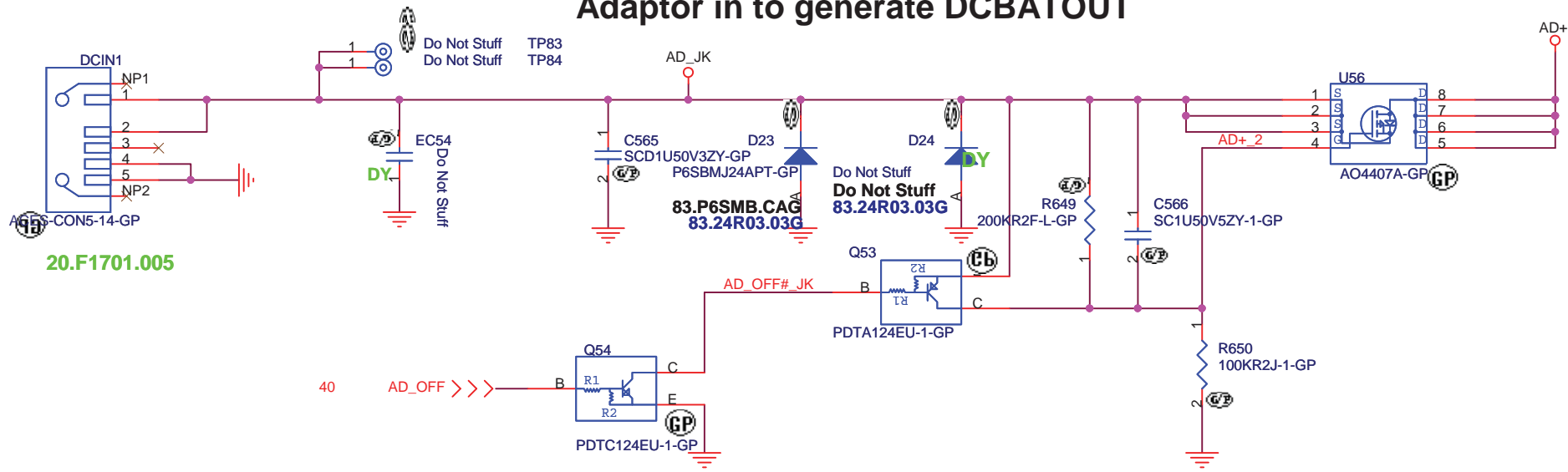
Hynix 1G 800M N11PGV SKU

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

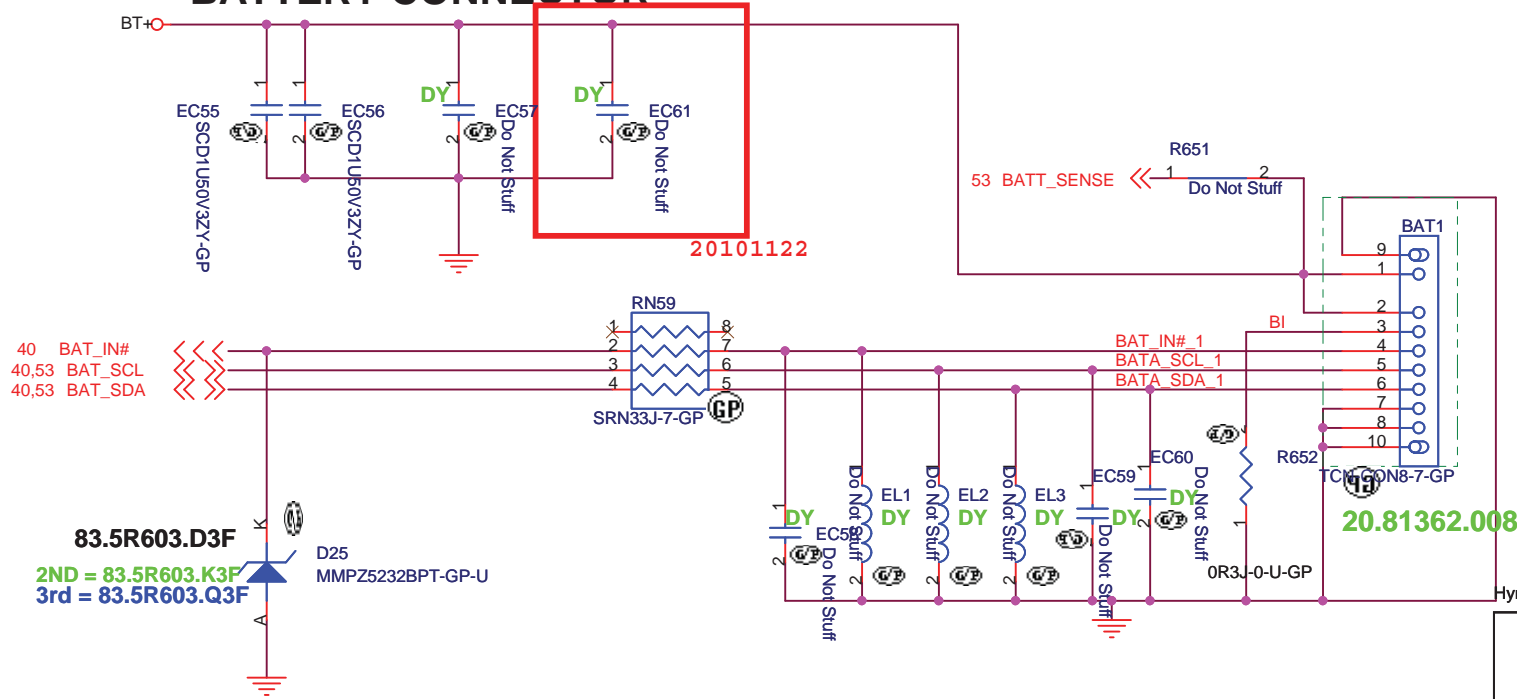
Title			DISCRETE VGA POWER
Size	Document Number	Rev	
C	JE43-CP	-1	
Date:	Wednesday, November 24, 2010	Sheet	56 of 69

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Adaptor in to generate DCBATOUT



BATTERY CONNECTOR



Pin Definition:

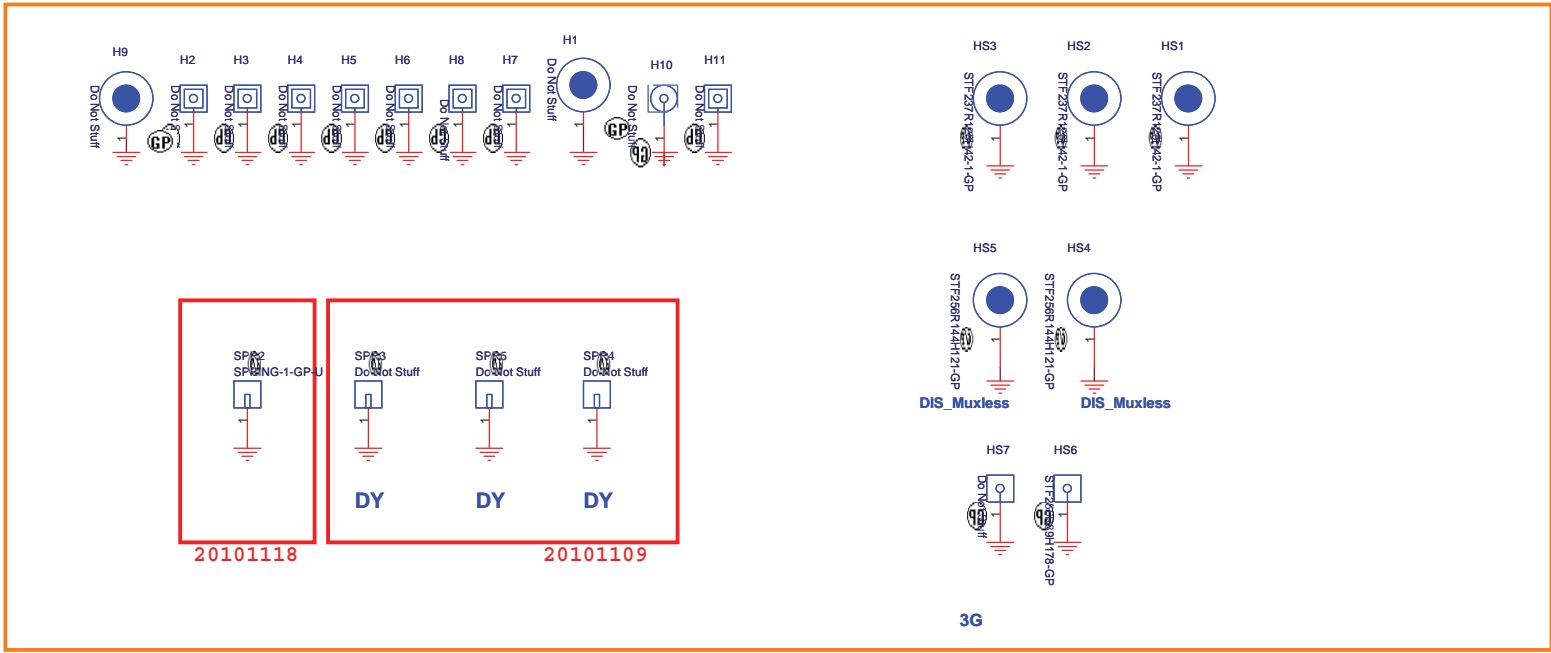
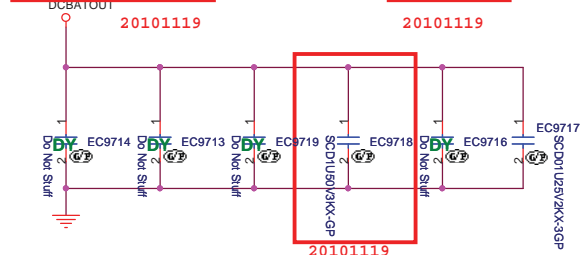
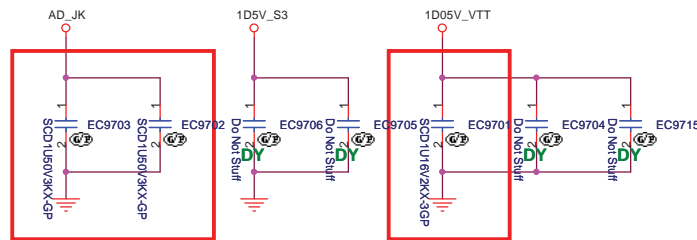
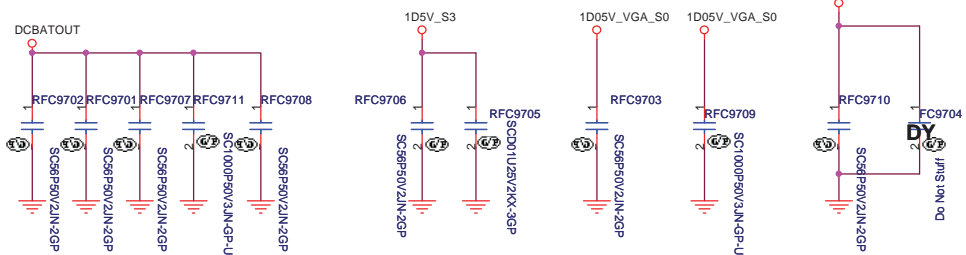
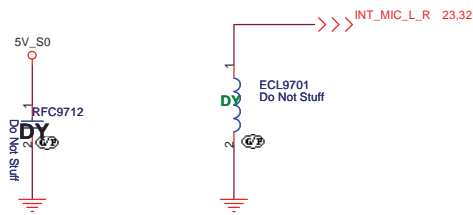
1	GND	Batt-, Battery Negative Terminal
2	GND	Batt-, Battery Negative Terminal
3	SMD	SMBus data interface I/O pin
4	SMC	SMBus clock interface I/O pin
5	TH	Connect to Resistor to GND (10kΩ to GND)
6	BI	System present pin, low active
7	BATT+	Batt+, Battery Positive Terminal
8	BATT+	Batt+, Battery Positive Terminal

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Check test point

delete 3D3V_S0 test point



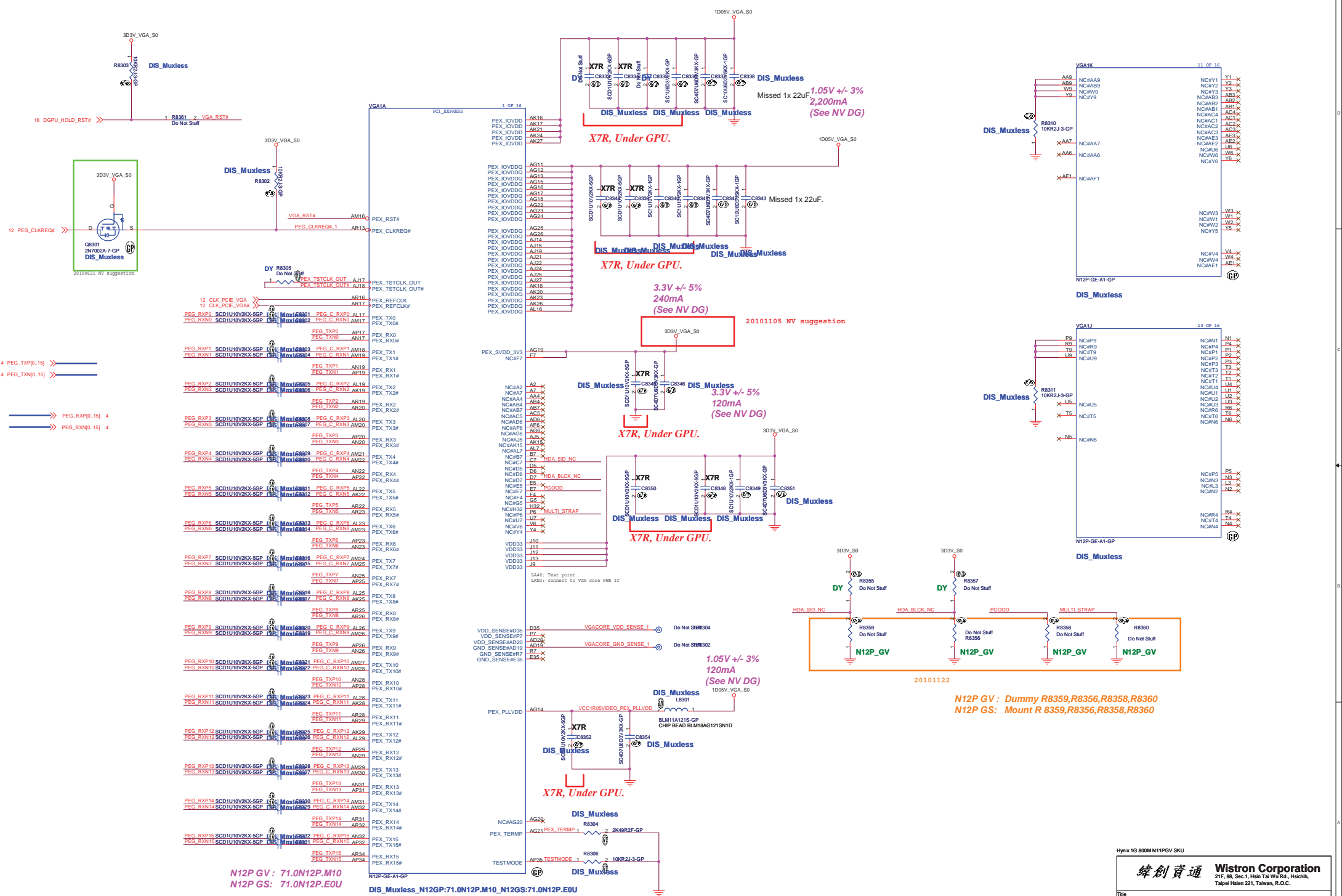
Test Point放在Dimm Door打開可量測處

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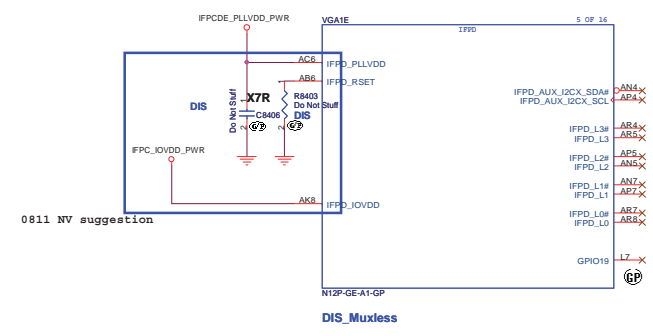
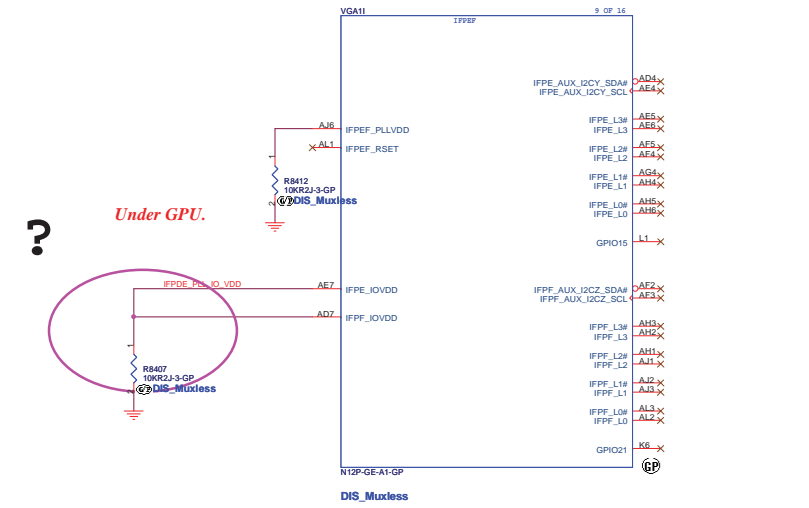
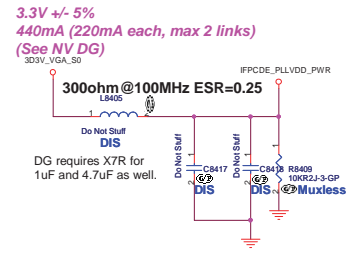
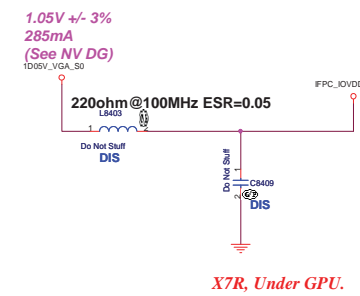
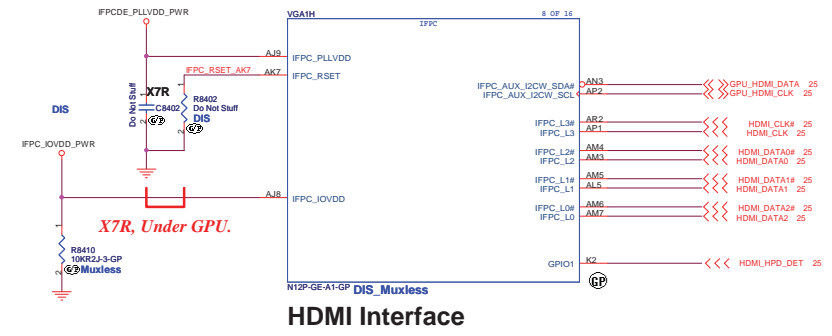
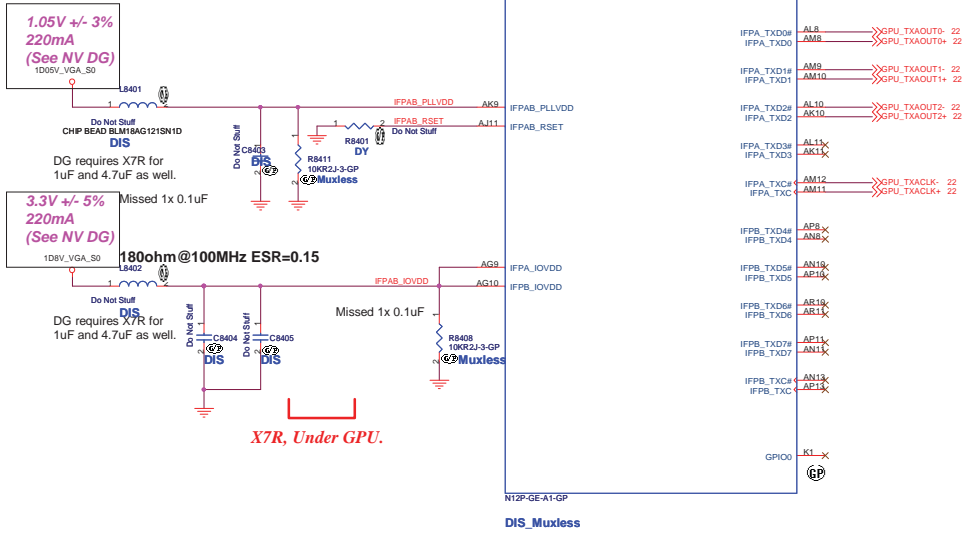
N12P GV : 71.0N12P.M10
N12P GS : 71.0N12P.EOU

DIS_Muxless_N12P:71.0N12P.M10_N12GS:71.0N12P.EOU

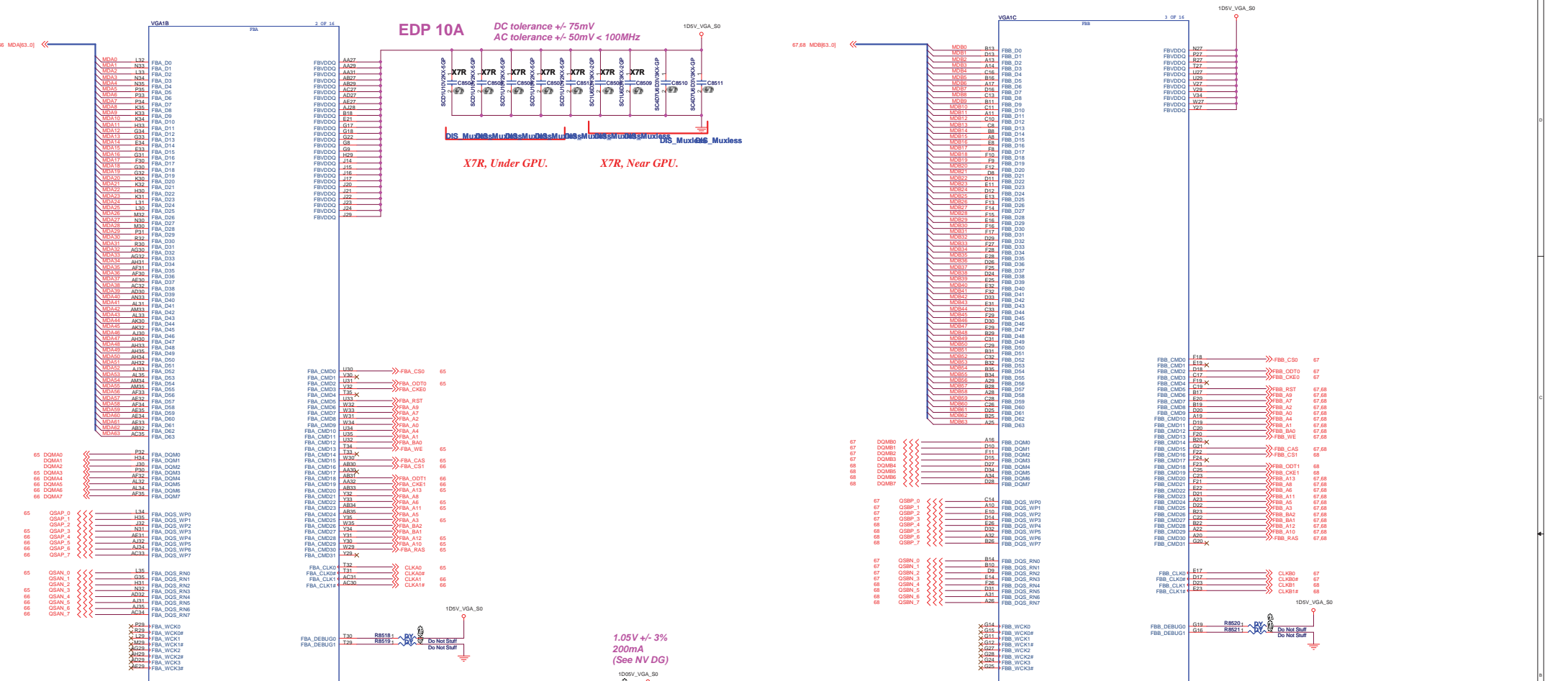
N12P GV : Dummy R8359,R8356,R8358,R8360
N12P GS : Mount R 8359,R8356,R8358,R8360

<http://hobi-elektronika.net>

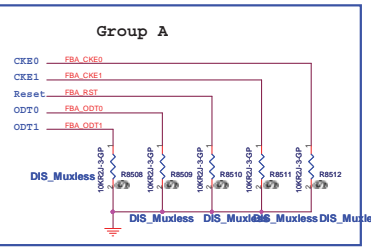
LVDS Interface



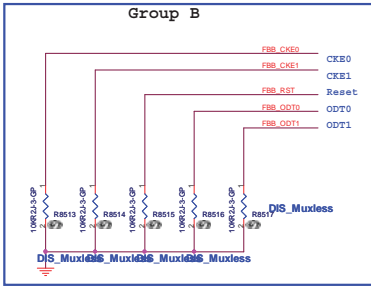
<http://hobi-elektronika.net>



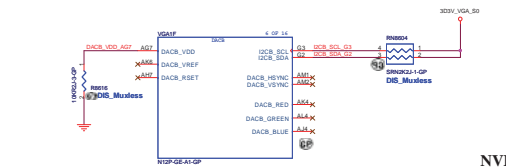
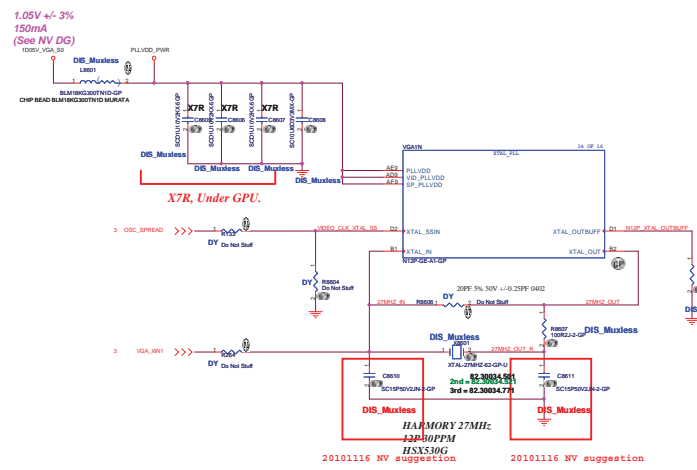
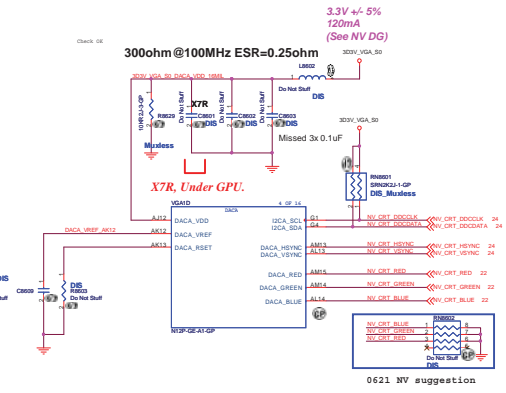
FBCLK Termination place on VRAM side



FBCLK Termination place on VRAM side



VGA Thermal sensor 787



Configuration	Vendor	Straps	Manufacturer Part Number	Speed Bin (MHz)
64Mx16 DDR3	Hynix	bx2	H5T1G63CFR-11C	900/800
	Samsung	bx3	K4W1G1646E-HC11	900
	Samsung	FB0	K4W1G1646E-BC11	900/800
	Hynix	bx0	H5T1G63CFR-12C	800
	Samsung	bx1	K4W1G1646E-HC12	900

NVIDIA TABLE

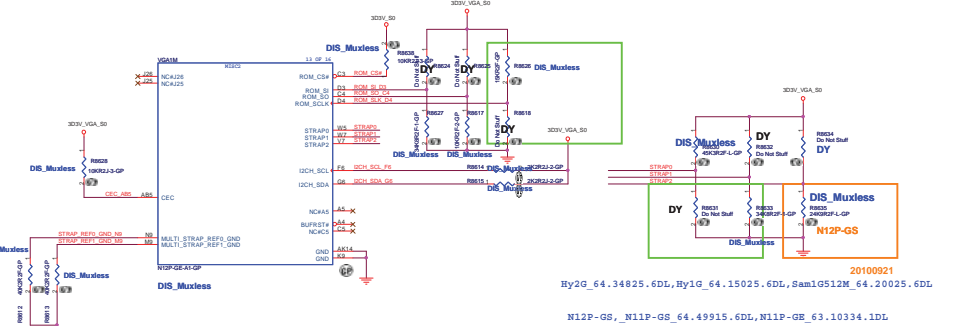
	Hynix 2G 0010 128*16*8	Hynix 1G 0010 64*16*8 800MHZ	Samsung 1G 0011 64*16*8 800MHZ	Samsung 512 0011 64*16*4 800MHZ	Samsung 2G 0111 128*16*8 800MHZ
RO_M_SIPD R8627	34.8Kohm	15Kohm	20Kohm	20Kohm	45Kohm
	64.34825.6DL	64.15025.6DL	64.20025.6DL	64.20025.6DL	64.45325.6DL

```

GPU_ROM_S1  for 10bit for 20bit for 10bit for 20bit
             Hynix VRAM Samsung VRAM Samsung VRAM Samsung VRAM
             RAM_CPG[0]=0 RAM_CPG[0]=0 RAM_CPG[0]=1 RAM_CPG[0]=1
             RAM_CPG[1]=1 RAM_CPG[1]=1 RAM_CPG[1]=1 RAM_CPG[1]=1
             RAM_CPG[2]=0 RAM_CPG[2]=0 RAM_CPG[2]=0 RAM_CPG[2]=0
             RAM_CPG[3]=0 RAM_CPG[3]=0 RAM_CPG[3]=0 RAM_CPG[3]=0

GPU_ROM_S0  VGA_DEVICE =1 (low bit)
             FB_0_SIZE =0
             SCL_417 =0 (High bit)

GPU_ROM_SCLK PEK_PLL_SW_TERN =0
              SLOT_CLK_CFG =1
              FB_TERN =0
              FCF_DRIVES[4] =-1 N11P Fermi Q1
    
```



Hy2G 64.34825.6DL, Hy1G 64.15025.6DL, Sam1G512M 64.20025.6DL
 N12P-GS, N11P-GS 64.49915.6DL, N11P-GE 63.10334.1DL

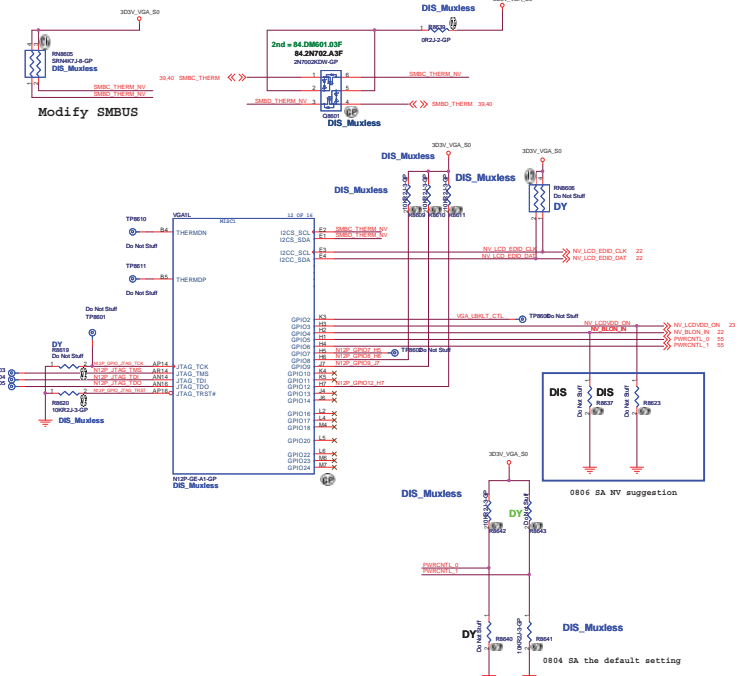


TABLE NVIDIA

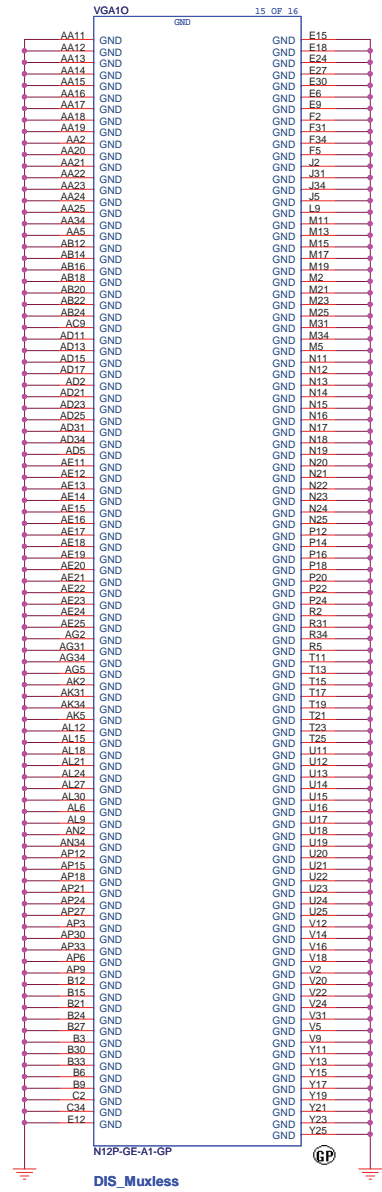
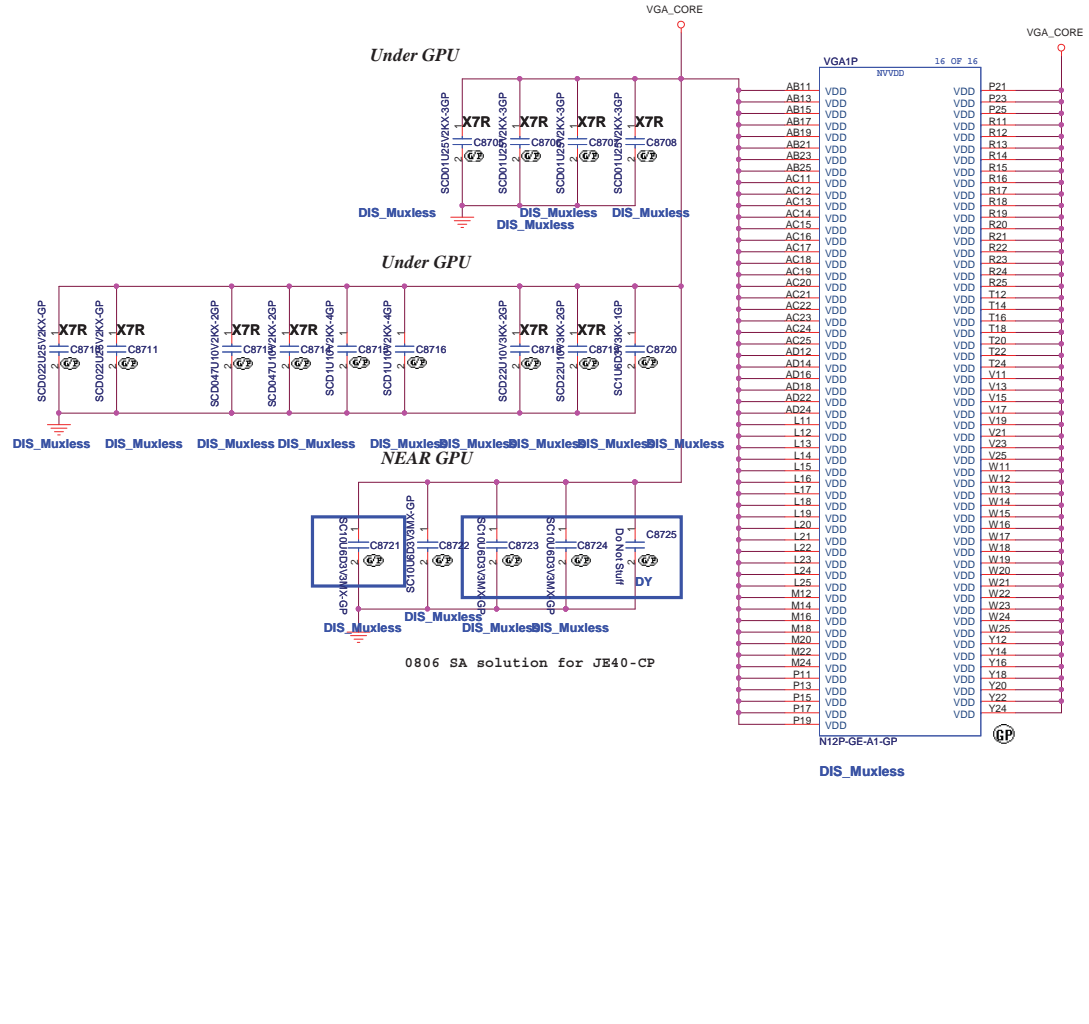
	71.0N12P.EU0	71.0N12P.A00			
	N12P-GS DEV ID: 0x0DF4	N12P-GV DEV ID: 0x0DF7	N11P-GE Fermi DEV ID: 0x0DF1 (0001)	N11P-GS Fermi DEV ID: 0x0DF0 (0000)	N12P-GV DEV ID: 0x0DF5 (0101)
STRAP2 PU R8634	25Kohm 64.24925.6DL	45Kohm 64.45325.6DL	10Kohm 63.10334.1DL	5Kohm 64.49915.6DL	30Kohm 64.30025.6DL

STRAP0 USER[0]=1 USER[1]=4 USER[2]=1 USER[3]=1
 N12P-GS USE 1111 (45K) N12P-GV N11P-GE Pull Low N11P-GS Pull Low N12P-GE

STRAP1 3GIO_PADCFG[0]=0 3GIO_PADCFG[1]=1 3GIO_PADCFG[2]=1 3GIO_PADCFG[3]=1
 N12P-GS USE 0110 (35K)

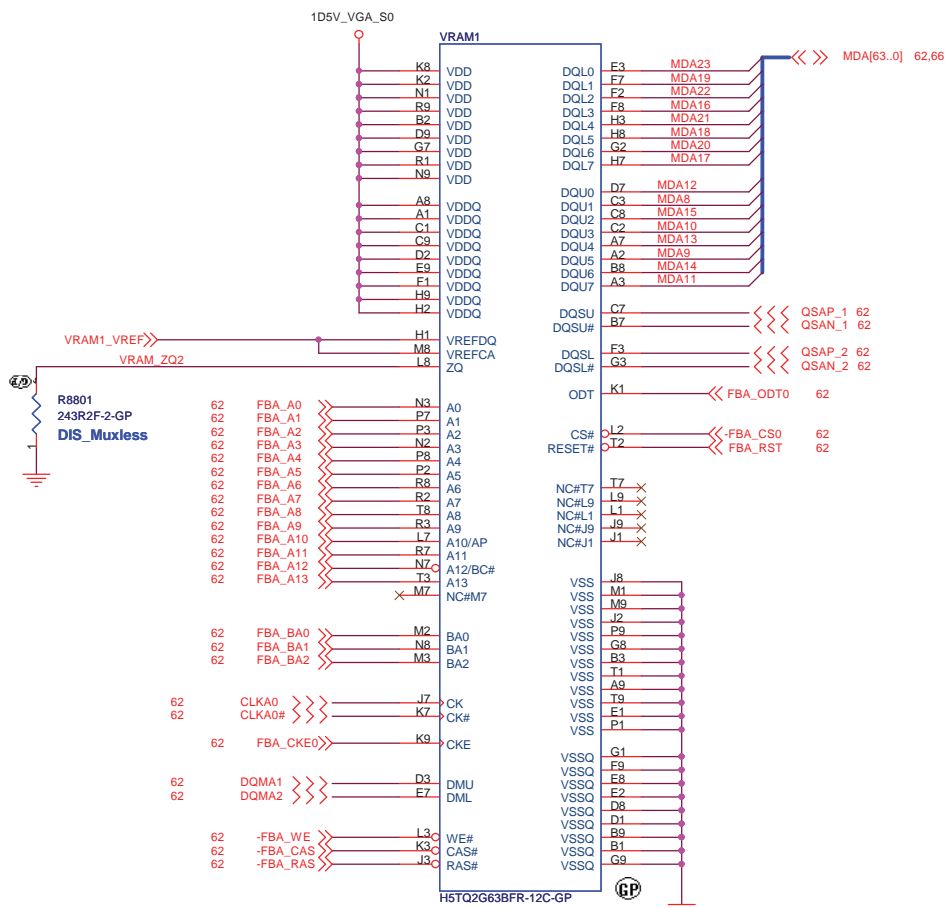
STRAP2 PCI_DRVID[0]=1 N12P-GS GP108-730-A1 0x0DF4 (0X4) (0100)
 PCI_DRVID[1]=0 N12P-GV GP108-705-A1 0x0DF7 (0X7) (0111)
 PCI_DRVID[2]=0 N11P-GE Fermi 0x0DF0 (0000)
 PCI_DRVID[3]=0 N11P-GE Fermi 0x0DF1 (0001)

EDP 50A (TDP 37W)



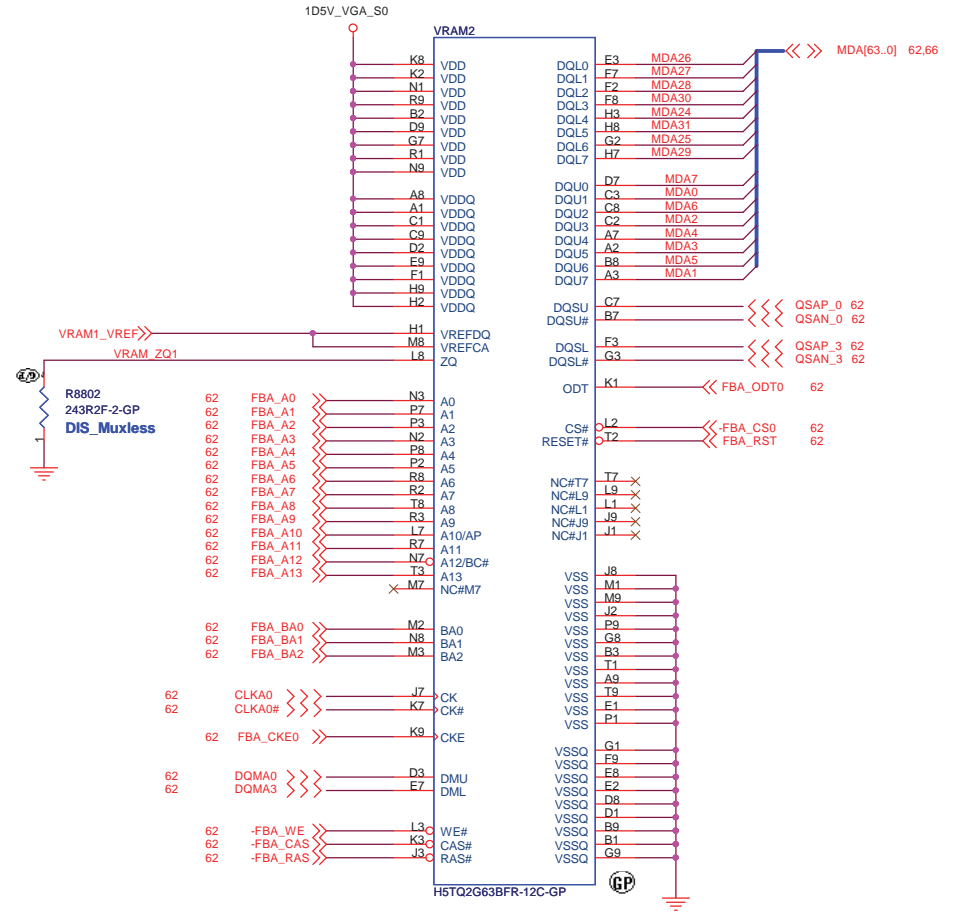
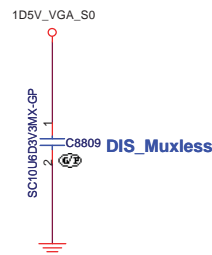
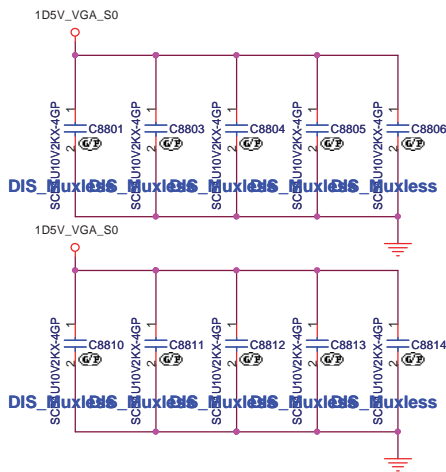
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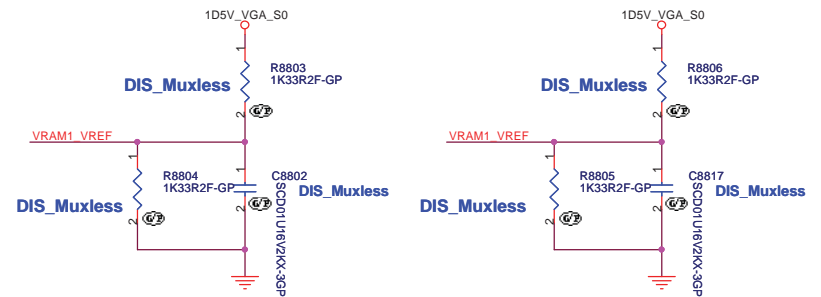


DIS_Muxless

Hy2GX8_VR.2GB0G.001,Sam1GX8_VR.1GB0B.006,,Hy1GX4_VR.1GB0G.004,Sam512X4_VR.1GB0B.006



DIS_Muxless

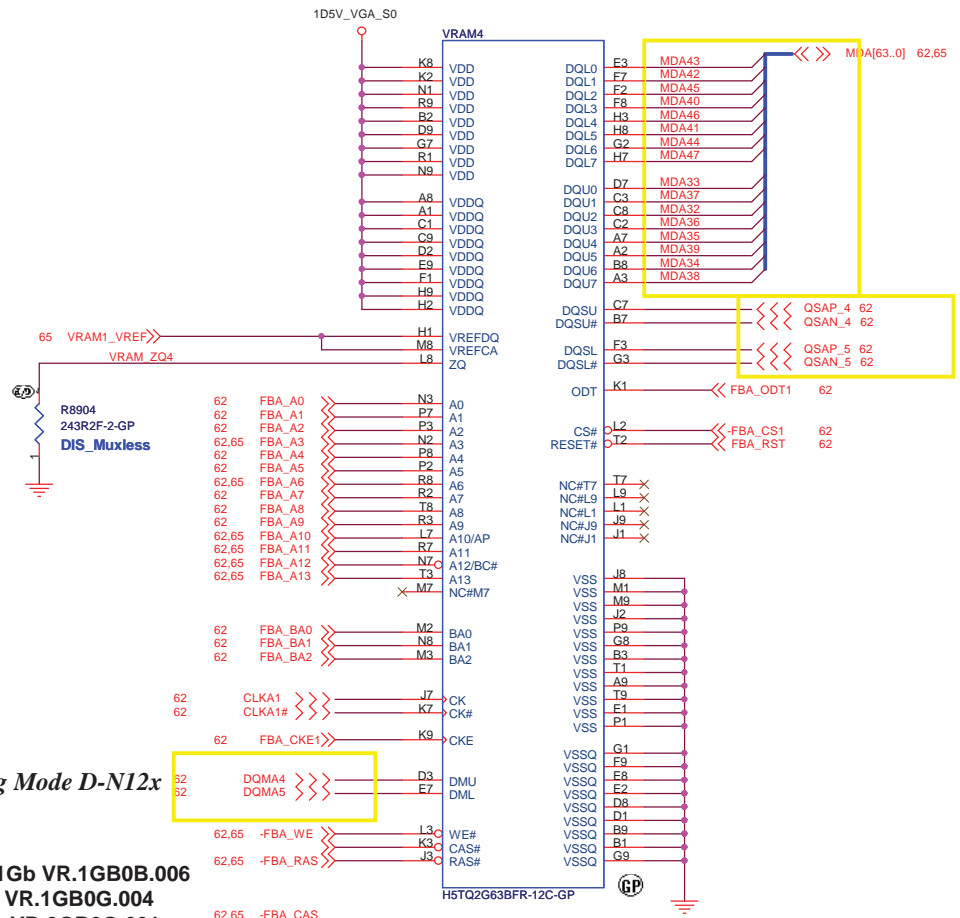
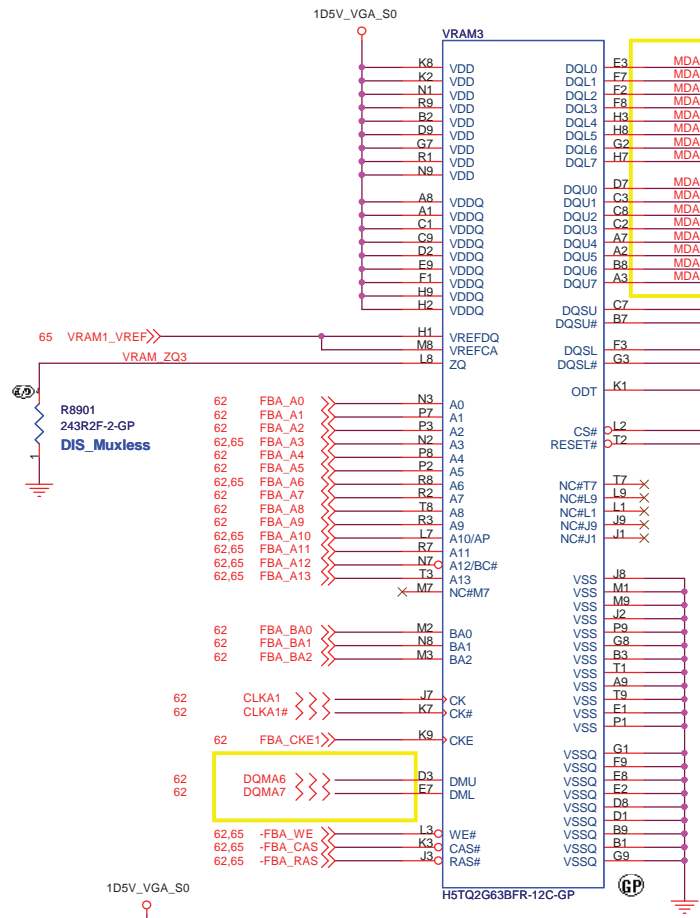


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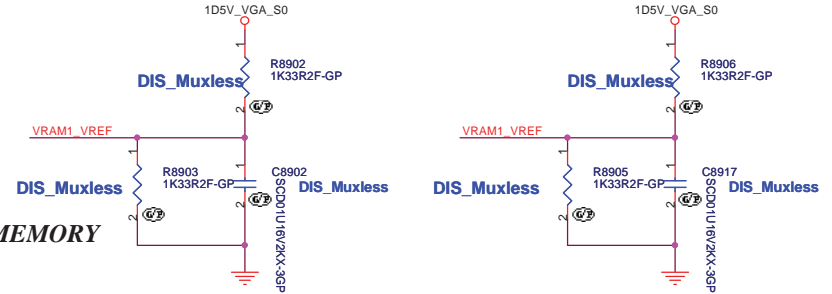
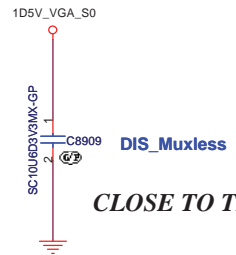
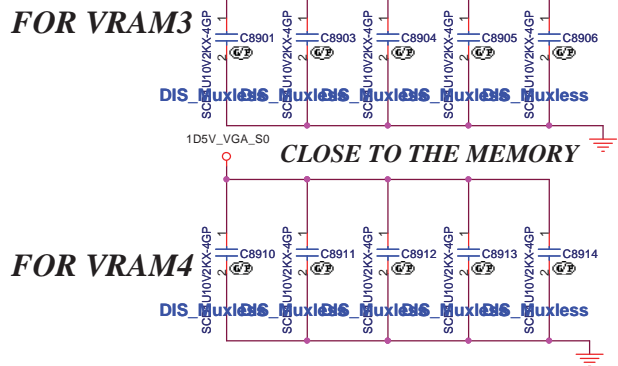
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FB CMD mapping Mode D-N12x

- VRAM SAMSUNG 1Gb VR.1GB0B.006
- VRAM HYNIX 1Gb VR.1GB0G.004
- VRAM HYNIX 2Gb VR.2GB0G.001

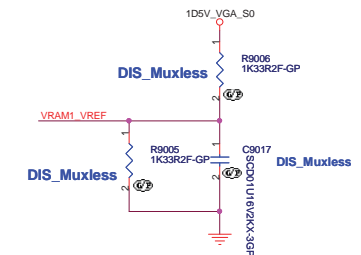
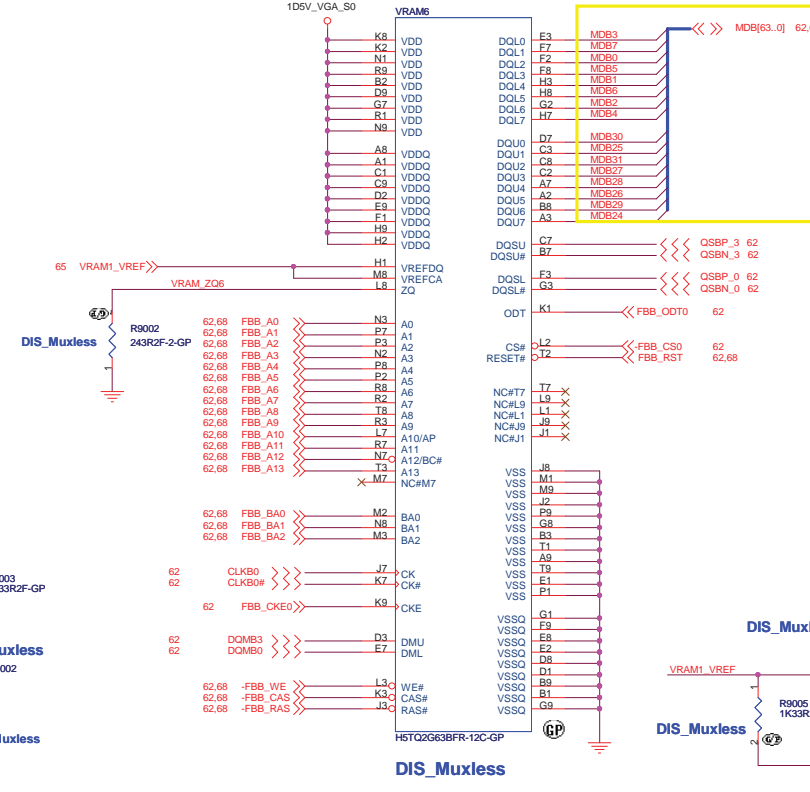
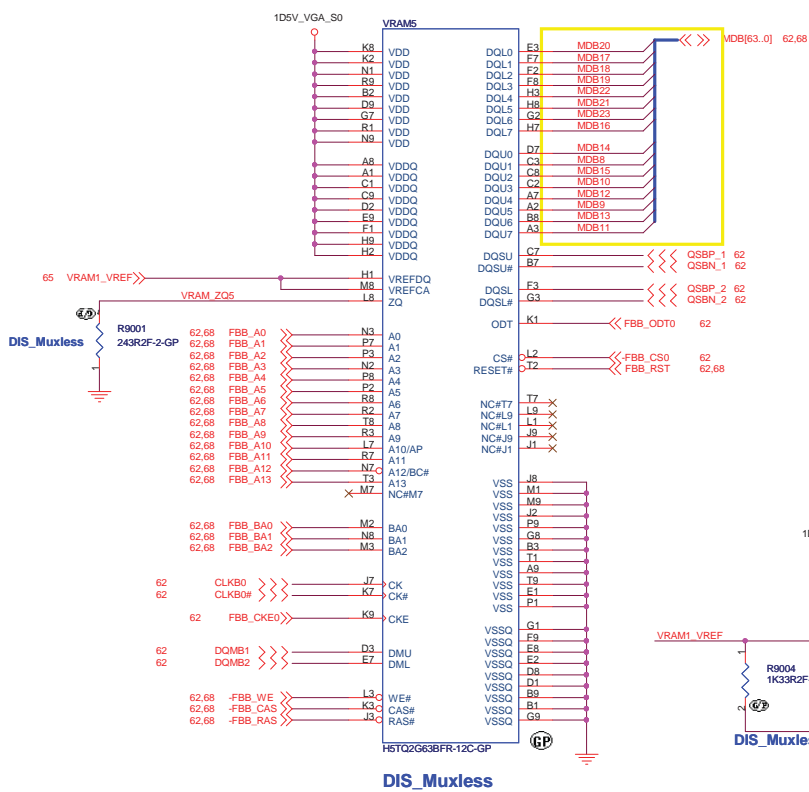


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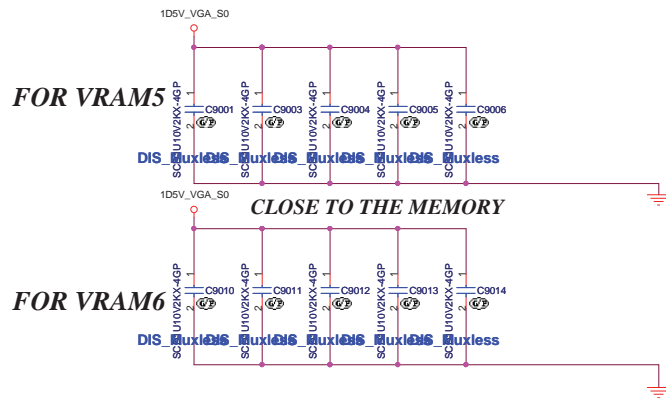
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Title: **GPU-VRAM3,4 (2/4)**

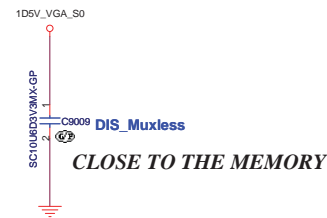
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VRAM SAMSUNG 1Gb VR.1GB0B.006
 VRAM HYNIX 1Gb VR.1GB0G.004
 VRAM HYNIX 2Gb VR.2GB0G.001



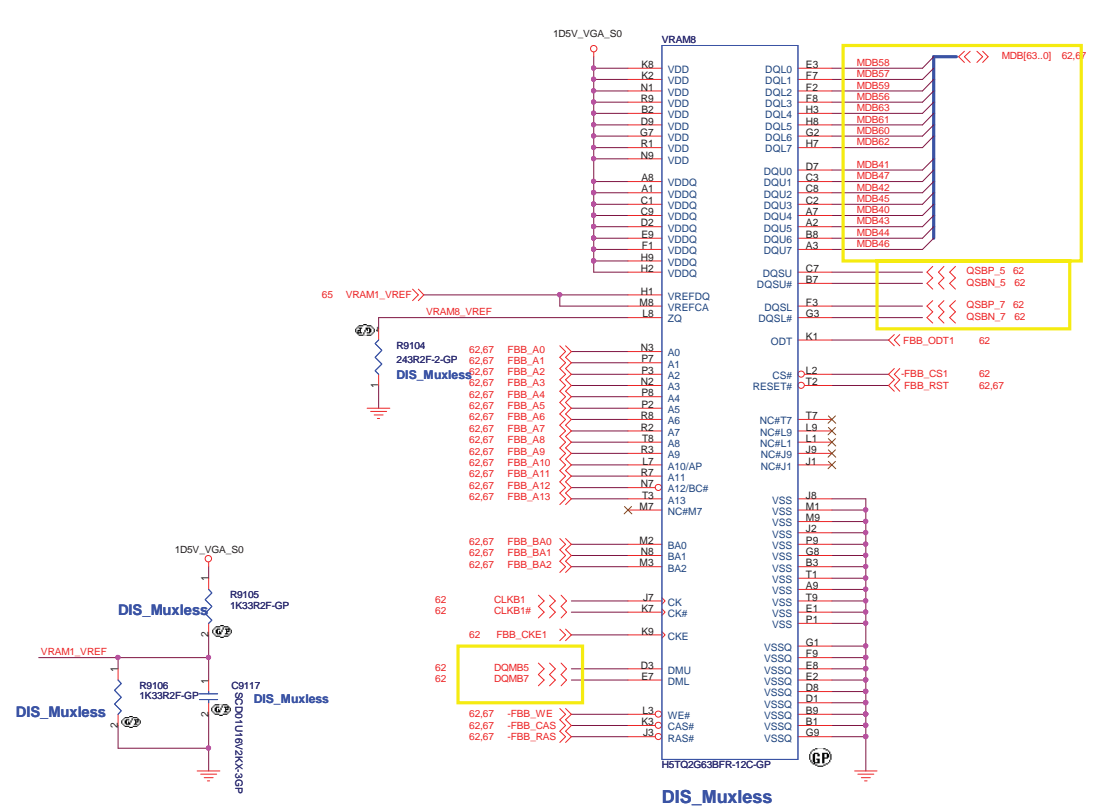
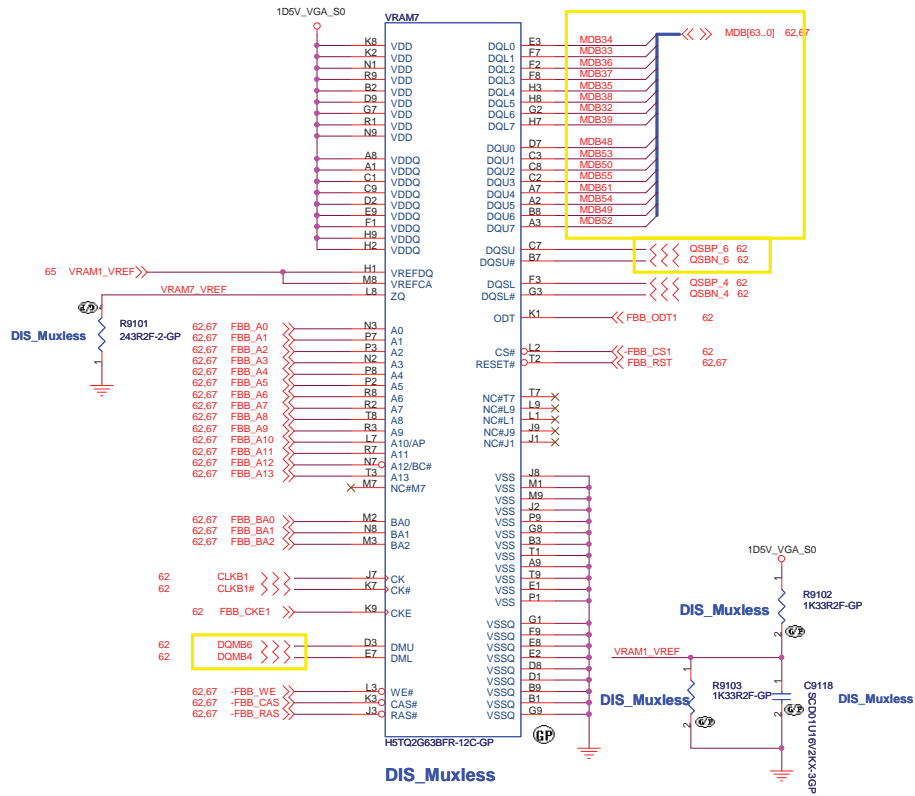
DG requires 4x0.1uF and 8x1.0uF per VRAM chip



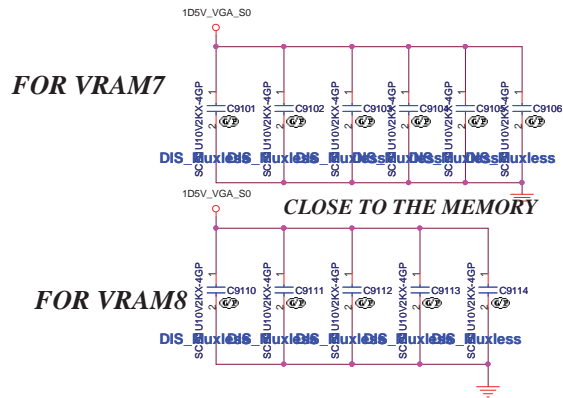
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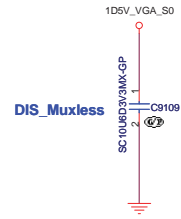
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VRAM SAMSUNG 1Gb VR.1GB0B.006
 VRAM HYNIX 1Gb VR.1GB0G.004
 VRAM HYNIX 2Gb VR.2GB0G.001



CLOSE TO THE MEMORY



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File: **GPU-VRAM7,8 (4/4)**

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Title Modify History		
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