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smart positioning


Rev. 1.3

# Data Sheet

## Fastrax UC430

This document describes the electrical connectivity and functionality of the Fastrax UC430 OEM GPS Receiver.

October 12, 2011

Fastrax Ltd

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## REFERENCES


| Ref. # | Publisher; Reference |
|---|---|
| (1) | CSR; SiRFstar IV Brochure |
| (2) | CSR; NMEA Reference Manual (CS-129435-MA-2).pdf |
| (3) | CSR; GSD4e OSP Manual (CS-129291-DC-9).pdf |
| (4) | National; AN-452.pdf (Microwire Serial Interface) |
| (5) | NXP; 39340011.pdf (The I2C-Bus Specification) |
| (6) | Fastrax; Jamming_mitigation.pdf |
| (7) | Fastrax; Reflow_soldering_ profile.pdf |
| (8) | Fastrax; Self Assistance and CGEE Data Storage to Host.pdf |
| (9) | Fastrax; SiRF_IV_blocking.pdf |
| (10) | Fastrax; SiRFIV_low_power_modes.pdf |
| | |

## CHANGE LOG

| Rev. | Notes | Date |
|---|---|---|
| 1.0 | Initial document, draft status | 2011-04-05 |
| 1.1 | Updated reference circuit diagrams due to ECLK GPIO3 function Message_Waiting output in SPI or UART handshaking configurations; modified some details in text for publishing; operation describes firmware 4.1.0 aka ROM2.0 device. | 2011-05-25 |
| 1.2 | Ground plane opening under embedded antenna increased to 4.8x7.2mm; increased embedded antenna radiation efficiency to 80%; added notes on future ROM firmware support for new external MEMS sensors; added note on enabling 5Hz fix rate; added notes on autonomous wakeup after power up; corrected and added referenced document numbers. | 2011-07-04 |
| 1.3 | Harmonized document with IT430 operation; updated General spec; removed DR support for gyro & barometer; removed APM low power mode; added notes on host SPI polling after hibernate; added notes on PPS; added T&R spec: updated RFIN ESD spec | 2011-10-12 |
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# 1 Contents

# 2 Overview

## 2.1 General

The Fastrax UC430 is an OEM GPS receiver module with embedded GPS antenna and which provides the SiRFstar IV receiver, ref (1) functionality using the state of the art SiRF GSD4e chip (ROM variant). The module has ultra small form factor 9.6 x 14.0 mm, height is 1.95 mm nominal (2.25 mm max) and can be assembled with SMT reflow soldering. The Fastrax UC430 receiver provides low power and very fast TTFF together with weak signal acquisition and tracking capability to meet even the most stringent performance expectations.

The module provides complete signal processing from antenna input to host port in either NMEA messages or in SiRF OSP binary protocol. The module requires a single power supply VDD +1.8V. The host port is configurable to UART, SPI or I2C during power up. Host data and I/O signal levels are 1.8V CMOS compatible, inputs are 3.6V tolerable.

The embedded GPS antenna provides good radiation efficiency (80% typ. @ 80x40mm ground plane), linear polarization and radiation pattern optimized for portable devices. The UC430 module supports also optional connectivity for external antenna signal (e.g. connector for an external GPS active antenna) with only a few external components. The antenna is insensitive to surroundings and has high tolerance against frequency shifts that result to fast time to market.

The SiRFstar IV provides a new feature called SiRFAware (also referenced as Micro Power Management mode), which enables fast TTFF for Snap start mode while consuming only 125 uA average current (typ.) in autonomous Hibernate state. The receiver does wakeup autonomously to calibrate internal GPS time and to collect ephemeris data while maintaining 1 sec Snap fix capability. The module has support and connectivity to optional external sensors for Dead Reckoning like 3-D Accelerometer and 3-D Compass on dedicated DR_I2C bus for Stationery Detection that aids navigation when receiver does not move during weak signal conditions like indoors.

The receiver is also optionally self-assisted since the Client Generated Extended Ephemeris (CGEE for 3 days) calculation is embedded in the software without any resources required from the host. The CGEE data is stored on external serial EEPROM memory on the dedicated DR_I2C bus (can be optionally transferred to/from host).

The SiRFstar IV contains also a CW Jammer Remover, which will track and remove up to 8 CW (Carrier Wave) type signals up to 80dBHz (equals to -90 dBm typ.) signal level.

This document describes the electrical connectivity and main functionality of the Fastrax UC430 OEM GPS Receiver module.

## 2.2 Block diagram

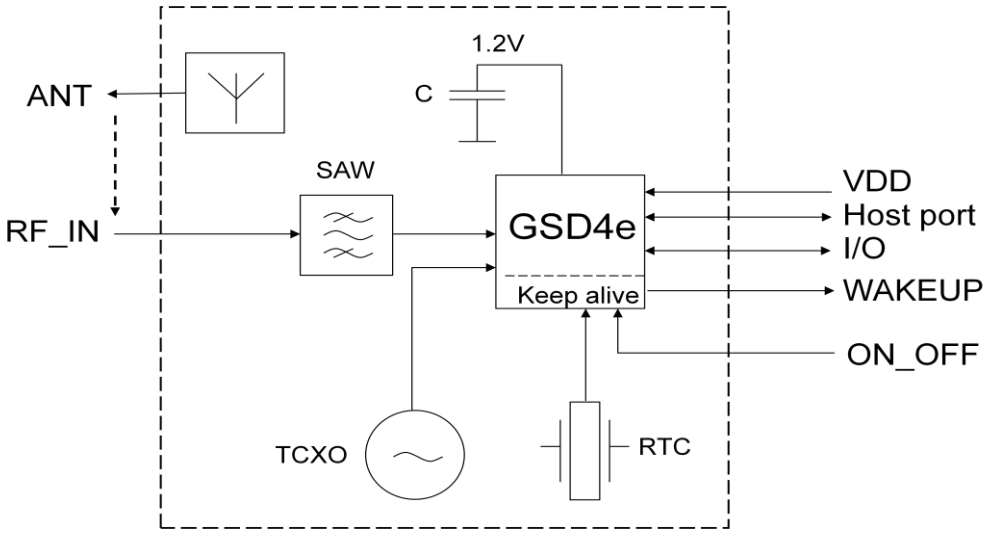



**Figure 1 Block diagram**

## 2.3 Frequency Plan

Clock frequencies generated internally in the Fastrax UC430 receiver:

- 32768 Hz real time clock (RTC)
- 16.369 MHz master clock (TCXO or crystal)
- 3142.96 MHz local oscillator of the RF down-converter

## 2.4 General Specifications

**Table 1 General specifications**

| | |
|---|---|
| Receiver | GPS L1 C/A-code, SPS |
| Chip set | SiRF IV, GSD4e, ROM variant |
| Channels | 48 |
| Tracking sensitivity | -163 dBm typ. |
| Navigation sensitivity | -161 dBm typ. |
| Navigation sensitivity, re-acq. | -162 dBm typ. |
| Navigation sensitivity, cold acq. | -147 dBm typ. |
| Update rate (default) | 1 Hz (configurable to 5Hz with ROM2.0 firmware rev 4.1.0 and above) |
| Position accuracy *(note 1)* | 2.5 m (50%) typ. Horizontal<br>5 m (50%) typ. Vertical<br>0.01 m/s (50%) typ. Velocity |
| Max altitude/velocity | <60.000 ft/<1.000 knots |
| Time to First Fix, cold acq. | 35 s typ. (*note 1*) |
| Time to First Fix, warm acq. | 35 s typ. *(note 1)* |
| Supply voltage, VDD | +1.8 V +/- 5% |
| Power consumption *(note 2)* | 68 mW typ. @ VDD=1.8 V and Low power modes e.g. 10mW @ TricklePower 100ms/1Hz |
| Power consumption (Hibernate state) | 36 uW typ. @ 1.8 V |
| External RF amplifier net gain range at RF Input (RF_IN) | 0… +35 dB |
| Storage temperature | -40°C…+85°C |
| Operating temperature | -40°C…+85°C *(note 3)* |

| | |
|---|---|
| Host port configuration | SPI(default), UART or $I^2C$ configurable via pull up/down resistor |
| Host port protocol | NMEA-0183 rev. 3.0 (configurable to SiRF binary OSP protocol) |
| Serial data format (UART) | 8 bits, no parity, 1 stop bit |
| Serial data speed (UART) | 4800 baud (configurable) |
| TM output (PPS) | 200 ms high pulse, rising edge +/-1 µs @ full second GPS epoch |

*Note 1: With nominal GPS signal levels -130dBm.*

*Note 2: Module boots for internal 1.2V LDO regulator mode. Internal Switcher regulator mode is not supported with default Bill-of-Materials.*

*Note 3: Operation in the temperature range –40°C… –30°C is allowed but Time-to-First-Fix performance and tracking sensitivity may be degraded.*

# 3 Operation

## 3.1 Operating modes

After power up the UC430 module boots from the internal ROM to Hibernate state. The module operation requires ON_OFF interrupt to wake up for Normal (Navigation, Full on) mode. Modes of operation:

- Full on (Navigation, Full Power)
  - Power management system modes
- Hibernate state
- Reset state

## 3.2 Full on mode

The module will enter Hibernate state after first power up with factory configuration settings. The Navigation mode will start after waking up from Hibernate state in cold start mode by sending ON_OFF signal interrupt pulse from host. Power consumption will vary depending on the amount of satellite acquisitions and number of satellites in track. This mode is also referenced as *Full on, Full Power* or *Navigation* mode.

Navigation is available and any configuration settings are valid as long as the VDD power supply is active. When the VDD is powered off, settings are reset to factory configuration and receiver performs a cold start on next power up.

VDD supply is intended to be kept active all the time and when needed the navigation activity is suggested to be controlled to low quiescent *Hibernate* state via ON_OFF control input; see also chapter 4.7. Autonomous wakeup after power up from *Hibernate* state to full on mode can be enabled by connecting WAKEUP signal to ON_OFF signal.

Navigation fix rate can be increased to 5 Hz by OSP binary message ID 136, Position Calc Mode set to xxxx x1xx (bin), e.g. 0x04, ref (3). Note that baud rate must be set high enough or message payload low enough in order to pass through all messages pending. Enabling 5 Hz navigation will increase typical current drain about 2 mA.

### 3.2.1 Host port configuration

User can select the host port configuration between UART, SPI (slave) and $I^2C$ (master/slave) during power up boot or reset. The port selection is not intended to be changed dynamically but only set once at power up. Default host port is SPI and other host port configurations requires external pull down or pull up resistor at CTS_N and RTS_N signals, see chapter 4.3 for details.

Default protocol for host communication is NMEA 4800 baud, ref (2). Protocol is switchable to SiRF binary OSP (One Socket Protocol, ref (3) by NMEA protocol command $PSRF100.

Default NMEA message configuration: $GPGGA, $GPGSA and $GPRMC rate every second (in this order) and $GPGSV messages (can be 1… 4) every 5 seconds (sent after $GPGSA message). Also CGEE related $PSRF156 messages can be outputted at irregular interval. Message output and rate can be configured by NMEA message $PSRF103. $PSRF150 (OKtoSend) messages are also sent out when the receiver is ready to receive messages after wake up or when it is going into low-power mode and can't process input commands anymore.

### 3.2.2 Power management system modes

The UC430 module supports also SiRF operating modes for reduced average power consumption, ref (10) like Adaptive TricklePower™, Push-to-Fix™ and SiRFAware™ modes:

1. Adaptive TricklePower (ATP): In this mode the receiver stays at Full on power state for 200… 900ms and provides a valid fix. Between fixes with 1… 10 sec interval the receiver stays in Hibernate state. ATP mode

is configurable with SiRF binary protocol message ID151 (ref 3). The receiver stays once in a while in Full on power mode automatically (typ. every 1800 sec) to receive new ephemeris data from rising satellites or if received signal levels drop below certain level.

2. Push-to-Fix (PTF): In this mode the receiver is configured to wake up periodically, typically every 1800 sec (configurable range 10… 7200 sec), for position update and to collect new ephemeris data from rising satellites. Rest of the time the receiver stays in Hibernate state. When position update is needed, the host can wake up the receiver by ON_OFF control input interrupt (pulse low-high-low >90us after which the receiver performs either Snap or Hot start and a valid fix is available within 1… 8 seconds typ. This mode is configurable with SiRF binary protocol message ID151 & 167.

3. SiRFAware (aka Micro Power Management mode, MPM): In this mode the receiver is configured to wake up periodically for 18 sec, typically every 1800 sec, to collect new ephemeris data from rising satellites, and once in a while (rate depends on temperature change) for 250 ms to calibrate internal navigation state and GPS time estimate. Rest of the time the receiver stays in Hibernate state and module achieves 125 uA typ. average current drain. The host wakes up the receiver by ON_OFF control input interrupt (pulse low-high-low >90us) to Full on power mode after which the receiver performs Snap start and a valid fix is available within 1 second typ. After valid fix, operation can return back to Micro Power Management mode by re-sending the configuration binary message from host. This mode is configurable with SiRF OSP (One Socket Protocol) binary protocol message MID218 and it requires that fix is valid prior entering the mode.

These power management modes are also configurable with SiRF OSP binary protocol message MID 218, Power Mode Request. Note that position accuracy can be somewhat degraded in power management modes when compared to full power operation.

### 3.2.3 Updates in ROM firmware

The firmware in the internal ROM memory is expected to be updated from time to time. A firmware update may add new firmware features and may add support e.g. to new Dead Reckoning sensors. New firmware will also affect the need for possible patch code handling. Initial samples will have firmware revision 4.0.4 aka ROM1.3; production volumes will start to use rev. 4.1.0 aka ROM2.0 devices.

As the availability of previous ROM firmware revisions can't be guaranteed, it is important that any host control operation, including e.g. possible patch code download, is flexible and allows UC430 ROM firmware to be updated. This requires that any patch code stored at host or at external EEPROM can be either omitted or updated at later stages in order to match with future UC430 ROM firmware revisions.

Any new ROM firmware revision will also issue a new module revision due to Bill-of-Materials (type code) of the UC430 module since the silicon order code and firmware revision will change accordingly. Customers are advised to follow up Fastrax Change Notices on UC430 ROM firmware updates.

### 3.2.4 Patching ROM firmware

The firmware that is associated with UC430 is executed for internal ROM memory. It is a normal practice that firmware patches may be provided from time to time in order to address ROM firmware issues as a method of implementing bug fixes. Patch firmware (max. size 24 kB) and downloading tools are available via Fastrax support.

Patch is stored by default on external EEPROM at DR_$I^2C$ bus or at host. Note that power down will clear internal patch RAM (and thus also patch) but patch is automatically re-issued from external EEPROM after next power up.

The usage of external EEPROM allows also custom made patch code (CCK, Customer Configuration Kit) tailored for any specific configuration need like baud rate, protocol, I/O configuration etc.; contact Fastrax support for details on CCK.

### 3.2.5 Self-Assistance – Client Generated EE usage

The UC430 module supports Client Generated Extended Ephemeris (CGEE), which allows fast TTFF 10 sec typ. for 3 days. The CGEE data is generated internally from satellite ephemeris as a background task and thus host should allow the UC430 to navigate a few minutes and to collect ephemeris from as many satellites as possible before entering Hibernate state.

The CGEE feature is enabled by default when an external EEPROM is connected to DR_$I^2C$ bus for CGEE data storage; see chapter 4.11. The operation requires that power supply is kept active all the time for fastest TTFF; control navigation activity by the host via the ON_OFF control input. The CGEE data storage can be controlled by NMEA message $PSRF120 or OSP binary message ID 232, Sub ID 253.

The CGEE data can be also stored optionally to host; contact Fastrax support for availability and details, ref (8).

### 3.2.6 Almanac Based Positioning

User can enable so called Almanac Based Positioning (ABP, see NMEA command $PSRF103 or OSP command ID 136), which allows fast cold starts TTFF 22 sec typ. since broadcast ephemeris data is not need from visible satellites but the factory set (or broadcast or pushed) Almanac data is used for positioning. When broadcast ephemeris data gets available from visible satellites, the navigation will use automatically more precise ephemeris data for positioning. When ABP is enabled, the navigation message (e.g. NMEA $GPRMC) will indicate when ABP positioning is being used in navigation ($GPRMC: Mode=R).

The positioning accuracy is in the order of few hundred meters to kilometers and is usable mainly to coarse positioning (e.g. to find out in which country/state/district the receiver is located). Position accuracy is also expected to degenerate when actual Ephemeris/Almanac starts to differ from the factory set Almanac data in power down/on cycles. Host may try to overcome this problem by either keeping the power supply active all the time using Hibernate or by polling latest broadcast Almanac from the module (by OSP Message ID 146) prior power down and then pushing the Almanac back to module (by OSP Message ID 130) at next power up after waking up from Hibernate state. Note the Almanac data broadcast takes 12.5 minutes and thus allow the module to navigate in Full on mode at least for this period.

### 3.2.7 5 Hz Navigation

User can enable 5 Hz navigation rate by NMEA or binary command (ROM2.0 onwards). Prior changing the navigation rate from 1 Hz to 5 Hz suggestion is to increase host baud rate high enough, from 4800 baud to at least 5x by NMEA command $PSRF100, e.g. 38400 baud minimum in order to enable 5 times more message throughput.

NMEA command for 5 Hz navigation is $PSRF103,00,6,00,0*23. And 1Hz navigation can be restored by command $PSRF103,00,7,00,0*22. In OSP binary protocol the command is MID 136, Position Calc Mode set to 0x04.

## 3.3 Hibernate state

Hibernate state means a low quiescent (20uA typ.) power state where only the internal I/O Keep Alive, non-volatile RTC, patch RAM and backup RAM block is powered on. Other internal blocks like digital baseband and RF are internally powered off. The main supply input VDD shall be kept active all the time, even during Hibernate state. Waking up from and entering in to Hibernate state is controlled by host interrupt at ON_OFF control input (rising edge toggle low-high-low >90us).

During Hibernate state the I/O Keep Alive is still active, thus I/O signals keep respective states except TX and RX signals, which are configured to high input impedance state.

The receiver wakes up from Hibernate state on the next ON_OFF interrupt (at rising edge) using all internal aiding like GPS time, Ephemeris, Last Position etc. resulting to a fastest possible TTFF in either Hot or Warm start modes.

## 3.4 Reset state

Reset state is entered internally after power up until the internal RTC clock wakes up after which internal reset state is relaxed and module boots to Hibernate state. Host can override reset state via RESET_N input, low state active. Normally external reset override is not required but if power shall be removed abruptly see chapter 4.2 for reset suggestion.

Note that reset clears data RAM content, e.g. downloaded ROM patch code. User can overcome this problem by using patch storage to external EEPROM and thus the module is able to re-issue patch code header back to internal patch RAM after waking up from successive Hibernate state. Backup RAM content is not cleared and thus fast TTFF is possible after reset and system configuration settings are sustained.

# 4 Connectivity

## 4.1 Pad Assignments

The I/O signals are available as soldering (castellated) pads on the bottom side of the module. These pads are also used to attach the module on the motherboard. All digital I/O signal levels are 1.8V CMOS compatible and inputs are 3.6V tolerable. All unconnected I/O signals can be left unconnected when not used, unless instructed to use external pull up/down resistor.

**Table 2 Pad assignment**

| Contact | Signal | I/O type Full on | I/O type Hibernate | I/O type Reset | Signal description |
|---|---|---|---|---|---|
| 1 | EIT | S,C,B | S,C,B | HZ | - GPIO4<br>- External interrupt input signal, disabled by default. Provides an interrupt on either high or low logic level. *Connect to GND when not used.* |
| 2 | EIT2 | S,C,B | S,C,B | HZ | - GPIO8<br>- EIT2 external interrupt input #2, disabled by default. Provides an interrupt on either high or low logic level or edge-sensitive interrupt. *Connect to GND when not used.* |
| 3 | ECLK | S,C,B | S,C,B | HZ | - GPIO3<br>- Message_Waiting output when in SPI or UART handshaking host port configurations<br>- Reserved for ECLK clock input for frequency aiding applications, disabled by default. *Leave open or pull down when not used.* |
| 4 | GND | G | G | G | Ground |
| 5 | GND | G | G | G | Ground |
| 6 | TSYNC | S,C,B | S,C,B | HZ | - GPIO2<br>- Reserved for TSYNC that is the time transfer strobe input used in A-GPS precise time aiding *Connect to GND when not used.* |
| 7 | DR_I2C_CLK | S,C,B | S,C,B | HZ | - GPIO1<br>- Dead reckoning I²C host bus clock (SCL). Use external pull up resistor when bus is used. *Connect to GND or pull up when not used.* |
| 8 | DR_I2C_DIO | S,C,B | S,C,B | HZ | - GPIO0<br>-Dead reckoning $I^2C$ host bus data (SDA). Use external pull up resistor when bus is used. *Connect to GND or pull up when not used.* |
| 9 | VDD | P,I | P,I | P,I | Power supply input +1.8V nom. *De-couple externally with e.g. 4.7uF low ESR ceramic capacitor.* |
| 10 | GND | G | G | G | Ground |
| 11 | GND | G | G | G | Ground |
| 12 | GND | G | G | G | Ground |
| 13 | GND | G | G | G | Ground |
| 14 | GND | G | G | G | Ground |
| 15 | GND | G | G | G | Ground |
| 16 | ANT | A,O | A,O | A,O | Antenna signal output (50 ohm), max DC voltage 0V |
| 17 | RF_IN | A,I | A,I | A,I | Antenna signal input (50 ohm), max DC voltage |

| Contact | Signal | I/O type Full on | I/O type Hibernate | I/O type Reset | Signal description |
|---|---|---|---|---|---|
| | | | | | 0V |
| 18 | GND | G | G | G | Ground |
| 19 | GND | G | G | G | Ground |
| 20 | CTS_N | S,C,B, PD(a) | S,C,B, PD | HZ | - GPIO6<br>- SPI_CLK slave SPI clock input (CLK)<br>-UART_CTS_N UART Clear to Send (CTS), active low<br>- Host port boot strap, see 4.3<br>*Pull up externally for UART.* |
| 21 | GND | G | G | G | Ground |
| 22 | GND | G | G | G | Ground |
| 23 | RESET_N | C,I,PU | C,I,PU | C,I,PU | External reset input, active low. *Can be left unconnected when not used.* |
| 24 | RTS_N | S,C,B, PU(a) | S,C,B, PU | HZ | - GPIO7<br>- SPI_SS_N slave SPI chip select (CS#), active low<br>- UART_RTS_N UART Request to Send (RTS), active low<br>- Host port boot strap, see 4.3<br>*Can be left unconnected when not used.* |
| 25 | TX | S,C,B | S,C,B | HZ | - SPI_DO slave SPI data output (MISO)<br>- UART_TX UART data transmit (TX)<br>- I2C_CLK I²C bus clock (SCL) |
| 26 | RX | S,C,B | S,C,B | HZ | - SPI_DI slave SPI data input (MOSI)<br>-UART_RX UART data receive (RX). *Must be driven by host or use external pull up resistor (UART RX).*<br>- I2C_DIO I²C bus data (SDA) |
| 27 | GND | G | G | G | Ground |
| 28 | ON_OFF | S,C,B | S,C,B | S,C,B | Power control input used to command the module On (Navigation) or Off (Hibernate). *Must be driven by the host or connected to WAKEUP.* |
| 29 | TM | S,C,B | S,C,B | HZ | - GPIO5<br>- Time mark output signal *(default 1PPS)*<br>- Optionally GPS_ON, power control output signal for e.g. external LNA bias control.<br>- Optionally RTC_CLK, buffered RTC clock output.<br>*Can be left unconnected when not used.* |
| 30 | WAKEUP | C,O | C,O | C,O | Wakeup output for control of external regulator, e.g. battery to 1.8V for the VDD supply input when full power mode is entered. Can be used also externally for active antenna bias control, active high = high current/bias on. *Can be left unconnected when not used.* |
| 31 | GND | G | G | G | Ground |

*Note (a): Pull Up/down resistor present only shortly after power up.*

*Legend: A=Analogue, B=Bidirectional, C=CMOS, G=Ground, HZ=High Impedance, I=Input, O=Output, P=Power, PU=Internal Pullup 86 kohm typ., PD=Internal Pulldown 91 kohm typ., S=Schmitt Trigger (when Input). Note that with Birectional I/O the firmware has control for input vs. output I/O type depending on the firmware function.*

## 4.2 Power supply

The UC430 module requires only one power supply VDD. Keep the supply active all the time in order to keep the non-volatile RTC & RAM active for fastest possible TTFF.

VDD supply intended to be kept alive all the time. First power up may take 300ms typ. due to internal RTC startup time (may increase up to 5 seconds at cold temperature) after which the module will enter to Hibernate state. The host may try wakeup the module via successive ON_OFF interrupts sent every second until the host port messages are outputted and/or WAKEUP output is at high state.

When power supply is intended to be removed, it is suggested that prior power removal a serial message in binary (MID 205) or NMEA format ($PSRF117,16*0B<CR><LF>) is sent to module to shut down firmware operations orderly. Otherwise e.g. external EEPROM may get corrupted if power down happens in the middle of EEPROM writing, which may increase in TTFF. If external EEPROM is also used for ROM patch code, the abrupt power removal may cause patch code corruption that may end to system failure.

Second option for orderly shutdown is to send ON_OFF interrupt prior VDD removal. Operations shutdown may take anything between 10 to 900 ms depending upon operation in progress and messages pending and hence is dependent upon serial interface speed and host port type.

If it is likely that VDD supply will be removed abruptly, suggestion is to add external voltage monitor to detect under voltage condition below 5% nominal supply voltage and to drive RESET_N signal to reset condition (low state). This important especially when external EEPROM or data storage at host is used. VDD supply off-time is suggested to be over 10 seconds to next power up in order to clear all internal backup RAM content and to minimize risk for wrong backup data.

Main power supply VDD current varies according to the processor load and satellite acquisition. Typical VDD peak current is 56 mA (typ.) during waking for Full on power up (short peaks can be up to 90mA). Typical VDD current in low power Hibernate state is 20uA. The external power supply can be using dual low/high current modes, which can be controlled via the WAKEUP output signal (high current = WAKEUP high) as indication when full power is required by the module. The external power supply should be able to provide full current to VDD within 9 ms after WAKEUP low-to-high transition.

The internal 1.2V regulator is powered from VDD supply and it boots for LDO mode. The internal 1.2V power supply includes also Switcher mode regulator, which is not supported in UC430 (no switcher coil).

By-pass the VDD supply input by a low ESR ceramic de-coupling capacitor (e.g. 4.7 uF) placed nearby VDD pin to ensure low ripple voltage at VDD. Ensure that the VDD supply ripple voltage is low enough: 54 mV(RMS) max @ f = 0… 3MHz and 15 mV(RMS) max @ f > 3 MHz.

**NOTE**

VDD supply is intended to be active all the time. Abrupt removals of VDD supply are not suggested and when required, e.g. when using CGEE storage to external EEPROM, use an external voltage detector to force reset at VDD under voltage conditions.

De-couple the VDD input externally with e.g. 4.7uF low ESR ceramic capacitor connected to GND. The module has also internal a low ESR (~0.01 ohm) by-pass capacitor at VDD supply input. Ensure that the external regulator providing VDD supply is suitable for loads with low ESR ceramic capacitors.

VDD supply ripple voltage: 54 mV(RMS) max @ f = 0… 3MHz and 15 mV(RMS) max @ f > 3 MHz

## 4.3 Host port configuration

User can select the host port configuration between UART, SPI (slave) and $I^2C$ (master/slave) during power up boot. At system reset, the host port pins are disabled, so there will be no port conflict occurring. Depending on the host port type, the software enables the correct port drivers, sets up the port hardware, configures the pins according to the port type and begins operations.

The port selection is not intended to be changed dynamically but only set once at power up. Default host port is SPI (selected by internal pull up/down resistors that are present during power up) and other host port configurations requires connection of external pull down (to 0V) or pull up (to 1.8V) resistor at CTS_N and RTS_N pins, see table below.

**Table 3 Host port boot strap**

| Host port | RTS_N | CTS_N |
|---|---|---|
| UART | - | Pull up 10 kohm |
| SPI | - | - |
| $I^2C$ | Pull down 10 kohm | - |

## 4.4 Host port UART

UART is normally used for GPS data reports and receiver control. Serial data rates are selectable from 1200 baud to 1.8432 Mbaud. Default baud rate is 4800 baud; default protocol is NMEA (protocol and baud rate can be configured by NMEA $PSRF100 message). RX signal is suggested to be pulled up externally when not used.

## 4.5 Host port SPI

The host interface SPI is a slave mode SPI:

- Supports both SPI and Microwire formats
- An interrupt is provided when the transmit FIFO and output serial register (SR) are both empty
- The transmitter and receiver each have independent 1024B FIFO buffers
- The transmitter and receiver have individual software-defined 2-byte idle patterns of 0xA7 0xB4
- Clock polarity: default SPI mode 1 (CPOL=0; CPHA=1) i.e. data is captured on the clock's falling edge and data is propagated on a rising edge
- MSB is sent first
- SPI detects synchronization errors and is reset by software

- Supports a maximum clock of 6.8MHz
- Signals: TX (SPI_DO, MISO), RX (SPI_DI, MOSI), CTS_N (SPI_CLK) and RTS_N (SPI_SS_N)
- Supports GPIO3 Message_Waiting output (high state) (from ROM2.0 onwards).

The SPI bus is a synchronous serial data link and a '*de facto*' standard named by Motorola. For further information see e.g. Wikipedia: http://en.wikipedia.org/wiki/Serial_Peripheral_Interface_Bus.

Microwire is a restricted subset of SPI and a trademark of National Semiconductor. For details see e.g. http://www.national.com/an/AN/AN-452.pdf ref (4).

At system level the slave has no way of forcing data to the master to indicate it is ready for transmission; the master must poll the client periodically. Since the specified idle byte pattern for both receive and transmit is 0xB4 0xA7, the master can transmit this idle pattern into the slave repeatedly. If the master receives idle patterns back from the slave, it indicates that the slave currently has nothing to transmit but is ready to communicate. Default protocol is NMEA (protocol can be configured by NMEA $PSRF100 message).

On initial power up after sending wake up ON_OFF pulse, the first message to come out of the module is the OK_TO_SEND message. Note that it takes about 100 ms from wake up for the SPI drivers to get initialized. If the host starts to communicate via SPI bus too early before the 100 ms has elapsed after ON_OFF pulse, it may cause wrong host boot strap detection. The host may also use GPIO 3 (ECLK) signal (high state; from ROM2.0 onwards) for indication when SPI slave is ready to for communication and has a message In FIFO.

On the receive side, the host is expected to transmit idle pattern 0xA7 0xB4 when it is querying the module's transmit buffer, unless it has traffic to send to the module. In this way, the volume of discarded bytes is kept nearly as low as in the UART implementation because the hardware does not place most idle pattern bytes in its RX FIFO. The module will also assert GPIO 3 high state (from ROM2.0 onwards) whenever it has data in the module transmit FIFO. The host can observe this GPIO 3 (ECLK) signal to know when to poll the receiver for data.

The FIFO thresholds are placed to detect large messages requiring interrupt-driven servicing. On the transmit side, the intent is to fill the FIFO only when it is disabled and empty. In this condition, the SPI driver software loads as many queued messages as can completely fit in the FIFO. Then the FIFO is enabled. The host is required to poll messages until idle pattern bytes are detected. At this point the FIFO is empty and disabled, allowing the SPI driver to again respond to an empty FIFO interrupt and load the FIFO with any messages in queue.

When switching the module to hibernate state using orderly shutdown with an ON_OFF pulse, by a low power mode or by OSP/NMEA command message, the module will continue to run until the SPI transmit/output buffers are emptied. If the host flow stops polling or turns off the SPI clock before the SPI FIFO is empty and OK_TO_SEND message is sent from module to host, the module will never turn off.

Default protocol is NMEA (protocol can be configured by NMEA $PSRF100 message; commands containing UART baud rate: use default speeds 4800 baud for NMEA and 115200 baud for binary OSP).

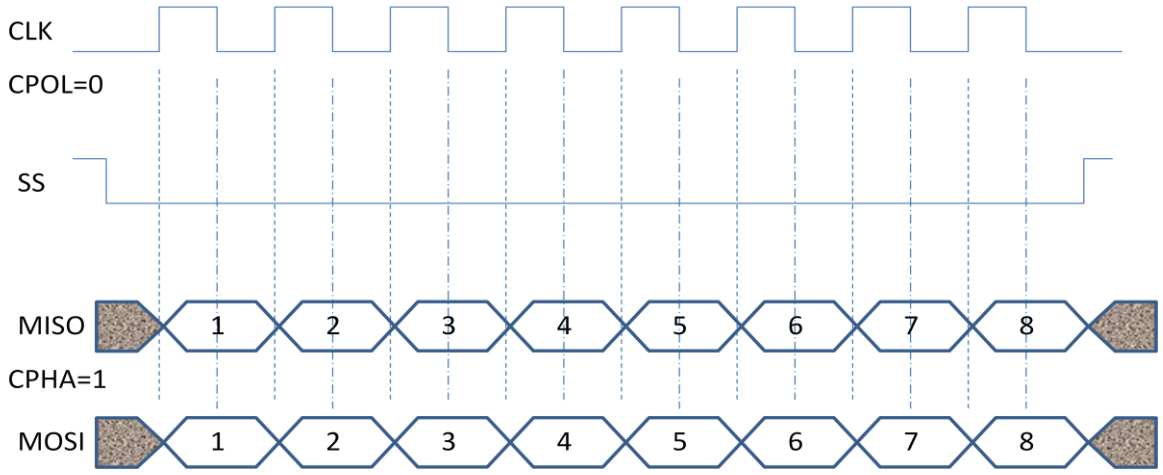



**Figure 2 SPI host port timing, SPI mode 1 (assuming one byte transfer)**

## 4.6 Host port I²C

The I²C host port interface supports:

- Default speed is 400kbps, configurable to 100kbps (by OSP Message ID 178, Sub ID 2)
- Default operating mode is multi-master
  - Transmit side operates as master by seizing the I²C bus when detected idle
  - Receive side operates as a slave when another master seizes bus and transmits to this address
- Configurable also to slave mode (by OSP Message ID 178, Sub ID 2)
- Default I2C address values are (configurable by OSP Message ID 178, Sub ID 2):
  - RX 0x60, TX 0x62
- Individual transmit and receive FIFO lengths of 64B
- Signals: TX (I2C_CLK, SCL) and RX (I2C_DIO, SDA) and requires external pull up resistors (to +1.8… +3.6V) on both signals somewhere in the system. Pull up resistor value depends on used clock speed and signal line stray capacitance; suggested pull up is e.g. 2.2kohm.

The operation of the I²C in multi-master mode with a master transmit and slave receive mimics a UART operation, where both module and host can independently freely transmit. Default protocol is NMEA (protocol can be configured by NMEA $PSRF100 message; commands containing UART baud rate: use default speeds 4800 baud for NMEA and 115200 baud for binary OSP).

The I²C bus operation is specified in detail including evaluating tools, application notes and drivers by Philips Semiconductors, see http://www.nxp.com/acrobat_download2/literature/9398/39340011.pdf ref (5).

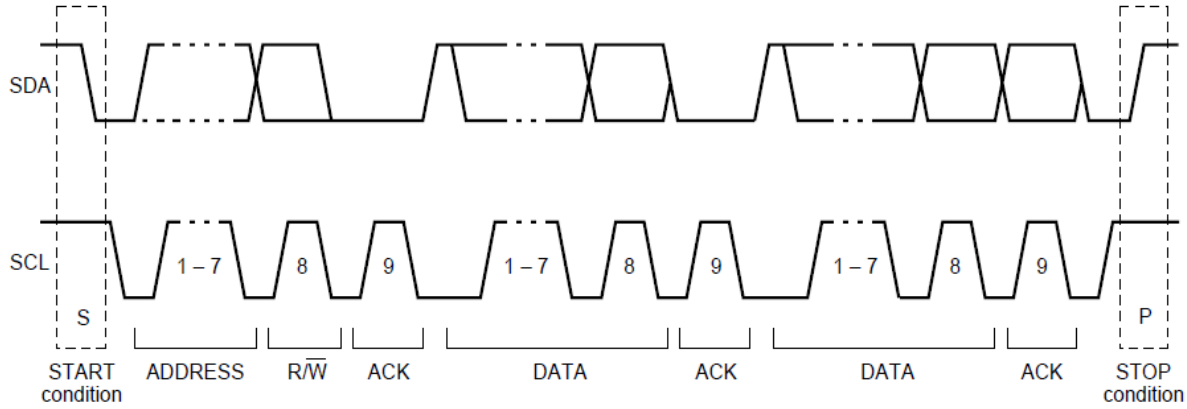



**Figure 3 I²C host port data transfer**

## NOTE

When host port is configured to I²C bus use external pull up resistors (e.g. 2.2 kohm to +1.8… +3.6 V) at both signals.

### 4.7 ON_OFF control input

The ON_OFF control input must be used by the host to wakeup the module after first power up and to control the receiver activity between Normal and Hibernate states and also to generate interrupt in TricklePower, Push-to-Fix and SiRFAware modes of operation.

The module will boot to Hibernate state after power up. First ON_OFF interrupt wakes up the module for Normal (Navigation) operation. Consequent ON_OFF interrupts switch the operation mode between Hibernate and Navigation modes. Autonomous wakeup after power up from Hibernate state to full on mode can be enabled by connecting WAKEUP signal to ON_OFF signal, see also chapter 4.13.

In NMEA protocol $PSRF150 (OKtoSend) messages are sent out when the receiver is ready to receive messages or when it is going into low-power mode and no more messages should be sent from the host. When Full power is restored, the first message sent is $PSRF150,1*3E<CR><LF> and when power is going to be reduced to Hibernate state, the last message sent is $PSRF150,0*3F<CR><LF>. Similar message is also available in binary OSP protocol (MID 18) that is sent when going into low-power mode and no more messages should be sent from the host.

The ON_OFF interrupt is generated by rising edge of a low-high-low pulse, which should be longer than 90us and less than 1s (suggestion is abt. 100ms pulse length). Do not generate ON_OFF interrupts less than 1 sec intervals. Especially take care that any multiple switch bounce pulses are filtered out.

During Hibernate state the I/O Keep Alive is still active, thus I/O signals keep respective states except TX and RX signals, which are configured to high input impedance state.

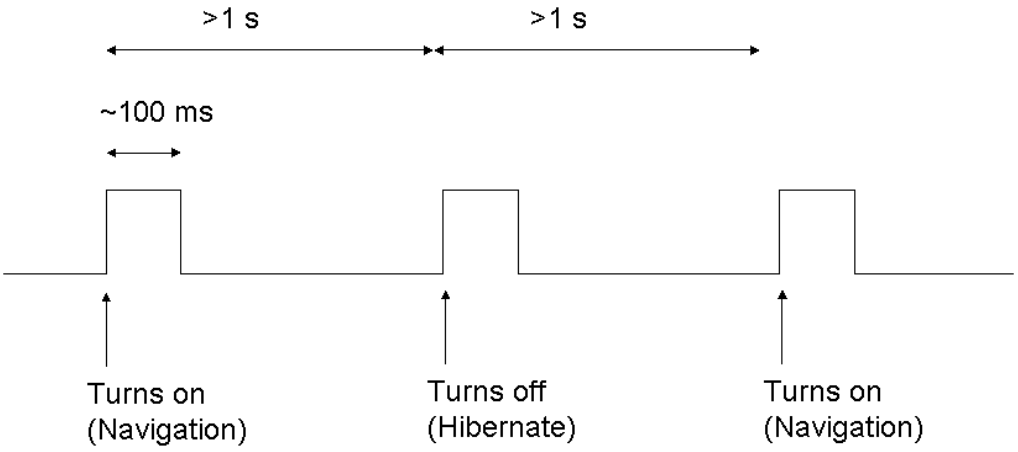



**Figure 4 ON_OFF timing**

The ON_OFF control input is configurable via a binary message from the host (Message ID 178 TrackerIC, Sub ID 2 TrackerConfig or via custom patch code; contact Fastrax support for details).

**NOTE**

| |
|---|
| Do not generate multiple ON_OFF interrupts less than 1 sec intervals. Especially filter out multiple pulses generated by a mechanical switch bounce. |

## 4.8 Reset input

The RESET_N (active low) signal provides external override of the internally generated power up/down reset. Normally external control of RESET_N is not necessary. When power supply VDD may be abruptly removed, suggestion is to use externally generated reset by means of external VDD voltage monitor.

When RESET_N signal is used, it will force volatile RAM data loss (e.g. ROM patch code is lost if external EEPROM is not used). Note that Non-Volatile Backup RAM content is not cleared and thus fast TTFF is possible and Patch code (if used) is recovered from external EEPROM after reset. The input has internal pull up resistor 86 kohm typ. and leave it not connected (floating) if not used.

## 4.9 Antenna input

The module has an embedded GPS antenna, which is available at ANT output. The antenna input signal RF_IN impedance is 50 ohms and it shall be connected externally to ANT output via a short trace between pads. The RF input signal path contains first a SAW band-pass filter, which provides excellent protection against out-of-band GPS blocking caused by possible near-by wireless transmitters, ref (9).

## 4.10 Active GPS antenna

The customer may use an external active GPS antenna connected via an external antenna switch. It is suggested that the active antenna has a net gain *including cable loss* in the range from +10 dB to +35 dB. Specified sensitivity is measured with external low noise (NF$\leq$1dB, G$\geq$15dB) amplifier, which gives about 2dB advantage in sensitivity when compared to embedded antenna usage without an external LNA.

An active antenna requires an external antenna switch in order to select RF_IN input between ANT and external GPS antenna signal. For reference see e.g. the application circuit diagram in chapter 7.2. Fastrax support can also provide other antenna switch circuits using discrete components.

The switch shall detect external active antenna presence for switching antenna signal path to external antenna by using e.g. the active antenna bias current detection. Second option is to use a suitable RF-connector with build-in switching operation. The external antenna switch must also provide a bias supply to the external active antenna and suggestion is also to add an external short circuit protection for antenna bias voltage. Note that both ANT and RF_IN signals provide DC-path to ground and thus do not apply any bias voltage to these signals. Max DC voltage at ANT and RF_IN signals is 0V; thus use an external series DC-block capacitor when needed.

When the module is in Hibernate state, the antenna switch and bias can be switched off externally by using WAKEUP signal output, see e.g. Application Circuit Diagram.

### 4.10.1 Jamming Remover

Jamming Remover (aka CW Detection) is an embedded HW block that detects, tracks and removes up to 8 pcs CW (Carrier Wave) type signals up to 80 dBHz (-90 dBm) signal levels. By default the Jamming Remover is disabled and usage requires an OSP binary command Message ID 220 (CW Configuration) to enable.

Jamming Remover can be used for detecting and solving EMI problems in the customer's system and it is effective against e.g. narrow band clock harmonics. Use PC utility SiRFLive to indicate and detect CW EMI signals, see also SiRFLive user manual for details. Jammer detection sensitivity is about 55 dBHz and below this threshold jammers are not detected.

Note that Jamming Removal is not effective against wide band noise (e.g. from host CPU memory bus), which cannot be separated from thermal noise floor and which increases effective noise floor and reduces GPS signal levels. When enabled, Jammer Remover will increase current drain by about 2 mA but impact on GPS performance is low at modest Jammer levels; however at high Jammer levels 70… 80 dBHz the signal sampling (ADC) starts to get saturated, which will reduce GPS signal levels.

See ref (6) Application Note for details on Jammer Remover usage.

## 4.11 Dead Reckoning $I^2C$ bus

The DR_$I^2C$ bus (master) provides optional connectivity to the following devices:

- Optional connectivity to EEPROM for Client Generated Extended Ephemeris (CGEE) data storage
- Optional ROM patch code storage to EEPROM and upload to UC430
- Optional MEMS sensors (e.g. support for 3-D Accelerometer or 3-D Compass for Stationery Detection with ROM2.0 firmware).

The DR $I^2C$ interface provides means for patch code and CGEE data storage via an external EEPROM. Once the patch or the CGEE data is stored to the EEPROM, the module will detect automatically the presence of these data blocks even after power removal during next wakeup and thus host renovation of the patch or CGEE data is not needed.

When enabled the optional 3-D Accelerometer MEMS sensor provides feature for Stationary Detection, which allows to reduce the position spread when in stationary condition during weak GPS signals e.g. indoors. When MEMS Accelerometer sensor is used connect also the sensor's INT output to IT430's EIT input, which allows the system to wake up more frequently during SiRFAware low power operation mode when GPS signal visibility is missing assuming that movement will result to improved GPS visibility.

When enabled the optional 3-D Magnetometer (Compass) provides attitude (heading) information that aids navigation in velocity heading.

The bus signals require external pull up resistors 2.2kohm on both SCL and SDA signals. Connect both signals to GND (or pull up) when not used. The sensor measurement data output is available via binary OSP message MID 72. Note that sensors are disabled by default and need to be enabled by binary Message ID 234, Sub ID 2 (message payload in hex EA 02 03).

DR I²C interface supports:

- Common EEPROM data formats (STMicroelectronics M24M01-R, 1 Mbit device; ROM2.0 onwards: Microchip 512 kbit 24AA512T-I/MF and 1 Mbit 24AA1025T-I/SN)
- Common sensor formats (ROM2.0 onwards: Kionix, KXTF9-4100 and Aichi Steel, AMI304)
- Typical data lengths (command + in/data out) of several bytes
- Standard I²C bus maximum data rate 400kbps; minimum data rate 100kbps
- Sensor data messages (ROM2.0, binary OSP):

| | | Message ID, Sub ID |
|---|---|---|
| ○ Sensor Configuration | Input | 234, 1 |
| ○ Sensor Enable | Input | 234, 2 Note: sensors are disabled by default |
| ○ Sensor Data Message | Output | 72,1 |
| ○ Receiver State Message | Output | 72,3 Note: static/moving indication |

**NOTE**

DR_I²C bus requires external pull up resistors (e.g. 2.2 kohm to +1.8… +3.6 V) at both signals.

## 4.12 Time Mark TM

The TM output signal provides pulse-per-second (PPS) output pulse signal for timing purposes. Pulse length (high state) is 200ms and it has 1us accuracy synchronized at rising edge to full UTC second with nominal GPS signal levels. The TM will output PPS after a few seconds from first fix when the fix epoch is synchronized to full second. The PPS output is valid when navigation is valid and will also continue after valid fix is lost by a certain navigation DR timeout (default configuration 15 seconds); the timeout is configurable by OSP binary protocol MID 136, DR Time Out. User can also enable NMEA $GPZDA message that is sent right after the TM pulse just sent.

The firmware may support optionally other output function configuration from TM signal, like GPS_ON output for e.g. external LNA power control or RTC_CLK, which outputs buffered RTC clock signal at 32768 Hz; contact Fastrax support for details on I/O configuration.

## 4.13 Wakeup

The WAKEUP output signal provides indication to e.g. external power supply when full power is required by the module. Polarity is active high = high current mode. The external power supply should be able to provide full current to VDD within 9ms after WAKEUP low->high transition.

WAKEUP signal can be also used externally to switch off the Active Antenna Bias supply voltage (VDD_ANT) during Hibernate state; polarity is active high = VDD_ANT active. The WAKEUP signal has a short pulse after initial power up due to internal state machine settling; this allows also autonomous wakeup to Full on Navigation mode after initial power up when the WAKEUP signal is connected to ON_OFF input.

**NOTE**

Autonomous wakeup to Full Navigation mode after initial power up can be enabled by connecting the WAKEUP signal to ON_OFF input.

## 4.14 Interrupt inputs EIT and EIT2

The EIT and EIT2 are external, level sensitive interrupt inputs. EIT2 pin is also configurable as an edge-sensitive input. Both pins are disabled at initial power-up and usage is configured by the software (firmware support is up ROM release or patch).

When using an external accelerometer on DR_$I^2C$ bus, connect the interrupting output of the sensor to the EIT input.

When not used connect these inputs to ground.

## 4.15 ELCK signal

The ECLK is reserved for external clock input with special variant for A-GPS frequency aiding and is disabled by default. With firmware 4.1.0 (aka ROM2.0) onwards the signal function is GPIO3 Message_Waiting (output), which is enabled when in SPI or UART handshaking host port modes. The signal is suggested to be left floating or pulled to GND when not used.

## 4.16 TSYNC signal

TSYNC input is reserved for external time aiding with a special variant used for A-GPS. The input is suggested to be connected to GND when not used.

## 4.17 Mechanical Dimensions

Module size is square 9.6 mm (width), 14.0 mm (length) and 1.95 mm (height, 2.25 mm max). General tolerance is ±0.3 mm. Note pin 1 polarity mark on the corner on the shield.

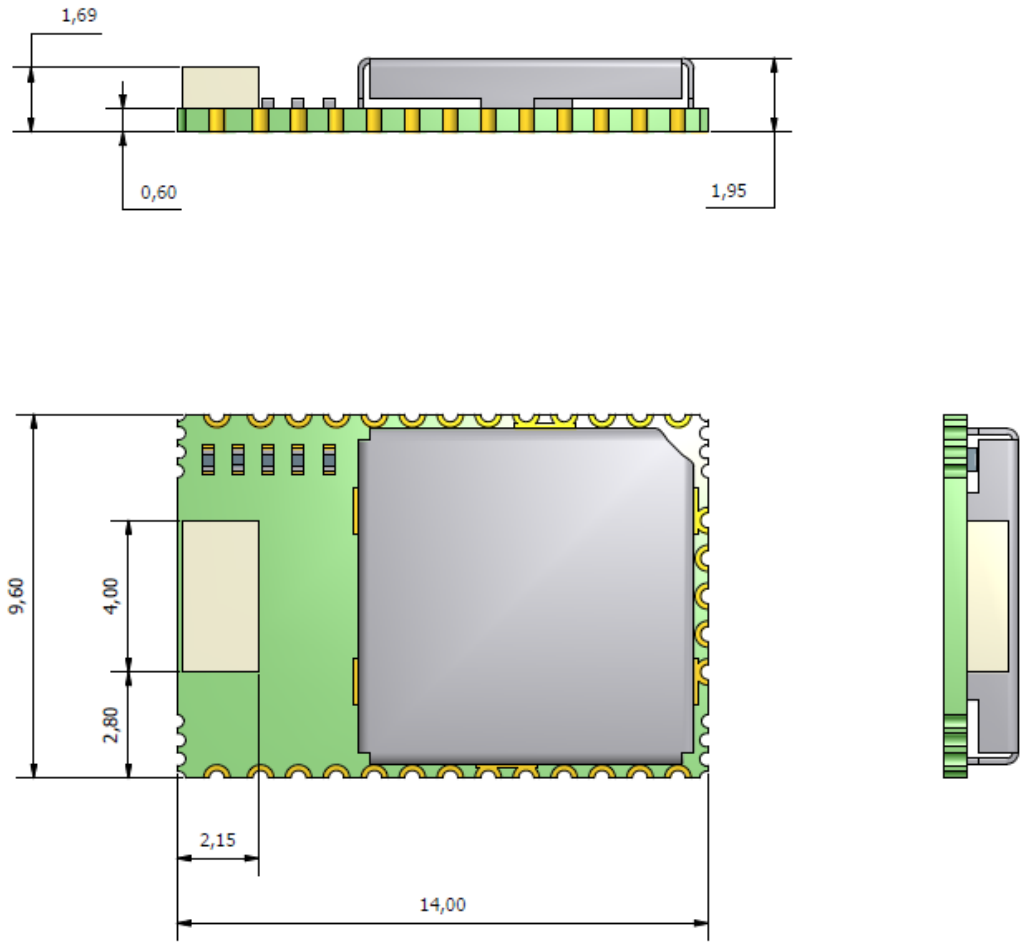



**Figure 5 Mechanical Dimensions**

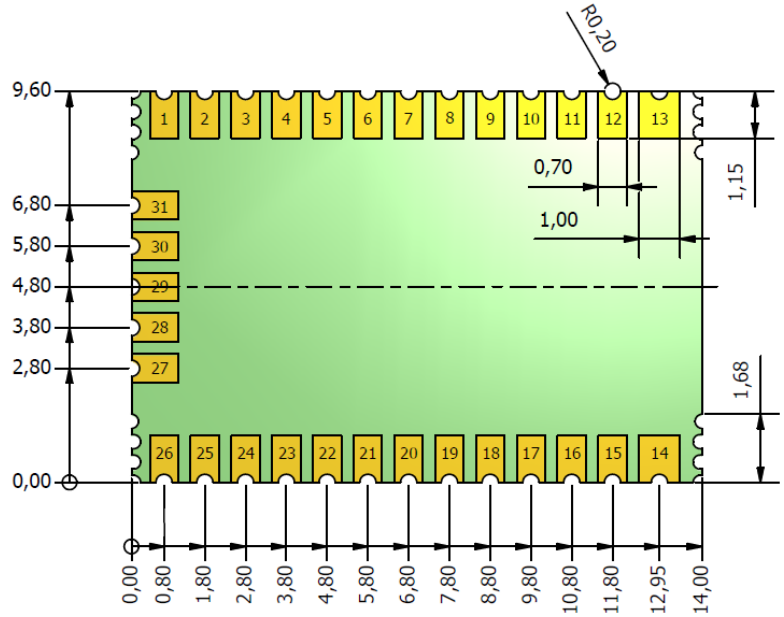



**Figure 6 Pin numbering and dimensions, bottom view**

### 4.18 Suggested pad layout

Suggested paste mask openings equal to pad layout. Note the keepout (void area) 4.8x7.2mm for copper & trace & components for all layers under the embedded antenna.

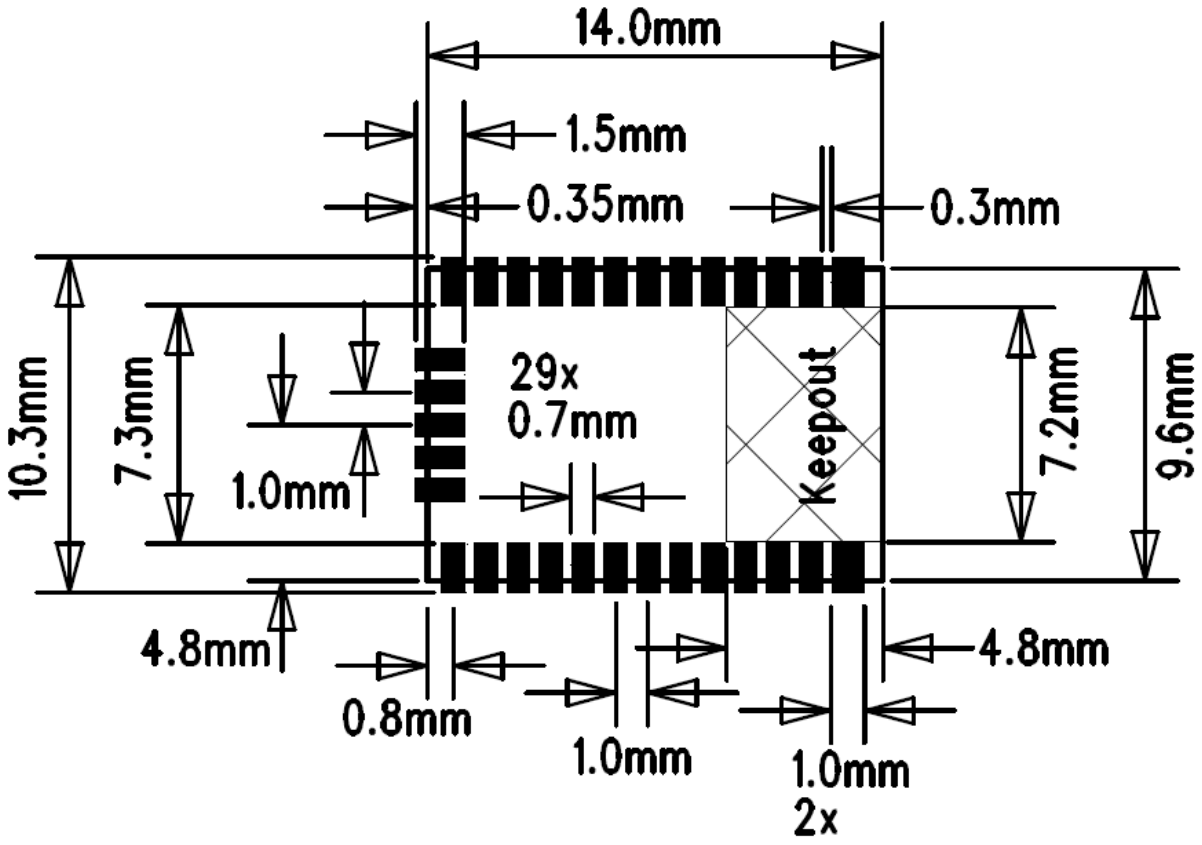



**Figure 7 Suggested pad layout and occupied area, top view**

# 5 Electrical Specifications

## 5.1 Absolute Maximum Ratings

Stressing the device beyond the Absolute Maximum Ratings may cause permanent damage. These are stress ratings only. Operation beyond the DC Electrical Specifications, Table 5 DC Electrical characteristics, is not recommended and extended exposure beyond the Recommended Operating Conditions can affect device reliability.

**Table 4 Absolute Maximum Ratings**

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $T_{AMB}$ | Operating and storage temperature | -40 | +85 | °C |
| $P_{DIS}$ | Power dissipation | - | 200 | mW |
| VDD | Supply voltage input | -0.3 | +2.2 | V |
| $V_{IO}$ | Input voltage on any input connection | -0.3 | +3.6 | V |
| $V_{IO}$(ESD) | IO ESD voltage (only RF_IN, Machine Model) | -50 | +50 | V |
| $V_{IO}$(ESD) | IO ESD voltage (excluding RF_IN, HBM model) | -2000 | +2000 | V |
| $P_{RF}$ | RF_IN input power (in band 1575 +/- 30 MHz) | - | +10 | dBm |
| $P_{RF}$ | RF_IN input power (out of band <1460 MHz or >1710 MHz) | - | +15 | dBm |

Note that module is Electrostatic Sensitive Device (ESD).

## 5.2 DC Electrical specifications

Operating conditions are $T_{AMB}$ =+25°C and VDD =+1.8 V unless stated otherwise.

**Table 5 DC Electrical characteristics**

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $T_{AMB}$ | Operating Temperature *(note 1)* | -40 | +25 | +85 | °C |
| VDD | Supply voltage input | +1.71 | +1.8 | +1.89 | V |
| $VDD_{AC}$ | Supply voltage ripple, AC coupled | | | 54 | mV(RMS) f=0…3 MHz |
| $VDD_{AC}$ | Supply voltage ripple, AC coupled | | | 15 | mV(RMS) f> 3 MHz |
| $I_{VDD}$ (peak) | Supply current, peak acq. | | 47 | 90 | mA |
| $I_{VDD}$ (ave) | Supply current average, tracking | | 37 | | mA |
| $I_{VDD}$ (Hib.) | Supply current, Hibernate state | | 20 | | µA |
| $I_{I(LEAK)}$ | Leakage current, Digital Input | -10 | | +10 | µA |
| $V_{OL}$ | Low level output voltage, $I_{OL}$ 2 mA | | | +0.4 | V |
| $V_{OH}$ | High level output voltage, $I_{OH}$ 2 mA | 0.75*VDD | | | V |
| $V_{IL}$ | Low level input voltage | -0.3 | | +0.45 | V |
| $V_{IH}$ | High level input voltage | 0.7*VDD | | +3.6 | V |

*Note 1: Operation in the temperature range –40°C… –30°C is allowed but Time-to-First-Fix performance and tracking sensitivity may be degraded.*

**NOTE**

Note that UC430 module is sensitive to supply voltage ripple caused by e.g. current drain variation and thus power supply should have effective series resistance (ESR) below 0.2 ohm.

## 5.3 AC Electrical characteristics

Operating conditions are $T_{AMB}$ =+25°C and VDD =+1.8 V unless stated otherwise.

**Table 6 AC Electrical characteristics**

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $t_{TM}$ | TM (PPS) cycle time | | 1 | | s |
| $t_{TM,H}$ | TM, high state pulse duration | | 200 | | ms |
| $\Delta t_{PPS}$ | TM accuracy, rising edge (*note 1*) | -1 | | +1 | µs |
| $f_{RTC}$ | RTC output frequency (*note 2*) | | 32768 | | Hz |

*Note 1: with nominal GPS signal levels -130dBm.*

*Note 2: when enabled by I/O configuration.*

# 6 Manufacturing

## 6.1 Assembly and Soldering

The UC430 module is intended for SMT assembly and soldering in a Pb-free reflow process on the top side of the PCB. Suggested solder paste stencil height is 150um minimum to ensure sufficient solder volume. If required paste mask pad openings can be increased to ensure proper soldering and solder wetting over pads.

Use pre-heating at 150… 180 ºC for 60… 120 sec. Suggested peak reflow temperature is 235… 245ºC (for SnAg3.0Cu0.5 alloy). Absolute max reflow temperature is 260ºC. For details see Fastrax document 'Soldering Profile' ref (7).

Note that module is Electrostatic Sensitive Device (ESD). Rated voltage is TBD max (Machine Model) at RF_IN signal.

**NOTE**

Note that module is Electrostatic Sensitive Device (ESD), rating TBD max (Machine Model) at RF_IN.

Avoid also ultrasonic exposure due to internal crystal and SAW components.

The UC430 module meets the requirements of Directive 2002/95/EC of the European Parliament and of the Council on the Restriction of Hazardous Substance (RoHS). For details contact Fastrax support.

## 6.2 Moisture sensitivity

UC430 module is moisture sensitive at MSL 3 (see the standard IPC/JEDEC J-STD-020C). The module must be stored in the original moisture barrier bag or if the bag is opened, the module must be repacked or stored in a dry cabin (according to the standard IPC/JEDEC J-STD-033B). Factory floor life in humid conditions is 1 week for MSL 3.

Moisture barrier bag self life is 1 year; thus it is suggested to assemble modules prior self life expiration. If the moisture barrier bad self life is exceeded, the modules must be baked prior usage; contact Fastrax support for details.

## 6.3 Marking

Module marking includes type code, batch code and serial number.

Type code is e.g. **UC430rbbbb** (may vary)**,** where

- **UC430** is module type code for UC430
- **r** is incremental firmware revision (e.g. **C** = Signature firmware rev. 4.1.0 aka ROM2.0, may vary)
- **bbbb** is BOM (Bill-of-Materials) revision code (e.g. **4150**, may vary)

Batch code is e.g.**100208** (may vary)**,** where

- **1** is factory code

- **0** is last digit of the year (e.g. 201**0**)
- **02** is month (e.g. February)
- **08** is incremental number of the production batch during the month

Serial number is unique for each module having 10 digits including tester code, last two digits of the year, julian date code and incremental number.

### 6.3.1 Module variants

The UC430 module is available in only in Signature firmware feature set. Supported features include:

- CW Jammer Remover
- Embedded Client and Server generated EE support
- TricklePower, APM and Push-to-Fix low power modes
- SiRFAware (aka Micro Power Management) 125 uA low power state for fastest TTFF
- Support for Almanac Based Navigation
- AGPS support (Init aiding, set ephemeris, CGEE and SGEE support)
- SBAS/WAAS support (requires a patch with ROM2.0)
- MEMS sensor support: 3-D Accelerometer, 3-D Compass
- Note: HW support only for LDO mode (switcher coil not included in hardware)

## 6.4 Tape and reel

Minimum order quantity is 500 pcs. Reel is packed in 500 pcs per reel.

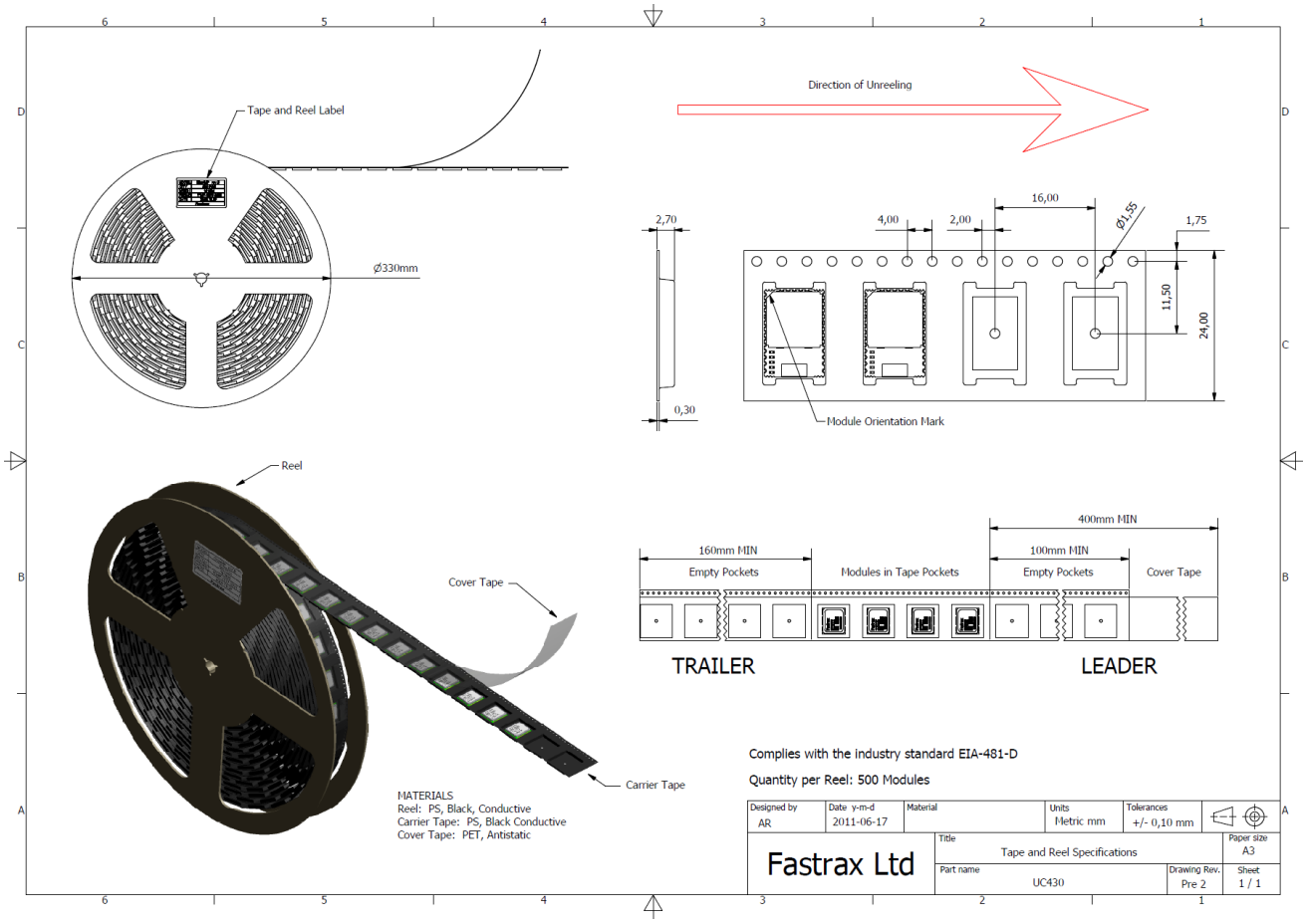



**Figure 8 Tape and reel specification**

# 7 Reference design

The idea of the reference design is to give a guideline for the applications using the OEM GPS module. In itself it is not a finished product, but an example that performs correctly.

In the following two chapters the reader is exposed to design rules that he should follow, when designing the GPS receiver in to the application. By following the rules one end up having an optimal design with no unexpected behavior caused by the PCB layout itself. In fact these guidelines are quite general in nature, and can be utilized in any PCB design related to RF techniques or to high speed logic.

## 7.1 Reference circuit diagram

The following picture describes a minimum connectivity for a typical autonomous navigation application. It consists of the UC430 module, which is powered by the main VDD supply (+1.8 V). The by-pass capacitor C1 is used to de-couple the VDD supply pin.

No back up supply is required. Instead keep the main supply VDD active all the time and use the ON_OFF control input to switch between Navigation and Hibernate operation modes. WAKEUP signal can be used optionally for external regulator mode control for full power state.

The host port is configured to UART by the pull up resistor R1. Serial port TX output is connected to host UART input. RX input connection to host UART output is required when sending commands to UC430. ON_OFF input must be driven by the host to wake up the module from Hibernate state after first power up. Optional connectivity for host includes TM signal for timing purposes.

Optional connectivity includes also an accelerometer sensor for stationary detection and an EEPROM on DR_$I^2C$ bus for Extended Ephemeris or ROM patch code data storage. Use external pull up resistors 2.2kohm at bus signals when bus is used. When bus is not used connect DR_$I^2C$ signals to ground.

Note that all I/O signal levels are CMOS 1.8V compatible and inputs are 3.6 V tolerable.

Some I/O signals have series resistors 47… 220 ohm, which are intended for RF-decoupling purposes to improve rejection to internally generated EMI that may leak to embedded GPS antenna.

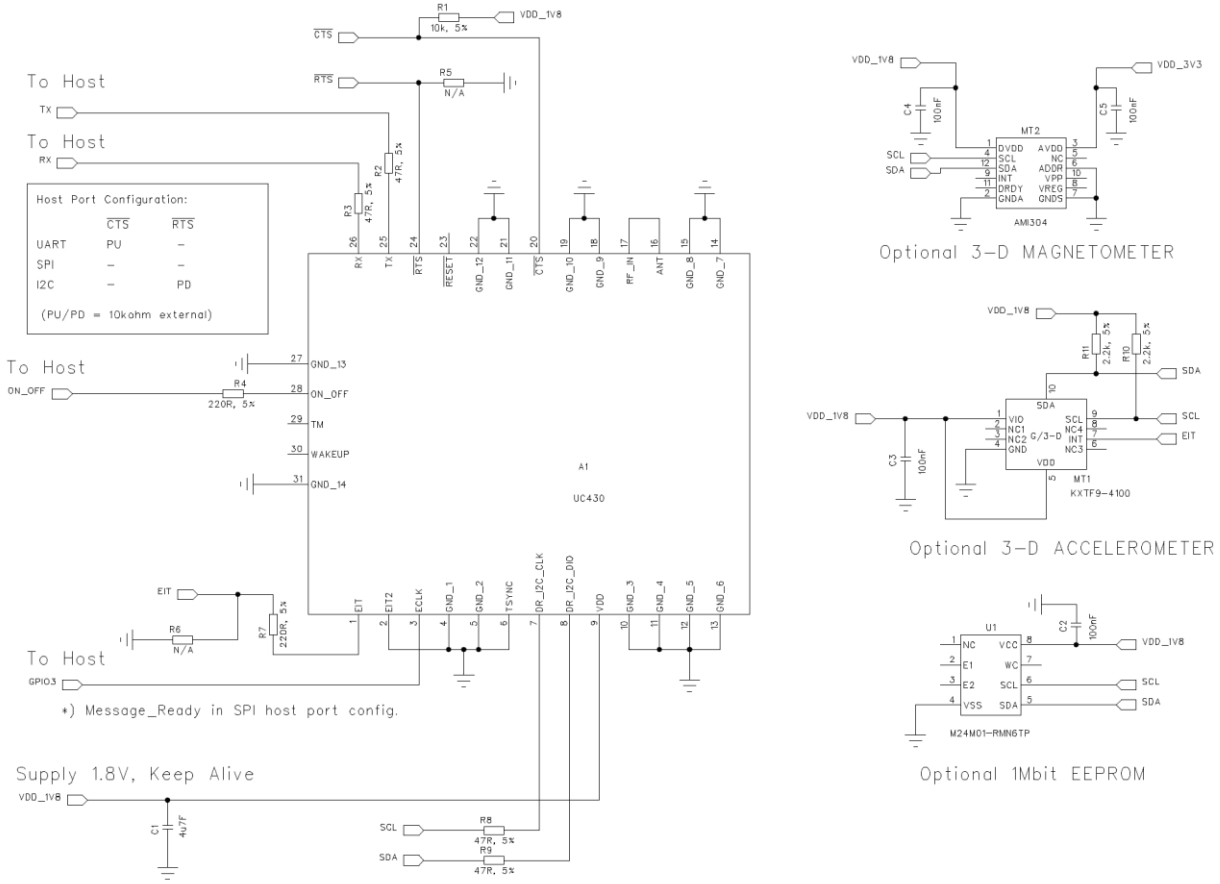



**Figure 9 Reference circuit diagram**

## 7.2 Reference circuit diagram, external antenna connectivity

The following reference circuit adds external GPS antenna connectivity by using Maxim MAX2674 LNA + Switch. The U2 provides an LNA and a Switch function, which detects presence of the external antenna by measuring the bias current drain and then switching RF signal path to external antenna. Note that max antenna bias current is limited below 20mA with MAX2674.

Prior the U2 LNA there is an option for band pass filter FL1. This filter can be omitted for general applications but for maritime and for applications with nearby wireless transmitting antenna the external band pass filter is suggested to be connected prior first LNA in order to improve out-of-band blocking rejection. Suitable filter types include e.g. Epcos B9416 or filters with similar characteristics (low insertion loss 1dB typ.).

Keep RF signal traces short in order to minimize losses and keep transmission line impedance at 50 ohm, see next chapter.

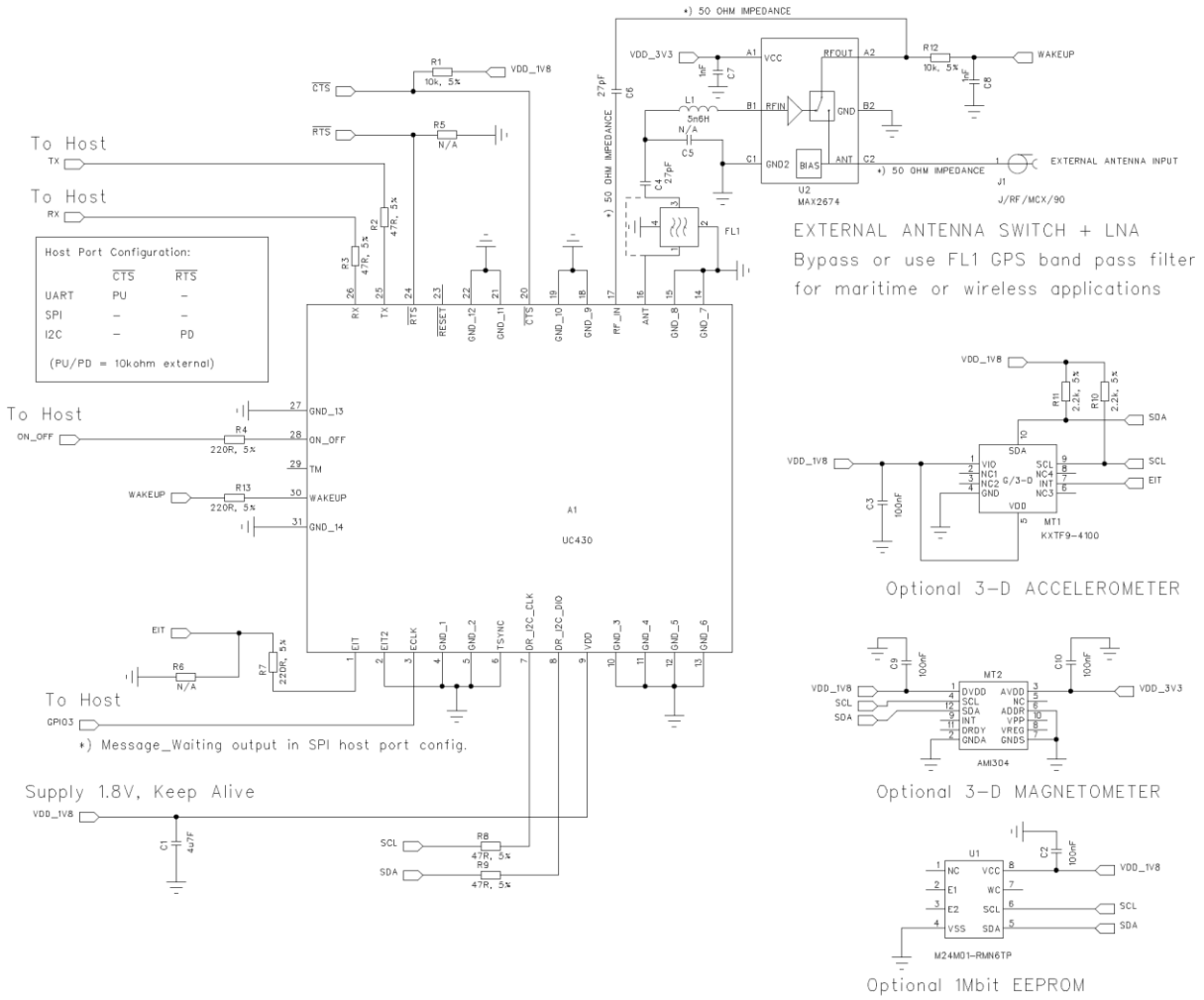



**Figure 10 Reference circuit diagram, external antenna**

## 7.3 PCB layout suggestion

The suggested 4-layer PCB build up is presented in the following table.

**Table 7 Suggested PCB build up**

| Layer | Description |
|---|---|
| 1 | Components + Ground plane (opening under UC430 antenna) |
| 2 | Signals and RF trace (opening under UC430 antenna) |
| 3 | Ground and power planes, signals (opening under UC430 antenna) |
| 4 | Ground plane, also short traces allowed (opening under UC430 antenna) |

The UC430 module is intended to be assembled at the top edge of the mother board. The embedded antenna operation relies on the ground plane on the mother board; optimum size is 80x40mm but larger or smaller ground plane can be used. Suggested minimum ground plane size is 45x20mm. Optimum placement is at the center of the top edge but offset placement is allowed by keeping at least 10mm distance to nearest ground plane edge.

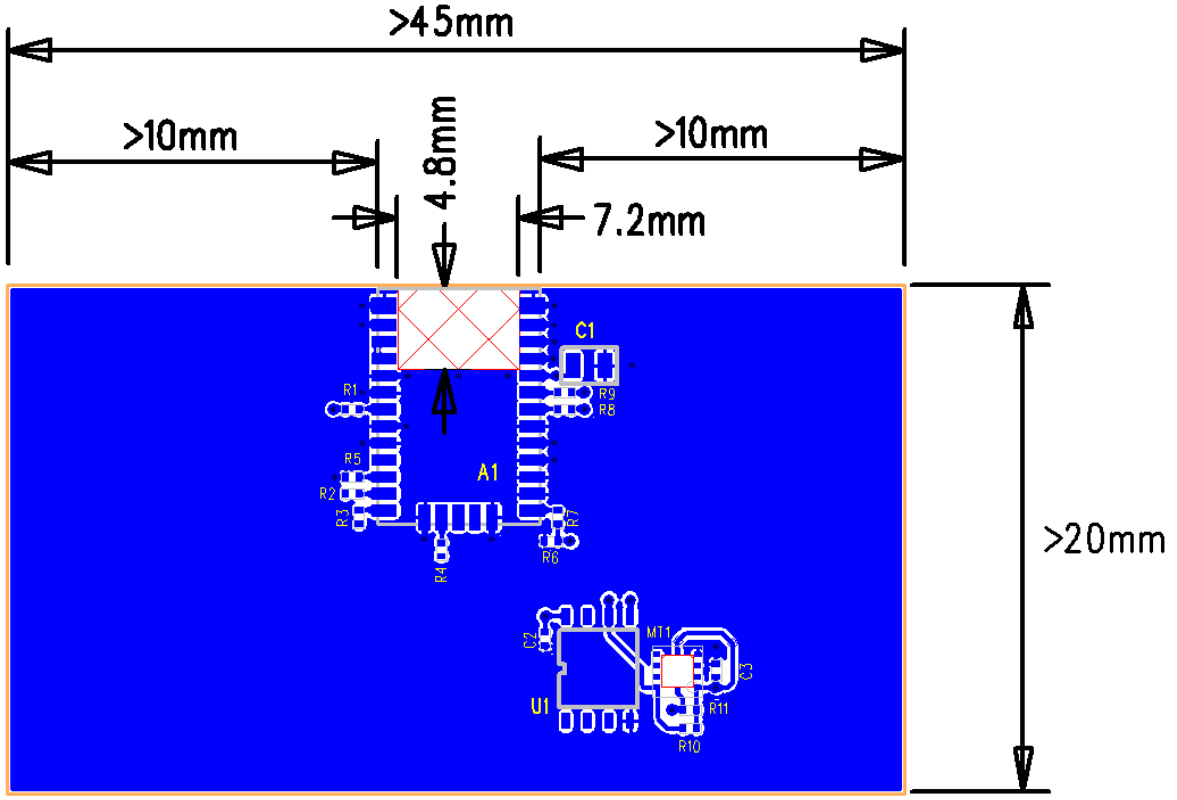



**Figure 11 Mother board ground plane and UC430 placement**

Note keepout 4.8x7.2mm under the embedded antenna. Component names refer to the reference cicuit diagram. Follow also GND via hole suggestive locations.

Routing signals directly under the module should be avoided. This area should be dedicated to keep-out to both traces and assigned to ground plane (copper plane), except for via holes, which can be placed close to the pad under the module. If possible, the amount of VIA holes underneath the module should be minimized.

Note that the embedded GPS antenna requires a small ground plane clearance and void area (keep out 4.8x7.2mm) for copper plane & trace for all layers under the antenna. Placement of other components is not allowed under the keep out on opposite side.

For a multi-layer PCB the inner layers below the UC430 is suggested to be dedicated signal traces and copper plane for the rest of the area. It is always better to route very long signal traces in the inner layers of the PCB. In this way the trace can be easily shielded with ground areas from above and below.

The serial resistors at the I/O should be placed as close to the UC430 module as possible. In this way the risk for the EMI leakage is minimized. For the same reason by-pass capacitors C1 should be connected very close to the module with short traces to IO contacts and to the ground plane. Place a GND via hole as close as possible to the capacitor.

Connect the GND soldering pads of the UC430 to ground plane with short traces (thermals) to via holes, which are connected to the ground plane. Use preferably one via hole for each GND pad.

A RF signal is suggested to be routed clearly away from other signals between two ground planes as a Stripline Transmission Line; this minimizes the possibility of interference and coupling. The proper width for the 50 ohm transmission line impedance depends on the dielectric material of the substrate, width of the signal trace and the

height (separation) of the two ground planes. With FR-4 material the width of the trace shall be about 30% of the ground plane height. E.g. 0.4mm ground plane height results to 0.15mm trace width with FR-4 substrate.

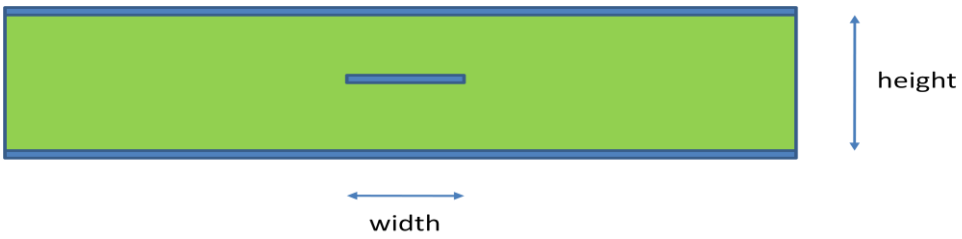



**Figure 12 Stripline transmission line**

Any board space free of signal traces should be covered with copper areas connected to ground net; in this way a solid RF ground plane is achieved throughout the circuit board. Several via holes should be used to connect the ground areas between different layers.

Additionally, it is important that the PCB build-up is symmetrical on both sides of the PCB core. This can be achieved by choosing identical copper content on each layers, and adding copper areas to route-free areas. If the circuit board is heavily asymmetric, the board may bend (wrap) during the PCB manufacturing or reflow soldering. Bending and wrapping may cause soldering failures and reduce end product reliability.

The AP430 Application Board layout described in next chapter can be also used as layout reference implementation.

### 7.3.1 Other electronics on mother board

Signal traces on top and bottom layers should have minimum length. Route signals mainly at inner layers below the top or bottom ground plane. In this way, a solid RF ground is achieved throughout the circuit board on top and bottom sides. Several via holes should be used to connect the ground areas between different layers.

Areas with dense component placing and dense routing requirements should be covered with a metal shield, which should be connected to ground plane with multiple GND via holes. Small ground plane openings for SMT components (length few mm, like LED or push buttons) in the ground plane are OK without a shield.

Dense areas having multiple via holes may open the ground plane for wide areas, thus blind and buried via holes are suggested to be used when changing layers for internal signals and power planes.

Use a power plane layer dedicated solely for power nets. Use wide trace width or even copper plane areas to achieve low impedance for power nets. Dedicate at least one layer as ground planes on adjacent layer above or below power plane layer in order to maximize capacitance to ground plane.

### 7.3.2 Avoiding EMI

Any GPS receiver is vulnerable to external spurious EMI signals since GPS signals are very weak below thermal noise floor. Any man made noise or spurious signals picked up by the GPS antenna increases the noise floor and reduces GPS signal levels. Carrier Wave (CW) type spurious signals like clock harmonics on GPS band may also cause cross correlation products that may interfere with GPS signal tracking.

Since the ground plane of the mother board plays a vital role in the embedded antenna operation, it is essential for good GPS performance that the following measures against EMI are properly implemented:

- High speed electronics like CPU & memory bus are enclosed in a ‘Faraday shield’. The electrical enclosure is formed by the ground planes on PCB + metal shield over components. Route signals at inner layers as discussed previously. Use preferably a power plane(s) layer for supply nets.

- Any signal that is routed outside the Faraday shield is protected against EMI noise on 1575MHz with a serial RF filter like
    - a serial resistor (> 330ohm, suitable for I/O with low current) or
    - with a dedicated EMI filter (or ferrite bead) suitable for higher current or
    - with suitable by-pass capacitor e.g. 18pF (low impedance due to series resonance at 1575MHz).

The following picture gives a suggestion for e.g. a 6-layer PCB build up, which forms a Faraday shield together with ground planes on PCB and with the shield over high speed electronics. Buried and blind via holes are used to keep EMI signal inside ground planes. I/O signals that are routed outside the Faraday enclosure are filtered with a suitable EMI filter. Power plane layer is used for supply nets with low impedance traces/planes.

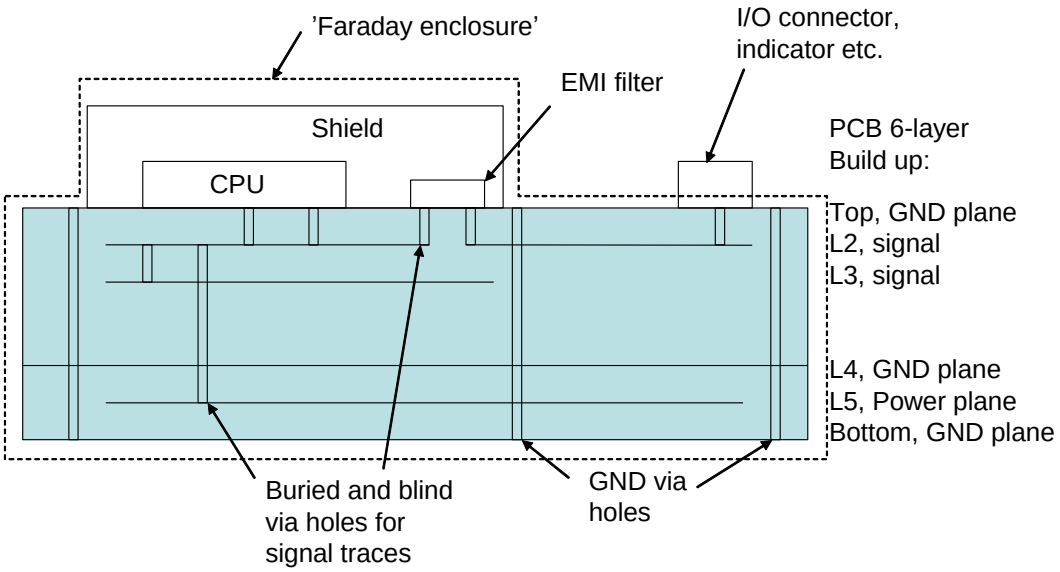



**Figure 13 Avoiding EMI with Faraday enclosure**

## 7.4 Embedded antenna operation

The embedded GPS antenna provides optimal radiation efficiency 80% typ. with 80x40mm ground plane. linear polarization with peak gain 1.1dBi and radiation pattern optimized for portable devices. The antenna is insensitive to surroundings and has high tolerance against frequency shifts. However on small ground plane widths the antenna gain and radiation efficiency reduces, e.g. the AC430 application board having 53mm width reduces signal levels by 2dB when compared to full 80x40mm ground plane dimensions. Radiation pattern of the embedded GPS antenna is shown in the picture below (on 80x40mm ground plane).

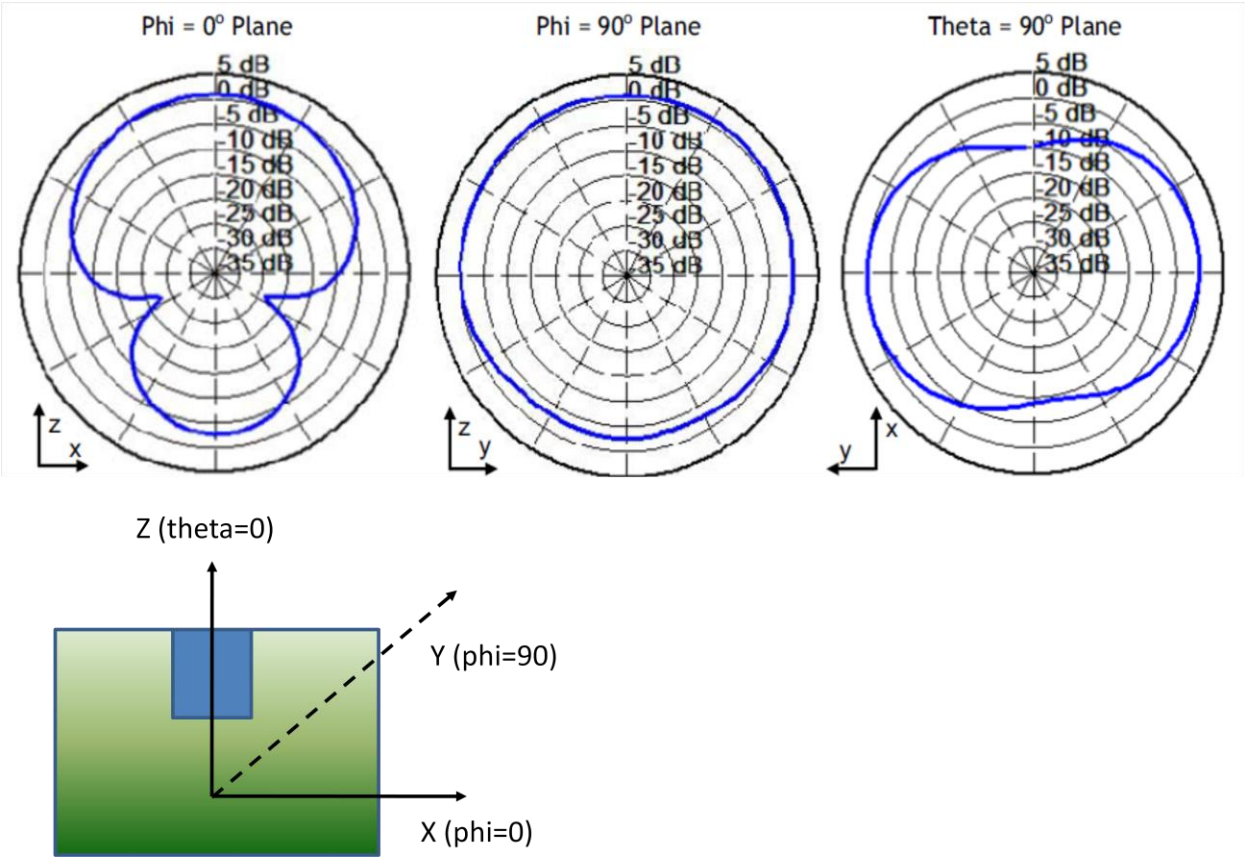



**Figure 14 Radiation pattern of the embedded antenna, 80x40mm ground plane**

Avoid placement of the module at a corner of the mother board. This will reduce radiation efficiency and cause frequency shifts. Optimal placement is at center of top edge; keep at least 10mm distance to nearest ground plane corner.

Placement of tall nearby components (h>3mm) should keep minimum d=6mm distance to the embedded antenna. Also any adjacent conductive metal plane should have d=6mm distance to the top edge of the module. Enclosure or plastic cover should have minimum d=1.5mm distance to the antenna.

Placement near human body (or any biological tissue) is accepted by keeping minimum d=10mm distance between mother board and the body. With smaller distances to the body, the radiation efficiency of the antenna will start to reduce due to signal losses in biological tissue. E.g. d=5mm to biological tissue will reduce GPS signal levels by about 6dB. Note also that the body will act also as a reflector and thus radiation pattern will point perpendicular to the body.

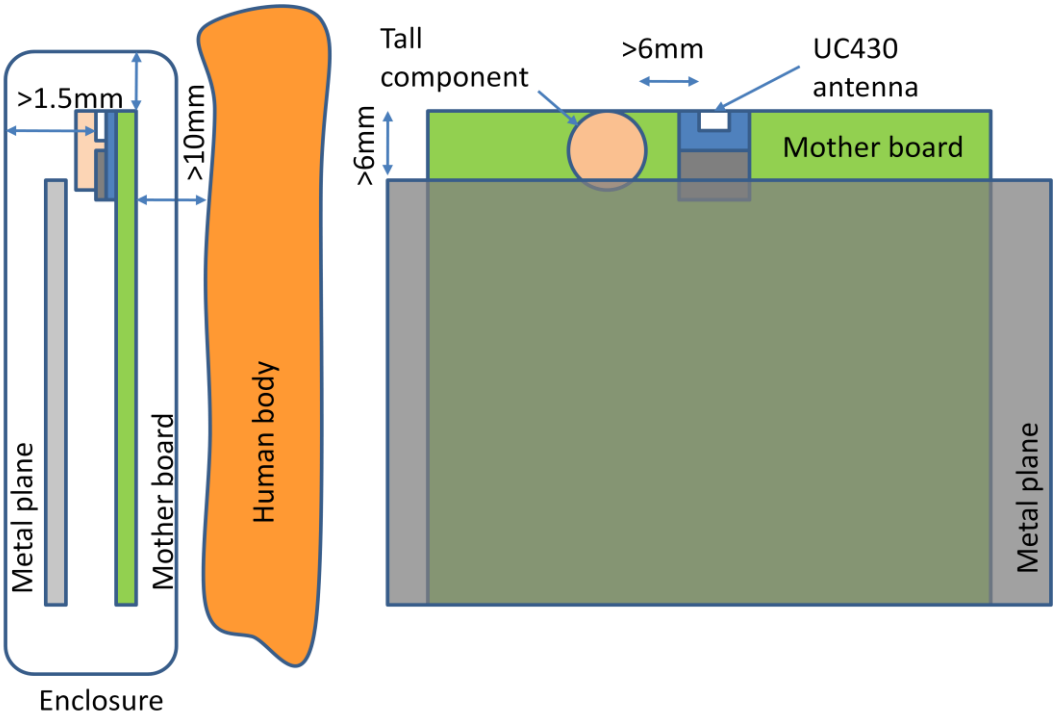



**Figure 15 Placement of UC430 relative to surroundings**

# 8 AC430 Application board for UC430

The Fastrax Application Board AC430 provides the UC430 connectivity to the Fastrax Evaluation Kit or to other evaluation purposes. It provides a single PCB board equipped with the UC430 module, 1.8V regulator, 1 Mbit EEPROM, MEMS accelerometer, 4 channel level translator for 1.8V I/O to 3.3V conversion, External GPS Antenna Switch + LNA, MCX antenna connector, Antenna Bias +3.3 V, Push-Button for ON_OFF control and 2x20 pin Card Terminal connector.

Default host port configuration is set to UART by switch S4… S8. Also connectivity to SPI and I2C host ports are supported via J3, see the AC430 circuit diagram for applicable switch settings.

**NOTE**

Note that UC430 module is sensitive to supply voltage ripple and thus current measurement instrument connected at J4 should have internal series resistance below 0.2 ohm; e.g. use 10A range in the instrument.

## 8.1 Board Terminal I/O-connector

The following signals are available at the 40-pin Card Terminal I/O connector J2. The same pin numbering applies also to the Fastrax Evaluation Kit pin header J4. Note that UART Port maps to serial Port 0 at the Fastrax Evaluation Kit. I/O signal levels are CMOS 3.3V compatible unless stated otherwise.

| Pin | Signal | I/O | Alternative GPIO name | Interface to Fastrax Evaluation Kit |
|---|---|---|---|---|
| 1 | - | - | - | Not connected |
| 2 | GND | - | - | Ground |
| 3 | - | - | - | Not connected |
| 4 | GND | - | - | Ground |
| 5 | TX_3V3 | O | TX | UART async. Output, VDD +3.3V |
| 6 | GND | - | - | Ground |
| 7 | RX | I | - | UART async. input |
| 8 | GND | - | - | Ground |
| 9 | VDD_3V3 | I | - | Power supply input +3.3V |
| 10 | GND | - | - | Ground |
| 11 | TM_3V3 | O | TM | 1PPS signal output, VDD +3.3V |
| 12 | GND | - | - | Ground |
| 13 | XRESET_3V3 | I | RESET_N | Active low async. system reset |
| 14 | - | - | - | Not connected |
| 15 | - | - | - | Not connected |
| 16 | - | I | - | Not connected |
| 17 | GND | - | - | Ground |
| 18 | - | - | - | Not connected |
| 19 | - | - | - | Not connected |
| 20 | - | - | - | Not connected |
| 21 | GND | - | - | Ground |
| 22 | - | - | - | Not connected |
| 23 | - | - | - | Not connected |
| 24 | - | - | - | Not connected |
| 25 | GND | - | - | Ground |

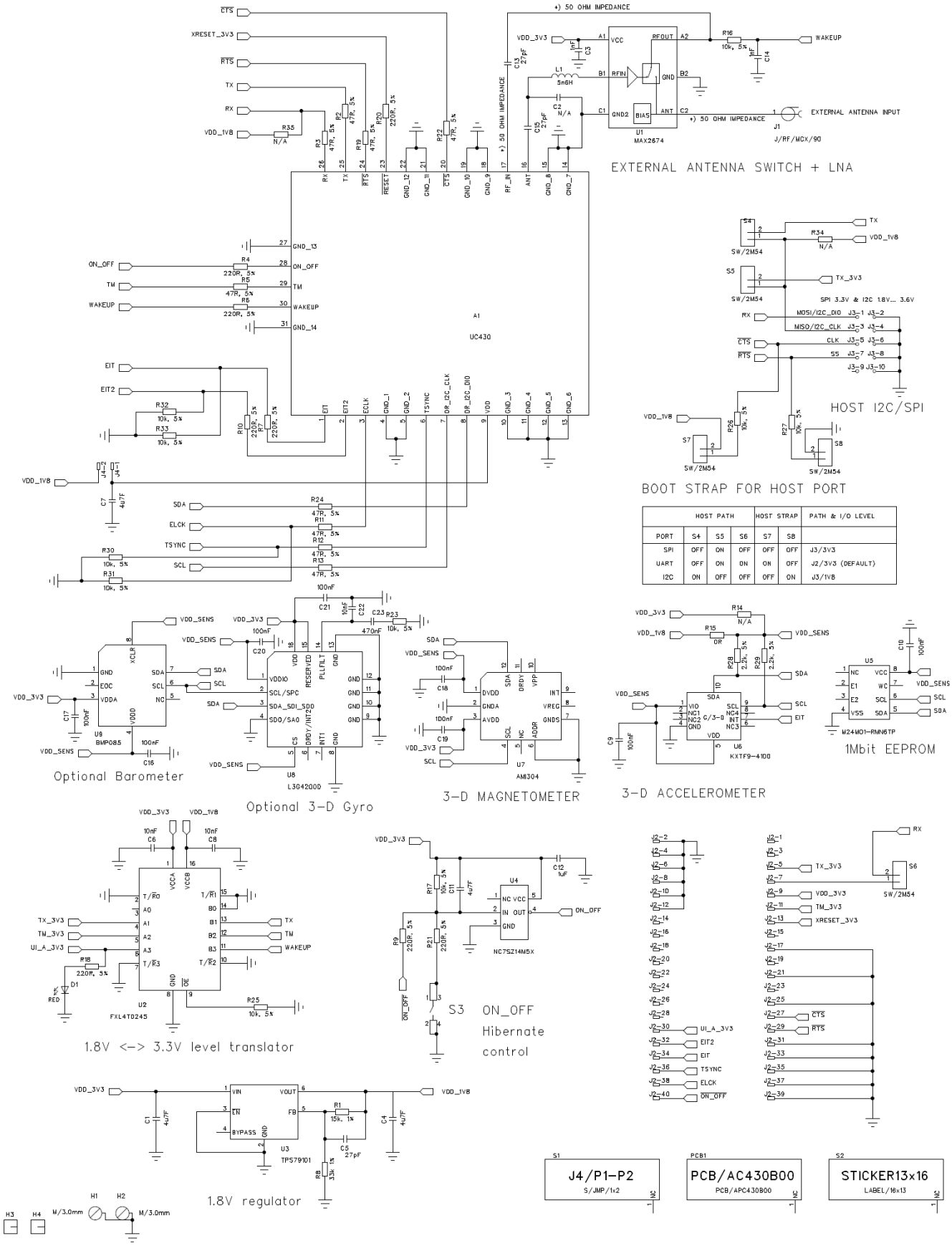
| Pin | Signal | I/O | Alternative GPIO name | Interface to Fastrax Evaluation Kit |
|---|---|---|---|---|
| 26 | - | - | - | Not connected |
| 27 | CTS | I | GPIO6 | UART CTS signal |
| 28 | - | - | - | Not connected |
| 29 | RTS | O | GPIO7 | UART RTS signal |
| 30 | UI_A_3V3 | O | WAKEUP | UI indicator A output, VDD +3.3V |
| 31 | GND | - | - | Ground |
| 32 | EIT2 | I | - | Interrupt EIT2 |
| 33 | GND | - | - | Ground |
| 34 | EIT | I | - | Interrupt EIT |
| 35 | GND | - | - | Ground |
| 36 | TSYNC | I | - | Timesync timing input |
| 37 | GND | - | - | Ground |
| 38 | ECLK | I/O | GPIO3 | ECLK clock input (or Message_Waiting output in SPI or UART handshaking host port modes) |
| 39 | GND | - | - | Ground |
| 40 | ON_OFF_N | I | ON_OFF (inv.) | Inverted ON_OFF control input, pulled up to VDD_3V3 |

## 8.2 Bill of materials

| DESIGNATOR | TECHNICALDESCRIPTION | VALUE |
|---|---|---|
| A1 | UC430 MODULE | UC430 |
| C1 | 4,7uF 6,3V X5R 0805 +-20% | 4u7F |
| C2 | Capacitor chip, 2.7pF 50V 5% NP0 0402 | N/A |
| C3 | Capacitor chip, 1nF 50V 10% X7R 0402 | 1nF |
| C4 | 4,7uF 6,3V X5R 0805 +-20% | 4u7F |
| C5 | Capacitor chip, 27pF 50V 5% NP0 0402 | 27pF |
| C6 | 10nF 50V 10% X7R 0402 | 10nF |
| C7 | 4,7uF 6,3V X5R 0805 +-20% | 4u7F |
| C8 | 10nF 50V 10% X7R 0402 | 10nF |
| C9 | Capacitor chip, 100nF 6.3V +-20% X5R 0402 | 100nF |
| C10 | Capacitor chip, 100nF 6.3V +-20% X5R 0402 | 100nF |
| C11 | 4,7uF 6,3V X5R 0805 +-20% | 4u7F |
| C12 | Capacitor chip, 1uF 6.3V +-20% X5R 0402 | 1uF |
| C13 | Capacitor chip, 27pF 50V 5% NP0 0402 | 27pF |
| C14 | Capacitor chip, 1nF 50V 10% X7R 0402 | 1nF |
| C15 | Capacitor chip, 27pF 50V 5% NP0 0402 | 27pF |
| C16 | Capacitor chip, 100nF 6.3V +-20% X5R 0402 | 100nF |
| C17 | Capacitor chip, 100nF 6.3V +-20% X5R 0402 | 100nF |
| C18 | Capacitor chip, 100nF 6.3V +-20% X5R 0402 | 100nF |
| C19 | Capacitor chip, 100nF 6.3V +-20% X5R 0402 | 100nF |
| C20 | Capacitor chip, 100nF 6.3V +-20% X5R 0402 | 100nF |
| C21 | Capacitor chip, 100nF 6.3V +-20% X5R 0402 | 100nF |
| C22 | 10nF 50V 10% X7R 0402 | 10nF |
| C23 | Capacitor chip, 470nF 6.3V +-10% X5R 0402 | 470nF |
| D1 | LED RED | TLSU1008 |
| H3 | FIDUCIAL, Circle, rectangle, triangle | FIDUCIAL |
| H4 | FIDUCIAL, Circle, rectangle, triangle | FIDUCIAL |
| J1 | 50 Ohm MCX connector, female, 90 Deg | MCX50 |
| J2 | EDGE MOUNT SOCKET STRIP 40 PINS | 2x20 edge |
| J3 | 2x5 pin-header, straight, 2.54mm | 2x5P2.54 |
| J4 | 1x2 pin-header, straight, pitch 2.54mm | 1x2P2.54 |
| L1 | Coil chip, 5.6nH 0402 +-5%, 300mA Q:8 0.26 DCR | 5n6H |

| | | |
|---|---|---|
| PCB1 | Application board for UC430 rev B00 | PCB/AC430B00 |
| R1 | Resistor chip, 15k 1% 0402 63mW | 15k, 1% |
| R2 | Resistor chip, 47R 0402 63mW 5% | 47R, 5% |
| R3 | Resistor chip, 47R 0402 63mW 5% | 47R, 5% |
| R4 | Resistor chip, 220R 5% 0402 63mW | 220R, 5% |
| R5 | Resistor chip, 47R 0402 63mW 5% | 47R, 5% |
| R6 | Resistor chip, 220R 5% 0402 63mW | 220R, 5% |
| R7 | Resistor chip, 220R 5% 0402 63mW | 220R, 5% |
| R8 | Resistor chip, 33k 1% 0402 63mW | 33k 1% |
| R9 | Resistor chip, 220R 5% 0402 63mW | 220R, 5% |
| R10 | Resistor chip, 220R 5% 0402 63mW | 220R, 5% |
| R11 | Resistor chip, 47R 0402 63mW 5% | 47R, 5% |
| R12 | Resistor chip, 47R 0402 63mW 5% | 47R, 5% |
| R13 | Resistor chip, 47R 0402 63mW 5% | 47R, 5% |
| R14 | Resistor chip, 0R 0402 | N/A |
| R15 | Resistor chip, 0R 0402 | 0R |
| R16 | Resistor chip, 10k 5% 0402 63mW | 10k, 5% |
| R17 | Resistor chip, 10k 5% 0402 63mW | 10k, 5% |
| R18 | Resistor chip, 220R 5% 0402 63mW | 220R, 5% |
| R19 | Resistor chip, 47R 0402 63mW 5% | 47R, 5% |
| R20 | Resistor chip, 220R 5% 0402 63mW | 220R, 5% |
| R21 | Resistor chip, 220R 5% 0402 63mW | 220R, 5% |
| R22 | Resistor chip, 47R 0402 63mW 5% | 47R, 5% |
| R23 | Resistor chip, 10k 5% 0402 63mW | 10k, 5% |
| R24 | Resistor chip, 47R 0402 63mW 5% | 47R, 5% |
| R25 | Resistor chip, 10k 5% 0402 63mW | 10k, 5% |
| R26 | Resistor chip, 10k 5% 0402 63mW | 10k, 5% |
| R27 | Resistor chip, 10k 5% 0402 63mW | 10k, 5% |
| R28 | Resistor chip, 2k2 5% 0402 63mW | 2.2k, 5% |
| R29 | Resistor chip, 2k2 5% 0402 63mW | 2.2k, 5% |
| R30 | Resistor chip, 10k 5% 0402 63mW | 10k, 5% |
| R31 | Resistor chip, 10k 5% 0402 63mW | 10k, 5% |
| R32 | Resistor chip, 10k 5% 0402 63mW | 10k, 5% |
| R33 | Resistor chip, 10k 5% 0402 63mW | 10k, 5% |
| R34 | Resistor chip, 1.5k 5% 0402 63mW | N/A |
| R35 | Resistor chip, 1.5k 5% 0402 63mW | N/A |
| S1 | Jumper, Pitch, 2.54mm, Red colour | J4/P1-P2 |
| S2 | Label 13x16mm iTrax03s | STICKER13x16 |
| S3 | Switch, SMD PUSH BUTTON | SW |
| S4 | Switch, on-off | SW JMP 2P54 |
| S5 | Switch, on-off | SW JMP 2P54 |
| S6 | Switch, on-off | SW JMP 2P54 |
| S7 | Switch, on-off | SW JMP 2P54 |
| S8 | Switch, on-off | SW JMP 2P54 |
| U1 | MAXIM MAX2674 GPS LNA + SWITCH | MAX2674 |
| U2 | Dual supply 4 bit translator with independent direction controls | FXL4TD245 |
| U3 | REGULATOR TPS79101 | TPS79101 |
| U4 | Schmit-Trigger inverter | NC7SZ14M5X |
| U5 | EEPROM 1Mbit, 1.8-5.5V, I2C, SO8N | M24M01-RMN6TP |
| U6 | Sensor, 3D Accelerometer, I2C interface, 1.8-3.6V | KXTF9-4100 |
| U7 | Sensor, 3D Magnetometer, I2C interface | AMI304 |
| U8 | Sensor, 3D Gyro, I2C interface | |
| U9 | Sensor, Barometer | |

## 8.3 AC 430 Circuit diagram




| HOST PATH | | | | HOST STRAP | | PATH & I/O LEVEL |
|---|---|---|---|---|---|---|
| PORT | S4 | S5 | S6 | S7 | S8 | |
| SPI | OFF | ON | OFF | OFF | OFF | J3/3V3 |
| UART | OFF | ON | ON | ON | OFF | J2/3V3 (DEFAULT) |
| I2C | ON | OFF | OFF | OFF | ON | J3/1V8 |

Figure 16 AC430 Circuit diagram

## 8.4 AC430 layout and assembly

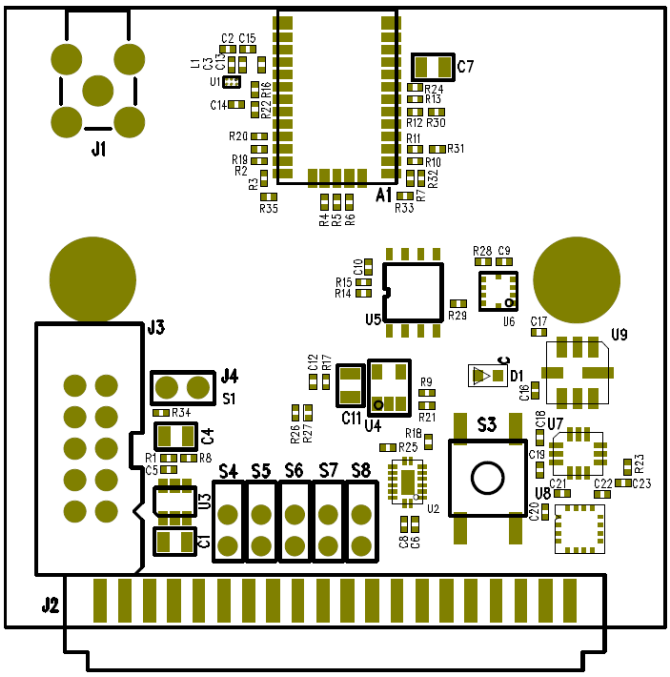



Figure 17 Assembly drawing, top side

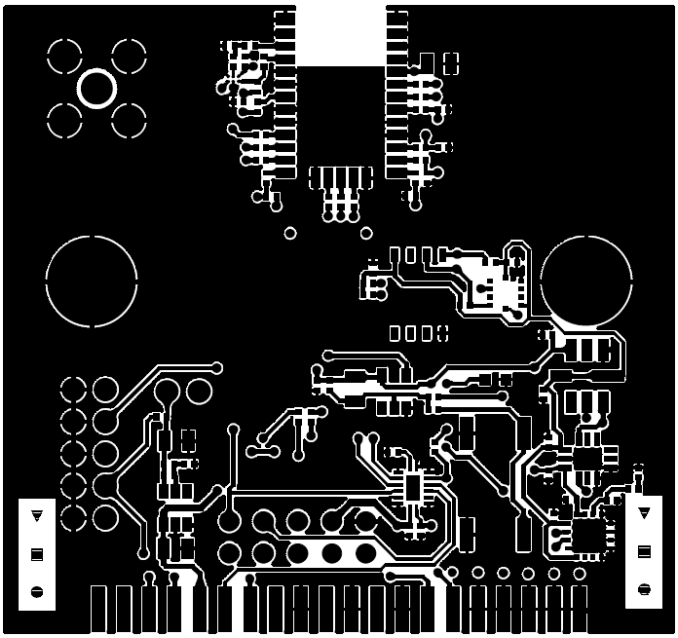


Figure 18 Layer 1, (top)

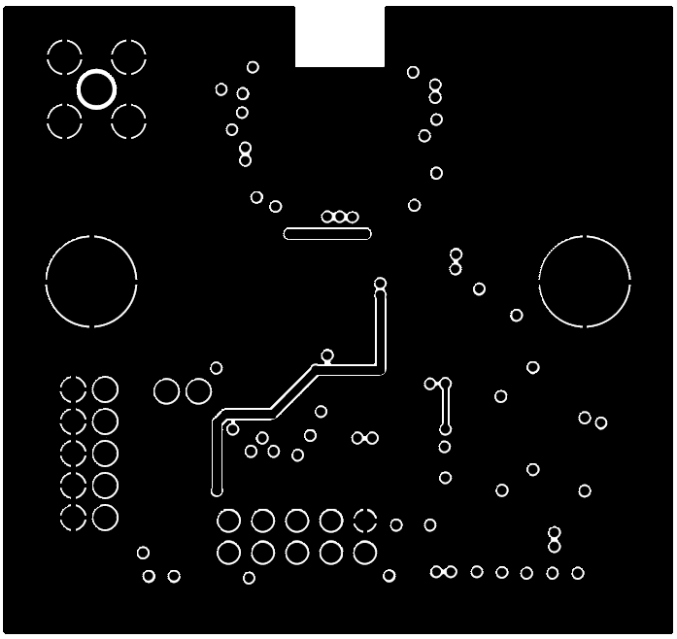


**Figure 19 Layer 2**

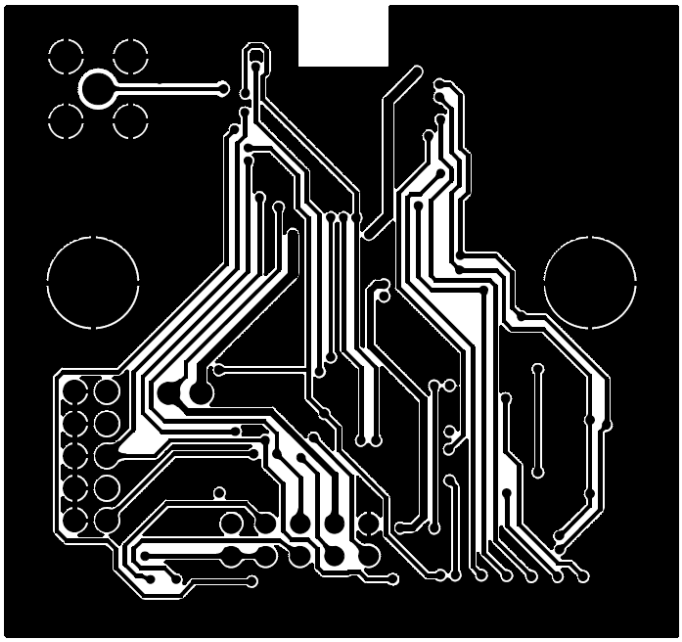


**Figure 20 Layer 3**

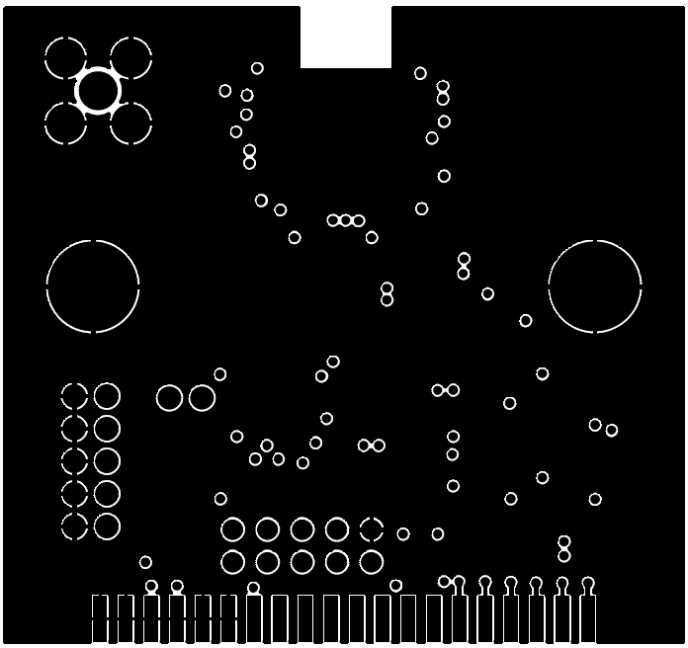


**Figure 21 Layer 4 (bottom)**

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**FR** - Pour connaître les tarifs et la disponibilité dans votre pays, cliquez sur l'un des liens suivants:

UC430

**EN**
This Datasheet is presented by the manufacturer

**DE**
Dieses Datenblatt wird vom Hersteller bereitgestellt

**FR**
Cette fiche technique est présentée par le fabricant