OpenVPX™ Trends and Updates

Greg Rocco, MIT Lincoln Laboratory

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LINCOLN LABORATORY
MASSACHUSETTS INSTITUTE OF TECHNOLOGY

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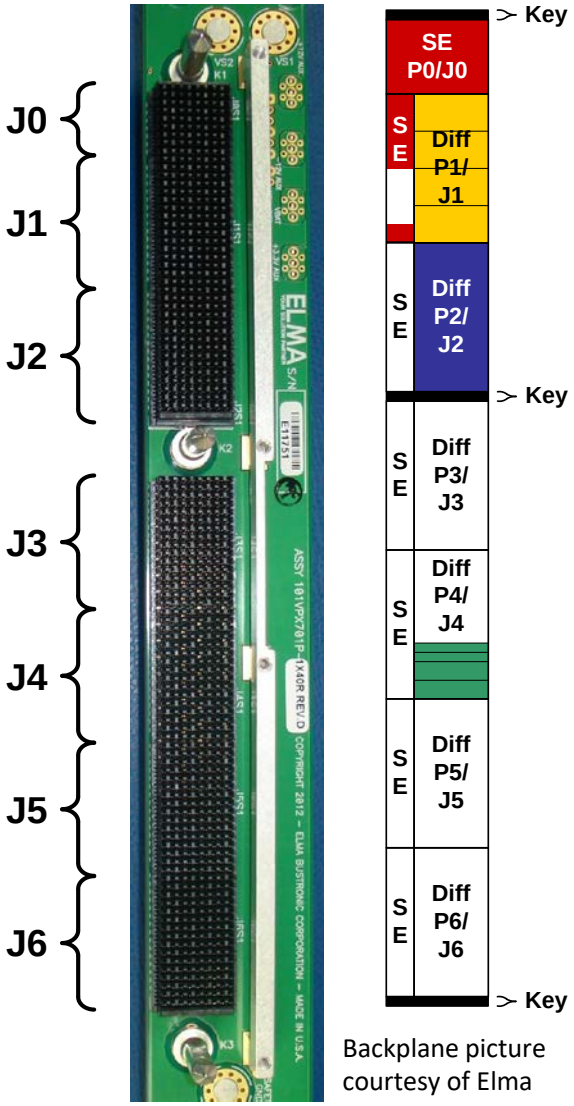
Outline

- **Review of ANSI/VITA 65.0-2017 and 65.1-2017**
  - With a focus on what is new
- **Relationship of OpenVPX with other standardization efforts**
- **Interoperability and User Defined pins**
  - Working to add Slot Profiles with very few or no User Defined pins



Backplane picture courtesy of Elma

A tutorial on OpenVPX and some other VITA standards is available at: http://www.vita.com/Tutorials

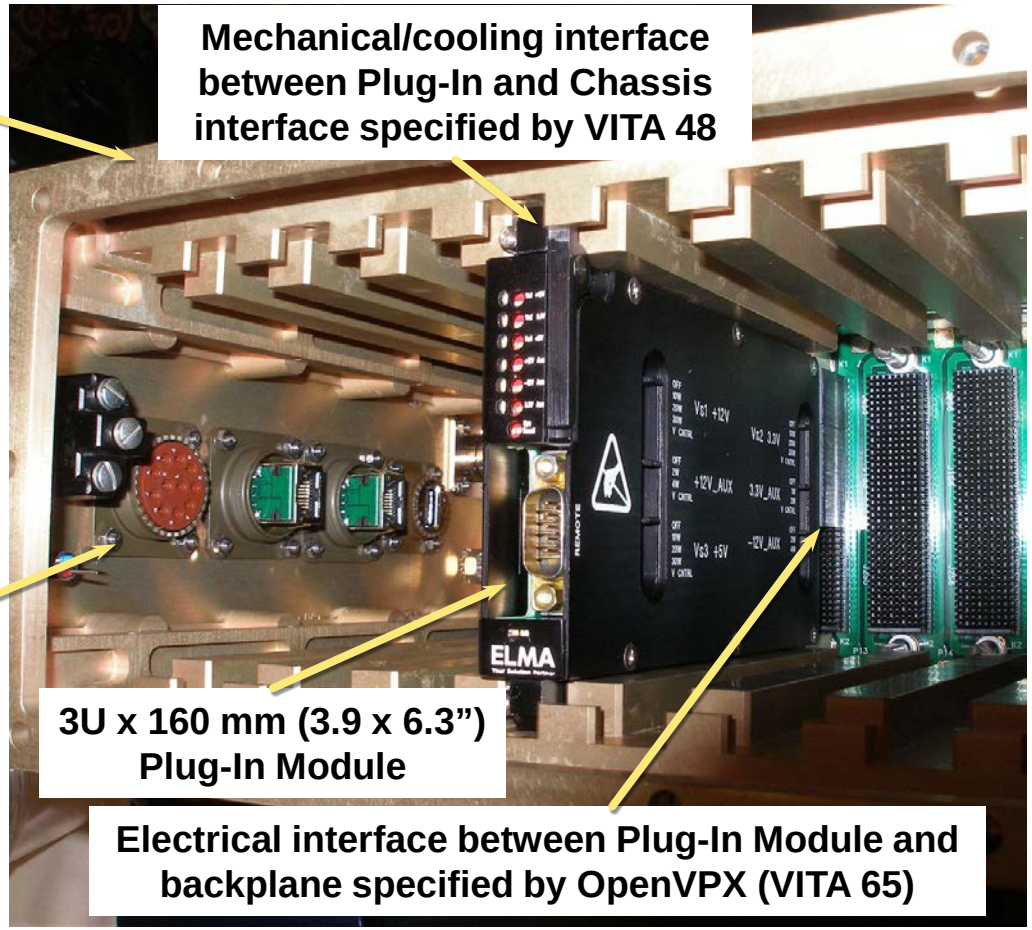
OpenVPX and Associated Standards

Conduction cooled chassis

Channels for cooling air

Chassis front panel

Pictures courtesy of Elma



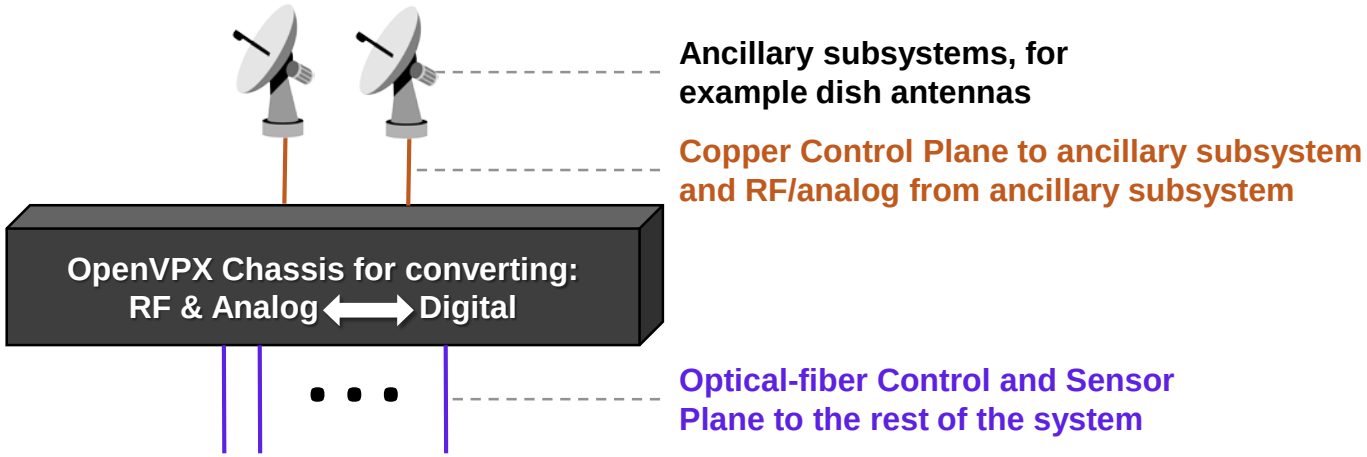
Mechanical/cooling interface between Plug-In and Chassis interface specified by VITA 48

3U x 160 mm (3.9 x 6.3”) Plug-In Module

Electrical interface between Plug-In Module and backplane specified by OpenVPX (VITA 65)

- These standards define interfaces between Plug-In Modules and chassis for products intended to be deployed in harsh environments

ANSI/VITA 65.0-2017 and 65.1-2017 Published Mid-2017

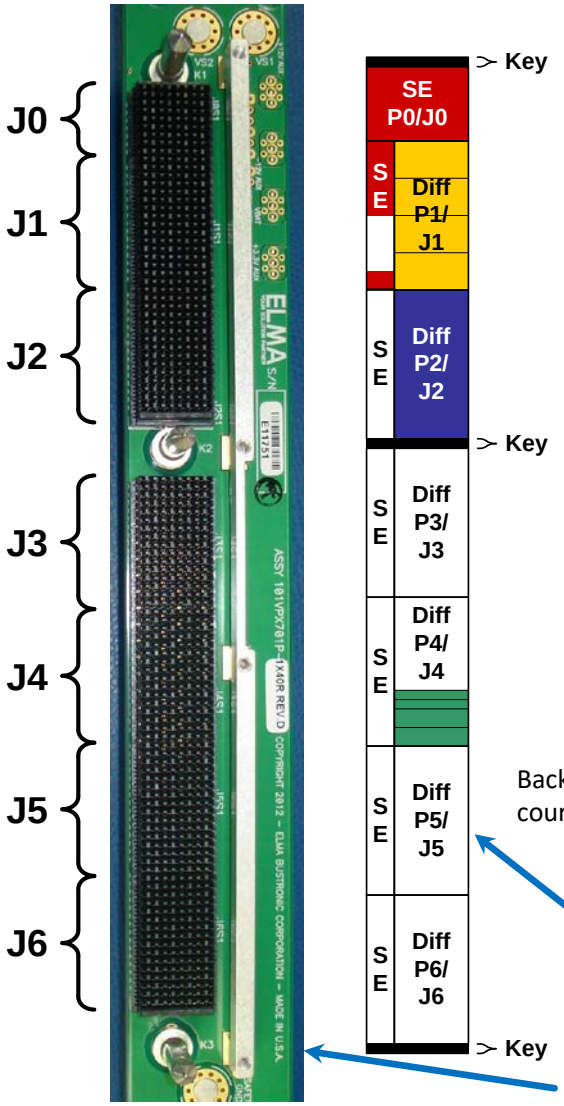


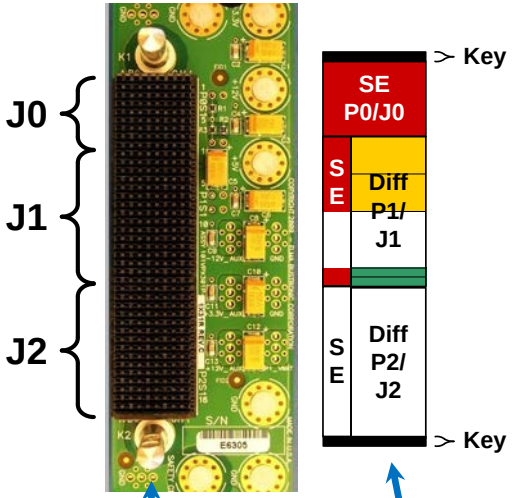
- **Initial versions of OpenVPX focused on processing subsystems**
- **The 2017 revision adds support of RF and data conversion subsystems**

- **Changes in 2017 revision to support RF and data conversion:**
  - **Option for Radial clocks or bussed clocks by slot**
  - **Optical (VITA 66.x) & coax (VITA 67.x) portions of backplane**
    - Organizational changes to handle significant expansion of optical/coax
  - **Control Plane Switch Profiles to support mix of:**
    - Copper connections within the chassis – 1000BASE-KX and 10GBASE-KR
    - Copper connections to local ancillary devices – 1000BASE-T and 10GBASE-T
    - Fiber connections to rest of system – 10GBASE-SR
  - **Data Plane Switch Profiles to support mix of:**
    - Copper connections within the chassis – 40GBASE-KR4
    - Fiber connections to rest of system – 40GBASE-SR4

- **Radial clocks enable applications needing much higher precision clocks than what bussed clocks can provide**
  - **Data conversion subsystems where groups of A/D and D/A converters are clocked at the same time**
  - **Precision time synchronization**
    - For time stamping, as is done for creation of VITA 49.0 data packets with timestamps
    - For controlling devices, such as receivers and exciters, using VITA 49.2

OpenVPX Profiles





3U OpenVPX 1-slot backplane

3U OpenVPX Slot Profile diagram
J0 – J2 are backplane connectors and
P0 – P2 are Plug-In Module connectors

Backplane pictures courtesy of Elma

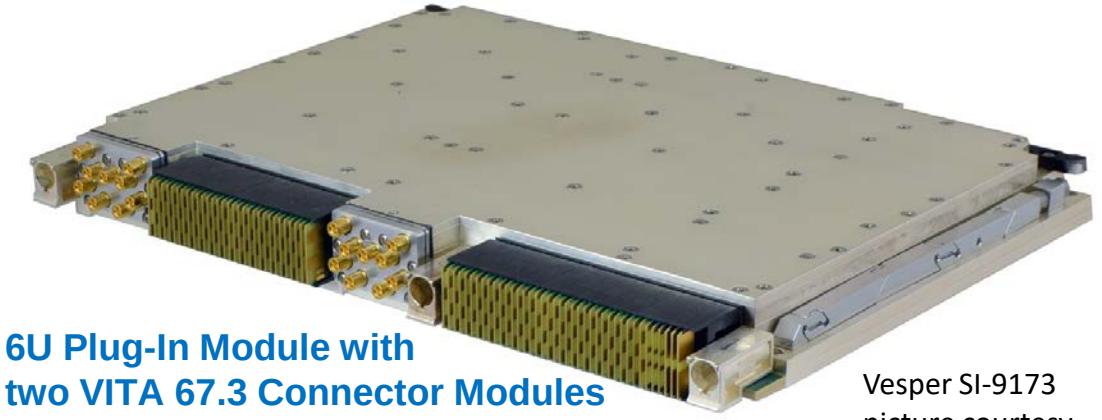
6U OpenVPX Slot Profile diagram
J0 – J6 are backplane connectors and
P0 – P6 are Plug-In Module connectors

6U OpenVPX 1-slot backplane

- **Slot Profiles specify**
  - Pins associated with a backplane slot
  - Pins associated with a Plug-In Module's connector to backplane
  - Assigns ports to groups of pins
  - Example Slot Profile name: SLT6-PAY-4F1Q2U2T-10.2.1
- **Backplane Profiles specify**
  - Which Slot Profiles a particular backplane has
  - How its Slot Profiles are interconnected
  - Example Backplane Profile name: BKP6-CEN16-11.2.2-n
- **Module Profiles specify**
  - The protocols and number of lanes to be mapped to the ports defined by the Slot Profile (e.g. 1000BASE-KX Ethernet)
  - Example Module Profile name: MOD6-PAY-4F1Q2U2T-12.2.1-n

Slot Profiles Now Have Dash Options

- **ANSI/VITA 65-2012 has tables of dash options for:**
  - Backplane Profiles – baud rates of channels
  - Module Profiles – protocols mapped to Slot Profile's ports
- **ANSI/VITA 65.0-2017 & 65.1 add dash options for Slot Profiles**
  - Slot Profiles can include aperture for optical/coax – for example: VITA 67.3 type C Connector Module
  - "-0" version of Slot Profile has aperture empty
  - Below are examples of Connector Modules that can go in a VITA 67.3 type C aperture. Each can be a dash option for Slot Profile.



- **6U Plug-In Module with two VITA 67.3 Connector Modules**
  - 9 SMPM contacts each
  - Mate with connector below (flipped vertically)
  - ANSI/VITA 65.0-2017 Slot Profile: SLT6-PAY-4F1Q1H2U2T1H-10.6.1-n

Vesper SI-9173 picture courtesy of Leonardo DRS

Image courtesy of TE Connectivity

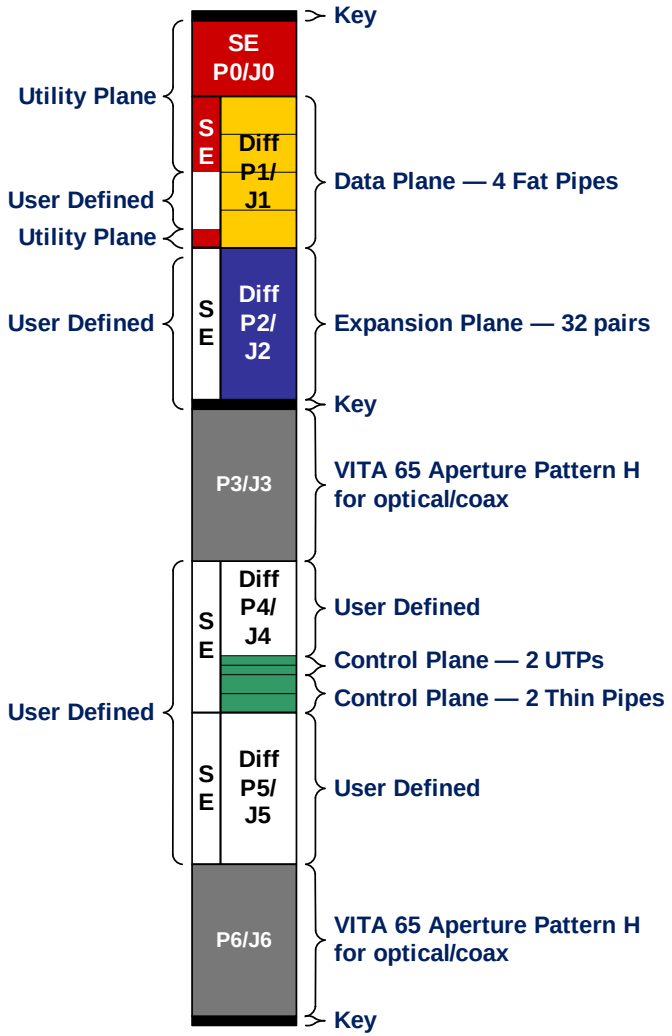
- **Backplane connector using VITA 67.3C footprint**
  - Can mate with Plug-In Modules with VITA 66.4 (optical) and 67.1 (coax) connectors
  - ANSI/VITA 65.1-2017 Connector Module definition: 9_SMPM_contacts-6.4.5.6.2

Picture courtesy of SV Microwave

- **VITA 67.3C backplane connector**
  - 9 SMPM contacts
  - Side which mates with Plug-in Module shown
  - ANSI/VITA 65.1-2017 Connector Module definition: 9_SMPM_contacts-6.4.5.6.2

VITA 65.0 and 65.1 Partitioning

- **Adding dash options to Slot Profiles also increases dash options for Backplane and Module Profiles as well as adding tables for Slot Profiles**
- **What was in ANSI/VITA 65-2012 is now in ANSI/VITA 65.0-2017 without the tables of dash options**
- **Tables of Backplane & Module Profile dash options moved to ANSI/VITA 65.1-2017**
  - Associated text stays in VITA 65.0
  - With VITA 65.0, instead of referencing tables in VITA 65.0, reference VITA 65.1
- **VITA 67.3 standardizes coax Connector Module footprints but not contact locations**
  - VITA 65.1 includes tables of contact locations
- **VITA 65.0 and 65.1 section numbers are consistent with each other**
  - VITA 65.1 has lots of skipped sections
- **VITA 65.1 written using Microsoft Excel in order to make dealing with tables easier**
  - Many of the tables are wider than what will nicely fit in the width of a page
  - Available in both Excel and .pdf



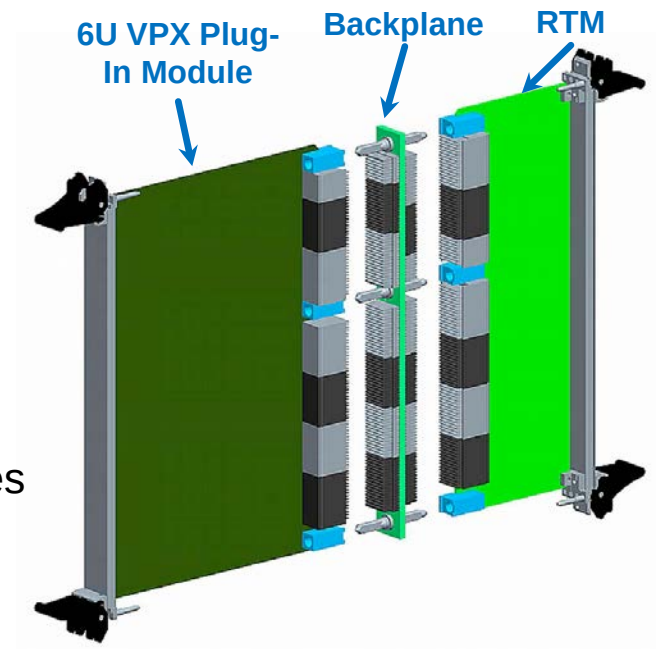
SLT6-PAY-4F1Q1H2U2T1H-10.6.1-n in ANSI/VITA 65.0-2017

Relationship of OpenVPX to Other Standardization Efforts

- **For next version of OpenVPX getting input from:**
  - SOSA (Sensor Open Systems Architecture) Hardware Working Group
  - HOST (Hardware Open Systems Technology) community of both those working on it and those using it
- **In SOSA we have discussions, which are ITAR controlled, to come up with best solutions in relation to target applications**
  - The VITA Standards Organization is international, so we cannot have discussion involving ITAR sensitive information
- **Working to align SOSA, HOST and OpenVPX**
  - In terms of Slot and Module Profiles, expect SOSA and HOST to be pointing at a subset of OpenVPX
  - Starting up effort to develop common approach to hardware management

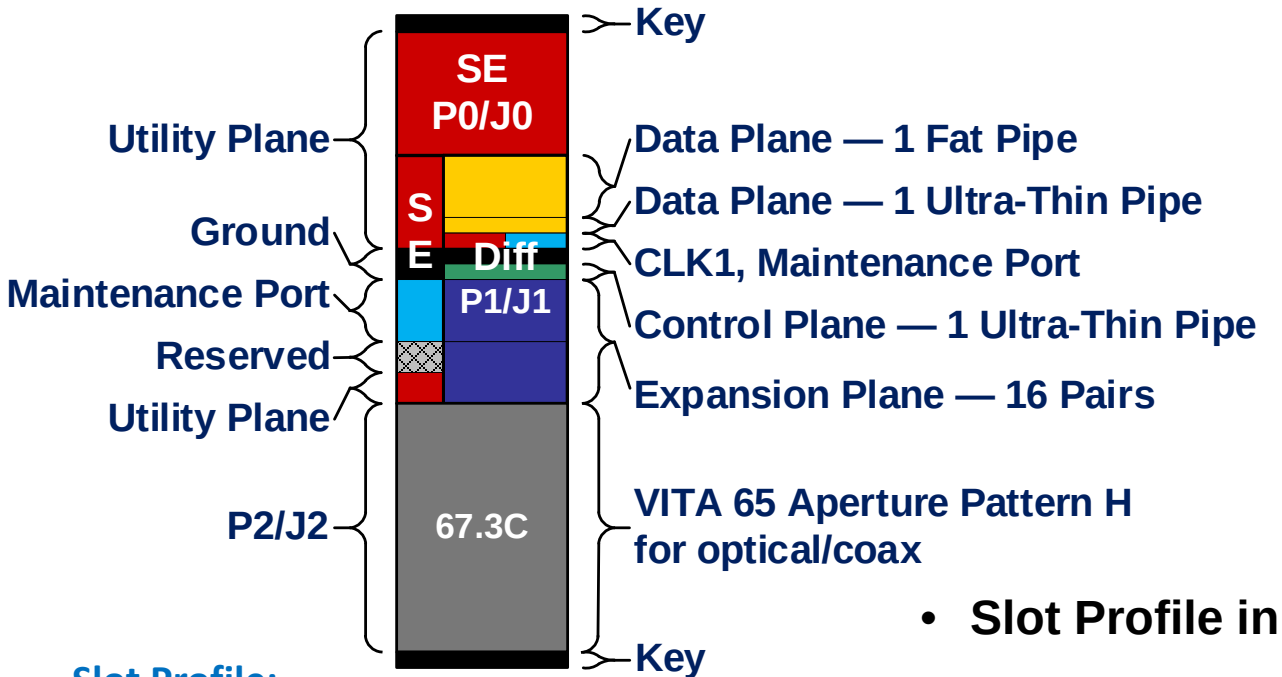
Interoperability – Dealing with User Defined Pins

- **In order to be able to use the same backplane with Plug-In Modules from multiple vendors, it is necessary to have a strategy for User Defined pins**
  - **Different suppliers likely to use UD pins differently – prevents interchangeability**
- **Some possible strategies for dealing with User Defined pins:**
  - **Do not use the them or do not have any**
  - **Use RTMs to connectorize them – not practical with many deployed systems**
  - **Have the backplane route them to a connector for a cable assembly which goes to internal side of chassis connectors**
    - Different versions of the cable assembly can be used to adapt to different Plug-In Modules
    - Jumpers on the backplane can be used to control which signals go to which pins of the connector for the cable assembly



- **There is a strong desire to be able to have backplane slots on deployed systems accept Plug-In Modules from multiple suppliers with no changes to backplane/chassis**
- **With next revision of OpenVPX will be adding more Slot Profiles with no User Define pins**

Common Payload Slot Profile for RF and Compute Intensive SBCs/FPGAs



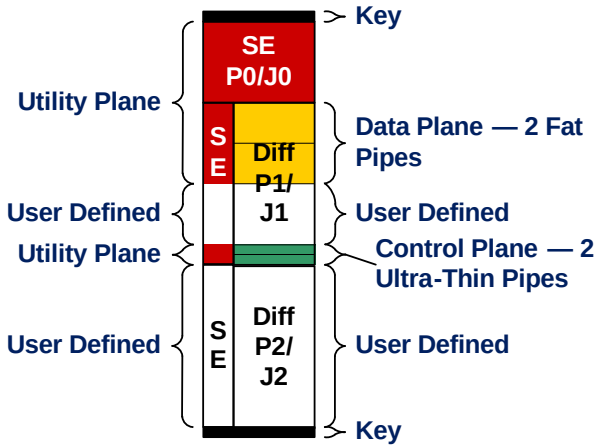
Slot Profile:
SLT3-PAY-1F1U1S1S1U1U2F1H-14.6.11-n
in ANSI/VITA 65.0-2017

3U Vesper SI-9172 picture courtesy of Leonardo DRS

- **Slot Profile in ANSI/VITA 65.0-2017 with no User Defined pins**
- **Intended for RF payloads and compute intensive SBCs & FPGAs**
  - Used by slots 4, 5, 8, 9 on of the Backplane Profile BKP3-TIM12-15.3.6-n
- **We will be adding more Slot Profiles with no User Defined pins**

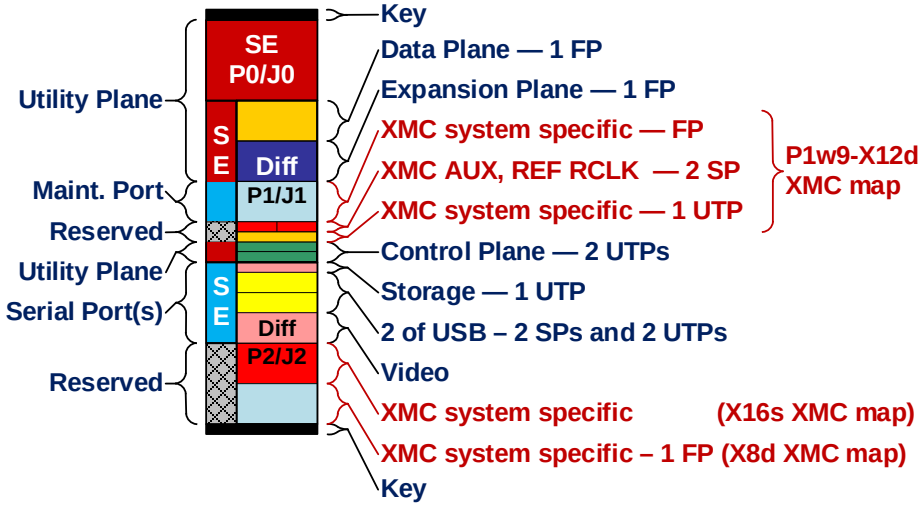
- **Use of this Slot Profile for compute intensive SBC and FPGA, as well as RF, Plug-In Modules, is a paradigm shift enabling easier configuration of systems**

Moving 3U I/O intensive SBCs to Slot Profiles with Fewer UD Pins



SLT3-PAY-2F2U-14.2.3 in ANSI/VITA 65.0-2017

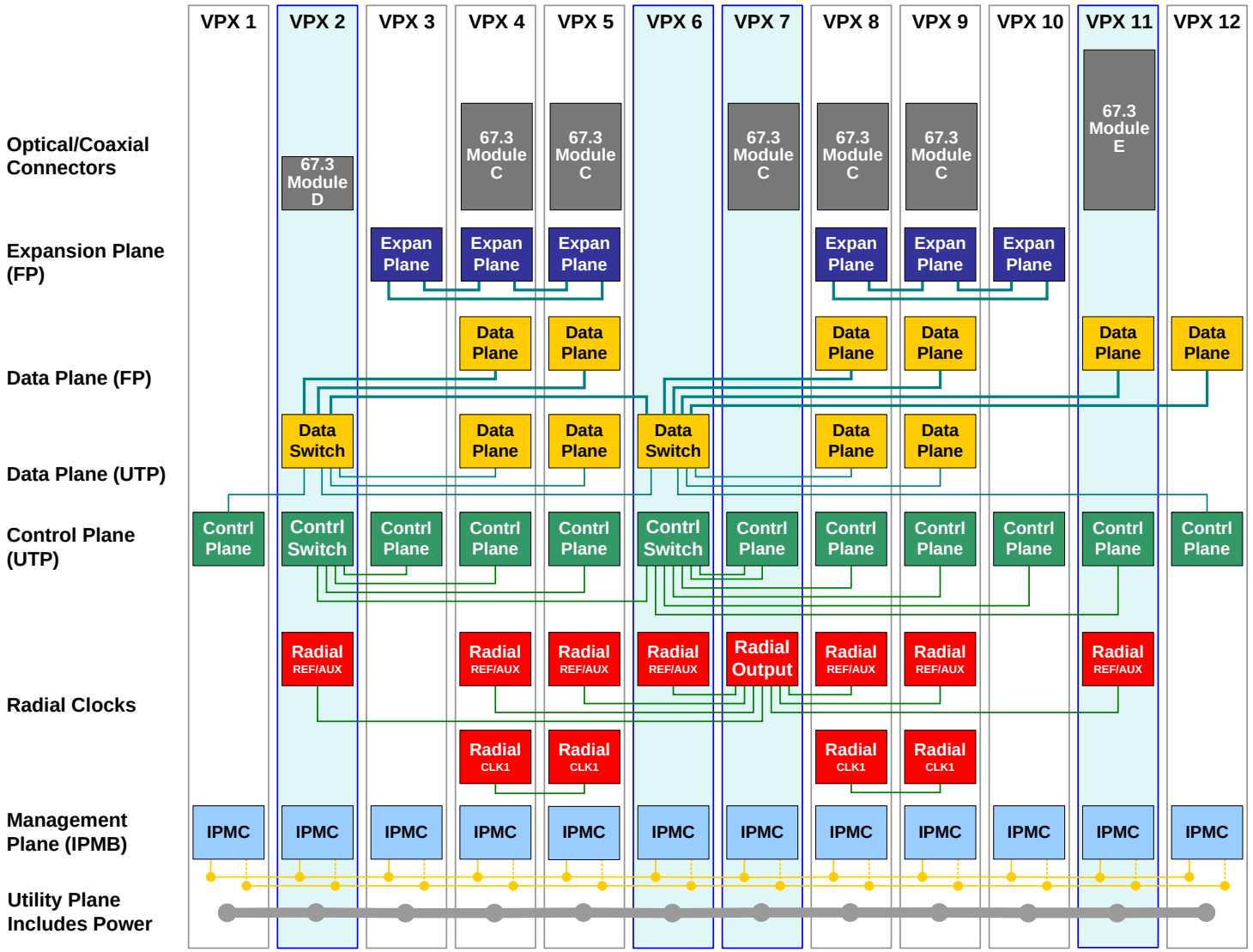
- **Existing Slot Profile has lots of User Defined pins**
  - A popular Slot Profile for SBCs
  - They get used differently by different suppliers and integrators
  - Creating inter-operability problems
  - Can have the effect of locking in suppliers and integrators
  - Slots 1, 3, 10, 12 of the Backplane Profile BKP3-TIM12-15.3.6-n
  - XMC used to customize for a particular system



Proposed SLT3-PAY-1F1F1F2S1U2U1U1S1U1S1U1T1F-14.2.17

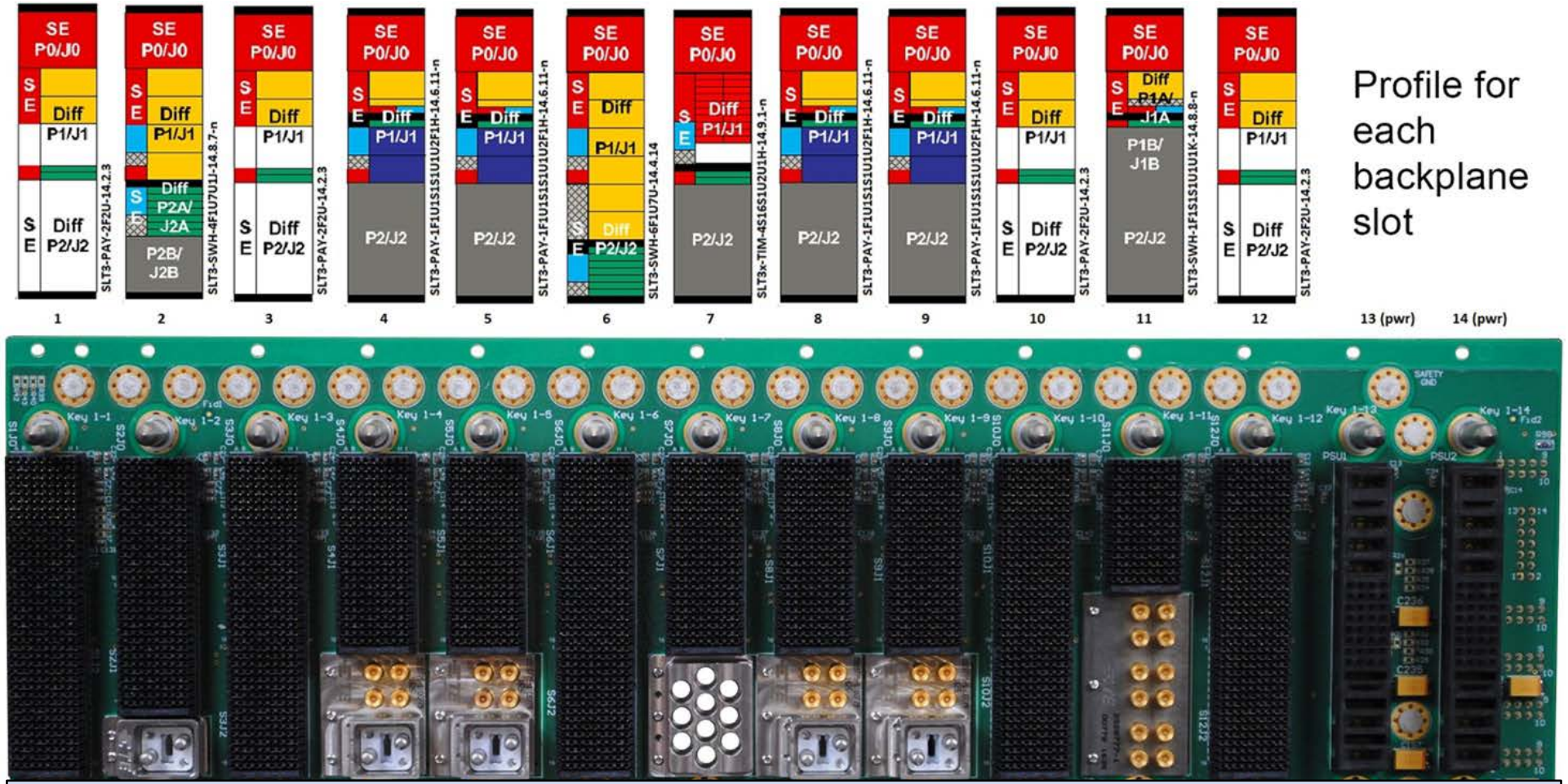
- **Slot Profile Working its way through proposal process**
  - Intended for I/O intensive SBCs
- **All defined, except pins intended to be used by XMC mappings**
  - XMC used to customize for a particular system

Existing 12-Slot 3U Backplane BKP3-TIM12-15.3.6-n



- **Slot 1, 3, 10, 12: SLT3-PAY-2F2U-14.2.3**
  - With slots 3 and 10 the Data Plane ports are being used on the Expansion Plane
- **Slots 2: SLT3x-SWH-4F1U7U1J-14.8.7-n**
  - Data and Control Plane switch with optical/coax
  - A Data Plane FP is repartitioned into 4 UTPs
- **Slots 4, 5, 8, 9: SLT3x-PAY-1F1U1S1S1U1U2F1H-14.6.11-n**
  - Payload slots with optical/coax
- **Slot 6: SLT3x-SWH-6F1U7U-14.4.14**
  - Data and Control Plane switch without optical/coax
  - A Data Plane FP is repartitioned into 4 UTPs
- **Slot 7: SLT3x-TIM-4S16S1U2U1H-14.9.1-n**
  - Radial clocks out
  - Generally also drives bussed clocks
  - Slots not receiving radial clocks have bussed clocks
- **Slot 11: SLT3x-SWH-1F1S1S1U1U1K-14.8.8-n**
  - Optical or RF Switch

Existing 12-Slot 3U Backplane BKP3-TIM12-15.3.6-n

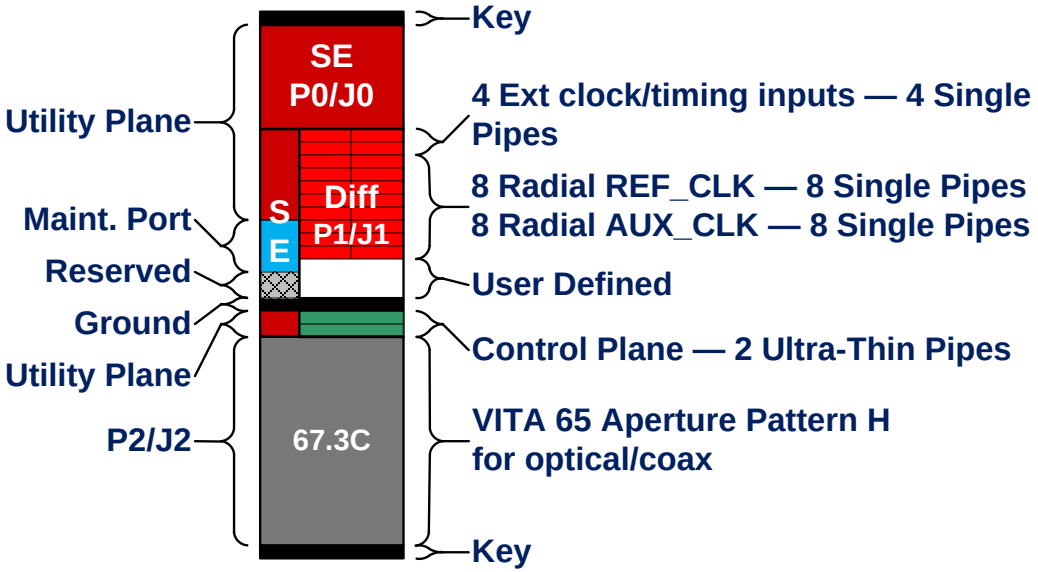


- **Slot 1, 3, 10, 12: SLT3-PAY-2F2U-14.2.3**
- **Slots 2: SLT3x-SWH-4F1U7U1J-14.8.7-1**
  - VITA 67.3D footprint for Plug-In Modules with VITA 66.4
- **Slots 4, 5, 8, 9: SLT3x-PAY-1F1U1S1S1U1U2F1H-14.6.11-1**
  - VITA 67.3C footprint for Plug-In Modules with 66.4 and 66.1
- **Slot 6: SLT3x-SWH-6F1U7U-14.4.14**
- **Slot 7: SLT3x-TIM-4S16S1U2U1H-14.9.1-1**
  - VITA 67.3C with 10 coax contacts
- **Slot 11: SLT3x-SWH-1F1S1S1U1U1K-14.8.8-1**
  - VITA 67.3E footprint for Plug-In Modules with 3 of VITA 66.1

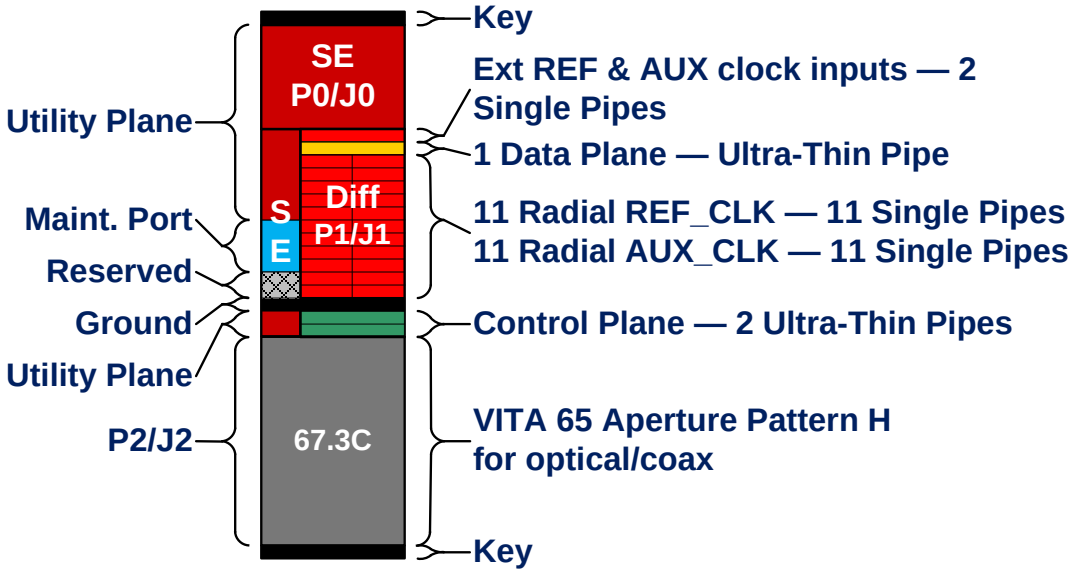
- **Examples of how some of the current thinking applies to this sort of backplane:**
  - Use slots like 4, 5, 8, 9 for either RF Payload Modules or compute intensive SBCs
  - Use slots like 1, 3, 10, 12 for I/O intensive SBCs, but with pin usage much more defined

Picture and Backplane Profile graphics courtesy of Elma for article used in, see: http://mil-embedded.com/articles/continued-found-recent-hardware-software-developments/

Family of Radial Clock Driving Slot Profiles



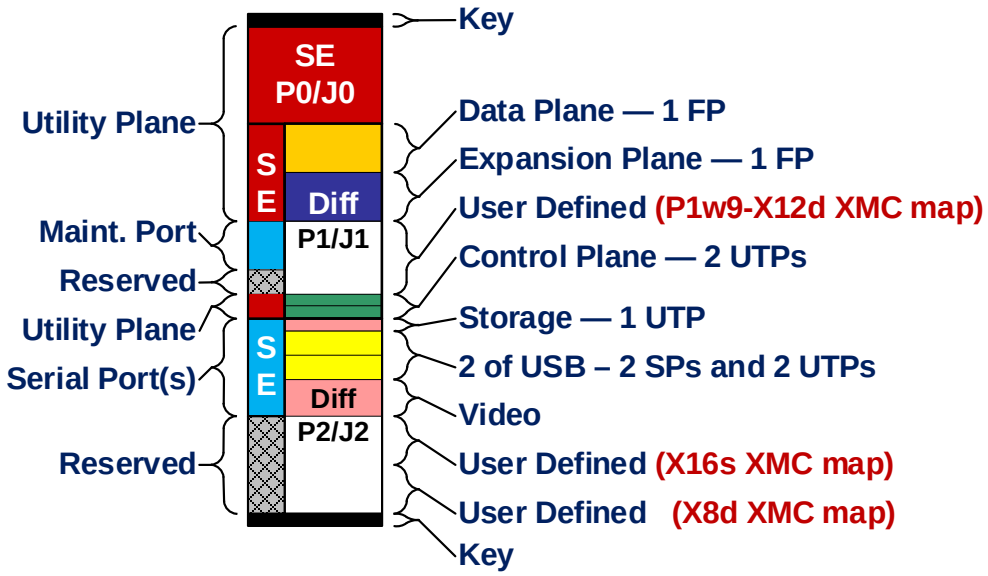
- **Existing: SLT3x-TIM-4S16S1U2U1H-14.9.1-n**
- **Existing Slot Profile in ANSI/VITA 65.0-2017**



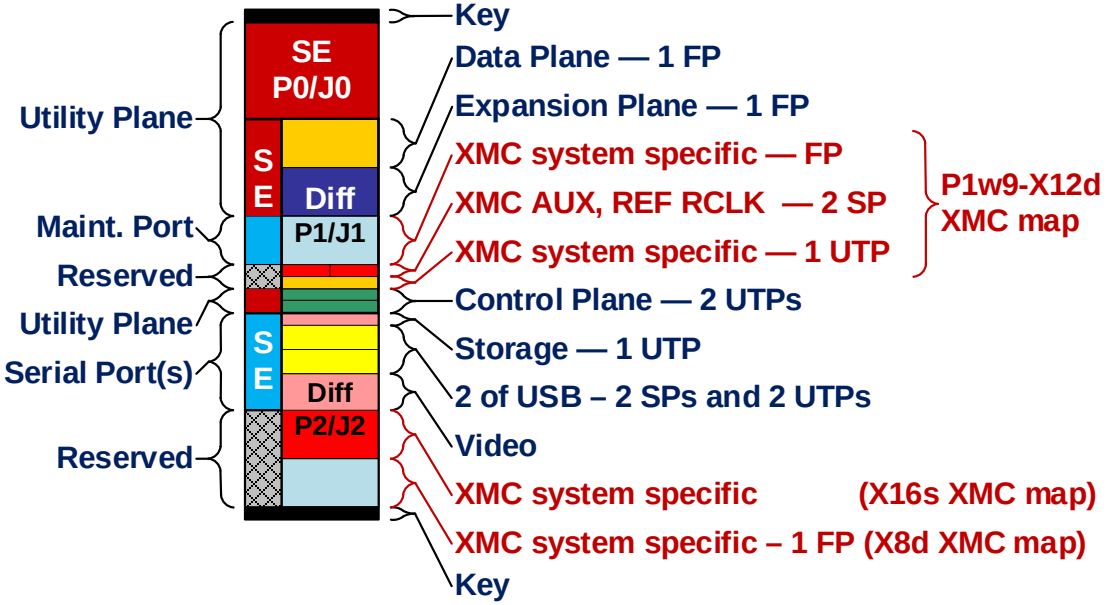
- **Proposed: SLT3x-TIM-2S1U22S1U2U1H-14.9.2-n**
- **Adds Data Plane UTP and 3 additional copies of REF_CLK and AUX_CLK outputs**

- **Slot Profile on right is early in the process of being proposed for the next version of OpenVPX**
  - Eliminates User Defined pins

Summary of Proposed I/O Intensive 3U SBC Slot Profiles



- **SLT3-PAY-1F1F2U1U1S1U1S1U1T-14.2.16**
- **User defined pins where XMC mapping can go – SBC with no XMC in place**

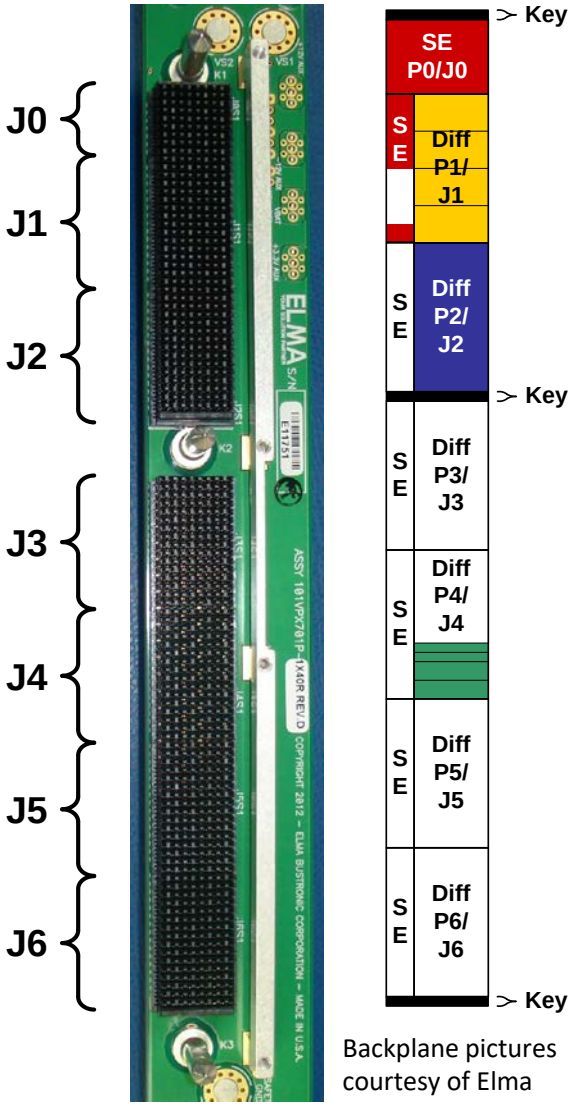


- **SLT3-PAY-1F1F1F2S1U2U1U1S1U1S1U1T1F-14.2.17**
- **SBC with XMC in place**

- **Slot Profiles intended for SBCs used for I/O intensive applications**
  - For SBCs which are computationally intensive suggest using SLT3-PAY-1F1U1S1S1U1U2F1H-14.6.11-n so RF and computation Plug-In Modules use same Slot Profile
  - XMC intended to personalize off-the-shelf SBC for particular systems – XMC maps to all remaining User Defined

Summary

- **ANSI/VITA 65.0-2017 and 65.1-2017 were published mid-2017**
  - Added option of clocks being radial
  - Much more extensive support for optical (ANSI/VITA 66.x) & coax (ANSI/VITA 67.x) portions of Slot Profiles
- **ANSI/VITA 65-2012 became 65.0 with profile tables moved to 65.1**
  - ANSI/VITA 65.0-2017; OpenVPX™ System Standard
  - ANSI/VITA 65.1-2017; OpenVPX™ System Standard – Profile Tables
- **SOSA and HOST communities being used to get input for next revision of OpenVPX standards**
- **User Defined pins can inhibit interoperability**
  - With next revision of OpenVPX standards adding more Slot Profiles with fewer or no User Defined pins



Backplane pictures courtesy of Elma